DL113
REV 6

MOTOROLA

MEMORY DATA

MOTOROLA MEMORY DATA

DATA CLASSIFICATION

Product Preview

This heading on a data sheet indicates that the device is in the formative stages or in design (under development). The disclaimer at the bottom of the first page reads: "This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice."

Advance Information

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MOTOROLA

MEMORIES

Prepared by
Technical Information Center

Motorola has developed a broad range of reliable memories for virtually any digital data processing system application. Complete specifications for the individual circuits are provided in the form of data sheets. In addition, a selector guide is included to simplify the task of choosing the best combination of circuits for optimum system architecture.

New Motorola memories are being introduced continually. For the latest releases, and additional technical information or pricing, contact your nearest authorized Motorola distributor or Motorola sales office.

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Selector Guide and Cross Reference

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DYNAMIC RAMs (HCMOS)

Density	Organi-zation	Motorola Part Number	Address Access Time (ns Max)	Operating Current (mA Max)	Pin Count	Package Options	Comments
1M	1Mx1	MCM511000A	70/80/100	80/70/60	18, 20, 20/26	(P)DIP, (Z)IP, SO(J)	Fast page mode cycle time=40/45/55 ns
		MCM51L1000A	70/80/100	80/70/60	18, 20, 20/26	(P)DIP, (Z)IP, SO(J)	Fast page mode with low power battery backup
		MCM511001A	70/80/100	80/70/60	18, 20, 20/26	(P)DIP, (Z)IP, SO(J)	Nibble mode access time=35/35/40 ns
		MCM511002A	70/80/100	80/70/60	18, 20, 20/26	(P)DIP, (Z)IP, SO(J)	Static column mode cycle time=40/45/55 ns
	256Kx4	MCM514256A	70/80/100	80/70/60	20, 20, 20/26	(P)DIP, (Z)IP, SO(J)	Fast page mode cycle time=40/45/55 ns
		MCM51L4256A	70/80/100	80/70/60	20, 20, 20/26	(P)DIP, (Z)IP, SO(J)	Fast page mode with low power battery backup
		MCM514258A	70/80/100	80/70/60	20, 20, 20/26	(P)DIP, (Z)IP, SO(J)	Static column mode cycle time=40/45/55 ns
4M	4Mx1	MCM514100	80/100	100/85	20, 20/26	(Z)IP, SO(J)	Fast page mode cycle time=50/60 ns
		MCM51L4100	80/100	100/85	20, 20/26	(Z)IP, SO(J)	Fast page mode with low power battery backup
	1Mx4	MCM514400	80/100	105/90	20, 20/26	(Z)IP, SO(J)	Fast page mode cycle time=50/60 ns
		MCM51L4400	80/100	105/90	20, 20/26	(Z)IP, SO(J)	Fast page mode with low power battery backup
		MCM514410	80/100	105/90	20, 20/26	(Z)IP, SO(J)	Fast page mode with write per bit

DRAM MODULES (Contact DRAM Marketing for Custom DRAM Modules)

Density	Organi-zation	Motorola Part Number	Address Access Time (ns Max)	Operating Current (mA Max)	Pin Count	Package Options	Comments
8M	1Mx8	MCM81000	70/80/100	640/560/480	30	(S)IMM, (L)SIP	Fast page mode cycle time=40/45/55 ns
		MCM8L1001	70/80/100	640/560/480	30	(S)IMM, (L)SIP	Fast page mode with low power battery backup
		MCM81001	70/80/100	640/560/480	30	(S)IMM, (L)SIP	Nibble mode access time=35/35/40 ns
		MCM81002	70/80/100	640/560/480	30	(S)IMM, (L)SIP	Static column mode cycle time=40/45/55 ns
8M w/Parity	1Mx9	MCM91000	70/80/100	720/630/540	30	(S)IMM, (L)SIP, SG (gold)	Fast page mode cycle time=40/45/55 ns
		MCM9L1000	70/80/100	720/630/540	30	(S)IMM, (L)SIP, SG (gold)	Fast page mode with low power battery backup
		MCM91001	70/80/100	720/630/540	30	(S)IMM, (L)SIP	Nibble mode access time=35/35/40 ns
		MCM91002	70/80/100	720/630/540	30	(S)IMM, (L)SIP	Static column mode cycle time=40/45/55 ns
2M	256Kx8	MCM84256	70/80/100	160/140/120	30	(S)IMM	Fast page mode cycle time=40/45/55 ns
		MCM8L4256	70/80/100	160/140/120	30	(S)IMM	Fast page mode with low power battery backup
2M w/Parity	256Kx9	MCM94256	70/80/100	240/210/190	30	(S)IMM	Fast page mode cycle time=40/45/55 ns
		MCM9L4256	70/80/100	240/210/190	30	(S)IMM	Fast page mode with low power battery backup
4M	1Mx4	MCM41000	80/100	280/240	26	(Z)IMM	Fast page mode cycle time=40/45/55 ns
	4Mx1	MCM11400	80/100	90/80	26	(Z)IMM	Fast page mode cycle time=40/45/55 ns
32M	4Mx8	MCM84000	80/100	800/680	30	(S)IMM	Fast page mode cycle time=50/60 ns
		MCM8L4000	80/100	800/680	30	(S)IMM	Fast page mode cycle time=50/60 ns
32M w/Parity	4Mx9	MCM94000	80/100	900/765	30	(S)IMM	Fast page mode cycle time=50/60 ns
		MCM9L4000	80/100	900/765	30	(S)IMM	Fast page mode cycle time=50/60 ns
8M w/Parity	256Kx36	MCM36256	70/80/100	960/840/760	72	(S)IMM, SG (gold)	Fast page mode cycle time=40/45/55 ns
16M w/Parity	512Kx36	MCM36512	70/80/100	1920/1680/1520	72	(S)IMM, SG (gold)	Fast page mode cycle time=40/45/55 ns
32M w/Parity	1Mx36	MCM36100	80/100	1144/984	72	(S)IMM, SG (gold)	Fast page mode cycle time=40/45/55 ns
64M w/Parity	2Mx36	MCM36200	80/100	1120/960	72	(S)IMM, SG (gold)	Fast page mode cycle time=40/45/55 ns
8M w/Parity	256Kx40	MCM40256*	70/80/100	800/700/600	72	(S)IMM, SG (gold)	Same as MCM36xxx, for error correction applications
16M w/Parity	512Kx40	MCM40512*	70/80/100	820/720/620	72	(S)IMM, SG (gold)	Same as MCM36xxx, for error correction applications
32M w/Parity	1Mx40	MCM40100*	80/100	1050/900	72	(S)IMM, SG (gold)	Same as MCM36xxx, for error correction applications
64M w/Parity	2Mx40	MCM40200*	80/100	1070/920	72	(S)IMM, SG (gold)	Same as MCM36xxx, for error correction applications

*To be introduced.

Package Information:

P=26 pin, 300 mil, plastic dual-in-line package
J=26 pin, 300 mil, plastic small outline "J" lead package
Z=20 pin, 300 mil, plastic zig-zag In-line package, or 26 pin zig-zag in-line memory module
S=30 pad single-in-line memory module, or 72 pad single-in-line memory module
L=30 pin single-in-line memory module
SG=30 pad single-in-line memory module with gold pac

DUAL PORT VIDEO RAMs

Density	Organization	Motorola Part Number	Address Access Time (ns Max)	Operating Current (mA Max)	Pin Count	Package Options	Comments
1M	256Kx4	MCM524258A	100/120	140/150	28, 28	(Z)IP, SO(J)	Dual port VRAM with 512x4 SAM port, ta=25/35 ns
	128Kx8	MCM528128A	100/120	140/150	40, 40	(P)DIP, (Z)IP, SO(J)	Dual port VRAM with 256x8 SAM port, ta=25/35 ns

GENERAL STATIC RAMs (HCMOS unless otherwise noted)

Density	Organization	Motorola Part Number	Address Access Time (ns Max)	Operating Current (mA Max)	Pin Count	Packaging	Comments
16K	2Kx8	MCM2018AN	35/45/55	135	24	300 mil, (P)DIP	NMOS. Replaces TMM2019D, MCM2016HN, MCM2018N.
256K	32Kx8	MCM60256A	85/100/120	70	28	(P)DIP, (F)SOG	100 µA standby current
		MCM60L256A	70/85/100/120	70	28	(P)DIP, (F)SOG	30 µA standby current
		MCM60L256A-C	100	70	28	(P)DIP, (F)SOG	Industrial temperature range (–40° to +85°C), low power
		MCM60L256A-V	100	70	28	(P)DIP, (F)SOG	Extended temperature range (–40° to +105°C), low power
1M	128Kx8 Pseudo SRAM	MCM518128	100	60	32	(P)DIP, (F)&(SF)SOG	Built-in refresh, $\overline{CE1}$ & CE2
		MCM518129	100	60	32	(F)SOG	Built-in refresh, $\overline{CE}$ & CS
		MCM51L8128	80/100	70/60	32	(P)DIP, (F)&(SF)SOG	200 µA standby current, built-in refresh, $\overline{CE1}$ & CE2
		MCM51L8129	80/100	70/60	32	(F)SOG	200 µA standby current, built-in refresh, $\overline{CE}$ & CS
		MCM51LV8128	80/100	70/60	32	(P)DIP, (F)&(SF)SOG	200 µA standby current, built-in refresh, $\overline{CE1}$ & CE2
		MCM51LV8129	80/100	70/60	32	(F)SOG	200 µA standby current, built-in refresh, $\overline{CE}$ & CS

Package Information: P=28 & 32 pin, 600 mil, plastic dual-in-line package
F=28 pin, 330 mil, plastic small outline gullwing package or,
32 pin, 450 mil, plastic small outline gullwing package
SF=32 pin, 330 mil, plastic small outline gullwing package

FAST STATIC RAMs (70 ns or Faster)

Density	Organization	Motorola Part Number	Pin Count	Packaging (Package Width in mils)	Address/ Cycle Time (ns Max)	Operating Current (mA max)	Technology	Comments
16K	2Kx8	MCM2018A	24	300 PDIP	45/55	135	NMOS	Replaces TMM2019D, MCM2016HN, MCM2018N.
	4Kx4	MCM6268	20	300 PDIP	20/25/35/45/55	110/110/110/80/80	HCMOS	20 ns in warehouse stock.
		MCM6269	20	300 PDIP	20/25/35	110	HCMOS	Fast Chip Select access time=10/12/15 ns.
		MCM6270	24/22	300 SOJ/PDIP	20/25/35	110	HCMOS	Fast Output Enable access time=10/12/15 ns.
64K	8Kx8	MCM6264	28	300/400 SOJ/300 PDIP	35/45/55	100/90/80	HCMOS	Look for DSP and cache memory applications.
		MCM6264D	28	300/400 SOJ/300 PDIP	20/25	115/110	HCMOS	20 ns fast and 8 bits wide.
		MCM6264	28	300 PDIP/SOJ	15	140	HCMOS	15 ns fast and 8 bits wide.
		MCM6264C	28	300/400 SOJ/300 PDIP	35/45/55	100/90/80	HCMOS	Industrial temperature range, –40° to 85°C.
		MCM6264D-C	28	300/400 SOJ/300 PDIP	25/30	115/110	HCMOS	Industrial temperature range, –40° to 85°C.
		MCM6264C	28	300 PDIP/SOJ	20	140	HCMOS	Industrial temperature range, –40° to 85°C.
	8Kx9	MCM6265	28	300 SOJ/PDIP	15/20/25	140/130/120	HCMOS	Ideal for applications requiring parity.
	16Kx4	MCM6288	22	300 PDIP	12/15/20/25/35	150/140/120/120/110	HCMOS	12 ns devices have tDVWH=6 ns max.
		MCM6290	24	300 SOJ/PDIP	12/15/20/25/35	150/140/120/120/110	HCMOS	12 ns devices have Output Enable=6 ns max.
	64Kx1	MCM6287	24/22	300 SOJ/PDIP	12/15/20/25/35	150/140/130/120/110	HCMOS	Mainframe applications, can also be used for parity bit.
256K	32Kx8	MCM6206	28	400 SOJ/600 PDIP	30/35/45	130/125/115	HCMOS	Two chip control functions: Chip Enable and Output Enable.
		MCM6206	28	300 SOJ/PDIP	17/20/25/35	155/150/140/135	HCMOS	17 ns with full 10% power supply.
		MCM6206C	28	300 SOJ/PDIP	25/35/45	140/135/130	HCMOS	Industrial temperature range, –40° to 85°C.
		MCM6706	28	300 SOJ	10/12/15	180/170/160	BiCMOS	New, Motorola BiCMOS.
	32Kx9	MCM6205	32	300 SOJ/PDIP	17/20/25/35	155/150/140/135	HCMOS	Ideal for applications requiring parity.
		MCM6205C	32	300 SOJ/PDIP	25/35/45	140/135/130	HCMOS	Industrial temperature range, –40° to 85°C.

FAST STATIC RAMs (70 ns or Faster) (Continued)

Density	Organi-zation	Motorola Part Number	Pin Count	Packaging (Package Width in mils)	Address/ Cycle Time (ns Max)	Operating Current (mA max)	Tech-nology	Comments
256K	64Kx4	MCM6709	28	300 SOJ	10/12/15	180/170/160	BiCMOS	New, Motorola BiCMOS.
	256Kx1	MCM6207	24	300 SOJ/PDIP	15/20/25	150/140/130	HCMOS	15 ns 256K with separate I/0.
1M	128Kx8	MCM6226	32	400 SOJ/PDIP	25/30	150/140	HCMOS	1M fast static RAM.
	256Kx4	MCM6228	28	400 SOJ/PDIP	25/30	145/135	HCMOS	1M fast static RAM.

FAST STATIC RAM MODULES

Density	Organi-zation	Motorola Part Number	Pin Count	Packaging	Address/ Cycle Time (ns Max)	Operating Current (mA max)	Tech-nology	Comments
2M	64Kx32	MCM3264Z	64	ZIP	20/25/30	1200/1120/1040	HCMOS	Perfect for 32-bit system, JEDEC standard.
	256Kx8	MCM8256Z	60	ZIP	20/25/30	1200/1120/1040	HCMOS	JEDEC standard module, faster speeds possible.
3M	2x64Kx24	MCM2464Z	58	ZIP	22/27	1680/1560	HCMOS	Two banks of x24 memory.

APPLICATION SPECIFIC STATIC RAMs

Description	Organi-zation	Motorola Part Number	Pin Count	Packaging	Address/ Cycle Time (ns Max)	Operating Current (mA max)	Tech-nology	Comments
Cache Tag RAM	4Kx4	MCM4180	24/22	300 mil SOJ/PDIP	18/20/25	140	HCMOS	Fully compatible with Mostek MK41H80.
Cache Tag RAM with Status Bit Registers	4Kx4	MCM62350	24	300 mil SOJ/PDIP	18/20/25	140	HCMOS	Housekeeping bits function, active pull-up match output. Flash clearable.
		MCM62351	24	300 mil SOJ/PDIP	18/20/25	140	HCMOS	Housekeeping bits function, open drain match output. Flash clearable.
Synchronous Static RAM	16Kx4	MCM6293	28	300 mil SOJ/PDIP	20/25	140	HCMOS	Registered outputs for fully pipelined applications, separate I/O's.
		MCM6294	28	300 mil SOJ/PDIP	20/25	140	HCMOS	Registered outputs plus output enable, separate I/O's.
		MCM6295	28	300 mil SOJ/PDIP	25/30	140	HCMOS	Transparent outputs plus output enable, separate I/O's.
	64Kx4	MCM62980	28	300 mil SOJ	15/20	170	HCMOS	Large cache memory for RISC and CISC systems.
		MCM62982	28	300 mil SOJ	12/15	170	HCMOS	Registered outputs for two stage pipeline.
	16Kx16	MCM62990	52	PLCC	17/20	360	HCMOS	Designed for advanced RISC-CISC cache applications.
	4x64Kx1	MCM62981	32	300 mil SOJ	15/20	170	HCMOS	Cache memory parity RAM.
		MCM62983	32	300 mil SOJ	12/15	170/130	HCMOS	Registered outputs, cache memory parity RAM.
	4Kx10	MCM62963	44	PLCC	18/20/25	170	HCMOS	Same functionality as MCM6293.
	4Kx12	MCM62973	44	PLCC	18/20/25	170	HCMOS	Same functionality as MCM6293.
		MCM62974	44	PLCC	18/20/25	170	HCMOS	Same functionality as MCM6294.
		MCM62975	44	PLCC	25/30	170	HCMOS	Same functionality as MCM6295.
	32Kx9	MCM62940	44	PLCC	19/24	250	HCMOS	Burst mode for 040 applications.
		MCM62950	44	PLCC	20/25	250	HCMOS	Designed for advanced RISC-CISC cache applications.
		MCM62960	44	PLCC	17/20/25	180	HCMOS	Designed for SPARC™ applications. Functionally equivalent to CY7C157.
		MCM62486	44	PLCC	19/24	250	HCMOS	Burst mode for 486 applications.
		MCM62110	52	PLCC	15/20	250	HCMOS	Dual I/O's for 88110.
DSPRAM	8Kx24	MCM56824	52	PLCC	25/30/35	250/210/180	HCMOS	Designed for DSP56001 applications.
Latched Address SRAM	8Kx20	MCM62820	52	PLCC	23/30	240/185	HCMOS	Designed for MIPS R3000 cache.
	16Kx16	MCM62995	52	PLCC	17/20/25	360	HCMOS	DSP96000 memory applications. Can be used like any asynchronous SRAM, samples available now.

ELECTRICALLY ERASABLE PROGRAMMABLE READ ONLY MEMORY

Density	Organi-zation	Motorola Part Number	Address Access Time (ns Max)	Operating Current (mA Max)	Pin Count	Packaging	Comments
2K	256Kx8	MCM2814P	3.5 µs	10	8	(P)DIP	2 or 4 wire serial access, data protection after reset.

Package Information: P=8 pin, 300 mil

DYNAMIC RAMs

MOTOROLA	FUJITSU	HITACHI	INTEL	MICRON	MITSUBISHI	NEC	OKI	SAMSUNG	TI	TOSHIBA
1M×1	**1M×1**	**1M×1**	**1M×1**	**1M×1**	**1M×1**	**1M×1**	**1M×1**	**1M×1**	**1M×1**	**1M×1**
MCM511000A	MB81C1000	HM511000	P21010	MT4C1024	M5M41000	μPD421000	MSM511000	KM41C1000	TMS4C1024	TC511000A
MCM511001A	MB81C1001	HM511001		MT4C1025	M5M41001	μPD421001	MSM511001	KM41C1001	TMS4C1025	TC511001A
MCM511002A	MB81C1003	HM511002		MT4C1026	M5M41002	μPD421002	MSM511002	KM41C1002	TMS4C1027	TC511002A
MCM514256A	MB81C4256	HM514256	P21014	MT4C4256	M5M44256A	μPD424256	MSM514256	KM44C256	TMS44C256	TC514256A
MCM514258A	MB81C4258	HM514258		MT4C4258	M5M44258A	μPD424258	MSM514258	KM44C258		TC514258A
1M×4	**1M×4**	**1M×4**	**1M×4**	**1M×4**	**1M×4**	**1M×4**	**1M×4**	**1M×4**	**1M×4**	**1M×4**
MCM514400	MB814400	HM514400		MT4C4001	M5M44400	μPD424400		KM44C1000		TC514400
4M×4	**4M×4**	**4M×4**	**4M×4**	**4M×4**	**4M×4**	**4M×4**	**4M×4**	**4M×4**	**4M×4**	**4M×4**
MCM514100	MB814100	HM514100	T21040	MT4C1004	M5M44100	μPD424100		KM41C4000		TC514100

DYNAMIC RAM MODULES

MOTOROLA	FUJITSU	HITACHI	INTEL	MICRON	MITSUBISHI	NEC	OKI	SAMSUNG	TI	TOSHIBA
256K×8	**256K×8**	**256K×8**	**256K×8**	**256K×8**	**256K×8**	**256K×8**	**256K×8**	**256K×8**	**256K×8**	**256K×8**
MCM84256		HB56D25608		MT8C8256	MH25608B	MC-41256A8	MSC2304_S8		TM4256_8	
MCM8L4256										
256K×9	**256K×9**	**256K×9**	**256K×9**	**256K×9**	**256K×9**	**256K×9**	**256K×9**	**256K×9**	**256K×9**	**256K×9**
MCM94256	MB85240	HB56D25609		MT8C9256	MH25609B	MC-41256A8	MSC2304_S9		TM4256_9	
MCM9L4256										
1M×8	**1M×8**	**1M×8**	**1M×8**	**1M×8**	**1M×8**	**1M×8**	**1M×8**	**1M×8**	**1M×8**	**1M×8**
MCM81000S	MB85230	HB56A18		MT8C8024	MH1M08B0	MC-421000A8	MSC2313_S8	KMM581000	TM024GAD8	THM81000
MCM8L1000S			SM2101910							
MCM81001S	MB85231			MT8C8025	MH1M08B1	MC-421000B8				
MCM81002S				MT8C8026	MH1M08B2	MC-421000C8				
1M×9	**1M×9**	**1M×9**	**1M×9**	**1M×9**	**1M×9**	**1M×9**	**1M×9**	**1M×9**	**1M×9**	**1M×9**
MCM91000S	MB85235	HB56A19		MT8C9024	MH1M09B0	MC-421000A9	MSC2312_S9	KMM591000	TM024EAD9	THM91000
MCM9L1000S										
MCM91001S				MT8C9025	MH1M09B1	MC-421000B9				
MCM91002S	MB85237			MT8C9026	MH1M09B2	MC-421000C9				
256K×36	**256K×36**	**256K×36**	**256K×36**	**256K×36**	**256K×36**	**256K×36**	**256K×36**	**256K×36**	**256K×36**	**256K×36**
MCM36256		HB56D25636B		MT8C36256	MH25636BJ					THM362500
512K×36	**512K×36**	**512K×36**	**512K×36**	**512K×36**	**512K×36**	**512K×36**	**512K×36**	**512K×36**	**512K×36**	**512K×36**
MCM36512		HB56D51236B		MT8C36512	MH51236BJ					THM365120
4M×8	**4M×8**	**4M×8**	**4M×8**	**4M×8**	**4M×8**	**4M×8**	**4M×8**	4M×8	4M×8	4M×8
MCM84000		HB56A48								
MCM8L4000										
4M×9	**4M×9**	**4M×9**	**4M×9**	**4M×9**	**4M×9**	**4M×9**	**4M×9**	**4M×9**	**4M×9**	**4M×9**
MCM94000		HB56A49			MH4M090J		MSC2340_YS9			
MCM9L4000										

FAST STATIC RAMs

MOTOROLA♦	IDT	CYPRESS	MICRON	PERFORMANCE	HITACHI	FUJITSU	TOSHIBA	MITSUBISHI	SONY
4K×4	**4K×4**	**4K×4**	**4K×4**	**4K×4**	**4K×4**	**4K×4**	**4K×4**	**4K×4**	**4K×4**
MCM6268P20	IDT6168SA20P	CY7C168A-20PC	MT5C1604-20	P4C168-20PC					
MCM6268P25	IDT6168SA25P	CY7C168A-25PC	MT5C1604-25	P4C168-25PC	HM6268P-25	MB81C68A-25P			
MCM6269P20		CY7C169A-20PC		P4C169-20PC					
MCM6269P25		CY7C169A-25PC		P4C169-25PC		MB81C69A-25P			
MCM6270J20	IDT61970S20Y	CY7C170A-20VC	MT5C1605DJ-20						
MCM6270J25	IDT61970S25Y	CY7C170A-25VC	MT5C1605DJ-25						
MCM6270P20	IDT61970S20P	CY7C170A-20PC	MT5C1605-20	P4C170-20PC					
MCM6270P25	IDT61970S25P	CY7C170A-25PC	MT5C1605-25	P4C170-25PC					
8K×8	**8K×8**	**8K×8**	**8K×8**	**8K×8**	**8K×8**	**8K×8**	**8K×8**	**8K×8**	**8K×8**
MCM6264NJ15*		CY7C185-15VC	MT5C6408DJ-15				TC5588J-15		CXK5863AJ15
MCM6264NJ20*	IDT7164S20Y	CY7C185-20VC	MT5C6408DJ-20	P4C164-20JC			TC5588J-20		CXK5863AJ20
MCM6264NJ25*	IDT7164S25Y	CY7C185-25VC	MT5C6408DJ-25	P4C164-25JC			TC5588J-25		CXK5863J25/AJ25
MCM6264P15*		CY7C185-15PC	MT5C6408-15				TC5588P-15		CXK5863AP15
MCM6264P20*	IDT7164S20P	CY7C185-20PC	MT5C6408-20	P4C164-20PC			TC5588P-20		CXK5863AP20
MCM6264P25*	IDT7164S25P	CY7C185-25PC	MT5C6408-25	P4C164-25PC			TC5588P-25		CXK5863P25/AP25
8K×9	**8K×9**	**8K×9**	**8K×9**	**8K×9**	**8K×9**	**8K×9**	**8K×9**	**8K×9**	**8K×9**
MCM6265J15						MB82B79-15PJ	TC5589J-15		
MCM6265J20				P4C163-20JC		MB82B79-20PJ	TC5589J-20	M5M179P-35	
MCM6265P15							TC5589P-15		
MCM6265P20				P4C163-20PC			TC5589P-20		
16K×4	**16K×4**	**16K×4**	**16K×4**	**16K×4**	**16K×4**	**16K×4**	**16K×4**	**16K×4**	**16K×4**
MCM6288P12		CY7C164-12PC	MT5C6404-12	P4C188-12PC	HM6788HP-12				
MCM6288P15	IDT7188S15P	CY7C164-15PC	MT5C6404-15	P4C188-15PC	HM6788HP-15		TC55416P-15H	M5M5188BP-15	CXK5464AP15
MCM6288P20	IDT7188S20P	CY7C164-20PC	MT5C6404-20	P4C188-20PC	HM6788HP-20		TC55416P-20/P-20H	M5M5188BP-20	CXK5464AP20
MCM6288P25	IDT7188S25P	CY7C164-25PC	MT5C6404-25	P4C188-25PC	HM6788P-25	MB81C74-25P	TC55416P-25	M5M5188AP-25	CXK5464AP25
MCM6290J12		CY7C166-12VC	MT5C6405DJ-12	P4C198-12JC	HM6789HJP-12				
MCM6290J15	IDT6198S15Y	CY7C166-15VC	MT5C6405DJ-15	P4C198-15JC	HM6789HJP-15		TC55417J-15H	M5M5189BJ-15	CXK5465J15
MCM6290J20	IDT6198S20Y	CY7C166-20VC	MT5C6405DJ-20	P4C198-20JC	HM6789HJP-20		TC55417J-20/J-20H	M5M5189BJ-20	CXK5465J20
MCM6290J25	IDT6198S25Y	CY7C166-25VC	MT5C6405DJ-25	P4C198-25JC	HM6789JP-25	MB81C75-25PJ	TC55417J-25	M5M5189AJ-25	CXK5465J25
MCM6290P12		CY7C166-12PC	MT5C6405-12	P4C198-12PC	HM6789HP-12				
MCM6290P15	IDT6198S15P	CY7C166-15PC	MT5C6405-15	P4C198-15PC	HM6789HP-15		TC55417P-15	M5M5189BP-15	CXK5465P15
MCM6290P20	IDT6198S20P	CY7C166-20PC	MT5C6405-20	P4C198-20PC	HM6789HP-20		TC55417P-20/P-20H	M5M5189BP-20	CXK5465P20
MCM6290P25	IDT6198S25P	CY7C166-25PC	MT5C6405-25	P4C198-25PC	HM6789P-25	MB81C75-25P	TC55417P-25	M5M5189AP-25	CXK5465P25
64K×1	**64K×1**	**64K×1**	**64K×1**	**64K×1**	**64K×1**	**64K×1**	**64K×1**	**64K×1**	**64K×1**
MCM6287J12			MT5C6401DJ-12	P4C187-12JC	HM6787HJP-12				
MCM6287J15	IDT7187S15Y	CY7C187-15VC	MT5C6401DJ-15	P4C187-15JC	HM6787HJP-15			M5M5187BJ-15	CXK5164J15
MCM6287J20	IDT7187S20Y	CY7C187-20VC	MT5C6401DJ-20	P4C187-20JC	HM6787HJP-20			M5M5187BJ-20	CXK5164J20
MCM6287J25	IDT7187S25Y	CY7C187-25VC	MT5C6401DJ-25	P4C187-25JC	HM6787JP-25	MB81C71A-25PJ		M5M518JAJ-25	CXK5164J25
MCM6287P12			MT5C6401-12	P4C187-12PC	HM6787HP-12				
MCM6287P15	IDT7187S15P	CY7C187-15PC	MT5C6401-15	P4C187-15PC	HM6787HP-15			M5M5187BP-15	CXK5164P15
MCM6287P20	IDT7187S20P	CY7C187-20PC	MT5C6401-20	P4C187-20PC	HM6787HP-20			M5M5187BP-20	CXK5164P20
MCM6287P25	IDT7187S25P	CY7C187-25PC	MT5C6401-25	P4C187-25PC	HM6787HP-25	MB81C71A-25P		M5M518JAP-25	CXK5164P25

♦ P = 300 mil PDIP, J = 300 mil SOJ, unless otherwise noted

*MCM6264: NJ = 300 mil SOJ, J = 400 mil SOJ, P = 300 mil PDIP, WP = 600 mil PDIP

FAST STATIC RAMs (Continued)

MOTOROLA♦	IDT	CYPRESS	MICRON	PERFORMANCE	HITACHI	FUJITSU	TOSHIBA	MITSUBISHI	SONY
32K×8	**32K×8**	**32K×8**	**32K×8**	**32K×8**	**32K×8**	**32K×8**	**32K×8**	**32K×8**	**32K×8**
MCM6206NJ20**	IDT71256S20P	CY7C199-20	MT5C2568DJ-20	P4C1256-20JC			TC55328J-20		
MCM6206NJ25**	IDT71256S25P		MT5C2568DJ-25	P4C1256-25JC	HM6787JP-25	MB8289-25	TC55328J-25		CXK58255AJ25
MCM6206NP20**	IDT71256S20P	CY7C198-20		P4C1256-20PC			TC55328P-20		
MCM6206NP25**	IDT71256S25P		MT5C2568-25	P4C1256-25PC	HM6787P-25	MB81C71A-25	TC55328P-25		CXK58255AP25
MCM6706J12	71B256S12Y								
MCM6706J15	71B256S15Y								
MCM6706P12	71B256S12P								
MCM6706P15	71B256S15P								
32K×9	**32K×9**	**32K×9**	**32K×9**	**32K×9**	**32K×9**	**32K×9**	**32K×9**	**32K×9**	**32K×9**
MCM6205N20							TC55329J-20		
MCM6205NJ25	IDT71259S25Y								
MCM6205NP20							TC55329P-20		
MCM6205NP25	IDT71259S25P					MB8289-25			
64K×4	**64K×4**	**64K×4**	**64K×4**	**64K×4**	**64K×4**	**64K×4**	**64K×4**	**64K×4**	**64K×4**
MCM6208J15								M5M5258BJ-15	
MCM6208J20	IDT71258S20Y		MT5C2564DJ-20	P4C1258-20JC	HM6708JP-20		TC55464J-20	M5M5258BJ-20	
MCM6208J25	IDT71258S25Y	CY7C194-25VC	MT5C2564DJ-25	P4C1258-25JC	HM6708JP-25		TC55464J-25	M5M5258AJ-25	
MCM6208P15								M5M5258BP-15	
MCM6208P20	IDT71258S20P		MT5C2564-20	P4C1258-20PC	HM6708P-20		TC55464P-20	M5M5258BP-20	
MCM6208P25	IDT71258S25P	CY7C194-25PC	MT5C2564-25	P4C1258-25PC	HM6708P-25		TC55464P-25	M5M5258AP-25	
MCM6708P10									
MCM6708P12	IDT71B258S12P								
MCM6708J10									
MCM6708J12	IDT71B258S12Y								
MCM6708P10									
MCM6708P12	IDT61B928S12P								
MCM6709J10									
MCM6709J12	IDT61B928S12Y								
MCM6209J15									
MCM6209J20	IDT61298S20Y		MT5C2565DJ-20	P4C1298-20JC			TC55465J-20		
MCM6209J25	IDT61298S25Y	CY7C196-25VC	MT5C2565DJ-25	P4C1298-25JC			TC55465J-25		
MCM6209P15									
MCM6209P20	IDT61298S20P		MT5C2565-20	P4C1298-20PC			TC55465P-20		
MCM6209P25	IDT61298S25P	CY7C196-25PC	MT5C2565-25	P4C1298-25PC			TC55465P-25		
256K×1	**256K×1**	**256K×1**	**256K×1**	**256K×1**	**256K×1**	**256K×1**	**256K×1**	**256K×1**	**256K×1**
MCM6207J15									
MCM6207J20	IDT712575S20Y		MT5C2561DJ-20	P4C1257-20JC	HM6707JP-20				
MCM6207J25	IDT712575S25Y		MT5C2561DJ-25	P4C1257-25JC	HM6707JP-25			M5M5260AJ-25	
MCM6207P15								M5M5257BP-15	
MCM6207P20	IDT712575S20P	CY7C197-20PC	MT5C2561-20	P4C1257-20PC	HM6707P-20			M5M5257BP-20	
MCM6207P25	IDT712575S25P	CY7C197-25PC	MT5C2561-25	P4C1257-25PC	HM6707P-25			M5M5257AP-25	

♦ P = 300 mil PDIP, J = 300 mil SOJ, unless otherwise noted

**MCM6206: NJ = 300 mil SOJ, J = 400 mil SOJ, NP = 300 mil PDIP, P = 600 mil PDIP

FAST STATIC RAM
APPLICATION SPECIFIC MEMORIES

MOTOROLA♦	IDT	SGS	SARATOGA
4K×4 CACHE TAG COMPARATORS			
MCM4180J,P	IDT6178SY,SP	MK41H80N	SSL4180PC
16K×4 SYNCHRONOUS			
MCM6293J,P	IDT61593SY,SP		SSM7193J,P
MCM6294J,P	IDT61594SY,SP		SSM7194J,P
MCM6295J,P	IDT61595S25Y,P		SSM7195J,P

♦ P = 300 mil PDIP, J = 300 mil SOJ

FAST STATIC RAM
MODULES

MOTOROLA♦	CYPRESS	HITACHI
64K×32		
MCM3264-20		
MCM3264-25	CYM1831-25	
MCM3264-30	CYM1831-30	
256K×8		
MCM8256-20		
MCM8256-25	CYM1441-25	HB66A2568A-25
MCM8256-30		

♦ P = 300 mil PDIP, J = 300 mil SOJ

CMOS Dynamic RAMs

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DYNAMIC RAMs (HCMOS)

Density	Organization	Motorola Part Number	Address Access Time (ns Max)	Operating Current (mA Max)	Pin Count	Package Options
1M	1Mx1	MCM511000A	70/80/100	80/70/60	18, 20, 20/26	(P)DIP, (Z)IP, SO(J)
		MCM51L1000A	70/80/100	80/70/60	18, 20, 20/26	(P)DIP, (Z)IP, SO(J)
		MCM511001A	70/80/100	80/70/60	18, 20, 20/26	(P)DIP, (Z)IP, SO(J)
		MCM511002A	70/80/100	80/70/60	18, 20, 20/26	(P)DIP, (Z)IP, SO(J)
	256Kx4	MCM514256A	70/80/100	80/70/60	20, 20, 20/26	(P)DIP, (Z)IP, SO(J)
		MCM51L4256A	70/80/100	80/70/60	20, 20, 20/26	(P)DIP, (Z)IP, SO(J)
		MCM514258A	70/80/100	80/70/60	20, 20, 20/26	(P)DIP, (Z)IP, SO(J)
4M	4Mx1	MCM514100	80/100	100/85	20, 20/26	(Z)IP, SO(J)
		MCM51L4100	80/100	100/85	20, 20/26	(Z)IP, SO(J)
	1Mx4	MCM514400	80/100	105/90	20, 20/26	(Z)IP, SO(J)
		MCM51L4400	80/100	105/90	20, 20/26	(Z)IP, SO(J)
		MCM514410	80/100	105/90	20, 20/26	(Z)IP, SO(J)

MCM511000A
MCM51L1000A

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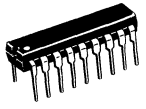
1M x 1 CMOS Dynamic RAM

Page Mode

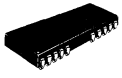
The MCM511000A is a 1.0μ CMOS high-speed, dynamic random access memory. It is organized as 1,048,576 one-bit words and fabricated with CMOS silicon-gate process technology. Advanced circuit design and fine line processing provide high performance, improved reliability, and low cost.

The MCM511000A requires only 10 address lines; row and column address inputs are multiplexed. The device is packaged in a standard 300-mil dual-in-line plastic package (DIP), a 300-mil SOJ plastic package, and a 100-mil zig-zag in-line plastic package (ZIP).

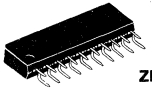
- Three-State Data Output
- Common I/O with Early Write
- Fast Page Mode
- Test Mode
- TTL-Compatible Inputs and Output
- $\overline{RAS}$ Only Refresh
- $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- Hidden Refresh
- 512 Cycle Refresh: MCM511000A = 8 ms
  MCM51L1000A = 64 ms
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}):
  MCM511000A-70 and MCM51L1000A-70 = 70 ns (Max)
  MCM511000A-80 and MCM51L1000A-80 = 80 ns (Max)
  MCM511000A-10 and MCM51L1000A-10 = 100 ns (Max)
- Low Active Power Dissipation:
  MCM511000A-70 and MCM51L1000A-70 = 440 mW (Max)
  MCM511000A-80 and MCM51L1000A-80 = 385 mW (Max)
  MCM511000A-10 and MCM51L1000A-10 = 330 mW (Max)
- Low Standby Power Dissipation:
  MCM511000A and MCM51L1000A = 11 mW (Max, TTL Levels)
  MCM511000A = 5.5 mW (Max, CMOS Levels)
  MCM51L1000A = 1.1 mW (Max, CMOS Levels)



P PACKAGE
300 MIL PLASTIC
CASE 707A



J PACKAGE
300 MIL SOJ
CASE 822

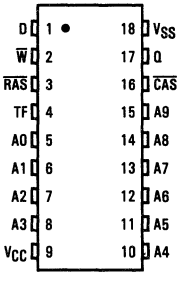


Z PACKAGE
PLASTIC
ZIG-ZAG IN-LINE
CASE 836

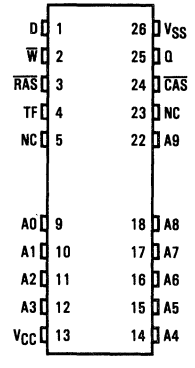
PIN NAMES	
A0-A9	Address Input
D	Data Input
Q	Data Output
$\overline{W}$	Read/Write Enable
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5 V)
V_{SS}	Ground
TF	Test Function Enable
NC	No Connection

PIN ASSIGNMENT

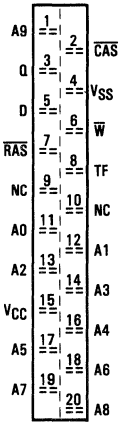
DUAL-IN-LINE



SMALL OUTLINE



ZIG-ZAG IN-LINE



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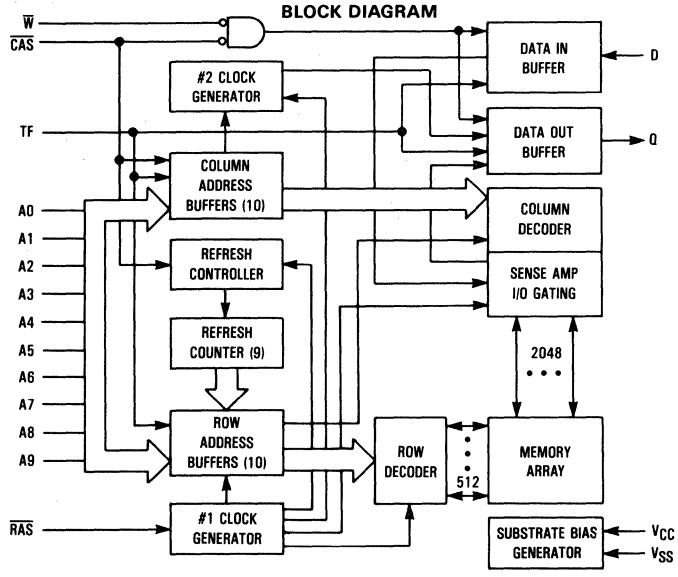
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−1 to +7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−1 to +7	V
Test Function Input Voltage	$V_{in(TF)}$	−1 to +10.5	V
Data Out Current	I_{out}	50	mA
Power Dissipation	P_D	600	mW
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V	1
	V_{SS}	0	0	0		
Logic High Voltage, All Inputs	V_{IH}	2.4	–	6.5	V	1
Logic Low Voltage, All Inputs	V_{IL}	−1.0	–	0.8	V	1
Test Function Input High Voltage	$V_{IH\ (TF)}$	V_{CC} + 4.5	–	10.5	V	1
Test Function Input Low Voltage	$V_{IL\ (TF)}$	−1.0	–	V_{CC} + 1.0	V	1

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current	I_{CC1}			mA	2
MCM511000A-70 and MCM51L1000A-70, t_{RC} = 130 ns		–	80		
MCM511000A-80 and MCM51L1000A-80, t_{RC} = 150 ns		–	70		
MCM511000A-10 and MCM51L1000A-10, t_{RC} = 180 ns		–	60		
V_{CC} Power Supply Current (Standby) ($\overline{RAS} = \overline{CAS} = V_{IH}$)	I_{CC2}	–	2.0	mA	
V_{CC} Power Supply Current During $\overline{RAS}$ only Refresh Cycles ($\overline{CAS} = V_{IH}$)	I_{CC3}			mA	2
MCM511000A-70 and MCM51L1000A-70, t_{RC} = 130 ns		–	80		
MCM511000A-80 and MCM51L1000A-80, t_{RC} = 150 ns		–	70		
MCM511000A-10 and MCM51L1000A-10, t_{RC} = 180 ns		–	60		
V_{CC} Power Supply Current During Fast Page Mode Cycle ($\overline{RAS} = V_{IL}$)	I_{CC4}			mA	2, 3
MCM511000A-70 and MCM51L1000A-70, t_{PC} = 40 ns		–	60		
MCM511000A-80 and MCM51L1000A-80, t_{PC} = 45 ns		–	50		
MCM511000A-10 and MCM51L1000A-10, t_{PC} = 55 ns		–	40		
V_{CC} Power Supply Current (Standby) ($\overline{RAS} = \overline{CAS} = V_{CC} - 0.2$ V) MCM511000A	I_{CC5}	–	1.0	mA	
MCM51L1000A		–	200	μA	
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle	I_{CC6}			mA	2
MCM511000A-70 and MCM51L1000A-70, t_{RC} = 130 ns		–	80		
MCM511000A-80 and MCM51L1000A-80, t_{RC} = 150 ns		–	70		
MCM511000A-10 and MCM51L1000A-10, t_{RC} = 180 ns		–	60		
V_{CC} Power Supply Current, Battery Backup Mode—MCM51L1000A only (t_{RC} = 125 μs; t_{RAS} = 1 μs; $\overline{CAS} = \overline{CAS}$ Before $\overline{RAS}$ Cycle or 0.2 V; A0-A9, $\overline{W}$, D = V_{CC} − 0.2 V or 0.2 V)	I_{CC7}	–	300	μA	
Input Leakage Current (Except TF) (0 V ≤ V_{in} ≤ 6.5 V)	$I_{lkg(I)}$	−10	10	μA	
Input Leakage Current (TF) (0 V ≤ $V_{in(TF)}$ ≤ V_{CC} + 0.5 V)	$I_{lkg(I)}$	−10	10	μA	
Output Leakage Current ($\overline{CAS} = V_{IH}$, 0 V ≤ V_{out} ≤ 5.5 V)	$I_{lkg(O)}$	−10	10	μA	
Test Function Input Current (V_{CC} + 4.5 V ≤ $V_{in(TF)}$ ≤ 10.5 V)	$I_{in(TF)}$	–	1	mA	
Output High Voltage (I_{OH} = −5 mA)	V_{OH}	2.4	–	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	–	0.4	V	

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Max	Unit	Notes
Input Capacitance	A0-A9, D	C_{in}	5	pF	4
	$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, TF		7	pF	4
Output Capacitance ($\overline{CAS} = V_{IH}$ to Disable Output)	Q	C_{out}	7	pF	4

NOTES:
1. All voltages referenced to V_{SS}.
2. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
3. Measured with one address transition per page mode cycle.
4. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\Delta t/\Delta V$.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ, WRITE, AND READ-WRITE CYCLES (See Notes 1, 2, 3, 4, and 5)

Parameter	Symbol		MCM511000A-70 MCM51L1000A-70		MCM511000A-80 MCM51L1000A-80		MCM511000A-10 MCM51L1000A-10		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	130	–	150	–	180	–	ns	6
Read-Write Cycle Time	t_{RELREL}	t_{RWC}	155	–	175	–	210	–	ns	6
Page Mode Cycle Time	t_{CELCEL}	t_{PC}	40	–	45	–	55	–	ns	
Page Mode Read-Write Cycle Time	t_{CELCEL}	t_{PRWC}	65	–	70	–	85	–	ns	
Access Time from $\overline{RAS}$	t_{RELQV}	t_{RAC}	–	70	–	80	–	100	ns	7, 8
Access Time from $\overline{CAS}$	t_{CELQV}	t_{CAC}	–	20	–	20	–	25	ns	7, 9
Access Time from Column Address	t_{AVQV}	t_{AA}	–	35	–	40	–	50	ns	7, 10
Access Time from Precharge $\overline{CAS}$	t_{CEHQV}	t_{CPA}	–	35	–	40	–	50	ns	7
$\overline{CAS}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	0	–	0	–	0	–	ns	7
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	20	0	20	0	20	ns	11
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{REHREL}	t_{RP}	50	–	60	–	70	–	ns	
$\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ Hold Time	t_{CELREH}	t_{RSH}	20	–	20	–	25	–	ns	
$\overline{CAS}$ Hold Time	t_{RELCEH}	t_{CSH}	70	–	80	–	100	–	ns	
$\overline{CAS}$ Pulse Width	t_{CELCEH}	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RELCEL}	t_{RCD}	20	50	20	60	25	75	ns	12
$\overline{RAS}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	35	15	40	20	50	ns	13
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	–	5	–	5	–	ns	
$\overline{CAS}$ Precharge Time (Page Mode Cycle Only)	t_{CEHCEL}	t_{CP}	10	–	10	–	10	–	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	–	0	–	0	–	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	–	10	–	15	–	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	–	0	–	0	–	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	–	15	–	20	–	ns	
Column Address Hold Time Referenced to $\overline{RAS}$	t_{RELAX}	t_{AR}	55	–	60	–	75	–	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{AVREH}	t_{RAL}	35	–	40	–	50	–	ns	

(continued)

NOTES:

1. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. TF pin must be at V_{IL} or open if not used.
6. The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. Measured with a current load equivalent to 2 TTL (−200 μA, +4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
8. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
9. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
10. Assumes that $t_{RAD} \geq t_{RAD}$ (max).
11. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
12. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
13. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.

READ, WRITE, AND READ-WRITE CYCLES (Continued)

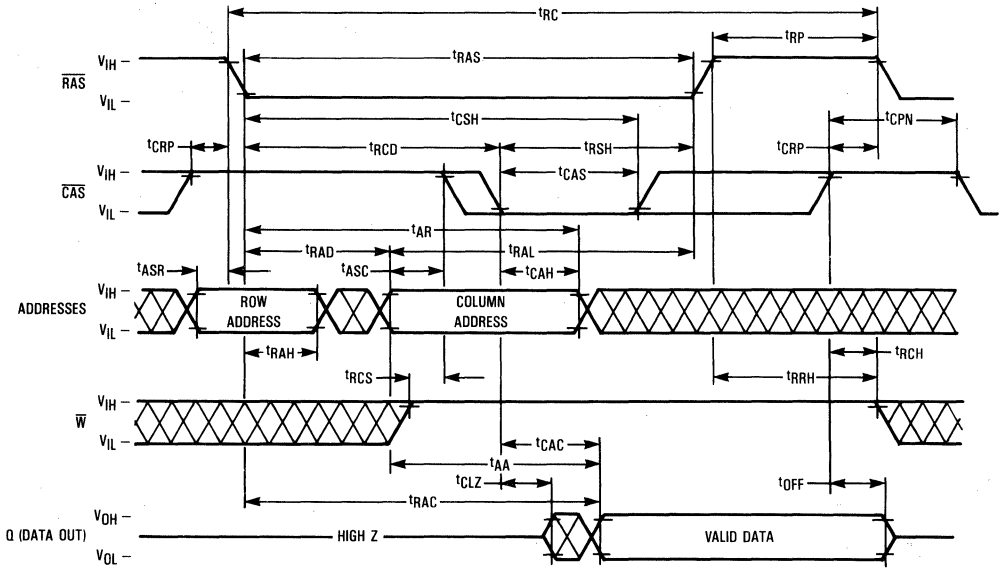
Parameter	Symbol		MCM511000A-70 MCM51L1000A-70		MCM511000A-80 MCM51L1000A-80		MCM511000A-10 MCM51L1000A-10		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	–	0	–	0	–	ns	
Read Command Hold Time Referenced to $\overline{CAS}$	t_{CEHWX}	t_{RCH}	0	–	0	–	0	–	ns	14
Read Command Hold Time Referenced to $\overline{RAS}$	t_{REHWX}	t_{RRH}	0	–	0	–	0	–	ns	14
Write Command Hold Time Referenced to $\overline{CAS}$	t_{CELWH}	t_{WCH}	15	–	15	–	20	–	ns	
Write Command Hold Time Referenced to $\overline{RAS}$	t_{RELWH}	t_{WCR}	55	–	60	–	75	–	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	15	–	15	–	20	–	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{WLREH}	t_{RWL}	20	–	20	–	25	–	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{WLCEH}	t_{CWL}	20	–	20	–	25	–	ns	
Data In Setup Time	t_{DVCEL}	t_{DS}	0	–	0	–	0	–	ns	15
Data In Hold Time	t_{CELDX}	t_{DH}	15	–	15	–	20	–	ns	15
Data In Hold Time Referenced to $\overline{RAS}$	t_{RELDX}	t_{DHR}	55	–	60	–	75	–	ns	
Refresh Period MCM511000A MCM51L1000A	t_{RVRV}	t_{RFSH}	– –	8 64	– –	8 64	– –	8 64	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	–	0	–	0	–	ns	16
$\overline{CAS}$ to Write Delay	t_{CELWL}	t_{CWD}	20	–	20	–	25	–	ns	16
$\overline{RAS}$ to Write Delay	t_{RELWL}	t_{RWD}	70	–	80	–	100	–	ns	16
Column Address to Write Delay Time	t_{AVWL}	t_{AWD}	35	–	40	–	50	–	ns	16
$\overline{CAS}$ Setup Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEL}	t_{CSR}	10	–	10	–	10	–	ns	
$\overline{CAS}$ Hold Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEH}	t_{CHR}	30	–	30	–	30	–	ns	
$\overline{CAS}$ Precharge to $\overline{CAS}$ Active Time	t_{REHCEL}	t_{RPC}	0	–	0	–	0	–	ns	
$\overline{CAS}$ Precharge Time for $\overline{CAS}$ Before $\overline{RAS}$ Counter Test	t_{CEHCEL}	t_{CPT}	40	–	40	–	50	–	ns	
$\overline{CAS}$ Precharge Time	t_{CEHCEL}	t_{CPN}	10	–	10	–	15	–	ns	
Test Mode Enable Setup Time Referenced to $\overline{RAS}$	t_{TEHREL}	t_{TES}	0	–	0	–	0	–	ns	
Test Mode Enable Hold Time Referenced to $\overline{RAS}$	t_{REHTEL}	t_{TEHR}	0	–	0	–	0	–	ns	
Test Mode Enable Hold Time Referenced to $\overline{CAS}$	t_{CEHTEL}	t_{TEHC}	0	–	0	–	0	–	ns	

NOTES:

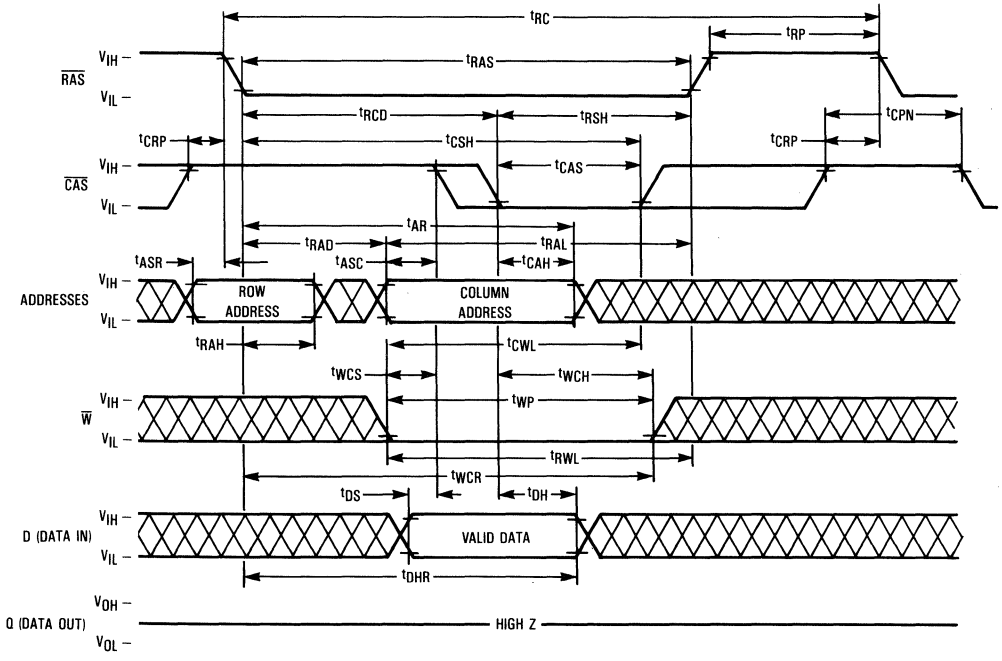
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{W}$ leading edge in delayed write or read-write cycles.
16. t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

2

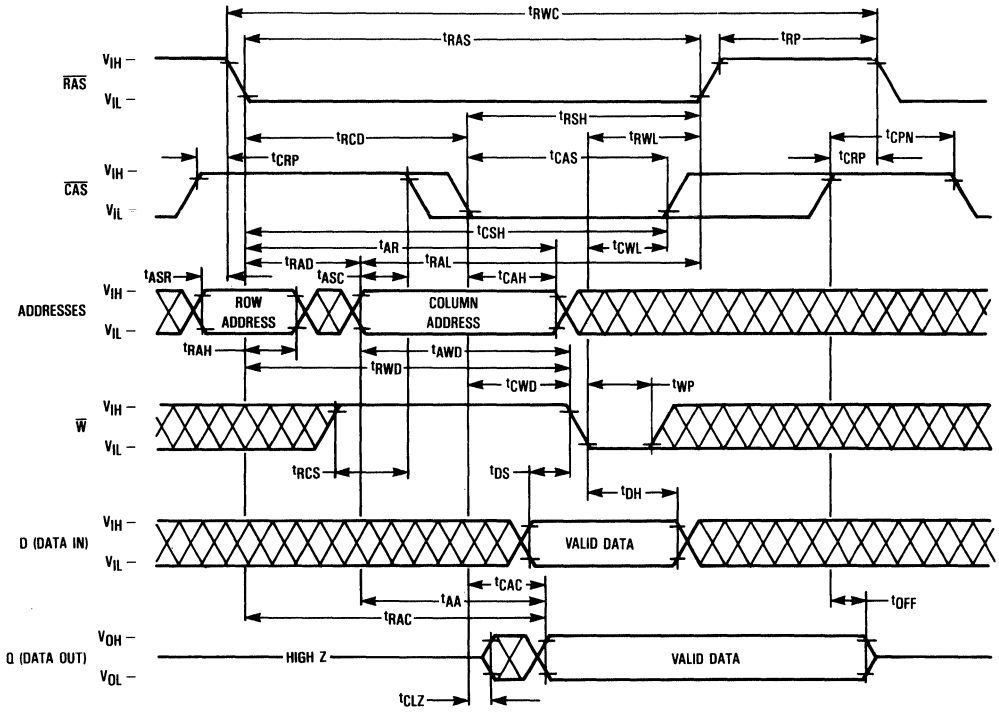
READ CYCLE



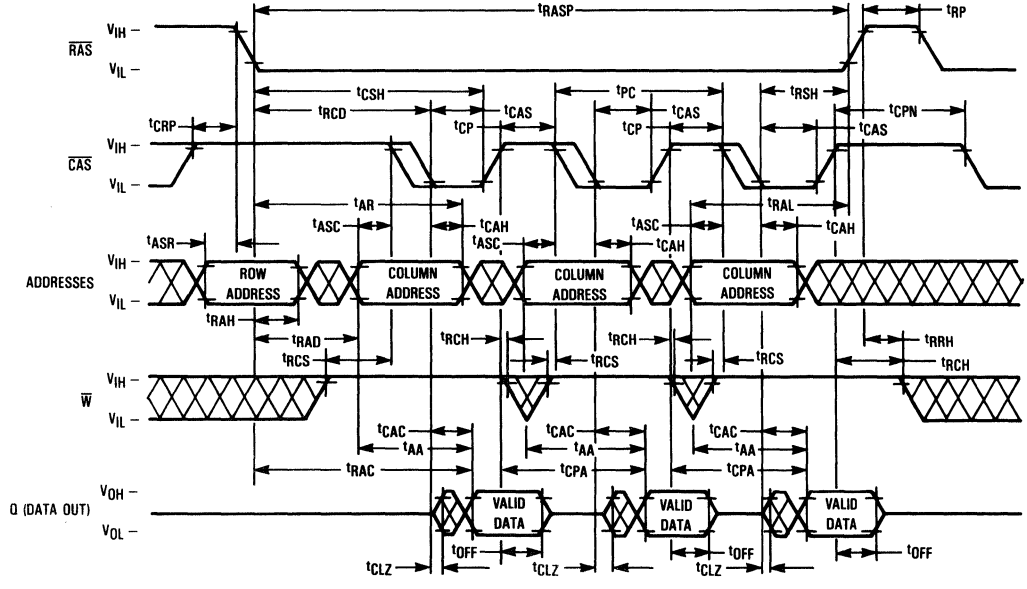
EARLY WRITE CYCLE



READ-WRITE CYCLE

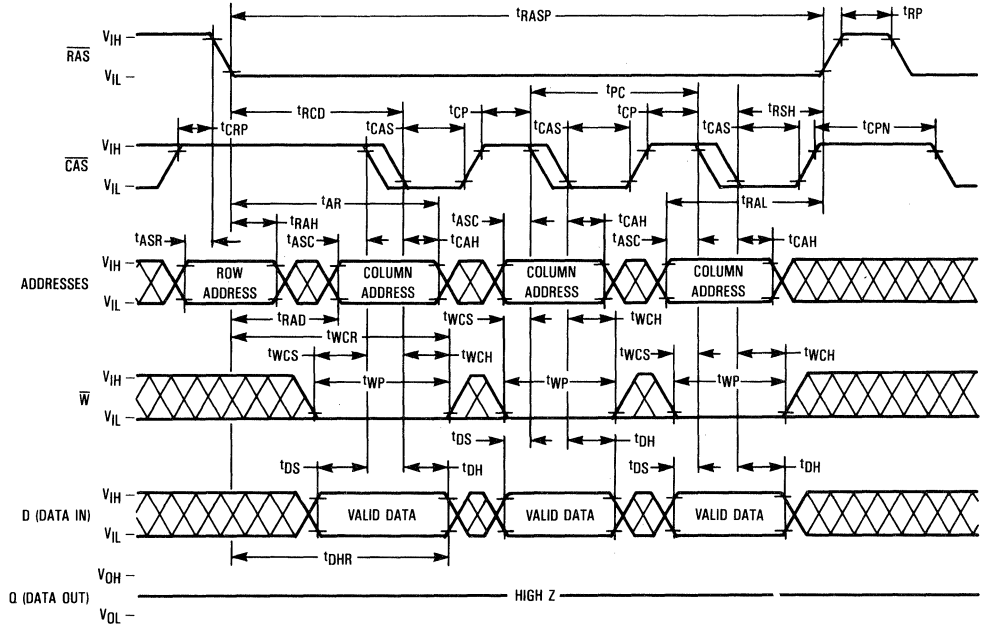


FAST PAGE MODE READ CYCLE

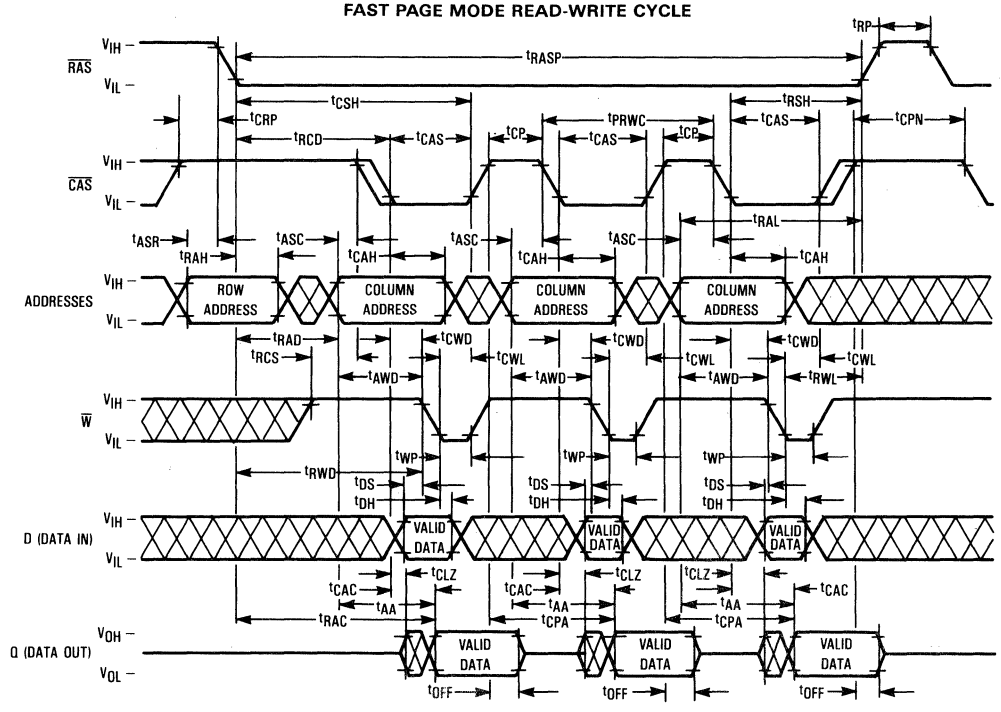


2

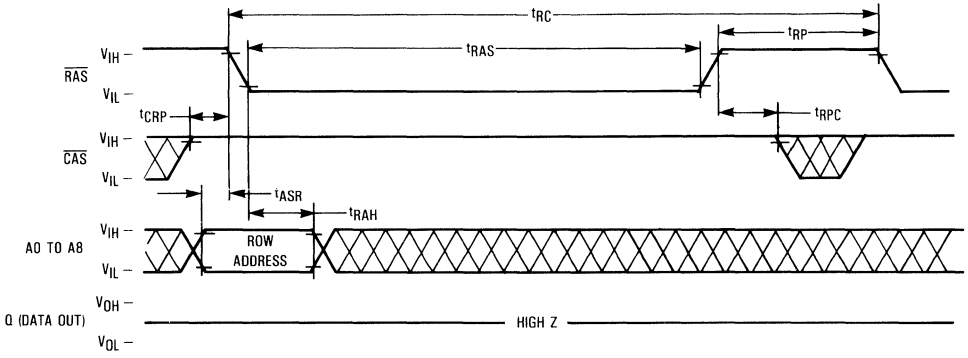
FAST PAGE MODE EARLY WRITE CYCLE



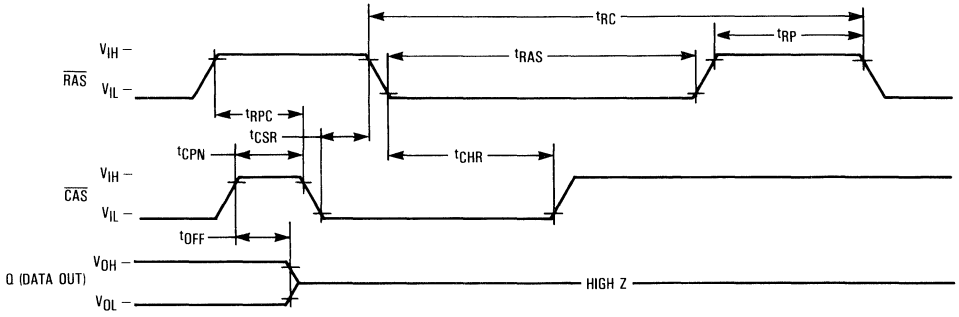
FAST PAGE MODE READ-WRITE CYCLE



$\overline{RAS}$ ONLY REFRESH CYCLE
($\overline{W}$ and A9 are Don't Care)

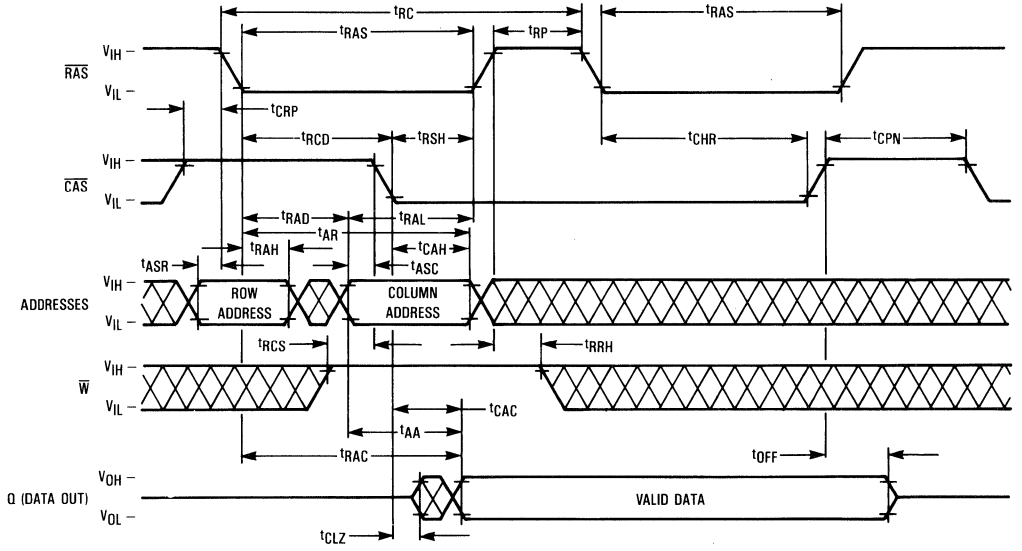


$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE
($\overline{W}$ and A0 to A9 are Don't Care)

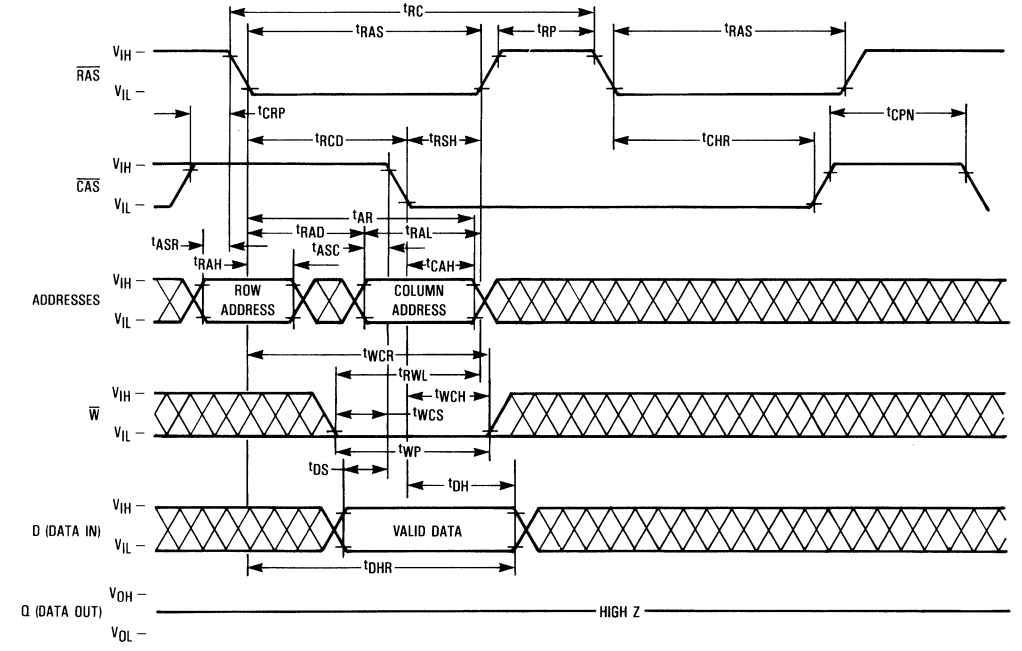


2

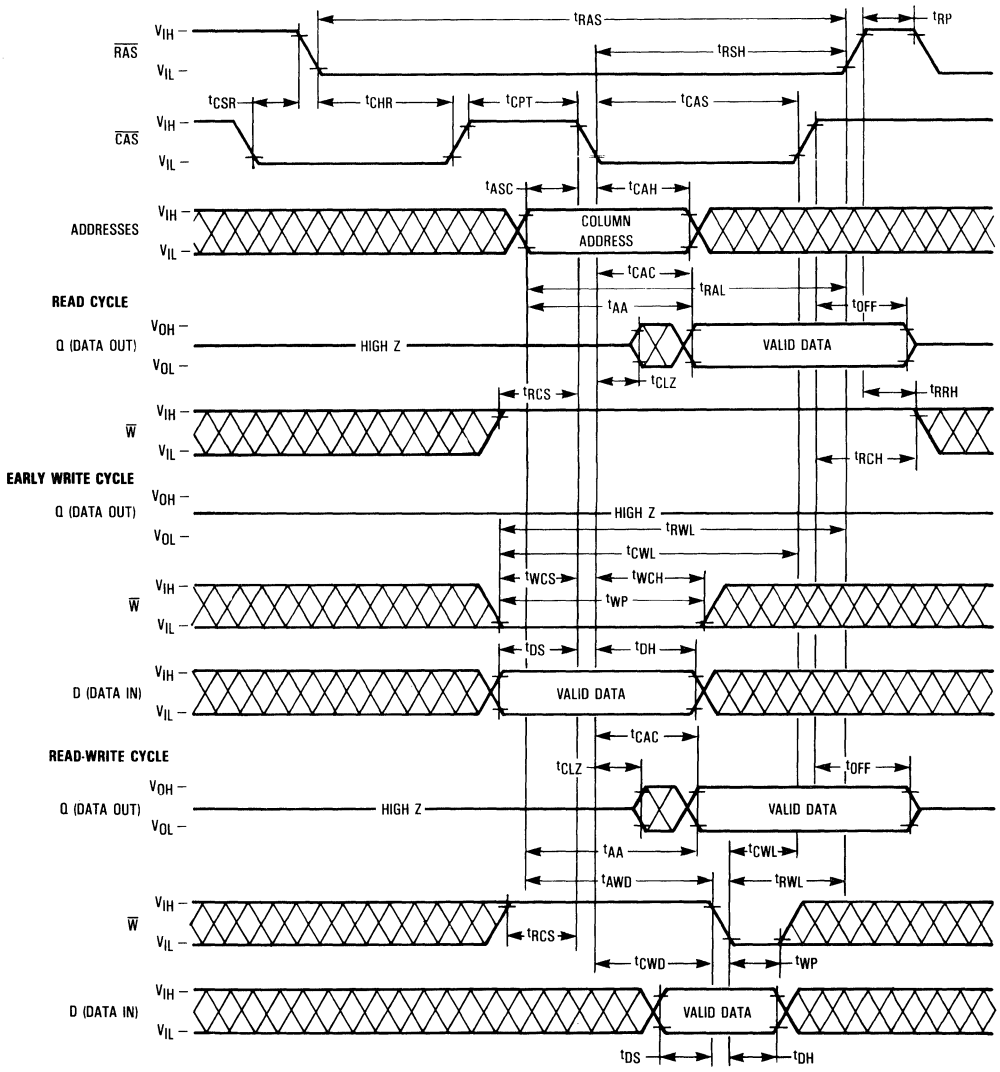
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (EARLY WRITE)



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



2

DEVICE INITIALIZATION

On power-up an initial pause of 200 microseconds is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize all dynamic nodes within the RAM. During an extended inactive state (greater than 8 milliseconds with the device powered up), a wake up sequence of eight active cycles is necessary to assure proper operation.

ADDRESSING THE RAM

The ten address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks, row address strobe ($\overline{RAS}$) and column address strobe ($\overline{CAS}$), into two separate 10-bit address fields. A total of twenty address bits, ten rows and ten columns, will decode one of the 1,048,576 bit locations in the device. $\overline{RAS}$ active transition is followed by $\overline{CAS}$ active transition (active = V_{IL}, t_{RCD} minimum) for all read or write cycles. The delay between $\overline{RAS}$ and $\overline{CAS}$ active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

The external $\overline{CAS}$ signal is ignored until an internal $\overline{RAS}$ signal is available. This "gate" feature on the external $\overline{CAS}$ clock enables the internal $\overline{CAS}$ line as soon as the row address hold time (t_{RAH}) specification is met (and defines t_{RCD} minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{CAS}$ clock.

There are two other variations in addressing the 1M RAM: **$\overline{RAS}$ only refresh cycle** and **$\overline{CAS}$ before $\overline{RAS}$ refresh cycle**. Both are discussed in separate sections that follow.

READ CYCLE

The DRAM may be read with four different cycles: "normal" random read cycle, page mode read cycle, read-write cycle, and page mode read-write cycle. The normal read cycle is outlined here, while the other cycles are discussed in separate sections.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with $\overline{RAS}$ and $\overline{CAS}$ active transitions latching the desired bit location. The write ($\overline{W}$) input level must be high (V_{IH}), t_{RCS} (minimum) before the $\overline{CAS}$ active transition, to enable read mode.

Both the $\overline{RAS}$ and $\overline{CAS}$ clocks trigger a sequence of events which are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window. However, $\overline{CAS}$ must be active before or at t_{RCD} maximum to guarantee valid data out (Q) at t_{RAC} (access time from $\overline{RAS}$ active transition). If the t_{RCD} maximum is exceeded, read access time is determined by the $\overline{CAS}$ clock active transition (t_{CAC}).

The $\overline{RAS}$ and $\overline{CAS}$ clocks must remain active for a minimum time of t_{RAS} and t_{CAS} respectively, to complete the read cycle. $\overline{W}$ must remain high throughout the cycle, and for time t_{RRH} or t_{RCH} after $\overline{RAS}$ or $\overline{CAS}$ inactive transition, respectively, to maintain the data at that bit location. Once $\overline{RAS}$ transitions to inactive, it must remain inactive for a minimum time of t_{RP} to precharge the internal device circuitry for the next active cycle. Q is valid, but not latched, as long as the $\overline{CAS}$ clock is active. When the $\overline{CAS}$ clock transitions to inactive, the output will switch to High Z.

WRITE CYCLE

The user can write to the DRAM with any of four cycles; early write, late write, page mode early write, and page mode read-write. Early and late write modes are discussed here, while page mode write operations are covered in another section.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of $\overline{W}$ to active (V_{IL}). Early and late write modes are distinguished by the active transition of $\overline{W}$, with respect to $\overline{CAS}$. Minimum active time t_{RAS} and t_{CAS}, and precharge time t_{RP} apply to write mode, as in the read mode.

An early write cycle is characterized by $\overline{W}$ active transition at minimum time t_{WCS} before $\overline{CAS}$ active transition. Data in (D) is referenced to $\overline{CAS}$ in an early write cycle. $\overline{RAS}$ and $\overline{CAS}$ clocks must stay active for t_{RWL} and t_{CWL}, respectively, after the start of the early write operation to complete the cycle.

Q remains High Z throughout an early write cycle because $\overline{W}$ active transition precedes or coincides with $\overline{CAS}$ active transition, keeping data-out buffers disabled. This feature can be utilized on systems with a common I/O bus, provided all writes are performed with early write cycles, to prevent bus contention.

A late write cycle occurs when $\overline{W}$ active transition is made after $\overline{CAS}$ active transition. $\overline{W}$ active transition could be delayed for almost 10 microseconds after $\overline{CAS}$ active transition, ($t_{RCD} + t_{CWD} + t_{RWL} + 2t_T) \leq t_{RAS}$, if other timing minimums (t_{RCD}, t_{RWL}, and t_T) are maintained. D is referenced to $\overline{W}$ active transition in a late write cycle. Output buffers are enabled by $\overline{CAS}$ active transition but Q may be indeterminate—see note 16 of AC operating conditions table. $\overline{RAS}$ and $\overline{CAS}$ must remain active for t_{RWL} and t_{CWL}, respectively, after $\overline{W}$ active transition to complete the write cycle.

READ-WRITE CYCLE

A read-write cycle performs a read and then a write at the same address, during the same cycle. This cycle is basically a late write cycle, as discussed in the **WRITE CYCLE** section, except $\overline{W}$ must remain high for t_{CWD} minimum after the $\overline{CAS}$ active transition, to guarantee valid Q before writing the bit.

PAGE MODE CYCLES

Page mode allows fast successive data operations at all 2048 column locations on a selected row of the 1M dynamic RAM. Read access time in page mode (t_{CAC}) is typically half the regular $\overline{RAS}$ clock access time, t_{RAC}. Page mode operation consists of keeping $\overline{RAS}$ active while toggling $\overline{CAS}$ between V_{IH} and V_{IL}. The row is latched by $\overline{RAS}$ active transition, while each $\overline{CAS}$ active transition allows selection of a new column location on the row.

A page mode cycle is initiated by a normal read, write, or read-write cycle, as described in prior sections. Once the timing requirements for the first cycle are met, $\overline{CAS}$ transitions to inactive for minimum of t_{CP}, while $\overline{RAS}$ remains low (V_{IL}). The second $\overline{CAS}$ active transition while $\overline{RAS}$ is low initiates the first page mode cycle (t_{PC} or t_{PRWC}). Either a read, write,

or read-write operation can be performed in a page mode cycle, subject to the same conditions as in normal operation (previously described). These operations can be intermixed in consecutive page mode cycles and performed in any order. The maximum number of consecutive page mode cycles is limited by t_{RASP}. Page mode operation is ended when $\overline{RAS}$ transitions to inactive, coincident with or following $\overline{CAS}$ inactive transition.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge degrades with time and temperature, thus each bit must be periodically **refreshed** (recharged) to maintain the correct bit state. Bits in the MCM511000A require refresh every 8 milliseconds, while refresh time for the MCM51L1000A is 64 milliseconds.

Refresh is accomplished by cycling through the 512 row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds for the MCM511000A, and 124.8 microseconds for the MCM51L1000A. Burst refresh, a refresh of all 512 rows consecutively, must be performed every 8 milliseconds on the MCM511000A and 64 milliseconds on the MCM51L1000A.

A normal read, write, or read-write operation to the RAM will refresh all the bits (2048) associated with the particular row decoded. Three other methods of refresh, **$\overline{RAS}$-only refresh**, **$\overline{CAS}$ before $\overline{RAS}$ refresh**, and **hidden refresh** are available on this device for greater system flexibility.

$\overline{RAS}$-Only Refresh

$\overline{RAS}$-only refresh consists of $\overline{RAS}$ transition to active, latching the row address to be refreshed, while $\overline{CAS}$ remains high (V_{IH}) throughout the cycle. An external counter is employed to ensure all rows are refreshed within the specified limit.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh

$\overline{CAS}$ before $\overline{RAS}$ refresh is enabled by bringing $\overline{CAS}$ active before $\overline{RAS}$. This clock order activates an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle. The output buffer remains at the same state it was in during the previous cycle (hidden refresh).

Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding $\overline{CAS}$ active at the end of a read or write cycle, while $\overline{RAS}$ cycles inactive for t_{RP} and back to active, starts the hidden refresh. This is essentially the execution of a $\overline{CAS}$ before $\overline{RAS}$ refresh from a cycle in progress (see Figure 1).

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST

The internal refresh counter of this device can be tested with a **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test**. This test is performed with a read-write operation. During the test, the internal refresh counter generates the row address, while the external address supplies the column address. The entire array is refreshed after 512 cycles, as indicated by the check data written in each row. See **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test cycle** timing diagram.

The test can be performed after a minimum of eight **$\overline{CAS}$** before **$\overline{RAS}$** initialization cycles. Test procedure:

1. Write "0"s into all memory cells with normal write mode.
2. Select a column address, read "0" out and write "1" into the cell by performing the **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test, read-write cycle**. Repeat this operation 512 times.
3. Read the "1"s which were written in step 2 in normal read mode.
4. Using the same starting column address as in step 2, read "1" out and write "0" into the cell by performing the **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test, read-write cycle**. Repeat this operation 512 times.
5. Read "0"s which were written in step 4 in normal read mode.
6. Repeat steps 1 to 5 using complement data.

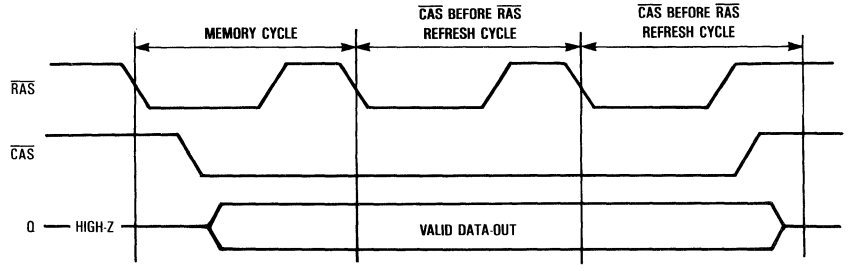


Figure 1. Hidden Refresh Cycle

2

TEST MODE

Internal organization of this device (256K × 4) allows it to be tested as if it were a 256K × 1 DRAM. Only nine of the ten addresses (A0-A8) are used in test mode; A9 is internally disabled. A test mode write cycle writes data, D (data in), to a bit in each of the four 256K × 1 blocks (B0-B3), in parallel. A test mode read cycle reads a bit in each of the four blocks. If data is the same in all four bits, Q (data out) is the same as the data in each bit. If data is not the same in all four bits, Q is high Z. See truth table and block diagram.

Test mode can be used in any timing cycle, including page mode cycles. The test mode function is enabled by holding the "TF" pin on "super voltage" for the specified period (t_{TES}, t_{TEHR}, t_{TEHC}; see TEST MODE CYCLE).

"Super voltage" = V_{CC} + 4.5 V

where

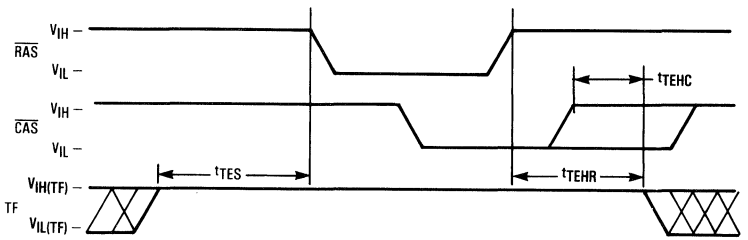
4.5 V < V_{CC} < 5.5 V and maximum voltage = 10.5 V.

A9 is ignored in test mode. In normal operation, the "TF" pin must either be connected to V_{IL}, or left open.

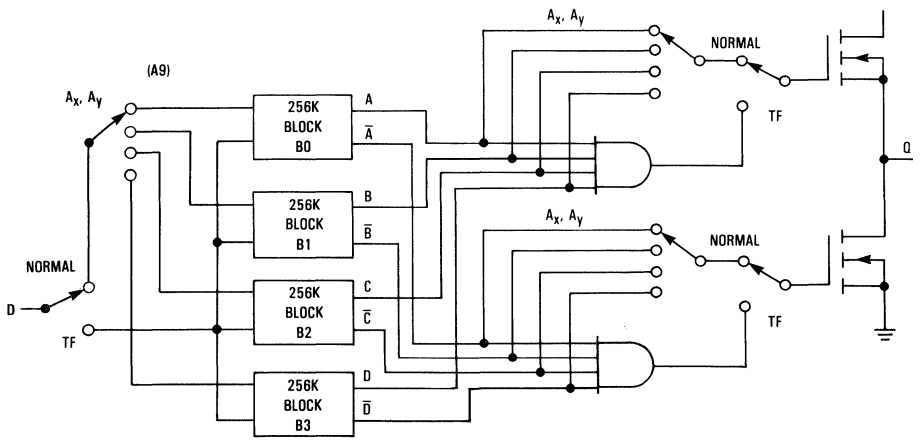
Test Mode Truth Table

D	B0	B1	B2	B3	Q
0	0	0	0	0	0
1	1	1	1	1	1
—	Any Other				High-Z

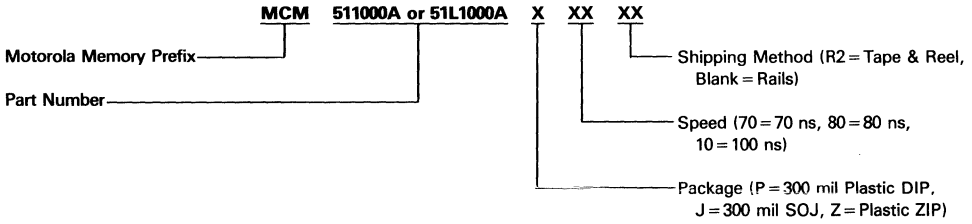
TEST MODE CYCLE



TEST FUNCTION BLOCK DIAGRAM



ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers—				
	MCM511000AP70	MCM511000AJ70	MCM511000AJ70R2	MCM511000AZ70
	MCM511000AP80	MCM511000AJ80	MCM511000AJ80R2	MCM511000AZ80
	MCM511000AP10	MCM511000AJ10	MCM511000AJ10R2	MCM511000AZ10
	MCM51L1000AP70	MCM51L1000AJ70	MCM51L1000AJ70R2	MCM51L1000AZ70
	MCM51L1000AP80	MCM51L1000AJ80	MCM51L1000AJ80R2	MCM51L1000AZ80
	MCM51L1000AP10	MCM51L1000AJ10	MCM51L1000AJ10R2	MCM51L1000AZ10

2

MCM511001A

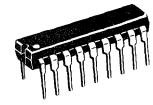
1M x 1 CMOS Dynamic RAM

Nibble Mode

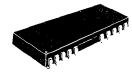
The MCM511001A is a 1.0μ CMOS high-speed, dynamic random access memory. It is organized as 1,048,576 one-bit words and fabricated with CMOS silicon-gate process technology. Advanced circuit design and fine line processing provide high performance, improved reliability, and low cost. The fast nibble mode feature allows high-speed serial access of up to 4 bits of data.

The MCM511001A requires only 10 address lines; row and column address inputs are multiplexed. The device is packaged in a standard 300-mil dual-in-line plastic package (DIP), a 300-mil SOJ plastic package, and a 100-mil zig-zag in-line plastic package (ZIP).

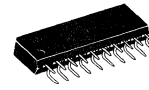
- Three-State Data Output
- Common I/O with Early Write
- Fast Nibble Mode
- Test Mode
- TTL-Compatible Inputs and Output
- $\overline{RAS}$ Only Refresh
- $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- Hidden Refresh
- 512 Cycle, 8 ms Refresh
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}): MCM511001A-70 = 70 ns (Maximum)
  MCM511001A-80 = 80 ns (Maximum)
  MCM511001A-10 = 100 ns (Maximum)
- Low Active Power Dissipation: MCM511001A-70 = 440 mW (Maximum)
  MCM511001A-80 = 385 mW (Maximum)
  MCM511001A-10 = 330 mW (Maximum)
- Low Standby Power Dissipation: 11 mW (Maximum, TTL Levels)
  5.5 mW (Maximum, CMOS Levels)



P PACKAGE
300 MIL PLASTIC
CASE 707A



J PACKAGE
300 MIL SOJ
CASE 822

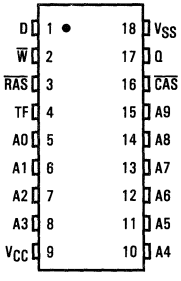


Z PACKAGE
PLASTIC
ZIG-ZAG IN-LINE
CASE 836

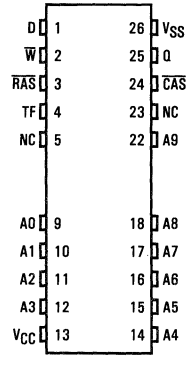
PIN NAMES	
A0-A9	Address Input
D	Data Input
Q	Data Output
$\overline{W}$	Read/Write Enable
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5 V)
V_{SS}	Ground
TF	Test Function Enable
NC	No Connection

PIN ASSIGNMENT

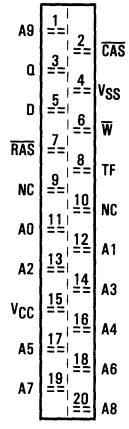
DUAL-IN-LINE



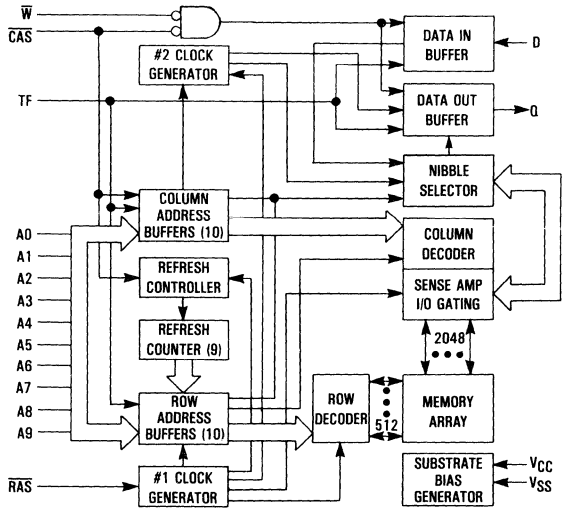
SMALL OUTLINE



ZIG-ZAG IN-LINE



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−1 to +7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−1 to +7	V
Test Function Input Voltage	$V_{in(TF)}$	−1 to +10.5	V
Data Out Current	I_{out}	50	mA
Power Dissipation	P_D	600	mW
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

2

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V	1
	V_{SS}	0	0	0		
Logic High Voltage, All Inputs	V_{IH}	2.4	–	6.5	V	1
Logic Low Voltage, All Inputs	V_{IL}	−1.0	–	0.8	V	1
Test Function Input High Voltage	$V_{IH\ (TF)}$	V_{CC}+4.5	–	10.5	V	1

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current	I_{CC1}			mA	2
MCM511001A-70, t_{RC} = 130 ns		–	80		
MCM511001A-80, t_{RC} = 150 ns		–	70		
MCM511001A-10, t_{RC} = 180 ns		–	60		
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	–	2.0	mA	
V_{CC} Power Supply Current During $\overline{RAS}$ only Refresh Cycles ($\overline{CAS}$ = V_{IH})	I_{CC3}			mA	2
MCM511001A-70, t_{RC} = 130 ns		–	80		
MCM511001A-80, t_{RC} = 150 ns		–	70		
MCM511001A-10, t_{RC} = 180 ns		–	60		
V_{CC} Power Supply Current During Nibble Mode Cycle ($\overline{RAS}$ = V_{IL})	I_{CC4}			mA	2
MCM511001A-70, t_{NC} = 35 ns		–	60		
MCM511001A-80, t_{NC} = 35 ns		–	50		
MCM511001A-10, t_{NC} = 40 ns		–	40		
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} − 0.2 V)	I_{CC5}	–	1.0	mA	
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle	I_{CC6}			mA	2
MCM511001A-70, t_{RC} = 130 ns		–	80		
MCM511001A-80, t_{RC} = 150 ns		–	70		
MCM511001A-10, t_{RC} = 180 ns		–	60		
Input Leakage Current (Except TF) (0 V ≤ V_{in} ≤ 6.5 V)	$I_{lkg(I)}$	−10	10	μA	
Input Leakage Current (TF) (0 V ≤ $V_{in(TF)}$ ≤ V_{CC} + 0.5 V)	$I_{lkg(I)}$	−10	10	μA	
Output Leakage Current ($\overline{CAS}$ = V_{IH}, 0 V ≤ V_{out} ≤ 5.5 V)	$I_{lkg(O)}$	−10	10	μA	
Test Function Input Current (V_{CC} + 4.5 V ≤ $V_{in(TF)}$ ≤ 10.5 V)	$I_{in(TF)}$	–	1	mA	
Output High Voltage (I_{OH} = −5 mA)	V_{OH}	2.4	–	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	–	0.4	V	

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Max	Unit	Notes
Input Capacitance	A0-A9, D	C_{in}	5	pF	3
	$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, TF		7	pF	3
Output Capacitance ($\overline{CAS}$ = V_{IH} to Disable Output)	Q	C_{out}	7	pF	3

NOTES:
1. All voltages referenced to V_{SS}.
2. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
3. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\Delta t/\Delta V$.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ, WRITE, AND READ-WRITE CYCLES (See Notes 1, 2, 3, 4, and 5)

Parameter	Symbol		MCM511001A-70		MCM511001A-80		MCM511001A-10		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	130	–	150	–	180	–	ns	6
Read-Write Cycle Time	t_{RELREL}	t_{RWC}	155	–	175	–	210	–	ns	6
Nibble Mode Cycle Time	t_{CEHCEH}	t_{NC}	35	–	35	–	40	–	ns	
Nibble Mode Read-Write Cycle Time	t_{CEHCEH}	t_{NRMW}	55	–	55	–	65	–	ns	
Access Time from $\overline{RAS}$	t_{RELQV}	t_{RAC}	–	70	–	80	–	100	ns	7, 8
Access Time from $\overline{CAS}$	t_{CELQV}	t_{CAC}	–	20	–	20	–	25	ns	7, 9
Access Time from Column Address	t_{AVQV}	t_{AA}	–	35	–	40	–	50	ns	7, 10
Nibble Mode Access Time	t_{CELQV}	t_{NCAC}	–	15	–	15	–	20	ns	7
$\overline{CAS}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	0	–	0	–	0	–	ns	7
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	20	0	20	0	20	ns	11
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{REHREL}	t_{RP}	50	–	60	–	70	–	ns	
$\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ Hold Time	t_{CELREH}	t_{RSH}	20	–	20	–	25	–	ns	
$\overline{CAS}$ Hold Time	t_{RELCEH}	t_{CSH}	70	–	80	–	100	–	ns	
$\overline{CAS}$ Pulse Width	t_{CELCEH}	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RELCEL}	t_{RCD}	20	50	20	60	25	75	ns	12
$\overline{RAS}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	35	15	40	20	50	ns	13
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	–	5	–	5	–	ns	
$\overline{CAS}$ Precharge Time	t_{CEHCEL}	t_{CPN}	10	–	10	–	10	–	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	–	0	–	0	–	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	–	10	–	15	–	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	–	0	–	0	–	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	–	15	–	20	–	ns	
Column Address Hold Time Referenced to $\overline{RAS}$	t_{RELAX}	t_{AR}	55	–	60	–	75	–	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{AVREH}	t_{RAL}	35	–	40	–	50	–	ns	

(continued)

NOTES:

1. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The TF pin must be at V_{IL} or open if not used.
6. The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. Measured with a current load equivalent to 2 TTL (−200 µA, +4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
8. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
9. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
10. Assumes that $t_{RAD} \geq t_{RAD}$ (max).
11. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
12. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
13. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.

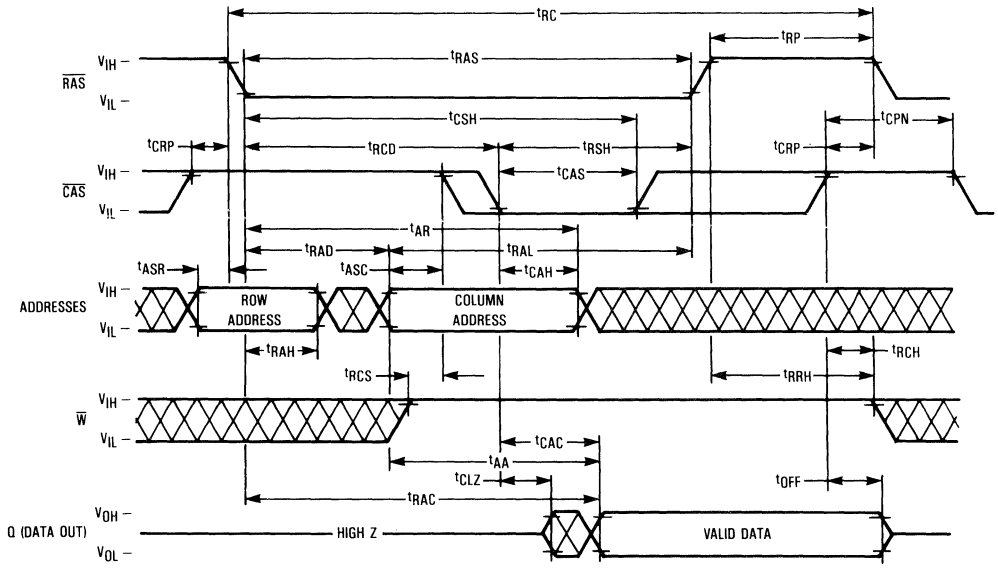
READ, WRITE, AND READ-WRITE CYCLES (Continued)

Parameter	Symbol		MCM511001A-70		MCM511001A-80		MCM511001A-10		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	–	0	–	0	–	ns	
Read Command Hold Time Referenced to $\overline{CAS}$	t_{CEHWX}	t_{RCH}	0	–	0	–	0	–	ns	14
Read Command Hold Time Referenced to $\overline{RAS}$	t_{REHWX}	t_{RRH}	0	–	0	–	0	–	ns	14
Write Command Hold Time Referenced to $\overline{CAS}$	t_{CELWH}	t_{WCH}	15	–	15	–	20	–	ns	
Write Command Hold Time Referenced to $\overline{RAS}$	t_{RELWH}	t_{WCR}	55	–	60	–	75	–	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	15	–	15	–	20	–	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{WLREH}	t_{RWL}	20	–	20	–	25	–	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{WLCEH}	t_{CWL}	20	–	20	–	25	–	ns	
Data In Setup Time	t_{DVCEL}	t_{DS}	0	–	0	–	0	–	ns	15
Data In Hold Time	t_{CELDX}	t_{DH}	15	–	15	–	20	–	ns	15
Data In Hold Time Referenced to $\overline{RAS}$	t_{RELDX}	t_{DHR}	55	–	60	–	75	–	ns	
Refresh Period	t_{RVRV}	t_{RFSH}	–	8	–	8	–	8	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	–	0	–	0	–	ns	16
$\overline{CAS}$ to Write Delay	t_{CELWL}	t_{CWD}	20	–	20	–	25	–	ns	16
$\overline{RAS}$ to Write Delay	t_{RELWL}	t_{RWD}	70	–	80	–	100	–	ns	16
Column Address to Write Delay Time	t_{AVWL}	t_{AWD}	35	–	40	–	50	–	ns	16
$\overline{CAS}$ Setup Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEL}	t_{CSR}	10	–	10	–	10	–	ns	
$\overline{CAS}$ Hold Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEH}	t_{CHR}	30	–	30	–	30	–	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	t_{REHCEL}	t_{RPC}	0	–	0	–	0	–	ns	
$\overline{CAS}$ Precharge Time for $\overline{CAS}$ Before $\overline{RAS}$ Counter Test	t_{CEHCEL}	t_{CPT}	40	–	40	–	50	–	ns	
Nibble Mode Pulse Width	t_{CELCEH}	t_{NCAS}	15	–	15	–	20	–	ns	
Nibble Mode $\overline{CAS}$ Precharge Time	t_{CEHCEL}	t_{NCP}	10	–	10	–	10	–	ns	
Nibble Mode $\overline{RAS}$ Hold Time	t_{CELREH}	t_{NRSH}	15	–	15	–	20	–	ns	
Nibble Mode $\overline{CAS}$ to Write Delay Time	t_{CELWL}	t_{NCWD}	15	–	15	–	20	–	ns	
Nibble Mode Write Command to $\overline{RAS}$ Lead Time	t_{WLREH}	t_{NRWL}	15	–	15	–	20	–	ns	
Nibble Mode Write Command to $\overline{CAS}$ Lead Time	t_{WLCEH}	t_{NCWL}	15	–	15	–	20	–	ns	
Test Mode Enable Setup Time Referenced to $\overline{RAS}$	t_{TEHREL}	t_{TES}	0	–	0	–	0	–	ns	
Test Mode Enable Hold Time Referenced to $\overline{RAS}$	t_{REHTEL}	t_{TEHR}	0	–	0	–	0	–	ns	
Test Mode Enable Hold Time Referenced to $\overline{CAS}$	t_{CEHTEL}	t_{TEHC}	0	–	0	–	0	–	ns	

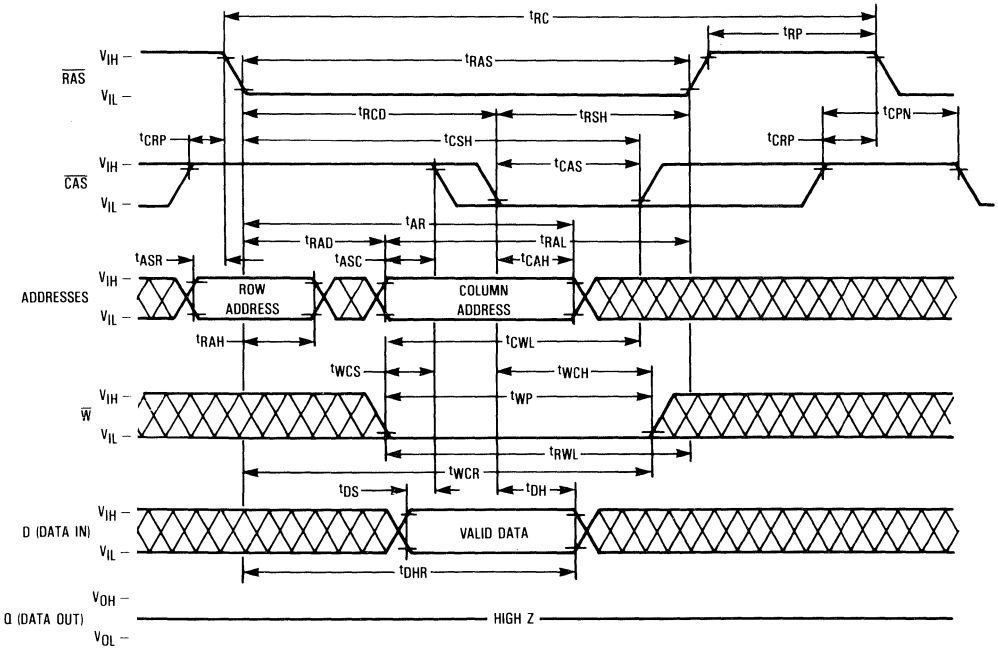
NOTES:

14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{W}$ leading edge in delayed write or read-write cycles.
16. t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

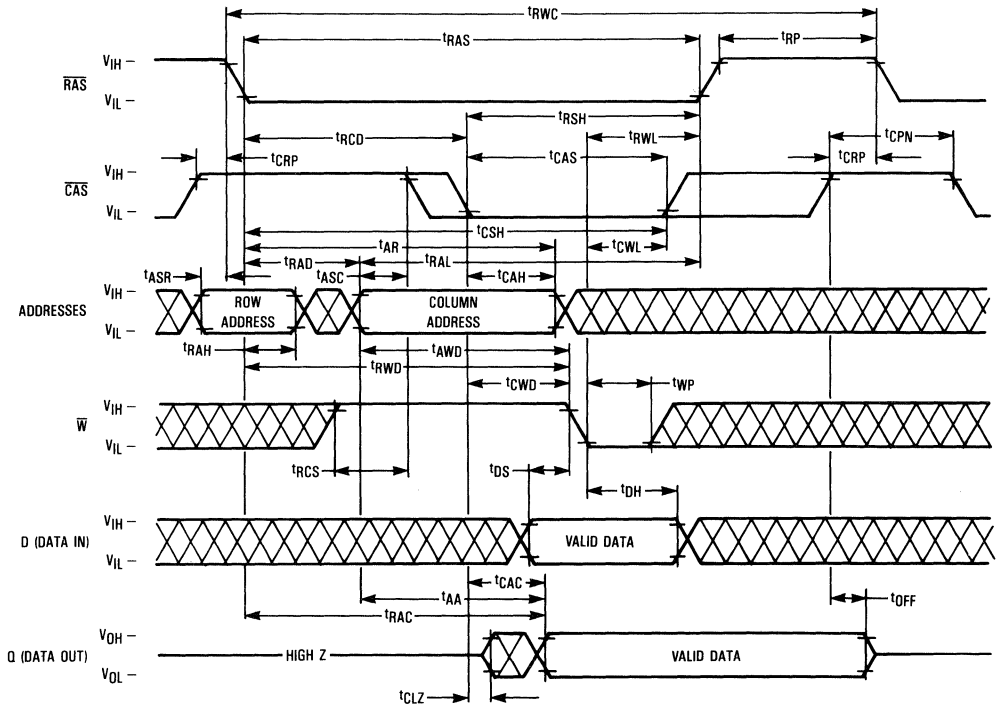
READ CYCLE



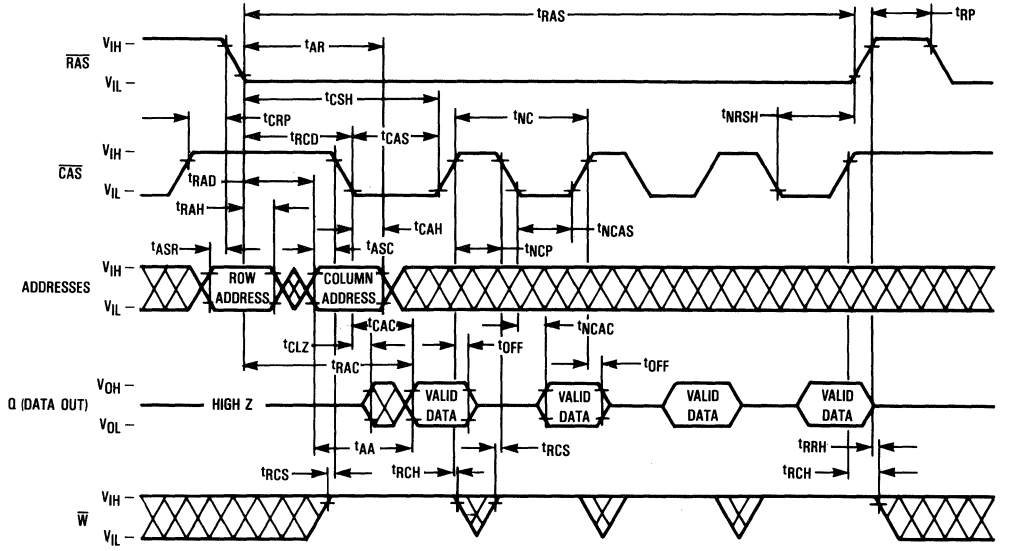
EARLY WRITE CYCLE



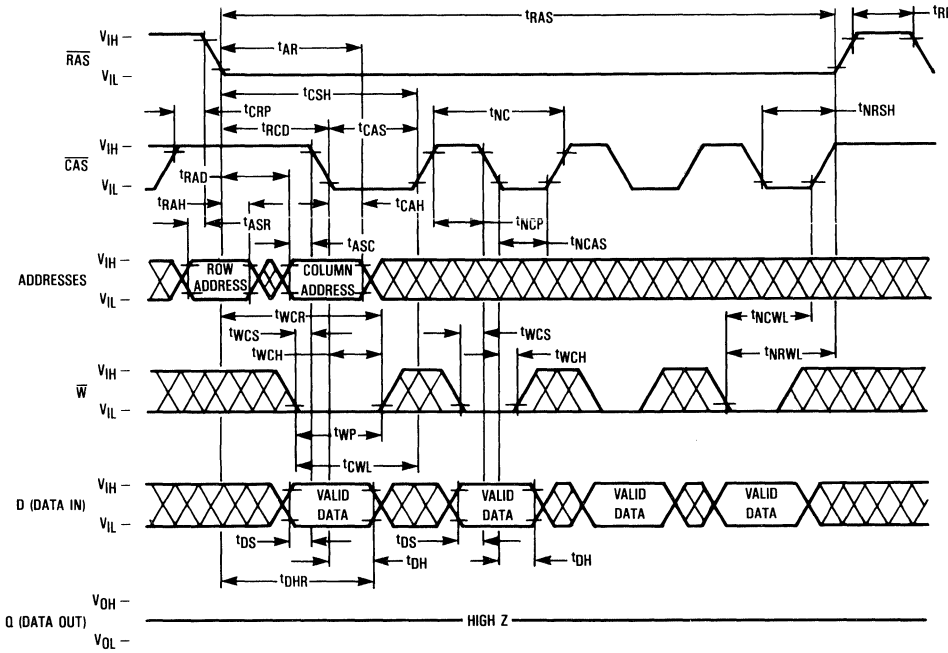
READ-WRITE CYCLE



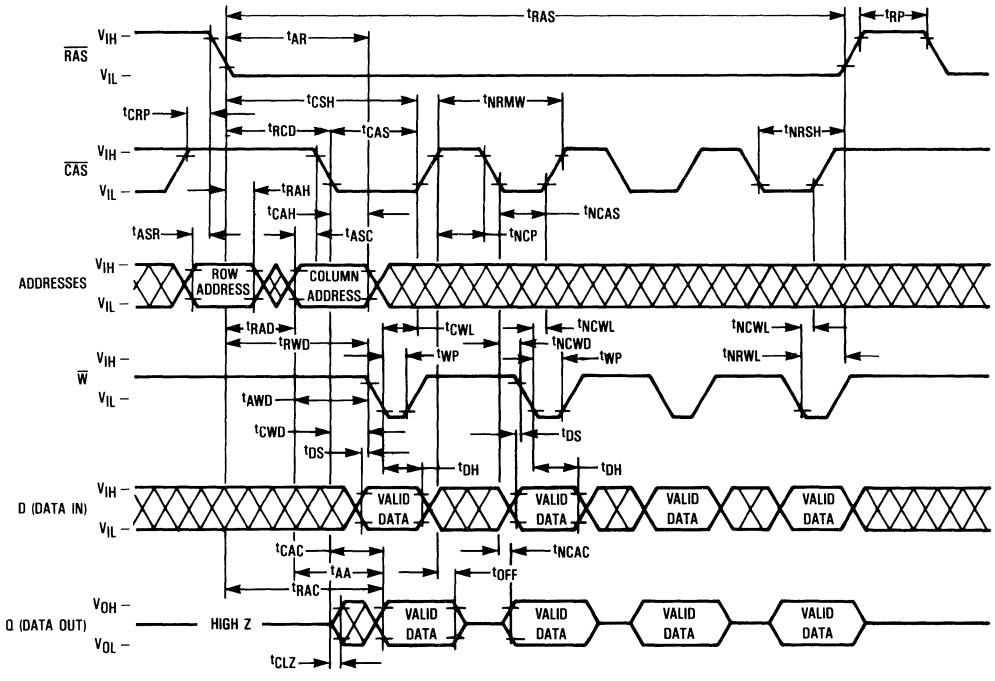
NIBBLE MODE READ CYCLE



NIBBLE MODE EARLY WRITE CYCLE



NIBBLE MODE READ-WRITE CYCLE



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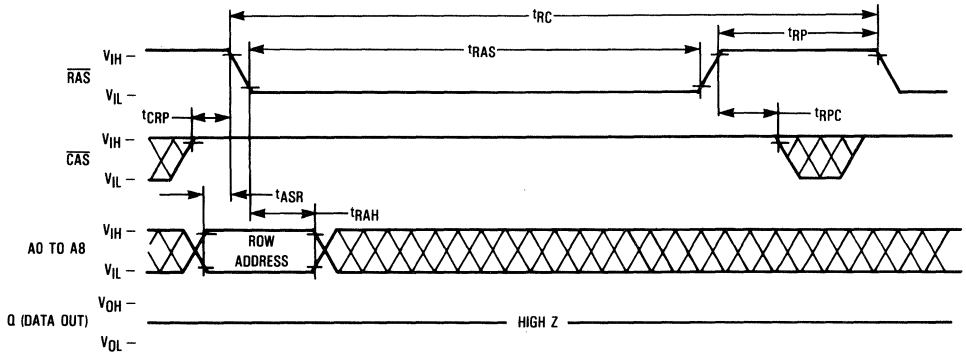
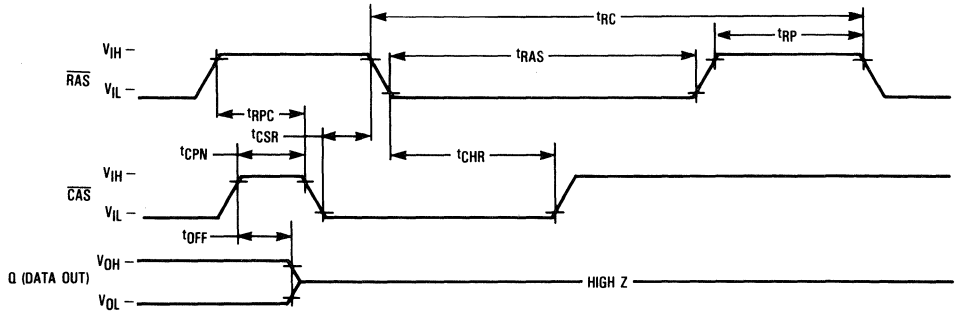
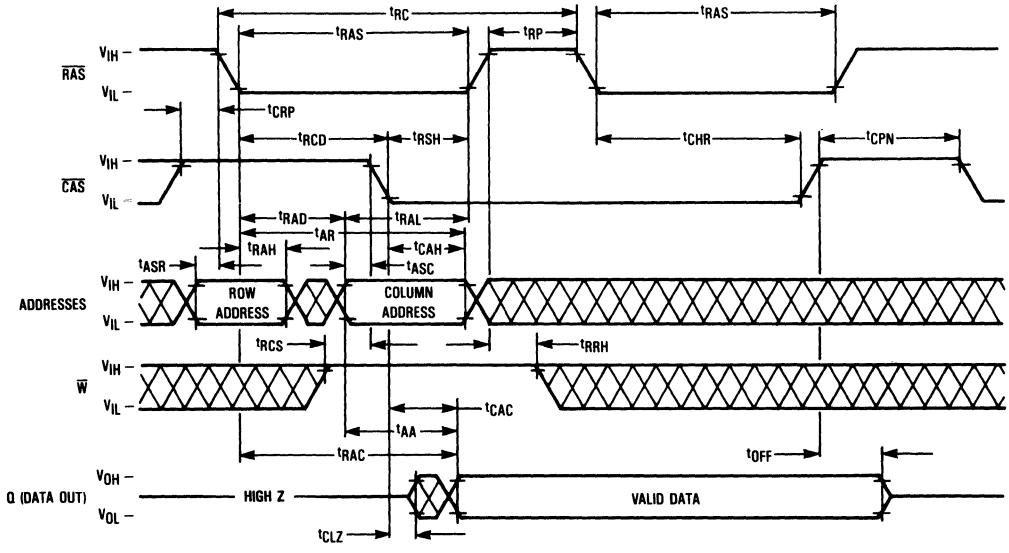
$\overline{RAS}$ ONLY REFRESH CYCLE
($\overline{W}$ and A9 are Don't Care)



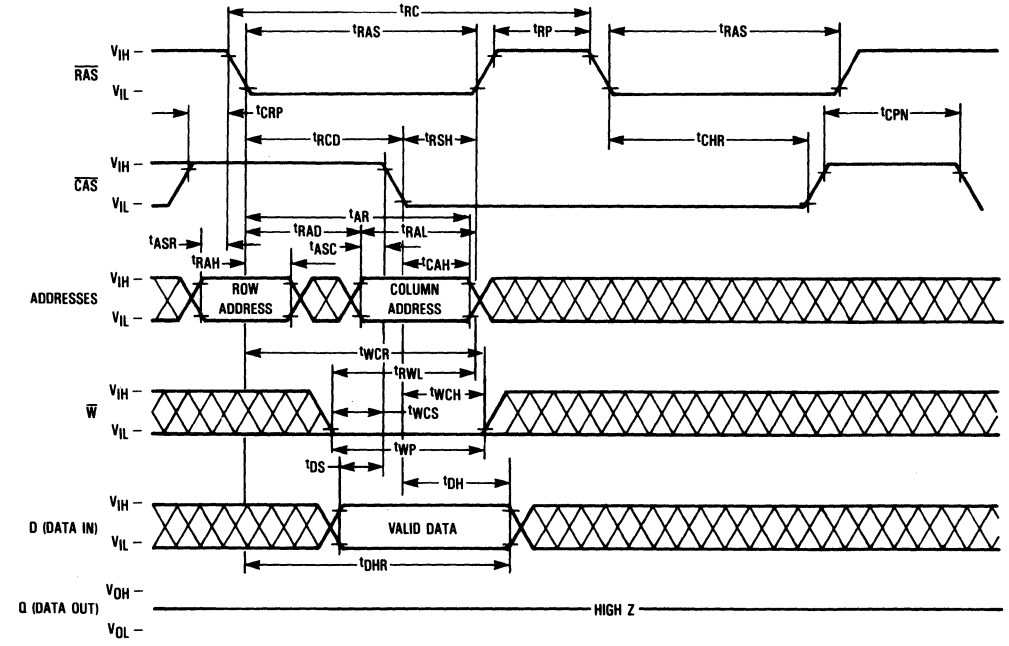
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE
($\overline{W}$ and A0 to A9 are Don't Care)



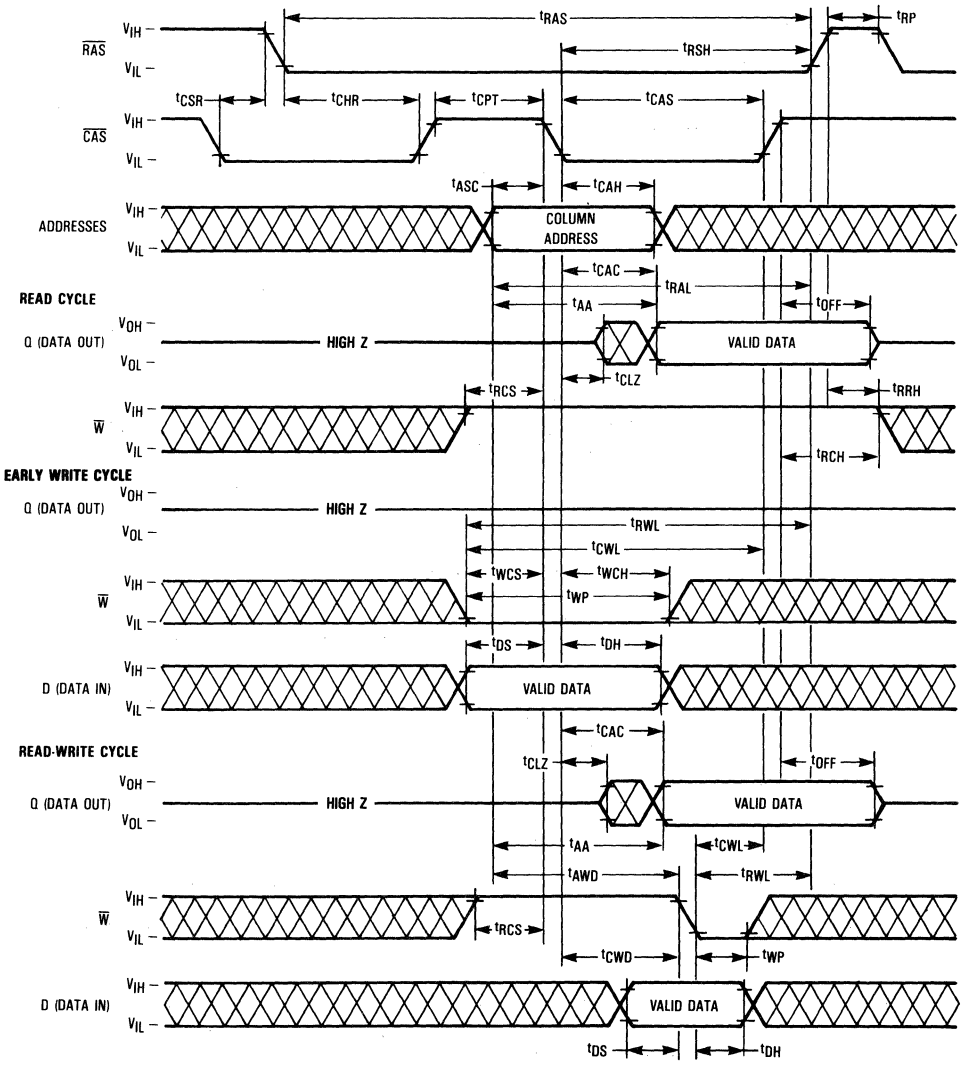
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (EARLY WRITE)



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



DEVICE INITIALIZATION

On power-up an initial pause of 200 microseconds is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize all dynamic nodes within the RAM. During an extended inactive state (greater than 8 milliseconds with the device powered up), a wake up sequence of eight active cycles is necessary to assure proper operation.

ADDRESSING THE RAM

The ten address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks, row address strobe ($\overline{RAS}$) and column address strobe ($\overline{CAS}$), into two separate 10-bit address fields. A total of twenty address bits, ten rows and ten columns, will decode one of the 1,048,576 bit locations in the device. $\overline{RAS}$ active transition is followed by $\overline{CAS}$ active transition (active = V_{IL}, t_{RCD} minimum) for all read or write cycles. The delay between $\overline{RAS}$ and $\overline{CAS}$ active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

The external $\overline{CAS}$ signal is ignored until an internal $\overline{RAS}$ signal is available. This "gate" feature on the external $\overline{CAS}$ clock enables the internal $\overline{CAS}$ line as soon as the row address hold time (t_{RAH}) specification is met (and defines t_{RCD} minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{CAS}$ clock.

There are two other variations in addressing the 1M RAM: **$\overline{RAS}$ only refresh cycle** and **$\overline{CAS}$ before $\overline{RAS}$ refresh cycle.** Both are discussed in separate sections that follow.

READ CYCLE

The DRAM may be read with four different cycles: "normal" random read cycle, nibble mode read cycle, read-write cycle, and nibble mode read-write cycle. The normal read cycle is outlined here, while the other cycles are discussed in separate sections.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with $\overline{RAS}$ and $\overline{CAS}$ active transitions latching the desired bit location. The write ($\overline{W}$) input level must be high (V_{IH}), t_{RCS} (minimum) before the $\overline{CAS}$ active transition, to enable read mode.

Both the $\overline{RAS}$ and $\overline{CAS}$ clocks trigger a sequence of events which are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window. However, $\overline{CAS}$ must be active before or at t_{RCD} maximum to guarantee valid data out (Q) at t_{RAC} (access time from $\overline{RAS}$ active transition). If the t_{RCD} maximum is exceeded, read access time is determined by the $\overline{CAS}$ clock active transition (t_{CAC}).

The $\overline{RAS}$ and $\overline{CAS}$ clocks must remain active for a minimum time of t_{RAS} and t_{CAS} respectively, to complete the read cycle. $\overline{W}$ must remain high throughout the cycle, and for time t_{RRH} or t_{RCH} after $\overline{RAS}$ or $\overline{CAS}$ inactive transition, respectively, to maintain the data at that bit location. Once $\overline{RAS}$ transitions to inactive, it must remain inactive for a minimum time of t_{RP} to precharge the internal device circuitry for the next active cycle. Q is valid, but not latched, as long as the $\overline{CAS}$ clock is active. When the $\overline{CAS}$ clock transitions to inactive, the output will switch to High Z (three-state).

WRITE CYCLE

The user can write to the DRAM with any of four cycles: early write, late write, nibble mode early write, and nibble mode read-write. Early and late write modes are discussed here, while nibble mode write operations are covered in another section.

A write cycle begins as described in **ADDRESSING THE RAM.** Write mode is enabled by the transition of $\overline{W}$ to active (V_{IL}). Early and late write modes are distinguished by the active transition of $\overline{W}$, with respect to $\overline{CAS}$. Minimum active times t_{RAS} and t_{CAS}, and precharge time t_{RP} apply to write mode, as in the read mode.

An early write cycle is characterized by $\overline{W}$ active transition at minimum time t_{WCS} before $\overline{CAS}$ active transition. Data in (D) is referenced to $\overline{CAS}$ in an early write cycle. $\overline{RAS}$ and $\overline{CAS}$ clocks must stay active for t_{RWL} and t_{CWL}, respectively, after the start of the early write operation to complete the cycle.

Q remains in three-state condition throughout an early write cycle because $\overline{W}$ active transition precedes or coincides with $\overline{CAS}$ active transition, keeping data-out buffers disabled. This feature can be utilized on systems with a common I/O bus, provided all writes are performed with early write cycles, to prevent bus contention.

A late write cycle occurs when $\overline{W}$ active transition is made after $\overline{CAS}$ active transition. $\overline{W}$ active transition could be delayed for almost 10 microseconds after $\overline{CAS}$ active transition, $(t_{RCD} + t_{CWD} + t_{RWL} + 2t_T) \leq t_{RAS}$, if other timing minimums (t_{RCD}, t_{RWL} and t_T) are maintained. D is referenced to $\overline{W}$ active transition in a late write cycle. Output buffers are enabled by $\overline{CAS}$ active transition but Q may be indeterminate—see note 16 of AC operating conditions table. $\overline{RAS}$ and $\overline{CAS}$ must remain active for t_{RWL} and t_{CWL}, respectively, after $\overline{W}$ active transition to complete the write cycle.

READ-WRITE CYCLE

A read-write cycle performs a read and then a write at the same address, during the same cycle. This cycle is basically a late write cycle, as discussed in the **WRITE CYCLE** section, except $\overline{W}$ must remain high for t_{CWD} minimum after the $\overline{CAS}$ active transition, to guarantee valid Q before writing the bit.

NIBBLE MODE CYCLES

Nibble mode allows fast successive serial data operations at two, three, or four bits of the 1M dynamic RAM. Read access time in nibble mode (t_{NCAC}) is considerably faster than the regular $\overline{RAS}$ clock access time t_{RAC}. Nibble mode operation consists of keeping $\overline{RAS}$ active while toggling $\overline{CAS}$ between V_{IH} and V_{IL}. The address of the first nibble bit is latched by $\overline{RAS}$ and $\overline{CAS}$ active transitions. Each subsequent $\overline{CAS}$ active transition increments the row and column addresses internally to access the next bit in binary fashion. After the fourth bit is accessed, the nibble pattern repeats itself: (0,0) (0,1) (1,0) (1,1) (0,0) (0,1) (1,0) (1,1) . . . . The A10 address determines the starting point of the 4-bit nibble, with row address A10 the least significant of the (column, row) ordered

2

pair. External addresses are ignored after the first nibble bit is selected.

A nibble mode cycle is initiated by a normal read, write, or read-write cycle, as described in prior sections. Once the timing requirements for the first cycle are met, $\overline{CAS}$ transitions to inactive for minimum of t_{NCP}, while $\overline{RAS}$ remains low (V_{IL}). The second $\overline{CAS}$ active transition while $\overline{RAS}$ is low initiates the first nibble mode cycle (t_{NC} or t_{NRMW}). Either a read, write, or read-write operation can be performed in a nibble mode cycle, subject to the same conditions as in normal operation (previously described). These operations can be intermixed in consecutive nibble mode cycles and performed in any order. The maximum number of consecutive nibble mode cycles is limited by t_{RAS}. Nibble mode operation ends when $\overline{RAS}$ transitions to inactive, coincident with or following a $\overline{CAS}$ inactive transition.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge degrades with time and temperature, thus each bit must be periodically **refreshed** (recharged) to maintain the correct bit state. Bits in the MCM511001A require refresh every 8 milliseconds.

Refresh is accomplished by cycling through the 512 row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds for the MCM511001A. Burst refresh, a refresh of all 512 rows consecutively, must be performed every 8 milliseconds.

A normal read, write, or read-write operation to the RAM will refresh all the bits (2048) associated with the particular row decoded. Three other methods of refresh, **$\overline{RAS}$-only refresh**, **$\overline{CAS}$ before $\overline{RAS}$ refresh**, and **hidden refresh** are available on this device for greater system flexibility.

$\overline{RAS}$-Only Refresh

$\overline{RAS}$-only refresh consists of $\overline{RAS}$ transition to active, latching the row address to be refreshed, while $\overline{CAS}$ remains high (V_{IH}) throughout the cycle. An external counter is employed to ensure all rows are refreshed within the specified limit.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh

$\overline{CAS}$ before $\overline{RAS}$ refresh is enabled by bringing $\overline{CAS}$ active before $\overline{RAS}$. This clock order activates an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle. The output buffer remains at the same state it was in during the previous cycle (hidden refresh).

Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding $\overline{CAS}$ active at the end of a read or write cycle, while $\overline{RAS}$ cycles inactive for t_{RP} and back to active, starts the hidden refresh. This is essentially the execution of a $\overline{CAS}$ before $\overline{RAS}$ refresh from a cycle in progress (see Figure 1).

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST

The internal refresh counter of this device can be tested with a **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test**. This test is performed with a read-write operation. During the test, the internal refresh counter generates the row address, while the external address supplies the column address. The entire array is refreshed after 512 cycles, as indicated by the check data written in each row. See **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test cycle** timing diagram.

The test can be performed after a minimum of eight $\overline{CAS}$ before $\overline{RAS}$ initialization cycles. Test procedure:

1. Write "0"s into all memory cells with normal write mode.
2. Select a column address, read "0" out and write "1" into the cell by performing the **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test, read-write cycle.** Repeat this operation 512 times.
3. Read the "1"s which were written in step 2 in normal read mode.
4. Using the same starting column address as in step 2, read "1" out and write "0" into the cell by performing the **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test, read-write cycle.** Repeat this operation 512 times.
5. Read "0"s which were written in step 4 in normal read mode.
6. Repeat steps 1 to 5 using complement data.

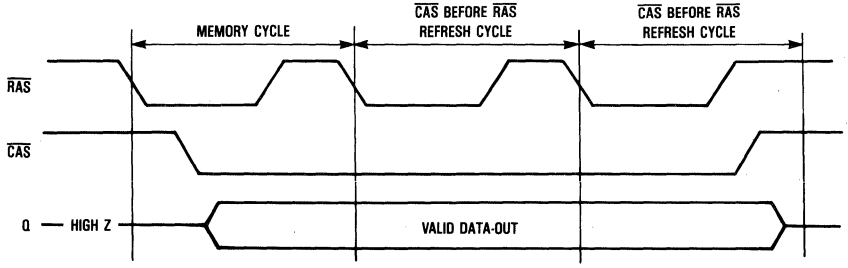


Figure 1. Hidden Refresh Cycle

TEST MODE

Internal organization of this device (256K × 4) allows it to be tested as if it were a 256K × 1 DRAM. Only nine of the ten addresses (A0-A8) are used in test mode; A9 is internally disabled. A test mode write cycle writes data, D (data in), to a bit in each of the four 256K × 1 blocks (B0-B3), in parallel. A test mode read cycle reads a bit in each of the four blocks. If data is the same in all four bits, Q (data out) is the same as the data in each bit. If data is not the same in all four bits, Q is high Z. See truth table and block diagram.

Test mode can be used in any timing cycle except nibble mode cycles. The test mode function is enabled by holding the "TF" pin on "super voltage" for the specified period (t_{TES}, t_{TEHR}, t_{TEHC}; see TEST MODE CYCLE).

"Super voltage" = V_{CC} + 4.5 V

where

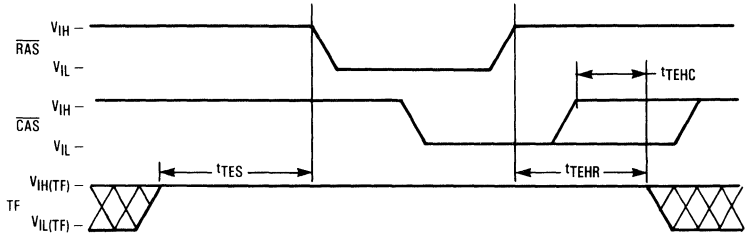
4.5 V < V_{CC} < 5.5 V and maximum voltage = 10.5 V.

A9 is ignored in test mode. In normal operation, the "TF" pin must either be connected to V_{IL}, or left open.

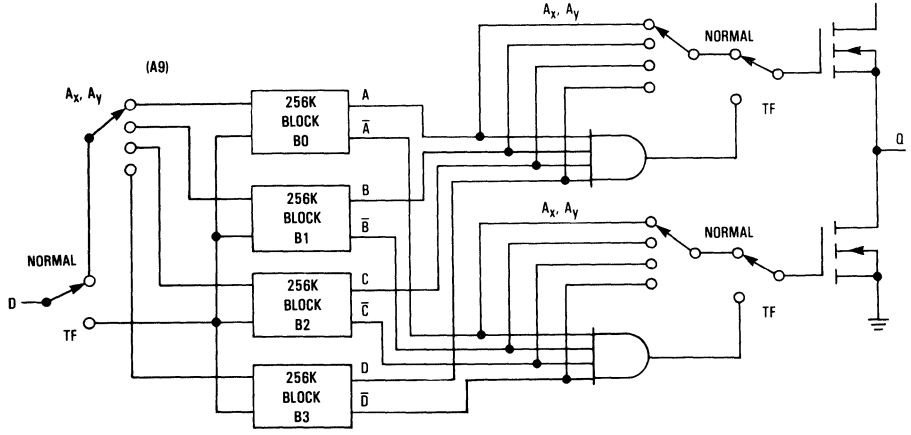
Test Mode Truth Table

D	B0	B1	B2	B3	Q
0	0	0	0	0	0
1	1	1	1	1	1
—	Any Other				High-Z

TEST MODE CYCLE



TEST FUNCTION BLOCK DIAGRAM



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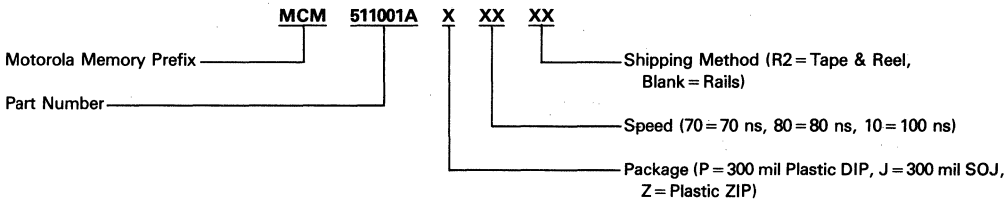
ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers—	MCM511001AP70	MCM511001AJ70	MCM511001AJ70R2	MCM511001AZ70
	MCM511001AP80	MCM511001AJ80	MCM511001AJ80R2	MCM511001AZ80
	MCM511001AP10	MCM511001AJ10	MCM511001AJ10R2	MCM511001AZ10

MCM511002A

2

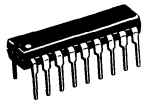
1M x 1 CMOS Dynamic RAM

Static Column

The MCM511002A is a 1.0μ CMOS high-speed, dynamic random access memory. It is organized as 1,048,576 one-bit words and fabricated with CMOS silicon-gate process technology. Advanced circuit design and fine line processing provide high performance, improved reliability, and low cost. The static column mode feature allows column data to be accessed upon the column address transition when $\overline{RAS}$ and $\overline{CS}$ are held low, similar to static RAM operation.

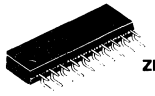
The MCM511002A requires only 10 address lines; row and column address inputs are multiplexed. The device is packaged in a standard 300-mil dual-in-line plastic package (DIP), a 300-mil SOJ plastic package, and a 100-mil zig-zag in-line plastic package (ZIP).

- Three-State Data Output
- Common I/O with Early Write
- Static Column Mode
- Test Mode
- TTL-Compatible Inputs and Output
- $\overline{RAS}$ Only Refresh
- $\overline{CS}$ Before $\overline{RAS}$ Refresh
- Hidden Refresh
- 512 Cycle, 8 ms Refresh
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}): MCM511002A-70 = 70 ns (Maximum)
  MCM511002A-80 = 80 ns (Maximum)
  MCM511002A-10 = 100 ns (Maximum)
- Low Active Power Dissipation: MCM511002A-70 = 440 mW (Maximum)
  MCM511002A-80 = 385 mW (Maximum)
  MCM511002A-10 = 330 mW (Maximum)
- Low Standby Power Dissipation: 11 mW (Maximum, TTL Levels)
  5.5 mW (Maximum, CMOS Levels)



P PACKAGE
300 MIL PLASTIC
CASE 707A

J PACKAGE
300 MIL SOJ
CASE 822

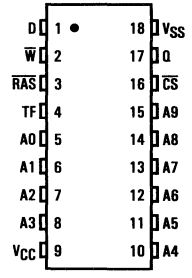


Z PACKAGE
PLASTIC
ZIG-ZAG IN-LINE
CASE 836

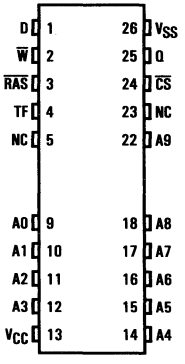
PIN NAMES	
A0-A9	Address Input
D	Data Input
Q	Data Output
$\overline{W}$	Read/Write Enable
$\overline{RAS}$	Row Address Strobe
$\overline{CS}$	Chip Select
V_{CC}	Power (+5 V)
V_{SS}	Ground
TF	Test Function Enable
NC	No Connection

PIN ASSIGNMENT

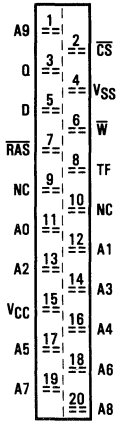
DUAL-IN-LINE



SMALL OUTLINE



ZIG-ZAG IN-LINE



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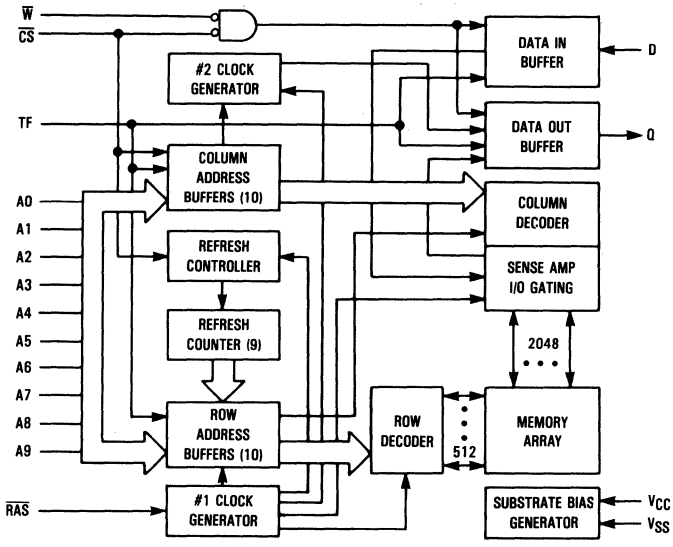
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−1 to +7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−1 to +7	V
Test Function Input Voltage	$V_{in(TF)}$	−1 to +10.5	V
Data Out Current	I_{out}	50	mA
Power Dissipation	P_D	600	mW
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V	1
	V_{SS}	0	0	0		
Logic High Voltage, All Inputs	V_{IH}	2.4	–	6.5	V	1
Logic Low Voltage, All Inputs	V_{IL}	−1.0	–	0.8	V	1
Test Function Input High Voltage	$V_{IH\ (TF)}$	V_{CC} + 4.5	–	10.5	V	1

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current	I_{CC1}			mA	2
MCM511002A-70, t_{RC} = 130 ns		–	80		
MCM511002A-80, t_{RC} = 150 ns		–	70		
MCM511002A-10, t_{RC} = 180 ns		–	60		
V_{CC} Power Supply Current (Standby) ($\overline{RAS} = \overline{CS} = V_{IH}$)	I_{CC2}	–	2.0	mA	
V_{CC} Power Supply Current During $\overline{RAS}$ only Refresh Cycles ($\overline{CS} = V_{IH}$)	I_{CC3}			mA	2
MCM511002A-70, t_{RC} = 130 ns		–	80		
MCM511002A-80, t_{RC} = 150 ns		–	70		
MCM511002A-10, t_{RC} = 180 ns		–	60		
V_{CC} Power Supply Current During Static Column Mode Cycle ($\overline{RAS} = \overline{CS} = V_{IL}$)	I_{CC4}			mA	2, 3
MCM511002A-70, t_{SC} = 40 ns		–	60		
MCM511002A-80, t_{SC} = 45 ns		–	50		
MCM511002A-10, t_{SC} = 50 ns		–	40		
V_{CC} Power Supply Current (Standby) ($\overline{RAS} = \overline{CS} = V_{CC} - 0.2$ V)	I_{CC5}	–	1.0	mA	
V_{CC} Power Supply Current During $\overline{CS}$ Before $\overline{RAS}$ Refresh Cycle	I_{CC6}			mA	2
MCM511002A-70, t_{RC} = 130 ns		–	80		
MCM511002A-80, t_{RC} = 150 ns		–	70		
MCM511002A-10, t_{RC} = 180 ns		–	60		
Input Leakage Current (Except TF) (0 V ≤ V_{in} ≤ 6.5 V)	$I_{lkg(I)}$	−10	10	μA	
Input Leakage Current (TF) (0 V ≤ $V_{in(TF)}$ ≤ V_{CC} + 0.5 V)	$I_{lkg(I)}$	−10	10	μA	
Output Leakage Current ($\overline{CS} = V_{IH}$, 0 V ≤ V_{out} ≤ 5.5 V)	$I_{lkg(O)}$	−10	10	μA	
Test Function Input Current (V_{CC} + 4.5 V ≤ $V_{in(TF)}$ ≤ 10.5 V)	$I_{in(TF)}$	–	1	mA	
Output High Voltage (I_{OH} = −5 mA)	V_{OH}	2.4	–	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	–	0.4	V	

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Max	Unit	Notes
Input Capacitance	A0-A9, D	C_{in}	5	pF	4
	$\overline{RAS}$, $\overline{CS}$, $\overline{W}$, TF		7	pF	4
Output Capacitance ($\overline{CS} = V_{IH}$ to Disable Output)	Q	C_{out}	7	pF	4

NOTES:
1. All voltages referenced to V_{SS}.
2. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
3. Measured with one address transition per static column mode cycle.
4. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\Delta t/\Delta V$.

2

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ, WRITE, AND READ-WRITE CYCLES (See Notes 1, 2, 3, 4, and 5)

Parameter	Symbol		MCM511002A-70		MCM511002A-80		MCM511002A-10		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	130	–	150	–	180	–	ns	6
Read-Write Cycle Time	t_{RELREL}	t_{RWC}	155	–	155	–	210	–	ns	6
Static Column Mode Cycle Time	t_{AVAV}	t_{SC}	40	–	45	–	50	–	ns	
Static Column Mode Read-Write Cycle Time	t_{AVAV}	t_{SRWC}	70	–	80	–	100	–	ns	
Access Time from $\overline{RAS}$	t_{RELQV}	t_{RAC}	–	70	–	80	–	100	ns	7, 8
Access Time from $\overline{CS}$	t_{CELQV}	t_{CAC}	–	20	–	20	–	25	ns	7, 9
Access Time from Column Address	t_{AVQV}	t_{AA}	–	35	–	40	–	50	ns	7, 10
Access Time from Last Write	t_{WLQV}	t_{ALW}	–	65	–	75	–	95	ns	7, 11
$\overline{CS}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	0	–	0	–	0	–	ns	7
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	20	0	20	0	20	ns	12
Data Out Hold from Address Change	t_{AXQX}	t_{AOH}	5	–	5	–	5	–	ns	
Data Out Enable from Write	t_{WHQV}	t_{OW}	–	20	–	20	–	25	ns	
Data Out Hold from Write	t_{WHQX}	t_{WOH}	0	–	0	–	0	–	ns	
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{REHREL}	t_{RP}	50	–	60	–	70	–	ns	
$\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ Pulse Width (Static Column Mode)	t_{RELREH}	t_{RASC}	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ Hold Time	t_{CELREH}	t_{RSH}	20	–	20	–	25	–	ns	
$\overline{CS}$ Hold Time	t_{RELCEH}	t_{CSH}	70	–	80	–	100	–	ns	
$\overline{CS}$ Pulse Width	t_{CELCEH}	t_{CS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{CS}$ Pulse Width (Static Column Mode)	t_{CELCEH}	t_{CSC}	20	100,000	20	100,000	25	100,000	ns	
$\overline{RAS}$ to $\overline{CS}$ Delay Time	t_{RELCEL}	t_{RCD}	20	50	20	60	25	75	ns	13
$\overline{RAS}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	35	15	40	20	50	ns	14
$\overline{CS}$ to $\overline{RAS}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	–	5	–	5	–	ns	
$\overline{CS}$ Precharge Time (Static Column Mode Cycle Only)	t_{CEHCEL}	t_{CP}	10	–	10	–	10	–	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	–	0	–	0	–	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	–	10	–	15	–	ns	

(continued)

NOTES:

1. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. TF pin must be at V_{IL} or open if not used.
6. The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. Measured with a current load equivalent to 2 TTL (−200 μA, +4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
8. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
9. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
10. Assumes that $t_{RAD} \geq t_{RAD}$ (max), and/or $t_{LWAD} \geq t_{LWAD}$ (max).
11. Assumes that $t_{LWAD} \leq t_{LWAD}$ (max).
12. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
13. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
14. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.

READ, WRITE, AND READ-WRITE CYCLES (Continued)

Parameter	Symbol		MCM511002A-70		MCM511002A-80		MCM511002A-10		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	–	0	–	0	–	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	–	15	–	20	–	ns	
Write Address Hold Time Referenced to $\overline{RAS}$	t_{RELAX}	t_{AWR}	55	–	60	–	75	–	ns	
Column Address Hold Time Referenced to $\overline{RAS}$	t_{RELAX}	t_{AR}	80	–	90	–	115	–	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{AVREH}	t_{RAL}	35	–	40	–	50	–	ns	
Column Address Hold Time Referenced to $\overline{RAS}$ High	t_{REHAX}	t_{AH}	5	–	5	–	10	–	ns	15
Write Command to $\overline{CS}$ Lead Time	t_{WLCEH}	t_{CWL}	20	–	20	–	25	–	ns	
Last Write to Column Address Delay Time	t_{WLAV}	t_{LWAD}	20	30	20	35	25	45	ns	16
Last Write to Column Address Hold Time	t_{WLAX}	t_{AHLW}	65	–	75	–	95	–	ns	
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	–	0	–	0	–	ns	
Read Command Hold Time	t_{CEHWX}	t_{RCH}	0	–	0	–	0	–	ns	17
Read Command Hold Time Referenced to $\overline{RAS}$	t_{REHWX}	t_{RRH}	0	–	0	–	0	–	ns	17
Write Command Hold Time	t_{CELWX}	t_{WCH}	15	–	15	–	20	–	ns	18
Write Command Hold Time Referenced to $\overline{RAS}$	t_{RELWH}	t_{WCR}	55	–	60	–	75	–	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	15	–	15	–	20	–	ns	
Write Command Inactive Time	t_{WHWL}	t_{WI}	10	–	10	–	10	–	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{WLREH}	t_{RWL}	20	–	20	–	25	–	ns	
Data In Setup Time	t_{DVCEL}	t_{DS}	0	–	0	–	0	–	ns	19
Data In Hold Time	t_{CELDX}	t_{DH}	15	–	15	–	20	–	ns	19
Data In Hold Time Referenced to $\overline{RAS}$	t_{RELDX}	t_{DHR}	55	–	60	–	75	–	ns	
Refresh Period	t_{RVRV}	t_{RFSH}	–	8	–	8	–	8	ms	
Write Command Setup Time (Output Data Disable)	t_{WLCEL}	t_{WCS}	0	–	0	–	0	–	ns	18
$\overline{CS}$ to Write Delay	t_{CELWL}	t_{CWD}	20	–	20	–	25	–	ns	18
$\overline{RAS}$ to Write Delay	t_{RELWL}	t_{RWD}	70	–	80	–	100	–	ns	18
Column Address to Write Delay Time	t_{AVWL}	t_{AWD}	35	–	40	–	50	–	ns	18
$\overline{CS}$ Setup Time for $\overline{CS}$ Before $\overline{RAS}$ Refresh	t_{RELCEL}	t_{CSR}	10	–	10	–	10	–	ns	
$\overline{CS}$ Hold Time for $\overline{CS}$ Before $\overline{RAS}$ Refresh	t_{RELCEH}	t_{CHR}	30	–	30	–	30	–	ns	
$\overline{CS}$ Precharge to $\overline{CS}$ Active Time	t_{REHCEL}	t_{RPC}	0	–	0	–	0	–	ns	
$\overline{CS}$ Precharge Time for $\overline{CS}$ Before $\overline{RAS}$ Counter Test	t_{CEHCEL}	t_{CPT}	40	–	40	–	50	–	ns	
$\overline{CS}$ Precharge Time	t_{CEHCEL}	t_{CPN}	10	–	10	–	15	–	ns	
Test Mode Enable Setup Time Referenced to $\overline{RAS}$	t_{TEHREL}	t_{TES}	0	–	0	–	0	–	ns	
Test Mode Enable Hold Time Referenced to $\overline{RAS}$	t_{REHTEL}	t_{TEHR}	0	–	0	–	0	–	ns	
Test Mode Enable Hold Time Referenced to $\overline{CAS}$	t_{CEHTEL}	t_{TEHC}	0	–	0	–	0	–	ns	

NOTES:

15. t_{AH} must be met for a read cycle.
16. Operation within the t_{LWAD} limit ensures that t_{ALW} can be met. t_{LWAD} (max) is specified as a reference point only; if t_{LWAD} is greater than the specified t_{LWAD} (max) limit, then access time is controlled exclusively by t_{AA}.
17. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
18. t_{WCS}, t_{WCH}, t_{RWD}, t_{CWD}, and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min) and $t_{WCH} \geq t_{WCH}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
19. These parameters are referenced to $\overline{CS}$ leading edge in early write cycles and to $\overline{W}$ leading edge in late write or read-write cycles.

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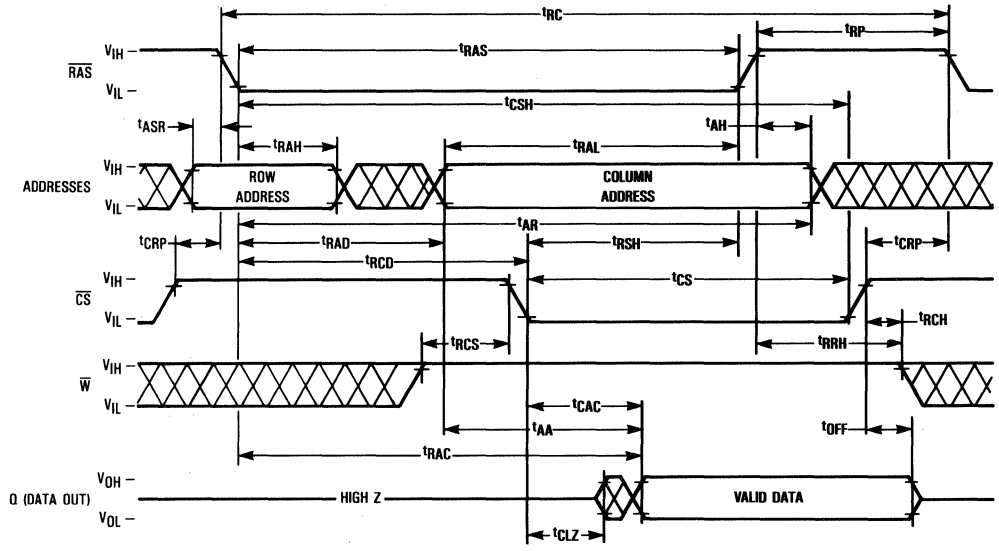
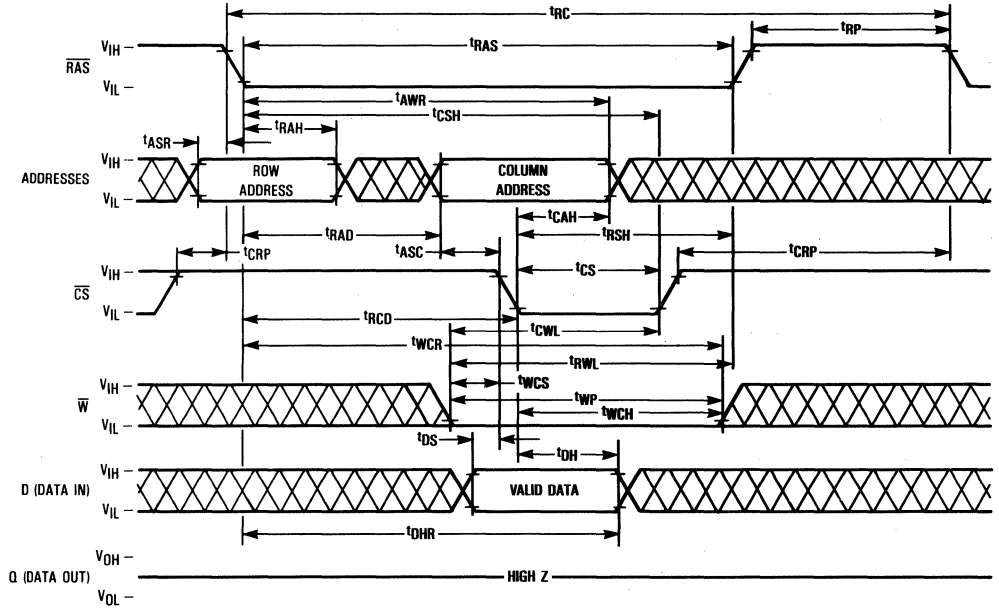
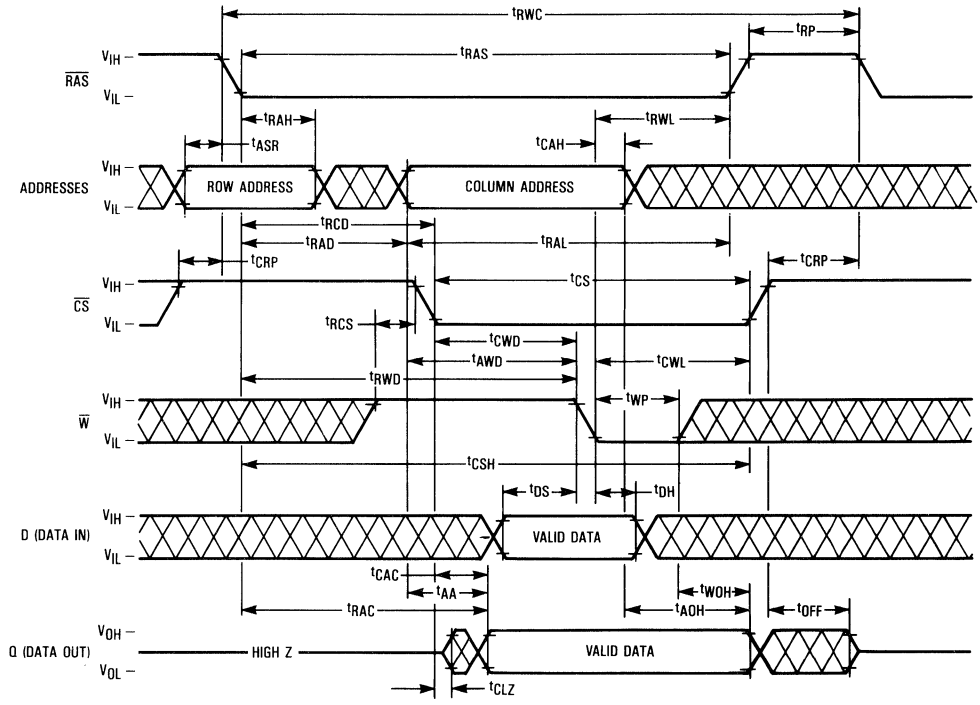
READ CYCLE



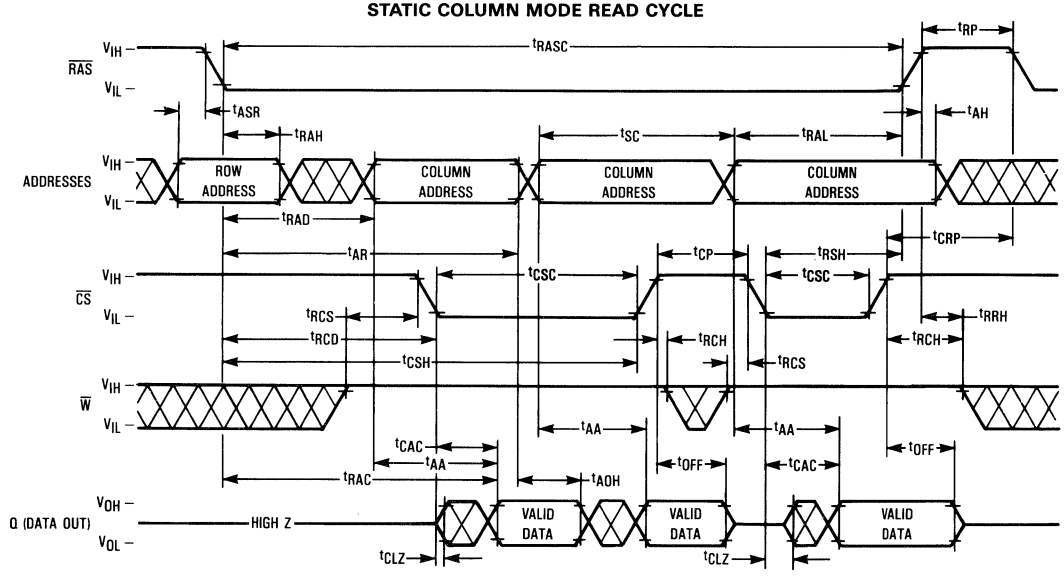
EARLY WRITE CYCLE



READ-WRITE CYCLE



STATIC COLUMN MODE READ CYCLE



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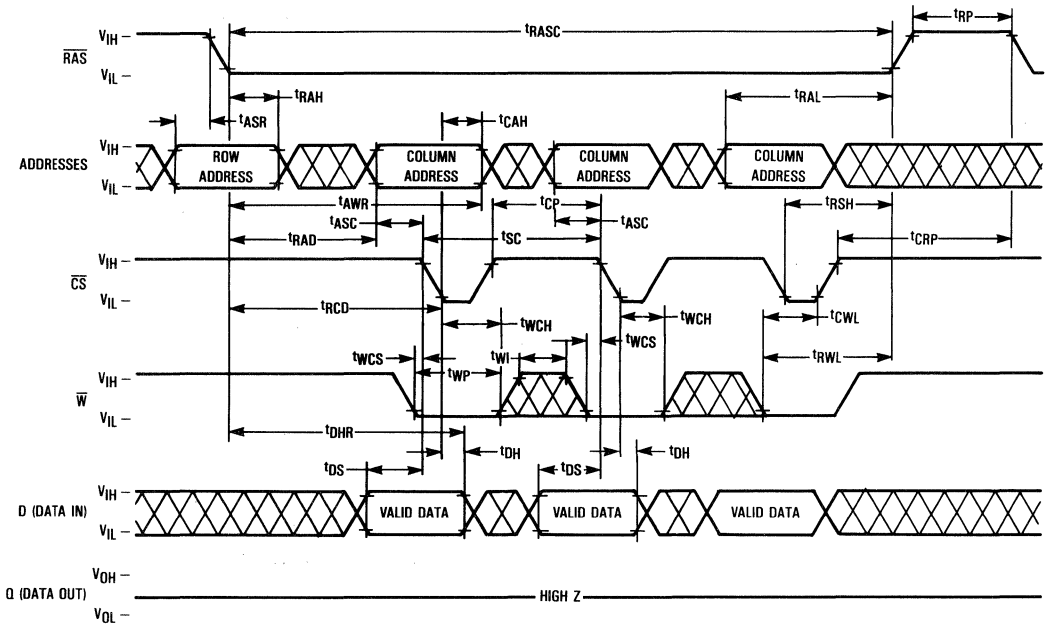
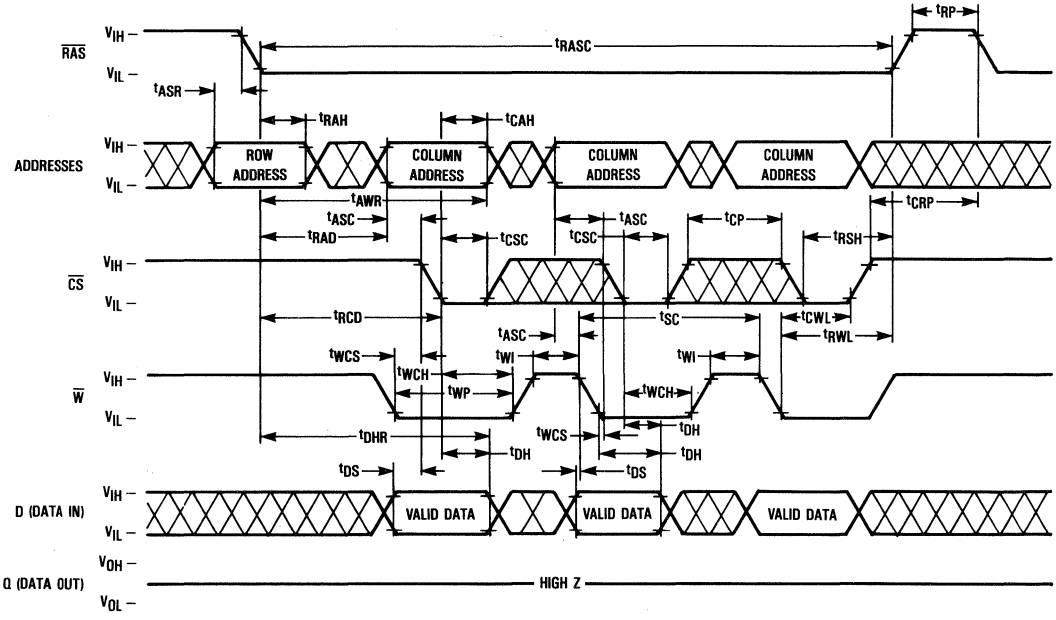
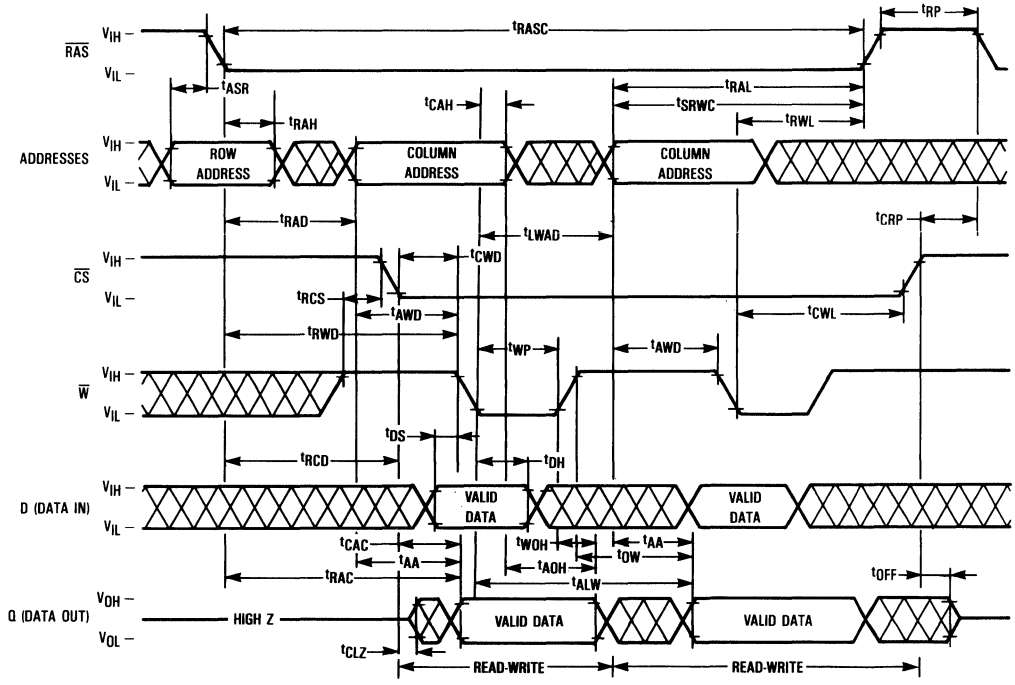
STATIC COLUMN MODE EARLY WRITE CYCLE (A)



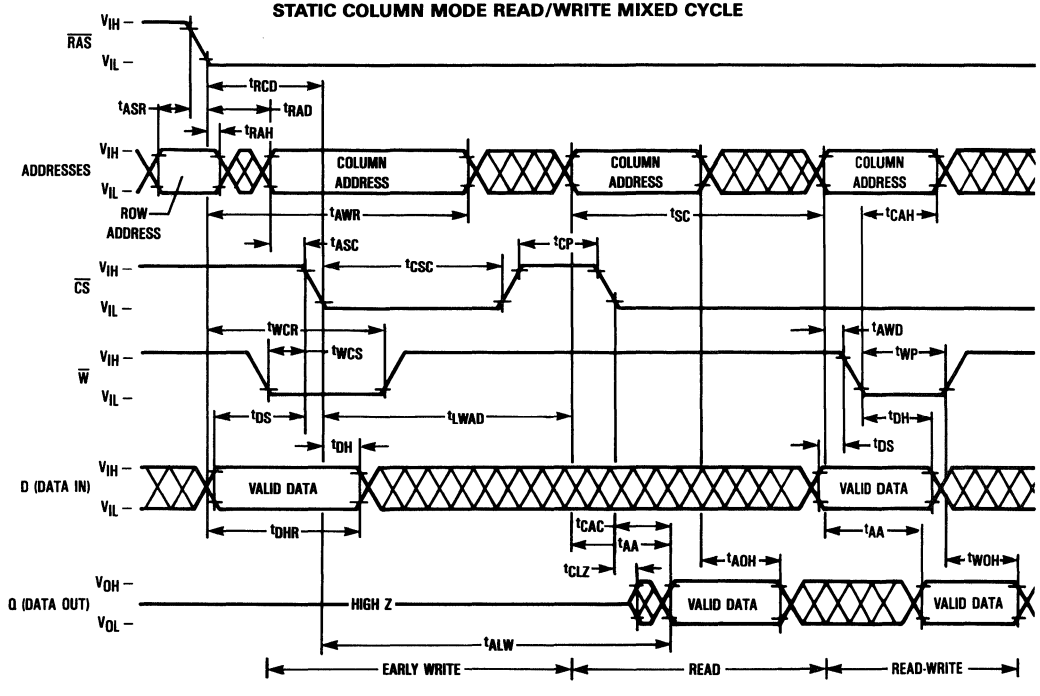
STATIC COLUMN MODE EARLY WRITE CYCLE (B)



STATIC COLUMN MODE READ-WRITE CYCLE



STATIC COLUMN MODE READ/WRITE MIXED CYCLE



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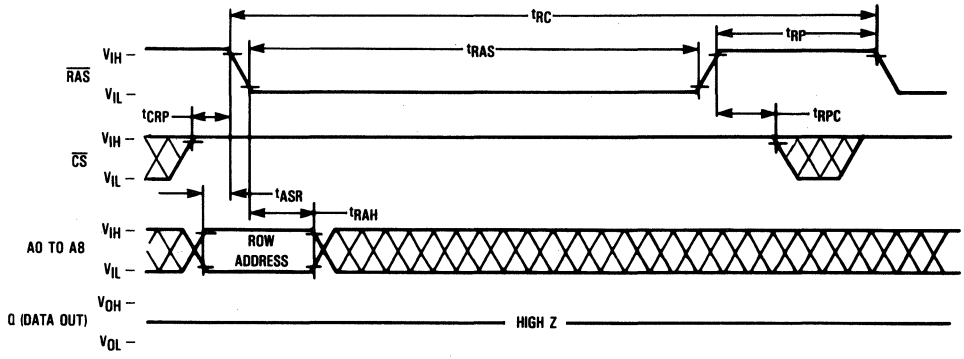
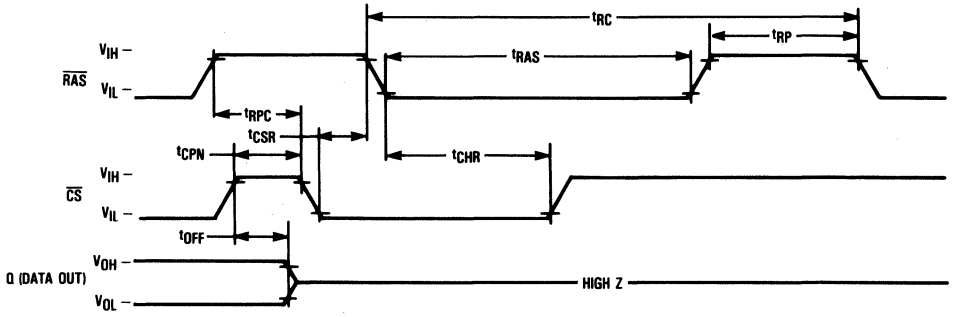
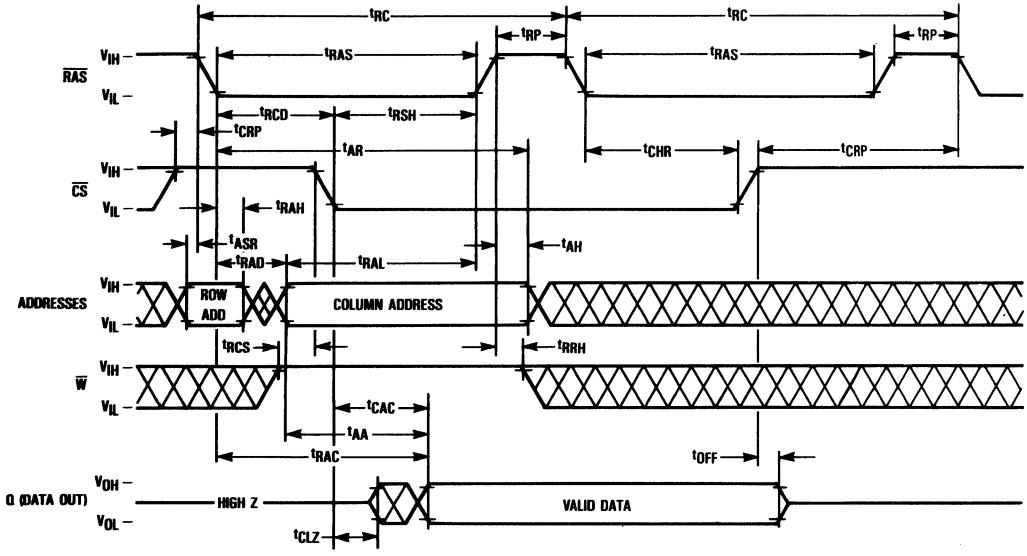
$\overline{RAS}$ ONLY REFRESH CYCLE
($\overline{W}$ and A9 are Don't Care)



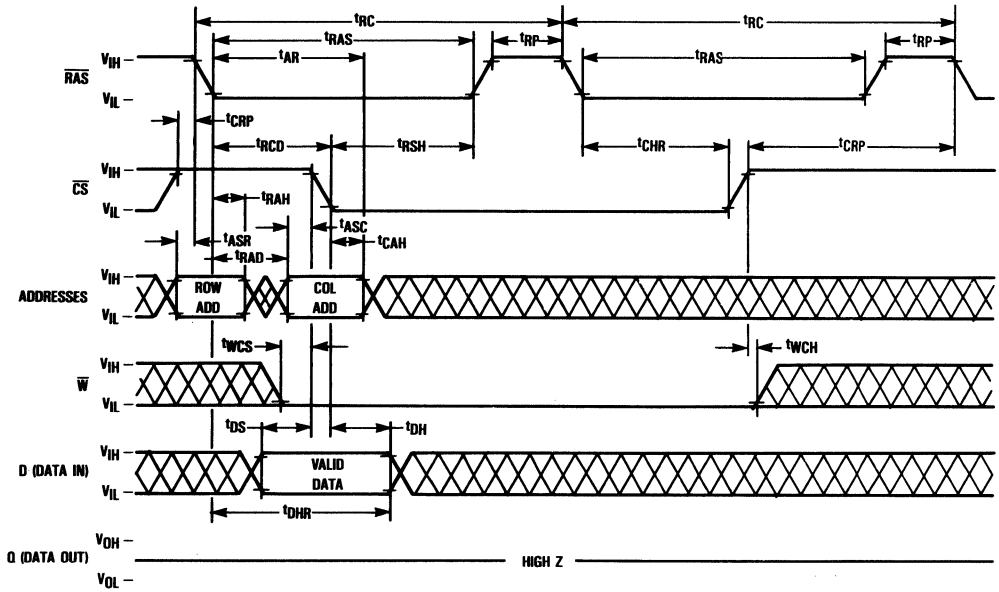
$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE
($\overline{W}$ and A0 to A9 are Don't Care)



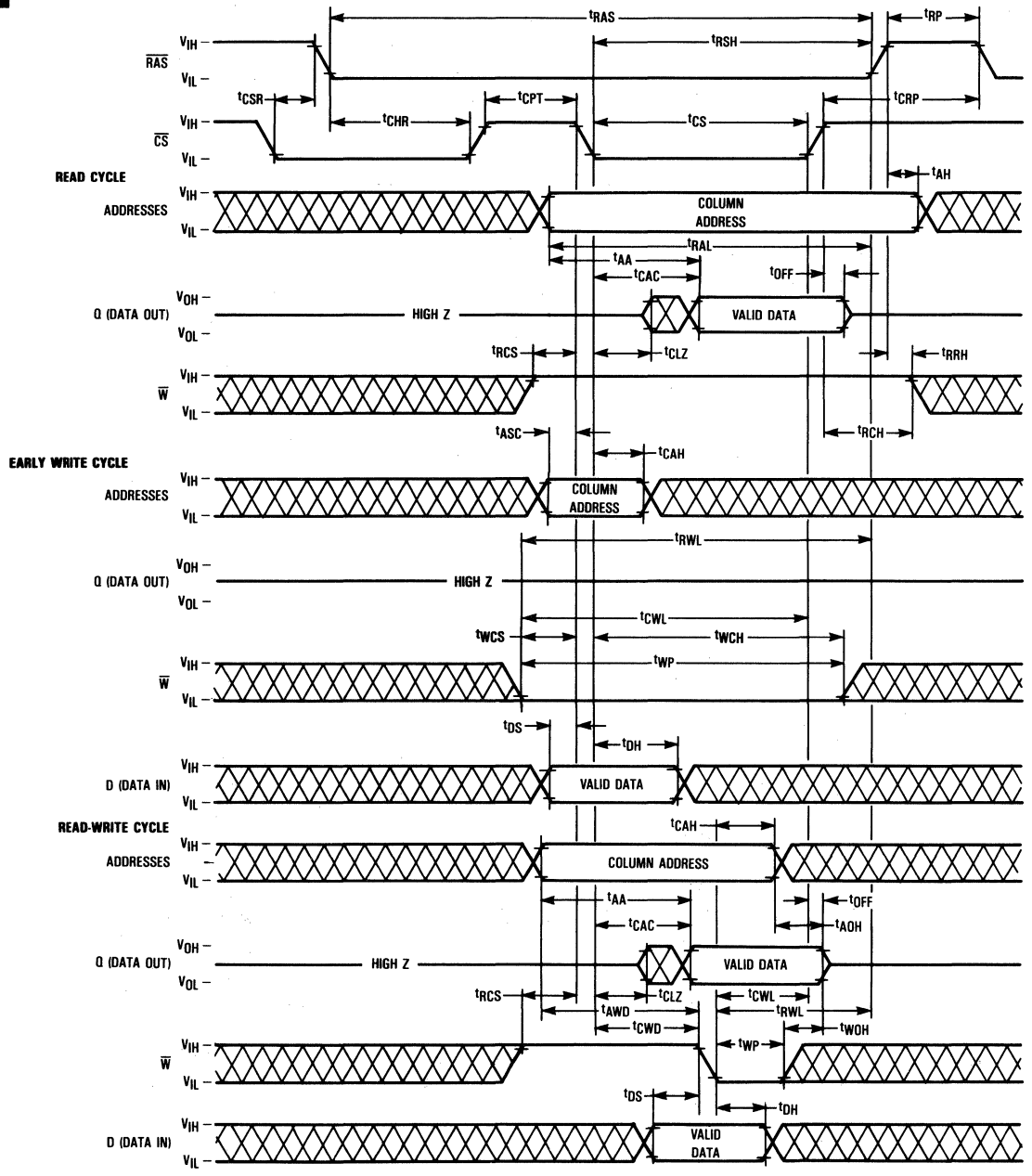
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (EARLY WRITE)



$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



DEVICE INITIALIZATION

On power-up an initial pause of 200 microseconds is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize all dynamic nodes within the RAM. During an extended inactive state (greater than 8 milliseconds with the device powered up), a wake up sequence of eight active cycles is necessary to assure proper operation.

ADDRESSING THE RAM

The ten address pins on the device are time multiplexed at the beginning of a memory cycle by the row address strobe ($\overline{RAS}$) clock, into two separate 10-bit address fields. A total of twenty address bits, ten rows and ten columns, will decode one of the 1,048,576 bit locations in the device. $\overline{RAS}$ active transition latches the row address field. Column addresses are not latched, hence the "static column" designation of this device. Chip select ($\overline{CS}$) active transition (active = V_{IL}, t_{RCD} minimum) follows $\overline{RAS}$ on all read, write, or read-write cycles, and is independent of column address. The static column feature allows greater flexibility in setting up the external external column addresses into the RAM.

There are other variations in addressing the 1M RAM: **$\overline{RAS}$ only refresh cycle** and **$\overline{CS}$ before $\overline{RAS}$ refresh cycle.** Both are discussed in separate sections that follow.

READ CYCLE

The DRAM may be read with four different cycles: random read cycle, read-write cycle, and "static column mode" read, and read-write. The random read cycle is outlined here, while the other cycles are discussed in separate sections.

The random read cycle begins as described in **ADDRESSING THE RAM**, with $\overline{RAS}$ active transition latching the desired row. The write ($\overline{W}$) input level must be high (V_{IH}), t_{RCS} (minimum) before the $\overline{CS}$ active transition, to enable read mode. A valid column address can be provided at any time (t_{RAD} minimum), independent of the $\overline{CS}$ active transition.

Both the $\overline{RAS}$ and $\overline{CS}$ clocks trigger a sequence of events which are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window. $\overline{CS}$ must be active and column address must be valid by t_{RCD} and t_{RAD} maximums, respectively, to guarantee valid data out (Q) at t_{RAC} (access time from $\overline{RAS}$ active transition). If either t_{RCD} or t_{RAD} maximum is exceeded, read access time is determined by the $\overline{CS}$ clock active transition (t_{CAC}) and/or valid column address (t_{AA}).

The $\overline{RAS}$ and $\overline{CS}$ clocks must remain active for a minimum time of t_{RAS} and t_{CS}, respectively, to complete the read cycle. The column address must remain valid for t_{AH} after $\overline{RAS}$ inactive transition to complete the read cycle. $\overline{W}$ must remain high throughout the cycle, and for time t_{RRH} or t_{RCH} after $\overline{RAS}$ or $\overline{CS}$ inactive transition, respectively, to maintain the data at that bit location. Once $\overline{RAS}$ transitions to inactive, it must remain inactive for a minimum time of t_{RP} to precharge the internal device circuitry for the next active cycle. Q is valid, but not latched, as long as the $\overline{CS}$ clock is active. When the $\overline{CS}$ clock transitions to inactive, the output will switch to High Z.

WRITE CYCLE

The DRAM may be written with any of four cycles: early write, late write and "static column mode" early write, and read-write. Early and late write modes are discussed here, while static column mode write operations are covered in another section.

A write cycle begins as described in **ADDRESSING THE RAM.** Write mode is enabled by the transition of $\overline{W}$ to active (V_{IL} level). Early and late write modes are distinguished by the active transition of $\overline{W}$ with respect to $\overline{CS}$ leading edge. Minimum active time t_{RAS} and t_{CS}, and precharge time t_{RP} apply to write mode, as in the read mode.

An early write cycle is characterized by $\overline{W}$ active transition at minimum time t_{WCS} before $\overline{CS}$ active transition. Column address set up and hold times (t_{ASC}, t_{CAH}), and data in (D) set up and hold times (t_{DS}, t_{DH}) are referenced to $\overline{CS}$ in an early write cycle. $\overline{RAS}$ and $\overline{CS}$ clocks must stay active for t_{RWL} and t_{CWL}, respectively, after the start of the early write operation to complete the cycle.

Q remains High Z throughout an early write cycle because $\overline{W}$ active transition precedes or coincides with $\overline{CS}$ active transition, keeping data-out buffers disabled. This feature can be utilized on systems with a common I/O bus, provided all writes are performed with early write cycles, to prevent bus contention.

A late write cycle occurs when $\overline{W}$ active transition is made after $\overline{CS}$ active transition. $\overline{W}$ active transition could be delayed for almost 10 microseconds after $\overline{CS}$ active transition, $(t_{RCD} + t_{CWD} + t_{RWL} + 2t_T) \leq t_{RAS}$, if other timing minimums (t_{RCD}, t_{RWL}, and t_T) are maintained. Column address and D timing parameters are referenced to $\overline{W}$ active transition in a late write cycle. Output buffers are enabled by $\overline{CS}$ active transition but Q may be indeterminate—see note 18 of AC operating conditions table. Parameters t_{RWL} and t_{CWL} also apply to late write cycles.

READ-WRITE CYCLE

A read-write cycle performs a read and then a write at the same address, during the same cycle. This cycle is basically a late write cycle, as discussed in the **WRITE CYCLE** section, except $\overline{W}$ must remain high for t_{CWD} and/or t_{AWD} minimum, to guarantee valid Q before writing the bit.

STATIC COLUMN MODE CYCLES

Static column mode refers to multiple successive data operations performed at any or all 1024 column locations on the selected row of the 1M dynamic RAM during one $\overline{RAS}$ cycle. Read access time of multiple operations (t_{AA} or t_{CAC}) is considerably faster than the regular $\overline{RAS}$ clock access time t_{RAC}. Multiple operations can be performed simply by keeping $\overline{RAS}$ active. $\overline{CS}$ may be toggled between active and inactive states at any time within the $\overline{RAS}$ cycle.

Once the timing requirements for the initial read, write, or read-write cycle are met and $\overline{RAS}$ remains low, the device is ready for the next operation. Operations can be intermixed in any order, at any column address, subject to normal operating conditions previously described. Every write operation must be clocked with either $\overline{CS}$ or $\overline{W}$, as indicated in **static column mode early write cycle** timing diagrams **A** and **B**. Column address and D timing parameters are referenced to the signal

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clocking the write operation. $\overline{CS}$ must be toggled inactive (t_{CP}) to perform a read operation after an early write operation (to turn output on), as indicated in **static column mode read/write mixed cycle** timing diagram. The maximum number of consecutive operations is limited by t_{RASC}. The cycle ends when $\overline{RAS}$ transitions to inactive.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge degrades with time and temperature, thus each bit must be periodically **refreshed** (recharged) to maintain the correct bit state. Bits in the MCM511002A require refresh every 8 milliseconds.

Refresh is accomplished by cycling through the 512 row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds for the MCM511002A. Burst refresh, a refresh of all 512 rows consecutively, must be performed every 8 milliseconds on the MCM511002A.

A normal read, write, or read-write operation to the RAM will refresh all the bits (2048) associated with the particular row decoded. Three other methods of refresh, **$\overline{RAS}$ only refresh, $\overline{CS}$ before $\overline{RAS}$ refresh,** and **hidden refresh** are available on this device for greater system flexibility.

$\overline{RAS}$-Only Refresh

$\overline{RAS}$-only refresh consists of $\overline{RAS}$ transition to active, latching the row address to be refreshed, while $\overline{CS}$ remains high (V_{IH}) throughout the cycle. An external counter is employed to ensure all rows are refreshed within the specified limit.

$\overline{CS}$ Before $\overline{RAS}$ Refresh

$\overline{CS}$ before $\overline{RAS}$ refresh is enabled by bringing $\overline{CS}$ active before $\overline{RAS}$. This clock order activates an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle. The output buffer remains at the same state it was in during the previous cycle (hidden refresh).

Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding $\overline{CS}$ active at the end of a read or write cycle, while $\overline{RAS}$ cycles inactive for t_{RP} and back to active, starts the hidden refresh. This is essentially the execution of a $\overline{CS}$ before $\overline{RAS}$ refresh from a cycle in progress (see Figure 1).

$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST

The internal refresh counter of this device can be tested with a **$\overline{CS}$ before $\overline{RAS}$ refresh counter test.** This test is performed with a read-write operation. During the test, the internal refresh counter generates the row address, while the external address supplies the column address. The entire array is refreshed after 512 test cycles, as indicated by the check data written in each row. See **$\overline{CS}$ before $\overline{RAS}$ refresh counter test cycle** timing diagram.

The test can be performed after a minimum of eight $\overline{CS}$ before $\overline{RAS}$ initialization cycles. Test procedure:

1. Write "0"s into all memory cells with normal write mode.
2. Select a column address, read "0" out and write "1" into the cell by performing the **$\overline{CS}$ before $\overline{RAS}$ refresh counter test, read-write cycle.** Repeat this operation 512 times.
3. Read the "1"s which were written in step 2 in normal read mode.
4. Using the same column address as in step 2, read "1" out and write "0" into the cell by performing the **$\overline{CS}$ before $\overline{RAS}$ refresh counter test, read-write cycle.** Repeat this operation 512 times.
5. Read "0"s which were written at in step 4 in normal read mode.
6. Repeat steps 1 to 5 using complement data.

TEST MODE

Internal organization of this device (256K × 4) allows it to be tested as if it were a 256K × 1 DRAM. Only nine of the ten addresses (A0–A8) are used in test mode; A9 is internally disabled. A test mode write cycle writes data, D (data in), to a bit in each of the four 256K × 1 blocks (B0–B3), in parallel. A test mode read cycle reads a bit in each of the four blocks. If data is the same in all four bits, Q (data out) is the same as the data in each bit. If data is not the same in all four bits, Q is high Z. See truth table and block diagram.

Test mode can be used in any timing cycle, including page mode cycles. The test mode function is enabled by holding the "TF" pin on "super voltage" for the specified period (t_{TES}, t_{TEHR}, t_{TEHC}; see TEST MODE CYCLE).

$$\text{"Super voltage"} = V_{CC} + 4.5\ V$$

where

$4.5\ V < V_{CC} < 5.5\ V$ and maximum voltage = 10.5 V.

A9 is ignored in test mode. In normal operation, the "TF" pin must either be connected to V_{IL}, or left open.

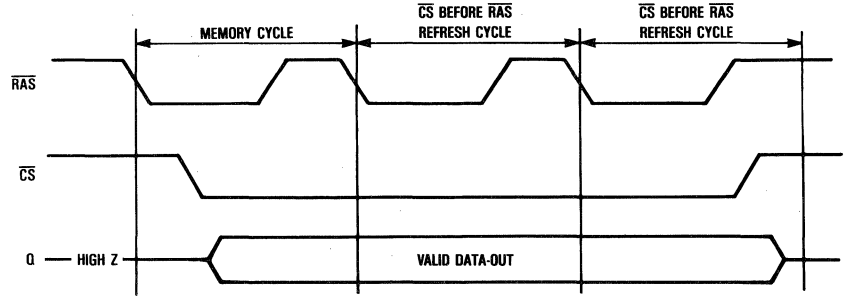
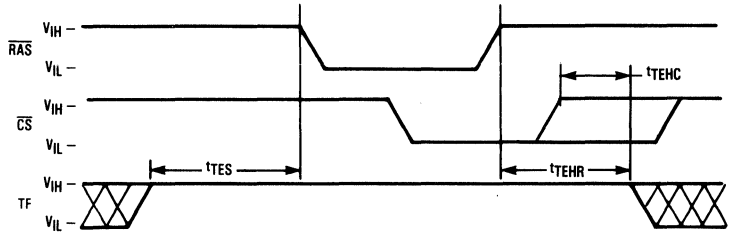


Figure 1. Hidden Refresh Cycle

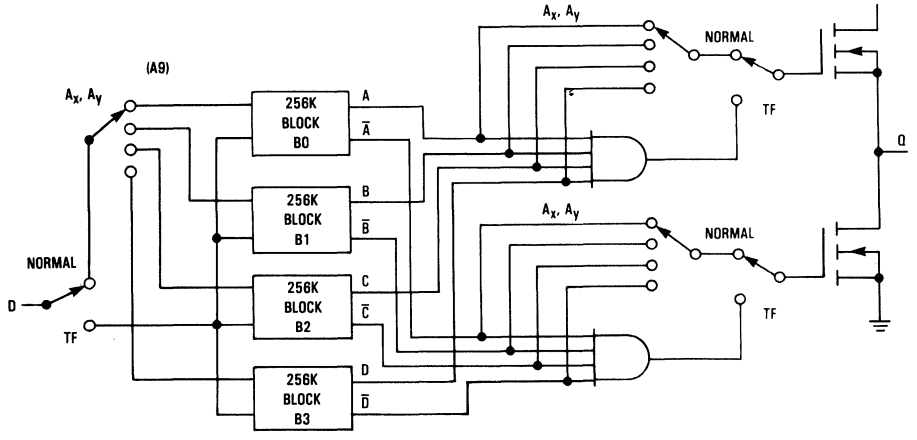
Test Mode Truth Table

D	B0	B1	B2	B3	Q
0	0	0	0	0	0
1	1	1	1	1	1
—	Any Other				High-Z

TEST MODE CYCLE



TEST FUNCTION BLOCK DIAGRAM



ORDERING INFORMATION
(Order by Full Part Number)

MCM 511002A X XX XX

- MCM — Motorola Memory Prefix
- 511002A — Part Number
- X — Package (P = 300 mil Plastic DIP, J = 300 mil SOJ, Z = Plastic ZIP)
- XX — Speed (70 = 70 ns, 80 = 80 ns, 10 = 100 ns)
- XX — Shipping Method (R2 = Tape & Reel, Blank = Rails)

Full Part Numbers—

MCM511002AP70	MCM511002AJ70	MCM511002AJ70R2	MCM511002AZ70
MCM511002AP80	MCM511002AJ80	MCM511002AJ80R2	MCM511002AZ80
MCM511002AP10	MCM511002AJ10	MCM511002AJ10R2	MCM511002AZ10

2

MCM514100
MCM51L4100

Advance Information

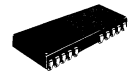
4M × 1 CMOS Dynamic RAM

Page Mode

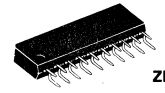
The MCM514100 is a 0.8μ CMOS high-speed, dynamic random access memory. It is organized as 4,194,304 one-bit words and fabricated with CMOS silicon-gate process technology. Advanced circuit design and fine line processing provide high performance, improved reliability, and low cost.

The MCM514100 requires only 11 address lines; row and column address inputs are multiplexed. The device is packaged in a standard 350-mil-wide J-lead small outline package, and a 100-mil zig-zag in-line package (ZIP).

- Three-State Data Output
- Common I/O with Early Write
- Fast Page Mode
- Test Mode
- TTL-Compatible Inputs and Output
- $\overline{RAS}$ Only Refresh
- $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- Hidden Refresh
- 1024 Cycle Refresh: MCM514100 = 16 ms
  MCM51L4100 = 128 ms
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}):
  MCM514100-80 and MCM51L4100-80 = 80 ns (Max)
  MCM514100-10 and MCM51L4100-10 = 100 ns (Max)
- Low Active Power Dissipation:
  MCM514100-80 and MCM51L4100-80 = 550 mW (Max)
  MCM514100-10 and MCM51L4100-10 = 468 mW (Max)
- Low Standby Power Dissipation:
  MCM514100 and MCM51L4100 = 11 mW (Max, TTL Levels)
  MCM514100 = 5.5 mW (Max, CMOS Levels)
  MCM51L4100 = 2.2 mW (Max, CMOS Levels)



J PACKAGE
PLASTIC
SMALL OUTLINE
CASE 822A

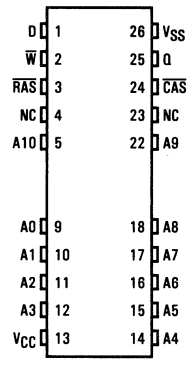


Z PACKAGE
PLASTIC
ZIG-ZAG IN-LINE
CASE 836

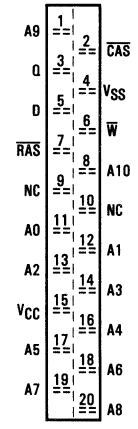
PIN NAMES	
A0-A10	Address Input
D	Data Input
Q	Data Output
$\overline{W}$	Read/Write Enable
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5 V)
V_{SS}	Ground
NC	No Connection

PIN ASSIGNMENT

SMALL OUTLINE

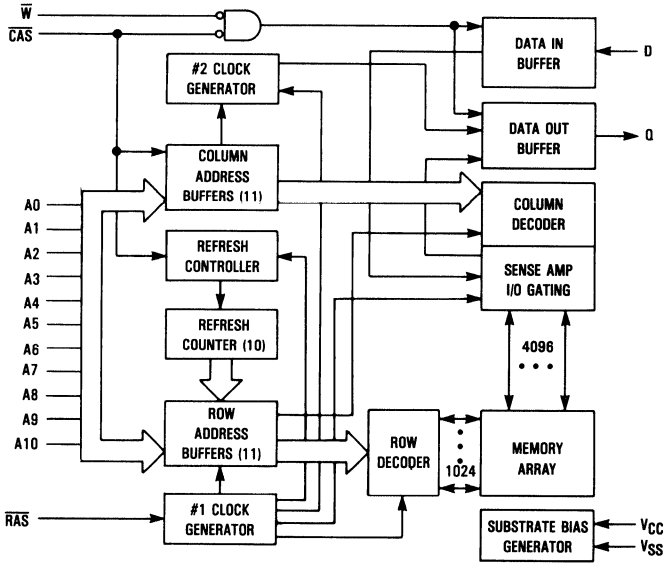


ZIG-ZAG IN-LINE



This document contains information on a new product. Specifications and information herein are subject to change without notice.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−1 to +7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−1 to +7	V
Data Out Current	I_{out}	50	mA
Power Dissipation	P_D	600	mW
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

2

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V	1
	V_{SS}	0	0	0		
Logic High Voltage, All Inputs	V_{IH}	2.4	–	6.5	V	1
Logic Low Voltage, All Inputs	V_{IL}	−1.0	–	0.8	V	1

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current MCM514100-80 and MCM51L4100-80, t_{RC} = 150 ns MCM514100-10 and MCM51L4100-10, t_{RC} = 180 ns	I_{CC1}	 – –	 100 85	mA	2
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	–	2.0	mA	
V_{CC} Power Supply Current During $\overline{RAS}$ only Refresh Cycles ($\overline{CAS}$ = V_{IH}) MCM514100-80 and MCM51L4100-80, t_{RC} = 150 ns MCM514100-10 and MCM51L4100-10, t_{RC} = 180 ns	I_{CC3}	 – –	 100 85	mA	2
V_{CC} Power Supply Current During Fast Page Mode Cycle ($\overline{RAS}$ = V_{IL}) MCM514100-80 and MCM51L4100-80, t_{PC} = 50 ns MCM514100-10 and MCM51L4100-10, t_{PC} = 60 ns	I_{CC4}	 – –	 60 50	mA	2, 4
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} − 0.2 V) MCM514100 MCM51L4100	I_{CC5}	– –	1.0 400	mA µA	
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle MCM514100-80 and MCM51L4100-80, t_{RC} = 150 ns MCM514100-10 and MCM51L4100-10, t_{RC} = 180 ns	I_{CC6}	 – –	 100 85	mA	2
V_{CC} Power Supply Current, Battery Backup Mode—MCM51L4100 only (t_{RC} = 125 µs; t_{RAS} = 1 µs; $\overline{CAS}$ = $\overline{CAS}$ Before $\overline{RAS}$ Cycle or 0.2 V; A0-A10, $\overline{W}$, D = V_{CC} − 0.2 V or 0.2 V)	I_{CC7}	–	500	µA	
Input Leakage Current (0 V ≤ V_{in} ≤ 6.5 V)	$I_{lkg(I)}$	−10	10	µA	
Output Leakage Current ($\overline{CAS}$ = V_{IH}, 0 V ≤ V_{out} ≤ 5.5 V)	$I_{lkg(O)}$	−10	10	µA	
Output High Voltage (I_{OH} = −5 mA)	V_{OH}	2.4	–	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	–	0.4	V	

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Max	Unit	Notes
Input Capacitance	A0-A10, D	C_{in}	5	pF	3
	$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$		7	pF	3
Output Capacitance ($\overline{CAS}$ = V_{IH} to Disable Output)	Q	C_{out}	7	pF	3

NOTES:
1. All voltages referenced to V_{SS}.
2. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
3. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\Delta t/\Delta V$.
4. Measured with one address transition per page mode cycle.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ, WRITE, AND READ-WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM514100-80 MCM51L4100-80		MCM514100-10 MCM51L4100-10		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	150	–	180	–	ns	5
Read-Write Cycle Time	t_{RELREL}	t_{RWC}	175	–	210	–	ns	5
Page Mode Cycle Time	t_{CELCEL}	t_{PC}	50	–	60	–	ns	
Page Mode Read-Write Cycle Time	t_{CELCEL}	t_{PRWC}	75	–	90	–	ns	
Access Time from $\overline{RAS}$	t_{RELQV}	t_{RAC}	–	80	–	100	ns	6, 7
Access Time from $\overline{CAS}$	t_{CELQV}	t_{CAC}	–	20	–	25	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	–	40	–	50	ns	6, 9
Access Time from Precharge $\overline{CAS}$	t_{CEHQV}	t_{CPA}	–	45	–	55	ns	6
$\overline{CAS}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	0	–	0	–	ns	6
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	20	0	20	ns	10
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{REHREL}	t_{RP}	60	–	70	–	ns	
$\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RAS}	80	10,000	100	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	80	200,000	100	200,000	ns	
$\overline{RAS}$ Hold Time	t_{CELREH}	t_{RSH}	20	–	25	–	ns	
$\overline{CAS}$ Hold Time	t_{RELCEH}	t_{CSH}	80	–	100	–	ns	
$\overline{CAS}$ Pulse Width	t_{CELCEH}	t_{CAS}	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RELCEL}	t_{RCD}	20	60	25	75	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	40	20	50	ns	12
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	–	10	–	ns	
$\overline{CAS}$ Precharge Time	t_{CEHCEL}	t_{CP}	10	–	10	–	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	–	0	–	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	–	15	–	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	–	0	–	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	–	20	–	ns	
Column Address Hold Time Referenced to $\overline{RAS}$	t_{RELAX}	t_{AR}	60	–	75	–	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{AVREH}	t_{RAL}	40	–	50	–	ns	

(continued)

NOTES:

1. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
6. Measured with a current load equivalent to 2 TTL (−200 µA, +4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
8. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
9. Assumes that $t_{RAD} \geq t_{RAD}$ (max).
10. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
12. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.

2

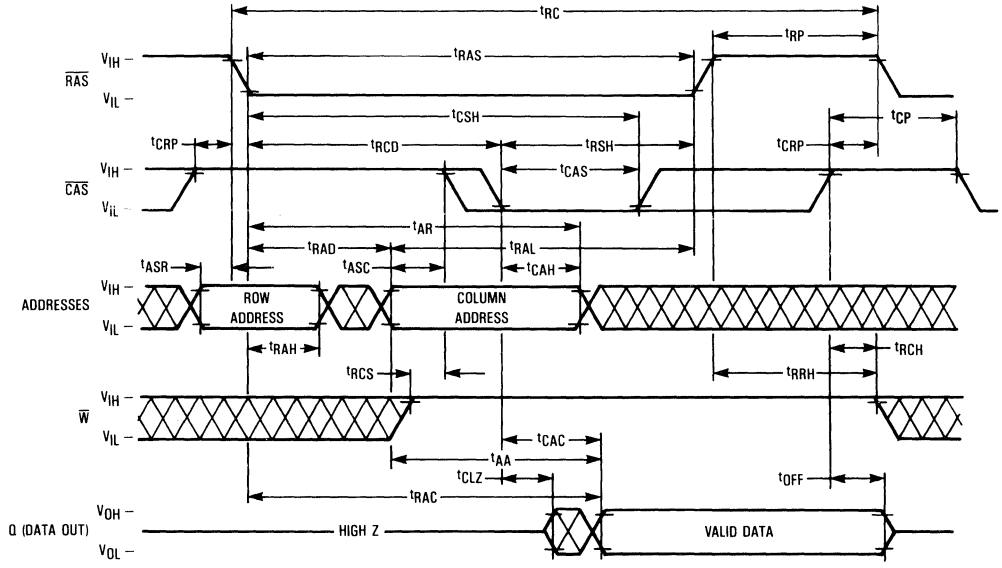
READ, WRITE, AND READ-WRITE CYCLES (Continued)

Parameter	Symbol		MCM514100-80 MCM51L4100-80		MCM514100-10 MCM51L4100-10		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	–	0	–	ns	
Read Command Hold Time Referenced to $\overline{CAS}$	t_{CEHWX}	t_{RCH}	0	–	0	–	ns	13
Read Command Hold Time Referenced to $\overline{RAS}$	t_{REHWX}	t_{RRH}	0	–	0	–	ns	13
Write Command Hold Time Referenced to $\overline{CAS}$	t_{CELWH}	t_{WCH}	15	–	20	–	ns	
Write Command Hold Time Referenced to $\overline{RAS}$	t_{RELWH}	t_{WCR}	60	–	75	–	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	15	–	20	–	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{WLREH}	t_{RWL}	20	–	25	–	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{WLCEH}	t_{CWL}	20	–	25	–	ns	
Data in Setup Time	t_{DVCEL}	t_{DS}	0	–	0	–	ns	14
Data in Hold Time	t_{CELDX}	t_{DH}	15	–	20	–	ns	14
Data in Hold Time Referenced to $\overline{RAS}$	t_{RELDX}	t_{DHR}	60	–	75	–	ns	
Refresh Period MCM514100 MCM51L4100	t_{RVRV}	t_{RFSH}	– –	16 128	– –	16 128	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	–	0	–	ns	15
$\overline{CAS}$ to Write Delay	t_{CELWL}	t_{CWD}	20	–	25	–	ns	15
$\overline{RAS}$ to Write Delay	t_{RELWL}	t_{RWD}	80	–	100	–	ns	15
Column Address to Write Delay Time	t_{AVWL}	t_{AWD}	40	–	50	–	ns	15
$\overline{CAS}$ Precharge to Write Delay Time (Page Mode)	t_{CEHWL}	t_{CPWD}	45	–	55	–	ns	15
$\overline{CAS}$ Setup Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEL}	t_{CSR}	5	–	10	–	ns	
$\overline{CAS}$ Hold Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEH}	t_{CHR}	15	–	20	–	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	t_{REHCEL}	t_{RPC}	0	–	0	–	ns	
$\overline{CAS}$ Precharge Time for $\overline{CAS}$ Before $\overline{RAS}$ Counter Test	t_{CEHCEL}	t_{CPT}	40	–	50	–	ns	
Write Command Set Up Time (Test Mode)	t_{WLREL}	t_{WTS}	10	–	10	–	ns	
Write Command Hold Time (Test Mode)	t_{RELWH}	t_{WTH}	10	–	10	–	ns	
Write to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh)	t_{WHREL}	t_{WRP}	10	–	10	–	ns	
Write to $\overline{RAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh)	t_{RELWL}	t_{WRH}	10	–	10	–	ns	

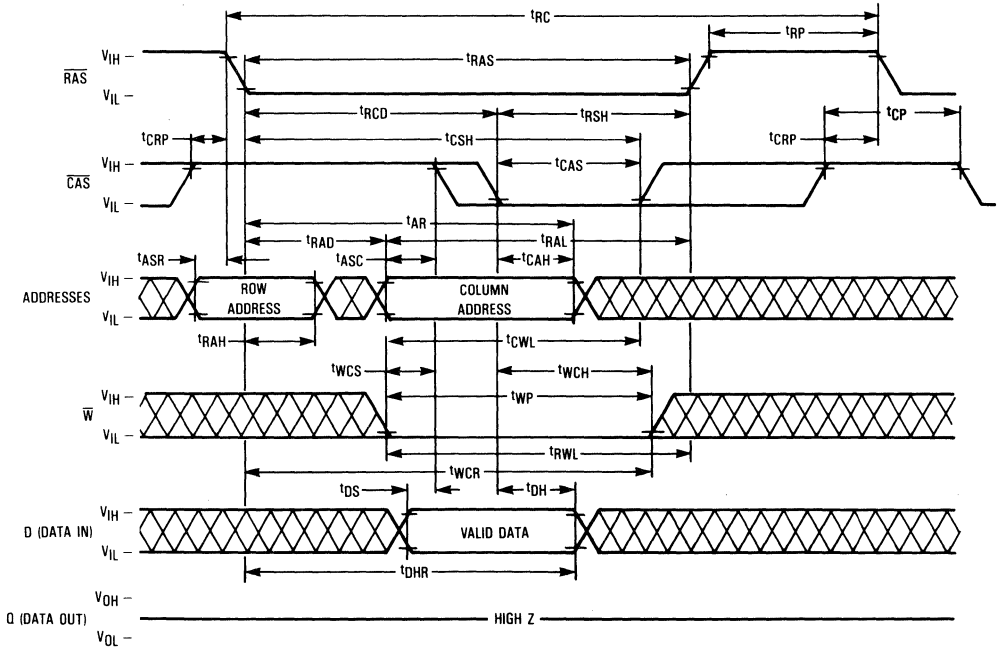
NOTES:

13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{W}$ leading edge in read-write cycles.
15. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min), and $t_{CPWD} \geq t_{CPWD}$ (min) (page mode), the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

READ CYCLE



EARLY WRITE CYCLE



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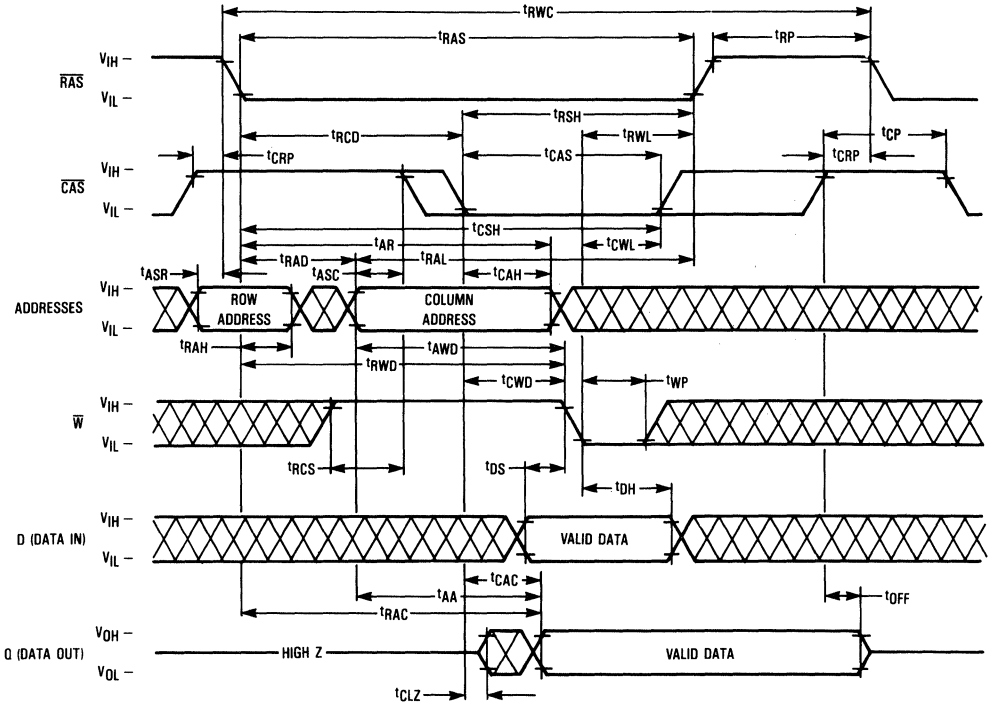
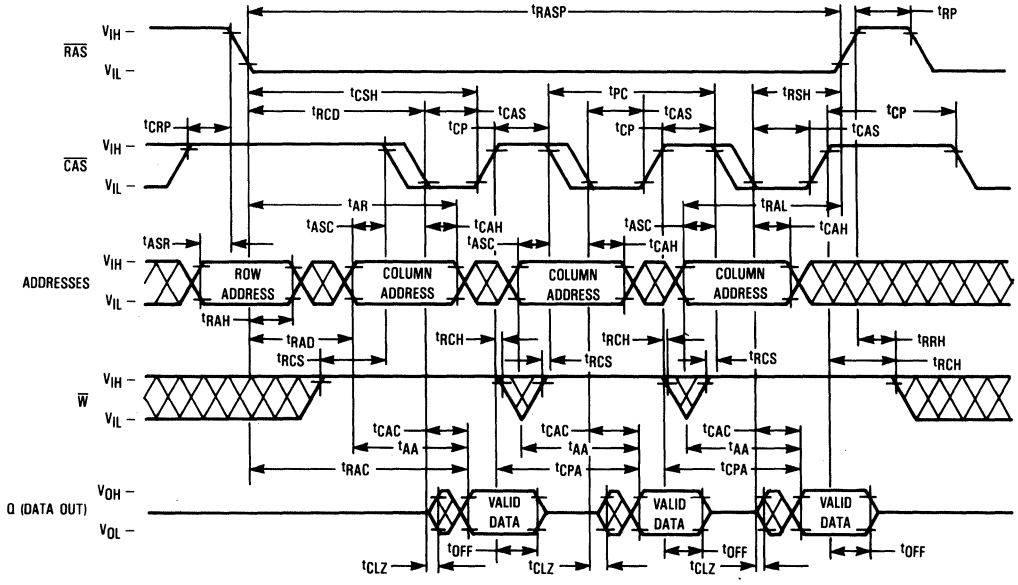
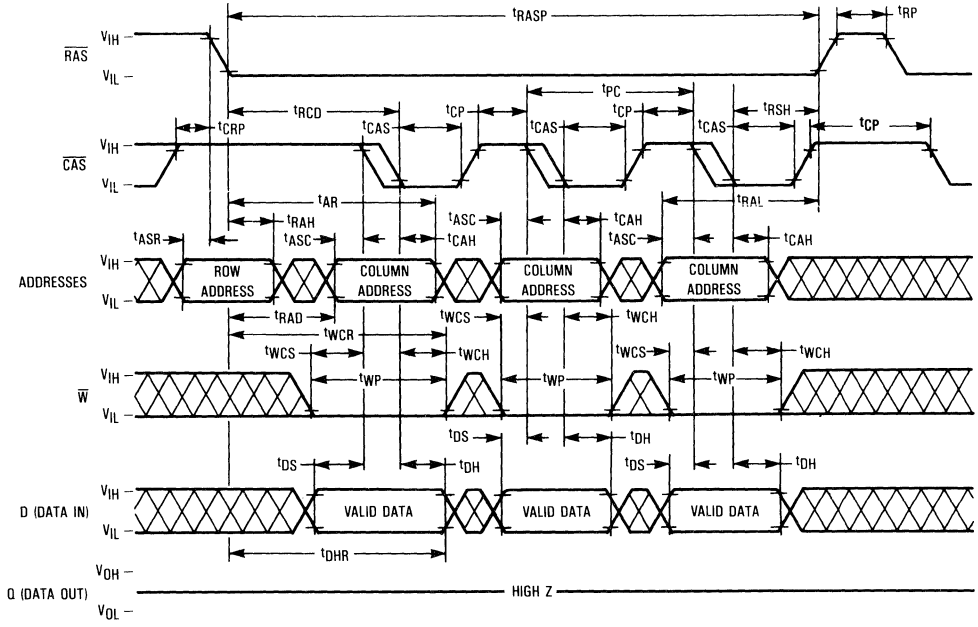
READ-WRITE CYCLE



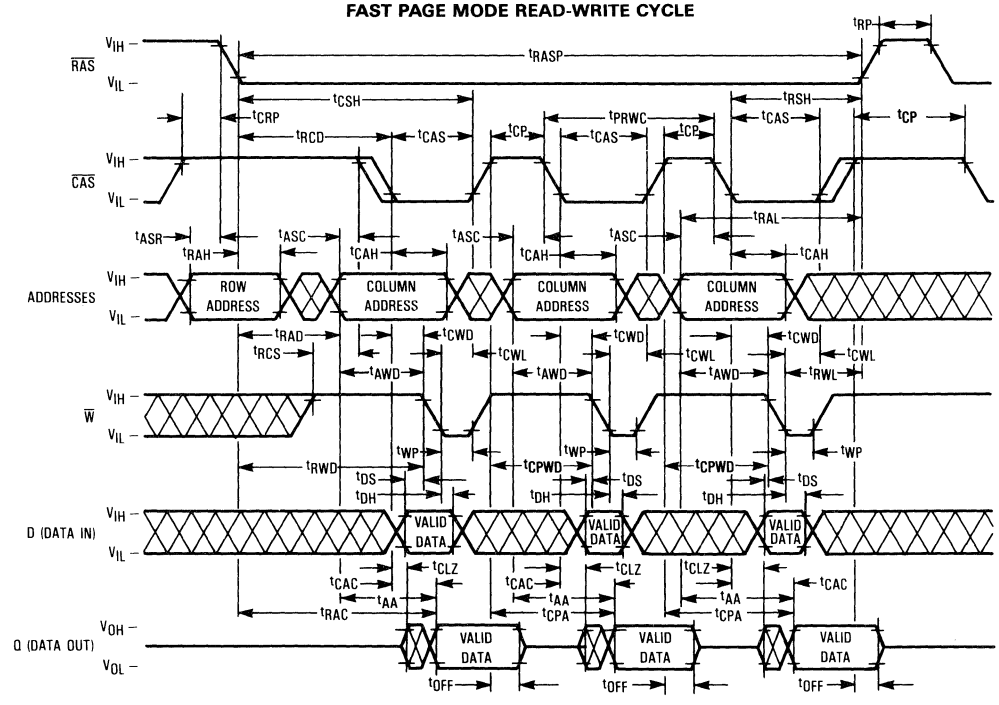
FAST PAGE MODE READ CYCLE



FAST PAGE MODE EARLY WRITE CYCLE



FAST PAGE MODE READ-WRITE CYCLE



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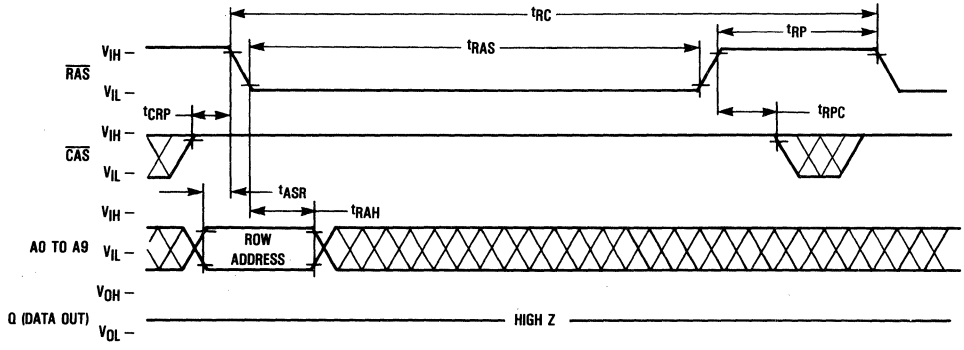
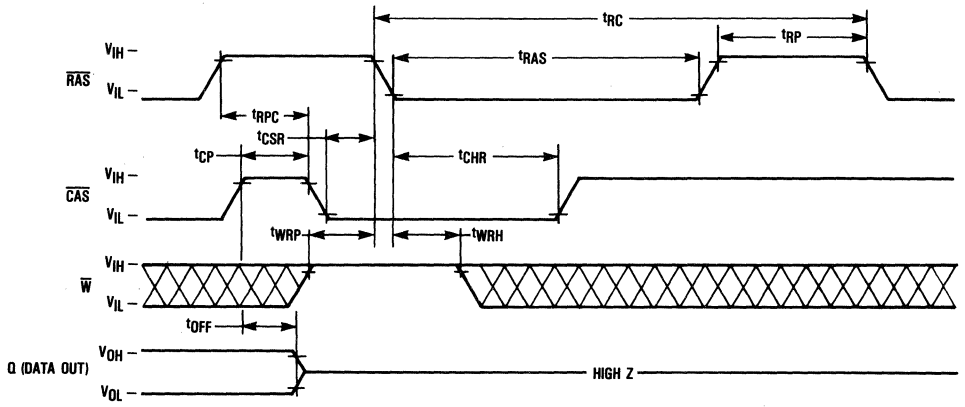
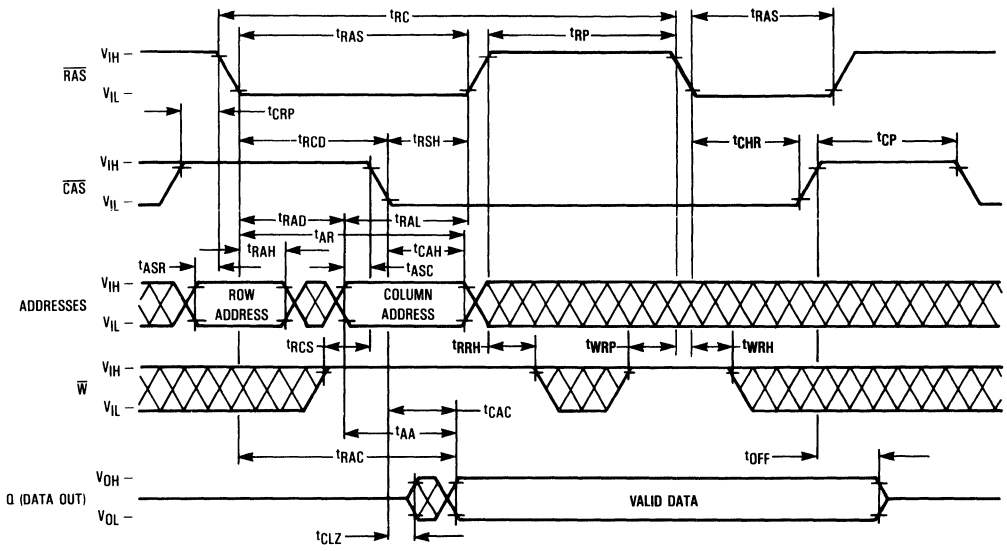
$\overline{RAS}$ ONLY REFRESH CYCLE
($\overline{W}$ and A10 are Don't Care)



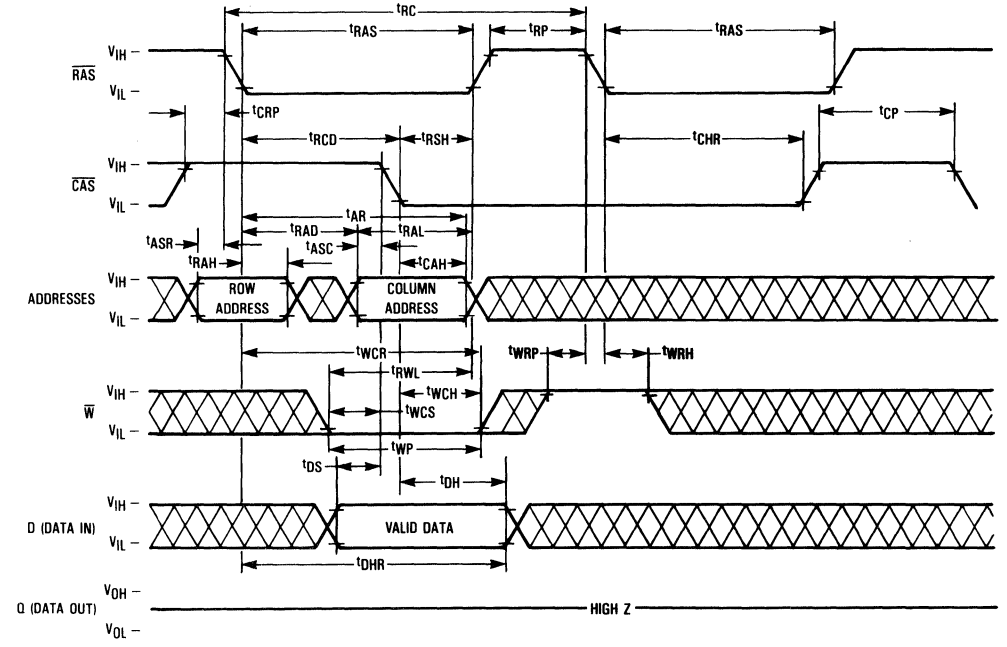
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE
(A0 to A10 are Don't Care)



HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (EARLY WRITE)



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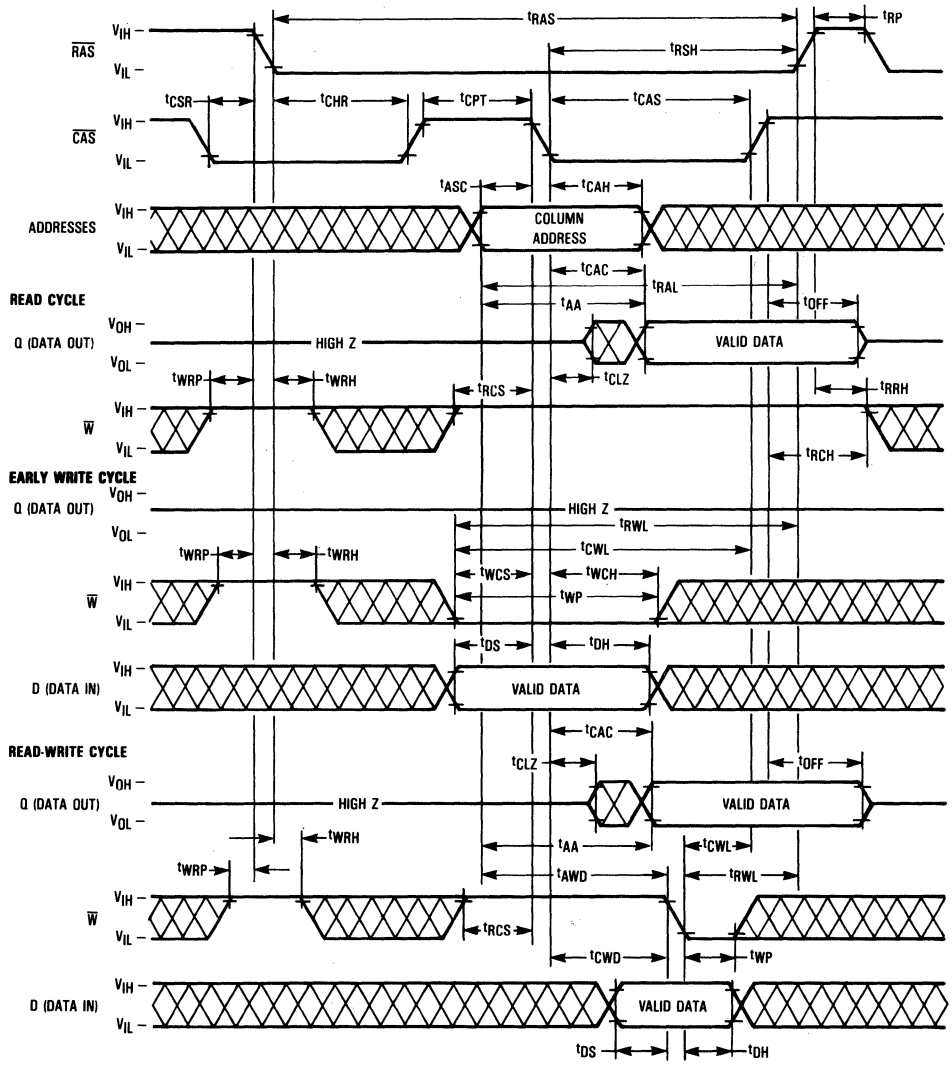
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



DEVICE INITIALIZATION

On power-up an initial pause of 200 microseconds is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize all dynamic nodes within the RAM. During an extended inactive state (greater than 16 milliseconds with the device powered up), a wake up sequence of eight active cycles is necessary to assure proper operation.

ADDRESSING THE RAM

The eleven address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks, row address strobe ($\overline{RAS}$) and column address strobe ($\overline{CAS}$), into two separate 11-bit address fields. A total of twenty two address bits, eleven rows and eleven columns, will decode one of the 4,194,304 bit locations in the device. $\overline{RAS}$ active transition is followed by $\overline{CAS}$ active transition (active = V_{IL}, t_{RCD} minimum) for all read or write cycles. The delay between $\overline{RAS}$ and $\overline{CAS}$ active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

The external $\overline{CAS}$ signal is ignored until an internal $\overline{RAS}$ signal is available. This "gate" feature on the external $\overline{CAS}$ clock enables the internal $\overline{CAS}$ line as soon as the row address hold time (t_{RAH}) specification is met (and defines t_{RCD} minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{CAS}$ clock.

There are three other variations in addressing the 4M RAM: **$\overline{RAS}$ only refresh cycle**, **$\overline{CAS}$ before $\overline{RAS}$ refresh cycle**, and **page mode**. All three are discussed in separate sections that follow.

READ CYCLE

The DRAM may be read with four different cycles: "normal" random read cycle, page mode read cycle, read-write cycle, and page mode read-write cycle. The normal read cycle is outlined here, while the other cycles are discussed in separate sections.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with $\overline{RAS}$ and $\overline{CAS}$ active transitions latching the desired bit location. The write ($\overline{W}$) input level must be high (V_{IH}), t_{RCS} (minimum) before the $\overline{CAS}$ active transition, to enable read mode.

Both the $\overline{RAS}$ and $\overline{CAS}$ clocks trigger a sequence of events which are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window. However, $\overline{CAS}$ must be active before or at t_{RCD} maximum to guarantee valid data out (Q) at t_{RAC} (access time from $\overline{RAS}$ active transition). If the t_{RCD} maximum is exceeded, read access time is determined by the $\overline{CAS}$ clock active transition (t_{CAC}).

The $\overline{RAS}$ and $\overline{CAS}$ clocks must remain active for a minimum time of t_{RAS} and t_{CAS} respectively, to complete the read cycle. $\overline{W}$ must remain high throughout the cycle, and for time t_{RRH} or t_{RCH} after $\overline{RAS}$ or $\overline{CAS}$ inactive transition, respectively, to maintain the data at that bit location. Once $\overline{RAS}$ transitions to inactive, it must remain inactive for a minimum time of t_{RP} to precharge the internal device circuitry for the next active cycle. Q is valid, but not latched, as long as the $\overline{CAS}$ clock is active. When the $\overline{CAS}$ clock transitions to inactive, the output will switch to High Z (three-state).

WRITE CYCLE

The user can write to the DRAM with any of four cycles; early write, late write, page mode early write, and page mode read-write. Early and late write modes are discussed here, while page mode write operations are covered in another section.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of $\overline{W}$ to active (V_{IL}). Early and late write modes are distinguished by the active transition of $\overline{W}$, with respect to $\overline{CAS}$. Minimum active time t_{RAS} and t_{CAS}, and precharge time t_{RP} apply to write mode, as in the read mode.

An early write cycle is characterized by $\overline{W}$ active transition at minimum time t_{WCS} before $\overline{CAS}$ active transition. Data in (D) is referenced to $\overline{CAS}$ in an early write cycle. $\overline{RAS}$ and $\overline{CAS}$ clocks must stay active for t_{RWL} and t_{CWL}, respectively, after the start of the early write operation to complete the cycle.

Q remains in three-state condition throughout an early write cycle because $\overline{W}$ active transition precedes or coincides with $\overline{CAS}$ active transition, keeping data-out buffers disabled. This feature can be utilized on systems with a common I/O bus, provided all writes are performed with early write cycles, to prevent bus contention.

A late write cycle occurs when $\overline{W}$ active transition is made after $\overline{CAS}$ active transition. $\overline{W}$ active transition could be delayed for almost 10 microseconds after $\overline{CAS}$ active transition, ($t_{RCD} + t_{CWD} + t_{RWL} + 2t_T) \leq t_{RAS}$, if other timing minimums (t_{RCD}, t_{RWL} and t_T) are maintained. D is referenced to $\overline{W}$ active transition in a late write cycle. Output buffers are enabled by $\overline{CAS}$ active transition but Q may be indeterminate—see note 15 of AC operating conditions table. $\overline{RAS}$ and $\overline{CAS}$ must remain active for t_{RWL} and t_{CWL}, respectively, after $\overline{W}$ active transition to complete the write cycle.

READ-WRITE CYCLE

A read-write cycle performs a read and then a write at the same address, during the same cycle. This cycle is basically a late write cycle, as discussed in the **WRITE CYCLE** section, except $\overline{W}$ must remain high for t_{CWD} minimum after the $\overline{CAS}$ active transition, to guarantee valid Q before writing the bit.

PAGE MODE CYCLES

Page mode allows fast successive data operations at all 2048 column locations on a selected row of the 4M dynamic RAM. Read access time in page mode (t_{CAC}) is typically half the regular $\overline{RAS}$ clock access time, t_{RAC}. Page mode operation consists of keeping $\overline{RAS}$ active while toggling $\overline{CAS}$ between V_{IH} and V_{IL}. The row is latched by $\overline{RAS}$ active transition, while each $\overline{CAS}$ active transition allows selection of a new-column location on the row.

A page mode cycle is initiated by a normal read, write, or read-write cycle, as described in prior sections. Once the timing requirements for the first cycle are met, $\overline{CAS}$ transitions to inactive for minimum of t_{CP}, while $\overline{RAS}$ remains low (V_{IL}). The second $\overline{CAS}$ active transition while $\overline{RAS}$ is low initiates the first page mode cycle (t_{PC} or t_{PRWC}). Either a read, write,

2

or read-write operation can be performed in a page mode cycle, subject to the same conditions as in normal operation (previously described). These operations can be intermixed in consecutive page mode cycles and performed in any order. The maximum number of consecutive page mode cycles is limited by t_{RASP}. Page mode operation is ended when $\overline{RAS}$ transitions to inactive, coincident with or following $\overline{CAS}$ inactive transition.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Each bit must be periodically **refreshed** (recharged) to maintain the correct bit state. Bits in the MCM514100 require refresh every 16 milliseconds, while refresh time for the MCM51L4100 is 128 milliseconds.

This is accomplished by cycling through the 1024 row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds for the MCM514100, and 124.8 microseconds for the MCM51L4100. Burst refresh, a refresh of all 1024 rows consecutively, must be performed every 16 milliseconds on the MCM514100 and 128 milliseconds on the MCM51L4100.

A normal read, write, or read-write operation to the RAM will refresh all the bits (4096) associated with the particular row decoded. Three other methods of refresh, **$\overline{RAS}$-only refresh**, **$\overline{CAS}$ before $\overline{RAS}$ refresh**, and **hidden refresh** are available on this device for greater system flexibility.

$\overline{RAS}$-Only Refresh

$\overline{RAS}$-only refresh consists of $\overline{RAS}$ transition to active, latching the row address to be refreshed, while $\overline{CAS}$ remains high (V_{IH}) throughout the cycle. An external counter is employed to ensure all rows are refreshed within the specified limit.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh

$\overline{CAS}$ before $\overline{RAS}$ refresh is enabled by bringing $\overline{CAS}$ active before $\overline{RAS}$. This clock order activates an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle. The output buffer remains at the same state it was in during the previous cycle (hidden refresh). $\overline{W}$ must be inactive for time t_{WRP} before and time t_{WRH} after $\overline{RAS}$ active transition to prevent switching the device into a **test mode cycle**.

Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding $\overline{CAS}$ active the end of a read or write cycle, while $\overline{RAS}$ cycles inactive for t_{RP} and back to active, starts the hidden refresh. This is essentially the execution of a $\overline{CAS}$ before $\overline{RAS}$ refresh from a cycle in progress (see Figure 1.) $\overline{W}$ is subject to the same conditions with respect to $\overline{RAS}$ active transition (to prevent test mode cycle) as in $\overline{CAS}$ before $\overline{RAS}$ refresh.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST

The internal refresh counter of this device can be tested with a **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test**. This test is performed with a read-write operation. During the test, the internal refresh counter generates the row address, while the external address supplies the column address. The entire array is refreshed after 1024 cycles, as indicated by the check data written in each row. See **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test cycle** timing diagram.

The test can be performed after a minimum of 8 **$\overline{CAS}$ before $\overline{RAS}$** initialization cycles. Test procedure:

1. Write "0"s into all memory cells with normal write mode.
2. Select a column address, read "0" out and write "1" into the cell by performing the **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test, read-write cycle**. Repeat this operation 1024 times.
3. Read the "1"s which were written in step 2 in normal read mode.
4. Using the same starting column address as in step 2, read "1" out and write "0" into the cell by performing the **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test, read-write cycle**. Repeat this operation 1024 times.
5. Read "0"s which were written in step 4 in normal read mode.
6. Repeat steps 1 to 5 using complement data.

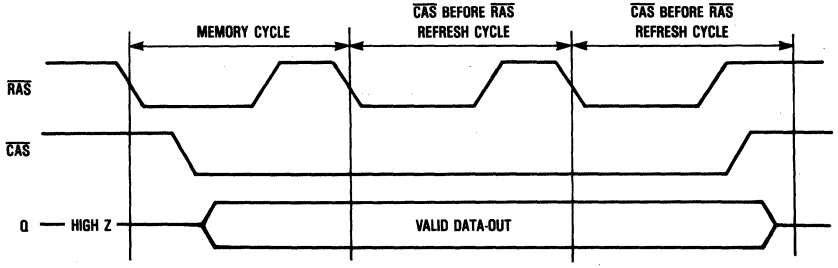


Figure 1. Hidden Refresh Cycle

TEST MODE

The internal organization of this device (512K × 8) allows it to be tested as if it were a 512K × 1 DRAM. Nineteen of the twenty two addresses are used when operating the device in test mode. Row address A10, and column addresses A0 and A10 are ignored by the device in test mode. A test mode cycle reads and/or writes data to a bit in each of the eight 512K blocks (B0-B7) in parallel. External data out is determined by the internal test mode logic of the device. See truth table and test mode block diagram following.

Test mode is enabled by performing a **test mode cycle** (see test mode timing diagram and parameter specifications table). Test mode is disabled by a **$\overline{RAS}$ only refresh** cycle or **$\overline{CAS}$ before $\overline{RAS}$ refresh** cycle. The test mode performs refresh with the internal refresh counter like a **$\overline{CAS}$ before $\overline{RAS}$ refresh.**

Test Mode Truth Table

D	B0	B1	B2	B3	B4	B5	B6	B7	Q
0	0	0	0	0	0	0	0	0	1
1	1	1	1	1	1	1	1	1	1
—	Any Other								0

TEST MODE
AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ, WRITE, AND READ-WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM514100-80 MCM51L4100-80		MCM514100-10 MCM51L4100-10		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	155	—	185	—	ns	5
Read-Write Cycle Time	t_{RELREL}	t_{RWC}	180	—	215	—	ns	5
Page Mode Cycle Time	t_{CELCEL}	t_{PC}	55	—	65	—	ns	
Page Mode Read-Write Cycle Time	t_{CELCEL}	t_{PRWC}	80	—	95	—	ns	
Access Time from $\overline{RAS}$	t_{RELQV}	t_{RAC}	—	85	—	105	ns	6, 7
Access Time from $\overline{CAS}$	t_{CELQV}	t_{CAC}	—	25	—	30	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	—	45	—	55	ns	6, 9
Access Time from Precharge $\overline{CAS}$	t_{CEHQV}	t_{CPA}	—	50	—	60	ns	6
$\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RAS}	85	10,000	105	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	85	200,000	105	200,000	ns	
$\overline{RAS}$ Hold Time	t_{CELREH}	t_{RSH}	25	—	30	—	ns	
$\overline{CAS}$ Hold Time	t_{RELCEH}	t_{CSH}	85	—	105	—	ns	
$\overline{CAS}$ Pulse Width	t_{CELCEH}	t_{CAS}	25	10,000	30	10,000	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{AVREH}	t_{RAL}	45	—	55	—	ns	
$\overline{CAS}$ to Write Delay	t_{CELWL}	t_{CWD}	25	—	30	—	ns	10
$\overline{RAS}$ to Write Delay	t_{RELWL}	t_{RWD}	85	—	105	—	ns	10
Column Address to Write Delay Time	t_{AVWL}	t_{AWD}	45	—	55	—	ns	10
$\overline{CAS}$ Precharge to Write Delay Time (Page Mode)	t_{CEHWL}	t_{CPWD}	50	—	60	—	ns	10

NOTES:

1. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
6. Measured with a current load equivalent to 2 TTL (−200 μA, +4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
8. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
9. Assumes that $t_{RAD} \geq t_{RAD}$ (max).
10. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min), and $t_{CPWD} \geq t_{CPWD}$ (min) (page mode), the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

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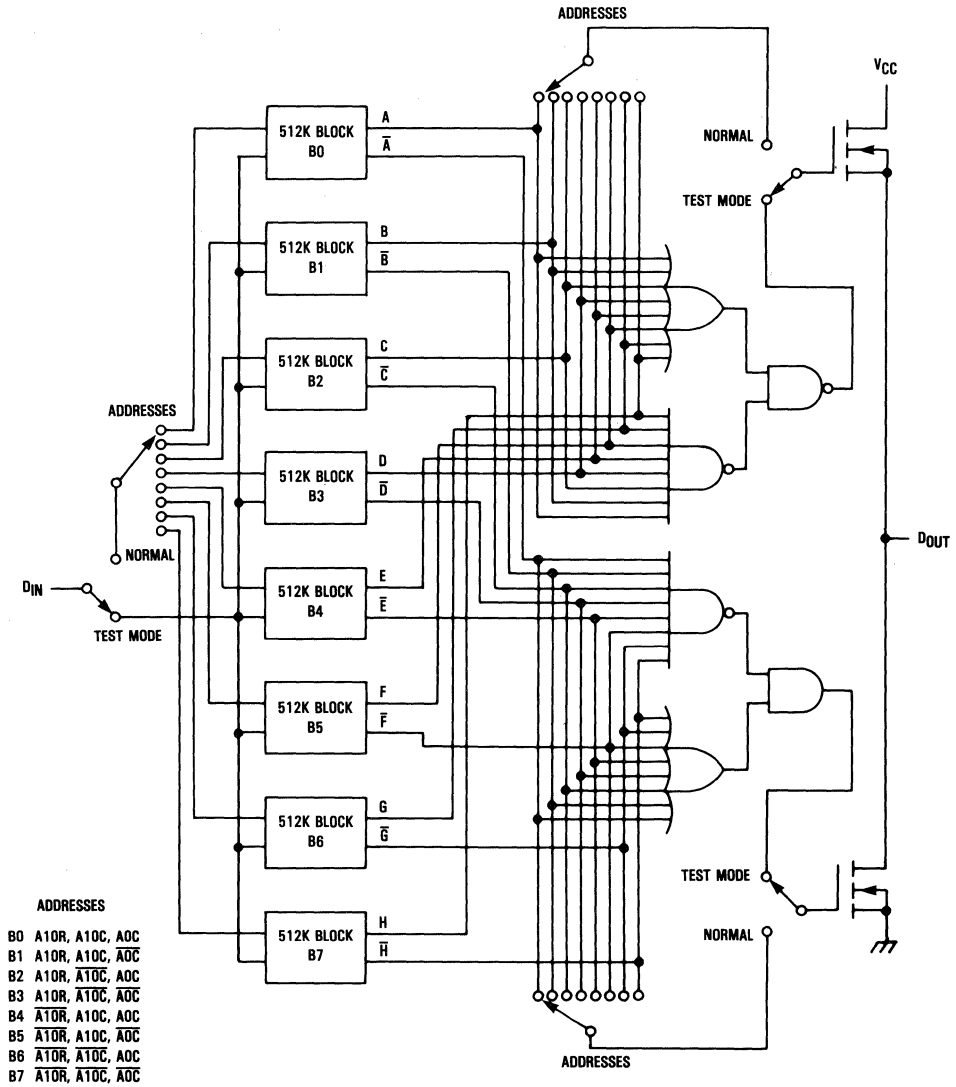
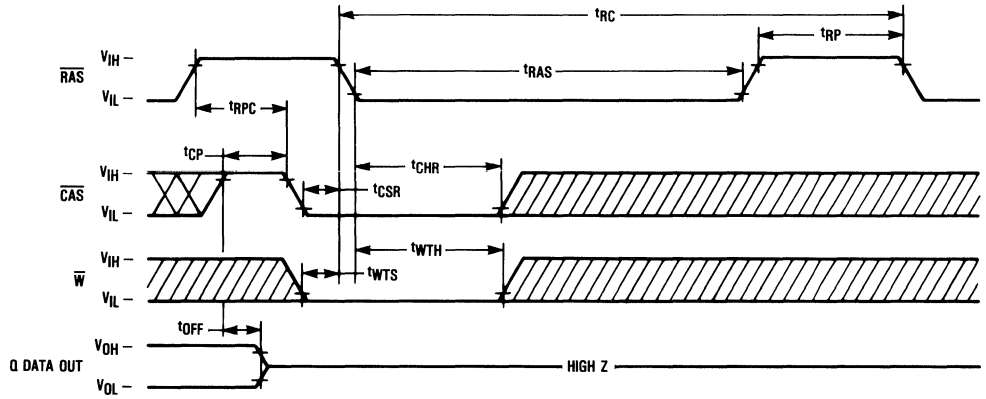
TEST MODE BLOCK DIAGRAM



ADDRESSES

B0 A10R, A10C, A0C
B1 A10R, A10C, $\overline{A0C}$
B2 A10R, $\overline{A10C}$, A0C
B3 A10R, $\overline{A10C}$, $\overline{A0C}$
B4 $\overline{A10R}$, A10C, A0C
B5 $\overline{A10R}$, A10C, $\overline{A0C}$
B6 $\overline{A10R}$, $\overline{A10C}$, A0C
B7 $\overline{A10R}$, $\overline{A10C}$, $\overline{A0C}$

TEST MODE CYCLE
(D and A0 to A10 are Don't Care)



ORDERING INFORMATION
(Order by Full Part Number)

MCM 514100 or 51L4100 X XX XX

- Motorola Memory Prefix
- Part Number
- Shipping Method (R2 = Tape & Reel, Blank = Rails)
- Speed (80 = 80 ns, 10 = 100 ns)
- Package (J = Plastic SO with J leads, Z = Plastic ZIP)

Full Part Numbers—	MCM514100J80	MCM514100J80R2	MCM514100Z80
	MCM514100J10	MCM514100J10R2	MCM514100Z10
	MCM51L4100J80	MCM51L4100J80R2	MCM51L4100Z80
	MCM51L4100J10	MCM51L4100J10R2	MCM51L4100Z10

2

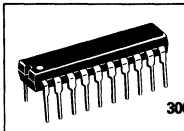
MCM514256A
MCM51L4256A

256K x 4 CMOS Dynamic RAM
Page Mode

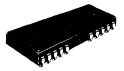
The MCM514256A is a 1.0μ CMOS high-speed, dynamic random access memory. It is organized as 262,144 four-bit words and fabricated with CMOS silicon-gate process technology. Advanced circuit design and fine line processing provide high performance, improved reliability, and low cost.

The MCM514256A requires only nine address lines; row and column address inputs are multiplexed. The device is packaged in a standard 300-mil dual-in-line package (DIP), a 300-mil SOJ plastic package, and a 100-mil zig-zag in-line plastic package (ZIP).

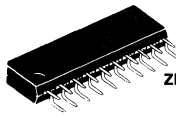
- Three-State Data Output
- Fast Page Mode
- TTL-Compatible Inputs and Output
- $\overline{RAS}$ Only Refresh
- $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- Hidden Refresh
- 512 Cycle Refresh:
  - MCM514256A = 8 ms
  - MCM51L4256A = 64 ms
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}):
  - MCM514256A-70 and MCM51L4256A-70 = 70 ns (Max)
  - MCM514256A-80 and MCM51L4256A-80 = 80 ns (Max)
  - MCM514256A-10 and MCM51L4256A-10 = 100 ns (Max)
- Low Active Power Dissipation:
  - MCM514256A-70 and MCM51L4256A-70 = 440 mW (Max)
  - MCM514256A-80 and MCM51L4256A-80 = 385 mW (Max)
  - MCM514256A-10 and MCM51L4256A-10 = 330 mW (Max)
- Low Standby Power Dissipation:
  - MCM514256A and MCM51L4256A = 11 mW (Max), TTL Levels
  - MCM514256A = 5.5 mW (Max), CMOS Levels
  - MCM51L4256A = 1.1 mW (Max), CMOS Levels



P PACKAGE
300 MIL PLASTIC
CASE 738A



J PACKAGE
300 MIL SOJ
CASE 822

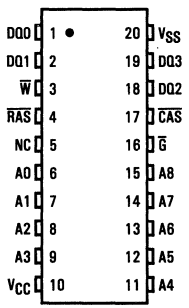


Z PACKAGE
PLASTIC
ZIG-ZAG IN-LINE
CASE 836

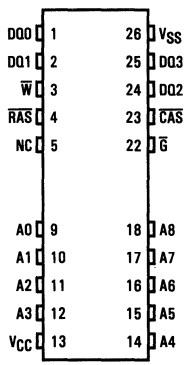
PIN NAMES	
A0-A8	Address Input
DQ0-DQ3	Data Input/Output
$\overline{G}$	Output Enable
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5 V)
V_{SS}	Ground
NC	No Connection

PIN ASSIGNMENT

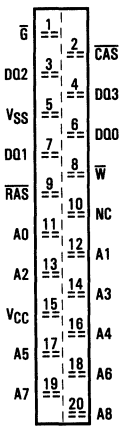
DUAL-IN-LINE



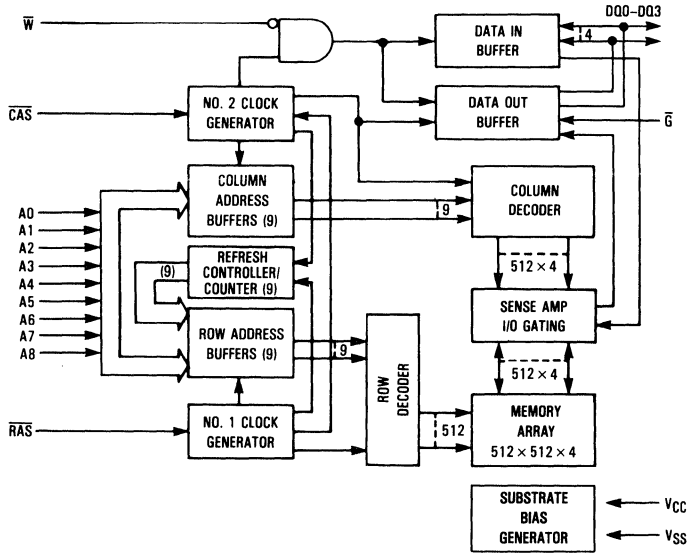
SMALL OUTLINE



ZIG-ZAG IN-LINE



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−1 to +7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−1 to +7	V
Data Out Current	I_{out}	50	mA
Power Dissipation	P_D	600	mW
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

2

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V	1
	V_{SS}	0	0	0		
Logic High Voltage, All Inputs	V_{IH}	2.4	–	6.5	V	1
Logic Low Voltage, All Inputs	V_{IL}	−1.0	–	0.8	V	1

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current	I_{CC1}			mA	2
MCM514256A-70 and MCM51L4256A-70, t_{RC} = 130 ns		–	80		
MCM514256A-80 and MCM51L4256A-80, t_{RC} = 150 ns		–	70		
MCM514256A-10 and MCM51L4256A-10, t_{RC} = 180 ns		–	60		
V_{CC} Power Supply Current (Standby) ($\overline{RAS} = \overline{CAS} = V_{IH}$)	I_{CC2}	–	2.0	mA	
V_{CC} Power Supply Current During $\overline{RAS}$ only Refresh Cycles ($\overline{CAS} = V_{IH}$)	I_{CC3}			mA	2
MCM514256A-70 and MCM51L4256A-70, t_{RC} = 130 ns		–	80		
MCM514256A-80 and MCM51L4256A-80, t_{RC} = 150 ns		–	70		
MCM514256A-10 and MCM51L4256A-10, t_{RC} = 180 ns		–	60		
V_{CC} Power Supply Current During Fast Page Mode Cycle ($\overline{RAS} = V_{IL}$)	I_{CC4}			mA	2, 3
MCM514256A-70 and MCM51L4256A-70, t_{PC} = 40 ns		–	60		
MCM514256A-80 and MCM51L4256A-80, t_{PC} = 45 ns		–	50		
MCM514256A-10 and MCM51L4256A-10, t_{PC} = 55 ns		–	40		
V_{CC} Power Supply Current (Standby) ($\overline{RAS} = \overline{CAS} = V_{CC} - 0.2$ V) MCM514256A	I_{CC5}	–	1.0	mA	
MCM51L4256A		–	200	µA	
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle	I_{CC6}			mA	2
MCM514256A-70 and MCM51L4256A-70, t_{RC} = 130 ns		–	80		
MCM514256A-80 and MCM51L4256A-80, t_{RC} = 150 ns		–	70		
MCM514256A-10 and MCM51L4256A-10, t_{RC} = 180 ns		–	60		
V_{CC} Power Supply Current, Battery Backup Mode—MCM51L4256A only (t_{RC} = 125 µs; t_{RAS} = 1 µs; $\overline{CAS} = \overline{CAS}$ Before $\overline{RAS}$ Cycle or 0.2 V; A0-A8, $\overline{G}$, $\overline{W}$, DQ0-DQ3 = V_{CC} − 0.2 V or 0.2 V)	I_{CC7}	–	300	µA	
Input Leakage Current (0 V ≤ V_{in} ≤ 6.5 V)	$I_{lkg(I)}$	−10	10	µA	
Output Leakage Current ($\overline{CAS} = V_{IH}$, 0 V ≤ V_{out} ≤ 5.5 V)	$I_{lkg(O)}$	−10	10	µA	
Output High Voltage (I_{OH} = −5 mA)	V_{OH}	2.4	–	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	–	0.4	V	

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Max	Unit	Notes
Input Capacitance	A0-A8	C_{in}	5	pF	4
	$\overline{G}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$		7	pF	4
Output Capacitance ($\overline{CAS} = V_{IH}$ to Disable Output)	DQ0-DQ3	C_{out}	7	pF	4

NOTES:
1. All voltages referenced to V_{SS}.
2. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
3. Measured with one address transition per page mode cycle.
4. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\Delta t/\Delta V$.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ, WRITE, AND READ-WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM514256A-70 MCM51L4256A-70		MCM514256A-80 MCM51L4256A-80		MCM514256A-10 MCM51L4256A-10		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	130	–	150	–	180	–	ns	5
Read-Write Cycle Time	t_{RELREL}	t_{RMW}	185	–	205	–	245	–	ns	5
Fast Page Mode Cycle Time	t_{CELCEL}	t_{PC}	40	–	45	–	55	–	ns	
Fast Page Mode Read-Write Cycle Time	t_{CELCEL}	t_{PRMW}	95	–	100	–	115	–	ns	
Access Time from $\overline{RAS}$	t_{RELQV}	t_{RAC}	–	70	–	80	–	100	ns	6, 7
Access Time from $\overline{CAS}$	t_{CELQV}	t_{CAC}	–	20	–	20	–	25	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	–	35	–	40	–	50	ns	6, 9
Access Time from Precharge $\overline{CAS}$	t_{CEHQV}	t_{CPA}	–	35	–	40	–	50	ns	6
$\overline{CAS}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	0	–	0	–	0	–	ns	6
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	20	0	20	0	20	ns	10
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{REHREL}	t_{RP}	50	–	60	–	70	–	ns	
$\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ Hold Time	t_{CELREH}	t_{RSH}	20	–	20	–	25	–	ns	
$\overline{CAS}$ Hold Time	t_{RELCEH}	t_{CSH}	70	–	80	–	100	–	ns	
$\overline{CAS}$ Pulse Width	t_{CELCEH}	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RELCEL}	t_{RCD}	20	50	20	60	25	75	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	35	15	40	20	50	ns	12
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	–	5	–	10	–	ns	
$\overline{CAS}$ Precharge Time	t_{CEHCEL}	t_{CPN}	10	–	10	–	15	–	ns	
$\overline{CAS}$ Precharge Time (Page Mode Cycle Only)	t_{CEHCEL}	t_{CP}	10	–	10	–	10	–	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	–	0	–	0	–	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	–	10	–	15	–	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	–	0	–	0	–	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	–	15	–	20	–	ns	
Column Address Hold Time Referenced to $\overline{RAS}$	t_{RELAX}	t_{AR}	55	–	60	–	75	–	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{AVREH}	t_{RAL}	35	–	40	–	50	–	ns	

(continued)

NOTES:

1. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specifications for t_{RC} (min) and t_{RMW} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
6. Measured with a current load equivalent to 2 TTL (−200 µA, +4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
8. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
9. Assumes that $t_{RAD} \geq t_{RAD}$ (max).
10. t_{OFF} (max) and/or t_{GZ} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
12. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.

2

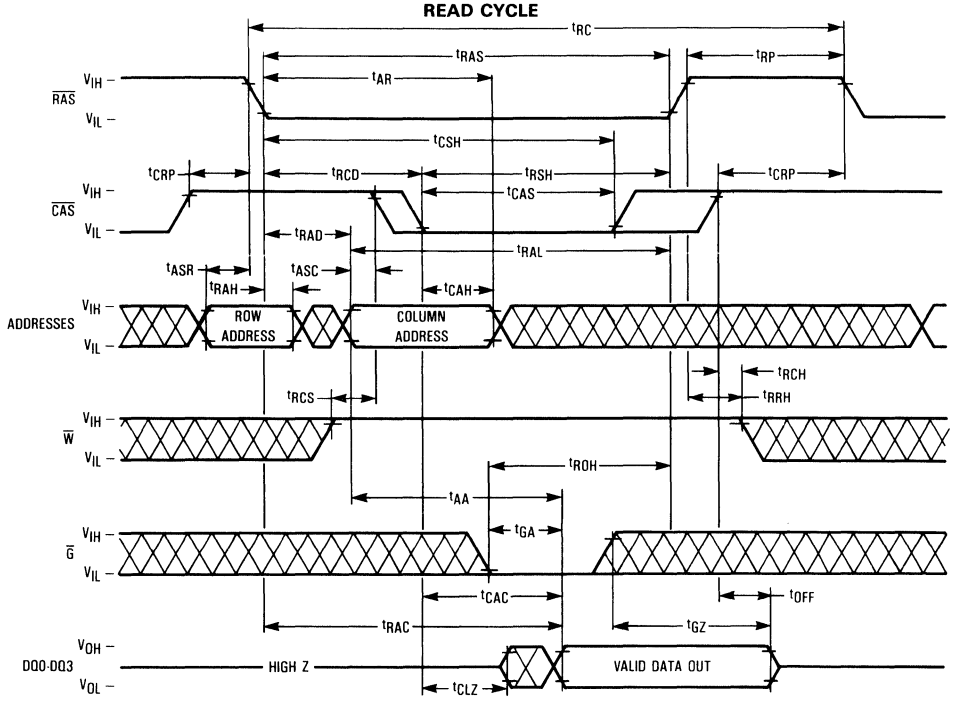
READ, WRITE, AND READ-WRITE CYCLES (Continued)

Parameter	Symbol		MCM514256A-70 MCM51L4256A-70		MCM514256A-80 MCM51L4256A-80		MCM514256A-10 MCM51L4256A-10		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	–	0	–	0	–	ns	
Read Command Hold Time	t_{CEHWX}	t_{RCH}	0	–	0	–	0	–	ns	13
Read Command Hold Time Referenced to $\overline{RAS}$	t_{REHWX}	t_{RRH}	0	–	0	–	0	–	ns	13
Write Command Hold Time Referenced to $\overline{CAS}$	t_{CELWH}	t_{WCH}	15	–	15	–	20	–	ns	
Write Command Hold Time Referenced to $\overline{RAS}$	t_{RELWH}	t_{WCR}	55	–	60	–	75	–	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	15	–	15	–	20	–	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{WLREH}	t_{RWL}	20	–	20	–	25	–	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{WLCEH}	t_{CWL}	20	–	20	–	25	–	ns	
Data In Setup Time	t_{DVCEL}	t_{DS}	0	–	0	–	0	–	ns	14
Data In Hold Time	t_{CELDX}	t_{DH}	15	–	15	–	20	–	ns	14
Data In Hold Time Referenced to $\overline{RAS}$	t_{RELDX}	t_{DHR}	55	–	60	–	75	–	ns	
Refresh Period MCM514256A MCM51L4256A	t_{RVRV}	t_{RFSH}	– –	8 64	– –	8 64	– –	8 64	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	–	0	–	0	–	ns	15
$\overline{CAS}$ to Write Delay	t_{CELWL}	t_{CWD}	50	–	50	–	60	–	ns	15
$\overline{RAS}$ to Write Delay	t_{RELWL}	t_{RWD}	100	–	110	–	135	–	ns	15
Column Address to Write Delay Time	t_{AVWL}	t_{AWD}	65	–	70	–	85	–	ns	15
$\overline{CAS}$ Setup Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEL}	t_{CSR}	10	–	10	–	10	–	ns	
$\overline{CAS}$ Hold Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEH}	t_{CHR}	30	–	30	–	30	–	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	t_{REHCEL}	t_{RPC}	0	–	0	–	0	–	ns	
$\overline{CAS}$ Precharge Time for $\overline{CAS}$ Before $\overline{RAS}$ Counter Test	t_{CEHCEL}	t_{CPT}	40	–	40	–	50	–	ns	
$\overline{RAS}$ Hold Time Referenced to $\overline{G}$	t_{GLREH}	t_{ROH}	10	–	10	–	20	–	ns	
$\overline{G}$ Access Time	t_{GLQV}	t_{GA}	–	20	–	20	–	25	ns	
$\overline{G}$ to Data Delay	t_{GLHDX}	t_{GD}	20	–	20	–	25	–	ns	
Output Buffer Turn-Off Delay Time from $\overline{G}$	t_{GHQZ}	t_{GZ}	0	20	0	20	0	25	ns	10
$\overline{G}$ Command Hold Time	t_{WLGL}	t_{GH}	20	–	20	–	25	–	ns	

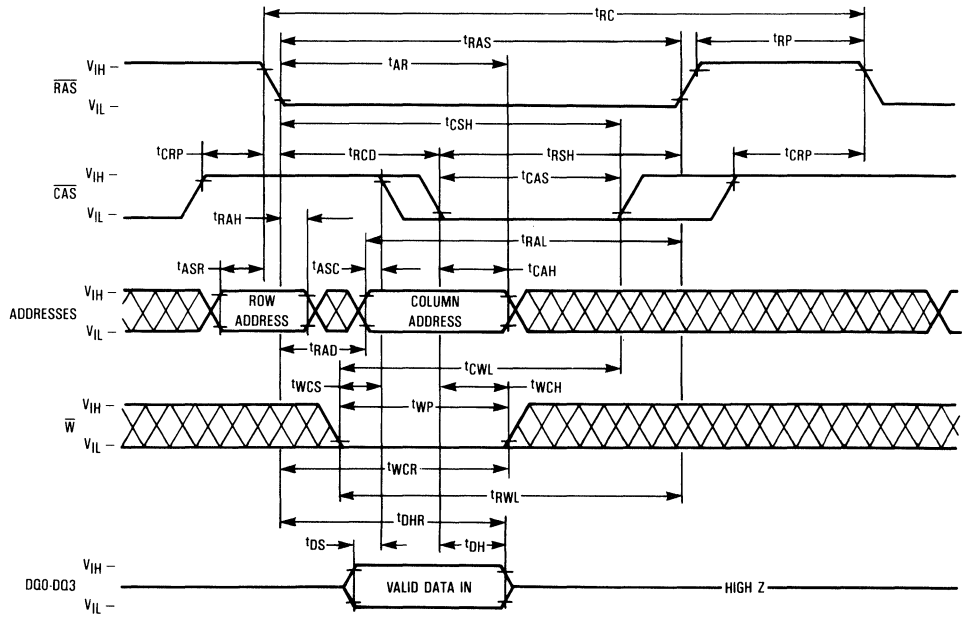
NOTES:

13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{W}$ leading edge in delayed write or read-write cycles.
15. t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

READ CYCLE



EARLY WRITE CYCLE



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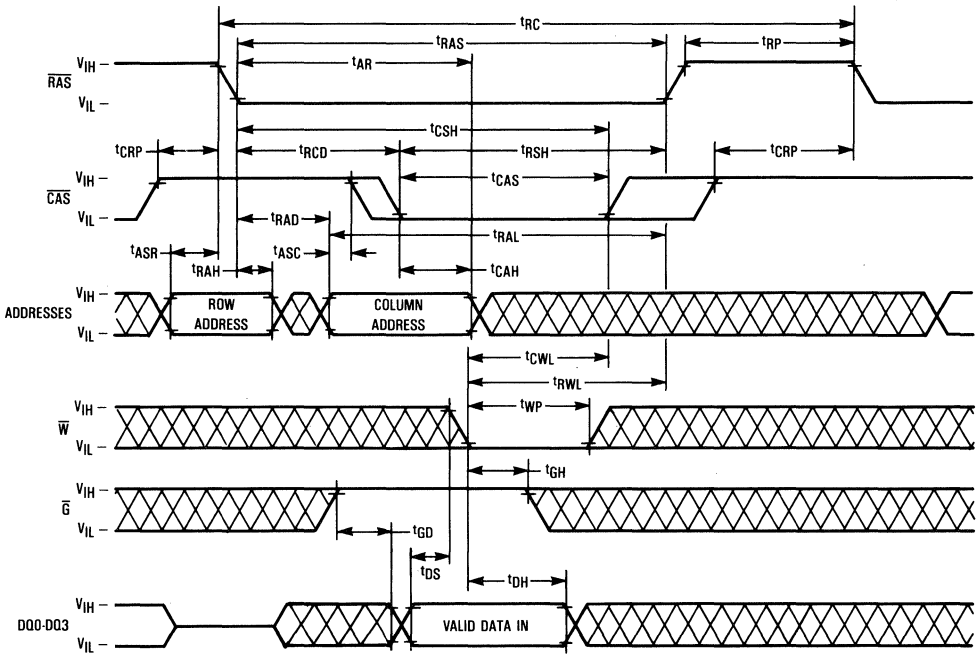
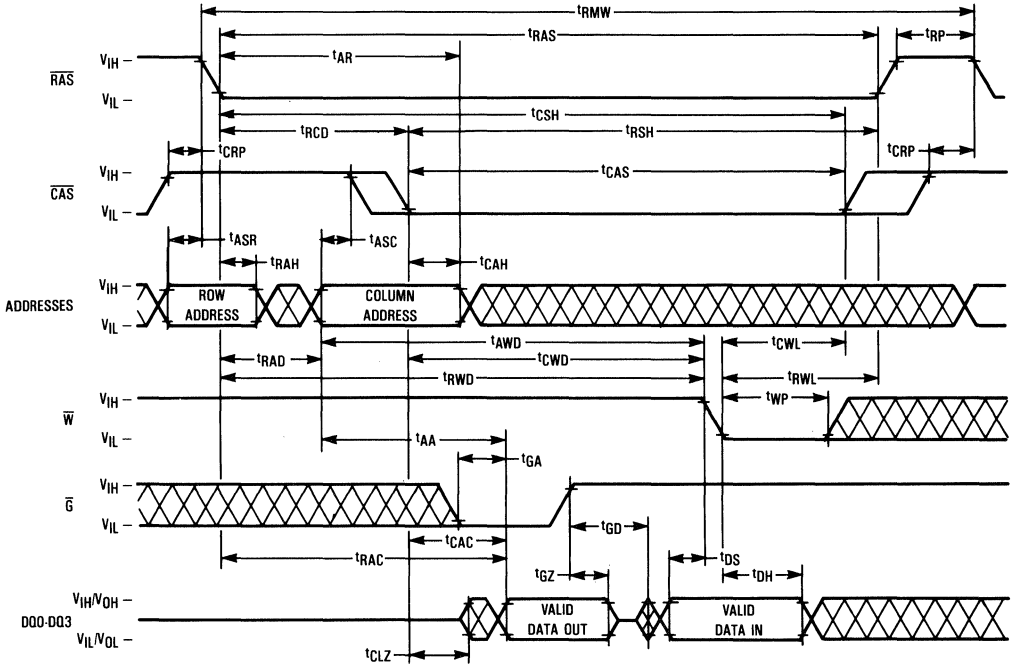
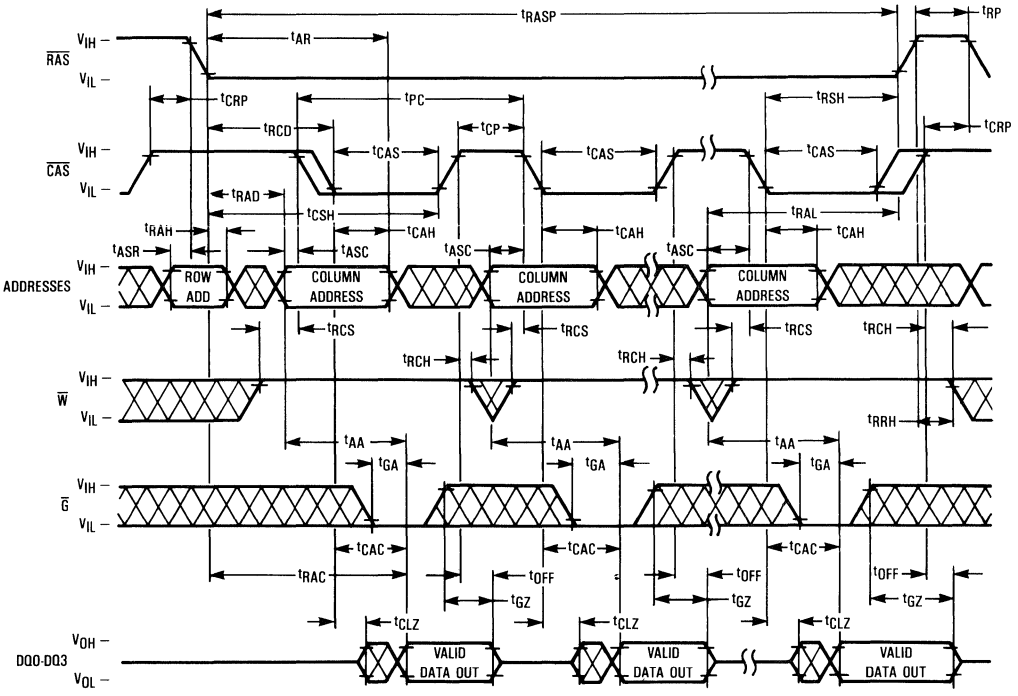
$\overline{G}$ CONTROLLED LATE WRITE CYCLE



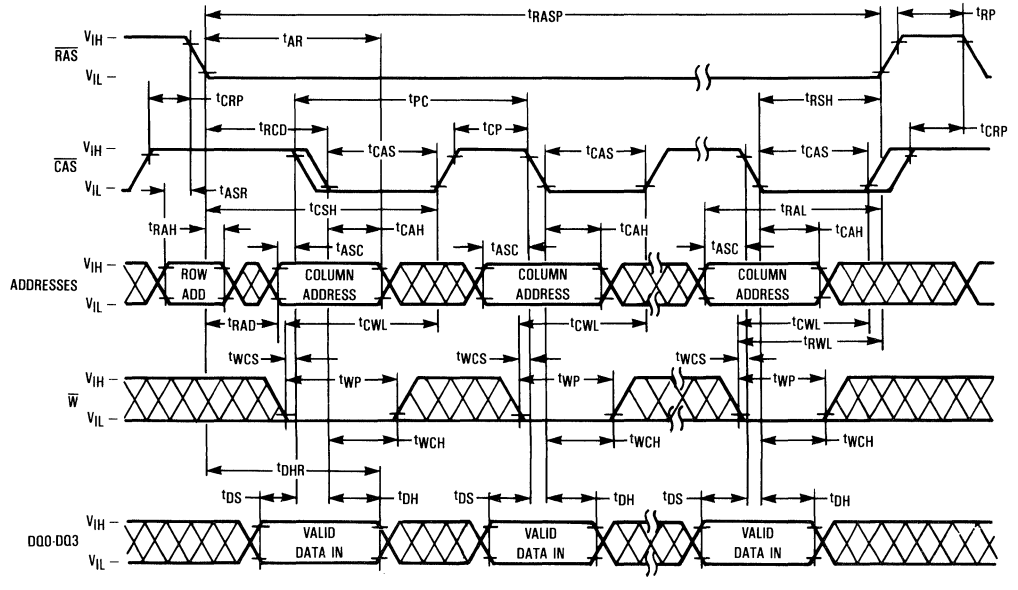
READ-WRITE CYCLE



FAST PAGE MODE READ CYCLE



FAST PAGE MODE EARLY WRITE CYCLE



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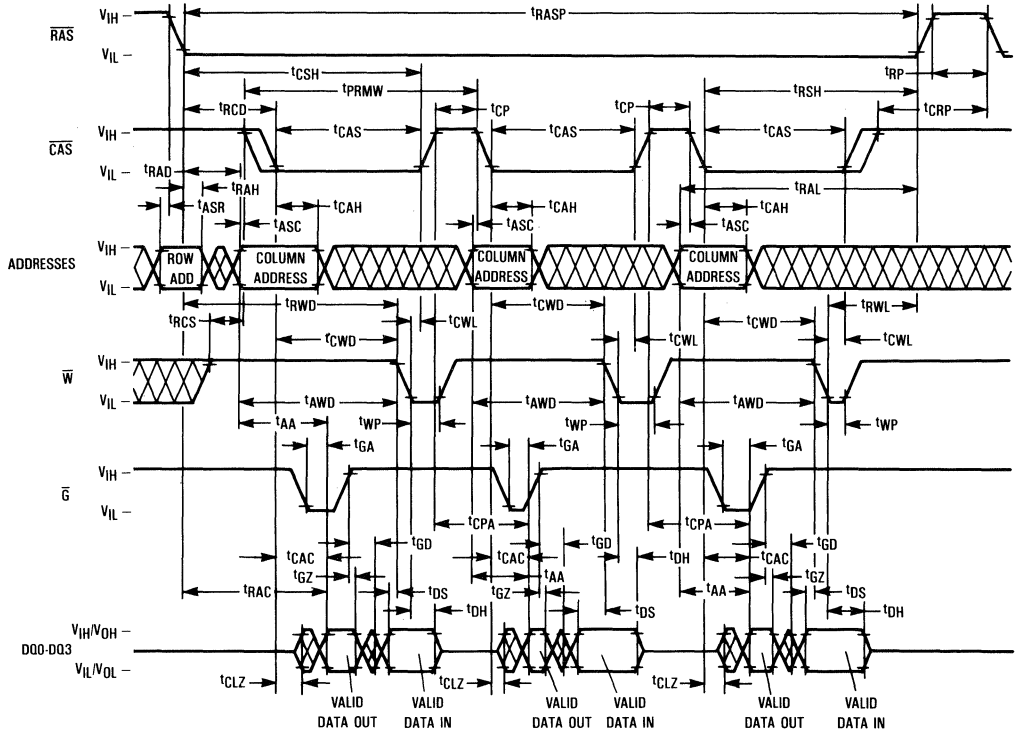
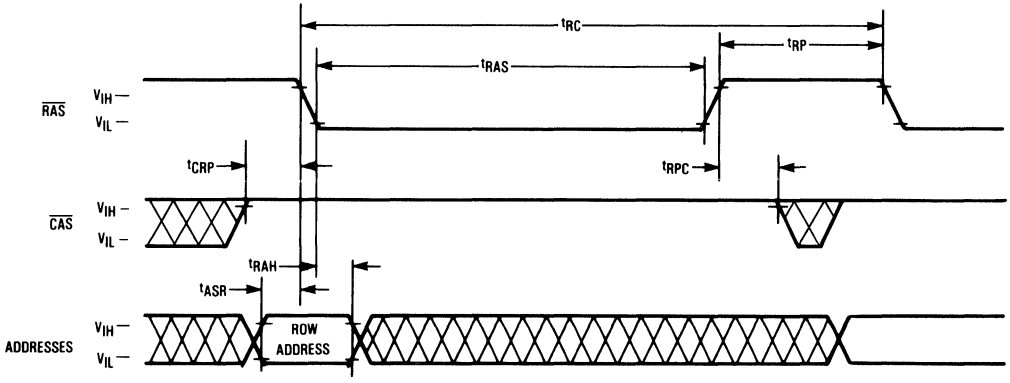
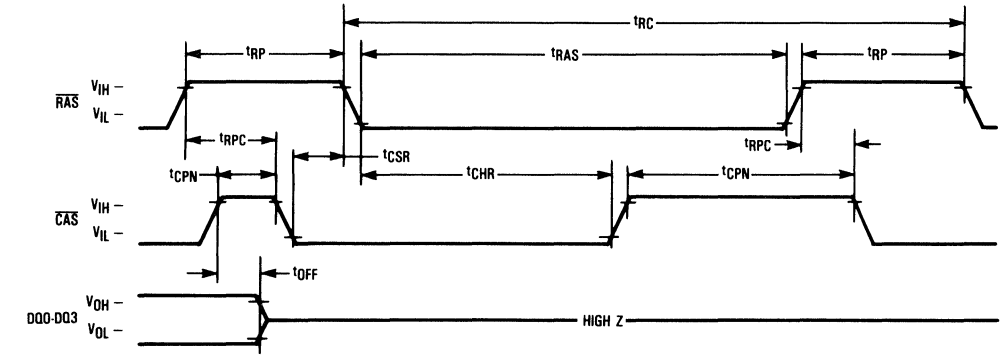
FAST PAGE MODE READ-WRITE CYCLE



$\overline{RAS}$ ONLY REFRESH CYCLE
($\overline{W}$ and $\overline{G}$ are Don't Care)



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE
($\overline{W}$, $\overline{G}$, and A0-A8 are Don't Care)



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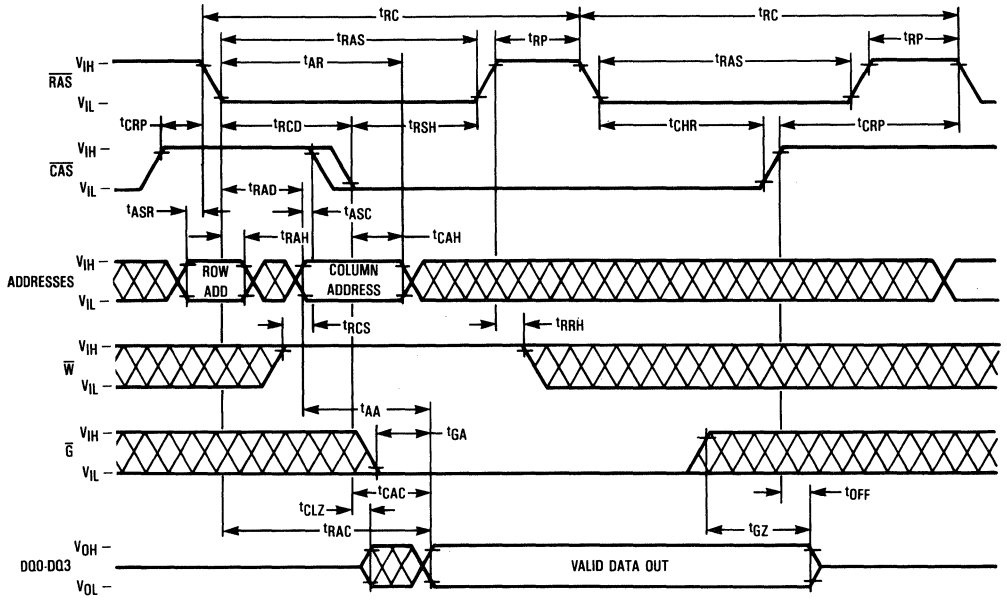
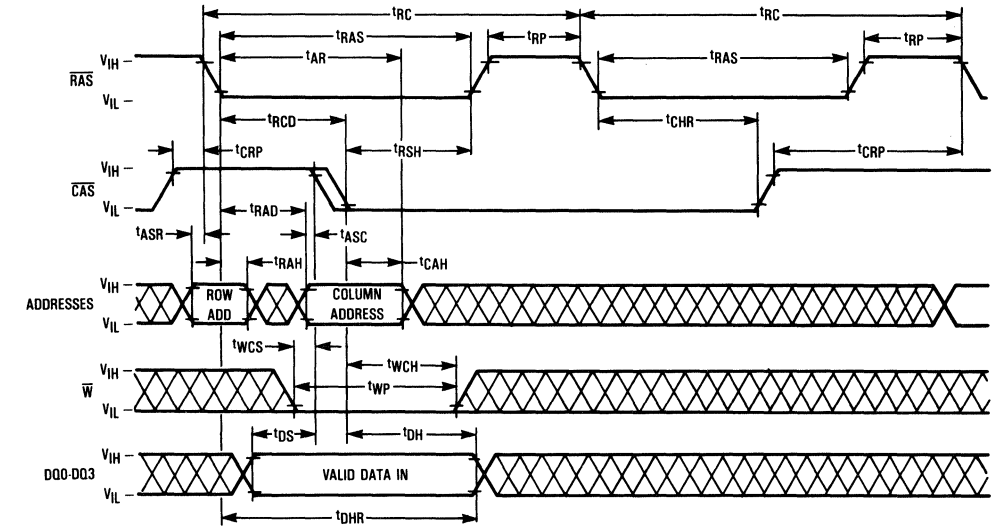
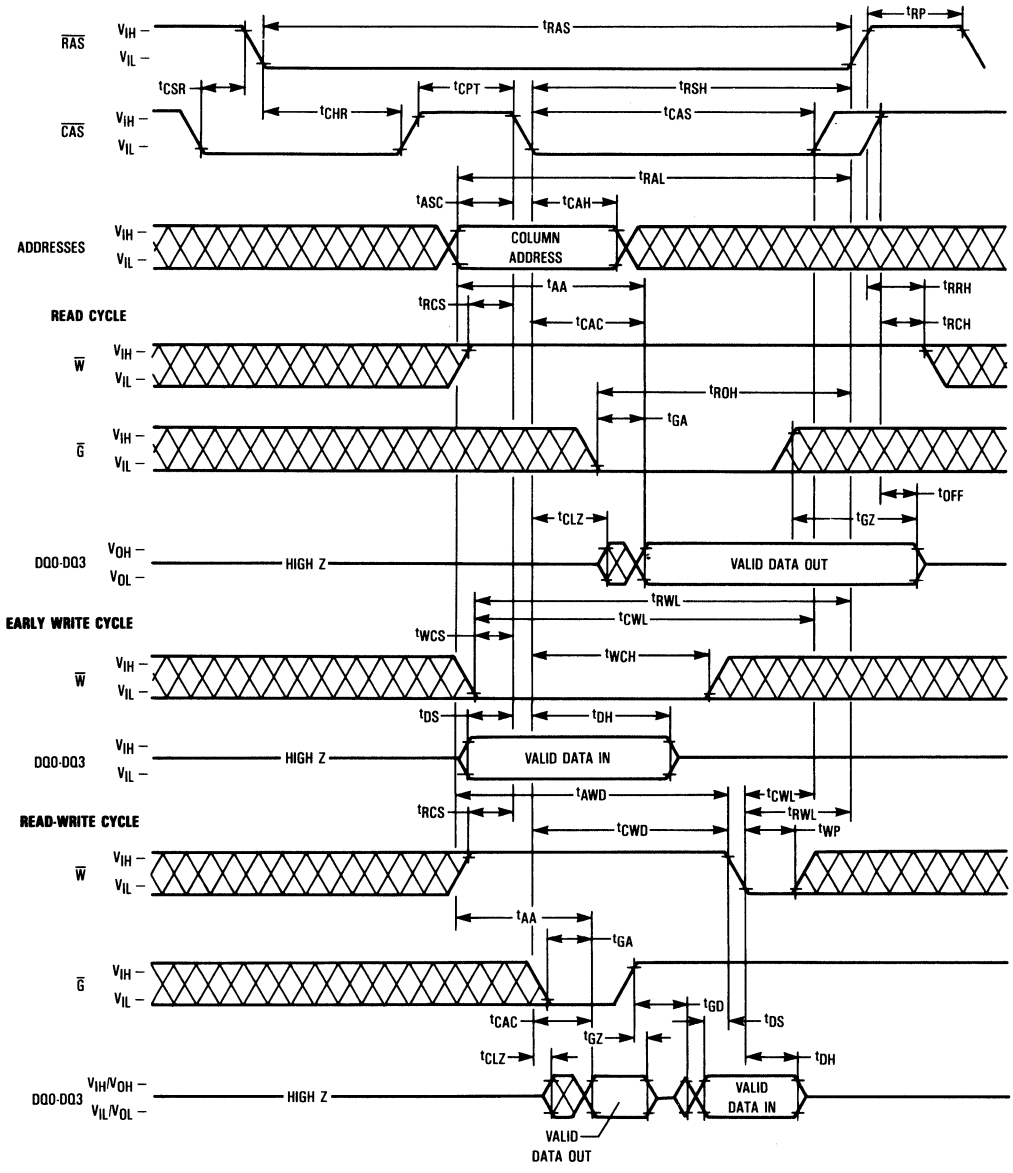
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (EARLY WRITE)



CAS BEFORE RAS REFRESH COUNTER TEST CYCLE



2

DEVICE INITIALIZATION

On power-up an initial pause of 200 microseconds is required for the internal substrate generator to establish the correct bias voltage. This is to be followed by a minimum of eight active cycles of the row address strobe ($\overline{RAS}$) to initialize all dynamic nodes within the RAM. During an extended inactive state (greater than 8 milliseconds with the device powered up), a wake up sequence of eight active cycles is necessary to assure proper operation.

ADDRESSING THE RAM

The nine address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks, row address strobe ($\overline{RAS}$) and column address strobe ($\overline{CAS}$), into two separate 9-bit address fields. A total of eighteen address bits, nine rows and nine columns, will decode one of the 262,144 bit locations in the device. $\overline{RAS}$ active transition is followed by $\overline{CAS}$ active transition (active = V_{IL}, t_{RCD} minimum) for all read or write cycles. The delay between $\overline{RAS}$ and $\overline{CAS}$ active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

The external $\overline{CAS}$ signal is ignored until an internal $\overline{RAS}$ signal is available. This gate feature on the external $\overline{CAS}$ clock enables the internal $\overline{CAS}$ line as soon as the row address hold time (t_{RAH}) specification is met (and defines t_{RCD} minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{CAS}$ clock.

There are two other variations in addressing the 256K × 4 RAM: **$\overline{RAS}$ only refresh cycle** and **$\overline{CAS}$ before $\overline{RAS}$ refresh cycle**. Both are discussed in separate sections that follow.

READ CYCLE

The DRAM may be read with four different cycles: normal random read cycle, page mode read cycle, read-write cycle, and page mode read-write cycle. The normal read cycle is outlined here, while the other cycles are discussed in separate sections.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with $\overline{RAS}$ and $\overline{CAS}$ active transitions latching the desired bit location. The write ($\overline{W}$) input level must be high (V_{IH}), t_{RCS} (minimum) before the $\overline{CAS}$ active transition, to enable read mode.

Both the $\overline{RAS}$ and $\overline{CAS}$ clocks trigger a sequence of events which are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window. Both $\overline{CAS}$ and output enable ($\overline{G}$) control read access time: $\overline{CAS}$ must be active before or at t_{RCD} maximum and $\overline{G}$ must be active t_{RAC}-t_{GA} (both minimum) after $\overline{RAS}$ active transition to guarantee valid data out (Q) at t_{RAC} (access time from $\overline{RAS}$ active transition). If the t_{RCD} maximum is exceeded and/or $\overline{G}$ active transition does not occur in time, read access time is determined by either the $\overline{CAS}$ or $\overline{G}$ clock active transition (t_{CAC} or t_{GA}).

The $\overline{RAS}$ and $\overline{CAS}$ clocks must remain active for a minimum time of t_{RAS} and t_{CAS}, respectively, to complete the read cycle. $\overline{W}$ must remain high throughout the cycle, and for time t_{RRH} or t_{RCH} after $\overline{RAS}$ or $\overline{CAS}$ inactive transition, respectively, to maintain the data at that bit location. Once $\overline{RAS}$ transitions to inactive, it must remain inactive for a minimum time of t_{RP} to precharge the internal device circuitry for the next active cycle. Q is valid, but not latched, as long as the $\overline{CAS}$ and $\overline{G}$ clocks are active. When either the $\overline{CAS}$ or $\overline{G}$ clock transitions to inactive, the output will switch to High Z, t_{OFF} or t_{GZ} after inactive transition.

WRITE CYCLE

The DRAM may be written with any of four cycles: early write, late write, page mode early write, and page mode read-write. Early and late write modes are discussed here, while page mode write operations are covered in another section.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of $\overline{W}$ to active (V_{IL}). Early and late write modes are distinguished by the active transition of $\overline{W}$, with respect to $\overline{CAS}$. Minimum active time t_{RAS} and t_{CAS}, and precharge time t_{RP} apply to write mode, as in the read mode.

An early write cycle is characterized by $\overline{W}$ active transition at minimum time t_{WCS} before $\overline{CAS}$ active transition. Data In (D) is referenced to $\overline{CAS}$ in an early write cycle. $\overline{RAS}$ and $\overline{CAS}$ clocks must stay active for t_{RWL} and t_{CWL}, respectively, after the start of the early write operation to complete the cycle.

Q remains High Z throughout an early write cycle because $\overline{W}$ active transition precedes or coincides with $\overline{CAS}$ active transition, keeping data out buffers disabled, effectively disabling $\overline{G}$.

A late write cycle (referred to as $\overline{G}$ controlled write) occurs when $\overline{W}$ active transition is made after $\overline{CAS}$ active transition. $\overline{W}$ active transition could be delayed for almost 10 microseconds after $\overline{CAS}$ active transition, ($t_{RCD} + t_{CWD} + t_{RWL} + t_T$) ≤ t_{RAS}, if timing minimums t_{RCD}, t_{RWL}, and t_T are maintained. D is referenced to $\overline{W}$ active transition in a late write cycle. Output buffers are enabled by $\overline{CAS}$ active transition but Q may be indeterminate—see note 15 of AC operating conditions table. Parameters t_{RWL} and t_{CWL} also apply to late write cycles.

READ-WRITE CYCLE

A read-write cycle performs a read and then a write at the same address, during the same cycle. This cycle is basically a late write cycle, as discussed in the **WRITE CYCLE** section, except $\overline{W}$ must remain high for t_{CWD} minimum after the $\overline{CAS}$ active transition, to guarantee valid Q before writing the bit.

PAGE MODE CYCLES

Page mode allows fast successive data operations at all 512 column locations on a selected row of the 256K × 4 dynamic RAM. Read access time in page mode (t_{CAC}) is typically half the regular $\overline{RAS}$ clock access time, t_{RAC}. Page mode operation consists of keeping $\overline{RAS}$ active while toggling $\overline{CAS}$ between V_{IH} and V_{IL}. The row is latched by $\overline{RAS}$ active transition, while each $\overline{CAS}$ active transition allows selection of a new column location on the row.

A page mode cycle is initiated by a normal read, write, or read-write cycle, as described in prior sections. Once the timing requirements for the first cycle are met, $\overline{CAS}$ transitions to inactive for minimum t_{CP}, while $\overline{RAS}$ remains low (V_{IL}). The second $\overline{CAS}$ active transition while $\overline{RAS}$ is low initiates the first page mode cycle (t_{PC} or t_{PRWC}). Either a read, write,

or read-write operation can be performed in a page mode cycle, subject to the same conditions as in normal operation (previously described). These operations can be intermixed in consecutive page mode cycles and performed in any order. The maximum number of consecutive page mode cycles is limited by t_{RASP}. Page mode operation is ended when $\overline{RAS}$ transitions to inactive, coincident with or following $\overline{CAS}$ inactive transition.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge degrades with time and temperature, thus each bit must be periodically refreshed (recharged) to maintain the correct bit state. Bits in the MCM514256A require refresh every 8 milliseconds, while refresh time for the MCM51L4256A is 64 milliseconds.

Refresh is accomplished by cycling through the 512 row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds for the MCM514256A, and 124.8 microseconds for the MCM51L4256A. Burst refresh, a refresh of all 512 rows consecutively, must be performed every 8 milliseconds on the MCM514256A and 64 milliseconds on the MCM51L4256A.

A normal read, write, or read-write operation to the RAM will refresh all the bits (2048) associated with the particular row decoded. Three other methods of refresh, **$\overline{RAS}$ only refresh**, **$\overline{CAS}$ before $\overline{RAS}$ refresh**, and **Hidden refresh** are available on this device for greater system flexibility.

$\overline{RAS}$-Only Refresh

$\overline{RAS}$-only refresh consists of $\overline{RAS}$ transition to active, latching the row address to be refreshed, while $\overline{CAS}$ remains high (V_{IH}) throughout the cycle. An external counter is employed to ensure all rows are refreshed within the specified limit.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh

$\overline{CAS}$ before $\overline{RAS}$ refresh is enabled by bringing $\overline{CAS}$ active before $\overline{RAS}$. This clock order activates an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle. The output buffer remains at the same state it was in during the previous cycle (hidden refresh).

Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding $\overline{CAS}$ active at the end of a read or write cycle, while $\overline{RAS}$ cycles inactive for t_{RP} and back to active, starts the hidden refresh. This is essentially the execution of a $\overline{CAS}$ before $\overline{RAS}$ refresh from a cycle in progress (see Figure 1).

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST

The internal refresh counter of this device can be tested with a **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test**. This test is performed with a read-write operation. During the test, the internal refresh counter generates the row address, while the external address supplies the column address. The entire array is refreshed after 512 cycles, as indicated by the check data written in each row. See **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test cycle** timing diagram.

The test can be performed after a minimum of eight $\overline{CAS}$ before $\overline{RAS}$ initialization cycles. Test procedure:

1. Write "0"s into all memory cells with normal write mode.
2. Select a column address, read "0" out and write "1" into the cell by performing the **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test, read-write cycle**. Repeat this operation 512 times.
3. Read the "1"s which were written in step 2 in normal read mode.
4. Using the same starting column address as in step 2, read "1" out and write "0" into the cell by performing **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test, read-write cycle**. Repeat this operation 512 times.
5. Read "0"s which were written in step 4 in normal read mode.
6. Repeat steps 1 to 5 using complement data.

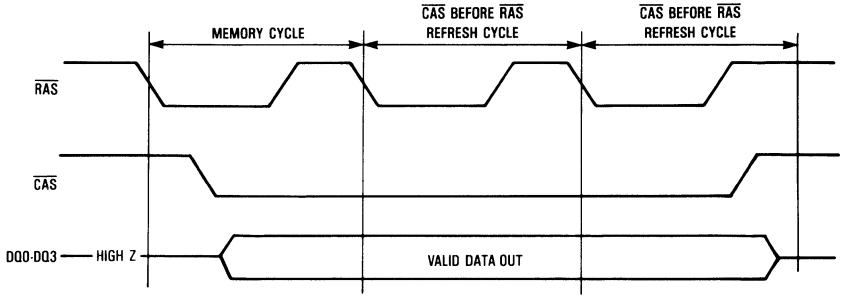
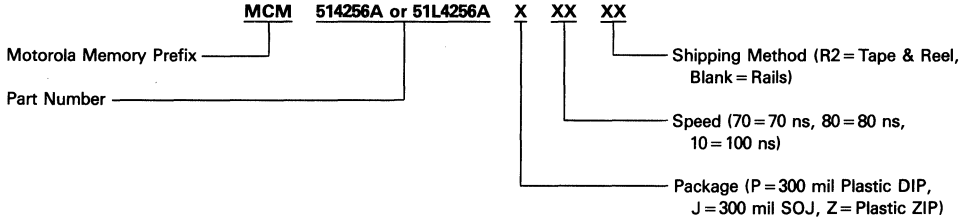


Figure 1. Hidden Refresh Cycle

2

ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers—	MCM514256AP70	MCM514256AJ70	MCM514256AJ70R2	MCM514256AZ70
	MCM514256AP80	MCM514256AJ80	MCM514256AJ80R2	MCM514256AZ80
	MCM514256AP10	MCM514256AJ10	MCM514256AJ10R2	MCM514256AZ10
	MCM51L4256AP70	MCM51L4256AJ70	MCM51L4256AJ70R2	MCM51L4256AZ70
	MCM51L4256AP80	MCM51L4256AJ80	MCM51L4256AJ80R2	MCM51L4256AZ80
	MCM51L4256AP10	MCM51L4256AJ10	MCM51L4256AJ10R2	MCM51L4256AZ10

MCM514258A

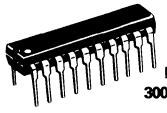
2

256K x 4 CMOS Dynamic RAM
Static Column

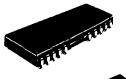
The MCM514258A is a 1.0μ CMOS high-speed, dynamic random access memory. It is organized as 262,144 four-bit words and fabricated with CMOS silicon-gate process technology. Advanced circuit design and fine line processing provide high performance, improved reliability, and low cost.

The MCM514258A requires only nine address lines; row and column address inputs are multiplexed. The device is packaged in a standard 300-mil dual-in-line plastic package (DIP), a 300-mil SOJ plastic package, and a 100-mil zig-zag in-line plastic package (ZIP).

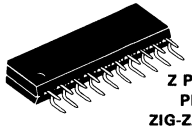
- Three-State Data Output
- Static Column Mode
- TTL-Compatible Inputs and Output
- $\overline{RAS}$ Only Refresh
- $\overline{CS}$ Before $\overline{RAS}$ Refresh
- Hidden Refresh
- 512 Cycle, 8 ms Refresh
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}):
  - MCM514258A-70 = 70 ns (Max)
  - MCM514258A-80 = 80 ns (Max)
  - MCM514258A-10 = 100 ns (Max)
- Low Active Power Dissipation:
  - MCM514258A-70 = 440 mW (Max)
  - MCM514258A-80 = 385 mW (Max)
  - MCM514258A-10 = 330 mW (Max)
- Low Standby Power Dissipation:
  - 11 mW (Max), TTL Levels
  - 5.5 mW (Max), CMOS Levels



P PACKAGE
300 MIL PLASTIC
CASE 738A



J PACKAGE
300 MIL SOJ
CASE 822

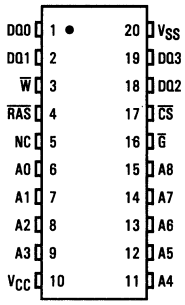


Z PACKAGE
PLASTIC
ZIG-ZAG IN-LINE
CASE 836

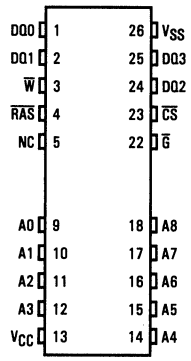
PIN NAMES	
A0-A8	Address Input
DQ0-DQ3	Data Input/Output
$\overline{G}$	Output Enable
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CS}$	Chip Select
V_{CC}	Power (+5 V)
V_{SS}	Ground
NC	No Connection

PIN ASSIGNMENT

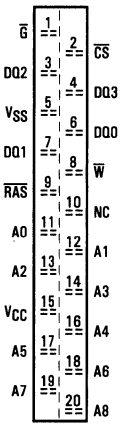
DUAL-IN-LINE



SMALL OUTLINE

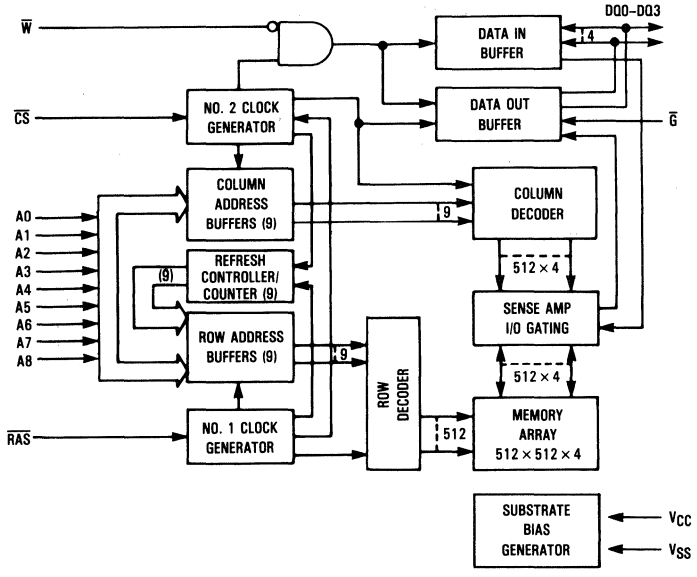


ZIG-ZAG IN-LINE



2

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−1 to +7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−1 to +7	V
Data Out Current	I_{out}	50	mA
Power Dissipation	P_D	600	mW
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V	1
	V_{SS}	0	0	0		
Logic High Voltage, All Inputs	V_{IH}	2.4	–	6.5	V	1
Logic Low Voltage, All Inputs	V_{IL}	−1.0	–	0.8	V	1

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current	I_{CC1}			mA	2
MCM514258A-70, t_{RC} = 130 ns		–	80		
MCM514258A-80, t_{RC} = 150 ns		–	70		
MCM514258A-10, t_{RC} = 180 ns		–	60		
V_{CC} Power Supply Current (Standby) ($\overline{RAS} = \overline{CS} = V_{IH}$)	I_{CC2}	–	2.0	mA	
V_{CC} Power Supply Current During $\overline{RAS}$ only Refresh Cycles ($\overline{CS} = V_{IH}$)	I_{CC3}			mA	2
MCM514258A-70, t_{RC} = 130 ns		–	80		
MCM514258A-80, t_{RC} = 150 ns		–	70		
MCM514258A-10, t_{RC} = 180 ns		–	60		
V_{CC} Power Supply Current During Static Column Mode Cycle ($\overline{RAS} = \overline{CS} = V_{IL}$)	I_{CC4}			mA	2, 4
MCM514258A-70, t_{SC} = 40 ns		–	60		
MCM514258A-80, t_{SC} = 45 ns		–	50		
MCM514258A-10, t_{SC} = 50 ns		–	40		
V_{CC} Power Supply Current (Standby) ($\overline{RAS} = \overline{CS} = V_{CC} - 0.2$ V)	I_{CC5}	–	1.0	mA	
V_{CC} Power Supply Current During $\overline{CS}$ Before $\overline{RAS}$ Refresh Cycle	I_{CC6}			mA	2
MCM514258A-70, t_{RC} = 130 ns		–	80		
MCM514258A-80, t_{RC} = 150 ns		–	70		
MCM514258A-10, t_{RC} = 180 ns		–	60		
Input Leakage Current (0 V ≤ V_{in} ≤ 6.5 V)	$I_{lkg(I)}$	−10	10	μA	
Output Leakage Current ($\overline{CS} = V_{IH}$, 0 V ≤ V_{out} ≤ 5.5 V)	$I_{lkg(O)}$	−10	10	μA	
Output High Voltage (I_{OH} = −5 mA)	V_{OH}	2.4	–	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	–	0.4	V	

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Max	Unit	Notes
Input Capacitance	A0–A8	C_{in}	5	pF	3
	$\overline{G}$, $\overline{RAS}$, $\overline{CS}$, $\overline{W}$		7	pF	3
Output Capacitance ($\overline{CS} = V_{IH}$ to Disable Output)	DQ0–DQ3	C_{out}	7	pF	3

NOTES:
1. All voltages referenced to V_{SS}.
2. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
3. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\Delta t / \Delta V$.
4. Measured with one address transition per static column mode cycle.

2

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ, WRITE, AND READ-WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM514258A-70		MCM514258A-80		MCM514258A-10		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	130	–	150	–	180	–	ns	5
Read-Write Cycle Time	t_{RELREL}	t_{RMW}	185	–	205	–	245	–	ns	5
Static Column Mode Cycle Time	t_{AVAV}	t_{SC}	40	–	45	–	55	–	ns	
Static Column Mode Read-Write Cycle Time	t_{AVAV}	t_{SRMW}	100	–	110	–	135	–	ns	
Access Time from $\overline{RAS}$	t_{RELQV}	t_{RAC}	–	70	–	80	–	100	ns	6, 7
Access Time from $\overline{CS}$	t_{CELQV}	t_{CAC}	–	25	–	25	–	30	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	–	35	–	40	–	50	ns	6, 9
Access Time from Last Write	t_{WLQV}	t_{ALW}	–	65	–	75	–	95	ns	6, 10
$\overline{CS}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	0	–	0	–	0	–	ns	6
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	20	0	20	0	30	ns	11
Output Data Hold Time from Column Address	t_{AXQX}	t_{AOH}	5	–	5	–	5	–	ns	
Output Data Enable Time from Write	t_{WHQV}	t_{OW}	–	20	–	20	–	30	ns	
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{REHREL}	t_{RP}	50	–	60	–	70	–	ns	
$\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ Pulse Width (Static Column Mode)	t_{RELREH}	t_{RASC}	70	100,000	80	100,000	100	100,000	ns	
$\overline{CS}$ to $\overline{RAS}$ Hold Time	t_{CELREH}	t_{RSH}	25	–	25	–	30	–	ns	
$\overline{RAS}$ to $\overline{CS}$ Hold Time	t_{RELCEH}	t_{CSH}	70	–	80	–	100	–	ns	
$\overline{CS}$ Pulse Width	t_{CELCEH}	t_{CS}	25	10,000	25	10,000	30	10,000	ns	
$\overline{CS}$ Pulse Width (Static Column Mode)	t_{CELCEH}	t_{CSC}	25	100,000	25	100,000	30	100,000	ns	
$\overline{RAS}$ to $\overline{CS}$ Delay Time	t_{RELCEL}	t_{RCD}	20	45	20	55	25	70	ns	12
$\overline{RAS}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	35	15	40	20	50	ns	13
$\overline{CS}$ to $\overline{RAS}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	–	5	–	5	–	ns	
$\overline{CS}$ Precharge Time	t_{CEHCEL}	t_{CPN}	10	–	10	–	15	–	ns	
$\overline{CS}$ Precharge Time (Static Column Mode)	t_{CEHCEL}	t_{CP}	10	–	10	–	10	–	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	–	0	–	0	–	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	–	10	–	15	–	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	–	0	–	0	–	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	–	15	–	20	–	ns	
Write Address Hold Time Referenced to $\overline{RAS}$	t_{RELAX}	t_{AWR}	55	–	60	–	75	–	ns	
Column Address Hold Time Referenced to $\overline{RAS}$	t_{RELAX}	t_{AR}	85	–	95	–	115	–	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{AVREH}	t_{RAL}	35	–	40	–	50	–	ns	

(continued)

NOTES:

1. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specifications for t_{RC} (min) and t_{RMW} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
6. Measured with a current load equivalent to 2 TTL (−200 μA, +4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
8. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
9. Assumes that $t_{RAD} \geq t_{RAD}$ (max).
10. Assumes that $t_{LWAD} \leq t_{LWAD}$ (max).
11. t_{OFF} (max) and/or t_{GZ} define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
12. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
13. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.

READ, WRITE, AND READ-WRITE CYCLES (Continued)

Parameter	Symbol		MCM514258A-70		MCM514258A-80		MCM514258A-10		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Column Address Hold Time Referenced to $\overline{RAS}$	t_{REHAX}	t_{AH}	10	–	10	–	10	–	ns	14
Last Write to Column Address Delay Time	t_{WLAV}	t_{LWAD}	20	30	20	35	25	45	ns	15
Last Write to Column Address Hold Time	t_{WLAX}	t_{AHLW}	65	–	75	–	95	–	ns	
Read Command Setup Time Referenced to $\overline{CS}$	t_{WHCEL}	t_{RCS}	0	–	0	–	0	–	ns	
Read Command Hold Time Referenced to $\overline{CS}$	t_{CEHWX}	t_{RCH}	0	–	0	–	0	–	ns	16
Read Command Hold Time Referenced to $\overline{RAS}$	t_{REHWX}	t_{RRH}	0	–	0	–	0	–	ns	16
Write Command Hold Time (Output Data Disable)	t_{CEHWH}	t_{WCH}	15	–	15	–	20	–	ns	17
Write Command Hold Time Referenced to $\overline{RAS}$	t_{RELWH}	t_{WCR}	55	–	60	–	75	–	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	15	–	15	–	20	–	ns	
Write Inactive Time	t_{WHWL}	t_{WI}	10	–	10	–	10	–	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{WLREH}	t_{RWL}	20	–	20	–	25	–	ns	
Write Command to $\overline{CS}$ Lead Time	t_{WLCEH}	t_{CWL}	20	–	20	–	25	–	ns	
Data In Setup Time	t_{DVCEL}	t_{DS}	0	–	0	–	0	–	ns	18
Data In Hold Time	t_{CELDX}	t_{DH}	15	–	15	–	20	–	ns	18
Data In Hold Time Referenced to $\overline{RAS}$	t_{RELDX}	t_{DHR}	55	–	60	–	75	–	ns	
Refresh Period	t_{RVRV}	t_{RFSH}	–	8	–	8	–	8	ms	
Write Command Setup Time (Output Data Disable)	t_{WLCEL}	t_{WCS}	0	–	0	–	0	–	ns	17
$\overline{CS}$ to Write Delay (RW Cycle)	t_{CELWL}	t_{CWD}	55	–	55	–	65	–	ns	17
$\overline{RAS}$ to Write Delay (RW Cycle)	t_{RELWL}	t_{RWD}	100	–	110	–	135	–	ns	17
Column Address to Write Delay Time	t_{AVWL}	t_{AWD}	65	–	70	–	85	–	ns	17
$\overline{CS}$ Setup Time for $\overline{CS}$ Before $\overline{RAS}$ Refresh	t_{CELREL}	t_{CSR}	10	–	10	–	10	–	ns	
$\overline{CS}$ Hold Time for $\overline{CS}$ Before $\overline{RAS}$ Refresh	t_{RELCEH}	t_{CHR}	30	–	30	–	30	–	ns	
$\overline{RAS}$ Precharge to $\overline{CS}$ Active Time	t_{REHCEL}	t_{RPC}	0	–	0	–	0	–	ns	
$\overline{CS}$ Precharge Time for $\overline{CS}$ Before $\overline{RAS}$ Counter Test	t_{CEHCEL}	t_{CPT}	40	–	40	–	50	–	ns	
$\overline{RAS}$ Hold Time Referenced to $\overline{G}$	t_{GLREH}	t_{ROH}	10	–	10	–	20	–	ns	
$\overline{G}$ Access Time	t_{GLQV}	t_{GA}	–	25	–	25	–	25	ns	
$\overline{G}$ to Data Delay	t_{GHDX}	t_{GD}	20	–	20	–	25	–	ns	
Output Buffer Turn-off Delay Time from $\overline{G}$	t_{GHQZ}	t_{GZ}	0	20	0	20	0	25	ns	11
$\overline{G}$ Command Hold Time	t_{WLGL}	t_{GH}	20	–	20	–	25	–	ns	

NOTES:

14. t_{AH} must be met for a read cycle.
15. Operation within the t_{LWAD} (max) limit ensures that t_{ALW} (max) can be met. t_{LWAD} (max) is specified as a reference point only; if t_{LWAD} is greater than the specified t_{LWAD} (max) limit, then access time is controlled exclusively by t_{AA}.
16. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
17. t_{WCH}, t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min) and $t_{WCH} \geq t_{WCH}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
18. These parameters are referenced to $\overline{CS}$ leading edge in random write cycles and to $\overline{W}$ leading edge in late write or read-write cycles.

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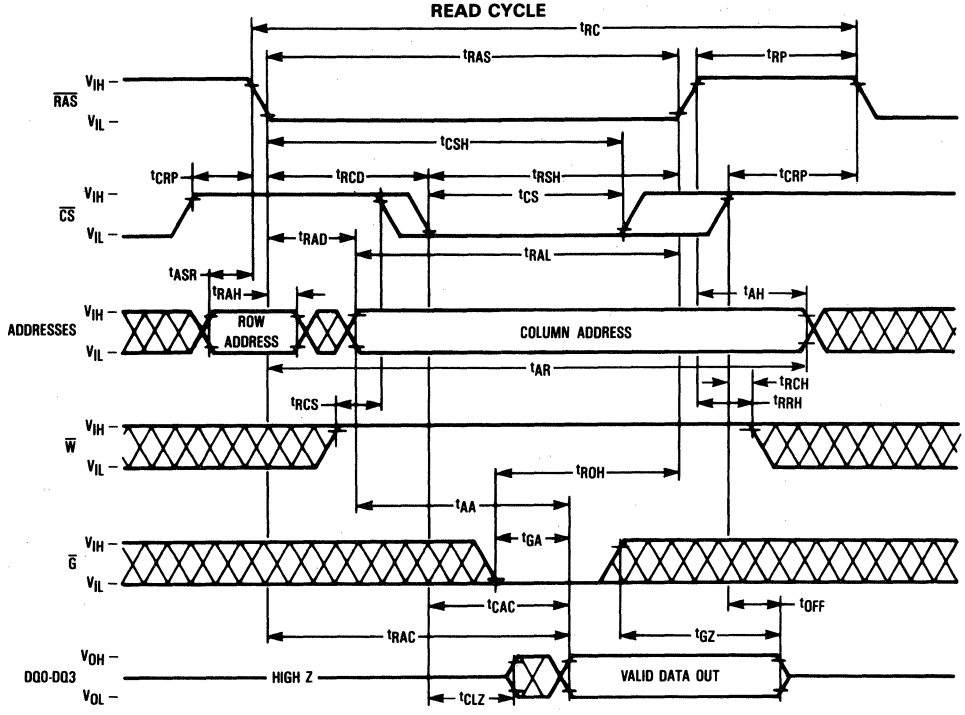
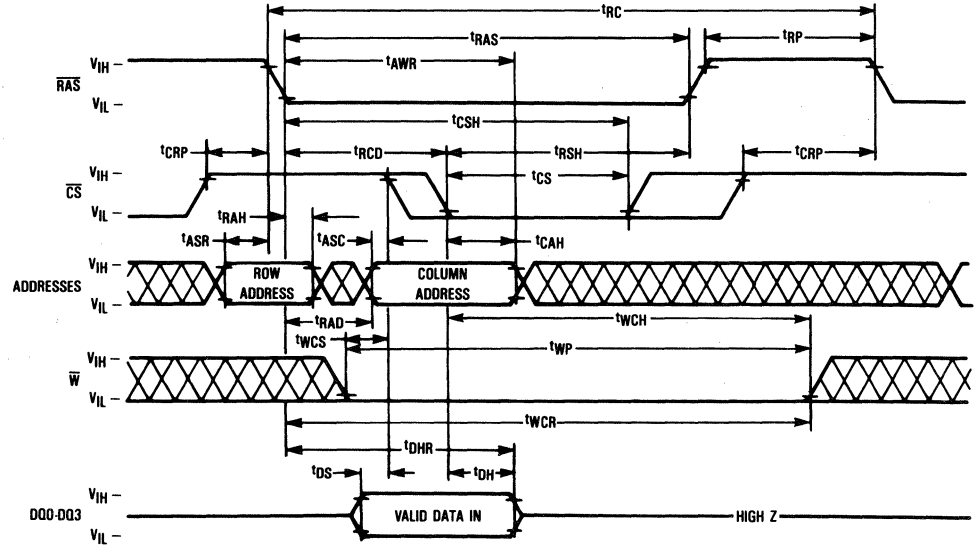
READ CYCLE

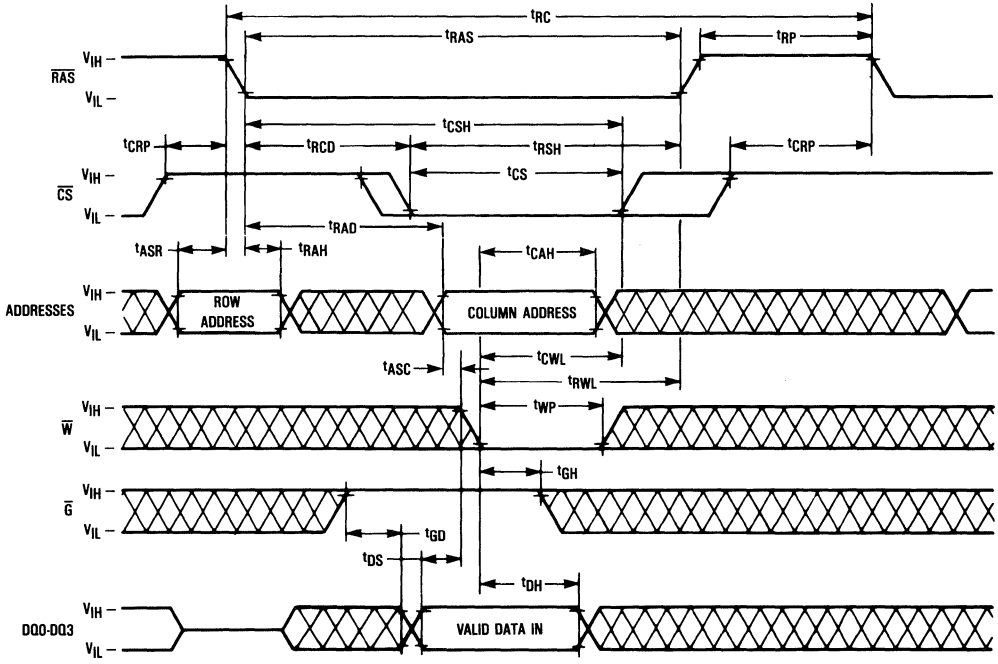


EARLY WRITE CYCLE

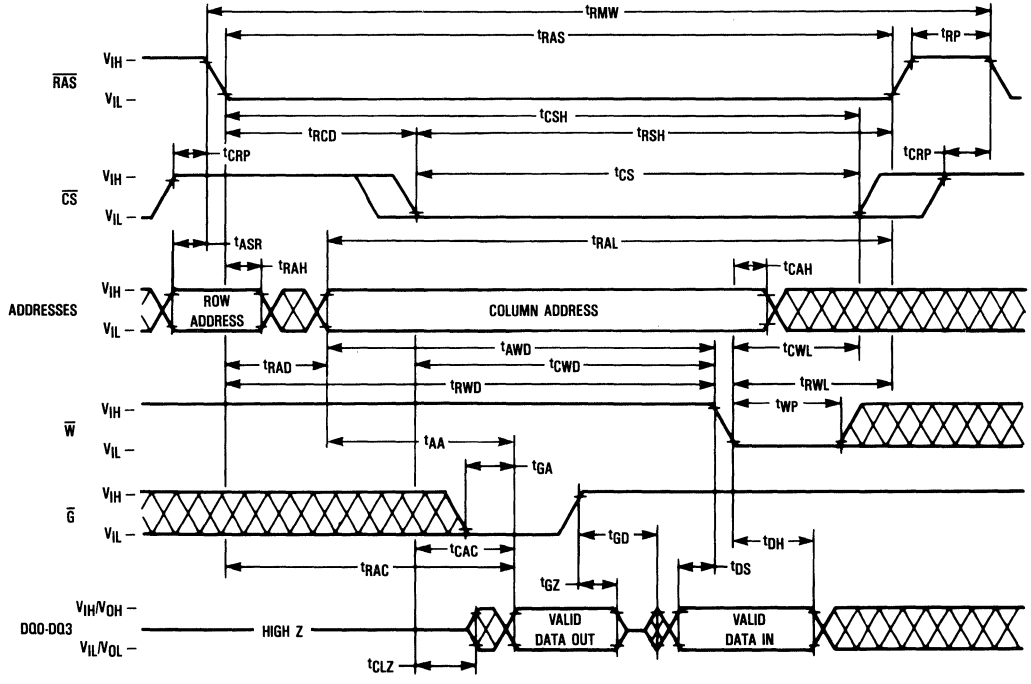
(G is Don't Care)



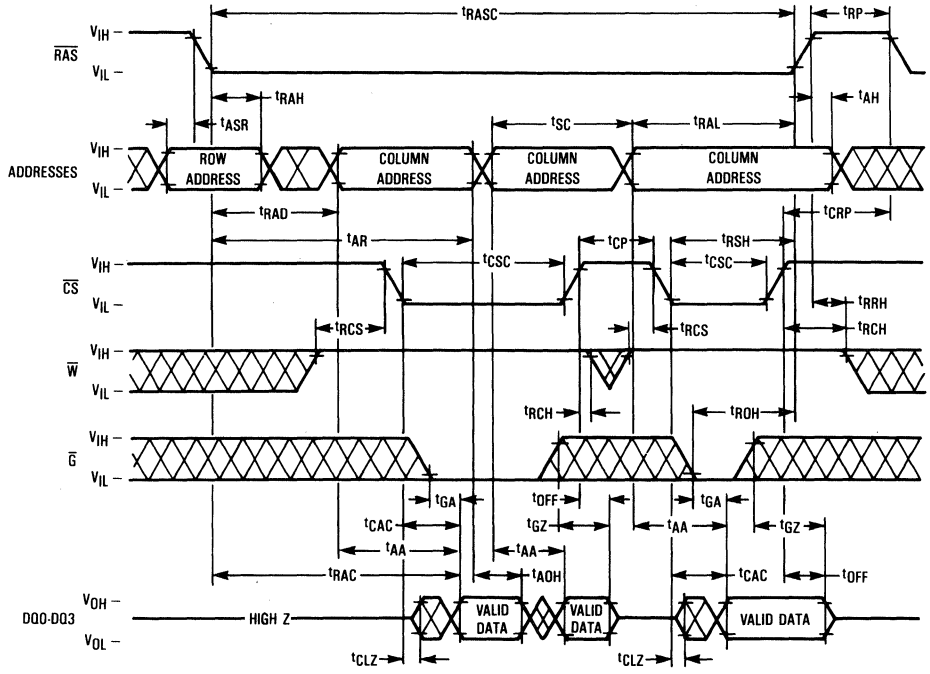
$\overline{G}$ CONTROLLED LATE WRITE CYCLE



READ-WRITE CYCLE

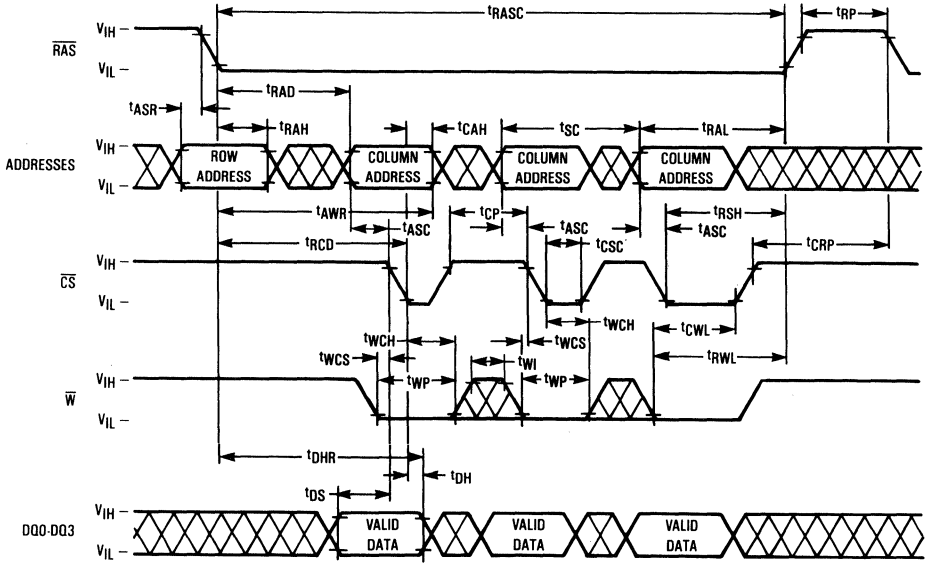


STATIC COLUMN MODE READ CYCLE



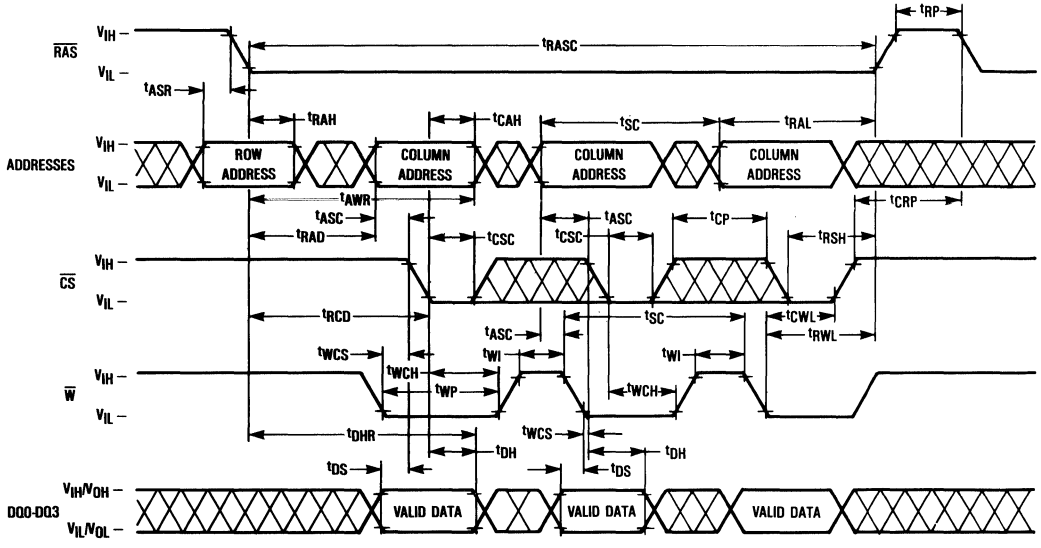
STATIC COLUMN MODE EARLY WRITE CYCLE (A)

($\overline{G}$ is Don't Care)

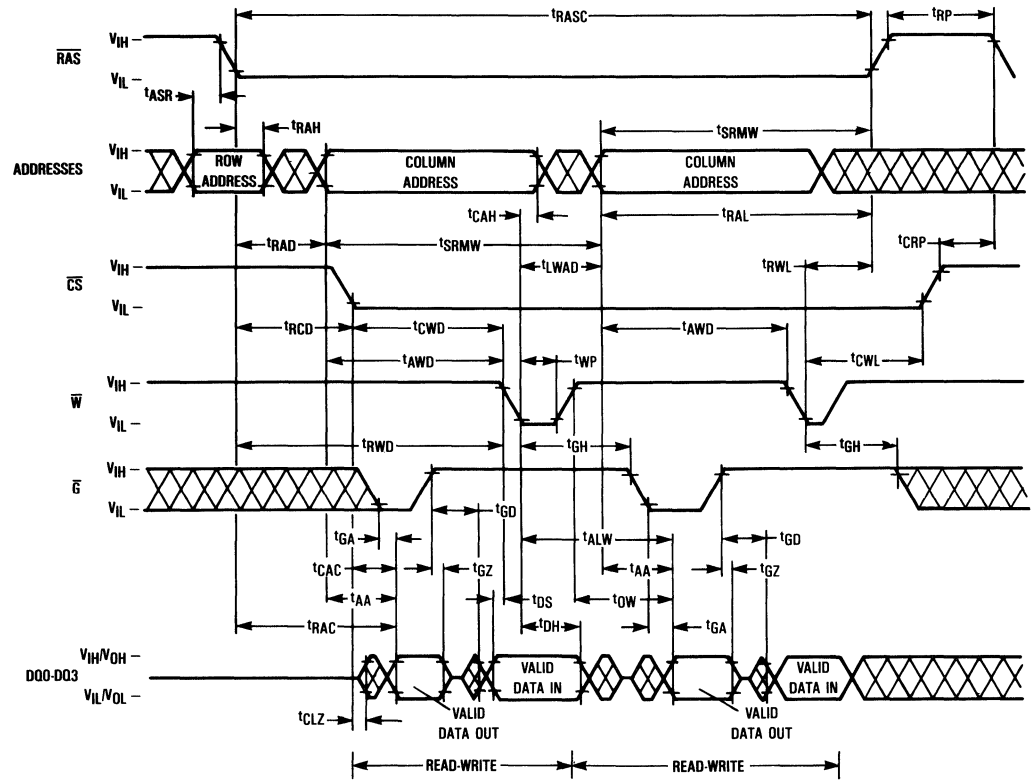


STATIC COLUMN MODE EARLY WRITE CYCLE (B)

(G is Don't Care)



STATIC COLUMN MODE READ-WRITE CYCLE



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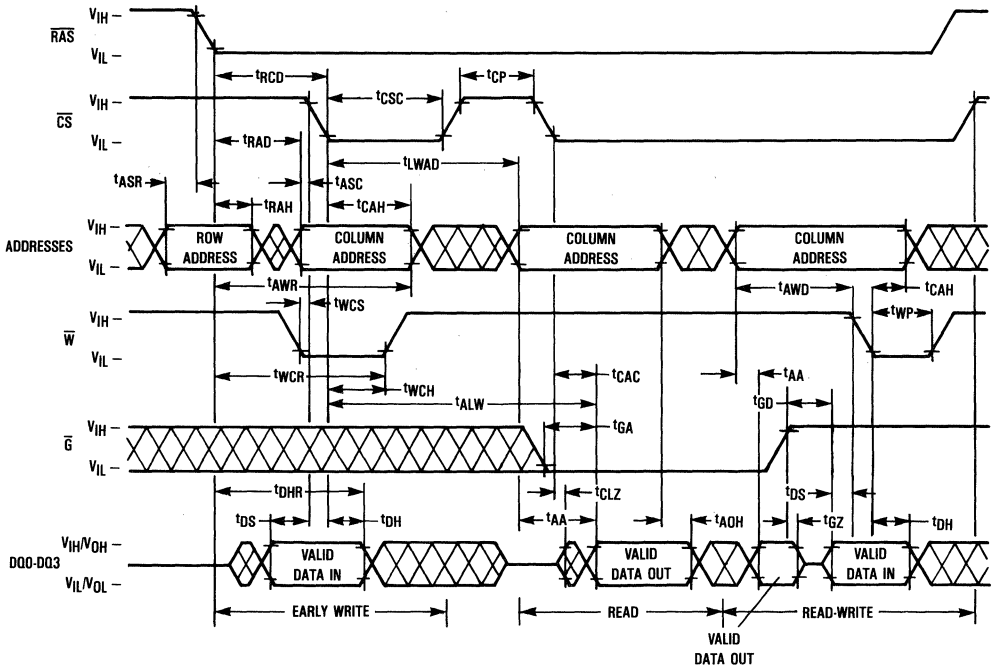
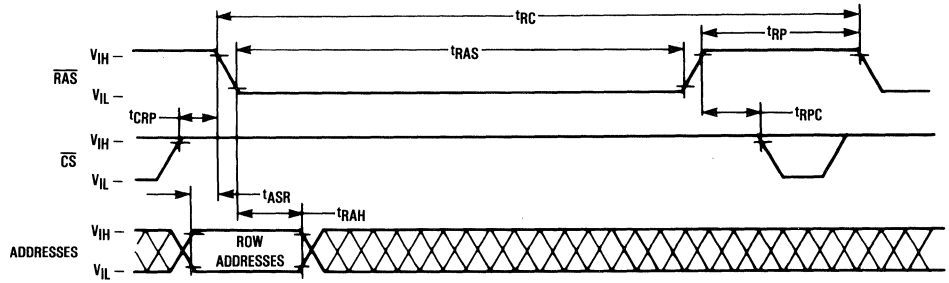
STATIC COLUMN MODE READ/WRITE MIXED CYCLE



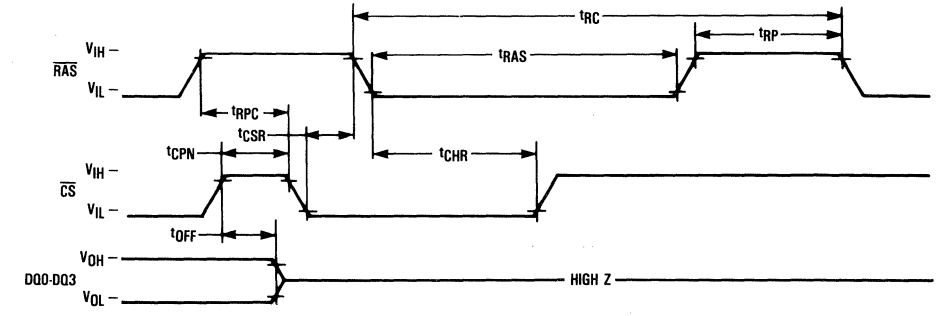
RAS ONLY REFRESH CYCLE

(W and G are Don't Care)

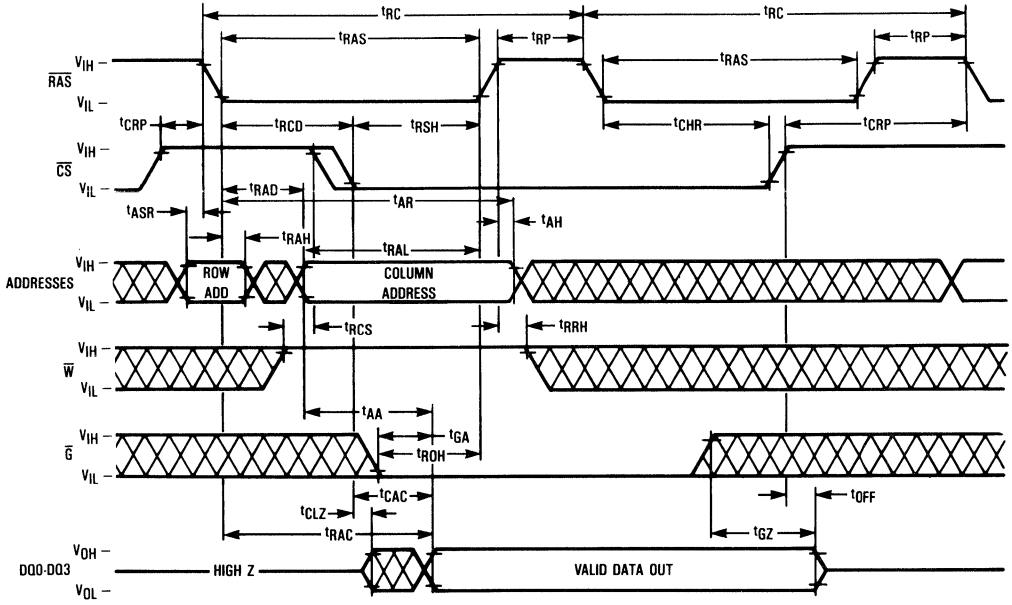


CS BEFORE RAS REFRESH CYCLE

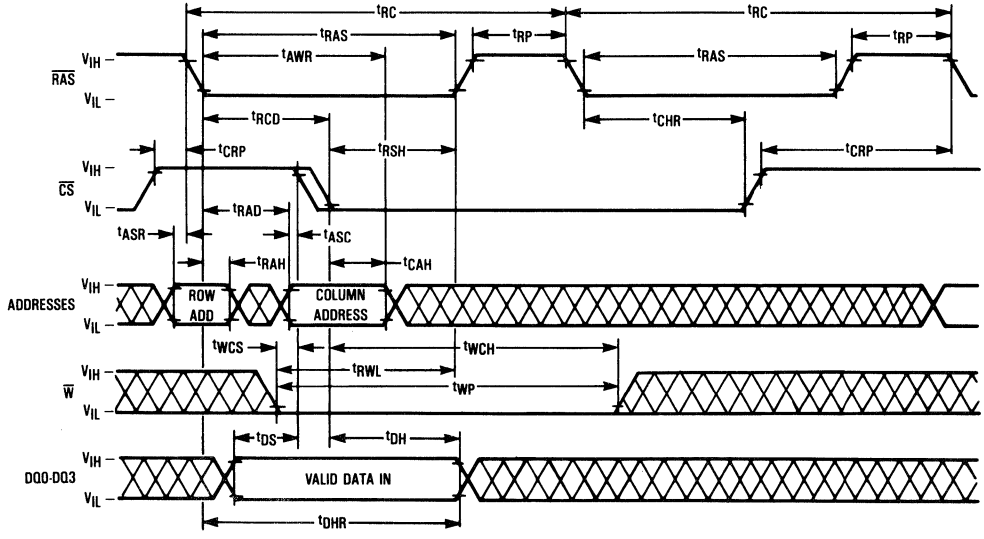
(W, G, and A0 to A8 are Don't Care)



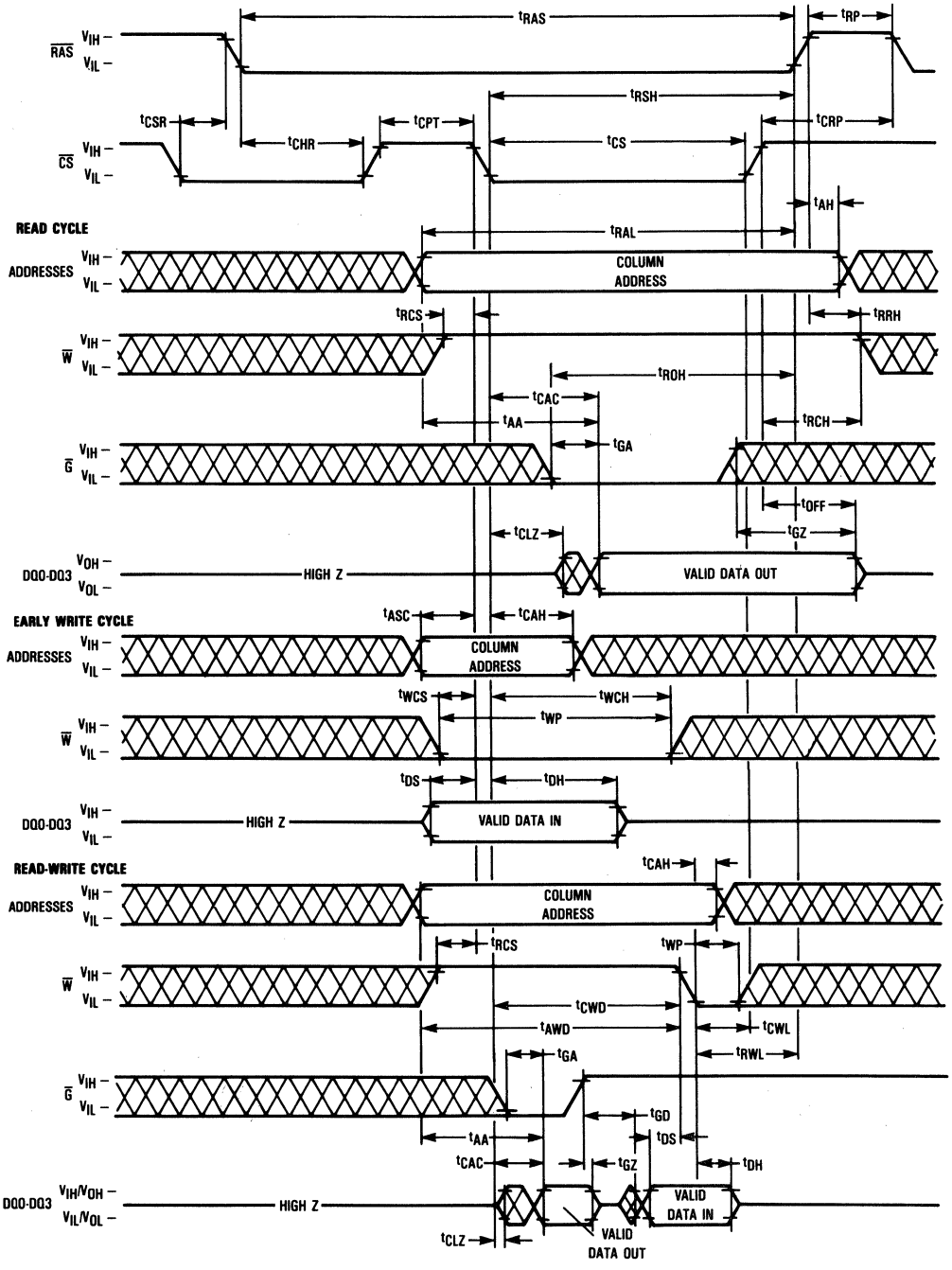
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (EARLY WRITE)
($\overline{G}$ is Don't Care)



$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



DEVICE INITIALIZATION

On power-up an initial pause of 200 microseconds is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize all dynamic nodes within the RAM. During an extended inactive state (greater than 8 milliseconds with the device powered up), a wake up sequence of eight active cycles is necessary to assure proper operation.

ADDRESSING THE RAM

The nine address pins on the device are time multiplexed at the beginning of a memory cycle by the row address strobe ($\overline{RAS}$) clock, into two separate 9-bit address fields. A total of eighteen address bits, nine rows and nine columns, will decode one of the 262,144 bit locations in the device. $\overline{RAS}$ active transition latches the row address field. Column addresses are not latched, hence the "static column" designation of this device. Chip select ($\overline{CS}$) active transition (active = V_{IL}, t_{RCD} minimum) follows $\overline{RAS}$ on all read, write, or read-write cycles, and is independent of column address. The static column feature allows greater flexibility in setting up the external external column addresses into the RAM.

There are two other variations in addressing the 256K × 4 RAM: **$\overline{RAS}$ only refresh cycle** and **$\overline{CS}$ before $\overline{RAS}$ refresh cycle**. Both are discussed in separate sections that follow.

READ CYCLE

The DRAM may be read with four different cycles: random read cycle, read-write cycle, and "static column mode" read, and read-write. The random read cycle is outlined here, while the other cycles are discussed in separate sections.

The random read cycle begins as described in **ADDRESSING THE RAM**, with $\overline{RAS}$ active transition latching the desired row. The write ($\overline{W}$) input level must be high (V_{IH}), t_{RCS} (minimum) before the $\overline{CS}$ active transition, to enable read mode. A valid column address can be provided at any time (t_{RAD} minimum), independent of the $\overline{CS}$ active transition.

Both the $\overline{RAS}$ and $\overline{CS}$ clocks trigger a sequence of events which are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window. Both $\overline{CS}$ and output enable ($\overline{G}$) control read access time: $\overline{CS}$ and $\overline{G}$ must be active (and column address must be valid) by t_{RCD} maximum, and t_{RAC}-t_{GA} minimum, respectively, to guarantee valid data out (Q) at t_{RAC} (access time from $\overline{RAS}$ active transition). If either t_{RCD} maximum is exceeded or $\overline{G}$ active transition does not occur in time, read access time is determined by the $\overline{CS}$ and/or $\overline{G}$ clock active transition (t_{CAC}, t_{GA}).

The $\overline{RAS}$ and $\overline{CS}$ clocks must remain active for a minimum time of t_{RAS} and t_{CS}, respectively, to complete the read cycle. The column address must remain valid for t_{AH} after $\overline{RAS}$ inactive transition to complete the read cycle. $\overline{W}$ must remain high throughout the cycle, and for time t_{RRH} or t_{RCH} after $\overline{RAS}$ or $\overline{CS}$ inactive transition, respectively, to maintain the data at that bit location. Once $\overline{RAS}$ transitions to inactive, it must remain inactive for a minimum time of t_{RP} to precharge the internal device circuitry for the next active cycle. Q is valid, but not latched, as long as the $\overline{CS}$ and $\overline{G}$ clocks are active. When either the $\overline{CS}$ or $\overline{G}$ clock transitions to inactive, the output will switch to High Z, t_{OFF} or t_{GZ} after inactive transition.

WRITE CYCLE

The DRAM may be written with any of four cycles: early write, late write and "static column mode" early write, and read-write. Early and late write modes are discussed here, while static column mode write operations are covered in another section.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of $\overline{W}$ to active (V_{IL} level). Early and late write modes are distinguished by the active transition of $\overline{W}$ with respect to $\overline{CS}$ leading edge. Minimum active time t_{RAS} and t_{CS}, and precharge time t_{RP} apply to write mode, as in the read mode.

An early write cycle is characterized by $\overline{W}$ active transition at minimum time t_{WCS} before $\overline{CS}$ active transition. Column address set up and hold times (t_{ASC}, t_{CAH}), and data in (D) set up and hold times (t_{DS}, t_{DH}) are referenced to $\overline{CS}$ in an early write cycle. $\overline{RAS}$ and $\overline{CS}$ clocks must stay active for t_{RWL} and t_{CWL}, respectively, after the start of the early write operation to complete the cycle.

Q remains High Z throughout an early write cycle because $\overline{W}$ active transition precedes or coincides with $\overline{CS}$ active transition, keeping data-out buffers disabled effectively disabling $\overline{G}$.

A late write cycle (referred to as $\overline{G}$ controlled write) occurs when $\overline{W}$ active transition is made after $\overline{CS}$ active transition. $\overline{W}$ active transition could be delayed for almost 10 microseconds after $\overline{CS}$ active transition, ($t_{RAD} + t_{ASC} + t_{RWL} + 2t_T \leq t_{RAS}$, if other timing minimums (t_{ASC}, t_{RWL}, and t_T) are maintained. Column address and D timing parameters are referenced to $\overline{W}$ active transition in a late write cycle. Output buffers are enabled by $\overline{CS}$ active transition but Q may be indeterminate—see note 17 of AC operating conditions table. Parameters t_{RWL} and t_{CWL} also apply to late write cycles.

READ-WRITE CYCLE

A read-write cycle performs a read and then a write at the same address, during the same cycle. This cycle is basically a late write cycle, as discussed in the **WRITE CYCLE** section, except $\overline{W}$ must remain high for t_{CWD} and/or t_{AWD} minimum, to guarantee valid Q before writing the bit.

STATIC COLUMN MODE CYCLES

Static column mode refers to multiple successive data operations performed at any or all 512 column locations on the selected row of the 256 × 4 dynamic RAM during one $\overline{RAS}$ cycle. Read access time of multiple operations (t_{AA} or t_{CAC}) is considerably faster than the regular $\overline{RAS}$ clock access time t_{RAC}. Multiple operations can be performed simply by keeping $\overline{RAS}$ active. $\overline{CS}$ may be toggled between active and inactive states at any time within the $\overline{RAS}$ cycle.

Once the timing requirements for the initial read, write, or read-write cycle are met and $\overline{RAS}$ remains low, the device is ready for the next operation. Operations can be intermixed in any order, at any column address, subject to normal operating conditions previously described. Every write operation must be clocked with either $\overline{CS}$ or $\overline{W}$, as indicated in **static column**

2

mode early write cycle timing diagrams **A** and **B**. Column address and D timing parameters are referenced to the signal clocking the write operation. $\overline{CS}$ must be toggled inactive (t_{CP}) to perform a read operation after an early write operation (to turn output on), as indicated in **static column mode read/write mixed cycle** timing diagram. The maximum number of consecutive operations is limited by t_{RASC}. The cycle ends when $\overline{RAS}$ transitions to inactive.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge degrades with time and temperature, thus each bit must be periodically **refreshed** (recharged) to maintain the correct bit state. Bits in the MCM514258A require refresh every 8 milliseconds.

Refresh is accomplished by cycling through the 512 row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds for the MCM514258A. Burst refresh, a refresh of all 512 rows consecutively, must be performed every 8 milliseconds on the MCM514258A.

A normal read, write, or read-write operation to the RAM will refresh all the bits (2048) associated with the particular row decoded. Three other methods of refresh, **$\overline{RAS}$ only refresh, $\overline{CS}$ before $\overline{RAS}$ refresh,** and **hidden refresh** are available on this device for greater system flexibility.

$\overline{RAS}$-Only Refresh

$\overline{RAS}$-only refresh consists of $\overline{RAS}$ transition to active, latching the row address to be refreshed, while $\overline{CS}$ remains high (V_{IH}) throughout the cycle. An external counter is employed to ensure all rows are refreshed within the specified limit.

$\overline{CS}$ Before $\overline{RAS}$ Refresh

$\overline{CS}$ before $\overline{RAS}$ refresh is enabled by bringing $\overline{CS}$ active before $\overline{RAS}$. This clock order activates an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle. The output buffer remains at the same state it was in during the previous cycle (hidden refresh).

Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding $\overline{CS}$ active at the end of a read or write cycle, while $\overline{RAS}$ cycles inactive for t_{RP} and back to active, starts the hidden refresh. This is essentially the execution of a $\overline{CS}$ before $\overline{RAS}$ refresh from a cycle in progress (see Figure 1).

$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST

The internal refresh counter of this device can be tested with a **$\overline{CS}$ before $\overline{RAS}$ refresh counter test.** This test is performed with a read-write operation. During the test, the internal refresh counter generates the row address, while the external address supplies the column address. The entire array is refreshed after 512 test cycles, as indicated by the check data written in each row. See **$\overline{CS}$ before $\overline{RAS}$ refresh counter test cycle** timing diagram.

The test can be performed after a minimum of eight $\overline{CS}$ before $\overline{RAS}$ initialization cycles. Test procedure:

1. Write "0"s into all memory cells with normal write mode.
2. Select a column address, read "0" out and write "1" into the cell by performing the **$\overline{CS}$ before $\overline{RAS}$ refresh counter test, read-write cycle.** Repeat this operation 512 times.
3. Read the "1"s which were written in step 2 in normal read mode.
4. Using the same column address as in step 2, read "1" out and write "0" into the cell by performing the **$\overline{CS}$ before $\overline{RAS}$ refresh counter test, read-write cycle.** Repeat this operation 512 times.
5. Read "0"s which were written at in step 4 in normal read mode.
6. Repeat steps 1 to 5 using complement data.

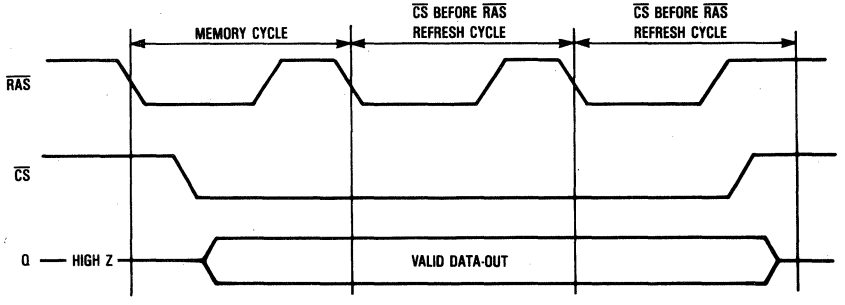
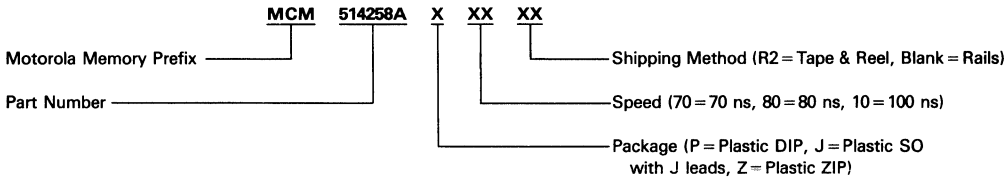


Figure 1. Hidden Refresh Cycle

ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers—	MCM514258AP70	MCM514258AJ70	MCM514258AJ70R2	MCM514258AZ70
	MCM514257AP80	MCM514258AJ80	MCM514258AJ80R2	MCM514258AZ80
	MCM514258AP10	MCM514258AJ10	MCM514258AJ10R2	MCM514258AZ10

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MCM514400
MCM51L4400

Advance Information

1M × 4 CMOS Dynamic RAM

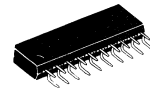
Page Mode

The MCM514400 is a 0.8μ CMOS high-speed, dynamic random access memory. It is organized as 1,048,576 four-bit words and fabricated with CMOS silicon-gate process technology. Advanced circuit design and fine line processing provide high performance, improved reliability, and low cost.

The MCM514400 requires only ten address lines; row and column address inputs are multiplexed. The device is packaged in a standard 350-mil-wide J-lead small outline package, and a 100-mil zig-zag in-line package (ZIP).

- Three-State Data Output
- Fast Page Mode
- Test Mode
- TTL-Compatible Inputs and Output
- $\overline{RAS}$ Only Refresh
- $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- Hidden Refresh
- 1024 Cycle Refresh: MCM514400 = 16 ms
  MCM51L4400 = 128 ms
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}):
  MCM514400-80 and MCM51L4400-80 = 80 ns (Max)
  MCM514400-10 and MCM51L4400-10 = 100 ns (Max)
- Low Active Power Dissipation:
  MCM514400-80 and MCM51L4400-80 = 578 mW (Max)
  MCM514400-10 and MCM51L4400-10 = 495 mW (Max)
- Low Standby Power Dissipation:
  MCM514400 and MCM51L4400 = 11 mW (Max, TTL Levels)
  MCM514400 = 5.5 mW (Max, CMOS Levels)
  MCM51L4400 = 2.2 mW (Max, CMOS Levels)

J PACKAGE
PLASTIC
SMALL OUTLINE
CASE 822A

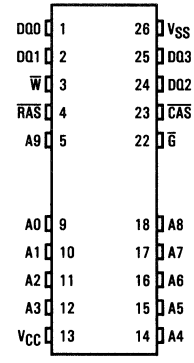


Z PACKAGE
PLASTIC
ZIG-ZAG IN-LINE
CASE 836

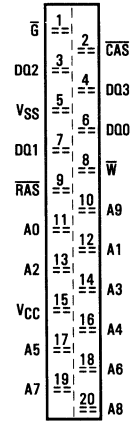
PIN NAMES	
A0-A9	Address Input
DQ0-DQ3	Data Input/Output
$\overline{G}$	Output Enable
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5 V)
V_{SS}	Ground

PIN ASSIGNMENT

SMALL OUTLINE

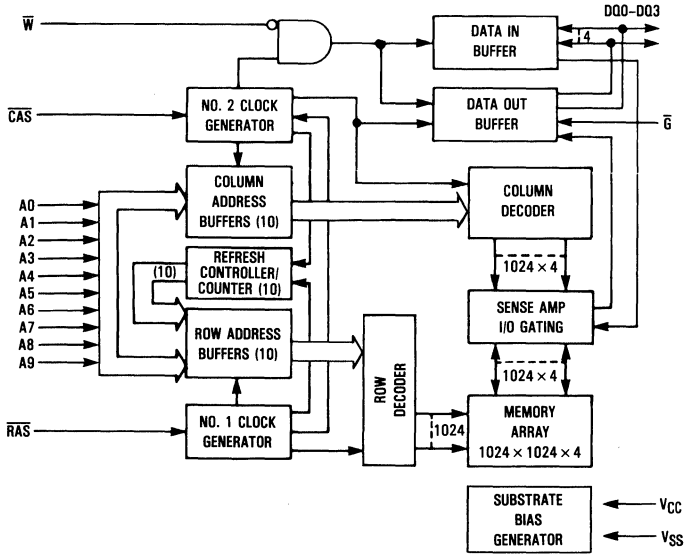


ZIG-ZAG IN-LINE



This document contains information on a new product. Specifications and information herein are subject to change without notice.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−1 to +7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−1 to +7	V
Data Out Current	I_{out}	50	mA
Power Dissipation	P_D	600	mW
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

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DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V	1
	V_{SS}	0	0	0		
Logic High Voltage, All Inputs	V_{IH}	2.4	–	6.5	V	1
Logic Low Voltage, All Inputs	V_{IL}	−1.0	–	0.8	V	1

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current MCM514400-80 and MCM51L4400-80, t_{RC} = 150 ns MCM514400-10 and MCM51L4400-10, t_{RC} = 180 ns	I_{CC1}	 – –	 105 90	mA	2
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	–	2.0	mA	
V_{CC} Power Supply Current During $\overline{RAS}$ only Refresh Cycles ($\overline{CAS}$ = V_{IH}) MCM514400-80 and MCM51L4400-80, t_{RC} = 150 ns MCM514400-10 and MCM51L4400-10, t_{RC} = 180 ns	I_{CC3}	 – –	 105 90	mA	2
V_{CC} Power Supply Current During Fast Page Mode Cycle ($\overline{RAS}$ = V_{IL}) MCM514400-80 and MCM51L4400-80, t_{PC} = 45 ns MCM514400-10 and MCM51L4400-10, t_{PC} = 55 ns	I_{CC4}	 – –	 70 60	mA	2, 3
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} − 0.2 V) MCM514400 MCM51L4400	I_{CC5}	– –	1.0 400	mA µA	
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle MCM514400-80 and MCM51L4400-80, t_{RC} = 150 ns MCM514400-10 and MCM51L4400-10, t_{RC} = 180 ns	I_{CC6}	 – –	 105 90	mA	2
V_{CC} Power Supply Current, Battery Backup Mode—MCM51L4400 only (t_{RC} = 125 µs; t_{RAS} = 1 µs; $\overline{CAS}$ = $\overline{CAS}$ Before $\overline{RAS}$ Cycle or 0.2 V; A0-A9, $\overline{G}$, $\overline{W}$, DQ0-DQ3 = V_{CC} − 0.2 V or 0.2 V)	I_{CC7}	–	500	µA	
Input Leakage Current (0 V ≤ V_{in} ≤ 6.5 V)	$I_{lkg(I)}$	−10	10	µA	
Output Leakage Current ($\overline{CAS}$ = V_{IH}, 0 V ≤ V_{out} ≤ 5.5 V)	$I_{lkg(O)}$	−10	10	µA	
Output High Voltage (I_{OH} = −5 mA)	V_{OH}	2.4	–	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	–	0.4	V	

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Max	Unit	Notes
Input Capacitance	A0-A9	C_{in}	5	pF	4
	$\overline{G}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$		7	pF	4
I/O Capacitance ($\overline{CAS}$ = V_{IH} to Disable Output)	DQ0-DQ3	$C_{I/O}$	7	pF	4

NOTES:
1. All voltages referenced to V_{SS}.
2. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
3. Measured with one address transition per page mode cycle.
4. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\Delta t/\Delta V$.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ, WRITE, AND READ-WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM514400-80 MCM51L4400-80		MCM514400-10 MCM51L4400-10		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	150	–	180	–	ns	5
Read-Write Cycle Time	t_{RELREL}	t_{RWC}	205	–	245	–	ns	5
Fast Page Mode Cycle Time	t_{CELCEL}	t_{PC}	50	–	60	–	ns	
Fast Page Mode Read-Write Cycle Time	t_{CELCEL}	t_{PRWC}	105	–	125	–	ns	
Access Time from $\overline{RAS}$	t_{RELQV}	t_{RAC}	–	80	–	100	ns	6, 7
Access Time from $\overline{CAS}$	t_{CELQV}	t_{CAC}	–	20	–	25	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	–	40	–	50	ns	6, 9
Access Time from Precharge $\overline{CAS}$	t_{CEHQV}	t_{CPA}	–	45	–	55	ns	6
$\overline{CAS}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	0	–	0	–	ns	6
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	20	0	20	ns	10
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{REHREL}	t_{RP}	60	–	70	–	ns	
$\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RAS}	80	10,000	100	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	80	200,000	100	200,000	ns	
$\overline{RAS}$ Hold Time	t_{CELREH}	t_{RSH}	20	–	25	–	ns	
$\overline{CAS}$ Hold Time	t_{RELCEH}	t_{CSH}	80	–	100	–	ns	
$\overline{CAS}$ Pulse Width	t_{CELCEH}	t_{CAS}	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RELCEL}	t_{RCD}	20	60	25	75	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	40	20	50	ns	12
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	–	10	–	ns	
$\overline{CAS}$ Precharge Time	t_{CEHCEL}	t_{CP}	10	–	10	–	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	–	0	–	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	–	15	–	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	–	0	–	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	–	20	–	ns	
Column Address Hold Time Referenced to $\overline{RAS}$	t_{RELAX}	t_{AR}	60	–	75	–	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{AVREH}	t_{RAL}	40	–	50	–	ns	

(continued)

NOTES:

1. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
6. Measured with a current load equivalent to 2 TTL (−200 µA, +4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
8. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
9. Assumes that $t_{RAD} \geq t_{RAD}$ (max).
10. t_{OFF} (max) and/or t_{GZ} (max) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
12. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.

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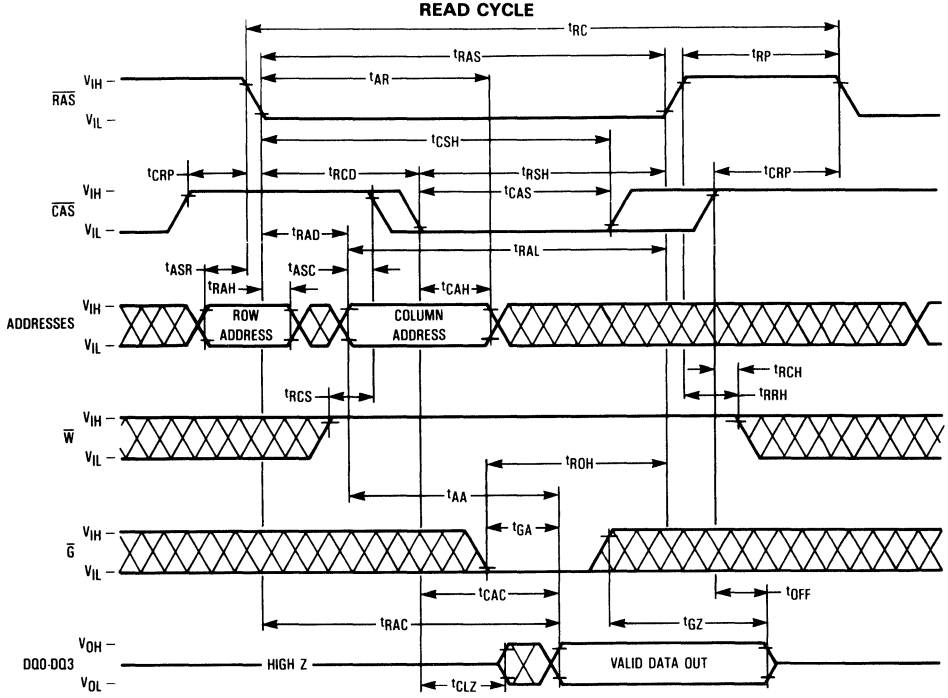
READ, WRITE, AND READ-WRITE CYCLES (Continued)

Parameter	Symbol		MCM514400-80 MCM51L4400-80		MCM514400-10 MCM51L4400-10		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	–	0	–	ns	
Read Command Hold Time Referenced to $\overline{CAS}$	t_{CEHWX}	t_{RCH}	0	–	0	–	ns	13
Read Command Hold Time Referenced to $\overline{RAS}$	t_{REHWX}	t_{RRH}	0	–	0	–	ns	13
Write Command Hold Time Referenced to $\overline{CAS}$	t_{CELWH}	t_{WCH}	15	–	20	–	ns	
Write Command Hold Time Referenced to $\overline{RAS}$	t_{RELWH}	t_{WCR}	60	–	75	–	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	15	–	20	–	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{WLREH}	t_{RWL}	20	–	25	–	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{WLCEH}	t_{CWL}	20	–	25	–	ns	
Data In Setup Time	t_{DVCEL}	t_{DS}	0	–	0	–	ns	14
Data In Hold Time	t_{CELDX}	t_{DH}	15	–	20	–	ns	14
Data In Hold Time Referenced to $\overline{RAS}$	t_{RELDX}	t_{DHR}	60	–	75	–	ns	
Refresh Period MCM514400 MCM51L4400	t_{RVRV}	t_{RFSH}	– –	16 128	– –	16 128	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	–	0	–	ns	15
$\overline{CAS}$ to Write Delay	t_{CELWL}	t_{CWD}	50	–	60	–	ns	15
$\overline{RAS}$ to Write Delay	t_{RELWL}	t_{RWD}	110	–	135	–	ns	15
Column Address to Write Delay Time	t_{AVWL}	t_{AWD}	70	–	85	–	ns	15
$\overline{CAS}$ Precharge to Write Delay Time (Page Mode)	t_{CEHWL}	t_{CPWD}	75	–	90	–	ns	15
$\overline{CAS}$ Setup Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEL}	t_{CSR}	5	–	10	–	ns	
$\overline{CAS}$ Hold Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEH}	t_{CHR}	15	–	20	–	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	t_{REHCEL}	t_{RPC}	0	–	0	–	ns	
$\overline{CAS}$ Precharge Time for $\overline{CAS}$ Before $\overline{RAS}$ Counter Test	t_{CEHCEL}	t_{CPT}	40	–	50	–	ns	
$\overline{RAS}$ Hold Time Referenced to $\overline{G}$	t_{GLREH}	t_{ROH}	10	–	20	–	ns	
$\overline{G}$ Access Time	t_{GLQV}	t_{GA}	–	20	–	25	ns	
$\overline{G}$ to Data Delay	t_{GLHDX}	t_{GD}	20	–	25	–	ns	
Output Buffer Turn-Off Delay Time from $\overline{G}$	t_{GHQZ}	t_{GZ}	0	20	0	20	ns	10
$\overline{G}$ Command Hold Time	t_{WLGL}	t_{GH}	20	–	25	–	ns	
Write Command Setup Time (Test Mode)	t_{WLREL}	t_{WTS}	10	–	10	–	ns	
Write Command Hold Time (Test Mode)	t_{RELWH}	t_{WTH}	10	–	10	–	ns	
Write to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh)	t_{WHREL}	t_{WRP}	10	–	10	–	ns	
Write to $\overline{RAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh)	t_{RELWL}	t_{WRH}	10	–	10	–	ns	

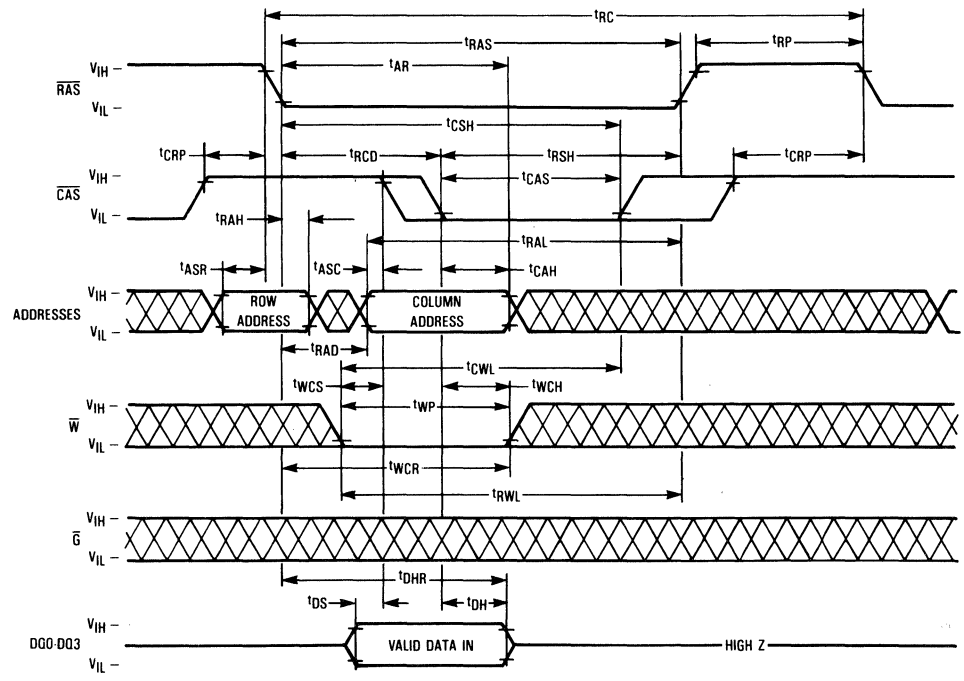
NOTES:

13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{W}$ leading edge in late write or read-write cycles.
15. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min), and $t_{CPWD} \geq t_{CPWD}$ (min) (page mode), the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

READ CYCLE



EARLY WRITE CYCLE



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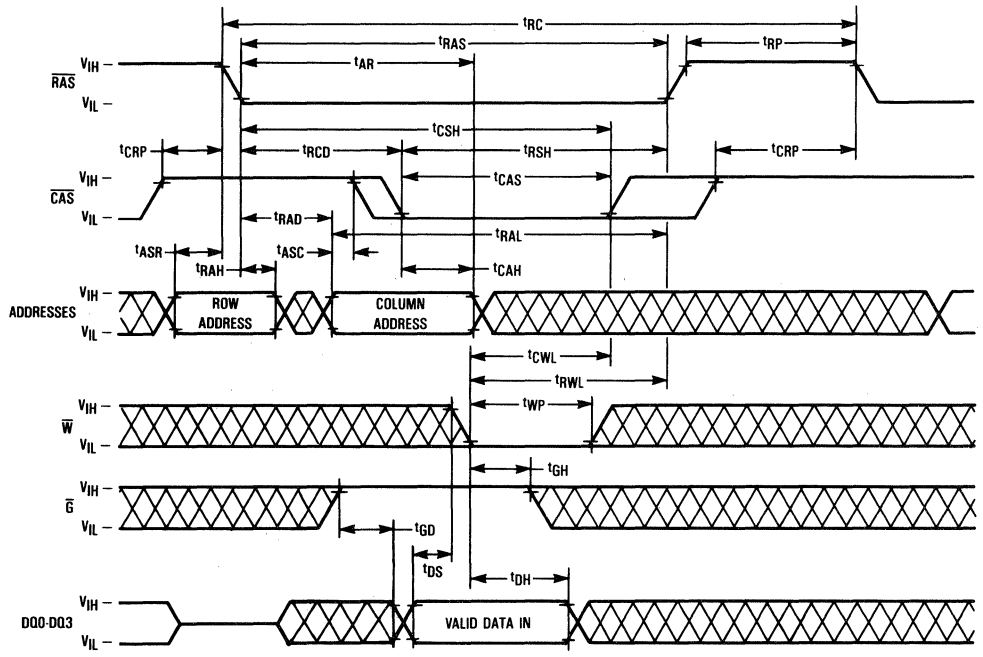
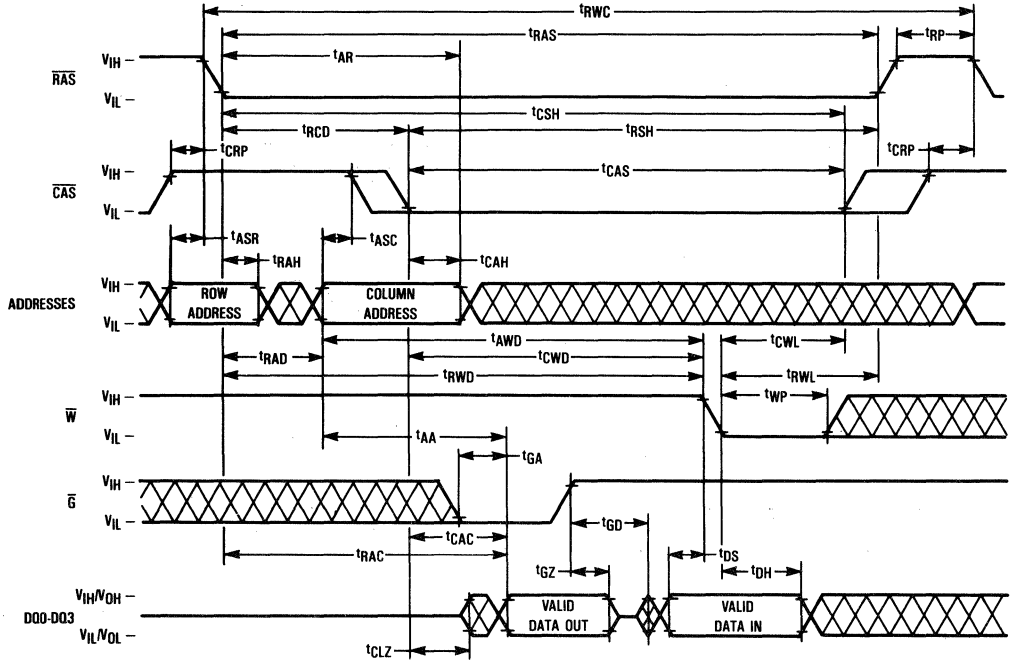
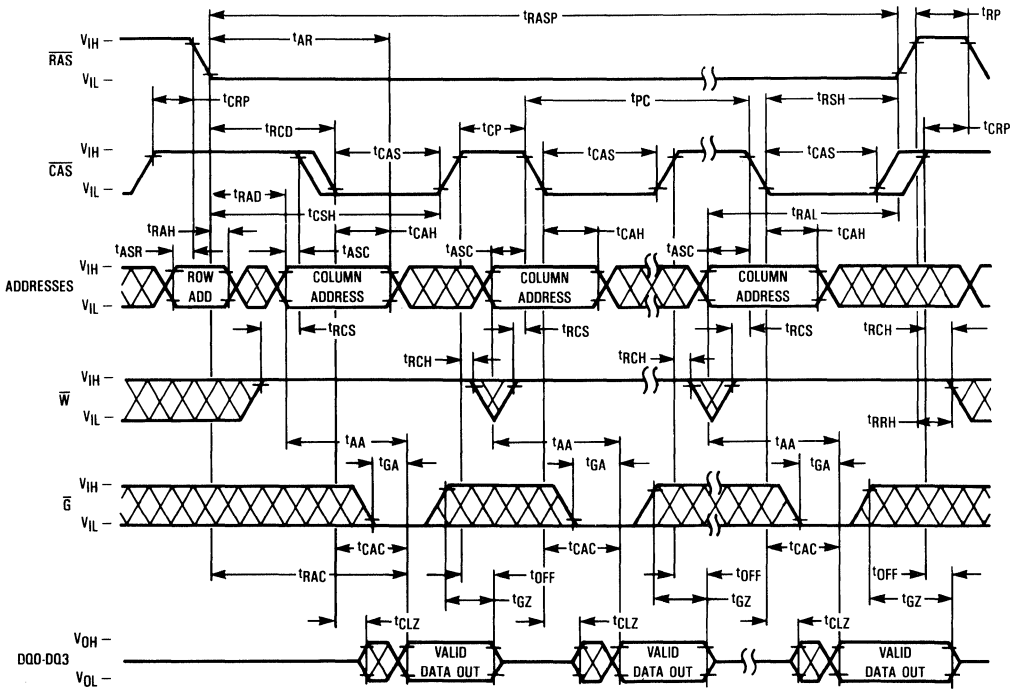
$\overline{G}$ CONTROLLED WRITE CYCLE



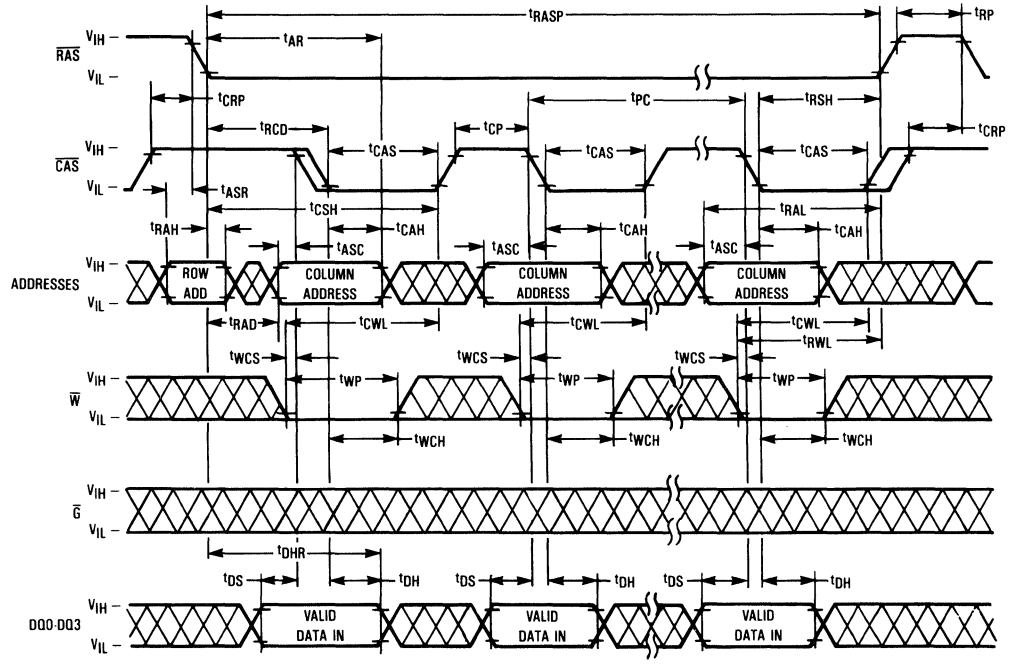
READ-WRITE CYCLE



FAST PAGE MODE READ CYCLE



FAST PAGE MODE EARLY WRITE CYCLE



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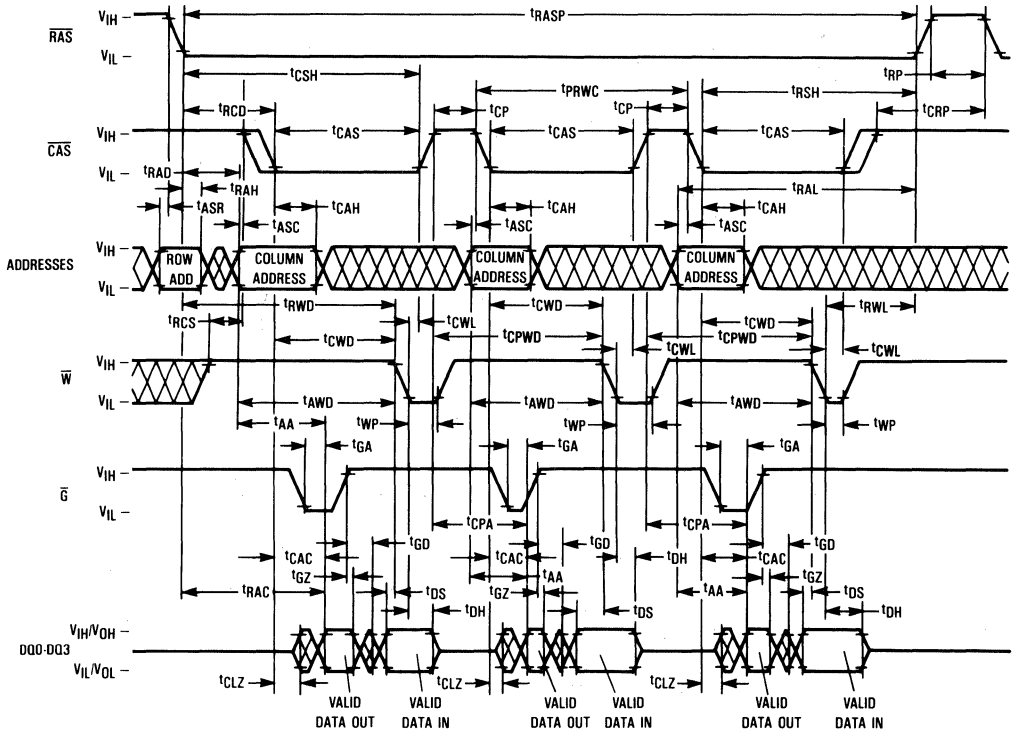
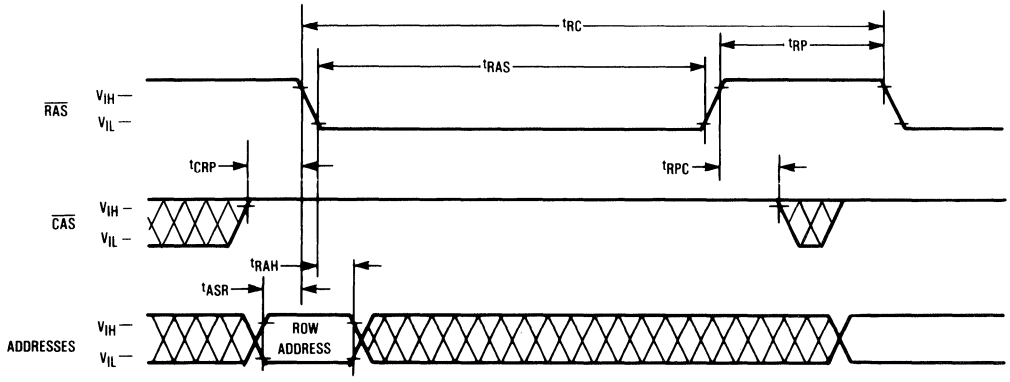
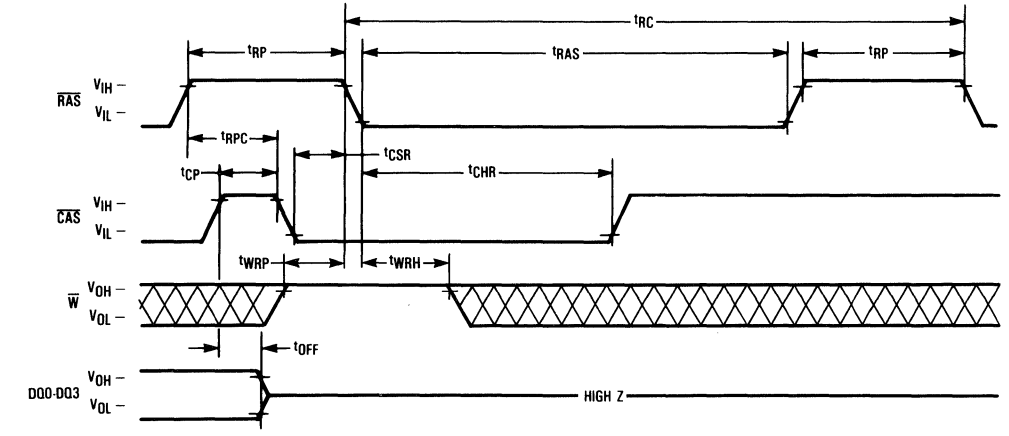
FAST PAGE MODE READ-WRITE CYCLE



$\overline{RAS}$ ONLY REFRESH CYCLE
($\overline{W}$ and $\overline{G}$ are Don't Care)



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE
($\overline{G}$ and A0-A9 are Don't Care)



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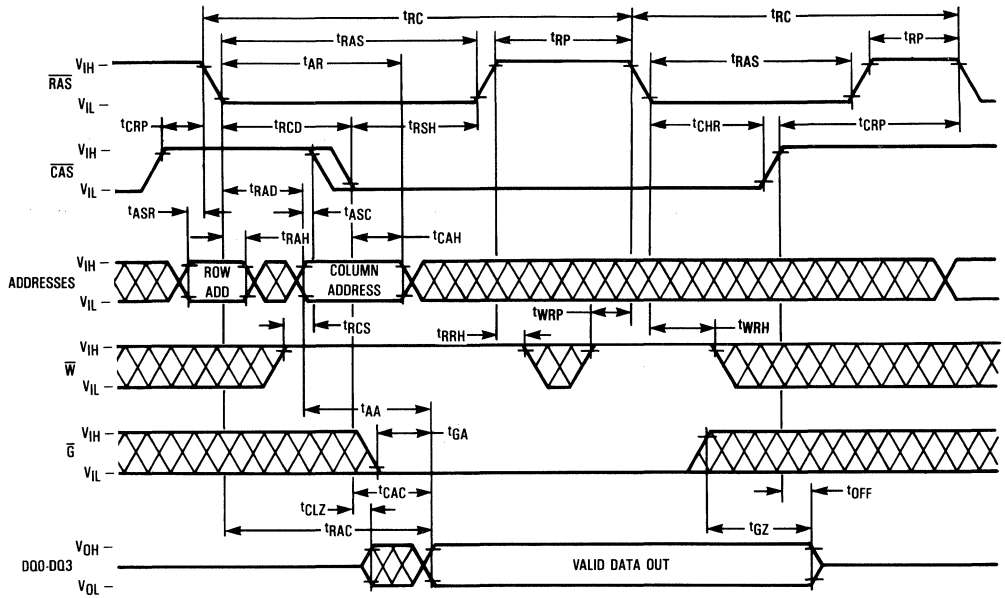
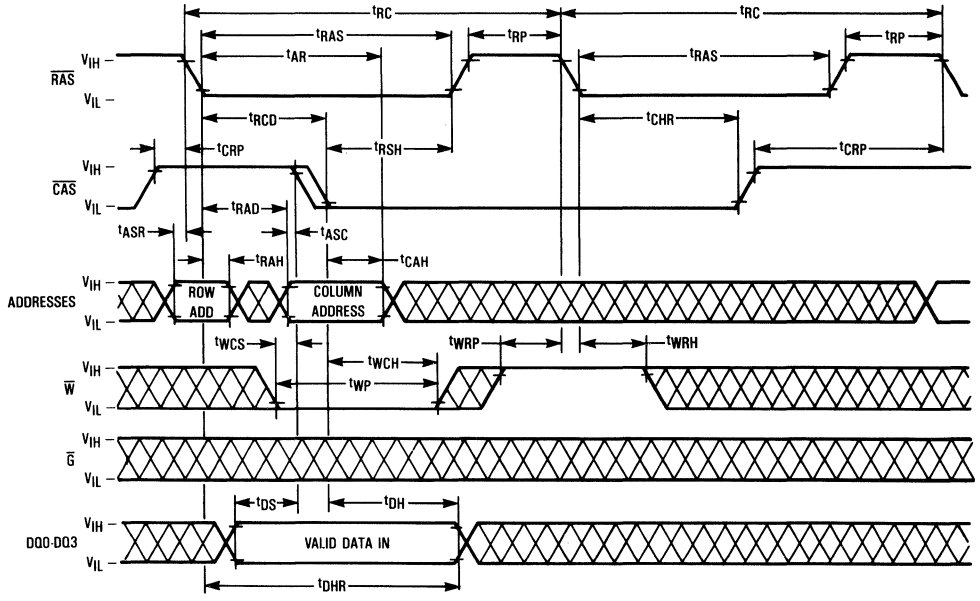
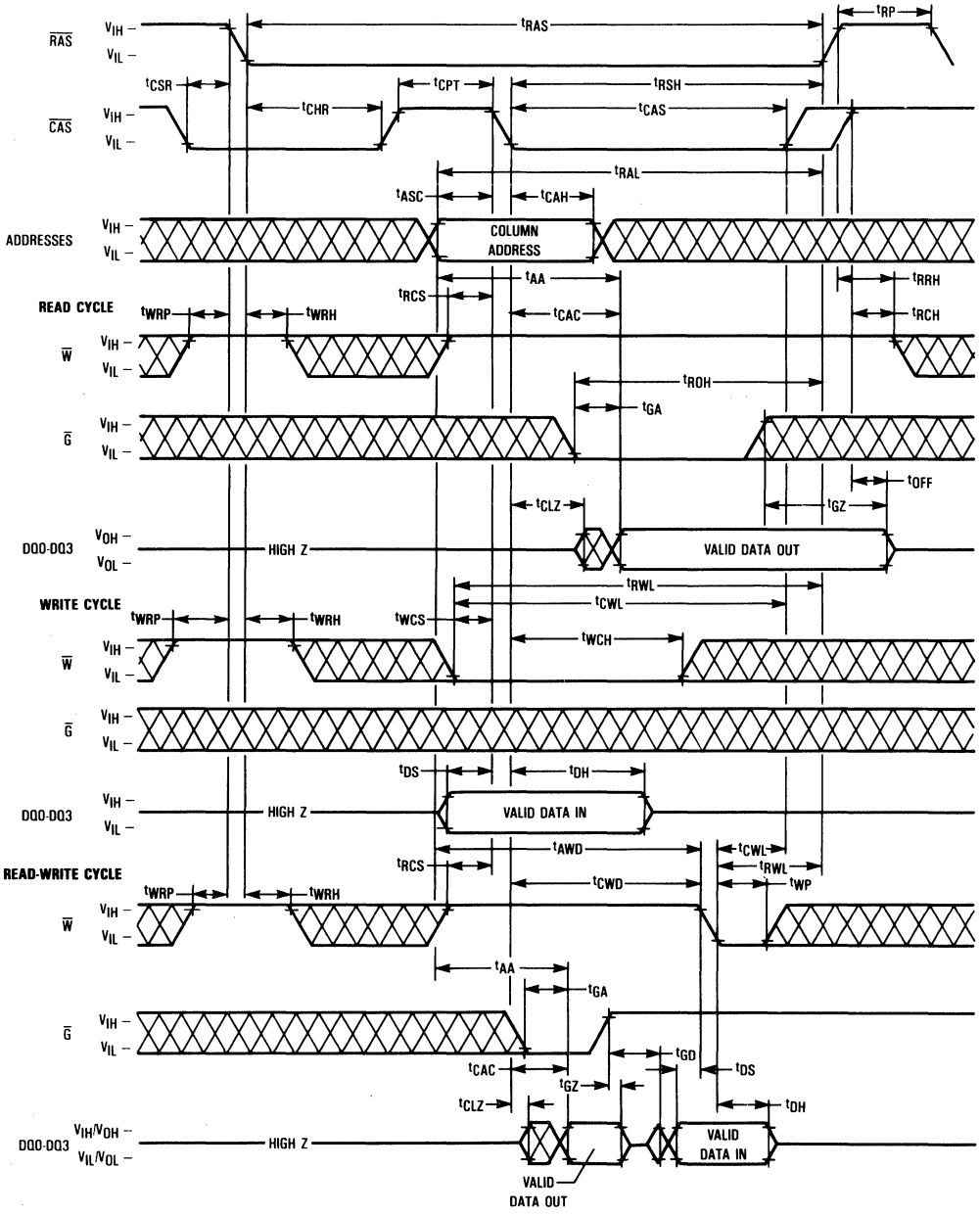
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (EARLY WRITE)



CAS BEFORE RAS REFRESH COUNTER TEST CYCLE



2

DEVICE INITIALIZATION

On power-up an initial pause of 200 microseconds is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize all dynamic nodes within the RAM. During an extended inactive state (greater than 16 milliseconds with the device powered up), a wake up sequence of eight active cycles is necessary to assure proper operation.

ADDRESSING THE RAM

The ten address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks, row address strobe ($\overline{RAS}$) and column address strobe ($\overline{CAS}$), into two separate 10-bit address fields. A total of twenty address bits, ten rows and ten columns, will decode one of the 1,048,576 bit locations in the device. $\overline{RAS}$ active transition is followed by $\overline{CAS}$ active transition (active = V_{IL}, t_{RCD} minimum) for all read or write cycles. The delay between $\overline{RAS}$ and $\overline{CAS}$ active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

The external $\overline{CAS}$ signal is ignored until an internal $\overline{RAS}$ signal is available. This "gate" feature on the external $\overline{CAS}$ clock enables the internal $\overline{CAS}$ line as soon as the row address hold time (t_{RAH}) specification is met (and defines t_{RCD} minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{CAS}$ clock.

There are three other variations in addressing the 1M × 4 RAM: **$\overline{RAS}$ only refresh cycle, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle**, and **page mode**. All three are discussed in separate sections that follow.

READ CYCLE

The DRAM may be read with four different cycles: "normal" random read cycle, page mode read cycle, read-write cycle, and page mode read-write cycle. The normal read cycle is outlined here, while the other cycles are discussed in separate sections.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with $\overline{RAS}$ and $\overline{CAS}$ active transitions latching the desired bit location. The write ($\overline{W}$) input level must be high (V_{IH}), t_{RCS} (minimum) before the $\overline{CAS}$ active transition, to enable read mode.

Both the $\overline{RAS}$ and $\overline{CAS}$ clocks trigger a sequence of events which are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window. Both $\overline{CAS}$ and output enable ($\overline{G}$) control read access time: $\overline{CAS}$ must be active before or at t_{RCD} maximum and $\overline{G}$ must be active t_{RAC}-t_{GA} (both minimum) after $\overline{RAS}$ active transition to guarantee valid data out (Q) at t_{RAC} (access time from $\overline{RAS}$ active transition). If the t_{RCD} maximum is exceeded and/or $\overline{G}$ active transition does not occur in time, read access time is determined by either the $\overline{CAS}$ or $\overline{G}$ clock active transition (t_{CAC} or t_{GA}).

The $\overline{RAS}$ and $\overline{CAS}$ clocks must remain active for a minimum time of t_{RAS} and t_{CAS} respectively, to complete the read cycle. $\overline{W}$ must remain high throughout the cycle, and for time t_{RRH} or t_{RCH} after $\overline{RAS}$ or $\overline{CAS}$ inactive transition, respectively, to maintain the data at that bit location. Once $\overline{RAS}$ transitions to inactive, it must remain inactive for a minimum time of t_{RP} to precharge the internal device circuitry for the next active cycle. Q is valid, but not latched, as long as the $\overline{CAS}$ and $\overline{G}$ clocks are active. When either the $\overline{CAS}$ or $\overline{G}$ clock transitions to inactive, the output will switch to High Z (three-state) t_{OFF} or t_{GZ} after the inactive transition.

WRITE CYCLE

The user can write to the DRAM with any of four cycles; early write, late write, page mode early write, and page mode read-write. Early and late write modes are discussed here, while page mode write operations are covered in another section.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of $\overline{W}$ to active (V_{IL}). Early and late write modes are distinguished by the active transition of $\overline{W}$, with respect to $\overline{CAS}$. Minimum active time t_{RAS} and t_{CAS}, and precharge time t_{RP} apply to write mode, as in the read mode.

An early write cycle is characterized by $\overline{W}$ active transition at minimum time t_{WCS} before $\overline{CAS}$ active transition. Data in (D) is referenced to $\overline{CAS}$ in an early write cycle. $\overline{RAS}$ and $\overline{CAS}$ clocks must stay active for t_{RWL} and t_{CWL}, respectively, after the start of the early write operation to complete the cycle.

Q remains in three-state condition throughout an early write cycle because $\overline{W}$ active transition precedes or coincides with $\overline{CAS}$ active transition, keeping data-out buffers and $\overline{G}$ disabled.

A late write cycle (referred to as $\overline{G}$-controlled write) occurs when $\overline{W}$ active transition is made after $\overline{CAS}$ active transition. $\overline{W}$ active transition could be delayed for almost 10 microseconds after $\overline{CAS}$ active transition, ($t_{RCD} + t_{CWD} + t_{RWL} + 2t_T \leq t_{RAS}$, if other timing minimums (t_{RCD}, t_{RWL} and t_T) are maintained. D is referenced to $\overline{W}$ active transition in a late write cycle. Output buffers are enabled by $\overline{CAS}$ active transition but outputs are switched off by $\overline{G}$ inactive transition, which is required to write to the device. Q may be indeterminate—see note 15 of AC operating conditions table. $\overline{RAS}$ and $\overline{CAS}$ must remain active for t_{RWL} and t_{CWL}, respectively, after $\overline{W}$ active transition to complete the write cycle. $\overline{G}$ must remain inactive for t_{GH} after $\overline{W}$ active transition to complete the write cycle.

READ-WRITE CYCLE

A read-write cycle performs a read and then a write at the same address, during the same cycle. This cycle is basically a late write cycle, as discussed in the **WRITE CYCLE** section, except $\overline{W}$ must remain high for t_{CWD} minimum after the $\overline{CAS}$ active transition, to guarantee valid Q before writing the bit.

PAGE MODE CYCLES

Page mode allows fast successive data operations at all 1024 column locations on a selected row of the 1M × 4 dynamic RAM. Read access time in page mode (t_{CAC}) is typically half the regular $\overline{RAS}$ clock access time, t_{RAC}. Page mode operation consists of keeping $\overline{RAS}$ active while toggling $\overline{CAS}$ between V_{IH} and V_{IL}. The row is latched by $\overline{RAS}$ active transition, while each $\overline{CAS}$ active transition allows selection of a new column location on the row.

A page mode cycle is initiated by a normal read, write, or read-write cycle, as described in prior sections. Once the timing requirements for the first cycle are met, $\overline{CAS}$ transitions to inactive for minimum of t_{CP}, while $\overline{RAS}$ remains low (V_{IL}).

The second $\overline{CAS}$ active transition while $\overline{RAS}$ is low initiates the first page mode cycle (t_{PC} or t_{PRWC}). Either a read, write, or read-write operation can be performed in a page mode cycle, subject to the same conditions as in normal operation (previously described). These operations can be intermixed in consecutive page mode cycles and performed in any order. The maximum number of consecutive page mode cycles is limited by t_{RASP}. Page mode operation is ended when $\overline{RAS}$ transitions to inactive, coincident with or following $\overline{CAS}$ inactive transition.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Each bit must be periodically **refreshed** (recharged) to maintain the correct bit state. Bits in the MCM514400 require refresh every 16 milliseconds, while refresh time for the MCM51L4400 is 128 milliseconds.

This is accomplished by cycling through the 1024 row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds for the MCM514400, and 124.8 microseconds for the MCM51L4400. Burst refresh, a refresh of all 1024 rows consecutively, must be performed every 16 milliseconds on the MCM514400 and 128 milliseconds on the MCM51L4400.

A normal read, write, or read-write operation to the RAM will refresh all the bits (4096) associated with the particular row decoded. Three other methods of refresh, **$\overline{RAS}$-only refresh**, **$\overline{CAS}$ before $\overline{RAS}$ refresh**, and **hidden refresh** are available on this device for greater system flexibility.

$\overline{RAS}$-Only Refresh

$\overline{RAS}$-only refresh consists of $\overline{RAS}$ transition to active, latching the row address to be refreshed, while $\overline{CAS}$ remains high (V_{IH}) throughout the cycle. An external counter is employed to ensure all rows are refreshed within the specified limit.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh

$\overline{CAS}$ before $\overline{RAS}$ refresh is enabled by bringing $\overline{CAS}$ active before $\overline{RAS}$. This clock order activates an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle. The output buffer remains at the same state it was in during the previous cycle (hidden refresh). $\overline{W}$ must be inactive for time t_{WRP} before and time t_{WRH} after $\overline{RAS}$ active transition to prevent switching the device into a **test mode cycle**.

Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding $\overline{CAS}$ active at the end of a read or write cycle, while $\overline{RAS}$ cycles inactive for t_{RP} and back to active, starts the hidden refresh. This is essentially the execution of a $\overline{CAS}$ before $\overline{RAS}$ refresh from a cycle in progress (see Figure 1). $\overline{W}$ is subject to the same conditions with respect to $\overline{RAS}$ active transition (to prevent test mode cycle) as in $\overline{CAS}$ before $\overline{RAS}$ refresh.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST

The internal refresh counter of this device can be tested with a **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test**. This test is performed with a read-write operation. During the test, the internal refresh counter generates the row address, while the external address supplies the column address. The entire array is refreshed after 1024 cycles, as indicated by the check data written in each row. See **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test cycle** timing diagram.

The test can be performed after a minimum of **eight $\overline{CAS}$ before $\overline{RAS}$** initialization cycles. Test procedure:

1. Write "0"s into all memory cells with normal write mode.
2. Select a column address, read "0" out and write "1" into the cell by performing the **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test, read-write cycle**. Repeat this operation 1024 times.
3. Read the "1"s which were written in step 2 in normal read mode.
4. Using the same starting column address as in step 2, read "1" out and write "0" into the cell by performing the **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test, read-write cycle**. Repeat this operation 1024 times.
5. Read "0"s which were written in step 4 in normal read mode.
6. Repeat steps 1 to 5 using complement data.

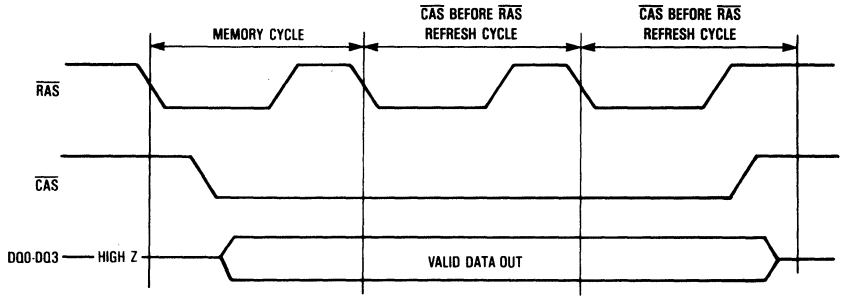


Figure 1. Hidden Refresh Cycle

2

TEST MODE

The internal organization of this device (512K × 8) allows it to be tested as if it were a 512K × 1 DRAM. Nineteen of the twenty addresses are used when operating the device in test mode. Column address A0 is ignored by the device in test mode. A test mode cycle reads and/or writes data to a bit in each of the eight 512K blocks (B0–B7) in parallel. External data out is determined by the internal test mode logic of the device. See truth table and test mode block diagram following.

Test mode is enabled by performing a **test mode cycle** (see test mode timing diagram and parameter specifications table). Test mode is disabled by a **$\overline{RAS}$ only refresh** cycle or **$\overline{CAS}$ before $\overline{RAS}$ refresh** cycle. The test mode performs refresh with the internal refresh counter like a **$\overline{CAS}$ before $\overline{RAS}$ refresh**.

Test Mode Truth Table

D	B0, B1	B2, B3	B4, B5	B6, B7	Q
0	0	0	0	0	1
1	1	1	1	1	1
—	Any Other				0

TEST MODE
AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

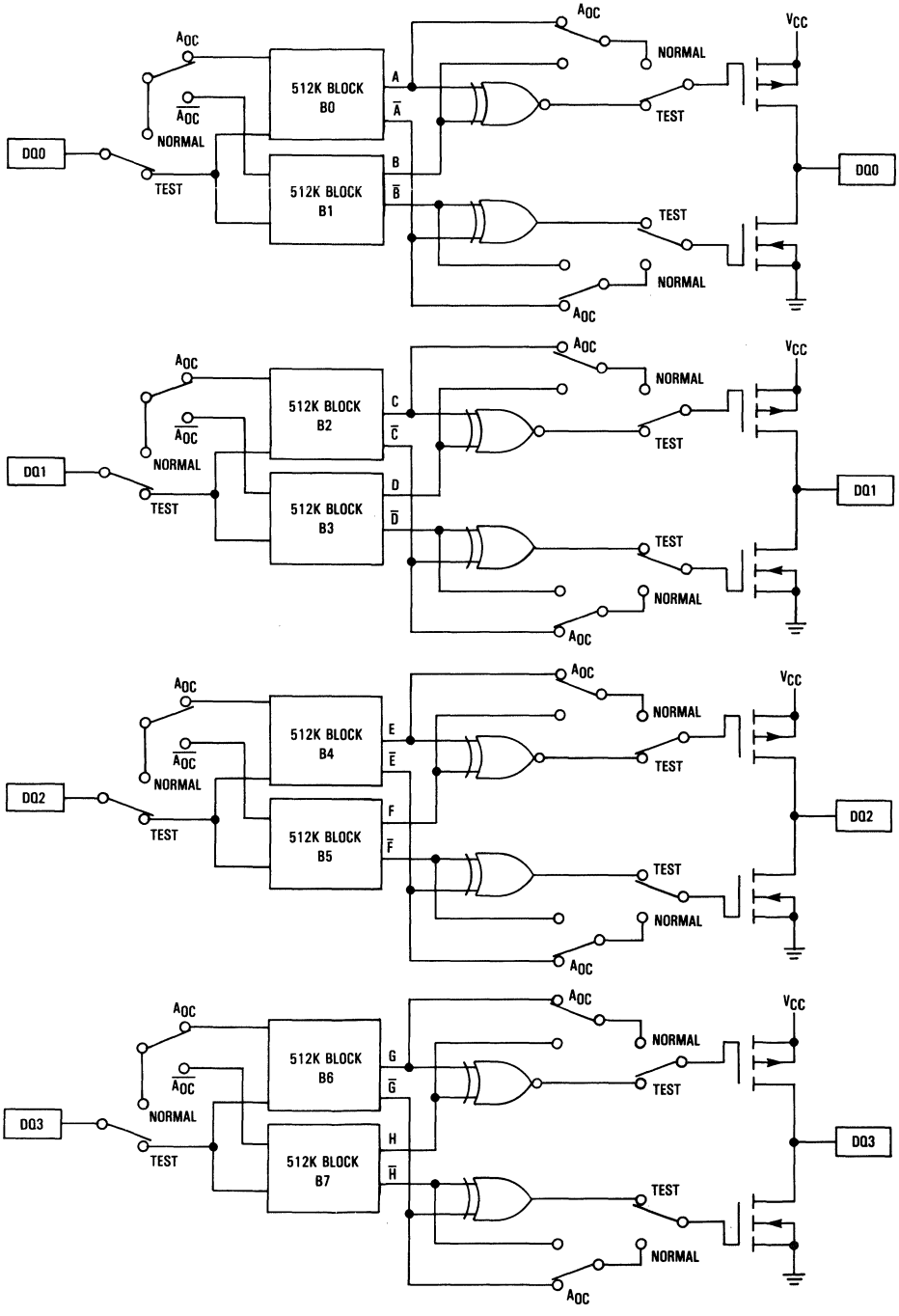
READ, WRITE, AND READ-WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM514400-80 MCM51L4400-80		MCM514400-10 MCM51L4400-10		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	155	—	185	—	ns	5
Read-Write Cycle Time	t_{RELREL}	t_{RWC}	210	—	250	—	ns	5
Fast Page Mode Cycle Time	t_{CELCEL}	t_{PC}	55	—	65	—	ns	
Fast Page Mode Read-Write Cycle Time	t_{CELCEL}	t_{PRWC}	115	—	135	—	ns	
Access Time from $\overline{RAS}$	t_{RELQV}	t_{RAC}	—	85	—	105	ns	6, 7
Access Time from $\overline{CAS}$	t_{CELQV}	t_{CAC}	—	25	—	30	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	—	45	—	55	ns	6, 9
Access Time from Precharge $\overline{CAS}$	t_{CEHQV}	t_{CPA}	—	50	—	60	ns	6
$\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RAS}	85	10,000	105	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	85	200,000	105	200,000	ns	
$\overline{RAS}$ Hold Time	t_{CELREH}	t_{RSH}	25	—	30	—	ns	
$\overline{CAS}$ Hold Time	t_{RELCEH}	t_{CSH}	85	—	105	—	ns	
$\overline{CAS}$ Pulse Width	t_{CELCEH}	t_{CAS}	25	10,000	30	10,000	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{AVREH}	t_{RAL}	45	—	55	—	ns	
$\overline{CAS}$ to Write Delay	t_{CELWL}	t_{CWD}	55	—	65	—	ns	10
$\overline{RAS}$ to Write Delay	t_{RELWL}	t_{RWD}	115	—	140	—	ns	10
Column Address to Write Delay Time	t_{AVWL}	t_{AWD}	75	—	90	—	ns	10
$\overline{CAS}$ Precharge to Write Delay Time (Page Mode)	t_{CEHWL}	t_{CPWD}	85	—	95	—	ns	10
$\overline{G}$ Access Time	t_{GLQV}	t_{GA}	—	25	—	30	ns	
$\overline{G}$ Command Hold Time	t_{WLGL}	t_{GH}	25	—	30	—	ns	

NOTES:

1. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
6. Measured with a current load equivalent to 2 TTL (−200 μA, +4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
8. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
9. Assumes that $t_{RAD} \geq t_{RAD}$ (max).
10. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min), and $t_{CPWD} \geq t_{CPWD}$ (min) (page mode), the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

TEST MODE BLOCK DIAGRAM



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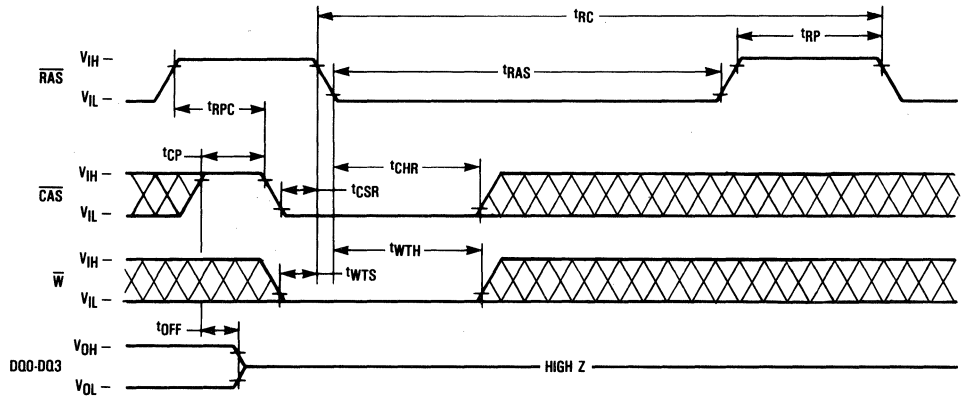
TEST MODE CYCLE
($\overline{G}$ and A0 to A9 are Don't Care)



ORDERING INFORMATION
(Order by Full Part Number)

MCM 514400 or 51L4400 X XX XX

- Motorola Memory Prefix
- Part Number
- Shipping Method (R2 = Tape & Reel, Blank = Rails)
- Speed (80 = 80 ns, 10 = 100 ns)
- Package (J = Plastic SO with J leads, Z = Plastic ZIP)

Full Part Numbers—	MCM514400J80	MCM514400J80R2	MCM514400Z80
	MCM514400J10	MCM514400J10R2	MCM514400Z10
	MCM51L4400J80	MCM51L4400J80R2	MCM51L4400Z80
	MCM51L4400J10	MCM51L4400J10R2	MCM51L4400Z10

DRAM Modules 3

DRAM MODULES (Contact DRAM Marketing for Custom DRAM Modules)

Density	Organi-zation	Motorola Part Number	Address Access Time (ns Max)	Operating Current (mA Max)	Pin Count	Package Options
8M	1Mx8	MCM81000	70/80/100	640/560/480	30	(S)IMM, (L)SIP
		MCM8L1001	70/80/100	640/560/480	30	(S)IMM, (L)SIP
		MCM81001	70/80/100	640/560/480	30	(S)IMM, (L)SIP
		MCM81002	70/80/100	640/560/480	30	(S)IMM, (L)SIP
8M w/Parity	1Mx9	MCM91000	70/80/100	720/630/540	30	(S)IMM, (L)SIP, SG (gold)
		MCM9L1000	70/80/100	720/630/540	30	(S)IMM, (L)SIP, SG (gold)
		MCM91001	70/80/100	720/630/540	30	(S)IMM, (L)SIP
		MCM91002	70/80/100	720/630/540	30	(S)IMM, (L)SIP
2M	256Kx8	MCM84256	70/80/100	160/140/120	30	(S)IMM
		MCM8L4256	70/80/100	160/140/120	30	(S)IMM
2M w/Parity	256Kx9	MCM94256	70/80/100	240/210/190	30	(S)IMM
		MCM9L4256	70/80/100	240/210/190	30	(S)IMM
4M	1Mx4	MCM41000	80/100	280/240	26	(Z)IMM
	4Mx1	MCM11400	80/100	90/80	26	(Z)IMM
32M	4Mx8	MCM84000	80/100	800/680	30	(S)IMM
		MCM8L4000	80/100	800/680	30	(S)IMM
32M w/Parity	4Mx9	MCM94000	80/100	900/765	30	(S)IMM
		MCM9L4000	80/100	900/765	30	(S)IMM
8M w/Parity	256Kx36	MCM36256	70/80/100	960/840/760	72	(S)IMM, SG (gold)
16M w/Parity	512Kx36	MCM36512	70/80/100	1920/1680/1520	72	(S)IMM, SG (gold)
32M w/Parity	1Mx36	MCM36100	80/100	1144/984	72	(S)IMM, SG (gold)
64M w/Parity	2Mx36	MCM36200	80/100	1120/960	72	(S)IMM, SG (gold)
8M w/Parity	256Kx40	MCM40256*	70/80/100	800/700/600	72	(S)IMM, SG (gold)
16M w/Parity	512Kx40	MCM40512*	70/80/100	820/720/620	72	(S)IMM, SG (gold)
32M w/Parity	1Mx40	MCM40100*	80/100	1050/900	72	(S)IMM, SG (gold)
64M w/Parity	2Mx40	MCM40200*	80/100	1070/920	72	(S)IMM, SG (gold)

*To be introduced.

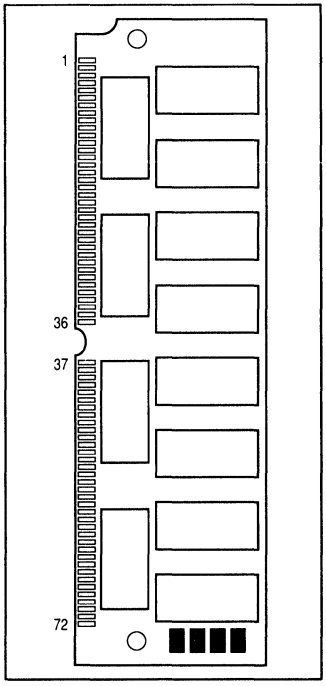
Product Preview

MCM36100
MCM36L100

1M × 36 Bit Dynamic Random Access Memory Module

The MCM36100S is a 36M, dynamic random access memory (DRAM) module organized as 1,048,576 × 36 bits. The module is a 72-lead single-in-line memory module (SIMM) consisting of eight MCM514400 DRAMs housed in standard 350-mil-wide SOJ packages and four CMOS 1M × 1 DRAMs housed in 20/26 lead SOJ packages, mounted on a substrate along with a 0.22 µF (min) decoupling capacitor mounted under each DRAM. The MCM514400 is a CMOS high speed, dynamic random access memory organized as 1,048,576 four-bit words and fabricated with CMOS silicon-gate process technology.

- Three-State Data Output
- Early-Write Common I/O Capability
- Fast Page Mode Capability
- TTL-Compatible Inputs and Outputs
- $\overline{RAS}$ Only Refresh
- $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- Hidden Refresh
- 1024 Cycle Refresh:
  MCM36100S = 16 ms (Max)
  MCM36L100S = 128 ms (Max)
- Consists of Eight 1M × 4 DRAMs, Four 1M × 1 DRAMs, and Twelve 0.22 µF (Min) Decoupling Capacitors
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}):
  MCM36100S-80 = 80 ns (Max)
  MCM36100S-10 = 100 ns (Max)
- Low Active Power Dissipation:
  MCM36100S-80 = 6.16 W (Max)
  MCM36100S-10 = 5.28 W (Max)
- Low Standby Power Dissipation:
  TTL Levels = 132 mW (Max)
  CMOS Levels = 66 mW (Max, MCM36100S)
  CMOS Levels = 22 mW (Max, MCM36L100S)



PIN NAMES

A0–A9	Address Inputs
DQ0–DQ35	Data Input/Output
$\overline{CAS0}$–$\overline{CAS3}$	Column Address Strobe
PD1–PD4	Presence Detect
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{W}$	Read/Write Input
V_{CC}	Power (+ 5 V)
V_{SS}	Ground
NC	No Connection

All power supply and ground pins must be connected for proper operation of the device.

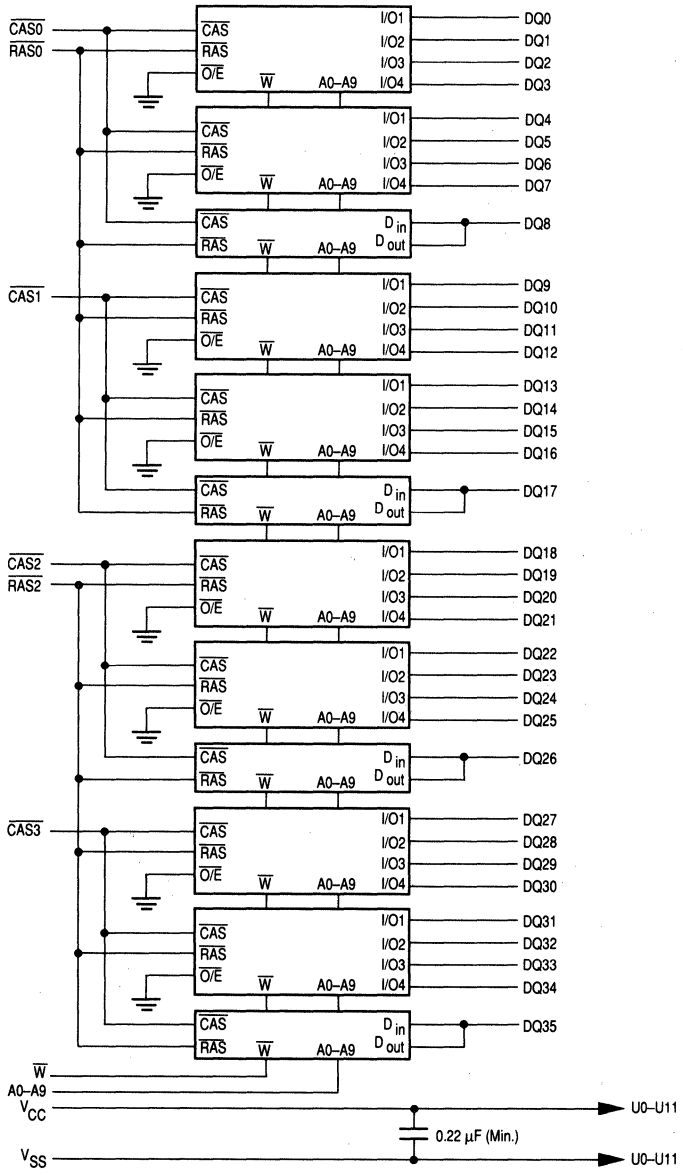
PIN OUT

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V_{SS}	13	A1	25	DQ24	37	DQ17	49	DQ9	61	DQ14
2	DQ0	14	A2	26	DQ7	38	DQ35	50	DQ27	62	DQ33
3	DQ18	15	A3	27	DQ25	39	V_{SS}	51	DQ10	63	DQ15
4	DQ1	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ28	64	DQ34
5	DQ19	17	A5	29	NC	41	$\overline{CAS2}$	53	DQ11	65	DQ16
6	DQ2	18	A6	30	V_{CC}	42	$\overline{CAS3}$	54	DQ29	66	NC
7	DQ20	19	NC	31	A8	43	$\overline{CAS1}$	55	DQ12	67	PD1
8	DQ3	20	DQ4	32	A9	44	$\overline{RAS0}$	56	DQ30	68	PD2
9	DQ21	21	DQ22	33	NC	45	NC	57	DQ13	69	PD3
10	V_{CC}	22	DQ5	34	$\overline{RAS2}$	46	NC	58	DQ31	70	PD4
11	NC	23	DQ23	35	DQ26	47	$\overline{W}$	59	V_{CC}	71	NC
12	A0	24	DQ6	36	DQ8	48	NC	60	DQ32	72	V_{SS}

This document contains information on a new product. Specifications and information herein are subject to change without notice.

3

BLOCK DIAGRAM



PRESENCE DETECT PIN OUT			
Pin Name	**70 ns**	**80 ns**	**100 ns**
PD1	V_{SS}	V_{SS}	V_{SS}
PD2	V_{SS}	V_{SS}	V_{SS}
PD3	V_{SS}	NC	V_{SS}
PD4	NC	V_{SS}	V_{SS}

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 1 to + 7	V
Voltage Relative to V_{SS} (For Any Pin Except V_{CC})	V_{in}, V_{out}	– 1 to + 7	V
Data Output Current per DQ Pin	I_{out}	50	mA
Power Dissipation	P_D	8.4	W
Operating Temperature Range	T_A	0 to + 70	°C
Storage Temperature Range	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high impedence circuits.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V	1
	V_{SS}	0	0	0		
Logic High Voltage, All Inputs	V_{IH}	2.4	—	6.5	V	1
Logic Low Voltage, All Inputs	V_{IL}	– 1.0	—	0.8	v	1

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current MCM36100-80, t_{RC} = 150 ns MCM36100-10, t_{RC} = 180 ns	I_{CC1}	 — —	 1120 960	mA	2
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	—	24	mA	
V_{CC} Power Supply Current During $\overline{RAS}$ only Refresh Cycles MCM36100-80, t_{RC} = 150 ns MCM36100-10, t_{RC} = 180 ns	I_{CC3}	 — —	 1120 960	mA	2
V_{CC} Power Supply Current During Fast Page Mode Cycle MCM36100-80, t_{RC} = 150 ns MCM36100-10, t_{RC} = 180 ns	I_{CC4}	 — —	 760 640	mA	2
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V) MCM36100 MCM36L100	I_{CC5}	— —	12 4	mA	
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle MCM36100-80, t_{RC} = 150 ns MCM36100-10, t_{RC} = 180 ns	I_{CC6}	 — —	 1120 960	mA	2
Input Leakage Current ($V_{SS} \le V_{in} \le V_{CC}$)	$I_{lkg(I)}$	– 120	120	µA	
Output Leakage Current ($\overline{CAS}$ at Logic 1, $V_{SS} \le V_{out} \le V_{CC}$)	$I_{lkg(O)}$	– 20	20	µA	
Output High Voltage (I_{OH} = – 5 mA)	V_{OH}	2.4	—	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	—	0.4	V	

NOTES:
1. All voltages referenced to V_{SS}.
2. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.

3

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Min	Max	Unit	Notes
Input Capacitance (A0–A9)	C_{I1}	—	88	pF	1
Input Capacitance ($\overline{W}$)	C_{I2}	—	94	pF	1
Input Capacitance ($\overline{RAS0}$, $\overline{RAS2}$)	C_{I3}	—	52	pF	1
Input Capacitance ($\overline{CAS0}$–$\overline{CAS3}$)	C_{I4}	—	36	pF	1
I/O Capacitance (DQ0–DQ7, DQ9–DQ16, DQ18–DQ25, DQ27–DQ34)	C_{DQ1}	—	17	pF	1
I/O Capacitance (DQ8, DQ17, DQ26, DQ35)	C_{DQ2}	—	22	pF	1

NOTE:
1. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: C = 1 Δ t / Δ V.

AC OPERATING CONDITIONS AND CHARACTERISTICS
(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ AND WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM36100-80		MCM36100-10		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	150	—	180	—	ns	5
Page Mode Cycle Time	t_{CELCEL}	t_{PC}	50	—	60	—	ns	
Access Time from $\overline{RAS}$	t_{RELQV}	t_{RAC}	—	80	—	100	ns	6, 7
Access Time from $\overline{CAS}$	t_{CELQV}	t_{CAC}	—	20	—	25	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	—	40	—	50	ns	6, 9
Access Time from Precharge $\overline{CAS}$	t_{CEHQV}	t_{CPA}	—	45	—	55	ns	6
$\overline{CAS}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	0	—	0	—	ns	6
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	20	0	20	ns	10
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{REHREL}	t_{RP}	60	—	70	—	ns	
$\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RAS}	80	10,000	100	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	80	100,000	100	100,000	ns	
$\overline{RAS}$ Hold Time	t_{CELREH}	t_{RSH}	25	—	25	—	ns	
$\overline{CAS}$ Hold TIme	t_{RELCEH}	t_{CSH}	80	—	100	—	ns	
$\overline{CAS}$ Pulse Width	t_{CELCEH}	t_{CAS}	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RELCEL}	t_{RCD}	20	60	25	75	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	40	20	50	ns	12

(continued)

NOTES:
1. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
6. Measured with a current load equivalent to 2 TTL (– 200 µA, + 4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
8. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
9. Assumes that $t_{RAD} \geq t_{RAD}$ (max).
10. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively to t_{CAC}.
12. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.

READ AND WRITE CYCLES (Continued)

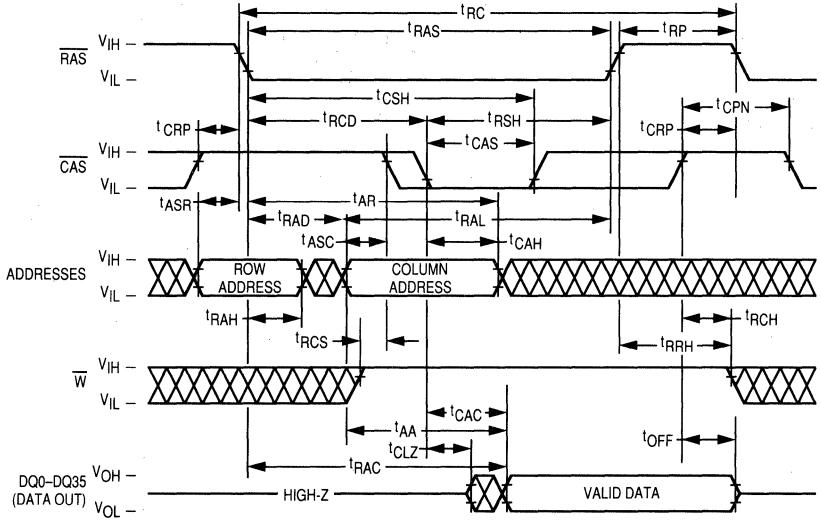
Parameter	Symbol		MCM36100-80		MCM36100-10		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	—	10	—	ns	
$\overline{CAS}$ Precharge Time (Page Mode Cyle Only)	t_{CEHCEL}	t_{CP}	10	—	10	—	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	—	15	—	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	—	20	—	ns	
Column Address Hold Time Referenced to $\overline{RAS}$	t_{RELAX}	t_{AR}	60	—	75	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{AVREH}	t_{RAL}	40	—	50	—	ns	
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	0	—	ns	
Read Command Hold Time Referenced to $\overline{CAS}$	t_{CEHWX}	t_{RCH}	0	—	0	—	ns	13
Read Command Hold Time Referenced to $\overline{RAS}$	t_{REHWX}	t_{RRH}	0	—	0	—	ns	13
Write Command Hold Time Referenced to $\overline{CAS}$	t_{CELWH}	t_{WCH}	15	—	20	—	ns	
Write Command Hold Time Referenced to $\overline{RAS}$	t_{RELWH}	t_{WCR}	60	—	75	—	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	15	—	20	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{WLREH}	t_{RWL}	20	—	25	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{WLCEH}	t_{CWL}	20	—	25	—	ns	
Data in Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	ns	14, 15
Data in Hold Time	t_{CELDX}	t_{DH}	15	—	20	—	ns	14, 15
Data in Hold Time Referenced to $\overline{RAS}$	t_{RELDX}	t_{DHR}	60	—	75	—	ns	
Refresh Period MCM36100 MCM36L100	t_{RVRV}	t_{RFSH}	— —	16 128	— —	16 128	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	—	0	—	ns	15, 16
$\overline{CAS}$ Setup Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEL}	t_{CSR}	10	—	10	—	ns	
$\overline{CAS}$ Hold Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEH}	t_{CHR}	30	—	30	—	ns	
$\overline{CAS}$ Precharge to $\overline{CAS}$ Active Time	t_{REHCEL}	t_{RPC}	0	—	0	—	ns	
$\overline{CAS}$ Precharge Time for $\overline{CAS}$ Before $\overline{RAS}$ Counter Test	t_{CEHCEL}	t_{CPT}	40	—	50	—	ns	
$\overline{CAS}$ Precharge Time	t_{CEHCEL}	t_{CPN}	10	—	15	—	ns	

NOTES:

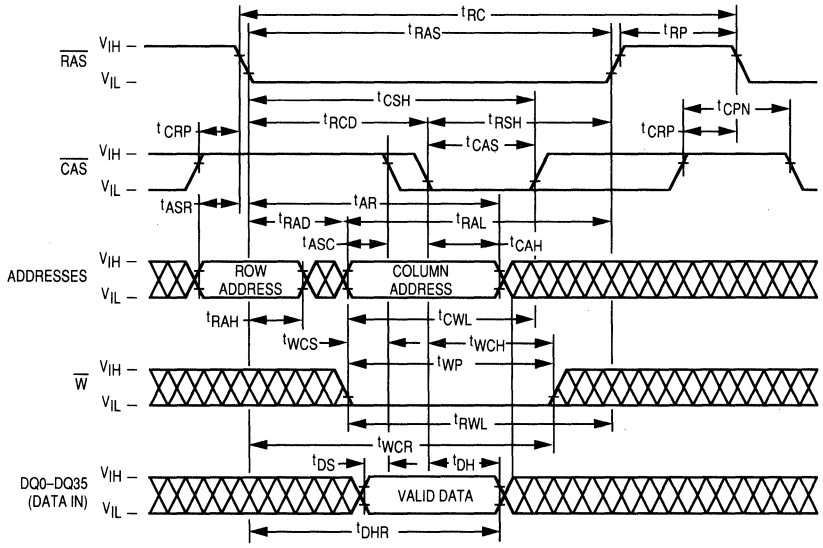
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles.
15. Early write only ($t_{WCS} \geq t_{WCS}$ (min)).
16. t_{WCS} is not a restrictive operating parameter. It is included in the data sheet as an electrical characteristic only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle. If this condition is not satisifed, the condition of the data out (at access time) is indeterminate.

3

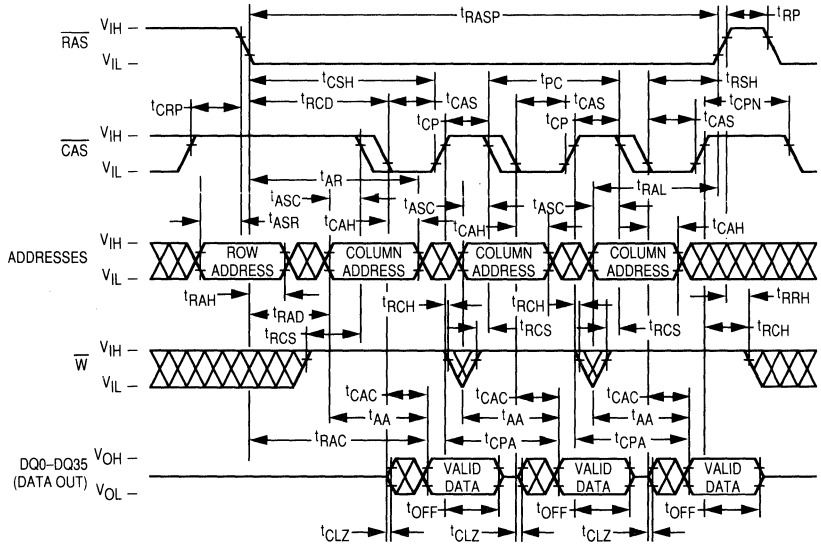
READ CYCLE



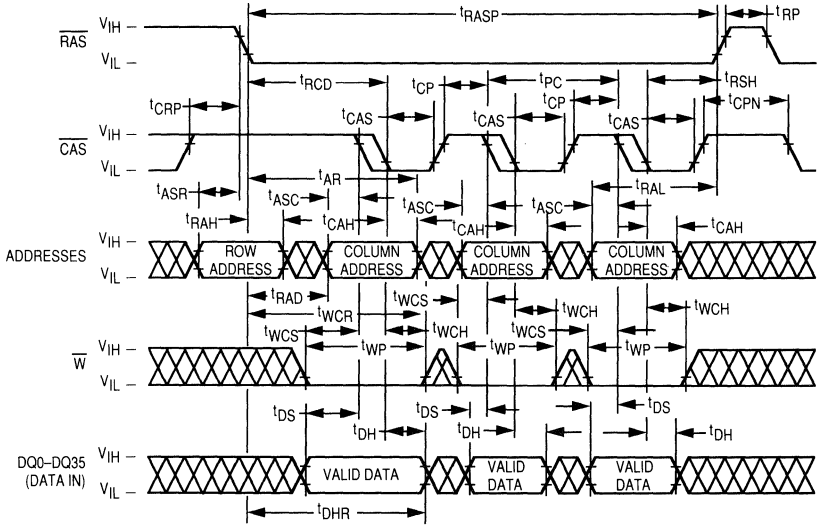
EARLY WRITE CYCLE



FAST PAGE MODE READ CYCLE

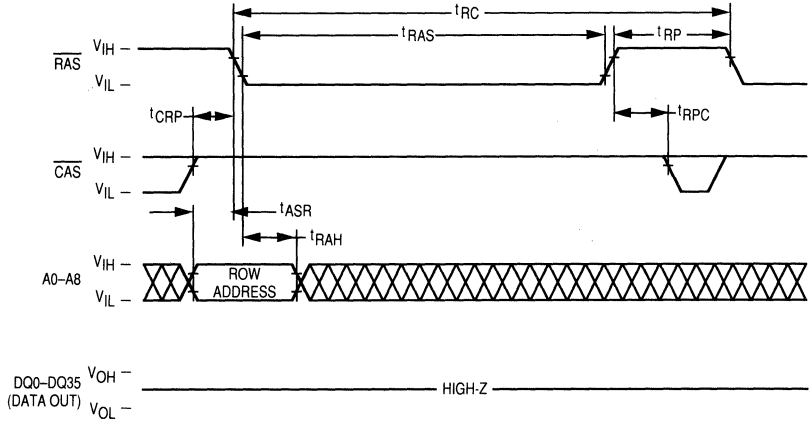


FAST PAGE MODE WRITE CYCLE (EARLY WRITE)

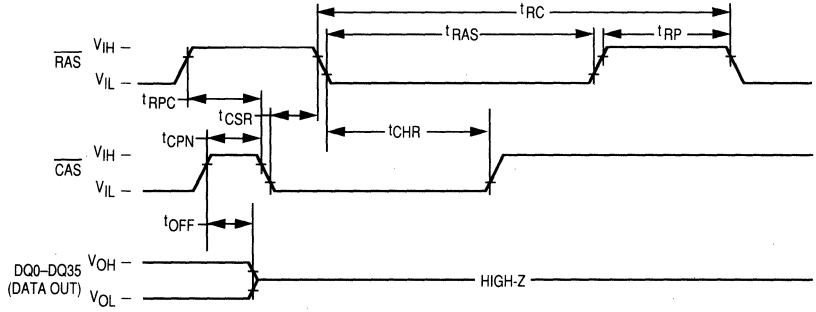


3

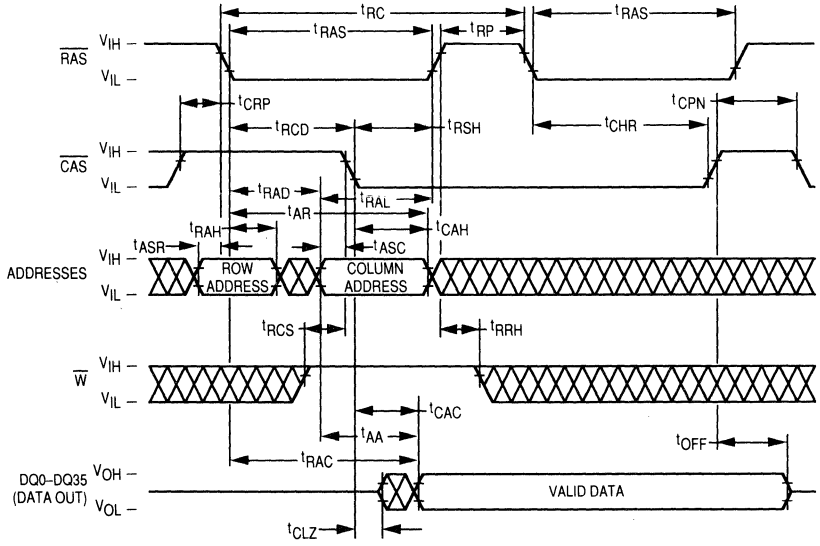
$\overline{RAS}$ ONLY REFRESH CYCLE
($\overline{W}$ and A9 are Don't Care)



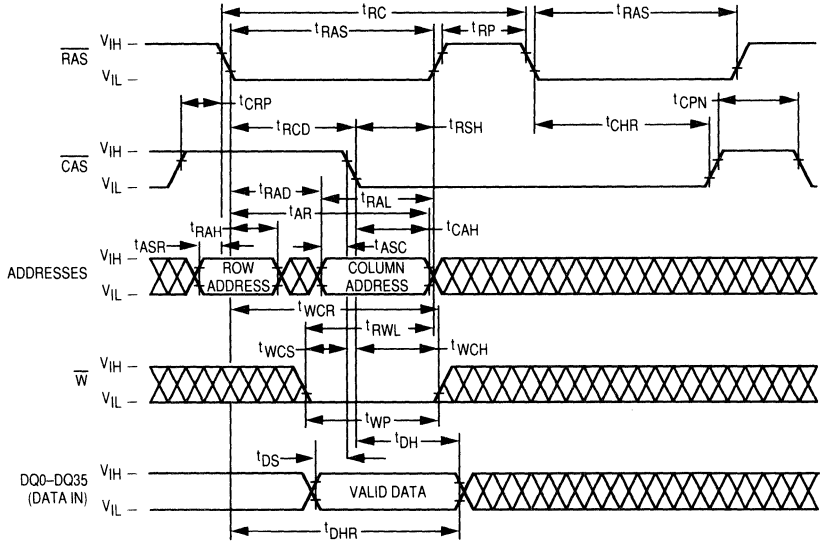
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE
($\overline{W}$ and A0 to A9 are Don't Care)



HIDDEN REFRESH CYCLE (READ)

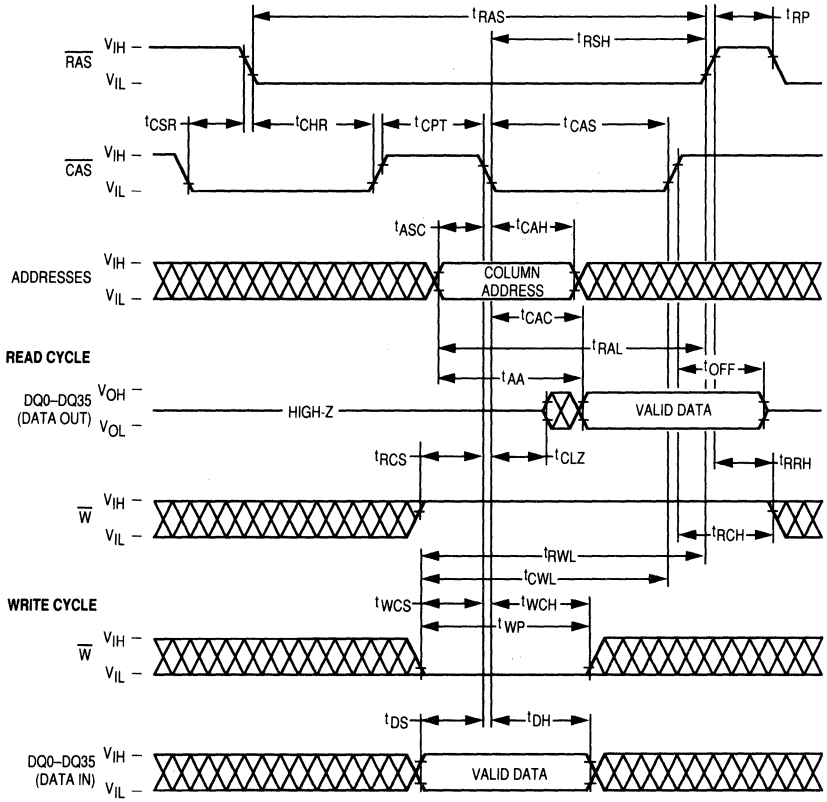


HIDDEN REFRESH CYCLE (WRITE)



3

CAS BEFORE RAS REFRESH COUNTER TEST CYCLE



DEVICE INITIALIZATION

On power-up an initial pause of 200 microseconds is required for the internal substate generator pump to establish the correct bias voltage. This is to be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize the various dynamic nodes internal to the module. During an extended inactive state of the device (greater than 4 milliseconds with device powered up), the wake up sequence (8 active cycles) will be necessary to assure proper device operation.

ADDRESSING THE RAM

The ten address bus pins on the device are time multiplexed with two separate 10-bit address fields that are strobed at the beginning of the memory cycle by two clocks (active negative) called the row address strobe ($\overline{RAS}$) and the column address strobe ($\overline{CAS}$). A total of twenty address bits will decode one of the 524,288 word locations in the device. The column address strobe follows the row address strobe by a specified minimum and maxium time called t_{RCD}, which is the row to column strobe delay. This time interval is also referred to as the multiplex window which gives flexibility to a system designer to set up the external addresses into the RAM. These conditions have to be met for normal read or write cycles. This initial portion of the cycle accomplishes the normal addressing of the device. These are, however, two other variations in addressing the module, one is called the $\overline{RAS}$ only refresh cycle (described later) where a 9-bit row address field is presented on the input pins and latched by the $\overline{RAS}$ clock. The most significant bit on Row Address A9 is not required for refresh. The other variation, which is called page mode, allows the user to column access all words within a selected row. (See **PAGE-MODE CYCLES** section.)

READ CYCLE

A read cycle is referred to as a normal read cycle to differentiate it from a page mode read cycle, which is covered in a later section.

The memory read cycle begins with the row addresses valid and the $\overline{RAS}$ clock transitioning from V_{IH} to the V_{IL} level. The $\overline{CAS}$ clock must also make a transition from V_{IH} to the V_{IL} level at the specified t_{RCD} timing limits when the column addresses are latched. Both the $\overline{RAS}$ and $\overline{CAS}$ clocks trigger a sequence of events which are controlled by several delayed internal clocks. Also, these clocks are linked in such a manner that the access time of the device is independent of the address multiplex window. The only stipulation is that the $\overline{CAS}$ clock must be active before or at the t_{RCD} maximum specification for an access (data valid) from the $\overline{RAS}$ clock edge to be guaranteed (t_{RAC}). If the t_{RCD} maximum condition is not met, the access (t_{CAC}) from the $\overline{CAS}$ clock active transition will determine read access time. The external $\overline{CAS}$ signal is ignored until an internal $\overline{RAS}$ signal is available. This gating feature on the $\overline{CAS}$ clock will allow the external $\overline{CAS}$ signal to become active as soon as the row address hold time (t_{RAH}) specification has been met and defines the t_{RCD} minimum specification. The time difference between t_{RCD} minimum and t_{RCD} maximum can be used to absorb skew delays in switching the address bus from the row to column addresses and in generating the $\overline{CAS}$ clock.

Once the clocks have become active, they must stay active for the minimum (t_{RAS}) period for the $\overline{RAS}$ clock and the minimum (t_{CAS}) period for the $\overline{CAS}$ clock. The $\overline{RAS}$ clock must stay inactive for the minimum (t_{RP}) time. The former is for the completion of the cycle in progress, and the latter is for the device internal circuitry to be precharged for the next active cycle.

Data out is not latched and is valid as long as the $\overline{CAS}$ clock is active; the output will switch to the three-state mode when the $\overline{CAS}$ clock goes inactive. To perform a read cycle, the write ($\overline{W}$) input must be held at the V_{IH} level from the time the $\overline{CAS}$ clock makes its active transition (t_{RCS}) to the time when it transitions into the inactive (t_{RCH}) mode.

WRITE CYCLE

A write cycle is similar to a read cycle except that the write ($\overline{W}$) clock must go active (V_{IL} level) at or before the $\overline{CAS}$ clock goes active at a minimum t_{WCS} time. If the above condition is met, then the cycle in progress is referred to as an early write cycle. In an early write cycle, the write clock and the data in are referenced to the active transition of the $\overline{CAS}$ clock edge. There are two important parameters with respect to the write cycle: the column strobe to write lead time (t_{CWL}) and the row strobe to write lead time (t_{RWL}). These define the minimum time that $\overline{RAS}$ and $\overline{CAS}$ clocks need to be active after the write operation has started ($\overline{W}$ clock at V_{IL} level).

PAGE-MODE CYCLES

Page mode operation allows fast successive data operations at all 1024 column locations on a selected row. Page access (t_{CAC}) is typically half the regular $\overline{RAS}$ clock access (t_{RAC}) on the Motorola 1M dynamic RAM. Page mode operation consists of holding the $\overline{RAS}$ clock active while cycling the $\overline{CAS}$ clock to access the column locations determined by the 10-bit column address field.

The page cycle is always initiated with a row address being provided and latched by the $\overline{RAS}$ clock, followed by the column address and $\overline{CAS}$ clock. From the timing illustrated, the initial cycle is a normal read or write cycle, that has been previously described, followed by the shorter $\overline{CAS}$ cycles (t_{PC}). The $\overline{CAS}$ cycle time (t_{PC}) consists of the $\overline{CAS}$ clock active time (t_{CAS}), and $\overline{CAS}$ clock precharge time (t_{CP}) and two transitions. In practice, any combination of read and write cycles can be performed to suit a particular application.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Therefore, to retain the correct information, the module needs to be refreshed at least once every 16 milliseconds. This is accomplished by sequentially cycling through the 1024 row address locations every 16 milliseconds (i.e., at least one row every 15.6 microseconds). A normal read or write operation to the module will also refresh all the words associated with the particular row(s) decoded.

$\overline{RAS}$-Only Refresh

In this refresh method, the system must perform a $\overline{RAS}$-only cycle on 1024 row addresses every 16 milliseconds. The row addresses are latched in with the $\overline{RAS}$ clock, and the associated internal row locations are refreshed. As the heading implies, the $\overline{CAS}$ clock is not required and must be inactive or at a V_{IH} level.

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CAS Before RAS Refresh

This refresh cycle is initiated when RAS falls, after CAS has been low (by t_{CSR}). This activates the internal refresh counter which generates the row address to be refreshed. Externally applied addresses are ignored during the automatic refresh cycle. If the output buffer was off before the automatic refresh cycle, the output will stay in the high impedance state. If the output was enabled by CAS in the previous cycle, the data out will be maintained during the automatic refresh cycle as long as CAS is held active (hidden refresh).

Hidden Refresh

The hidden refresh method allows refresh cycles to be performed while maintaining valid data at the output pin. Hidden refresh is performed by holding CAS at V_{IL} and taking RAS high and after a specified precharge period (t_{RP}), executing a CAS before RAS refresh cycle. (See Figure 1.)

CAS BEFORE RAS REFRESH COUNTER TEST

The internal refresh counter of the device can be tested with a **CAS before RAS refresh counter test**. This refresh counter test is performed with read and write operations. During this test, the internal refresh counter generates the row address, while the external address input supplies the column address. The entire array is refreshed after 1024 test cycles, as indicated by the check data written in each row. See **CAS before RAS refresh counter test cycle** timing diagram.

The test can be performed only after a minimum of **8 CAS before RAS** initialization cycles. The test procedure is as follows:

1. Write "0"s into all memory cells (normal write mode).
2. Select a column address, and read "0" out of the cell by performing **CAS before RAS refresh counter test, read cycle**. Repeat this operation 1024 times.
3. Select a column address, and write "1" into the cell by performing **CAS before RAS refresh counter test, write cycle**. Repeat this operation 1024 times.
4. Read "1"s (normal read mode), which were written at step 3.
5. Repeat steps 1 to 4 using complement data.

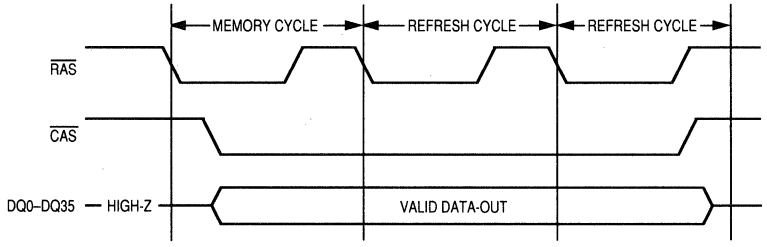
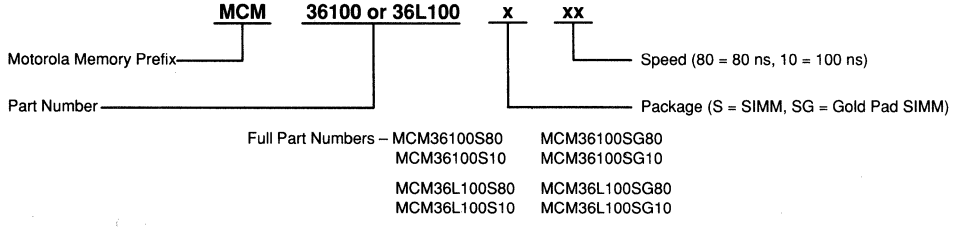


Figure 1. Hidden Refresh Cycle

ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers – MCM36100S80 MCM36100SG80
MCM36100S10 MCM36100SG10

MCM36L100S80 MCM36L100SG80
MCM36L100S10 MCM36L100SG10

NOTE: Contact your Motorola representative for further information on the Gold Pad SIMM packages.

MCM36200
MCM36L200

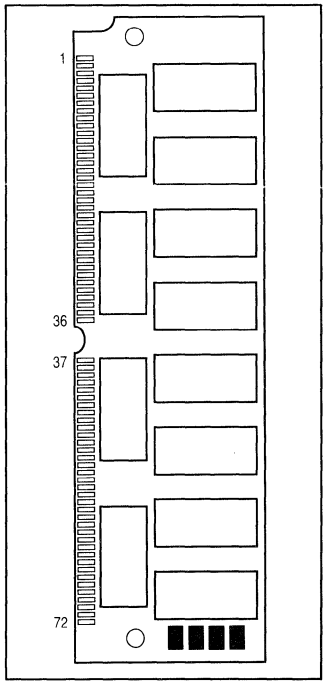
3

Product Preview

2M × 36 Bit Dynamic Random Access Memory Module

The MCM36200S is a 72M, dynamic random access memory (DRAM) module organized as 2,097,152 × 36 bits. The module is a double-sided 72-lead single-in-line memory module (SIMM) consisting of eight MCM514400 DRAMs housed in standard 350-mil-wide SOJ packages and four CMOS 1M × 1 DRAMs housed in 20/26 lead SOJ packages, mounted on a substrate along with a 0.22 µF (min) decoupling capacitor mounted under each DRAM. The MCM514400 is a CMOS high speed, dynamic random access memory organized as 1,048,576 four-bit words and fabricated with CMOS silicon-gate process technology.

- Three-State Data Output
- Early-Write Common I/O Capability
- Fast Page Mode Capability
- TTL-Compatible Inputs and Outputs
- $\overline{RAS}$ Only Refresh
- $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- Hidden Refresh
- 1024 Cycle Refresh:
  MCM36200S = 16 ms (Max)
  MCM36L200S = 128 ms (Max)
- Consists of Sixteen 1M × 4 DRAMs, Eight 1M × 1 DRAMs, and Twenty Four 0.22 µF (Min) Decoupling Capacitors
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}):
  MCM36200S-80 = 80 ns (Max)
  MCM36200S-10 = 100 ns (Max)
- Low Active Power Dissipation:
  MCM36200S-80 = 6.30 W (Max)
  MCM36200S-10 = 5.41 W (Max)
- Low Standby Power Dissipation:
  TTL Levels = 264 mW (Max)
  CMOS Levels = 132 mW (Max, MCM36200S)
  CMOS Levels = 44 mW (Max, MCM36L200S)



PIN NAMES

A0–A9	Address Inputs
DQ0–DQ35	Data Input/Output
$\overline{CAS0}$–$\overline{CAS3}$	Column Address Strobe
PD1–PD4	Presence Detect
$\overline{RAS0}$–$\overline{RAS3}$	Row Address Strobe
$\overline{W}$	Read/Write Input
V_{CC}	Power (+ 5 V)
V_{SS}	Ground
NC	No Connection

All power supply and ground pins must be connected for proper operation of the device.

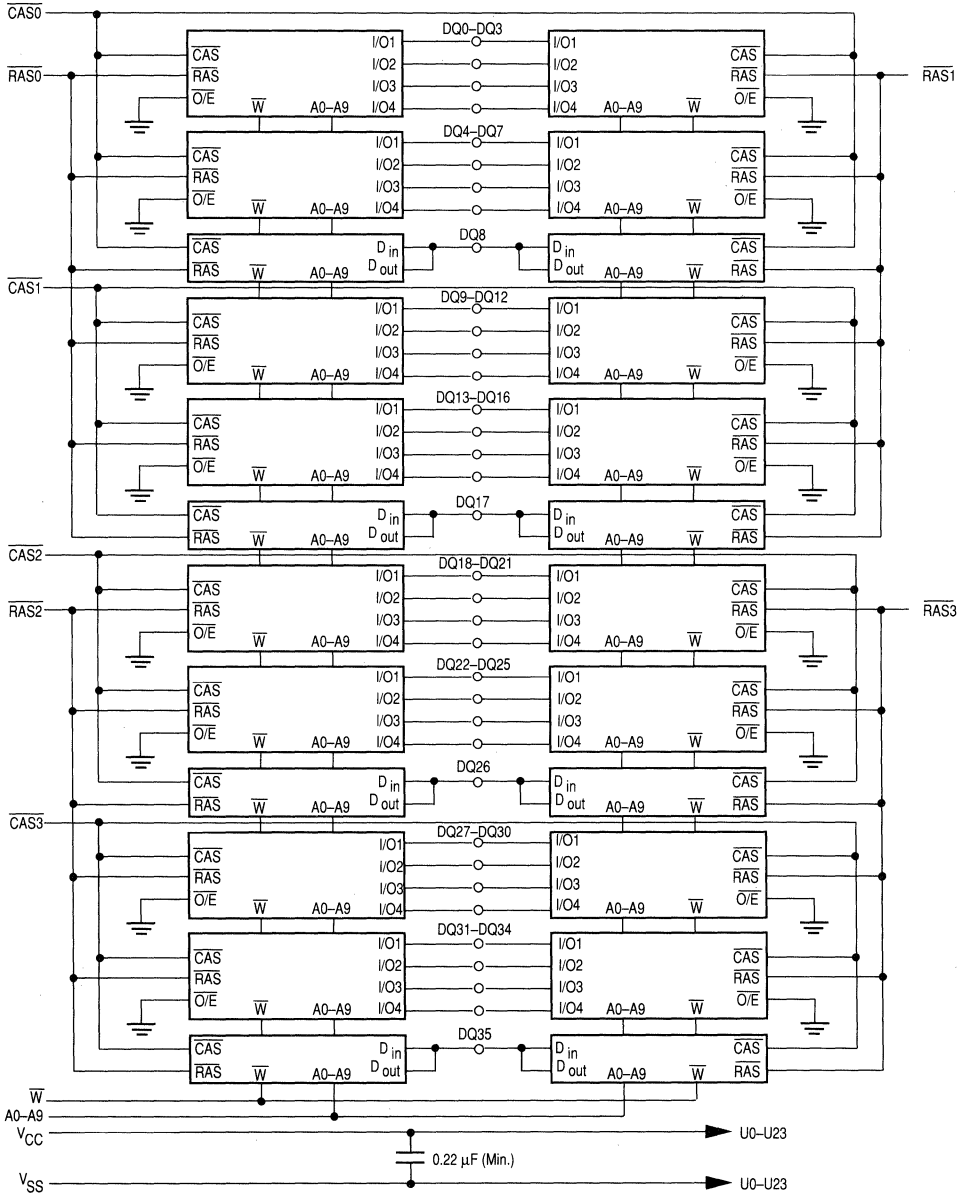
PIN OUT

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V_{SS}	13	A1	25	DQ24	37	DQ17	49	DQ9	61	DQ14
2	DQ0	14	A2	26	DQ7	38	DQ35	50	DQ27	62	DQ33
3	DQ18	15	A3	27	DQ25	39	V_{SS}	51	DQ10	63	DQ15
4	DQ1	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ28	64	DQ34
5	DQ19	17	A5	29	NC	41	$\overline{CAS2}$	53	DQ11	65	DQ16
6	DQ2	18	A6	30	V_{CC}	42	$\overline{CAS3}$	54	DQ29	66	NC
7	DQ20	19	NC	31	A8	43	$\overline{CAS1}$	55	DQ12	67	PD1
8	DQ3	20	DQ4	32	A9	44	$\overline{RAS0}$	56	DQ30	68	PD2
9	DQ21	21	DQ22	33	$\overline{RAS3}$	45	$\overline{RAS1}$	57	DQ13	69	PD3
10	V_{CC}	22	DQ5	34	$\overline{RAS2}$	46	NC	58	DQ31	70	PD4
11	NC	23	DQ23	35	DQ26	47	$\overline{W}$	59	V_{CC}	71	NC
12	A0	24	DQ6	36	DQ8	48	NC	60	DQ32	72	V_{SS}

This document contains information on a new product. Specifications and information herein are subject to change without notice.

3

BLOCK DIAGRAM



PRESENCE DETECT PIN OUT			
Pin Name	**70 ns**	**80 ns**	**100 ns**
PD1	NC	NC	NC
PD2	NC	NC	NC
PD3	V_{SS}	NC	V_{SS}
PD4	NC	V_{SS}	V_{SS}

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 1 to + 7	V
Voltage Relative to V_{SS} (For Any Pin Except V_{CC})	V_{in}, V_{out}	– 1 to + 7	V
Data Output Current per DQ Pin	I_{out}	50	mA
Power Dissipation	P_D	8.58	W
Operating Temperature Range	T_A	0 to + 70	°C
Storage Temperature Range	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high impedence circuits.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V	1
	V_{SS}	0	0	0		
Logic High Voltage, All Inputs	V_{IH}	2.4	—	6.5	V	1
Logic Low Voltage, All Inputs	V_{IL}	– 1.0	—	0.8	v	1

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current MCM36200-80, t_{RC} = 150 ns MCM36200-10, t_{RC} = 180 ns	I_{CC1}	 — —	 1144 984	mA	2
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	—	48	mA	
V_{CC} Power Supply Current During $\overline{RAS}$ only Refresh Cycles MCM36200-80, t_{RC} = 150 ns MCM36200-10, t_{RC} = 180 ns	I_{CC3}	 — —	 1144 984	mA	2
V_{CC} Power Supply Current During Fast Page Mode Cycle MCM36200-80, t_{RC} = 150 ns MCM36200-10, t_{RC} = 180 ns	I_{CC4}	 — —	 624 504	mA	2
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V) MCM36200 MCM36L200	I_{CC5}	— —	24 4.8	mA	
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle MCM36200-80, t_{RC} = 150 ns MCM36200-10, t_{RC} = 180 ns	I_{CC6}	 — —	 1144 984	mA	2
Input Leakage Current ($V_{SS} \le V_{in} \le V_{CC}$)	$I_{lkg(I)}$	– 240	240	µA	
Output Leakage Current ($\overline{CAS}$ at Logic 1, $V_{SS} \le V_{out} \le V_{CC}$)	$I_{lkg(O)}$	– 20	20	µA	
Output High Voltage (I_{OH} = – 5 mA)	V_{OH}	2.4	—	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	—	0.4	V	

NOTES:
1. All voltages referenced to V_{SS}.
2. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Max	Unit	Notes
Input Capacitance (A0–A9)	C_{I1}	—	161	pF	1
Input Capacitance ($\overline{W}$)	C_{I2}	—	178	pF	1
Input Capacitance ($\overline{RAS0}$–$\overline{RAS2}$)	C_{I3}	—	52	pF	1
Input Capacitance ($\overline{CAS0}$–$\overline{CAS3}$)	C_{I4}	—	52	pF	1
I/O Capacitance (DQ0–DQ7, DQ9–DQ16, DQ18–DQ25, DQ27–DQ34)	C_{DQ1}	—	29	pF	1
I/O Capacitance (DQ8, DQ17, DQ26, DQ35)	C_{DQ2}	—	39	pF	1

NOTE:
1. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = 1\ \Delta\ t / \Delta\ V$.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ AND WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM36200-80		MCM36200-10		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	150	—	180	—	ns	5
Page Mode Cycle Time	t_{CELCEL}	t_{PC}	50	—	60	—	ns	
Access Time from $\overline{RAS}$	t_{RELQV}	t_{RAC}	—	80	—	100	ns	6, 7
Access Time from $\overline{CAS}$	t_{CELQV}	t_{CAC}	—	20	—	25	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	—	40	—	50	ns	6, 9
Access Time from Precharge $\overline{CAS}$	t_{CEHQV}	t_{CPA}	—	45	—	55	ns	6
$\overline{CAS}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	0	—	0	—	ns	6
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	20	0	20	ns	10
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{REHREL}	t_{RP}	60	—	70	—	ns	
$\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RAS}	80	10,000	100	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	80	100,000	100	100,000	ns	
$\overline{RAS}$ Hold Time	t_{CELREH}	t_{RSH}	25	—	25	—	ns	
$\overline{CAS}$ Hold TIme	t_{RELCEH}	t_{CSH}	80	—	100	—	ns	
$\overline{CAS}$ Pulse Width	t_{CELCEH}	t_{CAS}	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RELCEL}	t_{RCD}	20	60	25	75	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	40	20	50	ns	12

(continued)

NOTES:
1. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
6. Measured with a current load equivalent to 2 TTL (– 200 µA, + 4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
8. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
9. Assumes that $t_{RAD} \geq t_{RAD}$ (max).
10. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively to t_{CAC}.
12. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.

READ AND WRITE CYCLES (Continued)

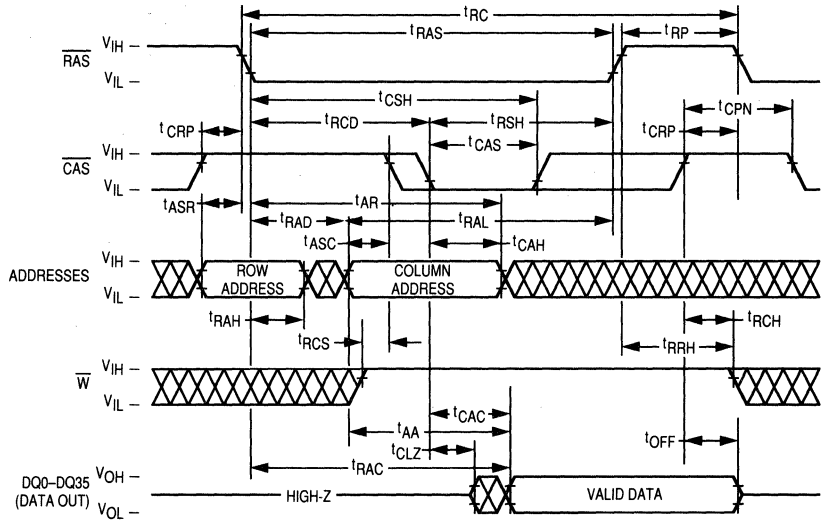
Parameter	Symbol		MCM36200		MCM36L200		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	—	10	—	ns	
$\overline{CAS}$ Precharge Time (Page Mode Cyle Only)	t_{CEHCEL}	t_{CP}	10	—	10	—	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	—	15	—	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	—	20	—	ns	
Column Address Hold Time Referenced to $\overline{RAS}$	t_{RELAX}	t_{AR}	60	—	75	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{AVREH}	t_{RAL}	40	—	50	—	ns	
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	0	—	ns	
Read Command Hold Time Referenced to $\overline{CAS}$	t_{CEHWX}	t_{RCH}	0	—	0	—	ns	13
Read Command Hold Time Referenced to $\overline{RAS}$	t_{REHWX}	t_{RRH}	0	—	0	—	ns	13
Write Command Hold Time Referenced to $\overline{CAS}$	t_{CELWH}	t_{WCH}	15	—	20	—	ns	
Write Command Hold Time Referenced to $\overline{RAS}$	t_{RELWH}	t_{WCR}	60	—	75	—	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	15	—	20	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{WLREH}	t_{RWL}	20	—	25	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{WLCEH}	t_{CWL}	20	—	25	—	ns	
Data in Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	ns	14, 15
Data in Hold Time	t_{CELDX}	t_{DH}	15	—	20	—	ns	14, 15
Data in Hold Time Referenced to $\overline{RAS}$	t_{RELDX}	t_{DHR}	60	—	75	—	ns	
Refresh Period MCM36200 MCM36L200	t_{RVRV}	t_{RFSH}	— —	16 128	— —	16 128	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	—	0	—	ns	15, 16
$\overline{CAS}$ Setup Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEL}	t_{CSR}	10	—	10	—	ns	
$\overline{CAS}$ Hold Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEH}	t_{CHR}	30	—	30	—	ns	
$\overline{CAS}$ Precharge to $\overline{CAS}$ Active Time	t_{REHCEL}	t_{RPC}	0	—	0	—	ns	
$\overline{CAS}$ Precharge Time for $\overline{CAS}$ Before $\overline{RAS}$ Counter Test	t_{CEHCEL}	t_{CPT}	40	—	50	—	ns	
$\overline{CAS}$ Precharge Time	t_{CEHCEL}	t_{CPN}	10	—	15	—	ns	

NOTES:

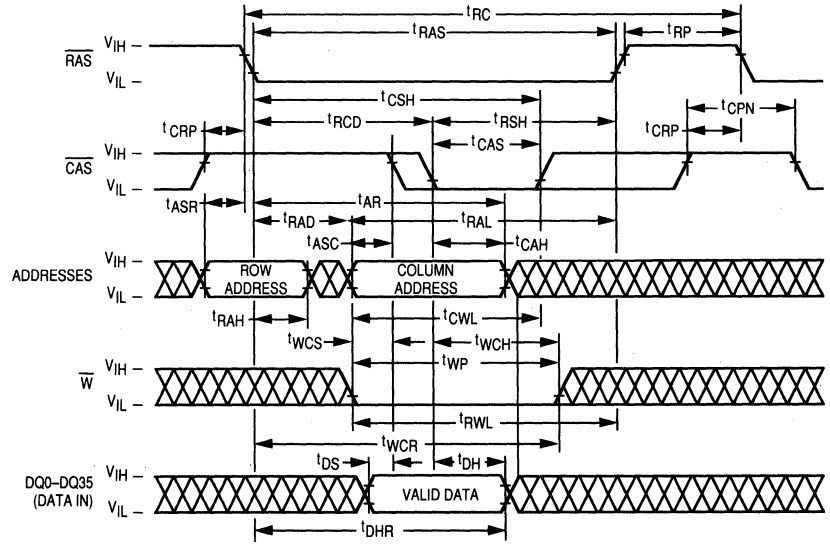
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles.
15. Early write only ($t_{WCS} \geq t_{WCS}$ (min)).
16. t_{WCS} is not a restrictive operating parameter. It is included in the data sheet as an electrical characteristic only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle. If this condition is not satisifed, the condition of the data out (at access time) is indeterminate.
17. To avoid bus contention and potential damage to the module, $\overline{RAS0}$ and $\overline{RAS1}$ may not be active low simultaneously. Similarly, $\overline{RAS2}$ and $\overline{RAS3}$ may not be simultaneously active low.

3

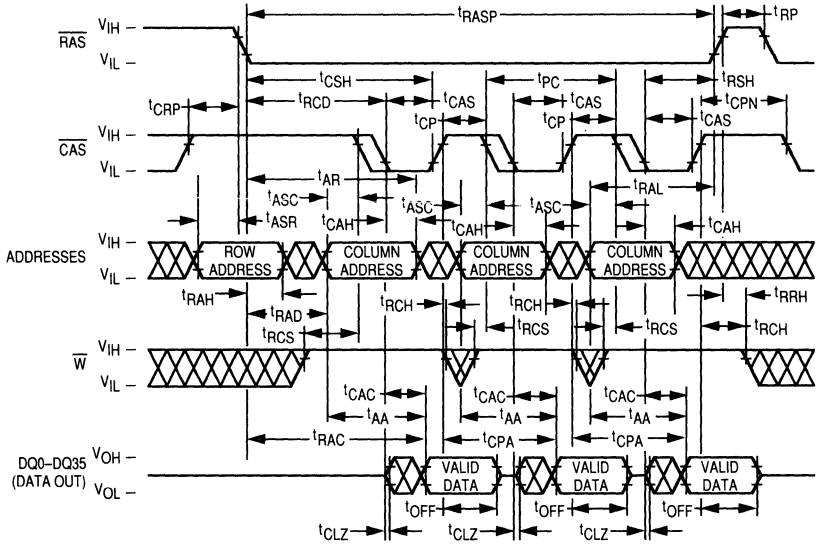
READ CYCLE



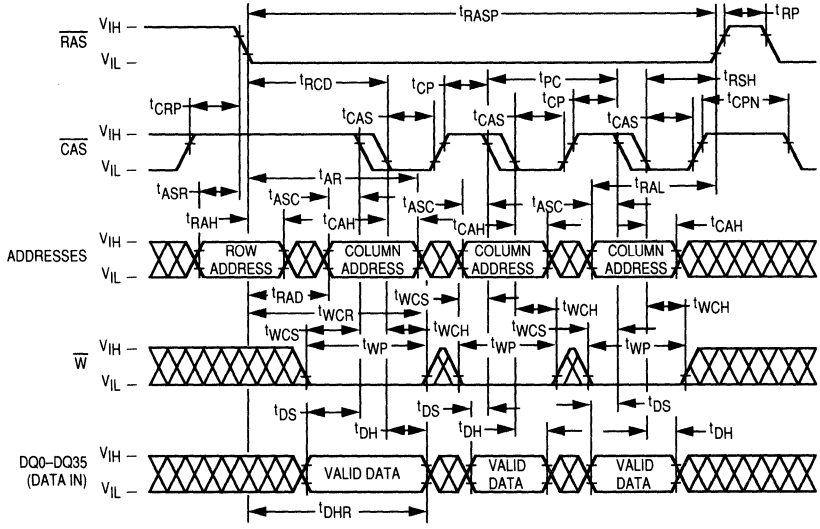
EARLY WRITE CYCLE



FAST PAGE MODE READ CYCLE

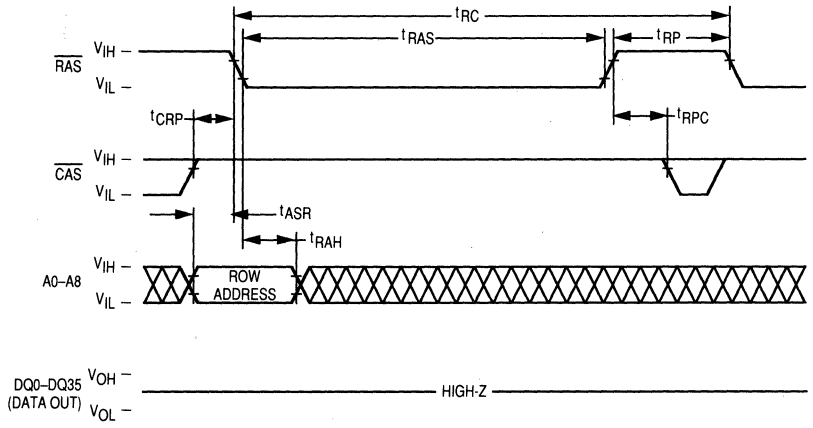


FAST PAGE MODE WRITE CYCLE (EARLY WRITE)

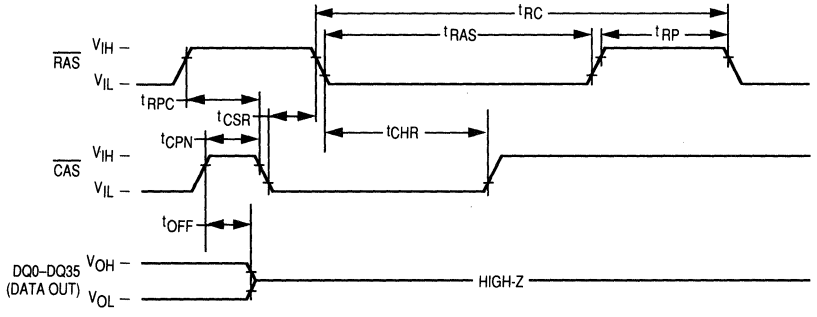


3

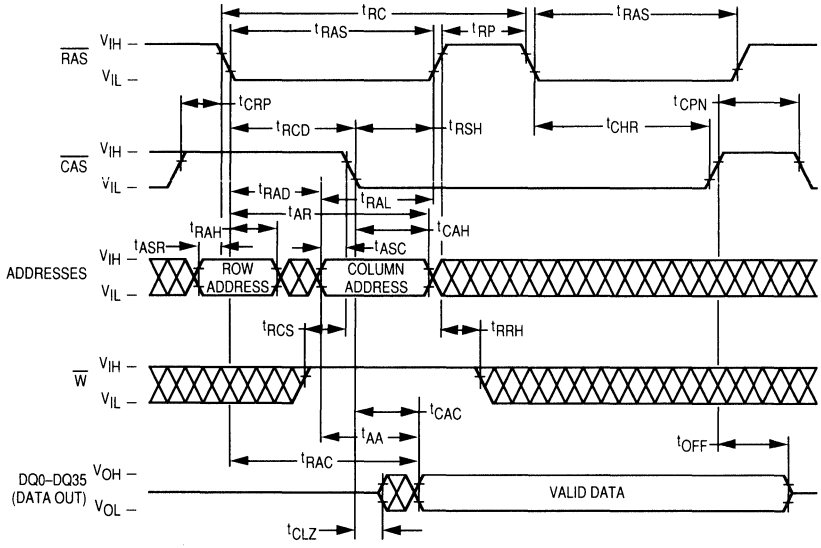
$\overline{RAS}$ ONLY REFRESH CYCLE
($\overline{W}$ and A9 are Don't Care)



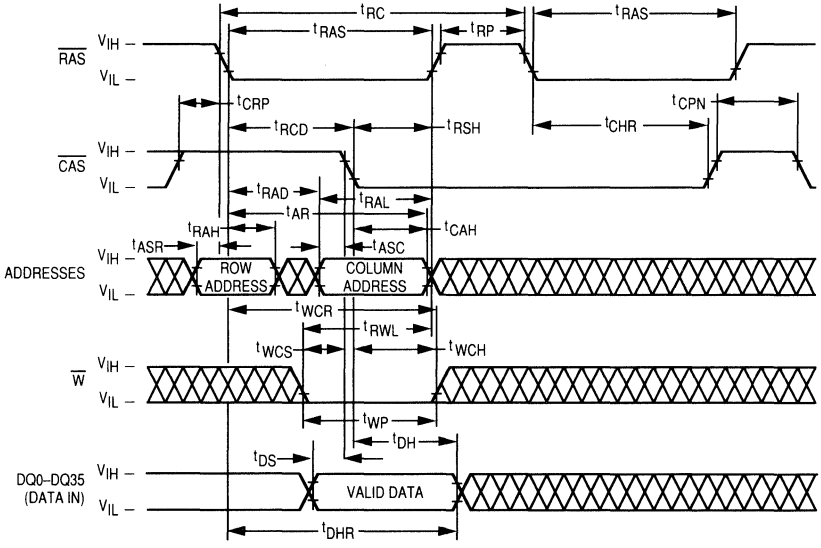
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE
($\overline{W}$ and A0 to A9 are Don't Care)



HIDDEN REFRESH CYCLE (READ)

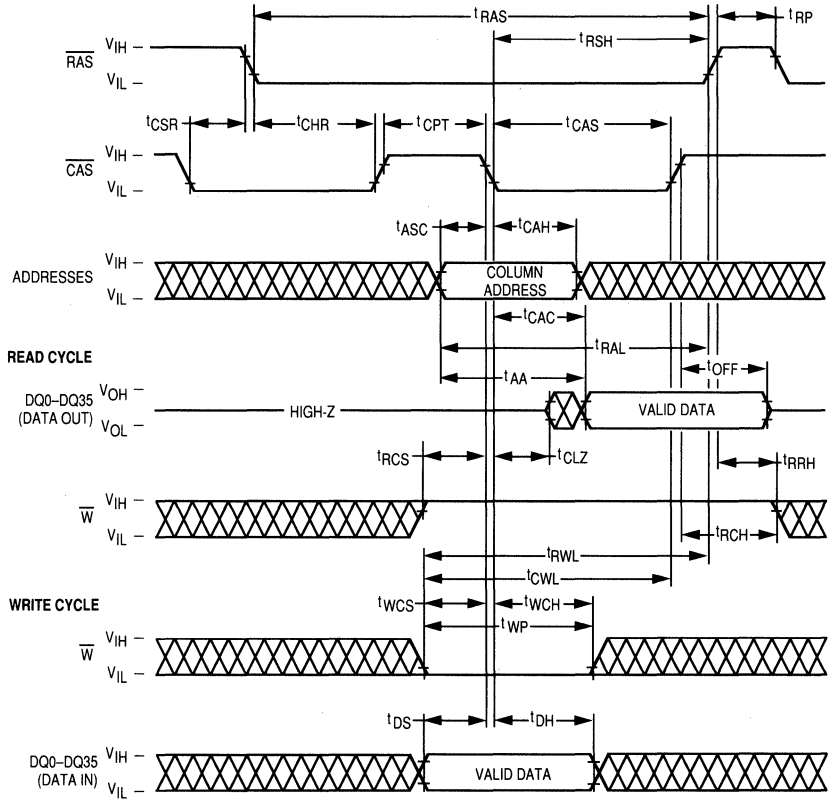


HIDDEN REFRESH CYCLE (WRITE)



3

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



DEVICE INITIALIZATION

On power-up an initial pause of 200 microseconds is required for the internal substate generator pump to establish the correct bias voltage. This is to be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize the various dynamic nodes internal to the module. During an extended inactive state of the module (greater than 4 milliseconds with device powered up), the wake up sequence (8 active cycles) will be necessary to assure proper device operation.

ADDRESSING THE RAM

The ten address bus pins on the device are time multiplexed with two separate 10-bit address fields that are strobed at the beginning of the memory cycle by two clocks (active negative) called the row address strobe ($\overline{RAS}$) and the column address strobe ($\overline{CAS}$). A total of twenty address bits will decode one of the 2,097,152 word locations in the module. The column address strobe follows the row address strobe by a specified minimum and maxium time called t_{RCD}, which is the row to column strobe delay. This time interval is also referred to as the multiplex window which gives flexibility to a system designer to set up the external addresses into the RAM. These conditions have to be met for normal read or write cycles. This initial portion of the cycle accomplishes the normal addressing of the device. These are, however, two other variations in addressing the module, one is called the $\overline{RAS}$ only refresh cycle (described later) where a 9-bit row address field is presented on the input pins and latched by the $\overline{RAS}$ clock. The most significant bit on Row Address A9 is not required for refresh. The other variation, which is called page mode, allows the user to column access all words within a selected row. (See **PAGE-MODE CYCLES** section).

READ CYCLE

A read cycle is referred to as a normal read cycle to differentiate it from a page mode read cycle, which is covered in a later section.

The memory read cycle begins with the row addresses valid and the $\overline{RAS}$ clock transitioning from V_{IH} to the V_{IL} level. The $\overline{CAS}$ clock must also make a transition from V_{IH} to the V_{IL} level at the specified t_{RCD} timing limits when the column addresses are latched. Both the $\overline{RAS}$ and $\overline{CAS}$ clocks trigger a sequence of events which are controlled by several delayed internal clocks. Also, these clocks are linked in such a manner that the access time of the device is independent of the address multiplex window. The only stipulation is that the $\overline{CAS}$ clock must be active before or at the t_{RCD} maximum specification for an access (data valid) from the $\overline{RAS}$ clock edge to be guaranteed (t_{RAC}). If the t_{RCD} maximum condition is not met, the access (t_{CAC}) from the $\overline{CAS}$ clock active transition will determine read access time. The external $\overline{CAS}$ signal is ignored until an internal $\overline{RAS}$ signal is available. This gating feature on the $\overline{CAS}$ clock will allow the external $\overline{CAS}$ signal to become active as soon as the row address hold time (t_{RAH}) specification has been met and defines the t_{RCD} minimum specification. The time difference between t_{RCD} minimum and t_{RCD} maximum can be used to absorb skew delays in switching the address bus from the row to column addresses and in generating the $\overline{CAS}$ clock.

Once the clocks have become active, they must stay active for the minimum (t_{RAS}) period for the $\overline{RAS}$ clock and the minimum (t_{CAS}) period for the $\overline{CAS}$ clock. The $\overline{RAS}$ clock must stay inactive for the minimum (t_{RP}) time. The former is for the completion of the cycle in progress, and the latter is for the device internal circuitry to be precharged for the next active cycle.

Data out is not latched and is valid as long as the $\overline{CAS}$ clock is active; the output will switch to the three-state mode when the $\overline{CAS}$ clock goes inactive. To perform a read cycle, the write ($\overline{W}$) input must be held at the V_{IH} level from the time the $\overline{CAS}$ clock makes its active transition (t_{RCS}) to the time when it transitions into the inactive (t_{RCH}) mode.

WRITE CYCLE

A write cycle is similar to a read cycle except that the write ($\overline{W}$) clock must go active (V_{IL} level) at or before the $\overline{CAS}$ clock goes active at a minimum t_{WCS} time. If the above condition is met, then the cycle in progress is referred to as an early write cycle. In an early write cycle, the write clock and the data in are referenced to the active transition of the $\overline{CAS}$ clock edge. There are two important parameters with respect to the write cycle: the column strobe to write lead time (t_{CWL}) and the row strobe to write lead time (t_{RWL}). These define the minimum time that $\overline{RAS}$ and $\overline{CAS}$ clocks need to be active after the write operation has started ($\overline{W}$ clock at V_{IL} level).

PAGE-MODE CYCLES

Page mode operation allows fast successive data operations at all 1024 column locations on a selected row. Page access (t_{CAC}) is typically half the regular $\overline{RAS}$ clock access (t_{RAC}) on the Motorola 1M dynamic RAM. Page mode operation consists of holding the $\overline{RAS}$ clock active while cycling the $\overline{CAS}$ clock to access the column locations determined by the 10-bit column address field.

The page cycle is always initiated with a row address being provided and latched by the $\overline{RAS}$ clock, followed by the column address and $\overline{CAS}$ clock. From the timing illustrated, the initial cycle is a normal read or write cycle, that has been previously described, followed by the shorter $\overline{CAS}$ cycles (t_{PC}). The $\overline{CAS}$ cycle time (t_{PC}) consists of the $\overline{CAS}$ clock active time (t_{CAS}), and $\overline{CAS}$ clock precharge time (t_{CP}) and two transitions. In practice, any combination of read and write cycles can be performed to suit a particular application.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Therefore, to retain the correct information, the module needs to be refreshed at least once every 16 milliseconds. This is accomplished by sequentially cycling through the 1024 row address locations every 16 milliseconds (i.e., at least one row every 15.6 microseconds). A normal read or write operation to the module will also refresh all the words associated with the particular row(s) decoded.

$\overline{RAS}$-Only Refresh

In this refresh method, the system must perform a $\overline{RAS}$-only cycle on 1024 row addresses every 16 milliseconds. The row addresses are latched in with the $\overline{RAS}$ clock, and the associated internal row locations are refreshed. As the heading implies, the $\overline{CAS}$ clock is not required and must be inactive or at a V_{IH} level.

3

CAS Before RAS Refresh

This refresh cycle is initiated when RAS falls, after CAS has been low (by t_{CSR}). This activates the internal refresh counter which generates the row address to be refreshed. Externally applied addresses are ignored during the automatic refresh cycle. If the output buffer was off before the automatic refresh cycle, the output will stay in the high impedance state. If the output was enabled by CAS in the previous cycle, the data out will be maintained during the automatic refresh cycle as long as CAS is held active (hidden refresh).

Hidden Refresh

The hidden refresh method allows refresh cycles to be performed while maintaining valid data at the output pin. Hidden refresh is performed by holding CAS at V_{IL} and taking RAS high and after a specified precharge period (t_{RP}), executing a CAS before RAS refresh cycle. (See Figure 1.)

CAS BEFORE RAS REFRESH COUNTER TEST

The internal refresh counter of the device can be tested with a **CAS before RAS refresh counter test**. This refresh counter test is performed with read and write operations. During this test, the internal refresh counter generates the row address, while the external address input supplies the column address. The entire array is refreshed after 1024 test cycles, as indicated by the check data written in each row. See **CAS before RAS refresh counter test cycle** timing diagram.

The test can be performed only after a minimum of **8 CAS before RAS** initialization cycles. The test procedure is as follows:

1. Write "0"s into all memory cells (normal write mode).
2. Select a column address, and read "0" out of the cell by performing **CAS before RAS refresh counter test, read cycle**. Repeat this operation 1024 times.
3. Select a column address, and write "1" into the cell by performing **CAS before RAS refresh counter test, write cycle**. Repeat this operation 1024 times.
4. Read "1"s (normal read mode), which were written at step 3.
5. Repeat steps 1 to 4 using complement data.

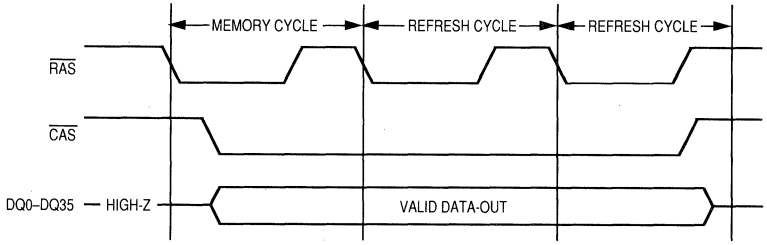


Figure 1. Hidden Refresh Cycle

ORDERING INFORMATION
(Order by Full Part Number)

MCM **36200 or 36L200** **x** **xx**

Motorola Memory Prefix

Part Number

Speed (80 = 80 ns, 10 = 100 ns)

Package (S = SIMM, SG = Gold Pad SIMM)

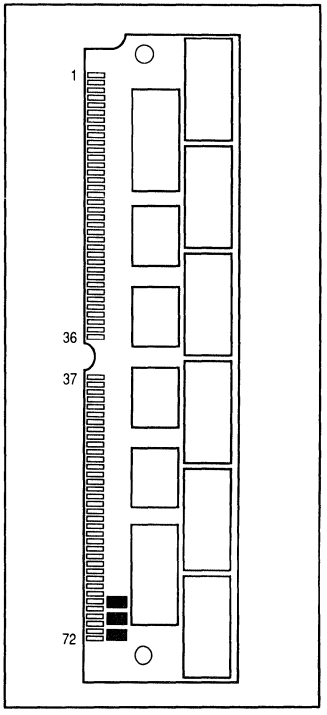
Full Part Numbers –		
	MCM36200S70	MCM36200SG70
	MCM36200S80	MCM36200SG80
	MCM36200S10	MCM36200SG10
	MCM36L200S70	MCM36L200SG70
	MCM36L200S80	MCM36L200SG80
	MCM36L200S10	MCM36L200SG10

NOTE: Contact your Motorola representative for further information on the Gold Pad SIMM packages.

MCM36256

Advance Information

256K × 36 Bit Dynamic Random Access Memory Module



The MCM36256S is a 9M, dynamic random access memory (DRAM) module organized as 262,144 × 36 bits. The module is a 72-lead single-in-line memory module (SIMM) consisting of eight MCM514256A DRAMs housed in 20/26 J-lead small outline packages (SOJ) and four CMOS 256K × 1 DRAMs housed in 18-lead PLCC packages, mounted on a substrate along with a 0.22 µF (min) decoupling capacitor mounted under each DRAM. The MCM514256A is a 1.0 µ CMOS high speed, dynamic random access memory organized as 262,144 four-bit words and fabricated with CMOS silicon-gate process technology.

- Three-State Data Output
- Early-Write Common I/O Capability
- Fast Page Mode Capability
- TTL-Compatible Inputs and Outputs
- $\overline{RAS}$ Only Refresh
- $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- Hidden Refresh
- 512 Cycle Refresh:
  MCM36256 = 8 ms (Max)
- Consists of Eight 256K × 4 DRAMs, Four 256K × 1 DRAMs, and Twelve 0.22 µF (Min) Decoupling Capacitors
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}):
  MCM36256S-70 = 70 ns (Max)
  MCM36256S-80 = 80 ns (Max)
  MCM36256S-10 = 100 ns (Max)
- Low Active Power Dissipation:
  MCM36256S-70 = 5.28 W (Max)
  MCM36256S-80 = 4.62 W (Max)
  MCM36256S-10 = 3.96 W (Max)
- Low Standby Power Dissipation:
  TTL Levels = 132 mW (Max)
  CMOS Levels = 66 mW (Max)

PIN OUT

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V_{SS}	13	A1	25	DQ24	37	DQ17	49	DQ9	61	DQ14
2	DQ0	14	A2	26	DQ7	38	DQ35	50	DQ27	62	DQ33
3	DQ18	15	A3	27	DQ25	39	V_{SS}	51	DQ10	63	DQ15
4	DQ1	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ28	64	DQ34
5	DQ19	17	A5	29	NC	41	$\overline{CAS2}$	53	DQ11	65	DQ16
6	DQ2	18	A6	30	V_{CC}	42	$\overline{CAS3}$	54	DQ29	66	NC
7	DQ20	19	NC	31	A8	43	$\overline{CAS1}$	55	DQ12	67	PD1
8	DQ3	20	DQ4	32	NC	44	$\overline{RAS0}$	56	DQ30	68	PD2
9	DQ21	21	DQ22	33	NC	45	NC	57	DQ13	69	PD3
10	V_{CC}	22	DQ5	34	$\overline{RAS2}$	46	NC	58	DQ31	70	PD4
11	NC	23	DQ23	35	DQ26	47	$\overline{W}$	59	V_{CC}	71	NC
12	A0	24	DQ6	36	DQ8	48	NC	60	DQ32	72	V_{SS}

PIN NAMES

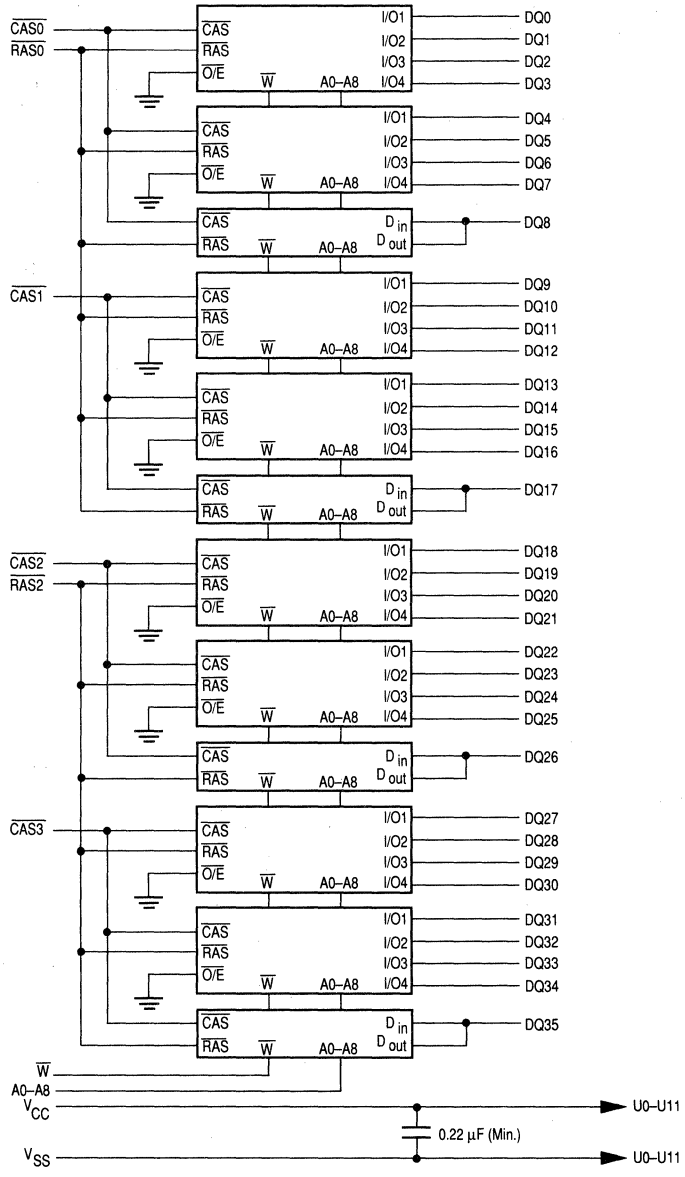
A0–A8	Address Inputs
DQ0–DQ35	Data Input/Output
$\overline{CAS0}$–$\overline{CAS3}$	Column Address Strobe
PD1–PD4	Presence Detect
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{W}$	Read/Write Input
V_{CC}	Power (+ 5 V)
V_{SS}	Ground
NC	No Connection

All power supply and ground pins must be connected for proper operation of the device.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

3

BLOCK DIAGRAM



PRESENCE DETECT PIN OUT			
Pin Name	**70 ns**	**80 ns**	**100 ns**
PD1	V_{SS}	V_{SS}	V_{SS}
PD2	NC	NC	NC
PD3	V_{SS}	NC	V_{SS}
PD4	NC	V_{SS}	V_{SS}

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 1 to + 7	V
Voltage Relative to V_{SS} (For Any Pin Except V_{CC})	V_{in}, V_{out}	– 1 to + 7	V
Data Output Current per DQ Pin	I_{out}	50	mA
Power Dissipation	P_D	7.2	W
Operating Temperature Range	T_A	0 to + 70	°C
Storage Temperature Range	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high impedence circuits.

3

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V	1
	V_{SS}	0	0	0		
Logic High Voltage, All Inputs	V_{IH}	2.4	—	6.5	V	1
Logic Low Voltage, All Inputs	V_{IL}	– 1.0	—	0.8	v	1

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current	I_{CC1}			mA	2
MCM36256-70, t_{RC} = 130 ns		—	960		
MCM36256-80, t_{RC} = 150 ns		—	840		
MCM36256-10, t_{RC} = 180 ns		—	720		
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	—	24	mA	
V_{CC} Power Supply Current During $\overline{RAS}$ only Refresh Cycles	I_{CC3}			mA	2
MCM36256-70, t_{RC} = 130 ns		—	960		
MCM36256-80, t_{RC} = 150 ns		—	840		
MCM36256-10, t_{RC} = 180 ns		—	720		
V_{CC} Power Supply Current During Fast Page Mode Cycle	I_{CC4}			mA	2
MCM36256-70, t_{RC} = 40 ns		—	720		
MCM36256-80, t_{RC} = 45 ns		—	600		
MCM36256-10, t_{RC} = 55 ns		—	480		
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)	I_{CC5}	—	12	mA	
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle	I_{CC6}			mA	2
MCM36256-70, t_{RC} = 130 ns		—	960		
MCM36256-80, t_{RC} = 150 ns		—	840		
MCM36256-10, t_{RC} = 180 ns		—	720		
Input Leakage Current ($V_{SS} \le V_{in} \le V_{CC}$)	$I_{lkg(I)}$	– 120	120	µA	
Output Leakage Current ($\overline{CAS}$ at Logic 1, $V_{SS} \le V_{out} \le V_{CC}$)	$I_{lkg(O)}$	– 10	+ 10	µA	
Output High Voltage (I_{OH} = – 5 mA)	V_{OH}	2.4	—	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	—	0.4	V	

NOTES:
1. All voltages referenced to V_{SS}.
2. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.

3

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Min	Max	Unit	Notes
Input Capacitance (A0–A8)	C_{I1}	—	88	pF	1
Input Capacitance ($\overline{W}$)	C_{I2}	—	94	pF	1
Input Capacitance ($\overline{RAS0}$, $\overline{RAS2}$)	C_{I3}	—	52	pF	1
Input Capacitance ($\overline{CAS0}$–$\overline{CAS3}$)	C_{I4}	—	36	pF	1
I/O Capacitance (DQ0–DQ7, DQ9–DQ16, DQ18–DQ25, DQ27–DQ34)	C_{DQ1}	—	17	pF	1
I/O Capacitance (DQ8, DQ17, DQ26, DQ35)	C_{DQ2}	—	22	pF	1

NOTE:
1. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: C = 1 Δ t / Δ V.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ AND WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM36256-70		MCM36256-80		MCM36256-10		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	130	—	150	—	180	—	ns	5
Page Mode Cycle Time	t_{CELCEL}	t_{PC}	40	—	45	—	55	—	ns	
Access Time from $\overline{RAS}$	t_{RELQV}	t_{RAC}	—	70	—	80	—	100	ns	6, 7
Access Time from $\overline{CAS}$	t_{CELQV}	t_{CAC}	—	20	—	20	—	25	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	—	35	—	40	—	50	ns	6, 9
Access Time from Precharge $\overline{CAS}$	t_{CEHQV}	t_{CPA}	—	35	—	40	—	50	ns	6
$\overline{CAS}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	0	—	0	—	0	—	ns	6
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	20	0	20	0	20	ns	10
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{REHREL}	t_{RP}	50	—	60	—	70	—	ns	
$\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ Hold Time	t_{CELREH}	t_{RSH}	20	—	25	—	25	—	ns	
$\overline{CAS}$ Hold TIme	t_{RELCEH}	t_{CSH}	70	—	80	—	100	—	ns	
$\overline{CAS}$ Pulse Width	t_{CELCEH}	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RELCEL}	t_{RCD}	20	50	20	60	25	75	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	35	15	40	20	50	ns	12

(continued)

NOTES:
1. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
6. Measured with a current load equivalent to 2 TTL (– 200 µA, + 4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
8. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
9. Assumes that $t_{RAD} \geq t_{RAD}$ (max).
10. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively to t_{CAC}.
12. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.

READ AND WRITE CYCLES (Continued)

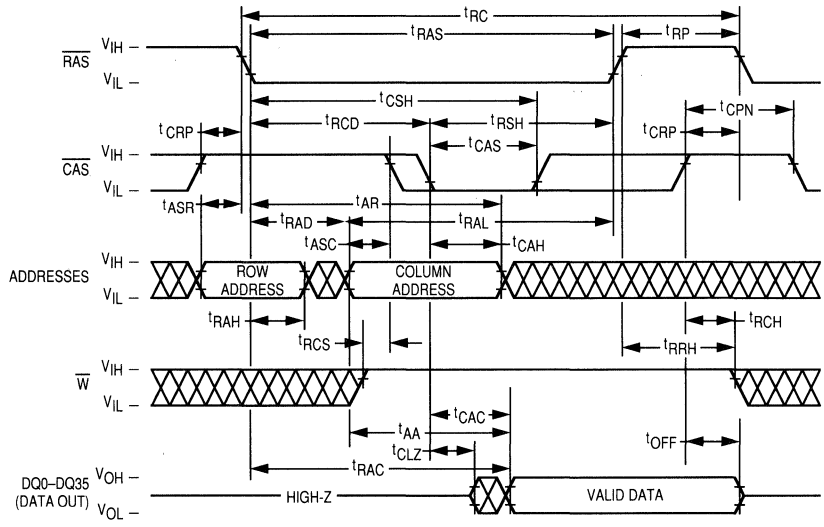
Parameter	Symbol		MCM36256-70		MCM36256-80		MCM36256-10		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	—	5	—	10	—	ns	
$\overline{CAS}$ Precharge Time (Page Mode Cyle Only)	t_{CEHCEL}	t_{CP}	10	—	10	—	10	—	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	—	10	—	15	—	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	—	15	—	20	—	ns	
Column Address Hold Time Referenced to $\overline{RAS}$	t_{RELAX}	t_{AR}	55	—	60	—	75	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{AVREH}	t_{RAL}	35	—	40	—	50	—	ns	
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time Referenced to $\overline{CAS}$	t_{CEHWX}	t_{RCH}	0	—	0	—	0	—	ns	13
Read Command Hold Time Referenced to $\overline{RAS}$	t_{REHWX}	t_{RRH}	0	—	0	—	0	—	ns	13
Write Command Hold Time Referenced to $\overline{CAS}$	t_{CELWH}	t_{WCH}	15	—	15	—	20	—	ns	
Write Command Hold Time Referenced to $\overline{RAS}$	t_{RELWH}	t_{WCR}	55	—	60	—	75	—	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	15	—	15	—	20	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{WLREH}	t_{RWL}	20	—	20	—	25	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{WLCEH}	t_{CWL}	20	—	20	—	25	—	ns	
Data in Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	0	—	ns	14, 15
Data in Hold Time	t_{CELDX}	t_{DH}	15	—	15	—	20	—	ns	14, 15
Data in Hold Time Referenced to $\overline{RAS}$	t_{RELDX}	t_{DHR}	55	—	60	—	75	—	ns	
Refresh Period	t_{RVRV}	t_{RFSH}	—	8	—	8	—	8	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	—	0	—	0	—	ns	15, 16
$\overline{CAS}$ Setup Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEL}	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEH}	t_{CHR}	30	—	30	—	30	—	ns	
$\overline{CAS}$ Precharge to $\overline{CAS}$ Active Time	t_{REHCEL}	t_{RPC}	0	—	0	—	0	—	ns	
$\overline{CAS}$ Precharge Time for $\overline{CAS}$ Before $\overline{RAS}$ Counter Test	t_{CEHCEL}	t_{CPT}	40	—	40	—	50	—	ns	
$\overline{CAS}$ Precharge Time	t_{CEHCEL}	t_{CPN}	10	—	10	—	15	—	ns	

NOTES:

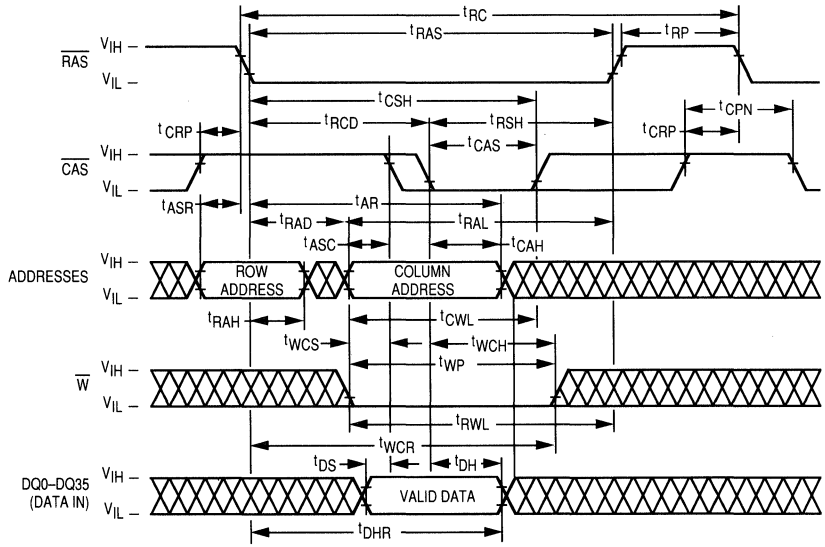
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles.
15. Early write only ($t_{WCS} \geq t_{WCS}$ (min)).
16. t_{WCS} is not a restrictive operating parameter. It is included in the data sheet as an electrical characteristic only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle. If this condition is not satisifed, the condition of the data out (at access time) is indeterminate.

3

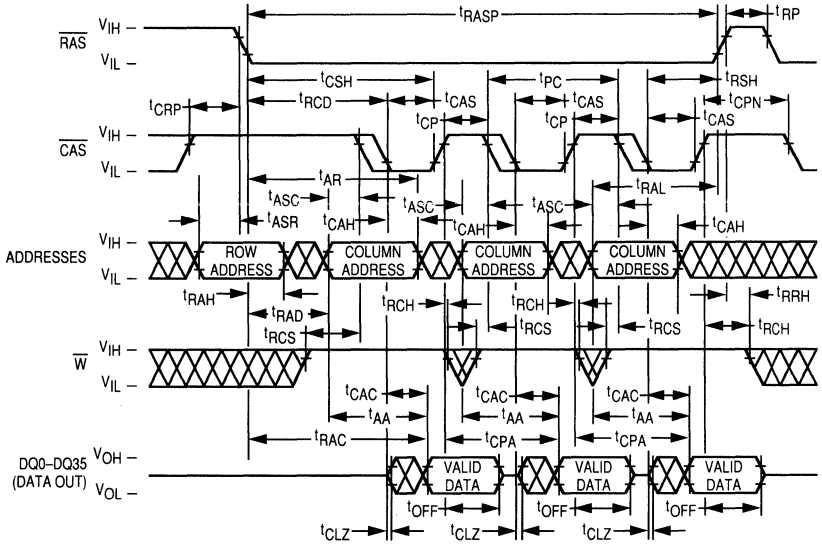
READ CYCLE



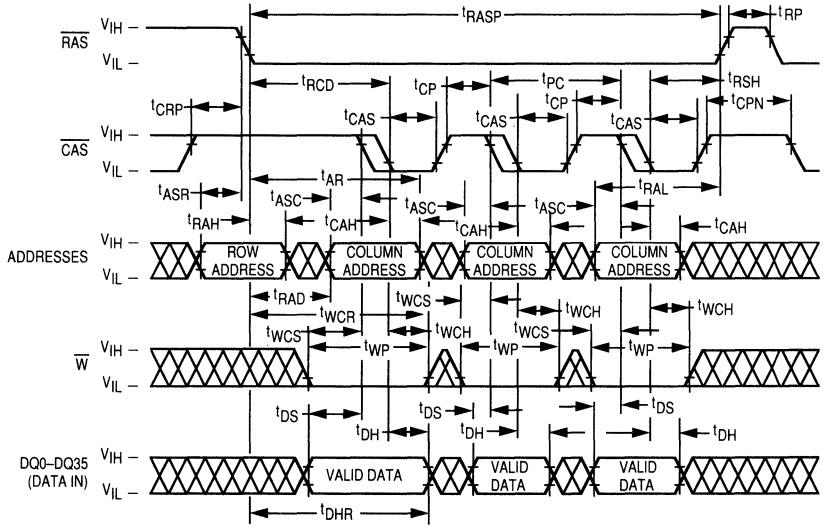
EARLY WRITE CYCLE



FAST PAGE MODE READ CYCLE



FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



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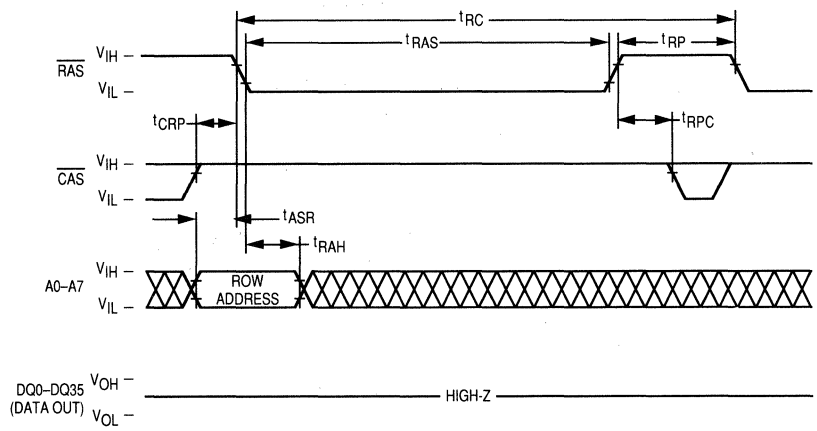
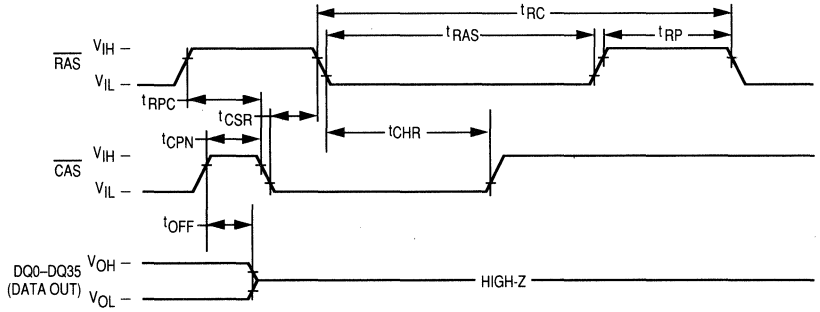
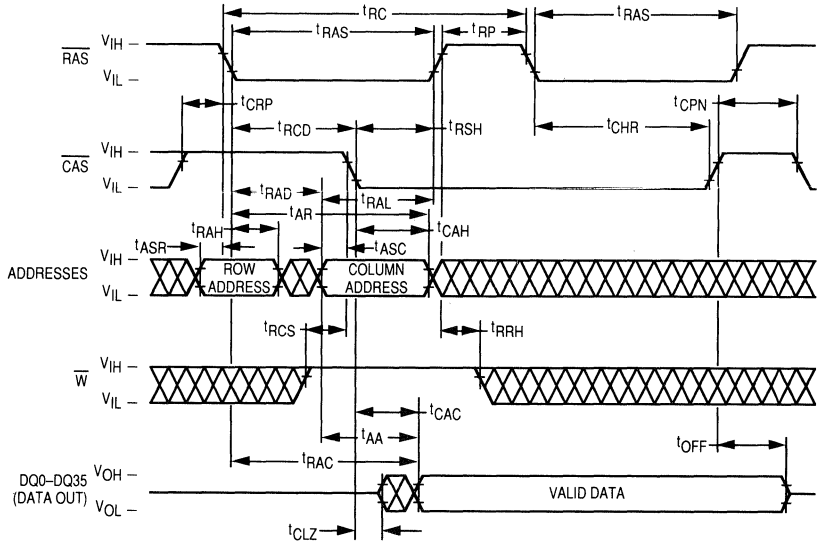
$\overline{RAS}$ ONLY REFRESH CYCLE
($\overline{W}$ and A8 are Don't Care)



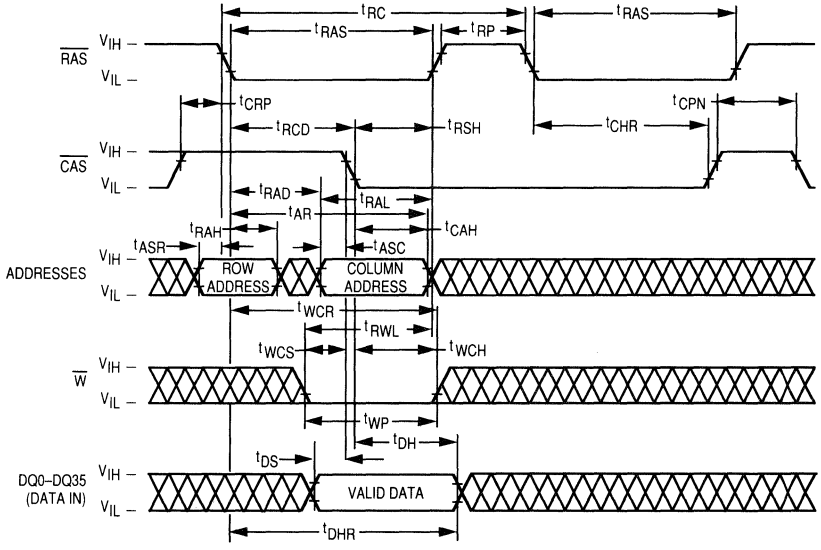
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE
($\overline{W}$ and A0 to A8 are Don't Care)



HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



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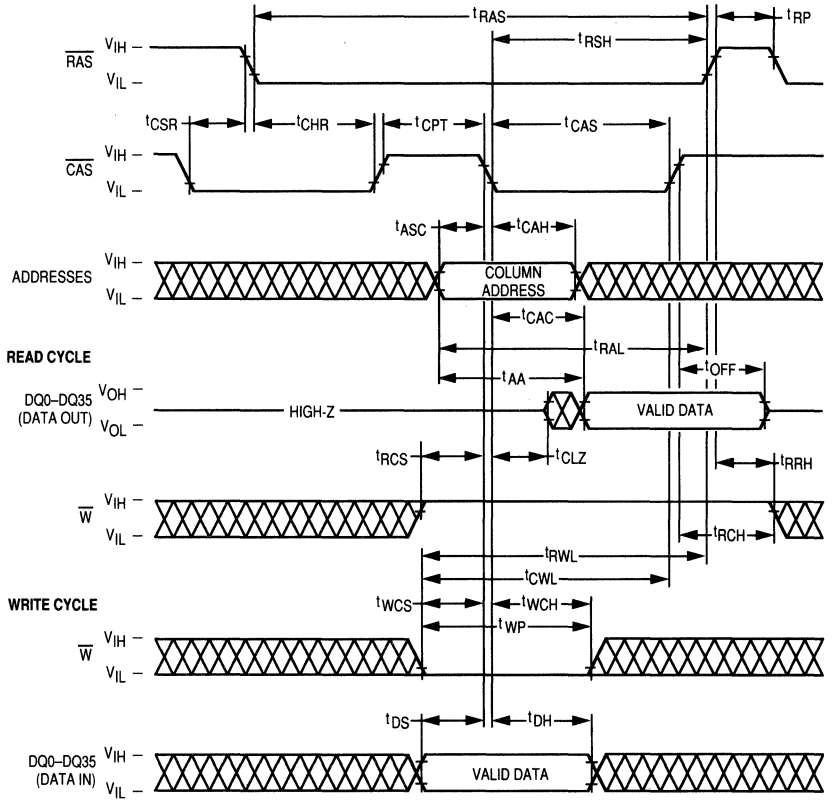
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



DEVICE INITIALIZATION

On power-up an initial pause of 200 microseconds is required for the internal substate generator pump to establish the correct bias voltage. This is to be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize the various dynamic nodes internal to the module. During an extended inactive state of the module (greater than 4 milliseconds with device powered up), the wake up sequence (8 active cycles) will be necessary to assure proper device operation.

ADDRESSING THE RAM

The nine address bus pins on the device are time multiplexed with two separate 9-bit address fields that are strobed at the beginning of the memory cycle by two clocks (active negative) called the row address strobe ($\overline{RAS}$) and the column address strobe ($\overline{CAS}$). A total of eighteen address bits will decode one of the 262,144 word locations in the device. The column address strobe follows the row address strobe by a specified minimum and maxium time called t_{RCD}, which is the row to column strobe delay. This time interval is also referred to as the multiplex window which gives flexibility to a system designer to set up the external addresses into the RAM. These conditions have to be met for normal read or write cycles. This initial portion of the cycle accomplishes the normal addressing of the device. These are, however, other variations in addressing the module: the refresh modes ($\overline{RAS}$ only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, hidden refresh), and another mode called page mode which allows the user to column access all words within a selected row. The refresh mode and page mode operations are described in more detail in later sections.

READ CYCLE

A read cycle is referred to as a normal read cycle to differentiate it from a page mode read cycle, which is covered in a later section.

The memory read cycle begins with the row addresses valid and the $\overline{RAS}$ clock transitioning from V_{IH} to the V_{IL} level. The $\overline{CAS}$ clock must also make a transition from V_{IH} to the V_{IL} level at the specified t_{RCD} timing limits when the column addresses are latched. Both the $\overline{RAS}$ and $\overline{CAS}$ clocks trigger a sequence of events which are controlled by several delayed internal clocks. Also, these clocks are linked in such a manner that the access time of the device is independent of the address multiplex window. The only stipulation is that the $\overline{CAS}$ clock must be active before or at the t_{RCD} maximum specification for an access (data valid) from the $\overline{RAS}$ clock edge to be guaranteed (t_{RAC}). If the t_{RCD} maximum condition is not met, the access (t_{CAC}) from the $\overline{CAS}$ clock active transition will determine read access time. The external $\overline{CAS}$ signal is ignored until an internal $\overline{RAS}$ signal is available. This gating feature on the $\overline{CAS}$ clock will allow the external $\overline{CAS}$ signal to become active as soon as the row address hold time (t_{RAH}) specification has been met and defines the t_{RCD} minimum specification. The time difference between t_{RCD} minimum and t_{RCD} maximum can be used to absorb skew delays in switching the address bus from the row to column addresses and in generating the $\overline{CAS}$ clock.

Once the clocks have become active, they must stay active for the minimum (t_{RAS}) period for the $\overline{RAS}$ clock and the minimum (t_{CAS}) period for the $\overline{CAS}$ clock. The $\overline{RAS}$ clock must stay inactive for the minimum (t_{RP}) time. The former is for the completion of the cycle in progress, and the latter is for the device internal circuitry to be precharged for the next active cycle.

Data out is not latched and is valid as long as the $\overline{CAS}$ clock is active; the output will switch to the three-state mode when the $\overline{CAS}$ clock goes inactive. To perform a read cycle, the write ($\overline{W}$) input must be held at the V_{IH} level from the time the $\overline{CAS}$ clock makes its active transition (t_{RCS}) to the time when it transitions into the inactive (t_{RCH}) mode.

WRITE CYCLE

A write cycle is similar to a read cycle except that the write ($\overline{W}$) clock must go active (V_{IL} level) at or before the $\overline{CAS}$ clock goes active at a minimum t_{WCS} time. If the above condition is met, then the cycle in progress is referred to as an early write cycle. In an early write cycle, the write clock and the data in are referenced to the active transition of the $\overline{CAS}$ clock edge. There are two important parameters with respect to the write cycle: the column strobe to write lead time (t_{CWL}) and the row strobe to write lead time (t_{RWL}). These define the minimum time that $\overline{RAS}$ and $\overline{CAS}$ clocks need to be active after the write operation has started ($\overline{W}$ clock at V_{IL} level).

PAGE-MODE CYCLES

Page mode operation allows fast successive data operations at all 512 column locations on a selected row. Page access (t_{CAC}) is typically half the regular $\overline{RAS}$ clock access (t_{RAC}) on the Motorola 1M dynamic RAM. Page mode operation consists of holding the $\overline{RAS}$ clock active while cycling the $\overline{CAS}$ clock to access the column locations determined by the 10-bit column address field.

The page cycle is always initiated with a row address being provided and latched by the $\overline{RAS}$ clock, followed by the column address and $\overline{CAS}$ clock. From the timing illustrated, the initial cycle is a normal read or write cycle, that has been previously described, followed by the shorter $\overline{CAS}$ cycles (t_{PC}). The $\overline{CAS}$ cycle time (t_{PC}) consists of the $\overline{CAS}$ clock active time (t_{CAS}), and $\overline{CAS}$ clock precharge time (t_{CP}) and two transitions. In practice, any combination of read and write cycles can be performed to suit a particular application.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Therefore, to retain the correct information, the module needs to be refreshed at least once every 8 milliseconds. This is accomplished by sequentially cycling through the 512 row address locations every 8 milliseconds (i.e., at least one row every 15.6 microseconds). A normal read or write operation to the module will also refresh all the words associated with the particular row(s) decoded.

$\overline{RAS}$-Only Refresh

In this refresh method, the system must perform a $\overline{RAS}$-only cycle on 512 row addresses every 8 milliseconds. The row addresses are latched in with the $\overline{RAS}$ clock, and the associated internal row locations are refreshed. As the heading implies, the $\overline{CAS}$ clock is not required and must be inactive or at a V_{IH} level.

3

$\overline{CAS}$ Before $\overline{RAS}$ Refresh

This refresh cycle is initiated when $\overline{RAS}$ falls, after $\overline{CAS}$ has been low (by t_{CSR}). This activates the internal refresh counter which generates the row address to be refreshed. Externally applied addresses are ignored during the automatic refresh cycle. If the output buffer was off before the automatic refresh cycle, the output will stay in the high impedance state. If the output was enabled by $\overline{CAS}$ in the previous cycle, the data out will be maintained during the automatic refresh cycle as long as $\overline{CAS}$ is held active (hidden refresh).

Hidden Refresh

The hidden refresh method allows refresh cycles to be performed while maintaining valid data at the output pin. Hidden refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. (See Figure 1.)

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST

The internal refresh counter of the device can be tested with a **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test**. This refresh counter test is performed with read and write operations. During this test, the internal refresh counter generates the row address, while the external address input supplies the column address. The entire array is refreshed after 512 test cycles, as indicated by the check data written in each row. See **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test cycle** timing diagram.

The test can be performed only after a minimum of **8 $\overline{CAS}$ before $\overline{RAS}$** initialization cycles. The test procedure is as follows:

1. Write "0"s into all memory cells (normal write mode).
2. Select a column address, and read "0" out of the cell by performing **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test, read cycle**. Repeat this operation 512 times.
3. Select a column address, and write "1" into the cell by performing **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test, write cycle**. Repeat this operation 512 times.
4. Read "1"s (normal read mode), which were written at step 3.
5. Repeat steps 1 to 4 using complement data.

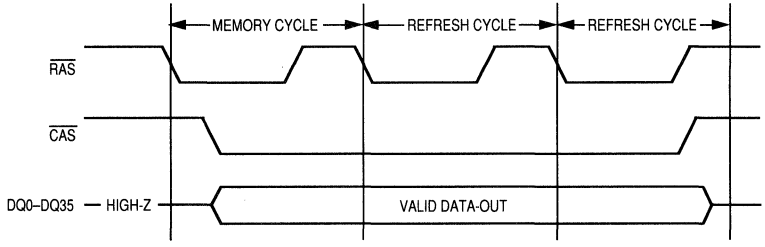
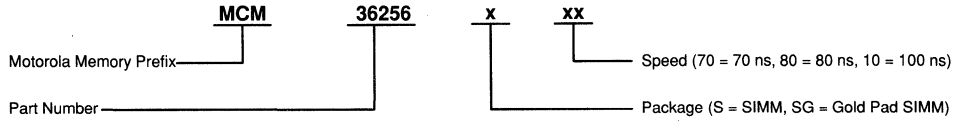


Figure 1. Hidden Refresh Cycle

ORDERING INFORMATION
(Order by Full Part Number)

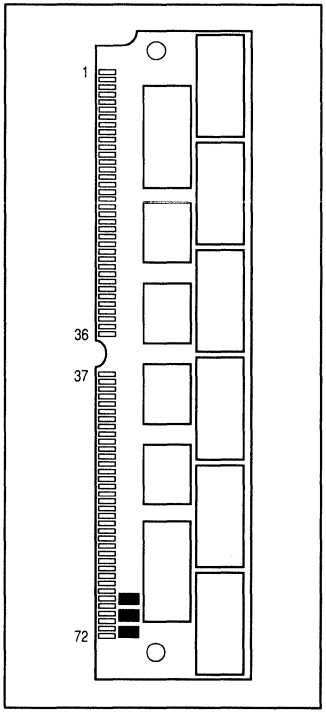


Full Part Numbers – MCM36256S70, MCM36256S80, MCM36256S10, MCM36256SG70, MCM36256SG80, MCM36256SG10

MCM36512

Advance Information

512K × 36 Bit Dynamic Random Access Memory Module



The MCM36512S is an 18M, dynamic random access memory (DRAM) module organized as 524,288 × 36 bits. The module is a 72-lead double-sided single-in-line memory module (SIMM) consisting of sixteen MCM514256A DRAMs housed in 20/26 J-lead small outline packages (SOJ) and eight CMOS 256K × 1 DRAMs housed in 18-lead PLCC packages, mounted on a substrate along with a 0.22 µF (min) decoupling capacitor mounted under each DRAM. The MCM514256A is a 1.0 µ CMOS high speed, dynamic random access memory organized as 262,144 four-bit words and fabricated with CMOS silicon-gate process technology.

- Three-State Data Output
- Early-Write Common I/O Capability
- Fast Page Mode Capability
- TTL-Compatible Inputs and Outputs
- $\overline{RAS}$ Only Refresh
- $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- Hidden Refresh
- 512 Cycle Refresh:
  MCM36512 = 8 ms (Max)
- Consists of Sixteen 256K × 4 DRAMs, Eight 256K × 1 DRAMs, and Twenty Four 0.22 µF (Min) Decoupling Capacitors
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}):
  MCM36512S-70 = 70 ns (Max)
  MCM36512S-80 = 80 ns (Max)
  MCM36512S-10 = 100 ns (Max)
- Low Active Power Dissipation:
  MCM36512S-70 = 5.412 W (Max)
  MCM36512S-80 = 4.752 W (Max)
  MCM36512S-10 = 4.092 W (Max)
- Low Standby Power Dissipation:
  TTL Levels = 264 mW (Max)
  CMOS Levels = 132 mW (Max)

PIN OUT

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V_{SS}	13	A1	25	DQ24	37	DQ17	49	DQ9	61	DQ14
2	DQ0	14	A2	26	DQ7	38	DQ35	50	DQ27	62	DQ33
3	DQ18	15	A3	27	DQ25	39	V_{SS}	51	DQ10	63	DQ15
4	DQ1	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ28	64	DQ34
5	DQ19	17	A5	29	NC	41	$\overline{CAS2}$	53	DQ11	65	DQ16
6	DQ2	18	A6	30	V_{CC}	42	$\overline{CAS3}$	54	DQ29	66	NC
7	DQ20	19	NC	31	A8	43	$\overline{CAS1}$	55	DQ12	67	PD1
8	DQ3	20	DQ4	32	NC	44	$\overline{RAS0}$	56	DQ30	68	PD2
9	DQ21	21	DQ22	33	$\overline{RAS3}$	45	$\overline{RAS1}$	57	DQ13	69	PD3
10	V_{CC}	22	DQ5	34	$\overline{RAS2}$	46	NC	58	DQ31	70	PD4
11	NC	23	DQ23	35	DQ26	47	$\overline{W}$	59	V_{CC}	71	NC
12	A0	24	DQ6	36	DQ8	48	NC	60	DQ32	72	V_{SS}

PIN NAMES

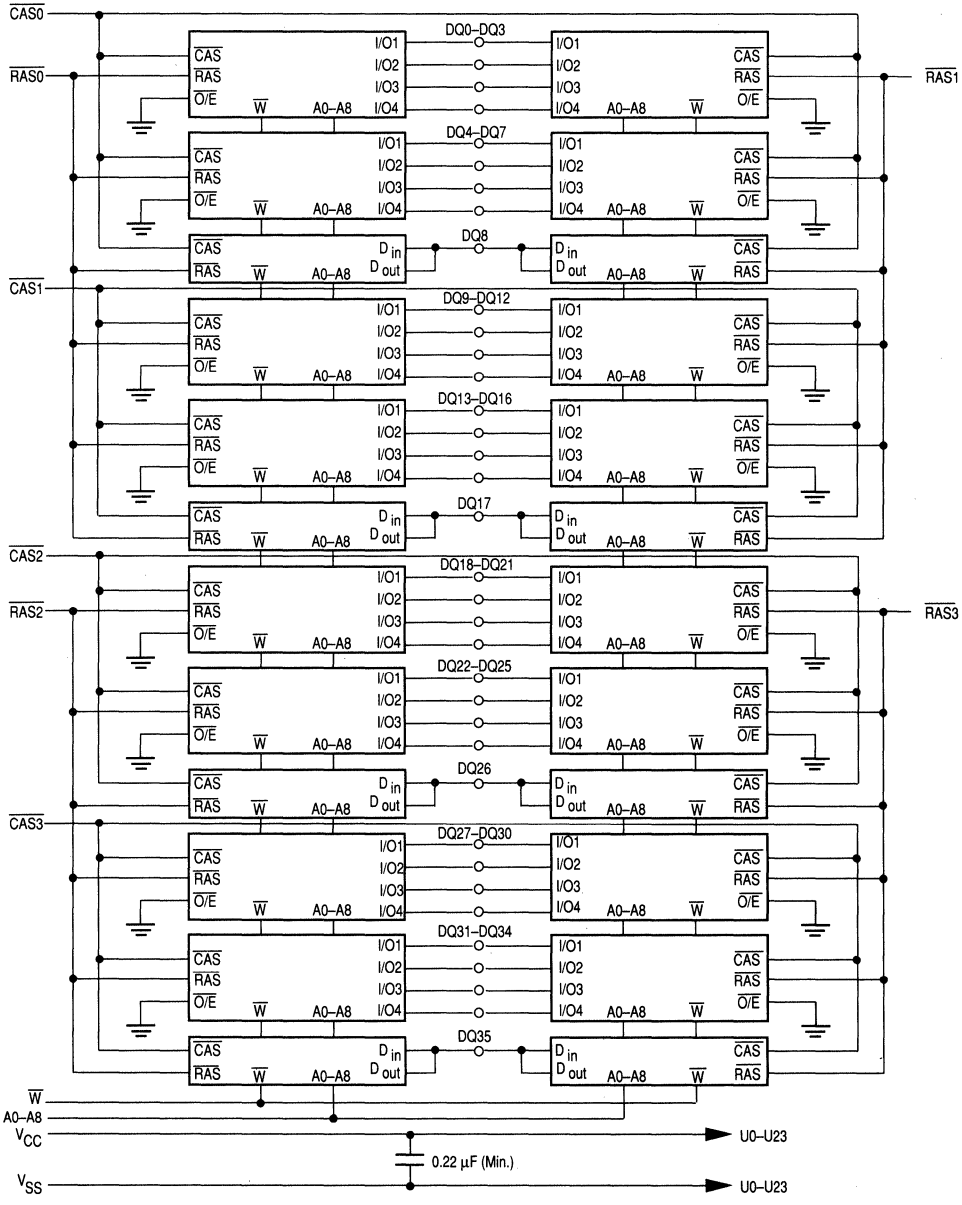
A0–A8	Address Inputs
DQ0–DQ35	Data Input/Output
$\overline{CAS0}$–$\overline{CAS3}$	Column Address Strobe
PD1–PD4	Presence Detect
$\overline{RAS0}$–$\overline{RAS3}$	Row Address Strobe
$\overline{W}$	Read/Write Input
V_{CC}	Power (+ 5 V)
V_{SS}	Ground
NC	No Connection

All power supply and ground pins must be connected for proper operation of the device.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

3

BLOCK DIAGRAM



PRESENCE DETECT PIN OUT			
Pin Name	**70 ns**	**80 ns**	**100 ns**
PD1	NC	NC	NC
PD2	V_{SS}	V_{SS}	V_{SS}
PD3	V_{SS}	NC	V_{SS}
PD4	NC	V_{SS}	V_{SS}

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 1 to + 7	V
Voltage Relative to V_{SS} (For Any Pin Except V_{CC})	V_{in}, V_{out}	– 1 to + 7	V
Data Output Current per DQ Pin	I_{out}	50	mA
Power Dissipation	P_D	7.4	W
Operating Temperature Range	T_A	0 to + 70	°C
Storage Temperature Range	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high impedence circuits.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V	1
	V_{SS}	0	0	0		
Logic High Voltage, All Inputs	V_{IH}	2.4	—	6.5	V	1
Logic Low Voltage, All Inputs	V_{IL}	– 1.0	—	0.8	v	1

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current MCM36512-70, t_{RC} = 130 ns MCM36512-80, t_{RC} = 150 ns MCM36512-10, t_{RC} = 180 ns	I_{CC1}	 — — —	 984 864 744	mA	2
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	—	48	mA	
V_{CC} Power Supply Current During $\overline{RAS}$ only Refresh Cycles MCM36512-70, t_{RC} = 130 ns MCM36512-80, t_{RC} = 150 ns MCM36512-10, t_{RC} = 180 ns	I_{CC3}	 — — —	 984 864 744	mA	2
V_{CC} Power Supply Current During Fast Page Mode Cycle MCM36512-70, t_{RC} = 40 ns MCM36512-80, t_{RC} = 45 ns MCM36512-10, t_{RC} = 55 ns	I_{CC4}	 — — —	 744 624 504	mA	2
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)	I_{CC5}	—	24	mA	
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle MCM36512-70, t_{RC} = 130 ns MCM36512-80, t_{RC} = 150 ns MCM36512-10, t_{RC} = 180 ns	I_{CC6}	 — — —	 984 864 744	mA	2
Input Leakage Current ($V_{SS} \le V_{in} \le V_{CC}$)	$I_{lkg(I)}$	– 240	240	µA	
Output Leakage Current ($\overline{CAS}$ at Logic 1, $V_{SS} \le V_{out} \le V_{CC}$)	$I_{lkg(O)}$	– 20	20	µA	
Output High Voltage (I_{OH} = – 5 mA)	V_{OH}	2.4	—	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	—	0.4	V	

NOTES:
1. All voltages referenced to V_{SS}.
2. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Min	Max	Unit	Notes
Input Capacitance (A0–A8)	C_{I1}	—	161	pF	1
Input Capacitance ($\overline{W}$)	C_{I2}	—	178	pF	1
Input Capacitance ($\overline{RAS0}$–$\overline{RAS3}$)	C_{I3}	—	52	pF	1
Input Capacitance ($\overline{CAS0}$–$\overline{CAS3}$)	C_{I4}	—	52	pF	1
I/O Capacitance (DQ0–DQ7, DQ9–DQ16, DQ18–DQ25, DQ27–DQ34)	C_{DQ1}	—	29	pF	1
I/O Capacitance (DQ8, DQ17, DQ26, DQ35)	C_{DQ2}	—	39	pF	1

NOTE:
1. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: C = 1 Δ t / Δ V.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ AND WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM36512-70		MCM36512-80		MCM36512-10		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	130	—	150	—	180	—	ns	5
Page Mode Cycle Time	t_{CELCEL}	t_{PC}	40	—	45	—	55	—	ns	
Access Time from $\overline{RAS}$	t_{RELQV}	t_{RAC}	—	70	—	80	—	100	ns	6, 7
Access Time from $\overline{CAS}$	t_{CELQV}	t_{CAC}	—	20	—	20	—	25	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	—	35	—	40	—	50	ns	6, 9
Access Time from Precharge $\overline{CAS}$	t_{CEHQV}	t_{CPA}	—	35	—	40	—	50	ns	6
$\overline{CAS}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	0	—	0	—	0	—	ns	6
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	20	0	20	0	20	ns	10
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{REHREL}	t_{RP}	50	—	60	—	70	—	ns	
$\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ Hold Time	t_{CELREH}	t_{RSH}	20	—	25	—	25	—	ns	
$\overline{CAS}$ Hold TIme	t_{RELCEH}	t_{CSH}	70	—	80	—	100	—	ns	
$\overline{CAS}$ Pulse Width	t_{CELCEH}	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RELCEL}	t_{RCD}	20	50	20	60	25	75	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	35	15	40	20	50	ns	12

(continued)

NOTES:
1. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
6. Measured with a current load equivalent to 2 TTL (– 200 μA, + 4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
8. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
9. Assumes that $t_{RAD} \geq t_{RAD}$ (max).
10. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively to t_{CAC}.
12. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.

READ AND WRITE CYCLES (Continued)

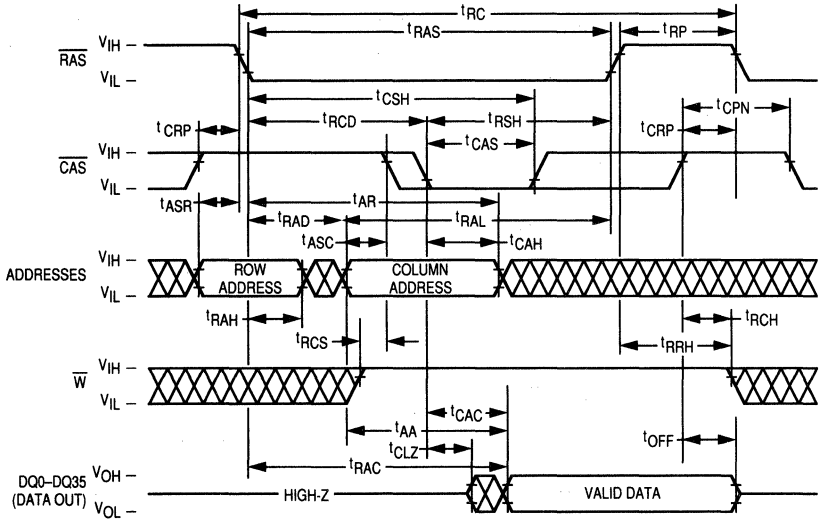
Parameter	Symbol		MCM36512-70		MCM36512-80		MCM36512-10		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	—	5	—	10	—	ns	
$\overline{CAS}$ Precharge Time (Page Mode Cyle Only)	t_{CEHCEL}	t_{CP}	10	—	10	—	10	—	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	—	10	—	15	—	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	—	15	—	20	—	ns	
Column Address Hold Time Referenced to $\overline{RAS}$	t_{RELAX}	t_{AR}	55	—	60	—	75	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{AVREH}	t_{RAL}	35	—	40	—	50	—	ns	
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time Referenced to $\overline{CAS}$	t_{CEHWX}	t_{RCH}	0	—	0	—	0	—	ns	13
Read Command Hold Time Referenced to $\overline{RAS}$	t_{REHWX}	t_{RRH}	0	—	0	—	0	—	ns	13
Write Command Hold Time Referenced to $\overline{CAS}$	t_{CELWH}	t_{WCH}	15	—	15	—	20	—	ns	
Write Command Hold Time Referenced to $\overline{RAS}$	t_{RELWH}	t_{WCR}	55	—	60	—	75	—	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	15	—	15	—	20	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{WLREH}	t_{RWL}	20	—	20	—	25	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{WLCEH}	t_{CWL}	20	—	20	—	25	—	ns	
Data in Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	0	—	ns	14, 15
Data in Hold Time	t_{CELDX}	t_{DH}	15	—	15	—	20	—	ns	14, 15
Data in Hold Time Referenced to $\overline{RAS}$	t_{RELDX}	t_{DHR}	55	—	60	—	75	—	ns	
Refresh Period	t_{RVRV}	t_{RFSH}	—	8	—	8	—	8	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	—	0	—	0	—	ns	15, 16
$\overline{CAS}$ Setup Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEL}	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEH}	t_{CHR}	30	—	30	—	30	—	ns	
$\overline{CAS}$ Precharge to $\overline{CAS}$ Active Time	t_{REHCEL}	t_{RPC}	0	—	0	—	0	—	ns	
$\overline{CAS}$ Precharge Time for $\overline{CAS}$ Before $\overline{RAS}$ Counter Test	t_{CEHCEL}	t_{CPT}	40	—	40	—	50	—	ns	
$\overline{CAS}$ Precharge Time	t_{CEHCEL}	t_{CPN}	10	—	10	—	15	—	ns	

NOTES:

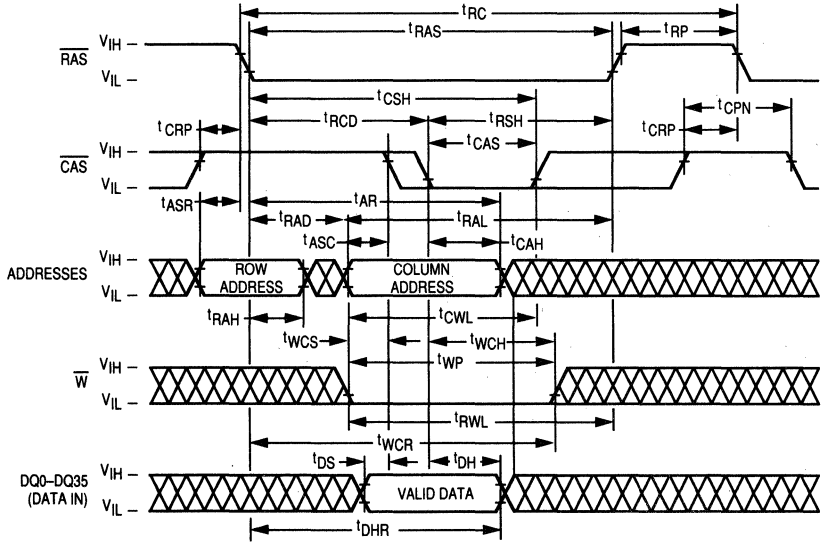
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles.
15. Early write only ($t_{WCS} \geq t_{WCS}$ (min)).
16. t_{WCS} is not a restrictive operating parameter. It is included in the data sheet as an electrical characteristic only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle. If this condition is not satisifed, the condition of the data out (at access time) is indeterminate.
17. To avoid bus contention and potential damage to the module, $\overline{RAS0}$ and $\overline{RAS1}$ may not be active low simultaneously. Similarly, $\overline{RAS2}$ and $\overline{RAS3}$ may not be simultaneously active low.

3

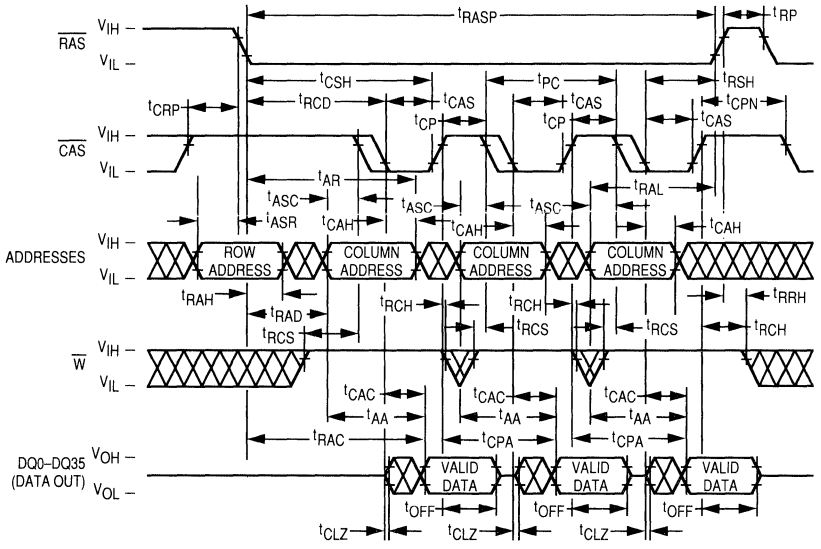
READ CYCLE



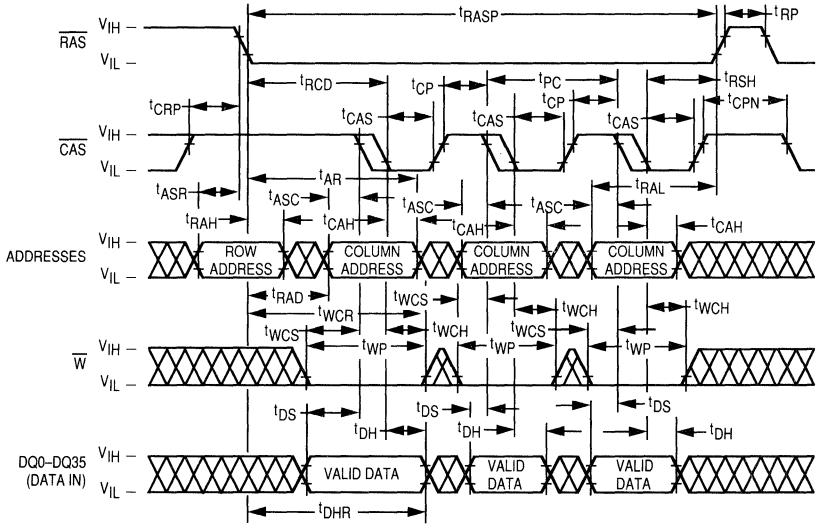
EARLY WRITE CYCLE



FAST PAGE MODE READ CYCLE



FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



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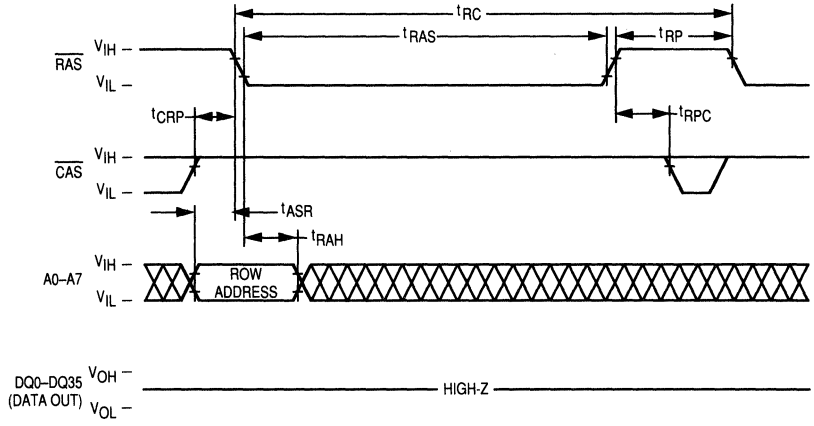
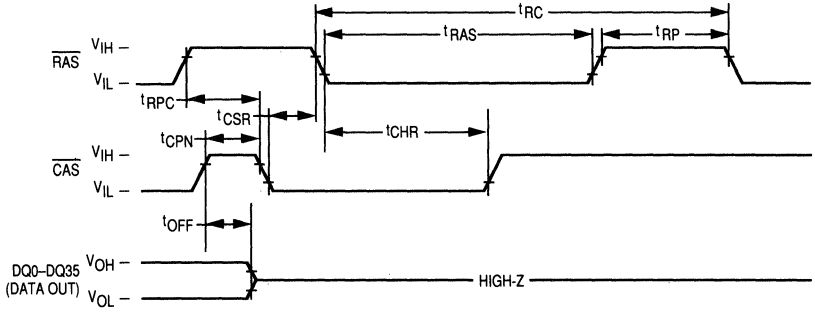
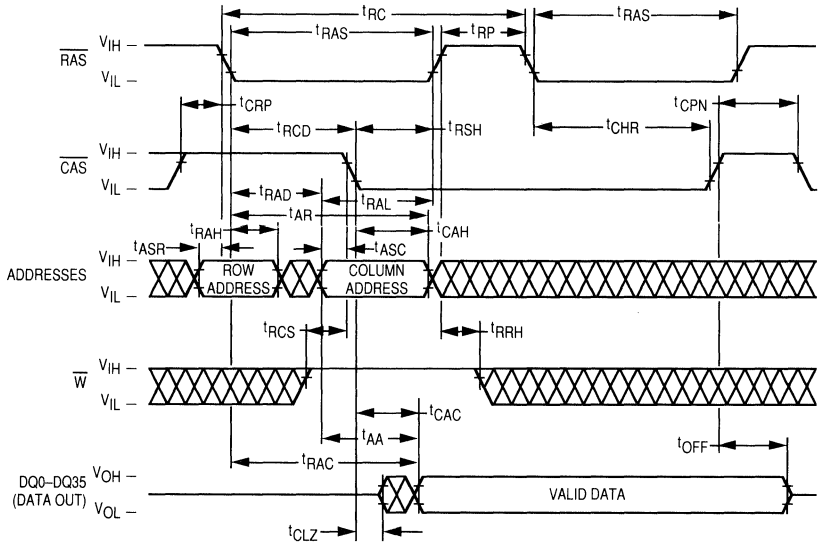
$\overline{RAS}$ ONLY REFRESH CYCLE
($\overline{W}$ and A8 are Don't Care)



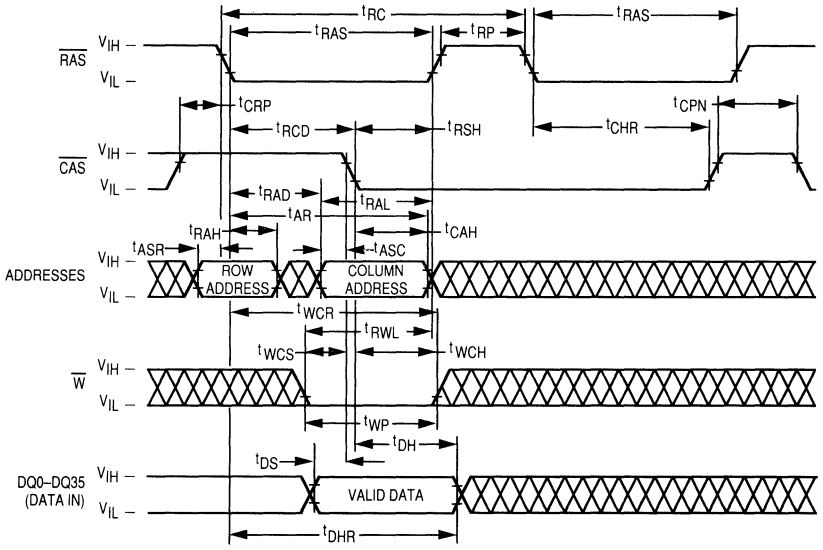
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE
($\overline{W}$ and A0 to A8 are Don't Care)



HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



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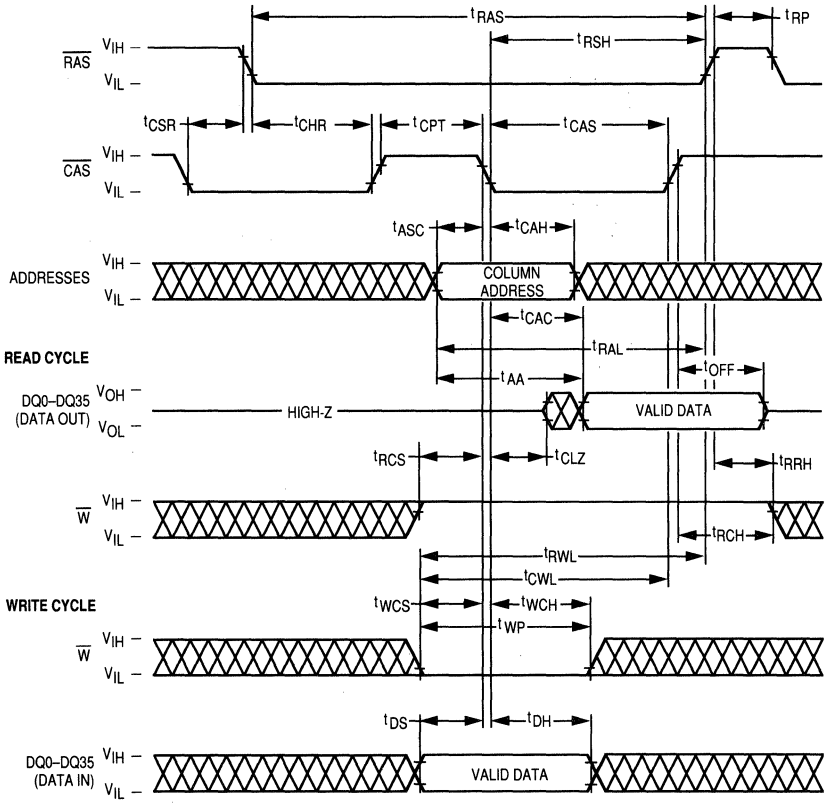
$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST CYCLE



DEVICE INITIALIZATION

On power-up an initial pause of 200 microseconds is required for the internal substate generator pump to establish the correct bias voltage. This is to be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize the various dynamic nodes internal to the module. During an extended inactive state of the module (greater than 4 milliseconds with device powered up), the wake up sequence (8 active cycles) will be necessary to assure proper device operation.

ADDRESSING THE RAM

The nine address bus pins on the device are time multiplexed with two separate 9-bit address fields that are strobed at the beginning of the memory cycle by two clocks (active negative) called the row address strobe ($\overline{RAS}$) and the column address strobe ($\overline{CAS}$). A total of eighteen address bits will decode one of the 262,144 word locations in the device. The column address strobe follows the row address strobe by a specified minimum and maxium time called t_{RCD}, which is the row to column strobe delay. This time interval is also referred to as the multiplex window which gives flexibility to a system designer to set up the external addresses into the RAM. These conditions have to be met for normal read or write cycles. This initial portion of the cycle accomplishes the normal addressing of the device. These are, however, other variations in addressing the module: the refresh modes ($\overline{RAS}$ only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, hidden refresh), and another mode called page mode which allows the user to column access all words within a selected row. The refresh mode and page mode operations are described in more detail in later sections.

READ CYCLE

A read cycle is referred to as a normal read cycle to differentiate it from a page mode read cycle, which is covered in a later section.

The memory read cycle begins with the row addresses valid and the $\overline{RAS}$ clock transitioning from V_{IH} to the V_{IL} level. The $\overline{CAS}$ clock must also make a transition from V_{IH} to the V_{IL} level at the specified t_{RCD} timing limits when the column addresses are latched. Both the $\overline{RAS}$ and $\overline{CAS}$ clocks trigger a sequence of events which are controlled by several delayed internal clocks. Also, these clocks are linked in such a manner that the access time of the device is independent of the address multiplex window. The only stipulation is that the $\overline{CAS}$ clock must be active before or at the t_{RCD} maximum specification for an access (data valid) from the $\overline{RAS}$ clock edge to be guaranteed (t_{RAC}). If the t_{RCD} maximum condition is not met, the access (t_{CAC}) from the $\overline{CAS}$ clock active transition will determine read access time. The external $\overline{CAS}$ signal is ignored until an internal $\overline{RAS}$ signal is available. This gating feature on the $\overline{CAS}$ clock will allow the external $\overline{CAS}$ signal to become active as soon as the row address hold time (t_{RAH}) specification has been met and defines the t_{RCD} minimum specification. The time difference between t_{RCD} minimum and t_{RCD} maximum can be used to absorb skew delays in switching the address bus from the row to column addresses and in generating the $\overline{CAS}$ clock.

Once the clocks have become active, they must stay active for the minimum (t_{RAS}) period for the $\overline{RAS}$ clock and the minimum (t_{CAS}) period for the $\overline{CAS}$ clock. The $\overline{RAS}$ clock must stay inactive for the minimum (t_{RP}) time. The former is for the completion of the cycle in progress, and the latter is for the device internal circuitry to be precharged for the next active cycle.

Data out is not latched and is valid as long as the $\overline{CAS}$ clock is active; the output will switch to the three-state mode when the $\overline{CAS}$ clock goes inactive. To perform a read cycle, the write ($\overline{W}$) input must be held at the V_{IH} level from the time the $\overline{CAS}$ clock makes its active transition (t_{RCS}) to the time when it transitions into the inactive (t_{RCH}) mode.

WRITE CYCLE

A write cycle is similar to a read cycle except that the write ($\overline{W}$) clock must go active (V_{IL} level) at or before the $\overline{CAS}$ clock goes active at a minimum t_{WCS} time. If the above condition is met, then the cycle in progress is referred to as an early write cycle. In an early write cycle, the write clock and the data in are referenced to the active transition of the $\overline{CAS}$ clock edge. There are two important parameters with respect to the write cycle: the column strobe to write lead time (t_{CWL}) and the row strobe to write lead time (t_{RWL}). These define the minimum time that $\overline{RAS}$ and $\overline{CAS}$ clocks need to be active after the write operation has started ($\overline{W}$ clock at V_{IL} level).

PAGE-MODE CYCLES

Page mode operation allows fast successive data operations at all 512 column locations on a selected row. Page access (t_{CAC}) is typically half the regular $\overline{RAS}$ clock access (t_{RAC}) on the Motorola 1M dynamic RAM. Page mode operation consists of holding the $\overline{RAS}$ clock active while cycling the $\overline{CAS}$ clock to access the column locations determined by the 10-bit column address field.

The page cycle is always initiated with a row address being provided and latched by the $\overline{RAS}$ clock, followed by the column address and $\overline{CAS}$ clock. From the timing illustrated, the initial cycle is a normal read or write cycle, that has been previously described, followed by the shorter $\overline{CAS}$ cycles (t_{PC}). The $\overline{CAS}$ cycle time (t_{PC}) consists of the $\overline{CAS}$ clock active time (t_{CAS}), and $\overline{CAS}$ clock precharge time (t_{CP}) and two transitions. In practice, any combination of read and write cycles can be performed to suit a particular application.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Therefore, to retain the correct information, the module needs to be refreshed at least once every 8 milliseconds. This is accomplished by sequentially cycling through the 512 row address locations every 8 milliseconds (i.e., at least one row every 15.6 microseconds). A normal read or write operation to the module will also refresh all the words associated with the particular row(s) decoded.

$\overline{RAS}$-Only Refresh

In this refresh method, the system must perform a $\overline{RAS}$-only cycle on 512 row addresses every 8 milliseconds. The row addresses are latched in with the $\overline{RAS}$ clock, and the associated internal row locations are refreshed. As the heading implies, the $\overline{CAS}$ clock is not required and must be inactive or at a V_{IH} level.

3

$\overline{CAS}$ Before $\overline{RAS}$ Refresh

This refresh cycle is initiated when $\overline{RAS}$ falls, after $\overline{CAS}$ has been low (by t_{CSR}). This activates the internal refresh counter which generates the row address to be refreshed. Externally applied addresses are ignored during the automatic refresh cycle. If the output buffer was off before the automatic refresh cycle, the output will stay in the high impedance state. If the output was enabled by $\overline{CAS}$ in the previous cycle, the data out will be maintained during the automatic refresh cycle as long as $\overline{CAS}$ is held active (hidden refresh).

Hidden Refresh

The hidden refresh method allows refresh cycles to be performed while maintaining valid data at the output pin. Hidden refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. (See Figure 1.)

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST

The internal refresh counter of the device can be tested with a **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test**. This refresh counter test is performed with read and write operations. During this test, the internal refresh counter generates the row address, while the external address input supplies the column address. The entire array is refreshed after 512 test cycles, as indicated by the check data written in each row. See **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test cycle** timing diagram.

The test can be performed only after a minimum of **8 $\overline{CAS}$ before $\overline{RAS}$** initialization cycles. The test procedure is as follows:

1. Write "0"s into all memory cells (normal write mode).
2. Select a column address, and read "0" out of the cell by performing **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test, read cycle**. Repeat this operation 512 times.
3. Select a column address, and write "1" into the cell by performing **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test, write cycle**. Repeat this operation 512 times.
4. Read "1"s (normal read mode), which were written at step 3.
5. Repeat steps 1 to 4 using complement data.

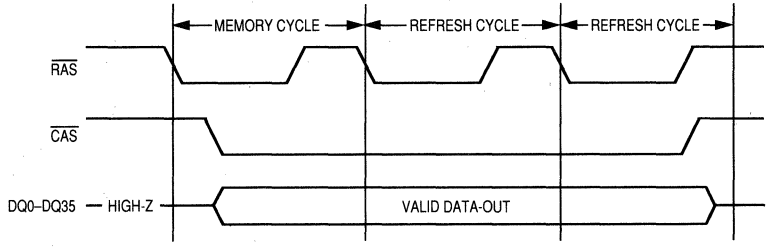
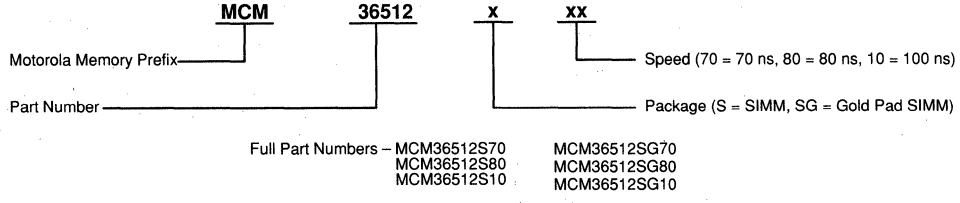


Figure 1. Hidden Refresh Cycle

ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers – MCM36512S70, MCM36512S80, MCM36512S10, MCM36512SG70, MCM36512SG80, MCM36512SG10

MCM81000
MCM8L1000

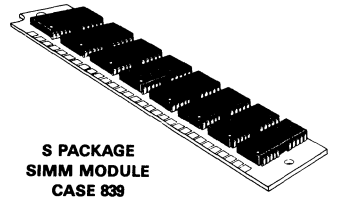
3

Advance Information

1M x 8 Bit Dynamic Random Access Memory Module

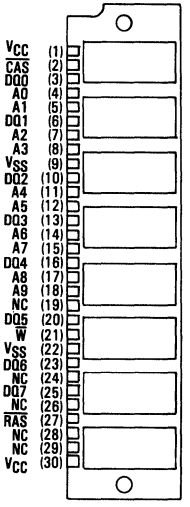
The MCM81000L and MCM81000S are 8M, dynamic random access memory (DRAM) modules organized as 1,048,576 x 8 bits. The modules are 30-lead single-in-line memory modules (SIMM) or 30-pin single-in-line packages (SIP) consisting of eight MCM511000A DRAMs housed in a 20/26 J-lead small outline package (SOJ) and mounted on a substrate along with a 0.22 μF (min) decoupling capacitor mounted under each DRAM. The MCM511000A is a 1.0μ CMOS high speed, dynamic random access memory organized as 1,048,576 one-bit words and fabricated with CMOS silicon-gate process technology.

- Three-State Data Output
- Early-Write Common I/O Capability
- Fast Page Mode Capability
- TTL-Compatible Inputs and Outputs
- $\overline{RAS}$ Only Refresh
- $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- Hidden Refresh
- 512 Cycle Refresh:
  - MCM81000 = 8 ms (Max)
  - MCM8L1000 = 64 ms (Max)
- Consists of Eight 1M DRAMs and Eight 0.22 μF (Min) Decoupling Capacitors
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}):
  - MCM81000-70 = 70 ns (Max)
  - MCM81000-80 = 80 ns (Max)
  - MCM81000-10 = 100 ns (Max)
- Low Active Power Dissipation:
  - MCM81000-70 = 3.6 W (Max)
  - MCM81000-80 = 3.1 W (Max)
  - MCM81000-10 = 2.7 W (Max)
- Low Standby Power Dissipation:
  - TTL Levels = 88 mW (Max)
  - CMOS Levels (MCM81000) = 45 mW (Max)
    (MCM8L1000) = 9 mW (Max)
- $\overline{CAS}$ Control for Eight Common I/O Lines
- Available in Edge Connector (MCM81000S) or Pin Connector (MCM81000L)

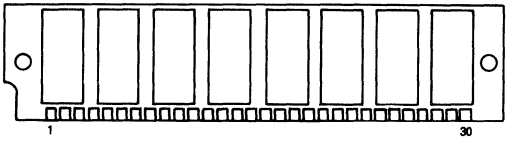


S PACKAGE
SIMM MODULE
CASE 839

30-PIN
SINGLE IN-LINE PACKAGE
(TOP VIEW, MCM81000S/8L1000S)



MCM81000S OR MCM8L1000S (SIMM)

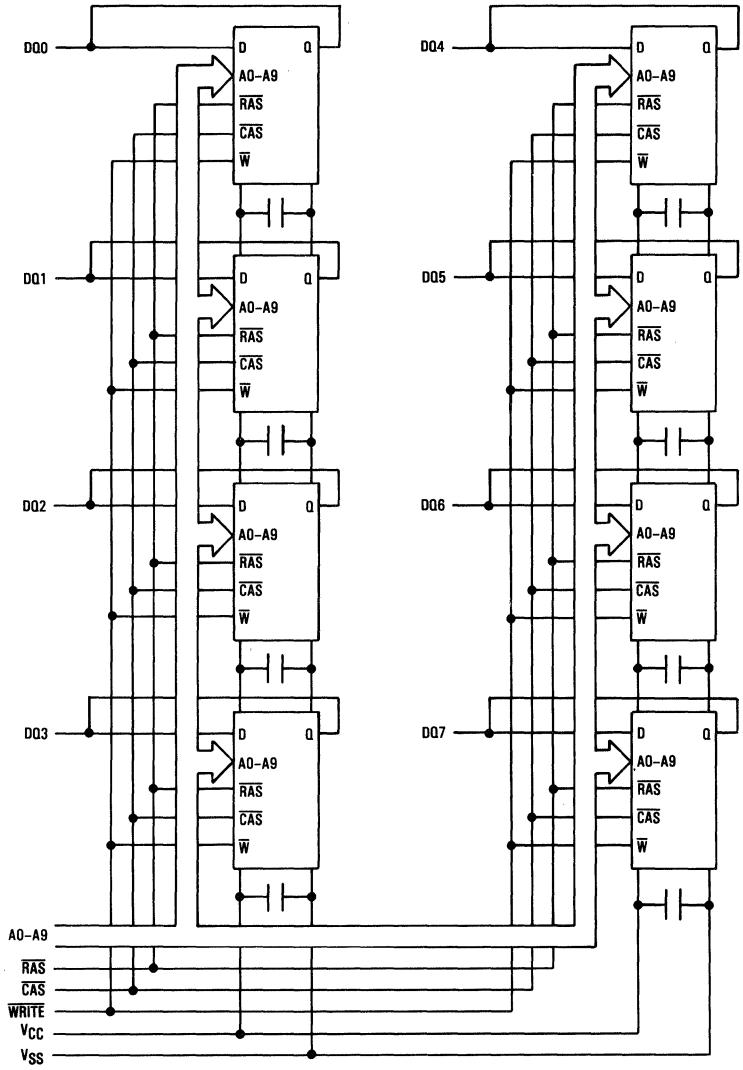


PIN NAMES	
A0-A9	Address Inputs
DQ0-DQ7	Data Input/Output
$\overline{CAS}$	Column Address Strobe
$\overline{RAS}$	Row Address Strobe
$\overline{W}$	Read/Write Input
V_{CC}	Power (+5 V)
V_{SS}	Ground
NC	No Connection

This document contains information on a new product. Specifications and information herein are subject to change without notice.

3

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−1 to +7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−1 to +7	V
Data Out Current per DQ Pin	I_{out}	50	mA
Power Dissipation	P_D	4.8	W
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V	1
	V_{SS}	0	0	0		
Logic High Voltage, All Inputs	V_{IH}	2.4	–	6.5	V	1
Logic Low Voltage, All Inputs	V_{IL}	−1.0	–	0.8	V	1

DC CHARACTERISTICS

Characteristic		Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current		I_{CC1}			mA	2
MCM81000-70, t_{RC} = 130 ns			–	640		
MCM81000-80, t_{RC} = 150 ns			–	560		
MCM81000-10, t_{RC} = 180 ns			–	480		
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}	–	16	mA	
V_{CC} Power Supply Current During $\overline{RAS}$ only Refresh Cycles		I_{CC3}			mA	2
MCM81000-70, t_{RC} = 130 ns			–	640		
MCM81000-80, t_{RC} = 150 ns			–	560		
MCM81000-10, t_{RC} = 180 ns			–	480		
V_{CC} Power Supply Current During Fast Page Mode Cycle		I_{CC4}			mA	2
MCM81000-70, t_{PC} = 40 ns			–	480		
MCM81000-80, t_{PC} = 45 ns			–	400		
MCM81000-10, t_{PC} = 55 ns			–	320		
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} − 0.2 V)	MCM81000	I_{CC5}	–	8	mA	
	MCM8L1000		–	1.6		
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle		I_{CC6}			mA	2
MCM81000-70, t_{RC} = 130 ns			–	640		
MCM81000-80, t_{RC} = 150 ns			–	560		
MCM81000-10, t_{RC} = 180 ns			–	480		
Input Leakage Current ($V_{SS} \le V_{in} \le V_{CC}$)		$I_{lkg(I)}$	−80	80	μA	
Output Leakage Current ($\overline{CAS}$ at Logic 1, $V_{SS} \le V_{out} \le V_{CC}$)		$I_{lkg(O)}$	−20	20	μA	
Output High Voltage (I_{OH} = −5 mA)		V_{OH}	2.4	–	V	
Output Low Voltage (I_{OL} = 4.2 mA)		V_{OL}	–	0.4	V	

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Max	Unit	Notes
Input Capacitance	A0-A9, $\overline{W}$, $\overline{CAS}$, $\overline{RAS}$	C_{in}	50	pF	3
Input/Output Capacitance	DQ0-DQ7	$C_{I/O}$	15	pF	3

NOTES:
1. All voltages referenced to V_{SS}.
2. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
3. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\Delta t/\Delta V$.

3

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ AND WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM81000-70		MCM81000-80		MCM81000-10		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	130	–	150	–	180	–	ns	5
Page Mode Cycle Time	t_{CELCEL}	t_{PC}	40	–	45	–	55	–	ns	
Access Time from $\overline{RAS}$	t_{RELQV}	t_{RAC}	–	70	–	80	–	100	ns	6, 7
Access Time from $\overline{CAS}$	t_{CELQV}	t_{CAC}	–	20	–	20	–	25	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	–	35	–	40	–	50	ns	6, 9
Access Time from Precharge $\overline{CAS}$	t_{CEHQV}	t_{CPA}	–	35	–	40	–	50	ns	6
$\overline{CAS}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	0	–	0	–	0	–	ns	6
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	20	0	20	0	20	ns	10
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{REHREL}	t_{RP}	50	–	60	–	70	–	ns	
$\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ Hold Time	t_{CELREH}	t_{RSH}	20	–	20	–	25	–	ns	
$\overline{CAS}$ Hold Time	t_{RELCEH}	t_{CSH}	70	–	80	–	100	–	ns	
$\overline{CAS}$ Pulse Width	t_{CELCEH}	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RELCEL}	t_{RCD}	20	50	20	60	25	75	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	35	15	40	20	50	ns	12
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	–	5	–	5	–	ns	
$\overline{CAS}$ Precharge Time (Page Mode Cycle Only)	t_{CEHCEL}	t_{CP}	10	–	10	–	10	–	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	–	0	–	0	–	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	–	10	–	15	–	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	–	0	–	0	–	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	–	15	–	20	–	ns	
Column Address Hold Time Referenced to $\overline{RAS}$	t_{RELAX}	t_{AR}	55	–	60	–	75	–	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{AVREH}	t_{RAL}	35	–	40	–	50	–	ns	

(continued)

NOTES:

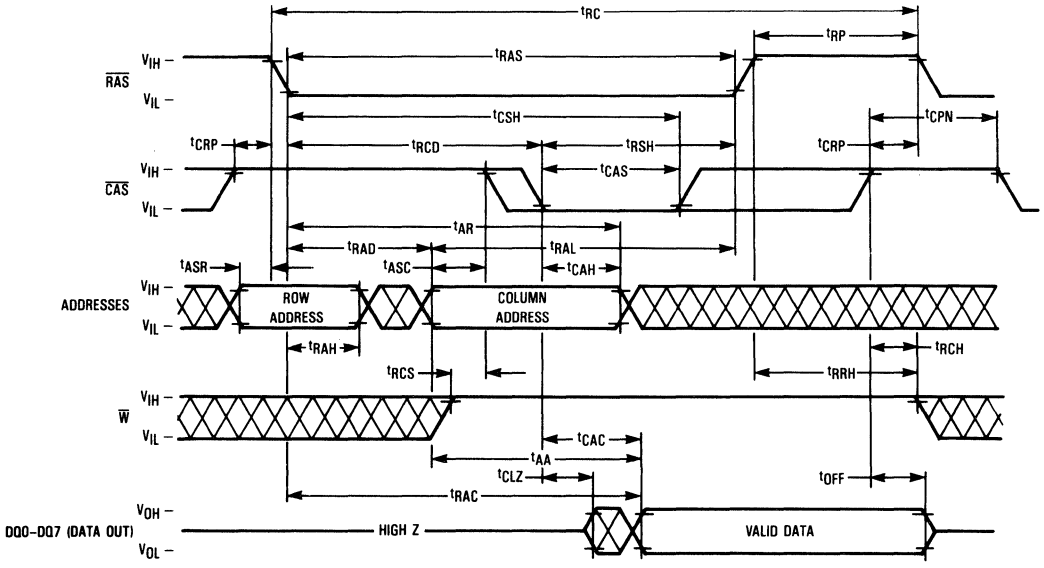
1. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
6. Measured with a current load equivalent to 2 TTL (−200 µA, +4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
8. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
9. Assumes that $t_{RAD} \geq t_{RAD}$ (max).
10. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
12. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.

READ AND WRITE CYCLES (Continued)

Parameter	Symbol		MCM81000-70		MCM81000-80		MC81000-10		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	–	0	–	0	–	ns	
Read Command Hold Time Referenced to $\overline{CAS}$	t_{CEHWX}	t_{RCH}	0	–	0	–	0	–	ns	13
Read Command Hold Time Referenced to $\overline{RAS}$	t_{REHWX}	t_{RRH}	0	–	0	–	0	–	ns	13
Write Command Hold Time Referenced to $\overline{CAS}$	t_{CELWH}	t_{WCH}	15	–	15	–	20	–	ns	
Write Command Hold Time Referenced to $\overline{RAS}$	t_{RELWH}	t_{WCR}	55	–	60	–	75	–	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	15	–	15	–	20	–	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{WLREH}	t_{RWL}	20	–	20	–	25	–	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{WLCEH}	t_{CWL}	20	–	20	–	25	–	ns	
Data in Setup Time	t_{DVCEL}	t_{DS}	0	–	0	–	0	–	ns	14, 15
Data in Hold Time	t_{CELDX}	t_{DH}	15	–	15	–	20	–	ns	14, 15
Data in Hold Time Referenced to $\overline{RAS}$	t_{RELDX}	t_{DHR}	55	–	60	–	75	–	ns	
Refresh Period MCM81000 MCM8L1000	t_{RVRV}	t_{RFSH}	– –	8 64	– –	8 64	– –	8 64	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	–	0	–	0	–	ns	15, 16
$\overline{CAS}$ Setup Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEL}	t_{CSR}	10	–	10	–	10	–	ns	
$\overline{CAS}$ Hold Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEH}	t_{CHR}	30	–	30	–	30	–	ns	
$\overline{CAS}$ Precharge to $\overline{CAS}$ Active Time	t_{REHCEL}	t_{RPC}	0	–	0	–	0	–	ns	
$\overline{CAS}$ Precharge Time for $\overline{CAS}$ Before $\overline{RAS}$ Counter Test	t_{CEHCEL}	t_{CPT}	40	–	40	–	50	–	ns	
$\overline{CAS}$ Precharge Time	t_{CEHCEL}	t_{CPN}	10	–	10	–	15	–	ns	

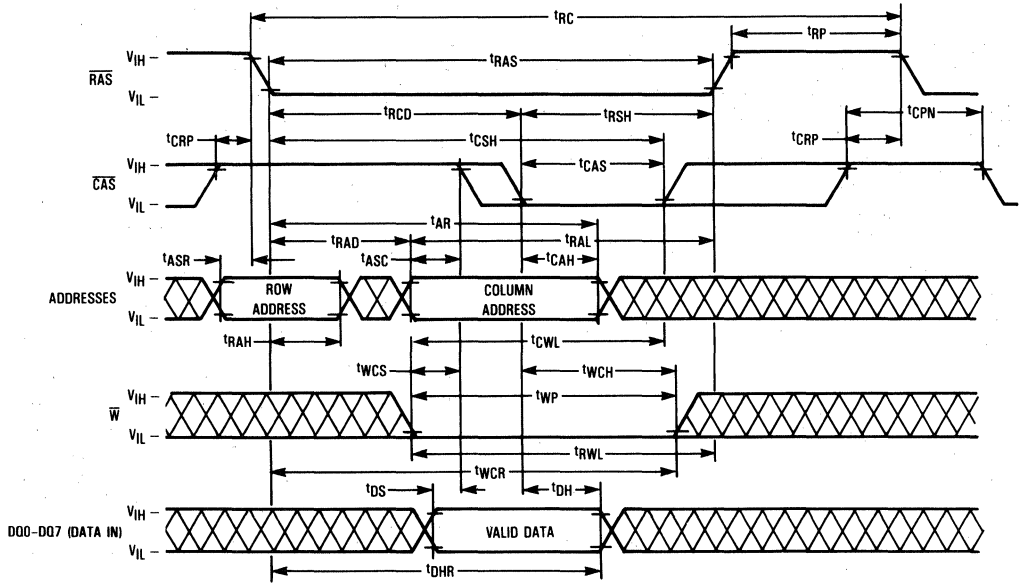
NOTES:
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles.
15. Early write only ($t_{WCS} \geq t_{WCS}$ (min)).
16. t_{WCS} is not a restrictive operating parameter. It is included in the data sheet as an electrical characteristic only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle. If this condition is not satisfied, the condition of the data out (at access time) is indeterminate.

READ CYCLE

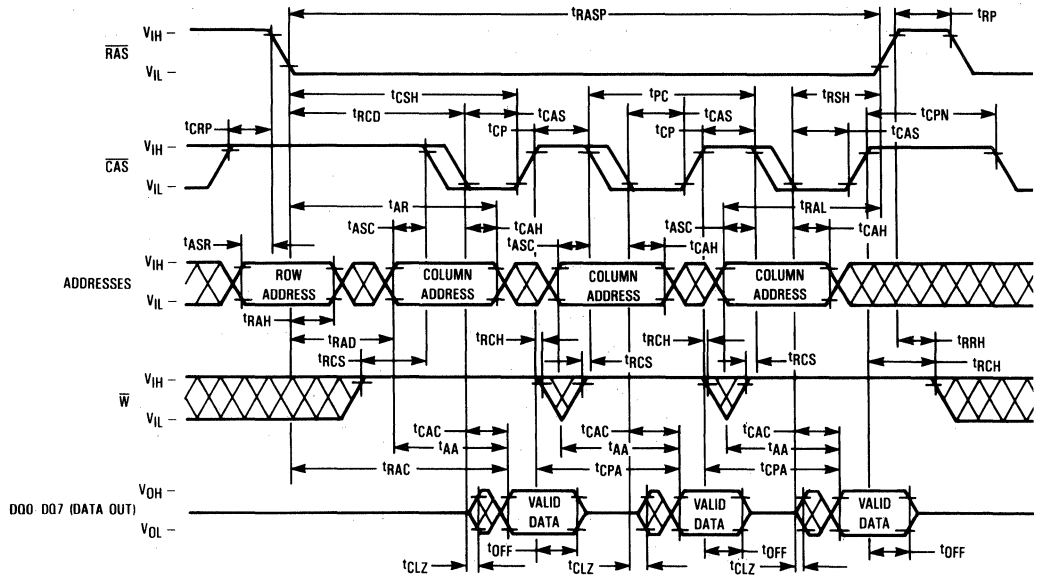


3

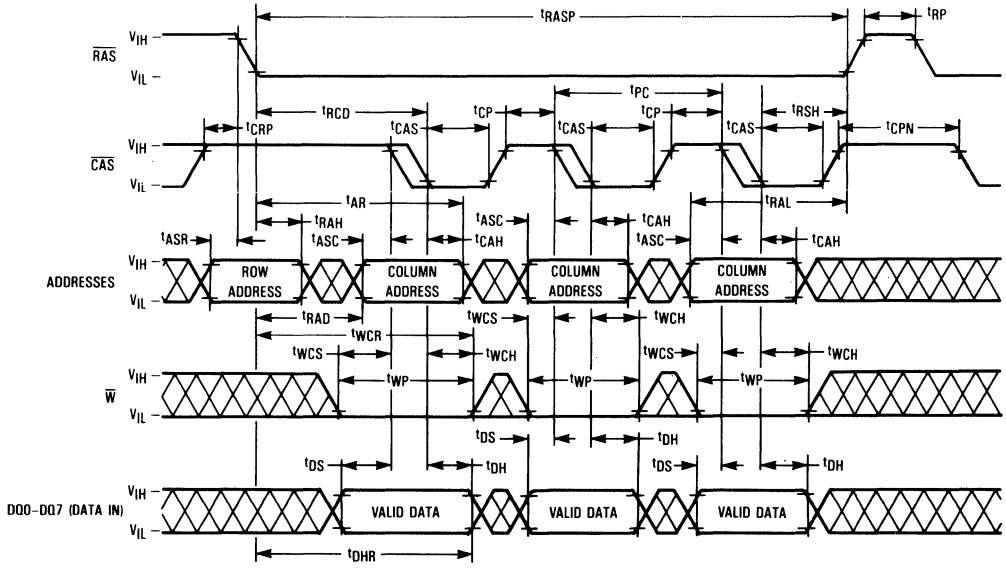
EARLY WRITE CYCLE



FAST PAGE MODE READ CYCLE

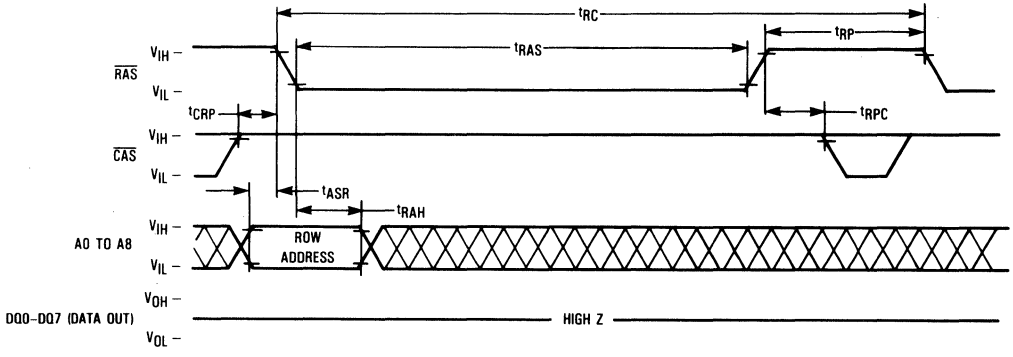


FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



RAS ONLY REFRESH CYCLE

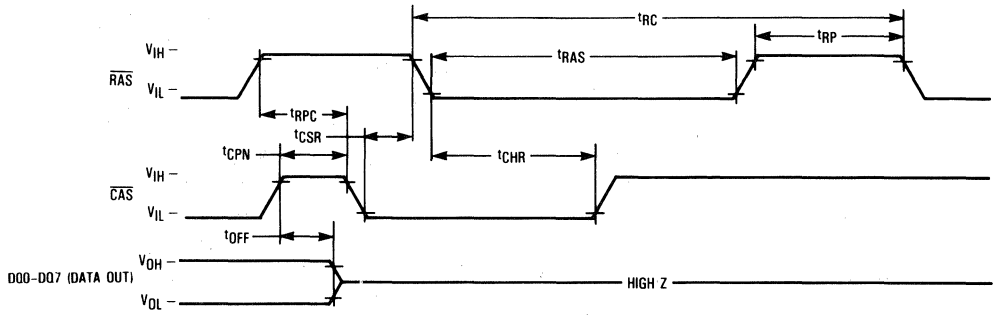
(W and A9 are Don't Care)



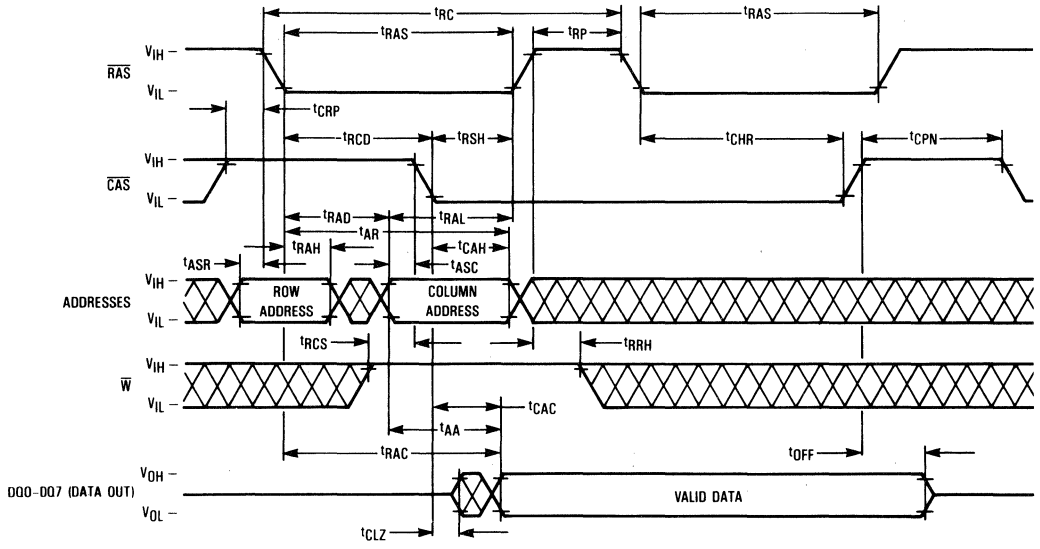
3

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

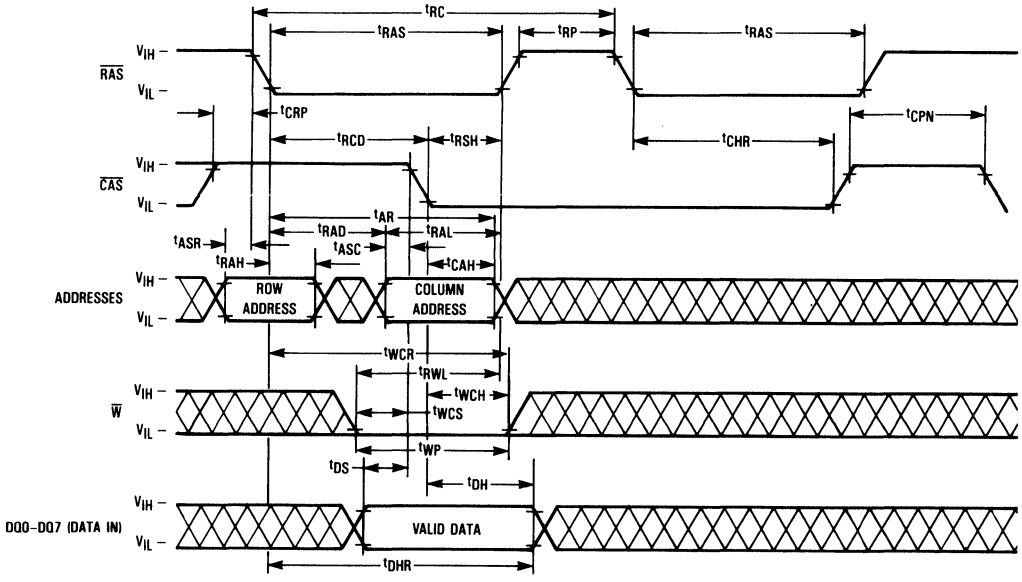
($\overline{W}$ and A0 to A9 are Don't Care)



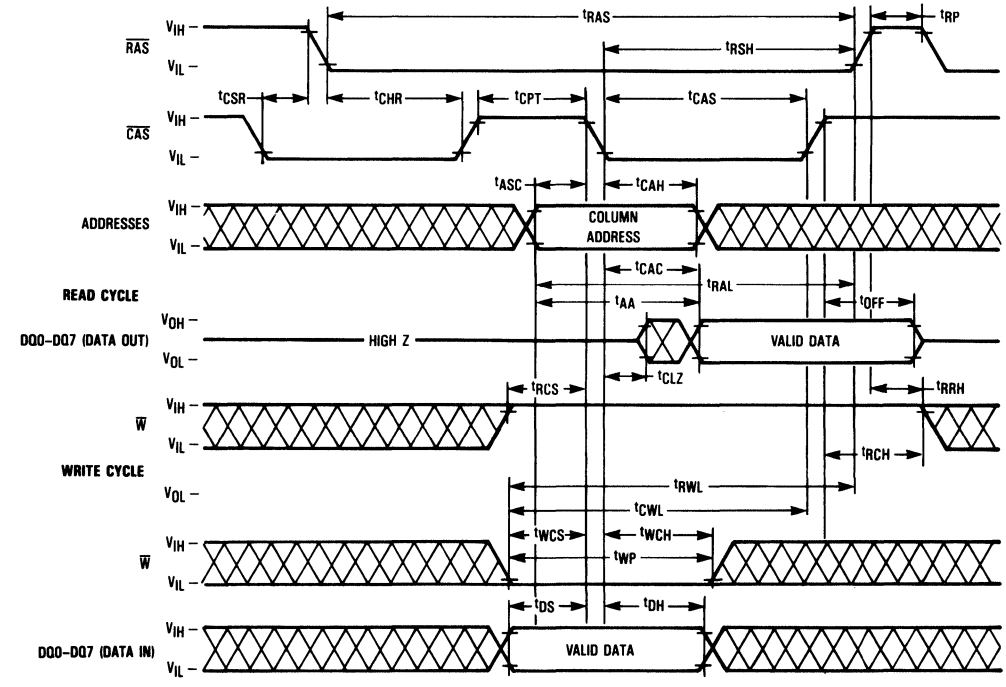
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



CAS BEFORE RAS REFRESH COUNTER TEST CYCLE



3

DEVICE INITIALIZATION

On power-up an initial pause of 200 microseconds is required for the internal substrate generator pump to establish the correct bias voltage. This is to be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize the various dynamic nodes internal to the device. During an extended inactive state of the device (greater than 4 milliseconds with device powered up), the wake up sequence (8 active cycles) will be necessary to assure proper device operation.

ADDRESSING THE RAM

The ten address bus pins on the device are time multiplexed with two separate 10-bit address fields that are strobed at the beginning of the memory cycle by two clocks (active negative) called the row address strobe ($\overline{RAS}$) and the column address strobe ($\overline{CAS}$). A total of twenty address bits will decode one of the 1,048,576 byte locations in the device. The column address strobe follows the row address strobe by a specified minimum and maximum time called "t_{RCD}," which is the row to column strobe delay. This time interval is also referred to as the multiplex window which gives flexibility to a system designer to set up his external addresses into the RAM. These conditions have to be met for normal read or write cycles. This initial portion of the cycle accomplishes the normal addressing of the device. There are, however, two other variations in addressing the 1M RAM module, one is called the $\overline{RAS}$ only refresh cycle (described later) where a 9-bit row address field is presented on the input pins and latched by the $\overline{RAS}$ clock. The most significant bit on Row Address A9 is not required for refresh. The other variation, which is called page mode, allows the user to column access all 1024 bytes within a selected row. (See **PAGE-MODE CYCLES** section.)

READ CYCLE

A read cycle is referred to as a normal read cycle to differentiate it from a page mode read cycle, which is covered in a later section.

The memory read cycle begins with the row addresses valid and the $\overline{RAS}$ clock transitioning from V_{IH} to the V_{IL} level. The $\overline{CAS}$ clock must also make a transition from V_{IH} to the V_{IL} level at the specified t_{RCD} timing limits when the column addresses are latched. Both the $\overline{RAS}$ and $\overline{CAS}$ clocks trigger a sequence of events which are controlled by several delayed internal clocks. Also, these clocks are linked in such a manner that the access time of the device is independent of the address multiplex window. The only stipulation is that the $\overline{CAS}$ clock must be active before or at the t_{RCD} maximum specification for an access (data valid) from the $\overline{RAS}$ clock edge to be guaranteed (t_{RAC}). If the t_{RCD} maximum condition is not met, the access (t_{CAC}) from the $\overline{CAS}$ clock active transition will determine read access time. The external $\overline{CAS}$ signal is ignored until an internal $\overline{RAS}$ signal is available. This gating feature on the $\overline{CAS}$ clock will allow the external $\overline{CAS}$ signal to become active as soon as the row address hold time (t_{RAH}) specification has been met and defines the t_{RCD} minimum specification. The time difference between t_{RCD} minimum and t_{RCD} maximum can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{CAS}$ clock.

Once the clocks have become active, they must stay active for the minimum (t_{RAS}) period for the $\overline{RAS}$ clock and the minimum (t_{CAS}) period for the $\overline{CAS}$ clock. The $\overline{RAS}$ clock must stay inactive for the minimum (t_{RP}) time. The former is for the completion of the cycle in progress, and the latter is for the device internal circuitry to be precharged for the next active cycle.

Data out is not latched and is valid as long as the $\overline{CAS}$ clock is active; the output will switch to the three-state mode when the $\overline{CAS}$ clock goes inactive. To perform a read cycle, the write ($\overline{W}$) input must be held at the V_{IH} level from the time the $\overline{CAS}$ clock makes its active transition (t_{RCS}) to the time when it transitions into the inactive (t_{RCH}) mode.

WRITE CYCLE

A write cycle is similar to a read cycle except that the Write ($\overline{W}$) clock must go active (V_{IL} level) at or before the $\overline{CAS}$ clock goes active at a minimum t_{WCS} time. If the above condition is met, then the cycle in progress is referred to as an early write cycle. In an early write cycle, the write clock and the data in are referenced to the active transition of the $\overline{CAS}$ clock edge. There are two important parameters with respect to the write cycle: the column strobe to write lead time (t_{CWL}) and the row strobe to write lead time (t_{RWL}). These define the minimum time that $\overline{RAS}$ and $\overline{CAS}$ clocks need to be active after the write operation has started ($\overline{W}$ clock at V_{IL} level).

PAGE-MODE CYCLES

Page mode operation allows fast successive data operations at all 1024 column locations on a selected row. Page access (t_{CAC}) is typically half the regular $\overline{RAS}$ clock access (t_{RAC}) on the Motorola 1M dynamic RAM. Page mode operation consists of holding the $\overline{RAS}$ clock active while cycling the $\overline{CAS}$ clock to access the column locations determined by the 10-bit column address field.

The page cycle is always initiated with a row address being provided and latched by the $\overline{RAS}$ clock, followed by the column address and $\overline{CAS}$ clock. From the timing illustrated, the initial cycle is a normal read or write cycle, that has been previously described, followed by the shorter $\overline{CAS}$ cycles (t_{PC}). The $\overline{CAS}$ cycle time (t_{PC}) consists of the $\overline{CAS}$ clock active time (t_{CAS}), and $\overline{CAS}$ clock precharge time (t_{CP}) and two transitions. In practice, any combination of read and write cycles can be performed to suit a particular application.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Therefore, to retain the correct information, the module needs to be refreshed at least once every 8 milliseconds. This is accomplished by sequentially cycling through the 512 row address locations every 8 milliseconds (i.e., at least one row every 15.6 microseconds). A normal read or write operation to the module will also refresh all the bytes (2048) associated with the particular row(s) decoded.

$\overline{RAS}$-Only Refresh

In this refresh method, the system must perform a $\overline{RAS}$-only cycle on 512 row addresses every 8 milliseconds. The row addresses are latched in with the $\overline{RAS}$ clock, and the associated internal row locations are refreshed. As the heading implies, the $\overline{CAS}$ clock is not required and must be inactive or at a V_{IH} level.

CAS Before RAS Refresh

This refresh cycle is initiated when RAS falls, after CAS has been low (by t_{CSR}). This activates the internal refresh counter which generates the row address to be refreshed. Externally applied addresses are ignored during the automatic refresh cycle. If the output buffer was off before the automatic refresh cycle, the output will stay in the high impedance state. If the output was enabled by CAS in the previous cycle, the data out will be maintained during the automatic refresh cycle as long as CAS is held active (hidden refresh).

Hidden Refresh

The hidden refresh method allows refresh cycles to be performed while maintaining valid data at the output pin. Hidden refresh is performed by holding CAS at V_{IL} and taking RAS high and after a specified precharge period (t_{RP}), executing a CAS before RAS refresh cycle. (See Figure 1.)

CAS BEFORE RAS REFRESH COUNTER TEST

The internal refresh counter of this device can be tested with a **CAS before RAS refresh counter test.** This refresh counter test is performed with read and write operations. During this test, the internal refresh counter generates the row address, while the external address input supplies the column address. The entire array is refreshed after 512 test cycles, as indicated by the check data written in each row. See **CAS before RAS refresh counter test cycle** timing diagram.

The test can be performed only after a minimum of **8 CAS before RAS** initialization cycles. The test procedure is as follows:

1. Write "0"s into all memory cells (normal write mode).
2. Select a column address, and read "0" out of the cell by performing **CAS before RAS refresh counter test, read cycle.** Repeat this operation 512 times.
3. Select a column address, and write "1" into the cell by performing **CAS before RAS refresh counter test, write cycle.** Repeat this operation 512 times.
4. Read "1"s (normal read mode), which were written at step 3.
5. Repeat steps 1 to 4 using complement data.

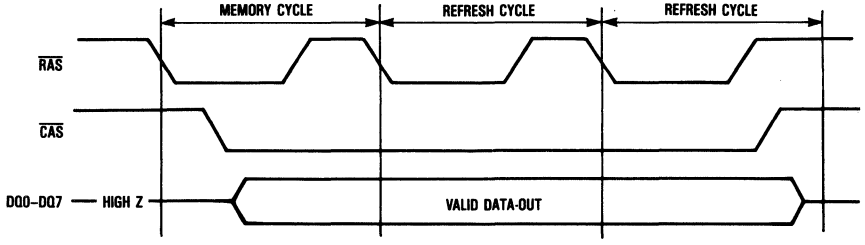
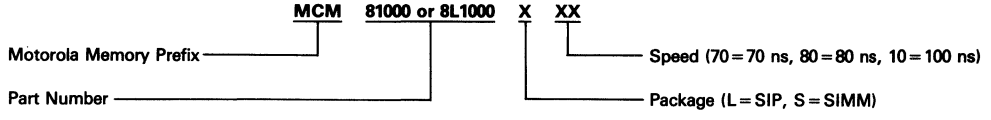


Figure 1. Hidden Refresh Cycle

ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers—	MCM81000L70	MCM81000S70
	MCM81000L80	MCM81000S80
	MCM81000L10	MCM81000S10
	MCM8L1000L70	MCM8L1000S70
	MCM8L1000L80	MCM8L1000S80
	MCM8L1000L10	MCM8L1000S10

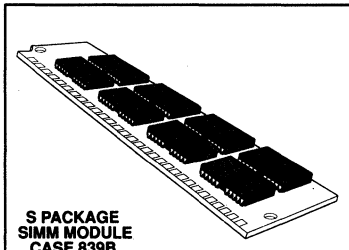
NOTE: Contact your Motorola representative for further information on the SIP package.

MCM84000
MCM8L4000

3

Advance Information

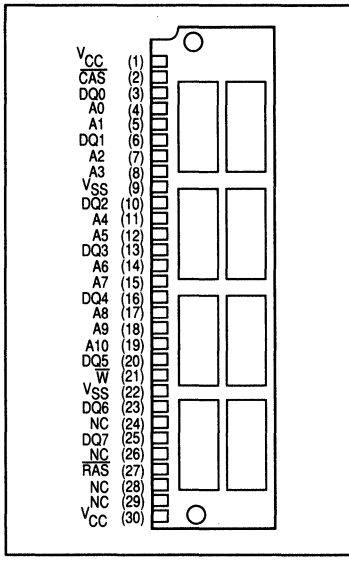
4M × 8 Bit Dynamic Random Access Memory Module



S PACKAGE
SIMM MODULE
CASE 839B

The MCM84000S is a 32M, dynamic random access memory (DRAM) module organized as 4,194,304 x 8 bits. The module is a 30-lead single-in-line memory module (SIMM) consisting of eight MCM514100 DRAMs housed in 20/26 J-lead small outline packages (SOJ) mounted on a substrate along with a 0.22 microfarad (min) decoupling capacitor mounted under each DRAM. The MCM514100 is a CMOS high speed, dynamic random access memory organized as 4,194,304 one-bit words and fabricated with CMOS silicon-gate process technology.

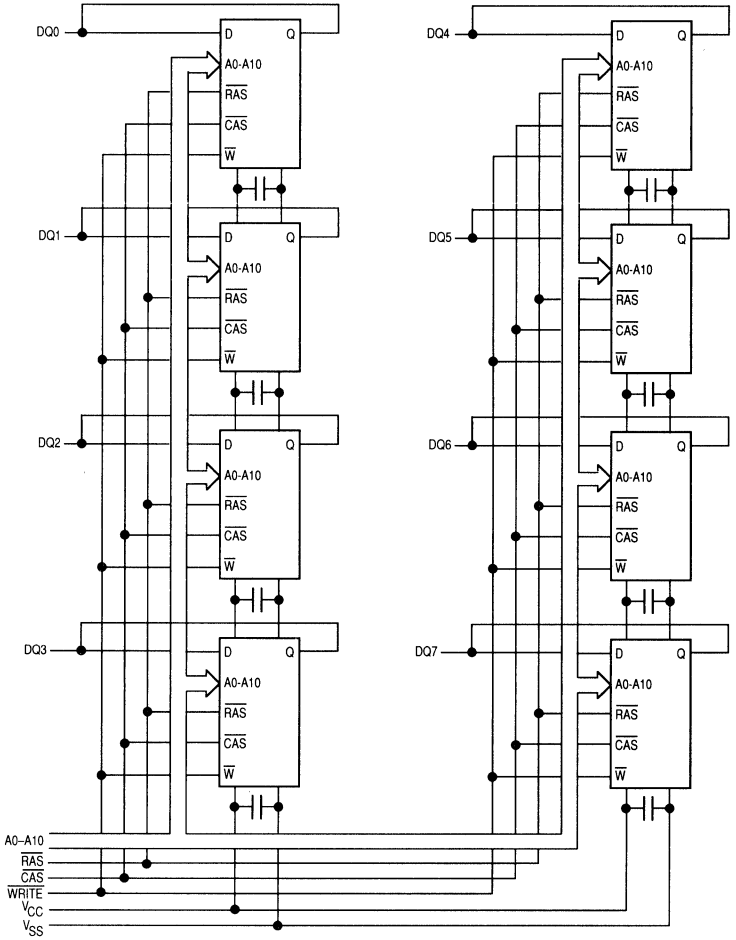
- Three-State Data Output
- Early-Write Common I/O Capability
- Fast Page Mode Capability
- TTL-Compatible Inputs and Outputs
- $\overline{RAS}$ Only Refresh
- $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- Hidden Refresh
- 1024 Cycle Refresh:
  MCM84000 = 16 ms
  MCM8L4000 = 128 ms
- Consists of Eight 4M x 1 DRAMs and Eight 0.22 µF (Min) Decoupling Capacitors
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}):
  MCM84000S-80 = 80 ns (Max)
  MCM84000S-10 = 100 ns (Max)
- Low Active Power Dissipation:
  MCM84000S-80 and MCM8L4000S-80 = 4.4 W (Max)
  MCM84000S-10 and MCM8L4000S-10 = 3.75 W (Max)
- Low Standby Power Dissipation:
  TTL Levels = 88 mW (Max)
  CMOS Levels (MCM84000) = 45 mW (Max)
  (MCM8L4000) = 18 mW (Max)
- $\overline{CAS}$ Control for Eight Common I/O Lines



PIN NAMES	
A0–A10	Address Inputs
DQ0–DQ7	Data Input/Output
$\overline{CAS}$	Column Address Strobe
$\overline{RAS}$	Row Address Strobe
$\overline{W}$	Read/Write Input
V_{CC}	Power (+5 V)
V_{SS}	Ground
NC	No Connection

This document contains information on a new product. Specifications and information herein are subject to change without notice.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−1 to +7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−1 to +7	V
Data Out Current per DQ Pin	I_{out}	50	mA
Power Dissipation	P_D	4.8	W
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

3

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V	1
	V_{SS}	0	0	0		
Logic High Voltage, All Inputs	V_{IH}	2.4	—	6.5	V	1
Logic Low Voltage, All Inputs	V_{IL}	-1.0	—	0.8	V	1

DC CHARACTERISTICS

Characteristic		Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current MCM84000–80, t_{RC} = 150 ns MCM84000–10, t_{RC} = 180 ns		I_{CC1}	 — —	 800 680	mA	2
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}	—	16	mA	
V_{CC} Power Supply Current During $\overline{RAS}$ Only Refresh Cycles MCM84000-80, t_{RC} = 150 ns MCM84000-10, t_{RC} = 180 ns		I_{CC3}	 — —	 800 680	mA	2
V_{CC} Power Supply Current During Fast Page Mode Cycle MCM84000-80, t_{PC} = 45 ns MCM84000-10, t_{PC} = 55 ns		I_{CC4}	 — —	 480 400	mA	2
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)	MCM84000 MCM8L4000	I_{CC5}	— —	8 3.2	mA	
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle MCM84000-80, t_{RC} = 150 ns MCM84000-10, t_{RC} = 180 ns		I_{CC6}	 — —	 800 680	mA	2
Input Leakage Current ($V_{SS} \leq V_{in} \leq V_{CC}$)		$I_{lkg(I)}$	–80	80	µA	
Output Leakage Current ($\overline{CAS}$ at Logic 1, $V_{SS} \leq V_{in} \leq V_{CC}$)		$I_{lkg(O)}$	–20	20	µA	
Output High Voltage (I_{OH} = –5 mA)		V_{OH}	2.4	—	V	
Output Low Voltage (I_{OL} = 4.2 mA)		V_{OL}	—	0.4	V	

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Max	Unit	Notes
Input Capacitance	A0–A10, $\overline{W}$, $\overline{CAS}$, $\overline{RAS}$	C_{in}	50	pF	3
Input/Output Capacitance	DQ0–DQ7	$C_{I/O}$	15	pF	3

NOTES:

1. All voltages referenced to V_{SS}.
2. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
3. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\Delta t/\Delta V$.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted

READ AND WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM84000-80		MCM84000-10		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	150	—	180	—	ns	5
Page Mode Cycle Time	t_{CELCEL}	t_{PC}	50	—	60	—	ns	
Access Time from $\overline{RAS}$	t_{RELQV}	t_{RAC}	—	80	—	100	ns	6, 7
Access Time from $\overline{CAS}$	t_{CELQV}	t_{CAC}	—	20	—	25	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	—	40	—	50	ns	6, 9
Access Time from Precharge $\overline{CAS}$	t_{CEHQV}	t_{CPA}	—	45	—	55	ns	6
$\overline{CAS}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	0	—	0	—	ns	6
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	20	0	20	ns	10
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{REHREL}	t_{RP}	60	—	70	—	ns	
$\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RAS}	80	10,000	100	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	80	200,000	100	200,000	ns	
$\overline{RAS}$ Hold Time	t_{CELREH}	t_{RSH}	20	—	25	—	ns	
$\overline{CAS}$ Hold Time	t_{RELCEH}	t_{CSH}	80	—	100	—	ns	
$\overline{CAS}$ Pulse Width	t_{CELCEH}	t_{CAS}	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RELCEL}	t_{RCD}	20	60	25	75	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	40	20	50	ns	12
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	—	10	—	ns	
$\overline{CAS}$ Precharge Time (Page Mode Cycle Only)	t_{CEHCEL}	t_{CP}	10	—	10	—	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	—	15	—	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	—	20	—	ns	
Column Address Hold Time Referenced to $\overline{RAS}$	t_{RELAX}	t_{AR}	60	—	75	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{AVREH}	t_{RAL}	40	—	50	—	ns	

(continued)

NOTES:

1. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
6. Measured with a current load equivalent to 2 TTL (–200 µA, +4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
8. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
9. Assumes that $t_{RAD} \geq t_{RAD}$ (max).
10. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
12. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.

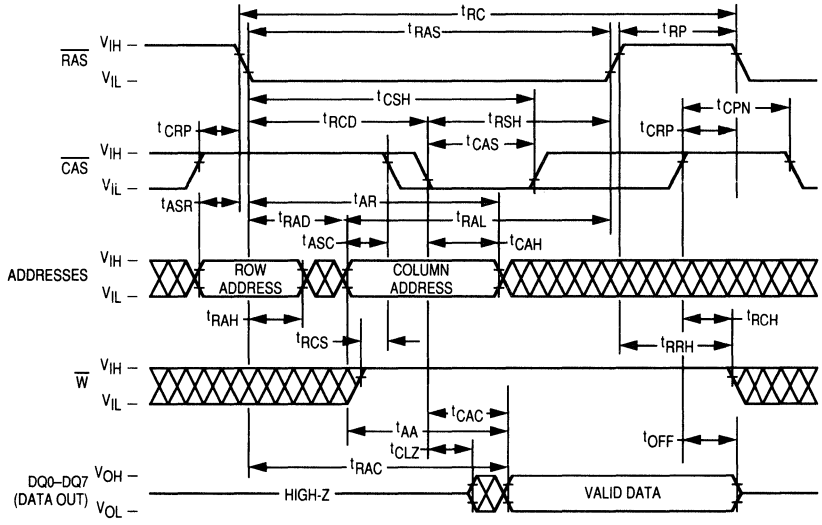
READ AND WRITE CYCLES (Continued)

Parameter	Symbol		MCM84000-80		MCM84000-10		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	0	—	ns	
Read Command Hold Time Referenced to $\overline{CAS}$	t_{CEHWX}	t_{RCH}	0	—	0	—	ns	13
Read Command Hold Time Referenced to $\overline{RAS}$	t_{REHWX}	t_{RRH}	0	—	0	—	ns	13
Write Command Hold Time Referenced to $\overline{CAS}$	t_{CELWH}	t_{WCH}	15	—	20	—	ns	
Write Command Hold Time Reference to $\overline{RAS}$	t_{RELWH}	t_{WCR}	60	—	75	—	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	15	—	20	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{WLREH}	t_{RWL}	20	—	25	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{WLCEH}	t_{CWL}	20	—	25	—	ns	
Data in Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	ns	14, 15
Data in Hold Time	t_{CELDX}	t_{DH}	15	—	20	—	ns	14, 15
Data in Hold Time Referenced to $\overline{RAS}$	t_{RELDX}	t_{DHR}	60	—	75	—	ns	
Refresh Period MCM84000 MCM8L4000	t_{RVRV}	t_{RFSH}	— —	16 128	— —	16 128	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	—	0	—	ns	15, 16
$\overline{CAS}$ Setup Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEL}	t_{CSR}	5	—	10	—	ns	
$\overline{CAS}$ Hold Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEH}	t_{CHR}	15	—	20	—	ns	
$\overline{CAS}$ Precharge to $\overline{CAS}$ Active Time	t_{REHCEL}	t_{RPC}	0	—	0	—	ns	
$\overline{CAS}$ Precharge Time for $\overline{CAS}$ Before $\overline{RAS}$ Counter Test	t_{CEHCEL}	t_{CPT}	40	—	50	—	ns	
$\overline{CAS}$ Precharge Time	t_{CEHCEL}	t_{CPN}	10	—	10	—	ns	

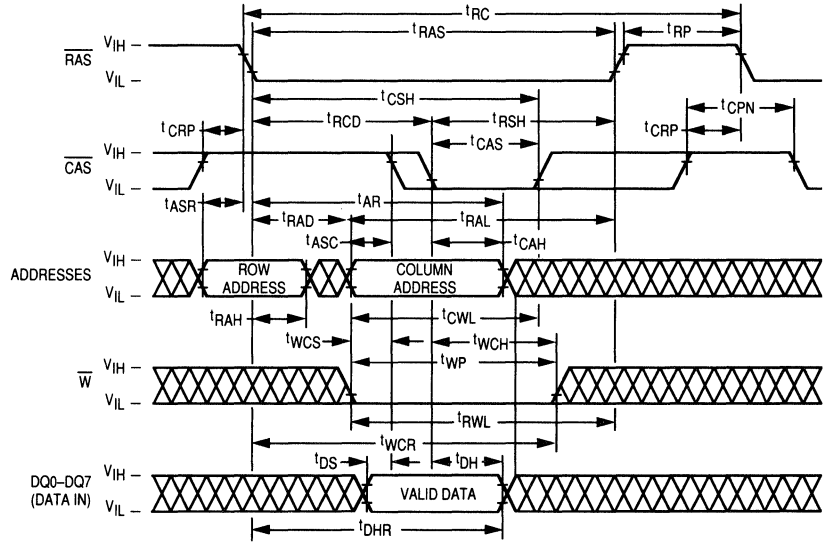
NOTES:

13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. These parameters are reference to $\overline{CAS}$ leading edge in random write cycles.
15. Early write only ($t_{WCS} \geq t_{WCS}$ (min)).
16. t_{WCS} is not a restrictive operating parameter. It is included in the data sheet as an electrical characteristic only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle. If this condition is not satisfied, the condition of the data out (at access time) is indeterminate.

READ CYCLE

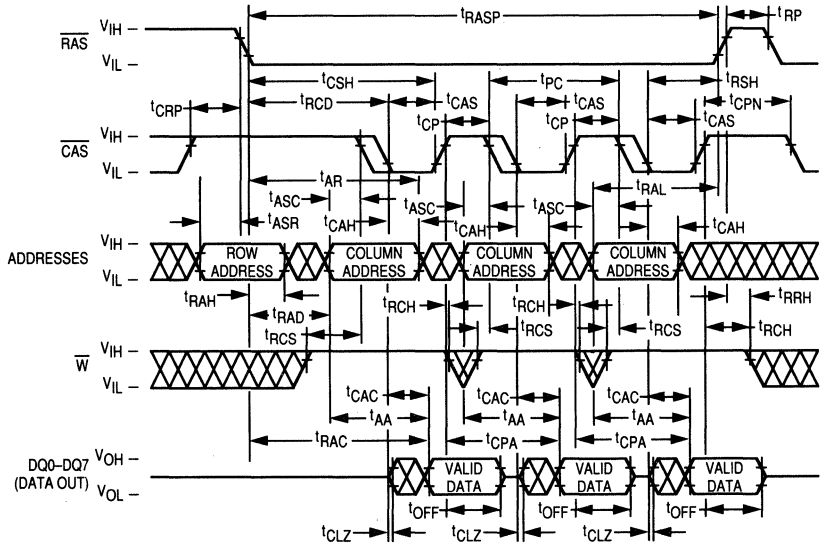


EARLY WRITE CYCLE

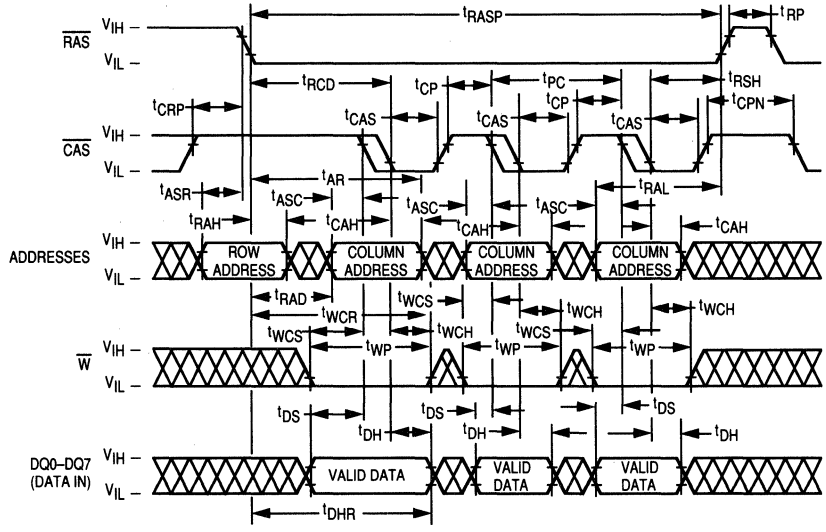


3

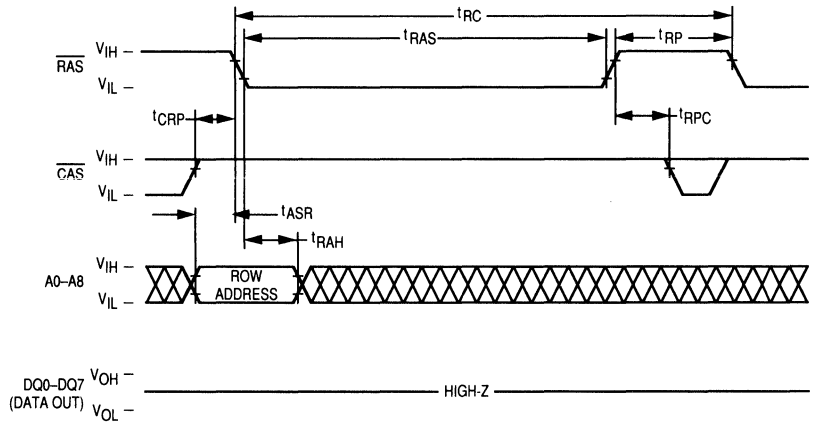
FAST PAGE MODE READ CYCLE



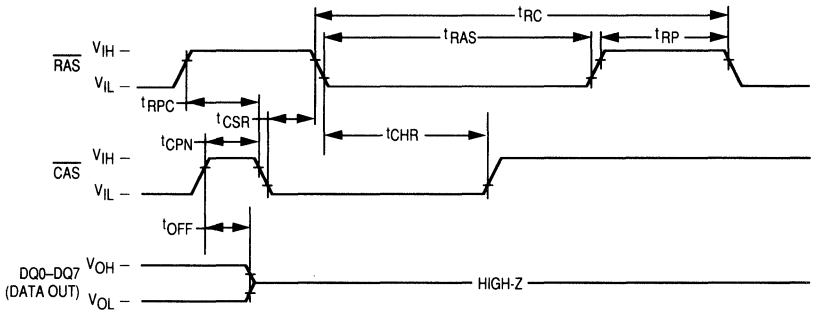
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



$\overline{RAS}$ ONLY REFRESH CYCLE
($\overline{W}$ and A10 are Don't Care)

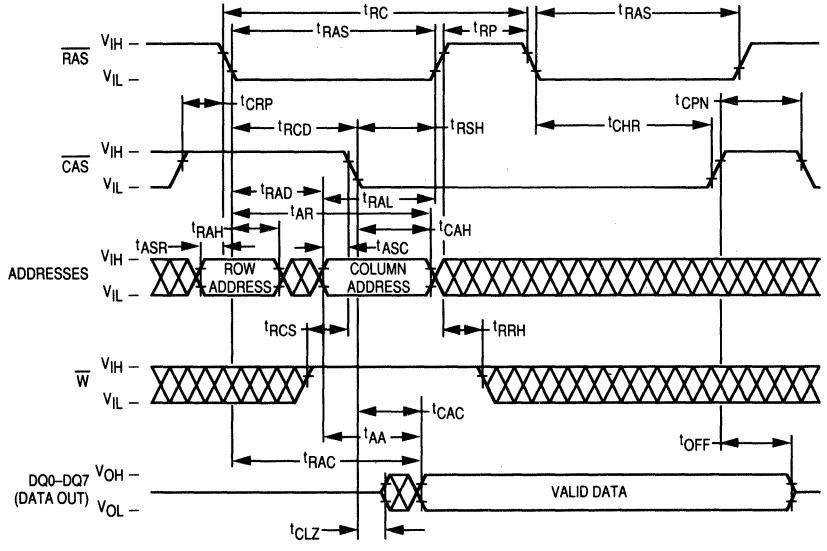


$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE
($\overline{W}$ and A0 to A10 are Don't Care)

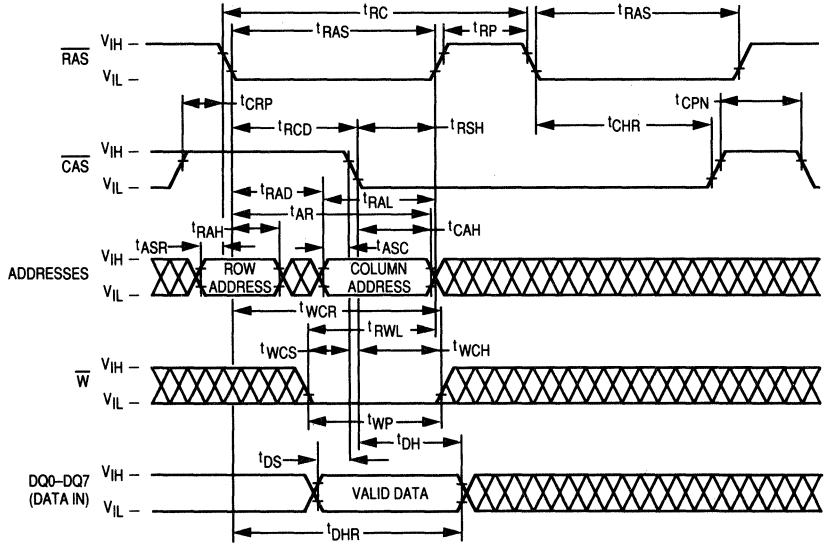


3

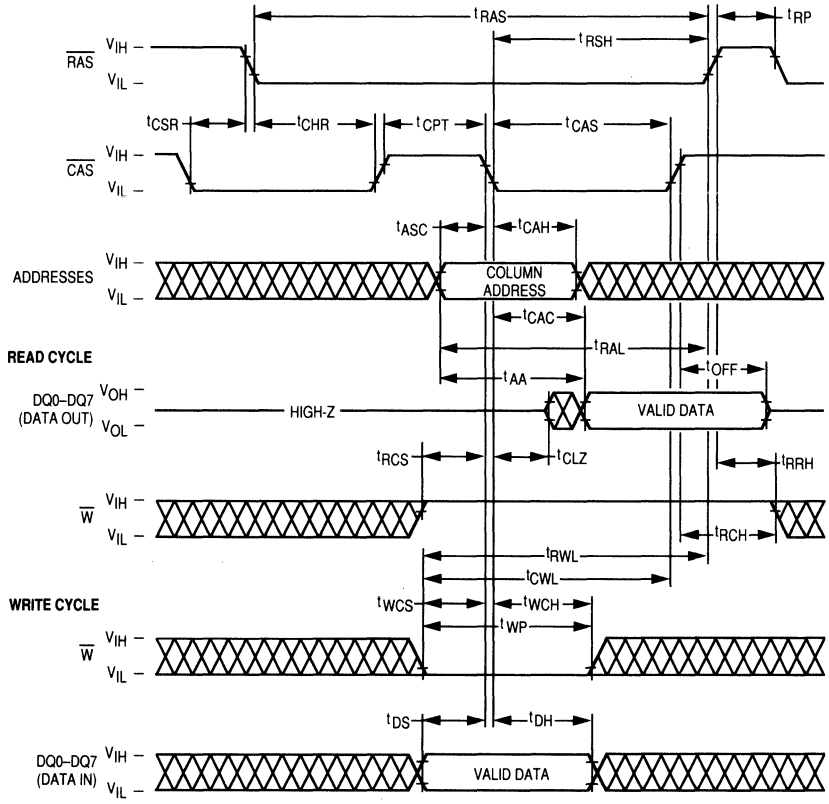
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



3

DEVICE INITIALIZATION

On power-up an initial pause of 200 microseconds is required for the internal substrate generator pump to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize all dynamic nodes within the RAM. During an extended inactive state (greater than 16 milliseconds with device powered up), a wake up sequence of eight active cycles is necessary to assure proper operation.

ADDRESSING THE RAM

The eleven address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks, row address strobe ($\overline{RAS}$) and column address strobe ($\overline{CAS}$), into two separate 11-bit address fields. A total of twenty two address bits, eleven rows and eleven columns, will decode one of the 4,194,304 byte locations in the device. $\overline{RAS}$ active transition is followed by $\overline{CAS}$ active transition (active = V_{IL}, t_{RCD} minimum) for all read or write cycles. The delay between $\overline{RAS}$ and $\overline{CAS}$ active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

The external $\overline{CAS}$ signal is ignored until an internal $\overline{RAS}$ signal is available. This "gate" feature on the external $\overline{CAS}$ clock enables the internal $\overline{CAS}$ line as soon as the row address hold time (t_{RAH}) specification is met (and defines t_{RCD} minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{CAS}$ clock.

There are three other variations in addressing the 4M RAM: **$\overline{RAS}$ only refresh cycle**, **$\overline{CAS}$ before $\overline{RAS}$ refresh cycle**, and **page mode.** All three are discussed in separate sections that follow.

READ CYCLE

The DRAM may be read with two different cycles: "normal" random read cycle and page mode read cycle. The normal read cycle is outlined here, while the page mode cycle is discussed in a separate section.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with the $\overline{RAS}$ and $\overline{CAS}$ active transitions latching the desired bit location. The write ($\overline{W}$) input level must be high (V_{IH}), t_{RCS} (minimum) before the $\overline{CAS}$ active transition, to enable read mode.

Both the $\overline{RAS}$ and $\overline{CAS}$ clocks trigger a sequence of events which are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window. However, $\overline{CAS}$ must be active before or at t_{RCD} maximum to guarantee valid data out (Q) at t_{RAC} (access time from $\overline{RAS}$ active transition). If the t_{RCD} maximum is exceeded, read access time is determined by the $\overline{CAS}$ clock active transition (t_{CAC}).

The $\overline{RAS}$ and $\overline{CAS}$ clocks must remain active for a minimum time of t_{RAS} and t_{CAS} respectively, to complete the read cycle. $\overline{W}$ must remain high throughout the cycle, and for time t_{RRH} or t_{RCH} after $\overline{RAS}$ or $\overline{CAS}$ inactive transition, respectively, to maintain the data at that bit location. Once $\overline{RAS}$ transitions to inactive, it must remain inactive for a minimum time of t_{RP} to precharge the internal device circuitry for the next active cycle. Q is valid, but not latched, as long as the $\overline{CAS}$ clock is active. When the $\overline{CAS}$ clock transitions to inactive, the output will switch to High Z (three-state).

WRITE CYCLE

The user can write to the DRAM with two cycles; early write and page mode early write. Early write mode is discussed here, while the page mode write operation is covered in another section.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of $\overline{W}$ to active (V_{IL}). Minimum active time t_{RAS} and t_{CAS}, and precharge time t_{RP} apply to write mode, as in the read mode.

An early write cycle is characterized by $\overline{W}$ active transition at minimum time t_{WCS} before $\overline{CAS}$ active transition. Data in (D) is referenced to $\overline{CAS}$ in an early write cycle. $\overline{RAS}$ and $\overline{CAS}$ clocks must stay active for t_{RWL} and t_{CWL}, respectively, after the start of the early write operation to complete the cycle.

Q remains in three-state condition throughout an early write cycle because $\overline{W}$ active transition precedes or coincides with $\overline{CAS}$ active transition, keeping data-out buffers disabled.

PAGE-MODE CYCLES

Page mode allows fast successive data operations at all 2048 column locations on a selected row of the dynamic RAM. Read access time in page mode (t_{CAC}) is typically half the regular $\overline{RAS}$ clock access time, t_{RAC}. Page mode operation consists of keeping $\overline{RAS}$ active while toggling $\overline{CAS}$ between V_{IH} and V_{IL}. The row is latched by $\overline{RAS}$ active transition, while each $\overline{CAS}$ active transition allows selection of a new-column location on the row.

A page mode cycle is initiated by a normal read or write cycle, as described in prior sections. Once the timing requirements for the first cycle are met, $\overline{CAS}$ transitions to inactive for minimum of t_{CP}, while $\overline{RAS}$ remains low (V_{IL}). The second $\overline{CAS}$ active transition while $\overline{RAS}$ is low initiates the first page mode cycle (t_{PC} or t_{PRWC}). Either a read or write operation can be performed in a page mode cycle, subject to the same conditions as in normal operation (previously described). These operations can be intermixed in consecutive page mode cycles and performed in any order. The maximum number of consecutive page mode cycles is limited by t_{RASP}. Page mode operation is ended when $\overline{RAS}$ transitions to inactive, coincident with or following $\overline{CAS}$ inactive transition.

REFRESH CYCLES

The dymanic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Each byte must be periodically **refreshed** (recharged) to maintain the correct byte state. Bytes in the MCM84000 require refresh every 16 milliseconds, while refresh time for the MCM8L4000 is 128 milliseconds.

This is accomplished by cycling through the 1024 row addresses in sequence within the specified refresh time. All the bytes on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every

A normal read, write, or read-write operation to the RAM will refresh all the bytes (4096) associated with the particular row decoded. Three other methods of refresh, **RAS-only refresh**, **CAS before RAS refresh**, and **hidden refresh** are available on this device for greater system flexibility.

RAS-Only Refresh

RAS-only refresh consists of RAS transition to active, latching the row address to be refreshed, while CAS remains high (V_{IH}) throughout the cycle. An external counter is employed to ensure all rows are refreshed within the specified limit.

CAS Before RAS Refresh

CAS before RAS refresh is enabled by bring CAS active before RAS. This clock order activates an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle. The output buffer remains at the same state it was in during the previous cycle (hidden refresh).

Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding CAS active the end of a read or write cycle, while RAS cycles inactive for t_{RP} and back to active, starts the hidden refresh. This is essentially the execution of a CAS before RAS refresh from a cycle in progress (see Figure 1).

CAS BEFORE RAS REFRESH COUNTER TEST

The internal refresh counter of this device can be tested with a **CAS before RAS refresh counter test.** This test is performed with a read-write operation. During the test, the internal refresh counter generates the row address, while the external address supplies the column address. The entire array is refreshed after 1024 cycles, as indicated by the check data written in each row. See **CAS before RAS refresh counter test cycle** timing diagram.

The test can be performed after a minimum of **8 CAS before RAS** initialization cycles. Test procedure:

1. Write "0"s into all memory cells (normal write mode).
2. Select a column address, and read "0" out of the cell by performing **CAS before RAS refresh counter test, read cycle.** Repeat this operation 1024 times.
3. Select a column address, and write "1" into the cell by performing **CAS before RAS refresh counter test, write cycle.** Repeat this operation 1024 times.
4. Read "1"s (normal read mode), which were written at step 3.
5. Repeat steps 1 to 4 using complement data.

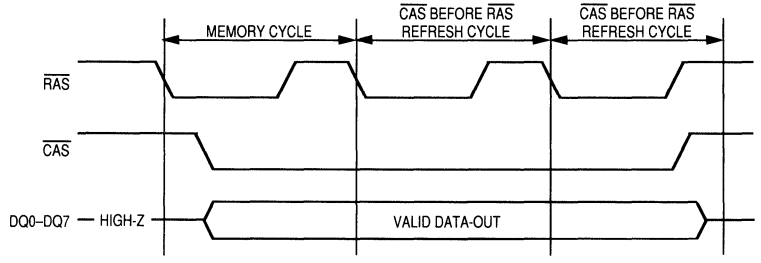
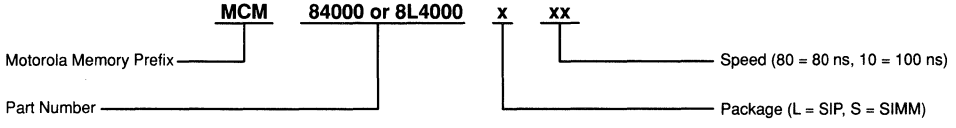


Figure 1. Hidden Refresh Cycle

ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers – MCM84000L80 MCM84000S80
MCM84000L10 MCM84000S10

MCM8L4000L80 MCM8L4000S80
MCM8L4000L10 MCM8L4000S10

NOTE: Contact your Motorola Representative for further information on the SIP package.

3

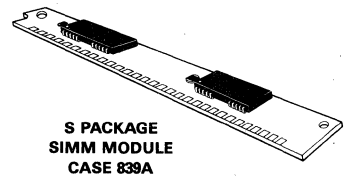
MCM84256
MCM8L4256

Advance Information

256K x 8 Bit Dynamic Random Access Memory Module

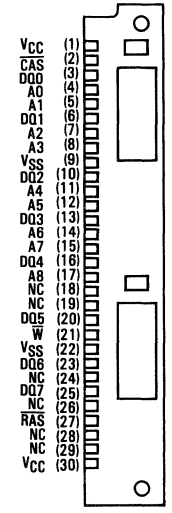
The MCM84256 is a 2M, dynamic random access memory (DRAM) module organized as 262,144 x 8 bits. The module is a 30-lead single-in-line memory module (SIMM) consisting of two MCM514256A DRAMs housed in 20/26 J-lead small outline packages (SOJ) and mounted on a substrate along with a 0.22 μF (min) decoupling capacitor mounted adjacent to each DRAM. The MCM514256A is a 1.0μ CMOS high speed, dynamic random access memory organized as 262,144 four-bit words and fabricated with CMOS silicon-gate process technology.

- Three-State Data Output
- Early-Write Common I/O Capability
- Fast Page Mode Capability
- TTL-Compatible Inputs and Outputs
- $\overline{RAS}$ Only Refresh
- $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- Hidden Refresh
- 512 Cycle Refresh:
  - MCM84256 = 8 ms (Max)
  - MCM8L4256 = 64 ms (Max)
- Consists of Two 256K x 4 DRAMs and Two 0.22 μF (Min) Decoupling Capacitors
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}):
  - MCM84256-70 = 70 ns (Max)
  - MCM84256-80 = 80 ns (Max)
  - MCM84256-10 = 100 ns (Max)
- Low Active Power Dissipation:
  - MCM84256-70 = 0.9 W (Max)
  - MCM84256-80 = 0.8 W (Max)
  - MCM84256-10 = 0.7 W (Max)
- Low Standby Power Dissipation:
  - TTL Levels = 22 mW (Max)
  - CMOS Levels (MCM84256) = 11 mW (Max)
    (MCM8L4256) = 2.2 mW (Max)
- $\overline{CAS}$ Control for Eight Common I/O Lines
- Available in Edge Connector



S PACKAGE
SIMM MODULE
CASE 839A

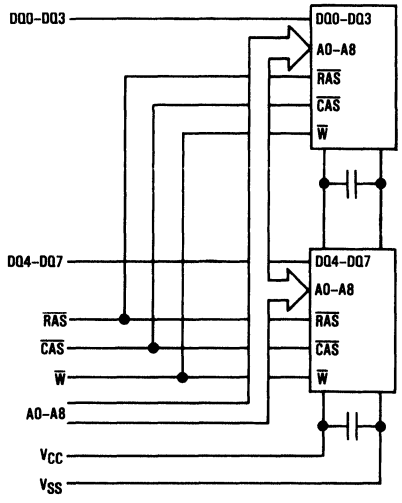
30-PIN
SINGLE IN-LINE PACKAGE
(TOP VIEW, MCM84256S/8L4256S)



PIN NAMES	
A0-A8	Address Inputs
DQ0-DQ7	Data Input/Output
$\overline{CAS}$	Column Address Strobe
$\overline{RAS}$	Row Address Strobe
$\overline{W}$	Read/Write Input
V_{CC}	Power (+5 V)
V_{SS}	Ground
NC	No Connection

This document contains information on a new product. Specifications and information herein are subject to change without notice.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−1 to +7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−1 to +7	V
Data Out Current per DQ Pin	I_{out}	50	mA
Power Dissipation	P_D	2	W
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V	1
	V_{SS}	0	0	0		
Logic High Voltage, All Inputs	V_{IH}	2.4	–	6.5	V	1
Logic Low Voltage, All Inputs	V_{IL}	−1.0	–	0.8	V	1

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current	I_{CC1}			mA	2
MCM84256-70, t_{RC} = 130 ns		–	160		
MCM84256-80, t_{RC} = 150 ns		–	140		
MCM84256-10, t_{RC} = 180 ns		–	120		
V_{CC} Power Supply Current (Standby) ($\overline{RAS} = \overline{CAS} = V_{IH}$)	I_{CC2}	–	4	mA	
V_{CC} Power Supply Current During $\overline{RAS}$ only Refresh Cycles	I_{CC3}			mA	2
MCM84256-70, t_{RC} = 130 ns		–	160		
MCM84256-80, t_{RC} = 150 ns		–	140		
MCM84256-10, t_{RC} = 180 ns		–	120		
V_{CC} Power Supply Current During Fast Page Mode Cycle	I_{CC4}			mA	2
MCM84256-70, t_{PC} = 40 ns		–	120		
MCM84256-80, t_{PC} = 45 ns		–	100		
MCM84256-10, t_{PC} = 55 ns		–	80		
V_{CC} Power Supply Current (Standby) ($\overline{RAS} = \overline{CAS} = V_{CC} - 0.2$ V) MCM84256	I_{CC5}	–	2	mA	
MCM8L4256		–	400	µA	
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle	I_{CC6}			mA	2
MCM84256-70, t_{RC} = 130 ns		–	160		
MCM84256-80, t_{RC} = 150 ns		–	140		
MCM84256-10, t_{RC} = 180 ns		–	120		
Input Leakage Current ($V_{SS} \le V_{in} \le V_{CC}$)	$I_{lkg(I)}$	−20	20	µA	
Output Leakage Current ($\overline{CAS}$ at Logic 1, $V_{SS} \le V_{out} \le V_{CC}$)	$I_{lkg(O)}$	−10	10	µA	
Output High Voltage (I_{OH} = −5 mA)	V_{OH}	2.4	–	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	–	0.4	V	

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Max	Unit	Notes
Input Capacitance	A0-A8, $\overline{W}$, $\overline{CAS}$, $\overline{RAS}$	C_{in}	20	pF	3
Input/Output Capacitance	DQ0-DQ7	$C_{I/O}$	15	pF	3

NOTES:
1. All voltages referenced to V_{SS}.
2. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
3. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\Delta t/\Delta V$.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ AND WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM84256-70		MCM84256-80		MCM84256-10		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	130	–	150	–	180	–	ns	5
Page Mode Cycle Time	t_{CELCEL}	t_{PC}	40	–	45	–	55	–	ns	
Access Time from $\overline{RAS}$	t_{RELQV}	t_{RAC}	–	70	–	80	–	100	ns	6, 7
Access Time from $\overline{CAS}$	t_{CELQV}	t_{CAC}	–	20	–	20	–	25	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	–	35	–	40	–	50	ns	6, 9
Access Time from Precharge $\overline{CAS}$	t_{CEHQV}	t_{CPA}	–	35	–	40	–	50	ns	6
$\overline{CAS}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	0	–	0	–	0	–	ns	6
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	20	0	20	0	20	ns	10
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{REHREL}	t_{RP}	50	–	60	–	70	–	ns	
$\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ Hold Time	t_{CELREH}	t_{RSH}	20	–	20	–	25	–	ns	
$\overline{CAS}$ Hold Time	t_{RELCEH}	t_{CSH}	70	–	80	–	100	–	ns	
$\overline{CAS}$ Pulse Width	t_{CELCEH}	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RELCEL}	t_{RCD}	20	50	20	60	25	75	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	35	15	40	20	50	ns	12
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	–	5	–	10	–	ns	
$\overline{CAS}$ Precharge Time (Page Mode Cycle Only)	t_{CEHCEL}	t_{CP}	10	–	10	–	10	–	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	–	0	–	0	–	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	–	10	–	15	–	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	–	0	–	0	–	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	–	15	–	20	–	ns	
Column Address Hold Time Referenced to $\overline{RAS}$	t_{RELAX}	t_{AR}	55	–	60	–	75	–	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{AVREH}	t_{RAL}	35	–	40	–	50	–	ns	

(continued)

NOTES:

1. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
6. Measured with a current load equivalent to 2 TTL (−200 μA, +4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
8. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
9. Assumes that $t_{RAD} \geq t_{RAD}$ (max).
10. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
12. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.

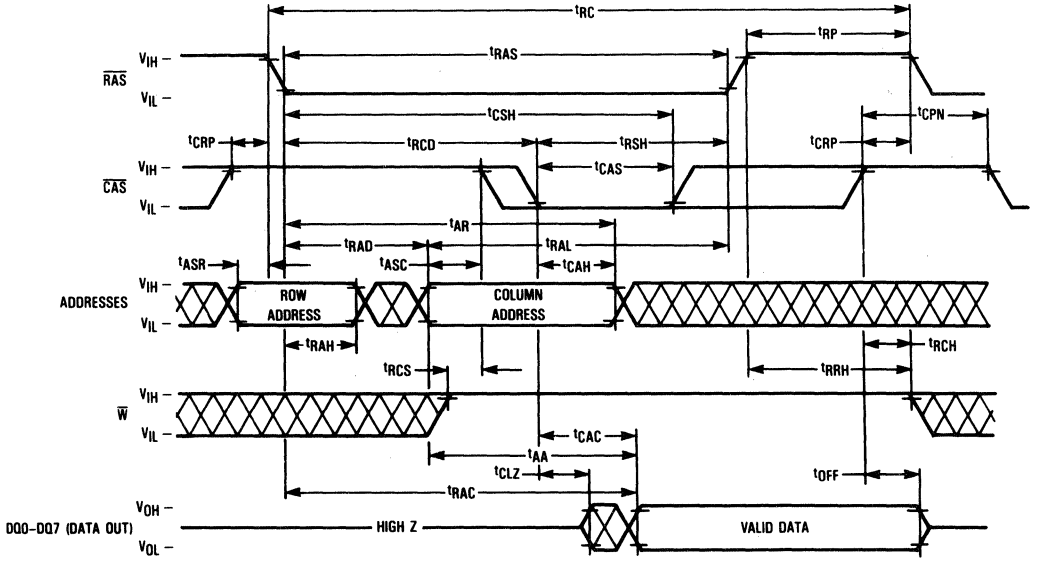
3

READ AND WRITE CYCLES (Continued)

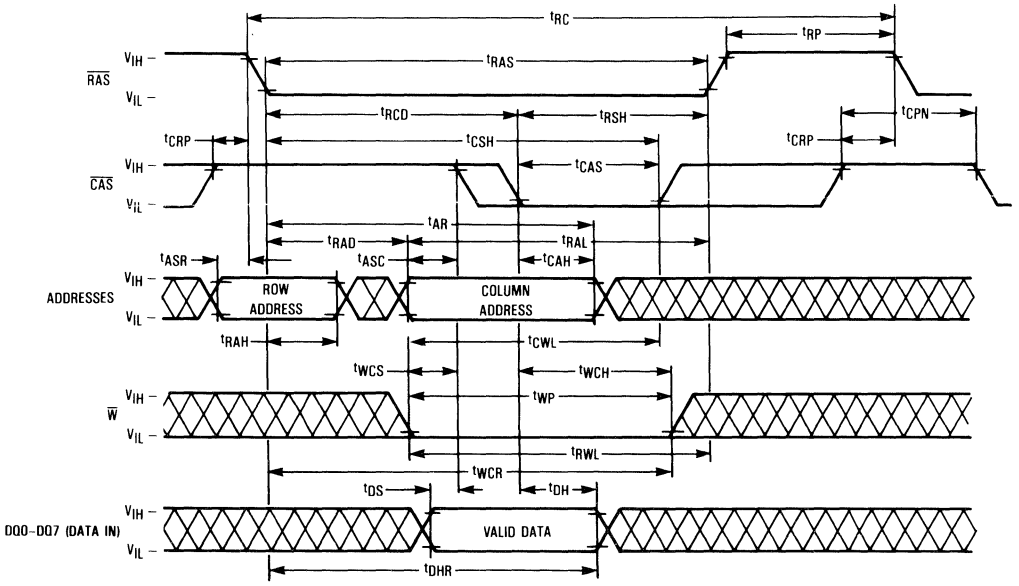
Parameter	Symbol		MCM84256-70		MCM84256-80		MC84256-10		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	–	0	–	0	–	ns	
Read Command Hold Time Referenced to $\overline{CAS}$	t_{CEHWX}	t_{RCH}	0	–	0	–	0	–	ns	13
Read Command Hold Time Referenced to $\overline{RAS}$	t_{REHWX}	t_{RRH}	0	–	0	–	0	–	ns	13
Write Command Hold Time Referenced to $\overline{CAS}$	t_{CELWH}	t_{WCH}	15	–	15	–	20	–	ns	
Write Command Hold Time Referenced to $\overline{RAS}$	t_{RELWH}	t_{WCR}	55	–	60	–	75	–	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	15	–	15	–	20	–	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{WLREH}	t_{RWL}	20	–	20	–	25	–	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{WLCEH}	t_{CWL}	20	–	20	–	25	–	ns	
Data in Setup Time	t_{DVCEL}	t_{DS}	0	–	0	–	0	–	ns	14, 15
Data in Hold Time	t_{CELDX}	t_{DH}	15	–	15	–	20	–	ns	14, 15
Data in Hold Time Referenced to $\overline{RAS}$	t_{RELDX}	t_{DHR}	55	–	60	–	75	–	ns	
Refresh Period MCM84256 MCM8L4256	t_{RVRV}	t_{RFSH}	– –	8 64	– –	8 64	– –	8 64	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	–	0	–	0	–	ns	15, 16
$\overline{CAS}$ Setup Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEL}	t_{CSR}	10	–	10	–	10	–	ns	
$\overline{CAS}$ Hold Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEH}	t_{CHR}	30	–	30	–	30	–	ns	
$\overline{CAS}$ Precharge to $\overline{CAS}$ Active Time	t_{REHCEL}	t_{RPC}	0	–	0	–	0	–	ns	
$\overline{CAS}$ Precharge Time for $\overline{CAS}$ Before $\overline{RAS}$ Counter Test	t_{CEHCEL}	t_{CPT}	40	–	40	–	50	–	ns	
$\overline{CAS}$ Precharge Time	t_{CEHCEL}	t_{CPN}	10	–	10	–	15	–	ns	

NOTES:
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles.
15. Early write only ($t_{WCS} \geq t_{WCS}$ (min)).
16. t_{WCS} is not a restrictive operating parameter. It is included in the data sheet as an electrical characteristic only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle. If this condition is not satisfied, the condition of the data out (at access time) is indeterminate.

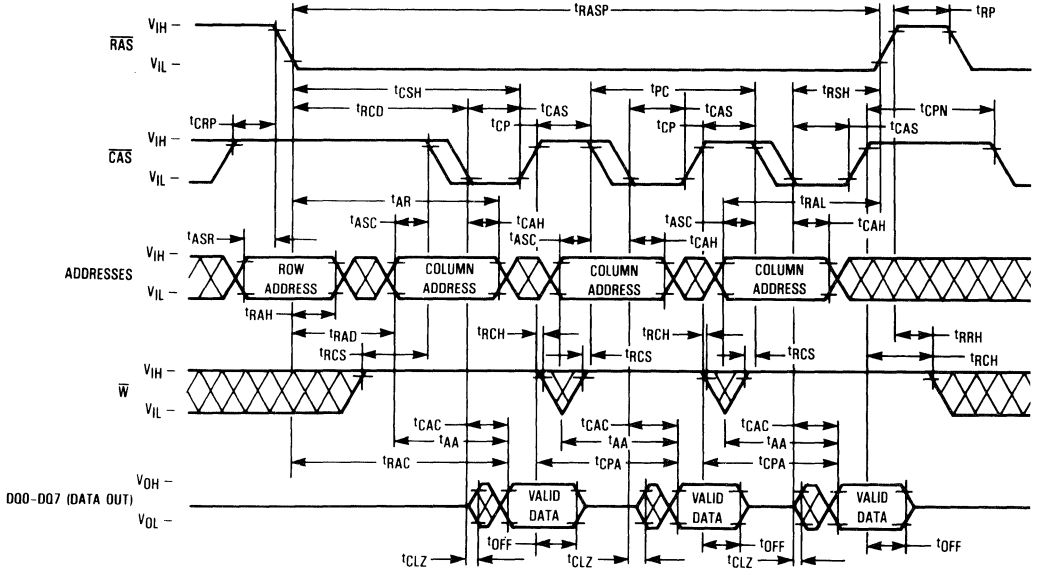
READ CYCLE



EARLY WRITE CYCLE



FAST PAGE MODE READ CYCLE



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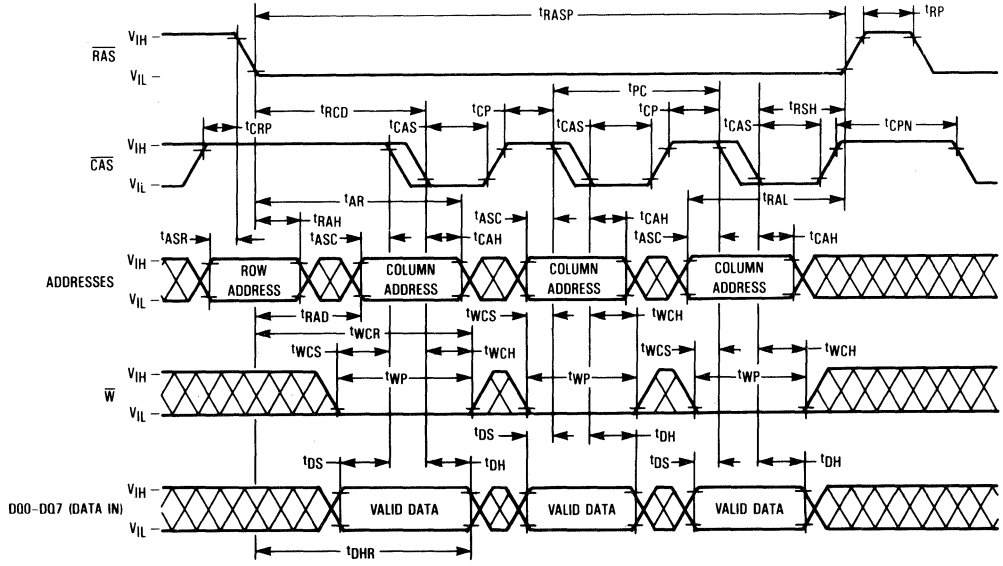
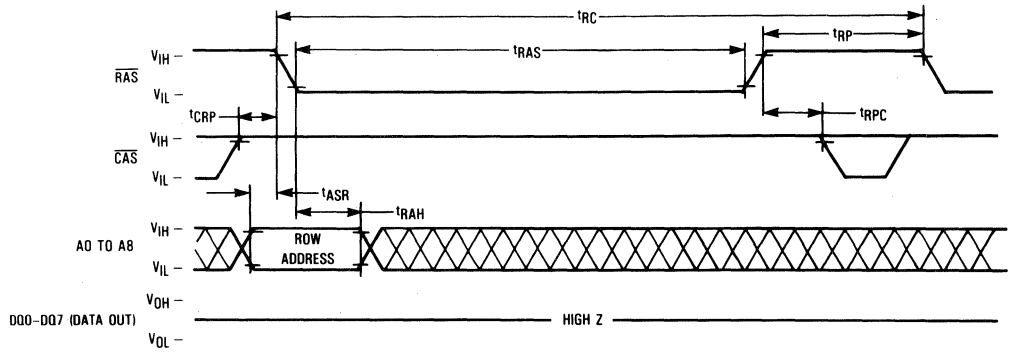
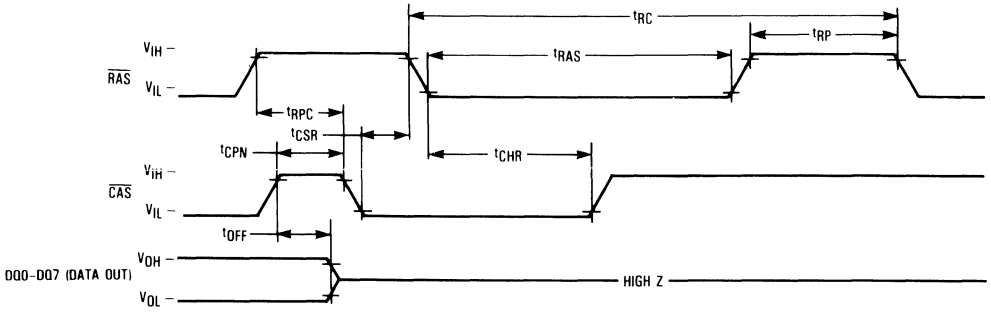
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



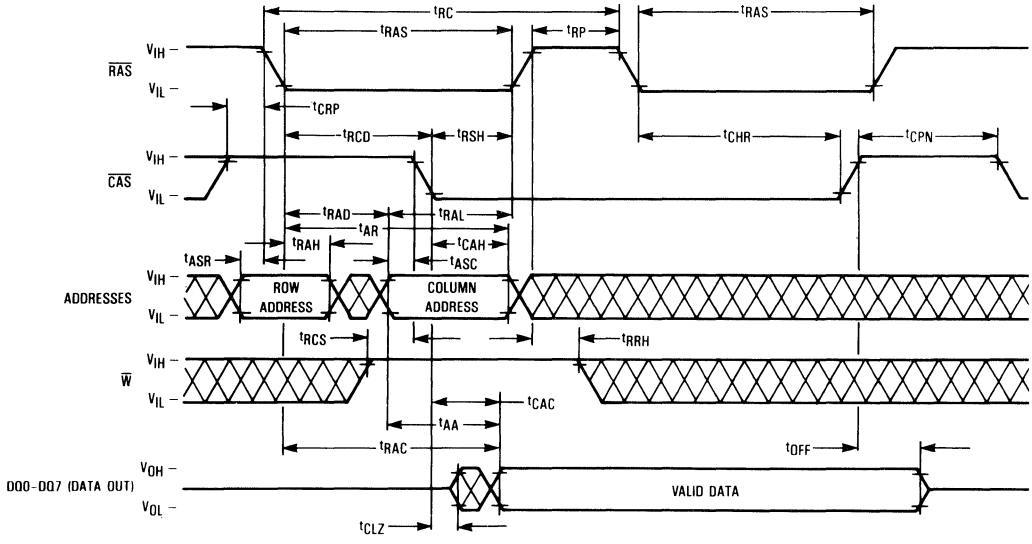
RAS ONLY REFRESH CYCLE
(W and A8 are Don't Care)



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE
($\overline{W}$ and A0 to A8 are Don't Care)



HIDDEN REFRESH CYCLE (READ)



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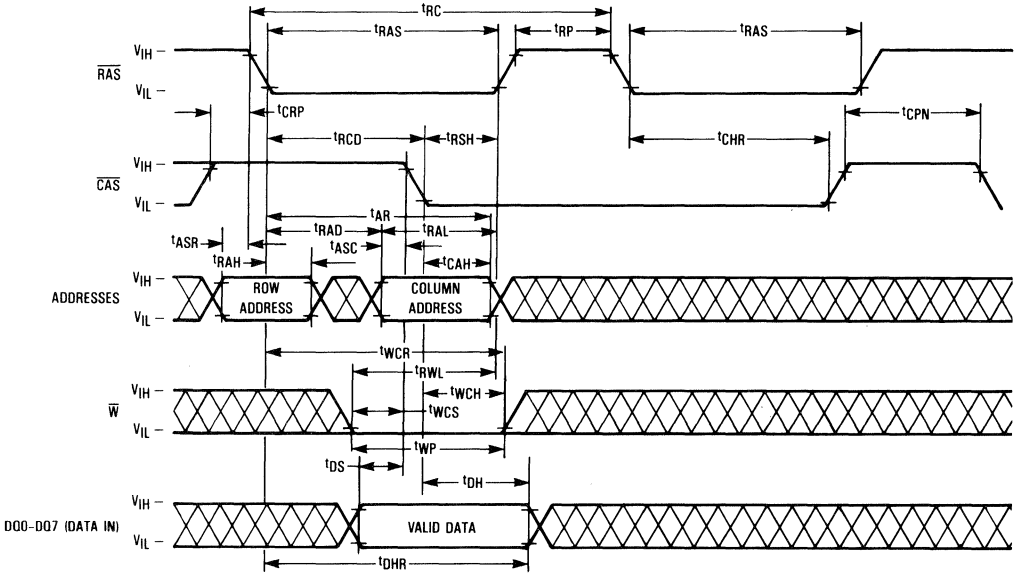
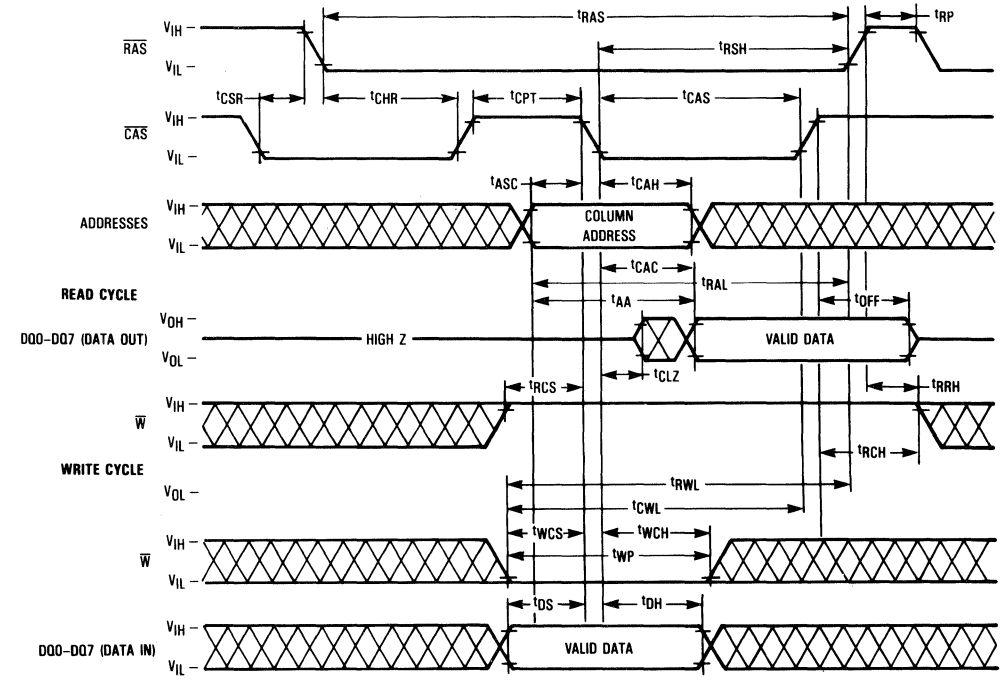
HIDDEN REFRESH CYCLE (WRITE)



CAS BEFORE RAS REFRESH COUNTER TEST CYCLE



DEVICE INITIALIZATION

On power-up an initial pause of 200 microseconds is required for the internal substrate generator pump to establish the correct bias voltage. This is to be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize the various dynamic nodes internal to the device. During an extended inactive state of the device (greater than 4 milliseconds with device powered up), the wake up sequence (8 active cycles) will be necessary to assure proper device operation.

ADDRESSING THE RAM

The nine address bus pins on the device are time multiplexed with two separate 9-bit address fields that are strobed at the beginning of the memory cycle by two clocks (active negative) called the row address strobe ($\overline{RAS}$) and the column address strobe ($\overline{CAS}$). A total of eighteen address bits will decode one of the 262,144 byte locations in the device. The column address strobe follows the row address strobe by a specified minimum and maximum time called "t_{RCD}," which is the row to column strobe delay. This time interval is also referred to as the multiplex window which gives flexibility to a system designer to set up the external addresses into the RAM. These conditions have to be met for normal read or write cycles. This initial portion of the cycle accomplishes the normal addressing of the device. There are, however, other variations in addressing the module: the refresh modes ($\overline{RAS}$ only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, hidden refresh), and another mode called page mode which allows the user to column access the 512 bits within a selected row. The refresh mode and page mode operations are described in more detail in later sections.

READ CYCLE

A read cycle is referred to as a normal read cycle to differentiate it from a page mode read cycle, which is covered in a later section.

The memory read cycle begins with the row addresses valid and the $\overline{RAS}$ clock transitioning from V_{IH} to the V_{IL} level. The $\overline{CAS}$ clock must also make a transition from V_{IH} to the V_{IL} level at the specified t_{RCD} timing limits when the column addresses are latched. Both the $\overline{RAS}$ and $\overline{CAS}$ clocks trigger a sequence of events which are controlled by several delayed internal clocks. Also, these clocks are linked in such a manner that the access time of the device is independent of the address multiplex window. The only stipulation is that the $\overline{CAS}$ clock must be active before or at the t_{RCD} maximum specification for an access (data valid) from the $\overline{RAS}$ clock edge to be guaranteed (t_{RAC}). If the t_{RCD} maximum condition is not met, the access (t_{CAC}) from the $\overline{CAS}$ clock active transition will determine read access time. The external $\overline{CAS}$ signal is ignored until an internal $\overline{RAS}$ signal is available. This gating feature on the $\overline{CAS}$ clock will allow the external $\overline{CAS}$ signal to become active as soon as the row address hold time (t_{RAH}) specification has been met and defines the t_{RCD} minimum specification. The time difference between t_{RCD} minimum and t_{RCD} maximum can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{CAS}$ clock.

Once the clocks have become active, they must stay active for the minimum (t_{RAS}) period for the $\overline{RAS}$ clock and the minimum (t_{CAS}) period for the $\overline{CAS}$ clock. The $\overline{RAS}$ clock must stay inactive for the minimum (t_{RP}) time. The former is for the completion of the cycle in progress, and the latter is for the device internal circuitry to be precharged for the next active cycle.

Data out is not latched and is valid as long as the $\overline{CAS}$ clock is active; the output will switch to the three-state mode when the $\overline{CAS}$ clock goes inactive. To perform a read cycle, the write ($\overline{W}$) input must be held at the V_{IH} level from the time the $\overline{CAS}$ clock makes its active transition (t_{RCS}) to the time when it transitions into the inactive (t_{RCH}) mode.

WRITE CYCLE

A write cycle is similar to a read cycle except that the Write ($\overline{W}$) clock must go active (V_{IL} level) at or before the $\overline{CAS}$ clock goes active at a minimum t_{WCS} time. If the above condition is met, then the cycle in progress is referred to as an early write cycle. In an early write cycle, the write clock and the data in are referenced to the active transition of the $\overline{CAS}$ clock edge. There are two important parameters with respect to the write cycle: the column strobe to write lead time (t_{CWL}) and the row strobe to write lead time (t_{RWL}). These define the minimum time that $\overline{RAS}$ and $\overline{CAS}$ clocks need to be active after the write operation has started ($\overline{W}$ clock at V_{IL} level).

PAGE-MODE CYCLES

Page mode operation allows fast successive data operations at all 512 column locations on a selected row. Page access (t_{CAC}) is typically half the regular $\overline{RAS}$ clock access (t_{RAC}) on the Motorola 1M dynamic RAM. Page mode operation consists of holding the $\overline{RAS}$ clock active while cycling the $\overline{CAS}$ clock to access the column locations determined by the 9-bit column address field.

The page cycle is always initiated with a row address being provided and latched by the $\overline{RAS}$ clock, followed by the column address and $\overline{CAS}$ clock. From the timing illustrated, the initial cycle is a normal read or write cycle, that has been previously described, followed by the shorter $\overline{CAS}$ cycles (t_{PC}). The $\overline{CAS}$ cycle time (t_{PC}) consists of the $\overline{CAS}$ clock active time (t_{CAS}), and $\overline{CAS}$ clock precharge time (t_{CP}) and two transitions. In practice, any combination of read and write cycles can be performed to suit a particular application.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Therefore, to retain the correct information, the module needs to be refreshed at least once every 8 milliseconds. This is accomplished by sequentially cycling through the 512 row address locations every 8 milliseconds (i.e., at least one row every 15.6 microseconds). A normal read or write operation to the module will also refresh all the bytes associated with the particular row(s) decoded.

$\overline{RAS}$-Only Refresh

In this refresh method, the system must perform a $\overline{RAS}$-only cycle on 512 row addresses every 8 milliseconds. The row addresses are latched in with the $\overline{RAS}$ clock, and the associated internal row locations are refreshed. As the heading implies, the $\overline{CAS}$ clock is not required and must be inactive or at a V_{IH} level.

3

$\overline{CAS}$ Before $\overline{RAS}$ Refresh

This refresh cycle is initiated when $\overline{RAS}$ falls, after $\overline{CAS}$ has been low (by t_{CSR}). This activates the internal refresh counter which generates the row address to be refreshed. Externally applied addresses are ignored during the automatic refresh cycle. If the output buffer was off before the automatic refresh cycle, the output will stay in the high impedance state. If the output was enabled by $\overline{CAS}$ in the previous cycle, the data out will be maintained during the automatic refresh cycle as long as $\overline{CAS}$ is held active (hidden refresh).

Hidden Refresh

The hidden refresh method allows refresh cycles to be performed while maintaining valid data at the output pin. Hidden refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. (See Figure 1.)

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST

The internal refresh counter of this device can be tested with a **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test.** This refresh counter test is performed with read and write operations. During this test, the internal refresh counter generates the row address, while the external address input supplies the column address. The entire array is refreshed after 512 test cycles, as indicated by the check data written in each row. See **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test cycle** timing diagram.

The test can be performed only after a minimum of **8 $\overline{CAS}$ before $\overline{RAS}$** initialization cycles. The test procedure is as follows:

1. Write "0"s into all memory cells (normal write mode).
2. Select a column address, and read "0" out of the cell by performing **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test, read cycle.** Repeat this operation 512 times.
3. Select a column address, and write "1" into the cell by performing **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test, write cycle.** Repeat this operation 512 times.
4. Read "1"s (normal read mode), which were written at step 3.
5. Repeat steps 1 to 4 using complement data.

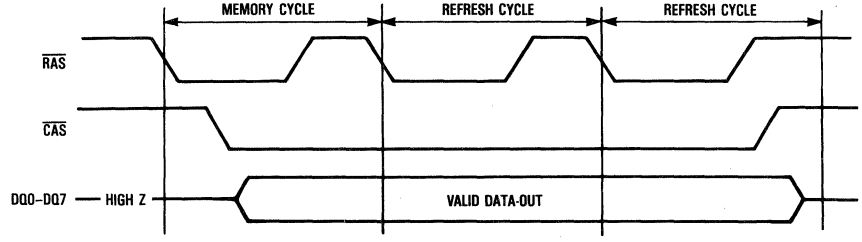


Figure 1. Hidden Refresh Cycle

ORDERING INFORMATION
(Order by Full Part Number)

MCM 84256 or 8L4256 X XX

Motorola Memory Prefix

Part Number

Speed (70 = 70 ns, 80 = 80 ns, 10 = 100 ns)

Package (S = SIMM)

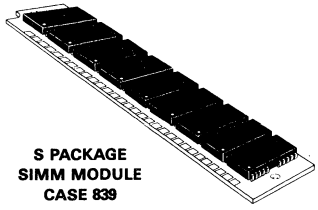
Full Part Numbers — MCM84256S70, MCM84256S80, MCM84256S10, MCM8L4256S70, MCM8L4256S80, MCM8L4256S10

MCM91000
MCM9L1000

3

Advance Information

1M x 9 Bit Dynamic Random Access Memory Module

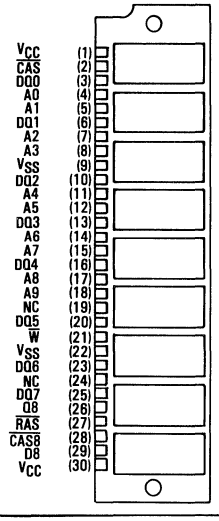


S PACKAGE
SIMM MODULE
CASE 839

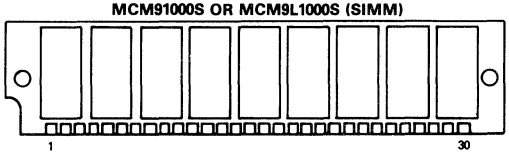
The MCM91000L and MCM91000S are 9M, dynamic random access memory (DRAM) modules organized as 1,048,576 x 9 bits. The modules are 30-lead single-in-line memory modules (SIMM) or 30-pin single-in-line packages (SIP) consisting of nine MCM511000A DRAMs housed in a 20/26 J-lead small outline package (SOJ) and mounted on a substrate along with a 0.22 μF (min) decoupling capacitor mounted under each DRAM. The MCM511000A is a 1.0μ CMOS high speed, dynamic random access memory organized as 1,048,576 one-bit words and fabricated with CMOS silicon-gate process technology.

- Three-State Data Output
- Early-Write Common I/O Capability
- Fast Page Mode Capability
- TTL-Compatible Inputs and Outputs
- $\overline{RAS}$ Only Refresh
- $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- Hidden Refresh
- 512 Cycle Refresh:
  - MCM91000 = 8 ms (Max)
  - MCM9L1000 = 64 ms (Max)
- Consists of Nine 1M DRAMs and Nine 0.22 μF (Min) Decoupling Capacitors
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}):
  - MCM91000-70 = 70 ns (Max)
  - MCM91000-80 = 80 ns (Max)
  - MCM91000-10 = 100 ns (Max)
- Low Active Power Dissipation:
  - MCM91000-70 = 4.0 W (Max)
  - MCM91000-80 = 3.5 W (Max)
  - MCM91000-10 = 3.0 W (Max)
- Low Standby Power Dissipation:
  - TTL Levels = 99 mW (Max)
  - CMOS Levels (MCM91000) = 50 mW (Max)
    (MCM9L1000) = 10 mW (Max)
- $\overline{CAS}$ Control for Eight Common I/O Lines
- $\overline{CAS}$ Control for Separate I/O Pair
- Available in Edge Connector (MCM91000S) or Pin Connector (MCM91000L)
- Available in Gold Pad Edge Connector (MCM91000SG)

30-PIN
SINGLE IN-LINE PACKAGE
(TOP VIEW, MCM91000S/9L1000S)



MCM91000S OR MCM9L1000S (SIMM)

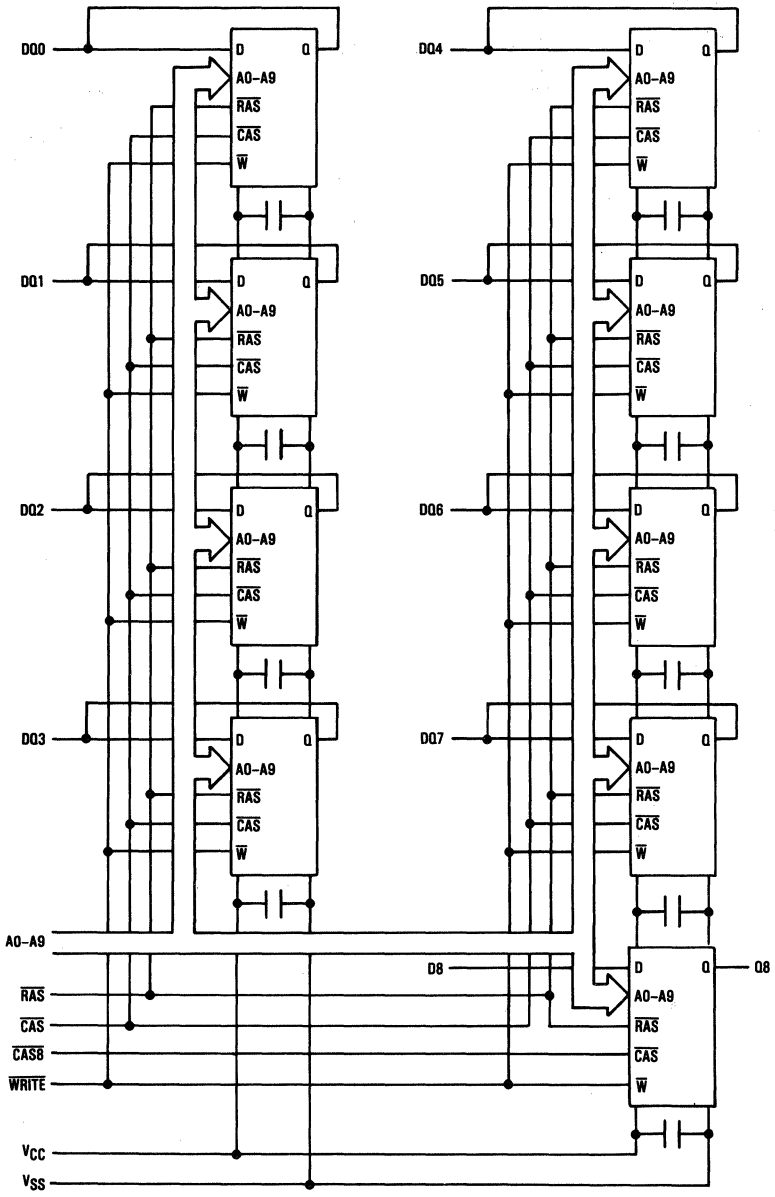


PIN NAMES	
A0-A9	Address Inputs
DQ0-DQ7	Data Input/Output
D8	Data Input
Q8	Data Output
$\overline{CAS}$	Column Address Strobe
$\overline{RAS}$	Row Address Strobe
$\overline{W}$	Read/Write Input
$\overline{CAS8}$	Column Address Strobe
V_{CC}	Power (+5 V)
V_{SS}	Ground
NC	No Connection

This document contains information on a new product. Specifications and information herein are subject to change without notice.

3

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−1 to +7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−1 to +7	V
Data Out Current per DQ Pin	I_{out}	50	mA
Power Dissipation	P_D	5.4	W
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V	1
	V_{SS}	0	0	0		
Logic High Voltage, All Inputs	V_{IH}	2.4	—	6.5	V	1
Logic Low Voltage, All Inputs	V_{IL}	−1.0	—	0.8	V	1

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current	I_{CC1}			mA	2
MCM91000-70, t_{RC} = 130 ns		—	720		
MCM91000-80, t_{RC} = 150 ns		—	630		
MCM91000-10, t_{RC} = 180 ns		—	540		
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	—	18	mA	
V_{CC} Power Supply Current During $\overline{RAS}$ only Refresh Cycles	I_{CC3}			mA	2
MCM91000-70, t_{RC} = 130 ns		—	720		
MCM91000-80, t_{RC} = 150 ns		—	630		
MCM91000-10, t_{RC} = 180 ns		—	540		
V_{CC} Power Supply Current During Fast Page Mode Cycle	I_{CC4}			mA	2
MCM91000-70, t_{PC} = 40 ns		—	540		
MCM91000-80, t_{PC} = 45 ns		—	450		
MCM91000-10, t_{PC} = 55 ns		—	360		
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} − 0.2 V) MCM91000	I_{CC5}	—	9	mA	
MCM9L1000		—	1.8		
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle	I_{CC6}			mA	2
MCM91000-70, t_{RC} = 130 ns		—	720		
MCM91000-80, t_{RC} = 150 ns		—	630		
MCM91000-10, t_{RC} = 180 ns		—	540		
Input Leakage Current ($V_{SS} \le V_{in} \le V_{CC}$)	$I_{lkg(I)}$	−90	90	μA	
Output Leakage Current ($\overline{CAS}$ at Logic 1, $V_{SS} \le V_{out} \le V_{CC}$)	$I_{lkg(O)}$	−20	20	μA	
Output High Voltage (I_{OH} = −5 mA)	V_{OH}	2.4	—	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	—	0.4	V	

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Max	Unit	Notes
Input Capacitance	A0-A9, $\overline{W}$, $\overline{CAS}$, $\overline{RAS}$	C_{in}	60	pF	3
	D8, $\overline{CAS8}$		7	pF	3
Input/Output Capacitance	DQ0-DQ7	$C_{I/O}$	15	pF	3
Output Capacitance ($\overline{CAS}$ = V_{IH} to Disable Output)	Q8	C_{out}	10	pF	3

NOTES:
1. All voltages referenced to V_{SS}.
2. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
3. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\Delta t/\Delta V$.

3

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ AND WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM91000-70		MCM91000-80		MCM91000-10		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	130	–	150	–	180	–	ns	5
Page Mode Cycle Time	t_{CELCEL}	t_{PC}	40	–	45	–	55	–	ns	
Access Time from $\overline{RAS}$	t_{RELQV}	t_{RAC}	–	70	–	80	–	100	ns	6, 7
Access Time from $\overline{CAS}$	t_{CELQV}	t_{CAC}	–	20	–	20	–	25	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	–	35	–	40	–	50	ns	6, 9
Access Time from Precharge $\overline{CAS}$	t_{CEHQV}	t_{CPA}	–	35	–	40	–	50	ns	6
$\overline{CAS}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	0	–	0	–	0	–	ns	6
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	20	0	20	0	20	ns	10
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{REHREL}	t_{RP}	50	–	60	–	70	–	ns	
$\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ Hold Time	t_{CELREH}	t_{RSH}	20	–	25	–	ns			
$\overline{CAS}$ Hold Time	t_{RELCEH}	t_{CSH}	70	–	80	–	100	–	ns	
$\overline{CAS}$ Pulse Width	t_{CELCEH}	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RELCEL}	t_{RCD}	20	50	20	60	25	75	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	35	15	40	20	50	ns	12
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	–	5	–	5	–	ns	
$\overline{CAS}$ Precharge Time (Page Mode Cycle Only)	t_{CEHCEL}	t_{CP}	10	–	10	–	10	–	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	–	0	–	0	–	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	–	10	–	15	–	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	–	0	–	0	–	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	–	15	–	20	–	ns	
Column Address Hold Time Referenced to $\overline{RAS}$	t_{RELAX}	t_{AR}	55	–	60	–	75	–	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{AVREH}	t_{RAL}	35	–	40	–	50	–	ns	

(continued)

NOTES:

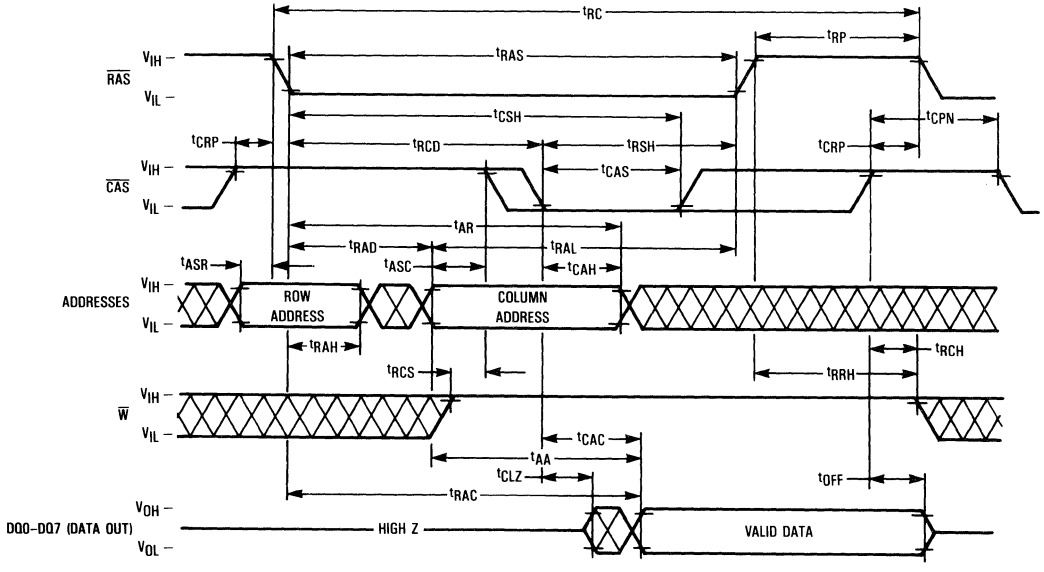
1. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
6. Measured with a current load equivalent to 2 TTL (−200 μA, +4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
8. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
9. Assumes that $t_{RAD} \geq t_{RAD}$ (max).
10. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
12. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.

READ AND WRITE CYCLES (Continued)

Parameter	Symbol		MCM91000-70		MCM91000-80		MC91000-10		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	–	0	–	0	–	ns	
Read Command Hold Time Referenced to $\overline{CAS}$	t_{CEHWX}	t_{RCH}	0	–	0	–	0	–	ns	13
Read Command Hold Time Referenced to $\overline{RAS}$	t_{REHWX}	t_{RRH}	0	–	0	–	0	–	ns	13
Write Command Hold Time Referenced to $\overline{CAS}$	t_{CELWH}	t_{WCH}	15	–	15	–	20	–	ns	
Write Command Hold Time Referenced to $\overline{RAS}$	t_{RELWH}	t_{WCR}	55	–	60	–	75	–	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	15	–	15	–	20	–	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{WLREH}	t_{RWL}	20	–	20	–	25	–	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{WLCEH}	t_{CWL}	20	–	20	–	25	–	ns	
Data in Setup Time	t_{DVCEL}	t_{DS}	0	–	0	–	0	–	ns	14, 15
Data in Hold Time	t_{CELDX}	t_{DH}	15	–	15	–	20	–	ns	14, 15
Data in Hold Time Referenced to $\overline{RAS}$	t_{RELDX}	t_{DHR}	55	–	60	–	75	–	ns	
Refresh Period MCM91000 MCM9L1000	t_{RVRV}	t_{RFSH}	– –	8 64	– –	8 64	– –	8 64	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	–	0	–	0	–	ns	15, 16
$\overline{CAS}$ Setup Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEL}	t_{CSR}	10	–	10	–	10	–	ns	
$\overline{CAS}$ Hold Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEH}	t_{CHR}	30	–	30	–	30	–	ns	
$\overline{CAS}$ Precharge to $\overline{CAS}$ Active Time	t_{REHCEL}	t_{RPC}	0	–	0	–	0	–	ns	
$\overline{CAS}$ Precharge Time for $\overline{CAS}$ Before $\overline{RAS}$ Counter Test	t_{CEHCEL}	t_{CPT}	40	–	40	–	50	–	ns	
$\overline{CAS}$ Precharge Time	t_{CEHCEL}	t_{CPN}	10	–	10	–	15	–	ns	

NOTES:
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles.
15. Early write only ($t_{WCS} \geq t_{WCS}$ (min)).
16. t_{WCS} is not a restrictive operating parameter. It is included in the data sheet as an electrical characteristic only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle. If this condition is not satisfied, the condition of the data out (at access time) is indeterminate.

READ CYCLE



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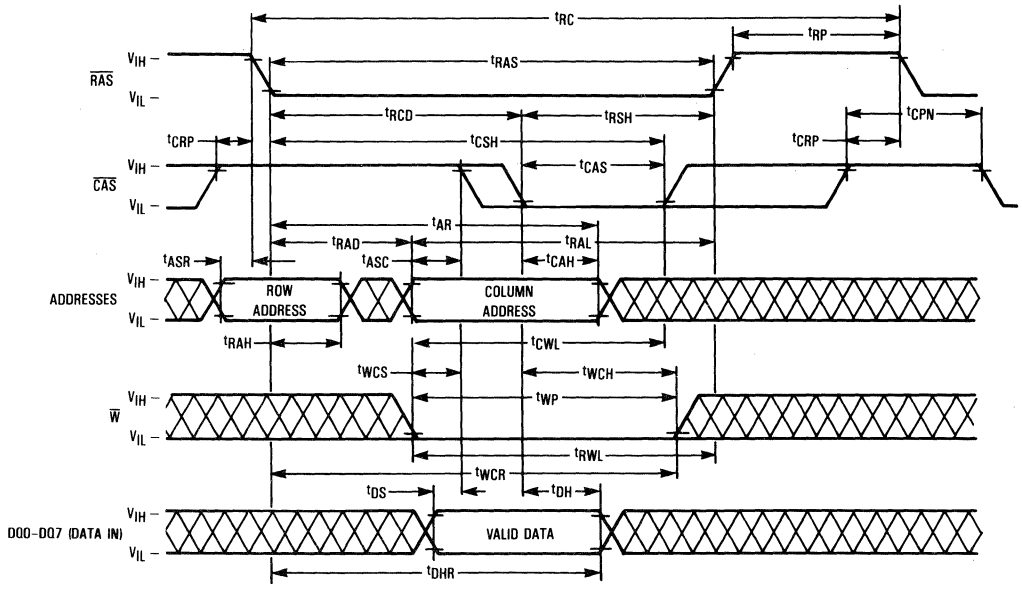
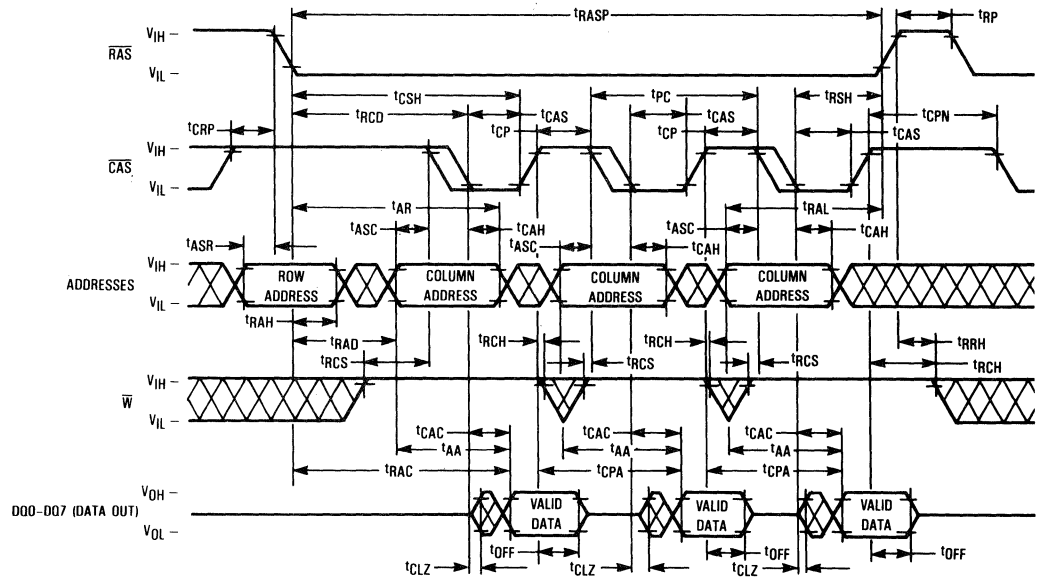
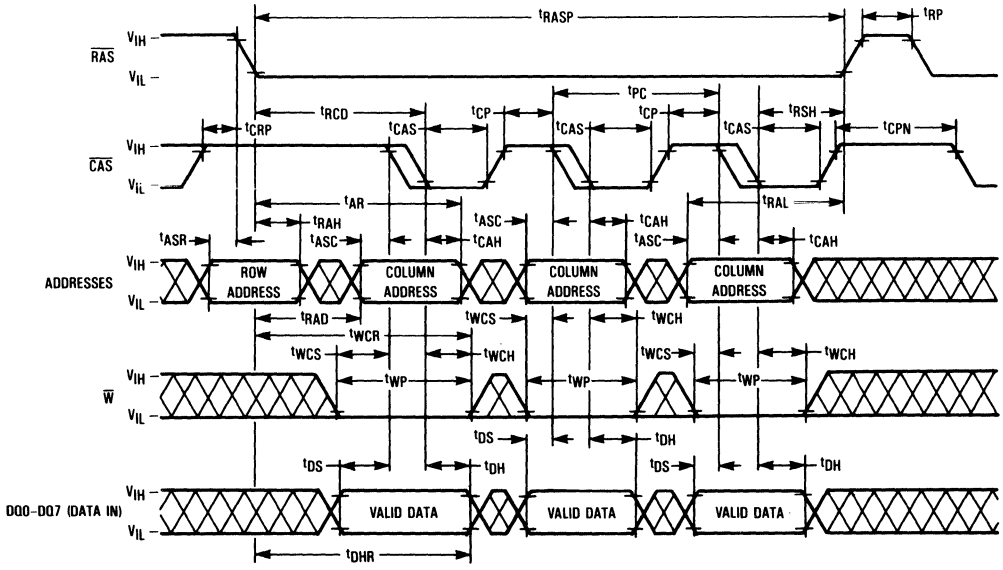
EARLY WRITE CYCLE



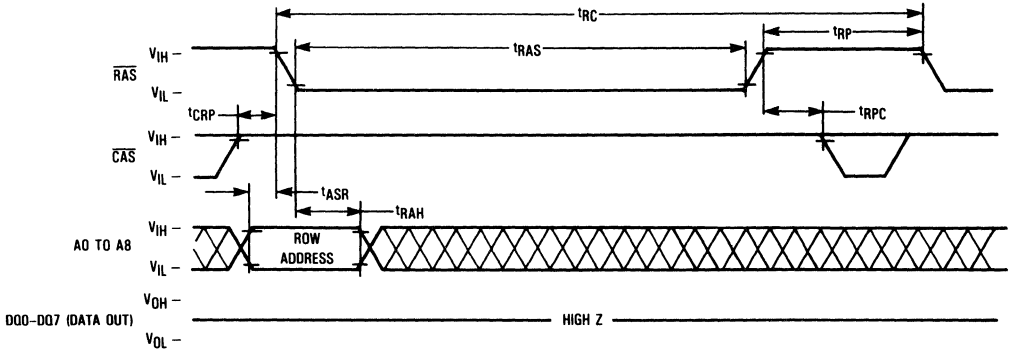
FAST PAGE MODE READ CYCLE



FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



RAS ONLY REFRESH CYCLE
(W and A9 are Don't Care)



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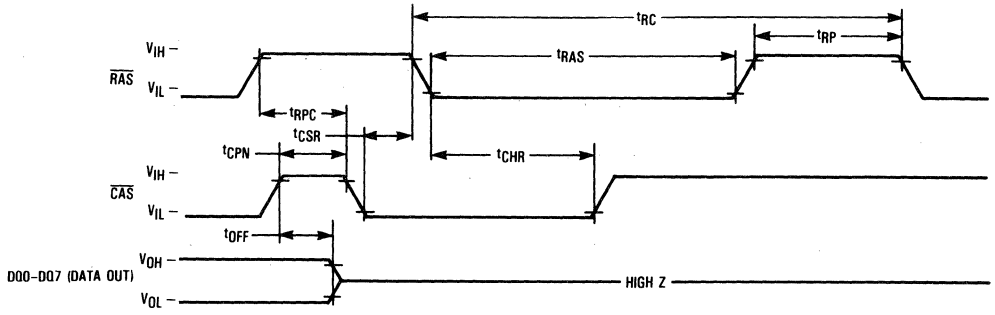
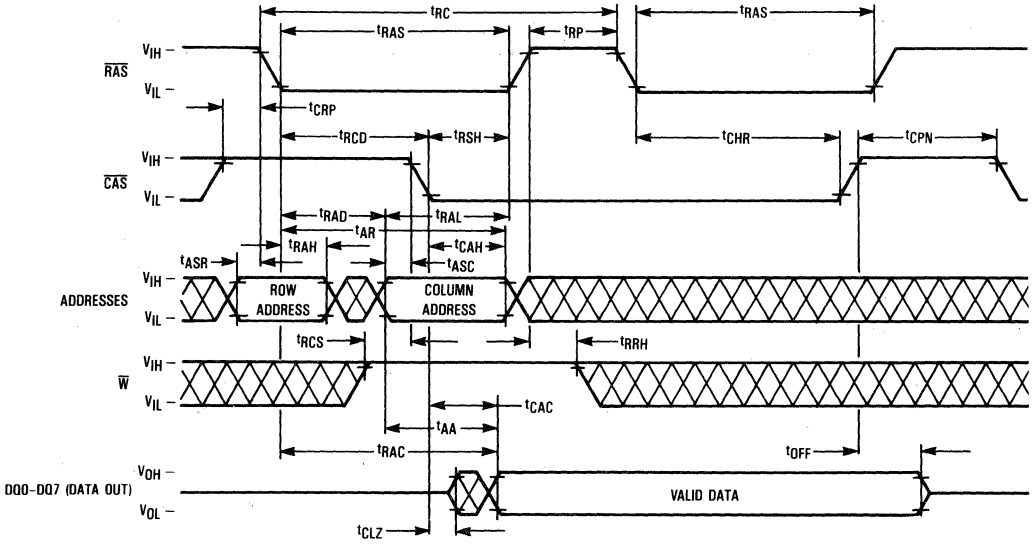
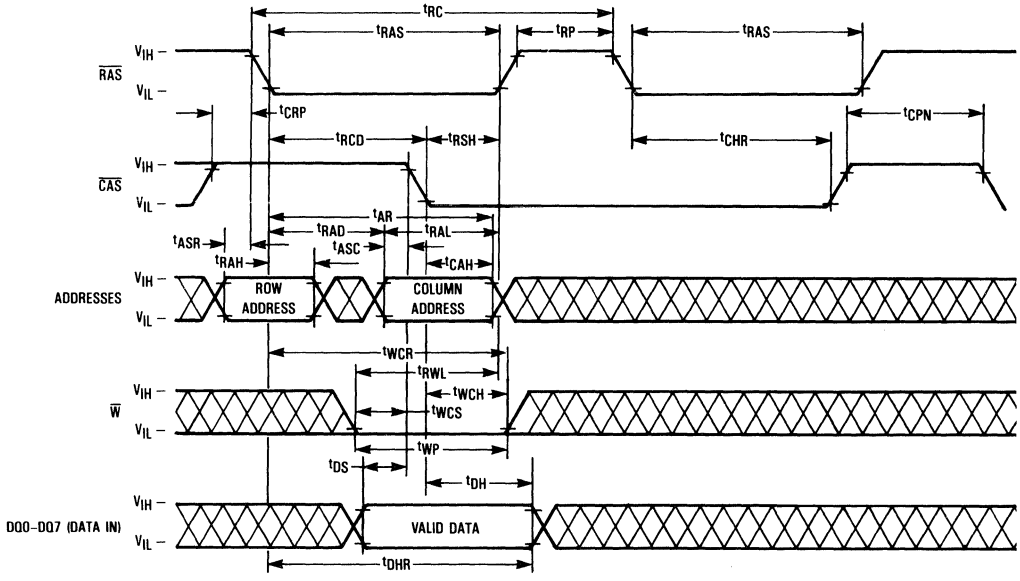
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE
($\overline{W}$ and A0 to A9 are Don't Care)



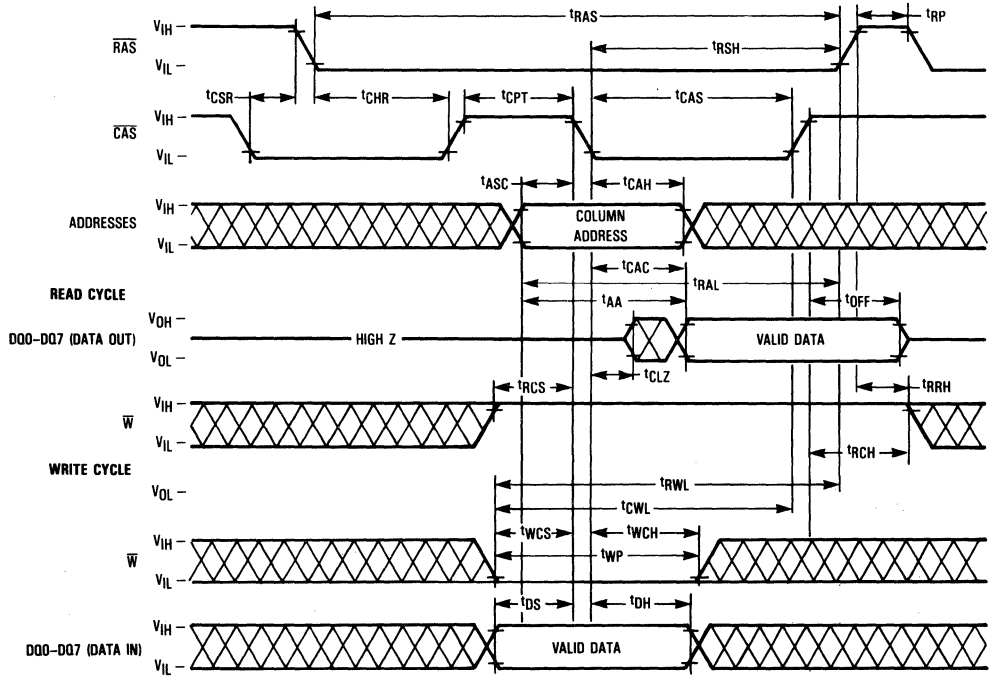
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



CAS BEFORE RAS REFRESH COUNTER TEST CYCLE



3

DEVICE INITIALIZATION

On power-up an initial pause of 200 microseconds is required for the internal substrate generator pump to establish the correct bias voltage. This is to be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize the various dynamic nodes internal to the device. During an extended inactive state of the device (greater than 4 milliseconds with device powered up), the wake up sequence (8 active cycles) will be necessary to assure proper device operation.

ADDRESSING THE RAM

The ten address bus pins on the device are time multiplexed with two separate 10-bit address fields that are strobed at the beginning of the memory cycle by two clocks (active negative) called the row address strobe ($\overline{RAS}$) and the column address strobe ($\overline{CAS}$). A total of twenty address bits will decode one of the 1,048,576 byte locations in the device. The column address strobe follows the row address strobe by a specified minimum and maximum time called "t_{RCD}," which is the row to column strobe delay. This time interval is also referred to as the multiplex window which gives flexibility to a system designer to set up his external addresses into the RAM. These conditions have to be met for normal read or write cycles. This initial portion of the cycle accomplishes the normal addressing of the device. There are, however, two other variations in addressing the 1M RAM module, one is called the $\overline{RAS}$ only refresh cycle (described later) where a 9-bit row address field is presented on the input pins and latched by the $\overline{RAS}$ clock. The most significant bit on Row Address A9 is not required for refresh. The other variation, which is called page mode, allows the user to column access all 1024 bytes within a selected row. (See **PAGE-MODE CYCLES** section.)

READ CYCLE

A read cycle is referred to as a normal read cycle to differentiate it from a page mode read cycle, which is covered in a later section.

The memory read cycle begins with the row addresses valid and the $\overline{RAS}$ clock transitioning from V_{IH} to the V_{IL} level. The $\overline{CAS}$ clock must also make a transition from V_{IH} to the V_{IL} level at the specified t_{RCD} timing limits when the column addresses are latched. Both the $\overline{RAS}$ and $\overline{CAS}$ clocks trigger a sequence of events which are controlled by several delayed internal clocks. Also, these clocks are linked in such a manner that the access time of the device is independent of the address multiplex window. The only stipulation is that the $\overline{CAS}$ clock must be active before or at the t_{RCD} maximum specification for an access (data valid) from the $\overline{RAS}$ clock edge to be guaranteed (t_{RAC}). If the t_{RCD} maximum condition is not met, the access (t_{CAC}) from the $\overline{CAS}$ clock active transition will determine read access time. The external $\overline{CAS}$ signal is ignored until an internal $\overline{RAS}$ signal is available. This gating feature on the $\overline{CAS}$ clock will allow the external $\overline{CAS}$ signal to become active as soon as the row address hold time (t_{RAH}) specification has been met and defines the t_{RCD} minimum specification. The time difference between t_{RCD} minimum and t_{RCD} maximum can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{CAS}$ clock.

Once the clocks have become active, they must stay active for the minimum (t_{RAS}) period for the $\overline{RAS}$ clock and the minimum (t_{CAS}) period for the $\overline{CAS}$ clock. The $\overline{RAS}$ clock must stay inactive for the minimum (t_{RP}) time. The former is for the completion of the cycle in progress, and the latter is for the device internal circuitry to be precharged for the next active cycle.

Data out is not latched and is valid as long as the $\overline{CAS}$ clock is active; the output will switch to the three-state mode when the $\overline{CAS}$ clock goes inactive. To perform a read cycle, the write ($\overline{W}$) input must be held at the V_{IH} level from the time the $\overline{CAS}$ clock makes its active transition (t_{RCS}) to the time when it transitions into the inactive (t_{RCH}) mode.

WRITE CYCLE

A write cycle is similar to a read cycle except that the Write ($\overline{W}$) clock must go active (V_{IL} level) at or before the $\overline{CAS}$ clock goes active at a minimum t_{WCS} time. If the above condition is met, then the cycle in progress is referred to as an early write cycle. In an early write cycle, the write clock and the data in are referenced to the active transition of the $\overline{CAS}$ clock edge. There are two important parameters with respect to the write cycle: the column strobe to write lead time (t_{CWL}) and the row strobe to write lead time (t_{RWL}). These define the minimum time that $\overline{RAS}$ and $\overline{CAS}$ clocks need to be active after the write operation has started ($\overline{W}$ clock at V_{IL} level).

PAGE-MODE CYCLES

Page mode operation allows fast successive data operations at all 1024 column locations on a selected row. Page access (t_{CAC}) is typically half the regular $\overline{RAS}$ clock access (t_{RAC}) on the Motorola 1M dynamic RAM. Page mode operation consists of holding the $\overline{RAS}$ clock active while cycling the $\overline{CAS}$ clock to access the column locations determined by the 10-bit column address field.

The page cycle is always initiated with a row address being provided and latched by the $\overline{RAS}$ clock, followed by the column address and $\overline{CAS}$ clock. From the timing illustrated, the initial cycle is a normal read or write cycle, that has been previously described, followed by the shorter $\overline{CAS}$ cycles (t_{PC}). The $\overline{CAS}$ cycle time (t_{PC}) consists of the $\overline{CAS}$ clock active time (t_{CAS}), and $\overline{CAS}$ clock precharge time (t_{CP}) and two transitions. In practice, any combination of read and write cycles can be performed to suit a particular application.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Therefore, to retain the correct information, the module needs to be refreshed at least once every 8 milliseconds. This is accomplished by sequentially cycling through the 512 row address locations every 8 milliseconds (i.e., at least one row every 15.6 microseconds). A normal read or write operation to the module will also refresh all the bytes (2048) associated with the particular row(s) decoded.

$\overline{RAS}$-Only Refresh

In this refresh method, the system must perform a $\overline{RAS}$-only cycle on 512 row addresses every 8 milliseconds. The row addresses are latched in with the $\overline{RAS}$ clock, and the associated internal row locations are refreshed. As the heading implies, the $\overline{CAS}$ clock is not required and must be inactive or at a V_{IH} level.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh

This refresh cycle is initiated when $\overline{RAS}$ falls, after $\overline{CAS}$ has been low (by t_{CSR}). This activates the internal refresh counter which generates the row address to be refreshed. Externally applied addresses are ignored during the automatic refresh cycle. If the output buffer was off before the automatic refresh cycle, the output will stay in the high impedance state. If the output was enabled by $\overline{CAS}$ in the previous cycle, the data out will be maintained during the automatic refresh cycle as long as $\overline{CAS}$ is held active (hidden refresh).

Hidden Refresh

The hidden refresh method allows refresh cycles to be performed while maintaining valid data at the output pin. Hidden refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. (See Figure 1.)

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST

The internal refresh counter of this device can be tested with a **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test**. This refresh counter test is performed with read and write operations. During this test, the internal refresh counter generates the row address, while the external address input supplies the column address. The entire array is refreshed after 512 test cycles, as indicated by the check data written in each row. See **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test cycle** timing diagram.

The test can be performed only after a minimum of **8 $\overline{CAS}$ before $\overline{RAS}$** initialization cycles. The test procedure is as follows:

1. Write "0"s into all memory cells (normal write mode).
2. Select a column address, and read "0" out of the cell by performing **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test, read cycle**. Repeat this operation 512 times.
3. Select a column address, and write "1" into the cell by performing **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test, write cycle**. Repeat this operation 512 times.
4. Read "1"s (normal read mode), which were written at step 3.
5. Repeat steps 1 to 4 using complement data.

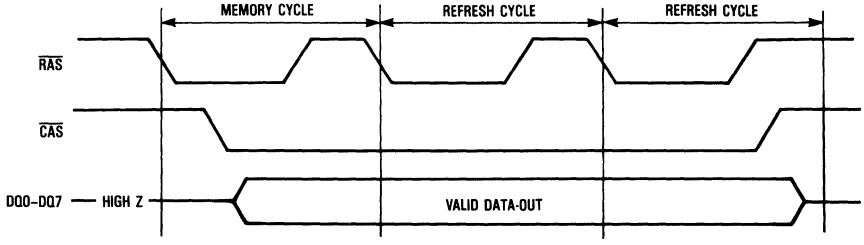


Figure 1. Hidden Refresh Cycle

ORDERING INFORMATION
(Order by Full Part Number)

MCM 91000 or 9L1000 X XX

Motorola Memory Prefix

Part Number

Speed (70 = 70 ns, 80 = 80 ns, 10 = 100 ns)

Package (L = SIP, S = SIMM, SG = Gold Pad SIMM)

Full Part Numbers—	MCM91000L70	MCM91000S70	MCM91000SG70
	MCM91000L80	MCM91000S80	MCM91000SG80
	MCM91000L10	MCM91000S10	MCM91000SG10
	MCM9L1000L70	MCM9L1000S70	MCM9L1000SG70
	MCM9L1000L80	MCM9L1000S80	MCM9L1000SG80
	MCM9L1000L10	MCM9L1000S10	MCM9L1000SG10

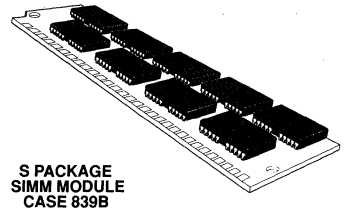
NOTE: Contact your Motorola representative for further information on the SIP and Gold Pad SIMM packages.

MCM94000
MCM9L4000

3

Advance Information

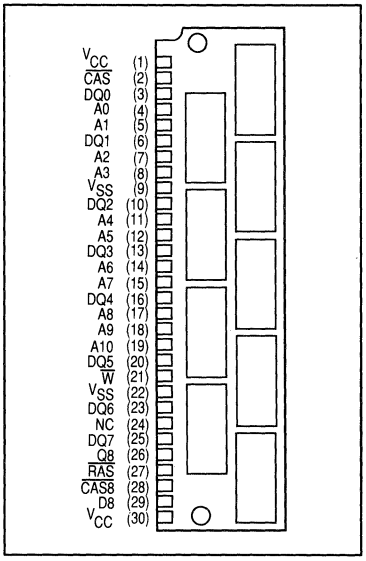
4M × 9 Bit Dynamic Random Access Memory Module



S PACKAGE
SIMM MODULE
CASE 839B

The MCM94000S is a 36M, dynamic random access memory (DRAM) module organized as 4,194,304 x 9 bits. The module is a 30-lead single-in-line memory module (SIMM) consisting of nine MCM514100 DRAMs housed in 20/26 J-lead small outline packages (SOJ) mounted on a substrate along with a 0.22 microfarad (min) decoupling capacitor mounted under each DRAM. The MCM514100 is a CMOS high speed, dynamic random access memory organized as 4,194,304 one-bit words and fabricated with CMOS silicon-gate process technology.

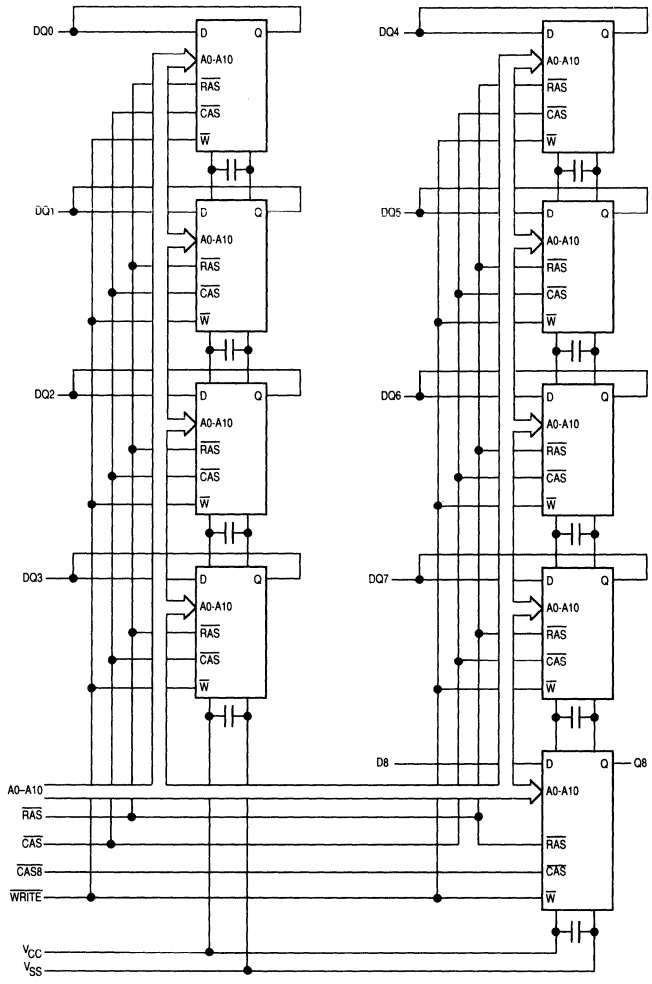
- Three-State Data Output
- Early-Write Common I/O Capability
- Fast Page Mode Capability
- TTL-Compatible Inputs and Outputs
- $\overline{RAS}$ Only Refresh
- $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- Hidden Refresh
- 1024 Cycle Refresh:
  MCM94000 = 16 ms
  MCM9L4000 = 128 ms
- Consists of Nine 4M x 1 DRAMs and Nine 0.22 µF (Min) Decoupling Capacitors
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}):
  MCM94000S-80 = 80 ns (Max)
  MCM94000S-10 = 100 ns (Max)
- Low Active Power Dissipation:
  MCM94000S-80 and MCM9L4000S-80 = 4.95 W (Max)
  MCM94000S-10 and MCM9L4000S-10 = 4.21 W (Max)
- Low Standby Power Dissipation:
  TTL Levels = 99 mW (Max)
  CMOS Levels (MCM94000) = 50 mW (Max)
  (MCM9L4000) = 20 mW (Max)
- $\overline{CAS}$ Control for Eight Common I/O Lines
- $\overline{CAS}$ Control for Separate I/O Pair



PIN NAMES	
A0–A10	Address Inputs
DQ0–DQ7	Data Input/Output
D8	Data Input
Q8	Data Output
$\overline{CAS}$	Column Address Strobe
$\overline{RAS}$	Row Address Strobe
$\overline{W}$	Read/Write Input
CAS8	Column Address Strobe
V_{CC}	Power (+5 V)
V_{SS}	Ground
NC	No Connection

This document contains information on a new product. Specifications and information herein are subject to change without notice.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−1 to + 7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−1 to + 7	V
Data Out Current per DQ Pin	I_{out}	50	mA
Power Dissipation	P_D	5.4	W
Operating Temperature Range	T_A	0 to + 70	°C
Storage Temperature Range	T_{stg}	− 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

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DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V	1
	V_{SS}	0	0	0		
Logic High Voltage, All Inputs	V_{IH}	2.4	—	6.5	V	1
Logic Low Voltage, All Inputs	V_{IL}	–1.0	—	0.8	V	1

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current MCM94000-80, t_{RC} = 150 ns MCM94000-10, t_{RC} = 180 ns	I_{CC1}	 — —	 900 765	mA	2
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	—	18	mA	
V_{CC} Power Supply Current During $\overline{RAS}$ only Refresh Cycles MCM94000-80, t_{RC} = 150 ns MCM94000-10, t_{RC} = 180 ns	I_{CC3}	 — —	 900 765	mA	2
V_{CC} Power Supply Current During Fast Page Mode Cycle MCM94000-80, t_{PC} = 45 ns MCM94000-10, t_{PC} = 55 ns	I_{CC4}	 — —	 540 450	mA	2
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V) MCM94000 MCM9L4000	I_{CC5}	— —	9 3.6	mA	
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle MCM94000-80, t_{RC} = 150 ns MCM94000-10, t_{RC} = 180 ns	I_{CC6}	 — —	 900 765	mA	2
Input Leakage Current ($V_{SS} \le V_{in} \le V_{CC}$)	$I_{lkg(I)}$	–90	90	µA	
Output Leakage Current ($\overline{CAS}$ at Logic 1, $V_{SS} \le V_{in} \le V_{CC}$)	$I_{lkg(O)}$	–20	20	µA	
Output High Voltage (I_{OH} = –5 mA)	V_{OH}	2.4	—	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	—	0.4	V	

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Max	Unit	Notes
Input Capacitance	A0–A10, $\overline{W}$, $\overline{CAS}$, $\overline{RAS}$	C_{in}	60	pF	3
	D8, $\overline{CAS8}$		7	pF	3
Input/Output Capacitance	DQ0–DQ7	$C_{I/O}$	15	pF	3
Output Capacitance ($\overline{CAS}$ = V_{IH} to Disable Output)	Q8	C_{out}	10	pF	3

NOTES:

1. All voltages referenced to V_{SS}.
2. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
3. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\Delta t/\Delta V$.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted

READ AND WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM94000-80		MCM94000-10		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	150	—	180	—	ns	5
Page Mode Cycle Time	t_{CELCEL}	t_{PC}	50	—	60	—	ns	
Access Time from $\overline{RAS}$	t_{RELQV}	t_{RAC}	—	80	—	100	ns	6, 7
Access Time from $\overline{CAS}$	t_{CELQV}	t_{CAC}	—	20	—	25	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	—	40	—	50	ns	6, 9
Access Time from Precharge $\overline{CAS}$	t_{CEHQV}	t_{CPA}	—	45	—	55	ns	6
$\overline{CAS}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	0	—	0	—	ns	6
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	20	0	20	ns	10
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{REHREL}	t_{RP}	60	—	70	—	ns	
$\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RAS}	80	10,000	100	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	80	200,000	100	200,000	ns	
$\overline{RAS}$ Hold Time	t_{CELREH}	t_{RSH}	20	—	25	—	ns	
$\overline{CAS}$ Hold Time	t_{RELCEH}	t_{CSH}	80	—	100	—	ns	
$\overline{CAS}$ Pulse Width	t_{CELCEH}	t_{CAS}	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RELCEL}	t_{RCD}	20	60	25	75	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	40	20	50	ns	12
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	—	10	—	ns	
$\overline{CAS}$ Precharge Time (Page Mode Cycle Only)	t_{CEHCEL}	t_{CP}	10	—	10	—	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	—	15	—	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	—	20	—	ns	
Column Address Hold Time Referenced to $\overline{RAS}$	t_{RELAX}	t_{AR}	60	—	75	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{AVREH}	t_{RAL}	40	—	50	—	ns	

(continued)

NOTES:

1. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
6. Measured with a current load equivalent to 2 TTL (–200 µA, +4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
8. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
9. Assumes that $t_{RAD} \geq t_{RAD}$ (max).
10. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
12. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled by t_{AA}.

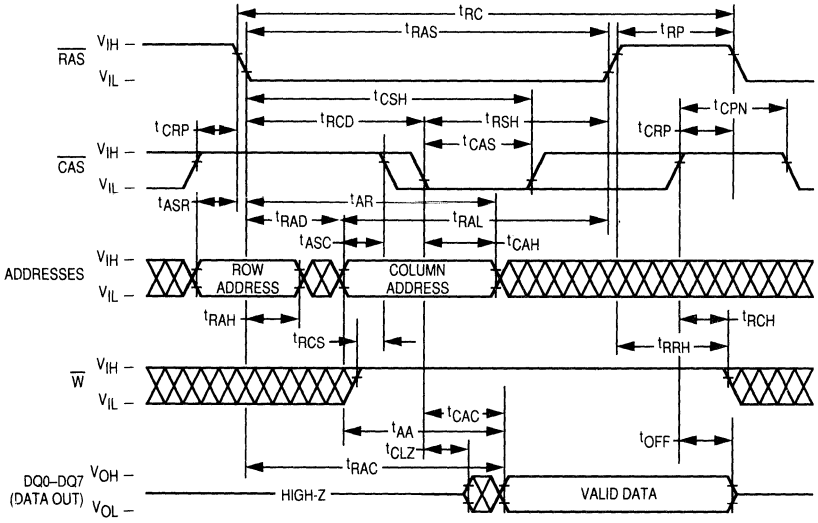
READ AND WRITE CYCLES (Continued)

Parameter	Symbol		MCM94000-80		MCM94000-10		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	0	—	ns	
Read Command Hold Time Referenced to $\overline{CAS}$	t_{CEHWX}	t_{RCH}	0	—	0	—	ns	13
Read Command Hold Time Reference to $\overline{RAS}$	t_{REHWX}	t_{RRH}	0	—	0	—	ns	13
Write Command Hold Time Referenced to $\overline{CAS}$	t_{CELWH}	t_{WCH}	15	—	20	—	ns	
Write Command Hold Time Reference to $\overline{RAS}$	t_{RELWH}	t_{WCR}	60	—	75	—	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	15	—	20	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{WLREH}	t_{RWL}	20	—	25	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{WLCEH}	t_{CWL}	20	—	25	—	ns	
Data in Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	ns	14, 15
Data in Hold Time	t_{CELDX}	t_{DH}	15	—	20	—	ns	14, 15
Data in Hold Time Referenced to $\overline{RAS}$	t_{RELDX}	t_{DHR}	60	—	75	—	ns	
Refresh Period MCM94000 MCM9L4000	t_{RVRV}	t_{RFSH}	— —	16 128	— —	16 128	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	—	0	—	ns	15, 16
$\overline{CAS}$ Setup Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEL}	t_{CSR}	5	—	20	—	ns	
$\overline{CAS}$ Hold Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEH}	t_{CHR}	15	—	20	—	ns	
$\overline{CAS}$ Precharge to $\overline{CAS}$ Active Time	t_{REHCEL}	t_{RPC}	0	—	0	—	ns	
$\overline{CAS}$ Precharge Time for $\overline{CAS}$ Before $\overline{RAS}$ Counter Test	t_{CEHCEL}	t_{CPT}	40	—	50	—	ns	
$\overline{CAS}$ Precharge Time	t_{CEHCEL}	t_{CPN}	10	—	10	—	ns	

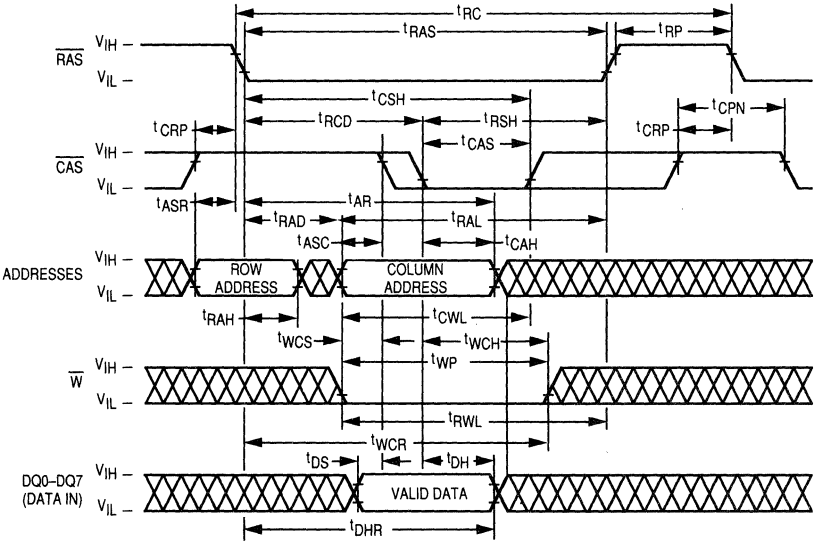
NOTES:

13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. These parameters are reference to $\overline{CAS}$ leading edge in random write cycles.
15. Early write only ($t_{WCS} \geq t_{WCS}$ (min)).
16. t_{WCS} is not a restrictive operating parameter. It is included in the data sheet as an electrical characteristic only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle. If this condition is not satisfied, the condition of the data out (at access time) is indeterminate.

READ CYCLE



EARLY WRITE CYCLE



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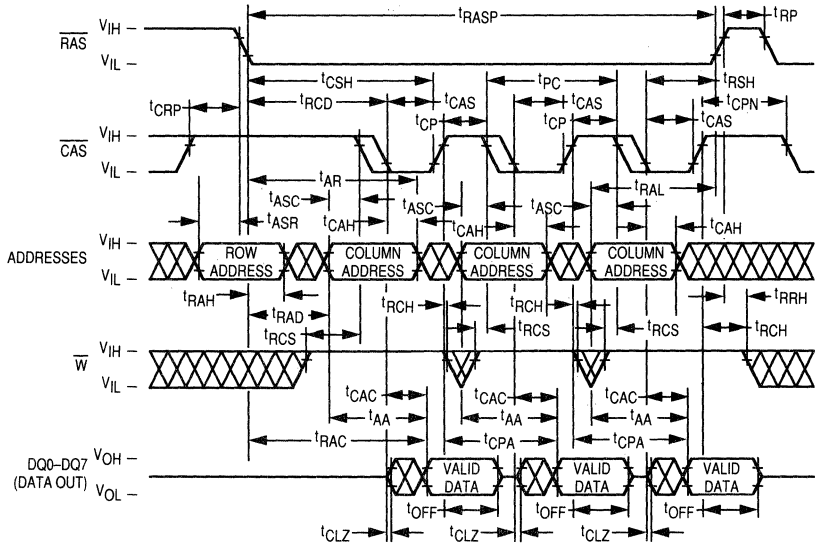
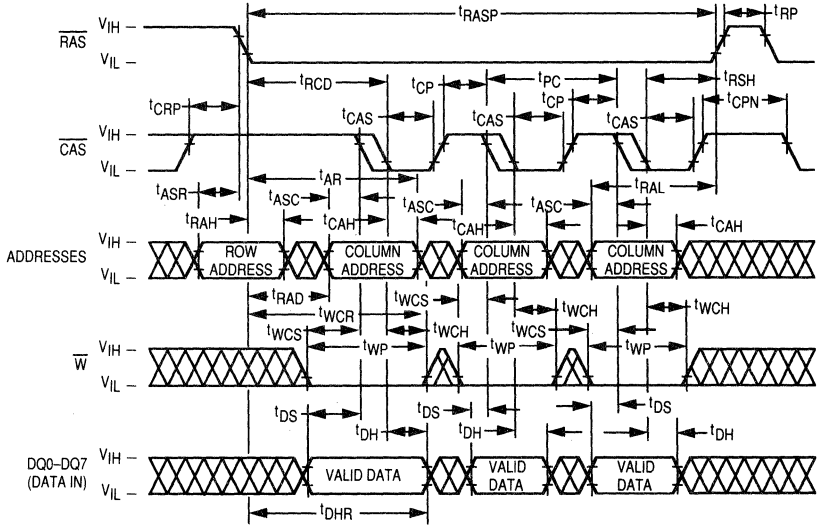
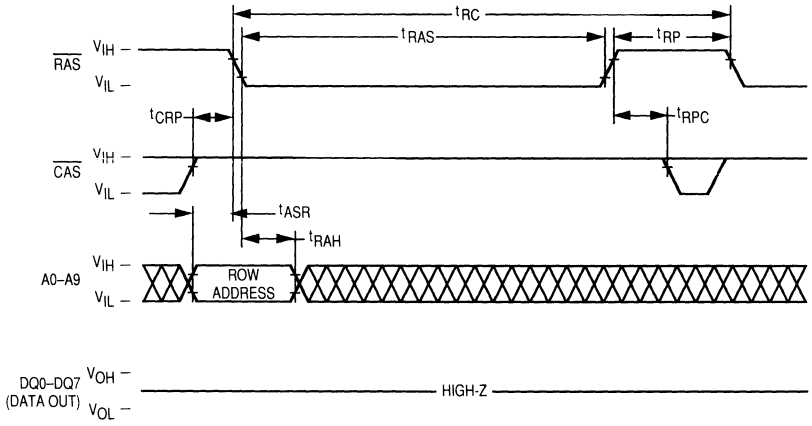
FAST PAGE MODE READ CYCLE



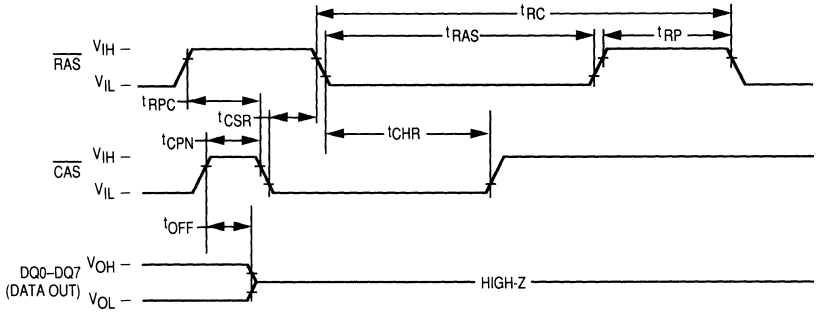
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



$\overline{RAS}$ ONLY REFRESH CYCLE
($\overline{W}$ and A10 are Don't Care)



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE
(A0 to A10 are Don't Care)



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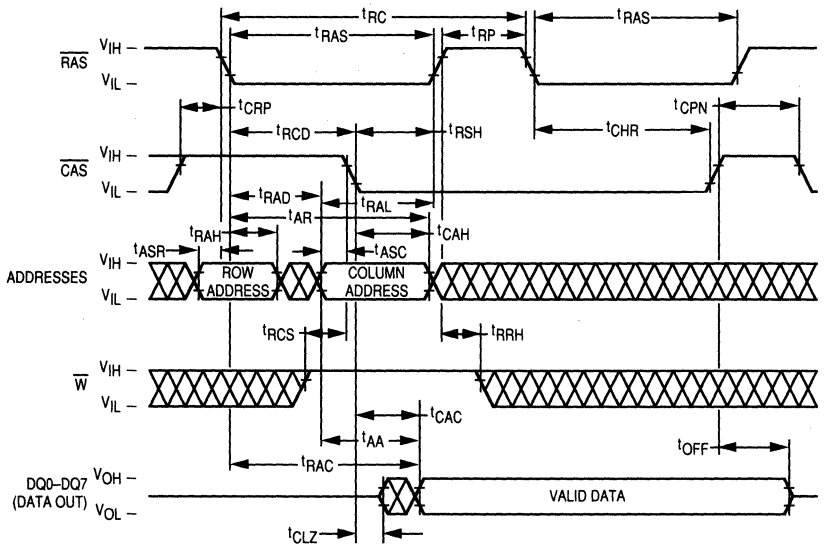
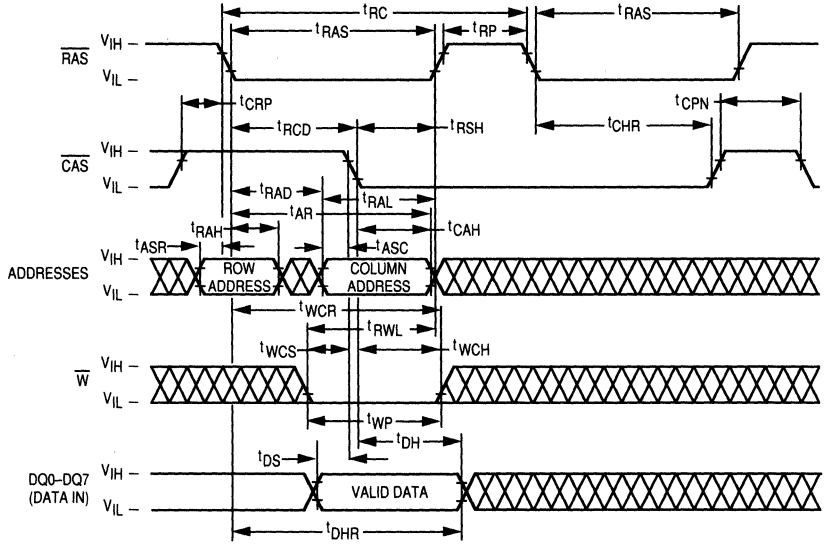
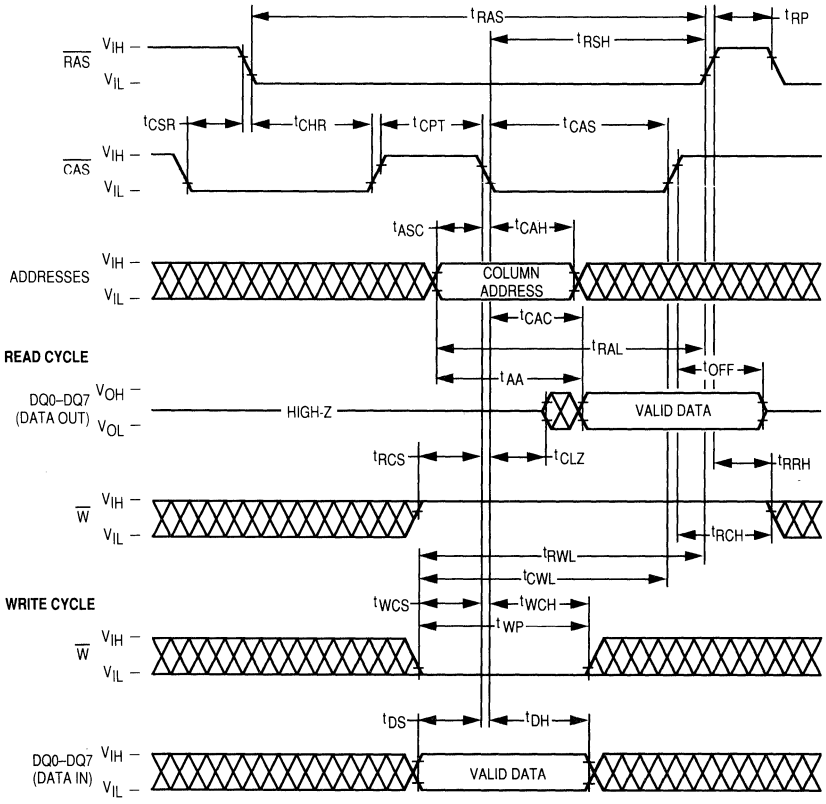
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



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DEVICE INITIALIZATION

On power-up an initial pause of 200 microseconds is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize all dynamic nodes within the RAM. During an extended inactive state (greater than 16 milliseconds with device powered up), a wake up sequence of eight active cycles is necessary to assure proper operation.

ADDRESSING THE RAM

The eleven address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks, row address strobe ($\overline{RAS}$) and column address strobe ($\overline{CAS}$), into two separate 11-bit address fields. A total of twenty two address bits, eleven rows and eleven columns, will decode one of the 4,194,304 byte locations in the device. $\overline{RAS}$ active transition is followed by $\overline{CAS}$ active transition (active = V_{IL}, t_{RCD} minimum) for all read or write cycles. The delay between $\overline{RAS}$ and $\overline{CAS}$ active transition, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

The external $\overline{CAS}$ signal is ignored until an internal $\overline{RAS}$ signal is available. This "gate" feature on the external $\overline{CAS}$ clock enables the internal $\overline{CAS}$ line as soon as the row address hold time (t_{RAH}) specification is met (and defines t_{RCD} minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{CAS}$ clock.

There are three other variations in addressing the 4M RAM: **$\overline{RAS}$ only refresh cycle**, **$\overline{CAS}$ before $\overline{RAS}$ refresh cycle**, and **page mode**. All three are discussed in separate sections that follow.

READ CYCLE

The DRAM may be read with two different cycles: "normal" random read cycle, and page mode read cycle. The normal read cycle is outlined here, while the page mode cycle is discussed in a separate section.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with the $\overline{RAS}$ and $\overline{CAS}$ active transitions latching the desired bit location. The write ($\overline{W}$) input level must be high (V_{IH}), t_{RCS} (minimum) before the $\overline{CAS}$ active transition, to enable read mode.

Both the $\overline{RAS}$ and $\overline{CAS}$ clocks trigger a sequence of events which are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window. However, $\overline{CAS}$ must be active before or at t_{RCD} maximum to guarantee valid data out (Q) at t_{RAC} (access time from $\overline{RAS}$ active transition). If the t_{RCD} maximum is exceeded, read access time is determined by the $\overline{CAS}$ clock active transition (t_{CAC}).

The $\overline{RAS}$ and $\overline{CAS}$ clocks must remain active for a minimum time of t_{RAS} and t_{CAS} respectively, to complete the read cycle. $\overline{W}$ must remain high throughout the cycle, and for time t_{RRH} or t_{RCH} after $\overline{RAS}$ or $\overline{CAS}$ inactive transition, respectively, to maintain the data at that bit location. Once $\overline{RAS}$ transitions to inactive, it must remain inactive for a minimum time of t_{RP} to precharge the internal device circuitry for the next active cycle. Q is valid, but not latched, as long as the $\overline{CAS}$ clock is active. When the $\overline{CAS}$ clock transitions to inactive, the output will switch to High Z (three-state).

WRITE CYCLE

The user can write to the DRAM with two cycles; early write and page mode early write. Early write mode is discussed here, while the page mode write operation is covered in another section.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of $\overline{W}$ to active (V_{IL}). Minimum active time t_{RAS} and t_{CAS}, and precharge time t_{RP} apply to write mode, as in the read mode.

An early write cycle is characterized by $\overline{W}$ active transition at minimum time t_{WCS} before $\overline{CAS}$ active transition. Data in (D) is referenced to $\overline{CAS}$ in an early write cycle. $\overline{RAS}$ and $\overline{CAS}$ clocks must stay active for t_{RWL} and t_{CWL}, respectively, after the start of the early write operation to complete the cycle.

Q remains in three-state condition throughout an early write cycle because $\overline{W}$ active transition precedes or coincides with $\overline{CAS}$ active transition, keeping data-out buffers disabled.

PAGE-MODE CYCLES

Page mode allows fast successive data operations at all 2048 column locations on a selected row of the dynamic RAM. Read access time in page mode (t_{CAC}) is typically half the regular $\overline{RAS}$ clock access time, t_{RAC}. Page mode operation consists of keeping $\overline{RAS}$ active while toggling $\overline{CAS}$ between V_{IH} and V_{IL}. The row is latched by $\overline{RAS}$ active transition, while each $\overline{CAS}$ active transition allows selection of a new-column location on the row.

A page mode cycle is initiated by a normal read or write cycle, as described in prior sections. Once the timing requirements for the first cycle are met, $\overline{CAS}$ transitions to inactive for minimum of t_{CP}, while $\overline{RAS}$ remains low (V_{IL}). The second $\overline{CAS}$ active transition while $\overline{RAS}$ is low initiates the first page mode cycle (t_{PC} or t_{PRWC}). Either a read or write operation can be performed in a page mode cycle, subject to the same conditions as in normal operation (previously described). These operations can be intermixed in consecutive page mode cycles and performed in any order. The maximum number of consecutive page mode cycles is limited by t_{RASP}. Page mode operation is ended when $\overline{RAS}$ transitions to inactive, coincident with or following $\overline{CAS}$ inactive transition.

REFRESH CYCLES

The dymanic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Each byte must be periodically **refreshed** (recharged) to maintain the correct byte state. Bytes in the MCM94000 require refresh every 16 milliseconds, while refresh time for the MCM9L4000 is 128 milliseconds.

This is accomplished by cycling through the 1024 row addresses in sequence within the specified refresh time. All the bytes on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds for the MCM94000, and 124.8 microseconds for

the MCM9L4000. Burst refresh, a refresh of all 1024 rows consecutively, must be performed every 16 milliseconds on the MCM94000 and 128 milliseconds on the MCM9L4000.

A normal read, write, or read-write operation to the RAM will refresh all the bytes (4096) associated with the particular row decoded. Three other methods of refresh, **$\overline{\text{RAS}}$-only refresh**, **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh**, and **hidden refresh** are available on this device for greater system flexibility.

$\overline{\text{RAS}}$-Only Refresh

$\overline{\text{RAS}}$-only refresh consists of $\overline{\text{RAS}}$ transition to active, latching the row address to be refreshed, while $\overline{\text{CAS}}$ remains high (V_{IH}) throughout the cycle. An external counter is employed to ensure all rows are refreshed within the specified limit.

$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh

$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh is enabled by bringing $\overline{\text{CAS}}$ active before $\overline{\text{RAS}}$. This clock order activates an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle. The output buffer remains at the same state it was in during the previous cycle (hidden refresh).

Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding $\overline{\text{CAS}}$ active the end of a read or write cycle, while $\overline{\text{RAS}}$ cycles inactive for t_{RP} and back to active, starts the hidden refresh. This is essentially the execution of a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh from a cycle in progress (see Figure 1).

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST

The internal refresh counter of this device can be tested with a **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test**. This test is performed with a read-write operation. During the test, the internal refresh counter generates the row address, while the external address supplies the column address. The entire array is refreshed after 1024 cycles, as indicated by the check data written in each row. See **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test cycle** timing diagram.

The test can be performed after a minimum of **8 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$** initialization cycles. Test procedure:

1. Write "0"s into all memory cells (normal write mode).
2. Select a column address, and read "0" out of the cell by performing **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test, read cycle.** Repeat this operation 1024 times.
3. Select a column address, and write "1" into the cell by performing **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test, write cycle.** Repeat this operation 1024 times.
4. Read "1"s (normal read mode), which were written at step 3.
5. Repeat steps 1 to 4 using complement data.

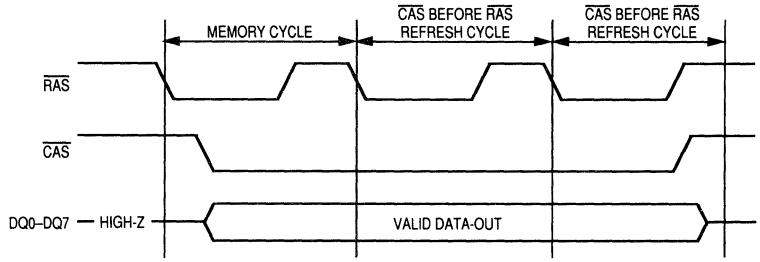
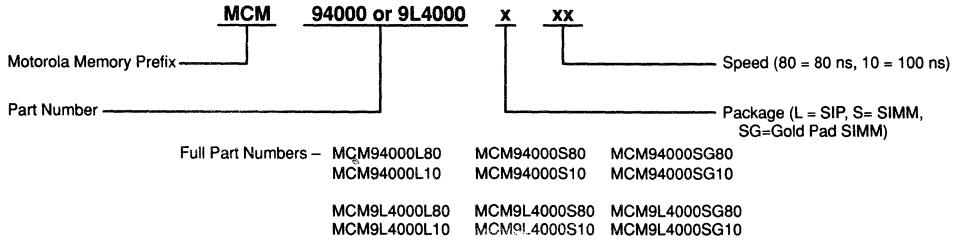


Figure 1. Hidden Refresh Cycle

ORDERING INFORMATION
(Order by Full Part Number)

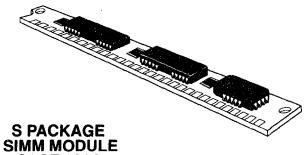


MCM94256

3

Product Preview

256K × 9 Bit Dynamic Random Access Memory Module

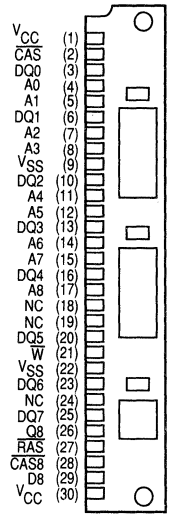


S PACKAGE
SIMM MODULE
CASE 839A

The MCM94256S is a 2.25M bit, dynamic random access memory (DRAM) module organized as 262,144 x 9 bits. The module is a 30-lead single-in-line memory module (SIMM) consisting of two MCM514256A DRAMs housed in 20/26 J-lead small outline packages (SOJ) and one CMOS 256K x 1 DRAM housed in an 18-lead PLCC package, mounted on a substrate along with a 0.22 µF (min) decoupling capacitor mounted adjacent to each DRAM. The MCM514256A is a 1.0µ CMOS high speed, dynamic random access memory organized as 262,144 four-bit words and fabricated with CMOS silicon-gate process technology.

- Three-State Data Output
- Early-Write Common I/O Capability
- Fast Page Mode Capability
- TTL-Compatible Inputs and Outputs
- $\overline{RAS}$ Only Refresh
- $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- Hidden Refresh
- 512 Cycle Refresh:
  MCM94256 = 8 ms (Max)
- Consists of Two 256K x 4 DRAMs, One 256K x 1 DRAM, and Three 0.22 µF (Min) Decoupling Capacitors
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}):
  MCM94256S-70 = 70 ns (Max)
  MCM94256S-80 = 80 ns (Max)
  MCM94256S-10 = 100 ns (Max)
- Low Active Power Dissipation:
  MCM94256S-70 = 1.32 W (Max)
  MCM94256S-80 = 1.16 W (Max)
  MCM94256S-10 = 1.05 W (Max)
- Low Standby Power Dissipation:
  TTL Levels = 33 mW (Max)
  CMOS Levels = 16.5 mW (Max)
- $\overline{CAS}$ Control for Eight Common I/O Lines
- $\overline{CAS}$ Control for Separate I/O Pair

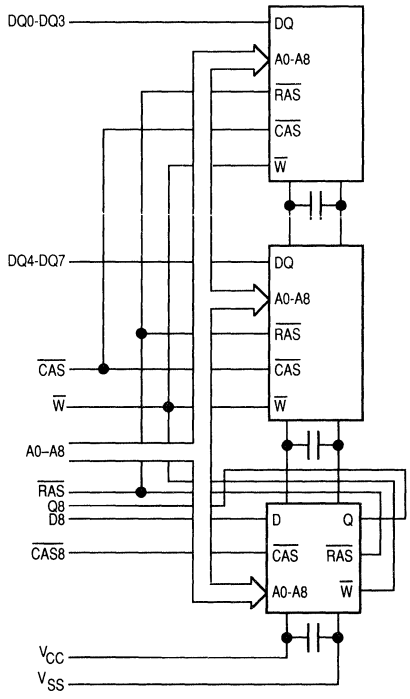
30-PIN
SINGLE IN-LINE PACKAGE
(TOP VIEW, MCM94256)



PIN NAMES	
A0–A8	Address Inputs
DQ0–DQ7	Data Input/Output
D8	Data Input
Q8	Data Output
$\overline{CAS}$	Column Address Strobe
$\overline{CAS8}$	Column Address Strobe
$\overline{RAS}$	Row Address Strobe
$\overline{W}$	Read/Write Input
V_{CC}	Power (+5 V)
V_{SS}	Ground
NC	No Connection

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	–1 to +7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	–1 to +7	V
Data Out Current per DQ Pin	I_{out}	50	mA
Power Dissipation	P_D	2.6	W
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	–55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

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DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V	1
	V_{SS}	0	0	0		
Logic High Voltage, All Inputs	V_{IH}	2.4	—	6.5	V	1
Logic Low Voltage, All Inputs	V_{IL}	–1.0	—	0.8	V	1

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current	I_{CC1}			mA	2
MCM94256-70, t_{RC} = 130 ns		—	240		
MCM94256-80, t_{RC} = 150 ns		—	210		
MCM94256-10, t_{RC} = 180 ns		—	190		
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	—	6	mA	
V_{CC} Power Supply Current During $\overline{RAS}$ only Refresh Cycle	I_{CC3}			mA	2
MCM94256-70, t_{RC} = 130 ns		—	240		
MCM94256-80, t_{RC} = 150 ns		—	210		
MCM94256-10, t_{RC} = 180 ns		—	190		
V_{CC} Power Supply Current During Fast Page Mode Cycle	I_{CC4}			mA	2
MCM94256-70, t_{PC} = 40 ns		—	180		
MCM94256-80, t_{PC} = 45 ns		—	150		
MCM94256-10, t_{PC} = 55 ns		—	130		
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)	I_{CC5}	—	3	mA	
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle	I_{CC6}			mA	2
MCM94256-70, t_{RC} = 130 ns		—	240		
MCM94256-80, t_{RC} = 150 ns		—	210		
MCM94256-10, t_{RC} = 180 ns		—	190		
Input Leakage Current ($V_{SS} \le V_{in} \le V_{CC}$)	$I_{lkg(I)}$	–30	30	µA	
Output Leakage Current ($\overline{CAS}$ at Logic 1, $V_{SS} \le V_{in} \le V_{CC}$)	$I_{lkg(O)}$	–10	10	µA	
Output High Voltage (I_{OH} = –5 mA)	V_{OH}	2.4	—	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	—	0.4	V	

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Max	Unit	Notes
Input Capacitance	A0–A8, $\overline{W}$, $\overline{CAS}$, $\overline{RAS}$	C_{in}	20	pF	3
	D8, $\overline{CAS8}$		7		
Input/Output Capacitance	DQ0–DQ7	$C_{I/O}$	15	pF	3
Output Capacitance	Q8	C_{out}	10	pF	3

NOTES:

1. All voltages referenced to V_{SS}.
2. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
3. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\Delta t/\Delta V$.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted

READ AND WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM94256–70		MCM94256–80		MCM94256–10		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	130	—	150	—	180	—	ns	5
Page Mode Cycle Time	t_{CELCEL}	t_{PC}	40	—	45	—	55	—	ns	
Access Time from $\overline{RAS}$	t_{RELQV}	t_{RAC}	—	70	—	80	—	100	ns	6, 7
Access Time from $\overline{CAS}$	t_{CELQV}	t_{CAC}	—	20	—	20	—	25	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	—	35	—	40	—	50	ns	6, 9
Access Time from Precharge $\overline{CAS}$	t_{CEHQV}	t_{CPA}	—	35	—	40	—	50	ns	6
$\overline{CAS}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	0	—	0	—	0	—	ns	6
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	20	0	20	0	20	ns	10
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{REHREL}	t_{RP}	50	—	60	—	70	—	ns	
$\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ Hold Time	t_{CELREH}	t_{RSH}	20	—	20	—	25	—	ns	
$\overline{CAS}$ Hold Time	t_{RELCEH}	t_{CSH}	70	—	80	—	100	—	ns	
$\overline{CAS}$ Pulse Width	t_{CELCEH}	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RELCEL}	t_{RCD}	20	50	20	60	25	75	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	35	15	40	20	50	ns	12
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	—	5	—	10	—	ns	
$\overline{CAS}$ Precharge Time (Page Mode Cycle Only)	t_{CEHCEL}	t_{CP}	10	—	10	—	10	—	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	—	10	—	15	—	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	—	15	—	20	—	ns	
Column Address Hold Time Referenced to $\overline{RAS}$	t_{RELAX}	t_{AR}	55	—	60	—	75	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{AVREH}	t_{RAL}	36	—	40	—	50	—	ns	

(continued)

NOTES:

1. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
6. Measured with a current load equivalent to 2 TTL (–200 µA, +4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
8. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
9. Assumes that $t_{RAD} \geq t_{RAD}$ (max).
10. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
12. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled by t_{AA}.

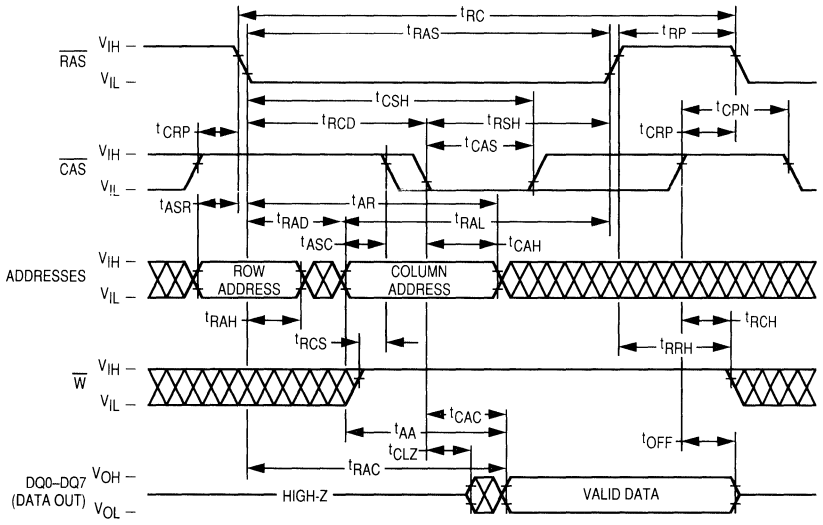
READ AND WRITE CYCLES (Continued)

Parameter	Symbol		MCM94256–70		MCM94256–80		MCM94256–10		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time Referenced to $\overline{CAS}$	t_{CEHWX}	t_{RCH}	0	—	0	—	0	—	ns	13
Read Command Hold Time Referenced to $\overline{RAS}$	t_{REHWX}	t_{RRH}	0	—	0	—	0	—	ns	13
Write Command Hold Time Referenced to $\overline{CAS}$	t_{CELWH}	t_{WCH}	15	—	15	—	20	—	ns	
Write Command Hold Time Reference to $\overline{RAS}$	t_{RELWH}	t_{WCR}	55	—	60	—	75	—	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	15	—	15	—	20	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{WLREH}	t_{RWL}	20	—	20	—	25	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{WLCEH}	t_{CWL}	20	—	20	—	25	—	ns	
Data in Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	0	—	ns	14, 15
Data in Hold Time	t_{CELDX}	t_{DH}	15	—	15	—	20	—	ns	14, 15
Data in Hold Time Referenced to $\overline{RAS}$	t_{RELDX}	t_{DHR}	55	—	60	—	75	—	ns	
Refresh Period	t_{RVRV}	t_{RFSH}	—	4	—	4	—	4	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	—	0	—	0	—	ns	15, 16
$\overline{CAS}$ Setup Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEL}	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEH}	t_{CHR}	30	—	30	—	30	—	ns	
$\overline{CAS}$ Precharge to $\overline{CAS}$ Active Time	t_{REHCEL}	t_{RPC}	0	—	0	—	0	—	ns	
$\overline{CAS}$ Precharge Time for $\overline{CAS}$ Before $\overline{RAS}$ Counter Test	t_{CEHCEL}	t_{CPT}	40	—	40	—	50	—	ns	
$\overline{CAS}$ Precharge Time	t_{CEHCEL}	t_{CPN}	10	—	10	—	15	—	ns	

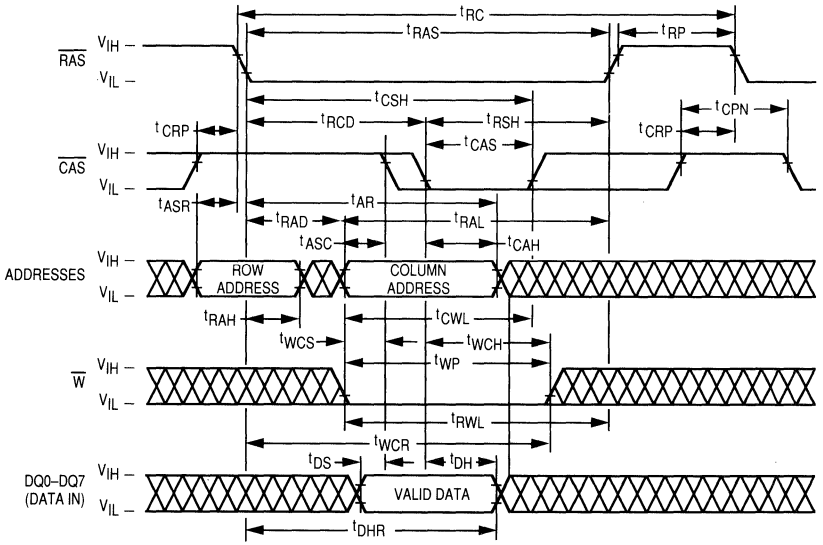
NOTES:

13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. These parameters are reference to $\overline{CAS}$ leading edge in random write cycles.
15. Early write only ($t_{WCS} \geq t_{WCS}$ (min)).
16. t_{WCS} is not a restrictive operating parameter. It is included in the data sheet as an electrical characteristic only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle. If this condition is not satisfied, the condition of the data out (at access time) is indeterminate.

READ CYCLE



EARLY WRITE CYCLE



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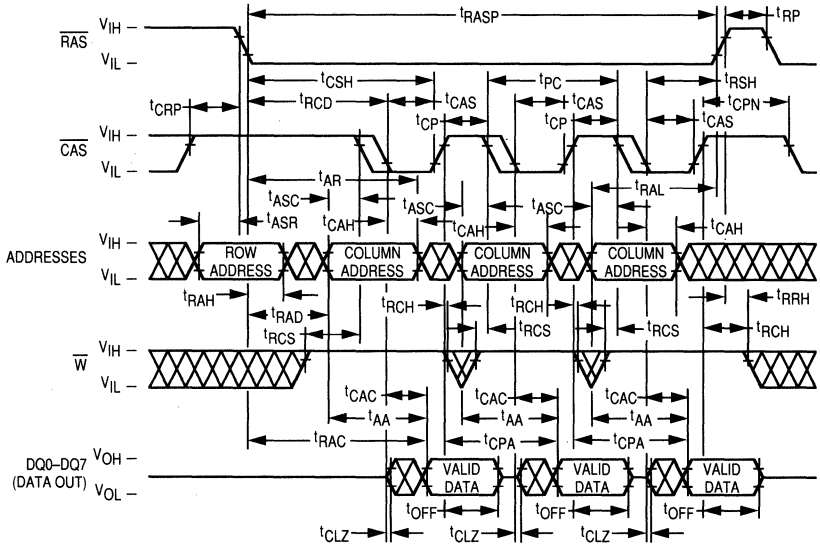
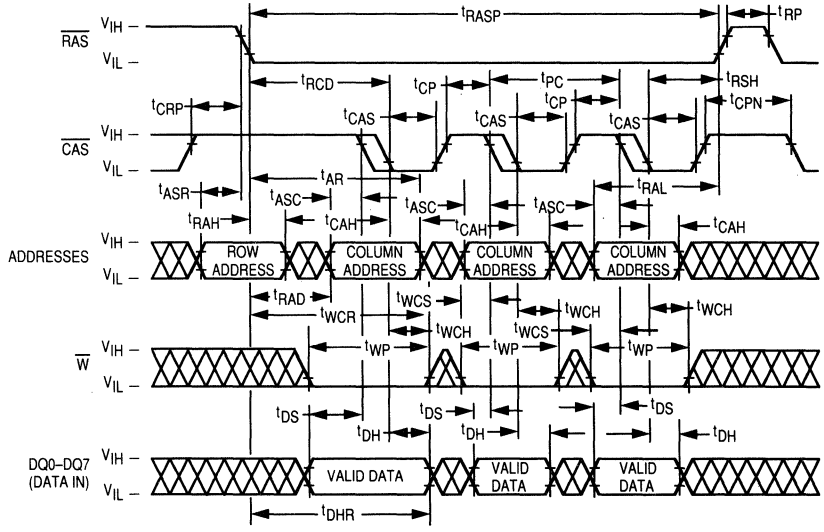
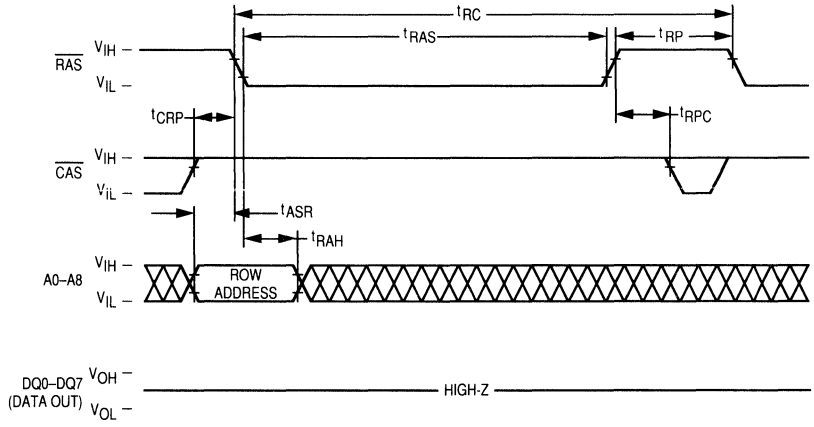
FAST PAGE MODE READ CYCLE



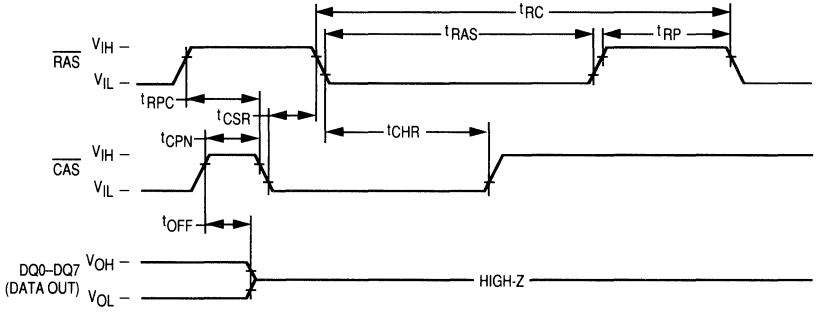
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



$\overline{RAS}$ ONLY REFRESH CYCLE
($\overline{W}$ and A8 are Don't Care)



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE
($\overline{W}$ and A0 to A8 are Don't Care)



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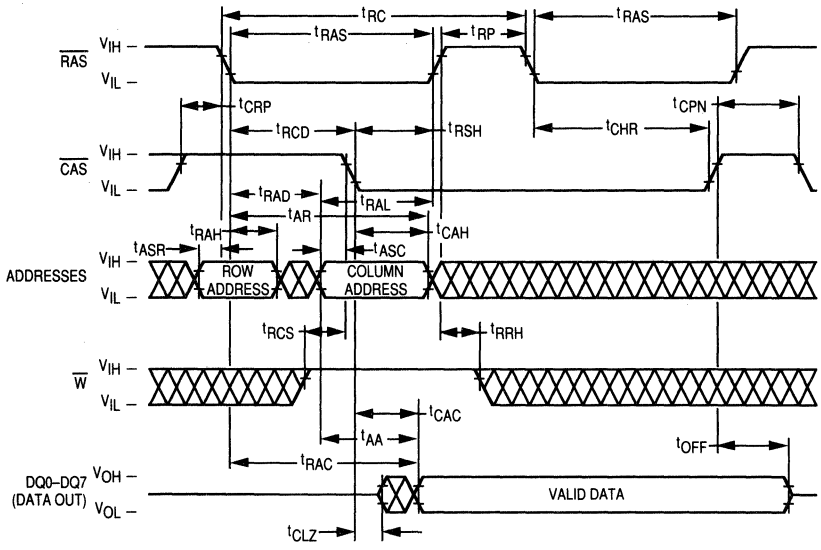
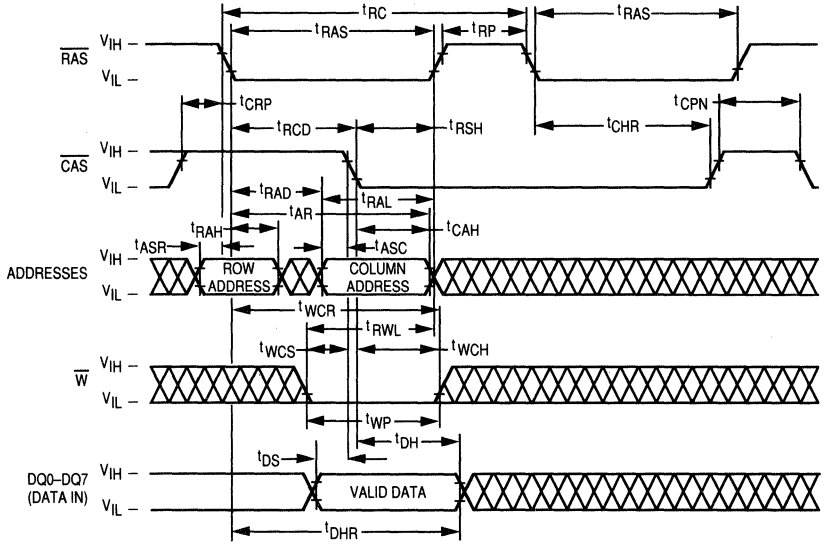
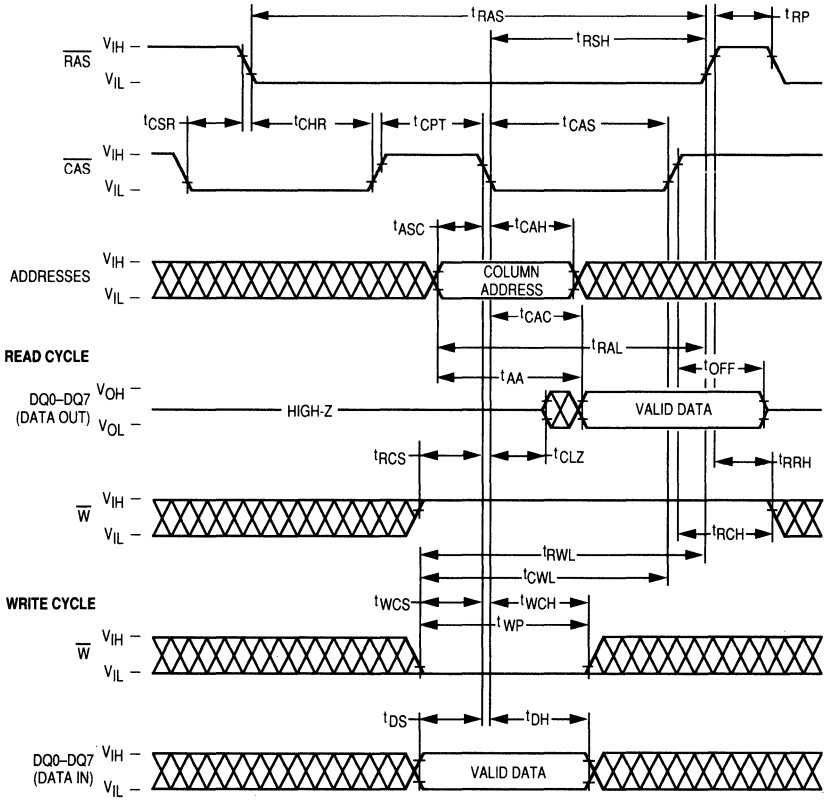
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



DEVICE INITIALIZATION

On power-up an initial pause of 200 microseconds is required for the internal substrate generator pump to establish the correct bias voltage. This is to be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize the various dynamic nodes internal to the device. During an extended inactive state of the device (greater than 4 milliseconds with device powered up), the wake up sequence (8 active cycles) will be necessary to assure proper device operation.

ADDRESSING THE RAM

The nine address bus pins on the device are time multiplexed with two separate 9-bit address fields that are strobed at the beginning of the memory cycle by two clocks (active negative) called the row address strobe ($\overline{RAS}$) and the column address strobe ($\overline{CAS}$). A total of eighteen address bits will decode one of the 262,144 byte locations in the device. The column address strobe follows the row address strobe by a specified minimum and maximum time called "t_{RCD}," which is the row to column strobe delay. This time interval is also referred to as the multiplex window which gives flexibility to a system designer to set up the external addresses into the RAM. These conditions have to be met for normal read or write cycles. This initial portion of the cycle accomplishes the normal addressing of the device. There are, however, other variations in addressing the module: the refresh modes ($\overline{RAS}$ only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, hidden refresh), and another mode called page mode, which allows the user to column access the 512 bits within a selected row. The refresh mode and page mode operations are described in more detail in later sections.

READ CYCLE

A read cycle is referred to as a normal read cycle to differentiate it from a page mode read cycle, which is covered in a later section.

The memory read cycle begins with the row addresses valid and the $\overline{RAS}$ clock transitioning from V_{IH} to the V_{IL} level. The $\overline{CAS}$ clock must also make a transition from V_{IH} to the V_{IL} level at the specified t_{RCD} timing limits when the column addresses are latched. Both the $\overline{RAS}$ and $\overline{CAS}$ clocks trigger a sequence of events which are controlled by several delayed internal clocks. Also, these clocks are linked in such a manner that the access time of the device is independent of the address multiplex window. The only stipulation is that the $\overline{CAS}$ clock must be active before or at the t_{RCD} maximum specification for an access (data valid) from the $\overline{RAS}$ clock edge to be guaranteed (t_{RAC}). If the t_{RCD} maximum condition is not met, the access (t_{CAC}) from the $\overline{CAS}$ clock active transition will determine read access time. The external $\overline{CAS}$ signal is ignored until an internal $\overline{RAS}$ signal is available. This gating feature on the $\overline{CAS}$ clock will allow the external $\overline{CAS}$ signal to become active as soon as the row address hold time (t_{RAH}) specification has been met and defines the t_{RCD} minimum specification. The time difference between t_{RCD} minimum and t_{RCD} maximum can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{CAS}$ clock.

Once the clocks have become active, they must stay active for the minimum (t_{RAS}) period for the $\overline{RAS}$ clock and the minimum (t_{CAS}) period for the $\overline{CAS}$ clock. The $\overline{RAS}$ clock must stay inactive for the minimum (t_{RP}) time. The former is for the competion of the cycle in progress, and the latter is for the device internal circuitry to be precharged for the next active cycle.

Data out is not latched and is valid as long as the $\overline{CAS}$ clock is active; the output will switch to the three-state mode when the $\overline{CAS}$ clock goes inactive. To perform a read cycle, the write ($\overline{W}$) input must be held at the V_{IH} level from the time the $\overline{CAS}$ clock makes its active transition (t_{RCS}) to the time when it transitions into the inactive (t_{RCH}) mode.

WRITE CYCLE

A write cycle is similar to a read cycle except that the write ($\overline{W}$) clock must go active (V_{IL} level) at or before the $\overline{CAS}$ clock goes active at a minimum t_{WCS} time. If the above condition is met, then the cycle in progress is referred to as an early write cycle. In an early write cycle, the write clock and the data in are referenced to the active transition of the $\overline{CAS}$ clock edge. There are two important parameters with respect to the write cycle: the column strobe to write lead time (t_{CWL}) and the row strobe to write lead time (t_{RWL}). These define the minimum time that $\overline{RAS}$ and $\overline{CAS}$ clocks need to be active after the write operation has started ($\overline{W}$ clock at V_{IL} level).

PAGE-MODE CYCLES

Page mode operation allows fast successive data operations at all 512 column locations on a selected row. Page access (t_{CAC}) is typically half the regular $\overline{RAS}$ clock access (t_{RAC}) on the Motorola 1M dynamic RAM. Page mode operation consists of holding the $\overline{RAS}$ clock active while cycling the $\overline{CAS}$ clock to access the column locations determined by the 9-bit column address field.

The page cycle is always initiated with a row address being provided and latched by the $\overline{RAS}$ clock, followed by the column address and $\overline{CAS}$ clock. From the timing illustrated, the initial cycle is a normal read or write cycle, that has been previously described, followed by the shorter $\overline{CAS}$ cycles (t_{PC}). The $\overline{CAS}$ cycle time (t_{PC}) consists of the $\overline{CAS}$ clock active time (t_{CAS}), and $\overline{CAS}$ clock precharge time (t_{CP}) and two transitions. In practice, any combination of read and write cycles can be performed to suit a particular application.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Therefore, to retain the correct information, the module needs to be refreshed at least once every 8 milliseconds. This is accomplished by sequentially cycling through the 512 row address locations every 8 milliseconds (i.e., at least one row every 15.6 microseconds). A normal read or write operation to the module will also refresh all the bytes associated with the particular row(s) decoded.

RAS-Only Refresh

In this refresh method, the system must perform a RAS-only cycle on 512 row addresses every 8 milliseconds. The row addresses are latched in with the RAS clock, and the associated internal row locations are refreshed. As the heading implies, the CAS clock is not required and must be inactive or at a V_{IH} level.

CAS Before RAS Refresh

This refresh cycle is initiated when RAS falls, after CAS has been low (by t_{CSR}). This activates the internal refresh counter which generates the row address to be refreshed. Externally applied addresses are ignored during the automatic refresh cycle. If the output buffer was off before the automatic refresh cycle, the output will stay in the high impedance state. If the output was enabled by CAS in the previous cycle, the data out will be maintained during the automatic refresh cycle as long as CAS is held active (hidden refresh).

Hidden Refresh

The hidden refresh method allows refresh cycles to be performed while maintaining valid data at the output pin. Hidden refresh is performed by holding CAS at V_{IL} and taking RAS high and after a specified precharge period (t_{RP}), executing a CAS before RAS refresh cycle. (See Figure 1.)

CAS BEFORE RAS REFRESH COUNTER TEST

The internal refresh counter of this device can be tested with a **CAS before RAS refresh counter test.** This refresh counter test is performed with read and write operations. During this test, the internal refresh counter generates the row address, while the external address input supplies the column address. The entire array is refreshed after 512 test cycles, as indicated by the check data written in each row. See **CAS before RAS refresh counter test cycle** timing diagram.

The test can be performed only after a minimum of **8 CAS before RAS** initialization cycles. The test procedure is as follows:

1. Write "0"s into all memory cells (normal write mode).
2. Select a column address, and read "0" out of the cell by performing **CAS before RAS refresh counter test, read cycle.** Repeat this operation 512 times.
3. Select a column address, and write "1" into the cell by performing **CAS before RAS refresh counter test, write cycle.** Repeat this operation 512 times.
4. Read "1"s (normal read mode), which were written at step 3.
5. Repeat steps 1 to 4 using complement data.

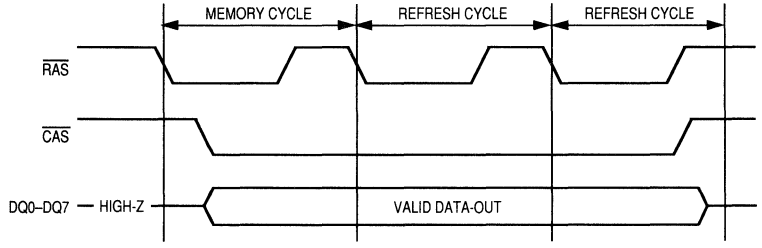
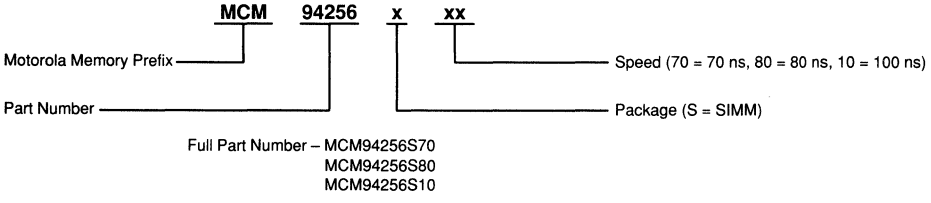


Figure 1. Hidden Refresh Cycle

ORDERING INFORMATION
(Order by Full Part Number)



Full Part Number – MCM94256S70
MCM94256S80
MCM94256S10

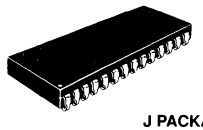
Video RAMs 4

DUAL PORT VIDEO RAMs

Density	Organi-zation	Motorola Part Number	Address Access Time (ns Max)	Operating Current (mA Max)	Pin Count	Package Options
1M	256Kx4	MCM524258A	100/120	140/150	28, 28	(Z)IP, SO(J)
	128Kx8	MCM528128A	100/120	140/150	40, 40	(P)DIP, (Z)IP, SO(J)

MCM524258A

Product Preview
256K × 4 CMOS Multiport Video RAM Page Mode



J PACKAGE
400 MIL SOJ
CASE 810

Z PACKAGE
PLASTIC
ZIG-ZAG IN-LINE
CASE TBD

4

The MCM524258A is a CMOS multiport video RAM. It is organized as a 262,144 by 4-bit word dynamic random access memory (RAM) port with a 512 by 4-bit word static, serial access, memory (SAM) port. The MCM524258A is flexible, offering: random read and write to the RAM port, high-speed read and write to the SAM port, and bidirectional transfer of data between the RAM and SAM. The RAM and SAM ports can be accessed independently, except during data transfer operations between the RAM and SAM. Special features of the MCM524258A include Page Mode, Flash Write, Block Write, and Write per Bit on the RAM port, and Split Register Data Transfer on the SAM port. The MCM524258A is fabricated with a 1.0 μ CMOS silicon gate process, which provides fast access times, low power dissipation, and wide operating margins.

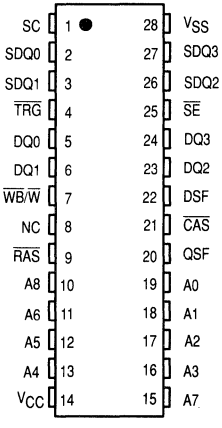
- Organization:
  - RAM Port 256K × 4 Bits
  - SAM Port 512 × 4 Bits
- RAM Port:
  - Page Mode, Block Write, Flash Write, Write Per Bit
  - 512 Cycle, 8 Millisecond Refresh
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
  - Hidden Refresh
  - Three-State Data Outputs
  - TTL Compatible Inputs and Outputs
  - Fast Access Time (t_{RAC}):
    - MCM524258A-10 = 100 ns (Max)
    - MCM524258A-12 = 120 ns (Max)
  - Low Active Power Dissipation (Max, SAM Standby):
    - MCM524258A-10 = 110 mA
    - MCM524258A-12 = 100 mA
  - Low Standby Power Dissipation (Max, SAM Standby):
    - MCM524258A-10 = 10 mA
    - MCM524258A-12 = 10 mA
- SAM Port:
  - Split Register Data Transfer
  - Static Register, No Refresh Required
  - 512 Tap Locations
  - Fast Access Time (t_{SCA}):
    - MCM524258A-10 = 25 ns (Max)
    - MCM524258A-12 = 35 ns (Max)
  - Low Serial Cycle Time (t_{SCC}):
    - MCM524258A-10 = 30 ns (Min)
    - MCM524258A-12 = 40 ns (Min)
- RAM – SAM Bidirectional Transfer:
  - Read and Write
  - Real Time Read
  - Split Read/Write

PIN NAMES	
A0–A8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{TRG}$	Data Transfer/Output Enable
$\overline{WB/W}$	Write Per Bit/Write Enable
DSF	Special Function Control
DQ0–DQ3	RAM Write Mask/ RAM Input–Output
SC	Serial Clock
$\overline{SE}$	Serial RAM Enable
SDQ0–SDQ3	SAM Input–Output
QSF	Output Split Register
V_{CC}	Power (+ 5 V)
V_{SS}	Ground
NC	No Connect

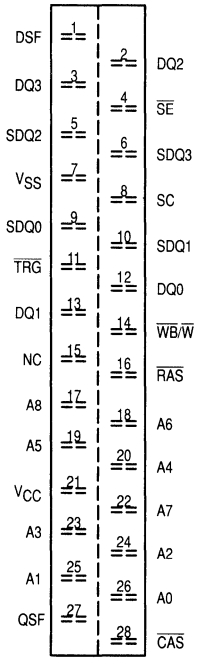
All power supply and ground pins must be connected for proper operation of the device.

PIN ASSIGNMENTS

400 MIL SOJ

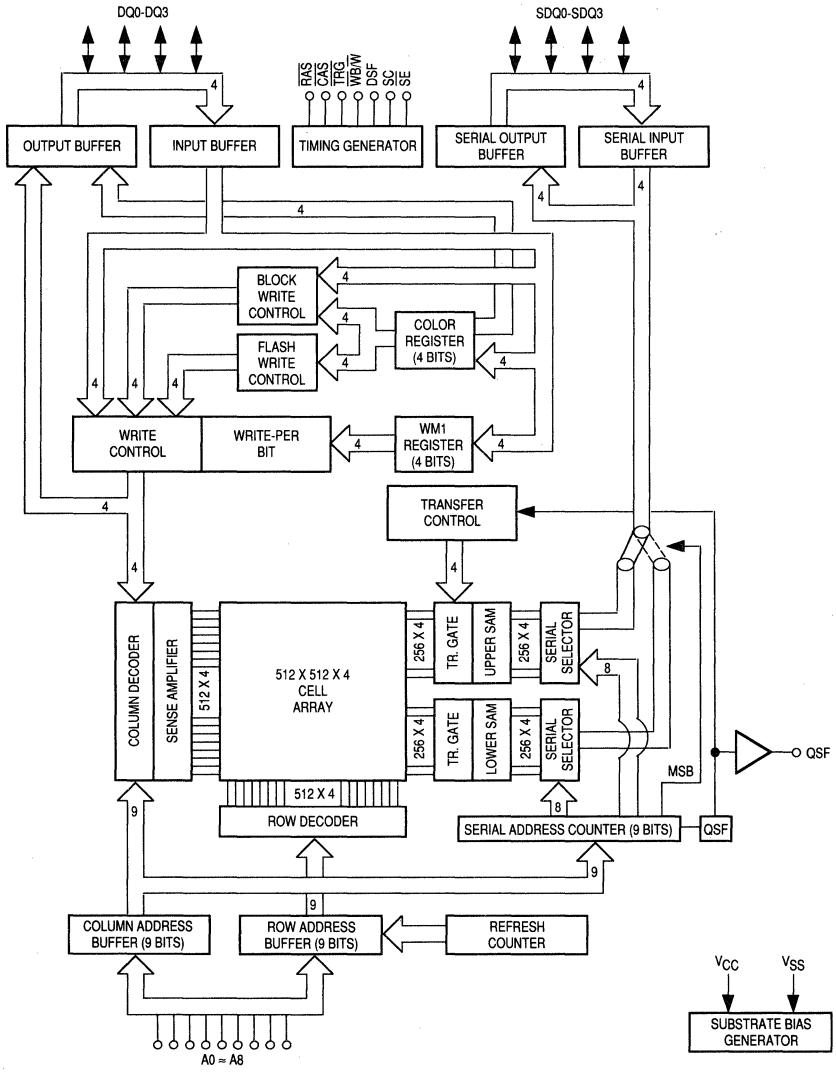


400 MIL ZIP



4

BLOCK DIAGRAM



MCM528128A

Product Preview
128K × 8 CMOS Multiport Video RAM Page Mode

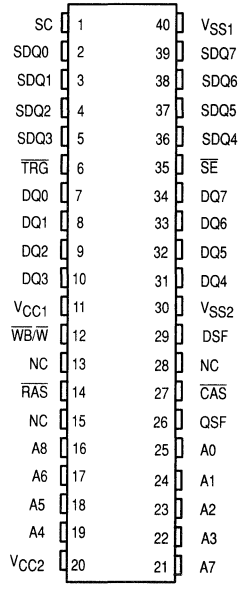
The MCM528128A is a CMOS multiport video RAM. It is organized as a 131,072 by 8-bit word dynamic random access memory (RAM) port with a 256 by 8-bit word static, serial access, memory (SAM) port. The MCM528128A is flexible, offering: random read and write to the RAM port, high-speed read and write to the SAM port, and bidirectional transfer of data between the RAM and SAM. The RAM and SAM ports can be accessed independently, except during data transfer operations between the RAM and SAM. Special features of the MCM528128A include Page Mode, Flash Write, Block Write, and Write per Bit on the RAM port, and Split Register Data Transfer on the SAM port. The MCM528128A is fabricated with a 1.0 μ CMOS silicon gate process, which provides fast access times, low power dissipation, and wide operating margins.

- Organization:
  - RAM Port 128K × 8 Bits
  - SAM Port 256 × 8 Bits
- RAM Port:
  - Page Mode, Block Write, Flash Write, Write Per Bit
  - 512 Cycle, 8 Millisecond Refresh
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
  - Hidden Refresh
  - Three-State Data Outputs
  - TTL Compatible Inputs and Outputs
  - Fast Access Time (t_{RAC}):
    - MCM528128A-10 = 100 ns (Max)
    - MCM528128A-12 = 120 ns (Max)
  - Low Active Power Dissipation (Max, SAM Standby):
    - MCM528128A-10 = 110 mA
    - MCM521288A-12 = 100 mA
  - Low Standby Power Dissipation (Max, SAM Standby):
    - MCM528128A-10 = 10 mA
    - MCM528128A-12 = 10 mA
- SAM Port:
  - Split Register Data Transfer
  - Static Register, No Refresh Required
  - 256 Tap Locations
  - Fast Access Time (t_{SCA}):
    - MCM528128A-10 = 25 ns (Max)
    - MCM528128A-12 = 35 ns (Max)
  - Low Serial Cycle Time (t_{SCC}):
    - MCM528128A-10 = 30 ns (Min)
    - MCM521288A-12 = 40 ns (Min)
- RAM – SAM Bidirectional Transfer:
  - Read and Write
  - Real Time Read
  - Split Read/Write

P PACKAGE
600 MIL PLASTIC
CASE TBD

J PACKAGE
400 MIL SOJ
CASE TBD

PIN ASSIGNMENT



PIN NAMES

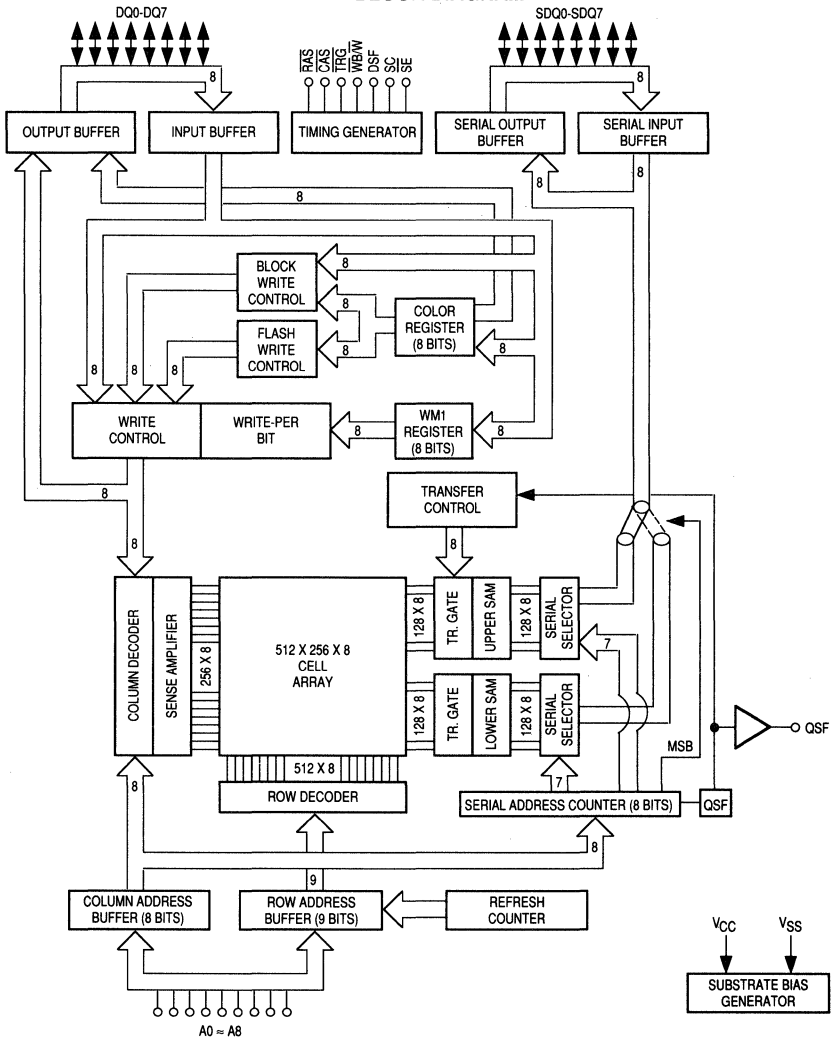
A0–A8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{TRG}$	Data Transfer/Output Enable
$\overline{WB/W}$	Write Per Bit/Write Enable
DSF	Special Function Control
DQ0–DQ7	RAM Write Mask/ RAM Input–Output
SC	Serial Clock
$\overline{SE}$	Serial RAM Enable
SDQ0–SDQ7	SAM Input–Output
QSF	Output Split Register
V_{CC1}, V_{CC2}	Power (+ 5 V)
V_{SS1}, V_{SS2}	Ground
NC	No Connect

All power supply and ground pins must be connected for proper operation of the device.

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

4

BLOCK DIAGRAM



Pseudo Static RAMs 5

5

PSEUDO STATIC RAMs (HCMOS unless otherwise noted)

Density	Organi-zation	Motorola Part Number	Address Access Time (ns Max)	Operating Current (mA Max)	Pin Count	Packaging
1M	128Kx8 Pseudo SRAM	MCM518128	100	60	32	(P)DIP, (F)&(SF)SOG
		MCM518129	100	60	32	(F)SOG
		MCM51L8128	80/100	70/60	32	(P)DIP, (F)&(SF)SOG
		MCM51L8129	80/100	70/60	32	(F)SOG
		MCM51LV8128	80/100	70/60	32	(P)DIP, (F)&(SF)SOG
		MCM51LV8129	80/100	70/60	32	(F)SOG

MCM518128
MCM51L8128
MCM51LV8128

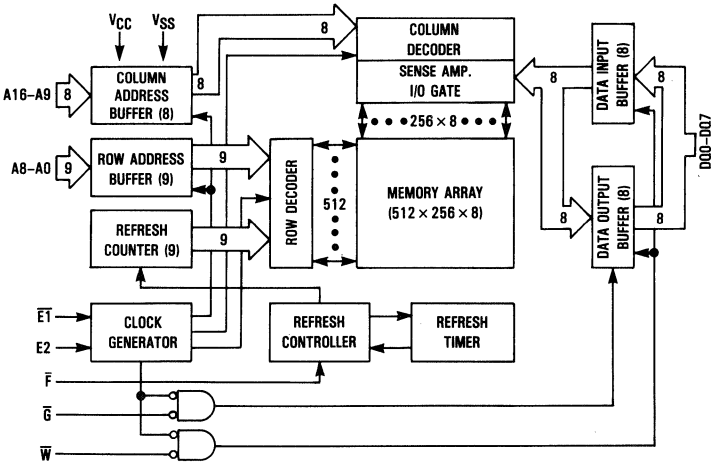
128K × 8 Bit CMOS Pseudo Static Random Access Memory

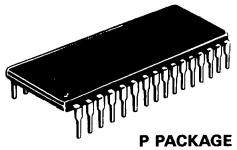
The MCM518128 is a 1,048,576 bit low-power pseudo-static random access memory organized as 131,072 words of 8 bits, fabricated using 1.0 μm silicon-gate advanced CMOS process technology. The MCM518128 family products utilize one-transistor dynamic storage cells and direct static addresses to achieve high density and fast access time. The advanced CMOS circuit design reduces power consumption and provides greater reliability. The data retention mode allows for very low power with battery backup in lap-top applications.

The refresh input ($\overline{F}$) allows two types of refresh application—auto refresh and self refresh. The MCM518128 is pin compatible with the 128K × 8 SRAM JEDEC pinout and offers a low cost alternative to 1M SRAMs and a simpler design for DRAM memory applications.

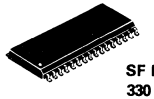
The MCM518128 is available in a 600 mil, 32 pin plastic dual-in-line package and in a narrow 32 lead plastic small outline package.

- Single 5 V Supply ± 10%
- 128K × 8 Bit Memory Organization
- Low Power Dissipation—385 mW (Maximum Active)
- TTL Compatible Inputs and Outputs
- Battery Backup Capability from 4.5 V to 5.5 V (3.0 V to 5.5 V with MCM51LV8128)
- Low Standby Current 200 μA (Maximum) with MCM51L8128 and MCM51LV8128
- Auto Refresh Power Down Function
- 512 Refresh Cycles/8 ms
- Auto Refresh is Executed by Internal Counter
- Self Refresh is Executed by Internal Timer
- Pin Compatible with 1M SRAM JEDEC Pinout
- Three State Outputs
- Fast Access Times: MCM51L8128-80/MCM51LV8128-80 = 80 ns (Max)
  MCM518128-10/MCM51L8128-10/MCM51LV8128-10 = 100 ns (Max)





P PACKAGE
600 MIL PLASTIC DIP
CASE 850



SF PACKAGE
330 MIL SOG
CASE 854

PIN ASSIGNMENT

F	1	32	VCC
A16	2	31	A15
A14	3	30	E2
A12	4	29	W
A7	5	28	A13
A6	6	27	A8
A5	7	26	A9
A4	8	25	A11
A3	9	24	G
A2	10	23	A10
A1	11	22	ET
A0	12	21	DQ7
DQ0	13	20	DQ6
DQ1	14	19	DQ5
DQ2	15	18	DQ4
VSS	16	17	DQ3

PIN NAMES

A0-A16	Address Input
W	Write Enable
ET, E2	Chip Enable
G	Output Enable
F	Refresh Input
DQ0-DQ7	Data Input/Output
VCC	Power Supply
VSS	Ground

5

TRUTH TABLE

$\overline{E1}$	E2	$\overline{G}$	$\overline{W}$	$\overline{F}$	Mode	Supply Current	I/O Pin
L	H	L	H	H/L	Read*	I_{CCA}	D_{out}
L	H	X	L	H/L	Write*	I_{CCA}	D_{in}
L	H	H*	H*	H/L	CE Only Refresh	I_{CCA}	High Z
H	X	X	X	⊓⊓⊓	Auto Refresh	I_{CCF3}	High Z
X	L	X	X	⊓⊓⊓	Auto Refresh	I_{CCF3}	High Z
H	X	X	X	L	Self Refresh	I_{CCF}**	High Z
X	L	X	X	L	Self Refresh	I_{CCF}**	High Z
H	X	X	X	H	Standby	I_{SB}***	High Z
X	L	X	X	H	Standby	I_{SB}***	High Z

$L = V_{IL}$ $H = V_{IH}$ X = don't care ⊓⊓⊓ = Toggle $H/L = V_{IH}$ or V_{IL}, but must not toggle

*The Read and Write operations effectively perform a CE Only Refresh of the row being addressed.

**I_{CCF1} or I_{CCF2} depending on input voltage levels (see DC Characteristics).

***I_{SB1} or I_{SB2} depending on input voltage levels (see DC Characteristics).

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

5

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−1.0 to 7.0	V
Voltage to Any Pin with Respect to V_{SS}	V_{in}, V_{out}	−1.0 to 7.0	V
Power Dissipation	P_D	600	mW
Soldering Temperature•Time	T_{solder}	260•10	°C•s
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +150	°C
Short Circuit Output Current	I_{out}	50	mA

NOTE:
Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.4	—	6.5	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

NOTE: All voltages are referenced to GND.

DC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	−10.0	—	10.0	μA
Output Leakage Current ($\overline{E1} = V_{IH}$ or $E2 = V_{IL}$, $\overline{G} = V_{IH}$ or $\overline{W} = V_{IL}$, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	−10.0	—	10.0	μA
Operating Current ($\overline{E1} = V_{IL}$ and $E2 = V_{IH}$, Address Cycling, $t_{RC} = t_{RC}$ min) t_{RC} = 130 ns t_{RC} = 160 ns	I_{CCA}*	— —	50 40	70 60	mA
Standby Current ($\overline{E1} = V_{IH}$ or $E2 = V_{IL}$, $\overline{F} = V_{IH}$) MCM518128 MCM51L8128/MCM51LV8128	I_{SB1}	— —	— —	2 1	mA
Standby Current ($\overline{E1} \geq V_{CC} - 0.2$ V or $E2 \leq 0.2$ V, $\overline{F} \geq V_{CC} - 0.2$ V) MCM518128 MCM51L8128/MCM51LV8128	I_{SB2}**	— —	— 100	1 200	mA μA
Self Refresh Current ($\overline{E1} = V_{IH}$ or $E2 = V_{IL}$, $\overline{F} = V_{IL}$) (Average Current) MCM518128 MCM51L8128/MCM51LV8128	I_{CCF1}	— —	— —	2 1	mA
Self Refresh Current ($\overline{E1} \geq V_{CC} - 0.2$ V or $E2 \leq 0.2$ V, $\overline{F} \leq 0.2$ V) (Average Current) MCM518128 MCM51L8128/MCM51LV8128	I_{CCF2}**	— —	— 100	1 200	mA μA
Auto Refresh Current (Average Current) ($\overline{F}$ Toggling, $t_{FC} = t_{FC}$ min)	I_{CCF3}	—	—	2	mA
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	—	—	0.4	V
Output High Voltage (I_{OH} = −5.0 mA)	V_{OH}	2.4	—	—	V

*I_{CCA} depends on cycle rate and output loading. Specified values are obtained with the output open.

**In the standby and self refresh modes with $\overline{E1} \geq V_{CC} - 0.2$ V, these limits are guaranteed when $E2 \geq V_{CC} - 0.2$ V or $E2 \leq 0.2$ V. Conversely, if the device is disabled with $E2 \leq 0.2$ V, these limits are guaranteed when $\overline{E1} \geq V_{CC} - 0.2$ V or $\overline{E1} \leq 0.2$ V.

CAPACITANCE (f = 1 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Min	Max	Unit
Input Capacitance	A0-A16	C_{in}	–	5	pF
	$\overline{E1}$, E2, $\overline{G}$, $\overline{W}$, $\overline{F}$		–	7	
Output Capacitance	DQ0-DQ7	C_{out}	–	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

Input Pulse Levels . . . . . 0.6 V, 2.6 V
Input Rise/Fall Time . . . . . 5 ns
Input Timing Measurement Reference Levels . . . . . .0.8 and 2.4 V
Output Timing Measurement Reference Levels . . . . .0.8 and 2.2 V
Output Load . . . . . 2 TTL Loads and 100 pF

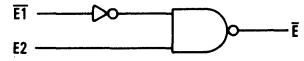
READ, WRITE, AND READ-MODIFY-WRITE CYCLES

(An initial pause of 100 μs with high $\overline{E1}$ or low E2 is required after power-up, before proper device operation is achieved.)

Parameter	Symbol		MCM51L8128-80 MCM51LV8128-80		MCM518128-10 MCM51L8128-10 MCM51LV8128-10		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Random Read, Write Cycle Time	$t_{EVEV(R)}$	t_{RC}	130	–	160	–	ns	1
Read Modify Write Cycle Time	$t_{EVEV(RW)}$	t_{RMW}	195	–	235	–	ns	1
Chip Enable Pulse Width	t_{ELEH}	t_{CE}	80	10,000	100	10,000	ns	1, 2
Chip Enable Precharge Time	t_{EHEL}	t_P	40	–	50	–	ns	1
Chip Enable Access Time	t_{ELQV}	t_{CEA}	–	80	–	100	ns	1
Output Enable Access Time	t_{GLQV}	t_{OEA}	–	35	–	40	ns	
Chip Enable to Output in Low-Z	t_{ELQX}	t_{CLZ}	30	–	30	–	ns	1
Output Enable to Output in Low-Z	t_{GLQX}	t_{OLZ}	0	–	0	–	ns	
Output Active from End of Write	t_{WHQX}	t_{WLZ}	0	–	0	–	ns	
Chip Disable to Output in High-Z	t_{EHQZ}	t_{CHZ}	0	25	0	30	ns	1, 3
$\overline{G}$ Disable to Output in High-Z	t_{GHQZ}	t_{OHZ}	0	25	0	30	ns	3
Write Enable to Output in High-Z	t_{WLQZ}	t_{WHZ}	0	25	0	30	ns	3
$\overline{G}$ Output Disable Set-Up Time	t_{GHEL}	t_{ODS}	0	–	0	–	ns	1
$\overline{G}$ Output Disable Hold Time	t_{EHGL}	t_{ODH}	10	–	10	–	ns	1
Read Command Set-Up Time	t_{WHEL}	t_{RCS}	0	–	0	–	ns	1
Read Command Hold Time	t_{EHWL}	t_{RCH}	0	–	0	–	ns	1
Write Pulse Width	t_{WLWH}	t_{WP}	60	–	70	–	ns	
Write Command Hold Time	t_{ELWH}	t_{WCH}	60	10,000	70	10,000	ns	1
Write Command to CE Lead Time	t_{WLEH}	t_{CWL}	60	10,000	70	10,000	ns	

NOTES: (Continued)

1. Chip is Enabled only when $\overline{E1}$ is set low and E2 is set high.



The start of a memory cycle is determined by the latter of $\overline{E1}$ going low or E2 going high ($\overline{E}$ going low), and the end of the memory cycle is determined by the earlier of $\overline{E1}$ going high or E2 going low ($\overline{E}$ going high). The PSRAM is a synchronous RAM, and therefore a memory access cycle will always be started at the falling edge of $\overline{E}$. The PSRAM will go into the standby mode when $\overline{E}$ is held high.

2. The timings, t_{CE} (min) and t_{CE} (max), must be kept for proper device operation as follows.

3. t_{CHZ}, t_{OHZ}, t_{WHZ} define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

5

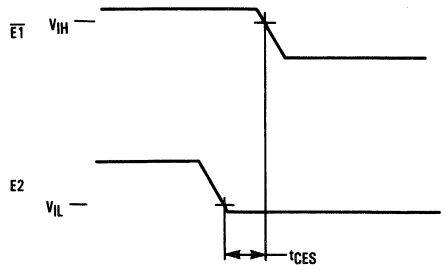
READ, WRITE, AND READ-MODIFY-WRITE CYCLES

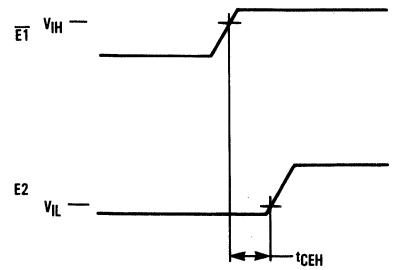
(An initial pause of 100 μs with high $\overline{E1}$ or low E2 is required after power-up, before proper device operation is achieved.)

Parameter	Symbol		MCM51L8128-80 MCM51LV8128-80		MCM518128-10 MCM51L8128-10 MCM51LV8128-10		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Data Set-Up Time from $\overline{W}$	t_{DVWH}	t_{DSW}	30	–	35	–	ns	4
Data Set-Up Time from CE	t_{DVEH}	t_{DSC}	30	–	35	–	ns	1, 4
Data Hold Time from $\overline{W}$	t_{WHDX}	t_{DHW}	0	–	0	–	ns	4
Data Hold Time from CE	t_{EHDX}	t_{DHC}	0	–	0	–	ns	1, 4
Address Set-Up Time	t_{AVEL}	t_{ASC}	0	–	0	–	ns	1, 5
Address Hold Time	t_{ELAX}	t_{AHC}	20	–	25	–	ns	5
Auto Refresh Cycle Time	t_{FVFV}	t_{FC}	130	–	160	–	ns	
$\overline{F}$ Delay Time from CE	t_{EHFL}	t_{RFD}	40	–	50	–	ns	1
$\overline{F}$ Pulse Width (Auto Refresh)	t_{FLFH}	t_{FAP}	30	8,000	30	8,000	ns	6
$\overline{F}$ Precharge Time	t_{FHFL}	t_{FP}	30	–	30	–	ns	6
$\overline{F}$ Command Hold Time	t_{ELFL}	t_{RHC}	15	–	15	–	ns	1
$\overline{F}$ Pulse Width (Self Refresh)	t_{FLFH}	t_{FAS}	8,000	–	8,000	–	ns	6
CE Delay Time from $\overline{F}$ (Self Refresh)	t_{FHEL}	t_{FRS}	160	–	190	–	ns	1, 6
Refresh Period (512 Cycle A0 to A8)	t_{RF}	t_{REF}	–	8	–	8	ms	
E2 Low Set-Up Time	t_{E2LE1L}	t_{CES}	5	–	5	–	ns	1, 7
E2 Low Hold Time	t_{E1HE2H}	t_{CEH}	5	–	5	–	ns	1, 7
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	ns	

NOTES:

4. In write cycle, the input data is latched at the earlier of $\overline{W}$ or $\overline{E1}$ rising edge and E2 falling edge. Therefore the input data must be valid during set-up time (t_{DSW} or t_{DSC}) and hold time (t_{DHW} or t_{DHC}).
5. All address inputs are latched at the falling edge of $\overline{E1}$ and the rising edge of E2. Therefore all the address inputs must be valid during t_{ASC} and t_{AHC}.
6. Two refresh operations—auto refresh and self refresh are defined by the $\overline{F}$ pulse width under the condition of $\overline{E1} = V_{IH}$ or $E2 = V_{IL}$:
   Auto refresh: $\overline{F}$ pulse width $\leq t_{FAP}$ (max).
   Self refresh: $\overline{F}$ pulse width $\geq t_{FAS}$ (min).
   The timing parameter (t_{FRS}) must be kept for proper device operation in the following conditions:
   a. After self refresh.
   b. In case $\overline{F} = V_{IL}$ after power-up.
7. When switching disable controls, the timings t_{CES} and t_{CEH} must be kept for proper device operation as follows:

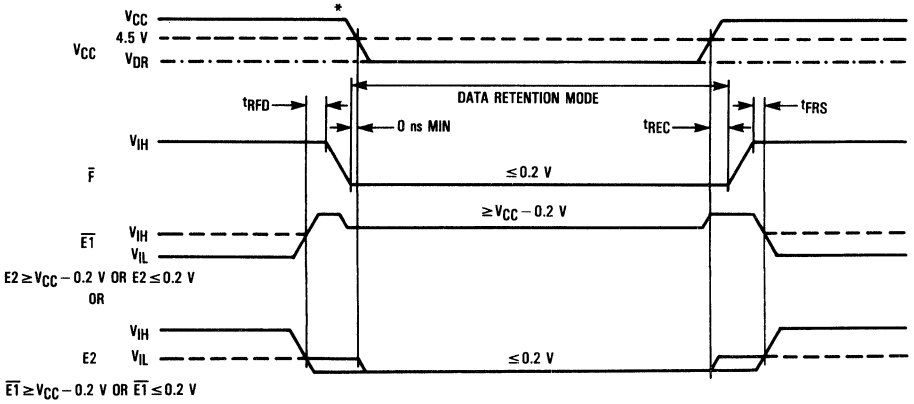




DATA RETENTION CHARACTERISTICS (T_A = 0 ~ 70°C) (MCM51LV8128 Only)

Symbol	Parameter		Min	Typ	Max	Unit
V_{DR}	Data Retention Supply Voltage		3.0	–	5.5	V
I_{CCF2}	Self Refresh Current	V_{DR} = 3.0 V	–	40	100	μA
	(Average Current)	V_{DR} = 5.5 V	–	100	200	
t_{rec}	Recovery Time		5	–	–	ms

*The falling slope of V_{CC} must be more than 50 ms in order to operate the device safely. (20 ms/V)

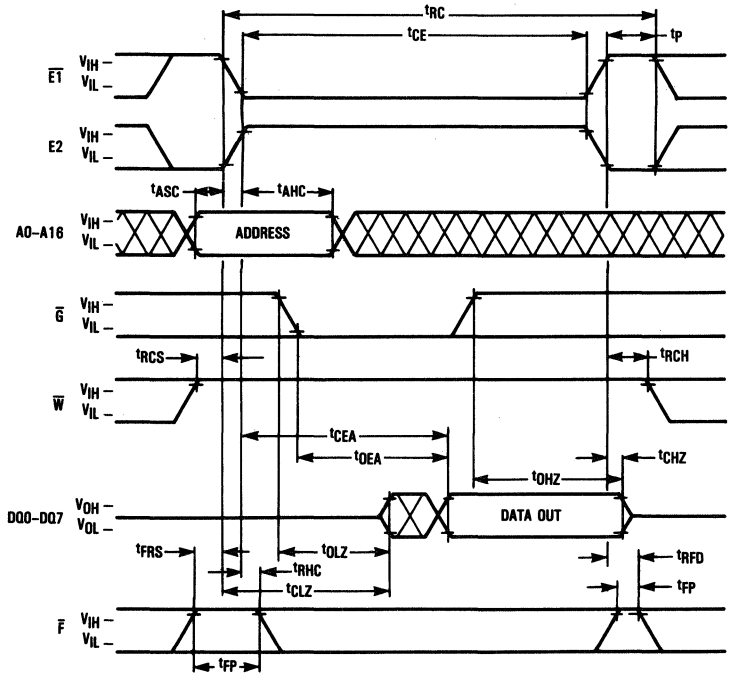


NOTES:
1. $\overline{G}$, $\overline{W}$, A0-A16 = Don't Care.
2. I_{CCF1} is applied in $\overline{F} = V_{IL}$ max, $\overline{E1} = V_{IH}$ min, $E2 = V_{IL}$ max.
3. Data Retention is a special case of the Self Refresh mode. All modes other than the Self Refresh mode require Auto Refresh or CE Only Refresh with 512 cycles/8 ms.
4. Enter the Self Refresh mode before dropping V_{CC} below 4.5 V for Data Retention mode.

The Motorola MCM51LV8128 pseudo static RAM has data retention capability at a V_{CC} level as low as three volts. This is particularly useful with battery backup applications. While in the data retention mode the pseudo static RAM will draw no more than 100 microamps of current at 3 V V_{CC} in the temperature range from 0°C to 70°C. The data retention mode of the pseudo static RAM is basically a self refresh mode where each row in the memory array is automatically refreshed at periodic intervals by on-chip refresh control circuitry. The pseudo static RAM will enter self refresh mode eight microseconds after the refresh pin makes a transition from high to low while the device is in standby mode. Under these conditions the device will remain in self refresh mode until either brought out of standby mode or until the refresh pin is clocked high.

5

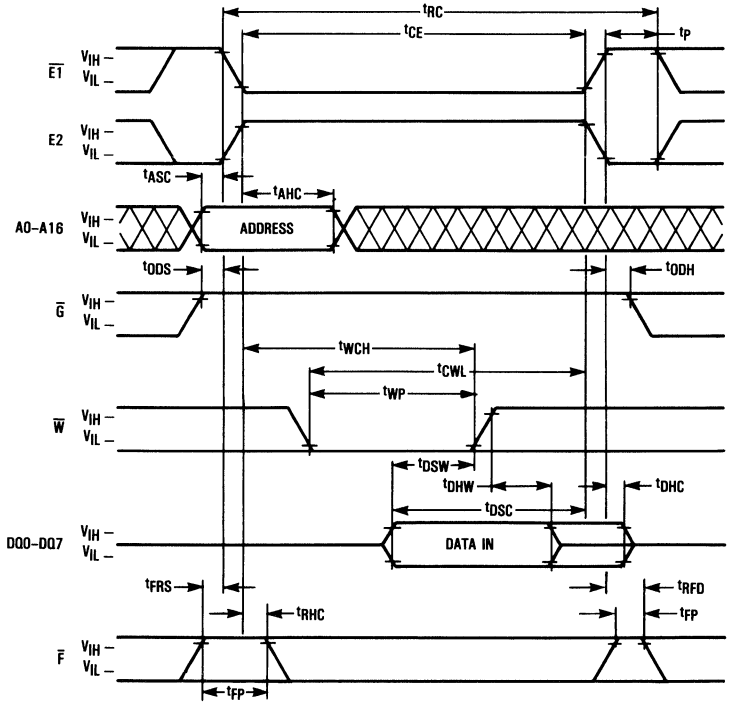
READ CYCLE



NOTE: The device can be operated with clocking "$\overline{E1}$" (or E2) pin only provided that "E2" (or $\overline{E1}$) is connected to V_{IH} (or V_{IL}) level.

A read cycle is initiated by $\overline{E}$ and $\overline{G}$ going low during the same cycle while the $\overline{W}$ signal is held high. Valid data will be output after a delay of t_{CEA} from the falling edge of $\overline{E}$ and a delay of t_{OEA} from the falling edge of $\overline{G}$. The data will remain valid on the outputs for the time t_{OHZ} from the rising edge of $\overline{G}$ and t_{CHZ} from the rising edge of $\overline{E}$. All address inputs are latched at the falling edge of $\overline{E}$, therefore, all the address inputs must be valid during address setup and address hold times t_{ASC} and t_{AHC}.

WRITE CYCLE 1
($\overline{G}$ Fixed High)

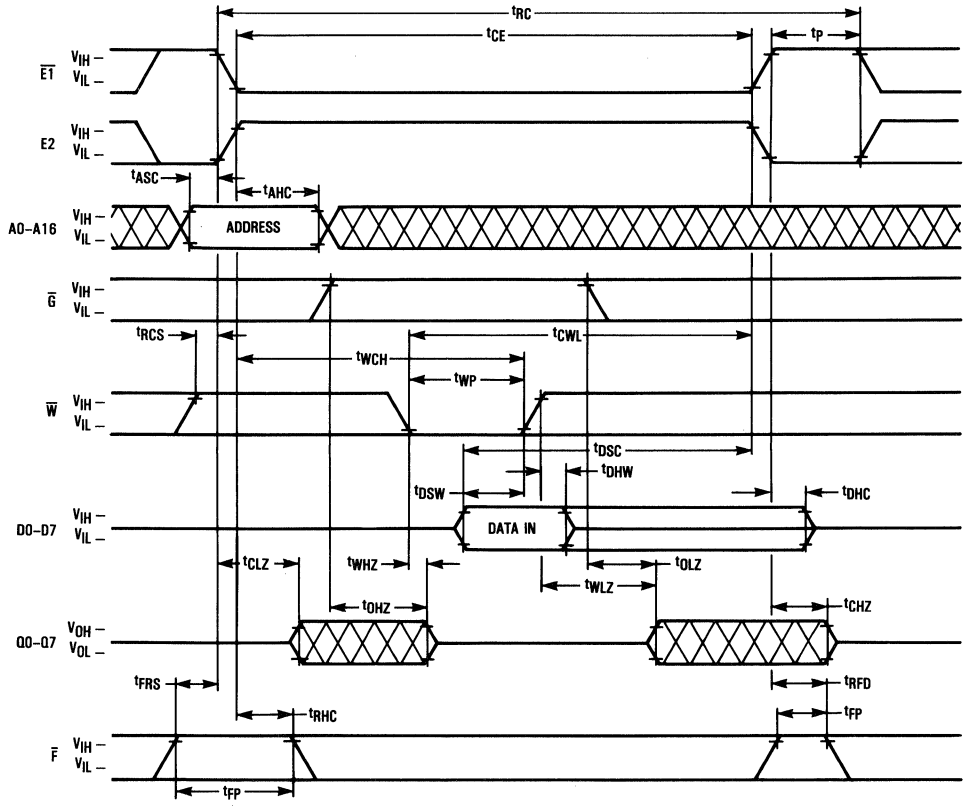


NOTE: The device can be operated with clocking "$\overline{E1}$" (or E2) pin only provided that "E2" (or $\overline{E1}$) is connected to V_{IH} (or V_{IL}) level.

A write cycle is initiated when both $\overline{E}$ and $\overline{W}$ go low during the same cycle. The write operation is terminated with the input data being latched at the rising edge of either $\overline{E}$ or $\overline{W}$, whichever occurs first. Therefore, the input data must be valid during data setup and data hold times t_{DSW}/t_{DSC} and t_{DHW}/t_{DHC}.

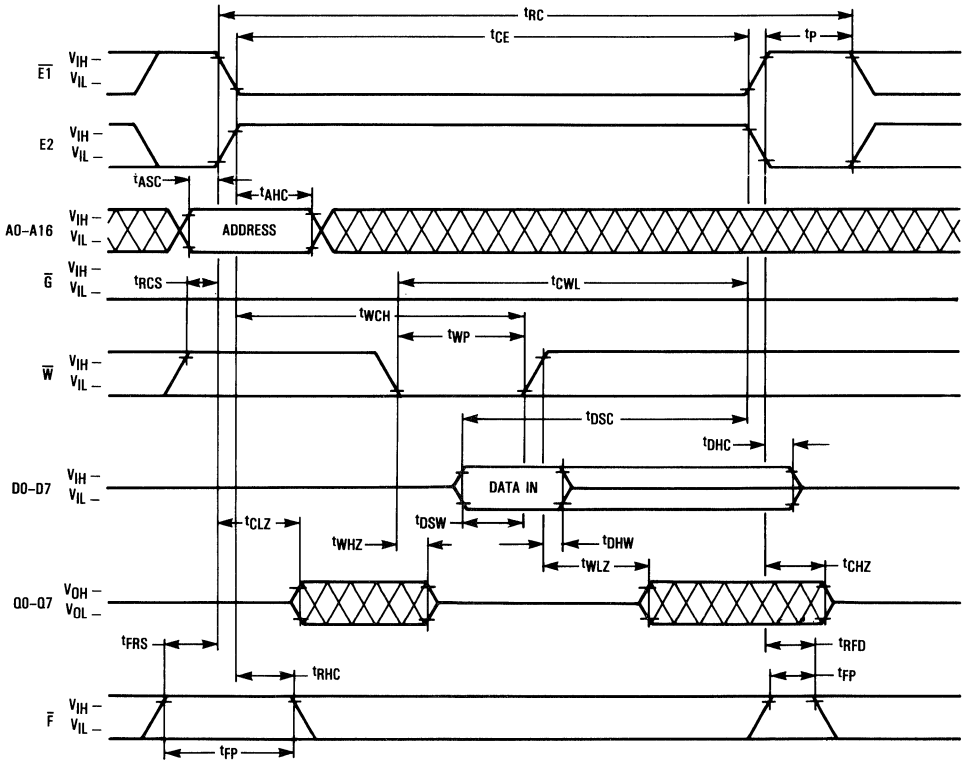
5

WRITE CYCLE 2
($\overline{G}$ Clock)



NOTE: The device can be operated with clocking "$\overline{E1}$" (or E2) pin only provided that "E2" (or $\overline{E1}$) is connected to V_{IH} (or V_{IL}) level.

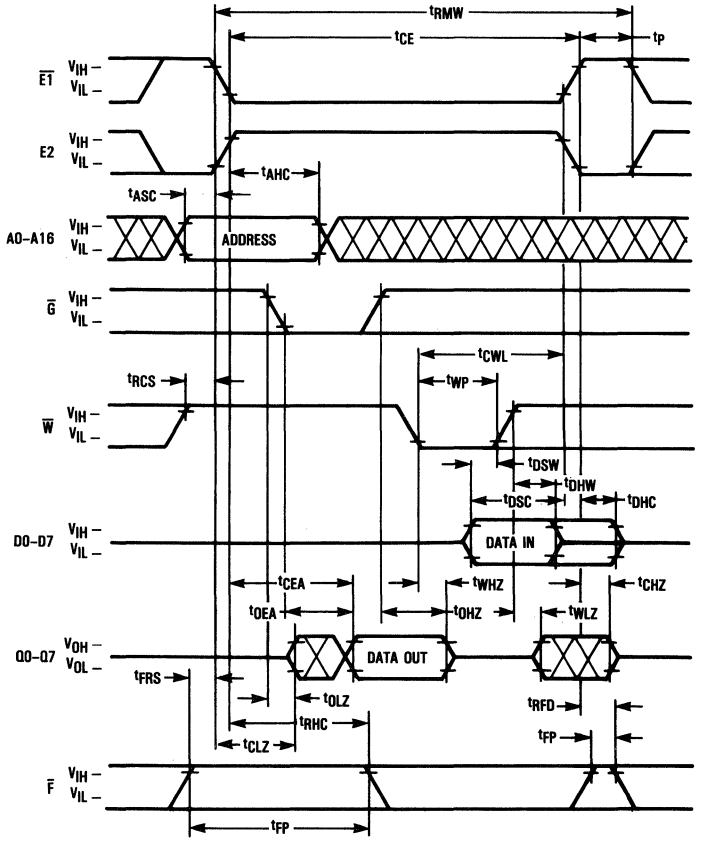
WRITE CYCLE 3
($\overline{G}$ Fixed Low)



NOTE: The device can be operated with clocking "$\overline{E1}$" (or E2) pin only provided that "E2" (or $\overline{E1}$) is connected to V_{IH} (or V_{IL}) level.

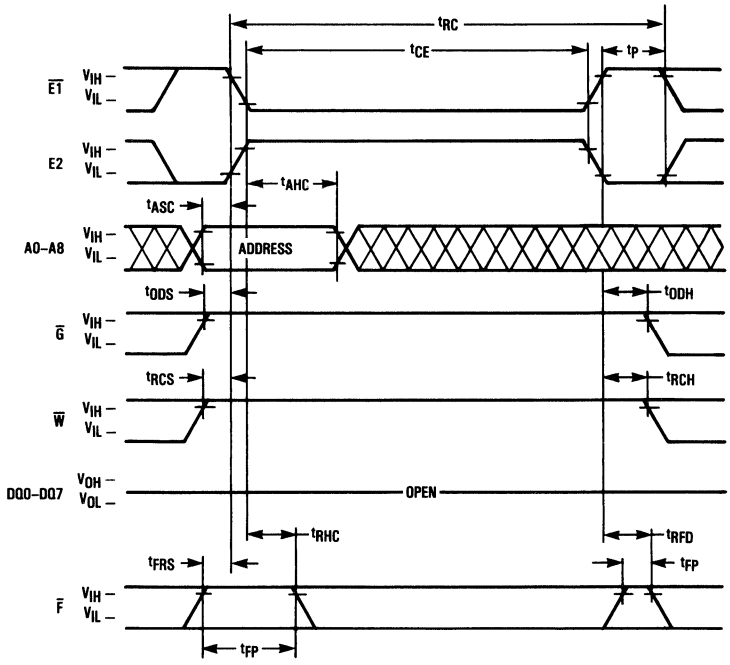
5

READ MODIFY WRITE CYCLE



NOTE: The device can be operated with clocking "$\overline{E1}$" (or E2) pin only provided that "E2" (or $\overline{E1}$) is connected to V_{IH} (or V_{IL}) level.

CHIP ENABLE ONLY REFRESH
(A9-A16 = Don't Care)

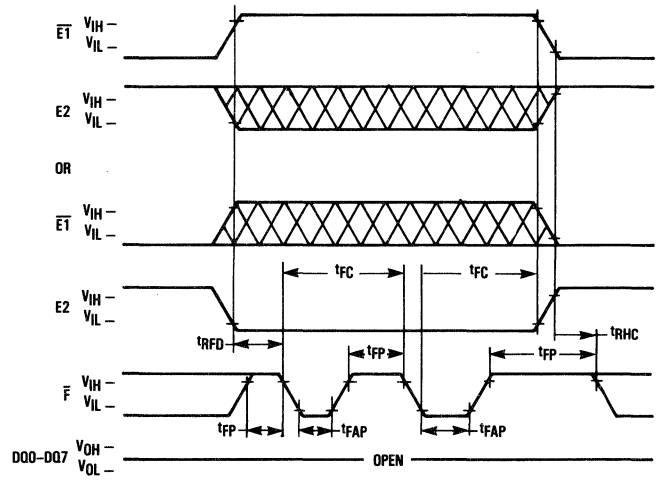


NOTE: The device can be operated with clocking "$\overline{E1}$" (or E2) pin only provided that "E2" (or $\overline{E1}$) is connected to V_{IH} (or V_{IL}) level.

The chip enable only refresh is similar to the $\overline{RAS}$-only refresh of a DRAM. This type of refresh is accomplished by performing a memory cycle at each of the 512 rows (defined by A0-A8) within the specified refresh period.

5

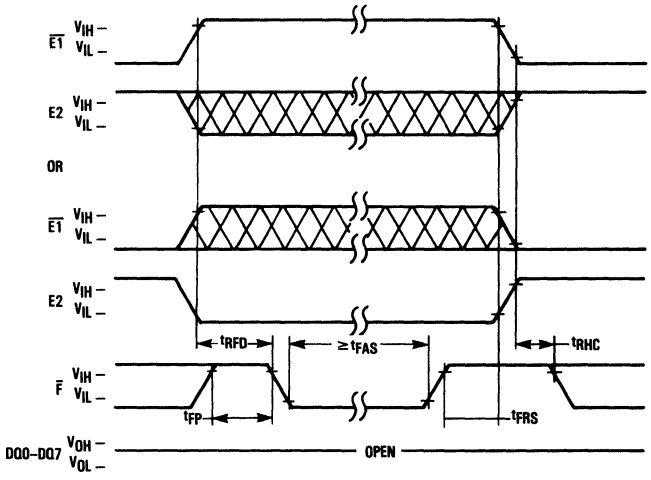
AUTO REFRESH
($\overline{G}$, $\overline{W}$, A0-A16 = Don't Care)



NOTE: During an auto refresh, an internal row address counter is incremented at the falling edge of $\overline{F}$, and a new row is refreshed. This diagram shows $\overline{F}$ toggling twice, thus refreshing 2 rows.

The auto refresh is similar to the $\overline{CAS}$-before-$\overline{RAS}$ refresh of a DRAM. When the $\overline{F}$ signal is clocked while $\overline{E}$ is high, the internal refresh counter and on-chip refresh circuitry are enabled and an internal refresh operation takes place. Each time the $\overline{F}$ signal is clocked (as specified and with $\overline{E}$ high), a subsequent row is refreshed and the internal refresh address counter is automatically incremented in preparation for the next auto refresh cycle. Note that the auto refresh $\overline{F}$ pulse width (t_{FAP}) must be more than 30 ns and less than 8 μs for this type of refresh operation to properly take place.

SELF REFRESH
($\overline{G}$, $\overline{W}$, A0-A16 = Don't Care)



NOTE: In the self refresh mode, after $\overline{F}$ has been held low for t_{FAS}, an internal timer will refresh a new row approximately every 150 μs. Due to the long period of this method of refresh, it is recommended that self refresh only be used for extremely long standby periods, such as a battery backup operation.

The self refresh is similar to the auto refresh and is recommended for use during the periods when the PSRAM is in the standby mode for an extended amount of time. For this type of refresh the $\overline{F}$ signal is held low for as long as the device is deselected. When the self refresh $\overline{F}$ pulse width (t_{FAS}) exceeds 8 μs, a timer activates an internal refresh operation at consecutive internal refresh address counter locations. Note that upon completion of the self refresh cycle the timing parameter t_{FRS} (chip enable delay time from $\overline{F}$ self refresh) must be followed for proper device operation during the following cycle.

ORDERING INFORMATION
(Order by Full Part Number)

MCM | 518128 or 51L8128 or 51LV8128 | XX | XX

- MCM — Motorola Memory Prefix
- 518128 or 51L8128 or 51LV8128 — Part Number (With L = Low Power Version, with LV = Low Power with Data Retention Version)
- XX — Package (P = 600 mil Plastic DIP, SF = 330 mil SOG)
- XX — Speed (80 = 80 ns, 10 = 100 ns)

Full Part Numbers—

MCM518128P10	MCM518128SF10
MCM51L8128P80	MCM51L8128SF80
MCM51L8128P10	MCM51L8128SF10
MCM51LV8128P80	MCM51LV8128SF80
MCM51LV8128P10	MCM51LV8128SF10

MCM518129
MCM51L8129
MCM51LV8129

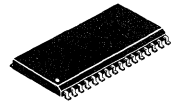
128K x 8 Bit CMOS Pseudo Static Random Access Memory

The MCM518129 is a 1,048,576 bit low-power pseudo-static random access memory organized as 131,072 words of 8 bits, fabricated using 1.0 μm silicon-gate advanced CMOS process technology. The MCM518129 family products utilize one-transistor dynamic storage cells and direct static addresses to achieve high density and fast access time. The advanced CMOS circuit design reduces power consumption and provides greater reliability. The data retention mode allows for very low power with battery backup in lap-top applications.

The refresh input ($\overline{F}$) allows two types of refresh application—auto refresh and self refresh. The MCM518129 is pin compatible with the 128K x 8 SRAM JEDEC pinout and offers a low cost alternative to 1M SRAMs and a simpler design for DRAM memory applications.

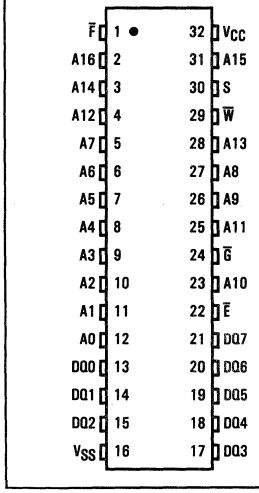
The MCM518129 is available in a wide 32 lead plastic small outline package.

- Single 5 V Supply ±10%
- 128K x 8 Bit Memory Organization
- Low Power Dissipation—385 mW (Maximum Active)
- TTL Compatible Inputs and Outputs
- Battery Backup Capability from 4.5 V to 5.5 V (3.0 V to 5.5 V with MCM51LV8129)
- Chip Select Standby Mode
- Low Standby Current 200 μA (Maximum) with MCM51L8129 and MCM51LV8129
- Auto Refresh Power Down Function
- 512 Refresh Cycles/8 ms
- Auto Refresh is Executed by Internal Counter
- Self Refresh is Executed by Internal Timer
- Pin Compatible with 1M SRAM JEDEC Pinout
- Three State Outputs
- Fast Access Times: MCM51L8129-80/MCM51LV8129-80 = 80 ns (Max)
  MCM518129-10/MCM51L8129-10/MCM51LV8129-10 = 100 ns (Max)



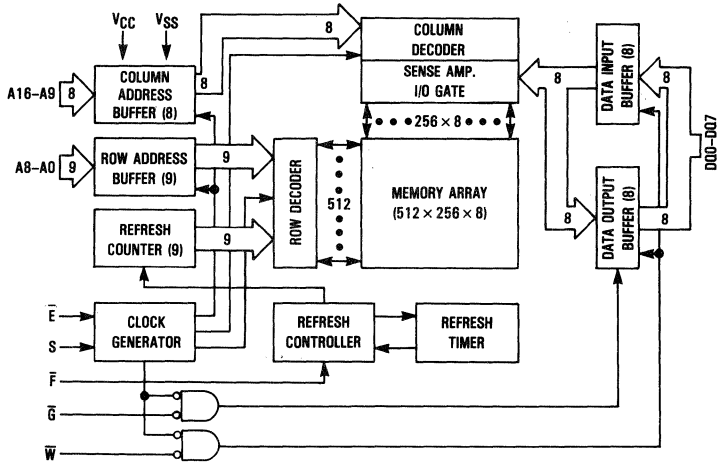
F PACKAGE
450 MIL SOG
CASE 855

PIN ASSIGNMENT



PIN NAMES

A0-A16	Address Input
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
S	Chip Select
$\overline{G}$	Output Enable
$\overline{F}$	Refresh Input
DQ0-DQ7	Data Input/Output
V_{CC}	Power Supply
V_{SS}	Ground



TRUTH TABLE

$\overline{E}$	S at $\overline{E}$ Going Low	$\overline{G}$	$\overline{W}$	$\overline{F}$	Mode	I/O Pin
L	H	L	H	H/L	Read*	D_{out}
L	H	X	L	H/L	Write*	D_{in}
L	H	H*	H*	H/L	CE Only Refresh	High Z
H	X	X	X	⊓⊔⊓	Auto Refresh	High Z
H	X	X	X	L	Self Refresh	High Z
L	L	X	X	H/L	Chip Select Standby	High Z
H	X	X	X	H	Standby	High Z

L = V_{IL} H = V_{IH} X = don't care ⊓⊔⊓ = Toggle
H/L = V_{IH} or V_{IL}, but must not toggle.
*The Read and Write operations effectively perform a CE Only Refresh of the row being addressed.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

5

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−1.0 to 7.0	V
Voltage to Any Pin with Respect to V_{SS}	V_{in}, V_{out}	−1.0 to 7.0	V
Power Dissipation	P_D	600	mW
Soldering Temperature•Time	T_{solder}	260•10	°C•s
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +150	°C
Short Circuit Output Current	I_{out}	50	mA

NOTE:
Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.4	–	6.5	V
Input Low Voltage	V_{IL}	−1.0	–	0.8	V

NOTE: All voltages are referenced to GND.

DC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	−10.0	–	10.0	μA
Output Leakage Current ($\overline{E}$ = V_{IH}, $\overline{G}$ = V_{IH} or $\overline{W}$ = V_{IL}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	−10.0	–	10.0	μA
Operating Current ($\overline{E}$ = V_{IL}, Address Cycling, t_{RC} = t_{RC} min) t_{RC} = 130 ns t_{RC} = 160 ns	I_{CCA}*	– –	50 40	70 60	mA
Standby Current ($\overline{E}$ = V_{IH}, $\overline{F}$ = V_{IH}) MCM518129 MCM51L8129/MCM51LV8129	I_{SB1}	– –	– –	2 1	mA
Standby Current ($\overline{E}$ ≥ V_{CC} − 0.2 V, $\overline{F}$ ≥ V_{CC} − 0.2 V) MCM518129 MCM51L8129/MCM51LV8129	I_{SB2}**	– –	– 100	1 200	mA μA
Self Refresh Current ($\overline{E}$ = V_{IH}, $\overline{F}$ = V_{IL}) MCM518129 (Average Current) MCM51L8129/MCM51LV8129	I_{CCF1}	– –	– –	2 1	mA
Self Refresh Current ($\overline{E}$ ≥ V_{CC} − 0.2 V, $\overline{F}$ ≤ 0.2 V) MCM518129 (Average Current) MCM51L8129/MCM51LV8129	I_{CCF2}**	– –	– 100	1 200	mA μA
Auto Refresh Current (Average Current) ($\overline{F}$ Toggling, t_{FC} = t_{FC} min)	I_{CCF3}	–	–	2	mA
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	–	–	0.4	V
Output High Voltage (I_{OH} = −5.0 mA)	V_{OH}	2.4	–	–	V

*I_{CCA} depends on cycle rate and output loading. Specified values are obtained with the output open.
**In the Standby mode with $\overline{E}$ ≥ V_{CC} − 0.2 V, these limits are guaranteed when $\overline{F}$ ≥ V_{CC} − 0.2 V. In the Self Refresh mode with $\overline{E}$ ≥ V_{CC} − 0.2 V, these limits are guaranteed when $\overline{F}$ ≤ 0.2 V. In the Chip Select Standby mode, these limits are guaranteed when $\overline{E}$ ≤ 0.2 V, S ≤ 0.2 V (when $\overline{E}$ goes low), and $\overline{F}$ ≥ V_{CC} − 0.2 V or $\overline{F}$ ≤ 0.2 V.

CAPACITANCE (f = 1 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Min	Max	Unit
Input Capacitance	A0–A16	C_{in}	–	5	pF
	$\overline{E}$, S, $\overline{G}$, $\overline{W}$, $\overline{F}$		–	7	
Output Capacitance	DQ0–DQ7	C_{out}	–	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

Input Pulse Levels . . . . . 0.6 V, 2.6 V
Input Rise/Fall Time . . . . . 5 ns
Input Timing Measurement Reference Levels . . . . . .0.8 and 2.4 V
Output Timing Measurement Reference Levels . . . . .0.8 and 2.2 V
Output Load . . . . . 2 TTL Loads and 100 pF

5

READ, WRITE, AND READ-MODIFY-WRITE CYCLES

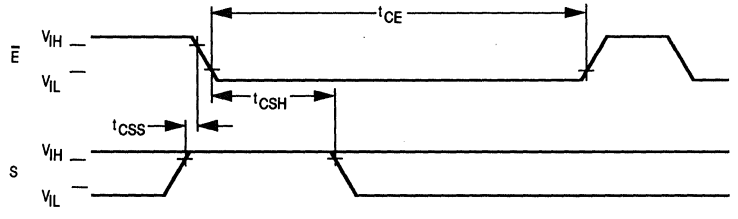
(An initial pause of 100 μs with high $\overline{E}$ is required after power-up, before proper device operation is achieved.)

Parameter	Symbol		MCM51L8129-80 MCM51LV8129-80		MCM518129-10 MCM51L8129-10 MCM51LV8129-10		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Random Read, Write Cycle Time	$t_{EVEV(R)}$	t_{RC}	130	–	160	–	ns	1
Read Modify Write Cycle Time	$t_{EVEV(RW)}$	t_{RMW}	195	–	235	–	ns	1
Chip Enable Pulse Width	t_{ELEH}	t_{CE}	80	10,000	100	10,000	ns	1
Chip Enable Precharge Time	t_{EHEL}	t_P	40	–	50	–	ns	1
Chip Enable Access Time	t_{ELQV}	t_{CEA}	–	80	–	100	ns	1
Output Enable Access Time	t_{GLQV}	t_{OEA}	–	35	–	40	ns	
Chip Enable to Output in Low-Z	t_{ELQX}	t_{CLZ}	30	–	30	–	ns	1
Output Enable to Output in Low-Z	t_{GLQX}	t_{OLZ}	0	–	0	–	ns	
Output Active from End of Write	t_{WHQX}	t_{WLZ}	0	–	0	–	ns	
Chip Disable to Output in High-Z	t_{EHQZ}	t_{CHZ}	0	25	0	30	ns	2
$\overline{G}$ Disable to Output in High-Z	t_{GHQZ}	t_{OHZ}	0	25	0	30	ns	2
Write Enable to Output in High-Z	t_{WLQZ}	t_{WHZ}	0	25	0	30	ns	2
$\overline{G}$ Output Disable Set-Up Time	t_{GHEL}	t_{ODS}	0	–	0	–	ns	1
$\overline{G}$ Output Disable Hold Time	t_{EHGL}	t_{ODH}	10	–	10	–	ns	1
Read Command Set-Up Time	t_{WHEL}	t_{RCS}	0	–	0	–	ns	1
Read Command Hold Time	t_{EHWL}	t_{RCH}	0	–	0	–	ns	1
Chip Select Set-Up Time	t_{SHEL}	t_{CSS}	0	–	0	–	ns	1
Chip Select Hold Time	t_{ELSL}	t_{CSH}	20	–	25	–	ns	1
Write Pulse Width	t_{WLWH}	t_{WP}	60	–	70	–	ns	
Write Command Hold Time	t_{ELWH}	t_{WCH}	60	10,000	70	10,000	ns	1
Write Command to CE Lead Time	t_{WLEH}	t_{CWL}	60	10,000	70	10,000	ns	

(Continued)

NOTES:

1. The timings, t_{CE} (min) and t_{CE} (max), must be kept for proper device operation as follows:



The start of a memory cycle is determined by $\overline{E}$ going low while S is high, and the end of the memory cycle is determined by $\overline{E}$ going high. The PSRAM will go into the standby mode when $\overline{E}$ is held high.

2. t_{CHZ}, t_{OHZ}, t_{WHZ} define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

READ, WRITE, AND READ-MODIFY-WRITE CYCLES

(An initial pause of 100 μs with high $\overline{E}$ is required after power-up, before proper device operation is achieved.)

Parameter	Symbol		MCM51L8129-80 MCM51LV8129-80		MCM518129-10 MCM51L8129-10 MCM51LV8129-10		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Data Set-Up Time from $\overline{W}$	t_{DVWH}	t_{DSW}	30	–	35	–	ns	3
Data Set-Up Time from CE	t_{DVEH}	t_{DSC}	30	–	35	–	ns	3
Data Hold Time from $\overline{W}$	t_{WHDX}	t_{DHW}	0	–	0	–	ns	3
Data Hold Time from CE	t_{EHDX}	t_{DHC}	0	–	0	–	ns	3
Address Set-Up Time	t_{AVEL}	t_{ASC}	0	–	0	–	ns	4
Address Hold Time	t_{ELAX}	t_{AHC}	20	–	25	–	ns	4
Auto Refresh Cycle Time	t_{FVFV}	t_{FC}	130	–	160	–	ns	
$\overline{F}$ Delay Time from CE	t_{EHFL}	t_{RFD}	40	–	50	–	ns	1
$\overline{F}$ Pulse Width (Auto Refresh)	t_{FLFH}	t_{FAP}	30	8,000	30	8,000	ns	5
$\overline{F}$ Precharge Time	t_{FHFL}	t_{FP}	30	–	30	–	ns	5
$\overline{F}$ Command Hold Time	t_{ELFL}	t_{RHC}	15	–	15	–	ns	1
$\overline{F}$ Pulse Width (Self Refresh)	t_{FLFH}	t_{FAS}	8,000	–	8,000	–	ns	5
CE Delay Time from $\overline{F}$ (Self Refresh)	t_{FHEL}	t_{FRS}	160	–	190	–	ns	1, 5
Refresh Period (512 Cycle A0 to A8)	t_{RF}	t_{REF}	–	8	–	8	ms	
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	ns	

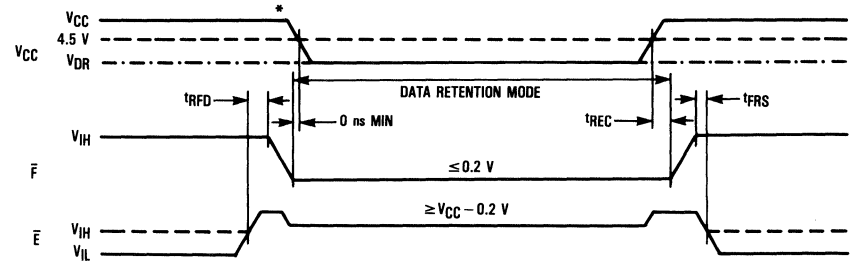
NOTES:

3. In write cycle, the input data is latched at the earlier of $\overline{W}$ or $\overline{E}$ rising edge. Therefore the input data must be valid during set-up time (t_{DSW} or t_{DSC}) and hold time (t_{DHW} or t_{DHC}).
4. All address inputs are latched at the falling edge of $\overline{E}$. Therefore all the address inputs must be valid during t_{ASC} and t_{AHC}.
5. Two refresh operations—auto refresh and self refresh are defined by the $\overline{F}$ pulse width under the condition of $\overline{E} = V_{IH}$:
   Auto refresh: $\overline{F}$ pulse width $\leq t_{FAP}$ (max).
   Self refresh: $\overline{F}$ pulse width $\geq t_{FAS}$ (min).
   The timing parameter (t_{FRS}) must be kept for proper device operation in the following conditions:
   a. After self refresh.
   b. In case $\overline{F} = V_{IL}$ after power-up.

DATA RETENTION CHARACTERISTICS (T_A = 0 ~ 70°C) (MCM51LV8129 Only)

Symbol	Parameter		Min	Typ	Max	Unit
V_{DR}	Data Retention Supply Voltage		3.0	–	5.5	V
I_{CCF2}	Self Refresh Current	V_{DR} = 3.0 V	–	40	100	μA
	(Average Current)	V_{DR} = 5.5 V	–	100	200	
t_{rec}	Recovery Time		5	–	–	ms

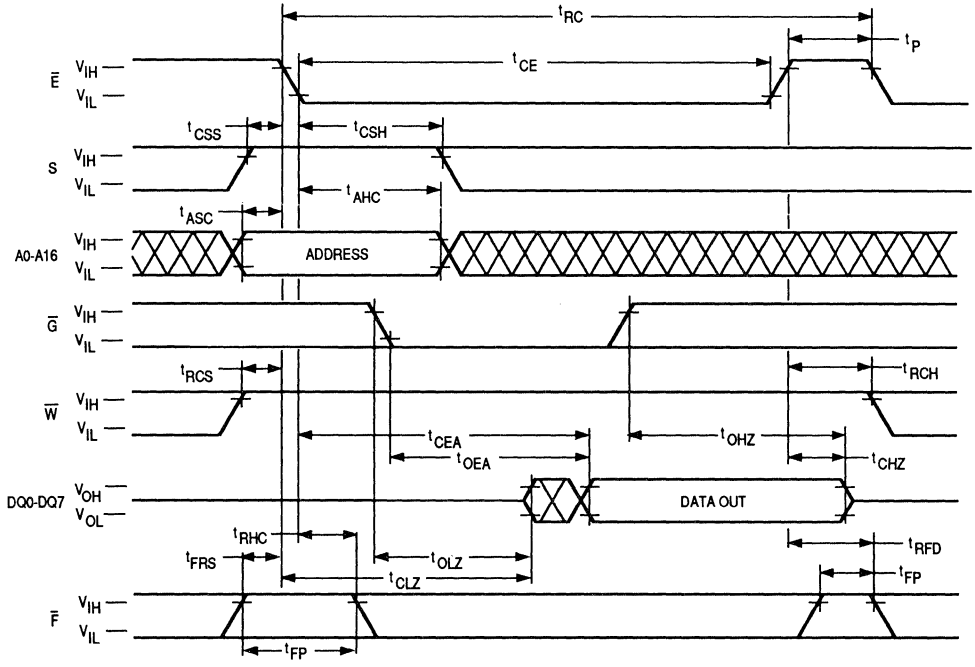
*The falling slope of V_{CC} must be more than 50 ms in order to operate the device safely. (20 ms/V)



NOTES:
*The falling slope of V_{CC} must be more than 50 ms in order to operate the device safely. (20 ms/V)
1. S, $\overline{G}$, $\overline{W}$, A0-A16 = Don't Care.
2. I_{CCF1} is applied in $\overline{F} = V_{IL}$ max, $\overline{E} = V_{IH}$ min.
3. Data Retention is a special case of the Self Refresh mode. All modes other than the Self Refresh mode require Auto Refresh or CE Only Refresh with 512 cycles/8 ms.
4. Enter the Self Refresh mode before dropping V_{CC} below 4.5 V for Data Retention mode.

The Motorola MCM51LV8129 pseudo static RAM has data retention capability at a V_{CC} level as low as three volts. This is particularly useful with battery backup applications. While in the data retention mode the pseudo static RAM will draw no more than 100 microamps of current at 3 V V_{CC} in the temperature range from 0°C to 70°C. The data retention mode of the pseudo static RAM is basically a self refresh mode where each row in the memory array is automatically refreshed at periodic intervals by on-chip refresh control circuitry. The pseudo static RAM will enter self refresh mode eight microseconds after the refresh pin makes a transition from high to low while the device is in standby mode. Under these conditions the device will remain in self refresh mode until either brought out of standby mode or until the refresh pin is clocked high.

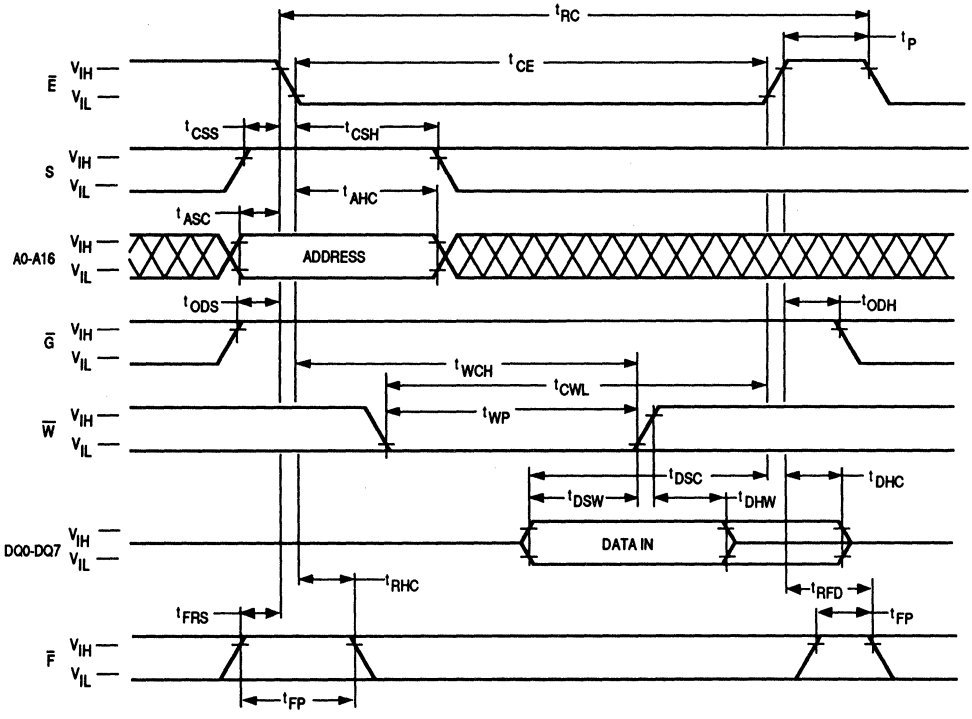
READ CYCLE



A read cycle is initiated by $\overline{E}$ and $\overline{G}$ going low during the same cycle while the $\overline{W}$ signal is held high. Valid data will be output after a delay of t_{CEA} from the falling edge of $\overline{E}$ and a delay of t_{OEA} from the falling edge of $\overline{G}$. The data will remain valid on the outputs for the time t_{OHZ} from the rising edge of $\overline{G}$ and t_{CHZ} from the rising edge of $\overline{E}$. All address inputs are latched at the falling edge of $\overline{E}$, therefore, all the address inputs must be valid during address setup and address hold times t_{ASC} and t_{AHC}.

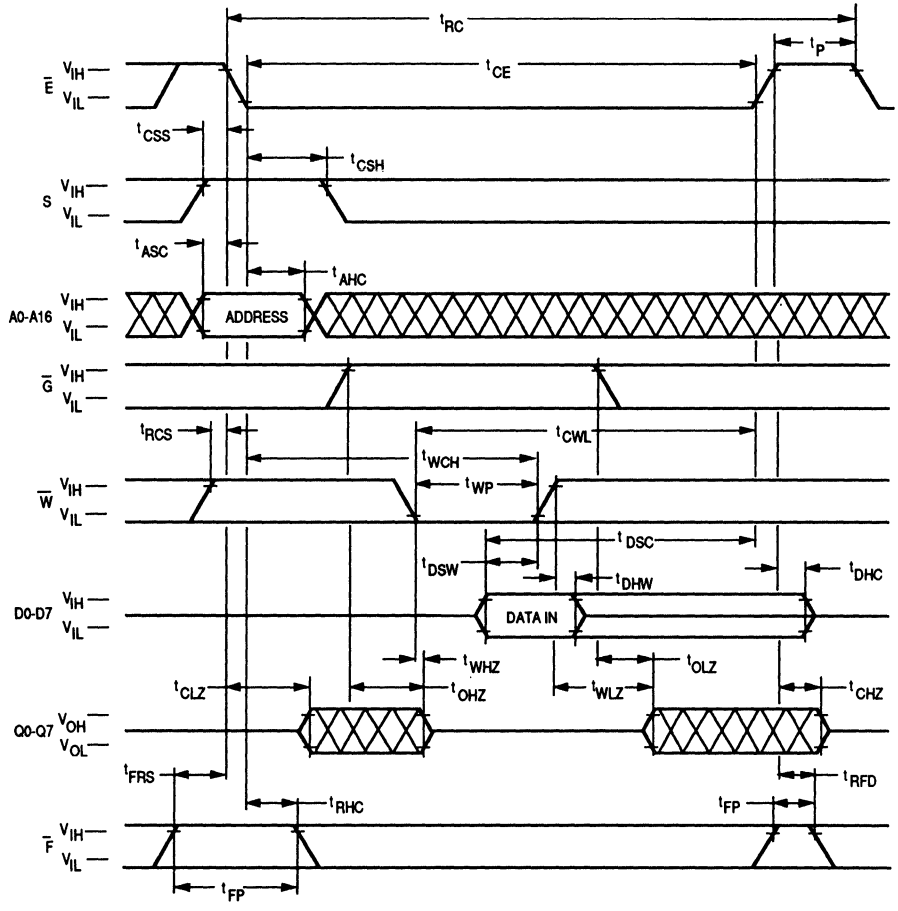
5

WRITE CYCLE 1
($\overline{G}$ Fixed High)



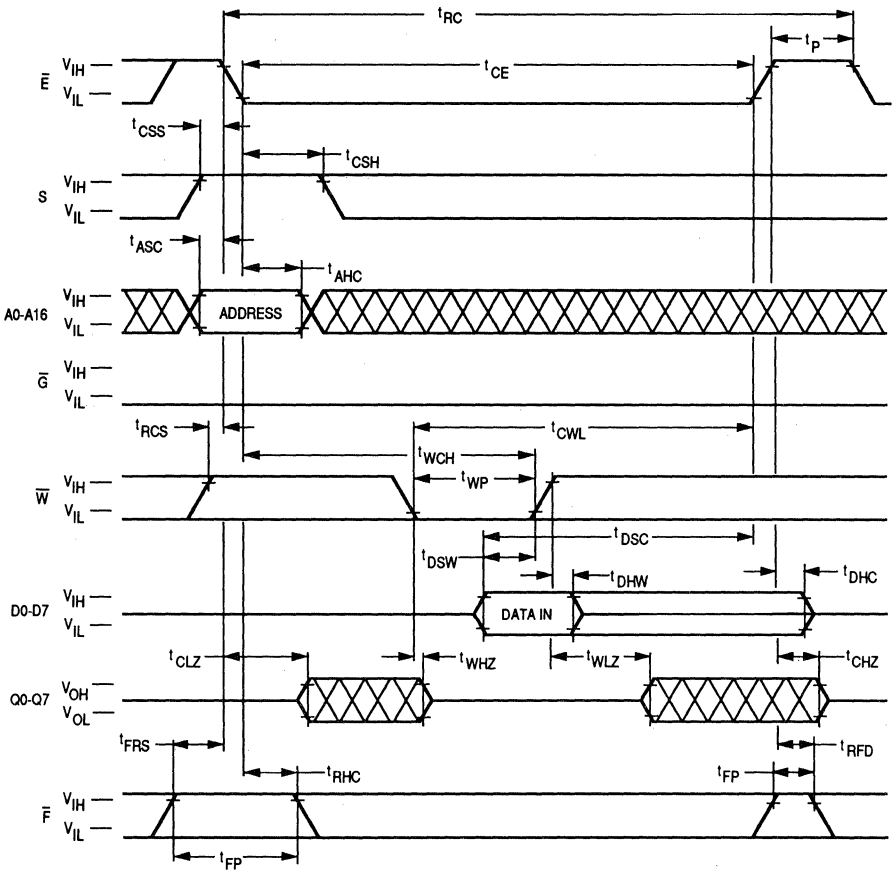
A write cycle is initiated when both $\overline{E}$ and $\overline{W}$ go low during the same cycle. The write operation is terminated with the input data being latched at the rising edge of either $\overline{E}$ or $\overline{W}$, whichever occurs first. Therefore, the input data must be valid during data setup and data hold times t_{DSW}/t_{DSC} and t_{DHW}/t_{DHC}.

WRITE CYCLE 2
($\overline{G}$ Clock)

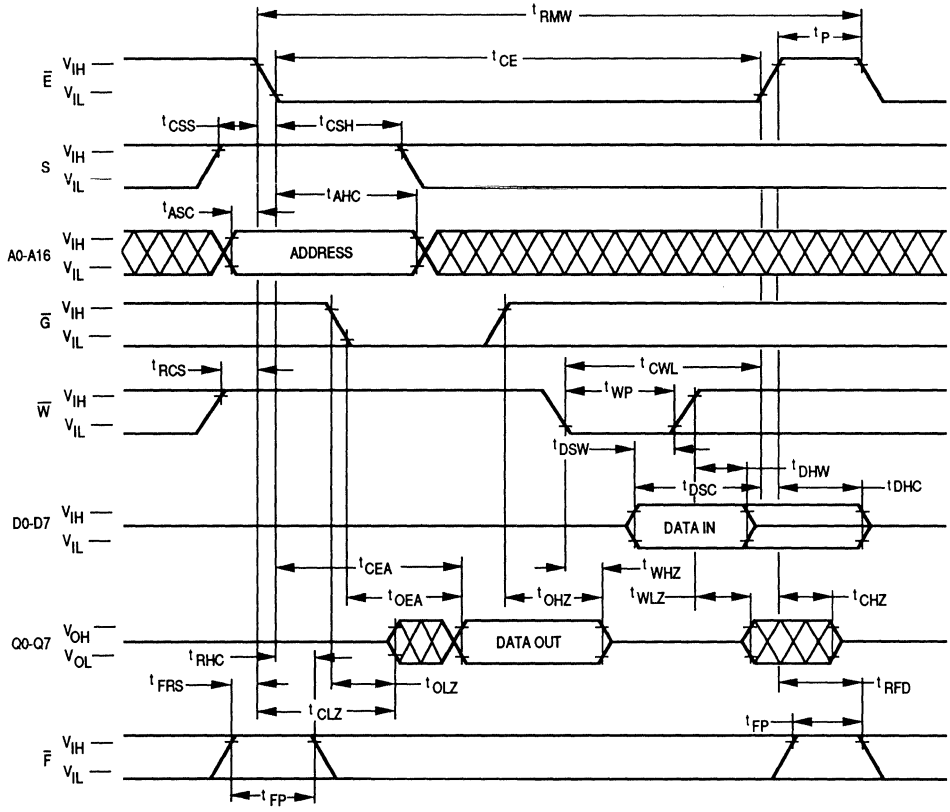


5

WRITE CYCLE 3
($\overline{G}$ Fixed Low)

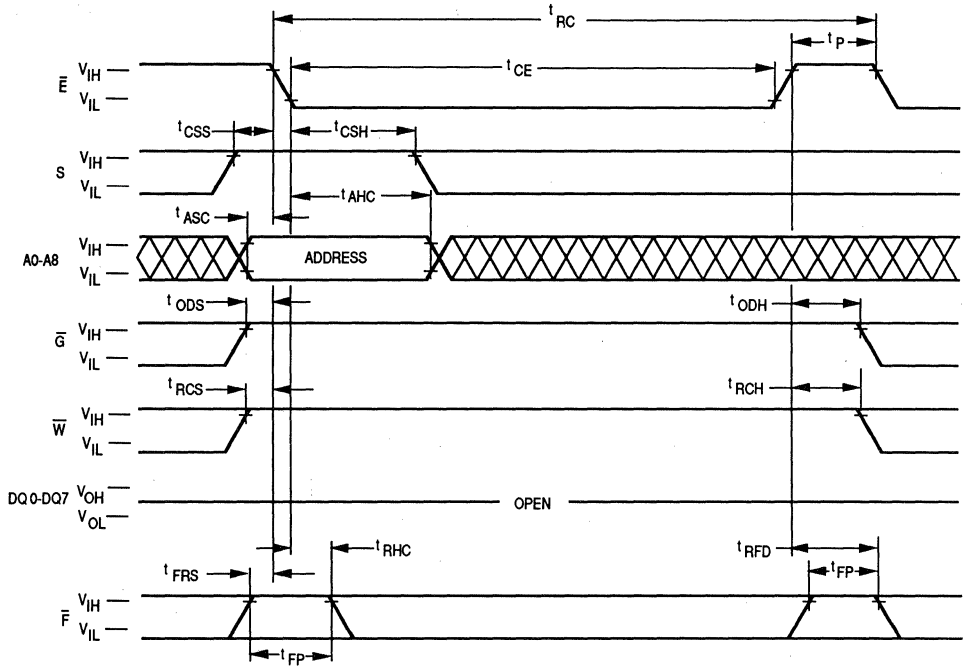


READ MODIFY WRITE CYCLE



5

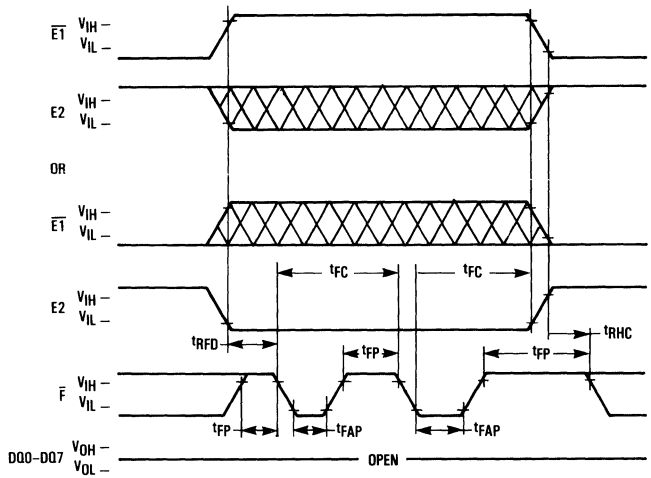
CHIP ENABLE ONLY REFRESH



NOTE: A9-A16 = Don't Care.

The chip enable only refresh is similar to the $\overline{RAS}$-only refresh of a DRAM. This type of refresh is accomplished by performing a memory cycle at each of the 512 rows (defined by A0-A8) within the specified refresh period.

AUTO REFRESH
($\overline{G}$, $\overline{W}$, A0-A16 = Don't Care)

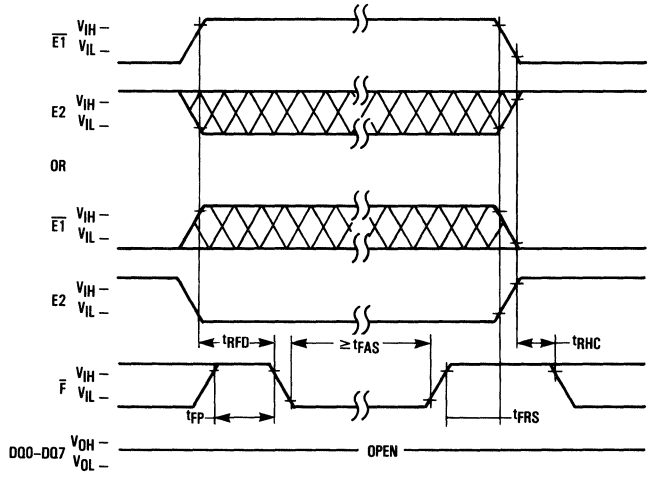


NOTE: During an auto refresh, an internal row address counter is incremented at the falling edge of $\overline{F}$, and a new row is refreshed. This diagram shows $\overline{F}$ toggling twice, thus refreshing 2 rows.

The auto refresh is similar to the $\overline{CAS}$-before-$\overline{RAS}$ refresh of a DRAM. When the $\overline{F}$ signal is clocked while $\overline{E}$ is high, the internal refresh counter and on-chip refresh circuitry are enabled and an internal refresh operation takes place. Each time the $\overline{F}$ signal is clocked (as specified and with $\overline{E}$ high), a subsequent row is refreshed and the internal refresh address counter is automatically incremented in preparation for the next auto refresh cycle. Note that the auto refresh $\overline{F}$ pulse width (t_{FAP}) must be more than 30 ns and less than 8 μs for this type of refresh operation to properly take place.

5

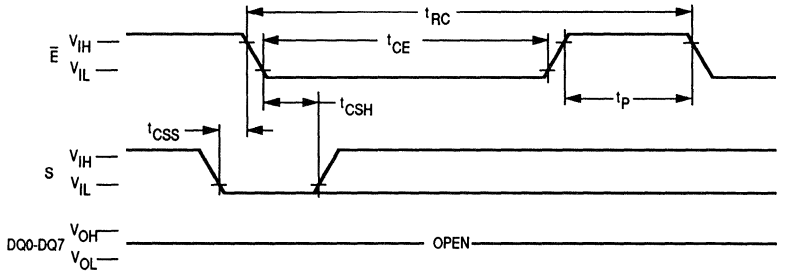
SELF REFRESH
($\overline{G}$, $\overline{W}$, A0-A16 = Don't Care)



NOTE: In the self refresh mode, after $\overline{F}$ has been held low for t_{FAS}, an internal timer will refresh a new row approximately every 150 μs. Due to the long period of this method of refresh, it is recommended that self refresh only be used for extremely long standby periods, such as a battery backup operation.

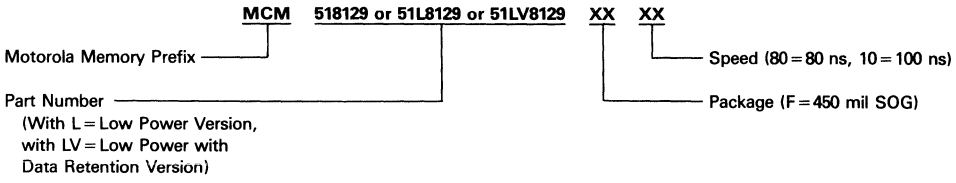
The self refresh is similar to the auto refresh and is recommended for use during the period when the PSRAM is in the standby mode for extended periods of time. For this type of refresh the $\overline{F}$ signal is held low for as long as the device is deselected. When the self refresh $\overline{F}$ pulse width (t_{FAS}) exceeds 8 μs, a timer activates an internal refresh operation at consecutive internal refresh address counter locations. Note that upon completion of the self refresh cycle the timing parameter t_{FRS} (chip enable delay time from $\overline{F}$ self refresh) must be followed for proper device operation during the following cycle.

CHIP SELECT STANDBY MODE



NOTE: $\overline{G}$, $\overline{W}$, A0-A16 = Don't Care.

ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers—MCM518129F10
MCM51L8129F80
MCM51L8129F10
MCM51LV8129F80
MCM51LV8129F10

5

General MOS Static RAMs

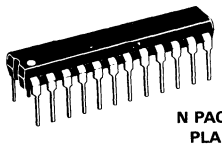
6

GENERAL STATIC RAMs (HCMOS unless otherwise noted)

Density	Organi-zation	Motorola Part Number	Address Access Time (ns Max)	Operating Current (mA Max)	Pin Count	Packaging
16K	2Kx8	MCM2018AN	35/45/55	135	24	300 mil, (P)DIP
256K	32Kx8	MCM60256A	85/100/120	70	28	(P)DIP, (F)SOG
		MCM60L256A	70/85/100/120	70	28	(P)DIP, (F)SOG
		MCM60L256A-C	100	70	28	(P)DIP, (F)SOG
		MCM60L256A-V	100	70	28	(P)DIP, (F)SOG

MCM2018A

Fast 16K Bit Static RAM



N PACKAGE
PLASTIC
CASE 724

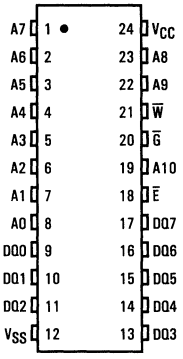
The MCM2018A is a 16,384 bit static random access memory organized as 2048 words by 8 bits, fabricated using Motorola's high-performance silicon-gate MOS (HMOS) technology. It uses an innovative design approach which combines the ease-of-use features of fully static operation (no external clocks or timing strobes required) with the reduced standby power dissipation associated with clocked memories. To the user this means low standby power dissipation without the need for address setup and hold times, nor reduced data rates due to cycle times that are longer than access times. Perfect for cache and sub-100 ns buffer memory systems, this high speed static RAM is intended for applications that demand superior performance and reliability.

Chip enable ($\overline{E}$) controls the power-down feature. It is not a clock but rather a chip control that affects power consumption. In less than a cycle time after $\overline{E}$ goes high, the part automatically reduces its power requirements and remains in this low-power standby mode as long as $\overline{E}$ remains high. This feature provides significant system-level power savings.

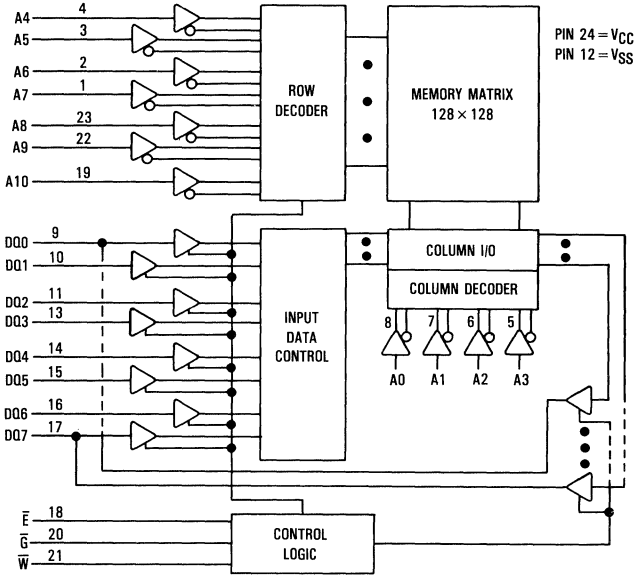
The MCM2018A is in a 24-pin dual-in-line 300 mil wide package with the industry standard JEDEC approved pinout.

- Single +5 V Operation, ±10%
- Fully Static: No Clock or Timing Strobe Required
- Fast Access Time: MCM2018A-35 = 35 ns (Maximum)
  MCM2018A-45 = 45 ns (Maximum)
- Power Supply Current: 135 mA Maximum (Active)
  20 mA Maximum (Standby)
- Three-State Output

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES	
A0-A10	Address Input
DQ0-DQ7	Data Input/Output
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E}$	Chip Enable
V_{CC}	+5 V Power Supply
V_{SS}	Ground

6

MODE SELECTION

Mode	$\overline{E}$	$\overline{G}$	$\overline{W}$	V_{CC} Current	DQ
Standby	H	X	X	I_{SB}	High Z
Read	L	L	H	I_{CC}	Q
Write Cycle	L	X	L	I_{CC}	D

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage on Any Pin With Respect to V_{SS}	V_{in}, V_{out}	−0.5 to +7.0	V
DC Output Current	I_{out}	±20	mA
Power Dissipation	P_D	1.1	Watt
Temperature Under Bias	T_{bias}	−10 to +80	°C
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

6

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.0	3.0	6.0	V
	V_{IL}	−0.5*	0	0.8	V

*The device will withstand undershoots to the −2.5 volt level with a maximum pulse width of 50 ns. This is periodically sampled rather than 100% tested.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (V_{CC} = 5.5 V, V_{in} = GND to V_{CC})	$I_{lkg(I)}$	−1.0	1.0	μA
Output Leakage Current ($\overline{E}$ = V_{IH} or $\overline{G}$ = V_{IH}, $V_{I/O}$ = GND to V_{CC})	$I_{lkg(O)}$	−1.0	1.0	μA
Operating Power Supply Current ($\overline{E}$ = V_{IL}, $I_{I/O}$ = 0 mA)	I_{CC}	—	135	mA
Standby Power Supply Current ($\overline{E}$ = V_{IH})	I_{SB}	—	20	mA
Output Low Voltage (I_{OL} = 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = −4.0 mA)	V_{OH}	2.4	—	V

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Typ	Max	Unit
Input Capacitance	All Inputs Except $\overline{E}$ and DQ	C_{in}	3	5	pF
	$\overline{E}$		5	7	
I/O Capacitance	DQ	$C_{I/O}$	5	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

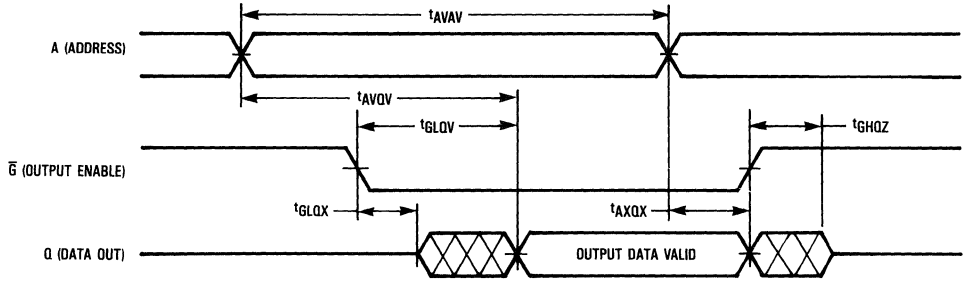
Input Pulse Levels . . . . . 0 and 3.0 V
Input Rise and Fall Times . . . . . 5 ns
Input and Output Timing Measurement Reference Levels . . . 1.5 V
Output Load . . . . . See Figure 1

READ CYCLE (See Note 1)

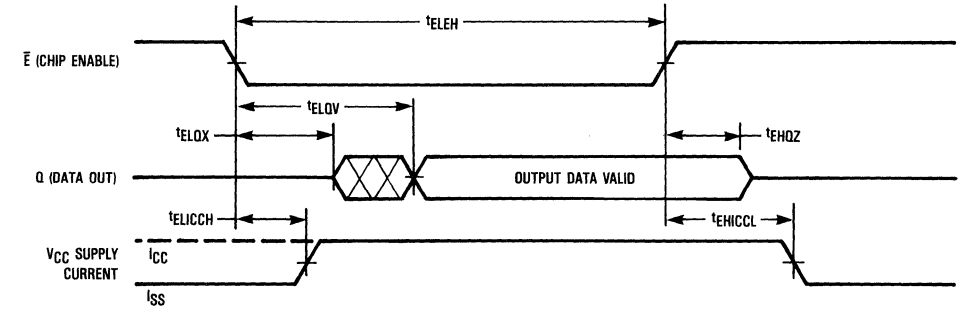
Parameter	Symbol		MCM2018A-35		MCM2018A-45		Units	Notes
	Standard	Alternate	Min	Max	Min	Max		
Address Valid to Address Valid (Read Cycle Time)	t_{AVAV}	t_{RC}	35	–	45	–	ns	
Address Valid to Output Valid (Address Access Time)	t_{AVQV}	t_{AC}	–	35	–	45	ns	
Chip Enable Low to Chip Enable High (Read Cycle Time)	t_{ELEH}	t_{RC}	35	–	45	–	ns	
Chip Enable Low to Output Valid (Chip Enable Access Time)	t_{ELQV}	t_{ACS}	–	35	–	45	ns	
Output Enable Low to Output Valid (Output Enable Access Time)	t_{GLQV}	t_{OE}	–	20	–	20	ns	
Chip Enable Low to Output Invalid (Chip Enable to Output Active)	t_{ELQX}	t_{CLZ}	5	–	5	–	ns	2
Chip Enable High to Output High Z (Chip Disable to Output Disable)	t_{EHQZ}	t_{CHZ}	0	20	0	20	ns	2
Output Enable Low to Output Invalid (Output Enable to Output Active)	t_{GLQX}	t_{OLZ}	0	–	0	–	ns	2
Output Enable High to Output High Z (Output Disable to Output Disable)	t_{GHQZ}	t_{OHZ}	0	20	0	20	ns	2
Address Invalid to Output Invalid (Output Hold Time)	t_{AXQX}	t_{OH}	5	–	5	–	ns	
Chip Enable Low to Power Up	t_{ELICCH}	t_{PU}	0	–	0	–	ns	
Chip Enable High to Power Down	t_{EHICCL}	t_{PD}	–	20	–	20	ns	

NOTES:
1. Transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IL} and V_{IH} (or between V_{IH} and V_{IL}) in a monotonic manner.
2. Transition is measured ±200 mV from the steady state output voltage with the output loading specified in Figure 1.
3. In read cycle 2, all addresses are valid prior to or coincident with chip enable ($\overline{E}$) transition low.

READ CYCLE 1 ($\overline{W} = V_{IH}$, $\overline{E} = V_{IL}$)



READ CYCLE 2 ($\overline{W} = V_{IH}$, $\overline{G} = V_{IL}$; See Note 3 Above)

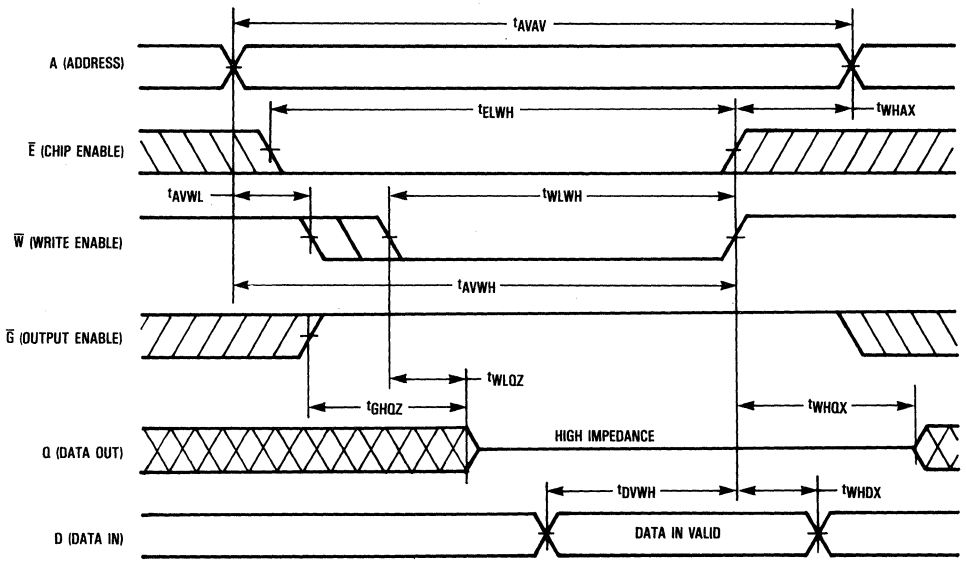


WRITE CYCLE (See Notes 1 and 2)

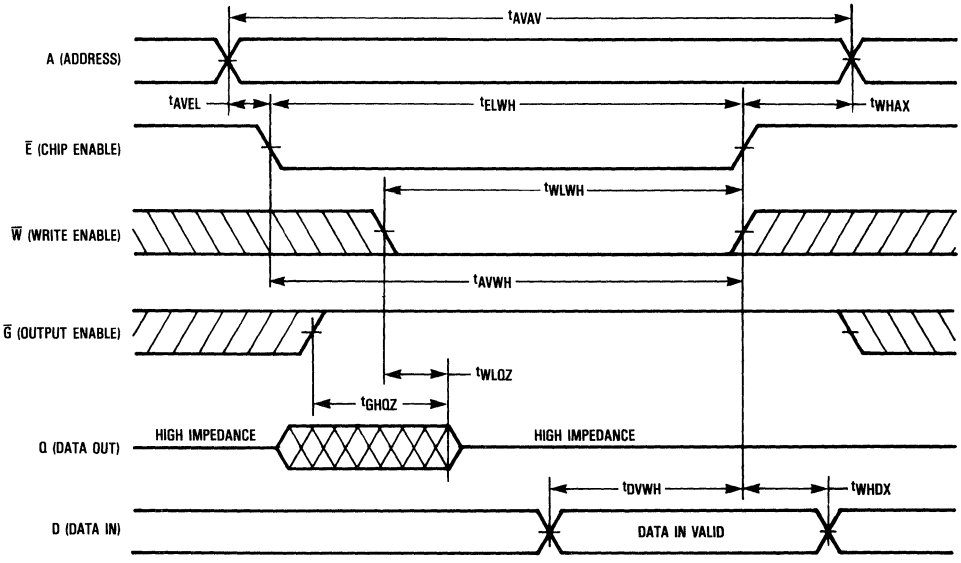
Parameter	Symbol		MCM2018A-35		MCM2018A-45		Units	Notes
	Standard	Alternate	Min	Max	Min	Max		
Address Valid to Address Valid (Write Cycle Time)	t_{AVAV}	t_{WC}	35	–	45	–	ns	
Chip Enable Low to Write High (Chip Enable to End of Write)	t_{ELWH}	t_{EW}	30	–	40	–	ns	
Address Valid to Chip Enable Low (Address Setup to Chip Enable)	t_{AVEL}	t_{AS}	0	–	0	–	ns	
Address Valid to Write Low (Address Setup to Write)	t_{AVWL}	t_{AS}	0	–	0	–	ns	
Address Valid to Write High	t_{AVWH}	t_{AW}	30	–	40	–	ns	3
Write Low to Write High (Write Pulse Width)	t_{WLWH}	t_{WP}	30	–	35	–	ns	
Write High to Address Don't Care (Address Hold After End of Write)	t_{WHAX}	t_{WR}	0	–	0	–	ns	4
Write High to Output Don't Care (Output Active After End of Write)	t_{WHQX}	t_{WLZ}	0	–	0	–	ns	5
Write Low to Output High Z (Write Enable to Output Disable)	t_{WLQZ}	t_{WHZ}	0	20	0	20	ns	5
Data Valid to Write High (Data Setup to End of Write)	t_{DVWH}	t_{DS}	15	–	20	–	ns	3
Write High to Data Don't Care (Data Hold After End of Write)	t_{WHDX}	t_{DH}	0	–	0	–	ns	3, 5
Output Enable High to Output High Z	t_{GHQZ}	t_{OHZ}	0	20	0	20	ns	

NOTES:
1. Write enable ($\overline{W}$) must be high during all address transitions.
2. If the chip enable ($\overline{E}$) low transition occurs simultaneously with the write enable ($\overline{W}$) transition, the output remains in a high impedance state.
3. Both chip enable ($\overline{E}$) and write enable ($\overline{W}$) must be active (low) to write data into the memory. Either signal can terminate the write cycle by going high. Data in setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
4. t_{WHAX} is measured from the earlier of, chip enable ($\overline{E}$) or write enable ($\overline{W}$) going high to the end of write cycle.
5. Output enable ($\overline{G}$) can be either low or high during a write cycle. If chip enable ($\overline{E}$) and $\overline{G}$ are both low during this period then the data input/output (DQ) pins are in the output state. Under these conditions input signals of opposite phase to the outputs must not be applied.

WRITE CYCLE 1 ($\overline{W}$ Controlled)



WRITE CYCLE 2 ($\overline{E}$ Controlled)



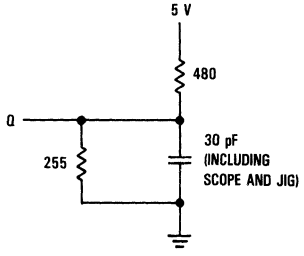


Figure 1. Output Load

ORDERING INFORMATION
(Order by Full Part Number)

MCM 2018A X XX

Motorola Memory Prefix

Part Number

Speed (35 = 35 ns, 45 = 45 ns)

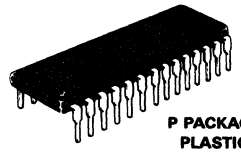
Package (N = 300-mil Plastic)

Full Part Numbers — MCM2018AN35
MCM2018AN45

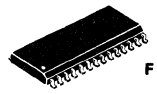
MCM60256A
MCM60L256A

Advance Information

32K x 8 Bit CMOS Static Random Access Memory



P PACKAGE
PLASTIC
CASE 710



F PACKAGE
SOG
CASE 751H

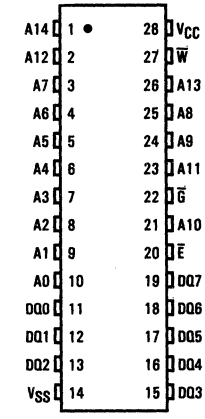
The MCM60256A is a 262,144 bit low-power static random access memory organized as 32,768 words of 8 bits, fabricated using silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides greater reliability. The operating current is 5 mA/MHz (typ) and the minimum cycle time is 85 ns. For long cycle times (>100 ns), the automatic power down (APD) circuitry will temporarily shut down various power consuming circuits, thereby reducing the active power consumption.

Chip enable ($\overline{E}$) controls the power-down feature. It is not a clock but rather a chip control that affects power consumption. When $\overline{E}$ is a logic high, the part is placed in low power standby mode. The maximum standby current for MCM60L256A is 2 μA (T_A=25°C). Chip enable also controls the data retention mode. Another control feature, output enable ($\overline{G}$) allows access to the memory contents as fast as 45 ns (MCM60256A-85). Thus the MCM60256A is suitable for use in various microprocessor application systems where high speed, low power, and battery backup are required.

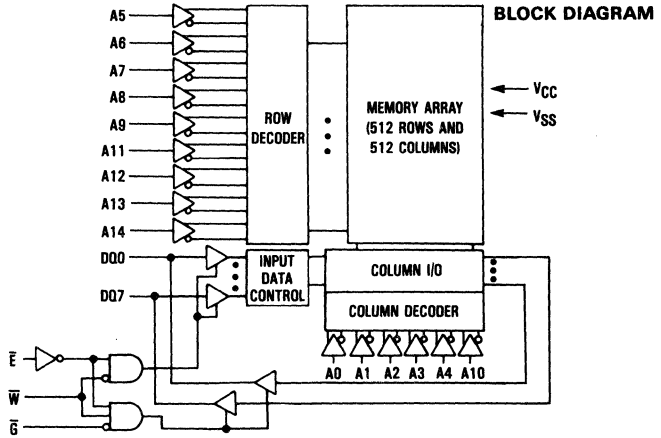
The MCM60256A is offered in a 600 mil, 28 pin plastic dual-in-line package as well as the 330 mil, 28 pin plastic small outline gullwing package.

- Single 5 V Supply, ±10%
- 32K x 8 Organization
- Fully Static — No Clock or Timing Strobes Necessary
- Low Power Dissipation—27.5 mW/MHz (Typical Active)
- Output Enable and Chip Enable Inputs for More System Design Flexibility and Low Power Standby Mode
- Battery Backup Capability (MCM60L256A)
- Data Retention Supply Voltage=2.0 V to 5.5 V
- All Inputs and Outputs Are TTL Compatible
- Three State Outputs
- Fast Access Times: MCM60256A-85 and MCM60L256A-85=85 ns (Max)
  MCM60256A-10 and MCM60L256A-10=100 ns (Max)
  MCM60256A-12 and MCM60L256A-12=120 ns (Max)

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES	
A0-A14	Address
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
DQ0-DQ7	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

This document contains information on a new product. Specifications and information herein are subject to change without notice.

TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	Supply Current	I/O Pin
H	X	X	Not Selected	I_{SB}	High Z
L	H	H	Output Disabled	I_{CC}	High Z
L	L	H	Read	I_{CC}	D_{out}
L	X	L	Write	I_{CC}	D_{in}

X = don't care

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.3 to +7.0	V
Voltage to Any Pin with Respect to V_{SS}	V_{in}, V_{out}	−0.5 to V_{CC}+0.5	V
Power Dissipation (T_A = 25°C) PDIP SOG	P_D	1.0 0.6	W
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

6

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	–	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	−0.3*	–	0.8	V

*V_{IL} (min) = −0.3 V dc; V_{IL} (min) = −3.0 V ac (pulse width ≤50 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	–	<0.01	±1.0	μA
Output Leakage Current ($\overline{E}$ = V_{IH} or $\overline{G}$ = V_{IH} or $\overline{W}$ = V_{IL}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	–	<0.01	±1.0	μA
Operating Current (Read Cycle)	I_{CCA1}				mA
($\overline{E}$ = V_{IL}, $\overline{W}$ = V_{IH}, Other Input = V_{IH}/V_{IL}, I_{out} = 0 mA)					
MCM60L256A: t_{AVAV} = 1 μs		–	10	15	
MCM60256A, MCM60L256A-85: t_{AVAV} = 85 ns		–	–	70	
MCM60256A, MCM60L256A-10: t_{AVAV} = 100 ns		–	–	70	
MCM60256A, MCM60L256A-12: t_{AVAV} = 120 ns		–	–	70	
($\overline{E}$ = 0.2 V, $\overline{W}$ = V_{CC} − 0.2 V, Other Input = V_{CC} − 0.2 V/0.2 V, I_{out} = 0 mA)	I_{CCA2}				
MCM60L256A: t_{AVAV} = 1 μs		–	5	8	
MCM60256A, MCM60L256A-85: t_{AVAV} = 85 ns		–	–	60	
MCM60256A, MCM60L256A-10: t_{AVAV} = 100 ns		–	–	60	
MCM60256A, MCM60L256A-12: t_{AVAV} = 120 ns		–	–	60	
Standby Current ($\overline{E}$ = V_{IH})	I_{SB1}	–	–	3.0	mA
Standby Current ($\overline{E}$ ≥ V_{CC} − 0.2 V, V_{CC} = 2.0 to 5.5 V) MCM60256A	I_{SB2}	–	2	100	μA
MCM60L256A		–	–	30	
MCM60L256A (T_A = 25°C)		–	–	2	
Output Low Voltage (I_{OL} = 4.0 mA)	V_{OL}	–	–	0.4	V
Output High Voltage (I_{OH} = −1.0 mA)	V_{OH}	2.4	–	–	V

Typical values are referenced to T_A = 25°C and V_{CC} = 5.0 V

CAPACITANCE (f = 1 MHz, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Min	Max	Unit
Input Capacitance (V_{in} = 0 V)	All Inputs Except DQ	C_{in}	–	10	pF
I/O Capacitance ($V_{I/O}$ = 0 V)	DQ	$C_{I/O}$	–	10	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

Input Pulse Levels . . . . . 0.6 V, 2.4 V
Input Rise/Fall Time . . . . . 5 ns
Input Timing Measurement Reference Levels . . . . . 1.5 V
Output Timing Measurement Reference Levels . . . . .0.8 and 2.2 V
Output Load . . . . . See Figure 1

READ CYCLE (See Note 1)

Parameter	Symbol	Alt Symbol	MCM60256A-85 MCM60L256A-85		MCM60256A-10 MCM60L256A-10		MCM60256A-12 MCM60L256A-12		Unit	Notes
			Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	85	–	100	–	120	–	ns	–
Address Access Time	t_{AVQV}	t_{AA}	–	85	–	100	–	120	ns	–
$\overline{E}$ Access Time	t_{ELQV}	t_{AC}	–	85	–	100	–	120	ns	–
$\overline{G}$ Access Time	t_{GLQV}	t_{OE}	–	45	–	50	–	60	ns	–
Output Hold from Address Change	t_{AXQX}	t_{OH}	10	–	10	–	10	–	ns	–
Chip Enable to Output Low-Z	t_{ELQX}	t_{CLZ}	10	–	10	–	10	–	ns	2, 3
Output Enable to Output Low-Z	t_{GLQX}	t_{OLZ}	5	–	5	–	5	–	ns	2, 3
Chip Enable to Output High-Z	t_{EHQZ}	t_{CHZ}	0	30	0	35	0	40	ns	2, 3
Output Enable to Output High-Z	t_{GHQZ}	t_{OHZ}	0	30	0	35	0	40	ns	2, 3

NOTES:
1. $\overline{W}$ is high at all times for read cycles.
2. All high-Z and low-Z parameters are considered in a high or low impedance state when the output has made a 100 mV transition from the previous steady state voltage.
3. These parameters are periodically sampled and not 100% tested.

READ CYCLE

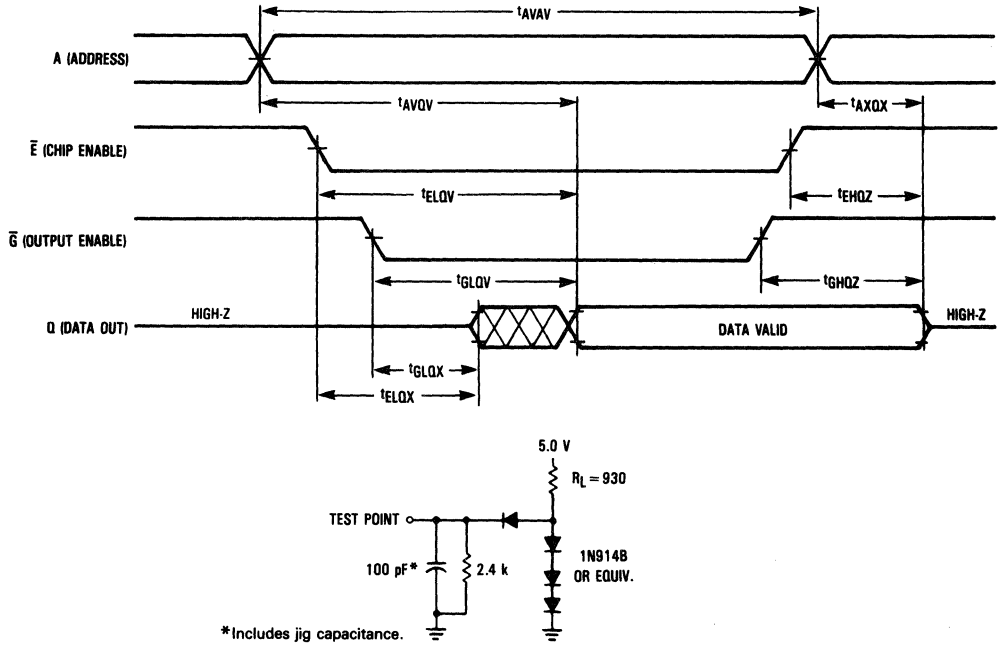


Figure 1. AC Test Load

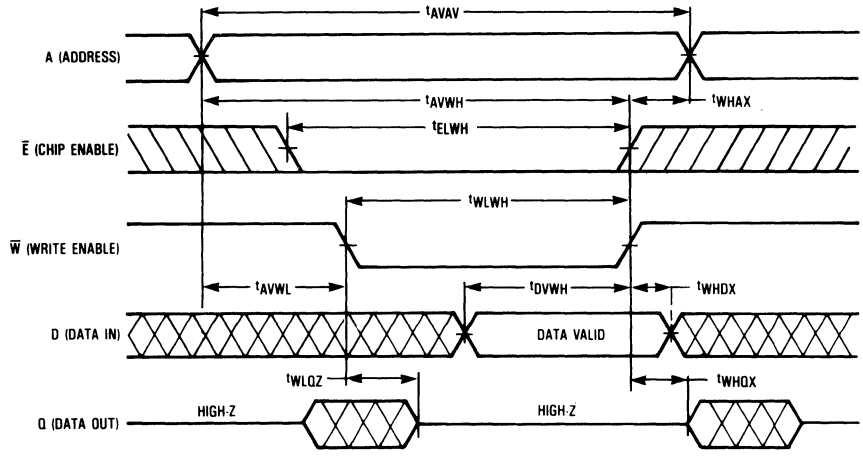
WRITE CYCLE 1 AND 2 (See Note 1)

Parameter	Symbol	Alt Symbol	MCM60256A-85 MCM60L256A-85		MCM60256A-10 MCM60L256A-10		MCM60256A-12 MCM60L256A-12		Unit	Notes
			Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	85	–	100	–	120	–	ns	–
Address Setup Time	t_{AVWL}/t_{AVEL}	t_{AS}	0	–	0	–	0	–	ns	–
Address Valid to End of Write	t_{AVWH}/t_{AVEH}	t_{AW}	75	–	80	–	85	–	ns	–
Write Pulse Width	t_{WLWH}	t_{WP}	60	–	60	–	70	–	ns	2
Data Valid to End of Write	t_{DVWH}/t_{DVEH}	t_{DW}	35	–	35	–	40	–	ns	–
Data Hold Time	t_{WHDX}/t_{EHDX}	t_{DH}	0	–	0	–	0	–	ns	–
Write Low to Output in High-Z	t_{WLQZ}	t_{WHZ}	0	25	0	25	0	30	ns	3, 4
Write High to Output Low-Z	t_{WHQX}	t_{WLZ}	10	–	10	–	10	–	ns	3, 4
Write Recovery Time	t_{WHAX}/t_{EHAX}	t_{WR}	5	–	0	–	0	–	ns	5
Chip Enable to End of Write	t_{ELWH}/t_{ELEH}	t_{CW}	65	–	80	–	85	–	ns	–

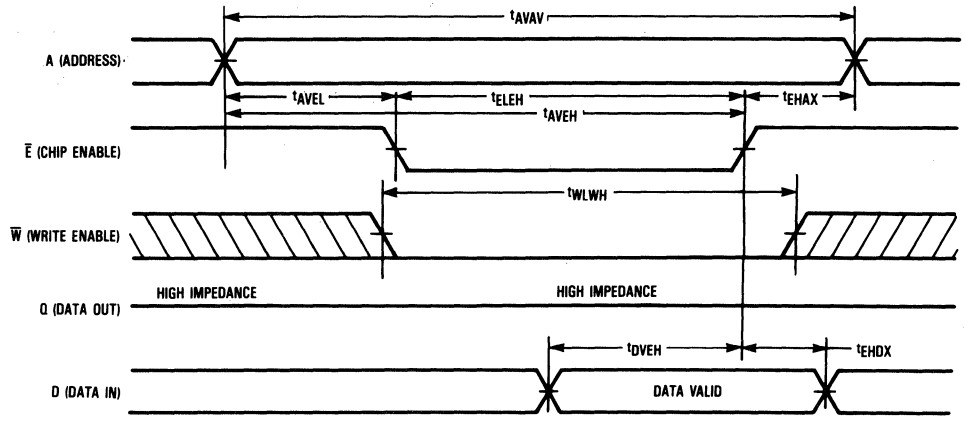
NOTES:
1. Outputs are in high impedance state if $\overline{G}$ is high during Write Cycle.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{E}$ and a low $\overline{W}$. If $\overline{W}$ goes low prior to $\overline{E}$ low then outputs will remain in a high impedance state.
3. All high-Z and low-Z parameters are considered in a high or low impedance state when the outputs have made a 100 mV transition from the previous steady state voltage.
4. These parameters are periodically sampled and not 100% tested.
5. t_{WR} is measured from the earlier of $\overline{E}$ or $\overline{W}$ going high to the end of write cycle.

6

WRITE CYCLE 1 ($\overline{W}$ CONTROLLED)



WRITE CYCLE 2 ($\overline{E}$ Controlled)

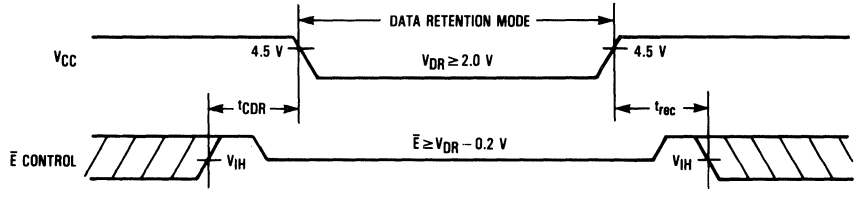


DATA RETENTION CHARACTERISTICS (T_A = 0 to +70°C)

Parameter		Symbol	Min	Typ	Max	Unit
V_{CC} for Data Retention ($\overline{E} \geq V_{CC} - 0.2$ V)		V_{DR}	2.0	—	5.5	V
Data Retention Current ($\overline{E} \geq V_{CC} - 0.2$ V)	MCM60256A : V_{CC} = 3.0 V	I_{CCDR}	—	—	50	µA
	V_{CC} = 5.5 V		—	—	100	
	MCM60L256A: V_{CC} = 3.0 V		—	—	10**	
	V_{CC} = 5.5 V		—	—	30	
Chip Disable to Data Retention Time		t_{CDR}	0	—	—	ns
Operation Recovery Time		t_{rec}	t_{AVAV}*	—	—	ns

*t_{AVAV} = Read Cycle Time
**This characteristic is guaranteed to meet 3 µA max at T_A = 0 to +40°C.

DATA RETENTION MODE



NOTE: If the V_{IH} of $\overline{E}$ is 2.4 V in operation, I_{SB1} current flows during the period that the V_{CC} voltage is decreasing from 4.5 V to 2.4 V.

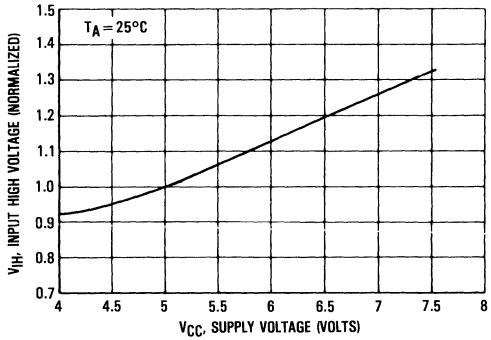


Figure 1. Input High Voltage versus Supply Voltage

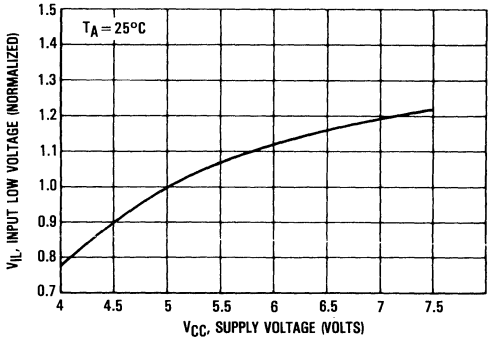


Figure 2. Input Low Voltage versus Supply Voltage

6

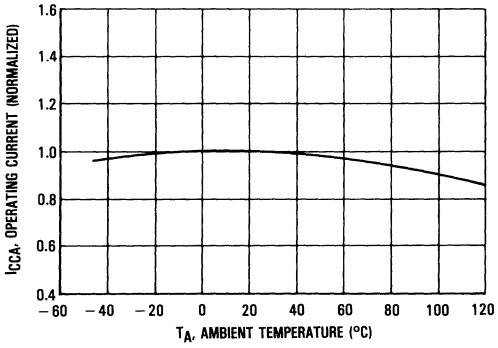


Figure 3. Operating Current versus Ambient Temperature

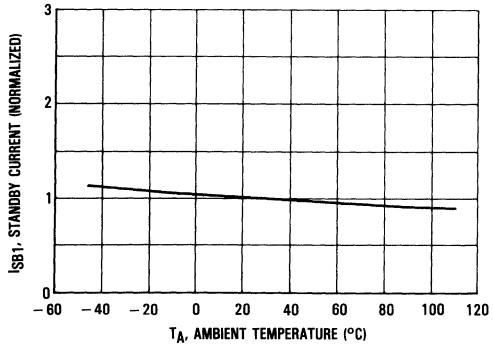


Figure 4. I_{SB1} Standby Current versus Ambient Temperature

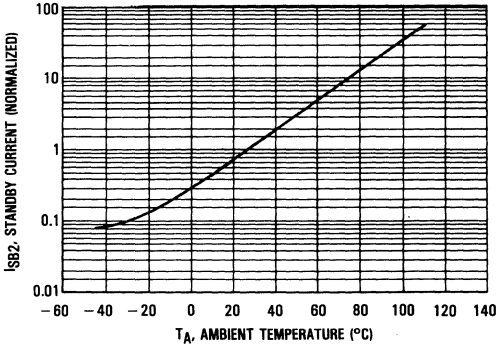


Figure 5. I_{SB2} Standby Current versus Ambient Temperature

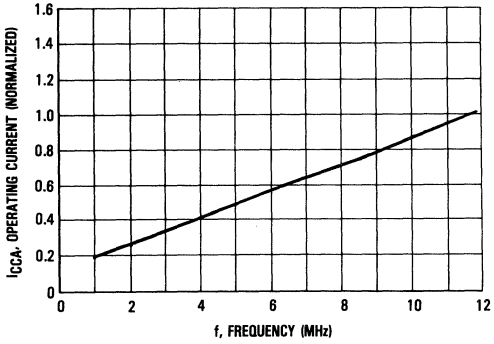


Figure 6. Low Power Operating Current versus Frequency (Read)

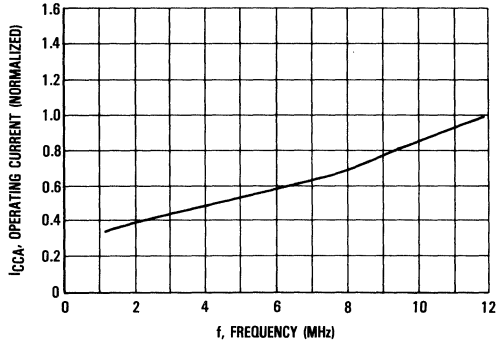


Figure 7. Operating Current versus Frequency (Write)

6

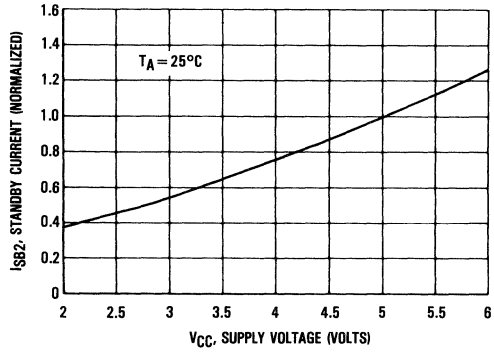


Figure 8. Low Power I_{SB2} Standby Current versus Supply Voltage

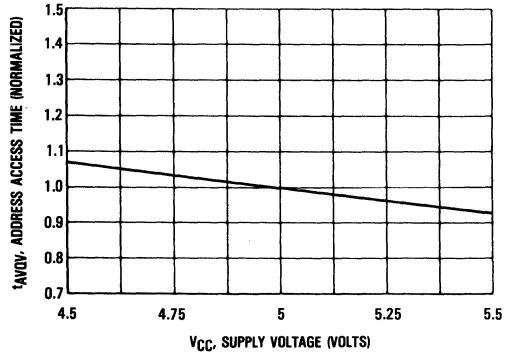


Figure 9. Access Time versus Supply Voltage

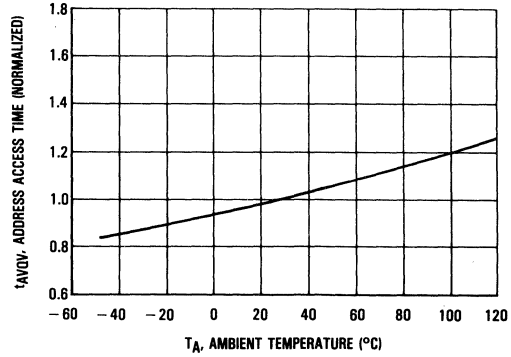
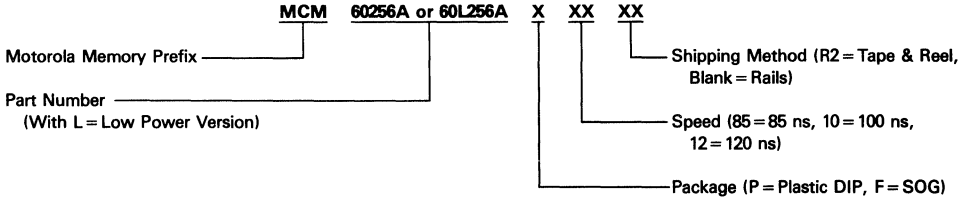


Figure 10. Access Time versus Ambient Temperature

ORDERING INFORMATION
(Order by Full Part Number)



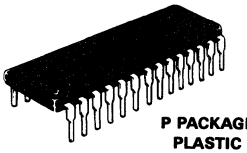
Full Part Numbers—	MCM60256AP85	MCM60256AF85	MCM60256AF85R2
	MCM60256AP10	MCM60256AF10	MCM60256AF10R2
	MCM60256AP12	MCM60256AF12	MCM60256AF12R2
	MCM60L256AP85	MCM60L256AF85	MCM60L256AF85R2
	MCM60L256AP10	MCM60L256AF10	MCM60L256AF10R2
	MCM60L256AP12	MCM60L256AF12	MCM60L256AF12R2

6

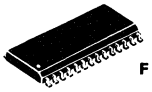
MCM60L256A-70

Advance Information

32K x 8 Bit CMOS Static Random Access Memory



P PACKAGE
PLASTIC
CASE 710



F PACKAGE
SOG
CASE 751H

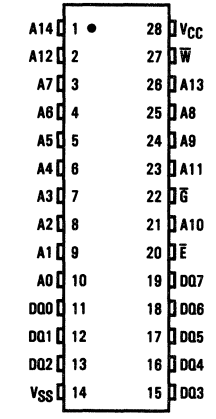
The MCM60L256A-70 is a 262,144 bit low-power static random access memory organized as 32,768 words of 8 bits, fabricated using silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides greater reliability. The operating current is 5 mA/MHz (typ) and the minimum cycle time is 70 ns. For long cycle times (>100 ns), the automatic power down (APD) circuitry will temporarily shut down various power consuming circuits, thereby reducing the active power consumption.

Chip enable ($\overline{E}$) controls the power-down feature. It is not a clock but rather a chip control that affects power consumption. When $\overline{E}$ is a logic high, the part is placed in low power standby mode. The maximum standby current for MCM60L256A-70 is 2 μA (T_A=25°C). Chip enable also controls the data retention mode. Another control feature, output enable ($\overline{G}$) allows access to the memory contents as fast as 40 ns (MCM60L256A-70). Thus the MCM60L256A-70 is suitable for use in various microprocessor application systems where high speed, low power, and battery backup are required.

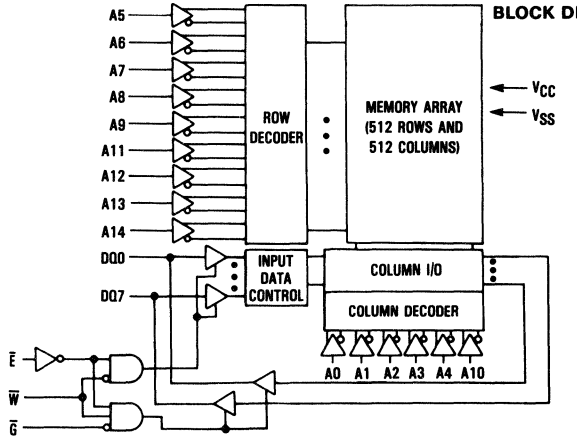
The MCM60L256A-70 is offered in a 600 mil, 28 pin plastic dual-in-line package (PDIP) as well as the 330 mil, 28 pin plastic small outline gullwing package (SOG).

- Single 5 V Supply, ±10%
- 32K x 8 Organization
- Fully Static — No Clock or Timing Strobes Necessary
- Low Power Dissipation—27.5 mW/MHz (Typical Active)
- Output Enable and Chip Enable Inputs for More System Design Flexibility and Low Power Standby Mode
- Battery Backup Capability
- Data Retention Supply Voltage=2.0 V to 5.5 V
- All Inputs and Outputs Are TTL Compatible
- Three State Outputs
- Fast Access Times: 70 ns (Max)

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A0-A14	Address
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
DQ0-DQ7	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

This document contains information on a new product. Specifications and information herein are subject to change without notice.

TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	Supply Current	I/O Pin
H	X	X	Not Selected	I_{SB}	High Z
L	H	H	Output Disabled	I_{CC}	High Z
L	L	H	Read	I_{CC}	D_{out}
L	X	L	Write	I_{CC}	D_{in}

X = don't care

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.3 to +7.0	V
Voltage to Any Pin with Respect to V_{SS}	V_{in}, V_{out}	−0.5 to V_{CC}+0.5	V
Power Dissipation (T_A = 25°C) PDIP SOG	P_D	1.0 0.6	W
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

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DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	–	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	−0.3*	–	0.8	V

*V_{IL} (min) = −0.3 V dc; V_{IL} (min) = −3.0 V ac (pulse width ≤50 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	–	<0.01	±1.0	μA
Output Leakage Current ($\overline{E}$ = V_{IH} or $\overline{G}$ = V_{IH} or $\overline{W}$ = V_{IL}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	–	<0.01	±1.0	μA
Operating Current (Read Cycle) ($\overline{E}$ = V_{IL}, $\overline{W}$ = V_{IH}, Other Input = V_{IH}/V_{IL}, I_{out} = 0 mA) MCM60L256A-70: t_{AVAV} = 1 μs MCM60L256A-70: t_{AVAV} = 70 ns	I_{CCA1}	 – –	 10 –	 15 70	mA
($\overline{E}$ = 0.2 V, $\overline{W}$ = V_{CC} − 0.2 V, Other Input = V_{CC} − 0.2 V/0.2 V, I_{out} = 0 mA) MCM60L256A-70: t_{AVAV} = 1 μs MCM60L256A-70: t_{AVAV} = 70 ns	I_{CCA2}	 – –	 5 –	 8 60	
Standby Current ($\overline{E}$ = V_{IH})	I_{SB1}	–	–	3.0	mA
Standby Current ($\overline{E}$ ≥ V_{CC} − 0.2 V, V_{CC} = 2.0 to 5.5 V) MCM60L256A-70 MCM60L256A-70 (T_A = 25°C)	I_{SB2}	– –	– –	30 2	μA
Output Low Voltage (I_{OL} = 4.0 mA)	V_{OL}	–	–	0.4	V
Output High Voltage (I_{OH} = −1.0 mA)	V_{OH}	2.4	–	–	V

Typical values are referenced to T_A = 25°C and V_{CC} = 5.0 V

CAPACITANCE (f = 1 MHz, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Min	Max	Unit
Input Capacitance (V_{in} = 0 V)	All Inputs Except DQ	C_{in}	–	10	pF
I/O Capacitance ($V_{I/O}$ = 0 V)	DQ	$C_{I/O}$	–	10	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC}=5.0 V ±10%, T_A=0 to 70°C, Unless Otherwise Noted)

Input Pulse Levels . . . . . 0.6 V, 2.4 V
Input Rise/Fall Time . . . . . 5 ns
Input Timing Measurement Reference Levels . . . . . 1.5 V
Output Timing Measurement Reference Levels . . . . .0.8 and 2.2 V
Output Load . . . . . See Figure 1

READ CYCLE (See Note 1)

Parameter	Symbol	Alt Symbol	MCM60L256A-70		Unit	Notes
			Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	70	–	ns	–
Address Access Time	t_{AVQV}	t_{AA}	–	70	ns	–
$\overline{E}$ Access Time	t_{ELQV}	t_{AC}	–	70	ns	–
$\overline{G}$ Access Time	t_{GLQV}	t_{OE}	–	40	ns	–
Output Hold from Address Change	t_{AXQX}	t_{OH}	10	–	ns	–
Chip Enable to Output Low-Z	t_{ELQX}	t_{CLZ}	10	–	ns	2, 3
Output Enable to Output Low-Z	t_{GLQX}	t_{OLZ}	5	–	ns	2, 3
Chip Enable to Output High-Z	t_{EHQZ}	t_{CHZ}	0	25	ns	2, 3
Output Enable to Output High-Z	t_{GHQZ}	t_{OHZ}	0	25	ns	2, 3

NOTES:
1. $\overline{W}$ is high at all times for read cycles.
2. All high-Z and low-Z parameters are considered in a high or low impedance state when the output has made a 100 mV transition from the previous steady state voltage.
3. These parameters are periodically sampled and not 100% tested.

READ CYCLE

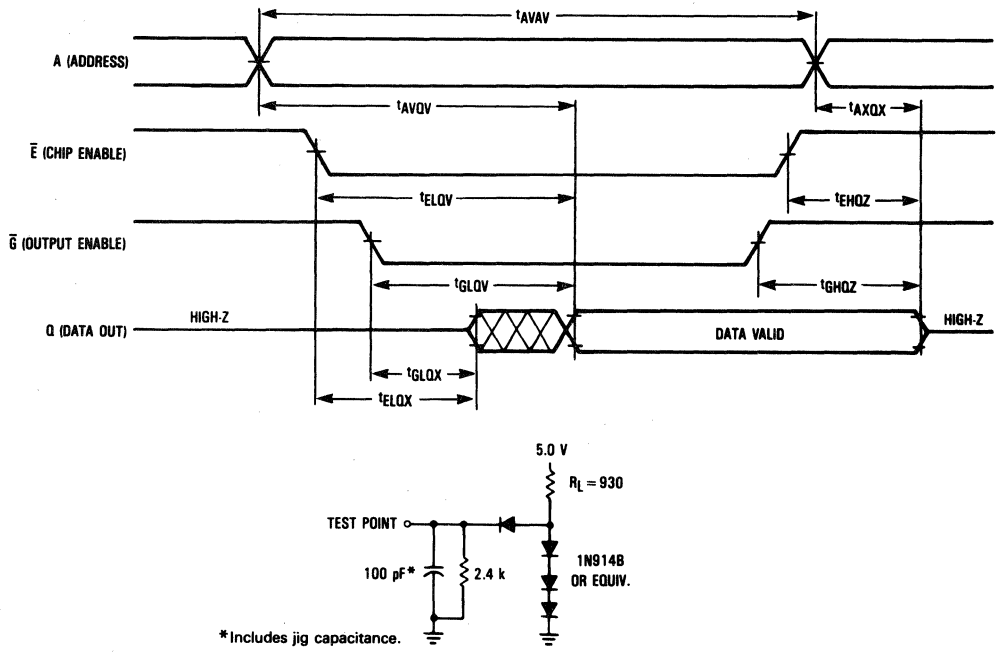


Figure 1. AC Test Load

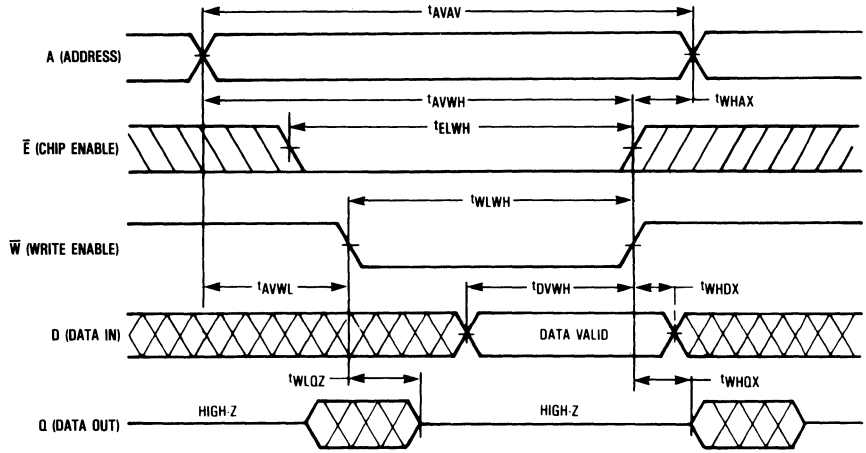
WRITE CYCLE 1 AND 2 (See Note 1)

Parameter	Symbol	Alt Symbol	MCM60L256A-70		Unit	Notes
			Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	70	–	ns	–
Address Setup Time	t_{AVWL}/t_{AVEL}	t_{AS}	0	–	ns	–
Address Valid to End of Write	t_{AVWH}/t_{AVEH}	t_{AW}	60	–	ns	–
Write Pulse Width	t_{WLWH}	t_{WP}	50	–	ns	2
Data Valid to End of Write	t_{DVWH}/t_{DVEH}	t_{DW}	25	–	ns	–
Data Hold Time	t_{WHDX}/t_{EHDX}	t_{DH}	0	–	ns	–
Write Low to Output in High-Z	t_{WLQZ}	t_{WHZ}	0	25	ns	3, 4
Write High to Output Low-Z	t_{WHQX}	t_{WLZ}	5	–	ns	3, 4
Write Recovery Time	t_{WHAX}/t_{EHAX}	t_{WR}	0	–	ns	5
Chip Enable to End of Write	t_{ELWH}/t_{ELEH}	t_{CW}	50	–	ns	–

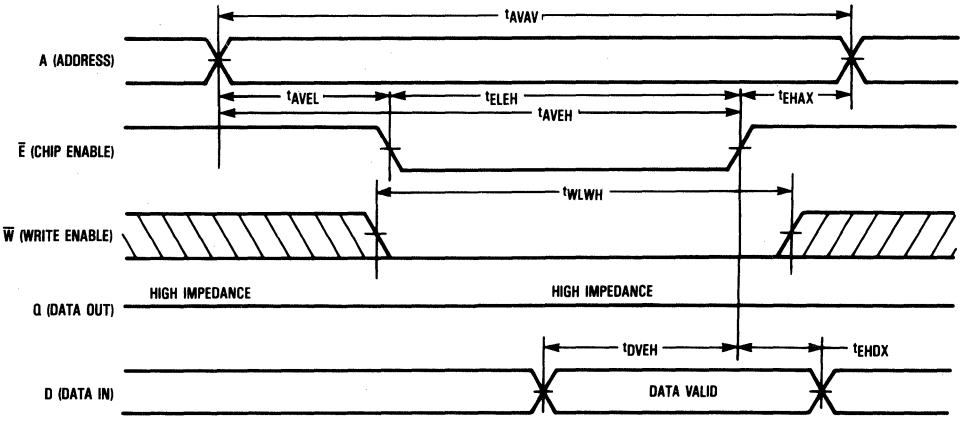
NOTES:
1. Outputs are in high impedance state if $\overline{G}$ is high during Write Cycle.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{E}$ and a low $\overline{W}$. If $\overline{W}$ goes low prior to $\overline{E}$ low then outputs will remain in a high impedance state.
3. All high-Z and low-Z parameters are considered in a high or low impedance state when the outputs have made a 100 mV transition from the previous steady state voltage.
4. These parameters are periodically sampled and not 100% tested.
5. t_{WR} is measured from the earlier of $\overline{E}$ or $\overline{W}$ going high to the end of write cycle.

6

WRITE CYCLE 1 ($\overline{W}$ CONTROLLED)



WRITE CYCLE 2 ($\overline{E}$ CONTROLLED)

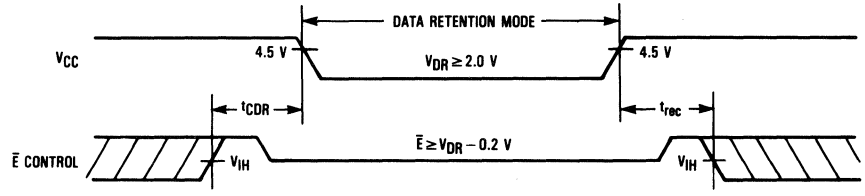


DATA RETENTION CHARACTERISTICS (T_A = 0 to +70°C)

Parameter		Symbol	Min	Typ	Max	Unit
V_{CC} for Data Retention ($\overline{E} \geq V_{CC} - 0.2$ V)		V_{DR}	2.0	–	5.5	V
Data Retention Current ($\overline{E} \geq V_{CC} - 0.2$ V)	MCM60L256A-70: V_{CC} = 3.0 V	I_{CCDR}	–	–	10**	μA
	V_{CC} = 5.5 V		–	–	30	
Chip Disable to Data Retention Time		t_{CDR}	0	–	–	ns
Operation Recovery Time		t_{rec}	t_{AVAV}*	–	–	ns

*t_{AVAV} = Read Cycle Time
**This characteristic is guaranteed to meet 3 μA max at T_A = 0 to +40°C.

DATA RETENTION MODE



NOTE: If the V_{IH} of $\overline{E}$ is 2.4 V in operation, I_{SB1} current flows during the period that the V_{CC} voltage is decreasing from 4.5 V to 2.4 V.

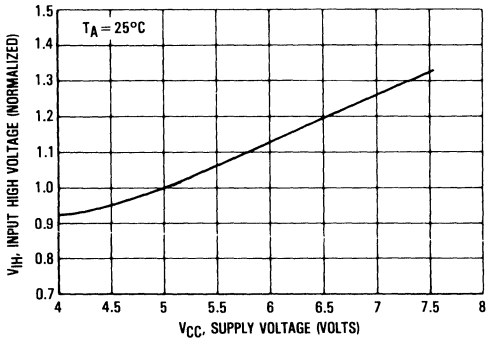


Figure 1. Input High Voltage versus Supply Voltage

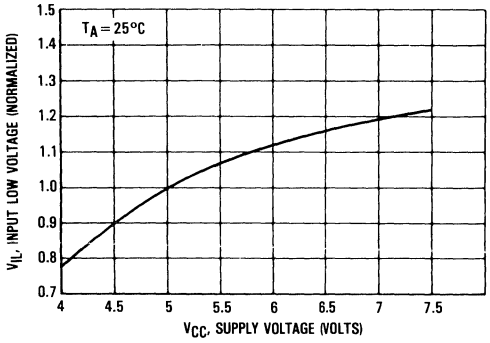


Figure 2. Input Low Voltage versus Supply Voltage

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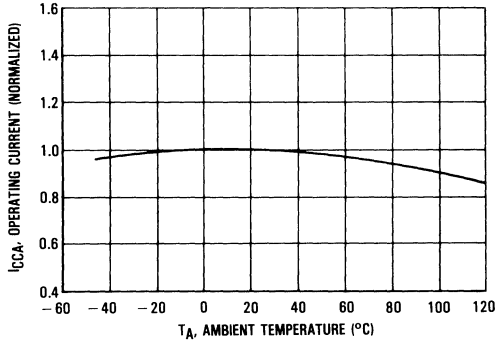

Figure 3. Operating Current versus Ambient Temperature

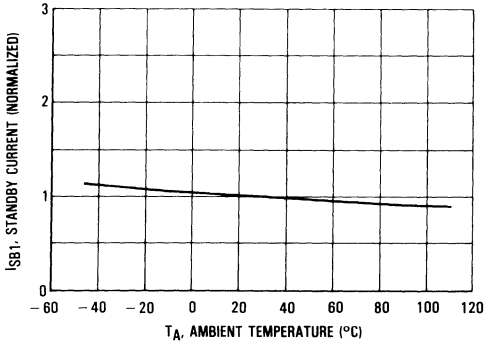

Figure 4. I_{SB1} Standby Current versus Ambient Temperature

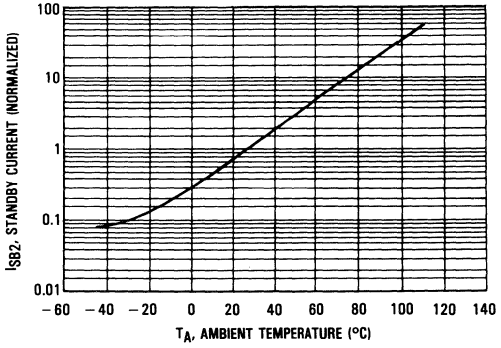

Figure 5. I_{SB2} Standby Current versus Ambient Temperature

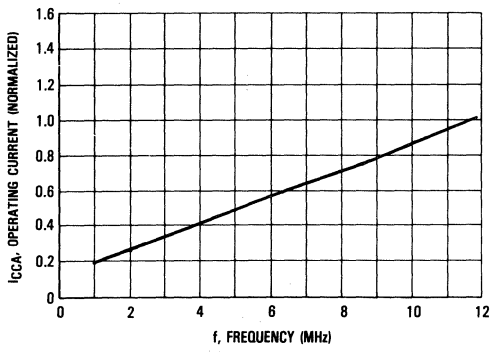

Figure 6. Low Power Operating Current versus Frequency (Read)

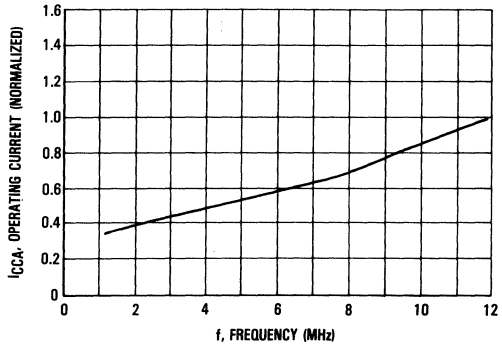

Figure 7. Operating Current versus Frequency (Write)

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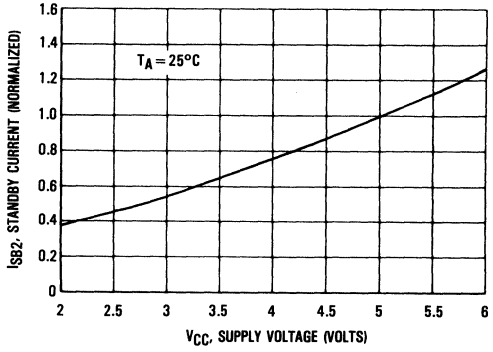


Figure 8. Low Power I_{SB2} Standby Current versus Supply Voltage

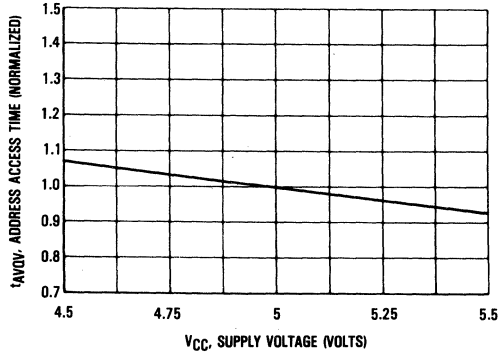


Figure 9. Access Time versus Supply Voltage

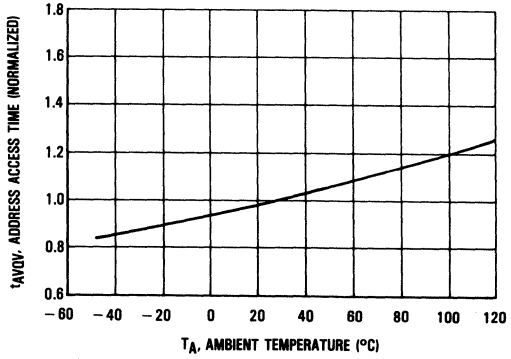
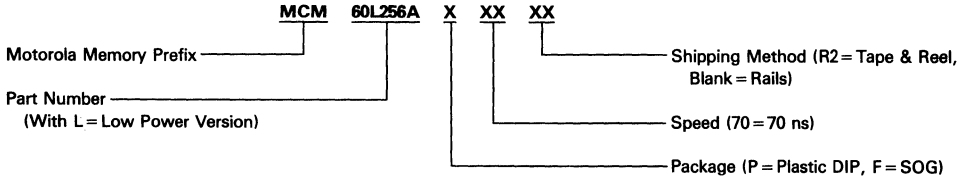


Figure 10. Access Time versus Ambient Temperature

ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers—MCM60L256AP70 MCM60L256AF70 MCM60L256AF70R2

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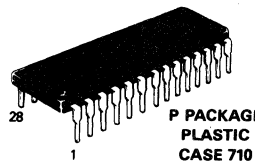
MCM60256A-C
MCM60L256A-C

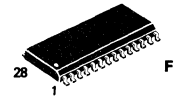
Advance Information

32K x 8 Bit CMOS Static Random Access Memory

Industrial Temperature Range: – 40 to 85°C



P PACKAGE
PLASTIC
CASE 710



F PACKAGE
SOG
CASE 751H

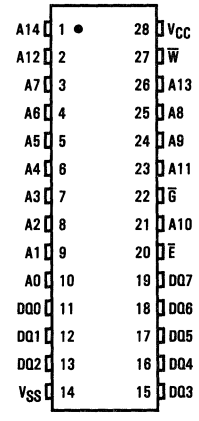
The MCM60256A-C is a 262,144 bit low-power static random access memory organized as 32,768 words of 8 bits, fabricated using silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides greater reliability. The operating current is 5 mA/MHz (typ) and the cycle time is 100 ns. For long cycle times (>100 ns), the automatic power down (APD) circuitry will temporarily shut down various power consuming circuits, thereby reducing the active power consumption.

Chip enable ($\overline{E}$) controls the power-down feature. It is not a clock but rather a chip control that affects power consumption. When $\overline{E}$ is a logic high, the part is placed in low power standby mode. The maximum standby current is 2 μA (T_A=25°C). Chip enable also controls the data retention mode. Another control feature, output enable ($\overline{G}$) allows access to the memory contents as fast as 50 ns. Thus the MCM60256A-C is suitable for use in various microprocessor application systems where high speed, low power, and battery backup are required.

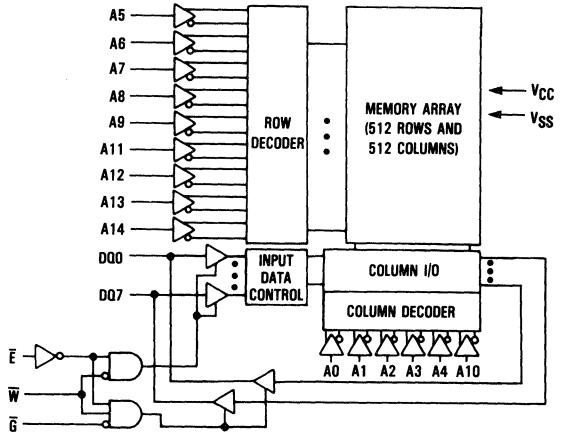
The MCM60256A-C is offered in a 28 pin, 600 mil plastic dual-in-line package and a 330 mil gull-wing SO package.

- Single 5 V Supply, ±10%
- 32K x 8 Organization
- Fully Static — No Clock or Timing Strobes Necessary
- Low Power Dissipation—27.5 mW/MHz (Typical Active)
- Output Enable and Chip Enable Inputs for More System Design Flexibility and Low Power Standby Mode
- Battery Backup Capability (Maximum Standby Current=2 μA @ 25°C)
- Data Retention Supply Voltage=2.0 V to 5.5 V
- All Inputs and Outputs Are TTL Compatible
- Three State Outputs
- Fast Access Time: MCM60256A-C10 and MCM60L256A-C10=100 ns (Max)

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A0-A14	Address
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
DQ0-DQ7	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

This document contains information on a new product. Specifications and information herein are subject to change without notice.

TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	Supply Current	I/O Pin
H	X	X	Not Selected	I_{SB}	High Z
L	H	H	Output Disabled	I_{CC}	High Z
L	L	H	Read	I_{CC}	D_{out}
L	X	L	Write	I_{CC}	D_{in}

X = don't care

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.3 to +7.0	V
Voltage to Any Pin with Respect to V_{SS}	V_{in}, V_{out}	−0.5 to V_{CC} +0.5	V
Power Dissipation (T_A = 25°C) PDIP SOG	P_D	1.0 0.6	W
Operating Temperature	T_A	−40 to +85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

6

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = −40 to 85°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} +0.3	V
Input Low Voltage	V_{IL}	−0.3*	—	0.8	V

*V_{IL} (min) = −0.3 V dc; V_{IL} (min) = −3.0 V ac (pulse width ≤50 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	<0.01	±1.0	μA
Output Leakage Current ($\overline{E}$ = V_{IH} or $\overline{G}$ = V_{IH} or $\overline{W}$ = V_{IL}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	<0.01	±1.0	μA
Operating Current (Read Cycle) ($\overline{E}$ = V_{IL}, $\overline{W}$ = V_{IH}, Other Input = V_{IH}/V_{IL}, I_{out} = 0 mA) t_{AVQV} = 1 μs t_{AVQV} = 100 ns	I_{CCA1}	— —	10 —	15 70	mA
($\overline{E}$ = 0.2 V, $\overline{W}$ = V_{CC} − 0.2 V, Other Input = V_{CC} − 0.2 V/0.2 V, I_{out} = 0 mA) t_{AVQV} = 1 μs t_{AVQV} = 100 ns	I_{CCA2}	— —	5 —	8 60	
Standby Current ($\overline{E}$ = V_{IH})	I_{SB1}	—	—	3.0	mA
Standby Current ($\overline{E}$ ≥ V_{CC} − 0.2 V, V_{CC} = 2.0 to 5.5 V) (T_A = 25°C)	I_{SB2}	— —	2 —	100 2	μA
Output Low Voltage (I_{OL} = 4.0 mA)	V_{OL}	—	—	0.4	V
Output High Voltage (I_{OH} = −1.0 mA)	V_{OH}	2.4	—	—	V

Typical values are referenced to T_A = 25°C and V_{CC} = 5.0 V

CAPACITANCE (f = 1 MHz, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Min	Max	Unit
Input Capacitance (V_{in} = 0 V)	All Inputs Except DQ	C_{in}	—	10	pF
I/O Capacitance ($V_{I/O}$ = 0 V)	DQ	$C_{I/O}$	—	10	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = −40 to 85°C, Unless Otherwise Noted)

Input Pulse Levels . . . . . 0.6 V, 2.4 V
Input Rise/Fall Time . . . . . 5 ns
Input Timing Measurement Reference Levels . . . . . 1.5 V
Output Timing Measurement Reference Levels . . . . .0.8 and 2.2 V
Output Load . . . . . See Figure 1

READ CYCLE (See Note 1)

Parameter	Symbol	Alt Symbol	Min	Max	Unit	Notes
Read Cycle Time	t_{AVAV}	t_{RC}	100	–	ns	–
Address Access Time	t_{AVQV}	t_{AA}	–	100	ns	–
$\overline{E}$ Access Time	t_{ELQV}	t_{AC}	–	100	ns	–
$\overline{G}$ Access Time	t_{GLQV}	t_{OE}	–	50	ns	–
Output Hold from Address Change	t_{AXQX}	t_{OH}	10	–	ns	–
Chip Enable to Output Low-Z	t_{ELQX}	t_{CLZ}	10	–	ns	2, 3
Output Enable to Output Low-Z	t_{GLQX}	t_{OLZ}	5	–	ns	2, 3
Chip Enable to Output High-Z	t_{EHQZ}	t_{CHZ}	0	35	ns	2, 3
Output Enable to Output High-Z	t_{GHQZ}	t_{OHZ}	0	35	ns	2, 3

NOTES:
1. $\overline{W}$ is high at all times for read cycles.
2. All high-Z and low-Z parameters are considered in a high or low impedance state when the output has made a 100 mV transition from the previous steady state voltage.
3. These parameters are periodically sampled and not 100% tested.

READ CYCLE

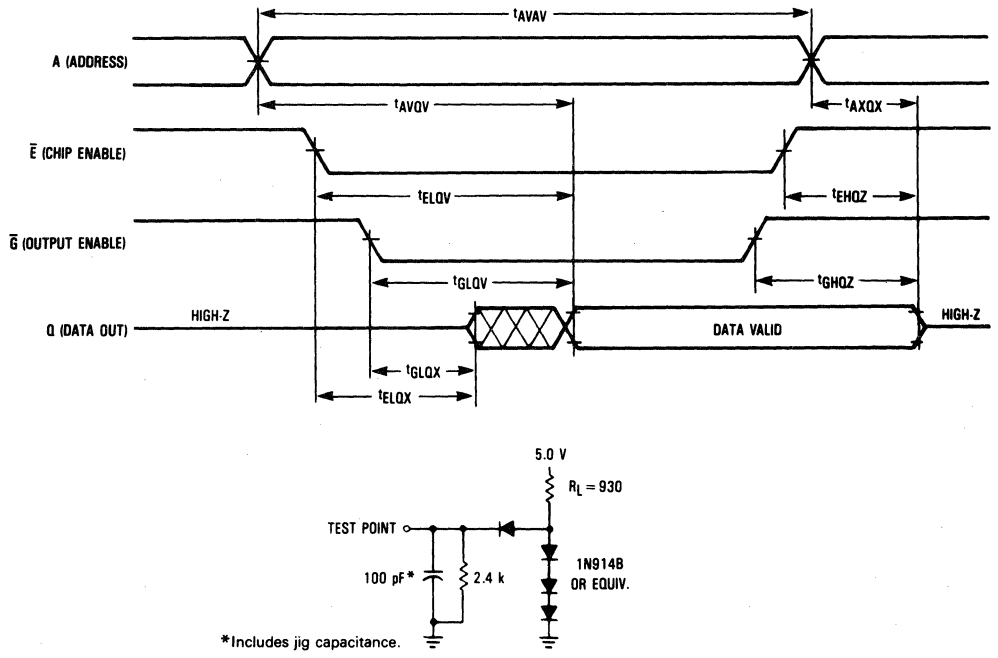


Figure 1. AC Test Load

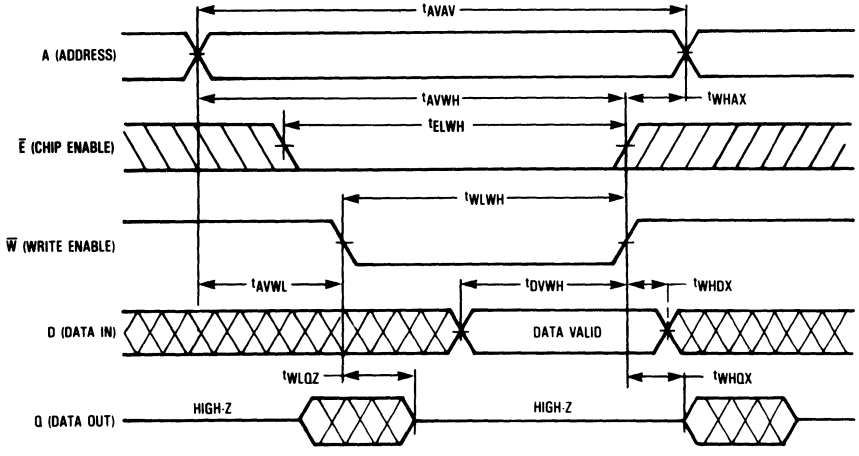
WRITE CYCLE 1 AND 2 (See Note 1)

Parameter	Symbol	Alt Symbol	Min	Max	Unit	Notes
Write Cycle Time	t_{AVAV}	t_{WC}	100	–	ns	–
Address Setup Time	t_{AVWL}/t_{AVEL}	t_{AS}	0	–	ns	–
Address Valid to End of Write	t_{AVWH}/t_{AVEH}	t_{AW}	80	–	ns	–
Write Pulse Width	t_{WLWH}	t_{WP}	60	–	ns	2
Data Valid to End of Write	t_{DVWH}/t_{DVEH}	t_{DW}	35	–	ns	–
Data Hold Time	t_{WHDX}/t_{EHDX}	t_{DH}	0	–	ns	–
Write Low to Output in High-Z	t_{WLQZ}	t_{WHZ}	0	25	ns	3, 4
Write High to Output Low-Z	t_{WHQX}	t_{WLZ}	10	–	ns	3, 4
Write Recovery Time	t_{WHAX}/t_{EHAX}	t_{WR}	0	–	ns	5
Chip Enable to End of Write	t_{ELWH}/t_{ELEH}	t_{CW}	80	–	ns	–

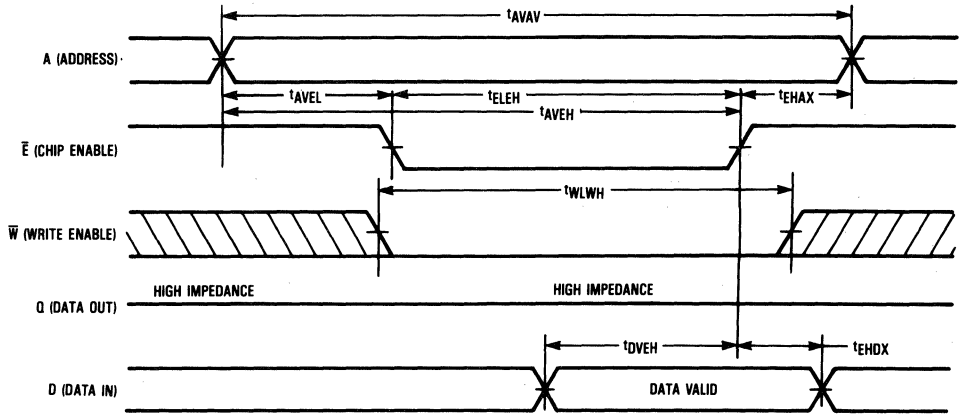
NOTES:
1. Outputs are in high impedance state if $\overline{G}$ is high during Write Cycle.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{E}$ and a low $\overline{W}$. If $\overline{W}$ goes low prior to $\overline{E}$ low then outputs will remain in a high impedance state.
3. All high-Z and low-Z parameters are considered in a high or low impedance state when the outputs have made a 100 mV transition from the previous steady state voltage.
4. These parameters are periodically sampled and not 100% tested.
5. t_{WR} is measured from the earlier of $\overline{E}$ or $\overline{W}$ going high to the end of write cycle.

6

WRITE CYCLE 1 ($\overline{W}$ CONTROLLED)



WRITE CYCLE 2 ($\overline{E}$ Controlled)

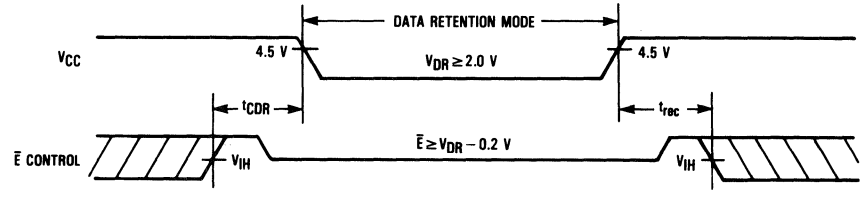


DATA RETENTION CHARACTERISTICS (T_A = −40 to 85°C)

Parameter		Symbol	Min	Typ	Max	Unit
V_{CC} for Data Retention ($\overline{E} \geq V_{CC} - 0.2$ V)		V_{DR}	2.0	–	5.5	V
Data Retention Current ($\overline{E} \geq V_{CC} - 0.2$ V)	V_{CC} = 3.0 V V_{CC} = 5.5 V	I_{CCDR}	– –	– –	50 100	μA
Chip Disable to Data Retention Time		t_{CDR}	0	–	–	ns
Operation Recovery Time		t_{rec}	t_{AVAV}*	–	–	ns

*t_{AVAV} = Read Cycle Time

DATA RETENTION MODE



NOTE: If the V_{IH} of $\overline{E}$ is 2.4 V in operation, I_{SB1} current flows during the period that the V_{CC} voltage is decreasing from 4.5 V to 2.4 V.

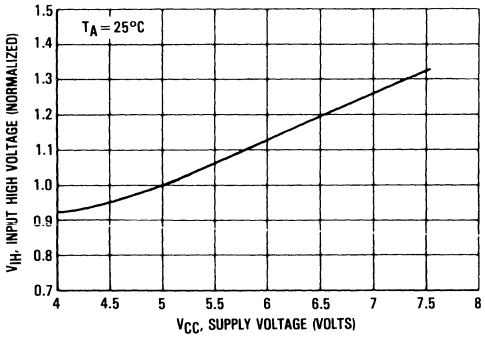


Figure 1. Input High Voltage versus Supply Voltage

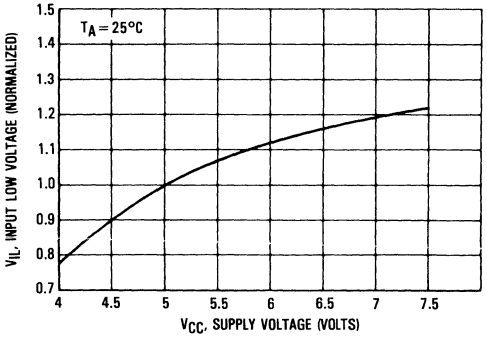


Figure 2. Input Low Voltage versus Supply Voltage

6

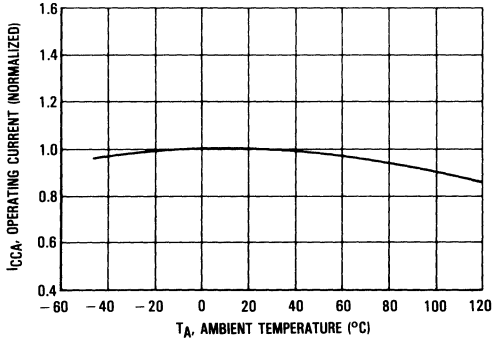


Figure 3. Operating Current versus Ambient Temperature

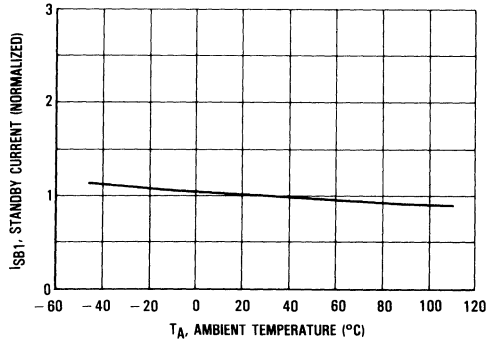


Figure 4. I_{SB1} Standby Current versus Ambient Temperature

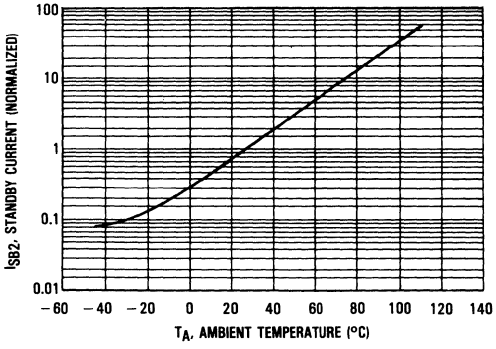


Figure 5. I_{SB2} Standby Current versus Ambient Temperature

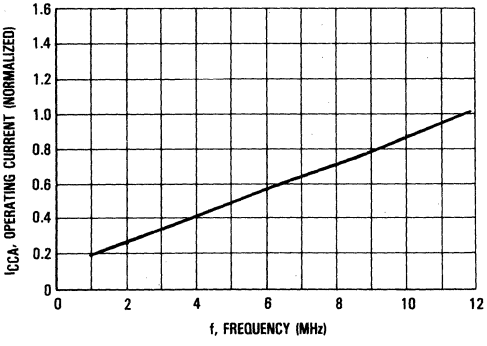


Figure 6. Low Power Operating Current versus Frequency (Read)

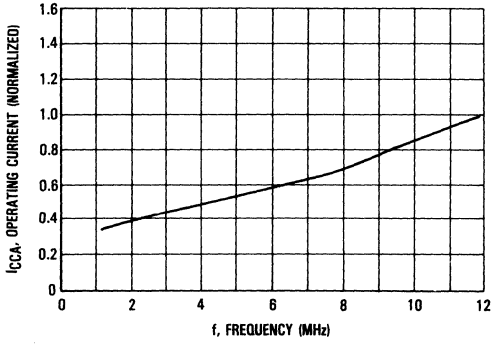


Figure 7. Operating Current versus Frequency (Write)

6

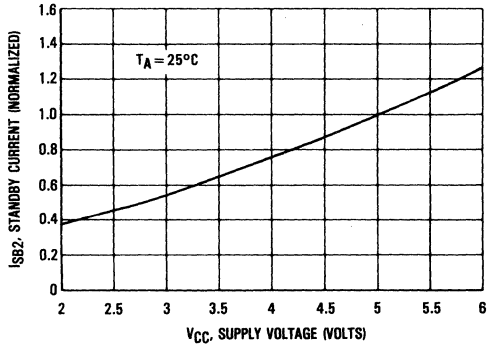


Figure 8. Low Power I_{SB2} Standby Current versus Supply Voltage

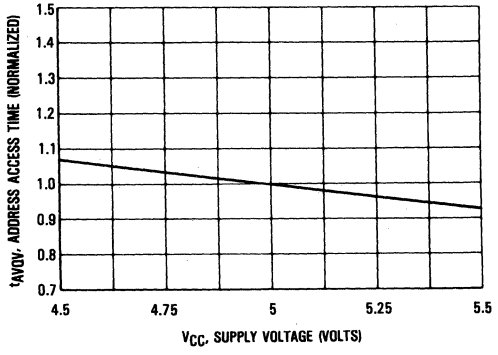


Figure 9. Access Time versus Supply Voltage

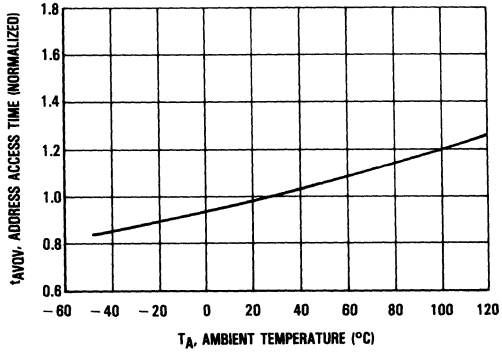
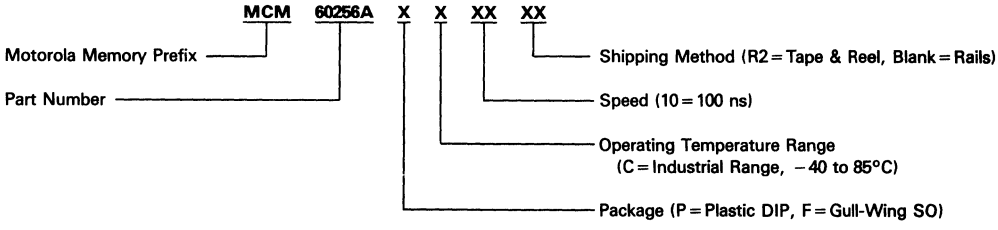


Figure 10. Access Time versus Ambient Temperature

ORDERING INFORMATION
(Order by Full Part Number)



Full Part Number —		
	MCM60256APC10	MCM60L256APC10
	MCM60256AFC10	MCM60L256AFC10
	MCM60256AFC10R2	MCM60L256AFC10R2

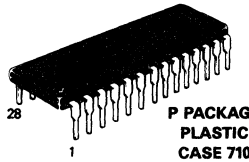
6

MCM60L256A-V

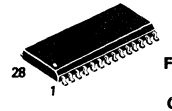
Advance Information

32K x 8 Bit CMOS Static Random Access Memory

Extended Temperature Range: −40 to 105°C



P PACKAGE
PLASTIC
CASE 710



F PACKAGE
SOG
CASE 751H

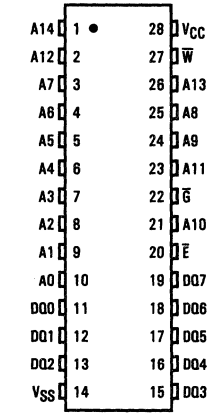
The MCM60L256A-V is a 262,144 bit low-power static random access memory organized as 32,768 words of 8 bits, fabricated using silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides greater reliability. The operating current is 5 mA/MHz (typ) and the cycle time is 100 ns. For long cycle times (>100 ns), the automatic power down (APD) circuitry will temporarily shut down various power consuming circuits, thereby reducing the active power consumption.

Chip enable ($\overline{E}$) controls the power-down feature. It is not a clock but rather a chip control that affects power consumption. When $\overline{E}$ is a logic high, the part is placed in low power standby mode. The maximum standby current is 2 μA (T_A=25°C). Chip enable also controls the data retention mode. Another control feature, output enable ($\overline{G}$) allows access to the memory contents as fast as 50 ns. Thus the MCM60L256A-V is suitable for use in various microprocessor application systems where high speed, low power, and battery backup are required.

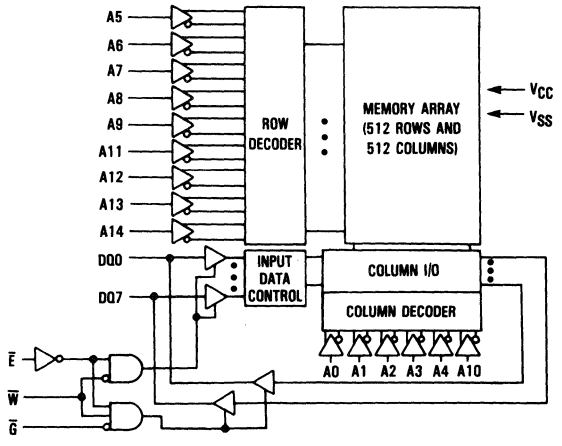
The MCM60L256A-V is offered in a 28 pin, 600 mil plastic dual-in-line package and a 330 mil gull-wing SO package.

- Single 5 V Supply, ±10%
- 32K x 8 Organization
- Fully Static — No Clock or Timing Strobes Necessary
- Low Power Dissipation—27.5 mW/MHz (Typical Active)
- Output Enable and Chip Enable Inputs for More System Design Flexibility and Low Power Standby Mode
- Battery Backup Capability (Maximum Standby Current=2 μA @ 25°C)
- Data Retention Supply Voltage=2.0 V to 5.5 V
- All Inputs and Outputs Are TTL Compatible
- Three State Outputs
- Fast Access Time: MCM60L256A-V10=100 ns (Max)

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A0-A14	Address
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
DQ0-DQ7	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

This document contains information on a new product. Specifications and information herein are subject to change without notice.

TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	Supply Current	I/O Pin
H	X	X	Not Selected	I_{SB}	High Z
L	H	H	Output Disabled	I_{CC}	High Z
L	L	H	Read	I_{CC}	D_{out}
L	X	L	Write	I_{CC}	D_{in}

X = don't care

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.3 to +7.0	V
Voltage to Any Pin with Respect to V_{SS}	V_{in}, V_{out}	−0.5 to V_{CC}+0.5	V
Power Dissipation (T_A = 25°C) PDIP SOG	P_D	1.0 0.6	W
Operating Temperature	T_A	−40 to +105	°C
Storage Temperature	T_{stg}	−55 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

6

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = −40 to 105°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	–	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	−0.3*	–	0.8	V

*V_{IL} (min) = −0.3 V dc; V_{IL} (min) = −3.0 V ac (pulse width ≤50 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	–	<0.01	±1.0	μA
Output Leakage Current ($\overline{E}$ = V_{IH} or $\overline{G}$ = V_{IH} or $\overline{W}$ = V_{IL}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	–	<0.01	±1.0	μA
Operating Current (Read Cycle)	I_{CCA1}				mA
($\overline{E}$ = V_{IL}, $\overline{W}$ = V_{IH}, Other Input = V_{IH}/V_{IL}, I_{out} = 0 mA) t_{AVQV} = 1 μs		–	10	15	
t_{AVQV} = 100 ns		–	–	70	
($\overline{E}$ = 0.2 V, $\overline{W}$ = V_{CC} − 0.2 V, Other Input = V_{CC} − 0.2 V/0.2 V,	I_{CCA2}				
I_{out} = 0 mA) t_{AVQV} = 1 μs		–	5	8	
t_{AVQV} = 100 ns		–	–	60	
Standby Current ($\overline{E}$ = V_{IH})	I_{SB1}	–	–	3.0	mA
Standby Current ($\overline{E}$ ≥ V_{CC} − 0.2 V, V_{CC} = 2.0 to 5.5 V)	I_{SB2}	–	2	100	μA
(T_A = 25°C)		–	–	2	
Output Low Voltage (I_{OL} = 4.0 mA)	V_{OL}	–	–	0.4	V
Output High Voltage (I_{OH} = −1.0 mA)	V_{OH}	2.4	–	–	V

Typical values are referenced to T_A = 25°C and V_{CC} = 5.0 V

CAPACITANCE (f = 1 MHz, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Min	Max	Unit
Input Capacitance (V_{in} = 0 V)	All Inputs Except DQ	C_{in}	–	10	pF
I/O Capacitance ($V_{I/O}$ = 0 V)	DQ	$C_{I/O}$	–	10	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = −40 to 105°C, Unless Otherwise Noted)

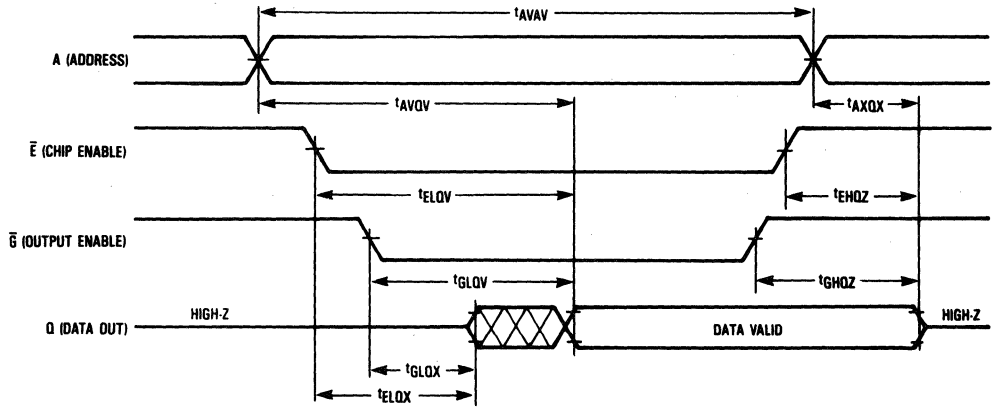
Input Pulse Levels . . . . . 0.6 V, 2.4 V
Input Rise/Fall Time . . . . . 5 ns
Input Timing Measurement Reference Levels . . . . . 1.5 V
Output Timing Measurement Reference Levels . . . . .0.8 and 2.2 V
Output Load . . . . . See Figure 1

READ CYCLE (See Note 1)

Parameter	Symbol	Alt Symbol	Min	Max	Unit	Notes
Read Cycle Time	t_{AVAV}	t_{RC}	100	—	ns	—
Address Access Time	t_{AVQV}	t_{AA}	—	100	ns	—
$\overline{E}$ Access Time	t_{ELQV}	t_{AC}	—	100	ns	—
$\overline{G}$ Access Time	t_{GLQV}	t_{OE}	—	50	ns	—
Output Hold from Address Change	t_{AXQX}	t_{OH}	10	—	ns	—
Chip Enable to Output Low-Z	t_{ELQX}	t_{CLZ}	10	—	ns	2, 3
Output Enable to Output Low-Z	t_{GLQX}	t_{OLZ}	5	—	ns	2, 3
Chip Enable to Output High-Z	t_{EHQZ}	t_{CHZ}	0	35	ns	2, 3
Output Enable to Output High-Z	t_{GHQZ}	t_{OHZ}	0	35	ns	2, 3

NOTES:
1. $\overline{W}$ is high at all times for read cycles.
2. All high-Z and low-Z parameters are considered in a high or low impedance state when the output has made a 100 mV transition from the previous steady state voltage.
3. These parameters are periodically sampled and not 100% tested.

READ CYCLE



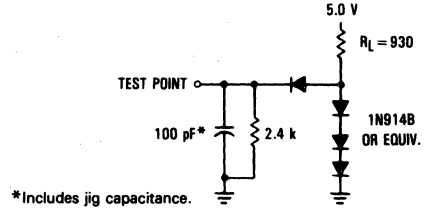


Figure 1. AC Test Load

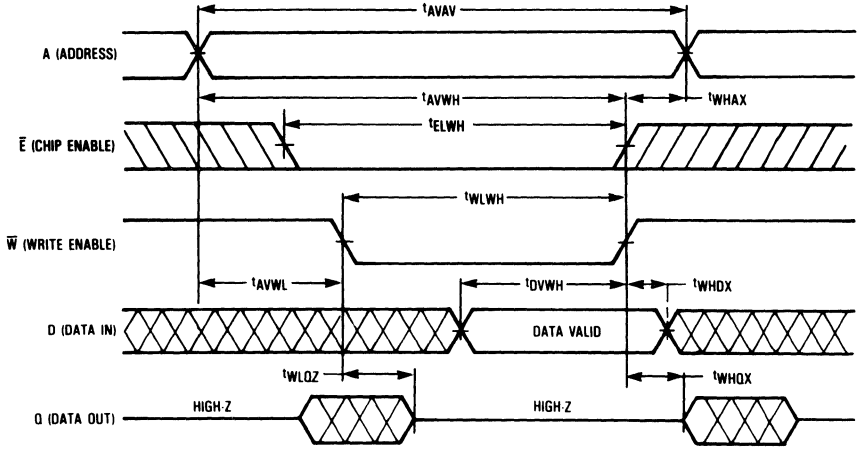
WRITE CYCLE 1 AND 2 (See Note 1)

Parameter	Symbol	Alt Symbol	Min	Max	Unit	Notes
Write Cycle Time	t_{AVAV}	t_{WC}	100	—	ns	—
Address Setup Time	t_{AVWL}/t_{AVEL}	t_{AS}	0	—	ns	—
Address Valid to End of Write	t_{AVWH}/t_{AVEH}	t_{AW}	80	—	ns	—
Write Pulse Width	t_{WLWH}	t_{WP}	60	—	ns	2
Data Valid to End of Write	t_{DVWH}/t_{DVEH}	t_{DW}	35	—	ns	—
Data Hold Time	t_{WHDX}/t_{EHDX}	t_{DH}	0	—	ns	—
Write Low to Output in High-Z	t_{WLQZ}	t_{WHZ}	0	30	ns	3, 4
Write High to Output Low-Z	t_{WHQX}	t_{WLZ}	10	—	ns	3, 4
Write Recovery Time	t_{WHAX}/t_{EHAX}	t_{WR}	0	—	ns	5
Chip Enable to End of Write	t_{ELWH}/t_{ELEH}	t_{CW}	80	—	ns	—

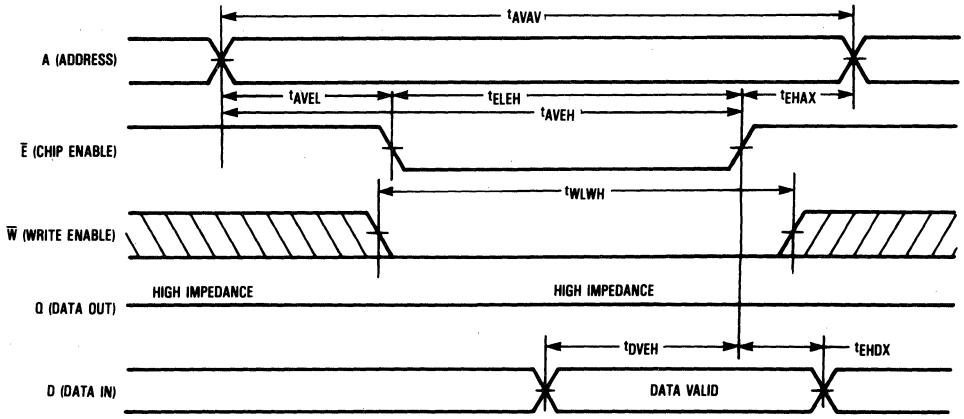
NOTES:
1. Outputs are in high impedance state if $\overline{G}$ is high during Write Cycle.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{E}$ and a low $\overline{W}$. If $\overline{W}$ goes low prior to $\overline{E}$ low then outputs will remain in a high impedance state.
3. All high-Z and low-Z parameters are considered in a high or low impedance state when the outputs have made a 100 mV transition from the previous steady state voltage.
4. These parameters are periodically sampled and not 100% tested.
5. t_{WR} is measured from the earlier of $\overline{E}$ or $\overline{W}$ going high to the end of write cycle.

6

WRITE CYCLE 1 ($\overline{W}$ CONTROLLED)



WRITE CYCLE 2 ($\overline{E}$ Controlled)

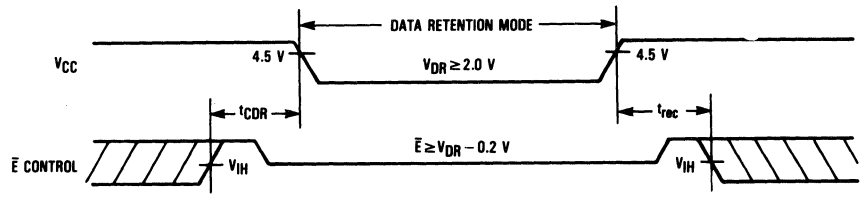


DATA RETENTION CHARACTERISTICS (T_A = −40 to 105°C)

Parameter		Symbol	Min	Typ	Max	Unit
V_{CC} for Data Retention ($\overline{E} \geq V_{CC} - 0.2$ V)		V_{DR}	2.0	—	5.5	V
Data Retention Current ($\overline{E} \geq V_{CC} - 0.2$ V)	V_{CC} = 3.0 V	I_{CCDR}	—	—	50	μA
	V_{CC} = 5.5 V		—	—	100	
Chip Disable to Data Retention Time		t_{CDR}	0	—	—	ns
Operation Recovery Time		t_{rec}	t_{AVAV}*	—	—	ns

*t_{AVAV} = Read Cycle Time

DATA RETENTION MODE



NOTE: If the V_{IH} of $\overline{E}$ is 2.4 V in operation, I_{SB1} current flows during the period that the V_{CC} voltage is decreasing from 4.5 V to 2.4 V.

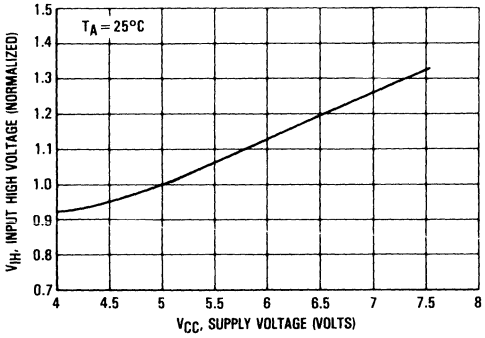


Figure 1. Input High Voltage versus Supply Voltage

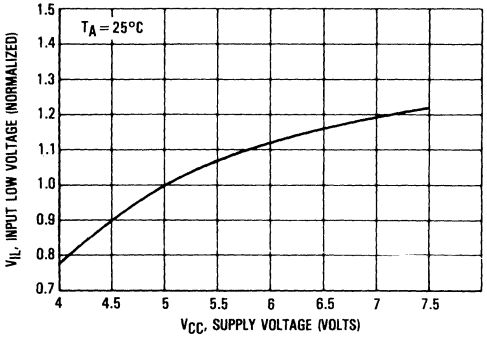


Figure 2. Input Low Voltage versus Supply Voltage

6

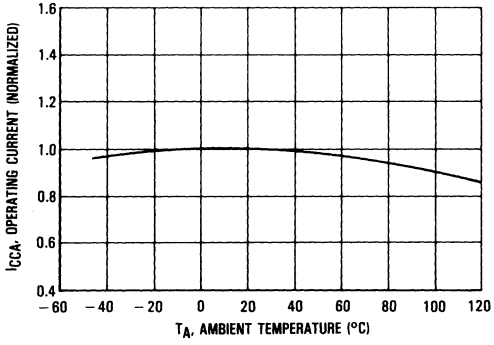


Figure 3. Operating Current versus Ambient Temperature

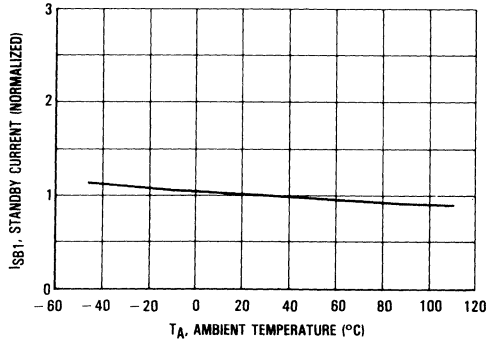


Figure 4. I_{SB1} Standby Current versus Ambient Temperature

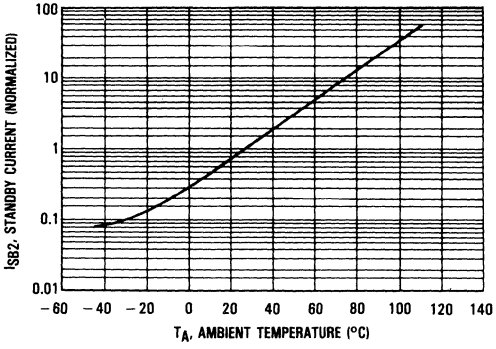


Figure 5. I_{SB2} Standby Current versus Ambient Temperature

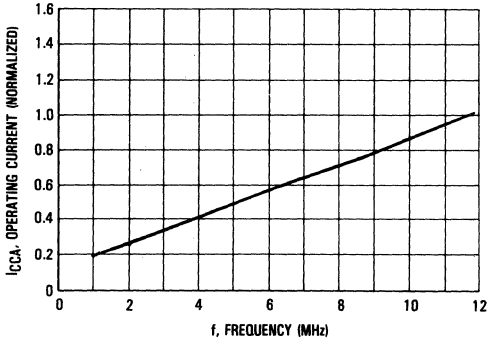


Figure 6. Low Power Operating Current versus Frequency (Read)

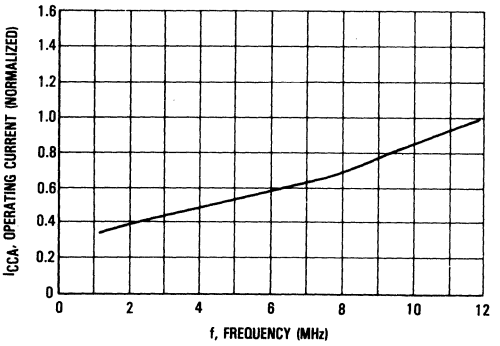


Figure 7. Operating Current versus Frequency (Write)

6

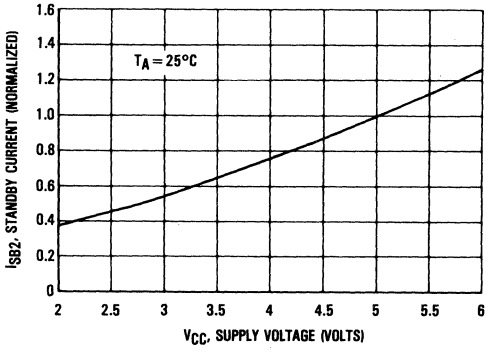


Figure 8. Low Power I_{SB2} Standby Current versus Supply Voltage

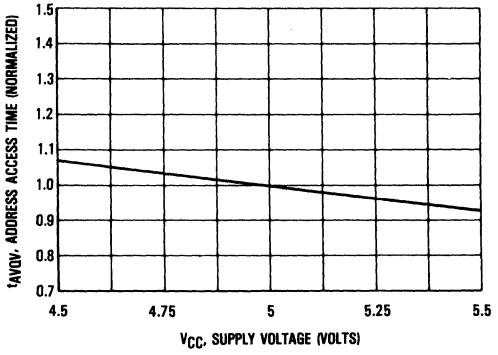


Figure 9. Access Time versus Supply Voltage

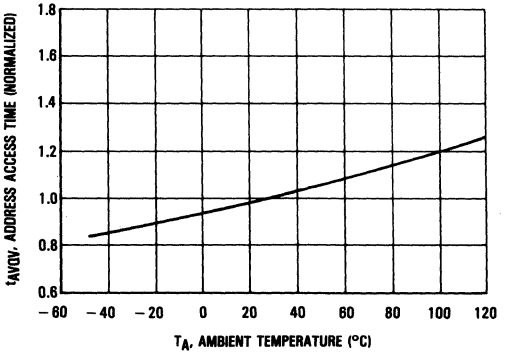
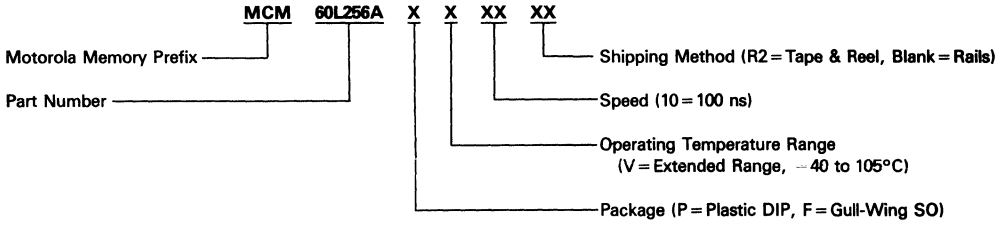


Figure 10. Access Time versus Ambient Temperature

ORDERING INFORMATION
(Order by Full Part Number)



Full Part Number—MCM60L256APV10
MCM60L256AFV10
MCM60L256AFV10R2

6

CMOS Fast Static RAMs

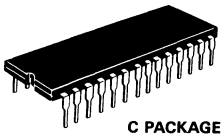
7

FAST STATIC RAMs (70 ns or Faster)

Density	Organization	Motorola Part Number	Pin Count	Packaging (Package Width in mils)	Address/ Cycle Time (ns Max)	Operating Current (mA max)	Technology
16K	2Kx8	MCM2018A	24	300 PDIP	45/55	135	NMOS
	4Kx4	MCM6268	20	300 PDIP	20/25/35/45/55	110/110/110/80/80	HCMOS
		MCM6269	20	300 PDIP	20/25/35	110	HCMOS
		MCM6270	24/22	300 SOJ/PDIP	20/25/35	110	HCMOS
64K	8Kx8	MCM6264	28	300/400 SOJ/300 PDIP	35/45/55	100/90/80	HCMOS
		MCM6264D	28	300/400 SOJ/300 PDIP	20/25	115/110	HCMOS
		MCM6264	28	300 PDIP/SOJ	15	140	HCMOS
		MCM6264C	28	300/400 SOJ/300 PDIP	35/45/55	100/90/80	HCMOS
		MCM6264D-C	28	300/400 SOJ/300 PDIP	25/30	115/110	HCMOS
		MCM6264C	28	300 PDIP/SOJ	20	140	HCMOS
	8Kx9	MCM6265	28	300 SOJ/PDIP	15/20/25	140/130/120	HCMOS
	16Kx4	MCM6288	22	300 PDIP	12/15/20/25/35	150/140/120/120/110	HCMOS
		MCM6290	24	300 SOJ/PDIP	12/15/20/25/35	150/140/120/120/110	HCMOS
	64Kx1	MCM6287	24/22	300 SOJ/PDIP	12/15/20/25/35	150/140/130/120/110	HCMOS
256K	32Kx8	MCM6206	28	400 SOJ/600 PDIP	30/35/45	130/125/115	HCMOS
		MCM6206	28	300 SOJ/PDIP	17/20/25/35	155/150/140/135	HCMOS
		MCM6206C	28	300 SOJ/PDIP	25/35/45	140/135/130	HCMOS
		MCM6706	28	300 SOJ	10/12/15	180/170/160	BiCMOS
	32Kx9	MCM6205	32	300 SOJ/PDIP	17/20/25/35	155/150/140/135	HCMOS
		MCM6205C	32	300 SOJ/PDIP	25/35/45	140/135/130	HCMOS
	64Kx4	MCM6208	24	300 SOJ/PDIP	15/20/25/35	155/145/135/125	HCMOS
		MCM6708	24	300 SOJ	10/12/15	180/170/160	BiCMOS
		MCM6209	28	300 SOJ/PDIP	15/20/25/35	155/145/135/125	HCMOS
		MCM6709	28	300 SOJ	10/12/15	180/170/160	BiCMOS
	256Kx1	MCM6207	24	300 SOJ/PDIP	15/20/25	150/140/130	HCMOS
1M	128Kx8	MCM6226	32	400 SOJ/PDIP	25/30	150/140	HCMOS
	256Kx4	MCM6228	28	400 SOJ/PDIP	25/30	145/135	HCMOS

MCM6164
MCM61L64

8K x 8 Bit Fast Static Random Access Memory



C PACKAGE
CERAMIC
CASE 733

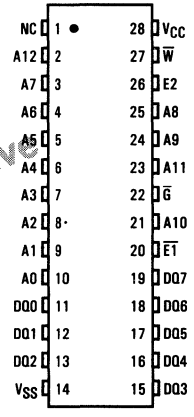
The MCM6164/MCM61L64 is a 65,536 bit static random access memory organized as 8192 words of 8 bits, fabricated using Motorola's second-generation high-performance silicon-gate CMOS (HCMOS III) technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides greater reliability.

The chip enable pins ($\overline{E1}$ and E2) are not clocks. Either pin, when asserted false, causes the part to enter a low power standby mode. The part will remain in standby mode until both pins are asserted true again. The availability of active high and active low chip enable pins provides more system design flexibility than single chip enable devices.

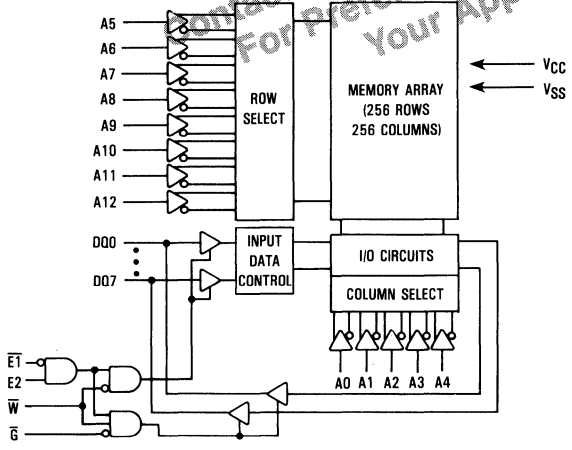
The MCM6164/MCM61L64 is available in a 600 mil, 28 pin ceramic dual-in-line package, with JEDEC standard pinout.

- Single 5 V Supply, ±10%
- 8K x 8 Organization
- Fully Static — No Clock or Timing Strobes Necessary
- Fast Access Time — 45, 55 ns (Maximum)
- Low Power Dissipation — 495, 440 mW (Maximum, Active)
- Low Power/Data Retention Version (MCM61L64)
- Fully TTL Compatible
- Three State Data Outputs
- Also Available in Industrial Temperature Range (−40 to 85°C) as MCM6164C

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A0-A12	Address
$\overline{W}$	Write Enable
$\overline{E1}$, E2	Chip Enable
$\overline{G}$	Output Enable
DQ0-DQ7	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground
NC	No Connection

7

TRUTH TABLE

$\overline{E1}$	E2	$\overline{G}$	$\overline{W}$	Mode	Supply Current	I/O Pin
H	X	X	X	Not Selected	I_{SB}	High Z
X	L	X	X	Not Selected	I_{SB}	High Z
L	H	H	H	Output Disabled	I_{CC}	High Z
L	H	L	H	Read	I_{CC}	D_{out}
L	H	X	L	Write	I_{CC}	D_{in}

X = don't care

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC}+0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation (T_A = 25°C)	P_D	1.0	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

7

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	–	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	−0.3*	–	0.8	V

*V_{IL} (min) = −0.3 V dc, V_{IL} (min) = −3.0 V (pulse width ≤20 ns)

DC CHARACTERISTICS

Characteristic		Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})		$I_{lkg(I)}$	–	<0.01	±1.0	μA
Output Leakage Current ($\overline{E1}$ = V_{IH}, E2 = V_{IL}, or $\overline{G}$ = V_{IH}, V_{out} = 0 to V_{CC})		$I_{lkg(O)}$	–	<0.01	±1.0	μA
Power Supply Current ($\overline{E1}$ = V_{IL}, E2 = V_{IH}, I_{out} = 0)	t_{AVAV} = 45 ns	I_{CC}	–	50	90	mA
	t_{AVAV} = 55 ns		–	40	80	
Standby Current ($\overline{E1}$ = V_{IH} or E2 = V_{IL})		I_{SB1}	–	1.3	3.0	mA
Standby Current ($\overline{E1}$ ≥ V_{CC} −0.2 V or E2 ≤ 0.2 V)	MCM6164	I_{SB2}	–	–	1.0	mA
	MCM61L64		–	5	50	μA
Output Low Voltage (I_{OL} = 8.0 mA)		V_{OL}	–	0.15	0.4	V
Output High Voltage (I_{OH} = −4.0 mA)		V_{OH}	2.4	3.0	–	V

Typical values are referenced to T_A = 25°C and V_{CC} = 5.0 V

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Max	Unit
Input Capacitance	All Inputs Except DQ	C_{in}	6	pF
Input/Output Capacitance	DQ	$C_{I/O}$	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

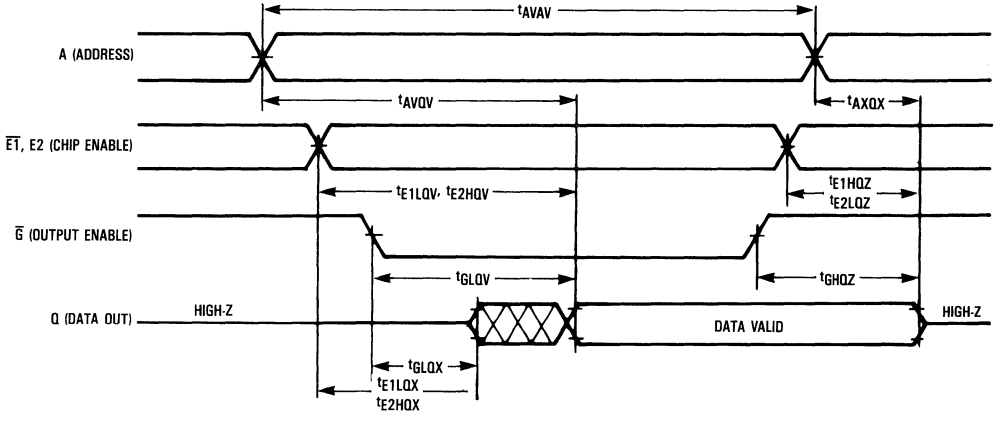
Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . .0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns

Output Timing Measurement Reference Level . . . 0.8 V and 2.0 V
Output Load . . . . . Figure 1

READ CYCLE (See Note 1)

Characteristic	Symbol	Alt Symbol	MCM6164-45 MCM61L64-45		MCM6164-55 MCM61L64-55		Unit	Notes
			Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	45	–	55	–	ns	–
Address Cycle Time	t_{AVQV}	t_{AA}	–	45	–	55	ns	–
$\overline{E1}$ Access Time	t_{E1LQV}	t_{AC1}	–	45	–	55	ns	–
E2 Access Time	t_{E2HQV}	t_{AC2}	–	45	–	55	ns	–
$\overline{G}$ Access Time	t_{GLQV}	t_{OE}	–	20	–	25	ns	–
Output Hold from Address Change	t_{AXQX}	t_{OH}	5	–	5	–	ns	–
Chip Enable to Output Low-Z	t_{E1LQX}, t_{E2HQX}	t_{CLZ}	5	–	5	–	ns	2, 3
Output Enable to Output Low-Z	t_{GLQX}	t_{OLZ}	0	–	0	–	ns	2, 3
Chip Enable to Output High-Z	t_{E1HQZ}, t_{E2LQZ}	t_{CHZ}	0	20	0	20	ns	2, 3
Output Enable to Output High-Z	t_{GHQZ}	t_{OHZ}	0	20	0	20	ns	2, 3

NOTES:
1. $\overline{W}$ is high at all times for read cycles.
2. All high-Z and low-Z parameters are considered in a high or low impedance state when the output has made a 500 mV transition from the previous steady state voltage.
3. Periodically sampled rather than 100% tested.



TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

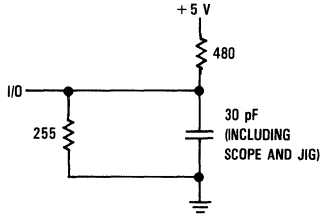


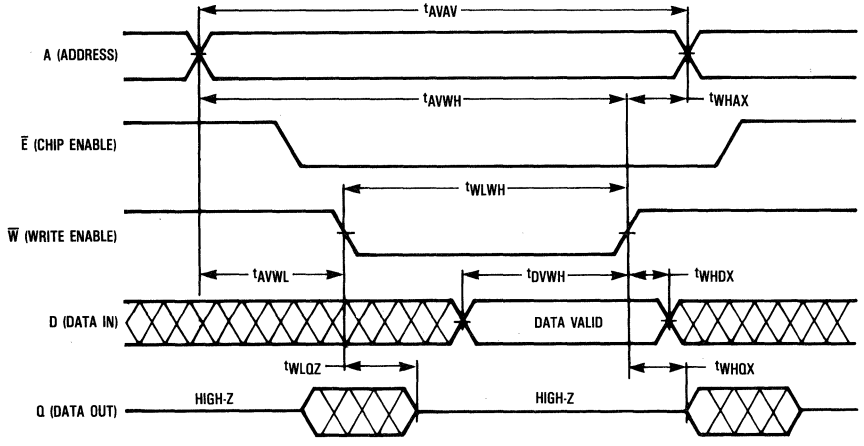
Figure 1. Test Load

WRITE CYCLE 1 ($\overline{W}$ CONTROLLED) (See Note 1)

Characteristic	Symbol	Alt Symbol	MCM6164-45 MCM61L64-45		MCM6164-55 MCM61L64-55		Unit	Notes
			Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	45	–	55	–	ns	–
Address Setup Time	t_{AVWL}	t_{AS}	0	–	0	–	ns	–
Address Valid to End of Write	t_{AVWH}	t_{AW}	40	–	50	–	ns	–
Write Pulse Width	t_{WLWH}	t_{WP}	25	–	30	–	ns	2
Data Valid to End of Write	t_{DVWH}	t_{DW}	20	–	25	–	ns	–
Data Hold Time	t_{WHDX}	t_{DH}	0	–	0	–	ns	3
Write Low to Output in High-Z	t_{WLQZ}	t_{WHZ}	0	20	0	20	ns	4, 5
Write High to Output Low-Z	t_{WHQX}	t_{OW}	5	–	5	–	ns	4, 5
Write Recovery Time	t_{WHAX}	t_{WR}	0	–	0	–	ns	–

NOTES:
1. A write cycle starts at the latest transition of a low $\overline{E1}$, low $\overline{W}$ or high E2. A write cycle ends at the earliest transition of a high $\overline{E1}$, high $\overline{W}$ or low E2.
2. If $\overline{W}$ goes low coincident with or prior to $\overline{E1}$ low or E2 high then the outputs will remain in a high impedance state.
3. During this time the output pins may be in the output state. Signals of opposite phase to the outputs must not be applied at this time.
4. All high-Z and low-Z parameters are considered in a high or low impedance state when the output has made a 500 mV transition from the previous steady state voltage.
5. Periodically sampled rather than 100% tested.

7



TYPICAL CHARACTERISTICS

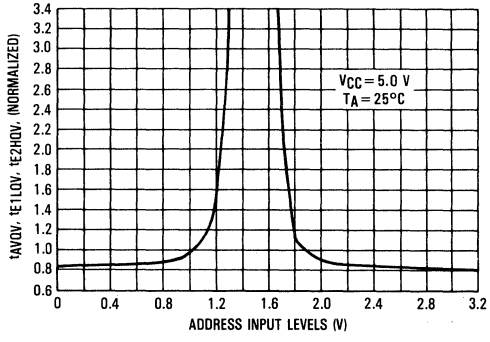
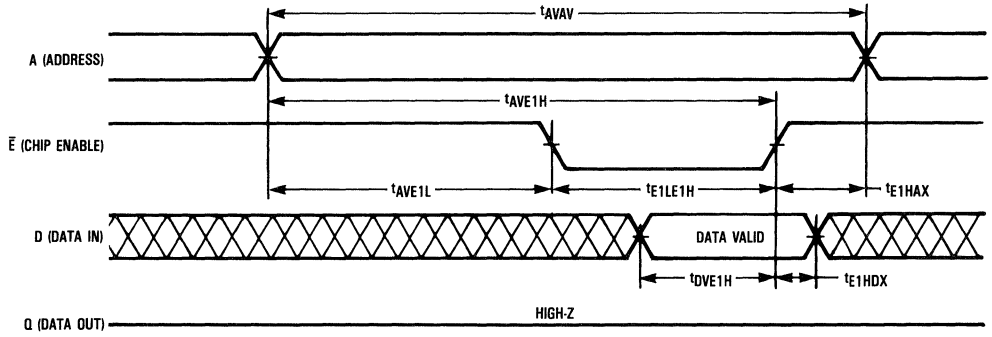


Figure 2. Access Time Versus Address Input Levels

WRITE CYCLE 2 (ENABLE CONTROLLED) (See Notes 1 and 2)

Characteristic	Symbol	Alt Symbol	MCM6164-45 MCM61L64-45		MCM6164-55 MCM61L64-55		Unit	Notes
			Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	45	–	55	–	ns	–
Address Setup Time	t_{AVE1L}	t_{AS}	0	–	0	–	ns	–
Address Valid to End of Write	t_{AVE1H}	t_{AW}	40	–	50	–	ns	–
Chip Enable to End of Write	t_{E1LE1H}	t_{CW}	40	–	50	–	ns	3
Data Valid to End of Write	t_{DVE1H}	t_{DW}	20	–	25	–	ns	–
Data Hold Time	t_{E1HDX}	t_{DH}	0	–	0	–	ns	4
Write Recovery Time	t_{E1HAX}	t_{WR}	0	–	0	–	ns	–

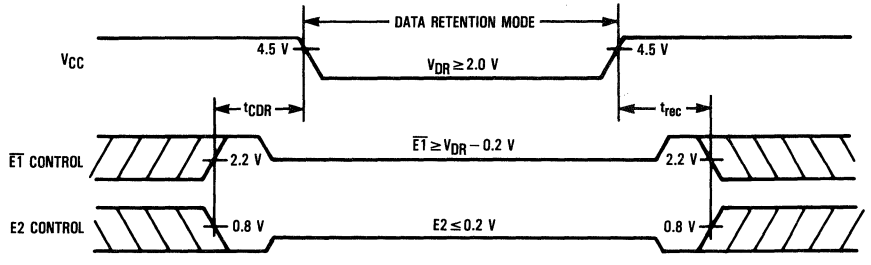
NOTES:
1. A write cycle starts at the latest transition of a low $\overline{E1}$, low $\overline{W}$ or high E2. A write cycle ends at the earliest transition of a high $\overline{E1}$, high $\overline{W}$ or low E2.
2. $\overline{E1}$ and E2 timings are identical when E2 signals are inverted.
3. If $\overline{W}$ goes low coincident with or prior to $\overline{E1}$ low or E2 high then the outputs will remain in a high impedance state.
4. During this time the output pins may be in the output state. Signals of opposite phase to the outputs must not be applied at this time.



LOW V_{CC} DATA RETENTION CHARACTERISTICS (T_A = 0 to +70°C) (MCM61L64 Only)

Characteristic	Symbol	Min	Typ	Max	Unit
V_{CC} for Data Retention ($\overline{E1} \geq V_{CC} - 0.2$ V or E2 ≤ 0.2 V, $V_{in} \geq V_{CC} - 0.2$ V or $V_{in} \leq 0.2$ V)	V_{DR}	2.0	1.0	7.0	V
Data Retention Current (V_{CC} = 3.0 V, $\overline{E1} \geq 2.8$ V or E2 ≤ 0.2 V, $V_{in} \geq 2.8$ V or $V_{in} \leq 0.2$ V)	I_{CCDR}	–	10	30	μA
Chip Disable to Data Retention Time (see waveform below)	t_{CDR}	0	–	–	ns
Operation Recovery Time (see waveform below)	t_{rec}	t_{AVAV}*	–	–	ns

*t_{AVAV} = Read Cycle Time



TYPICAL CHARACTERISTICS
(Continued)

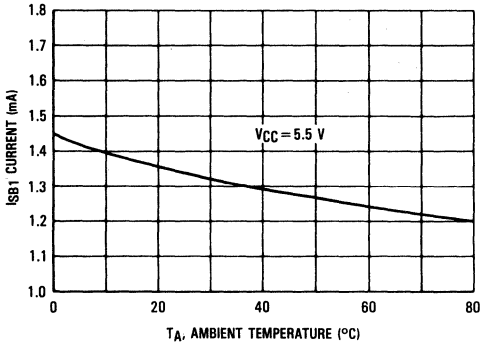


Figure 3. Standby Current Versus Temperature

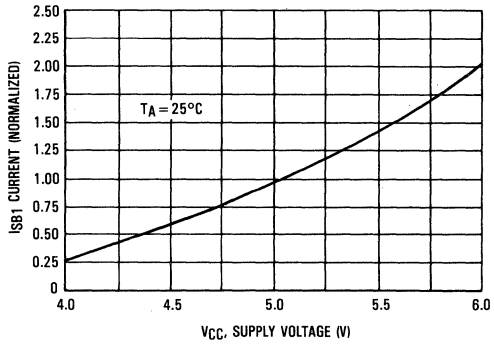


Figure 4. Standby Current Versus Supply Voltage

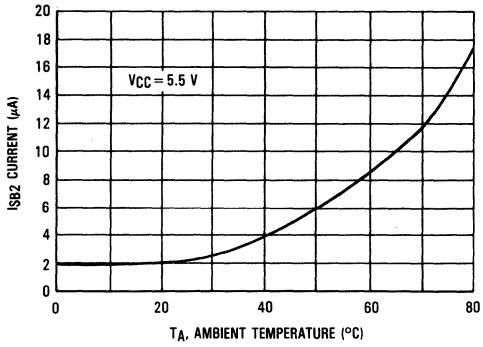


Figure 5. Standby Current Versus Temperature

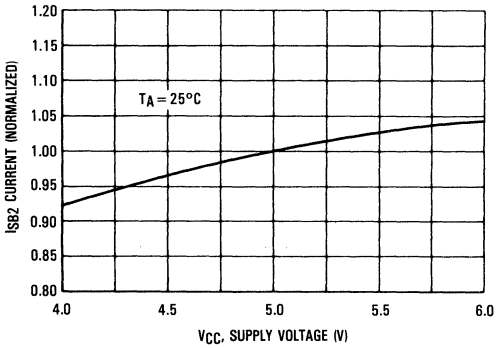


Figure 6. Standby Current Versus Supply Voltage

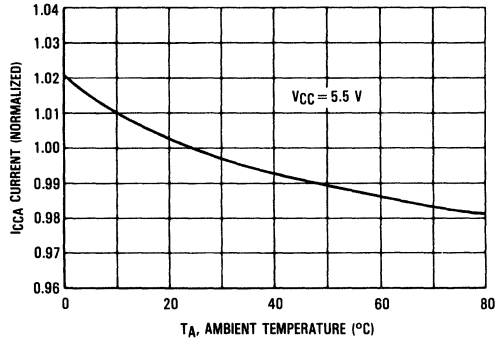


Figure 7. Supply Current Versus Temperature

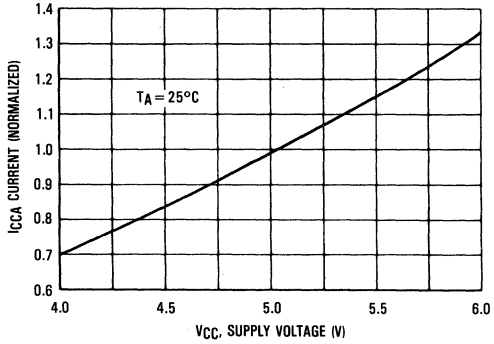


Figure 8. Supply Current Versus Supply Voltage

TYPICAL CHARACTERISTICS
(Continued)

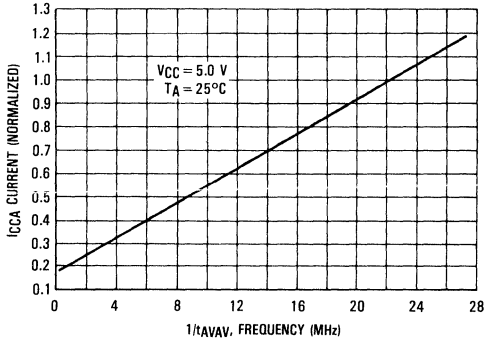


Figure 9. Supply Current Versus Frequency

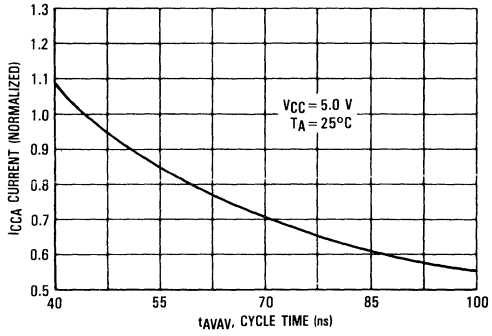


Figure 10. Supply Current Versus Cycle Time

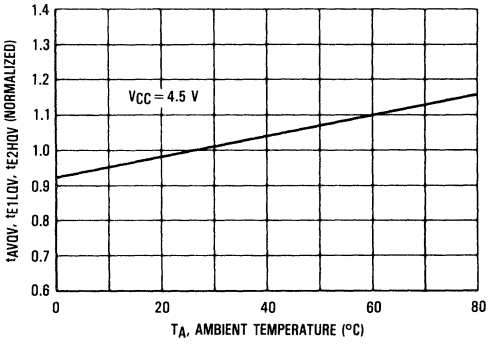


Figure 11. Access Time Versus Temperature

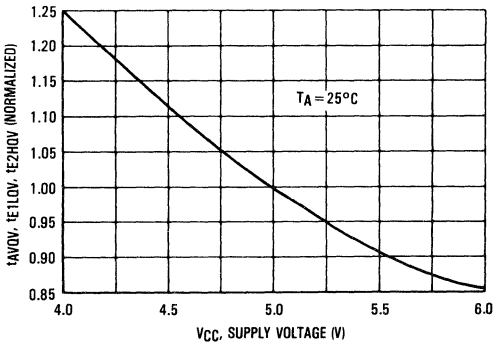


Figure 12. Access Time Versus Supply Voltage

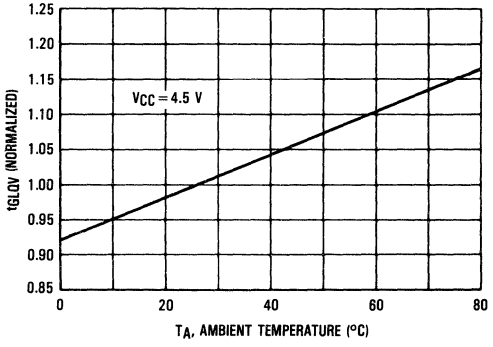


Figure 13. Access Time Versus Temperature

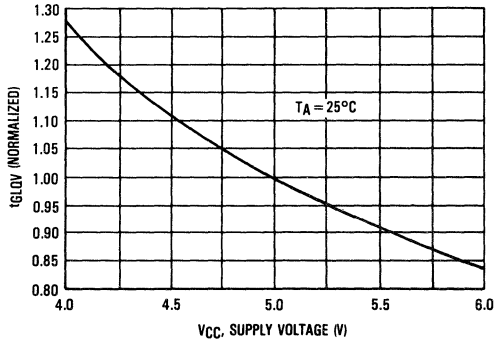
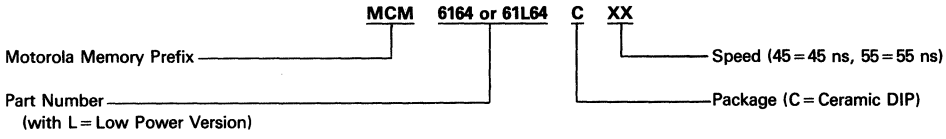


Figure 14. Access Time Versus Supply Voltage

ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers — MCM6164C45 MCM6164C55 MCM61L64C45 MCM61L64C55

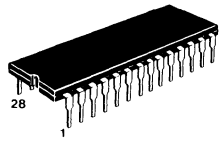
7

MCM6164C

Advance Information

8K x 8 Bit Fast Static Random Access Memory

Industrial Temperature Range: – 40 to 85°C



C PACKAGE
CERAMIC
CASE 733

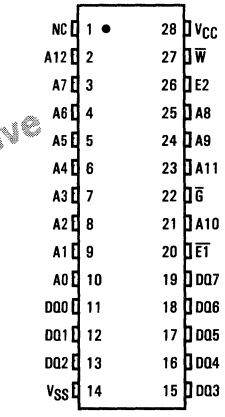
The MCM6164C is a 65,536 bit static random access memory organized as 8192 words of 8 bits, fabricated using Motorola's second-generation high-performance silicon-gate CMOS (HCMOS III) technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides greater reliability. With its operating temperature range of –40°C to +85°C and hermetic package, the MCM6164C is ideally suited for harsh industrial type environments.

The chip enable pins ($\overline{E1}$ and E2) are not clocks. Either pin, when asserted false, causes the part to enter a low power standby mode. The part will remain in standby mode until both pins are asserted true again. The availability of active high and active low chip enable pins provides more system design flexibility than single chip enable devices.

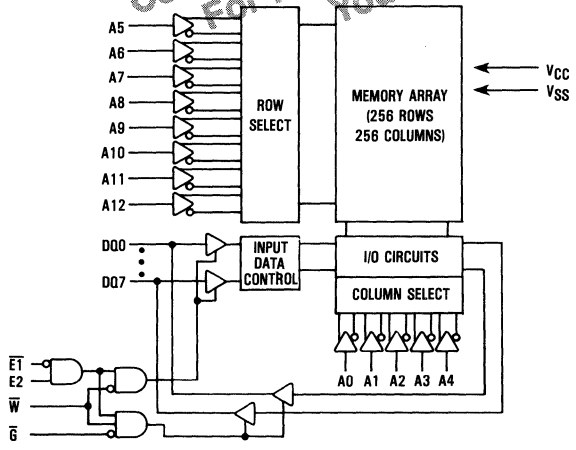
The MCM6164C is available in a 600 mil, 28 pin ceramic dual-in-line package with the JEDEC standard pinout.

- Single 5 V Supply, ±10%
- 8K x 8 Organization
- Fully Static—No Clock or Timing Strobes Necessary
- Fast Access Time—55 or 70 ns (Maximum)
- Low Power Dissipation—440 or 385 mW (Maximum, Active)
- Fully TTL Compatible
- Three State Data Outputs
- Also Available in Commercial Temperature Range (0 to 70°C) as MCM6164/MCM61L64

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A0-A12	Address
$\overline{W}$	Write Enable
$\overline{E1}$, E2	Chip Enable
$\overline{G}$	Output Enable
DQ0-DQ7	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground
NC	No Connection

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This document contains information on a new product. Specifications and information herein are subject to change without notice.

TRUTH TABLE

$\overline{E1}$	E2	$\overline{G}$	$\overline{W}$	Mode	Supply Current	I/O Pin
H	X	X	X	Not Selected	I_{SB}	High Z
X	L	X	X	Not Selected	I_{SB}	High Z
L	H	H	H	Output Disabled	I_{CC}	High Z
L	H	L	H	Read	I_{CC}	D_{out}
L	H	X	L	Write	I_{CC}	D_{in}

X = don't care

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC}+0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation (T_A = 25°C)	P_D	1.0	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	−40 to +85	°C
Storage Temperature	T_{stg}	−65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

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DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = −40 to 85°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	−0.3*	—	0.8	V

*V_{IL} (min) = −0.3 V dc, V_{IL} (min) = −3.0 V (pulse width ≤20 ns)

DC CHARACTERISTICS

Characteristic		Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})		$I_{lkg(I)}$	—	<0.01	±2.0	μA
Output Leakage Current ($\overline{E1}$ = V_{IH}, E2 = V_{IL}, or $\overline{G}$ = V_{IH}, V_{out} = 0 to V_{CC})		$I_{lkg(O)}$	—	<0.01	±2.0	μA
Power Supply Current ($\overline{E1}$ = V_{IL}, E2 = V_{IH}, I_{out} = 0)	t_{AVAV} = 55 ns	I_{CC}	—	40	80	mA
	t_{AVAV} = 70 ns		—	35	70	
Standby Current ($\overline{E1}$ = V_{IH} or E2 = V_{IL})		I_{SB1}	—	1.3	3.0	mA
Standby Current ($\overline{E1}$ ≥ V_{CC} − 0.2 V or E2 ≤ 0.2 V)		I_{SB2}	—	0.005	1.0	mA
Output Low Voltage (I_{OL} = 8.0 mA)		V_{OL}	—	0.15	0.4	V
Output High Voltage (I_{OH} = −4.0 mA)		V_{OH}	2.4	3.0	—	V

Typical values are referenced to T_A = 25°C and V_{CC} = 5.0 V

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Max	Unit
Input Capacitance	All Inputs Except DQ	C_{in}	6	pF
Input/Output Capacitance	DQ	$C_{I/O}$	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ±10%, T_A = −40 to +85°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns
Output Timing Measurement Reference Level . . . 0.8 V and 2.0 V
Output Load . . . . . Figure 1

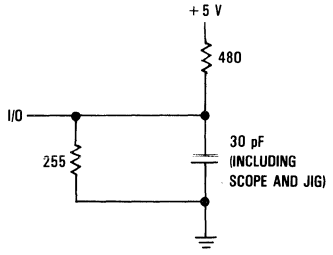
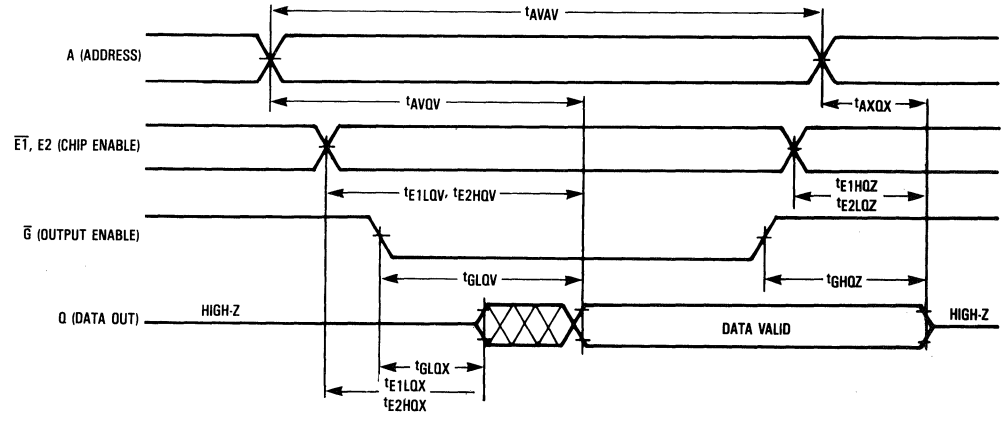


Figure 1. Test Load

READ CYCLE (See Note 1)

Parameter	Symbol	Alt Symbol	MCM6164CC55		MCM6164CC70		Notes
			Min	Max	Min	Max	
Read Cycle Time	t_{AVAV}	t_{RC}	55	–	70	–	–
Address Cycle Time	t_{AVQV}	t_{AA}	–	55	–	70	–
$\overline{E1}$ Access Time	t_{E1LQV}	t_{AC1}	–	55	–	70	–
E2 Access Time	t_{E2HQV}	t_{AC2}	–	55	–	70	–
$\overline{G}$ Access Time	t_{GLQV}	t_{OE}	–	25	–	30	–
Output Hold from Address Change	t_{AXQX}	t_{OH}	5	–	5	–	–
Chip Enable to Output Low-Z	t_{E1LQX}, t_{E2HQX}	t_{CLZ}	5	–	5	–	2, 3
Output Enable to Output Low-Z	t_{GLQX}	t_{OLZ}	0	–	0	–	2, 3
Chip Enable to Output High-Z	t_{E1HQZ}, t_{E2LQZ}	t_{CHZ}	0	20	0	20	2, 3
Output Enable to Output High-Z	t_{GHQZ}	t_{OHZ}	0	20	0	20	2, 3

NOTES:
1. $\overline{W}$ is high at all times for read cycles.
2. All high-Z and low-Z parameters are considered in a high or low impedance state when the output has made a 500 mV transition from the previous steady state voltage.
3. Periodically sampled rather than 100% tested.

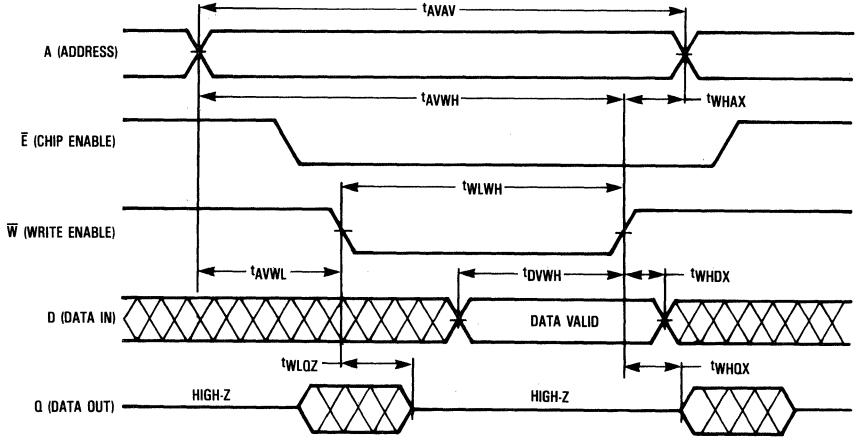


WRITE CYCLE 1 ($\overline{W}$ CONTROLLED) (See Note 1)

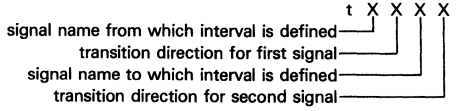
Parameter	Symbol	Alt Symbol	MCM6164CC55		MCM6164CC70		Notes
			Min	Max	Min	Max	
Write Cycle Time	t_{AVAV}	t_{WC}	55	–	70	–	–
Address Setup Time	t_{AVWL}	t_{AS}	0	–	0	–	–
Address Valid to End of Write	t_{AVWH}	t_{AW}	50	–	60	–	–
Write Pulse Width	t_{WLWH}	t_{WP}	30	–	40	–	2
Data Valid to End of Write	t_{DVWH}	t_{DW}	25	–	30	–	–
Data Hold Time	t_{WHDX}	t_{DH}	0	–	0	–	3
Write Low to Output in High-Z	t_{WLQZ}	t_{WHZ}	0	20	0	20	4, 5
Write High to Output Low-Z	t_{WHQX}	t_{OW}	5	–	5	–	4, 5
Write Recovery Time	t_{WHAX}	t_{WR}	0	–	0	–	–

NOTES:
1. A write cycle starts at the latest transition of a low $\overline{E1}$, low $\overline{W}$ or high E2. A write cycle ends at the earliest transition of a high $\overline{E1}$, high $\overline{W}$ or low E2.
2. If $\overline{W}$ goes low coincident with or prior to $\overline{E1}$ low or E2 high then the outputs will remain in a high impedance state.
3. During this time the output pins may be in the output state. Signals of opposite phase to the outputs must not be applied at this time.
4. All high-Z and low-Z parameters are considered in a high or low impedance state when the output has made a 500 mV transition from the previous steady state voltage.
5. Periodically sampled rather than 100% tested.

7



TIMING PARAMETER ABBREVIATIONS



The transition definitions used in this data sheet are:
- H = transition to high
- L = transition to low
- V = transition to valid
- X = transition to invalid or don't care
- Z = transition to off (high impedance)

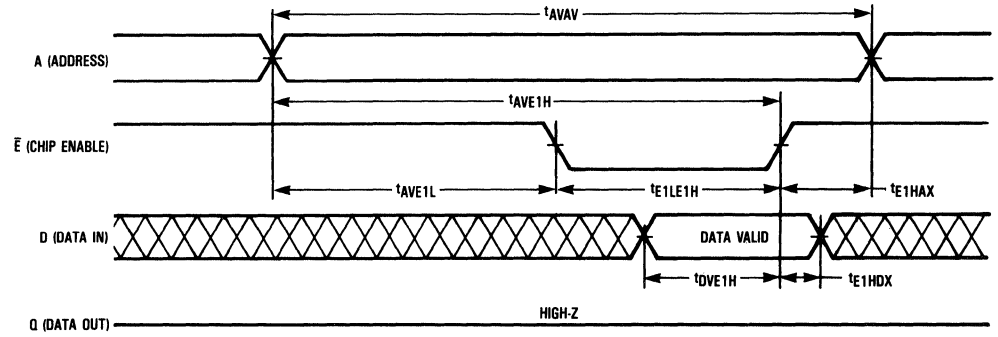
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

WRITE CYCLE 2 (ENABLE CONTROLLED) (See Notes 1 and 2)

Parameter	Symbol	Alt Symbol	MCM6164CC55		MCM6164CC70		Notes
			Min	Max	Min	Max	
Write Cycle Time	t_{AVAV}	t_{WC}	55	–	70	–	–
Address Setup Time	t_{AVE1L}	t_{AS}	0	–	0	–	–
Address Valid to End of Write	t_{AVE1H}	t_{AW}	50	–	60	–	–
Chip Enable to End of Write	t_{E1LE1H}	t_{CW}	50	–	60	–	3
Data Valid to End of Write	t_{DVE1H}	t_{DW}	25	–	30	–	–
Data Hold Time	t_{E1HDX}	t_{DH}	0	–	0	–	4
Write Recovery Time	t_{E1HAX}	t_{WR}	0	–	0	–	

NOTES:
1. A write cycle starts at the latest transition of a low $\overline{E1}$, low $\overline{W}$ or high E2. A write cycle ends at the earliest transition of a high $\overline{E1}$, high $\overline{W}$ or low E2.
2. $\overline{E1}$ and E2 timings are identical when E2 signals are inverted.
3. If $\overline{W}$ goes low coincident with or prior to $\overline{E1}$ low or E2 high then the outputs will remain in a high impedance state.
4. During this time the output pins may be in the output state. Signals of opposite phase to the outputs must not be applied at this time.



TYPICAL CHARACTERISTICS

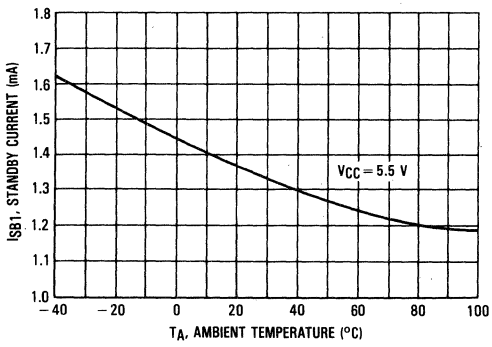


Figure 2. Standby Current Versus Temperature

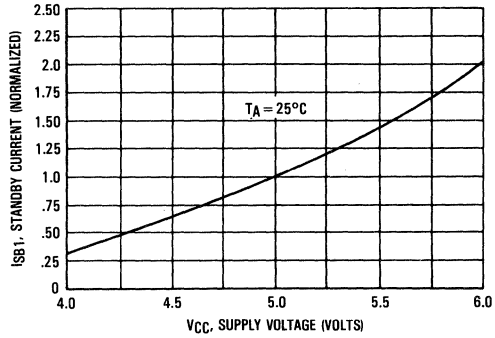


Figure 3. Standby Current Versus Supply Voltage

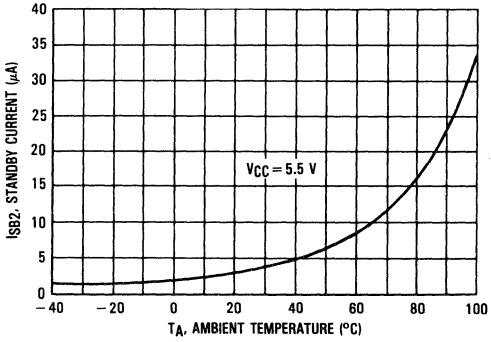


Figure 4. Standby Current Versus Temperature

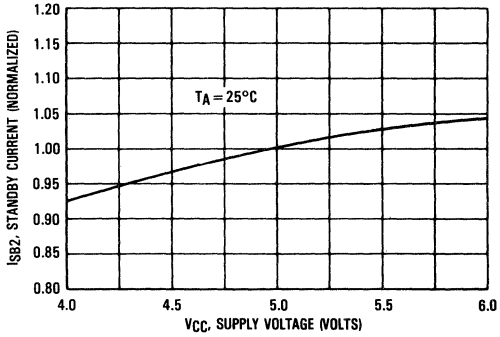


Figure 5. Standby Current Versus Supply Voltage

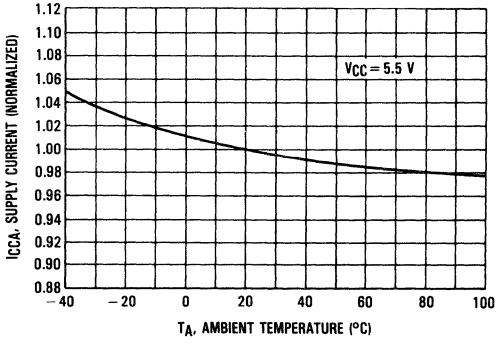


Figure 6. Supply Current Versus Temperature

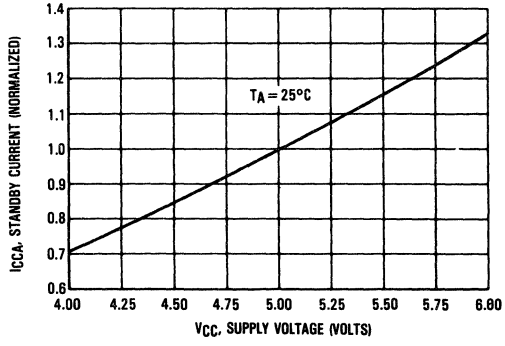


Figure 7. Supply Current Versus Supply Voltage

TYPICAL CHARACTERISTICS
(Continued)

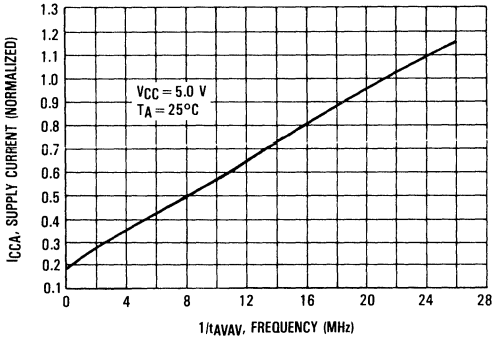


Figure 8. Supply Current Versus Frequency

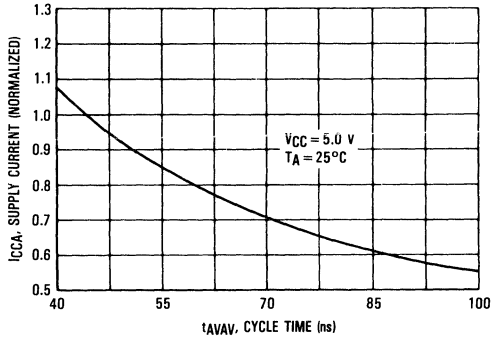


Figure 9. Supply Current Versus Cycle Time

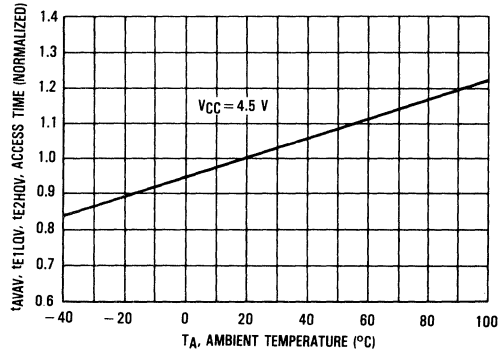


Figure 10. Access Time Versus Temperature

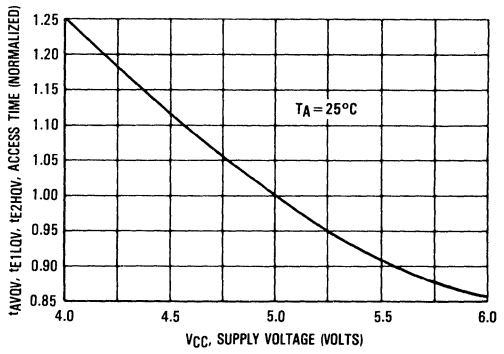


Figure 11. Access Time Versus Supply Voltage

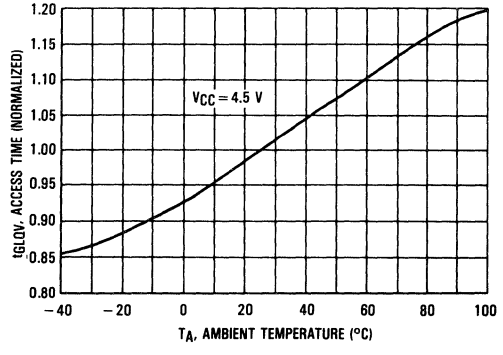


Figure 12. Access Time Versus Temperature

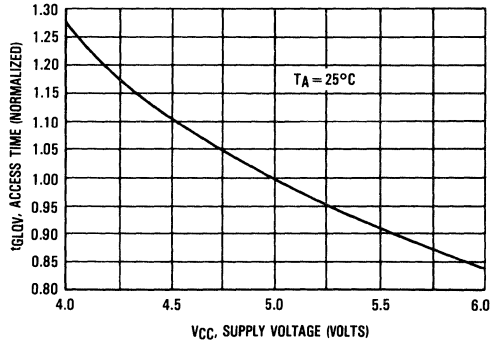
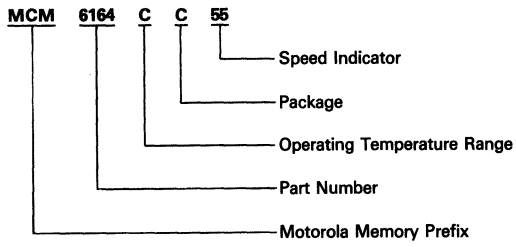


Figure 13. Access Time Versus Supply Voltage

ORDERING INFORMATION
(Order by Full Part Number)



Full Part Number—MCM6164CC55 or MCM6164CC70

7

MCM6205

Advance Information

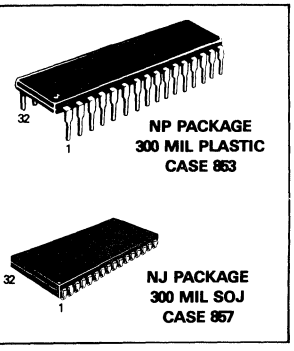
32K x 9 Bit Fast Static Random Access Memory

The MCM6205 is a 294,912 bit static random access memory organized as 32,768 words of 9 bits, fabricated using Motorola's high-performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

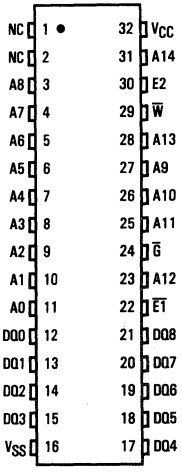
The chip enable pins ($\overline{E1}$ and E2) are not clocks. Either pin, when asserted false, causes the part to enter a low power standby mode. This feature provides significant system-level power savings. The part will remain in standby mode until both pins are asserted true again. Another control feature, output enable ($\overline{G}$), allows access to the memory contents as fast as 12.5 ns (MCM6205-30).

The MCM6205 is packaged in a 300 mil, 32 pin plastic dual-in-line package or a 32 lead, 300 mil plastic SOJ package with the JEDEC standard pinout.

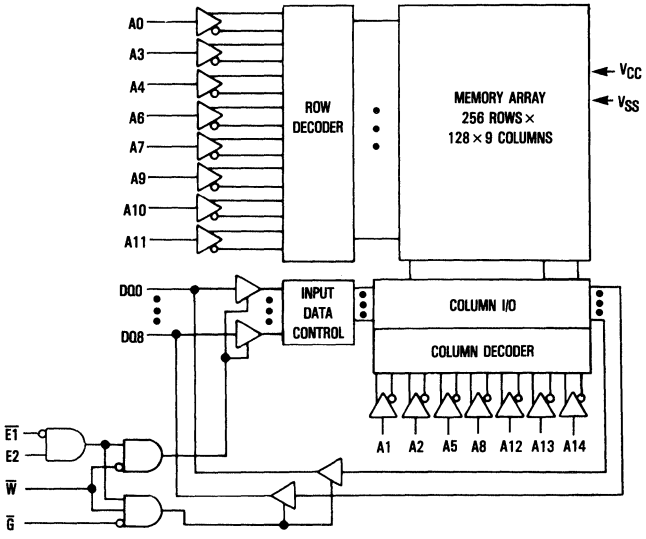
- Single 5 V Supply, ±10%
- Fast Access Time—30, 35, and 45 ns (Maximum)
- Chip Controls: Chip Enable ($\overline{E1}$, E2) for Reduced-Power Standby Mode
  Output Enable ($\overline{G}$) for Fast Access to Data
- Three State Outputs
- Fully TTL Compatible
- High Board Density SOJ Package Available



PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES	
A0-A14	Address
$\overline{W}$	Write Enable
$\overline{E1}$, E2	Chip Enable
$\overline{G}$	Output Enable
DQ0-DQ8	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground
NC	No Connection

This document contains information on a new product. Specifications and information herein are subject to change without notice.

TRUTH TABLE

$\overline{E1}$	E2	$\overline{G}$	$\overline{W}$	Mode	Supply Current	I/O Pin	Cycle
H	X	X	X	Not Selected	I_{SB1}, I_{SB2}	High-Z	—
X	L	X	X	Not Selected	I_{SB1}, I_{SB2}	High-Z	—
L	H	H	H	Output Disabled	I_{CC}	High-Z	—
L	H	L	H	Read	I_{CC}	D_{out}	Read Cycle
L	H	X	L	Write	I_{CC}	D_{in}	Write Cycle

X = don't care

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC}+0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation (T_A = 25°C)	P_D	1.0	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature—Plastic	T_{stg}	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

7

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

*V_{IL} (min) = −0.3 V dc; V_{IL} (min) = −2.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter		Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})		$I_{lkg(I)}$	—	±1.0	μA
Output Leakage Current ($\overline{E}$ = V_{IH}, or $\overline{G}$ = V_{IH}, V_{out} = 0 to 5.5 V)		$I_{lkg(O)}$	—	±1.0	μA
Power Supply Current ($\overline{E}$ = V_{IL}, I_{out} = 0, V_{CC} = Max)	(t_{AVAV} = 30 ns) (t_{AVAV} = 35 ns) (t_{AVAV} = 45 ns)	I_{CCA}	— — —	150 140 135	mA
Standby Current ($\overline{E}$ = V_{IH}) (TTL Levels)		I_{SB1}	—	40	mA
Standby Current ($\overline{E}$ ≥ V_{CC} − 0.2 V) (CMOS Levels)		I_{SB2}	—	20	mA
Output Low Voltage (I_{OL} = 8.0 mA)		V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = −4.0 mA)		V_{OH}	2.4	—	V

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, periodically sampled and not 100% tested.)

Characteristic		Symbol	Max	Unit
Input Capacitance	All Inputs Except $\overline{W}$ $\overline{W}$	C_{in}	6 8	pF
I/O Capacitance		$C_{I/O}$	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . .0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns

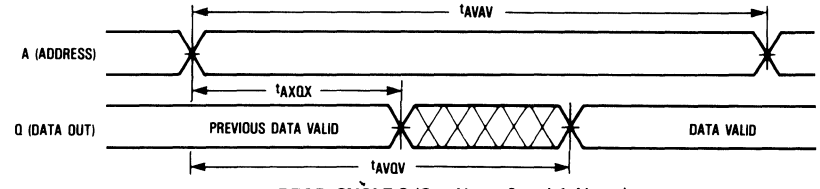
Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load . . . . . .See Figure 1A Unless Otherwise Noted

READ CYCLE (See Notes 1 and 2)

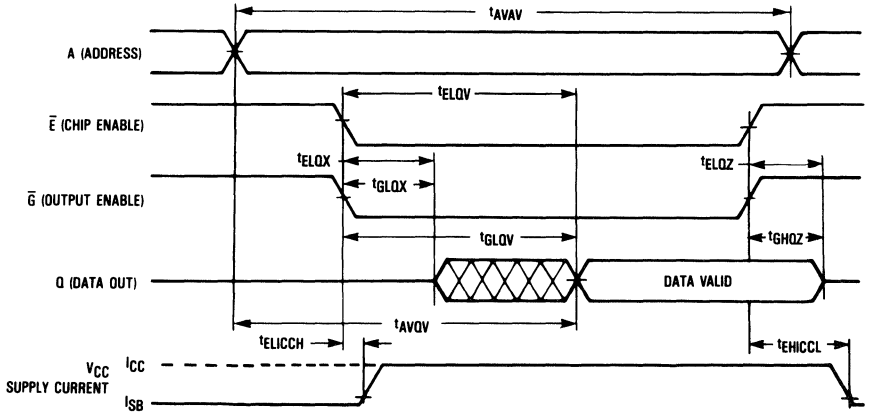
Parameter	Symbol		MCM6205-30		MCM6205-35		MCM6205-45		Units	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	30	–	35	–	45	–	ns	3
Address Access Time	t_{AVQV}	t_{AA}	–	30	–	35	–	45	ns	
Chip Enable Access Time	t_{ELQV}	t_{AC}	–	30	–	35	–	45	ns	4
Chip Enable Low to High	t_{ELEH}	t_{CW}	30	–	35	–	45	–	ns	
Output Hold from Address Change	t_{AXQX}	t_{OH}	5	–	5	–	5	–	ns	
Output Enable Access Time	t_{GLQV}	t_{OE}	–	12.5	–	15	–	20	ns	
Output Enable Low to Output Active	t_{GLQX}	t_{OLZ}	0	–	0	–	0	–	ns	5,6,7
Output Enable High to Output High-Z	t_{GHQZ}	t_{OHZ}	0	17	0	17	0	17	ns	5,6,7
Chip Enable Low to Output Active	t_{ELQX}	t_{CLZ}	5	–	5	–	5	–	ns	5,6,7
Chip Enable High to Output High-Z	t_{ELQZ}	t_{CHZ}	0	20	0	20	0	20	ns	5,6,7
Power Up Time	t_{ELICCH}	t_{PU}	0	–	0	–	0	–	ns	
Power Down Time	t_{EHICCL}	t_{PD}	–	30	–	35	–	45	ns	

NOTES: 1. $\overline{W}$ is high for read cycle.
2. $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E1}$.
3. All read cycle timing is referenced from the last valid address to the first transitioning address.
4. Addresses valid prior to or coincident with $\overline{E}$ going low.
5. At any given voltage and temperature, t_{EHQZ} max < t_{ELQX} min, and t_{GHQZ} max < t_{ELQX} min, both for a given device and from device to device.
6. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B.
7. This parameter is sampled and not 100% tested.
8. Device is continuously selected ($\overline{E} \le V_{IL}$ and $\overline{G} \le V_{IL}$).

READ CYCLE 1 (See Note 8 Above)



READ CYCLE 2 (See Notes 2 and 4 Above)

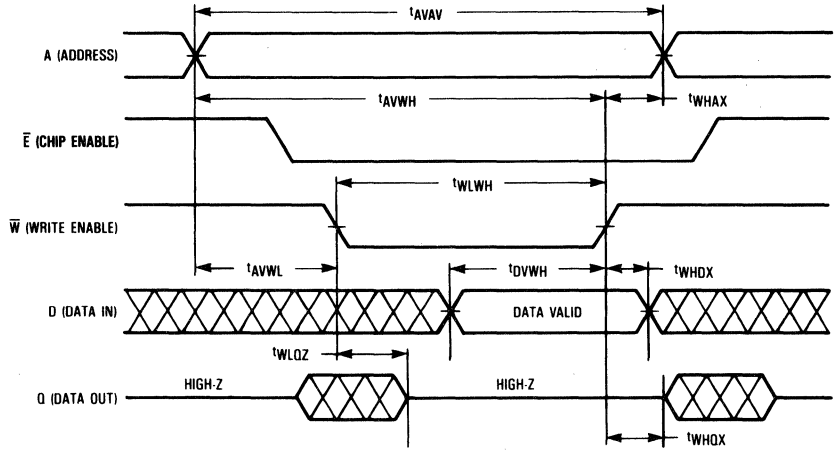


WRITE CYCLE 1 ($\overline{W}$ Controlled) (See Notes 1, 2, and 3)

Parameter	Symbol		MCM6205-30		MCM6205-35		MCM6205-45		Units	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	30	–	35	–	45	–	ns	4
Address Setup Time	t_{AVWL}	t_{AS}	0	–	0	–	0	–	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	25	–	25	–	30	–	ns	
Write Pulse Width	t_{WLWH}	t_{WP}	25	–	25	–	30	–	ns	5
Data Valid to End of Write	t_{DVWH}	t_{DW}	15	–	15	–	20	–	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	–	0	–	0	–	ns	
Write Low to Output High-Z	t_{WLQZ}	t_{WZ}	0	20	0	20	0	20	ns	6,7,8
Write High to Output Active	t_{WHQX}	t_{OW}	5	–	5	–	5	–	ns	6,7,8
Write Recovery Time	t_{WHAX}	t_{WR}	0	–	0	–	0	–	ns	

NOTES:
1. A write cycle occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low. A write cycle ends at the earliest transition of $\overline{E}$ high or $\overline{W}$ high.
2. $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E1}$.
3. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
4. All timings are referenced from the last valid address to the first transitioning address.
5. If $\overline{G} \geq V_{IH}$, the output will remain in a high impedance state.
6. At any given voltage and temperature, t_{WLQZ} max < t_{WHQX} min, both for a given device and from device to device.
7. Transition is measured ±500 mV from steady-state voltage with load in Figure 1B.
8. These parameters are periodically sampled and not 100% tested.

7



AC TEST LOADS

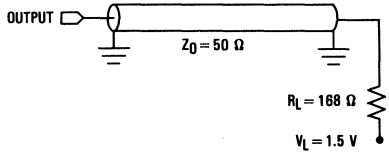


Figure 1A

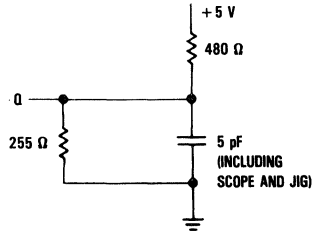
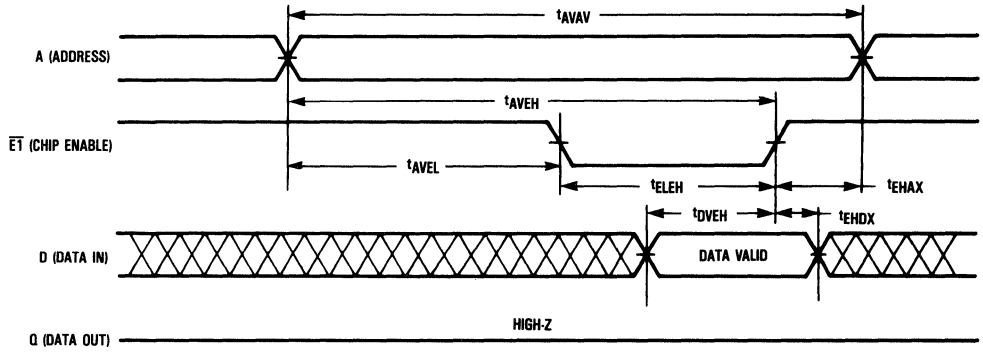


Figure 1B

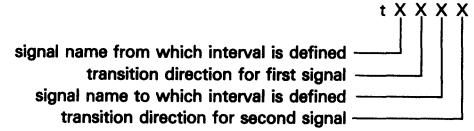
WRITE CYCLE 2 ($\overline{E}$ Controlled) (See Notes 1, 2, and 3)

Parameter	Symbol		MCM6205-30		MCM6205-35		MCM6205-45		Units	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	30	–	35	–	45	–	ns	
Address Setup Time	t_{AVEL}	t_{AS}	0	–	0	–	0	–	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	25	–	25	–	35	–	ns	
Chip Enable to End of Write	t_{ELEH}	t_{CW}	20	–	25	–	35	–	ns	4,5
Data Valid to End of Write	t_{DVEH}	t_{DW}	15	–	15	–	20	–	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	–	0	–	0	–	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	–	0	–	0	–	ns	

NOTES: 1. A write cycle occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low. A write cycle ends at the earliest transition of $\overline{E}$ high or $\overline{W}$ high.
2. $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E1}$.
3. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance state.



TIMING PARAMETER ABBREVIATIONS

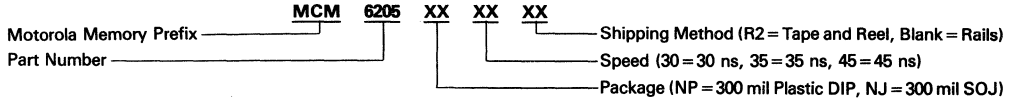


The transition definitions used in this data sheet are:
H = transition to high
L = transition to low
V = transition to valid
X = transition to invalid or don't care
Z = transition to off (high impedance)

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers—	MCM6205NP30	MCM6205NJ30	MCM6205NJ30R2
	MCM6205NP35	MCM6205NJ35	MCM6205NJ35R2
	MCM6205NP45	MCM6205NJ45	MCM6205NJ45R2

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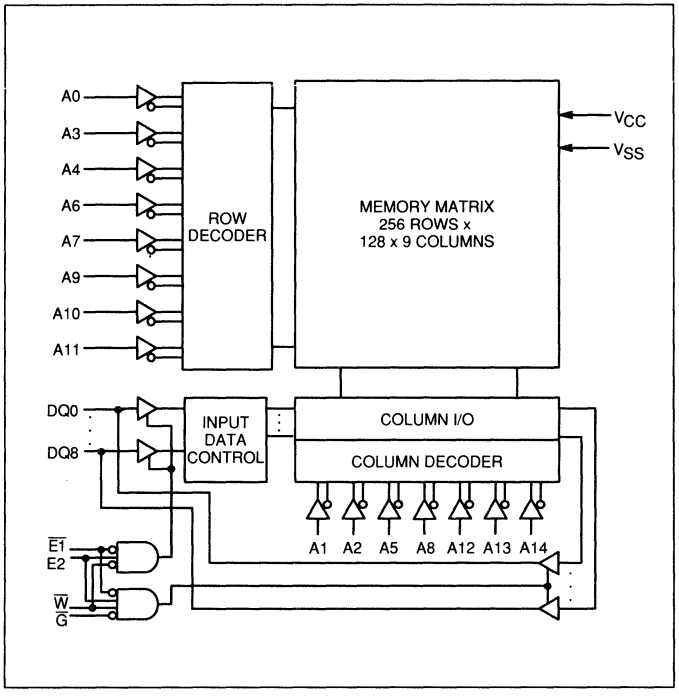
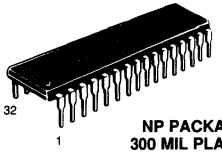
32K x 9 Bit Fast Static RAM

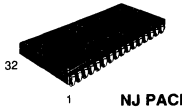
MCM6205-17, -20, -25
See QuickRAM, Page 7-122

MCM6205C-12, -15
See QuickRAM II, Page 7-142





NP PACKAGE
300 MIL PLASTIC
CASE 853



NJ PACKAGE
300 MIL SOJ
CASE 857

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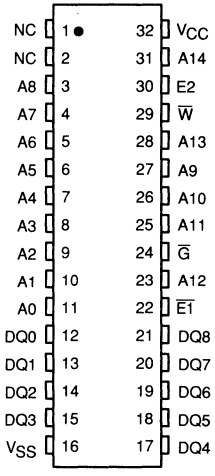
PIN ASSIGNMENT



PIN NAMES	
A0-A14 ..... Address Input	E1, E2 ..... Chip Enable
DQ0–DQ8 ..... Data Input/Output	NC ..... No Connection
W ..... Write Enable	V_{CC} ..... +5 V Power Supply
G ..... Output Enable	V_{SS} ..... Ground

MCM6205 TRUTH TABLE (X = don't care)

E1	E2	G	W	Mode	V_{CC} Current	Output	Cycle
H	X	X	X	Not Selected	I_{SB1}, I_{SB2}	High-Z	—
X	L	X	X	Not Selected	I_{SB1}, I_{SB2}	High-Z	—
L	H	H	H	Output Disabled	I_{CCA}	High-Z	—
L	H	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	H	X	L	Write	I_{CCA}	High-Z	Write Cycle

MCM6206

Advance Information

32K x 8 Bit Fast Static Random Access Memory

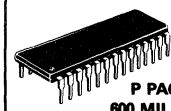
The MCM6206 is a 262,144 bit static random access memory organized as 32,768 words of 8 bits, fabricated using Motorola's high-performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

Chip enable ($\overline{E}$) controls the power-down feature. It is not a clock but rather a chip control that affects power consumption. In less than a cycle time after $\overline{E}$ goes high, the part automatically reduces its power requirements and remains in this low-power standby mode as long as $\overline{E}$ remains high. This feature provides significant system-level power savings. Another control feature, output enable ($\overline{G}$) allows access to the memory contents as fast as 12.5 ns (MCM6206-30).

The MCM6206 is packaged in a 300 or 600 mil, 28 pin plastic dual-in-line package or a 28 lead 300 or 400 mil plastic SOJ package with the JEDEC standard pinout.

- Single 5 V Supply, ±10%
- Fully Static—No Clock or Timing Strobes Necessary
- Fast Access Time—30, 35, or 45 ns (Maximum)
- Low Power Dissipation
- Two Chip Controls; $\overline{E}$ for Automatic Power Down
  $\overline{G}$ for Fast Access to Data
- Three State Outputs
- Fully TTL Compatible

NP PACKAGE
300 MIL PLASTIC
CASE 710B

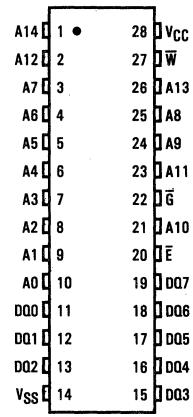


P PACKAGE
600 MIL PLASTIC
CASE 710

J PACKAGE
400 MIL SOJ
CASE 810

NJ PACKAGE
300 MIL SOJ
CASE 810B

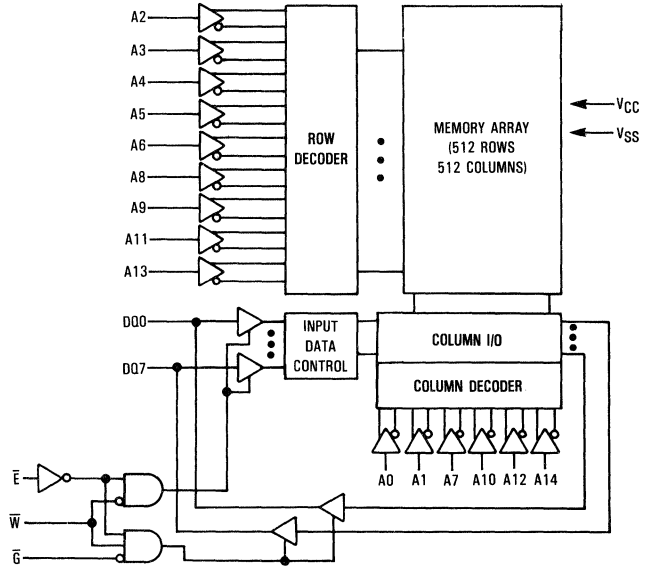
PIN ASSIGNMENT



PIN NAMES

A0-A14	Address
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
DQ0-DQ7	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

BLOCK DIAGRAM



This document contains information on a new product. Specifications and information herein are subject to change without notice.

TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	Supply Current	I/O Pin
H	X	X	Not Selected	I_{SB}	High Z
L	H	H	Output Disabled	I_{CC}	High Z
L	L	H	Read	I_{CC}	D_{out}
L	X	L	Write	I_{CC}	D_{in}

X—Don't Care

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC}+0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation (T_A=25°C)	P_D	1.0	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature—Plastic	T_{stg}	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

7

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC}=5.0 ±10%, T_A=0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	–	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	−0.3*	–	0.8	V

*V_{IL} (min) = −0.3 V dc; V_{IL} (min) = −3.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter		Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in}=0 to V_{CC})		$I_{lkg(I)}$	–	±1.0	μA
Output Leakage Current ($\overline{E}$=V_{IH}, or $\overline{G}$=V_{IH}, V_{out}=0 to 5.5 V)		$I_{lkg(O)}$	–	±1.0	μA
Power Supply Current ($\overline{E}$=V_{IL}, I_{out}=0)	(t_{AVAV}=30 ns) (t_{AVAV}=35 ns) (t_{AVAV}=45 ns)	I_{CC}	– – –	140 135 130	mA
Standby Current ($\overline{E}$=V_{IH}) (TTL Levels)		I_{SB1}	–	40	mA
Standby Current ($\overline{E}$ ≥ V_{CC}−0.2 V) (CMOS Levels)		I_{SB2}	–	20	mA
Output Low Voltage (I_{OL}=8.0 mA)		V_{OL}	–	0.4	V
Output High Voltage (I_{OH}=−4.0 mA)		V_{OH}	2.4	–	V

CAPACITANCE (f=1.0 MHz, T_A=25°C, periodically sampled and not 100% tested.)

Characteristic		Symbol	Max	Unit
Input Capacitance	All Inputs Except $\overline{W}$ $\overline{W}$	C_{in}	6 8	pF
I/O Capacitance		$C_{I/O}$	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

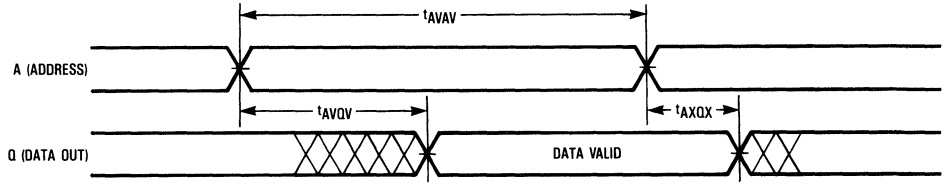
Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns
Input Timing Measurement Reference Levels . . . . . 1.5 V
Output Timing Measurement Reference Levels . . . . . 1.5 V
Output Load . . . . . See Figure 1

READ CYCLE 1 & 2 (See Note 1)

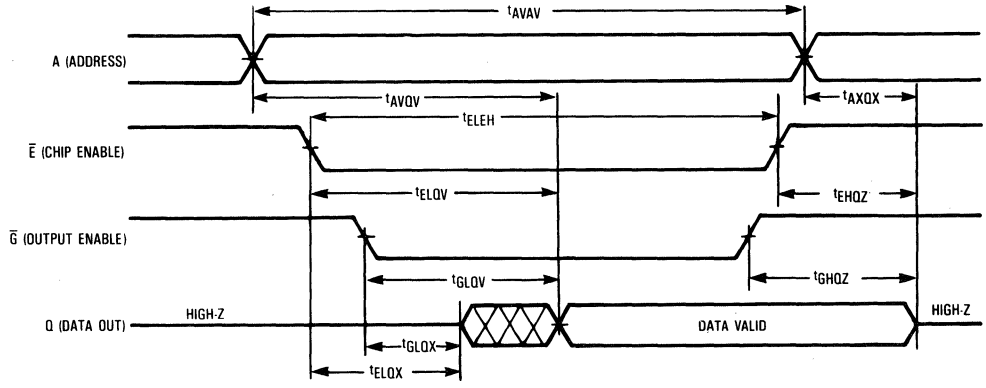
Parameter	Symbol	Alt Symbol	MCM6206-30		MCM6206-35		MCM6206-45		Unit	Notes
			Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	30	–	35	–	45	–	ns	–
Address Access Time	t_{AVQV}	t_{AA}	–	30	–	35	–	45	ns	–
$\overline{E}$ Access Time	t_{ELQV}	t_{AC}	–	30	–	35	–	45	ns	–
$\overline{G}$ Access Time	t_{GLQV}	t_{OE}	–	12.5	–	15	–	20	ns	–
Enable Low to Enable High	t_{ELEH}	t_{CW}	30	–	35	–	45	–	ns	–
Output Hold from Address Change	t_{AXQX}	t_{OH}	5	–	5	–	5	–	ns	2
Chip Enable to Output Low-Z	t_{ELQX}	t_{CLZ}	5	–	5	–	5	–	ns	2, 3
Output Enable to Output Low-Z	t_{GLQX}	t_{OLZ}	0	–	0	–	0	–	ns	2, 3
Chip Enable to Output High-Z	t_{EHQZ}	t_{CHZ}	0	20	0	20	0	20	ns	2, 3
Output Enable to Output High-Z	t_{GHQZ}	t_{OHZ}	0	17	0	17	0	17	ns	2, 3

NOTES:
1. $\overline{W}$ is high at all times for read cycles.
2. All high-Z and low-Z parameters are considered in a high or low impedance state when the output has made a 500 mV transition from the previous steady state voltage.
3. These parameters are periodically sampled and not 100% tested.

READ CYCLE 1 ($\overline{E}=V_{IL}$, $\overline{G}=V_{IL}$)



READ CYCLE 2



WRITE CYCLE 1 & 2 (See Note 1)

Parameter	Symbol	Alt Symbol	MCM6206-30		MCM6206-35		MCM6206-45		Unit	Notes
			Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	30	–	35	–	45	–	ns	–
Address Setup to Write Low Address Setup to Enable Low	t_{AVWL} t_{AVEL}	t_{AS}	0	–	0	–	0	–	ns	2
Address Valid to Write High Address Valid to Enable High	t_{AVWH} t_{AVEH}	t_{AW}	25	–	25	–	35	–	ns	–
Data Valid to Write High Data Valid to Enable High	t_{DVWH} t_{DVEH}	t_{DW}	15	–	15	–	20	–	ns	–
Data Hold From Write High Data Hold From Enable High	t_{WHDX} t_{EHDX}	t_{DH}	0	–	0	–	0	–	ns	–
Write Recovery Time Enable Recovery Time	t_{WHAX} t_{EHAX}	t_{WR}	0	–	0	–	0	–	ns	2
Chip Enable to End of Write Enable Low to Enable High	t_{ELWH} t_{ELEH}	t_{CW}	20	–	25	–	35	–	ns	1
Write Pulse Width	t_{WLWH}	t_{WP}	25	–	25	–	30	–	ns	3
Write Low to Output High-Z	t_{WLQZ}	t_{WHZ}	0	20	0	20	0	20	ns	4, 5
Write High to Output Low-Z	t_{WHQX}	t_{WLZ}	5	–	5	–	5	–	ns	4, 5

NOTES:
1. A write cycle starts at the latest transition of a low $\overline{E}$ or low $\overline{W}$. A write cycle ends at the earliest transition of a high $\overline{E}$ or high $\overline{W}$.
2. $\overline{W}$ must be high during all address transitions whenever $\overline{E}$ is low.
3. If $\overline{G}$ is enabled, allow an additional 15 ns t_{WLWH} to avoid bus contention.
4. All high-Z and low-Z parameters are considered in a high or low impedance state when the output has made a 500 mV transition from the previous steady state voltage.
5. These parameters are periodically sampled and not 100% tested.

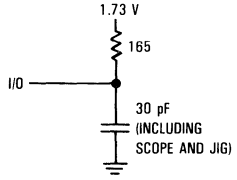
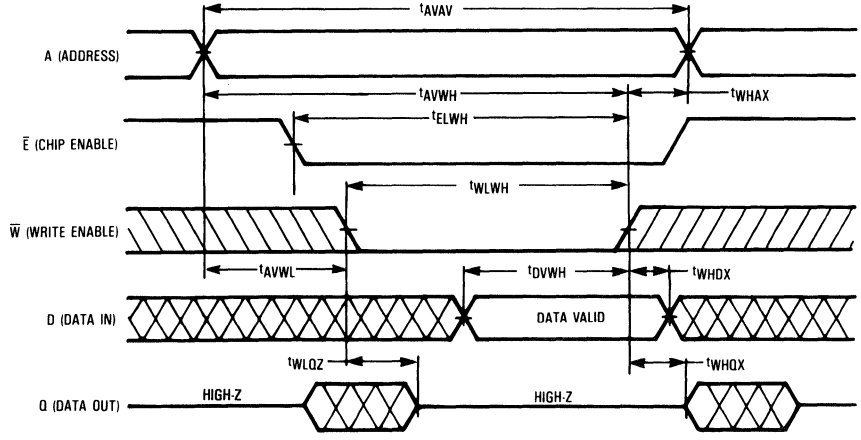
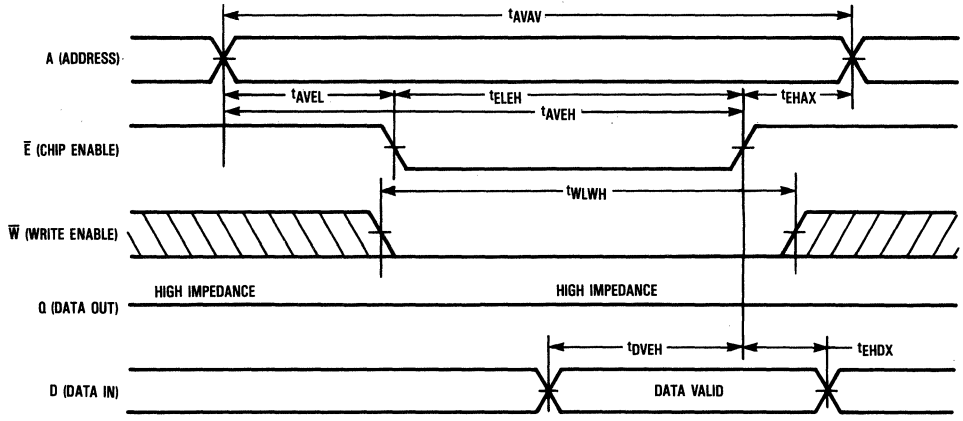


Figure 1. Test Load

WRITE CYCLE 1 ($\overline{W}$ Controlled)



WRITE CYCLE 2 ($\overline{E}$ Controlled)



7

ORDERING INFORMATION
(Order by Full Part Number)

MCM 6206 X XX XX

- Motorola Memory Prefix
- Part Number
- Shipping Method (R2 = Tape & Reel, Blank = Rails)
- Speed (30 = 30 ns, 35 = 35 ns, 45 = 45 ns)
- Package (P = 600 mil Plastic DIP, NP = 300 mil Plastic DIP, J = 400 mil SOJ, NJ = 300 mil SOJ)

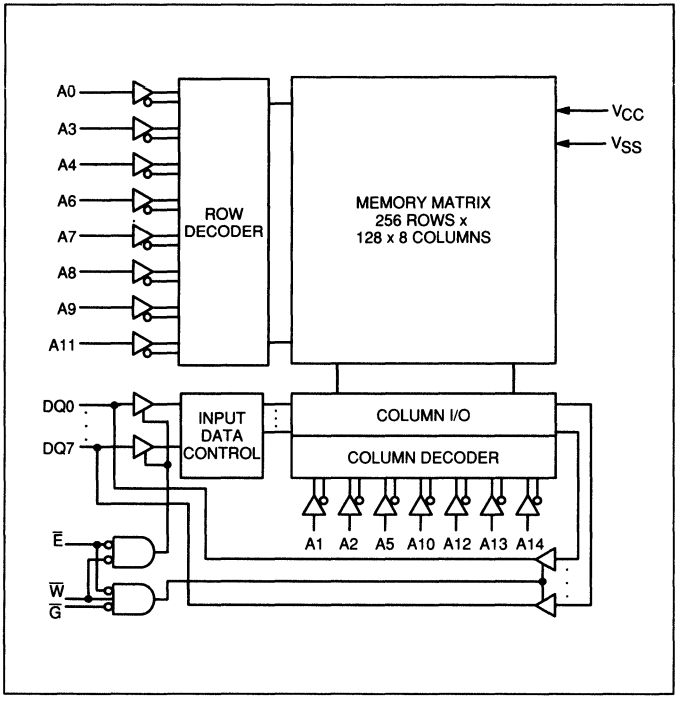
Full Part Numbers—

MCM6206P30	MCM6206NP30	MCM6206J30	MCM6206J30R2	MCM6206NJ30	MCM6206NJ30R2
MCM6206P35	MCM6206NP35	MCM6206J35	MCM6206J35R2	MCM6206NJ35	MCM6206NJ35R2
MCM6206P45	MCM6206NP45	MCM6206J45	MCM6206J45R2	MCM6206NJ45	MCM6206NJ45R2

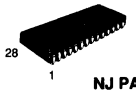
32K x 8 Bit Fast Static RAM

MCM6206-17, -20, -25
See QuickRAM, Page 7-122

MCM6206C-12, -15
See QuickRAM II, Page 7-142

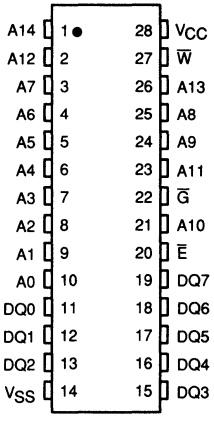


NP PACKAGE
300 MIL PLASTIC
CASE 710B



NJ PACKAGE
300 MIL SOJ
CASE 810B

PIN ASSIGNMENT



PIN NAMES	
A0-A14 ..... Address Input	E ..... Chip Enable
DQ0–DQ7 ..... Data Input/Output	V_{CC} ..... +5 V Power Supply
W ..... Write Enable	V_{SS} ..... Ground
G ..... Output Enable	

MCM6206 TRUTH TABLE (X = don't care)

E	G	W	Mode	V_{CC} Current	Output	Cycle
H	X	X	Not Selected	I_{SB1}, I_{SB2}	High-Z	—
L	H	H	Output Disabled	I_{CCA}	High-Z	—
L	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	X	L	Write	I_{CCA}	High-Z	Write Cycle

7

MCM6206C

Advance Information

32K × 8 Bit Static RAM

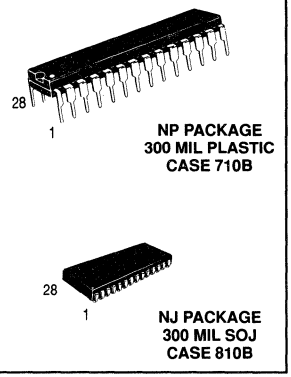
Industrial Temperature Range: –40 to 85°C

The MCM6206C is a 262,144 bit static random access memory organized as 32,768 words of 8 bits, fabricated using high-performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

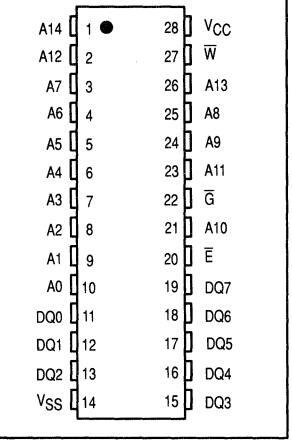
Chip enable ($\overline{E}$) controls the power-down feature. It is not a clock but rather a chip control that affects power consumption. In less than a cycle time after $\overline{E}$ goes high, the part automatically reduces its power requirements and remains in this low-power standby mode as long as $\overline{E}$ remains high. This feature provides significant system-level power savings. Another control feature, output enable ($\overline{G}$) allows access to the memory contents as fast as 12 ns (MCM6206C-25).

The MCM6206C is available in a 300 mil, 28 lead plastic dual-in-line package or a 300 mil, 28 lead plastic SOJ package with the JEDEC standard pinout.

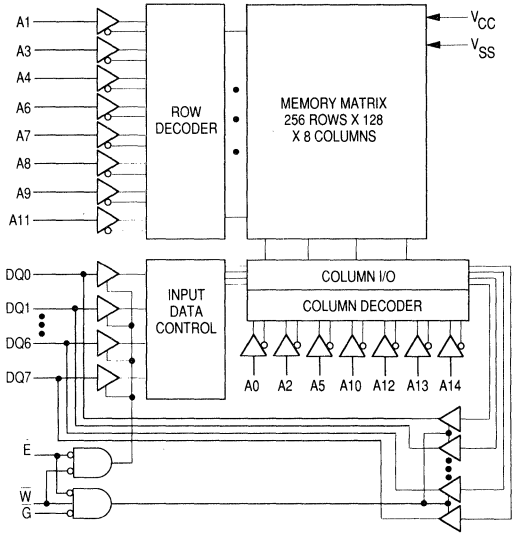
- Single 5 V ± 10% Power Supply
- Fast Access Time: 25, 30, 35, 45, 55 ns
- Chip Controls:
  Chip Enable ($\overline{E}$) for Reduced-Power Standby Mode
  Output Enable ($\overline{G}$) for Fast Access to Data
- Three-State Outputs
- Fully TTL Compatible
- Power Operation: 150 mA Maximum, Active AC (MCM6206C-25)
- High Board Density SOJ Package Available



PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A0–A14	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E}$	Chip Enable
DQ0–DQ7	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground

All power supply and ground pins must be connected for proper operation of the device.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	Not Selected	I_{ISB1}, I_{SB2}	High-Z	—
L	H	H	Read	I_{CCA}	High-Z	—
L	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	X	L	Write	I_{CCA}	D_{in}	Write Cycle

X = Don't Care

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high impedance circuits.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to 7.0	V
Voltage Relative to V_{SS} (For Any Pin Except V_{CC})	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation (T_A = 25°C)	P_D	1.5	W
Temperature Under Bias	T_{bias}	– 50 to + 95	°C
Operating Temperature	T_A	– 40 to + 85	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

7

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = – 40 to + 85°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

*V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns); V_{IL} (min) = – 0.5 V dc)

DC CHARACTERISTICS

Parameter		Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})		$I_{lkg(I)}$	—	± 1	µA
Output Leakage Current ($\overline{E}$ = V_{IL}, V_{out} = 0 to V_{CC})		$I_{lkg(O)}$	—	± 1	µA
AC Supply Current (I_{out} = 0 mA, V_{CC} = Max)	t_{AVAV} = 25 ns	I_{CCA}	—	150	mA
	t_{AVAV} = 30 ns		—	150	
	t_{AVAV} = 35 ns		—	150	
	t_{AVAV} = 45 ns		—	140	
	t_{AVAV} = 55 ns		—	140	
TTL Standby Current ($\overline{E}$ = V_{IH}, No Restrictions on Other Inputs)		I_{SB1}	—	40	mA
CMOS Standby Current ($\overline{E}$ ≥ V_{CC} – 0.2 V, No Restrictions on Other Inputs)		I_{SB2}	—	20	mA
Output Low Voltage (I_{OL} = + 8.0 mA)		V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)		V_{OH}	2.4	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Max	Unit
Input Capacitance	(All Inputs Except $\overline{W}$ and DQ)	C_{in}	6	pF
	$\overline{W}$		8	
Input/Output Capacitance		$C_{I/O}$	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = – 40 to + 85°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 5 ns

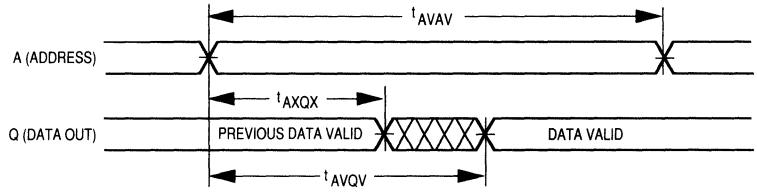
Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

READ CYCLE TIMING (See Note 1)

Parameter	Symbol		MCM6206C-25		MCM6206C-30		MCM6206C-35		MCM6206C-45		MCM6206C-55		Unit	Notes
	Std.	Alt.	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	25	—	30	—	35	—	45	—	55	—	ns	2
Address Access Time	t_{AVQV}	t_{AA}	—	25	—	30	—	35	—	45	—	55	ns	
Enable Access Time	t_{ELQV}	t_{ACS}	—	25	—	30	—	35	—	45	—	55	ns	
Output Enable Access Time	t_{GLQV}	t_{OE}	—	12	—	12.5	—	15	—	20	—	25	ns	
Output Hold from Address Change	t_{AXQX}	t_{OH}	4	—	4	—	4	—	4	—	4	—	ns	
Enable Low to Output Active	t_{ELQX}	t_{CLZ}	4	—	4	—	4	—	4	—	4	—	ns	3, 4, 5
Output Enable to Output Active	t_{GLQX}	t_{OLZ}	0	—	0	—	0	—	0	—	0	—	ns	3, 4, 5
Enable High to Output High-Z	t_{EHQZ}	t_{CHZ}	0	10	0	10	0	10	0	10	0	10	ns	3, 4, 5
Output Enable High to Output High-Z	t_{GHQZ}	t_{OHZ}	0	10	0	10	0	10	0	10	0	10	ns	3, 4, 5
Power Up Time	t_{ELICCH}	t_{PU}	0	—	0	—	0	—	0	—	0	—	ns	
Power Down Time	t_{EHICCL}	t_{PD}	—	25	—	30	—	35	—	45	—	55	ns	

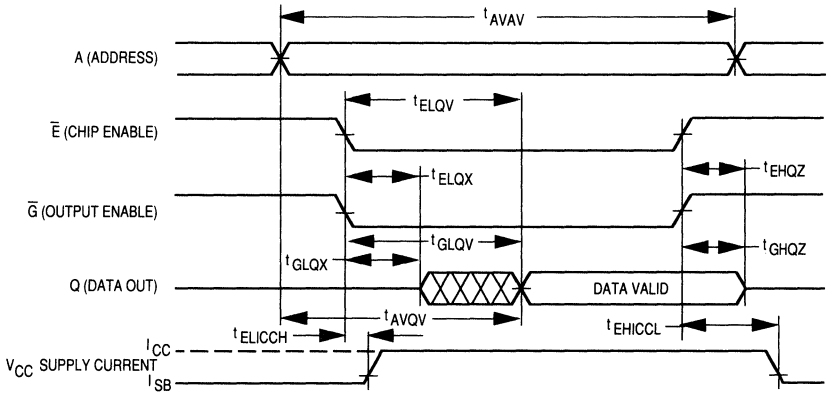
NOTES:
1. $\overline{W}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transitioning address.
3. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} min, and t_{GHQZ} max is less than t_{GHQX} min, both for a given device and from device to device.
4. Transition is measured + 500 mV from steady-state voltage with load of Figure 1B.
5. This parameter is sampled and not 100% tested.

READ CYCLE 1 (See Note)



NOTE: Device is continuously selected ($\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$)

READ CYCLE 2 (See Note)



NOTE: Addresses valid prior to or coincident with $\overline{E}$ going low.

AC TEST LOADS

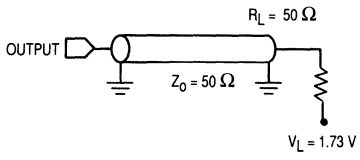


Figure 1A

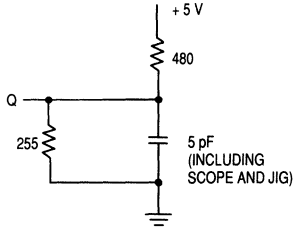


Figure 1B

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the module point of view. Thus, the access time is shown as a maximum since the module never provides data later than that time.

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Note 1)

Parameter	Symbol		MCM6206C-25		MCM6206C-30		MCM6206C-35		MCM6206C-45		MCM6206C-55		Unit	Notes
	Std.	Alt.	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	25	—	30	—	35	—	45	—	55	—	ns	2
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	20	—	25	—	25	—	35	—	45	—	ns	
Write Pulse Width	t_{WLWH}	t_{WP}	20	—	20	—	25	—	30	—	35	—	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	10	—	15	—	15	—	20	—	25	—	ns	
Data Hold TIme	t_{WHDX}	t_{DH}	0	—	0	—	0	—	0	—	0	—	ns	
Write Low to Data High-Z	t_{WLQZ}	t_{WZ}	0	10	0	10	0	10	0	10	0	10	ns	3, 4, 5
Write High to Output Active	t_{WHQX}	t_{OW}	4	—	4	—	4	—	4	—	4	—	ns	3, 4, 5
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	0	—	0	—	0	—	ns	

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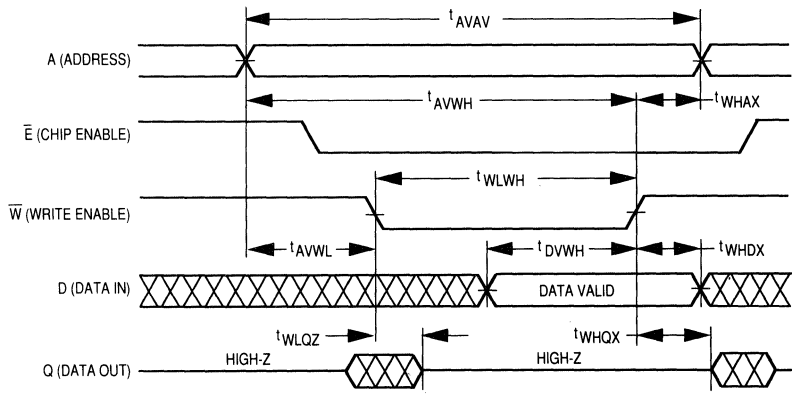
NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. All write cycle timing is referenced from the last valid address to the first transitioning address.
3. Transition is measured + 500 mV from steady-state voltage with load of Figure 1B.
4. This parameter is sampled and not 100% tested.
5. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1

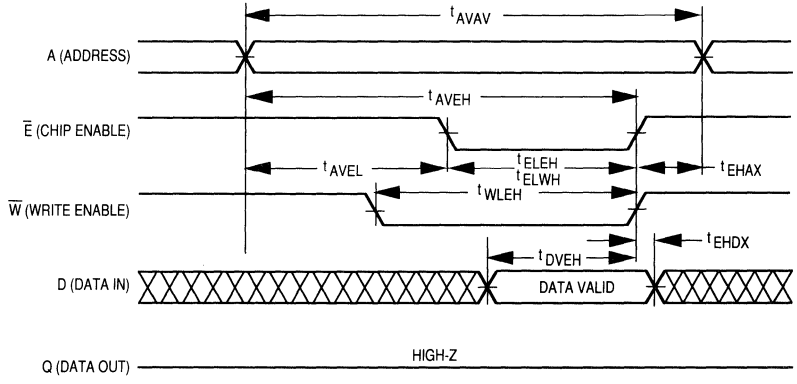


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Note 1)

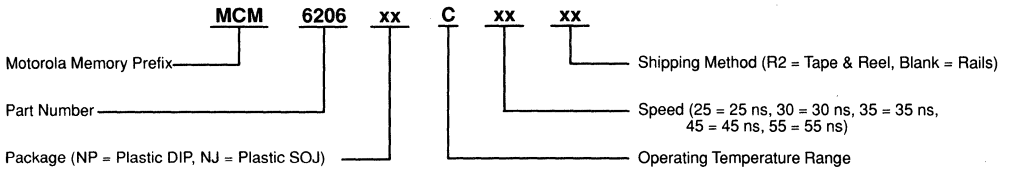
Parameter	Symbol		MCM6206C-25		MCM6206C-30		MCM6206C-35		MCM6206C-45		MCM6206C-55		Unit	Notes
	Std.	Alt.	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	25	—	30	—	35	—	45	—	55	—	ns	2
Address Setup Time	t_{AVEL}	t_{AS}	0	—	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	20	—	25	—	25	—	35	—	45	—	ns	
Enable to End of Write	t_{ELEH}	t_{CW}	15	—	20	—	25	—	35	—	40	—	ns	3, 4
Enable to End of Write	t_{ELWH}	t_{CW}	15	—	20	—	25	—	35	—	40	—	ns	
Write Pulse Width	t_{WLEH}	t_{WP}	20	—	20	—	25	—	30	—	35	—	ns	
Data Valid to End of Write	t_{DVEH}	t_{DW}	10	—	10	—	15	—	20	—	25	—	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	—	0	—	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	—	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. All write cycle timing is referenced from the last valid address to the first transitioning address.
3. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
4. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2



ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers –	MCM6206NPC25	MCM6206NJC25	MCM6206NJC25R2
	MCM6206NPC30	MCM6206NJC30	MCM6206NJC30R2
	MCM6206NPC35	MCM6206NJC35	MCM6206NJC35R2
	MCM6206NPC45	MCM6206NJC45	MCM6206NJC45R2
	MCM6206NPC55	MCM6206NJC55	MCM6206NJC55R2

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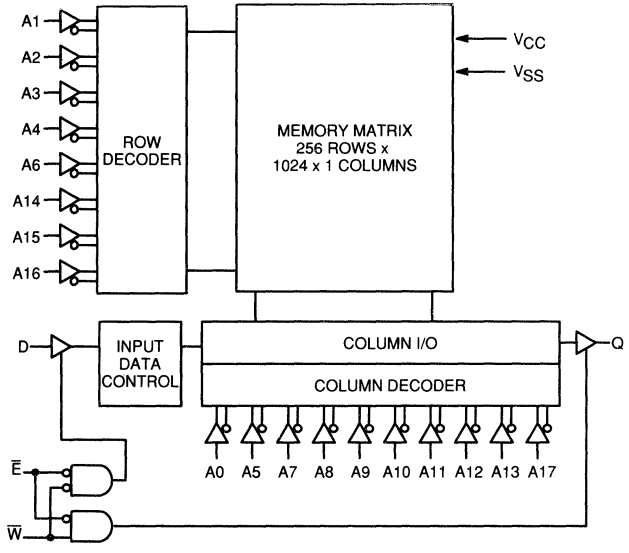
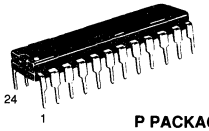
MCM6207-15, -20, -25
See QuickRAM, Page 7-122

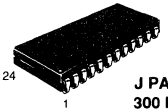
MCM6207C-10, -12
See QuickRAM II, Page 7-142

256K x 1 Bit Fast Static RAM



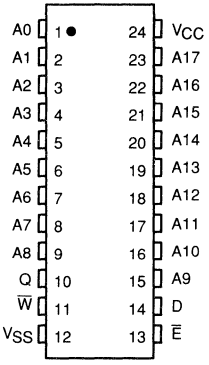


P PACKAGE
300 MIL PLASTIC
CASE 724A



J PACKAGE
300 MIL SOJ
CASE 810A

PIN ASSIGNMENT



PIN NAMES	
A0-A17 ..... Address Input	Q ..... Data Output
E ..... Chip Enable	VCC ..... +5 V Power Supply
W ..... Write Enable	VSS ..... Ground
D ..... Data Input	

MCM6207 TRUTH TABLE (X = don't care)

E	W	Mode	VCC Current	Output	Cycle
H	X	Not Selected	I_{SB1}, I_{SB2}	High-Z	—
L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	L	Write	I_{CCA}	High-Z	Write Cycle

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MCM6208-35, -45
MCM6209-35, -45

64K x 4 Bit Static RAMs

The MCM6208 and MCM6209 are 262,144 bit static random access memories organized as 65,536 words of 4 bits, fabricated using Motorola's high-performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption for greater reliability.

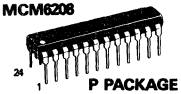
The MCM6209 has both chip enable ($\overline{E}$) and output enable ($\overline{G}$) inputs, allowing greater system flexibility. Either input, when high, will force the outputs to high impedance.

- Single 5 V ±10% Power Supply
- Fast Access Time (Maximum):

(xx = 08 or 09)	Address	Chip Enable	MCM6209 Output Enable
MCM62xx-35	35 ns	35 ns	15 ns
MCM62xx-45	45 ns	45 ns	17 ns

- Equal Address and Chip Enable Access Time
- Output Enable ($\overline{G}$) Feature for Increased System Flexibility and to Eliminate Bus Contention Problems (MCM6209)
- Fully TTL Compatible—Three-State Data Output

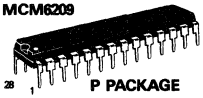
MCM6208



P PACKAGE
300 MIL PLASTIC
CASE 724A

J PACKAGE
300 MIL SOJ
CASE 810A

MCM6209

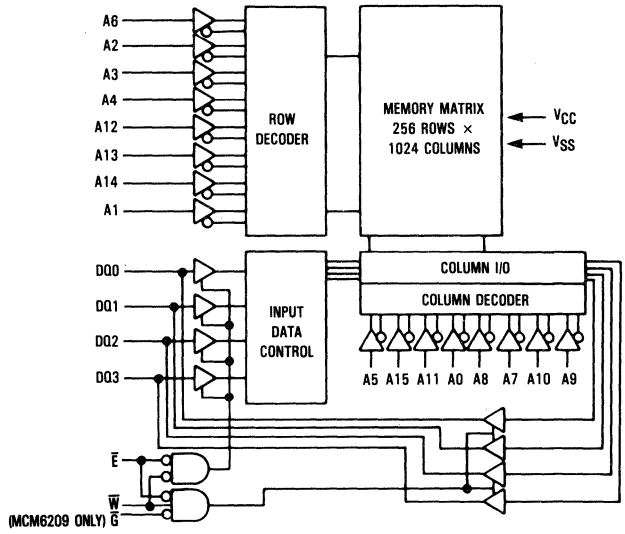


P PACKAGE
300 MIL PLASTIC
CASE 710B

J PACKAGE
300 MIL SOJ
CASE 810B

7

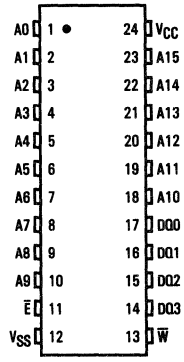
BLOCK DIAGRAM



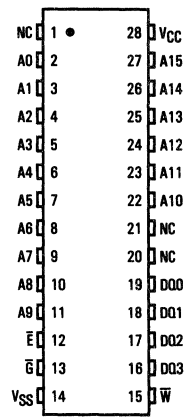
PIN NAMES	
A0-A15 . . . . . Address Input	$\overline{E}$ . . . . . Chip Enable
DQ0-DQ3 . . Data Input/Output	NC . . . . . No Connection
$\overline{W}$ . . . . . Write Enable	V_{CC} . . . . +5 V Power Supply
$\overline{G}$ (MCM6209) . . Output Enable	V_{SS} . . . . . Ground

PIN ASSIGNMENT

MCM6208



MCM6209



MCM6208 TRUTH TABLE

$\overline{E}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	Not Selected	ISB1, ISB2	High-Z	—
L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	L	Write	I_{CCA}	High-Z	Write Cycle

MCM6209 TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	I/O Pin	Cycle
H	X	X	Not Selected	I_{SB}	High-Z	—
L	H	H	Read	I_{CCA}	High-Z	—
L	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	X	L	Write	I_{CCA}	D_{in}	Write Cycle

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC}+0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation (T_A=25°C)	P_D	1.0	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

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DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC}=5.0 V ±10%, T_A=0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

*V_{IL} (min) = −0.5 V dc; V_{IL} (min) = −2.0 V ac (pulse width ≤20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, V_{in}=0 to V_{CC})	$I_{lkg(I)}$	—	—	±1.0	μA
Output Leakage Current ($\overline{E}$=V_{IH}, V_{out}=0 to V_{CC})	$I_{lkg(O)}$	—	—	±1.0	μA
AC Supply Current (I_{out}=0 mA) t_{AVAV}=35 ns	I_{CCA}	—	—	130	mA
t_{AVAV}=45 ns		—	—	130	
AC Standby Current ($\overline{E}$=V_{IH}, No Restrictions on Other Inputs)	I_{SB1}	—	—	35	mA
CMOS Standby Current ($\overline{E}$≥V_{CC}−0.2 V, No Restrictions on Other Inputs)	I_{SB2}	—	—	10	mA
Output Low Voltage (I_{OL}=8.0 mA)	V_{OL}	—	—	0.4	V
Output High Voltage (I_{OH}=−4.0 mA)	V_{OH}	2.4	—	—	V

CAPACITANCE (f=1.0 MHz, dV=3.0 V, T_A=25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	4	6	pF
I/O Capacitance	$C_{I/O}$	5	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC}=5 V ±10%, T_A=0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . .0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns

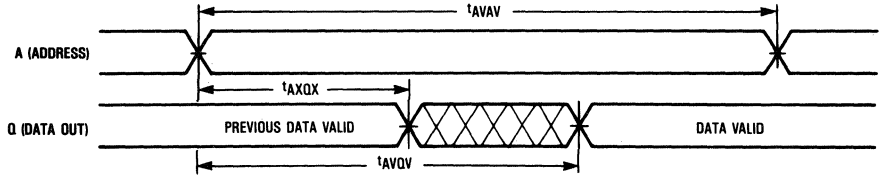
Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load . . . . . Figure 1A Unless Otherwise Noted

READ CYCLE (See Note 1)

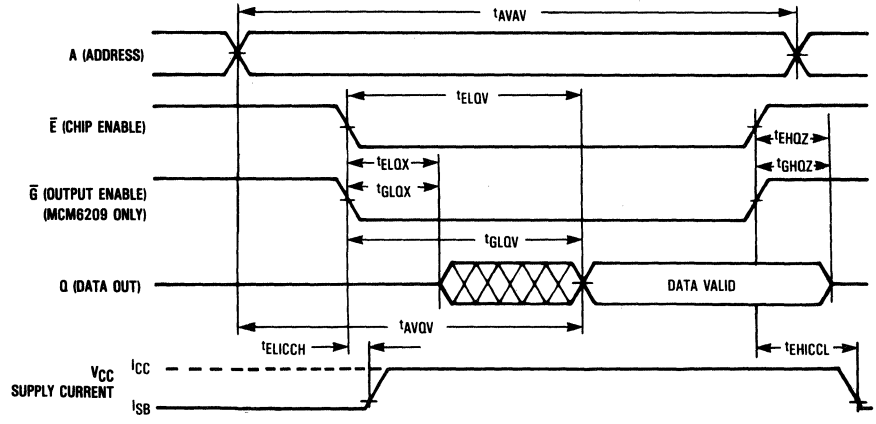
Parameter		Symbol		MCM6208-35 MCM6209-35		MCM6208-45 MCM6209-45		Units	Notes
		Standard	Alternate	Min	Max	Min	Max		
Read Cycle Time		t_{AVAV}	t_{RC}	35	–	45	–	ns	2
Address Access Time		t_{AVQV}	t_{AA}	–	35	–	45	ns	
Enable Access Time		t_{ELQV}	t_{ACS}	–	35	–	45	ns	3
Output Hold from Address Change		t_{AXQX}	t_{OH}	4	–	4	–	ns	
Output Enable Access Time	MCM6209	t_{GLQV}	t_{OE}	–	15	–	17	ns	
Output Enable Low to Output Active	MCM6209	t_{GLQX}	t_{LZ}	0	–	0	–	ns	4,5,6
Output Enable High to Output High-Z	MCM6209	t_{GHQZ}	t_{HZ}	0	10	0	10	ns	4,5,6
Enable Low to Output Active		t_{ELQX}	t_{LZ}	4	–	4	–	ns	4,5,6
Enable High to Output High-Z		t_{EHQZ}	t_{HZ}	0	10	0	10	ns	4,5,6
Power Up Time		t_{ELICCH}	t_{PU}	0	–	0	–	ns	
Power Down Time		t_{EHICCL}	t_{PD}	–	35	–	45	ns	

NOTES: 1. $\overline{W}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transitioning address.
3. Addresses valid prior to or coincident with $\overline{E}$ going low.
4. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} min, and t_{GHQZ} max is less than t_{GLQX} min, both for a given device and from device to device.
5. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E}=V_{IL}$) and $\overline{G}=V_{IL}$ (MCM6209 only).

READ CYCLE 1 (See Note 7 Above)



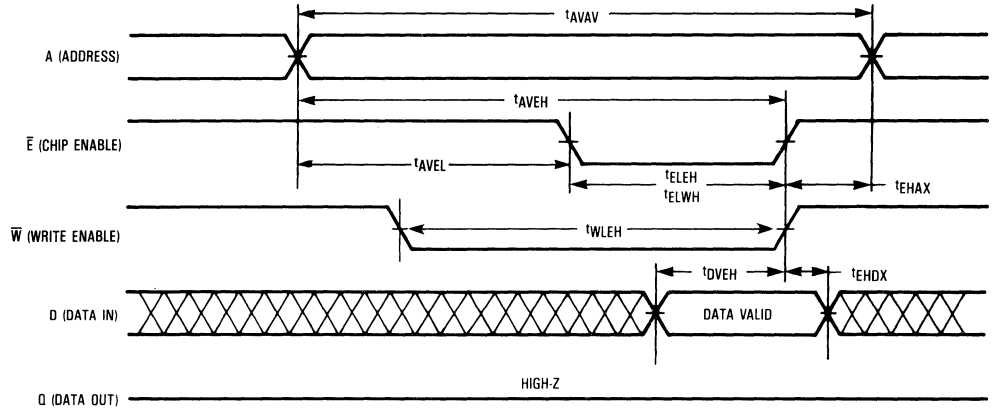
READ CYCLE 2 (See Note 3 Above)



WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 5)

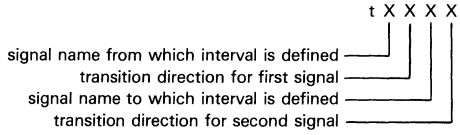
Parameter	Symbol		MCM6208-35 MCM6209-35		MCM6208-45 MCM6209-45		Units	Notes
	Standard	Alternate	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	35	–	45	–	ns	2
Address Setup Time	t_{AVEL}	t_{AS}	0	–	0	–	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	20	–	20	–	ns	
Enable to End of Write	t_{ELEH}	t_{CW}	15	–	15	–	ns	3,4
Enable to End of Write	t_{ELWH}	t_{CW}	15	–	15	–	ns	3,4
Write Pulse Width	t_{WLEH}	t_{WP}	20	–	20	–	ns	
Data Valid to End of Write	t_{DVEH}	t_{DW}	10	–	10	–	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	–	0	–	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	–	0	–	ns	

NOTES: 1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. All write cycle timing is referenced from the last valid address to the first transitioning address.
3. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
4. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.
5. MCM6209, if $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.



7

TIMING PARAMETER ABBREVIATIONS



The transition definitions used in this data sheet are:
H = transition to high
L = transition to low
V = transition to valid
X = transition to invalid or don't care
Z = transition to off (high impedance)

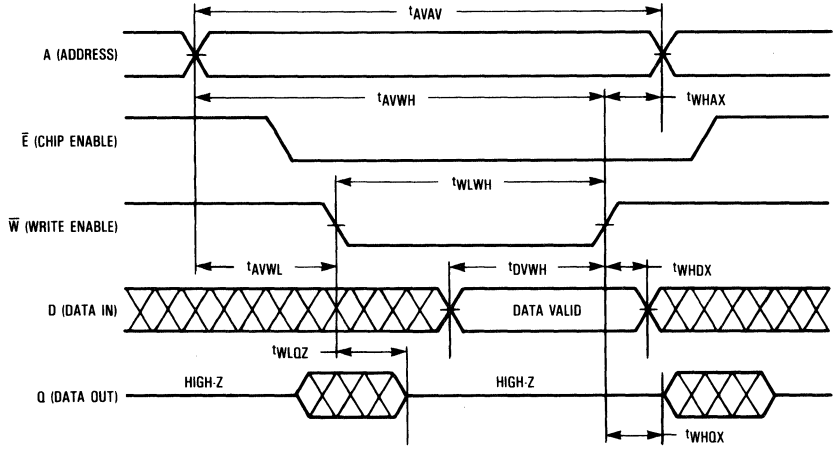
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 6)

Parameter	Symbol		MCM6208-35 MCM6209-35		MCM6208-45 MCM6209-45		Units	Notes
	Standard	Alternate	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	35	–	45	–	ns	2
Address Setup Time	t_{AVWL}	t_{AS}	0	–	0	–	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	20	–	20	–	ns	
Write Pulse Width	t_{WLWH}	t_{WP}	20	–	20	–	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	10	–	10	–	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	–	0	–	ns	
Write Low to Output High-Z	t_{WLQZ}	t_{WZ}	0	10	0	10	ns	3,4,5
Write High to Output Active	t_{WHQX}	t_{OW}	4	–	4	–	ns	3,4,5
Write Recovery Time	t_{WHAX}	t_{WR}	0	–	0	–	ns	

NOTES: 1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. All write cycle timing is referenced from the last valid address to the first transitioning address.
3. Transition is measured ±500 mV from steady-state voltage with load in Figure 1B.
4. Parameter is sampled and not 100% tested.
5. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min both for a given device and from device to device.
6. MCM6209, if $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.



AC TEST LOADS

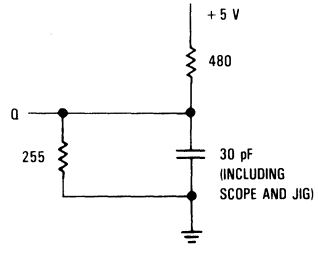


Figure 1A

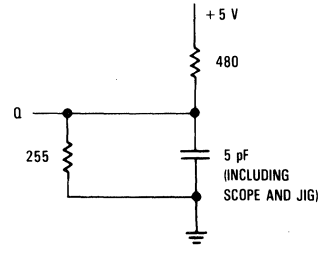
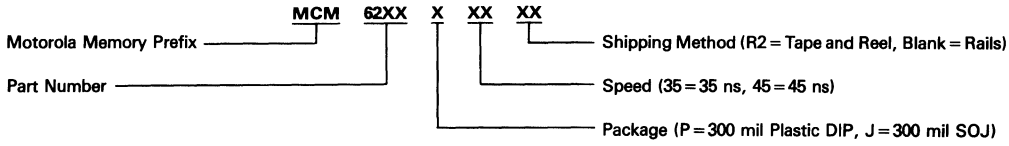


Figure 1B

ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers—	MCM6208P35	MCM6208J35	MCM6208J35R2
	MCM6208P45	MCM6208J45	MCM6208J45R2
	MCM6209P35	MCM6209J35	MCM6209J35R2
	MCM6209P45	MCM6209J45	MCM6209J45R2

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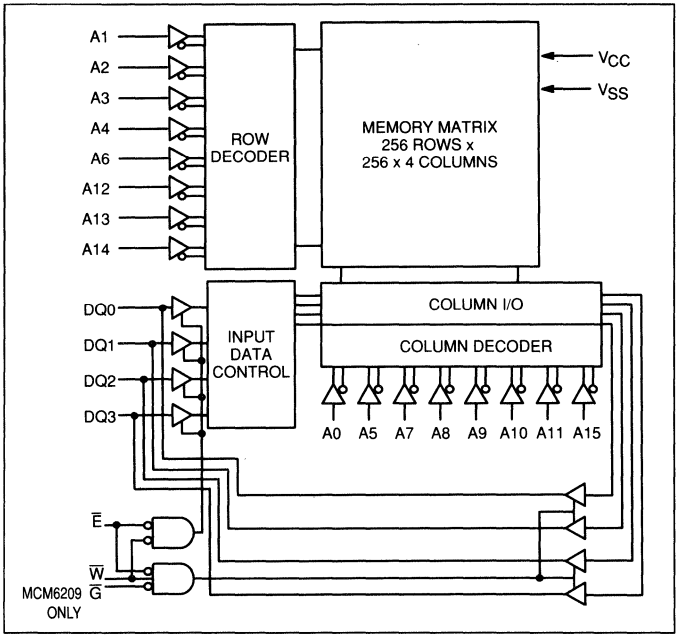
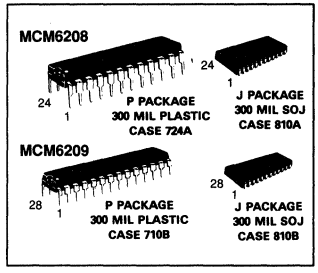
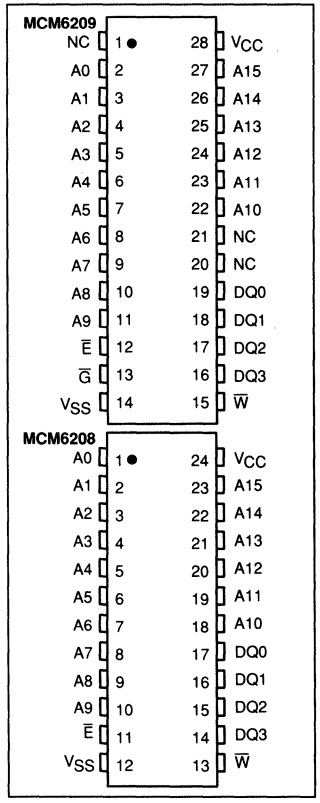
64K x 4 Bit Fast Static RAMs

MCM6208-15, -20, -25
MCM6209-15, -20, -25
See QuickRAM, Page 7-122

MCM6208C-10, -12
MCM6209C-10, -12
See QuickRAM II, Page 7-142







PIN NAMES			
A0-A15	Address Input	$\overline{E}$	Chip Enable
DQ0–DQ3	Data Input/Output	NC	No Connection
$\overline{W}$	Write Enable	V_{CC}	+5 V Power Supply
$\overline{G}$ (MCM6209)	Output Enable	V_{SS}	Ground

MCM6208 TRUTH TABLE (X = don't care)

$\overline{E}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	Not Selected	I_{SB1}, I_{SB2}	High-Z	—
L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	L	Write	I_{CCA}	High-Z	Write Cycle

MCM6209 TRUTH TABLE (X = don't care)

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	Not Selected	I_{SB1}, I_{SB2}	High-Z	—
L	H	H	Output Disabled	I_{CCA}	High-Z	—
L	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	X	L	Write	I_{CCA}	High-Z	Write Cycle

MCM6226

Product Preview

128K × 8 Bit Static Random Access Memory

The MCM6226 is a 1,048,576 bit static random-access memory organized as 131,072 words of 8 bits, fabricated using high-performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

The MCM6226 is equipped with both chip enable ($\overline{E}$) and output enable ($\overline{G}$) inputs, allowing for greater system flexibility. Either input, when high, will force the outputs to high impedance.

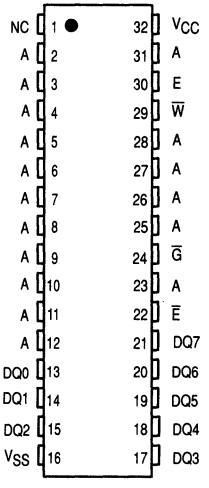
The MCM6226 is available in a 400 mil, 32 lead plastic dual-in-line package or a 400 mil, 32 lead plastic SOJ package with the JEDEC standard pinout.

- Single 5 V ± 10% Power Supply
- Fast Access Time: 25, 30 ns
- Equal Address and Chip Enable Access Time
- Three-State Outputs
- Fully TTL Compatible
- Power Operation: 160 mA Maximum, Active AC (MCM6226-25)
- High Board Density SOJ Package Available

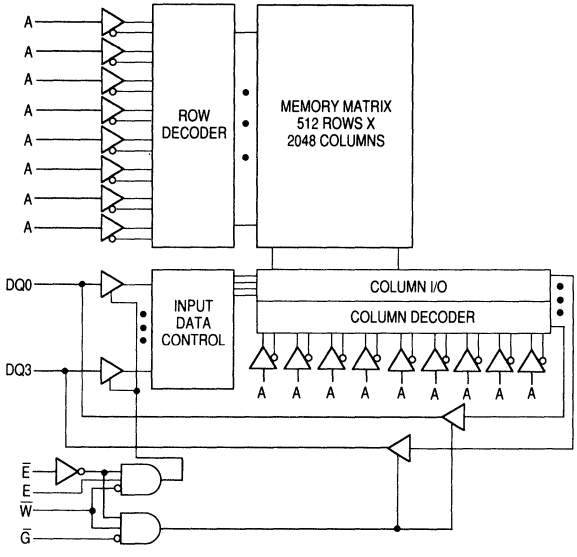
WJ PACKAGE
400 MIL SOJ
CASE TBD

DIP PACKAGE
TBD

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES	
A0–A16	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E}$, E	Chip Enable
DQ0–DQ7	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

All power supply and ground pins must be connected for proper operation of the device.

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

TRUTH TABLE

$\overline{E}$, E	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	Not Selected	I_{SB1}, I_{SB2}	High-Z	—
L	H	H	Read	I_{CCA}	High-Z	—
L	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	X	L	Write	I_{CCA}	D_{in}	Write Cycle

X = Don't Care

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high impedence circuits.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to 7.0	V
Voltage Relative to V_{SS} (For Any Pin Except V_{CC})	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation (T_A = 25°C)	P_D	1.1	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

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DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

*V_{IL} (min) = – 2.0 Vac (pulse width ≤ 20 ns); V_{IL} (min) = – 0.5 Vdc)

DC CHARACTERISTICS

Parameter		Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})		$I_{lkg(I)}$	—	± 1	µA
Output Leakage Current ($\overline{E}$ = V_{IL}, V_{out} = 0 to V_{CC})		$I_{lkg(O)}$	—	± 1	µA
AC Supply Current (I_{out} = 0 mA, V_{CC} = Max)	MCM6226-25: t_{AVAV} = 25 ns	I_{CCA}	—	160	mA
	MCM6226-30: t_{AVAV} = 30 ns		—	150	
TTL Standby Current ($\overline{E}$ = V_{IH}, No Restrictions on Other Inputs)		I_{SB1}	40	50	mA
CMOS Standby Current ($\overline{E}$ ≥ V_{CC} – 0.2 V, No Restrictions on Other Inputs)		I_{SB2}	20	30	mA
Output Low Voltage (I_{OL} = + 8.0 mA)		V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)		V_{OH}	2.4	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Max	Unit
Input Capacitance	(All Inputs Except $\overline{E}$, E, and DQ)	C_{in}	6	pF
	$\overline{E}$, E		7	
Input/Output Capacitance	DQ	$C_{I/O}$	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 5 ns

Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

READ CYCLE TIMING (See Note 1)

Parameter	Symbol		MCM6226-25		MCM6226-30		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	—	25	—	30	ns	2
Address Access Time	t_{AVQV}	t_{AA}	—	25	—	30	ns	
Enable Access Time	t_{ELQV}	t_{ACS}	—	25	—	30	ns	
Output Enable Access Time	t_{GLQV}	t_{OE}	—	12	—	15	ns	
Output Hold from Address Change	t_{AXQX}	t_{OH}	5	—	5	—	ns	
Enable Low to Output Active	t_{ELQX}	t_{CLZ}	4	—	4	—	ns	3, 4, 5
Output Enable to Output Active	t_{GLQX}	t_{OLZ}	0	—	0	—	ns	3, 4, 5
Enable High to Output High-Z	t_{EHQZ}	t_{CHZ}	0	10	0	12	ns	3, 4, 5
Output Enable High to Output High-Z	t_{GHQZ}	t_{OHZ}	0	10	0	12	ns	3, 4, 5
Power Up Time	t_{ELICCH}	t_{PU}	0	—	0	—	ns	
Power Down Time	t_{EHICCL}	t_{PD}	—	25	—	30	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transitioning address.
3. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} min, and t_{GHQZ} max is less than t_{GHQX} min, both for a given device and from device to device.
4. Transition is measured + 500 mV from steady-state voltage with load of Figure 1B.
5. This parameter is sampled and not 100% tested.
6. Device is continuously selected ($\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}).
7. Addresses valid prior to or coincident with $\overline{E}$ going low.

AC TEST LOADS

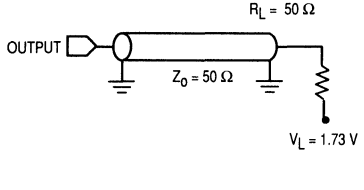


Figure 1A

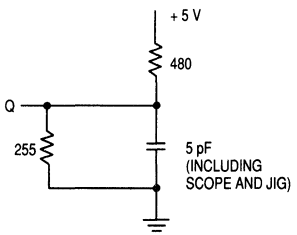
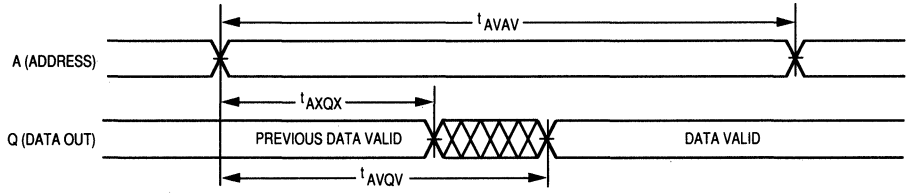


Figure 1B

TIMING LIMITS

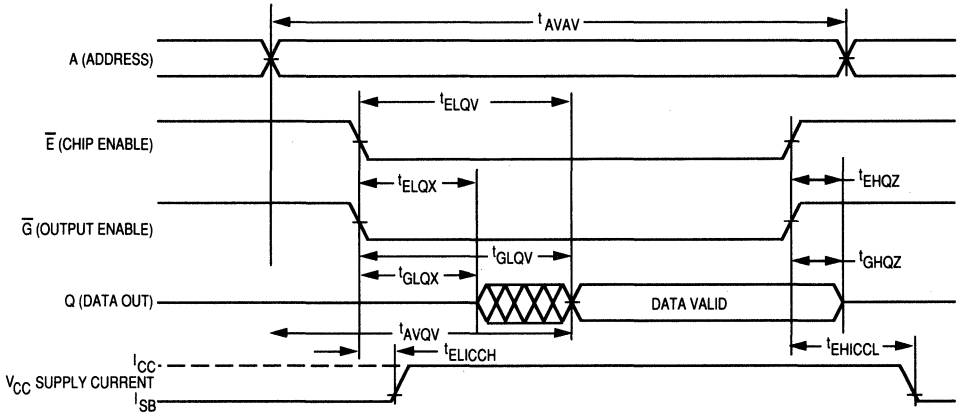
The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the module point of view. Thus, the access time is shown as a maximum since the module never provides data later than that time.

READ CYCLE 1 (See Note)



NOTE: Device is continuously selected ($\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$).

READ CYCLE 2 (See Note)



NOTE: Addresses valid prior to or coincident with $\overline{E}$ going low.

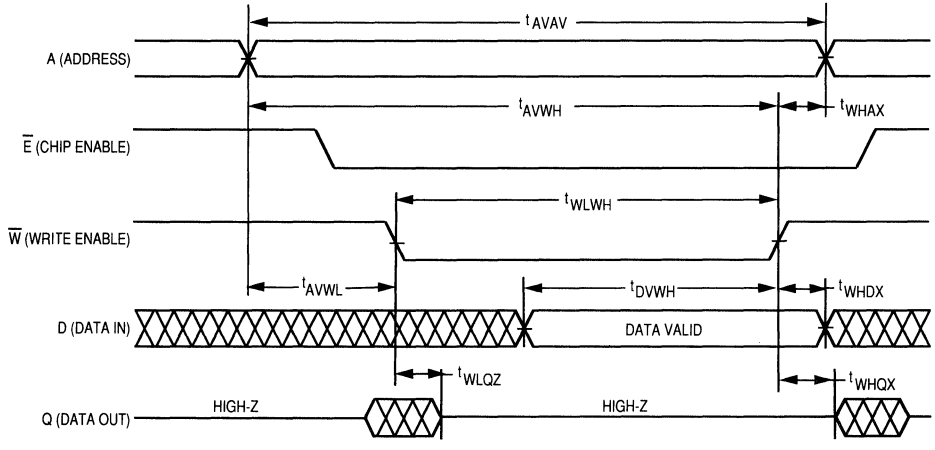
WRITE CYCLE 1 ($\overline{W}$ Controlled, See Note 1)

Parameter	Symbol		MCM6226-25		MCM6226-30		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	25	—	30	—	ns	2
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	20	—	25	—	ns	
Write Pulse Width	t_{WLWH}	t_{WP}	20	—	25	—	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	10	—	15	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	—	0	—	ns	
Write Low to Data High-Z	t_{WLQZ}	t_{WZ}	0	10	0	12	ns	3, 4, 5
Wirte High to Output Active	t_{WHQX}	t_{OW}	4	—	4	—	ns	3, 4, 5
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. All write cycle timing is referenced from the last valid address to the first transitioning address.
3. Transition is measured + 500 mV from steady-state voltage with load of Figure 1B.
4. This parameter is sampled and not 100% tested.
5. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min both for a given device and from device to device.

7

WRITE CYCLE 1



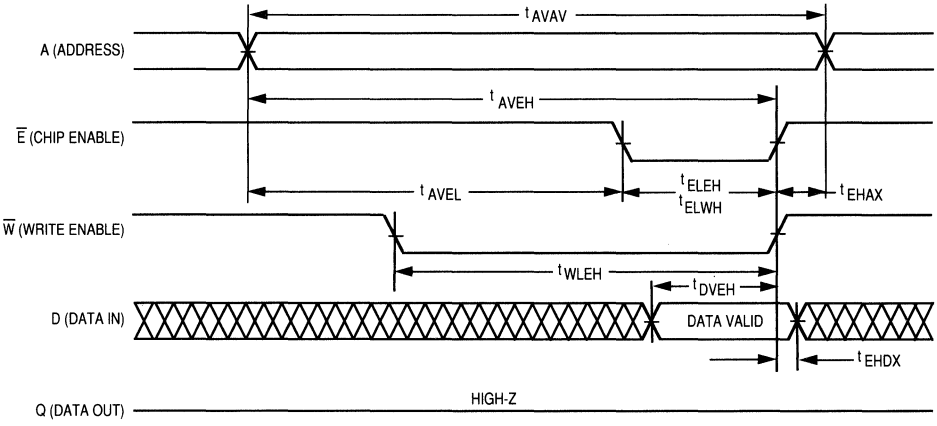
WRITE CYCLE 2 ($\overline{E}$ Controlled, See Note 1)

Parameter	Symbol		MCM6226-25		MCM62226-30		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	25	—	30	—	ns	2
Address Setup Time	t_{AVEL}	t_{AS}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	20	—	25	—	ns	
Enable to End of Write	t_{ELEH}	t_{CW}	20	—	25	—	ns	3, 4
Enable to End of Write	t_{ELWH}	t_{CW}	20	—	25	—	ns	
Write Pulse Width	t_{WLEH}	t_{WP}	20	—	25	—	ns	
Data Valid to End of Write	t_{DVEH}	t_{DW}	10	—	12	—	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	—	0	—	ns	

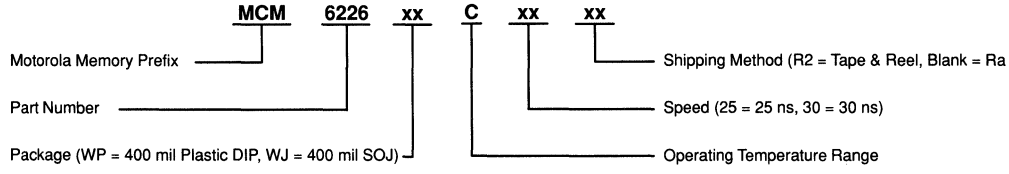
NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. All write cycle timing is referenced from the last valid address to the first transitioning address.
3. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
4. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

7

WRITE CYCLE 2



ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers – MCM6226WPC25 MCM6226WJC25 MCM6226WJC25R2
MCM6226WPC30 MCM6226WJC30 MCM6226WJC30R2

MCM6228

Product Preview

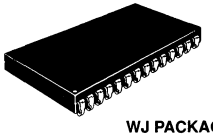
256K × 4 Bit Static Random Access Memory

The MCM6228 is a 1,048,576 bit static random-access memory organized as 262,144 words of 4 bits, fabricated using high-performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

The MCM6228 is equipped with both chip enable ($\overline{E}$) and output enable ($\overline{G}$) inputs, allowing for greater system flexibility. Either input, when high, will force the outputs to high impedance.

The MCM6228 is available in a 400 mil, 28 lead plastic dual-in-line package or a 400 mil, 28 lead plastic SOJ package with the JEDEC standard pinout.

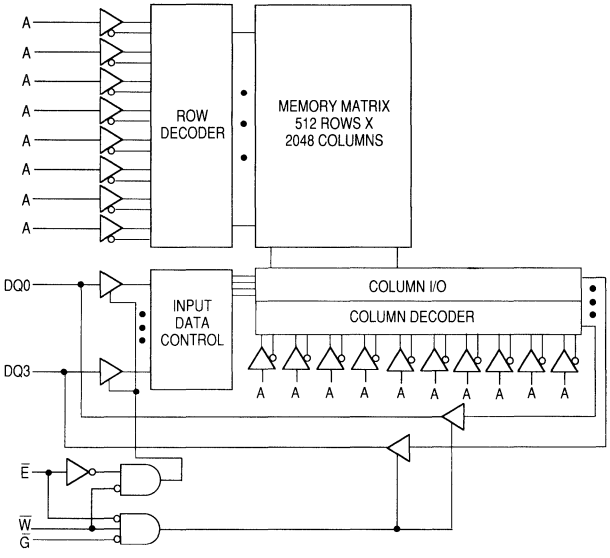
- Single 5 V ± 10% Power Supply
- Fast Access Time: 25, 30 ns
- Equal Address and Chip Enable Access Time
- Three-State Outputs
- Fully TTL Compatible
- Power Operation: 160 mA Maximum, Active AC (MCM6228-25)
- High Board Density SOJ Package Available



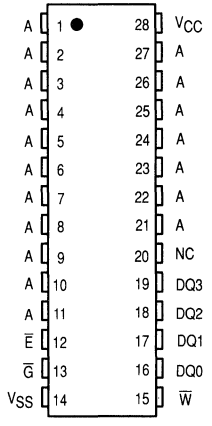
WJ PACKAGE
400 MIL SOJ
CASE 810

DIP PACKAGE
TBD

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN NAMES	
A0–A17	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E}$	Chip Enable
DQ0–DQ3	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground

All power supply and ground pins must be connected for proper operation of the device.

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This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	Not Selected	I_{ISB1}, I_{SB2}	High-Z	—
L	H	H	Read	I_{CCA}	High-Z	—
L	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	X	L	Write	I_{CCA}	D_{in}	Write Cycle

X = Don't Care

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high impedence circuits.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to 7.0	V
Voltage Relative to V_{SS} (For Any Pin Except V_{CC})	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation (T_A = 25°C)	P_D	1.1	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

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DC OPERATING CONDITIONS AND CHARACTERISTICS
(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

*V_{IL} (min) = – 2.0 Vac (pulse width ≤ 20 ns); V_{IL} (min) = – 0.5 Vdc)

DC CHARACTERISTICS

Parameter		Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})		$I_{lkg(I)}$	—	± 1	µA
Output Leakage Current ($\overline{E}$ = V_{IL}, V_{out} = 0 to V_{CC})		$I_{lkg(O)}$	—	± 1	µA
AC Supply Current (I_{out} = 0 mA, V_{CC} = Max)	MCM6228-25: t_{AVAV} = 25 ns	I_{CCA}	—	160	mA
	MCM6228-30: t_{AVAV} = 30 ns		—	150	
TTL Standby Current ($\overline{E}$ = V_{IH}, No Restrictions on Other Inputs)		I_{SB1}	40	50	mA
CMOS Standby Current ($\overline{E}$ ≥ V_{CC} – 0.2 V, No Restrictions on Other Inputs)		I_{SB2}	20	30	mA
Output Low Voltage (I_{OL} = + 8.0 mA)		V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)		V_{OH}	2.4	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Max	Unit
Input Capacitance	(All Inputs Except $\overline{E}$ and DQ)	C_{in}	6	pF
	$\overline{E}$		7	
Input/Output Capacitance	DQ	$C_{I/O}$	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 5 ns

Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

READ CYCLE TIMING (See Note 1)

Parameter	Symbol		MCM6228-25		MCM6228-30		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	—	25	—	30	ns	2
Address Access Time	t_{AVQV}	t_{AA}	—	25	—	30	ns	
Enable Access Time	t_{ELQV}	t_{ACS}	—	25	—	30	ns	
Output Enable Access Time	t_{GLQV}	t_{OE}	—	12	—	15	ns	
Output Hold from Address Change	t_{AXQX}	t_{OH}	5	—	5	—	ns	
Enable Low to Output Active	t_{ELQX}	t_{CLZ}	4	—	4	—	ns	3, 4, 5
Output Enable to Output Active	t_{GLQX}	t_{OLZ}	0	—	0	—	ns	3, 4, 5
Enable High to Output High-Z	t_{EHQZ}	t_{CHZ}	0	10	0	12	ns	3, 4, 5
Output Enable High to Output High-Z	t_{GHQZ}	t_{OHZ}	0	10	0	12	ns	3, 4, 5
Power Up Time	t_{ELICCH}	t_{PU}	0	—	0	—	ns	
Power Down Time	t_{EHICCL}	t_{PD}	—	25	—	30	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transitioning address.
3. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} min, and t_{GHQZ} max is less than t_{GHQX} min, both for a given device and from device to device.
4. Transition is measured + 500 mV from steady-state voltage with load of Figure 1B.
5. This parameter is sampled and not 100% tested.
6. Device is continuously selected ($\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}).
7. Addresses valid prior to or coincident with $\overline{E}$ going low.

AC TEST LOADS

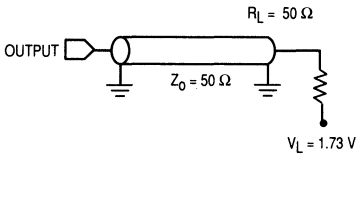


Figure 1A

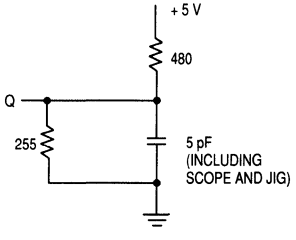


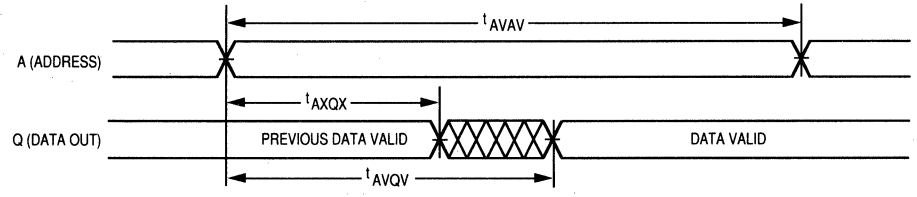
Figure 1B

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the module point of view. Thus, the access time is shown as a maximum since the module never provides data later than that time.

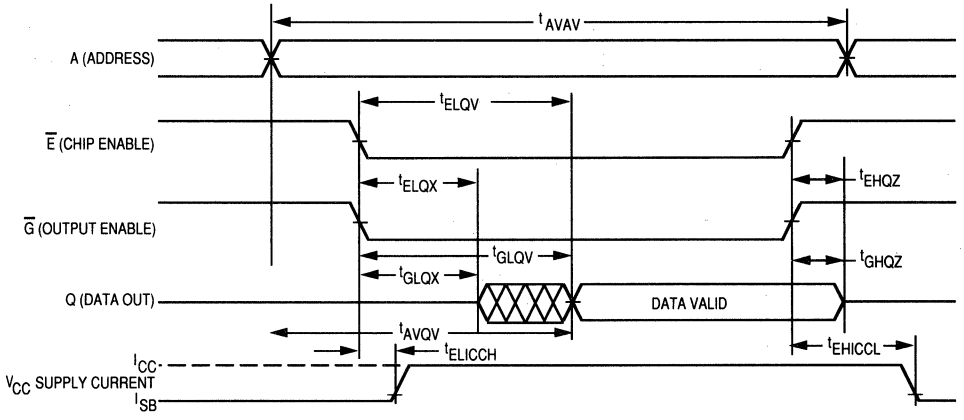
7

READ CYCLE 1 (See Note)



NOTE: Device is continuously selected ($\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$).

READ CYCLE 2 (See Note)



NOTE: Addresses valid prior to or coincident with $\overline{E}$ going low.

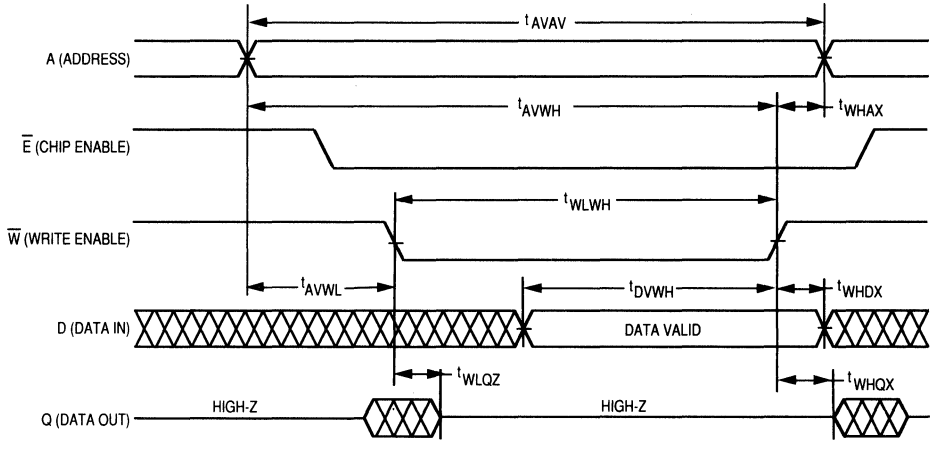
WRITE CYCLE 1 ($\overline{W}$ Controlled, See Note 1)

Parameter	Symbol		MCM6228-25		MCM6228-30		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	25	—	30	—	ns	2
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	20	—	25	—	ns	
Write Pulse Width	t_{WLWH}	t_{WP}	20	—	25	—	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	10	—	15	—	ns	
Data Hold TIme	t_{WHDX}	t_{DH}	0	—	0	—	ns	
Write Low to Data High-Z	t_{WLQZ}	t_{WZ}	0	10	0	12	ns	3, 4, 5
Wirte High to Output Active	t_{WHQX}	t_{OW}	4	—	4	—	ns	3, 4, 5
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. All write cycle timing is referenced from the last valid address to the first transitioning address.
3. Transition is measured + 500 mV from steady-state voltage with load of Figure 1B.
4. This parameter is sampled and not 100% tested.
5. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min both for a given device and from device to device.

7

WRITE CYCLE 1



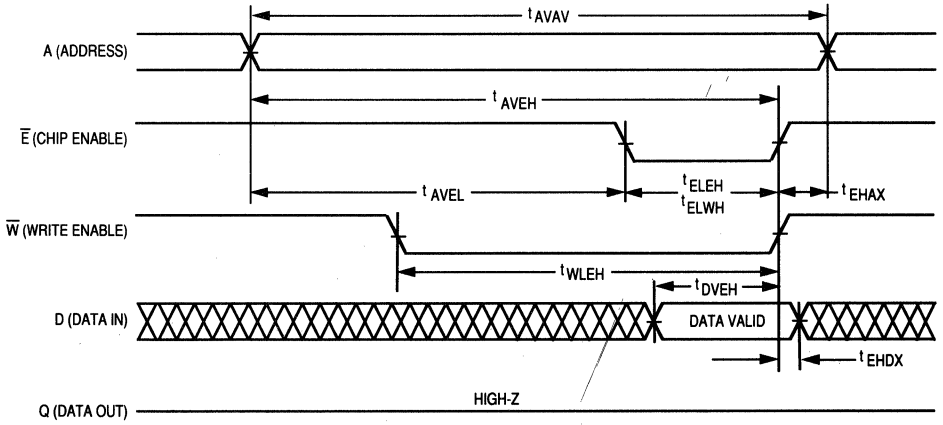
WRITE CYCLE 2 ($\overline{E}$ Controlled, See Note 1)

Parameter	Symbol		MCM6228-25		MCM62228-30		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	25	—	30	—	ns	2
Address Setup Time	t_{AVEL}	t_{AS}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	20	—	25	—	ns	
Enable to End of Write	t_{ELEH}	t_{CW}	20	—	25	—	ns	3, 4
Enable to End of Write	t_{ELWH}	t_{CW}	20	—	25	—	ns	
Write Pulse Width	t_{WLEH}	t_{WP}	20	—	25	—	ns	
Data Valid to End of Write	t_{DVEH}	t_{DW}	10	—	12	—	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. All write cycle timing is referenced from the last valid address to the first transitioning address.
3. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
4. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

7

WRITE CYCLE 2



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6228 xx C xx xx

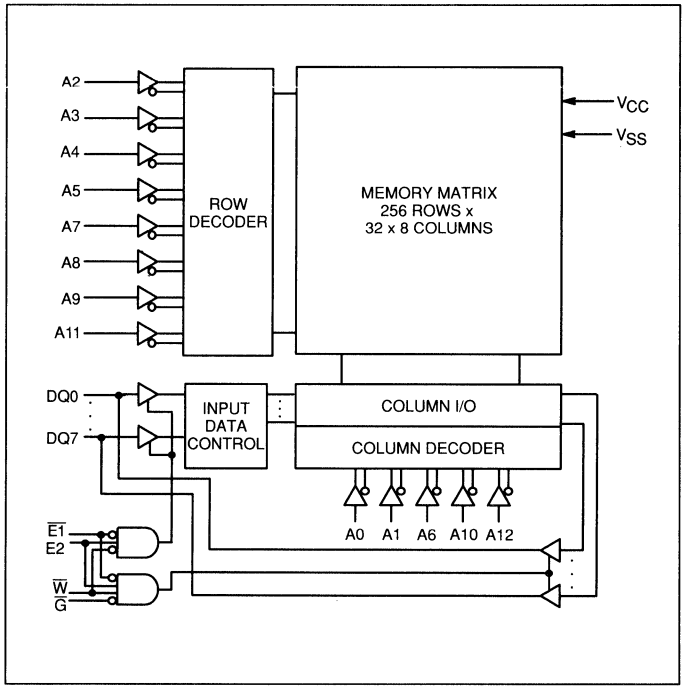
- MCM — Motorola Memory Prefix
- 6228 — Part Number
- xx — Package (WP = 400 mil Plastic DIP, WJ = 400 mil SOJ)
- C — Operating Temperature Range
- xx — Speed (25 = 25 ns, 30 = 30 ns)
- xx — Shipping Method (R2 = Tape & Reel, Blank = Rail)

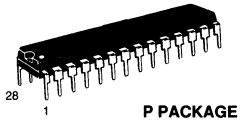
Full Part Numbers – MCM6228WPC25, MCM6228WPC30, MCM6228WJC25, MCM6228WJC30, MCM6228WJC25R2, MCM6228WJC30R2

8K x 8 Bit Fast Static RAM

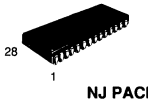
MCM6264-15, -20
See QuickRAM, Page 7-122

MCM6264C-10, -12
See QuickRAM II, Page 7-142



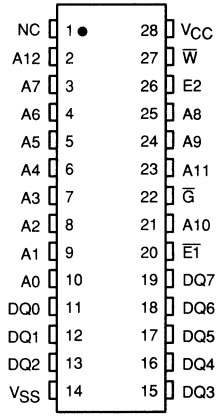


P PACKAGE
300 MIL PLASTIC
CASE 710B



NJ PACKAGE
300 MIL SOJ
CASE 810B

PIN ASSIGNMENT



PIN NAMES	
A0-A12 ..... Address Input	$\overline{E1}$, E2 ..... Chip Enable
DQ0–DQ7 ..... Data Input/Output	NC ..... No Connection
$\overline{W}$ ..... Write Enable	V_{CC} ..... +5 V Power Supply
$\overline{G}$ ..... Output Enable	V_{SS} ..... Ground

MCM6264 TRUTH TABLE (X = don't care)

$\overline{E1}$	E2	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	X	Not Selected	I_{SB1}, I_{SB2}	High-Z	—
X	L	X	X	Not Selected	I_{SB1}, I_{SB2}	High-Z	—
L	H	H	H	Output Disabled	I_{CCA}	High-Z	—
L	H	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	H	X	L	Write	I_{CCA}	High-Z	Write Cycle

7

MCM6264C

8K × 8 Bit Fast Static RAM

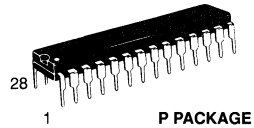
Industrial Temperature Range: –40 to 85°C

The MCM6264C is a 64,536 bit static random access memory organized as 8,192 words of 8 bits, fabricated using high-performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

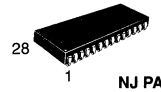
Chip enables ($\overline{E1}$ and E2) control the power-down feature. They are not clocks but rather chip controls that affect power consumption. In less than a cycle time after $\overline{E1}$ goes high (and E2 goes low), the part automatically reduces it power requirements and remains in this low-power standby mode as long as $\overline{E1}$ remains high and (E2 remains low). This feature provides significant system-level power savings. Another control feature, output enable ($\overline{G}$) allows access to the memory contents as fast as 10 ns (MCM6264C-20).

The MCM6264C is available in a 300 mil, 28 lead plastic dual-in-line package or a 300 mil, 28 lead plastic SOJ package with the JEDEC standard pinout.

- Single 5 V ± 10% Power Supply
- Fast Access Time: 20, 25 ns
- Chip Controls:
  Chip Enables ($\overline{E1}$ and E2) for Reduced-Power Standby Mode
  Output Enable ($\overline{G}$) for Fast Access to Data
- Three-State Outputs
- Fully TTL Compatible
- Power Operation: 140 mA Maximum, Active AC (MCM6264C-20)
- High Board Density SOJ Package Available

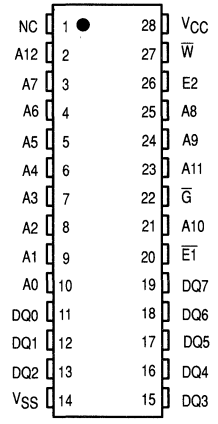


P PACKAGE
300 MIL PLASTIC
CASE 710B

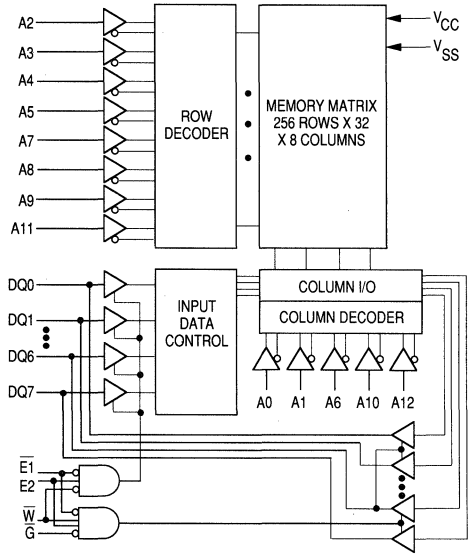


NJ PACKAGE
300 MIL SOJ
CASE 810B

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES	
A0–A12	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E1}$, E2	Chip Enable
DQ0–DQ7	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
NC	No Connection

All power supply and ground pins must be connected for proper operation of the device.

TRUTH TABLE

$\overline{E1}$	$\overline{E2}$	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	X	Not Selected	I_{SB1}, I_{SB2}	High-Z	—
X	L	X	X	Not Selected	I_{SB1}, I_{SB2}	High-Z	—
L	H	H	H	Read	I_{CCA}	High-Z	—
L	H	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	H	X	L	Write	I_{CCA}	D_{in}	Write Cycle

X = Don't Care

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to 7.0	V
Voltage Relative to V_{SS} (For Any Pin Except V_{CC})	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation (T_A = 25°C)	P_D	1.0	W
Temperature Under Bias	T_{bias}	– 50 to + 95	°C
Operating Temperature	T_A	– 40 to + 85	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

7

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = – 40 to + 85°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

*V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns); V_{IL} (min) = – 0.5 V dc)

DC CHARACTERISTICS

Parameter		Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})		$I_{lkg(I)}$	—	± 1	µA
Output Leakage Current ($\overline{E1}$ = V_{IL}, E2 = V_{IH}, V_{out} = 0 to V_{CC})		$I_{lkg(O)}$	—	± 1	µA
AC Supply Current (I_{out} = 0 mA, V_{CC} = Max)	t_{AVAV} = 20 ns t_{AVAV} = 25 ns	I_{CCA}	— —	140 130	mA
TTL Standby Current ($\overline{E1}$ = V_{IH}, E2 = V_{IL}, No Restrictions on Other Inputs)	t_{AVAV} = 20 ns t_{AVAV} = 25 ns	I_{SB1}	— —	40 35	mA
CMOS Standby Current ($\overline{E1}$ ≥ V_{CC} – 0.2 V, E2 ≤ 0.2 V, No Restrictions on Other Inputs)		I_{SB2}	—	20	mA
Output Low Voltage (I_{OL} = + 8.0 mA)		V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)		V_{OH}	2.4	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Max	Unit
Input Capacitance (All Inputs Except DQ)	C_{in}	6	pF
Input/Output Capacitance	$C_{I/O}$	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS
(V_{CC} = 5.0 V ± 10%, T_A = – 40 to + 85°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 5 ns

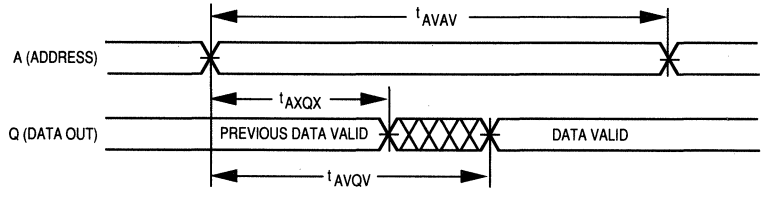
Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

READ CYCLE TIMING (See Notes 1 and 6)

Parameter	Symbol		MCM6264C-20		MCM6264C-25		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	20	—	25	—	ns	2
Address Access Time	t_{AVQV}	t_{AA}	—	20	—	25	ns	
Enable Access Time	t_{ELQV}	t_{ACS}	—	20	—	25	ns	
Output Enable Access Time	t_{GLQV}	t_{OE}	—	10	—	12	ns	
Output Hold from Address Change	t_{AXQX}	t_{OH}	4	—	4	—	ns	
Enable Low to Output Active	t_{ELQX}	t_{CLZ}	4	—	4	—	ns	3, 4, 5
Output Enable to Output Active	t_{GLQX}	t_{OLZ}	0	—	0	—	ns	3, 4, 5
Enable High to Output High-Z	t_{EHQZ}	t_{CHZ}	0	8	0	10	ns	3, 4, 5
Output Enable High to Output High-Z	t_{GHQZ}	t_{OHZ}	0	8	0	10	ns	3, 4, 5
Power Up Time	t_{ELICCH}	t_{PU}	0	—	0	—	ns	
Power Down Time	t_{EHICCL}	t_{PD}	—	20	—	25	ns	

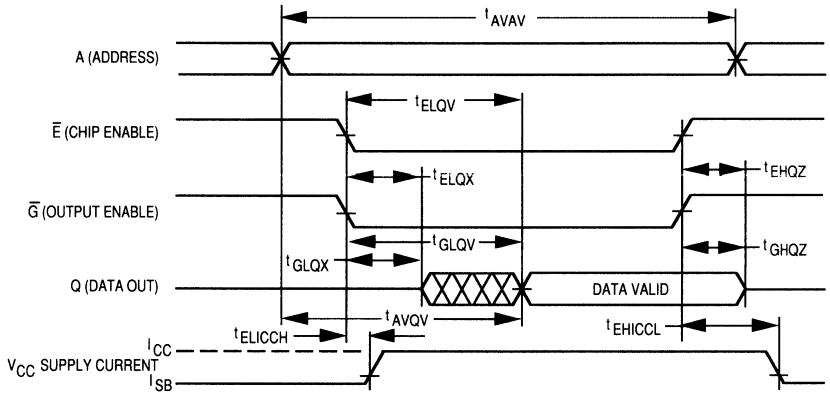
NOTES:
1. $\overline{W}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transitioning address.
3. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} min, and t_{GHQZ} max is less than t_{GHQX} min, both for a given device and from device to device.
4. Transition is measured + 500 mV from steady-state voltage with load of Figure 1B.
5. This parameter is sampled and not 100% tested.
6. $\overline{E1}$ and E2 are both represented by $\overline{E}$ in this data sheet. E2 is opposite polarity to $\overline{E1}$.

READ CYCLE 1 (See Notes)



NOTES:
1. Device is continuously selected ($\overline{E1}$ = V_{IL}, E2 = V_{IH}, G = V_{IL}).
2. Addresses valid prior to or coincident with $\overline{E1}$ going low (and E2 going high).

READ CYCLE 2 (See Notes)



NOTES:
1. Addresses valid prior to or coincident with $\overline{E1}$ going low (and E2 going high).
2. $\overline{E1}$ and E2 are both represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E1}$.

7

AC TEST LOADS

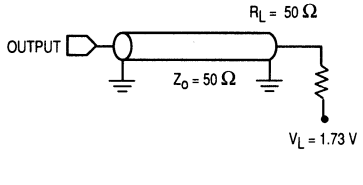


Figure 1A

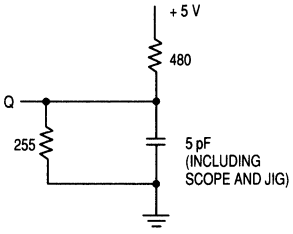


Figure 1B

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the module point of view. Thus, the access time is shown as a maximum since the module never provides data later than that time.

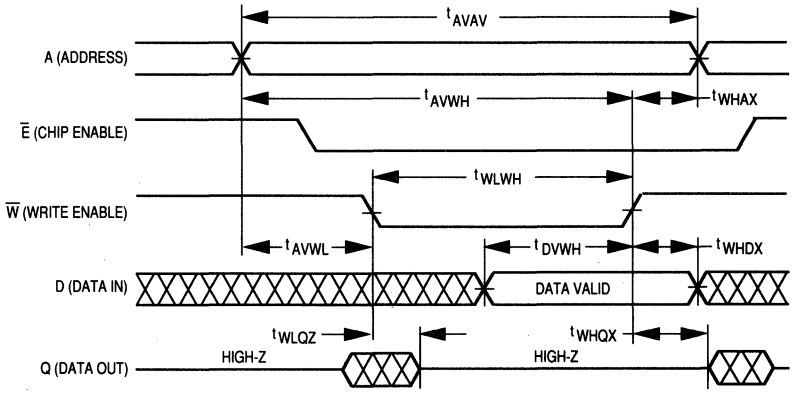
WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 6)

Parameter	Symbol		MCM6264C-20		MCM6264C-25		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	20	—	25	—	ns	2
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	15	—	20	—	ns	
Write Pulse Width	t_{WLWH}	t_{WP}	15	—	20	—	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	8	—	10	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	—	0	—	ns	
Write Low to Data High-Z	t_{WLQZ}	t_{WZ}	0	8	0	10	ns	3, 4, 5
Write High to Output Active	t_{WHQX}	t_{OW}	4	—	4	—	ns	3, 4, 5
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E1}$ low (and E2 high) and $\overline{W}$ low.
2. All write cycle timing is referenced from the last valid address to the first transitioning address.
3. Transition is measured + 500 mV from steady-state voltage with load of Figure 1B.
4. This parameter is sampled and not 100% tested.
5. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min both for a given device and from device to device.
6. $\overline{E1}$ and E2 are both represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E1}$.

7

WRITE CYCLE 1



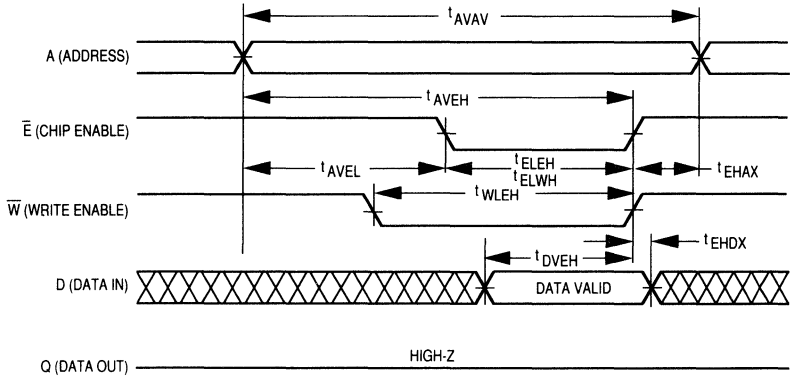
WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 5)

Parameter	Symbol		MCM6264C-20		MCM6264C-25		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	20	—	25	—	ns	2
Address Setup Time	t_{AVEL}	t_{AS}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	15	—	20	—	ns	
Enable to End of Write	t_{ELEH}	t_{CW}	12	—	15	—	ns	3,4
Enable to End of Write	t_{ELWH}	t_{CW}	12	—	15	—	ns	
Write Pulse Width	t_{WLEH}	t_{WP}	12	—	15	—	ns	
Data Valid to End of Write	t_{DVEH}	t_{DW}	8	—	10	—	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	—	0	—	ns	
Write Receovery Time	t_{EHAX}	t_{WR}	0	—	0	—	ns	

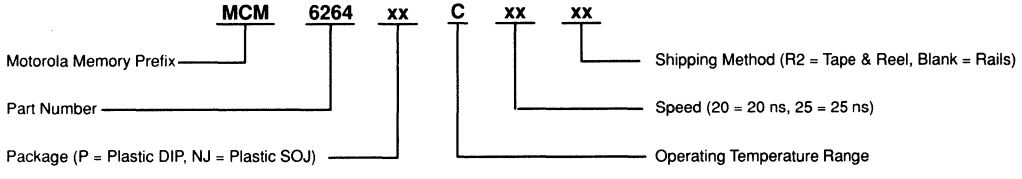
NOTES:
1. A write occurs during the overlap of $\overline{E1}$ low (and E2 high) and $\overline{W}$ low.
2. All write cycle timing is referenced from the last valid address to the first transitioning address.
3. If $\overline{E1}$ goes low (and E2 goes high) coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
4. If $\overline{E1}$ goes high (and E2 goes low) coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.
5. $\overline{E1}$ and E2 are both represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E1}$.

7

WRITE CYCLE 2



ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers – MCM6264PC20 MCM6264NJC20 MCM6264NJC20R2
MCM6264PC25 MCM6264NJC25 MCM6264NJC25R2

MCM6264D

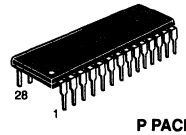
8K × 8 Bit Fast Static RAM

The MCM6264D is a 65,536 bit static random access memory organized as 8,192 words of 8 bits, fabricated using high-performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

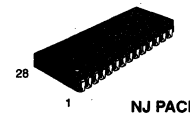
Chip enables ($\overline{E1}$ and E2) control the power-down feature. They are not clocks but rather chip controls that affect power consumption. In less than a cycle time after $\overline{E1}$ goes high (and E2 goes low), the part automatically reduces it power requirements and remains in this low-power standby mode as long as $\overline{E1}$ remains high and (E2 remains low). This feature provides significant system-level power savings.

The MCM6264D is available in a 300 mil, 28 lead plastic dual-in-line package or a 300 mil, 28 lead plastic SOJ package with the JEDEC standard pinout.

- Single 5 V ± 10% Power Supply
- Fast Access Time: 20, 25, 35, 45 ns
- Chip Controls:
  - Chip Enables ($\overline{E1}$ and E2) for Reduced-Power Standby Mode
  - Output Enable ($\overline{G}$) Feature for Increased System Flexibility and to Eliminate Bus Contention Problems
- Three-State Outputs
- Fully TTL Compatible
- Power Operation: 120, 100, 90, 80 mA (Maximum)
- High Board Density SOJ Package Available
- Also Available in Industrial Temperature Range as MCM6264D-C

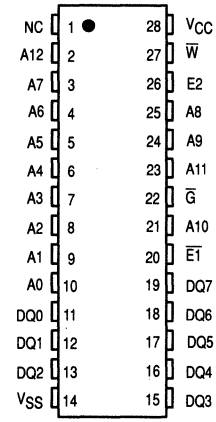


P PACKAGE
300 MIL PLASTIC
CASE 710B

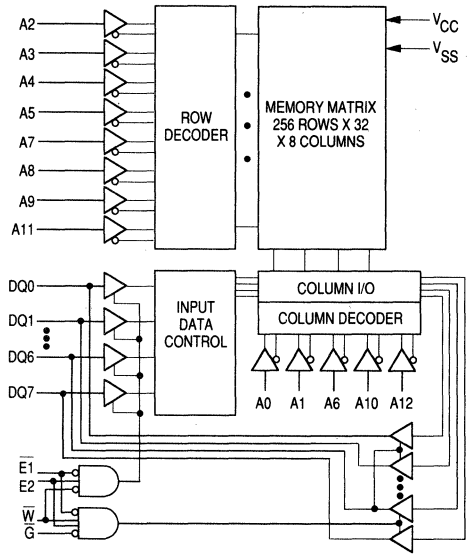


NJ PACKAGE
300 MIL SOJ
CASE 810B

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES	
A0–A12	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E1}$, E2	Chip Enable
DQ0–DQ7	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
NC	No Connection

All power supply and ground pins must be connected for proper operation of the device.

TRUTH TABLE

$\overline{E1}$	E2	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	X	Not Selected	I_{SB1}, I_{SB2}	High-Z	—
X	L	X	X	Not Selected	I_{SB1}, I_{SB2}	High-Z	—
L	H	H	H	Read	I_{CCA}	High-Z	—
L	H	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	H	X	L	Write	I_{CCA}	D_{in}	Write Cycle

X = Don't Care

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	− 0.5 to 7.0	V
Voltage Relative to V_{SS} (For Any Pin Except V_{CC})	V_{in}, V_{out}	− 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation (T_A = 25°C)	P_D	1.0	W
Temperature Under Bias	T_{bias}	− 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	− 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedence circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

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DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	– 0.3*	—	0.8	V

*V_{IL} (min) = – 0.3 V dc; V_{IL} (min) = – 3.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter		Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})		$I_{lkg(I)}$	—	± 1	μA
Output Leakage Current ($\overline{E1}$ = V_{IL}, E2 = V_{IH}, V_{out} = 0 to V_{CC})		$I_{lkg(O)}$	—	± 1	μA
AC Supply Current (I_{out} = 0 mA, V_{CC} = Max)	t_{AVAV} = 20 ns	I_{CCA}	—	120	mA
	t_{AVAV} = 25 ns		—	100	
	t_{AVAV} = 35 ns			90	
	t_{AVAV} = 45 ns			80	
TTL Standby Current ($\overline{E1}$ = V_{IH}, E2 = V_{IL}, No Restrictions on Other Inputs)		I_{SB1}	—	10	mA
CMOS Standby Current ($\overline{E1}$ ≥ V_{CC} – 0.2 V, E2 ≤ 0.2 V, No Restrictions on Other Inputs)		I_{SB2}	—	5	mA
Output Low Voltage (I_{OL} = + 8.0 mA)		V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)		V_{OH}	2.4	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Max	Unit
Input Capacitance (All Inputs Except DQ)	C_{in}	6	pF
Input/Output Capacitance	$C_{I/O}$	8	pF

AC TEST LOAD

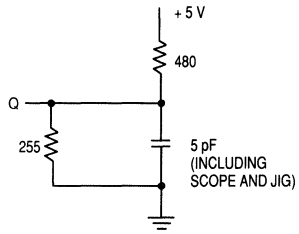


Figure 1

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the module point of view. Thus, the access time is shown as a maximum since the module never provides data later than that time.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 5 ns

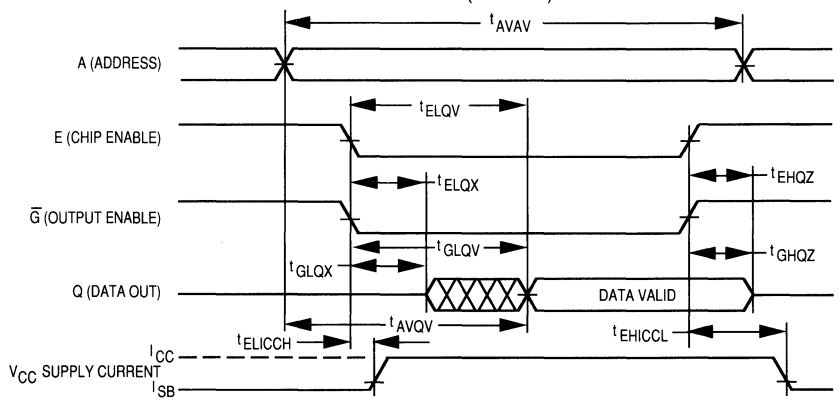
Output Timing Measurement Reference Level ..... 0.8 and 2.0 V
Output Load ..... See Figure 1 Unless Otherwise Noted

READ CYCLE TIMING (See Note 1)

Parameter	Symbol		MCM6264D-20		MCM6264D-25		MCM6264D-35		MCM6264D-45		Unit	Notes
	Std.	Alt.	Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	20	—	25	—	35	—	45	—	ns	
Address Access Time	t_{AVQV}	t_{AA}	—	20	—	25	—	35	—	45	ns	
Enable Access Time	t_{ELQV}	t_{ACS}	—	20	—	25	—	35	—	45	ns	4
Output Enable Access Time	t_{GLQV}	t_{OE}	—	10	—	10	—	15	—	20	ns	
Output Hold from Address Change	t_{AXQX}	t_{OH}	4	—	4	—	5	—	5	—	ns	
Enable Low to Output Active	t_{ELQX}	t_{CLZ}	4	—	4	—	5	—	5	—	ns	2, 3, 4
Output Enable to Output Active	t_{GLQX}	t_{OLZ}	2	—	2	—	0	—	0	—	ns	2, 3
Enable High to Output High-Z	t_{EHQZ}	t_{CHZ}	0	15	0	15	0	15	0	15	ns	2, 3, 4
Output Enable High to Output High-Z	t_{GHQZ}	t_{OHZ}	0	15	0	15	0	15	0	15	ns	2, 3
Power Up Time	t_{ELICCH}	t_{PU}	0	—	0	—	0	—	0	—	ns	2, 3, 4
Power Down Time	t_{EHICCL}	t_{PD}	—	20	—	25	0	35	0	45	ns	2, 3, 4

NOTES:
1. $\overline{W}$ is high for read cycle.
2. All high-Z and low-Z parameters are considered in a high or low impedance state when the output has made a 500 mV transition from previous steady state voltage.
3. These parameters are periodically sampled and not 100% tested.
4. $\overline{E1}$ and E2 are both represented by $\overline{E}$ in this data sheet. E2 is opposite polarity to $\overline{E1}$.

READ CYCLE (See Note)



NOTE: $\overline{W}$ is high for read cycle.

7

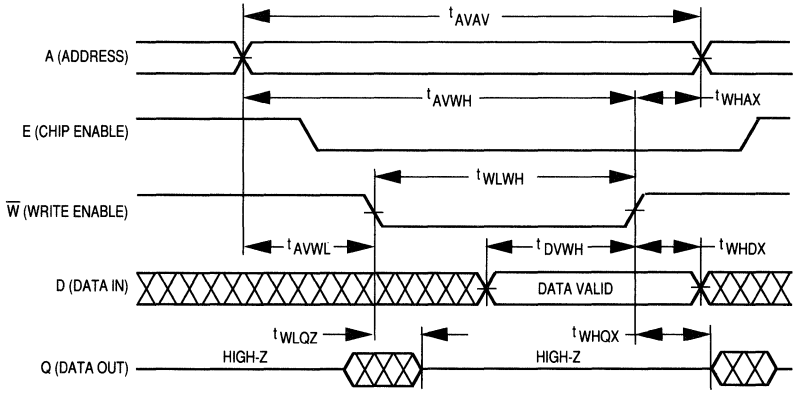
WRITE CYCLE 1 ($\overline{W}$ Controlled, See Note 1)

Parameter	Symbol		MCM6264D-20		MCM6264D-25		MCM6264D-35		MCM6264D-45		Unit	Notes
	Std.	Alt.	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	20	—	25	—	35	—	45	—	ns	
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	15	—	20	—	25	—	35	—	ns	
Write Pulse Width	t_{WLWH}	t_{WP}	15	—	15	—	20	—	25	—	ns	3
Data Valid to End of Write	t_{DVWH}	t_{DW}	10	—	10	—	15	—	20	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	—	0	—	0	—	0	—	ns	3
Write Low to Data High-Z	t_{WLQZ}	t_{WZ}	0	10	0	15	0	15	0	15	ns	4, 5
Write High to Output Active	t_{WHQX}	t_{OW}	4	—	4	—	5	—	5	—	ns	4, 5
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	0	—	0	—	ns	

7

NOTES:
1. A write cycle starts at the latest transition of a low $\overline{E1}$, low $\overline{W}$, or high E2. A write cycle ends at the earliest transition of a high $\overline{E1}$, high $\overline{W}$, or low E2.
2. If $\overline{W}$ goes low coincident with or prior to $\overline{E1}$ low or E2 high then the outputs will remain in a high impedance state.
3. During this time the output pins may be in the output stage. Signals of opposite phase to the outputs must not be applied at this time.
4. All high-Z and low-Z parameters are considered in a high or low impedance state when the output has made a 500 mV transition from the previous steady state voltage.
5. These parameters are sampled and not 100% tested.

WRITE CYCLE 1



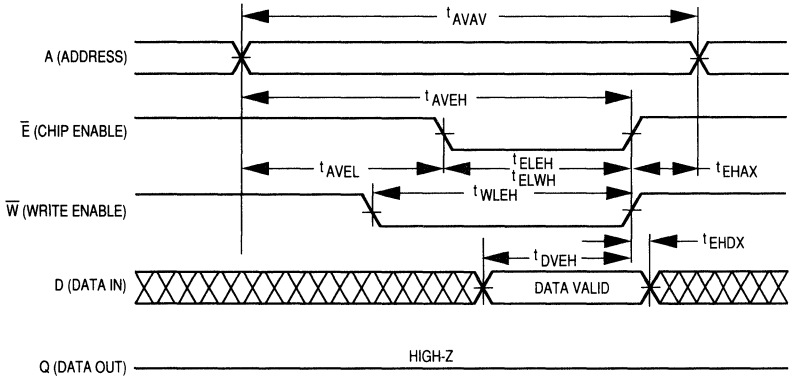
WRITE CYCLE 2 ($\overline{E}$ Controlled, See Note 1)

Parameter	Symbol		MCM6264D-20		MCM6264D-25		MCM6264D-35		MCM6264D-45		Unit	Notes
	Std.	Alt.	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	20	—	25	—	35	—	45	—	ns	
Address Setup Time	t_{AVEL}	t_{AS}	0	—	0	—	0	—	0	—	ns	2, 5
Address Valid to End of Write	t_{AVEH}	t_{AW}	15	—	20	—	25	—	35	—	ns	2, 5
Enable to End of Write	t_{ELEH}	t_{CW}	15	—	20	—	25	—	35	—	ns	2, 3, 5
Data Valid to End of Write	t_{DVEH}	t_{DW}	10	—	10	—	15	—	20	—	ns	2, 5
Data Hold Time	t_{EHDX}	t_{DH}	0	—	0	—	0	—	0	—	ns	2, 4, 5
Write Recovery Time	t_{EHAX}	t_{WR}	0	—	0	—	0	—	0	—	ns	2, 5

NOTES:
1. A write cycle starts at the latest transition of a low $\overline{E1}$, low $\overline{W}$, or high E2. A write cycle ends at the earliest transition of a high $\overline{E1}$, high $\overline{W}$, or low E2.
2. $\overline{E1}$ and E2 timings are identical when E2 signals are inverted.
3. If $\overline{W}$ goes low coincident with or prior to $\overline{E1}$ low or E2 high then the outputs will remain in a high impedance state.
4. During this time the output pins may be in the output stage. Signals of opposite phase to the outputs must not be applied at this time.
5. $\overline{E1}$ and E2 are both represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E1}$.

7

WRITE CYCLE 2



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6264D xx xx xx

- MCM — Motorola Memory Prefix
- 6264D — Part Number
- xx — Package (P = Plastic DIP, J = 400 mil Plastic SOJ, NJ = 300 mil Plastic SOJ)
- xx — Speed (20 = 20 ns, 25 = 25 ns, 35 = 35 ns, 45 = 45 ns)
- xx — Shipping Method (R2 = Tape & Reel, Blank = Rails)

Full Part Numbers –			
	MCM6264DP20	MCM6264DNJ20	MCM6264DNJ20R2
	MCM6264DP25	MCM6264DNJ25	MCM6264DNJ25R2
	MCM6264DP35	MCM6264DNJ35	MCM6264DNJ35R2
	MCM6264DP45	MCM6264DNJ45	MCM6264DNJ45R2

MCM6264D-C

8K × 8 Bit Fast Static RAM

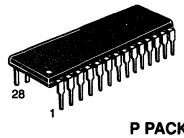
Industrial Temperature Range: –40 to 85°C

The MCM6264D-C is a 64,536 bit static random access memory organized as 8,192 words of 8 bits, fabricated using high-performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

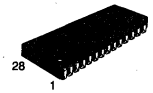
Chip enables ($\overline{E1}$ and E2) control the power-down feature. They are not clocks but rather chip controls that affect power consumption. In less than a cycle time after $\overline{E1}$ goes high (and E2 goes low), the part automatically reduces it power requirements and remains in this low-power standby mode as long as $\overline{E1}$ remains high and (E2 remains low). This feature provides significant system-level power savings.

The MCM6264D-C is available in a 300 mil, 28 lead plastic dual-in-line package or a 300, 28 lead plastic SOJ package with the JEDEC standard pinout.

- Single 5 V ± 10% Power Supply
- Fast Access Time: 25, 35, 45, 55 ns
- Chip Controls:
  - Chip Enables ($\overline{E1}$ and E2) for Reduced-Power Standby Mode
  - Output Enable ($\overline{G}$) Feature for Increased System Flexibility and to Eliminate Bus Contention Problems
- Three-State Outputs
- Fully TTL Compatible
- Low Power Operation: 115, 100, 90, 80 mA (Maximum)
- High Board Density SOJ Package Available
- Also Available in Commercial Temperature Range as MCM6264D

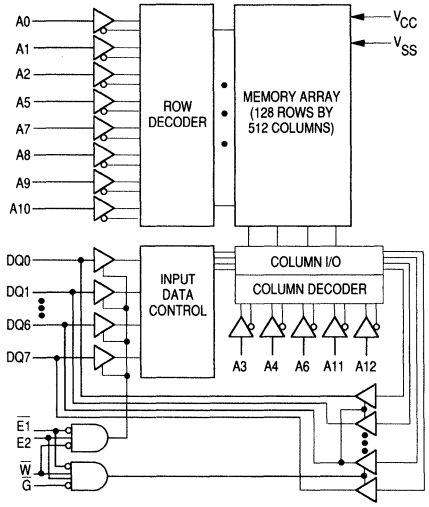


P PACKAGE
300 MIL PLASTIC
CASE 710B

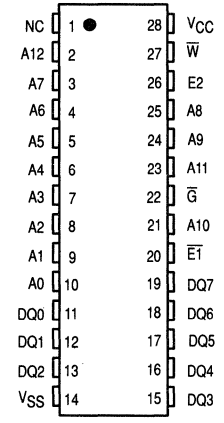


NJ PACKAGE
300 MIL SOJ
CASE 810B

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN NAMES

A0–A12	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E1}$, E2	Chip Enable
DQ0–DQ7	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
NC	No Connection

All power supply and ground pins must be connected for proper operation of the device.

TRUTH TABLE

$\overline{E1}$	E2	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	X	Not Selected	I_{ISB1}, I_{SB2}	High-Z	—
X	L	X	X	Not Selected	I_{ISB1}, I_{SB2}	High-Z	—
L	H	H	H	Read	I_{CCA}	High-Z	—
L	H	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	H	X	L	Write	I_{CCA}	D_{in}	Write Cycle

X = Don't Care

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedence circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to 7.0	V
Voltage Relative to V_{SS} (For Any Pin Except V_{CC})	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation (T_A = 25°C)	P_D	1.0	W
Temperature Under Bias	T_{bias}	– 50 to + 95	°C
Operating Temperature	T_A	– 40 to + 85	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

7

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = – 40 to + 85°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	– 0.3*	—	0.8	V

*V_{IL} (min) = – 0.3 Vdc; V_{IL} (min) = – 3.0 Vac (pulse width ≤ 20 ns); V_{IL} (min) = – 0.5 Vdc)

DC CHARACTERISTICS

Parameter		Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})		$I_{lkg(I)}$	—	± 1	µA
Output Leakage Current ($\overline{E1}$ = V_{IL}, E2 = V_{IH}, V_{out} = 0 to V_{CC})		$I_{lkg(O)}$	—	± 1	µA
AC Supply Current (I_{out} = 0 mA, V_{CC} = Max)	t_{AVAV} = 25 ns	I_{CCA}	—	115	mA
	t_{AVAV} = 35 ns		—	100	
	t_{AVAV} = 45 ns		—	90	
	t_{AVAV} = 55 ns		—	80	
TTL Standby Current ($\overline{E1}$ = V_{IH}, E2 = V_{IL}, No Restrictions on Other Inputs)		I_{SB1}	—	10	mA
CMOS Standby Current ($\overline{E1}$ ≥ V_{CC} – 0.2 V, E2 ≤ 0.2 V, No Restrictions on Other Inputs)		I_{SB2}	—	5	mA
Output Low Voltage (I_{OL} = + 8.0 mA)		V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)		V_{OH}	2.4	—	V

CAPACITANCE (f = 1.0 Mhz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Max	Unit
Input Capacitance (All Inputs Except DQ)	C_{in}	6	pF
Input/Output Capacitance	$C_{I/O}$	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 5 ns

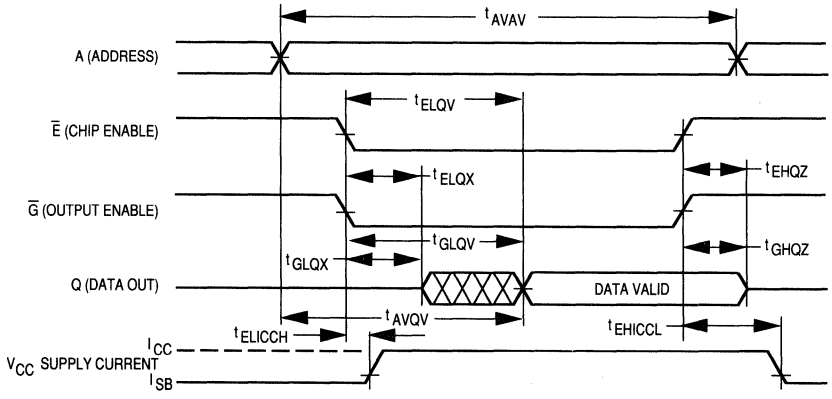
Output Timing Measurement Reference Level ..... 0.8 and 2.0 V
Output Load ..... See Figure 1

READ CYCLE TIMING (See Note 1)

Parameter	Symbol		MCM6264DC-25		MCM6264DC-35		MCM6264DC-45		MCM6264DC-55		Notes
	Std.	Alt.	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{AVAV}	t_{RC}	25	—	35	—	45	—	55	—	
Address Access Time	t_{AVQV}	t_{AA}	—	25	—	35	—	45	—	55	
Enable Access Time	t_{ELQV}	t_{ACS}	—	25	—	35	—	45	—	55	4
Output Enable Access Time	t_{GLQV}	t_{OE}	—	10	—	15	—	20	—	25	
Output Hold from Address Change	t_{AXQX}	t_{OH}	4	—	5	—	5	—	5	—	
Enable Low to Output Active	t_{ELQX}	t_{CLZ}	4	—	5	—	5	—	5	—	2, 3, 4
Output Enable to Output Active	t_{GLQX}	t_{OLZ}	2	—	2	—	2	—	2	—	2, 3
Enable High to Output High-Z	t_{EHQZ}	t_{CHZ}	0	15	0	15	0	15	0	15	2, 3, 4
Output Enable High to Output High-Z	t_{GHQZ}	t_{OHZ}	0	15	0	15	0	15	0	15	2, 3
Power Up Time	t_{ELICCH}	t_{PU}	0	—	0	—	0	—	0	—	2, 3, 4
Power Down Time	t_{EHICCL}	t_{PD}	—	25	—	35	0	45	0	55	2, 3, 4

NOTES:
1. $\overline{W}$ is high for read cycle.
2. All high-Z and low -Z parameters are considered in a high or low impedance state when the output has made a 500 mV transition from previous steady state voltage.
3. These parameters are periodically sampled and not 100% tested.
4. $\overline{E1}$ and E2 are both represented by $\overline{E}$ in this data sheet. E2 is opposite polarity to $\overline{E1}$.

READ CYCLE



NOTE: $\overline{W}$ is high for read cycle.

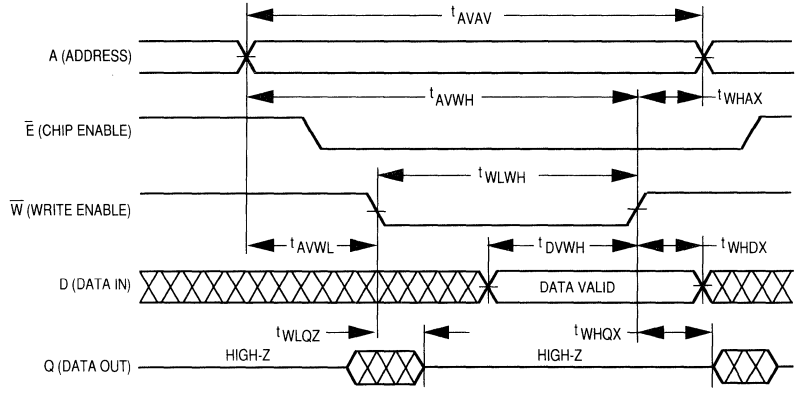
WRITE CYCLE 1 ($\overline{W}$ Controlled, See Note 1)

Parameter	Symbol		MCM6264DC-25		MCM6264DC-35		MCM6264DC-45		MCM6264DC-55		Unit	Notes
	Std.	Alt.	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	25	—	35	—	45	—	55	—	ns	
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	20	—	25	—	35	—	45	—	ns	
Write Pulse Width	t_{WLWH}	t_{WP}	15	—	20	—	25	—	30	—	ns	3
Data Valid to End of Write	t_{DVWH}	t_{DW}	10	—	15	—	20	—	25	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	—	0	—	0	—	0	—	ns	3
Write Low to Data High-Z	t_{WLQZ}	t_{WZ}	0	15	0	15	0	15	0	15	ns	4, 5
Wirte High to Output Active	t_{WHQX}	t_{OW}	4	—	5	—	5	—	5	—	ns	4, 5
Write Recover Time	t_{WHAX}	t_{WR}	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write cycle starts at the latest transition of a low $\overline{E1}$, low $\overline{W}$, or high E2. A write cycle ends at the earliest transition of a high $\overline{E1}$, high $\overline{W}$, or low E2.
2. If $\overline{W}$ goes low coincident with or prior to $\overline{E1}$ low or E2 high then the outputs will remain in a high impedance state.
3. During this time the output pins may be in the output stage. Signals of opposite phase to the outputs must not be applied at this time.
4. All high-Z and low-Z parameters are considered in a high or low impedance state when the output has made a 500 mV transition from the previous steady state voltage.
5. These parameters are sampled and not 100% tested.

7

WRITE CYCLE 1



AC TEST LOAD

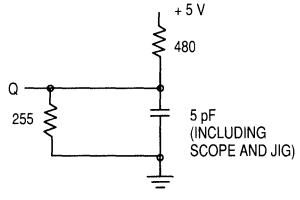


Figure 1

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the module point of view. Thus, the access time is shown as a maximum since the module never provides data later than that time.

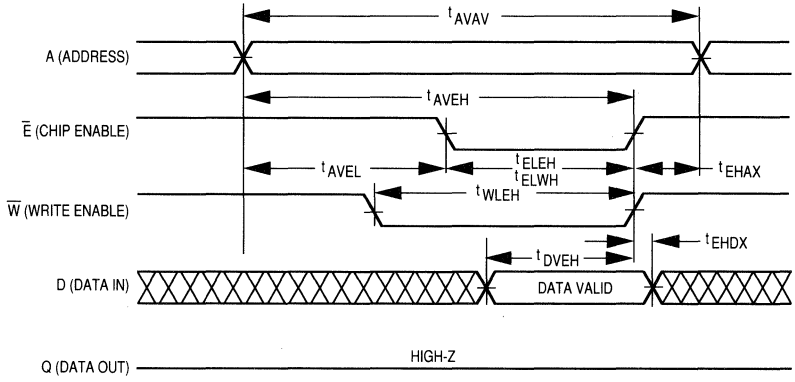
WRITE CYCLE 2 ($\overline{E}$ Controlled, See Note 1)

Parameter	Symbol		MCM6264DC-25		MCM6264DC-35		MCM6264DC-45		MCM6264DC-55		Unit	Notes
	Std.	Alt.	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	25	—	35	—	45	—	55	—	ns	
Address Setup Time	t_{AVEL}	t_{AS}	0	—	0	—	0	—	0	—	ns	2, 5
Address Valid to End of Write	t_{AVEH}	t_{AW}	20	—	25	—	35	—	45	—	ns	2, 5
Enable to End of Write	t_{ELEH}	t_{CW}	20	—	25	—	35	—	45	—	ns	2, 3, 5
Data Valid to End of Write	t_{DVEH}	t_{DW}	10	—	15	—	20	—	25	—	ns	2, 5
Data Hold Time	t_{EHDX}	t_{DH}	0	—	0	—	0	—	0	—	ns	2, 4, 5
Write Recover Time	t_{EHAX}	t_{WR}	0	—	0	—	0	—	0	—	ns	2, 5

NOTES:
1. A write cycle starts at the latest transition of a low $\overline{E1}$, low $\overline{W}$, or high E2. A write cycle ends at the earliest transition of a high $\overline{E1}$, high $\overline{W}$, or low E2.
2. $\overline{E1}$ and E2 timings are identical when E2 signals are inverted.
3. If $\overline{W}$ goes low coincident with or prior to $\overline{E1}$ low or E2 high then the outputs will remain in a high impedance state.
4. During this time the output pins maybe in the output stage. Signals of opposite phase to the outputs must not be applied at this time.
5. $\overline{E1}$ and E2 are both represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E1}$.

7

WRITE CYCLE 2



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6264D xx C xx xx

- Motorola Memory Prefix
- Part Number
- Package (P = Plastic DIP, J = 400 mil Plastic SOJ, NJ = 300 mil Plastic SOJ)
- Operating Temperature Range (C = –40° to 85°C, Blank = Commercial)
- Speed (25 = 25 ns, 35 = 35 ns, 45 = 45 ns, 55 = 55 ns)
- Shipping Method (R2 = Tape & Reel, Blank = Rails)

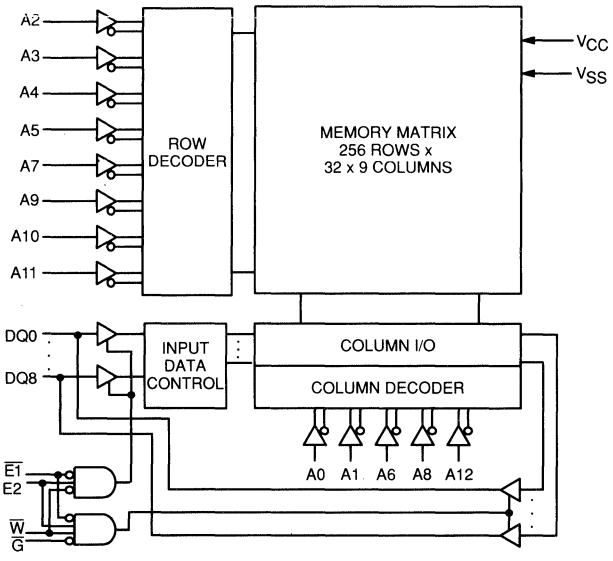
Full Part Numbers –

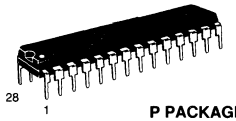
MCM6264DPC25	MCM6264DNJC25	MCM6264DNJC25R2
MCM6264DPC35	MCM6264DNJC35	MCM6264DNJC35R2
MCM6464DPC45	MCM6264DNJC45	MCM6264DNJC45R2
MCM6264DPC55	MCM6264DNJC55	MCM6264DNJC55R2

8K x 9 Bit Fast Static RAM

MCM6265-15, -20, -25
See QuickRAM, Page 7-122

MCM6265C-10, -12
See QuickRAM II, Page 7-142

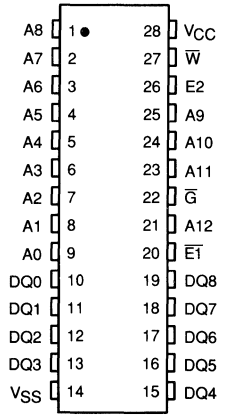




P PACKAGE
300 MIL PLASTIC
CASE 710B

NJ PACKAGE
300 MIL SOJ
CASE 810B

PIN ASSIGNMENT



PIN NAMES	
A0-A12 ..... Address Input	$\overline{E1}$, E2 ..... Chip Enable
DQ0–DQ8 ..... Data Input/Output	V_{CC} ..... +5 V Power Supply
$\overline{W}$ ..... Write Enable	V_{SS} ..... Ground
$\overline{G}$ ..... Output Enable	

MCM6265 TRUTH TABLE (X = don't care)

$\overline{E1}$	E2	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	X	Not Selected	I_{SB1}, I_{SB2}	High-Z	—
X	L	X	X	Not Selected	I_{SB1}, I_{SB2}	High-Z	—
L	H	H	H	Output Disabled	I_{CCA}	High-Z	—
L	H	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	H	X	L	Write	I_{CCA}	High-Z	Write Cycle

7

MCM6268
MCM6269

4K × 4 Bit Static Random Access Memory

The MCM6268 and MCM6269 are 16,384-bit static random access memories organized as 4096 words of 4 bits, fabricated using Motorola's high-performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides greater reliability. Fast access time makes this device suitable for cache and other sub-50 ns applications.

The MCM6268 uses a chip enable ($\overline{E}$) function which is not a clock. In less than a cycle time after $\overline{E}$ goes high, the part enters a low-power standby mode, remaining in that state until $\overline{E}$ goes low again. This device also incorporates internal power down circuitry that will reduce active current for less than 100% duty cycle applications. These features provide reduced system power requirements without degrading access time performance.

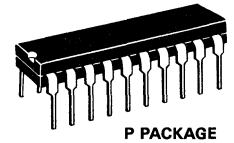
Similar in design to the Motorola MCM6268, the MCM6269 features an enhanced chip select circuit allowing access to data in as little as 10 ns.

Both devices are available in a 20 lead plastic dual-in-line package and feature the standard JEDEC pinout.

- Single 5 V Supply, ±10%
- 4K × 4 Bit Organization
- Fully Static—No Clock or Timing Strobes Necessary
- Three State Output
- Fully TTL Compatible
- Fast Access Time (Maximum) (xx = 68 or 69):

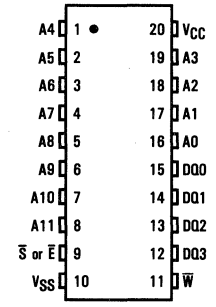
		MCM6268	MCM6269
	Address	Chip Enable	Chip Select
MCM62xxP20	20 ns	20 ns	10 ns
MCM62xxP25	25 ns	25 ns	12 ns
MCM62xxP35	35 ns	35 ns	15 ns
MCM6268P45	45 ns	45 ns	
MCM6268P55	55 ns	55 ns	

- Low Power Operation: 110 mA Maximum, Active AC



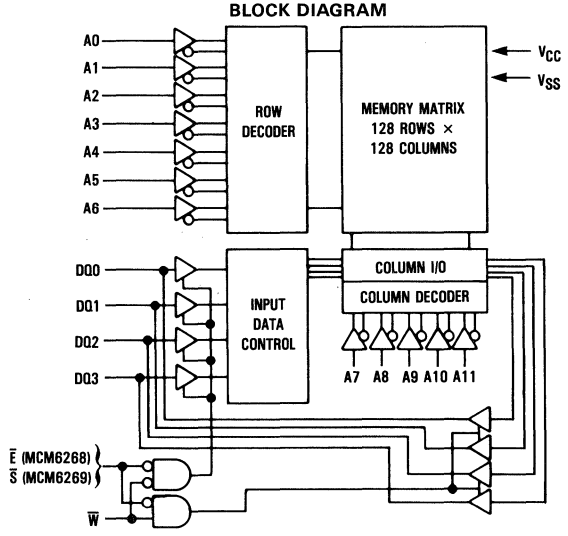
P PACKAGE
PLASTIC
CASE 738

PIN ASSIGNMENT



PIN NAMES	
A0-A11	Address Input
$\overline{W}$	Write Enable
$\overline{E}$ (MCM6268)	Chip Enable
$\overline{S}$ (MCM6269)	Chip Select
DQ0-DQ3	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

BLOCK DIAGRAM



TRUTH TABLE

$\overline{E}/\overline{S}$	$\overline{W}$	Mode	V_{CC} Current (MCM6268)	V_{CC} Current (MCM6269)	I/O Pin	Cycle
H	X	Not Selected	ISB1, ISB2	I_{CC}	High-Z	—
L	H	Read	I_{CC}	I_{CC}	D_{out}	Read Cycle
L	L	Write	I_{CC}	I_{CC}	D_{in}	Write Cycle

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC}+0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation (T_A=25°C)	P_D	1.0	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

7

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.0	—	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

*V_{IL} (min) = −0.5 V dc; V_{IL} (min) = −3.0 V ac (pulse width ≤20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in}=0 to V_{CC})	$I_{lkg(I)}$	—	±1.0	μA
Output Leakage Current ($\overline{E}$ or $\overline{S}$=V_{IH}, V_{out}=0 to V_{CC})	$I_{lkg(O)}$	—	±1.0	μA
AC Supply Current (I_{out}=0 mA) MCM6268/69-20, 25, 35	I_{CC}	—	110	mA
MCM6268-45, 55		—	80	
TTL Standby Current ($\overline{E}$=V_{IH}, No Restrictions on Other Inputs) (MCM6268)	I_{SB1}	—	20	mA
CMOS Standby Current ($\overline{E}$≥V_{CC}−0.2 V, No Restrictions on Other Inputs) MCM6268-20, 25, 35	I_{SB2}	—	15	mA
MCM6268-45, 55		—	2	
($\overline{S}$≥V_{CC}−0.2 V, V_{in}≤0.2 V, or ≥V_{CC}−0.2 V) (MCM6269)	I_{SB}	—	15	
Output Low Voltage (I_{OL}=8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH}=−4.0 mA)	V_{OH}	2.4	—	V

CAPACITANCE (f=1.0 MHz, dV=3.0 V, T_A=25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Capacitance All Inputs Except $\overline{E}$, $\overline{S}$	C_{in}	—	4	6	pF
$\overline{E}$, $\overline{S}$		—	5	7	
I/O Capacitance	$C_{I/O}$	—	5	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

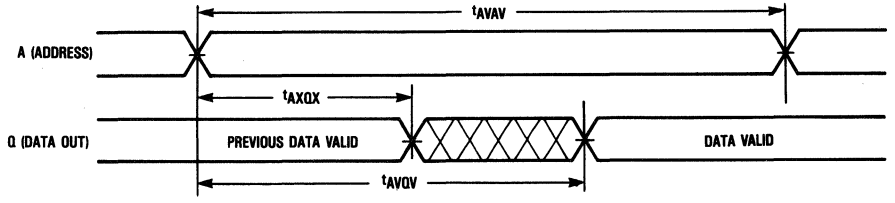
Input Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns
Output Reference Level . . . . . 1.5 V
Output Load . . . . . Figure 1A Unless Otherwise Noted

READ CYCLE (See Note 1)

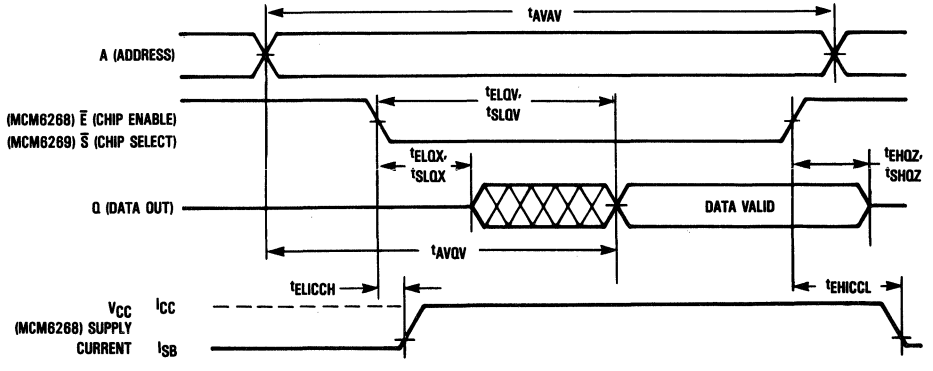
Parameter	Symbol		MCM6268P20 MCM6269P20		MCM6268P25 MCM6269P25		MCM6268P35 MCM6269P35		MCM6268P45		MCM6268P55		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	20	–	25	–	35	–	40	–	55	–	ns	2
Address Access Time	t_{AVQV}	t_{AA}	–	20	–	25	–	35	–	40	–	50	ns	
Enable Access Time (MCM6268)	t_{ELQV}	t_{ACS}	–	20	–	25	–	35	–	45	–	55	ns	
Select Access Time (MCM6269)	t_{SLQV}	t_{ACS}	–	10	–	12	–	15					ns	
Output Hold from Address Change	t_{AXQX}	t_{OH}	5	–	5	–	5	–	5	–	5	–	ns	
Enable Low to Output Active	t_{ELQX}	t_{LZ}	5	–	5	–	5	–	10	–	10	–	ns	3,4,5
Select Low to Output Active (MCM6269)	t_{SLQX}	t_{LZ}	5	–	5	–	5	–					ns	3,4,5
Enable High to Output High-Z	t_{EHQZ}	t_{HZ}	0	8	0	10	0	15	0	15	0	20	ns	3,4,5
Select High to Output High-Z (MCM6269)	t_{SHQZ}	t_{HZ}	0	8	0	10	0	15					ns	3,4,5
Power Up Time (MCM6268)	t_{ELICCH}	t_{PU}	0	–	0	–	0	–	0	–	0	–	ns	
Power Down Time (MCM6268)	t_{EHICCL}	t_{PD}	–	20	–	20	–	30	–	45	–	55	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transitioning address.
3. At any given voltage and temperature, t_{EHQZ} (or t_{SHQZ}) max, is less than t_{ELQX} (or t_{SLQX}) min, both for a given device and from device to device.
4. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B.
5. This parameter is sampled and not 100% tested.
6. Device is continuously selected ($\overline{E}$ or $\overline{S}$ = V_{IL}).
7. Addresses valid prior to or coincident with $\overline{E}$ or $\overline{S}$ going low.

READ CYCLE 1 (See Note 6 Above)



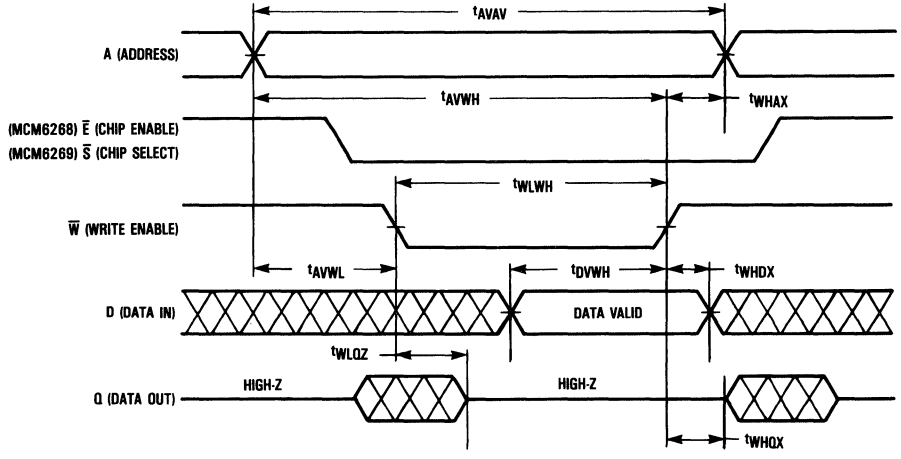
READ CYCLE 2 (See Note 7 Above)



WRITE CYCLE 1 ($\overline{W}$ Controlled, See Note 1)

Parameter	Symbol		MCM6268P20 MCM6269P20		MCM6268P25 MCM6269P25		MCM6268P35 MCM6269P35		MCM6268P45		MCM6268P55		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	20	–	25	–	35	–	40	–	50	–	ns	2
Address Setup Time	t_{AVWL}	t_{AS}	0	–	0	–	0	–	0	–	0	–	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	15	–	20	–	30	–	35	–	45	–	ns	
Write Pulse Width	t_{WLWH}	t_{WP}	15	–	20	–	25	–	35	–	45	–	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	10	–	10	–	15	–	15	–	20	–	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	–	0	–	0	–	0	–	0	–	ns	
Write Low to Output High-Z	t_{WLQZ}	t_{WZ}	0	8	0	10	0	15	0	20	0	25	ns	3,4,5
Write High to Output Active	t_{WHQX}	t_{OW}	5	–	5	–	5	–	5	–	5	–	ns	3,4,5
Write Recovery Time	t_{WHAX}	t_{WR}	0	–	0	–	0	–	0	–	0	–	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ or $\overline{S}$ low and $\overline{W}$ low.
2. All write cycle timing is referenced from the last valid address to the first transitioning address.
3. Transition is measured ±500 mV from steady-state voltage with load in Figure 1B.
4. Parameter is sampled and not 100% tested.
5. At any given voltage and temperature, t_{WLQZ} max, is less than t_{WHQX} min, both for a given device and from device to device.



AC TEST LOADS

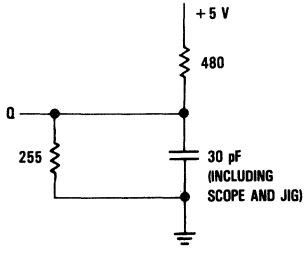


Figure 1A

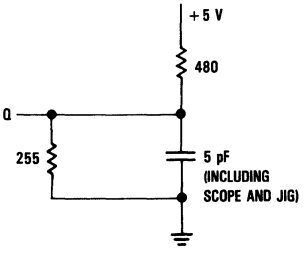


Figure 1B

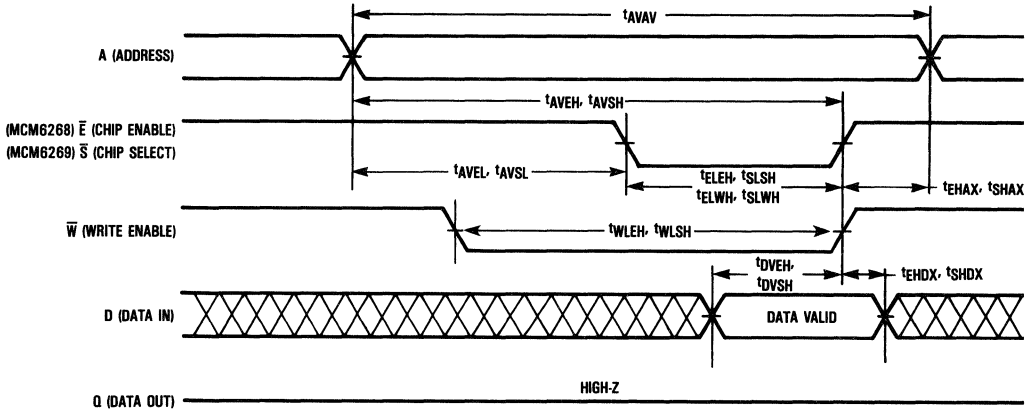
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

WRITE CYCLE 2 ($\overline{E}$, $\overline{S}$ Controlled; See Note 1)

Parameter	Symbol		MCM6268P20 MCM6269P20		MCM6268P25 MCM6269P25		MCM6268P35 MCM6269P35		MCM6268P45		MCM6268P55		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	20	–	25	–	35	–	40	–	50	–	ns	2
Address Setup Time	t_{AVEL}, t_{AVSL}	t_{AS}	0	–	0	–	0	–	0	–	0	–	ns	
Address Valid to End of Write	t_{AVEH}, t_{AVSH}	t_{AW}	15	–	20	–	30	–	35	–	45	–	ns	
Enable to End of Write (MCM6268)	t_{ELEH}	t_{CW}	15	–	20	–	30	–	35	–	45	–	ns	3,4
Select to End of Write (MCM6269)	t_{SLSH}	t_{CW}	15	–	20	–	30	–					ns	3,4
Enable to End of Write (MCM6268)	t_{ELWH}	t_{CW}	15	–	20	–	30	–	30	–	30	–	ns	
Select to End of Write (MCM6269)	t_{SLWH}	t_{CW}	15	–	20	–	30	–					ns	
Write Pulse Width	t_{WLEH}, t_{WLSH}	t_{WP}	15	–	20	–	25	–	30	–	30	–	ns	
Data Valid to End of Write	t_{DVEH}, t_{DVSH}	t_{DW}	10	–	10	–	15	–	15	–	20	–	ns	
Data Hold Time	t_{EHDX}, t_{SHDX}	t_{DH}	0	–	0	–	0	–	0	–	0	–	ns	
Write Recovery Time	t_{EHAX}, t_{SHAX}	t_{WR}	0	–	0	–	0	–	0	–	0	–	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ or $\overline{S}$ low and $\overline{W}$ low.
2. All write cycle timing is referenced from the last valid address to the first transitioning address.
3. If $\overline{E}$ or $\overline{S}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
4. If $\overline{E}$ or $\overline{S}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6268 or 6269 P XX

Motorola Memory Prefix — MCM

Part Number — 6268 or 6269

Speed (20 = 20 ns, 25 = 25 ns, 35 = 35 ns, 45 = 45 ns, 55 = 55 ns) — XX

Package (P = Plastic DIP) — P

Full Part Numbers — MCM6268P20, MCM6268P25, MCM6268P35, MCM6268P45, MCM6268P55, MCM6269P20, MCM6269P25, MCM6269P35

MCM6270

4K x 4 Bit Static RAM

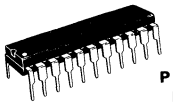
The MCM6270 is a 16,384-bit static random access memory organized as 4096 words of 4 bits, fabricated using Motorola's high-performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption for greater reliability.

The MCM6270 is equipped with both chip enable ($\overline{E}$) and output enable ($\overline{G}$) inputs, allowing for greater system flexibility. Either input, when high, will force the outputs to high impedance.

- Single 5 V Supply, ±10%
- Fully Static—No Clock or Timing Strobes Necessary
- Three-State Outputs
- Fully TTL Compatible
- Fast Access Time (Maximum):

	Address	Chip Enable	Output Enable
MCM6270-20	20 ns	20 ns	10 ns
MCM6270-25	25 ns	25 ns	12 ns
MCM6270-35	35 ns	35 ns	14 ns

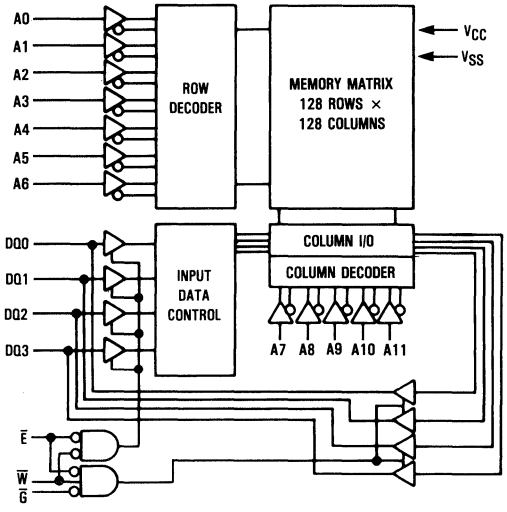
- Low Power Operation: 110 mA Maximum, Active AC
- Output Enable ($\overline{G}$) Feature for Increased System Flexibility and to Eliminate Bus Contention Problems



P PACKAGE
PLASTIC
CASE 736A

J PACKAGE
300 MIL SOJ
CASE 810A

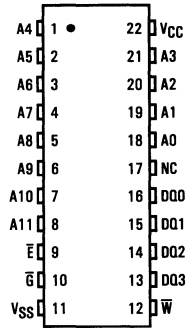
BLOCK DIAGRAM



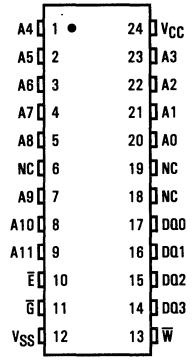
PIN NAMES	
A0-A11 . . . . . Address Input	$\overline{E}$ . . . . . Chip Enable
DQ0-DQ3 . Data Input/Output	V_{CC} . . . +5 V Power Supply
$\overline{W}$ . . . . . Write Enable	V_{SS} . . . . . Ground
$\overline{G}$ . . . . . Output Enable	NC . . . . . No Connection

PIN ASSIGNMENT

DUAL-IN-LINE



SMALL OUTLINE



7

TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	I/O Pin	Cycle
H	X	X	Not Selected	I_{SB}	High-Z	—
L	H	H	Read	I_{CCA}	High-Z	—
L	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	X	L	Write	I_{CCA}	D_{in}	Write Cycle

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage (V_{CC})	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC}+0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation (+25°C)	P_D	1.0	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

7

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.0	—	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

*V_{IL} (min) = −0.5 V dc; V_{IL} (min) = −3.0 V ac (pulse width ≤20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	±1.0	μA
Output Leakage Current ($\overline{E}$ = V_{IH} or $\overline{G}$ = V_{IH} or $\overline{W}$ = V_{IL}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	±1.0	μA
AC Supply Current (I_{out} = 0 mA)	I_{CCA}	—	110	mA
TTL Standby Current ($\overline{E}$ = V_{IH}, No Restrictions on Other Inputs)	I_{SB1}	—	20	mA
CMOS Standby Current ($\overline{E}$ ≥ V_{CC} − 0.2 V, No Restrictions on Other Inputs)	I_{SB2}	—	15	mA
Output Low Voltage (I_{OL} = 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = −4.0 mA)	V_{OH}	2.4	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Typ	Max	Unit
Input Capacitance	All Inputs Except $\overline{E}$	C_{in}	4	6	pF
	$\overline{E}$		5	7	
I/O Capacitance	DQ	$C_{I/O}$	5	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . .0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns

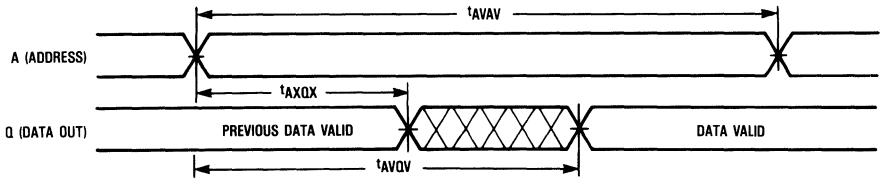
Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load . . . . . Figure 1A Unless Otherwise Noted

READ CYCLE (See Note 1)

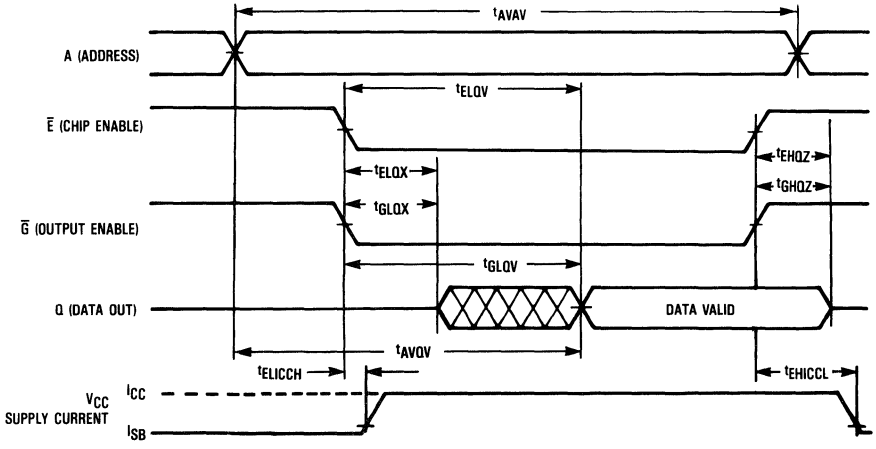
Parameter	Symbol		MCM6270-20		MCM6270-25		MCM6270-35		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	20	—	25	—	35	—	ns	2
Address Access Time	t_{AVQV}	t_{AA}	—	20	—	25	—	35	ns	
Chip Enable Access Time	t_{ELQV}	t_{ACS}	—	20	—	25	—	35	ns	
Output Enable Access Time	t_{GLQV}	t_{OE}	—	10	—	12	—	14	ns	
Output Hold from Address Change	t_{AXQX}	t_{OH}	5	—	5	—	5	—	ns	
Chip Enable Low to Output Active	t_{ELQX}	t_{LZ}	5	—	5	—	5	—	ns	3,4,5
Chip Enable High to Output High-Z	t_{EHQZ}	t_{HZ}	0	8	0	10	0	15	ns	3,4,5
Output Enable Low to Output Active	t_{GLQX}	t_{LZ}	0	—	0	—	0	—	ns	3,4,5
Output Enable High to Output High-Z	t_{GHQZ}	t_{HZ}	0	8	0	10	0	15	ns	3,4,5
Power Up Time	t_{ELICCH}	t_{PU}	0	—	0	—	0	—	ns	
Power Down Time	t_{EHICCL}	t_{PD}	—	20	—	20	—	30	ns	

NOTES: 1. $\overline{W}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transitioning address.
3. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} min, and t_{GHQZ} max is less than t_{GLQX} min, both for a given device and from device to device.
4. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B.
5. This parameter is sampled and not 100% tested.
6. Device is continuously selected ($\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}).
7. Addresses valid prior to or coincident with $\overline{E}$ going low.

READ CYCLE 1 (See Note 6 Above)



READ CYCLE 2 (See Note 7 Above)

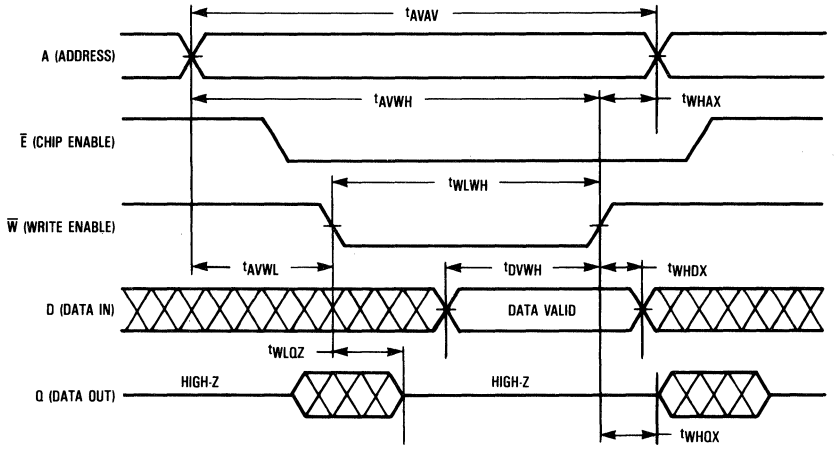


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol		MCM6270-20		MCM6270-25		MCM6270-35		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	20	–	25	–	35	–	ns	3
Address Setup Time	t_{AVWL}	t_{AS}	0	–	0	–	0	–	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	15	–	20	–	30	–	ns	
Write Pulse Width	t_{WLWH}	t_{WP}	15	–	20	–	25	–	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	10	–	10	–	15	–	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	–	0	–	0	–	ns	
Write Low to Output High-Z	t_{WLQZ}	t_{WZ}	0	8	0	10	0	15	ns	4,5,6
Write High to Output Active	t_{WHQX}	t_{OW}	5	–	5	–	5	–	ns	4,5,6
Write Recovery Time	t_{WHAX}	t_{WR}	0	–	0	–	0	–	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. Transition is measured ±500 mV from steady-state voltage with load in Figure 1B.
5. Parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max, is less than t_{WHQX} min, both for a given device and from device to device.

7



AC TEST LOADS

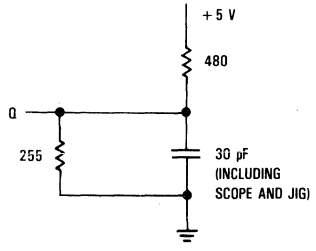


Figure 1A

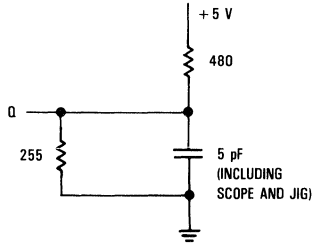
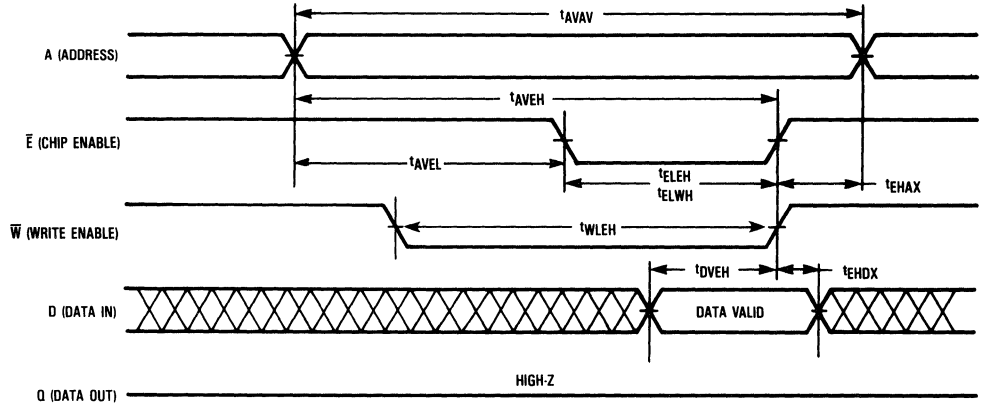


Figure 1B

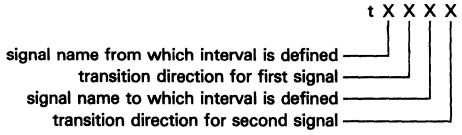
WRITE CYCLE 2 ($\overline{E}$ Controlled; See Notes 1 and 2)

Parameter	Symbol		MCM6270-20		MCM6270-25		MCM6270-35		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	20	–	25	–	35	–	ns	3
Address Setup Time	t_{AVEL}	t_{AS}	0	–	0	–	0	–	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	15	–	20	–	30	–	ns	
Chip Enable to End of Write	t_{ELEH}	t_{CW}	15	–	20	–	30	–	ns	4,5
Chip Enable to End of Write	t_{ELWH}	t_{CW}	15	–	20	–	30	–	ns	4,5
Write Pulse Width	t_{WLEH}	t_{WP}	15	–	20	–	25	–	ns	
Data Valid to End of Write	t_{DVEH}	t_{DW}	10	–	10	–	15	–	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	–	0	–	0	–	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	–	0	–	0	–	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.



TIMING PARAMETER ABBREVIATIONS

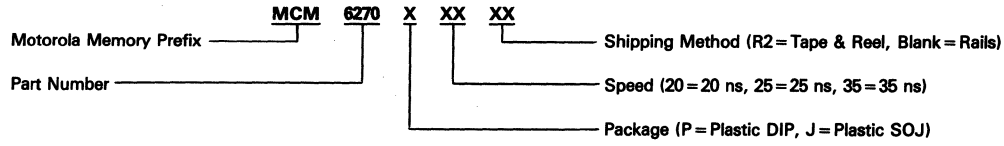


The transition definitions used in this data sheet are:
- H = transition to high
- L = transition to low
- V = transition to valid
- X = transition to invalid or don't care
- Z = transition to off (high impedance)

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

ORDERING INFORMATION
(Order by Full Part Number)

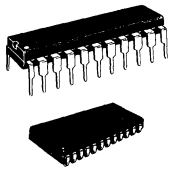


Full Part Numbers—MCM6270P20, MCM6270P25, MCM6270P35
MCM6270J20, MCM6270J25, MCM6270J35
MCM6270J20R2, MCM6270J25R2, MCM6270J35R2

7

MCM6287

64K x 1 Bit Static Random Access Memory



P PACKAGE
PLASTIC
CASE 736A

J PACKAGE
300 MIL SOJ
CASE 810A

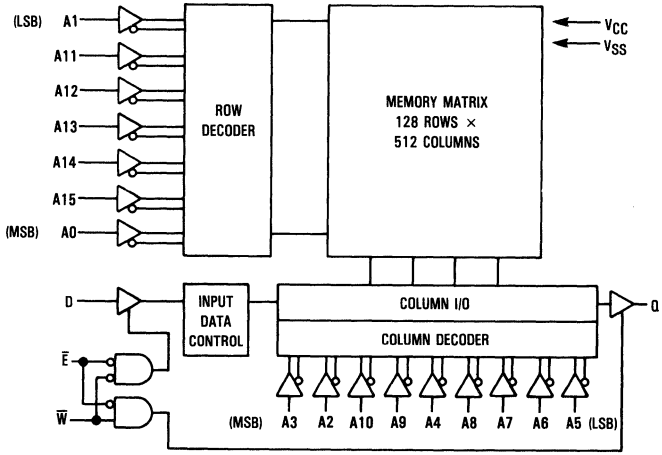
The MCM6287 is a 65,536 bit static random access memory organized as 65,536 words of 1 bit, fabricated using Motorola's high-performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption for greater reliability.

The chip enable ($\overline{E}$) pin is not a clock. In less than a cycle time after $\overline{E}$ goes high, the part enters a low-power standby mode, remaining in that state until $\overline{E}$ goes low again. This device also incorporates internal power down circuitry that will reduce active current for less than 100% duty cycle applications. These features provide reduced system power requirements without degrading access time performance.

The MCM6287 is available in a 300 mil, 22 lead plastic DIP and a 24 lead, 300 mil, surface-mount SOJ package. Both feature JEDEC standard pinout.

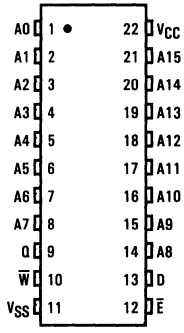
- Single 5 V ±10% Power Supply
- Fast Access Time: 25/35 ns
- Equal Address and Chip Enable Access Time
- Low Power Operation: 120/110 mA Maximum, Active AC
- High Board Density SOJ Available
- Three State Data Output
- Fully TTL Compatible

BLOCK DIAGRAM

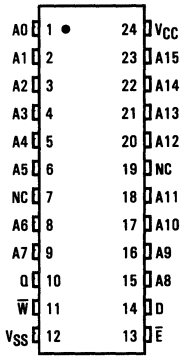


PIN ASSIGNMENT

DUAL-IN-LINE



SMALL OUTLINE



PIN NAMES	
A0-A15	Address Input
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
D	Data Input
Q	Data Output
V_{CC}	Power (+5 V)
V_{SS}	Ground
NC	No Connection

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TRUTH TABLE

$\overline{E}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	Not Selected	ISB1, ISB2	High-Z	–
L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	L	Write	I_{CCA}	High-Z	Write Cycle

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC}+0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation (T_A=25°C)	P_D	1.0	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature—Plastic Ceramic	T_{stg}	−55 to +125 −65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

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DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.0	–	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	−0.5*	–	0.8	V

*V_{IL} (min) = −0.5 V dc; V_{IL} (min) = −3.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter		Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in}=0 to V_{CC})		$I_{lkg(I)}$	–	±1.0	μA
Output Leakage Current ($\overline{E}$=V_{IH}, V_{out}=0 to V_{CC})		$I_{lkg(O)}$	–	±1.0	μA
AC Supply Current (I_{out}=0 mA)	MCM6287-25: t_{AVAV}=25 ns	I_{CCA}	–	120	mA
	MCM6287-35: t_{AVAV}=35 ns	I_{CCA}	–	110	
TTL Standby Current ($\overline{E}$=V_{IH}, No Restrictions on Other Inputs)		I_{SB1}	–	20	mA
CMOS Standby Current ($\overline{E}$≥V_{CC}−0.2 V, No Restrictions on Other Inputs)		I_{SB2}	–	15	mA
Output Low Voltage (I_{OL}=8.0 mA)		V_{OL}	–	0.4	V
Output High Voltage (I_{OH}=−4.0 mA)		V_{OH}	2.4	–	V

CAPACITANCE (f=1.0 MHz, dV=3.0 V, T_A=25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Typ	Max	Unit
Input Capacitance	All Inputs Except $\overline{E}$	C_{in}	4	6	pF
	$\overline{E}$		5	7	
Output Capacitance		C_{out}	5	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns

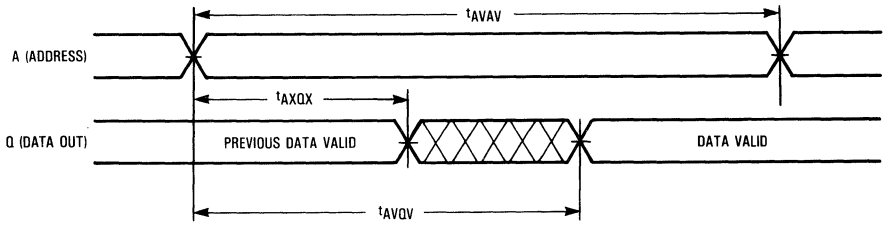
Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load . . . . . Figure 1A Unless Otherwise Noted

READ CYCLE (See Note 1)

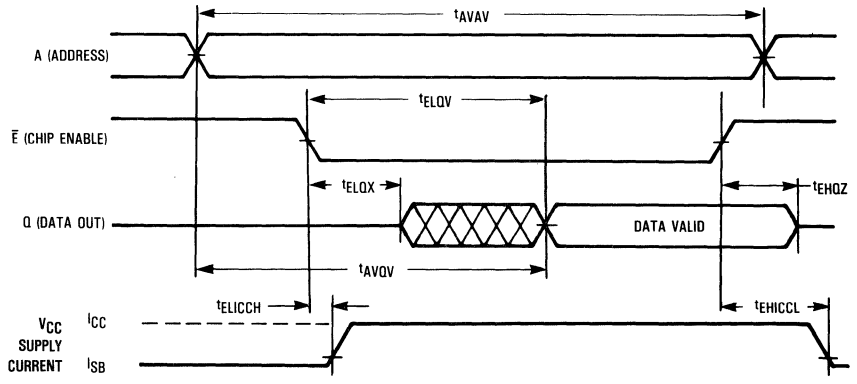
Parameter	Symbol		MCM6287-25		MCM6287-35		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	25	–	35	–	ns	2
Address Access Time	t_{AVQV}	t_{AA}	–	25	–	35	ns*	
Enable Access Time	t_{ELQV}	t_{ACS}	–	25	–	35	ns	3
Output Hold from Address Change	t_{AXQX}	t_{OH}	5	–	5	–	ns	
Enable Low to Output Active	t_{ELQX}	t_{LZ}	5	–	5	–	ns	4,5,6
Enable High to Output High-Z	t_{EHQZ}	t_{HZ}	0	15	0	15	ns	4,5,6
Power Up Time	t_{ELICCH}	t_{PU}	0	–	0	–	ns	
Power Down Time	t_{EHICCL}	t_{PD}	–	25	–	30	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transitioning address.
3. Addresses valid prior to or coincident with $\overline{E}$ going low.
4. At any given voltage and temperature, t_{EHQZ} max, is less than t_{ELQX} min, both for a given device and from device to device.
5. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E}$ = V_{IL}).

READ CYCLE 1 (See Note 7 Above)



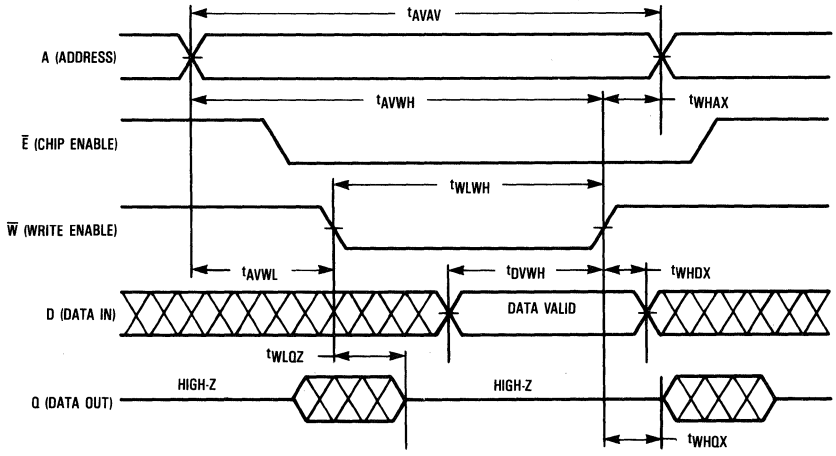
READ CYCLE 2 (See Note 3 Above)



WRITE CYCLE 1 ($\overline{W}$ Controlled, See Note 1)

Parameter	Symbol		MCM6287-25		MCM6287-35		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	25	–	35	–	ns	2
Address Setup Time	t_{AVWL}	t_{AS}	0	–	0	–	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	20	–	25	–	ns	
Write Pulse Width	t_{WLWH}	t_{WP}	20	–	20	–	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	15	–	15	–	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	–	0	–	ns	
Write Low to Output High-Z	t_{WLQZ}	t_{WZ}	0	15	0	15	ns	3,4
Write High to Output Active	t_{WHQX}	t_{OW}	5	–	5	–	ns	3,4
Write Recovery Time	t_{WHAX}	t_{WR}	0	–	0	–	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. All write cycle timing is referenced from the last valid address to the first transitioning address.
3. Transition is measured ±500 mV from steady-state voltage with load in Figure 1B.
4. Parameter is sampled and not 100% tested.



AC TEST LOADS

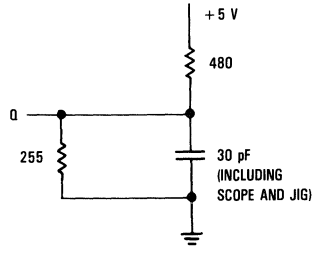


Figure 1A

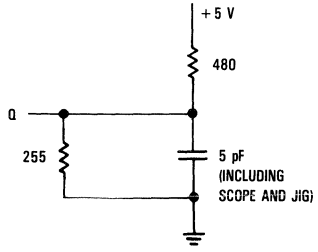


Figure 1B

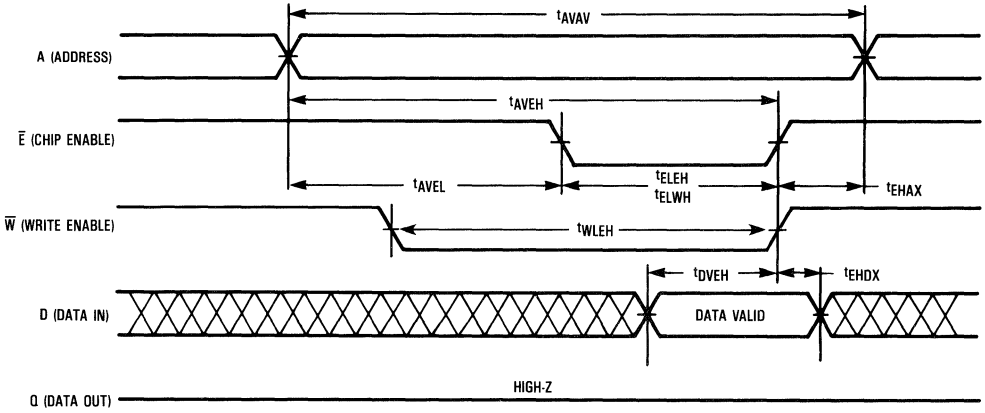
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

WRITE CYCLE 2 ($\overline{E}$ Controlled, See Note 1)

Parameter	Symbol		MCM6287-25		MCM6287-35		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	25	—	35	—	ns	2
Address Setup Time	t_{AVEL}	t_{AS}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	20	—	25	—	ns	
Enable to End of Write	t_{ELEH}	t_{CW}	20	—	25	—	ns	3,4
Enable to End of Write	t_{ELWH}	t_{CW}	20	—	25	—	ns	
Write Pulse Width	t_{WLEH}	t_{WP}	20	—	20	—	ns	
Data Valid to End of Write	t_{DVEH}	t_{DW}	15	—	15	—	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. All write cycle timing is referenced from the last valid address to the first transitioning address.
3. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
4. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.



7

TYPICAL CHARACTERISTICS

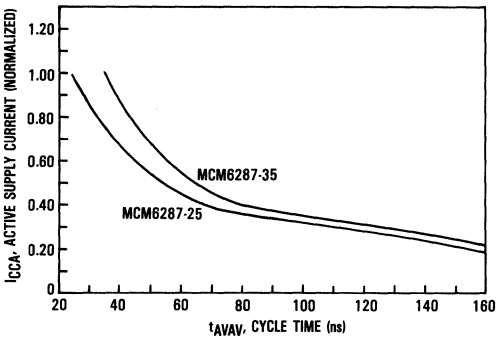


Figure 2. Relative Power versus Cycle Time

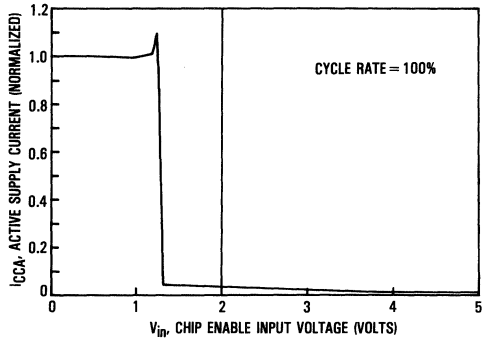


Figure 3. Active Supply Current versus Chip Enable Input Voltage

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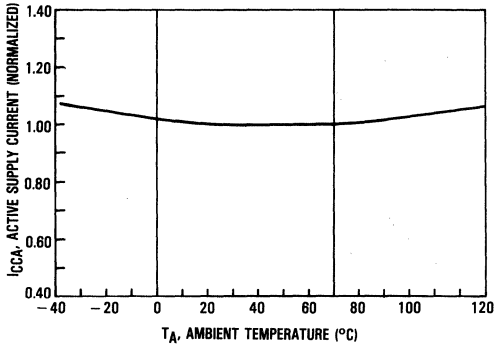


Figure 4. Active Supply Current versus Temperature

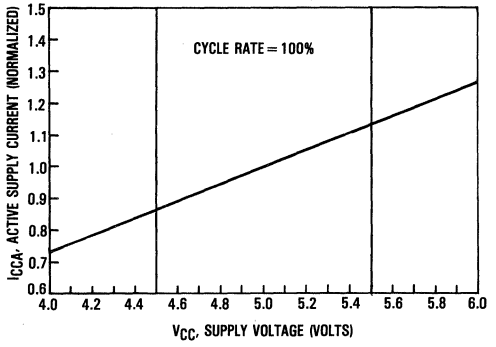


Figure 5. Active Supply Current versus Supply Voltage

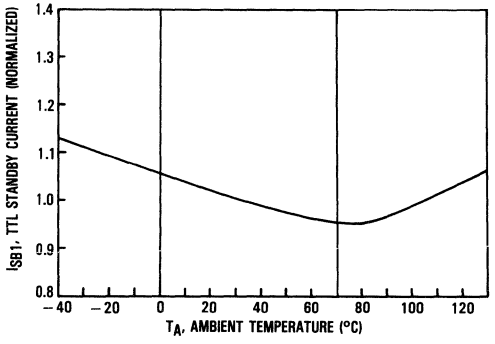


Figure 6. Standby Supply Current versus Temperature

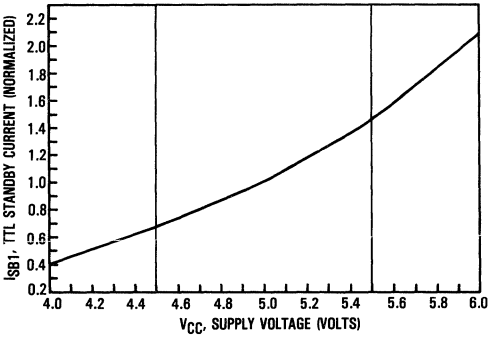


Figure 7. Standby Supply Current versus Supply Voltage

TYPICAL CHARACTERISTICS (Continued)

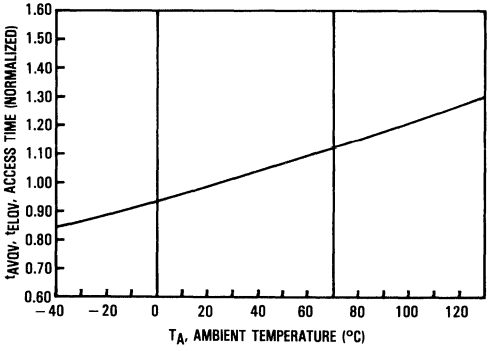


Figure 8. Address and Enable Access Times versus Temperature

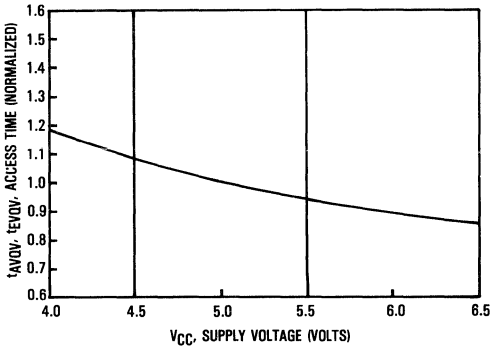


Figure 9. Address and Enable Access Times versus Supply Voltage

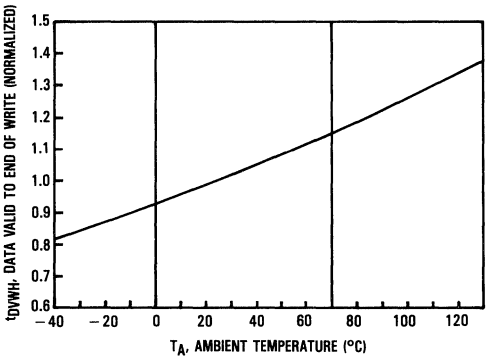


Figure 10. Data Setup Time versus Temperature

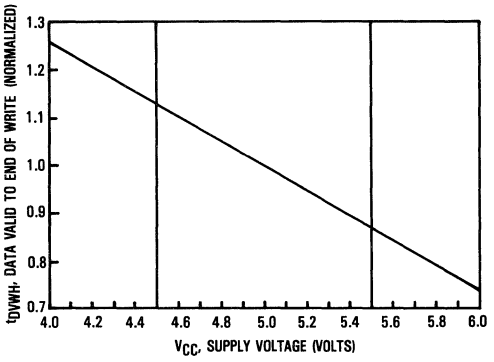


Figure 11. Data Setup Time versus Supply Voltage

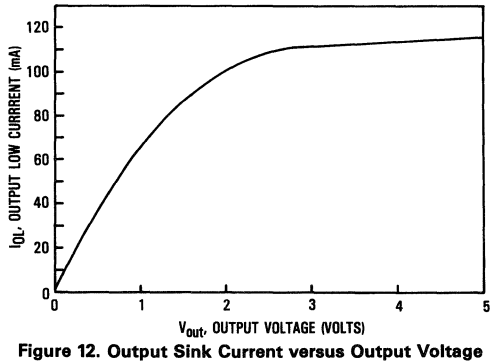


Figure 12. Output Sink Current versus Output Voltage

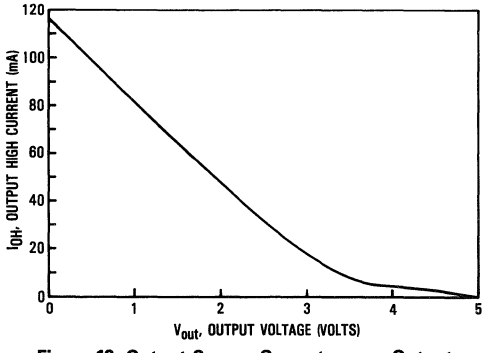
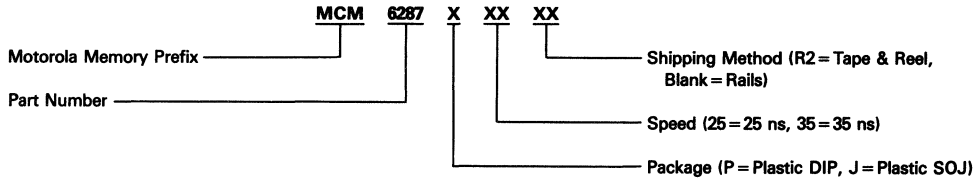


Figure 13. Output Source Current versus Output Voltage

ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers — MCM6287P25, MCM6287P35, MCM6287J25, MCM6287J35, MCM6287J25R2, MCM6287J35R2

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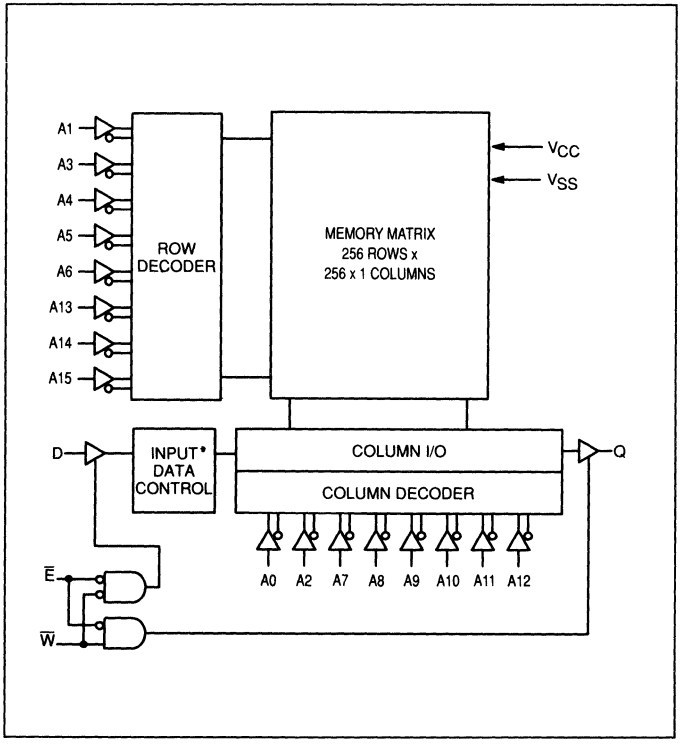
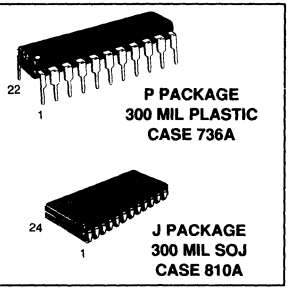
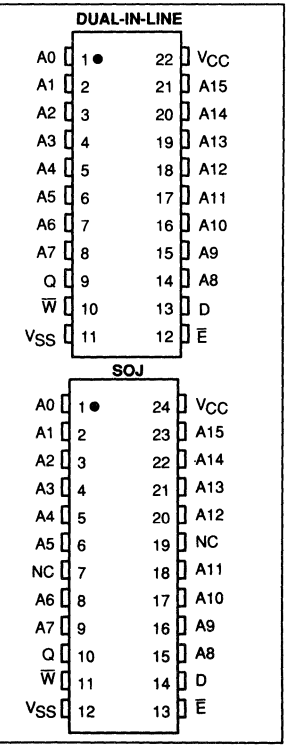
64K x 1 Bit Fast Static RAM

MCM6287-12, -15, -20
See QuickRAM, Page 7-122

MCM6287C-8, -10
See QuickRAM II, Page 7-142







PIN NAMES	
A0-A15 ..... Address Input	Q ..... Data Output
E ..... Chip Enable	VCC ..... +5 V Power Supply
W ..... Write Enable	VSS ..... Ground
D ..... Data Input	NC ..... No Connection

MCM6287 TRUTH TABLE (X = don't care)

E	W	Mode	VCC Current	Output	Cycle
H	X	Not Selected	I_{SB1}, I_{SB2}	High-Z	—
L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	L	Write	I_{CCA}	High-Z	Write Cycle

7

MCM6288
MCM6290

16K x 4 Bit Static RAMs

The MCM6288 and MCM6290 are 65,536 bit static random access memories organized as 16,384 words of 4 bits, fabricated using Motorola's high-performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption for greater reliability.

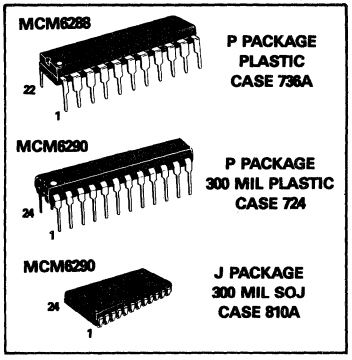
The chip enable ($\overline{E}$) pin is not a clock. In less than a cycle time after $\overline{E}$ goes high, the part enters a low-power standby mode, remaining in that state until $\overline{E}$ goes low again. These devices also incorporate internal power down circuitry that will reduce active current for less than 100% duty cycle applications. These features reduce system power requirements without degrading access time performance.

The MCM6290 has both chip enable ($\overline{E}$) and output enable ($\overline{G}$) inputs, allowing greater system flexibility. Either input, when high, will force the outputs to high impedance.

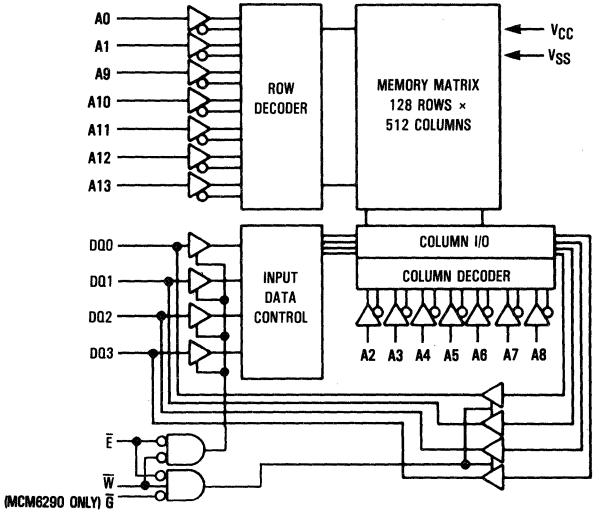
- Single 5 V ±10% Power Supply
- Fast Access Time (Maximum):

(xx = 88 or 90)	Address	Chip Enable	MCM6290 Output Enable
MCM62xx-20	20 ns	20 ns	10 ns
MCM62xx-25	25 ns	25 ns	12 ns
MCM62xx-30	30 ns	30 ns	15 ns
MCM62xx-35	35 ns	35 ns	15 ns

- Equal Address and Chip Enable Access Time
- Output Enable ($\overline{G}$) Feature for Increased System Flexibility and to Eliminate Bus Contention Problems (MCM6290)
- Low Power Operation: 120–110 mA Maximum, Active AC
- Fully TTL Compatible—Three-State Data Output



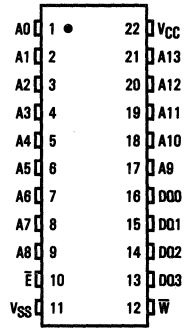
BLOCK DIAGRAM



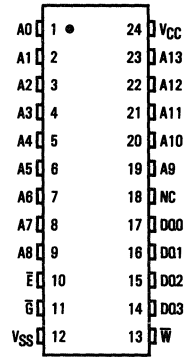
PIN NAMES	
A0-A13 . . . . . Address Input	$\overline{E}$ . . . . . Chip Enable
DQ0-DQ3. . Data Input/Output	NC . . . . . No Connection
$\overline{W}$ . . . . . Write Enable	V_{CC}. . . . +5 V Power Supply
$\overline{G}$ (MCM6290) . . Output Enable	V_{SS}. . . . . Ground

PIN ASSIGNMENT

MCM6288



MCM6290



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MCM6288 TRUTH TABLE

$\overline{E}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	Not Selected	ISB1, ISB2	High-Z	—
L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	L	Write	I_{CCA}	High-Z	Write Cycle

MCM6290 TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	I/O Pin	Cycle
H	X	X	Not Selected	I_{SB}	High-Z	—
L	H	H	Read	I_{CCA}	High-Z	—
L	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	X	L	Write	I_{CCA}	D_{in}	Write Cycle

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC}+0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation (T_A=25°C)	P_D	1.0	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

7

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.0	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

*V_{IL} (min) = −0.5 V dc; V_{IL} (min) = −3.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter		Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in}=0 to V_{CC})		$I_{lkg(I)}$	—	±1.0	μA
Output Leakage Current ($\overline{E}$=V_{IH}, V_{out}=0 to V_{CC})		$I_{lkg(O)}$	—	±1.0	μA
AC Supply Current (I_{out}=0 mA)	t_{AVAV}=20 ns	I_{CCA}	—	120	mA
	t_{AVAV}=25 ns		—	120	
	t_{AVAV}=30 ns		—	120	
	t_{AVAV}=35 ns		—	110	
TTL Standby Current ($\overline{E}$=V_{IH}, No Restrictions on Other Inputs)		I_{SB1}	—	20	mA
CMOS Standby Current ($\overline{E}$≥V_{CC}−0.2 V, No Restrictions on Other Inputs)		I_{SB2}	—	15	mA
Output Low Voltage (I_{OL}=8.0 mA)		V_{OL}	—	0.4	V
Output High Voltage (I_{OH}=−4.0 mA)		V_{OH}	2.4	—	V

CAPACITANCE (f=1.0 MHz, dV=3.0 V, T_A=25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Typ	Max	Unit
Input Capacitance	All Inputs Except $\overline{E}$	C_{in}	4	6	pF
	$\overline{E}$		5	7	
I/O Capacitance		$C_{I/O}$	5	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns

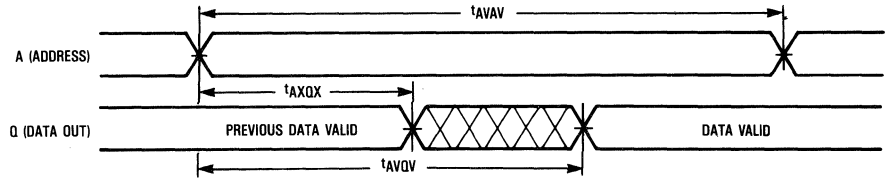
Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load . . . . . Figure 1A Unless Otherwise Noted

READ CYCLE (See Note 1)

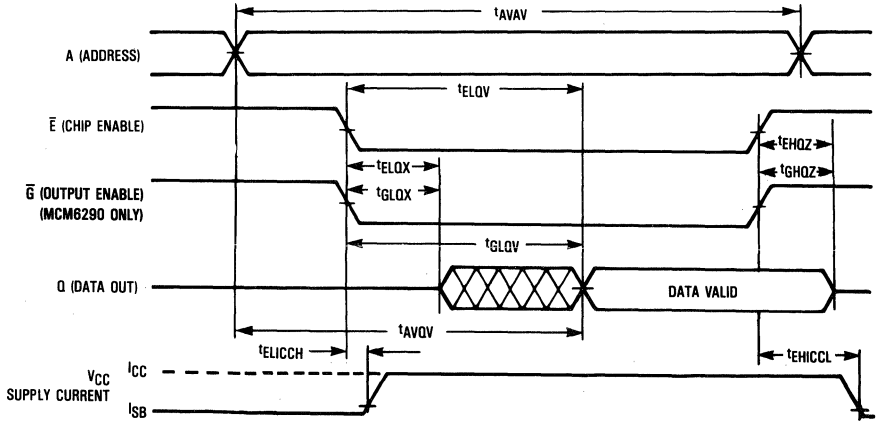
Parameter		Symbol		MCM6288-20 MCM6290-20		MCM6288-25 MCM6290-25		MCM6288-30 MCM6290-30		MCM6288-35 MCM6290-35		Unit	Notes
		Standard	Alternate	Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time		t_{AVAV}	t_{RC}	20	–	25	–	30	–	35	–	ns	2
Address Access Time		t_{AVQV}	t_{AA}	–	20	–	25	–	30	–	35	ns	
Enable Access Time		t_{ELQV}	t_{ACS}	–	20	–	25	–	30	–	35	ns	3
Output Hold from Address Change		t_{AXQX}	t_{OH}	5	–	5	–	5	–	5	–	ns	
Output Enable Access Time	MCM6290	t_{GLQV}	t_{OE}	–	10	–	12	–	15	–	15	ns	
Output Enable Low to Output Active	MCM6290	t_{GLQX}	t_{LZ}	0	–	0	–	0	–	0	–	ns	4,5,6
Output Enable High to Output High-Z	MCM6290	t_{GHQZ}	t_{HZ}	0	8	0	10	0	12	0	15	ns	4,5,6
Enable Low to Output Active		t_{ELQX}	t_{LZ}	5	–	5	–	5	–	5	–	ns	4,5,6
Enable High to Output High-Z		t_{EHQZ}	t_{HZ}	0	8	0	10	0	12	0	15	ns	4,5,6
Power Up Time		t_{ELICCH}	t_{PU}	0	–	0	–	0	–	0	–	ns	
Power Down Time		t_{EHICCL}	t_{PD}	–	20	–	25	–	30	–	30	ns	

NOTES: 1. $\overline{W}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transitioning address.
3. Addresses valid prior to or coincident with $\overline{E}$ going low.
4. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} min, and t_{GHQZ} max is less than t_{GLQX} min, both for a given device and from device to device.
5. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E}$ = V_{IL}) and $\overline{G}$ = V_{IL} (MCM6290 only).

READ CYCLE 1 (See Note 7 Above)



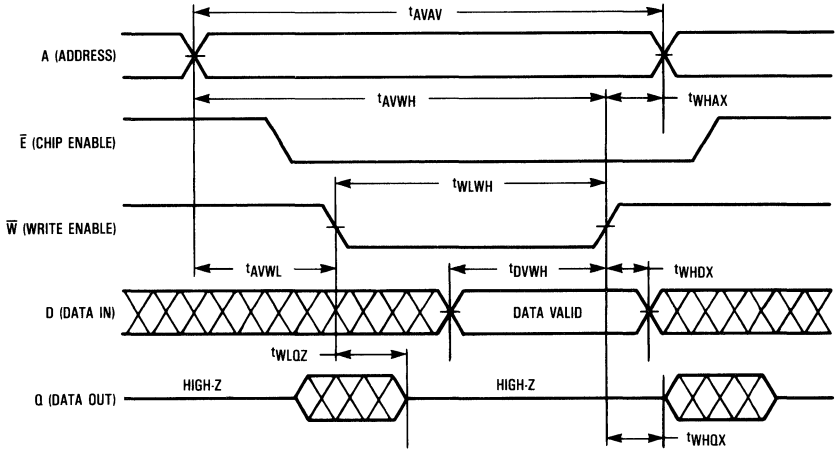
READ CYCLE 2 (See Note 3 Above)



WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 6)

Parameter	Symbol		MCM6288-20 MCM6290-20		MCM6288-25 MCM6290-25		MCM6288-30 MCM6290-30		MCM6288-35 MCM6290-35		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	20	–	25	–	30	–	35	–	ns	2
Address Setup Time	t_{AVWL}	t_{AS}	0	–	0	–	0	–	0	–	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	15	–	20	–	25	–	30	–	ns	
Write Pulse Width	t_{WLWH}	t_{WP}	15	–	20	–	25	–	30	–	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	10	–	10	–	12	–	15	–	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	–	0	–	0	–	0	–	ns	
Write Low to Output High-Z	t_{WLQZ}	t_{WZ}	0	8	0	10	0	12	0	15	ns	3,4,5,6
Write High to Output Active	t_{WHQX}	t_{OW}	5	–	5	–	5	–	5	–	ns	3,4,5
Write Recovery Time	t_{WHAX}	t_{WR}	0	–	0	–	0	–	0	–	ns	

NOTES: 1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. All write cycle timing is referenced from the last valid address to the first transitioning address.
3. Transition is measured ±500 mV from steady-state voltage with load in Figure 1B.
4. Parameter is sampled and not 100% tested.
5. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min both for a given device and from device to device.
6. MCM6290, if $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.



AC TEST LOADS

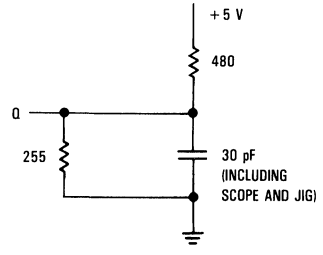


Figure 1A

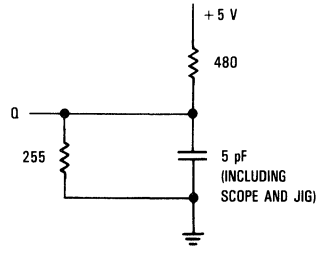
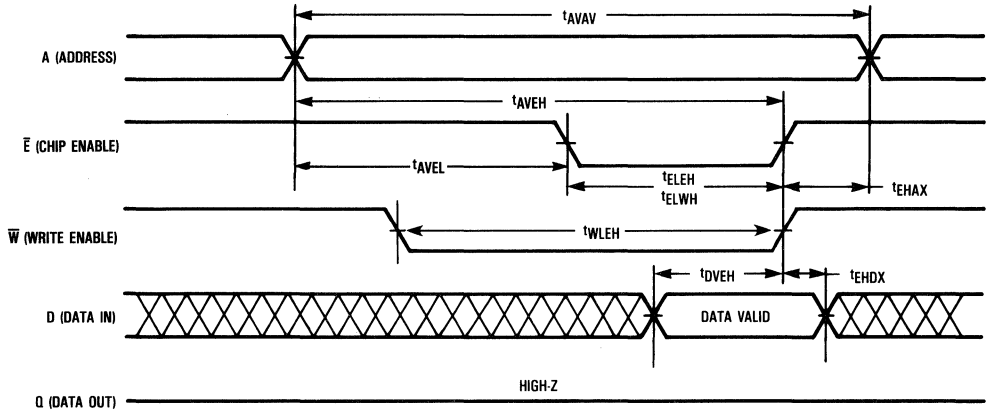


Figure 1B

WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 5)

Parameter	Symbol		MCM6288-20 MCM6290-20		MCM6288-25 MCM6290-25		MCM6288-30 MCM6290-30		MCM6288-35 MCM6290-35		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	20	–	25	–	30	–	35	–	ns	2
Address Setup Time	t_{AVEL}	t_{AS}	0	–	0	–	0	–	0	–	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	15	–	20	–	25	–	30	–	ns	
Enable to End of Write	t_{ELEH}	t_{CW}	15	–	20	–	25	–	30	–	ns	3,4
Enable to End of Write	t_{ELWH}	t_{CW}	15	–	20	–	25	–	30	–	ns	3,4
Write Pulse Width	t_{WLEH}	t_{WP}	15	–	20	–	25	–	30	–	ns	
Data Valid to End of Write	t_{DVEH}	t_{DW}	10	–	10	–	12	–	15	–	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	–	0	–	0	–	0	–	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	–	0	–	0	–	0	–	ns	

NOTES: 1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. All write cycle timing is referenced from the last valid address to the first transitioning address.
3. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
4. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.
5. MCM6290, if $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.



TIMING PARAMETER ABBREVIATIONS

t X X X X

signal name from which interval is defined
transition direction for first signal
signal name to which interval is defined
transition direction for second signal

The transition definitions used in this data sheet are:
H = transition to high
L = transition to low
V = transition to valid
X = transition to invalid or don't care
Z = transition to off (high impedance)

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

ORDERING INFORMATION
(Order by Full Part Number)

MCM	62XX	X	XX	XX
Motorola Memory Prefix	Part Number	Package (P = Plastic DIP, J = Plastic SOJ)	Speed (25 = 25 ns, 30 = 30 ns, 35 = 35 ns, 45 = 45 ns)	Shipping Method (R2 = Tape and Reel, Blank = Rails)

Full Part Numbers —				
	MCM6288P20	MCM6290P20	MCM6290J20	MCM6290J20R2
	MCM6288P25	MCM6290P25	MCM6290J25	MCM6290J25R2
	MCM6288P30	MCM6290P30	MCM6290J30	MCM6290J30R2
	MCM6288P35	MCM6290P35	MCM6290J35	MCM6290J35R2

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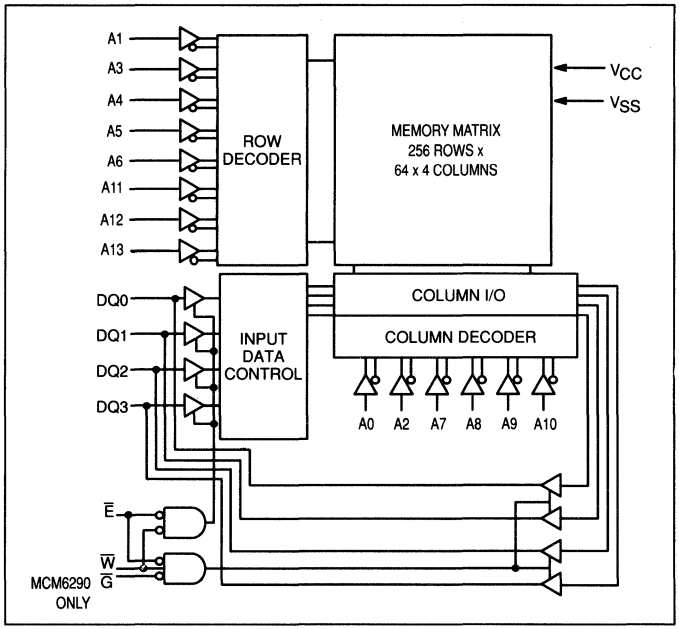
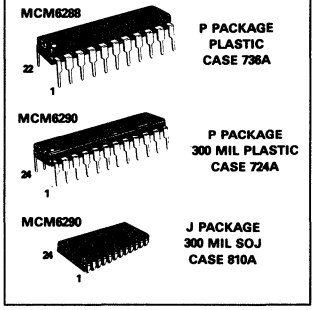
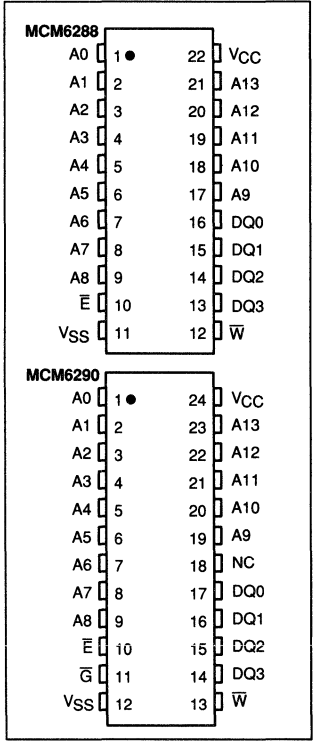
16K x 4 Bit Fast Static RAMs

MCM6288-12, -15
MCM6290-12, -15
See QuickRAM, Page 7-122

MCM6288C-8, -10
MCM6290C-8, -10
See QuickRAM II, Page 7-142







PIN NAMES	
A0-A13 ..... Address Input	E ..... Chip Enable
DQ0–DQ3 ..... Data Input/Output	NC ..... No Connection
W ..... Write Enable	V_{CC} ..... +5 V Power Supply
G (MCM6290) ..... Output Enable	V_{SS} ..... Ground

MCM6288 TRUTH TABLE (X = don't care)

E	W	Mode	V_{CC} Current	Output	Cycle
H	X	Not Selected	I_{SB1}, I_{SB2}	High-Z	—
L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	L	Write	I_{CCA}	High-Z	Write Cycle

MCM6290 TRUTH TABLE (X = don't care)

E	G	W	Mode	V_{CC} Current	Output	Cycle
H	X	X	Not Selected	I_{SB1}, I_{SB2}	High-Z	—
L	H	H	Output Disabled	I_{CCA}	High-Z	—
L	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	X	L	Write	I_{CCA}	High-Z	Write Cycle

MCM6706

Product Preview

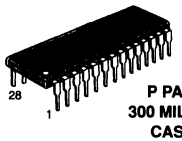
32K x 8 Bit Static Random Access Memory

The MCM6706 is a 262,144 bit static random access memory organized as 32,768 words of 8 bits, fabricated using high performance silicon-gate BiCMOS technology. Static design eliminates the need for external clocks or timing strobes.

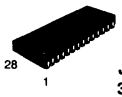
Output enable ($\overline{G}$) is a special control feature that provides increased system flexibility and eliminates bus contention problems.

The MCM6706 is available in a 300 mil, 28 lead surface-mount SOJ package and a 300 mil, 28 pin plastic dual-in-line package.

- Single 5.0 V ±10% Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- All Inputs and Outputs are TTL Compatible
- Three State Outputs
- Fast Access Times: MCM6706 — 10 ns
  MCM6706 — 12 ns
  MCM6706 — 15 ns

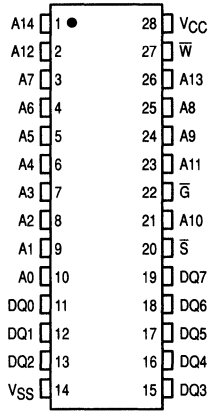


P PACKAGE
300 MIL PLASTIC
CASE 710B

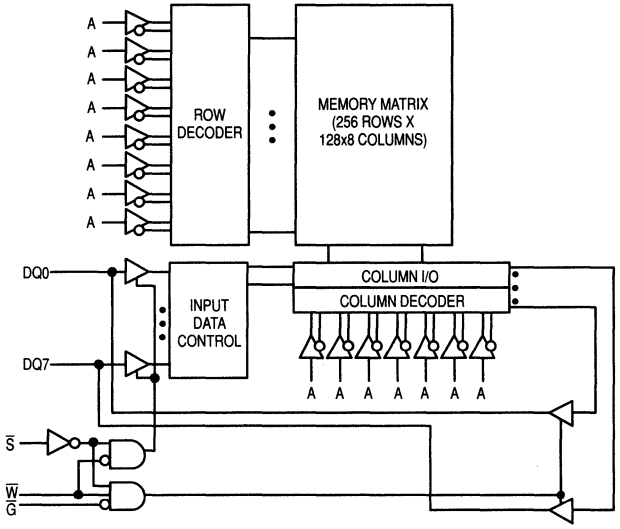


J PACKAGE
300 MIL SOJ
CASE 810B

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A0–A14	Address Inputs
$\overline{W}$	Write Enable
$\overline{S}$	Chip Select
$\overline{G}$	Output Enable
DQ0–DQ7	Data Input/Output
V_{CC}	+5.0 V Power Supply
V_{SS}	Ground

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This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

TRUTH TABLE

$\overline{S}$	$\overline{G}$	$\overline{W}$	Mode	I/O Pin	Cycle
H	X	X	Not Selected	High-Z	—
L	H	H	Read	High-Z	—
L	L	H	Read	D_{out}	Read Cycle
L	X	L	Write	D_{in}	Write Cycle

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	–0.5 to +7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	–0.5 to V_{CC}+0.5	V
Output Current	I_{out}	±30	mA
Power Dissipation	P_D	2.0	W
Temperature Under Bias	T_{bias}	–10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature — Plastic	T_{stg}	–55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

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DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.3*	V
Input Low Voltage	V_{IL}	–0.5**	—	0.8	V

*V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 2.0 ns) for I ≤ 20 mA.

**V_{IL} (min) = –0.5 V dc; V_{IL} (min) = –2.0 V ac (pulse width ≤ 2.0 ns) for I ≤ 20 mA.

DC CHARACTERISTICS

Parameter		Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})		$I_{lkg(I)}$	—	—	±1.0	µA
Output Leakage Current ($\overline{S}$ = V_{IH}, V_{out} = 0 to V_{CC})		$I_{lkg(O)}$	—	—	±1.0	µA
AC Supply Current (I_{out} = 0 mA)	MCM6706 –10: t_{AVAV} = 10 ns	I_{CCA}	—	150	200	mA
	MCM6706 –12: t_{AVAV} = 12 ns		—	140	195	
	MCM6706 –15: t_{AVAV} = 15 ns		—	130	190	
Output Low Voltage (I_{OL} = 8.0 mA)		V_{OL}	—	—	0.4	V
Output High Voltage (I_{OH} = –4.0 mA)		V_{OH}	2.4	—	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	4.0	6.0	pF
I/O Capacitance	$C_{I/O}$	5.0	7.0	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 2.0 ns

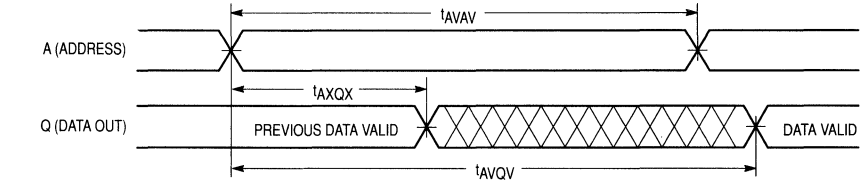
Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load . . . . . See Figure 1

READ CYCLE (See Notes 1 and 2)

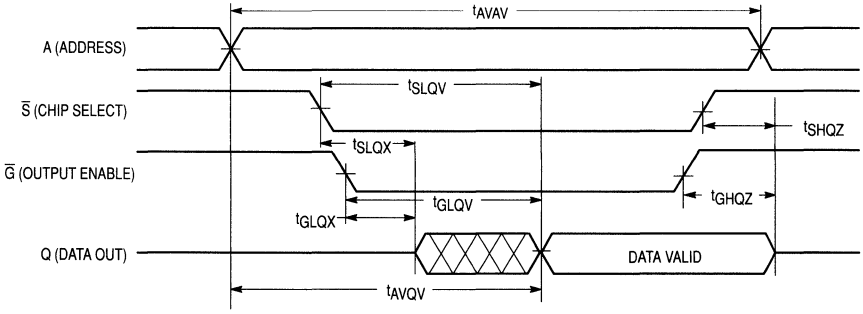
Parameter	Symbol		MCM6706-10		MCM6706-12		MCM6706-15		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	10	—	12	—	15	—	ns	3
Address Access Time	t_{AVQV}	t_{AA}	—	10	—	12	—	15	ns	
Chip Select Access Time	t_{SLQV}	t_{ACS}	—	5	—	6	—	8	ns	
Output Enable Access time	t_{GLQV}	t_{OE}	—	5	—	6	—	8	ns	
Output Hold from Address Change	t_{AXQX}	t_{OH}	4	—	4	—	4	—	ns	
Chip Select Low to Output Active	t_{SLQX}	t_{LZ}	1	—	1	—	1	—	ns	4,5,6
Chip Select High to Output High-Z	t_{SHQZ}	t_{HZ}	0	5	0	6	0	6	ns	4,5,6
Output Enable Low to Output Active	t_{GLQX}	t_{LZ}	1	—	1	—	1	—	ns	4,5,6
Output Enable High to Output High-Z	t_{GHQZ}	t_{HZ}	0	5	0	6	0	6	ns	4,5,6

NOTES:
1. $\overline{W}$ is high for read cycle.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All read cycle timing is referenced from the last valid address to the first transitioning address.
4. At any given voltage and temperature, t_{SHQZ} max < t_{SLQX} min, and t_{GHQZ} max < t_{GHQX} min, both for a given device and from device to device.
5. Transition is measured 100 mV from steady-state voltage with load of Figure 1.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{S}$ = V_{IL}, $\overline{G}$ = V_{IL}).
8. Addresses valid prior to or coincident with $\overline{S}$ going low.

READ CYCLE 1 (See Note 7 Above)



READ CYCLE 2 (See Note 8 Above)



WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol		MCM6706-10		MCM6706-12		MCM6706-15		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	10	—	12	—	15	—	ns	3
Address Setup Time	t_{AVWL}	t_{AS}	2	—	2	—	2	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	9	—	10	—	12	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLSH}	t_{WP}	6	—	7	—	8	—	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	5	—	6	—	7	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	—	0	—	0	—	ns	
Write Low to Data High-Z	t_{WLQZ}	t_{WZ}	0	5	0	6	0	6	ns	4,5,6
Write High to Output Active	t_{WHQX}	t_{OW}	2	—	2	—	2	—	ns	4,5,6
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{S}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured 100 mV from steady-state voltage with load of Figure 1.
5. Parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max is < t_{WHQX} min both for a given device and from device to device.

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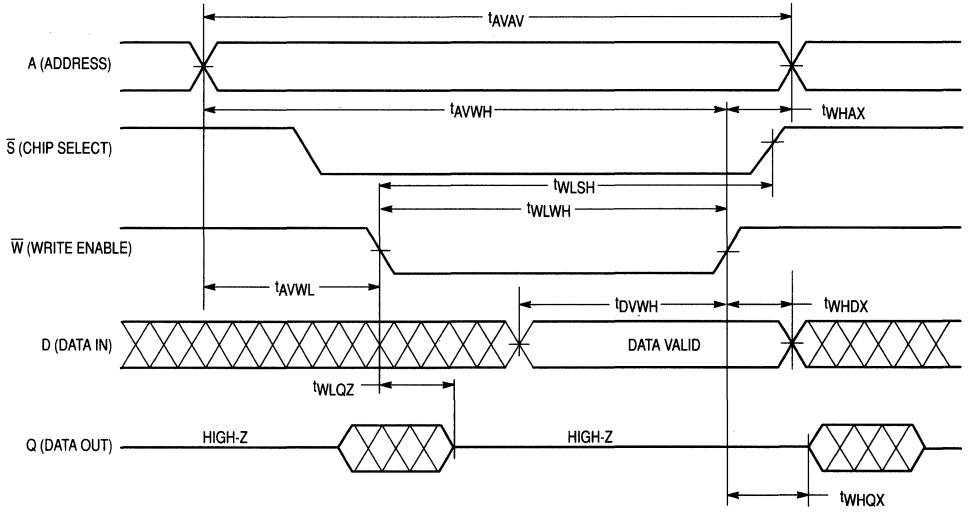


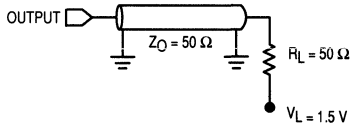


Figure 1. AC Test Load

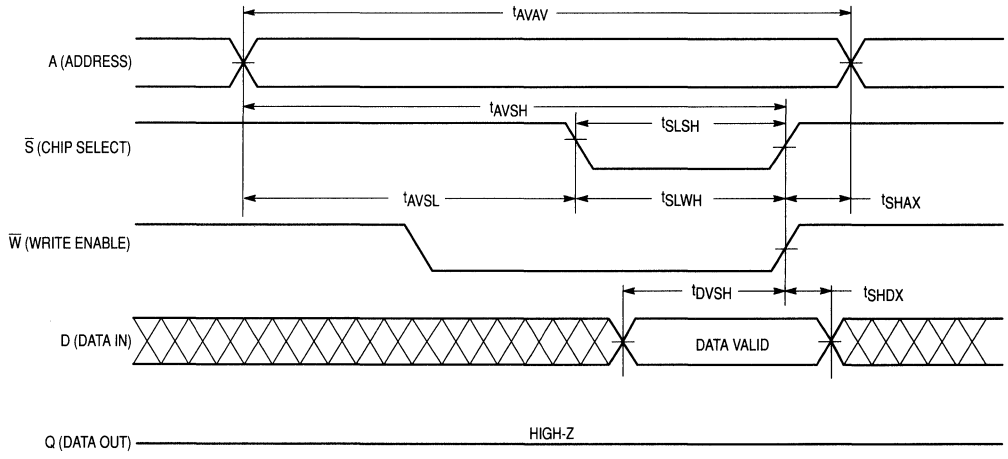
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

WRITE CYCLE 2 ($\overline{S}$ Controlled, See Notes 1 and 2)

Parameter	Symbol		MCM6706-10		MCM6706-12		MCM6706-15		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	10	—	12	—	15	—	ns	3
Address Setup Time	t_{AVSL}	t_{AS}	2	—	2	—	2	—	ns	
Address Valid to End of Write	t_{AVSH}	t_{AW}	9	—	10	—	12	—	ns	
Chip Select to End of Write	t_{SLWH}, t_{SLSH}	t_{CW}	6	—	7	—	8	—	ns	4,5
Data Valid to End of Write	t_{DVSH}	t_{DW}	5	—	6	—	7	—	ns	
Data Hold Time	t_{SHDX}	t_{DH}	0	—	0	—	0	—	ns	
Write Recovery Time	t_{SHAX}	t_{WR}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{S}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. If $\overline{S}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
5. If $\overline{S}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6706 X XX XX

- MCM — Motorola Memory Prefix
- 6706 — Part Number
- X — Package (P = 300 mil Plastic DIP, J = 300 mil SOJ)
- XX — Speed (10 = 10 ns, 12 = 12 ns, 15 = 15 ns)
- XX — Shipping Method (R2 = Tape & Reel, Blank = Rails)

Full Part Number —			
	MCM6706P10	MCM6706J10	MCM6706J10R2
	MCM6706P12	MCM6706J12	MCM6706J12R2
	MCM6706P15	MCM6706J15	MCM6706J15R2

MCM6708
MCM6709

Product Preview

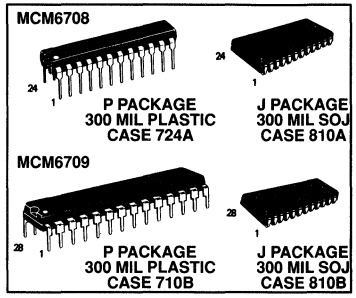
64K × 4 Bit Static RAM

The MCM6708 and the MCM6709 are 262,144 bit static random access memories organized as 65,536 words of 4 bits, fabricated using high-performance silicon-gate BICMOS technology. Static design eliminates the need for external clocks or timing strobes.

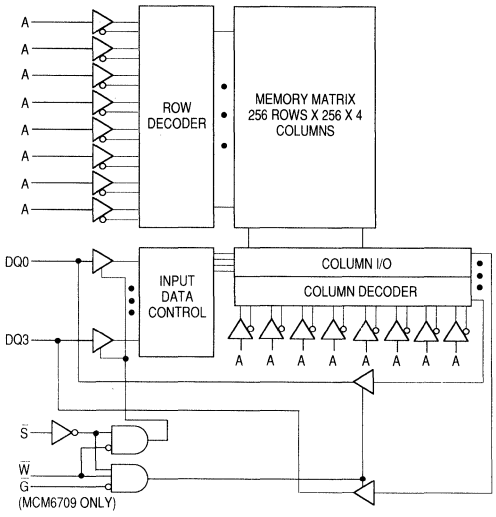
Output enable, ($\overline{G}$), a special control feature of the MCM6709, provides increased system flexibility and eliminates bus contention problems.

The MCM6708 is available in a 300 mil, 24 lead plastic surface-mount SOJ package and a 300 mil, 24 lead PDIP. The MCM6709 is available in a 300 mil, 28 lead plastic surface-mount SOJ package and a 300 mil, 28 lead PDIP.

- Single 5 V ± 10% Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- All Inputs and Outputs are TTL Compatible
- Three State Outputs
- Fast Access Times:
  MCM6708 — 10 ns MCM6709 — 10 ns
  MCM6708 — 12 ns MCM6709 — 12 ns



BLOCK DIAGRAM



PIN ASSIGNMENT

MCM6708

A0	1	24	V_{CC}
A1	2	23	A15
A2	3	22	A14
A3	4	21	A13
A4	5	20	A12
A5	6	19	A11
A6	7	18	A10
A7	8	17	DQ0
A8	9	16	DQ1
A9	10	15	DQ2
$\overline{S}$	11	14	DQ3
V_{SS}	12	13	$\overline{W}$

MCM6709

NC	1	28	V_{CC}
A0	2	27	A15
A1	3	26	A14
A2	4	25	A13
A3	5	24	A12
A4	6	23	A11
A5	7	22	A10
A6	8	21	NC
A7	9	20	NC
A8	10	19	DQ0
A9	11	18	DQ1
$\overline{S}$	12	17	DQ2
$\overline{G}$	13	16	DQ3
V_{SS}	14	15	$\overline{W}$

PIN NAMES

A0–A15	Address Inputs	$\overline{W}$	Write Enable
$\overline{G}$	Output Enable	$\overline{S}$	Chip Select
DQ0-DQ3	Data Input/Output	V_{CC}	+5 V Power Supply
V_{SS}	Ground	NC	No Connect

All power supply and ground pins must be connected for proper operation of the device.

TRUTH TABLE

$\overline{S}$	$\overline{G}$	$\overline{W}$	Mode	I/O Pin	Cycle
H	X	X	Not Selected	High-Z	—
L	H	H	Read	High-Z	—
L	L	H	Read	D_{out}	Read Cycle
L	X	L	Write	D_{in}	Read Cycle

X = Don't Care

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to 7.0	V
Voltage Relative to V_{SS} (For Any Pin Except V_{CC})	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 30	mA
Power Dissipation	P_D	2.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedence circuit.

This BICMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

7

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3*	V
Input Low Voltage	V_{IL}	– 0.5**	—	0.8	V

*V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 2 ns) for I ≤ 20 mA.
**V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2 V ac (pulse width ≤ 2 ns) for I ≤ 20 mA.

DC CHARACTERISTICS

Parameter		Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})		$I_{lkg(I)}$	—	—	± 1	µA
Output Leakage Current ($\overline{S}$ = V_{IH}, V_{out} = 0 to V_{CC})		$I_{lkg(O)}$	—	—	± 1	µA
AC Supply Current (I_{out} = 0 mA)	MCM6708-10/MCM609-10: t_{AVAV} = 10 ns	I_{CC}	—	150	200	mA
	MCM6708-12/MCM609-12: t_{AVAV} = 12 ns		—	140	195	
Output Low Voltage (I_{OL} = + 8.0 mA)		V_{OL}	—	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)		V_{OH}	2.4	—	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance (All Inputs Except DQ)	C_{in}	4	6	pF
Input/Output Capacitance	$C_{I/O}$	5	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns

Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1

READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol		MCM6708-10 MCM6709-10		MCM6708-12 MCM6709-12		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	10	—	12	—	ns	3
Address Access Time	t_{AVQV}	t_{AA}	—	10	—	12	ns	
Select Access Time	t_{SLQV}	t_{ACS}	—	5	—	6	ns	
Output Enable Access Time	t_{GLQV}	t_{OE}	—	5	—	6	ns	
Output Hold from Address Change	t_{AXQX}	t_{OH}	4	—	4	—	ns	
Select Low to Output Active	t_{SLQX}	t_{LZ}	1	—	1	—	ns	4, 5, 6
Output Enable Low to Output Active	t_{GLQX}	t_{LZ}	1	—	1	—	ns	4, 5, 6
Select High to Output High-Z	t_{SHQZ}	t_{HZ}	0	5	0	6	ns	4, 5, 6
Output Enable High to Output High-Z	t_{GHQZ}	t_{HZ}	0	5	0	6	ns	4, 5, 6

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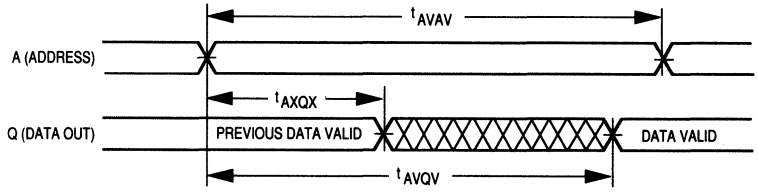
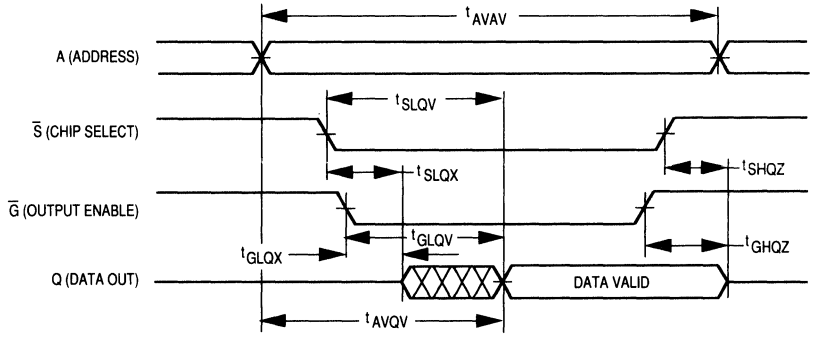
NOTES:
1. $\overline{W}$ is high for read cycle.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All read cycle timings are referenced from the last valid address to the first transitioning address.
4. At any given voltage and temperature, t_{SHQZ} max is less than t_{SLQX} min, and t_{GHQZ} max is less than t_{GHQX} min, both for a given device and from device to device.
5. Transition is measured 100 mV from steady-state voltage with load of Figure 1.
6. This parameter is sampled and not 100% tested.

READ CYCLE 1 (See Note)



NOTE: Device is continuously selected ($\overline{S}$ = V_{IL}, $\overline{G}$ = V_{IL}).

READ CYCLE 2 (See Note)



NOTE: Addresses valid prior to or coincident with $\overline{S}$ going low.

AC TEST LOADS

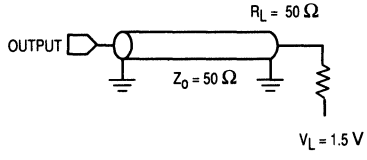


Figure 1

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the module point of view. Thus, the access time is shown as a maximum since the module never provides data later than that time.

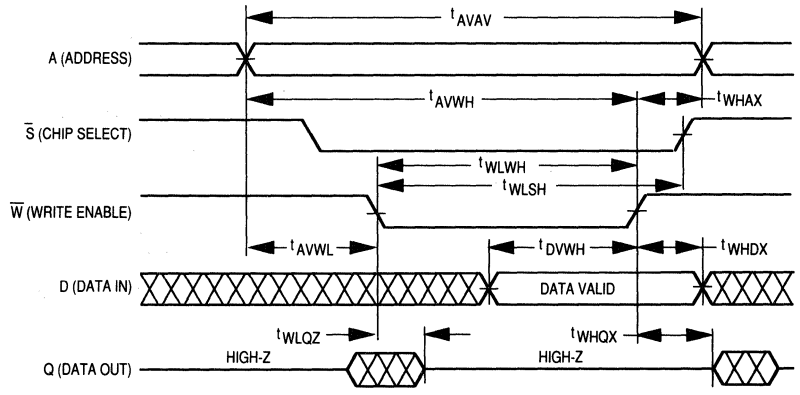
WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol		MCM6708-10 MCM6709-10		MCM6708-12 MCM6709-12		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	10	—	12	—	ns	3
Address Setup Time	t_{AVWL}	t_{AS}	2	—	2	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	9	—	10	—	ns	
Write Pulse Width	t_{WLWH} t_{WLSH}	t_{WP}	6	—	7	—	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	5	—	6	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	—	0	—	ns	
Write Low to Data High-Z	t_{WLQZ}	t_{WZ}	0	5	0	6	ns	4, 5, 6
Write High to Output Active	t_{WHQX}	t_{OW}	2	—	2	—	ns	4, 5, 6
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{S}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. Transition is measured 100 mV from steady-state voltage with load of Figure 1.
5. This parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min both for a given device and from device to device.

7

WRITE CYCLE 1

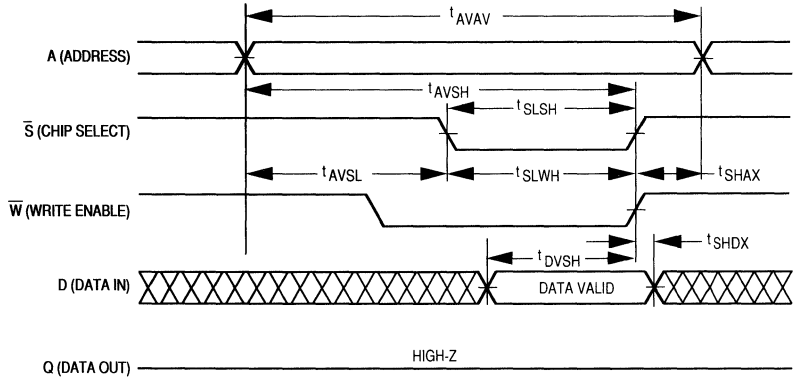


WRITE CYCLE 2 ($\overline{S}$ Controlled, See Notes 1 and 2)

Parameter	Symbol		MCM6708-10 MCM6709-10		MCM6708-12 MCM6709-12		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	10	—	12	—	ns	3
Address Setup Time	t_{AVSL}	t_{AS}	2	—	2	—	ns	
Address Valid to End of Write	t_{AVSH}	t_{AW}	9	—	10	—	ns	
Select to End of Write	t_{SLSH} t_{SLWH}	t_{CW}	6	—	7	—	ns	4,5
Data Valid to End of Write	t_{DVSH}	t_{DW}	5	—	6	—	ns	
Data Hold Time	t_{SHDX}	t_{DH}	0	—	0	—	ns	
Write Recovery Time	t_{SHAX}	t_{WR}	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{S}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. If $\overline{S}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
5. If $\overline{S}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2



ORDERING INFORMATION
(Order by Full Part Number)

MCM	6708 6709	x	xx	xx
Motorola Memory Prefix				
	Part Number			
		Package (NP = Plastic DIP, NJ = Plastic SOJ)		
			Speed (10 = 10 ns, 12 = 12 ns)	
				Shipping Method (R2 = Tape & Reel, Blank = Rails)

Full Part Numbers – MCM6708P10 MCM6708J10 MCM6708J10R2
MCM6708P12 MCM6708J12 MCM6708J12R2
MCM6709P10 MCM6709J10 MCM6709J10R2
MCM6709P12 MCM6709J12 MCM6709J12R2

MCM67081
MCM67082

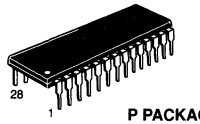
Product Preview

64K × 4 Bit Static RAM
with Separate Input/Output

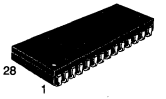
The MCM67081 and the MCM67082 are 262,144 bit static random-access memories organized as 65,536 words of 4 bits, fabricated using high-performance silicon-gate BICMOS technology. Static design eliminates the need for external clocks or timing strobes, while BICMOS circuitry reduces power consumption and provides for greater reliability.

Both the MCM67081 and MCM67082 are available in 300 mil, 28 lead surface-mount SOJ packages and 300 mil, 28 lead plastic DIP.

- Single 5 V ± 10% Power Supply
- Fully Static – No Clock or Timing Strobes Necessary
- All Inputs and Outputs are TTL Compatible
- Separate Data Inputs and Three-State Outputs
- Fast Access Times:
  MCM67081 – 10, 12, 15 ns
  MCM67082 – 10, 12, 15 ns

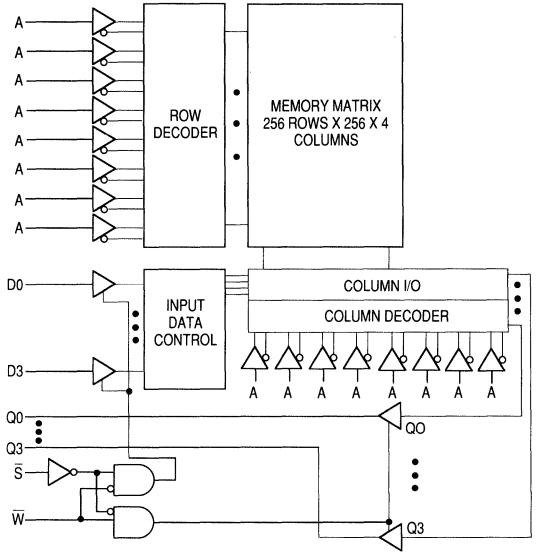


P PACKAGE
300 MIL PLASTIC
CASE 710B

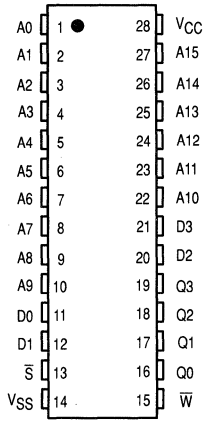


J PACKAGE
300 MIL SOJ
CASE 810B

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN NAMES	
A0–A15	Address Inputs
$\overline{W}$	Write Enable
$\overline{S}$	Chip Select
D0–D3	Data Input
Q0–Q3	Data Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground

All power supply and ground pins must be connected for proper operation of the device.

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MCM67081 TRUTH TABLE

$\overline{S}$	$\overline{W}$	D	Mode	V_{CC} Current	Q	Cycle
H	H	X	Not Selected	I_{ISB}	High-Z	—
H	L	X	Not Selected	I_{SB}	High-Z	—
L	H	X	Read	I_{CCA}	Read	Read Cycle
L	L	H	Write	I_{CCA}	H	Write Cycle
L	L	L	Write	I_{CCA}	L	Write Cycle

X = Don't Care

MCM67082 TRUTH TABLE

$\overline{S}$	$\overline{W}$	D	Mode	V_{CC} Current	Q	Cycle
H	H	X	Not Selected	I_{ISB}	High-Z	—
H	L	X	Not Selected	I_{SB}	High-Z	—
L	H	X	Read	I_{CCA}	Read	Read Cycle
L	L	H	Write	I_{CCA}	High-Z	Write Cycle
L	L	L	Write	I_{CCA}	High-Z	Write Cycle

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to 7.0	V
Voltage Relative to V_{SS} (For Any Pin Except V_{CC})	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 30	mA
Power Dissipation	P_D	2.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high impedence circuits.

This BICMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

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DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3*	V
Input Low Voltage	V_{IL}	− 0.5**	—	0.8	V

*V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 2 ns) for I ≤ 20 mA.
**V_{IL} (min) = − 0.5 V dc; V_{IL} (min) = − 2 V ac (pulse width ≤ 2 ns) for I ≤ 20 mA.

DC CHARACTERISTICS

Parameter		Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})		$I_{lkg(I)}$	—	—	± 1	µA
Output Leakage Current ($\overline{S}$ = V_{IH}, V_{out} = 0 to V_{CC})		$I_{lkg(O)}$	—	—	± 1	µA
AC Supply Current (I_{out} = 0 mA)	MCM67081/MCM67082-10: t_{AVAV} = 10 ns	I_{CCA}	—	150	200	mA
	MCM67081/MCM67082-12: t_{AVAV} = 12 ns		—	140	195	
	MCM67081/MCM67082-15: t_{AVAV} = 15 ns			130	190	
Output Low Voltage (I_{OL} = + 8.0 mA)		V_{OL}	—	—	0.4	V
Output High Voltage (I_{OH} = − 4.0 mA)		V_{OH}	2.4	—	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	4	6	pF
Input/Output Capacitance	$C_{I/O}$	5	7	pF

AC TEST LOADS

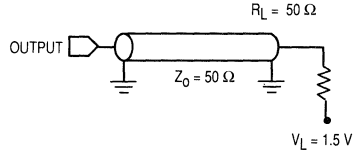


Figure 1

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the module point of view. Thus, the access time is shown as a maximum since the module never provides data later than that time.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns

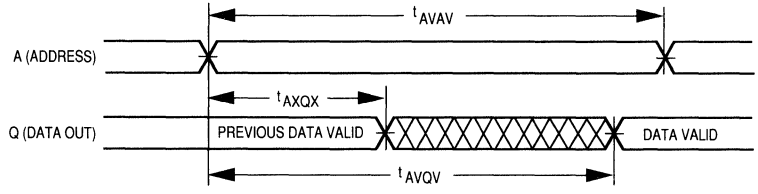
Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1

READ CYCLE TIMING (See Note 1)

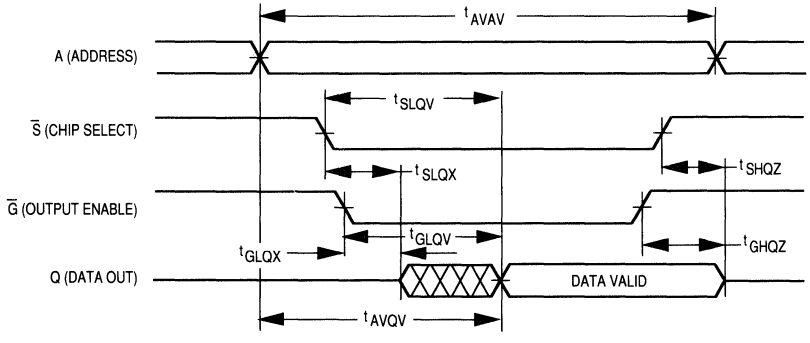
Parameter	Symbol		MCM67081-10 MCM67082-10		MCM67081-12 MCM67082-12		MCM67081-15 MCM67082-15		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	10	—	12	—	15	—	ns	2
Address Access Time	t_{AVQV}	t_{AA}	—	10	—	12	—	15	ns	
Select Access Time	t_{SLQV}	t_{ACS}	—	5	—	6	—	8	ns	
Output Hold from Address Change	t_{AXQX}	t_{OH}	4	—	4	—	4	—	ns	
Select Low to Output Active	t_{SLQX}	t_{LZ}	1	—	1	—	1	—	ns	3, 4, 5
Select High to Output High-Z	t_{SHQZ}	t_{HZ}	0	5	0	6	0	6	ns	3, 4, 5

NOTES:
1. $\overline{W}$ is high for read cycle.
2. All read cycle timings are referenced from the last valid address to the first transitioning address.
3. At any given voltage and temperature, t_{SHQZ} max is less than t_{SLQX} min, both for a given device and from device to device.
4. Transition is measured 100 mV from steady-state voltage with load of Figure 1.
5. This parameter is sampled and not 100% tested.
6. Device is continuously selected ($\overline{S}$ = V_{IL}).
7. Addresses valid prior to or coincident with $\overline{S}$ going low.

READ CYCLE 1 (See Note)



READ CYCLE 2 (See Note)



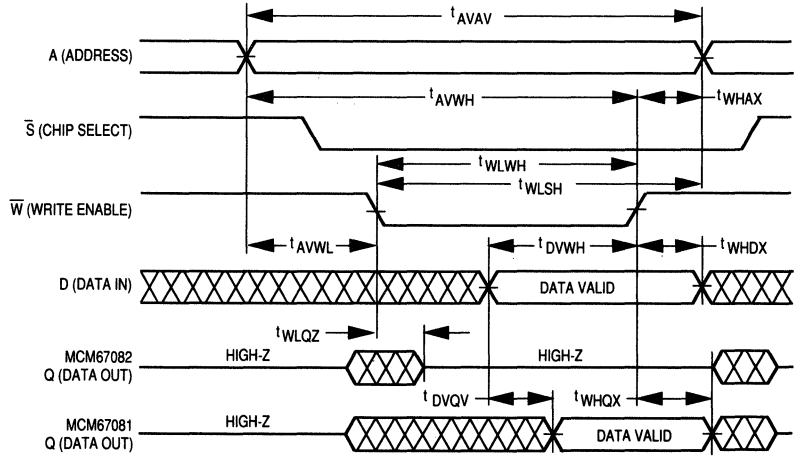
WRITE CYCLE 1 ($\overline{W}$ Controlled, See Note 1)

Parameter	Symbol		MCM67081-10 MCM67082-10		MCM67081-12 MCM67082-12		MCM67081-15 MCM67082-15		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	10	—	12	—	15	—	ns	2
Address Setup Time	t_{AVWL}	t_{AS}	2	—	2	—	2	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	9	—	10	—	12	—	ns	
Write Pulse Width	t_{WLWH}	t_{WP}	6	—	7	—	8	—	ns	
Write Pulse Width	t_{WLSH}	t_{WP}	6	—	7	—	8	—	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	5	—	6	—	7	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	—	0	—	0	—	ns	
Write Low to Data High-Z	t_{WLQZ}	t_{WZ}	0	5	0	6	0	6	ns	3, 4, 5
Write High to Output Active	t_{WHQX}	t_{OW}	2	—	2	—	2	—	ns	3, 4, 5
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	0	—	ns	
Data Valid to Output Valid	t_{DVQV}	t_{ADV}	7	—	8	—	10	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{S}$ low and $\overline{W}$ low.
2. All write cycle timings are referenced from the last valid address to the first transitioning address.
3. Transition is measured 100 mV from steady-state voltage with load of Figure 1.
4. This parameter is sampled and not 100% tested.
5. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min both for a given device and from device to device.

7

WRITE CYCLE 1

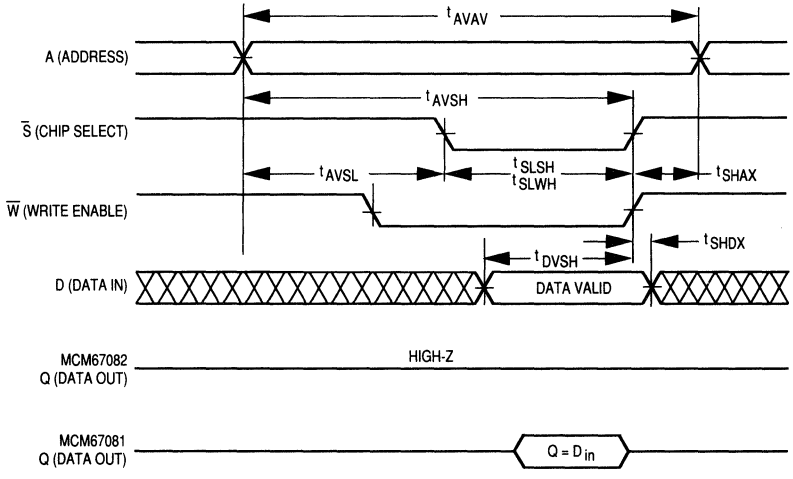


WRITE CYCLE 2 ($\overline{S}$ Controlled, See Notes 1, 2, 3, 4, and 5)

Parameter	Symbol		MCM67081-10 MCM67082-10		MCM67081-12 MCM67082-12		MCM67081-15 MCM67082-15		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	10	—	12	—	15	—	ns	2
Address Setup Time	t_{AVSL}	t_{AS}	2	—	2	—	2	—	ns	
Address Valid to End of Write	t_{AVSH}	t_{AW}	9	—	10	—	12	—	ns	
Select to End of Write	t_{SLSH}	t_{CW}	6	—	7	—	8	—	ns	3, 4
Enable to End of Write	t_{SLWH}	t_{CW}	6	—	7	—	8	—	ns	
Data Valid to End of Write	t_{DVSH}	t_{DW}	5	—	6	—	7	—	ns	
Data Hold Time	t_{SHDX}	t_{DH}	0	—	0	—	0	—	ns	
Write Recovery Time	t_{SHAX}	t_{WR}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{S}$ low and $\overline{W}$ low.
2. All write cycle timings are referenced from the last valid address to the first transitioning address.
3. If $\overline{S}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
4. If $\overline{S}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2



ORDERING INFORMATION
(Order by Full Part Number)

MCM 67081 / 67082 xx C xx xx

- Motorola Memory Prefix
- Part Number
- Package (P = 300 mil Plastic, J = 300 mil SOJ)
- Operating Temperature Range
- Speed (10 = 10 ns, 12 = 12 ns, 15 = 15 ns)
- Shipping Method (R2 = Tape & Reel, Blank = Rails)

Full Part Numbers – MCM67081P10 MCM67081J10 MCM67082P10 MCM67082J10
MCM67081P12 MCM67081J12 MCM67082P12 MCM67082J12
MCM67081P15 MCM67081J15 MCM67082P15 MCM67082J15

Advance Information
QuickRAM™
Fast Static RAM Family

The QuickRAM Family of fast static RAMs is fabricated using Motorola's high-performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

The product family includes devices with four different densities: 294,912 bits, 262,144 bits, 73,728 bits, and 65,536 bits.

These devices meet JEDEC standards for functionality and pinout, and are available in plastic dual-in-line and plastic small-outline J-leaded packages.

- Single 5 V ±10% Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- Fast Access Times: 12, 15, 17, 20, and 25 ns
- Equal Address and Chip Enable Access Times
- Output Enable ($\overline{G}$) Feature for Increased System Flexibility and to Eliminate Bus Contention Problems — on MCM6205/06, MCM6209, MCM6264/65, and MCM6290
- Low Power Operation: 120–160 mA Maximum AC
- Fully TTL Compatible — Three State Output
- Separate Data Input and Output on MCM6207 and MCM6287

7

256K

256K x 1
MCM6207-15, -20, -25

64K x 4
MCM6208-15, -20, -25

64K x 4 with OE
MCM6209-15, -20, -25

32K x 8
MCM6206-17, -20, -25

32K x 9
MCM6205-17, -20, -25

64K

64K x 1
MCM6287-12, -15, -20

16K x 4
MCM6288-12, -15

16K x 4 with OE
MCM6290-12, -15

8K x 8
MCM6264-15, -20

8K x 9
MCM6265-15, -20, -25

CONTENTS

DEVICE NUMERICAL INDEX

Part Number	Access Times (ns)	Organization	Page
MCM6205-17, -20, -25	17, 20, 25	32K x 9	14
MCM6206-17, -20, -25	17, 20, 25	32K x 8	12
MCM6207-15, -20, -25	15, 20, 25	256K x 1	8
MCM6208-15, -20, -25	15, 20, 25	64K x 4	10
MCM6209-15, -20, -25	15, 20, 25	64K x 4 OE	10
MCM6264-15, -20	15, 20	8K x 8	13
MCM6265-15, -20, -25	15, 20, 25	8K x 9	15
MCM6287-12, -15, -20	12, 15, 20	64K x 1	9
MCM6288-12, -15	12, 15	16K x 4	11
MCM6290-12, -15	12, 15	16K x 4 OE	11

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage Relative to V_{SS}	V_{CC}	– 0.5 to +7	V
Voltage on Any Pin, Except V_{CC}, Relative to V_{SS}	V_{in}, V_{out}	– 0.5 to V_{CC} +0.5	V
Output Current (per I/O)	I_{out}	±30	mA
Power Dissipation	P_D	1	W
Temperature Under Bias	T_{bias}	– 10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature-Plastic	T_{stg}	– 55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the OPERATING CONDITIONS. Exposure to voltages higher than the operating voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

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DC OPERATING CONDITIONS AND CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Parameter	Conditions	Symbol	Min	Max	Unit
Supply Voltage	Operating Voltage Range	V_{CC}	4.5	5.5	V
Input High Voltage		V_{IH}	2.2	V_{CC}+0.3*	V
Input Low Voltage		V_{IL}	–0.5**	0.8	V
Input Leakage Current	0 V ≤ V_{in} ≤ V_{CC}	$I_{lkg(I)}$	—	±1	µA
Output Leakage Current	Output(s) Disabled, 0 V ≤ V_{out} ≤ V_{CC}	$I_{lkg(O)}$	—	±1	µA
Output High Voltage	I_{OH} = –4 mA	V_{OH}	2.4	—	V
Output Low Voltage	I_{OL} = 8 mA	V_{OL}	—	0.4	V

*V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 20 ns)

**V_{IL} (min) = –0.5 V dc, V_{IL} (min) = –2 V ac (pulse width ≤ 20 ns)

POWER SUPPLY CURRENTS (AC Operating Conditions Unless Otherwise Noted)

Density	Config.	Device	Parameter	Symbol	-12	-15	-17	-20	-25	Unit
64K	16K x 4	MCM6288/90	AC Active Supply Current (I_{out} = 0 mA, V_{CC} = Max, f = f_{max})	I_{CCA}	150	140	—	—	—	mA
	64K x 1	MCM6287			150	140	—	130	—	
	8K x 8	MCM6264			—	140	—	130	—	
	8K x 9	MCM6265			—	140	—	130	120	
	All	All	AC Standby Current ($\overline{E}$ = V_{IH}, V_{CC} = Max, f = f_{max})	I_{SB1}	45	40	—	35	30	mA
	All	All	CMOS Standby Current (V_{CC} = Max, f = 0 MHz, $\overline{E} \geq V_{CC} - 0.2$ V* $V_{in} \leq V_{SS}$ +0.2 V, or $\geq V_{CC}$ −0.2 V)	I_{SB2}	20	20	—	20	20	mA
256K	64K x 4	MCM6208/09	AC Active Supply Current (I_{out} = 0 mA, V_{CC} = Max, f = f_{max})	I_{CCA}	—	155	—	145	135	mA
	256K x 1	MCM6207			—	150	—	140	130	
	32K x 8	MCM6206			—	—	155	150	140	
	32K x 9	MCM6205			—	—	160	155	145	
	All	All	AC Standby Current ($\overline{E}$ = V_{IH}, V_{CC} = Max, f = f_{max})	I_{SB1}	—	50	45	45	40	mA
	All	All	CMOS Standby Current (V_{CC} = Max, f = 0 MHz, $\overline{E} \geq V_{CC} - 0.2$ V* $V_{in} \leq V_{SS}$ +0.2 V, or $\geq V_{CC}$ −0.2 V)	I_{SB2}	—	20	20	20	20	mA

*For devices with multiple chip enables of opposite polarity, $\overline{E1} \geq V_{CC} - 0.2$ V or E2 ≤ V_{SS} + 0.2 V

CAPACITANCE (f = 1 MHz, dV = 3 V, T_A = 25°C, Periodically sampled rather than 100% tested)

Characteristic	Symbol	Max	Unit
Address and Data Input Capacitance	C_{in}		pF
MCM6287 (64K x 1), MCM6288/90 (16K x 4)		6	
MCM6264 (8K x 8), MCM6265 (8K x 9)		6	
MCM6207 (256K x 1), MCM6208/09 (64K x 4)		6	
MCM6205 (32K x 9), MCM6206 (32K x 8)		6	
Control Pin Input Capacitance ($\overline{E}$,* $\overline{G}$, $\overline{W}$)	C_{in}		pF
MCM6287 (64K x 1), MCM6288/90 (16K x 4)		6	
MCM6264 (8K x 8), MCM6265 (8K x 9)		6	
MCM6207 (256K x 1), MCM6208/09 (64K x 4)		6	
MCM6205 (32K x 9), MCM6206 (32K x 8)		8	
Output Capacitance	C_{out}		pF
MCM6287 (64K x 1), MCM6288/90 (16K x 4)		7	
MCM6264 (8K x 8), MCM6265 (8K x 9)		7	
MCM6207 (256K x 1), MCM6208/09 (64K x 4)		8	
MCM6205 (32K x 9), MCM6206 (32K x 8)		8	

*For devices with multiple chip enables, $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E}$.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3 V
Input Rise/Fall Time ..... 5 ns

Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... Figure 1A Unless Otherwise Noted

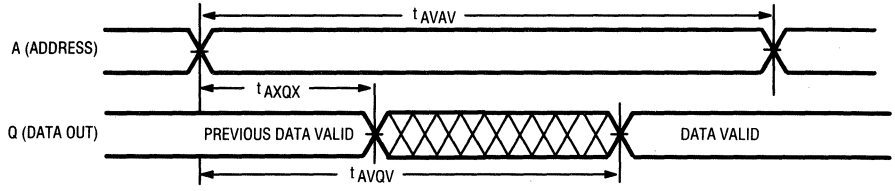
READ CYCLE (See Notes 1 and 2)

Product Family	Configuration	-12	-15	-17	-20	-25	Density
MCM6288 and MCM6290	16K x 4	√	√	—	EXISTING MOTOROLA		
MCM6287	64K x 1	√	√	—	√	PRODUCTS	64K
MCM6264	8K x 8		√	—	√		
MCM6265	8K x 9		√	—	√	√	
MCM6208 and MCM6209	64K x 4		√	—	√	√	
MCM6207	256K x 1	FUTURE	√	—	√	√	256K
MCM6206	32K x 8	MOTOROLA		√	√	√	
MCM6205	32K x 9	PRODUCTS		√	√	√	

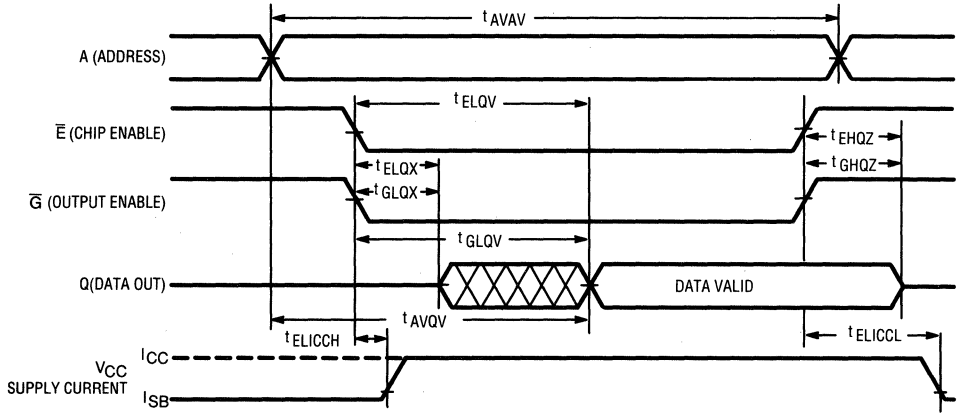
Parameter	Symbol Std	Symbol Alt	-12 Min	-12 Max	-15 Min	-15 Max	-17 Min	-17 Max	-20 Min	-20 Max	-25 Min	-25 Max	Unit	Notes
Read Cycle Time	t_{AVAV}	t_{RC}	12	—	15	—	17	—	20	—	25	—	ns	3
Address Access Time	t_{AVQV}	t_{AA}	—	12	—	15	—	17	—	20	—	25	ns	
Enable Access Time	t_{ELQV}	t_{ACS}	—	12	—	15	—	17	—	20	—	25	ns	4
Output Enable Access Time	t_{GLQV}	t_{OE}	—	6	—	8	—	9	—	10	—	12	ns	
Output Hold from Address Change	t_{AXQX}	t_{OH}	4	—	4	—	4	—	4	—	4	—	ns	
Enable Low to Output Active	t_{ELQX}	t_{CLZ}	4	—	4	—	4	—	4	—	4	—	ns	5,6,7
Output Enable Low to Output Active	t_{GLQX}	t_{OLZ}	0	—	0	—	0	—	0	—	0	—	ns	5,6,7
Enable High to Output High-Z	t_{EHQZ}	t_{CHZ}	0	6	0	8	0	8	0	9	0	10	ns	5,6,7
Output Enable High to Output High-Z	t_{GHQZ}	t_{OHZ}	0	6	0	7	0	8	0	8	0	10	ns	5,6,7
Power Up Time	t_{ELICCH}	t_{PU}	0	—	0	—	0	—	0	—	0	—	ns	
Power Down Time	t_{EHICCL}	t_{PD}	—	12	—	15	—	17	—	20	—	25	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. For devices with multiple chip enables, $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E}$.
3. All timings are referenced from the last valid address to the first transitioning address.
4. Addresses valid prior to or coincident with $\overline{E}$ going low.
5. At any given voltage and temperature, t_{EHQZ} max < t_{ELQX} min, and t_{GHQZ} max < t_{GLQX} min, both for a given device and from device to device.
6. Transition is measured 500 mV from steady-state voltage with load of Figure 1B.
7. This parameter is sampled and not 100% tested.
8. Device is continuously selected. $\overline{E} \le V_{IL}$ and $\overline{G} \le V_{IL}$.

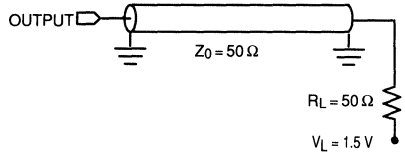
READ CYCLE 1 (See Note 8)



READ CYCLE 2 (See Notes 2 and 4)



AC TEST LOADS



See Output Load Conditions, page 18.

Figure 1A

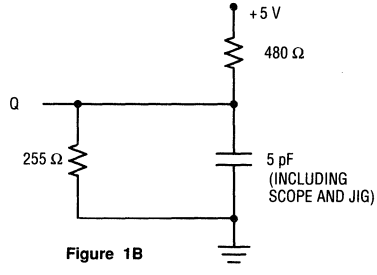
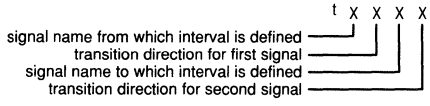


Figure 1B

TIMING PARAMETER ABBREVIATIONS



The transition definitions used in this data sheet are:

- H = transition to high
- L = transition to low
- V = transition to valid
- X = transition to invalid or don't care
- Z = transition to off (high impedance)

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device output will be valid no later than that time.

WRITE CYCLES

Product Family	Configuration	-12	-15	-17	-20	-25	Density
MCM6288 and MCM6290	16K x 4	√	√	—	EXISTING MOTOROLA PRODUCTS		64K
MCM6287	64K x 1	√	√	—	√		
MCM6264	8K x 8	FUTURE MOTOROLA PRODUCTS	√	—	√		
MCM6265	8K x 9		√	—	√	√	
MCM6208 and MCM6209	64K x 4		√	—	√	√	256K
MCM6207	256K x 1		√	—	√	√	
MCM6206	32K x 8			√	√	√	
MCM6205	32K x 9			√	√	√	

WRITE CYCLE 1 ($\overline{W}$ Controlled) (See Notes 1, 2, and 3)

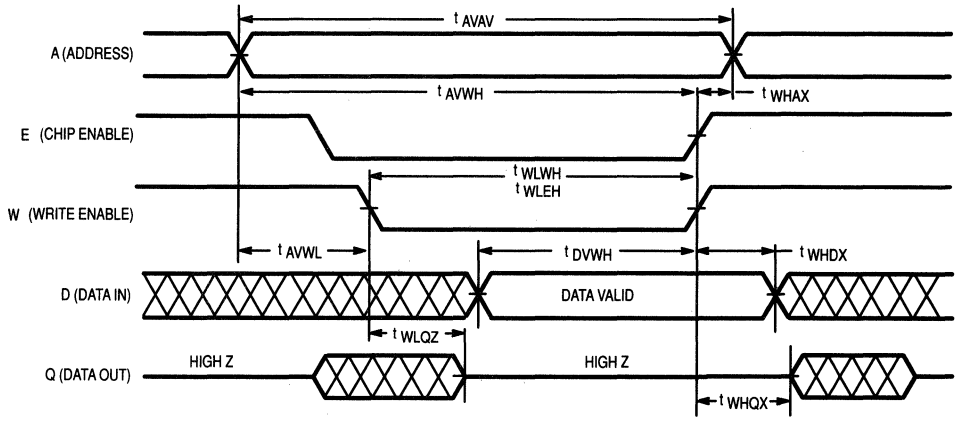
Parameter	Symbol Std	Symbol Alt	-12 Min	-12 Max	-15 Min	-15 Max	-17 Min	-17 Max	-20 Min	-20 Max	-25 Min	-25 Max	Unit	Notes
Write Cycle Time	t_{AVAV}	t_{WC}	12	—	15	—	17	—	20	—	25	—	ns	4
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	10	—	12	—	14	—	15	—	20	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	t_{WP}	10	—	12	—	14	—	15	—	20	—	ns	
Write Pulse Width, $\overline{G}$ High (Output Enable devices)	t_{WLWH}, t_{WLEH}	t_{WP}	8	—	10	—	11	—	12	—	15	—	ns	5
Data Valid to End of Write	t_{DVWH}	t_{DW}	6	—	7	—	8	—	8	—	10	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	—	0	—	0	—	0	—	0	—	ns	
Write Low to Output High-Z	t_{WLQZ}	t_{WZ}	0	6	0	7	0	8	0	8	0	10	ns	6,7,8
Write High to Output Active	t_{WHQX}	t_{OW}	4	—	4	—	4	—	4	—	4	—	ns	6,7,8
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	0	—	0	—	0	—	ns	

WRITE CYCLE 2 ($\overline{E}$ Controlled) (See Notes 1, 2, and 3)

Parameter	Symbol Std	Symbol Alt	-12 Min	-12 Max	-15 Min	-15 Max	-17 Min	-17 Max	-20 Min	-20 Max	-25 Min	-25 Max	Unit	Notes
Write Cycle Time	t_{AVAV}	t_{WC}	12	—	15	—	17	—	20	—	25	—	ns	4
Address Setup Time	t_{AVEL}	t_{AS}	0	—	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	10	—	12	—	14	—	15	—	20	—	ns	
Enable to End of Write	t_{ELEH}, t_{ELWH}	t_{CW}	8	—	10	—	11	—	12	—	15	—	ns	9,10
Data Valid to End of Write	t_{DVEH}	t_{DW}	6	—	7	—	8	—	8	—	10	—	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	—	0	—	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	—	0	—	0	—	0	—	0	—	ns	

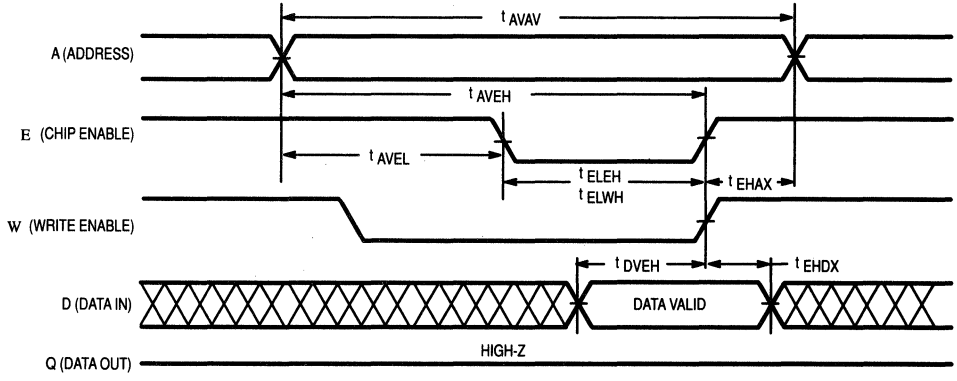
NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. For devices with multiple chip enables, $\overline{E}1$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E}$.
3. For Output Enable devices, if $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
4. All timings are referenced from the last valid address to the first transitioning address.
5. For Output Enable devices, if $\overline{G} \geq V_{IH}$, the output will remain in a high impedance state.
6. At any given voltage and temperature, t_{WLQG} max < t_{WHQX} min, both for a given device and from device to device.
7. Transition is measured 500 mV from steady-state voltage with load of Figure 1B.
8. This parameter is sampled and not 100% tested.
9. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
10. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance state.

WRITE CYCLE 1 (See Note 2)



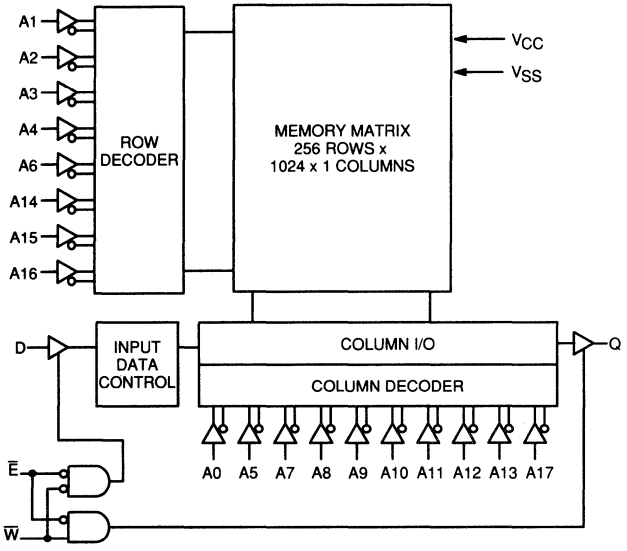
7

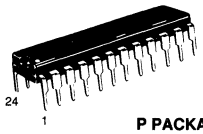
WRITE CYCLE 2 (See Note 2)



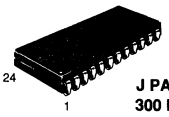
256K x 1 Bit Fast Static RAM

MCM6207



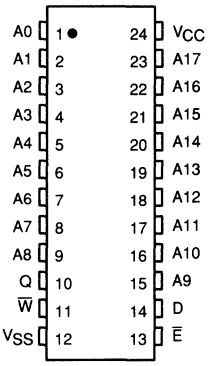


P PACKAGE
300 MIL PLASTIC
CASE 724A



J PACKAGE
300 MIL SOJ
CASE 810A

PIN ASSIGNMENT



PIN NAMES	
A0-A17 ..... Address Input	Q ..... Data Output
E ..... Chip Enable	VCC ..... +5 V Power Supply
W ..... Write Enable	VSS ..... Ground
D ..... Data Input	

MCM6207 TRUTH TABLE (X = don't care)

E	W	Mode	V_{CC} Current	Output	Cycle
H	X	Not Selected	I_{SB1}, I_{SB2}	High-Z	—
L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	L	Write	I_{CCA}	High-Z	Write Cycle

ORDERING INFORMATION (Order by Full Part Number)

MCM 6207 X XX XX

Motorola Memory Prefix — MCM

Part Number — 6207

Package (P = 300 mil Plastic DIP, J = 300 mil SOJ) — X

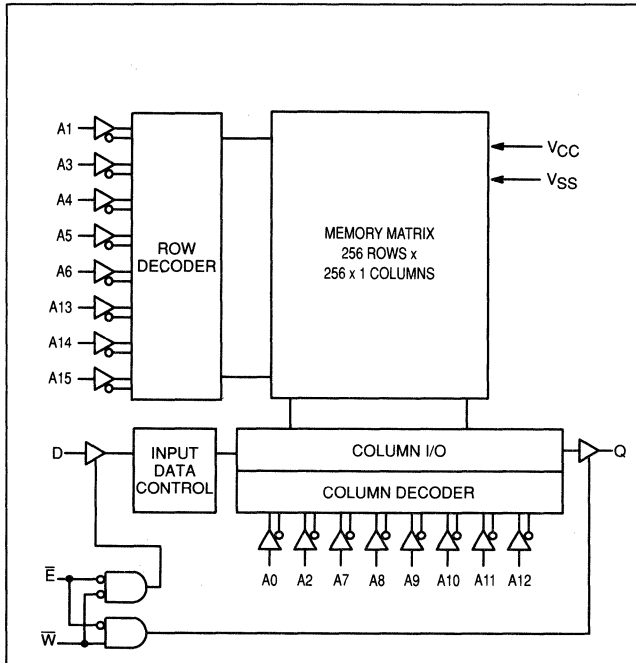
Speed (15 = 15 ns, 20 = 20 ns, 25 = 25 ns) — XX

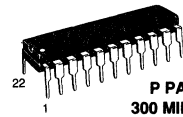
Shipping Method (R2 = Tape & Reel, Blank = Rails) — XX

Full Part Numbers—MCM6207P15 MCM6207J15 MCM6207J15R2
MCM6207P20 MCM6207J20 MCM6207J20R2
MCM6207P25 MCM6207J25 MCM6207J25R2

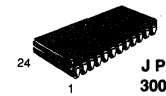
64K x 1 Bit Fast Static RAM

MCM6287



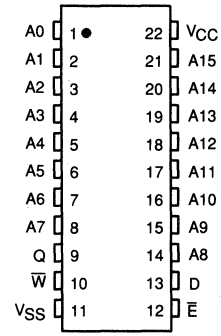


P PACKAGE
300 MIL PLASTIC
CASE 736A

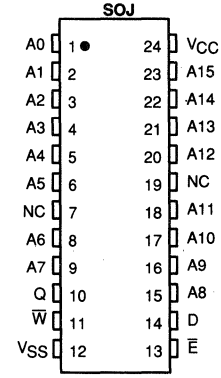


J PACKAGE
300 MIL SOJ
CASE 810A

DUAL-IN-LINE



SOJ



PIN NAMES			
A0-A15	Address Input	Q	Data Output
$\overline{E}$	Chip Enable	V_{CC}	+5 V Power Supply
$\overline{W}$	Write Enable	V_{SS}	Ground
D	Data Input	NC	No Connection

MCM6287 TRUTH TABLE (X = don't care)

$\overline{E}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	Not Selected	I_{SB1}, I_{SB2}	High-Z	—
L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	L	Write	I_{CCA}	High-Z	Write Cycle

ORDERING INFORMATION (Order by Full Part Number)

MCM 6287 X XX XX

Motorola Memory Prefix — MCM

Part Number — 6287

Package (P = 300 mil Plastic DIP, J = 300 mil SOJ) — X

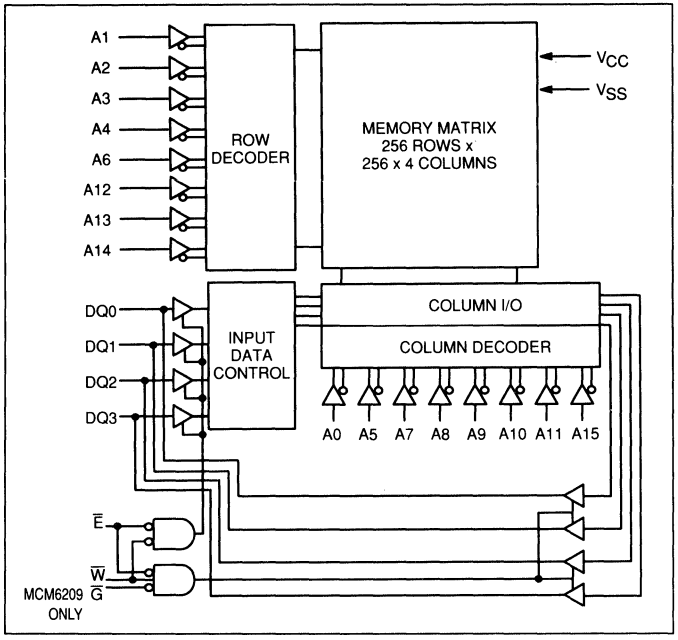
Speed (12 = 12 ns, 15 = 15 ns, 20 = 20 ns) — XX

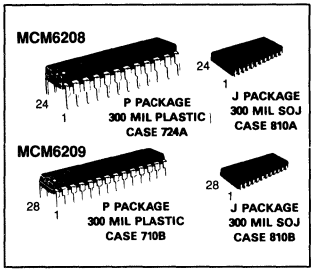
Shipping Method (R2 = Tape & Reel, Blank = Rails) — XX

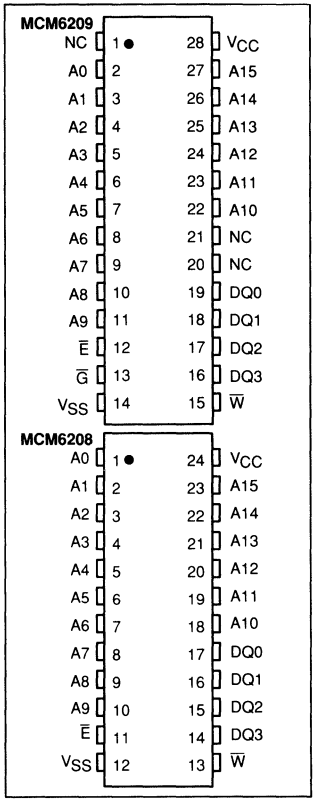
Full Part Numbers—MCM6287P12 MCM6287J12 MCM6287J12R2
MCM6287P15 MCM6287J15 MCM6287J15R2
MCM6287P20 MCM6287J20 MCM6287J20R2

64K x 4 Bit Fast Static RAMs

MCM6208
MCM6209







PIN NAMES			
A0-A15	Address Input	$\overline{E}$	Chip Enable
DQ0–DQ3	Data Input/Output	NC	No Connection
$\overline{W}$	Write Enable	V_{CC}	+5 V Power Supply
$\overline{G}$ (MCM6209)	Output Enable	V_{SS}	Ground

MCM6208 TRUTH TABLE (X = don't care)

$\overline{E}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	Not Selected	I_{SB1}, I_{SB2}	High-Z	—
L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	L	Write	I_{CCA}	High-Z	Write Cycle

MCM6209 TRUTH TABLE (X = don't care)

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	Not Selected	I_{SB1}, I_{SB2}	High-Z	—
L	H	H	Output Disabled	I_{CCA}	High-Z	—
L	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	X	L	Write	I_{CCA}	High-Z	Write Cycle

ORDERING INFORMATION (Order by Full Part Number)

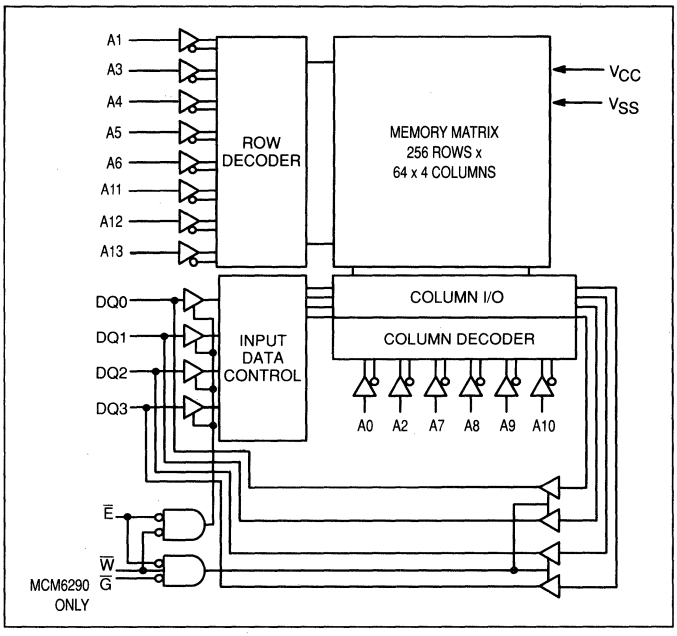
MCM 62XX X XX XX

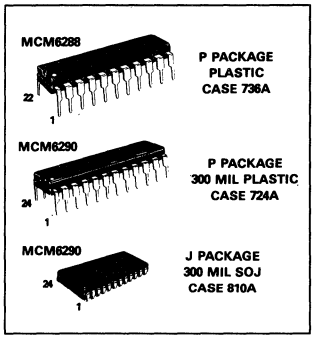
- MCM — Motorola Memory Prefix
- 62XX — Part Number
- X — Package (P = 300 mil Plastic DIP, J = 300 mil SOJ)
- XX — Speed (15 = 15 ns, 20 = 20 ns, 25 = 25 ns)
- XX — Shipping Method (R2 = Tape & Reel, Blank = Rails)

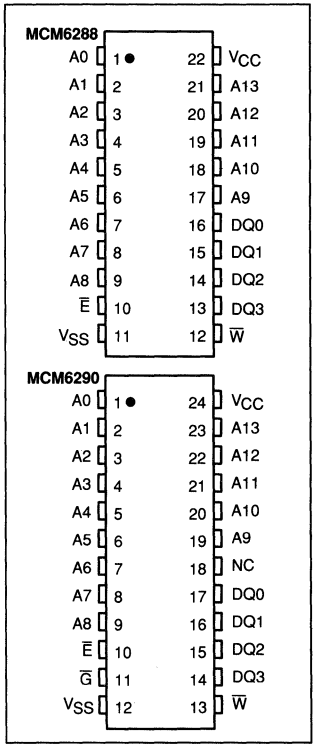
Full Part Numbers—MCM6208P15 MCM6208J15 MCM6208J15R2 MCM6209P15 MCM6209J15 MCM6209J15R2
MCM6208P20 MCM6208J20 MCM6208J20R2 MCM6209P20 MCM6209J20 MCM6209J20R2
MCM6208P25 MCM6208J25 MCM6208J25R2 MCM6209P25 MCM6209J25 MCM6209J25R2

16K x 4 Bit Fast Static RAMs

MCM6288
MCM6290







PIN NAMES	
A0-A13 ..... Address Input	$\overline{E}$ ..... Chip Enable
DQ0–DQ3 ..... Data Input/Output	NC ..... No Connection
$\overline{W}$ ..... Write Enable	V_{CC} ..... +5 V Power Supply
$\overline{G}$ (MCM6290) ..... Output Enable	V_{SS} ..... Ground

MCM6288 TRUTH TABLE (X = don't care)

$\overline{E}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	Not Selected	I_{SB1}, I_{SB2}	High-Z	—
L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	L	Write	I_{CCA}	High-Z	Write Cycle

MCM6290 TRUTH TABLE (X = don't care)

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	Not Selected	I_{SB1}, I_{SB2}	High-Z	—
L	H	H	Output Disabled	I_{CCA}	High-Z	—
L	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	X	L	Write	I_{CCA}	High-Z	Write Cycle

ORDERING INFORMATION (Order by Full Part Number)

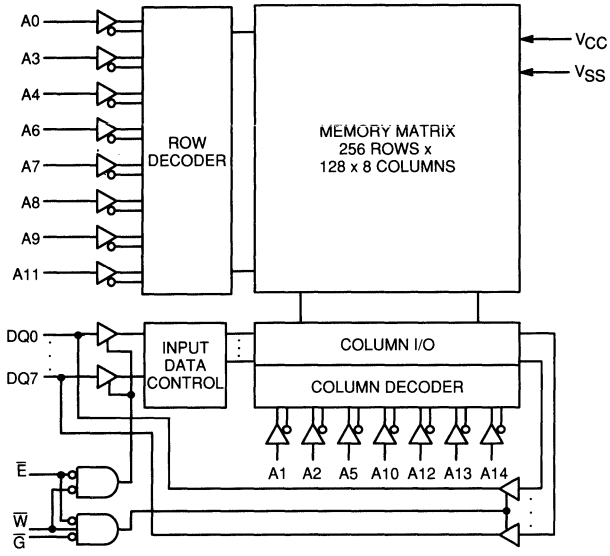
MCM 62XX X XX XX

Motorola Memory Prefix — MCM
Part Number — 62XX
Package (P = 300 mil Plastic DIP, J = 300 mil SOJ) — X
Speed (12 = 12 ns, 15 = 15 ns) — XX
Shipping Method (R2 = Tape & Reel, Blank = Rails) — XX

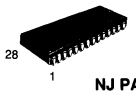
Full Part Numbers—MCM6288P12 MCM6290P12 MCM6290J12 MCM6290J12R2
MCM6288P15 MCM6290P15 MCM6290J15 MCM6290J15R2

32K x 8 Bit Fast Static RAM

MCM6206

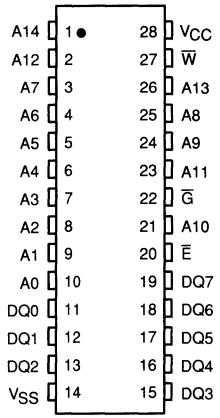


NP PACKAGE
300 MIL PLASTIC
CASE 710B



NJ PACKAGE
300 MIL SOJ
CASE 810B

PIN ASSIGNMENT



PIN NAMES	
A0-A14 ..... Address Input	E ..... Chip Enable
DQ0–DQ7 ..... Data Input/Output	VCC ..... +5 V Power Supply
W ..... Write Enable	VSS ..... Ground
G ..... Output Enable	

MCM6206 TRUTH TABLE (X = don't care)

E	G	W	Mode	VCC Current	Output	Cycle
H	X	X	Not Selected	I_{SB1}, I_{SB2}	High-Z	—
L	H	H	Output Disabled	I_{CCA}	High-Z	—
L	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	X	L	Write	I_{CCA}	High-Z	Write Cycle

ORDERING INFORMATION (Order by Full Part Number)

MCM 6206 X XX XX

Motorola Memory Prefix — MCM

Part Number — 6206

Package (NP = 300 mil Plastic DIP, NJ = 300 mil SOJ) — X

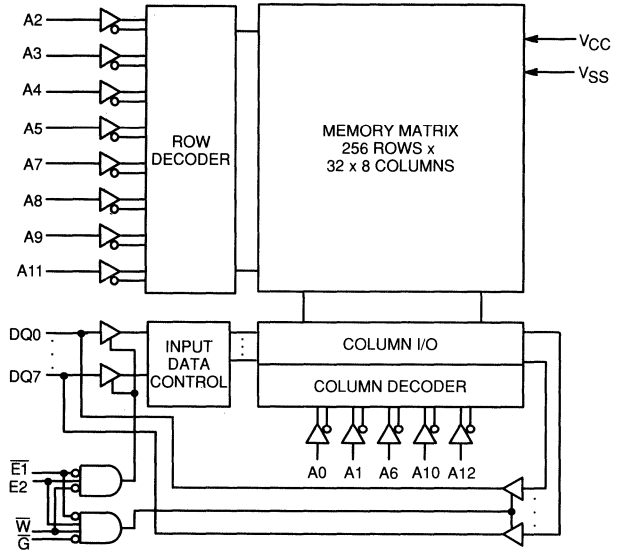
Speed (17 = 17 ns, 20 = 20 ns, 25 = 25 ns) — XX

Shipping Method (R2 = Tape & Reel, Blank = Rails) — XX

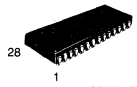
Full Part Numbers—MCM6206NP17 MCM6206NJ17 MCM6206NJ17R2
MCM6206NP20 MCM6206NJ20 MCM6206NJ20R2
MCM6206NP25 MCM6206NJ25 MCM6206NJ25R2

8K x 8 Bit Fast Static RAM

MCM6264

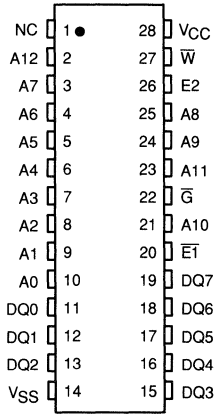


P PACKAGE
300 MIL PLASTIC
CASE 710B



NJ PACKAGE
300 MIL SOJ
CASE 810B

PIN ASSIGNMENT



PIN NAMES

A0-A12 ..... Address Input	$\overline{E1}$, E2 ..... Chip Enable
DQ0–DQ7 ..... Data Input/Output	NC ..... No Connection
$\overline{W}$ ..... Write Enable	V_{CC} ..... +5 V Power Supply
$\overline{G}$ ..... Output Enable	V_{SS} ..... Ground

MCM6264 TRUTH TABLE (X = don't care)

$\overline{E1}$	E2	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	X	Not Selected	I_{SB1}, I_{SB2}	High-Z	—
X	L	X	X	Not Selected	I_{SB1}, I_{SB2}	High-Z	—
L	H	H	H	Output Disabled	I_{CCA}	High-Z	—
L	H	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	H	X	L	Write	I_{CCA}	High-Z	Write Cycle

ORDERING INFORMATION (Order by Full Part Number)

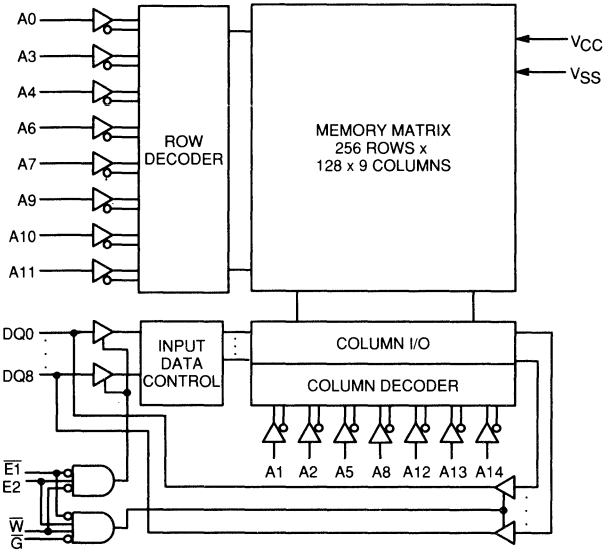
MCM 6264 X XX XX

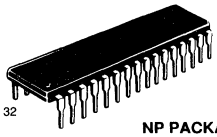
- MCM — Motorola Memory Prefix
- 6264 — Part Number
- X — Package (P = 300 mil Plastic DIP, NJ = 300 mil SOJ)
- XX — Speed (15 = 15 ns, 20 = 20 ns)
- XX — Shipping Method (R2 = Tape & Reel, Blank = Rails)

Full Part Numbers—MCM6264P15 MCM6264NJ15 MCM6264NJ15R2
MCM6264P20 MCM6264NJ20 MCM6264NJ20R2

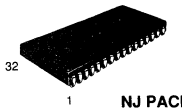
32K x 9 Bit Fast Static RAM

MCM6205



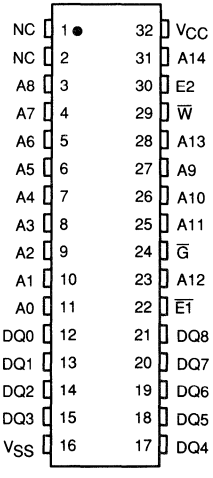


NP PACKAGE
300 MIL PLASTIC
CASE 853



NJ PACKAGE
300 MIL SOJ
CASE 857

PIN ASSIGNMENT



PIN NAMES	
A0-A14 ..... Address Input	$\overline{E1}$, E2 ..... Chip Enable
DQ0–DQ8 ..... Data Input/Output	NC ..... No Connection
$\overline{W}$ ..... Write Enable	V_{CC} ..... +5 V Power Supply
$\overline{G}$ ..... Output Enable	V_{SS} ..... Ground

MCM6205 TRUTH TABLE (X = don't care)

$\overline{E1}$	E2	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	X	Not Selected	I_{SB1}, I_{SB2}	High-Z	—
X	L	X	X	Not Selected	I_{SB1}, I_{SB2}	High-Z	—
L	H	H	H	Output Disabled	I_{CCA}	High-Z	—
L	H	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	H	X	L	Write	I_{CCA}	High-Z	Write Cycle

ORDERING INFORMATION (Order by Full Part Number)

MCM 6205 X XX XX

Motorola Memory Prefix

Part Number

Shipping Method (R2 = Tape & Reel, Blank = Rails)

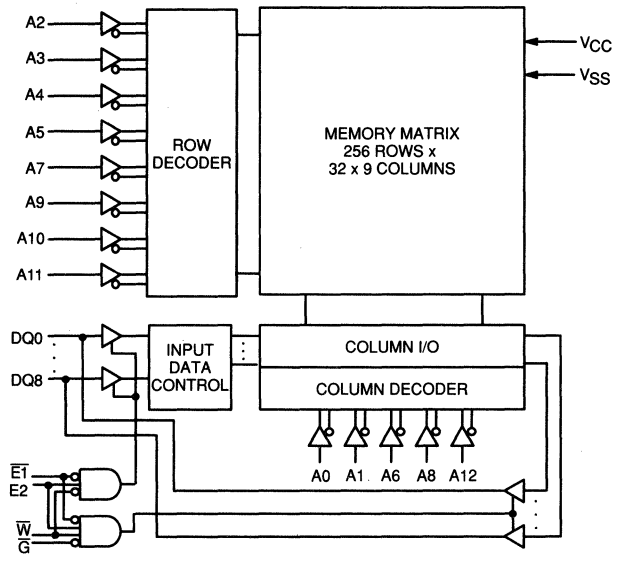
Speed (17 = 17 ns, 20 = 20 ns, 25 = 25 ns)

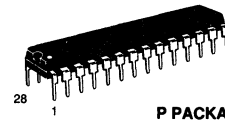
Package (NP = 300 mil Plastic DIP, NJ = 300 mil SOJ)

Full Part Numbers—MCM6205NP17 MCM6205NJ17 MCM6205NJ17R2
MCM6205NP20 MCM6205NJ20 MCM6205NJ20R2
MCM6205NP25 MCM6205NJ25 MCM6205NJ25R2

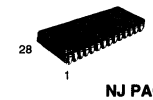
8K x 9 Bit Fast Static RAM

MCM6265



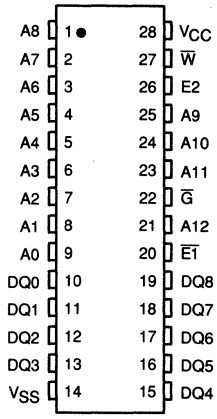


P PACKAGE
300 MIL PLASTIC
CASE 710B



NJ PACKAGE
300 MIL SOJ
CASE 810B

PIN ASSIGNMENT



PIN NAMES	
A0-A12 ..... Address Input	$\overline{E1}$, E2 ..... Chip Enable
DQ0–DQ8 ..... Data Input/Output	V_{CC} ..... +5 V Power Supply
$\overline{W}$ ..... Write Enable	V_{SS} ..... Ground
$\overline{G}$ ..... Output Enable	

MCM6265 TRUTH TABLE (X = don't care)

$\overline{E1}$	E2	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	X	Not Selected	I_{SB1}, I_{SB2}	High-Z	—
X	L	X	X	Not Selected	I_{SB1}, I_{SB2}	High-Z	—
L	H	H	H	Output Disabled	I_{CCA}	High-Z	—
L	H	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	H	X	L	Write	I_{CCA}	High-Z	Write Cycle

ORDERING INFORMATION (Order by Full Part Number)

MCM 6265 X XX XX

Motorola Memory Prefix — MCM
Part Number — 6265
Package (P = 300 mil Plastic DIP, NJ = 300 mil SOJ) — X
Speed (15 = 15 ns, 20 = 20 ns, 25 = 25 ns) — XX
Shipping Method (R2 = Tape & Reel, Blank = Rails) — XX

Full Part Numbers—MCM6265P15 MCM6265NJ15 MCM6265NJ15R2
MCM6265P20 MCM6265NJ20 MCM6265NJ20R2
MCM6265P25 MCM6265NJ25 MCM6265NJ25R2

OUTPUT LOAD CONDITIONS

INTRODUCTION

This review describes the ac loading used for testing this family of parts. Component test engineers should pay careful attention to the test conditions and derating curves for deviations from the specified load. This information is also applicable for system engineers calculating required device speed for a given environment. This information will help the user make the appropriate choice of device performance for their needs.

As device access times decrease, so do output transition times. With faster rise and fall times come additional problems associated with output and signal path impedances. In any system running at frequencies where the propagation delay of a signal path (t_{pd}) is greater than 1/2 of the total signal transition time, transmission line effects will be seen on the signal. This results in overshoot and undershoot at the load end of a conductor, which can cause problems in testing, or in actual use of the device. This discussion gives a brief overview of the factors contributing to these effects, and the measures that can be used to predict or eliminate them. For a detailed discussion of both PC board layout considerations and applicable transmission line theory, consult the *MECL System Design Handbook*, publication HB205R1, Motorola, Inc., 1983.

DEFINITION OF TERMS

t_{pd}	Propagation delay in seconds
L_0	Inductance in henries/meter
C_0	Capacitance in farads/meter
R_L	Load resistance in ohms
$R_{DS(on)}$	Resistance from drain to source of a FET device when on
R_O	Output resistance in ohms. For CMOS devices, this is the $R_{DS(on)}$ resistance of the output devices.
R_{OH}	Output resistance for a high, or "1", signal from the device
R_{OL}	Output resistance for a low, or "0", signal from the device
ρ_L	Reflection coefficient of the load end of a signal
ρ_S	Reflection coefficient of the source end of a signal, the device output
V_L	Termination voltage of the load resistor in a transmission line termination network

TRANSMISSION LINE OVERVIEW

What is a transmission line and how does it affect output waveforms? In simple terms, a transmission line is a signal path that exhibits a characteristic impedance. The type of lines discussed in this paper are primarily microstrip (Figure 2A) and stripline signal paths (Figure 2B) found in most PC boards today. The inductance and capacitance of these lines are a function of the line thickness and width in combination with the dielectric properties of the PC board material and the distance of the line from the ground plane. The impedance of the line is determined by these characteristics and the additional distributed capacitance from other devices on the line.

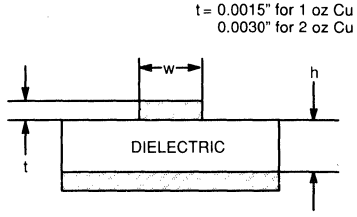


Figure 2A. Microstrip Signal Path

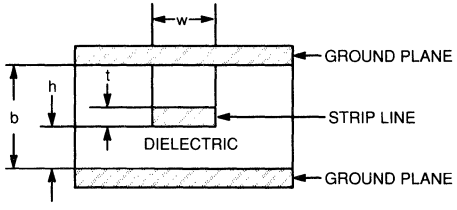


Figure 2B. Stripline Signal Path

The characteristic impedance of a microstrip or stripline path is given by the formula $Z_0 = \sqrt{L_0 / C_0}$. The propagation delay of the path, t_{pd}, is $t_{pd} = \sqrt{L_0 C_0} \times \text{length} = Z_0 C_0 \times \text{length}$. For example, the propagation delay of a microstrip line on G10 epoxy/glass material is approximately 1.76 ns/ft, while the delay for a stripline is about 2.27 ns/ft.

The effect of a transmission line on a device output depends on the electrical length of the line. In all cases, a signal traveling down the line will be affected at the end of the line if it is not terminated with a resistor of the characteristic impedance of the line. The amount of effect is determined by the reflection coefficient of the load, ρ_L, where:

$$\rho_L = \left(\frac{R_L - Z_0}{R_L + Z_0}\right) \quad (1)$$

This reflection occurs at a time t_{pd} after a change at the source of the signal. A similar reflection occurs at $2t_{pd}$ after this new signal has returned from the load to the source, and is determined by the source reflection coefficient, ρ_S, where:

$$\rho_S = \left(\frac{R_O - Z_0}{R_O + Z_0}\right) \quad (2)$$

R_O is the output resistance of the device. In the case of an electrical line length with tpd less than 1/2 of the rise/fall time of the output signal, the transmission line effects are seen as a delay of the signal transition times. This is caused by the load reflection returning to the source during the actual signal transition and being included in the duration of the signal. For the case of an electrical length with t_{pd} greater than 1/2 of the rise/fall time of the output signal, the reflection effects may be seen

directly. In severe cases, signal overshoot or undershoot can cause an invalid level to be seen at the load end at $3t_{pd}$.

The formulas for determining reflection coefficients require knowledge of the output impedance of the device, the characteristic impedance of the signal path, and the termination resistance. The goal of termination is to guarantee that the output signal at the receiving end (load) has enough margin to keep reflection effects from causing a false level to be detected. In an ideal case, the termination resistance is equal to the characteristic impedance of the line, and therefore, no reflection is generated at the load. In that one case, the impedance mismatch at the source is of importance only for signal rise time, V_{OH} and V_{OL} considerations.

The effect of additional distributed capacitance on a transmission line is a reduction in impedance resulting in little change to t_{pd}. This additional capacitance does, however, change the signal transition times resulting in a longer rise and fall time.

OUTPUT BUFFERS

The schematic drawing for a typical CMOS TTL output buffer is shown in Figure 3A. Figure 3B shows the equivalent circuit as actually implemented in many devices. The actual values for R_{OH} and R_{OL} vary from design to design but the range of values is similar.

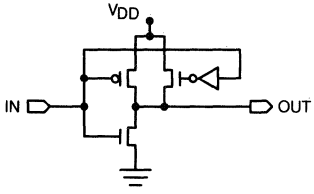


Figure 3A. Typical Output Buffer

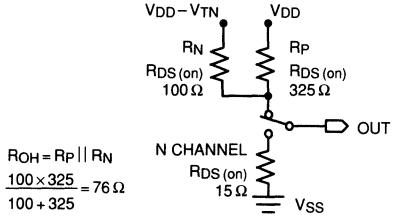


Figure 3B. Effective Circuit

As can be seen from Figure 3, the output impedance of a TTL output buffer is different for high and low output signals. This relation, along with the choice of V_{DD} level, termination resistance, and voltage determine the output high and low levels the part will produce in the system. In a dc condition with R_L = 50 Ω = and V_L = 1.5 V, the output voltages would be:

$$V_{OL} = V_{SS} + (V_L - V_{SS})\left(\frac{R_{OL}}{R_{OL} + R_L}\right)$$

$$V_{OL} = 0\text{ V} + (1.5\text{ V} - 0\text{ V})\left(\frac{15\ \Omega}{15\ \Omega + 50\ \Omega}\right)$$

$$V_{OL} = 0.35\text{ V} \qquad (3)$$

$$V_{OH} = V_L + \left(V_{DD} - V_L - V_{TN}\frac{R_P}{R_P + R_N}\right)\left(\frac{R_L}{R_L + R_{OH}}\right)$$

$$V_{OH} = 1.5\text{ V} + \left(4.4\text{ V} - 1.5\text{ V} - 1.2\text{ V}\ \frac{325\ \Omega}{100\ \Omega + 325\ \Omega}\right)\left(\frac{50\ \Omega}{50\ \Omega + 76\ \Omega}\right)$$

$$V_{OH} = 2.33\text{ V} \qquad (4)$$

TRADITIONAL TTL OUTPUT LOAD SPECIFICATIONS

The output loading typically specified in the industry until now is shown in Figure 4A. The load consists of a resistor network and capacitance. The values for the network were chosen to present a dc load of 8 mA during an output low condition ($V_{OL} \leq 0.4$ V) and –4 mA for an output high ($V_{OH} \geq 2.4$ V). A 5 V supply was chosen as the termination supply and a divider network was calculated to provide the specified currents. In addition, a lumped capacitive load of 30 pF was added to the output to represent input loading from other devices. In actual practice during testing, the load used is a Thevenin equivalent as shown in Figure 4B, with capacitance being provided by the 50 Ω transmission line connection to the test head and the test fixture capacitance.

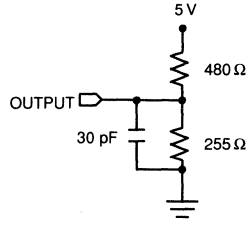


Figure 4A. Typical TTL Load

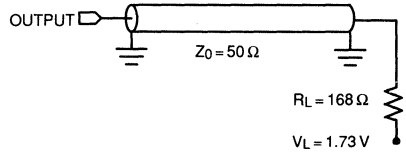


Figure 4B. Thevenin Equivalent Test Load

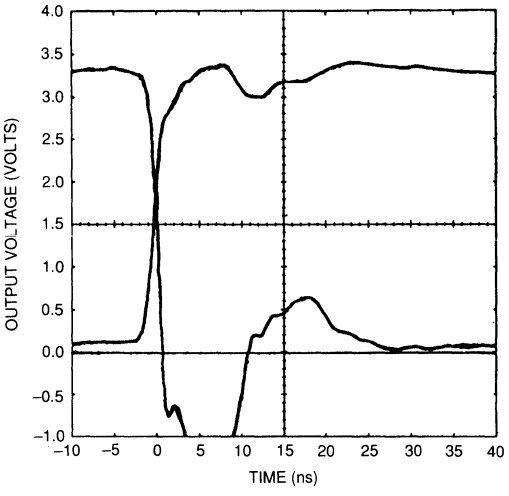


Figure 5. Output Waveforms with Thevenin Equivalent Test Load

The calculated performance of this setup would be that of a transmission line with a Z_0 of 50 Ω terminated to an R_L of 168 Ω at a V_L of 1.73 V. This would be ρ_L = (168 Ω – 50 Ω) / (168 Ω + 50 Ω) = 0.54. This means that the ΔV at the load would be 154% of the source ΔV. Using the example output buffer with V_{DD} = 5.0 V, the dc V_{OL} would be 0.14 V and the incident V_{OH}, using the 50 Ω from Z_0 in place of R_L, would be 2.67 V, giving a ΔV of 2.53 V. This means that for a low to high going signal at the source, at time t_{pd} later, the load would go to V_{OL} + ΔV + (ΔV × 0.54), or 4.01 V.

Figure 5 shows the actual measured waveform at the load end of a test fixture as described in Figure 4B. The t_{pd} of the signal path is measured using a TDR (time domain reflectometer) to be approximately 4 ns. Notice the reflection effects at each multiple of t_{pd} on both waveforms. The actual measured waveforms differ from predicted results due to inductance in the ground and V_{DD} path of the device being tested.

In a testing environment, the t_{pd} is subtracted from the time measured to give the actual output delay of the device (access time). Because of this, the distortions at the device output are of no concern. The ringing at the load end, however, can cause severe problems when trying to accurately test the speed of the parts. In the past, the access time has been measured from some mid-level voltage which is centered between the high and low output swing. This has the effect of giving the most noise margin to ringing output signals. However, this maximum noise margin does not guarantee that problems will not arise.

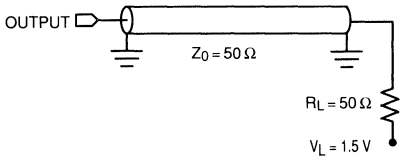


Figure 6. New High Frequency AC Test Load

NEW HIGH FREQUENCY AC TEST LOAD

In order to properly test and guarantee the ac performance of these new fast static RAMs, it is necessary to change the conditions for ac loading to a load that will allow accurate evaluation of the device parameters. Because of this, the specified ac load is now a transmission line terminated with a resistor of the characteristic impedance of the line to a load voltage (see Figure 6).

The calculated performance of this load in a normal test environment would be ρ_L = (50 Ω – 50 Ω) / (50 Ω + 50 Ω) = 0.0. This means that the ΔV at the load would be the same as the source ΔV with no signal reflection.

As seen in Figure 7, using a transmission line terminated to a load supply through a resistor equal to the characteristic impedance of the line produces a load waveform which matches the source signal. Additionally, under ideal conditions, no reflection effects are produced with this load. This results in the maximum possible noise margin for both test and system environments. In this test setup, power supply inductance causes some output noise which is seen at the load.

Figures 8 and 9 are derating curves for calculating the effects of varying C_O and R_L. These curves are based on typical device performance and are not intended to be absolute worst case specifications.

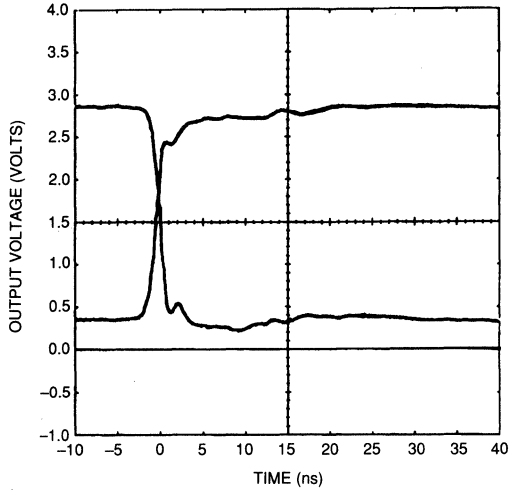


Figure 7. Output Waveforms with High Frequency AC Test Load

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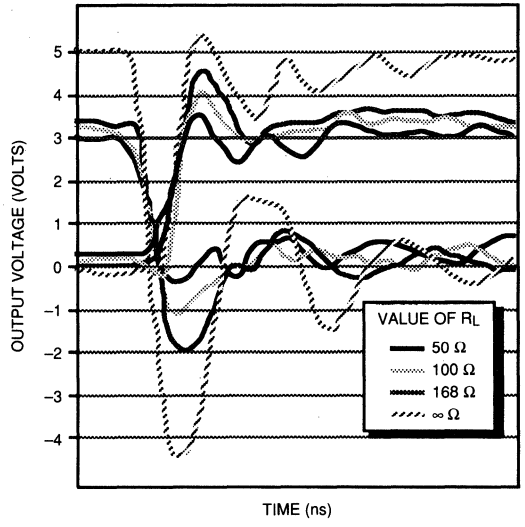

Figure 8. Output Voltage as a Function of R_L

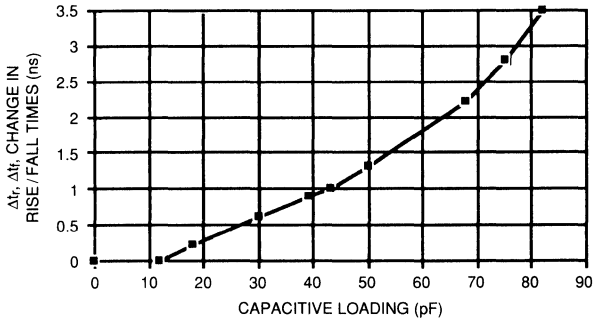

Figure 9. Change in Output Rise and Fall Times for Lumped Capacitive Loads

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Product Preview

QuickRAM™ II
Fast Static RAM Family

The QuickRAM Family of fast static RAMs is fabricated using Motorola's high-performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

The product family includes devices with four different densities: 294,912 bits, 262,144 bits, 73,728 bits, and 65,536 bits.

These devices meet JEDEC standards for functionality and pinout, and are available in plastic dual-in-line and plastic small-outline J-leaded packages.

- Single 5 V ±10% Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- Fast Access Times: 8, 10, 12, and 15 ns
- Equal Address and Chip Enable Access Times
- Output Enable ($\overline{G}$) Feature for Increased System Flexibility and to Eliminate Bus Contention Problems — on MCM6205/06, MCM6209, MCM6264/65, and MCM6290
- Low Power Operation: 150–180 mA Maximum AC
- Fully TTL Compatible — Three State Output
- Separate Data Input and Output on MCM6207 and MCM6287

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CONTENTS

DEVICE NUMERICAL INDEX (See Note)

Part Number	Access Times (ns)	Organization	Page
MCM6205C-12, -15	12, 15	32K x 9	14
MCM6206C-12, -15	12, 15	32K x 8	12
MCM6207C-10, -12	10, 12	256K x 1	8
MCM6208C-10, -12	10, 12	64K x 4	10
MCM6209C-10, -12	10, 12	64K x 4 OE	10
MCM6264C-10, -12	10, 12	8K x 8	13
MCM6265C-10, -12	10, 12	8K x 9	15
MCM6287C-8, -10	8, 10	64K x 1	9
MCM6288C-8, -10	8, 10	16K x 4	11
MCM6290C-8, -10	8, 10	16K x 4 OE	11

NOTE: Device Specifications for the faster access times are included to assist future system designs. Contact a Motorola Sales Representative for scheduled availability.

256K

256K x 1
MCM6207C-10, -12

64K x 4
MCM6208C-10, -12

64K x 4 with OE
MCM6209C-10, -12

32K x 8
MCM6206C-12, -15

32K x 9
MCM6205C-12, -15

64K

64K x 1
MCM6287C-8, -10

16K x 4
MCM6288C-8, -10

16K x 4 with OE
MCM6290C-8, -10

8K x 8
MCM6264C-10, -12

8K x 9
MCM6265C-10, -12

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage Relative to V_{SS}	V_{CC}	– 0.5 to +7	V
Voltage on Any Pin, Except V_{CC}, Relative to V_{SS}	V_{in}, V_{out}	– 0.5 to V_{CC} +0.5	V
Output Current (per I/O)	I_{out}	±30	mA
Power Dissipation	P_D	1	W
Temperature Under Bias	T_{bias}	– 10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature-Plastic	T_{stg}	– 55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the OPERATING CONDITIONS. Exposure to voltages higher than the operating voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

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DC OPERATING CONDITIONS AND CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Parameter	Conditions	Symbol	Min	Max	Unit
Supply Voltage	Operating Voltage Range	V_{CC}	4.5	5.5	V
Input High Voltage		V_{IH}	2.2	V_{CC}+0.3*	V
Input Low Voltage		V_{IL}	–0.5**	0.8	V
Input Leakage Current	0 V ≤ V_{in} ≤ V_{CC}	$I_{lkg(I)}$	—	±1	µA
Output Leakage Current	Output(s) Disabled, 0 V ≤ V_{out} ≤ V_{CC}	$I_{lkg(O)}$	—	±1	µA
Output High Voltage	I_{OH} = –4 mA	V_{OH}	2.4	—	V
Output Low Voltage	I_{OL} = 8 mA	V_{OL}	—	0.4	V

**V_{IL} (min) = –0.5 V dc, V_{IL} (min) = –2 V ac (pulse width ≤ 20 ns)

*V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 20 ns)

POWER SUPPLY CURRENTS (AC Operating Conditions Unless Otherwise Noted)

Density	Config.	Device	Parameter	Symbol	-8	-10	-12	-15	Unit
64K	16K x 4	MCM6288C/90C	AC Active Supply Current (I_{out} = 0 mA, V_{CC} = Max, f = f_{max})	I_{CCA}	180	170	—	—	mA
	64K x 1	MCM6287C			170	160	—	—	
	8K x 8	MCM6264C			—	170	150	—	
	8K x 9	MCM6265C			—	170	150	—	
	All	All	AC Standby Current ($\overline{E}$ = V_{IH}, V_{CC} = Max, f = f_{max})	I_{SB1}	55	50	45	40	mA
	All	All	CMOS Standby Current (V_{CC} = Max, f = 0 MHz, $\overline{E} \geq V_{CC} - 0.2$ V* $V_{in} \leq V_{SS} + 0.2$ V, or $\geq V_{CC} - 0.2$ V)	I_{SB2}	20	20	20	20	mA
256K	64K x 4	MCM6208C/09C	AC Active Supply Current (I_{out} = 0 mA, V_{CC} = Max, f = f_{max})	I_{CCA}	—	175	165	—	mA
	256K x 1	MCM6207C			—	170	160	—	
	32K x 8	MCM6206C			—	—	175	165	
	32K x 9	MCM6205C			—	—	180	170	
	All	All	AC Standby Current ($\overline{E}$ = V_{IH}, V_{CC} = Max, f = f_{max})	I_{SB1}	—	60	55	50	mA
	All	All	CMOS Standby Current (V_{CC} = Max, f = 0 MHz, $\overline{E} \geq V_{CC} - 0.2$ V* $V_{in} \leq V_{SS} + 0.2$ V, or $\geq V_{CC} - 0.2$ V)	I_{SB2}	—	20	20	20	mA

*For devices with multiple chip enables of opposite polarity, $\overline{E1} \geq V_{CC} - 0.2$ V or $E2 \leq V_{SS} + 0.2$ V

CAPACITANCE (f = 1 MHz, dV = 3 V, T_A = 25°C, Periodically sampled rather than 100% tested)

Characteristic	Symbol	Max	Unit
Address and Data Input Capacitance	C_{in}		pF
MCM6287C (64K x 1), MCM6288C/90C (16K x 4)		6	
MCM6264C (8K x 8), MCM6265C (8K x 9)		6	
MCM6207C (256K x 1), MCM6208C/09C (64K x 4)		6	
MCM6205C (32K x 9), MCM6206C (32K x 8)		6	
Control Pin Input Capacitance ($\overline{E}$,* $\overline{G}$, $\overline{W}$)	C_{in}		pF
MCM6287C (64K x 1), MCM6288C/90C (16K x 4)		6	
MCM6264C (8K x 8), MCM6265C (8K x 9)		6	
MCM6207C (256K x 1), MCM6208C/09C (64K x 4)		6	
MCM6205C (32K x 9), MCM6206C (32K x 8)		8	
Output Capacitance	C_{out}		pF
MCM6287C (64K x 1), MCM6288C/90C (16K x 4)		7	
MCM6264C (8K x 8), MCM6265C (8K x 9)		7	
MCM6207C (256K x 1), MCM6208C/09C (64K x 4)		8	
MCM6205C (32K x 9), MCM6206C (32K x 8)		8	

*For devices with multiple chip enables, $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E}$.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3 V
Input Rise/Fall Time ..... 5 ns

Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... Figure 1A Unless Otherwise Noted

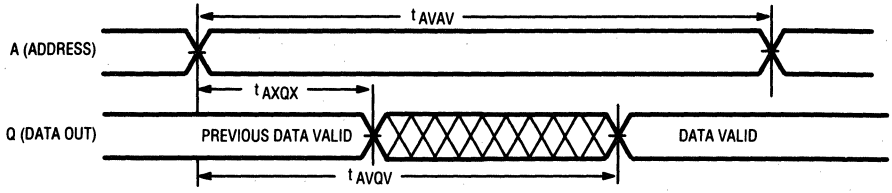
READ CYCLE (See Notes 1 and 2)

Product Family	Configuration	-8	-10	-12	-15	Density
MCM6288C and MCM6290C	16K x 4	√	√	EXISTING MOTOROLA PRODUCTS		64K
MCM6287C	64K x 1	√	√			
MCM6264C	8K x 8	FUTURE MOTOROLA PRODUCTS	√			
MCM6265C	8K x 9		√			
MCM6208C and MCM6209C	64K x 4		√			256K
MCM6207C	256K x 1		√			
MCM6206C	32K x 8			√	√	
MCM6205C	32K x 9			√	√	

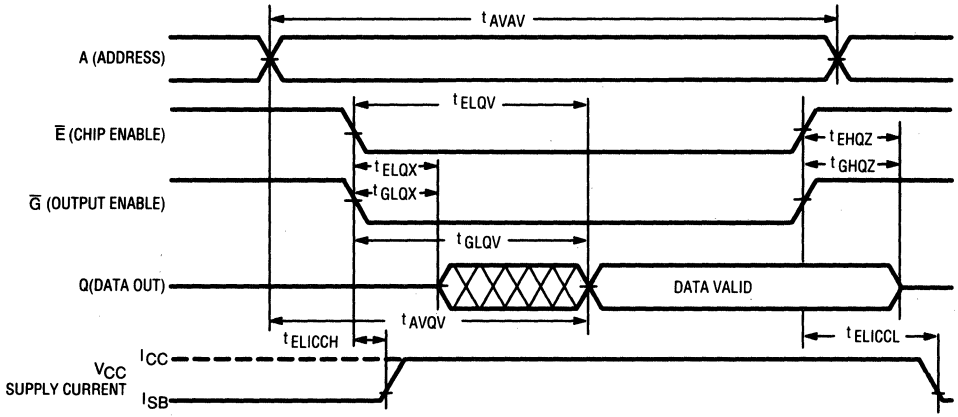
Parameter	Symbol Std	Symbol Alt	-8 Min	-8 Max	-10 Min	-10 Max	-12 Min	-12 Max	-15 Min	-15 Max	Unit	Notes
Read Cycle Time	t_{AVAV}	t_{RC}	8	—	10	—	12	—	15	—	ns	3
Address Access Time	t_{AVQV}	t_{AA}	—	8	—	10	—	12	—	15	ns	
Enable Access Time	t_{ELQV}	t_{ACS}	—	8	—	10	—	12	—	15	ns	4
Output Enable Access Time	t_{GLQV}	t_{OE}	—	4	—	5	—	6	—	8	ns	
Output Hold from Address Change	t_{AXQX}	t_{OH}	4	—	4	—	4	—	4	—	ns	
Enable Low to Output Active	t_{ELQX}	t_{CLZ}	4	—	4	—	4	—	4	—	ns	5,6,7
Output Enable Low to Output Active	t_{GLQX}	t_{OLZ}	0	—	0	—	0	—	0	—	ns	5,6,7
Enable High to Output High-Z	t_{EHQZ}	t_{CHZ}	0	4	0	5	0	6	0	8	ns	5,6,7
Output Enable High to Output High-Z	t_{GHQZ}	t_{OHZ}	0	4	0	5	0	6	0	7	ns	5,6,7
Power Up Time	t_{ELICCH}	t_{PU}	0	—	0	—	0	—	0	—	ns	
Power Down Time	t_{EHICCL}	t_{PD}	—	8	—	10	—	12	—	15	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. For devices with multiple chip enables, $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E}$.
3. All timings are referenced from the last valid address to the first transitioning address.
4. Addresses valid prior to or coincident with $\overline{E}$ going low.
5. At any given voltage and temperature, t_{EHQZ} max < t_{ELQX} min, and t_{GHQZ} max < t_{GLQX} min, both for a given device and from device to device.
6. Transition is measured 500 mV from steady-state voltage with load of Figure 1B.
7. This parameter is sampled and not 100% tested.
8. Device is continuously selected. $\overline{E} \leq V_{IL}$ and $\overline{G} \leq V_{IL}$.

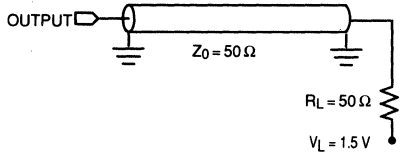
READ CYCLE 1 (See Note 8)



READ CYCLE 2 (See Notes 2 and 4)



AC TEST LOADS



See Output Load Conditions, page 18.

Figure 1A

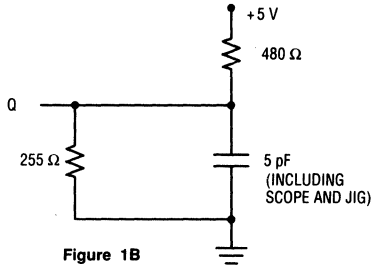
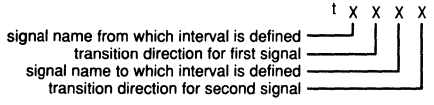


Figure 1B

TIMING PARAMETER ABBREVIATIONS



The transition definitions used in this data sheet are:
- H = transition to high
- L = transition to low
- V = transition to valid
- X = transition to invalid or don't care
- Z = transition to off (high impedance)

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device output will be valid no later than that time.

WRITE CYCLES

Product Family	Configuration	-8	-10	-12	-15	Density
MCM6288C and MCM6290C	16K x 4	√	√	EXISTING MOTOROLA PRODUCTS		64K
MCM6287C	64K x 1	√	√			
MCM6264C	8K x 8	FUTURE MOTOROLA PRODUCTS	√	√		
MCM6265C	8K x 9		√	√		
MCM6208C and MCM6209C	64K x 4		√	√		256K
MCM6207C	256K x 1		√	√		
MCM6206C	32K x 8			√	√	
MCM6205C	32K x 9			√	√	

WRITE CYCLE 1 ($\overline{W}$ Controlled) (See Notes 1, 2, and 3)

Parameter	Symbol		-8		-10		-12		-15		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	8	—	10	—	12	—	15	—	ns	4
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	8	—	9	—	10	—	12	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	t_{WP}	8	—	9	—	10	—	12	—	ns	
Write Pulse Width, $\overline{G}$ High (Output Enable devices)	t_{WLWH}, t_{WLEH}	t_{WP}	6	—	7	—	8	—	10	—	ns	5
Data Valid to End of Write	t_{DVWH}	t_{DW}	4	—	5	—	6	—	7	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	—	0	—	0	—	0	—	ns	
Write Low to Output High-Z	t_{WLQZ}	t_{WZ}	0	4	0	5	0	6	0	7	ns	6,7,8
Write High to Output Active	t_{WHQX}	t_{OW}	4	—	4	—	4	—	4	—	ns	6,7,8
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	0	—	0	—	ns	

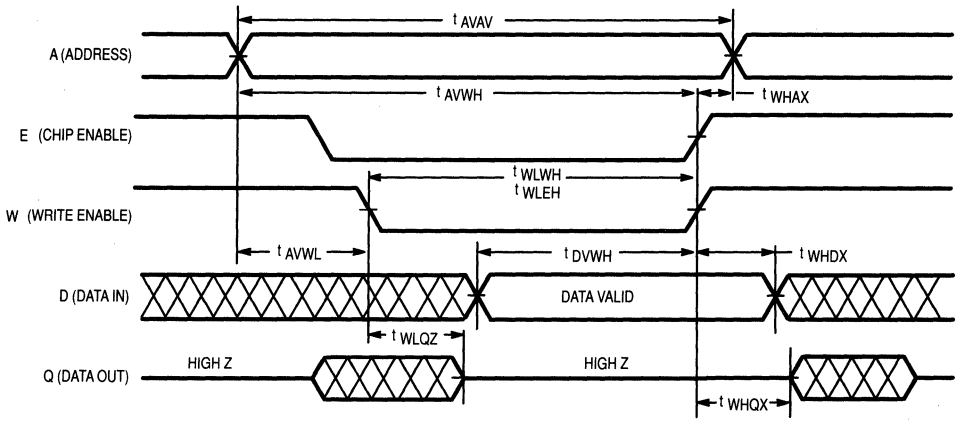
WRITE CYCLE 2 ($\overline{E}$ Controlled) (See Notes 1, 2, and 3)

Parameter	Symbol		-8		-10		-12		-15		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	8	—	10	—	12	—	15	—	ns	4
Address Setup Time	t_{AVEL}	t_{AS}	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	8	—	9	—	10	—	12	—	ns	
Enable to End of Write	t_{ELEH}, t_{ELWH}	t_{CW}	6	—	7	—	8	—	10	—	ns	9,10
Data Valid to End of Write	t_{DVEH}	t_{DW}	4	—	5	—	6	—	7	—	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	—	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	—	0	—	0	—	0	—	ns	

NOTES:

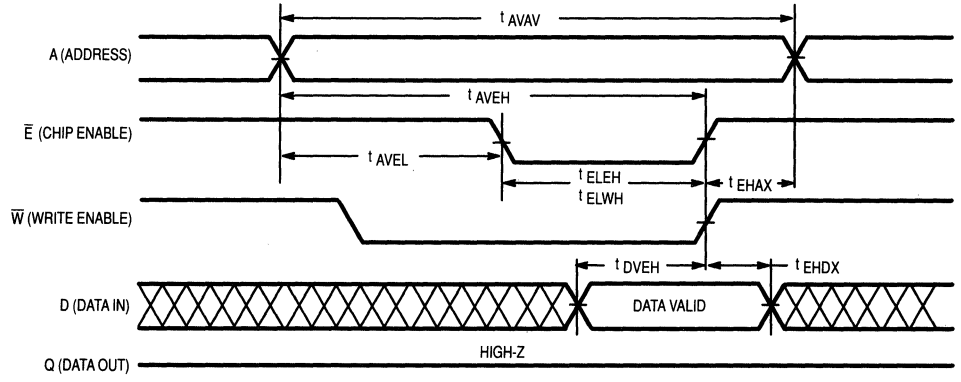
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. For devices with multiple chip enables, $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E}$.
3. For Output Enable devices, if $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
4. All timings are referenced from the last valid address to the first transitioning address.
5. For Output Enable devices, if $\overline{G} \geq V_{IH}$, the output will remain in a high impedance state.
6. At any given voltage and temperature, t_{WLQG} max < t_{WHQX} min, both for a given device and from device to device.
7. Transition is measured 500 mV from steady-state voltage with load of Figure 1B.
8. This parameter is sampled and not 100% tested.
9. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
10. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance state.

WRITE CYCLE 1 (See Note 2)



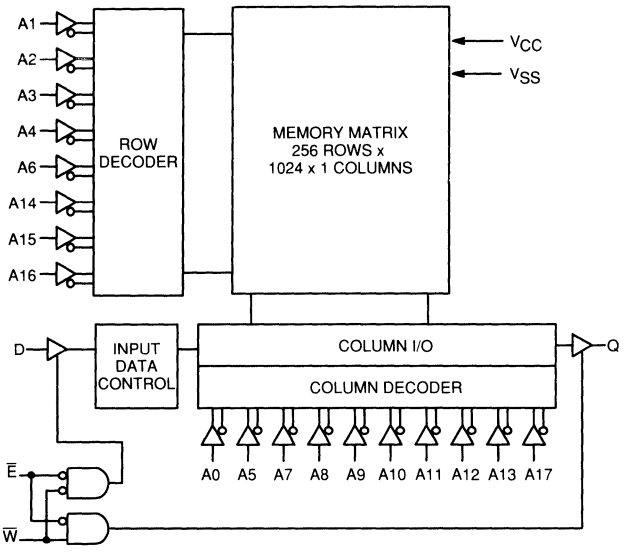
7

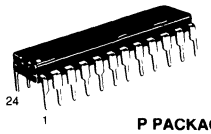
WRITE CYCLE 2 (See Note 2)



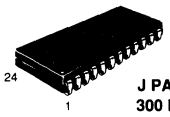
256K x 1 Bit Fast Static RAM

MCM6207C



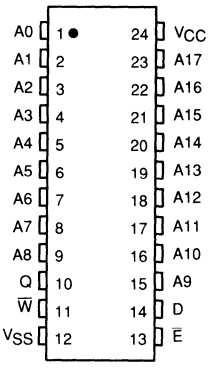


P PACKAGE
300 MIL PLASTIC
CASE 724A



J PACKAGE
300 MIL SOJ
CASE 810A

PIN ASSIGNMENT



PIN NAMES	
A0-A17 ..... Address Input	Q ..... Data Output
$\overline{E}$ ..... Chip Enable	V_{CC} ..... +5 V Power Supply
$\overline{W}$ ..... Write Enable	V_{SS} ..... Ground
D ..... Data Input	

MCM6207C TRUTH TABLE (X = don't care)

$\overline{E}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	Not Selected	I_{SB1}, I_{SB2}	High-Z	—
L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	L	Write	I_{CCA}	High-Z	Write Cycle

ORDERING INFORMATION (Order by Full Part Number)

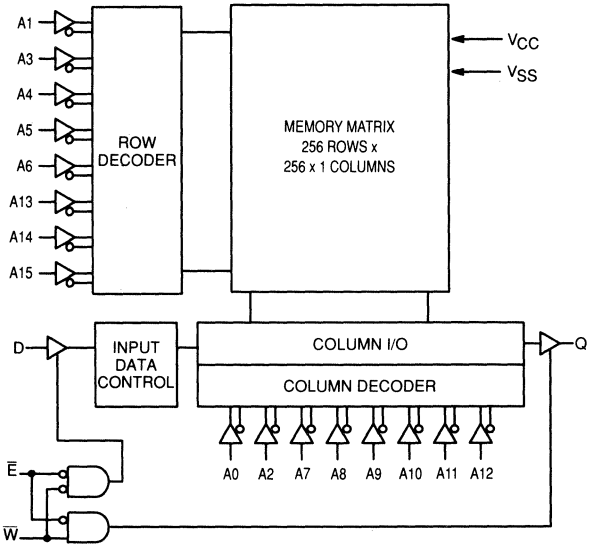
MCM 6207 C X XX XX

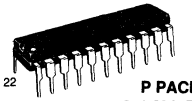
- MCM — Motorola Memory Prefix
- 6207 — Part Number
- C — Revision
- X — Package (P = 300 mil Plastic DIP, J = 300 mil SOJ)
- XX — Speed (12 = 12 ns)
- XX — Shipping Method (R2 = Tape & Reel, Blank = Rails)

Full Part Numbers—MCM6207CP12 MCM6207CJ12 MCM6207CJ12R2

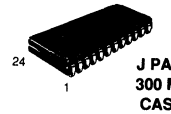
64K x 1 Bit Fast Static RAM

MCM6287C



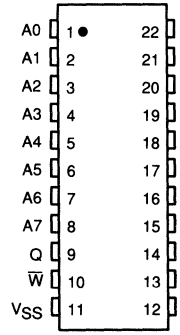


P PACKAGE
300 MIL PLASTIC
CASE 736A

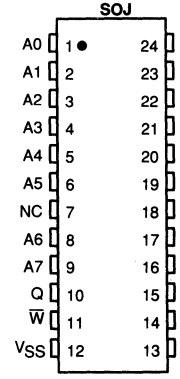


J PACKAGE
300 MIL SOJ
CASE 810A

DUAL-IN-LINE



SOJ



PIN NAMES			
A0-A15	Address Input	Q	Data Output
$\overline{E}$	Chip Enable	V_{CC}	+5 V Power Supply
$\overline{W}$	Write Enable	V_{SS}	Ground
D	Data Input	NC	No Connection

MCM6287C TRUTH TABLE (X = don't care)

$\overline{E}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	Not Selected	I_{SB1}, I_{SB2}	High-Z	—
L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	L	Write	I_{CCA}	High-Z	Write Cycle

ORDERING INFORMATION (Order by Full Part Number)

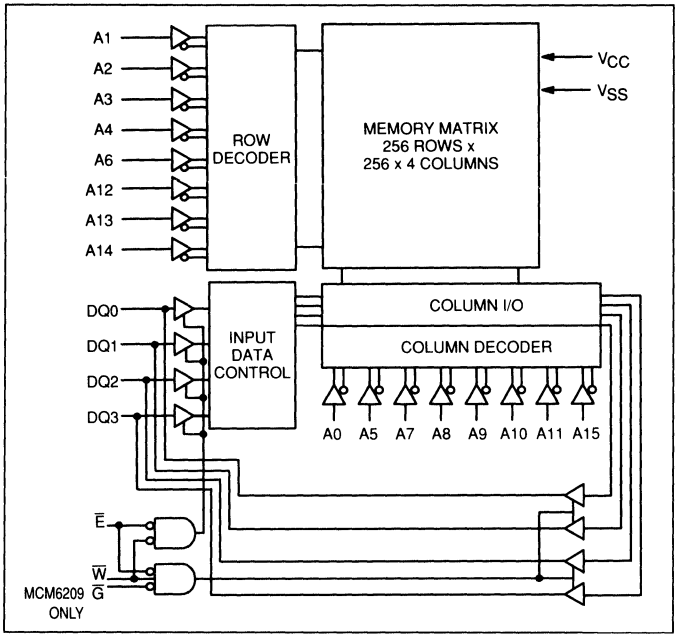
MCM 6287 C X XX XX

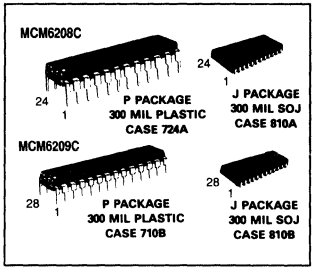
- MCM — Motorola Memory Prefix
- 6287 — Part Number
- C — Revision
- X — Package (P = 300 mil Plastic DIP, J = 300 mil SOJ)
- XX — Speed (10 = 10 ns)
- XX — Shipping Method (R2 = Tape & Reel, Blank = Rails)

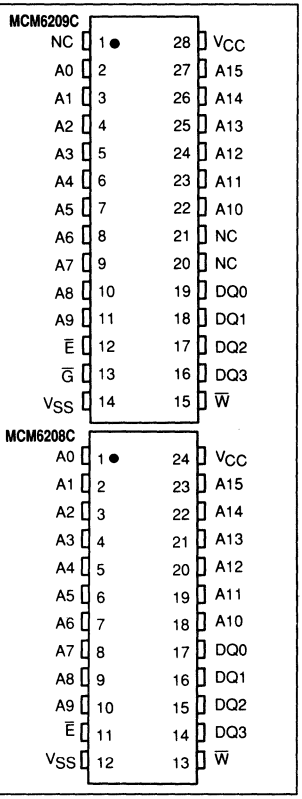
Full Part Numbers—MCM6287CP10 MCM6287CJ10 MCM6287CJ10R2

64K x 4 Bit Fast Static RAMs

MCM6208C
MCM6209C







PIN NAMES			
A0-A15	Address Input	$\overline{E}$	Chip Enable
DQ0–DQ3	Data Input/Output	NC	No Connection
$\overline{W}$	Write Enable	V_{CC}	+5 V Power Supply
$\overline{G}$ (MCM6209C)	Output Enable	V_{SS}	Ground

MCM6208C TRUTH TABLE (X = don't care)

$\overline{E}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	Not Selected	I_{SB1}, I_{SB2}	High-Z	—
L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	L	Write	I_{CCA}	High-Z	Write Cycle

MCM6209C TRUTH TABLE (X = don't care)

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	Not Selected	I_{SB1}, I_{SB2}	High-Z	—
L	H	H	Output Disabled	I_{CCA}	High-Z	—
L	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	X	L	Write	I_{CCA}	High-Z	Write Cycle

ORDERING INFORMATION (Order by Full Part Number)

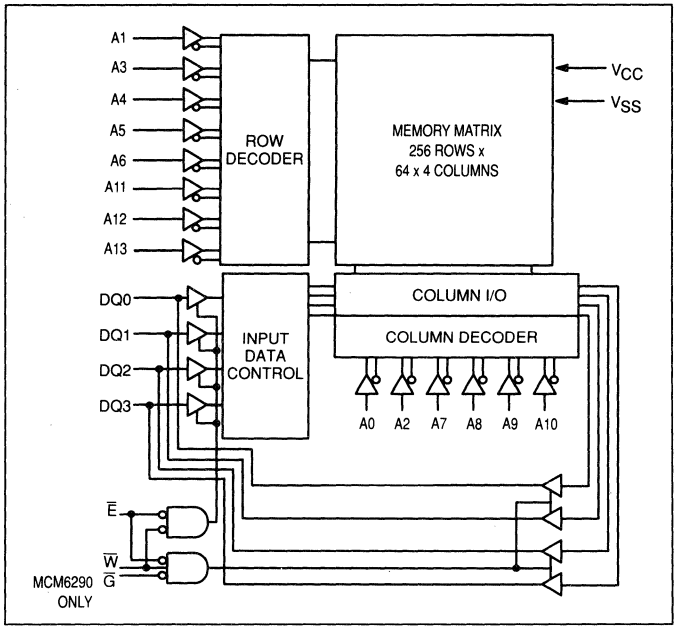
MCM 62XX C X XX XX

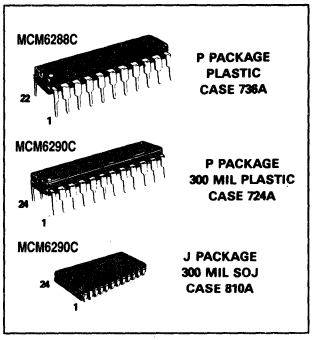
- MCM — Motorola Memory Prefix
- 62XX — Part Number
- C — Revision
- X — Package (P = 300 mil Plastic DIP, J = 300 mil SOJ)
- XX — Speed (12 = 12 ns)
- XX — Shipping Method (R2 = Tape & Reel, Blank = Rails)

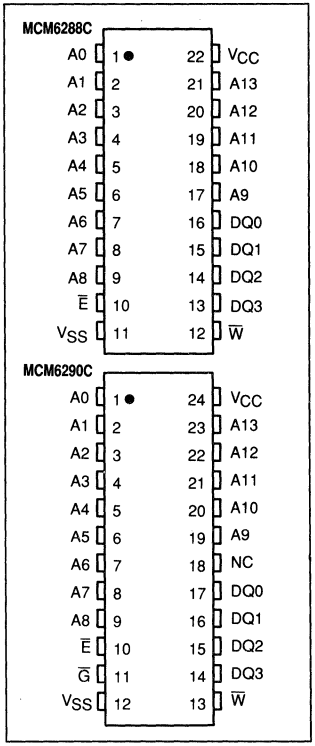
Full Part Numbers—MCM6208CP12 MCM6208CJ12 MCM6208CJ12R2
MCM6209CP12 MCM6209CJ12 MCM6209CJ12R2

16K x 4 Bit Fast Static RAMs

MCM6288C
MCM6290C







PIN NAMES			
A0-A13	Address Input	$\overline{E}$	Chip Enable
DQ0–DQ3	Data Input/Output	NC	No Connection
$\overline{W}$	Write Enable	V_{CC}	+5 V Power Supply
$\overline{G}$ (MCM6290C)	Output Enable	V_{SS}	Ground

MCM6288C TRUTH TABLE (X = don't care)

$\overline{E}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	Not Selected	I_{SB1}, I_{SB2}	High-Z	—
L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	L	Write	I_{CCA}	High-Z	Write Cycle

MCM6290C TRUTH TABLE (X = don't care)

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	Not Selected	I_{SB1}, I_{SB2}	High-Z	—
L	H	H	Output Disabled	I_{CCA}	High-Z	—
L	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	X	L	Write	I_{CCA}	High-Z	Write Cycle

ORDERING INFORMATION (Order by Full Part Number)

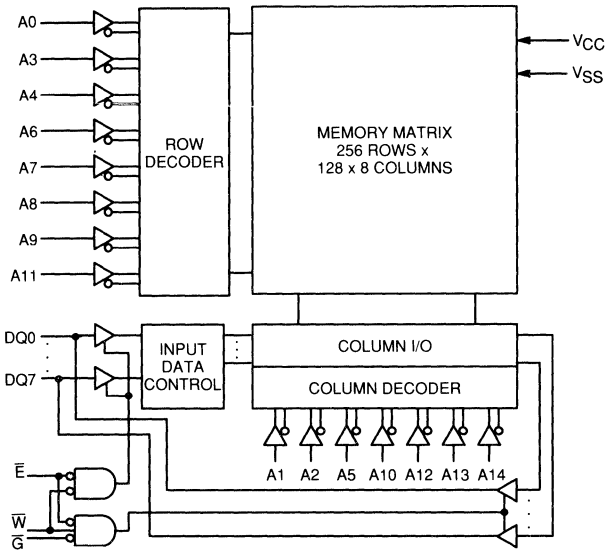
MCM 62XX C X XX XX

- MCM — Motorola Memory Prefix
- 62XX — Part Number
- C — Revision
- X — Package (P = 300 mil Plastic DIP, J = 300 mil SOJ)
- XX — Speed (10 = 10 ns)
- XX — Shipping Method (R2 = Tape & Reel, Blank = Rails)

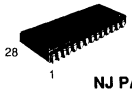
Full Part Numbers—MCM6288CP10 MCM6290CP10 MCM6290CJ10 MCM6290CJ10R2

32K x 8 Bit Fast Static RAM

MCM6206C

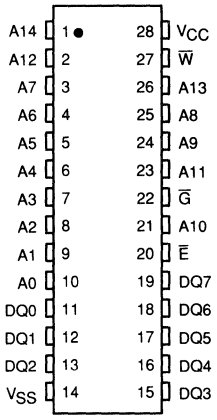


NP PACKAGE
300 MIL PLASTIC
CASE 710B



NJ PACKAGE
300 MIL SOJ
CASE 810B

PIN ASSIGNMENT



PIN NAMES

A0-A14 ..... Address Input	$\overline{E}$ ..... Chip Enable
DQ0–DQ7 ..... Data Input/Output	V_{CC} ..... +5 V Power Supply
$\overline{W}$ ..... Write Enable	V_{SS} ..... Ground
$\overline{G}$ ..... Output Enable	

MCM6206C TRUTH TABLE (X = don't care)

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	Not Selected	I_{SB1}, I_{SB2}	High-Z	—
L	H	H	Output Disabled	I_{CCA}	High-Z	—
L	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	X	L	Write	I_{CCA}	High-Z	Write Cycle

ORDERING INFORMATION (Order by Full Part Number)

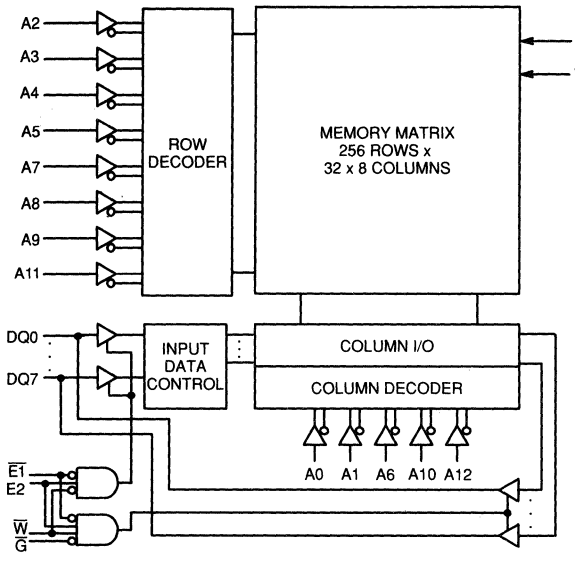
MCM 6206 C X XX XX

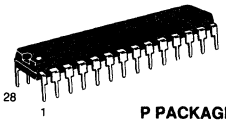
- MCM — Motorola Memory Prefix
- 6206 — Part Number
- C — Revision
- X — Package (NP = 300 mil Plastic DIP, NJ = 300 mil SOJ)
- XX — Speed (15 = 15 ns)
- XX — Shipping Method (R2 = Tape & Reel, Blank = Rails)

Full Part Numbers—MCM6206CNP15 MCM6206CNJ15 MCM6206CNJ15R2

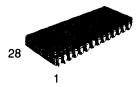
8K x 8 Bit Fast Static RAM

MCM6264C



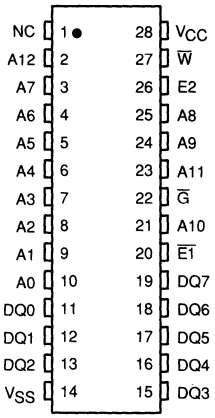


P PACKAGE
300 MIL PLASTIC
CASE 710B



NJ PACKAGE
300 MIL SOJ
CASE 810B

PIN ASSIGNMENT



PIN NAMES	
A0-A12 ..... Address Input	$\overline{E1}$, E2 ..... Chip Enable
DQ0–DQ7 ..... Data Input/Output	NC ..... No Connection
$\overline{W}$ ..... Write Enable	V_{CC} ..... +5 V Power Supply
$\overline{G}$ ..... Output Enable	V_{SS} ..... Ground

MCM6264C TRUTH TABLE (X = don't care)

$\overline{E1}$	E2	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	X	Not Selected	I_{SB1}, I_{SB2}	High-Z	—
X	L	X	X	Not Selected	I_{SB1}, I_{SB2}	High-Z	—
L	H	H	H	Output Disabled	I_{CCA}	High-Z	—
L	H	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	H	X	L	Write	I_{CCA}	High-Z	Write Cycle

ORDERING INFORMATION (Order by Full Part Number)

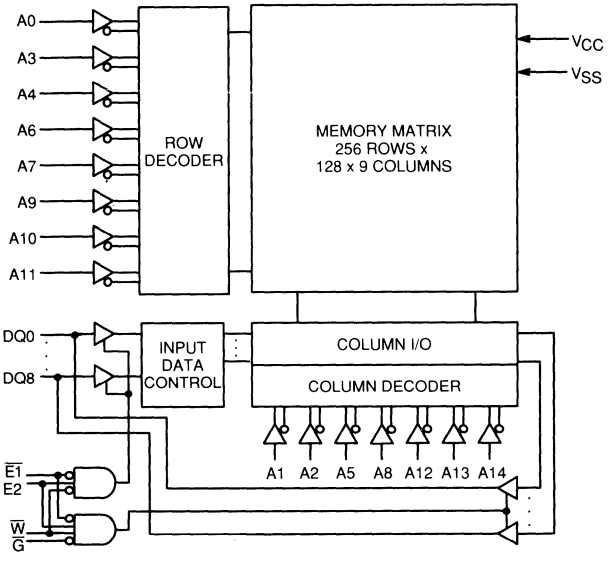
MCM 6264 C X XX XX

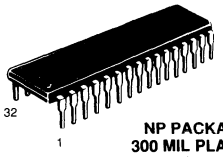
- MCM — Motorola Memory Prefix
- 6264 — Part Number
- C — Revision
- X — Package (P = 300 mil Plastic DIP, NJ = 300 mil SOJ)
- XX — Speed (12 = 12 ns)
- XX — Shipping Method (R2 = Tape & Reel, Blank = Rails)

Full Part Numbers—MCM6264CP12 MCM6264CNJ12 MCM6264CNJ12R2

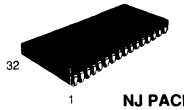
32K x 9 Bit Fast Static RAM

MCM6205C



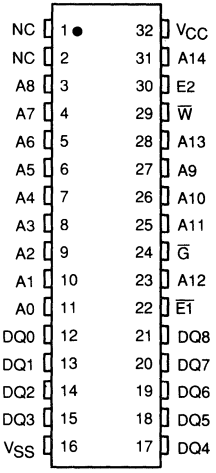


NP PACKAGE
300 MIL PLASTIC
CASE 853



NJ PACKAGE
300 MIL SOJ
CASE 857

PIN ASSIGNMENT



PIN NAMES

A0-A14 ..... Address Input	$\overline{E1}$, E2 ..... Chip Enable
DQ0–DQ8 ..... Data Input/Output	NC ..... No Connection
$\overline{W}$ ..... Write Enable	V_{CC} ..... +5 V Power Supply
$\overline{G}$ ..... Output Enable	V_{SS} ..... Ground

MCM6205C TRUTH TABLE (X = don't care)

$\overline{E1}$	E2	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	X	Not Selected	I_{SB1}, I_{SB2}	High-Z	—
X	L	X	X	Not Selected	I_{SB1}, I_{SB2}	High-Z	—
L	H	H	H	Output Disabled	I_{CCA}	High-Z	—
L	H	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	H	X	L	Write	I_{CCA}	High-Z	Write Cycle

ORDERING INFORMATION (Order by Full Part Number)

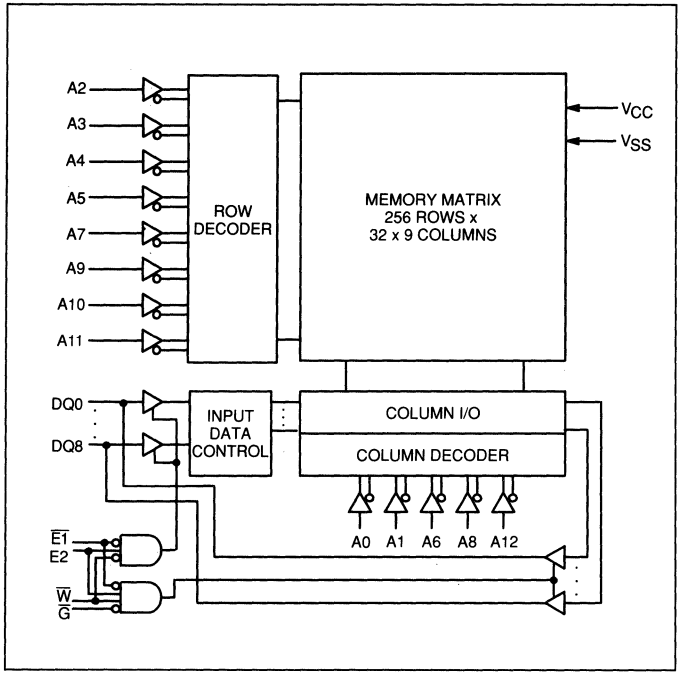
MCM 6205 C X XX XX

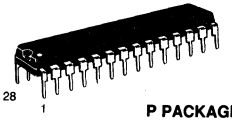
- MCM — Motorola Memory Prefix
- 6205 — Part Number
- C — Revision
- X — Package (NP = 300 mil Plastic DIP, NJ = 300 mil SOJ)
- XX — Speed (15 = 15 ns)
- XX — Shipping Method (R2 = Tape & Reel, Blank = Rails)

Full Part Numbers—MCM6205CNP15 MCM6205CNJ15 MCM6205CNJ15R2

8K x 9 Bit Fast Static RAM

MCM6265C

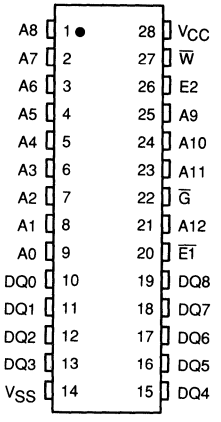




P PACKAGE
300 MIL PLASTIC
CASE 710B

NJ PACKAGE
300 MIL SOJ
CASE 810B

PIN ASSIGNMENT



PIN NAMES	
A0-A12 ..... Address Input	$\overline{E1}$, E2 ..... Chip Enable
DQ0–DQ8 ..... Data Input/Output	V_{CC} ..... +5 V Power Supply
$\overline{W}$ ..... Write Enable	V_{SS} ..... Ground
$\overline{G}$ ..... Output Enable	

MCM6265C TRUTH TABLE (X = don't care)

$\overline{E1}$	E2	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	X	Not Selected	I_{SB1}, I_{SB2}	High-Z	—
X	L	X	X	Not Selected	I_{SB1}, I_{SB2}	High-Z	—
L	H	H	H	Output Disabled	I_{CCA}	High-Z	—
L	H	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	H	X	L	Write	I_{CCA}	High-Z	Write Cycle

ORDERING INFORMATION (Order by Full Part Number)

MCM 6265 C X XX XX

- MCM — Motorola Memory Prefix
- 6265 — Part Number
- C — Revision
- X — Package (P = 300 mil Plastic DIP, NJ = 300 mil SOJ)
- XX — Speed (12 = 12 ns)
- XX — Shipping Method (R2 = Tape & Reel, Blank = Rails)

Full Part Numbers—MCM6265CP12 MCM6265CNJ12 MCM6265CNJ12R2

OUTPUT LOAD CONDITIONS

INTRODUCTION

This review describes the ac loading used for testing this family of parts. Component test engineers should pay careful attention to the test conditions and derating curves for deviations from the specified load. This information is also applicable for system engineers calculating required device speed for a given environment. This information will help the user make the appropriate choice of device performance for their needs.

As device access times decrease, so do output transition times. With faster rise and fall times come additional problems associated with output and signal path impedances. In any system running at frequencies where the propagation delay of a signal path (t_{pd}) is greater than 1/2 of the total signal transition time, transmission line effects will be seen on the signal. This results in overshoot and undershoot at the load end of a conductor, which can cause problems in testing, or in actual use of the device. This discussion gives a brief overview of the factors contributing to these effects, and the measures that can be used to predict or eliminate them. For a detailed discussion of both PC board layout considerations and applicable transmission line theory, consult the *MECL System Design Handbook*, publication HB205R1, Motorola, Inc., 1983.

DEFINITION OF TERMS

t_{pd}	Propagation delay in seconds
L_0	Inductance in henries/meter
C_0	Capacitance in farads/meter
R_L	Load resistance in ohms
$R_{DS(on)}$	Resistance from drain to source of a FET device when on
R_O	Output resistance in ohms. For CMOS devices, this is the $R_{DS(on)}$ resistance of the output devices.
R_{OH}	Output resistance for a high, or "1", signal from the device
R_{OL}	Output resistance for a low, or "0", signal from the device
ρ_L	Reflection coefficient of the load end of a signal
ρ_S	Reflection coefficient of the source end of a signal, the device output
V_L	Termination voltage of the load resistor in a transmission line termination network

TRANSMISSION LINE OVERVIEW

What is a transmission line and how does it affect output waveforms? In simple terms, a transmission line is a signal path that exhibits a characteristic impedance. The type of lines discussed in this paper are primarily microstrip (Figure 2A) and stripline signal paths (Figure 2B) found in most PC boards today. The inductance and capacitance of these lines are a function of the line thickness and width in combination with the dielectric properties of the PC board material and the distance of the line from the ground plane. The impedance of the line is determined by these characteristics and the additional distributed capacitance from other devices on the line.

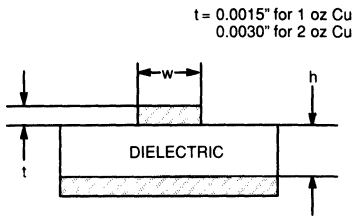


Figure 2A. Microstrip Signal Path

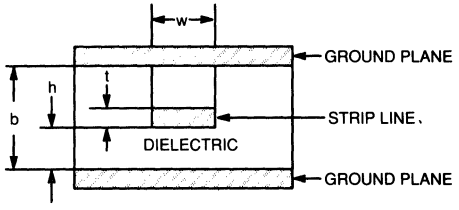


Figure 2B. Stripline Signal Path

The characteristic impedance of a microstrip or stripline path is given by the formula $Z_0 = \sqrt{L_0 / C_0}$. The propagation delay of the path, t_{pd}, is $t_{pd} = \sqrt{L_0 C_0} \times \text{length} = Z_0 C_0 \times \text{length}$. For example, the propagation delay of a microstrip line on G10 epoxy/glass material is approximately 1.76 ns/ft, while the delay for a stripline is about 2.27 ns/ft.

The effect of a transmission line on a device output depends on the electrical length of the line. In all cases, a signal traveling down the line will be affected at the end of the line if it is not terminated with a resistor of the characteristic impedance of the line. The amount of effect is determined by the reflection coefficient of the load, ρ_L, where:

$$\rho_L = \left(\frac{R_L - Z_0}{R_L + Z_0}\right) \quad (1)$$

This reflection occurs at a time t_{pd} after a change at the source of the signal. A similar reflection occurs at $2t_{pd}$ after this new signal has returned from the load to the source, and is determined by the source reflection coefficient, ρ_S, where:

$$\rho_S = \left(\frac{R_O - Z_0}{R_O + Z_0}\right) \quad (2)$$

R_O is the output resistance of the device. In the case of an electrical line length with tpd less than 1/2 of the rise/fall time of the output signal, the transmission line effects are seen as a delay of the signal transition times. This is caused by the load reflection returning to the source during the actual signal transition and being included in the duration of the signal. For the case of an electrical length with t_{pd} greater than 1/2 of the rise/fall time of the output signal, the reflection effects may be seen

directly. In severe cases, signal overshoot or undershoot can cause an invalid level to be seen at the load end at $3t_{pd}$.

The formulas for determining reflection coefficients require knowledge of the output impedance of the device, the characteristic impedance of the signal path, and the termination resistance. The goal of termination is to guarantee that the output signal at the receiving end (load) has enough margin to keep reflection effects from causing a false level to be detected. In an ideal case, the termination resistance is equal to the characteristic impedance of the line, and therefore, no reflection is generated at the load. In that one case, the impedance mismatch at the source is of importance only for signal rise time, V_{OH} and V_{OL} considerations.

The effect of additional distributed capacitance on a transmission line is a reduction in impedance resulting in little change to t_{pd}. This additional capacitance does, however, change the signal transition times resulting in a longer rise and fall time.

OUTPUT BUFFERS

The schematic drawing for a typical CMOS TTL output buffer is shown in Figure 3A. Figure 3B shows the equivalent circuit as actually implemented in many devices. The actual values for R_{OH} and R_{OL} vary from design to design but the range of values is similar.

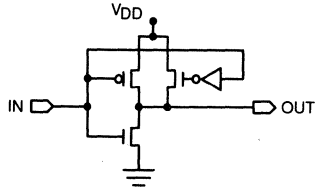


Figure 3A. Typical Output Buffer

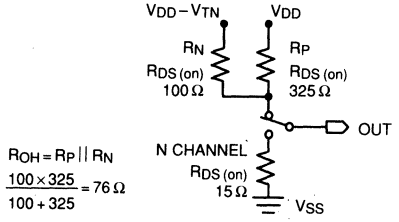


Figure 3B. Effective Circuit

As can be seen from Figure 3, the output impedance of a TTL output buffer is different for high and low output signals. This relation, along with the choice of V_{DD} level, termination resistance, and voltage determine the output high and low levels the part will produce in the system. In a dc condition with R_L = 50 Ω = and V_L = 1.5 V, the output voltages would be:

$$V_{OL} = V_{SS} + (V_L - V_{SS})\left(\frac{R_{OL}}{R_{OL} + R_L}\right)$$

$$V_{OL} = 0\ V + (1.5\ V - 0\ V)\left(\frac{15\ \Omega}{15\ \Omega + 50\ \Omega}\right)$$

$$V_{OL} = 0.35\ V \qquad (3)$$

$$V_{OH} = V_L + \left(V_{DD} - V_L - V_{TN}\frac{R_P}{R_P + R_N}\right)\left(\frac{R_L}{R_L + R_{OH}}\right)$$

$$V_{OH} = 1.5\ V + \left(4.4\ V - 1.5\ V - 1.2\ V\ \frac{325\ \Omega}{100\ \Omega + 325\ \Omega}\right)\left(\frac{50\ \Omega}{50\ \Omega + 76\ \Omega}\right)$$

$$V_{OH} = 2.33\ V \qquad (4)$$

TRADITIONAL TTL OUTPUT LOAD SPECIFICATIONS

The output loading typically specified in the industry until now is shown in Figure 4A. The load consists of a resistor network and capacitance. The values for the network were chosen to present a dc load of 8 mA during an output low condition ($V_{OL} \leq 0.4$ V) and –4 mA for an output high ($V_{OH} \geq 2.4$ V). A 5 V supply was chosen as the termination supply and a divider network was calculated to provide the specified currents. In addition, a lumped capacitive load of 30 pF was added to the output to represent input loading from other devices. In actual practice during testing, the load used is a Thevenin equivalent as shown in Figure 4B, with capacitance being provided by the 50 Ω transmission line connection to the test head and the test fixture capacitance.

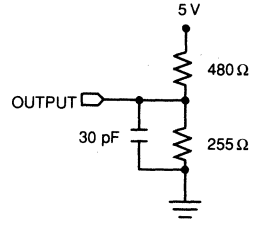


Figure 4A. Typical TTL Load

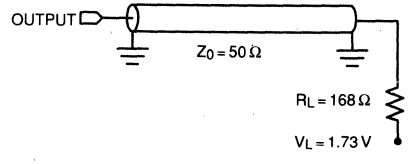


Figure 4B. Thevenin Equivalent Test Load

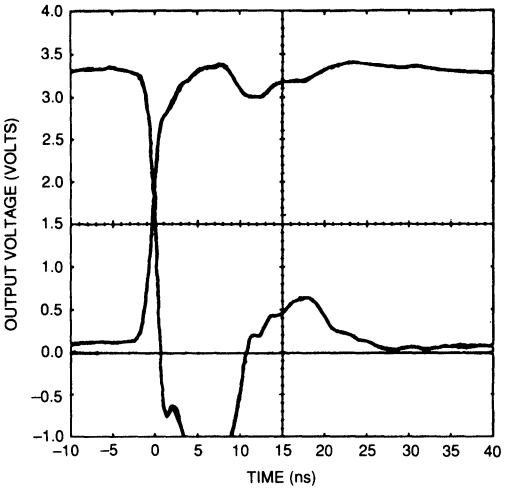


Figure 5. Output Waveforms with Thevenin Equivalent Test Load

The calculated performance of this setup would be that of a transmission line with a Z_0 of 50 Ω terminated to an R_L of 168 Ω at a V_L of 1.73 V. This would be ρ_L = (168 Ω − 50 Ω) / (168 Ω + 50 Ω) = 0.54. This means that the ΔV at the load would be 154% of the source ΔV. Using the example output buffer with V_{DD} = 5.0 V, the dc V_{OL} would be 0.14 V and the incident V_{OH}, using the 50 Ω from Z_0 in place of R_L, would be 2.67 V, giving a ΔV of 2.53 V. This means that for a low to high going signal at the source, at time t_{pd} later, the load would go to V_{OL} + ΔV + (ΔV × 0.54), or 4.01 V.

Figure 5 shows the actual measured waveform at the load end of a test fixture as described in Figure 4B. The t_{pd} of the signal path is measured using a TDR (time domain reflectometer) to be approximately 4 ns. Notice the reflection effects at each multiple of t_{pd} on both waveforms. The actual measured waveforms differ from predicted results due to inductance in the ground and V_{DD} path of the device being tested.

In a testing environment, the t_{pd} is subtracted from the time measured to give the actual output delay of the device (access time). Because of this, the distortions at the device output are of no concern. The ringing at the load end, however, can cause severe problems when trying to accurately test the speed of the parts. In the past, the access time has been measured from some mid-level voltage which is centered between the high and low output swing. This has the effect of giving the most noise margin to ringing output signals. However, this maximum noise margin does not guarantee that problems will not arise.

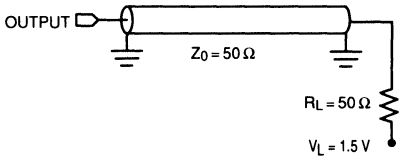


Figure 6. New High Frequency AC Test Load

NEW HIGH FREQUENCY AC TEST LOAD

In order to properly test and guarantee the ac performance of these new fast static RAMs, it is necessary to change the conditions for ac loading to a load that will allow accurate evaluation of the device parameters. Because of this, the specified ac load is now a transmission line terminated with a resistor of the characteristic impedance of the line to a load voltage (see Figure 6).

The calculated performance of this load in a normal test environment would be ρ_L = (50 Ω − 50 Ω) / (50 Ω + 50 Ω) = 0.0. This means that the ΔV at the load would be the same as the source ΔV with no signal reflection.

As seen in Figure 7, using a transmission line terminated to a load supply through a resistor equal to the characteristic impedance of the line produces a load waveform which matches the source signal. Additionally, under ideal conditions, no reflection effects are produced with this load. This results in the maximum possible noise margin for both test and system environments. In this test setup, power supply inductance causes some output noise which is seen at the load.

Figures 8 and 9 are derating curves for calculating the effects of varying C_O and R_L. These curves are based on typical device performance and are not intended to be absolute worst case specifications.

7

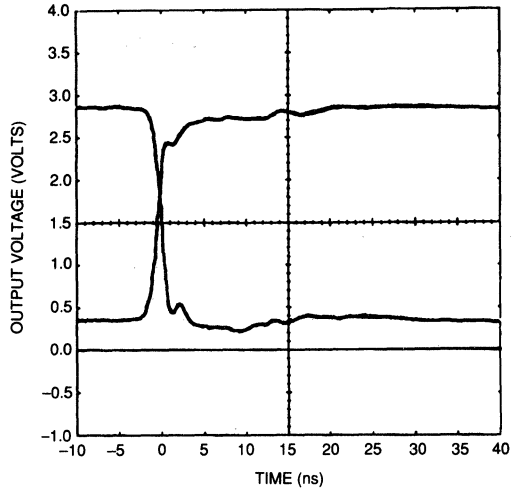


Figure 7. Output Waveforms with High Frequency AC Test Load

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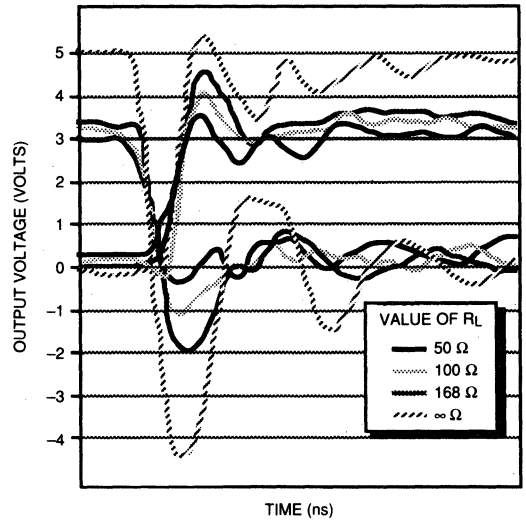


Figure 8. Output Voltage as a Function of R_L

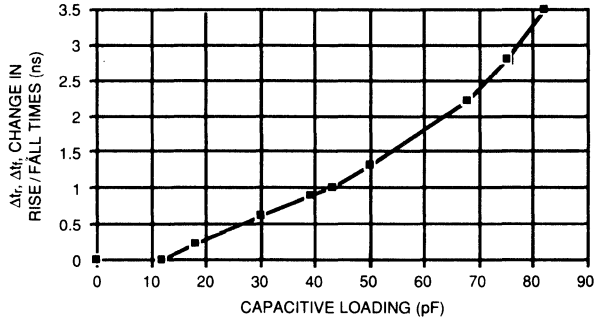


Figure 9. Change in Output Rise and Fall Times for Lumped Capacitive Loads

7

CMOS Fast Static RAM Modules

8

FAST STATIC RAM MODULES

Density	Organi-zation	Motorola Part Number	Pin Count	Packaging	Address/ Cycle Time (ns Max)	Operating Current (mA max)	Tech-nology
2M	64Kx32	MCM3264Z	64	ZIP	20/25/30	1200/1120/1040	HCMOS
	256Kx8	MCM8256Z	60	ZIP	20/25/30	1200/1120/1040	HCMOS
3M	2x64Kx24	MCM2464Z	58	ZIP	22/27	1680/1560	HCMOS

MCM2464

Product Preview

2 × 64K × 24 Bit Static Random Access Memory Module

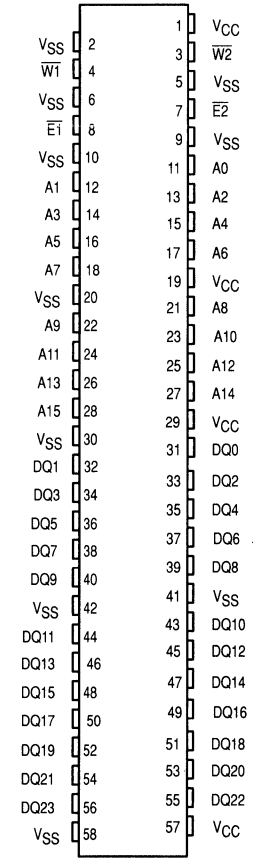
The MCM2464 is a 3M bit static random access memory module organized as two banks of 65,536 words each with 24 bits. The module is a 58 lead zig-zag in-line module consisting of twelve MCM6208 fast static RAMs packaged in 24 J-lead small outline package (SOJ) and mounted on a board along with twelve decoupling capacitors.

The MCM6208 is a high-performance CMOS fast static RAM organized as 65,536 words of 4 bits, fabricated using high performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

The MCM2464 is equipped with separate write enable ($\overline{W1}$ and $\overline{W2}$) and chip enable ($\overline{E1}$ and $\overline{E2}$) control inputs for each bank, allowing for greater system flexibility. The $\overline{Ex}$ input, when high, will force the outputs of bank x to high impedance.

- Single 5 V ± 8% Power Supply
- Fast Access Time: 22/27 ns
- Equal Address and Chip Enable Access Time
- Three-State Outputs
- Fully TTL Compatible
- Power Operation: 1680/1560 mA Maximum, Active AC
- High Board Density ZIP Module
- Bank Operation: Two 64K x 24 Bit Banks with Separate Chip Enables and Write Enables
- High Quality Multi-Layer FR4 PWB with Separate Internal Power and Ground Planes
- Custom Marking Available
- Incorporates Motorola's State-of-the-Art QuickRAM Fast Statics

PIN ASSIGNMENT
58 LEAD ZIG-ZAG IN-LINE MODULE
TOP VIEW



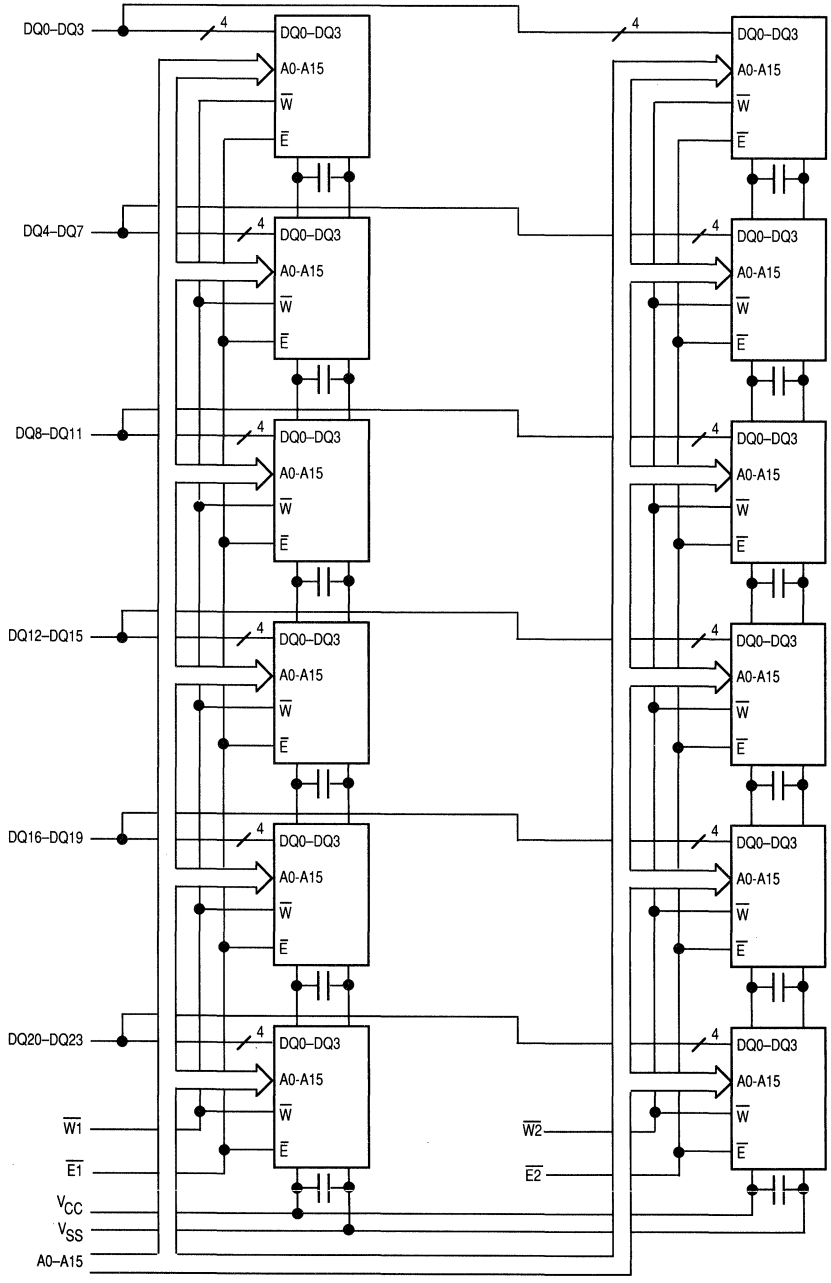
PIN NAMES	
A0–A15	Address Inputs
$\overline{W1}$–$\overline{W2}$	Bank Write Enable
$\overline{E1}$–$\overline{E2}$	Bank Enables
DQ0–DQ24	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground

All power supply and ground pins must be connected for proper operation of the device.

8

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

$\overline{Ex}$*	$\overline{Wx}$	Mode	V_{CC} Current	Output	Cycle
H	X	Not Selected	I_{SB1}, I_{SB2}	High-Z	—
L	H	Read Bank x	I_{CCA}	D_{out}	Read Cycle
L	L	Write	I_{CCA}	D_{in}	Write Cycle

*$\overline{Ex}$ = H implies $\overline{E1}$ = $\overline{E2}$ = H, $\overline{Ex}$ = L implies $\overline{E1}$ = L and $\overline{E2}$ = H, or $\overline{E1}$ = H and $\overline{E2}$ = L. In other words only one bank may be enabled at any time. Enabling both banks simultaneously during a read will cause bus contention on the output pins.

This devices on this module contain circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high impedence circuits.

These CMOS memory circuits have been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The module is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to 7.0	V
Output Power Supply Voltage	V_{CCQ}	– 0.5 to V_{CC}	V
Voltage Relative to V_{SS}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation (T_A = 70°C, V_{CC} = 5 V, t_{KHKH} = 20 ns)	P_D	13.2	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperatrue	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

8

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 8%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.6	5.0	5.4	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

*V_{IL} (min) = – 3.0 Vac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	—	± 8	µA
Output Leakage Current ($\overline{G}$, $\overline{Ex}$ = V_{IH}, V_{out} = 0 to V_{CCQ})	$I_{lkg(O)}$	—	—	± 8	µA
AC Supply Current ($\overline{G}$, $\overline{Ex}$ = V_{IL}, I_{out} = 0 mA, All Inputs = V_{IL} = 0.0 V and V_{IH} ≥ 3.0) MCM2464-22: t_{AVAV} ≥ 22 ns MCM2464-27: t_{AVAV} ≥ 27 ns	I_{CCA}	 — —	 840 780	 1680 1560	mA
Standby Current ($\overline{Ex}$ = V_{IH}, All Inputs = V_{IL} and V_{IH})	I_{SB1}	—	360	480	mA
CMOS Standby Current ($\overline{Ex}$ ≥ V_{CC} – 0.2 V, All Inputs ≥ V_{CC} – 0.2 V or ≤ 0.2 V)	I_{SB2}	—	240	360	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	—	V

NOTE: Good decoupling of the local power supply should always be used.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance — A0–A15	C_{in}	80	—	pF
Input Capacitance — $\overline{E1}$,–$\overline{E2}$, $\overline{W1}$–$\overline{W2}$	C_{in}	40	—	pF
Input/Output Capacitance (DQ0–DQ24)	$C_{I/O}$	20	—	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 8%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 5 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

READ CYCLE TIMING (See Notes 1 and 8)

Parameter	Symbol		MCM2464-22		MCM2464-27		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	22	—	27	—	ns	2
Address Access Time	t_{AVQV}	t_{AA}	—	22	—	27	ns	
Enable Access Time	t_{ELQV}	t_{ACS}	—	22	—	27	ns	
Output Hold from Address Change	t_{AXQX}	t_{OH}	5	—	6	—	ns	
Enable Low to Output Active	t_{ELQX}	t_{CLZ}	5	—	6	—	ns	3, 4, 5
Enable High to Output High-Z	t_{EHQZ}	t_{CHZ}	0	9	0	11	ns	3, 4, 5
Power Up Time	t_{ELICCH}	t_{PU}	0	—	0	—	ns	
Power Down Time	t_{EHICCL}	t_{PD}	—	22	—	27	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transitioning address.
3. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} min, both for a given device and from device to device.
4. Transition is measured + 500 mV from steady-state voltage with load of Figure 1B.
5. This parameter is sampled and not 100% tested.
6. Device is continuously selected $\overline{E}$ = V_{IL}.
7. Addresses valid prior to or coincident with $\overline{E}$ going low.
8. $\overline{E1}$–$\overline{E2}$ are represented by $\overline{E}$ in these timing specifications, only one of the $\overline{E}$xs may be asserted.

AC TEST LOADS

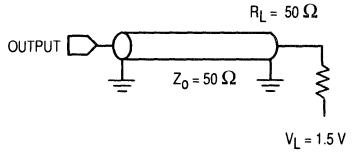


Figure 1A

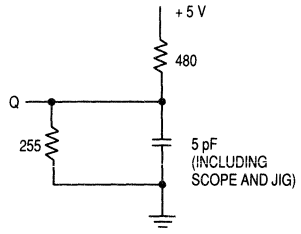
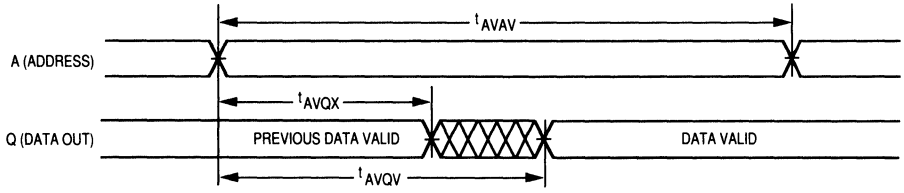


Figure 1B

TIMING LIMITS

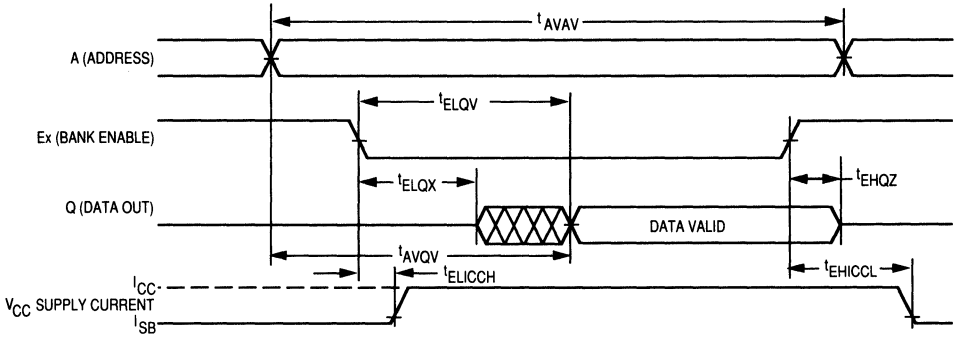
The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the module point of view. Thus, the access time is shown as a maximum since the module never provides data later than that time.

READ CYCLE 1 (See Note)



NOTE: Device is continuously selected ($\overline{E}$ = V_{IL}).

READ CYCLE 2 (See Note)



NOTE: Addresses valid prior to or coincident with $\overline{E}$ going low.

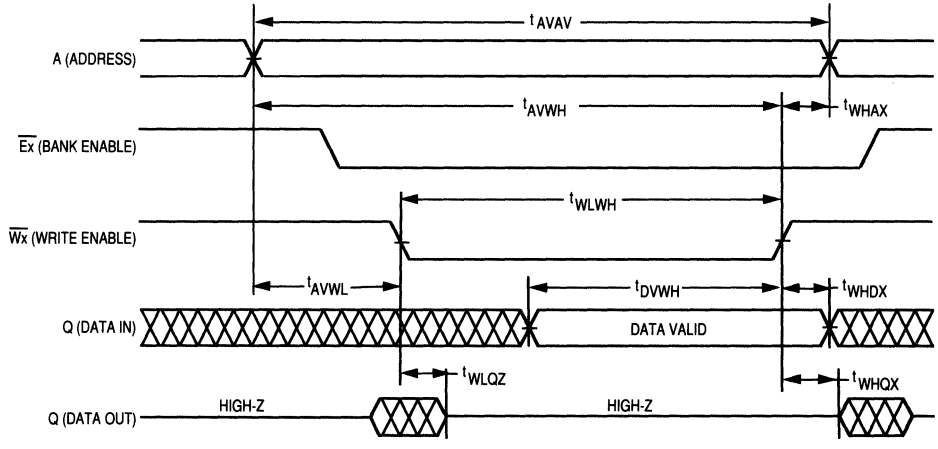
8

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 6)

Parameter	Symbol		MCM2464-22		MCM2464-27		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	22	—	27	—	ns	2
Address Setup Time	t_{AVWL}	t_{AS}	2	—	2	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	17	—	21	—	ns	
Write Pulse Width	t_{WLWH}	t_{WP}	17	—	21	—	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	9	—	11	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	—	0	—	ns	
Write Low to Data High-Z	t_{WLQZ}	t_{WZ}	0	8	0	11	ns	4, 5, 6
Write High to Output Active	t_{WHQX}	t_{OW}	6	—	6	—	ns	4, 5, 6
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. All write cycle timing is referenced from the last valid address to the first transitioning address.
3. Transition is measured + 500 mV from steady-state voltage with load of Figure 1B.
4. This parameter is sampled and not 100% tested.
5. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min both for a given device and from device to device.
6. $\overline{E1}$–$\overline{E2}$ are presented by $\overline{E}$ in these timing specifications, only one of the $\overline{Ex}$s may be asserted at any time.

WRITE CYCLE 1



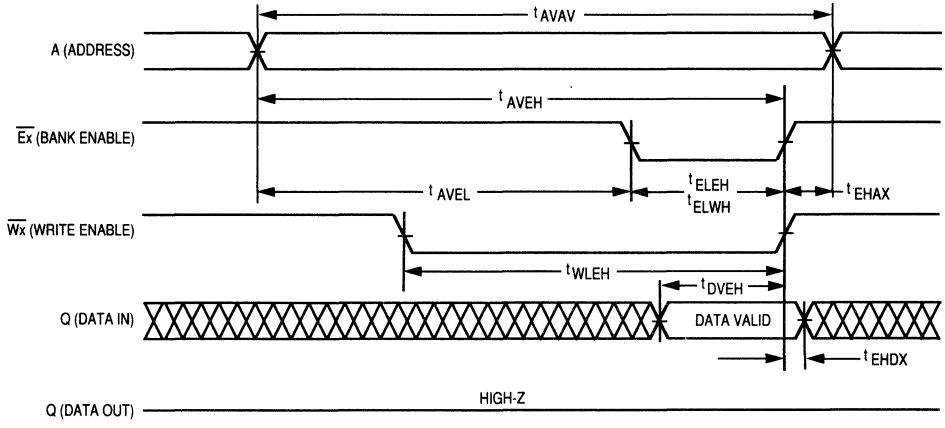
8

WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 5)

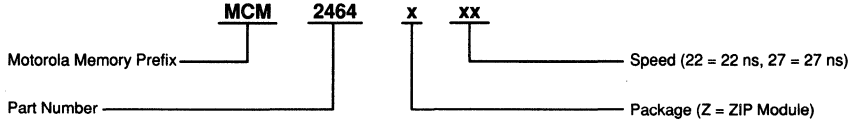
Parameter	Symbol		MCM2464-22		MCM2464-27		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	22	—	27	—	ns	2
Address Setup Time	t_{AVEL}	t_{AS}	2	—	2	—	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	17	—	21	—	ns	
Enable to End of Write	t_{ELEH}	t_{CW}	13	—	17	—	ns	3, 4
Enable to End of Write	t_{ELWH}	t_{CW}	13	—	17	—	ns	
Write Pulse Width	t_{WLEH}	t_{WP}	13	—	17	—	ns	
Data Valid to End of Write	t_{DVEH}	t_{DW}	9	—	11	—	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. All write cycle timing is referenced from the last valid address to the first transitioning address.
3. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
4. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedence condition.
5. $\overline{E1}$–$\overline{E2}$ are represented by $\overline{E}$ in these timing specifications, only one of the $\overline{Ex}$s may be asserted at any time.

WRITE CYCLE 2



ORDERING INFORMATION
(Order by Full Part Number)



Full Part Number – MCM2464Z22 MCM2464Z27

MCM3264

Product Preview

64K × 32 Bit Static Random Access Memory Module

The MCM3264 is a 2M bit static random access memory module organized as 65,536 words of 32 bits. The module is a 64 lead zig-zag in-line module consisting of eight MCM6209 fast static RAMs packaged in 28 J-lead small outline package (SOJ) and mounted on a printed circuit board along with a decoupling capacitor for each FSRAM.

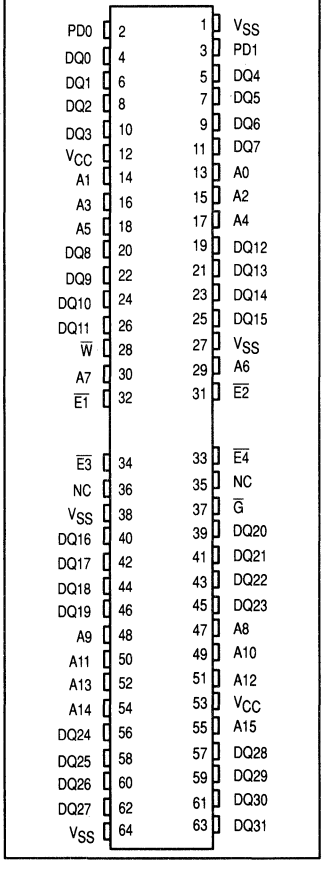
The MCM6209 is a high performance CMOS fast static RAM organized as 65,536 words of 4 bits, fabricated using high performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

The MCM3264 is equipped with output enable ($\overline{G}$) and four separate byte enable ($\overline{E1}$–$\overline{E4}$) inputs, allowing for greater system flexibility. The $\overline{G}$ input, when high, will force the outputs to high impedance. $\overline{Ex}$ high will do the same for byte x.

PD0 and PD1 are reserved for density expansion. PD0 is open and PD1 is connected to ground. These pins can be used to identify the density of the memory module.

- Single 5 V ± 10% Power Supply
- Fast Access Time: 20/25/30 ns
- Equal Address and Chip Enable Access Time
- Three State Outputs
- Full TTL Compatible
- JEDEC Standard Pin Out
- Power Operation: 1240/1160/1080 mA Maximum, Active AC
- High Board Density ZIP Module
- Byte Operation: Four Separate Chip Enables, One for Each Byte (Eight Bits)
- High Quality Four Layer FR4 PWB with Separate Internal Power and Ground Plane
- Incorporates Motorola's State-of-the-Art QuickRAM Fast Statics

PIN ASSIGNMENT
64-LEAD ZIG-ZAG IN-LINE MODULE
TOP VIEW

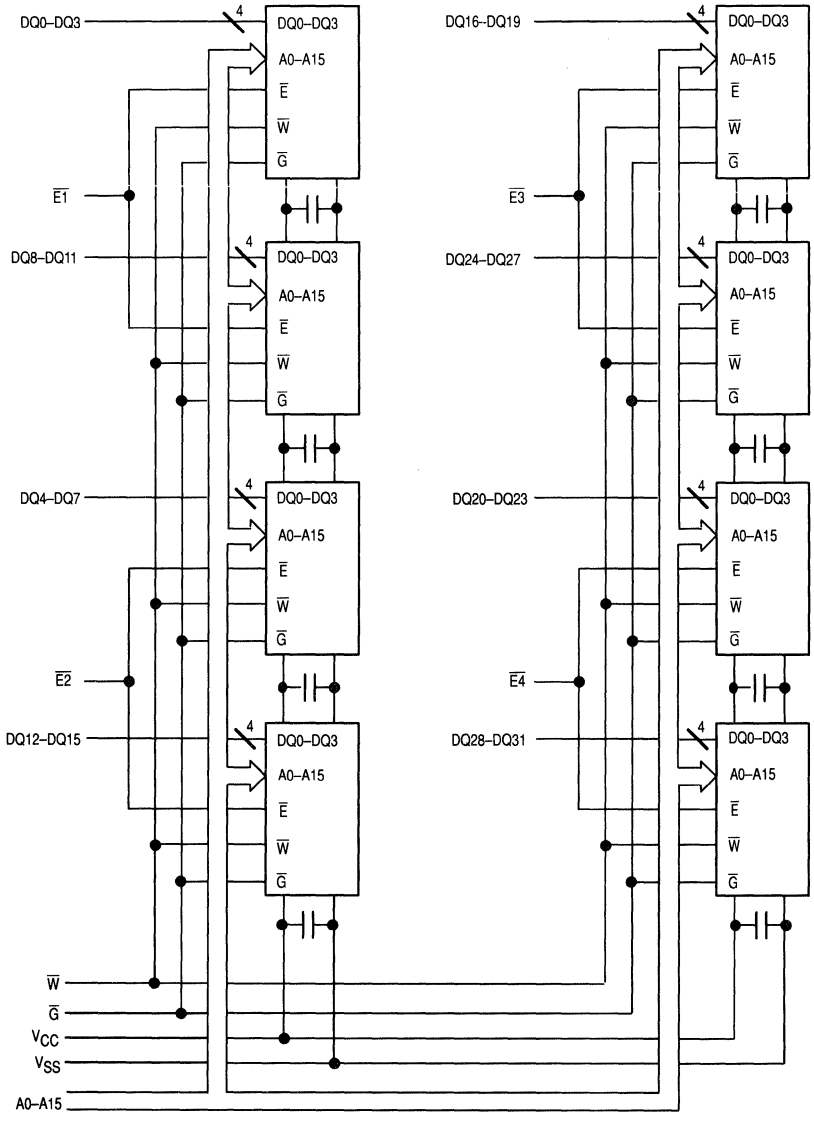


PIN NAMES	
A0-A15	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E1}$–$\overline{E4}$	Byte Enables
DQ0–DQ31	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
PD0-PD1	Package Density
NC	No Connection

All power supply and ground pins must be connected for proper operation of the device.

QuickRAM is a trademark of Motorola, Inc.

FUNCTIONAL BLOCK DIAGRAM



8

MCM3264 TRUTH TABLE

$\overline{Ex}$	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	Not Selected	I_{ISB1}, I_{SB2}	High-Z	—
L	H	H	Read	I_{CCA}	High-Z	—
L	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	X	L	Write	I_{CCA}	D_{in}	Write Cycle

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to 7.0	V
Voltage Relative to V_{SS}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation (T_A = 70°C, V_{CC} = 5 V, t_{AVAV} = 20 ns)	P_D	1.5	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

The devices on this module contain circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high impedence circuits.

These CMOS memory circuits have been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The module is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS
(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

8

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	3.0	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	– 0.5*	0.0	0.8	V

* V_{IL} (min) = – 3.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter		Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})		$I_{lkg(I)}$	—	—	± 8	µA
Output Leakage Current ($\overline{G}$, $\overline{Ex}$ = V_{IH}, V_{out} = 0 to V_{CCQ})		$I_{lkg(O)}$	—	—	± 8	µA
AC Supply Current ($\overline{G}$, $\overline{Ex}$ = V_{IH}, All Inputs = V_{IL} = 0.0 V and V_{IH} ≥ 3.0, I_{out} = 0 mA, Cycle Times ≥ t_{AVAV} min)	MCM3264-20: t_{AVAV} = 20 ns MCM3264-25: t_{AVAV} = 25 ns MCM3264-30: t_{AVAV} = 30 ns	I_{CCA}	— — —	960 880 800	1240 1160 1080	mA
Standby Current ($\overline{Ex}$ = V_{IH}, All Inputs = V_{IL} and V_{IH})	MCM3264-20: t_{AVAV} = 20 ns MCM3264-25: t_{AVAV} = 25 ns MCM3264-30: t_{AVAV} = 30 ns	I_{SB1}	—	240 240 240	400 360 320	mA
CMOS Standby Current ($\overline{S1}$ ≥ V_{CC} – 0.2 V, S0 ≤ 0.2 V, All Inputs ≥ V_{CC} – 0.2 V or ≤ 0.2 V)		I_{SB2}	—	160	240	mA
Output Low Voltage (I_{OL} = + 8.0 mA)		V_{OL}	—	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)		V_{IH}	2.4	—	—	V

NOTE: Good decoupling of the local power supply should always be used.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Typ	Max	Unit
Input Capacitance	All Pins Expect DQ0–DQ31 and $\overline{E1}$–$\overline{E4}$ $\overline{E1}$–$\overline{E4}$	C_{in}	32 10	48 14	pF
Input/Output Capacitance (DQ0–DQ31)		$C_{I/O}$	8	9	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS
(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 5 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol		MCM3264-20		MCM3264-25		MCM3264-30		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	20	—	25	—	30	—	ns	3
Address Access Time	t_{AVQV}	t_{AA}	—	20	—	25	—	30	ns	
Enable Access Time	t_{ELQV}	t_{ACS}	—	20	—	25	—	30	ns	
Output Enable Access Time	t_{GLQV}	t_{OE}	—	10	—	12	—	14	ns	
Output Hold from Address Change	t_{AXQX}	t_{OH}	4	—	4	—	4	—	ns	
Enable Low to Output Active	t_{ELQX}	t_{CLZ}	4	—	4	—	4	—	ns	4, 5, 6
Output Enable to Output Active	t_{GLQX}	t_{OLZ}	0	—	0	—	0	—	ns	4, 5, 6
Enable High to Output High-Z	t_{EHQZ}	t_{CHZ}	0	8	0	10	0	12	ns	4, 5, 6
Output Enable High to Output High-Z	t_{GHQZ}	t_{OHZ}	0	8	0	10	0	12	ns	4, 5, 6
Power Up Time	t_{ELICCH}	t_{PU}	0	—	0	—	0	—	ns	
Power Down Time	t_{EHICCL}	t_{PD}	—	20	—	25	—	30	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. $\overline{E1}$–$\overline{E4}$ are represented by $\overline{E}$ in these timing specifications, any combination of $\overline{E}$xs may be asserted.
3. All read cycle timing is referenced from the last valid address to the first transitioning address.
4. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} min, and t_{GHQZ} max is less than t_{GHQX} min, both for a given device and from device to device.
5. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E}$ = V_{IL}, G = V_{IL}).
8. Addresses valid prior to or coincident with $\overline{E}$ going low.

8

AC TEST LOADS

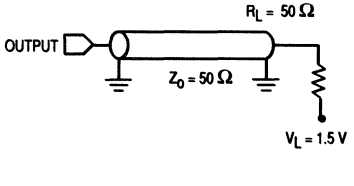


Figure 1A

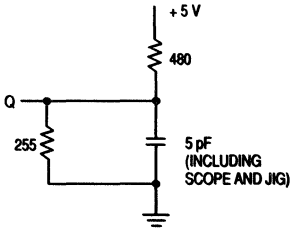
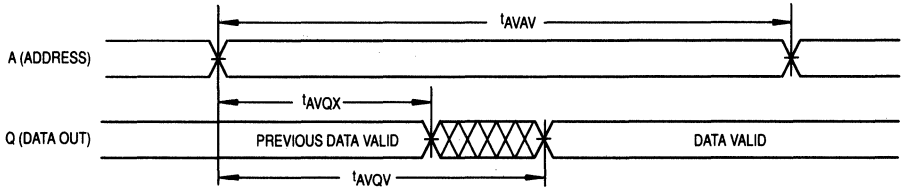


Figure 1B

TIMING LIMITS

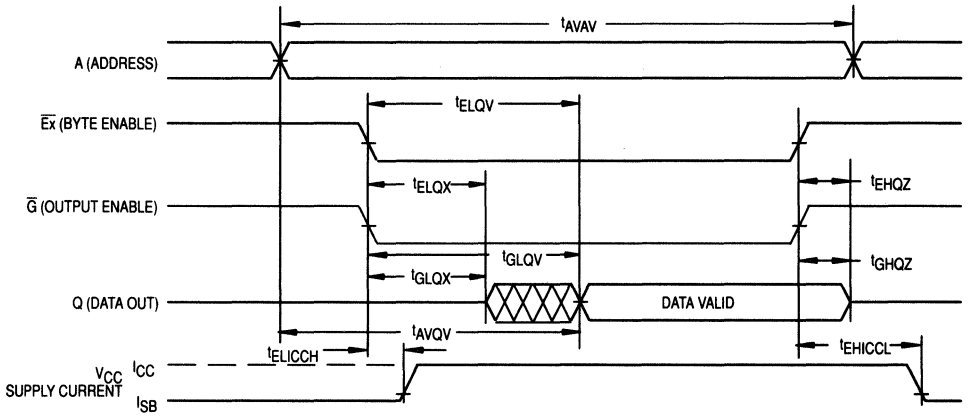
The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the module point of view. Thus, the access time is shown as a maximum since the module never provides data later than that time.

READ CYCLE 1 (See Note)



NOTE: Device is continuously selected ($\overline{E}$ = V_{IL}, G = V_{IL}).

READ CYCLE 2 (See Note)



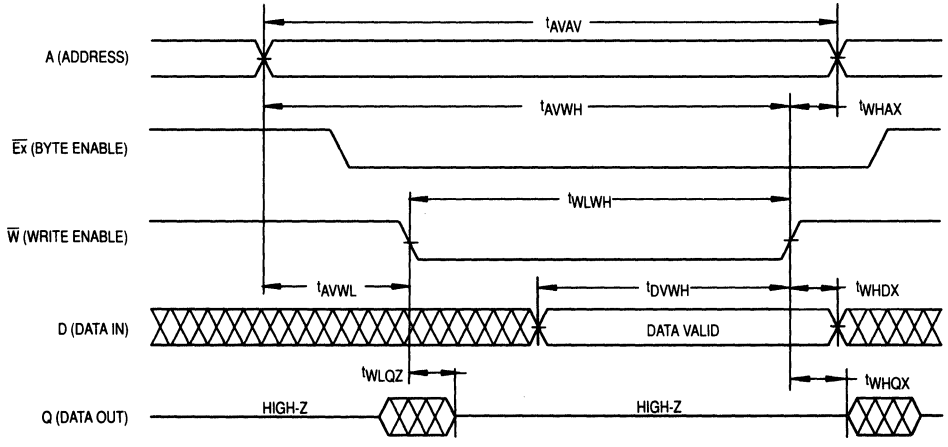
NOTE: Addresses valid prior to or coincident with $\overline{E}$ going low.

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol		MCM3264-20		MCM3264-25		MCM3264-30		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	20	—	25	—	30	—	ns	3
Address Setup Time	t_{AVWL}	t_{AS}	2	—	2	—	2	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	15	—	20	—	25	—	ns	
Write Pulse Width	t_{WLWH}	t_{WP}	15	—	20	—	25	—	ns	
Write Pulse Width, $\overline{G}$ High	t_{WLWH}	t_{WP}	12	—	15	—	20	—	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	8	—	10	—	12	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	—	0	—	0	—	ns	
Write Low to Data High-Z	t_{WLQZ}	t_{WZ}	0	8	0	10	0	12	ns	4, 5, 6
Write High to Output Active	t_{WHQX}	t_{OW}	4	—	4	—	4	—	ns	4, 5, 6
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. $\overline{E1}$–$\overline{E4}$ are represented by $\overline{E}$ in these timing specifications, any combination of $\overline{Ex}$s may be asserted. $\overline{G}$ is a don't care when $\overline{W}$ is low.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B.
5. This parameter is sampled and not 100% tested.
6. At any given time voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1



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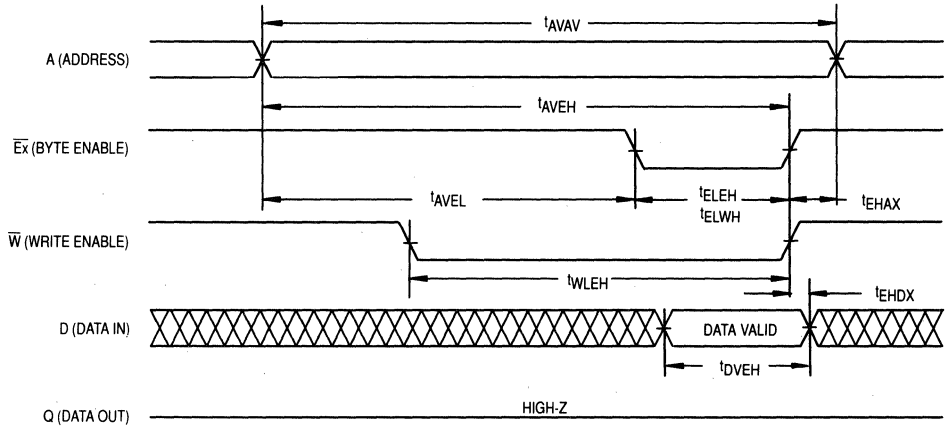
WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

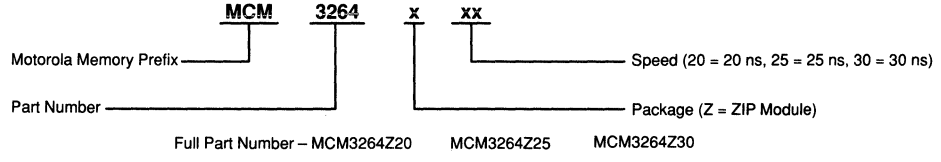
Parameter	Symbol		MCM3264-20		MCM3264-25		MCM3264-30		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	20	—	25	—	30	—	ns	3
Address Setup Time	t_{AVEL}	t_{AS}	2	—	2	—	2	—	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	15	—	20	—	25	—	ns	
Enable to End of Write	t_{ELEH}	t_{CW}	12	—	15	—	20	—	ns	4, 5
Enable to End of Write	t_{ELWH}	t_{CW}	12	—	15	—	20	—	ns	
Write Pulse Width	t_{WLEH}	t_{WP}	15	—	20	—	25	—	ns	
Data Valid to End of Write	t_{DVEH}	t_{DW}	8	—	10	—	12	—	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. $\overline{E1}$–$\overline{E4}$ are represented by $\overline{E}$ in these timing specifications, any combination of $\overline{Ex}$s may be asserted. $\overline{G}$ is a don't care when $\overline{W}$ is low.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedence condition.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedence condition.

WRITE CYCLE 2



ORDERING INFORMATION
(Order by Full Part Number)



MCM8256

Product Preview

256K × 8 Bit Static Random Access Memory Module

The MCM8256 is a 2M bit static random access memory module organized as 262,144 words of 8 bits. The module is a 64-lead zig-zag in-line package (ZIP) consisting of eight MCM6207 fast static RAMs packaged in 24 J-lead small outline package (SOJ) and mounted on a printed circuit board along with a decoupling capacitor for each FSRAM.

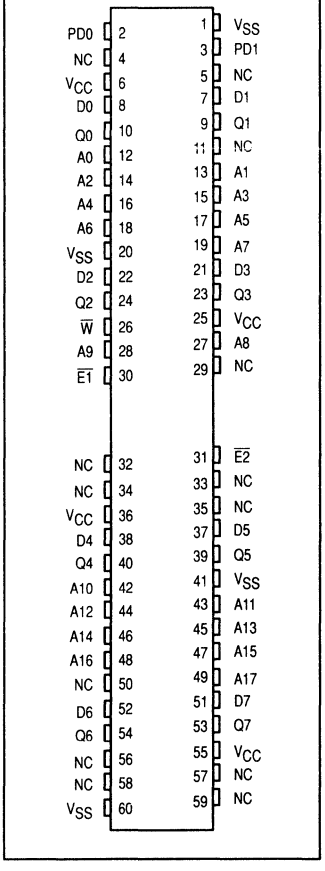
The MCM6207 is a high performance CMOS fast static RAM organized as 262,144 words of 1 bit, fabricated using high performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

The MCM8256 is equipped with separate chip enable ($\overline{E1}$–$\overline{E2}$) control inputs for each nibble, allowing for greater system flexibility. The $\overline{Ex}$ input, when high, will force the outputs of nibble x to high impedance.

PD0 and PD1 are reserved for density expansion. PD0 is open and PD1 is connected to ground. These pins can be used to identify the density of the memory module.

- Single 5 V ± 10% Power Supply
- Fast Access Time: 20/25/30 ns
- Equal Address and Chip Enable Access Time
- Three State Outputs
- Full TTL Compatible
- JEDEC Standard Pin Out
- Power Operation: 1200/1120/1040 mA Maximum, Active AC
- High Board Density ZIP Module
- Nibble Operation: Two Separate Chip Enables, One for Each Four Bits
- High Quality Multi-Layer FR4 PWB with Separate Internal Power and Ground Planes
- Custom Marking Available
- Incorporates Motorola's State-of-the-Art QuickRAM Fast Statics

PIN ASSIGNMENT
60-LEAD ZIG-ZAG IN-LINE MODULE
TOP VIEW



PIN NAMES	
A0–A17	Address Inputs
$\overline{W1}$	Write Enable
$\overline{E1}$–$\overline{E2}$	Byte Enables
DQ0–DQ7	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
PD0-PD1	Package Density
NC	No Connection

All power supply and ground pins must be connected for proper operation of the device.

QuickRAM is a trademark of Motorola, Inc.

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

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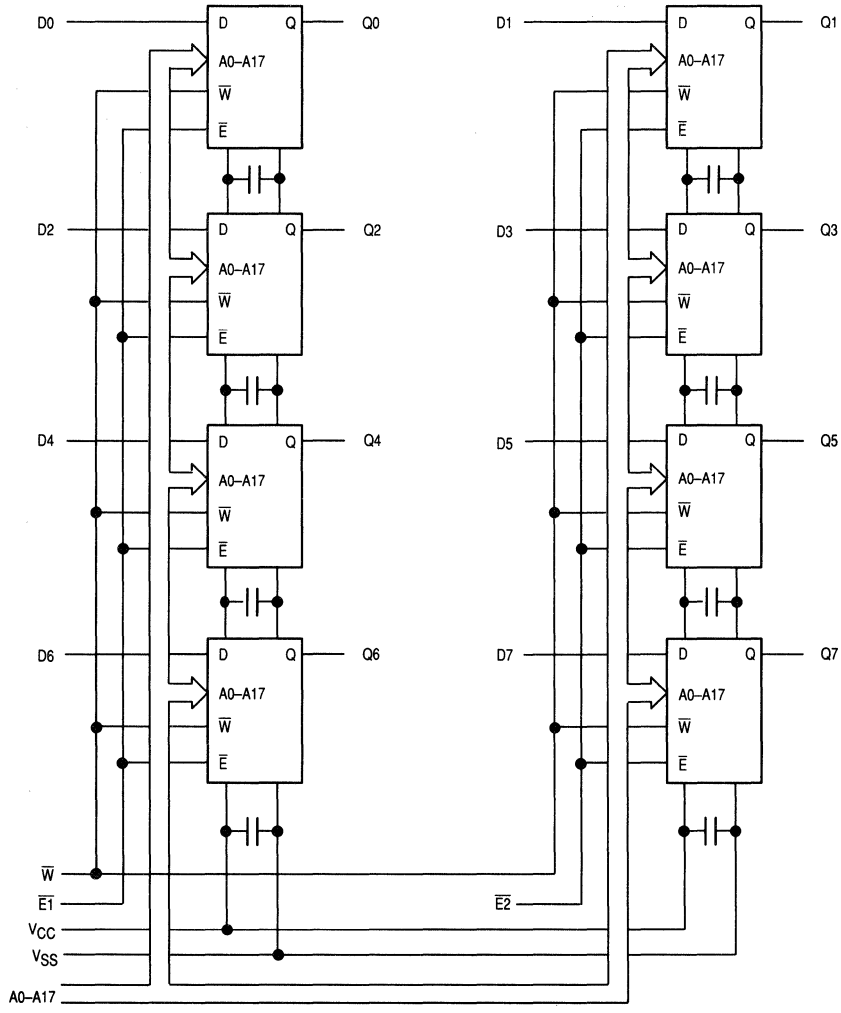
FUNCTIONAL BLOCK DIAGRAM



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MCM8256 TRUTH TABLE

$\overline{E}x$	$\overline{W}$	Mode	V_{CC} Current	Input	Output	Cycle
H	X	Not Selected	I_{ISB1}, I_{SB2}	High-Z	High-Z	—
L	H	Read	I_{CCA}	High-Z	D_{out}	Read Cycle
L	L	Write	I_{CCA}	D_{in}	High-Z	Write Cycle

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to 7.0	V
Voltage Relative to V_{SS}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation (T_A = 70°C, V_{CC} = 5 V, t_{AVAV} = 20 ns)	P_D	1.5	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

The devices on this module contain circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high impedence circuits.

These CMOS memory circuits have been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The module is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS
(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	3.0	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	– 0.5*	0.0	0.8	V

* V_{IL} (min) = – 3.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter		Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})		$I_{lkg(I)}$	—	—	± 8	µA
Output Leakage Current ($\overline{E1}$ and $\overline{E2}$ = V_{IH}, V_{out} = 0 to V_{CC})		$I_{lkg(O)}$	—	—	± 8	µA
AC Supply Current ($\overline{E1}$ and $\overline{E2}$ = V_{IL}, All Inputs = V_{IL} = 0.0 V and V_{IH} ≥ 3.0, I_{out} = 0 mA, Cycle Times ≥ t_{AVAV} min)	MCM8256-20: t_{AVAV} = 20 ns	I_{CCA}	—	960	1200	mA
	MCM8256-25: t_{AVAV} = 25 ns		—	880	1120	
	MCM8256-30: t_{AVAV} = 30 ns		—	800	1040	
Standby Current ($\overline{E1}$ and $\overline{E2}$ = V_{IH}, All Inputs = V_{IL} and V_{IH})		I_{SB1}	—	240	320	mA
CMOS Standby Current (V_{CC} = Max, f = 0 MHz, $\overline{E}$ ≥ V_{CC} – 0.2 V, V_{in} ≤ V_{SS} + 0.2 V or ≥ V_{CC} – 0.2 V)		I_{SB2}	—	160	240	mA
Output Low Voltage (I_{OL} = + 8.0 mA)		V_{OL}	—	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)		V_{IH}	2.4	—	—	V

NOTE: Good decoupling of the local power supply should always be used.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Typ	Max	Unit
Input Capacitance	$\overline{W}$ and Address	C_{in}	45	54	pF
	$\overline{E1}$–$\overline{E2}$		25	30	
	D0–D7		6	7	
Input/Output Capacitance	Q0–Q7	$C_{I/O}$	8	9	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS
(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 5 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol		MCM8256-20		MCM8256-25		MCM8256-30		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	20	—	25	—	30	—	ns	3
Address Access Time	t_{AVQV}	t_{AA}	—	20	—	25	—	30	ns	
Enable Access Time	t_{ELQV}	t_{ACS}	—	20	—	25	—	30	ns	
Output Hold from Address Change	t_{AXQX}	t_{OH}	4	—	4	—	4	—	ns	
Enable Low to Output Active	t_{ELQX}	t_{CLZ}	4	—	4	—	4	—	ns	4, 5, 6
Enable High to Output High-Z	t_{EHQZ}	t_{CHZ}	0	8	0	10	0	12	ns	4, 5, 6
Power Up Time	t_{ELICCH}	t_{PU}	0	—	0	—	0	—	ns	
Power Down Time	t_{EHICCL}	t_{PD}	—	20	—	25	—	30	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. $\overline{E}1$–$\overline{E}2$ are represented by $\overline{E}$ in these timing specifications, any combination of $\overline{E}$xs may be asserted.
3. All read cycle timing is referenced from the last valid address to the first transitioning address.
4. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} min both for a given device and from device to device.
5. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E}$ = V_{IL}).
8. Addresses valid prior to or coincident with $\overline{E}$ going low.

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AC TEST LOADS

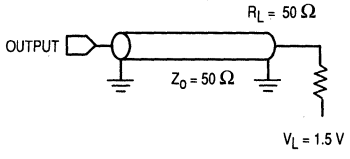


Figure 1A

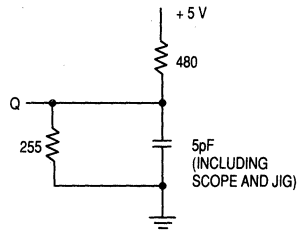
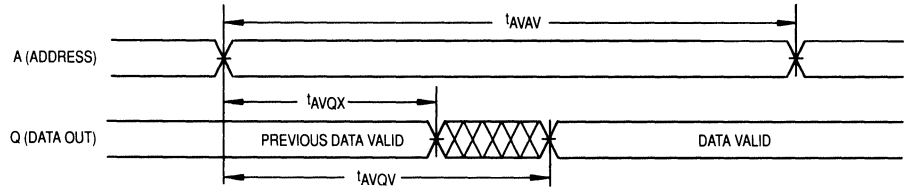


Figure 1B

TIMING LIMITS

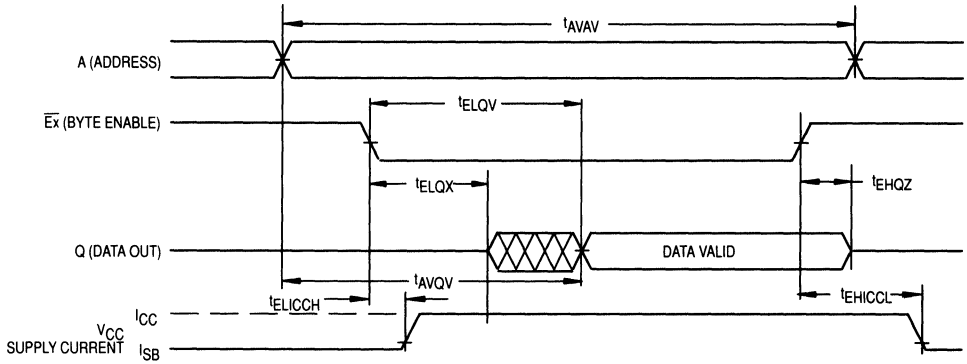
The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the module point of view. Thus, the access time is shown as a maximum since the module never provides data later than that time.

READ CYCLE 1 (See Note)



NOTE: Device is continuously selected ($\overline{E}$ = V_{IL}).

READ CYCLE 2 (See Note)



NOTE: Addresses valid prior to or coincident with $\overline{E}$ going low.

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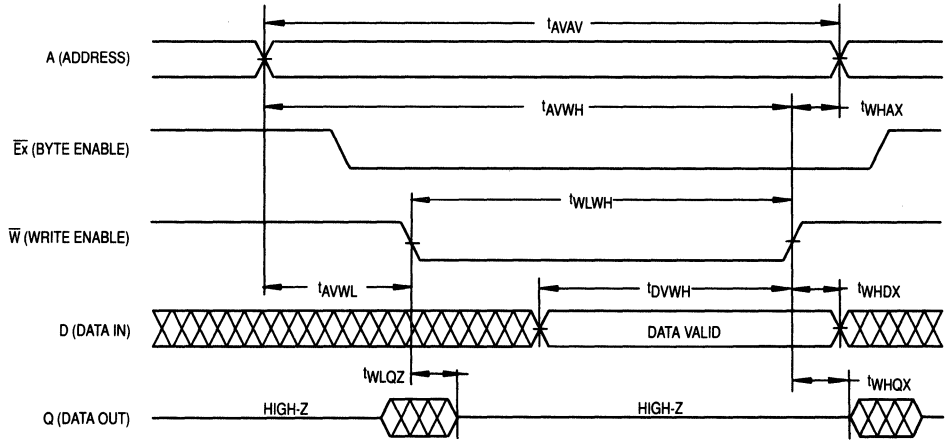
WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol		MCM8256-20		MCM8256-25		MCM8256-30		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	20	—	25	—	30	—	ns	3
Address Setup Time	t_{AVWL}	t_{AS}	2	—	2	—	2	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	15	—	20	—	25	—	ns	
Write Pulse Width	t_{WLWH}	t_{WP}	12	—	15	—	20	—	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	8	—	10	—	12	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	—	0	—	0	—	ns	
Write Low to Data High-Z	t_{WLQZ}	t_{WZ}	0	8	0	10	0	12	ns	4, 5, 6
Write High to Output Active	t_{WHQX}	t_{OW}	4	—	4	—	4	—	ns	4, 5, 6
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. $\overline{E1}$–$\overline{E2}$ are represented by $\overline{E}$ in these timing specifications, any combination of $\overline{Ex}$s may be asserted.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B.
5. This parameter is sampled and not 100% tested.
6. At any given time voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1

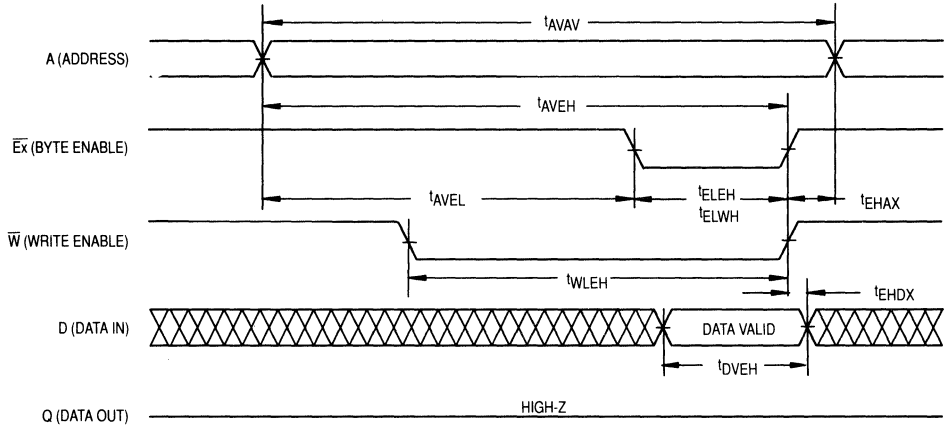


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

Parameter	Symbol		MCM8256-20		MCM8256-25		MCM8256-30		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	20	—	25	—	30	—	ns	3
Address Setup Time	t_{AVEL}	t_{AS}	2	—	2	—	2	—	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	15	—	20	—	25	—	ns	
Enable to End of Write	t_{ELEH}	t_{CW}	12	—	15	—	20	—	ns	4, 5
Enable to End of Write	t_{ELWH}	t_{CW}	12	—	15	—	20	—	ns	
Write Pulse Width	t_{WLEH}	t_{WP}	15	—	20	—	25	—	ns	
Data Valid to End of Write	t_{DVEH}	t_{DW}	8	—	10	—	12	—	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. $\overline{E}1$–$\overline{E}2$ are represented by $\overline{E}$ in these timing specifications, any combination of $\overline{E}$xs may be asserted.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedence condition.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedence condition.

WRITE CYCLE 2



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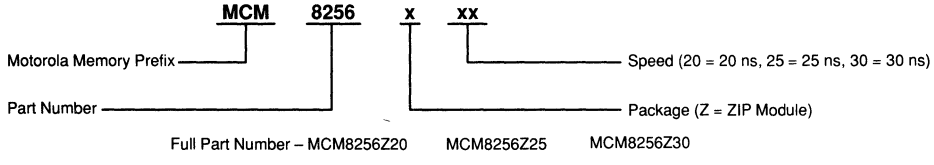
ORDERING INFORMATION
(Order by Full Part Number)



Full Part Number – MCM8256Z20 MCM8256Z25 MCM8256Z30

Application Specific MOS Static RAMs

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APPLICATION SPECIFIC STATIC RAMs

Description	Organi-zation	Motorola Part Number	Pin Count	Packaging	Address/ Cycle Time (ns Max)	Operating Current (mA max)	Tech-nology
Cache Tag RAM	4Kx4	MCM4180	24/22	300 mil SOJ/PDIP	18/20/25	140	HCMOS
Cache Tag RAM with Status Bit Registers	4Kx4	MCM62350	24	300 mil SOJ/PDIP	18/20/25	140	HCMOS
		MCM62351	24	300 mil SOJ/PDIP	18/20/25	140	HCMOS
Synchronous Static RAM	16Kx4	MCM6293	28	300 mil SOJ/PDIP	20/25	140	HCMOS
		MCM6294	28	300 mil SOJ/PDIP	20/25	140	HCMOS
		MCM6295	28	300 mil SOJ/PDIP	25/30	140	HCMOS
	64Kx4	MCM62980	28	300 mil SOJ	15/20	170	HCMOS
		MCM62982	28	300 mil SOJ	12/15	170	HCMOS
	16Kx16	MCM62990	52	PLCC	17/20	360	HCMOS
	4x64Kx1	MCM62981	32	300 mil SOJ	15/20	170	HCMOS
		MCM62983	32	300 mil SOJ	12/15	170/130	HCMOS
	4Kx10	MCM62963	44	PLCC	18/20/25	170	HCMOS
	4Kx12	MCM62973	44	PLCC	18/20/25	170	HCMOS
		MCM62974	44	PLCC	18/20/25	170	HCMOS
		MCM62975	44	PLCC	25/30	170	HCMOS
	32Kx9	MCM62940	44	PLCC	19/24	250	HCMOS
		MCM62950	44	PLCC	20/25	250	HCMOS
		MCM62960	44	PLCC	17/20/25	180	HCMOS
		MCM62486	44	PLCC	19/24	250	HCMOS
		MCM62110	52	PLCC	15/20	250	HCMOS
DSPRAM	8Kx24	MCM56824	52	PLCC	25/30/35	250/210/180	HCMOS
Latched Address SRAM	8Kx20	MCM62820	52	PLCC	23/30	240/185	HCMOS
	16Kx16	MCM62995	52	PLCC	17/20/25	360	HCMOS

MCM4180

4K x 4 Bit Cache Address Tag Comparator

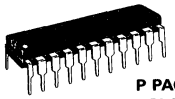
The MCM4180 is a 16,384 bit cache address tag comparator organized as 4096 tags of 4 bits, fabricated using Motorola's high-performance silicon-gate CMOS technology. The device integrates a 4K x 4 SRAM core with an on-board comparator for efficient implementation of a cache memory.

The device has a $\overline{CLR}$ pin for flash clear of the RAM, useful for system initialization.

The MCM4180 compares RAM contents with current input data. The result is either an active high MATCH level for a cache hit, or an active low level for a cache miss.

The MCM4180 is available in 22 lead plastic DIP and 24 lead SOJ packages.

- Single 5 V ±10% Power Supply
- Fast Address to MATCH Time: 18/20/22/25 ns max
- Fast Data to MATCH Time: 10/10/10/12 ns max
- Fast Read of Tag RAM Contents: 20/22/25/30 ns max
- Flash Clear of the Tag RAM ($\overline{CLR}$ Pin)
- Pin and Function Compatible with MK41H80

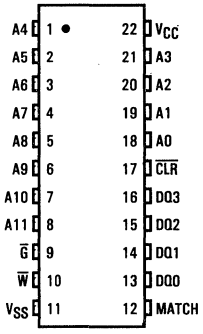


P PACKAGE
PLASTIC
CASE 736A

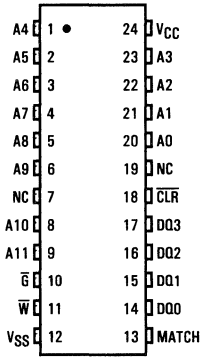
J PACKAGE
300 MIL SOJ
CASE 810A

PIN ASSIGNMENT

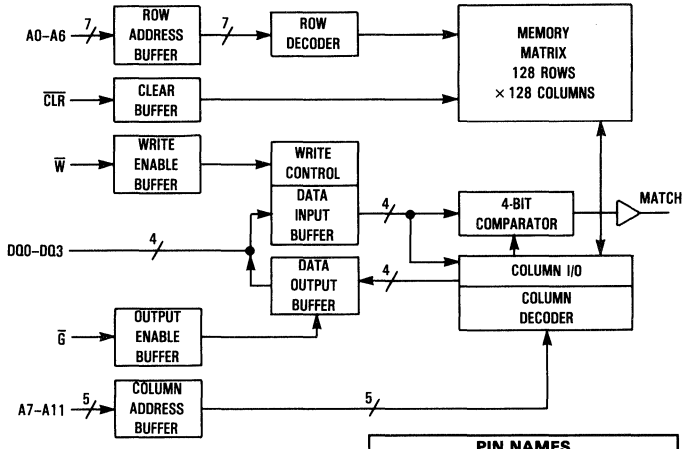
DUAL-IN-LINE



SMALL OUTLINE



BLOCK DIAGRAM



PIN NAMES	
A0-A11	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{CLR}$	Flash Clear Input
MATCH	MATCH (Hit) Output
DQ0-DQ3	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground
NC	No Connection

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TRUTH TABLE

$\overline{W}$	$\overline{G}$	$\overline{CLR}$	DQ0-DQ3	MATCH	Mode
H	H	H	Compare D_{in}	Valid	Compare
L	X	H	D_{in}	Assert	Write
H	L	H	D_{out}	Assert	Read
X	X	L	High-Z	Assert	Clear

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}/V_{out}	−0.5 to V_{CC}+0.5	V
Output Current MATCH Output I/O Pins, Per I/O	I_{out}	±40 ±20	mA
Power Dissipation (T_A = 25°C)	P_D	1.0	W
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Temperature Under Bias	T_{bias}	−10 to +85	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

*V_{IL} min = −0.5 V dc; V_{IL} min = −3.0 V ac (pulse width ≤20 ns)

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	±1.0	μA
Output Leakage Current, Except MATCH Output ($\overline{G}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	±1.0	μA
AC Supply Current (I_{out} = 0 mA, All Inputs = V_{IL} or V_{IH}, Cycle Time ≥t_{AVAV} min)	I_{CCA}	—	140*	mA
Output Low Voltage (I/O Pins: I_{OL} = 8.0 mA, MATCH Output: I_{OL} = 12.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I/O Pins: I_{OH} = −4.0 mA, MATCH Output: I_{OH} = −10.0 mA)	V_{OH}	2.4	—	V

*I_{CC} active current for the clear cycle exceeds this specification. However, this is a transient phenomenon and will not affect the power dissipation of the device. Good decoupling of the local power supply should always be used.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	4	5	pF
I/O Capacitance	C_{out}	5	7	pF
MATCH Output Capacitance	C_{match}	6	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . .0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns

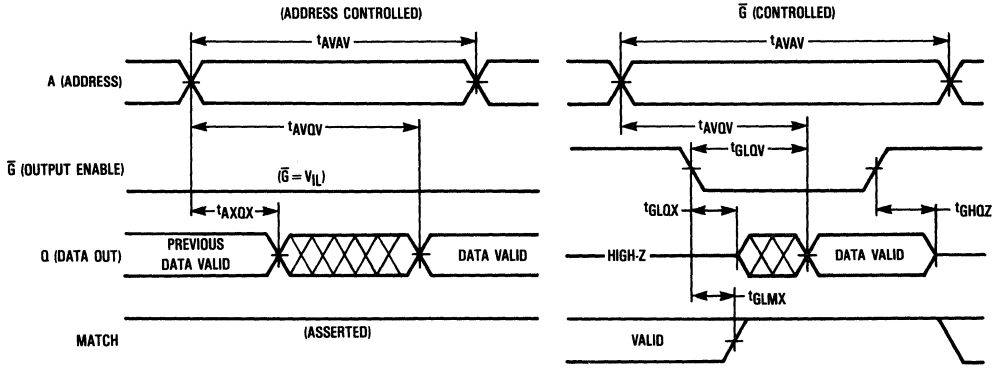
Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load (I/O Pins) . . . . . See Figure 1a
Output Load (MATCH Output) . . . . . See Figure 1c

READ CYCLE (See Note 1)

Characteristic	Symbol		MCM4180-18		MCM4180-20		MCM4180-22		MCM4180-25		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	20	–	22	–	25	–	30	–	ns	
Address Access Time	t_{AVQV}	t_{AA}	–	20	–	22	–	25	–	30	ns	
$\overline{G}$ Access Time	t_{GLQV}	t_{OEA}	–	11	–	12	–	12	–	12	ns	
Output Hold from Address Change	t_{AXQX}	t_{OH}	0	–	0	–	0	–	0	–	ns	
$\overline{G}$ Low to Output Active	t_{GLQX}	t_{OEL}	3	–	3	–	5	–	5	–	ns	2
$\overline{G}$ High to Output High-Z	t_{GHQZ}	t_{OEZ}	–	7	–	8	–	8	–	10	ns	2
$\overline{G}$ Low to MATCH Assert	t_{GLMX}	t_{CH}	0	8	0	10	0	10	0	12	ns	

NOTES:
1. $\overline{CLR} = V_{IH}$, $\overline{W} = V_{IH}$ continuously during read cycles.
2. Transition is measured ±500 mV from steady state voltage with load of Figure 1b. This parameter is sampled and not 100% tested.

READ CYCLE



AC TEST LOADS

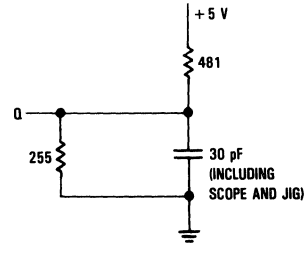


Figure 1a

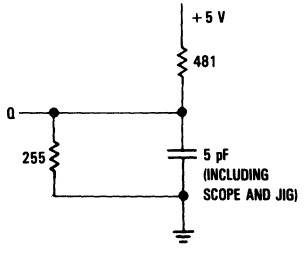


Figure 1b

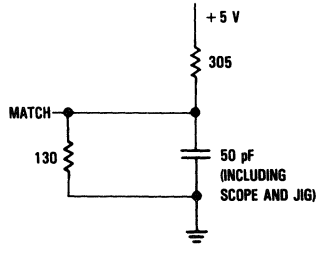


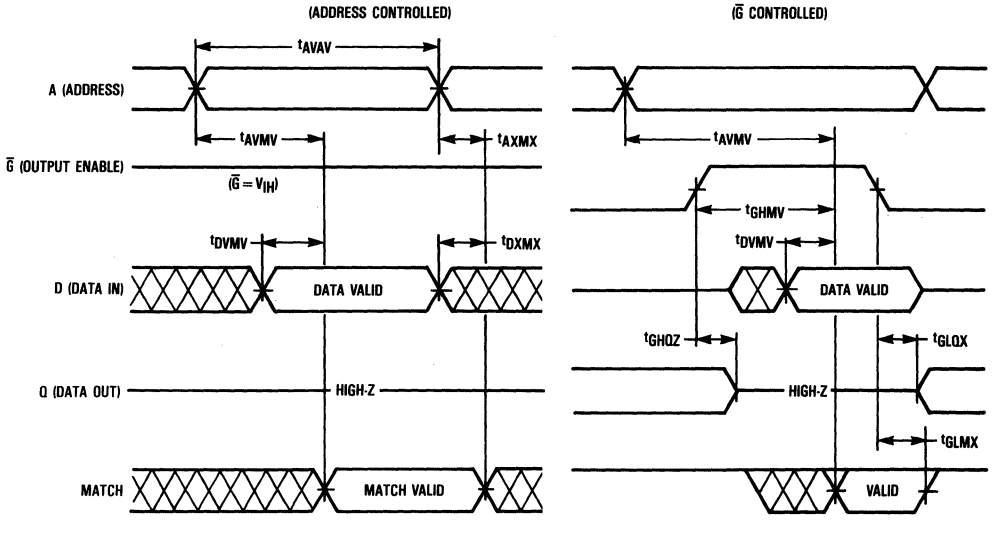
Figure 1c

COMPARE CYCLE (See Note 1)

Characteristic	Symbol		MCM4180-18		MCM4180-20		MCM4180-22		MCM4180-25		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max	Min	Max		
Compare Cycle Time	t_{AVAV}	t_C	20	–	22	–	25	–	30	–	ns	
Address Valid to MATCH Valid	t_{AVMV}	t_{ACA}	–	18	–	20	–	22	–	25	ns	
$\overline{G}$ High to MATCH Valid	t_{GHMV}	t_{GCA}	–	15	–	15	–	15	–	18	ns	
Data Valid to MATCH Valid	t_{DVMV}	t_{DCA}	–	10	–	10	–	10	–	12	ns	
MATCH Hold from $\overline{G}$ Low	t_{GLMX}	t_{CH}	0	10	0	10	0	10	0	12	ns	
MATCH Hold from Address Change	t_{AXMX}	t_{ACH}	5	–	5	–	5	–	5	–	ns	
MATCH Hold from Data Invalid	t_{DXMX}	t_{DCH}	3	–	3	–	3	–	3	–	ns	
$\overline{G}$ Low to Output Active	t_{GLQX}	t_{LZ}	3	–	3	–	5	–	5	–	ns	2
$\overline{G}$ High to Output High-Z	t_{GHQZ}	t_{HZ}	–	8	–	8	–	8	–	10	ns	2

NOTES:
1. A compare cycle is performed when $\overline{CLR}$, $\overline{W}$, and $\overline{G}$ are all high.
2. Transition is measured ±500 mV from steady state voltage with load of Figure 1b. This parameter is sampled and not 100% tested.

COMPARE CYCLE

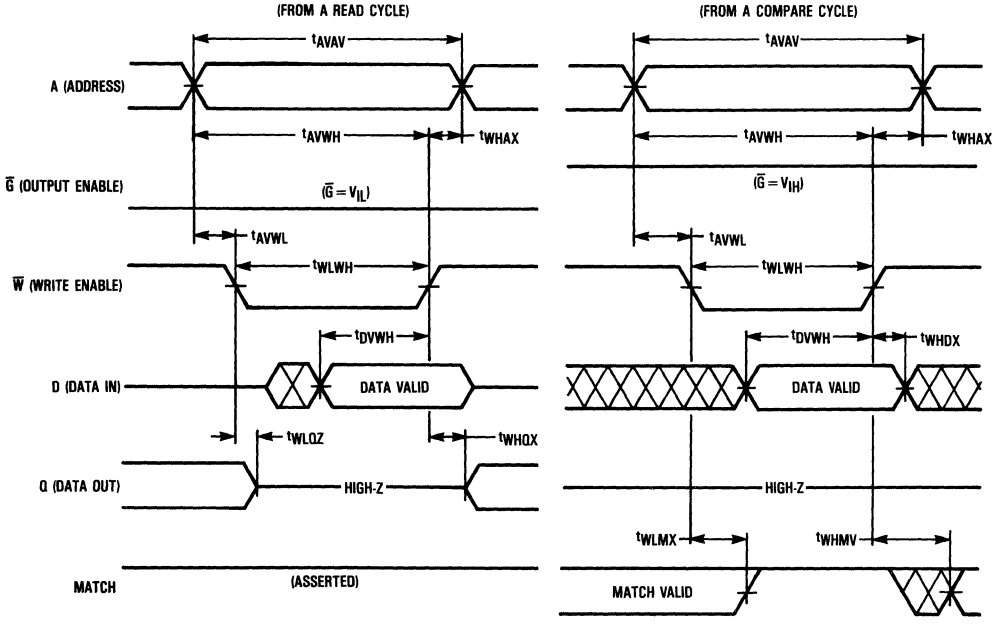


WRITE CYCLE (See Note 1)

Characteristic	Symbol		MCM4180-18		MCM4180-20		MCM4180-22		MCM4180-25		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	20	–	22	–	25	–	30	–	ns	
Write Pulse Width	t_{WLWH}	t_{WEW}	12	–	14	–	18	–	20	–	ns	
Address Setup to Beginning of Write	t_{AVWL}	t_{AS}	0	–	0	–	0	–	0	–	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	16	–	16	–	18	–	20	–	ns	
Data Valid to End of Write	t_{DVWH}	t_{DS}	10	–	10	–	10	–	12	–	ns	
Data Hold from Write End	t_{WHDX}	t_{DH}	0	–	0	–	0	–	0	–	ns	
Write Low to Output High-Z	t_{WLQZ}	t_{HZ}	0	8	0	8	0	9	0	10	ns	2
Address Hold from Write End	t_{WHAX}	t_{WAH}	0	–	0	–	0	–	0	–	ns	
Write Low to MATCH Assert	t_{WLMX}	t_{WCH}	0	12	0	15	0	15	0	15	ns	
Write High to MATCH Valid	t_{WHMV}	t_{WCA}	–	20	–	20	–	22	–	25	ns	
Write High to Output Active	t_{WHQX}	t_{LZ}	3	–	3	–	5	–	5	–	ns	2

NOTES:
1. A write occurs during the overlap of $\overline{W}$ low and $\overline{CLR}$ high.
2. Transition is measured ±500 mV from steady state voltage with load of Figure 1b. This parameter is sampled and not 100% tested.

WRITE CYCLE



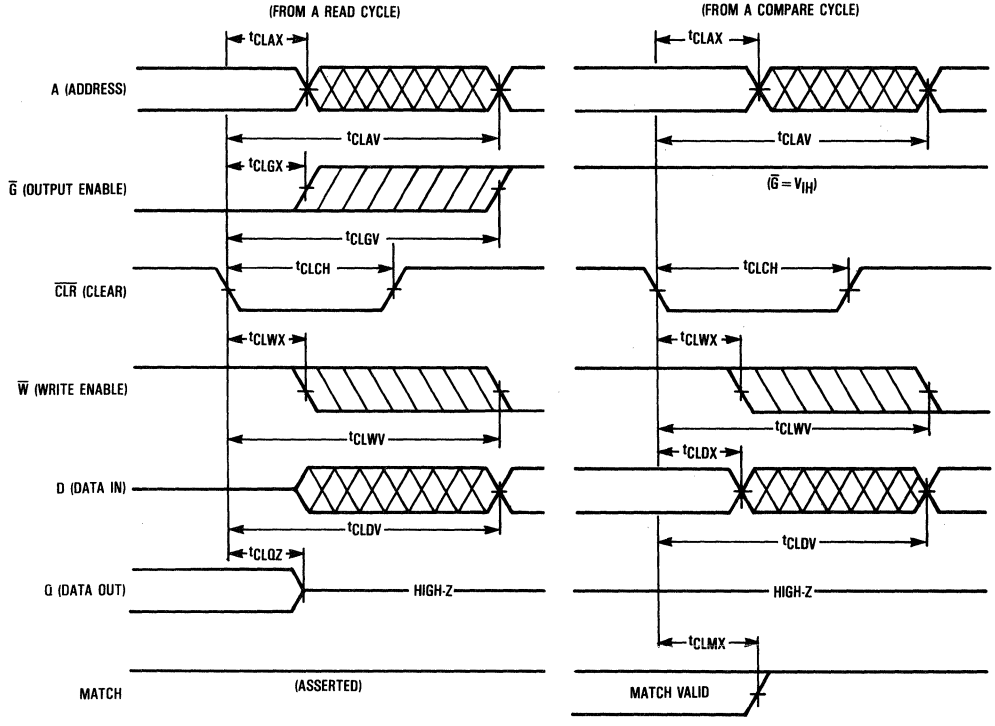
9

CLEAR CYCLE (See Note 1)

Characteristic		Symbol		MCM4180-18		MCM4180-20		MCM4180-22		MCM4180-25		Unit	Notes
		Standard	Alternate	Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{CLR}$ Low to Inputs Recognized (Clear Cycle Time)	A	t_{CLAV}	t_{CR}	–	70	–	70	–	70	–	70	ns	2
	$\overline{G}$	t_{CLGV}	t_{CR}										
	$\overline{W}$	t_{CLWV}	t_{CR}										
	D	t_{CLDV}	t_{CR}										
$\overline{CLR}$ Pulse Width		t_{CLCH}	t_{CLP}	20	–	22	–	25	–	30	–	ns	2
$\overline{CLR}$ Low to Inputs Don't Care	A	t_{CLAX}	t_{CX}	0	–	0	–	0	–	0	–	ns	
	$\overline{G}$	t_{CLGX}	t_{CX}										
	D	t_{CLDX}	t_{CX}										
	$\overline{W}$	t_{CLWX}	t_{CX}										
$\overline{CLR}$ Low to MATCH Assert		t_{CLMX}	t_{MH}	0	15	0	15	0	15	0	18	ns	
$\overline{CLR}$ Low to Output High-Z		t_{CLQZ}	t_{CZ}	–	15	–	15	–	15	–	18	ns	3

NOTES:
1. The address, data, $\overline{W}$, and $\overline{G}$ inputs are a don't care during a clear cycle.
2. The clear cycle is initiated at the falling edge of $\overline{CLR}$.
3. Transition is measured ±500 mV from steady state voltage with load of Figure 1b. This parameter is sampled and not 100% tested.

CLEAR CYCLE



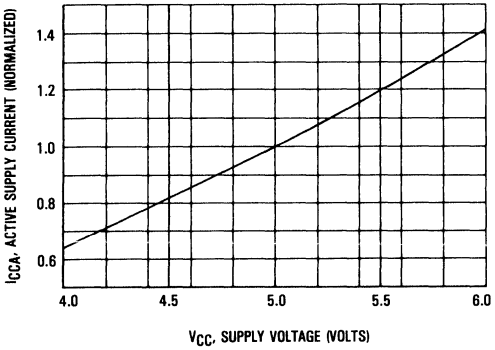


Figure 2. Active Supply Current versus Supply Voltage

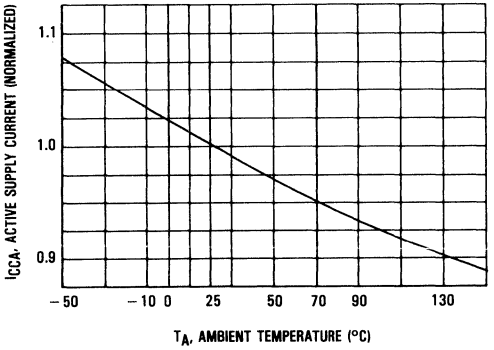


Figure 3. Active Supply Current versus Temperature

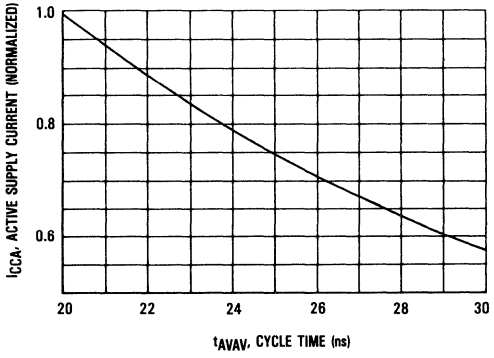


Figure 4. Active Supply Current versus Cycle Time

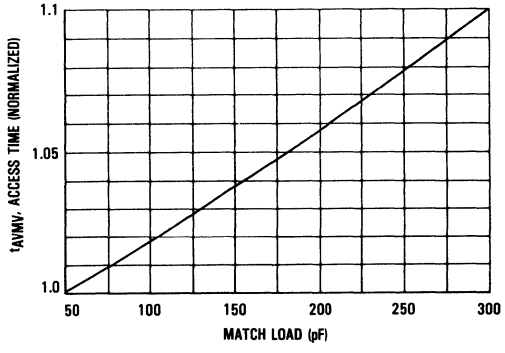


Figure 5. Address to MATCH Access Time versus MATCH AC Test Load Capacitance of Figure 1c

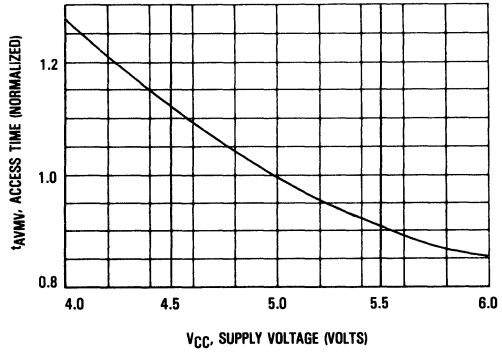


Figure 6. Address to MATCH Access Time versus Supply Voltage

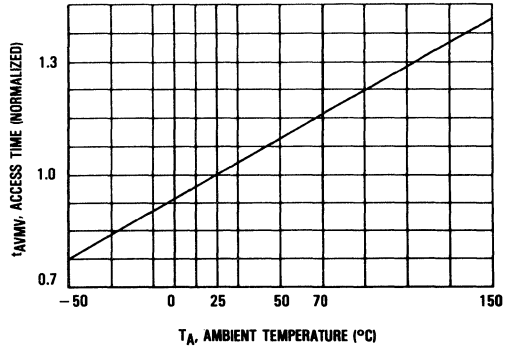


Figure 7. Address to MATCH Access Time versus Temperature

9

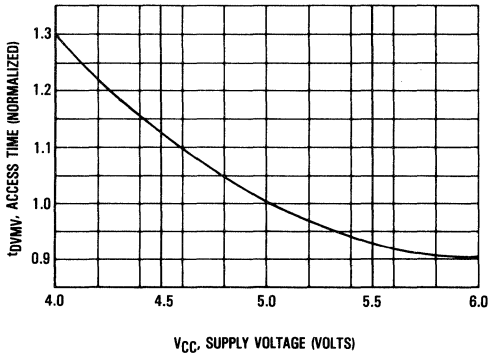


Figure 8. Data to MATCH Access Time versus Supply Voltage

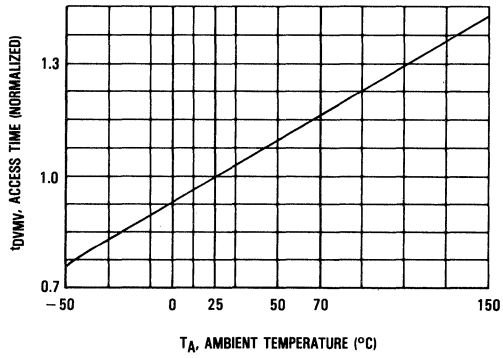


Figure 9. Data to MATCH Access Time versus Temperature

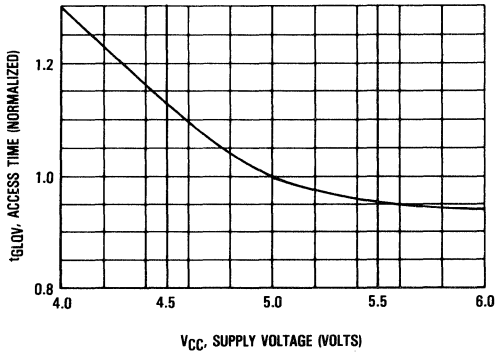


Figure 10. Output Enable to MATCH Access Time versus Supply Voltage

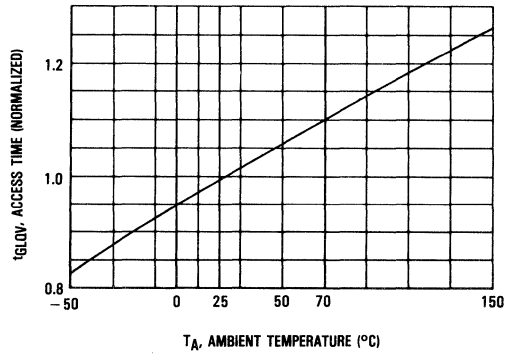


Figure 11. Output Enable to MATCH Access Time versus Temperature

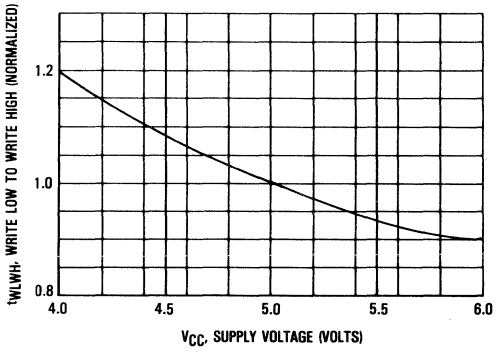


Figure 12. Write Pulse Width versus Supply Voltage

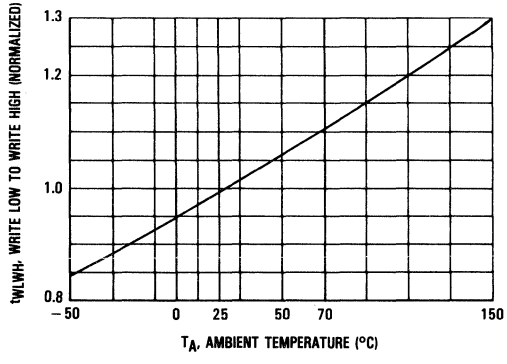


Figure 13. Write Pulse Width versus Temperature

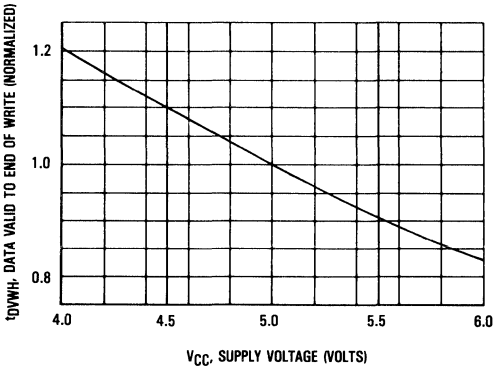


Figure 14. Data Setup Time versus Supply Voltage

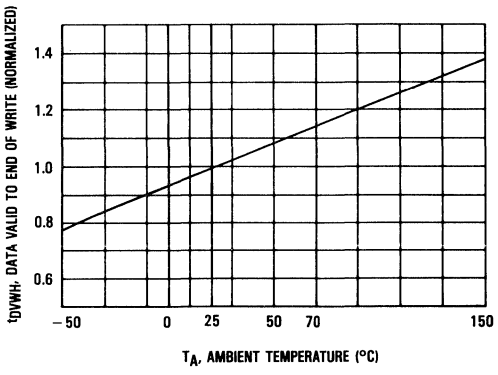


Figure 15. Data Setup Time versus Temperature

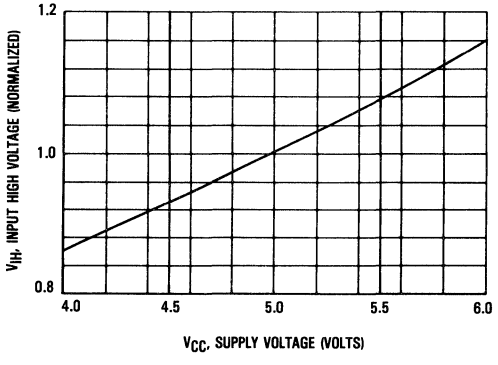


Figure 16. Input High Voltage versus Supply Voltage

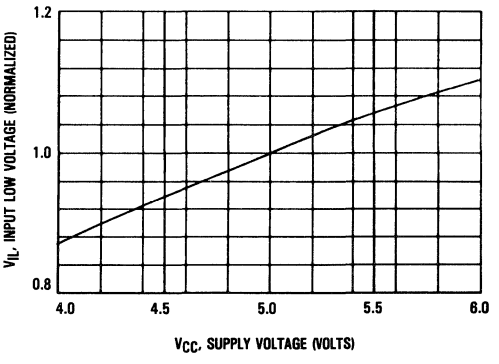


Figure 17. Input Low Voltage versus Supply Voltage

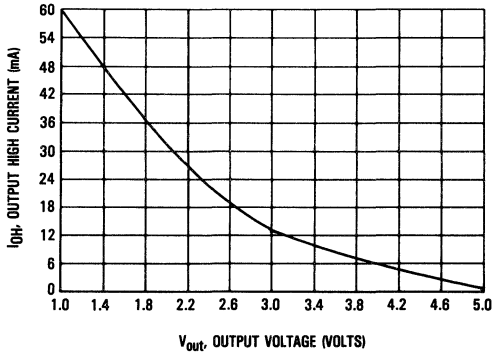


Figure 18. Output Source Current versus Output Voltage

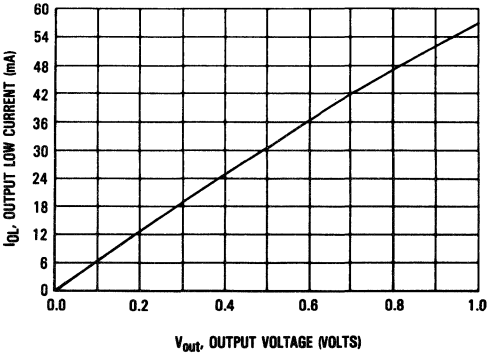
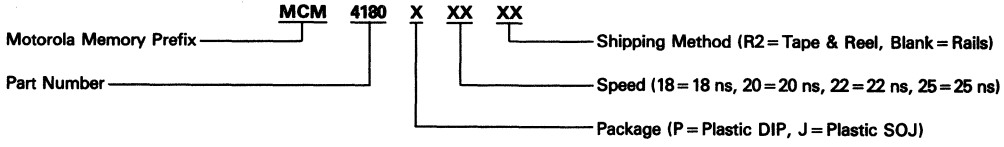


Figure 19. Output Sink Current versus Output Voltage

ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers—				
	MCM4180P18	MCM4180P20	MCM4180P22	MCM4180P25
	MCM4180J18	MCM4180J20	MCM4180J22	MCM4180J25
	MCM4180J18R2	MCM4180J20R2	MCM4180J22R2	MCM4180J25R2

9

MCM6292

16K x 4 Bit Synchronous Static RAM
with Transparent Outputs

The MCM6292 is a 65,536 bit synchronous static random access memory organized as 16,384 words of 4 bits, fabricated using Motorola's second-generation high-performance silicon-gate CMOS (HCMOS III) technology. The device integrates input registers, high speed SRAM, and high-drive capability output latching onto a single monolithic circuit for reduced parts count implementation of cache data RAM and writeable control store applications. The MCM6292 is well suited for applications involving the MC68030, MC68040, and AMD29K microprocessors. It is ideal for burst mode or pipelined bus applications.

Synchronous design allows precise cycle control with the use of an external clock (K), while CMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

The address (A0-A13), data (D0-D3), write ($\overline{W}$), and chip enable ($\overline{E}$) inputs are all clock (K) controlled, positive-edge-triggered, noninverting registers.

The MCM6292 provides transparent output operation when K is low for access of RAM data within the same cycle (output data is latched when K is high).

Write operations are internally self-timed and initiated by the rising edge of the K input. This feature eliminates complex off-chip write pulse generation and provides increased flexibility for incoming signals.

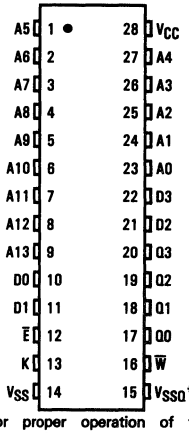
The MCM6292 is available in a 300-mil, 28-pin plastic DIP as well as a 300-mil, 28-pin plastic SOJ package.

- Single 5 V ±10% Power Supply
- Fast Access and Cycle Times: 25/30 ns Max
- Address, Data Input, $\overline{E}$, and $\overline{W}$ Registers On-Chip
- Transparent Output Latch for Access Within the Same Cycle
- High Output Drive Capability
- Internally Self-Timed Write Pulse Generation
- Separate Data Input and Data Output Pins
- High Board Density SOJ Package Available
- Typical Applications: General-Purpose Buffer Storage, Writeable Control Store, Data Cache, or Cache Tag

P PACKAGE
300 MIL PLASTIC
CASE 710A

NJ PACKAGE
300 MIL SOJ
CASE 810B

PIN ASSIGNMENT

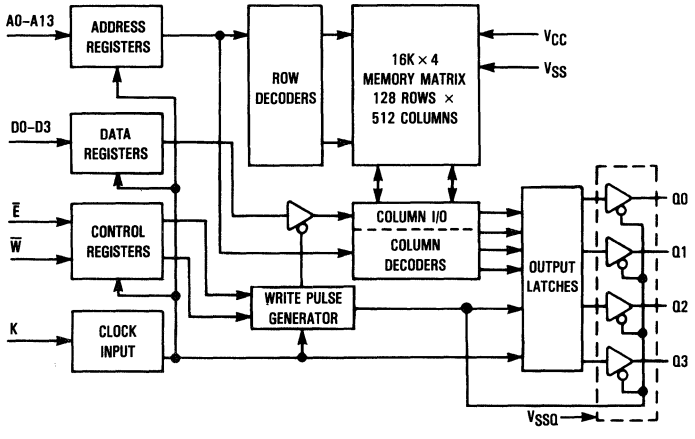


*For proper operation of the device, both V_{SS} and V_{SSQ} must be connected to ground.

PIN NAMES

A0-A13	Address Inputs
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
D0-D3	Data Inputs
Q0-Q3	Data Outputs
K	Clock Input
V_{CC}	+5 V Power Supply
V_{SS}	Ground
V_{SSQ}	Output Buffer Ground

BLOCK DIAGRAM



9

TRUTH TABLE

$\overline{E}$	$\overline{W}$	Operation	Q0-Q3
L	L	Write	High Z
L	H	Read	D_{out}
H	X	Not Selected	High Z

NOTE: The values of $\overline{E}$ and $\overline{W}$ are valid inputs for the setup and hold times relative to the K rising edge.

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to $V_{SS}=V_{SSQ}=0$ V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS}/V_{SSQ} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC}+0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation ($T_A=25°C$)	P_D	1.0	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for ALL rising edges of clock (K) while the device is selected.

This device contains circuitry that will ensure the output devices are in High Z at power up. Care should be taken by the user to ensure that all clocks are at V_{IL} or V_{IH} during power up to prevent spurious read cycles from occurring.

DC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{CC}=5.0$ V ±10%, $T_A=0$ to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to $V_{SS}=V_{SSQ}=0$ V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	–	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	−0.5*	–	0.8	V

*V_{IL} (min) = −0.5 V dc; V_{IL} (min) = −3.0 V ac (pulse width ≤20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, $V_{in}=0$ to V_{CC})	$I_{lkg(I)}$	–	±1.0	μA
Output Leakage Current ($\overline{E}=V_{IH}$, $V_{out}=0$ to V_{CC}, Outputs must be high-Z)	$I_{lkg(O)}$	–	±1.0	μA
AC Supply Current ($\overline{E}=V_{IL}$, $I_{out}=0$ mA, All Inputs = V_{IL} or V_{IH}, Cycle Time ≥ t_{KHKH} min)	I_{CCA}	–	140	mA
Standby Current ($\overline{E}=V_{IH}$; Other Inputs = V_{IH} ≥3.0 V or V_{IL} ≤0.4 V; $I_{out}=0$ mA, Cycle Time ≥ t_{KHKH} min)	I_{SB1}	–	55	mA
Output Low Voltage ($I_{OL}=12.0$ mA)	V_{OL}	–	0.4	V
Output High Voltage ($I_{OH}=-10.0$ mA)	V_{OH}	2.4	–	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, $T_A=25°C$, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	4	6	pF
Output Capacitance	C_{out}	7	10	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC}=5.0 V ±10%, T_A=0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . .0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns

Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load. . . . . .See Figure 1A Unless Otherwise Noted

READ CYCLE (See Note 1)

Parameter	Symbol	MCM6292-25		MCM6292-30		Unit	Notes
		Min	Max	Min	Max		
Read Cycle Time	t_{KHKH}	25	–	30	–	ns	2
Clock Access Time	t_{KHQV}	–	25	–	30	ns	4, 6
Data Valid from Clock Low	t_{KLQV}	–	10	–	13	ns	5, 6
Output Hold from Clock Low	t_{KLQX}	0	–	0	–	ns	3, 6
Clock Low to Q High Z ($\overline{E}$=V_{IH})	t_{KLQZ}	–	10	–	13	ns	3, 6
Clock Low Pulse Width	t_{KLKH}	5	–	5	–	ns	
Clock High Pulse Width	t_{KHKL}	5	–	5	–	ns	
Setup Times for: $\overline{E}$	t_{EVKH}	5	–	5	–	ns	7
A	t_{AVKH}						
$\overline{W}$	t_{WHKH}						
Hold Times for: $\overline{E}$	t_{KHEX}	3	–	3	–	ns	7
A	t_{KHAX}						
$\overline{W}$	t_{KHWX}						

NOTES:
1. A read is defined by $\overline{W}$ high and $\overline{E}$ low for the setup and hold times.
2. All read cycle timing is referenced from K.
3. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B. This parameter is sampled not 100% tested.
4. For Read Cycle 1 timing, clock high pulse width $<(t_{KHQV}-t_{KLQV})$.
5. For Read Cycle 2 timing, clock high pulse width $\geq(t_{KHQV}-t_{KLQV})$.
6. K must be at a low level for outputs to transition.
7. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for **ALL** rising edges of clock (K) while the device is selected.

9

AC TEST LOADS

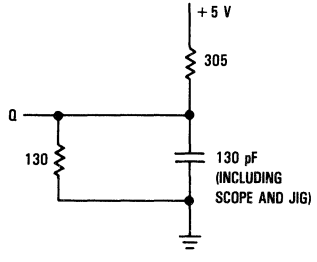


Figure 1A

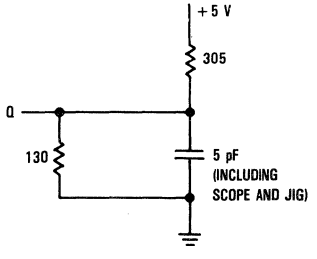
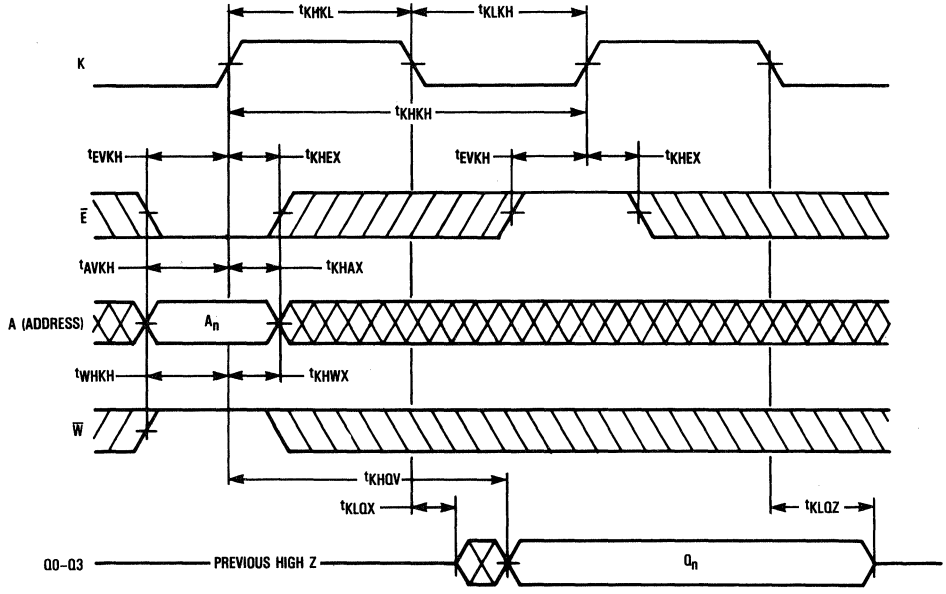
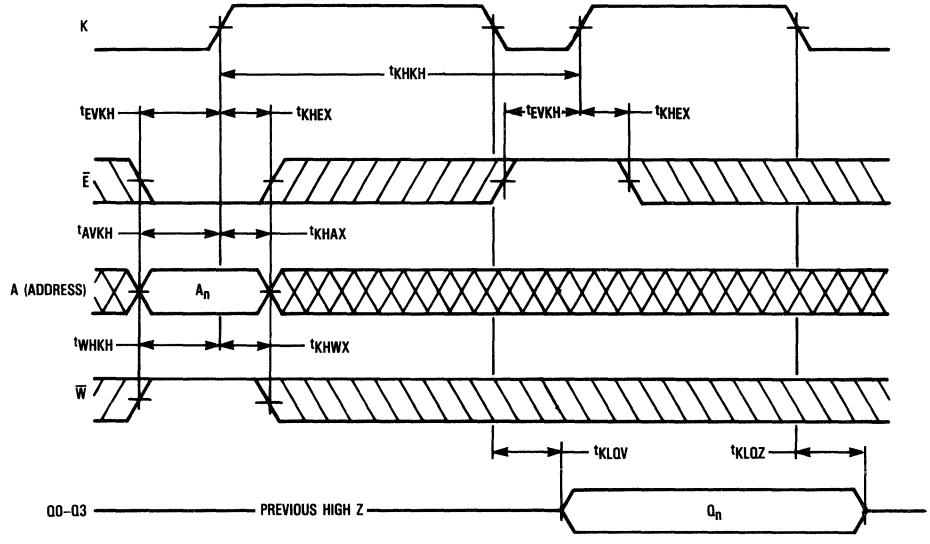


Figure 1B

READ CYCLE 1 (See Note 1)



READ CYCLE 2 (See Note 2)

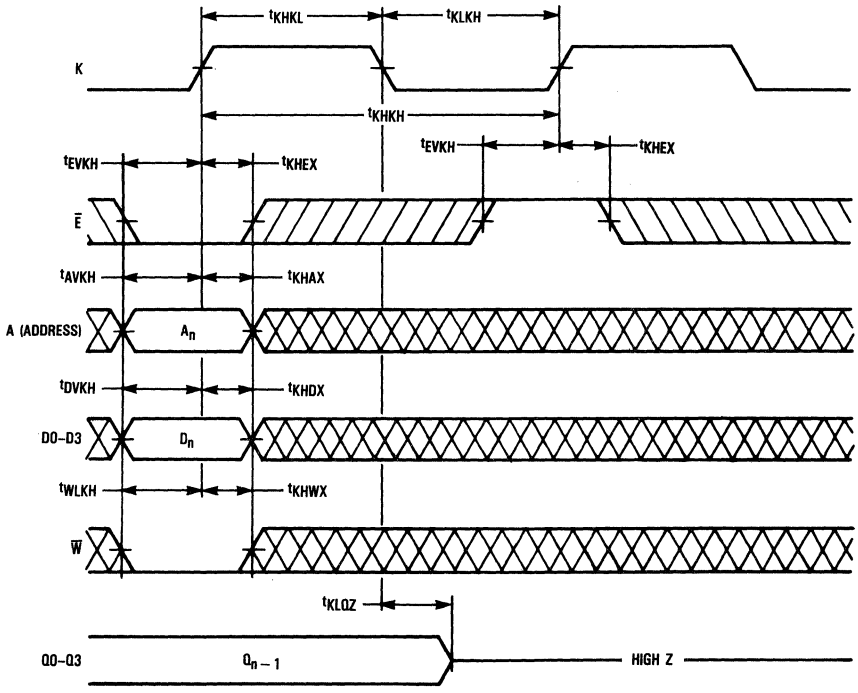


NOTES:
1. For Read Cycle 1 timing, clock high pulse width $<(t_{KHQV} - t_{KLQV})$.
2. For Read Cycle 2 timing, clock high pulse width $\geq(t_{KHQV} - t_{KLQV})$.

WRITE CYCLE ($\overline{W}$ Controlled, See Note 1)

Parameter		Symbol	MCM6292-25		MCM6292-30		Unit	Notes
			Min	Max	Min	Max		
Write Cycle Time		t_{KHKH}	25	—	30	—	ns	2
Clock Low to Output High Z		t_{KLQZ}	—	10	—	13	ns	3
Setup Times for:	$\overline{E}$	t_{EVKH}	5	—	5	—	ns	4
	A	t_{AVKH}						
	$\overline{W}$	t_{WLKH}						
	D	t_{DVKH}						
Hold Times for:	$\overline{E}$	t_{KHEX}	3	—	3	—	ns	4
	A	t_{KHAX}						
	$\overline{W}$	t_{KHWX}						
	D	t_{KHDX}						

NOTES:
1. A write is performed when $\overline{W}$ and $\overline{E}$ are both low for the specified setup and hold times.
2. All write cycle timing is referenced from K.
3. K must be at a low level for outputs to transition.
4. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for **ALL** rising edges of clock (K) while the device is selected.



9

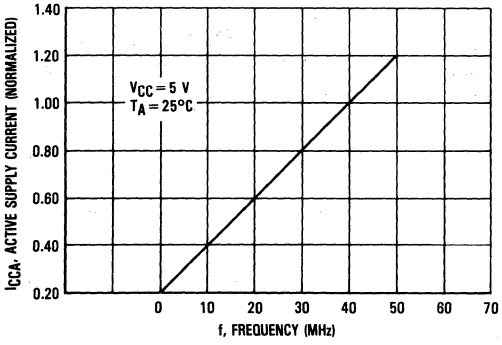


Figure 2. Active Supply Current versus Frequency

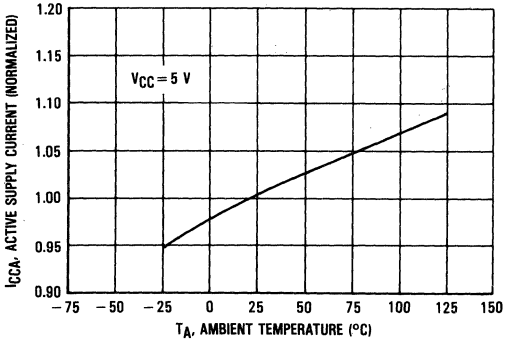


Figure 3. Active Supply Current versus Temperature

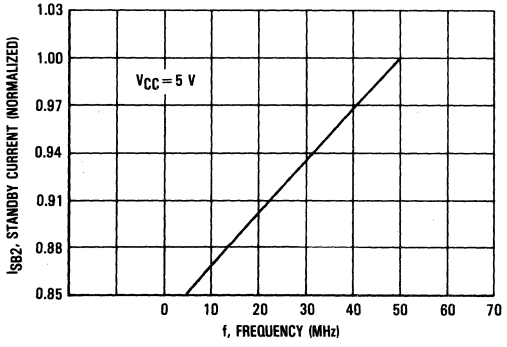


Figure 4. Standby Current versus Frequency

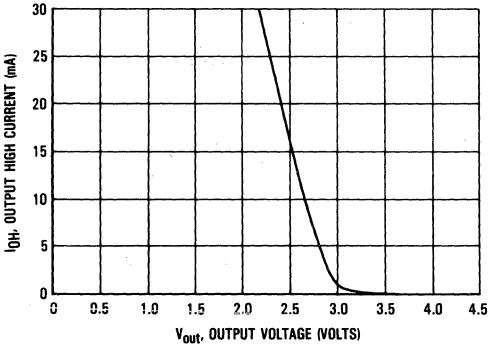


Figure 5. Output Source Current versus Output Voltage

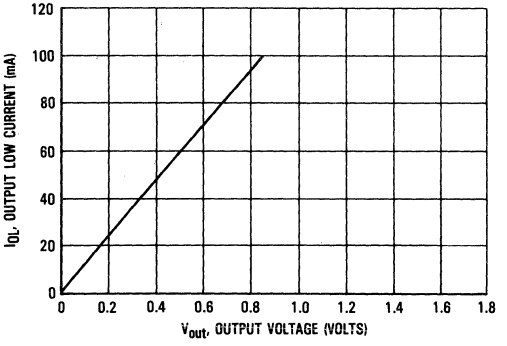


Figure 6. Output Sink Current versus Output Voltage

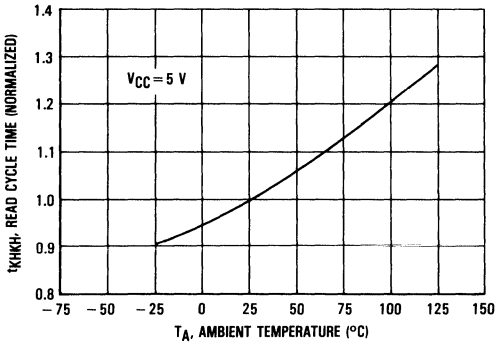


Figure 7. Read Cycle Time versus Temperature

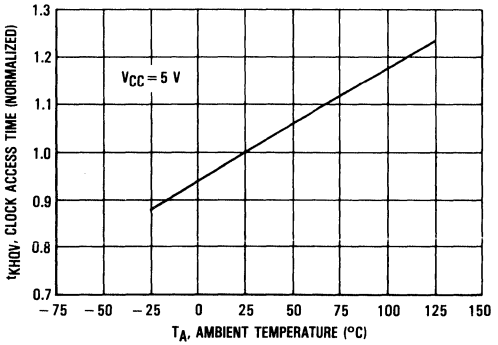


Figure 8. Clock Access Time versus Temperature

ORDERING INFORMATION
(Order by Full Part Number)

MCM 6292 X XX XX

- MCM — Motorola Memory Prefix
- 6292 — Part Number
- X — Package (P = Plastic DIP, NJ = Plastic SOJ)
- XX — Speed (25 = 25 ns, 30 = 30 ns)
- XX — Shipping Method (R2 = Tape & Reel, Blank = Rails)

Full Part Numbers — MCM6292P25, MCM6292P30, MCM6292NJ25, MCM6292NJ30, MCM6292NJ25R2, MCM6292NJ30R2

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APPLICATIONS INFORMATION

The Motorola family of synchronous SRAMs is designed to provide a performance and parts count advantage in applications such as writeable control stores, memory mapping, and cache memory. The on-board input registers eliminate the need for external latch chips in systems where addresses and data are not on the bus long enough to satisfy standard SRAM setup and hold times. Latches on the output port provide extended hold times independent of address or other device input changes to better meet system access requirements. The clock (K) input controls the operation of the input registers and output latches, and provides a direct means of synchronizing the SRAM to a system clock.

The MCM6292 offers transparent output operation, which allows output data access within the same t_{KHKH} cycle. This feature lends itself well to applications requiring RAM data to be set up on the system bus prior to the next rising clock edge. On the rising edge of the clock (K) signal, the output data for the previous cycle is latched until the next falling clock edge. When the clock (K) signal is low, the output is allowed to transition relative to the most recent rising clock (K) edge.

Figure 9 shows a typical system configuration using four MCM6292 chips. The system addresses are tied to the MCM6292s in parallel, while system data is distributed among the four input data ports of 4 bits each. Output data is tied to a separate output data bus to exploit the separate I/O configuration of the MCM6292. The clock (K) signal is a logical derivation of the system clock.

Figure 10 shows typical bus timing for the configuration of Figure 9. The system bus supplies address, data, and control signals, while accepting data from the memory on rising clock edges. In some applications, the clock (K) signal may need to be a delayed system clock to allow adequate address and data setup times.

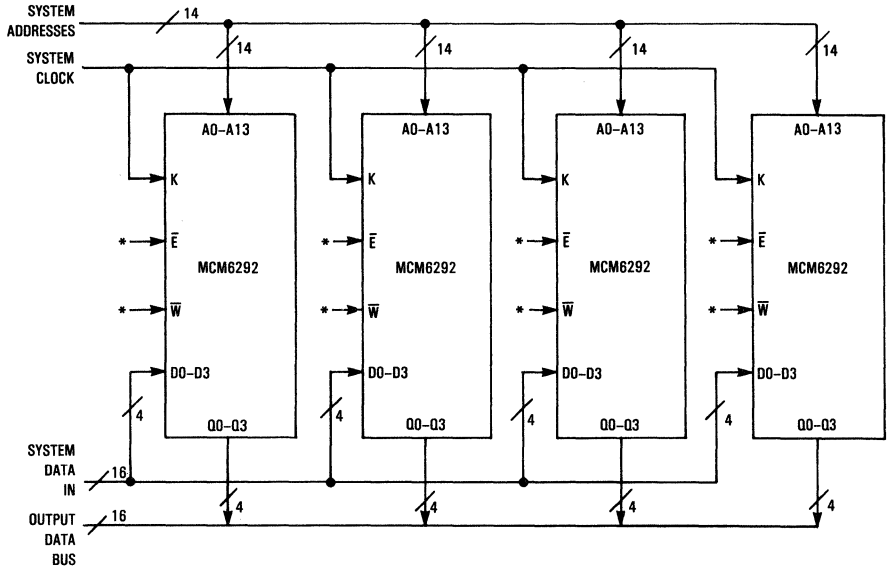
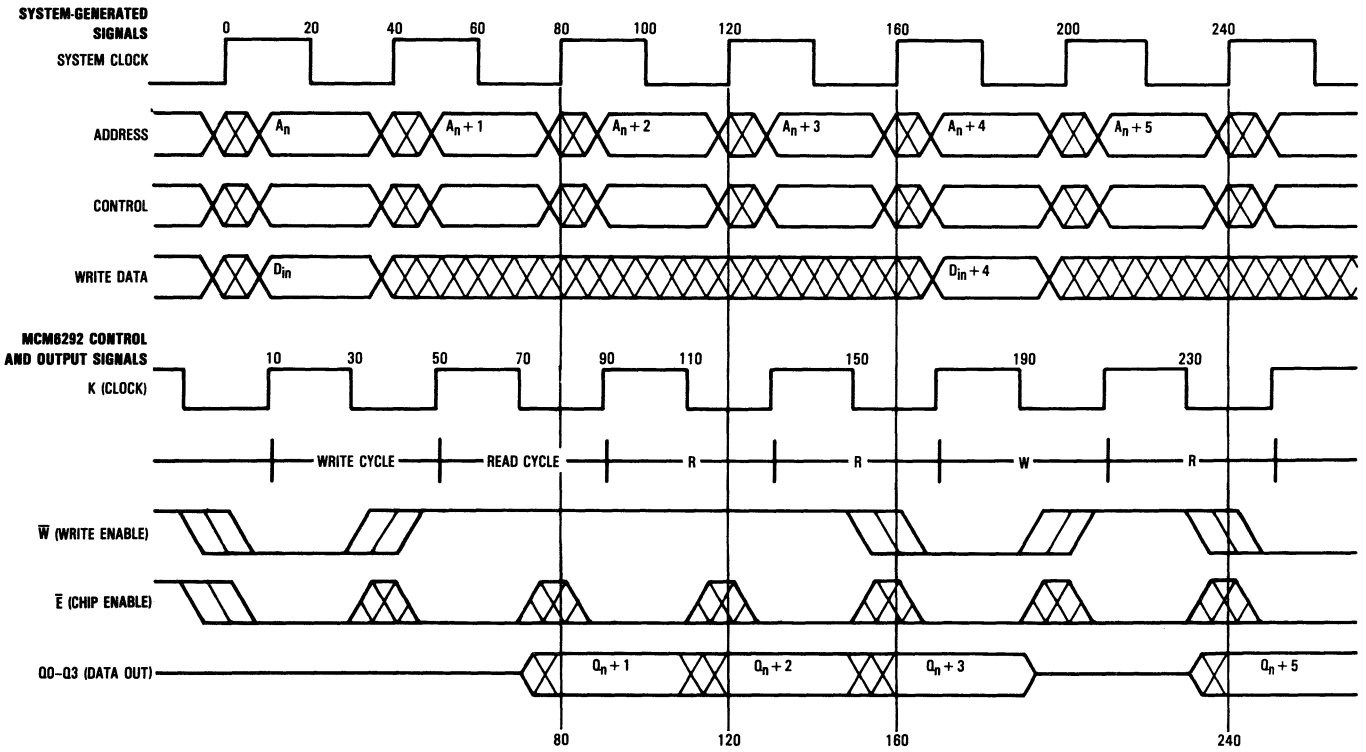


Figure 9. Typical Configuration for a 16-Bit Bus



NOTES:
1. The system supplies address, data, and control information and accepts data from memory on the rising edge of the system clock.
2. The memory clock is delayed 10 ns (for this example) to allow input information to propagate to the memory chips.

Figure 10. Nonpipeline System Timing

MCM6293

16K x 4 Bit Synchronous Static RAM
with Output Registers

P PACKAGE
300 MIL PLASTIC
CASE 710A

NJ PACKAGE
300 MIL SOJ
CASE 810B

The MCM6293 is a 65,536 bit synchronous static random access memory organized as 16,384 words of 4 bits, fabricated using Motorola's second-generation high-performance silicon-gate CMOS (HCMOS III) technology. The device integrates input registers, high speed SRAM, and high-drive capability output registers onto a single monolithic circuit for reduced parts count implementation of cache data RAM and writeable control store applications. It is well suited for telecommunications switches and test equipment.

Synchronous design allows precise cycle control with the use of an external clock (K), while CMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

The address (A0-A13), data (D0-D3), write ($\overline{W}$), and chip enable ($\overline{E}$) inputs are all clock (K) controlled, positive-edge-triggered, noninverting registers.

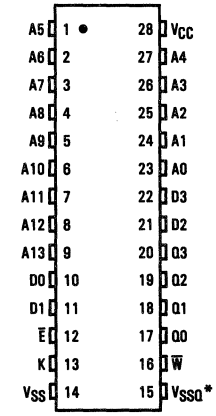
The MCM6293 provides output register operation. At the rising edge of K, the RAM data from the previous K high cycle is presented. This function is well suited to fully pipelined applications.

Write operations are internally self-timed and initiated by the rising edge of the K input. This feature eliminates complex off-chip write pulse generation and provides increased flexibility for incoming signals.

The MCM6293 is available in a 300-mil, 28-pin plastic DIP as well as a 300-mil, 28-pin plastic SOJ package.

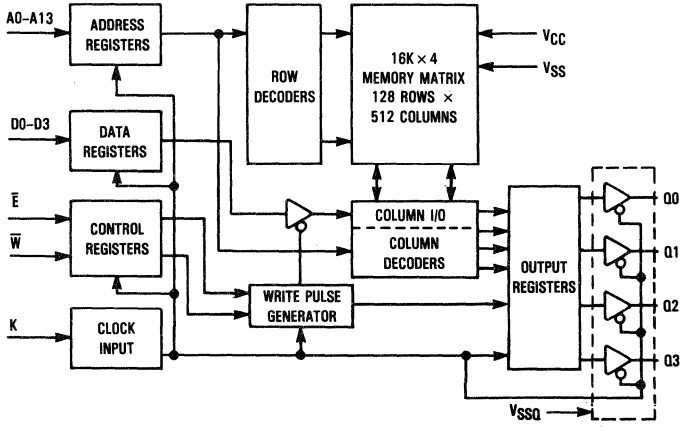
- Single 5 V ±10% Power Supply
- Fast Cycle Times: 20/25 ns Max
- Fast Clock (K) Access Times: 10 ns Max
- Address, Data Input, $\overline{E}$, and $\overline{W}$ Registers On-Chip
- Output Registers for Fully Pipelined Applications
- High Output Drive Capability
- Internally Self-Timed Write Pulse Generation
- Separate Data Input and Data Output Pins
- High Board Density SOJ Package Available
- Typical Applications: General-Purpose Buffer Storage, Writeable Control Store, Data Cache, or Cache Tag

PIN ASSIGNMENT



*For proper operation of the device, both V_{SS} and V_{SSQ} must be conected to ground.

BLOCK DIAGRAM



PIN NAMES

A0-A13	Address Inputs
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
D0-D3	Data Inputs
Q0-Q3	Data Outputs
K	Clock Input
V_{CC}	+5 V Power Supply
V_{SS}	Ground
V_{SSQ}	Output Buffer Ground

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TRUTH TABLE

$\overline{E}$	$\overline{W}$	Operation	Q0-Q3
L	L	Write	High Z
L	H	Read	D_{out}
H	X	Not Selected	High Z

NOTE: The values of $\overline{E}$ and $\overline{W}$ are valid inputs for the setup and hold times relative to the K rising edge.

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to $V_{SS} = V_{SSQ} = 0$ V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS}/V_{SSQ} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC} +0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation (T_A = 25°C)	P_D	1.0	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for **ALL** rising edges of clock (K) while the device is selected.

This device contains circuitry that will ensure the output devices are in High Z at power up. Care should be taken by the user to ensure that all clocks are at V_{IL} or V_{IH} during power up to prevent spurious read cycles from occurring.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to $V_{SS} = V_{SSQ} = 0$ V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} +0.3	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

*V_{IL} (min) = −0.5 V dc; V_{IL} (min) = −3.0 V ac (pulse width ≤20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	±1.0	μA
Output Leakage Current ($\overline{E} = V_{IH}$, V_{out} = 0 to V_{CC}, Outputs must be high-Z)	$I_{lkg(O)}$	—	±1.0	μA
AC Supply Current ($\overline{E} = V_{IL}$, I_{out} = 0 mA, All Inputs = V_{IH} or V_{IL}, Cycle Time ≥ t_{KHKH} min)	I_{CCA}	—	140	mA
Standby Current ($\overline{E} = V_{IH}$; Other Inputs = V_{IH} ≥3.0 V or V_{IL} ≤0.4 V; I_{out} = 0 mA, Cycle Time ≥ t_{KHKH} min)	I_{SB1}	—	55	mA
Output Low Voltage (I_{OL} = 12.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = −10.0 mA)	V_{OH}	2.4	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	4	6	pF
Output Capacitance	C_{out}	7	10	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . .0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns

Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load. . . . . .See Figure 1A Unless Otherwise Noted

READ CYCLE (See Note 1)

Parameter	Symbol	MCM6293-20		MCM6293-25		Unit	Notes
		Min	Max	Min	Max		
Read Cycle Time	t_{KHKH}	20	–	25	–	ns	2
Clock Access Time	t_{KHQV}	–	10	–	10	ns	3
Output Active from Clock High	t_{KHQX}	0	–	0	–	ns	4
Clock High to Q High Z ($\overline{E}=V_{IH}$)	t_{KHQZ}	–	10	–	10	ns	4
Clock Low Pulse Width	t_{KLKH}	5	–	5	–	ns	
Clock High Pulse Width	t_{KHKL}	5	–	5	–	ns	
Setup Times for: $\overline{E}$	t_{EVKH}	5	–	5	–	ns	5
A	t_{AVKH}						
$\overline{W}$	t_{WHKH}						
Hold Times for: $\overline{E}$	t_{KHEX}	3	–	3	–	ns	5
A	t_{KHAX}						
$\overline{W}$	t_{KHWX}						

NOTES:
1. A read is defined by $\overline{W}$ high and $\overline{E}$ low for the setup and hold times.
2. All read cycle timing is referenced from K.
3. Valid data from K high will be the data stored at the address of the last valid read cycle.
4. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B. This parameter is sampled not 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQX} min for a given device.
5. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for **ALL** rising edges of clock (K) while the device is selected.

9

AC TEST LOADS

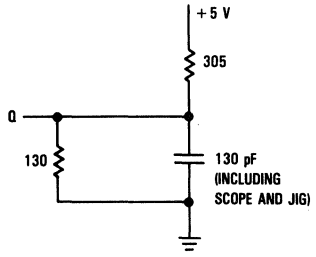


Figure 1A

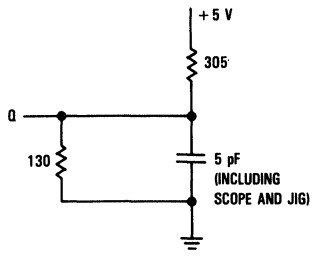
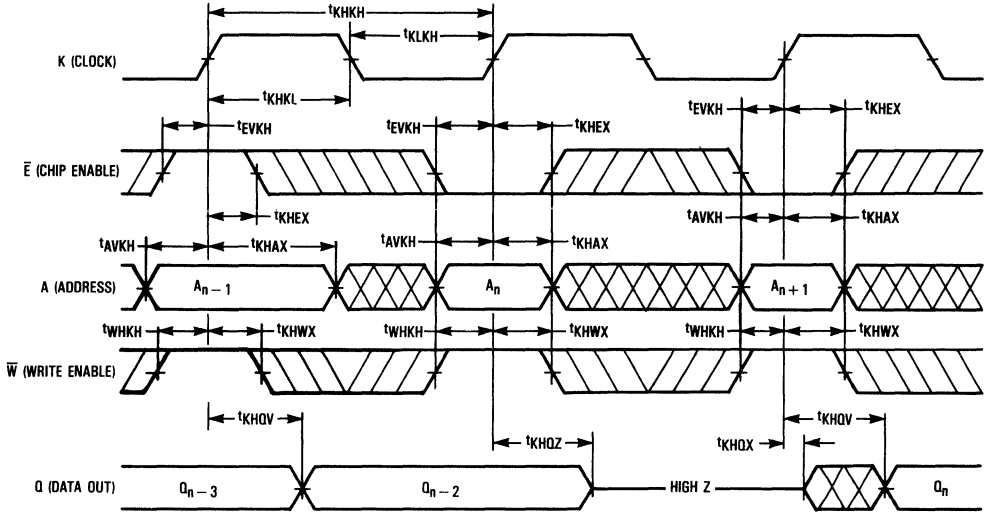
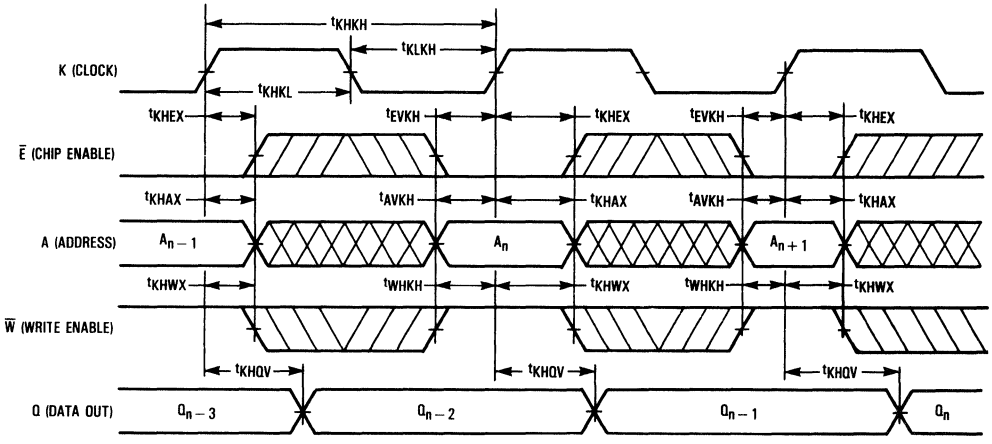


Figure 1B

READ CYCLE 1 (See Note 1)



READ CYCLE 2 (See Note 1)



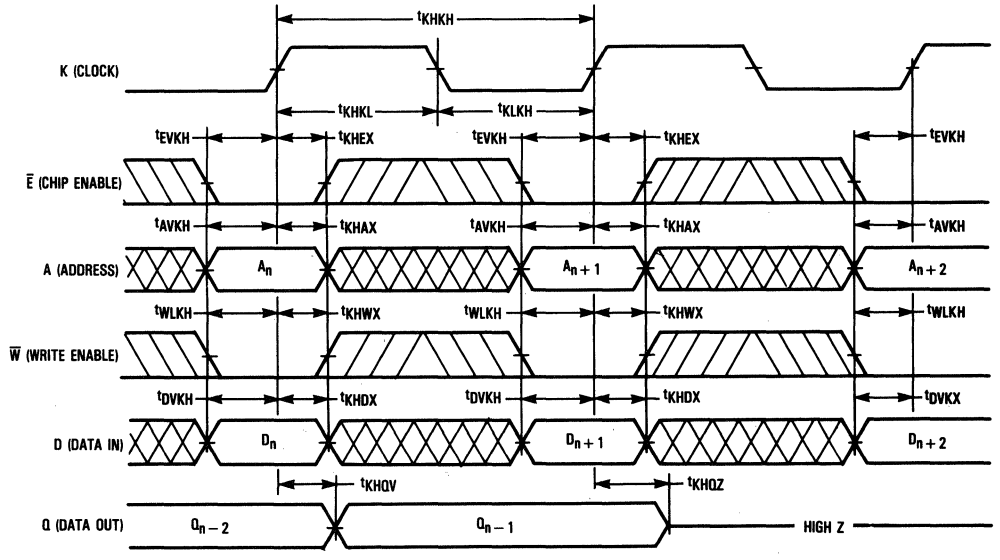
NOTE:
1. The outputs Q_{n-3} and Q_{n-2} are derived from two previous read cycles where $\overline{W} = V_{IH}$ and $\overline{E} = V_{IL}$ for those cycles.

WRITE CYCLE ($\overline{W}$ Controlled, See Note 1)

Parameter		Symbol	MCM6293-20		MCM6293-25		Unit	Notes
			Min	Max	Min	Max		
Write Cycle Time		t_{KHKH}	20	–	25	–	ns	2
Clock High to Output High Z ($\overline{W}=V_{IL}$)		t_{KHQZ}	–	10	–	10	ns	3
Setup Times for:	$\overline{E}$	t_{EVKH}	5	–	5	–	ns	4
	A	t_{AVKH}						
	$\overline{W}$	t_{WLKH}						
	D	t_{DVKH}						
Hold Times for:	$\overline{E}$	t_{KHEX}	3	–	3	–	ns	4
	A	t_{KHAX}						
	$\overline{W}$	t_{KHWX}						
	D	t_{KHDX}						

NOTES:
1. A write is performed when $\overline{W}$ and $\overline{E}$ are both low for the specified setup and hold times.
2. All write cycle timing is referenced from K.
3. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B. This parameter is sampled not 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQX} min for a given device.
4. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for **ALL** rising edges of clock (K) while the device is selected.

WRITE CYCLE



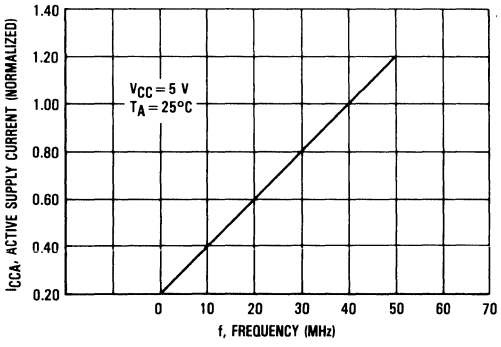


Figure 2. Active Supply Current versus Frequency

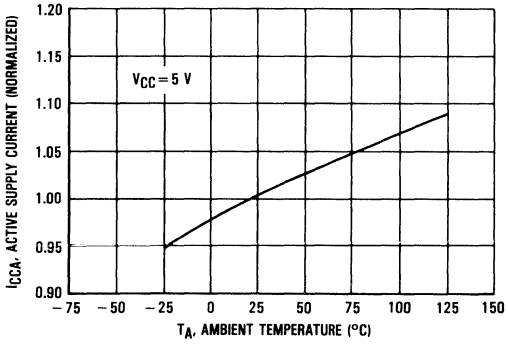


Figure 3. Active Supply Current versus Temperature

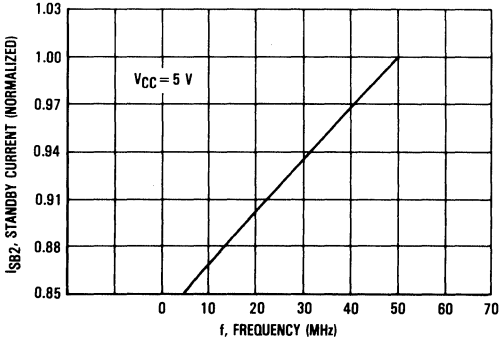


Figure 4. Standby Current versus Frequency

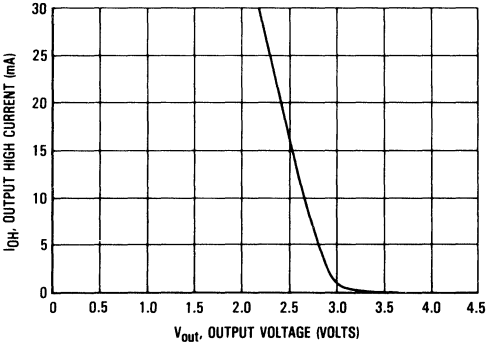


Figure 5. Output Source Current versus Output Voltage

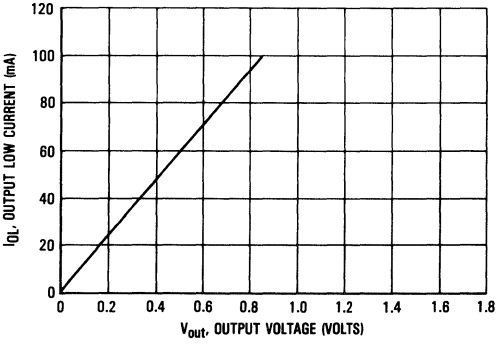


Figure 6. Output Sink Current versus Output Voltage

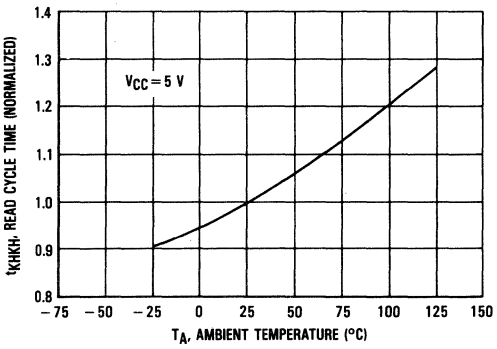


Figure 7. Read Cycle Time versus Temperature

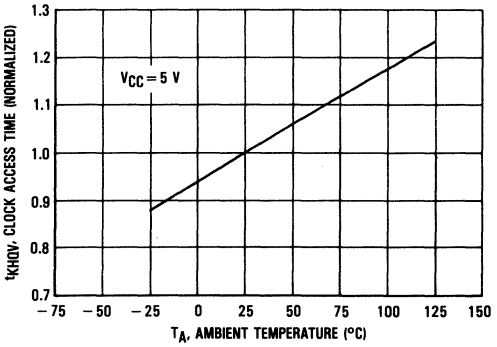


Figure 8. Clock Access Time versus Temperature

ORDERING INFORMATION
(Order by Full Part Number)

MCM 6293 X XX XX

Motorola Memory Prefix

Part Number

Shipping Method (R2 = Tape & Reel, Blank = Rails)

Speed (20 = 20 ns, 25 = 25 ns)

Package (P = Plastic DIP, NJ = 300 mil SOJ)

Full Part Numbers—	MCM6293P20	MCM6293NJ20	MCM6293NJ20R2
	MCM6293P25	MCM6293NJ25	MCM6293NJ25R2

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APPLICATIONS INFORMATION

The Motorola family of synchronous SRAMs is designed to provide a performance and parts count advantage in applications such as writeable control stores, memory mapping, and cache memory. The on-board input registers eliminate the need for external latch chips in systems where addresses and data are not on the bus long enough to satisfy standard SRAM setup and hold times. Registers on the output port provide extended hold times independent of address or other device input changes to better meet system access requirements. The clock (K) input controls the operation of the input registers and output registers, and provides a direct means of synchronizing the SRAM to a system clock.

The MCM6293 offers registered output operation. On the rising edge of the clock (K) signal, the output data for the previous cycle is latched until the next rising clock edge.

Figure 9 shows a typical system configuration using four MCM6293 chips. The system addresses are tied to the MCM6293s in parallel, while system data is distributed among the four input data ports of 4 bits each. Output data is tied to a separate output data bus to exploit the separate I/O configuration of the MCM6293. The clock (K) signal is a logical derivation of the system clock.

Figure 10 shows typical bus timing for the configuration of Figure 9. The system bus supplies address, data, and control signals, while accepting data from the memory on rising clock edges. In some applications, the clock (K) signal may need to be a delayed system clock to allow adequate address and data setup times.

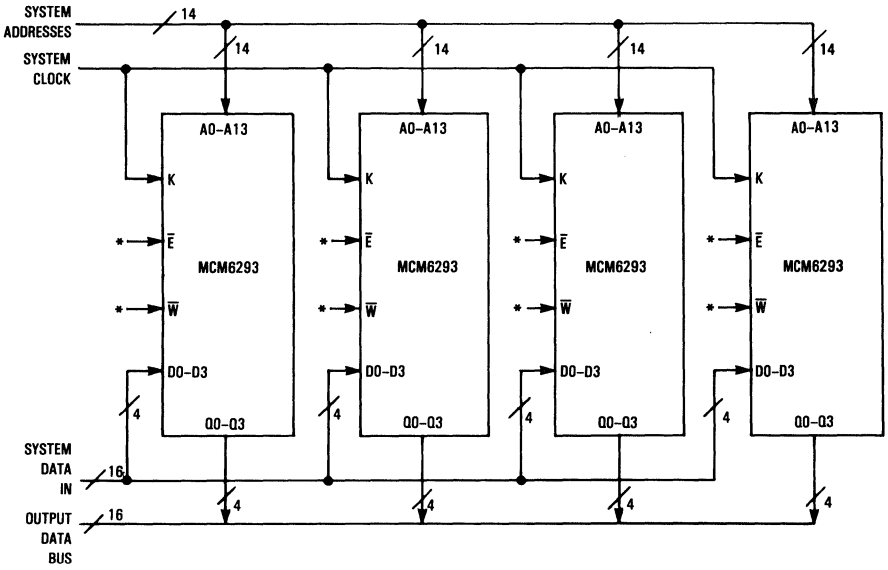
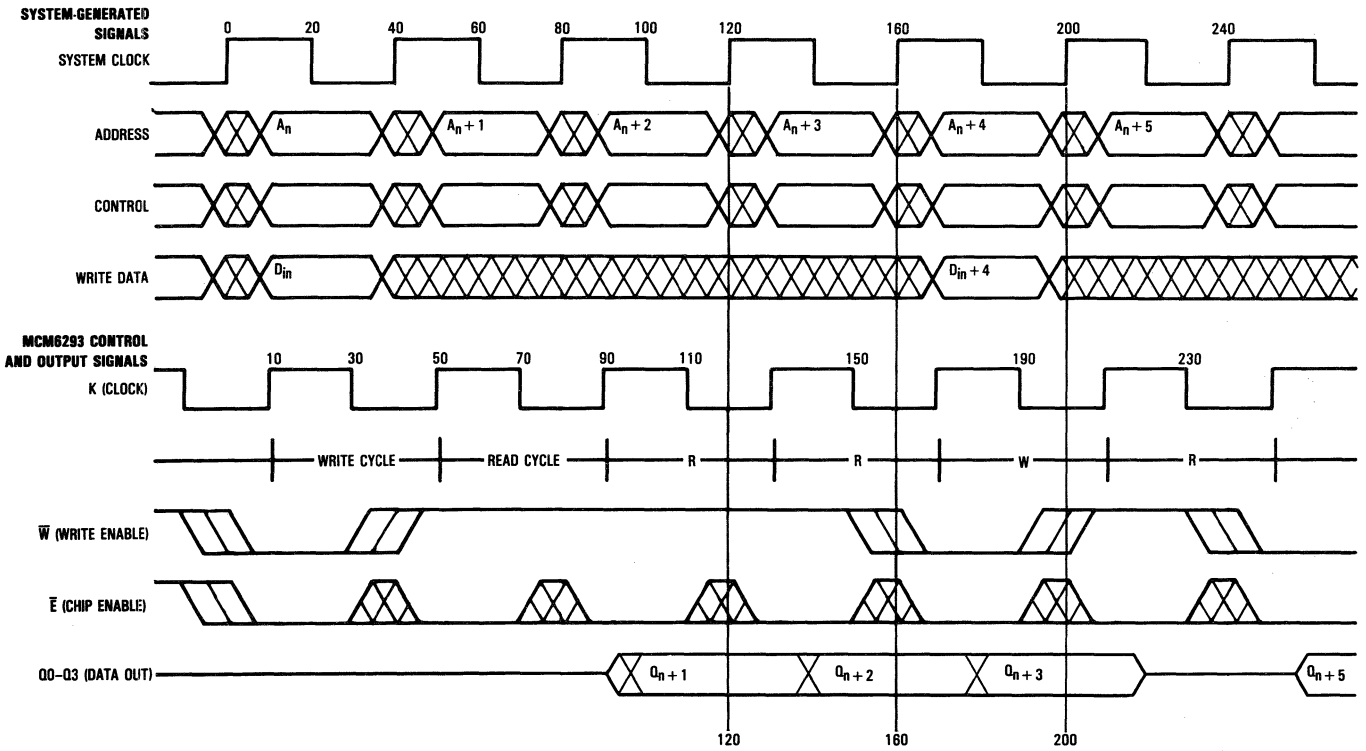


Figure 9. Typical Configuration for a 16-Bit Bus



NOTES:
1. The system supplies address, data, and control information and accepts data from memory on the rising edge of the system clock.
2. The memory clock is delayed 10 ns (for this example) to allow input information to propagate to the memory chips.

Figure 10. Pipeline System Timing

MCM6294

16K x 4 Bit Synchronous Static RAM
with Output Registers and Output Enable

The MCM6294 is a 65,536 bit synchronous static random access memory organized as 16,384 words of 4 bits, fabricated using Motorola's second-generation high-performance silicon-gate CMOS (HCMOS III) technology. The device integrates input registers, high speed SRAM, and high-drive capability output registers onto a single monolithic circuit for reduced parts count implementation of cache data RAM and writeable control store applications. Synchronous design allows precise cycle control with the use of an external clock (K), while CMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability. It is well suited for telecommunications switches and test equipment.

The address (A0-A13), data (D0-D3), and write ($\overline{W}$) inputs are all clock (K) controlled, positive-edge-triggered, noninverting registers.

The MCM6294 provides output register operation. At the rising edge of K, the RAM data from the previous K high cycle is presented. This function is well suited to fully pipelined applications.

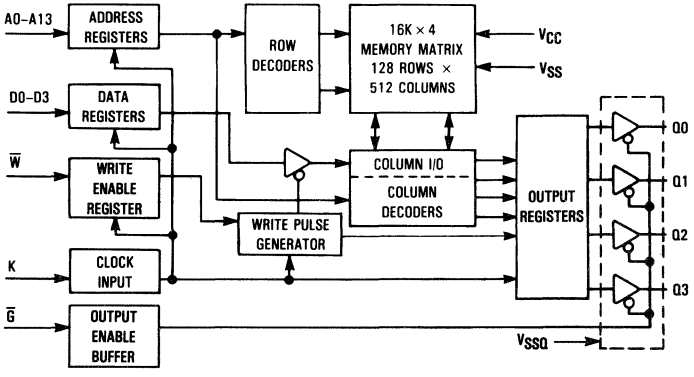
The output enable ($\overline{G}$) provides asynchronous bus control for common I/O or bank switch applications.

Write operations are internally self-timed and initiated by the rising edge of the K input. This feature eliminates complex off-chip write pulse generation and provides increased flexibility for incoming signals.

The MCM6294 is available in a 300-mil, 28-pin plastic DIP as well as a 300-mil, 28-pin plastic SOJ package.

- Single 5 V ±10% Power Supply
- Fast Cycle Times: 20/25 ns Max
- Fast Clock (K) Access Times: 10 ns Max
- Address, Data Input, and $\overline{W}$ Registers On-Chip
- Output Enable for Asynchronous Bus Control
- Output Registers for Fully Pipelined Applications
- High Output Drive Capability
- Internally Self-Timed Write Pulse Generation
- Separate Data Input and Data Output Pins
- High Board Density SOJ Package Available
- Typical Applications: General-Purpose Buffer Storage, Writeable Control Store, Data Cache, or Cache Tag

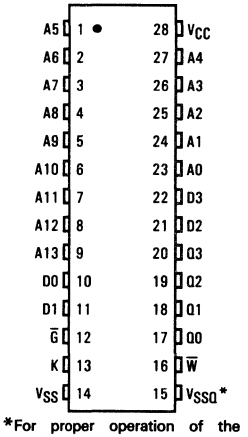
BLOCK DIAGRAM



P PACKAGE
300 MIL PLASTIC
CASE 710A

NJ PACKAGE
300 MIL SOJ
CASE 810B

PIN ASSIGNMENT



*For proper operation of the device, both V_{SS} and V_{SSQ} must be connected to ground.

PIN NAMES

A0-A13	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
D0-D3	Data Inputs
Q0-Q3	Data Outputs
K	Clock Input
V_{CC}	+5 V Power Supply
V_{SS}	Ground
V_{SSQ}	Output Buffer Ground

9

TRUTH TABLE

$\overline{G}$	$\overline{W}$	Operation	Q0-Q3
X	L	Write	High Z
L	H	Read	D_{out}
H	H	Output Disable	High Z

NOTE: The value $\overline{W}$ is a valid input for the setup and hold times relative to the K rising edge. The value $\overline{G}$ is an asynchronous input.

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to $V_{SS} = V_{SSQ} = 0$ V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS}/V_{SSQ} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC} +0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation (T_A = 25°C)	P_D	1.0	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for **ALL** rising edges of clock (K) while the device is selected.

This device contains circuitry that will ensure the output devices are in High Z at power up. Care should be taken by the user to ensure that all clocks are at V_{IL} or V_{IH} during power up to prevent spurious read cycles from occurring.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to $V_{SS} = V_{SSQ} = 0$ V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	–	V_{CC} +0.3	V
Input Low Voltage	V_{IL}	−0.5*	–	0.8	V

*V_{IL} (min) = −0.5 V dc; V_{IL} (min) = −3.0 V ac (pulse width ≤20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, $V_{in} = 0$ to V_{CC})	$I_{lkg(I)}$	–	±1.0	μA
Output Leakage Current ($\overline{G} = V_{IH}$, $V_{out} = 0$ to V_{CC}, Outputs must be high-Z)	$I_{lkg(O)}$	–	±1.0	μA
AC Supply Current ($\overline{G} = V_{IL}$, $I_{out} = 0$ mA, Cycle Time = t_{KHKH} min)	I_{CCA}	–	140	mA
Output Low Voltage (I_{OL} = 12.0 mA)	V_{OL}	–	0.4	V
Output High Voltage (I_{OH} = −10.0 mA)	V_{OH}	2.4	–	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	4	6	pF
Output Capacitance	C_{out}	7	10	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . .0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns

Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load. . . . . .See Figure 1A Unless Otherwise Noted

READ CYCLE (See Note 1)

Parameter		Symbol	MCM6294-20		MCM6294-25		Unit	Notes
			Min	Max	Min	Max		
Read Cycle Time		t_{KHKH}	20	–	25	–	ns	2
Clock Access Time		t_{KHQV}	–	10	–	10	ns	3
Output Active from Clock High		t_{KHQX}	0	–	0	–	ns	4
Clock Low Pulse Width		t_{KLKH}	5	–	5	–	ns	
Clock High Pulse Width		t_{KHKL}	5	–	5	–	ns	
Setup Times for:	A $\overline{W}$	t_{AVKH} t_{WHKH}	5	–	5	–	ns	5
Hold Times for:	A $\overline{W}$	t_{KHAX} t_{KHWX}	3	–	3	–	ns	5
$\overline{G}$ High to Q High Z		t_{GHQZ}	–	10	–	10	ns	4, 6
$\overline{G}$ Low to Q Active		t_{GLQX}	0	–	0	–	ns	4, 6
$\overline{G}$ Low to Q Valid		t_{GLQV}	–	10	–	10	ns	

NOTES:
1. A read is defined by $\overline{W}$ high for the setup and hold times.
2. All read cycle timing is referenced from K or from $\overline{G}$.
3. Valid data from K high will be the data stored at the address of the last valid read cycle.
4. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B. This parameter is sampled not 100% tested.
5. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for **ALL** rising edges of clock (K) while the device is selected.
6. At any given voltage and temperature, t_{GHQZ} max is less than t_{GLQX} min for a given device.

AC TEST LOADS

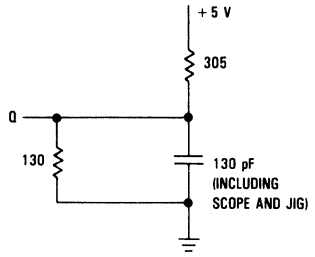


Figure 1A

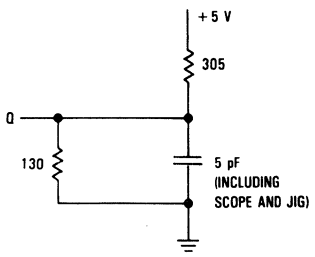
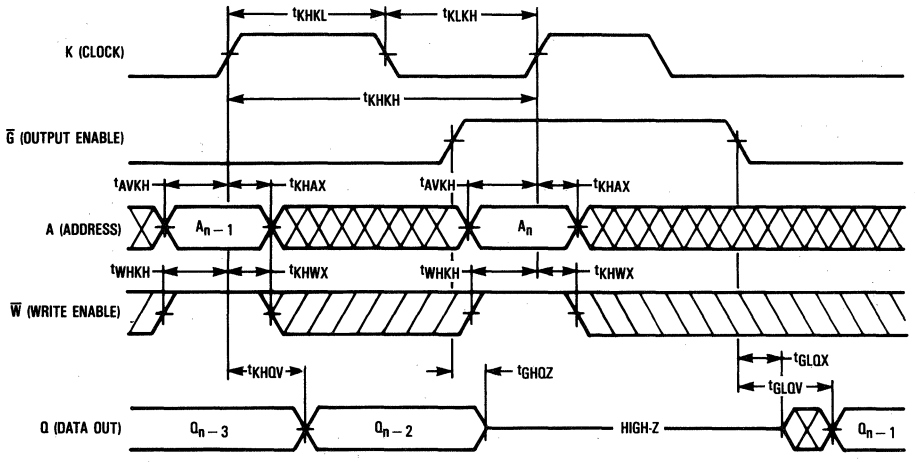
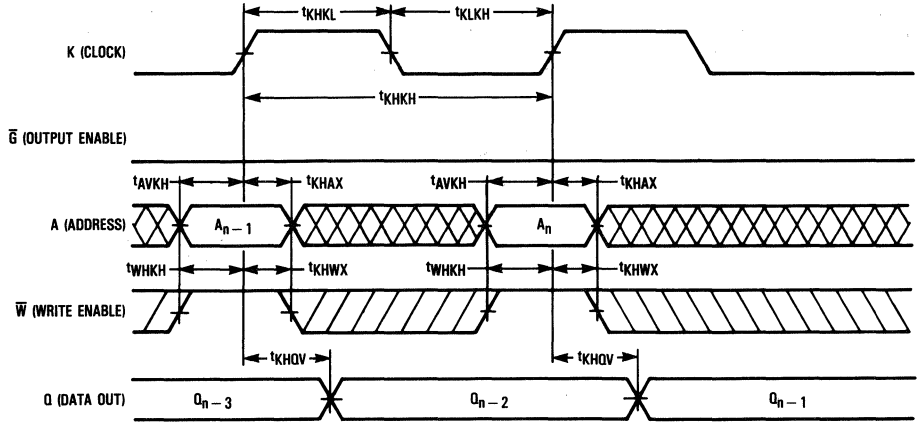


Figure 1B

READ CYCLE 1 (See Note 1)



READ CYCLE 2 (See Note 1)



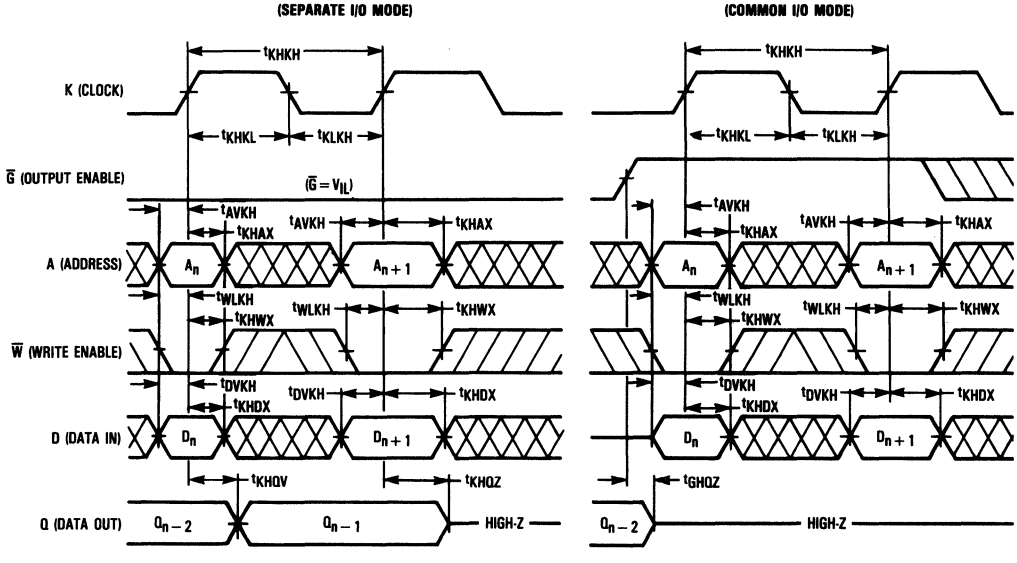
NOTE:
1. The outputs Q_{n-3} and Q_{n-2} are derived from two previous read cycles, where $\overline{W} = V_{IH}$ for those cycles.

WRITE CYCLE ($\overline{W}$ Controlled, See Note 1)

Parameter		Symbol	MCM6294-20		MCM6294-25		Unit	Notes
			Min	Max	Min	Max		
Write Cycle Time		t_{KHKH}	20	–	25	–	ns	2
Clock High to Output High Z ($\overline{W}=V_{IL}$)		t_{KHQZ}	–	10	–	10	ns	3
$\overline{G}$ High to Q High Z		t_{GHQZ}	–	10	–	10	ns	4
Setup Times for:	A	t_{AVKH}	5	–	5	–	ns	5
	$\overline{W}$	t_{WLKH}						
	D	t_{DVKH}						
Hold Times for:	A	t_{KHAX}	3	–	3	–	ns	5
	$\overline{W}$	t_{KHWX}						
	D	t_{KHDX}						

NOTES:
1. A write is performed when $\overline{W}$ is low for the specified setup and hold times.
2. All write cycle timing is referenced from K or from $\overline{G}$.
3. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQX} min for a given device.
4. $\overline{G}$ becomes a don't care signal for successive writes after the first write cycle.
5. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for ALL rising edges of clock (K) while the device is selected.

WRITE CYCLE 1



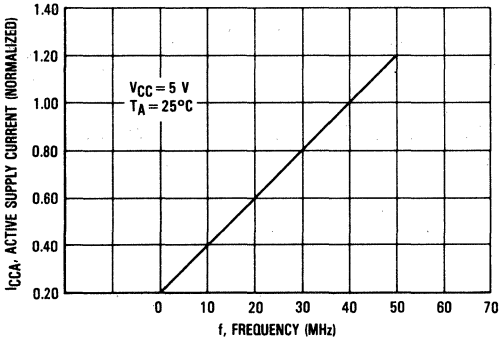


Figure 2. Active Supply Current versus Frequency

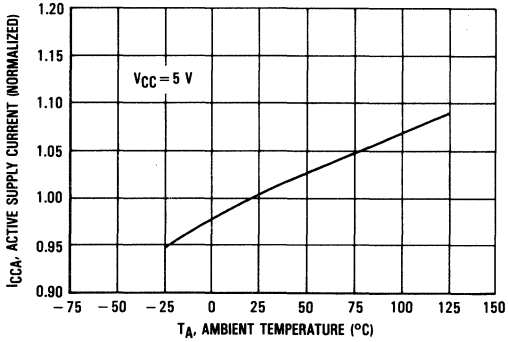


Figure 3. Active Supply Current versus Temperature

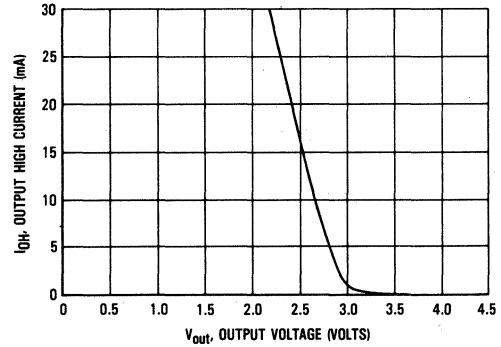


Figure 4. Output Source Current versus Output Voltage

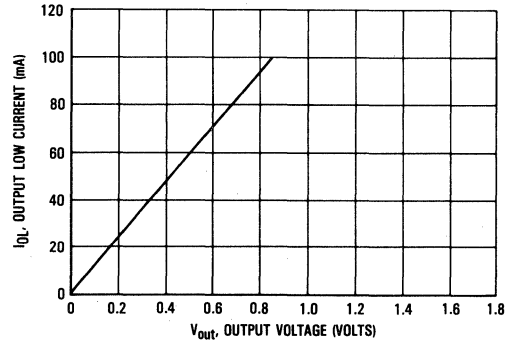


Figure 5. Output Sink Current versus Output Voltage

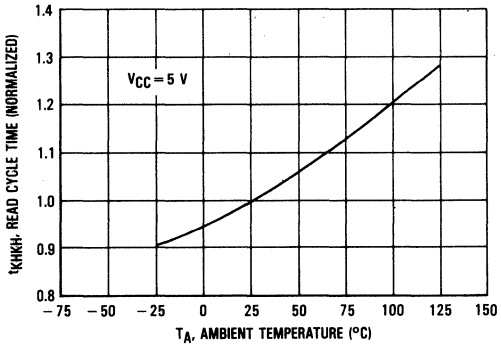


Figure 6. Read Cycle Time versus Temperature

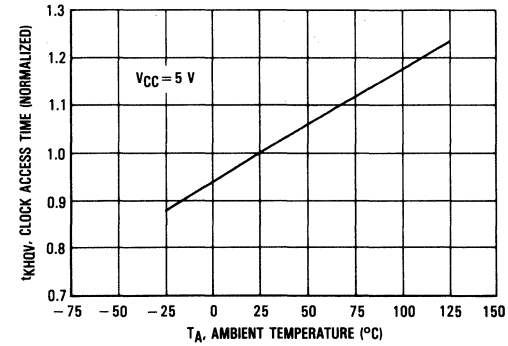


Figure 7. Clock Access Time versus Temperature

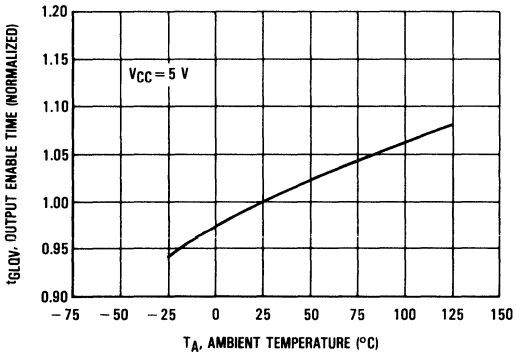


Figure 8. Output Enable Time versus Temperature

ORDERING INFORMATION
(Order by Full Part Number)

MCM 6294 X XX XX

- MCM — Motorola Memory Prefix
- 6294 — Part Number
- X — Package (P = Plastic DIP, NJ = 300 mil SOJ)
- XX — Speed (20 = 20 ns, 25 = 25 ns)
- XX — Shipping Method (R2 = Tape & Reel, Blank = Rails)

Full Part Numbers — MCM6294P20, MCM6294P25, MCM6294NJ20, MCM6294NJ25, MCM6294NJ20R2, MCM6294NJ25R2

9

APPLICATIONS INFORMATION

The Motorola family of synchronous SRAMs is designed to provide a performance and parts count advantage in applications such as writeable control stores, memory mapping, and cache memory. The on-board input registers eliminate the need for external latch chips in systems where addresses and data are not on the bus long enough to satisfy standard SRAM setup and hold times. Registers on the output port provide extended hold times independent of address or other device input changes to better meet system access requirements. The clock (K) input controls the operation of the input registers and output registers, and provides a direct means of synchronizing the SRAM to a system clock.

The MCM6294 offers registered output operation. On the rising edge of the clock (K) signal, the output data for the previous cycle is latched until the next rising clock edge.

Figure 9 shows a typical system configuration using four MCM6294 chips. The system addresses are tied to the MCM6294s in parallel, while system data is distributed among the four input data ports of 4 bits each. Output data is tied to a separate output data bus to exploit the separate I/O configuration of the MCM6294. The clock (K) signal is a logical derivation of the system clock.

Figure 10 shows typical bus timing for the configuration of Figure 9. The system bus supplies address, data, and control signals, while accepting data from the memory on rising clock edges. In some applications, the clock (K) signal may need to be a delayed system clock to allow adequate address and data setup times.

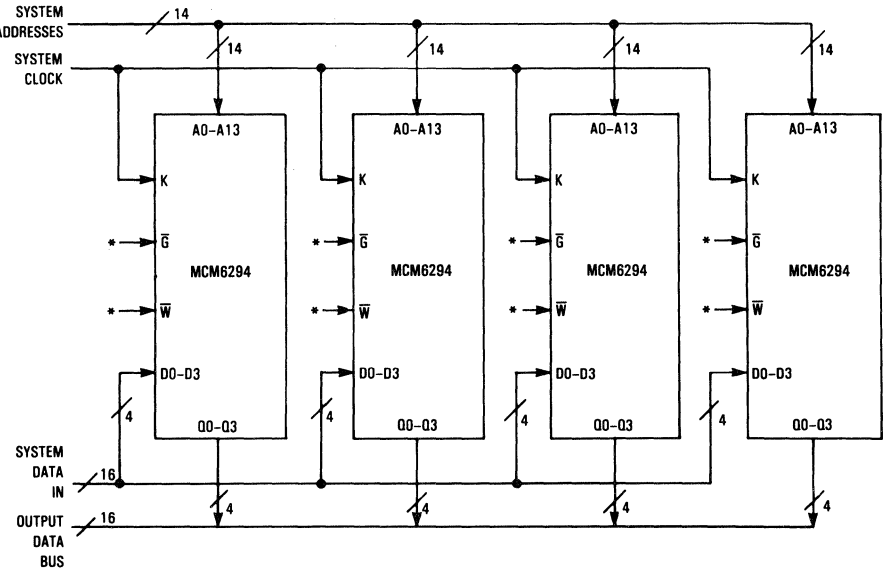
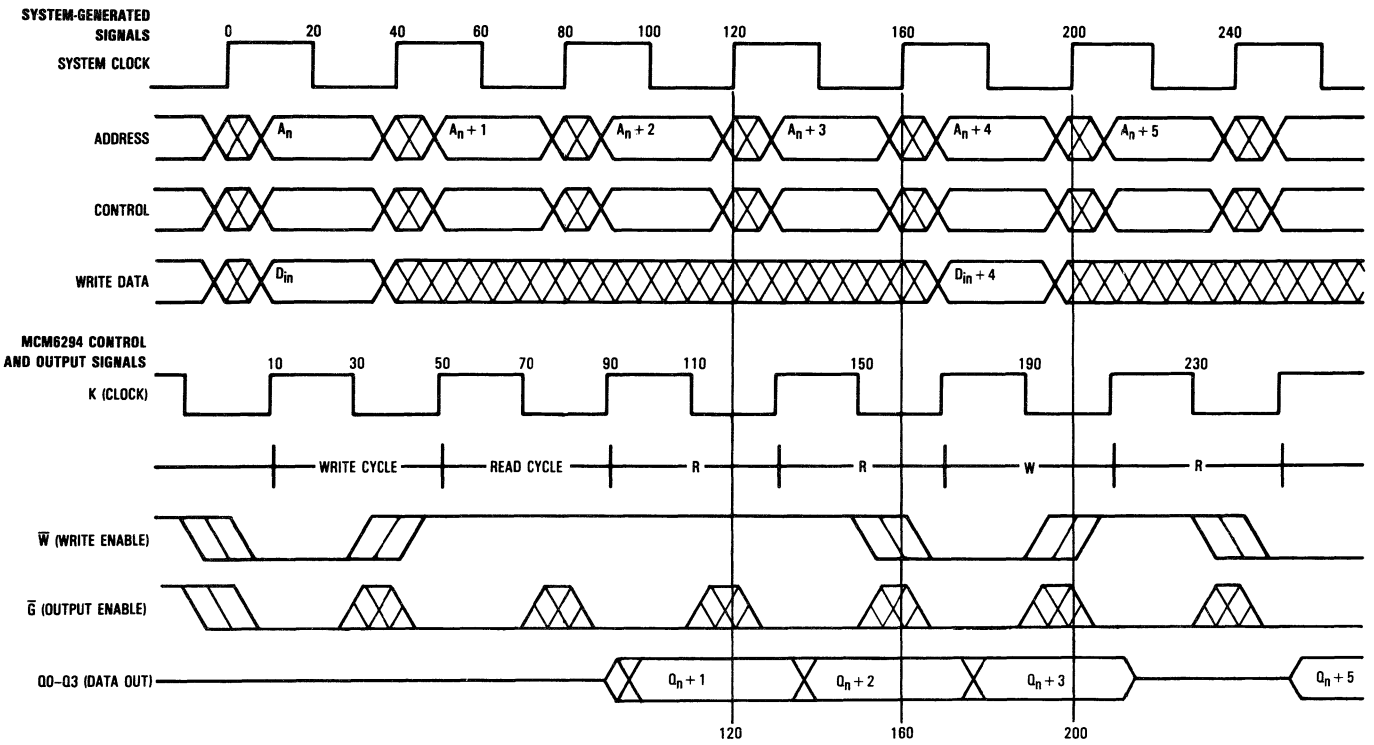


Figure 9. Typical Configuration for a 16-Bit Bus



NOTES:
1. The system supplies address, data, and control information and accepts data from memory on the rising edge of the system clock.
2. The memory clock is delayed 10 ns (for this example) to allow input information to propagate to the memory chips.

Figure 10. Pipeline System Timing

MCM6295

16K x 4 Bit Synchronous Static RAM
with Transparent Outputs and Output Enable

P PACKAGE
300 MIL PLASTIC
CASE 710A

NJ PACKAGE
300 MIL SOJ
CASE 810B

The MCM6295 is a 65,536 bit synchronous static random access memory organized as 16,384 words of 4 bits, fabricated using Motorola's second-generation high-performance silicon-gate CMOS (HCMOS III) technology. The device integrates input registers, high speed SRAM, and high-drive capability output latching onto a single monolithic circuit for reduced parts count implementation of cache data RAM and writeable control store applications. The MCM6295 is well suited for applications involving the MC68030, MC68040, and AMD29K microprocessors. It is ideal for burst mode or pipelined bus applications.

Synchronous design allows precise cycle control with the use of an external clock (K), while CMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

The address (A0-A13), data (D0-D3), and write ($\overline{W}$) inputs are all clock (K) controlled, positive-edge-triggered, noninverting registers.

The MCM6295 provides transparent output operation when K is low for access of RAM data within the same cycle (output data is latched when K is high).

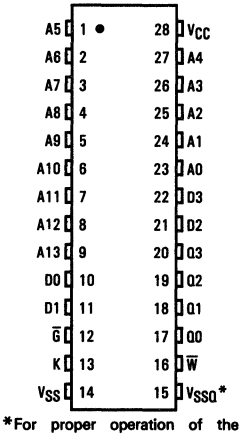
The output enable ($\overline{G}$) provides asynchronous bus control for common I/O or bank switch applications.

Write operations are internally self-timed and initiated by the rising edge of the K input. This feature eliminates complex off-chip write pulse generation and provides increased flexibility for incoming signals.

The MCM6295 is available in a 300-mil, 28-pin plastic DIP as well as a 300-mil, 28-pin plastic SOJ package.

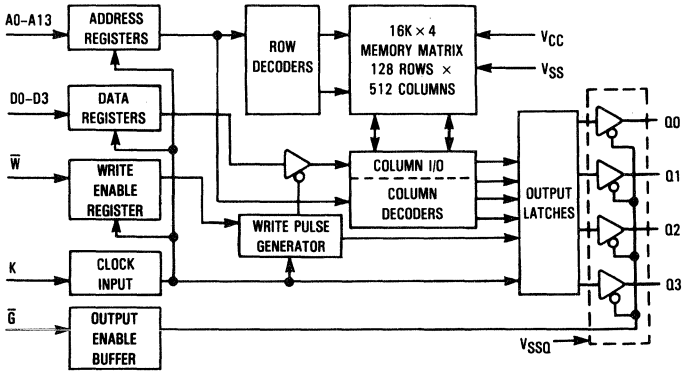
- Single 5 V ±10% Power Supply
- Fast Access and Cycle Times: 25/30 ns Max
- Address, Data Input, and $\overline{W}$ Registers On-Chip
- Transparent Output Latch for Access Within the Same Cycle
- Output Enable for Asynchronous Bus Control
- High Output Drive Capability
- Internally Self-Timed Write Pulse Generation
- Separate Data Input and Data Output Pins
- High Board Density SOJ Package Available
- Typical Applications: General-Purpose Buffer Storage, Writeable Control Store, Data Cache, or Cache Tag

PIN ASSIGNMENT



*For proper operation of the device, both V_{SS} and V_{SSQ} must be connected to ground.

BLOCK DIAGRAM



PIN NAMES	
A0-A13	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
D0-D3	Data Inputs
Q0-Q3	Data Outputs
K	Clock Input
V_{CC}	+5 V Power Supply
V_{SS}	Ground
V_{SSQ}	Output Buffer Ground

9

TRUTH TABLE

$\overline{G}$	$\overline{W}$	Operation	Q0-Q3
X	L	Write	High Z
L	H	Read	D_{out}
H	H	Output Disabled	High Z

NOTE: The value $\overline{W}$ is a valid input for the setup and hold times relative to the K rising edge. The value $\overline{G}$ is an asynchronous input.

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to $V_{SS} = V_{SSQ} = 0$ V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS}/V_{SSQ} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC} +0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation (T_A = 25°C)	P_D	1.0	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for **ALL** rising edges of clock (K) while the device is selected.

This device contains circuitry that will ensure the output devices are in High Z at power up. Care should be taken by the user to ensure that all clocks are at V_{IL} or V_{IH} during power up to prevent spurious read cycles from occurring.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to $V_{SS} = V_{SSQ} = 0$ V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	–	V_{CC} +0.3	V
Input Low Voltage	V_{IL}	−0.5*	–	0.8	V

*V_{IL} (min) = −0.5 V dc; V_{IL} (min) = −3.0 V ac (pulse width ≤20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, $V_{in} = 0$ to V_{CC})	$I_{lkg(I)}$	–	±1.0	μA
Output Leakage Current ($\overline{S} = V_{IH}$, $V_{out} = 0$ to V_{CC}, Outputs must be in high-Z)	$I_{lkg(O)}$	–	±1.0	μA
AC Supply Current ($\overline{G} = V_{IL}$, $I_{out} = 0$ mA, Cycle Time ≥ t_{KHKH} min)	I_{CCA}	–	140	mA
Output Low Voltage (I_{OL} = 12.0 mA)	V_{OL}	–	0.4	V
Output High Voltage (I_{OH} = −10.0 mA)	V_{OH}	2.4	–	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	4	6	pF
Output Capacitance	C_{out}	7	10	pF

9

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . .0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns

Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load . . . . . .See Figure 1A Unless Otherwise Noted

READ CYCLE (See Note 1)

Parameter	Symbol	MCM6295-25		MCM6295-30		Unit	Notes
		Min	Max	Min	Max		
Read Cycle Time	t_{KHKH}	25	–	30	–	ns	2
Clock Access Time	t_{KHQV}	–	25	–	30	ns	4, 6
Data Valid from Clock Low	t_{KLQV}	–	10	–	13	ns	5, 6
Output Hold from Clock Low	t_{KLQX}	0	–	0	–	ns	3, 6
Clock Low Pulse Width	t_{KLKH}	5	–	5	–	ns	
Clock High Pulse Width	t_{KHKL}	5	–	5	–	ns	
Setup Times for: A	t_{AVKH}	5	–	5	–	ns	7
Setup Times for: $\overline{W}$	t_{WHKH}	5	–	5	–	ns	7
Hold Times for: A	t_{KHAX}	3	–	3	–	ns	7
Hold Times for: $\overline{W}$	t_{KHWX}	3	–	3	–	ns	7
$\overline{G}$ High to Q High Z	t_{GHQZ}	–	10	–	13	ns	8
$\overline{G}$ Low to Q Active	t_{GLQX}	0	–	0	–	ns	8
$\overline{G}$ Low to Q Valid	t_{GLQV}	–	10	–	13	ns	

NOTES:
1. A read is defined by $\overline{W}$ high for the setup and hold times.
2. All read cycle timing is referenced from K or from $\overline{G}$.
3. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B. This parameter is sampled not 100% tested.
4. For Read Cycle 1 timing, clock high pulse width $< (t_{KHQV} - t_{KLQV})$.
5. For Read Cycle 2 timing, clock high pulse width $\geq (t_{KHQV} - t_{KLQV})$.
6. K must be at a low level for outputs to transition.
7. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for **ALL** rising edges of clock (K) while the device is selected.
8. At any given voltage and temperature, t_{GHQZ} max is less than t_{GLQX} min, both for a given device and from device to device.

9

AC TEST LOADS

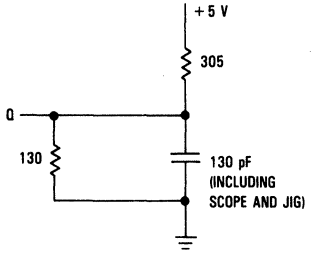


Figure 1A

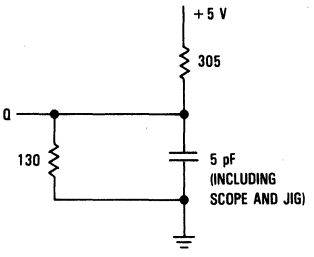
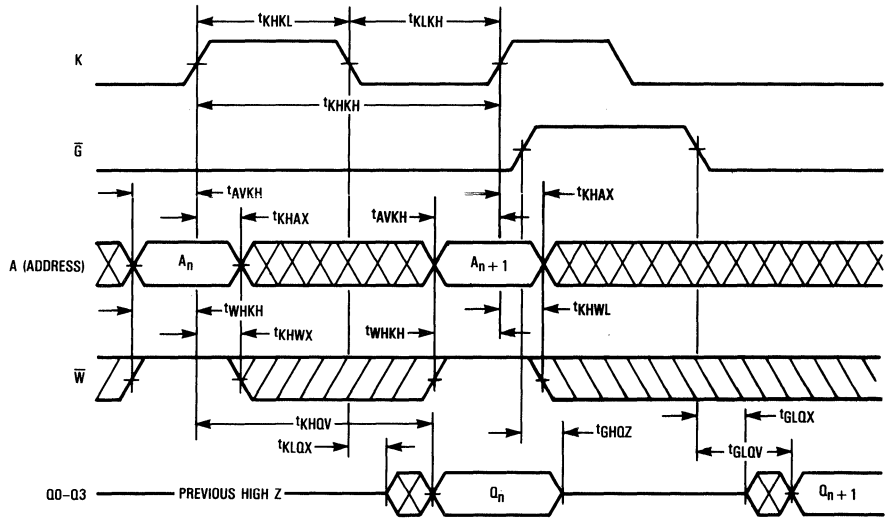
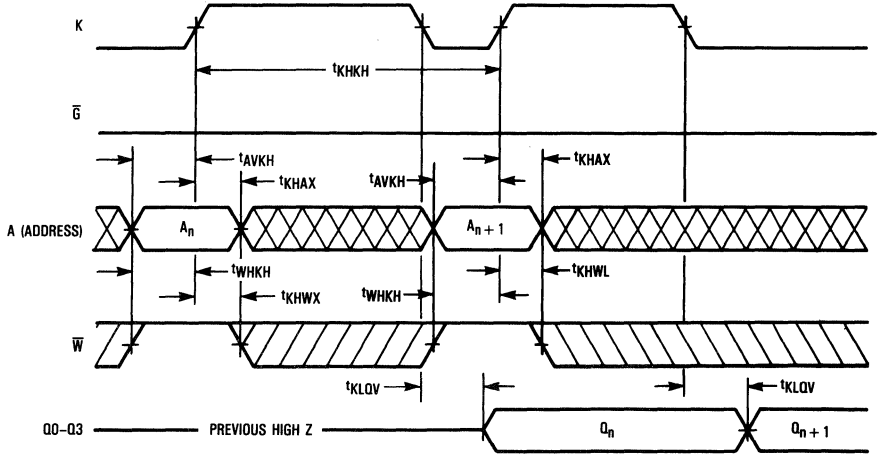


Figure 1B

READ CYCLE 1 (See Note 1)



READ CYCLE 2 (See Note 2)

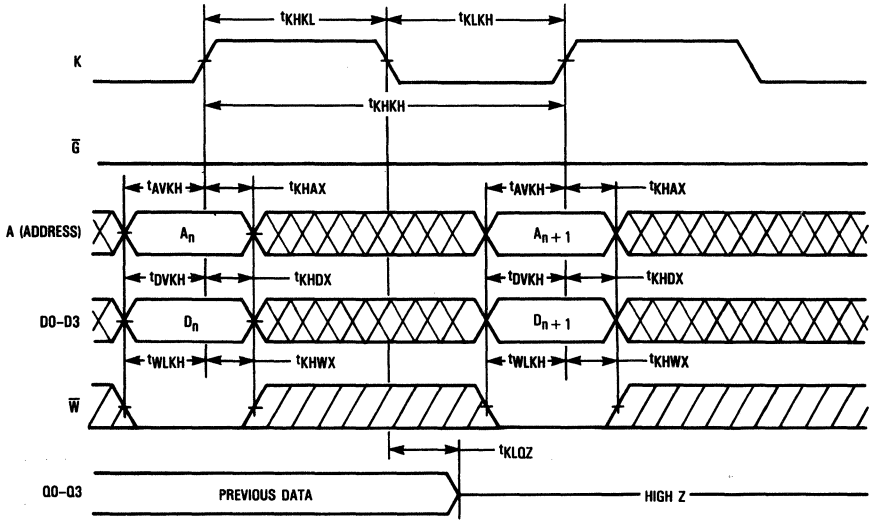


NOTES:
1. For Read Cycle 1 timing, clock high pulse width $<(t_{KHQV}-t_{KLQV})$.
2. For Read Cycle 2 timing, clock high pulse width $\geq(t_{KHQV}-t_{KLQV})$.

WRITE CYCLE ($\overline{W}$ Controlled, See Note 1)

Parameter		Symbol	MCM6295-25		MCM6295-30		Unit	Notes
			Min	Max	Min	Max		
Write Cycle Time		t_{KHKH}	25	–	30	–	ns	2
Clock Low to Output High Z ($\overline{W}=V_{IL}$)		t_{KLQZ}	–	10	–	13	ns	3
$\overline{G}$ High to Q High Z		t_{GHQZ}	–	10	–	13	ns	4
Setup Times for:	A	t_{AVKH}	5	–	5	–	ns	5
	$\overline{W}$	t_{WLKH}						
	D	t_{DVKH}						
Hold Times for:	A	t_{KHAX}	3	–	3	–	ns	5
	$\overline{W}$	t_{KHWX}						
	D	t_{KHDX}						

NOTES:
1. A write is performed when $\overline{W}$ is low for the specified setup and hold times.
2. All write cycle timing is referenced from K.
3. K must be at a low level for outputs to transition.
4. $\overline{G}$ becomes a don't care signal for successive writes after the first write cycle.
5. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for **ALL** rising edges of clock (K) while the device is selected.



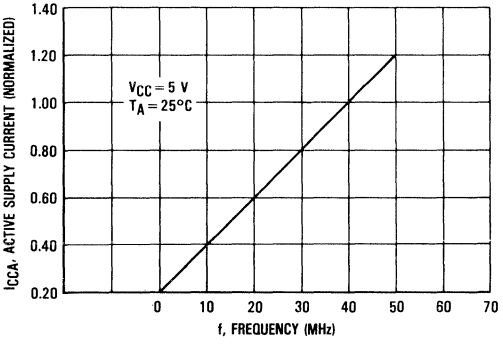


Figure 2. Active Supply Current versus Frequency

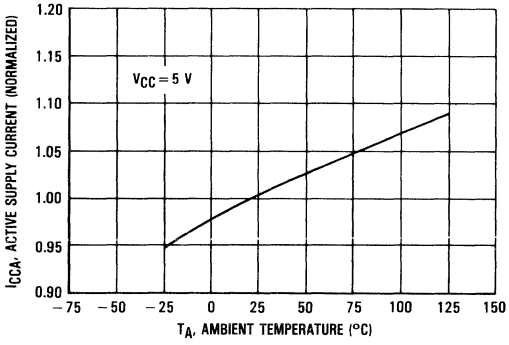


Figure 3. Active Supply Current versus Temperature

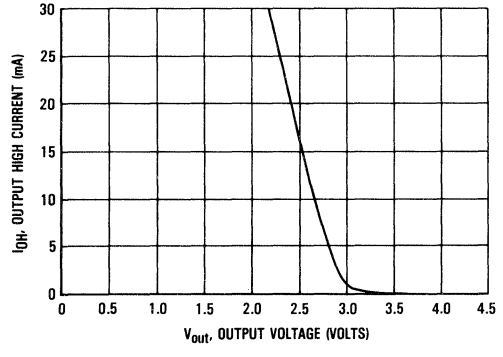


Figure 4. Output Source Current versus Output Voltage

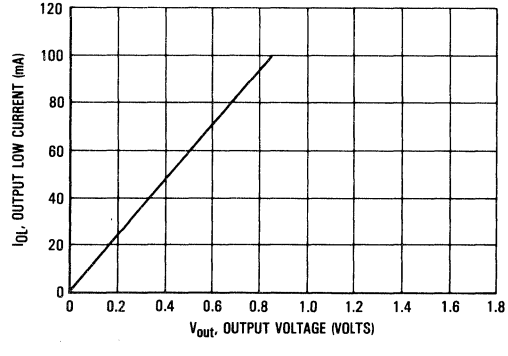


Figure 5. Output Sink Current versus Output Voltage

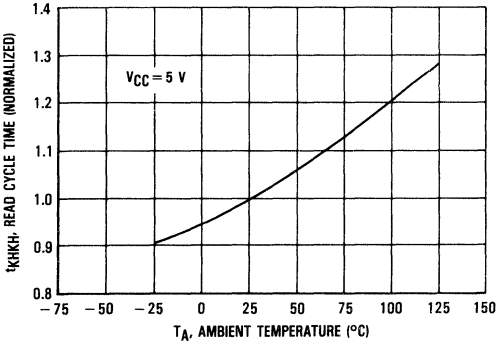


Figure 6. Read Cycle Time versus Temperature

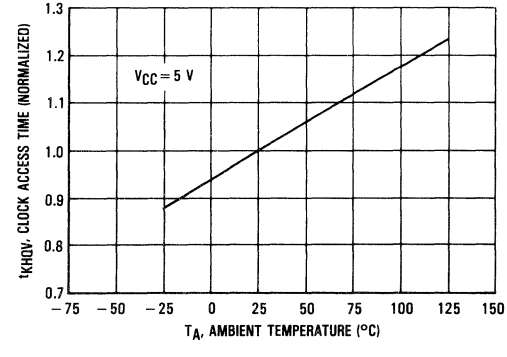


Figure 7. Clock Access Time versus Temperature

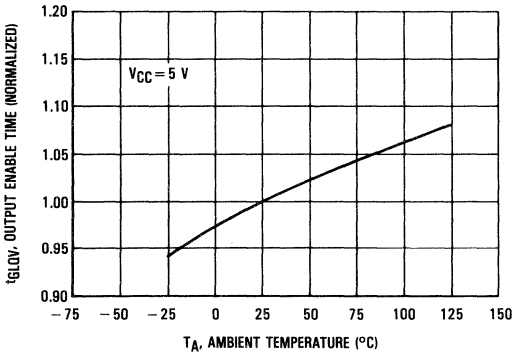


Figure 8. Output Enable Time versus Temperature

ORDERING INFORMATION
(Order by Full Part Number)

MCM 6295 X XX XX

Motorola Memory Prefix — MCM

Part Number — 6295

Package (P = 300 mil Plastic DIP, NJ = 300 mil SOJ) — X

Speed (25 = 25 ns, 30 = 30 ns) — XX

Shipping Method (R2 = Tape & Reel, Blank = Rails) — XX

Full Part Numbers — MCM6295P25, MCM6295P30, MCM6295NJ25, MCM6295NJ30, MCM6295NJ25R2, MCM6295NJ30R2

9

APPLICATIONS INFORMATION

The Motorola family of synchronous SRAMs is designed to provide a performance and parts count advantage in applications such as writeable control stores, memory mapping, and cache memory. The on-board input registers eliminate the need for external latch chips in systems where addresses and data are not on the bus long enough to satisfy standard SRAM setup and hold times. Latches on the output port provide extended hold times independent of address or other device input changes to better meet system access requirements. The clock (K) input controls the operation of the input registers and output latches, and provides a direct means of synchronizing the SRAM to a system clock.

The MCM6295 offers transparent output operation, which allows output data access within the same t_{KHKH} cycle. This feature lends itself well to applications requiring RAM data to be set up on the system bus prior to the next rising clock edge. On the rising edge of the clock (K) signal, the output data for the previous cycle is latched until the next falling clock edge. When the clock (K) signal is low, the output is allowed to transition relative to the most recent rising clock (K) edge.

Figure 9 shows a typical system configuration using four MCM6295 chips. The system addresses are tied to the MCM6295s in parallel, while system data is distributed among the four input data ports of 4 bits each. Output data is tied to a separate output data bus to exploit the separate I/O configuration of the MCM6295. The clock (K) signal is a logical derivation of the system clock.

Figure 10 shows typical bus timing for the configuration of Figure 9. The system bus supplies address, data, and control signals, while accepting data from the memory on rising clock edges. In some applications, the clock (K) signal may need to be a delayed system clock to allow adequate address and data setup times.

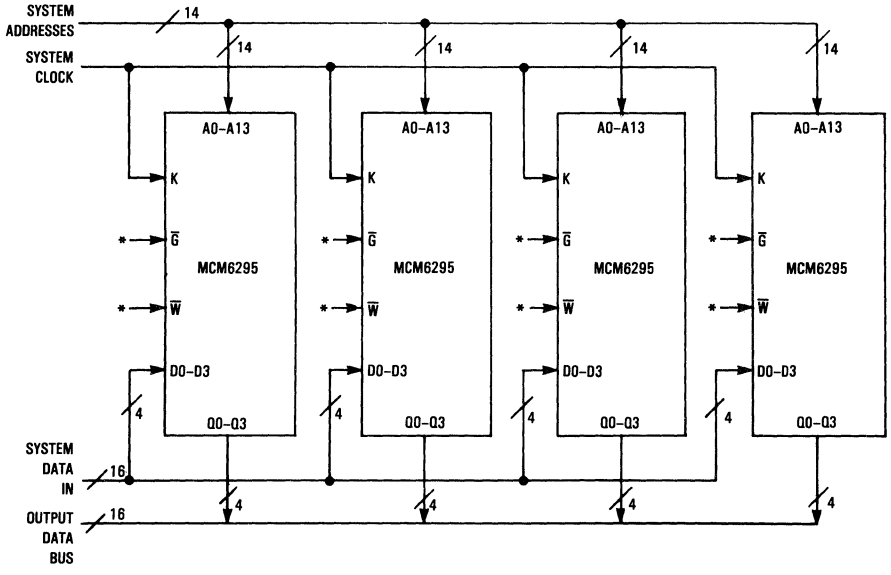
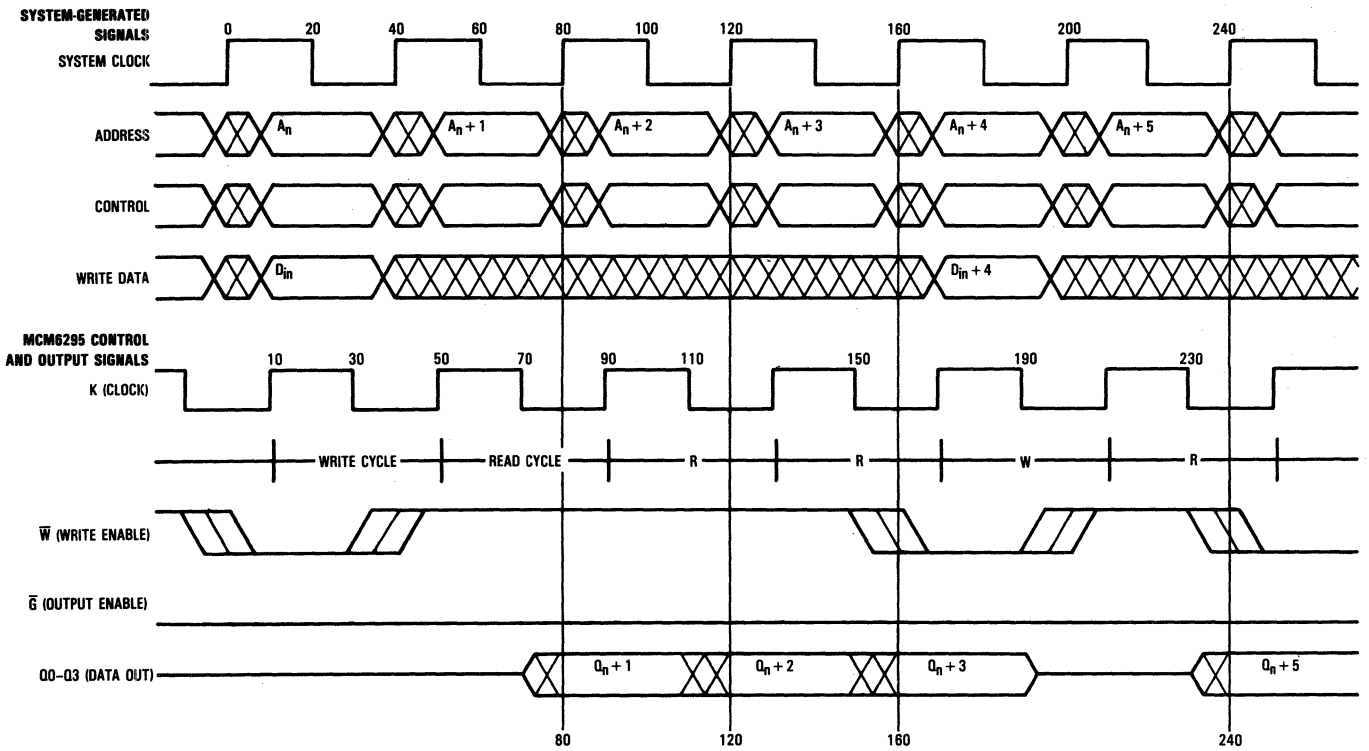


Figure 9. Typical Configuration for a 16-Bit Bus



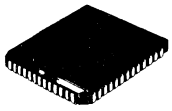
NOTES:
1. The system supplies address, data, and control information and accepts data from memory on the rising edge of the system clock.
2. The memory clock is delayed 10 ns (for this example) to allow input information to propagate to the memory chips.

Figure 10. Nonpipeline System Timing

MCM56824

Product Preview

DSPRAM™
8K × 24 Bit Fast Static RAM



FN PACKAGE
52-LEAD PLCC
CASE 778

The MCM56824 is a 196,608 bit static random access memory organized as 8,192 words of 24 bits, fabricated using Motorola's high-performance silicon-gate CMOS technology. The device integrates an 8K × 24 SRAM core with multiple chip enable inputs, output enable, and an externally controlled single address pin multiplexer. These functions allow for direct connection to the Motorola DSP56001 Digital Signal Processor and provide a very efficient means for implementation of a reduced parts count system requiring no additional interface logic. This device can also be used as three 8K × 8 SRAMs by holding V/$\overline{S}$ low.

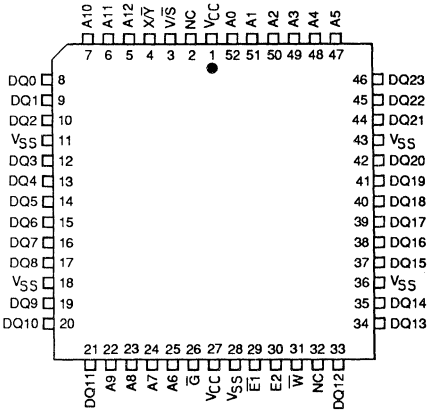
The availability of multiple chip enable ($\overline{E1}$ and E2) and output enable ($\overline{G}$) inputs provides for greater system flexibility when multiple devices are used. With either chip enable input unasserted, the device will enter standby mode, which is useful in low-power applications. A single on-chip multiplexer selects A12 or X/$\overline{Y}$ as the highest order address input depending upon the state of the V/$\overline{S}$ control input. This feature allows one physical static RAM component to efficiently store program and vector or scalar operands. By connecting DSP56001 program memory select ($\overline{PS}$) to the VECTOR/SCALAR (V/$\overline{S}$) MUX control pin, such partitioning can occur with no additional components. This allows efficient utilization of the RAM resource regardless of operand type. Refer to the application diagrams at the end of this document for additional information.

Multiple power and ground pins have been utilized to minimize effects induced by output noise.

- Single 5 V ± 10% Power Supply
- Fast Access and Cycle Times: 25/30/35 ns Max
- Fully Static Read and Write Operations
- Equal Address and Chip Enable Access Times
- On-Chip Single Address Multiplexer
- Active High and Active Low Chip Enable Inputs
- Output Enable Controlled Three-State Outputs
- High Board Density PLCC Package
- Low-Power Standby Mode
- Fully TTL Compatible

$\overline{DSPRAM}$ is a trademark of Motorola, Inc.

PIN ASSIGNMENT

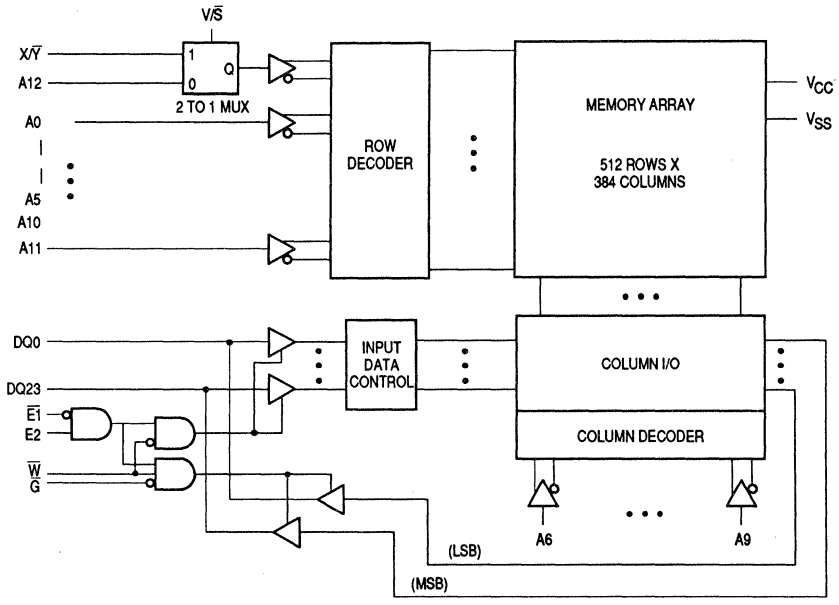


PIN NAMES	
A0–A11	Address Inputs
A12,X/$\overline{Y}$	Multiplexed Address
V/$\overline{S}$	Address Multiplexer Control
$\overline{W}$	Write Enable
$\overline{E1}$, E2	Chip Enable
$\overline{G}$	Output Enable
DQ0–DQ23	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground
NC	No Connection

For proper operation of the device, all V_{SS} pins must be connected to ground.

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

BLOCK DIAGRAM



TRUTH TABLE

$\overline{E1}$	E2	$\overline{G}$	$\overline{W}$	V/$\overline{S}$	Mode	Supply Current	I/O Status
H	X	X	X	X	Not Selected	I_{SB}	High-Z
X	L	X	X	X	Not Selected	I_{SB}	High-Z
L	H	H	H	X	Output Disable	I_{CC}	High-Z
L	H	L	H	H	Read Using X/$\overline{Y}$	I_{CC}	Data Out
L	H	L	H	L	Read Using A12	I_{CC}	Data Out
L	H	X	L	H	Write Using X/$\overline{Y}$	I_{CC}	Data In
L	H	X	L	L	Write Using A12	I_{CC}	Data In

NOTE: X = don't care.

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to 7.0 V	V
Voltage Relative to V_{SS}	V_{in}, V_{out}	−0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation (T_A = 70°C, V_{CC} = 5 V, t_{AVAV} = 50 ns)	P_D	1.25	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is assumed to be in a test socket or mounted on a printed circuit board with at least 300 LFPM of transverse air flow being maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	3.0	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	−0.5*	0.0	0.8	V

*V_{IL} (min) = −3.0 V ac (pulse width ≤20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	±1.0	µA
Output Leakage Current ($\overline{G}$ = V_{IH}, $\overline{E1}$ = V_{IH}, E2 = V_{IL}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	±1.0	µA
AC Supply Current ($\overline{G}$ = V_{IH}, $\overline{E1}$ = V_{IL}, E2 = V_{IH}, I_{out} = 0 mA, All Other Inputs = V_{IL} = 0.0 V or V_{IH} = 3.0 V)	I_{CCA}			mA
MCM56824-25: Cycle Time ≥ 25 ns		—	250	
MCM56824-30: Cycle Time ≥ 30 ns		—	210	
MCM56824-35: Cycle Time ≥ 35 ns		—	180	
Standby Current ($\overline{E1}$ = V_{IH}, E2 = V_{IL}, All Inputs = V_{IL} or V_{IH})	I_{SB1}	—	15	mA
CMOS Standby Current ($\overline{E1}$ ≥ V_{CC} − 0.2 V, E2 ≤ 0.2 V, All Inputs ≥ V_{CC} − 0.2 V or ≤ 0.2 V)	I_{SB2}	—	10	mA
Output Low Voltage (I_{OL} = +8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = −4.0 mA)	V_{OH}	2.4	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Typical	Max	Unit
Input Capacitance	All Pins Except DQ0–DQ23	C_{in}	4	6	pF
Input/Output Capacitance	DQ0–DQ23	$C_{I/O}$	6	8	pF

9

AC TEST LOADS

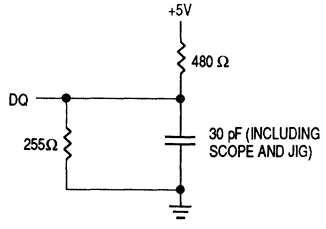


Figure 1A

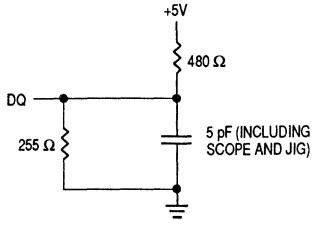


Figure 1B

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

READ CYCLE TIMING (See Notes 1, 2, 3)

Parameter	Symbol		MCM56824-25		MCM56824-30		MCM56824-35		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	25	—	30	—	35	—	ns	
Address Access Time	t_{AVQV}	t_{AA}	—	25	—	30	—	35	ns	
MUX Control Valid to Output Valid	t_{VSVQV}	t_{AA}	—	25	—	30	—	35	ns	
Chip Enable to Output Valid	t_{E1LQV} t_{E2HQV}	t_{AC1} t_{AC2}	—	25	—	30	—	35	ns	4
Output Enable to Output Valid	t_{GLQV}	t_{OE}	—	12	—	15	—	15	ns	
Output Active from Chip Enable	t_{E1LQX} t_{E2HQX}	t_{CLZ}	2	—	2	—	2	—	ns	4, 5
Output Active from Output Enable	t_{GLQX}	t_{OLZ}	2	—	2	—	2	—	ns	5
Output Hold from Address Change	t_{AXQX}	t_{OH}	5	—	5	—	5	—	ns	
Output Hold from MUX Control Change	t_{VSXQX}	t_{VSOH}	5	—	5	—	5	—	ns	
Chip Enable to Output High Z	t_{E1HQZ} t_{E2LQZ}	t_{CHZ}	0	12	0	15	0	15	ns	4, 5
Output Enable High to Output High Z	t_{GHQZ}	t_{OHZ}	0	12	0	15	0	15	ns	5

NOTES:
1. A read cycle is defined by $\overline{W}$ high.
2. All read cycle timings are referenced from the last valid address or V/$\overline{S}$ transition to the first address or V/$\overline{S}$ transition.
3. Addresses and V/$\overline{S}$ valid prior to or coincident with $\overline{E1}$ going low or E2 going high.
4. $\overline{E1}$ in the timing diagrams represents both $\overline{E1}$ and E2 with $\overline{E1}$ asserted low and E2 asserted high.
5. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{E1HQZ} max is less than t_{E1LQX} min, t_{E2LQZ} max is less than t_{E2HQX} min, and t_{GHQZ} max is less than t_{GLQX} min for a given device and from device to device.

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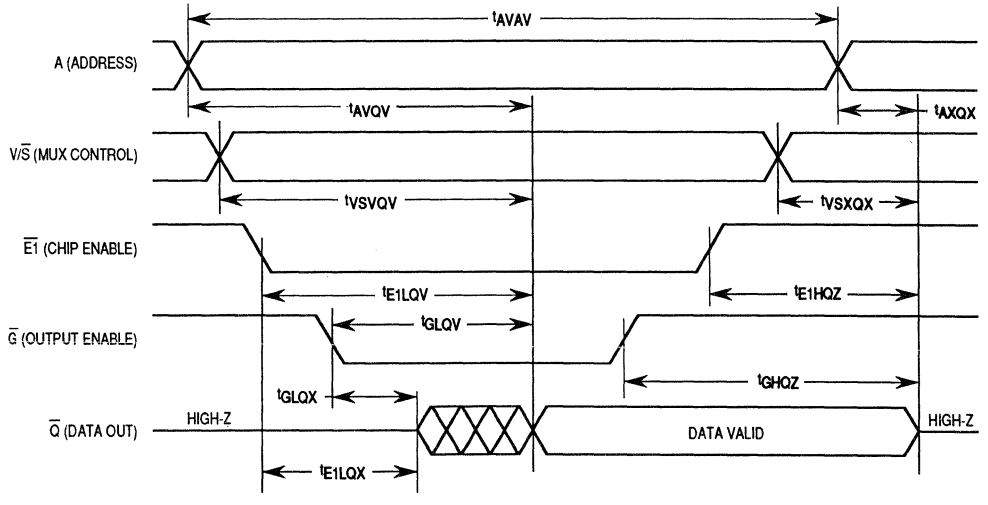
READ CYCLE

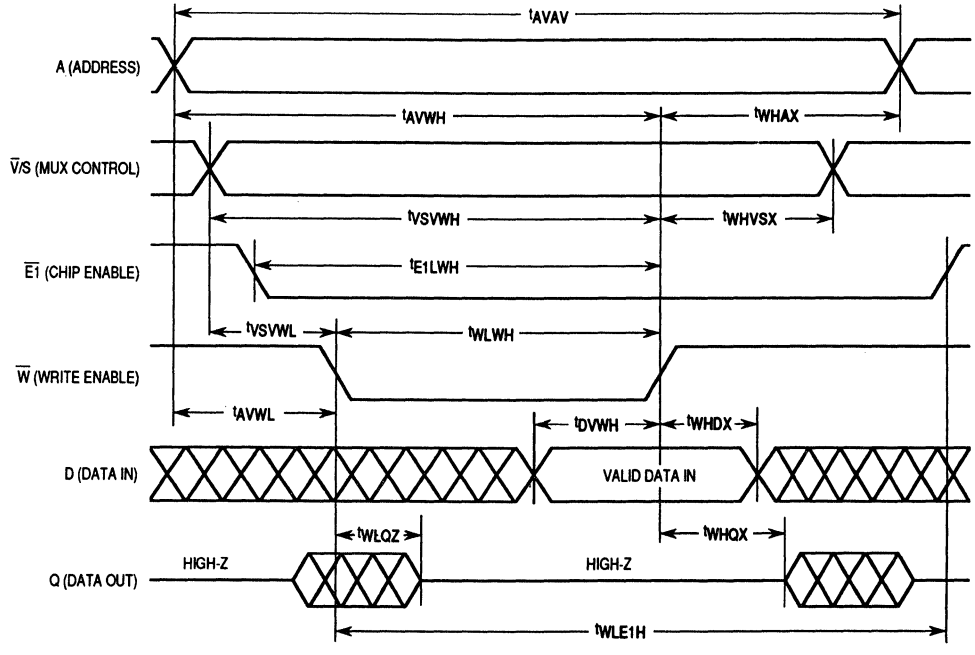


WRITE CYCLE TIMING, WRITE ENABLE INITIATED (See Note 1)

Parameter	Symbol		MCM56824-25		MCM56824-30		MCM56824-35		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	25	—	30	—	35	—	ns	
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	0	—	ns	2
MUX Control Setup Time	t_{VSVWL}	t_{VSS}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	20	—	25	—	30	—	ns	
MUX Control Valid to End of Write	t_{VSVWH}	t_{VSW}	20	—	25	—	30	—	ns	
Write Pulse Width	t_{WLWH}	t_{WP}	15	—	18	—	20	—	ns	3
Write Enable to Chip Enable Disable	t_{WLE1H} t_{WLE2L}	t_{CW}	15	—	18	—	20	—	ns	3, 4
Chip Enable to End of Write	t_{E1LWH} t_{E2HWH}	t_{CW}	15	—	18	—	20	—	ns	3, 4
Data Valid to End of Write	t_{DVWH}	t_{DW}	10	—	12	—	15	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	—	0	—	0	—	ns	5
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	0	—	ns	2
MUX Control Recovery Time	t_{WHVSX}	t_{VSR}	0	—	0	—	0	—	ns	
Write High to Output Low Z	t_{WHQX}	t_{OW}	2	—	2	—	2	—	ns	6
Write Low to Output High Z	t_{WLQZ}	t_{WHZ}	0	12	0	15	0	15	ns	6

NOTES:
1. A write cycle starts at the latest transition of $\overline{E1}$ low, $\overline{W}$ low, or E2 high. A write cycle ends at the earliest transition of $\overline{E1}$ high, $\overline{W}$ high, or E2 low.
2. Write must be high for all address and V/$\overline{S}$ transitions.
3. If $\overline{W}$ goes low coincident with or prior to $\overline{E1}$ low or E2 high the outputs will remain in a high-impedance state.
4. $\overline{E1}$ in the timing diagrams represents both $\overline{E1}$ and E2 with $\overline{E1}$ asserted low and E2 asserted high.
5. During this time the output pins may be in the output state. Signals of opposite phase must not be applied to the outputs at this time.
6. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B. This prameter is sampled and not 100% tested. At any given voltage and temperature, t_{E1HQZ} max is less than t_{E1LQX} min, t_{E2LQZ} max is less than t_{E2HQX} min, and t_{GHQZ} max is less than t_{GLQX} min for a given device and from device to device.

$\overline{W}$ INITIATED WRITE CYCLE



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WRITE CYCLE TIMING, CHIP ENABLE INITIATED (See Note 1)

Parameter	Symbol		MCM56824-25		MCM56824-30		MCM56824-35		Unit	Notes
	Symbol	Alternate	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	25	—	30	—	35	—	ns	
Address Setup Time	t_{AVE1L} t_{AVE2H}	t_{AS}	0	—	0	—	0	—	ns	2
MUX Control Setup Time	t_{VSE1L} t_{VSE2H}	t_{VSS}	0	—	0	—	0	—	ns	2
Address Valid to End of Write	t_{AVE1H} t_{AVE2L}	t_{SW}	20	—	25	—	30	—	ns	2
MUX Control Valid to End of Write	t_{VSE1H} t_{VSE2L}	t_{VSW}	20	—	25	—	30	—	ns	2
Chip Enable to End of Write	t_{E1LE1H} t_{E2HE2L}	t_{CW}	15	—	18	—	20	—	ns	2, 3
Data Valid to End of Write	t_{DVE1H} t_{DVE2L}	t_{DW}	10	—	12	—	15	—	ns	2
Data Hold Time	t_{E1HDX} t_{E2LDX}	t_{DH}	0	—	0	—	0	—	ns	2, 4
Write Recovery Time	t_{E1HAX} t_{E2LAX}	t_{WR}	0	—	0	—	0	—	ns	2
MUX Control Recovery Time	t_{E1HVSX} t_{E2LVSX}	t_{VSR}	0	—	0	—	0	—	ns	2

NOTES:
1. A write cycle starts at the latest transition of $\overline{E1}$ low, $\overline{W}$ low, or E2 high. A write cycle ends at the earliest transition of $\overline{E1}$ high, $\overline{W}$ high, or E2 low.
2. $\overline{E1}$ in the timing diagrams represents both $\overline{E1}$ and E2 with $\overline{E1}$ asserted low and E2 asserted high.
3. If $\overline{W}$ goes low coincident with or prior to $\overline{E1}$ low or E2 high the outputs will remain in a high-impedance state.
4. During this time the output pins may be in the output state. Signals of opposite phase must not be applied to the outputs at this time.

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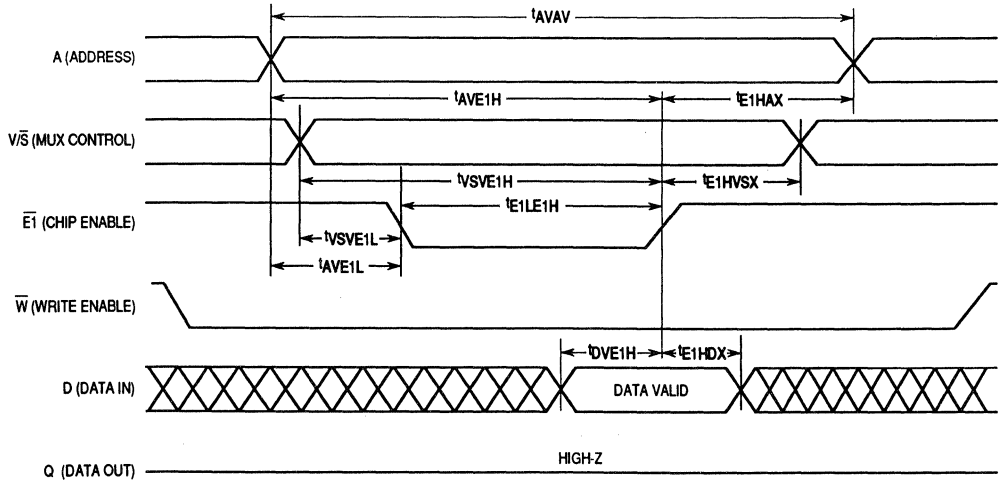
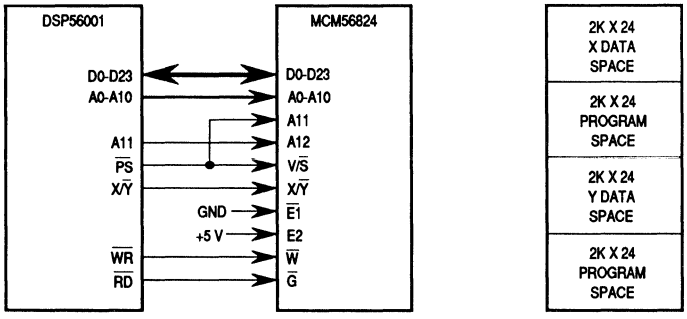
$\overline{E1}$ OR E2 INITIATED WRITE CYCLE

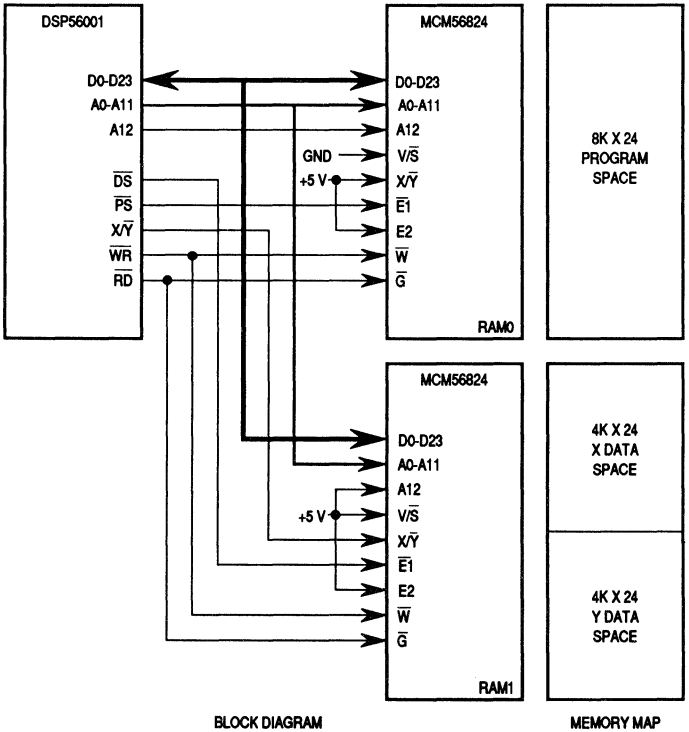


DSP56001/MCM56824 One-Chip Memory Solution
(4K Program/2K X-Data/2K Y-Data)



BLOCK DIAGRAM MEMORY MAP

DSP56001/MCM56824 Two-Chip Memory Solution
(8K Program/4K X-Data/4K Y-Data)



BLOCK DIAGRAM MEMORY MAP

NOTE: E2 may be connected to a DSP56001 high-order address bit to eliminate internal/external memory overlap.

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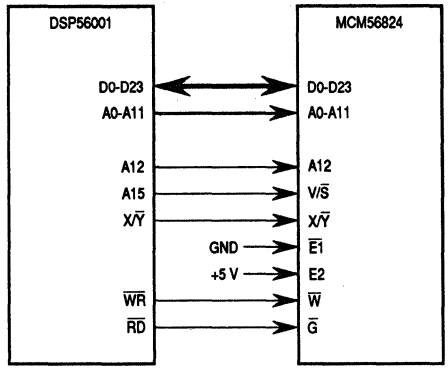
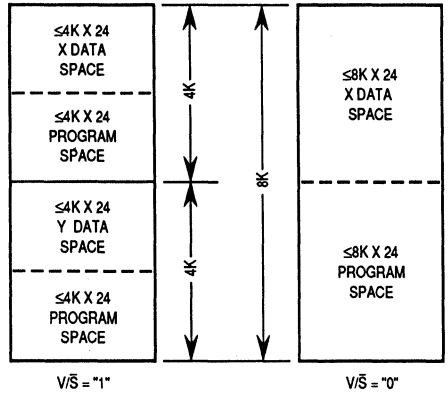


BLOCK DIAGRAM



MEMORY MAPS

The DSPRAM may be dynamically repartitioned by connecting DSP56001 address A15 to V/S. This allows for software control of the relative sizes of the program and X and/or Y data spaces.

ORDERING INFORMATION
(Order by Full Part Number)

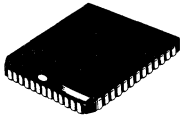
MCM	56824	XX	XX
Motorola Memory Prefix	Part Number	Package (FN = PLCC)	Speed (25 = 25 ns, 30 = 30 ns, 35 = 35 ns)

Full Part Numbers — MCM56824FN25 MCM56824FN30 MCM56824FN35

Product Preview

32K × 9 Bit Synchronous Dual I/O Fast Static RAM with Parity Checker

MCM62110



FN PACKAGE
PLASTIC
CASE 778

The MCM62110 is a 294,912 bit synchronous static random access memory organized as 32,768 words of 9 bits, fabricated using Motorola's high-performance silicon-gate CMOS technology. The device integrates a 32K x 9 SRAM core with advanced peripheral circuitry consisting of address registers, two sets of input data registers, two sets of output latches, active high and active low chip enables, and a parity checker. The RAM checks odd parity during RAM read cycles. The data parity error ($\overline{DPE}$) output is an open drain type output which indicates the result of this check. This device has increased output drive capability supported by multiple power pins. In addition, the output levels can be either 3.3 V or 5 V TTL compatible by choice of the appropriate output bus power supply.

The device has both asynchronous and synchronous inputs. Asynchronous inputs include the processor output enable ($\overline{POE}$), system output enable ($\overline{SOE}$), and the clock (K).

The address (A0–A14) and chip enable ($\overline{E1}$ and E2) inputs are synchronous and are registered on the falling edge of K. Write enable ($\overline{W}$), processor input enable ($\overline{PIE}$) and system input enable ($\overline{SIE}$) are registered on the rising edge of K. Writes to the RAM are self-timed.

All data inputs/outputs, PDQ0–PDQ7, SDQ0–SDQ7, PDQP, and SDQP have input data registers triggered by the rising edge of the clock. These pins also have three-state output latches which are transparent during the high level of the clock and latched during the low level of the clock.

This device has a special feature which allows data to be passed through the RAM between the system and processor ports in either direction. This streaming is accomplished by latching in data from one port and asynchronously output enabling the other port. It is also possible to write to the RAM while streaming.

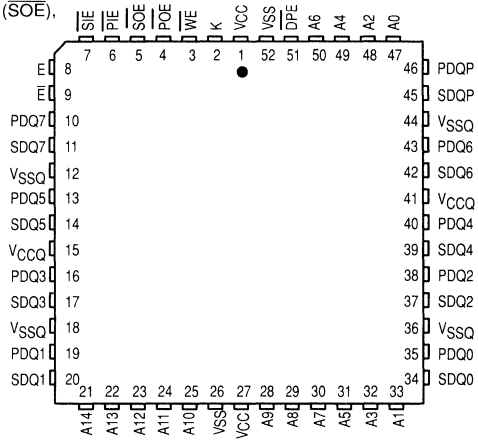
Additional power supply pins have been utilized for maximum performance. The output buffer power (V_{CCQ}) and ground pins (V_{SSQ}) are electrically isolated from V_{SS} and V_{CC}, and supply power and ground only to the output buffers. This allows connecting the output buffers to 3.3 V instead of 5.0 V if desired. If 3.3 V output levels are chosen, the output buffer impedance in the "high" state is approximately equal to the impedance in the "low" state thereby allowing simplified transmission line terminations.

The MCM62110 will be available in a 52 pin plastic leaded chip carrier (PLCC).

This device is ideally suited for pipelined systems and systems with multiple data buses and multiprocessing systems, where a local processor has a bus isolated from a common system bus.

- Single 5 V ± 10% Power Supply
- Choice of 5 V or 3.3 V ± 10% Power Supplies for Output Level Compatibility
- Fast Access and Cycle Times: 15/20 ns Max
- Self-Timed Write Cycles
- Clock Controlled Output Latches
- Address, Chip Enable, and Data Input Registers
- Common Data Inputs and Data Outputs
- Dual I/O for Separate Processor and Memory Buses
- Separate Output Enable Controlled Three-State Outputs
- Odd Parity Checker during Reads
- Open Drain Output on Data Parity Error ($\overline{DPE}$) Allowing Wire-ORing of Outputs
- High Output Drive Capability: 85 pF/Output at Rated Access Time
- High Board Density 52 Lead PLCC Package
- Active High and Low Chip Enables for Easy Memory Depth Expansion

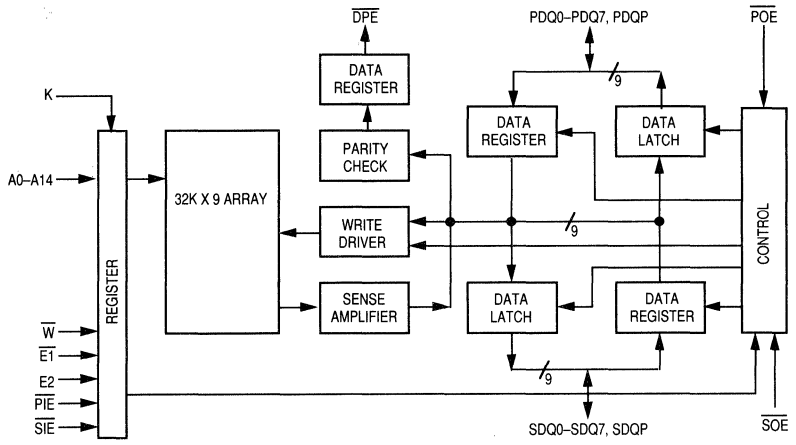
PIN ASSIGNMENT



PIN NAMES	
A0–A14	Address Inputs
K	Clock Input
$\overline{W}$	Write Enable
$\overline{E1}$	Active Low Chip Enable
E2	Active High Chip Enable
$\overline{PIE}$	Processor Input Enable
$\overline{SIE}$	System Input Enable
$\overline{POE}$	Processor Output Enable
$\overline{SOE}$	System Output Enable
$\overline{DPE}$	Data Parity Error
PDQ0–DPQ7	Processor Data I/O
PDQP	Processor Data Parity
SDQ0–SDQ7	System Data I/O
SDQP	System Data Parity
V_{CC}	+ 5 V Power Supply
V_{CCQ}	Output Buffer Power Supply
V_{SSQ}	Output Buffer Ground
V_{SS}	Ground

All power supply and ground pins must be connected for proper operation of the device. $V_{CC} \geq V_{CCQ}$ at all times including power up.

BLOCK DIAGRAM



FUNCTIONAL TRUTH TABLE (See Notes 1 and 8)

W	PIE	SIE	POE	SOE	Mode	Memory Subsystem Cycle	PDQ0–PDQ7, PDQP Output	SDQ0–SDQ7, SDQP Output	DPE	Notes
1	1	1	0	1	Read	Processor Read	Data Out	High-Z	Parity Out	2, 3
1	1	1	1	0	Read	Copy Back	High-Z	Data Out	Parity Out	2, 3
1	1	1	0	0	Read	Dual Bus Read	Data Out	Data Out	Parity Out	2,3
1	0	0	X	X	N/A	NOP	High-Z	High-Z	1	4
1	X	X	1	1	Read	NOP	High-Z	High-Z	1	
0	0	0	X	X	N/A	NOP	High-Z	High-Z	1	4
0	0	1	1	1	Write	Processor Write Hit	Data In	High-Z	1	5
0	1	0	1	1	Write	Allocate	High-Z	Data In	1	
0	0	1	1	0	Write	Write Through	Data In	Stream Data	1	6
0	1	0	0	1	Write	Allocate With Stream	Stream Data	Data In	1	6
1	0	1	1	0	N/A	Cache Inhibit Write	Data In	Stream Data	1	6
1	1	0	0	1	N/A	Cache Inhibit Read	Stream Data	Data In	1	6
0	1	1	X	X	N/A	NOP	High-Z	High-Z	1	4
X	0	1	0	0	N/A	Invalid	Data In	Stream	1	7
X	0	1	0	1	N/A	Invalid	Data In	High-Z	1	7
X	1	0	0	0	N/A	Invalid	Stream	Data In	1	7
X	1	0	1	0	N/A	Invalid	High-Z	Data In	1	7

NOTES:
1. A '0' represents an input voltage $\leq V_{IL}$ and a '1' represents an input voltage $\geq V_{IH}$. All inputs must satisfy the specified setup and hold times for the falling or rising edge of K. Some entries in this truth table represent latched values. This table assumes that the chip is selected (i.e., $\overline{E1} = 0$ and E2 = 1) and V_{CC} current is equal to I_{CCA}. If this is not true, the chip will be in standby mode, the V_{CC} current will equal I_{SB1} or I_{SB2} $\overline{DPE}$ will default to 1 and all RAM outputs will be in High-Z. Other possible combinations of control inputs not covered by this note or the table above are not supported and the RAMs behavior is not specified.
2. A read cycle is defined as a cycle where data is driven on the internal data bus by the RAM.
3. $\overline{DPE}$ is registered on the rising edge of K at the beginning of the following clock cycle
4. No RAM cycle is performed.
5. A write cycle is defined as a cycle where data is driven onto the internal data bus through one of the data I/O ports (PDQ0–PDQ7 and PDQP or SDQ0–SDQ7 and SPDQ), and written into the RAM.
6. Data is driven on the internal data bus by one I/O port through its data input register and latched into the data output latch of the other I/O port.
7. Data contention will occur.
8. If either $\overline{IE}$ signal is sampled low on the rising edge of clock, the corresponding $\overline{OE}$ is a don't care, and the corresponding outputs are High–Z.

PARITY CHECKER

Parity Scheme	$\overline{DPE}$
$\overline{E1} = V_{IH}$ and/or $E2 = V_{IL}$	1
RAMP = $\overline{RAM0} \oplus \overline{RAM1} \oplus \ldots \oplus \overline{RAM7}$	1
RAMP ≠ $\overline{RAM0} \oplus \overline{RAM1} \oplus \ldots \oplus \overline{RAM7}$	0

NOTE: RAMP, $\overline{RAM0}$, $\overline{RAM1}$ . . . , refer to the data that is present on the RAMs internal bus, not necessarily data that resides in the RAM array. $\overline{DPE}$ is always delayed one clock, and is registered on the rising edge of K at the beginning of the following clock cycle (see AC CHARACTERISTICS).

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to $V_{SS} = V_{SSQ} = 0$ V)

Rating	Symbol	Value	Unit
Power Supply	V_{CC}	– 0.5 to 7.0	V
Voltage Relative to V_{SS}/V_{SSQ} for Any Pin Except V_{CC} and V_{CCQ}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation (T_A = 70°C)	P_D	1.2	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

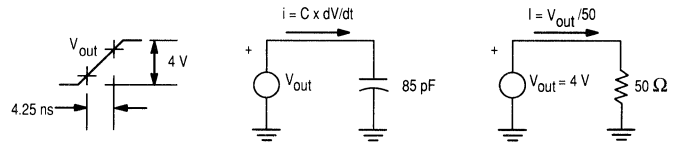
NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions to taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High-Z at power up.

CAPACITIVE LOAD EQUIVALENT RESISTANCE



$i = C \times \left(\frac{dV_{out}}{dt}\right) = 85 \times 10^{-12} \times \left(\frac{4\ V}{4.25 \times 10^{-9}}\right) = 80\ mA$

$i = \frac{V}{R} = \frac{4}{50} = 80\ mA$

85 pF load is equivalent to a 50 Ω termination

9

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, V_{CCQ} = 5.0 V or 3.3 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = V_{SSQ} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Output Buffer Supply Voltage (5.0 V TTL Compatible) (3.3 V 50 Ω Compatible)	V_{CCQ}	 4.5 3.0	 5.0 3.3	 5.5 3.6	V
Input High Voltage	V_{IH}	2.2	3.0	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	–0.5*	0.0	0.8	V

* V_{IL} (min) = 3.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	—	± 1.0	µA
Output Current ($\overline{G}$ = V_{IH})	$I_{lkg(O)}$	—	—	± 1.0	µA
AC Supply Current ($\overline{SOE}$ = $\overline{POE}$ = V_{IL}, All Inputs = V_{IL} or V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, I_{out} = 0 mA, MCM62110-15: t_{KHKH} = 15 ns Cycle Time ≥ t_{KHKH} min) MCM62110-20: t_{KHKH} = 20 ns	I_{CCA}	 — —	 220 200	 250 250	mA
TTL Standby Current (V_{CC} = Max, $\overline{E1}$ = V_{IH} or E2 = V_{IL})	I_{SB1}	—	—	40	mA
CMOS Standby Current (V_{CC} = Max, f = 0 MHz, $\overline{E1}$ = V_{IH} or E2 = V_{IL}, V_{in} ≤ V_{SS} + 0.2 V or ≥ V_{CC} –0.2 V)	I_{SB2}	—	—	30	mA
Output Low Voltage (I_{OL} = + 8.0 mA, $\overline{DPE}$: I_{OL} = +32.0 mA)	V_{OL}	—	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance (all Pins Expect I/Os)	C_{in}	4	6	pF
Input/Output Capacitance (PDQ0–PDQ7, SDQ0–SDQ7, PDQP, SDQP)	$C_{I/O}$	8	10	pF
Data Parity Error Output Capacitance ($\overline{DPE}$)	$C_{out(DPE)}$	6	7	pF

9

AC TEST LOADS

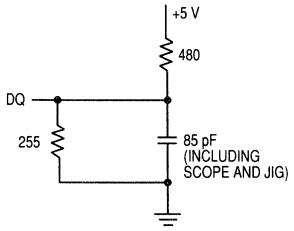


Figure 1A

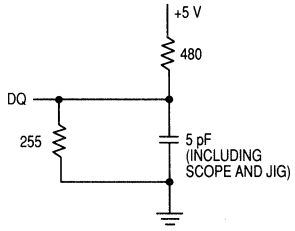


Figure 1B

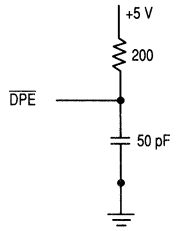


Figure 1C

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, V_{CCQ} = 5.0 V or 3.3 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Measurement Timing Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

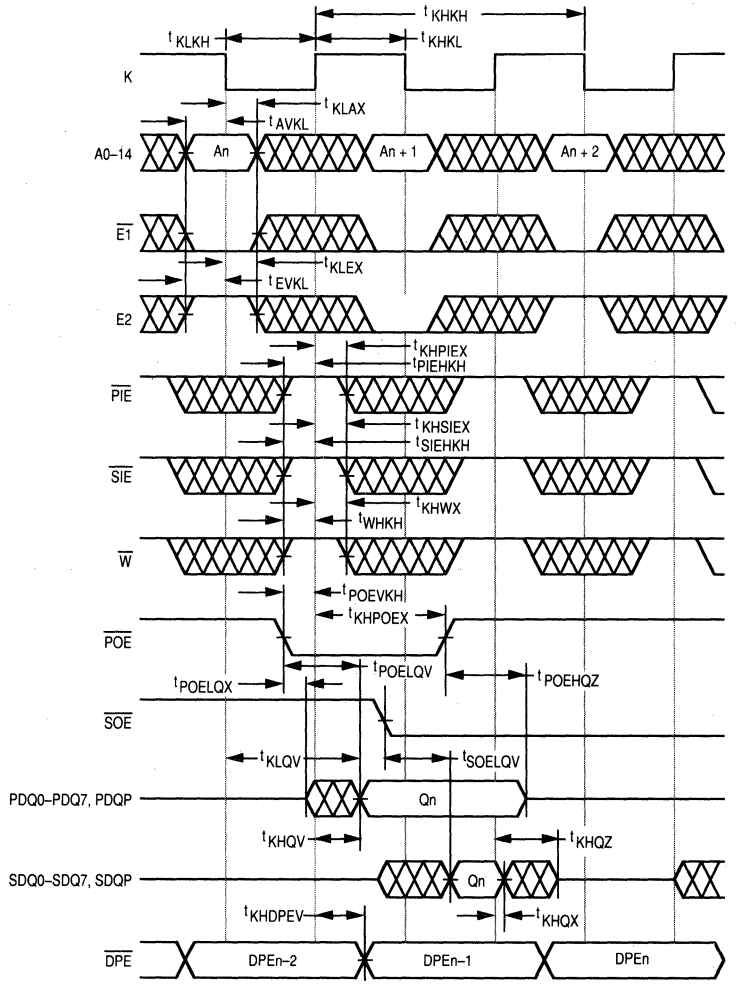
Read Cycle (See Note 1)

Parameter	Symbol	MCM62110-15 Min	MCM62110-15 Max	MCM62110-20 Min	MCM62110-20 Max	Unit	Notes
Read Cycle Time Clock High to Clock High	t_{KHKH}	15	—	20	—	ns	2
Clock Low Pulse Width	t_{KLKH}	5	—	5	—	ns	
Clock High Pulse Width	t_{KHKL}	7	—	7	—	ns	
Clock Access Time Clock Low to Output Valid	t_{KLQV}	—	15	—	20	ns	3, 4
Clock High to $\overline{DPE}$ Valid	t_{KHDPEV}	—	8	—	10	ns	5
Clock High to Output Valid	t_{KHQV}	—	8	—	10	ns	4, 6
Output Hold from Clock High	t_{KHQX}	2	—	2	—	ns	4, 7
Clock High to Q High-Z ($\overline{E1}$ or E2 = False)	t_{KHQZ}	—	8	—	10	ns	7
Setup TImes: A	t_{AVKL}	3	—	3	—	ns	
$\overline{W}$	t_{WHKH}						
$\overline{E1}$, E2	t_{EVKL}						
$\overline{PIE}$	t_{PIEHKH}						
$\overline{SIE}$	t_{SIEHKH}						
$\overline{POE}$	t_{POEVKH}						8
$\overline{SOE}$	t_{SOEVKH}						8
Hold Times: A	t_{KLAX}	2	—	2	—	ns	
$\overline{W}$	t_{KHWX}						
$\overline{E1}$, E2	t_{KLEX}						
$\overline{PIE}$	t_{KHPIEX}						
$\overline{SIE}$	t_{KHSIEZ}						
$\overline{POE}$	t_{KHPOEX}						8
$\overline{SOE}$	t_{KHSOEX}						8
Output Enable High to Q High-Z	t_{POEHQZ} t_{SOEHQZ}	0	8	0	9	ns	7
Output Enable Low to Q Active	t_{POELQX} t_{SOELQX}	0	—	0	—	ns	7
Output Enable Low to Output Valid	t_{POELQV} t_{SOELQV}	—	6	—	8	ns	

NOTES:
1. A read is defined by $\overline{W}$ high for the setup and hold times.
2. All read cycle timing is referenced from K, $\overline{SOE}$, or $\overline{POE}$.
3. For Read Cycle 1 timing, clock low pulse width < ($t_{KLQV} - t_{KHQV}$).
4. K must be at a high level for outputs to transition.
5. $\overline{DPE}$ is valid exactly one clock cycle after the output data is valid.
6. For Read Cycle 2 timing, clock low pulse width ≥ ($t_{KLQV} - t_{KHQV}$).
7. Transition is measured ± 500 mV from steady-state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{KHQZ} is less than t_{KHQX}, t_{POEHQZ} is less than t_{POELQX} for a given device, and t_{SOEHQZ} is less than t_{SOELQX} for a given device.
8. These read cycle timings guarantee proper parity operation.

9

READ CYCLE (See Note)



NOTE: $\overline{DPE}$ is valid exactly one clock cycle after the output data is valid.

9

WRITE CYCLE (See Note 1)

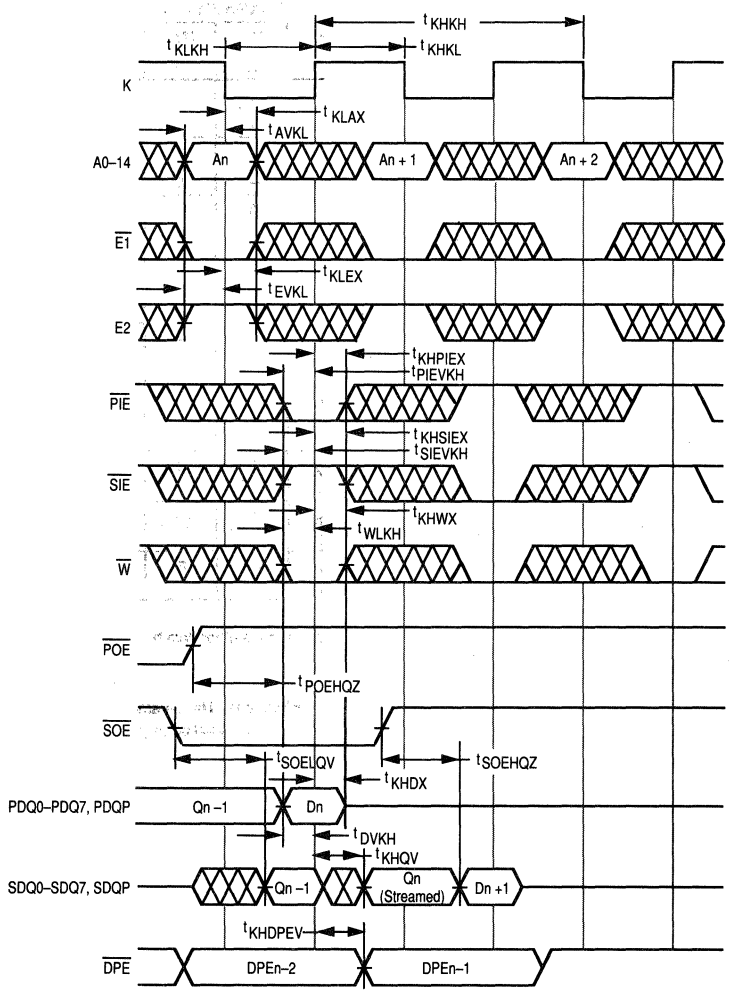
Parameter	Symbol	MCM62110-15		MCM62110-20		Unit	Notes
		Min	Max	Min	Max		
Write Cycle Times	t_{KHKH}	15	—	20	—	ns	2
Clock Low Pulse Width	t_{KLKH}	5	—	5	—	ns	
Clock High Pulse Width	t_{KHKL}	—	7	—	7	ns	
Clock High to $\overline{DPE}$ Valid	t_{KHDPEV}	—	8	—	10	ns	3
Clock High to Output High-Z ($\overline{W} = V_{IL}$ and $\overline{SIE} = \overline{PIE} = V_{IH}$)	t_{KHQZ}	—	8	—	10	ns	4, 5
Setup Times: A	t_{AVKL}	3	—	3	—	ns	
$\overline{W}$	t_{WLKH}						
$\overline{E1}$, E2	t_{EVKL}						
$\overline{PIE}$	t_{PIEVKH}						
$\overline{SIE}$	t_{SIEVKH}						
SDQ0–SDQ7, SDQP, PDQ0–PDQ7, PDQP	t_{DVKH}						
Hold Times: A	t_{KLAX}	2	—	2	—	ns	
$\overline{W}$	t_{KHWX}						
$\overline{E1}$, E2	t_{KLEX}						
$\overline{PIE}$	t_{KHPIEX}						
$\overline{SIE}$	t_{KHSIEX}						
SDQ0–SDQ7, SDQP, PDQ0–PDQ7, PDQP	t_{KHDX}						
Write with Streaming ($\overline{PIE} = \overline{SOE} = V_{IL}$ or $\overline{SIE} = \overline{POE} = V_{IL}$) Clock High to Output Valid	t_{KHQV}	—	8	—	8	ns	6

NOTES:

1. A write is performed with $\overline{W} = V_{IL}$, $\overline{E1} = V_{IL}$, $E2 = V_{IH}$ for the specified setup and hold times and either $\overline{PIE} = V_{IL}$ or $\overline{SIE} = V_{IL}$. If both $\overline{PIE} = V_{IL}$ and $\overline{SIE} = V_{IL}$ or $\overline{PIE} = V_{IH}$ and $\overline{SIE} = V_{IH}$, then this is treated like a NOP and no write is performed.
2. All write cycle timings are referenced from K.
3. $\overline{DPE}$ is valid exactly one clock cycle after the data is written.
4. K must be at a high level for the outputs to transition.
5. Transition is measured ±500 mV from steady-state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{KHQZ} is less than t_{KHQX} for a given device.
6. A write with streaming is defined as a write cycle which writes data from one data bus to the array and outputs the same data onto the other data bus.

9

WRITE CYCLE (See Note)



NOTE: $\overline{DPE}$ is valid exactly one clock cycle after the output data is written.

STREAM CYCLE (See Note 1)

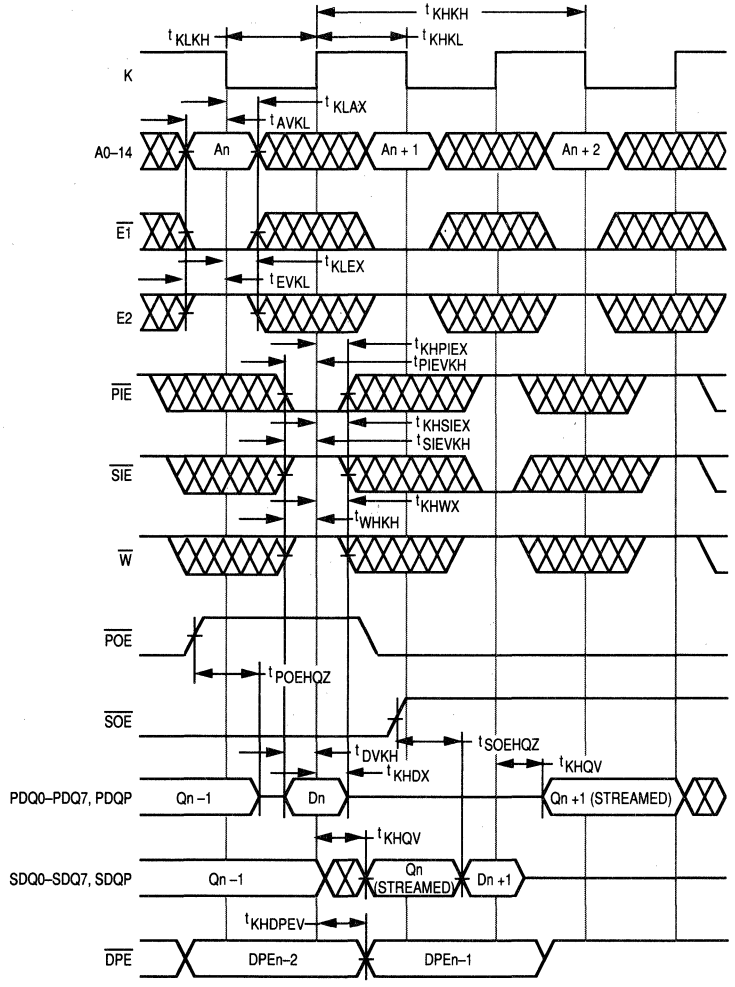
Parameter	Symbol	MCM62110-15		MCM62110-20		Unit	Notes
		Min	Max	Min	Max		
Stream Cycle Time	t_{KHKH}	15	—	20	—	ns	2
Clock Low Pulse Width	t_{KLKH}	5	—	5	—	ns	
Clock High Pulse Width	t_{KHKL}	7	—	7	—	ns	
Stream Access Time	t_{KHQV}	—	8	—	8	ns	
Clock High to $\overline{DPE}$ Valid	t_{KHDPEV}	—	8	—	10	ns	3
Setup Times: A	t_{AVKL}	3	—	3	—	ns	
$\overline{W}$	t_{WHKH}						
$\overline{E1}$, E2	t_{EVKL}						
$\overline{PIE}$	t_{PIEVKH}						
$\overline{SIE}$	t_{SIEVKH}						
SDQ0–SDQ7, SDQP, PDQ0–PDQ7, PDQP	t_{DVKH}						
Hold Times: A	t_{KLAX}	2	—	2	—	ns	
$\overline{W}$	t_{KHWX}						
$\overline{E1}$, E2	t_{KLEX}						
$\overline{PIE}$	t_{KHPIEX}						
$\overline{SIE}$	t_{KHSIEX}						
SDQ0–SDQ7, SDQP, PDQ0–PDQ7, PDQP	t_{KHDX}						
Output Enable High to Q High-Z	t_{POEHQZ} t_{SOEHQZ}	0	8	0	9	ns	4
Output Enable Low to Q Active	t_{POELQX} t_{SOELQX}	0	—	0	—	ns	4
Output Enable Low to Output Valid	t_{POELQV} t_{SOELQV}	—	6	—	8	ns	

NOTES:

1. A stream cycle is defined as a cycle where data is passed from one data bus to the other data bus.
2. All stream cycle timing is referenced from K.
3. $\overline{DPE}$ is valid exactly one clock cycle after the data outputs are valid.
4. Transition is measured ±500 mV from steady-state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{POEHQZ} is less than t_{POELQX}, t_{SOEHQZ} is less than t_{SOELQX}, and t_{KHQZ} is less than t_{KHQX} for a given device.

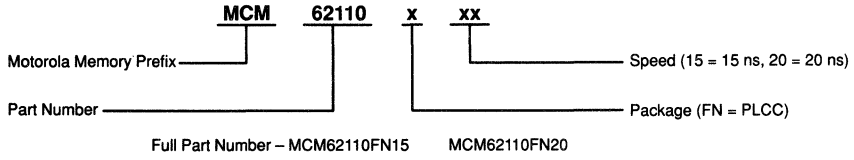
9

STREAM CYCLE (See Note)



NOTE: $\overline{DPE}$ is valid exactly one clock cycle after the output data is valid.

ORDERING INFORMATION
(Order by Full Part Number)



Full Part Number – MCM62110FN15 MCM62110FN20

MCM62350

4K × 4 Bit Cache Address Tag Comparator

with System Status Bit Functions

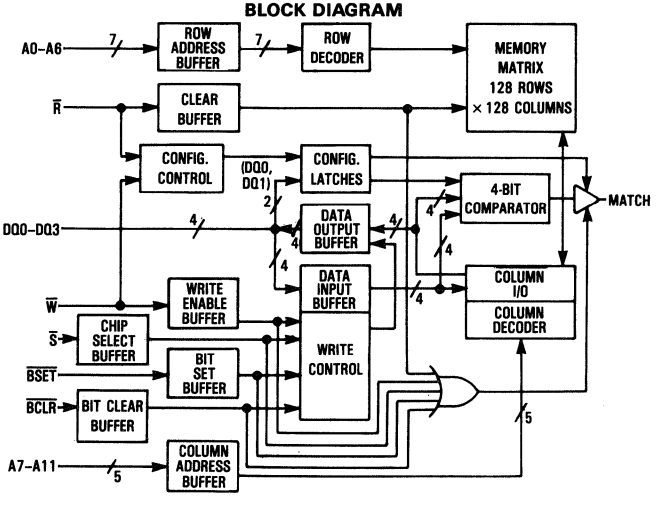
The MCM62350 is a 16,384 bit cache address tag comparator organized as 4096 tags of 4 bits, fabricated using Motorola's high-performance silicon-gate CMOS technology. The device integrates a 4K × 4 SRAM core, an on-board comparator, and special pin functions for tag valid and system status bit applications. These functions allow easy interface to the MC68020 and MC68030 microprocessors, or any other environment where efficient implementation of external cache memory is required. The MCM62350 is available in 24 lead plastic DIP and SOJ packages.

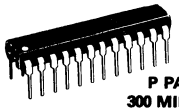
The device has a reset ($\overline{R}$) pin for flash clear of the RAM within two minimum cycles. This function is useful for system initialization. Individual bits within a tag field can be set or cleared via the $\overline{BSET}$ and $\overline{BCLR}$ control input pins for valid bit updates.

The MCM62350 has two configurable comparator modes. The comparator can be configured as standard XNOR (exclusive NOR) for address tag comparison, or AOI (AND-OR-Invert) for determining whether specific bits in the 4-bit word are set (for system status bit applications). In addition, the MATCH output can be programmed as true high or true low for potential logic delay savings. The configuration of these modes is accomplished by performing a write cycle with the $\overline{R}$ pin held low.

- Single 5 V ±10% Power Supply
- Fast Address to MATCH Time; 20/22/25 ns max
- Fast Data to MATCH Time; 10/10/12 ns max
- Fast Read of Tag RAM Contents; 22/25/30 ns max
- Flash Clear of the Tag RAM
- Programmable Active Output Level of MATCH
- Bit Manipulation of Tags via $\overline{BSET}$ and $\overline{BCLR}$ Writes
- Configurable Comparator Modes:
  - XNOR Mode for Address Tag Comparison
  - AOI Mode for System Valid Bit Comparison

BLOCK DIAGRAM

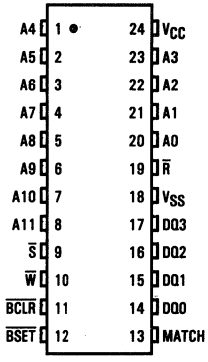




P PACKAGE
300 MIL PLASTIC
CASE 724

J PACKAGE
300 MIL SOJ
CASE 810A

PIN ASSIGNMENT



PIN NAMES	
A0-A11	Address Inputs
$\overline{W}$	Write Enable
$\overline{S}$	Chip Select
$\overline{BCLR}$	Bit Clear Control Input
$\overline{BSET}$	Bit Set Control Input
$\overline{R}$	Reset (Flash Clear) Input
MATCH	MATCH (Hit) Output
DQ0-DQ3	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

9

SIGNAL DESCRIPTIONS

A0-A11—ADDRESS INPUTS

The address lines are used for indexing into the tag RAM portion of the chip.

DQ0-DQ3—DATA INPUT/OUTPUT

The data lines are used as input for compare, write, and configuration cycles, and as output for read cycles.

$\overline{BSET}$—BIT SET CONTROL INPUT

This control signal is used for ORing data into the tag RAM during $\overline{BSET}$ write cycles. Independent bits within the tag can be set using the appropriate mask, as indicated in the bit set truth table. The $\overline{BSET}$ input can also be used to initiate a read cycle.

$\overline{BCLR}$—BIT CLEAR CONTROL INPUT

This control signal is used for ANDing the complement of data into the tag RAM during $\overline{BCLR}$ write cycles. Independent bits within the tag can be cleared using the appropriate mask, as indicated in the bit clear truth table. The $\overline{BCLR}$ input can also be used to initiate a read cycle (note that at least one of the $\overline{BSET}$/$\overline{BCLR}$ signals must be asserted to trigger a read cycle).

$\overline{R}$—RESET (FLASH CLEAR) INPUT

The reset control signal is used to initiate a clear cycle or a configuration cycle.

$\overline{S}$—CHIP SELECT

This control signal is used to chip select the device.

$\overline{W}$—WRITE ENABLE

The write enable signal is used to initiate write cycles.

MATCH—MATCH (HIT) OUTPUT

This output signal is used to indicate a match of DQ0-DQ3 inputs with the contents of the tag RAM addressed by A0—A11.

FUNCTIONAL TRUTH TABLE

$\overline{S}$	$\overline{W}$	$\overline{BCLR}$	$\overline{BSET}$	$\overline{R}$	DQ0-DQ3	MATCH	Cycle
L	H	H	H	H	Compare D_{in}	Valid	Compare
L	H	L	X	H	Read D_{out}	Assert	Read
L	H	X	L	H	Read D_{out}	Assert	Read
L	L	H	H	H	Write D_{in}	Assert	Write
L	L	L	H	H	Bit Clear Mask	Assert	$\overline{BCLR}$ Write
L	L	H	L	H	Bit Set Mask	Assert	$\overline{BSET}$ Write
X	H	X	X	L	High-Z	Assert	Clear (Reset)
L	L	X	X	L	Config D_{in}*	Assert	Configuration
H	X	X	X	H	High-Z	Assert	Deselect

*DQ2 and DQ3 are don't cares during a configuration cycle.

9

COMPARATOR BEHAVIORAL TABLE

Type	DQ0	DQ1	DQ2	DQ3	RAMQ0	RAMQ1	RAMQ2	RAMQ3	MATCH
XNOR	Q0	Q1	Q2	Q3	Q0	Q1	Q2	Q3	1
XNOR	$\overline{Q0}$	Q1	Q2	Q3	Q0	Q1	Q2	Q3	0
AOI	Q0	Q1	Q2	Q3	Q0	Q1	Q2	Q3	1
AOI	L	Q1	Q2	Q3	X	Q1	Q2	Q3	1
AOI	H	Q1	Q2	Q3	L	Q1	Q2	Q3	0

L = Low
H = High
0 = False
1 = True
X = Don't Care

BIT CLEAR TRUTH TABLE (See Note)

Data In	Initial Stored Data	Final Stored Data	
0	0	0	Bit
0	1	1	Unchanged
1	0	0	Bit Cleared
1	1	0	to "Zero"

BIT SET TRUTH TABLE (See Note)

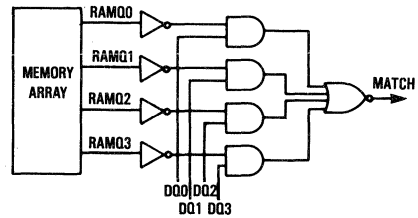
Data In	Initial Stored Data	Final Stored Data	
0	0	0	Bit
0	1	1	Unchanged
1	0	1	Bit Set
1	1	1	to "One"

NOTE: These tables reflect the behavior of single bit positions. The four bits in the tag can all be set or cleared in tandem, or bits within the tag can be independently set or cleared with the appropriate mask.

CONFIGURATION TABLE

DQ0	DQ1	Comparator Type	Match True Level
L	L	XNOR	Low
L	H	XNOR	High
H	L	AOI	Low
H	H	AOI	High

AOI COMPARATOR LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Voltages referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}/V_{out}	−0.5 to V_{CC}+0.5	V
Output Current MATCH Output I/O Pins, Per I/O	I_{out}	±40 ±20	mA
Power Dissipation (T_A = 25°C)	P_D	1.0	W
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Temperature Under Bias	T_{bias}	−10 to +85	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

The power supply (V_{CC}) should be stable for at least 100 μs before operating the device. During this inverval, the part will internally configure itself for XNOR compares, with the MATCH output active high. In addition, the memory array of RAM bits will be cleared.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	–	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	−0.5*	–	0.8	V

*V_{IL} min = −0.5 V dc; V_{IL} min = −3.0 V ac (pulse width ≤20 ns)

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	–	±1.0	μA
Output Leakage Current, Except MATCH Output ($\overline{S}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	–	±1.0	μA
AC Supply Current (All Inputs = V_{IL} or V_{IH}, I_{out} = 0 mA, Cycle Time ≥ t_{AVAV} min)	I_{CCA}	–	140*	mA
Output Low Voltage (I/O Pins: I_{OL} = 8.0 mA, MATCH Output: I_{OL} = 12.0 mA)	V_{OL}	–	0.4	V
Output High Voltage (I/O Pins: I_{OH} = −4.0 mA, MATCH Output: I_{OH} = −10.0 mA)	V_{OH}	2.4	–	V

*I_{CC} active current for the clear cycle exceeds this specification. However, this is a transient phenomenon and will not affect the power dissipation of the device. Good decoupling of the local power supply should always be used.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	4	5	pF
I/O Capacitance	C_{out}	5	7	pF
MATCH Output Capacitance	C_{match}	6	7	pF

AC TEST LOADS

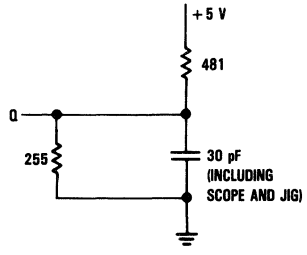


Figure 1a

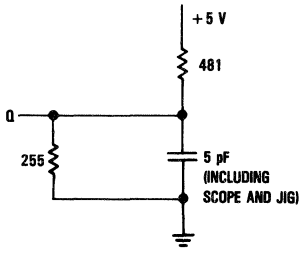


Figure 1b

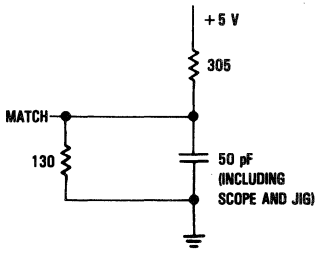


Figure 1c

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level	1.5 V	Output Timing Measurement Reference Level	1.5 V
Input Pulse Levels	0 to 3.0 V	Output Load (I/O Pins)	See Figure 1a
Input Rise/Fall Time	5 ns	Output Load (MATCH Output)	See Figure 1c

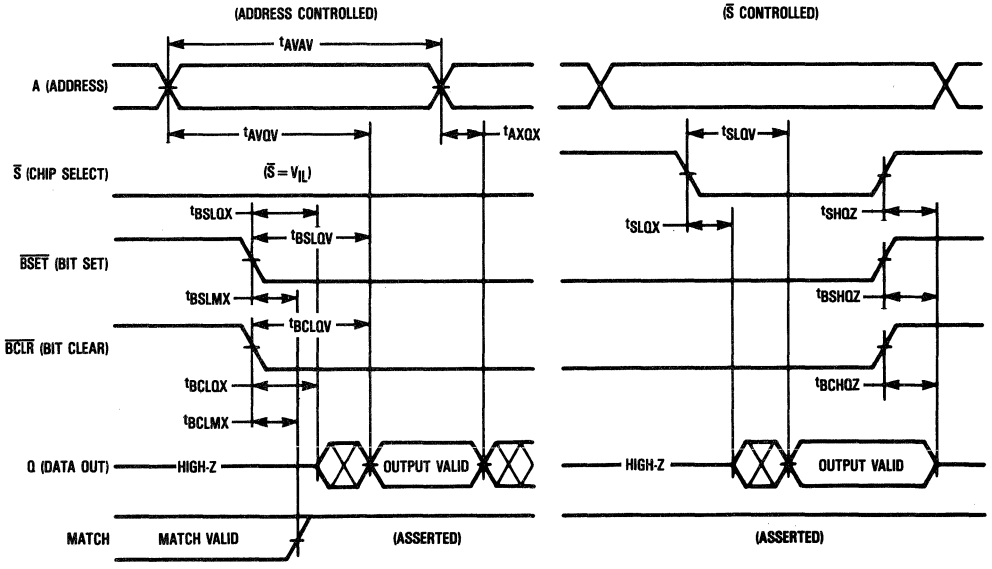
READ CYCLE (See Notes 1 and 2)

Characteristic	Symbol		MCM62350-20		MCM62350-22		MCM62350-25		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	22	–	25	–	30	–	ns	
Address Access Time	t_{AVQV}	t_{AA}	–	22	–	25	–	30	ns	
Select Access Time	t_{SLQV}	t_{ACS}	–	11	–	12	–	15	ns	
$\overline{BCLR}$ Access Time	t_{BCLQV}	t_{ABC}	–	22	–	25	–	30	ns	3
$\overline{BSET}$ Access Time	t_{BSLQV}	t_{ABS}	–	22	–	25	–	30	ns	3
Output Hold from Address Change	t_{AXQX}	t_{OH}	0	–	0	–	0	–	ns	
Select Low to Output Active	t_{SLQX}	t_{CSL}	5	–	5	–	5	–	ns	4
$\overline{BSET}$/$\overline{BCLR}$ Low to Output Active	t_{BSLQX}/t_{BCLQX}	t_{LZ}	7	–	10	–	10	–	ns	4
$\overline{S}$ High to Output High-Z	t_{SHQZ}	t_{CSZ}	–	8	–	9	–	10	ns	4
$\overline{BSET}$/$\overline{BCLR}$ High to Output High-Z	t_{BSHQZ}/t_{BCHQZ}	t_{HZ}	–	8	–	9	–	10	ns	4
$\overline{BSET}$/$\overline{BCLR}$ Low to MATCH Assert	t_{BSLMX}/t_{BCLMX}	t_{CH}	0	15	0	15	0	18	ns	

NOTES:
1. $\overline{R} = V_{IH}$, $\overline{W} = V_{IH}$ continuously during read cycles. One of either $\overline{BSET}$ or $\overline{BCLR}$ pins must be asserted low to activate the outputs. The MATCH output becomes asserted when either the $\overline{BSET}$ or $\overline{BCLR}$ pin transitions low.
2. MATCH assertion is always shown high for distinction between asserted and valid.
3. For brevity in signal names, BC is used to represent $\overline{BCLR}$ transitions, while BS is used to represent $\overline{BSET}$ transitions.
4. Transition is measured ±500 mV from steady state voltage with load of Figure 1b. This parameter is sampled and not 100% tested.

9

READ CYCLE

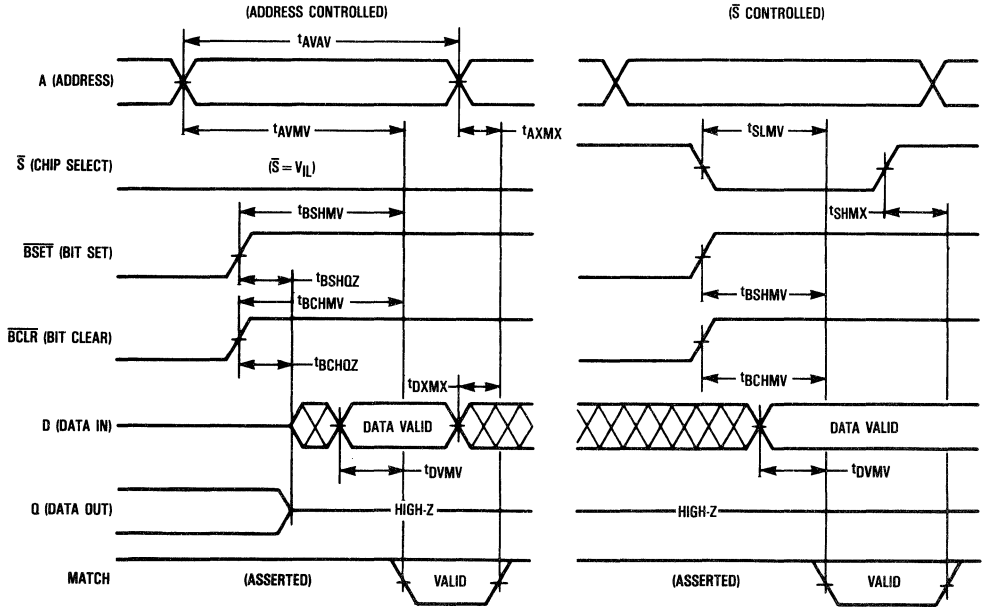


COMPARE CYCLE (See Notes 1 and 2)

Characteristic	Symbol		MCM62350-20		MCM62350-22		MCM62350-25		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Compare Cycle Time	t_{AVAV}	t_C	22	–	25	–	30	–	ns	
Address Valid to MATCH Valid	t_{AVMV}	t_{ACA}	–	20	–	22	–	25	ns	
$\overline{BCLR}$ High to MATCH Valid	t_{BCHMV}	t_{BCCA}	–	15	–	15	–	18	ns	3
$\overline{BSET}$ High to MATCH Valid	t_{BSHMV}	t_{BSCA}	–	15	–	15	–	18	ns	3
Data Valid to MATCH Valid	t_{DVMV}	t_{DCA}	–	10	–	10	–	12	ns	
$\overline{S}$ Low to MATCH Valid	t_{SLMV}	t_{CSCA}	–	12	–	15	–	18	ns	
MATCH Hold from Address Change	t_{AXMX}	t_{ACH}	5	–	5	–	5	–	ns	
MATCH Hold from Data Change	t_{DXMX}	t_{DCH}	3	–	3	–	3	–	ns	
$\overline{S}$ High to MATCH Assert	t_{SHMX}	t_{CH}	0	10	0	10	0	12	ns	
$\overline{BCLR}$ High to Output High-Z	t_{BCHQZ}	t_{BCZ}	–	8	–	9	–	10	ns	4
$\overline{BSET}$ High to Output High-Z	t_{BSHQZ}	t_{BSZ}	–	8	–	9	–	10	ns	4

NOTES:
1. $\overline{R} = V_{IH}$, $\overline{W} = V_{IH}$ continuously during compare cycles.
2. MATCH assertion is always shown high for distinction between asserted and valid.
3. For brevity in signal names, BC is used to represent $\overline{BCLR}$ transitions, while BS is used to represent $\overline{BSET}$ transitions.
4. Transition is measured ±500 mV from steady state voltage with load of Figure 1b. This parameter is sampled and not 100% tested.

COMPARE CYCLE

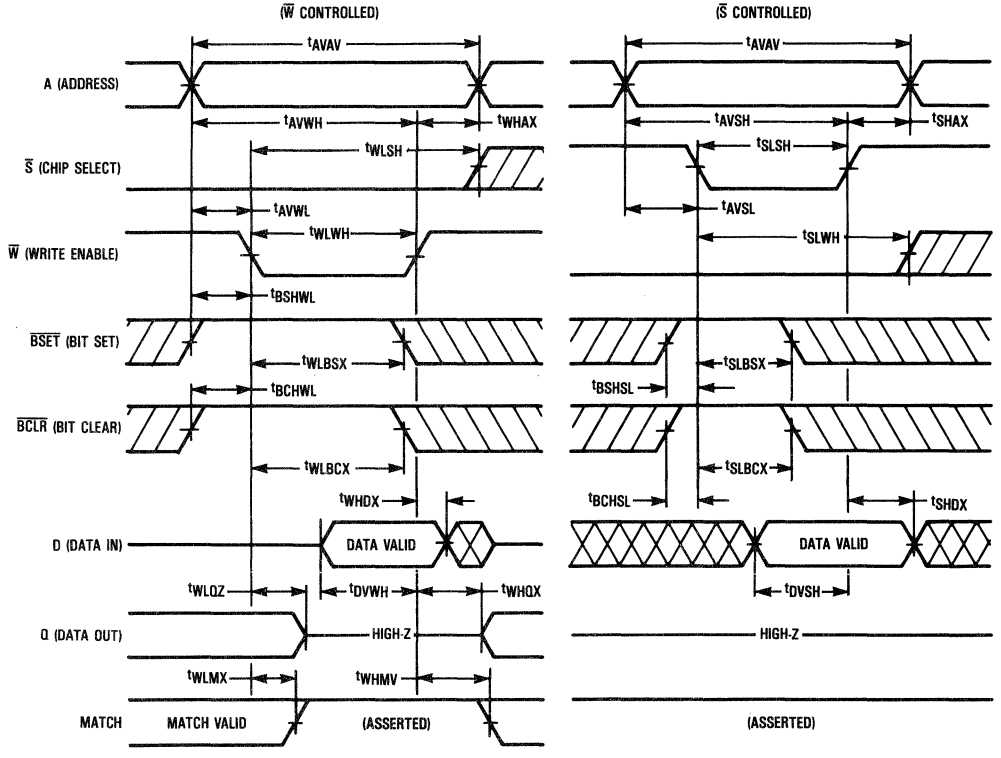


STANDARD WRITE CYCLE (See Notes 1 and 2)

Characteristic	Symbol		MCM62350-20		MCM62350-22		MCM62350-25		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	22	—	25	—	30	—	ns	
Write Pulse Width	t_{WLWH}/t_{SLSH} t_{WLSH}/t_{SLWH}	t_{WP} t_{WP}	14	—	18	—	20	—	ns	
Address Setup to Beginning of Write	t_{AVWL}/t_{AVSL}	t_{AS}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}/t_{AVSH}	t_{AW}	16	—	18	—	20	—	ns	
Data Valid to End of Write	t_{DVWH}/t_{DVSH}	t_{DW}	10	—	10	—	12	—	ns	
Data Hold from Write End	t_{WHDX}/t_{SHDX}	t_{DH}	0	—	0	—	0	—	ns	
Write Low to Output High-Z	t_{WLQZ}	t_{WZ}	—	8	—	9	—	10	ns	3, 4
Address Hold from Write End	t_{WHAX}/t_{SHAX}	t_{WR}	0	—	0	—	0	—	ns	
Write Low to MATCH Assert	t_{WLMX}	t_{WCH}	0	15	0	15	0	15	ns	4
$\overline{BSET}/\overline{BCLR}$ Setup to Beginning of Write	t_{BSHWL}/t_{BSHSL} t_{BCHWL}/t_{BCHSL}	t_{BSS} t_{BCS}	−1	—	−1	—	−1	—	ns	
$\overline{BSET}/\overline{BCLR}$ Hold Time from Write Start	t_{WLBSX}/t_{SLBSX} t_{WLBCX}/t_{SLBCX}	t_{BSH} t_{BCH}	10	—	10	—	10	—	ns	
Write High to MATCH Valid	t_{WHMV}	t_{WCA}	—	20	—	22	—	25	ns	4
Write High to Output Active	t_{WHQX}	t_{OW}	3	—	5	—	5	—	ns	3, 4

NOTES:
1. A standard write occurs during the overlap of $\overline{W}$ and $\overline{S}$ low and $\overline{BSET}$ and $\overline{BCLR}$ high. The $\overline{R}$ pin is high continuously during a write cycle.
2. MATCH assertion is always shown high for distinction between asserted and valid.
3. Transition is measured ±500 mV from steady state voltage with load of Figure 1b. This parameter is sampled and not 100% tested.
4. Both the MATCH output and Q0-Q3 are shown as valid in the $\overline{W}$ controlled cycle below to convey their timing relative to $\overline{W}$. In reality, only one of either MATCH or Q0-Q3 can be valid at one time, as determined by $\overline{BSET}$ and $\overline{BCLR}$ inputs.

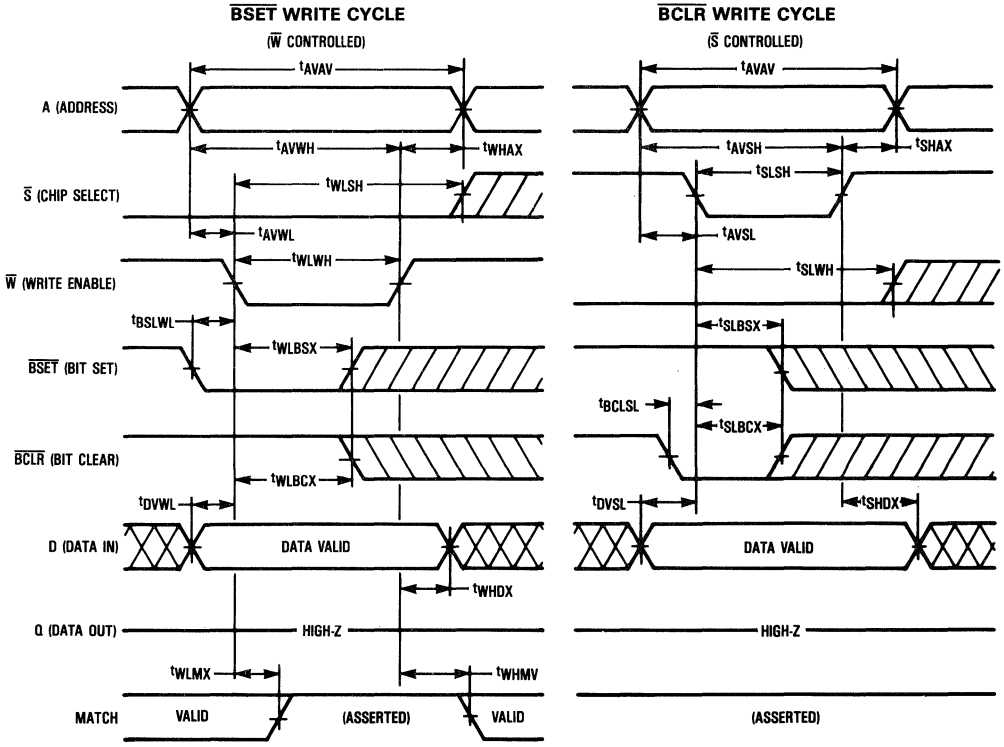
STANDARD WRITE CYCLE



$\overline{BSET}/\overline{BCLR}$ WRITE CYCLE (See Notes 1 and 2)

Characteristic	Symbol		MCM62350-20		MCM62350-22		MCM62350-25		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	22	–	25	–	30	–	ns	
Write Pulse Width	t_{WLWH}/t_{SLSH} t_{WLSH}/t_{SLWH}	t_{WP} t_{WP}	14	–	18	–	20	–	ns	
Address Setup to Beginning of Write	t_{AVWL}/t_{AVSL}	t_{AS}	0	–	0	–	0	–	ns	
Address Valid to End of Write	t_{AVWH}/t_{AVSH}	t_{AW}	14	–	18	–	20	–	ns	
Data Setup to Beginning of Write	t_{DVWL}/t_{DVSL}	t_{DS}	0	–	−1	–	−1	–	ns	3
Data Hold from Write End	t_{WHDX}/t_{SHDX}	t_{DH}	0	–	0	–	0	–	ns	
Address Hold from Write End	t_{WHAX}/t_{SHAX}	t_{WR}	0	–	0	–	0	–	ns	
$\overline{W}$ Low to MATCH Assert	t_{WLMX}	t_{WCH}	0	15	0	15	0	15	ns	
$\overline{BSET}/\overline{BCLR}$ Setup to Beginning of Write	t_{BSLWL}/t_{BSLSL} t_{BCLWL}/t_{BCLSL}	t_{BSS} t_{BCS}	−1	–	−1	–	−1	–	ns	3
$\overline{BSET}/\overline{BCLR}$ Hold Time from Write Start	t_{WLBSX}/t_{SLBSX} t_{WLBCX}/t_{SLBCX}	t_{BSH} t_{BCH}	10	–	10	–	10	–	ns	
Write High to MATCH Valid	t_{WHMV}	t_{WCA}	–	20	–	22	–	25	ns	

NOTES:
1. A $\overline{BSET}/\overline{BCLR}$ write occurs during the overlap of $\overline{W}$ and $\overline{S}$ low and $\overline{BSET}$ or $\overline{BCLR}$ low. The $\overline{R}$ pin is high continuously during a write cycle. $\overline{BSET}$ and $\overline{BCLR}$ write cycles can be $\overline{W}$ controlled or $\overline{S}$ controlled. Only two of four possible cycles are shown here for brevity.
2. MATCH assertion is always shown high for distinction between asserted and valid.
3. Data output buffer must be in high-Z prior to start of either $\overline{BSET}$ or $\overline{BCLR}$ write cycles. Note that for $\overline{W}$ controlled cycles, the user must avoid excessive setup time of $\overline{BSET}/\overline{BCLR}$ to avoid bus contention. Data must be set up for t_{DVWL}/t_{DVSL} time to ensure the data integrity of non-modified bits during $\overline{BSET}/\overline{BCLR}$ write cycles. In the event that invalid data is presented for non-modified bits during the $\overline{BSET}/\overline{BCLR}$ write, note that it is not possible to recover the original data state by simply presenting valid data before the end of write.

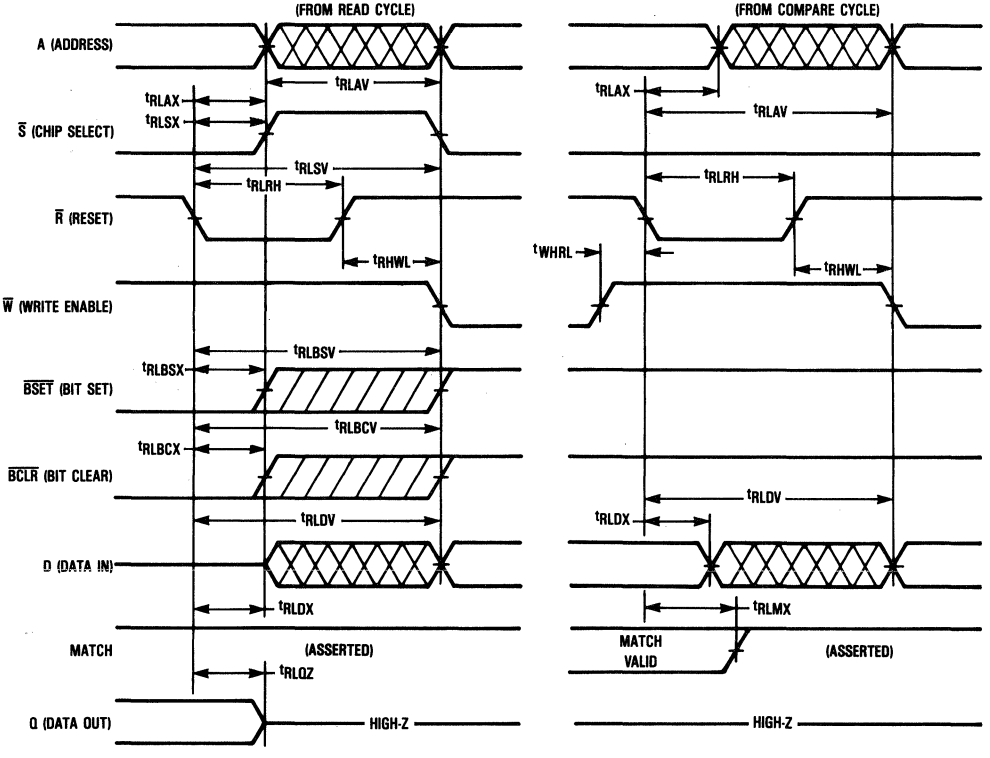


CLEAR CYCLE (See Notes 1 and 2)

Characteristic		Symbol		MCM62350-20		MCM62350-22		MCM62350-25		Unit	Notes
		Standard	Alternate	Min	Max	Min	Max	Min	Max		
$\overline{R}$ Low to Inputs Recognized (Clear Cycle Time)	A	t_{RLAV}	t_{CR}	–	70	–	70	–	70	ns	
	$\overline{S}$	t_{RLSV}	t_{CR}								
	$\overline{BSET}$	t_{RLBSV}	t_{CR}								
	$\overline{BCLR}$	t_{RLBCV}	t_{CR}								
	D	t_{RLDV}	t_{CR}								
$\overline{R}$ Pulse Width		t_{RLRH}	t_{CLP}	22	–	25	–	30	–	ns	
Read Setup to $\overline{R}$ Low		t_{WHRL}	t_{RS}	5	–	5	–	5	–	ns	3
Write Hold from $\overline{R}$ High		t_{RHWL}	t_{WH}	0	–	0	–	0	–	ns	3
$\overline{R}$ Low to Inputs Don't Care	A	t_{RLAX}	t_{CX}	0	–	0	–	0	–	ns	4
	$\overline{S}$	t_{RLSX}	t_{CX}								
	$\overline{BSET}$	t_{RLBSX}	t_{CX}								
	$\overline{BCLR}$	t_{RLBCX}	t_{CX}								
	D	t_{RLDX}	t_{CX}								
$\overline{R}$ Low to MATCH Assert		t_{RLMX}	t_{MH}	0	15	0	15	0	18	ns	
$\overline{R}$ Low to Output High-Z		t_{RLQZ}	t_{CZ}	–	15	–	15	–	18	ns	5

NOTES:
1. The address, $\overline{BSET}$, and $\overline{BCLR}$ inputs are don't cares during a clear cycle.
2. MATCH assertion is always shown high for distinction between asserted and valid.
3. The clear cycle is initiated at the falling edge of $\overline{R}$. The t_{WHRL} and t_{RHWL} parameters must be satisfied to prevent an undesired configuration cycle.
4. "Inputs" for this parameter refers to all inputs except $\overline{W}$.
5. Transition is measured ±500 mV from steady state voltage with load of Figure 1b. This parameter is sampled and not 100% tested.

CLEAR CYCLE

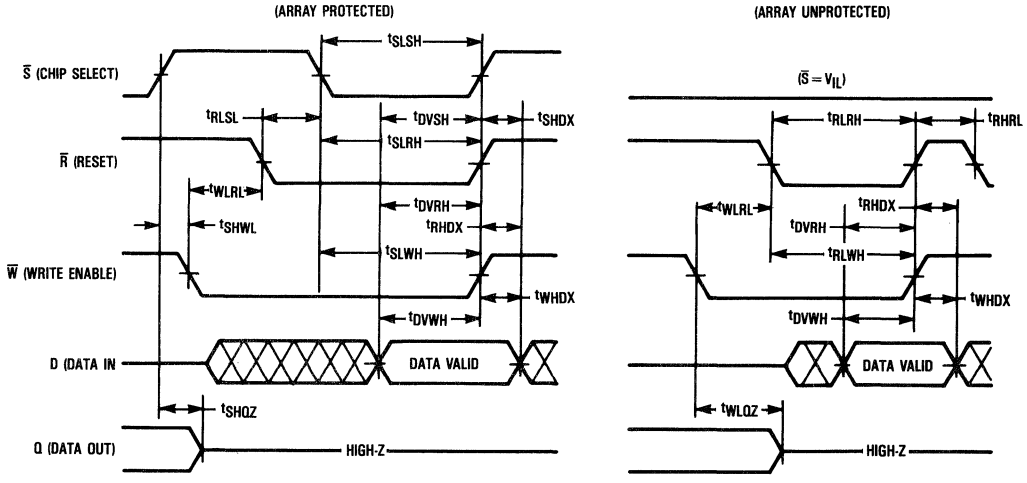


CONFIGURATION CYCLE (See Notes 1 and 2)

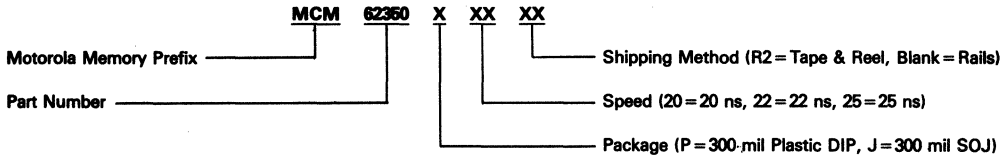
Characteristic		Symbol		MCM62350-20		MCM62350-22		MCM62350-25		Unit	Notes
		Standard	Alternate	Min	Max	Min	Max	Min	Max		
Configuration Control Pulse Width	$\overline{S}$ $\overline{R}$	t_{SLSH} t_{RLRH}	t_{SP} t_{SP}	20	—	22	—	25	—	ns	3
Data Setup to End of Configuration Cycle	$\overline{S}$ $\overline{R}$ $\overline{W}$	t_{DVSH} t_{DVRH} t_{DVWH}	t_{DS} t_{DS} t_{DS}	10	—	10	—	12	—	ns	
Data Hold from End of Configuration Cycle	$\overline{S}$ $\overline{R}$ $\overline{W}$	t_{SHDX} t_{RHDX} t_{WHDX}	t_{DH} t_{DH} t_{DH}	0	—	0	—	0	—	ns	
$\overline{R}$ High Pulse Width		t_{RHRL}	t_{CP}	5	—	5	—	5	—	ns	
Write Setup to $\overline{R}$ Low		t_{WLRL}	t_{WS}	5	—	5	—	5	—	ns	
$\overline{S}$ Setup to End of Configuration		t_{SLWH} t_{SLRH}	t_{SWS} t_{SCS}	20	—	20	—	25	—	ns	4
$\overline{R}$ Setup to End of Configuration		t_{RLWH}	t_{SR}	20	—	20	—	25	—	ns	
$\overline{R}$ Setup to $\overline{S}$ Low		t_{RLSL}	t_{CSS}	5	—	5	—	5	—	ns	3
$\overline{S}$ Setup to Beginning of Write		t_{SHWL}	t_{WSS}	0	—	0	—	0	—	ns	
$\overline{S}$ High to Output High-Z		t_{SHQZ}	t_{HZ}	—	9	—	9	—	10	ns	5
$\overline{W}$ Low to Output High-Z		t_{WLQZ}	t_{HZ}	—	9	—	9	—	10	ns	5

NOTES:
1. A configuration cycle is performed during the overlap of $\overline{W}$ low, $\overline{R}$ low, and $\overline{S}$ low. Address, DQ2, DQ3, $\overline{BSET}$, and $\overline{BCLR}$ inputs are don't cares during configuration cycles.
2. To ensure proper configuration of the device during power up, chip select must be equal to or greater than V_{IH}.
3. A valid configuration can be performed with $\overline{S}$ asserted prior to $\overline{R}$ and $\overline{W}$ low transitions. Be aware, however, that array data may be altered under this condition.
4. Note that terminating the cycle with $\overline{R}$ while leaving $\overline{W}$ and $\overline{S}$ asserted may cause array data to be altered.
5. Transition is measured ±500 mV from steady state voltage with load of Figure 1b. This parameter is sampled and not 100% tested.

CONFIGURATION CYCLE



ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers—	MCM62350P20	MCM62350P22	MCM62350P25
	MCM62350J20	MCM62350J22	MCM62350J25
	MCM62350J20R2	MCM62350J22R2	MCM62350J25R2

9

MCM62351

4K x 4 Bit Cache Address Tag Comparator

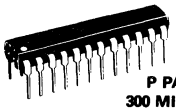
with System Status Bit Functions

The MCM62351 is a 16,384 bit cache address tag comparator organized as 4096 tags of 4 bits, fabricated using Motorola's high-performance silicon-gate CMOS technology. The device integrates a 4K x 4 SRAM core, an on-board comparator, and special pin functions for tag valid and system status bit applications. These functions allow easy interface to the MC68020 and MC68030 microprocessors, or any other environment where efficient implementation of external cache memory is required.

The device has a reset ($\overline{R}$) pin for flash clear of the RAM, which is useful for system initialization. Individual bits within a tag can be set or cleared via the $\overline{BSET}$ and $\overline{BCLR}$ control input pins for valid bit updates.

The MCM62351 has two configurable comparator modes. The comparator can be configured as standard XNOR (exclusive NOR) for address tag comparison, or AOI (AND-OR-Invert) for determining whether specific bits in the 4-bit word are set (for system status applications). The configuration of the comparator is accomplished by performing a write cycle with the $\overline{R}$ pin held low. The MATCH output is open drain, allowing efficient combination of multiple MATCH outputs using a wired-OR connection.

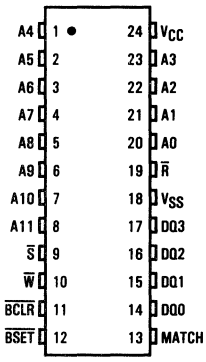
- Single 5 V ±10% Power Supply
- Fast Address to MATCH Time; 20/22/25 ns max
- Fast Data to MATCH Time; 10/10/12 ns max
- Fast Read of Tag RAM Contents; 22/25/30 ns max
- Flash Clear of the Tag RAM
- Open Drain MATCH Output
- Bit Manipulation of Tags via $\overline{BSET}$ and $\overline{BCLR}$ Writes
- Configurable Comparator Modes:
  - XNOR Mode for Address Tag Comparison
  - AOI Mode for System Valid Bit Comparison
- High Board Density SOJ Package Available



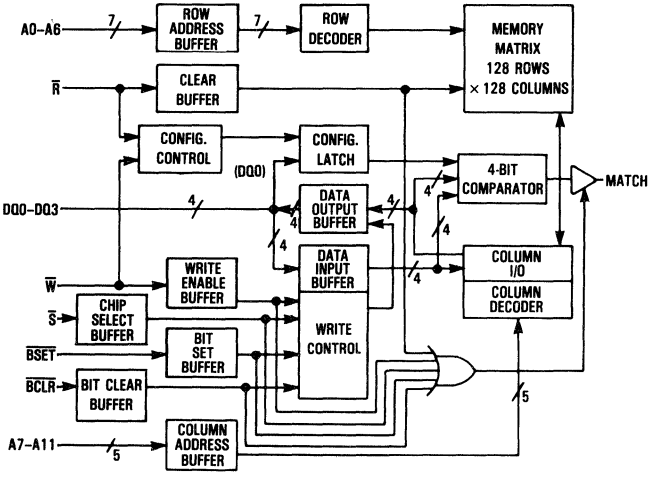
P PACKAGE
300 MIL PLASTIC
CASE 724

J PACKAGE
300 MIL SOJ
CASE 810A

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A0-A11	Address Inputs
$\overline{W}$	Write Enable
$\overline{S}$	Chip Select
$\overline{BCLR}$	Bit Clear Control Input
$\overline{BSET}$	Bit Set Control Input
$\overline{R}$	Reset (Flash Clear) Input
MATCH	MATCH (Hit) Output
DQ0-DQ3	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

9

SIGNAL DESCRIPTIONS

A0-A11—ADDRESS INPUTS

The address lines are used for indexing into the tag RAM portion of the chip.

DQ0-DQ3—DATA INPUT/OUTPUT

The data lines are used as input for compare, write, and configuration cycles, and as output for read cycles.

$\overline{BSET}$—BIT SET CONTROL INPUT

This control signal is used for ORing data into the tag RAM during $\overline{BSET}$ write cycles. Independent bits within the tag can be set using the appropriate mask, as indicated in the bit set truth table. The $\overline{BSET}$ input can also be used to initiate a read cycle.

$\overline{BCLR}$—BIT CLEAR CONTROL INPUT

This control signal is used for ANDing the complement of data into the tag RAM during $\overline{BCLR}$ write cycles. Independent bits within the tag can be cleared using the appropriate mask, as indicated in the bit clear truth table. The $\overline{BCLR}$ input can also be used to initiate a read cycle (note that at least one of the $\overline{BSET}$/$\overline{BCLR}$ signals must be asserted to trigger a read cycle).

$\overline{R}$—RESET (FLASH CLEAR) INPUT

The reset control signal is used to initiate a clear cycle or a configuration cycle.

$\overline{S}$—CHIP SELECT

This control signal is used to chip select the device.

$\overline{W}$—WRITE ENABLE

The write enable signal is used to initiate write cycles.

MATCH—MATCH (HIT) OUTPUT

This output signal is used to indicate a match of DQ0-DQ3 inputs with the contents of the tag RAM addressed by A0—A11.

FUNCTIONAL TRUTH TABLE

$\overline{S}$	$\overline{W}$	$\overline{BCLR}$	$\overline{BSET}$	$\overline{R}$	DQ0-DQ3	MATCH	Cycle
L	H	H	H	H	Compare D_{in}	Valid	Compare
L	H	L	X	H	Read D_{out}	Assert	Read
L	H	X	L	H	Read D_{out}	Assert	Read
L	L	H	H	H	Write D_{in}	Assert	Write
L	L	L	H	H	Bit Clear Mask	Assert	$\overline{BCLR}$ Write
L	L	H	L	H	Bit Set Mask	Assert	$\overline{BSET}$ Write
X	H	X	X	L	High-Z	Assert	Clear (Reset)
L	L	X	X	L	Config D_{in}*	Assert	Configuration
H	X	X	X	H	High-Z	Assert	Deselect

*DQ1, DQ2, and DQ3 are don't cares during a configuration cycle.

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COMPARATOR TRUTH TABLE

Type	DQ0	DQ1	DQ2	DQ3	RAMQ0	RAMQ1	RAMQ2	RAMQ3	MATCH
XNOR	Q0	Q1	Q2	Q3	Q0	Q1	Q2	Q3	1
XNOR	$\overline{Q0}$	Q1	Q2	Q3	Q0	Q1	Q2	Q3	0
AOI	Q0	Q1	Q2	Q3	Q0	Q1	Q2	Q3	1
AOI	L	Q1	Q2	Q3	X	Q1	Q2	Q3	1
AOI	H	Q1	Q2	Q3	L	Q1	Q2	Q3	0

L = Low
H = High
0 = False
1 = True
X = Don't Care

BIT CLEAR TRUTH TABLE (See Note)

Data In	Initial Stored Data	Final Stored Data	
0	0	0	Bit
0	1	1	Unchanged
1	0	0	Bit Cleared
1	1	0	to "Zero"

BIT SET TRUTH TABLE (See Note)

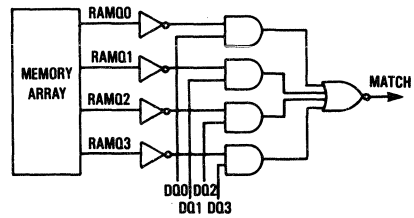
Data In	Initial Stored Data	Final Stored Data	
0	0	0	Bit
0	1	1	Unchanged
1	0	1	Bit Set
1	1	1	to "One"

NOTE: These tables reflect the behavior of single bit positions. The four bits in the tag can all be set or cleared in tandem, or bits within the tag can be independently set or cleared with the appropriate mask.

CONFIGURATION TABLE

DQ0	Comparator Type
L	XNOR
H	AOI

AOI COMPARATOR LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Voltages referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}/V_{out}	−0.5 to V_{CC}+0.5	V
Output Current MATCH Output I/O Pins, Per I/O	I_{out}	±40 ±20	mA
Power Dissipation (T_A = 25°C)	P_D	1.0	W
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Temperature Under Bias	T_{bias}	−10 to +85	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

The power supply (V_{CC}) should be stable for at least 100 μs before operating the device. During this interval, the part will internally configure itself for XNOR compares. In addition, the memory array of RAM bits will be cleared.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

*V_{IL} min = −0.5 V dc; V_{IL} min = −3.0 V ac (pulse width ≤20 ns)

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	±1.0	μA
Output Leakage Current ($\overline{S}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	±1.0	μA
MATCH Output Leakage Current (MATCH Asserted)	$I_{lkg(M)}$	—	±2.0	μA
AC Supply Current (All Inputs = V_{IL} or V_{IH}, I_{out} = 0 mA, Cycle Time ≥ t_{AVAV} min)	I_{CCA}	—	140*	mA
Output Low Voltage (I/O Pins: I_{OL} = 8.0 mA, MATCH Output: I_{OL} = 25.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I/O Pins: I_{OH} = 4.0 mA)	V_{OH}	2.4	—	V

*I_{CC} active current for the clear cycle exceeds this specification. However, this is a transient phenomenon and will not affect the power dissipation of the device. Good decoupling of the local power supply should always be used.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	4	5	pF
I/O Capacitance	C_{out}	5	7	pF
MATCH Output Capacitance	C_{match}	6	7	pF

AC TEST LOADS

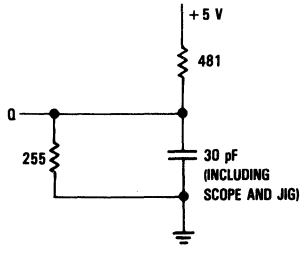


Figure 1a

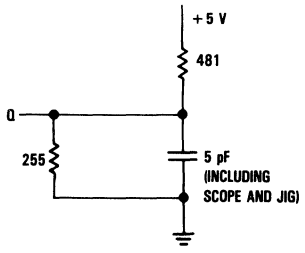


Figure 1b

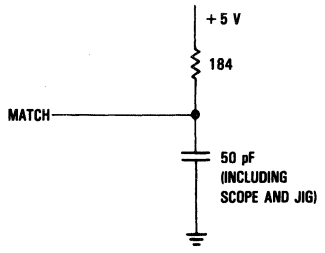


Figure 1c

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . .0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns

Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load (I/O Pins) . . . . . See Figure 1a
Output Load (MATCH Output) . . . . . See Figure 1c

READ CYCLE (See Note 1)

Characteristic	Symbol		MCM62351-20		MCM62351-22		MCM62351-25		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	22	–	25	–	30	–	ns	
Address Access Time	t_{AVQV}	t_{AA}	–	22	–	25	–	30	ns	
Select Access Time	t_{SLQV}	t_{ACS}	–	10	–	12	–	15	ns	
$\overline{BCLR}$ Access Time	t_{BCLQV}	t_{ABC}	–	22	–	25	–	30	ns	2
$\overline{BSET}$ Access Time	t_{BSLQV}	t_{ABS}	–	22	–	25	–	30	ns	2
Output Hold from Address Change	t_{AXQX}	t_{OH}	0	–	0	–	0	–	ns	
Select Low to Output Active	t_{SLQX}	t_{CSL}	5	–	5	–	5	–	ns	3
$\overline{BSET}$/$\overline{BCLR}$ Low to Output Active	t_{BSLQX}/t_{BCLQX}	t_{LZ}	7	–	10	–	10	–	ns	3
$\overline{S}$ High to Output High-Z	t_{SHQZ}	t_{CSZ}	–	8	–	9	–	10	ns	3
$\overline{BSET}$/$\overline{BCLR}$ High to Output High-Z	t_{BSHQZ}/t_{BCHQZ}	t_{HZ}	–	8	–	9	–	10	ns	3
$\overline{BSET}$/$\overline{BCLR}$ Low to MATCH Assert	t_{BSLMX}/t_{BCLMX}	t_{CH}	0	15	0	15	0	18	ns	

NOTES:
1. $\overline{R} = V_{IH}$, $\overline{W} = V_{IH}$ continuously during read cycles. One of either $\overline{BSET}$ or $\overline{BCLR}$ pins must be asserted low to activate the outputs. The MATCH output becomes asserted when either the $\overline{BSET}$ or $\overline{BCLR}$ pin transitions low.
2. For brevity in signal names, BC is used to represent $\overline{BCLR}$ transitions, while BS is used to represent $\overline{BSET}$ transitions.
3. Transition is measured ±500 mV from steady state voltage with load of Figure 1b. This parameter is sampled and not 100% tested.

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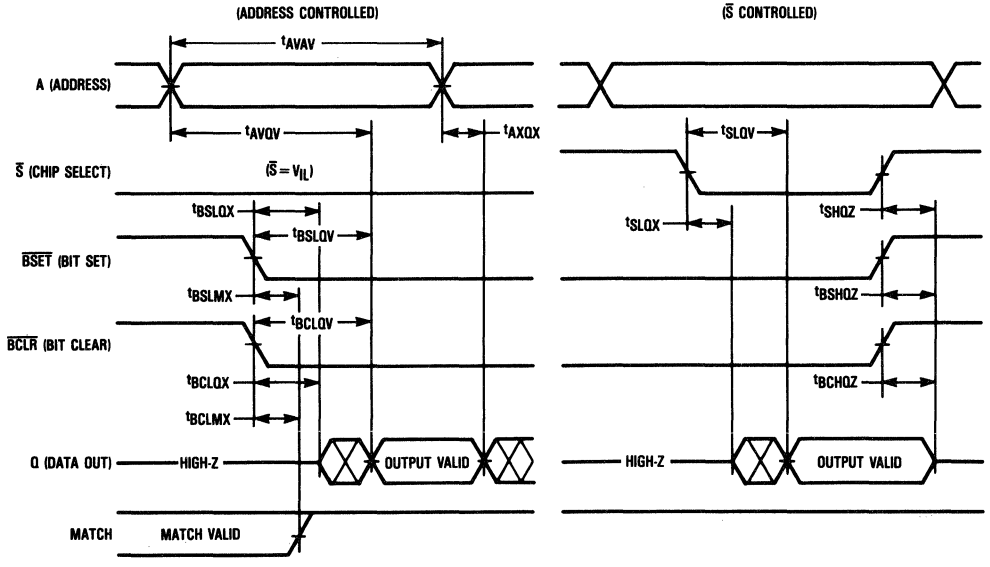
READ CYCLE

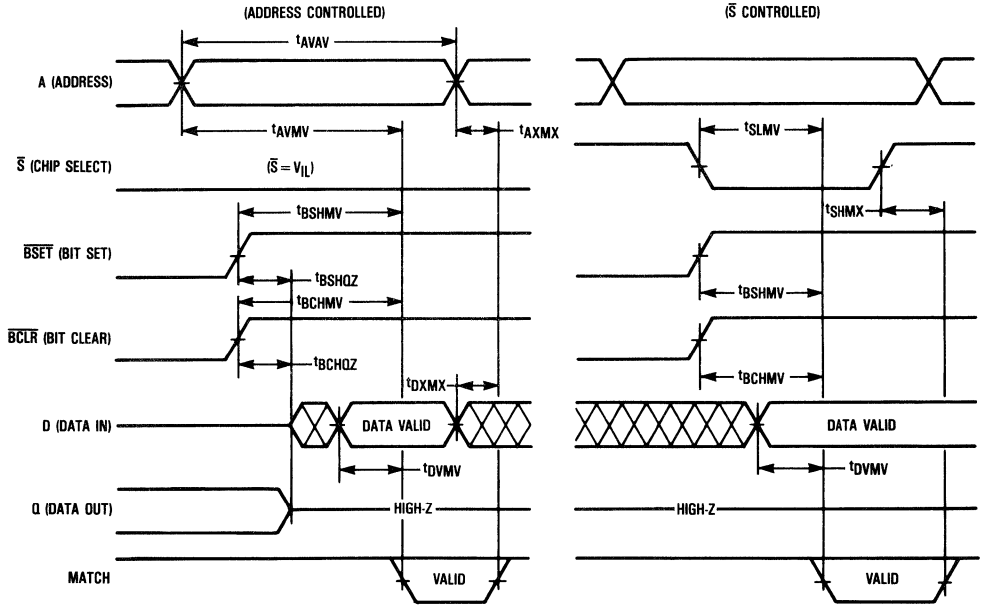


COMPARE CYCLE (See Note 1)

Characteristic	Symbol		MCM62351-20		MCM62351-22		MCM62351-25		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Compare Cycle Time	t_{AVAV}	t_C	22	–	25	–	30	–	ns	
Address Valid to MATCH Valid	t_{AVMV}	t_{ACA}	–	20	–	22	–	25	ns	
$\overline{BCLR}$ High to MATCH Valid	t_{BCHMV}	t_{BCCA}	–	15	–	15	–	18	ns	2
$\overline{BSET}$ High to MATCH Valid	t_{BSHMV}	t_{BSCA}	–	15	–	15	–	18	ns	2
Data Valid to MATCH Valid	t_{DVMV}	t_{DCA}	–	10	–	10	–	12	ns	
$\overline{S}$ Low to MATCH Valid	t_{SLMV}	t_{CSCA}	–	12	–	15	–	18	ns	
MATCH Hold from Address Change	t_{AXMX}	t_{ACH}	5	–	5	–	5	–	ns	
MATCH Hold from Data Change	t_{DXMX}	t_{DCH}	3	–	3	–	3	–	ns	
$\overline{S}$ High to MATCH Assert	t_{SHMX}	t_{CH}	0	10	0	10	0	12	ns	
$\overline{BCLR}$ High to Output High-Z	t_{BCHQZ}	t_{BCZ}	–	8	–	9	–	10	ns	3
$\overline{BSET}$ High to Output High-Z	t_{BSHQZ}	t_{BSZ}	–	8	–	9	–	10	ns	3

NOTES:
1. $\overline{R} = V_{IH}$, $\overline{W} = V_{IH}$ continuously during compare cycles.
2. For brevity in signal names, BC is used to represent $\overline{BCLR}$ transitions, while BS is used to represent $\overline{BSET}$ transitions.
3. Transition is measured ±500 mV from steady state voltage with load of Figure 1b. This parameter is sampled and not 100% tested.

COMPARE CYCLE



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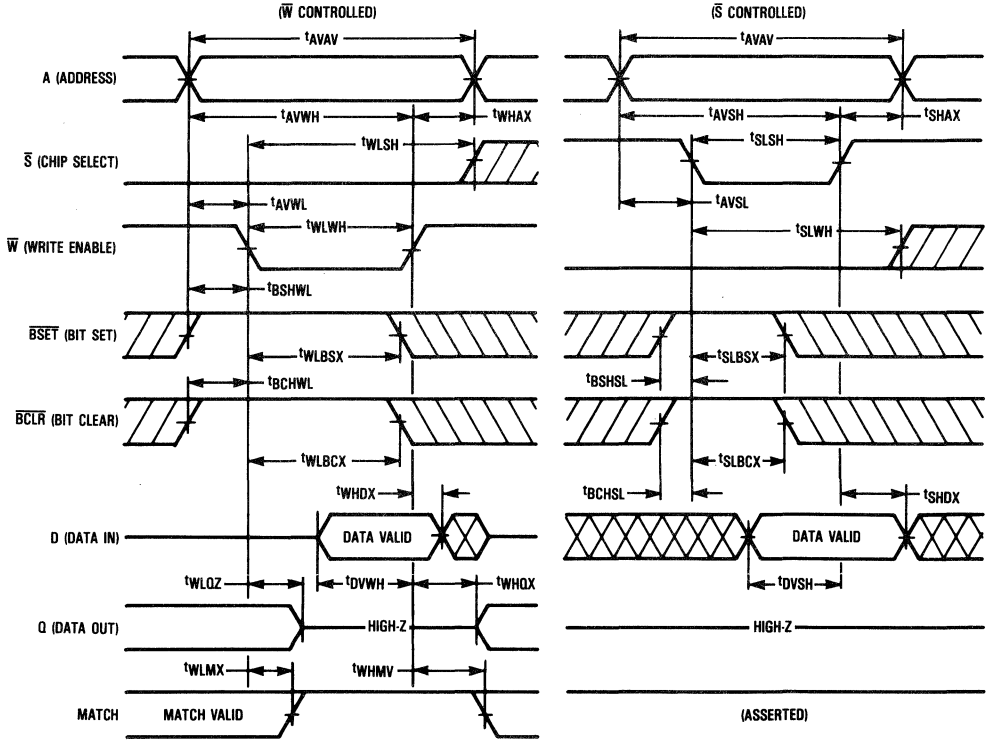
STANDARD WRITE CYCLE (See Note 1)

Characteristic	Symbol		MCM62351-20		MCM62351-22		MCM62351-25		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	22	–	25	–	30	–	ns	
Write Pulse Width	t_{WLWH}/t_{SLSH} t_{WLSH}/t_{SLWH}	t_{WP} t_{WP}	14	–	18	–	20	–	ns	
Address Setup to Beginning of Write	t_{AVWL}/t_{AVSL}	t_{AS}	0	–	0	–	0	–	ns	
Address Valid to End of Write	t_{AVWH}/t_{AVSH}	t_{AW}	16	–	18	–	20	–	ns	
Data Valid to End of Write	t_{DVWH}/t_{DVSH}	t_{DW}	10	–	10	–	12	–	ns	
Data Hold from Write End	t_{WHDX}/t_{SHDX}	t_{DH}	0	–	0	–	0	–	ns	
Write Low to Output High-Z	t_{WLQZ}	t_{WZ}	–	8	–	9	–	10	ns	2, 3
Address Hold from Write End	t_{WHAX}/t_{SHAX}	t_{WR}	0	–	0	–	0	–	ns	
Write Low to MATCH Assert	t_{WLMX}	t_{WCH}	0	15	0	15	0	15	ns	3
$\overline{BSET}/\overline{BCLR}$ Setup to Beginning of Write	t_{BSHWL}/t_{BSHSL} t_{BCHWL}/t_{BCHSL}	t_{BSS} t_{BCS}	−1	–	−1	–	−1	–	ns	
$\overline{BSET}/\overline{BCLR}$ Hold Time from Write Start	t_{WLBSX}/t_{SLBSX} t_{WLBCX}/t_{SLBCX}	t_{BSH} t_{BCH}	10	–	10	–	10	–	ns	
Write High to MATCH Valid	t_{WHMV}	t_{WCA}	–	20	–	22	–	25	ns	3
Write High to Output Active	t_{WHQX}	t_{OW}	3	–	5	–	5	–	ns	2, 3

NOTES:
1. A standard write occurs during the overlap of $\overline{W}$ and $\overline{S}$ low and $\overline{BSET}$ and $\overline{BCLR}$ high. The $\overline{R}$ pin is high continuously during a write cycle.
2. Transition is measured ±500 mV from steady state voltage with load of Figure 1b. This parameter is sampled and not 100% tested.
3. Both the MATCH output and Q0-Q3 are shown as valid in the $\overline{W}$ controlled cycle below to convey their timing relative to $\overline{W}$. In reality, only one of either MATCH or Q0-Q3 can be valid at one time, as determined by $\overline{BSET}$ and $\overline{BCLR}$ inputs.

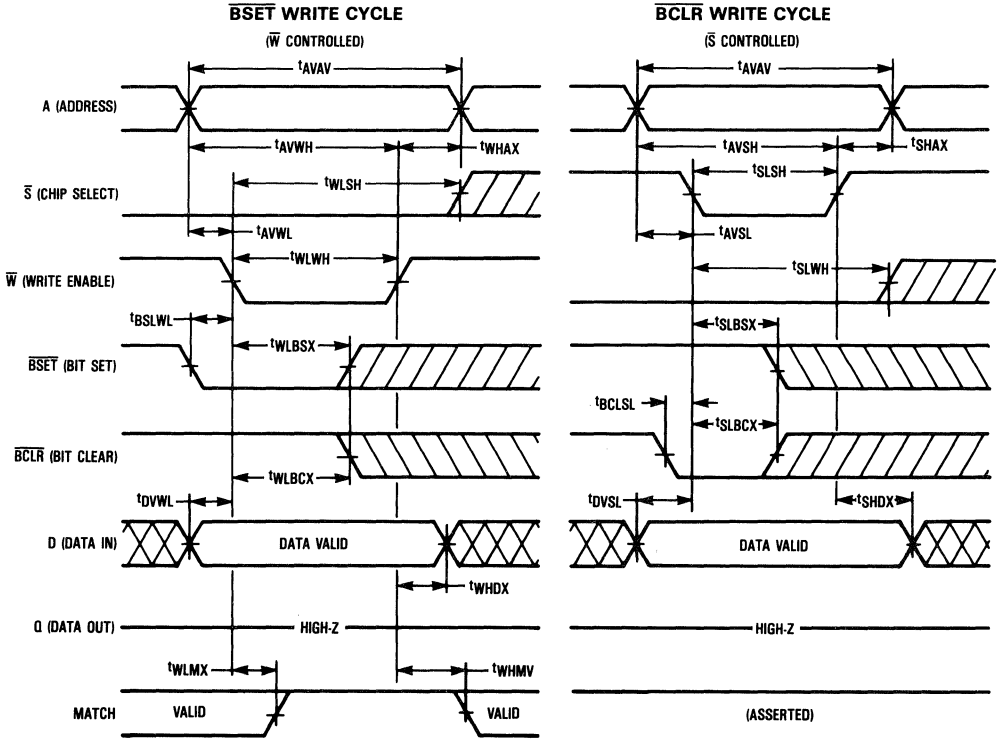
STANDARD WRITE CYCLE



$\overline{BSET}/\overline{BCLR}$ WRITE CYCLE (See Note 1)

Characteristic	Symbol		MCM62351-20		MCM62351-22		MCM62351-25		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	22	–	25	–	30	–	ns	
Write Pulse Width	t_{WLWH}/t_{SLSH} t_{WLSH}/t_{SLWH}	t_{WP} t_{WP}	14	–	18	–	20	–	ns	
Address Setup to Beginning of Write	t_{AVWL}/t_{AVSL}	t_{AS}	0	–	0	–	0	–	ns	
Address Valid to End of Write	t_{AVWH}/t_{AVSH}	t_{AW}	14	–	18	–	20	–	ns	
Data Setup to Beginning of Write	t_{DVWL}/t_{DVSL}	t_{DS}	0	–	−1	–	−1	–	ns	2
Data Hold from Write End	t_{WHDX}/t_{SHDX}	t_{DH}	0	–	0	–	0	–	ns	
Address Hold from Write End	t_{WHAX}/t_{SHAX}	t_{WR}	0	–	0	–	0	–	ns	
$\overline{W}$ Low to MATCH Assert	t_{WLMX}	t_{WCH}	0	15	0	15	0	15	ns	
$\overline{BSET}/\overline{BCLR}$ Setup to Beginning of Write	t_{BSLWL}/t_{BSLSL} t_{BCLWL}/t_{BCLSL}	t_{BSS} t_{BCS}	−1	–	−1	–	−1	–	ns	2
$\overline{BSET}/\overline{BCLR}$ Hold Time from Write Start	t_{WLBSX}/t_{SLBSX} t_{WLBCX}/t_{SLBCX}	t_{BSH} t_{BCH}	10	–	10	–	10	–	ns	
Write High to MATCH Valid	t_{WHMV}	t_{WCA}	–	20	–	22	–	25	ns	

NOTES:
1. A $\overline{BSET}/\overline{BCLR}$ write occurs during the overlap of $\overline{W}$ and $\overline{S}$ low and $\overline{BSET}$ or $\overline{BCLR}$ low. The $\overline{R}$ pin is high continuously during a write cycle. $\overline{BSET}$ and $\overline{BCLR}$ write cycles can be $\overline{W}$ controlled or $\overline{S}$ controlled. Only two of four possible cycles are shown here for brevity.
2. Data output buffer must be in high-Z prior to start of either $\overline{BSET}$ or $\overline{BCLR}$ write cycles. Note that for $\overline{W}$ controlled cycles, the user must avoid excessive setup time of $\overline{BSET}/\overline{BCLR}$ to avoid bus contention. Data must be set up for t_{DVWL}/t_{DVSL} time to ensure the data integrity of non-modified bits during $\overline{BSET}/\overline{BCLR}$ write cycles. In the event that invalid data is presented for non-modified bits during the $\overline{BSET}/\overline{BCLR}$ write, note that it is not possible to recover the original data state by simply presenting valid data before the end of write.



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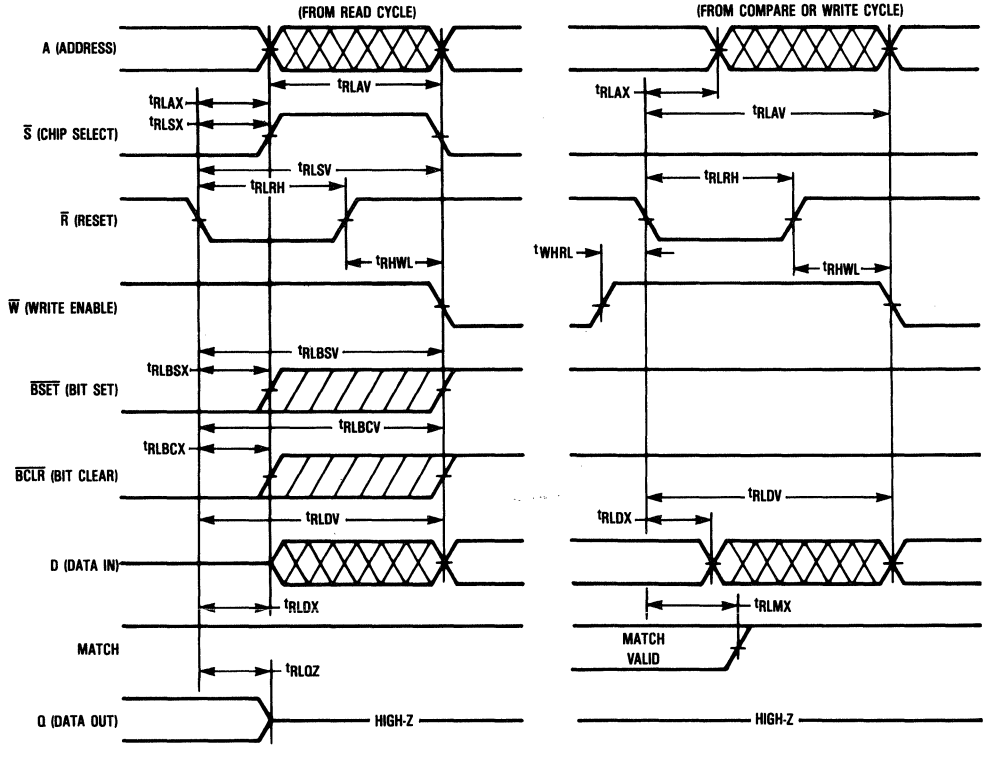
CLEAR CYCLE (See Note 1)

Characteristic	Symbol		MCM62351-20		MCM62351-22		MCM62351-25		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
$\overline{R}$ Low to Inputs Recognized (Clear Cycle Time) A	t_{RLAV}	t_{CR}	–	70	–	70	–	70	ns	
$\overline{S}$	t_{RLSV}	t_{CR}								
$\overline{BSET}$	t_{RLBSV}	t_{CR}								
$\overline{BCLR}$	t_{RLBCV}	t_{CR}								
D	t_{RLDV}	t_{CR}								
$\overline{R}$ Pulse Width	t_{RLRH}	t_{CLP}	22	–	25	–	30	–	ns	
Read Setup to $\overline{R}$ Low	t_{WHRL}	t_{RS}	5	–	5	–	5	–	ns	2
Write Hold from $\overline{R}$ High	t_{RHWL}	t_{WH}	0	–	0	–	0	–	ns	2
$\overline{R}$ Low to Inputs Don't Care A	t_{RLAX}	t_{CX}	0	–	0	–	0	–	ns	3
$\overline{S}$	t_{RLSX}	t_{CX}								
$\overline{BSET}$	t_{RLBSX}	t_{CX}								
$\overline{BCLR}$	t_{RLBCX}	t_{CX}								
D	t_{RLDX}	t_{CX}								
$\overline{R}$ Low to MATCH Assert	t_{RLMX}	t_{MH}	0	15	0	15	0	18	ns	
$\overline{R}$ Low to Output High-Z	t_{RLQZ}	t_{CZ}	–	15	–	15	–	18	ns	4

NOTES:
1. The address, $\overline{BSET}$, and $\overline{BCLR}$ inputs are don't cares during a clear cycle.
2. The clear cycle is initiated at the falling edge of $\overline{R}$. The t_{WHRL} and t_{RHWL} parameters must be satisfied to prevent an undesired configuration cycle.
3. "Inputs" for this parameter refers to all inputs except $\overline{W}$.
4. Transition is measured ±500 mV from steady state voltage with load of Figure 1b. This parameter is sampled and not 100% tested.

CLEAR CYCLE

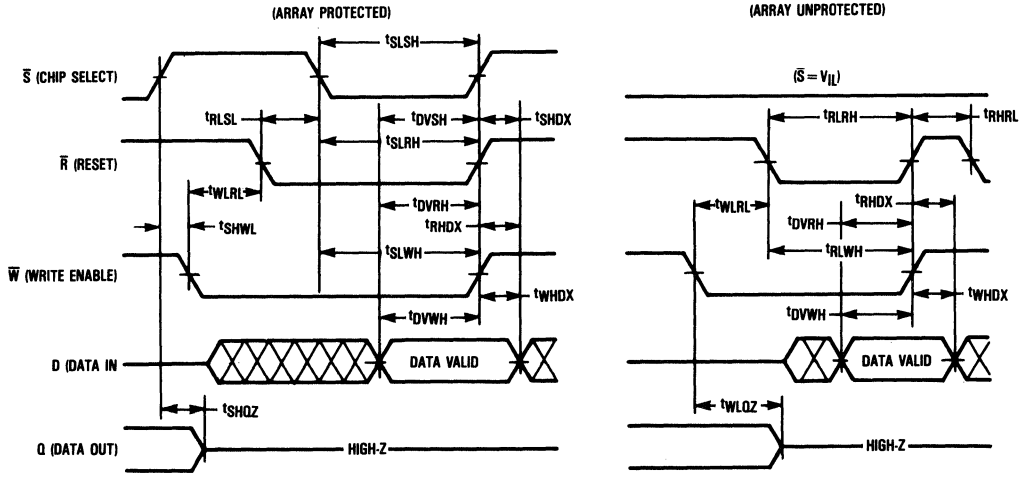


CONFIGURATION CYCLE (See Notes 1 and 2)

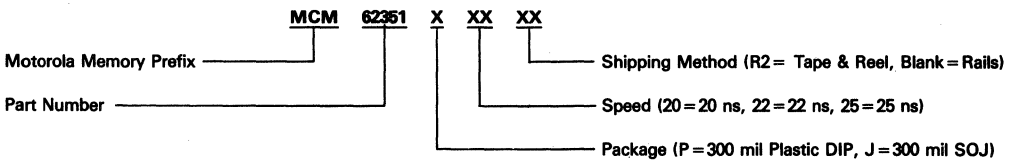
Characteristic	Symbol		MCM62351-20		MCM62351-22		MCM62351-25		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Configuration Control Pulse Width $\overline{S}$	t_{SLSH}	t_{SP}	20	–	20	–	25	–	ns	3
Configuration Control Pulse Width $\overline{R}$	t_{RLRH}	t_{SP}								
Data Setup to End of Configuration Cycle $\overline{S}$	t_{DVSH}	t_{DS}	10	–	10	–	12	–	ns	
Data Setup to End of Configuration Cycle $\overline{R}$	t_{DVRH}	t_{DS}								
Data Setup to End of Configuration Cycle $\overline{W}$	t_{DVWH}	t_{DS}								
Data Hold from End of Configuration Cycle $\overline{S}$	t_{SHDX}	t_{DH}	0	–	0	–	0	–	ns	
Data Hold from End of Configuration Cycle $\overline{R}$	t_{RHDX}	t_{DH}								
Data Hold from End of Configuration Cycle $\overline{W}$	t_{WHDX}	t_{DH}								
$\overline{R}$ High Pulse Width	t_{RHRL}	t_{CP}	5	–	5	–	5	–	ns	
Write Setup to $\overline{R}$ Low	t_{WLRL}	t_{WS}	5	–	5	–	5	–	ns	
$\overline{S}$ Setup to End of Configuration	t_{SLWH}	t_{SWS}	20	–	20	–	25	–	ns	4
$\overline{S}$ Setup to End of Configuration	t_{SLRH}	t_{SCS}								
$\overline{R}$ Setup to End of Configuration	t_{RLWH}	t_{SR}	20	–	20	–	25	–	ns	
$\overline{R}$ Setup to $\overline{S}$ Low	t_{RLSL}	t_{CSS}	5	–	5	–	5	–	ns	3
$\overline{S}$ Setup to Beginning of Write	t_{SHWL}	t_{WSS}	0	–	0	–	0	–	ns	
$\overline{S}$ High to Output High-Z	t_{SHQZ}	t_{HZ}	–	9	–	9	–	10	ns	5
$\overline{W}$ Low to Output High-Z	t_{WLQZ}	t_{HZ}	–	9	–	9	–	10	ns	5

NOTES:
1. A configuration cycle is performed during the overlap of $\overline{W}$ low, $\overline{R}$ low, and $\overline{S}$ low. Address, DQ1, DQ2, DQ3, $\overline{BSET}$, and $\overline{BCLR}$ inputs are don't cares during configuration cycles.
2. To ensure proper configuration of the device during power up, chip select must be equal to or greater than V_{IH}.
3. A valid configuration can be performed with $\overline{S}$ asserted prior to $\overline{R}$ and $\overline{W}$ low transitions. Be aware, however, that array data may be altered under this condition.
4. Note that terminating the cycle with $\overline{R}$ while leaving $\overline{W}$ and $\overline{S}$ asserted may cause array data to be altered.
5. Transition is measured ±500 mV from steady state voltage with load of Figure 1b. This parameter is sampled and not 100% tested.

CONFIGURATION CYCLE



ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers—	MCM62351P20	MCM62351P22	MCM62351P25
	MCM62351J20	MCM62351J22	MCM62351J25
	MCM62351J20R2	MCM62351J22R2	MCM62351J25R2

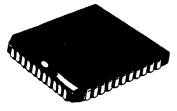
9

MCM62486

Product Preview

32K × 9 Bit BurstRAM™ Synchronous Static RAM

With Burst Counter and Self-Timed Write



FN PACKAGE
44–LEAD PLCC
CASE 777

The MCM62486 is a 294,912 bit synchronous static random access memory designed to provide a burstable, high performance, secondary cache for the i486 microprocessor. It is organized as 32,768 words of 9 bits, fabricated with Motorola's high-performance silicon-gate CMOS technology. The device integrates input registers, a 2-bit counter, high speed SRAM, and high drive capability outputs onto a single monolithic circuit for reduced parts count implementation of cache data RAM applications. Synchronous design allows precise cycle control with the use of an external clock (K). CMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

Addresses (A0–A14), data inputs (D0–D8), and all control signals except output enable ($\overline{G}$) are clock (K) controlled through positive-edge-triggered noninverting registers.

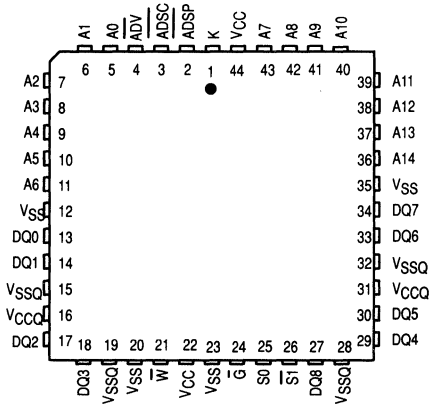
Bursts can be initiated with either address status processor ($\overline{ADSP}$) or address status cache controller ($\overline{ADSC}$) input pins. Subsequent burst addresses can be generated internally by the MCM62486 (burst sequence imitates that of the i486) and controlled by the burst address advance ($\overline{ADV}$) input pin. The following pages provide more detailed information on burst controls.

Write cycles are internally self-timed and are initiated by the rising edge of the clock (K) input. This feature eliminates complex off-chip write pulse generation and provides increased flexibility for incoming signals.

The MCM62486 will be available in a 44 pin plastic leaded chip carrier (PLCC). Multiple power and ground pins have been utilized to minimize effects induced by output noise. Separate power and ground pins have been employed for DQ0–DQ8 to allow user-controlled output levels of 5 volts or 3.3 volts.

- Single 5 V ± 10% Power Supply
- Choice of 5 V or 3.3 V ± 10% Power Supplies for Output Level Compatibility
- Fast Access Times: 14/19/24 ns Max and Cycle Times: 20/25/30 ns Min
- Internal Input Registers (Address, Data, Control)
- Internally Self–Timed Write Cycle
- $\overline{ADSP}$, $\overline{ADSC}$, and $\overline{ADV}$ Burst Control Pins
- Asynchronous Output Enable Controlled Three-State Outputs
- Common Data Inputs and Data Outputs
- High Output Drive Capability: 85 pF per I/O
- High Board Density PLCC Package
- Fully TTL Compatible
- Active High and Low Chip Select Inputs for Easy Depth Expansion

PIN ASSIGNMENT



PIN NAMES

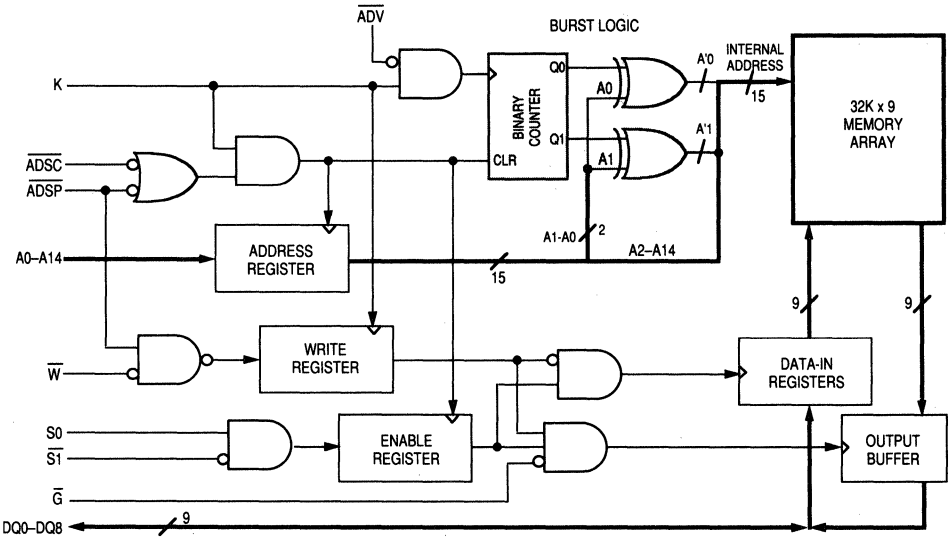
A0–A14	Address Inputs
K	Clock
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{S0}$,$\overline{S1}$	Chip Selects
$\overline{ADV}$	Burst Address Advance
$\overline{ADSP}$, $\overline{ADSC}$	Address Status
DQ0–DQ8	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{CCQ}	Output Buffer Power Supply
V_{SS}	Ground
V_{SSQ}	Output Buffer Ground

All power supply and ground pins must be connected for proper operation of the device. $V_{CC} \geq V_{CCQ}$ at all times including power up.

9

BurstRAM is a trademark of Motorola, Inc.
i486 is a trademark of Intel Corp.

BLOCK DIAGRAM (See Note)



NOTE: All registers are positive-edge triggered. The $\overline{ADSC}$ or $\overline{ADSP}$ signals control the duration of the burst and the start of the next burst. When $\overline{ADSP}$ is sampled low, any ongoing burst is interrupted and a read (independent of $\overline{W}$ and $\overline{ADSC}$) is performed using the new external address. When $\overline{ADSC}$ is sampled low (and $\overline{ADSP}$ is sampled high), any ongoing burst is interrupted and a read or write (dependent on $\overline{W}$) is performed using the new external address. Chip selects (S0, $\overline{S1}$) are sampled only when a new base address is loaded. After the first cycle of the burst, $\overline{ADV}$ controls subsequent burst cycles. When $\overline{ADV}$ is sampled low, the internal address is advanced prior to the operation. When $\overline{ADV}$ is sampled high, the internal address is not advanced, thus inserting a wait state into the burst sequence accesses. Upon completion of a burst, the address will wrap around to its initial state. See **BURST SEQUENCE TABLE**.

BURST SEQUENCE TABLE (See Note)

External Address	A14–A2	A1	A0
1st Burst Address	A14–A2	A1	$\overline{A0}$
2nd Burst Address	A14–A2	$\overline{A1}$	A0
3rd Burst Address	A14–A2	$\overline{A1}$	$\overline{A0}$

NOTE: The burst wraps around to its initial state upon completion.

SYNCHRONOUS TRUTH TABLE (See Notes 1, 2, 3, and 4)

S	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{W}$	K	Address Used	Operation
F	L	X	X	X	L-H	N/A	Deselected
F	X	L	X	X	L-H	N/A	Deselected
T	L	X	X	X	L-H	External Address	Read Cycle, Begin Burst
T	H	L	X	L	L-H	External Address	Write Cycle, Begin Burst
T	H	L	X	H	L-H	External Address	Read Cycle, Begin Burst
X	H	H	L	L	L-H	Next Address	Write Cycle, Continue Burst
X	H	H	L	H	L-H	Next Address	Read Cycle, Continue Burst
X	H	H	H	L	L-H	Current Address	Write Cycle, Suspend Burst
X	H	H	H	H	L-H	Current Address	Read Cycle, Suspend Burst

NOTES:
1. X means Don't Care
2. All inputs except $\overline{G}$ must meet setup and hold times for the low-to-high transition of clock (K).
3. S represents S0 and $\overline{S1}$. T implies $\overline{S1}$ = L and S0 = H; F implies $\overline{S1}$ = H or S0 = L.
4. Wait states are inserted by suspending burst.

ASYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

Operation	$\overline{G}$	I/O Status
Read	L	Data Out (DQ0–DQ8)
Read	H	High-Z
Write	X	High-Z — Data In (DQ0–DQ8)
Deselected	X	High-Z

NOTES:
1. X means Don't Care
2. For a write operation following a read operation, $\overline{G}$ must be high before the input data required setup time and held high through the input data hold time.

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to 7.0	V
Output Power Supply Voltage	V_{CCQ}	– 0.5 to V_{CC}	V
Voltage Relative to V_{SS}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation (T_A = 70°C, V_{CC} = 5 V, t_{KHKH} = 20 ns)	P_D	1.2	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions to taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

9

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, V_{CCQ} = 5.0 V or 3.3 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range	V_{CC}	4.5	5.0	5.5	V
Output Buffer Supply Voltage (5.0 V TTL Compatible) (3.3 V 50 Ω Compatible)	V_{CCQ}	 4.5 3.0	 5.0 3.3	 5.5 3.6	V
Input High Voltage	V_{IH}	2.2	3.0	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	– 0.5 *	0.0	0.8	V

* V_{IL} (min) = – 3.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{G}$, $\overline{S1}$ = V_{IH}, S0 = V_{IL}, V_{out} = 0 to V_{CCQ})	$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current ($\overline{G}$, $\overline{S1}$, = V_{IH}, S0 = V_{IL}, All Inputs = V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, I_{out} = 0 mA, Cycle Time ≥ t_{KHKH} min)	I_{CCA}	—	185	mA
Standby Current ($\overline{S1}$ = V_{IH}, S0 = V_{IL}, All Inputs = V_{IL} and V_{IH}, Cycle Time ≥ t_{KHKH} min)	I_{SB1}	—	40	mA
CMOS Standby Current ($\overline{S1}$ ≥ V_{CC} – 0.2 V, S0 ≤ 0.2 V, All Inputs ≥ V_{CC} – 0.2 V or ≤ 0.2 V, Cycle Time ≥ t_{KHKH} min)	I_{SB2}	—	30	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

NOTE: Good decoupling of the local power supply should always be used. DC characteristics are guaranteed for all possible i486 bus cycles.

9

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance (All Pins Except DQ0–DQ8)	C_{in}	4	5	pF
Input/Output Capacitance (DQ0–DQ8)	$C_{I/O}$	8	10	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, V_{CCQ} = 5.0 V or 3.3 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol		MCM62486-14		MCM62486-19		MCM62486-24		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	t_{CYC}	20	—	25	—	30	—	ns	
Clock Access Time	t_{KHQV}	t_{CD}	—	14	—	19	—	24	ns	4
Output Enable to Output Valid	t_{GLQV}	t_{OE}	—	7	—	8	—	9	ns	
Clock High to Output Active	t_{KHQX1}	t_{DC1}	3	—	3	—	3	—	ns	
Clock High to Output Change	t_{KHQX2}	t_{DC2}	3	—	3	—	3	—	ns	
Output Enable to Output Active	t_{GLQX}	t_{OLZ}	0	—	0	—	0	—	ns	
Output Disable to Q High-Z	t_{GHQZ}	t_{OHZ}	—	7	—	8	—	9	ns	5
Clock High to Q High-Z	t_{KHQZ}	t_{CZ}	—	10	—	12	—	15	ns	
Clock High Pulse Width	t_{KHKL}	t_{CH}	8	—	9.5	—	11	—	ns	
Clock Low Pulse Width	t_{KLKH}	t_{CL}	8	—	9.5	—	11	—	ns	
Setup Times: Address Address Status Data In Write Address Advance Chip Select	t_{AVKH} t_{ADSVKH} t_{DVKH} t_{WVKH} t_{ADVVKH} t_{S0VKH} t_{S1VKH}	t_{AS} t_{SS} t_{DS} t_{WS}	3	—	3	—	3	—	ns	6
Hold Times: Address Address Status Data In Write Address Advance Chip Select	t_{KHAX} t_{KHADSX} t_{KHDX} t_{KHWX} t_{KHADVX} t_{KHS0X} t_{KHS1X}	t_{AH} t_{SH} t_{DH} t_{WH}	2	—	2	—	2	—	ns	6

NOTES:
1. A read cycle is defined by $\overline{W}$ high or $\overline{ADSP}$ low for the setup and hold times. A write cycle is defined by $\overline{W}$ low and $\overline{ADSP}$ high for the setup and hold times.
2. All read and write cycle timings are referenced from K or $\overline{G}$.
3. $\overline{G}$ is a don't care when $\overline{W}$ is sampled low.
4. Maximum access times are guaranteed for all possible i486 external bys cycles.
5. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{GHQZ} max is less than t_{GLQX} min for a given device and from device to device.
6. This is a synchronous device. All addresses must meet the specified setup and hold times for ***ALL*** rising edges of clock (K) whenever $\overline{ADSP}$ and $\overline{ADSC}$ is low and the chip is selected. All other synchronous inputs must meet the specified setup and hold times for ***ALL*** rising edges of K when the chip is selected. Chip select must be true ($\overline{S1}$ low and S0 high) at each rising edge of clock for the device (when $\overline{ADSP}$ or $\overline{ADSC}$ is low) to remain enabled. Timings for $\overline{S1}$ and S0 are similar.

AC TEST LOADS

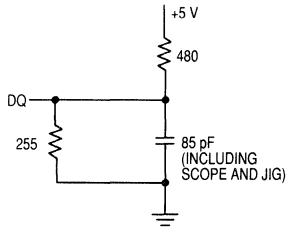


Figure 1A

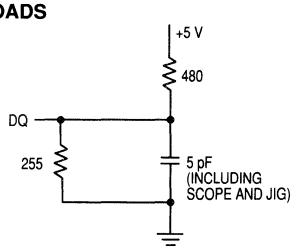
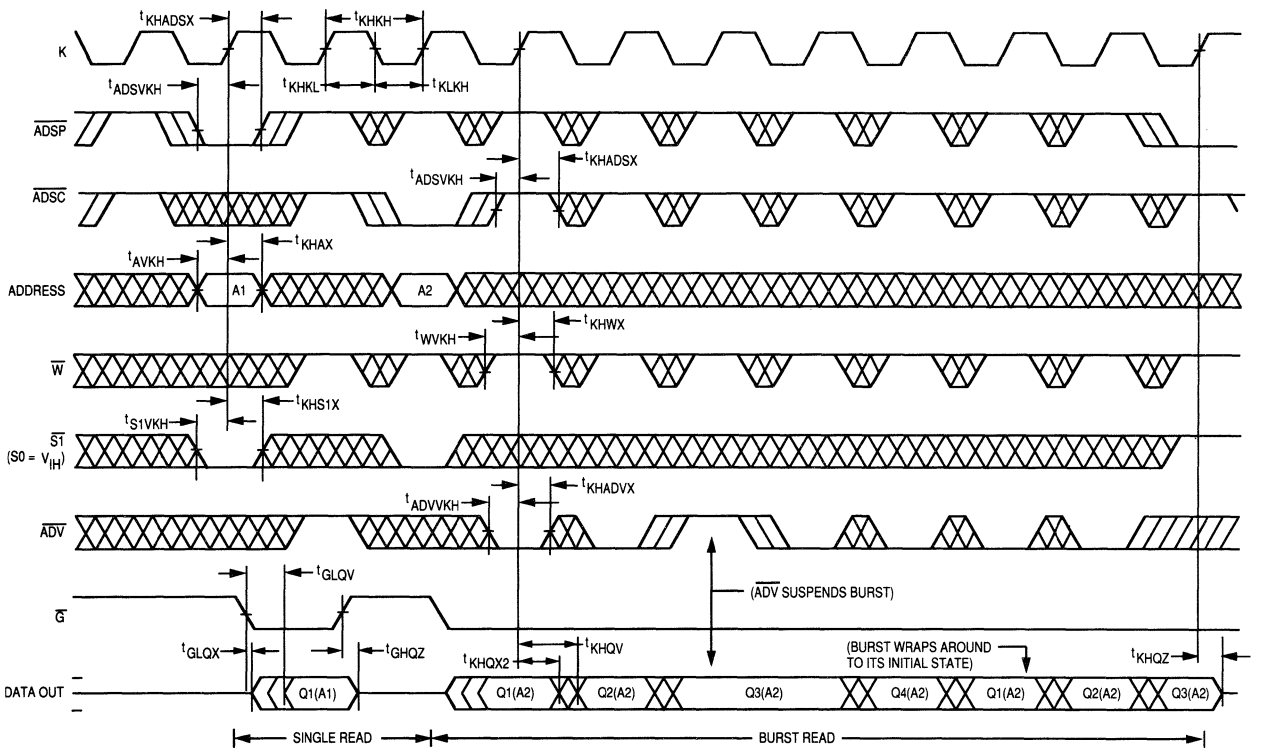


Figure 1B

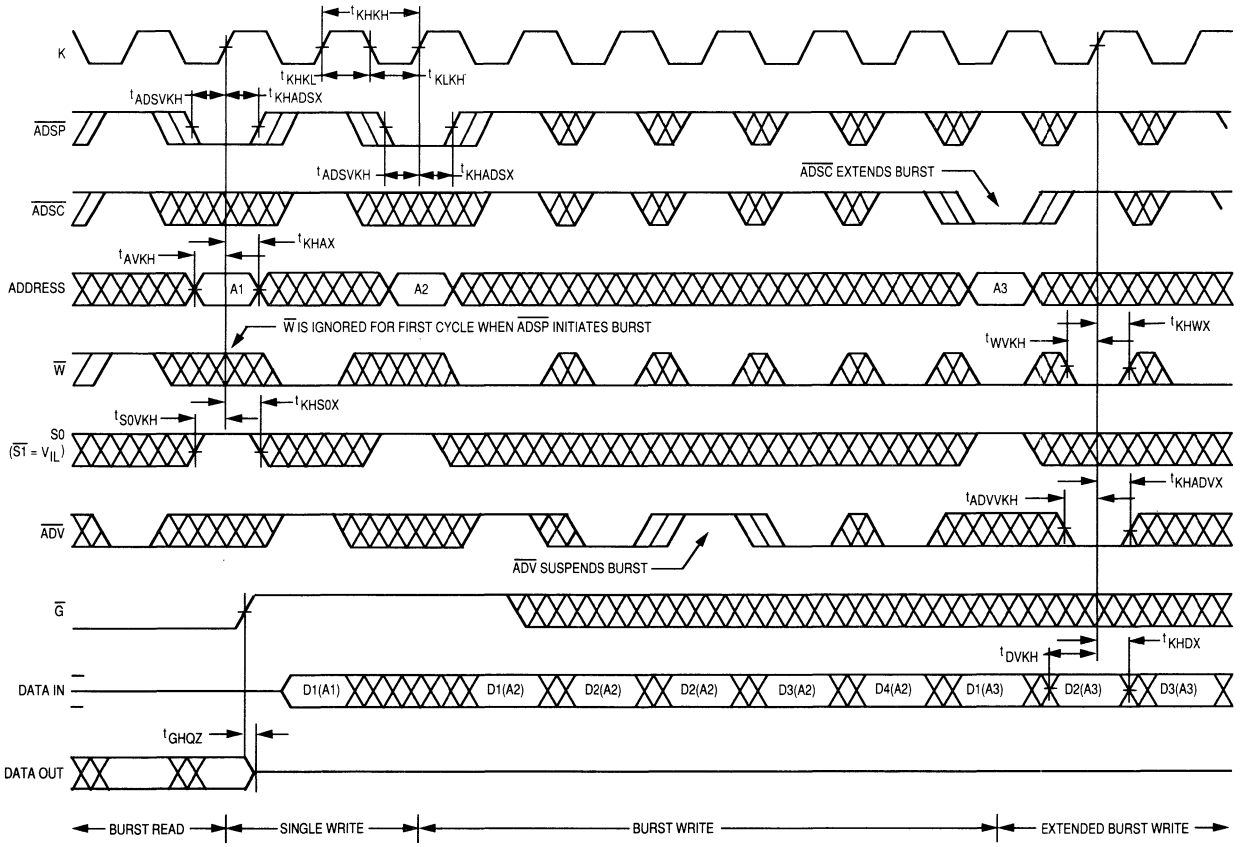
9

READ CYCLES

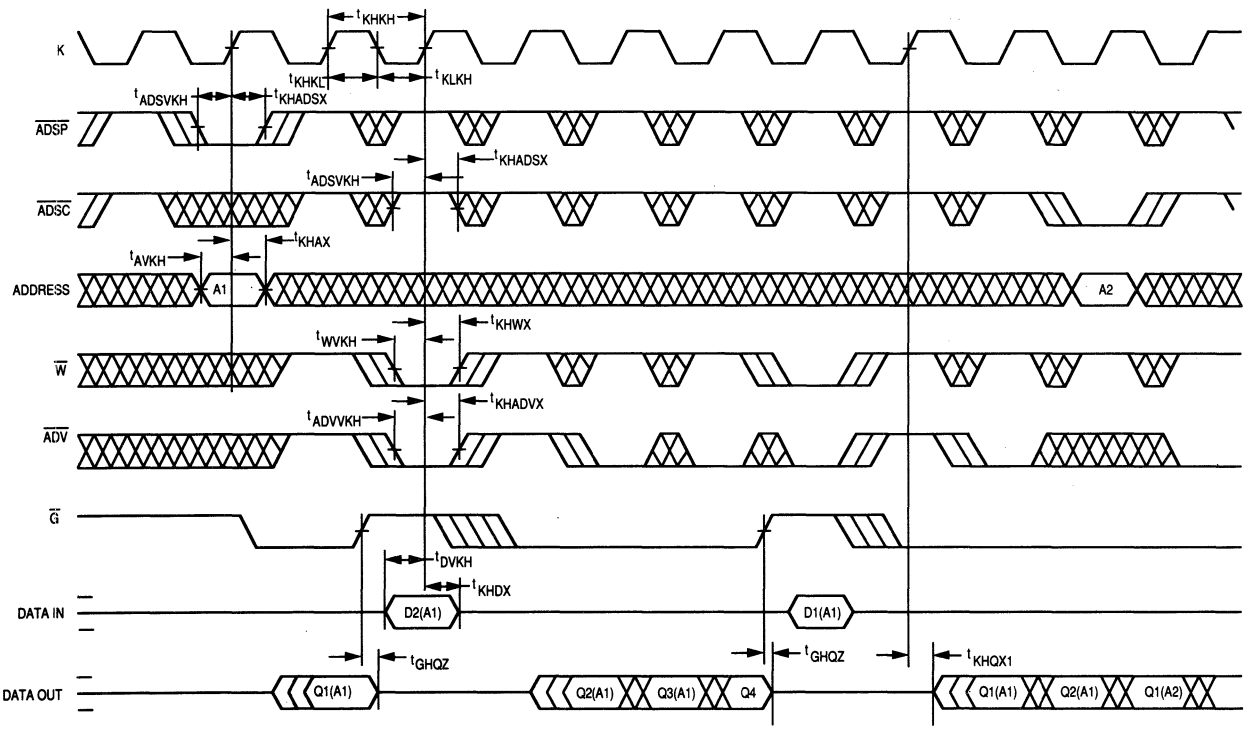


NOTE: Q1(A2) represents the first output data from the base address A2; Q2(A2) represents the next output data in the burst sequence with A2 as the base address.

WRITE CYCLES



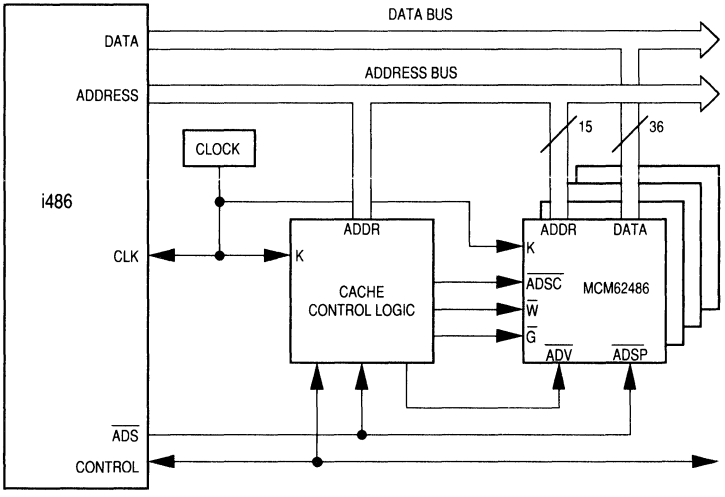
COMBINATION READ/WRITE CYCLES



($\overline{S1}$ = V_{IL}; S0 = V_{IH})

NOTE: This diagram does not show typical processor cycles, but is intended to show the functionality of the SRAM.

APPLICATION EXAMPLE



128K BYTE BURSTABLE, SECONDARY CACHE USING
4 MCM62486FN24s WITH A 33 MHz i486

9

ORDERING INFORMATION
(Order by Full Part Number)

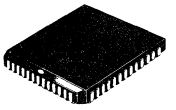
MCM	62486	x	xx
Motorola Memory Prefix			Speed (14 = 14 ns, 19 = 19 ns, 24 = 24 ns)
Part Number			Package (FN = PLCC)

Full Part Number – MCM62486FN14 MCM62486FN19 MCM62486FN24

Product Preview

8K × 20 Bit Fast Static RAM

MCM62820



FN PACKAGE
PLASTIC
CASE 778

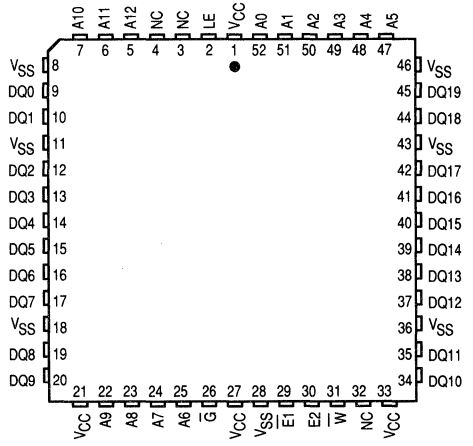
The MCM62820 is a 163,840 bit static random access memory organized as 8,192 words of 20 bits, fabricated using Motorola's high-performance silicon-gate CMOS technology. The device integrates an 8Kx20 SRAM core with address and chip enable input latches, multiple chip enable inputs, and an output enable input.

The availability of output enable ($\overline{G}$) and multiple chip enable ($\overline{E1}$ and E2) inputs provide for greater system flexibility when multiple devices are used. With either chip enable input negated, the device will enter standby mode, useful in low power applications. All address (A0–A12) and chip enable ($\overline{E1}$, E2) inputs propagate through level-sensitive on-chip latching controlled by LE. This feature alleviates the need for external address and chip enable latching. This device was designed specifically to operate as cache memory with the R3000 RISC Microprocessor (see Figure 2), but it will also be very adaptable wherever wide and fass SRAMs are needed.

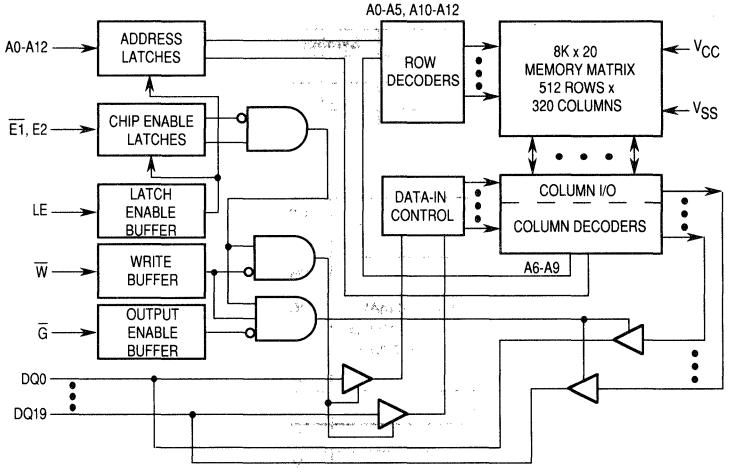
The MCM62820 will be available in a 52 pin plastic leaded chip-carrier. Multiple power and ground pins have been utilized to minimize effects induced by output noise.

- Single 5 V ±10% Power
- Fast Access and Cycle Times: 23/30 ns Max
- Fully Static Read and Write Operations
- Equal Address and Chip Enable Access Times
- On Chip Address and Chip Enable Latches
- Active High and Active Low Chip Enable Inputs
- Output Enable Controlled Three State Outputs
- High Board Density PLCC Package
- Low Power Standby Mode
- Fully TTL Compatible

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES	
A0–A12	Address Inputs
LE	Latch Enable
$\overline{W}$	Write Enable
$\overline{E1}$, E2	Chip Enable
$\overline{G}$	Output Enable
DQ0–DQ19	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground
NC	No Connection

For proper operation of the device, all V_{SS} pins must be connected to ground.

TRUTH TABLE

$\overline{E1}$	E2	$\overline{G}$	$\overline{W}$	LE	Mode	Supply Current	I/O Status
H	X	X	X	X	Not Selected	I_{SB}	High-Z
X	L	X	X	X	Not Selected	I_{SB}	High-Z
L	H	H	H	X	Output Disabled	I_{CC}	High-Z
L	H	L	H	H	Read with Transparent Inputs	I_{CC}	Data Out
L	H	L	H	L	Read with Latched Inputs	I_{CC}	Data Out
L	H	X	L	H	Write with Transparent Inputs	I_{CC}	Data In
L	H	X	L	L	Write with Latched Inputs	I_{CC}	Data In

NOTE: X means don't care. Inputs A0–A12, $\overline{E1}$, E2 are latched or transparent depending upon the state of latch enable (LE).

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is assumed to be in a test socket or mounted on a printed circuit board with at least 300 LFPM of transverse air flow being maintained.

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to V_{SS}=0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	–0.5 to +7.0	V
Voltage Relative to V_{SS}	V_{in}, V_{out}	–0.5 to V_{CC} +0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation (T_A=70°C, V_{CC}=5 V, t_{AVAV}=23 ns)	P_D	2.5	W
Temperature Under Bias	T_{bias}	–10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	–55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC}= 5.0 V ±10%, T_A=0 to +70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}=0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	3.0	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	–0.5*	0.0	0.8	V

*V_{IL} (min)=–3.0 V ac (pulse width ≤20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in}=0 to V_{CC})	$I_{lkg(I)}$	—	±1.0	µA
Output Leakage Current ($\overline{G}$=V_{IH}, $\overline{E1}$=V_{IH}, E2=V_{IL}, V_{out}=0 to V_{CC})	$I_{lkg(O)}$	—	±1.0	µA
AC Supply Current ($\overline{G}$=V_{IH}, $\overline{E1}$=V_{IL}, E2=V_{IH}, All Inputs=V_{IL}=0.0 V and V_{IH}≥3.0, I_{out}=0 mA) Cycle Time≥23 ns Cycle Time≥30 ns	I_{CCA}	 — —	 240 185	mA
Standby Current ($\overline{E1}$=V_{IH}, E2=V_{IL}, All Inputs=V_{IL} or V_{IH})	I_{SB1}	—	15.0	mA
CMOS Standby Current ($\overline{E1}$≥V_{CC}–0.2 V, E2≤0.2 V, All Inputs ≥V_{CC}–0.2 V or ≤0.2 V)	I_{SB2}	—	10.0	mA
Output Low Voltage (I_{OL}=+8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH}=–4.0 mA)	V_{OH}	2.4	—	V

CAPACITANCE (f=1.0 MHz, dV=3.0 V, T_A=25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Typ	Max	Unit
Input Capacitance	All Pins Except DQ0–DQ19	C_{in}	4	6	pF
Input/Output Capacitance	DQ0–DQ19	$C_{I/O}$	6	8	pF

9

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC}=5.0 V ±10%, T_A=0 to 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 3 ns

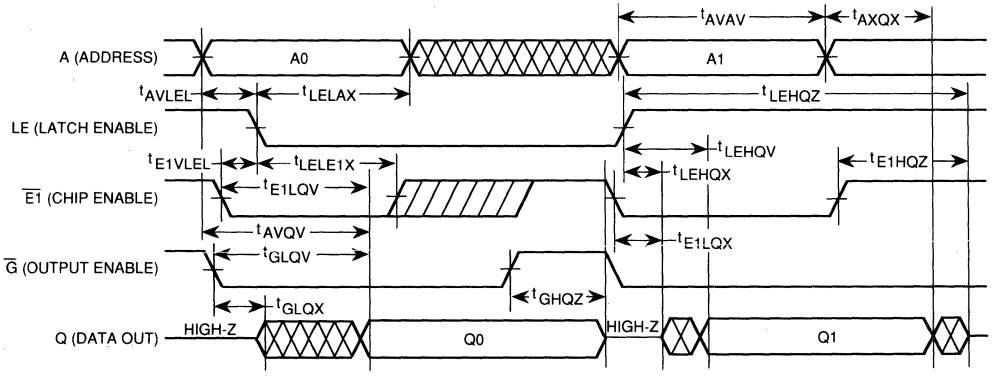
Output Measurement Reference Level . . . . . 1.5 V
Output Load . . . . . See Figure 1A Unless Otherwise Noted

READ CYCLE TIMING (See Notes 1, 2, 3)

Parameter	Symbol		MCM62820–23		MCM62820–30		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	23	—	30	—	ns	
Address Access Time	t_{AVQV}	t_{AA}	—	23	—	30	ns	
Chip Enable to Output Valid	t_{E1LQV} t_{E2HQV}	t_{AC1}	—	23	—	30	ns	4
Latch Enable High to Output Valid	t_{LEHQV}		25	—	30	—	ns	
Output Enable to Output Valid	t_{GLQV}	t_{OE}	—	10	—	12	ns	
Output Active from Chip Enable	t_{E1LQX} t_{E2HQX}	t_{CLZ}	2	—	2	—	ns	4, 5
Output Active from Output Enable	t_{GLQX}	t_{OLZ}	2	—	2	—	ns	5
Output Active from Latch Enable High	t_{LEHQX}		2	—	2	—	ns	5
Output Hold from Address Change	t_{AXQX}	t_{OH}	3	—	3	—	ns	
Setup Times For: A	t_{AVLEL}	t_{AS}	4	—	4	—	ns	4, 6
$\overline{E1}$	t_{E1VLEL}	t_{CS}						
E2	t_{E2VLEL}	t_{CS}						
Hold Times for: A	t_{LELAX}	t_{AH}	3	—	3	—	ns	4, 6
$\overline{E1}$	t_{LELE1X}	t_{CH}						
E2	t_{LELE2X}	t_{CH}						
Chip Enable High to Output High Z	t_{E1HQZ} t_{E2LQZ}	t_{CHZ}	0	9	0	10	ns	4, 5
Latch Enable High to Output High Z	t_{LEHQZ}	t_{CHZ}	0	9	0	10	ns	5
Output Enable to Output High Z	t_{GHQZ}	t_{OHZ}	0	8	0	10	ns	5

NOTES:
1. A read cycle is defined by $\overline{W}$ high.
2. All read cycle timings are referenced from the last valid address to the first transitioning address.
3. Addresses must be valid prior to or coincident with $\overline{E1}$ going low or E2 going high.
4. $\overline{E1}$ in the timing diagrams represents both $\overline{E1}$ and E2 with $\overline{E1}$ asserted low and E2 asserted high.
5. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{E1HQZ} max is less than t_{E1LQX} min, t_{E2LQZ} max is less than t_{E2HQX} min and t_{GHQZ} max is less than t_{GLQX} min for a given device and from device to device.
6. These inputs are latched and must meet the required setup and hold times for ***ALL*** latch enable (LE) low transitions.

READ CYCLE



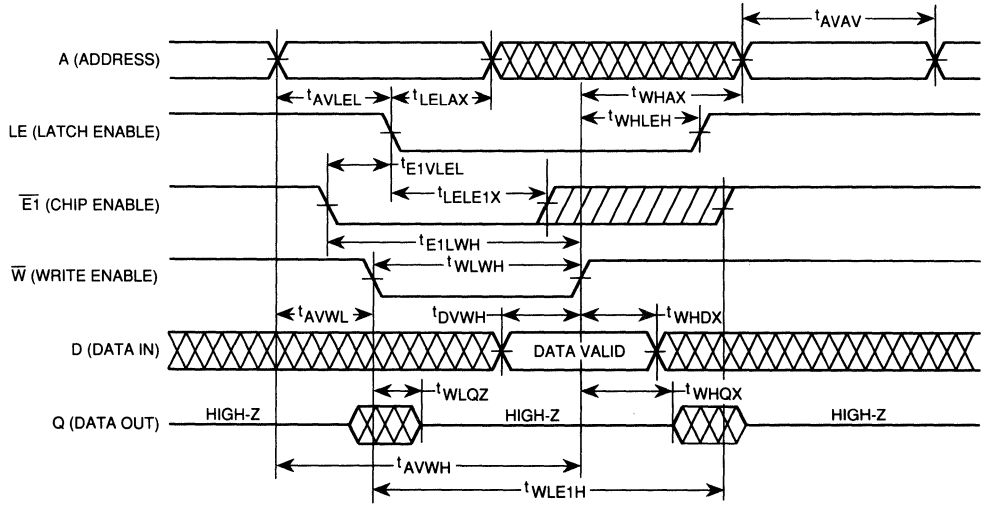
WRITE CYCLE TIMING, Write Enable Initiated (See Note 1)

Parameter	Symbol		MCM62820–23		MCM62820–30		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	23	—	30	—	ns	
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	ns	2
Address Valid to End of Write	t_{AVWH}	t_{AW}	20	—	25	—	ns	
Write Pulse Width	t_{WLWH}	t_{WP}	15	—	18	—	ns	3
Write Enable to Chip Enable Disable	t_{WLE1H} t_{WLE2L}	t_{CW}	15	—	18	—	ns	4
Chip Enable to End of Write	t_{E1LWH} t_{E2HWH}	t_{CW}	15	—	18	—	ns	3, 4, 5
Data Valid to End of Write	t_{DVWH}	t_{DW}	7	—	10	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	—	0	—	ns	6
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	ns	2
Setup Times for: A $\overline{E1}$ E2	t_{AVLEL} t_{E1VLEL} t_{E2VLEL}	t_{AS} t_{CS} t_{CS}	4	—	4	—	ns	4, 5
LE Hold to End of Write	t_{WHLEH}	t_{LEH}	–2	—	–2	—	ns	
Hold Times for: A $\overline{E1}$ E2	t_{LELAX} t_{LELE1X} t_{LELE2X}	t_{AH} t_{CH} t_{CH}	3	—	3	—	ns	4, 5
Write Low to Output High Z	t_{WLQZ}	t_{WHZ}	0	9	0	10	ns	7
Write High to Output Low Z	t_{WHQX}	t_{WLZ}	2	—	2	—	ns	7

NOTES:
1. A write cycle starts at the latest transition of $\overline{E1}$ low, $\overline{W}$ low, or E2 high. A write cycle ends at the earliest transition of a $\overline{E1}$ high $\overline{W}$ high, or E2 low.
2. Write must be high for all address transitions.
3. If $\overline{W}$ goes low coincident with or prior to $\overline{E1}$ low or E2 high the outputs will remain in a high impedance state.
4. $\overline{E1}$ in the timing diagrams represents both $\overline{E1}$ and E2 with $\overline{E1}$ asserted low and E2 asserted high.
5. These inputs are latched and must meet the required setup and hold times for ***ALL*** latch enable (LE) low transitions.
6. During this time the output pins may be in the output state. Signals of opposite phase must not be applied to the outputs at this time.
7. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{E1HQZ} max is less than t_{E1LQX} min, t_{E2LQZ} max is less than t_{E2HQX} min and t_{GHQX} max is less than t_{GLQX} min for a given device and from device to device.

9

WRITE ENABLE INITIATED WRITE CYCLE

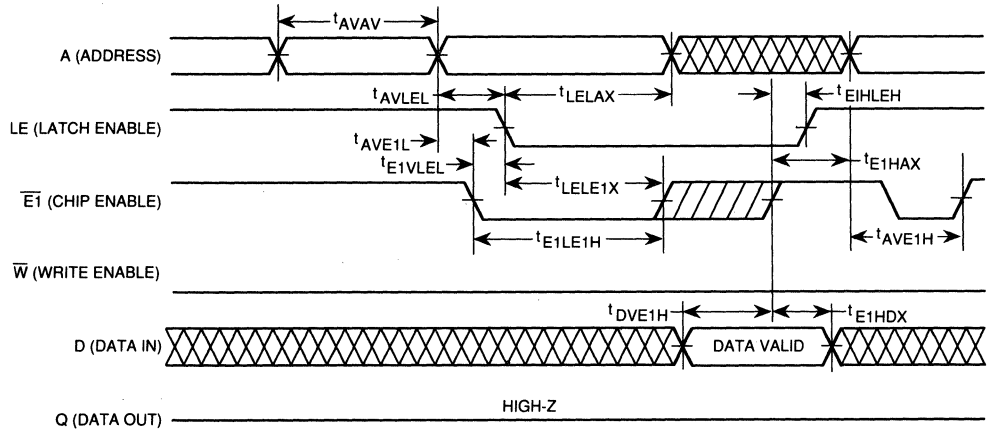


WRITE CYCLE TIMING, Chip Enable Initiated (See Notes 1 and 2)

Parameter	Symbol		MCM62820–23		MCM62820–30		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	23	—	30	—	ns	
Address Setup TIme	t_{AVE1L} t_{AVE2H}	t_{AS}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVE1H} t_{AVE2L}	t_{AW}	20	—	25	—	ns	
Data Valid to End of Write	t_{DVE1H} t_{DVE2L}	t_{DW}	7	—	10	—	ns	
Chip Enable to End of Write	t_{E1LE1H} t_{E2HE2L}	t_{CW}	15	—	18	—	ns	3
Data Hold Time	t_{E1HDX} t_{E2LDX}	t_{DH}	0	—	0	—	ns	4
Write Recovery Time	t_{E1HAX} t_{E2LAX}	t_{WR}	0	—	0	—	ns	
LE Hold to End of Write	t_{E1HLEH} t_{E2LLEH}	t_{E1HLEH} t_{E2LLEH}	−2	—	−2	—	ns	
Setup TImes for: A $\overline{E1}$ E2	t_{AVLEL} t_{E1VLEL} t_{E2VLEL}	t_{AS} t_{CS} t_{CS}	4	—	4	—	ns	5
Hold TImes for: A $\overline{E1}$ E2	t_{LELAX} t_{LELE1X} t_{LELE2X}	t_{AH} t_{CH} t_{CH}	3	—	3	—	ns	5

NOTES:
1. A write cycle starts at the latest transition of $\overline{E1}$ low, $\overline{W}$ low, or E2 high. A write cycle ends at the earliest transition of a $\overline{E1}$ high, $\overline{W}$ high, or E2 low.
2. $\overline{E1}$ in the timing diagrams represents both $\overline{E1}$ and E2 with $\overline{E1}$ asserted low and E2 asserted high.
3. If $\overline{W}$ goes low coincident with or prior to $\overline{E1}$ low or E2 high the outputs will remain in a high impedance state.
4. During this time the output pins may be in the output state. Signals of opposite phase must not be applied to the outputs at this time.
5. These inputs are latched and must meet the required setup and hold times for ***ALL*** latch enable (LE) low transitions.

CHIP ENABLE INITIATED WRITE CYCLE



AC TEST LOADS

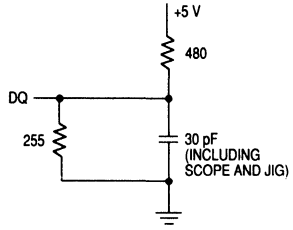


Figure 1A

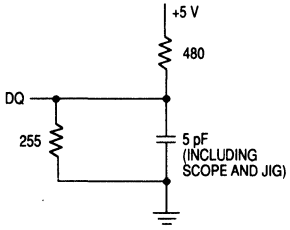


Figure 1B

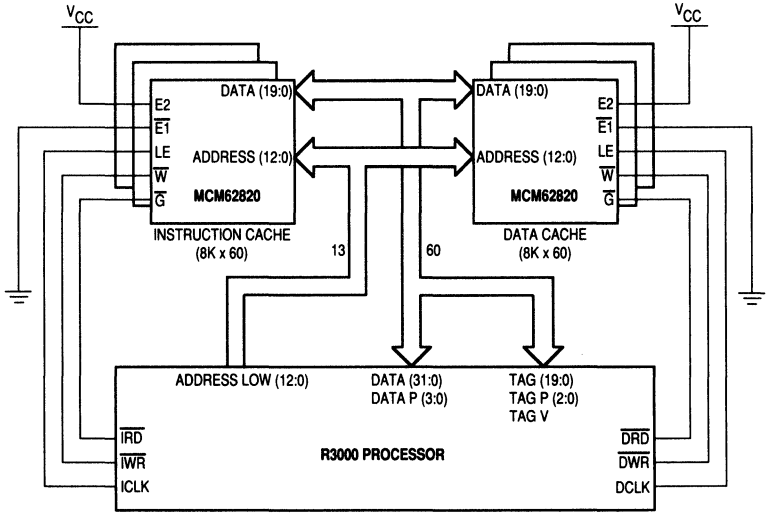
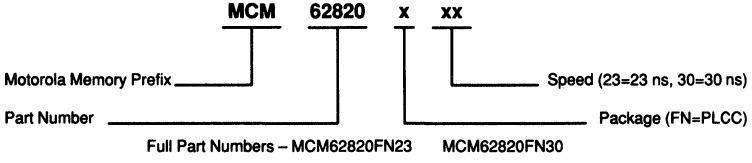


Figure 2. R3000 Application Example with 64K Byte Segregated Instruction/Data Cache Using Six Motorola MCM62820 Latched SRAMs

ORDERING INFORMATION
(Order by Full Part Number)

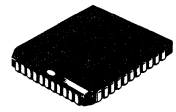


MCM62940

Product Preview

32K × 9 Bit BurstRAM™ Synchronous Static RAM

With Burst Counter and Self-Timed Write



FN PACKAGE
44-LEAD PLCC
CASE 777

The MCM62940 is a 294,912 bit synchronous static random access memory designed to provide a burstable, high performance, secondary cache for the MC68040 microprocessor. It is organized as 32,768 words of 9 bits, fabricated using Motorola's high-performance silicon-gate CMOS technology. The device integrates input registers, a 2-bit counter, high speed SRAM, and high drive capability outputs onto a single monolithic circuit for reduced parts count implementation of cache data RAM applications. Synchronous design allows precise cycle control with the use of an external clock (K). CMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

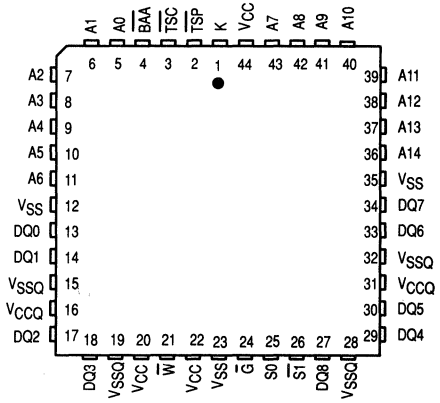
Addresses (A0–A14), data inputs (D0–D8), and all control signals, except output enable ($\overline{G}$), are clock (K) controlled through positive-edge-triggered noninverting registers.

Bursts can be initiated with either transfer start processor ($\overline{TSP}$) or transfer start cache controller ($\overline{TSC}$) input pins. Subsequent burst addresses are generated internally by the MCM62940 (burst sequence imitates that of the MC68040) and controlled by the burst address advance ($\overline{BAA}$) input pin. The following pages provide more detailed information on burst controls.

Write cycles are internally self-timed and are initiated by the rising edge of the clock (K) input. This feature eliminates complex off-chip write pulse generation and provides increased flexibility for incoming signals.

The MCM62940 is packaged in a 44 pin plastic leaded chip carrier (PLCC). Multiple power and ground pins have been utilized to minimize effects induced by output noise. Separate power and ground pins have been employed for DQ0–DQ8 to allow user-controlled output levels of 5 volts or 3.3 volts.

PIN ASSIGNMENT



- Single 5 V ± 10% Power Supply
- Choice of 5 V or 3.3 V ± 10% Power Supplies for Output Level Compatibility
- Fast Access Times: 14/19/24 ns Max and Cycle Times: 20/25/30 ns Min
- Internal Input Registers (Address, Data, Control)
- Internally Self-Timed Write Cycle
- $\overline{TSP}$, $\overline{TSC}$, and $\overline{BAA}$ Burst Control Pins
- Asynchronous Output Enable Controlled Three-State Outputs
- Common Data Inputs and Data Outputs
- High Output Drive Capability: 85 pF per I/O
- High Board Density PLCC Package
- Fully TTL Compatible
- Active High and Low Chip Select Inputs for Easy Depth Expansion

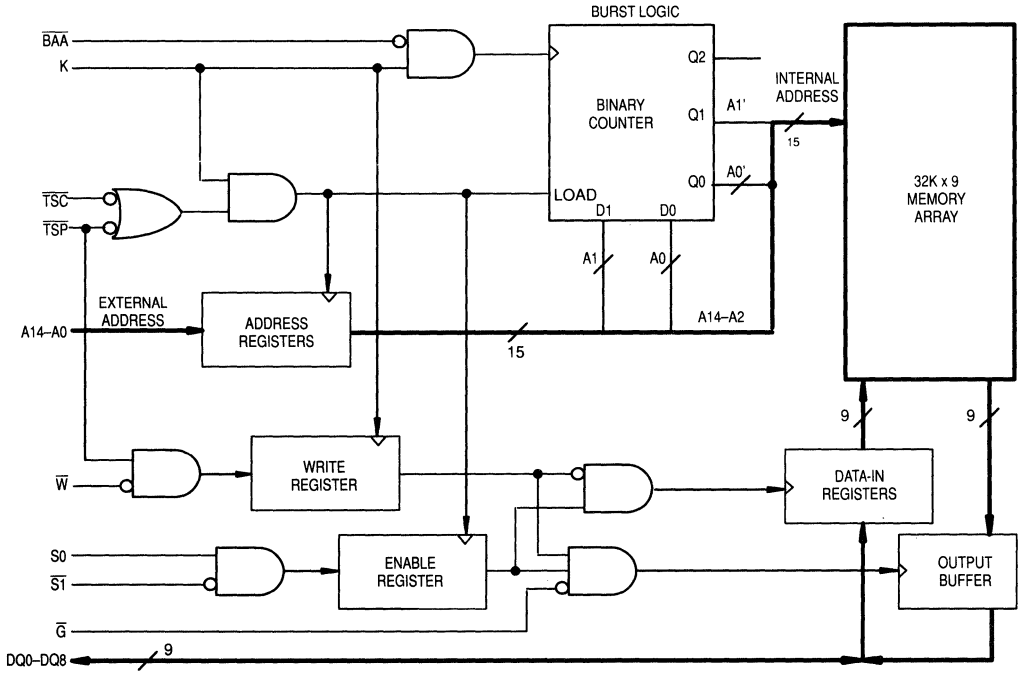
PIN NAMES	
A0–A14	Address Inputs
K	Clock
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
S0, $\overline{S1}$	Chip Selects
$\overline{BAA}$	Burst Address Advance
$\overline{TSP}$, $\overline{TSC}$	Transfer Start
DQ0–DQ8	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{CCQ}	Output Buffer Power Supply
V_{SS}	Ground
V_{SSQ}	Output Buffer Ground

All power supply and ground pins must be connected for proper operation of the device. $V_{CC} \geq V_{CCQ}$ at all times including power up.

BurstRAM is a trademark of Motorola, Inc.

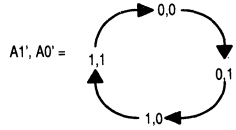
This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

BLOCK DIAGRAM (See Note)



NOTE: All registers are positive-edge triggered. The $\overline{TSC}$ or $\overline{TSP}$ signals control the duration of the burst and the start of the next burst. When $\overline{TSP}$ is sampled low, any ongoing burst is interrupted and a read (independent of $\overline{W}$ and $\overline{TSC}$) is performed using the new external address. When $\overline{TSC}$ is sampled low (and $\overline{TSP}$ is sampled high), any ongoing burst is interrupted and a read or write (dependent on $\overline{W}$) is performed using the next external address. Chip selects (S0, $\overline{S1}$) are sampled only when a new base address is loaded. After the first cycle of the burst, $\overline{BAA}$ controls subsequent burst cycles. When $\overline{BAA}$ is sampled low, the internal address is advanced prior to the operation. When $\overline{BAA}$ is sampled high, the internal address is not advanced, thus inserting a wait state into the burst sequence accesses. Upon completion of a burst, the address will wrap around to its initial state. See **BURST SEQUENCE GRAPH**.

BURST SEQUENCE GRAPH (See Note)



NOTE: The external two values for A1 and A0 provide the starting point for the burst sequence graph. The burst logic advances A1 and A0 as shown above.

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SYNCHRONOUS TRUTH TABLE (See Notes 1, 2, 3, and 4)

S	$\overline{TSP}$	$\overline{TSC}$	$\overline{BAA}$	$\overline{W}$	K	Address	Operation
F	L	X	X	X	L-H	N/A	Deselected
F	X	L	X	X	L-H	N/A	Deselected
T	L	X	X	X	L–H	External Address	Read Cycle, Begin Burst
T	H	L	X	L	L-H	External Address	Write Cycle, Begin Burst
T	H	L	X	H	L-H	External Address	Read Cycle, Begin Burst
X	H	H	L	L	L-H	Next Address	Write Cycle, Continue Burst
X	H	H	L	H	L-H	Next Address	Read Cycle, Continue Burst
X	H	H	H	L	L-H	Current Address	Write Cycle, Suspend Burst
X	H	H	H	H	L-H	Current Address	Read Cycle, Suspend Burst

NOTES:
1. X means Don't Care
2. All inputs except $\overline{G}$ must meet setup and hold times for the low-to-high transition of clock (K).
3. S represents S0 and $\overline{S1}$. T implies S0 = H and $\overline{S1}$ = L; F implies S0 = L or $\overline{S1}$ = H.
4. Wait states are inserted by suspending burst.

ASYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

Operation	$\overline{G}$	I/O Status
Read	L	Data Out (DQ0–DQ8)
Read	H	High-Z
Write	X	High-Z — Data In (DQ0–DQ8)
Deselected	X	High-Z

NOTES:
1. X means Don't Care
2. For a write operation following a read operation, $\overline{G}$ must be high before the input data required setup time and held high throughout the input data hold time.

9

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to 7.0	V
Output Power Supply Voltage	V_{CCQ}	– 0.5 to V_{CC}	V
Voltage Relative to V_{SS}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation (T_A = 70°C, V_{CC} = 5 V, t_{KHKH} = 20 ns)	P_D	1.2	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions to taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, V_{CCQ} = 5.0 V or 3.3 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Output Buffer Supply Voltage (5.0 V TTL Compatible) (3.3 V 50 Ω Compatible	V_{CCQ}	 4.5 3.0	 5.0 3.3	 5.5 3.6	V
Input High Voltage	V_{IH}	2.2	3.0	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	– 0.5 *	0.0	0.8	V

* V_{IL} (min) = – 3.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{G}$, $\overline{S1}$ = V_{IH}, S0 = V_{IL}, V_{out} = 0 to V_{CCQ})	$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current ($\overline{G}$, $\overline{S1}$ = V_{IH}, S0 = V_{IL}, All Inputs = V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, I_{out} = 0 mA, Cycle Time ≥ t_{KHKH} min) MCM62940-14: t_{KHKH} = 20 ns MCM62940-24: t_{KHKH} = 25 ns MCM62940-19: t_{KHKH} = 30 ns	I_{CCA}	 — — —	 185 175 165	mA
Standby Current ($\overline{S1}$ = V_{IH}, S0 = V_{IL}, All Inputs = V_{IL} and V_{IH}, Cycle Time ≥ t_{KHKH} min)	I_{SB1}	—	40	mA
CMOS Standby Current ($\overline{S1}$ ≥ V_{CC} – 0.2 V, S0 ≤ 0.2 V, All Inputs ≥ V_{CC} – 0.2 V or ≤ 0.2 V, Cycle TIme ≥ t_{KHKH} min)	I_{SB2}	—	30	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

NOTE: Good decoupling of the local power supply should always be used. DC characteristics are guaranteed for all possible MC68040 bus cycles.

9

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance (All Pins Except DQ0–DQ8)	C_{in}	4	5	pF
Input/Output Capacitance (DQ0–DQ8)	$C_{I/O}$	8	10	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, V_{CCQ} = 5.0 V or 3.3 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns
Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol		MCM62940-14		MCM62940-19		MCM62940-24		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	t_{CYC}	20	—	25	—	30	—	ns	
Clock Access Time	t_{KHQV}	t_{CD}	—	14	—	19	—	24	ns	4
Output Enable to Output Valid	t_{GLQV}	t_{OE}	—	7	—	8	—	9	ns	
Clock High to Output Active	t_{KHQX1}	t_{DC1}	3	—	3	—	3	—	ns	
Clock High to Output Change	t_{KHQX2}	t_{DC2}	5	—	5	—	5	—	ns	
Output Enable to Output Active	t_{GLQX}	t_{OLZ}	0	—	0	—	0	—	ns	
Output Disable to Q High-Z	t_{GHQZ}	t_{OHZ}	—	7	—	8	—	9	ns	5
Clock High to Q High-Z	t_{KHQZ}	t_{CZ}	—	10	—	11	—	12	ns	
Clock High Pulse Width	t_{KHKL}	t_{CH}	8	—	9.5	—	11	—	ns	
Clock Low Pulse Width	t_{KLKH}	t_{CL}	8	—	9.5	—	11	—	ns	
Setup Times: Address Address Status Data In Write Address Advance Chip Select	t_{AVKH} t_{TSVKH} t_{DVKH} t_{WVKH} t_{BAVKH} t_{S0VKH} t_{S1VKH}	t_{AS} t_{SS} t_{DS} t_{WS}	3	—	3	—	3	—	ns	6
Hold Times: Address Address Status Data In Write Address Advance Chip Select	t_{KHAX} t_{KHTSX} t_{KHDX} t_{KHWX} t_{KHBAX} t_{KHS0X} t_{KHS1X}	t_{AH} t_{SH} t_{DH} t_{WH}	2	—	2	—	2	—	ns	6

NOTES:

1. A read cycle is defined by $\overline{W}$ high or $\overline{TSP}$ low for the setup and hold times. A write cycle is defined by $\overline{W}$ low and $\overline{TSP}$ high for the setup and hold times.
2. All read and write cycle timings are referenced from K or $\overline{G}$.
3. $\overline{G}$ is a don't care when $\overline{W}$ is sampled low.
4. Maximum access times are guaranteed for all possible MC68040 external bus cycles.
5. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{GHQZ} max is less than t_{GLQX} min for a given device and from device to device.
6. This is a synchronous device. All addresses must meet the specified setup and hold times for ***ALL*** rising edges of clock (K) whenever $\overline{TSP}$ or $\overline{TSC}$ are low and the chip is selected. All other synchronous inputs must meet the specified setup and hold times for ***ALL*** rising edges of K when the chip is selected.Chip select must be true ($\overline{S1}$ low and S0 high) at each rising edge of clock for the device (when $\overline{TSP}$ or $\overline{TSC}$ is low) to remain enabled. Timings for $\overline{S1}$ and S0 are similar.

AC TEST LOADS

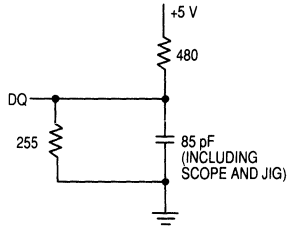


Figure 1A

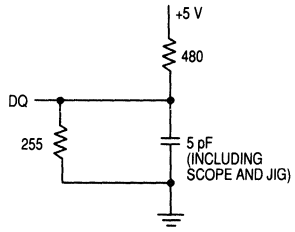
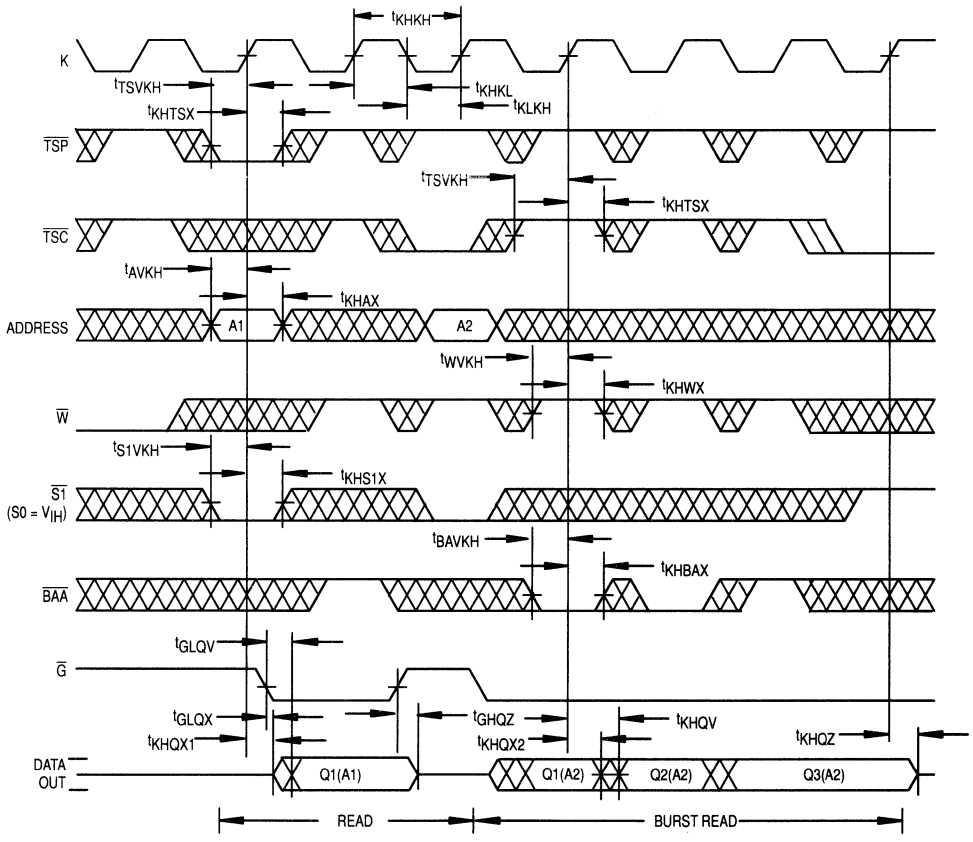


Figure 1B

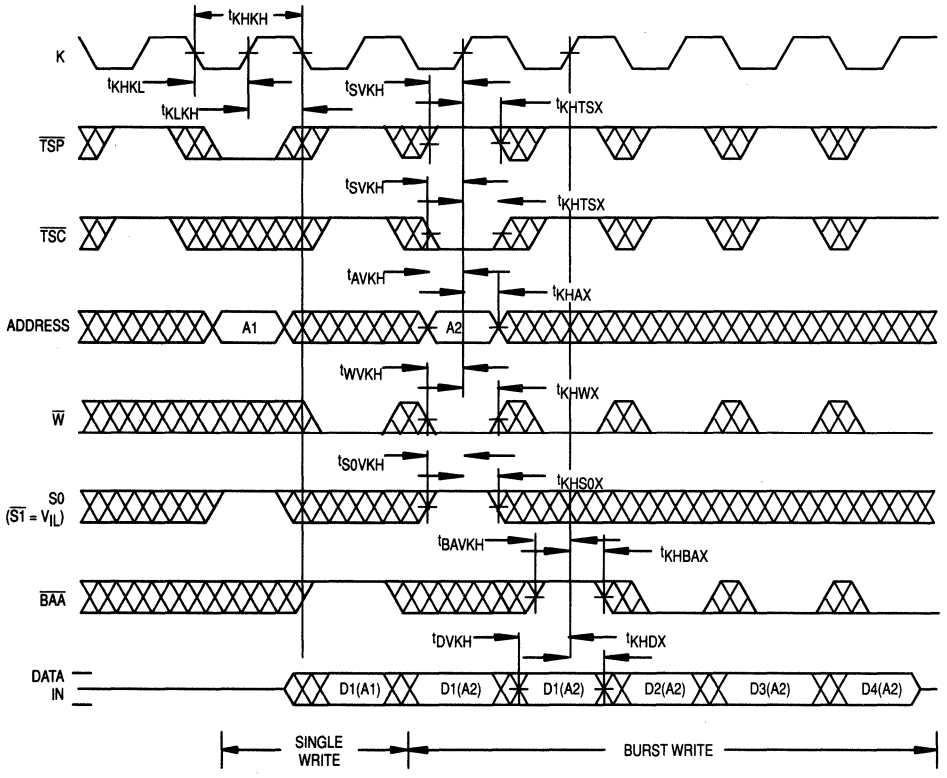
READ CYCLE



NOTE: Q1(A2) represents the first output from the external address A2; Q2(A2) represents the next output data in the burst sequence with A2 as the base address.

9

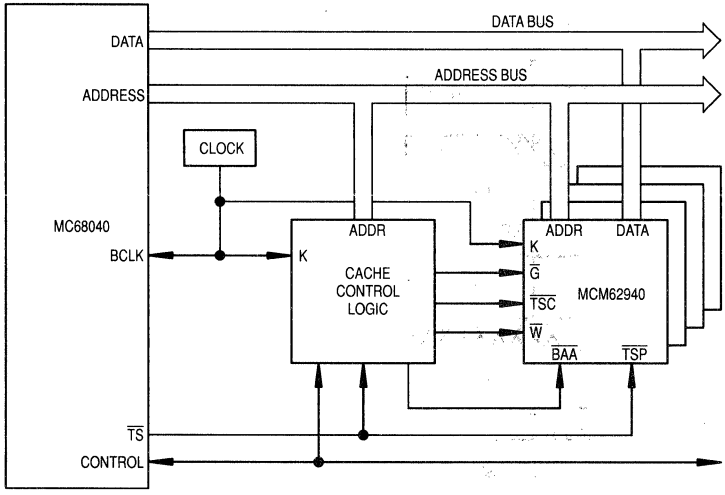
WRITE CYCLE



NOTE: $\overline{G} = V_{IH}$

9

APPLICATION EXAMPLE



128K BYTE BURSTABLE, SECONDARY CACHE
USING FOUR MCM62940FN24'S WITH A 33 MHz MC68040

ORDERING INFORMATION
(Order by Full Part Number)

MCM	62940	x	xx
Motorola Memory Prefix			Speed (14 = 14 ns, 19 = 19 ns, 24 = 24 ns)
Part Number			Package (FN = PLCC)

Full Part Number – MCM62940FN14 MCM62940FN19 MCM62940FN24

9

MCM62950

Product Preview

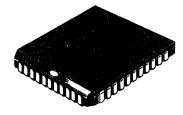
32K × 9 Bit Synchronous Static RAM

The MCM62950 is a 294,912 bit synchronous static random access memory organized as 32,768 words of 9 bits, fabricated using Motorola's high-performance silicon-gate CMOS technology. The device integrates input registers, high-speed SRAM, and high drive capability outputs onto a single monolithic circuit for reduced parts count implementation of cache data RAM applications. Synchronous design allows precise cycle control with the use of an external clock (K). Asynchronous controls consist of asynchronous write enable ($\overline{AW}$) and output enable ($\overline{G}$). CMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

Addresses (A0–A14) and control signals, except output enable ($\overline{G}$) and asynchronous write enable ($\overline{AW}$), are sampled through positive-edge-triggered noninverting registers. Data outputs are asynchronously controlled by $\overline{G}$.

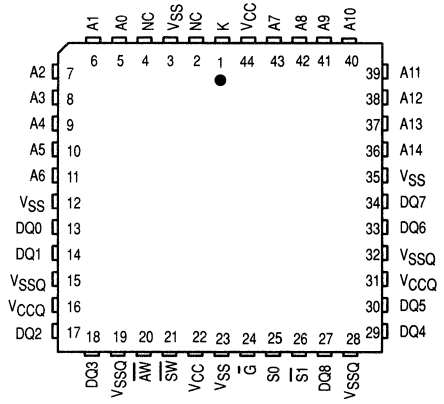
Write cycles are differentiated from read cycles by the state of the synchronous write enable pin ($\overline{SW}$) at the rising edge of K. Write cycles are completed only if $\overline{AW}$ is asserted within the specified setup time to the following rising edge of K. Write cycles may be aborted by negating the $\overline{AW}$ signal prior to the low going edge of K. Data for the write may be delayed until the latter half of the write cycle.

The MCM62950 is packaged in a 44-pin plastic leaded chip carrier (PLCC). Multiple power and ground pins have been utilized to minimize effects induced by output noise. Separate power and ground pins have been employed for DQ0–DQ8 to allow user-controlled output levels of 5 volts or 3.3 volts.



FN PACKAGE
44-LEAD PLCC
CASE 777

PIN ASSIGNMENT

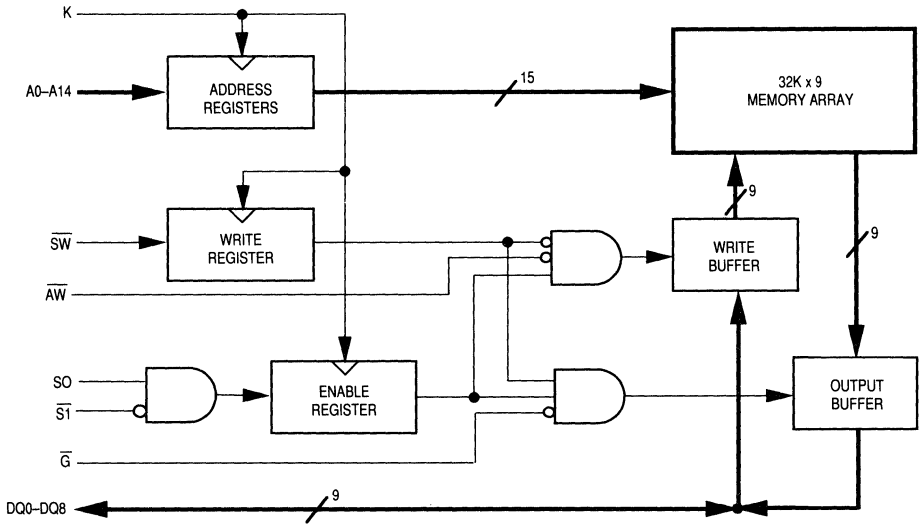


- Single 5 V ± 10% Power Supply
- Choice of 5 V or 3.3 V ± 10% Power Supplies for Output Level Compatibility
- Fast Access Times: 20/25 ns Max and Cycle Times: 20/25 ns Min
- Internal Input Registers (Address, Control)
- Late Write Abort Feature
- Output Enable Controlled Three-State Outputs
- Common Data Inputs and Data Outputs
- High Output Drive Capability: 85 pF per I/O
- High Board Density PLCC Package
- Fully TTL Compatible
- Active High and Low Chip Select Inputs for Easy Depth Expansion

PIN NAMES	
A0–A14	Address Inputs
K	Clock
$\overline{SW}$	Synchronous Write
$\overline{AW}$	Asynchronous Write
$\overline{G}$	Output Enable
S0, $\overline{S1}$	Chip Selects
DQ0–DQ8	Data Input/Output
V_{CC}	+5 V Power Supply
V_{CCQ}	Output Buffer Power Supply
V_{SS}	Ground
V_{SSQ}	Output Buffer Ground

All power supply and ground pins must be connected for proper operation of the device. $V_{CC} \geq V_{CCQ}$ at all times including power up.

BLOCK DIAGRAM



SYNCHRONOUS TRUTH TABLE (See Notes 1, 2, 3, and 4)

S	$\overline{SW}$	$\overline{AW}$	$\overline{G}$	K	Operation	I/O Status
F	X	X	X	L-H	Deselected	High-Z
T	L	X	X	L-H	Write	High-Z
(T)	(L)	L	X	L	Write	Data-In
(T)	(L)	H	X	L	Aborted Write (No Action)	High-Z
T	H	X	–	L-H	Read Initiated	–
(T)	(H)	X	H	X	Read	High-Z
(T)	(H)	X	L	X	Read	Data Out

NOTES:
1. X means Don't Care
2. S0, $\overline{S1}$, and $\overline{W}$ must meet setup and hold times for the low-to-high transition of clock (K).
3. S represents $\overline{S0}$ and S1. T implies $\overline{S1}$ = L and S0 = H; F implies $\overline{S1}$ = H or S0 = L.
4. $\overline{W}$ = (L) implies $\overline{W}$ = L for the last clock transition from low to high. Similarly for S = (T).

AC TEST LOADS

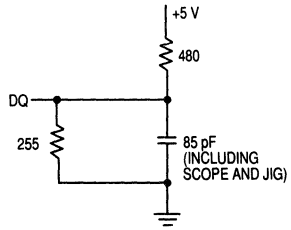


Figure 1A

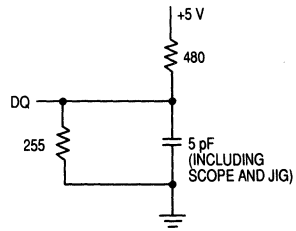


Figure 1B

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to 7.0	V
Output Power Supply Voltage	V_{CCQ}	– 0.5 to V_{CC}	V
Voltage Relative to V_{SS}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation (T_A = 70°C, V_{CC} = 5 V, t_{KHKH} = 20 ns)	P_D	1.2	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions to taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

DC OPERATING CONDITIONS AND CHARACTERISTICS
(V_{CC} = V_{CCQ} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Output Buffer Supply Voltage (5.0 V TTL Compatible) (3.3 V 50 Ω Compatible	V_{CCQ}	 4.5 3.0	 5.0 3.3	 5.5 3.6	V
Input High Voltage	V_{IH}	2.2	3.0	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	– 0.5*	0.0	0.8	V

* V_{IL} (min) = – 3.0 Vac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{G}$, $\overline{S1}$ = V_{IH}, S0 = V_{IL}, V_{out} = 0 to V_{CCQ})	$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current ($\overline{G}$, S0 = V_{IH}, $\overline{S1}$ = V_{IL}, All Inputs = V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, I_{out} = 0 mA, Cycle Time ≥ t_{KHKH} min) MCM62950-20: t_{KHKH} = 20 ns MCM62950-25: t_{KHKH} = 25 ns	I_{CCA}	— —	185 175	mA
Standby Current ($\overline{S1}$ = V_{IH}, S0 = V_{IL}, All Inputs = V_{IL} and V_{IH})	I_{SB1}	—	40	mA
CMOS Standby Current ($\overline{S1}$ ≥ V_{CC} – 0.2 V, S0 ≤ 0.2 V, All Inputs ≥ V_{CC} – 0.2 V or ≤ 0.2 V, Cycle TIme ≥ t_{KHKH} min)	I_{SB2}	—	30	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	0.1	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

NOTE: Good decoupling of the local power supply should always be used.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance (All Pins Except DQ0–DQ8)	C_{in}	4	5	pF
Input/Output Capacitance (DQ0–DQ8)	$C_{I/O}$	8	10	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = V_{CCQ} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

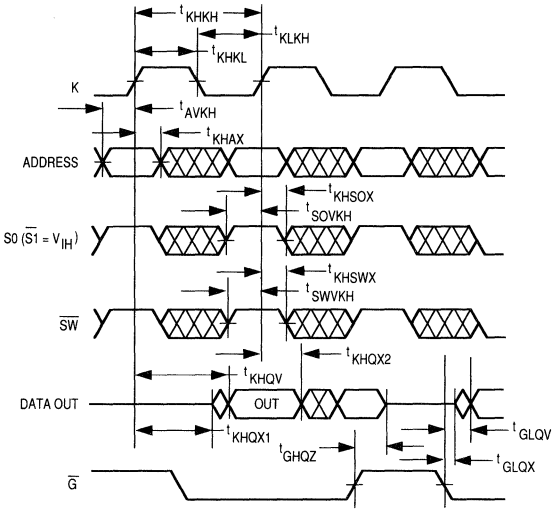
READ/WRITE CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol	MCM62950-20		MCM62950-25		Unit	Notes
		Min	Max	Min	Max		
Clock Control:						ns	
Cycle Time	t_{KHKH}	20	—	25	—		
Clock High Pulse Width	t_{KHKL}	8	—	11	—		
Clock Low Pulse Width	t_{KLKH}	8	—	11	—		
Read Access Times:						ns	
Clock Access Time	t_{KHQV}	—	20	—	25		
Output Enable to Output Valid	t_{GLQV}	—	8	—	9		
Aborted Write Cycles:						ns	
Clock Low to Asynchronous Write High	t_{KLAWH}	—	0	—	0		
Clock High to Asynchronous Write Invalid	t_{KHAWX}	2	—	2	—		
Write Cycles:						ns	
Asynchronous Write Low to Clock High	t_{AWLKH}	6	—	6	—		
Clock High to Asynchronous Write Invalid	t_{KHAWX}	2	—	2	—		
Data-In Valid to Clock High (Transparent Data)	t_{DVKH}	6	—	6	—		
Clock High to Data Invalid (Transparent Data)	t_{KHDX}	2	—	2	—		
Output Buffer Control:						ns	
Clock High to Output Low-Z after Write	t_{KHQX1}	8	—	8	—		
Clock High to Output Change	t_{KHQX2}	5	—	5	—		
Output Enable to Output Active	t_{GLQX}	0	—	0	—		
Output Disable to Q High-Z	t_{GHQZ}	—	8	—	9		4
Clock High to Q High-Z	t_{KHQZ}	—	10	—	10		4
Registe Setup Times for: Address	t_{AVKH}	3	—	3	—	ns	5
Synchronous Write	t_{WVKH}						
Chip Select	t_{S0VKH}, t_{S1VKH}						
Register Hold Times for: Address	t_{KHAX}	2	—	2	—	ns	5
Synchronous Write	t_{KHWX}						
Chip Select	t_{KHS0X}, t_{KHS1X}						

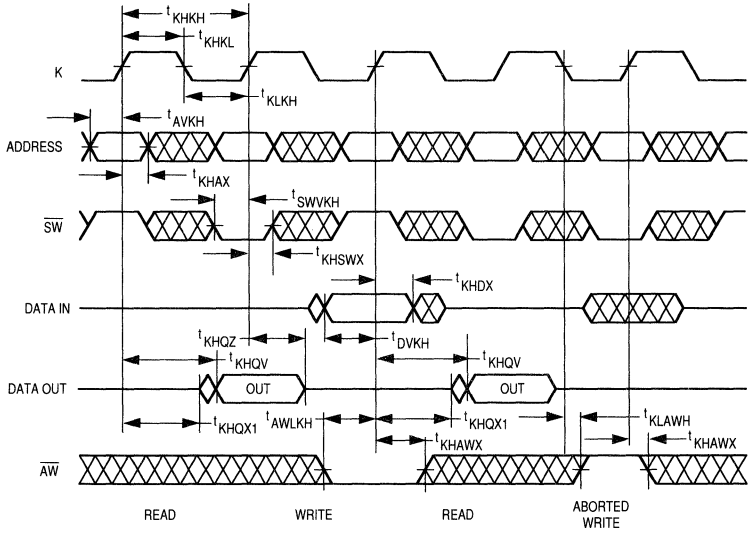
NOTES:
1. A read cycle is defined by $\overline{SW}$ high for the setup and hold times. A write cycle is defined by $\overline{SW}$ low for the setup and hold times.
2. All read and write cycle timings are referenced from K or $\overline{G}$.
3. $\overline{G}$ is a don't care when $\overline{SW}$ is sampled low.
4. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{GHQZ} max is less than t_{GLQX} min for a given device and from device to device.
5. This is a synchronous device. All address inputs must meet the specified setup and hold times with stable logic levels for ***ALL*** rising edges of clock (K) when the device is selected. All synchronous inputs must meet the specified setup and hold times with stable logic levels for **ALL** rising edges of clock (K) when the device is selected. Timings for $\overline{S1}$ and S0 are similar.

9

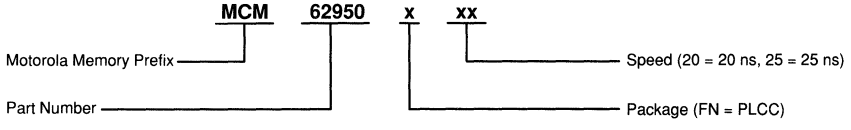
READ CYCLE



READ–WRITE–READ CYCLE

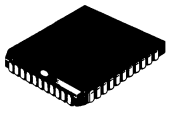


ORDERING INFORMATION
(Order by Full Part Number)



Full Part Number – MCM62950FN20 MCM62950FN25

MCM62960



FN PACKAGE
44-LEAD PLCC
CASE 777

Product Preview

32K × 9 Bit Synchronous Static RAM

The MCM62960 is a 294,912 bit synchronous static random access memory designed to provide a high-performance, cache for the SPARC™ Family of microprocessors. It is organized as 32,768 words of 9 bits, fabricated using Motorola's high-performance silicon-gate CMOS technology. The device integrates input registers, high-speed SRAM, and high drive capability outputs onto a single monolithic circuit for reduced parts count implementation of cache data RAM applications.

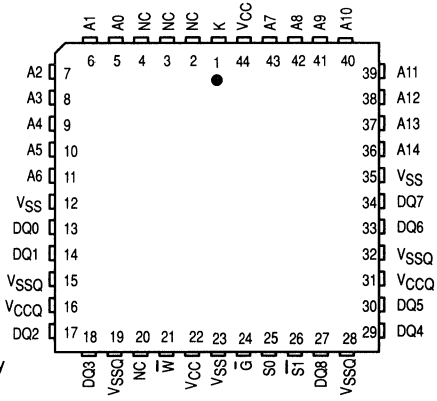
Synchronous design allows precise cycle control with the use of an external clock (K). CMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

Output enable ($\overline{G}$) is an asynchronous control input. Addresses (A0–A14) and chip select inputs (S0, $\overline{S1}$) are sampled through positive-edge-triggered, noninverting registers on the rising edge of the clock input (K). Write enable ($\overline{W}$) and data-in are sampled on the following edge of K through negative-edge-triggered, noninverting registers.

The MCM62960 is packaged in a 44-pin plastic leaded chip carrier (PLCC). Multiple power and ground pins have been utilized to minimize effects induced by output noise. Separate power and ground pins have been employed for DQ0–DQ8 to allow user-controlled output levels of 5 volts or 3.3 volts.

- Single 5 V ± 10% Power Supply
- Choice of 5 V or 3.3 V ± 10% Power Supplies for Output Level Compatibility
- Fast Access Times: 17/20/24 ns Max and Cycle Times: 20/25/30 ns Min
- Internal Input Registers (Address, Control, Data)
- Internally Self–Timed Write Cycle
- Output Enable Controlled Three-State Outputs
- Common Data Inputs and Data Outputs
- High Output Drive Capability: 85 pF per I/O
- High Board Density PLCC Package
- Fully TTL Compatible
- Active High and Low Chip Select Inputs for Easy Depth Expansion

PIN ASSIGNMENT



PIN NAMES	
A0–A14	Address Inputs
K	Clock
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
S0, $\overline{S1}$	Chip Selects
DQ0–DQ8	Data Input/Output
V_{CC}	+5 V Power Supply
V_{CCQ}	Output Buffer Power Supply
V_{SS}	Ground
V_{SSQ}	Output Ground
NC	No Connection

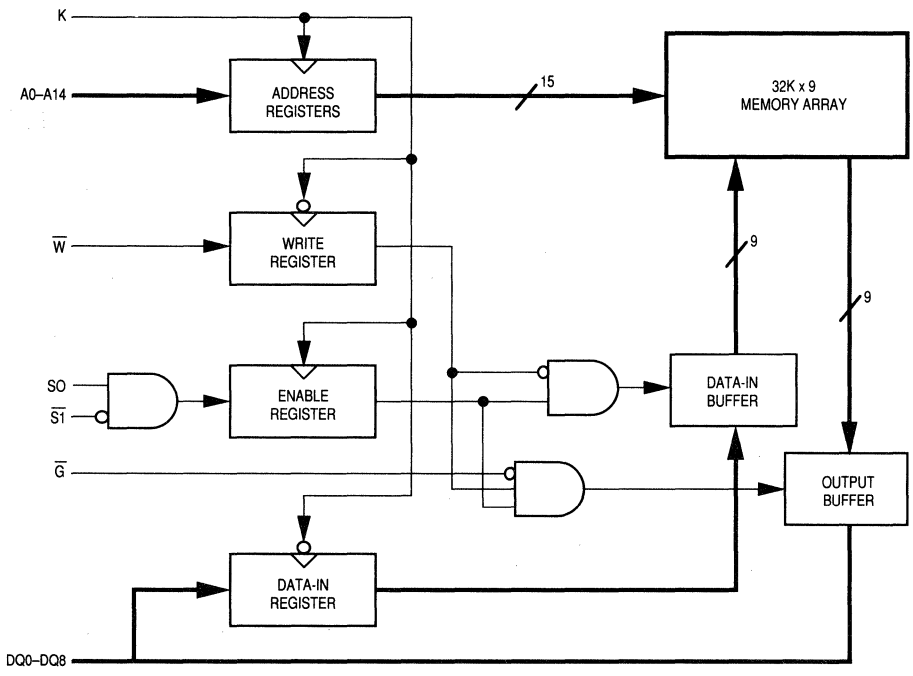
All power supply and ground pins must be connected for proper operation of the device. $V_{CC} \geq V_{CCQ}$ at all times including power up.

9

SPARC is a trademark of Sun Corp.

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

BLOCK DIAGRAM



TRUTH TABLE (See Notes 1, 2, 3, and 4)

S	$\overline{W}$	$\overline{G}$	Input/Output	Operation
F	X	X	High-Z	Deselected
T	H	L	Data Out	Read Cycle
T	H	H	High-Z	Read Cycle
T	L	H	Write Data In	WriteCycle

NOTES:

1. X means Don't Care
2. All address and chip select inputs must meet setup and hold times for ***ALL*** low-to-high transitions of clock (K). $\overline{W}$ input must meet setup and hold times for ***ALL*** high-to-low transitions of clock (K).
3. S represents S0 and $\overline{S1}$. T implies $\overline{S1}$ = L and S0 = H; F implies $\overline{S1}$ = H or S0 = L.
4. During a write cycle, $\overline{G}$ must be high before the input data required setup time and held high throughout the data hold time.

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to 7.0	V
Output Power Supply Voltage	V_{CCQ}	– 0.5 to V_{CC}	V
Voltage Relative to V_{SS}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation (T_A = 70°C, V_{CC} = 5 V, t_{KHKH} = 20 ns)	P_D	1.2	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions to taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = V_{CCQ} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Output Buffer Supply Voltage (5.0 V TTL Compatible) (3.3 V 50 Ω Compatible)	V_{CCQ}	 4.5 3.0	 5.0 3.3	 5.5 3.6	V
Input High Voltage	V_{IH}	2.2	3.0	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	– 0.5*	0.0	0.8	V

* V_{IL} (min) = – 3.0 Vac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{G}$, $\overline{S1}$ = V_{IH}, S0 = V_{IL}, V_{out} = 0 to V_{CCQ})	$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current ($\overline{G}$, S0 = V_{IH}, $\overline{S1}$ = V_{IL}, All Inputs = V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, I_{out} = 0 mA, Cycle Time ≥ t_{KHKH} min) MCM62960-20: t_{KHKH} = 25 ns MCM62960-24: t_{KHKH} = 30 ns	I_{CCA}	— —	175 165	mA
Standby Current ($\overline{S1}$ = V_{IH}, S0 = V_{IL}, All Inputs = V_{IL} and V_{IH}, Cycle Time ≥ t_{KHKH} min)	I_{SB1}	—	40	mA
CMOS Standby Current ($\overline{S1}$ ≥ V_{CC} – 0.2 V, S0 ≤ 0.2 V, All Inputs ≥ V_{CC} – 0.2 V or ≤ 0.2 V, Cycle Time ≥ t_{KHKH} min)	I_{SB2}	—	30	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

NOTE: Good decoupling of the local power supply should always be used.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance (All Pins Except DQ0–DQ8)	C_{in}	4	6	pF
Input/Output Capacitance (DQ0–DQ8)	$C_{I/O}$	8	10	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = V_{CCQ} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns
Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol	MCM62960-17		MCM62960-20		MCM62960-24		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Clock Control:								ns	
Cycle Time	t_{KHKH}	20	—	25	—	30	—		
Clock High Pulse Width	t_{KHKL}	8	—	10	—	12	—		
Clock Low Pulse Width	t_{KLKH}	8	—	10	—	12	—		
Read Cycles:								ns	
Clock Access Time	t_{KHQV}	—	17	—	20	—	24		
Output Enable to Output Valid	t_{GLQV}	—	7	—	8	—	9		
Output Buffer Control:								ns	
Clock High to Output Low-Z	t_{KHQX1}	3	—	3	—	3	—		
Clock High to Output Change	t_{KHQX2}	5	—	5	—	5	—		
Clock High to Q High-Z	t_{KHQZ}	10	—	11	—	12	—		
Output Enable to Output Active	t_{GLQX}	0	—	0	—	0	—		
Output Disable to Q High-Z	t_{GHQZ}	—	7	—	8	—	9		3
Register/Latch Setup Times: Address	t_{AVKH}	2	—	2	—	2	—	ns	4
Data	t_{DVKL}	3	—	3	—	3	—		
Write Enable	t_{WVKL}	2	—	2	—	2	—		
Chip Select	t_{S0VKH}	2	—	2	—	2	—		
	t_{S1VKH}	2	—	2	—	2	—		
Register/Latch Hold Times: Address	t_{KHAX}	3	—	3	—	3	—	ns	4
Data	t_{KLDX}	2	—	2	—	2	—		
Write Enable	t_{KLWX}	3	—	3	—	3	—		
Chip Select	t_{KHS0X}	3	—	3	—	3	—		
	t_{KHS1X}	3	—	3	—	3	—		

NOTES:
1. A read cycle is defined by $\overline{W}$ high for the setup and hold times. A write cycle is defined by $\overline{W}$ low for the setup and hold times.
2. All read and write cycle timings are referenced from K or $\overline{G}$.
3. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{GHQZ} max is less than t_{GLQX} min for a given device and from device to device.
4. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for **ALL** rising (or falling in the case of $\overline{W}$ and Data In) edges of clock (K) when the device is selected. To select or deselect the device, both chip selects must be valid at the rising edge of K. Timings for $\overline{S1}$ and S0 are similar.

9

AC TEST LOADS

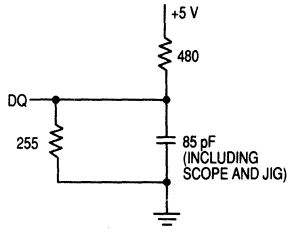


Figure 1A

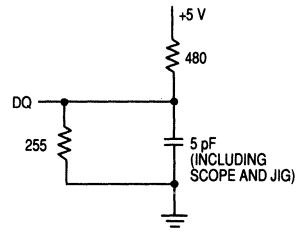
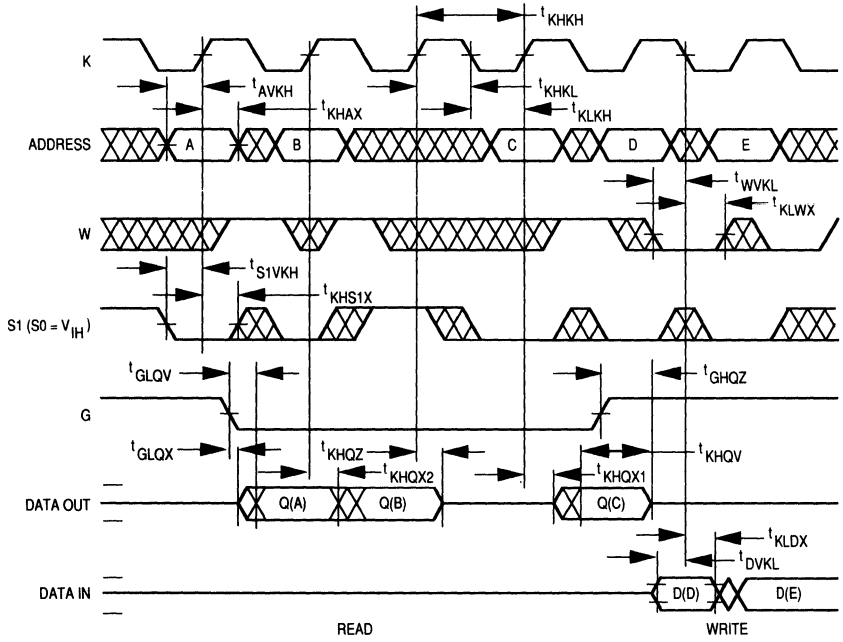


Figure 1B

READ – WRITE CYCLE



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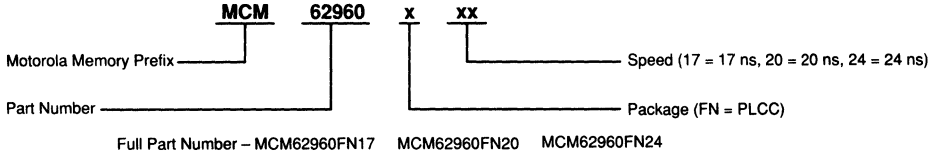
ORDERING INFORMATION
(Order by Full Part Number)

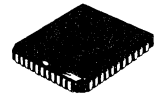


MCM62963

Product Preview

4K x 10 Bit Synchronous Static RAM

with Output Registers



FN PACKAGE
44-LEAD PLCC
CASE 777

The MCM62963 is a 40,960 bit synchronous static random access memory organized as 4096 words of 10 bits, fabricated using Motorola's second-generation high-performance silicon-gate CMOS (HCMOS III) technology. The device integrates input registers, high speed SRAM, and high-drive capability output registers onto a single monolithic circuit. This allows reduced parts count implementation of cache data RAM, writeable control store applications, and other applications that utilize long words.

Synchronous design allows precise cycle control with the use of an external clock (K), while CMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

The address (A0–A11), data (D0–D9), write ($\overline{W}$), and chip enable ($\overline{E}$) inputs are all clock (K) controlled, positive-edge-triggered, noninverting registers.

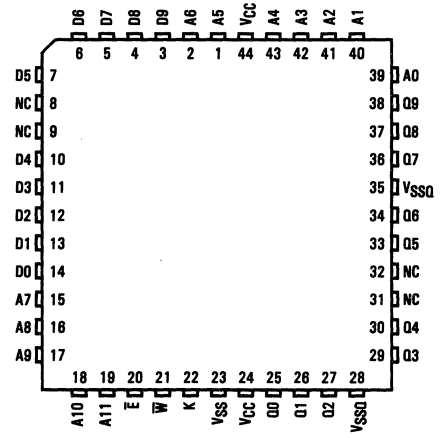
The chip enable ($\overline{E}$) input is a synchronous input clock that places the device in a low power mode when high at the rising edge of the clock (K).

The MCM62963 provides output register operation. At the rising edge of clock (K), the RAM data from the previous clock (K) high cycle is presented.

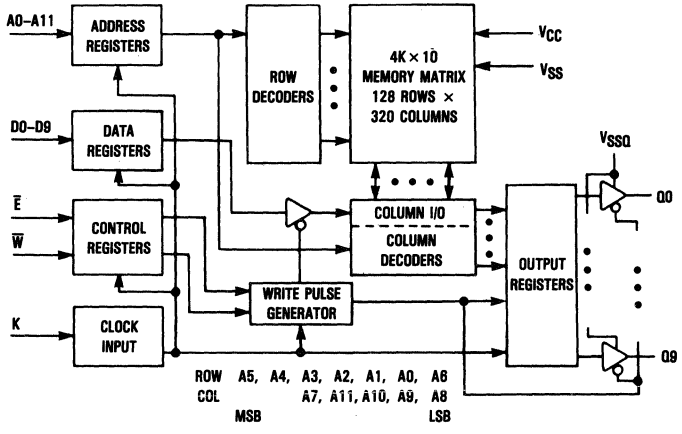
Write operations are internally self-timed and initiated by the rising edge of the clock (K) input. This feature eliminates complex off-chip write pulse generation and provides increased flexibility for incoming signals.

- Single 5 V ±10% Power Supply
- Fast Cycle Times: 18/20/25/30 ns Max
- Fast Clock (K) Access Times: 10/10/10/13 ns Max
- Address, Data Input, $\overline{E}$, and $\overline{W}$ Registers On-Chip
- Output Registers for Fully Pipelined Applications
- High Output Drive Capability
- Internally Self-Timed Write Pulse Generation
- Separate Data Input and Data Output Pins

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES	
A0-A11	Address Inputs
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
D0-D9	Data Inputs
Q0-Q9	Data Outputs
K	Clock Input
V_{CC}	+5 V Power Supply
V_{SS}	Ground
V_{SSQ}	Output Buffer Ground
NC	No Connection

For proper operation of the device V_{SS} and both V_{SSQ} leads must be connected to ground.

TRUTH TABLE

$\overline{E}$	$\overline{W}$	Operation	Q0-Q9	Current
L	L	Write	High Z	I_{CC}
L	H	Read	D_{out}	I_{CC}
H	X	Not Selected	High Z	I_{SB}

NOTE: The values of $\overline{E}$ and $\overline{W}$ are valid inputs for the setup and hold times relative to the K rising edge.

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to $V_{SS}=V_{SSQ}=0$ V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS}/V_{SSQ} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC}+0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation (T_A=25°C)	P_D	1.5	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for **ALL** rising edges of clock (K) while the device is selected.

This device contains circuitry that will ensure the output devices are in High Z at power up. Care should be taken by the user to ensure that all clocks are at V_{IL} or V_{IH} during power up to prevent spurious read cycles from occurring.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC}=5.0 V ±10%, T_A=0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to $V_{SS}=V_{SSQ}=0$ V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

*V_{IL} (min) = −3.0 V ac (pulse width ≤20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in}=0 to V_{CC})	$I_{lkg(I)}$	—	±1.0	μA
Output Leakage Current ($\overline{E}=V_{IH}$, V_{out}=0 to V_{CC}, Outputs must be high-Z)	$I_{lkg(O)}$	—	±1.0	μA
AC Supply Current ($\overline{E}=V_{IL}$, All Inputs=V_{IL} or V_{IH}, I_{out}=0 mA, Cycle Time≥t_{KHKH} min)	I_{CCA}			mA
MCM62963-18: t_{KHKH}=18 ns		—	180	
MCM62963-20: t_{KHKH}=20 ns		—	170	
MCM62963-25: t_{KHKH}=25 ns		—	170	
MCM62963-30: t_{KHKH}=30 ns		—	150	
Standby Current ($\overline{E}=V_{IH}$, V_{IH}≥3.0 V, V_{IL}≤0.4 V, I_{out}=0 mA, Cycle Time≥=t_{KHKH} min)	I_{SB}	—	30	mA
Output Low Voltage (I_{OL}=12.7 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH}=−1.8 mA)	V_{OH}	2.8	—	V

CAPACITANCE (f=1.0 MHz, dV=3.0 V, T_A=25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	4	6	pF
Output Capacitance	C_{out}	5	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . .0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns

Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load. . . . . .See Figure 1A Unless Otherwise Noted

READ CYCLE (See Note 1)

Parameter	Symbol	MCM62963-18		MCM62963-20		MCM62963-25		MCM62963-30		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{KHKH}	18	–	20	–	25	–	30	–	ns	2
Clock Access Time	t_{KHQV}	–	10	–	10	–	10	–	13	ns	3
Output Active from Clock High	t_{KHQX}	3	–	3	–	3	–	3	–	ns	4
Clock High to Q High Z ($\overline{E}$=V_{IH})	t_{KHQZ}	–	10	–	10	–	10	–	13	ns	4
Clock Low Pulse Width	t_{KLKH}	5	–	5	–	5	–	5	–	ns	
Clock High Pulse Width	t_{KHKL}	5	–	5	–	5	–	5	–	ns	
Setup Times for: $\overline{E}$	t_{EVKH}	5	–	5	–	5	–	5	–	ns	5
A	t_{AVKH}										
$\overline{W}$	t_{WHKH}										
Hold Times for: $\overline{E}$	t_{KHEX}	3	–	3	–	3	–	3	–	ns	5
A	t_{KHAX}										
$\overline{W}$	t_{KHWX}										

NOTES:
1. A read is defined by $\overline{W}$ high and $\overline{E}$ low for the setup and hold times.
2. All read cycle timing is referenced from K.
3. Valid data from K high will be the data stored at the address of the last valid read cycle.
4. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B. This parameter is sampled not 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQX} min for a given device.
5. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for **ALL** rising edges of clock (K) while the device is selected.

9

AC TEST LOADS

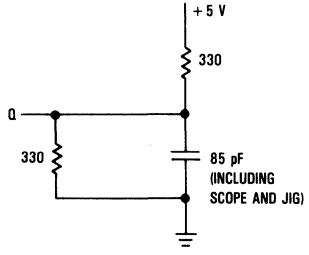


Figure 1A

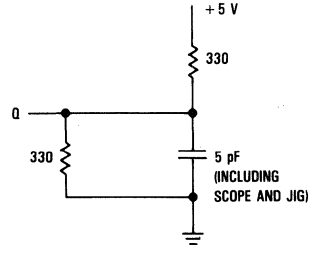
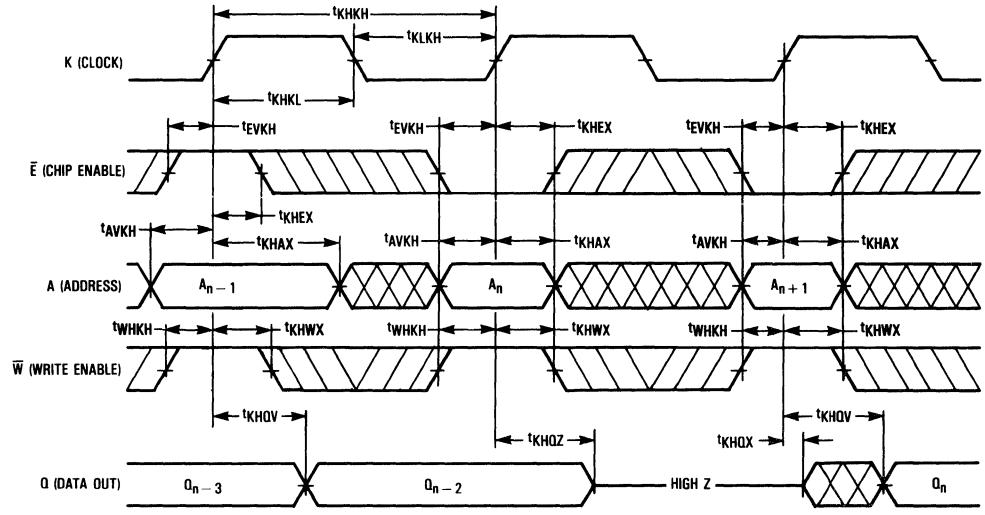
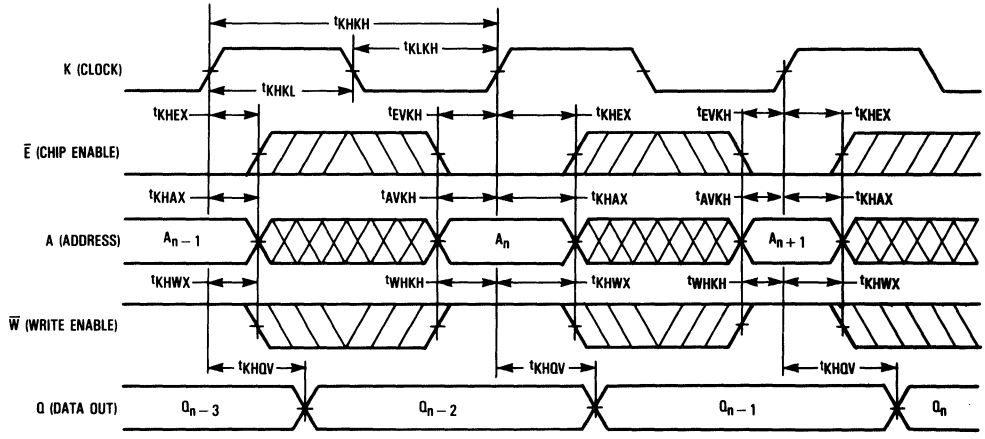


Figure 1B

READ CYCLE 1 (See Note 1)



READ CYCLE 2 (See Note 1)



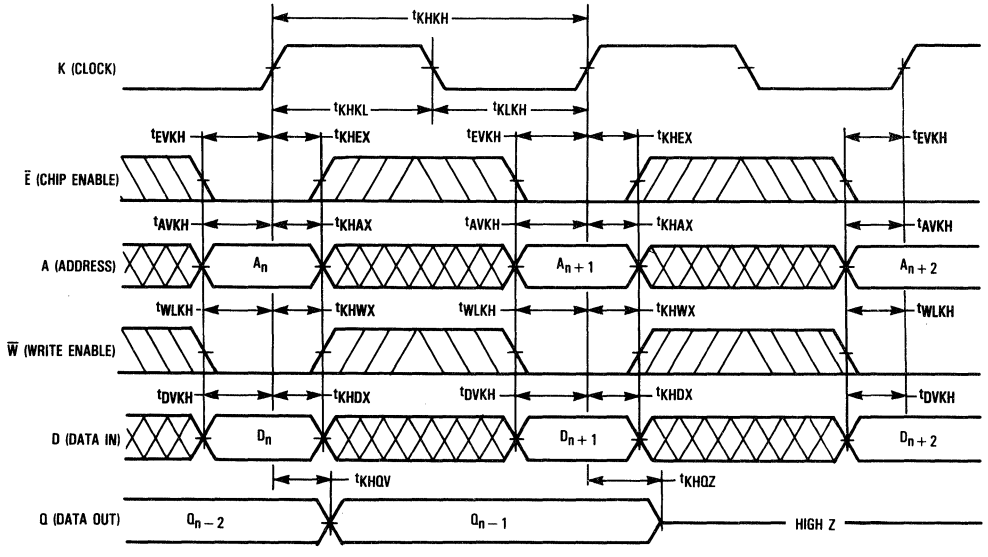
NOTE:
1. The outputs Q_{n-3} and Q_{n-2} are derived from two previous read cycles where $\overline{W} = V_{IH}$ and $\overline{E} = V_{IL}$ for those cycles.

WRITE CYCLE ($\overline{W}$ Controlled, See Note 1)

Parameter		Symbol	MCM62963-18		MCM62963-20		MCM62963-25		MCM62963-30		Unit	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time		t_{KHKH}	18	–	20	–	25	–	30	–	ns	2
Clock High to Q High Z ($\overline{W}=V_{IL}$)		t_{KHQZ}	–	10	–	10	–	10	–	13	ns	3
Setup Times for:	$\overline{E}$	t_{EVKH}	5	–	5	–	5	–	5	–	ns	4
	A	t_{AVKH}										
	$\overline{W}$	t_{WLKH}										
	D	t_{DVKH}										
Hold Times for:	$\overline{E}$	t_{KHEX}	3	–	3	–	3	–	3	–	ns	4
	A	t_{KHAX}										
	$\overline{W}$	t_{KHWX}										
	D	t_{KHDX}										

NOTES:
1. A write is performed when $\overline{W}$ and $\overline{E}$ are both low for the specified setup and hold times.
2. All write cycle timing is referenced from K.
3. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B. This parameter is sampled not 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQX} min for a given device.
4. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for **ALL** rising edges of clock (K) while the device is selected.

WRITE CYCLE



ORDERING INFORMATION
(Order by Full Part Number)

MCM 62963 X XX

Motorola Memory Prefix

Part Number

Speed (18 = 18 ns, 20 = 20 ns, 25 = 25 ns, 30 = 30 ns)

Package (FN = PLCC)

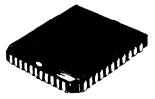
Full Part Numbers — MCM62963FN18 MCM62963FN20 MCM62963FN25 MCM62963FN30

MCM62964

Product Preview

4K × 10 Bit Synchronous Static RAM

with Output Registers and Output Enable



FN PACKAGE
44-LEAD PLCC
CASE 777

The MCM62964 is a 40,960 bit synchronous static random access memory organized as 4096 words of 10 bits, fabricated using Motorola's second-generation high-performance silicon-gate CMOS (HCMOS III) technology. The device integrates input registers, high speed SRAM, and high-drive capability output registers onto a single monolithic circuit for reduced parts count implementation of cache data RAM, writeable control store applications, and other applications that utilize long words.

Synchronous design allows precise cycle control with the use of an external clock (K), while CMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

The address (A0–A11), data (D0–D9), and write ($\overline{W}$) inputs are all clock (K) controlled, positive-edge-triggered, noninverting registers.

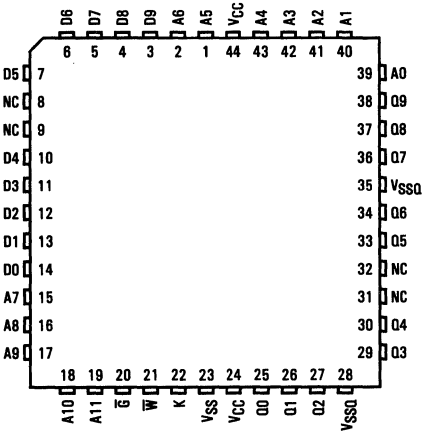
The MCM62964 provides output register operation. At the rising edge of clock (K), the RAM data from the previous clock (K) high cycle is presented.

The output enable ($\overline{G}$) provides asynchronous bus control for common I/O or bank switch applications.

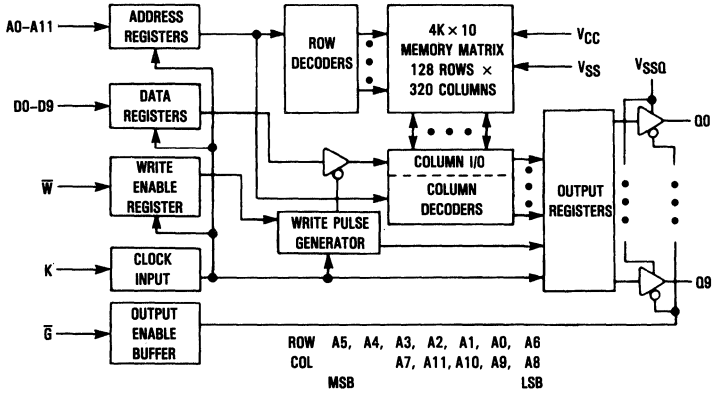
Write operations are internally self-timed and initiated by the rising edge of the clock (K) input. This feature eliminates complex off-chip write pulse generation and provides increased flexibility for incoming signals.

- Single 5 V ±10% Power Supply
- Fast Cycle Times: 20/25/30 ns Max
- Fast Clock (K) Access Times: 10/10/13 ns Max
- Address, Data Input, and $\overline{W}$ Registers On-Chip
- Output Enable for Asynchronous Bus Control
- Output Registers for Fully Pipelined Applications
- High Output Drive Capability
- Internally Self-Timed Write Pulse Generation
- Separate Data Input and Data Output Pins

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES	
A0-A11	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
D0-D9	Data Inputs
Q0-Q9	Data Outputs
K	Clock Input
V_{CC}	+5 V Power Supply
V_{SS}	Ground
V_{SSQ}	Output Buffer Ground
NC	No Connection

For proper operation of the device V_{SS} and both V_{SSQ} leads must be connected to ground.

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

TRUTH TABLE

$\overline{W}$	Operation	Q0-Q9	Current
L	Write	High Z	I_{CCA}
H	Read	D_{out}	I_{CCA}

NOTE: The value $\overline{W}$ is a valid input for the setup and hold times relative to the K rising edge.

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to $V_{SS}=V_{SSQ}=0$ V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS}/V_{SSQ} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC}+0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation (T_A=25°C)	P_D	1.5	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for ALL rising edges of clock (K) while the device is selected.

This device contains circuitry that will ensure the output devices are in High Z at power up. Care should be taken by the user to ensure that all clocks are at V_{IL} or V_{IH} during power up to prevent spurious read cycles from occurring.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC}=5.0 V ±10%, T_A=0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to $V_{SS}=V_{SSQ}=0$ V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	–	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	−0.5*	–	0.8	V

*V_{IL} (min) = −3.0 V ac (pulse width ≤20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in}=0 to V_{CC})	$I_{lkg(I)}$	–	±1.0	μA
Output Leakage Current ($\overline{G}=V_{IH}$, V_{out}=0 to V_{CC}, Outputs must be high-Z)	$I_{lkg(O)}$	–	±1.0	μA
AC Supply Current ($\overline{G}=V_{IL}$, All Inputs=V_{IL} or V_{IH}, I_{out}=0 mA, Cycle Time≥t_{KHKH} min)	I_{CCA}			mA
MCM62964-20: t_{KHKH}=20 ns		–	170	
MCM62964-25: t_{KHKH}=25 ns		–	170	
MCM62964-30: t_{KHKH}=30 ns		–	150	
Output Low Voltage (I_{OL}=12.7 mA)	V_{OL}	–	0.4	V
Output High Voltage (I_{OH}=−1.8 mA)	V_{OH}	2.8	–	V

CAPACITANCE (f=1.0 MHz, dV=3.0 V, T_A=25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	4	6	pF
Output Capacitance	C_{out}	5	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . .0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns

Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load . . . . . .See Figure 1A Unless Otherwise Noted

READ/WRITE CYCLE

Parameter	Symbol	MCM62964-20		MCM62964-25		MCM62964-30		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{KHKH}	20	–	25	–	30	–	ns	1, 3
Write Cycle Time	t_{KHKH}	20	–	25	–	30	–	ns	2, 3
Clock High Access Time	t_{KHQV}	–	10	–	10	–	13	ns	3, 4
$\overline{G}$ Low to Output Valid	t_{GLQV}	–	10	–	10	–	13	ns	3
Output Active from Clock High	t_{KHQX}	0	–	0	–	0	–	ns	
Output Active from $\overline{G}$ Low	t_{GLQX}	0	–	0	–	0	–	ns	
Clock Low Pulse Width	t_{KLKH}	5	–	5	–	5	–	ns	
Clock High Pulse Width	t_{KHKL}	5	–	5	–	5	–	ns	
Setup Times for: A	t_{AVKH}	5	–	5	–	5	–	ns	1, 2, 5
D	t_{DVKH}								
$\overline{W}$	t_{WVKH}								
Hold Times for: A	t_{KHAX}	3	–	3	–	3	–	ns	1, 2, 5
D	t_{KHDX}								
$\overline{W}$	t_{KHWX}								
Clock High to Output High Z ($\overline{W}$ = V_{IL})	t_{KHQZ}	0	10	0	10	0	13	ns	3, 6
$\overline{G}$ High to Output High Z	t_{GHQZ}	0	10	0	10	0	13	ns	3, 6, 7

NOTES:
1. A read is defined by $\overline{W}$ high for the specified setup and hold times.
2. A write is defined by $\overline{W}$ low for the specified setup and hold times.
3. All read and write cycle timing is referenced from K or from $\overline{G}$.
4. Valid data from K high will be the data stored at the address of the last valid read cycle.
5. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for **ALL** rising edges of clock (K) while the device is selected.
6. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQX} min and t_{GHQZ} max is less than t_{GLQX} min for a given device.
7. $\overline{G}$ becomes a don't care signal for successive writes after the first write cycle.

9

AC TEST LOADS

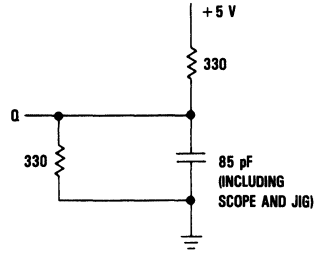


Figure 1A

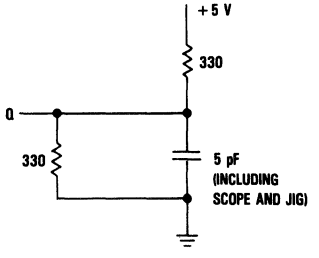
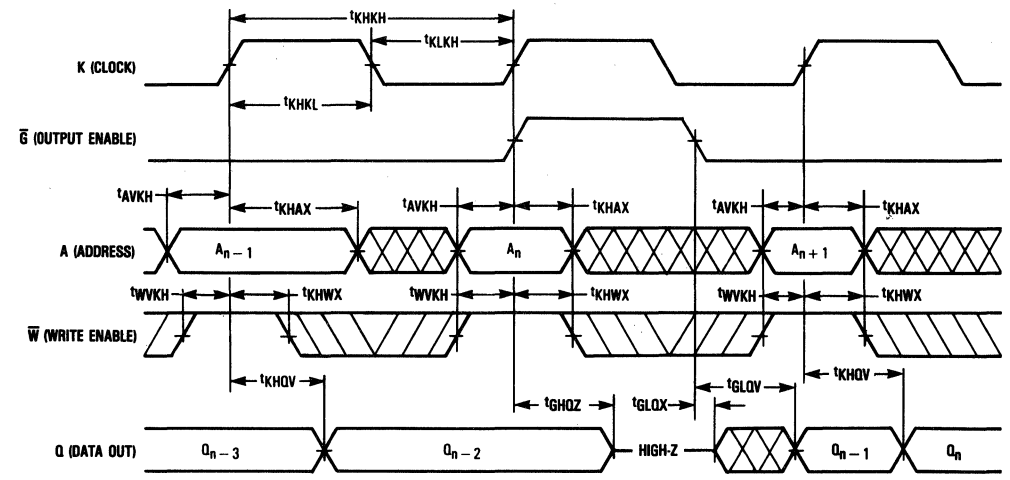
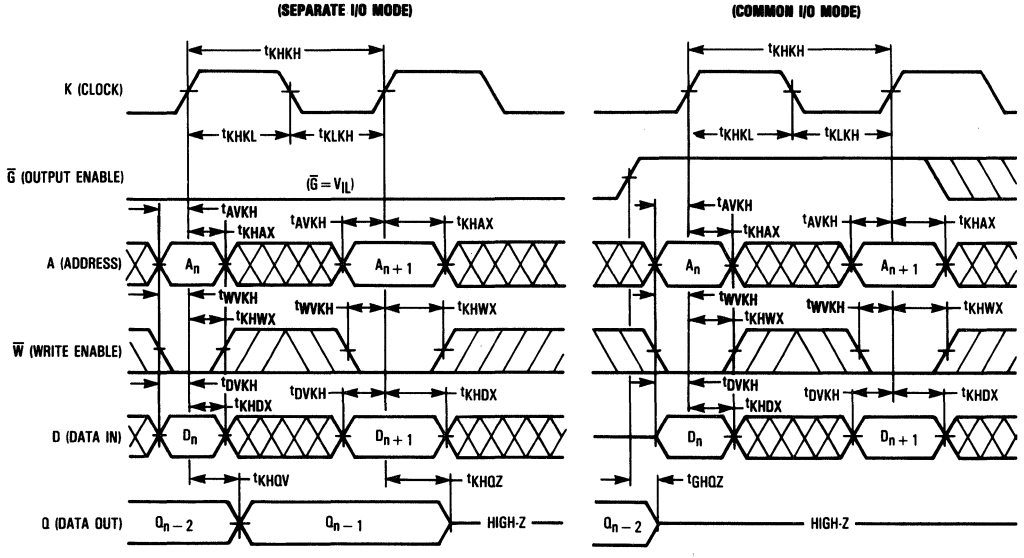


Figure 1B

READ CYCLE



WRITE CYCLE



ORDERING INFORMATION
(Order by Full Part Number)

MCM 62964 X XX

- MCM — Motorola Memory Prefix
- 62964 — Part Number
- X — Package (FN = PLCC)
- XX — Speed (20 = 20 ns, 25 = 25 ns, 30 = 30 ns)

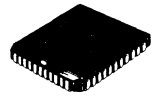
Full Part Numbers — MCM62964FN20 MCM62964FN25 MCM62964FN30

MCM62965

Product Preview

4K × 10 Bit Synchronous Static RAM

with Transparent Outputs and Output Enable



FN PACKAGE
44-LEAD PLCC
CASE 777

The MCM62965 is a 40,960 bit synchronous static random access memory organized as 4096 words of 10 bits, fabricated using Motorola's second-generation high-performance silicon-gate CMOS (HCMOS III) technology. The device integrates input registers, high speed SRAM, and high-drive capability output latching onto a single monolithic circuit for reduced parts count implementation of cache data RAM, writeable control store applications, and other applications that utilize long words.

Synchronous design allows precise cycle control with the use of an external clock (K), while CMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

The address (A0–A11), data (D0–D9), and write ($\overline{W}$) inputs are all clock (K) controlled, positive-edge-triggered, noninverting registers.

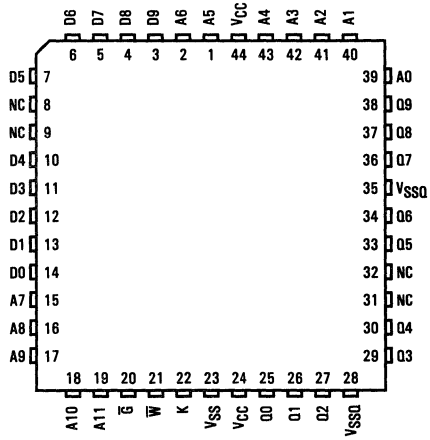
The MCM62965 provides transparent output operation when clock (K) is low for access of RAM data within the same cycle (output data is latched when clock (K) is high).

The output enable ($\overline{G}$) provides asynchronous bus control for common I/O or bank switch applications.

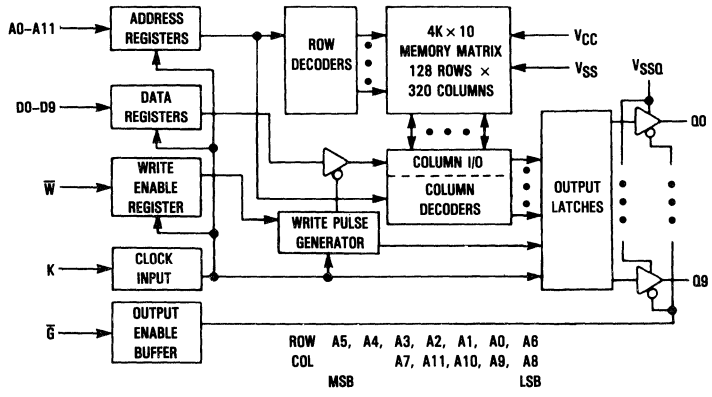
Write operations are internally self-timed and initiated by the rising edge of the clock (K) input. This feature eliminates complex off-chip write pulse generation and provides increased flexibility for incoming signals.

- Single 5 V ±10% Power Supply
- Fast Cycle Times: 25/30/35 ns Max
- Fast Clock (K) Access Times: 10/13/15 ns Max
- Address, Data Input, and $\overline{W}$ Registers On-Chip
- Transparent Output Latch for Access Within the Same Cycle
- Output Enable for Asynchronous Bus Control
- High Output Drive Capability
- Internally Self-Timed Write Pulse Generation
- Separate Data Input and Data Output Pins

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES	
A0-A11	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
D0-D9	Data Inputs
Q0-Q9	Data Outputs
K	Clock Input
V_{CC}	+5 V Power Supply
V_{SS}	Ground
V_{SSQ}	Output Buffer Ground
NC	No Connection

For proper operation of the device V_{SS} and both V_{SSQ} leads must be connected to ground.

TRUTH TABLE

$\overline{W}$	Operation	Q0-Q9	Current
L	Write	High Z	I_{CCA}
H	Read	D_{out}	I_{CCA}

NOTE: The value $\overline{W}$ is a valid input for the setup and hold times relative to the K rising edge.

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to $V_{SS}=V_{SSQ}=0$ V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS}/V_{SSQ} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC}+0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation ($T_A=25°C$)	P_D	1.5	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for **ALL** rising edges of clock (K) while the device is selected.

This device contains circuitry that will ensure the output devices are in High Z at power up. Care should be taken by the user to ensure that all clocks are at V_{IL} or V_{IH} during power up to prevent spurious read cycles from occurring.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{CC}=5.0$ V ±10%, $T_A=0$ to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to $V_{SS}=V_{SSQ}=0$ V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	–	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	−0.5*	–	0.8	V

*V_{IL} (min) = −3.0 V ac (pulse width ≤20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, $V_{in}=0$ to V_{CC})	$I_{lkg(I)}$	–	±1.0	μA
Output Leakage Current ($\overline{G}=V_{IH}$, $V_{out}=0$ to V_{CC}, Outputs must be high-Z)	$I_{lkg(O)}$	–	±1.0	μA
AC Supply Current ($\overline{G}=V_{IL}$, All Inputs = V_{IL} or V_{IH}, $I_{out}=0$ mA, Cycle Time ≥ t_{KHKH} min)	I_{CCA}			mA
MCM62965-25: $t_{KHKH}=25$ ns		–	170	
MCM62965-30: $t_{KHKH}=30$ ns		–	170	
MCM62965-35: $t_{KHKH}=35$ ns		–	150	
Output Low Voltage ($I_{OL}=12.7$ mA)	V_{OL}	–	0.4	V
Output High Voltage ($I_{OH}=-1.8$ mA)	V_{OH}	2.8	–	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, $T_A=25°C$, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	4	6	pF
Output Capacitance	C_{out}	5	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . .0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns

Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load . . . . . .See Figure 1A Unless Otherwise Noted

READ/WRITE CYCLE

Parameter		Symbol	MCM62965-25		MCM62965-30		MCM62965-35		Unit	Notes
			Min	Max	Min	Max	Min	Max		
Read Cycle Time		t_{KHKH}	25	–	30	–	35	–	ns	1, 3
Write Cycle Time		t_{KHKH}	25	–	30	–	35	–	ns	2, 3
Clock High Access Time		t_{KHQV}	–	25	–	30	–	35	ns	3, 4, 5
Clock Low to Output Valid		t_{KLQV}	–	10	–	13	–	15	ns	3, 4, 5
$\overline{G}$ Low to Output Valid		t_{GLQV}	–	10	–	13	–	15	ns	3
Output Active from Clock Low		t_{KLQX}	0	–	0	–	0	–	ns	
Output Active from $\overline{G}$ Low		t_{GLQX}	0	–	0	–	0	–	ns	
Clock Low Pulse Width		t_{KLKH}	5	–	5	–	5	–	ns	
Clock High Pulse Width		t_{KHKL}	5	–	5	–	5	–	ns	
Setup Times for:	A	t_{AVKH}	5	–	5	–	5	–	ns	1, 2, 6
	D	t_{DVKH}								
	$\overline{W}$	t_{WHKH}								
Hold Times for:	A	t_{KHAX}	3	–	3	–	3	–	ns	1, 2, 6
	D	t_{KHDX}								
	$\overline{W}$	t_{KHWX}								
Clock Low to Output High Z ($\overline{W}$ = V_{IL})		t_{KLQZ}	0	10	0	13	0	15	ns	5, 7
$\overline{G}$ High to Output High Z		t_{GHQZ}	0	10	0	13	0	15	ns	3, 7, 8

NOTES:
1. A read is defined by $\overline{W}$ high for the specified setup and hold times.
2. A write is defined by $\overline{W}$ low for the specified setup and hold times.
3. All read and write cycle timing is referenced from K or from $\overline{G}$.
4. Access time is controlled by t_{KLQV} if the clock high pulse width ≥ ($t_{KHQV} - t_{KLQV}$); otherwise it is controlled by t_{KHQV}.
5. K must be low for the outputs to transition.
6. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for **ALL** rising edges of clock (K) while the device is selected.
7. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQX} min and t_{GHQZ} max is less than t_{GLQX} min for a given device.
8. $\overline{G}$ becomes a don't care signal for successive writes after the first write cycle.

9

AC TEST LOADS

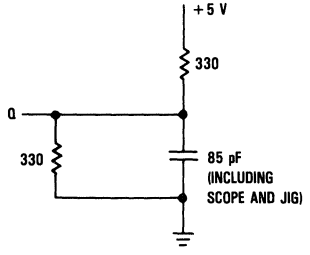


Figure 1A

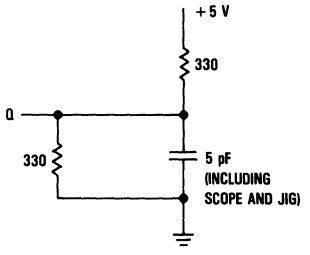
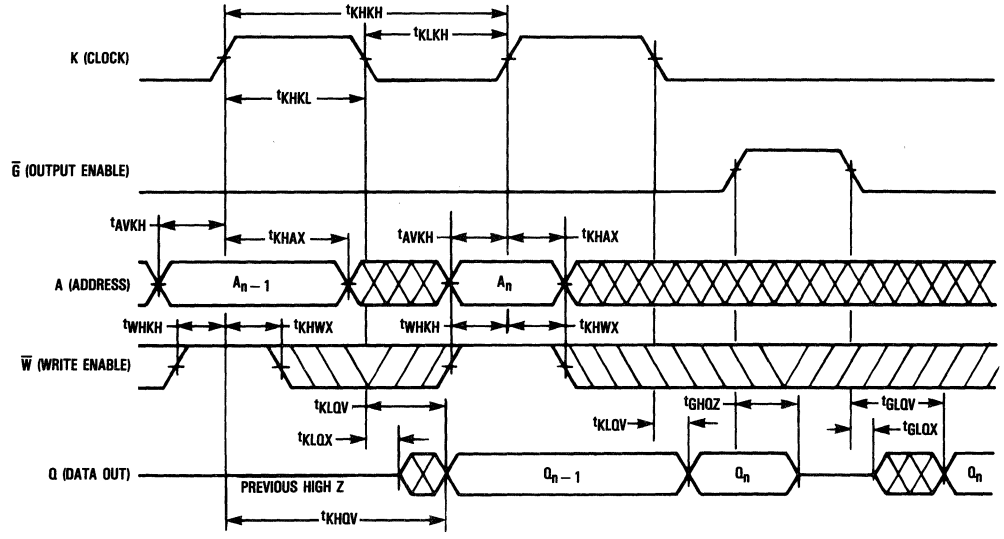
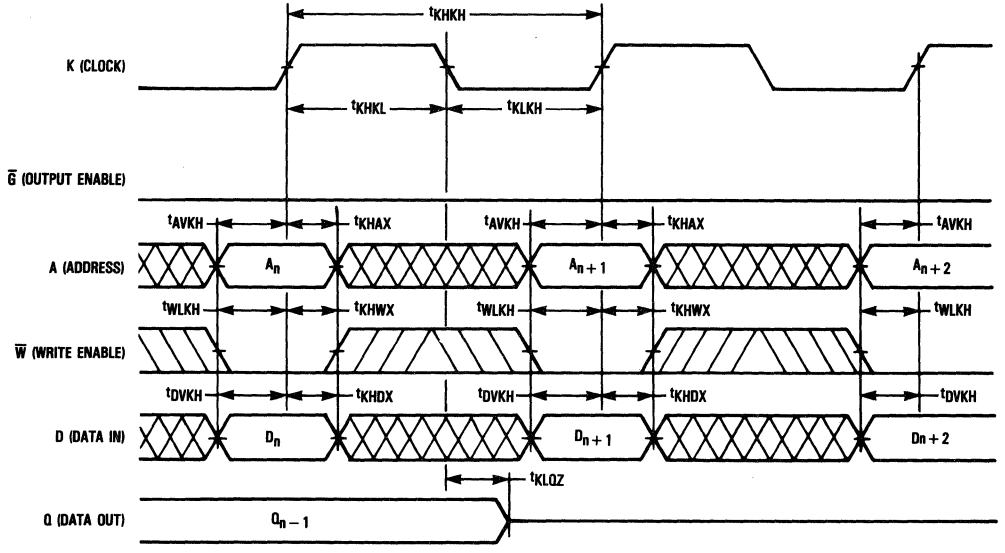


Figure 1B

READ CYCLE



WRITE CYCLE



ORDERING INFORMATION
(Order by Full Part Number)

MCM 62965 X XX

- MCM — Motorola Memory Prefix
- 62965 — Part Number
- X — Package (FN = PLCC)
- XX — Speed (25 = 25 ns, 30 = 30 ns, 35 = 35 ns)

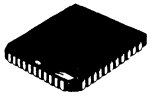
Full Part Numbers — MCM62965FN25 MCM62965FN30 MCM62965FN35

MCM62973

Product Preview

4K x 12 Bit Synchronous Static RAM

with Output Registers



FN PACKAGE
44-LEAD PLCC
CASE 777

The MCM62973 is a 49,152 bit synchronous static random access memory organized as 4096 words of 12 bits, fabricated using Motorola's second-generation high-performance silicon-gate CMOS (HCMOS III) technology. The device integrates input registers, high speed SRAM, and high-drive capability output registers onto a single monolithic circuit for reduced parts count implementation of cache data RAM, writeable control store applications, and other applications that utilize long words.

Synchronous design allows precise cycle control with the use of an external clock (K), while CMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

The address (A0-A11), data (D0-D11), write ($\overline{W}$), and chip enable ($\overline{E}$) inputs are all clock (K) controlled, positive-edge-triggered, noninverting registers.

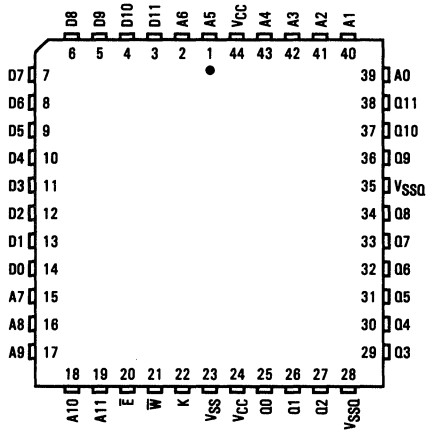
The chip enable ($\overline{E}$) input is a synchronous input clock that places the device in a low power mode when high at the rising edge of the clock (K).

The MCM62973 provides output register operation. At the rising edge of clock (K), the RAM data from the previous clock (K) high cycle is presented.

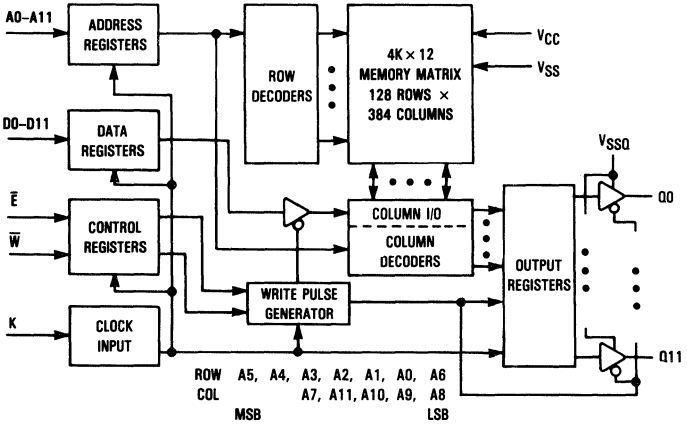
Write operations are internally self-timed and initiated by the rising edge of the clock (K) input. This feature eliminates complex off-chip write pulse generation and provides increased flexibility for incoming signals.

- Single 5 V ±10% Power Supply
- Fast Cycle Times: 18/20/25/30 ns Max
- Fast Clock (K) Access Times: 10/10/10/13 ns Max
- Address, Data Input, $\overline{E}$, and $\overline{W}$ Registers On-Chip
- Output Registers for Fully Pipelined Applications
- High Output Drive Capability
- Internally Self-Timed Write Pulse Generation
- Separate Data Input and Data Output Pins

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES	
A0-A11	Address Inputs
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
D0-D11	Data Inputs
Q0-Q11	Data Outputs
K	Clock Input
V_{CC}	+5 V Power Supply
V_{SS}	Ground
V_{SSQ}	Output Buffer Ground

For proper operation of the device V_{SS} and both V_{SSQ} leads must be connected to ground.

TRUTH TABLE

$\overline{E}$	$\overline{W}$	Operation	Q0-Q11	Current
L	L	Write	High Z	I_{CC}
L	H	Read	D_{out}	I_{CC}
H	X	Not Selected	High Z	I_{SB}

NOTE: The values of $\overline{E}$ and $\overline{W}$ are valid inputs for the setup and hold times relative to the K rising edge.

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to $V_{SS}=V_{SSQ}=0$ V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS}/V_{SSQ} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC}+0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation ($T_A=25°C$)	P_D	1.5	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for **ALL** rising edges of the clock (K) while the device is selected.

This device contains circuitry that will ensure the output devices are in High Z at power up. Care should be taken by the user to ensure that all clocks are at V_{IL} or V_{IH} during power up to prevent spurious read cycles from occurring.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{CC}=5.0$ V ±10%, $T_A=0$ to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to $V_{SS}=V_{SSQ}=0$ V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	–	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	−0.5*	–	0.8	V

*V_{IL} (min) = −3.0 V ac (pulse width ≤20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, $V_{in}=0$ to V_{CC})	$I_{lkg(I)}$	–	±1.0	μA
Output Leakage Current ($\overline{E}=V_{IH}$, $V_{out}=0$ to V_{CC}, Outputs must be in High Z)	$I_{lkg(O)}$	–	±1.0	μA
AC Supply Current ($\overline{E}=V_{IL}$, All Inputs = V_{IL} or V_{IH}, $I_{out}=0$ mA, Cycle Time ≥ t_{KHKH} min)	I_{CCA}			mA
MCM62973-18: $t_{KHKH}=18$ ns		–	180	
MCM62973-20: $t_{KHKH}=20$ ns		–	170	
MCM62973-25: $t_{KHKH}=25$ ns		–	170	
MCM62973-30: $t_{KHKH}=30$ ns		–	150	
Standby Current ($\overline{E}=V_{IH}$, $V_{IH}\geq3.0$ V, $V_{IL}\leq0.4$ V, $I_{out}=0$ mA, Cycle Time ≥ = t_{KHKH} min)	I_{SB}	–	30	mA
Output Low Voltage ($I_{OL}=12.7$ mA)	V_{OL}	–	0.4	V
Output High Voltage ($I_{OH}=-1.8$ mA)	V_{OH}	2.8	–	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, $T_A=25°C$, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	4	6	pF
Output Capacitance	C_{out}	5	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . .0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns

Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load. . . . . .See Figure 1A Unless Otherwise Noted

READ CYCLE (See Note 1)

Parameter	Symbol	MCM62973-18		MCM62973-20		MCM62973-25		MCM62973-30		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{KHKH}	18	–	20	–	25	–	30	–	ns	2
Clock Access Time	t_{KHQV}	–	10	–	10	–	10	–	13	ns	3
Output Active from Clock High	t_{KHQX}	3	–	3	–	3	–	3	–	ns	4
Clock High to Q High Z ($\overline{E}$ = V_{IH})	t_{KHQZ}	–	10	–	10	–	10	–	13	ns	4
Clock Low Pulse Width	t_{KLKH}	5	–	5	–	5	–	5	–	ns	
Clock High Pulse Width	t_{KHKL}	5	–	5	–	5	–	5	–	ns	
Setup Times for: $\overline{E}$	t_{EVKH}	5	–	5	–	5	–	5	–	ns	5
A	t_{AVKH}										
$\overline{W}$	t_{WHKH}										
Hold Times for: $\overline{E}$	t_{KHEX}	3	–	3	–	3	–	3	–	ns	5
A	t_{KHAX}										
$\overline{W}$	t_{KHWX}										

NOTES:
1. A read is defined by $\overline{W}$ high and $\overline{E}$ low for the setup and hold times.
2. All read cycle timing is referenced from K.
3. Valid data from K high will be the data stored at the address of the last valid read cycle.
4. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B. This parameter is sampled not 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQX} min for a given device.
5. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for **ALL** rising edges of clock (K) while the device is selected.

9

AC TEST LOADS

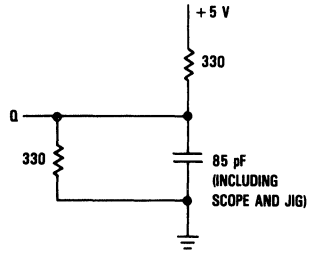


Figure 1A

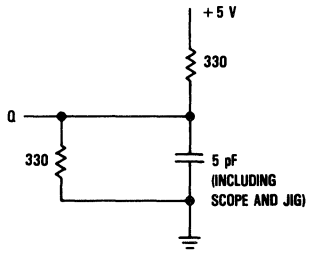
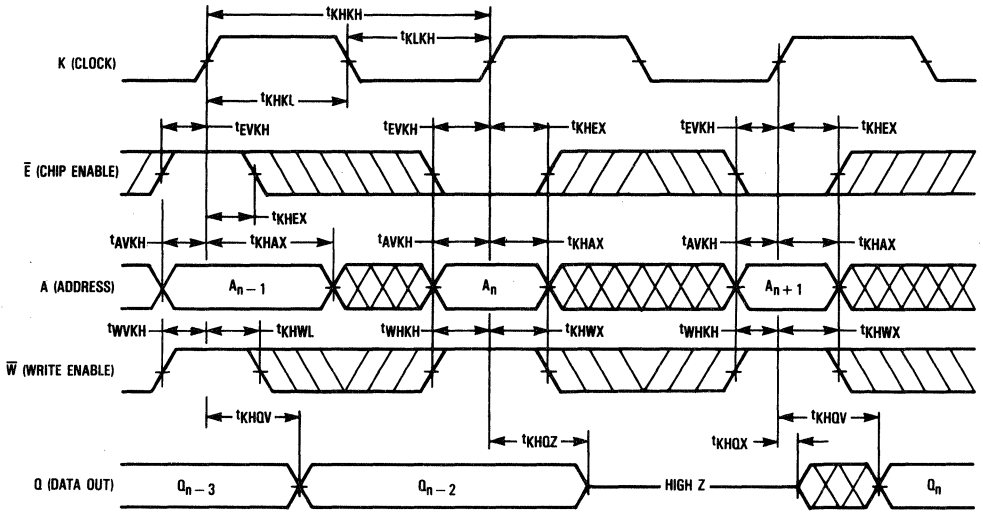
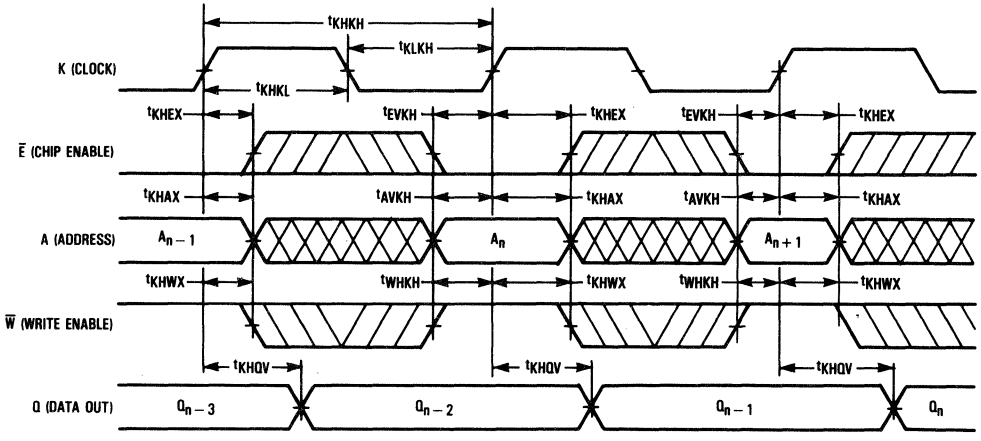


Figure 1B

READ CYCLE 1 (See Note 1)



READ CYCLE 2 (See Note 1)



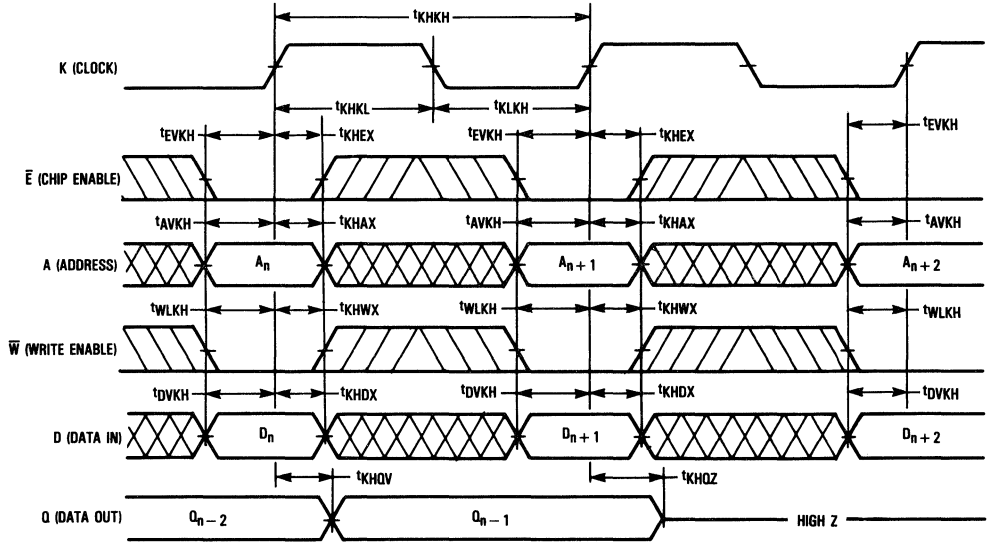
NOTE:
1. The outputs Q_{n-3} and Q_{n-2} are derived from two previous read cycles where $\overline{W} = V_{IH}$ and $\overline{E} = V_{IL}$ for those cycles.

WRITE CYCLE ($\overline{W}$ Controlled, See Note 1)

Parameter		Symbol	MCM62973-18		MCM62973-20		MCM62973-25		MCM62973-30		Unit	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time		t_{KHKH}	18	—	20	—	25	—	30	—	ns	2
Clock High to Output High Z ($\overline{W}=V_{IL}$)		t_{KHQZ}	—	10	—	10	—	10	—	13	ns	3
Setup Times for:	$\overline{E}$	t_{EVKH}	5	—	5	—	5	—	5	—	ns	4
	A	t_{AVKH}										
	$\overline{W}$	t_{WLKH}										
	D	t_{DVKH}										
Hold Times for:	$\overline{E}$	t_{KHEX}	3	—	3	—	3	—	3	—	ns	4
	A	t_{KHAX}										
	$\overline{W}$	t_{KHWX}										
	D	t_{KHDX}										

NOTES:
1. A write is performed when $\overline{W}$ and $\overline{E}$ are both low for the specified setup and hold times.
2. All write cycle timing is referenced from K.
3. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B. This parameter is sampled not 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQX} min for a given device.
4. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for **ALL** rising edges of clock (K) while the device is selected.

WRITE CYCLE



ORDERING INFORMATION
(Order by Full Part Number)

MCM 62973 X XX

- MCM — Motorola Memory Prefix
- 62973 — Part Number
- X — Package (FN = PLCC)
- XX — Speed (18 = 18 ns, 20 = 20 ns, 25 = 25 ns, 30 = 30 ns)

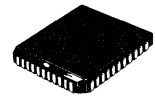
Full Part Numbers — MCM62973FN18 MCM62973FN20 MCM62973FN25 MCM62973FN30

MCM62974

Product Preview

4K x 12 Bit Synchronous Static RAM

with Output Registers and Output Enable



FN PACKAGE
44-LEAD PLCC
CASE 777

The MCM62974 is a 49,152 bit synchronous static random access memory organized as 4096 words of 12 bits, fabricated using Motorola's second-generation high-performance silicon-gate CMOS (HCMOS III) technology. The device integrates input registers, high speed SRAM, and high-drive capability output registers onto a single monolithic circuit for reduced parts count implementation of cache data RAM, writeable control store applications, and other applications that utilize long words.

Synchronous design allows precise cycle control with the use of an external clock (K), while CMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

The address (A0–A11), data (D0–D11), and write ($\overline{W}$) inputs are all clock (K) controlled, positive-edge-triggered, noninverting registers.

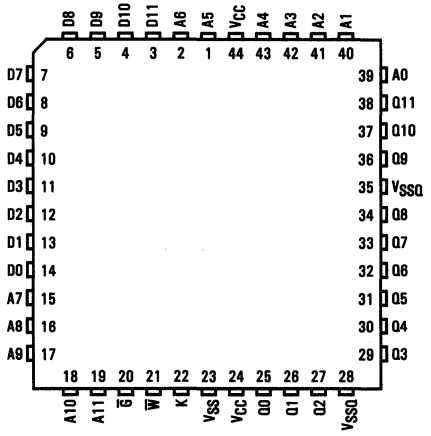
The MCM62974 provides output register operation. At the rising edge of clock (K), the RAM data from the previous clock (K) high cycle is presented.

The output enable ($\overline{G}$) provides asynchronous bus control for common I/O or bank switch applications.

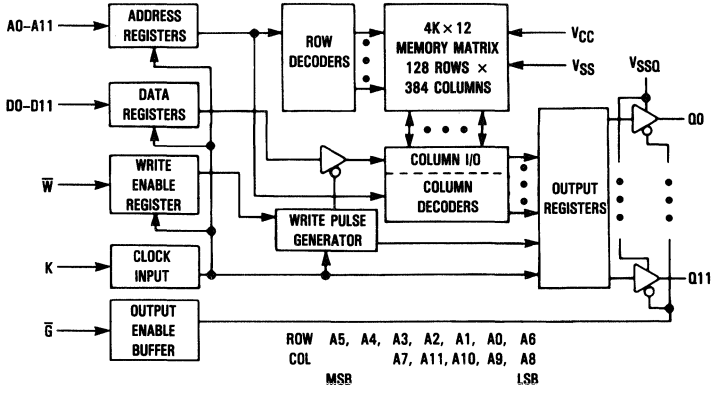
Write operations are internally self-timed and initiated by the rising edge of the clock (K) input. This feature eliminates complex off-chip write pulse generation and provides increased flexibility for incoming signals.

- Single 5 V ±10% Power Supply
- Fast Cycle Times: 18/20/25/30 ns Max
- Fast Clock (K) Access Times: 10/10/10/13 ns Max
- Address, Data Input, and $\overline{W}$ Registers On-Chip
- Output Enable for Asynchronous Bus Control
- Output Registers for Fully Pipelined Applications
- High Output Drive Capability
- Internally Self-Timed Write Pulse Generation
- Separate Data Input and Data Output Pins

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES	
A0-A11	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
D0-D11	Data Inputs
Q0-Q11	Data Outputs
K	Clock Input
V_{CC}	+5 V Power Supply
V_{SS}	Ground
V_{SSQ}	Output Buffer Ground

For proper operation of the device V_{SS} and both V_{SSQ} leads must be connected to ground.

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

TRUTH TABLE

$\overline{W}$	Operation	Q0-Q9	Current
L	Write	High Z	I_{CCA}
H	Read	D_{out}	I_{CCA}

NOTE: The value $\overline{W}$ is a valid input for the setup and hold times relative to the K rising edge.

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to $V_{SS}=V_{SSQ}=0$ V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS}/V_{SSQ} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC}+0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation (T_A=25°C)	P_D	1.5	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for **ALL** rising edges of clock (K) while the device is selected.

This device contains circuitry that will ensure the output devices are in High Z at power up. Care should be taken by the user to ensure that all clocks are at V_{IL} or V_{IH} during power up to prevent spurious read cycles from occurring.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC}=5.0 V ±10%, T_A=0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to $V_{SS}=V_{SSQ}=0$ V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

*V_{IL} (min) = −3.0 V ac (pulse width ≤20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in}=0 to V_{CC})	$I_{lkg(I)}$	—	±1.0	μA
Output Leakage Current ($\overline{G}=V_{IH}$, V_{out}=0 to V_{CC}, Outputs must be high-Z)	$I_{lkg(O)}$	—	±1.0	μA
AC Supply Current ($\overline{G}=V_{IL}$, All Inputs=V_{IL} or V_{IH}, I_{out}=0 mA, Cycle Time≥t_{KHKH} min)	I_{CCA}			mA
MCM62974-18: t_{KHKH}=18 ns		—	180	
MCM62974-20: t_{KHKH}=20 ns		—	170	
MCM62974-25: t_{KHKH}=25 ns		—	170	
MCM62974-30: t_{KHKH}=30 ns		—	150	
Output Low Voltage (I_{OL}=12.7 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH}=−1.8 mA)	V_{OH}	2.8	—	V

CAPACITANCE (f=1.0 MHz, dV=3.0 V, T_A=25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	4	6	pF
Output Capacitance	C_{out}	5	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . .0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns

Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load . . . . . .See Figure 1A Unless Otherwise Noted

READ/WRITE CYCLE

Parameter	Symbol	MCM62974-18		MCM62974-20		MCM62974-25		MCM62974-30		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{KHKH}	18	–	20	–	25	–	30	–	ns	1, 3
Write Cycle Time	t_{KHKH}	18	–	20	–	25	–	30	–	ns	2, 3
Clock High Access Time	t_{KHQV}	–	10	–	10	–	10	–	13	ns	3, 4
$\overline{G}$ Low to Output Valid	t_{GLQV}	–	10	–	10	–	10	–	13	ns	3
Output Active from Clock High	t_{KHQX}	0	–	0	–	0	–	0	–	ns	
Output Active from $\overline{G}$ Low	t_{GLQX}	0	–	0	–	0	–	0	–	ns	
Clock Low Pulse Width	t_{KLKH}	5	–	5	–	5	–	5	–	ns	
Clock High Pulse Width	t_{KHKL}	5	–	5	–	5	–	5	–	ns	
Setup Times for: A D $\overline{W}$	t_{AVKH} t_{DVKH} t_{WVKH}	5	–	5	–	5	–	5	–	ns	1, 2, 5
Hold Times for: A D $\overline{W}$	t_{KHAX} t_{KHDX} t_{KHWX}	3	–	3	–	3	–	3	–	ns	1, 2, 5
Clock High to Output High Z ($\overline{W}$ = V_{IL})	t_{KHQZ}	0	10	0	10	0	10	0	13	ns	3, 6
$\overline{G}$ High to Output High Z	t_{GHQZ}	0	10	0	10	0	10	0	13	ns	3, 6, 7

NOTES:
1. A read is defined by $\overline{W}$ high for the specified setup and hold times.
2. A write is defined by $\overline{W}$ low for the specified setup and hold times.
3. All read and write cycle timing is referenced from K or from $\overline{G}$.
4. Valid data from K high will be the data stored at the address of the last valid read cycle.
5. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for **ALL** rising edges of clock (K) while the device is selected.
6. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQX} min and t_{GHQZ} max is less than t_{GLQX} min for a given device.
7. $\overline{G}$ becomes a don't care signal for successive writes after the first write cycle.

9

AC TEST LOADS

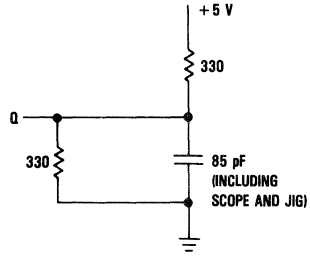


Figure 1A

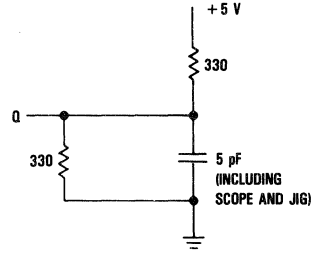
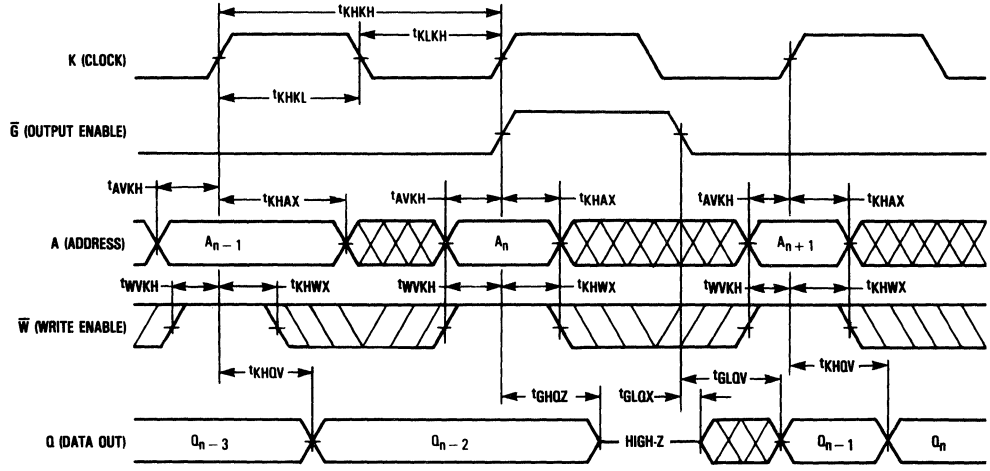
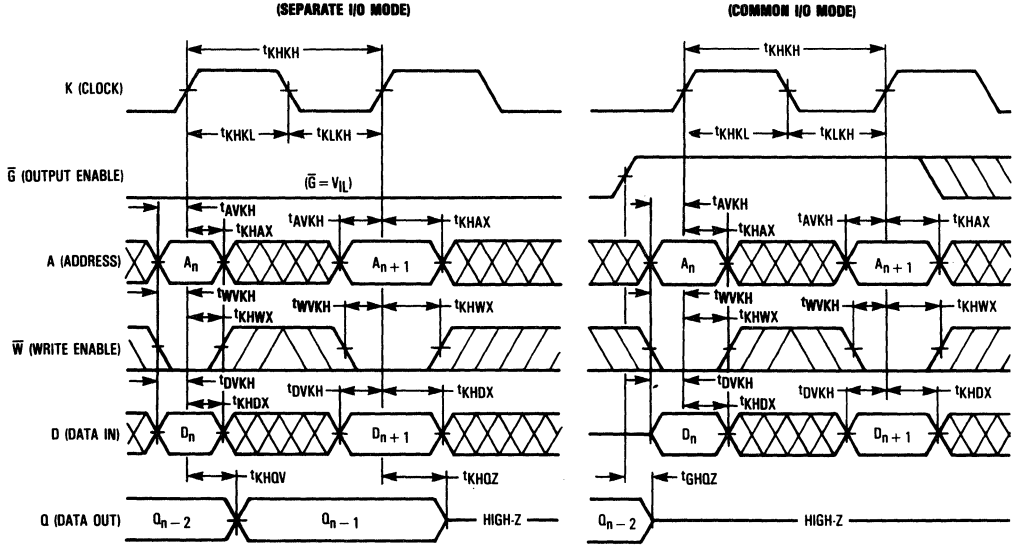


Figure 1B

READ CYCLE



WRITE CYCLE



ORDERING INFORMATION
(Order by Full Part Number)

MCM 62974 X XX

- MCM — Motorola Memory Prefix
- 62974 — Part Number
- X — Package (FN = PLCC)
- XX — Speed (18 = 18 ns, 20 = 20 ns, 25 = 25 ns, 30 = 30 ns)

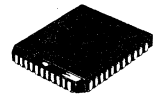
Full Part Numbers — MCM62974FN18 MCM62974FN20 MCM62974FN25 MCM62974FN30

MCM62975

Product Preview

4K x 12 Bit Synchronous Static RAM

with Transparent Outputs and Output Enable



FN PACKAGE
44-LEAD PLCC
CASE 777

The MCM62975 is a 49,152 bit synchronous static random access memory organized as 4096 words of 12 bits, fabricated using Motorola's second-generation high-performance silicon-gate CMOS (HCMOS III) technology. The device integrates input registers, high speed SRAM, and high-drive capability output latching onto a single monolithic circuit for reduced parts count implementation of cache data RAM, writeable control store applications, and other applications that utilize long words.

Synchronous design allows precise cycle control with the use of an external clock (K), while CMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

The address (A0–A11), data (D0–D11), and write ($\overline{W}$) inputs are all clock (K) controlled, positive-edge-triggered, noninverting registers.

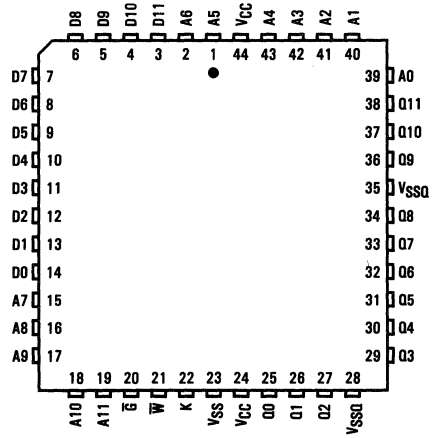
The MCM62975 provides transparent output operation when clock (K) is low for access of RAM data within the same cycle (output data is latched when clock (K) is high).

The output enable ($\overline{G}$) provides asynchronous bus control for common I/O or bank switch applications.

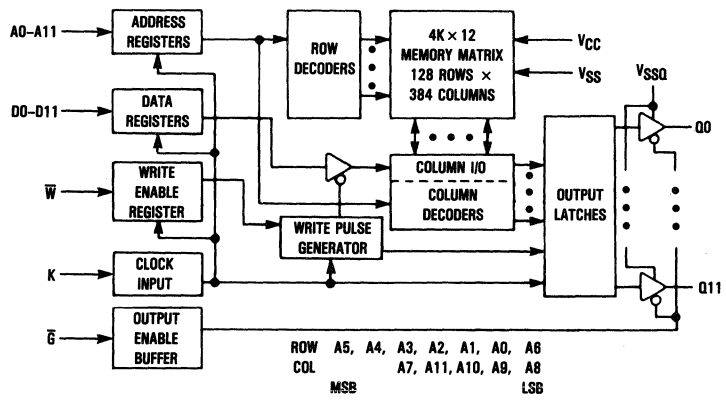
Write operations are internally self-timed and initiated by the rising edge of the clock (K) input. This feature eliminates complex off-chip write pulse generation and provides increased flexibility for incoming signals.

- Single 5 V ±10% Power Supply
- Fast Cycle Times: 25/30/35 ns Max
- Fast Clock (K) Access Times: 10/13/15 ns Max
- Address, Data Input, and $\overline{W}$ Registers On-Chip
- Transparent Output Latch for Access Within the Same Cycle
- Output Enable for Asynchronous Bus Control
- High Output Drive Capability
- Internally Self-Timed Write Pulse Generation
- Separate Data Input and Data Output Pins

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES	
A0-A11	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
D0-D11	Data Inputs
Q0-Q11	Data Outputs
K	Clock Input
V_{CC}	+5 V Power Supply
V_{SS}	Ground
V_{SSQ}	Output Buffer Ground

For proper operation of the device V_{SS} and both V_{SSQ} leads must be connected to ground.

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

TRUTH TABLE

$\overline{W}$	Operation	Q0-Q11	Current
L	Write	High Z	I_{CCA}
H	Read	D_{out}	I_{CCA}

NOTE: The value $\overline{W}$ is a valid input for the setup and hold times relative to the K rising edge.

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to $V_{SS} = V_{SSQ} = 0$ V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS}/V_{SSQ} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC} +0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation (T_A = 25°C)	P_D	1.5	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for **ALL** rising edges of clock (K) while the device is selected.

This device contains circuitry that will ensure the output devices are in High Z at power up. Care should be taken by the user to ensure that all clocks are at V_{IL} or V_{IH} during power up to prevent spurious read cycles from occurring.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to $V_{SS} = V_{SSQ} = 0$ V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	–	V_{CC} +0.3	V
Input Low Voltage	V_{IL}	−0.5*	–	0.8	V

*V_{IL} (min) = −3.0 V ac (pulse width ≤20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	–	±1.0	μA
Output Leakage Current ($\overline{G} = V_{IH}$, V_{out} = 0 to V_{CC}, Outputs must be high-Z)	$I_{lkg(O)}$	–	±1.0	μA
AC Supply Current ($\overline{G} = V_{IL}$, All Inputs = V_{IL} or V_{IH}, I_{out} = 0 mA, Cycle Time ≥ t_{KHKH} min)	I_{CCA}			mA
MCM62975-25: t_{KHKH} = 25 ns		–	170	
MCM62975-30: t_{KHKH} = 30 ns		–	170	
MCM62975-35: t_{KHKH} = 35 ns		–	150	
Output Low Voltage (I_{OL} = 12.7 mA)	V_{OL}	–	0.4	V
Output High Voltage (I_{OH} = −1.8 mA)	V_{OH}	2.8	–	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	4	6	pF
Output Capacitance	C_{out}	5	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . .0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns

Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load. . . . . .See Figure 1A Unless Otherwise Noted

READ/WRITE CYCLE

Parameter	Symbol	MCM62975-25		MCM62975-30		MCM62975-35		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{KHKH}	25	–	30	–	35	–	ns	1, 3
Write Cycle Time	t_{KHKH}	25	–	30	–	35	–	ns	2, 3
Clock High Access Time	t_{KHQV}	–	25	–	30	–	35	ns	3, 4, 5
Clock Low to Output Valid	t_{KLQV}	–	10	–	13	–	15	ns	3, 4, 5
$\overline{G}$ Low to Output Valid	t_{GLQV}	–	10	–	13	–	15	ns	3
Output Active from Clock Low	t_{KLQX}	0	–	0	–	0	–	ns	
Output Active from $\overline{G}$ Low	t_{GLQX}	0	–	0	–	0	–	ns	
Clock Low Pulse Width	t_{KLKH}	5	–	5	–	5	–	ns	
Clock High Pulse Width	t_{KHKL}	5	–	5	–	5	–	ns	
Setup Times for: A	t_{AVKH}	5	–	5	–	5	–	ns	1, 2, 6
D	t_{DVKH}								
$\overline{W}$	t_{WHKH}								
Hold Times for: A	t_{KHAX}	3	–	3	–	3	–	ns	1, 2, 6
D	t_{KHDX}								
$\overline{W}$	t_{KHWX}								
Clock Low to Output High Z ($\overline{W}$ = V_{IL})	t_{KLQZ}	0	10	0	13	0	15	ns	5, 7
$\overline{G}$ High to Output High Z	t_{GHQZ}	0	10	0	13	0	15	ns	3, 7, 8

NOTES:
1. A read is defined by $\overline{W}$ high for the specified setup and hold times.
2. A write is defined by $\overline{W}$ low for the specified setup and hold times.
3. All read and write cycle timing is referenced from K or from $\overline{G}$.
4. Access time is controlled by t_{KLQV} if the clock high pulse width ≥ ($t_{KHQV} - t_{KLQV}$); otherwise it is controlled by t_{KHQV}.
5. K must be low for the outputs to transition.
6. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for ALL rising edges of clock (K) while the device is selected.
7. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQX} min and t_{GHQZ} max is less than t_{GLQX} min for a given device.
8. $\overline{G}$ becomes a don't care signal for successive writes after the first write cycle.

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AC TEST LOADS

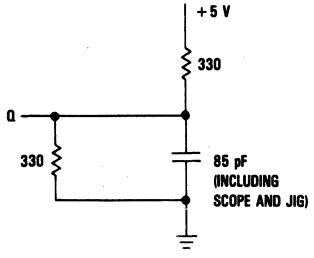


Figure 1A

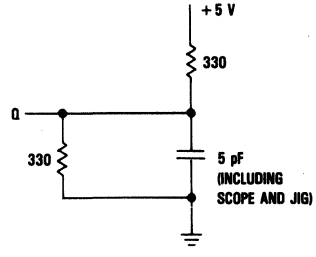
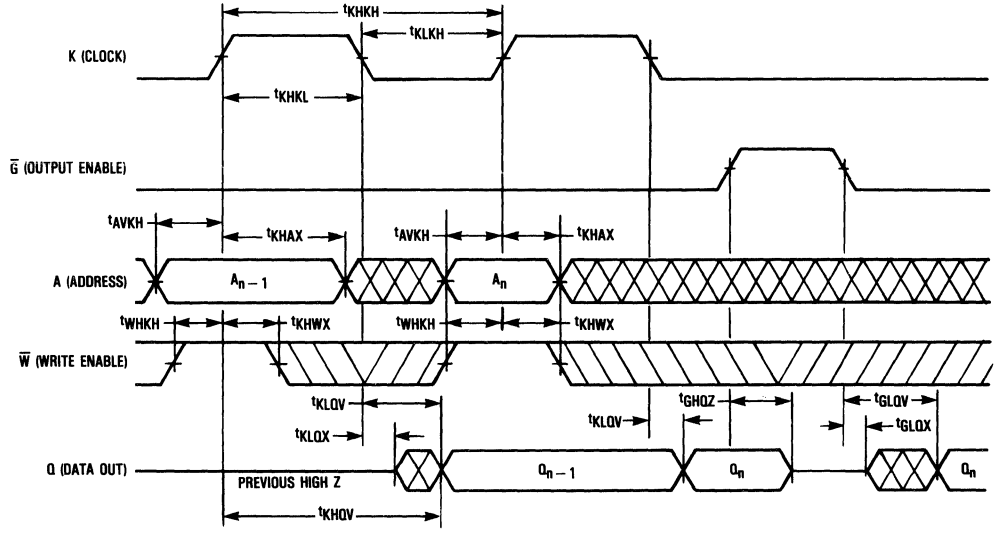
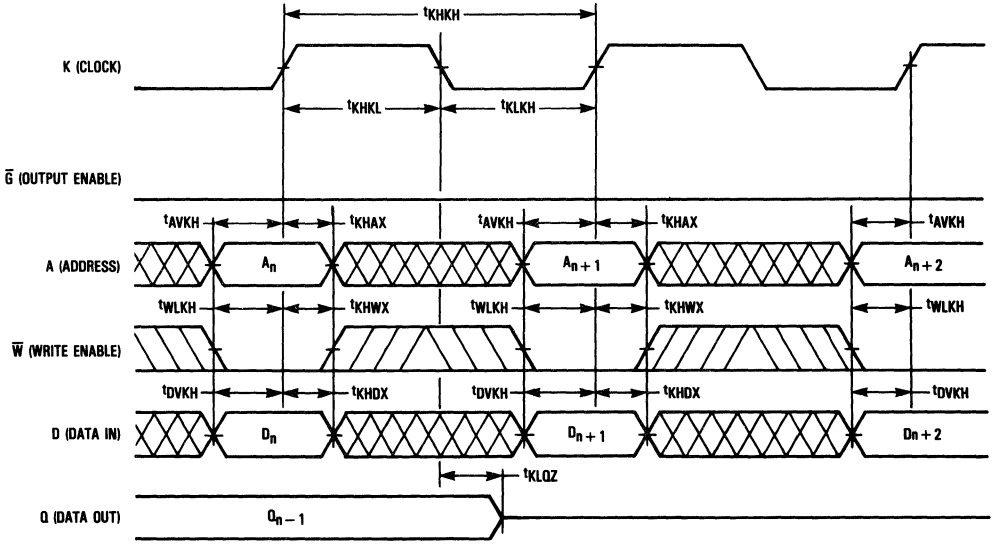


Figure 1B

READ CYCLE



WRITE CYCLE



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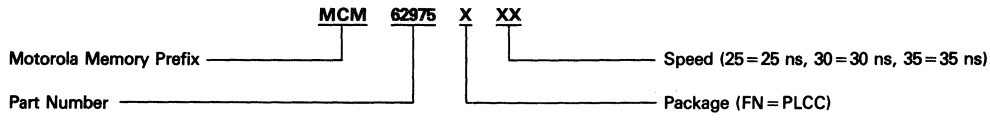
ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers—MCM62975FN25 MCM62975FN30 MCM62975FN35

9

MCM62980

Advance Information

64K × 4 Bit Fast Synchronous Static RAM

The MCM62980 is a 262,144 bit synchronous static random access memory organized as 65,536 words of 4 bits, fabricated using Motorola's high–performance silicon–gate CMOS technology. The device integrates a 64K x 4 SRAM core with advanced peripheral circuitry consisting of positive edge triggered registers on address and synchronous write enable inputs. Asynchronous controls consist of asynchronous write strobe and output enable ($\overline{G}$). This device has increased output drive capability supported by multiple power pins.

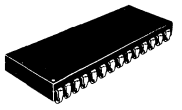
Write cycles are differentiated from read cycles by the state of the synchronous write enable pin ($\overline{SW}$) at the rising edge of clock (K). Write cycles are completed only if asynchronous write strobe ($\overline{AW}$) is asserted within the specified setup time of the following rising edge of clock (K). Write cycles may be aborted by negating the $\overline{AW}$ signal prior to the low transition of the clock.

Additional power supply pins have been utilized and placed on the package for maximum performance. In addition one set of power pins is electrically isolated from the other set and supplies power only to the output buffers. This allows connecting the output buffers to 3.3 V instead of 5.0 V if desired. If 3.3 V output levels are chosen, the output buffer impedance in the "high" state is approximately equal to the impedance in the "low" state which allows simple yet effective transmission line terminations to be achieved.

The MCM62980 will be available in a 28 pin 300 mil plastic SOJ.

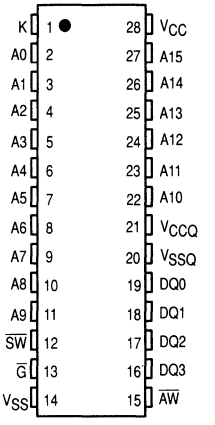
Applications for this device include cache data and tag RAMs. See Figure 2 for applications information.

- Single 5 V ±10% Power Supply
- Choice of 5.0 V or 3.3 V ±10% Power Supplies for Output Buffers
- Fast Access and Cycle Times: 15/20 ns Max
- Fully Synchronous Operation, Single Clock Control
- Clock Timed Writes with Asynchronous Late Write Abort
- Registered Address Inputs
- Common Data Inputs and Data Outputs
- Output Enable Controlled Three-State Outputs
- High Output Drive Capability: 85 pF/Output at Rated Access Time
- High Board Density 300 mil PSOJ Package



J PACKAGE
300 MIL SOJ
CASE 810B

PIN ASSIGNMENT



PIN NAMES	
A0–A15	Address Inputs
$\overline{AW}$	Asynchronous Write Strobe
$\overline{SW}$	Synchronous Write Enable
K	Clock
$\overline{G}$	Output Enable
DQ0–DQ3	Data Input/Output
V_{CC}	+5 V Power Supply
V_{CCQ}	Output Buffer Power Supply
V_{SSQ}	Output Buffer Ground
V_{SS}	Ground

All power supply and ground pins must be connected for proper operation of the device. $V_{CC} \geq V_{CCQ}$ at all times including power up.

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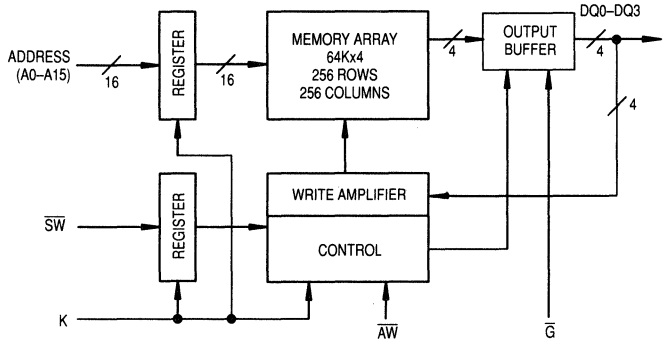
This document contains information on a new product. Specifications and information herein are subject to change without notice.

BLOCK DIAGRAM



TRUTH TABLE (See Note)

$\overline{SW}$	$\overline{AW}$	$\overline{G}$	Mode	Supply Current	I/O Status
H	X	L	Read Cycle	I_{CC}	Data Out
H	X	H	Read Cycle	I_{CC}	High-Z
L	L	X	Write Cycle	I_{CC}	High-Z
L	H	X	Aborted Write Cycle	I_{CC}	High-Z

NOTE: $\overline{SW}$ and $\overline{AW}$ satisfy the specified setup and hold times for the rising edge of clock (K).

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to $V_{SS} = V_{SSQ} = 0$ V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	–0.5 to 7.0	V
Voltage Relative to V_{SS}/V_{SSQ} for Any Pin Except V_{CC} and V_{CCQ}	V_{in}, V_{out}	–0.5 to V_{CC} +0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation (T_A = 25°C)	P_D	1.0	W
Temperature Under Bias	T_{bias}	–10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	–55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electrical fields; however, it is advised that normal precautions to taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High Z at power up.

AC TEST LOADS

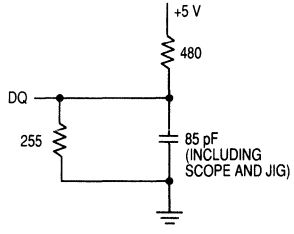


Figure 1A

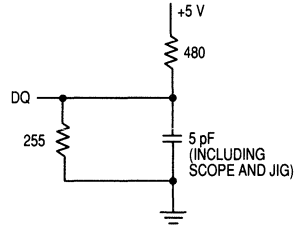


Figure 1B

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, V_{CCQ} = 5.0 V or 3.3 V ± 10%, T_A = 0 to +70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = V_{SSQ} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Output Buffer Supply Voltage (5.0 V TTL Compatible) (3.3 V 50 Ω Compatible)	V_{CCQ}*	 4.5 3.0	 5.0 3.3	 5.5 3.6	V
Input High Voltage	V_{IH}	2.2	3.0	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	–0.5**	0.0	0.8	V

*V_{CCQ} must be ≤ V_{CC} at all times, including power up.
**V_{IL} (min) = –3.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	—	± 1.0	µA
Output Leakage Current ($\overline{G}$ = V_{IH})	$I_{lkg(O)}$	—	—	± 1.0	µA
AC Supply Current ($\overline{G}$ = V_{IH}, All Inputs = V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, I_{out} = 0 mA, Cycle Times ≥ t_{KHKH} min)	I_{CCA}	—	130	170	mA
Output Low Voltage (I_{OL} = +8.0 mA)	V_{OL}	—	—	0.4	V
Output High Voltage (I_{OH} = –4.0 mA)	V_{OH}	2.4	—	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (All Pins Except DQ0–DQ3)	C_{in}	4	6	pF
Input/Output Capacitance (DQ0–DQ3)	$C_{I/O}$	8	10	pF

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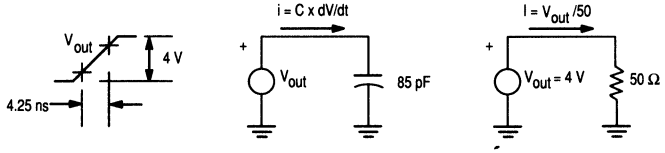
CAPACITIVE LOAD EQUIVALENT RESISTANCE



$$i = C \times \left(\frac{dV_{out}}{dt}\right) = 85 \times 10^{-12} \times \left(\frac{4\ V}{4.25 \times 10^{-9}}\right) = 80\ mA$$

$$i = \frac{V}{R} = \frac{4}{50} = 80\ mA$$

85 pF load is equivalent to a 50 Ω termination

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, V_{CCQ} = 5.0 V or 3.3 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

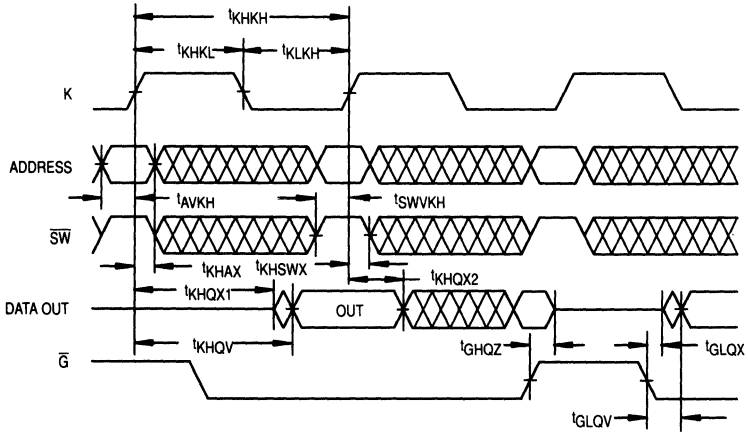
Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

READ AND WRITE CYCLE TIMING (See Note 1)

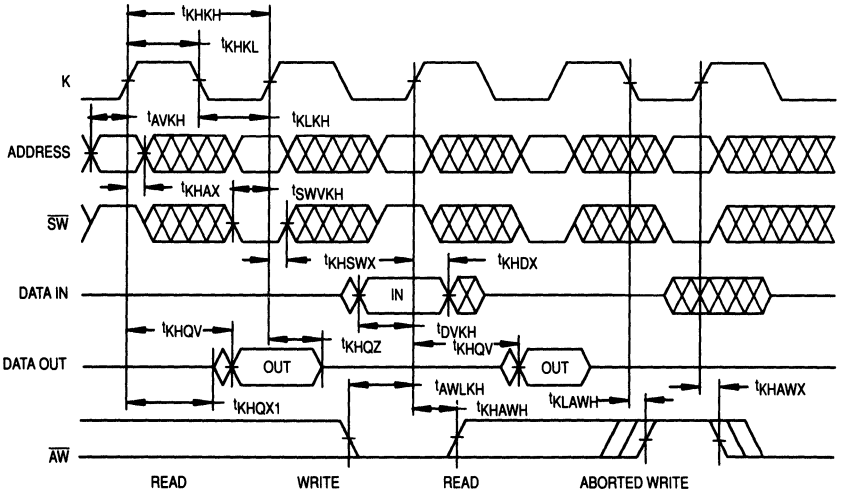
Parameter	Symbol	MCM62980–15		MCM62980–20		Unit	Notes
		Min	Max	Min	Max		
Cycle Times:						ns	
Clock High to Clock High	t_{KHKH}	15	—	20	—		
Access Times:						ns	
Clock High to Output Valid	t_{KHQV}	—	15	—	20		2
Output Enable Low Output Valid	t_{GLQV}	—	6	—	8		2
Aborted Write Cycles:						ns	
Clock Low to Asynchronous Write Strobe High	t_{KLAWH}	—	0	—	0		
Clock High to Asynchronous Write Strobe Invalid	t_{KHAWX}	2	—	2	—		
Output Buffer Control:						ns	
Output Enable High to Output High-Z	t_{GHQZ}	2	6	2	8		3
Output Enable Low to Output Low-Z	t_{GLQX}	2	—	2	—		3
Reads:							
Clock High to Output Low-Z after Write	t_{KHQX1}	8	—	8	—		3
Clock High to Output Invalid	t_{KHQX2}	5	—	5	—		
Writes:							
Clock High to Output High-Z after Read	t_{KHQZ}	3	10	3	10		3
Clock:						ns	
Clock High Time	t_{KHKL}	4	—	4	—		
Clock Low Time	t_{KLKH}	8	—	10	—		
Setup Times:						ns	
Address Valid to Clock High	t_{AVKH}	2	—	2	—		
Synchronous Write Enable Valid to Clock High	t_{SWVKH}	2	—	2	—		
Writes:							
Data In Valid to Clock High	t_{DVKH}	6	—	6	—		
Asynchronous Write Strobe Low to Clock High	t_{AWLKH}	6	—	6	—		
Hold Times:						ns	
Clock High to Address Invalid	t_{KHAX}	2	—	2	—		
Clock High to Synchronous Write Enable Invalid	t_{KHSWX}	2	—	2	—		
Writes:							
Clock High to Data In Invalid	t_{KHDX}	0	—	0	—		
Clock High to Asynchronous Write Strobe High	t_{KHAWH}	2	—	2	—		

NOTES:
1. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for **ALL** rising edges of clock (K).
2. Into rated load of 85 pF equivalent resistive load (see Figure 1).
3. Transition is measured ± 500 mV from steady-state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{KHQZ} is less than t_{KHQX1} and t_{GHQZ} is less than t_{GLQX} for a given device.

READ CYCLES



READ — WRITE — READ CYCLES



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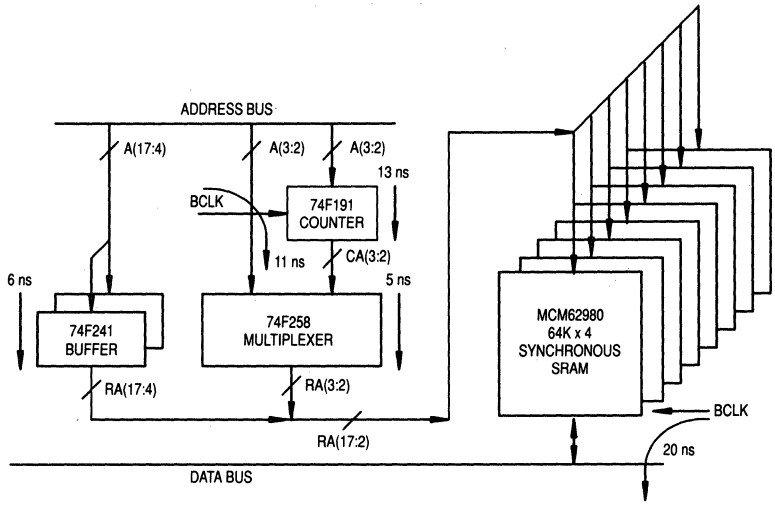

Figure 2. Burstable 64K x 32 Memory Array

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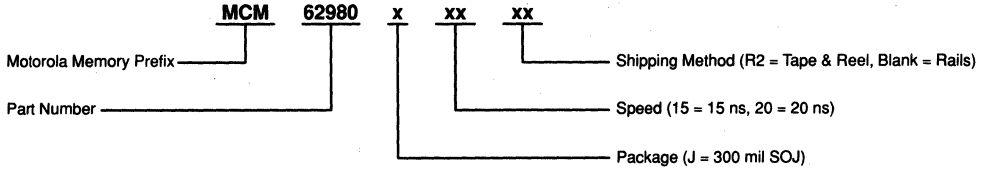
ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers – MCM62980J15 MCM62980J15R2
MCM62980J20 MCM62980J20R2

MCM62981

Advance Information

64K × 4 Bit Fast Synchronous ParityRam™

The MCM62981 is a 262,144 bit synchronous static random access memory organized as 65,536 words of 4 bits, fabricated using Motorola's high-performance silicon-gate CMOS technology. The device integrates a 64K x 4 SRAM core with advanced peripheral circuitry consisting of positive edge triggered registers on address and synchronous write enable inputs. Asynchronous controls include asynchronous write strobes and output enable ($\overline{G}$). This device has increased output drive capability supported by multiple power pins. Four asynchronous write strobes ($\overline{AW0}$–$\overline{AW3}$) are provided to allow each bit position to be written individually, thereby simplifying the task of supporting byte parity. This x4 organized SRAM is ideally suited for parity on 32 bit words.The device is functionally similar to the MCM62980 and MCM62990 with the only difference being the individual bit write capablilty.

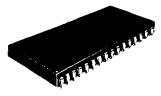
Write cycles are differentiated from read cycles by the state of the synchronous write enable pin ($\overline{SW}$) at the rising edge of clock (K). Write cycles are completed only if the appropriate asynchronous write strobe ($\overline{AWx}$) is asserted within the specified setup time of the following rising edge of clock (K). Write cycles may be aborted by ensuring each $\overline{AWx}$ is negated by the time the clock transitions to the low state.

Additional power supply pins have been utilized and placed on the package for maximum performance. In addition one set of power pins is electrically isolated from the other set and supplies power only to the output buffers. This allows connecting the output buffers to 3.3 V instead of 5.0 V if desired. If 3.3 V output levels are chosen, the output buffer impedance in the "high" state is approximately equal to the impedance in the "low" state which allows simple yet effective transmission line terminations to be achieved.

The MCM62981 will be available in a 32 pin 300 mil plastic SOJ.

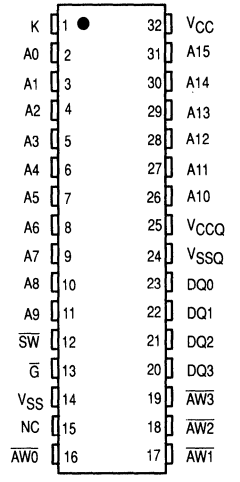
Applications for this device include parity RAMs for fast data caches.

- Single 5 V ±10% Power Supply
- Choice of 5.0 V or 3.3 V ±10% Power Supplies for Output Buffers
- Fast Access and Cycle Times: 15/20 ns Max
- Fully Synchronous Operation, Single Clock Control
- Clock Timed Writes with Asynchronous Late Write Abort
- Each Bit Position Individually Writeable for Simple Parity Support
- Registered Address Inputs
- Common Data Inputs and Data Outputs
- Output Enable Controlled Three-State Outputs
- High Output Drive Capability: 85 pF/Output at Rated Access Time



J PACKAGE
300 MIL SOJ
CASE 857

PIN ASSIGNMENT



PIN NAMES

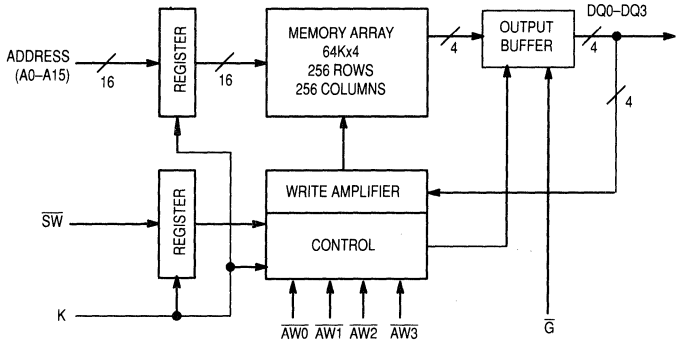
A0–A15	Address Inputs
$\overline{AW0}$–$\overline{AW3}$	Asynchronous Write Strobes
$\overline{SW}$	Synchronous Write Enable
K	Clock
$\overline{G}$	Output Enable
DQ0–DQ3	Data Input/Output
V_{CC}	+5 V Power Supply
V_{CCQ}	Output Buffer Power Supply
V_{SSQ}	Output Buffer Ground
V_{SS}	Ground
NC	No Connect

All power supply and ground pins must be connected for proper operation of the device. $V_{CC} \geq V_{CCQ}$ at all times including power up.

ParityRAM is a trademark of Motorola Inc.

This document contains information on a new porduct. Specifications and information herein are subject to change without notice.

BLOCK DIAGRAM



TRUTH TABLE (See Note)

$\overline{SW}$	$\overline{AWx}$	$\overline{G}$	Mode	Supply Current	I/O Status
H	X	L	Read Cycle	I_{CC}	Data Out
H	X	H	Read Cycle	I_{CC}	High-Z
L	L	X	Write Cycle	I_{CC}	High-Z
L	H	X	Aborted Write Cycle	I_{CC}	High-Z

NOTE: $\overline{SW}$ and $\overline{AWx}$ satisfy the specified setup and hold times for the rising edge of clock (K).

This device contains circuitry to protect the inputs against damage due to high static voltages or electrical fields; however, it is advised that normal precautions to taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High Z at power up.

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to V_{SS} = V_{SSQ} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	–0.5 to 7.0	V
Voltage Relative to V_{SS}/V_{SSQ} for Any Pin Except V_{CC} and V_{CCQ}	V_{in}, V_{out}	–0.5 to V_{CC} +0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation (T_A = 25°C)	P_D	1.0	W
Temperature Under Bias	T_{bias}	–10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	–55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

AC TEST LOADS

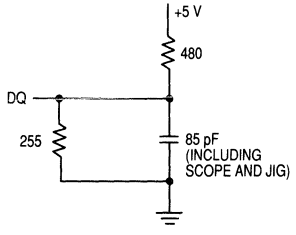


Figure 1A

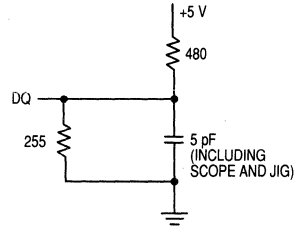


Figure 1B

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, V_{CCQ} = 5.0 V or 3.3 V ± 10%, T_A = 0 to +70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = V_{SSQ} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Output Buffer Supply Voltage (5.0 V TTL Compatible) (3.3 V 50 Ω Compatible)	V_{CCQ}	 4.5 3.0	 5.0 3.3	 5.5 3.6	V
Input High Voltage	V_{IH}	2.2	3.0	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	–0.5*	0.0	0.8	V

*V_{IL} (min) = –3.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

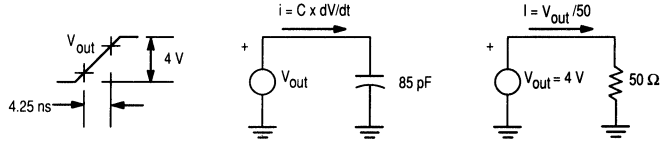
Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	—	± 1.0	µA
Output Leakage Current ($\overline{G}$ = V_{IH})	$I_{lkg(O)}$	—	—	± 1.0	µA
AC Supply Current ($\overline{G}$ = V_{IH}, All Inputs = V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, I_{out} = 0 mA, Cycle Times ≥ t_{KHKH} min)	I_{CCA}	—	130	170	mA
Output Low Voltage (I_{OL} = +8.0 mA)	V_{OL}	—	—	0.4	V
Output High Voltage (I_{OH} = –4.0 mA)	V_{OH}	2.4	—	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (All Pins Except DQ0–DQ3)	C_{in}	4	6	pF
Input/Output Capacitance (DQ0–DQ3)	$C_{I/O}$	8	10	pF

9

CAPACITIVE LOAD EQUIVALENT RESISTANCE



$i = C \times \left(\frac{dV_{out}}{dt}\right) = 85 \times 10^{-12} \times \left(\frac{4\ V}{4.25 \times 10^{-9}}\right) = 80\ mA$

$i = \frac{V}{R} = \frac{4}{50} = 80\ mA$

85 pF load is equivalent to a 50 Ω termination

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, V_{CCQ} = 5.0 V or 3.3 V ± 10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

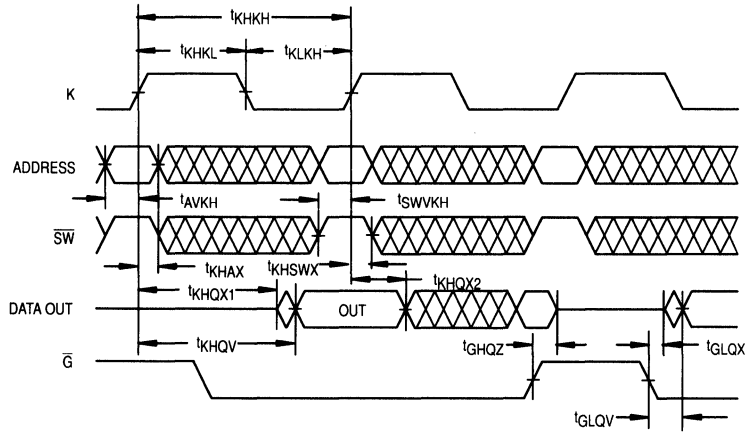
READ AND WRITE CYCLE TIMING (See Note 1)

Parameter	Symbol	MCM62981–15		MCM62981–20		Unit	Notes
		Min	Max	Min	Max		
Cycle Times:						ns	
Clock High to Clock High	t_{KHKH}	15	—	20	—		
Access Times:						ns	
Clock High to Output Valid	t_{KHQV}	—	15	—	20		2
Output Enable Low Output Valid	t_{GLQV}	—	6	—	8		2
Aborted Write Cycles:						ns	
Clock Low to Asynchronous Write Strobe High	t_{KLAWxH}	—	0	—	0		
Clock High to Asynchronous Write Strobe Invalid	t_{KHAWxX}	2	—	2	—		
Output Buffer Control:						ns	
Output Enable High to Output High-Z	t_{GHQZ}	2	6	2	8		3
Output Enable Low to Output Low-Z	t_{GLQX}	2	—	2	—		3
Reads:							
Clock High to Output Low-Z after Write	t_{KHQX1}	8	—	8	—		3
Clock High to Output Invalid	t_{KHQX2}	5	—	5	—		
Writes:							
Clock High to Output High-Z after Read	t_{KHQZ}	3	10	3	10		3
Clock:						ns	
Clock High Time	t_{KHKL}	4	—	4	—		
Clock Low Time	t_{KLKH}	8	—	10	—		
Setup Times:						ns	
Address Valid to Clock High	t_{AVKH}	2	—	2	—		
Synchronous Write Enable Valid to Clock High	t_{SWVKH}	2	—	2	—		
Writes:							
Data In Valid to Clock High	t_{DVKH}	6	—	6	—		
Asynchronous Write Strobe Low to Clock High	t_{AWxLKH}	6	—	6	—		
Hold Times:						ns	
Clock High to Address Invalid	t_{KHAX}	2	—	2	—		
Clock High to Synchronous Write Enable Invalid	t_{KHSWX}	2	—	2	—		
Writes:							
Clock High to Data In Invalid	t_{KHDX}	0	—	0	—		
Clock High to Asynchronous Write Strobe High	t_{KHAWxH}	2	—	2	—		

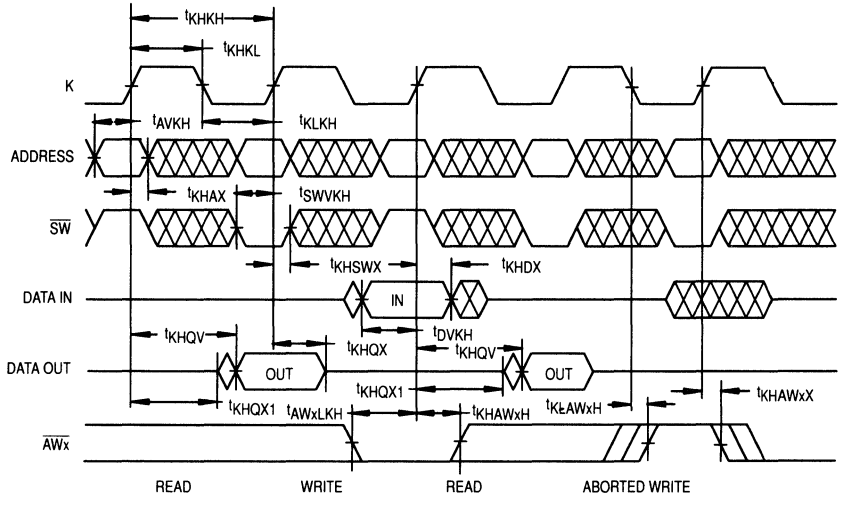
NOTES:
1. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for **ALL** rising edges of clock (K).
2. Into rated load of 85 pF equivalent resistive load (see Figure 1).
3. Transition is measured ±500 mV from steady-state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{KHQZ} is less than t_{KHQX1} and t_{GHQZ} is less than t_{GLQX} for a given device.

9

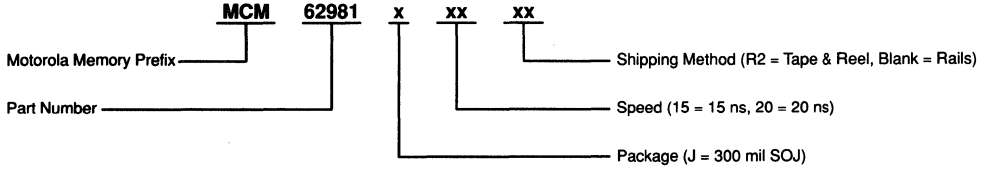
READ CYCLES



READ – WRITE – READ CYCLES



ORDERING INFORMATION
(Order by Full Part Number)



Full Part Number – MCM62981J15 MCM62981J15R2
MCM62981J20 MCM62981J20R2

MCM62982

Advance Information

64K × 4 Bit Fast Synchronous Static RAM with Output Registers

J PACKAGE
PLASTIC
CASE 810B

The MCM62982 is a 262,144 bit synchronous static random access memory organized as 65,536 words of 4 bits, fabricated using Motorola's high-performance silicon-gate CMOS technology. The device integrates a 64K x 4 SRAM core with advanced peripheral circuitry consisting of positive edge triggered registers on address and synchronous write enable inputs and output registers. Asynchronous controls consist of asynchronous write strobe and output enable ($\overline{G}$). This device has increased output drive capability supported by multiple power pins.

Write cycles are differentiated from read cycles by the state of the synchronous write enable pin ($\overline{SW}$) at the rising edge of clock (K). Write cycles are completed only if asynchronous write strobe ($\overline{AW}$) is asserted within the specified setup time of the following rising edge of clock (K). Write cycles may be aborted by negating the $\overline{AW}$ signal prior to the low transition of the clock.

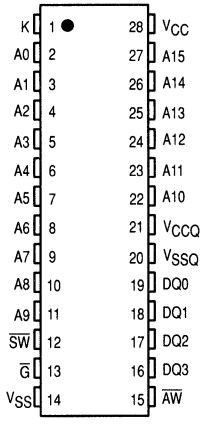
Read cycle output register operation occurs on the rising edge of clock (K) and provides data from the previous clock (K) high in a two cycle pipeline operation.

Additional power supply pins have been utilized and placed on the package for maximum performance. In addition one set of power pins is electrically isolated from the other set and supplies power only to the output buffers. This allows connecting the output buffers to 3.3 V instead of 5.0 V if desired. If 3.3 V output levels are chosen, the output buffer impedance in the "high" state is approximately equal to the impedance in the "low" state which allows simple yet effective transmission line terminations to be achieved.

The MCM62982 will be available in a 28-pin 300-mil plastic SOJ.

- Single 5 V ± 10% Power Supply
- Choice of 5 V or 3.3 V ± 10% Power Supplies for Output Buffers
- Fast Access and Cycle Times: 12/15 ns Max
- Fully Synchronous Operation, Single Clock Control
- Clock Timed Writes with Asynchronous Late Write Abort
- Registered Address Inputs
- Output Registers for Fully Pipelined Applications
- Common Data Inputs and Data Outputs
- Output Enable Controlled Three-State Outputs
- High Output Drive Capability: 85 pF/Output at Rated Access Time
- High Board Density PSOJ Package

PIN ASSIGNMENT

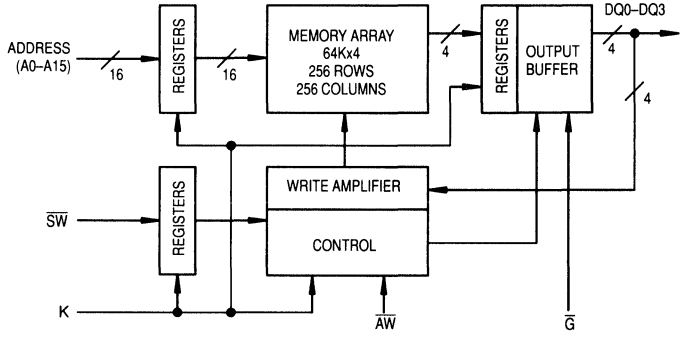


PIN NAMES	
A0–A15	Address Inputs
$\overline{AW}$	Asynchronous Write Strobe
$\overline{SW}$	Synchronous Write Enable
K	Clock
$\overline{G}$	Output Enable
DQ0–DQ3	Data Input/Output
V_{CC}	+5 V Power Supply
V_{CCQ}	Output Buffer Power Supply
V_{SSQ}	Output Buffer Ground
V_{SS}	Ground

All power supply and ground pins must be connected for proper operation of the device. $V_{CC} \geq V_{CCQ}$ at all times including power up.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

BLOCK DIAGRAM



TRUTH TABLE (See Note)

$\overline{SW}$	$\overline{AW}$	$\overline{G}$	Mode	Supply Current	I/O Status
H	X	L	Read Cycle	I_{CC}	Data Out
H	X	H	Read Cycle	I_{CC}	High-Z
L	L	X	Write Cycle	I_{CC}	High-Z
L	H	X	Aborted Write Cycle	I_{CC}	High-Z

NOTE: $\overline{SW}$ and $\overline{AW}$ satisfy the specified setup and hold times for the rising edge of clock (K).

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to $V_{SS} = V_{SSQ} = 0$ V, See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	–0.5 to 7.0	V
Voltage Relative to V_{SS}/V_{SSQ} for Any Pin Except V_{CC} and V_{CCQ}	V_{in}, V_{out}	–0.5 to V_{CC} +0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation (T_A = 25°C)	P_D	1.0	W
Temperature Under Bias	T_{bias}	–10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	–55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electrical fields; however, it is advised that normal precautions to taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High-Z at power up.

9

AC TEST LOADS

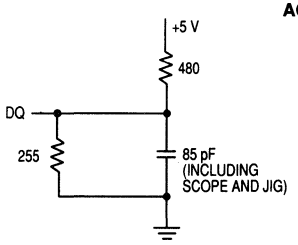


Figure 1A

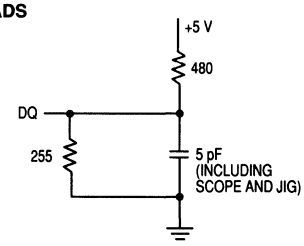


Figure 1B

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, V_{CCQ} = 5.0 V or 3.3 V ± 10%, T_A = 0 to +70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = V_{SSQ} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Output Buffer Supply Voltage (5.0 V TTL Compatible) (3.3 V 50 Ω Compatible)	V_{CCQ}*	 4.5 3.0	 5.0 3.3	 5.5 3.6	V
Input High Voltage	V_{IH}	2.2	3.0	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	–0.5**	0.0	0.8	V

*V_{CCQ} must be ≤ V_{CC} at all times, including power up.
**V_{IL} (min) = –3.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

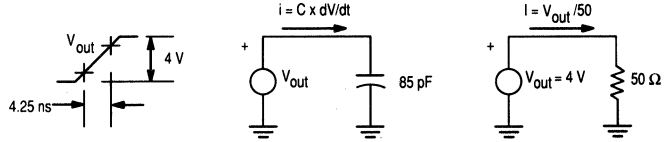
Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	—	±1.0	µA
Output Leakage Current ($\overline{G}$ = V_{IH})	$I_{lkg(O)}$	—	—	±1.0	µA
AC Supply Current ($\overline{G}$ = V_{IH}, All Inputs = V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, I_{out} = 0 mA, Cycle Times ≥ t_{KHKH} min)	I_{CCA}	—	150	170	mA
Output Low Voltage (I_{OL} = +8.0 mA)	V_{OL}	—	—	0.4	V
Output High Voltage (I_{OH} = –4.0 mA)	V_{OH}	2.4	—	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (All Pins Except DQ0–DQ3)	C_{in}	4	6	pF
Input/Output Capacitance (DQ0–DQ3)	$C_{I/O}$	8	10	pF

9

CAPACITIVE LOAD EQUIVALENT RESISTANCE



$$i = C \times \left(\frac{dV_{out}}{dt}\right) = 85 \times 10^{-12} \times \left(\frac{4\ V}{4.25 \times 10^{-9}}\right) = 80\ mA \qquad i = \frac{V}{R} = \frac{4}{50} = 80\ mA$$

85 pF load is equivalent to a 50 Ω termination

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, V_{CCQ} = 5.0 V or 3.3 V ± 10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

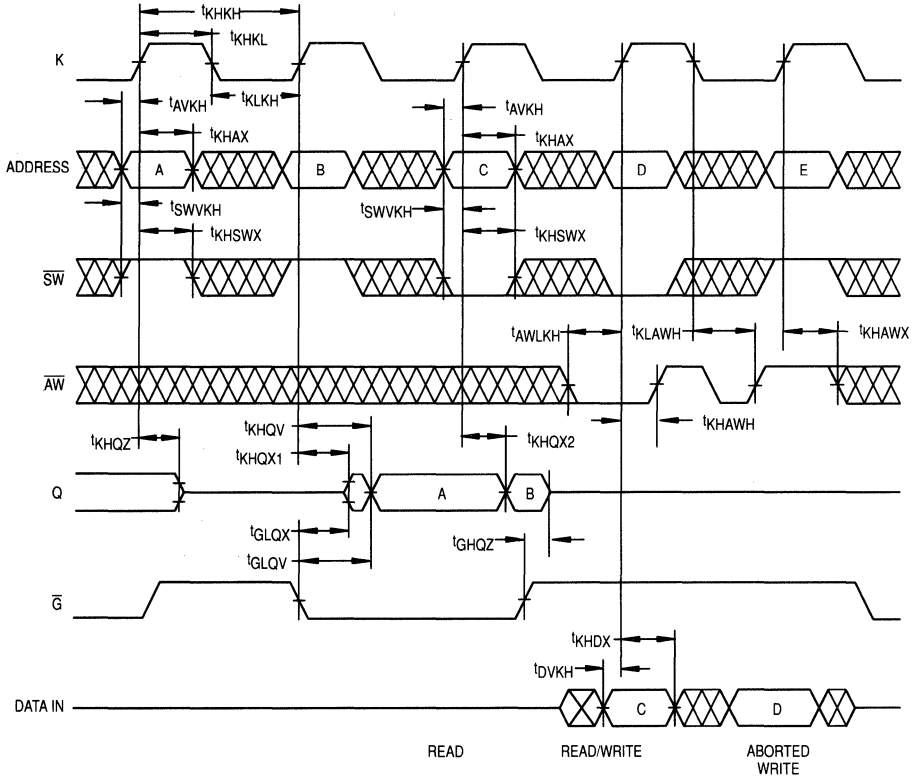
READ AND WRITE CYCLE TIMING (See Note 1)

Parameter	Symbol	MCM62982–12		MCM62982–15		Unit	Notes
		Min	Max	Min	Max		
Cycle Times:						ns	
Clock High to Clock High	t_{KHKH}	12	—	15	—		
Access Times:						ns	
Clock High to Output Valid	t_{KHQV}	—	8	—	10		2
Output Enable Low Output Valid	t_{GLQV}	—	6	—	6		2
Aborted Write Cycles:						ns	
Clock Low to Asynchronous Write Strobe High	t_{KLAWH}	—	0	—	0		
Clock High to Asynchronous Write Strobe Invalid	t_{KHAWX}	2	—	2	—		
Output Buffer Control:						ns	
Output Enable High to Output High-Z	t_{GHQZ}	0	6	2	6		3
Output Enable Low to Output Low-Z	t_{GLQX}	0	—	2	—		3
Reads:							
Clock High to Output Low-Z after Write	t_{KHQX1}	4	—	4	—		3
Clock High to Output Invalid	t_{KHQX2}	5	—	5	—		
Writes:							
Clock High to Output High-Z after Read	t_{KHQZ}	3	8	3	10		3
Clock:						ns	
Clock High Time	t_{KHKL}	3	—	4	—		
Clock Low Time	t_{KLKH}	8	—	8	—		
Setup Times:						ns	
Address Valid to Clock High	t_{AVKH}	2	—	2	—		
Synchronous Write Enable Valid to Clock High	t_{SWVKH}	2	—	2	—		
Writes:							
Data In Valid to Clock High	t_{DVKH}	5	—	6	—		
Asynchronous Write Strobe Low to Clock High	t_{AWLKH}	5	—	6	—		
Hold Times:						ns	
Clock High to Address Invalid	t_{KHAX}	2	—	2	—		
Clock High to Synchronous Write Enable Invalid	t_{KHSWX}	2	—	2	—		
Writes:							
Clock High to Data In Invalid	t_{KHDX}	0	—	0	—		
Clock High to Asynchronous Write Strobe High	t_{KHAWH}	2	—	2	—		

NOTES:
1. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for **ALL** rising edges of clock (K).
2. Into rated load of 85 pF equivalent resistive load (see Figure 1).
3. Transition is measured ±500 mV from steady-state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{KHQZ} is less than t_{KHQX1} and t_{GHQZ} is less than t_{GLQX} for a given device.

9

READ AND WRITE CYCLES



ORDERING INFORMATION
(Order by Full Part Number)

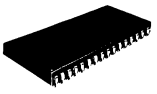
MCM	62982	x	xx	xx
Motorola Memory Prefix	Part Number	Package (J = 300 mil SOJ)	Speed (12 = 12 ns, 15 = 15 ns)	Shipping Method (R2 = Tape & Reel, Blank = Rails)

Full Part Numbers – MCM62982J12 MCM62982J12R2
MCM62982J15 MCM62982J15R2

MCM62983

Advance Information

64K × 4 Bit Fast Synchronous ParityRAM™ with Output Registers



J PACKAGE
PLASTIC
CASE 857

The MCM62983 is a 262,144 bit synchronous static random access memory organized as 65,536 words of 4 bits, fabricated using Motorola's high-performance silicon-gate CMOS technology. The device integrates a 64K x 4 SRAM core with advanced peripheral circuitry consisting of positive edge triggered registers on address and synchronous write enable inputs. Asynchronous controls include asynchronous write strobes and output enable ($\overline{G}$). This device has increased output drive capability supported by multiple power pins. Four asynchronous write strobes ($\overline{AW0}$–$\overline{AW3}$) are provided to allow each bit position to be written individually, thereby simplifying the task of supporting byte parity. This x4 organized SRAM is ideally suited for parity on 32 bit words. The device is functionally similar to the MCM62982 with the only difference being the individual bit write capablilty.

Write cycles are differentiated from read cycles by the state of the synchronous write enable pin ($\overline{SW}$) at the rising edge of clock (K). Write cycles are completed only if the appropriate asynchronous write strobe ($\overline{AWx}$) is asserted within the specified setup time of the following rising edge of clock (K). Write cycles may be aborted by ensuring each $\overline{AWx}$ is negated by the time the clock transitions to the low state.

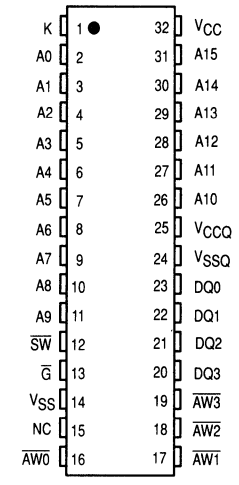
Read cycle output register operation occurs on the rising edge of clock (K) and provides data from the previous clock (K) high in a two cycle pipeline operation.

Additional power supply pins have been utilized and placed on the package for maximum performance. In addition one set of power pins is electrically isolated from the other set and supplies power only to the output buffers. This allows connecting the output buffers to 3.3 V instead of 5.0 V if desired. If 3.3 V output levels are chosen, the output buffer impedance in the "high" state is approximately equal to the impedance in the "low" state which allows simple yet effective transmission line terminations to be achieved.

The MCM62983 will be available initially in a 32-pin 300-mil plastic SOJ followed by a 300-mil 32-pin plastic DIP.

- Single 5 V ± 10% Power Supply
- Choice of 5 V or 3.3 V ± 10% Power Supplies for Output Level Buffers
- Fast Access and Cycle Times: 12/15 ns Max
- Fully Synchronous Operation, Single Clock Control
- Clock Timed Writes with Asynchronous Late Write Abort
- Each Bit Position Individually Writeable for Simple Parity Support
- Registered Address Inputs
- Output Registers for Fully Pipelined Applications
- Common Data Inputs and Data Outputs
- Output Enable Controlled Three-State Outputs
- High Output Drive Capability: 85 pF/Output at Rated Access Time
- High Board Density PSOJ Package

PIN ASSIGNMENT



PIN NAMES

A0–A15	Address Inputs
$\overline{AW0}$–$\overline{AW3}$	Asynchronous Write Strobes
$\overline{SW}$	Synchronous Write Enable
K	Clock
$\overline{G}$	Output Enable
DQ0–DQ3	Data Input/Output
V_{CC}	+5 V Power Supply
V_{CCQ}	Output Buffer Power Supply
V_{SSQ}	Output Buffer Ground
V_{SS}	Ground
NC	No Connect

All power supply and ground pins must be connected for proper operation of the device. $V_{CC} \geq V_{CCQ}$ at all times including power up.

ParityRAM is a trademark of Motorola Inc.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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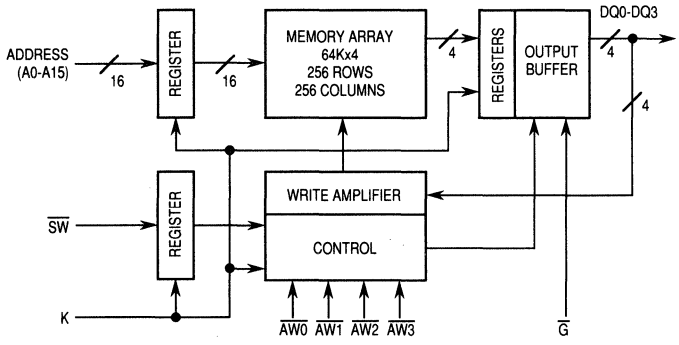
BLOCK DIAGRAM



TRUTH TABLE (See Note)

$\overline{SW}$	$\overline{AWx}$	$\overline{G}$	Mode	Supply Current	I/O Status
H	X	L	Read Cycle	I_{CC}	Data Out
H	X	H	Read Cycle	I_{CC}	High-Z
L	L	X	Write Cycle	I_{CC}	High-Z
L	H	X	Aborted Write Cycle	I_{CC}	High-Z

NOTE: $\overline{SW}$ and $\overline{AWx}$ satisfy the specified setup and hold times for the rising edge of clock (K).

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to $V_{SS} = V_{SSQ} = 0$ V, See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to 7.0	V
Voltage Relative to V_{SS}/V_{SSQ} for Any Pin Except V_{CC} and V_{CCQ}	V_{in}, V_{out}	−0.5 to V_{CC} +0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation (T_A=25°C)	P_D	1.0	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electrical fields; however, it is advised that normal precautions to taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High-Z at power up.

AC TEST LOADS

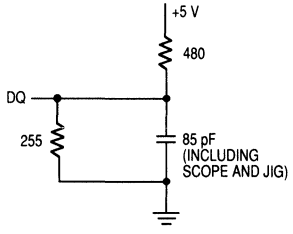


Figure 1A

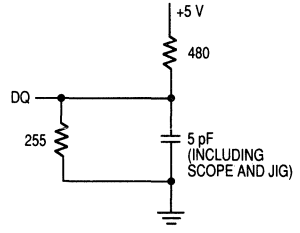


Figure 1B

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, V_{CCQ} = 5.0 V or 3.3 V ± 10%, T_A = 0 to +70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = V_{SSQ} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Output Buffer Supply Voltage (5.0 V TTL Compatible) (3.3 V 50 Ω Compatible)	V_{CCQ}*	 4.5 3.0	 5.0 3.3	 5.5 3.6	V
Input High Voltage	V_{IH}	2.2	3.0	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	–0.5**	0.0	0.8	V

*V_{CCQ} must be ≤ V_{CC} at all times, including power up.
**V_{IL} (min) = –3.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	—	±1.0	µA
Output Leakage Current ($\overline{G}$ = V_{IH})	$I_{lkg(O)}$	—	—	±1.0	µA
AC Supply Current ($\overline{G}$ = V_{IH}, All Inputs = V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, I_{out} = 0 mA, Cycle Times ≥ t_{KHKH} min)	I_{CCA}	—	150	170	mA
Output Low Voltage (I_{OL} = +8.0 mA)	V_{OL}	—	—	0.4	V
Output High Voltage (I_{OH} = –4.0 mA)	V_{OH}	2.4	—	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (All Pins Except DQ0–DQ3)	C_{in}	4	6	pF
Input/Output Capacitance (DQ0–DQ3)	$C_{I/O}$	8	10	pF

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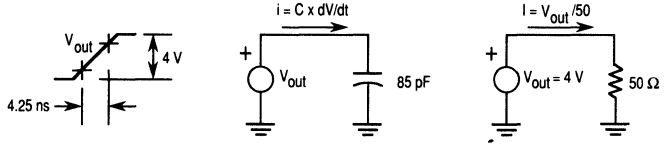
CAPACITIVE LOAD EQUIVALENT RESISTANCE



$$i = C \times \left(\frac{dV_{out}}{dt}\right) = 85 \times 10^{-12} \times \left(\frac{4\ V}{4.25 \times 10^{-9}}\right) = 80\ mA$$

$$i = \frac{V}{R} = \frac{4}{50} = 80\ mA$$

85 pF load is equivalent to a 50 Ω termination

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, V_{CCQ} = 5.0 V or 3.3 V ± 10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

READ AND WRITE CYCLE TIMING (See Note 1)

Parameter	Symbol	MCM62983–12		MCM62983–15		Unit	Notes
		Min	Max	Min	Max		
Cycle Times:						ns	
Clock High to Clock High	t_{KHKH}	12	—	15	—		
Access Times:						ns	
Clock High to Output Valid	t_{KHQV}	—	8	—	10		2
Output Enable Low Output Valid	t_{GLQV}	—	6	—	6		2
Aborted Write Cycles:						ns	
Clock Low to Asynchronous Write Strobe High	t_{KLAWxH}	—	0	—	0		
Clock High to Asynchronous Write Strobe Invalid	t_{KHAWxX}	2	—	2	—		
Output Buffer Control:						ns	
Output Enable High to Output High-Z	t_{GHQZ}	0	6	2	6		3
Output Enable Low to Output Low-Z	t_{GLQX}	0	—	2	—		3
Reads:							
Clock High to Output Low-Z after Write	t_{KHQX1}	4	—	4	—		3
Clock High to Output Invalid	t_{KHQX2}	5	—	5	—		
Writes:							
Clock High to Output High-Z after Read	t_{KHQZ}	3	8	3	10		3
Clock:						ns	
Clock High Time	t_{KHKL}	3	—	4	—		
Clock Low Time	t_{KLKH}	8	—	8	—		
Setup Times:						ns	
Address Valid to Clock High	t_{AVKH}	2	—	2	—		
Synchronous Write Enable Valid to Clock High	t_{SWVKH}	2	—	2	—		
Writes:							
Data In Valid to Clock High	t_{DVKH}	5	—	6	—		
Asynchronous Write Strobe Low to Clock High	t_{AWxLKH}	5	—	6	—		
Hold Times:						ns	
Clock High to Address Invalid	t_{KHAX}	2	—	2	—		
Clock High to Synchronous Write Enable Invalid	t_{KHSWX}	2	—	2	—		
Writes:							
Clock High to Data In Invalid	t_{KHDX}	0	—	0	—		
Clock High to Asynchronous Write Strobe High	t_{KHAWxH}	2	—	2	—		

NOTES:
1. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for **ALL** rising edges of clock (K).
2. Into rated load of 85 pF equivalent resistive load (see Figure 1).
3. Transition is measured ± 500 mV from steady-state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{KHQZ} is less than t_{KHQX1} and t_{GHQZ} is less than t_{GLQX} for a given device.

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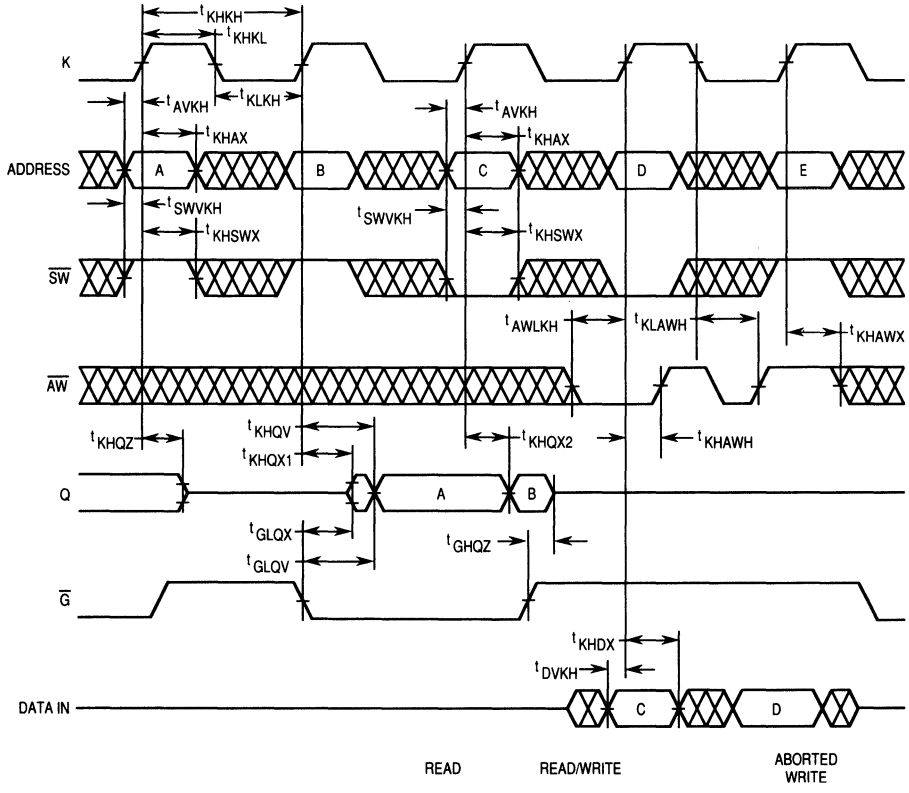
READ AND WRITE CYCLES



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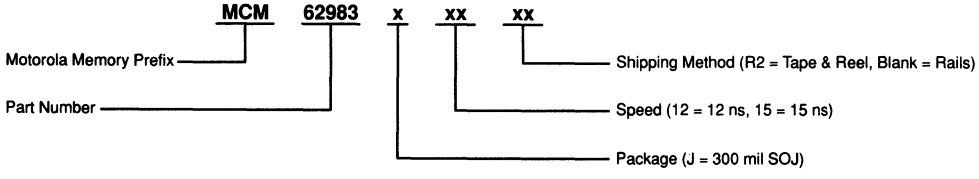
ORDERING INFORMATION
(Order by Full Part Number)

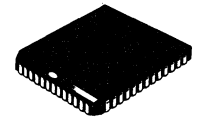


Full Part Number – MCM62983J12 MCM62983J12R2
MCM62983J15 MCM62983J15R2

MCM62990

Advance Information

16K × 16 Bit Fast Synchronous Static RAM



FN PACKAGE
PLASTIC
CASE 778

The MCM62990 is a 262,144 bit synchronous static random access memory organized as 16,384 words of 16 bits, fabricated using Motorola's high-performance silicon-gate CMOS technology. The device integrates a 16Kx16 SRAM core with advanced peripheral circuitry. Inputs to the device fall into two categories: synchronous and asynchronous. All synchronous inputs pass through positive-edge- triggered registers controlled by a single clock input (K). The synchronous inputs include all addresses, the two chip enables (SE and $\overline{SE}$), and the synchronous write enable ($\overline{SW}$).

Asynchronous inputs include the asynchronous byte write strobes ($\overline{AWL}$ and $\overline{AWH}$), output enable ($\overline{G}$), data (DQ0–DQ15), data latch enable (DL), and the clock (K). Input data can be asynchronously latched by DL to provide simplified data-in timings during write cycles.

Address and write control are registered on-chip which greatly simplifies write cycles. Dual write strobes ($\overline{AWL}$ and $\overline{AWH}$) are provided to allow individually writeable bytes. $\overline{AWL}$ controls DQ0–DQ7, the lower bits while $\overline{AWH}$ controls DQ8–DQ15, the upper bits. In addition, the AWs allow late write cycles to be aborted if they are "false" during the low period of the clock. Dual chip enables (SE and $\overline{SE}$) are provided allowing address decoding to be accomplished on-chip when the device is used in a dual bank mode.

An input data latch is provided. When data latch enable (DL) is high the data latches are in the transparent state. When DL is low the data latches are in the latched state. This data input latch simplifies write cycles by guaranteeing data hold time in a simple fashion.

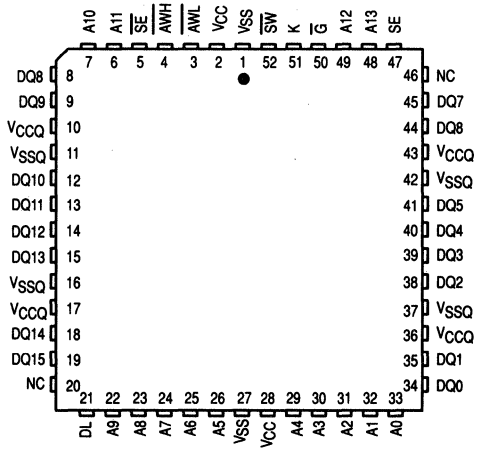
Additional power supply pins have been utilized and placed on the package for maximum performance. In addition one set of power pins is electrically isolated from the other two and supplies power only to the output buffers. This allows connecting the output buffers to 3.3 V instead of 5.0 V if desired. If 3.3 V output levels are chosen, the output buffer impedance in the "high" state is approximately equal to the impedance in the "low" state which allows simple yet effective transmission line terminations to be achieved.

The MCM62990 will be available in a 52 pin plastic leaded chip carrier (PLCC).

Typical applications for this device are cache memory and tag RAMs, memory in systems which are pipelined and systems which require wide data bus widths and reduced parts count.

- Single 5 V ± 10% Power Supply
- Choice of 5 V or 3.3 V Power Supplies for Output Buffers
- Fast Access and Cycle Times: 17/20/25 ns Max
- Byte Writeable via Dual Write Strobes with Abort Write Capability
- Separate Data Input Latch for Simplified Write Cycles
- Clock Controlled Registered Address, Write Control, and Dual Chip Enables
- Common Data Inputs and Data Outputs
- Output Enable Controlled Three-State Outputs
- High Output Drive Capability: 85 pF/Output at Rated Access Time
- High Board Density 52 Lead PLCC Package

PIN ASSIGNMENT

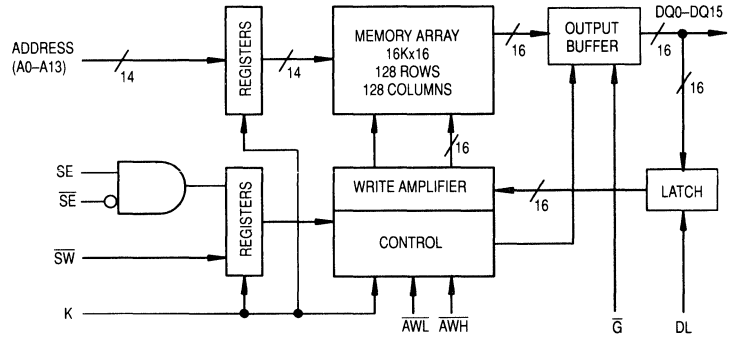


PIN NAMES	
A0–A13	Address Inputs
K	Clock Input
DL	Data Latch Enable
$\overline{SW}$	Synchronous Write Enable
$\overline{AWL}$	Lower Byte Async Write Strobe
$\overline{AWH}$	Upper Byte Async Write Strobe
SE	Synchronous Chip Enable
$\overline{SE}$	Synchronous Chip Enable
$\overline{G}$	Asynchronous Output Enable
DQ0–DQ15	Data Input/Output
V_{CC}	+5 V Power Supply
V_{CCQ}	Output Buffer Power Supply
V_{SSQ}	Output Buffer Ground
V_{SS}	Ground
NC	No Connect

All power supply and ground pins must be connected for proper operation of the device. $V_{CC} \geq V_{CCQ}$ at all times including power up.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

BLOCK DIAGRAM



TRUTH TABLE (See Notes)

SEs	$\overline{SW}$	$\overline{AWL}$	$\overline{AWH}$	DL	$\overline{G}$	Mode	Supply Current	I/O Status
F	X	X	X	X	X	Deselected Cycle	I_{SB}	High-Z
T	H	X	X	X	H	Read Cycle	I_{CC}	High-Z
T	H	X	X	X	L	Read Cycle	I_{CC}	Data Out
T	L	L	L	H	X	Write Cycle All Bits Transparent Data In	I_{CC}	High-Z
T	L	H	H	X	X	Aborted Write Cycle	I_{CC}	High-Z
T	L	L	H	H	X	Write Cycle Lower 8 Bits Transparent Data In	I_{CC}	High-Z
T	L	H	L	L	X	Write Cycle Upper 8 Bits Latched Data In	I_{CC}	High-Z

NOTES:
1. X means don't care. True (T) is $\overline{SE}$ = 1 and $\overline{SE}$ = 0.
2. Registered inputs (addresses, $\overline{SW}$, SE, and $\overline{SE}$) satisfy the specified setup and hold times about the rising edge of clock (K). Data-in satisfies the specified setup and hold times for DL.
3. A transparent write cycle is defined by DL high during the write cycle.
4. A latched write cycle is defined by DL transitioning low during the write cycle and satisfying the specified setup and hold times.

This device contains circuitry to protect the inputs against damage due to high static voltages or electrical fields; however, it is advised that normal precautions to taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High Z at power up.

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to V_{SS} = V_{SSQ} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	–0.5 to 7.0 V	V
Voltage Relative to V_{SS}/V_{SSQ} for Any Pin Except V_{CC} and V_{CCQ}	V_{in}, V_{out}	–0.5 to V_{CC} +0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation (T_A = 70°C)	P_D	2.0	W
Temperature Under Bias	T_{bias}	–10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	–55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, V_{CCQ} = 5.0 V or 3.3 V ± 10%, T_A = 0 to +70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = V_{SSQ} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Output Buffer Supply Voltage (5.0 V TTL Compatible) (3.3 V 50 Ω Compatible)	V_{CCQ}*	 4.5 3.0	 5.0 3.3	 5.5 3.6	V
Input High Voltage	V_{IH}	2.2	3.0	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	–0.5**	0.0	0.8	V

*V_{CCQ} must be ≤ V_{CC} at all times, including power up.
**V_{IL} (min) = –3.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	—	±1.0	µA
Output Leakage Current ($\overline{G}$ = V_{IH})	$I_{lkg(O)}$	—	—	±1.0	µA
AC Supply Current ($\overline{G}$ = V_{IH}, All Inputs = V_{IL} or V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, I_{out} = 0 mA, Cycle Time ≥ t_{KHKH} min) MCM62990–17: t_{KHKH} = 17 ns MCM62990–20: t_{KHKH} = 20 ns MCM62990–25: t_{KHKH} = 25 ns	I_{CCA}	 — — —	 280 290 310	 360 360 360	mA
Standby Current ($\overline{E}$ = V_{IH}, E = V_{IL}, All Inputs = V_{IL} or V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, I_{out} = 0 mA, Cycle Time ≥ t_{KHKH} min)	I_{SB}	—	50	80	mA
Output Low Voltage (I_{OL} = +8.0 mA)	V_{OL}	—	—	0.4	V
Output High Voltage (I_{OH} = –4.0 mA)	V_{OH}	2.4	—	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (All Pins Except DQ0–DQ15)	C_{in}	4	6	pF
Input/Output Capacitance (DQ0–DQ15)	$C_{I/O}$	8	10	pF

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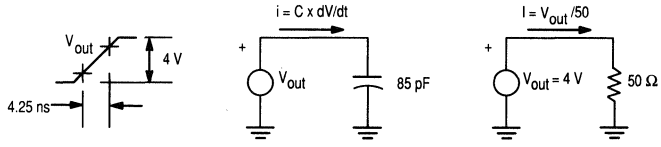
CAPACITIVE LOAD EQUIVALENT RESISTANCE



$$i = C \times \left(\frac{dV_{out}}{dt}\right) = 85 \times 10^{-12} \times \left(\frac{4\ V}{4.25 \times 10^{-9}}\right) = 80\ mA \qquad i = \frac{V}{R} = \frac{4}{50} = 80\ mA$$

85 pF load is equivalent to a 50 Ω termination

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, V_{CCQ} = 5.0 V or 3.3 V ± 10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

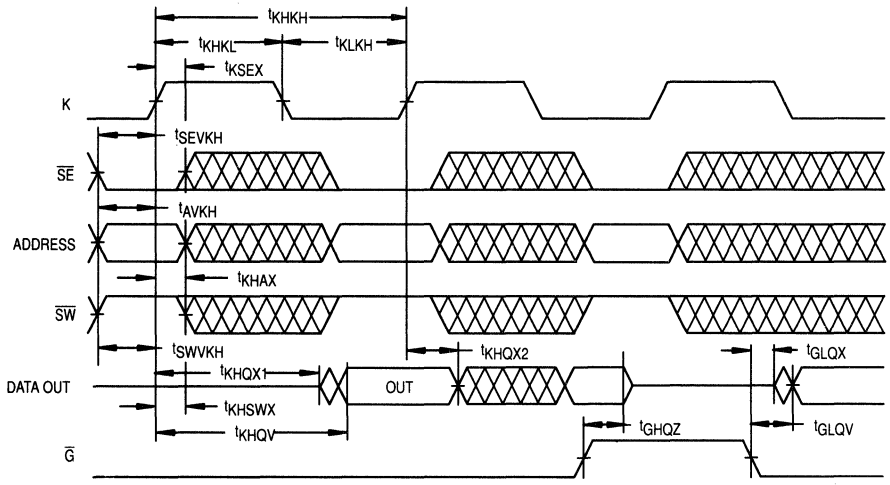
Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

READ AND WRITE CYCLE TIMING (See Notes 1 and 2)

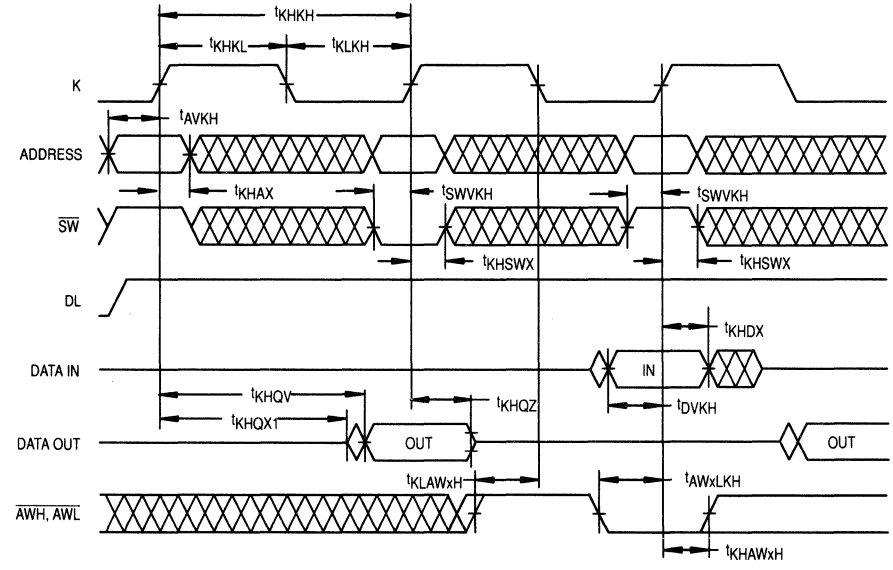
Parameter	Symbol	MCM62990-17		MCM62990-20		MCM62990-25		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Cycle Times								ns	
Clock High to Clock High	t_{KHKH}	17	—	20	—	25	—		
Access Times								ns	
Clock High to Output Valid	t_{KHQV}	—	17	—	20	—	25		3
Output Enable Low to Output Valid	t_{GLQV}	—	6	—	8	—	10		3
Aborted Write Cycles								ns	
Clock Low to Asynchronous Write Strobes ($\overline{AWL}$, $\overline{AWH}$) High	t_{KLAWxH}	—	0	—	0	—	0		
Clock High to $\overline{AWx}$ Invalid	t_{KHAWxX}	2	—	2	—	2	—		
Output Buffer Control								ns	
Asynchronous Output Enable ($\overline{G}$) High to Output High Z	t_{GHQZ}	2	6	2	8	2	10		4
$\overline{G}$ Low to Output Low Z	t_{GLQX}	2	—	2	—	2	—		4
Reads:									
Clock (K) High to Output Low Z After Deselect or Write	t_{KHQX1}	8	—	8	—	8	—		4
Data Out Hold After Clock High	t_{KHQX2}	5	—	5	—	5	—		
Writes:									
K High to Output High Z After Read	t_{KHQZ}	3	10	3	10	3	12		4
Clock								ns	
Clock High Time	t_{KHKL}	4	—	4	—	4	—		
Clock Low Time	t_{KLKH}	8	—	10	—	10	—		
Setup Time								ns	
Address Valid to Clock High	t_{AVKH}	3	—	3	—	3	—		5
Synchronous Write ($\overline{SW}$) Valid to Clock High	t_{SWVKH}	3	—	3	—	3	—		5
Synchronous Enables (SE, $\overline{SE}$) Valid to Clock High	t_{SEVKH}	3	—	3	—	3	—		5
Writes:									
Data-In Valid to CLock High	t_{DVKH}	6	—	6	—	7	—		1, 5
$\overline{AWL}$, $\overline{AWH}$ Low to Clock High	t_{AWxLKH}	6	—	6	—	7	—		5
Data Latch:									
Data-In Valid to DL Low	t_{DVDLL}	1	—	1	—	1	—		2, 5
Hold Times								ns	
Clock High to Address Invalid	t_{KHAX}	2	—	2	—	2	—		5
Clock High to $\overline{SW}$ Invalid	t_{KHSWX}	2	—	2	—	2	—		5
Clock High to SE, $\overline{SE}$ Invalid	t_{KHSEX}	2	—	2	—	2	—		5
Writes:									
Clock High to Data-In Invalid	t_{KHDX}	2	—	2	—	2	—		1, 5
Clock High to $\overline{AWL}$, $\overline{AWH}$ High	t_{KHAWxH}	2	—	2	—	2	—		5
Clock High to DL High	t_{KHDLH}	2	—	2	—	2	—		2, 5
Data Latch:									
DL Low to Data-In Invalid	t_{DLLDX}	3	—	3	—	3	—		2, 5
DL High to Clock High	t_{DLHKH}	6	—	6	—	7	—		2, 5

NOTES:
1. A transparent write cycle is defined by DL high during the write cycle.
2. A latched write cycle is defined by DL transitioning low during the write cycle and satisfying the specified hold time for the rising edge of clock (K).
3. Into rated load of 85 pF equivalent resistive load (see Figure 1A).
4. Transition is measured ±500 mV from steady-state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{KHQZ} is less than t_{KHQX} and t_{GHQZ} is less than t_{GLQX} for a given device.
5. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for **ALL** rising edges of clock (K) or falling edges of data latch enable (DL).

READ CYCLES

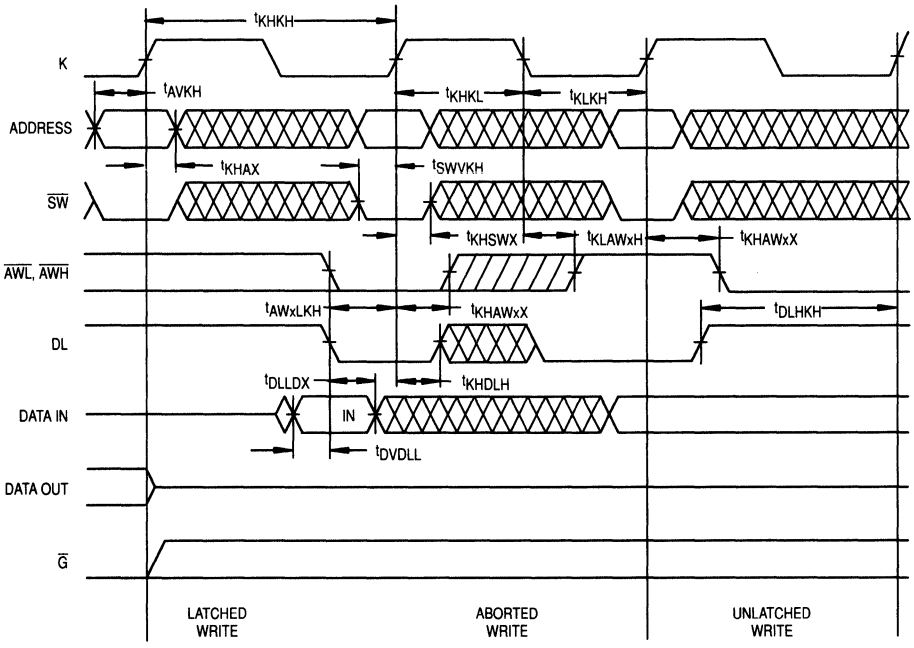


READ — UNLATCHED WRITE — READ CYCLES



9

WRITE CYCLES



AC TEST LOADS

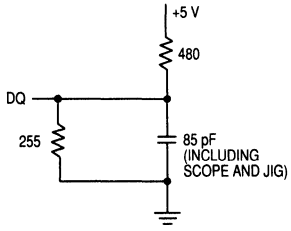


Figure 1A

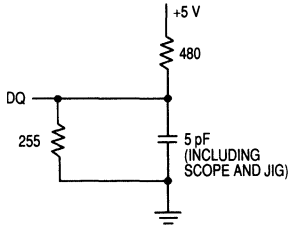
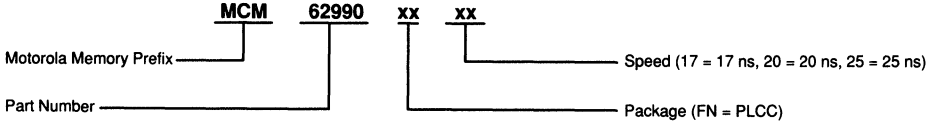


Figure 1B

ORDERING INFORMATION
(Order by Full Part Number)

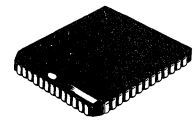


Full Part Number – MCM62990FN17 MCM62990FN20 MCM62990FN25

MCM62995

Advance Information

16K × 16 Bit Asynchronous/Latched Address Fast Static RAM



FN PACKAGE
PLASTIC
CASE 778

The MCM62995 is a 262,144 bit latched address static random access memory organized as 16,384 words of 16 bits, fabricated using Motorola's high-performance silicon-gate CMOS technology. The device integrates a 16Kx16 SRAM core with advanced peripheral circuitry consisting of address and data input latches, active high and active low chip enables, separate upper and lower byte write strobes, and a fast output enable. This device has increased output drive capability supported by multiple power pins. In addition, the output levels can be either 3.3 V or 5 V TTL compatible by choice of the appropriate output bus power supply.

Address, data in, and chip enable latches are provided. When latch enable (LE for address and chip enables and DL for data in) is high the address, data in, and chip enable latches are in the transparent state. If latch enable (LE, DL) is tied high the device can be used as a asynchronous SRAM. When latch enable (LE, DL) is low the address, data in, and chip enable latches are in the latched state. This input latch simplifies read and write cycles by guaranteeing address and data-in hold time in a simple fashion.

Dual write strobes ($\overline{BWL}$ and $\overline{BWH}$) are provided to allow individually writeable bytes. $\overline{BWL}$ controls DQ0–DQ7, the lower bits. While $\overline{BWH}$ controls DQ8–DQ15, the upper bits.

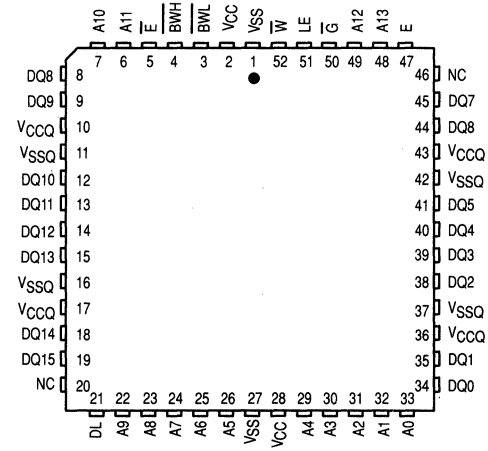
Additional power supply pins have been utilized and placed on the package for maximum performance. In addition, the output buffer power pins are electrically isolated from the other two and supply power only to the output buffers. This allows connecting the output buffers to 3.3 V instead of 5.0 V if desired. If 3.3 V output levels are chosen, the output buffer impedance in the "high" state is approximately equal to the impedance in the "low" state thereby allowing simplified transmission line terminations.

The MCM62995 will be available in a 52 pin plastic leaded chip carrier (PLCC).

This device is ideally suited for systems which require wide data bus widths, cache memory, and tag RAMs. See Figure 2 for applications information.

- Single 5 V ± 10% Power Supply
- Choice of 5 V or 3.3 V ± 10% Power Supplies for Output Buffers
- Fast Access and Cycle Times: 17/20/25 ns Max
- Byte Writeable via Dual Write Strobes with Abort Write Capability
- Separate Data Input Latch for Simplified Write Cycles
- Address and Chip Enable Input Latches
- Common Data Inputs and Data Outputs
- Output Enable Controlled Three-State Outputs
- High Output Drive Capability: 85 pF/Output at Rated Access Time
- High Board Density 52 Lead PLCC Package

PIN ASSIGNMENT

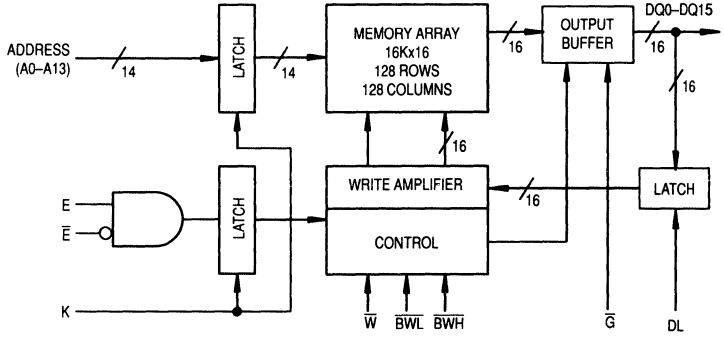


PIN NAMES	
A0–A13	Address Inputs
LE	Latch Enable
DL	Data Latch Enable
$\overline{W}$	Write Enable
$\overline{BWL}$	Byte Write Strobe Low
BWH	Byte Write Strobe High
E	Active High Chip Enable
$\overline{E}$	Active Low Chip Enable
$\overline{G}$	Output Enable
DQ0–DQ15	Data Input/Output
V_{CC}	+5 V Power Supply
V_{CCQ}	Output Buffer Power Supply
V_{SSQ}	Otuput Buffer Ground
V_{SS}	Ground
NC	No Connect

All power supply and ground pins must be connected for proper operation of the device. $V_{CC} \geq V_{CCQ}$ at all times including power up.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

BLOCK DIAGRAM



TRUTH TABLE (See Note)

Es	W	BWL	BWH	LE	DL	G	Mode	Supply Current	I/O Status
F	X	X	X	X	X	X	Deselected Cycle	I_{SB}	High-Z
T	H	X	X	H	X	H	Read Cycle	I_{CC}	High-Z
T	H	X	X	H	X	L	Read Cycle	I_{CC}	Data Out
T	H	X	X	L	X	L	Latched Read Cycle	I_{CC}	Data Out
T	L	L	L	H	H	X	Write Cycle All Bits	I_{CC}	High-Z
T	L	H	H	X	X	X	Aborted Write Cycle	I_{CC}	High-Z
T	L	L	H	H	H	X	Write Cycle Lower 8 Bits	I_{CC}	High-Z
T	L	H	L	H	L	X	Write Cycle Upper 8 Bits Latched Data In	I_{CC}	High-Z
T	L	L	L	L	L	X	Latched Write Cycle Latched Data In	I_{CC}	High-Z

NOTE: True (T) is E = 1 and Ē = 0. E, Ē, and addresses satisfy the specified setup and hold times for the falling edge of LE. Data in satisfies the specified setup and hold time for falling edge of DL.

This device contains circuitry to protect the inputs against damage due to high static voltages or electrical fields; however, it is advised that normal precautions to taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High-Z at power up.

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to $V_{SS} = V_{SSQ} = 0$ V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	–0.5 to 7.0	V
Voltage Relative to V_{SS}/V_{SSQ} for Any Pin Except V_{CC} and V_{CCQ}	V_{in}, V_{out}	–0.5 to V_{CC} +0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation (T_A = 70°C)	P_D	2.0	W
Temperature Under Bias	T_{bias}	–10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	–55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, V_{CCQ} = 5.0 V or 3.3 V ± 10%, T_A = 0 to +70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = V_{SSQ} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Output Buffer Supply Voltage (5.0 V TTL Compatible) (3.3 V 50 Ω Compatible)	V_{CCQ}*	 4.5 3.0	 5.0 3.3	 5.5 3.6	V
Input High Voltage	V_{IH}	2.2	3.0	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	–0.5**	0.0	0.8	V

*V_{CCQ} must be ≤ V_{CC} at all times, including power up.
**V_{IL} (min) = –3.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	—	± 1.0	µA
Output Leakage Current ($\overline{G}$ = V_{IH})	$I_{lkg(O)}$	—	—	± 1.0	µA
AC Supply Current ($\overline{G}$ = V_{IL}, All Inputs = V_{IL} or V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, I_{out} = 0 mA, Cycle Time ≥ t_{AVAV} min) MCM62995–17: t_{AVAV} = 17 ns MCM62995–20: t_{AVAV} = 20 ns MCM62995–25: t_{AVAV} = 25 ns	I_{CCA}	 — — —	 310 290 280	 360 360 360	mA
Standby Current ($\overline{E}$ = V_{IH}, E = V_{IL}, All Inputs = V_{IL} or V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, I_{out} = 0 mA, Cycle Time ≥ t_{AVAV} min)	I_{SB}	—	50	80	mA
Output Low Voltage (I_{OL} = +8.0 mA)	V_{OL}	—	—	0.4	V
Output High Voltage (I_{OH} = –4.0 mA)	V_{OH}	2.4	—	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (All Pins Except DQ0–DQ15)	C_{in}	4	6	pF
Input/Output Capacitance (DQ0–DQ15)	$C_{I/O}$	8	10	pF

TEST LOADS

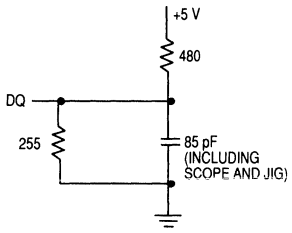


Figure 1A

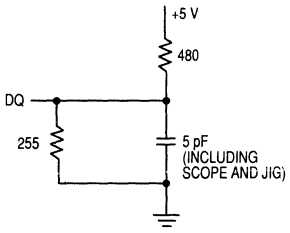
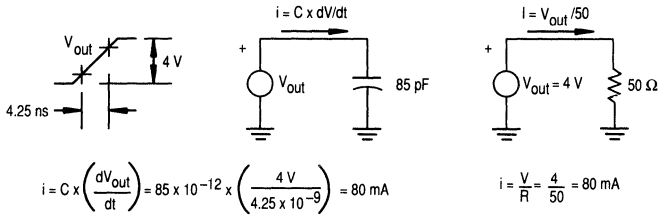


Figure 1B

CAPACITIVE LOAD EQUIVALENT RESISTANCE



$$i = C \times \left(\frac{dV_{out}}{dt}\right) = 85 \times 10^{-12} \times \left(\frac{4\ V}{4.25 \times 10^{-9}}\right) = 80\ mA$$

$$i = \frac{V}{R} = \frac{4}{50} = 80\ mA$$

85 pF load is equivalent to a 50 Ω termination

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AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, V_{CCQ} = 5.0 V or 3.3 V ± 10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

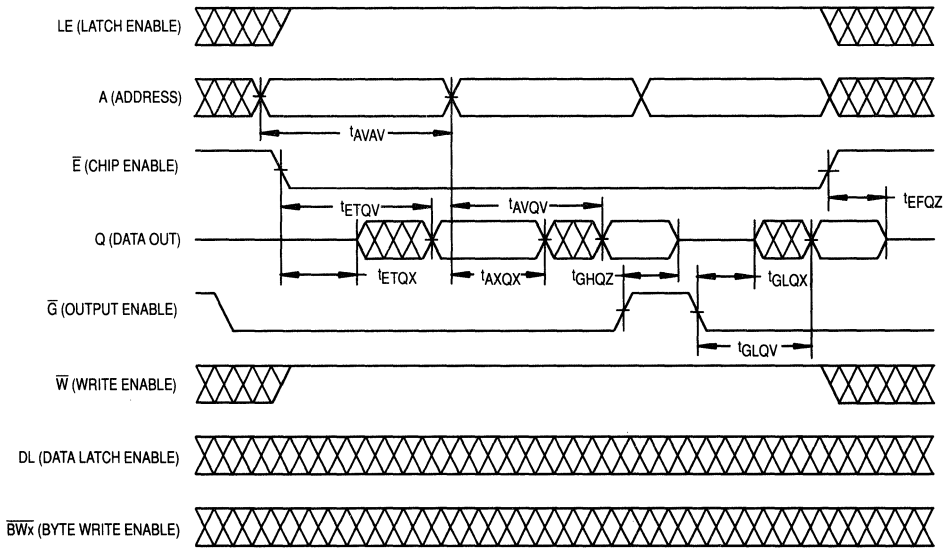
ASYNCHRONOUS READ CYCLE TIMING (See Notes 1, 2, 3, and 4)

Parameter	Symbol	MCM62995–17		MCM62995–20		MCM62995–25		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Times	t_{AVAV}	17	—	20	—	25	—	ns	5
Access Times:								ns	
Address Valid to Output Valid	t_{AVQV}	—	17	—	20	—	25		
E, $\overline{E}$ "True" to Output Valid	t_{ETQV}	—	17	—	20	—	25		6
Output Enable Low to Output Valid	t_{GLQV}	—	6	—	8	—	10		
Output Hold from Address Change	t_{AXQX}	4	—	4	—	4	—	ns	
Output Buffer Control:								ns	
E, $\overline{E}$ "True" to Output Active	t_{ETQX}	2	—	2	—	2	—		7
$\overline{G}$ Low to Output Active	t_{GLQX}	2	—	2	—	2	—		7
E, $\overline{E}$ "False" to Output High-Z	t_{EFQZ}	2	9	2	9	2	10		7
$\overline{G}$ High to Output High-Z	t_{GHQZ}	2	6	2	9	2	10		7
Power Up Time	t_{ETICCH}	0	—	0	—	0	—	ns	

NOTES:
1. LE and DL are equal to V_{IH} for all asynchronous cycles.
2. Write enable is equal to V_{IH} for all read cycles.
3. ET is defined by $\overline{E}$ going low coincident with or after E goes high, or E going high coincident with or after $\overline{E}$ goes low.
4. EF is defined by $\overline{E}$ going high or E going low.
5. All read cycle timing is referenced from the last valid address to the first transitioning address.
6. Addresses valid prior to or coincident with $\overline{E}$ going low or E going high.
7. Transition is measured ±500 mV from steady-state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{EFQZ} is less than t_{ETQX} and t_{GHQZ} for a given device.

9

ASYNCHRONOUS READ CYCLE



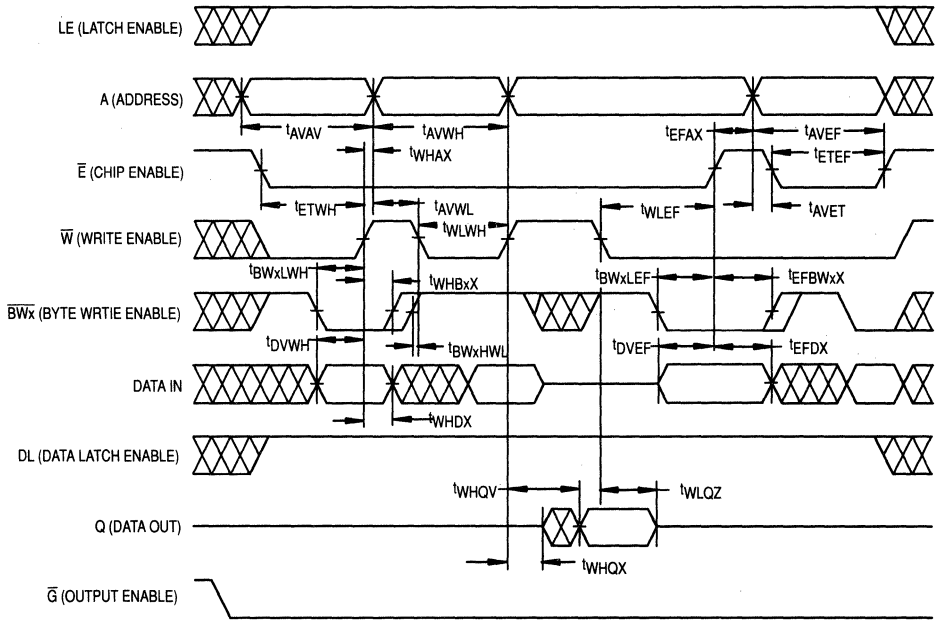
ASYNCHRONOUS WRITE CYCLE TIMING (See Notes 1, 2, 3, 4, and 5)

Parameter	Symbol	MCM62995–17		MCM62995–20		MCM62995–25		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Times	t_{AVAV}	17	—	20	—	25	—	ns	6
Setup Times:								ns	
Address Valid to End of Write	t_{AVWH}	13	—	15	—	20	—		
Address Valid to End of Write	t_{AVEF}	13	—	15	—	20	—		
Address Valid to $\overline{W}$ Low	t_{AVWL}	0	—	0	—	0	—		
Address Valid to E, $\overline{E}$ "True"	t_{AVET}	0	—	0	—	0	—		
Data Valid to $\overline{W}$ High	t_{DVWH}	6	—	8	—	10	—		
Data Valid to E or $\overline{E}$ "False"	t_{DVEF}	6	—	8	—	10	—		
Byte Write Low to $\overline{W}$ High	t_{BWxLWH}	6	—	8	—	10	—		
Byte Write Low to E, $\overline{E}$ "False"	t_{BWxLEF}	6	—	8	—	10	—		
Byte Write High to $\overline{W}$ Low (Abort)	t_{BWxHWL}	0	—	0	—	0	—		2
Hold Times:								ns	
$\overline{W}$ High to Address Invalid	t_{WHAX}	0	—	0	—	0	—		
E, $\overline{E}$ "False" to Address Invalid	t_{EFAX}	1	—	1	—	1	—		
$\overline{W}$ High to Data Invalid	t_{WHDX}	0	—	0	—	0	—		
E, $\overline{E}$ "False" to Data Invalid	t_{EFDX}	0	—	0	—	0	—		
$\overline{W}$ High to Byte Write Invalid	t_{WHBWxX}	2	—	2	—	2	—		
E, $\overline{E}$ "False" to Byte Write Invalid	t_{EFBWxX}	2	—	2	—	2	—		
Write Pulse Width:								ns	
Write Pulse Width	t_{WLWH}	13	—	15	—	20	—		
Write Pulse Width	t_{WLEF}	13	—	15	—	20	—		7
Enable to End of Write	t_{ETWH}	13	—	15	—	20	—		8
Enable to End of Write	t_{ETEF}	13	—	15	—	20	—		7, 8
Output Buffer Control:								ns	
$\overline{W}$ High to Output Valid	t_{WHQV}	18	—	20	—	25	—		
$\overline{W}$ High to Output Active	t_{WHQX}	5	—	5	—	5	—		9
$\overline{W}$ Low to Output High-Z	t_{WLQZ}	0	9	0	9	0	10		9, 10

NOTES:

1. LE and DL are equal to V_{IH} for all asynchronous cycles.
2. A write occurs during the overlap of ET, $\overline{W}$ low, and $\overline{BWx}$ low. An aborted write occurs when $\overline{BWx}$ remains at V_{IH} while $\overline{W}$ is low and satisfies the required setup and hold times..
3. Write must be equal to V_{IH} for all address transitions.
4. ET is defined by $\overline{E}$ going low coincident with or after E goes high, or E going high coincident with or after $\overline{E}$ goes low.
5. EF is defined by $\overline{E}$ going high or E going low.
6. All write cycle timing is referenced from the last valid address to the first transitioning address.
7. If E or $\overline{E}$ goes false coincident with or before $\overline{W}$ goes high, the output will remain in a high-impedance state.
8. If E and $\overline{E}$ goes true coincident with or after $\overline{W}$ goes low, the output will remain in a high-impedance state.
9. Transition is measured ±500 mV from steady-state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{WLQZ} is less than t_{WHQX} for a given device.
10. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will reamin in a high-impedance state.

ASYNCHRONOUS WRITE CYCLE



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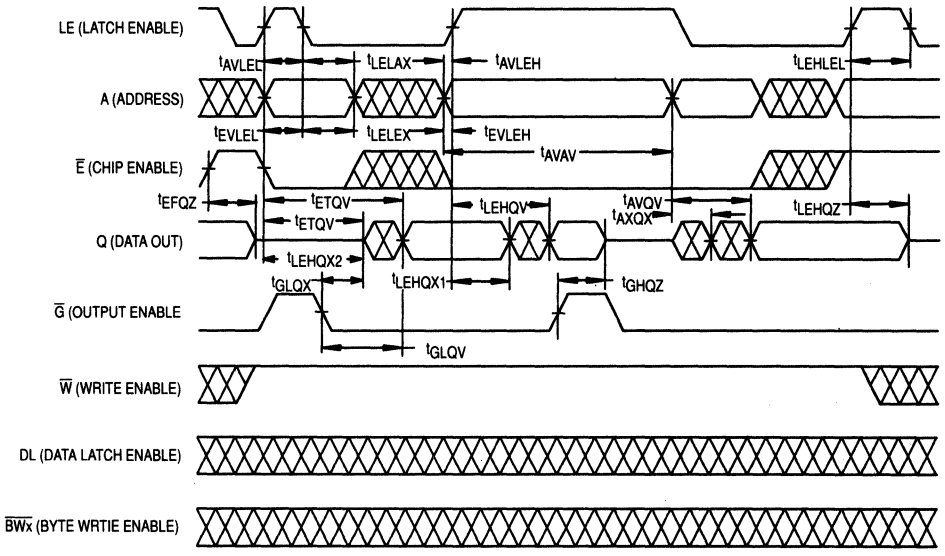
LATCHED READ CYCLE TIMING (See Notes 1, 2, 3, and 4)

Parameter	Symbol	MCM62995–17		MCM62995–20		MCM62995–25		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Times	t_{AVAV}	17	—	20	—	25	—	ns	5
Access Times:								ns	
Address Valid to Output Valid	t_{AVQV}	—	17	—	20	—	25		
E, $\overline{E}$ "True" to Output Valid	t_{ETQV}	—	17	—	20	—	25		5
LE High to Output Valid	t_{LEHQV}	—	17	—	20	—	25		6
Output Enable Low to Output Valid	t_{GLQV}	—	6	—	8	—	10		
Setup Times:								ns	
Address Valid to LE Low	t_{AVLEL}	2	—	2	—	2	—		6
E, $\overline{E}$ "Valid" to LE Low	t_{EVLEL}	2	—	2	—	2	—		6
Address Valid to LE High	t_{AVLEH}	0	—	0	—	0	—		
E, $\overline{E}$ "Valid" to LE High	t_{EVLEH}	0	—	0	—	0	—		
Hold Times:								ns	
LE Low to Address Invalid	t_{LELAX}	3	—	3	—	3	—		6
LE Low to E, $\overline{E}$ "Invalid"	t_{LELEX}	3	—	3	—	3	—		6
Output Hold:								ns	
Address Invalid to Output Invalid	t_{AXQX}	4	—	4	—	4	—		
LE High to Output Invalid	t_{LEHQX1}	4	—	4	—	4	—		
Latch Enable High Pulse Width	t_{LEHLEL}	5	—	5	—	5	—	ns	
Output Buffer Control:								ns	
E, $\overline{E}$ "True" to Output Active	t_{ETQX}	2	—	2	—	2	—		7
$\overline{G}$ Low to Output Active	t_{GLQX}	2	—	2	—	2	—		7
LE High to Output Active	t_{LEHQX2}	2	—	2	—	2	—		7
E, $\overline{E}$ "False" to Output High-Z	t_{EFQZ}	2	9	2	9	2	10		7
LE High to Output High-Z	t_{LEHQZ}	2	9	2	9	2	10		7
$\overline{G}$ High to Output High-Z	t_{GHQZ}	2	6	2	8	2	10		7

NOTES:
1. Write enable is equal to V_{IH} for all read cycles.
2. All read cycle timing is referenced from the last valid address to the first transitioning address.
3. ET is defined by $\overline{E}$ going low coincident with or after E goes high, or E going high coincident with or after $\overline{E}$ goes low.
4. EF is defined by $\overline{E}$ going high or E going low.
5. Addresses valid prior to or coincident with $\overline{E}$ going low and E going high.
6. All latched inputs must meet the specified setup and hold times with stable logic levels for **ALL** falling edges of latch enable (LE) and data latch enable (DL).
7. Transition is measured ± 500 mV from steady-state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{EFQZ} is less than t_{ETQX} and t_{LEHQZ} is less than t_{LEHQX2} and t_{GHQZ} is less than t_{GLQX} for a given device.

LATCHED READ CYCLES



9

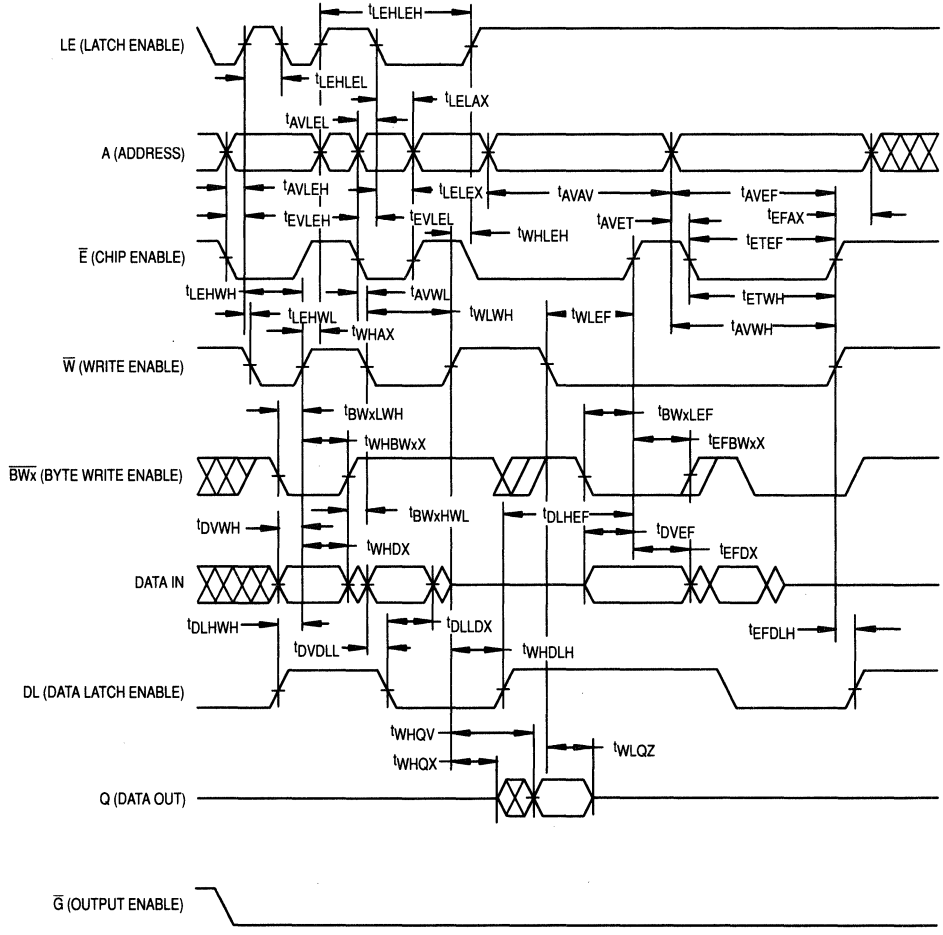
LATCHED WRITE CYCLE TIMING (See Notes 1, 2, 3, and 4)

Parameter	Symbol	MCM62995–17		MCM62995–20		MCM62995–25		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Times:								ns	
Address Valid to Address Valid	t_{AVAV}	17	—	20	—	25	—		5
LE High to LE High	t_{LEHLEH}	17	—	20	—	25	—		5
Setup Times:								ns	
Address Valid to End of Write	t_{AVWH}	13	—	15	—	20	—		
Address Valid to End of Write	t_{AVEF}	13	—	15	—	20	—		
E, $\overline{E}$ "Valid" to LE Low	t_{EVLEL}	2	—	2	—	2	—		
Address Valid to LE Low	t_{AVLEL}	2	—	2	—	2	—		
E, $\overline{E}$ "Valid" to LE High	t_{EVLEH}	0	—	0	—	0	—		
Address Valid to LE High	t_{AVLEH}	0	—	0	—	0	—		
LE High to $\overline{W}$ Low	t_{LEHWL}	0	—	0	—	0	—		
Address Valid to $\overline{W}$ Low	t_{AVWL}	0	—	0	—	0	—		
Address Valid to E, $\overline{E}$ "True"	t_{AVET}	0	—	0	—	0	—		
Data Valid to DL Low	t_{DVDLL}	1	—	1	—	1	—		
Data Valid to $\overline{W}$ High	t_{DVWH}	6	—	8	—	10	—		
Data Valid to E or $\overline{E}$ "False"	t_{DVEF}	6	—	8	—	10	—		
DL High to $\overline{W}$ High	t_{DLHWH}	6	—	8	—	10	—		
DL High to E, $\overline{E}$ "False"	t_{DLHEF}	6	—	8	—	10	—		
Byte Write Low to $\overline{W}$ High	t_{BWxLWH}	6	—	8	—	10	—		
Byte Write Low to E, $\overline{E}$ "False"	t_{BWxLEF}	6	—	8	—	10	—		
Byte Write High to $\overline{W}$ Low (Abort)	t_{BWxHWL}	0	—	0	—	0	—		1
Hold Times:								ns	
LE Low to E, $\overline{E}$ "Invalid"	t_{LELEX}	3	—	3	—	3	—		5
LE Low to Address Invalid	t_{LELAX}	3	—	3	—	3	—		5
DL Low to Data Invalid	t_{DLLDX}	3	—	3	—	3	—		
$\overline{W}$ High to Address Invalid	t_{WHAX}	0	—	0	—	0	—		
E, $\overline{E}$ "False" to Address Invalid	t_{EFAX}	1	—	1	—	1	—		
$\overline{W}$ High to Data Invalid	t_{WHDX}	0	—	0	—	0	—		
E, $\overline{E}$ "False" to Data Invalid	t_{EFDX}	0	—	0	—	0	—		
$\overline{W}$ High to DL High	t_{WHDLH}	0	—	0	—	0	—		
E, $\overline{E}$ "False" to DL High	t_{EFDLH}	0	—	0	—	0	—		
$\overline{W}$ High to Byte Write Invalid	t_{WHBWxX}	2	—	2	—	2	—		
E, $\overline{E}$ "False" to Byte Write Invalid	t_{EFBWxX}	2	—	2	—	2	—		
$\overline{W}$ High to LE High	t_{WHLEH}	0	—	0	—	0	—		
Write Pulse Width:								ns	
LE High to $\overline{W}$ High	t_{LEHWH}	13	—	15	—	20	—		6
Write Pulse Width	t_{WLWH}	13	—	15	—	20	—		
Write Pulse Width	t_{WLEF}	13	—	15	—	20	—		7
Enable to End of Write	t_{ETWH}	13	—	15	—	20	—		8
Enable to End of Write	t_{ETEF}	13	—	15	—	20	—		7, 8
Latch Enable High Pulse Width	t_{LEHLEL}	5	—	5	—	5	—	ns	
Output Buffer Control:								ns	
$\overline{W}$ High to Output Valid	t_{WHQV}	17	—	20	—	25	—		
$\overline{W}$ High to Output Active	t_{WHQX}	5	—	5	—	5	—		9
$\overline{W}$ Low to Output High-Z	t_{WLQZ}	0	9	0	9	0	10		9, 10

NOTES:

1. A write occurs during the overlap of ET, $\overline{W}$ low and $\overline{BWx}$ low. An aborted write occurs when $\overline{BWx}$ remains at V_{IH} while $\overline{W}$ is low and meets the required setup and hold times.
2. Write must be equal to V_{IH} for all address transitions.
3. ET is defined by $\overline{E}$ going low coincident with or after E goes high, or E going high coincident with or after $\overline{E}$ goes low.
4. EF is defined by $\overline{E}$ going high or E going low.
5. All write cycle timing is referenced from the last valid address to the first transitioning address.
6. All latched inputs must meet the specified setup and hold times with stable logic levels for **ALL** falling edges of latch enable (LE) and data latch enable (DL).
7. If E or $\overline{E}$ goes false coincident with or before $\overline{W}$ goes high, the output will remain in a high-impedance state.
8. If E and $\overline{E}$ goes true coincident with or after $\overline{W}$ goes low, the output will remain in a high-impedance state.
9. Transition is measured ±500 mV from steady-state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{WLQZ} is less than t_{WHQX} for a given device.
10. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will reamin in a high-impedance state.

LATCHED WRITE CYCLES



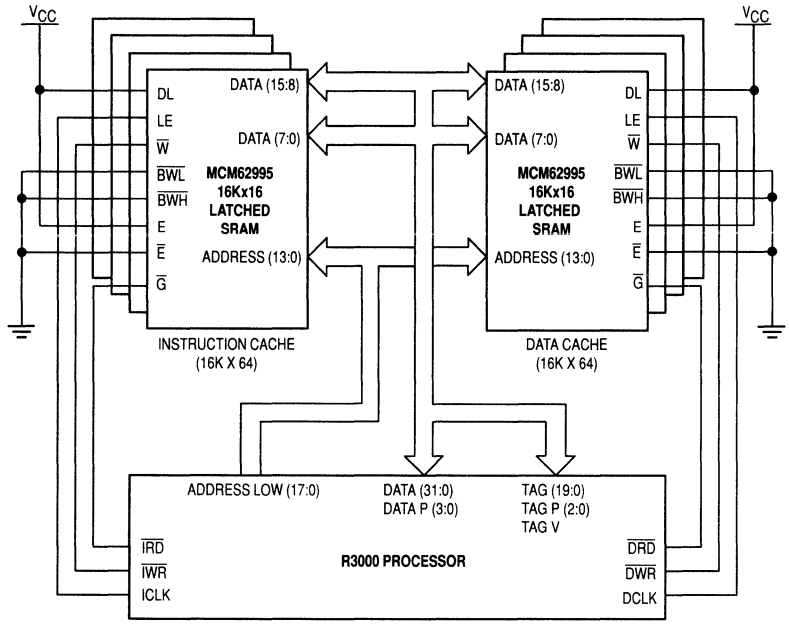


Figure 2. R3000 Application Example with 128K Byte Segregated Instruction/Data Cache Using Eight Motorola MCM62995 Latched SRAMs

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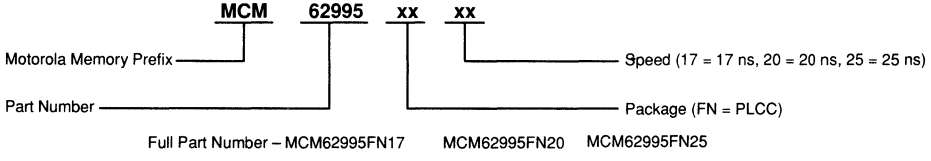
ORDERING INFORMATION
(Order by Full Part Number)



MOS EEPROM 10

ELECTRICALLY ERASABLE PROGRAMMABLE READ ONLY MEMORY

Density	Organi-zation	Motorola Part Number	Address Access Time (ns Max)	Operating Current (mA Max)	Pin Count	Packaging
2K	256Kx8	MCM2814P	3.5 µs	10	8	(P)DIP

MCM2814

256x8 BIT SERIAL EEPROM

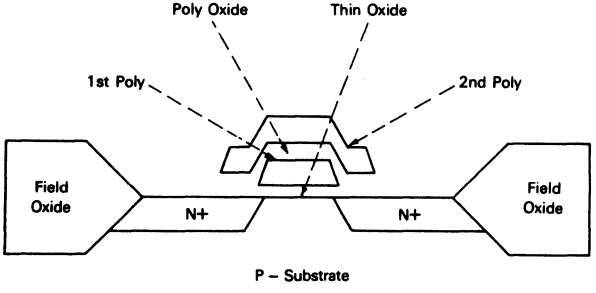
The MCM2814 is a 2048-bit serial electrically erasable PROM. Designed for handling data in applications requiring both non-volatile memory and in-system information updates.

The MCM2814 is fabricated in an 8-pin DIL package using floating-gate HCMOS EEPROM technology.

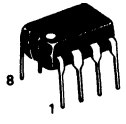
Features:

- 2048 bits organised as 256 bytes.
- Byte programmable.
- 3 - 6V supply during read operations.
- On-chip Programming Voltage Generator.
- Two programming modes: two-wire serial access, M-bus/four-wire serial access SPI.
- Data protection of 1/4, 1/2, or 3/4 array with EEPROM bits.
- Simultaneous programming of 1 to 4 bytes.
- Automatic byte address increment in Read mode.
- Chip selection with separate pin.
- Single 4.5V to 6V supply during programming.
- Digital filtering on Clock and Data inputs.
- Bit program operation: no byte erase necessary.
- Data protection after Reset.
- Write/Erase endurance:10000 cycles over 0 to 70 DEG C.
- Typically 100,000 W/E cycles at ambient temperatures.
- Data retention: 10 years

FETMOS
(Floating-Gate Electron Tunnelling MOS)

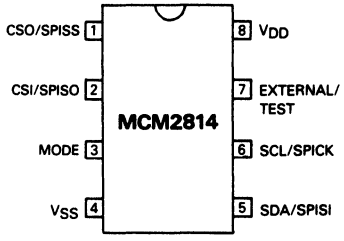


HCMOS
(FLOATING-GATE TECHNOLOGY)
256 x 8 BIT ELECTRICALLY ERASABLE PROGRAMMABLE READ ONLY MEMORY



P SUFFIX
PLASTIC PACKAGE
CASE 626-04

PIN ASSIGNMENT



PIN DESCRIPTION

V_{DD}:	Power Supply
V_{SS}:	Ground (Ref)
External/ Test	Connected to on-chip Voltage Multiplier output
Mode =	0 M-bus
CS0	Chip Select (Hardwired)
CS1	Chip Select (Hardwired)
SDA	Serial Date I/O
SCL	Serial Clock Input
Mode =	1 SPI
SPISS	Slave Select Input
SPISO	Serial Data Output
SPISI	Serial Data Input
SPICK	Serial Clock Input

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SECTION 1. PIN DESCRIPTION

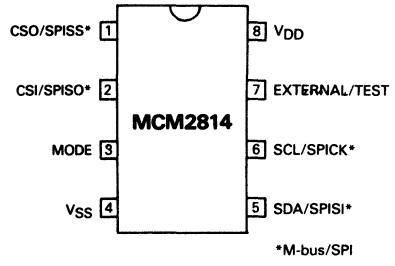

Figure 1 Pinout

1.1 V_{SS}/V_{DD} (Pins 4/8)

V_{DD} and V_{SS} are used to power the circuit. In read mode this supply voltage must be comprised in the V_{DDR} range. (See **5.2 Electrical Characteristics**). In program mode this supply range is limited to V_{DDP}.

1.2 External/Test (Pin 7)

This pin is used for testing the on-chip voltage multiplier that generates the programming voltage required for a program operation, and should be left open for 5 Volt only operation.
An external capacitor (Low leakage) on this pin might have a positive impact on the programming endurance, as the V_{PP} rise time will be increased.
Recommendations will be issued after the characterisation. As this on-chip generator has a high impedance, an external supply can be connected to this pin. This also allows to block any inadvertant programming by maintaining this pin at V_{DD}.

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1.3 Mode (Pin 3)

This pin is used to select one of two modes of operation: M-bus mode at the low logic level or SPI mode at high level.
This pin is usually hardwired to V_{SS} or V_{DD}. It should only be changed if the circuit is internally in a standby state.
This pin is high impedance when V_{DD} is at V_{SS} level.

1.4 CS1 / SPISO (Pin 2)

In M-bus mode, this pin is used for selecting multiple identical chips on the same serial bus. The chip address is formed by 5 bits predefined for this chip, followed by 2 additional chip select bits. These last two bits must correspond to the CS1 / CS0 code for proper chip selection. Up to four MCM 2814 can be connected on the same SCL and SDA lines. (See **Figure 4**).

In SPI mode this pin is a push-pull slave data output (SPISO). It will shift-out byte addresses and data as described in Section 4.
This pin is usually connected to the data input pin of a SPI master (MISO).
This pin can not be pulled higher than 0.5 V above V_{DD}, even if V_{DD} is at V_{SS} level.

1.5 CSO / SPISS (Pin 1)

In M-bus mode this pin is used in conjunction with CS1 for chip selection. (See **above**).

In SPI mode this pin is a Slave Select input. In this mode the serial access is deselected when the SPISS input is high, and the SPISO data output pin is forced high impedance. Multiple chips using the same SPICK, SPISI and SPISO lines, can be selected via this pin as described in Figure 10.
After powering up the device, a falling edge of the SPISS line is required to start the SPI serial access.

This pin is high impedance when V_{DD} is at V_{SS} level.

1.6 SCL / SPICK (Pin 6)

The serial clock is supplied on pin SCL / SPICK. This pin is an input only, therefore the chip can only operate as a slave under the control of a serial bus master.
The clock input rising edge is used to shift in data present on the SDA/SPISI pin, and the falling edge is used to shift out data on the SDA or SPISO pin.

This pin is high impedance when V_{DD} is at V_{SS} level.

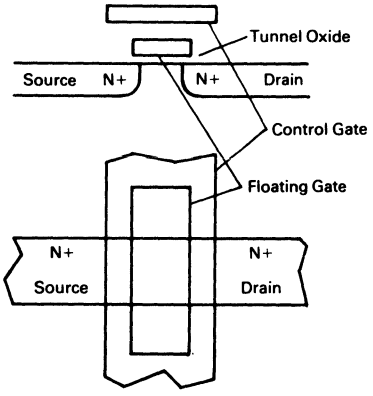
1.7 SDA / SPISI (Pin 5)

In M-bus mode, SDA pin is used to transmit data serially in the memory (Receiver) or from the memory (Transmitter). Data transmitted via this pin includes chip addresses, byte addresses, byte data, Read/Write and acknowledge bits. When SDA is in output, it operates as a pull-down only device (Open-drain). The protocol of this transmission is described in Figures 5 and 6.

In SPI mode, this pin is a Slave data Input (SPISI) only and is used to receive opcodes, byte addresses and byte data. It is usually connected to the data output pin of a SPI master. (MOSI).

This pin is high impedance when V_{DD} is at V_{SS} level.

SECTION 2. EEPROM



	CG	D	S
READ	0V	VDD	0V
PROG 1	0V	VPP	OPEN
PROG 0	VPP	0V	0V

Figure 2 EEPROM Transistor

256 Bytes of EEPROM memory are implemented in a floating gate double poly-silicon process. A Byte Address register is used to select one of the bytes. Three basic state of operation can be distinguished :

- Standby state.
- Read state
- Program state

2.1 EEPROM Operation

2.1.1 Standby State

In this state, neither a programming, nor a serial transmission occurs, and the power consumption is minimum. (See **3.4.1** and **4.5**).

2.1.2 Read State

In read state the data of the selected byte is transferred from the memory array to the data shift register used for the serial transmission. This state is active during a serial transmission.

2.1.3 Program State

In this state, a programming voltage higher than V_{DD} is necessary. This voltage is generated by the on-chip voltage multiplier or can be supplied externally. During programming V_{DD} must be within the V_{DDP} range. (See **5.2**).

In M-bus mode, the programming starts at the end of a write command, when a STOP or a new START condition occurs. The programming is enabled at this time, as well as the on-chip voltage multiplier. If there is a capacitive load on the V_{PP} pin, the V_{PP} rise time should be added to the minimum program time t_{PROG}.

In SPI mode, programming could start when a write serial transmission is ended with an SPISS rising edge. Actual programming will only happen if enabled by a V_{PP} enable serial command. This command can be transmitted before or after the write sequence.

2.2 EEPROM Data Protection

Some circuitry has been included to prevent unwanted modification of EEPROM data, and is described below. However, a noisy serial link is very often the cause of bad data or data written to the wrong address. Besides measures to reduce this noise on the board, the serial clock and data inputs (SCL/SDA) have Schmitt triggers and digital filters to reject some of the noise.

2.2.1 Power Up Reset

Immediately after power is applied, programming is inhibited to prevent EEPROM data loss during the system power up.

In both modes this condition is removed when a READ is performed.
In M-bus mode, this condition is removed by reading the data in any byte address using the normal read sequence.

In SPI mode, it is sufficient to send the READ opcode before a new V_{PP} enable command and the write sequence.

At Reset the following circuitry is initialised:

- The circuit is in standby state.
- In M-bus mode, it is waiting for a start condition.
- In SPI mode, it is waiting for a high to low SPISS transition.
- The data outputs are high impedance (SDA, SPISO).
- The programming is disabled.
- The on-chip Vpp generator is off.

2.2.2 Programming Voltage Enable

In SPI mode only, an internal programming voltage enable flip-flop can be set or cleared with two separate opcodes, thus reducing the risk of unwanted EEPROM programming.

2.2.3 Array Write Protect

In both modes, byte address 255 ($FF) contains EEPROM bits with a special function. When one or two bits of this address are programmed at once, the programming of EEPROM sections is inhibited according to the following table:

Data at ADDR $FF		Protected Addresses	No. of Bytes Protected
XXXX	00XX	No Write Prot.	-
XXXX	01XX	$C0 – $FB	60
XXXX	10XX	$80 – $FB	124
XXXX	11XX	$40 – $FB	188

X = Don't care

Table 1 EEPROM Write Protect

This protection is reversible as address 255 ($FF) can be modified at any time.

2.3 EEPROM Properties

NO ERASE : Unlike most EEPROM's it is not necessary to erase a byte before writing new data to it.
The program operation takes t_{PROG} and must be externally timed.

CUMULATIVE : As the programming operation is under external control, it can be done at once or at various time frames as long as the total programming time exceeds the specified minimum t_{PROG} value.
t_{PROG} is defined with V_{PP} at its programming level.

SELF LIMITING : Excess pogramming has no positive effect, as programmed EEPROM thresholds will asymptotically reach their nominal values. Programming durations above the recommended t_{PROG} have negative impacts on the EEPROM programming endurance.

2.4 EEPROM Reliability

Reliability figures are statistical in nature. Therefore no minimum or maximum specifications can be applied. The result of reliability tests will be published instead. These tests are conducted on a regular basis during the production life of a circuit and reports are available upon request.

2.4.1 Data Retention

Typical data retention should exceed 10 years for the specified operating temperature range. Data retention is usually tested with the device under bias, but without accessing the EEPROM array.

2.4.2 Read Stress

Unlike some non-volatile memories, there should be no disturbance of the stored data under continuous read of EEPROM bytes. The life limit under continuous read condition should therefore be similar to the normal operating life of the device.

2.4.3 Program Endurance

As for all EEPROM'S, there is a wearout mechanism associated with the programming mechanism on the non volatile memory. More than 10,000 programming cycles should be possible per memory bit, additionally 100,000 cycles is typical for the specified temperature range. A programming cycle is defined as a 0 to 1 to 0 programming. Unlike most EEPROM'S where the whole byte is erased before being re-programmed, if just one bit is modified in a byte, only this bit will see the programming stress.
Some endurance experiments have shown that the number of programming cycles can be increased if the Vpp rise time is increased. This can be achieved with an external capacitor on Vpp when the on-chip Vpp generator is used. In SPI mode, the Vpp should be enabled after the write command has been transmitted. If an external Vpp is provided, it should be ramped up only after the write command is transmitted. In this case, a Vpp above the maximum value also has a negative impact on the endurance.

2.5 Vpp Voltage Multiplier

In M-bus mode, the on-chip V_{PP} generator is turned on or off automatically during a program sequence.

In SPI mode, it is switched on only after a serial V_{PP} enable command has been issued, independently of write or read commands.

SECTION 3. M-BUS OPERATING MODE

The MODE pin can be hardwired to V_{DD} or V_{SS} to select two different modes of operation. Differences are at the serial transmission level and in the EEPROM operation. They are called M-bus mode and SPI mode.

3.1 M-bus Mode

Only two wires are needed to control the device operation. The serial transmission of this mode is similar to the IIC (*) serial communication standard. It features :

- Up to 4 identical chips on the same 2 wire bus.
- CS1 / CS0 pins for chip selection.
- SCL clock line, input only.
- SDA line used as Input and Output.
- Data acknowledge bit generated.
- Auto programming after reception of new data.
- Programming time under external control.
- Write inhibit after reset.

*IIC is a trademark of Philips

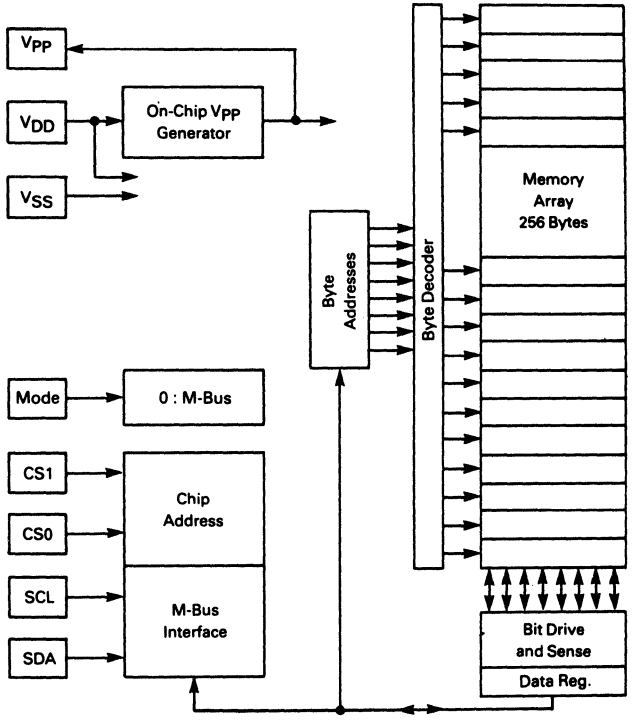


Figure 3 M-bus Block Diagram

3.2 Lexicon

This lexicon will describe some terms used in this serial interface description.

MASTER : The device that initiates the serial transmission is designated as master. In general, it is the device generating the clock. This memory can never function as a master.

SLAVE : This memory always operates as a slave.

TRANSMITTER : The device with its SDA pin in output is a data transmitter. In the case of multiple devices in output, the device sending a low level will win due to the Open-Drain connection.

RECEIVER : A device that has been properly selected by a chip address followed by a write bit is a receiver, and will

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shift data present on the SDA pin in internal registers.

MSB : The Most Significant Bit is the first bit transmitted and received.

START CONDITION : The start condition is defined as a 1 to 0 transition of SDA when SCL is high. The first byte of data following a start condition includes the chip address followed by the R/W bit. All devices connected on the same bus receive this data to check if they are addressed.

STOP CONDITION : The stop condition is defined as a 0 to 1 transition of SDA when SCL is high. In this circuit, the stop condition is never mandatory. An EEPROM programming can be initiated by the STOP or also by any following START condition.
A STOP after a serial read sequence will put the device in standby state.

CHIP ADDRESS : The first byte transmitted after a START contains the chip address followed by the Read/Write bit. The 7 bit chip address is formed of 5 fixed bits followed by 2 chip select bits.
Fixed bits are 1010X for this device (X is a don't care bit).

The 2 chip select bits must correspond to the 2 chip select inputs for proper chip selection. By this means, up to 4 identical chips can be connected on the same SDA / SCL lines, in order to form a memory bank of up to 8 KBits.

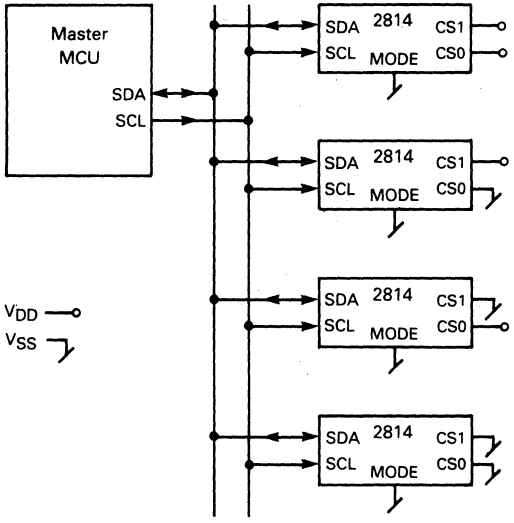
READ/WRITE BIT : The 8th bit transmitted by the master after the 7 bit chip address will indicate the direction of transfer for the next bytes. (Until a new start or stop). If low, the following bytes are transmitted by the master. If high, the following bytes are transmitted by the MCM 2814.

BYTE ADDRESS : The first byte of data received by the memory after the chip address, will be latched in the byte address register and is used to select one of the 256 EEPROM bytes.

ACKNOWLEDGE BIT : This bit is sent by the selected receiver on the data line after a byte reception. Due to the open drain structure, a valid acknowledge bit corresponds to a low level. While operating as a transmitter, sending a sequence of data bits, this device will check the acknowledge bit generated by the master. The absence of this bit will stop the transmission of data.

3.3 Chip Selection

The 2 chip select bits transmitted in the chip address must match the status of CS1 and CS0 inputs.



Pin Status			Chip Address Transmitted
Mode	CS1	CS0	
0	1	1	1010 X11
0	1	0	1010 X10
0	0	1	1010 X01
0	0	0	1010 X00

X = Don't care

Figure 4 M-bus Chip Selection

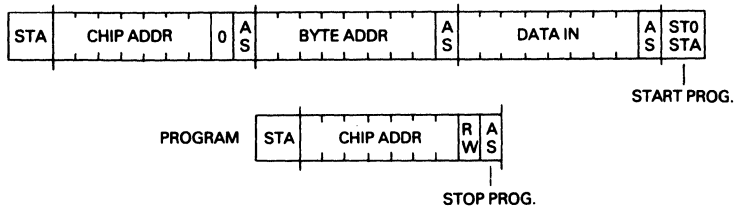
3.4 Protocol

At the protocol level, the transmission of data is defined in the form of sequences of Start (STA), Stop (STO) conditions, and bytes followed by acknowledge bits.

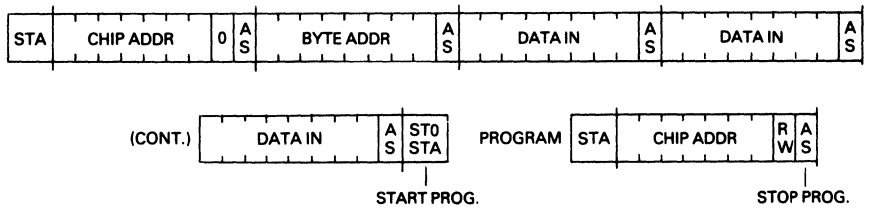
3.4.1 Standby State

When no serial transmission and no programming are made, the circuit is in standby. A STOP condition following a read sequence or a write byte address sequence (without data write), will put the circuit in standby. A new START condition will wake up the device, to get the chip address. If the chip address is not valid, the device will return in standby.
The power consumption is minimum in standby.

Write One Byte



Write up to 4 Bytes



STA: Start Condition R/W BIT: 1 = Read/0 = Write AS: Slave Acknowledge (2814)
STO: Stop Condition INC: Increment Byte Address AM: Master Acknowledge

Figure 5 M-bus Write Protocol

3.4.2 Write Sequence

The serial write to the memory includes a serial transmission of the byte address and the data to be written. When this is completed by a stop or a new start condition, the programming sequence is initiated.

Programming is under control of the master. It is initiated by the write sequence just described, and stopped by any new valid selection of the chip.
Therefore, the t_{PROG} time is defined as the time between these two operations, and is defined by the master.

Bad chip addresses or chip addresses for other chips on the same bus do not suspend the programming.

The on-chip V_{PP} generator is automatically turned on or off when needed. If an external V_{PP} is applied, the programming voltage is only allowed into the array during the above defined t_{PROG} time.

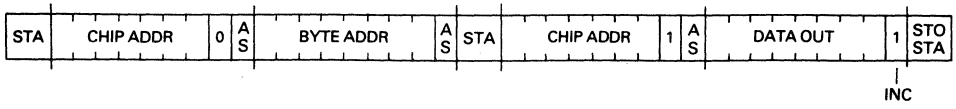
It is possible to program simultaneously up to 4 bytes, provided the 6 most significant bits of their addresses are identical. The byte address is incremented after each new data byte shifted in.

3.4.3 Read Sequence

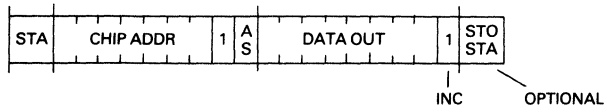
Reading data from the memory is made in two steps. First the byte address must be loaded in the byte address register. Then data can be read out of the memory. The first step is only required to define the byte address. If this address was predefined from a previous read this step can be skipped.
The byte address is automatically incremented after each data byte transmitted.
This is also valid after the last byte of a transmission. Therefore, the next read sequence without any byte address specified, will transmit data of the next byte. A read sequence will transmit data bytes of successive addresses until the absence of the acknowledge bit from the master. In this case the SDA output driver will switch off and the circuit will go to standby.

10

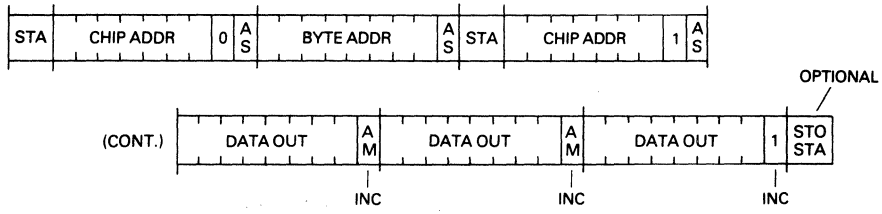
Read One Byte. (Inc. Write Byte Address)



Read One More Byte. (Byte Address Defined)



Read Many Bytes



STA: Start Condition R/W BIT: 1 = Read/0 = Write AS: Slave Acknowledge (2814)
STO: Stop Condition INC: Increment Byte Address AM: Master Acknowledge

Figure 6 M-bus Read Protocol

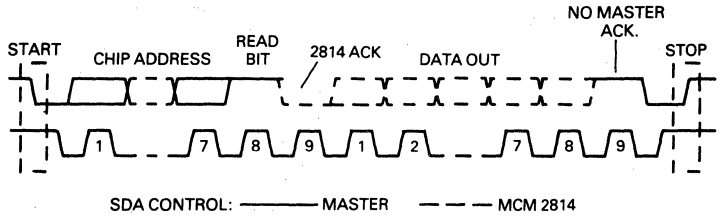


Figure 7 M-bus Read Detail

3.4.4 Signal Levels

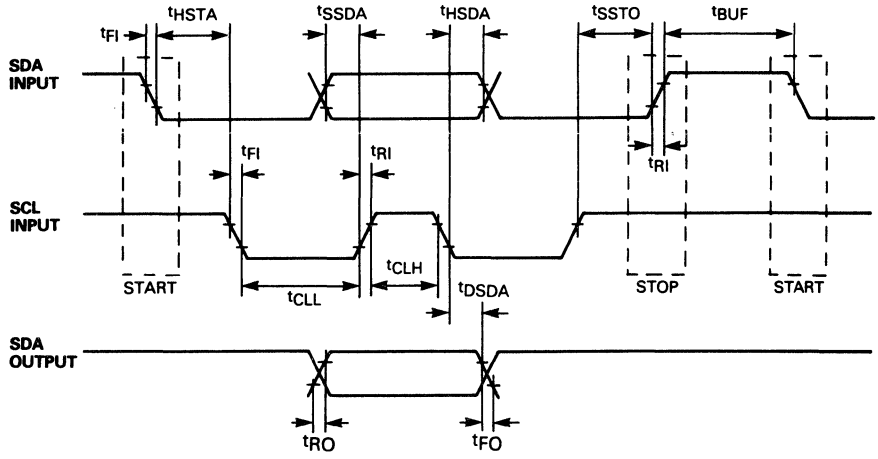


Figure 8 M-bus Timings

Electrical and switching characteristics are described in Section 5.
During a transmission, SDA line transitions must occur when SCL is low. A negative transition of SDA with SCL high is recognised as a START condition, the positive transition as a STOP condition.

The acknowledge bit is provided by the device receiving data. Therefore, during this time the data transmitter must leave the SDA line at high impedance.
As this memory has an open drain SDA output, an external pull-up resistor to V_{DD} should be included on SDA line.

SECTION 4. SPI OPERATING MODE

The serial transmission of this mode requires 4 wires to control the device operation. It features:

- Multiple chips on same 3 wire bus with separate chip select lines.
- SPISS chip selection.
- SPICK clock line, Input only.
- SPISI line used as Input only.
- SPISO line used as Output only.
- No acknowledge bit.
- Programming under control of the master via serial opcodes.
- Programming time under external control.
- Write inhibit after reset.
- Write enable/disable via serial opcodes.
- Byte address output for transparency.

This SPI mode can be used with the SPI of Motorola Microprocessor MC6805S2/S3, MC6805K2/L3/L8, MC68HC05C4 and MC68HC11.

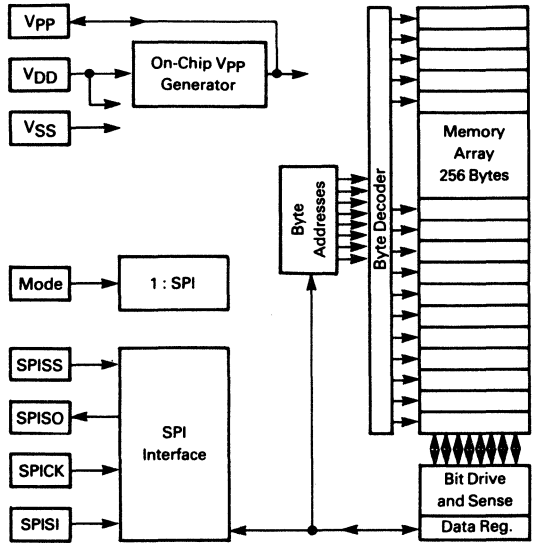


Figure 9 SPI Block Diagram

4.1 SPI Serial Interface

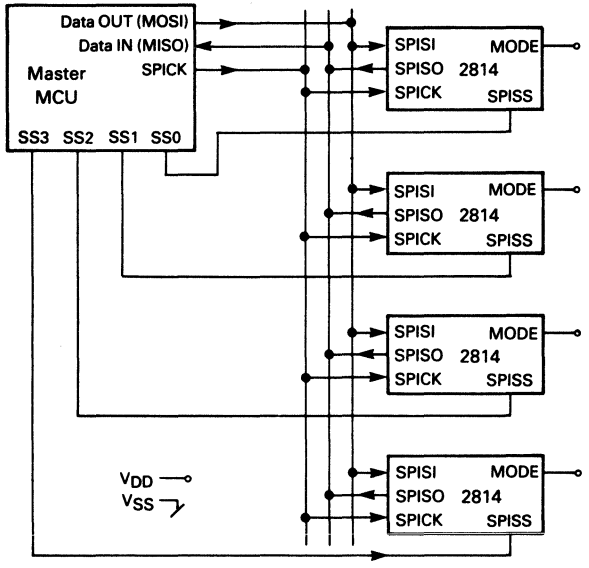


Figure 10 SPI Chip Selection

The serial interface via pins SPICL, SPISI and SPISO is compatible with the SPI standard when the MODE pin is high.

4.2 Lexicon

This lexicon will describe some terms used in this serial interface description.

MASTER : The device that generates the serial clock on SPICK is designated as master. This memory can never function as a master.

SLAVE : This memory always operate as a slave as the SPICK pin is always an input.

TRANSMITTER / RECEIVER : This device has separate pins for data transmission (SPISO) and reception (SPISI). Simultaneous data input and output can therefore occur when the chip is selected with SPISS and is clocked (SPICK).

MSB : The Most Significant Bit is the first bit transmitted and received.

CHIP SELECT : The chip is selected when pin SPISS is low. When the chip is not selected, no data will be input from pin SPISI, and output pin SPISO is high impedance.

4.3 Serial Op-Code

The first byte transmitted after the chip is selected with SPISS going low, contains the opcode that defines the operation to be performed.

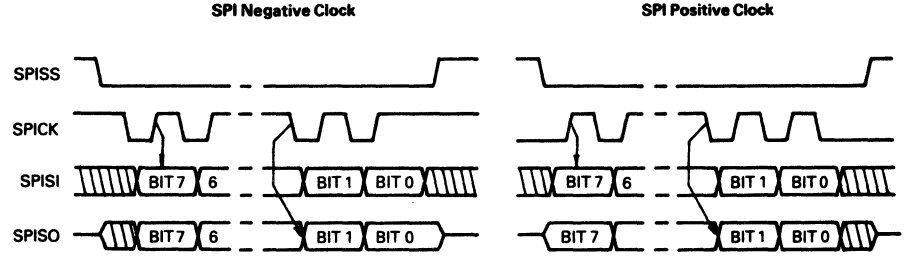
Data Transmitted	Operation
1010 0111	Read byte address followed by data.
1010 0110	Program enable. V_{PP} generator ON.
1010 0100	Program disable. V_{PP} generator OFF.
1010 0010	Write (Program) data.

Table 2 SPI Opcodes

All other codes are invalid. After an invalid code is received, no data is shifted in the MCM 2814 and the SPISO data output is high impedance until a new SPISS falling edge re-initialises the serial communication.

4.4 Protocol

The MCM2814 SPI interface accepts both a negative or positive clock.
The SPI protocol for this device defines the bytes transmitted on the SPISI and SPISO data lines for proper chip operation.



Positive Clock Edge: Shift IN
Negative Clock Edge: Data OUT

Figure 11 SPI Clock Phase and Polarity

4.5 Standby State

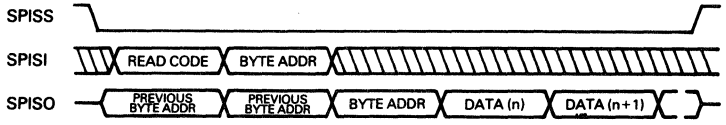
The circuit is in standby when no serial transmission takes place, when no write is waiting for the V_{PP} enable command and when the V_{PP} generator is off.
When SPISS is high, standby state will follow:

- A power up reset.
- A V_{PP} disable command.
- A Read, providing no V_{PP} enable command has been issued previously.

The power consumption is minimum in standby.

4.6 Read Sequence

Read One or More Bytes



Invalid Opcodes

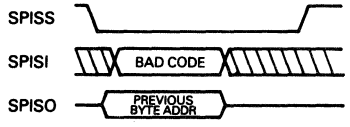
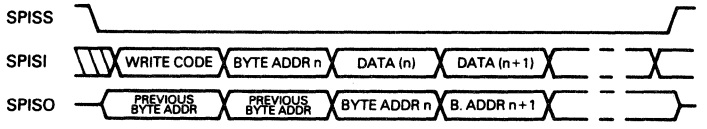


Figure 12 SPI Read

Reading the memory via the serial SPI link requires the following sequence. The SPISS line is pulled low to select the device. The read opcode is transmitted on the SPISI line followed by the byte address. When this is done, data on the SPISI line has no more influence on the memory. At the beginning of an SPI transaction, the SPISO buffer is turned on and will shift out the current byte address. This can be used for a relative addressing of the byte address. The new byte address is then transmitted followed by corresponding data. If just one byte is read, SPISS can be pulled back to the high level. It is possible to continue the read sequence, as the byte address is automatically incremented. The byte address is shifted out only once, in the beginning of a transmission.

4.7 Program Sequence

Write One to Four Bytes



Vpp Enable/Disable

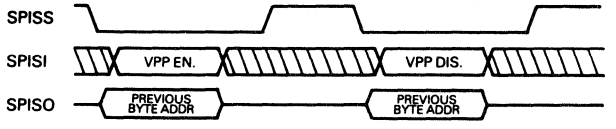


Figure 13 SPI Program

To program a byte, two separate conditions must be simultaneously present. The program must be enabled via the Vpp enable command, and a serial write must be done. The Vpp enable will also turn on the on-chip Vpp generator. At this time, the chip is obviously not in standby, even if SPISS is high. The program disable command will stop the on-chip Vpp supply and protect the EEPROM data against unwanted modifications. An external Vpp supply will also be internally enabled or disabled by this mechanism.

A write serial sequence includes an SPISS high to low transition, followed by the write code on the SPISI line. The byte address followed by the corresponding data to be written are then shifted through the SPISI pin. At the

beginning of an SPI transaction, the SPISO buffer is turned on and will shift out the current byte address. This can be used for a relative addressing of the byte to be programmed. The new byte address is also echoed for possible checking by the master. If Vpp is enabled, the programming will start after the SPISS line goes back to a high level. It is also possible to issue the Vpp enable command after the write sequence.
If the Vpp enable command is issued after the serial write, no Read or invalid code should be transmitted in between as this would clear the programming latch containing the data to be programmed.
The programming is suspended when a new chip selection with SPISS low occurs. It is then possible to send a new write command to program new data. A Vpp enable or a Read command will stop the programming.

It is possible to program simultaneously up to 4 bytes, provided the 6 most significant bits of their addresses are identical. The byte address is incremented after each new data byte shifted in.

4.8 Signal Levels

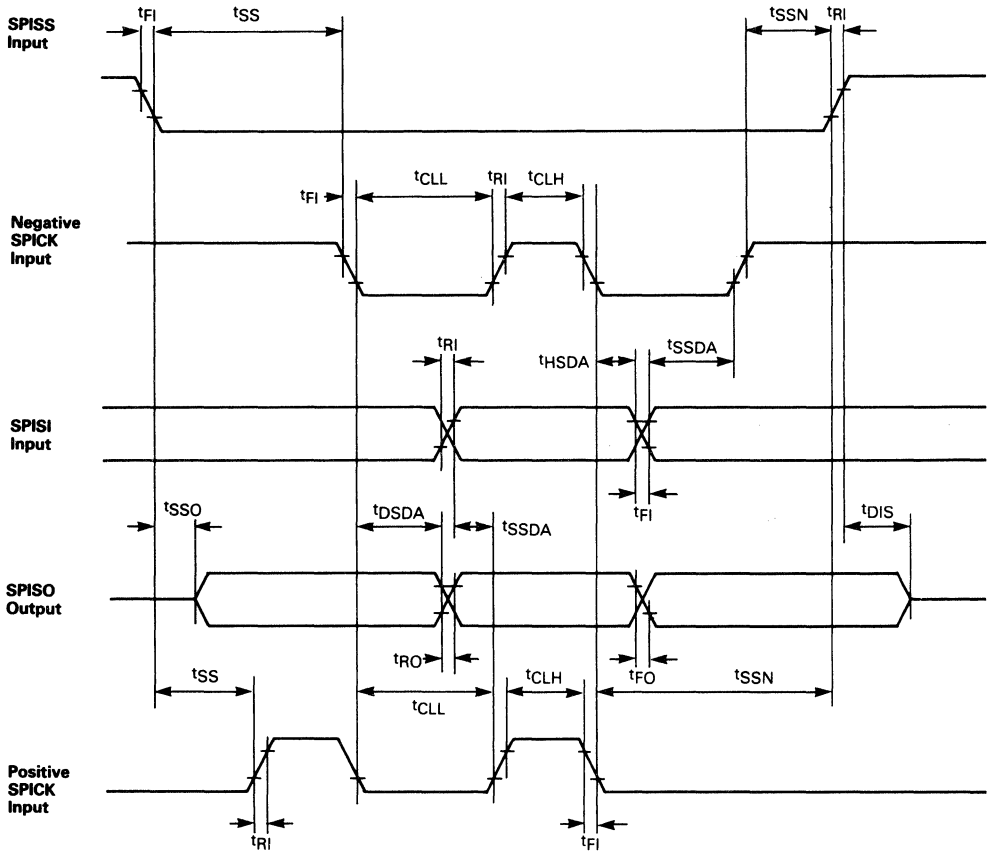


Figure 14 SPI Timings

Electrical and switching characteristics are described in **Section 5**.

SECTION 5. CHARACTERISTICS

V_{SS} = 0 V

5.1 Maximum Ratings

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	−0.3 to +7.0	Vdc
Input voltage pins 1, 3, 5, 6	V_{in}	−0.3 to +7.0	Vdc
Input voltage pin 2	V_{in}	−0.3 to V_{DD} +0.3	Vdc
Current on any Input	I_{in}	0.1	mA
Sink current SDA	ISDAL	10	mA
Sink current SPISO	ISOL	10	mA
Source current SPISO	ISOH	10	mA
Operating temperature	T_A	0 to 70	°C
Storage temperature	T_S	−55 to 125**	°C
Junction Temperature	T_j	150**	°C
Thermal resistance	Th_{ja}	200	°C/W

Stresses above those listed under 'Maximum Ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum operating conditions for extended periods may affect reliability.

**In particular, continuous high temperature application may cause leakage of stored charge in EEPROM, resulting in data loss.

5.2 Electrical Characteristics

Characteristic	Symbol	Min	Typ	Max	Unit
Supply voltage STANDBY	V_{DDS}	-	-	6.0	Vdc
Supply current STANDBY*	I_{DDS}	-	0.5	1.0	μA
Supply voltage READ **	V_{DDR}	3.0	-	6.0	Vdc
Supply current READ*	I_{DDR}	-	0.3	1.5	mA
Supply voltage PROG**	V_{DDP}	4.5	-	6.0	Vdc
Supply current PROG*	I_{DDP}	-	0.5	3.0	mA

*Inputs at V_{SS} or V_{DD}.
**A separate data sheet will be available for 3.3 V ±10% operation.

10

5.3 Electrical Characteristics

Characteristic	Symbol	Min	Typ	Max	Unit
SCL, SDA, SPISS, SPISI Inputs					
Input low voltage	V_{IL}	−0.3	-	0.3*V_{DD}	Vdc
Input high voltage	V_{IH}	0.7*V_{DD}	-	V_{DD} +0.3	Vdc
Input leakage	I_{IN}	-	-	±10	μA
SDA/SPISO Pull down Outputs					
Output low I_{OL} <10μA	V_{OL}	-	-	0.1	Vdc
Output high leakage	I_{OH}	-	-	±10	μA
Output low I_{OL} = 3 mA V_{DD} = 5 V	V_{OL}	-	-	0.4	Vdc
Output low I_{OL} = 1 mA V_{DD} = 3 V	V_{OL}	-	-	0.4	Vdc
SPISO Pull up Output					
Output high I_{OH} = 1.6 mA V_{DD} = 5 V	V_{OH}	V_{DD} − 0.8	-	-	Vdc
Output high I_{OH} = 0.4 mA V_{DD} = 3 V	V_{OH}	V_{DD} − 0.3	-	-	Vdc
MODE, CS1, CS0 Inputs					
Input low voltage	V_{ILV}	−0.3	-	0.3*V_{DD}	Vdc
Input high voltage	V_{IH}	0.7*V_{DD}	-	V_{DD} + 0.3	Vdc
Input leakage	I_{IN}	-	-	±10	μA
Input capacitance	C_{IN}	-	10	-	pF

5.4 SWITCHING PARAMETERS

5.4.1 General Characteristics

Parameter	Parameter	Min	Typ	Max	Min
Programming time 1 byte	t_{PROG}	10	–	–	**mS**
Programming time 4 bytes	t_{PROG}	20	–	–	mS
Write/Erase at 0 to 70 DEG C	$cy_{W/E}$	–	–	10,000	cycles
Write/Erase at ambient temperature	$cy_{W/E}$	–	100,000	–	cycles

10

5.4.2 Serial Bus Input

Characteristic	Symbol	Min	Typ	Max	Unit
SDA/SPISI, SCL/SPICK, SPISS Inputs					
Clock frequency	F_{SCL}	0.0	-	125	kHz
Clock High time	t_{CLH}	4.0	-	-	µS
Clock Low time	t_{CLL}	4.0	-	-	µS
Stop to Start delay	t_{BUF}	4.0	-	-	µS
Start hold time	t_{HSTA}	4.0	-	-	µS
Data hold time	t_{HSDA}	0.0	-	-	µS
Data set-up time	t_{SSDA}	250	-	-	nS
Input Rise time	t_{RI}	-	-	1.0	µS
Input Fall time	t_{FI}	-	-	300	nS
Stop set-up time	t_{SSTO}	4.0	-	-	µS
SPISS Lead time	t_{SS}	4.0	-	-	µS
SPISS Lag time	t_{SSN}	4.0	-	-	µS

All values refer to V_{IH} and V_{IL} levels.

5.4.3 Serial Bus Output

V_{DD} = 5 Vdc ±10%. T_A = 0 to 70°C. C_L = 200 pF.

Characteristic	Symbol	Min	Typ	Max	Unit
SDA/SPISO Outputs					
Data delay	t_{DSDA}	-	1.5	3.5	µS
Rise time SDA	t_{RO}	-	-	*	nS
Rise time SPISO	t_{RO}	-	-	100	nS
Fall time	t_{FO}	-	-	100	nS
SPI select time	t_{SSO}	-	-	1.2	µS
Disable time	t_{DIS}	-	1.5	3.5	µS

10

V_{DD} = 3.3 Vdc ± 10%. T_A = 0 to 70°C. C_L = 200 pF.

Characteristic	Symbol	Min	Typ	Max	Unit
SDA/SPISO Outputs					
Data delay	t_{DSDA}	-	2.0	3.5	µS
Rise time SDA	t_{RO}	-	-	*	nS
Rise time SPISO	t_{RO}	-	-	200	nS
Fall time	t_{FO}	-	-	200	nS
SPI select time	t_{SSO}	-	-	1.5	µS
Disable time	t_{DIS}	-	2.0	3.5	µS

All values referred to V_{IH} and V_{IL} levels.
*Depends on external pull-up resistor value.

Military Products 11

MEMORIES

MIL-STD-883C

Bipolar Memories				883C Package Type and Lead Finish			
Device	**883C**	**Description**	**Pins**	**DIL**	**FP**	**CAN**	**LCCC**
10539	/B	32 x 8-Bit ECL PROM, 17 ns	16	EA	FA		2A
10545	/B	64-Bit ECL Register File, RAM, 18 ns	16	EA	FA		2A
10549	/B	256 x 4-Bit ECL PROM, 30 ns	16	EA	FA		2A
10552	/B	256 x 1-Bit ECL RAM, 15 ns	16	EA	FA		2A
93415	/B	1024 x 1-Bit RAM, Open-Collector	16	EA	FA		
93422	/B	256 x 4-Bit RAM, 3-State Output, 60 ns	22	WA			
93422A	/B	256 x 4-Bit RAM, 3-State Output, 45 ns	22	WA			
93L422	/B	256 x 4-Bit RAM, 3-State Output, 75 ns, Low Power	22	WA			
93425	/B	1024 x 1-Bit RAM, 3-State Output	16	EA	FA		

High Speed CMOS III Cache Tag Memories				883C Package Type and Lead Finish			
Device	**883C**	**Description**	**Pins**	**SB DIL**	**FP**	**CAN**	**LCCC**
4180-30	/B	4K x 4 Cache Tag RAM Comparators, 30 ns	22	3Q90			
4180-35	/B	4K x 4 Cache Tag RAM Comparators, 35 ns	22	3Q90			
4180-40	/B	4K x 4 Cache Tag RAM Comparators, 40 ns	22	3Q90			
62300-30	/B	4K x 4 Cache Tag RAM Comparators, 30 ns	24	Planned			
62350-35	/B	4K x 4 Cache Tag RAM Comparators, 35 ns	24	Planned			
62350-40	/B	4K x 4 Cache Tag RAM Comparators, 40 ns	24	Planned			
62351-30	/B	4K x 4 Cache Tag RAM Comparators, 30 ns	24	Planned			
62351-35	/B	4K x 4 Cache Tag RAM Comparators, 35 ns	24	Planned			
62351-40	/B	4K x 4 Cache Tag RAM Comparators, 40 ns	24	Planned			

CMOS DRAMs				883C Package Type and Lead Finish			
Device	**883C**	**Description**	**Pins**	**SB DIL**	**FP**	**CAN**	**LCCC**
511000-80	/B	1M x 1 High Speed DRAM, Fast Page Mode, 80 ns	18	3Q90			
511000-80	/B	1M x 1 High Speed DRAM, Fast Page Mode, 80 ns	20				3Q90
511000-90	/B	1M x 1 High Speed DRAM, Fast Page Mode, 90 ns	18	3Q90			
511000-90	/B	1M x 1 High Speed DRAM, Fast Page Mode, 90 ns	20				3Q90
511000-110	/B	1M x 1 High Speed DRAM, Fast Page Mode, 110 ns	18	3Q90			
511000-110	/B	1M x 1 High Speed DRAM, Fast Page Mode, 110 ns	20				3Q90

Slow SRAMs				883C Package Type and Lead Finish			
Device	**883C**	**Description**	**Pins**	**SB DIL**	**FP**	**CAN**	**LCCC**
60256-100	/B	32K x 8 Slow Static RAM, 100 ns	28	4Q90			
60256-110	/B	32K x 8 Slow Static RAM, 110 ns	28	4Q90			
60256-130	/B	32K x 8 Slow Static RAM, 130 ns	28	4Q90			

DSP RAMs				883C Package Type and Lead Finish			
Device	**883C**	**Description**	**Pins**	**DIL**	**FP**	**CAN**	**CLCC**
56824-35	/B	8K x 24 DSP RAM, 35 ns	52				Planned
56824-40	/B	8K x 24 DSP RAM, 40 ns	52				Planned
56824-45	/B	8K x 24 DSP RAM, 45ns	52				Planned

MEMORIES

MIL-STD-883C

High Speed CMOS III Static Memories				883C Package Type and Lead Finish			
Device	**883C**	**Description**	**Pins**	**DIL**	**FP**	**CAN**	**LCCC**
6164-55	/B	8K x 8 Fast Static RAM, 55 ns	28	XA			
6164-55	/B	8K x 8 Fast Static RAM, 55 ns	32				UA
6164-70	/B	8K x 8 Fast Static RAM, 70 ns	28	XA			
6164-70	/B	8K x 8 Fast Static RAM, 70 ns	32				UA
6168-55	/B	4K x 4 Fast Static RAM, 55 ns	20	RA			UA
6168-70	/B	4K x 4 Fast Static RAM, 70 ns	20	RA			UA
6206-35	/B	32K x 8 Fast Static RAM, 35 ns	28	3Q90			
6206-35	/B	32K x 8 Fast Static RAM, 35 ns	32				3Q90
6206-45	/B	32K x 8 Fast Static RAM, 45 ns	28	3Q90			
6206-45	/B	32K x 8 Fast Static RAM, 45 ns	32				3Q90
6206-55	/B	32K x 8 Fast Static RAM, 55 ns	28	3Q90			
6206-55	/B	32K x 8 Fast Static RAM, 55 ns	32				3Q90
6206-70	/B	32K x 8 Fast Static RAM, 70 ns	28	3Q90			
6206-70	/B	32K x 8 Fast Static RAM, 70 ns	32				3Q90
6206-100	/B	32K x 8 Fast Static RAM, 100 ns	28	3Q90			
6206-100	/B	32K x 8 Fast Static RAM, 100 ns	32				3Q90
6264-35	/B	8K x 8 Fast Static RAM, 35 ns	28	XA			
6264-35	/B	8K x 8 Fast Static RAM, 35 ns	32				3Q90
6264-45	/B	8K x 8 Fast Static RAM, 45 ns	28	XA			
6264-45	/B	8K x 8 Fast Static RAM, 45 ns	32				3Q90
62L64-35	/B	8K x 8 Fast Static RAM, 35 ns, Low Power	28	XA			
62L64-35	/B	8K x 8 Fast Static RAM, 35 ns, Low Power	32				3Q90
62L64-45	/B	8K x 8 Fast Static RAM, 45 ns, Low Power	28	XA			
62L64-45	/B	8K x 8 Fast Static RAM, 45 ns, Low Power	32				3Q90
6268-35	/B	4K x 4 Fast Static RAM, 35 ns	20	RA	2Q90		UA
6268-45	/B	4K x 4 Fast Static RAM, 45 ns	20	RA	2Q90		UA
6287-35	/B	64K x 1 Fast Static RAM, 35 ns, Low Power	22	XA			UA
6287-45	/B	64K x 1 Fast Static RAM, 45 ns, Low Power	22	XA			UA
62L87-35	/B	64K x 1 Fast Static RAM, 35 ns, Low Power	22	XA			UA
62L87-45	/B	64K x 1 Fast Static RAM, 45 ns, Low Power	22	XA			UA
6288-35	/B	16K x 4 Fast Static RAM, 35 ns	22	XA			UA
6288-45	/B	16K x 4 Fast Static RAM, 45 ns	22	XA			UA
62L88-35	/B	16K x 4 Fast Static RAM, 35 ns, Low Power	22	XA			UA
62L88-45	/B	16K x 4 Fast Static RAM, 45 ns, Low Power	22	XA			UA
6290-35	/B	16K x 4 FSRAM, Chip Enable/Out Enable, 35 ns	24	LA			
6290-35	/B	16K x 4 FSRAM, Chip Enable/Out Enable, 35 ns	28				3Q90
6290-45	/B	16K x 4 FSRAM, Chip Enable/Out Enable, 45 ns	24	LA			
6290-45	/B	16K x 4 FSRAM, Chip Enable/Out Enable, 45 ns	28				3Q90
62L90-35	/B	16K x 4 FSRAM, Chip Enable/Out Enable, 35 Low Power	24	LA			
62L90-35	/B	16K x 4 FSRAM, Chip Enable/Out Enable, 35 ns, Low Power	28				3Q90

MEMORIES

MIL-STD-883C

High Speed CMOS III Static Memories				883C Package Type and Lead Finish			
Device	**883C**	**Description**	**Pins**	**DIL**	**FP**	**CAN**	**LCCC**
62L90-45	/B	16K x 4 FSRAM, Chip Enable/Out Enable, 45 ns, Low Power	24	LA			
62L90-45	/B	16K x 4 FSRAM, Chip Enable/Out Enable, 45 ns, Low Power	28				3Q90
6292-30	/B	16K x 4 Synch SRAM, Transparent Output 30 ns	28	4Q90			
6292-30	/B	16K x 4 Synch SRAM, Transparent Output 30 ns	32				4Q90
6292-35	/B	16K x 4 Synch SRAM, Transparent Output 35 ns	28	4Q90			
6292-35	/B	16K x 4 Synch SRAM, Transparent Output 35 ns	32				4Q90
6292-40	/B	16K x 4 Synch SRAM, Transparent Output 40 ns	28	4Q90			
6292-40	/B	16K x 4 Synch SRAM, Transparent Output 40 ns	32				4Q90
6293-30	/B	16K x 4 Synch SRAM, Synch Output, 30 ns	28	4Q90			
6293-30	/B	16K x 4 Synch SRAM, Synch Output, 30 ns	32				4Q90
6293-35	/B	16K x 4 Synch SRAM, Synch Output, 35 ns	28	4Q90			
6293-35	/B	16K x 4 Synch SRAM, Synch Output, 35 ns	32				4Q90
6293-40	/B	16K x 4 Synch SRAM, Synch Output, 40 ns	28	4Q90			
6293-40	/B	16K x 4 Synch SRAM, Synch Output, 40 ns	32				4Q90
6294-30	/B	16K x 4 Synch SRAM, Out Reg/Out Enable, 30 ns	28	2Q90			
6294-30	/B	16K x 4 Synch SRAM, Out Reg/Out Enable, 30 ns	32				2Q90
6294-35	/B	16K x 4 Synch SRAM, Out Reg/Out Enable, 35 ns	28	2Q90			
6294-35	/B	16K x 4 Synch SRAM, Out Reg/Out Enable, 35 ns	32				2Q90
6294-40	/B	16K x 4 Synch SRAM, Out Reg/Out Enable, 40 ns	28	2Q90			
6294-40	/B	16K x 4 Synch SRAM, Out Reg/Out Enable, 40 ns	32				2Q90
6295-30	/B	16K x 4 Synch SRAM, Transparent Output, Out Enable, 30 ns	28	4Q90			
6295-30	/B	16K x 4 Synch SRAM, Transparent Output, Out Enable, 30 ns	32				4Q90
6295-35	/B	16K x 4 Synch SRAM, Transparent Output, Out Enable, 35 ns	28	4Q90			
6295-35	/B	16K x 4 Synch SRAM, Transparent Output, Out Enable, 35 ns	32				4Q90
6295-40	/B	16K x 4 Synch SRAM, Transparent Output, Out Enable, 40 ns	28	4Q90			
6295-40	/B	16K x 4 Synch SRAM, Transparent Output, Out Enable, 40 ns	32				4Q90

MEMORIES

Standard Military Drawings (SMD)

Bipolar RAM				SMD Package Type and Lead Finish			
Device	SMD	Description	Pins	DIL	FP	CAN	LCCC
10545	5962-8856001	64-Bit Register File (RAM)	16	EA	FA		ZA

HCMOS III Static RAMs				SMD Package Type and Lead Finish			
Device	SMD	Description	Pins	DIL	FP	CAN	LCCC
6164-55	5962-8552505	8K x 8 Fast Static RAM, 55 ns	28	XA			
6164-55	5962-8552505	8K x 8 Fast Static RAM, 55 ns	32				YA
6164-70	5962-8552504	8K x 8 Fast Static RAM, 70 ns	28	XA			
6164-70	5962-8552504	8K x 8 Fast Static RAM, 70 ns	32				YA
6168-55	5962-8670507	4K x 4 Fast Static RAM, 55 ns	20	RA			XA
6168-70	5962-8670509	4K x 4 Fast Static RAM, 70 ns	20	RA			XA
6206-45	5962-8866204	32K x 8 Fast Static RAM, 45 ns	28	3Q90			
6206-45	5962-8866204	32K x 8 Fast Static RAM, 45 ns	32				3Q90
6206-55	5962-8866203	32K x 8 Fast Static RAM, 55 ns	28	3Q90			
6206-55	5962-8866203	32K x 8 Fast Static RAM, 55 ns	32				3Q90
6206-70	5962-8866202	32K x 8 Fast Static RAM, 70 ns	28	3Q90			
6206-70	5962-8866202	32K x 8 Fast Static RAM, 70 ns	32				3Q90
6206-100	5962-8866201	32K x 8 Fast Static RAM, 100 ns	28	3Q90			
6206-100	5962-8866201	32K x 8 Fast Static RAM, 100 ns	32				3Q90
6264-35	5962-8552507	8K x 8 Fast Static RAM, 35 ns	28	XA			
6264-45	5962-8552506	8K x 8 Fast Static RAM, 45 ns	28	XA			
62L64-35	5962-8552508	8K x 8 Fast Static RAM, 35 ns, Low Power	28	XA			
62L64-45	5962-8552509	8K x 8 Fast Static RAM, 45 ns, Low Power	28	XA			
6268-35	5962-8670503	4K x 4 Fast Static RAM, 35 ns	20	RA	2Q90		XA
6268-45	5962-8670505	4K x 4 Fast Static RAM, 45 ns	20	RA	2Q90		XA
6287-35	5962-8601501	64K x 1 Fast Static RAM, 35 ns	22	XA			ZA
6287-45	5962-8601503	64K x 1 Fast Static RAM, 45 ns	22	XA			ZA
62L87-35	5962-8601502	64K x 1 Fast Static RAM, 35 ns, Low Power	22	XA			ZA
62L87-45	5962-8601504	64K x 1 Fast Static RAM, 45 ns, Low Power	22	XA			ZA
6288-35	5962-8685924	16K x 4 Fast Static RAM, 35 ns	22	TA			ZA
6288-45	5962-8685922	16K x 4 Fast Static RAM, 45 ns	22	TA			ZA
62L88-35	5962-8685923	16K x 4 Fast Static RAM, 35 ns, Low Power	22	TA			ZA
62L88-45	5962-8685921	16K x 4 Fast Static RAM, 45 ns, Low Power	22	TA			ZA
6290-35	5962-8685918	16K x 4 FSRAM w/Chip Output Enable, 35 ns	24	LA			
6290-35	5962-8685918	16K x 4 FSRAM w/Chip Output Enable, 35 ns	28				3Q90
6290-45	5962-8685916	16K x 4 FSRAM w/Chip Output Enable, 45 ns	24	LA			
6290-45	5962-8685916	16K x 4 FSRAM w/Chip Output Enable, 45 ns	28				3Q90
62L90-35	5962-8685917	16K x 4 FSRAM w/Chip Output Enable, 35 ns, Low Power	24	LA			
62L90-35	5962-8685917	16K x 4 FSRAM w/Chip Output Enable, 35 ns, Low Power	28				3Q90
62L90-45	5962-8685915	16K x 4 FSRAM w/Chip Output Enable, 45 ns, Low Power	24	LA			
62L90-45	5962-8685915	16K x 4 FSRAM w/Chip Output Enable, 45 ns, Low Power	28				3Q90

MEMORIES

MIL-M-38510

Bipolar Memories				JAN Package Type and Lead Finish			
Device	**JM38510/**	**Description**	**Pins**	**DIL**	**FP**	**CAN**	**LCCC**
93L422	23112	256 x 4 Bit RAM, 3-State Output, 75 ns	22	WA			
93L422	23110	256 x 4 Bit RAM, 3-State Output, 60 ns	22	2Q90			

Reliability Information 12

MOTOROLA CORPORATE QUALITY GOAL

IMPROVE PRODUCT AND SERVICES QUALITY TEN TIMES BY 1989
AND AT LEAST ONE HUNDRED FOLD BY 1991.

ACHIEVE SIX SIGMA CAPABILITY BY 1992.

With a deep sense of urgency, spread dedication to quality to every facet of the corporation and achieve a culture of continual improvement to ASSURE TOTAL CUSTOMER SATISFACTION. There is only one ultimate goal: zero defects in everything we do.

signed:

BOB GALVIN
Chairman

BILL WEISZ
Vice Chairman

JOHN MITCHELL
President

GEORGE FISHER
Deputy to Chief
Executive Office

GARY TOOKER
Chief to Corporate
Staff Officer

JACK GERMAIN
Motorola Director
of Quality

JIM LINCICOME
Government Electronics
Group

CARL LINDHOLM
International
Operations

LEVY KATZIR
New Enterprises

JIM NORLING
Semiconductor Products
Sector

STEVE LEVY
Japanese Operations

DON JONES
Chief Financial
Officer

JIM DONNELLY
Personnel

RAY FARMER
Communications Sector

ED STAIANO
General Systems
Group

GERHARD SCHULMEYER
Automotive & Industrial
Electronics Group

DIVISION QUALITY STATEMENT

MOTOROLA MOS MEMORY PRODUCTS DIVISION

COMMITMENT TO SIX SIGMA
WORLD CLASS

The Memory Products Division staff are pleased to announce our commitment to be a World Class MOS Memory supplier. This means more bullet proof designs which can tolerate handling, processes at the limit and beyond, and outstanding control of the manufacturing processes such that the integration of the design process will result in six sigma products.

We will accomplish this through our dedication to a continuous quality improvement culture. This will ensure our success in reaching the Motorola Corporate goal of total customer satisfaction.

Through our quality improvement process using SIX SIGMA methodology we can and will accomplish being the best memory supplier through WORLD CLASS product margins and services in their truest sense.

ENDORSEMENTS:

Jim George | Bud Broeker | Bill Bowers | Jim Eachus

Mike Parks | Roger Kung | Bill Pfaff

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OUR SIX SIGMA CHALLENGE

WHAT IS SIX SIGMA?

Six Sigma is the required capability level to approach the Standard. The Standard is Zero Defects. Our goal is to be best-in-class in Product, Sales, and Service.

WHY SIX SIGMA?

The performance of a product is determined by how much margin exists between the process characteristics required by the design, and the actual value of those characteristics. These characteristics are produced by processes in the factory, and at the suppliers.

Each process attempts to reproduce its characteristics identically from unit to unit, but within each process some variation does occur. For some processes, such as those which use real-time feedback to control the outcome, the variation is quite small, and for others it may be quite large.

Variation of the process is measured in Standard Deviations (Sigma) from the Mean. The normal variation, defined as process width, is ±3 Sigma about the mean.

Approximately 2,700 parts per million parts/steps will fall outside the normal variation of ±3 Sigma, see Figure 1. This, by itself, does not appear disconcerting. However, when we build a product containing 1,200 parts/steps, we can expect 3.24 defects per unit (1200 × 0.0027), on an average. This would result in a rolled yield of less than 4%, which means fewer than 4 units out of every hundred would go through the entire manufacturing process without a defect, see Table 1.

Thus, we can see that for a product to be built virtually defect-free, it must be designed to accept characteristics that are significantly more than ±3 Sigma away from the Mean.

It can be shown that a design that can accept **twice the normal variation** of the process, or ±6 Sigma, can be expected to have no more than 3.4 parts per million defective for each characteristic, even if the process mean were to shift by as much as ±1.5 Sigma, see Figure 1. To quantify this, Capability Index (Cp) is used, where:

$$Cp = \frac{\text{design specification width}}{\text{process width}}$$

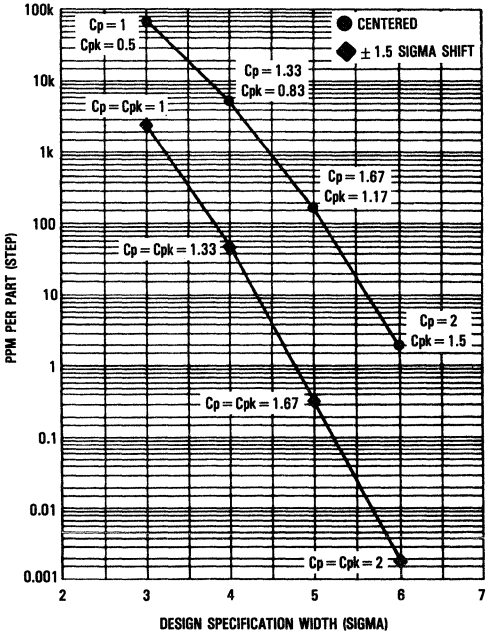

Figure 1. Standard Deviations from Mean

Table 1. Rolled Yield

TOTAL DEFECTS PER UNIT	ROLLED THROUGHPUT YIELD (%)
5.3	0.5
4.6	1.0
3.9	2.0
3.5	3.0
3.2	4.0
3.0	5.0
2.3	10
1.9	15
1.6	20
1.4	25
1.2	30
1.0	37
0.9	40
0.8	45
0.7	50
0.6	55
0.51	60
0.43	65
0.36	70
0.29	75
0.22	80
0.16	85
0.10	90
0.05	95
0.00	100

ROLLED THROUGHPUT YIELD (%) = $100\ e^{-d/u}$

A design specification width of ±6 Sigma and a process width of ±3 Sigma yields a Cp of 12/6 = 2. However, as shown in Figure 2, the process mean can shift. When the process mean is shifted with respect to the design target mean, the Capability Index is adjusted with a factor k, and becomes Cpk. Cpk = Cp(1 − k), where:

$$k = \frac{\text{process shift}}{\text{design specification width/2}}$$

The k factor for ±6 Sigma design with a 1.5 Sigma process shift = 1.5/(12/2) = 0.25, and the Cpk = 2(1 − 0.25) = 1.5.

In the same case of a product containing 1,200 parts/steps, we would now expect only 0.0041 defects per unit (1200 × 0.0000034). This would mean that 996 units out of 1,000 would go through the entire manufacturing process without a defect (see Table 2).

It is our five year goal to achieve ±6 Sigma capability in Product, Sales, and Service.

Table 2. Overall Yield vs Sigma (Distribution Shifted ±1.5 σ)

NUMBER OF PARTS (STEPS)	±3 σ (%)	±4 σ (%)	±5 σ (%)	±6 σ (%)
1	93.32	99.379	99.9767	99.99966
7	61.63	95.733	99.839	99.9976
10	50.08	93.96	99.768	99.9966
20	25.08	88.29	99.536	99.9932
40	6.29	77.94	99.074	99.9864
60	1.58	68.81	98.614	99.9796
80	0.40	60.75	98.156	99.9728
100	0.10	53.64	97.70	99.966
150	–	39.38	96.61	99.949
200	–	28.77	95.45	99.932
300	–	15.43	93.26	99.898
400	–	8.28	91.11	99.864
500	–	4.44	89.02	99.830
600	–	2.38	86.97	99.796
700	–	1.28	84.97	99.762
800	–	0.69	83.02	99.729
900	–	0.37	81.11	99.695
1000	–	0.20	79.24	99.661
1200	–	0.06	75.88	99.593
3000	–	–	50.15	98.985
17000	–	–	0.02	94.384
38000	–	–	–	87.880
70000	–	–	–	78.820
150000	–	–	–	60.000

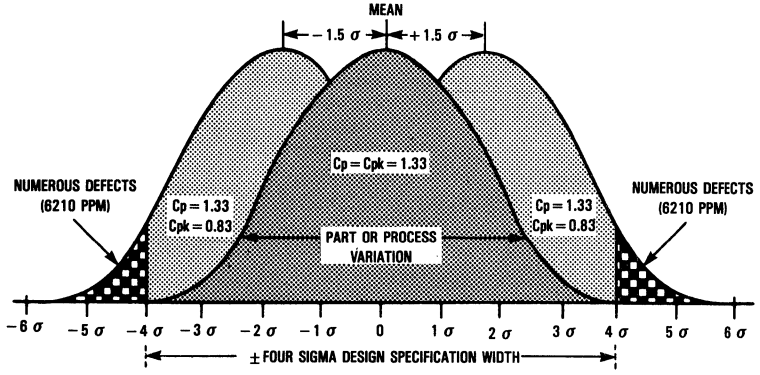

Figure 2a. Four Sigma Capability

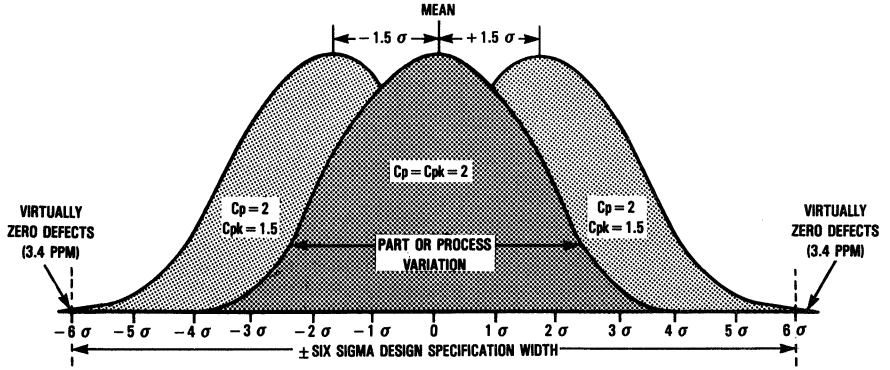

Figure 2b. Six Sigma Capability

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QUALITY MONITORING

Average Outgoing Quality (AOQ) refers to the number of devices per million that are outside specification limits at the time of shipment. Motorola has continually improved its outgoing quality, and has established a goal of zero defects. This level of quality will lead to vendor certification programs with many of our customers. The program ensures a certain level of quality, thus allowing a customer to either reduce or eliminate the need for incoming inspections.

By paying strict attention to quality at an early stage, the possibility of failures occurring further down the line is greatly minimized. Motorola's electrical parametric testing eliminates devices that do not conform to electrical specification. Additional parametric testing on a sample basis provides data for continued improvement.

AVERAGE OUTGOING QUALITY (AOQ) CALCULATION

$$\text{AOQ in PPM} = (\text{Process Average}) \cdot (\text{Lot Acceptance Rate}) \cdot (10^6)$$

$$\text{Process Average} = \frac{\text{Total Projected Reject Devices}^*}{\text{Total Number of Devices}}$$

$$\text{Projected Reject Devices} = \frac{\text{Defects in Sample}}{\text{Sample Size}} \cdot \text{Lot Size}$$

$$\text{Total Number of Devices} = \text{Sum of all the units in each submitted lot}$$

$$\text{Lot Acceptance Rate} = 1 - \frac{\text{Number of Lots Rejected}}{\text{Number of Lots Tested}}$$

10^6 = Conversion to parts per million (PPM)

MARKING PERMANENCY, HERMETICITY, AND SOLDERABILITY MONITORS

Marking permanency testing is performed per Motorola specification. The procedure involves soaking the device in various solvents, brushing the markings, and then inspecting the markings for legibility.

Hermeticity monitoring includes tests for both fine and gross leaks in the hermetic package seal.

Solderability testing is used to ensure that device leads can be soldered without voids, discoloration, flaking, dewetting, or bridging. Typically, the test specifies steam preconditioning followed by a 235° to 260°C solder dip and microscope inspection of the leads.

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RELIABILITY MONITORING

Motorola recognizes the need to monitor established MOS Memory products to maintain the level of quality and reliability demonstrated through the internal and joint qualification processes. Motorola maintains a system of monitor programs that provide monthly feedback on the extensive matrix of Motorola fabrication, assembly, and testing technologies that produce our products. As with qualification activity, great care is taken to assure the accuracy and quality of the data generated.

*All rejects: visual, mechanical, and electrical (dc, ac, and high/low temperature).

RELIABILITY STRESS TESTS

The following summary gives brief descriptions of the various reliability tests included in both reliability qualification and monitor programs. Not all of the tests listed are performed by each program and other tests can be performed when appropriate. Refer to Table 3.

Table 3. Stresses and Typical Stress Conditions

Stress	Typical Stress Condition
High Temperature Operating Life, Dynamic or Static	125°C, 6.0 V
Temperature Cycle	−65°C to +150°C Air to Air
Thermal Shock	−65°C to +150°C Liquid to Liquid
Temperature Humidity Bias	85°C, 85% RH, 5.0 V
Autoclave	121°C, 100% RH, 15 psig
Pressure Temperature Humidity Bias	148°C, 90% RH, 44 psig, 5.0 V
Low Temperature Operating Life	0°C/25°C, 6.0 V

HIGH TEMPERATURE OPERATING LIFE

High temperature operating life (HTOL or HTRB) testing is performed to accelerate failure mechanisms that are thermally activated through the application of extreme temperatures and the use of biased operating conditions. The temperature and voltage conditions used in the stress will vary with the product being stressed. However, the typical stress ambient is 125°C with the bias applied equal to or greater than the data sheet nominal value. All devices used in the HTOL test are sampled directly after final electrical test with no prior burn-in or other prescreening unless called out in the normal production flow. Testing can either be performed with dynamic signals applied to the device or in a static bias configuration.

TEMPERATURE CYCLE

Temperature cycle testing accelerates the effects of thermal expansion mismatch among the different components within a specific die and packaging system. This test is typically performed per MIL-STD-883 or MIL-STD-750 with the minimum and maximum temperatures being −65°C and +150°C. During temperature cycle testing, devices are inserted into a cycling system and held at the cold dwell temperature for at least ten minutes. Following this cold dwell, the devices are heated to the hot dwell where they remain for another ten minute minimum time period. The system employs a circulating air environment to assure rapid stabilization at the specified temperature. The dwell at each extreme, plus the two transition times of five minutes each (one up to the hot dwell temperature, another down to the cold dwell temperature), constitute one cycle. Test duration for this test will vary with device and packaging system employed.

THERMAL SHOCK

The objective of thermal shock testing is the same as that for temperature cycle testing—to emphasize differences in expansion coefficients for components of the packaging system. However, thermal shock provides additional stress in that

the device is exposed to a sudden change in temperature due to the transfer time of ten seconds maximum as well as the increased thermal conductivity of a liquid ambient. This test is typically performed per MIL-STD-883 or MIL-STD-750 with the minimum and maximum temperatures being −65°C and +150°C. Devices are placed in a fluorocarbon bath and cooled to minimum specified temperature. After being held in the cold chamber for five minutes minimum, the devices are transferred to an adjacent chamber filled with fluorocarbon at the maximum specified temperature for an equivalent time. Two five-minute dwells plus two ten-second transitions constitute one cycle.

TEMPERATURE HUMIDITY BIAS

Temperature humidity bias (THB or H^3TRB) is an environmental test performed at a temperature of 85°C and a relative humidity of 85%. The test is designed to measure the moisture resistance of plastic encapsulated circuits. A nominal static bias is applied to the device to create the electrolytic cells necessary to accelerate corrosion of the metallization.

AUTOCLAVE

Autoclave is an environmental test which measures device resistance to moisture penetration and the resultant effects of galvanic corrosion. Conditions employed during the test include 121°C, 100% relative humidity, and 15 psig. Corrosion of the die is the expected failure mechanism. Autoclave is a highly accelerated and destructive test.

PTHB (PRESSURE-TEMPERATURE-HUMIDITY-BIAS)

This test is performed to accelerate the effects of moisture penetration with the dominant effect being corrosion. The test detects similar failure mechanisms as THB but at a greatly accelerated rate. Conditions usually employed during the test are a temperature of 148°C, pressure of 44 psig or greater, a relative humidity of 90%, and a bias level which is the nominal rating of the device.

LOW TEMPERATURE OPERATING LIFE

This test is performed primarily to accelerate hot carrier injection effects in semiconductor devices by exposing them to room ambient or colder temperatures with the use of biased operating conditions. Threshold shifts or other parametric changes are typically the basis for failure. The length of this test will vary with temperature and bias conditions employed.

SYSTEM SOFT ERROR

System soft error is designed to detect errors caused by impact ionization of silicon by high energy particles. This stress is performed on a system level basis. The system is operated for millions of device hours to obtain an accurate measure of actual system soft error performance.

MECHANICAL SHOCK

This test is typically performed per MIL-STD-883 or MIL-STD-750 and is used to examine the ability of the device to withstand a sudden change in mechanical stress typically due to abrupt changes in motion as seen in handling, transportation, or actual use. The typical test condition would be as follows: acceleration = 1500 g, orientation = Y1 plane, t = 0.5 ms, and number of pulses = 5.

VARIABLE FREQUENCY VIBRATION

This test is typically performed per MIL-STD-883 or MIL-STD-750 and is used to examine the ability of the device to withstand deterioration due to mechanical resonance. The typical test condition is: peak acceleration = 20 g, frequency range = 20 Hz to 20 kHz, and t = 48 minutes.

CONSTANT ACCELERATION

This test is typically performed per MIL-STD-883 or MIL-STD-750 and is used to indicate structural or mechanical weaknesses in a device/packaging system by applying a severe mechanical stress. A typical test condition used is as follows: stress level = 30 kg, orientation = Y1 plane, and t = 1 minute.

QUALITY SYSTEMS

A Global Quality System is key to achieving our goal of "Best In Class". Quality systems are implemented in wafer fabrication, assembly, final test, and distribution world wide. Figure 3 depicts Quality Assurance involvement and the techniques applied in the general flow of product and Figure 4 shows Memory Manufacturing locations world wide.

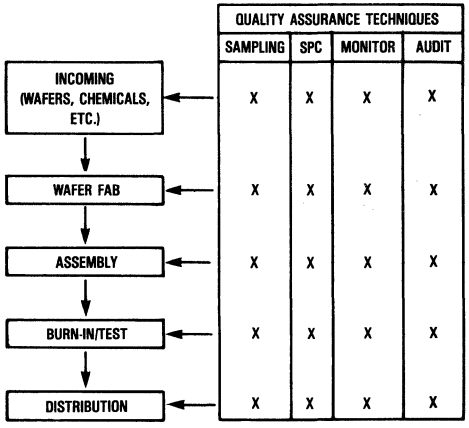

Figure 3. General Product Flow

Direct Customer interaction ensures the receipt of product that meets all of their requirements 100% of the time. In fact, the MOS Memories Reliability and Quality Assurance department has devised a customer advocate list that assigns key Reliability and Quality Assurance personnel to specific customers in order to facilitate any inquiry regarding quality, reliability, or any other issue they may want to discuss.

All processes and procedures that relate to the manufacturing of MOS Memories are fully documented, and regular audits are performed to ensure continuous adherence to proper procedures. We are always striving to produce and reproduce the highest quality product available throughout the world.

MOS Memory Products Division promotes the concept of statistical process controls throughout the entire manufacturing process. This is exemplified by our commitment to in-depth statistical process control training programs for everyone—from the line operator to upper management. Favorable results have already been realized from the initial phases of implementation, with much more to follow.

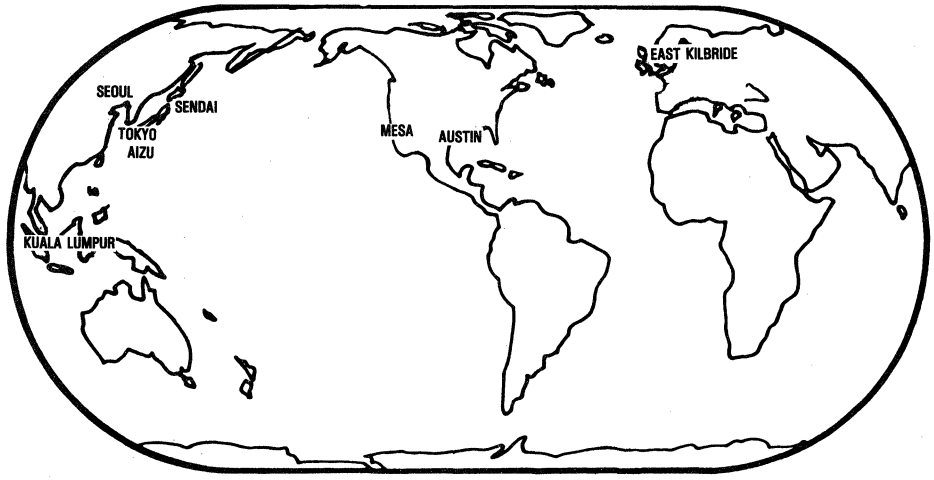

Figure 4. Wafer Fab/Assembly/Final Test Locations

The MOS Memory Products Division maintains a World Wide Quality Assurance system that is second to none. Daily status reports are received from remote locations, and any problems that arise are tackled on a timely basis. The MOS Memory Products Division is also a leader in accurate and efficient methods of quality data collection and reporting.

Every unit that the MOS Memory Products Division produces is coded so that complete traceability is maintained, including visibility to the wafer and assembly lot level. The Quality System ensures that we can provide any specific processing information to our customers on request.

INTERNAL QUALIFICATION DISCIPLINE

Motorola recognizes the need to establish that all MOS Memory devices, both new products as well as existing ones, reach and maintain a level of quality and reliability that is unsurpassed in the electronics marketplace. To ensure this, internal qualification requirements, procedures, and methods as well as vendor qualification specifications have been developed. These activities are intended to provide a consistent, comprehensive, and methodical approach to device qualification and to improve our customer's understanding of Motorola's qualification results and their subsequent application implications.

For qualification results to be valid and acceptable, the collected data must be proven accurate to the highest possible confidence level. Therefore, a complete device history and data log is kept with any lost or missing data potentially leading to test results that are unusable for qualification purposes. Testing conditions and pass/fail criteria are established before stressing begins. Strict adherence to these criteria and the use of control devices insure that the test results are valid and meaningful.

New MOS Memory devices which are under development or in the prototype stage are subject to requirements defined for the three levels of the development cycle. These levels are the alpha, beta, and introductory phases of device development. Each phase contains guidelines and controls concerning issues such as device labeling, number of customers, sample quantities, pricing and stocking levels, and open-order-entry timing. Decisions regarding these items are made jointly by marketing, design, product, and reliability personnel.

JOINT QUALIFICATION

As a result of the rigorous discipline used for internal qualification of Motorola MOS Memory products, our customers can benefit from joint qualification activities. Motorola's clearly defined qualification procedures improve the customer's ability to comprehend the qualification results in an effective manner which aides in their qualification decision making process. Through parallel qualification activities between Motorola and its customers, this procedure can cut qualification costs by reducing duplication of effort, improving resource utilization, and shortening introduction cycle time. This helps to ensure competitive edge advantages for our customers.

Joint Qualification activities result in a partnership type of interaction between Motorola and its customers on an engineering level. This assists our customers in two critical areas. First, it allows them to understand more clearly the strengths and weaknesses of Motorola's products. Secondly, our customers can make clear decisions concerning which stresses they need to concentrate on during their internal qualification activities.

HISTORICAL PERFORMANCE

Over the course of the last five years, significant achievements have been made on quality and delivery performance. The Six Sigma methodology will assist the MOS Memory Products Division in pursuit of our standard of zero defects and 100% on time delivery.

Figure 5 indicates the product Average Outgoing Quality performance as measured in parts per million.

As of October 1988 our average outgoing quality was below 50 parts per million. We are striving to reach Six Sigma.

1988 MALCOLM BALDRIGE NATIONAL QUALITY AWARD

Motorola won the first Malcolm Baldrige National Quality Award. The award recognizes the achievements of U.S. manufacturing and service companies. The award was established in 1987 to promote quality awareness, recognize the achievements of U.S. companies, and publicize successful quality strategies. Our quality process was examined for corporate quality leadership, information and analysis, planning, human resource utilization, quality assurance, quality improvement results, and Customer Satisfaction. Our fundamental objective—Everyone's overriding responsibility is Total Customer Satisfaction. Six Sigma Quality is a key initiative for the achievement of our fundamental objective.

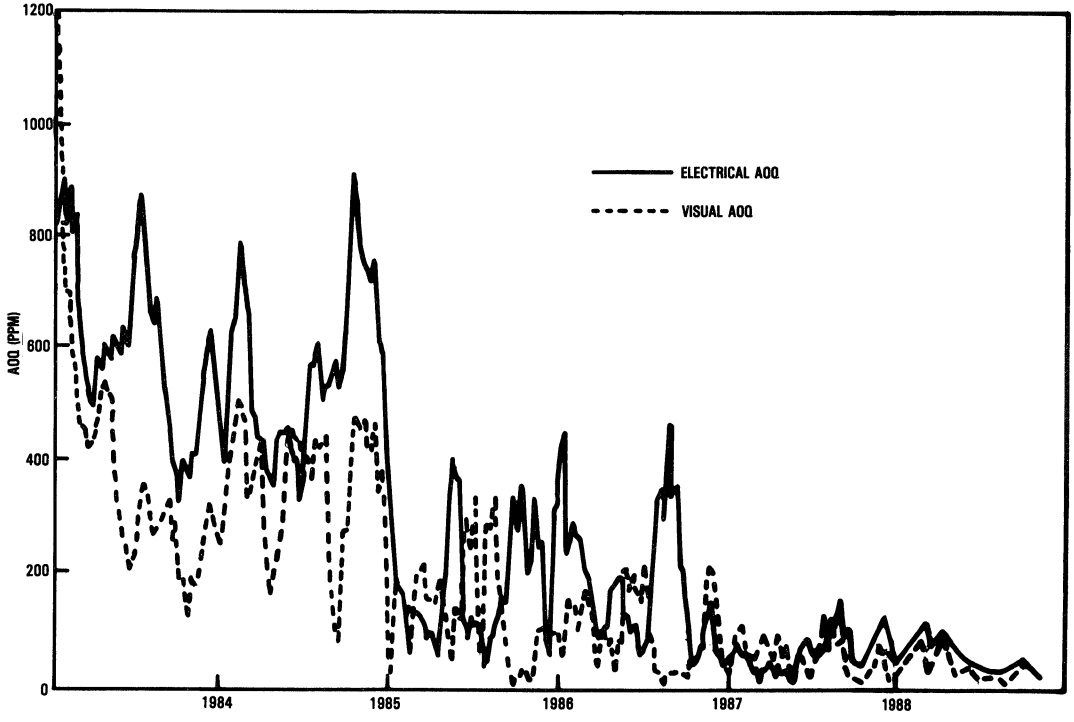

Figure 5. Motorola MOS Memory Products Division Average Outgoing Quality—4 Week Average World Memory

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Applications Information

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AN987

DRAM Refresh Modes

DRAMs offer the lowest cost per bit of any memory, and for that reason are enormously popular in a wide range of applications. This low cost per bit is achieved with a very simple bit cell design, among other things, but rooted in this simplicity are some inherent drawbacks. One major limitation is the need to refresh each memory bit at regular intervals. This note discusses what refresh is, the reasons refresh is required for DRAM operation, and the various types of refresh available on the Motorola 1M × 1 and 256K × 4 DRAMs. Specific comments refer to the 1M × 1 85-ns DRAM. Refer to specific device data sheets for analogous information on other devices.

The heart of any memory device is the bit cell. A 1M DRAM has 1,048,576 of these cells in the memory array. Each cell holds a single bit of information in the form of a high or low voltage, where high voltage = a binary "1" and low voltage = a binary "0". The DRAM bit cell consists of one transistor and one capacitor. The transistor acts as a switch, regulating when the capacitor will charge and discharge, while the capacitor stores a high or low voltage charge.

All capacitors leak over time, slowly losing the charge stored in them, regardless of how carefully they are constructed. Junction and dielectric leakage are two capacitor discharge paths that are characteristic of the DRAM bit cell, and both are affected by temperature. The capacitor in the bit cell can hold a small charge, on the order of 35–125 fF (fF = 1×10^{-15} farads). As this charge dissipates through leakage paths, the small difference between a "1" and a "0" diminishes. If nothing is done to restore the charge on the capacitor to its initial value, the sensing circuitry on the DRAM will eventually be unable to detect a charge difference and will read the cell as a "0".

Thus, all the capacitors in the memory array must be periodically recharged, or refreshed. Refresh is accomplished by accessing each row in the array, one row at a time. When a row is accessed, it is turned on, and voltage is applied to the row, recharging each capacitor on the row to its initial value. Specified refresh time on the 1M × 1 DRAM is 8 milliseconds; every row must be recharged every 8 milliseconds. This is a vast improvement over refresh times required for earlier generations of DRAMs. The 16K × 1 DRAM required refresh every 2 milliseconds, the 256K × 1 DRAM requires a refresh every 4 milliseconds. Longer refresh times mean more time available for access to memory, and less time required to refresh the device.

Design and operation of the DRAM allow only one row to be refreshed at a time; 512 refresh cycles are required to refresh the entire 1M × 1 memory array. The array is actually 1024 rows by 1024 columns, but it operates electrically like two half arrays of 512 rows by 1024 columns. During refresh, every row is treated as if it runs through both halves of the array, refreshing 2048 column locations (bit cells) per row. This design results in fewer refresh cycles required to recharge the entire array, since only 512 rows need to be accessed, rather than 1024.

Refresh can be performed in either a single **burst** of 512 consecutive refresh cycles (one cycle per row) every 8 milliseconds, or **distributed** over time, one refresh cycle every 15 microseconds (8 milliseconds per 512 rows = 15.6 microseconds per row) on average, or some combination of these two extremes. As long as every row is refreshed within 8 milliseconds, the actual method used is best determined by system use of the DRAM. The burst takes 84 microseconds to complete (165 nanoseconds per row × 512 rows for 85 nanoseconds per device). During this burst refresh time, no memory operations can be performed on the device. Distributed refresh disables memory access for 165 nanoseconds every 15 microseconds.

The 1M × 1 DRAM can be refreshed in three ways: $\overline{RAS}$ only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, and hidden refresh. In addition, any normal read or write refreshes all 2048 bit cells on the row accessed. Regardless of the refresh method used, the time required to refresh one row is the random read or write ($\overline{RAS}$) cycle time (t_{RC}). When operating the device in page, nibble, or static column mode, only the row being accessed is refreshed. The device must be in normal random mode to utilize any of these specific refresh methods.

$\overline{RAS}$ only refresh requires external row counters, to ensure all rows are refreshed within the specified time, and externally-supplied row addresses. $\overline{CAS}$ before $\overline{RAS}$ relies on internal row counters and internally generates the address of the next row to be refreshed. Hidden refresh is a variation on $\overline{CAS}$ before $\overline{RAS}$ refresh that holds valid data at the output while refresh is occurring. Whenever the device is in a refresh cycle, neither a read nor a write operation can be performed. Hidden refresh allows the device to be read ahead of refresh, then holds the valid data at the output while refresh cycles are in progress. It appears that the refresh is hidden among data cycles because valid data is maintained at the output.

$\overline{RAS}$ only refresh is performed by supplying row addresses A0–A8 and completing a $\overline{RAS}$ cycle (t_{RC}); switching $\overline{RAS}$ from inactive (high) to active (low), holding $\overline{RAS}$ low (t_{RAS}), then switching back to high, and holding $\overline{RAS}$ high (t_{RP}). A9 is ignored during $\overline{RAS}$ only refresh, since this address normally determines which half of the array is to be accessed. $\overline{CAS}$ must be held high through this $\overline{RAS}$ cycle, hence the name $\overline{RAS}$ only refresh. An external row counter is required for this refresh method. See Figure 1.

$\overline{CAS}$ before $\overline{RAS}$ refresh is performed by switching $\overline{CAS}$ from high to low while $\overline{RAS}$ is high, then switching $\overline{RAS}$ low (t_{CSR}). This reversal of the usual clock order activates an internal row counter that generates addresses to be refreshed; external addresses are ignored in this cycle. $\overline{CAS}$ must be held low (t_{CHR}) after $\overline{RAS}$ transitions to low. After that time it can either be held low or switched to high. See Figure 2. The $\overline{CAS}$ before $\overline{RAS}$ refresh counter test, specified on all DRAM data sheets that offer this type of refresh, is used to check for proper operation of the internal row counters and correct address generation.

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Hidden refresh is a $\overline{CAS}$ before $\overline{RAS}$ refresh that has been initiated during a read or write operation. At the end of a typical read cycle, $\overline{CAS}$ would be switched to high before $\overline{RAS}$, turning off the output. In a hidden refresh cycle, $\overline{RAS}$ is switched to high, concluding the $\overline{RAS}$ cycle (t_{RC}), while $\overline{CAS}$ is held low. $\overline{RAS}$ is held high (t_{RP}), then switched low, beginning another $\overline{RAS}$ cycle. As long as $\overline{CAS}$ is held low, data is valid at the output, resulting in a long read cycle. Since data can be read while the device is being refreshed, the refresh operation(s) appears to be hidden by the read cycle. The same refresh can be performed after a write cycle is initiated. This method of refresh allows refresh cycles to be mixed within read and write cycles. During the refresh cycle, a write operation cannot be performed. See Figure 3.

Refresh is an integral and necessary part of DRAM operation. Substantial improvement has been made in increasing the time between refresh cycles, but as long as the bit cell design utilizes a capacitor, periodic recharging will be required. Three methods of refresh are available on the 1M × 1 DRAM: $\overline{RAS}$ only, $\overline{CAS}$ before $\overline{RAS}$, and hidden refresh. The Motorola 1M × 1 and 256K × 4 will work in virtually all systems as a result of flexibility provided by this assortment of refresh methods.

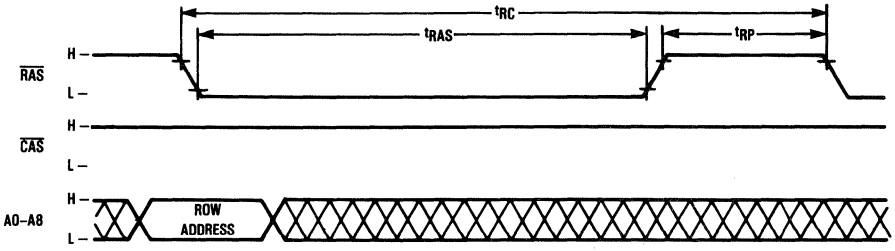

Figure 1. $\overline{RAS}$ Only Refresh Cycle

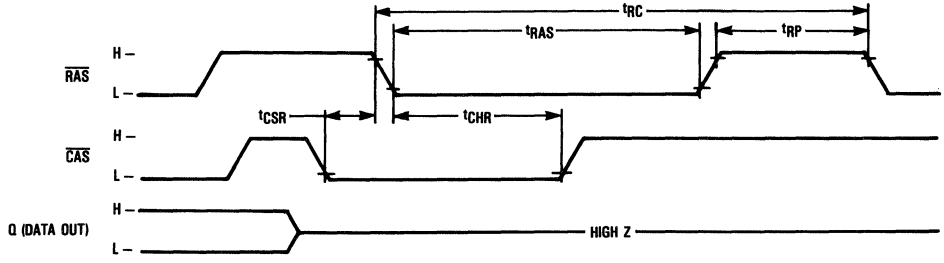

Figure 2. $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle

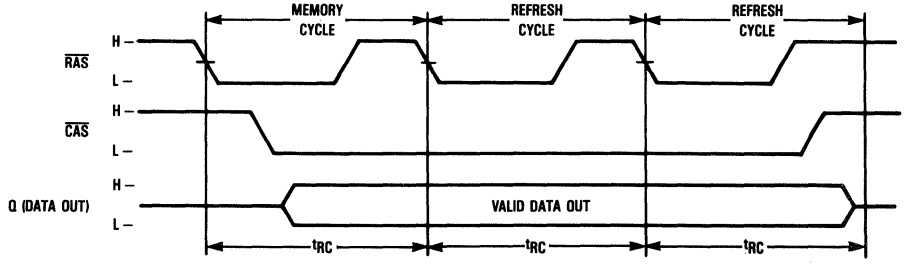

Figure 3. Hidden Refresh Cycle

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AN986

Page, Nibble, and Static Column Modes: High-Speed, Serial-Access Options on 1M-Bit + DRAMs

The 1M-bit and higher density DRAMs offered by Motorola, in addition to operating in a standard mode at advertised access times, have special operating modes that will significantly decrease access time. These are page, nibble, and static column modes. All three modes are available in the 1M × 1 configuration; page and static column modes are also available on the 256K × 4 configuration. Read, write, and read-write operations can be mixed and performed in any order while these devices are operating in either random or special mode.

The comments that follow refer specifically to successive read operations for page, nibble, and static column modes on the 1M × 1 device. The read operation is chosen for sake of simplicity in illustrating these special operating modes. However, decreased access times will occur for all operations, performed in any order, when the device is operated in any of these modes. General operating comments apply to the 256K × 4 device as well.

All of these special operating modes are useful in applications that require high-speed serial access. Typical examples include video bit map graphics monitors or RAM disks. Page mode is the standard, available since the days of the 16K × 1 DRAM. Static column is the latest mode to be made available on DRAMs, and nibble mode first appeared somewhere in between. Page and static column offer the same column location access, but operate somewhat differently. Nibble is unlike either of the other modes, but faster than both in its niche. All modes are initiated after a standard read or write is performed.

Page and static column modes allow access to any of 1024 column locations on a specific row, while nibble allows access to a maximum of four bits. The location of the first bit in nibble mode determines the other bits to be accessed. Nibble mode allows the fastest access of the three devices (t_{NCAC}), all other parameters held equal, at about 1/4 the standard (t_{RAC}) rate. Page and static column access times (t_{CAC}, t_{AA}) are, respectively, about 1/3 and 1/2 the standard rate.

Cycle time is a better indicator of relative speed improvement, since it measures the minimum time between any two successive reads. Cycle time is approximately 1/4 for nibble and 1/3 for page and static column modes, with respect to a

Table 1. Operating Characteristic Comparison

Parameter		Page	Nibble	Static Column	Random
Access Time (ns)*	t_{CAC}	25	—	—	—
	t_{NCAC}	—	20	—	—
	t_{AA}	—	—	45	—
	t_{RAC}	—	—	—	85
Cycle Time (ns)*	t_{PC}	50	—	—	—
	t_{NC}	—	40	—	—
	t_{SC}	—	—	50	—
	t_{RC}	—	—	—	165
Accessible Bits		1024	4	1024	All
Order of Accessible Bits		Random	Fixed	Random	Random
Conditions	$\overline{RAS}$	Active	Active	Active	Cycle
	$\overline{CAS}$ or $\overline{CS}$**	Cycle	Cycle	Active	Cycle
	Addresses	Cycle	N/A	Cycle	Cycle
	Outputs	Cycle	Cycle	Active	Cycle
Time to Read 4 Bits (ns)*		235	205	235	660
Time to Read 1024 Unique Bits (ns)*		51,235	70,400	51,235	168,960

*Values for a 1M × 1 85-ns device.

**$\overline{CS}$ on Static Column.

Page: 4 bit read = $t_{RAC} + 3t_{PC}$
1024 bit read = $t_{RAC} + 1023t_{PC}$

Nibble: 4 bit read = $t_{RAC} + 3t_{NC}$
1024 bit read = $256 \cdot (t_{RAC} + 3t_{NC} + t_{RP})$

Static Column: 4 bit read = $t_{RAC} + 3t_{SC}$
1024 bit read = $t_{RAC} + 1023t_{SC}$

Random: 4 bit read = $4t_{RC}$
1024 bit read = $1024t_{RC}$

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random cycle time of 165 nanoseconds. When operated in these high-speed modes, users will typically access most or all of the bits available to that mode, once the mode has been initiated. Thus the best measure of speed for nibble mode is the rate at which four bits are read, while the rate at which 1024 bits are read is the best measure of page or static column mode. When the actual operating conditions are considered, as described elsewhere, the difference between t_{CAC}, t_{NCAC}, and t_{AA} measurements hold relatively little significance.

Page mode is slightly more difficult to interface in a system than static column mode due to extra $\overline{CAS}$ pulses that are required in page mode. Static column generates less noise than page mode, because output buffers and $\overline{CS}$ are always active in this mode. Noise transients, generated every time $\overline{CAS}$ is cycled from inactive to active, are thus eliminated in the static column mode.

PAGE MODE

Page mode allows faster access to any of the 1024 column locations on a given row, typically at one third the standard (t_{RAC}) rate for randomly-performed operations. Page mode consists of cycling the $\overline{CAS}$ clock from active (low) to inactive (high) and back, and providing a column address, while holding the $\overline{RAS}$ clock active (low). A new column location can be accessed with each $\overline{CAS}$ cycle (t_{PC}).

Page mode is initiated with a standard read or write operation. Row address is latched by the $\overline{RAS}$ clock transition to active, followed by column address and $\overline{CAS}$ clock active. Performing a $\overline{CAS}$ cycle (t_{PC}) and supplying a column address while $\overline{RAS}$ clock remains active constitutes the first page mode cycle. Subsequent page mode cycles can be performed as long as $\overline{RAS}$ clock is active. The first access (data valid) occurs at the standard rate (t_{RAC}). All of the read operations in page mode following the initial operation are measured at the faster rate (t_{CAC}), provided all other timing minimums are maintained (see Figure 1a). Page mode cycle time determines how fast successive bits are read (see Figure 1b).

NIBBLE MODE

Nibble mode allows serial access to two, three, or four bits of data at a much higher rate than random operations (t_{RAC}). Nibble mode consists of cycling the $\overline{CAS}$ clock while holding the $\overline{RAS}$ clock active, like page mode. Internal row and column address counters increment at each $\overline{CAS}$ cycle, thus no external column addresses are required (unlike page or static column modes). After cycling $\overline{CAS}$ three times in nibble mode, the address sequence repeats and the same four bits are accessed again, in serial order, upon subsequent cycles of $\overline{CAS}$:

00, 01, 10, 11, 00, 01, 10, 11, . . .

Nibble mode operation is initiated with a standard read or write cycle. Row address is latched by $\overline{RAS}$ clock transition to active, followed by column addresses and $\overline{CAS}$ clock. Performing a $\overline{CAS}$ cycle (t_{NC}) while $\overline{RAS}$ clock remains active constitutes the first nibble mode cycle. Subsequent nibble mode cycles can be performed as long as the $\overline{RAS}$ clock is held active. The first access (data out) occurs at the standard rate (t_{RAC}). All of the read operations in nibble mode following the initial operation are measured at the faster rate (t_{NCAC}), provided all other timing minimums are maintained (see Figure 2a). Nibble mode cycle time determines how fast successive bits are read (see Figure 2b).

STATIC COLUMN MODE

This mode is useful in applications that require less noise than page mode. Output buffers are always on when the device is in this mode and $\overline{CS}$ clock is not cycled, resulting in fewer transients and simpler operation. It allows faster access to any of the 1024 column addresses on a given row, typically at half the standard (t_{RAC}) rate for randomly performed operations. Static column consists of changing column addresses while holding the $\overline{RAS}$ and $\overline{CS}$ clocks active. A new column location can be accessed with each static column cycle (t_{SC}).

Static column mode operation is initiated with a standard read or write cycle. Row address is latched by $\overline{RAS}$ clock transition to active, followed by column addresses and $\overline{CS}$ clock. Performing an address cycle (t_{SC}) while $\overline{RAS}$ and $\overline{CS}$ clocks remain active constitutes the first static column cycle. Subsequent static column cycles can be performed as long as the $\overline{RAS}$ and $\overline{CS}$ clocks are held active. The first access (data out) occurs at the standard (t_{RAC}) rate. All of the read operations in static column following the initial operation are measured at the faster rate (t_{AA}), provided all other timing minimums are maintained (see Figure 3a). Static column cycle time determines how fast successive bits are read (see Figure 3b).

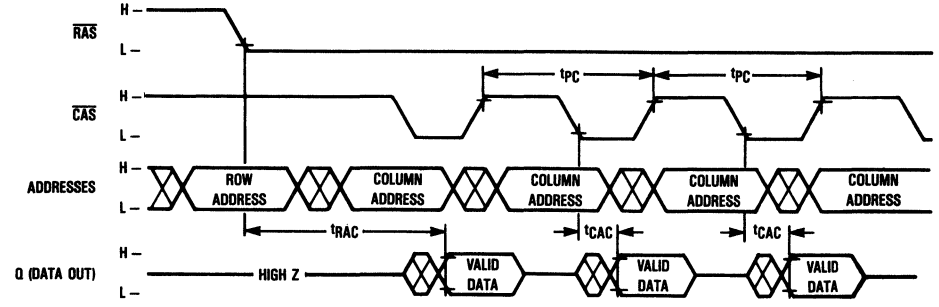

Figure 1a. Page Mode Read Cycle

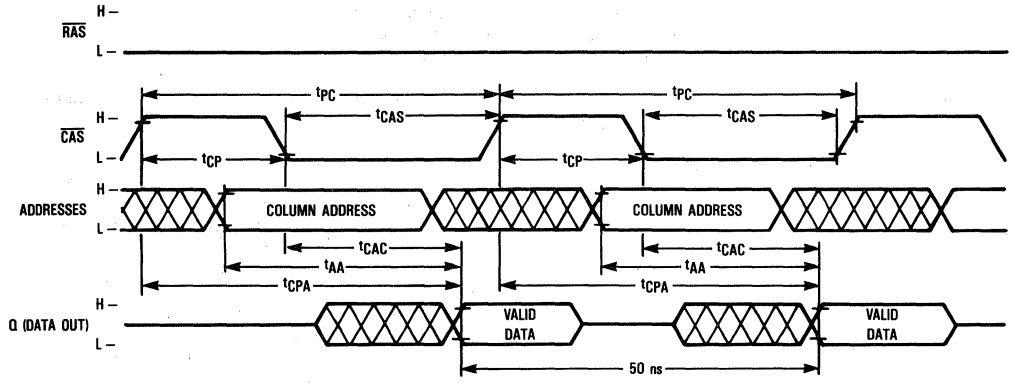

Figure 1b. Page Mode Cycle Minimum Timing

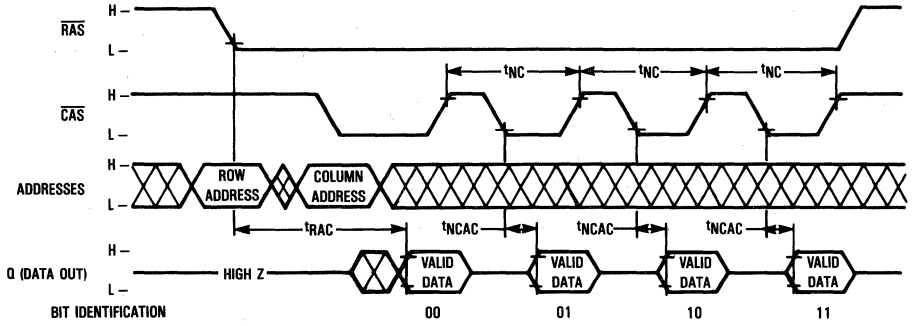

Figure 2a. Nibble Mode Read Cycle

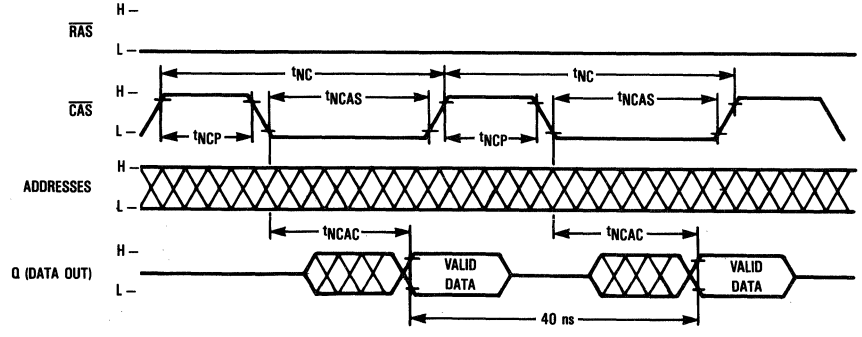

Figure 2b. Nibble Mode Cycle Minimum Timing

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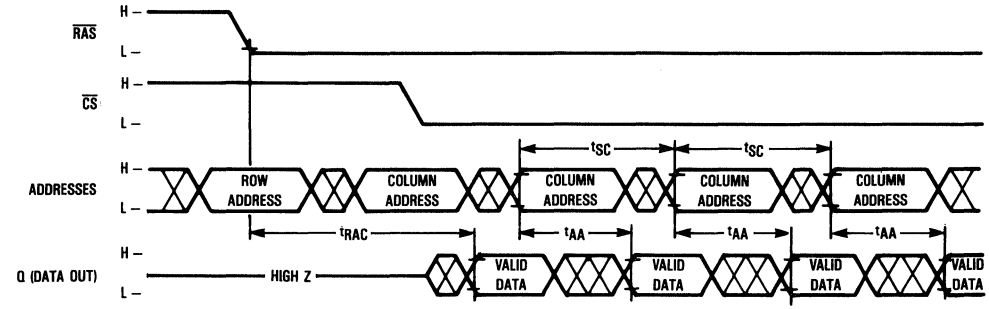

Figure 3a. Static Column Mode Read Cycle

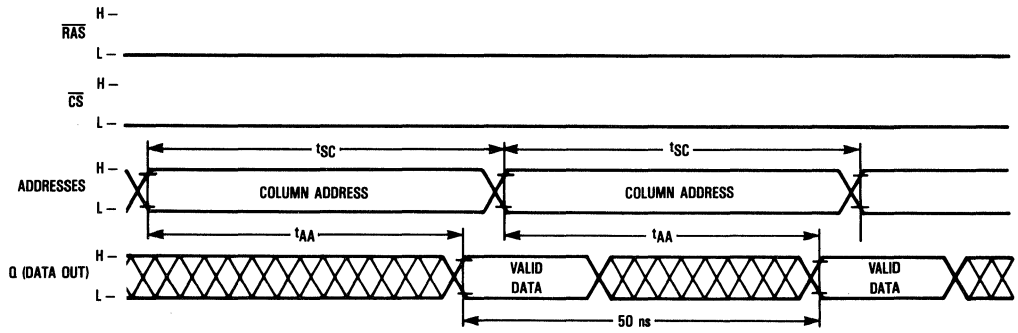

Figure 3b. Static Column Mode Cycle Minimum Timing

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Pseudo Static RAM Simplifies Interfacing With Microprocessors

INTRODUCTION

This application note describes Motorola's 128Kx8 pseudo static RAM (PSRAM), the MCM518128, and its implementation in an MC68000 microprocessor system. PSRAMs provide the low cost, high density memory of a dynamic RAM (DRAM), while also having the byte wide I/O and non-multiplexed addressing of a static RAM (SRAM). Since the PSRAM uses the same bit cell structure as a DRAM, the normal memory operation must be periodically interrupted so that the memory array can be refreshed.

PSRAM OPERATION

Refresh Modes

For the MCM518128, refreshing is accomplished by accessing each one of the 512 rows of the array, one row at a time. Each row must be accessed every 8 milliseconds to ensure data integrity. Motorola's MCM518128 PSRAM features three different refresh modes: chip enable only refresh, auto refresh, and self refresh.

The **chip enable only refresh** occurs any time a valid row address (A0–A8) is present and the device switches from standby to active for a period of one chip enable pulse width (t_{CE}), see Figure 1. Therefore, any time a read or write occurs, a row is refreshed when the chip enable transition latches in the address. This makes chip enable refresh useful for a distributed refresh operation. By accessing a different row every 15.6 microseconds (8 milliseconds per 512 rows), the entire array is refreshed.

The **auto refresh** occurs when the part is disabled by either $\overline{E1}$ going high or E2 going low and then toggling the refresh pin $\overline{F}$ (see Figure 2). Each time the refresh pin toggles, an internal row address counter is incremented, and a new row is refreshed. This makes the auto refresh mode suitable for a burst refresh operation, wherein the entire array is refreshed at one time by clocking $\overline{F}$ 512 times. The auto refresh mode of the PSRAM is most versatile in that a distributed refresh can also be performed. If every 15.6 microseconds the device is placed in standby and $\overline{F}$ is clocked once, the refresh requirements of the PSRAM can be met. The advantage of auto refresh over chip enable only refresh is that no addresses need be supplied, addresses are kept track of by the internal counter. All timing parameters associated with the auto refresh mode must be kept for proper device operation. A burst refresh of the entire array would be accomplished in 66.7 microseconds (t_{RFD}+512 rows x t_{FC}+t_{RHC}). A distributed refresh of a single row is accomplished in 185 nanoseconds (t_{RFD}+t_{FC}+t_{RHC}).

The **self refresh** occurs if the device is in the standby mode for more than 8 microseconds (t_{FAS}), and the $\overline{F}$ pin is clocked low a time t_{RFD} after the device is initially disabled (see Figure 3). The device will not change from standby to self refresh unless this $\overline{F}$ transition occurs. After t_{FAS}, an internal clock starts and a refresh cycle is performed approximately every 150 microseconds. This makes the self refresh ideal for long standby periods, as would occur during a battery backup. To refresh the entire array during a self refresh takes 76.8 milliseconds (t_{RFD}+t_{FAS}+512 rows x 150 microseconds+t_{FRS}+t_{RHC}).

Read and Write Operations

During read and write operations, the chip enables of the PSRAM must latch in the valid address. This differentiates the pseudo static RAM from a fully static RAM. The $\overline{E1}$ and E2 chip enable pins of the PSRAM are therefore analogous to RAS and CAS of a DRAM. But unlike a DRAM, the PSRAM has separate row and column address pins, so the address is latched in with a single chip enable transition. For this reason, the read operation of the PSRAM is comparable to the page mode operation of the DRAM (see Figure 4). During the write operation of the PSRAM, the chip enables operate in the same manner as they did for the read operation (see Figure 5).

PSRAM SYSTEM CONFIGURATION

Figure 6 shows the conceptualized system interface between an MC68000 microprocessor and four banks of MCM518128 PSRAMs that provide a one megabyte deep system architecture. This system is interfaced much as if it were using DRAMs for the memory, except that the costly DRAM controller is not necessary. The logic necessary for the timing controller and refresh timer is also simpler in a PSRAM system than in a DRAM system. Since the state machines used in this logic will vary greatly depending on the specific system application, it is left to the users to design according to their own needs.

Bank Select

In the system illustrated, addresses A17 and A18 generate the chip enable signals going to the E2 pin of each bank. Chip enable $\overline{E1}$ is tied active low in the system shown, with E2 controlling the memories. The upper and lower data strobes $\overline{UDS}$ and $\overline{LDS}$ are used in generating the $\overline{W}$ signals for writing data to the upper and lower byte. The output enable signal $\overline{G}$, in combination with the chip enable signals, selects the bank being read.

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The bank select and timing controller can be made using programmable logic sequencers and arrays for system flexibility. Figure 6 is drawn to illustrate that the same PAL could be used for both the bank select and timing controller, but the number of actual devices used to construct the logic will vary depending on the depth of the memory and the complexity of the state machines.

Refresh Timer

The refresh timer signals the timing controller whenever it is time to execute a refresh cycle by means of the refresh request signal $\overline{\text{REFREQ}}$. The PSRAM must have each of its 512 rows refreshed every 8 milliseconds which implies that a row must be accessed every 15.6 microseconds for a distributed refresh, or a minimum of 66.7 microseconds for a burst refresh. Therefore, during a distributed refresh, using a 12.5 MHz system clock, the refresh timer requires a division factor of 195 to minimize the time the processor is in a wait state.

During a distributed refresh, the $\overline{\text{REFREQ}}$ signal is generated every 195 clock cycles and remains active low until the refresh complete signal RFC is returned by the timing controller. The division factor will have to be adjusted accordingly if different clock rates or memory sizes are used. The logic can be simplified if the refresh is done more frequently, but on a 2^n clock cycle, such as 128. It is important that the refresh timer not stop, so that the 8-millisecond PSRAM refresh requirement is maintained.

The refresh timer is most easily realized using an inexpensive 8-bit counter, but programmable logic may also be utilized depending on the system requirements.

Timing Controller

The timing controller arbitrates between the memory refresh cycles and the microprocessor access cycles. In the illustrated system, it also toggles the refresh pin $\overline{\text{F}}$ for use of the auto refresh mode, although this could also be accomplished by means of a separate timer/counter. The timing controller also transmits the chip enable signals from the bank select. During a refresh cycle, the timing controller will manipulate the chip enables in a manner appropriate to the refresh mode being employed.

For memory/MPU arbitration, the timing controller is a state machine, achievable through the use of a programmable sequencer. When the $\overline{\text{REFREQ}}$ signal is received from the refresh timer, the timing controller will perform a refresh immediately, if the MPU is not in the middle of an access cycle. If the MPU is performing an access cycle, the refresh is delayed until the access cycle is complete. If the MPU attempts an access during the refresh cycle, an internal register in the timing controller is set, and the access is made as soon as the refresh cycle is complete.

The address strobe signal $\overline{\text{AS}}$ from the MPU tells the timing controller that an access has been requested. An unused high order address could also be used to inform the timing controller whether the access cycle is a memory access or an I/O access. During read or write cycles, the timing controller sends $\overline{\text{DTACK}}$ low, telling the MPU that the data transfer is completed.

When a refresh cycle is ready to begin, the MPU is sent into a wait state by the timing controller's forcing $\overline{\text{DTACK}}$ high. The timing controller then continues its refresh sequence, sending the chip enable and refresh signals to the memory array, according to the refresh mode being used. For example, the memories are placed in standby and $\overline{\text{F}}$ is toggled if an auto refresh is being performed.

After the refresh is complete, the RFC signal tells the refresh timer to send $\overline{\text{REFREQ}}$ high, and normal MPU access may resume.

SUMMARY

The pseudo static RAM (PSRAM) offers system designers an affordable and easily implemented solution to their memory requirements. The PSRAM combines the low cost, high density array of the DRAM with the direct addressing and byte wide data transfer of the SRAM. This results in simplified control logic, less board space, reduced design time, and a significant overall cost savings.

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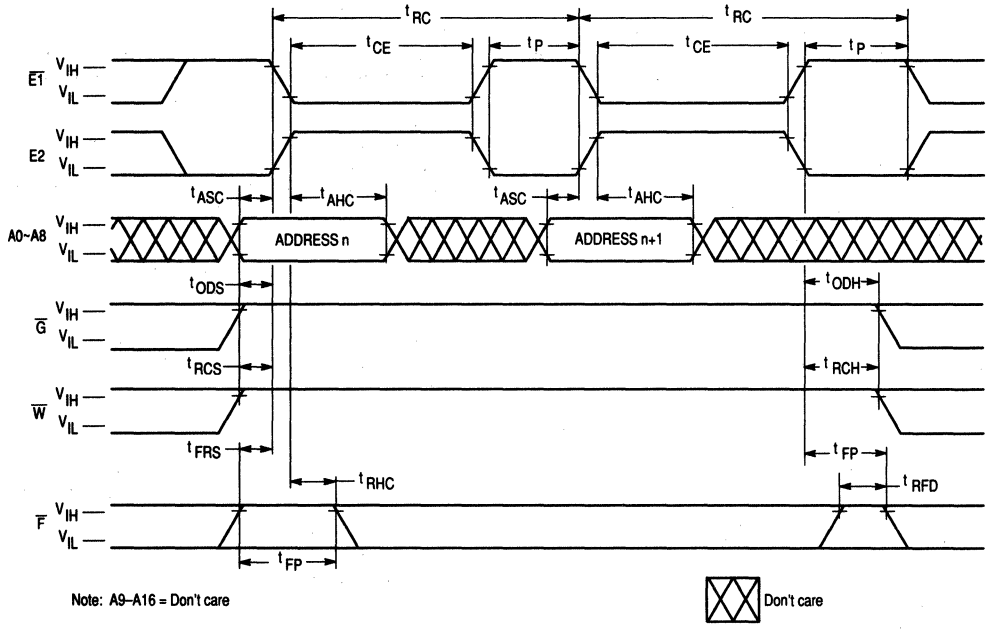

Figure 1. Timing diagram for the chip enable only refresh mode of the MCM518128 PSRAM. The illustration shows the chip enables latching in two row addresses, thus refreshing two rows of the array. Note that the refresh pin $\overline{F}$ need not clock in this refresh mode. The device can be operated by cycling $\overline{E1}$ (or E2) only, provided that E2 (or $\overline{E1}$) is tied active high (or low). This is true for all modes of operation, including read and write.

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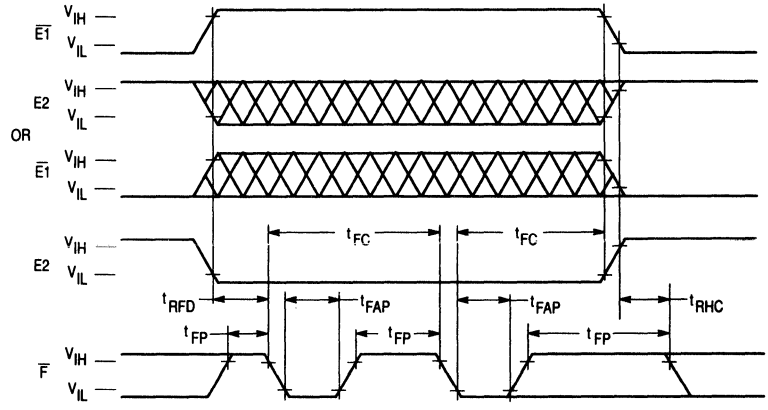

Figure 2. Timing diagram for the auto refresh mode of the MCM518128 PSRAM. In the illustration, $\overline{F}$ is clocked twice in order to refresh two rows of the array

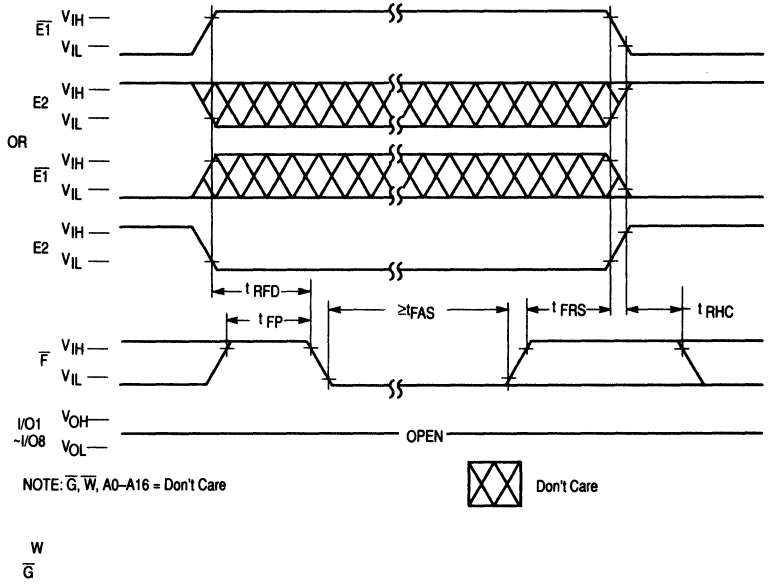

Figure 3. Timing diagram for the self refresh mode of the MCM518128 PSRAM. The recommended operating conditions for the device must be maintained for proper operation in a battery backup application.

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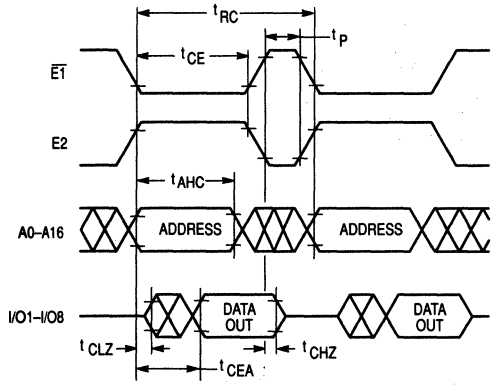

Figure 4. Minimum read cycle timing for reading data from two addresses of the MCM518128 PSRAM. In this example, $\overline{G}$ is held at V_{IL} and $\overline{W}$ is held at V_{IH}. The refresh pin $\overline{F}$ is a don't care during time t_{CE}, but must not clock during time tp. Regardless of the mode of operation, address inputs are latched by $\overline{E1}$ going low, or E2 going high.

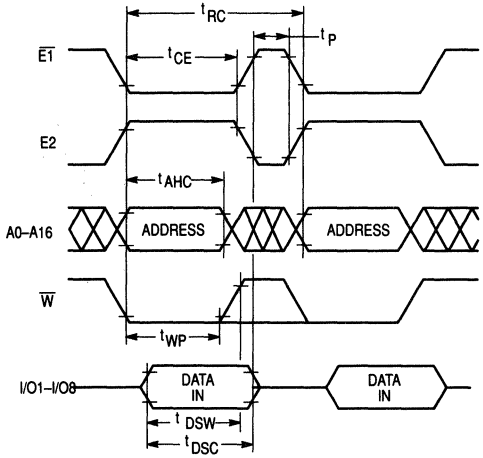

Figure 5. Minimum write cycle timing for writing data to two addresses of the MCM518128 PSRAM. In this example, $\overline{G}$ is held at V_{IH}. The refresh pin $\overline{F}$ is a don't care during time t_{CE}, but must not clock during time tp. In write cycles, the input data is latched at the earlier of $\overline{W}$ going high, $\overline{E1}$ going high, or E2 going low.

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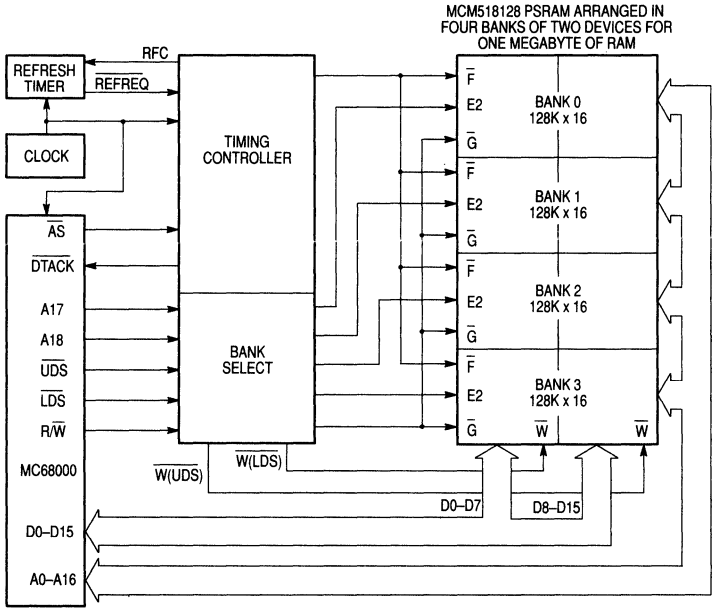

Figure 6. Block diagram shows the necessary components to Interface an MC68000 microprocessor to an array of MCM518128 128Kx8 PSRAMs giving a total of one megabyte of RAM.

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Avoiding Bus Contention in Fast Access RAM Designs

INTRODUCTION

When designing a bus oriented system, the possibility of bus contention must be taken into consideration. Bus contention occurs when two or more devices try to output opposite logic levels on the same common bus line.

This application note points out common causes of bus contention when designing with fast static random access memories and describes ways to eliminate or reduce contention.

WHAT CAUSES BUS CONTENTION?

The most common form of bus contention occurs when one device has not completely turned off (output in a high-impedance state) before another device is turned on (output active). Basically, contention is a timing overlap problem that results in large, transient current spikes. These large current spikes not only generate system noise, but can also affect the long term reliability of the devices on the bus (see Figure 1).

BUS CONTENTION AND FAST STATIC RAMs

Since memory devices are primarily used in bus oriented systems, care must be taken to avoid bus contention in memory designs. Fast static RAMs with common I/O data lines (or any high frequency device with common I/O pins) are the most likely candidates to encounter bus contention. This is due to the tight timing requirements that are needed to achieve high-speed operation. If timing control is not well maintained, bus contention will occur. The most common form of bus contention for memories occurs when switching from a read mode to a write mode or vice versa.

SWITCHING FROM A READ TO WRITE MODE

With $\overline{E}$ low (device selected), on the falling edge of $\overline{W}$ (write asserted) the RAM output driver begins to turn off (high-impedance state). Depending on the input and output logic levels, if sufficient time is not allowed for the output to fully turn off before an input driver turns on, bus contention will occur (see Figure 2a).

Figure 2a shows an example of a RAM trying to drive a bus line low while an input driver is trying to drive the line high. If the situation were reversed (RAM output high and the input driver low), bus contention would still exist.

Of course the obvious way to avoid this type of bus contention is to make sure that the input buffer is not enabled until the write low to output high-impedance (t_{WLQZ}) time is satisfied (see Figure 2b). This specification is usually given on most manufacturers' data sheets.

Another method to eliminate bus contention would be to use $\overline{E}$ to deselect the RAM before asserting $\overline{W}$ (low). This allows the RAM output extra time to go into high-impedance state before the input driver is enabled. $\overline{E}$ and $\overline{W}$ are later asserted low to begin a write cycle (see Figure 2c).

SWITCHING FROM A WRITE TO A READ MODE

With $\overline{E}$ set low (device selected), on the rising edge of $\overline{W}$ (write terminated) the address or data-in changes before the device has had a chance to terminate the write mode. If this should occur, and depending on the input and output logic levels, a bus contention situation could exist (see Figure 3). To avoid address changing type bus contention requires that the address not change till the write recovery specification (t_{WHAX}) is satisfied. To avoid bus contention caused by data changing requires that the data-in remains stable for the duration of the data hold specification (t_{WHDX}). Most of

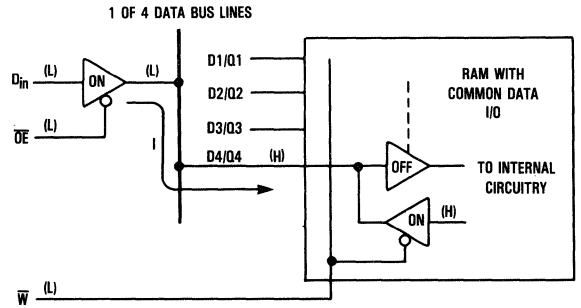

Figure 1. Common I/O Bus Contention

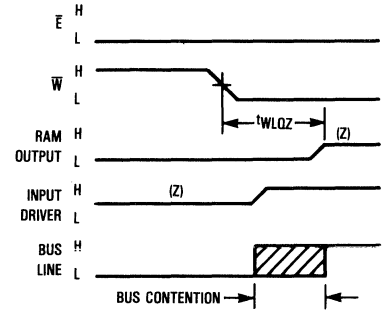

Figure 2a. Input Driver Enabled Prior to Disabling RAM Output

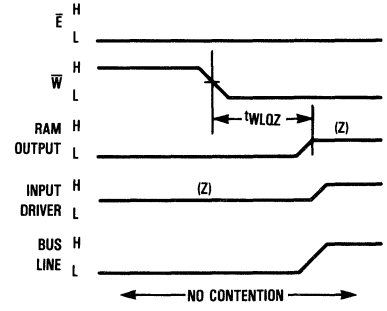

Figure 2b. Input Driver Disabled Prior to Enabling RAM Output

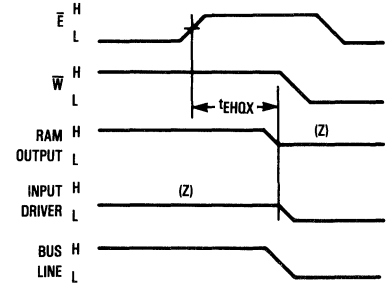

Figure 2c. Using Ē to Avoid Bus Contention

Motorola's fast static RAMs specify write recovery and data hold times of 0 ns. However, it is always a good practice to allow some margin to take care of possible race conditions.

Both of these types of contention could also be avoided by taking Ē high prior to taking W̄ high. This will give the RAM output driver time to go to a high-impedance state before W̄ goes high. In this case Ē is used to terminate the write cycle instead of W̄ (see Figure 3c).

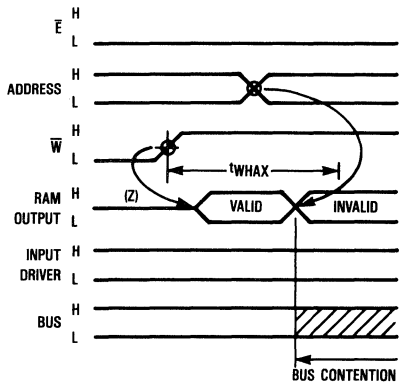

Figure 3a. Data Setup Time Violation

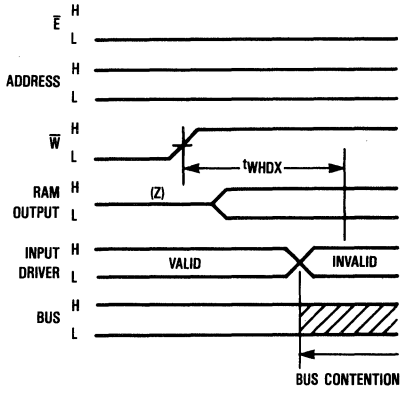

Figure 3b. Data Hold Time Violation

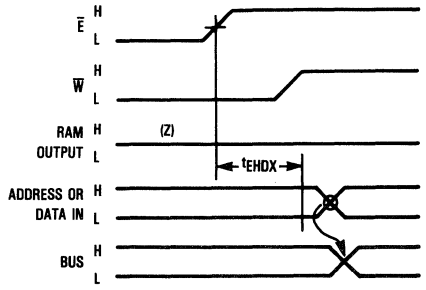

Figure 3c. Using Ē to Avoid Bus Contention

OTHER WAYS TO ELIMINATE BUS CONTENTION

If the RAM has an output enable pin (Ḡ), synchronizing schemes can be incorporated to help eliminate bus contention. Taking Ḡ high will ensure that even when the RAM is in a read mode the output will be in a high-impedance state. This will allow the input driver to be enabled longer.

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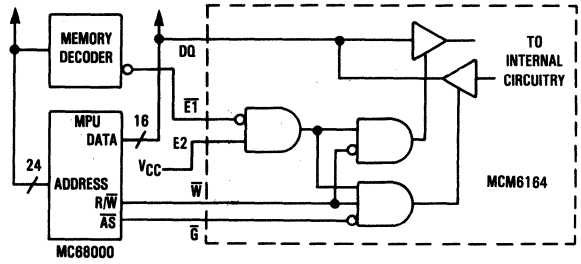

Figure 4a. Using $\overline{G}$ to Avoid Bus Contention

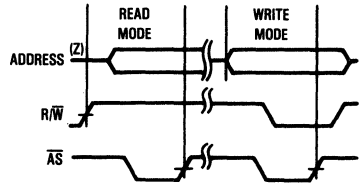

Figure 4b. Timing Diagram of the MC68000

Most advanced microprocessors, such as the MC68000 and MC68020, have asynchronous bus control signals that take advantage of fast memory devices with output enable pins. Figure 4 shows one way to avoid bus contention using a Motorola MC68000 interfaced to a Motorola 45-ns MCM6164.

A more obvious way to eliminate bus contention is to use slow memory devices. Slow memories have loose timing requirements that allow devices to fully turn off before another device turns on. Of course this defeats the whole purpose of fast static memory devices.

Another obvious way to eliminate bus contention is to use memory devices that have separate data I/O pins. In this way the R/$\overline{W}$ signal from the microprocessor can control a buffer device to eliminate bus contention (see Figure 5). However, the industry is demanding RAM with common I/O because these devices cost less and save system real estate.

Common I/O devices reduce package size since fewer pins are needed. Smaller packages result in less PCB space requirement. Common I/O devices also eliminate the need for an extra buffer with its associated expense and space requirement. In general fast static RAMs configured greater than a X1 will have common data I/O pins.

Another popular way to reduce bus contention is to put a current limiting series resistor on each bus line (see Figure 6). The series resistor does not eliminate bus contention, but it helps reduce the large transient currents associated with bus contention. However, series resistors increase access time as well as increasing component count. The added access time depends on the total bus capacitance (including the capacitance of the devices on the bus) and the total bus resistance. The added delay should be added on to the point at which bus contention ceases. The following formulas can be used to determine the added access delay.

$$t_{HL} = R_L \cdot C_L \cdot \ln \frac{V_{in}(initial) - V_{in}(final)}{V_{IL}(max) - V_{in}(final)}$$

$$t_{LH} = R_L \cdot C_L \cdot \ln \frac{V_{in}(final) - V_{in}(initial)}{V_{in}(final) - V_{IH}(min)}$$

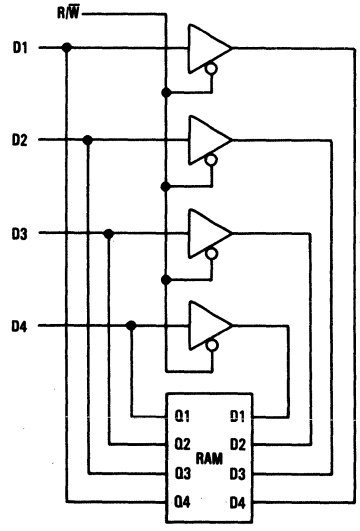

Figure 5. Separate I/O Buffer

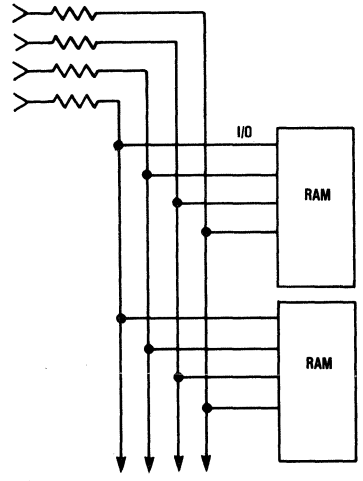

Figure 6. Using Series Terminating Resistors

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Generally the value of the resistor should be around 100 ohms. The larger the resistor the less the transient current generated, but the greater the delay. Using a 150-ohm resistor will limit the current flow to less than 20 milliamperes while adding approximately 3 nanoseconds extra access time. However, note that even with series resistors bus contention duty cycle must be minimized to reduce EMI and bus ringing.

Although it is very important to reduce bus contention, CMOS memories can tolerate more bus noise generated by bus contention than can bipolar memories, due to the excellent noise immunity advantage of CMOS over bipolar technology. However, even when using CMOS memories, large destructive transient currents generated by bus contention can still occur.

CONCLUSION

Bus contention must be taken into consideration in most bus-oriented system design. The occurrence of bus contention generates large transient currents that produce system noise and could also affect the system's long term reliability.

Fast random access memories with common data I/O pins are very susceptible to bus contention due to tight timing requirements. Although it is almost impossible to totally eliminate bus contention, it must be the goal of the system designer to minimize bus contention.

AN973

Avoiding Data Errors with Fast Static RAMs

Microprocessors are now capable of 20-25 MHz. This places a great demand on SRAMs to supply super-fast access times. Today's sub-100-nanosecond SRAMs in production are rapidly moving to sub-50 nanoseconds as yesterday's prototypes ramp into production, and sub-25 nanoseconds is just on the horizon. This need for high-speed SRAMs is amplified by the fact that setup, hold times, and cycle edge accuracies do not usually improve at the same rate as the clock frequency. There is help on the way in terms of application specific SRAMs that put on chip some of the "glue" features that eliminate gate delays caused by decoders, drivers, or clock signals; but for now, the main burden will fall upon SRAM designers to make up for the "lost time" in the shorter cycles. Some of the tools of the SRAM designer are improved processes, tighter design rules, and improved circuit techniques such as address transition detection. When you combine all of these features into a high performance SRAM, you no longer have the bistable flip-flop of yesterday but a highly tuned circuit that is more closely related to a DRAM. This is where the system designer can help. Although SRAM designers are doing everything possible to make the devices stable and noise immune, there is no substitute for a good solid system layout and design. The following discussion gives system designers some insight into potential trouble areas from a component engineering viewpoint.

CHARACTERISTICS OF HIGH-SPEED BUSES

When data is transmitted over long distances, the line on which the data travels has to be considered a transmission line. A long distance is relative to the rate at which data is being toggled. Address and data buses associated with high-throughput microprocessors (e.g., M68000 family) must also be thought of as transmission lines, since it is not uncommon for these processors to run bus cycles of 40-nanosecond periods or less.

Other features of high-end microprocessor buses are that they tend to operate in harsh, noisy-type environments, and most of these buses are unterminated. A high-impedance, unterminated bus line acts just like an antenna. It not only radiates EMI, it can also receive EMI: This can result in bus ringing, crosstalk, and various other noise associated problems. The more transmission lines a bus has, the more antennas to pick up and radiate noise. Of course, the best way to reduce this EMI is to ensure that the bus is properly terminated into a low-impedance load. This low-impedance load could be in the form of a pull-up or pull-down resistor tied to each bus line. Ideally, the termination resistor should be equal to the characteristic impedance of the bus line. A transmission line terminated into its own characteristic impedance has the best incident wave switching as well as the least amount of reflection.

Since an unterminated bus looks almost entirely like a capacitive load, the larger the resistor value the slower the rate at which data can be presented to the receiving device. This is due to the time it takes to charge and discharge this capacitive line through the termination resistor. If a small value resistor is used, the charging/discharging time delay can be minimized (t = RC). However, the smaller the resistor the greater the power consumption through the resistor. Also, if the resistor value is too small, its value will approach that of the source resistance of the transmitting device, which could lead to a degradation of noise margin to the receiving devices. A resistor value between 1 kilohm and 10 kilohms is usually adequate. The actual value should be optimized through experimentation (see Figure 1).

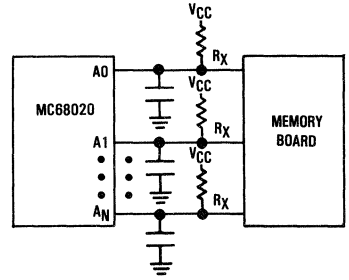

Figure 1. Microprocessor Address Bus with Pull-Up Resistors

HIGH SPEED SRAM DESIGN TECHNIQUES

In order to speed up access times of high-speed RAMs, many new design techniques have surfaced. One of the most innovative techniques to emerge is known as address transition detection (ATD) circuitry. Since row address access times are typically slower than column address access times, this circuitry originally used the row addresses to trigger a clocking sequence that restored bit lines, shorted data lines, equalized sense amplifiers, and threestated the output as the output buffers were equalized. This meant that many of the internal transistions could be completed by the time that the signals were decoded and propagated through the device seeking the proper cell and outputting data. This then made row and column access times much more equal and eliminated one of the speed bottlenecks. This scheme also has the added advantage of reducing power consumption because the static bit line loads can be reduced in size by utilizing a parallel equalization that is also generated at the ATD initiation and used to pull up the bit line 0 before selection of the new word line. Since

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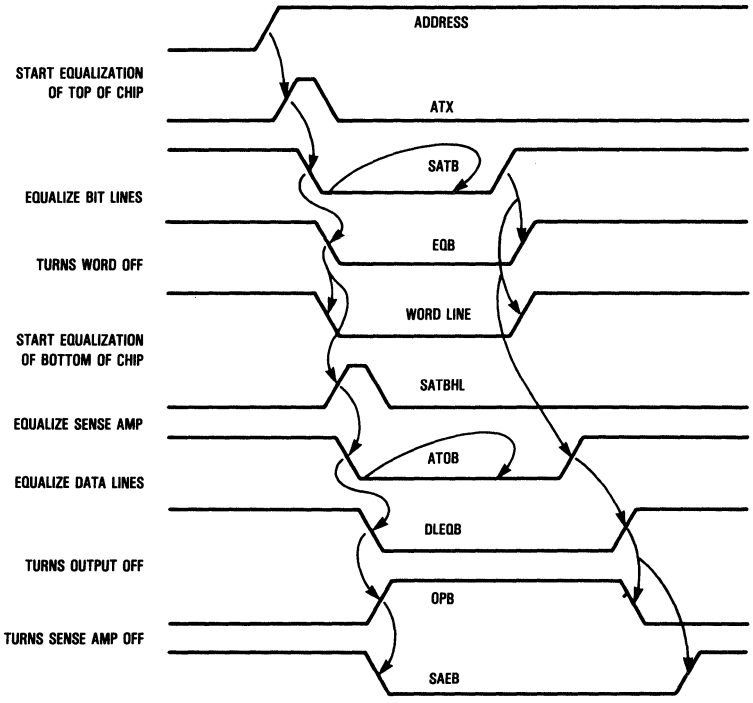

Figure 2. Address Transition Detection Timing Chain

its inception, ATD has been expanded and is now activated by all addresses and chip select pins instead of just row addresses. A typical timing chain, as shown in Figure 2, applies to Motorola's MCM6164 8K×8 SRAM and exemplifies the clock sequence dependency.

ATD has been shown to be very effective as a performance enhancer and will remain a valuable tool for designers, but it can be seen that we now essentially have a clock-activated part. What happens if addresses are floated or oscillate at a frequency greater than the ATD response? What happens if addresses are skewed, thereby getting successive ATD initiations? There is also the case of signals being gated from numerous sources, in which the address may start in one direction and then reverse several times before it finally seeks a valid high or low level. Circuit designers believe that these potential problems have been resolved over the last few years as testing techniques and circuit simulations have wrung out the infinite number of application variations. However, there is a simple, foolproof way that system designers can eliminate any potential for this type of a problem. Deselect the device during address transitions (see Figure 3).

Since new design techniques have made chip select access times equal to address access times, system designers can take advantage of this and improve reliabilty of their system by increasing overall immunity to a noisy environment. This can cover a host of potential board-induced problems from oscillating multiplexer or driver units, to spurious address glitches put out by MPUs.

Another design improvement is related to rise and fall times on the output levels, known by circuit designers as di/dt. This is the inductance associated with the changing current as loads are charging and discharging. This inductance is coupled back to the device, and through connections and bus resistance can cause the power supply or ground to change drastically. This is pushed to the limits as output drivers become more powerful, and is especially aggravated by multiple I/O devices like byte-wide SRAMs which may have all eight data lines switch from all 0s to all 1s or vice versa. These spurious noise spikes on the power lines can affect the data contents of the device, as well as any other device sharing the same power and ground buses (see Figure 4). Circuit designers have developed circuitry that has a feedback loop that controls the rise and fall time just enough to minimize overshoot, undershoot, and ringing. This di/dt is the inherent reason why byte-wide SRAMs are typically 4–5 nanoseconds slower than single output devices.

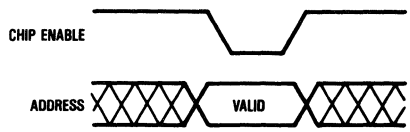

Figure 3. Deselection of Device During Address Transition

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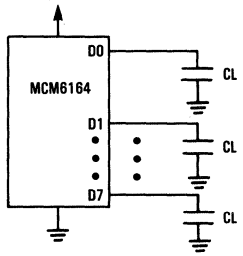

Figure 4a. MCM6164C Data Bus

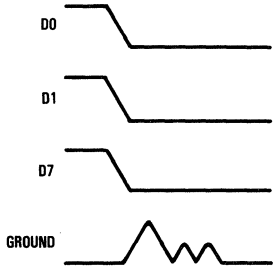

Figure 4b. Ground Bounce When Data Switches from All 1s to All 0s

PCB POWER FEED CONSIDERATIONS

Another source of noise can be inadequate power feeds and power supply decoupling. Large ground planes should be used to reduce both inductances and resistances. The resistances of the power supply lines should be less than 0.1 ohm. If the inductances or resistances of the power supply lines become significant, V_{CC} or ground bounce can occur. Since all inputs are referenced to ground, gate input thresholds could be exceeded, causing data errors to be generated. An excellent PCB design is one that incorporates a multilayer board. One layer should be entirely devoted to a ground plane.

The use of good-quality decoupling capacitors can help to keep noise off the power lines. A value between 0.01 microfarad and 0.1 microfarad (use 0.1 microfarad for ×8 organizations) should be used for each RAM. This capacitor should be located as close to the RAM power pins as possible. When using IC sockets, it is recommended that sockets with gold-plated copper contacts and built-in decoupling capacitors be used.

A large value capacitor (≥1 microfarad) should be used on each V_{CC} line. The purpose of this capacitor is to provide for sudden current demand (current surges) from the power supply.

Figure 5 illustrates a typical memory board design.

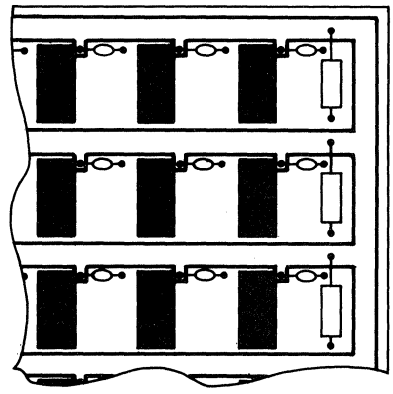

Figure 5. Typical Memory Board

SUMMARY

Digital transmission line theory must be taken into account when designing high-frequency buses. A high-impedance, unterminated bus behaves much like an antenna, receiving as well as transmitting EMI. The use of termination resistors on these buses can reduce EMI. Many innovative designs have evolved to speed up access times of fast static RAMs. One of the more innovative designs is that of address transition detection circuitry. Most high-speed RAMs today use this technique to decrease access time. Good PCB power feed design, as well as the judicious use of decoupling capacitors, is essential for optimum performance from fast static RAMs.

Much of the time, the problems caused by a marginal device, system layout, or pushing for the last nanosecond is an intermittent random type of problem that could result in either destroyed data or access time push-out. If you are having a problem, call Motorola MOS Memories in Austin, Texas, (512) 928-SRAM (928-7726). We are on your design team!

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AN984

25 MHz Logical Cache for an MC68020

Prepared by:
Motorola — East Kilbride, Scotland

INTRODUCTION

As the speed of the MC68020 processor increases it becomes more difficult and more expensive to provide large amounts of no-wait states memory. The addition of a logical cache in a memory management based system then becomes a more viable alternative to the problem. For a typical 25 MHz MC68020 system the incorporation of a no-wait states cache is one of the most economical ways in which the true performance attainable from this particular processor can be achieved.

CACHE DESCRIPTION

The cache described in this application note is a 32K byte (8K long words) direct mapped logical cache. The cache is organized such that both supervisor and user, program and data accesses are stored. The entries are tagged appropriately with the function code lines. To avoid any stale data problems that may occur with the data the cache update logic includes a 'write through' mechanism that forces any data writes to update both the memory and the cache. The cache operates with no wait states with a 25 MHz MC68020.

BLOCK DIAGRAM DESCRIPTION

The cache can be broken down into several functional parts as follows:

- tag RAMs
- data RAMs
- control logic
- entry update mechanism

The cache is organized as 8K long word entries (see Figure 1) which are referenced by a 22 bit TAG field. This TAG is made up of the upper address lines (TA15–TA31), the function codes (TFC0-2) and the size pins (TSIZE0-1). By incorporating the size pins into the TAG field means that the data entry can be validated even if it were referenced as a misaligned data transfer. The function codes allow the entries to be referenced separately with respect to user/supervisor and program and data entries.

The cache mechanism will begin operation as soon as an address becomes valid on the logical address bus. This address accesses the TAG RAM within the cache and the corresponding entry is compared with the relevant section of the logical address bus (LA15-LA31) and the control bus (FC0-2, SIZE0-1).

If this comparison is valid then this gives an indication to the comparator logic that a valid entry may be present within the cache data RAMs.

To determine whether this data entry is indeed valid a simultaneous access is made to the VALID bit RAM with the lower section of the logical address bus (LA2-LA14). If the entry in this VALID RAM is a logic 0 then this indicates that the corresponding data entry at that cache address (LA2-LA14) is a valid entry.

Access to that data item can then be made on the condition of several control signals (e.g. R/W*, CACHE-E*, etc.) and the data buffers to the system data bus will be enabled. This is termed as a CACHE HIT.

Conversely, if the entry in the VALID bit RAM was a logic 1 then this would indicate that the corresponding data item was not a valid cache entry and so the isolation data buffers would not be enabled to the system bus. This is termed as a CACHE MISS.

When the cache detects a HIT then the bus cycle is completed from the data RAMs and the system operates with no wait states.

If on the other hand the cache detects a MISS then the processor has to fetch its data from external memory which by its nature will be slower and will incur wait states.

To facilitate the data fetch from external memory the cache mechanism forces the processor to do a RETRY of the MISSed bus cycle. This retried bus cycle will then go out to external memory and fetches the relevant data item which will be latched by the processor and also used to update the cache. Subsequent accesses to this address will then find the data resident in the cache.

To preserve data integrity a CACHE MISS is also generated by a data write cycle. On writing to an address the cache forces a MISS such that the data item will be written to the cache in addition to the external memory. Subsequent data reads at this location will find that the data item is resident and is the most recent version.

Forced CACHE MISSes are also generated when the logical

address is detected as being a peripheral access (e.g. serial I/O device) or when the processor is executing a CPU space cycle (e.g. interrupt acknowledge).

CACHE CONTROL MECHANISM

The cache hit signal (CHIT*) is generated as a result of the comparison of the TAG data, the VALID bit and various control signals. When the logical address from the processor becomes valid the cache TAG RAMs are enabled and the TAG data is produced for comparison.

These TAG RAMs are addressed as an 8K long word bank and so logical address lines LA2 to LA14 are used.

The TAG RAM itself contains information relating to the bus status of the cached item. This bus status consists of a section of the logical address bus (LA15-LA31) and some control signals (FC0-2, SIZE0-1). When these TAG RAMs are accessed this previous bus status is compared with the existing bus to detect if there is a match.

Comparators U215, U216 and U217 (see Figure 4) are used to compare this information and if there is a match the outputs Oa=b (pin 19) will be asserted.

The assertion of these three comparator outputs is then conditioned by various other factors to determine whether a cache hit signal should be generated.

While the TAG RAMs are being accessed by logical address lines LA2-LA14 a VALID bit RAM is also accessed. The information contained in this VALID bit determines whether or not the cache data is valid. When the cache is enabled all the entries in the VALID RAM are set to logic 1 to indicate that there are no valid entries in the cache.

Subsequent memory accesses then cause a cache miss which results in a cache entry being made. When this cache entry is made the status of the bus (LA15-31, FC0-2, SIZE0-1) is saved in the TAG RAM at the location pointed to by the cache index (LA2-14). The information on the data bus is then saved in the data RAMs at address with cache index LA2-14 and the corresponding VALID bit entry is also set (i.e. the cache entry is marked as being valid).

Subsequent accesses to that address will then cause the TAG address comparators to assert their outputs and the VALID bit to be set. The assertion of the cache hit signal (CHIT*) is then dependent upon the status of several other control signals such as cache enable (CACHE-E*), CPU space and peripheral access (IOEN*). Accesses to CPU space are not cached because of the problems that might arise when servicing interrupts or accessing coprocessors. In addition access to peripheral devices (indicated by the signal IOEN*) are not cached because of the read write nature of some peripheral device registers.

When these signals are taken into account the resultant assertion of the cache hit signal (CHIT*) will then cause the processor to complete the bus cycle with no wait states.

Control of the cache is facilitated by three hardware primitives: Cache Enable, Cache Disable and Cache Clear. These primitives are initiated by accessing a specific address within CPU space which is not used for any other CPU space functions.

On requesting a cache enable function the mechanism causes the VALID bit RAM to be set to logic 1's, indicating no valid cache entries, and then assert the CACHE-E* signal to the rest of the system.

The cache disable function simply negates this CACHE-E* signal.

The cache clear function is included to allow the support of multi-tasking software. On initiation of the cache clear function all entries in the VALID bit RAM are cleared so emptying the cache. This is useful where the software has to perform a context switch.

CACHE CONTROL LOGIC

The Cache control logic allows the software programmer to enable the cache, disable the cache and to clear the cache contents. Accesses to the control logic can only be done under CPU space. This prevents accidentally writing to the control logic during normal operation (the SFC and DFC registers are programmed for CPU space with the MOVEC instruction, and the MOVES is used in writing to the control logic). Hence only the supervisor mode of operation can control the cache.

The address lines LA24-LA26 are used to decode the cache control functions, these being inputs fed to an 74LS138 U241 (see Figure 3). In addition to these addresses in CPU space, the programmer should also select an area of memory that will not cause contention with the normal MC68020 CPU functions.

An example decode could be $1070000 ($ is used to represent a hexadecimal number) for clear cache, $2070000 for disable cache and $4070000 for enable cache.

Cache Enable

The cache is enabled by accessing to a CPU address similar to the one given above, the data being irrelevant. On enabling the cache all entries are made invalid. This ensures that no stale data problems are created from accesses when the cache was previously enabled.

The output from U118D (see Figure 3) is used to enable a sequencer consisting of three 4-bit binary counters: U246, U247 and U248. These counters are used to increment the address bus to set the valid bits to all 1's (entry is invalid). The addresses are presented to the valid RAM U259 via the latches U249 and U250, the outputs from these being enabled at the same time as a write to enable the cache. Also during this sequence the logical address bus to this RAM is tri-stated from the RAM's address bus by U243 and U244.

Under normal operation the latches U243 and U244 are enabled and U249, U250 are disabled allowing the valid RAM to be addressed from the logical address bus. The 12-bit sequence clears 4 K entries in the cache (each entry is a long word).

The sequence is repeated twice to clear the whole 8 K entry cache. The two D-type flip flops U251B and U251A are used to write first to the upper 4 K then the lower 4 K entries.

At the end of the cache clear sequence the cache is enabled via the S-R flip flop U257D and U118C. The CACHE.E* is then used in the comparator logic to indicate that the cache is enabled. In addition the DSACK0* and DSACK1* is returned to the MC68020.

As far as the processor is concerned the cache clear mechanism can be thought of as a long instruction. The valid

RAM latches data with respect to the sequencer clock (40 MHz for 25 ns SRAM's) and a logic 1 is latched on each falling edge of this clock.

A logic 1 is written into the valid RAM when: the sequencer is enabled; it is the falling edge of the 40 MHz clock and the WRITEN* signal from the entry update mechanism is high (U258C, U263A and U219D). This logic is also used to write a logic 0 into the valid RAM during normal operation.

To prevent external bus contention when the cache is being written to, a signal ADDBUFDIS* is generated which can be used to disable external address buffers. The CMISS signal should be used to disable the external address buffers during a cache hit.

Cache Clear

The cache clear mechanism is used to allow the operating system to perform a context switch. A cache clear command will produce the same output as the enable cache command.

Using the 40 MHz clock gives a context switch time of approximately 0.025 x 1024 x 8 = 205 us. If this is unacceptable the mechanism can be speeded up by using several valid bit RAMs of lower density in parallel, or using a RAM with a clear feature.

Cache Disable

This command produces an input into U240B to set the S-R flip flop to cache disable (CACHE.E* set to a logic 1). The reset signal is also fed into U240B to ensure that the cache is always disabled at reset.

ENTRY UPDATE MECHANISM

This section of logic (see Figure 2) is used to control the cache mechanism for updating entries in the cache. In addition, the logic will produce control signals used to latch data into the Tag and Data RAMs and control the isolation data buffers for the cache (U236 - U239 in Figure 5).

The mechanism used to update the entries in the cache is only enabled on a read cycle (R/W* signal into U261D) and when the cache is enabled (CACHE.E* signal into U261C).

The control logic is required to perform three distinct operations:

- On a write cycle the WRITEN* signal should be asserted to latch data into the RAMs to perform a write through operation. When the address is next accessed it will reside in the cache.
- On a read cycle that does not generate a cache hit, the logic needs to initiate a retry operation to enable the cache to latch the data which is being read by the MC68020.
- Thirdly, on a read cycle, which causes a cache hit, the bus cycle needs to be terminated to allow zero wait state operation at 25 MHz from the cache.

Write Cycles

Assuming the cache is enabled then on a write cycle the output from U240D produces logic 0 (the output from U261C will be logic 0). This output produces a signal INHIBIT* which prevents the cache returning DSACK0*, DSACK1*, HALT* and BERR* (U256A, B, C, D), used for read cycles (see Figure 2).

A signal FORCEW* is also generated via U258B and U219C to control the output enable of the cache isolation buffers to allow data to be routed to the cache data RAMs (see Figure 5).

The WRITEN* signal is finally generated from U258A to produce the W* enable for the TAG and DATA RAMs. WRITEN* is also used to enable the buffers: U212 - U214, to route the current logical address, function codes and size lines into the TAG RAMs (see Figure 4).

Two banks of RAMs are used to obtain an 8 K entry long word cache; the lower bank of RAMs are enabled with LA14* from U255C and the upper bank is enabled by LA14. This is needed to allow 25 MHz operation (25 ns SRAM - MCM6268-25 -are used as shown in Figure 4).

On the assertion of DSACK0*, DSACK1* from the external physical memory the two D-type flip-flops U235A and U253B (see Figure 2) are used to negate the WRITEN* just after the falling edge of the processor clock S4 (just after the MC68020 latches data). On the negation of WRITEN*, tag data is written into the tag field.

The information on the data bus is latched into the cache data RAM and the tag buffers and data isolation buffers isolate the cache from the system busses. This section together with the whole entry update mechanism must operate logically very quickly hence FAST logic is used throughout.

Read Cycle with a Cache Miss

Timing diagram 1 shows the cache sequence when a cache miss occurs. From this diagram it can be seen that the addresses on the address bus do not become stable until 5 ns into S1 worst case. At this point it will take 25 ns to obtain information from the TAG data RAMs (the RAMs are permanently enabled).

In addition to this there is a delay through two levels of comparator (U215 - U218). This gives an absolute maximum propagation delay time of 46 ns after the address bus is stable before a valid CHIT* signal is generated. With the above conditions a valid cache hit signal (CHIT*) should be asserted in the middle of S3 for a TAG match. The entry update mechanism uses this information to determine if there is going to be a cache miss or a cache hit.

In the case of a cache miss the following sequence of events are executed: DSACK0* and DSACK1* are asserted by the assertion of the MC68020 AS* (U255B) by U256A and U256B as shown in Figure 2. The INHIBIT is set to a logic 1 by U261C, U261D and U262A. U252A is then used to bring U252B out of RESET on the falling edge of S2. This D-type is then used to sample the CHIT* signal in the middle of S3. In the case of a cache miss the D input will still remain high, forcing the cache miss signal CMISS to go high. This is used to enable external data buffers for the MC68020. This causes the BERR* and HALT* signal to be asserted simultaneously to request a retry cycle (via U261B, U256C and U256D). This takes advantage of the MC68020's ability to recognize a late retry if spec 27A is satisfied. (Note that

68020 inserts an additional 3 clock cycles after S5 of this cycle).

On the termination of this bus cycle all signals are negated as shown in the timing diagram, with the exception of the INHIBIT. This is because on the rising edge of LAS* the output from Q* of U269A is fed back to the input to produce a low INHIBIT signal for the following retry cycle This low INHIBIT signal prevents the DSACK0*, DSACK1*, BERR* and HALT* lines from being asserted by the cache during the retry cycle.

Timing diagram 2 shows the retry cycle. The length of this cycle is determined by the actual physical device being read so it is shown as an unknown number of wait states. The same cycle is repeated as above, however, during this cycle INHIBIT has been asserted causing FORCEW* (force a write to the RAMs) and WRITEN* to be asserted. This has the effect of updating the cache on the read cycle by forcing the cache to latch the addresses, function code and size signals to the TAG RAM and the DATA bus contents into the data RAMs.

The buffers U236 - U239 are enabled by (CHIT*) ANDed with (FORCEW*) and the direction is controlled by CHIT*. In this case CHIT* is a logic 1 causing data to be written into the RAMs. The buffers U212 - U214 are enabled by the WRITEN* signal.

On return of the DSACK0*, DSACK1* from the physical system, the WRITEN* signal is negated (via U257A, U255C, U253A, U253B, U219B and U258A) to latch data into the RAMs just after the falling edge of S4.

In addition to this all the signals are negated at the end of the cycle and the INHIBIT signal returns to a logic 1 level on the negation of LAS* (U262A and U240D).

Read Cycle with a Cache Hit

When a read cycle occurs at an address which has a corresponding input in the cache, a cache hit will occur. This cycle is similar to the one above except the CHIT* signal from the comparators U215 - U218 is asserted by the middle of S3, setting CMISS inactive (output from Q of U252B is set to a logic low) and forcing the external data buffers to be disabled preventing data bus contention. The BERR* and HALT* are also prevented from being asserted by U261B so no late retry cycle is signalled to the MC68020.

Finally, the cache data RAM isolation buffers U236 - U239 are enabled and the direction is selected to be output from the RAMs to the data bus. As there is no bus activity which stops the recognition of DSACK0* and DSACK1*, this read cycle by the MC68020 from the cache is performed in zero wait states at 25 MHz.

At the end of the cycle all the signals are negated for the next bus cycle.

CONCLUSION

The design of a 25 MHz logical data cache to interface between the processor and an MMU involves the use of very fast logic and static RAMs for zero wait state operation. The RAM access speed required in this application is 25 nS to allow no wait states operation.

The control logic has been designed discretely with FAST Schottky TTL since the use of PLAs would have a serious effect on gate propagation delay times.

The MC68020 supports a late retry cycle recognition and this is used in the design to take corrective action in the case of a cache miss.

As greater performance is required from the MC68020 the move towards high frequency zero-wait state operation becomes a more important requirement. If an MMU is placed between the processor and memory this will have an effect on zero-wait operation at the higher frequencies.

If the logical data cache can be made large enough, so that a high hit rate can be achieved, then slower physical memory could be tolerated in the system.

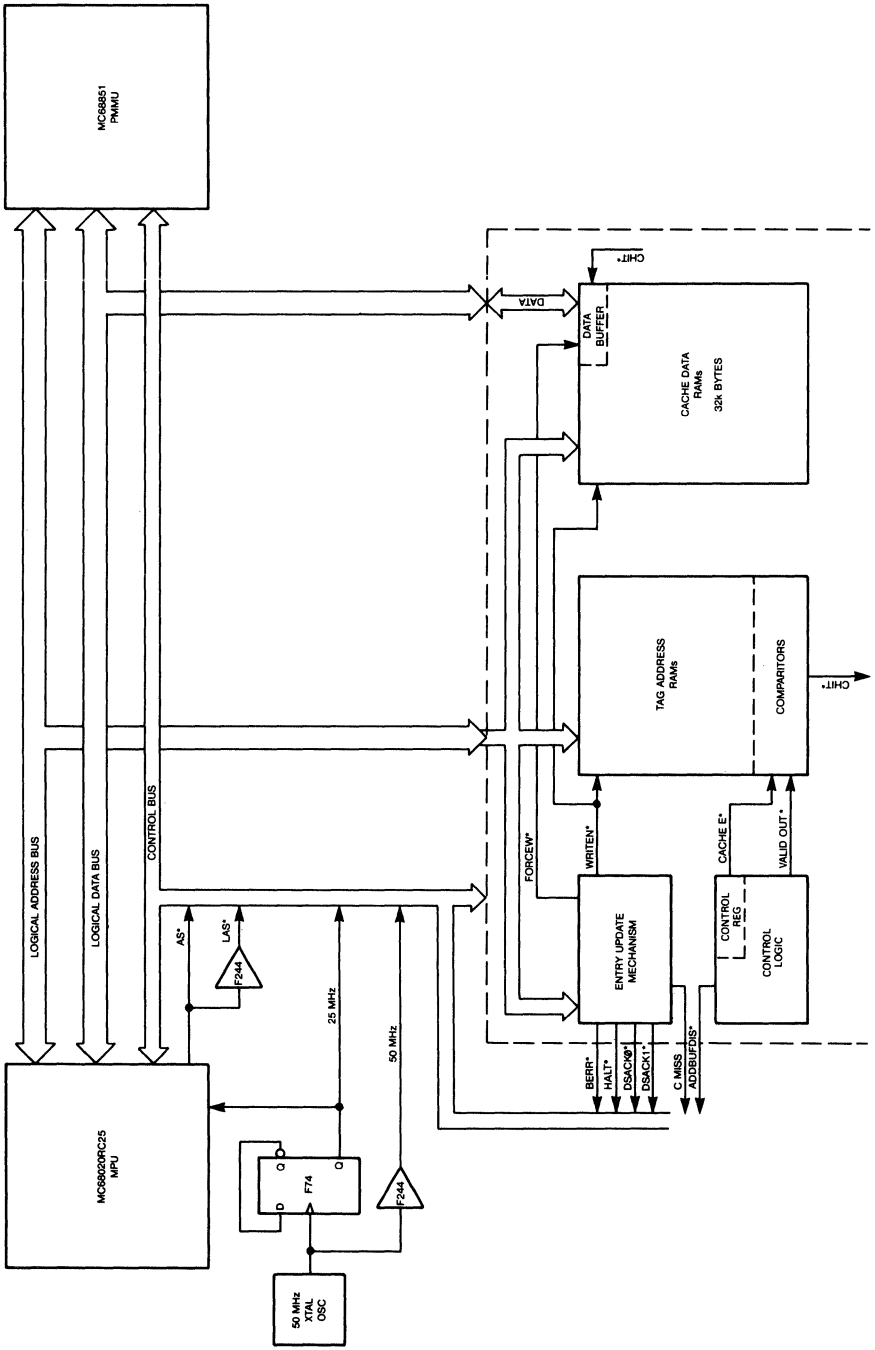

Figure 1: Block Diagram

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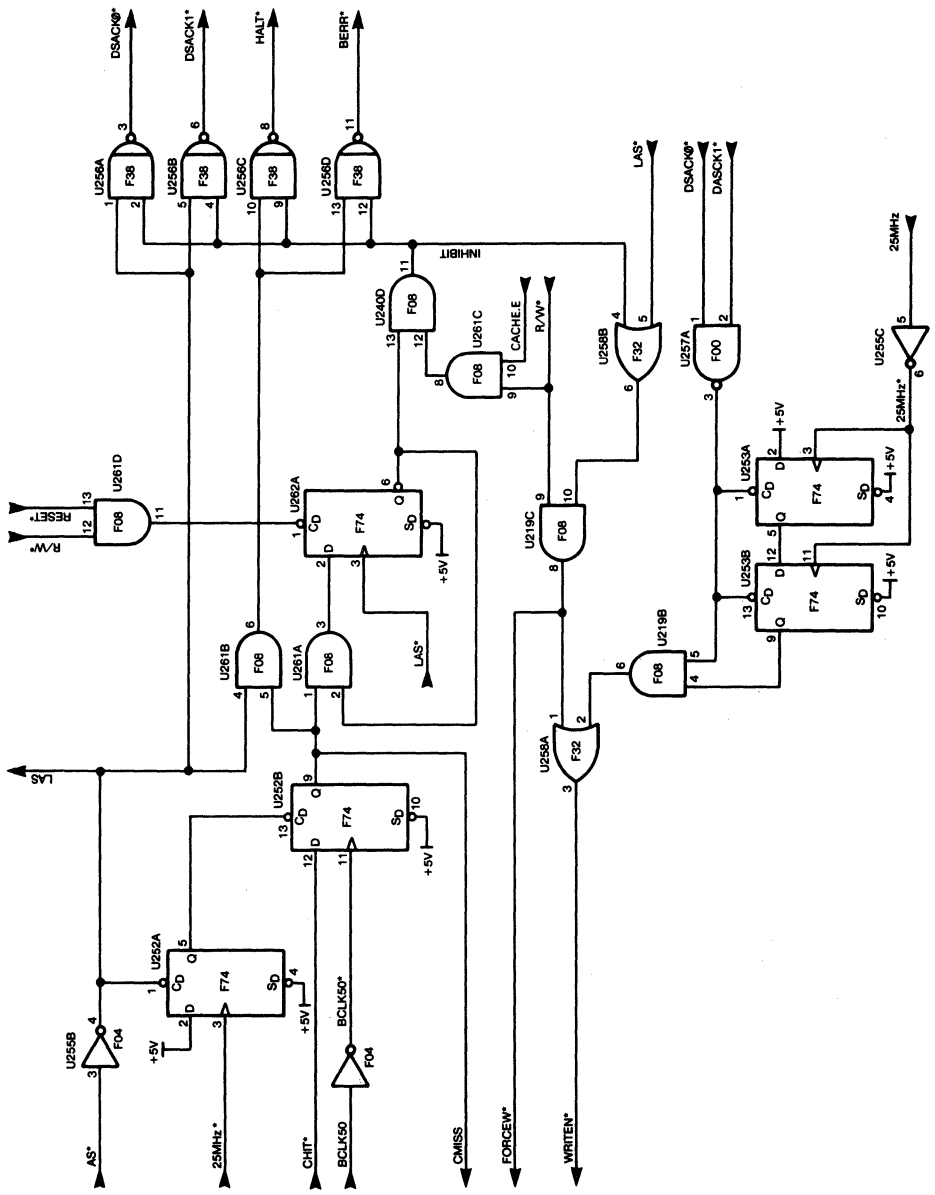

Figure 2: Entry Update Mechanism

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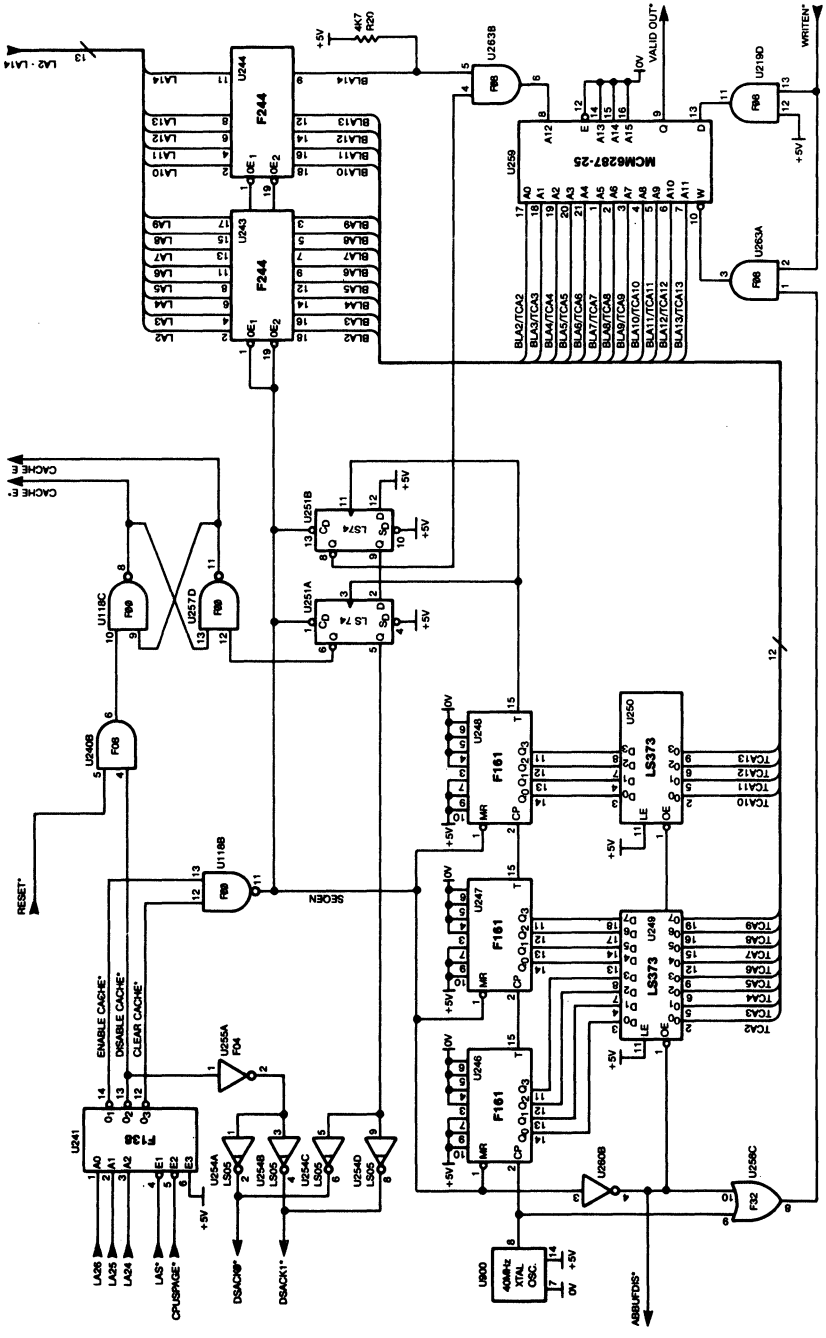


Figure 3: Control Logic

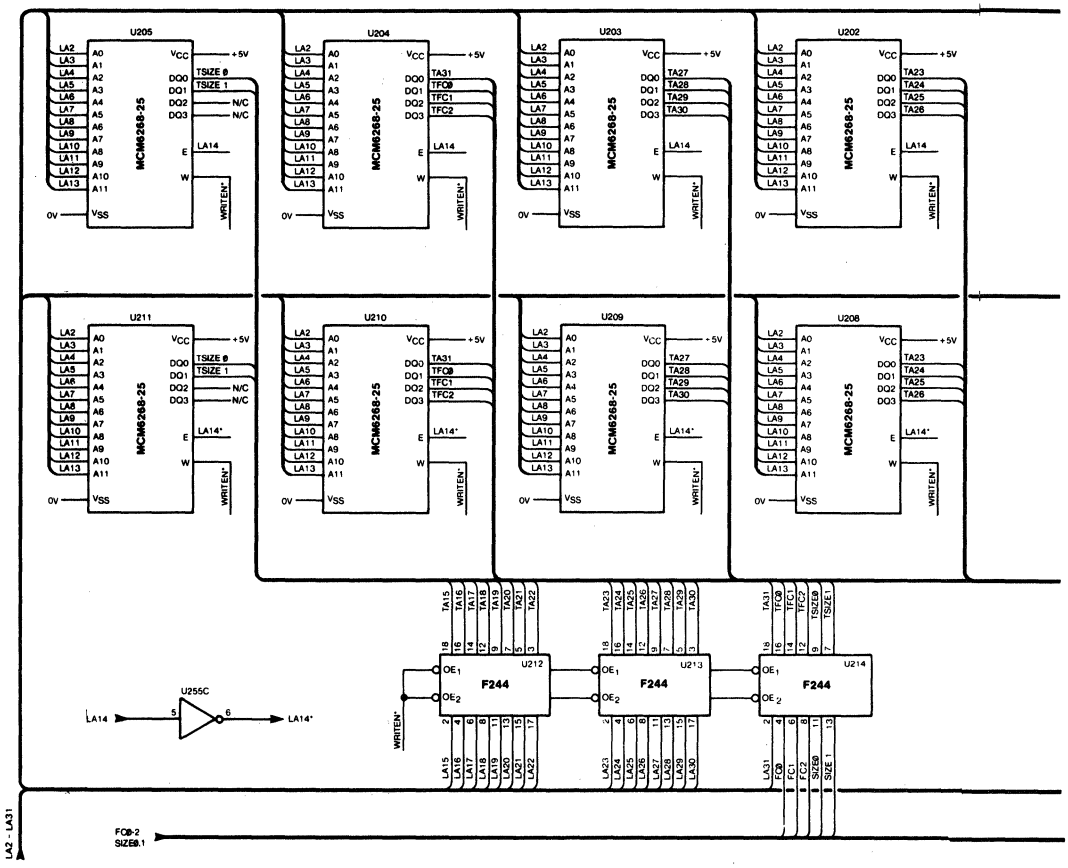
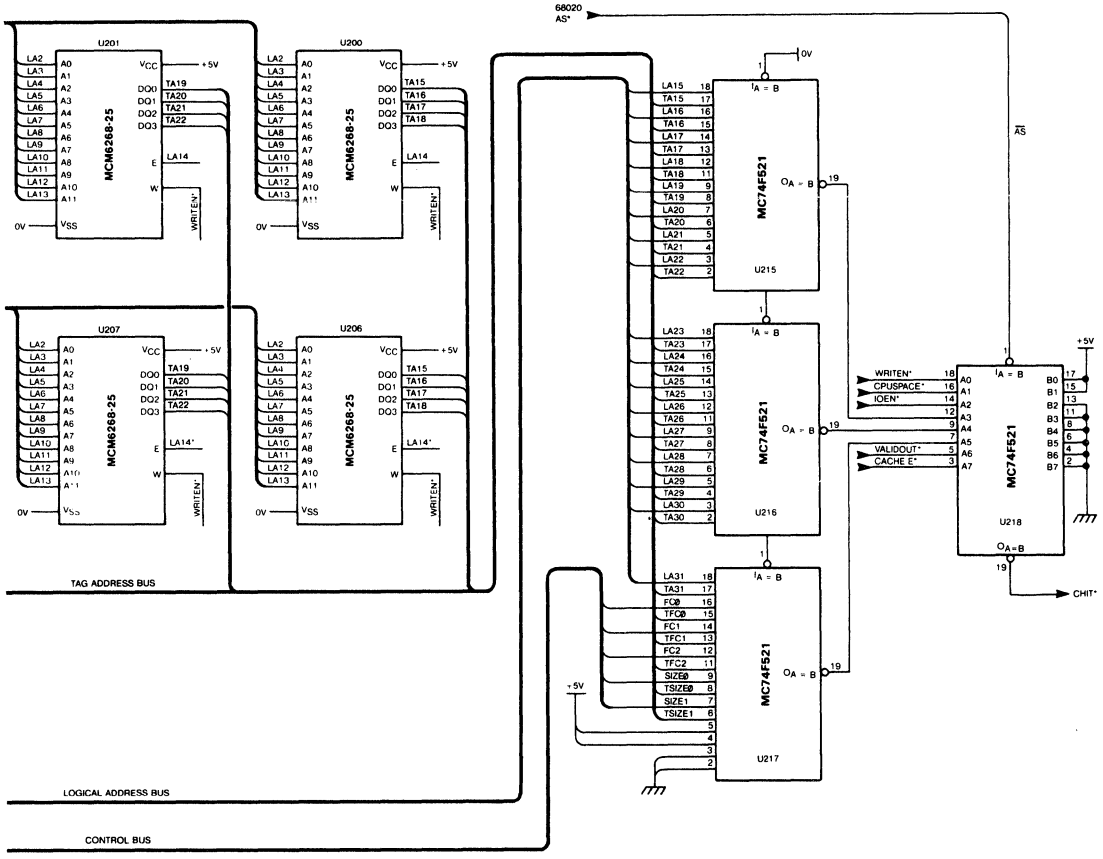


Figure 4: TAG Address RAMs


68020
AS*
U201
U200
U207
U206
MCM6268-25
+5V
0V
TA19
TA20
TA21
TA22
TA15
TA16
TA17
TA18
LA14
LA14*
WRITEN*
TAG ADDRESS BUS
MC74F521
U215
U216
U217
U218
LOGICAL ADDRESS BUS
CONTROL BUS
WRITEN*
CPUSPACE*
IOEN*
VALIDOUT*
CACHE E*
CHIT*

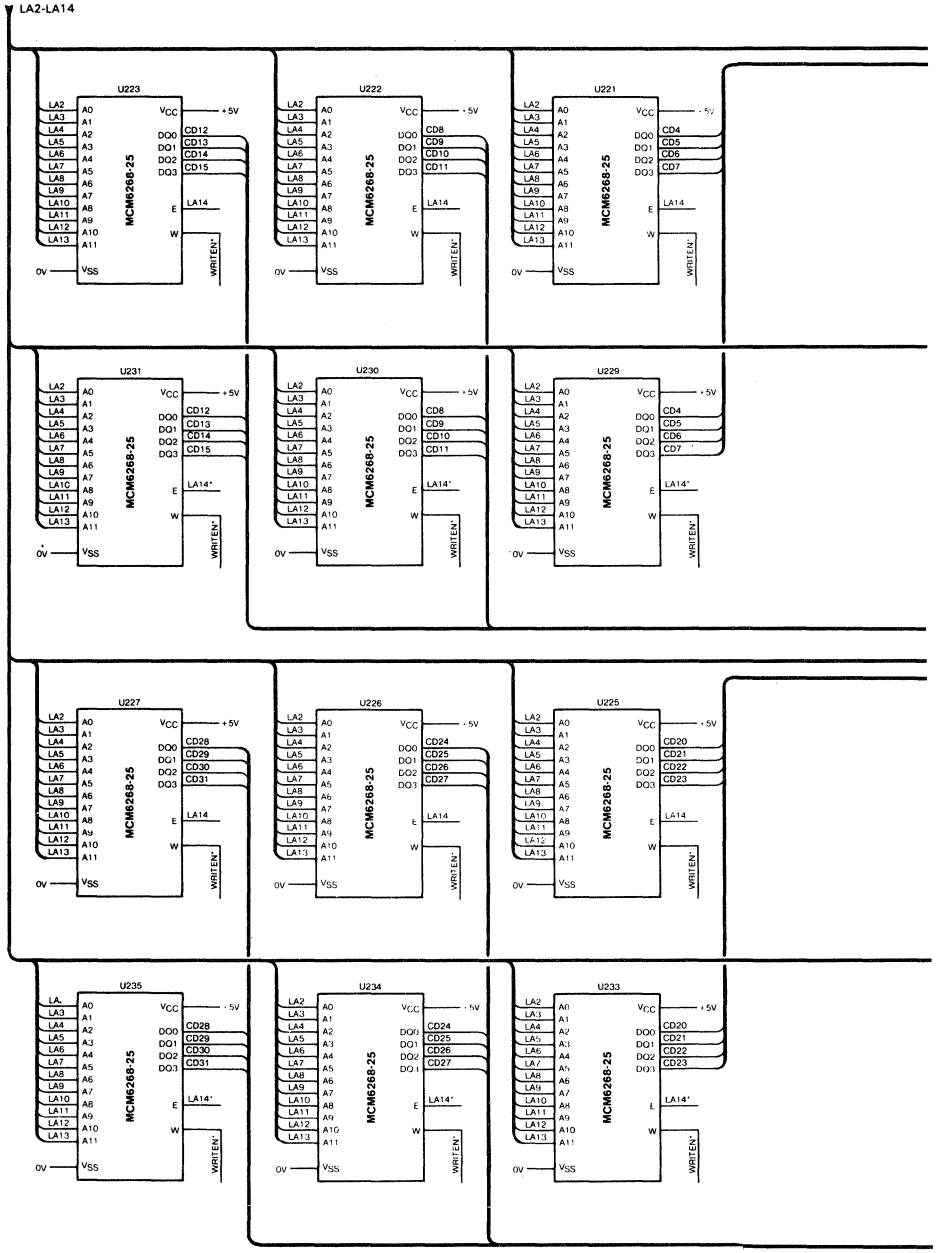
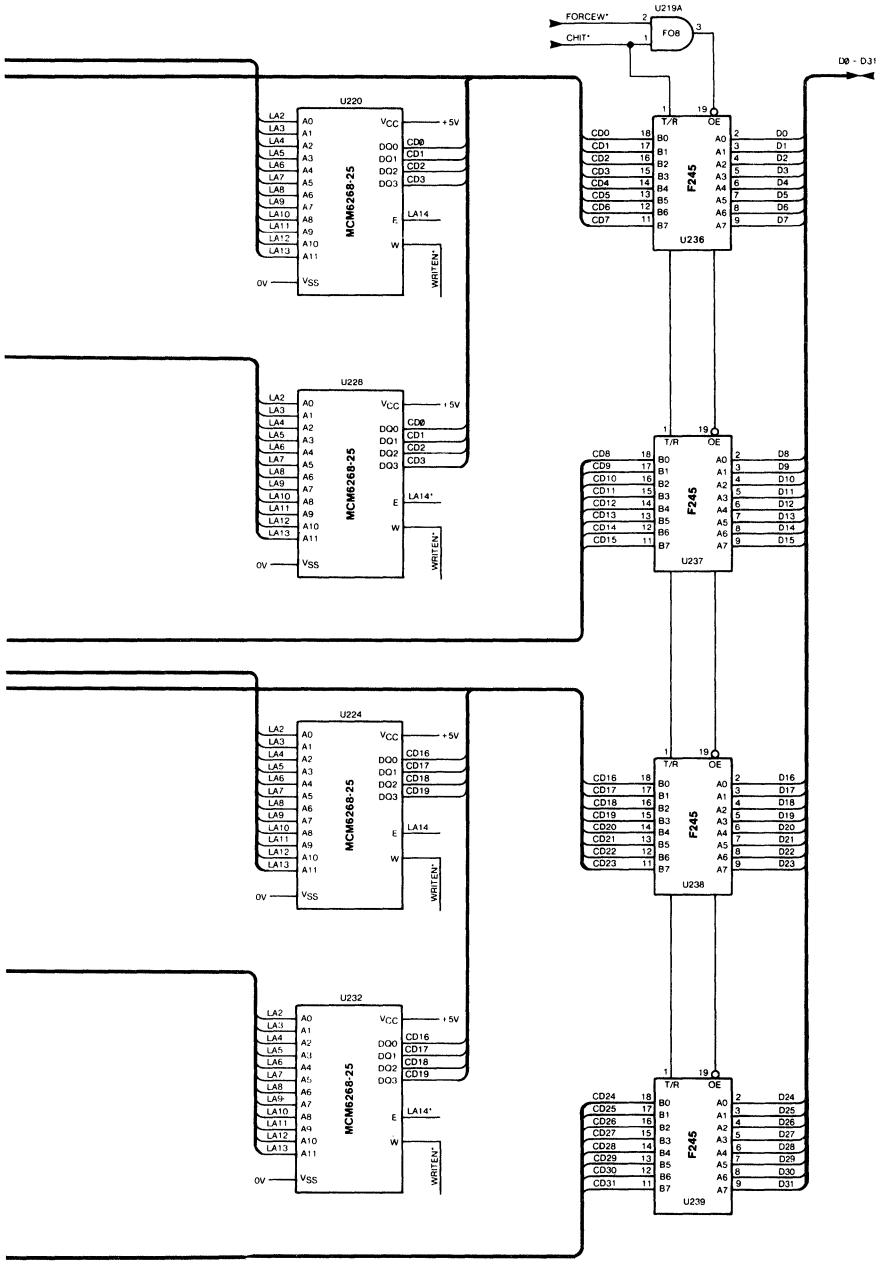
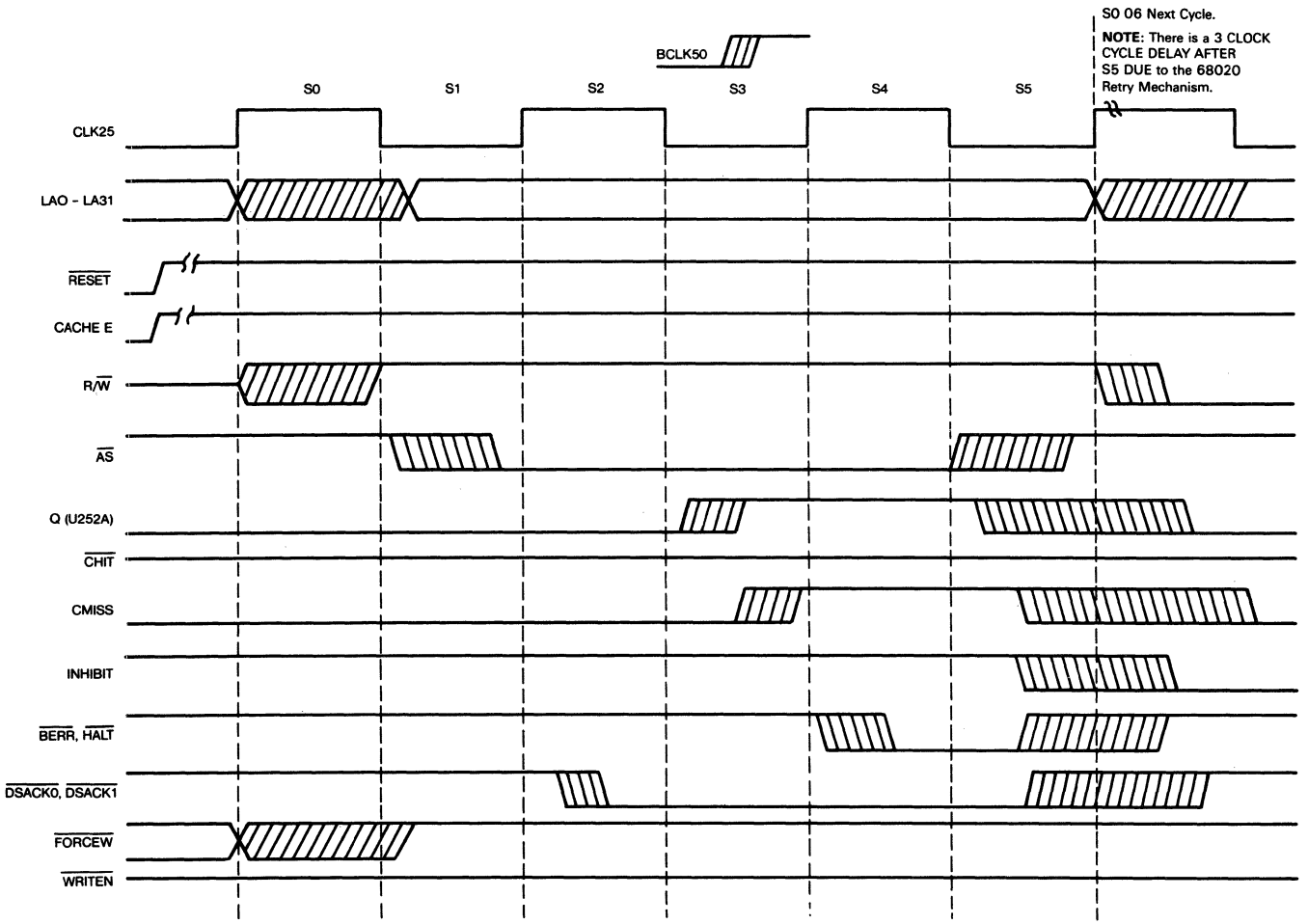
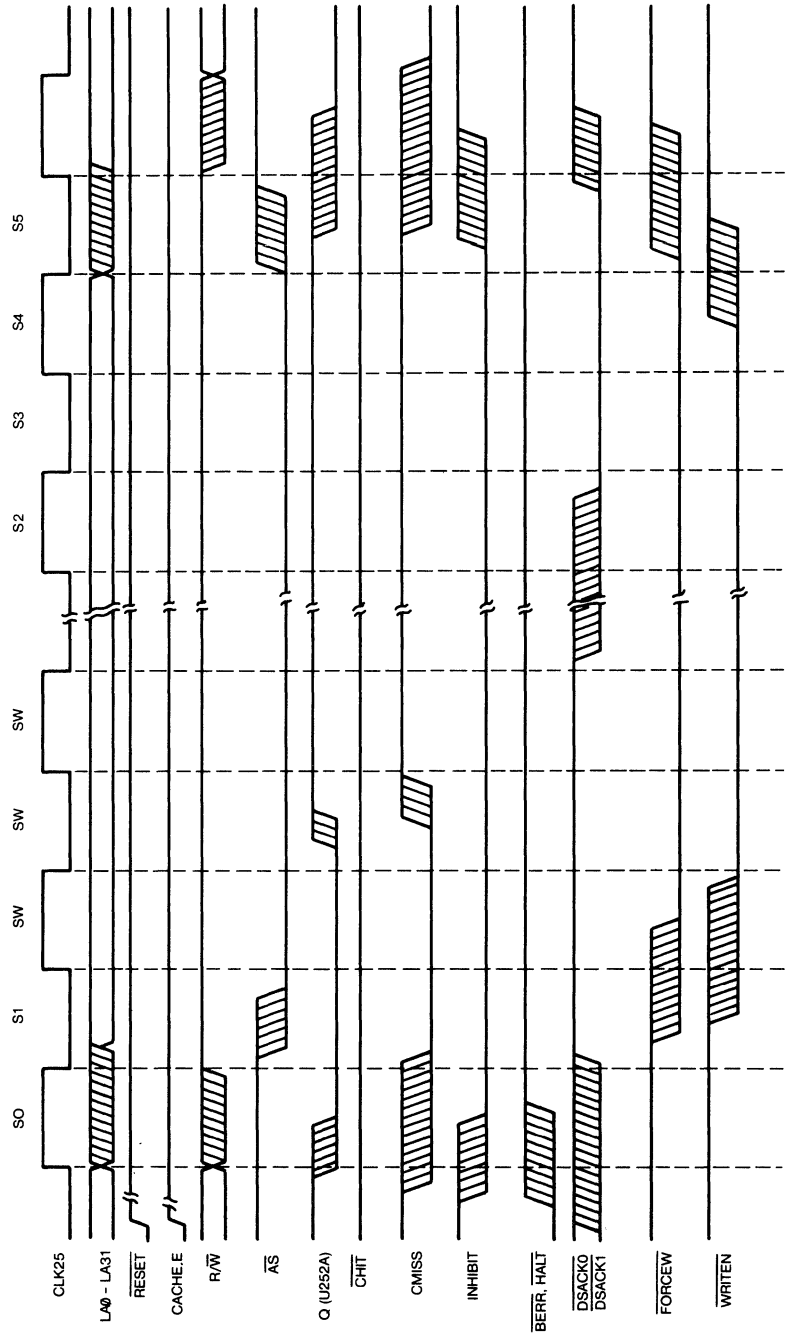


Figure 5: Cache Data RAMS


U219A
FORCEW*
CHIT*
FO8
D0 - D31
U220
U228
U224
U232
MCM6268-25
F245
U236
U237
U238
U239
WRITEN*
+5V
0V



Timing Diagram 1 - Cache Miss



Timing Diagram 2 - Retry of the Cache Miss Cycle

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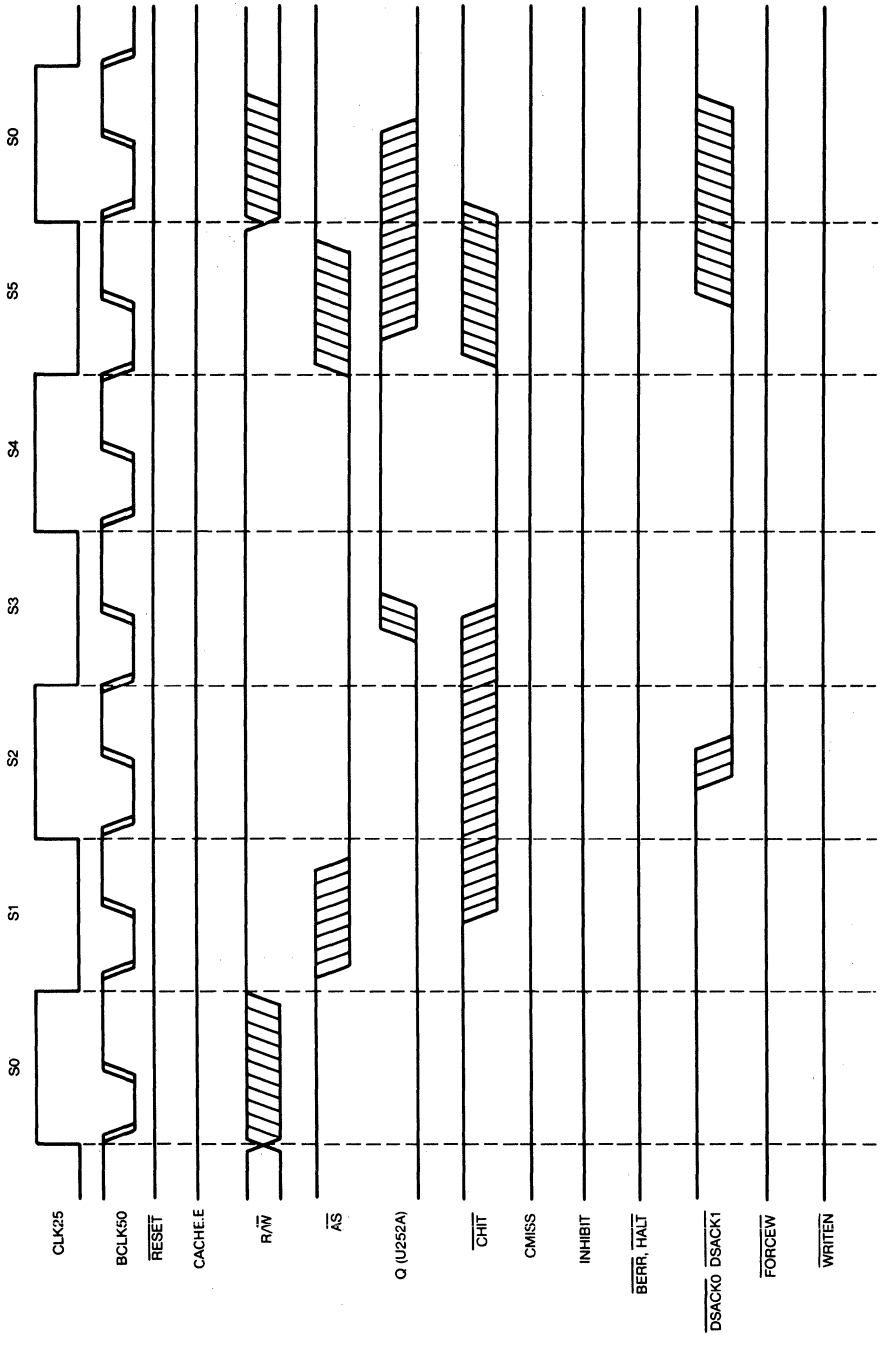

Timing Diagram 3 - Cache Hit

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DESIGN APPLICATIONS

DESIGNING A CACHE FOR A FAST PROCESSOR

COMPARATOR CHIPS HELP CREATE A HIGH-SPEED CACHE FOR THE MC68030

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Austin, TX 78762; (512) 928-6141.

To wring the best performance from the new breed of superfast microprocessors, system designers frequently turn to external caches. Direct mapped and set-associative caches offer advantages, compared with fully associative caches. In designing an address-tag-and-comparator system for a direct-mapped or set-associative cache, engineers must consider issues such as the speed of the hit, the address-bus loading, and the data-block size *(see "What's the Cache?")*.

Issues relating to the specific high-speed microprocessor also crop up. For instance, a system built around the MC68030 microprocessor must support two-cycle reads and writes related to the address-tag-comparator timing. Designers must also resolve questions of whether or not and how to support a burst mode. To support this mode, they must decide on address-tag and cache-data-RAM requirements unique to the mode, such as automatically incrementing addresses for the address tags and the cache-data RAM. They must also consider the data setup and hold timing requirements at the processor.

CACHE TAG RAMS

Matching the speed of the MC68030 microprocessor, the cache-tag comparators in the MCM4180, MCM62350, and MCM62351, organized to handle 4 kwords by 4 bits, compare data in the cache RAM with an external 4-bit-wide data field. The comparison results appear on the devices' Match pins. Each of the cache-tag devices is bulk clearable and has read and write functions. Of all the cache-system configurations possible with this MCM family of RAMS, for a 32-bit-by-16-kword system, a block of four MCM4180s as tag valid-bits comparators and four MCM62350s provide the fastest hardware arrangement, least bus loading, and lowest cost *(Fig. 1)*.

The MCM4180 includes an Exclusive-Nor (XNOR) comparator, which matches each bit position with the stored data for a true result. This type of comparator requires that every bit position match the stored data for the result to be true.

The MCM62350 and MCM62351 supply a user-configurable comparator offering the conventional XNOR mode and an And-Or-Invert (AOI) mode. Unlike the XNOR mode, the AOI comparator treats zeros in any bit position as don't-care bits during the compare operation. The AOI option is extremely useful for comparing status bits often stored with each address tag. The status bits can represent validating entry bits, which allow storing multiple data entries with each address-tag entry (block size = n), as well as individual so-called dirty bits needed for copy-back caching schemes.

The MCM62350 and MCM62351 RAMs also feature bit-set and bit-clear write cycles, which allow individual bits to be unconditionally set or cleared through a mask. Thus, any combination of the four bits in any particular location can be set or cleared without having to read the RAM, modify the data, and write it back as in a conventional SRAM. This feature is useful with the AOI com-

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parator for storing status bits. Also, both the MCM62350 and the MCM62351 have ground pins positioned to achieve minimum self-inductance in both DIP and small-outline J-type packages.

The MCM62350 differs from the MCM62351 in that it offers a user-configurable Match-output active level. The MCM62351 has an active high open-drain Match output. Wire-ORed connections of separate Match pins allow the comparison width to expand efficiently.

The design of external caches for the MC68030 involves two major timing problem areas—in the address-tag-comparator and in the data cache. Since the synchronous bus protocol makes it possible to use short bus cycles and supports burst-mode accessing, the prudent designer will also choose to use it for external cache interfacing to the MC68030 *(see "A Synchronous Bus Protocol").*

The primary challenge with timing the address-tag comparator is to avoid wait states when the processor runs at a high frequency. Generally, only a hit in any given bus cycle should assert the Synchronous Termination Handshake (/STERM) signal. The first order of business, then, is how to generate /STERM.

To avoid a wait state, the MC68030 asserts the worst-case Address Strobe (/AS) signal at the same time that the /STERM signal is activated. As a result, cache designs for this processor cannot generally use the /AS to signal the cache that a bus cycle is starting.

Nevertheless, the address-tag comparison must be qualified based on valid addresses that /AS announces. Fortunately, a signal called External Cycle Start (/ECS) is valid slightly earlier than the addresses. Whenever the processor needs an instruction or data, it therefore asserts

WHAT'S THE CACHE?

With a cache, when a processor executes a new task, it fetches from the system's main dynamic memory the first instruction and corresponding data, plus the instructions and data for several subsequent operations at adjacent memory addresses.

The cache's SRAM memory fetches the instructions and data from the adjacent main-memory addresses because they have a high probability of being used in the operations that follow. Most programs contain loops, and if the cache is large enough, the needed information will be present in the fast cache, shortening the average memory-access time.

That's a cache hit. If the cache doesn't contain the information, a miss occurs. In this case, the main memory again responds, and the cache receives updated instructions and data.

A cache controller circuit sequences the necessary functional steps. For normal program operation, the system doesn't directly address the cache. The cache subsystem stores both the information and its corresponding main-memory address. The controller compares the stored address in the cache, called the address tag, with the address the processor provides to determine whether the cache contains the requested data.

Cache types are usually delineated by their placement policy, or mapping algorithm, which determines where new information is stored in the cache. Most caches are either associatively content addressable or directly mapped, random-accessible types.

Whereas in a straight RAM, the processor directly accesses the information, in a content-addressable memory a match with a stored address of the information's original main-memory location causes the contents-addressable portion of the cache to respond with a pointer *(see the figure, opposite, left).* The pointer, or address, then specifies the data's location in a random-access-memory portion of the cache system. This fully associative memory cache copies the information in any main-memory location into any location in the cache.

A directly mapped cache, on the other hand, uses random-access memories to store both an address tag and the information's image *(see the figure, opposite, right).* The low-order bits of the address from the processor provide an index into the address-tag-store portion of the cache system, which stores the high-order address bits. To determine whether the requested information resides in the cache, the system compares the high-order address bits from the processor's bus with the contents of the address-tag-store RAM. If they're the same, the cache contains the requested information. Unlike in a fully associative cache, in a directly mapped cache, a memory-address location has its information copied into only one unique location.

The fully associative content-addressable memory cache can have a higher hit rate than any other cache type of the same size m. But it's very expensive, compared with a directly mapped random-access cache memory of comparable size.

When n directly mapped caches operate in parallel, the cache is designated as an n-way set-associative type. Nevertheless, system designers may consider both directly mapped and fully associative types as set-associative caches. A directly mapped cache is simply a one-way set-associative type, and a fully associative one is an m-way set-associative type.

A four-way set-associative cache yields about the same hit

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/ECS during the clock's high phase when the new addresses appear. Should the processor find what it needs in its internal caches, it would not assert /AS and an external bus cycle would not run. If /STERM activates when no bus cycle runs, the processor ignores it.

The timing diagram of the synchronous bus shows that after addresses are valid, /STERM must be activated within just a half clock period minus the clock-rise time to avoid wait states. Operating at 25 MHz, that leaves only 15 ns to check for a cache hit and assert /STERM if wait states are to be avoided.

The circuit must furnish an extra gate for the results of the tag comparator to be ANDed with a qualifier—a latched /ECS signal. A 74F64 AOI gate can AND the Match signals from the tag comparators to this qualifier. Unfortunately, this gate adds a 5.5-ns delay to the circuit. Consequently, the tag comparators must perform their comparison in 9.5 ns.

Since TTL-compatible tag comparators aren't that fast, this technique isn't feasible. Two options remain: Always assert /STERM after /ECS, and if the cache misses assert /BERR and /HALT retry, or insert a wait state. With retries, at 25 MHz, the tag comparator has 35 ns to perform its function and generate /STERM. At 33 MHz, it has just 28 ns. For the wait-state option, 34.5 ns is available to generate /STERM after the addresses are valid.

Retries, however, can run into trouble. After requesting a retry, the processor must disable the cache to prevent a system deadlock condition when the bus cycle reruns. Also, before the bus cycle can rerun, a two-clock-cycle delay occurs. As a result, the penalty incurred when the external cache misses might be greater than it would be if the processor asserted /STERM only on a cache hit.

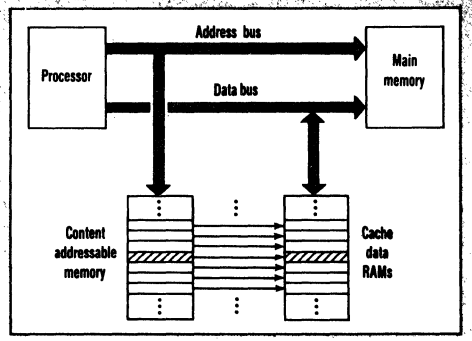
rate as a fully associative one-way cache of the same size. In an *n*-way set-associative cache, any particular address location maps data in *n* locations in the cache.

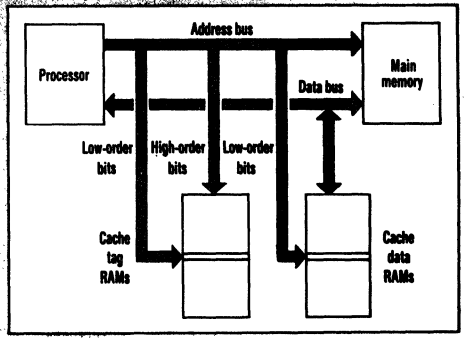
Consider the issues involved in designing the address-tag store and comparator of a directly mapped cache. For maximum performance, the time taken to bus load the addresses should be minimum. Thus, one component should both store and compare the address tags to minimize delays resulting from off-chip signal propagation. For a 16-kword by 32-bit cache operating on a 32-bit address bus, the part must store a 16-bit-wide address-tag field, plus a 17th bit to indicate that the address tag is a valid entry. Consequently, the storage of only one cache data item for each address-tag entry—a block size equal to one—requires an address-tag storage capability of 16 kwords by 17 bits.

When storing *n* data items with each address tag entry, the block size equals *n*. Keeping the cache size constant reduces the depth of the address-tag store by a factor of *n*.

Having only one validating bit for each address tag, however, requires either an *n*-by-32-bit main-memory data-bus width or running *n* 32-bit bus cycles to fill the cache line in the event of a miss. Another event could also transfer the *n* by 32 bits. A less restrictive way to support *n* entries per address tag is to have *n* validating bits stored along with the address tag. Then when the system records a miss, the controller updates the address tag and sends only the validating bit corresponding to the transferred data item. This procedure requires only a 32-bit data bus and one main-memory cycle to allocate a new cache line.

An increased block size would mean that designers need fewer memory components to build the address-tag store and comparator. A large block size with fewer components not only saves board space and shrinks cost, but also reduces address-bus loading, which then, of course, will result in faster performance.





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Therefore a no-wait-state cache with a low hit rate can perform worse than a cache with a wait state.

A secondary difficulty with tag comparators in MC68030 cache designs is supporting burst-mode accesses. The address-tag-comparator timing is clearly a limiting factor in the design of external caches for the MC68030. Because the burst-mode cycles furnish only a first address for the four desired long words, the circuit must provide autoincrementing addressing to the address-tag comparator and the cache-data RAMs. This requirement, coupled with the fact that burst transfers can occur in single clock cycles, implies that incrementing the addresses into the address-tag comparator will not be fast enough to support one-cycle bursting.

Organizing the cache with a block size of four is a viable one-cycle bursting solution. Storing a valid bit for each long word per tag, then, requires only checking the valid bit on the fly during the bursting portion of the burst-mode transfer.

This approach can exploit the fast timing of the compare port in an MCM62350 or MCM62351 to store the valid bits. It also allows the AOI comparator option for the valid-bit comparisons to operate effectively *(Fig. 2)*.

A PAL POINTER

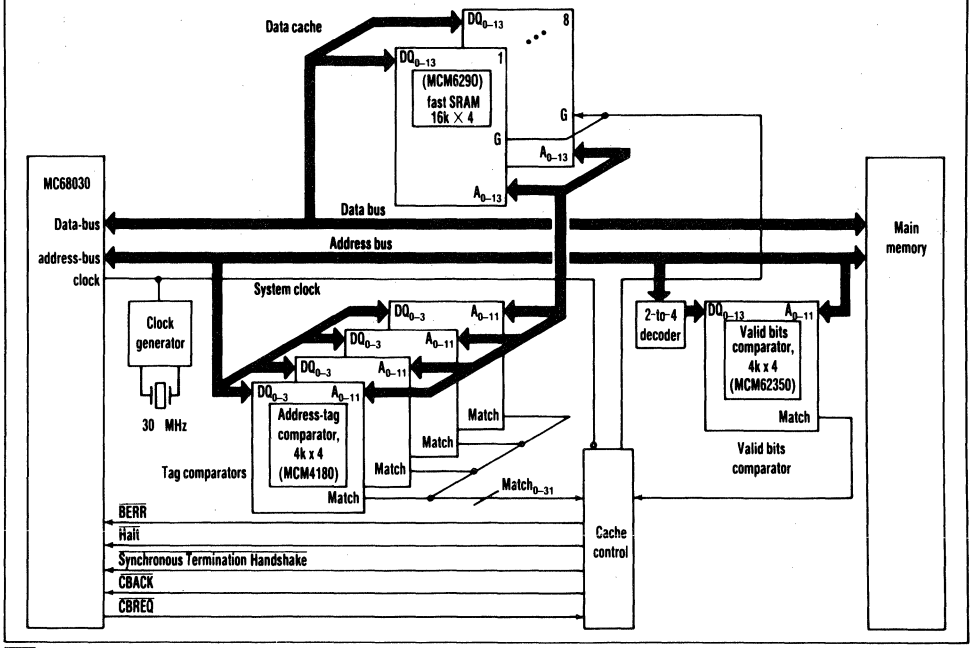
The open-drain Match pins of the MCM62351s permit wire-ORing of the four address-tag outputs to the matching circuit and thereby the elimination of a fan-in gate. A PAL device makes possible a simple, fast input to this circuit by providing a pointer for checking only the relevant long word while bursting. The address tag still needs comparison, but only on the initial access.

The PAL should contain a decoder to decode addresses A2 and A3 from the processor. The resulting one-of-four outputs then enter a shift register, also built into the PAL. In this way, the four outputs from the PAL provide the compare port of the status-bit comparator with a rotating pointer. In the AOI comparator, a single valid bit compares when only one of the four compare inputs is at a logic-one level. The other three valid bits become don't cares.

A block size of four not only allows single-cycle bursting to work, but it also saves components. Furthermore, because address-line loading is reduced, the processor can drive its address bus more quickly. The result is fast hardware.

The main data-RAM issues relate to burst mode. They include address autoincrementing and data setup

NO WAIT-STATE CACHE FOR FAST RAMS



1. A CACHE SYSTEM with four XNOR-configured comparators and one AOI configured comparator—each with a depth of 4-kword entries, a 16-kword-by-32-bit cache, and a block size of four—has the lowest cost, reduced bus loading, and fast hardware.

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A SYNCHRONOUS BUS PROTOCOL

The MC68030 adds a new bus protocol—the synchronous bus cycle—to the MC68XXX family of processors. Like its predecessors, the MC68030 supports the standard asynchronous bus protocol. Unlike the asynchronous bus on the MC68020, the 60830's synchronous bus doesn't support dynamic bus sizing. As a result, all synchronous bus cycles issue from a 32-bit port.

The minimum length of the MC68030's synchronous bus cycle is two clock periods, whereas the MC68020 has a minimum bus cycle of three clock periods. Also, the MC68030 has on-chip memory-management functions; the MC68020 does not. Since an MC68851 memory-management unit requires a clock cycle to translate logical addresses to physical addresses, the minimum physical bus-cycle length of an MC68020-MC68851 combination requires four clock periods. The MC68030 bus can therefore operate twice as fast as an equivalent MC68020-MC68851 system at any given clock frequency.

Another feature added to the MC68030 bus, the burst-mode protocol runs only in synchronous mode. The MC68030 has two internal caches—an instruction cache and a data cache. Both have 16 lines with a block size of four (four 32-bit words per address tag). When either internal cache of the MC68030 records a line miss from a cachable area of main memory, the system attempts to burst four long 32-bit words to fill the new line.

The processor places the address of the first long word on the bus and expects the return of the corresponding data, plus three additional long words, in as little as three clock cycles. The processor doesn't change the address on the bus during these subsequent transfers. Rather, it assumes that the external memory increments address lines A2 and A3 in a modulo-four fashion, as if the the bus were operating in nibble mode. Thus, with no wait states, the MC68030 receives as many as four long words in just five clock cycles by using the burst-mode protocol. Because the application's characteristics affect the type of code the system runs, the decision of whether or not to use the burst mode is very important. System designers would do well to study the matter in depth.

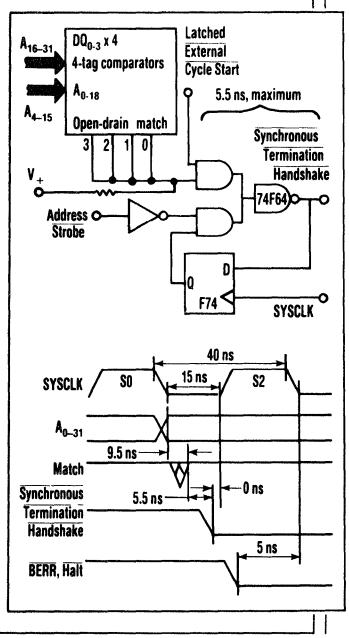
A knowledge of the timing requirements of no-wait-state operation is crucial to understanding how the MC68030's synchronous bus operates *(see the figure)*. When a new bus cycle starts, the processor delivers memory addresses during a system-clock high time, but the addresses are guaranteed valid only at the end of the clock high time.

To avoid wait states, the Synchronous Termination Handshake signal, /STERM, must assert 0 ns before the rising edge of the next system-clock pulse. If this condition is met, the processor latches the data on the next falling edge of the clock. The processor needs a 5-ns setup time for the data with respect to the falling edge of the clock.

If the processor requires wait states, /STERM can be delayed relative to the clock rising edge to allow the use of slow memories in the synchronous mode. This feature applies also to burst-mode cycles. But when the processor recognizes /STERM on a clock rising edge, data latches on the next falling edge, subject, of course, to adequate setup and hold times.

When the processor runs a burst cycle, it can accept new data with the same setup time to the clock on the clock's next three falling edges. The processor also needs an 8-ns data hold time after the clock falls when operating at 25 MHz. Accordingly, if the processor runs burst cycles at 25 MHz, the data must be valid during the bursting portion of the cycle for 13 ns of the 40-ns clock period to meet the processor's setup and hold time requirements.

Like its predecessors, the MC68030 microprocessor supports bus retries and reruns. If the bus-termination handshake STERM/, or DSACKx/, is asserted with proper setup time relative to a rising clock edge, activating BERR/ and HALT/ with a 5-ns setup relative to the next falling edge of the clock aborts and reruns the current bus cycle. But this action results in two dead clocks on the bus before the bus cycle restarts. Nevertheless, no wait-state caches designed for the MC68030 use this technique to prevent the processor from latching bad data when an external cache records a miss.



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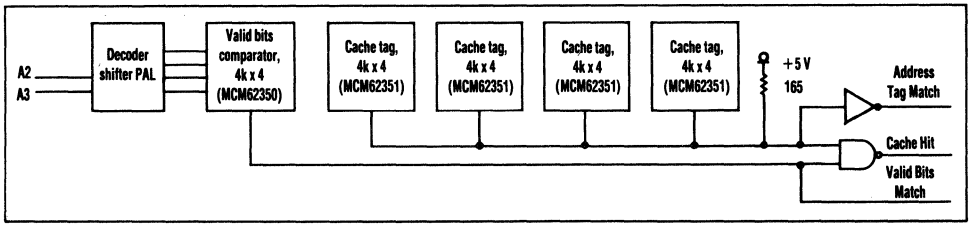


2. ORGANIZING THE CACHE with a block size of four is a viable single-cycle burst-mode solution. This approach can exploit the fast timing of the compare port in an MCM62350 or MCM62351 to store the valid bits and make it possible to effectively apply the AOI comparator option for the valid-bit comparisons. The open-drain Match pins of the MCM62351 permit the wire-ORing of the four address-tag outputs to the matching circuit, thereby eliminating a fan-in gate.

and hold timing to the processor. At issue is whether burst mode supports two-cycle write timing.

If a synchronous bus cycle is run, the data must set up at the processor without delay (in 5 ns), before the first falling edge of the clock after the processor recognizes the STERM signal. If the cycle is two clock periods, then the time available to access the cache-data RAM equals a clock period. For a 25-MHz clock, the time available would be 35-ns. A 33-MHz clock would yield a 25-ns interval.

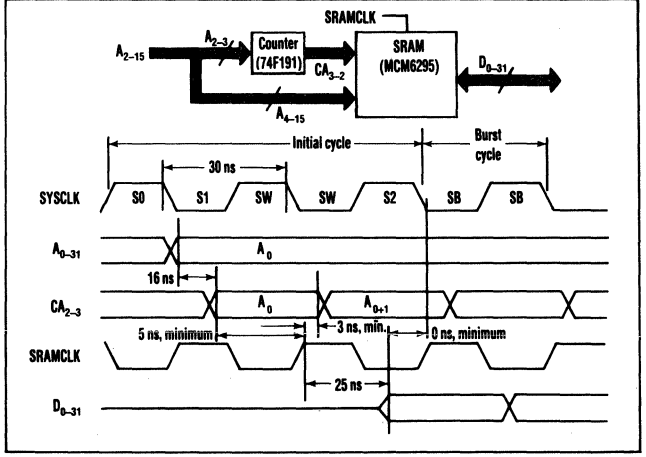
For single-clock burst cycles, also, 35 ns is available for RAM accesses at 25 MHz. But the data hold time after a clock low at 25 MHz is merely 15 ns. That short time interval calls for very fast output-enable SRAMs, such as the MCM6290.

To support the burst mode, a 74F191 counter, inserted in series with A2 and A3 address pins, gives two incremental addresses to the cache-data run for autoincrement addressing. Unfortunately, the processor's data-hold-time requirements prevent this scheme from working. Besides, the counter's latency in a parallel-load mode requires a RAM faster than 35 ns.

A MCM6295 synchronous SRAM as the cache-data RAM, with one 74F191 counter, readily supports single-cycle bursting *(Fig. 3)*. Latching the data outputs when the synchronous SRAM clock is low resolves the issue of data-hold time. Furthermore, once the synchronous SRAM clock drives high, the addresses into the device are registered and can be changed for the next access in the burst sequence.

When the MC68030 performs a two-clock write cycle, the data and address sent to the RAMs are simultaneously valid for only a half clock period. For clock frequencies over 25 MHz, this time isn't adequate to complete a write cycle in typical fast static RAMs. In that case, it's necessary to insert a wait state.□

A THREE-CYCLE BURST READ



3. AN MCM6295 SYNCHRONOUS SRAM, a cache-data RAM with one 74F191 counter, readily supports single-cycle bursts.

Richard Crisp led the design team for the Motorola cache-tag comparators. He has helped design several microprocessors, including the MC69000, MC658020, and the Intel P7CP. Crisp, who holds a BS from Texas A&M University, has four U.S. patents.

Brian Branson received a BS from Colorado State University. At Motorola, he designs application-specific static and dynamic RAMs. He has one patent pending.

Ron Hanson holds a BS from Rose-Hulman Institute of Technology and an MBA from Indiana University, in Bloomington. Hanson is a product marketing engineer for fast static RAMs at Motorola.

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AR260/D

ENHANCING SYSTEM PERFORMANCE USING SYNCHRONOUS SRAMs

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INTRODUCTION TO SYNCHRONOUS SRAM ARCHITECTURE

Fast static RAMs (FSRAMs) are commanding a lot of attention from today's high performance system designers who frequently find that the speed of their system is limited by the performance of FSRAMs on the market. As 32-bit microprocessor-based systems become faster and more prevalent, the demand for sub 25 ns FSRAMs will grow even more.

FSRAMs are the driving force behind semiconductor technology today: they have the smallest circuit features—as low as 0.8 micron from some manufacturers—and use special processes like double-level metal and BIMOS. The Fast SRAM has come a long way from its slower ancestors like the 1K × 4 Model 2114. The ease of use and dependable performance that resulted from the asynchronous performance of SRAMs have been replaced by the raw speed which is pacing today's demand; however, FSRAMs are still expected to meet the basic SRAM specifications for pure asynchronous performance. This dichotomy has caused problems as chip designers come up with more innovative ways to speed up their circuits. Address transition-detection circuitry, for example, caused a number of problems when first introduced in 2K × 8 FSRAMs under certain system conditions. With such advanced technology being used and the cost of manufacturing these chips so high, Motorola has developed an alternative to a high-tech 15 ns access SRAM that uses conventional technology.

Motorola's newest SRAMs are the first to fully embrace the primary purpose of Fast SRAMs. They totally abandon the previous definition of asynchronous SRAMs. They have the requirement of a clock signal, and are, therefore, Synchronous SRAMs. They have separate pins for input and output data, and do not specify standby power.

Motorola offers four different 65,536-bit Synchronous SRAM family members organized as 16K × 4: Models MCM6292, MCM6293, MCM6294, and MCM6295. The technology used for their implementation is the fast, low power-consuming, and noise-immune HCMOS III, which uses a silicon gate for its fabrication. One of the main advantages to using these devices is that they can be designed into system cache-memory or writeable control-store applications with fewer interfacing glue-type parts than the standard SRAM memory. Among the reasons for this are the integrated input and output latches that are capable of driving loads up to 130 pF. Due to the increased operating speed of the device and the additional output-buffer loads, an extra ground pin has been placed on the chip.

Four different devices have been specified so that all combinations of the output-latching and output-enable features are in the offering. The MCM6292 comes equipped with latches that are edge triggered on the inputs but transparent on the outputs. To support systems with pipelined data, the MCM6293 is offered with edge-triggered latches on both the inputs and outputs. The MCM6295 and MCM6294 are output-enable versions of the two basic parts. All of the Synchronous SRAMs come with separate data-in and data-out pins; however, some systems specify a more conventional common I/O mode, and the asynchronous output-enable control ($\overline{G}$) which replaced the $\overline{S}$ signal on these parts can be helpful in such a case.

In many designs using SRAMs, there is actually extra time during the cycle that is being wasted. In more critical applications, the Synchronous SRAM offers an alternative to the conventional SRAM. An external clock input (K) can be used to precisely control the cycle by directing the operation of the on-chip latches.

The designer of small personal computer systems can use the Synchronous SRAM in a number of storage areas. One of the primary applications, cache memory, is high-speed memory that resides between the central processing unit (CPU) and the main memory of the system. Accesses to this fast cache typically require 60 ns versus the 200 ns needed to perform an access to main memory. One way the cache is used is to store data or instructions from main memory that are frequently called for by an application. As an example of this, higher-level languages often use repetitive loops: by storing the data necessary for these repeated operations and instructions in the cache, accesses to the main memory can be avoided.

A typical system is illustrated in Figure 1. It is configured as a cache memory residing between the CPU and the system bus. The system bus links the main memory and I/O devices to the CPU by way of the cache.

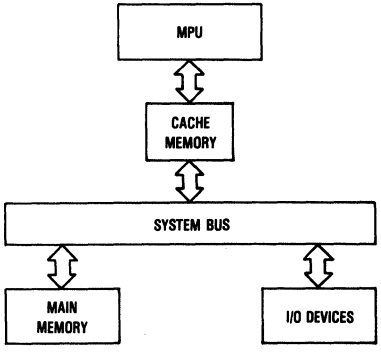

Figure 1. A primary synchronous SRAM application is high-speed cache memory residing between the CPU and the main memory of a personal computer system. Accesses to the cache typically require 50 ns, whereas main memory takes 200 ns.

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In operation, there is one set of locations in which data is stored and another set of locations containing a cache tag for each word in the cache. The cache tag identifies the main memory location with which the data is associated. A comparison is made between the cache tags, which are located in the cache memory, and the address, which is generated by the microprocessor at the beginning of a cycle. If a cache tag and the address match, there is no access made to main memory, but instead the read or write cycle is executed on the corresponding byte of data stored in the cache. When the address does not find a match, a miss occurs, and new locations must be read into the cache from main memory.

A cache miss is the result of a mismatch between the cache tag and the desired address to be accessed by the CPU. When this occurs, the system logic is allowed to perform a retry of the previous access. The appropriate address is accessed from main memory. Following an update of the cache, the data is then available for processing.

The cache hit rate is the actual percentage of accesses made to the cache in which the requested address is resident. In order to keep the hit rate as high as possible, a variety of software routines are used. The function of these routines is to keep the cache as full as possible with the most frequently used data. In so doing, the cache hit rate for both the data and instruction caches will be maximized, increasing overall information throughput.

The Harvard architecture, an efficient method used in many current day applications, is characteristic of a configuration which supports parallelism throughout a system. Synchronous SRAMs can be organized as relatively small external caches connected to the data buses and instruction paths located between the CPU and main memory. This will allow simultaneous instruction execution and data prefetches. The external cache demonstrates another system speed enhancement capability of these devices.

ADDRESSING CONSIDERATIONS FOR READ/WRITE CYCLES

To better understand the Synchronous SRAM's addressing capabilities in regard to read and write cycles, refer to Figure 2. In this illustration, there are four MCM6292 synchronous SRAM devices configured to operate on a 16-bit data bus. Each memory has four data inputs and four data outputs to allow the transfer to data. The address bus consists of 14 address bits, A0-A13. These 14 bits are required to decode and access the 65,536 memory locations of each device. The memory matrix is configured as 128 rows by 512 columns. The system clock is connected to the (K) input of each memory and used to latch all inputs, outputs, write enable, and chip select.

In Figure 3, there are two different read-cycle timings being represented for the MCM6292 (transparent output latches). Both are examples of systems that use the rising edge of (K) to latch all inputs to the memory device. The states of the outputs are then held until the clock makes its transition to the low state. With this Synchronous SRAM, however, it is possible to have different memory access times, depending upon the condition of the clock (K). If the clock pulse is high for less than the 25 ns access time of the memory device, the total access time is rated at t_{KHQV} or 25 ns (Read Cycle 1). On the other hand, if the high portion of the clock cycle lasts longer than 25 ns, the total access time becomes t_{KLQV} (10 ns maximum) plus the length of the clock high (Read Cycle 2).

Figure 4 has been included to show the timing of a write cycle. The timing of a write operation is similar to that of the previously discussed read cycle. One point to consider is that to generate a write pulse, there is no requirement for complex external interfacing chips. This is accomplished through the self-timing mechanism which samples both the write enable and input data when (K) rises. A high-impedance state is entered when the clock returns low.

MPU AND MEMORY SPEED CONSIDERATIONS AT A SYSTEM LEVEL

One consideration worth mentioning is that many memories are not able to keep up with very high-speed MPU control devices. This has been a problem with DRAM technology for a number of years. MPUs operating at clock speeds of over 20 MHz are common in both business and engineering systems

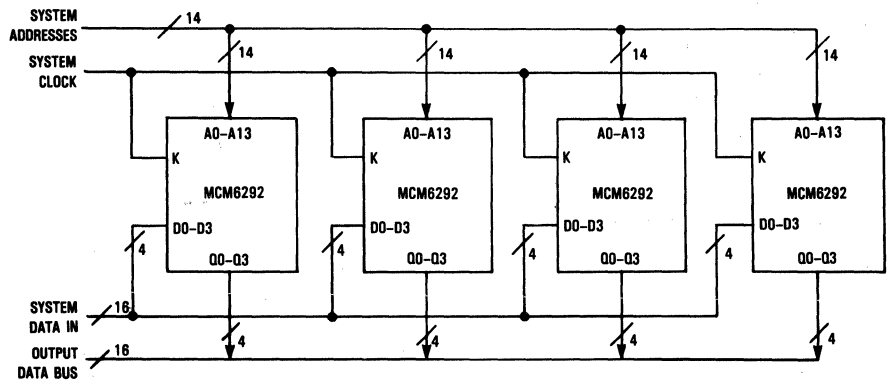
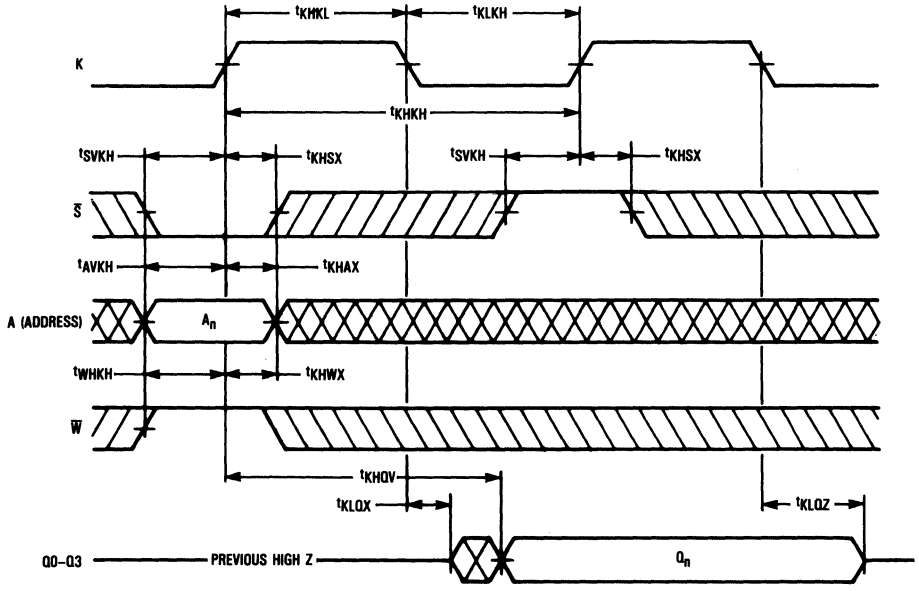
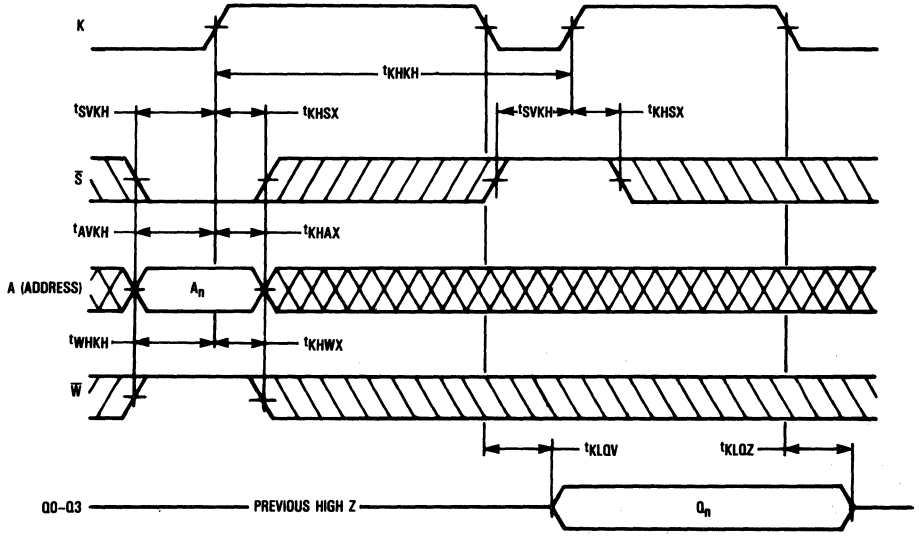


Figure 2. An array of synchronous SRAMs is configured for a 16-bit data bus. Each MCM6292 has four data inputs, four data outputs, and fourteen address lines.

READ CYCLE 1 (See Note 1)



READ CYCLE 2 (See Note 2)



NOTES:
1. For Read Cycle 1 timing, clock high pulse width $< (t_{KHQV} - t_{KLQV})$.
2. For Read Cycle 2 timing, clock high pulse width $\geq (t_{KHQV} - t_{KLQV})$.

Figure 3. If the system's clock high, t_{KHKL}, is shorter than the MCM6292's 25 ns access time, then the total access time will be 25 ns. However, if t_{KHKL} is longer than 25 ns, total access time is increased.

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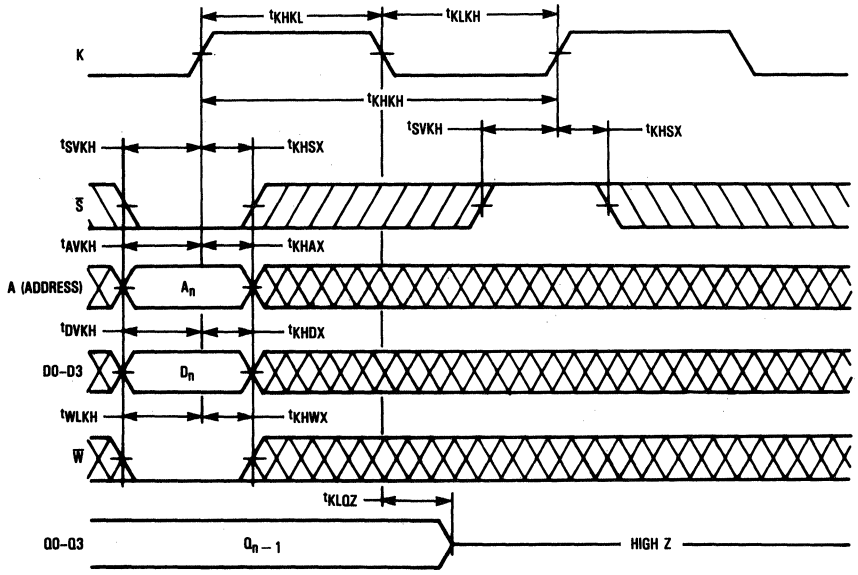

Figure 4. In a write cycle, the self-timing mechanism of the MCM6292 samples both the write enable and the input data when the clock signal, K, rises.

in use today; therefore, 25 ns Synchronous SRAMs are ideal to operate with zero wait states.

Wait states are implemented with slower SRAMs and most DRAMs to freeze the state of the microprocessor address and data bus for a clock cycle. As long as the signal controlling wait states is asserted, more wait-state periods will be generated. The microprocessor resumes operation when the wait-state signal is negated.

The alternative to implementing a wait state to halt the microprocessor for a slow memory device is to use the much faster Synchronous SRAM. Its timing parameters can be more exactly controlled, making the system operate more efficiently. Faster data throughput plus an improvement in overall system performance make the Synchronous SRAM cache a very cost-effective solution in a microprocessor-based system.

When performing read and write operations in a personal computer system, the timing relationship between a high-speed microprocessor's system clock and a typical Synchronous SRAM's cycle time constraints is very critical. These operations could be as simple as inputting console information for CRT display outputs or as complex as supporting multitasking environments or concurrent execution of operations.

High-performance microprocessor systems with operating frequencies of 20-25 MHz are a realistic timing example being offered today. For microprocessors capable of operating at these speeds, a 25 ns Synchronous SRAM is ideally suited. These devices not only provide precise clocked timing control, but also will support applications requiring system clocks running at over 30 MHz. This can be accomplished without incurring any degradation of the processor by inserting wait states.

WHAT'S TO COME FROM SYNCHRONOUS SRAMs

Very high cache hit rates can be attained from a relatively small cache store. The high-rate efficiency is primarily due to the fact that the cache is located external to the CPU rather than actually being an on-chip cache, as is the case with some high-performance microprocessors.

In addition to the popular high-speed cache-memory applications, Synchronous SRAMs are also ideal for writeable control store environments. Data can be downloaded into a Synchronous SRAM array, and the information can be accessed at very high speeds—much faster than from a DRAM array.

Memories are taking on new roles. Because of this, they are being used in a wide variety of application areas and operating to support functions previously not possible. Future Synchronous SRAM devices will be even more complex and some will very likely contain higher degrees of intelligence. Many will be designed with special system functions in mind. Higher-speed operation working from lower voltage sources is just one example. There will be enhancements allowing the designer more flexibility and enabling him to reach supercomputer performance.

Current-day static memories support numerous applications. The synchronous SRAMs discussed above will be offered in 300-mil, 28-lead CERDIP and 400-mil, 28-lead plastic SOJ packages. These configurations satisfy the requirements of most systems presently. As chip integration and sophistication continue to advance, the packaging technology will also need to advance to promote future innovations within the industry.

For more information on MCM6292-series synchronous SRAMs, contact Memory Marketing at Motorola, Inc., MOS Memory Products Div., P.O. Box 6000, Austin, TX 78762. (512) 928-6700.

AR258

HIGH FREQUENCY SYSTEM OPERATION USING SYNCHRONOUS SRAMs

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INTRODUCTION

The market for semiconductor memory products suitable for today's high speed cache applications is changing dramatically as the demand for higher performance super mini, ASIC, and microprocessor based computers rapidly increases. This development has put heavy pressure on MOS memory suppliers for faster and faster static RAMs to support shorter and shorter processor cycle times. To utilize their full system performance, fast SRAMs require precise system control, long address hold times, and have tight write pulse requirements. They provide short data valid time, cause common I/O data contention, and offer low drive capability. Todays high performance processors themselves have similar I/O requirements. Therefore system designers have many concerns when designing a fast memory subsystem. They must use additional logic (latches, drivers, pulse generators, etc.) to allow the memory subsystem to interact efficiently with the processor at the fastest system cycle times.

A solution to get the memory and the processor to work well together at fast cycle and access times lies not only in faster components, but in minimizing the need for external glue logic and its associated delays. The Synchronous Static RAM is defined as having on chip latches for all its inputs and outputs, added drive capability, and a self timed write cycle all under the control of the system clock. This eliminates the need for most external logic chips and allows the memory to run at higher system speeds than standard SRAMs with comparable access times.

This paper outlines the basic architecture of a Synchronous SRAM that Motorola plans to introduce in the first half of 1988. We will highlight its advantages over standard SRAMs in high frequency computer system operation. This is followed by an application example for a MC68030 cache subsystem.

ARCHITECTURE AND OPERATION

ARCHITECTURE

A block diagram of the 16K×4 Synchronous SRAM is shown in Figure 1. This diagram shows all inputs, outputs, and control signals ($\overline{W}$, $\overline{S}$, and K) to the part; addresses (A0-A13), data in (D0-D3), data out (Q0-Q3), clock (K), chip select ($\overline{S}$), and write enable ($\overline{W}$). All inputs, outputs, write enable, and chip select are latched by the clock.

The latches are one of two types, either positive edge triggered or transparent. The positive edge triggered latches are latched by the rising edge of clock (K). The transparent latches are frozen when the clock is in the high state and open when it is in the low state. Our parts feature two of the possible combinations of input and output latches. The first part, the MCM6292, features edge triggered latches on the inputs and transparent latches on the outputs. Our second part, the MCM6293, has edge triggered latches on both inputs and outputs, to aid in pipelining data.

The output buffers on all of our parts are capable of driving 130 pF loads. The output buffers were designed to drive this load because in some systems the latches that they replace would be required to drive a comparable size load. Due to the size of load that the output buffers must drive, and the speed at which the part operates, we have added an extra ground pin (V_{SSQ}). This pin is the ground connection for all of our output drivers, and allows us to drive our outputs harder and also gives us noise immunity on the ground bus.

For systems that require a common I/O configuration we expect to offer the MCM6295 and the MCM6294, which are the MCM6292 and the MCM6293 with an asynchronous output enable ($\overline{G}$) option. These parts, the MCM6294 and the MCM6295, replace the chip select ($\overline{S}$) buffer with an asynchronous output enable ($\overline{G}$) buffer.

OPERATION

The operation of these parts is much the same as a standard 16K×4 SRAM except for the fact that the inputs and outputs are latched and the cycle begins with the low to high transition of the clock. The following examples will concentrate on a read and write cycle for both the MCM6292 and the MCM6293. The MCM6294 and MCM6295 read and write cycles are the same as the MCM6292 and the MCM6293 except that the outputs can be put into a high impedance state at any time by using output enable ($\overline{G}$).

During a read, see Figure 2, all inputs are latched into the part at the rising edge of the clock (K) in both the MCM6292 and the MCM6293. For the MCM6292, when clock goes high, the outputs become latched and are held in that state until the clock falls low. Since the output latches are transparent, during clock low time, there are two possible access times, t_{KHQV} and t_{KLQV}. These access times are dependent upon the high pulse width of the clock. If the high pulse width is less than the access time of the memory array the longer t_{KHQV} spec is the clock access time. However if the clock high pulse is longer than the memory array access time, the clock access time becomes t_{KLQV}. For the MCM6293 the

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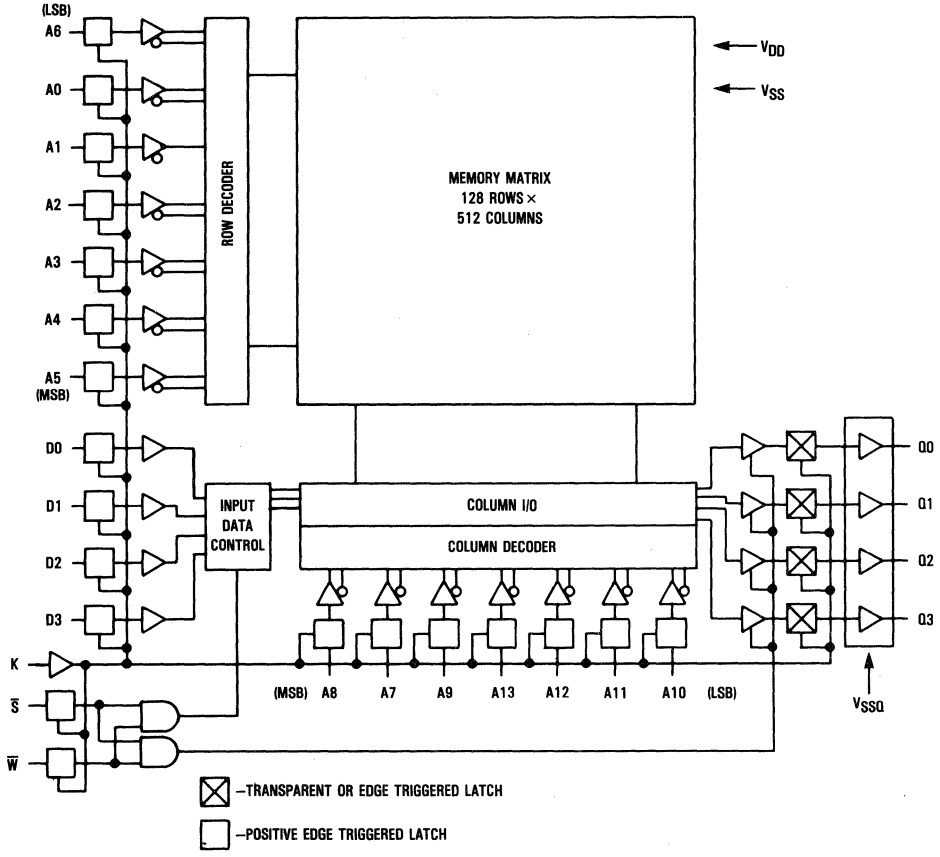

Figure 1. Synchronous SRAM Block Diagram

outputs transition only when the clock switches from low to high. The output data that is latched during the low to high transition of the clock is the data from the previous read cycle.

For the write cycle, see Figure 3, all inputs are handled in the same manner as in the read. Since both write enable and the input data are sampled on the rising edge of the clock the write becomes self timed. This eliminates the need for complex off chip write pulse generating circuitry. The outputs are put in a high impedance state t_{KLQZ} after the clock falls low for the MCM6292. In the MCM6293 the output buffers will not go into a high impedance state until the low to high transition of the clock at the beginning of the next cycle. The MCM6294 and the MCM6295 allow the user to put the output buffers into a high impedance state asynchronously by using the output enable input. This allows the user to put the output buffers into a high impedance state earlier in the cycle, which eases the data contention problem when the part is used in a common I/O system configuration.

SYSTEM ADVANTAGES (SRAM vs SSRAM)

SYSTEM DESCRIPTION AND TIMING

Figure 7 shows two examples of a 16K × 32 bit memory using standard parts. The systems shown require eighteen parts each, ten latches and eight 16K × 4 SRAMs, to implement the same function as eight synchronous SRAMs and no glue logic.

The functional equivalent of a MCM6292 is the standard 16K × 4 SRAM with edge triggered latches on the inputs and transparent latches on the outputs, as shown at the top of Figure 7. The parts used in this example are six 'F374 octal D-type flip flops, four 'F373 octal transparent latches, and eight 6288 16K × 4 SRAMs. The predicted timing diagram for the system is shown in Figure 4. This timing diagram compares the predicted system access with that of the MCM6292. In the timing diagrams an approximate skew of 5 ns was added to the address timing to allow for some propagation delay from the MPU or CPU. For the purpose of comparison, three timing

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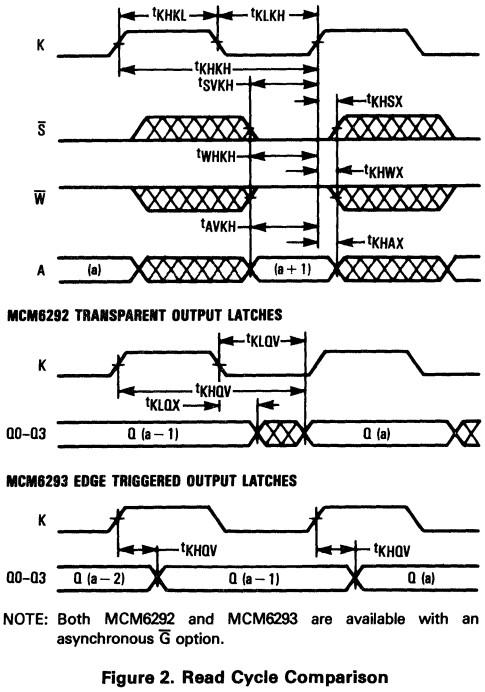
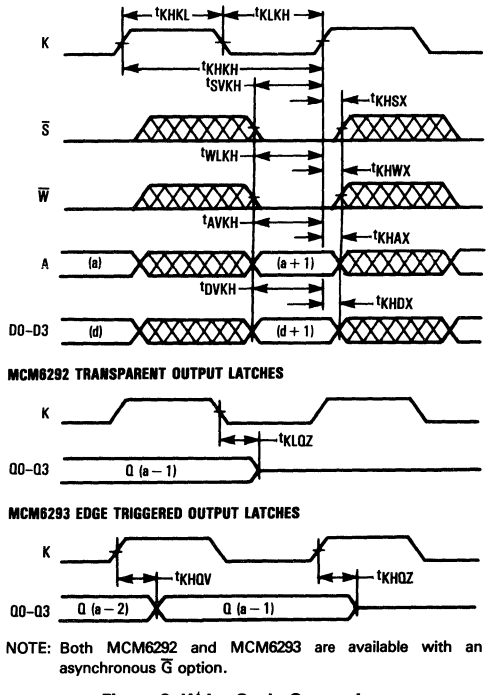


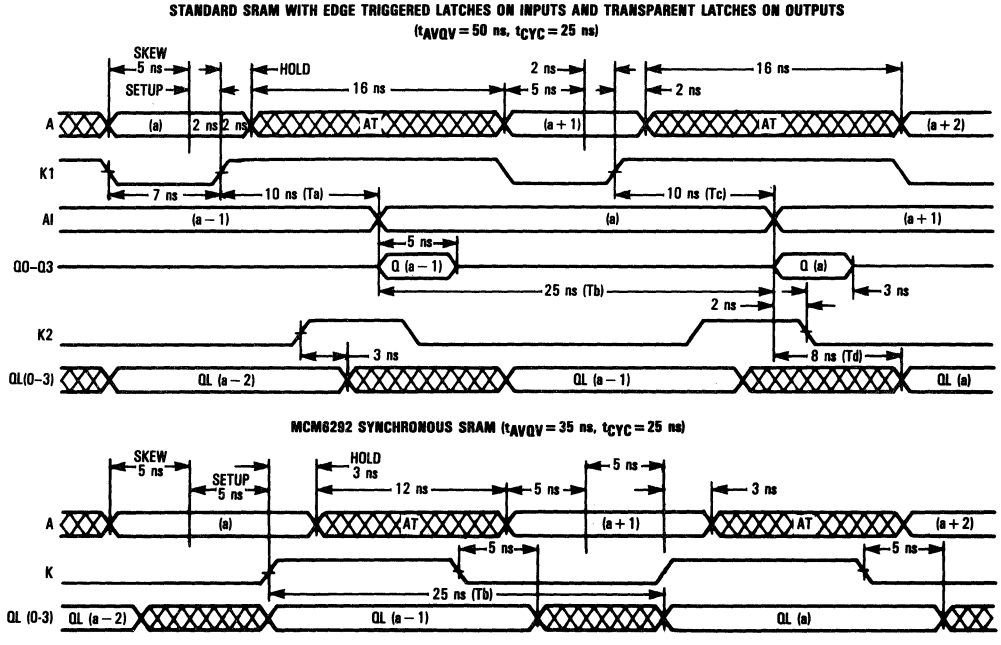
NOTE: Both MCM6292 and MCM6293 are available with an asynchronous $\overline{G}$ option.

Figure 2. Read Cycle Comparison



NOTE: Both MCM6292 and MCM6293 are available with an asynchronous $\overline{G}$ option.

Figure 3. Write Cycle Comparison



NOTE: AT—Address generation and transition time.

Figure 4. Standard SRAM vs MCM6292 Timing Diagram

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parameters were calculated, t_{CYC} (cycle time), t_{AVQV} (address valid to data out valid time), and t_{KQV} (address clock valid to data out valid time). The equations used to calculate each of the timing parameters for the standard SRAMs are as follows:

$$t_{CYC} = Ta + Tb - Tc$$
$$t_{KQV} = Ta + Tb + Td$$
$$t_{AVQV} = skew + setup + Ta + Tb + Td \ .$$

The equivalent timing parameters for the MCM6292 can be determined as follows:

$$t_{CYC} = Tb$$
$$t_{KQV} = Tb$$
$$t_{AVQV} = skew + setup + Tb \ .$$

The equivalent circuit for the MCM6293, as shown at the bottom of Figure 7, is a 16K × 4 SRAM with positive edge triggered latches on both inputs and outputs. For this example the parts used are, eight 6288 16K × 4 SRAMs and ten 'F374 octal D-type flip flops. The timing diagrams for this example are shown in Figure 5. The equations for calculating the timing parameters are as follows:

Standard SRAMs:

$$t_{CYC} = Ta + Tb - Tc$$
$$t_{KQV} = Ta + Tb + Td + Te$$
$$t_{AVQV} = skew + setup + Ta + Tb + Td + Te$$

MCM6293:

$$t_{CYC} = Tb$$
$$t_{KQV} = Tb + Te$$
$$t_{AVQV} = skew + setup + Tb + Te$$

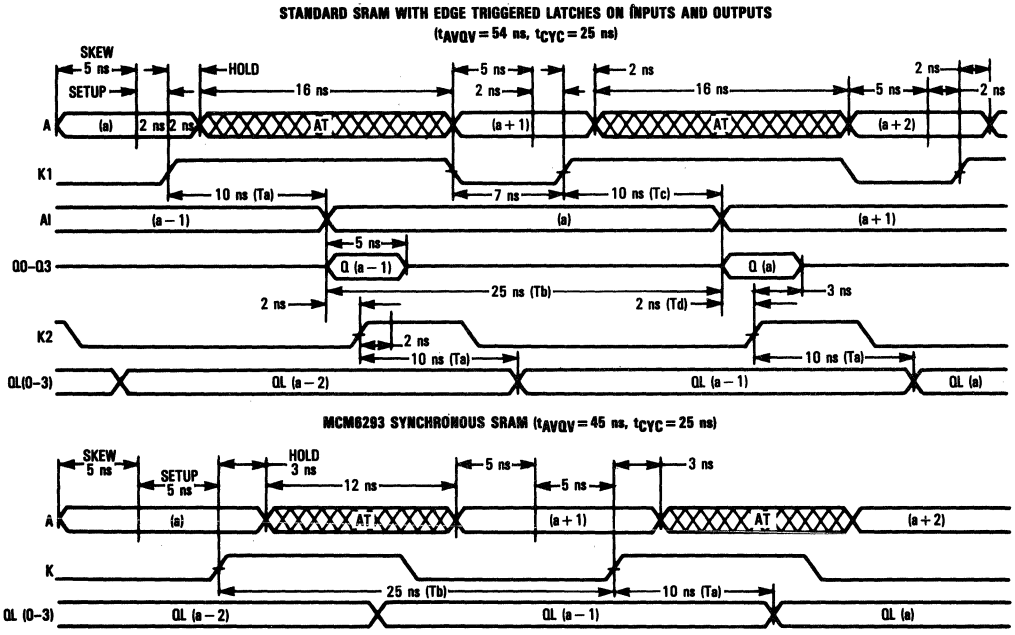
SYSTEM COMPARISONS

The timing parameters for the 25 ns 16K × 4 synchronous SRAMs and the equivalent circuits using 25 ns SRAMs are in Table 1. Also in Table 1 are timing parameters for other systems using progressively faster and more expensive SRAMs. From this table it can be determined that if either t_{AVQV} or t_{KQV} were the most important timing constraints a much faster SRAM would be needed to match the performance of the synchronous SRAM. For the performance of the system built with standard parts to match the performance of the 25 ns MCM6292, it would be necessary to use a 10 ns SRAM. Similarly, if the system used 25 ns MCM6293s the equivalent system made from standard parts would require 15 ns SRAMs.

Another important advantage of the synchronous parts over standard parts is the board level chip count; 18 parts are necessary when using standard SRAMs while only 8 parts are needed for the synchronous SRAM implementation. This is critical when board space is an important factor. Also, the fact that data and write enable are sampled on the rising edge of the clock, eliminates the need for complex write pulse generating circuitry. Finally, in order to get the high speed performance out of standard SRAMs, it requires precise timing and phase control of two clock signals (K1 and K2), while in the synchronous part only one clock (K) is needed.

APPLICATION: MC68030 CACHE SUBSYSTEM

The Synchronous SRAM combined with the Motorola MC68030 microprocessor illustrates the potential of this advanced memory architecture. The high frequency performance of microprocessors like the MC68030 can be impaired by having



NOTE: AT—Address generation and transition time.

Figure 5. Standard SRAM vs MCM6293 Timing Diagram

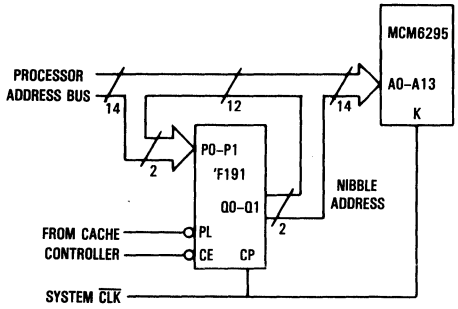


Figure 6. MC68030 Burst Read Addressing

to wait for slow memory to respond. For this example we will use a 16K by 32-bit cache system running at frequencies of up to 33-1/3 MHz. This does not mean that you can purchase MC68030 processors today at this speed, only that our 25 ns SSRAM will support this processor up to that speed. The MC68030 timings used for this example are extrapolated from the current 16.67 and 20 MHz specifications that exist today and are not intended to be the official specifications.

We will exploit the processor's burst read cycle which supports burst filling of its on-chip instruction and data caches, adding to the overall system performance. The on-chip caches are organized with a block size of four long words, so that there is only one tag for the four long words in a block. Since locality of reference is present to some degree in most programs, filling of all four entries when a single entry misses can be advantageous, especially if the time spent filling the additional entries is minimal. When the caches are burst-filled, data can be latched by the processor in as little as one clock for each 32 bits.[1]

The timing diagram shown in Figure 8 shows a burst read cycle (four 32-bit words read) in a 3-1-1-1 clock cycle configuration. The first word is read in 3 clock cycles and the remaining three words are read in one clock cycle each. The burst read cycle begins with a cache burst request ($\overline{CBREQ}$) from the processor followed by a cache burst acknowledge ($\overline{CBACK}$) from the memory controller. This means the processor is requesting a burst cycle and the accessed memory can comply. During the burst cycle the processor supplies the starting address in the normal synchronous fashion and holds it valid until all four long words are read. It does not provide the next three addresses required to complete the burst fill, so they must be generated off chip. For this example we used a 'F191 counter whose control signals, PL and $\overline{CE}$, are generated in a cache controller. The clock input, CP ($\overline{CLK}$), is the opposite phase of the system clock. The SSRAM operates with the same inverted system clock ($\overline{CLK}$) and receives its addresses from two sources; A2-A13 are supplied from the processor's address bus, and A0-A1 are supplied from the 'F191 counter to allow nibble counting as shown in Figure 6.

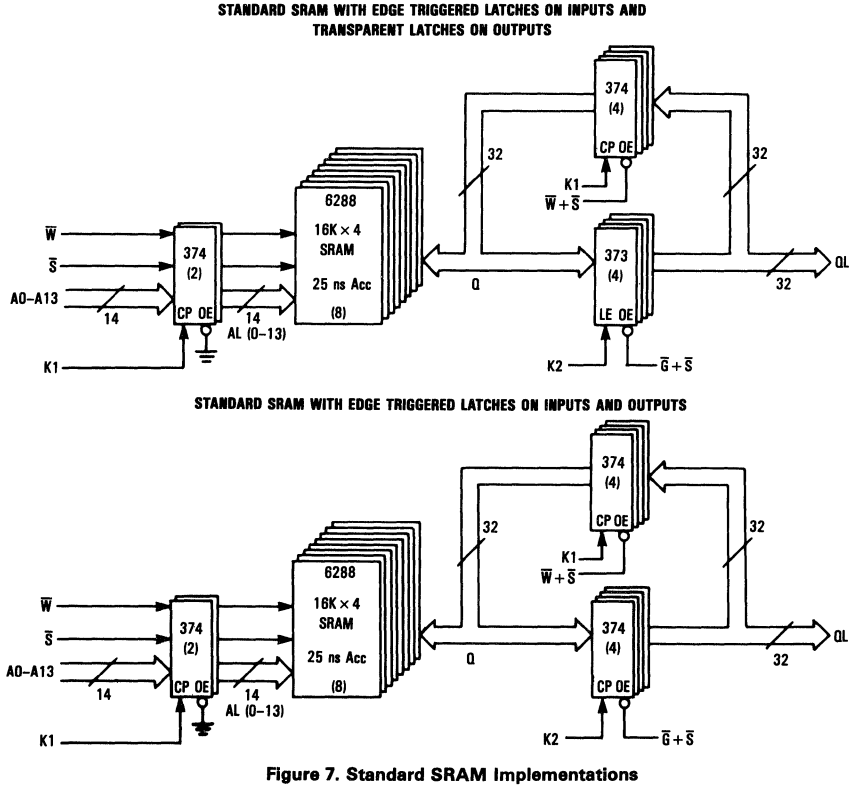
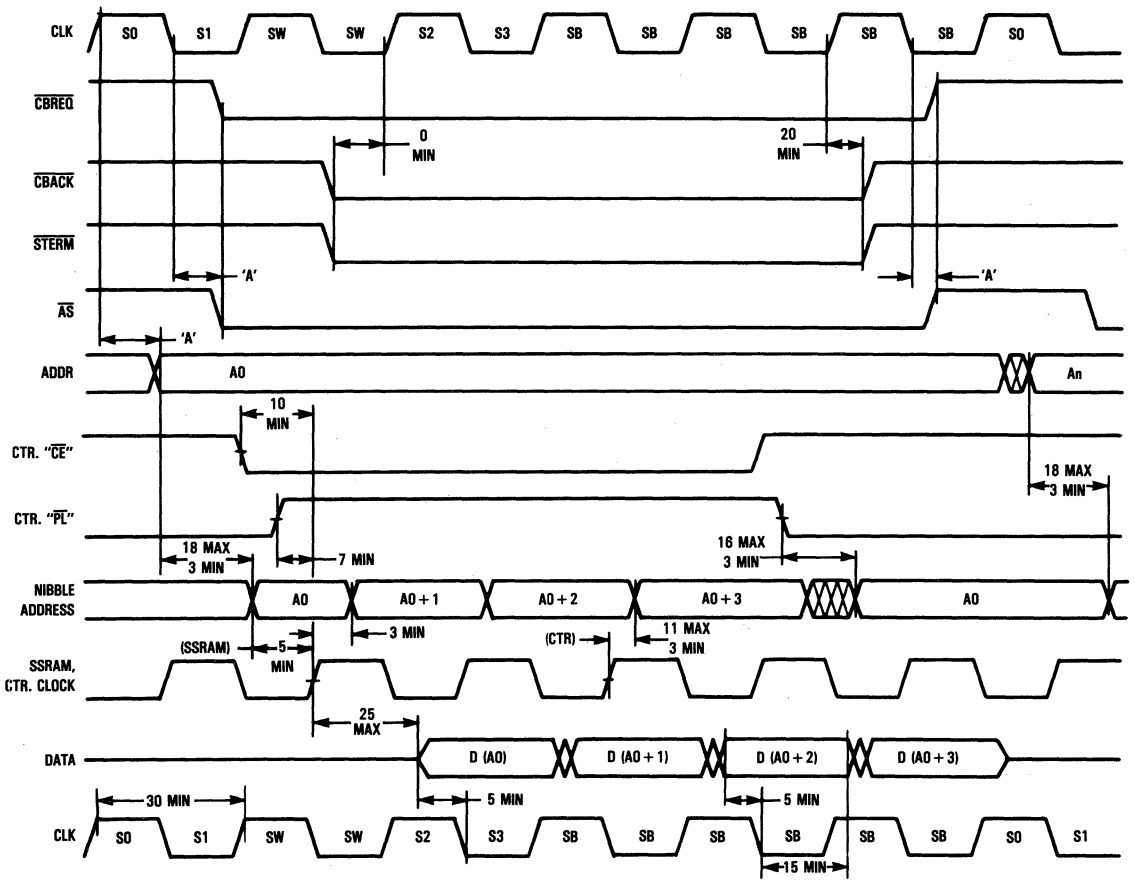


Figure 7. Standard SRAM Implementations



NOTES: 'A' ~ (minimum clock period)/2 CTR. = counter ('F191)

Figure 8. MC68030 Burst Fill Timing

Table 1. Timing Comparisons Between SSRAMs and SRAMs

Timings	25 ns SSRAM		25 ns SRAM		20 ns SRAM		15 ns SRAM		10 ns SRAM	
	Trans. Output	Edge Trig. Output	Trans. Output	Edge Trig. Output	Trans. Output	Edge Trig. Output	Trans. Output	Edge Trig. Output	Trans. Output	Edge Trig. Output
t_{CYC}	25 ns	25 ns	25 ns	25 ns	20 ns	20 ns	15 ns	15 ns	10 ns	10 ns
t_{AVQV}	35 ns	45 ns	50 ns	54 ns	45 ns	49 ns	40 ns	44 ns	35 ns	39 ns
t_{KQV}	25 ns	35 ns	43 ns	43 ns	38 ns	38 ns	33 ns	33 ns	28 ns	28 ns

The timing begins with the request, the acknowledgment and the generation of the first address. This address is used to access one of the four long words. Two low order address signals from this address must also be loaded into the counter. At the beginning of the cycle the parallel load signal for the counter is enabled, the address is then loaded in and the PL signal can be disabled. The counter will provide the memory this first address a propagation delay later and then increment it on successive clock edges to supply the memory with the remaining three needed addresses. After receiving all four 32-bit words the processor is free to continue.

A similar system built using standard MCM6288 (16K × 4) type SRAMs would require the use of off-chip input and output latches ('F373 or 'F374 type) in addition to the counter. It would require four chips to perform the latching function for 32-bit data in, and four chips to latch the 32-bit data out, for a total of eight additional 20 pin packages added to the memory PC board. This standard SRAM cache system would also require additional logic in the cache controller to support the write pulse, associated write enable and data in timing for write cycles, and the generation of a second clock (LE or CP) to separately control the input and output latches. To attain the cache system speed of 33-1/3 MHz would require a SRAM access time of approximately one bin faster than the SSRAM. In addition the external glue logic would have to be faster than what is currently offered in the 74F series logic.

SUMMARY

There are many applications for high-speed Synchronous Static RAMs. The integration of latches, self timed writes, bus drive capability, and clock control greatly simplifies system level implementation and ease of use. These features will allow SSRAMs to continue to support higher frequency system operation. Depending on the application, Synchronous Static RAMs can provide up to a 10 to 15 ns improvement in system access time over SRAMs that spec the same chip speeds. They save precious board space by reducing the chip count, and simplify controller design for latch control and write cycles.

ACKNOWLEDGMENTS

The authors would like to thank Brian Branson and Bill Martino for their inputs and comments that helped complete this paper. And special thanks to Richard Crisp for his MC68030 cache system timing analysis.

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2. Motorola Semiconductor Technical Data: "Fast and LS TTL Data", 1986.

Motorola Inc. can provide the usual promotional and technical literature associated with the Synchronous Static RAM family.

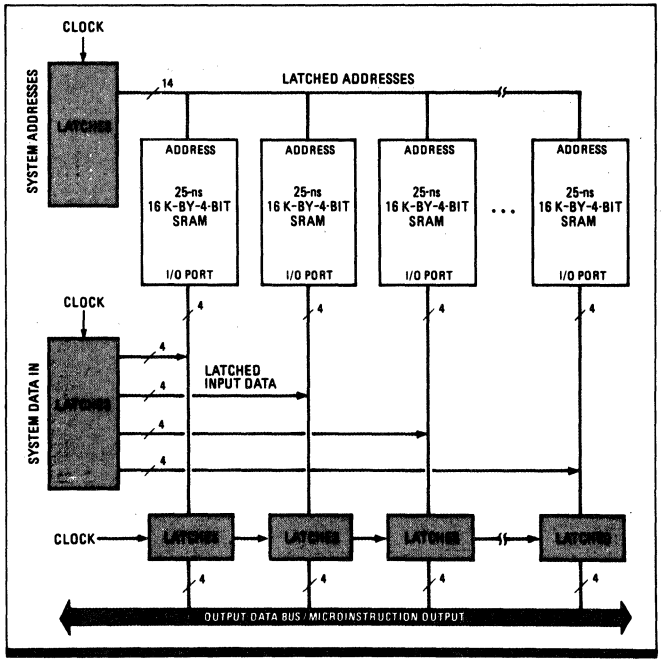
MOTOROLA'S RADICAL SRAM DESIGN SPEEDS SYSTEMS 40%

Key to higher throughput is a synchronous clocked architecture and on-chip I/O latches; the combination cuts interconnection delay by up to 20 ns

by Bernard C. Cole

Engineers at Motorola Inc.'s MOS Memory Products Division are taking a radically different approach from the current asynchronous architecture for static random-access memories. They are developing a synchronous architecture the company claims will improve system throughput by as much as 40% and will reduce system component count by as much as 50%.

The keys to the Austin, Texas, division's new architecture are: replacing the traditional self-clocked address-transition-detection circuitry, found in conventional asynchronous SRAMs, with a synchronous clocked architecture, and adding critical input and output latches on-chip. The combination of these features eliminates as much as 8 to 10 ns of interconnection delay on input and on output, says William Martino, the division's design manager for specialized memories. It also eliminates circuitry often required to make asynchronous devices appear synchronous in high-performance cache-memory systems, which depend heavily on the synchronization of critical timing parameters. Also incorporated on the chip are drive transistors capable of driving buses with capacitive loads of up to 130 pF without additional external circuitry. Motorola designers also enlarged the geometries to increase the inherent drive capability of the devices.



1. ASYNCHRONOUS. Using asynchronous SRAMs, designers of high-performance synchronous systems must incorporate latches on the inputs and outputs, adding 15 to 20 ns of delay.

The new architecture has been incorporated into four initial products that are members of a new family of 16-Kbit-by-4-bit SRAMs with cycle times ranging from 25 to 35 ns and access times in the 10 to 35 ns range. This equals that of comparably sized asynchronous SRAMs fabricated with the same 1.5-μm double-metal CMOS process [*Electronics*, Aug. 7, 1986, p. 81], says Frank Miller, synchronous SRAM project leader at the division. But Miller emphasizes that the elimination of as much as 20 ns of interconnection delay can almost double system-level performance.

Motorola expects to offer samples of the four clocked synchronous SRAM parts within about a month and plans to be in volume production by the end of the fourth quarter. Two of the devices, the MCM6292 and 6295, incorporate level-sensitive transparent latches,

whereas the MCM6293 and 6294 use positive-edge-triggered latches. Also the 6294 and 6295 each have an output enable pin that allows the user asynchronous control of the output buffers, allowing the parts to be used in common I/O at the board level. All the devices feature an active ac power dissipation of 600 mW and an active dc power of only 100 mW.

The advantages of Motorola's new family of synchronous SRAMs outweigh the advantages of asynchronous devices, Martino says. In asynchronous devices, great reliance is placed on address-transition detection, a self-clocking scheme that uses the address-signal transition, or edge, as a reference to synchronizing all operations on the chip to that signal. Martino says that asynchronous SRAMs are widely used because they allow and recognize address changes at any time. As a result, no external global clock is necessary to access data, making them easy to use. Also, compared with dynamic RAMs, asynchronous SRAMs take much less external circuitry, says Miller. Because they are free-running, the addresses can be changed whenever needed, and they are very easy to control.

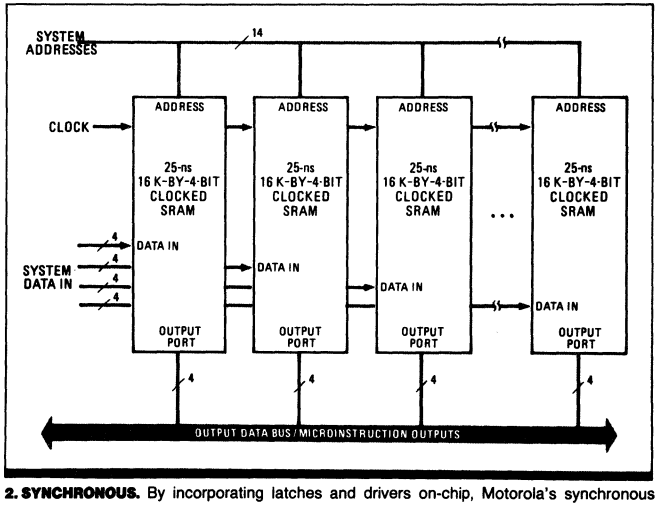
Although they are easy to use, asynchronous SRAMs must be surrounded by considerable external logic (see fig. 1) in many applications in high-performance processor systems such as writable control stores, data caches, and cache-tag memories [*Electronics*, June 11, 1987, p. 78] that require synchronous operation. The extra circuitry imposes a considerable performance penalty, and that can be a problem in cache applications in particular, says Martino, where the speed of memory typically must be at least an order of magnitude faster than main memory. Also, for a cache to work properly, critical timing relationships must be preserved so that a variety of simultaneous operations can be coordinated, such as searching the tag store, getting data out of cache, and replacing proper entries in the cache. The added delay of the external logic can make it difficult to preserve these relationships.

When system speeds were in the 200-ns range, Miller says, the additional 10-to-20-ns penalty of this external logic could be tolerated. "But with processor speeds improving so dramatically, now pushing below 100 ns toward 50 ns, this is a penalty that is critical, especially since the speed of the external logic has not kept pace with the improvements in speed at the chip level."

Depending on the type of register involved and the process used, the delay time, even with high-performance logic families, can be reduced to no more than 7 to 10 ns, says Martino. As a result, most speed improvements have come by pushing the speed of the memory chips themselves. But, as processors speed up, memories with sufficiently low access times are getting harder and harder to produce inexpensively, Martino says. Current 25-to-35-ns asynchronous SRAMs are barely adequate, he says. And newer processors will require a system throughput of no more than 35 to 40 ns. For such throughputs, SRAMs must be pushed to below 10 ns, only achievable now with bipolar and BiCMOS circuits, but at much higher power. "However, even if parts are pushed down to 1 ns and under, there is still that 10 ns on the input and another 10 ns on the output to deal with," says Martino.

The most important element in Motorola's new SRAM architecture (see fig. 2) is the incorporation of the external input and output latches necessary for synchronous operation on board. This design considerably simplifies system design and reduces interconnection delay. "By pulling all of that glue logic on board, it is no longer necessary to drive a large bus to TTL levels," says Martino. "It is now done on-chip, reducing the 10-ns delay down to picosecond levels. This allows the use of a 25-ns part for a 25-to-30-ns bus, rather than using more expensive, power-hungry 10- and 15-ns parts for the same chore."

The Motorola architecture uses address-input latches to hold the addresses so that the processor does not have to hold the addresses valid for the entire cycle. A similar function is served by the data latches on the input. The latches on the output, however, serve a dual function. First, they provide a longer setup and hold time over which the data is valid on the bus, necessary in most processing systems. With a



2. SYNCHRONOUS. By incorporating latches and drivers on-chip, Motorola's synchronous SRAM reduces chip count by more than 50% and reduces interconnection delay.

standard SRAM at minimum cycle time, that time is about 5 ns without any external latching. This is not enough time for most systems, which require the data to be on the bus for at least 15 to 20 ns, for the processor to receive the valid data. The other function of the latches is to provide the extra drive needed to drive the buses with capacitive loads of up to 130 pF.

The designers of the new SRAMs have eliminated the address-detection-transition circuitry; now they use on-chip clock input for a synchronous clocking scheme

Also incorporated on-chip to support the synchronous operation of the latches is a clock input that controls when the latches are transparent and when they are brought into play. Usually this clock input is a derivative of the system clock; that is, the latches are controlled by the edge of the system clock.

The Motorola designers have eliminated the address-detection-transition circuitry in the new SRAMs. Instead, they use the on-chip clock input to incorporate a synchronous clocking scheme in which the necessary address, data, chip-select, and write-enable information previously brought on board the chip by the address-detection-transition circuitry is now accessed at the beginning of the cycle in reference to the external clock, rather than to the address edge as in the asynchronous scheme. The technique, says Martino, is similar to how a DRAM brings in its addresses with setup and hold times in relation to a read-access or column-access signal input. "Since this device employs a clock with a high-going edge at the beginning of each cycle, it is no longer necessary to detect address- transitions," he says. "The system will tell the chip when to supply the necessary information by providing the clock at the appropriate time."

To eliminate the external drive circuitry, the inherent drive capability of the devices was increased fourfold, says Miller. So Motorola designers enlarged the geometries used to fabricate the pull-up and pull-down transistors, typically on the order of 1,500 μm wide, compared with 400- to 600-μm widths on the standard 30-pF devices, and as small as 6 μm in the memory array and 80 μm in the peripheral circuitry. Moreover, to achieve higher speed in spite of the higher drive currents, n-channel devices, which are only output devices, were used rather than the slower p-channel devices. Furthermore, these output devices were speeded up by incorporating a separate ground-supply pin for the output drivers. "This allowed us to burn more current in the output drivers without corrupting the operation of the rest of the circuit," Miller says.

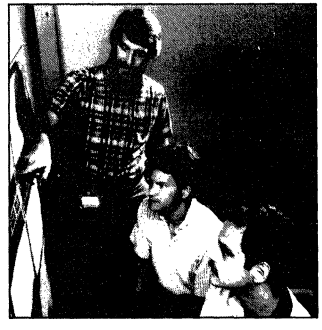
Although this required a substantial increase in the area devoted to the drive circuitry, the chip size, 146 by 404 mils, is not substantially larger than comparable 64-Kbit asynchronous SRAMs. The extra area required for the larger drivers and for the internal clocking circuitry is offset by the area eliminated by removal of the address-transition-detection circuitry required on asynchronous parts, Martino says. □

INGENIOUS SRAM DESIGN WAS DONE IN REMARKABLY SHORT TIME

For a memory device of such complexity and ingenious design, Motorola's new clocked synchronous static random-access-memory design was completed in a remarkably short time—only 12 months. Moreover, most of the work was done by a four-person design team: William Martino, design manager for specialized memories; Frank Miller, synchronous SRAM project leader; chip designer Scott Remington; and layout engineer Richard Southerland.

One reason for the fast turnaround was that the array and much of the peripheral circuitry is identical to what was used in the company's family of asynchronous 64-Kbit SRAMs, says Miller. "All we had to do was strip off those portions of the circuit relating to the asynchronous operation and replace them with new synchronous elements."

The team drew from two sources for the features incorporated into the synchronous design—including their cumulative design experience. Miller has seven years' experience in memory design. Remington, an eight-year Motorola veteran, worked on the company's 64-Kbit and 1- Mbit DRAMs. Southerland, a five-year Texas Instruments veteran, worked on most of Motorola's asynchronous SRAMs in his two years with the company.



EXPERTS. Miller, Southerland, and Remington, from left, are old hands at memory design.

The other source was extensive input from Motorola's customers. "We spent several months defining a variety of special-application memory devices, from dual-port SRAMs and video DRAMs to content-addressable memories," says Miller. "But when we started taking these designs around to customers for input, we found they were most concerned with ways to make standard parts work better. For designers of high-performance systems using cache architectures, one of the largest common denominators was complaints that they had to surround the asynchronous parts with a variety of glue logic to operate appropriately in a synchronous environment.

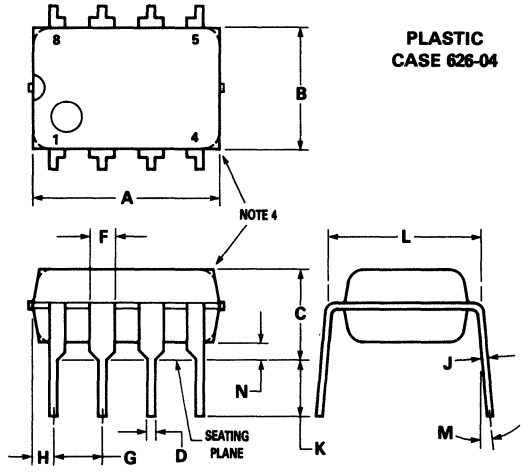
"The key is listening to the customers, finding out what their specific complaints are, and coming up with parts that satisfy those needs."

Mechanical Data

14

Package availability and ordering information are given on the individual data sheets.

8-LEAD PACKAGE

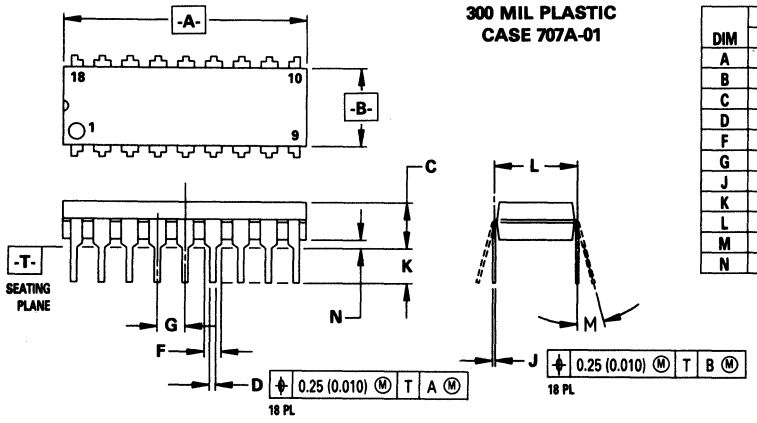


PLASTIC
CASE 626-04

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	—	10°	—	10°
N	0.51	0.76	0.020	0.030

NOTES:
1. LEAD POSITIONAL TOLERANCE:
   ⌖ ϕ 0.13 (0.005) Ⓜ | T | A Ⓜ | B Ⓜ
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
4. DIMENSIONS A AND B ARE DATUMS.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

18-LEAD PACKAGE

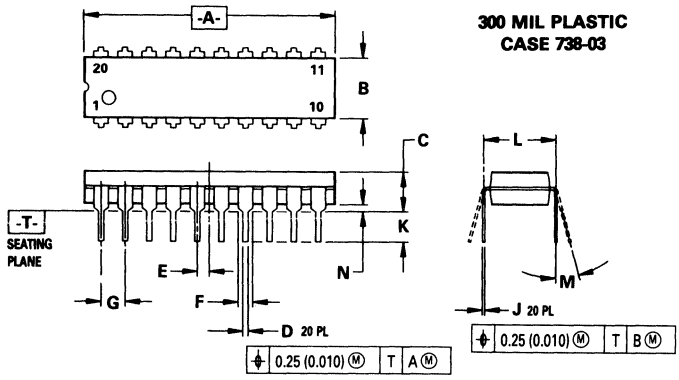


300 MIL PLASTIC
CASE 707A-01

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	21.85	22.35	0.860	0.880
B	7.12	7.49	0.280	0.295
C	3.56	4.57	0.140	0.180
D	0.36	0.55	0.014	0.022
F	1.27	1.77	0.050	0.070
G	2.54 BSC		0.100 BSC	
J	0.21	0.30	0.008	0.012
K	2.93	3.42	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION "L" TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.

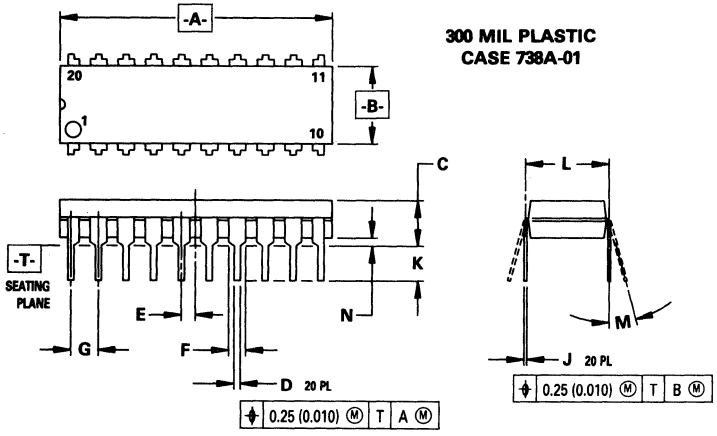
14



300 MIL PLASTIC
CASE 738-03

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	25.66	27.17	1.010	1.070
B	6.10	6.60	0.240	0.260
C	3.81	4.57	0.150	0.180
D	0.39	0.55	0.015	0.022
E	1.27 BSC		0.050 BSC	
F	1.27	1.77	0.050	0.070
G	2.54 BSC		0.100 BSC	
J	0.21	0.38	0.008	0.015
K	2.80	3.55	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION "L" TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.



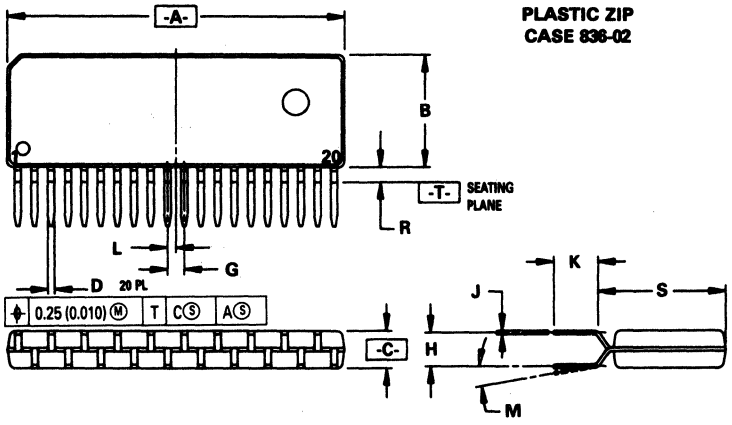
300 MIL PLASTIC
CASE 738A-01

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	24.39	24.89	0.960	0.980
B	7.12	7.49	0.280	0.295
C	3.69	4.44	0.145	0.175
D	0.39	0.55	0.015	0.022
E	1.27 BSC		0.050 BSC	
F	1.27	1.77	0.050	0.070
G	2.54 BSC		0.100 BSC	
J	0.21	0.38	0.008	0.015
K	2.80	3.55	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION "L" TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.

14

20-LEAD PACKAGES (Continued)

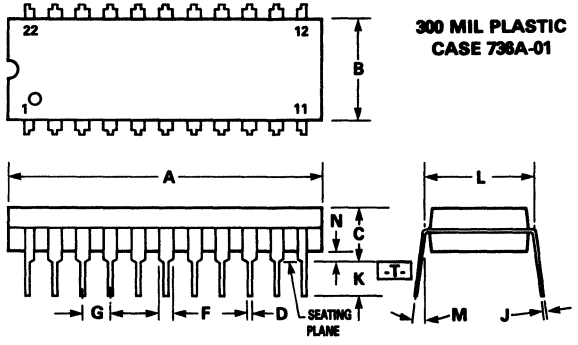


PLASTIC ZIP
CASE 836-02

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	25.53	25.90	1.005	1.020
B	8.59	8.89	0.338	0.350
C	2.75	2.94	0.108	0.116
D	0.45	0.55	0.018	0.022
G	1.27 BSC		0.050 BSC	
H	2.44	2.64	0.097	0.103
J	0.23	0.33	0.009	0.013
K	3.18	3.55	0.125	0.140
L	0.64 BSC		0.025 BSC	
M	0°	4°	0°	4°
R	0.89	1.39	0.035	0.055
S	9.66	10.16	0.380	0.400

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION "H" TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSIONS "A", "B", AND "S" DO NOT INCLUDE MOLD PROTRUSION.
5. MOLD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010).

22-LEAD PACKAGE

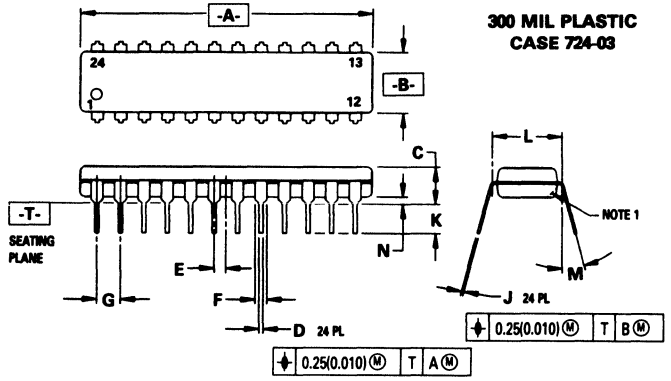


300 MIL PLASTIC
CASE 736A-01

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	25.65	27.17	1.010	1.070
B	6.10	6.60	0.240	0.260
C	3.74	4.57	0.155	0.180
D	0.38	0.55	0.015	0.022
F	1.27	1.77	0.050	0.070
G	2.54 BSC		0.100 BSC	
J	0.20	0.38	0.008	0.015
K	2.79	3.55	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

NOTES:
1. DIMENSION A IS A DATUM. T IS BOTH A DATUM AND A SEATING PLANE.
2. POSITIONAL TOLERANCE FOR D DIMENSION; 22 PL:
   0.25 (0.010) M -T- A M
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSIONING AND TOLERANCING PER Y14.5 M, 1982.
5. CONTROLLING DIMENSION: INCH.

14

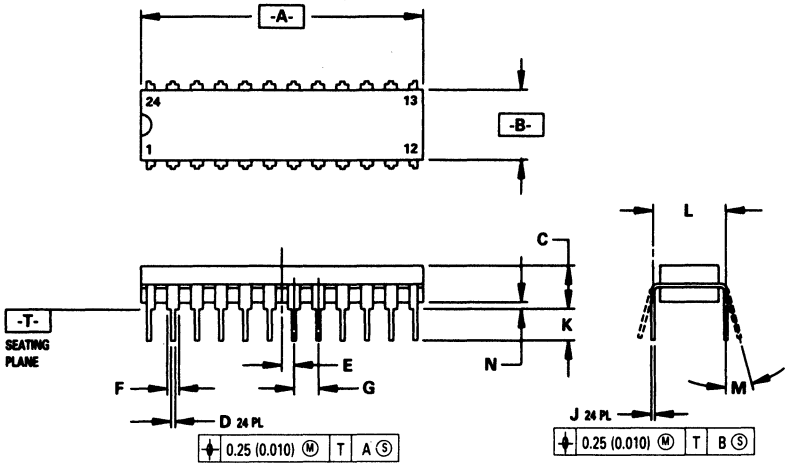


300 MIL PLASTIC
CASE 724-03

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	31.25	32.13	1.230	1.265
B	6.35	6.85	0.250	0.270
C	3.69	4.44	0.145	0.175
D	0.38	0.51	0.015	0.020
E	1.27 BSC		0.050 BSC	
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
J	0.18	0.30	0.007	0.012
K	2.80	3.55	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

NOTES:
1. CHAMFERRED CONTOUR OPTIONAL.
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH.

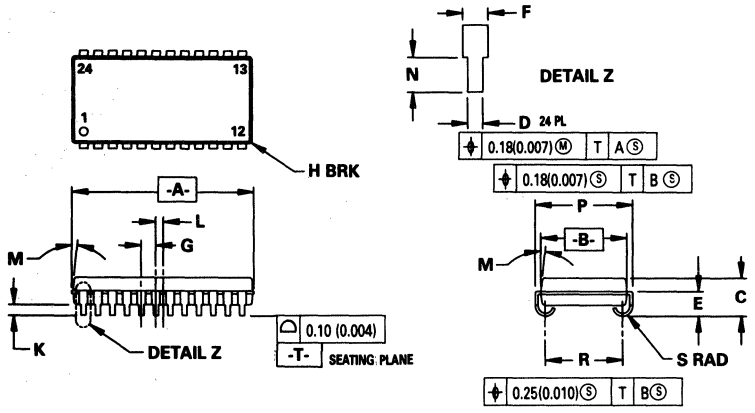
300 MIL PLASTIC
CASE 724A-01



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	29.47	29.71	1.160	1.170
B	7.12	7.62	0.280	0.300
C	3.81	4.57	0.150	0.180
D	0.39	0.53	0.015	0.021
E	1.27 BSC		0.050 BSC	
F	1.15	1.39	0.045	0.055
G	2.54 BSC		0.100 BSC	
J	0.21	0.30	0.008	0.012
K	3.18	3.42	0.125	0.135
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION A AND B DOES NOT INCLUDE MOLD FLASH. MAXIMUM MOLD FLASH 0.25 (0.010).

300 MIL SOJ
CASE 810A-01

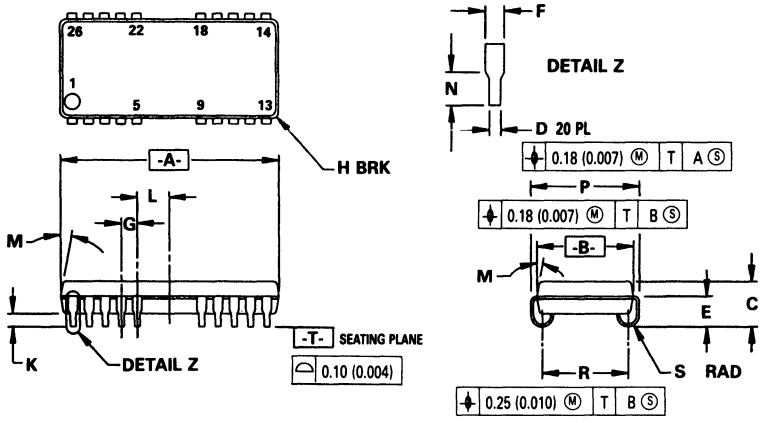


	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	15.75	16.00	0.620	0.630
B	7.50	7.74	0.295	0.305
C	3.26	3.75	0.128	0.148
D	0.39	0.50	0.015	0.020
E	2.24	2.48	0.088	0.098
F	0.67	0.81	0.026	0.032
G	1.27 BSC		0.050 BSC	
H	—	0.50	—	0.020
K	0.89	1.14	0.035	0.045
L	0.64 BSC		0.025 BSC	
M	0°	5°	0°	5°
N	0.89	1.14	0.035	0.045
P	8.51	8.76	0.335	0.345
R	6.61	7.11	0.260	0.280
S	0.77	1.01	0.030	0.040

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. DIMENSION "A" AND "B" DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
3. CONTROLLING DIMENSION: INCH.
4. DIM "R" TO BE DETERMINED AT DATUM -T-.

14

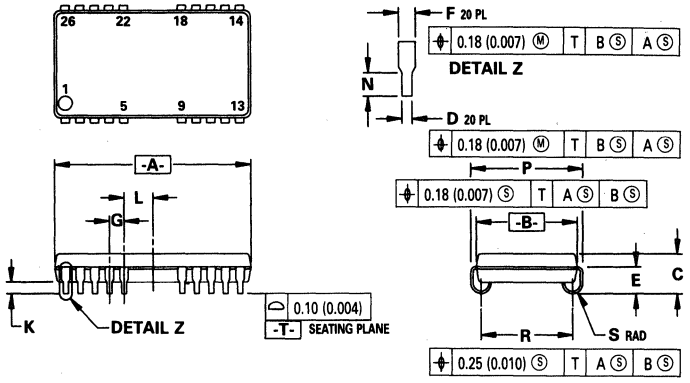
300 MIL SOJ
CASE 822-03



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	17.02	17.27	0.670	0.680
B	7.50	7.74	0.295	0.305
C	3.26	3.75	0.128	0.148
D	0.39	0.50	0.015	0.020
E	2.24	2.48	0.088	0.098
F	0.67	0.81	0.026	0.032
G	1.27 BSC		0.050 BSC	
H	—	0.50	—	0.020
K	0.89	1.14	0.035	0.045
L	2.54 BSC		0.100 BSC	
M	0°	10°	0°	10°
N	0.89	1.14	0.035	0.045
P	8.39	8.63	0.330	0.340
R	6.61	6.98	0.260	0.275
S	0.77	1.01	0.030	0.040

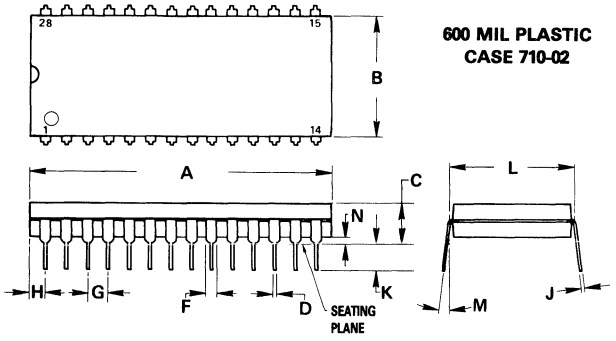
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION A & B DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIM R TO BE DETERMINED AT DATUM -T-.
5. FOR LEAD IDENTIFICATION PURPOSES, PIN POSITIONS 6, 7, 8, 19, 20, & 21 ARE NOT USED.

350 MIL SOJ
CASE 822A-01



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	17.02	17.27	0.670	0.680
B	8.77	9.01	0.345	0.355
C	3.26	3.75	0.128	0.148
D	0.41	0.50	0.016	0.020
E	2.24	2.48	0.088	0.098
F	0.67	0.81	0.026	0.032
G	1.27 BSC		0.050 BSC	
K	0.64	—	0.025	—
L	2.54 BSC		0.100 BSC	
N	0.89	1.14	0.035	0.045
P	9.66	9.90	0.380	0.390
R	7.88	8.25	0.310	0.325
S	0.77	1.01	0.030	0.040

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION A & B DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION A & B INCLUDE MOLD MISMATCH AND ARE DETERMINED AT THE PARTING LINE.
5. DIM R TO BE DETERMINED AT DATUM -T-.
6. FOR LEAD IDENTIFICATION PURPOSES, PIN POSITIONS 6, 7, 8, 19, 20, & 21 ARE NOT USED.

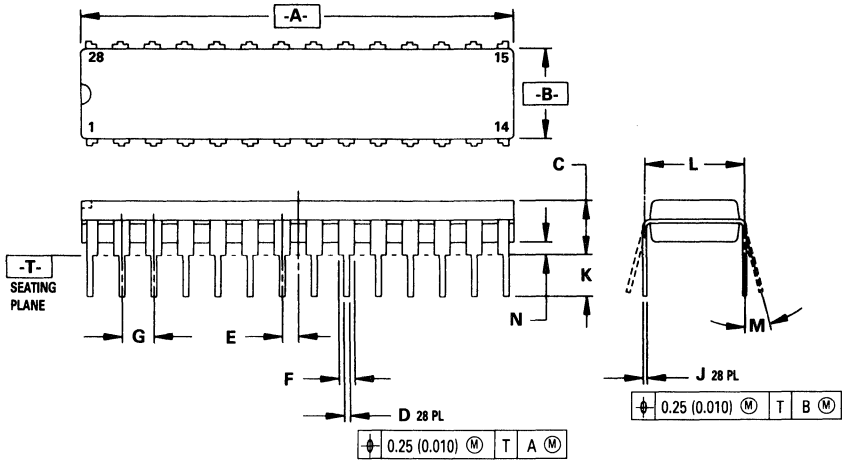


600 MIL PLASTIC
CASE 710-02

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	36.45	37.21	1.435	1.465
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm(0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

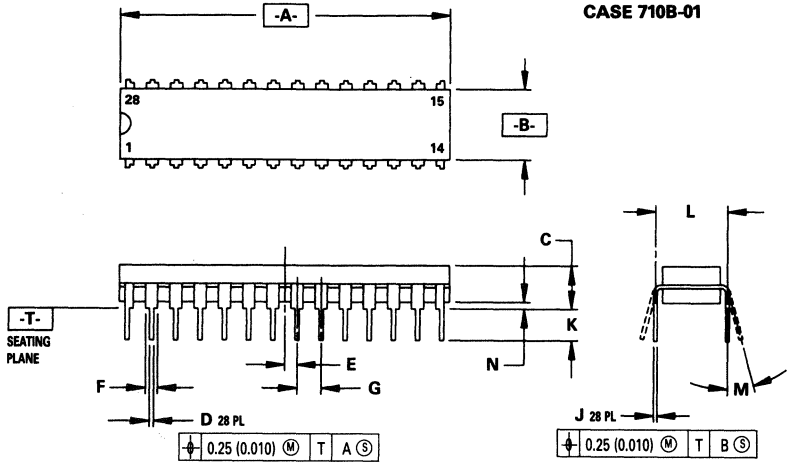
300 MIL PLASTIC
CASE 710A-01



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	34.17	34.29	1.345	1.350
B	6.86	7.36	0.270	0.290
C	—	4.31	—	0.170
D	0.41	0.50	0.016	0.020
E	1.27 BSC		0.050 BSC	
F	1.15	1.39	0.045	0.055
G	2.54 BSC		0.100 BSC	
J	0.21	0.30	0.008	0.012
K	3.18	3.42	0.125	0.135
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.39	—	0.015	—

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

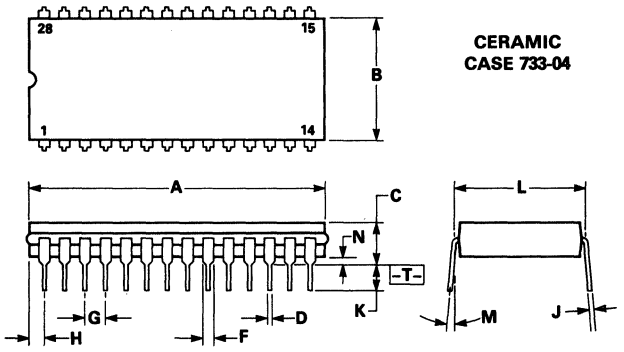
300 MIL PLASTIC
CASE 710B-01



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	34.55	34.79	1.360	1.370
B	7.12	7.62	0.280	0.300
C	3.81	4.57	0.150	0.180
D	0.39	0.53	0.015	0.021
E	1.27 BSC		0.050 BSC	
F	1.15	1.39	0.045	0.055
G	2.54 BSC		0.100 BSC	
J	0.21	0.30	0.008	0.012
K	3.18	3.42	0.125	0.135
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION A AND B DOES NOT INCLUDE MOLD FLASH. MAXIMUM MOLD FLASH 0.25 (0.010).

CERAMIC
CASE 733-04

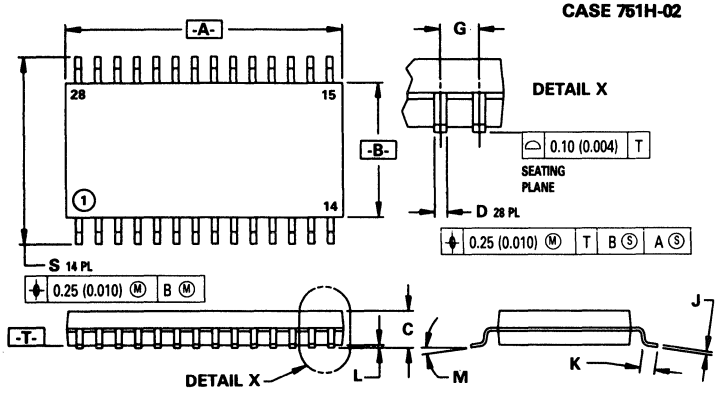


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	36.45	37.84	1.435	1.490
B	12.70	15.36	0.500	0.605
C	4.06	5.84	0.160	0.230
D	0.38	0.55	0.015	0.022
F	1.27	1.65	0.050	0.065
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.27	0.020	0.050

NOTES:
1. DIM -A- IS DATUM.
2. POSITIONAL TOL FOR LEADS:
   ϕ 0.25 (0.010) M T A M
3. -T- IS SEATING PLANE.
4. DIM A AND B INCLUDES MENISCUS.
5. DIM -L- TO CENTER OF LEADS WHEN FORMED PARALLEL.
6. DIMENSIONING & TOLERANCING PER Y14.5, 1982.
7. CONTROLLING DIM: INCH.

14

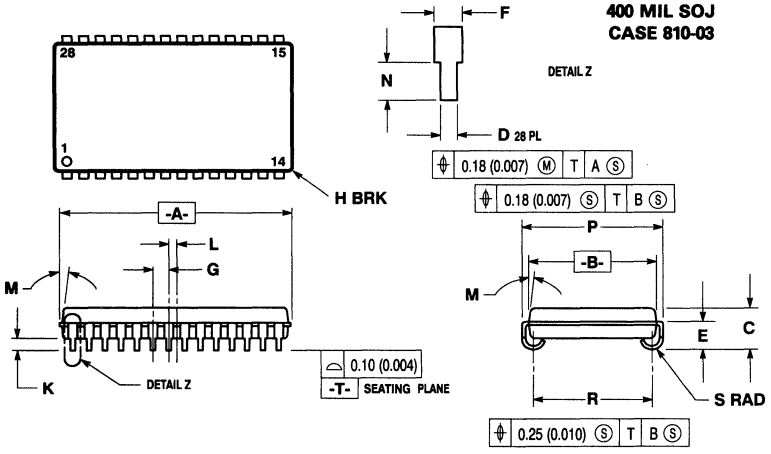
300 MIL SOG
CASE 751H-02



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	17.70	18.50	0.697	0.728
B	8.23	8.90	0.324	0.350
C	2.04	2.50	0.080	0.098
D	0.35	0.50	0.014	0.020
G	1.27 BSC		0.050 BSC	
J	0.14	0.25	0.0060	0.0098
K	0.40	1.27	0.016	0.050
L	0.05	0.20	0.002	0.008
M	0°	8°	0°	8°
S	11.50	12.10	0.453	0.476

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIM: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

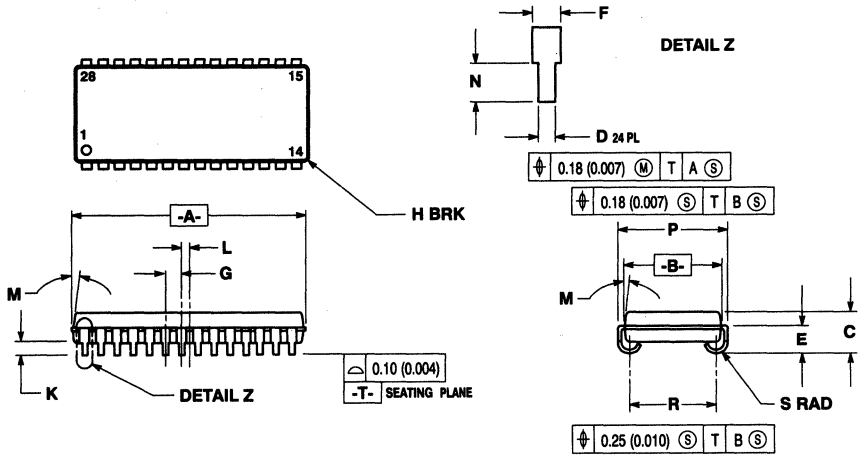
400 MIL SOJ
CASE 810-03



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	18.29	18.54	0.720	0.730
B	10.04	10.28	0.395	0.405
C	3.26	3.75	0.128	0.148
D	0.39	0.50	0.015	0.020
E	2.24	2.48	0.088	0.098
F	0.67	0.81	0.026	0.032
G	1.27 BSC		0.050 BSC	
H	—	0.50	—	0.020
K	0.89	1.14	0.035	0.045
L	0.64 BSC		0.025 BSC	
M	0°	5°	0°	5°
N	0.76	1.14	0.030	0.045
P	11.05	11.30	0.435	0.445
R	9.15	9.65	0.360	0.380
S	0.77	1.01	0.030	0.040

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. DIMENSION A & B DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
3. CONTROLLING DIMENSION: INCH.
4. DIM R TO BE DETERMINED AT DATUM -T-.

300 MIL SOJ
CASE 810B-03

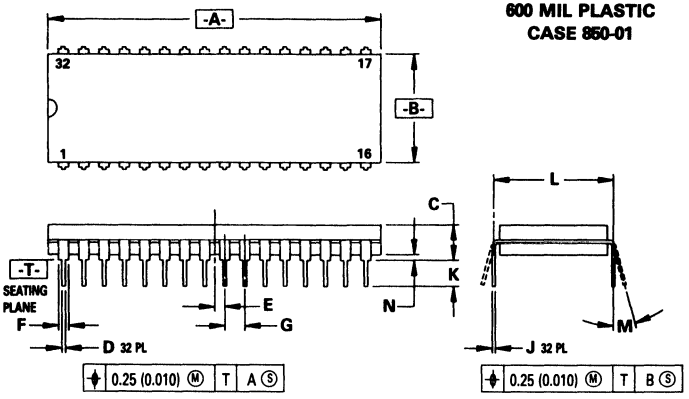


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.29	18.54	0.720	0.730
B	7.50	7.74	0.295	0.305
C	3.26	3.75	0.128	0.148
D	0.39	0.50	0.015	0.020
E	2.24	2.48	0.088	0.098
F	0.67	0.81	0.026	0.032
G	1.27 BSC		0.050 BSC	
H	—	0.50	—	0.020
K	0.89	1.14	0.035	0.045
L	0.64 BSC		0.025 BSC	
M	0°	10°	0°	10°
N	0.76	1.14	0.030	0.045
P	8.38	8.64	0.330	0.340
R	6.60	6.86	0.260	0.270
S	0.77	1.01	0.030	0.040

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. DIMENSION A & B DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
3. CONTROLLING DIMENSION: INCH.
4. DIM R TO BE DETERMINED AT DATUM -T-.

14

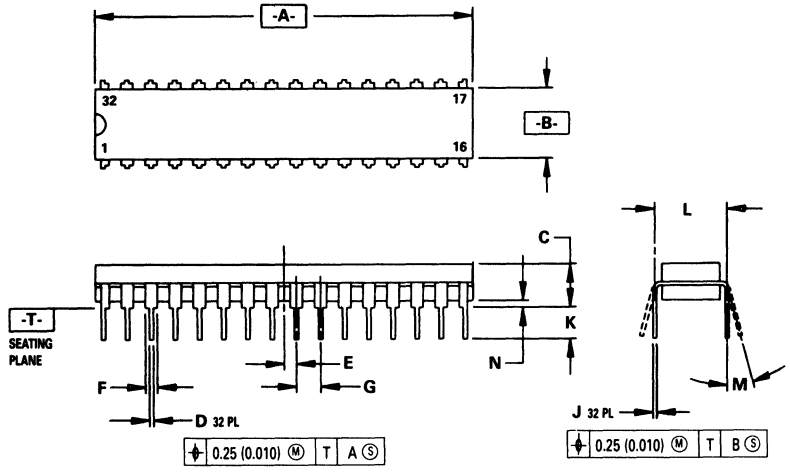
600 MIL PLASTIC
CASE 850-01



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	41.53	42.24	1.635	1.665
B	13.47	13.97	0.530	0.550
C	3.94	5.08	0.155	0.200
D	0.36	0.55	0.014	0.022
E	1.27 BSC		0.050 BSC	
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
J	0.21	0.38	0.008	0.015
K	2.93	3.42	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION A AND B DOES NOT INCLUDE MOLD FLASH. MAXIMUM MOLD FLASH 0.25 (0.010).

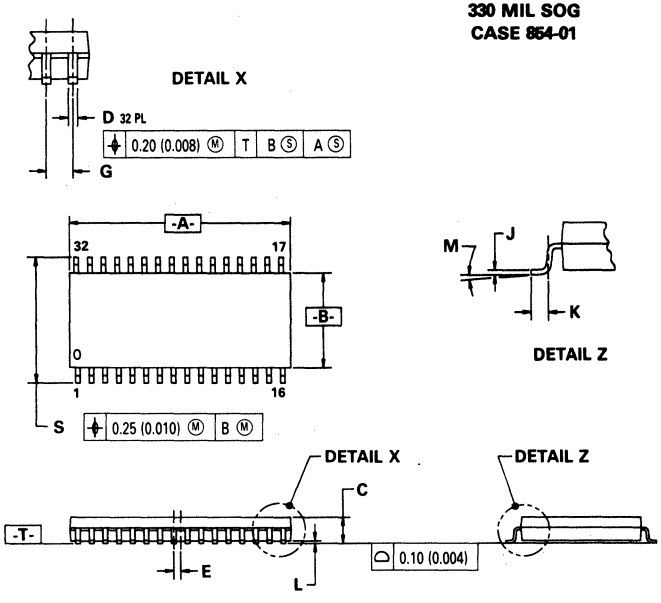
300 MIL PLASTIC
CASE 853-01



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	39.62	39.88	1.560	1.570
B	7.11	7.62	0.280	0.300
C	3.81	4.57	0.150	0.180
D	0.38	0.53	0.015	0.021
E	1.27 BSC		0.050 BSC	
F	1.14	1.40	0.045	0.055
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	3.43	0.125	0.135
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION A AND B DOES NOT INCLUDE MOLD FLASH. MAXIMUM MOLD FLASH 0.25 (0.010).

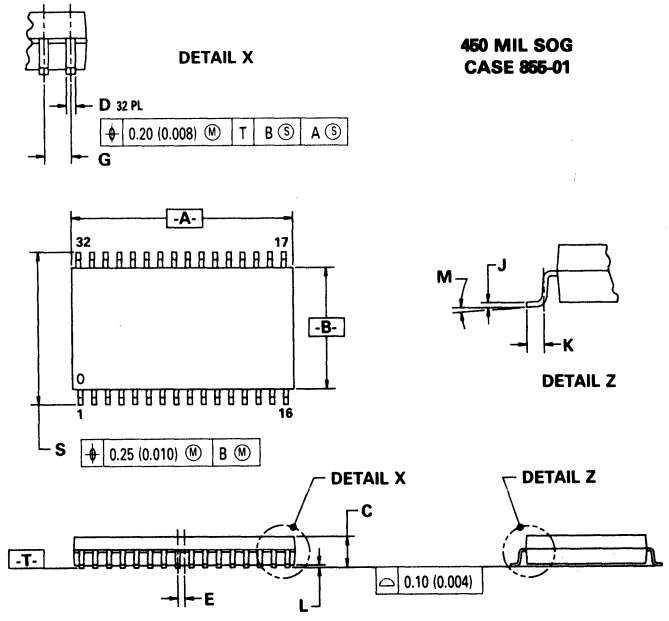
330 MIL SOG
CASE 854-01



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.40	20.70	0.803	0.815
B	8.70	8.90	0.342	0.350
C	2.30	2.60	0.090	0.102
D	0.36	0.51	0.014	0.020
E	0.64 BSC		0.025 BSC	
G	1.27 BSC		0.050 BSC	
J	0.15	0.32	0.006	0.012
K	0.61	1.00	0.024	0.039
L	0.10	0.30	0.004	0.012
M	0°	8°	0°	8°
S	11.91	12.52	0.469	0.493

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

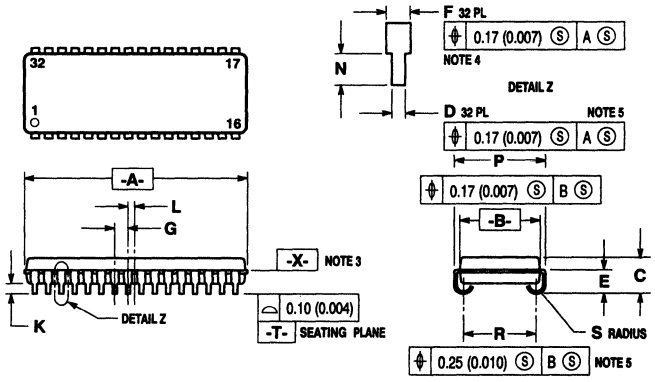
450 MIL SOG
CASE 855-01



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.40	20.70	0.803	0.815
B	11.10	11.30	0.437	0.445
C	2.75	3.04	0.108	0.120
D	0.35	0.50	0.014	0.020
E	0.64 BSC		0.025 BSC	
G	1.27 BSC		0.050 BSC	
J	0.14	0.32	0.006	0.012
K	0.60	1.00	0.024	0.039
L	0.10	0.35	0.004	0.014
M	0°	8°	0°	8°
S	13.80	14.40	0.543	0.567

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

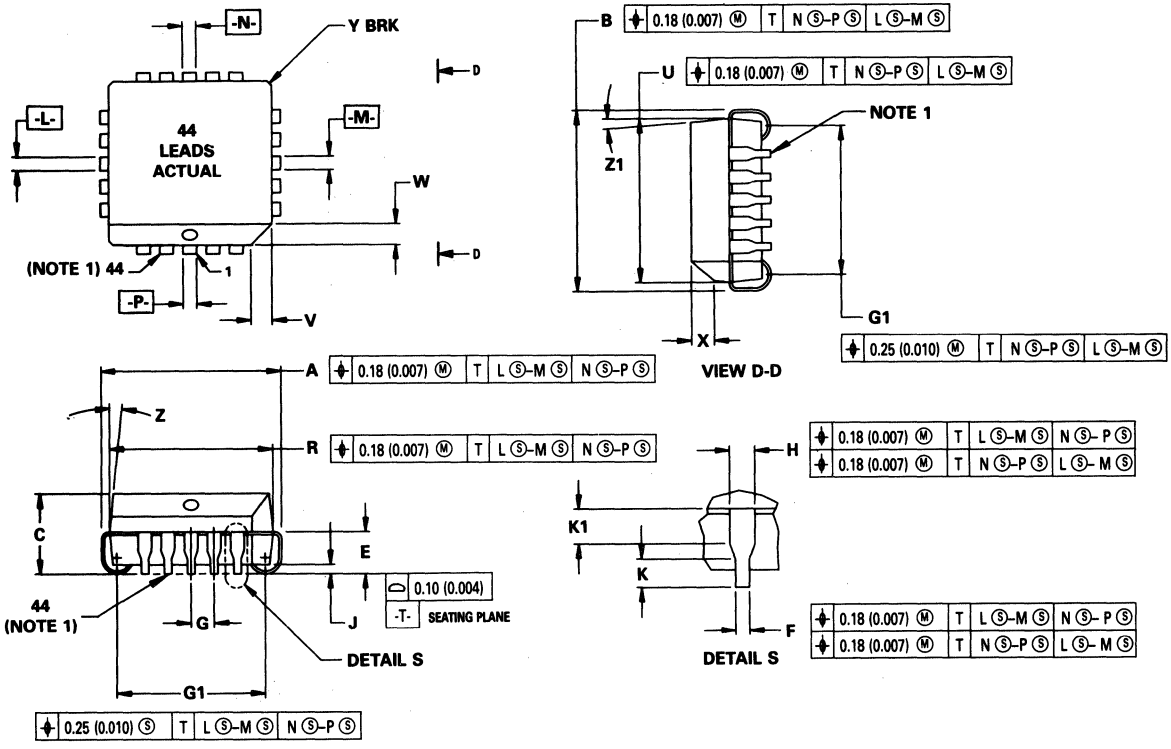
300 MIL SOJ
CASE 857-02



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.83	21.08	0.820	0.830
B	7.50	7.74	0.295	0.305
C	3.26	3.75	0.128	0.148
D	0.41	0.50	0.016	0.020
E	2.24	2.48	0.088	0.098
F	0.67	0.81	0.026	0.032
G	1.27 BSC		0.050 BSC	
K	0.89	1.14	0.035	0.045
L	0.64 BSC		0.025 BSC	
N	0.76	1.14	0.030	0.045
P	8.38	8.64	0.330	0.340
R	6.60	6.86	0.260	0.270
S	0.77	1.01	0.030	0.040

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DATUM PLANE -X- LOCATED AT TOP OF MOLD PARTING LINE AND COINCIDENT WITH TOP OF LEAD, WHERE LEAD EXITS BODY.
4. TO BE DETERMINED AT PLANE -X-.
5. TO BE DETERMINED AT PLANE -T-.
6. DIMENSION A & B DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.

PLASTIC CHIP CARRIER
CASE 777-02

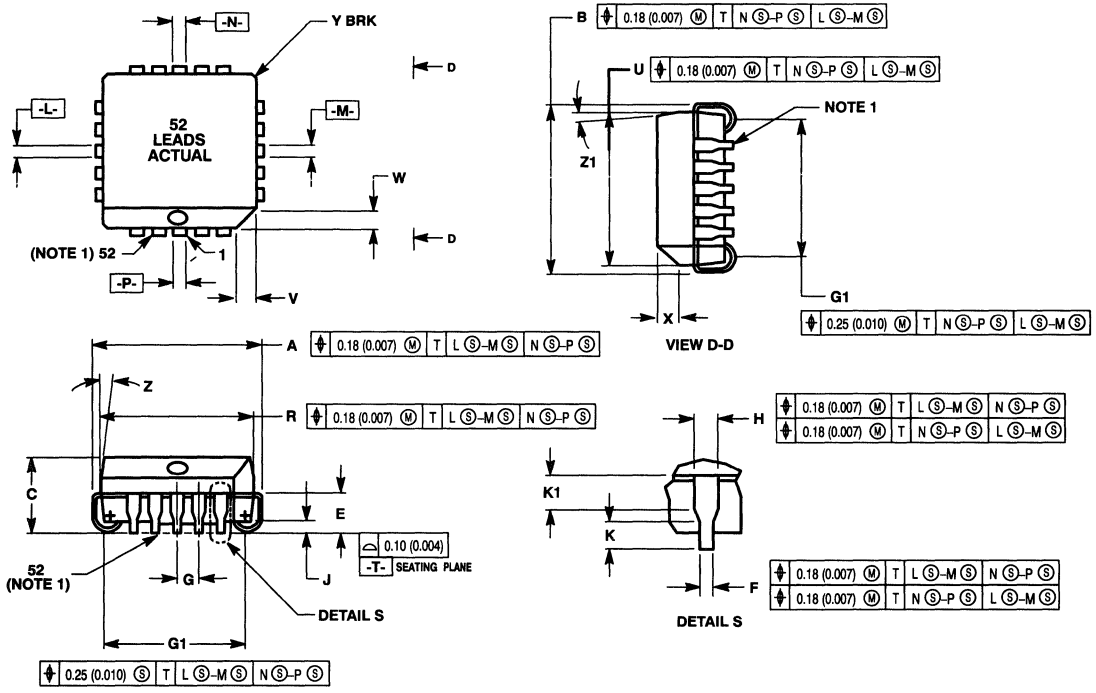


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	17.40	17.65	0.685	0.695
B	17.40	17.65	0.685	0.695
C	4.20	4.57	0.165	0.180
E	2.29	2.79	0.090	0.110
F	0.33	0.48	0.013	0.019
G	1.27 BSC		0.050 BSC	
H	0.66	0.81	0.026	0.032
J	0.51	—	0.020	—
K	0.64	—	0.025	—
R	16.51	16.66	0.650	0.656
U	16.51	16.66	0.650	0.656
V	1.07	1.21	0.042	0.048
W	1.07	1.21	0.042	0.048
X	1.07	1.42	0.042	0.056
Y	—	0.50	—	0.020
Z	2°	10°	2°	10°
G1	15.50	16.00	0.610	0.630
K1	1.02	—	0.040	—
Z1	2°	10°	2°	10°

NOTES:
1. **DUE TO SPACE LIMITATION, CASE 777-02 SHALL BE REPRESENTED BY A GENERAL (SMALLER) CASE OUTLINE DRAWING RATHER THAN SHOWING ALL 44 LEADS.**
2. DATUMS -L-, -M-, -N-, AND -P- DETERMINED WHERE TOP OF LEAD SHOULDER EXIT PLASTIC BODY AT MOLD PARTING LINE.
3. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
4. DIM R AND U DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 (0.010) PER SIDE.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
6. CONTROLLING DIMENSION: INCH.

14

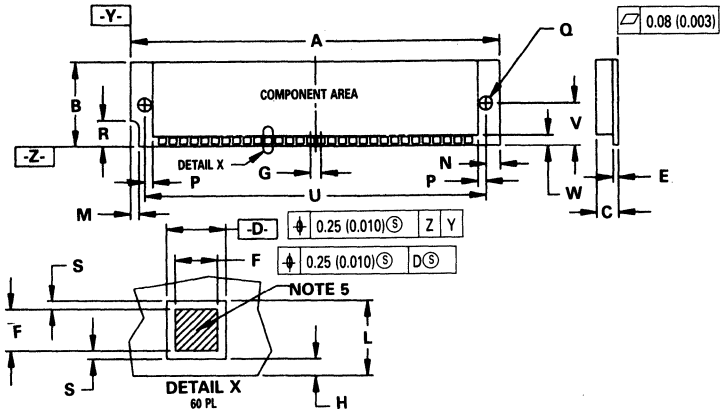
PLASTIC CHIP CARRIER
CASE 778-02



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.94	20.19	0.785	0.795
B	19.94	20.19	0.785	0.795
C	4.20	4.57	0.165	0.180
E	2.29	2.79	0.090	0.110
F	0.33	0.48	0.013	0.019
G	1.27 BSC		0.050 BSC	
H	0.66	0.81	0.026	0.032
J	0.51	—	0.020	—
K	0.64	—	0.025	—
R	19.05	19.20	0.750	0.756
U	19.05	19.20	0.750	0.756
V	1.07	1.21	0.042	0.048
W	1.07	1.21	0.042	0.048
X	1.07	1.42	0.042	0.056
Y	—	0.50	—	0.020
Z	2°	10°	2°	10°
G1	18.04	18.54	0.710	0.730
K1	1.02	—	0.040	—
Z1	2°	10°	2°	10°

NOTES:
1. **DUE TO SPACE LIMITATION, CASE 778-02 SHALL BE REPRESENTED BY A GENERAL (SMALLER) CASE OUTLINE DRAWING RATHER THAN SHOWING ALL 52 LEADS.**
2. DATUMS -L-, -M-, -N-, AND -P- DETERMINED WHERE TOP OF LEAD SHOULDER EXIT PLASTIC BODY AT MOLD PARTING LINE.
3. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
4. DIM R AND U DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 (0.010) PER SIDE.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
6. CONTROLLING DIMENSION: INCH.

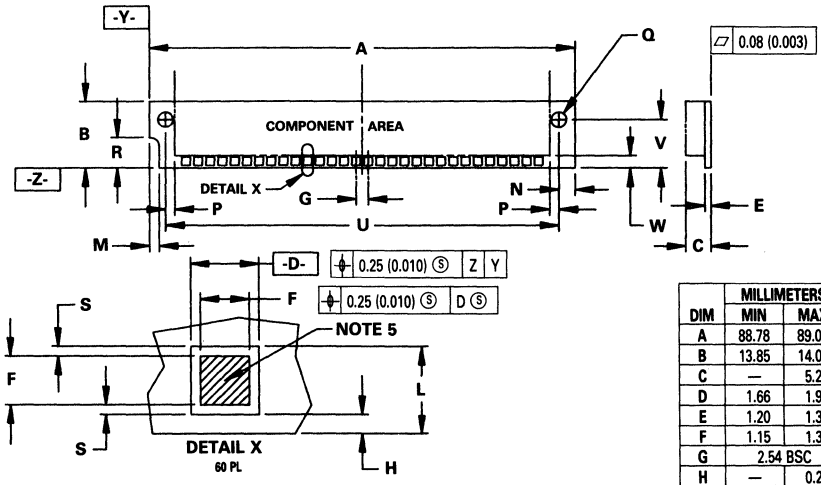
CASE 839-01



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	88.78	89.02	3.495	3.505
B	20.20	20.44	0.795	0.805
C	—	5.28	—	0.208
D	1.66	1.90	0.065	0.075
E	1.20	1.34	0.047	0.053
F	1.15	1.39	0.045	0.055
G	2.54 BSC		0.100 BSC	
H	—	0.25	—	0.010
L	2.04	—	0.080	—
M	1.91	2.15	0.075	0.085
N	3.26	3.50	0.128	0.138
P	1.15	—	0.045	—
Q	3.13	3.22	0.123	0.127
R	6.23	6.47	0.245	0.255
S	0.13	0.38	0.005	0.015
U	82.02	82.27	3.229	3.239
V	10.04	10.28	0.395	0.405
W	2.54	—	0.100	—

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. TABS TO BE ELECTRICALLY CONNECTED BOTH SIDES OF CARD.
4. DIMENSION E INCLUDES PLATING AND/OR METALIZATION.
5. CONTACT ZONE MUST BE FREE OF HOLES.

CASE 839A-01



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	88.78	89.02	3.495	3.505
B	13.85	14.09	0.545	0.555
C	—	5.28	—	0.208
D	1.66	1.90	0.065	0.075
E	1.20	1.34	0.047	0.053
F	1.15	1.39	0.045	0.055
G	2.54 BSC		0.100 BSC	
H	—	0.25	—	0.010
L	2.04	—	0.080	—
M	1.91	2.15	0.075	0.085
N	3.26	3.50	0.128	0.138
P	1.15	—	0.045	—
Q	3.13	3.22	0.123	0.127
R	6.23	6.47	0.245	0.255
S	0.13	0.38	0.005	0.015
U	82.02	82.27	3.229	3.239
V	10.04	10.28	0.395	0.405
W	2.54	—	0.100	—

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. TABS TO BE ELECTRICALLY CONNECTED BOTH SIDES OF CARD.
4. DIMENSION E INCLUDES PLATING AND/OR METALLIZATION.
5. CONTACT ZONE MUST BE FREE OF HOLES.

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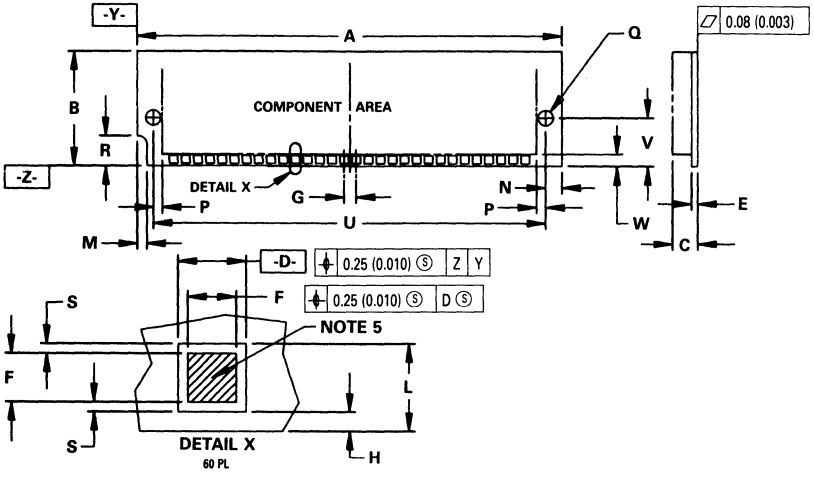
CASE 839B-01



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	88.78	89.02	3.495	3.505
B	23.88	24.13	0.940	0.950
C	—	5.28	—	0.208
D	1.66	1.90	0.065	0.075
E	1.20	1.34	0.047	0.053
F	1.15	1.39	0.045	0.055
G	2.54 BSC		0.100 BSC	
H	—	0.25	—	0.010
L	2.04	—	0.080	—
M	1.91	2.15	0.075	0.085
N	3.26	3.50	0.128	0.138
P	1.15	—	0.045	—
Q	3.13	3.22	0.123	0.127
R	6.23	6.47	0.245	0.255
S	0.13	0.38	0.005	0.015
U	82.02	82.27	3.229	3.239
V	10.04	10.28	0.395	0.405
W	2.54	—	0.100	—

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
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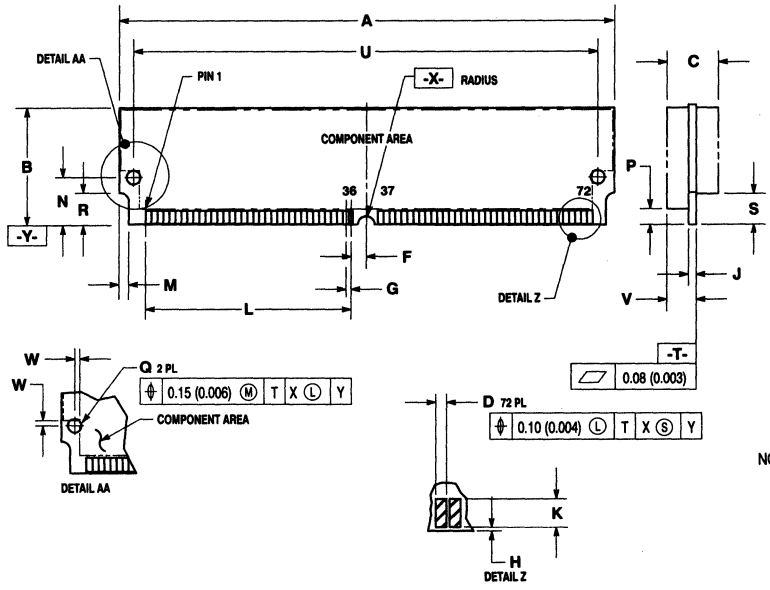
5. CONTACT ZONE MUST BE FREE OF HOLES.

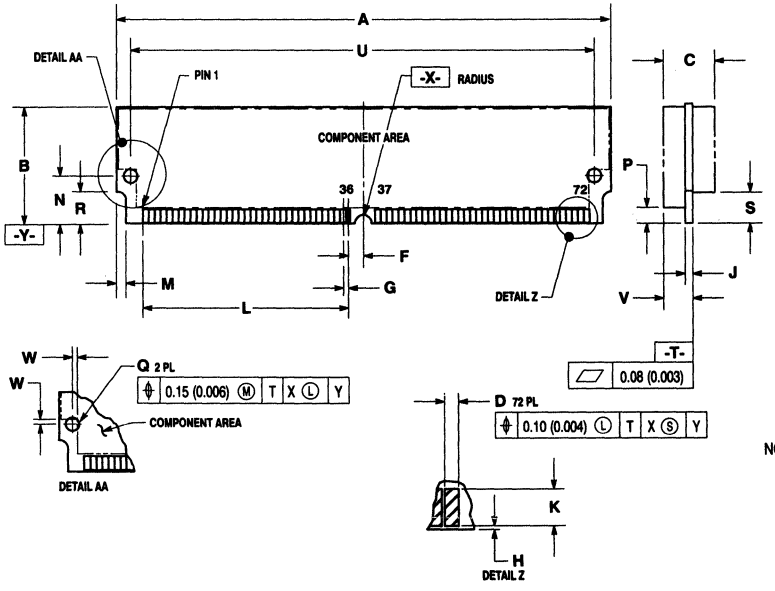
CASE 866-01



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	107.82	108.08	4.245	4.255
B	25.27	25.53	0.995	1.005
C	—	9.14	—	0.360
D	1.02	1.07	0.040	0.042
F	3.18 BSC		0.125 BSC	
G	1.27 BSC		0.050 BSC	
H	—	0.25	—	0.010
J	1.19	1.37	0.047	0.054
K	0.25	—	0.100	—
L	44.45 REF		1.750 REF	
M	1.90	2.16	0.075	0.085
N	10.16 BSC		0.400 BSC	
P	3.18	—	0.125	—
Q	3.12	3.22	0.123	0.127
R	6.22	6.48	0.245	0.255
S	5.72	—	0.225	—
U	101.19 BSC		3.984 BSC	
V	—	5.28	—	0.208
W	1.12	—	0.044	—
X	1.52	1.63	0.060	0.064

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CARD THICKNESS APPLIES ACROSS TABS AND INCLUDES PLATING AND/OR METALIZATION.

CASE 866A-01



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	107.82	108.08	4.245	4.255
B	30.48	33.02	1.200	1.300
C	—	9.14	—	0.360
D	1.02	1.07	0.040	0.042
F	3.18 BSC		0.125 BSC	
G	1.27 BSC		0.050 BSC	
H	—	0.25	—	0.010
J	1.19	1.37	0.047	0.054
K	0.25	—	0.100	—
L	44.45 REF		1.750 REF	
M	1.90	2.16	0.075	0.085
N	10.16 BSC		0.400 BSC	
P	3.18	—	0.125	—
Q	3.12	3.22	0.123	0.127
R	6.22	6.48	0.245	0.255
S	5.72	—	0.225	—
U	101.19 BSC		3.984 BSC	
V	—	5.28	—	0.208
W	1.12	—	0.044	—
X	1.52	1.63	0.060	0.064

NOTES:
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14

Embossed Tape and Reel

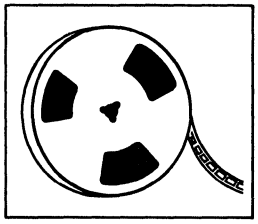
Tape and Reel Data for MOS Memory Surface Mount Devices

Embossed Tape and Reel is used to facilitate automatic pick and place equipment feed requirements. The tape is used as the shipping container for various products and requires a minimum of handling. The antistatic/conductive tape provides a secure cavity for the product when sealed with the "peel-back" cover tape.

- 13-Inch Reel
- Used For Automatic Pick and Place Feed Systems
- Minimizes Product Handling
- EIA-481
- SOJ-24, SOJ-28, SOJ-20/26

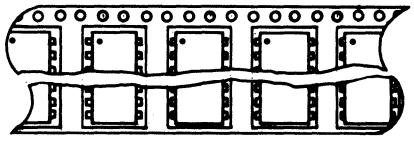
PACKAGES

SOJ-24
SOJ-28
SOJ-20/26



Ordering Information

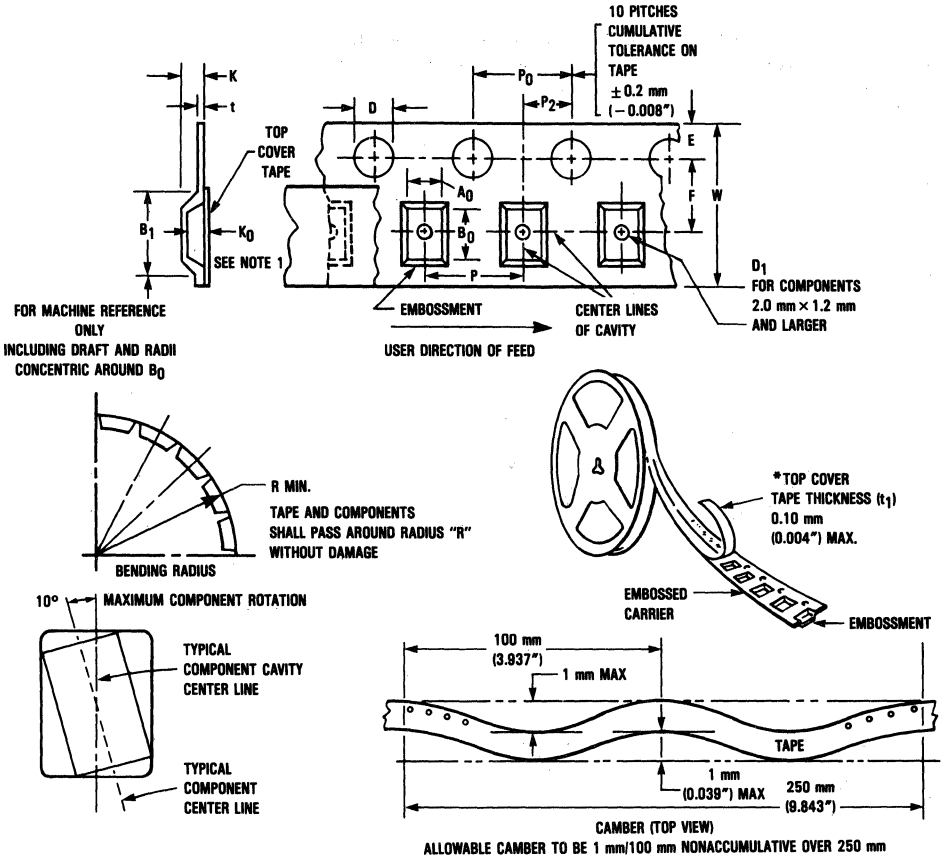
Use the standard device title and add the required suffix R2. Note that the individual reels have 1000 devices per reel. Also note the minimum lot size is one full reel for each line item, and orders are required to be in increments of the single reel quantity.



DIRECTION OF FEED

Package	Tape Width (mm)	Device per Reel	Reel Size (Inch)	Tape & Reel Lot Size (Min)	Device Suffix
SOJ-24	24	1,000	13	1,000	R2
SOJ-28	24	1,000	13	1,000	R2
SOJ-20/26	24	1,000	13	1,000	R2

CARRIER TAPE SPECIFICATIONS



DIMENSIONS

Tape Size	B_1 Max	D	D_1	E	F	K	P	P_0	P_2	R Min	T Max	W
24 mm	19.4 mm (0.764")	1.5+0.1 mm −0.0 (0.059+0.004" −0.0)	2.0 mm Min (0.079")	1.75±0.1 mm (0.069±0.004")	11.5±0.1 mm (0.453±0.004")	4.0 mm (0.157")	12.0±0.10 mm (0.472±0.004")	4.0±0.1 mm (0.157±0.004")	2.0±0.05 mm (0.079±0.002")	50 mm (1.968")	0.400 mm (0.016")	24±0.2 mm (0.945±0.008")

Metric Dimensions Govern—English are in parentheses for reference only.

NOTE 1: A_0, B_0, and K_0 are determined by component size. The clearance between the components and the cavity must be within 0.05 mm min to 0.50 mm max. The component cannot rotate more than 10° within the determined cavity.

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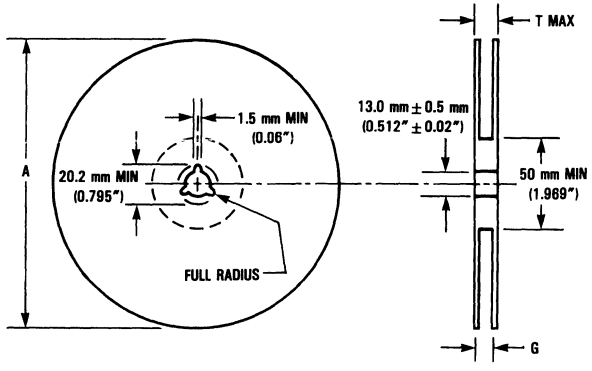
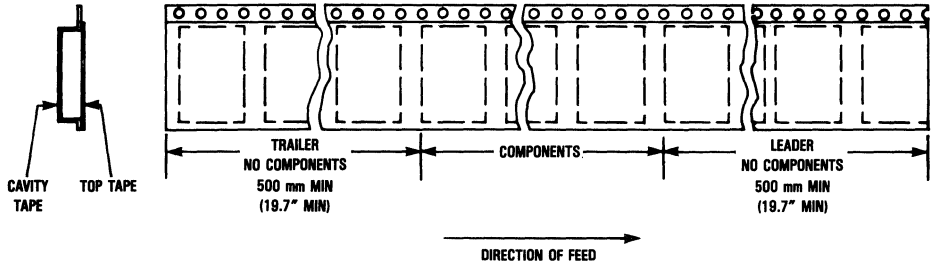
REEL DIMENSIONS

Metric Dimensions Govern—English are in Parentheses for Reference only.



Size	A Max	G	T MAX
24 mm	330 mm (12.992")	24.400 mm, +2.0 mm, −0.0 (0.961", +0.079", −0.00)	30.4 mm (1.197")

TAPE ENDS



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