LINEAR INTEGRATED CIRCUITS DATA BOOK

FIRST EDITION

MOTOROLA Semiconductor Products Inc.

LINEAR
INTEGRATED CIRCUITS
DATA BOOK

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This book presents technical data for a broad line of Linear Integrated Circuits. Complete specifications for the individual circuits are provided in data sheet form. In addition, the Linear Selector Guide is included to simplify the designers task of choosing the best circuit for a particular usage.

The information in this book has been carefully checked and is believed to be reliable; however, no responsibility is assumed for inaccuracies. Furthermore, this information does not convey to the purchaser of microelectronic devices any license under the patent rights of any manufacturer.

First Edition
December, 1971

MASTER INDEX of LINEAR INTEGRATED CIRCUITS DATA SHEET SPECIFICATIONS

DEVICE TYPE NUMBER	CIRCUIT FUNCTION
MC1303	Dual Stereo Preamplifier
MC1304	FM Multiplex Stereo Demodulator
MC1305	FM Multiplex Stereo Demodulator
MC1306	1/2-Watt Audio Amplifier
MC1307	FM Multiplex Stereo Demodulator
MC1326	Dual Doubly Balanced Chroma Demodulator with RGB Output Matrix
MC1328	Dual Doubly Balanced Chroma Demodulator
MC1330	Low-Level Video Detector
MC1335	FM Radio or Color TV Tuning Indicator
MC1345	TV Signal Processor
MC1350	IF Amplifier
MC1351	TV Sound Circuit
MC1352	TV Video IF Amplifier
MC1353	TV Video IF Amplifier
MC1355	Limiting FM IF Amplifier
MC1357	IF Amplifier and Quadrature Detector
MC1358	TV Sound IF Amplifier
MC1364	Automatic Frequency Control
MC1380	Class A Audio Driver
MC1398	TV Color Processing Circuit
MC1410*	Video Amplifier
MC1414	Dual Differential Comparator
MC1420*	Operational Amplifier
MC1430	Operational Amplifier
MC1431	Operational Amplifier
MC1433*	Operational Amplifier
MC1435*	Dual Operational Amplifier
MC1436*	Operational Amplifier
MC1436C*	Operational Amplifier
MC1437*	Operational Amplifier
MC1438*	Power Booster
MC1439*	Operational Amplifier
MC1440*	Core-Memory Sense Amplifier
MC1441*	Sense Amplifier
MC1444*	AC-Coupled 4-Channel Sense Amplifier
MC1445*	Wideband Amplifier
MC1446*	Plated-Wire Sense Amplifier
MC1454*	1-Watt Power Amplifier
MC1456*	Operational Amplifier
MC1456C*	Operational Amplifier

*MC1400 Series (or MCC1400 Series) device specifications appear on the MC1500 Series (or MCC1500 Series) data sheet.

DEVICE TYPE NUMBER	CIRCUIT FUNCTION
MC1458*	Operational Amplifier
MC1458C*	Operational Amplifier
MC1460*	Positive Voltage Regulator
MC1461*	Positive Voltage Regulator
MC1463*	Negative Voltage Regulator
MC1466*	Voltage and Current Regulator
MC1469*	Positive Voltage Regulator
MC1488	Quad MDTL Line Driver
MC1489	Quad MDTL Line Receivers
MC1489A	Quad MDTL Line Receivers
MC1494*	Four-Quadrant Multiplier
MC1495*	Four-Quadrant Multiplier
MC1496*	Balanced Modulator-Demodulator
MC1510	Video Amplifier
MC1514	Dual Differential Comparator
MC1520	Operational Amplifier
MC1530	Operational Amplifier
MC1531	Operational Amplifier
MC1533	Operational Amplifier
MC1535	Dual Operational Amplifier
MC1536	Operational Amplifier
MC1537	Operational Amplifier
MC1538	Power Booster
MC1539	Operational Amplifier
MC1540	Core-Memory Sense Amplifier
MC1541	Sense Amplifier
MC1543	Dual Sense Amplifier
MC1544	AC-Coupled 4-Channel Sense Amplifier
MC1545	Wideband Amplifier
MC1546	Plated-Wire Sense Amplifier
MC1550	RF-IF Amplifier
MC1552	Video Amplifier
MC1553	Video Amplifier
MC1554	1-Watt Power Amplifier
MC1556	Operational Amplifier
MC1588	Operational Amplifier
MC1560	Positive Voltage Regulator
MC1561	Positive Voltage Regulator
MC1563	Negative Voltage Regulator
MC1566	Voltage and Current Regulator
MC1569	Positive Voltage Regulator
MC1580	Dual Line Driver Receiver
MC1581	Dual MECL Line Receiver
MC1582	Dual MDTL, MTTL Line Driver
MC1583	Dual Saturated Logic Receiver

*MC1400 Series (or MCC1400 Series) device specifications appear on the MC1500 Series (or MCC1500 Series) data sheet.

MASTER INDEX (continued)

DEVICE TYPE NUMBER	CIRCUIT FUNCTION
MC1584	Dual MDTL, MTTL Receiver
MC1590	Wideband Amplifier with AGC
MC1594	Four-Quadrant Multiplier
MC1595	Four-Quadrant Multiplier
MC1596	Balanced Modulator-Demodulator
MC1709	Operational Amplifier
MC1709C	Operational Amplifier
MC1710	Differential Comparator
MC1710C	Differential Comparator
MC1711	Dual Differential Comparators
MC1711C	Dual Differential Comparators
MC1712	Wideband DC Amplifier
MC1712C	Wideband DC Amplifier
MC1723	Positive Voltage Regulator
MC1723C	Positive Voltage Regulator
MC1733	Differential Video Amplifier
MC1733C	Differential Video Amplifier
MC1741	Operational Amplifier
MC1741C	Operational Amplifier
MC1748	Operational Amplifier
MC1748C	Operational Amplifier
MC7520	Dual Sense Amplifiers
MC7521	Dual Sense Amplifiers
MC7522	Dual Sense Amplifiers
MC7523	Dual Sense Amplifiers
MC7524	Dual Sense Amplifiers
MC7525	Dual Sense Amplifiers
MCC1436*	Operational Amplifier (Chip)
MCC1439*	Operational Amplifier (Chip)
MCC1458*	Dual Operational Amplifier (Chip)
MCC1463*	Negative Voltage Regulator (Chip)
MCC1469*	Positive Voltage Regulator (Chip)
MCC1495*	Four-Quadrant Multiplier (Chip)
MCC1536	Operational Amplifier (Chip)
MCC1539	Operational Amplifier (Chip)
MCC1558	Dual Operational Amplifier (Chip)
MCC1563	Negative Voltage Regulator (Chip)
MCC1569	Positive Voltage Regulator (Chip)
MCC1595	Four-Quadrant Multiplier (Chip)
MCC1709	Operational Amplifier (Chip)
MCC1709C	Operational Amplifier (Chip)
MCC1710	Differential Comparator (Chip)
MCC1710C	Differential Comparator (Chip)
MCC1711	Dual Differential Comparator (Chip)

*MC1400 Series (or MCC1400 Series) device specifications appear on the MC1500 Series (or MCC1500 Series) data sheet.

MASTER INDEX (continued)

LINEAR

INTEGRATED CIRCUITS

INTERCHANGEABILITY GUIDE
and
CROSS REFERENCE LISTING

The following listing of Linear Integrated Circuit devices indicates the Motorola replacement available for Linear Integrated Circuits.

In some cases a Motorola suggested "similar to" device number is given. These parts have specification differences and therefore are not exact replacements. In many cases the "similar to" device offers improved performance.

Packaging availability information for each Motorola device is listed in the Linear Application Selector Guide and also appears on the individual data sheet for the device. Exact Outline Dimensions are shown in the Packaging Information section of this data book.

MANUFACTURERS REFERENCED

National Semiconductor
RCA
Texas Instruments
Fairchild Semiconductor

ABBREVIATION DEFINITIONS
for the
INTERCHANGEABILITY GUIDE
and
CROSS REFERENCE LISTING

A	Amplifier
CC	Communications Circuit
COML	Commercial
CP	Comparator
DA	Differential Amplifier
D-A	Digital-to-Analog
FMD	Frequency Modulator
IFA	Intermediate Frequency Amplifier
IFC	Interface Circuit
IND	Industrial
LD	Line Driver
LR	Line Receiver
MD	Memory Driver
MIL	Military
MUL	Multiplier
M/R	Modulator/Demodulator
OA	Operational Amplifier
PA	Power Amplifier
REG	Regulator
RF/IF	RF/IF Amplifier
SA	Sense Amplifier
SF	Special Function
SIM	Similar To
TBA	To Be Announced
TCA	Temperature Compensated Amplifier
TRI	Zero-Crossing Trigger
TV	TV Circuit
VA	Video Amplifier

NATIONAL TO MOTOROLA

Device Type No.	Function	Temperature Range	Pin-For-Pin Replacement	Motorola Device Type No.	Comments
LH101	OA	MIL	YES	MC1741	HYBRID; NO NULL
LH201	OA	COML	YES	MC1741	HYBRID; NO NULL
LM100	REG	MIL	NO	MC1723	POS REG; 15 mA
LM101	OA	MIL	YES	MC1748	–
LM101A	OA	MIL	YES	MLM101A	–
LM102	SF	MIL	YES	MLM110	VOLTAGE FOLLOWER; TBA
LM103	REG	MIL	–	–	DIODE REG
LM104	REG	MIL	YES	MLM104	NEG REG; 20 mA; TBA
LM105	REG	MIL	YES	MLM105	IMPROVED LM100; TBA
LM106	CP	MIL	SIM	MC1710	100 mA DRIVER; OPER COMP SUPPLIES
LM107	OA	MIL	YES	MLM107	NO OFFSET ADJUST; TBA
LM108	OA	MIL	–	–	NO NULL
LM108A	OA	MIL	–	–	NO NULL
LM109	REG	MIL	YES	MLM109	5-VOLT REG
LM110	SF	MIL	YES	MLM110	IMPROVED LML102; TBA
LM111	CP	MIL	–	–	HI-ZIN COMPARATOR
LM118	OA	MIL	–	–	50 V/μs
LM170	CC	MIL	NO	MC1590	AGC/SQUELCH AMPL
LM171	CC	MIL	NO	MFC6010	IF AMPL
LM172	CC	MIL	NO	MC1590	INCLUDES DETECTOR
LM200	REG	IND	NO	MC1723	POS REG; 15 mA
LM201	OA	COML	YES	MLM201A	TBA
LM201A	OA	COML	YES	MLM201A	–
LM202	SF	IND	YES	MLM210	VOLT FOLLOWER; TBA
LM204	REG	IND	YES	MLM204	NEG REG; 20 mA
LM205	REG	IND	YES	MLM205	IMPROVED LM100
LM206	CP	IND	SIM	MC1710	100-mA DRIVER
LM207	OA	IND	YES	MLM207	NO OFFSET ADJUST
LM208	OA	IND	–	–	–
LM208A	OA	IND	–	–	–
LM209	REG	IND	YES	MLM209	5-VOLT REG
LM210	SF	IND	YES	MLM210	IMPROVED LM202
LM211	CP	IND	–	–	HI-ZIN COMPARATOR
LM218	OA	IND	–	–	50 V/μs
LM270	CC	IND	NO	MC1590	AGC/SQUELCH (OR MC1350)
LM271	CC	IND	NO	MFC6010	IF AMPL
LM272	CC	IND	NO	MC1590	INCLUDES DETECTOR
LM300	REG	COML	NO	MC1723	POS REG; 15 mA
LM301A	OA	COML	YES	MLM301A	–
LM302	SF	COML	YES	MLM310	VOLTAGE FOLLOWER; TBA
LM304	REG	COML	YES	MC1563	NEG REG; 20 mA
LM305	REG	COML	YES	MC1723	IMPROVED LM100
LM306	CP	COML	SIM	MC1710C	100-mA DRIVER
LM307	OA	COML	YES	MLM307	NO OFFSET ADJUST
LM308	OA	COML	–	–	–
LM308A	OA	COML	–	–	–
LM309	REG	COML	YES	MLM309	5-VOLT REG
LM310	SF	COML	YES	MLM310	IMPROVED LM302; TBA
LM311	CP	COML	–	–	HI-ZIN COMPARATOR
LM318	OA	COML	–	–	50 V/μs
LM370	CC	COML	NO	MC1590	AGC/SQUELCH (OR MC1350)
LM371	CC	COML	NO	MFC6010	IF AMPL
LM372	CC	COML	NO	MC1590	INCLUDES DETECTOR (OR MC1350P)
LM703L	CC	COML	NO	MFC6010	–
LM709	OA	MIL	YES	MC1709	–
LM709A	OA	MIL	YES	MC1709	–
LM709C	OA	COML	YES	MC1709C	–
LM710	CP	MIL	YES	MC1710	–
LM710A	CP	MIL	YES	MC1710	–
LM710C	CP	COML	YES	MC1710C	–
LM711	CP	MIL	YES	MC1711	–
LM711C	CP	COML	YES	MC1711C	–
LM741	OA	MIL	YES	MC1741	–
LM741C	OA	COML	YES	MC1741C	–
LM748	OA	MIL	YES	MC1748	NONCOMP. MC1741
LM748C	OA	COML	YES	MC1748C	NONCOMP. MC1741C

RCA TO MOTOROLA

Device Type No.	Function	Temperature Range	Pin-For-Pin Replacement	Motorola Device Type No.	Comments
CA3000	DA	MIL	NO	MC1550	DC AMPL
CA3001	DA	MIL	NO	MC1550	DC IF VIDEO
CA3002	CC	MIL	NO	MC1550	IF AND VIDEO AMPL
CA3004	CC	MIL	NO	MC1550	RF/IF AMPL
CA3005	CC	MIL	NO	MC1550	RF/IF AMPL
CA3006	CC	MIL	NO	MC1550	RF/IF AMPL
CA3007	OA	MIL	NO	MC1550	AUDIO AMPL
CA3008	OA	MIL	NO	MC1712	OP AMPL
CA3010	OA	MIL	NO	MC1712	OP AMPL
CA3011	CC	MIL	NO	MC1590	OR MC1350 FM IF AMPL/HIGH
CA3012	CC	MIL	NO	MC1590	OR MC1350 FM IF AMPL/HIGH
CA3013	CC	MIL	NO	MC1355	OR MC1350 FM IF AMPL/HIGH
CA3014	CC	MIL	NO	MC1357	FM IF AMPL/LIM DET
CA3015	OA	MIL	NO	MC1712	OP AMPL
CA3016	OA	MIL	NO	MC1712	OP AMPL
CA3018	SF	MIL	–	–	TRANSISTOR ARRAY
CA3019	SF	MIL	–	–	DIODE ARRAY
CA3020	PA	MIL	NO	MC1554	AUDIO AMPL
CA3021	CC	MIL	NO	MC1590	IF AMPL OR MC1350
CA3022	CC	MIL	NO	MC1590	OR MC1350 VIDEO IF AMPL
CA3023	CC	MIL	NO	MC1590	OR MC1350 VIDEO IF AMPL
CA3026	SF	MIL	–	–	TRANSISTOR ARRAY
CA3028A	SF	MIL	NO	MC1550	DIFF/CASCODE AMPL
CA3028B	SF	MIL	NO	MC1550	TIGHT 3028A
CA3029	OA	COML	NO	MC1712C	SIM CA3008
CA3030	OA	COML	NO	MC1712C	SIM CA3015
CA3031	OA	MIL	YES	MC1712	SECOND SOURCE
CA3032	OA	COML	YES	MC1712	SECOND SOURCE
CA3033	OC	MIL	–	–	OP AMPL
CA3034	SF	MIL	–	–	(TV) DUAL PHASE DETECTOR
CA3035	SF	MIL	NO	MC1352	3 INDIV AMPLS OR MC1353
CA3036	SF	MIL	–	–	DUAL DARLINGTON
CA3037	OA	MIL	NO	MC1709	OP AMPL
CA3038	OA	MIL	NO	MC1709	OP AMPL
CA3039	SF	MIL	–	–	DIODE ARRAY
CA3040	CC	IND	NO	MC1510	VIDEO WIDE-BND AMPL
CA3041	SF	IND	NO	MC1351	FL IF AMPL LIM DET
CA3042	SF	IND	NO	MC1357	FM IF AMPL LIM DET
CA3043	SF	MIL	NO	MC1357	FM IF AMPL LIM DET
CA3044	SF	MIL	–	–	DUAL PHASE DETECTOR
CA3045	SF	MIL	–	–	TRANSISTOR ARRAY
CA3046	SF	IND	–	–	TRANSISTOR ARRAY
CA3047	OA	COML	NO	MC1533	OP AMPL
CA3048	SF	IND	–	–	4-IND AC AMPL
CA3049	SF	MIL	–	–	TRANSISTOR ARRAY
CA3050	DA	MIL	–	–	DUAL DIFF AMPL
CA3051	SF	IND	–	–	DUAL DIFF AMPL
CA3055	REG	MIL	NO	MC1723	1.8 V to 34 V, 100 mA
CA3059	TRI	IND	–	–	ZERO VOLTAGE SWITCH
CA3060	OA	MIL	–	–	3 IND OP TRANS AMPL
CA3062	SF	MIL	–	–	PHOTO DET AND POWER AMPL
CA3064	SF	COML	SIM	MC1350	AFC
CA3065	CC	COML	YES	MC1358	SECOND SOURCE
CA3075	CC	COML	SIM	MC1351	FM IF AMPL/LIM/DET
CA3076	CC	MIL	NO	MC1590	HI-GAIN IF AMPL
CA3085	REG	MIL	NO	MC1723	30 V, 12 mA
CA3085A	REG	MIL	NO	MC1723	40 V, 100 mA
CA3085B	REG	MIL	NO	MC1723	50 V, 100 mA
TA5625	SF	COML	–	–	–
TA5752	SF	COML	SIM	MC1326 OR MC1328	TV CHROMA DEMOD
TA5914	SF	COML	SIM	MC1352	TV VIDEO IF/AGC

TEXAS INSTRUMENTS TO MOTOROLA

Device Type No.	Function	Temperature Range	Pin-For-Pin Replacement	Motorola Device Type No.	Comments
SN52101A	OA	MIL	YES	MLM101A	–
SN52107	OA	MIL	YES	MLM107	TBA
SN52558	OA	MIL	YES	MC1558	–
SN52709	OA	MIL	YES	MC1709	–
SN52710	CP	MIL	YES	MC1710	–
SN52711	CP	MIL	YES	MC1711	–
SN52741	OA	MIL	YES	MC1741	–
SN52747	OA	MIL	YES	MC1747	TBA
SN52748	OA	MIL	YES	MC1748	–
SN52773	VA	MIL	YES	MC1733	–
SN52780	OA	MIL	–	–	–
SN55107	LR	MIL	YES	MC55107	LINE RECEIVER-TBA
SN55108	LR	MIL	YES	MC55108	LINE RECEIVER-TBA
SN55109	LD	MIL	YES	MC55109	LINE DRIVER-TBA
SN5510	DA	MIL	YES	MC1510	DIFF AMPL
SN55110	LD	MIL	NO	MC15110	LINE DRIVER-TBA
SN5511	DA	MIL	–	–	DIFF AMPL
SN5524	SA	MIL	YES	MC7524	SENSE AMPL
SN5525	SA	MIL	YES	MC7525	SENSE AMPL
SN56502	SF	MIL	–	–	LOG AMPLIFIER
SN56514	CC	MIL	SIM	MC1596	BALANCED MIXER
SN56702	CC	MIL	–	–	LOG AMPL
SN72301A	OA	IND	YES	MLM301A	–
SN72307	OA	IND	YES	MLM307	TBA
SN72558	OA	IND	YES	MC1458	SECOND SOURCE
SN72709	OA	IND	YES	MC1709C	–
SN72710	CP	IND	YES	MC1710C	–
SN72711	CP	IND	YES	MC1711C	–
SN72720N	CP	IND	YES	MC1414	DUAL MC1710
SN72741N	OA	IND	YES	MC1741C	–
SN72747	OA	IND	YES	MC1747C	TBA
SN72748	OA	IND	YES	MC1748C	–
SN72773	VA	IND	YES	MC1733C	–
SN75107	LR	IND	YES	MC75107	LINE RECEIVER-TBA
SN75108	LR	IND	YES	MC75108	LINE RECEIVER-TBA
SN75109	LD	IND	YES	MC75109	LINE DRIVER-TBA
SN7510	DA	IND	NO	MC1510	DIFF AMPL
SN75110	LD	IND	YES	MC75110	LINE DRIVER-TBA
SN7511	DA	IND	NO	MC1510	DIFF AMPL
SN7513	DA	IND	NO	MC1510	SECOND SOURCE
SN75150	LD	IND	NO	MC1488	LINE DRIVER
SN75154	LR	IND	NO	MC1489A	LINE RECEIVER
SN7520	SA	IND	YES	MC7520	SENSE AMPL
SN7521	SA	IND	YES	MC7521	SENSE AMPL
SN7522	SA	IND	YES	MC7522	SENSE AMPL
SN7523	SA	IND	YES	MC7523	SENSE AMPL
SN7524	SA	IND	YES	MC7524	SENSE AMPL
SN7525	SA	IND	YES	MC7525	SENSE AMPL
SN7526	SA	IND	–	–	SENSE AMPL
SN7527	SA	IND	–	–	SENSE AMPL
SN7528	SA	IND	YES	MC7528	SENSE AMPL-TBA
SN7529	SA	IND	YES	MC7529	SENSE AMPL-TBA
SN75303	MD	IND	–	–	MEMORY DRIVER
SN75308	SF	IND	–	–	TRANSISTOR ARRAY
SN75320	MD	IND	–	–	MEMORY DRIVER
SN75324	MD	IND	YES	MC75324	MEMORY DRIVER-TBA
SN75325	MD	IND	YES	MC75325	MEMORY DRIVER-TBA
SN75450	IFC	IND	YES	MC75450	INTERFACE CKT-TBA
SN75451	IFC	IND	YES	MC75451	INTERFACE CKT-TBA
SN7651	ICC	IND	NO	MC1496	BALANCED MIXER
SN76502	SF	IND	–	–	LOG AMPLIFIER
SN76600	CC	COML	YES	MC1350	SECOND SOURCE
SN76650	CC	COML	YES	MC1352P	SECOND SOURCE
SN76702	CC	IND	–	–	LOG AMPL

FAIRCHILD TO MOTOROLA

Device Type No.	Function	Temperature Range	Pin-For-Pin Replacement	Motorola Device Type No.	Comments
µA702	OA	MIL	YES	MC1712	SECOND SOURCE
µA702C	OA	COML	YES	MC1712C	SECOND SOURCE
µA703	RF/IF	MIL	NO	MFC6010	150 MHz
µA703C	RF/IF	COML	NO	MFC6010	150 MHz
µA703E	RF/IF	COML	NO	MFC6010	150 MHz
µA708	A	COML	—	—	HEARING AID AMPL
µA709A	OA	MIL	—	—	HI-PERFORMANCE µA709
µA709	OA	MIL	YES	MC1709	SECOND SOURCE
—	OA	MIL	YES	MC1709L	SECOND SOURCE
µA709C	OA	COML	YES	MC1709C	SECOND SOURCE
µA710	CP	MIL	YES	MC1710	SECOND SOURCE
µA710C	CP	COML	YES	MC1710C	SECOND SOURCE
µA711	CP	MIL	YES	MC1711	SECOND SOURCE (DUAL)
µA711C	CP	COML	YES	MC1711C	SECOND SOURCE (DUAL)
µA715	OA	MIL	—	—	f_c=65 MHz typ
µA715C	OA	COML	—	—	f_c=65 MHz typ
µA716	A	MIL	—	—	TELEPHONE AMPL
µA716C	A	COML	—	—	TELEPHONE AMPL
µA717E	A	COML	NO	MC1351	TV SOUND AMPL
µA719	RF/IF	MIL	NO	MC1357	RF AMPL QUAD FM DET
µA719C	RF/IF	COML	NO	MC1357	RF AMPL QUAD FM DET
µA722	DA	COML	—	—	10-BIT CURRENT SOURCE
µA722B	DA	COML	—	—	10-BIT CURRENT SOURCE
µA723	REG	MIL	YES	MC1723	SECOND SOURCE
µA723C	REG	COML	YES	MC1723C	SECOND SOURCE
µA725	OA	MIL	—	—	INSTRUMENTATION
µA725B	OA	COML	—	—	INSTRUMENTATION
µA725C	OA	COML	—	—	INSTRUMENTATION
µA726	TCA	MIL	—	—	TEMP COMP DIFF PAIR
µA726C	TCA	COML	—	—	TEMP COMP DIFF PAIR
µA727	TCA	MIL	—	—	—
µA727B	TCA	COML	—	—	—
µA729	FMD	COML	YES	MC1305	SECOND SOURCE, FM DECODER
µA730	OA	MIL	—	—	DIFFERENTIAL AMPL
µA730C	OA	COML	—	—	DIFFERENTIAL AMPL
µA731	SA	MIL	—	—	DUAL SENSE AMPL
µA731C	SA	COML	—	—	DUAL SENSE AMPL
µA732	FMD	COML	YES	MC1304	SECOND SOURCE
µA733	VA	MIL	YES	MC1733	SECOND SOURCE
µA733C	VA	COML	YES	MC1733C	SECOND SOURCE
µA735	OA	MIL	—	—	µ-POWER
µA735B,C	OA	COML	—	—	µ-POWER
µA737E	TV	COML	YES	MC1328	CHROMA DEMOD
µA739	OA	MIL	—	—	DUAL, LOW-NOISE
µA739C	OA	COML	YES	MC1303	DUAL, LOW-NOISE
µA740	OA	MIL	—	—	FET INPUT
µA740C	OA	COML	—	—	FET INPUT
µA741	OA	MIL	YES	MC1741	SECOND SOURCE
µA741C	OA	COML	YES	MC1741C	SECOND SOURCE
µA742	TRI	MIL	—	—	ZERO-CROSSING TRIGGER
µA742C	TRI	COML	—	—	ZERO-CROSSING TRIGGER
µA744	OA	MIL	—	—	RADIATION RESISTANT
µA745	OA	COML	—	—	DUAL AC AMPL
µA746E	TV	COML	NO	MC1328	CHROMA DEMOD
µA747	OA	MIL	NO	MC1558	DUAL MC1741
µA747C	OA	COML	NO	MC1458	DUAL MC1741C
µA748	OA	MIL	YES	MC1748	SECOND SOURCE
µA748C	OA	COML	YES	MC1748C	SECOND SOURCE
µA749	OA	MIL	—	—	DUAL MC1748

FAIRCHILD TO MOTOROLA (Continued)

Device Type No.	Function	Temperature Range	Pin-For-Pin Replacement	Motorola Device Type No.	Comments
μA749C	OA	COML	—	—	DUAL MC1748C
μA749D	OA	COML	—	—	DUAL AUDIO AMPL
μA751C	VA	COML	—	—	SIMILAR TO μA733
μA754C	TV	COML	NO	MC1355	TV/FM SOUND SYSTEM
μA757C	IFA	COML	NO	MC1350	IF AMPL WITH AGC
μA757C	IFA	COML	NO	MC1590	IF AMPL
μA761C-1	SA	COML	—	—	2-CHANNEL CORE-MEMORY SA
μA761C-2	SA	COML	—	—	SIMILAR TO SN7524/25
μA761C-3	SA	COML	—	—	16-PIN
μA777	OA	MIL	—	—	PRECISION OA
μA777B	OA	COML	—	—	PRECISION OA
μA777C	OA	COML	—	—	PRECISION OA
μA780	—	—	—	—	—
μA781	—	—	—	—	—
μA795	MUL	MIL	YES	MC1595	SECOND SOURCE
μA795C	MUL	COML	YES	MC1495	SECOND SOURCE
μA796	M/D	MIL	YES	MC1596	SECOND SOURCE
μA796C	M/D	COML	YES	MC1496	SECOND SOURCE
μA7624	SA	COML	NO	MC1541	2 CHAN SENSE AMPL (SIMILAR TO μA761)
μA7625	SA	—	NO	MC1541	2-CHANNEL SA (SIMILAR TO μA761)
μA9614	LD	MIL	NO	MC1582	DUAL DIFF LINE DRIVER
μA9614C	LD	COML	NO	MC1582	DUAL DIFF LINE DRIVER
μA9615	LR	MIL	NO	MC1584	DUAL DIFF LINE RECEIVER
μA9615C	LR	COML	NO	MC1584	DUAL DIFF LINE RECEIVER
μA9620	LR	MIL	NO	MC1580	—
μA9620C	LR	COML	NO	MC1580	—
μA9621	LD	MIL	NO	MC1584	DUAL DIFF LINE DRIVER
μA9621C	LD	COML	NO	MC1584	—
μA9622	LR	MIL	NO	MC1583	DUAL LINE RECEIVER

2

2

CASE DIMENSIONS

Dimensions are in inches.

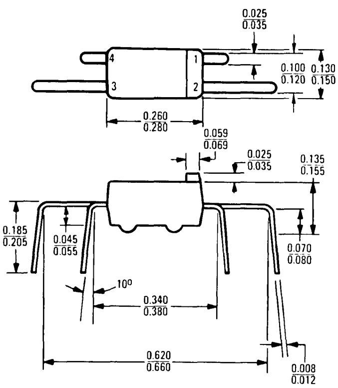
PACKAGING INFORMATION

The packaging availability for each device type is indicated on the individual data sheets and the Linear Selector Guide. All of the outline dimensions for the packages are given in this section. Outline dimensions for non-encapsulated standard linear device chips and beam-lead devices are found on the individual data sheets (see MCC or MCBC prefix followed by type number).

3

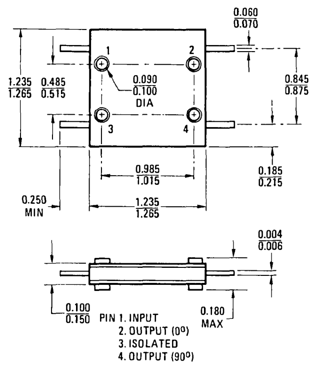
CASE 206A

Plastic Package
Weight ≈ 0.2 gram



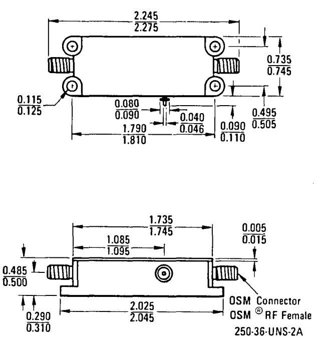
CASE 230

Metal Package
Weight ≈ 7.7 grams



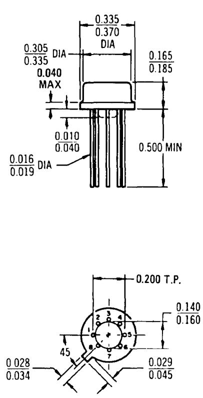
CASE 231

Metal Package
Weight ≈ 28.349 grams



CASE 601 TO-99

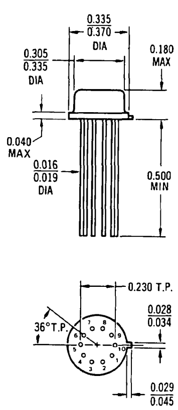
G Suffix Weight ≈ 0.92 gram
Metal Package



All JEDEC dimensions and notes apply
Case connected to pin 4 through substrate

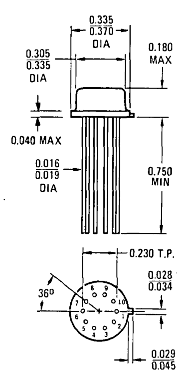
CASE 602A

G Suffix Weight ≈ 0.918 gram
Metal Package



CASE 602B

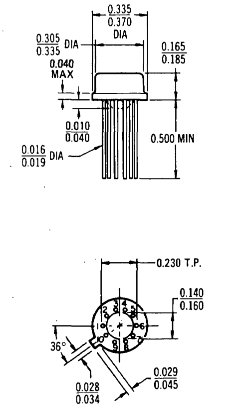
G Suffix Weight ≈ 0.918 gram
Metal Package



CASE 603-02 TO-100

G Suffix Weight ≈ 0.918 gram

Metal Package

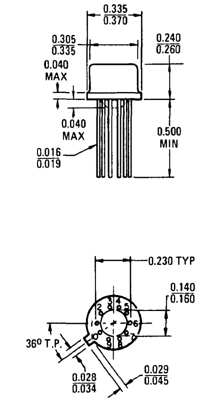


All JEDEC dimensions and notes apply

CASE 603-03

G Suffix Weight ≈ 0.918 gram

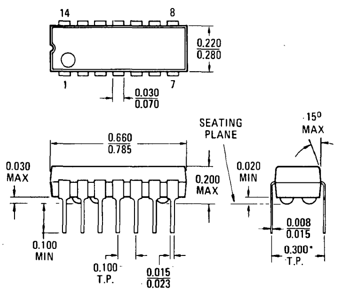
Metal Package



CASE 605 TO-116

P Suffix Weight ≈ 0.911 gram

Plastic Package



Four insulating stand-offs are provided

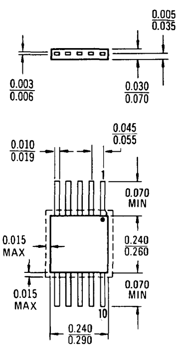
All JEDEC dimensions and notes apply

*Dimension is to lead centerline when formed parallel.

CASE 606 TO-91

F Suffix Weight ≈ 0.127 gram

Ceramic Package

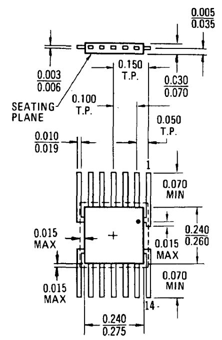


All JEDEC dimensions and notes apply

CASE 607 TO-86

F Suffix Weight ≈ 0.218 gram

Ceramic Package



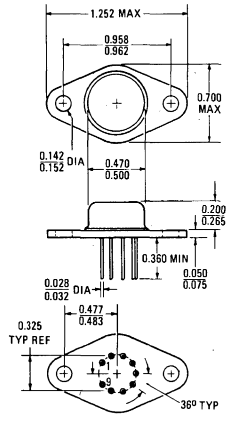
Lead 1 identified by color dot or by elbow on lead.

All JEDEC dimensions and notes apply

CASE 614

R Suffix Weight ≈ 6.315 grams

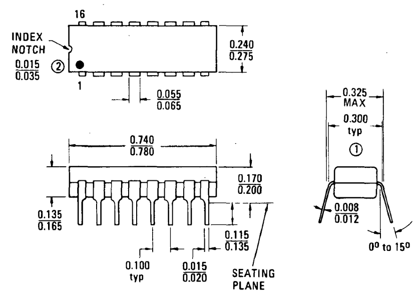
Metal Package



CASE 620

L Suffix Weight ≈ 1.97 grams

Ceramic Package



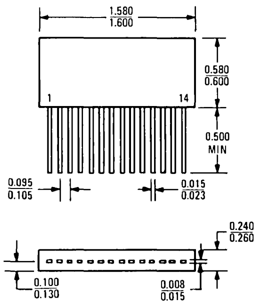
① This dimension is measured from the lead centers at the seating plane with leads vertical.

② Lead 1 identified by color dot, notch in lead, or notch in ceramic.

CASE 625

P Suffix Weight ≈ 7.0 grams

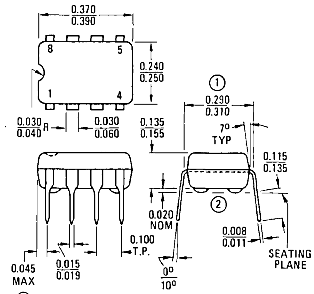
Plastic Package



CASE 626

P Suffix Weight ≈ 0.446 gram

Plastic Package



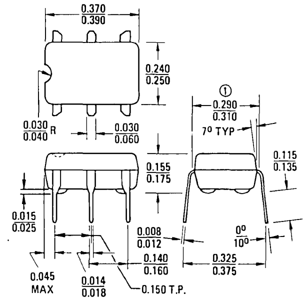
① Measure to center line of leads when parallel.

② Four insulating stand-offs are provided.

CASE 627

P Suffix Weight ≈ 0.40 gram

Plastic Package



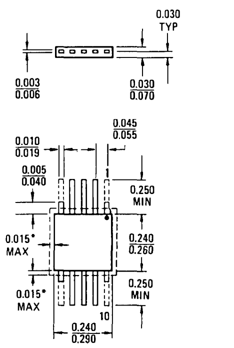
Weight ≈ 0.40 gram

① Measure to center line of leads when parallel.

CASE 628

F Suffix Weight ≈ 0.127 gram

Ceramic Package

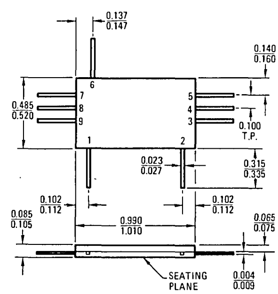


Lead 1 identified by color dot or by shoulder on lead.
Leads 1, 5, 6, 10 are clipped.
*Tolerance for lid skewing, glass meniscus, and glass overrun.

CASE 631

Plastic Package

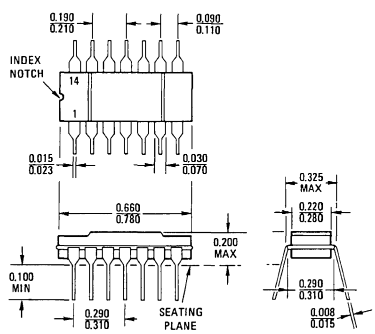
Weight ≈ 1.003 grams



CASE 632 — TO-116

L Suffix Weight ≈ 1.954 grams

Ceramic Package



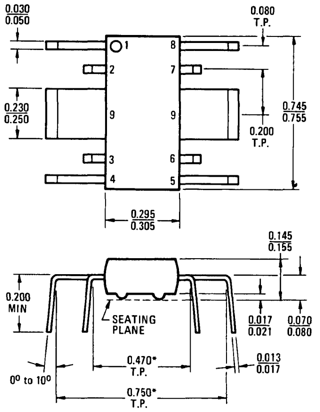
All JEDEC TO-116 dimensions and notes apply.

3

CASE 641

Plastic Package

Weight ≈ 1.85 grams

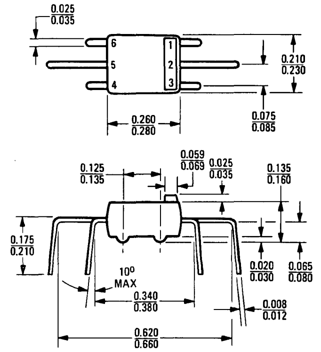


*Dimension is to lead centerline when formed parallel.

CASE 643A

Plastic Package

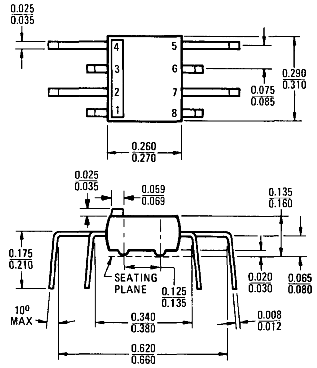
Weight ≈ 0.31 gram



CASE 644A

Plastic Package

Weight ≈ 0.45 gram

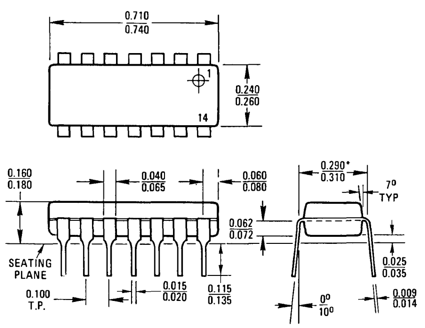


CASE 646

P Suffix

Plastic Package

Weight ≈ 0.911 gram



*Dimension is to lead centerline when formed parallel.

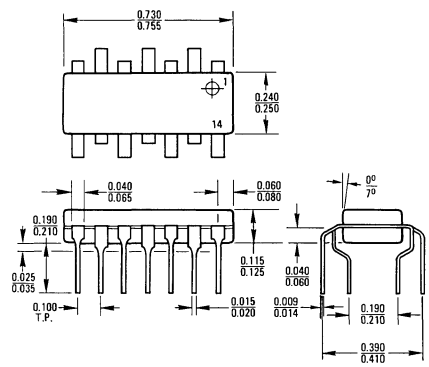
All JEDEC dimensions and notes apply.

CASE 647

PQ Suffix

Plastic Package

Weight ≈ 0.911 gram

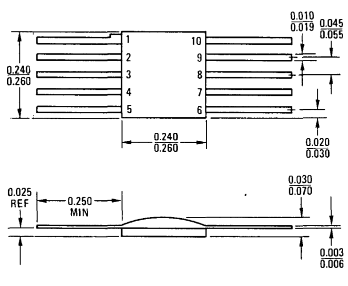


CASE 665

F Suffix

Ceramic Package

Weight ≈ 0.188 gram

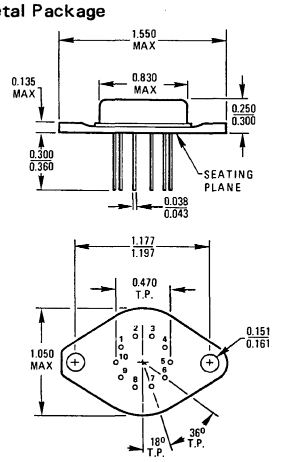


CASE 685

R Suffix

Metal Package

Weight ≈ 8.0 grams

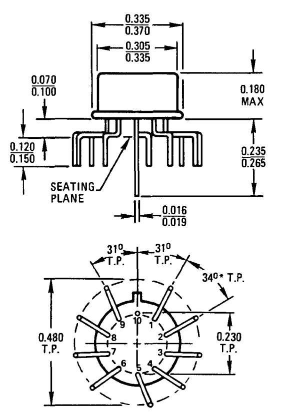


CASE 686

G Suffix

Metal Package

Weight ≈ 0.918 gram



*Seven places; (between all leads except 5 & 6, 9 & 10, 10 & 1)

GENERAL INFORMATION

STANDARD FEATURES for LINEAR INTEGRATED CIRCUIT CHIPS

(See MCC prefix data sheets for device specifications.)

All linear integrated circuit chips . . . .

- are 100% electrically tested to sufficient parameter limits (min/max) to permit distinct identification as either premium or industrial versions
- employ phosphorsilicate passivation which protects the entire active surface area including metalization interconnects during shipping and handling
- are 100% visually inspected to the criteria of MIL-STD-883, Method 2010.1, Condition B
- incorporate a minimum of 4000 Å gold backing to insure positive adherence bonding.

FEATURES for BEAM LEAD CHIPS

(See MCBC prefix data sheet for device specifications.)

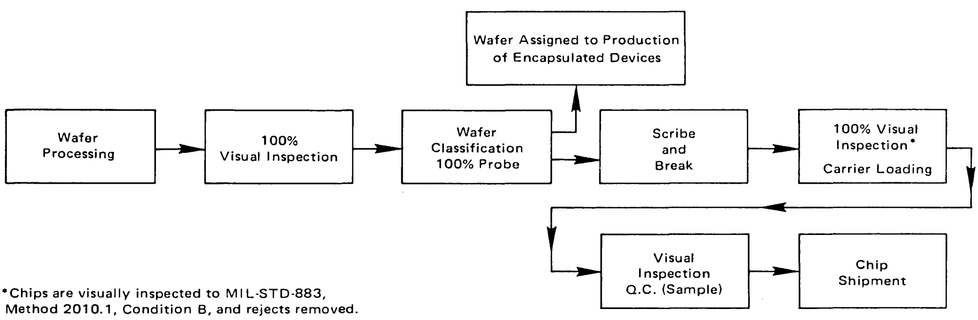
Beam lead linear integrated circuit chips . . . .

- are processed to the same criteria as the previously published beam-lead integrated circuits to insure the same reliability and performance features.

STANDARD CHIP PROCESSING

The industry-standard linear integrated circuits offered in Motorola's Microcircuit Components line are subjected to the same in-process controls as Motorola's standard encapsulated devices. The chip processing and quality control requirements are designed to insure reliability and performance of the finished product.

The processing and quality control flow chart shows that all wafer processing is completed prior to wafer assignment for subsequent encapsulation or special testing required for unencapsulated devices.



*Chips are visually inspected to MIL-STD-883, Method 2010.1, Condition B, and rejects removed.

GENERAL INFORMATION

NON-STANDARD CHIP PROCESSING

The industry standard unencapsulated integrated circuits are selected to meet a wide variety of application requirements. Nevertheless, there may be occasions when a designer can benefit from a non-standard device for a specific circuit requirement. To satisfy these requirements, almost any device from Motorola's extensive line of linear integrated circuits may be obtained on a specially negotiated basis. Although the electrical specifications of these chips are limited by certain test limitations, the customer may negotiate additional tests. Moreover, various chip technologies such as solder-bump and chrome-silver backing are available on a specially negotiated basis.

HANDLING PRECAUTIONS

Metalization interconnect passivation on all chips provides protection in shipping and handling. However, care should be exercised to prevent damaging the bonding pads. A vacuum pickup is useful for this purpose, tweezers are not recommended.

There are four basic requirements for handling devices in the customer's establishment:

1. Store devices in a covered or sealed container.
2. Store devices in an environment of no more than 30% relative humidity.
3. Process devices in a non-inert atmosphere not exceeding 100°, or in an inert atmosphere not exceeding 400°C.
4. Processing equipment should conform to the minimum standards of equipment normally employed by semiconductor manufacturers.

Motorola's engineering staff is available for consultation in the event of correlation or processing problems encountered in the use of Motorola semiconductor chips. For assistance of this nature, please contact your nearest Motorola sales representative.

STANDARD CARRIER PACKAGES

The non-spill type shipping carrier consists of a compartmentalized tray and fitted transparent cover. Each chip is placed in its compartment, geometry side up, so that incoming visual inspection may be performed prior to breaking the carrier seal. The shipping carrier is designed to:

- provide maximum device protection
- permit the customer to remove only a portion of the devices – the carrier can be resealed
- provide a storage container for the unused devices.

Additional package techniques are under development to facilitate handling, visual inspection and chip storage.

Various packaging and shipping options are available on a negotiated basis. For more information on these options, please contact your Motorola sales representative.

RECOMMENDED INCOMING INSPECTION

Motorola certifies that the devices have been subjected to the visual criteria of MIL-STD-883, Method 2010.1, Condition B.

Should the lot fail the customer's incoming visual inspection, the entire lot, with the package seals intact, shall be returned to Motorola. Incoming visual inspection should be performed prior to breaking the package seals. In no case will Motorola accept a partial return of devices.

APPLICATION SELECTOR GUIDE

LINEAR integrated circuits offer the design engineer a variety of functions for analog applications. This line includes devices for military, industrial, and consumer applications. Devices are available in a broad selection of operating characteristics and packaging. Refer to the last page of the Linear Selector Guide for package information.

At a Glance – MILITARY and INDUSTRIAL DEVICES

OPERATIONAL AMPLIFIERS

TYPE			SPECIFICATIONS TYPICAL AT T_A = +25°C						
-55 to +125°C	0 to +75°C	Case	A_{vol}, V/V	V_O, V_{pk}	I_{IB}, µA	$\lvert V_{IO} \rvert$ mV	SR,V/µs	f_C, MHz	Comments
MC1520	MC1420	602A	1,500	±4.0	0.8	5.0	5.0	10	z_o = 50 ohms, Diff. Output
MC1530	MC1430	602B,605,606	5,000	±5.2	3.0	1.0	1.0	6.0	z_o = 25 ohms
MC1531	MC1431	602B,605,606	3,500	±5.2	0.025	3.0	1.0	6.0	z_o = 25 ohms
MC1533	MC1433	602B,605,606,632	60,000	±13	0.5	1.0	2.0	0.2	V_{IO} Adjustable
MC1535	MC1435	602B,605,607,632	7,000	±2.8	1.2	1.0	0.67	2.0	Dual Op-Ampl.
MC1536*	MC1436*,C	601	500,000	±23	0.008	2.0	2.0	1.0	Internally Compensated ±28-Volt Supply
MC1537	MC1437	605,632	45,000	±14	0.2	1.0	0.25	1.0	Dual MC1709
MC1539*	MC1439*	601,632,605	120,000	±13	0.2	1.0	4.2	2.0	dV_{out}/dt = 34 @A_v = 100
MC1556	MC1456,C	601	200,000	±13	0.008	2.0	2.5	1.0	Internally Compensated
MC1558*	MC1458*,C	605,601,626,632	200,000	±14	0.2	1.0	0.8	1.0	Dual MC1741,C
MC1709*	MC1709C*	601,605,606,626,632	45,000	±14	0.2	1.0	0.25	1.0	
MCB1709F†	–	665	45,000	±14	0.2	1.0	0.25	1.0	Beam-Lead MC1709
MC1712	MC1712C	601,606,632	3,600	±5.3	2.5	1.1	1.5	5.0	
MC1741*	MC1741C*	601,605,606,626,632	200,000	±14	0.2	1.0	0.8	1.0	Internally Compensated
MCB1741F†	–	665	200,000	±14	0.2	1.0	0.8	1.0	Beam-Lead MC1741
MC1748*	MC1748C*	601	200,000	±14	0.08	1.0	0.8	1.0	Noncompensated MC1741,C
MCH2870M	MCH2870C	614	200,000	±13	0.2	1.0	0.8	1.1	Load current ±300 mA Internally Compensated
MLM101A	MLM301A	601	160,000	±14	0.03	0.7	1.0	11	

Definitions: A_{vol} Open-Loop Voltage Gain; V_O Output Voltage Swing; I_{IB} Input Bias Current; V_{IO} Input Offset Voltage; SR Slew Rate @ Unity Gain; f_C Unity Gain Crossover Frequency

*Also available as a non-encapsulated chip, use MCC prefix. †Also available as a non-encapsulated beam-lead-device, use MCBC prefix.

LINEAR/DIGITAL INTERFACE CIRCUITS

TYPE – Temperature Range				Typ–Input Threshold	Voltage Gain–Typ	Response Time–Typ	Comments
-55 to +125°C	Case	0 to +75°C	Case	(V_{th}, mVdc)	(A_v, V/V)	(t_R, ns)	
MC1514	632	MC1414	632	21.5/18.5 ①	1700†	40	A dual differential comparator for level detection, low-level sensing, and memory applications
MC1540	602B,606, 632	MC1440	602B,606, 632	17	85	20	Designed to detect bipolar differential signals derived by a core memory with cycle times as short as 0.5 µs
MC1541	607,632	MC1441	607,632	17	75	30/15 ②	A dual-channel gated sense amplifier with separate wide-band differential input amplifiers
MC1543	632	–	–	20	–	10/3.0 ②	A MECL dual core-memory sense amplifier; adjustable threshold with excellent threshold stability
MC1544	620	MC1444	620	1.0	–	65/50 ②	AC-coupled 4-channel sense amplifier – ideal for plated-wire, thin-film, and other hi-speed low-level sensing applications.
MC1546	620	MC1446	620	0.5 ③	600	60/40 ②	A four-channel plated wire sense amplifier designed to convert ±3.0 mV (or ±4.0 mV) signals from plated wire memories to MTTL logic levels
MC1710*	601,606, 632	MC1710C*	601,606, 632	0	1700†	40	A differential comparator providing high accuracy and fast response time
MC1711*	603-02,606, 632	MC1711C*	603-02,606, 632	0	1500†	40	A dual differential comparator providing high accuracy and fast response time

Type	Temperature	Case	Input Threshold mV @ V_{ref} = 15 mV Min	Typ	Max	Common-Mode Input Firing Range (V)	Cycle Time Min (ns)	Comments
MC7520	0 to +70°C	620	11	15	19	±3.0	200	Sense amplifiers featuring dual input preamplifiers connected to a common output stage, each may be strobed independently
MC7521	0 to +70°C	620	8.0	15	22	±3.0	200	
MC7522	0 to +70°C	620	11	15	19	±3.0	200	Sense amplifiers providing dual input amplifiers connected to a common output stage, each may be strobed independently – features open collector output
MC7523	0 to +70°C	620	8.0	15	22	±3.0	200	
MC7524	0 to +70°C	620	11	15	19	±3.0	200	Sense amplifiers providing two independent sense channels, each may be strobed independently – separate AND gate outputs
MC7525	0 to +70°C	620	8.0	15	22	±3.0	200	

① -55°C/+125°C ② Diff. Mode/Com. Mode †A_{vol} ③ Input Offset Voltage, mV typ

*Also available as a non-encapsulated chip, use MCC prefix.

MILITARY and INDUSTRIAL DEVICES (continued)

LINEAR/DIGITAL INTERFACE CIRCUITS (continued)

LINE DRIVER/RECEIVER SERIES			
TYPE	Temperature	Case	Comments
MC1488	0 to +75°C	632	EIA RS-232C Interface Circuit – Quad MDTL Line Driver
MC1489 A	0 to +75°C	632	EIA RS-232C Interface Circuit – Quad MDTL Line Receiver

LINE DRIVER/RECEIVER SERIES			Impedance-typ (kΩ @ 10 MHz)			Common-Mode Voltage		
TYPE	Temperature	Case	z_{in}	z_{out}	t_p ns, max	$CMVR_{in}$ (V-min)	$CMVR_O$ (V-min)	Comments
MC1580	-55 to +125°C	632	5.0	5.0	18	±3.5	+3.0/-9.0	Dual line driver/receiver; bias driver for MECL, interfacing for MDTL, MRTL and MTTL
MC1581	-55 to +125°C	632	8.0	–	20	±3.5	–	Dual MECL line receiver
MC1582	-55 to +125°C	632	–	7.0	20	–	+9.0/-3.0	Dual MDTL and MTTL line driver
MC1583	-55 to +125°C	632	12①	–	40	±3.5	–	Dual saturated logic receiver (open-collector)
MC1584	-55 to +125°C	632	7.0	–	37	±3.5	–	Dual MDTL and MTTL receiver (active pullup)

① f = 5.0 MHz

HIGH-FREQUENCY CIRCUITS

TYPE													
-55 to +125°C	0 to +75°C	Case	V_{CC}, V_{EE} (Vdc)	Bandwidth (MHz)	V_{OS} Vp-p	$\|z_{in}\|$ kΩ	@ kHz	$\|z_o\|$ Ω	@ kHz	A_{VS} (dB)	G_T 60 MHz (dB)	Diff. Input and Output	AGC
MC1510	MC1410	601	±6.0	dc to 40	4.5	6.0	20	35	20	40 (fixed)	–	Yes	No
MC1545	MC1445	602A, 607, 632	±5.0	dc to 75	2.5	10	50	25	50	18 (fixed)	–	Yes	Yes
MC1550	–	602B, 606	+6.0	50	6.0	1.8	1.0 M	100 k	1.0 M	26 (AGC = 0)	25	No	Yes
MC1552	–	602B	+6.0	40 @ A_V = 34 dB 35 @ A_V = 40 dB	4.2	10	100	16	100	30 – 40 (fixed)	–	No	No
MC1553	–	602B	+6.0	35 @ A_V = 46 dB 15 @ A_V = 52 dB	4.2	10	100	16	100	46 – 52 (fixed)	–	No	No
MC1590	–	601	+12	100 @ A_V = 4 dB 60 @ A_V = 25 dB	7.0	3.0	1.0 M	100 k	1.0 M	44 (AGC = 0)	45	Yes	Yes
MC1733	MC1733C	603 632	±60	40 @ A_V = 52 dB 90 @ A_V = 40 dB 120 @ A_V = 20 dB	4.0	4.0 30 250	1.0 1.0 1.0	20	1.0	52 40 20	–	Yes	No

MULTIPLIERS, MODULATORS, AND DETECTORS

TYPE					
-55 to +125°C	0 to +70°C	Case	Linearity Error (Typ)	Input Voltage Range Min (Vdc)	Comments
MC1594	–	620	±0.3%	±10	A four-quadrant multiplier designed to operate with ±15-volt supplies; has internal level-shift circuitry and voltage regulator.
–	MC1494	620	±0.5%	±10	
MC1595*	–	632	X Input = 0.5% Y Input = 1.0%	±10	Applications include multiply, divide, square root, mean square, phase detector, frequency doubler, balanced modulator/demodulator, electronic gain control.
–	MC1495*	632	X Input = 1.0% Y Input = 2.0%	±10	
			Carrier Suppression Typ (dB) @ f (MHz)	Common-Mode Rejection Typ (CMRR, dB)	
MC1596	MC1496	602A, 632	65 0.5 50 10	85	Balanced modulator/demodulator designed for use where the output voltage is a product of an input voltage (signal) and a switching function (carrier).

*Also available as a non-encapsulated chip, use MCC prefix.

MILITARY and INDUSTRIAL DEVICES (continued)

REGULATORS

TYPE -55 to +125°C	TYPE 0°C to +70°C	Case	V_{in} Range (Vdc) Min	V_{in} Range (Vdc) Max	Input-Output Diff. (Vdc) Min	Input-Output Diff. (Vdc) Max	V_O Range (Vdc) Min	V_O Range (Vdc) Max	TCV_O (%/°C - Typ)	V_{ref} (Vdc) Min	V_{ref} (Vdc) Max	I_B (mAdc - Max)	I_O (mAdc - Max)	P_D (W – Max) T_C +25°C	P_D (W – Max) T_A +25°C	Reg_{Line} (Max $\frac{\%V_O}{v_{in}}$)	Reg_{Load} ($\%V_O$ - Max)
POSITIVE VOLTAGE REGULATORS																	
–	MC1460	602A 614	9.0	20	3.0	20	2.5	17	±0.002	3.2	3.8	12	200 500	1.8 12	0.68 3.0	0.030	0.13 0.05
MC1560	–	602A 614	8.5	20	2.7	20	2.5	17	±0.002	3.2	3.8	9.0	200 500	1.8 12	0.68 3.0	0.015	0.13 0.05
–	MC1461	602A 614	9.0	35	3.0	35	2.5	32	±0.002	3.2	3.8	12	200 500	1.8 17.5	0.68 3.0	0.030	0.13 0.05
MC1561	–	602A 614	8.5	40	2.7	40	2.5	37	±0.002	3.2	3.8	9.0	200 500	1.8 17.5	0.68 3.0	0.015	0.13 0.05
–	MC1469†	602A 614	9.0	35	3.0	35	2.5	32	±0.002	3.2	3.8	12	200 500	1.8 17.5	0.68 3.0	0.030	0.13 0.05
MC1569†	–	602A 614	8.5	40	2.7	40	2.5	37	±0.002	3.4	3.6	9.0	200 500	1.8 17.5	0.68 3.0	0.015	0.13 0.05
–	MC1723C†	603-03 632	9.5	40	3.0	38	2.0	37	±0.002	6.80	7.50	4.0	150	–	0.8	0.030	0.20
MC1723†	–	603-03 632	9.5	40	3.0	38	2.0	37	±0.002	6.95	7.35	3.5	150	–	0.8	0.030	0.15
–	MFC4060*	206A	9.0	35	3.0	–	4.8	32	±0.005	3.8	4.6	–	200	–	1.0	0.03	0.2
–	MFC6030*	643A	9.0	35	3.0	–	4.8	32	±0.005	3.8	4.6	–	200	–	1.0	0.03	0.2
NEGATIVE VOLTAGE REGULATORS																	
–	MC1463†	602A 614	-9.0	-35	-3.0	40	-3.8	-32	±0.002	-3.2	-3.8	14	200 500	1.8 9.0	0.68 2.4	0.030	0.13 0.05
MC1563†	–	602A 614	-8.5	-40	-2.7	35	-3.6	-37	±0.002	-3.4	-3.6	11	200 500	1.8 9.0	0.68 2.4	0.015	0.13 0.05
MULTI-PURPOSE REGULATORS																	
–	MC1466	632	① ②	①②	①	①	0	①	0.01	17.3	19.7	12	①	①	①	0.03	0.03% +3 mV 0.2% +1 mA ③
MC1566	–								0.006	18	19	8.5				0.01	0.01% +1 mV 0.1% +1 mA ③

*Temperature Range of -10 to +75°C
†Also avaiable as a non-encapsulated device, use MCC prefix.

① Limited only by the characteristics of the external series pass transistor, may be hundreds of volts or many amperes.
② An auxiliary voltage (27 Vdc nom), isolated from both the unregulated dc input voltage and Gnd, is required to bias the IC.
③ Current Load Regulation (max).

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SPECIAL-PURPOSE CIRCUITS

POWER DRIVERS TYPE	Temperature	Case	BV_{CEO} (Vdc – Typ)	I_O – Typ (A)	h_{FE} – Typ	t_{on}/t_{off} (ns – Typ)	Comments
MCH1002	-30 to +75°C	625	40	0.5	–	115/260	Dual hybrid power drivers
MCH2005	-55 to +125°C	628	30	–	1000	350/450 max	Darlington hybrid power driver
MCH2890	0 to +70°C	685	120 (min)	6.0	–	260/1800	Dual power driver for use with hammer, solenoids, relays, lamps, paper tape punches, etc.

POWER BOOSTER TYPE	Temperature	Case	Impedance – Typ Input (MΩ)	Impedance – Typ Output (Ω)	BW (MHz – Typ)	Current Gain Typ	Output Current (mAdc – Max)
MC1438	0 to +75°C	614	0.4	10	1.5	3,000	300
MC1538	-55 to +125°C	614	0.4	10	1.5	3,000	300

Comments

A high current gain amplifier (70 dB) with unity voltage gain capability.

TYPE -55 to +125°C	TYPE 0 to +70°C	Case	Output Power (W – Typ)	Voltage Gain – Typ (A_v, V/V)	Total Harmonic Distortion (% – Typ)	Comments
MC1554	MC1454	602B	1.0	10, 18, 36	0.4	A power amplifier device capable of single or split supply operation.

ZERO VOLTAGE SWITCH TYPE	Temperature	Case	Comments
MFC8070	-10 to +75°C	644A	For use in ac power switching with output capable of triggering triacs

MILITARY and INDUSTRIAL DEVICES (continued)

SPECIAL-PURPOSE CIRCUITS (continued)

3 dB QUADRATURE COUPLERS			Frequency Range (MHz)	Impedance (Ohms)	Isolation (dB) Min	Amplitude Balance (dB) Max	Phase Balance (°) Max	Insertion Loss (dB) Max	VSWR Input Max
TYPE	Temperature	Case							
MIC5830	-55 to +100°C	230	225-400	50	20	±0.5	±1.5	0.25	1.2:1
MIC5830A	-55 to +100°C	230	225-400	50	20	±0.7	±3.0	0.30	1.2:1
MIC5831	-55 to +100°C	230	450-512	50	20	±0.5	±2.5	0.35	1.2:1

POWER MODULE			V^+, Vdc	Bandwidth (MHz)	Power Gain G_p – (dB Typ)	Comments
TYPE	Temperature	Case				
MIC5840	-55 to +80°C	231	+26	225 to 400	7.0*	. . . designed as a hybrid driver or final amplifier in VHF military communications equipment.

DUPLEXER			Input Power (Watts – Max)	Isolation (dB – Typ)	Insertion Loss (dB – Typ)	Comments
TYPE	Temperature	Case				
MIC5890	0 to +120°C	631	40	25**	0.1**	This three-port hybrid network functions as a single-pole double-throw switch connecting an antenna to a transmitter or receiver.

$^*P_O$ = 6.0 Watts, T_A = +25°C **Transmit-Mode, P_{in} = 10 W, I_{IB} = 10 to 20 mA, f = 460 MHz

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At a Glance – CONSUMER DEVICES

HIGH-FREQUENCY CIRCUITS

TYPE	Temperature	Case	Small-Signal Voltage Gain (A_v,dB – Typ)	Supply Drain Current (mA – Typ)	Noise Figure (dB – Typ)	Comments
MC1330	0 to +75°C	626	34 ③	15	–	Low-level video detector for color and monochrome TV receivers: replaces 3rd IF, detector, video and AFC buffers.
MC1350	0 to +75°C	626	50 ①	14	9.0 @ 60 MHz	IF amplifier featuring wide-range AGC.
MC1352	0 to +75°C	605, 647	52 ①	27	8.5 @ 60 MHz	TV video IF amplifier with AGC and keyer circuit.
MC1353	0 to +75°C	605, 647	52 ①	27	8.5 @ 60 MHz	Identical to MC1352 except for opposite tuner AGC polarity.
MC1550	–55 to +125°C	602B, 606	25 @ 60 MHz ②	1.5	5.0 @ 60 MHz	Constant input impedance over entire AGC range, RF-IF amplifier for communications equipment.
MFC4010A	–10 to +75°C	206A	70	3.0	1.0 mV ④ @ 20 Hz to 20 kHz	Designed for AM/IF and low-level audio applications.
MFC8030	-10 to +75°C	644A	40 @ 10 MHz	Variable	7.0	Differential cascode amplifier, ideal general-purpose differential building block.

TYPE	Temperature	Case	Typical BV_{CEO} (Vdc)	V_{CC}, Supply Voltage (Vdc – Max)	Max Base Differential Voltage ($\|\Delta V_{BE}\|$,mV)	Max Base Differential Current ($\|\Delta I_B\|$,μA)	Comments
MFC8000	–10 to +75°C	644A	40	75	15	1.0	Dual differential amplifiers; designed for the input stage of stereo power amplifiers
MFC8001	–10 to +75°C	644A	50	75	15	1.0	
MFC8002	–10 to +75°C	644A	60	75	15	1.0	

① Power gain ② Transducer power gain ③ Conversion gain ④ Output noise voltage

INTEGRATED CIRCUITS

LINEAR

HIGH-FREQUENCY CIRCUITS (continued)

SOUND IF AMPLIFIERS			Small-Signal Voltage Gain (A_v,dB – Typ)	Supply Drain Current (mA – Typ)	AM Rejection (dB – Typ)	Comments
TYPE	Temperature	Case				
MC1351	0 to +75°C	605, 647	65 ⑤	31	45	TV sound IF amplifier with quadrature detector and audio preamplifier
MC1357	0 to +75°C	646, 647	60 ⑤	15	45	TV sound IF with quadrature detector or FM radio IF amplifier
MC1358	−20 to +75°C	646, 647	>60 ⑥	33	51	TV sound IF with limiter, FM detector, audio driver, electronic attenuator
FM IF AMPLIFIERS			**Input Signal 3 dB Limiting (mV [rms] – Typ)**	**Small-Signal Voltage Gain (A_v,dB – Typ)**	**AM Rejection (e_{in} = 1 V [rms]) (dB – Typ)**	**Comments**
TYPE	**Temperature**	**Case**				
MFC6010	−10 to +75°C	643A	55	40 dB @ 10.7 MHz	40 dB	FM limiting IF amplifier designed for 10.7 MHz IF applications.
MC1355	0 to +75°C	605, 647	1.75	40 dB @ 10.7 MHz	60 dB	Four-stage limiting FM amplifier
MC1357	0 to +75°C	646, 647	0.6	53 dB @ 10.7 MHz	37 dB ⑦	TV sound IF with quadrature detector or FM radio IF amplifier suitable for automotive applications

⑤ IF voltage gain ⑥ Attenuator Volume Reduction Range ⑦ e_{in} = 10 mV (rms)

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LOW-FREQUENCY CIRCUITS

AUDIO POWER AMPLIFIER CIRCUITS						
TYPE	Temperature	Case	Output Power (W – Min)	Input Sensitivity @ Full P_O (mV – Max)	THD @ ½ Rated Pwr (% – Typ)	Comments
MC1306	0 to +75°C	626	0.5	270/360 ①	0.5	Complementary power amplifier and preamplifier
MFC4000B	−10 to +75°C	206A	0.25	42 ②	0.7	Designed for the output stage of battery-powered portable radios.
MFC6070	-10 to +55°C	643A	1.0	150	1.0	Designed for low-cost audio amplifiers in phonograph, TV and radio applications.
MFC8010	−10 to +55°C	644A	1.0	10 ②	1.0	Provides the complete audio system in TV, radio, and phonograph equipment, includes preamplifier
MFC9020	-10 to +75°C	641	2.0	200	1.0	Designed for the complete audio system in television, radio and phonograph equipment
DRIVER AND AUDIO PREAMPLIFIER CIRCUITS						
TYPE	**Temperature**	**Case**	**Open-Loop Voltage Gain (dB – Typ)**	**Power Supply Voltage (Vdc – Max)**	**Output Swing (V[rms] – Typ)**	**Comments**
MC1303	0 to +75°C	632	80	±15	5.5	Dual monolithic stereo preamplifier, channel separation of 60 dB min at 10 kHz
MC1380	-40 to +75°C	627	49	18	30*	Designed to drive germanium power transistors in auto radios
MFC4050	−10 to +75°C	206A	42	18	30*	Audio driver designed for driving Class A PNP power output stage of up to 4 watts of audio power
MFC8020A	−10 to +75°C	644A	80	35	9.0 (V_{CC} = 32 Vdc)	Class B audio driver designed as a preamplifier and driver circuit for complementary output transistors, will drive ≦ 15 W
MFC8040	−10 to +75°C	644A	90	33	7.0 (V_{CC} = 30 Vdc)	Low noise audio preamplifier, input noise level of 1.0 μV typical

① A_{vol}, preamplifier/power amplifier ② Input sensitivity is externally adjustable. *mA (rms) output current

REGULATORS

TYPE 0°C to +70°C	Case	V_{in} Range (Vdc) Min	V_{in} Range (Vdc) Max	Input Output Diff. (Vdc) Min	Input Output Diff. (Vdc) Max	V_O Range (Vdc) Min	V_O Range (Vdc) Max	TCV_O (%/°C - Typ)	V_{ref} (Vdc) Min	V_{ref} (Vdc) Max	I_{IB} (mAdc - Max)	I_O (mAdc - Max)	P_D (W – Max) T_C +25°C	P_D (W – Max) T_A +25°C	Reg_{Line} (Max $\frac{\%V_O}{V_{in}}$)	Reg_{Load} (%V_O-Max)
POSITIVE VOLTAGE REGULATORS																
MC1460	602A 614	9.0	20	3.0	20	2.5	17	±0.002	3.2	3.8	12	200 500	1.8 12	0.68 3.0	0.030	0.13 0.05
MC1461	602A 614	9.0	35	3.0	35	2.5	32	±0.002	3.2	3.8	12	200 500	1.8 17.5	0.68 3.0	0.030	0.13 0.05
MC1469†	602A 614	9.0	35	3.0	35	2.5	32	±0.002	3.2	3.8	12	200 500	1.8 17.5	0.68 3.0	0.030	0.13 0.05
MC1723C†	603-03 632	9.5	40	3.0	38	2.0	37	±0.002	6.80	7.50	4.0	150	–	0.8	0.030	0.20
MFC4060*	206A	9.0	35	3.0	–	4.8	32	±0.005	3.8	4.6	–	200	–	1.0	0.03	0.2
MFC6030*	643A	9.0	35	3.0	–	4.8	32	±0.005	3.8	4.6	–	200	–	1.0	0.03	0.2
NEGATIVE VOLTAGE REGULATORS																
MC1463†	602A 614	-9.0	-35	-3.0	40	-3.8	-32	±0.002	-3.2	-3.8	14	200 500	1.8 9.0	0.68 2.4	0.030	0.13 0.05
MULTI-PURPOSE REGULATORS																
MC1466	632	① ②	① ②	①	①	0	①	0.01	17.3	19.7	12	①	①	①	0.03	0.03% +3 mV 0.2% +1 mA ③

*Temperature Range of -10 to +75°C
† Also available as a non-encapsulated chip, use MCC prefix.

① Limited only by the characteristics of the external series pass transistor, may be hundreds of volts or many amperes.

② An auxiliary voltage (27 Vdc nom), isolated from both the unregulated dc input voltage and Gnd, is required to bias the IC.

③ Current Load Regulation (max).

SPECIAL-PURPOSE CIRCUITS

STEREO DEMODULATORS TYPE	Temperature	Case	Power Supply Voltage Range (Vdc – Typ)	THD – Typ (%)	P_D – Max (mW)	Comments
MC1304	0 to +75°C	605, 647	8.0-14	0.5	625	An FM multiplex stereo demodulator; derives the left and right channel audio information from the detected composite signal. MC1305 permits use of external stereo-channel separation control.
MC1305	0 to +75°C	605, 647	8.0-14	0.5	625	
MC1307	0 to +75°C	605, 647	8.0-14	0.5	625	Thrifty version of MC1304, without audio mute and stereo switch capabilities.

CHROMA DEMODULATORS TYPE	Temperature	Case	Output Voltage Swing (Vp-p – Typ)	Output Differential Voltage (Vdc – Typ)	Output Voltage Temperature Coefficient (mV/°C – Typ)	Comments
MC1326	0 to +75°C	605, 647	10	0.3	3.0	Dual doubly balanced chroma demodulator with RGB matrix and luminance and blanking inputs.
MC1328	0 to +75°C	603-02, 605 647	10	0.3	3.0	Dual doubly balanced chroma demodulator.

SPECIAL-PURPOSE CIRCUITS (continued)

TUNING INDICATOR			Drain Current (mA – Typ)	Saturation Voltage (Vdc – Typ)	Noise Inhibit (Vdc – Typ)	Threshold		Comments
TYPE	Temperature	Case				Lamp On Min/Max (Vdc)	Lamp Off Min/Max (Vdc)	
MC1335	0 to +75°C	626	5.5	0.85	1.9	5.8/6.2	5.1/6.9	Designed for fine tuning of FM radios

TV SIGNAL PROCESSOR			
TYPE	Temperature	Case	Comments
MC1345	0 to +70°C	605	. . . with sync separator, advanced high-quality noise inverter AGC Keyer and AGC amplifier. Features one IF AGC output, two tuner AGC outputs and adjustable AGC delay

AUTOMATIC FREQUENCY CONTROL			
TYPE	Temperature	Case	
MC1364	0 to + 75°C	605, 686	High-gain AFT system – 18 mV input for rated output

TV COLOR PROCESSING CIRCUIT			
TYPE	Temperature	Case	
MC1398	–20 to +75°C	605	. . . includes complete Chroma IF amplifier, automatic chroma control, color killer, dc chroma control and injection lock reference system with dc hue conrtol. Low peripheral parts count.

ELECTRONIC ATTENUATOR			Voltage Gain (dB – Typ)	Attenuation Range (dB – Typ)	THD (% – Typ)	Power Supply Voltage Range (Vdc)	Comments
TYPE	Temperature	Case					
MFC6040	-10 to +75°C	643A	13	90	0.6†	9.0 to 18	Ideal for dc volume control and AGC audio amplifier applications.

ZERO VOLTAGE SWITCH			
TYPE	Temperature	Case	Comments
MFC8070	-10 to +75°C	644A	For use in ac power switching with output capable of triggering triacs

†At Unity Gain

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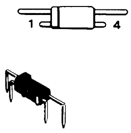
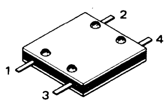
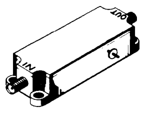
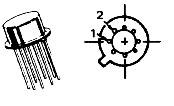
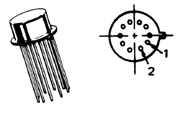
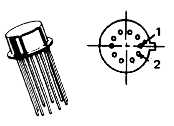
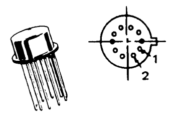
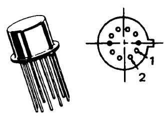
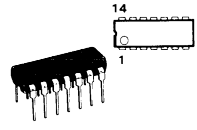
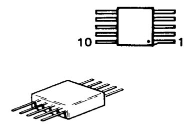
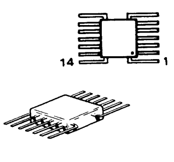
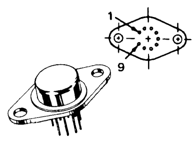
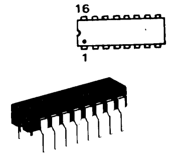
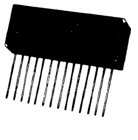
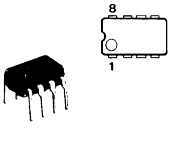
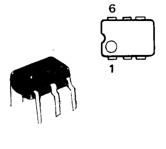
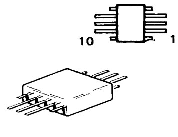
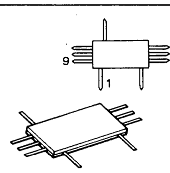
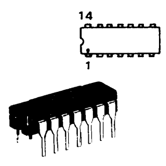
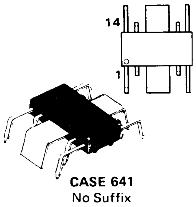
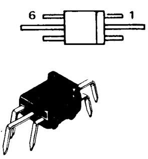
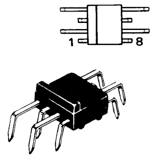
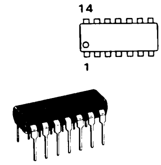
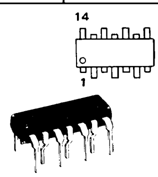
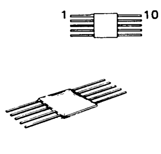
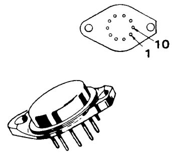
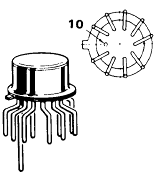
LINEAR IC PACKAGES

 **CASE 206A** No Suffix	 **CASE 230** No Suffix	 **CASE 231** No Suffix	 **CASE 601** (TO-99) Suffix G after type number	 **CASE 602A** Suffix G after type number
 **CASE 602B** Suffix G after type number	 **CASE 603-02** (TO-100) Suffix G after type number	 **CASE 603-03** Suffix G after type number	 **CASE 605** (TO-116) Suffix P after type number	 **CASE 606** (TO-91) Suffix F after type number
	 **CASE 607** (TO-86) Suffix F after type number	 **CASE 614** Suffix R after type number	 **CASE 620** Suffix L after type number	
 **CASE 625** Suffix P after type number	 **CASE 626** Suffix P after type number	 **CASE 627** Suffix P after type number	 **CASE 628** Suffix F after type number	 **CASE 631** No Suffix
 **CASE 632** (TO-116) Suffix L after type number	 **CASE 641** No Suffix	 **CASE 643A** No Suffix	 **CASE 644A** No Suffix	 **CASE 646** Suffix P after type number
 **CASE 647** Suffix PQ after type number	 **CASE 665** Suffix F after type number	 **CASE 685** Suffix R after type number	 **CASE 686** Suffix G after type number	

MC1303L

DUAL STEREO PREAMPLIFIER

MONOLITHIC DUAL STEREO PREAMPLIFIER

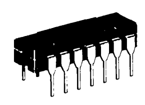
. . . designed for amplifying low-level stereo audio signals with two preamplifiers built into a single monolithic semiconductor.

Each Preamplifier Features:

- Large Output Voltage Swing – 4.0 V(rms) min
- High Open-Loop Voltage Gain = 6000 min
- Channel Separation = 60 dB min at 10 kHz
- Short-Circuit-Proof Design

DUAL STEREO PREAMPLIFIER INTEGRATED CIRCUIT

MONOLITHIC SILICON EPITAXIAL PASSIVATED



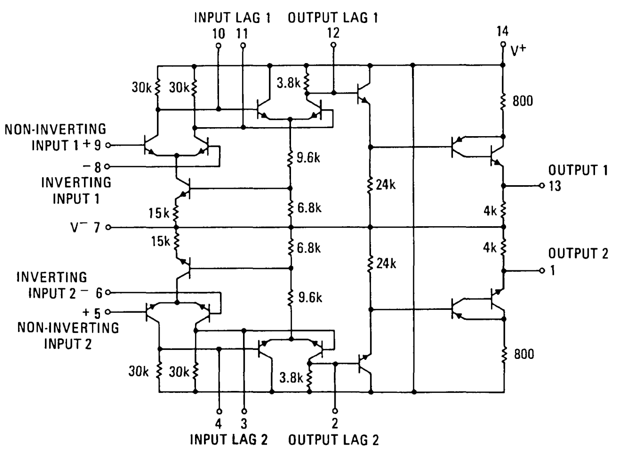
CERAMIC PACKAGE
CASE 632
TO-116

MAXIMUM RATINGS (T_A = + 25°C unless otherwise noted)

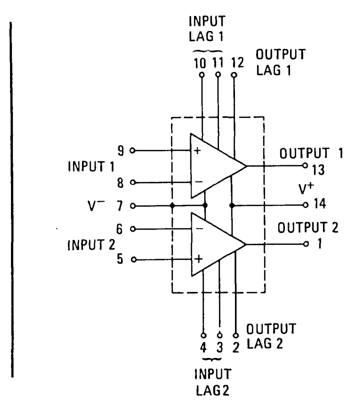
Rating	Symbol	Value	Unit
Power Supply Voltage	V^+ V^-	+15 -15	Vdc Vdc
Power Dissipation (Package Limitation) Derate above 25°C	P_D	625 5.0	mW mW/°C
Operating Temperature Range	T_A	0 to +75	°C

Maximum Ratings as defined in MIL-S-19500, Appendix A.

CIRCUIT SCHEMATIC

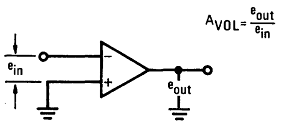
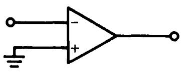
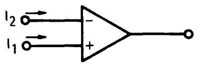
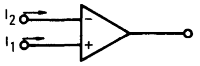
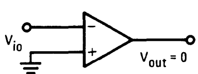
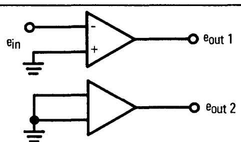


EQUIVALENT CIRCUIT



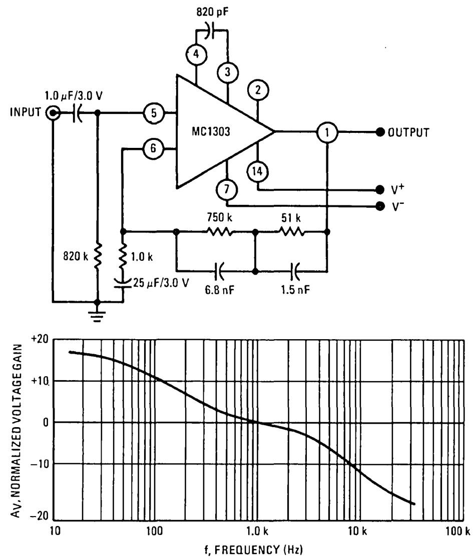
See Packaging Information Section for outline dimensions.

ELECTRICAL CHARACTERISTICS (Each Preamplifier) (V^+ = +13 Vdc, V^- = -13 Vdc, T_A = +25°C unless otherwise noted)

Characteristic Definitions (linear operations)	Characteristic	Symbol	Min	Typ	Max	Unit
	Open Loop Voltage Gain	A_{VOL}	6,000	10,000	-	V/V
	Output Voltage Swing (R_L = 10 kΩ)	V_{out}	4.0	5.5	-	V(rms)
	Input Bias Current $I_b = \frac{I_1 + I_2}{2}$	I_b	-	1.0	10	µA
	Input Offset Current ($I_{io} = I_1 - I_2$)	I_{io}	-	0.2	0.4	µA
	Input Offset Voltage	V_{io}	-	1.5	10	mV
	DC Power Dissipation (Power Supply = ±13 V, V_{out} = 0)	P_D	-	-	400	mW
	Channel Separation (f = 10 kHz)	$\frac{e_{out\ 1}}{e_{out\ 2}}$	60	70	-	dB

TYPICAL PREAMPLIFIER APPLICATIONS

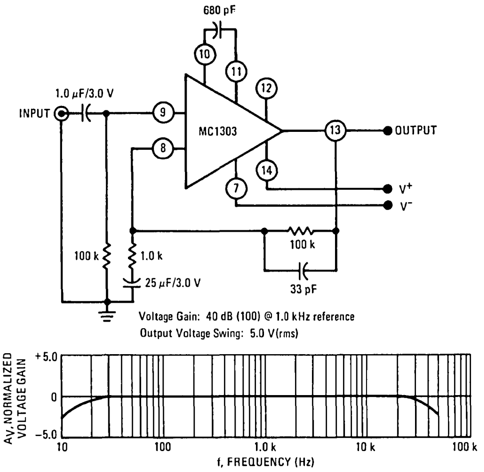
FIGURE 1 – MAGNETIC PHONO PLAYBACK PREAMPLIFIER/RIAA EQUALIZED



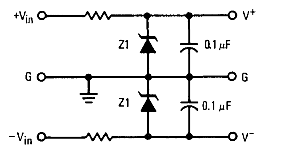
TYPICAL PERFORMANCE CHARACTERISTICS

Voltage Gain	: 34 dB (50) @ 1.0 kHz
Input Overload Point	: 100 mVrms @ 1.0 kHz
Output Voltage Swing	: 5.0 Vrms @ 1.0 kHz @ 0.1% THD.
Output Noise Level	: Better Than 70 dB Below 10 mV Phono Input (Input Shorted)

FIGURE 2 – BROADBAND AUDIO AMPLIFIER

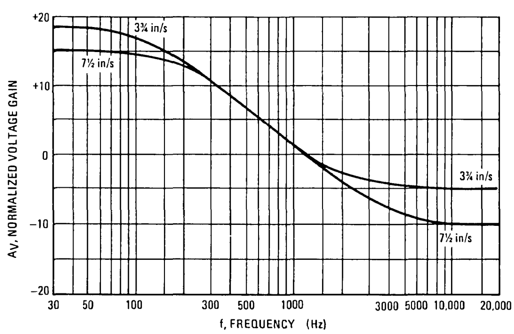


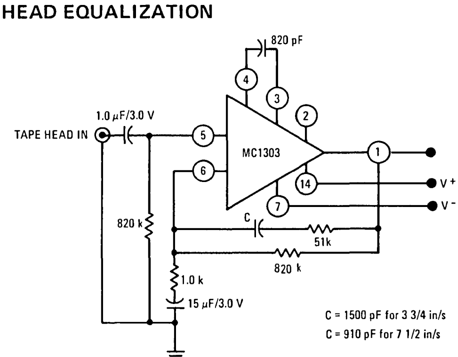
SUGGESTED POWER SUPPLY CIRCUIT



Z1 = MZ-500-19 (13 V nom.)
Select series R by allowing 11 mA for zener, and each dual I/C Preamplifier

FIGURE 3 – NAB TAPE HEAD EQUALIZATION





C = 1500 pF for 3 3/4 in/s
C = 910 pF for 7 1/2 in/s

Voltage Gain: 35 dB @ 1.0 kHz
Output Voltage Swing: 5.0 V(rms)

FIGURE 4 – POWER DISSIPATION versus SUPPLY VOLTAGE

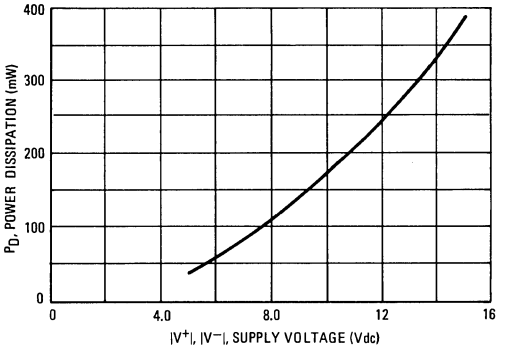


FIGURE 5 – OUTPUT LINEARITY

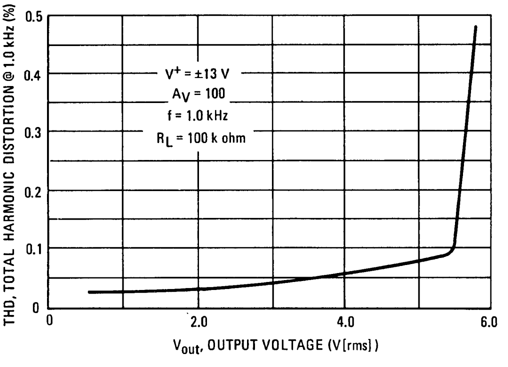
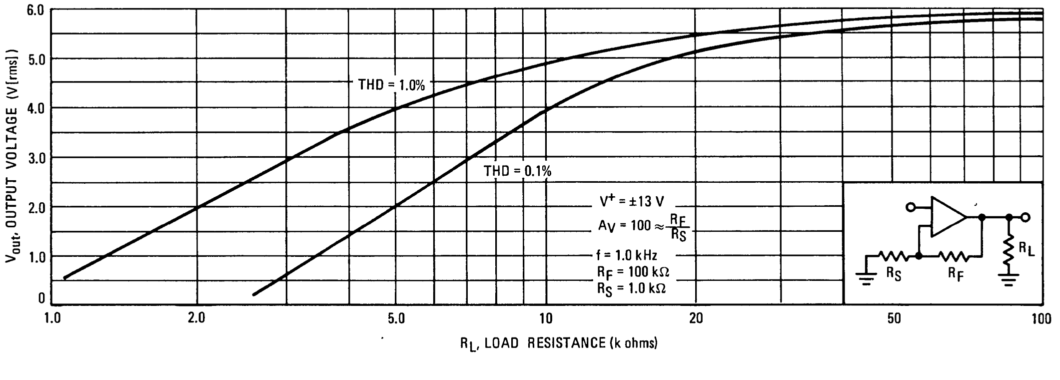


FIGURE 6 – INFLUENCE OF OUTPUT LOADING



6

NOISE CHARACTERISTICS

FIGURE 7A – INFLUENCE OF SOURCE RESISTANCE & BANDWIDTH

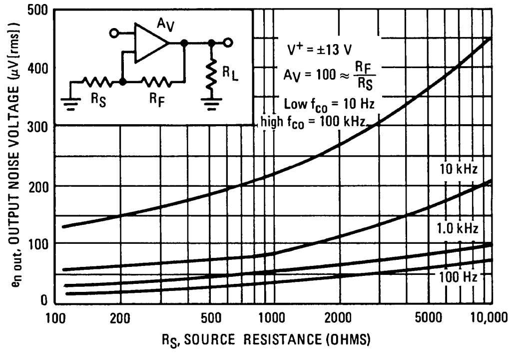
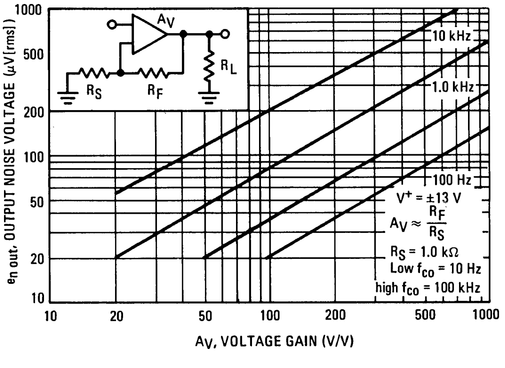


FIGURE 7B – INFLUENCE OF VOLTAGE GAIN & BANDWIDTH



MC1304
MC1305

STEREO DEMODULATOR

MONOLITHIC FM MULTIPLEX STEREO DEMODULATORS

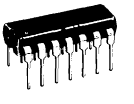
. . . derive the left and right audio information from the detected composite signal. The MC1304 eliminates the need for an external stereo-channel separation control. The MC1305 is similar to the MC1304 but permits the use of an external stereo-channel separation control for maximum separation.

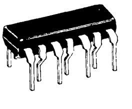
- Operation Practicable Over Wide Power-Supply Range, 8-14 Vdc
- Built-in Stereo-Indicator Lamp Driver
- Total Audio Muting Capability
- Automatic Switching – Stereo-Monaural
- Monaural Squelch Capability

FM MULTIPLEX STEREO DEMODULATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT

P SUFFIX
PLASTIC PACKAGE
CASE 605
TO-116





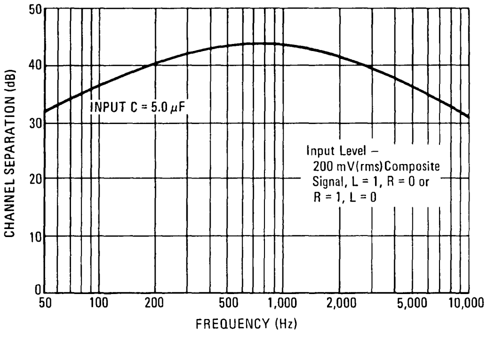
PQ SUFFIX
PLASTIC PACKAGE
CASE 647

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

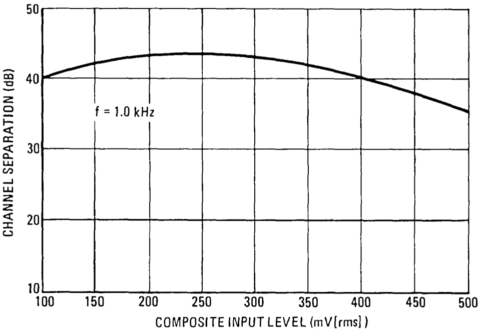
Rating	Value	Unit
Power Supply Voltage (Pins 1, 6, 9,* 11, 12) (Pin 7 is grounded)	+22	Vdc
Lamp Driver Current	40	mAdc
Power Dissipation (Package Limitation) (Both Packages) Derate above T_A = 25°C	625 5.0	mW mW/°C
Operating Temperature Range (Ambient)	0 to +75	°C
Storage Temperature Range	-65 to +150	°C

*Pin 8 for MC1305   "Maximum Ratings" as defined in MIL-S-19500, Appendix A.

CHANNEL SEPARATION versus FREQUENCY



CHANNEL SEPARATION versus COMPOSITE INPUT LEVEL



See Packaging Information Section for outline dimensions.

ELECTRICAL CHARACTERISTICS [V+ = 12 Vdc, T_A = +25°C unless otherwise noted. Test made with 75 μs de-emphasis network (3.9 kΩ, 0.02 μF) unless otherwise noted].

Characteristics	Min	Typ	Max	Unit
Input Impedance (f = 20 Hz)	12	20	–	kΩ
Stereo Channel Separation (See Notes 1 and 2) (f = 100 Hz) (f = 1.0 kHz) (f = 10 kHz)	– – –	35 45 30	– – –	dB
Channel Balance (Monaural Input = 200 mV[rms]), (Monaural, Left and Right Outputs)	–	0.5	–	dB
Total Harmonic Distortion (See Notes 1 and 3) (Modulation frequency - 1.0 kHz)	–	0.5	1.0	%
Ultrasonic Frequency Rejection (See Note 4) (19 kHz) (38 kHz)	– –	25 20	– –	dB
Inherent SCA Rejection (without filter) @60 kHz, 67 kHz and 74 kHz	–	50	–	dB
Lamp Indicator (R_A = 120Ω) Minimum 19 kHz Input Level for lamp on Maximum 19 kHz Input Level for lamp off	– 5.0	16 14	25 –	mV(rms)
Audio Muting Mute on (Voltage required at pin 5) Mute off (Voltage required at pin 5) Attentuation in Mute Mode (Note 5)	0.6 1.3 –	– – 55	1.0 2.0 –	Vdc Vdc dB
Stereo-Monaural Switching Stereo (Voltage required at pin 4) Monaural (Voltage required at pin 4)	1.3 –	– –	2.0 1.0	Vdc
Power Dissipation (V+ = 10 V) (Without lamp) (With lamp)	– –	150 180	300 300	mW

Note 1 – Measurement made with 200 mV(rms) Standard Multiplex Composite Signal and L = 1, R = 0 or R = 1, L = 0. Standard Multiplex Composite signal is here defined as a signal containing left and/or right audio information with a 10% (19 kHz) pilot signal in accordance with FCC regulations.

Note 2 – Stereo channel separation is adjustable for the MC1305 with a resistor from pin 9 to ground.

Note 3 – Distortion specification also applies to Monaural Signal.

Note 4 – Referenced to 1 kHz output signal with Standard Multiplex Composite Input Signal.

Note 5 – This is referenced to 1.0 kHz output signal with either Standard Multiplex Composite Signal or Monaural Input Signal.

FIGURE 1 – DISTORTION COMPONENTS IN AUDIO SIGNAL

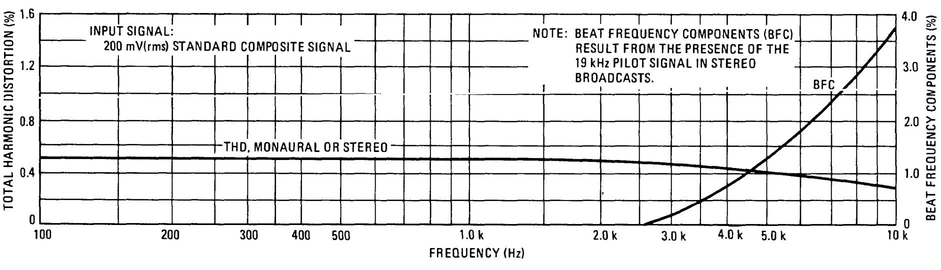


FIGURE 2 – TOTAL HARMONIC DISTORTION

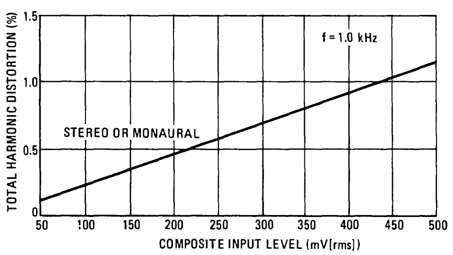


FIGURE 3 – MULTIPLEX SENSITIVITY

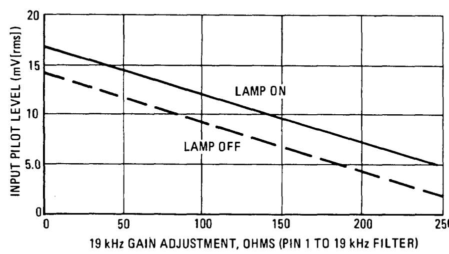


FIGURE 4 – MC1304 CIRCUIT SCHEMATIC

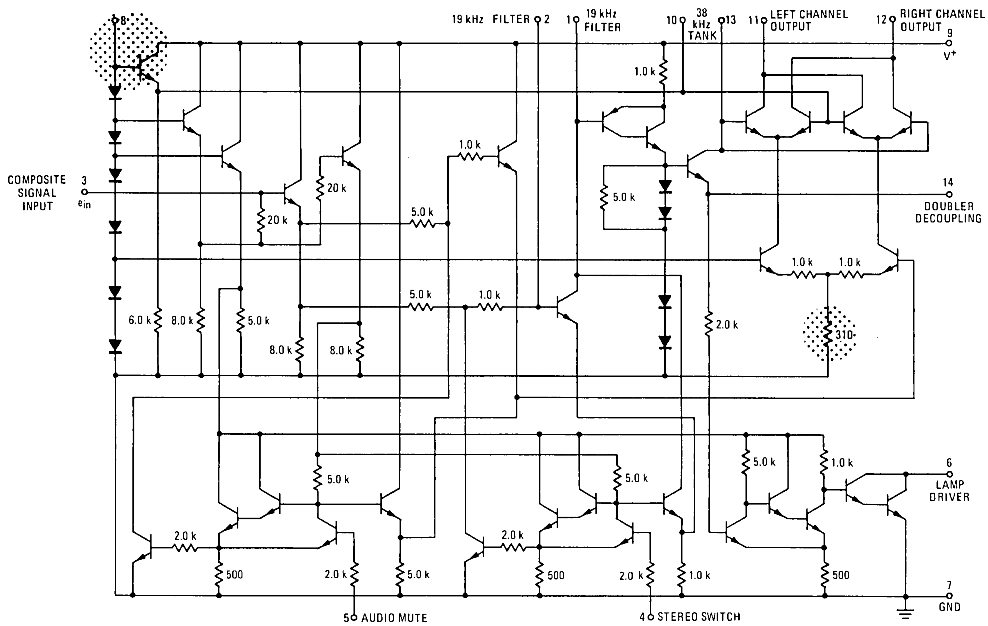
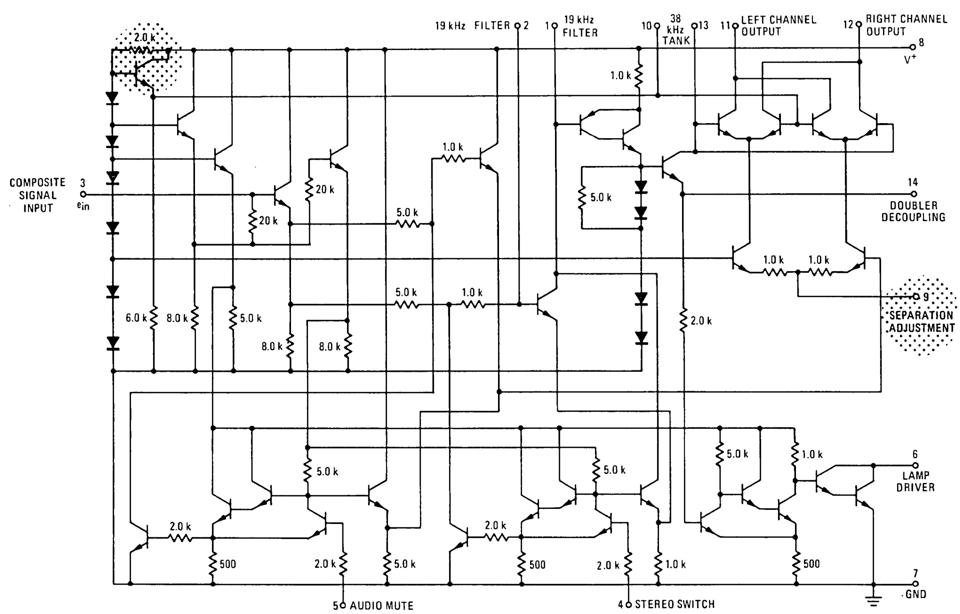


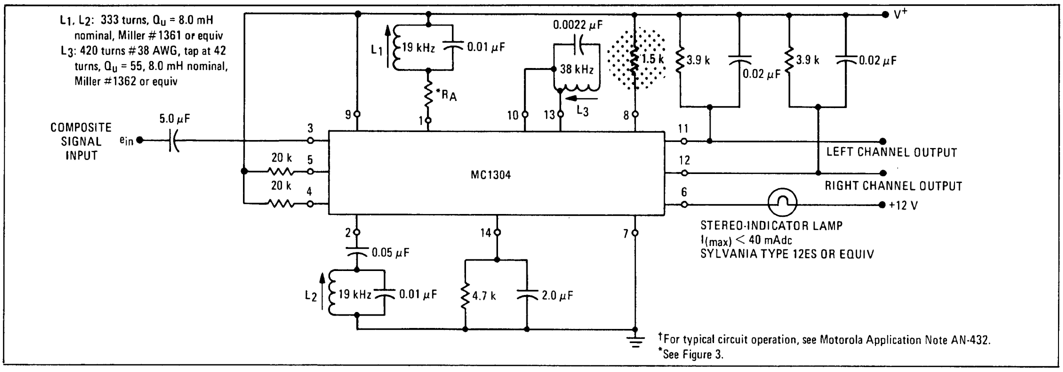
FIGURE 5 – MC1305 CIRCUIT SCHEMATIC



Portions of the circuits shown within the dotted areas pertain to the MC1304 or MC1305 as indicated by the titles of the circuits.

6

FIGURE 6 – MC1304 TYPICAL CIRCUIT CONFIGURATION†

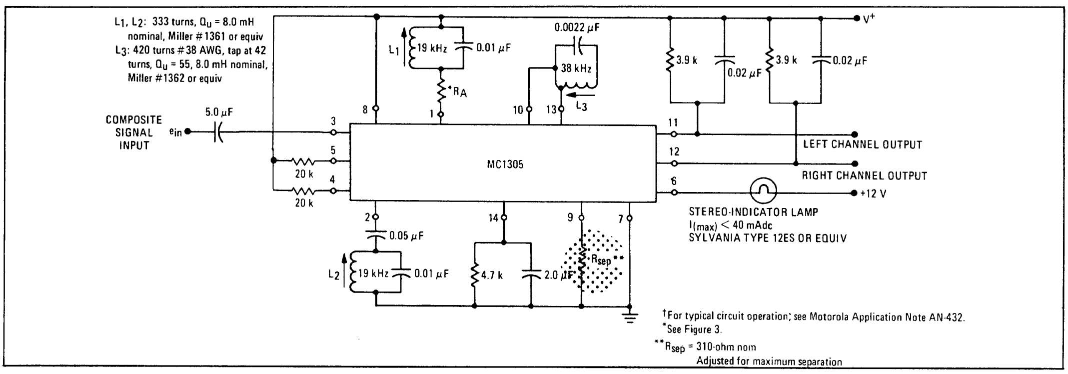


Typical dc voltages (All voltages measured with respect to ground, Pin 7, R_A = 0)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
V_{CC} = 8.5 Vdc	8.5	2.0	2.8	1.6	1.6	0.8	0	4.6*	8.5	3.9	6.3	6.3	3.9	1.9
V_{CC} = 12 Vdc	12	2.0	2.8	1.9	1.9	0.8	0	4.6**	12	3.9	9.7	9.7	3.9	1.9

*1.5 kΩ in series with pin 8
**2.7 kΩ in series with pin 8

FIGURE 7 – MC1305 TYPICAL CIRCUIT CONFIGURATION†



Typical dc voltages (All voltages measured with respect to ground Pin 7)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
V_{CC} = 8.5 Vdc	8.5	2.0	2.8	1.6	1.6	0.8	0	8.5	0.32	3.9	6.3	6.3	3.9	1.9
V_{CC} = 12 Vdc	12	2.0	2.8	1.9	1.9	0.8	0	12	0.36	3.9	9.7	9.7	3.9	1.9

Portions of the circuits shown within the dotted areas pertain to the MC1304 or MC1305 as indicated by the titles of the circuits.

MC1306P

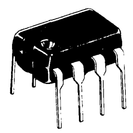
AUDIO AMPLIFIER

1/2-WATT AUDIO AMPLIFIER

The MC1306P is a monolithic complementary power amplifier and preamplifier designed to deliver 1/2-Watt into a loudspeaker with a 3.0 mV(rms) typical input. Gain and bandwidth are externally adjustable. Typical applications include portable AM-FM radios, tape recorder, phonographs, and intercoms.

- 1/2-Watt Power Output (9.0 Vdc Supply, 8-Ohm Load)
- High Overall Gain – 3.0 mV(rms) Sensitivity for 1/2-Watt Output
- Low Zero-Signal Current Drain – 4.0 mAdc @ 9.0 V typ
- Low Distortion – 0.5% at 250 mW typ

1/2-WATT AUDIO AMPLIFIER



PLASTIC PACKAGE
CASE 626

TYPICAL APPLICATIONS

FIGURE 1 – AM-FM RADIO, AUDIO SECTION

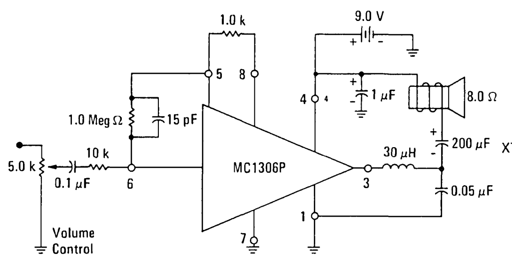
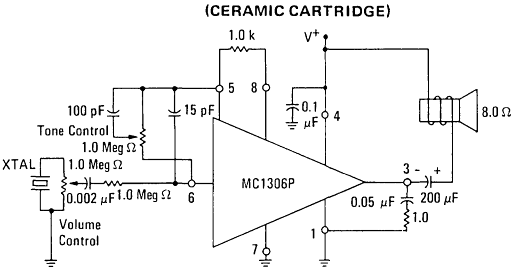
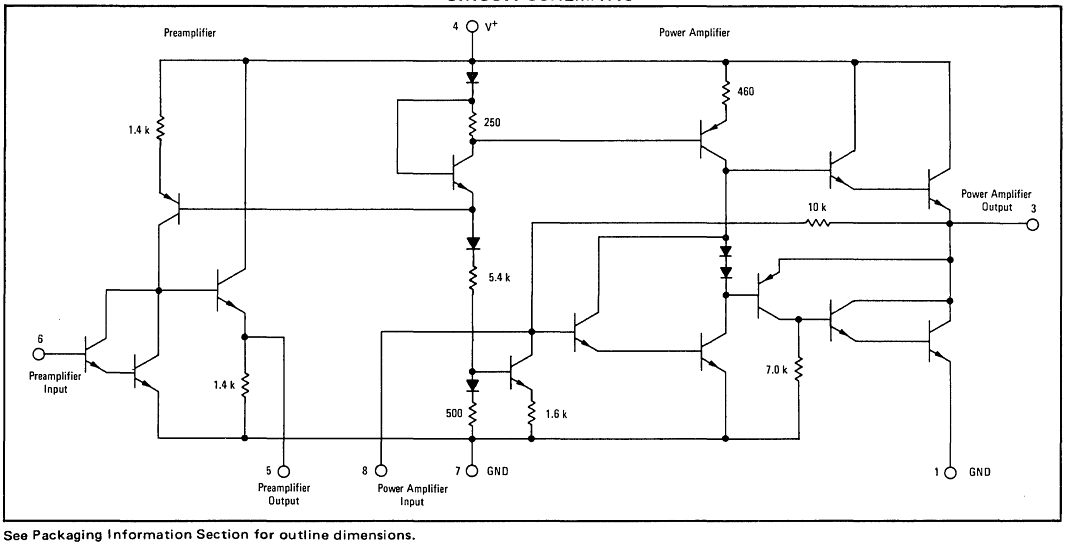


FIGURE 2 – PHONOGRAPH AMPLIFIER (CERAMIC CARTRIDGE)



CIRCUIT SCHEMATIC



See Packaging Information Section for outline dimensions.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+	12	Vdc
Load Current	I_L	400	mAdc
Power Dissipation (Package Limitation) T_A = +25°C Derate above T_A = +25°C	P_D $1/\theta_{JA}$	 625 5.0	 mW mW/°C
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

Maximum Ratings as defined in MIL-S-19500, Appendix A.

ELECTRICAL CHARACTERISTICS (V^+ = 9.0 V, R_L = 8.0 ohms, f = 1.0 kHz, (using test circuit of Figure 3), T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Open Loop Voltage Gain Pre-amplifier R_L = 1.0 k ohm Power-amplifier R_L = 16 ohms	A_{VOL}	 – –	 270 360	 – –	V/V
Sensitivity (P_o = 500 mW)	S	–	3.0	–	mV(rms)
Output Impedance (Power-amplifier)	Z_o	–	0.5	–	Ohm
Signal to Noise Ratio (P_o = 150 mW, f = 300 Hz to 10 kHz)	S/N	–	55	–	dB
Total Harmonic Distortion (P_o = 250 mW)	THD	–	0.5	–	%
Quiescent Output Voltage	V_o	–	$V^+/2$	–	Vdc
Output Power (THD ≤10%)	P_o	 500	 570	–	mW
Current Drain (zero signal)	I_D	–	4.0	–	mA
Power Dissipation (zero signal)	P_D	–	36	–	mW

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FIGURE 3 — TEST CIRCUIT

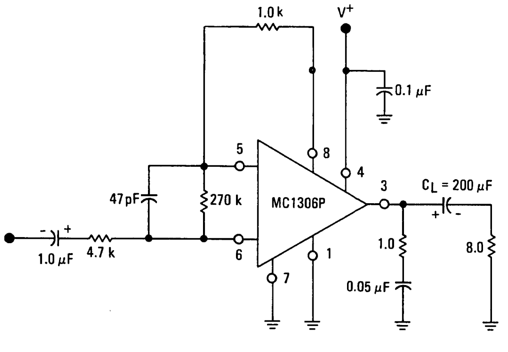
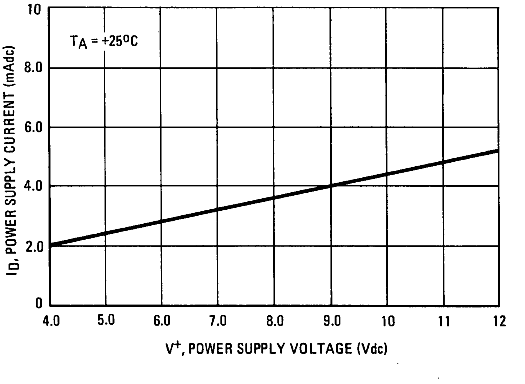


FIGURE 4 — ZERO SIGNAL BIAS CURRENT



TYPICAL CHARACTERISTICS

(V^+ = 9.0 V, f = 1.0 kHz, T_A = +25°C unless otherwise noted)

FIGURE 5 – EFFICIENCY

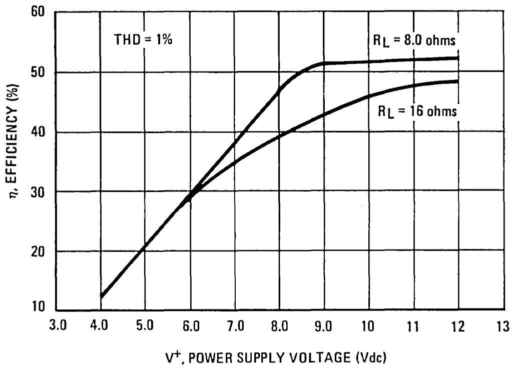


FIGURE 6 – OUTPUT POWER

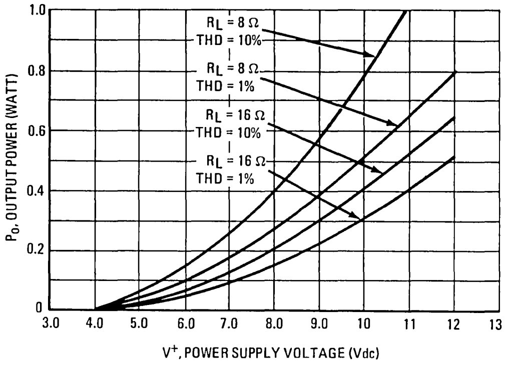


FIGURE 7 – TOTAL HARMONIC DISTORTION

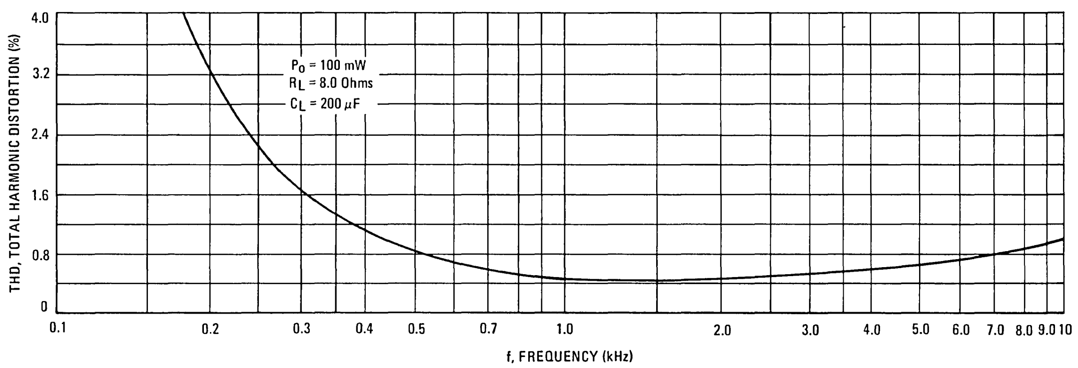


FIGURE 8 – EFFECT OF BATTERY AGING ON LOW-LEVEL DISTORTION

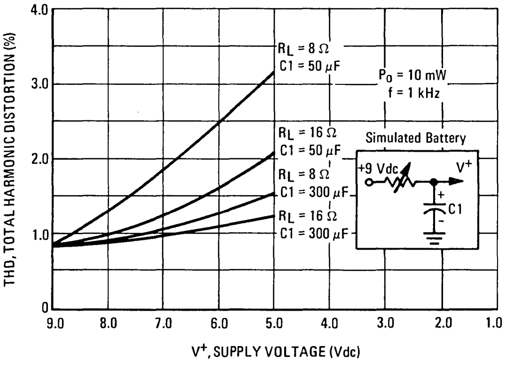


FIGURE 9 – DISTORTION

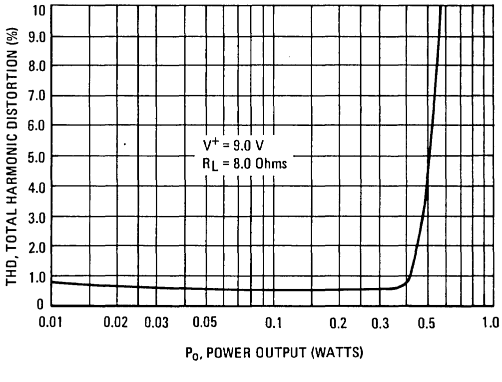
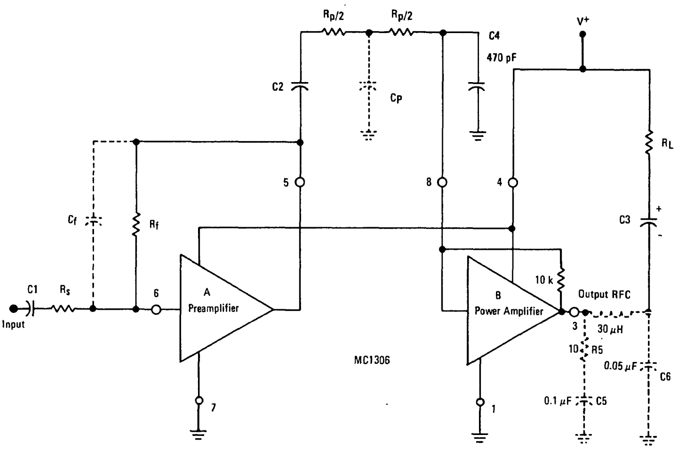


FIGURE 10 — TYPICAL CIRCUIT CONNECTION



DESIGN CONSIDERATIONS

The MC1306P provides the designer with a means to control preamplifier gain, power amplifier gain, input impedance, and frequency response. The following relationships will serve as guides.

1. Gain

The Preamplifier Stage Voltage Gain is:

$$A_{VA} \approx \frac{R_f}{R_s}$$

and is limited only by the open-loop gain (270 V/V). For good preamplifier dc stability R_f should be no larger than 1.0-megohm.

The Power Amplifier Voltage Gain is controlled in a similar manner where:

$$A_{VB} \approx \frac{10\text{ k}}{R_p}$$

The 10-k ohm feedback resistor is provided in the integrated circuit.

Recommended values of R_p range from 500-ohms to 3.3-k ohms. The low end is limited primarily by low-level distortion and the upper end is limited due to the voltage drive capabilities of the pre-amplifier. (A resistor can be added in the dc feedback loop, from pin 6 to ground, to increase this drive). The Overall Voltage Gain, then, is:

$$A_{VT} = \frac{R_f\ 10\text{ k}}{R_s\ R_p}$$

2. Input Impedance

The Preamplifier Input Impedance is:

$$Z_{in\,A} \approx R_s$$

and the Power Amplifier Input Impedance is:

$$Z_{in\,B} \approx R_p$$

3. Frequency Response

The low frequency response is controlled by the cumulative effect of the series coupling capacitors C1, C2, and C3. High-frequency response can be determined by the feedback capacitor, C_f, and the -3.0 dB point occurs when

$$X_{C_f} = R_f$$

Additional high frequency roll-off and noise reduction can be achieved by placing a capacitor from the center point of R_p to ground as shown in Figure 10.

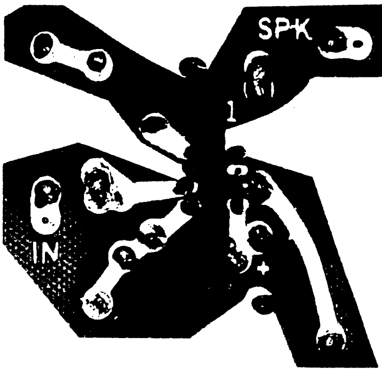
Capacitor C4 and the RC network shown in dotted lines may be needed to prevent high frequency parasitic oscillations. The RF choke, shown in series with the output, and capacitor C6 are used to prevent the high-frequency components in a large-signal clipped audio output waveform from radiating into the RF or IF sections of a radio (Figure 10).

4. Battery Operation

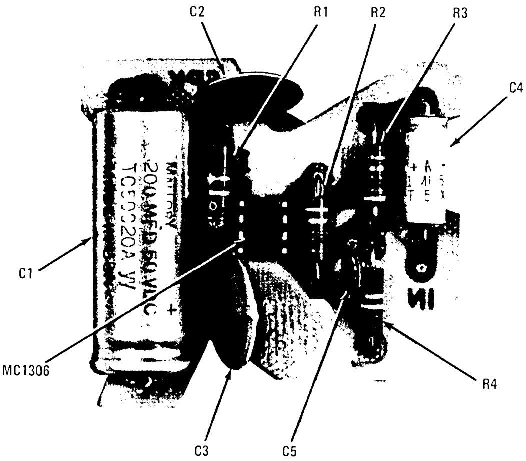
The increase of battery resistance with age has two undesirable effects on circuit performance. One effect is the increasing of amplifier distortion at low signal levels. This is readily corrected by increasing the size of the filter capacitor placed across the battery (as shown in Figure 8; a 300-μF filter capacitor gives distortions at low-tonal levels that are comparable to the "stiff" supply). The second effect of supply impedance is a lowering of power output capability for steady signals. This condition is not correctable, but is of questionable importance for music and voice signals.

5. Application Examples: (1) The audio section of the AM-FM radio (Figure 1) is adjusted for a preamplifier gain of 100 with an input impedance of 10-k ohms. The power amplifier gain is set at 10, which gives an overall voltage gain of 1000. The bandwidth has been set at 10-kHz. (2) The phono amplifier (Figure 2) is designed for a preamplifier gain of unity and a power amplifier gain of 10. The input impedance is 1.0-megohm. An adjustable treble control is provided within the feedback loop.

TYPICAL PRINTED CIRCUIT BOARD LAYOUT



LOCATION OF COMPONENTS



See Figure 3 for schematic diagram.

PARTS LIST

Component	Value
C1	200 μF
C2	0.1 μF
C3	0.05 μF
C4	1.0 μF
C5	47 pF
R1	1 ohm
R2	1 k ohm
R3	4.7 k ohms
R4	270 k ohms
MC1306	–
PC Board	–

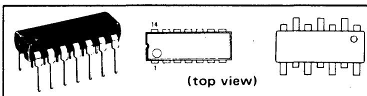
MONOLITHIC FM MULTIPLEX STEREO DEMODULATOR

. . . designed to derive the left and right channel audio information from the detected composite signal.

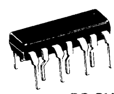
- Capable of Operation Over a Wide Power Supply Range – 8.0 – 14 Vdc
- Built-in Stereo-Indicator Lamp Driver

FM MULTIPLEX STEREO DEMODULATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT

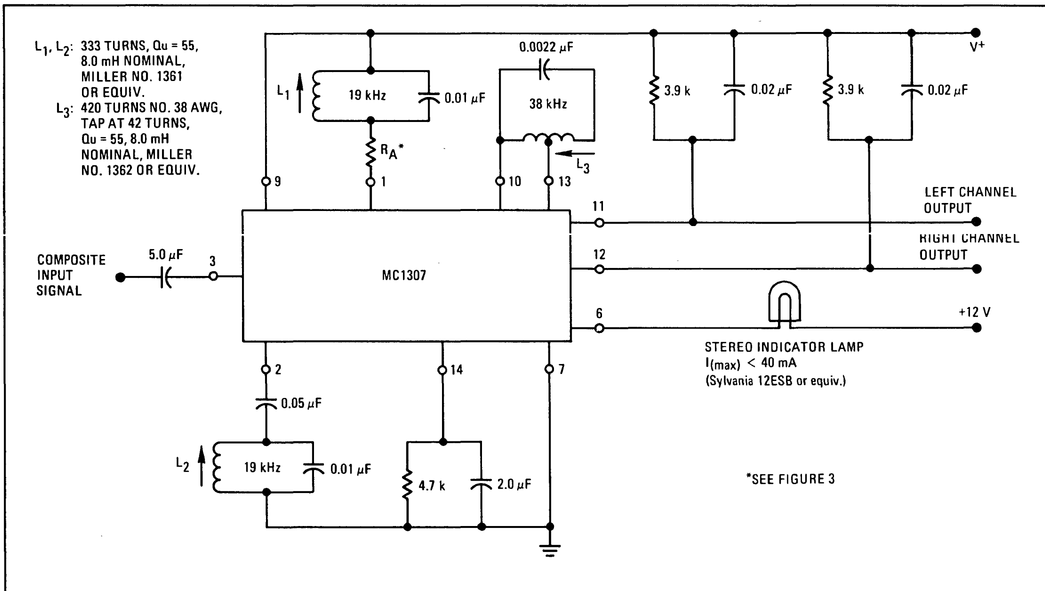


P SUFFIX
PLASTIC PACKAGE
CASE 605
TO-116



PQ SUFFIX
PLASTIC PACKAGE
CASE 647

FIGURE 1 – TYPICAL CIRCUIT CONFIGURATION

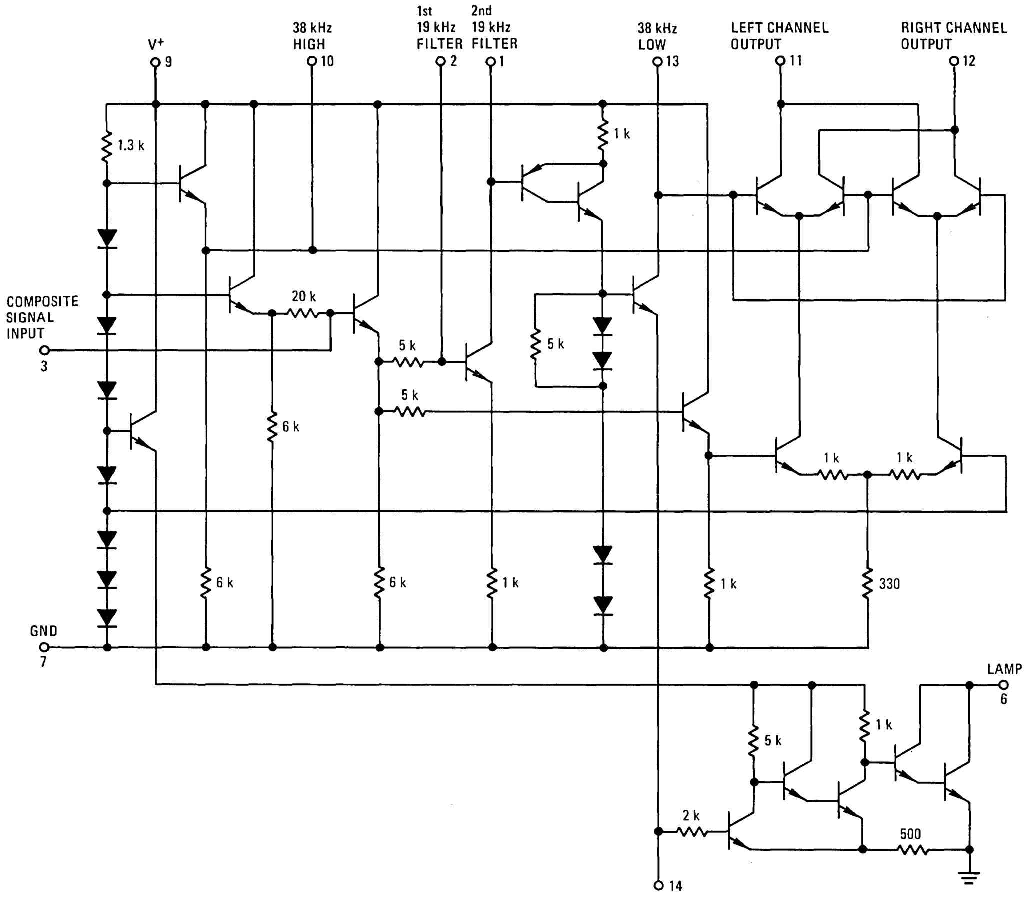


TYPICAL DC VOLTAGES (All measured using a VTVM with respect to Pin 7 (lamp on), R_A = 180 ohms, see Figure 3)

Pin Numbers	1	2	3	4	5	6	7	8	9	10	11	12	13	14
V^+ = 8.5 Vdc	8.5	2.7	3.6	–	–	0.8	0	–	8.5	4.4	6.2	6.2	4.4	1.5
V^+ = 12 Vdc	12	2.9	3.9	–	–	0.9	0	–	12	4.7	9.7	9.7	4.7	1.7

See Packaging Information Section for outline dimensions.

FIGURE 2 – CIRCUIT SCHEMATIC



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Value	Unit
Power Supply Voltage (Pins 1, 6, 9, 11, 12) (Pin 7 is grounded)	+22	Vdc
Lamp Driver Current	40	mAdc
Power Dissipation (Package Limitation) Derate above T_A = +25°C	625 5.0	mW mW/°C
Operating Temperature Range (Ambient)	0 to +75	°C
Storage Temperature Range	–65 to +150	°C

Maximum Ratings as defined in MIL-S-19500, Appendix A.

ELECTRICAL CHARACTERISTICS (V^+ = 12 Vdc, T_A = +25°C, tests made with a 75 μs de-emphasis network (3.9 kΩ, 0.02 μF) unless otherwise noted)

Characteristic	Min	Typ	Max	Unit
Input Impedance (f = 1.0 kHz)	12	20	–	kΩ
Stereo Channel Separation (See Note 1) (f = 100 Hz) (f = 1.0 kHz) (f = 10 kHz)	 – 20 –	 35 40 30	 – – –	dB
Total Harmonic Distortion (See Notes 1 and 2) (Modulation Frequency = 1.0 kHz)	–	0.5	1.0	%
Channel Balance (Monaural Input = 200 mV [rms]) (Monaural, Left and Right Outputs)	–	0.5	–	dB
Ultrasonic Frequency Rejection (See Note 3) (19 kHz) (38 kHz)	 – –	 25 20	 – –	dB
Inherent SCA Rejection (without filter) (f = 60 kHz, 67 kHz and 74 kHz) (See Note 3)	–	50	–	dB
Lamp Indicator (R_A = 180 Ω) (Minimum 19 kHz input level for lamp "on") (Maximum 19 kHz input level for lamp "off")	 – 5.0	 16 14	 25 –	mV(rms)
Power Dissipation (V^+ = 12 V) (Without lamp) (With lamp)	 – –	 140 170	 300 300	mW

Note 1 – Measurement made with 200 mV(rms) Standard Multiplex Composite Signal where L = 1, R = 0 or R = 1, L = 0. Standard Multiplex Composite Signal is here defined as a signal containing left and/or right audio information with a 10% (19 kHz) pilot signal in accordance with FCC regulations.

Note 2 – Distortion specification also applies to Monaural Signal.

Note 3 – Referenced to 1.0 kHz output signal with Standard Multiplex Composite Input Signal.

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FIGURE 3 – DISTORTION COMPONENTS IN AUDIO SIGNAL

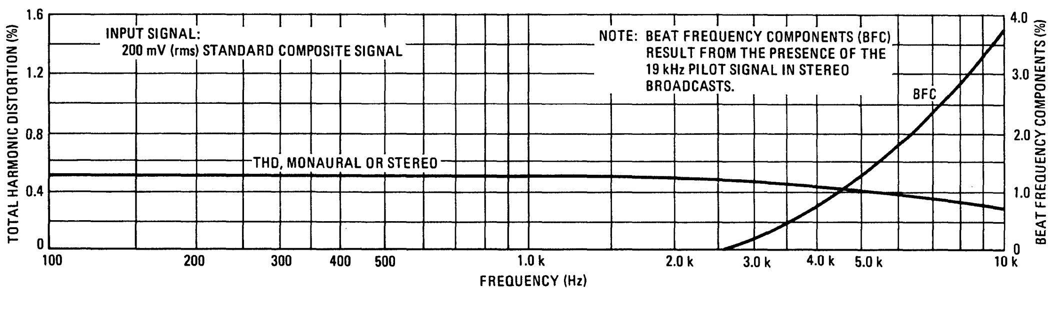


FIGURE 4 – TOTAL HARMONIC DISTORTION

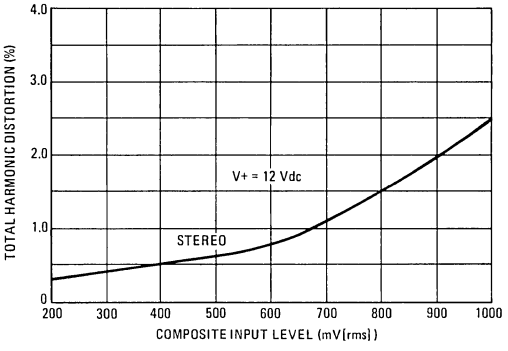


FIGURE 5 – MULTIPLEX SENSITIVITY

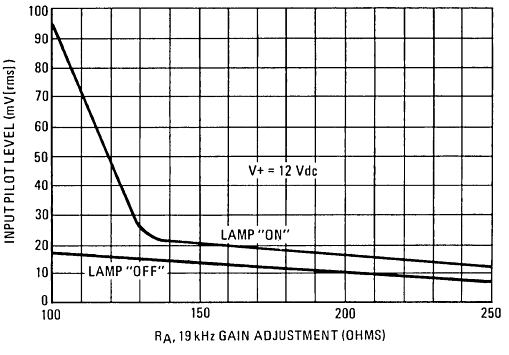


FIGURE 6 – CHANNEL SEPARATION

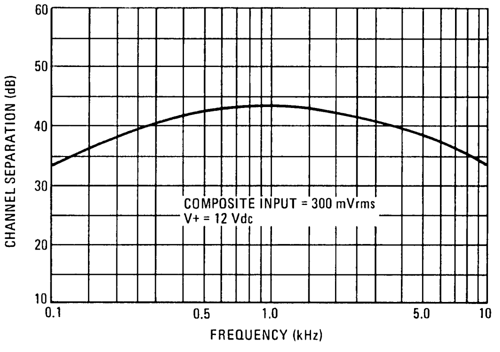
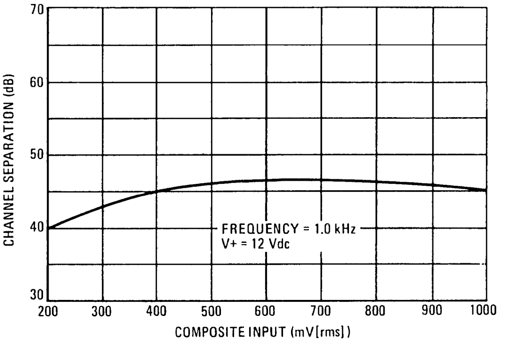


FIGURE 7 – CHANNEL SEPARATION



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MC1326

DUAL CHROMA DEMODULATOR

DUAL DOUBLY BALANCED CHROMA DEMODULATOR WITH R G B MATRIX AND CHROMA DRIVER STAGES

. . . a monolithic device designed for use in solid-state color television receivers.

- Luminance Input Provided
- Good Chroma Sensitivity – 0.3 Vp-p Input for 5 Vp-p Output
- Low Differential Output DC Offset Voltage – 0.6 V max
- DC Temperature Stability – 3 mV/°C typ
- Negligible Change in Output Voltage Swing with Varying 3.58 MHz Reference Input Signal
- High Ripple Rejection Achieved with MOS Filter Capacitors
- High Blue Output Voltage Swing – 10 Vp-p typ
- Blanking Input Provided

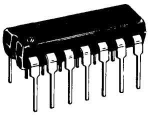
MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Value	Unit
Power Supply Voltage	30	Vdc
Chroma Signal Input Voltage	5.0	Vpk
Reference Signal Input Voltage	5.0	Vpk
Minimum Load Resistance	3.0	k ohms
Luminance Input Voltage	12	Vp-p
Blanking Input Voltage	7.0	Vp-p
Power Dissipation (Package Limitation) Plastic Packages Derate above T_A = +25°C	 625 5.0	 mW mW/°C
Operating Temperature Range (Ambient)	0 to +75	°C
Storage Temperature Range	–65 to +150	°C

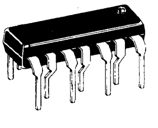
Maximum Ratings as defined in MIL-S-19500, Appendix A.

DUAL DOUBLY BALANCED CHROMA DEMODULATOR WITH R G B OUTPUT MATRIX

MONOLITHIC SILICON INTEGRATED CIRCUIT

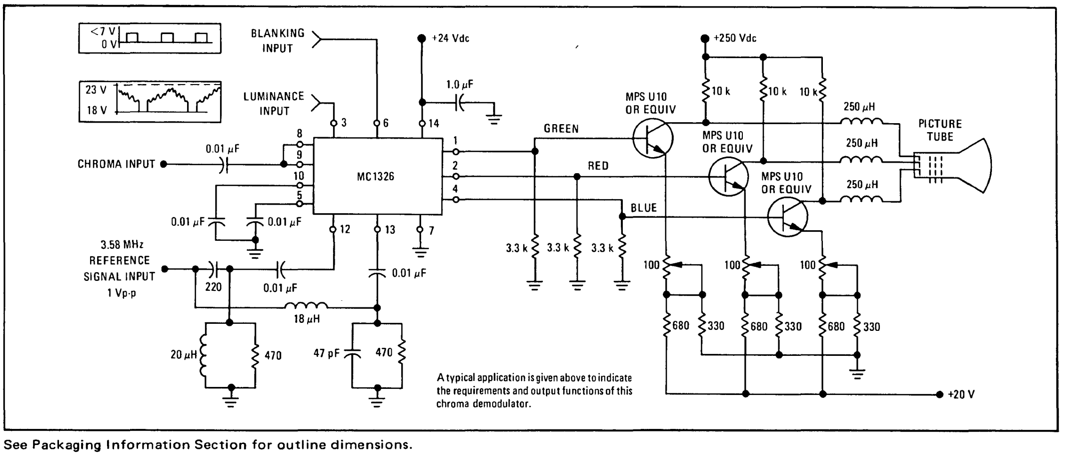


P SUFFIX
PLASTIC PACKAGE
CASE 605
TO-116



PQ SUFFIX
PLASTIC PACKAGE
CASE 647

FIGURE 1 – MC1326 TYPICAL APPLICATION

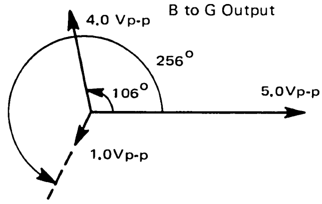


See Packaging Information Section for outline dimensions.

ELECTRICAL CHARACTERISTICS (V^+ = 24 Vdc, R_L = 3.3 k ohms, T_A = +25°C unless otherwise noted)

Characteristic	Pin No.	Min	Typ	Max	Unit
STATIC CHARACTERISTICS					
Quiescent Output Voltage See Figure 2	1, 2, 4	13	14.4	16	Vdc
Quiescent Input Current from Supply (Figure 2) ($R_L = \infty$) (R_L = 3.3 k ohms)		 – 16.5	 6.0 19	 – 25.5	mA
Reference Input DC Voltage (Figure 2)	5,12,13	–	6.2	–	Vdc
Chroma Reference Input DC Voltage (Figure 2)	8,9,10	–	3.4	–	Vdc
Differential Output Voltage (Reference Input Voltage = 1.0 Vp-p) See Note 1 and Figure 3	1, 2, 4	–	0.3	0.6	Vdc
Output Voltage Temperature Coefficient (Reference Input Voltage = 1.0 Vp-p, +25° to +65°C) See Note 1 and Figure 3	1, 2, 4	–	3.0	–	mV/°C

DYNAMIC CHARACTERISTICS (V^+ = 24 Vdc, R_L = 3.3 k ohms, Reference Input Voltage = 1.0 Vp-p, T_A = +25°C unless otherwise noted)

Characteristic	Pin No.	Min	Typ	Max	Unit
Blue Output Voltage Swing See Note 2 and Figure 4	4	8.0	10	–	Vp-p
Chroma Input Voltage (B Output = 5.0 Vp-p) See Note 3 and Figure 4	8	–	0.3	0.7	Vp-p
Luminance Input Resistance	3	100	–	–	kΩ
Luminance Gain From Pin 3 to Outputs (@ dc) (@ 5.0 MHz)	1, 2, 4	 – –	 0.95 0.5	 – –	–
Blanking Input Resistance 1.0 Vdc 0 Vdc	6	 – –	 1.1 75	 – –	kΩ
Detected Output Voltage (Adjust B Output to 5.0 Vp-p, Luminance Voltage = 23 V) See Note 4 G Output R Output	4 1 2	 0.75 3.5	 1.0 3.8	 1.25 4.2	Vp-p
Relative Output Phase (B Output = 5.0 Vp-p, Luminance Voltage = 23 V) B to R Output B to G Output 	 4, 2 4, 1	 101 248	 106 256	 111 264	Degrees
Demodulator Unbalance Voltage (no Chroma Input Voltage and normal Reference Signal Input Voltage)	1, 2, 4	–	250	500	mVp-p
B-Y Phase Shift (B-Y Reference Input to B-Y Output)	4, 13	–	3	–	Degrees
Residual Carrier and Harmonics Output Voltage (with Input Signal Voltage, normal Reference Signal Voltage and B Output = 5.0 Vp-p)	1, 2, 4	–	0.7	1.5	Vp-p
Reference Input Resistance (Chroma Input = 0)	12, 13	–	2.0	–	kΩ
Reference Input Capacitance (Chroma Input = 0)	12, 13	–	6.0	–	pF
Chroma Input Resistance	8, 9, 10	–	2.0	–	kΩ
Chroma Input Capacitance	8, 9, 10	–	2.0	–	pF

NOTES:

1. With Chroma Input Signal Voltage = 0 and normal Reference Input Signal Voltage = 1.0 Vp-p, all output voltages will be within specified limits and will not differ from each other by greater than 0.6 Vdc.
2. With normal Reference Input Signal Voltage, adjust Chroma Input Signal Voltage to 0.6 Vp-p.
3. With normal Reference Input Signal Voltage, adjust Chroma Input Signal Voltage until the Blue Output Voltage = 5 Vp-p. The Chroma Input Voltage at this point should be equal to or less than 0.7 Vp-p.
4. With normal Reference Input Signal Voltage, adjust the Chroma Input Signal until the Blue Output Voltage = 5 Vp-p. At this point, the Red and Green voltages will fall within the specified limits.

TEST CIRCUITS

(V+ = 24 Vdc, R_L = 3.3 Kilohms, T_A = +25°C unless otherwise noted)

FIGURE 2 – DC TEST CIRCUIT WITHOUT REFERENCE INPUT SIGNAL VOLTAGE (B-Y AND R-Y)
(For Testing Quiescent Current, DC Output Voltage, Difference Voltage)

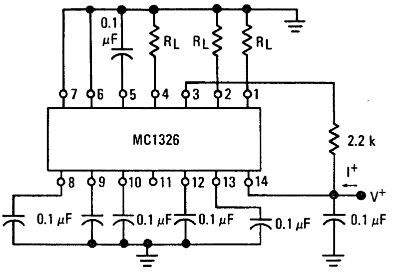


FIGURE 3 – DC OUTPUT VOLTAGE TEST CIRCUIT WITH NORMAL REFERENCE INPUT VOLTAGE (B, R, AND G)

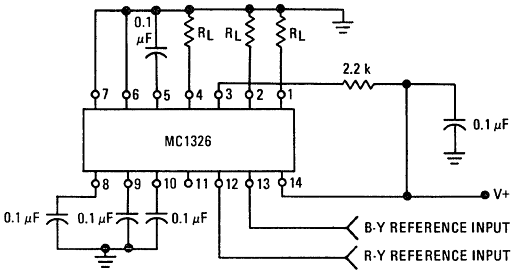


FIGURE 4 – DYNAMIC TEST CIRCUIT

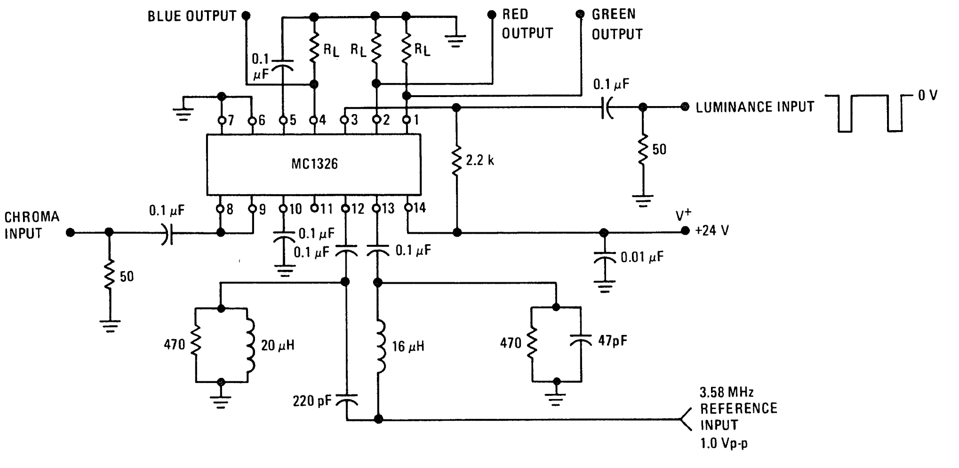


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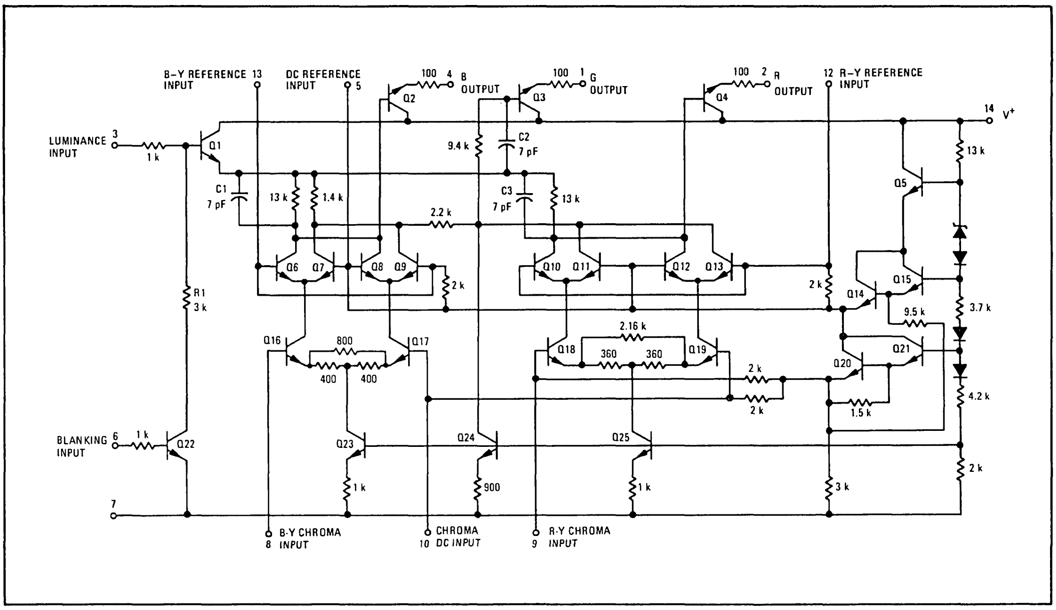
FIGURE 5 – CIRCUIT SCHEMATIC



CIRCUIT OPERATION

A double sideband suppressed carrier chroma signal flows between the bases of the two differential pairs, Q16 and Q17, Q18 and Q19. A reference signal of approximately 1 Vp-p amplitude having the same frequency as the suppressed chroma carrier with an appropriate phase relationship is supplied between the bases of the upper differential pairs Q6 and Q7, Q8 and Q9, Q10 and Q11, Q12 and Q13. The upper pairs are switched between full conduction and zero conduction at the carrier frequency rate. The collectors of the upper pairs are cross-coupled so that "doubly balanced" or "full-wave" synchronous detected chroma signals are obtained. Both positive and negative phases of the detected signal are available at opposite collector pairs.

While the detector section is almost identical to other available units, several excellent additional features are incorporated. Transistor Q1 is used as an emitter follower to which the collector load resistors of the detectors are returned. The collector impedances of the upper pair transistors are high compared with the collector load resistors, and any signal at the emitter of Q1 appears virtually unattenuated at the collectors of the upper pairs, and hence at the three detector output terminals. This feature may be used to mix the correct amount of the luminance portion of the color TV signal with the color difference signals produced by the detectors to give R-G-B outputs directly.

Capacitors C1, C2, and C3 compensate for most of the high frequency roll-off in the luminance signal. This is due to the collector capacitances of the detector transistors and the input capacitances of the emitter followers, Q2, Q3, Q4. Capacitors C1, C2, and C3 provide filtering of carrier harmonics from the detected color difference signals. This increases the available swing before clipping for the color difference signal, and reduces the high frequency components which must pass through the emitter followers (Q2, Q3, Q4) into the video output stages. Since high capacitance (>100 pF) is characteristic of the input impedance of a video output stage, the transistor emitter followers must operate at a high quiescent current (>5 mA) in order to pass large high frequency components without distortion. The filtering reduces the quiescent current required in the emitter followers and thus reduces dissipation in the integrated circuit.

If it is not required to mix the luminance signal via Q1, this transistor can be used for brightness control. If the base of Q1 is connected to a suitable variable dc voltage, this will vary the dc output levels of the three detected outputs accordingly and thereby vary the picture brightness level.

Blanking of the picture during line and frame flyback may be achieved by applying a positive-going blanking signal to the base of Q22. With an extra external resistor in series with the Q1 base of approximately 5 k ohms, when Q22 is turned on by the blanking pulse, the base of Q1 will be pulled negative by the current in R1, thus forcing all three detected outputs to go negative by the same amount. In a conventional solid-state receiver with a single video output stage driving the picture tube cathode, a negative-going signal at the base of the video output stage will blank the picture tube. When using the blanking input be certain the blanking pulse does not switch off the luminance input stage Q1 completely; this would turn off the collector supply for the demodulators and put the entire chroma demodulator out of lock at each blanking pulse.

Matrix for MC1326

$$\frac{\text{R-Y gain}}{\text{B-Y gain}} = 0.77$$

$$\text{-G-Y} = 0.11\ (\text{B-Y}) + 0.28\ (\text{R-Y})$$

For indicated requirements and output functions of the MC1326 chroma demodulator please refer to the typical application shown on the first page of this specification.

TYPICAL CHARACTERISTICS
(T_A = +25°C unless otherwise noted)

(Figures 6 through Figure 10 Reference Test Circuit of Figure 2)

FIGURE 6 – DC OUTPUT VOLTAGE

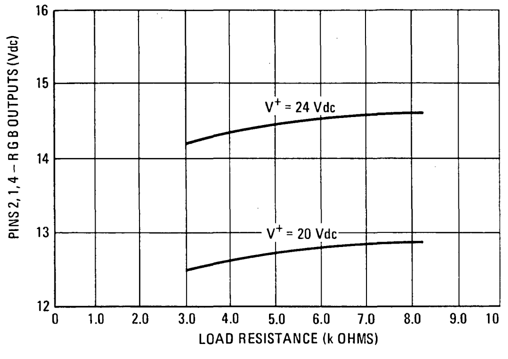


FIGURE 7 – POWER DISSIPATION

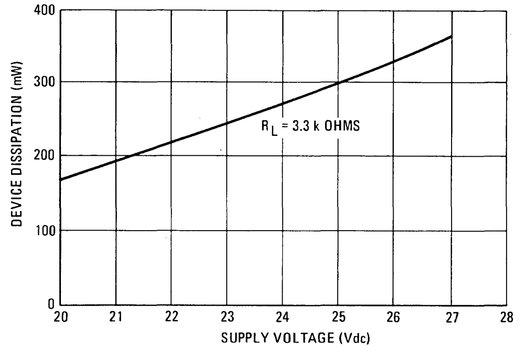


FIGURE 8 – DC OUTPUT VOLTAGE

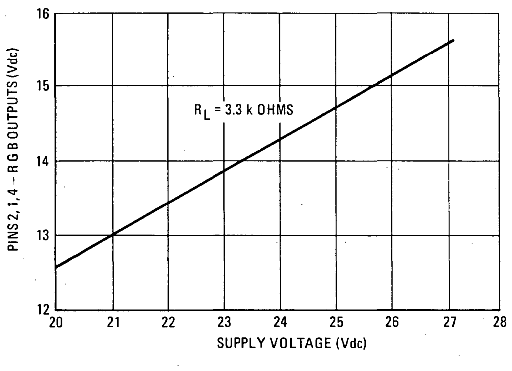


FIGURE 9 – POWER DISSIPATION

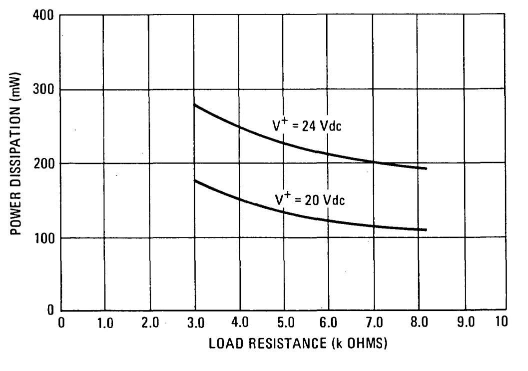


FIGURE 10 – DC OUTPUT VOLTAGE

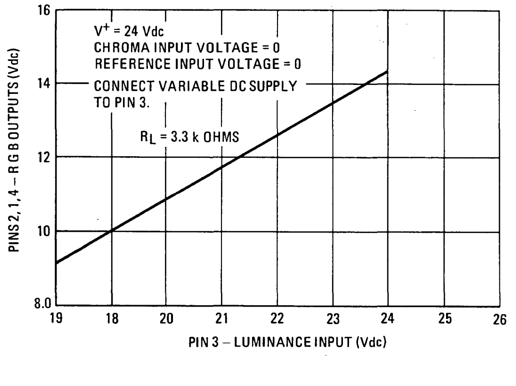
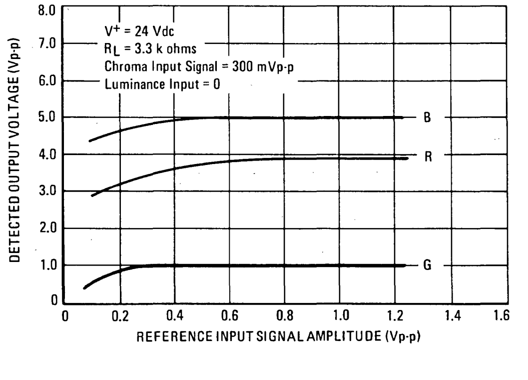


FIGURE 11 – DETECTED OUTPUT VOLTAGE
(Reference Test Circuit of Figure 4)



TYPICAL CHARACTERISTICS (continued)
(T_A = +25°C unless otherwise noted)

(Figures 12 through Figure 17 Reference Test Circuit of Figure 4)

FIGURE 12 – OUTPUT VOLTAGE

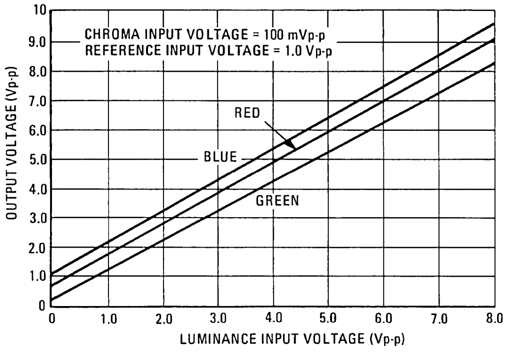


FIGURE 13 – GREEN OUTPUT

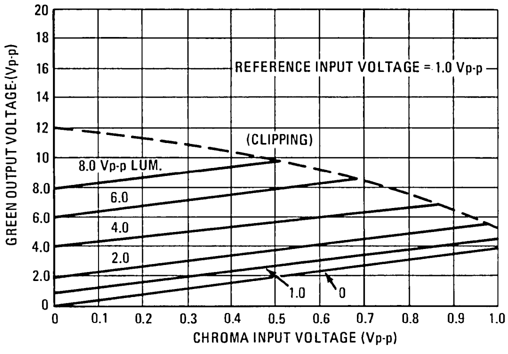


FIGURE 14 – RED OUTPUT

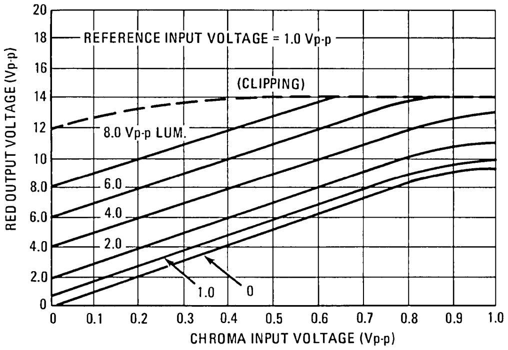


FIGURE 15 – BLUE OUTPUT

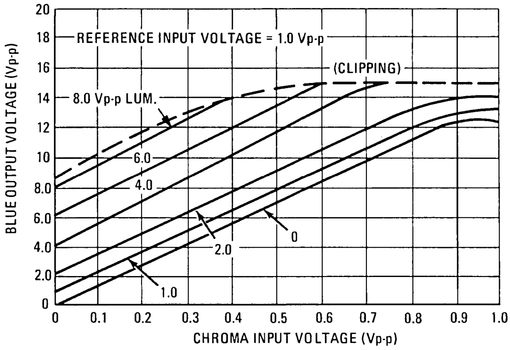


FIGURE 16 – LUMINANCE BANDWIDTH

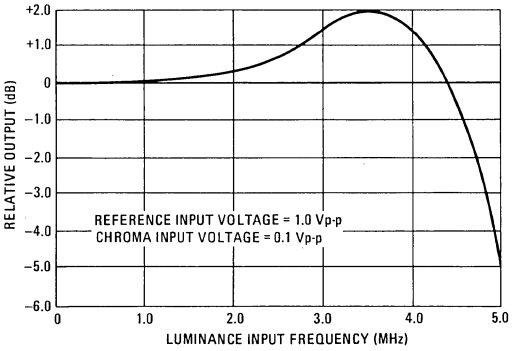
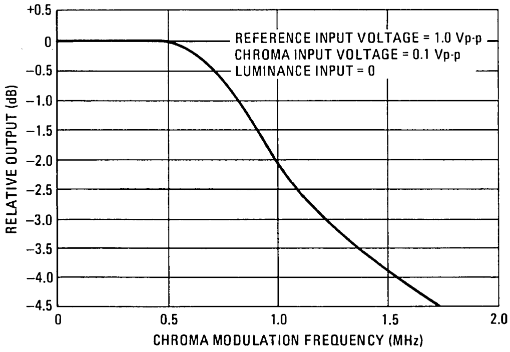


FIGURE 17 – CHROMA BANDWIDTH



6

MC1328

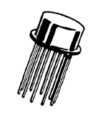
DUAL CHROMA DEMODULATOR

MONOLITHIC DUAL DOUBLY BALANCED CHROMA DEMODULATOR

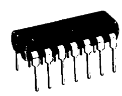
- Good Chroma Sensitivity (0.3 Vp-p Input Produces 5.0 Vp-p Output)
- Good dc Temperature Stability (3 mV/°C typ)
- Low Output dc Offset Voltages (0.6 V max)
- Pin Compatible with ULN-2114, ULN-2114A
- Negligible Change in Output Voltage Swing With Varying 3.58 MHz Reference Signal
- High Ripple Rejection Due To Built-In MOS Filter Capacitors
- High Output Voltage Swing (10 Vp-p Typ) – B-Y

DUAL DOUBLY BALANCED CHROMA DEMODULATOR

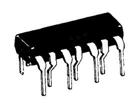
Monolithic Silicon Integrated Circuit



G SUFFIX
METAL PACKAGE
CASE 603-02
(TO-100)



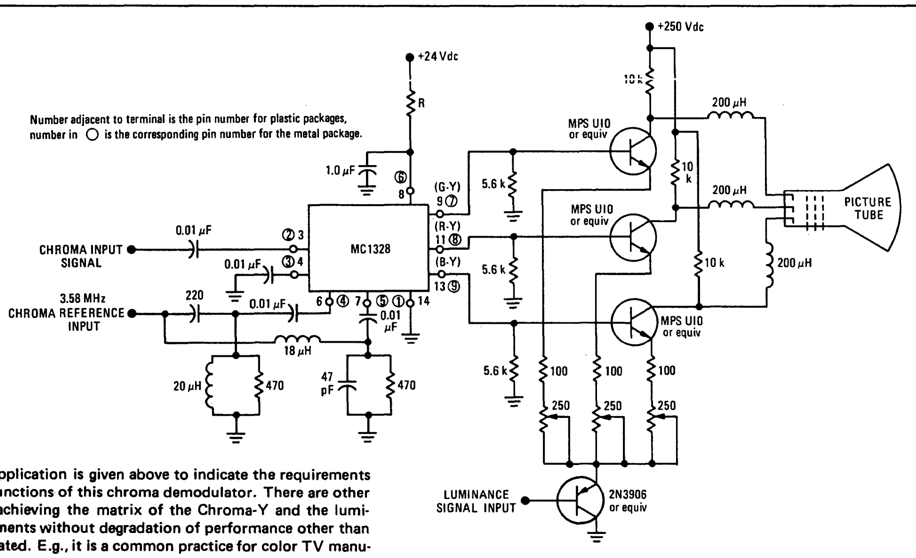
P SUFFIX
PLASTIC PACKAGE
CASE 605
(TO-116)



PQ SUFFIX
PLASTIC PACKAGE
CASE 647

6

FIGURE 1 – MC1328 TYPICAL APPLICATION



A practical application is given above to indicate the requirements and output functions of this chroma demodulator. There are other methods of achieving the matrix of the Chroma-Y and the luminance components without degradation of performance other than the one indicated. E.g., it is a common practice for color TV manufacturers to matrix in the picture tube.

See Packaging Information Section for outline dimensions.

MAXIMUM RATINGS (T_A = +25°C unless otherwise specified)

Rating	Value	Unit
Power Supply Voltage	30	Vdc
Power Dissipation (Package Limitation) Plastic Packages Derate above T_A = +25°C Metal Package Derate above T_A = +25°C	 625 5.0 680 4.5	 mW mW/°C mW mW/°C
Chroma Signal Input Voltage	5.0	Vpk
Reference Signal Input Voltage	5.0	Vpk
Minimum Load Resistance	3.0	k ohms
Operating Temperature Range (Ambient)	0 to +75	°C
Storage Temperature Range	-65 to +150	°C

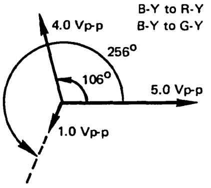
Maximum Ratings as defined in MIL-S-19500, Appendix A.

ELECTRICAL CHARACTERISTICS (V^+ = 24 Vdc, R_L = 3.3 k ohms, Reference Input Voltage = 1.0 Vp-p, T_A = +25°C unless otherwise noted)

STATIC CHARACTERISTICS

Characteristic	Pin No. Suffix G Pkg	Pin No. Suffix P, PQ Pkgs	Min	Typ	Max	Unit
Quiescent Output Voltage See Figure 2	7,8,9	9,11,13	13	14.3	16	Vdc
Quiescent Input Current (See Figure 2) (R_L = ∞, Chroma and Reference Input Voltages = 0) (R_L = 3.3 k ohms, Chroma and Reference Input Voltages = 0)	6	8	– 16.5	6.0 19	– 25.5	mA
Reference Input DC Voltage	4,5	6,7	–	6.2	–	Vdc
Chroma Input DC Voltage	2,3	3,4	–	3.4	–	Vdc
Differential Output Voltage See Note 1 and Figure 3	7,8,9	9,11,13	–	0.3	0.6	Vdc
Output Temperature Coefficient (No Output Differential Voltage > 0.6 Vdc, +25°C to +65°C) See Note 1 and Figure 3	7,8,9	9,11,13	–	3.0	–	mV/°C

DYNAMIC CHARACTERISTICS (V^+ = 24 Vdc, R_L = 3.3 k ohms, Referenced Input Voltage = 1.0 Vp-p, T_A = +25°C unless otherwise noted)

Characteristic	Pin No. Suffix G Pkg	Pin No. Suffix P, PQ Pkgs	Min	Typ	Max	Unit
Detected Output Voltage (B-Y) See Note 2	9	13	8.0	9.0	–	Vp-p
Chroma Input Voltage (B-Y Output = 5.0 Vp-p) See Note 3	2	3	–	0.3	0.7	Vp-p
Detected Output Voltage (Adjust B-Y Output to 5.0 Vp-p) See Note 4 G-Y R-Y	 7 8	 9 11	 0.75 3.5	 1.0 3.8	 1.25 4.2	Vp-p
Relative Output Phase (B-Y Output = 5.0 Vp-p) B-Y to R-Y B-Y to G-Y 	 9-8 9-7	 13-11 13-9	 101 248	 106 256	 111 264	Degrees
Demodulator Unbalance Voltage (no Chroma Input Voltage and normal Reference Signal Input Voltage)	7,8,9	9,11,13	–	250	500	mVp-p
B-Y Phase Shift (B-Y Reference Input to B-Y Output)	5-9	7-13	–	3	–	Degrees
Residual Carrier and Harmonics (with Input Signal Voltage, normal Reference Signal Voltage and B-Y = 5.0 Vp-p)	7,8,9	9,11,13	–	–	1.5	Vp-p
Reference Input Resistance (Chroma Input = 0)	4,5	6,7	–	2.0	–	k ohms
Reference Input Capacitance (Chroma Input = 0)	4,5	6,7	–	6.0	–	pF
Chroma Input Resistance	2,3	3,4	–	2.0	–	k ohms
Chroma Input Capacitance	2,3	3,4	–	2.0	–	pF

NOTES:

1. With Chroma Input Signal Voltage = 0 and normal Reference Input Signal Voltage (1.0 Vp-p), all output voltages will be within specified limits and will not differ from each other by greater than 0.6 Vdc.
2. With normal Reference Input Signal Voltage, adjust Chroma Input Signal Voltage to 0.6 Vp-p.
3. With normal Reference Input Signal Voltage, adjust Chroma Input Signal Voltage until the B-Y Output Voltage = 5 Vp-p. The Chroma Input Voltage at this point should be equal to or less than 0.7 Vp-p.
4. With normal Reference Input Signal Voltage, adjust the Chroma Input Signal until the B-Y Output Voltage = 5 Vp-p. At this point, the R-Y and G-Y voltages will fall within the specified limits.

TEST CIRCUITS

(V^+ = 24 Vdc, R_L = 3.3 kΩ, T_A = +25°C unless otherwise noted)

FIGURE 2 – TEST CIRCUIT WITH NO REFERENCE INPUT SIGNAL

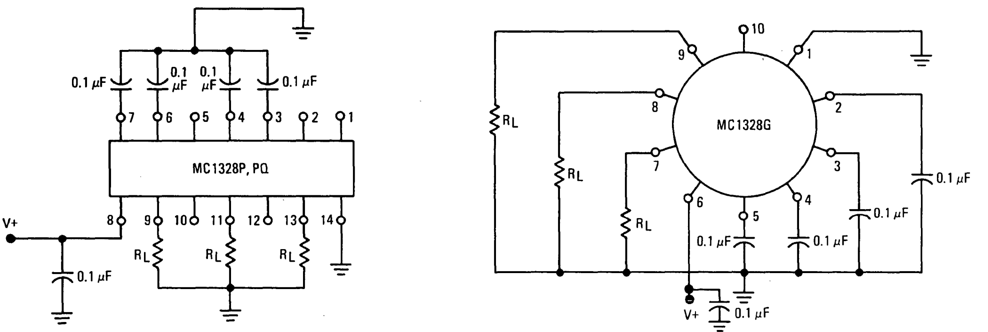
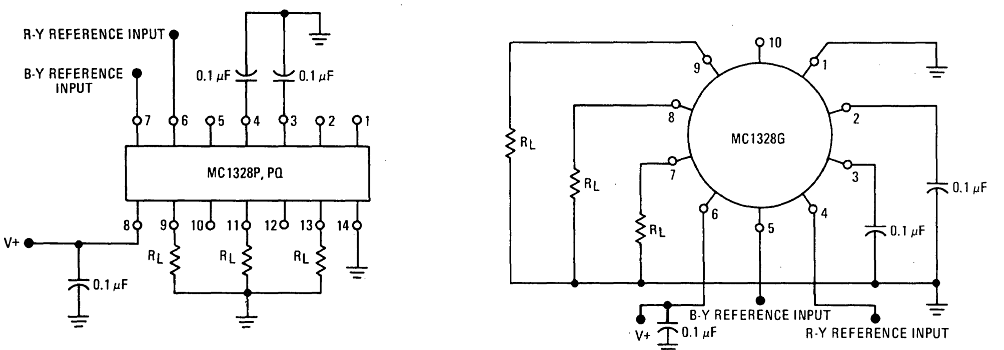


FIGURE 3 – TEST CIRCUIT WITH REFERENCE INPUT SIGNAL

(Quiescent Current, DC Output Voltage, Difference Voltage)



TYPICAL CHARACTERISTICS

FIGURE 4 – DETECTED OUTPUT

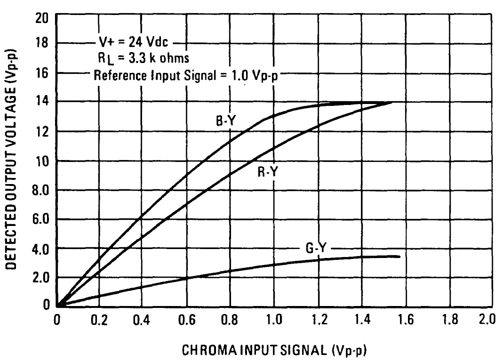
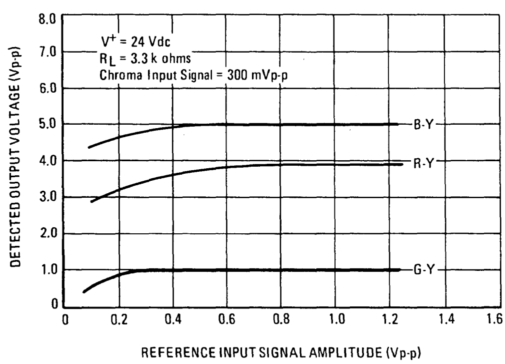


FIGURE 5 – DETECTED OUTPUT



TYPICAL CHARACTERISTICS (continued)

FIGURE 6 – DETECTED OUTPUT VOLTAGE

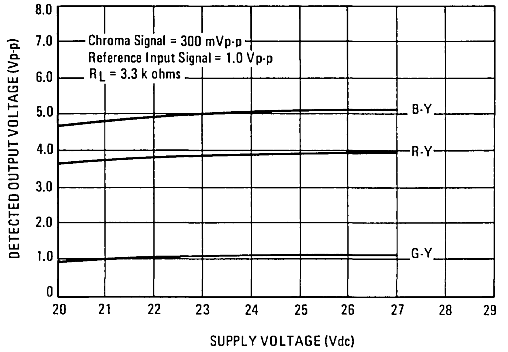


FIGURE 7 – DC OUTPUT VOLTAGE

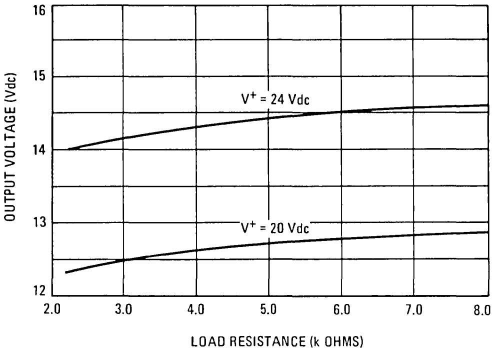


FIGURE 8 – DC OUTPUT VOLTAGE

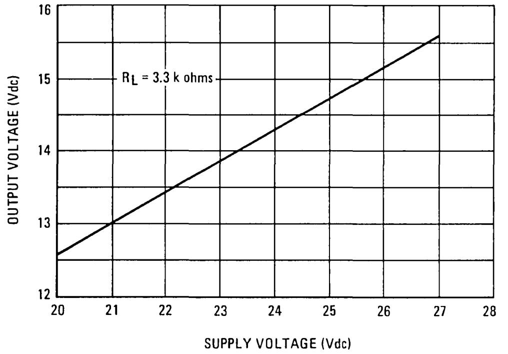


FIGURE 9 – POWER DISSIPATION

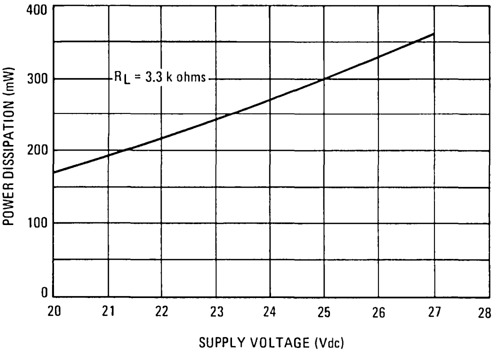


FIGURE 10 – POWER DISSIPATION

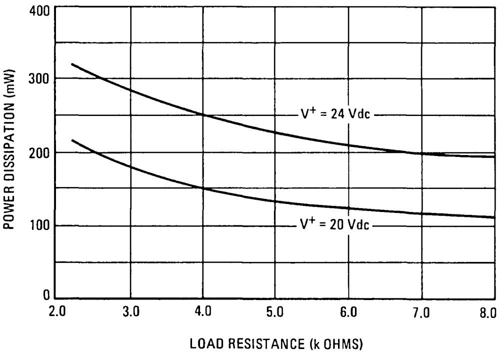
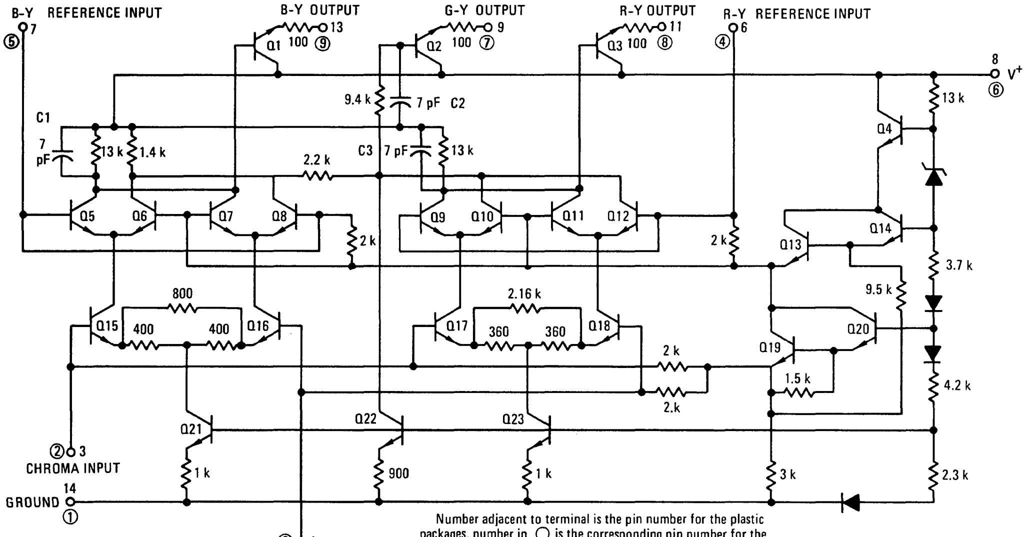


FIGURE 11 – CIRCUIT SCHEMATIC



6

CIRCUIT OPERATION

A double sideband suppressed carrier chroma signal flows between the bases of the two differential pairs, Q15 and Q16, Q17 and Q18. A reference signal of approximately 1 Vp-p amplitude having the same frequency as the suppressed chroma carrier with an appropriate phase relationship is supplied between the bases of the upper differential pairs Q5 and Q6, Q7 and Q8, Q9 and Q10, Q11 and Q12. The upper pairs are switched between full conduction and zero conduction at the carrier frequency rate. The collectors of the upper pairs are cross-coupled so that "doubly balanced" or "full-wave" synchronous detected chroma signals are obtained. Both positive and negative phases of the detected signal are available at opposite collector pairs.

Capacitors C1, C2 and C3 provide filtering of carrier harmonics from the detected color difference signals. This increases the available swing before clipping for the color difference signal, and reduces the high frequency components which must pass through the emitter followers (Q1, Q2, Q3) into the video output stages. Since high capacitance (>100 pF) is characteristic of the input impedance of a video output stage, the transistor emitter followers must operate at a high quiescent current (>5 mA) in order to pass large high frequency components without distortion. The filtering reduces the quiescent current required in the emitter followers and thus reduces dissipation in the integrated circuit.

MC1330P

VIDEO DETECTOR

MONOLITHIC LOW-LEVEL VIDEO DETECTOR

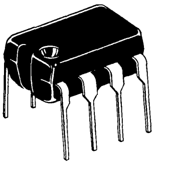
. . . an integrated circuit featuring very linear video characteristics, wide bandwidth. Designed for color and monochrome television receivers, replacing the third IF, detector, video buffer and the AFC buffer.

- Conversion Gain – 34 dB typ
- Video Frequency Response @ 6.0 MHz < 1.0 dB
- Input of 36 mV Produces 3.0 Vp-p Output
- High Video Output – 7.7 Vp-p
- Fully Balanced Detector
- High Rejection of IF Carrier
- Low Radiation of Spurious Frequencies

LOW-LEVEL VIDEO DETECTOR

MONOLITHIC SILICON

INTEGRATED CIRCUIT



PLASTIC PACKAGE
CASE 626

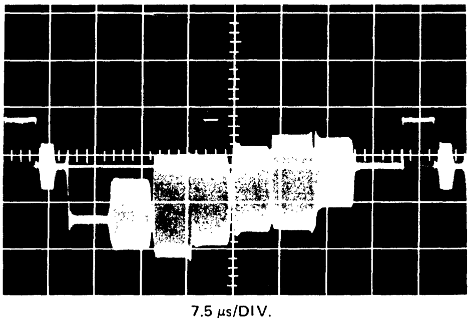
MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Value	Unit
Power Supply Voltage	+24	Vdc
Supply Current	26	mAdc
Input Voltage	1.0	V(rms)
Power Dissipation (Package Limitation) T_A = +25°C Derate above T_A = +25°C	 625 5.0	 mW mW/°C
Operating Temperature Range (Ambient)	0 to +75	°C
Storage Temperature Range	-65 to +150	°C

Maximum Ratings as defined in MIL-S-19500, Appendix A.

FIGURE 1 – DETECTED COLOR BARS

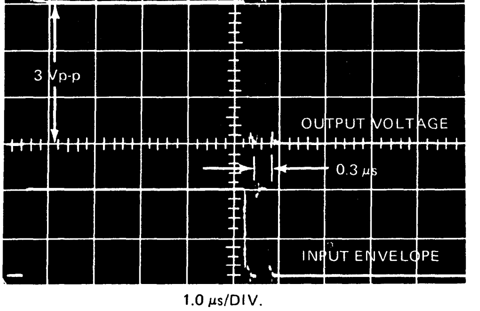
1.0 V/DIV.



7.5 µs/DIV.

FIGURE 2 – PULSE RESPONSE

1.0 V/DIV.



1.0 µs/DIV.

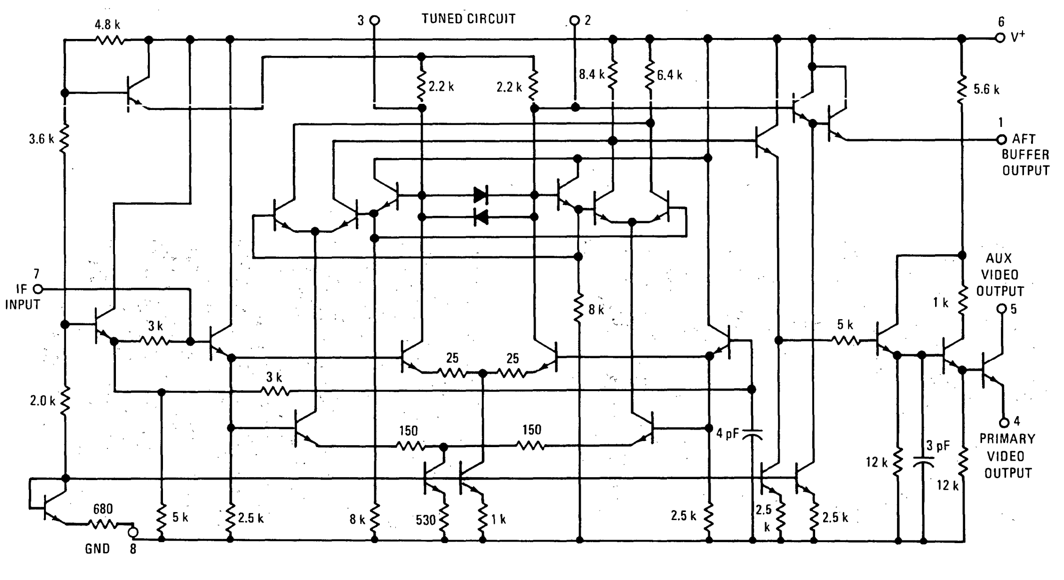
See Packaging Information Section for outline dimensions.

ELECTRICAL CHARACTERISTICS (V^+ = 20 Vdc, Q = 30, f_C = 45 MHz, T_A = +25°C unless otherwise noted.)

Characteristic	Pin	Min	Typ	Max	Unit
Supply Voltage Range	6	12	20	24	Vdc
Supply Current	5,6	–	15	–	mA
Zero Signal dc Output Voltage	4	6.8	7.7	8.3	Vdc
Maximum Signal dc Output Voltage	4	–	0	–	Vdc
Input Signal Voltage for 3.0 Vp-p Video Output (90% Modulation)	7	–	36	–	mV(rms)
Maximum Output Voltage Swing	4	–	7.7	–	Vp-p
Carrier Rejection at Output	4	42	60	–	dB
Carrier Output Voltage (at 3.0 Vp-p output) $f_{out} = f_C$ $f_{out} = 2 f_C$		 – –	 1.0 3.0	 – –	mV(rms)
3.0 dB Bandwidth of IF Carrier	7	–	80	–	MHz
3.0 dB Bandwidth of Video Output	4	–	12.3	–	MHz
Input Resistance Input Capacitance	7	– –	3.5 3.0	– –	kilohms pF
Output Resistance	4	–	180	–	ohms
Internal Resistance } (across tuned circuit) Internal Capacitance }	2,3	– –	4.4 1.0	– –	kilohms pF
AFT Buffer Output at Carrier Frequency ①	1	–	350	–	mVp-p
AFT Buffer dc Level	1	–	6.5	–	Vdc

① Measured with 10 times probe.

FIGURE 3 – CIRCUIT SCHEMATIC



TYPICAL CHARACTERISTICS

(T_A = +25°C unless otherwise noted)

FIGURE 4 – TEST CIRCUIT

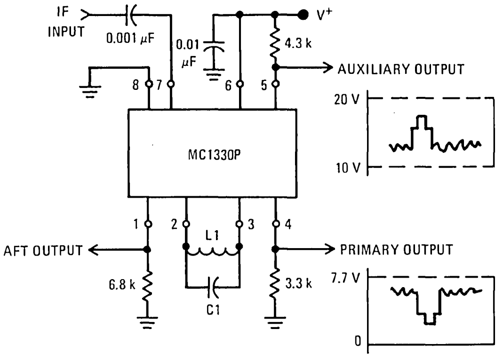


FIGURE 5 – OUTPUT VOLTAGE

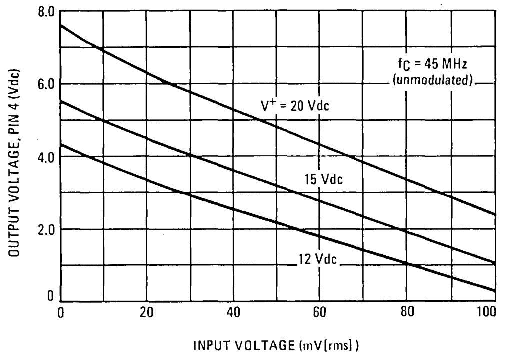


FIGURE 6 – OUTPUT VOLTAGE

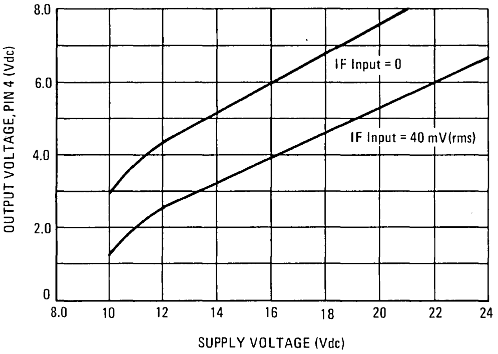


FIGURE 7 – DETECTOR LINEARITY

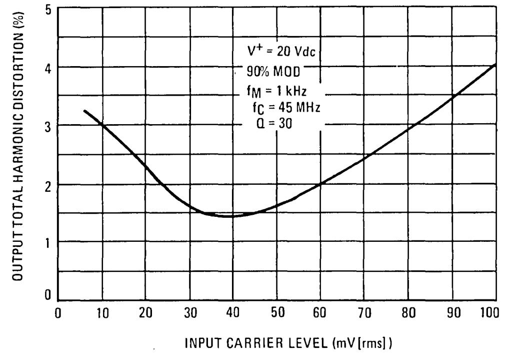


FIGURE 8 – VIDEO FREQUENCY RESPONSE

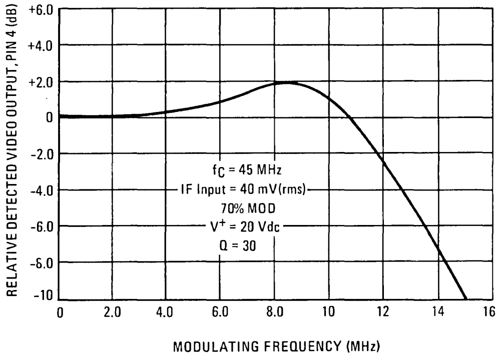
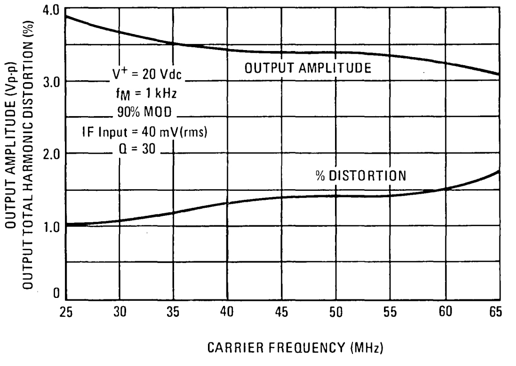
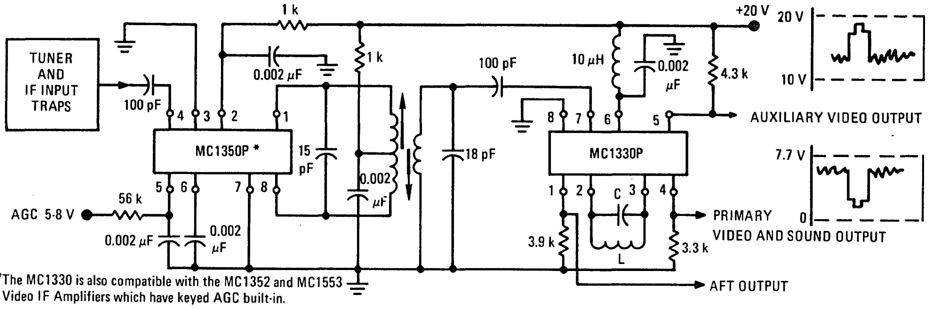


FIGURE 9 – CARRIER FREQUENCY PERFORMANCE



APPLICATIONS INFORMATION

FIGURE 10 – COLOR IF AMPLIFIER TYPICAL APPLICATION

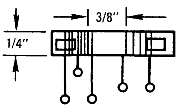


*The MC1330 is also compatible with the MC1352 and MC1553 Video IF Amplifiers which have keyed AGC built-in.

TV-IF Amplifier Information

A very compact high performance IF amplifier constructed as shown in Figure 11 minimizes the number of overall components and alignment adjustments. It can be readily combined with normal tuners and input tuning-trapping circuitry to provide the performance demanded of high quality receivers. This configuration will provide approximately 84 dB voltage gain and can accomodate the usual low impedance input network or, if desired, can take advantage of an impedance step-up from tuner to MC1350P input ($Z_{in} \approx 7.0$ kilohms). The burden of selectivity, formerly found between the third IF and detector, must now be placed at the interstage. The nominal 3 volt peak-to-peak output can be varied from 0 to 7.0 V with excellent linearity and freedom from spurious output products.

FIGURE 11 – TRANSFORMER



Primary Winding: 8 turns of AWG #26 close wound, CT
Secondary Winding: 6 turns of AWG #26 close wound, CT
Core: Arnold Type TH slugs or equiv.

Alignment is most easily accomplished with an AM generator, set at a carrier frequency of 45.75 MHz, modulated with a video frequency sweep. This provides the proper realistic conditions necessary to operate the low-level detector (LLD). The detector tank is first adjusted for maximum detected dc (with a CW input), next, the video sweep modulation is applied and the interstage and input circuits aligned, step by step, as in a standard IF amplifier.

Note: A normal IF sweep generator, essentially an FM generator, will not serve properly without modification. The LLD tank attempts to "follow" the sweep input frequency, and results in variations of switching amplitude in the detector. Hence, the apparent overall response becomes modified by the response of the LLD tank, which a real signal doesn't do.
This effect can be prevented by resistively adding a 45.75 MHz CW signal to the output of the sweep generator approximately 3 dB greater than the sweep amplitude.

MC1330P General Information

The MC1330P offers the designer a new approach to an old problem. Now linear detection can be performed at much lower power signal levels than possible with a detector diode.
Offering a number of distinct advantages, its easy implementation should meet with ready acceptance for television designs. Some specific features and information on systems design with this device are given below:
1. The device provides excellent linearity of output versus input, as shown in Figure 6. This graph also shows that video peak-to-peak amplitude (ac) does not change with supply voltage variation. (Slopes are parallel. Visualize a given variation of input CW and use the figure as a transfer function.)
2. The dc output level does change linearly with supply voltage. This can be accommodated by regulating the supply or by referencing the subsequent video amplifier to the same power supply.
3. The choice of Q for the tuned circuit of pins 2 and 3 is not critical. The higher the Q, the better the rejection of 920 kHz products but the more critical the tuning accuracy required. Values of Q from 20 to 50 are recommended. (Note the internal resistance.)
4. A video output with positive-going sync is available at pin 5 if required. This signal has a higher output impedance than pin 4 so it must be handled with greater care. If not used, pin 5 may be connected directly to the supply voltage (pin 6).
5. An AFT output (pin 1) provides 350 mV of clipped carrier output, sufficient voltage to drive an AFT ratio detector, with only one additional stage.

MC1335P

TUNING INDICATOR

FM RADIO OR COLOR TV TUNING INDICATOR

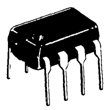
. . . a monolithic circuit designed to function as a tuning indicator for FM radios and a fine tuning indicator for color TV sets.

TYPICAL FEATURES INCLUDE:

- Very sharp positive tuning to eliminate error
- Cost and space saving over conventional tuning meters
- Low standby current – 5.5 mA typical

FM RADIO OR COLOR TV TUNING INDICATOR

MONOLITHIC SILICON EPITAXIAL PASSIVATED

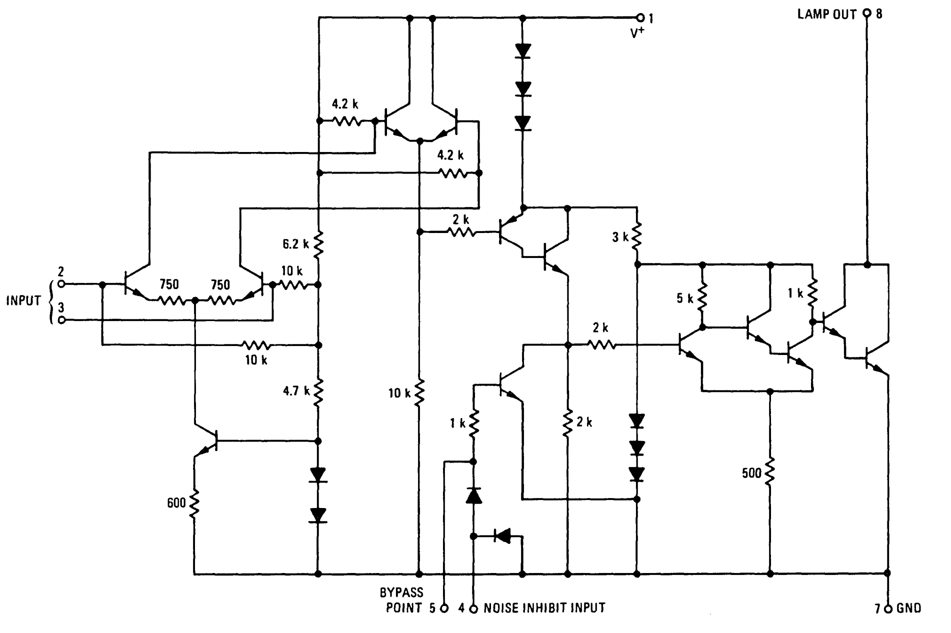


PLASTIC PACKAGE
CASE 626

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+	20	Vdc
Maximum Current to Pin 8	$I_{8(max)}$	40	mA
Power Dissipation (Package Limitation)	P_D	625	mW
Derate above T_A = +25°C	$1/\theta_{JA}$	5.0	mW/°C
Operating Temperature Range	T_A	0 to +75	°C

FIGURE 1 – CIRCUIT SCHEMATIC



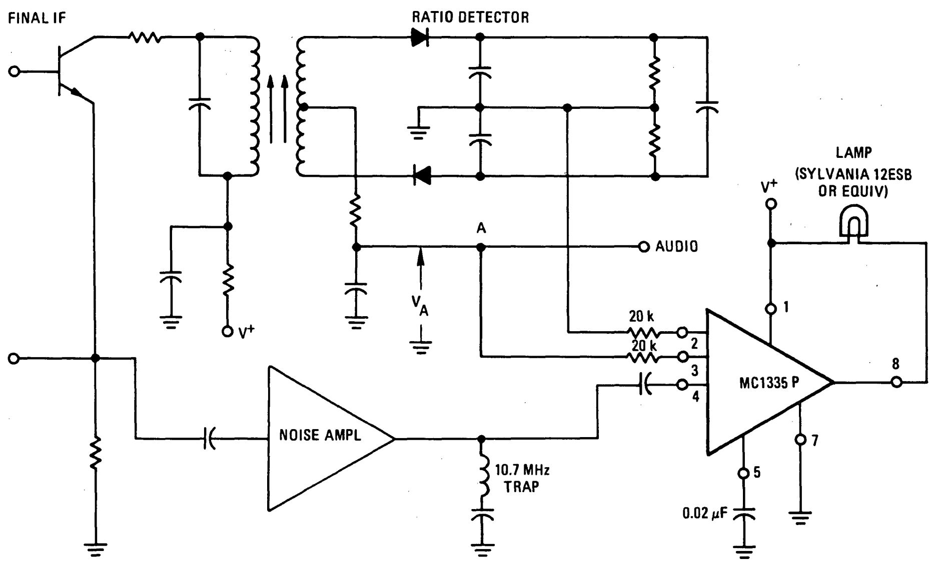
See Packaging Information Section for outline dimensions.

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted, V^+ = 12 V)

Characteristic	Symbol	Min	Typ	Max	Unit
Drain Current (Lamp Off)	I_D	4.0	5.5	8.0	mA
Saturation Voltage	V_{sat}	–	0.85	1.3	Vdc
Noise Inhibit (Lamp Off*)	NI	1.7	1.9	–	Vdc
Threshold (See Figure 2)	V_A				Vdc
Lamp On		≥5.8	–	≤6.2	
Lamp Off		≤5.1	–	≥6.9	

*Applied to pin 4

FIGURE 2 – TYPICAL FM RADIO TUNING INDICATOR APPLICATION



APPLICATIONS INFORMATION

The MC1335P is used to light a lamp when an FM receiver is correctly tuned. The three conditions of receiver operation that determine the response of the MC1335P indicator lamp are:

1. Lamp "ON" – The voltage developed at the input (Pins 2 and 3) is equal when the receiver is correctly tuned to the center of the incoming station.
2. Lamp "OFF" – Unequal voltages are present at the input (Pins 2 and 3); the receiver is not tuned correctly to the center of the incoming signal.
3. Lamp "EXTINGUISHED" – Noise voltage is supplied from the IF amplifier to the noise inhibitor (Pin 4) when the receiver is not tuned to a station and only noise is present at the receiver output.

Note: Voltages to satisfy conditions 1 and 2 are normally available from discriminator and ratio detector circuits. To satisfy condition 3, a noise amplifier normally is used, (See Figure 2).

6

MC1345P

TV SIGNAL PROCESSOR

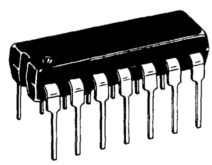
TV SIGNAL PROCESSOR

. . . a monolithic TV circuit with sync separator, advanced noise inversion, AGC comparator, and versatile RF AGC delay amplifier for use in color or monochrome TV receivers.

- Video Internally Delayed for Total Noise Inversion
- Low Impedance, Noise Cancelled Sync Output
- Refined AGC Gate
- Small IF AGC Output Change During RF AGC Interval
- Positive and Negative Going RF AGC Outputs
- Noise Threshold May Be Externally Adjusted
- Time Constants for Sync Separator Externally Chosen
- Stabilized for ±10% Supply Variations

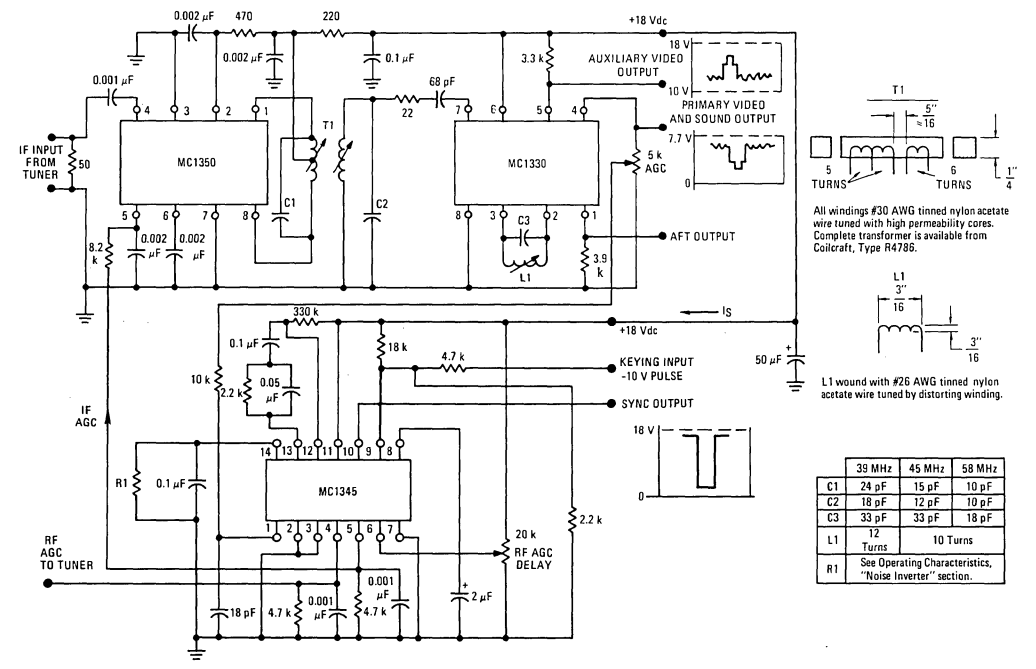
TV SIGNAL PROCESSOR

MONOLITHIC SILICON INTEGRATED CIRCUIT



PLASTIC PACKAGE
CASE 605
TO-116

FIGURE 1 – TYPICAL MC1345 APPLICATION WITH VIDEO IF AMPLIFIER



	39 MHz	45 MHz	58 MHz
C1	24 pF	15 pF	10 pF
C2	18 pF	12 pF	10 pF
C3	33 pF	33 pF	18 pF
L1	12 Turns	10 Turns	
R1	See Operating Characteristics, "Noise Inverter" section.		

See Packaging Information Section for outline dimensions.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Value	Unit
Power Supply Voltage (Pin 11)	+22	Vdc
Video Input Voltage (Pin 1)	+10	Vdc
Negative RF AGC Supply Voltage (Pin 3)	-10	Vdc
Gating Voltage (Pin 9)	15	Vp-p
Sync Separator Drive Voltage (Pin 12)	7.0	Vp-p
Power Dissipation (Package Limitation) Plastic Package Derate above T_A = +25°C	 625 5.0	 mW mW/°C
Operating Temperature Range (Ambient)	0 to +70	°C
Storage Temperature Range	-55 to +150	°C

Maximum Ratings as defined in MIL-S-19500, Appendix A.

ELECTRICAL CHARACTERISTICS (V^+ = +18 Vdc, T_A = +25°C unless otherwise noted)

Characteristic	Min	Typ	Max	Unit
Sync Tip dc Level of Input Signal	3.6	3.9	4.2	Vdc
Temperature Coefficient of Sync Tip (Input)	0	-1.3	-2.5	mV/°C
Sync Output Amplitude	–	16	–	Vp-p
Sync Output Impedance	–	–	100	Ohms
Sync Tip to Noise Threshold Separation (Input)	0.45	0.7	0.95	Vdc
IF AGC Voltage Change During RF Interval	–	0.10	0.5	Vdc
Peak AGC Charge Current	–	15	–	mAdc
Peak AGC Discharge Current	–	0.9	–	mAdc
IF AGC Voltage Range (See Figures 2 and 3)	9.0	–	–	Vdc
Positive RF AGC Voltage Range	–	10	–	Vdc
Positive RF AGC Minimum Voltage	0.5	1.5	2.0	Vdc
Negative RF AGC Voltage Range	–	10	–	Vdc
Negative RF AGC Maximum Voltage	9.5	10.5	11.5	Vdc
Total Supply Current, I_S (Circuit of Figure 1)	–	26	–	mAdc

FIGURE 2 – TEST CIRCUIT FOR AGC AMPLIFIER MEASUREMENTS

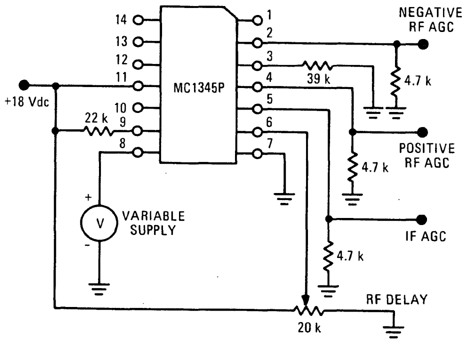
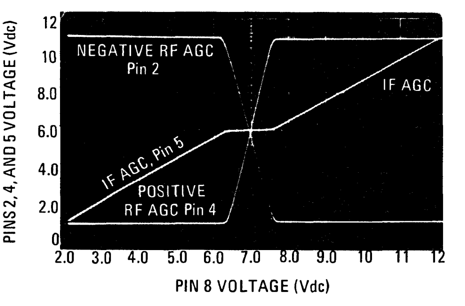
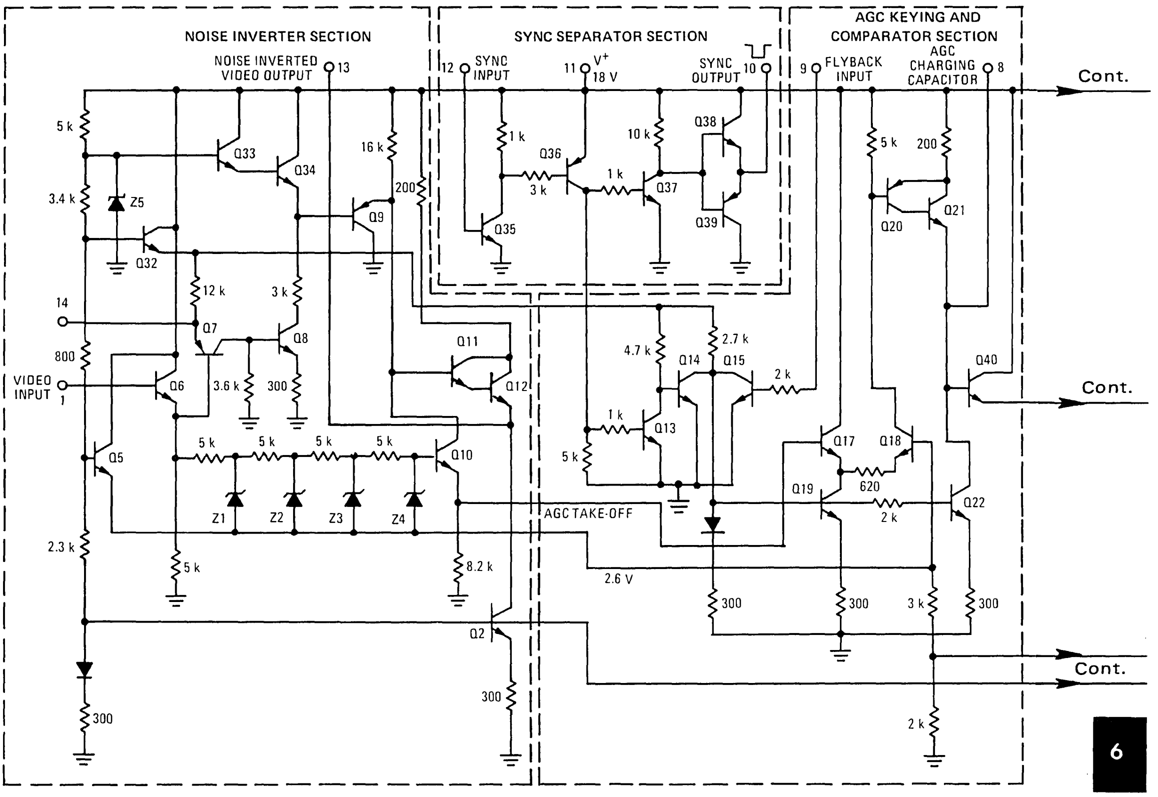


FIGURE 3 – AGC AMPLIFIER RESPONSE



6

FIGURE 4 – CIRCUIT SCHEMATIC



6

OPERATING CHARACTERISTICS

NOISE INVERTER

A composite video signal of from 1 to 3 volts peak-to-peak amplitude with negative-going sync, superimposed on a positive dc offset voltage, is required at the input, pin 1. The amplitude of the dc offset voltage will determine the allowable magnitude of the video input, since the sync tip will always be clamped at 3.9 V. See Figure 5.

The noise threshold is set by Q7's emitter voltage determined by Q32 and the bias-chain Zener diode. The resulting dc level (or noise threshold) may be lowered by adding an external resistor, R1 (Figure 1), connected from pin 14 to ground. With this arrangement, the lowered threshold would be given by:

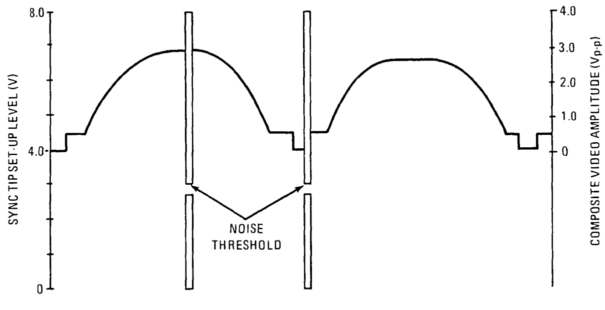
$$V = \frac{R1\ V_n}{R1 + 12{,}000\ \Omega}$$

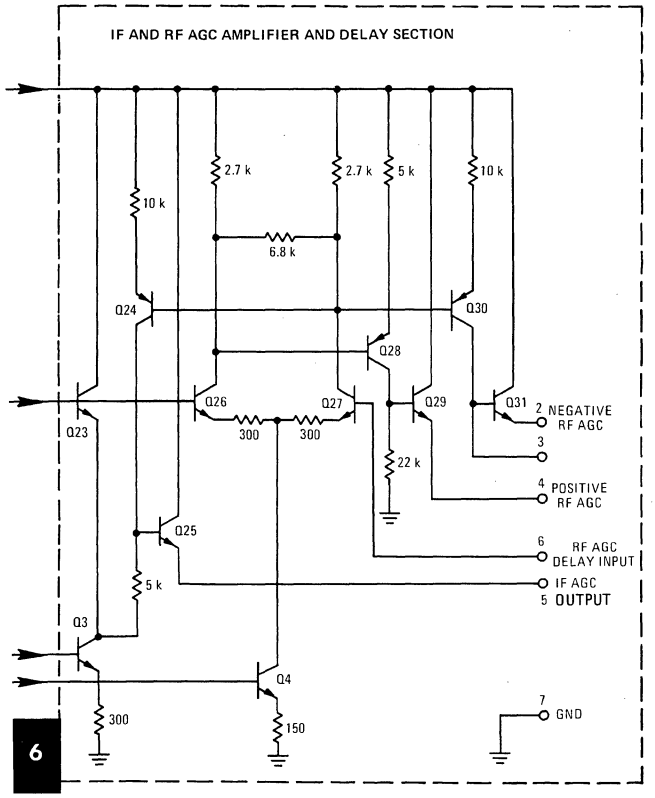
where V_n = noise threshold without R1 connected.

The noise threshold can also be raised to the same degree by connecting R1 from pin 14 to the supply voltage level. However, in this case, care should be exercised to insure that the resulting voltage appearing at pin 14 does not exceed the sync threshold (approximately 3.9 V).

Noise inversion is achieved as follows: first the composite input signal is impedance-buffered by the Q6 emitter-follower. Then,

FIGURE 5





the buffered signal is fed to Q10's base through an RC delay line (Z1 – Z4). Finally the signal appears, inverted and delayed by approximately 300 ns, at the base of Q11.

If an interference pulse occurs, with an amplitude enough above the sync tip level to reach the noise threshold, the pulse will drive the emitter of Q6 below its pre-set level. Q7 will conduct, and charge from the external capacitor connected to pin 14 will pass through Q7, turning on both Q8 and Q9. When Q9 is on, Q11's base is grounded, blanking the output of Q10's collector.

The video signal with the interfering noise cancelled, emerges at pin 13. Polarity is inverted, so the sync pulses are positive-going.

Blanking commences before the interference pulse itself emerges from the delay line, and the blanking action persists for a short time interval after the end of the noise pulse, due to energy stored in Q9's junction.

For very long noise pulses, the rate of discharge of the external capacitor sets the end of the blanking interval. In such a case, blanking could extend over several horizontal line-sweep periods, depending on the capacitor value used. The external capacitor is typically 0.1 μF, and this value allows continuous cancellation for approximately 4 line-sweep intervals.

Under weak signal conditions, high frequency noise from thermal or tropospheric sources is common. To prevent this type of interference from spuriously triggering the inverter, some RC filtering is required between the video detector and the video input at pin 1. For this filter, RC values of 10 kΩ and 18 pF are typical.

SYNC SEPARATOR

The noise-inverted video output at pin 13 is passed through an external RC filter network, to the sync separator input at pin 12, cutting off Q35, Q36, and Q37, except during the positive sync tips. Time constants for the filter are a matter of the designer's preference, and are chosen as for discrete-circuit sync separators.

Operation of the sync separator is as follows. Q35 conducts only during the positive-going sync pulse. Q36 amplifies and inverts the sync pulse, driving Q37 into saturation during the sync pulse interval. The output of Q37 drives the complementary pair, Q38/Q39, which yield a low output impedance negative-going sync pulse of greater than 15 V peak-to-peak amplitude. It should be noted that the first sync pulse occurring after noise inversion ends, will be slightly longer in duration than other sync pulses. Typical resistance and capacitance values for the RC sync input network are given in Figure 6A.

FIGURE 6A – NORMAL SYNC SEPARATION NETWORK

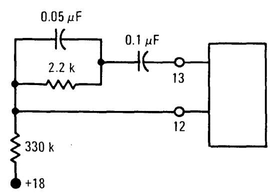
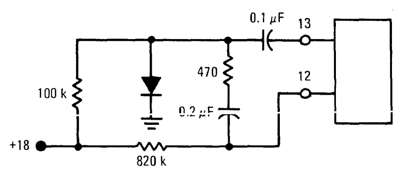


FIGURE 6B – ALTERNATE DIODE SYNC SEPARATION NETWORK



An alternate input network is shown in Figure 6B, it uses a diode to separate the sync pulses. In this case the pulses will be clamped to +0.7 V above ground. As a result, Q35 and the transistors following it serve as over-driven amplifiers.

KEYER AND COMPARATOR

The AGC system is internally connected to the video input at Q10's emitter. The sync signal at Q36 is internally connected to the AGC sync keyer which consists of Q13 and Q14. An externally-derived negative-going flyback pulse ($\simeq$ 12 V peak-to-peak) is applied to Q15 for flyback keying the AGC. Since the detected video output level is sampled only when the sync pulse and the flyback pulse are coincident, true keyed AGC action occurs.

An AGC comparator is formed by Q17 and Q18. The base of Q18 is connected to a fixed reference of 2.6 V. The base of Q17 is connected to the emitter of Q10, where the video signal has negative-going sync pulses. The emitters of both devices are supplied from a gated current source, Q19. This current source conducts only when Q14 and Q15 are simultaneously switched off. To do this, a positive sync pulse is required on the base of Q13, coincident with a negative flyback pulse on the base of Q15 (pin 9).

If the video signal at the emitter of Q10 increases in amplitude, the sync pulse becomes more negative. Thus, when Q19 is gated on, Q18 conducts and turns on both Q20 and Q21, which charge the external AGC filter capacitor connected at pin 8. A typical value for this capacitor is 2.0 μF.

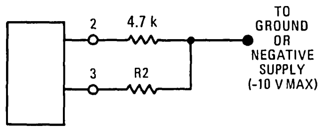
If the video signal decreases, Q18 will not conduct. However, Q22 will conduct and permit a current of 0.9 mA to flow out of the capacitor at pin 8. In effect, this "charge dumping" through Q22 promotes faster AGC action than could be attained with a conventional "charge only" system. Coupling between the charging capacitor and the AGC amplifier is through an emitter follower, Q40.

The MC1345 will operate without flyback pulses if pin 9 is grounded. However, the AGC noise immunity and aircraft flutter rejection will be impaired.

THE AGC AMPLIFIER

AGC for the IF is supplied by the emitter of Q25. The RF AGC is generated in the following way: Given a weak signal condition, Q26 is barely conducting, while Q27 passes the bulk of the current flowing from the current source, Q4. Assume that the base of Q27 is biased "on" by the RF AGC delay control connected to pin 6. The IF AGC will increase if the AGC input voltage from Q40 increases. When this latter voltage increases to a predetermined level (set by the delay control), Q26 turns on. Then, when Q26 turns on, Q27 turns off, which also turns Q24 off. As Q24 turns off, it will cancel any further increases at the base of Q25, which would come from Q23 through the 5.0 kΩ resistor. The result is that the IF AGC level is held constant during the RF AGC excursion. As Q26 is now conducting, Q28 and Q29 will also be turned on supplying the forward RF AGC voltage to pin 4. Then, when the RF AGC voltage excursion is complete, Q24 will have reached cutoff and will be unable to oppose the voltage rise at the base of Q25, thus allowing the IF AGC voltage to begin increasing.

FIGURE 7 – ALTERNATE RF AGC OUTPUT FOR FET OR TUBE TUNER



The negative RF AGC action is similar, except that Q30 and Q31 are turned off as Q28 and Q29 are turned on. The RF AGC delay, or turn-off of Q27, can be adjusted by the delay control so that it occurs at any selected point in the IF AGC range (see Figure 3).

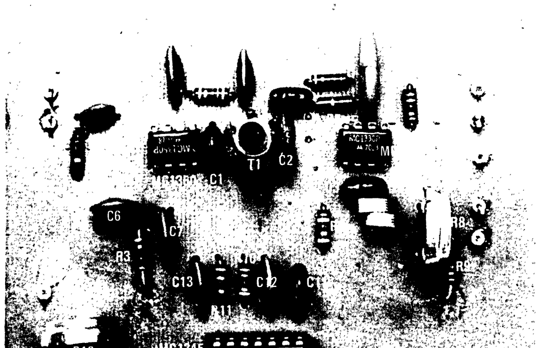
The negative AGC swing may be level-shifted by connecting the pin 2 and pin 3 resistors to a negative supply instead of to ground. The value of the pin 3 resistor, R2, for a given voltage swing, can be determined as:

$$R2 = 4000\ \Delta V$$

(See Figure 7 for component connections for negative AGC.)

All external component values given are only suggested values; the final choices will depend on the designer's preferences.

FIGURE 8 – PRINTED CIRCUIT BOARD COMPONENT LAYOUT OF IF AND JUNGLE CIRCUIT OF FIGURE 1

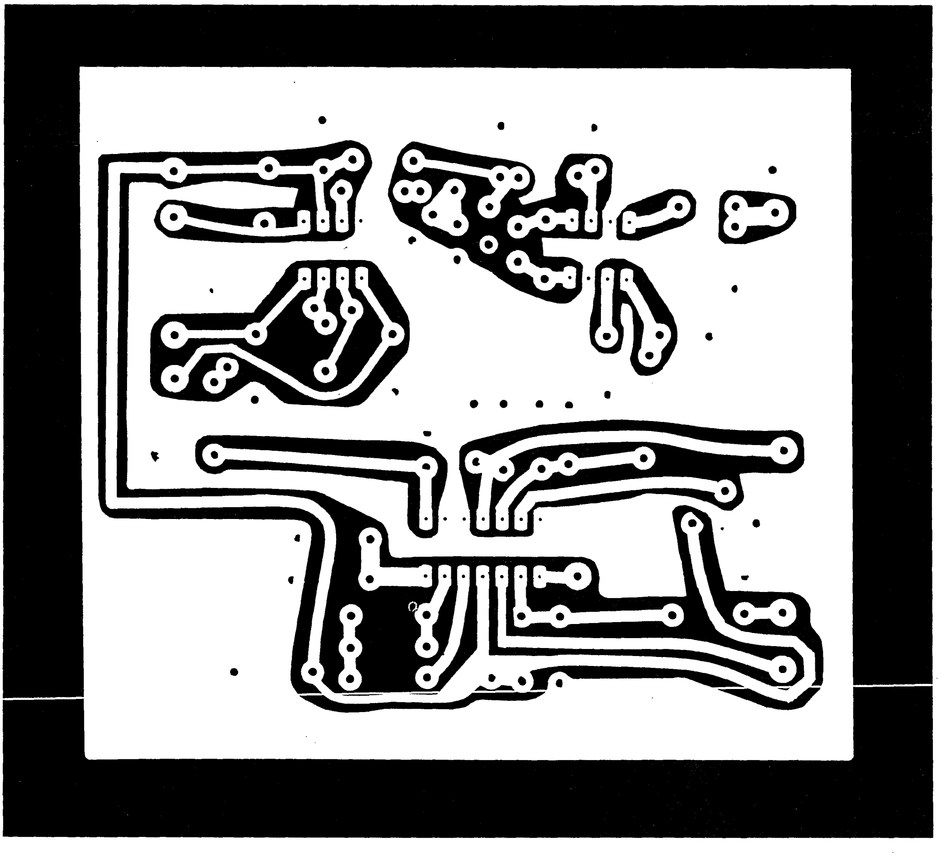


C1	See chart of Figure 1
C2	See chart of Figure 1
C3	See chart of Figure 1
C4	0.001 μF
C5	0.002 μF
C6	0.002 μF
C7	0.002 μF
C8	0.002 μF
C9	0.1 μF
C10	68 pF
C11	18 pF
C12	0.001 μF
C13	0.001 μF
C14	2 μF/10 V
C15	0.1 μF
C16	0.05 μF
C17	0.1 μF
C18	50 μF/25 V
L1	See Figure 1
T1	See Figure 1

R1	See Operating Characteristics discussion, Noise Inverter section
R2	470 ohms
R3	8200 ohms
R4	220 ohms
R5	22 ohms
R6	3300 ohms
R7	3900 ohms
R8	5 kilohm potentiometer
R9	10 kilohms
R10	4700 ohms
R11	4700 ohms
R12	2 kilohm potentiometer
R13	50 ohms
R14	2200 ohms
R15	330 kilohms
R16	18 kilohms
R17	2200 ohms
R18	4700 ohms

*See Noise Inverter Section (part can be omitted).

FIGURE 9 – PRINTED CIRCUIT BOARD
(Scale = 1:1)



SOUND IF AMPLIFIER

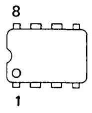
MONOLITHIC IF AMPLIFIER

. . . an integrated circuit featuring wide range AGC for use as an IF amplifier in radio and TV over the temperature range 0 to +75°C. The MC1352 is similar in design but has a keyed-AGC amplifier as an integral part of the same chip.

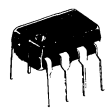
- Power Gain – 50 dB typ at 45 MHz,
  – 48 dB typ at 58 MHz
- AGC Range – 60 dB min, dc to 45 MHz
- Nearly Constant Input and Output Admittance Over the Entire AGC Range
- y_{21} Constant (-3.0 dB) to 90 MHz
- Low Reverse Transfer Admittance – << 1.0 μmho typ
- 12-Volt Operation, Single-Polarity Power Supply

IF AMPLIFIER

MONOLITHIC SILICON INTEGRATED CIRCUIT

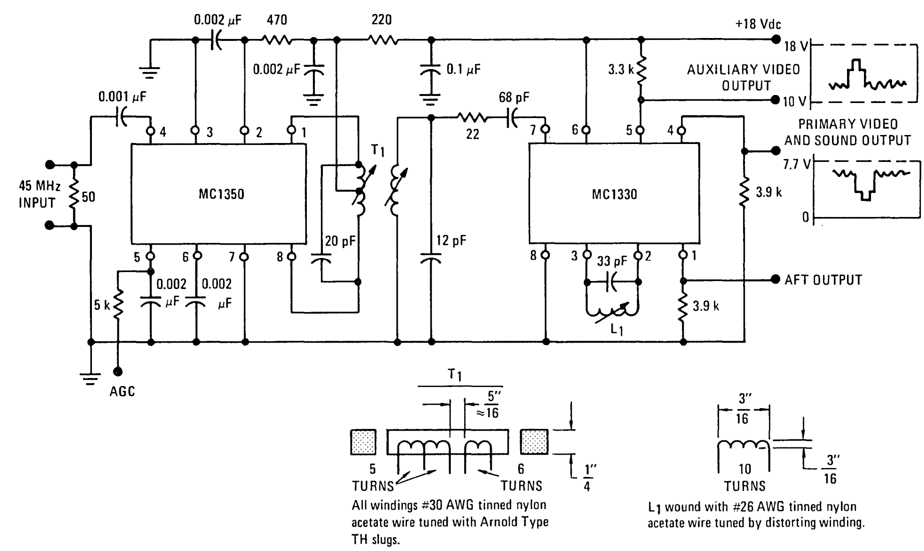


(top view)



PLASTIC PACKAGE
CASE 626

FIGURE 1 – TYPICAL MC1350 VIDEO IF AMPLIFIER and MC1330 LOW-LEVEL VIDEO DETECTOR CIRCUIT



See Packaging Information Section for outline dimensions.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+	+18	Vdc
Output Supply Voltage	V_1, V_8	+18	Vdc
AGC Supply Voltage	V_{AGC}	V^+	Vdc
Differential Input Voltage	V_{in}	5.0	Vdc
Power Dissipation (Package Limitation) Plastic Package Derate above 25°C	P_D	 625 5.0	 mW mW/°C
Operating Temperature Range	T_A	0 to +75	°C

ELECTRICAL CHARACTERISTICS (V^+ = +12 Vdc; T_A = +25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
AGC Range, 45 MHz (5.0 V to 7.0 V) (Figure 1)		60	68	–	dB
Power Gain (Pin 5 grounded via a 5.1 kΩ resistor) f = 58 MHz, BW = 4.5 MHz } See Figure 5 f = 45 MHz, BW = 4.5 MHz } f = 10.7 MHz, BW = 350 kHz } See Figure 6 f = 455 kHz, BW = 20 kHz }	A_p	 – 46 – –	 48 50 58 62	 – – – –	dB
Maximum Differential Voltage Swing 0 dB AGC –30 dB AGC	V_o	 – –	 20 8.0	 – –	V_{p-p}
Output Stage Current (Pins 1 and 8)	$I_1 + I_8$	–	5.6	–	mA
Total Supply Current (Pins 1, 2 and 8)	I_S	–	14	17	mAdc
Power Dissipation	P_D	–	168	204	mW

DESIGN PARAMETERS, Typical Values (V+ = +12 Vdc, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Frequency				Unit
		455 kHz	10.7 MHz	45 MHz	58 MHz	
Single-Ended Input Admittance	g_{11} b_{11}	0.31 0.022	0.36 0.50	0.39 2.30	0.5 2.75	mmhos
Input Admittance Variations with AGC (0 to 60 dB)	Δg_{11} Δb_{11}	– –	– –	60 0	– –	μmhos
Differential Output Admittance	g_{22} b_{22}	4.0 3.0	4.4 110	30 390	60 510	μmhos
Output Admittance Variations with AGC (0 to 60 dB)	Δg_{22} Δb_{22}	– –	– –	4.0 90	– –	μmhos
Reverse Transfer Admittance (Magnitude)	$\|y_{12}\|$	<<1.0	<<1.0	<<1.0	<<1.0	μmho
Forward Transfer Admittance Magnitude Angle (0 dB AGC) Angle (–30 dB AGC)	 $\|y_{21}\|$ $\angle y_{21}$ $\angle y_{21}$	 160 -5.0 -3.0	 160 -20 -18	 200 -80 -69	 180 -105 -90	 mmhos degrees degrees
Single-Ended Input Capacitance	C_{in}	7.2	7.2	7.4	7.6	pF
Differential Output Capacitance	C_o	1.2	1.2	1.3	1.6	pF

6

FIGURE 2 – TYPICAL GAIN REDUCTION
(Figures 5 and 6)

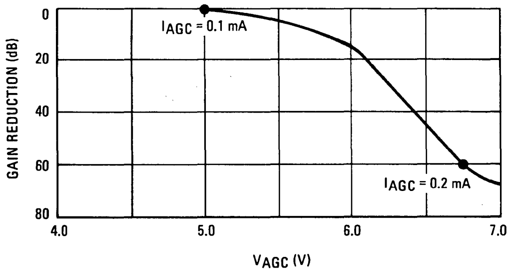
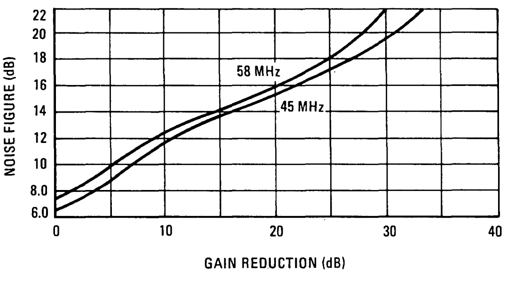


FIGURE 3 – NOISE FIGURE
(Figure 5)



GENERAL OPERATING INFORMATION

The input amplifiers (Q1 and Q2) operate at constant emitter currents so that input impedance remains independent of AGC action. Input signals may be applied single-ended or differentially (for ac) with identical results. Terminals 4 and 6 may be driven from a transformer, but a dc path from either terminal to ground is not permitted.

AGC action occurs as a result of an increasing voltage on the base of Q4 and Q5 causing these transistors to conduct more heavily thereby shunting signal current from the interstage amplifiers Q3 and Q6. The output amplifiers are supplied from an active current source to maintain constant quiescent bias thereby holding output admittance nearly constant. Collector voltage for the output amplifier must be supplied through a center-tapped tuning coil to Pins 1 and 8. The 12-volt supply (V^+) at Pin 2 may be used for this purpose, but output admittance remains more nearly constant if a separate 15-volt supply (V^{++}) is used, because the base voltage on the output amplifier varies with AGC bias.

FIGURE 4 – CIRCUIT SCHEMATIC

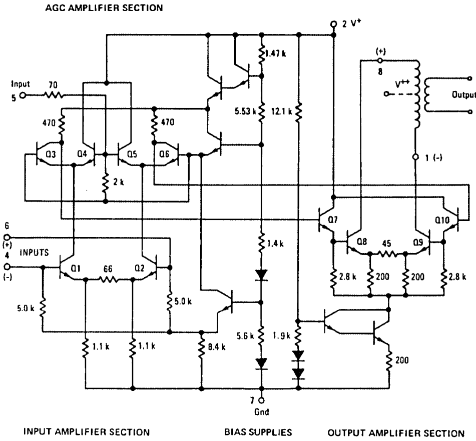
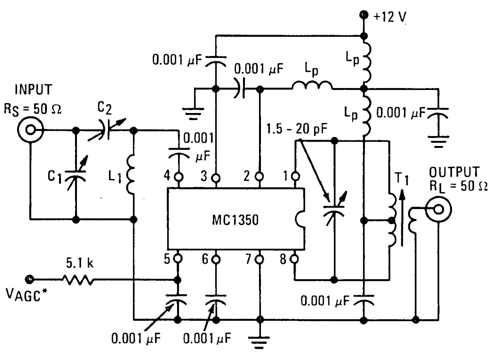


FIGURE 5 – POWER GAIN, AGC and NOISE FIGURE TEST CIRCUIT (45 MHz and 58 MHz)

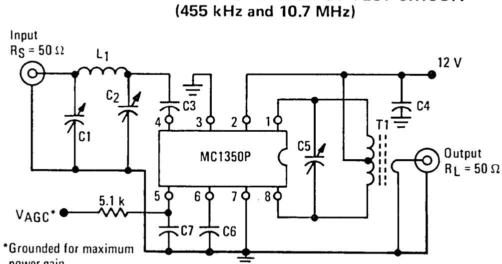


*Connect to ground for maximum power gain test.
All power-supply chokes (L_p), are self-resonate at input frequency. $L_p \geq 20$ kΩ
See Figure 10 for frequency response curve.

L_1 @ 45 MHz = 7 1/4 Turns on a 1/4" coil form.
@ 58 MHz = 6 Turns on a 1/4" coil form
T_1 Primary Winding = 18 Turns on a 1/4" coil form, center-tapped
Secondary Winding = 2 Turns centered over Primary Winding @ 45 MHz
= 1 Turn @ 58 MHz
Slug = Arnold TH Material 1/2" Long

	45 MHz		58 MHz	
L_1	0.4 μH	Q ≥ 100	0.3 μH	Q ≥ 100
T_1	1.3 - 3.4 μH	Q ≥ 100 @ 2 μH	1.2 - 3.8 μH	Q ≥ 100 @ 2 μH
C_1	50 - 160 pF		8 - 60 pF	
C_2	8 - 60 pF		3 - 35 pF	

FIGURE 6 – POWER GAIN and AGC TEST CIRCUIT (455 kHz and 10.7 MHz)



*Grounded for maximum power gain.

Note 1. Primary: 120 μH (center-tapped)
Q_u = 140 at 455 kHz
Primary: Secondary turns ratio ≈ 13

Note 2. Primary: 6.0 μH
Primary winding = 24 turns #36 AWG (close-wound on 1/4" dia. form)
Core = Arnold Type TH or equiv.
Secondary winding = 1-1/2 turns #36 AWG, 1/4" dia. (wound over center-tap)

Component	Frequency	
	455 kHz	10.7 MHz
C1	–	80–450 pF
C2	–	5.0–80 pF
C3	0.05 μF	0.001 μF
C4	0.05 μF	0.05 μF
C5	0.001 μF	36 pF
C6	0.05 μF	0.05 μF
C7	0.05 μF	0.05 μF
L1	–	4.6 μH
T1	Note 1	Note 2

TYPICAL CHARACTERISTICS

(V^+ = 12 V, T_A = +25°C)

FIGURE 7 – SINGLE-ENDED INPUT ADMITTANCE

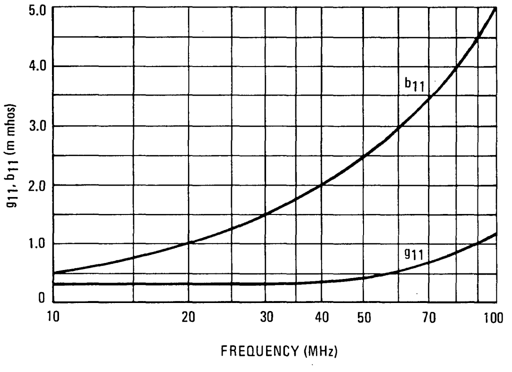


FIGURE 8 – FORWARD TRANSFER ADMITTANCE

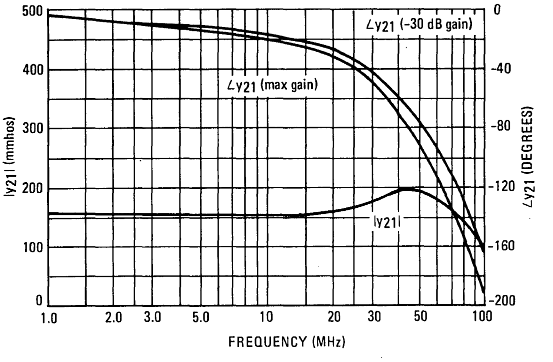


FIGURE 9 – DIFFERENTIAL OUTPUT ADMITTANCE

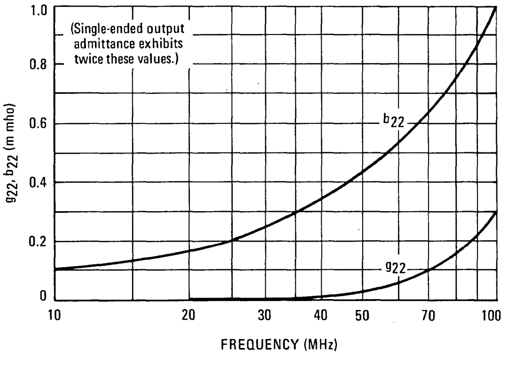
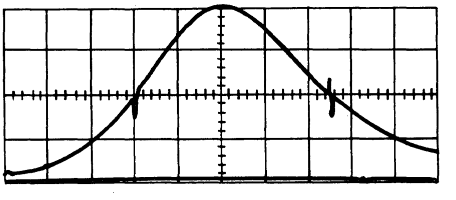
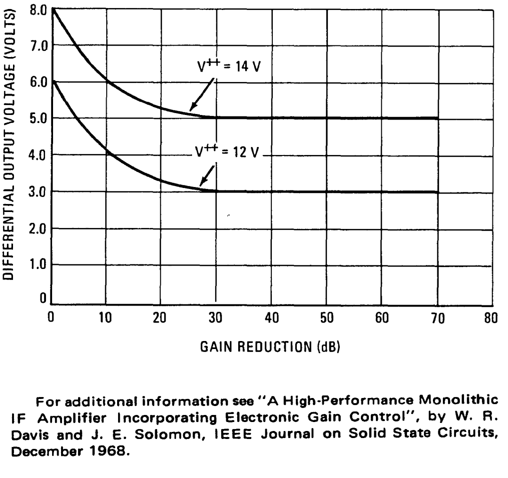


FIGURE 10 – TEST CIRCUIT RESPONSE CURVE (45 and 58 MHz)



Scale: 1 MHz/cm

FIGURE 11 – DIFFERENTIAL OUTPUT VOLTAGE



For additional information see "A High-Performance Monolithic IF Amplifier Incorporating Electronic Gain Control", by W. R. Davis and J. E. Solomon, IEEE Journal on Solid State Circuits, December 1968.

TV SOUND CIRCUIT

SOUND IF AMPLIFIER

MC1351

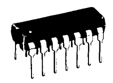
WIDE-BAND FM-AMPLIFIER; LIMITER, DETECTOR, AND AUDIO AMPLIFIER INTEGRATED CIRCUIT

. . . designed for IF limiting, detection, audio preamplifier and driver for the sound portion of a TV receiver.

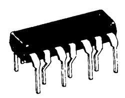
- Excellent Limiting with 80 μV(rms) Input Signal typ
- Large Output-Voltage Swing – to 3.5 V(rms) typ
- High IF Voltage Gain – 65 dB typ
- Zener Power-Supply Regulation Built-In
- Short-Circuit Protection
- A Coincidence Discriminator that Requires Only One RLC Phase Shift Network
- Preamplifier to Drive a Single External-Transistor Class-A Audio-Output Stage

TV SOUND CIRCUIT

MONOLITHIC SILICON EPITAXIAL PASSIVATED

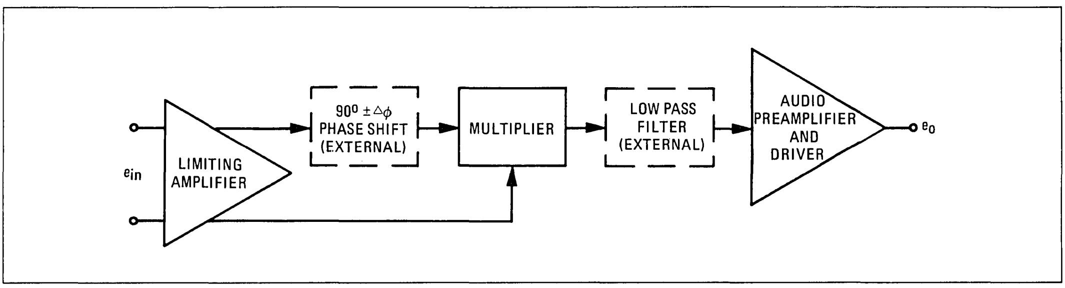


P SUFFIX
PLASTIC PACKAGE
CASE 605
TO-116

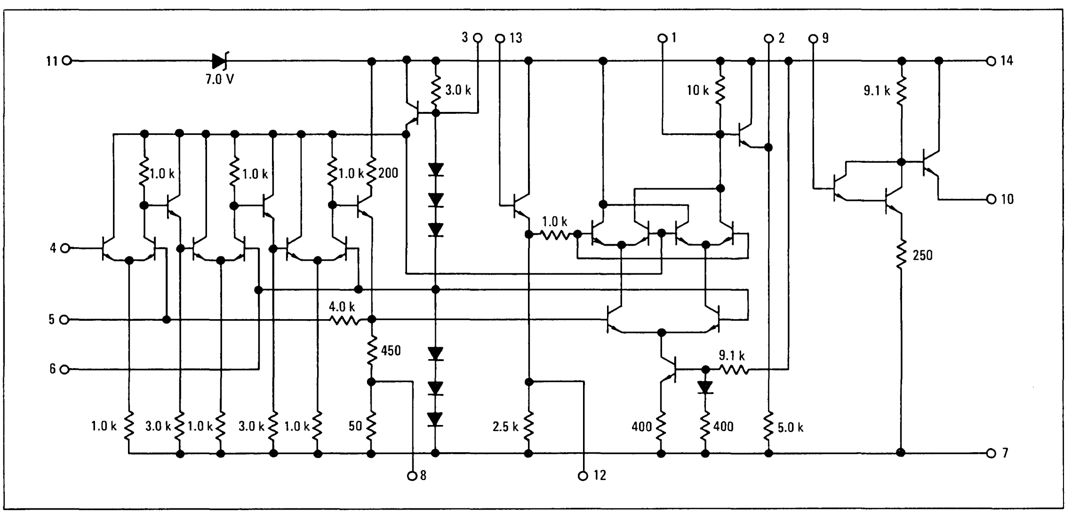


PQ SUFFIX
PLASTIC PACKAGE
CASE 647

BLOCK DIAGRAM



CIRCUIT SCHEMATIC



See Packaging Information Section for outline dimensions.

MAXIMUM RATINGS (T_A = +25° unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V+	+16	Vdc
Input Voltage	V_{in}	0.7	$V_{(rms)}$
Power Dissipation (Package Limitation) Plastic Packages Derate above +25°C	P_D $1/\theta_{JA}$	625 5.0	mW mW/°C
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

Maximum Ratings as defined in MIL-S-19500, Appendix A.

ELECTRICAL CHARACTERISTICS (V^+ = 12 Vdc, T_A = +25°C, f = 4.5 MHz, Deviation = ±25 kHz unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage (−3.0 dB Limiting)	V_L	–	80	160	μV(rms)
AM Rejection (V_{in} = 20 mV(rms), AM = 30%) (See Note 1) $AMR = 20 \log \frac{V_{OFM}}{V_{OAM}}$ { f = 4.5 MHz, Deviation = ±25 kHz, Q_L = 24 f = 5.5 MHz, Deviation = ±50 kHz, Q_L = 30	AMR	 – –	 45 45	 – –	dB
Total Harmonic Distortion (Q_L = 24) (See Note 1) (7.5 kHz Deviation)	THD	–	1.0	–	%
Maximum Undistorted Audio Output Voltage (Pin 10) (See Note 1) (Audio Gain Adjusted Externally) (Q = 24)	$V_{o(max)}$	–	3.5	–	V(rms)
Recovered Audio (Pin 2) (See Note 1) (f = 4.5 MHz, Deviation = ±25 kHz, Q_L = 24) (f = 5.5 MHz, Deviation = ±50 kHz, Q_L = 30)	V_A	 0.35 –	 0.50 0.80	 – –	V(rms)
Audio Preamplifier Open Loop Gain	A_{VP}	–	25	–	dB
IF Voltage Gain	A_{VIF}	–	65	–	dB
Parallel Input Resistance	R_{in}	–	9.0	–	kΩ
Parallel Input Capacitance	C_{in}	–	6.0	–	pF
Nominal Zener Voltage (I_Z = 5.0 mAdc)	V_{Reg}	–	11.6	–	Vdc
Power Supply Current (I_Z = 5.0 mAdc)	I_D	–	31	–	mAdc
Power Dissipation (I_Z = 5.0 mAdc)	P_D	–	300	375	mW

Note 1: Q_L is loaded circuit Q.

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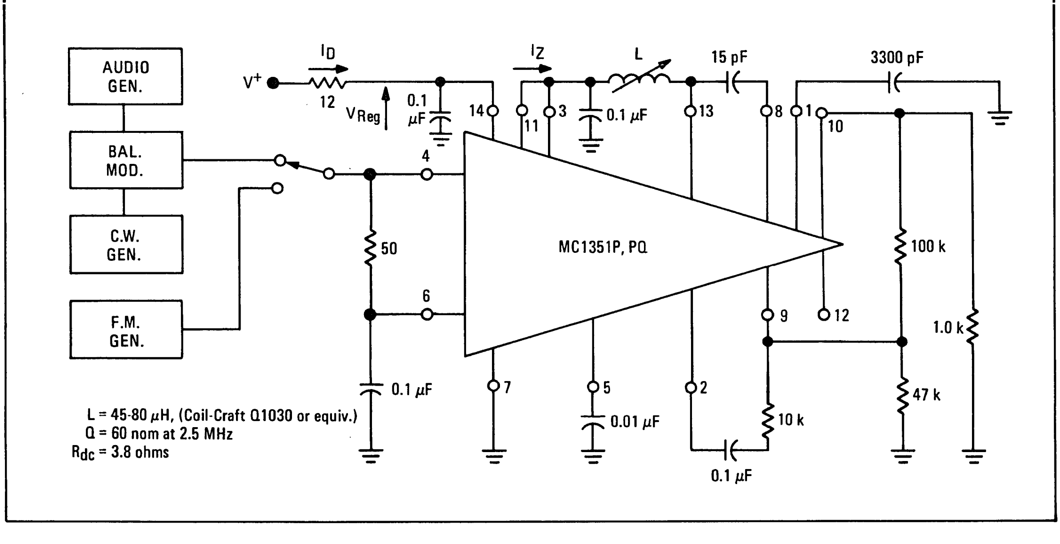
FIGURE 1 – TEST CIRCUIT (V^+ = +12 Vdc, T_A = +25°C)



TYPICAL CHARACTERISTICS

FIGURE 2 – DETECTED AUDIO OUTPUT versus INPUT LEVEL @ f = 4.5 MHz, ±25 kHz DEVIATION

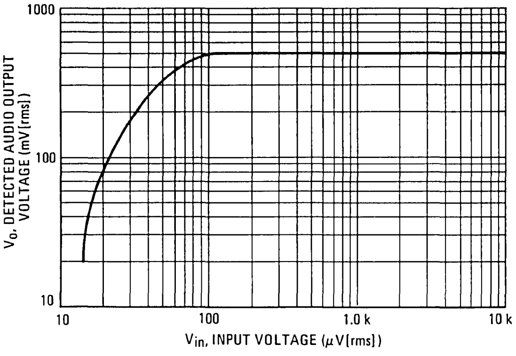


FIGURE 3 – DETECTED AUDIO OUTPUT versus INPUT LEVEL @ f = 5.5 MHz, ±50 kHz DEVIATION

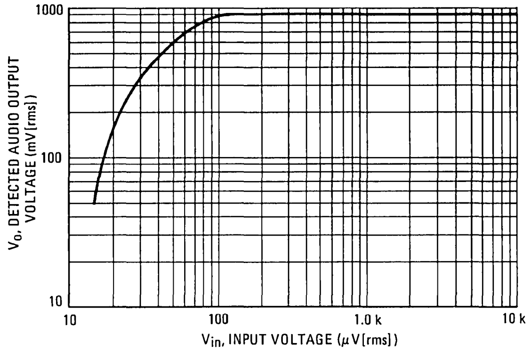


FIGURE 4 – DETECTOR "S" CURVE @ f = 4.5 MHz, BW = 200 kHz, Q = 24

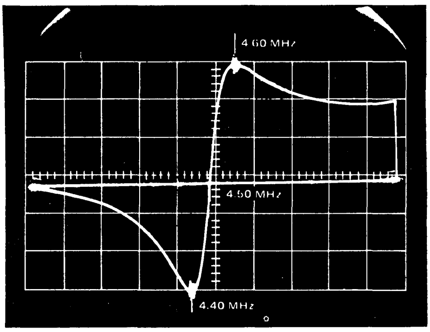


FIGURE 5 – DETECTOR "S" CURVE @ f = 5.5 MHz, BW = 220 kHz, Q = 30

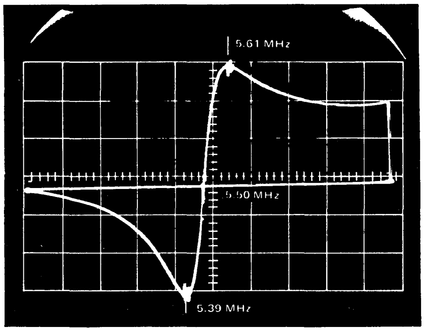


FIGURE 6 – IF VOLTAGE GAIN versus FREQUENCY

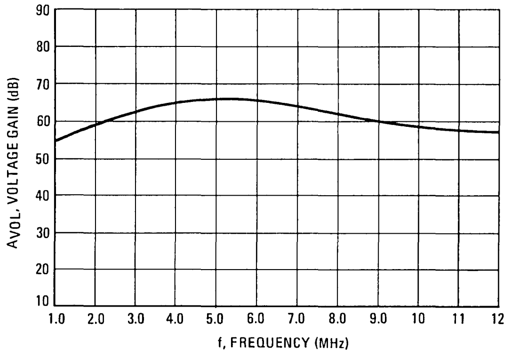


FIGURE 7 – AM REJECTION

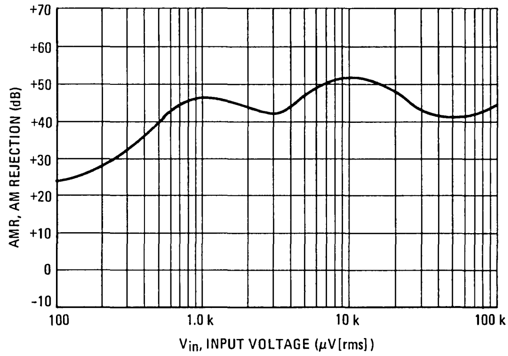
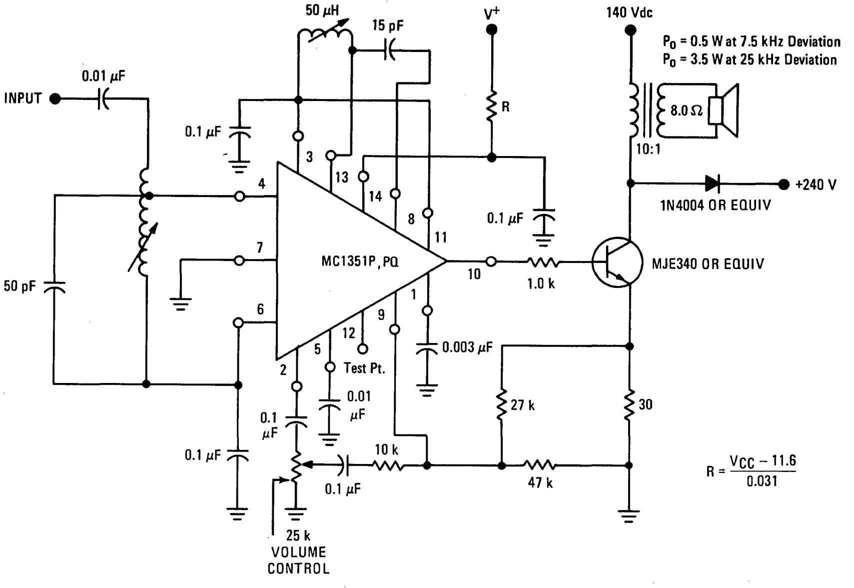


FIGURE 8 – 4.5 MHz TYPICAL APPLICATION



MC1352
MC1353

TV VIDEO IF AMPLIFIER

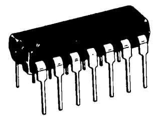
TV VIDEO IF AMPLIFIER WITH AGC AND KEYER CIRCUIT

. . . a monolithic IF amplifier with a complete gated wide-range AGC system for use as the 1st and 2nd IF stages and AGC keyer and amplifier in color or monochrome TV receivers.

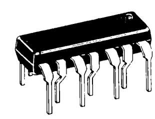
- Power Gain at 45 MHz, 52 dB typ
- Extremely Low Reverse-Transfer Admittance – << 1.0 μmho typ
- Nearly Constant Input and Output Admittance Over AGC Range
- Single-Polarity Power-Supply Operation
- High-Gain Gated AGC System for Either Positive or Negative-Going Video Signals
- Control Signal Available for Delayed AGC of Tuner
- Two Complementary Devices – MC1352 and MC1353 – Offer Opposite Tuner AGC Polarity

TV VIDEO IF AMPLIFIER WITH AGC AND KEYER CIRCUIT

MONOLITHIC SILICON INTEGRATED CIRCUIT

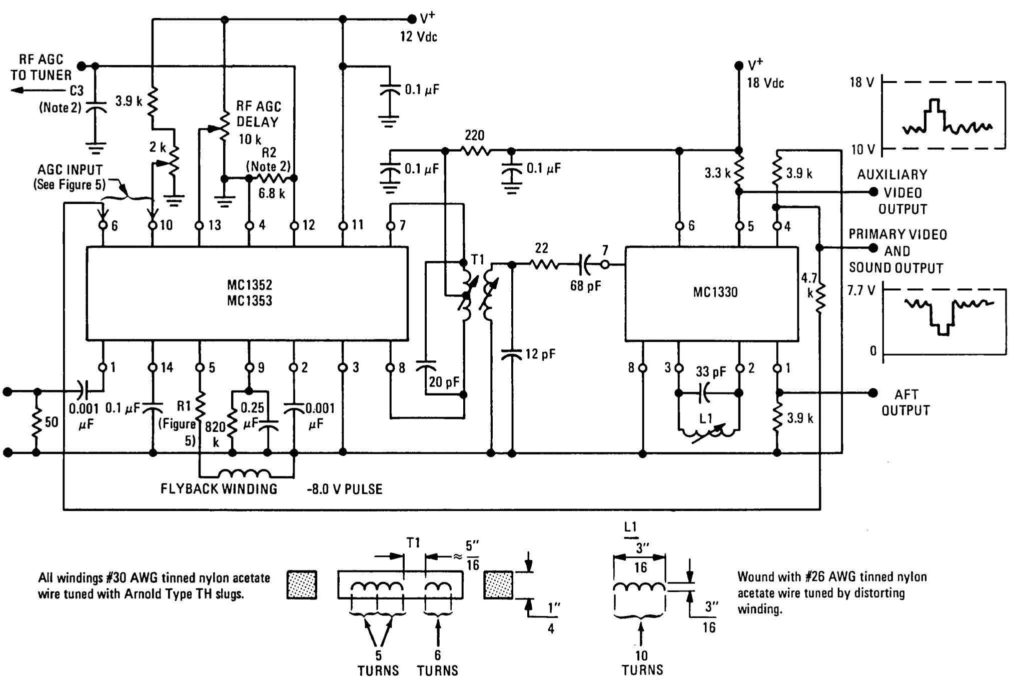


P SUFFIX
PLASTIC PACKAGE
CASE 605
TO-116



PQ SUFFIX
PLASTIC PACKAGE
CASE 647

FIGURE 1 – TYPICAL VIDEO IF AMPLIFIER APPLICATION



See Packaging Information Section for outline dimensions.

MAXIMUM RATINGS (Voltages referenced to pin 4, ground; T_A = +25°C unless otherwise noted)

Rating	Value	Unit
Power Supply (Pin 11)	+18	Vdc
Output Supply (Pins 7 and 8)	+18	Vdc
Signal Input Voltage (Pin 1 or 2, other pin ac grounded)	10	V_{p-p}
AGC Input Voltage (Pin 6 or 10, other pin ac grounded)	+6.0	Vdc
Gating Voltage, Pin 5	+10, -20	Vdc
Power Dissipation Derate above T_A = +25°C	625 5.0	mW mW/°C
Operating Temperature Range	0 to +70	°C
Storage Temperature Range	-55 to +150	°C

Maximum Ratings as defined in MIL-S-19500, Appendix A.

ELECTRICAL CHARACTERISTICS (V+ = +12 Vdc, Voltages referenced to pin 4, ground; T_A = +25°C unless otherwise noted)

Characteristic	Min	Typ	Max	Unit
AGC Range	–	75	–	dB
Power Gain f = 35 MHz or 45 MHz f = 58 MHz	 – –	 52 50	 – –	dB
Maximum Differential Output Voltage Swing 0 dB AGC -30 dB AGC	 – –	 16.8 8.4	 – –	V_{p-p}
Voltage Range for RF-AGC at Pin 12 Maximum Minimum	 – –	 7.0 0.2	 – –	Vdc
IF Gain Change Over RF-AGC Range	–	10	–	dB
Output Stage Current ($I_7 + I_8$)	–	5.7	–	mAdc
Total Supply Current ($I_7 + I_8 + I_{11}$)	–	27	31	mAdc
Total Power Dissipation	–	325	370	mW

DESIGN PARAMETERS, TYPICAL VALUES (V+ = 12 Vdc, T_A = +25°C unless otherwise noted)

Parameters	Symbol	f = 35 MHz	f = 45 MHz	f = 58 MHz	Unit
Single-Ended Input Admittance	g_{11} b_{11}	0.55 2.25	0.70 2.80	1.1 3.75	mmhos
Input Admittance Variations with AGC (0 to 60 dB)	Δg_{11} Δb_{11}	50 0	60 0	– –	µmhos
Differential Output Admittance	g_{22} b_{22}	20 430	40 570	75 780	µmhos
Output Admittance Variations with AGC (0 to 60 dB)	Δg_{22} Δb_{22}	3.0 80	4.0 100	– –	µmhos
Reverse Transfer Admittance	$\lvert y_{12} \rvert$	<<1.0	<<1.0	<<1.0	µmho
Forward Transfer Admittance Magnitude Angle (0 dB AGC) Angle (-30 dB AGC)	 $\lvert y_{12} \rvert$ $\angle y_{21}$ $\angle y_{21}$	 260 -73 -52	 240 -100 -72	 210 -135 -96	 mmhos degrees
Single-Ended Input Capacitance		9.5	10	10.5	pF
Differential Output Capacitance		2.0	2.0	2.5	pF

6

FIGURE 2 – CIRCUIT SCHEMATIC

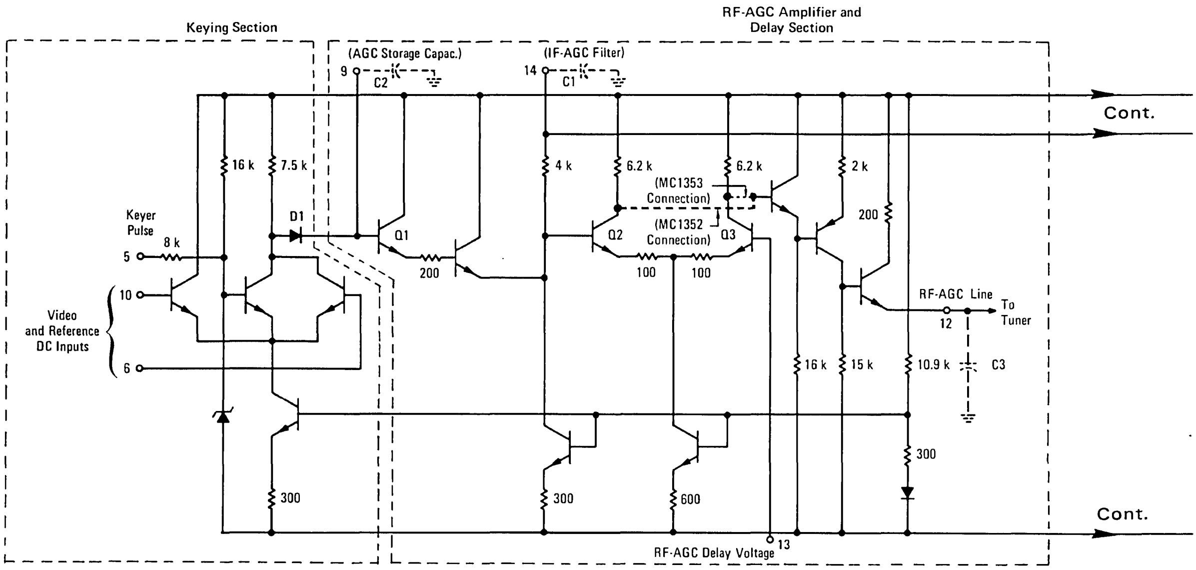
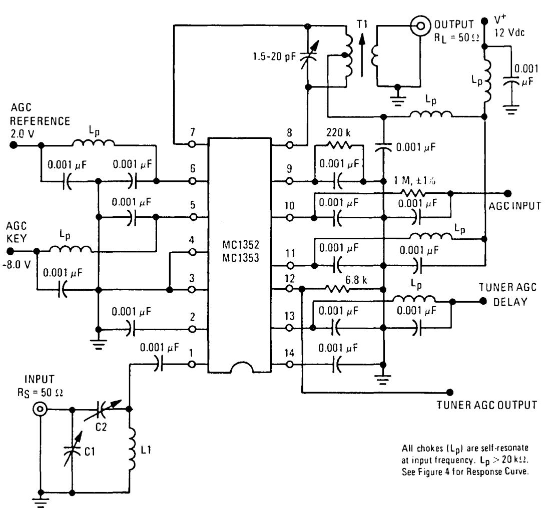


FIGURE 3 – POWER GAIN, AGC AND NOISE TEST CIRCUIT



All chokes (L_p) are self-resonate at input frequency. L_p > 20 kΩ. See Figure 4 for Response Curve.

	35 and 45 MHz		58 MHz	
L1	0.4 µH	Q ≥ 100	0.3 µH	Q ≥ 100
T1	1.3-3.4 µH	Q ≥ 100 @ 2 µH	1.2-3.8 µH	Q ≥ 100 @ 2 µH
C1	48-100 pF		40-80 pF	
C2	8-60 pF		12-45 pF	

L1 and T1 = #26 AWG Tinned Nylon Acetate Wire.

L1 @ 35 or 45 MHz = 7-1/4 Turns on a 1/4" coil form
@ 58 MHz = 6 Turns on a 1/4" coil form
T1 Primary Winding = 18 Turns on a 1/4" coil form
Secondary Winding = 2 Turns Wound Evenly over Primary Winding for 35 or 45 MHz and 1 Turn for 58 MHz
Slug = Arnold TH Material 1/2" long

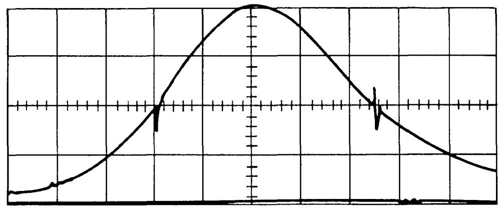
GENERAL OPERATING INFORMATION

Each device, MC1352 and MC1353, consists of an AGC section and an IF signal amplifier (Figure 2) subdivided into different functions as indicated by the illustration.

A gating pulse, a reference level, and a composite video signal are required for proper operation of the AGC section. Either positive or negative-going video may be used; necessary connections and signal levels are shown in Figure 1. The essential difference is that the video is fed into Pin 10 and the AGC reference level is applied to Pin 6 for a video signal with positive-going sync while the input connections are reversed for negative-going sync.

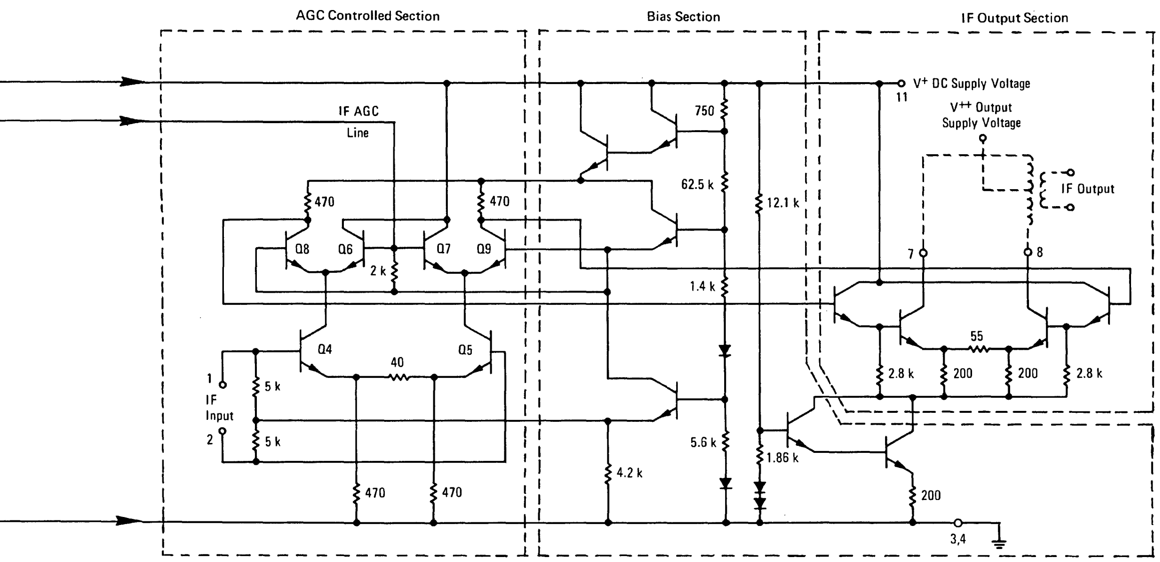
The action of the gating section is such that the proper voltage,

FIGURE 4 – TEST CIRCUIT RESPONSE CURVE (45 and 58 MHz)



Scale: 1 MHz/cm

IF AMPLIFIER



V_C, is maintained across the external capacitor, C2, for a particular video level and dc reference setting. The voltage V_C, is the result of the charge delivered through D1 and the charge drained by Q1. The charge delivered occurs during the time of the gating pulse, and its magnitude is determined by the amplitude of the video signal relative to the dc reference level. The voltage V_C is delivered via the IF-AGC amplifier and applied to the variable gain stage of the IF signal amplifier and is also applied to the RF-AGC amplifier, where it is compared to the fixed RF-AGC delay voltage reference by the differential amplifier, Q2 and Q3. The following stages amplify the output signal of either Q2 for MC1352, or Q3 for MC1353 and shift the dc levels causing the RF-AGC voltage to vary (positive-going for MC1352 or negative-going for MC1353).

The input amplifiers (Q4 and Q5) operate at constant emitter currents so that input impedance remains independent of AGC action. Input signals may be applied single-ended or differentially (for ac). Terminals 1 and 2 may be driven from a transformer, but a dc path from either terminal to ground is not permitted.

AGC action occurs as a result of an increasing voltage on the base of Q6 and Q7 causing those transistors to conduct more heavily thereby shunting signal current from the interstage amplifiers Q8 and Q9. The output amplifiers are fed from an active current source to maintain constant quiescent bias thereby holding output admittance nearly constant.

6

NOTES:

1. The 12-V supply must have a low ac impedance to prevent low-frequency instability in the RF-AGC loop. This can be achieved by a 12-V zener diode and a large decoupling capacitor. (5 μF).

2. Choices of C1, C2 and C3 depend somewhat on the set designers' preference concerning AGC stability versus AGC recovery speed. Typical values are C1 = 0.1 μF, C2 = 0.25 μF, C3 = 10 μF.

3. To set a fixed IF-AGC operating point (e.g., for receiver alignment) connect a 22 kΩ resistor from pin 9 to pin 11 to give minimum gain, then bias pin 14 to give the correct operating point using a 200 kΩ variable resistor to ground.

4. Although the unit will normally be operating with a very high power gain, the pin configuration has been carefully chosen so that shielding between input and output terminals will not normally be necessary even when a standard socket is used.

FIGURE 5 – TYPICAL AGC APPLICATION CHART

Video Polarity	Pin 6 Voltage	Pin 10 Voltage	Pin 5 R1 (Ω)
Negative-Going Sync.	5.5 2.0 0	Adj. 1.0–4.0 Vdc Nom 2.0 V	0
Positive-Going Sync.	Adj. 1.0–8.0 Vdc Nom 4.5 V	4.5 0	3.9 k

TYPICAL CHARACTERISTICS
(V^+ = +12 Vdc, T_A = +25°C unless otherwise noted)

FIGURE 6 – SINGLE-ENDED INPUT ADMITTANCE

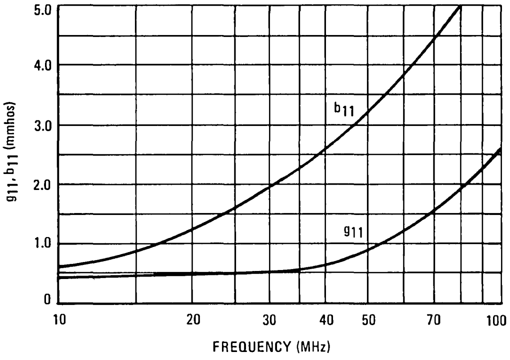


FIGURE 7 – DIFFERENTIAL OUTPUT ADMITTANCE

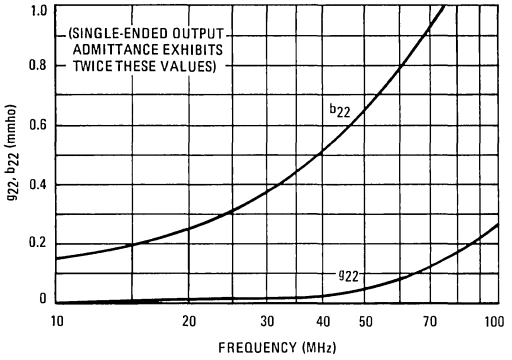


FIGURE 8 – FORWARD TRANSFER ADMITTANCE

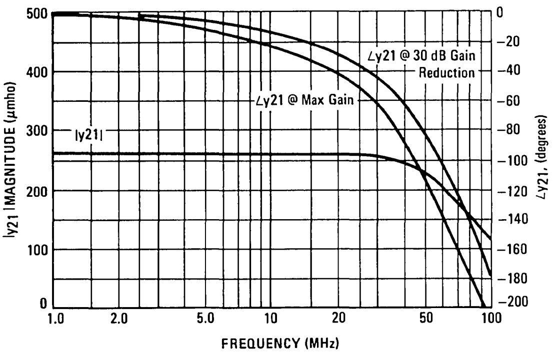


FIGURE 9 – DIFFERENTIAL OUTPUT VOLTAGE

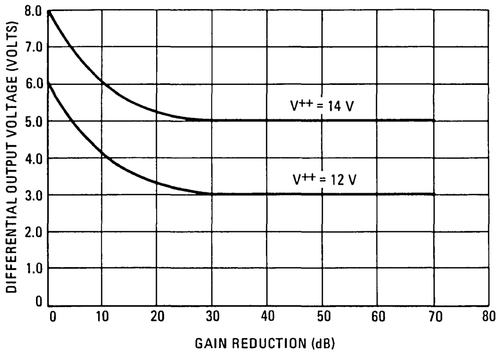


FIGURE 10 – MC1352 AGC CHARACTERISTICS

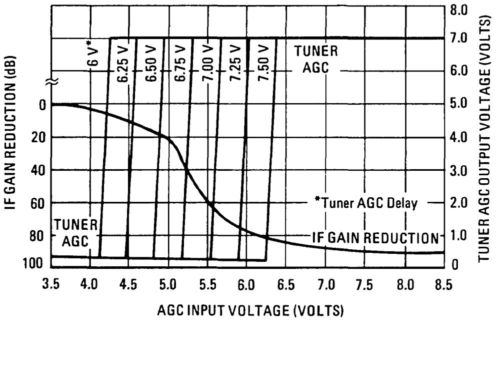
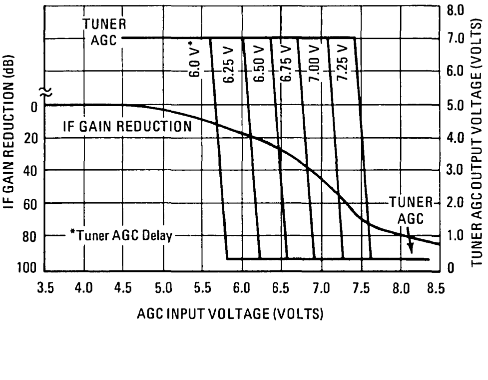


FIGURE 11 – MC1353 AGC CHARACTERISTICS

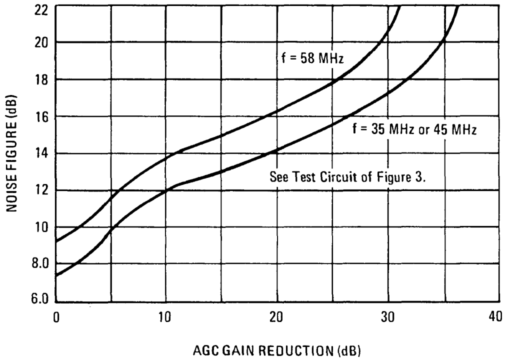


6

TYPICAL CHARACTERISTICS (continued)

($V^+ = +12$ Vdc, $T_A = +25^{\circ}C$ unless otherwise noted)

FIGURE 12 – TYPICAL NOISE FIGURE



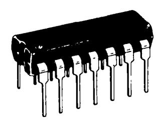
For additional information see "A High-Performance Monolithic IF Amplifier Incorporating Electronic Gain Control", by W. R. Davis and J. E. Solomon, IEEE Journal on Solid State Circuits, December 1968.

MC1355

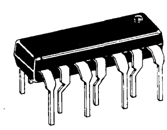
FM IF AMPLIFIER

LIMITING FM IF AMPLIFIER

MONOLITHIC SILICON INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 605
TO-116



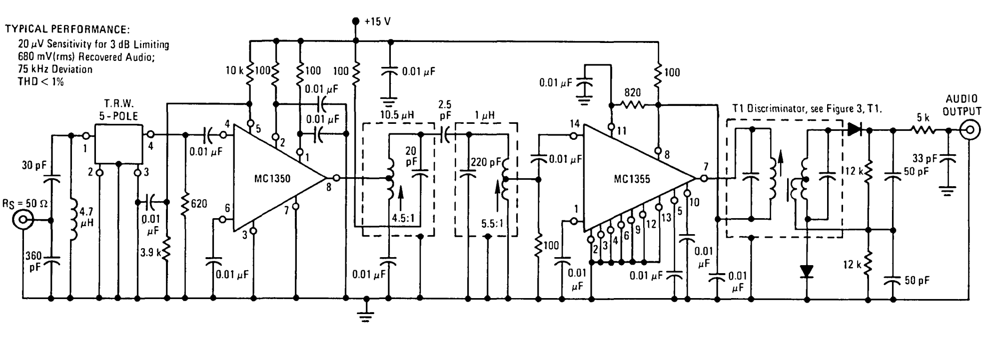
PQ SUFFIX
PLASTIC PACKAGE
CASE 647

BALANCED MONOLITHIC FOUR-STAGE HIGH-GAIN FM/IF AMPLIFIER

. . . designed for use with Foster-Seeley discriminator or ratio detector in high quality FM systems.

- High AM Rejection (60 dB typ)
- Wide Range of Supply Voltages (8 to 18 Vdc)
- Low Distortion (0.5% typ)

FIGURE 1 — TYPICAL FM-IF APPLICATION



When using the device as a non-saturating limiter the load must be chosen to prevent voltage saturation of the output stage. The load impedance can be calculated from:

$$R_L \le \frac{2(V^+ - 5.3)}{5.0} \text{ kilohms}$$

See Packaging Information Section for outline dimensions.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

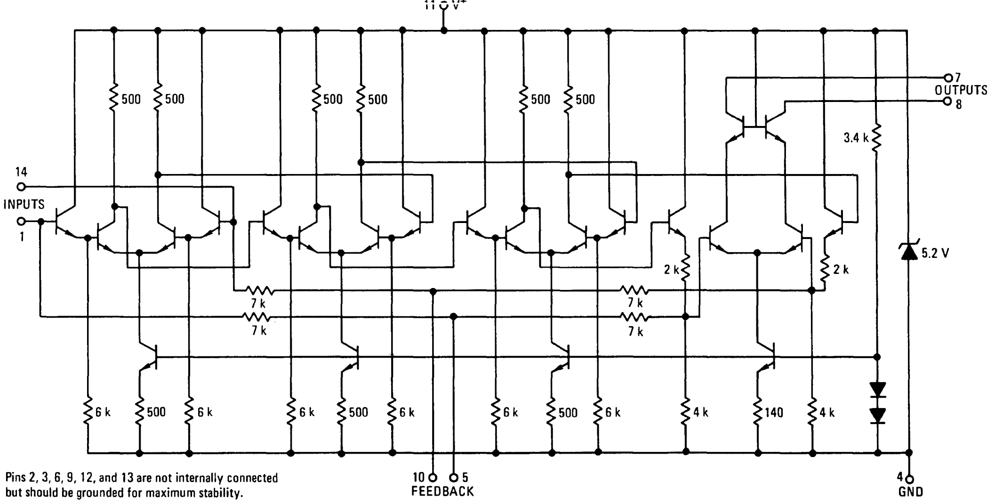
Rating	Value	Unit
Output Voltage (pins 7 & 8)	40	Vdc
Supply Current to pin 11	20	mA
Input Signal Voltage (single-ended)	5.0	Vp-p
Input Signal Voltage (differential)	10	Vp-p
Power Dissipation (package limitation) Derate above T_A = +25°C	625 5.0	mW mW/°C
Operating Temperature Range (Ambient)	0 to +75	°C
Storage Temperature Range	-65 to +150	°C

Maximum Ratings as defined in MIL-S-19500, Appendix A.

ELECTRICAL CHARACTERISTICS (V^+ = 15 Vdc, f = 10.7 MHz, T_A = +25°C, R_S = 820 ohms unless otherwise noted)

Characteristic	Min	Typ	Max	Units
Power Supply Voltage Range	8.0	15	18	Vdc
Total Circuit Current	–	16	–	mAdc
Total Output Stage Current	–	4.2	–	mA
Device Dissipation	–	125	–	mW
Internal Zener Voltage	–	5.2	–	Vdc
Input Signal for 3 dB Limiting	–	175	250	μV(rms)
Output Current Swing	3.5	4.2	5.0	mA p-p
AM Rejection (10 mv to 1.0 v (rms) input, FM @ 100%, AM @ 80%, Foster Seeley detector)	–	60	–	dB
Maximum AM Signal before Breakup (FM @ 100%, AM @ 80%)	–	–	1.4	V(rms)
Admittance Parameters Y_{11}	–	120 + j320	–	μmhos
Y_{12}	–	j0.6	–	μmho
Y_{21}	–	8 + j5.9	–	mhos
Y_{22}	–	15 + j230	–	μmhos

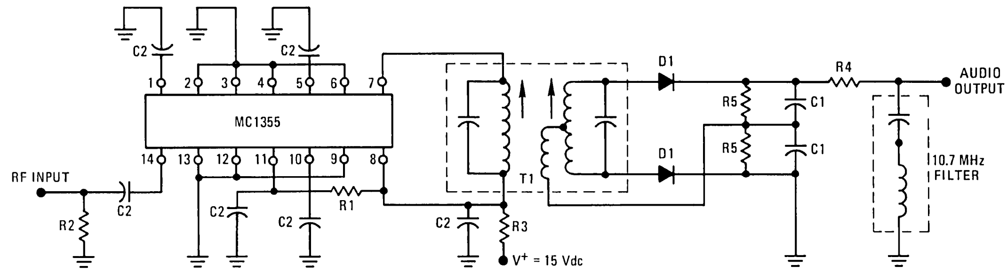
FIGURE 2 – CIRCUIT SCHEMATIC



Pins 2, 3, 6, 9, 12, and 13 are not internally connected but should be grounded for maximum stability.

TYPICAL CHARACTERISTICS

FIGURE 3 – TEST CIRCUIT



R1 820 ohms
R2 50 ohms
R3 100 ohms
R4 5 kilohms
R5 12 kilohms

C1 50 pF
C2 0.01 μF
T1 10.7 MHz Foster-Seeley Discriminator, Primary Impedance = 3.9 k, Peak-to-Peak Separation = 600 kHz

D1 Small Signal Germanium Diode (1N542 or equiv)

Specifications are given for a Foster-Seeley discriminator. Improved AM rejection at low signal levels can be obtained with a ratio detector.

For optimum circuit stability it is important to ground pins 2, 3, 4, 6, 9, 12, and 13.

FIGURE 4 – AM REJECTION TEST BLOCK DIAGRAM

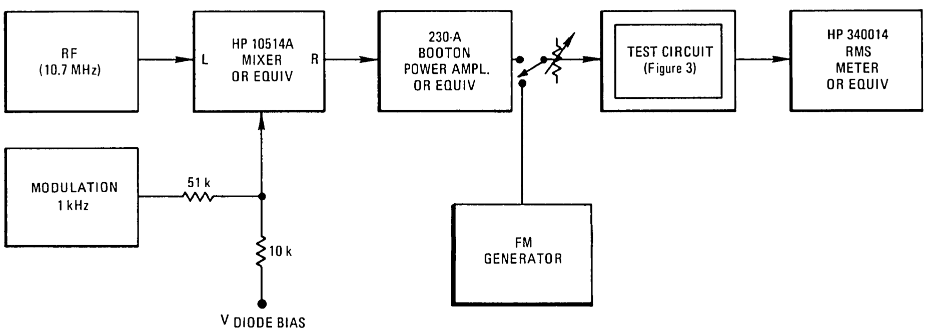


FIGURE 5 – LIMITING

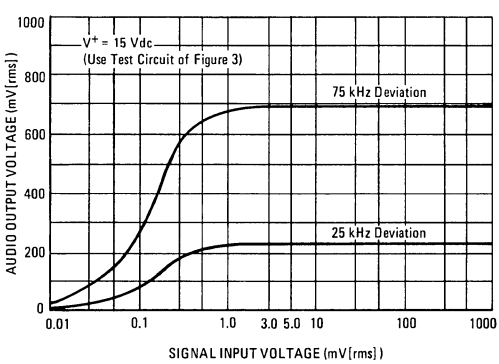
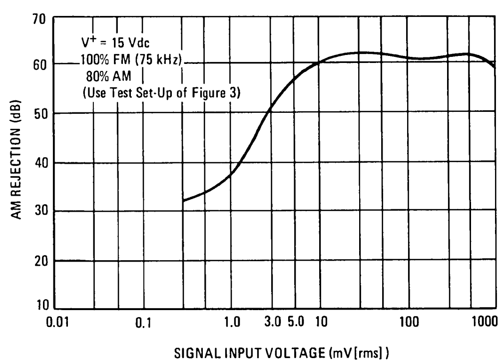


FIGURE 6 – AM REJECTION



6

TYPICAL CHARACTERISTICS (continued)

FIGURE 7 – OUTPUT DISTORTION

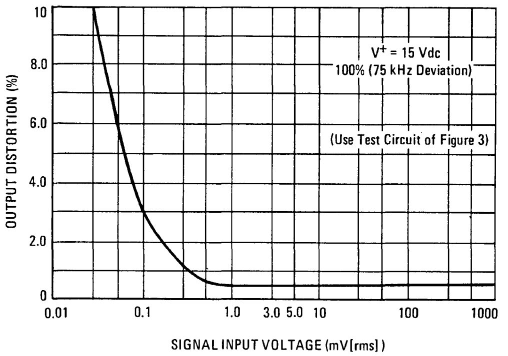


FIGURE 8 – SIGNAL-TO-NOISE RATIO SIGNAL

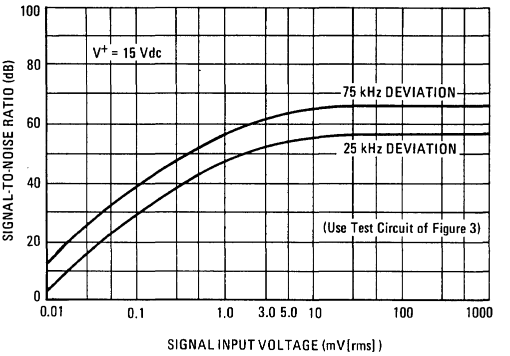
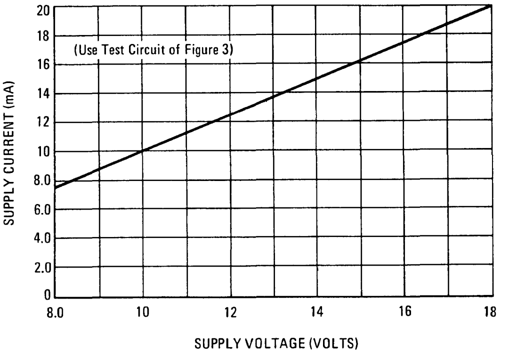


FIGURE 9 – TOTAL SUPPLY CURRENT



6

MC1357

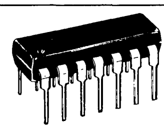
SOUND IF AMPLIFIER

MONOLITHIC TV SOUND IF OR FM IF AMPLIFIER WITH QUADRATURE DETECTOR

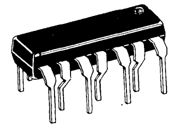
- A Direct Replacement for the ULN2111A
- Greatly Simplified FM Demodulator Alignment
- Excellent Performance at V^+ = 8.0 Vdc

IF AMPLIFIER AND QUADRATURE DETECTOR

MONOLITHIC SILICON INTEGRATED CIRCUIT



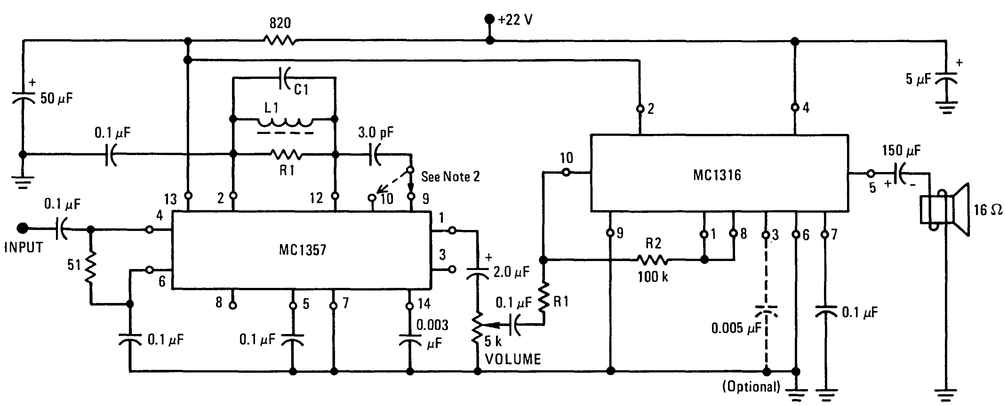
P SUFFIX
PLASTIC PACKAGE
CASE 646
TO-116



PQ SUFFIX
PLASTIC PACKAGE
CASE 647

6

FIGURE 1 – TV TYPICAL APPLICATION CIRCUIT



Typical Performance:
2 Watts Output
2% Distortion
250 µV Sensitivity (3 dB Lim.)

C1 = 120 pF
L1 = 14 µH
R1 = 20 kΩ
Q = 30

See Packaging Information Section for outline dimensions.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Value	Unit
Power Supply Voltage	16	Vdc
Input Voltage (Pin 4)	3.5	V_p
Power Dissipation (Package Limitation) Plastic Packages Derate above T_A = +25°C	625 5.0	mW mW/°C
Operating Temperature Range (Ambient)	0 to +75	°C
Storage Temperature Range	-65 to +150	°C

Maximum Ratings as defined in MIL-S-19500, Appendix A.

ELECTRICAL CHARACTERISTICS (V^+ = 12 Vdc, T_A = +25°C unless otherwise noted)

Characteristic		Pin	Min	Typ	Max	Units
Drain Current	V^+ = 8 V V^+ = 12 V	13	10 –	12 15	19 21	mA
Amplifier Input Reference Voltage		6	–	1.45	–	Vdc
Detector Input Reference Voltage		2	–	3.65	–	Vdc
Amplifier High Level Output Voltage		10	1.25	1.45	1.65	Vdc
Amplifier Low Level Output Voltage		9	–	0.145	0.2	Vdc
Detector Output Voltage	V^+ = 8 V V^+ = 12 V	1	– –	3.7 5.4	– –	Vdc
Amplifier Input Resistance		4	–	5.0	–	kΩ
Amplifier Input Capacitance		4	–	11	–	pF
Detector Input Resistance		12	–	70	–	kΩ
Detector Input Capacitance		12	–	2.7	–	pF
Amplifier Output Resistance		10	–	60	–	ohms
Detector Output Resistance		1	–	200	–	ohms
De-Emphasis Resistance		14	–	8.8	–	kΩ

DYNAMIC CHARACTERISTICS (FM Modulation Freq. = 1.0 kHz, Source Resistance = 50 ohms, T_A = +25°C for all tests.)

(V^+ = 12 Vdc, f_o = 4.5 MHz, $\Delta f = \pm 25$ kHz, Peak Separation = 150 kHz)

Characteristics	Pin	Min	Typ	Max	Units
Amplifier Voltage Gain ($V_{in} \leq 50\ \mu V$[rms])	10	–	60	–	dB
AM Rejection* (V_{in} = 10 mV[rms])	1	–	36	–	dB
Input Limiting Threshold Voltage	4	–	250	–	μV(rms)
Recovered Audio Output Voltage (V_{in} = 10 mV[rms])	1	–	0.72	–	V(rms)
Output Distortion (V_{in} = 10 mV[rms])	1	–	3	–	%

(V^+ = 12 Vdc, f_o = 5.5 MHz, $\Delta f = \pm 50$ kHz, Peak Separation = 260 kHz)

Characteristics	Pin	Min	Typ	Max	Units
Amplifier Voltage Gain ($V_{in} \leq 50\ \mu V$[rms])	10	–	60	–	dB
AM Rejection* (V_{in} = 10 mV[rms])	1	–	40	–	dB
Input Limiting Threshold Voltage	4	–	250	–	μV(rms)
Recovered Audio Output Voltage (V_{in} = 10 mV[rms])	1	–	1.2	–	V(rms)
Output Distortion (V_{in} = 10 mV[rms])	1	–	5	–	%

(V^+ = 8.0 Vdc, f_o = 10.7 MHz, $\Delta f = \pm 75$ kHz, Peak Separation = 550 kHz)

Characteristics	Pin	Min	Typ	Max	Units
Amplifier Voltage Gain ($V_{in} \leq 50\ \mu V$[rms])	10	–	53	–	dB
AM Rejection* (V_{in} = 10 mV[rms])	1	–	37	–	dB
Input Limiting Threshold Voltage	4	–	600	–	μV(rms)
Recovered Audio Output Voltage (V_{in} = 10 mV[rms])	1	–	0.30	–	V(rms)
Output Distortion (V_{in} = 10 mV[rms])	1	–	1.4	–	%

(V^+ = 12 Vdc, f_o = 10.7 MHz, $\Delta f = \pm 75$ kHz, Peak Separation = 550 kHz)

Characteristics	Pin	Min	Typ	Max	Units
Amplifier Voltage Gain ($V_{in} \leq 50\ \mu V$[rms])	10	–	53	–	dB
AM Rejection* (V_{in} = 10 mV[rms])	1	–	45	–	dB
Input Limiting Threshold Voltage	4	–	600	–	μV(rms)
Recovered Audio Output Voltage (V_{in} = 10 mV[rms])	1	–	0.48	–	V(rms)
Output Distortion (V_{in} = 10 mV[rms])	1	–	1.4	–	%

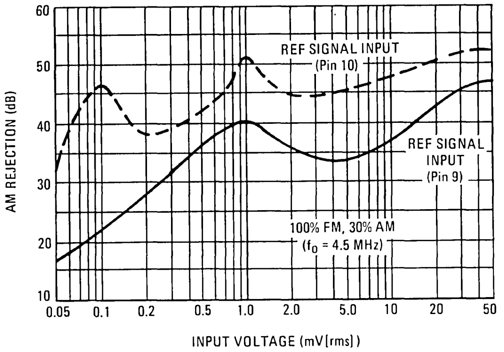
*100% FM, 30% AM Modulation

TYPICAL CHARACTERISTICS

(V+ = 12 V, T_A = +25°C unless otherwise noted)
(Use Test Circuit of Figure 13)

(f_o = 4.5 MHz)

FIGURE 2 – AM REJECTION



(f_o = 5.5 MHz)

FIGURE 3 – AM REJECTION

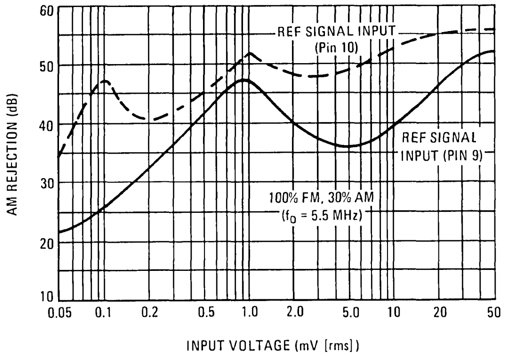


FIGURE 4 – DETECTED AUDIO OUTPUT

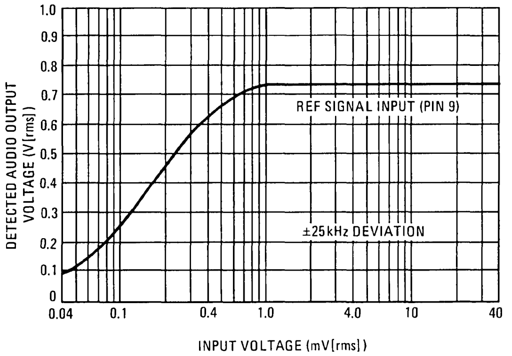


FIGURE 5 – DETECTED AUDIO OUTPUT

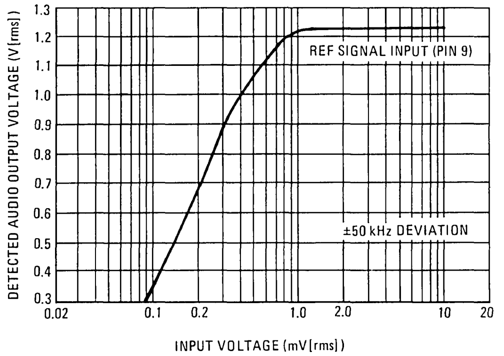


FIGURE 6 – DETECTOR TRANSFER CHARACTERISTIC

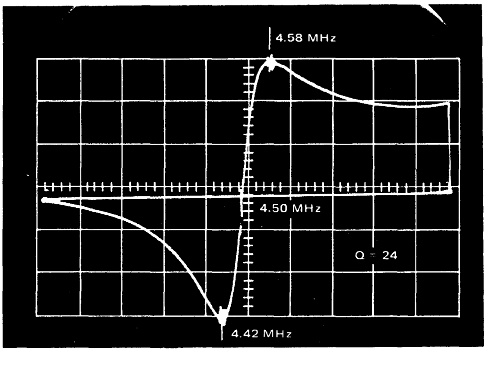
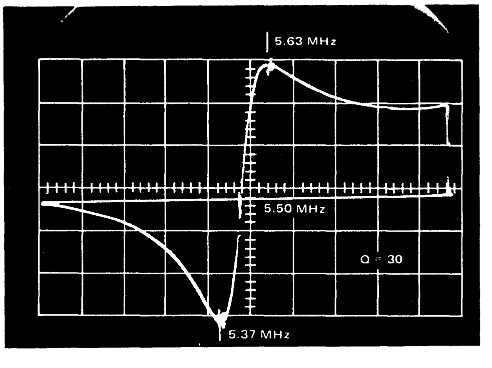


FIGURE 7 – DETECTOR TRANSFER CHARACTERISTIC



TYPICAL CHARACTERISTICS (continued)

(f_o = 10.7 MHz, T_A = +25°C unless otherwise noted.)
(Use Test Circuit of Figure 13)

FIGURE 8 – AM REJECTION

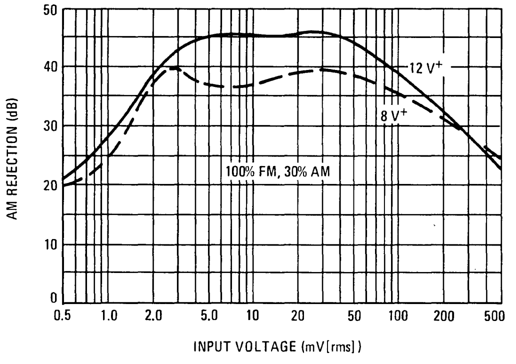


FIGURE 9 – AFC VOLTAGE DRIFT
(1.0 mV INPUT CARRIER @ 10.7 MHz)

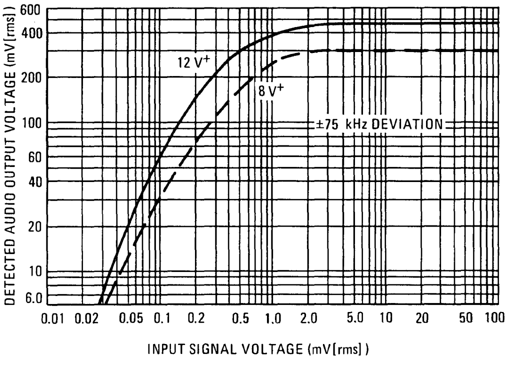


FIGURE 10 – LIMITING

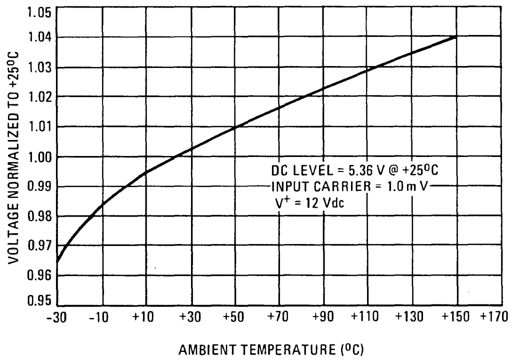


FIGURE 11 – SIGNAL-TO-NOISE RATIO

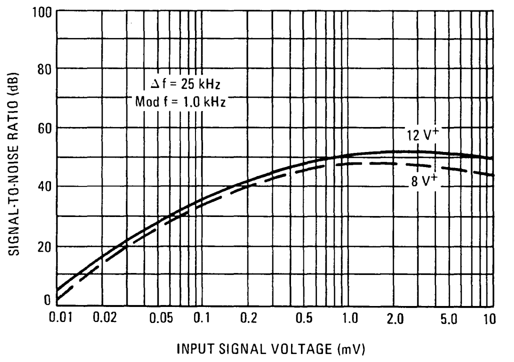


FIGURE 12 – DETECTOR TRANSFER CHARACTERISTIC

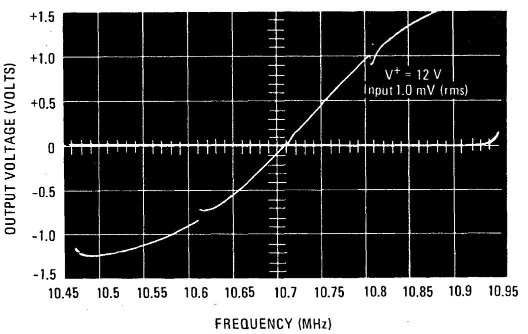
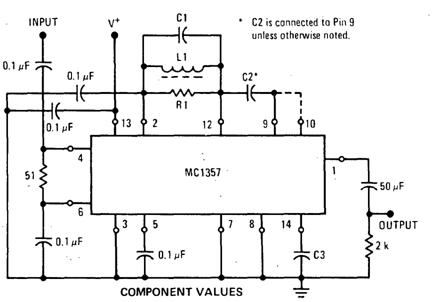


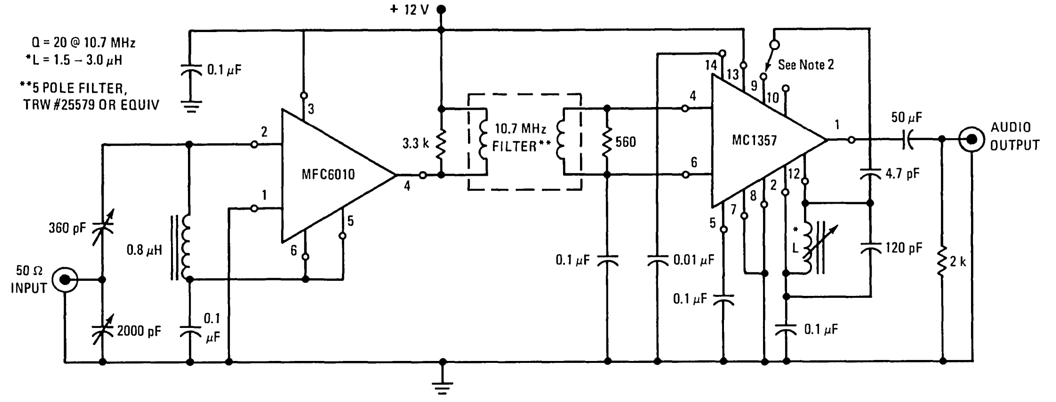
FIGURE 13 – TEST CIRCUIT



COMPONENT VALUES

f	L1	C1	R1	Q(R1, L1)	C2	C3
MHz	µH	pF	kΩ		pF	µF
4.5	14	120	20	30	3.0	0.003
5.5	8.0	100	20	30	3.0	0.003
10.7	2.0	120	3.9	20	4.7	0.01

FIGURE 14 – FM RADIO TYPICAL APPLICATION CIRCUIT



Note 1:

Information shown in Figures 15, 16, and 17 was obtained using the circuit of Figure 14.

Note 2:

Optional input to the quadrature coil may be from either pin 9 or pin 10 in the applications shown. Pin 9 has commonly been used on this type of part to avoid overload with various tuning techniques. For this reason, pin 9 is used in tests on the preceding pages (except as noted). However, a significant improvement of limiting sensitivity can be obtained using pin 10, see Figure 17, and no overload problems have been incurred with this tuned circuit configuration.

FIGURE 15 – OUTPUT DISTORTION

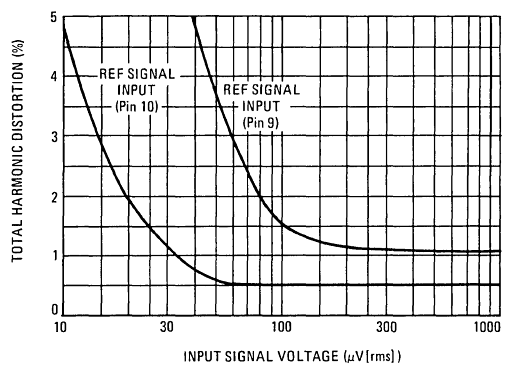


FIGURE 16 – SIGNAL-TO-NOISE RATIO

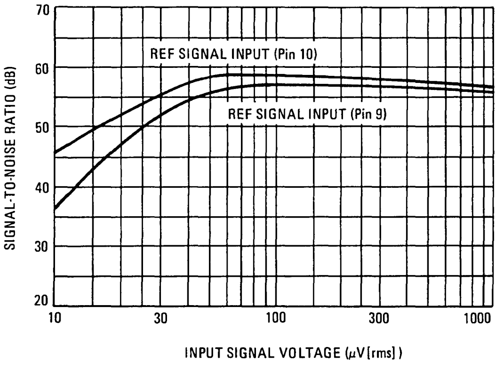


FIGURE 17 – RECOVERED AUDIO OUTPUT

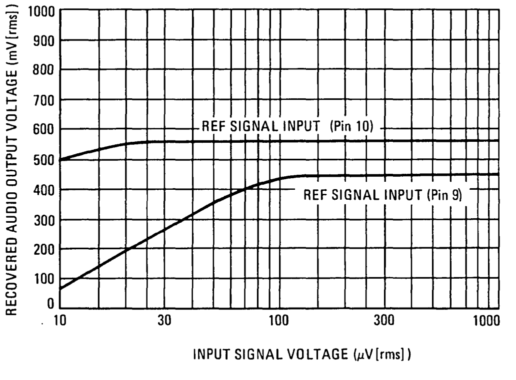
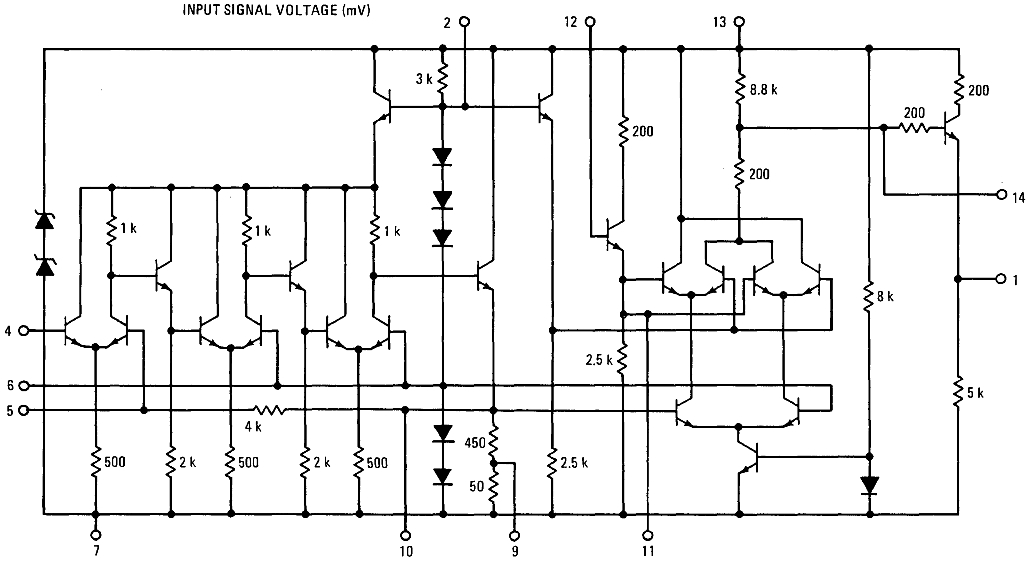


FIGURE 18 – CIRCUIT SCHEMATIC



MC1358

SOUND IF AMPLIFIER

TV SOUND IF AMPLIFIER

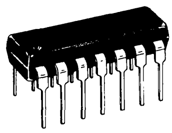
. . . a versatile monolithic device incorporating IF limiting, detection, electronic attenuation, audio amplifier, and audio driver capabilities.

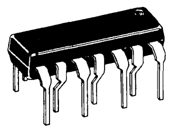
- Direct Replacement for the CA3065
- Differential Peak Detector Requiring a Single Tuned Circuit
- Electronic Attenuator Replaces Conventional ac Volume Control – Range > 60 dB
- Excellent AM Rejection @ 4.5 and 5.5 MHz
- High Stability
- Low Harmonic Distortion
- Audio Drive Capability – 6.0 mAp-p
- Minimum Undesirable Output Signal @ Maximum Attenuation

IF AMPLIFIER, LIMITER, FM DETECTOR, AUDIO DRIVER, ELECTRONIC ATTENUATOR

MONOLITHIC SILICON INTEGRATED CIRCUIT

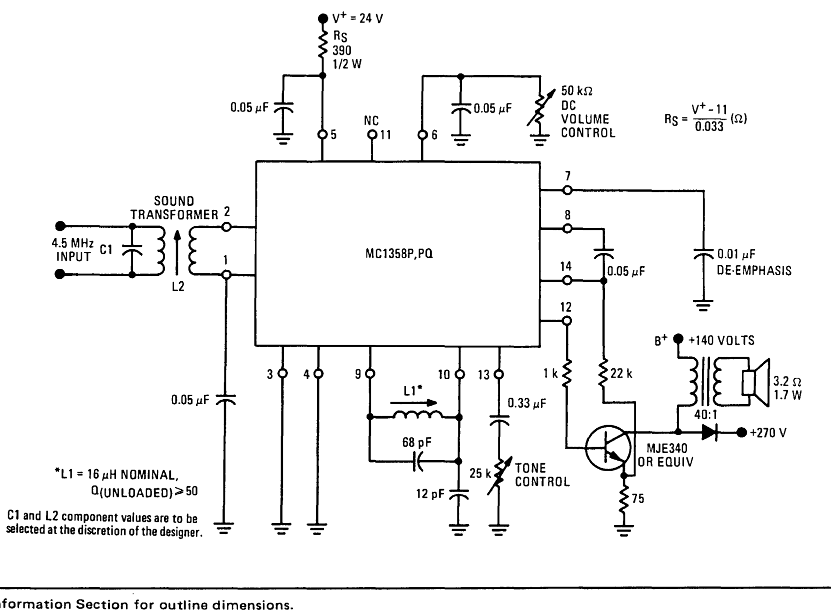
P SUFFIX
PLASTIC PACKAGE
CASE 646
TO-116





PQ SUFFIX
PLASTIC PACKAGE
CASE 647

FIGURE 1 – TYPICAL TV APPLICATION CIRCUIT



See Packaging Information Section for outline dimensions.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Value	Unit
Input Signal Voltage (Pins 1 and 2)	±3.0	Vdc
Power Supply Current	50	mA
Power Dissipation (Package Limitation) Plastic Packages Derate above T_A = +25°C	 625 5.0	 mW mW/°C
Operating Temperature Range (Ambient)	-20 to +75	°C
Storage Temperature Range	-65 to +150	°C

Maximum Ratings as defined in MIL-S-19500, Appendix A.

ELECTRICAL CHARACTERISTICS (V^+ = 24 Vdc, T_A = +25°C unless otherwise noted)

Characteristic	Pin	Min	Typ	Max	Unit
Regulated Voltage	5	10.3	11	12.2	Vdc
DC Supply Current (V^+ = 9 Vdc, R_S = 0)	5	10	16	24	mA
Quiescent Output Voltage	12	–	5.1	–	Vdc

DYNAMIC CHARACTERISTICS (V^+ = 24 Vdc, T_A = +25°C unless otherwise noted)

Characteristic	Min	Typ	Max	Unit
IF AMPLIFIER AND DETECTOR				
f_o = 4.5 MHz, Δf = ±25 kHz				
AM Rejection* (V_{in} = 10 mV [rms])	40	51	–	dB
Input Limiting Threshold Voltage	–	200	400	μV(rms)
Recovered Audio Output Voltage (V_{in} = 10 mV[rms])	0.5	0.70	–	V(rms)
Output Distortion (V_{in} = 10 mV [rms])	–	0.4	2.0	%
f_o = 5.5 MHz, Δf = ±50 kHz				
AM Rejection* (V_{in} = 10 mV [rms])	40	53	–	dB
Input Limiting Threshold Voltage	–	200	400	μV(rms)
Recovered Audio Output Voltage (V_{in} = 10 mV [rms])	0.5	0.91	–	V(rms)
Output Distortion (V_{in} = 10 mV [rms])	–	0.9	–	%
Input Impedance Components (f = 4.5 MHz, measurement between pins 1 and 2) Parallel Input Resistance Parallel Input Capacitance	 – –	 17 4.0	 – –	 kΩ pF
Output Impedance Components (f = 4.5 MHz, measurement between pin 9 and GND) Parallel Output Resistance Parallel Output Capacitance	 – –	 3.25 3.6	 – –	 kΩ pF
Output Resistance, Detector Pin 7 Pin 8	 – –	 7.5 250	 –	 kΩ Ω
ATTENUATOR				
Volume Reduction Range (See Figure 8) (dc Volume Control = ∞)	60	–	–	dB
Maximum Undesirable Signal (See Note 1) (dc Volume Control = ∞)	–	0.07	1.0	mV
AUDIO AMPLIFIER				
Voltage Gain (V_{in} = 0.1 V(rms), f = 400 Hz)	17.5	20	–	dB
Total Harmonic Distortion (V_o = 2.0 V(rms), f = 400 Hz)	–	2.0	–	%
Output Voltage (THD = 5%, f = 400 Hz)	2.0	3.0	–	V(rms)
Input Resistance (f = 400 Hz)	–	70	–	kΩ
Output Resistance (f = 400 Hz)	–	270	–	Ω

*100% FM, 30% AM Modulation.

Note 1. Undesirable signal is measured at pin 8 when volume control is set for minimum output.

TYPICAL CHARACTERISTICS

(V^+ = 24 V, T_A = +25°C unless otherwise noted)

(f_o = 4.5 MHz)

FIGURE 2 – AM REJECTION

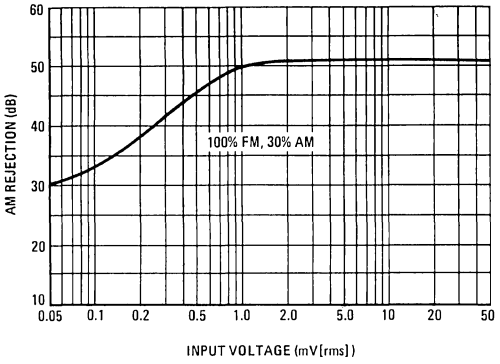


FIGURE 4 – DETECTED AUDIO OUTPUT

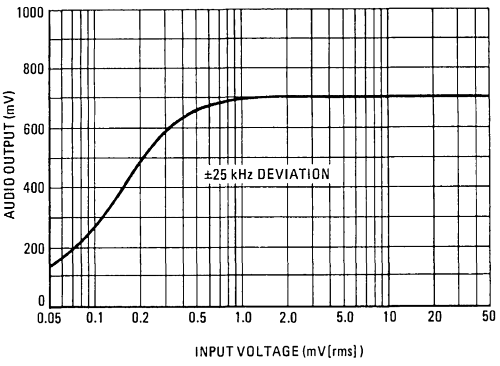
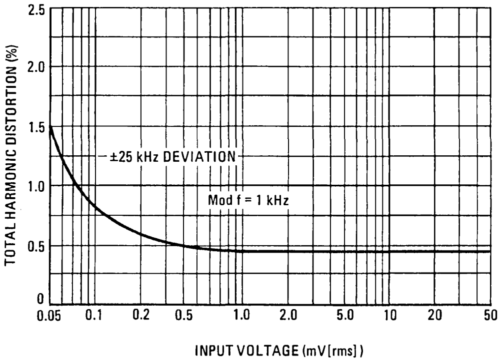


FIGURE 6 – IF AMPLIFIER AND DETECTOR THD



(f_o = 5.5 MHz)

FIGURE 3 – AM REJECTION

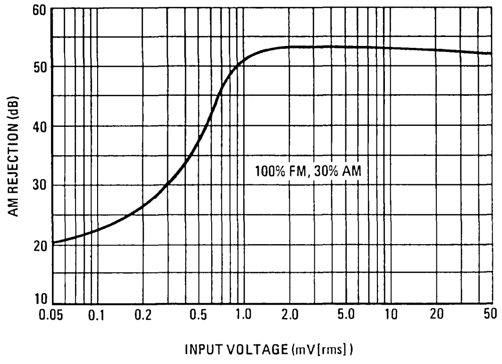


FIGURE 5 – DETECTED AUDIO OUTPUT

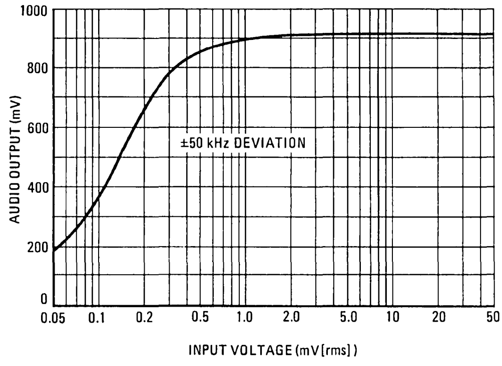
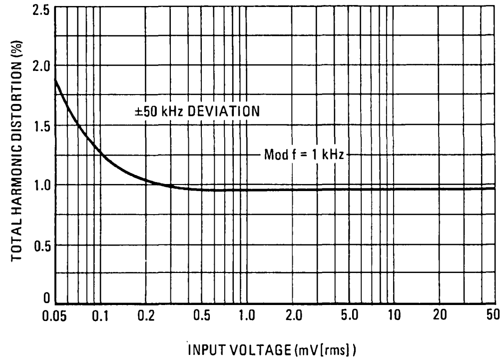


FIGURE 7 – IF AMPLIFIER AND DETECTOR THD



6

TYPICAL CHARACTERISTICS (continued)

FIGURE 8 – GAIN REDUCTION OF ATTENUATOR

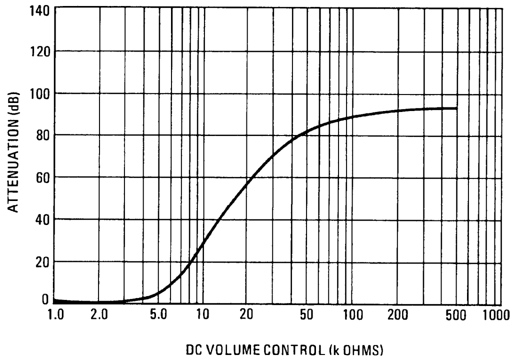


FIGURE 9 – AUDIO AMPLIFIER THD

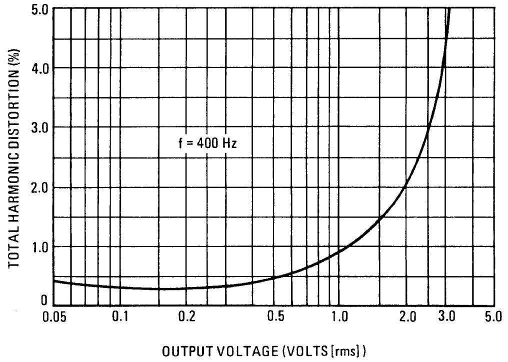


FIGURE 10 – IF FREQUENCY RESPONSE

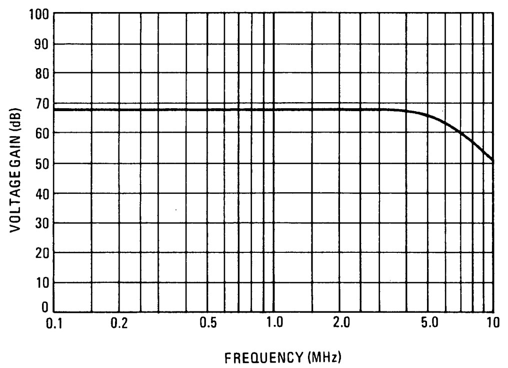


FIGURE 11 – IF FREQUENCY RESPONSE TEST CIRCUIT

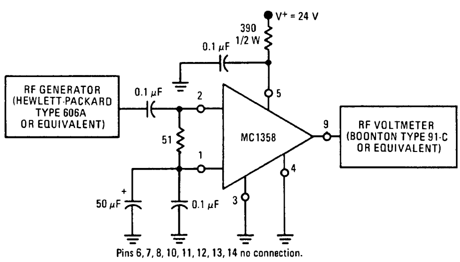


FIGURE 12 – AM REJECTION, DETECTED AUDIO, THD, ATTENUATION TEST CIRCUIT

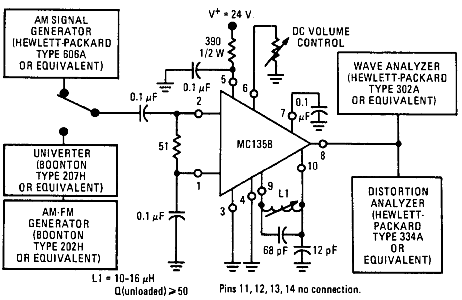


FIGURE 13 – AUDIO VOLTAGE GAIN, AUDIO THD TEST CIRCUIT

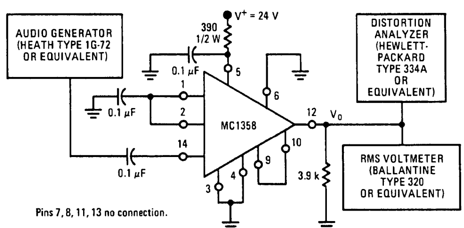
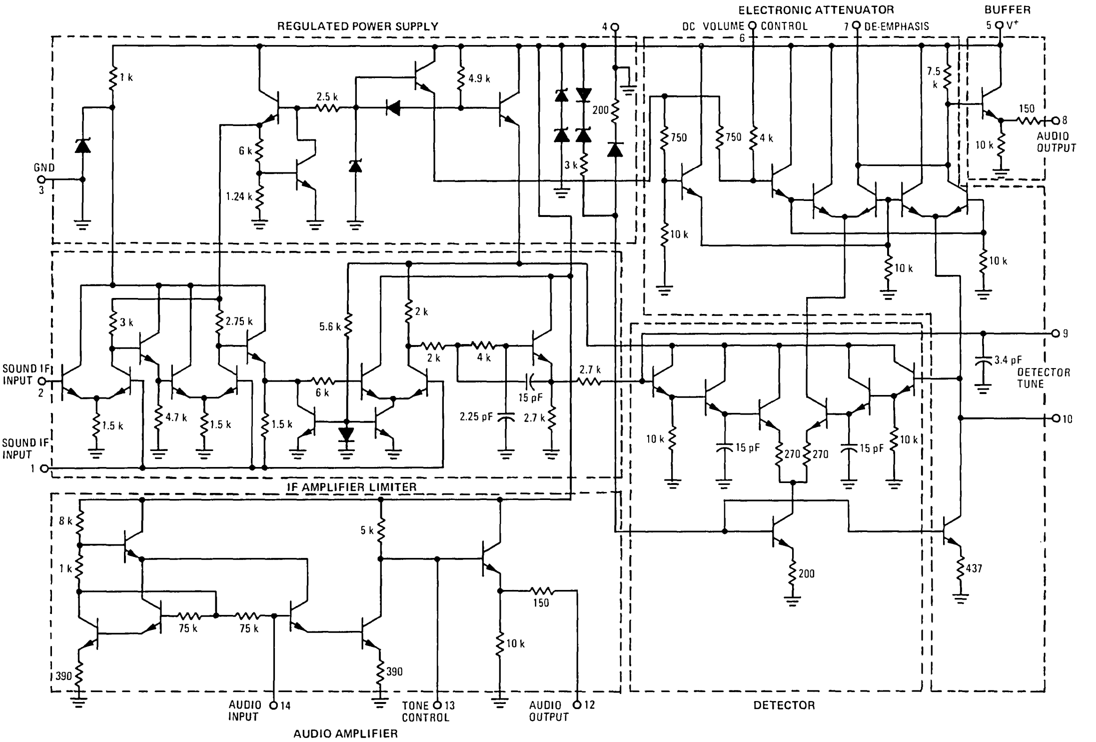


FIGURE 14 — CIRCUIT SCHEMATIC



MC1364

AUTOMATIC FREQUENCY CONTROL

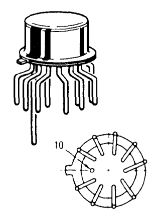
Advance Information

MONOLITHIC TV AUTOMATIC FREQUENCY CONTROL

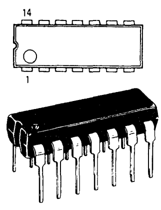
- High Gain Amplifier – 18 mV Input for Rated Output
- Direct Replacement for the CA3064
- Also Available in the 14-Lead Dual In-Line Package

AUTOMATIC FREQUENCY CONTROL

MONOLITHIC SILICON INTEGRATED CIRCUIT

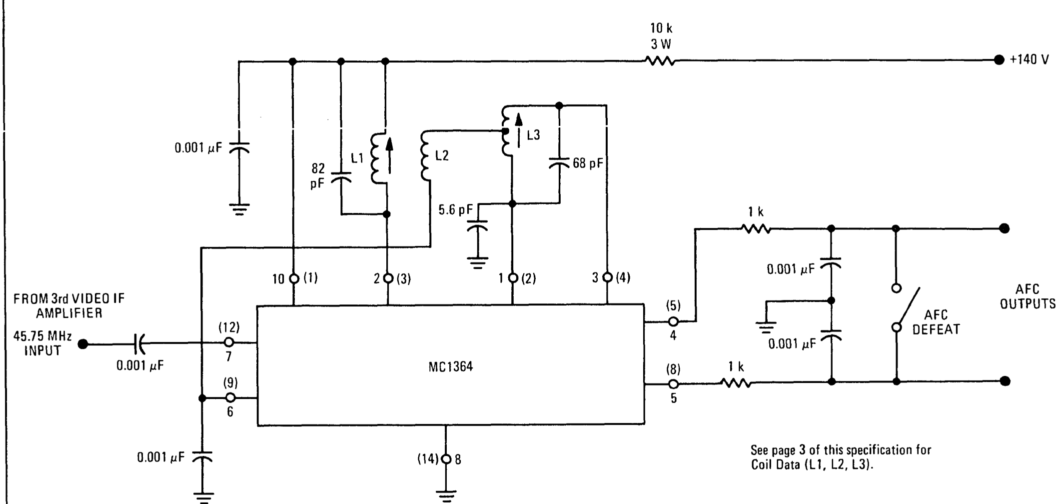


G SUFFIX
METAL PACKAGE
CASE 686



P SUFFIX
PLASTIC PACKAGE
CASE 605
TO-116

FIGURE 1 – TYPICAL APPLICATION CIRCUIT



See page 3 of this specification for Coil Data (L1, L2, L3).

The number without parenthesis is the pin number for the metal package. The number in parenthesis is the pin number for the plastic package.
Metal Package, Pin 9 – no connection
Plastic Package, Pins 6,7,10,11,13 – no connection

This is advance information on a new introduction and specifications are subject to change without notice.
See Packaging Information Section for outline dimensions.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted, see Note 1)

Rating	MC1364G	MC1364P	Unit
Input Signal Voltage (Pin 7 to 8)	+2.0, -10	+2.0, -10	Vdc
Output Collector Voltage (Pins 2 and 8)	20	20	Volts
Power Dissipation (Package Limitation) Derate above T_A = +25°C	680 5.6	625 5.0	mW mW/°C
Operating Temperature Range	-40 to +85	0 to +75	°C
Storage Temperature Range	-65 to +150	-65 to +125	°C

Maximum Ratings as defined in MIL-S-19500, Appendix A.

ELECTRICAL CHARACTERISTICS (V^+ = +30 Vdc, T_A = +25°C, see Test Circuit of Figure 2 unless otherwise noted)

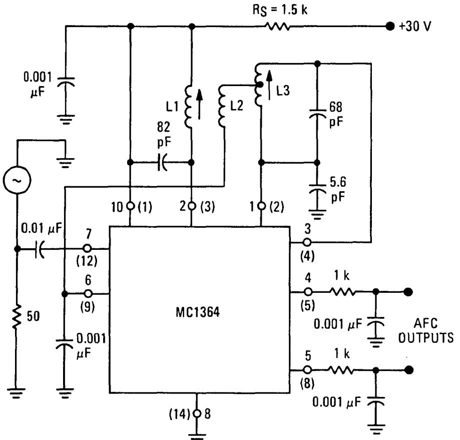
Characteristic	Min	Typ	Max	Unit
Total Device Dissipation	–	140	–	mW
Total Supply Current	–	12	–	mA
Current Drain, Total (Reduce V^+ so that V10 = 10.5 Vdc)	4.0	6.5	9.5	mA
Zener Regulating Voltage	10.9	11.8	12.8	V
Quiescent Current to Pin 2	1.0	2.0	4.0	mA
Quiescent Voltage at Pin 4 or Pin 5	5.0	6.6	8.0	V
Output Offset Voltage (Pin 4 to Pin 5)	-1.0	0	+1.0	V

DESIGN PARAMETERS, TYPICAL VALUES (V^+ = +30 Vdc, R_S = 1.5 k, f = 45.75 MHz)

Parameter	Symbol	Typ	Unit
Input Admittance	y_{11}	0.4 + j1	mmho
Reverse Transfer Admittance	y_{12}	0 + j3.4	μmho
Forward Transfer Admittance	y_{21}	110 + j140	mmhos
Output Admittance (Pin 2)	y_{22}	0.02 + j1	mmho

Note 1. Pin numbers used in the above tables are for the metal package, Case 686. For corresponding pin numbers for the plastic package, Case 605, see the Test Circuit, Figure 2).

FIGURE 2 – TEST CIRCUIT



$$R_S = \frac{V^+ - 11.8}{0.012} \text{ ohms}$$

The number without parenthesis is the pin number for the metal package. The number in parenthesis is the pin number for the plastic package.
Metal Package, Pin 9 - no connection
Plastic Package, Pins 6,7,10,11,13 - no connection

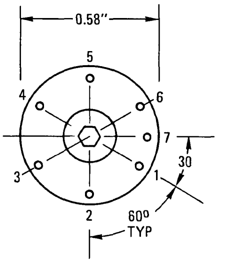
COIL DATA FOR DISCRIMINATOR WINDINGS FOR FIGURES 1 AND 2

L1 – Discriminator Primary: 3-1/6 turns; AWG #20 Enamel-covered wire – close-wound, at bottom of coil form. Inductance of L1 = 0.165 µH; Q_O = 120 at f_o = 45.75 MHz.
Start winding at Terminal #6; finish at Terminal #1. See Notes below.

L2 – Tertiary Windings: 2-1/6 turns; AWG #20 Enamel-covered wire – close-wound over bottom end of L1.
Start winding at Terminal #3; finish at Terminal #4. See Notes below.

L3 – Discriminator Secondary: 3-1/2 turns; AWG #20 Enamel-covered wire, center-tapped, space wound at bottom of coil form.
Start winding at Terminal #2; finish at Terminal #5, connect center tap to Terminal #7. See Notes below.

Notes:
1. Coil Forms; Cylindrical; -0.30" Dia. Max.
2. Tuning Core: 0.250" Dia. x 0.37" Length. Material: Carbinal J or equivalent.
3. Coil Form Base: See drawing below.
4. End of coil nearest terminal board to be designated the winding start end.
5. Mount the coils 3/4" apart, center to center.



TYPICAL CHARACTERISTICS
(See Test Circuit of Figure 2)

FIGURE 3 – TYPICAL NARROW BAND DYNAMIC CHARACTERISTICS

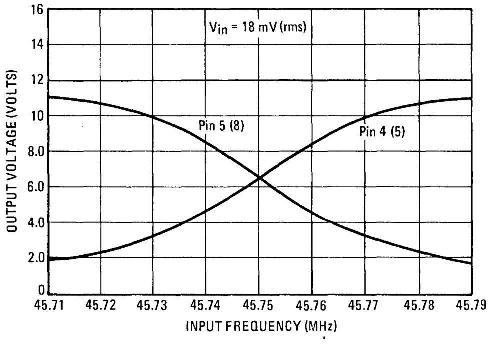


FIGURE 4 – TYPICAL WIDE BAND DYNAMIC CHARACTERISTICS

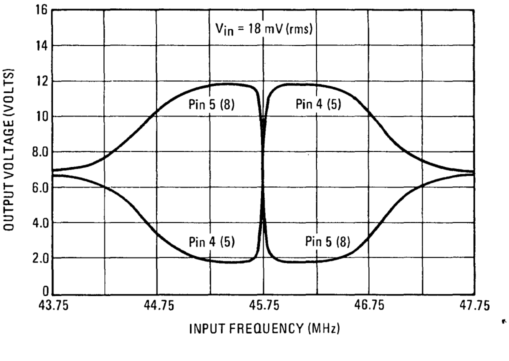
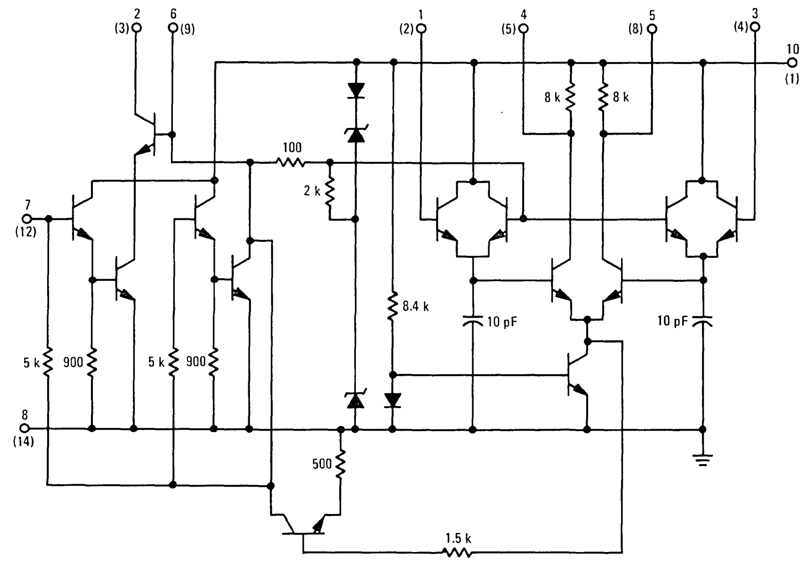


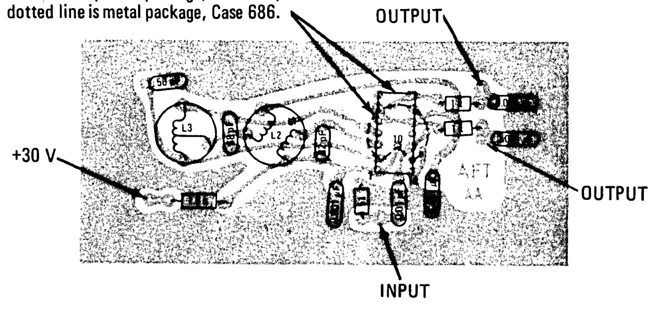
FIGURE 5 – CIRCUIT SCHEMATIC



The number without parenthesis is the pin number for the metal package. The number in parenthesis is the pin number for the plastic package.

Metal Package, Pin 9 - no connection
Plastic Package, Pins 6,7,10,11,13 - no connection

FIGURE 6 – PRINTED CIRCUIT BOARD AND PARTS ARRANGEMENT
(Copper Side)



AUDIO DRIVER

MC1380P

Advance Information

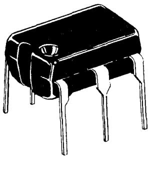
MONOLITHIC CLASS A AUDIO DRIVER

. . . designed to drive a germanium power transistor output stage in an auto radio. It permits direct-coupling to the output stage; this allows a wide tolerance on current gain and leakage current of the external output transistor when used within an external feedback loop.

- High Gain (280 V/V typ)
- Good Output Current Capability (58 mA typ)

CLASS A AUDIO DRIVER

SILICON MONOLITHIC INTEGRATED CIRCUIT

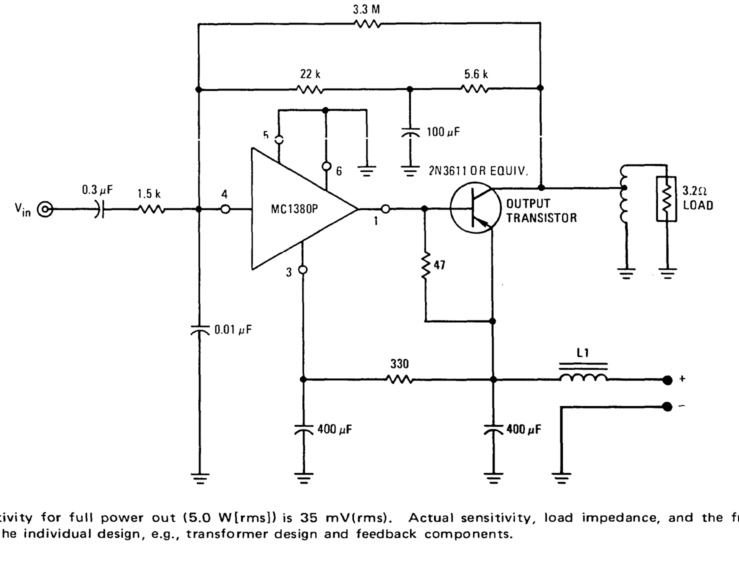


CASE 627

PLASTIC PACKAGE

6

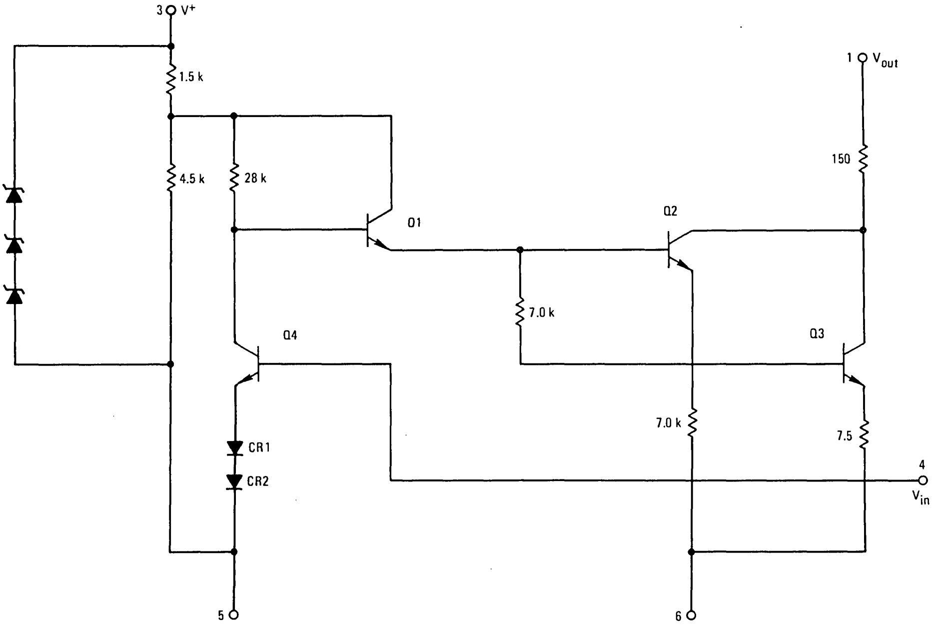
FIGURE 1 – TYPICAL APPLICATION (V^+ = 13.6 Vdc)



The typical sensitivity for full power out (5.0 W[rms]) is 35 mV(rms). Actual sensitivity, load impedance, and the frequency response is dependent upon the individual design, e.g., transformer design and feedback components.

See Packaging Information Section for outline dimensions.

FIGURE 2 – CIRCUIT SCHEMATIC



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Value	Unit
Power Supply Voltage	+18	Vdc
Power Dissipation (Package Limitation)	625	mW
Derate above T_A = +25°C	5.0	mW/°C
Operating Temperature Range	-40 to +75	°C
Storage Temperature Range	-40 to +85	°C

Maximum Ratings as defined in MIL-S-19500, Appendix A.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Min	Typ	Max	Unit
DC Input Voltage (Test per Figure 3)	1.9	–	2.5	Vdc
Open-Loop Voltage Gain (e_{in} (ac input) - 100 µV (rms), f = 1 kHz at terminal No. 4) (Test per Figure 4)	130	–	–	V/V
Current Output Capability (Test per Figure 5)	30	–	–	mA
Leakage Current (Test per Figure 6)	–	–	10	mAdc

TEST CIRCUITS

FIGURE 3 – DC INPUT VOLTAGE

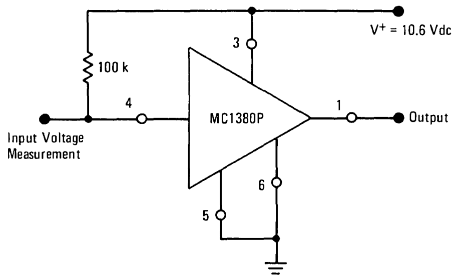


FIGURE 4 – OPEN-LOOP VOLTAGE GAIN

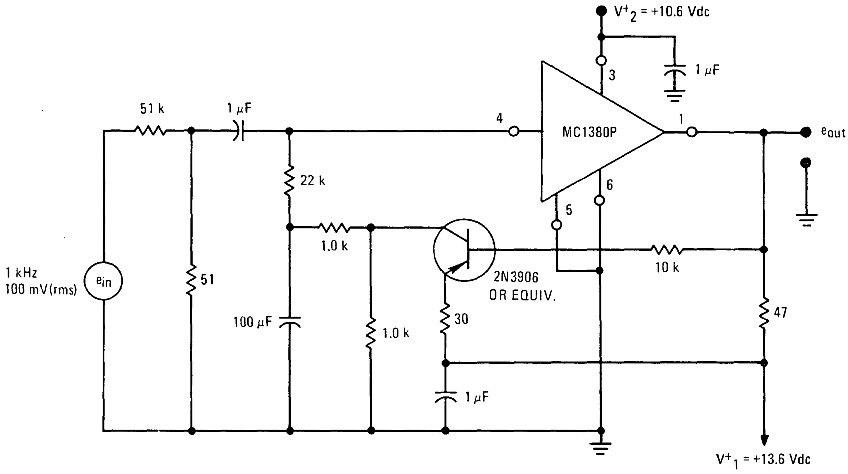


FIGURE 5 – OUTPUT CURRENT CAPABILITY

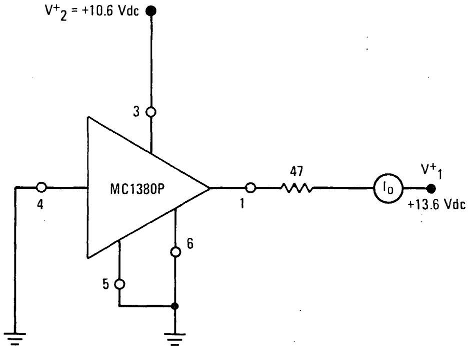
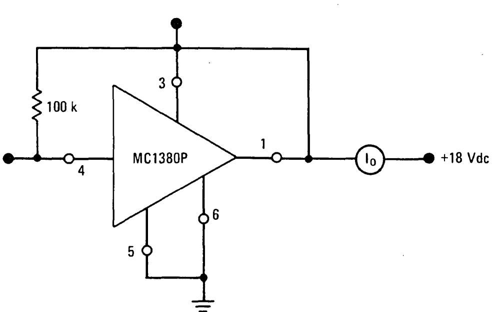


FIGURE 6 – LEAKAGE CURRENT



TV COLOR PROCESSING CIRCUIT

MC1398P

TV COLOR PROCESSING CIRCUIT

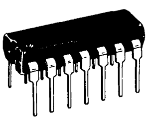
. . . a chroma IF amplifier with automatic chroma control, color killer, dc chroma control, and injection lock reference system followed by dc hue control.

MC1398P is a monolithic device designed for use in solid-state color television receivers.

- Minimum Number of External Components
- DC Control of Both Chroma Amplitude and Hue Shift
- Crystal-Controlled Internal Feedback Oscillator
- Built-in Noise Immunity
- Schmitt Trigger Color Killer
- Automatic Chroma Control
- Internal Burst Gate and Gate Pulse Shaping Circuit
- High Oscillator Lock-in Sensitivity
- Built-in Supply Regulation

TV COLOR PROCESSING CIRCUIT

MONOLITHIC SILICON INTEGRATED CIRCUIT



PLASTIC PACKAGE
CASE 605
TO-116

6

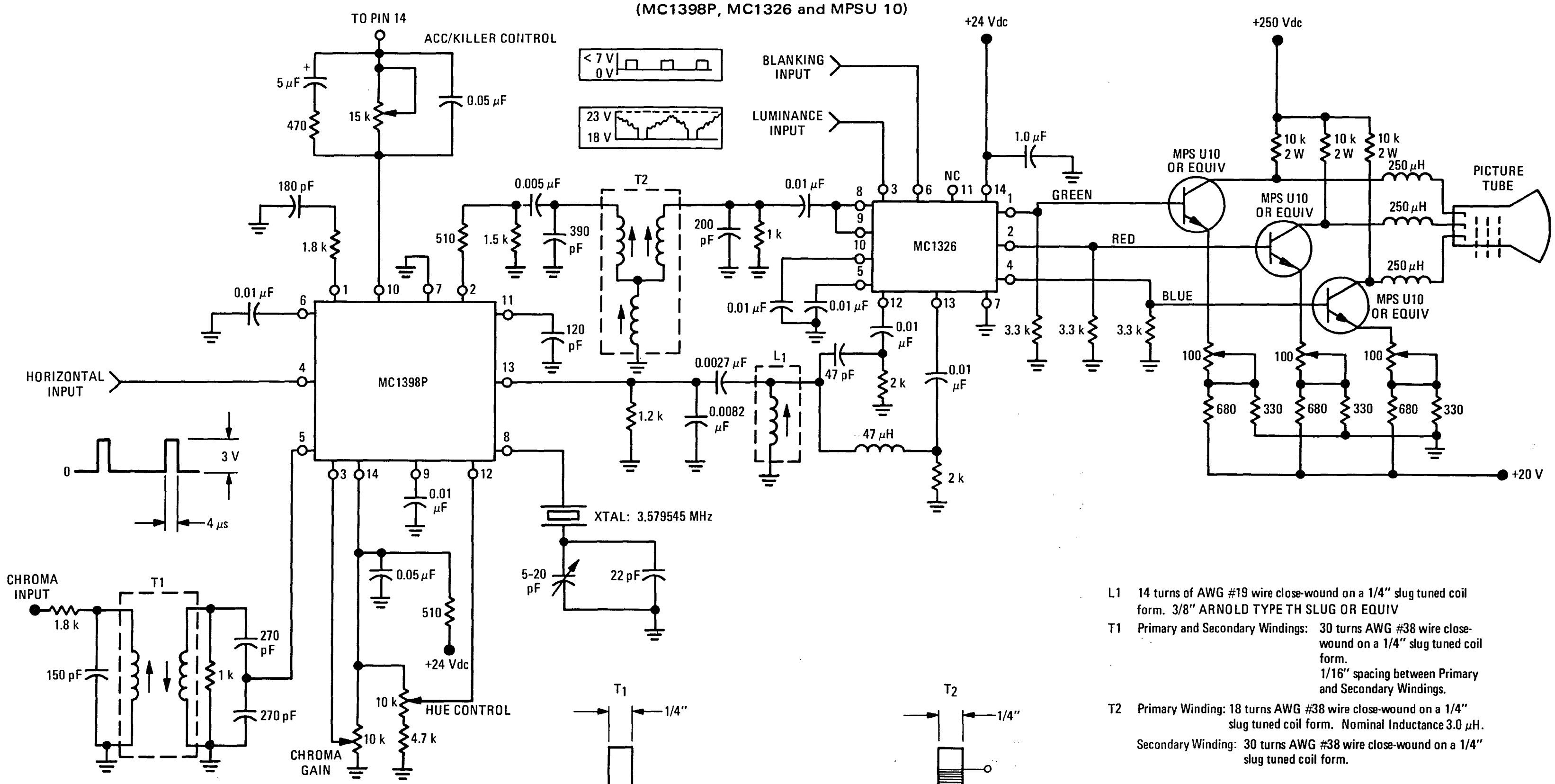
MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Value	Unit
Power Supply Current	32	mAdc
Horizontal Pulse Input Current	250	μA Peak
Power Dissipation (package limitation) Derate above T_A = +25°C	625 5.0	mW mW/°C
Operating Temperature Range (Ambient)	-20 to +75	°C
Storage Temperature Range	-65 to +150	°C

Maximum Ratings as defined in MIL-S-19500, Appendix A.

See Packaging Information Section for outline dimensions.

FIGURE 1 – TYPICAL CHROMA APPLICATIONS' CIRCUIT
(MC1398P, MC1326 and MPSU 10)



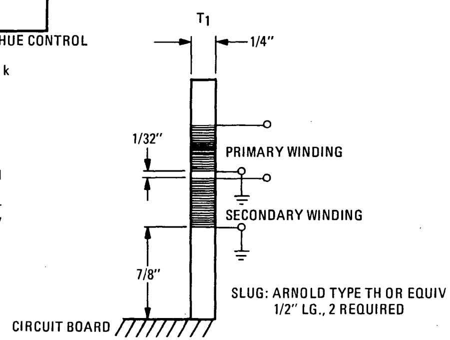
L1 14 turns of AWG #19 wire close-wound on a 1/4" slug tuned coil form. 3/8" ARNOLD TYPE TH SLUG OR EQUIV

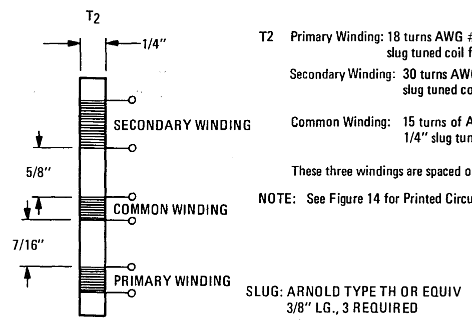
T1 Primary and Secondary Windings: 30 turns AWG #38 wire close-wound on a 1/4" slug tuned coil form.
1/16" spacing between Primary and Secondary Windings.

T2 Primary Winding: 18 turns AWG #38 wire close-wound on a 1/4" slug tuned coil form. Nominal Inductance 3.0 µH.
Secondary Winding: 30 turns AWG #38 wire close-wound on a 1/4" slug tuned coil form.
Common Winding: 15 turns of AWG #38 wire close-wound on a 1/4" slug tuned coil form.

These three windings are spaced on the form to have minimum mutual coupling.

NOTE: See Figure 14 for Printed Circuit Board layout (Copper Side)



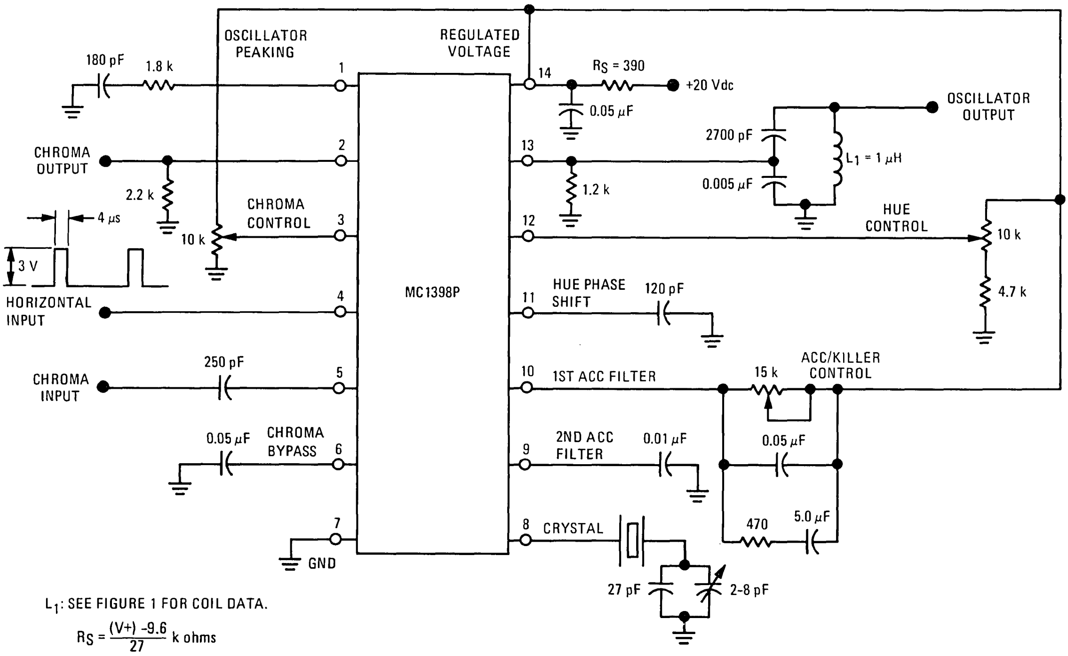


This coil data is intended as an aid only. It is expected that many designers will want to use other approaches.
The simplest method of turning the chroma IF "ON" for sweep alignment, is to supply an external bias of about 2.5 V to pin 9.

ELECTRICAL CHARACTERISTICS (V^+ = +20 Vdc, R_S = 390 ohms, T_A = +25°C unless otherwise noted.)

Characteristic	Min	Typ	Max	Unit
Regulated Voltage	9.0	9.6	11.5	Vdc
Power Supply Current	–	27	–	mAdc
Maximum Chroma Output ($E_{(pin\ 10)}$ = 8.6 Vdc, $E_{(pin\ 3)}$ = 9.6 Vdc @ e_{in} = 0)	0.8	1.75	–	Vp-p
Maximum Chroma Gain $E_{(pin\ 10)}$ = 8.6 Vdc @ e_{in} = 0 $E_{(pin\ 3)}$ = 9.6 Vdc @ e_{in} = 0	34	40	–	dB
ACC Range $E_{(pin\ 10)}$ = 8.6 Vdc @ e_{in} = 0, -1.0 dB down from maximum output	–	23	–	dB
Chroma Burst Level to Turn Killer "On" (Pin 10 Voltage = 8.6 Vdc @ e_{in} = 0)	–	1.4	–	mVp-p
Manual Chroma Gain Control Range $\Delta V_{(pin\ 3)}$ ($V_{(pin\ 14)}$ to 0 Vdc)	50	60	–	dB
Chroma Input Resistance	–	2.3	–	k ohms
Chroma Input Capacitance	–	13	–	pF
Chroma Output Impedance	–	15	–	ohms
Horizontal Input Pulse	2.2	3.0	4.0	V_p
Oscillator Output	180	208	–	mV (rms)
Oscillator Output Impedance	–	15	–	ohms
Hue Control Range $\Delta V_{(pin\ 12)}$ ($V_{(pin\ 14)}$ to 4.3 Vdc)	100	126	–	degrees

FIGURE 2 – MC1398P TEST CIRCUIT



L_1: SEE FIGURE 1 FOR COIL DATA.

$$R_S = \frac{(V+) - 9.6}{27} \text{ k ohms}$$

TYPICAL CHARACTERISTICS

(T_A = +25°C unless otherwise noted)
(Figures 3 through 8, See Test Circuit of Figure 2.)

FIGURE 3 – INPUT/OUTPUT CHARACTERISTICS

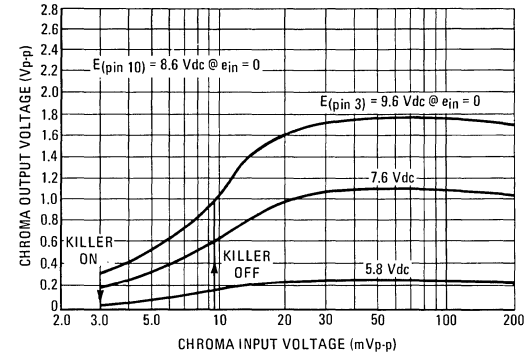


FIGURE 4 – INPUT/OUTPUT CHARACTERISTICS

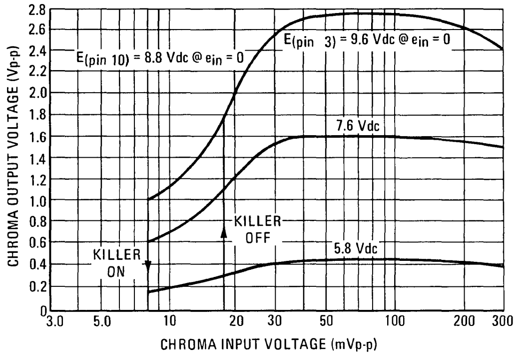


FIGURE 5 – KILLER OPERATION

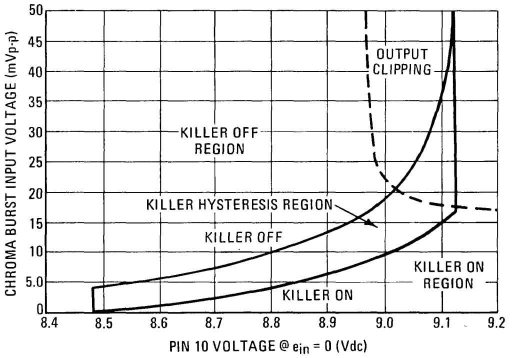
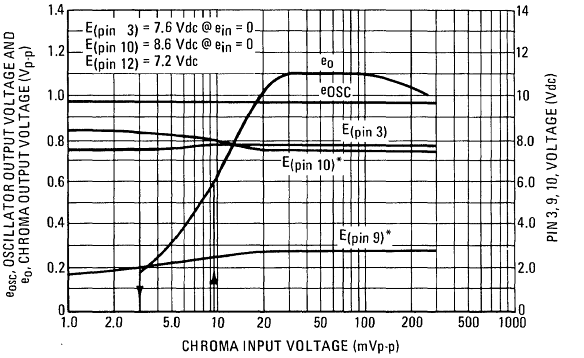


FIGURE 6 – CIRCUIT OUTPUT PARAMETERS versus CHROMA INPUT VOLTAGE



*$E_{(pin\ 9,\ 10)}$ is a function of Chroma Burst Input Voltage (e_{burst}) which is equal to 43% of the Chroma Input Voltage (e_{in}).

FIGURE 7 – HUE CONTROL OPERATION

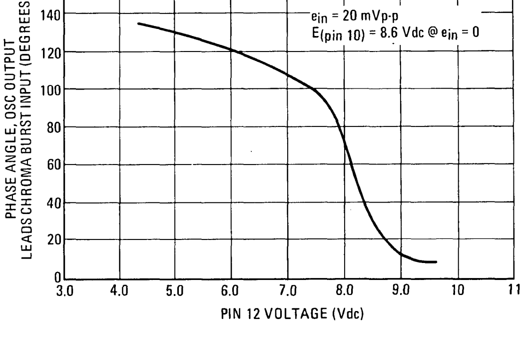
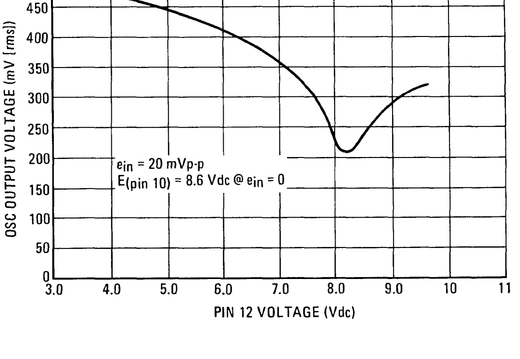


FIGURE 8 – OSCILLATOR OUTPUT versus PIN 12 VOLTAGE



6

TYPICAL CHARACTERISTICS

(Figures 9 through 12, See Circuit of Figure 1.)

FIGURE 9 – NTSC SIGNAL AT CHROMA INPUT (PIN 5)

50 mV/DIV

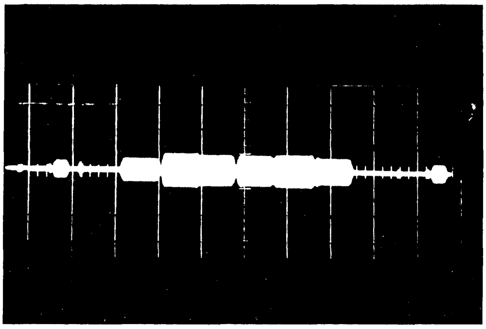
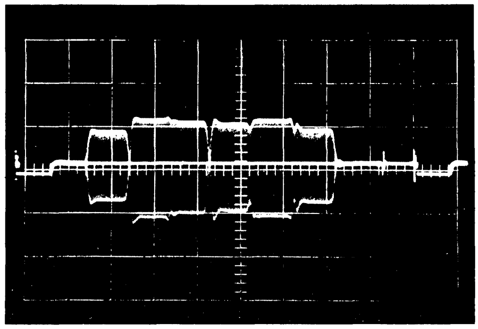


FIGURE 10 – NTSC SIGNAL AT CHROMA OUTPUT (PIN 2)

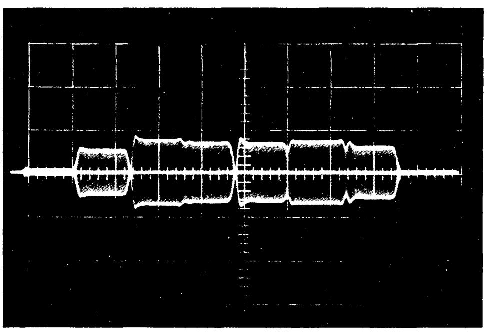
1.0 VOLT/DIV



e_{in} = 40 mVp-p
$E_{(pin\ 10)}$ = 8.6 Vdc @ e_{in} = 0
$E_{(pin\ 3)}$ = 9.6 Vdc (MAXIMUM GAIN)

FIGURE 11 – NTSC SIGNAL OUTPUT AT T_2

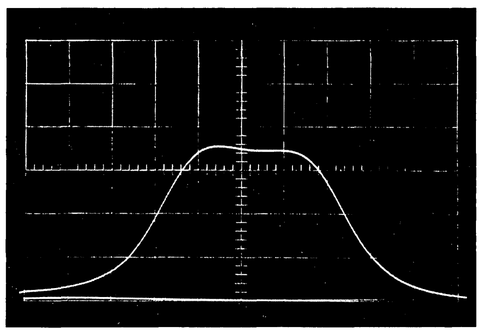
1.0 VOLT/DIV



e_{in} = 40mVp-p
$E_{(pin\ 10)}$ = 8.6 Vdc @ e_{in} = 0
$E_{(pin\ 3)}$ = 9.6 Vdc (MAXIMUM GAIN)

FIGURE 12 – OVERALL RESPONSE OF APPLICATIONS CIRCUIT (SEE FIGURE 1)

0.5 VOLT/DIV



500 kHz/DIV

e_{in} = 40 mVp-p (measured at pin 5)
$E_{(pin\ 10)}$ = 8.6 Vdc @ e_{in} = 0
$E_{(pin\ 3)}$ = 9.6 Vdc (MAXIMUM GAIN)

CENTER 3.58 MHz

MC1398 CIRCUIT DESCRIPTION

MC1398 is capable of providing the entire color processing function for television color receivers.

The chroma amplifier (Q2, Q3, Q9, Q8, Q17, Q18) in conjunction with the chroma gain and output section (Q10, Q11, Q15, Q21, Q14, Q20) provide 40 dB of gain. In addition, a wide range of chroma gain adjustment is possible through the use of a dc control voltage on pin 3. Attenuation of the chroma signal is due to current-sharing in transistors Q11 and Q15.

A low impedance chroma output (pin 2) is provided through the use of compound emitter-followers Q14 and Q20.

The burst gating and fill-in section is used to "gate" out the reference burst information to lock the local 3.579545 MHz oscillator with the reference. The gating differential amplifier (Q5 and Q7) must be supplied with a 4 μs horizontal pulse of 3.0 V peak amplitude. To prevent excessive level variations in the chroma signal during the gating operation the fill-in circuit (Q22, Q26, Q23) is used.

The primary function of the oscillator section is to regenerate the 3.579545 MHz chroma subcarrier in a manner to preserve a frequency and phase lock with the incoming reference burst. The oscillator is designed so that an output level (Q50) is provided proportional to the level of the incoming burst. This signal is utilized in the ACC section to develop an ACC voltage.

The reference burst is supplied to a differential amplifier (Q29, Q50) by emitter followers Q27 and Q28. This differential amplifier (Q29, Q50) will have an output only at the frequency of the crystal connected to pin 8 (3.579545 MHz). All other inputs to Q29 and Q50 will be rejected due to the common-mode rejection (CMR) of the differential amplifier. R32 and C1 are used to enhance the CMR noise performance of the oscillator. Q35 together with its associated network connected to pin 1 provides the needed feedback to sustain oscillation. The oscillator circuit exhibits high lock-up sensitivity (200 μV) over all ranges of usable chroma input.

Hue control and oscillator output sections are supplied from the oscillator section (Q38 and Q39) with two "limited" signals, 180 degrees out of phase. The oscillator voltage from Q39 is initially phase shifted by the RC time constant; determined by the value of the capacitor connected to pin 11 and R36.

The oscillator signal developed across R51 is the algebraic sum of the two oscillator signal inputs. Phase shifting of the output results from the addition of the two input signals in the two differential amplifiers Q30, Q31 and Q34, Q37. Summing of these two oscillator signals is controlled by the dc bias applied to pin 12. A low impedance oscillator output signal (pin 13) is provided by a compound emitter-follower composed of Q40 and Q41.

The ACC circuit provides two functions. This section is used to develop a dc voltage which is proportional to the input signal level. Secondly, through the use of a potentiometer connected to pin 10, the operating point of Q47 and Q46 can be adjusted; thereby determining the operating threshold of the killer section.

The first function is provided by rectifying the 3.579545 MHz oscillator signal in the offset differential amplifier of Q42 and Q45. Filtering of the ACC dc voltage is accomplished by capacitors connected to pins 9 and 10. ACC voltage is supplied to Q9 in the chroma amplifier section to provide the required gain control action.

The killer section is used to eliminate chroma output (pin 2) during monochrome broadcasts or low-level "noisy" color broadcasts.

A positive killer action is provided through the use of a Schmitt trigger (Q19, Q24, Q25) contained in this section. In addition, a desirable 3 dB "turn on", "turn off" hysteresis is accomplished in the trigger circuit.

Control voltage for the killer is developed in the ACC section and the operating threshold is adjustable by controlling the dc voltage at pin 10.

The killer action is produced when Q25 is driven into saturation. This saturation voltage effectively turns off Q15 and Q21 in the chroma gain/output section.

Bias and voltage regulator sections are used to supply internal dc bias voltages for the device. In addition, through the use of an internal regulator the MC1398 can be operated over a wide range of supply voltages.

FIGURE 13 – MC1398 CIRCUIT SCHEMATIC

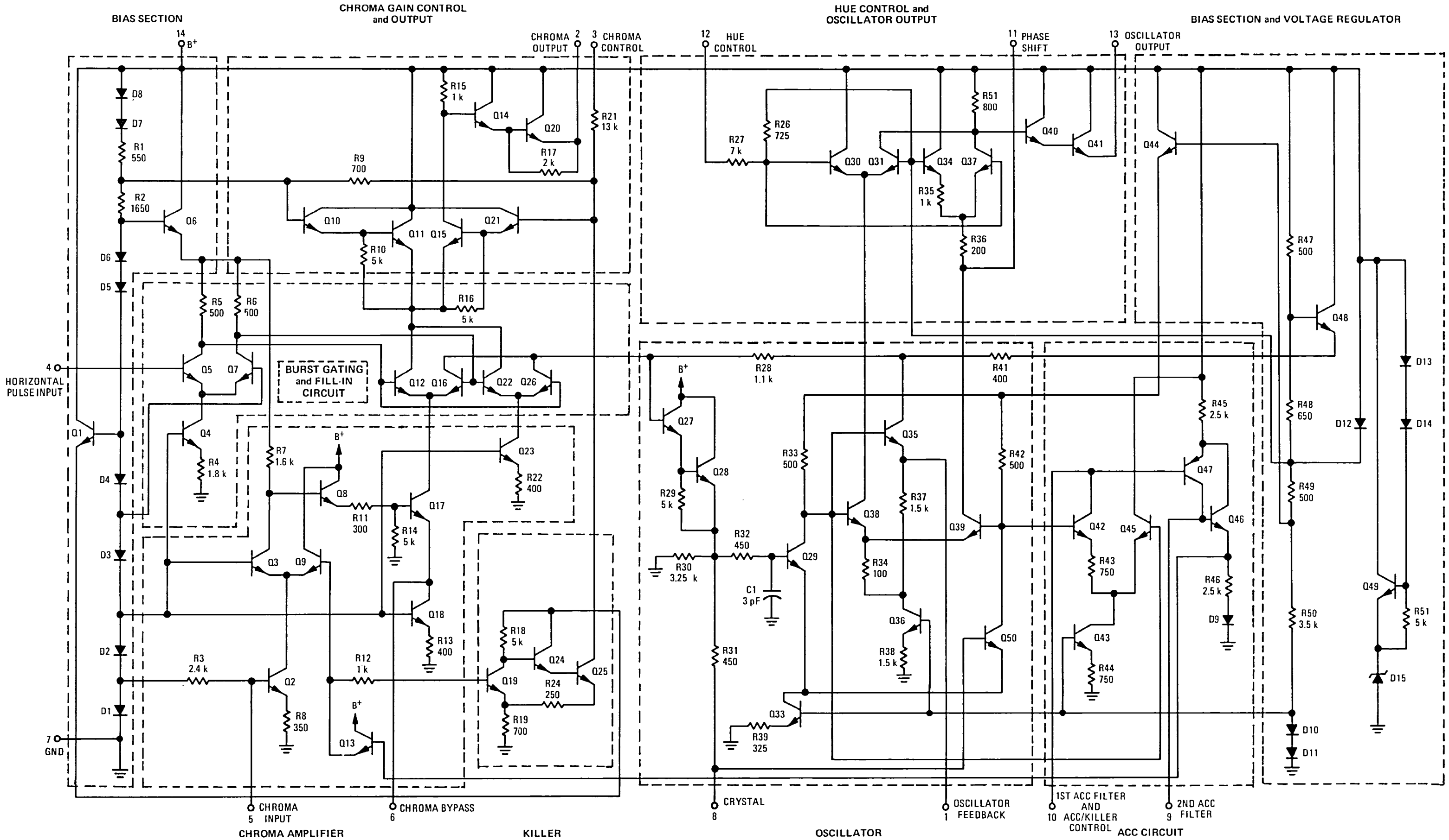
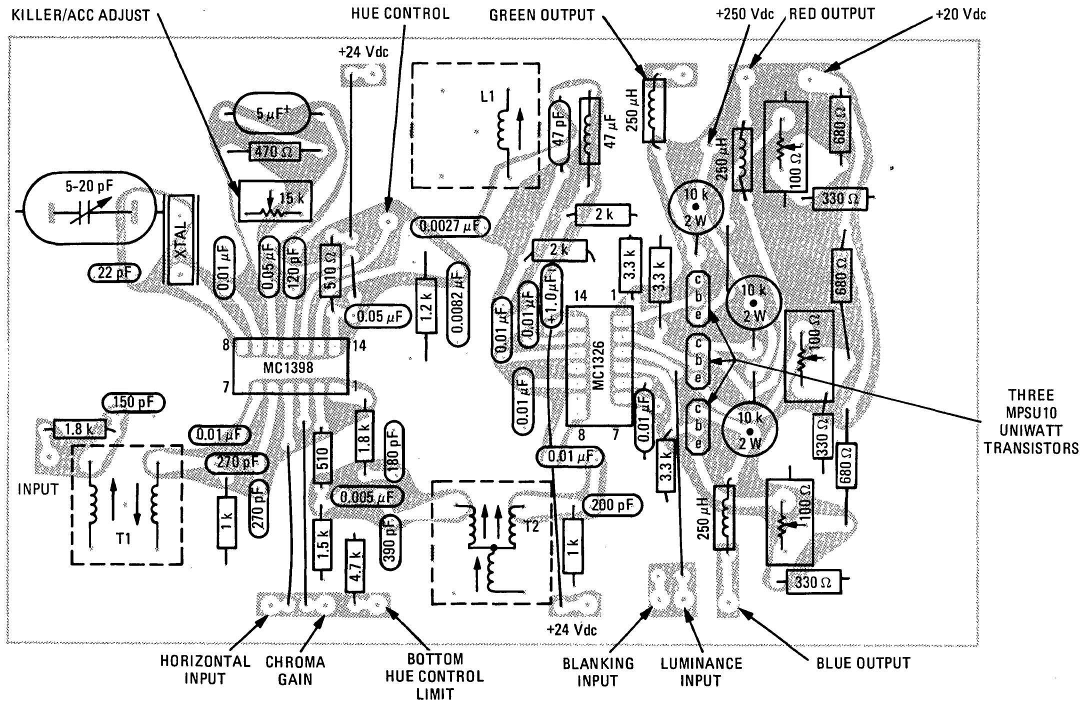


FIGURE 14 — PRINTED CIRCUIT LAYOUT OF MC1398P, MC1326, and MPSU10 TRANSISTORS



NOTES:
All resistors are 1/4 W unless otherwise noted.
The three 10 k - 2 W resistors are positioned on end.
See Figure 1 for circuit schematic and L1, T1 and T2 specifications.
(Copper Side Shown)

MC1398P APPLICATIONS INFORMATION

MC1398P is a multifunction circuit with considerable gain associated with the chroma amplifier and oscillator sections. It is important to the circuit layout utilizing the MC1398P that the chroma amplifier, oscillator, and oscillator output/hue section grounds are separated from each other. Ground loop problems will interfere with oscillation stability and lock-up if this precaution is not observed.

Care must be exercised to avoid coupling from the oscillator output coil (pin 13) to the crystal circuitry connected to pin 8. Stray coupling of these two points can result in excessive oscillator shift; or in some cases, oscillator drop-out during adjustment of the hue control.

A suitable circuit layout for the MC1398P is shown in Figure 14.

An adjustable capacitor (1.5—20 pF in parallel with a fixed 22 pF capacitor) is shown in series with the 3.58 MHz crystal. This capacitor is used to adjust the oscillator exactly on frequency, and insures excellent oscillator lock-up. However, acceptable oscillator performance can be obtained with a fixed value of capacitance (this value is dependent on the designers' choice of crystals).

MC1414L

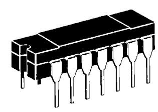
DUAL DIFFERENTIAL COMPARATOR

MONOLITHIC DUAL DIFFERENTIAL VOLTAGE COMPARATOR

. . . designed for use in level detection, low-level sensing, and memory applications.

Typical Amplifier Features:

- Two Separate Outputs
- Strobe Capability
- High Output Sink Current — 1.6 mA min Each Comparator
- Differential Input Characteristics:
  Input Offset Voltage = 1.5 mV
  Offset Voltage Drift = 5.0 μV/^{o}C
- Short Propagation Delay Time — 40 ns
- Output Compatible with All Saturating Logic Forms
  V_{out} = +3.2 V to -0.5 V typical

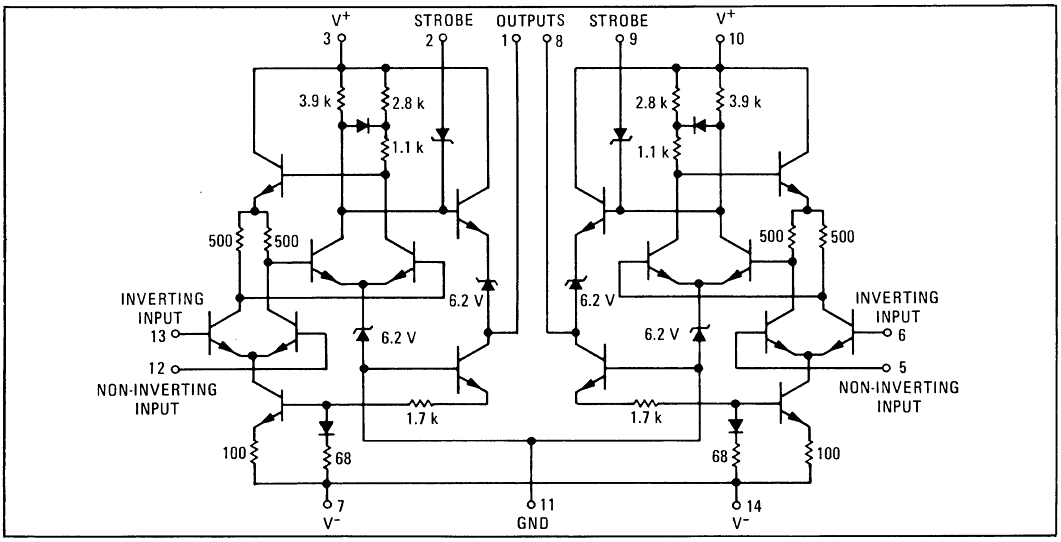


L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+ V^-	+14 -7.0	Vdc Vdc
Differential Input Signal	V_{in}	±5.0	Volts
Common Mode Input Swing	CMV_{in}	±7.0	Volts
Peak Load Current	I_L	10	mA
Power Dissipation (package limitation) Ceramic Dual In-Line Package Derate above T_A = 50°C	P_D	 750 6.0	 mW mW/°C
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

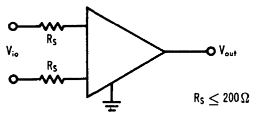
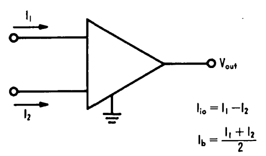
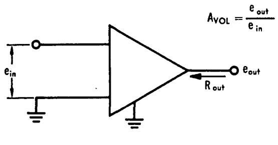
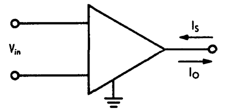
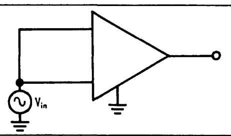
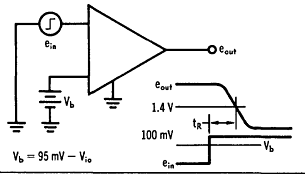
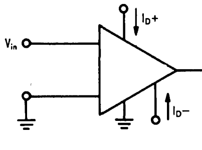
CIRCUIT SCHEMATIC



See Packaging Information Section for outline dimensions.

MC1414L (continued)

ELECTRICAL CHARACTERISTICS ($V+ = +12$ Vdc, $V^- = -6$ Vdc, $T_A = 25°C$ unless otherwise noted) (Each Comparator)

Characteristic Definitions (linear operation)	Characteristic	Symbol	Min	Typ	Max	Unit
	Input Offset Voltage $V_{out} = 1.4$ Vdc, $T_A = 25°C$ $V_{out} = 1.8$ Vdc, $T_A = 0°C$ $V_{out} = 1.0$ Vdc, $T_A = +75°C$	V_{io}	 - - -	 1.5 - -	 5.0 6.5 6.5	mVdc
	Temperature Coefficient of Input Offset Voltage	TC_{Vio}	-	5.0	-	µV/°C
	Input Offset Current $V_{out} = 1.4$ Vdc, $T_A = 25°C$ $V_{out} = 1.8$ Vdc, $T_A = 0°C$ $V_{out} = 1.0$ Vdc, $T_A = +75°C$	I_{io}	 - - -	 1.0 - -	 5.0 7.5 7.5	µAdc
	Input Bias Current $V_{out} = 1.4$ Vdc, $T_A = 25°C$ $V_{out} = 1.8$ Vdc, $T_A = 0°C$ $V_{out} = 1.0$ Vdc, $T_A = +75°C$	I_b	 - - -	 15 18 -	 25 40 40	µAdc
	Open Loop Voltage Gain $T_A = 25°C$ $T_A = 0$ to $+75°C$	A_{VOL}	 1000 800	 1500 -	 - -	V/V
	Output Resistance	R_{out}	-	200	-	ohms
	Differential Voltage Range	V_{in}	±5.0	-	-	Vdc
	Positive Output Voltage $V_{in} \geqq 5.0$ mV, $0 \leqq I_o \leqq 5.0$ mA	V_{OH}	2.5	3.2	4.0	Vdc
	Negative Output Voltage $V_{in} \geqq -5.0$ mV	V_{OL}	-1.0	-0.5	0	Vdc
	Output Sink Current $V_{in} \geqq -5.0$ mV, $V_{out} \geqq 0$, $T_A = 0$ to $+75°C$	I_s	1.6	2.5	-	mAdc
	Input Common Mode Range $V^- = -7.0$ Vdc	CMV_{in}	±5.0	-	-	Volts
	Common Mode Rejection Ratio $V^- = -7.0$ Vdc, $R_S \leqq 200\ \Omega$	CM_{rej}	70	100	-	dB
	Propagation Delay Time For Positive and Negative Going Input Pulse	t_{pd}	-	40	-	ns
	Total Power Supply Current $V_{out} \leqq 0$ Vdc	I_D+ I_D-	- -	12.8 11	18 14	mAdc
	Total Power Consumption		-	230	300	mW

TYPICAL CHARACTERISTICS
(Each Comparator)

FIGURE 1 – VOLTAGE TRANSFER CHARACTERISTICS

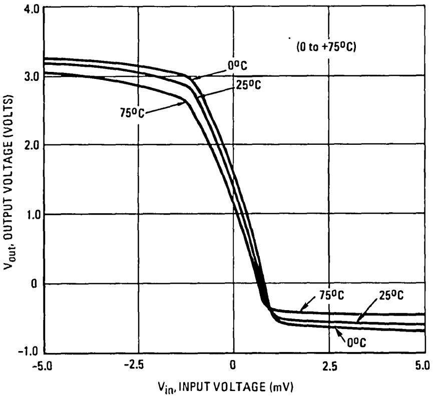


FIGURE 2 – INPUT OFFSET VOLTAGE versus TEMPERATURE

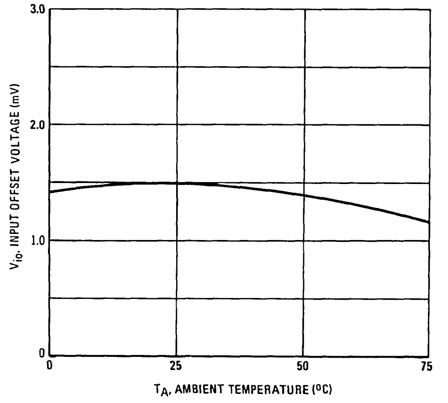


FIGURE 3 – INPUT OFFSET CURRENT versus TEMPERATURE

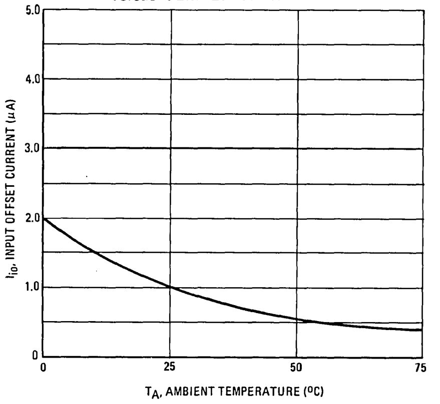


FIGURE 4 – INPUT BIAS CURRENT versus TEMPERATURE

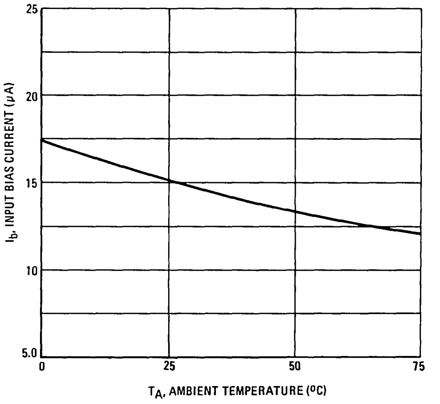


FIGURE 5 – GAIN VARIATION WITH POWER SUPPLY VOLTAGE

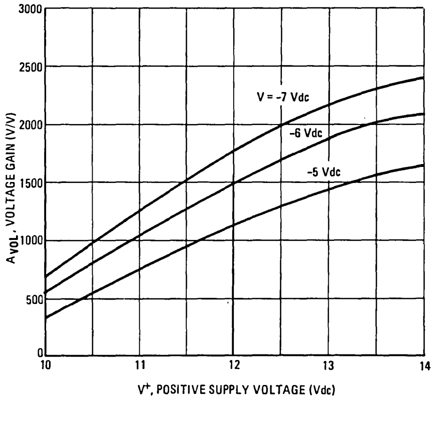


FIGURE 6 – VOLTAGE GAIN versus TEMPERATURE

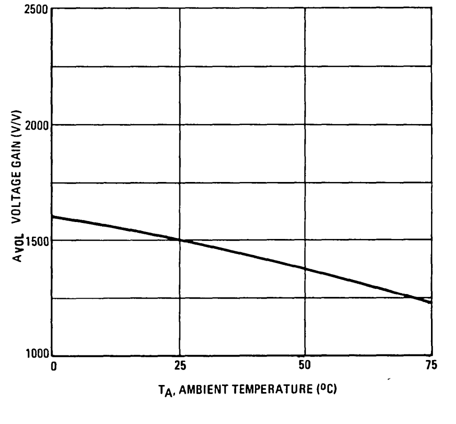


FIGURE 7 — RESPONSE TIME

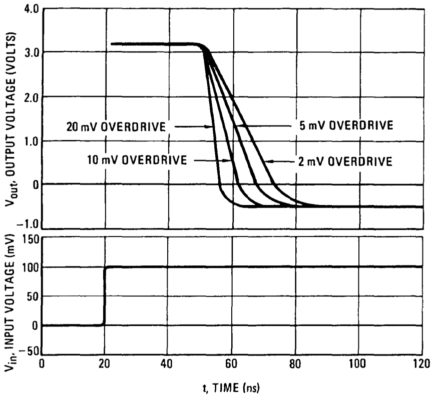


FIGURE 8 — POWER DISSIPATION versus TEMPERATURE

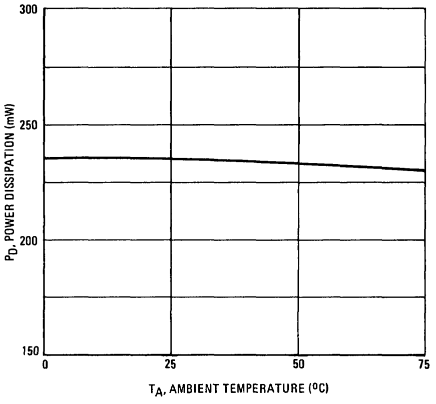


FIGURE 9 — RECOMMENDED SERIES RESISTANCE versus MRTL LOADS

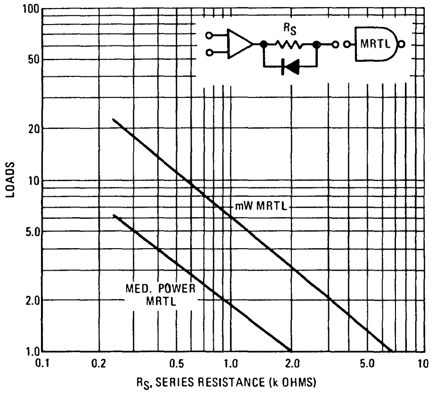


FIGURE 10 — SINK CURRENT versus TEMPERATURE

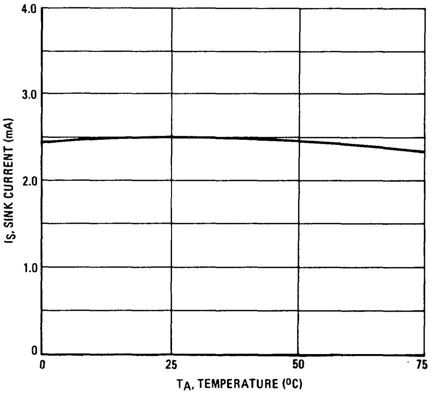
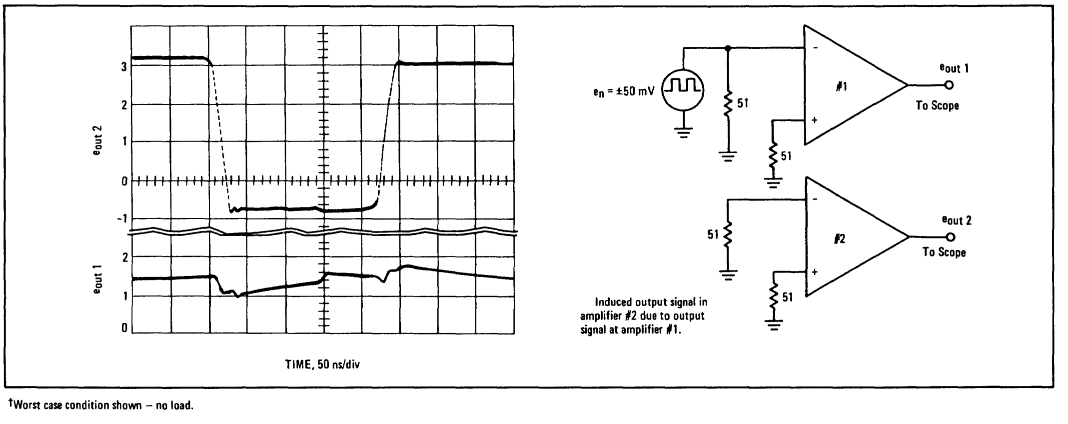


FIGURE 11 — CROSSTALK†

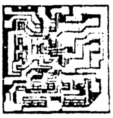


†Worst case condition shown — no load.

MC1430
MC1431

OPERATIONAL AMPLIFIERS

A MONOLITHIC SILICON EPITAXIAL PASSIVATED OPERATIONAL AMPLIFIER



. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

- High Open Loop Gain
  A_{VOL} = 74 dB typical
- Large Output Voltage Swing
  typically ±5 V @ ±6 V Supply
- Low Output Impedance
  Z_{out} = 25 ohms typical
- High Slew Rate
  typically 4.5 V/µs

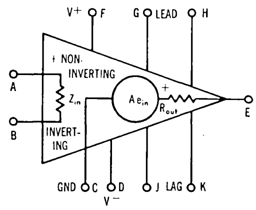
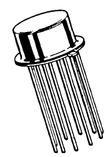


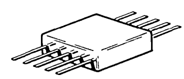
FIGURE 1 – EQUIVALENT CIRCUIT BOTH TYPES

OPERATIONAL AMPLIFIER INTEGRATED CIRCUITS

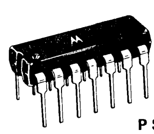


Pin 4 Electrically Connected to Can

G SUFFIX
METAL PACKAGE
CASE 602B



F SUFFIX
CERAMIC PACKAGE
CASE 606
TO-91



P SUFFIX
PLASTIC PACKAGE
CASE 605
TO-116

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+	+8.0	Vdc
Power Supply Voltage	V^-	-8.0	Vdc
Differential Input Signal	V_{in}	±5.0	Volts
Load Current	I_L	10	mA
Power Dissipation (Package Limitation)	P_D		
Metal Package		680	mW
Derate above T_A = +25°C		4.6	mW/°C
Ceramic Flat Package		500	mW
Derate above T_A = +25°C		3.3	mW/°C
Plastic Dual In-Line Package		400	mW
Derate above T_A = +25°C		3.3	mW/°C
Operating Temperature Range*	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

*For full temperature range (-55°C to +125°C) see MC1530-MC1531 data sheet.

FIGURE 2 – MC1430 (STANDARD INPUT)

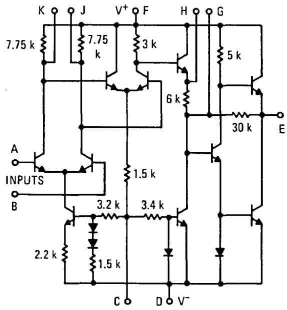
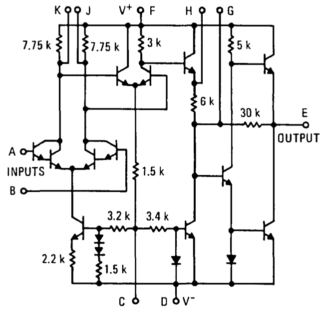


FIGURE 3 – MC1431 (DARLINGTON INPUT)

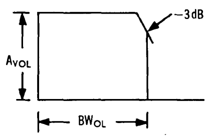
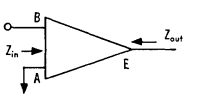
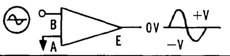
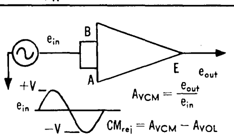
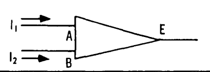
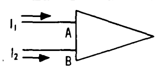
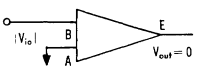


PIN CONNECTIONS

Schematic	A	B	C	D	E	F	G	H	J	K
"F" & "G" Pkgs.	1	2	3	4	5	6	7	8	9	10
"P" Package	4	6	8	7	11	12	13	14	1	2

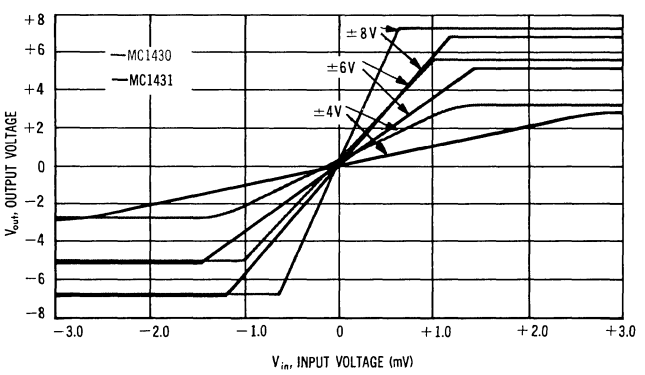
See Packaging Information Section for outline dimensions.

ELECTRICAL CHARACTERISTICS (V+ = +6 Vdc, V− = −6 Vdc, T_A = ± 25°C unless otherwise noted)

Characteristic Definitions*	Characteristic		Symbol	Min	Typ	Max	Unit
	Open Loop Voltage Gain	MC1430	A_{VOL}	69	74	—	dB
		MC1431		62	71	—	dB
		MC1430		3000	5000	—	V/V
		MC1431		1500	3500	—	V/V
	Open Loop Bandwidth (no roll-off capacitance)	MC1430	BW_{OL}	1.0	1.2	—	MHz
		MC1431		0.15	0.4	—	
	Output Impedance (f = 20 Hz)	MC1430, MC1431	Z_{out}	—	25	50	ohms
	Input Impedance (f = 20 Hz)	MC1430	Z_{in}	5.0	15	—	k ohms
		MC1431		300	600	—	
	Output Voltage Swing (1000 ohm Load)	MC1430, MC1431	V_{out}	±4.0	± 5.0	—	V_{peak}
	Input Common Mode Voltage Swing	MC1430	CMV_{in}	±2.0	± 2.5	—	V_{peak}
		MC1431		±2.0	± 2.2	—	
	Common Mode Rejection Ratio	MC1430	CM_{rej}	65	75	—	dB
		MC1431		60	75	—	
	Input Bias Current $\left(I_b = \frac{I_1 + I_2}{2}\right)$	MC1430	I_b	—	5.0	15	μA
		MC1431		—	0.1	0.3	
	Input Offset Current $I_{io} = I_1 - I_2$	MC1430	I_{io}	—	0.4	4.0	μA
		MC1431		—	0.01	0.1	
	Input Offset Voltage	MC1430	$\lvert V_{io} \rvert$	—	2.0	10	mV
		MC1431		—	5.0	15	
	DC Power Dissipation (Power Supply = ±6 V, V_{out} = 0)		P_D	—	110	150	mW
	Input Offset Voltage +75°C	MC1430	$\lvert V_{io} \rvert$	—	3.0	12.0	mV
	0°C			—	3.0	11.0	
	+75°C	MC1431		—	6.0	18.0	
	0°C			—	6.0	16.5	

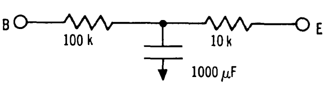
*All definitions imply linear operation (V_{io} = 0)

FIGURE 4 — NORMALIZED DC OPEN LOOP TRANSFER CHARACTERISTICS



RECOMMENDED OPERATING CONDITIONS

1. For High Slew Rate use Circuit A, Figure 9
2. For Minimum Noise use Circuit B, Figure 9
3. For operational stability Power Supply decoupling should be employed at all times.
4. Self Biasing network used to hold output voltage less than ±1 volt dc (quiescent)



MC1488L

LINEAR/DIGITAL INTERFACE CIRCUITS

QUAD LINE DRIVER

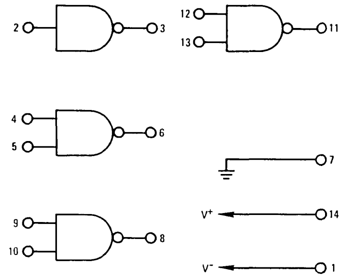
The MC1488L is a monolithic quad line driver designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. RS-232C.

Features:

- Current Limited Output
  10 mA typ
- Power-Off Source Impedance
  300 Ohms min
- Simple Slew Rate Control with External Capacitor
- Flexible Operating Supply Range
- Compatible with All Motorola DTL and TTL Logic Families

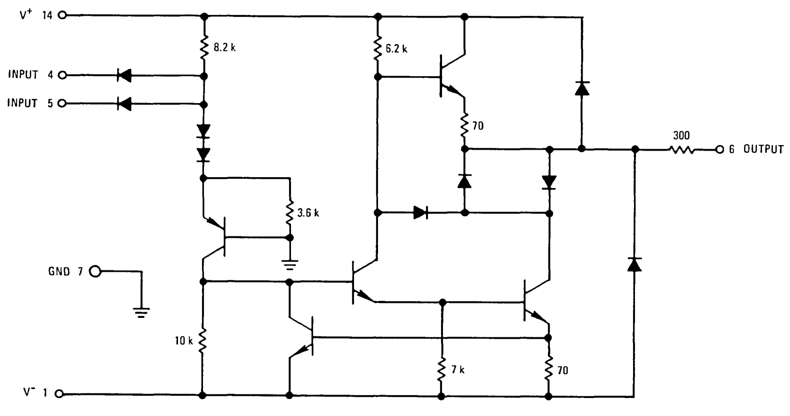
QUAD MDTL LINE DRIVER
RS-232C
INTEGRATED CIRCUIT

LOGIC DIAGRAM

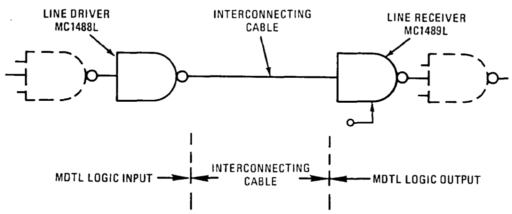


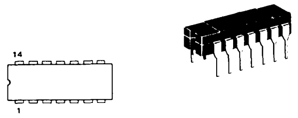
CIRCUIT SCHEMATIC

1/4 OF CIRCUIT SHOWN



TYPICAL APPLICATION





(top view)

CERAMIC PACKAGE
CASE 632
TO-116

See Packaging Information Section for outline dimensions.

Maximum Rating (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+ V^-	+15 -15	Vdc
Input Signal Voltage	V_{in}	$-15 \leq V_{in} \leq 7.0$	Vdc
Output Signal Voltage	V_o	±15	Vdc
Power Derating (Package Limitation, Ceramic Dual-In-Line Package) Derate above T_A = +25°C	P_D $1/\theta_{JA}$	1000 6.7	mW mW/°C
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +175	°C

ELECTRICAL CHARACTERISTICS (V^+ = +9.0 ± 1% Vdc, V^- = -9.0 ± 1% Vdc, T_A = 0 to +75°C unless otherwise noted)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Forward Input Current (V_{in} = 0 Vdc)	1	I_F	–	1.0	1.6	mA
Reverse Input Current (V_{in} = +5.0 Vdc)	1	I_R	–	–	10	µA
Output Voltage High	2	V_{OH}				Vdc
(V_{in} = 0.8 Vdc, R_L = 3.0 kΩ, V^+ = +9.0 Vdc, V^- = -9.0 Vdc)			+6.0	+7.0	–	
(V_{in} = 0.8 Vdc, R_L = 3.0 kΩ, V^+ = +13.2 Vdc, V^- = -13.2 Vdc)			+9.0	+10.5	–	
Output Voltage Low	2	V_{OL}				Vdc
(V_{in} = 1.9 Vdc, R_L = 3.0 kΩ, V^+ = +9.0 Vdc, V^- = -9.0 Vdc)			-6.0	-7.0	–	
(V_{in} = 1.9 Vdc, R_L = 3.0 kΩ, V^+ = +13.2 Vdc, V^- = -13.2 Vdc)			-9.0	-10.5	–	
Positive Output Short-Circuit Current	3	I_{SC^+}	+6.0	+10	+12	mA
Negative Output Short-Circuit Current	3	I_{SC^-}	-6.0	-10	-12	mA
Output Resistance ($V^+ = V^- = 0$, $\|V_o\|$ = ±2.0 V)	4	R_o	300	–	–	Ohms
Positive Supply Current ($R_l = \infty$)	5	I^+				mA
(V_{in} = 1.9 Vdc, V^+ = +9.0 Vdc)			–	+15	+20	
(V_{in} = 0.8 Vdc, V^+ = +9.0 Vdc)			–	+4.5	+6.0	
(V_{in} = 1.9 Vdc, V^+ = +12 Vdc)			–	+19	+25	
(V_{in} = 0.8 Vdc, V^+ = +12 Vdc)			–	+5.5	+7.0	
(V_{in} = 1.9 Vdc, V^+ = +15 Vdc)			–	–	+34	
(V_{in} = 0.8 Vdc, V^+ = +15 Vdc)			–	–	+12	
Negative Supply Current ($R_L = \infty$)	5	I^-				mA
(V_{in} = 1.9 Vdc, V^- = -9.0 Vdc)			–	-13	-17	
(V_{in} = 0.8 Vdc, V^- = -9.0 Vdc)			–	0	0	
(V_{in} = 1.9 Vdc, V^- = -12 Vdc)			–	-18	-23	
(V_{in} = 0.8 Vdc, V^- = -12 Vdc)			–	0	0	
(V_{in} = 1.9 Vdc, V^- = -15 Vdc)			–	–	-34	
(V_{in} = 0.8 Vdc, V^- = -15 Vdc)			–	–	-2.5	
Power Dissipation		P_D				mW
(V^+ = 9.0 Vdc, V^- = -9.0 Vdc)			–	–	333	
(V^+ = 12 Vdc, V^- = -12 Vdc)			–	–	576	

SWITCHING CHARACTERISTICS (V^+ = +9.0 ± 1% Vdc, V^- = -9.0 ± 1% Vdc, T_A = +25°C)

Propagation Delay Time (Z_L = 3.0 k and 15 pF)	6	t_{pd}^+	–	150	200	ns
Fall Time (Z_L = 3.0 k and 15 pF)	6	t_f	–	45	75	ns
Propagation Delay Time (Z_L = 3.0 k and 15 pF)	6	t_{pd}^-	–	65	120	ns
Rise Time (Z_L = 3.0 k and 15 pF)	6	t_r	–	55	100	ns

CHARACTERISTIC DEFINITIONS

FIGURE 1 – INPUT CURRENT

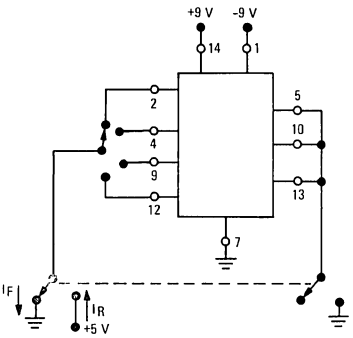


FIGURE 2 – OUTPUT VOLTAGE

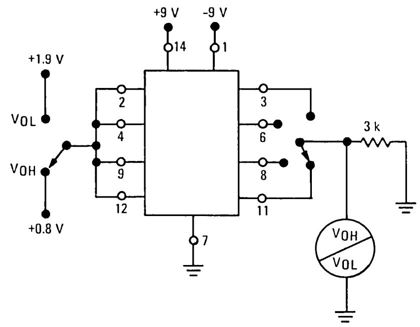


FIGURE 3 – OUTPUT SHORT-CIRCUIT CURRENT

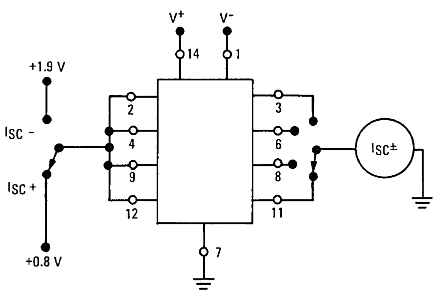


FIGURE 4 – OUTPUT RESISTANCE (POWER-OFF)

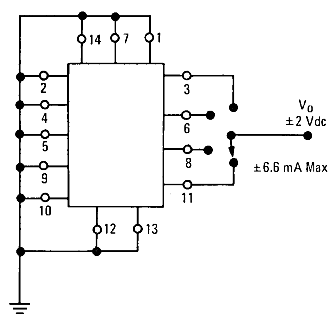


FIGURE 5 – POWER-SUPPLY CURRENTS

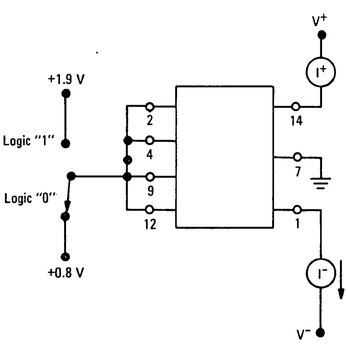
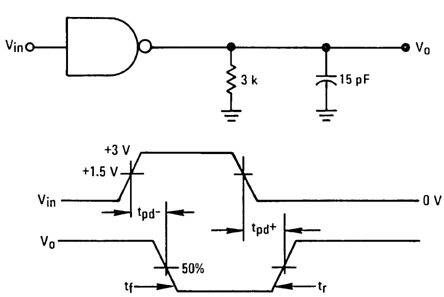


FIGURE 6 – SWITCHING RESPONSE



t_r and t_f Measured 10% to 90%

TYPICAL CHARACTERISTICS

(T_A = +25°C unless otherwise noted)

FIGURE 7 — TRANSFER CHARACTERISTICS versus POWER-SUPPLY VOLTAGE

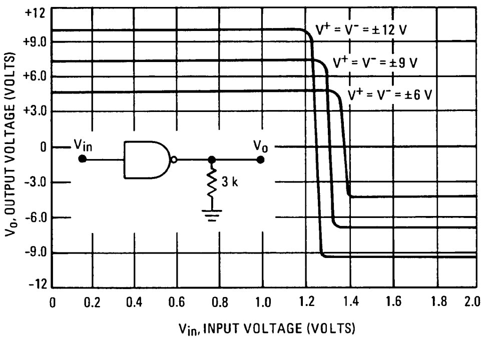


FIGURE 8 — SHORT-CIRCUIT OUTPUT CURRENT versus TEMPERATURE

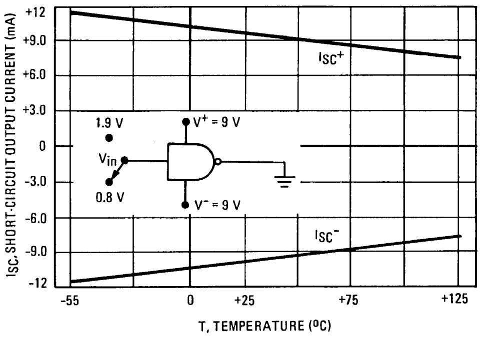


FIGURE 9 — OUTPUT SLEW RATE versus LOAD CAPACITANCE

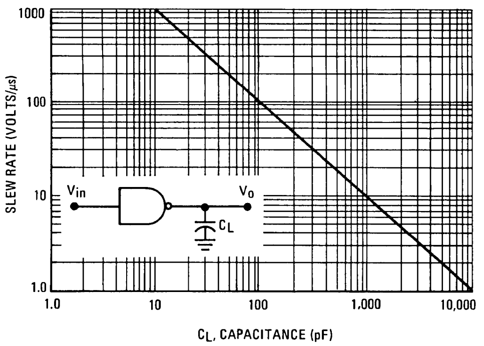


FIGURE 10 — OUTPUT VOLTAGE AND CURRENT-LIMITING CHARACTERISTICS

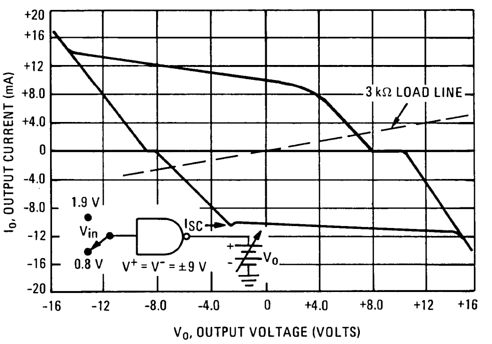
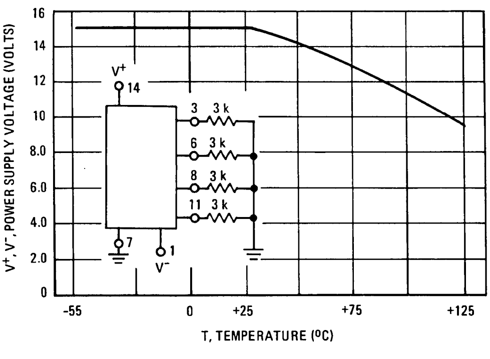


FIGURE 11 — MAXIMUM OPERATING TEMPERATURE versus POWER-SUPPLY VOLTAGE



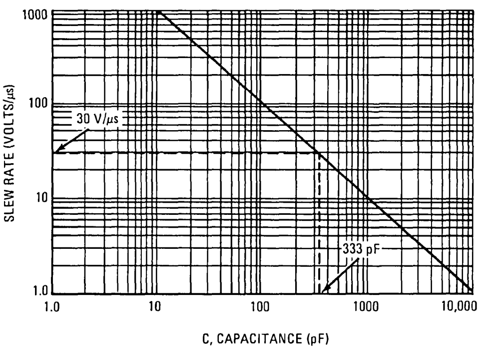
APPLICATIONS INFORMATION

The Electronic Industries Association (EIA) has released the RS232C specification detailing the requirements for the interface between data processing equipment and data communications equipment. This standard specifies not only the number and type of interface leads, but also the voltage levels to be used. The MC1488L quad driver and its companion circuit, the MC1489L quad receiver, provide a complete interface system between DTL or TTL logic levels and the RS232C defined levels. The RS232C requirements as applied to drivers are discussed herein.

The required driver voltages are defined as between 5 and 15-volts in magnitude and are positive for a logic "0" and negative for a logic "1". These voltages are so defined when the drivers are terminated with a 3000 to 7000-ohm resistor. The MC1488L meets this voltage requirement by converting a DTL/TTL logic level into RS232C levels with one stage of inversion.

The RS232C specification further requires that during transitions, the driver output slew rate must not exceed 30 volts per microsecond. The inherent slew rate of the MC1488L is much too

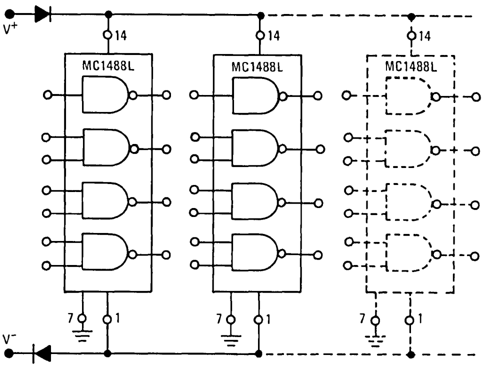
FIGURE 12 – SLEW RATE versus CAPACITANCE FOR I_{SC} = 10 mA



fast for this requirement. The current limited output of the device can be used to control this slew rate by connecting a capacitor to each driver output. The required capacitor can be easily determined by using the relationship $C = I_{SC} \times \Delta T/\Delta V$ from which Figure 12 is derived. Accordingly, a 330 pF capacitor on each output will guarantee a worst case slew rate of 30 volts per microsecond.

The interface driver is also required to withstand an accidental short to any other conductor in an interconnecting cable. The worst possible signal on any conductor would be another driver using a plus or minus 15 volt, 500 mA source. The MC1488L is designed to indefinitely withstand such a short to all four outputs in a package as long as the power-supply voltages are greater than 9.0 volts (i.e., $V^+ \geq 9.0$ V; $V^- \leq -9.0$ V). In some power-supply designs, a loss of system power causes a low impedance on the power-supply outputs. When this occurs, a low impedance to ground would exist at the power inputs to the MC1488L effectively shorting the 300-ohm output resistors to ground. If all four outputs were then shorted to plus or minus 15 volts, the power dissipation in these resistors

FIGURE 13 – POWER-SUPPLY PROTECTION TO MEET POWER-OFF FAULT CONDITIONS



would be excessive. Therefore, if the system is designed to permit low impedances to ground at the power-supplies of the drivers, a diode should be placed in each power-supply lead to prevent overheating in this fault condition. These two diodes, as shown in Figure 13, could be used to decouple all the driver packages in a system. (These same diodes will allow the MC1488L to withstand momentary shorts to the ±25-volt limits specified in the earlier Standard RS232B.) The addition of the diodes also permits the MC1488L to withstand faults with power-supplies of less than the 9.0 volts stated above.

The maximum short-circuit current allowable under fault conditions is more than guaranteed by the previously mentioned 10 mA output current limiting.

Other Applications

The MC1488L is an extremely versatile line driver with a myriad of possible applications. Several features of the drivers enhance this versatility:

1. Output Current Limiting – this enables the circuit designer to define the output voltage levels independent of power-supplies and can be accomplished by diode clamping of the output pins. Figure 14 shows the MC1488L used as a DTL to MOS translator where the high-level voltage output is clamped one diode above ground. The resistor divider shown is used to reduce the output voltage below the 300 mV above ground MOS input level limit.

2. Power-Supply Range – as can be seen from the schematic drawing of the drivers, the positive and negative driving elements of the device are essentially independent and do not require matching power-supplies. In fact, the positive supply can vary from a minimum seven volts (required for driving the negative pulldown section) to the maximum specified 15 volts. The negative supply can vary from approximately -2.5 volts to the minimum specified -15 volts. The MC1488L will drive the output to within 2 volts of the positive or negative supplies as long as the current output limits are not exceeded. The combination of the current-limiting and supply-voltage features allow a wide combination of possible outputs within the same quad package. Thus if only a portion of the four drivers are used for driving RS232C lines, the remainder could be used for DTL to MOS or even DTL to DTL translation. Figure 15 shows one such combination.

FIGURE 14 – MDTL/MTTL-TO-MOS TRANSLATOR

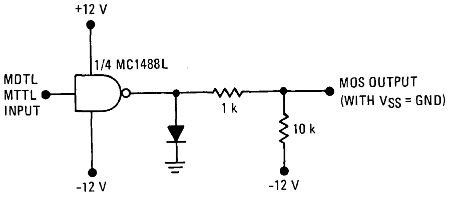
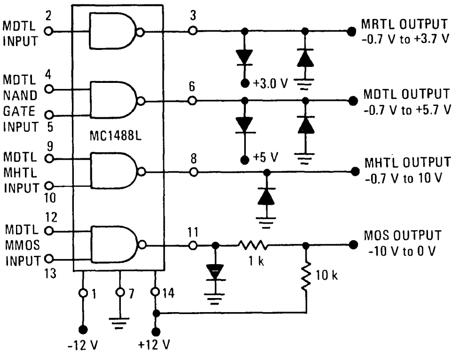


FIGURE 15 – LOGIC TRANSLATOR APPLICATIONS



LINEAR/DIGITAL INTERFACE CIRCUITS

MC1489L
MC1489AL

QUAD LINE RECEIVERS

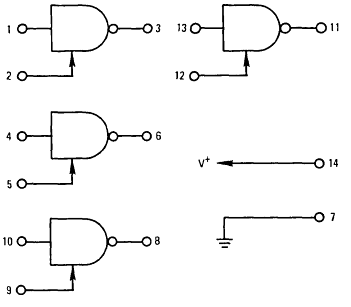
The MC1489 monolithic quad line receivers are designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. RS-232C.

- Input Resistance — 3.0 k to 7.0 kilohms
- Input Signal Range — ±30 Volts
- Input Threshold Hysteresis Built In
- Response Control
  - a) Logic Threshold Shifting
  - b) Input Noise Filtering

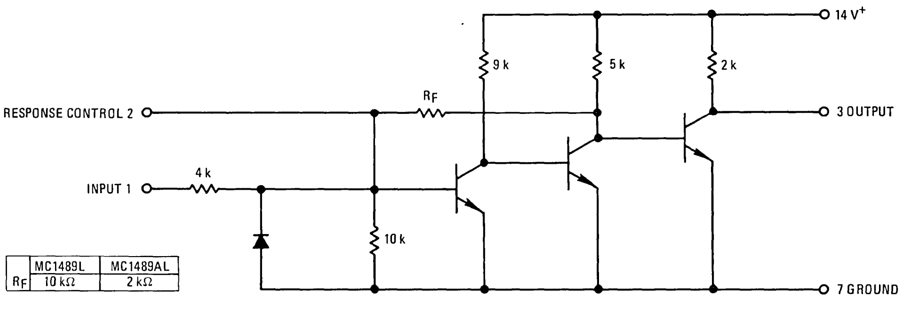
QUAD MDTL LINE RECEIVERS RS-232C

INTEGRATED CIRCUIT

LOGIC DIAGRAM

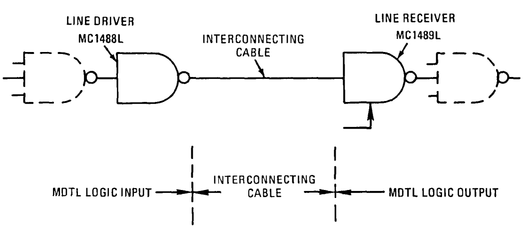


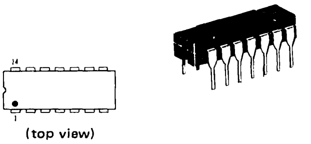
CIRCUIT SCHEMATIC (1/4 OF CIRCUIT SHOWN)



	MC1489L	MC1489AL
R_F	10 kΩ	2 kΩ

TYPICAL APPLICATION





(top view)

CERAMIC PACKAGE
CASE 632
TO-116

See Packaging Information Section for outline dimensions.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+	10	Vdc
Input Signal Range	V_{in}	±30	Vdc
Output Load Current	I_L	20	mA
Power Dissipation (Package Limitation, Ceramic Dual In-Line Package) Derate above T_A = +25°C	P_D $1/\theta_{JA}$	1000 6.7	mW mW/°C
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +175	°C

ELECTRICAL CHARACTERISTICS (Response control pin is open.) (V^+ = +5.0 Vdc ± 1%, T_A = 0 to +75°C unless otherwise noted.)

Characteristics		Figure	Symbol	Min	Typ	Max	Unit
Positive Input Current	(V_{in} = +25 Vdc) (V_{in} = +3.0 Vdc)	1	I_{IH}	3.6 0.43	– –	8.3 –	mA
Negative Input Current	(V_{in} = -25 Vdc) (V_{in} = -3.0 Vdc)	1	I_{IL}	-3.6 -0.43	– –	-8.3 –	mA
Input Turn-On Threshold Voltage (T_A = +25°C, $V_{OL} \leq$ 0.45 V)	MC1489L MC1489AL	2	V_{IH}	1.0 1.75	– 1.95	1.5 2.25	Vdc
Input Turn-Off Threshold Voltage (T_A = +25°C, $V_{OH} \geq$ 2.5 V, I_L = -0.5 mA)	MC1489L MC1489AL	2	V_{IL}	0.75 0.75	– 0.8	1.25 1.25	Vdc
Output Voltage High	(V_{in} = 0.75 V, I_L = -0.5 mA) (Input Open Circuit, I_L = -0.5 mA)	2	V_{OH}	2.6 2.6	4.0 4.0	5.0 5.0	Vdc
Output Voltage Low	(V_{in} = 3.0 V, I_L = 10 mA)	2	V_{OL}	–	0.2	0.45	Vdc
Output Short-Circuit Current		3	I_{SC}	–	3.0	–	mA
Power Supply Current	(V_{in} = +5.0 Vdc)	4	I^+	–	20	26	mA
Power Dissipation	(V_{in} = +5.0 Vdc)	4	P_D	–	100	130	mW

SWITCHING CHARACTERISTICS (V^+ = 5.0 Vdc ± 1%, T_A = +25°C)

Propagation Delay Time	(R_L = 3.9 kΩ)	5	t_{pd+}	–	25	85	ns
Rise Time	(R_L = 3.9 kΩ)	5	t_r	–	120	175	ns
Propagation Delay Time	(R_L = 390 Ω)	5	t_{pd-}	–	25	50	ns
Fall Time	(R_L = 390 Ω)	5	t_f	–	10	20	ns

TEST CIRCUITS

FIGURE 1 – INPUT CURRENT

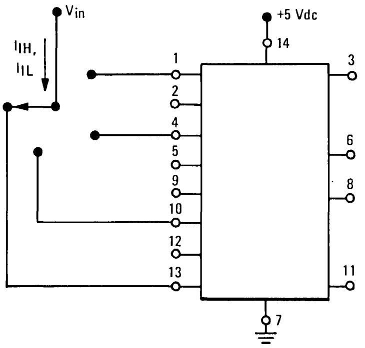


FIGURE 2 – OUTPUT VOLTAGE and INPUT THRESHOLD VOLTAGE

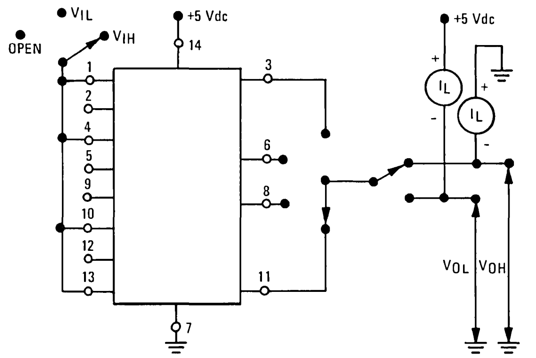


FIGURE 3 – OUTPUT SHORT-CIRCUIT CURRENT

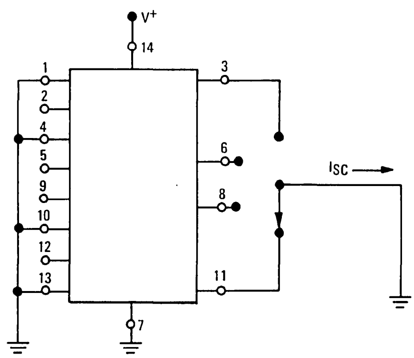


FIGURE 4 – POWER-SUPPLY CURRENT

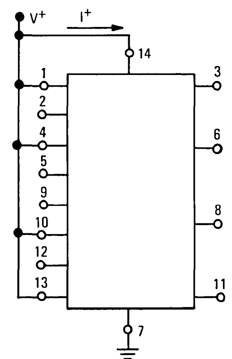


FIGURE 5 – SWITCHING RESPONSE

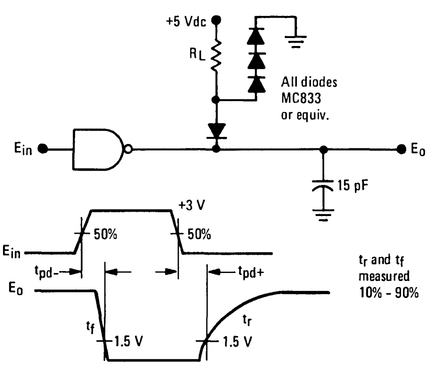
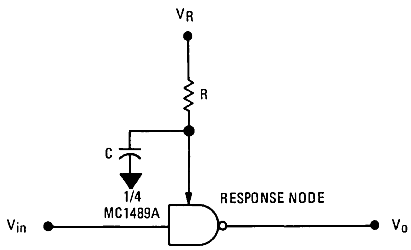


FIGURE 6 – RESPONSE CONTROL NODE



C, capacitor is for noise filtering.
R, resistor is for threshold shifting.

TYPICAL CHARACTERISTICS

($V^+ = 5.0$ Vdc, $T_A = +25^oC$ unless otherwise noted)

FIGURE 7 – INPUT CURRENT

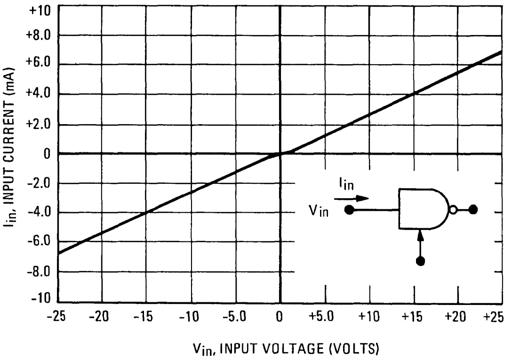


FIGURE 8 – MC1489 INPUT THRESHOLD VOLTAGE ADJUSTMENT

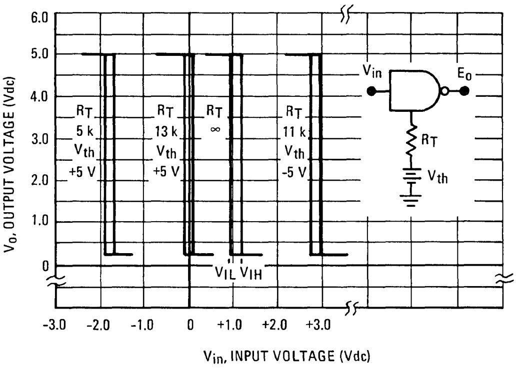


FIGURE 9 – MC1489A INPUT THRESHOLD VOLTAGE ADJUSTMENT

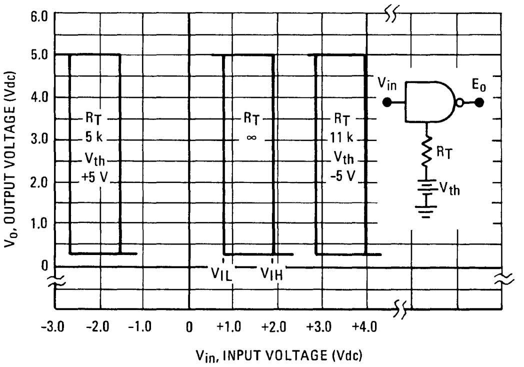


FIGURE 10 – INPUT THRESHOLD VOLTAGE versus TEMPERATURE

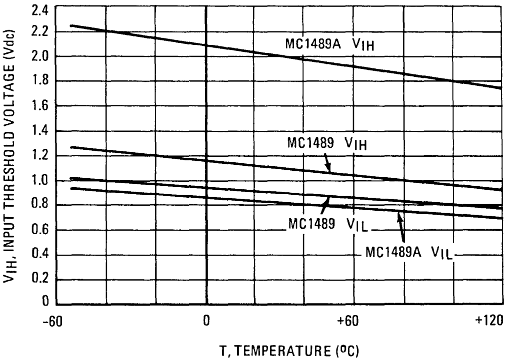
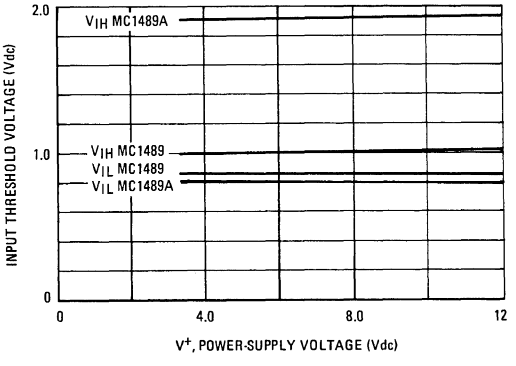


FIGURE 11 – INPUT THRESHOLD versus POWER-SUPPLY VOLTAGE



APPLICATIONS INFORMATION

General Information

The Electronic Industries Association (EIA) has released the RS-232C specification detailing the requirements for the interface between data processing equipment and data communications equipment. This standard specifies not only the number and type of interface leads, but also the voltage levels to be used. The MC1488L quad driver and its companion circuit, the MC1489L quad receiver, provide a complete interface system between DTL or TTL logic levels and the RS-232C defined levels. The RS-232C requirements as applied to receivers are discussed herein.

The required input impedance is defined as between 3000 ohms and 7000 ohms for input voltages between 3.0 and 25 volts in magnitude; and any voltage on the receiver input in an open circuit condition must be less than 2.0 volts in magnitude. The MC1489 circuits meet these requirements with a maximum open circuit voltage of one V_{BE} (Ref. Sect. 2.4).

The receiver shall detect a voltage between -3.0 and -25 volts as a logic "1" and inputs between +3.0 and +25 volts as a logic "0" (Ref. Sect. 2.3). On some interchange leads, an open circuit or "Power OFF" condition (300 ohms or more to ground) shall be decoded as an "OFF" condition or logic "1" (Ref. Sect. 2.5). For this reason, the input hysteresis thresholds of the MC1489 circuits are all above ground. Thus an open or grounded input will cause the same output as a negative or logic "1" input.

Device Characteristics

The MC1489 interface receivers have internal feedback from the second stage to the input stage providing input hysteresis for noise rejection. The MC1489L input has typical turn-on voltage of 1.25 volts and turn-off of 1.0 volt for a typical hysteresis of 250 mV. The MC1489AL has typical turn-on of 1.95 volts and turn-off of 0.8 volt for typically 1.15 volts of hysteresis.

Each receiver section has an external response control node in addition to the input and output pins, thereby allowing the designer to vary the input threshold voltage levels. A resistor can be connected between this node and an external power-supply. Figures 6, 8 and 9 illustrate the input threshold voltage shift possible through this technique.

This response node can also be used for the filtering of high-frequency, high-energy noise pulses. Figures 12 and 13 show typical noise-pulse rejection for external capacitors of various sizes.

These two operations on the response node can be combined or used individually for many combinations of interfacing applications. The MC1489 circuits are particularly useful for interfacing between MOS circuits and MDTL/MTTL logic systems. In this application, the input threshold voltages are adjusted (with the appropriate supply and resistor values) to fall in the center of the MOS voltage logic levels. (See Figure 14)

The response node may also be used as the receiver input as long as the designer realizes that he may not drive this node with a low impedance source to a voltage greater than one diode above ground or less than one diode below ground. This feature is demonstrated in Figure 15 where two receivers are slaved to the same line that must still meet the RS-232C impedance requirement.

FIGURE 12 — MC1489 NOISE REJECTION

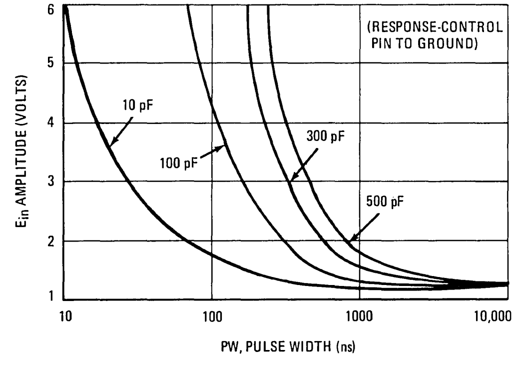
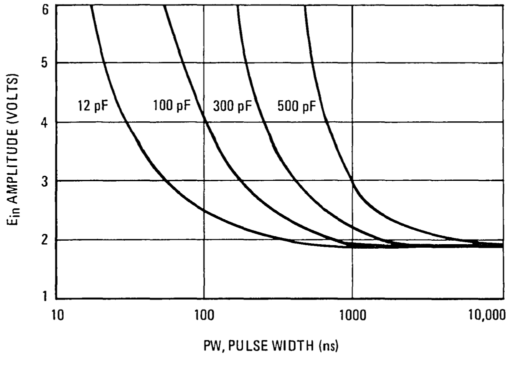


FIGURE 13 — MC1489A NOISE REJECTION



6

APPLICATIONS INFORMATION (continued)

FIGURE 14 – TYPICAL TRANSLATOR APPLICATION – MOS TO DTL OR TTL

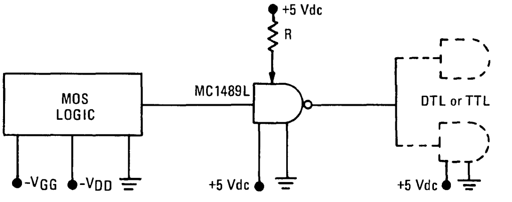
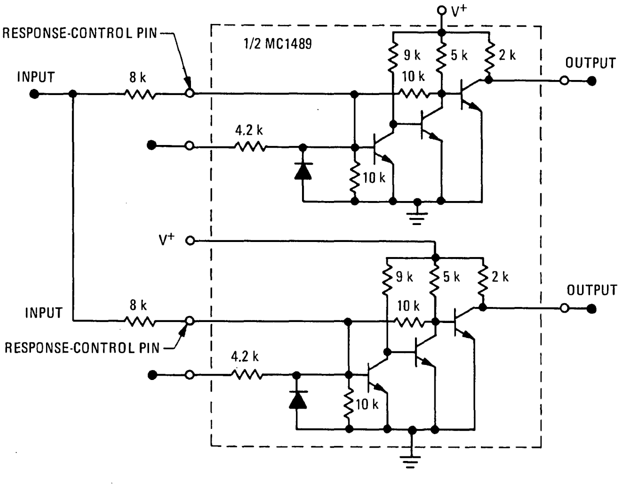


FIGURE 15 – TYPICAL PARALLELING OF TWO MC1489,A RECEIVERS TO MEET RS-232C



MC1510G
MC1410G

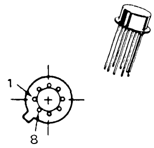
MONOLITHIC WIDEBAND VIDEO AMPLIFIER

. . . designed for use as a high-frequency differential amplifier with operating characteristics that provide a flat frequency response from dc to 40 MHz.

- High Gain Characteristics
  A_V = 93 typ
- Wide Bandwidth – dc to 40 MHz typ
- Large Output Voltage Swing
  4.5 V p-p typical @ ±6.0 V Supply
- Low Output Distortion
  THD ⩽ 1.5% typ

VIDEO AMPLIFIER INTEGRATED CIRCUIT

METAL PACKAGE
CASE 601
TO-99



(bottom view)

FIGURE 1 – VOLTAGE GAIN versus FREQUENCY

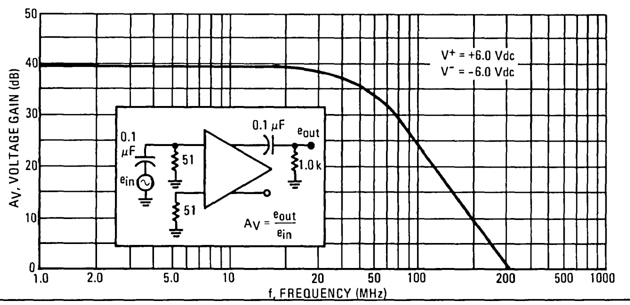
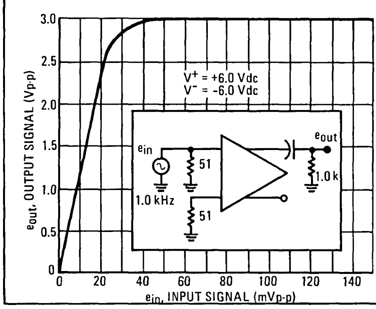
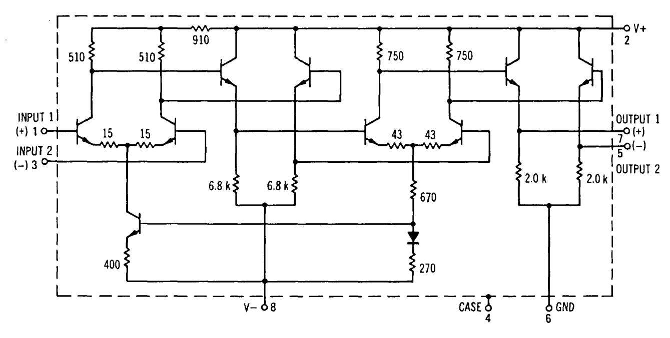


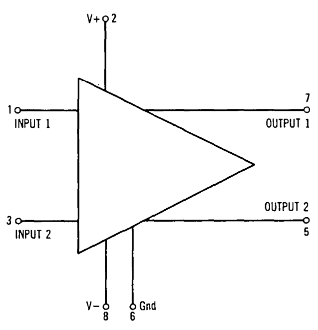
FIGURE 2 – LIMITING CHARACTERISTICS



CIRCUIT SCHEMATIC



EQUIVALENT CIRCUIT



See Packaging Information Section for outline dimensions.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+ V^-	+8.0 -8.0	Vdc Vdc
Differential Input Signal	V_{in}	±5.0	Volts
Common Mode Input Swing	CMV_{in}	±6.0	Volts
Load Current	I_L	10	mA
Output Short Circuit Duration	t_s	5.0	s
Power Dissipation (Package Limitation) Metal Can Derate above T_A = +25°C	P_D	 680 4.6	 mW mW/°C
Operating Temperature Range MC1410 MC1510	T_A	 0 to +75 -55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V^+ = +6 Vdc, V^- = -6 Vdc, R_L = 5.0 kohms, T_A = +25°C unless otherwise noted)

		MC1510			MC1410			
Characteristic	Symbol	Min	Typ	Max	Min	Typ	Max	Unit
Single Ended Voltage Gain	$A_{V(se)}$	75	93	110	60	90	120	V/V
Output Impedance (f = 20 kHz)	Z_{out}	–	35	–	–	35	–	Ω
Input Impedance (f = 20 kHz)	Z_{in}	–	6.0	–	–	6.0	–	kΩ
Bandwidth (-3.0 dB)	BW	–	40	–	–	40	–	MHz
Output Voltage Swing (f = 100 kHz)	V_{out}	–	4.5	–	–	4.5	–	Vp-p
Single Ended Output Distortion (e_{in} < 0.2% Distortion)	THD	–	1.5	5.0	–	2.0	–	%
Input Common Mode Voltage Swing	CMV_{in}	–	±1.0	–	–	±1.0	–	V_{peak}
Common Mode Voltage Gain (e_{in} = 0.3 V rms, f = 100 kHz) Common Mode Rejection Ratio	AVCM CM_{rej}	 -30 –	 -45 85	 – –	 -20 –	 -40 85	 – –	dB
Input Bias Current $\left(I_b = \frac{I_1 + I_2}{2}\right)$ Differential Output = 0	$\lvert I_b \rvert$	–	20	80	–	50	100	μA
Input Offset Current ($I_{io} = I_1 - I_2$)	$\lvert I_{io} \rvert$	–	3.0	20	–	5.0	30	μA
Output Offset Voltage Differential Mode (V_{in} = 0) Common Mode (Differential Output = 0)	$V_{out(DM)}$ $V_{out(CM)}$	 – 2.6	 0.5 3.1	 1.3 3.5	 – 2.0	 0.5 3.0	 2.0 4.0	Vdc
Step Response	t_f t_{pd} t_r	– – –	9.0 9.0 9.0	12 – 12	– – –	10 9.0 10	15 – 15	ns
Average Temperature Coefficient of Input Offset Voltage (R_S = 50 Ω, T_A = T_{low}* to T_{high}**) ($R_S \leq$ 10 k Ω, T_A = T_{low} to T_{high})	TC_{Vio}	 – –	 ±3.0 ±6.0	 – –	 – –	 ±3.0 ±6.0	 – –	μV/°C
DC Power Dissipation (Power Supply = ±6.0 V)	P_D	–	150	220	–	165	220	mW
Equivalent Average Input Noise Voltage (f = 10Hz to 500 kHz) (R_S = 0)	V_n	–	5.0	–	–	5.0	–	μV

*T_{low} = 0°C for MC1410 or –55°C for MC1510

**T_{high} = +75°C for MC1410 or +125°C for MC1510

TYPICAL CHARACTERISTICS

(V^+ = +6.0 Vdc, V^- = -6.0 Vdc, T_A = +25°C unless otherwise noted)

FIGURE 3
POWER DISSIPATION versus SUPPLY VOLTAGE

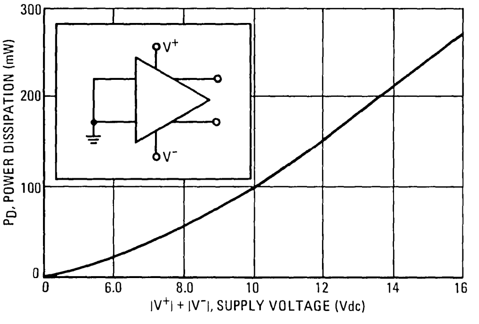


FIGURE 4
VOLTAGE GAIN versus SUPPLY VOLTAGE

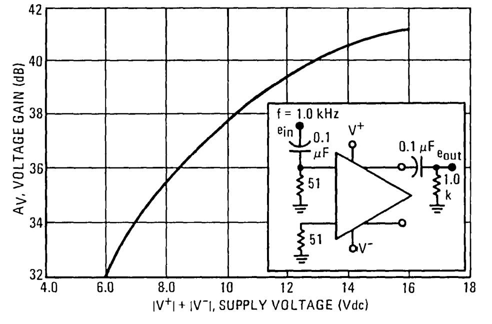


FIGURE 5
VOLTAGE GAIN versus TEMPERATURE

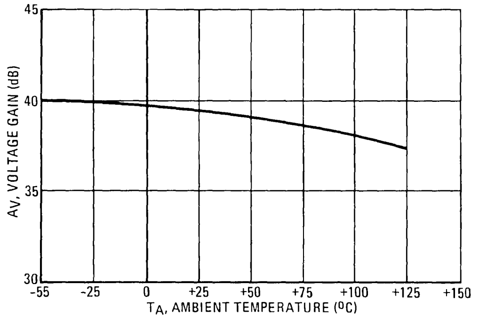


FIGURE 6
DC OUTPUT VOLTAGE versus TEMPERATURE

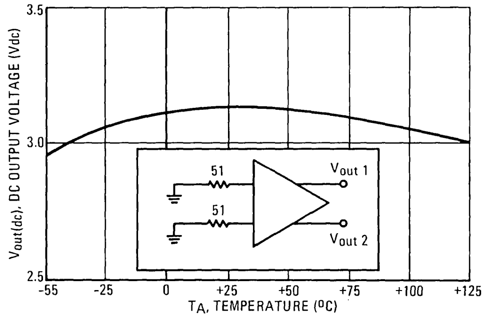


FIGURE 7
INPUT BIAS CURRENT versus TEMPERATURE

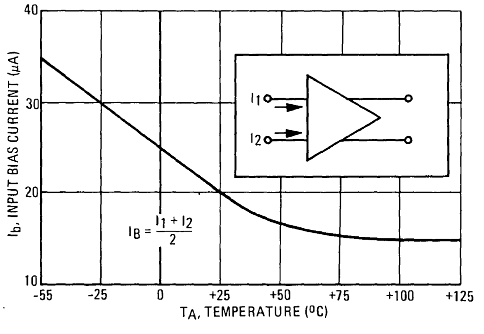
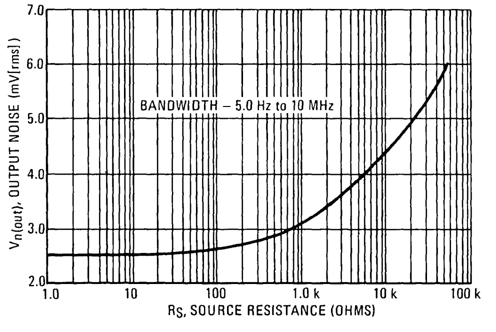


FIGURE 8
OUTPUT NOISE VOLTAGE versus SOURCE IMPEDANCE



TYPICAL APPLICATIONS

FIGURE 9
ENVELOPE DETECTOR

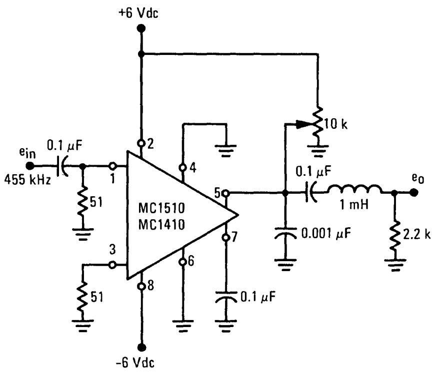


FIGURE 10
TWO STAGE VIDEO AMPLIFIER WITH ADJUSTABLE GAIN

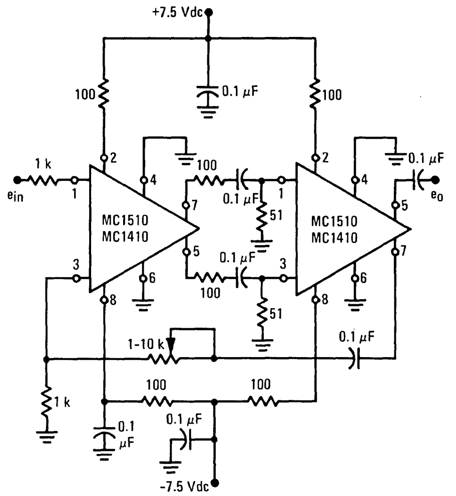


FIGURE 11
SINGLE STAGE WIDEBAND AMPLIFIER

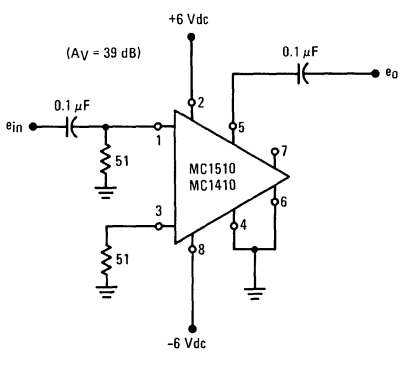
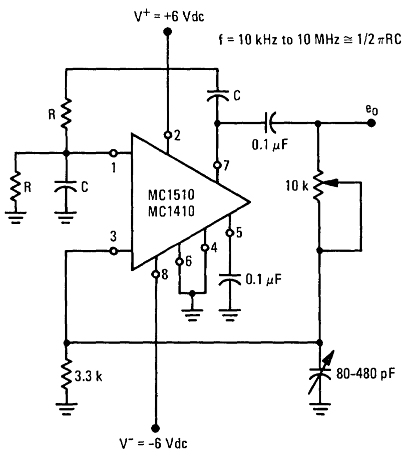


FIGURE 12
WEIN BRIDGE OSCILLATOR



6

MC1514L

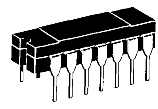
DUAL DIFFERENTIAL COMPARATOR

MONOLITHIC DUAL DIFFERENTIAL VOLTAGE COMPARATOR

. . . designed for use in level detection, low-level sensing, and memory applications.

Typical Amplifier Features:

- Two Separate Outputs
- Strobe Capability
- High Output Sink Current – 2.8 mA min Each Comparator
- Differential Input Characteristics:
  Input Offset Voltage = 1.0 mV
  Offset Voltage Drift = 3.0 μV/$^{\circ}$C
- Short Propagation Delay Time – 40 ns
- Output Compatible with All Saturating Logic Forms
  V_{out} = +3.2 V to -0.5 V typical

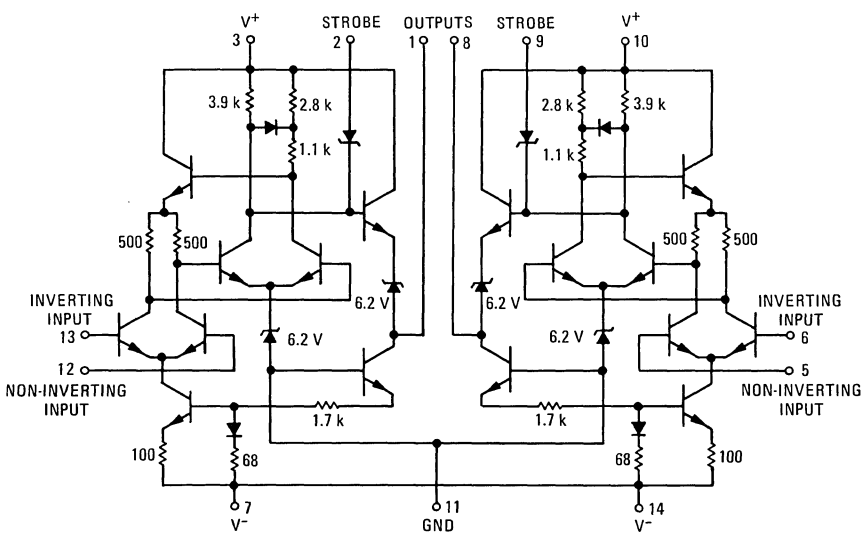


CERAMIC PACKAGE
CASE 632
TO-116

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

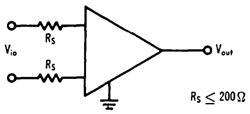
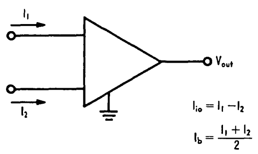
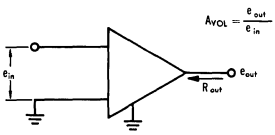
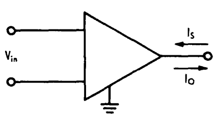
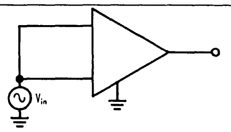
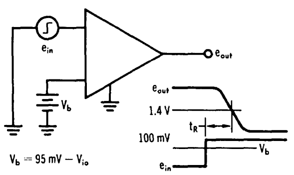
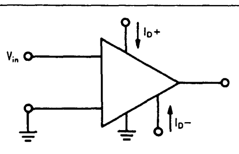
Rating	Symbol	Value	Unit
Power Supply Voltage	V^+ V^-	+14 -7.0	Vdc Vdc
Differential Input Signal	V_{in}	±5.0	Volts
Common Mode Input Swing	CMV_{in}	±7.0	Volts
Peak Load Current	I_L	10	mA
Power Dissipation (package limitation) Ceramic Dual-In-Line Package Derate above T_A = +25°C	P_D	 1000 6.7	 mW mW/°C
Operating Temperature Range	T_A	-55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

CIRCUIT SCHEMATIC



See Packaging Information Section for outline dimensions.

ELECTRICAL CHARACTERISTICS ($V^+ = +12$ Vdc, $V^- = -6$ Vdc, $T_A = 25°C$ unless otherwise noted) (Each Comparator)

Characteristic Definitions (linear operation)	Characteristic	Symbol	Min	Typ	Max	Unit
	Input Offset Voltage $V_{out} = 1.4$ Vdc, $T_A = 25°C$ $V_{out} = 1.8$ Vdc, $T_A = -55°C$ $V_{out} = 1.0$ Vdc, $T_A = +125°C$	V_{io}	 - - -	 1.0 - -	 2.0 3.0 3.0	mVdc
	Temperature Coefficient of Input Offset Voltage	TC_{Vio}	-	3.0	-	µV/°C
	Input Offset Current $V_{out} = 1.4$ Vdc, $T_A = 25°C$ $V_{out} = 1.8$ Vdc, $T_A = -55°C$ $V_{out} = 1.0$ Vdc, $T_A = +125°C$	I_{io}	 - - -	 1.0 - -	 3.0 7.0 3.0	µAdc
	Input Bias Current $V_{out} = 1.4$ Vdc, $T_A = 25°C$ $V_{out} = 1.8$ Vdc, $T_A = -55°C$ $V_{out} = 1.0$ Vdc, $T_A = +125°C$	I_b	 - - -	 12 - -	 20 45 20	µAdc
	Open Loop Voltage Gain $T_A = 25°C$ $T_A = -55$ to $+125°C$	A_{VOL}	 1250 1000	 1700 -	 - -	V/V
	Output Resistance	R_{out}	-	200	-	ohms
	Differential Voltage Range	V_{in}	±5.0	-	-	Vdc
	Positive Output Voltage $V_{in} \geqq 5.0$ mV, $0 \leqq I_o \leqq 5.0$ mA	V_{OH}	2.5	3.2	4.0	Vdc
	Negative Output Voltage $V_{in} \geqq -5.0$ mV	V_{OL}	-1.0	-0.5	0	Vdc
	Output Sink Current $V_{in} \geqq -5.0$ mV, $V_{out} \geqq 0$, $T_A = -55$ to $+125°C$	I_s	2.8	3.4	-	mAdc
	Input Common Mode Range $V^- = -7.0$ Vdc	CMV_{in}	±5.0	-	-	Volts
	Common Mode Rejection Ratio $V^- = -7.0$ Vdc, $R_S \leqq 200\Omega$	CM_{rej}	80	100	-	dB
	Propagation Delay Time For Positive and Negative Going Input Pulse	t_{pd}	-	40	-	ns
	Total Power Supply Current $V_{out} \leqq 0$ Vdc	I_D^+ I_D^-	- -	12.8 11	18 14	mAdc
	Total Power Consumption		-	230	300	mW

TYPICAL CHARACTERISTICS
(Each Comparator)

FIGURE 1 – VOLTAGE TRANSFER CHARACTERISTICS

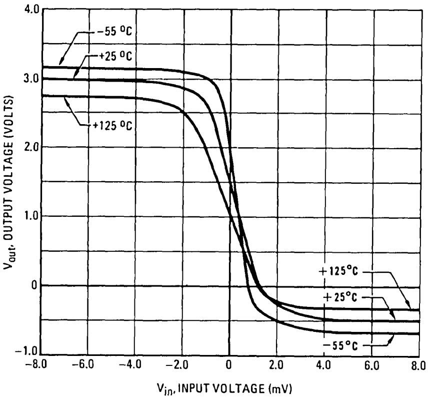


FIGURE 2 – INPUT OFFSET VOLTAGE versus TEMPERATURE

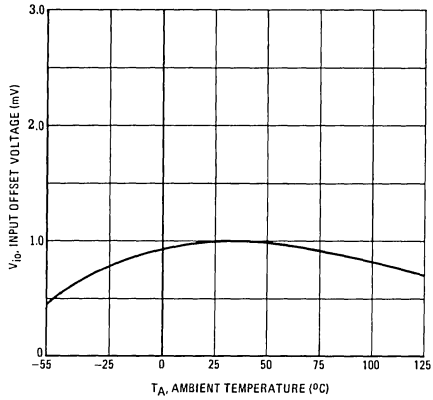


FIGURE 3 – INPUT OFFSET CURRENT versus TEMPERATURE

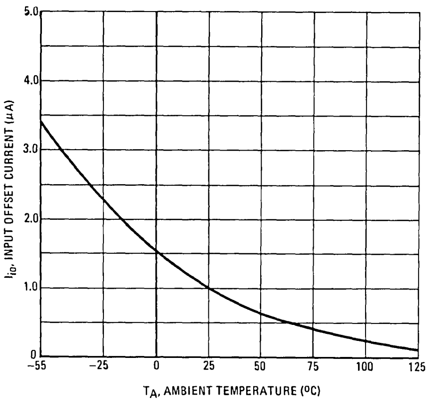


FIGURE 4 – INPUT BIAS CURRENT versus TEMPERATURE

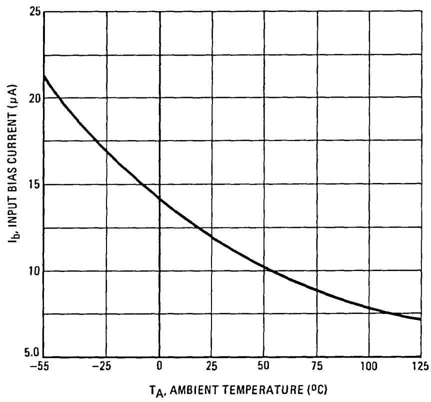


FIGURE 5 – GAIN VARIATION WITH POWER SUPPLY VOLTAGE

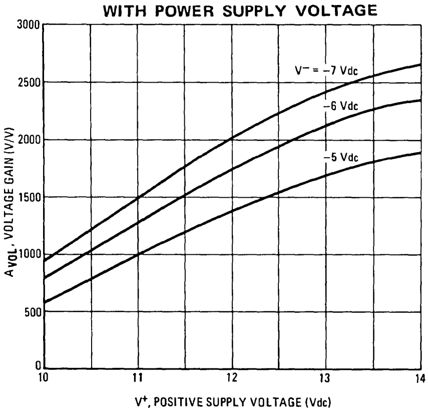


FIGURE 6 – VOLTAGE GAIN versus TEMPERATURE

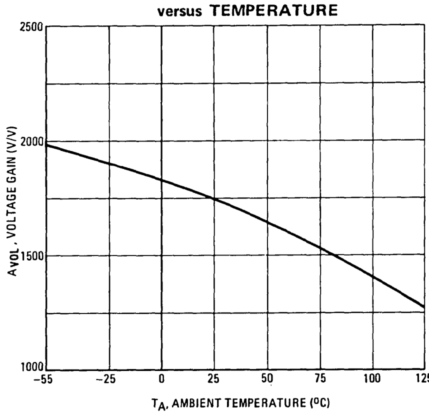


FIGURE 7 – RESPONSE TIME

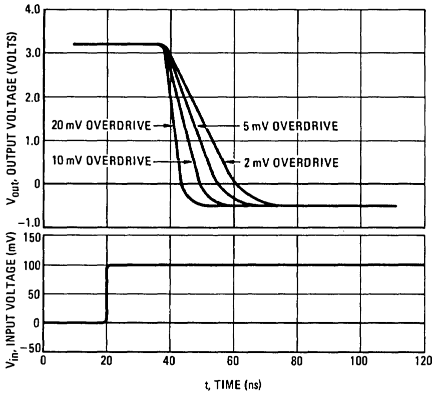


FIGURE 8 – POWER DISSIPATION versus TEMPERATURE

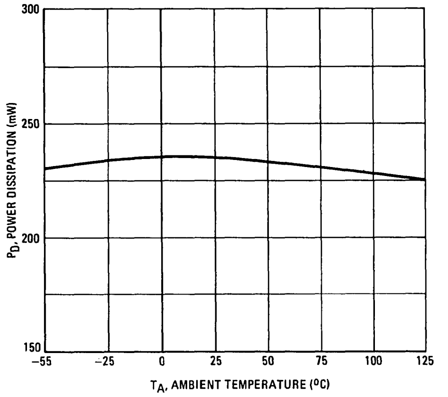


FIGURE 9 – RECOMMENDED SERIES RESISTANCE versus MRTL LOADS

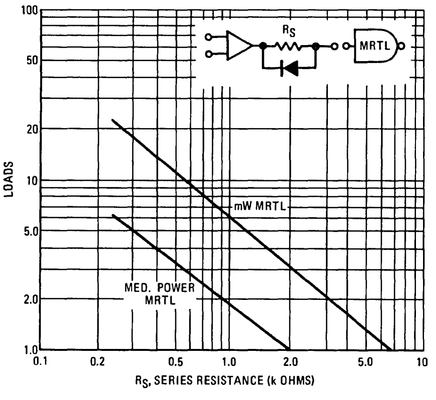


FIGURE 10 – SINK CURRENT versus TEMPERATURE

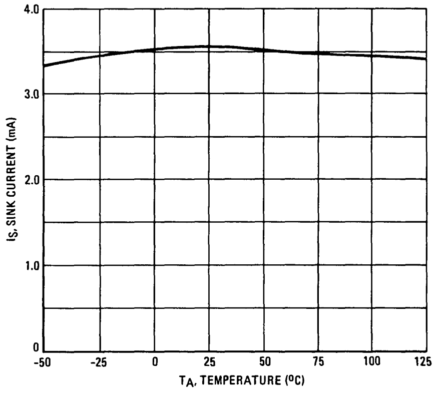
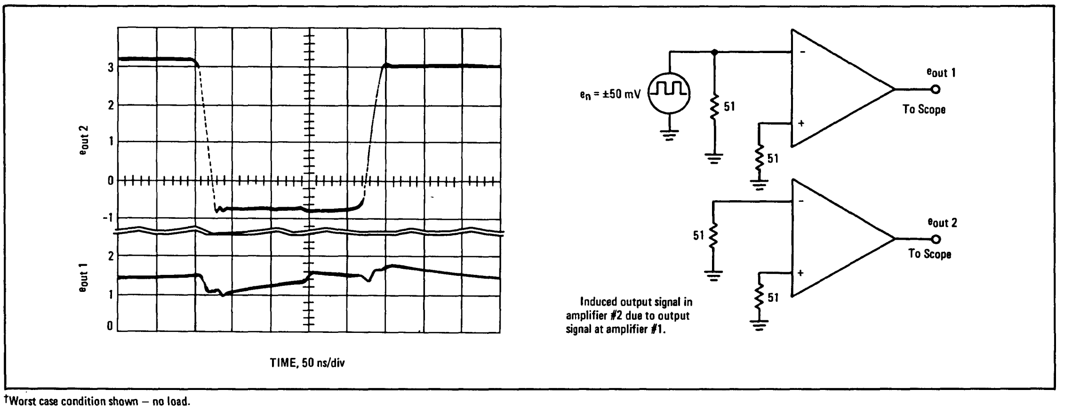


FIGURE 11 – CROSSTALK†

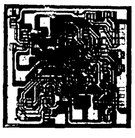


†Worst case condition shown – no load.

MC1520
MC1420

OPERATIONAL AMPLIFIERS

MONOLITHIC DIFFERENTIAL OUTPUT OPERATIONAL AMPLIFIER



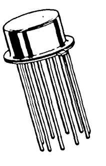
. . . designed for use in general-purpose or wide-band differential amplifier applications, especially those requiring differential outputs.

Typical Characteristics

- Differential Input and Differential Output
- Wide Closed-Loop Bandwidth; 10 MHz
- Differential Gain; 70 dB
- High Input Impedance; 2.0 megohms:
- Low Output Impedance; 50 ohms

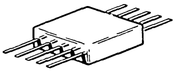
OPERATIONAL AMPLIFIER

MONOLITHIC SILICON
INTEGRATED
CIRCUIT



Pin 3 connected to case

G SUFFIX
METAL PACKAGE
CASE 602A



F SUFFIX
CERAMIC PACKAGE
CASE 606
TO-91

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+ V^-	+8.0 -8.0	Vdc
Differential Input Signal	V_{in}	±8.0	Vdc
Load Current	I_{L1}, I_{L2}	15	mA
Power Dissipation (Package Limitation) Metal Package Derate above T_A = +25°C Flat Package Derate above T_A = +25°C	P_D	 680 4.6 500 3.3	 mW mW/°C mW mW/°C
Operating Temperature Range MC1520 MC1420	T_A	-55 to +125 0 to + 75	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

6

CIRCUIT SCHEMATICS

FIGURE 1 – CIRCUIT SCHEMATIC

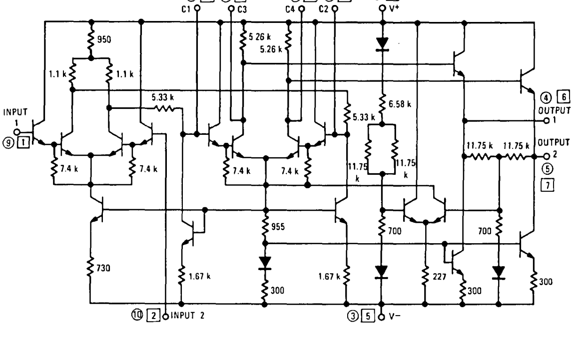
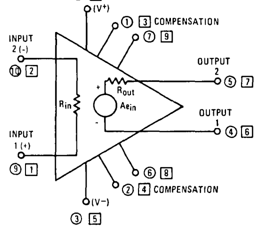


FIGURE 2 – EQUIVALENT CIRCUIT



○ contains pin number for metal can package
□ contains pin number for flat package

See Packaging Information Section for outline dimensions.

SINGLE-ENDED ELECTRICAL CHARACTERISTICS

(V^+ = +6.0 Vdc, V^-=-6.0 Vdc, T_A = +25°C unless otherwise noted)

Characteristic	Symbol	MC1520 Min	MC1520 Typ	MC1520 Max	MC1420 Min	MC1420 Typ	MC1420 Max	Unit
Open Loop Voltage Gain (T_{low} ② ≦ T_A ≦ T_{high} ②)	A_{VOL}	1000 60	1500 64	– –	750 –	1500 64	– –	V/V dB
Output Impedance (f = 20 Hz)	Z_{out}	–	50	100	–	50	–	ohms
Input Impedance (f = 20 Hz)	Z_{in}	0.5	2.0	–	–	2.0	–	megohms
Output Voltage Swing (R_L = 7.0 kΩ [Figure 8])	V_o	±3.5	±4.0	–	±3.0	±4.0	–	V_{peak}
Input Common-Mode Voltage Swing	CMV_{in}	±2.0	±3.0	–	–	±3.0	–	V_{peak}
Common-Mode Rejection Ratio	CM_{rej}	75	90	–	60	90	–	dB
Input Bias Current $\left(\left[I_b = \frac{I_1 + I_2}{2}\right], T_A = +25^\circ C\right)$	I_b	–	0.8	2.0	–	2.0	40	µA
Input Offset Current ($I_{io} = I_1 - I_2$) ($I_{io} = I_1 - I_2$, $T_A = T_{low}$) ($I_{io} = I_1 - I_2$, $T_A = T_{high}$)	$\lvert I_{io}\rvert$	– – –	30 – –	100 200 200	– – –	30 – –	200 – –	nA
Input Offset Voltage (T_A = +25°C)	$\lvert V_{io}\rvert$	–	5.0	10	–	5.0	15	mV
Step Response Gain = 1.0, 10% Overshoot R_1 = 10 kΩ R_2 = 10 kΩ R_3 = 5.0 kΩ C_s = 39 pF	t_f t_{pd} dV_{out}/dt ①	– – –	80 70 5.0	– – –	– – –	80 70 5.0	– – –	ns ns V/µs
Gain = 10, 10% Overshoot R_1 = 10 kΩ R_2 = 100 kΩ R_3 = 10 kΩ C_s = 10 pF	t_f t_{pd} dV_{out}/dt ①	– – –	80 70 15	– – –	– – –	80 70 15	– – –	ns ns V/µs
Gain = 100, No Overshoot R_1 = 1.0 kΩ R_2 = 100 kΩ R_3 = 1.0 kΩ C_s = 1.0 pF	t_f t_{pd} dV_{out}/dt ①	– – –	80 70 30	– – –	– – –	80 70 30	– – –	ns ns V/µs
Open Loop, No Overshoot R_1 = 50 Ω R_2 = ∞ R_3 = 50 Ω C_s = 0	t_f t_{pd} dV_{out}/dt ①	– – –	180 70 35	– – –	– – –	180 70 35	– – –	ns ns V/µs
Bandwidth: (Open Loop [Figure 4]) (Closed Loop [Unity Gain]) (Figure 5)	–	– –	2.0 10	– –	– –	2.0 10	– –	MHz
Input Noise Voltage (Open Loop) (5.0 Hz - 5.0 MHz)	$V_{n(in)}$	–	11	15	–	11	–	µV(rms)
Average Temperature Coefficient of Input Offset Voltage (R_S = 50 Ω, T_A = T_{low} to T_{high})	$\lvert TCV_{io}\rvert$	–	2.0	–	–	2.0	–	µV/°C
DC Power Dissipation (V_o = 0)	P_D	–	120	240	–	120	240	mW
Power Supply Sensitivity ($V^{\pm}$ Constant)	$S^{\pm}$	–	250	450	–	250	–	µV/V

① dV_{out}/dt = Slew Rate   ② T_{low} = 0°C for MC1420, -55°C for MC1520 T_{high} = +75°C for MC1420, +125°C for MC1520

DIFFERENTIAL ELECTRICAL CHARACTERISTICS

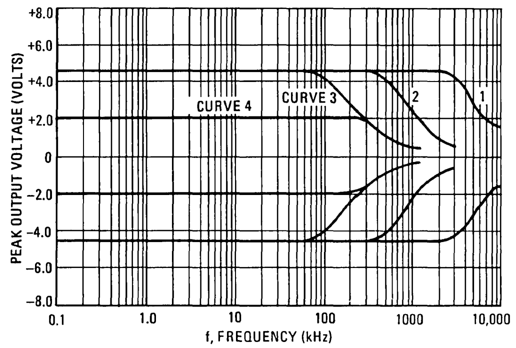
(V^+ = +6.0 Vdc, V^- = -6.0 Vdc, T_A = +25°C unless otherwise noted)

Characteristic	Symbol	MC1520 Min	MC1520 Typ	MC1520 Max	MC1420 Min	MC1420 Typ	MC1420 Max	Unit
Gain (Open Loop)	A_{VOL}	2000 66	3000 70	– –	1500 64	3000 70	– –	V/V dB
Input Impedance (f = 20 Hz)	Z_{in}	0.5	2.0	–	–	2.0	–	megohms
Output Impedance (f = 20 Hz)	Z_{out}	–	100	200	–	100	–	ohms
Common-Mode Output Voltage	V_o (CM)	-0.5	0	+0.5	–	0	–	Vdc
Output Voltage Swing (R_L = 7.0 kΩ)	V_o	±7.0	±8.0	–	±6.0	±8.0	–	V_{peak}

TYPICAL CHARACTERISTICS

(V^+ = +6.0 Vdc, V^- = -6.0 Vdc, T_A = +25°C, unless otherwise noted.)

FIGURE 3 – LARGE SIGNAL SWING versus FREQUENCY



TEST CIRCUIT

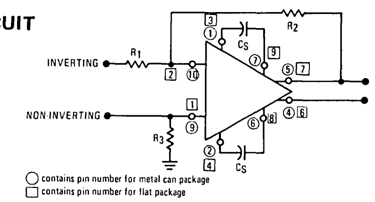


FIGURE NO.	CURVE NO.	MODE	VOLTAGE GAIN	TEST CONDITIONS R_1 (Ω)	R_2 (Ω)	R_3 (Ω)	C_S (pF)	NOISE OUTPUT mV (rms)
3	1	INVERTING	100	1.0 k	100 k	1.0 k	1.0	2.0
	2	INVERTING	10	10 k	100 k	10 k	10	0.55
	3	INVERTING	1.0	10 k	10 k	5.0 k	39	0.17
	4	NON-INVERTING	1.0	∞	10 k	10 k	39	0.17
4	1	NON-INVERTING	A_{VOL}	0	∞	50	1.0	1.0
	2	NON-INVERTING	A_{VOL}	0	∞	50	10	2.0
	3	NON-INVERTING	A_{VOL}	0	∞	50	39	5.2
5	1	NON-INVERTING	100	100	10 k	100	1.0	2.0
	2	NON-INVERTING	10	1.0 k	9.1 k	910	10	0.55
	3	NON-INVERTING	1.0	∞	10 k	10 k	39	0.17

FIGURE 4 – OPEN LOOP VOLTAGE GAIN

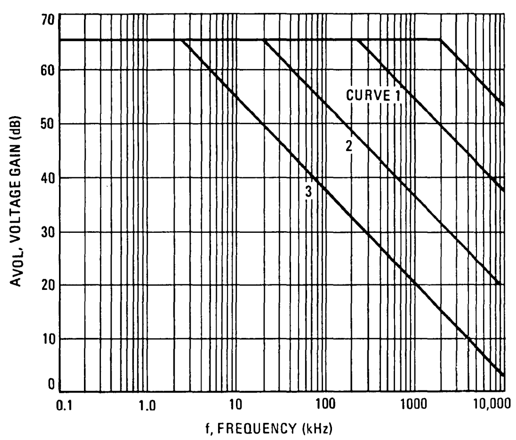
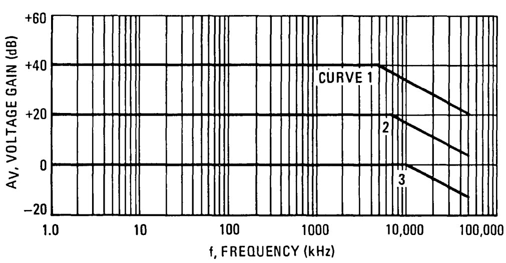


FIGURE 5 – CLOSED LOOP VOLTAGE GAIN versus FREQUENCY



TYPICAL OUTPUT CHARACTERISTICS

(V^+ = +6.0 Vdc, V^- = -6.0 Vdc, unless otherwise noted.)

FIGURE 6 – POWER DISSIPATION versus POWER SUPPLY VOLTAGE

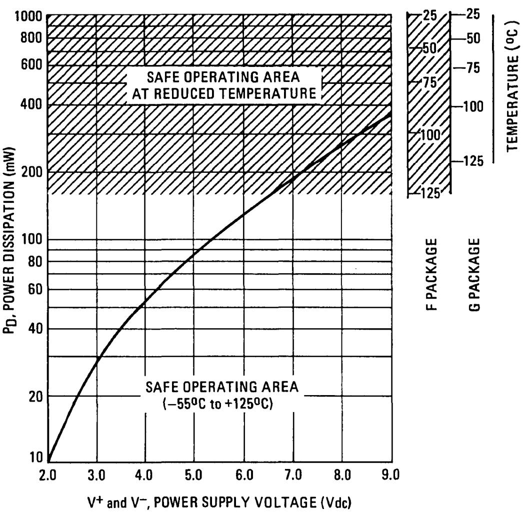


FIGURE 7 – OPEN LOOP VOLTAGE GAIN versus SUPPLY VOLTAGE

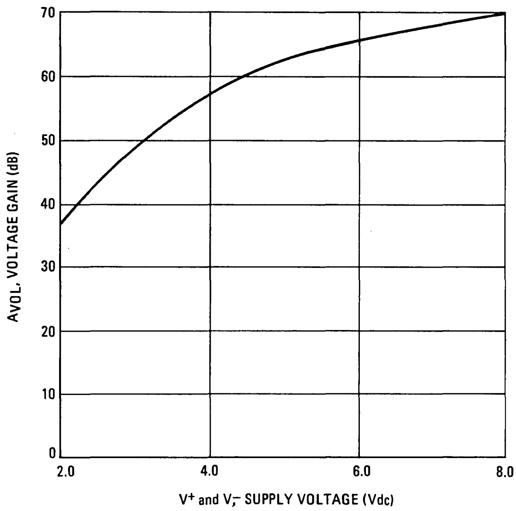


FIGURE 8 – SINGLE ENDED OUTPUT VOLTAGE versus LOAD RESISTANCE

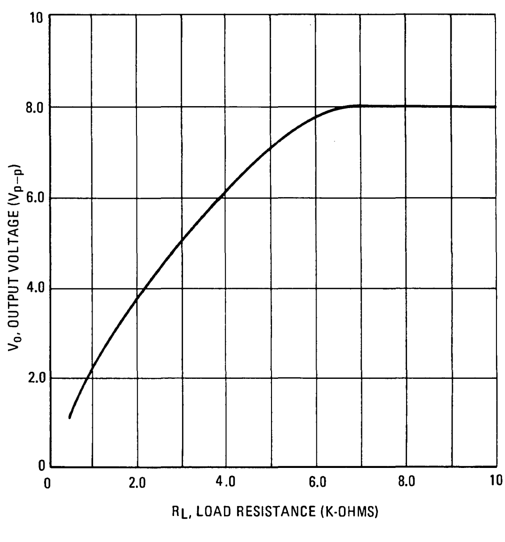
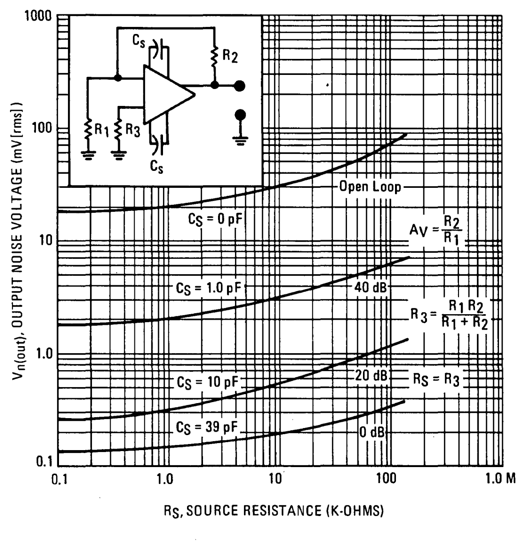


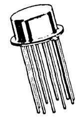
FIGURE 9 – OUTPUT NOISE VOLTAGE versus SOURCE RESISTANCE



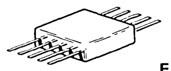
MC1530
MC1531

OPERATIONAL AMPLIFIERS

Lead 4 connected to case



G SUFFIX
METAL PACKAGE
CASE 602B



F SUFFIX
CERAMIC PACKAGE
CASE 606
TO-91

. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

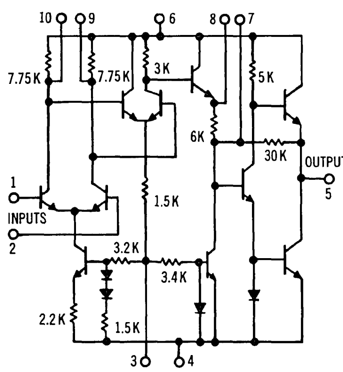
Typical Amplifier Features:

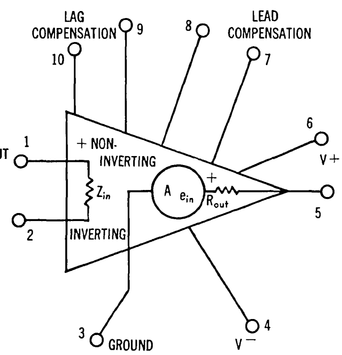
- Excellent Open Loop Gain Characteristics
  A_{VOL} = 74 dB typical
  A_{VOL} stability = ±1.5 dB from -55°C to +125°C
- Low Temperature Drift — ±3.0 μV/°C
- Large Output Voltage Swing — Typically ±5.0 V @ ±6.0 V Supply
- Low Output Impedance — Z_{out} = 25 ohms typical
- High Slew Rate — typically 4.5 V/μs @ A_V = 10

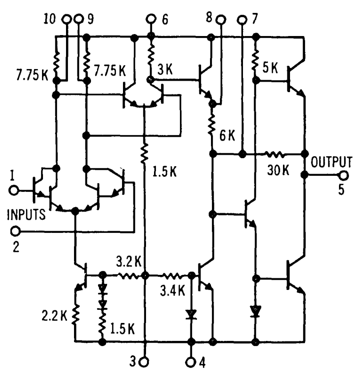
MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V+	+9.0	Vdc
Power Supply Voltage	V-	-9.0	Vdc
Differential Input Signal	V_{in}	±5.0	Vdc
Load Current	I_L	10	mA
Power Dissipation (Package Limitation)	P_D		
Metal Can		680	mW
Derate above 25+ C		4.6	mW/°C
Flat Package		500	mW
Derate above 25° C		3.3	mW/°C
Operating Temperature Range	T_A	-55 to + 125	°C
Storage Temperature Range	T_{stg}	-65 to + 175	°C

MC1530 (STANDARD INPUT) — **EQUIVALENT CIRCUIT (BOTH TYPES)** — **MC1531 (DARLINGTON INPUT)**



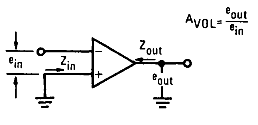
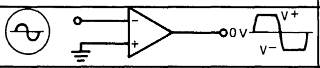
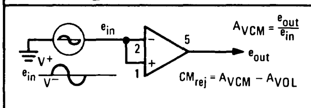
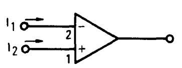
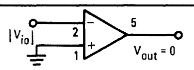
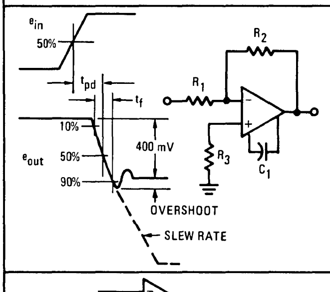
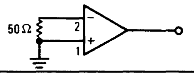
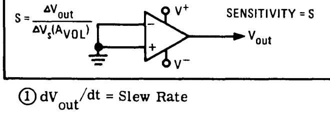




See Packaging Information Section for outline dimensions.

MC1530, MC1531 (continued)

ELECTRICAL CHARACTERISTICS (V^+ = +6.0Vdc, V^- = −6.0Vdc, T_A = 25°C unless otherwise noted)

Characteristic Definitions (linear operation)	Characteristic	Symbol	Min	Typ	Max	Unit
	Open Loop Voltage Gain (T_A = -55 to + 125° C) MC1530 MC1531	A_{VOL}	4500 2500	5000 3500	12500 7000	V/V
	MC1530 MC1531		73 68	74 71	82 77	dB
	Output Impedance (f = 20 Hz)	Z_{out}	-	25	50	ohms
	Input Impedance (f = 20 Hz) MC1530 MC1531	Z_{in}	10k 1.0M	20k 2.0M	- -	ohms
	Output Voltage Swing (R_L = 1.0 k ohm)	V_{out}	±4.5	±5.2	-	V_{peak}
	Input Common Mode Voltage Swing MC1530 MC1531	CMV_{in}	±2.0 ±2.0	±2.7 ±2.4	- -	V_{peak}
	Common Mode Rejection Ratio MC1530 MC1531	CM_{rej}	70 65	75 65	- -	dB
	Input Bias Current ($I_b = \frac{I_1 + I_2}{2}$) MC1530 MC1531	I_b	- -	3.0 0.025	10 0.150	µA
	Input Offset Current MC1530 $I_{io} = I_1 - I_2$ MC1531	I_{io}	- -	0.200 0.003	2.0 0.025	µA
	Input Offset Voltage MC1530 MC1531	$\lvert V_{io} \rvert$	- -	1.0 3.0	5.0 10	mV
	Step Response Gain = 100, 0% overshoot R_1 = 1.0 k ohm R_2 = 100 k ohm R_3 = 1.0 k ohm C_1 = 1800 pF	 t_f t_{pd} dV_{out}/dt ①	 - - -	 0.60 0.30 17	 - - -	 µs µs V/µs
	Gain = 10, 10% overshoot R_1 = 10 k ohm R_2 = 100 k ohm R_3 = 10 k ohm C_1 = 6800 pF	t_f t_{pd} dV_{out}/dt ①	- - -	0.24 0.18 4.5	- - -	µs µs V/µs
	Gain = 1.0, 5.0% overshoot R_1 = 10 k ohm R_2 = 10 k ohm R_3 = 5.0 k ohm C_1 = 33,000 pF	t_f t_{pd} dV_{out}/dt ①	- - -	0.20 0.16 1.0	- - -	µs µs V/µs
	Input Noise Voltage (Open Loop, 50 ohm MC1530 source, BW_{OL} = 5.0 MHz) MC1531	$V_{n(in)}$	- -	10 20	- -	μV_{rms}
	Average Temperature Coefficient of Input Offset Voltage 25°C to + 125° C MC1530 -55° C to + 25° C 25°C to + 125° C MC1531 -55° C + 25° C	TC_{Vio}	- - - -	3.8 8.0 11 20	- - - -	µV/°C
	D. C. Power Dissipation (Power Supply = ±6.0 V, V_{out}= 0)	P_D	-	110	150	mW
	Positive Supply Sensitivity (V^- constant)	S^+	-	100	-	µV/V
	Negative Supply Sensitivity (V^+ constant)	S^-	-	100	-	µV/V

① dV_{out}/dt = Slew Rate

6

TYPICAL OUTPUT CHARACTERISTICS

$V^+ = +6.0$ Vdc, $V^- = -6.0$ Vdc, $T_A = 25^oC$)

FIGURE 1 – TEST CIRCUIT

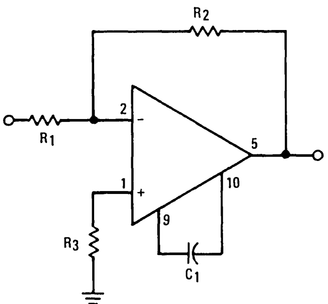


FIG. NO.	CURVE NO.	VOLTAGE GAIN	DEVICE	TEST CONDITIONS $R_1 (\Omega)$	$R_2 (\Omega)$	$R_3 (\Omega)$	C_1(pF)	OUTPUT NOISE (mV rms)
2	1	100	MC1530	1.0 k	100 k	1.0 k	1800	3.5
		100	MC1531	1.0 k	100 k	1.0 k	1800	3.4
	2	10	MC1530	10 k	100 k	10 k	6800	4.8
		10	MC1531	10 k	100 k	10 k	6800	4.8
	3	1.0	MC1530	10 k	10 k	5.0 k	33000	3.4
		1.0	MC1531	10 k	10 k	5.0 k	33000	7.0
3	1	100	MC1530	1.0 k	100 k	1.0 k	1800	3.5
		100	MC1531	1.0 k	100 k	1.0 k	1800	3.4
	2	10	MC1530	10 k	100 k	10 k	6800	4.8
		10	MC1531	10 k	100 k	10 k	6800	4.8
	3	1.0	MC1530	10 k	10 k	5.0 k	33000	3.4
		1.0	MC1531	10 k	10 k	5.0 k	33000	7.0
4	1	A_{VOL}	MC1530	0	∞	0	1800	7.6
		A_{VOL}	MC1531	0	∞	0	1800	19.0
	2	A_{VOL}	MC1530	0	∞	0	6800	5.5
		A_{VOL}	MC1531	0	∞	0	6800	15.0
	3	A_{VOL}	MC1530	0	∞	0	33000	5.0
		A_{VOL}	MC1531	0	∞	0	33000	11.0

FIGURE 2 – LARGE SIGNAL SWING versus FREQUENCY

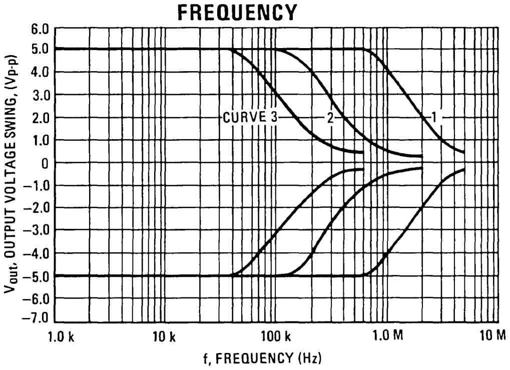


FIGURE 3 – VOLTAGE GAIN versus FREQUENCY

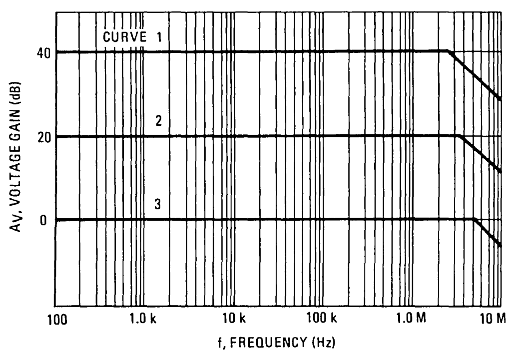


FIGURE 4 – OPEN LOOP VOLTAGE GAIN versus FREQUENCY

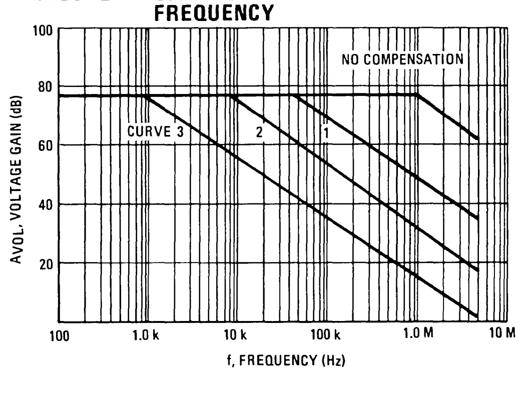


FIGURE 5 – SLEW RATE versus ROLLOFF CAPACITANCE

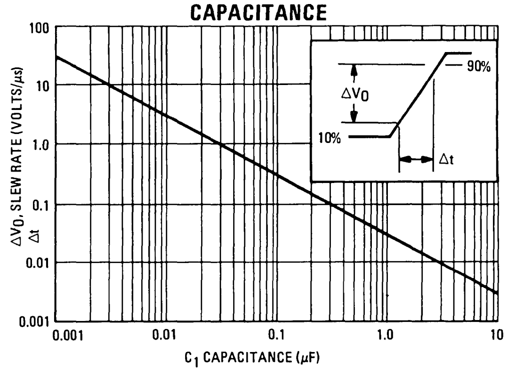


FIGURE 6 – VOLTAGE GAIN versus POWER SUPPLY VOLTAGE

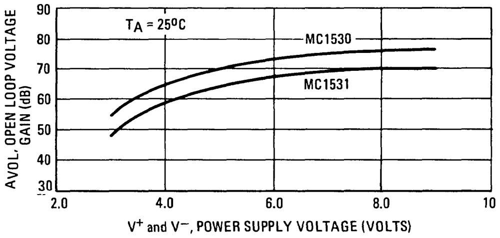


FIGURE 7 – COMMON MODE SWING versus POWER SUPPLY VOLTAGE

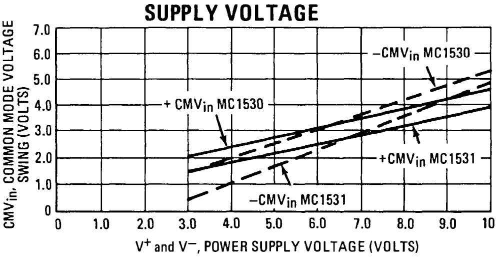


FIGURE 8 – POWER DISSIPATION versus POWER SUPPLY VOLTAGE

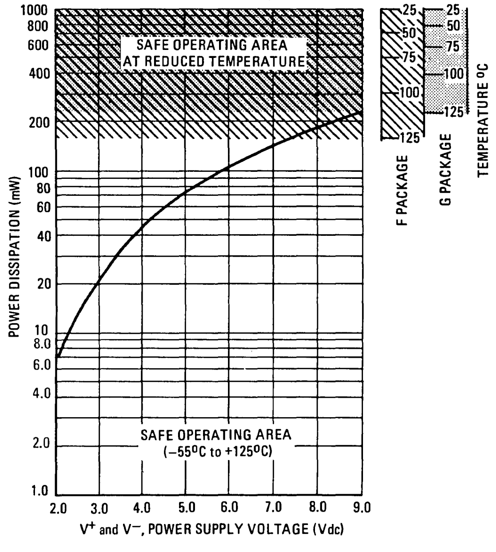
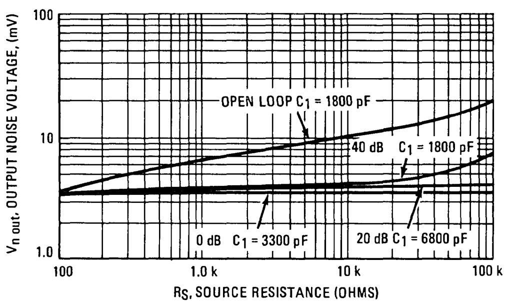


FIGURE 9 – OUTPUT NOISE VOLTAGE versus SOURCE RESISTANCE



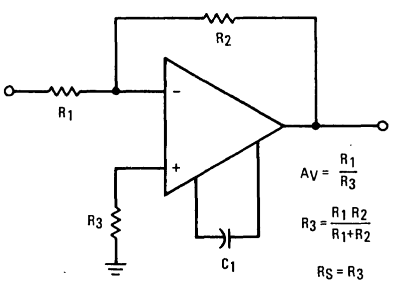
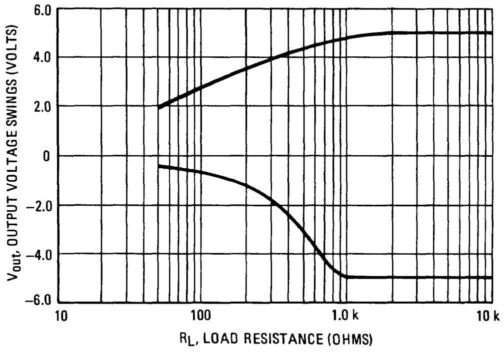


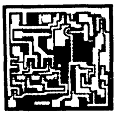
FIGURE 10 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE



MC1533
MC1433

OPERATIONAL AMPLIFIERS

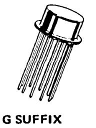
MONOLITHIC OPERATIONAL AMPLIFIER



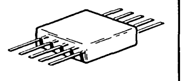
. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

- High-Performance Open Loop Gain Characteristics
  A_{VOL} = 60,000 typical
- Low Temperature Drift – ±5 μV/^{o}C
- Large Output Voltage Swing –
  ±13 V typical @ ±15 V Supply
- Low Output Impedance – Z_{out} = 100 ohms typical

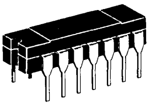
OPERATIONAL AMPLIFIER MONOLITHIC SILICON INTEGRATED CIRCUIT



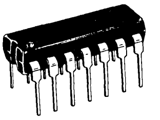
G SUFFIX
METAL PACKAGE
CASE 602B



F SUFFIX
CERAMIC PACKAGE
CASE 606
TO-91



L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116



P SUFFIX
PLASTIC PACKAGE
CASE 605
TO-116
(MC1433P Only)

6

FIGURE 1 – CIRCUIT SCHEMATIC

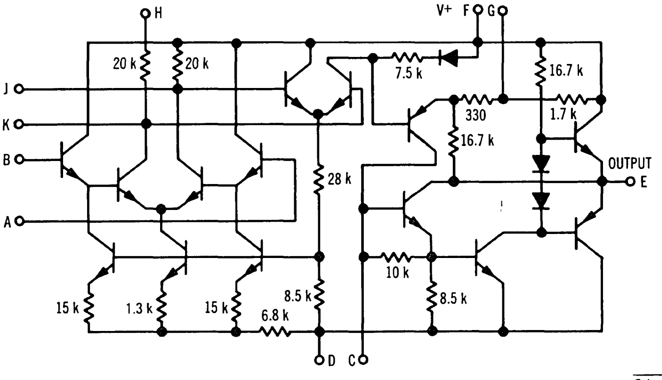
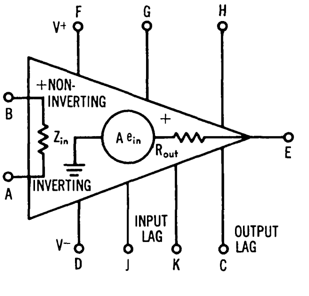


FIGURE 2 – EQUIVALENT CIRCUIT



PIN CONNECTIONS

Schematic	A	B	C	D	E	F	G	H	J	K
"G" Package	1	2	3	4	5	6	7	8	9	10
"F" Package	10	1	2	3	4	5	6	7	8	9
"L" & "P" Packages	4	5	6	7	11	12	13	14	2	3

See Packaging Information Section for outline dimensions.

ELECTRICAL CHARACTERISTICS (V^+ = +15 Vdc, V^- = -15 Vdc, T_A = +25°C unless otherwise noted)

Characteristic	Symbol	MC1533 Min	MC1533 Typ	MC1533 Max	MC1433 Min	MC1433 Typ	MC1433 Max	Unit
Open Loop Voltage Gain	A_{VOL}							–
(T_A = +25°C)		40,000	60,000	–	30,000	60,000	–	
(T_A = T_{low} ① to T_{high} ①)		35,000	50,000	–	20,000	50,000	–	
Output Impedance (f = 20 Hz)	Z_{out}	–	100	150	–	100	150	Ω
Input Impedance (f = 20 Hz)	Z_{in}	500	1000	–	300	600	–	kΩ
Output Voltage Swing	V_o							V_{peak}
(R_L = 10 kΩ)		±12	±13	–	±12	±13	–	
(R_L = 2 kΩ)		±11	±12	–	±10	±12	–	
Input Common Mode Voltage Swing	CMV_{in}	+9.0	+10	–	+8.0	+9.0	–	V_{peak}
		-8.0	-9.0	–	-8.0	-9.0	–	
Common Mode Rejection Ratio	CM_{rej}	90	100	–	80	100	–	dB
Input Bias Current	I_b							μA
(T_A = +25°C)		–	0.5	1.0	–	0.5	2.0	
(T_A = T_{low})		–	–	3.0	–	–	4.0	
Input Offset Current	$\|I_{io}\|$							μA
(T_A = +25°C)		–	0.03	0.15	–	0.1	0.50	
(T_A = T_{low})		–	–	0.5	–	–	0.75	
(T_A = T_{high})		–	–	0.2	–	–	0.75	
Input Offset Voltage ②	$\|V_{io}\|$							mV
(T_A = +25°C)		–	1.0	5.0	–	1.0	7.5	
(T_A = T_{low}, T_{high})		–	–	6.0	–	–	10	
Step Response (C_2 = 10 pF)								
Gain = 100, 10% overshoot,	t_f	–	0.25	–	–	0.25	–	μs
R_1 = 10 kΩ, R_2 = 1.0 MΩ,	t_{pd}	–	0.1	–	–	0.1	–	μs
R_3 = 100 Ω, C_1 = 0.01 μF	dV_{out}/dt ③	–	6.2	–	–	6.2	–	V/μs
Gain = 10, no overshoot,	t_f	–	0.3	–	–	0.3	–	μs
R_1 = 10 kΩ, R_2 = 100 kΩ,	t_{pd}	–	0.1	–	–	0.1	–	μs
R_3 = 10 Ω, C_1 = 0.1 μF	dV_{out}/dt ③	–	2.9	–	–	2.9	–	V/μs
Gain = 1, 5% overshoot,	t_f	–	0.2	–	–	0.2	–	μs
R_1 = 10 kΩ, R_2 = 10 kΩ,	t_{pd}	–	0.1	–	–	0.1	–	μs
R_3 = 10 Ω, C_1 = 1.0 μF	dV_{out}/dt ③	–	2.0	–	–	2.0	–	V/μs
Average Temperature Coefficient of Input Offset Voltage	$\|TC_{Vio}\|$							μV/°C
(T_A = T_{low} to +25°C)		–	8.0	–	–	10	–	
(T_A = +25°C to T_{high})		–	5.0	–	–	8.0	–	
Average Temperature Coefficient of Input Offset Current	$\|TC_{Iio}\|$							nA/°C
(T_A = T_{low} to T_{high})		–	0.1	–	–	0.1	–	
(T_A = +25°C to T_{high})		–	0.05	–	–	0.05	–	
DC Power Dissipation (Power Supply = ±15 V, V_o = 0)	P_D	–	125	170	–	125	240	mW
Positive Supply Sensitivity (V^- constant)	S^+	–	50	150	–	50	200	μV/V
Negative Supply Sensitivity (V^+ constant)	S^-	–	50	150	–	50	200	μV/V

① T_{high} = +75°C for MC1433, +125°C for MC1533; T_{low} = 0 for MC1433, -55°C for MC1533

② Input offset voltage (V_{io}) may be adjusted to zero.

③ dV_{out}/dt = Slew Rate

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage MC1533,MC1433	V^+	+20,+18	Vdc
MC1533,MC1433	V^-	-20,-18	Vdc
Differential Input Signal	V_{in}	±10	Volts
Common Mode Input Swing	CMV_{in}	$\pm V^+$	Volts
Load Current	I_L	10	mA
Output Short Circuit Duration	t_S	1.0	s
Power Dissipation (Package Limitation)	P_D		
Metal Package		680	mW
Derate above T_A = +25°C		4.6	mW/°C
Flat Package		500	mW
Derate above T_A = +25°C		3.3	mW/°C
Dual In-Line Ceramic Package		625	mW
Derate above T_A = +25°C		5.0	mW/°C
Dual In-Line Plastic Package		400	mW
Derate above T_A = +25°C		3.3	mW/°C
Operating Temperature Range	T_A		°C
MC1533		-55 to +125	
MC1433		0 to +75	
Storage Temperature Range	T_{stg}		°C
Metal and Ceramic Packages		-65 to +150	
Plastic Package		-65 to +125	

TYPICAL CHARACTERISTICS

FIGURE 3 – TEST CIRCUIT

V^+ = +15 Vdc, V^- = -15 Vdc, T_A = +25°C

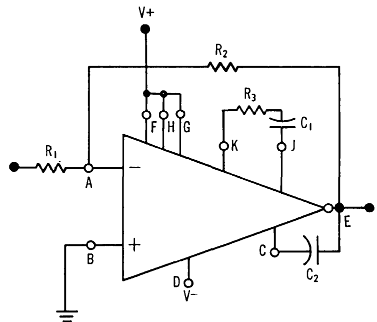


Fig. No.	Curve No.	Test Conditions				
		R_1 (Ω)	R_2 (Ω)	R_3 (Ω)	C_1 (μF)	C_2 (pF)
4	1	10 k	10 k	10	1.0	10
	2	10 k	100 k	10	0.1	10
	3	10 k	1.0 M	100	0.01	10
	3	1.0 k	1.0 M	390	0.002	10
5	1	10 k	10 k	10	1.0	10
	2	10 k	100 k	10	0.1	10
	3	10 k	1.0 M	100	0.01	10
	4	1.0 k	1.0 M	390	0.002	10
6	1	0	∞	10	1.0	10
	2	0	∞	10	0.1	10
	3	0	∞	100	0.01	10
	4	0	∞	390	0.002	10

TYPICAL CHARACTERISTICS (continued)

(V^+ = +15 Vdc, V^- = -15 Vdc, T_A = + 25°C unless otherwise noted)

FIGURE 4 – LARGE-SIGNAL SWING versus FREQUENCY

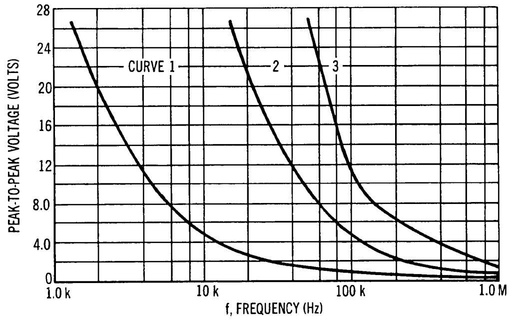


FIGURE 5 – VOLTAGE GAIN versus FREQUENCY

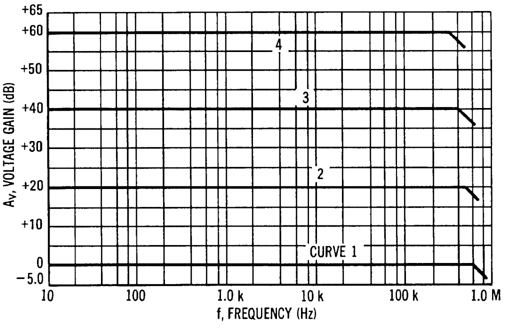


FIGURE 6 – OFFSET ADJUST CIRCUIT

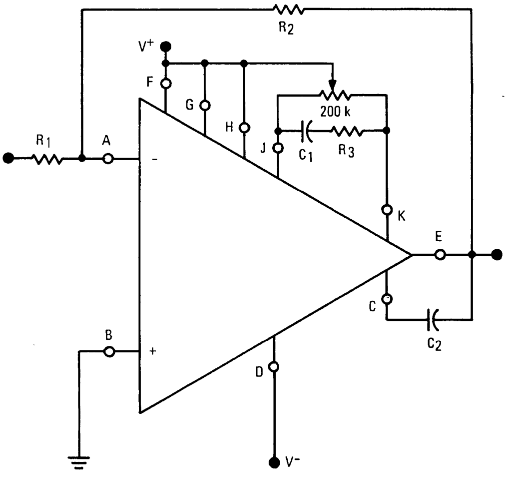
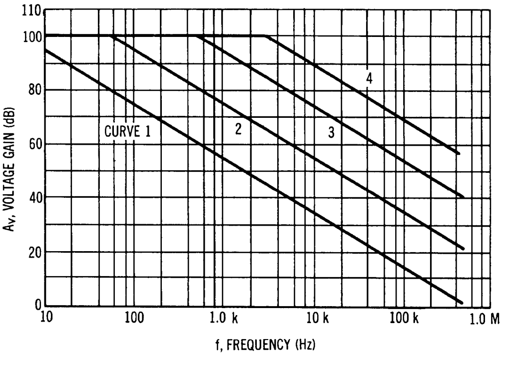


FIGURE 7 – OPEN LOOP VOLTAGE GAIN versus FREQUENCY
(HIGH GAIN CONFIGURATION)



PIN CONNECTIONS

Schematic	A	B	C	D	E	F	G	H	J	K
"G" Package	1	2	3	4	5	6	7	8	9	10
"F" Package	10	1	2	3	4	5	6	7	8	9
"L" & "P" Packages	4	5	6	7	11	12	13	14	2	3

6

TYPICAL CHARACTERISTICS (continued)

FIGURE 8 – POWER DISSIPATION versus POWER SUPPLY VOLTAGE

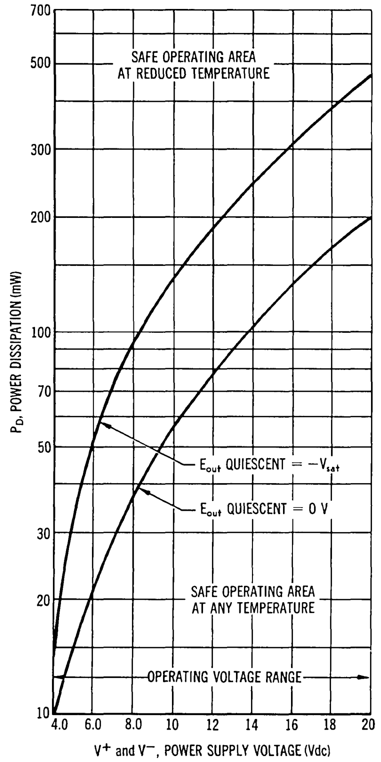


FIGURE 9 – VOLTAGE GAIN versus POWER SUPPLY VOLTAGE

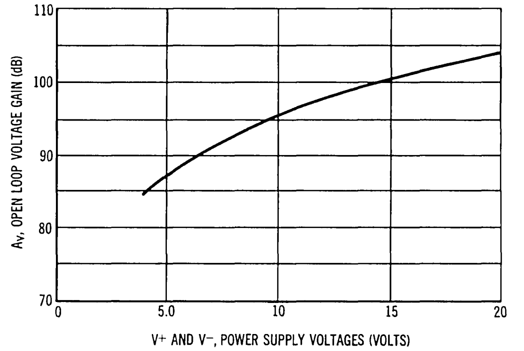


FIGURE 10 – COMMON MODE SWING versus POWER SUPPLY VOLTAGE

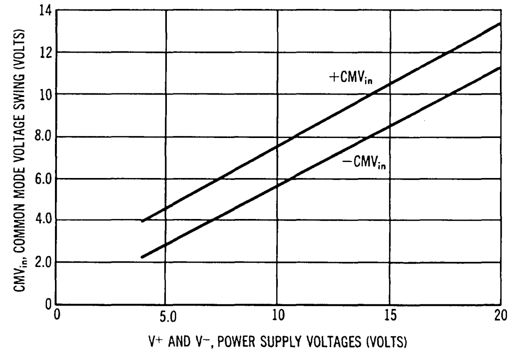
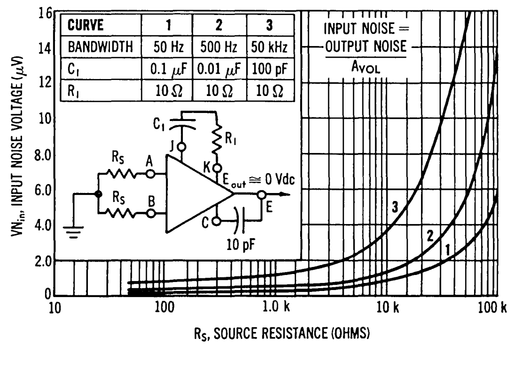


FIGURE 11 – INPUT NOISE VOLTAGE versus SOURCE RESISTANCE

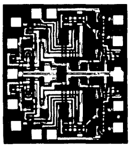


6

MC1535
MC1435

OPERATIONAL AMPLIFIERS

MONOLITHIC DUAL OPERATIONAL AMPLIFIERS



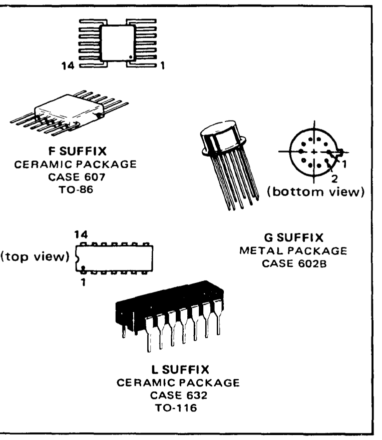
. . . designed for use as summing amplifiers, integrators, or amplifiers with operating characteristics as a function of the external feedback components. Ideal for chopper stabilized applications where extremely high gain is required with excellent stability.

Typical Amplifier Features:

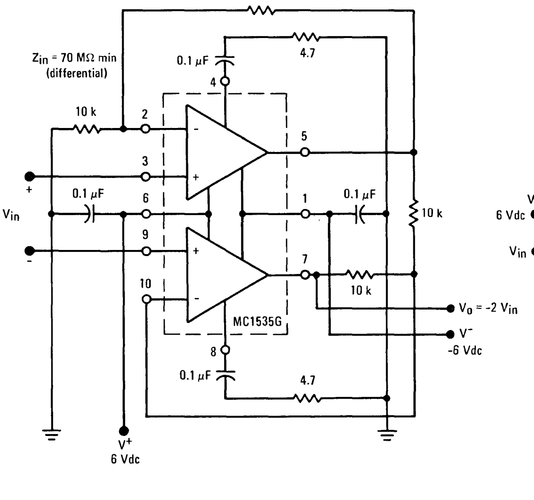
- High Open Loop Gain Characteristics – A_{VOL} = 7,000
- Low Temperature Drift – ±10 μV/°C
- Low Input Offset Voltage – 1.0 mV
- Low Input Noise Voltage – 0.5 μV

MONOLITHIC DUAL OPERATIONAL AMPLIFIERS INTEGRATED CIRCUIT

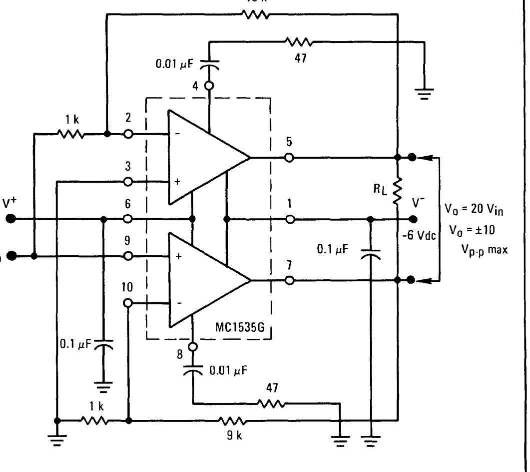
EPITAXIAL PASSIVATED



HIGH Z_{in}, DIFFERENTIAL TO SINGLE-ENDED AMPLIFIER

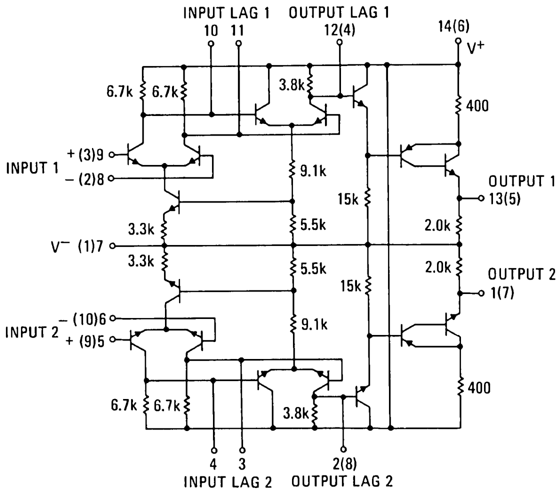


LARGE OUTPUT SWING CONFIGURATION (FLOATING LOAD)

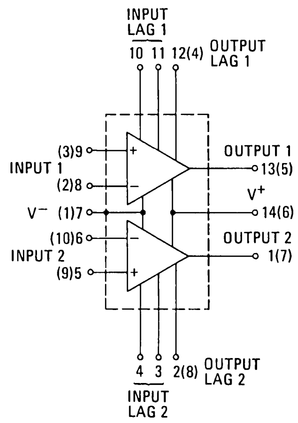


See Packaging Information Section for outline dimensions.

CIRCUIT SCHEMATIC



EQUIVALENT CIRCUIT



Number at end of terminal is pin number for ceramic packages.
Number in parenthesis is pin number for metal package. Input Lag available only in ceramic packages.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating		Symbol	MC1535	MC1435	Unit
Power Supply Voltage		V^+ V^-	+10 -10	+9.0 -9.0	Vdc
Differential Input Signal		V_{in}	±5.0	±5.0	Volts
Common-Mode Input Swing		CMV_{in}	+5.0 -4.0	+5.0 -4.0	Volts
Load Current		I_L	20	20	mA
Output Short Circuit Duration		T_{SC}	Continuous		
Power Dissipation (Package Limitation)		P_D			
Flat Ceramic Package	MC1535F, MC1435F		500		mW
Derate above T_A = +25°C			3.3		mW/°C
Metal Package	MC1535G, MC1435G		680		mW
Derate above T_A = +25°C			4.6		mW/°C
Ceramic Dual In-Line Package	MC1435L		625		mW
Derate above T_A = +25°C			5.0		mW/°C
Operating Temperature Range		T_A	-55 to +125	0 to +75	°C
Storage Temperature Range		T_{stg}	-65 to +150	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (Each Amplifier) (V^+ = +6.0 Vdc, V^- = -6.0 Vdc, T_A = +25°C unless otherwise noted)

Characteristics	Symbol	MC1535 Min	MC1535 Typ	MC1535 Max	MC1435 Min	MC1435 Typ	MC1435 Max	Unit
Input Bias Current	I_b							
$I_b = \frac{I_1 + I_2}{2}$, T_A = +25°C		–	1.2	3.0	–	1.2	5.0	µAdc
$T_A = T_{low}$ to T_{high} ①		–	–	6.0	–	–	10	
Input Offset Current	$\|I_{io}\|$							nAdc
T_A = +25°C		–	50	300	–	50	500	
T_A = +25°C to T_{high}		–	–	300	–	–	1500	
$T_A = T_{low}$ to +25°C		–	–	900	–	–	1500	
Input Offset Voltage	$\|V_{io}\|$							mVdc
T_A = +25°C		–	1.0	3.0	–	1.0	5.0	
$T_A = T_{low}$ to T_{high}		–	–	5.0	–	–	7.5	
Differential Input Impedance (Open-Loop, f = 20 Hz)								
Parallel Input Resistance	R_p	10	45	–	10	45	–	kohms
Parallel Input Capacitance	C_p	–	6.0	–	–	–	–	pF
Common-Mode Input Impedance (f = 20 Hz)	$Z_{(in)}$	–	250	–	–	250	–	Meg ohms
Common-Mode Input Voltage Swing	CMV_{in}	+3.0 -2.0	+3.9 -2.7	– –	+3.0 -2.0	+3.9 -2.7	– –	V_{pk}
Equivalent Input Noise Voltage (A_V = 100, R_s = 10 kohms, f = 1.0 kHz, BW = 1.0 Hz)	e_n	–	45	–	–	45	–	nV/(Hz)½
Common-Mode Rejection Ratio (f = 100 Hz)	CM_{rej}	-70	-90	–	-70	-90	–	dB
Open Loop Voltage Gain ($T_A = T_{low}$ to T_{high})	A_{VOL}	4,000	7,000	10,000	3,500	7,000	–	V/V
Power Bandwidth (A_V = 1, R_L = 2.0 kohms, THD ≤ 5%, V_o = 20 Vp-p)	P_{BW}	–	40	–	–	40	–	kHz
Unity Gain Crossover Frequency (open-loop)		–	1.0	–	–	1.0	–	MHz
Phase Margin (open-loop, unity gain)		–	75	–	–	75	–	degrees
Gain Margin		–	18	–	–	18	–	dB
Step Response								
Gain = 100, 30% overshoot,	t_f	–	0.3	–	–	0.3	–	µs
R1 = 4.7 kΩ, R2 = 470 kΩ,	t_{pd}	–	0.1	–	–	0.1	–	µs
R3 = 150 Ω, C1 = 1,000 pF	dV_{out}/dt ②	–	0.167	–	–	0.167	–	V/µs
Gain = 10, 10% overshoot,	t_f	–	1.9	–	–	1.9	–	µs
R1 = 47 kΩ, R2 = 470 kΩ,	t_{pd}	–	0.3	–	–	0.3	–	µs
R3 = 47 Ω, C1 = 0.01 µF	dV_{out}/dt ②	–	0.111	–	–	0.111	–	V/µs
Gain = 1, 5% overshoot,	t_f	–	27	–	–	27	–	µs
R1 = 47 kΩ, R2 = 47 kΩ,	t_{pd}	–	0.25	–	–	0.25	–	µs
R3 = 4.7 Ω, C1 = 0.1 µF	dV_{out}/dt ②	–	0.013	–	–	0.013	–	V/µs
Output Impedance (f = 20 Hz)	Z_{out}	–	1.7	–	–	1.7	–	kohms
Short-Circuit Output Current	I_{SC}	–	±17	–	–	±17	–	mAdc
Output Voltage Swing (R_L = 2.0 kohms)	V_o	±2.5	±2.8	–	±2.3	±2.7	–	Vp
Power Supply Sensitivity								µV/V
V^- = constant, $R_s \leq$ 10 kohms	S+	–	50	–	–	50	–	
V^+ = constant, $R_s \leq$ 10 kohms	S-	–	100	–	–	100	–	
Power Supply Current (Total)	I_D^+	–	8.3	12.5	–	8.3	15	mAdc
	I_D^-	–	8.3	12.5	–	8.3	15	
DC Quiescent Power Dissipation (Total) (V_o = 0)	P_D	–	100	150	–	100	180	mW

MATCHING CHARACTERISTICS

Characteristics	Symbol	MC1535 Min	MC1535 Typ	MC1535 Max	MC1435 Min	MC1435 Typ	MC1435 Max	Unit
Open Loop Voltage Gain	$A_{VOL1}-A_{VOL2}$	–	±1.0	–	–	±1.0	–	dB
Input Bias Current	$I_{b1}-I_{b2}$	–	±0.15	–	–	±0.15	–	µA
Input Offset Current	$I_{io1}-I_{io2}$	–	±0.02	–	–	±0.02	–	µA
Average Temperature Coefficient	$TC_{Iio1}-TC_{Iio2}$	–	±0.1	–	–	±0.1	–	nA/°C
Input Offset Voltage	$V_{io1}-V_{io2}$	–	±0.1	–	–	±0.1	–	mV
Average Temperature Coefficient	$TC_{Vio1}-TC_{Vio2}$	–	±0.5	–	–	±0.5	–	µV/°C
Channel Separation (See Fig. 10) (f = 10 kHz)	$\frac{e_{out\ 1}}{e_{out\ 2}}$	–	-60	–	–	-60	–	dB

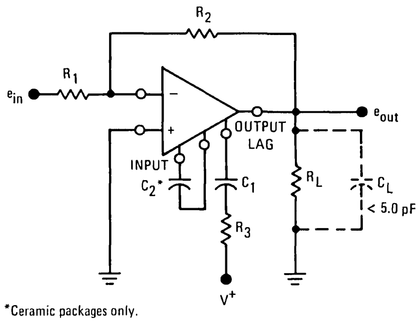
① T_{low}: 0°C for MC1435
-55°C for MC1535
T_{high}: +75°C for MC1435
+125°C for MC1535

② dV_{out}/dt = Slew Rate

TYPICAL OUTPUT CHARACTERISTICS

(V^+ = +6.0 Vdc, V^- = -6.0 Vdc, T_A = +25°C

FIGURE 1 – TEST CIRCUIT



*Ceramic packages only.

FIGURE NO.	CURVE NO.	VOLTAGE GAIN	TEST CONDITIONS $R_1(\Omega)$	$R_2(\Omega)$	C_1(pF)	$R_3(\Omega)$	C_2(pF)	OUTPUT NOISE (mV rms)
2	3	1	47 k	47 k	100,000	4.7	0	0.12
	3A	or 1	47 k	47 k	0	∞	50,000	0.46
3	1	100	4.7 k	470 k	1,000	150	0	1.7
		or 100	4.7 k	470 k	0	∞	510	2.1
	2	10	47 k	470 k	10,000	47	0	1.0
		or 10	47 k	470 k	0	∞	5,000	2.1
	3	1	47 k	47 k	100,000	4.7	0	0.12
		or 1	47 k	47 k	0	∞	50,000	0.46
4	1	A_{VOL}	100	∞	1,000	150	0	8.1
		or A_{VOL}	100	∞	0	∞	510	8.1
	2	A_{VOL}	100	∞	10,000	47	0	5.5
		or A_{VOL}	100	∞	0	∞	5,000	5.5
	3	A_{VOL}	100	∞	100,000	4.7	0	4.4
		or A_{VOL}	100	∞	0	∞	50,000	4.4

FIGURE 2 – LARGE SIGNAL SWING versus FREQUENCY

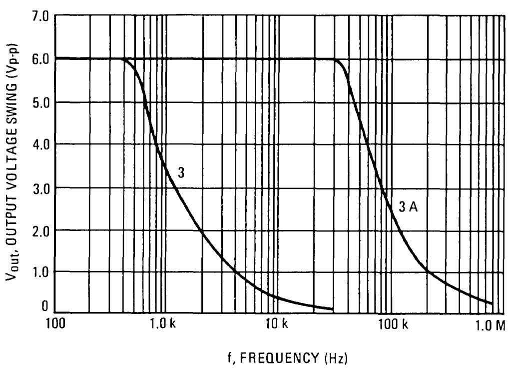


FIGURE 3 – VOLTAGE GAIN versus FREQUENCY

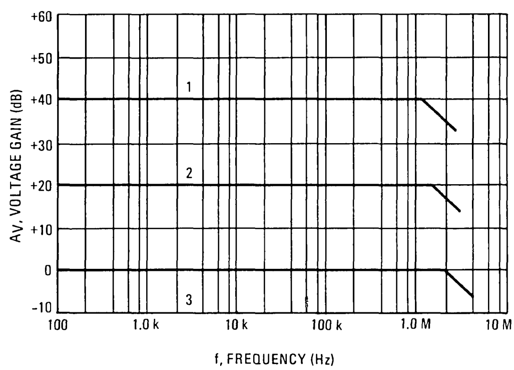


FIGURE 4 – OPEN LOOP VOLTAGE GAIN versus FREQUENCY

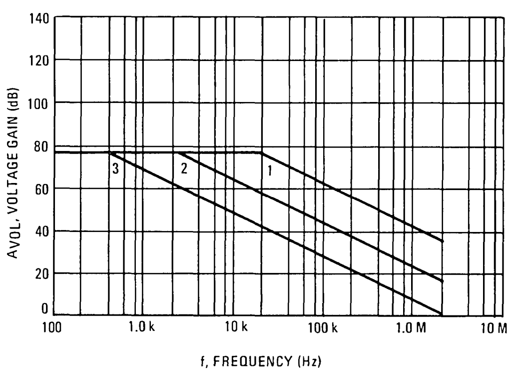


FIGURE 5 – INPUT OFFSET VOLTAGE versus TEMPERATURE

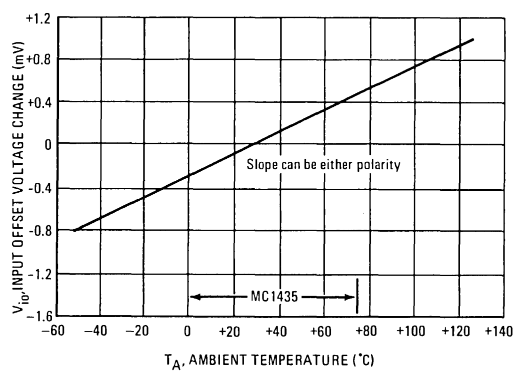


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FIGURE 6 – VOLTAGE GAIN versus POWER SUPPLY VOLTAGE

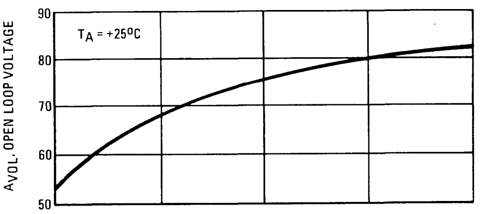


FIGURE 7 – COMMON MODE SWING versus POWER SUPPLY VOLTAGE

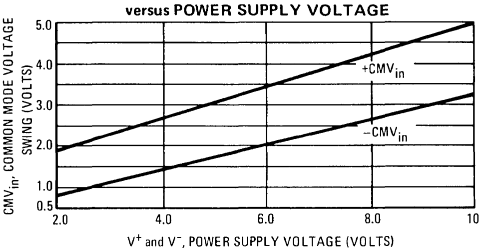


FIGURE 8 – POWER DISSIPATION versus POWER SUPPLY VOLTAGE

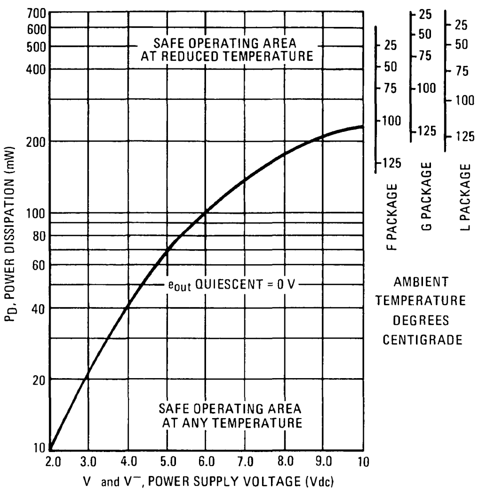
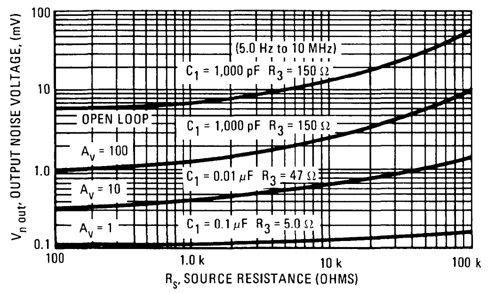


FIGURE 9 – OUTPUT WIDEBAND NOISE VOLTAGE versus SOURCE RESISTANCE



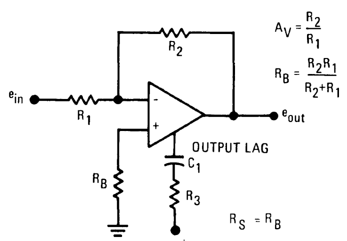
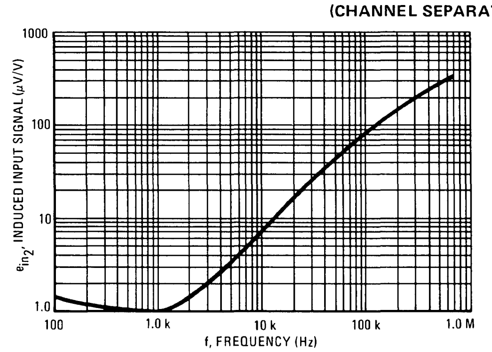
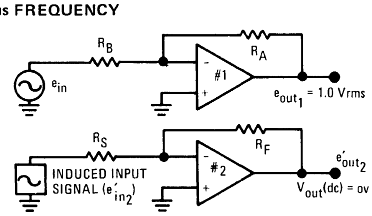


FIGURE 10 – INDUCED INPUT SIGNAL (CHANNEL SEPARATION) versus FREQUENCY





Induced input signal (µV of induced input signal in amplifier #2 per volt of output signal at amplifier #1)

$e'_{out2} = e'_{in2} \left(\frac{R_F}{R_S}\right)$, where e'_{out2} is the component of e_{out_2} due only to lack of perfect separation between the two amplifiers.

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MC1536G
MC1436G
MC1436CG

OPERATIONAL AMPLIFIER

HIGH VOLTAGE, INTERNALLY COMPENSATED MONOLITHIC OPERATIONAL AMPLIFIER

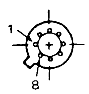
. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

- Maximum Supply Voltage – ±40 Vdc (MC1536G)
- Output Voltage Swing –
  ±30 $V_{pk(min)}$ (V^+ = +36 V, V^- = -36 V) (MC1536G)
  ±22 $V_{pk(min)}$ (V^+ = +28 V, V^- = -28 V)
- Input Bias Current – 20 nA max (MC1536G)
- Input Offset Current – 3.0 nA max (MC1536G)
- Fast Slew Rate – 2.0 V/μs typ
- Internally Compensated
- Offset Voltage Null Capability
- Input Over-Voltage Protection
- A_{VOL} – 500,000 typ
- Characteristics Independent of Power Supply Voltages – (±5.0 Vdc to ±36 Vdc)

OPERATIONAL AMPLIFIER INTEGRATED CIRCUIT

EPITAXIAL PASSIVATED

METAL PACKAGE
CASE 601
TO-99



(bottom view)

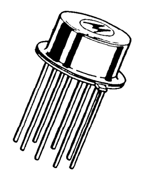


FIGURE 1 – DIFFERENTIAL AMPLIFIER WITH ±20 V COMMON-MODE INPUT VOLTAGE RANGE

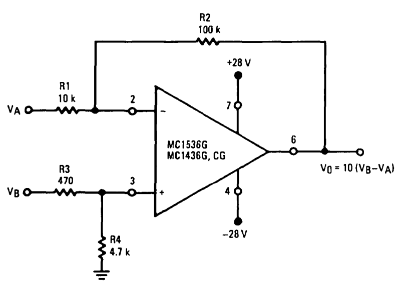


FIGURE 2 – VOLTAGE CONTROLLED CURRENT SOURCE or TRANSCONDUCTANCE AMPLIFIER WITH 0 TO 40 V COMPLIANCE

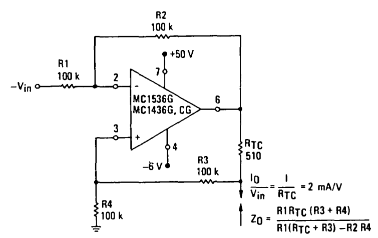


FIGURE 3 – TYPICAL NON-INVERTING X10 VOLTAGE AMPLIFIER

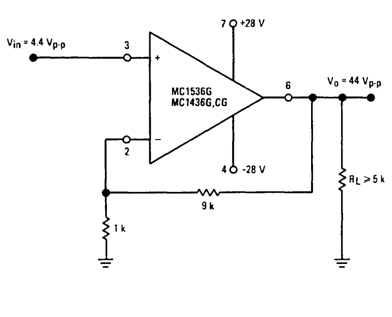
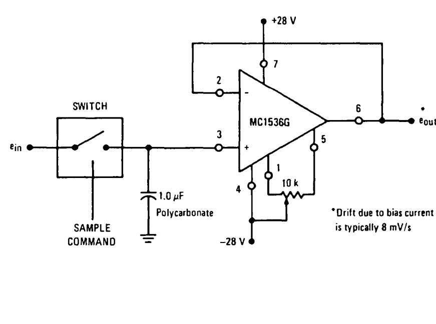


FIGURE 4 – LOW-DRIFT SAMPLE AND HOLD



See Packaging Information Section for outline dimensions.
See current MCC1536/1436 data sheet for standard linear chip information.

MC1536G, MC1436G, MC1436CG (continued)

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	MC1536G	MC1436G	MC1436CG	Unit
Power Supply Voltage	V^+ V^-	+40 -40	+34 -34	+30 -30	Vdc
Differential Input Signal	V_{in}	$\pm(V^+ + \lvert V^-\rvert - 3)$			Volts
Common-Mode Input Swing	CMV_{in}	$+V^+, -(\lvert V^-\rvert - 3)$			Volts
Output Short Circuit Duration ($V^+ = \lvert V^-\rvert$ = 28 Vdc, V_O = 0)	T_{SC}	5.0			s
Power Dissipation (Package Limitation) Derate above T_A = +25°C	P_D	680 4.6			mW mW/°C
Operating Temperature Range	T_A	-55 to +150	0 to +75		°C
Storage Temperature Range	T_{stg}	-65 to +150			°C

ELECTRICAL CHARACTERISTICS (V^+ = +28 Vdc, V^- = -28 Vdc, T_A = +25°C unless otherwise noted)

Characteristics	Symbol	MC1536G Min	MC1536G Typ	MC1536G Max	MC1436G Min	MC1436G Typ	MC1436G Max	MC1436CG Min	MC1436CG Typ	MC1436CG Max	Unit
Input Bias Current	I_b										nAdc
T_A = +25°C		–	8.0	20	–	15	40	–	25	90	
$T_A = T_{low}$ to T_{high} (See Note 1)		–	–	35	–	–	55	–	–	–	
Input Offset Current	$\lvert I_{io}\rvert$										nAdc
T_A = +25°C		–	1.0	3.0	–	5.0	10	–	10	25	
T_A = +25°C to T_{high}		–	–	4.5	–	–	14	–	–	–	
$T_A = T_{low}$ to +25°C		–	–	7.0	–	–	14	–	–	–	
Input Offset Voltage	$\lvert V_{io}\rvert$										mVdc
T_A = +25°C		–	2.0	5.0	–	5.0	10	–	5.0	12	
$T_A = T_{low}$ to T_{high}		–	–	7.0	–	–	14	–	–	–	
Differential Input Impedance (Open-Loop, f ≤ 5.0 Hz)											
Parallel Input Resistance	R_p	–	10	–	–	10	–	–	10	–	Meg ohms
Parallel Input Capacitance	C_p	–	2.0	–	–	2.0	–	–	2.0	–	pF
Common-Mode Input Impedance (f ≤ 5.0 Hz)	$Z_{(in)}$	–	250	–	–	250		–	250	–	Meg ohms
Common-Mode Input Voltage Swing	CMV_{in}	±24	±25	–	±22	±25	–	±18	±20	–	V_{pk}
Equivalent Input Noise Voltage	e_n										nV/(Hz)½
(A_V = 100, R_s = 10 k ohms, f = 1.0 kHz, BW = 1.0 Hz)		–	50	–	–	50	–	–	50	–	
Common-Mode Rejection Ratio (dc)	CM_{rej}	80	110	–	70	110	–	50	90	–	dB
Large Signal dc Open Loop Voltage Gain	A_{VOL}										V/V
(V_O = ± 10 V, R_L = 100 k ohms) T_A = +25°C		100,000	500,000	–	70,000	500,000	–	50,000	500,000	–	
(V_O = ± 10 V, R_L = 100 k ohms) $T_A = T_{low}$ to T_{high}		50,000	–	–	50,000	–	–	–	–	–	
(V_O = ±10 V, R_L = 10 k ohms, T_A = +25°C)		–	200,000	–	–	200,000	–	–	200,000	–	
Power Bandwidth (Voltage Follower)	P_{BW}										kHz
(A_V = 1, R_L = 5.0 k ohms, THD ≤ 5%, V_O = 40 Vp-p)		–	23	–	–	23	–	–	23	–	
Unity Gain Crossover Frequency (open-loop)	f_c	–	1.0	–	–	1.0	–	–	1.0	–	MHz
Phase Margin (open-loop, unity gain)	ϕ	–	50	–	–	50	–	–	50	–	degrees
Gain Margin	A_{GM}	–	18	–	–	18	–	–	18	–	dB
Slew Rate (Unity Gain)	dV_{out}/dt	–	2.0	–	–	2.0	–	–	2.0	–	V/µs
Output Impedance (f ≤ 5.0 Hz)	Z_{out}	–	1.0	–	–	1.0	–	–	1.0	–	k ohms
Short-Circuit Output Current	I_{SC}	–	±17	–	–	±17	–	–	±19	–	mAdc
Output Voltage Swing (R_L = 5.0 k ohms)	V_o										V_{pk}
V^+ = +28 Vdc, V^- = -28 Vdc		±22	±23	–	±20	±22	–	±20	±22	–	
V^+ = +36 Vdc, V^- = -36 Vdc		±30	±32	–	–	–	–	–	–	–	
Power Supply Sensitivity (dc)											µV/V
V^- = constant, R_s ≤ 10 k ohms	S+	–	15	100	–	35	200	–	50	–	
V^+ = constant, R_s ≤ 10 k ohms	S–	–	15	100	–	35	200	–	50	–	
Power Supply Current (See Note 2)	I_D+	–	2.2	4.0	–	2.6	5.0	–	2.6	5.0	mAdc
	I_D-	–	2.2	4.0	–	2.6	5.0	–	2.6	5.0	
DC Quiescent Power Dissipation	P_D										mW
(V_{oi} = 0)		–	124	224	–	146	280	–	146	280	

Note 1: T_{low}: 0°C for MC1436G,CG
-55°C for MC1536G
T_{high}: +75°C for MC1436G,CG
+150°C for MC1536G

Note 2: $V^+ = \lvert V^-\rvert$ = 5.0 Vdc to 36 Vdc for MC1536G
$V^+ = \lvert V^-\rvert$ = 5.0 Vdc to 30 Vdc for MC1436G
$V^+ = \lvert V^-\rvert$ = 5.0 Vdc to 28 Vdc for MC1436CG

FIGURE 5 — POWER BANDWIDTH

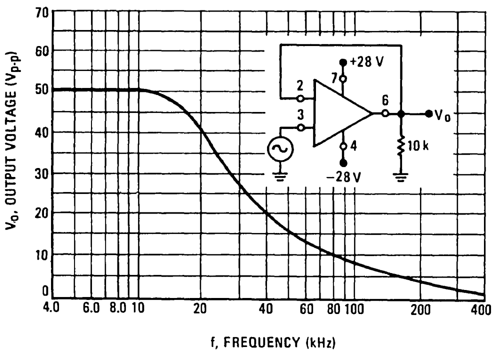


FIGURE 6 — PEAK OUTPUT VOLTAGE SWING versus POWER SUPPLY VOLTAGE

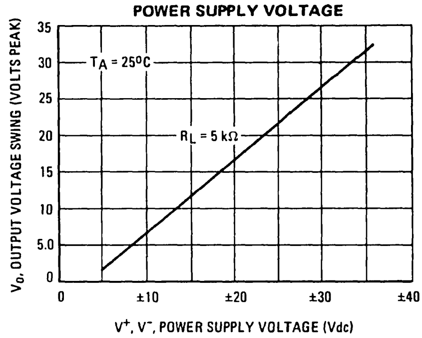


FIGURE 7 — OPEN-LOOP FREQUENCY RESPONSE

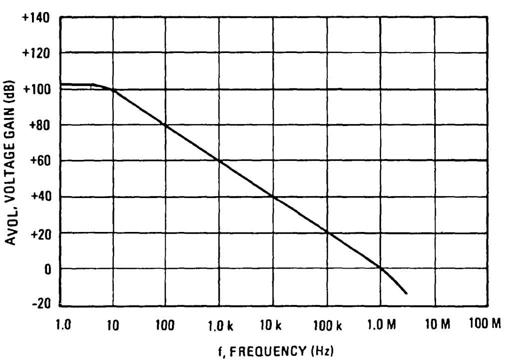


FIGURE 8 — OUTPUT SHORT-CIRCUIT CURRENT versus TEMPERATURE

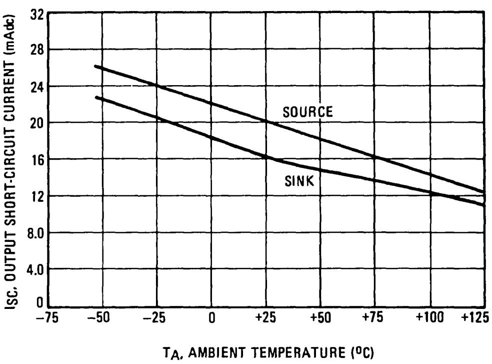


FIGURE 9 — INPUT BIAS CURRENT versus TEMPERATURE

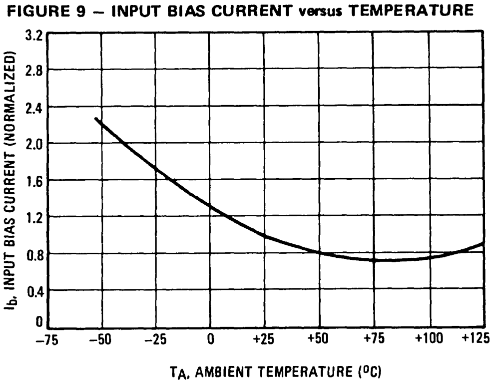


FIGURE 10 – INVERTING FEEDBACK MODEL

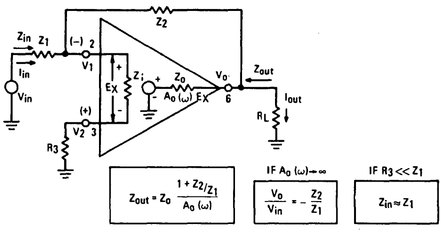


FIGURE 11 – NON-INVERTING FEEDBACK MODEL

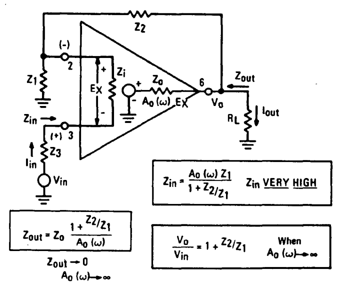


FIGURE 12 – AUDIO AMPLIFIER

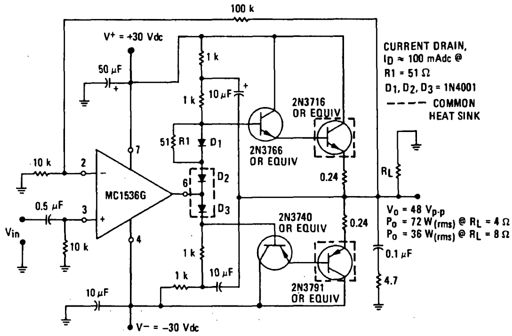


FIGURE 13 – CIRCUIT SCHEMATIC

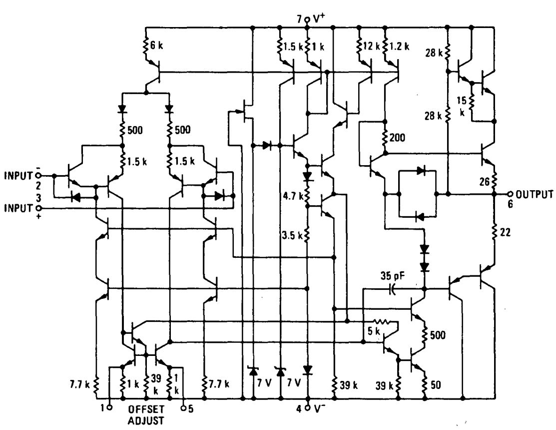
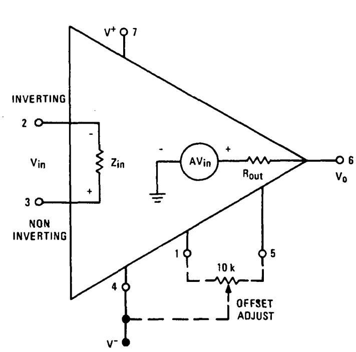


FIGURE 14 – EQUIVALENT CIRCUIT



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MC1537
MC1437

OPERATIONAL AMPLIFIERS

HIGHLY MATCHED MONOLITHIC DUAL OPERATIONAL AMPLIFIERS

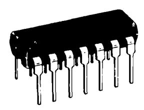
. . . designed for use as summing amplifiers, integrators, or amplifiers with operating characteristics as a function of the external feedback components. Ideal for chopper stabilized applications where extremely high gain is required with excellent stability.

Typical Amplifier Features:

- High-Performance Open Loop Gain Characteristics — A_{VOL} = 45,000 typical
- Low Temperature Drift — ±3 μV/°C
- Large Output Voltage Swing — ±14 V typical @ ±15 V Supply

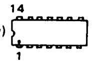
DUAL MC1709
MONOLITHIC SILICON OPERATIONAL AMPLIFIERS INTEGRATED CIRCUIT

P SUFFIX
PLASTIC PACKAGE
CASE 605
TO-116

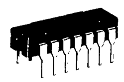


(MC1437 only)

(top view)



L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116



MAXIMUM RATINGS (T_A = +25°C)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+	+18	Vdc
	V^-	-18	Vdc
Differential Input Signal	V_{in}	±5.0	Volts
Common Mode Input Swing	CMV_{in}	$\pm V^+$	Volts
Output Short Circuit Duration	t_S	5.0	s
Power Dissipation (Package Limitation)	P_D		
Ceramic Package		750	mW
Derate above T_A = +25°C		6.0	mW/°C
Plastic Package		625	mW
Derate above T_A = +25°C		5.0	mW/°C
Operating Temperature Range	T_A		°C
MC1537		-55 to +125	
MC1437		0 to +75	
Storage Temperature Range	T_{stg}	-65 to +150	°C

FIGURE 1 — CIRCUIT SCHEMATIC

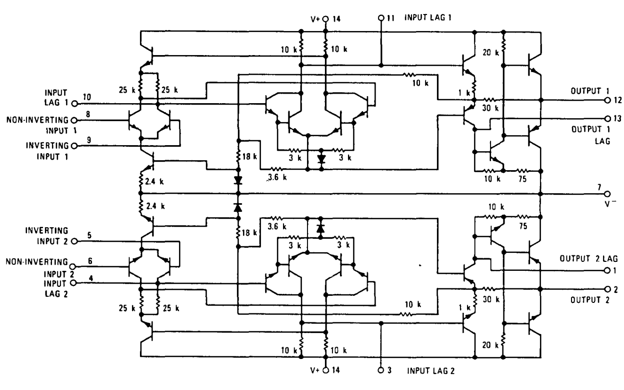
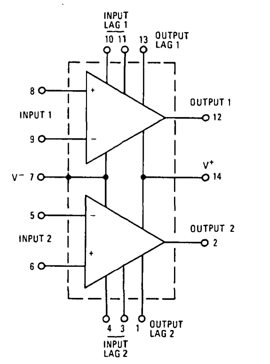


FIGURE 2 — EQUIVALENT CIRCUIT



See Packaging Information Section for outline dimensions.

MC1537, MC1437 (continued)

ELECTRICAL CHARACTERISTICS — Each Amplifier (V^+ = +15 Vdc, V^- = −15 Vdc, T_A = 25°C unless otherwise noted)

Characteristic	Symbol	MC1537 Min	MC1537 Typ	MC1537 Max	MC1437 Min	MC1437 Typ	MC1437 Max	Unit
Open Loop Voltage Gain (R_L = 5.0 kΩ, V_o = ±10 V, T_A = T_{low} ① to T_{high} ②)	A_{VOL}	25,000	45,000	70,000	15,000	45,000	–	–
Output Impedance (f = 20 Hz)	Z_o	–	30	–	–	30	–	Ω
Input Impedance (f = 20 Hz)	Z_{in}	150	400	–	50	150	–	kΩ
Output Voltage Swing	V_o							V_{peak}
(R_L = 10 kΩ)		±12	±14	–	±12	±14	–	
(R_L = 2.0 kΩ)		±10	±13	–	–	–	–	
Input Common-Mode Voltage Swing	CMV_{in}	±8.0	±10	–	±8.0	±10	–	V_{peak}
Common-Mode Rejection Ratio	CM_{rej}	70	100	–	65	100	–	dB
Input Bias Current	I_b							μA
$\left(I_b = \frac{I_1 + I_2}{2}\right)$ (T_A = +25°C)		–	0.2	0.5	–	0.4	1.5	
(T_A = T_{low} ①)		–	0.5	1.5	–	–	2.0	
Input Offset Current	$\lvert I_{io}\rvert$							μA
($I_{io} = I_1 - I_2$)		–	0.05	0.2	–	0.05	0.5	
($I_{io} = I_1 - I_2$, T_A = T_{low} ①)		–	–	0.5	–	–	0.75	
($I_{io} = I_1 - I_2$, T_A = T_{high} ②)		–	–	0.2	–	–	0.75	
Input Offset Voltage	$\lvert V_{io}\rvert$							mV
(T_A = +25°C)		–	1.0	5.0	–	1.0	7.5	
(T_A = T_{low} ① to T_{high} ②)		–	–	6.0	–	–	10	
Step Response								
Gain = 100, 5% overshoot, R_1 = 1 kΩ, R_2 = 100 kΩ, R_3 = 1.5 kΩ, C_1 = 100 pF, C_2 = 3.0 pF	t_f	–	0.8	–	–	0.8	–	μs
	t_{pd}	–	0.38	–	–	0.38	–	μs
	dV_{out}/dt ③	–	12	–	–	12	–	V/μs
Gain = 10, 10% overshoot, R_1 = 1 kΩ, R_2 = 10 kΩ, R_3 = 1.5 kΩ, C_1 = 500 pF, C_2 = 20 pF	t_f	–	0.6	–	–	0.6	–	μs
	t_{pd}	–	0.34	–	–	0.34	–	μs
	dV_{out}/dt ③	–	1.7	–	–	1.7	–	V/μs
Gain = 1, 5% overshoot, R_1 = 10 kΩ, R_2 = 10 kΩ, R_3 = 1.5 kΩ, C_1 = 5000 pF, C_2 = 200 pF	t_f	–	2.2	–	–	2.2	–	μs
	t_{pd}	–	1.3	–	–	1.3	–	μs
	dV_{out}/dt ③	–	0.25	–	–	0.25	–	V/μs
Average Temperature Coefficient of Input Offset Voltage	$\lvert TC_{Vio}\rvert$							μV/°C
(R_S = 50 Ω, T_A = T_{low} ① to T_{high} ②)		–	1.5	–	–	1.5	–	
(R_S ≦ 10 kΩ, T_A = T_{low} ① to T_{high} ②)		–	3.0	–	–	3.0	–	
Average Temperature Coefficient of Input Offset Voltage	$\lvert TC_{Iio}\rvert$							nA/°C
(T_A = T_{low} ① to +25°C)		–	0.7	–	–	0.7	–	
(T_A = +25°C to T_{high} ②)		–	0.7	–	–	0.7	–	
DC Power Dissipation (Total) (Power Supply = ±15 V, V_o = 0)	P_D	–	160	225	–	160	225	mW
Positive Supply Sensitivity (V^- constant)	S^+	–	10	150	–	10	200	μV/V
Negative Supply Sensitivity (V^+ constant)	S^-	–	10	150	–	10	200	μV/V

① T_{low} = 0°C for MC1437
= −55°C for MC1537

② T_{high} = +75°C for MC1437
= +125°C for MC1537

③ dV_{out}/dt = Slew Rate

MATCHING CHARACTERISTICS

Open Loop Voltage Gain	A_{VOL1}-A_{VOL2}	–	±1.0	–	–	±1.0	–	dB
Input Bias Current	I_{b1}-I_{b2}	–	±0.15	–	–	±0.15	–	μA
Input Offset Current	$\lvert I_{io1}\rvert$-$\lvert I_{io2}\rvert$	–	±0.02	–	–	±0.02	–	μA
Average Temperature Coefficient	$\lvert TC_{Iio1}\rvert$-$\lvert TC_{Iio2}\rvert$	–	±0.2	–	–	±0.2	–	nA/°C
Input Offset Voltage	$\lvert V_{io1}\rvert$-$\lvert V_{io2}\rvert$	–	±0.2	–	–	±0.2	–	mV
Average Temperature Coefficient	$\lvert TC_{Vio1}\rvert$-$\lvert TC_{Vio2}\rvert$	–	±0.5	–	–	±0.5	–	μV/°C
Channel Separation (f = 10 kHz)	$\frac{e_{out\ 1}}{e_{out\ 2}}$	–	90	–	–	90	–	dB

6

TYPICAL OUTPUT CHARACTERISTICS

FIGURE 3 – TEST CIRCUIT

$V^+ = +15$ Vdc, $V^- = 15$ Vdc, $T_A = 25^oC$

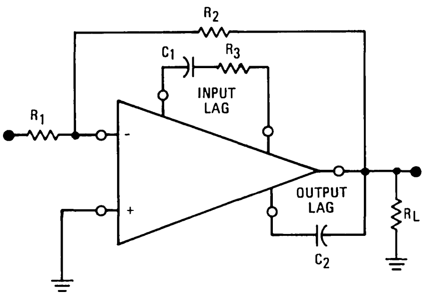


FIGURE NO.	CURVE NO.	VOLTAGE GAIN	TEST CONDITIONS $R_1(\Omega)$	$R_2(\Omega)$	$R_3(\Omega)$	C_1(pF)	C_2(pF)	OUTPUT NOISE (mV(rms))
4	1	1	10 k	10 k	1.5 k	5.0 k	200	0.10
	2	10	10 k	100 k	1.5 k	500	20	0.14
	3	100	10 k	1.0 M	1.5 k	100	3.0	0.7
	4	1000	1.0 k	1.0 M	0	10	3.0	5.2
5	1	1	10 k	10 k	1.5 k	5.0 k	200	0.10
	2	10	10 k	100 k	1.5 k	500	20	0.14
	3	100	10 k	1.0 M	1.5 k	100	3.0	0.7
	4	1000	1.0 k	1.0 M	0	10	3.0	5.2
6	1	A_{VOL}	0	∞	1.5 k	5.0 k	200	5.5
	2	A_{VOL}	0	∞	1.5 k	500	20	10.5
	3	A_{VOL}	0	∞	1.5 k	100	3.0	21.0
	4	A_{VOL}	0	∞	0	10	3.0	39.0
	5	A_{VOL}	0	∞	∞	0	3.0	—

FIGURE 4 – LARGE SIGNAL SWING versus FREQUENCY

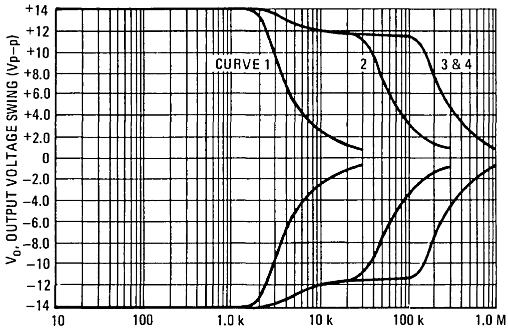


FIGURE 5 – VOLTAGE GAIN versus FREQUENCY

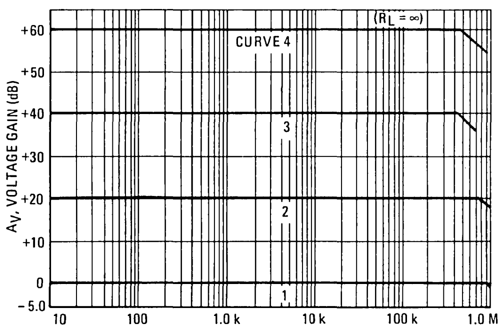


FIGURE 6 – OPEN LOOP VOLTAGE GAIN versus FREQUENCY

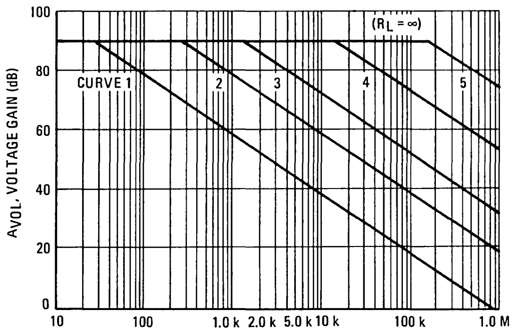
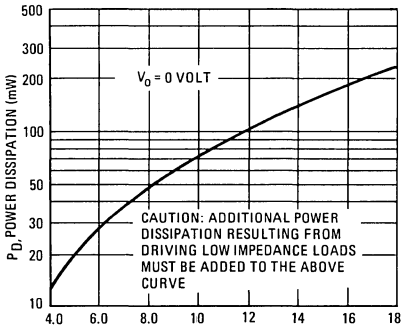


FIGURE 7 – TOTAL POWER DISSIPATION versus POWER SUPPLY VOLTAGE



TYPICAL CHARACTERISTICS (continued)

FIGURE 8 – VOLTAGE GAIN versus POWER SUPPLY VOLTAGE

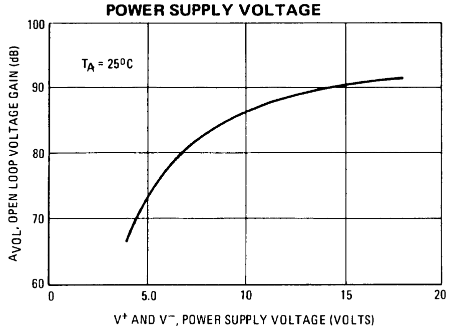


FIGURE 9 – COMMON INPUT SWING versus POWER SUPPLY VOLTAGE

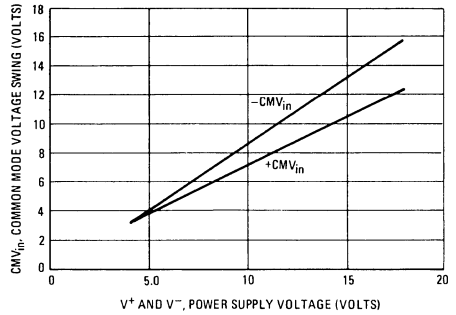


FIGURE 10 – INPUT OFFSET VOLTAGE versus TEMPERATURE

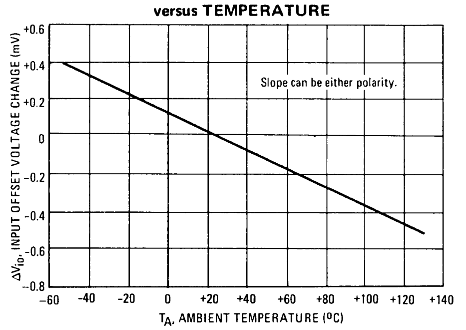


FIGURE 11 – OUTPUT NOISE VOLTAGE versus SOURCE RESISTANCE

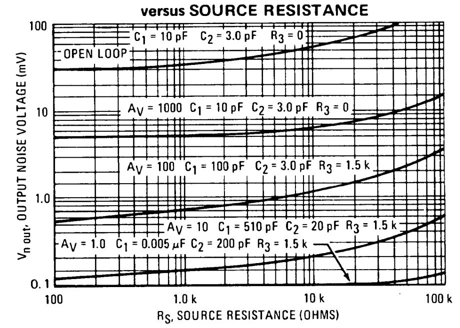
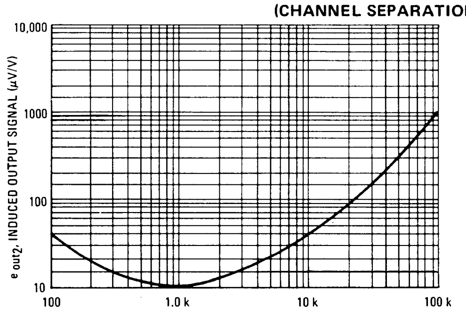
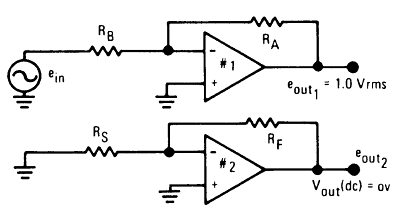


FIGURE 12 – INDUCED OUTPUT SIGNAL (CHANNEL SEPARATION) versus FREQUENCY





Induced output signal (µV of induced output signal in amplifier #2 per volt of output signal at amplifier #1).

6

MC1538R
MC1438R

POWER BOOSTER

MONOLITHIC POWER BOOSTER

The MC1538/MC1438 is designed as a high current gain amplifier (70 dB), with unity voltage gain that can deliver load currents up to ±300 mAdc. This device is ideally suited to follow an operational amplifier (such as MC1556/MC1456) for driving low impedance loads and improving the overall circuit performance.

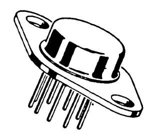
- High Input Impedance – 0.4 Meg-Ohm typ – when driving the MC1538/MC1438, the gain of an operational amplifier will approach the unloaded open-loop gain. Internal power dissipation of the operational amplifier will be independent of output voltage and therefore thermal drift will be reduced.
- Large Power Bandwidth – 1.5 MHz typ – considerably better than present operational amplifiers. Bandwidth and slew rate will be limited by the operational amplifier, not the MC1538/MC1438.
- Low Output Impedance – 10 Ohms typ – allows the MC1538/MC1438 to drive a capacitive load with greatly reduced phase shift compared with an operational amplifier. Output voltage swing capability is much increased when driving small load impedances.
- Adjustable Current Limit – ±5.0 mAdc to ±300 mAdc
- Excellent Power-Supply Rejection – 1.0 mV/V typ
- Current Gain – 3000 typ

POWER BOOSTER

INTEGRATED CIRCUIT FOR OPERATIONAL AMPLIFIERS

EPITAXIAL PASSIVATED

CASE 614

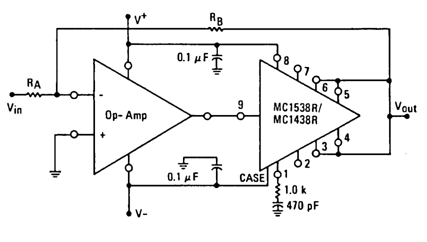


Weight≈6.315 grams

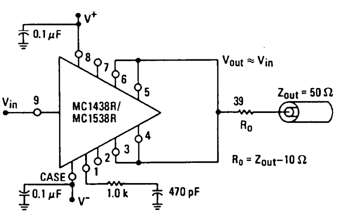
Case connected to V^-

TYPICAL APPLICATIONS

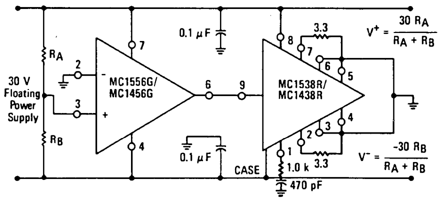
OPERATIONAL AMPLIFIER BOOST CIRCUIT



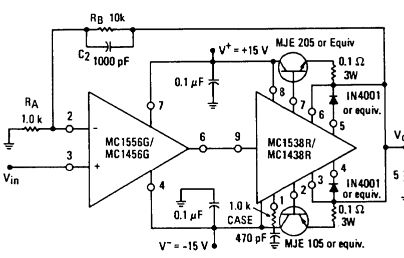
DIGITAL OR ANALOG LINE DRIVER



POWER SUPPLY SPLITTER



SERVO/POWER AMPLIFIER



See Packaging Information Section for outline dimensions.

MAXIMUM RATINGS (T_C = +25°C unless otherwise noted)

Rating	Symbol	MC1538R	MC1438R	Unit
Power Supply Voltage	V^+ V^-	+22 -22	+18 -18	Vdc
Input-Output Voltage Differential	$V_{in} - V_{out}$	-14.5, +44	-14, +36	Vdc
Input Voltage Swing	$\|V_{in}\|$	V^+ or V^-		Vdc
Load Current	I_L	350		mAdc
Power Dissipation and Thermal Characteristics T_A = +25°C Derate above T_A = +25°C Thermal Resistance, Junction to Air T_C = +25°C Derate above T_C = +25°C Thermal Resistance, Junction to Case	 P_D $1/\theta_{JA}$ θ_{JA} P_D $1/\theta_{JC}$ θ_{JC}	 3.0 24 41.6 17.5 140 7.15		 Watts mW/°C °C/W Watts mW/°C °C/W
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150		°C

OPERATING TEMPERATURE RANGE

Ambient Temperature MC1438R MC1538R	T_A	0 to +75 -55 to +125	°C

ELECTRICAL CHARACTERISTICS
(R_L = 300 ohms, T_C = +25°C unless otherwise noted.)

				MC1538R V^+ = +5 V to +20 V, V^- = -5 V to -20 V			MC1438R V^+ = +15 V, V^- = -15 V			
Characteristic (Linear Operation)	**Fig**	**Note**	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Voltage Gain (f = 1.0 kHz)	1	–	A_V	0.9	0.95	1.0	0.85	0.95	1.0	V/V
Current Gain ($A_I = \Delta I_o/\Delta I_{in}$)	1	–	A_I	–	3000	–	–	3000	–	A/A
Output Impedance (f = 1.0 kHz)	1	–	Z_{out}	–	10	–	–	10	–	Ohms
Input Impedance (f = 1.0 kHz)	1	–	Z_{in}	–	400	–	–	400	–	k ohms
Output Voltage Swing	1	3	V_{out}	±12	±13	–	±11	±12	–	Vdc
Input Bias Current	2	–	I_b	–	60	200	–	60	300	µAdc
Output Offset Voltage	2	1	V_{oo}	–	25	150	–	25	200	mVdc
Small Signal Bandwidth (R_L = 300 ohms) (V_{in} = 0 Vdc, v_{in} = 100 mV [rms])	1	–	$BW_{3\,dB}$	–	8.0	–	–	8.0	–	MHz
Power Bandwidth (V_{out} = 20 V_{p-p}, THD = 5%)	1	3	PBW	–	1.5	–	–	1.5	–	MHz
Total Harmonic Distortion (f = 1.0 kHz, V_{out} = 20 V_{p-p})	1	3	THD	–	0.5	–	–	0.5	–	%
Short-Circuit Output Current (R1 = R2 = ∞) (R1 = R2 = 3.3. ohms) Adjustable Range	 3 3 4,5	 2	I_{SC}	 75 – –	 95 300 5.0 to 300	 125 – –	 65 – –	 95 300 5.0 to 300	 140 – –	mAdc
Power Supply Sensitivity (V^- constant) (V^+ constant)	2	–	 S^+ S^-	 – –	 1.0 1.0	 – –	 – –	 1.0 1.0	 – –	mV/V
Power Supply Current (R_L = ∞, V_{in} = 0)	2	–	I_{D^+} or I_{D^-}	4.5	6.0	10	2.5	6.0	15	mAdc
Power Dissipation (R_L = ∞, V_{in} = 0)	2	3	P_D	150	180	300	75	180	450	mW

Note 1. Output offset Voltage is the quiescent dc output voltage with the input grounded.
Note 2. Short-Circuit Current, I_{SC}, is adjustable by varying R1, R2, R3 and R4. The positive current limit is set by R1 or R3, and the negative current limit is set by R2 or R4. See Figures 4 and 5 for curves of short-circuit current versus R1, R2, R3 and R4.
Note 3. V^+ = +15 V, V^- = -15 V.

MC1539
MC1439

OPERATIONAL AMPLIFIERS

MONOLITHIC OPERATIONAL AMPLIFIER

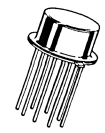
. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components. For detailed information see Motorola Application Note AN-439.

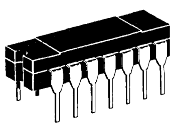
- Low Input Offset Voltage – 3.0 mV max
- Low Input Offset Current – 60 nA max
- Large Power-Bandwidth – 20 $V_{p\text{-}p}$ Output Swing at 20 kHz min
- Output Short-Circuit Protection
- Input Over-Voltage Protection
- Class AB Output for Excellent Linearity
- Slew Rate – 34 V/μs typ

OPERATIONAL AMPLIFIER INTEGRATED CIRCUIT

MONOLITHIC SILICON

G SUFFIX
METAL PACKAGE
CASE 601
TO-99





L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

P2 SUFFIX
PLASTIC PACKAGE
CASE 605
TO-116
(MC1439 only)

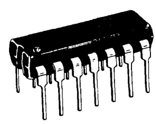
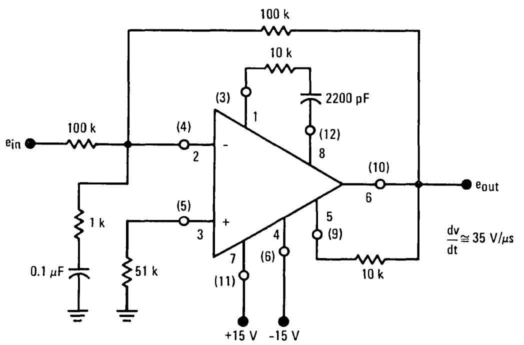


FIGURE 1 – HIGH SLEW RATE INVERTER



Pin numbers adjacent to terminals apply to 8-pin package, numbers in parenthesis apply to 14-pin packages.

FIGURE 2 – OUTPUT NULLING CIRCUIT

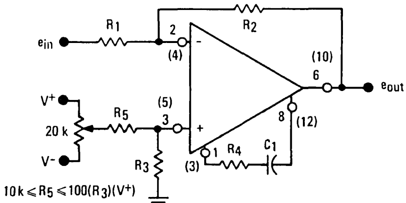
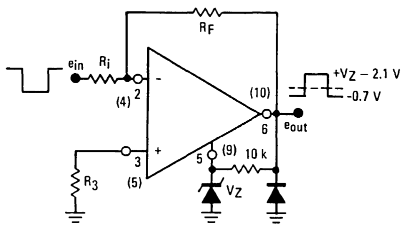


FIGURE 3 – OUTPUT LIMITING CIRCUIT



See Packaging Information Section for outline dimensions.
See current MCC1539/1439 data sheet for standard linear chip information.

ELECTRICAL CHARACTERISTICS (V^+ = +15 Vdc, V^- = −15 Vdc, T_A = +25°C unless otherwise noted)

Characteristic	Symbol	MC1539 Min	MC1539 Typ	MC1539 Max	MC1439 Min	MC1439 Typ	MC1439 Max	Unit
Input Bias Current	I_b							µA
(T_A = +25°C)		–	0.20	0.50	–	0.20	1.0	
(T_A = T_{low} ①)		–	0.23	0.70	–	0.23	1.5	
Input Offset Current	$\lvert I_{io} \rvert$							nA
(T_A = T_{low})		–	–	75	–	–	150	
(T_A = +25°C)		–	20	60	–	20	100	
(T_A = T_{high} ①)		–	–	75	–	–	150	
Input Offset Voltage	$\lvert V_{io} \rvert$							mV
(T_A = +25°C)		–	1.0	3.0	–	2.0	7.5	
(T_A = T_{low}, T_{high})		–	–	4.0	–	–	–	
Average Temperature Coefficient of Input Offset Voltage (T_A = T_{low} to T_{high})	$\lvert TCV_{io} \rvert$							µV/°C
(R_S = 50 Ω)		–	3.0	–	–	3.0	–	
($R_S \leq$ 10 kΩ)		–	5.0	–	–	5.0	–	
Input Impedance (f = 20 Hz)	Z_{in}	150	300	–	100	300	–	kΩ
Input Common-Mode Voltage Swing	CMV_{in}	±11	±12	–	±11	±12	–	V_{pk}
Equivalent Input Noise Voltage (R_S = 10 kΩ, Noise Bandwidth = 1.0 Hz, f = 1.0 kHz)	e_n	–	30	–	–	30	–	nV/(Hz)½
Common-Mode Rejection Ratio (f = 1.0 kHz)	CM_{rej}	80	110	–	80	110	–	dB
Open-Loop Voltage Gain (V_O = ±10 V, R_L = 10 kΩ, R_5 = ∞) (T_A = +25°C to T_{high})	A_{VOL}	50,000	120,000	–	15,000	100,000	–	–
(T_A = T_{low})		25,000	100,000	–	15,000	100,000	–	
Power Bandwidth (A_v = 1, THD $\leq$ 5%, V_O = 20 Vp-p)	PBW							kHz
(R_L = 2.0 kΩ)		–	–	–	10	50	–	
(R_L = 1.0 kΩ)		20	50	–	–	–	–	
Step Response								
Gain = 1000, no overshoot,	t_f	–	130	–	–	130	–	ns
R1 = 1.0 kΩ, R2 = 1.0 MΩ, R3 = 1.0 kΩ,	t_{pd}	–	190	–	–	190	–	ns
R4 = 30 kΩ, R5 = 10 kΩ, C1 = 1000 pF	dV_{out}/dt ②	–	6.0	–	–	6.0	–	V/µs
Gain = 1000, 15% overshoot,	t_f	–	80	–	–	80	–	ns
R1 = 1.0 kΩ, R2 = 1.0 MΩ, R3 = 1.0 kΩ,	t_{pd}	–	100	–	–	100	–	ns
R4 = 0, R5 = 10 kΩ, C1 = 10 pF	dV_{out}/dt	–	14	–	–	14	–	V/µs
Gain = 100, no overshoot,	t_f	–	60	–	–	60	–	ns
R1 = 1.0 kΩ, R2 = 100 kΩ, R3 = 1.0 kΩ,	t_{pd}	–	100	–	–	100	–	ns
R4 = 10 kΩ, R5 = 10 kΩ, C1 = 2200 pF	dV_{out}/dt	–	34	–	–	34	–	V/µs
Gain = 10, 15% overshoot,	t_f	–	120	–	–	120	–	ns
R1 = 1.0 kΩ, R2 = 10 kΩ, R3 = 1.0 kΩ,	t_{pd}	–	80	–	–	80	–	ns
R4 = 1.0 kΩ, R5 = 10 kΩ, C1 = 2200 pF	dV_{out}/dt	–	6.25	–	–	6.25	–	V/µs
Gain = 1, 15% overshoot,	t_f	–	160	–	–	160	–	ns
R1 = 10 kΩ, R2 = 10 kΩ, R3 = 5.0 kΩ,	t_{pd}	–	80	–	–	80	–	ns
R4 = 390 Ω, R5 = 10 kΩ, C1 = 2200 pF	dV_{out}/dt	–	4.2	–	–	4.2	–	V/µs
Output Impedance (f = 20 Hz)	Z_{out}	–	4.0	–	–	4.0	–	kΩ
Output Voltage Swing	V_{out}							V_{pk}
(R_L = 2.0 kΩ, f = 1.0 kHz)		–	–	–	±10	±13	–	
(R_L = 1.0 kΩ, f = 1.0 kHz)		±10	±13	–	–	–	–	
Positive Supply Sensitivity (V^- constant)	S^+	–	50	150	–	50	200	µV/V
Negative Supply Sensitivity (V^+ constant)	S^-	–	50	150	–	50	200	µV/V
Power Supply Current (V_O = 0)	I_{D+}	–	3.0	5.0	–	3.0	6.7	mAdc
	I_{D-}	–	3.0	5.0	–	3.0	6.7	

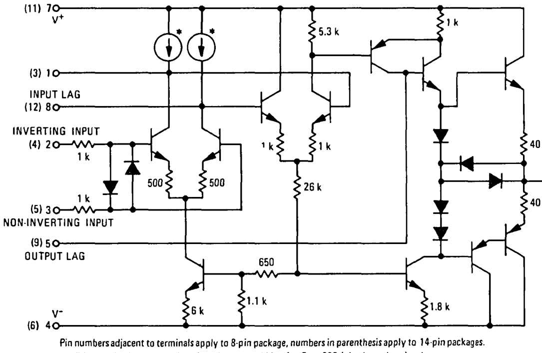
① T_{low} = 0°C for MC1439, −55°C for MC1539; T_{high} = +75°C for MC1439, +125°C for MC1539

② dV_{out}/dt = Slew Rate

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

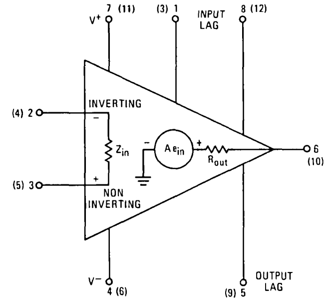
Rating	Symbol	Value	Unit
Power Supply Voltage	V^+ V^-	+18 -18	Vdc Vdc
Differential Input Signal	V_{in}	$\pm[V^+ + \lvert V^- \rvert]$	Vdc
Common Mode Input Swing	CMV_{in}	$+V^+, -\lvert V^- \rvert$	Vdc
Load Current	I_L	15	mA
Output Short Circuit Duration	t_S	Continuous	
Power Dissipation (Package Limitation) Metal Can Derate above T_A = +25°C Ceramic Dual In-Line Package Derate above T_A = +25°C Plastic Dual In-Line Package Derate above T_A = +25°C	P_D	 680 4.6 750 6.0 625 5.0	 mW mW/°C mW mW/°C mW mW/°C
Operating Temperature Range MC1539 MC1439	T_A	-55 to +125 0 to +75	°C
Storage Temperature Range Metal and Ceramic Packages Plastic Package	T_{stg}	 -65 to +150 -55 to +125	°C

FIGURE 4 – CIRCUIT SCHEMATIC



Pin numbers adjacent to terminals apply to 8-pin package, numbers in parenthesis apply to 14-pin packages.
Pin 7 is electrically connected to the substrate and V− for Case 605 (plastic package) only.
*Patent pending.

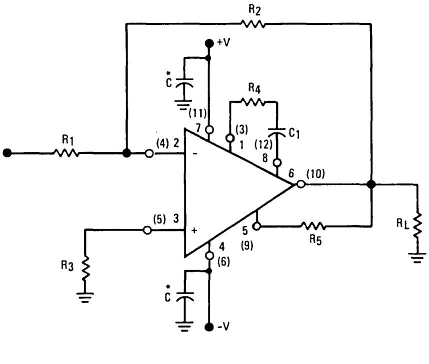
FIGURE 5 – EQUIVALENT CIRCUIT



TYPICAL CHARACTERISTICS

(V^+ = +15 Vdc, V^- = -15 Vdc, T_A = +25°C)

FIGURE 6 – TEST CIRCUIT



TYPICAL OUTPUT CHARACTERISTICS

(V^+ = +15 Vdc, V^- = -15 Vdc, T_A = 25°C)

FIGURE NO.	CURVE NO.	VOLTAGE GAIN	TEST CONDITIONS (FIGURE 6) R_1 (Ω)	R_2 (Ω)	R_3 (Ω)	R_4 (Ω)	R_5 (Ω)	C_1 (pF)
7,8,10,12	1	A_{VOL}	0	∞	0	∞	∞	0
	2	1	10 k	10 k	5.0 k	390	10 k	2200
	3	10	1.0 k	10 k	1.0 k	1.0 k	10 k	2200
	4	100	1.0 k	100 k	1.0 k	10 k	10 k	2200
	5	1000	1.0 k	1.0 M	1.0 k	30 k	10 k	1000
	6	1000	1.0 k	1.0 M	1.0 k	0	10 k	10
13	ALL	1	10 k	10 k	5.0 k	390	10 k	2200
14	ALL	10	1.0 k	10 k	1.0 k	1.0 k	10 k	2200
15	ALL	100	1.0 k	100 k	1.0 k	10 k	10 k	2200
16	ALL	1000	1.0 k	1.0 M	1.0 k	30 k	10 k	2200

TYPICAL CHARACTERISTICS (continued)

(V^+ = +15 Vdc, V^- = -15 Vdc, T_A = 25°C, unless otherwise noted)

FIGURE 7 – LARGE SIGNAL SWING versus FREQUENCY

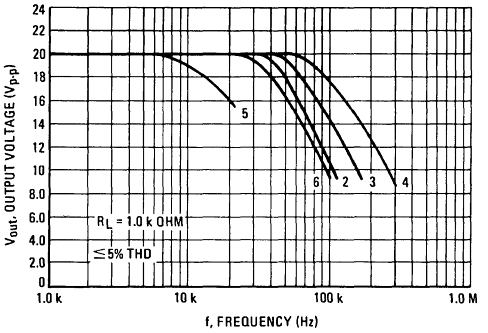


FIGURE 8 – OPEN LOOP VOLTAGE GAIN versus FREQUENCY

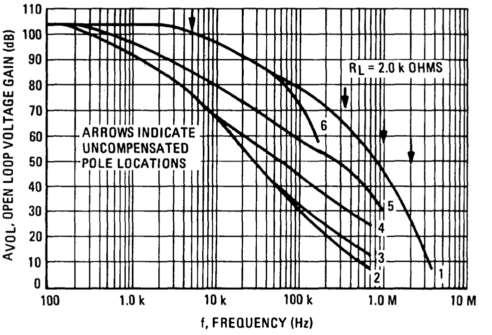


FIGURE 9 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

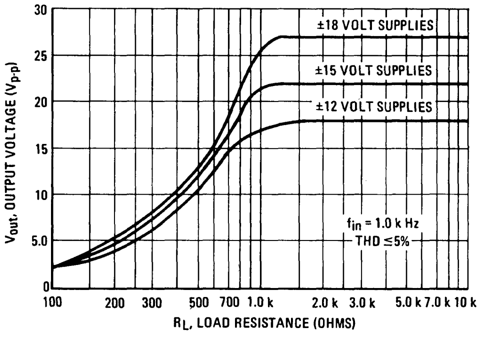


FIGURE 10 – OPEN LOOP PHASE SHIFT versus FREQUENCY

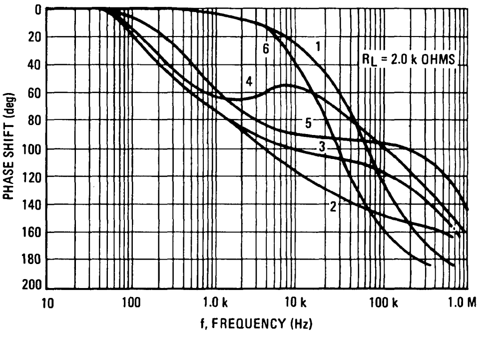


FIGURE 11 – OUTPUT VOLTAGE SWING (to clipping) versus SUPPLY

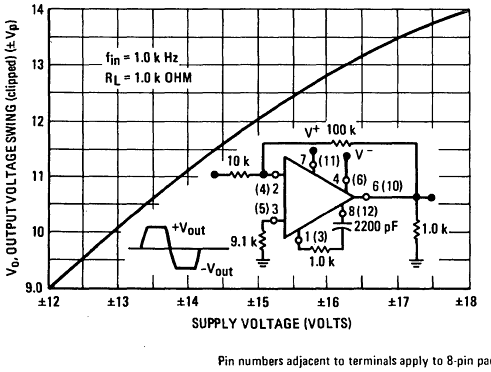
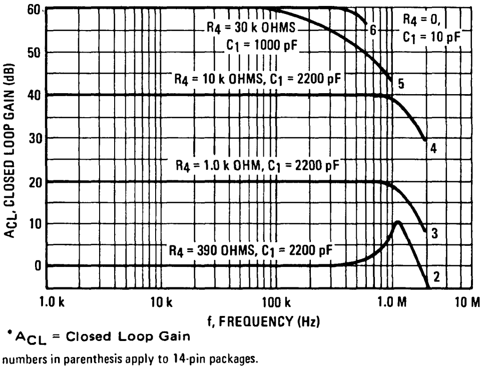


FIGURE 12 – CLOSED LOOP GAIN versus FREQUENCY



*A_{CL} = Closed Loop Gain

Pin numbers adjacent to terminals apply to 8-pin package , numbers in parenthesis apply to 14-pin packages.

FIGURE 13 – A_{CL}* = 1 RESPONSE versus TEMPERATURE

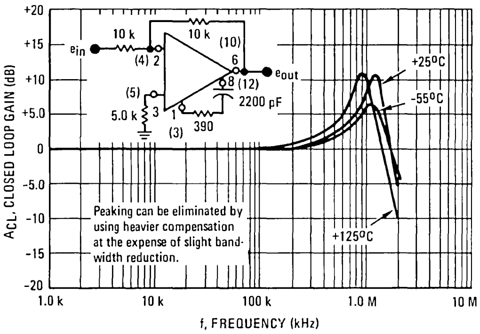


FIGURE 14 – A_{CL} = 10 RESPONSE versus TEMPERATURE

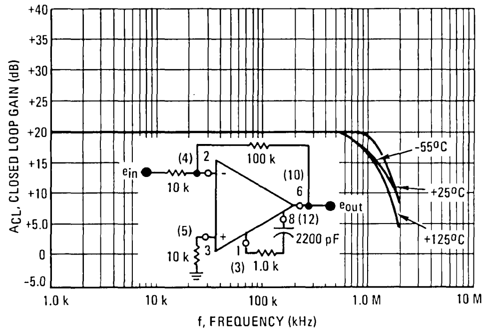


FIGURE 15 – A_{CL} = 100 RESPONSE versus TEMPERATURE

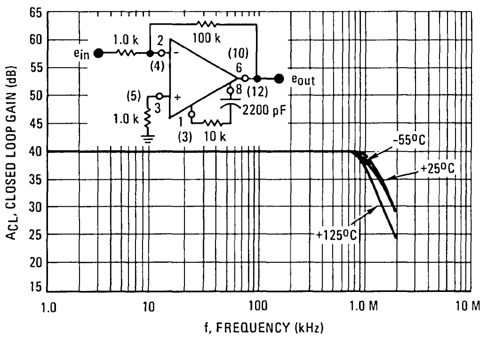


FIGURE 16 – A_{CL} = 1000 RESPONSE versus TEMPERATURE

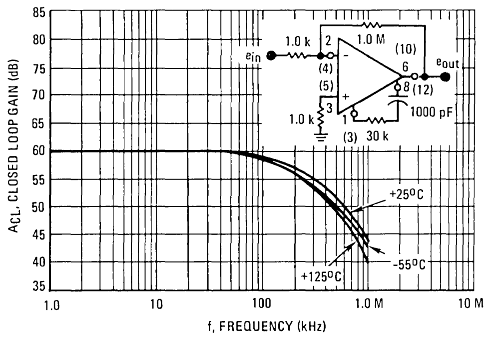


FIGURE 17 – SPECTRAL NOISE DENSITY

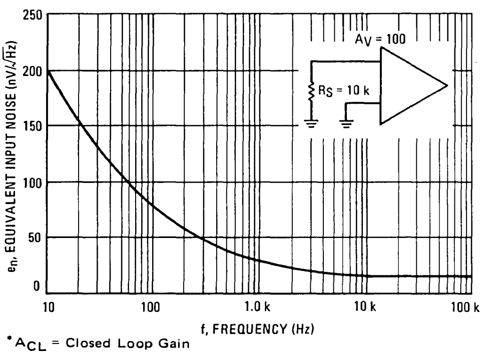
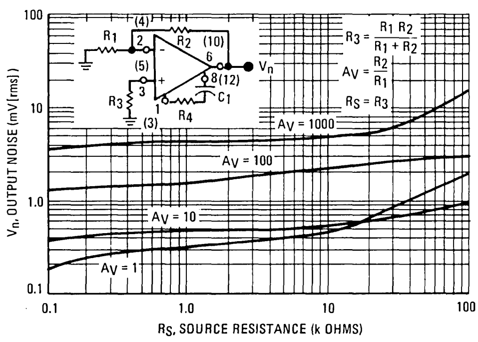


FIGURE 18 – OUTPUT NOISE versus SOURCE RESISTANCE



*A_{CL} = Closed Loop Gain

Pin numbers adjacent to terminals apply to 8-pin package, numbers in parenthesis apply to 14-pin packages.

TYPICAL CHARACTERISTICS (continued)

(V^+ = +15 Vdc, V^- = -15 Vdc, T_A = 25°C, unless otherwise noted)

FIGURE 19 – POWER DISSIPATION versus TEMPERATURE

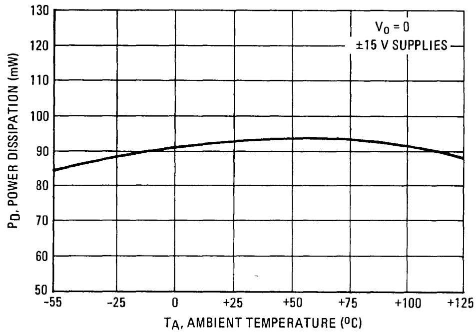


FIGURE 20 – POWER DISSIPATION versus POWER SUPPLY VOLTAGE

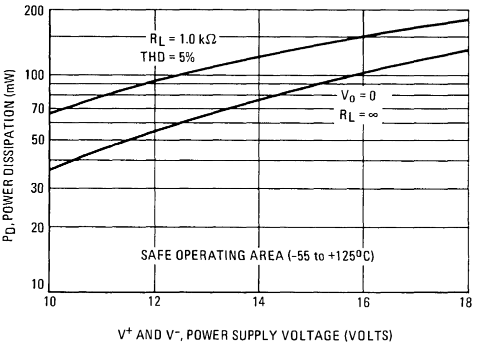


FIGURE 21 – POWER BANDWIDTH (LARGE SIGNAL SWING versus FREQUENCY)

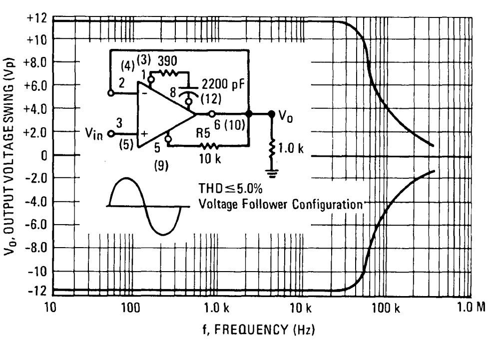


FIGURE 22 – COMMON-MODE INPUT VOLTAGE versus SUPPLY VOLTAGE

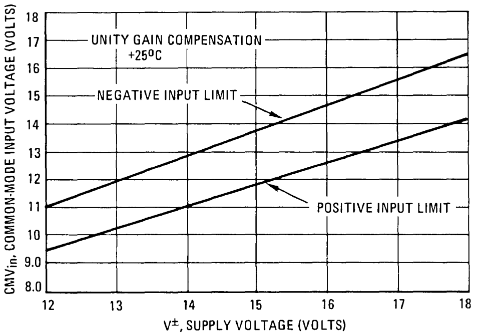


FIGURE 23 – COMMON-MODE REJECTION RATIO versus FREQUENCY

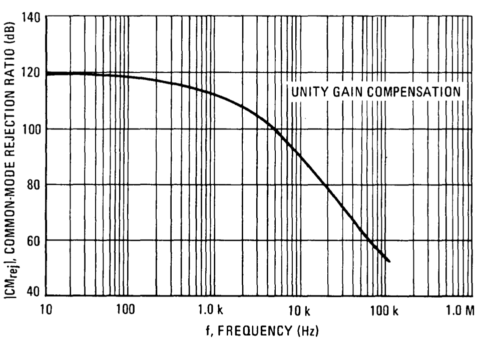
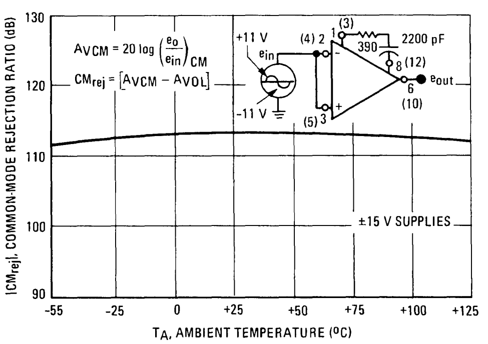
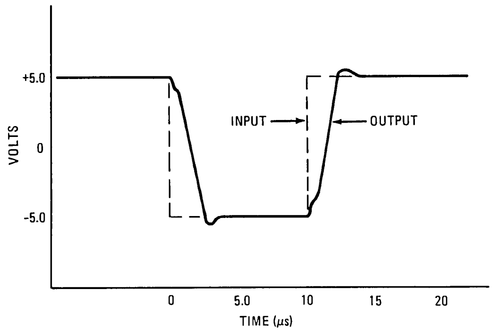


FIGURE 24 – COMMON-MODE REJECTION RATIO versus TEMPERATURE



Pin numbers adjacent to terminals apply to 8-pin package, numbers in parenthesis apply to 14-pin packages.

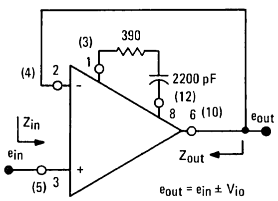
FIGURE 25 – VOLTAGE-FOLLOWER PULSE RESPONSE



TYPICAL APPLICATIONS

Pin numbers adjacent to terminals apply to 8-pin package, numbers in parenthesis apply to 14-pin packages.

FIGURE 26 – VOLTAGE FOLLOWER

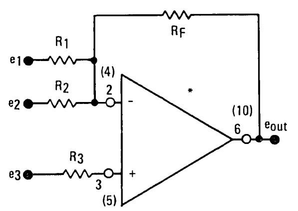


$e_{out} = e_{in} \pm V_{io}$

$Z_{in} > 40$ M OHMS

$$Z_{out\,CL} = Z_{out\,OL}\left[\frac{1 + \frac{R_F}{R_i}}{A_{OL}}\right] = 4\text{ k}\left[\frac{1+0}{10^5}\right] \approx 0.04\text{ OHM}$$

FIGURE 27 – DIFFERENTIAL AMPLIFIER

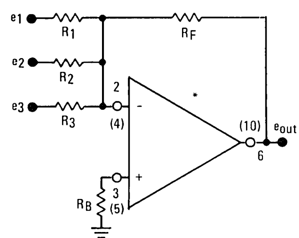


$$e_{out} = -\left[\frac{R_F}{R_1}e1 + \frac{R_F}{R_2}e2\right] + \left[1 + \frac{R_F}{R_3}\right]e3$$

$$\text{For } R_3 = \frac{R_1, R_2}{R_1 + R_2}$$

*Properly Compensated

FIGURE 28 – SUMMING AMPLIFIER

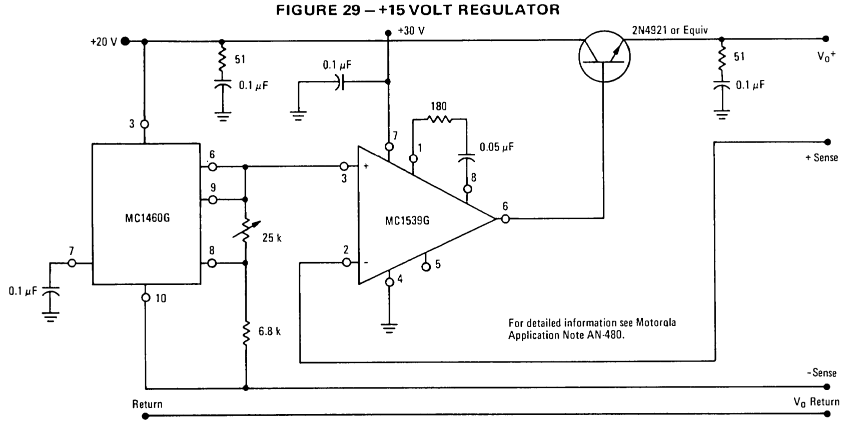


R_B = Parallel Combination of R_1, R_2, R_3, R_F.

$$e_{out} = -\left[\frac{R_F}{R_1}e1 + \frac{R_F}{R_2}e2 + \frac{R_F}{R_3}e3\right]$$

*Properly Compensated

FIGURE 29 – +15 VOLT REGULATOR



TYPICAL APPLICATIONS (continued)

FIGURE 30 – LOAD REGULATION FOR CIRCUIT OF FIGURE 29

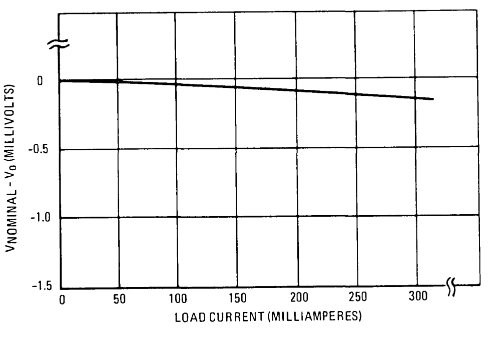
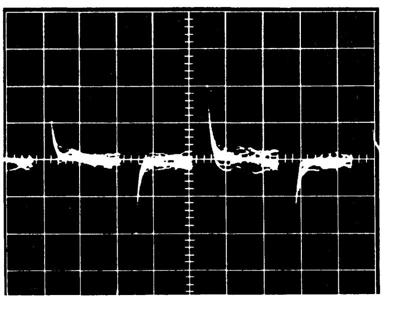


FIGURE 31 – REGULATOR OUTPUT VOLTAGE (under pulsed load condition)



MC1540
MC1440

SENSE AMPLIFIERS

MONOLITHIC SENSE AMPLIFIER

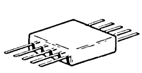
. . . consisting of a wideband differential amplifier, a dc restoration circuit which also incorporates facilities to externally adjust the threshold, and an MDTL output gate which is strobed from saturated logic. It is designed to detect bipolar differential signals derived by a core memory with cycle times as low as 0.5 μs.

- Differential Threshold Characteristics:
  - Adjustable Threshold – 10-25 mV
  - Nominal Threshold – 17 mV @ V_6 = -6 V
  - Input Offset Voltage – 1.0 mV typical
  - Threshold Drift – -10 μV/°C typical
- Fast Response Time – 20 ns typical
- Short Recovery Time:
  - 50 ns max @ e_{in} = 1.8 V Common Mode
  - 50 ns max @ e_{in} = 400 mV Differential Mode

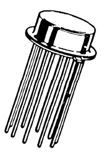
CORE MEMORY SENSE AMPLIFIER INTEGRATED CIRCUIT

SILICON EPITAXIAL PASSIVATED

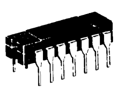
F SUFFIX
CERAMIC PACKAGE
CASE 606
TO-91



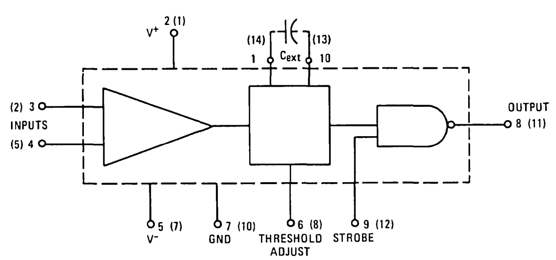
G SUFFIX
METAL PACKAGE
CASE 602B



L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

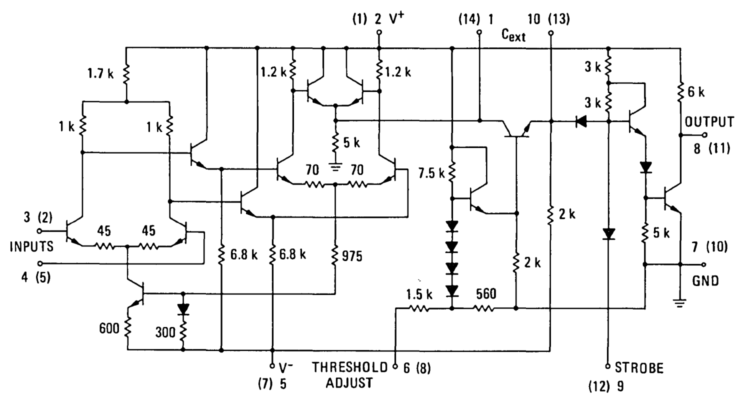


MC1540/MC1440 BLOCK DIAGRAM



Number at end of terminal represents pin number for devices in flat package and metal can. Number in parenthesis represents pin number for dual in-line package.

CIRCUIT SCHEMATIC



Number at end of terminal represents pin number for devices in flat package and metal can.
Number in parenthesis represents pin number for ceramic dual in-line package.

See Packaging Information Section for outline dimensions.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+ V^-	+10 -10	Vdc Vdc
Differential Input Signal	V_{in}	±5.0	Vdc
Common Mode Input Voltage	CMV_{in}	±5.0	Vdc
Load Current	I_L	25	mA
Power Dissipation (Package Limitation) Metal Can Derate above T_A = +25°C Flat Package Derate above T_A = +25°C Ceramic Dual In-Line Package Derate above T_A = +25°C	P_D	 680 4.6 500 3.3 625 5.0	 mW mW/°C mW mW/°C mW mW/°C
Operating Temperature Range MC1440F,G,L MC1540F,G,L	T_A	 0 to +75 -55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS
(V^+ = +6 Vdc ± 1%, V^- = -6 Vdc ± 1%, C_{ext} = 0.01 µF, T_A = +25°C unless otherwise noted)
Pin number references are for devices in flat package and metal can.
See block diagram for dual in-line package pin numbers.

			MC1540			MC1440			
Characteristic	Fig. No.	Symbol	Min	Typ	Max	Min	Typ	Max	Unit
Input Threshold Voltage	1	V_{th}							mV
(V_6 = -6.0 Vdc, T_A = 25°C)			14	17	20	12	17	24	
(V_6 = -6.0 V, T_A = T_{low}*)			12	17	24	10	17	30	
(V_6 = -6.0 V, T_A = T_{high}*)			12	17	22	10	17	30	
Input Offset Voltage	1	V_{io}	–	1.0	5.0	–	1.0	6.0	mV
Input Bias Current	2	I_b							µA
(V_3 = V_4 = 0, T_A = 25°C)			–	7.5	50	–	7.5	75	
(V_3 = V_4 = 0, T_A = T_{low}*)			–	–	100	–	–	100	
Input Offset Current	2	I_{io}	–	2.0	10	–	2.0	15	µA
Output Voltage High (V_3 = V_4 = 0)	3	V_{OH}	5.9	–	–	5.8	–	–	Vdc
Output Voltage Low	3	V_{OL}							mVdc
(V_3 = V_4 = 0, V_{10} = +6.0 Vdc, I_8 = 6.0 mAdc)			–	–	350	–	–	400	
(V_{10} = +6.0 Vdc, I_8 = 6.0 mAdc, T_A = T_{high}*)			–	–	400	–	–	450	
Amplifier Voltage Gain (V_3 = 15 mV peak)	4	A_V	–	85	–	–	85	–	–
Strobe Load Current (V_9 = 0)	–	I_S	–	–	1.2	–	–	1.5	mAdc
Strobe Reverse Current	–	I_R							µAdc
(V_9 = +5.0 Vdc)			–	–	2.0	–	–	5.0	
(V_9 = +6.0 Vdc, T_A = T_{high}*)			–	–	25	–	–	30	
Propagation Delay									ns
Input to Amplifier Output (V_3 = 25 mV pulse, V_9 = +2.0 Vdc)	5	t_{3+10+}	–	10	15	–	10	20	
Input to Gate Output (V_3 = 25 mV pulse, V_9 = +2.0 Vdc)	5	t_{3+8-}	–	20	30	–	20	50	
Strobe to Gate Output (V_3 = V_4 = 0, V_9 = +2.0 V pulse)	6	t_{9+8-}	–	10	15	–	10	30	
Recovery Time									ns
Differential Mode (V_3 = 400 mV pulse)	7	$t_{R(dm)}$	–	20	50	–	20	90	
Common Mode (V_3 = 1.8 V pulse)	8	$t_{R(cm)}$	–	20	50	–	20	60	
Power Dissipation	–	P_D	–	120	180	–	120	250	mW

*T_{low} = -55°C for MC1540 or 0°C for MC1440, T_{high} = +125°C for MC1540 or +75°C for MC1440.

A_V — Amplifier Voltage Gain — the ratio of output voltage at pin 1 to the input voltage at pin 3 or 4

I_b — Input Bias Current — the average input current defined as $(I_3 + I_4)/2$

I_{io} — Input Offset Current — the difference between input current values, $|I_3 - I_4|$

I_R — Strobe Reverse Current — leakage current when the strobe input is high

I_S — Strobe Load Current — amount of current drain from the circuit when the strobe pin is grounded

P_D — Power Dissipation — amount of power dissipated in the unit as defined by $|I_2 \times V^+| + |I_5 \times V^-|$

t_R — Recovery Time — The time that is required for the device to recover from the specified differential and common-mode overload inputs prior to strobe as reference to the 10% point of the trailing edge of an input pulse. The device is considered recovered when the threshold after a differential overload disturbance is within 1.0 mV of the threshold value without the disturbance, or, for common-mode disturbance, when the level at pin 10 is within 100 mV of the quiescent value.

$t_{x\pm y\pm}$ — Propagation Delay — The time that is required for the output pulse at pin y to achieve 50% of its final value or the 1.5 V level referenced to 50% of the input pulse at pin x. (The + and - denote positive and negative-going pulse transition.)

V_{OH} — Output Voltage High — high-level output voltage when the output gate is turned off

V_{OL} — Output Voltage Low — low-level output voltage when the output gate is turned on

V_{th} — Input Threshold — input pulse amplitude that causes the output to begin saturation

V_{io} — Input Offset Voltage — the difference in V_{th} at each input

FIGURE 1 — INPUT THRESHOLD AT OUTPUT VOLTAGE SWING FROM V_{OL} TO V_{OH}

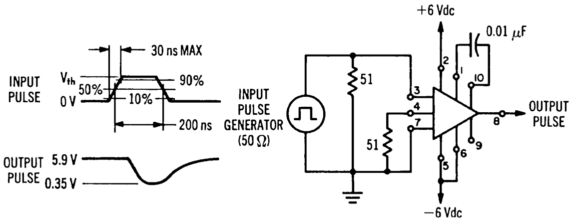


FIGURE 2 — INPUT BIAS CURRENT TEST CIRCUIT

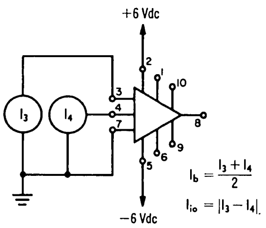


FIGURE 3 — OUTPUT VOLTAGE LEVELS

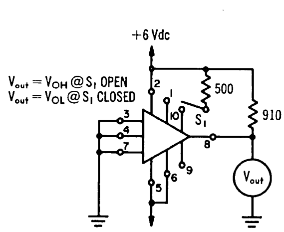


FIGURE 4 — AMPLIFIER VOLTAGE GAIN

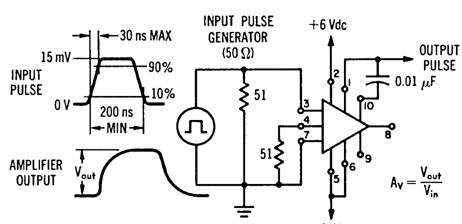


FIGURE 5 — PROPAGATION DELAY (STROBE HIGH)

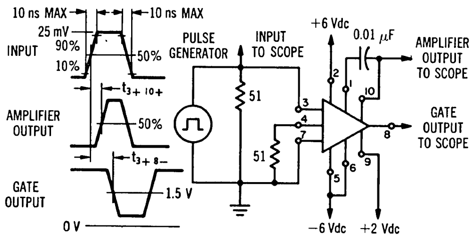


FIGURE 6 — PROPAGATION DELAY (STROBE INPUT)

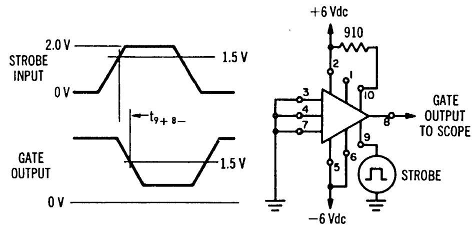


FIGURE 7 – DIFFERENTIAL MODE RECOVERY TIME TEST CIRCUIT

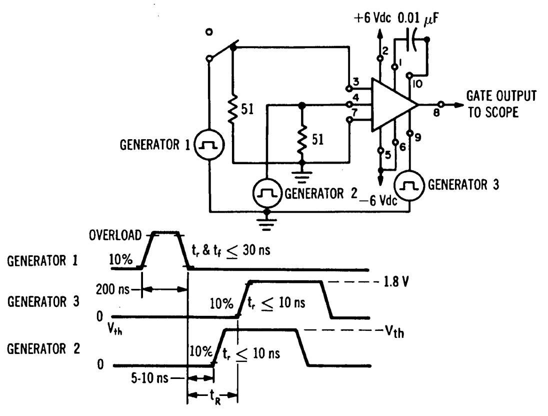
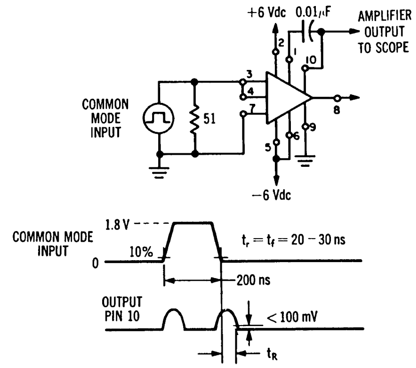


FIGURE 8 – COMMON MODE RECOVERY TIME TEST CIRCUIT



NOTE: The output shown is representative of that obtained. However, the two pulse amplitudes may not be equal or even present.

Pin numbers shown for devices in flat package and metal can. See block diagram for dual in-line package pin numbers.

FIGURE 9 – TYPICAL TRANSFER CHARACTERISTICS

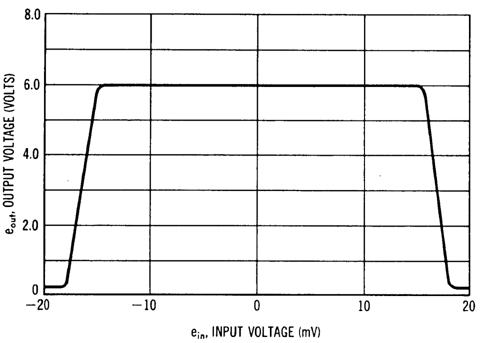


FIGURE 10 – TYPICAL THRESHOLD versus TEMPERATURE

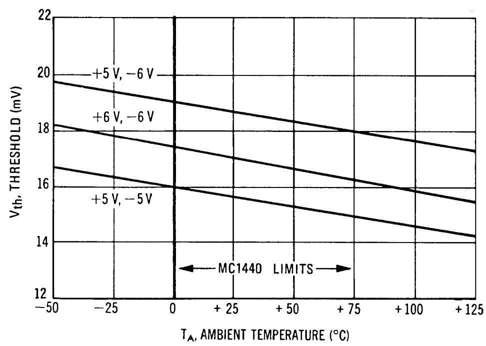


FIGURE 11 – TYPICAL THRESHOLD versus POWER SUPPLIES
T_A = +25°C (Threshold Adjust Attached to V^-)

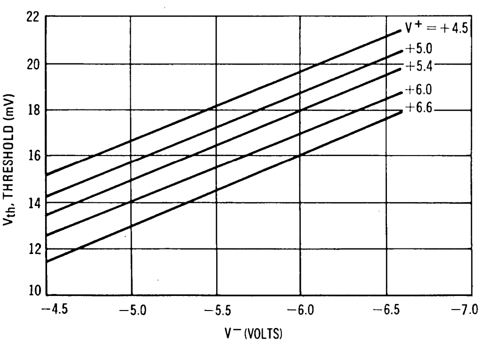
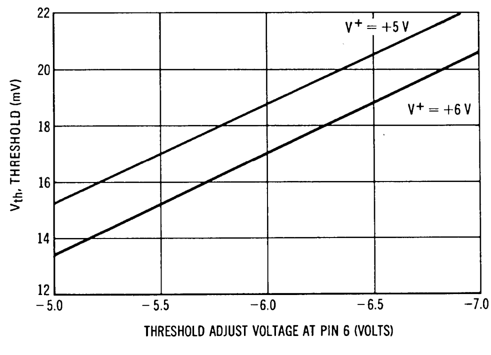


FIGURE 12 – TYPICAL THRESHOLD versus THRESHOLD VOLTAGE ADJUST FOR V^- = 6.0V



For a more detailed discussion regarding application of sense amplifiers, see Motorola Application Note AN-245, "The MC1540 – An Integrated Core Memory Sense Amplifier."

6

MC1541
MC1441

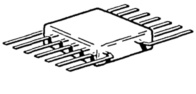
SENSE AMPLIFIERS

Dual-channel gated sense amplifier with separate wideband differential input amplifiers. Either input can be gated on from saturated logic levels. The sense amplifier features adjustable threshold, saturated logic output levels, and a strobe input that accommodates saturated logic levels. Designed to detect bipolar signals from either of two sense lines. Operates with core memory cycle times less than 0.5 μs.

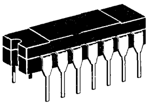
Typical Amplifier Features:

- Nominal Threshold — 17 mV
- Input Offset Voltage — 1.0 mV typical
- Propagation Delay
  - Input to Gate-Output — 20 ns
  - Input to Amplifier-Output — 10 ns
  - Gate Response Time — 15 ns
  - Strobe Response Time — 15 ns
- Common Mode Input Range — 1.5 Volts
- Differential Mode Input Range
  - With Gate On — 600 mV
  - With Gate Off — 1.5 Volts
- Power Dissipation — 140 mW typical

See Packaging Information Section for outline dimensions.



F SUFFIX
CERAMIC PACKAGE
CASE 607
TO-86



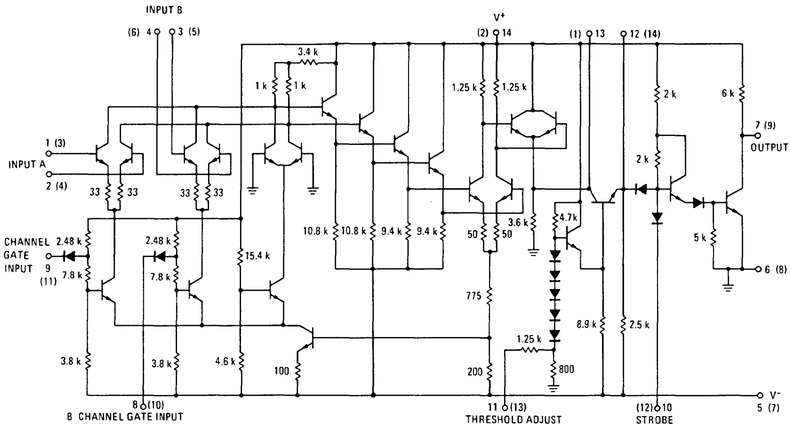
L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

6

MAXIMUM RATINGS

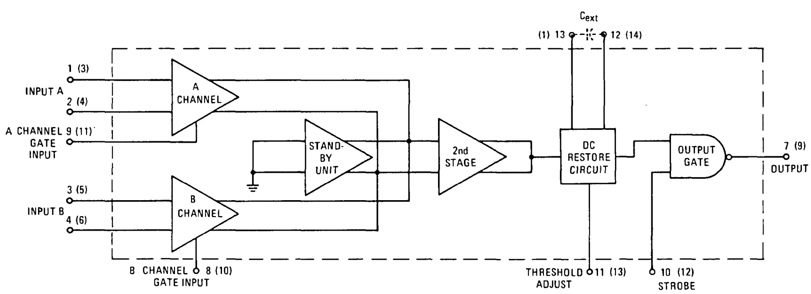
Rating	Symbol	Value	Unit
Power Supply Voltage	V^+ V^-	+10 -10	Vdc Vdc
Differential Input Signal	V_{in}	±5	Vdc
Common Mode Input Voltage	CMV_{in}	±5	Vdc
Load Current	I_L	25	mA
Power Dissipation (Package Limitation) Flat Package Derate above 25°C Ceramic Dual In-Line Package Derate above 25°C	P_D	 500 3.3 600 4.8	 mW mW/°C mW mW/°C
Operating Temperature Range MC1541F, MC1541L MC1441F, MC1441L,	T_A	 -55 to +125 0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

CIRCUIT SCHEMATIC



Number at terminal end denotes pin number for flat (F) package.
Number in parenthesis denotes pin number for dual in-line ceramic (L) package

LOGIC DIAGRAM



Number at terminal end denotes pin number for flat package. Number in parenthesis denotes pin number for dual in-line package.

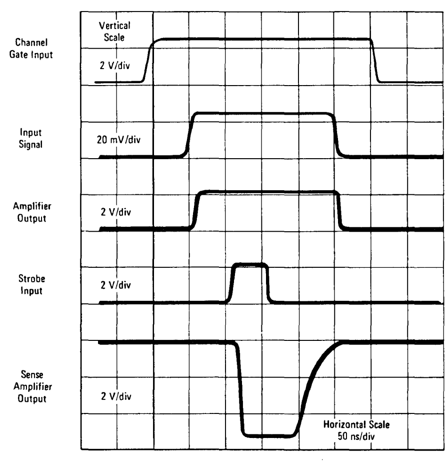


FIGURE 1 – TYPICAL OPERATION

ELECTRICAL CHARACTERISTICS

(V^+ = +5.0 Vdc ± 1%, V^- = 5.0 Vdc ± 1%, $V_{th(pin\ 11)}$ = -5.0 Vdc ± 1%, C_{ext} = 0.01 µF, T_A = 25°C unless otherwise noted)
(T_{low} = -55°C for MC1541 or 0°C for MC1441, T_{high} = +125°C for MC1541 or +75°C for MC1441. Pin numbers referenced in table denote flat package; to ascertain corresponding pin number for dual in-line package refer to the equivalent circuit.)

Characteristic	Fig. No.	Symbol	Min	Typ	Max	Unit
Input Threshold Voltage	8	V_{th}				mV
(T_A = +25°C)			14	17	20	
($T_{low} \leq T_A \leq T_{high}$) MC1441			13	-	21	
MC1541			12	17	22	
Input Offset Voltage	8	V_{io}	-	1.0	6.0	mV
Input Bias Current	9	I_b				µA
($V_1 = V_2 = V_3 = V_4 = 0$)			-	5.0	25	
($V_1 = V_2 = V_3 = V_4 = 0$, $T_A = T_{low}$)			-	-	50	
Input Offset Current	9	I_{io}	-	1.0	2.0	µA
Output Voltage High ($V_1 = V_2 = V_3 = V_4 = 0$, I_{OH} = 200 µA)		V_{OH}	3.0	-	-	Vdc
Output Voltage Low	10	V_{OL}				mVdc
($V_1 = V_2 = V_3 = V_4 = 0$, V_{12} = +5.0 Vdc, I_7 = 10 mAdc)			-	-	350	
(V_{12} = +5.0 Vdc, I_7 = 10 mAdc, $T_A = +T_{high}$)			-	-	400	
Strobe Load Current (V_{10} = 0)		I_S	-	-	1.5	mAdc
Strobe Reverse Current		I_{SR}				µAdc
(V_{10} = +5.0 Vdc)			-	-	2.0	
(V_{10} = +5.0 Vdc, $T_A = T_{high}$)			-	-	25	
Input Gate Voltage Low ($V_1 = V_3$ = 25 mVdc, $V_2 = V_4 = 0$)	11	V_{GL}	-	0.7	-	Vdc
Input Gate Voltage High ($V_1 = V_3$ = 25 mVdc, $V_2 = V_4 = 0$)	11	V_{GH}	-	1.6	-	Vdc
Input Gate Load Current (V_8 or V_9 = 0)		I_G	-	-	2.5	mAdc
Input Gate Reverse Current (V_8 or V_9 = 5.0 Vdc)		I_{GR}				µAdc
(T_A = 25°C)			-	-	2.0	
($T_A = T_{high}$)			-	-	25	
Common Mode Range	13	V_{CM}				Vdc
Input Gate High			-	±1.5	-	
Input Gate Low			-	±1.5	-	
Differential Mode Range	14					
Input Gate High		V_{DH}	-	±600	-	mV
Input Gate Low		V_{DL}	-	±1.5	-	Vdc
Power Dissipation		P_D	-	140	180	mW

SWITCHING CHARACTERISTICS

Characteristic	Fig. No.	Symbol	Min	Typ	Max	Unit
Propagation Delay						ns
Input to Amplifier Output (V_1 = 25 mV pulse, V_{10} = +2.0 Vdc)	8	t_{IA}	-	10	15	
Input to Output (V_1 = 25 mV pulse, V_{10} = +2.0 Vdc)	8	t_{IO}	-	20	30	
Strobe to Output ($V_1 = V_2 = V_3 = V_4 = 0$, V_{10} = +2.0 V pulse)	12	t_{SO}	-	15	20	
Gate Input to Amplifier Input (V_1 = 25 mV pulse, V_9 = 2.0 V pulse)	11	t_{GI}	-	10	15	
Gate Input to Amplifier Output (V_1 = 25 mVdc, V_9 = 2.0 V pulse)	11	t_{GA}	-	30	35	
Recovery Time						ns
Differential Mode	14	t_{DR}				
Input Gate High } V_1 or V_3 = 400 mV pulse			-	30	-	
Input Gate Low }			-	0	-	
Common Mode	13	t_{CMR}				
Input Gate High } V_1 or V_3 = 1.5 V pulse			-	15	30	
Input Gate Low }			-	15	30	

FIGURE 2 – TYPICAL INPUT THRESHOLD versus TEMPERATURE

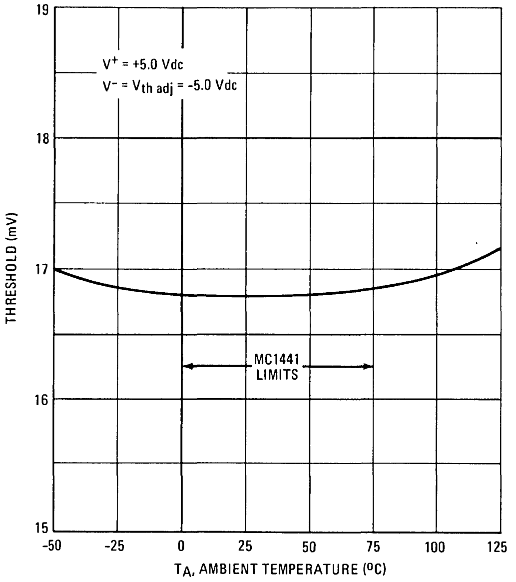


FIGURE 3 – TYPICAL THRESHOLD versus THRESHOLD VOLTAGE ADJUST

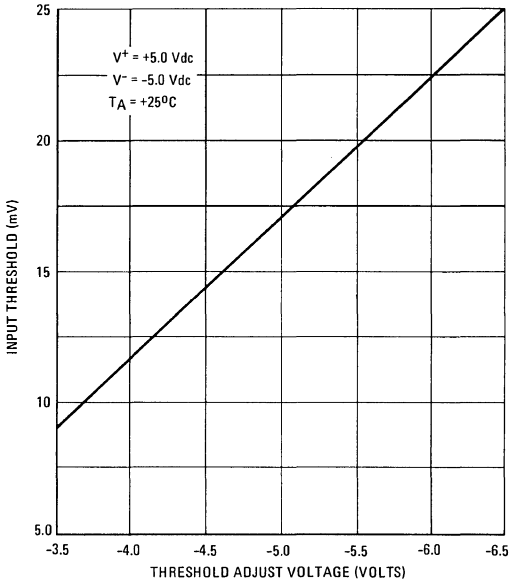


FIGURE 4 – TYPICAL INPUT THRESHOLD versus V-

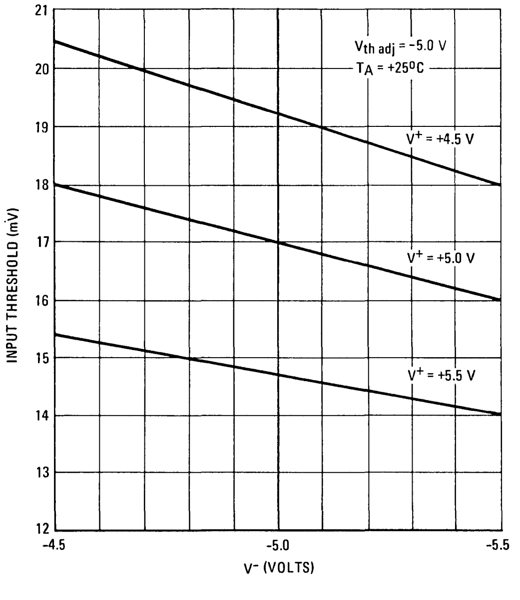


FIGURE 5 – TYPICAL INPUT THRESHOLD versus INPUT PULSE WIDTH

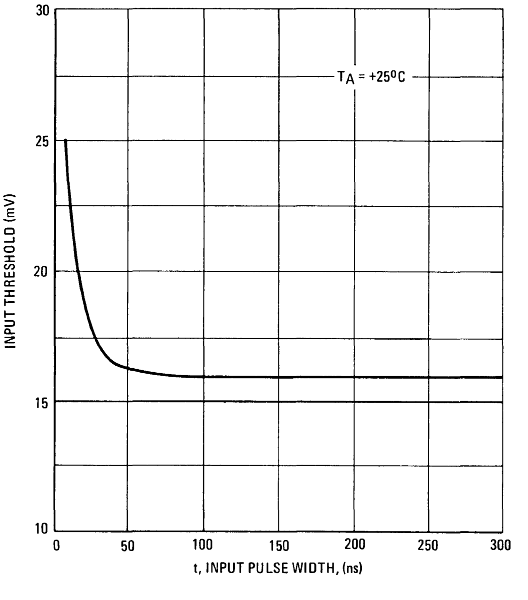


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FIGURE 6 – INPUT-OUTPUT TRANSFER CHARACTERISTICS

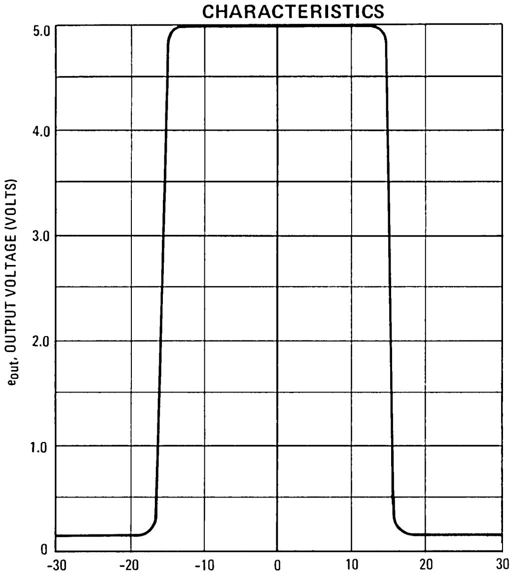


FIGURE 7 – CHANNEL GATE INPUT-AMPLIFIER OUTPUT TRANSFER CHARACTERISTICS

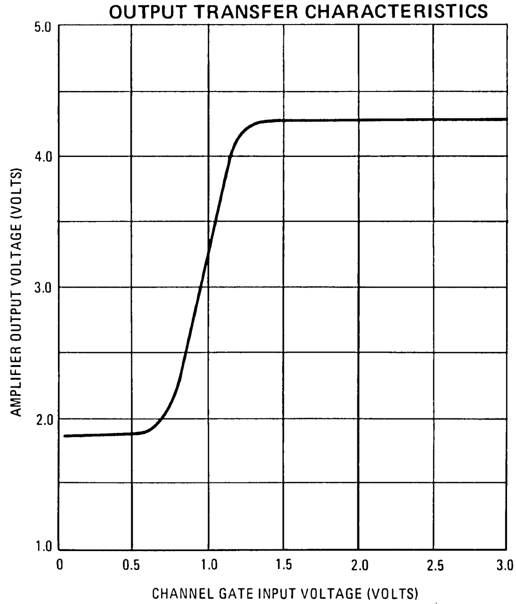
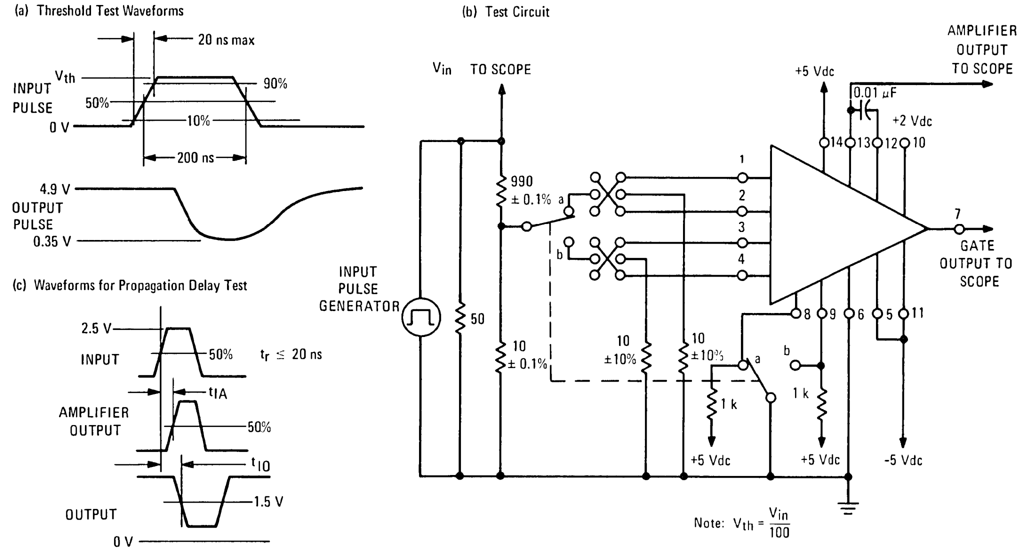
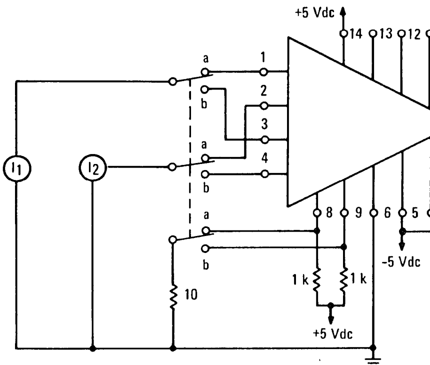


FIGURE 8 – INPUT THRESHOLD FOR OUTPUT VOLTAGE SWING FROM V_{OH} TO V_{OL} PROPAGATION DELAY FROM INPUT TO OUTPUT



Number at terminal end denotes the pin number for flat package only; to ascertain the corresponding pin number for the dual in line packages refer to the circuit schematic on the second page.

FIGURE 9 – INPUT BIAS CURRENT TEST CIRCUIT



$\frac{I_1 + I_2}{2} = I_b$ for "A" channel when switch is in "a" position

" $= I_b$ for "B" channel when switch is in "b" position

$|I_1 - I_2| = I_{io}$

FIGURE 10 – OUTPUT VOLTAGE LEVELS

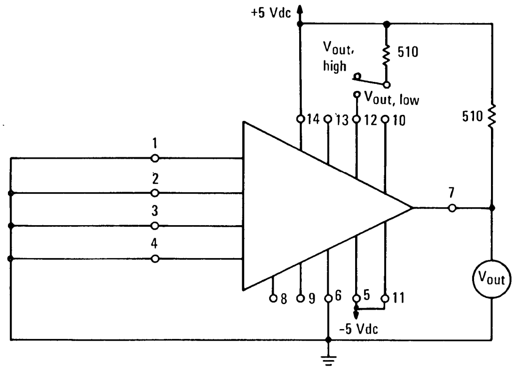
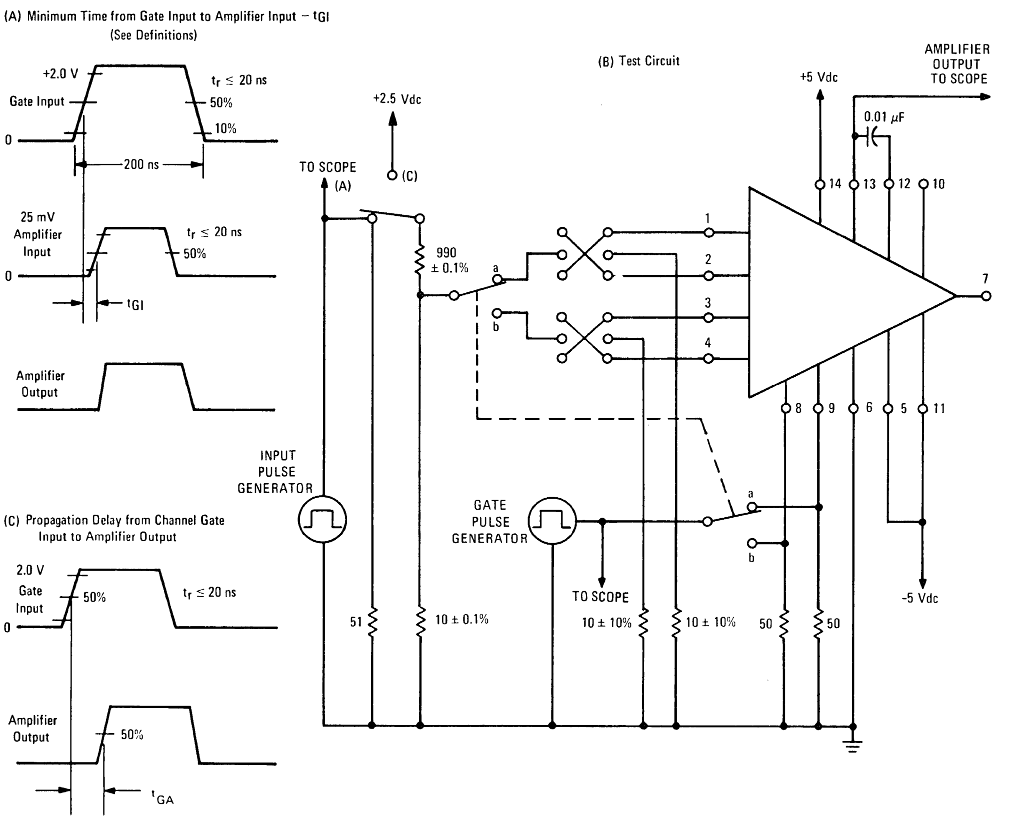


FIGURE 11 – MINIMUM TIME FROM CHANNEL GATE INPUT TO AMPLIFIER INPUT PROPAGATION DELAY FROM CHANNEL GATE INPUT TO AMPLIFIER OUTPUT



(Pin numbers shown on this page denote the pin numbers for the flat package only; to ascertain the corresponding pin numbers for the dual in-line package, refer to the circuit schematic on the second page.)

FIGURE 12 – PROPAGATION DELAY FROM STROBE INPUT TO OUTPUT

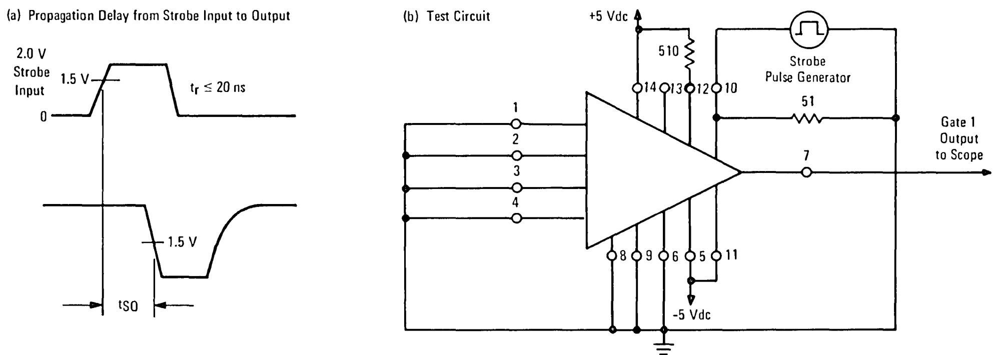


FIGURE 13 – COMMON-MODE RECOVERY AND COMMON-MODE RANGE

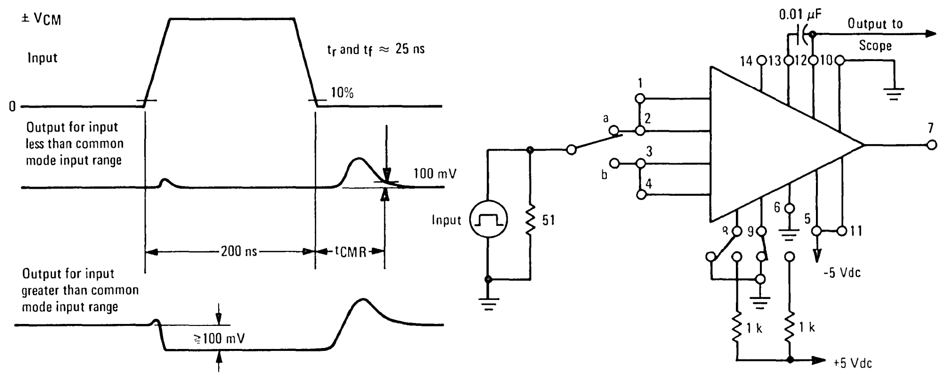
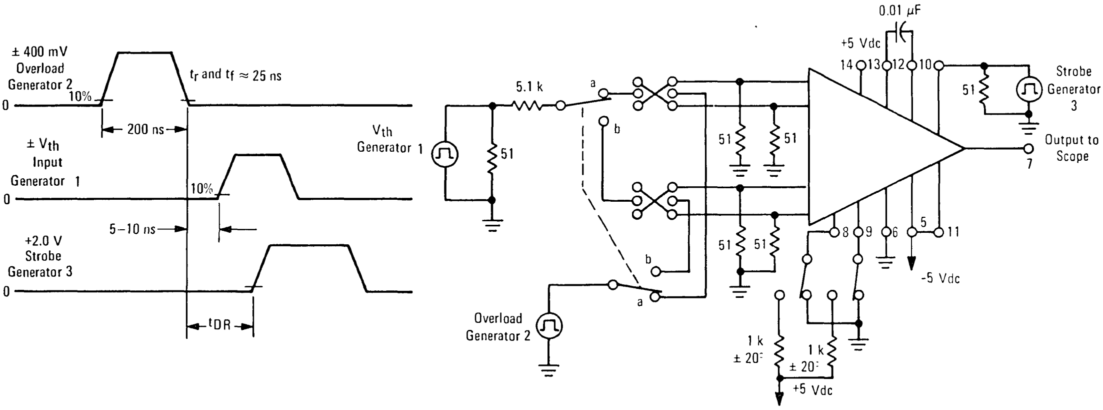


FIGURE 14 – DIFFERENTIAL RECOVERY AND DIFFERENTIAL RANGE



(Pin numbers shown on this page denote the pin numbers for the flat package only; to ascertain the corresponding pin numbers for the dual in-line package , refer to the circuit schematic on the second page.)

DEFINITIONS

Pin numbers referenced in the definitions below denote the flat package only; to ascertain the corresponding pin number for the dual in-line package refer to the circuit schematic.

I_B — Input Bias Current – The average input current defined as $(I_1 + I_2 + I_3 + I_4)/4$.

I_G — Channel Gate Load Current – The amount of current drain from the circuit when the channel gate input (Pin 8 or 9) is grounded.

I_{GR} — Channel Gate Reverse Current – The leakage current when the channel gate input (Pin 8 or 9) is high.

I_{io} — Input Offset Current – The difference between amplifier input current values $|I_1 - I_2|$ or $|I_3 - I_4|$.

I_S — Strobe Load Current – The amount of current drain from the circuit when the strobe pin is grounded.

I_{SR} — Strobe Reverse Current – The leakage current when the strobe input is high.

P_D — Power Dissipation – The amount of power dissipated in the unit.

t_{CMR} — Common Mode Recovery Time – The time required for the voltage at pin 12 to be within 100 mV of the dc value (after overshoot or ringing) as referenced to the 10% point of the trailing edge of a common mode overload signal.

t_{DR} — Differential Recovery Time – The time required for the device to recover from the specified differential input prior to strobe enable as referenced to the 10% point of the trailing edge of an input pulse. The device is considered recovered when the threshold with the overload signal applied is within 1.0 mV of the threshold with no overload input.

t_{GI} — Minimum Time Between Channel Gate Input and Signal Input – The minimum time between 50% point of channel gate input (Pin 8 or 9) and 50% point of signal input (Pins 1, 2, 3, or 4) that still allows a full width signal at amplifier output.

t_{GA} — Propagation Delay, Channel Gate Input to Amplifier Output – The time required for the amplifier output at pin 13 to reach 50% of its final value as referenced to 50% of the input gate pulse at pin 8 or 9 (Amplifier input = 25 mVdc).

t_{IA} — Propagation Delay, Input to Amplifier Output – The time required for the amplifier output pulse at pin 13 to achieve 50% of its final value referenced to 50% of the input pulse at pins 1 and 2 or 3 and 4.

t_{IO} — Propagation Delay, Input to Output – The time required for the gate output pulse at pin 7 to reach the 1.5 Volt level as referenced to 50% of the input pulse at pins 1 and 2 or 3 or 4.

t_{SO} — Strobe Propagation Delay to Output – The time required for the output pulse at pin 7 to reach the 1.5 Volt level as referenced to the 1.5 Volt level of the strobe input at pin 10.

V_{CM} — Maximum Common Mode Input Range – The common mode input voltage which causes the output voltage level of the amplifier to decrease by 100 mV. (This is independent of the channel gate input level.)

V_{DH} — Maximum Differential Input Range, Gate Input High – The differential input which causes the input stage to begin saturation.

V_{DL} — Maximum Differential Input Range, Gate Input Low – The differential input signal which causes the output voltage level of the amplifier to decrease by 100 mV.

V_{GH} — Channel Gate Input Voltage High – Gate pulse amplitude that allows the amplifier output pulse to just reach 100% of its final value. (Amplifier input is set at 25 mVdc).

V_{GL} — Channel Gate Input Voltage Low – Gate pulse amplitude that allows the amplifier output to just reach a 100 mV level. (Amplifier input is set at 25 mVdc).

V_{io} — Input Offset Voltage – The difference in V_{th} between inputs at pins 1 and 2 or 3 and 4.

V_{OH} — Output Voltage High – The high-level output voltage when the output gate is turned off.

V_{OL} — Output Voltage Low – The low-level output voltage when the output gate is saturated and the output sink current is 10 mA.

V_{th} — Input Threshold – Input pulse amplitude at pins 1, 2, 3 or 4 that causes the output gate to just reach V_{OL}.

MC1543L

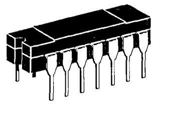
DUAL SENSE AMPLIFIER

DUAL MECL CORE-MEMORY SENSE AMPLIFIER

A dual dc coupled sense amplifier. Output levels are compatible with emitter coupled logic levels. MC1543L offers adjustable threshold and excellent threshold stability over a wide range of power-supply voltage variation.

Typical Amplifier Features:

- Input Threshold
  Adjustable from 10 to 40 mV (Positive or Negative Signals)
- Both OR and NOR Outputs Available
- Low Power Dissipation
- Threshold Insensitive to + or – Supply Variation
- Each Amplifier is Separately Strobed

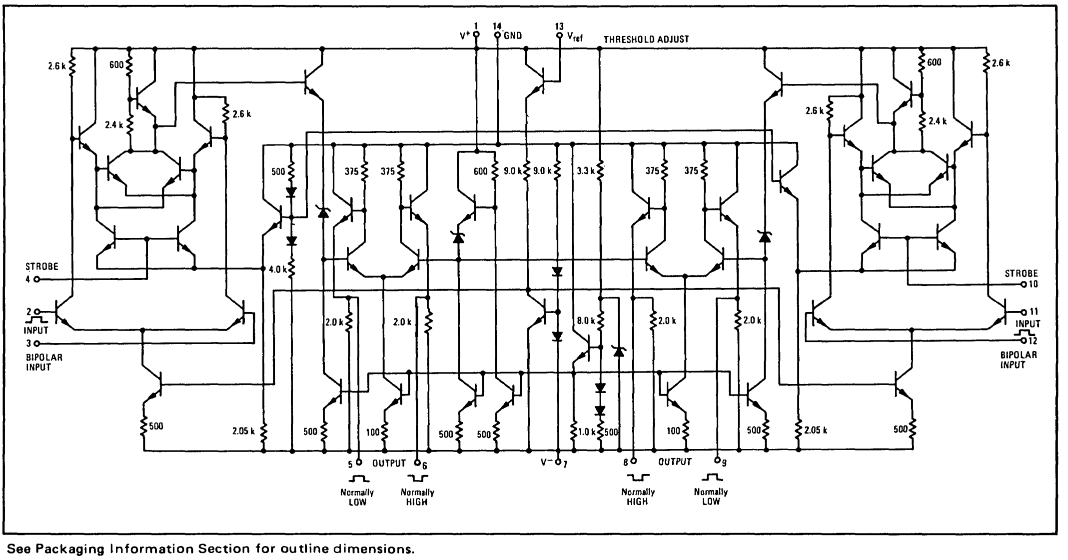


CERAMIC PACKAGE
CASE 632
TO-116

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

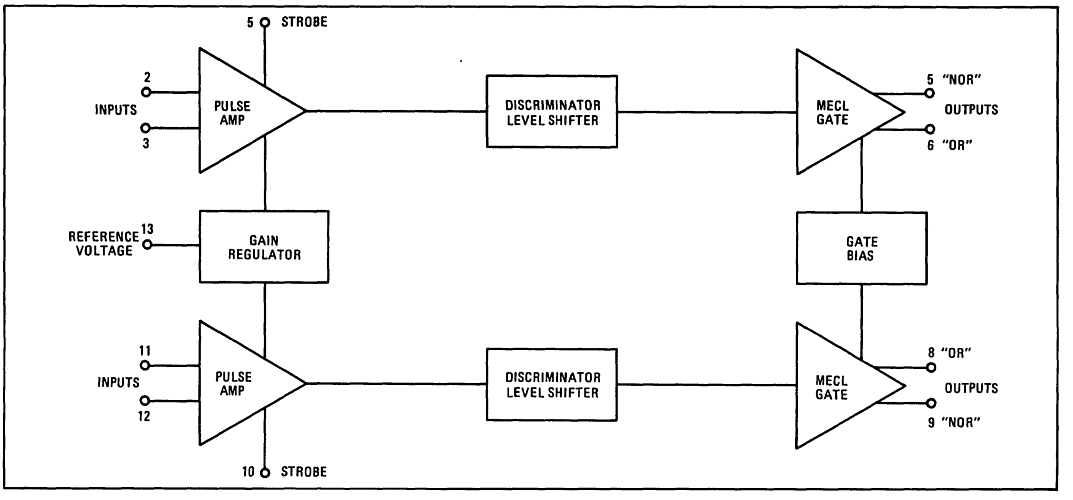
Rating	Symbol	Value	Unit
Power Supply Voltage	V^+ V^-	+10 −10	Vdc Vdc
Differential Input Signal	V_{in}	±5.0	Vdc
Common Mode Input Voltage	CMV_{in}	±5.0	Vdc
Load Current	I_L	25	mA
Power Dissipation (Package Limitation)	P_D		
Ceramic Dual-in-Line Package Derate above 25°C		1000 6.7	mW mW/°C
Operating Temperature Range	T_A	−55 to +125	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

CIRCUIT SCHEMATIC



See Packaging Information Section for outline dimensions.

EQUIVALENT CIRCUIT



ELECTRICAL CHARACTERISTICS (Each Amplifier)
(V^+ = +5.0 Vdc ±5%, V^- = –5.2 Vdc ±5%, V_{ref} = 0.54 V ±1%, T_A = +25°C unless otherwise noted)

Characteristic	Fig. No.	Symbol	Min	Typ	Max	Unit
Input Threshold Voltage	8	V_{th}	17	20	23	mV
Power Supply Currents ($V_2 = V_3 = V_{11} = V_{12} = V_{14} = 0$)	6	I_{CC}	–	9.5	12	mAdc
	6	I_{EE}	–	26.5	33	mAdc
Input Bias Current	7	I_b	–	3.5	10	µAdc
Input Offset Current	7	I_{io}	–	0.05	0.5	µAdc
Output Voltage High	9	V_{OH}	–0.85	–0.8	–0.67	Vdc
Output Voltage Low	9	V_{OL}	–	–1.7	–1.46	Vdc
Strobe Threshold Level	10	V_{ST}	–	–1.30	–	Vdc
Strobe Input Current High	10	I_{SH}	–	25	50	µAdc
Strobe Input Current Low	10	I_{SL}	–	0.01	0.1	µAdc
Input Common Mode Range	14	V_{CM}	3.0	4.0	–	Vdc
Input Threshold Range (by varying V_{ref})	8	V_{thR}	–	10-40	–	mV
Power Dissipation	6	P_D	–	185	230	mW
Reference Supply Input Current (Pin 13)	6	I_{ref}	–	10	40	µA

SWITCHING CHARACTERISTICS

Characteristic	Fig. No.	Symbol	Min	Typ	Max	Unit
Propagation Delay (Input to Output)	11	t_{IO}	–	28	35	ns
Propagation Delay (Strobe to Output)	12	t_{SO}	–	16	20	ns
Strobe Release Time	12	t_{SR}	–	18	30	ns
Recovery Time (Differential Mode) (e_{in} = 400 mVdc)	13	t_{DR}	–	10	15	ns
Recovery Time (Common Mode) (e_{in} = 4.0 Vdc)	14	t_{CMR}	–	3.0	15	ns
Strobe Width Minimum	12	t_S	–	8.0	–	ns

TEMPERATURE TESTS (–55°C to +125°C)

Characteristic	Fig. No.	Symbol	Min	Typ	Max	Unit
Input Threshold Voltage (–55°C)	8	V_{th}	18	21.5	25	mV
Input Threshold Voltage (+125°C)			15	18.5	22	
Input Bias Current	7	I_b	2.2	7.0	20	µAdc
Input Offset Current	7	I_{io}	0.02	0.1	1.0	µAdc

TYPICAL CHARACTERISTICS

FIGURE 1 – TYPICAL INPUT THRESHOLD versus TEMPERATURE

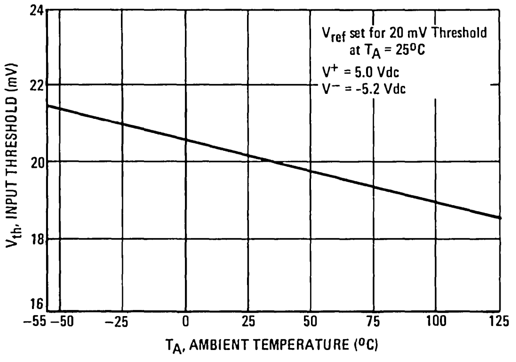


FIGURE 2 – TYPICAL INPUT THRESHOLD versus REFERENCE VOLTAGE

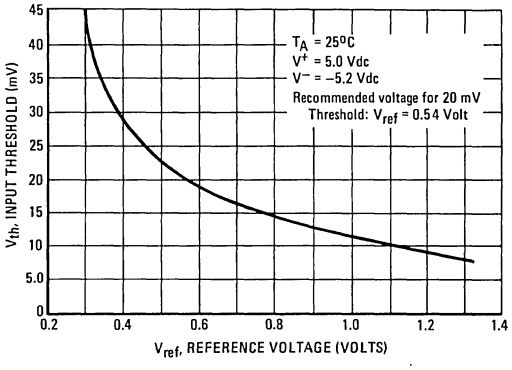


FIGURE 3A – TYPICAL INPUT THRESHOLD versus V^+

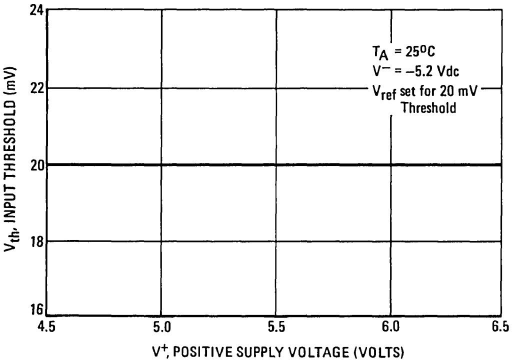


FIGURE 3B – TYPICAL INPUT THRESHOLD versus V^-

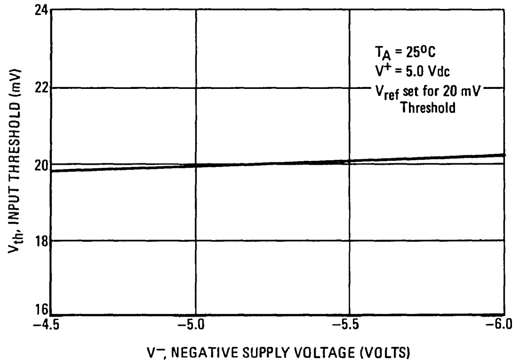


FIGURE 4 – TYPICAL INPUT THRESHOLD versus INPUT PULSE WIDTH

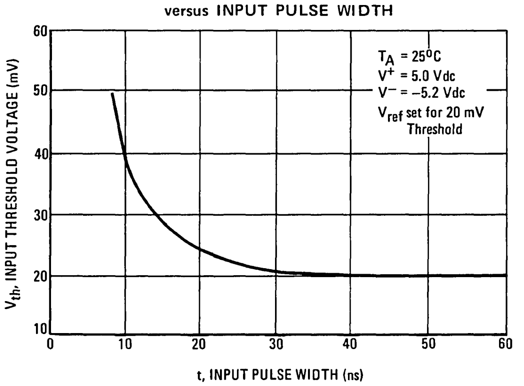


FIGURE 5 – INPUT-OUTPUT TRANSFER CHARACTERISTICS (one output)

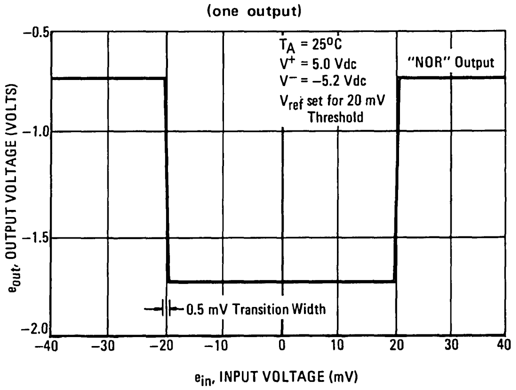


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FIGURE 6 – POWER SUPPLY CURRENT DRAIN

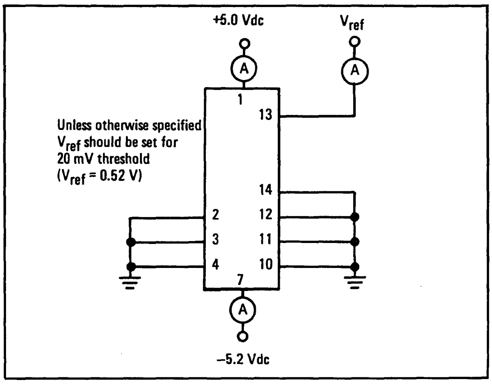


FIGURE 7 – INPUT BIAS CURRENT
INPUT OFFSET CURRENT

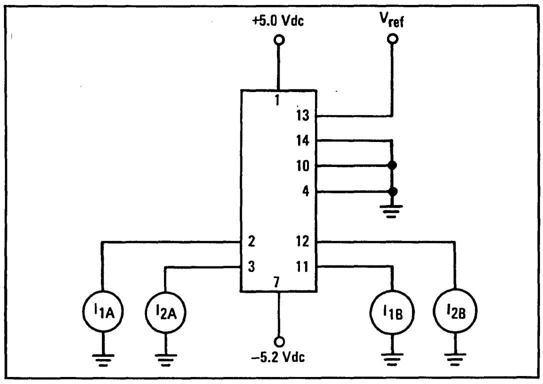


FIGURE 8 – INPUT THRESHOLD LEVEL

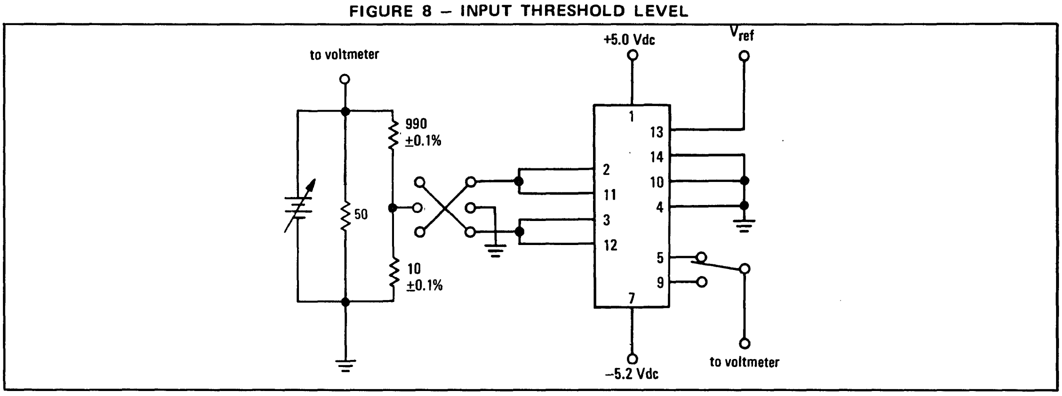


FIGURE 9 – OUTPUT VOLTAGE LEVELS

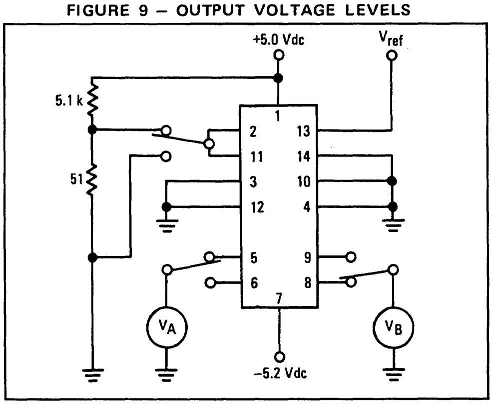


FIGURE 10 – STROBE THRESHOLD LEVEL
STROBE INPUT CURRENTS

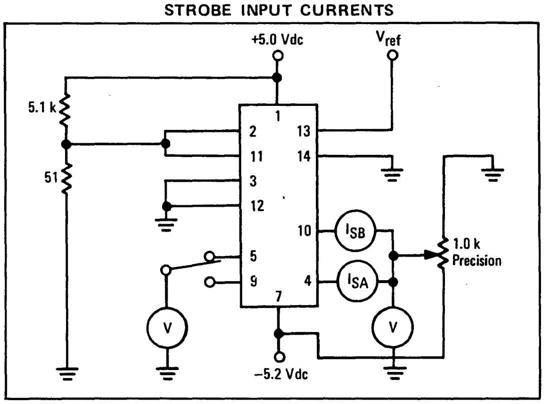


FIGURE 11 – PROPAGATION DELAY – INPUT TO OUTPUT

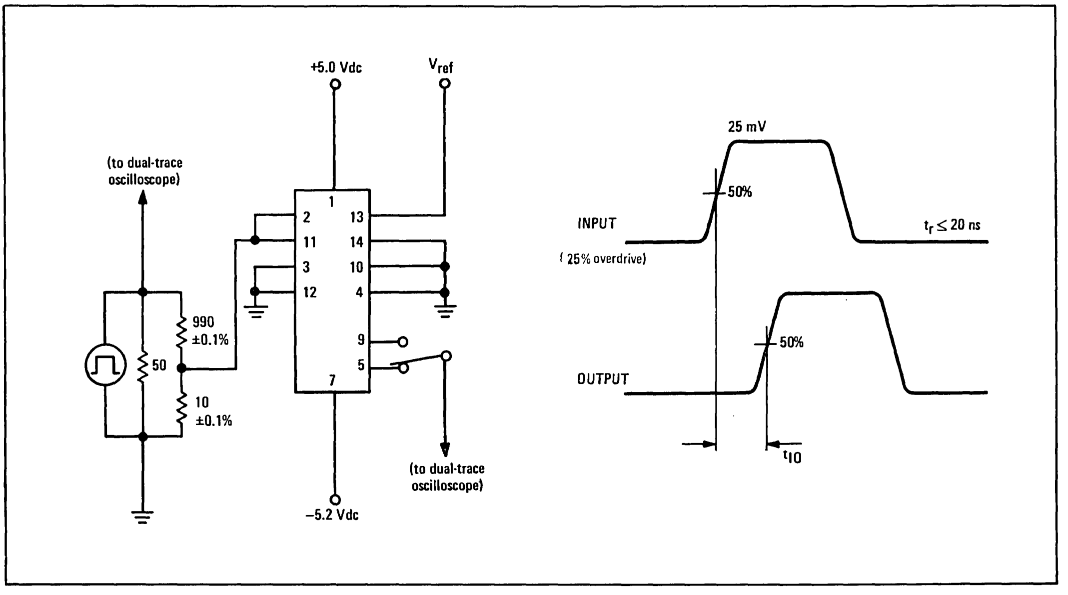


FIGURE 12 – PROPAGATION DELAY – STROBE TO OUTPUT and STROBE RELEASE TIME

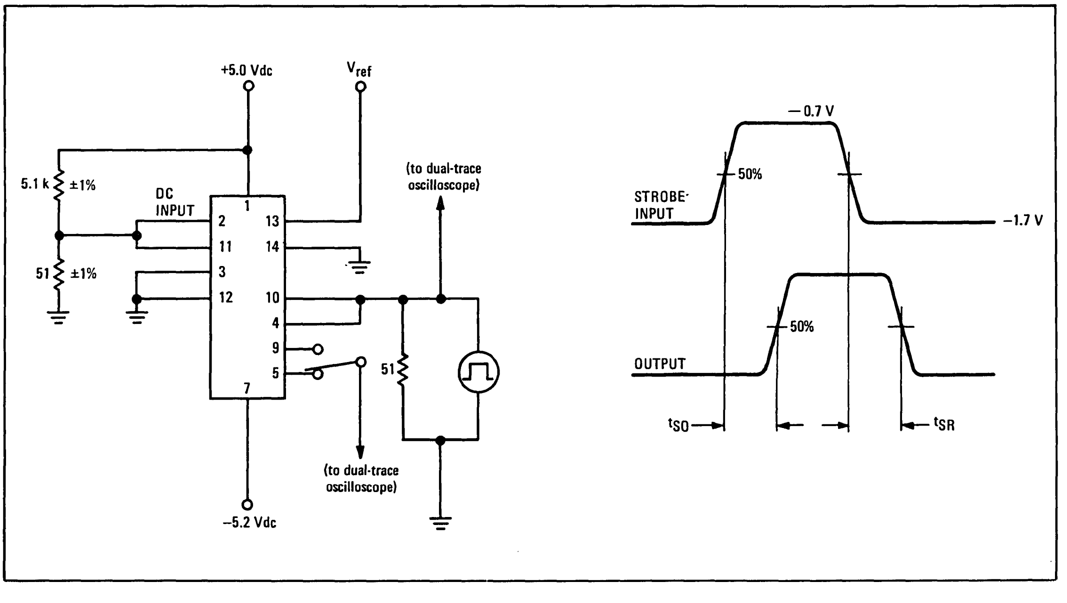


FIGURE 13 – DIFFERENTIAL MODE RECOVERY TIME
(See definition section)

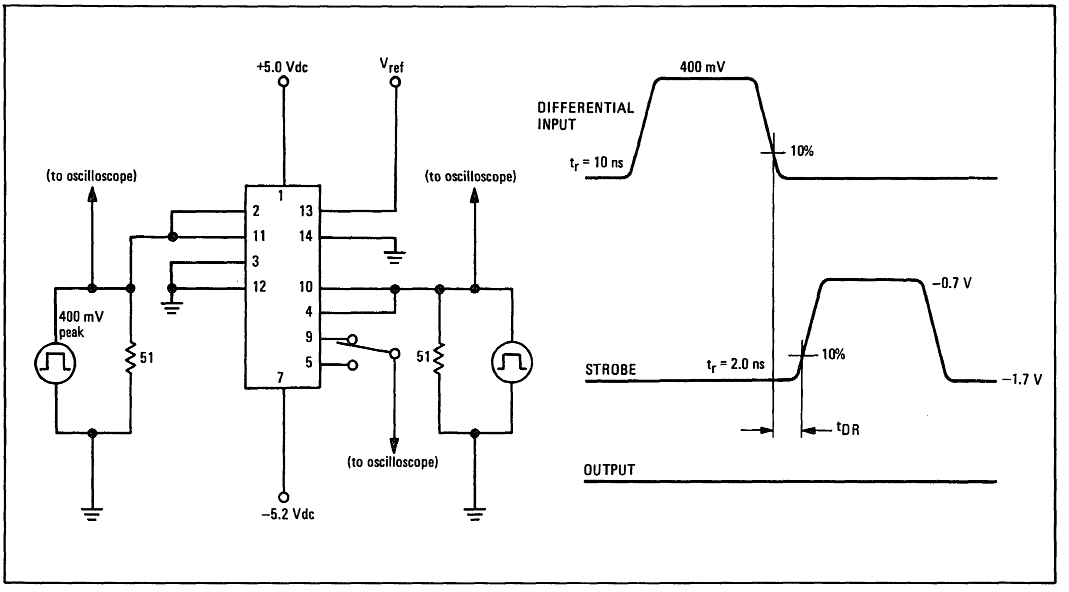
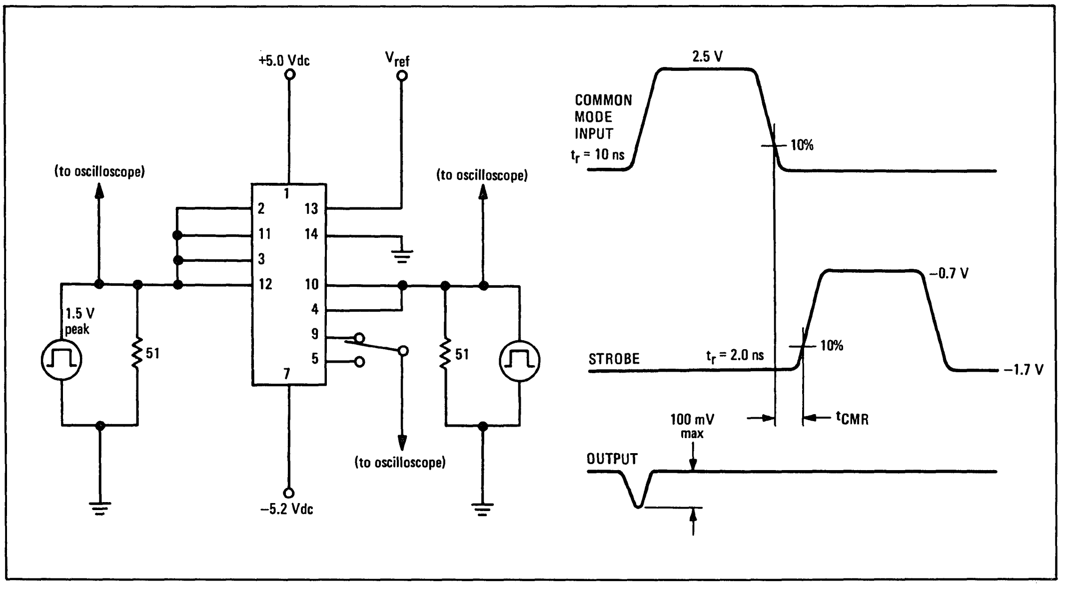


FIGURE 14 – COMMON MODE RECOVERY TIME
COMMON MODE INPUT RANGE
(See definition section)



DEFINITIONS

I_{io} Input Offset Current — The difference between amplifier input current values $|I_{1A} - I_{2A}|$ or $|I_{1B} - I_{2B}|$.

I_{SH} Strobe High Current — The amount of input current when the strobe pin is grounded.

I_{SL} Strobe Low Current — The leakage current when the strobe input is tied to the negative supply.

P_D Power Dissipation — The amount of power dissipated in the unit.

t_{CMR} Common Mode Recovery Time — The minimum time by which the strobe input may follow the high level common mode input signal without causing a signal to appear at the amplifier output.

t_{DR} Differential Mode Recovery Time — Differential recovery time, the minimum time by which the strobe input may follow the high level differential input signal without causing a signal to appear at the amplifier output.

t_{IO} Propagation Delay, Amplifier Input to Amplifier Output — The time required for the amplifier output to reach 50% of its final value as referenced to 50% of the level of the pulse input (Amplifier input = 25 mVdc or 25% over set threshold).

t_S Strobe Width — The amount of time the strobe must be high to obtain a given output. Minimum strobe width is that minimum time required to cause the output to complete a full swing V_{OL} to V_{OH} or V_{OH} to V_{OL}.

t_{SO} Propagation Delay, Strobe Input to Amplifier Output — The time required for the amplifier output pulse to achieve 50% of its final value referenced to 50% of the strobe input pulse at pins 4 or 10.

t_{SR} Strobe Release Time — The time required for the output to change to 50% of its swing after the strobe reaches 50% of its level going low. A dc level of 50 mV is the input signal.

V_{CM} Maximum Common Mode Input Range — The common mode input voltage which causes the output voltage level of the amplifier to change by 100 mV (strobe high).

V_{OH} Output Voltage High — The high-level output voltage at pins 6 and 8 with no input — or at pins 5 and 9 with input above threshold.

V_{OL} Output Voltage Low — The low-level output voltage at pins 5 and 9 with no input — or at pins 6 and 8 with input above threshold.

V_{ST} Strobe Threshold Level — The voltage at which the strobe turns the amplifier to the ON state.

V_{th} Input Threshold — Input pulse amplitude at pins 2, 3, 11, or 12 that causes the output gate to just reach its new value, V_{OL} or V_{OH}.

V_{thR} Input Threshold Range — The maximum spread of input threshold level that can be attained by varying the threshold voltage reference, V_{ref}.

MC1544L
MC1444L

SENSE AMPLIFIERS

Advance Information

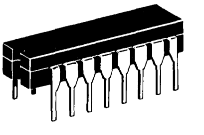
IDEAL FOR PLATED-WIRE, THIN-FILM AND OTHER HIGH-SPEED LOW-LEVEL SENSING APPLICATIONS

MC1544L/MC1444L features four input channels with decoded selection, two stages of gain employing capacitive coupling, and a MTTL compatible output gate. AC coupling reduces access times by eliminating the problems usually associated with input line offset voltages.

- Threshold Level – 1.0 mV typ
- Propagation Delay Time – 18 ns typ
- Decoded Input Channel Selection
- MTTL Compatible Inputs and Outputs
- Wired OR Output Capability
- DC Level Restore Gate on Capacitors Eliminates Repetition Rate Problems Common to ac-Coupled Circuits
- Output Strobe Capability

AC-COUPLED FOUR-CHANNEL SENSE AMPLIFIER

MONOLITHIC SILICON EPITAXIAL PASSIVATED INTEGRATED CIRCUIT



CERAMIC PACKAGE
CASE 620

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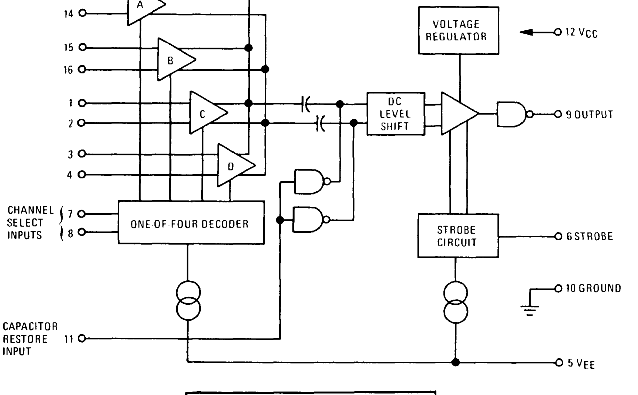
FIGURE 1 – BLOCK DIAGRAM



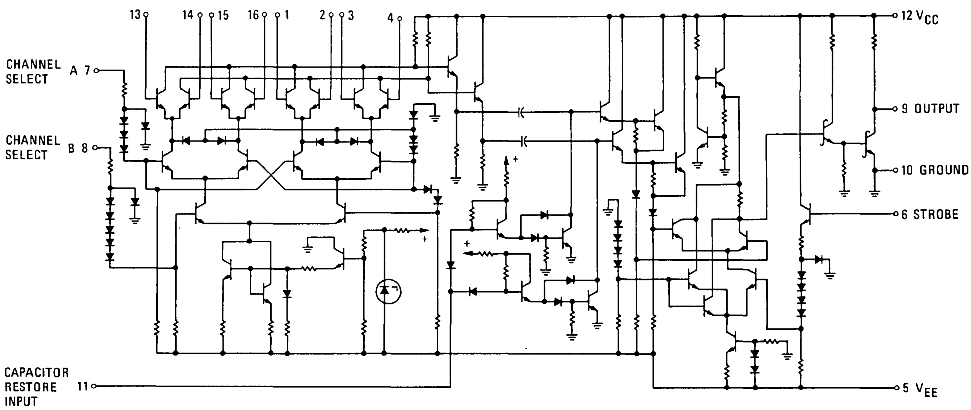
TRUTH TABLE		
PIN 7	PIN 8	CHANNEL SELECTED
HI	HI	A
LO	HI	B
HI	LO	C
LO	LO	D

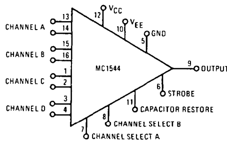
This is advance information and specifications are subject to change without notice.
See Packaging Information Section for outline dimensions.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

RATING	SYMBOL	VALUE	UNIT
Power Supply Voltage	V_{CC} V_{EE}	+7.0 −8.0	Vdc
Common-Mode Input Voltage	V_{CM+} V_{CM-}	+5.0 −6.0	Vdc
Differential-Mode Input Voltage	V_{DM+} V_{DM-}	+5.0 −6.0	Vdc
Capacitor Restore, Channel Select, and Strobe Input Voltage	V_{CR}, V_{CS}, V_S	+5.5	Vdc
Power Dissipation (Package Limitation) Derate above T_A = +25°C	P_D	1.0 6.7	W mW/°C
Operating Temperature Range MC1544L MC1444L	T_A	−55 to +125 0 to +75	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Junction Temperature	T_J	+175	°C

FIGURE 2 – CIRCUIT SCHEMATIC





ELECTRICAL CHARACTERISTICS

(T_A = +25°C unless otherwise noted)

TEST CURRENT/VOLTAGE VALUES													
μA		mA		VOLTS									
I_{CM+}	I_{CM-}	I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IL2}	V_{IH2}	V_{CCL}	V_{CC}	V_{CCH}	V_{EEL}	V_{EE}	V_{EEH}
200	−10	10	−0.4	0.8	2.0	0	3.5	4.75	5.0	5.25	−5.7	−6.0	−6.3

Characteristic		Symbol	Pin Under Test	Min	Typ	Max	Unit	I_1	I_2	I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IL2}	V_{IH2}	V_{CCL}	V_{CC}	V_{CCH}	V_{EEL}	V_{EE}	V_{EEH}	GND
								TEST CURRENT/VOLTAGES APPLIED TO PINS LISTED BELOW:														
Input Threshold Voltage (Note 1)	MC1544L	V_{TH}	13	–	1.0	–	mV	–	–	–	–	–	–	–	–	–	12	–	–	5	–	10
T_{low}* to T_{high}*	MC1444L		13	–	1.0	–	mV	–	–	–	–	–	–	–	–	–	12	–	–	5	–	10
Input Bias Current (Note 1)		I_b	13	–	20	–	μA	–	–	–	–	–	–	13, 14	7, 8	–	–	12	–	–	5	10
Input Offset Current		I_{io}	13, 14	–	1.0	–	μA	–	–	–	–	–	–	13, 14	7, 8	–	–	12	–	–	5	10
Channel Select Input Current (Note 2)	High Level	I_{CSH}	7	–	1.8	3.0	mA	–	–	–	–	–	–	–	7	–	–	12	–	–	5	10
	Low Level	I_{CSL}	7	–	0.6	1.0	mA	–	–	–	–	–	–	7	–	–	–	12	–	–	5	10
Capacitor Restore Input Current	High Level	I_{CRH}	11	–	0	10	μA	–	–	–	–	–	–	–	11	–	–	12	–	–	5	10
	Low Level	I_{CRL}	11	–	−2.5	−3.5	mA	–	–	–	–	–	–	11	–	–	–	12	–	–	5	10
Strobe Input Current	Low/High Level	I_S	6	–	40	200	μA	–	–	–	–	–	–	–	6	–	–	12	–	–	5	10
Channel Select Input Voltage (Note 3)	High Level	V_{CSH}	7	2.1	1.6	–	V	–	–	–	–	–	7	3, 8 13, 15	–	–	12	–	–	5	–	10
	Low Level	V_{CSL}	7	–	1.2	0.7	V	–	–	–	–	7	–	1, 8 13, 15	–	–	12	–	–	5	–	10
Channel Select Input Voltage (Note 3)	High Level	V_{CSH}	8	2.1	1.5	–	V	–	–	–	–	–	8	1, 3 7, 13	–	–	12	–	–	5	–	10
	Low Level	V_{CSL}	8	–	1.0	0.7	V	–	–	–	–	8	–	1, 7 13, 15	–	–	12	–	–	5	–	10
Capacitor Restore Input Voltage (Note 4)	High Level	V_{CRH}	11	2.0	1.5	–	V	–	–	–	–	–	11	–	6	–	12	–	–	5	–	10
	Low Level	V_{CRL}	11	–	1.5	0.8	V	–	–	–	–	11	–	–	6	–	12	–	–	5	–	10
Strobe Input Voltage (Note 4)	High Level	V_{SH}	6	2.0	1.5	–	V	–	–	–	–	–	6	11	–	–	12	–	–	5	–	10
	Low Level	V_{SL}	6	–	1.5	0.8	V	–	–	–	–	6	–	11	–	–	12	–	–	5	–	10
Output Voltage	High Level	V_{OH}	9	2.4	3.6	–	V	–	–	–	9	6	–	–	–	12	–	–	5	–	–	10
	Low Level	V_{OL}	9	–	0.4	0.5	V	–	–	9	–	–	–	–	–	12	–	–	–	–	–	10
Power Supply Currents	Positive	I_{CC}	12	15	22	30	mA	–	–	–	–	–	–	6, 13, 14	7, 8, 11	–	–	12	–	–	5	10
	Negative	I_{EE}	5	15	20	30	mA	–	–	–	–	–	–	6, 13, 14	7, 8, 11	–	–	12	–	–	5	10
Common-Mode Range Voltage (Note 1)		V_{CM^+} V_{CM^-}	13, 14 13, 14	– –	4.7 −6.0	– –	Vdc Vdc	13, 14 13, 14	– –	– –	– –	– –	– –	– –	7, 8 7, 8	– –	12 12	– –	– –	5 5	– –	10 10
Differential-Mode Range Voltage		V_{DM}	13	–	3.7	–	Vdc	13	–	–	–	–	–	14	7, 8	–	12	–	–	5	–	10

*MC1544 T_{low} −55°C, T_{high} = +125°C, MC1444 T_{low} = 0°C, T_{high} = +75°C.

NOTES:

1. Only one input test is shown, other inputs are tested in the same manner and are selected according to the truth table in Figure 1.
2. Pin 8 is tested in the same manner.
3. This requirement is considered satisfied if the input bias currents of all unselected channels total less than 1.0 μA which guarantees that these channels are "off."
4. This requirement is evaluated during the ac threshold test (Figures 1, 2): A 10 mV signal (e_{in_1}) is applied to the input, V_{CRH} will result in V_{OH} at the output while V_{CRL} will allow normal operation.
5. This requirement is evaluated as in Note 4 except V_{SH} allows normal operation and V_{SL} causes V_{OH} at the output.

SWITCHING CHARACTERISTICS (T_A = +25°C unless otherwise noted)

Characteristic		Symbol	Figure	Min	Typ	Max	Unit
Propagation Delay Time		t_{pd-} t_{pd+}	1, 5	– –	18 40	25 –	ns
Strobe to Input Lead Time		t_{si}	1, 5	–	10	–	ns
Strobe to Output Delay Time		t_{so-} t_{so+}	1, 6	– –	18 30	25 –	ns
Channel Select to Input Lead Time		t_{csi}	1, 5	–	15	–	ns
Channel Select to Output Delay Time		t_{cso-} t_{cso+}	1, 7	– –	25 40	– –	ns
Capacitor Restore to Input Lead Time		t_{cri}	1, 5	–	10	–	ns
Capacitor Restore Time (50 mV Offset)		t_{cr}	1, 8	–	15	–	ns
Common-Mode Recovery Time	e_{in_1} = +2.0V e_{in_1} = −2.0V	t_{CMR+} t_{CRM-}	19	– –	50 50	– –	ns
Differential-Mode Recovery Time	e_{in_1} = +1.0V e_{in_1} = −1.0V	t_{DMR+} t_{DMR-}	20	– –	65 65	– –	ns

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FIGURE 3 – AC TEST CIRCUIT

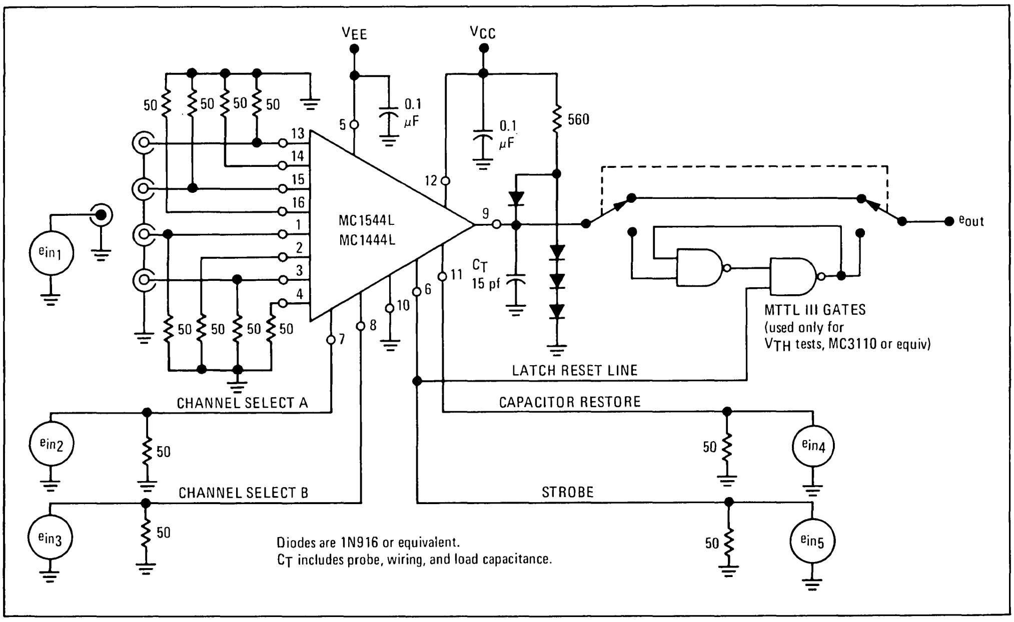


FIGURE 4 – THRESHOLD VOLTAGE TEST

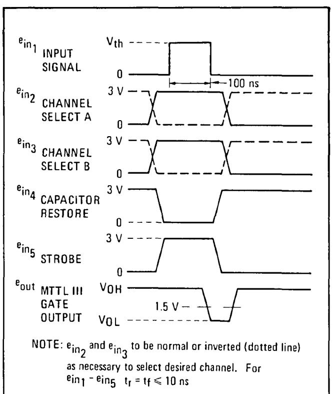


FIGURE 5 – t_{csi}, t_{cri}, t_{si}, t_{pd-}, t_{pd+}

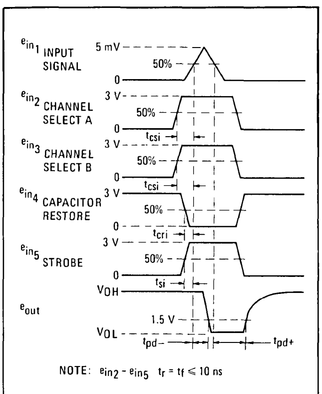


FIGURE 6 – t_{so-}, t_{so+}

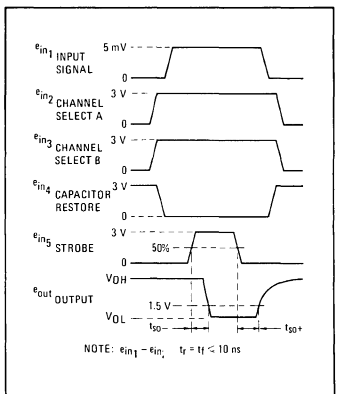


FIGURE 7 – t_{cso+}, t_{cso-}

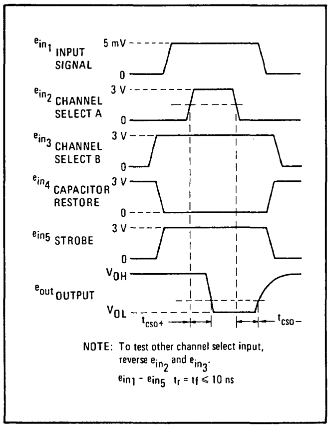
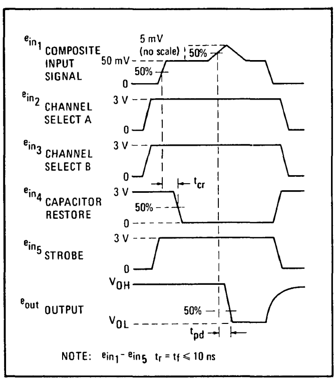


FIGURE 8 – t_{cr}



DEFINITIONS

I_b	Input current to the base of any input transistor when the base of the other transistor of the differential pair is at the same voltage
I_{CC}	Positive power supply current
I_{CRH}	The current into the channel select input when the input is at a high-level of 3.5 volts
I_{CRL}	The current out of the capacitor restore input when the input is at a low-level of 0 volts
I_{CSH}	The input current to a channel select input when that input is at a high-level of 3.5 volts
I_{CSL}	The current into a channel select input when the input is at a low-level of 0 volts
I_{EE}	Negative power supply current
I_{io}	The difference between the base currents of any input differential pair of transistors when the base voltages are equal
I_{OH}	Output logic "1" state source current
I_{OL}	Output logic "0" state sink current
I_{SH}	The current into the strobe input when the input is at a high-level of 3.5 volts
I_{SL}	The current into the strobe input when the input is at a low-level of 0 volts
$t_{CMR\pm}$	The minimum time between the 50% level of the trailing edge of a + or - 2 volt common-mode signal ($t_r = t_f \leq 15$ ns) and the 50% level of the leading edge of a 5 mV input pulse when the capacitor restore and strobe inputs are used in a normal manner as shown in Figure 21
t_{cr}	The minimum time between the 50% level of the leading edge of a 50 mV input offset signal and the 50% level of the leading edge of the capacitor restore pulse as shown in Figure 8
t_{cri}	The minimum time between the 50% level of the leading edge of the capacitor restore signal and the 50% level of the leading edge of a 5 mV input signal as shown in Figure 5
t_{csi}	The minimum time between the 50% level of the leading edge of the channel select and the 50% level of the leading edge of a 5 mV input signal as shown in Figure 5
t_{cso+}	The delay time from the 50% level of the trailing edge of the channel select signal to the 1.5 volt level of the positive edge of the output when the input to the selected channel is held at the "1" level as shown in Figure 7
t_{cso-}	The delay time from the 50% level of the leading edge of the channel select signal to the 1.5 volt level of the negative edge of the output when the input to the selected channel is held at the "1" level as shown in Figure 7
$t_{DMR\pm}$	The minimum time between the 50% level of the trailing edge of a + or - 1 volt differential-mode signal ($t_r = t_f \leq 15$ ns) and the 50% level of the leading edge of a 5 mV input pulse when the capacitor restore and strobe inputs are used in a normal manner as shown in Figure 22
t_{pd+}	The delay time from the 50% level of the trailing edge of a 5 mV input signal to the 1.5 volt level of the positive edge of the output as shown in Figure 5
t_{pd-}	The delay time from the 50% level of the leading edge of a 5 mV input signal to the 1.5 volt level of the negative edge of the output as shown in Figure 5
t_{si}	The minimum time between the 50% level of the leading edge of the strobe and the 50% level of the leading edge of the input signal as shown in Figure 5
t_{so+}	The delay time from the 50% level of the trailing edge of the strobe to the 1.5 volt level of the positive edge of the output when the input is held at the "1" level as shown in Figure 6
t_{so-}	The delay time from the 50% level of the leading edge of the strobe to the 1.5 volt level of the negative edge of the output when the input is held at the "1" level as shown in Figure 6
V_{CC}	Positive power supply voltage
V_{CCH}	Maximum operating positive power supply voltage
V_{CCL}	Minimum operating positive power supply voltage
V_{CM^+}	The maximum common-mode input voltage that will not saturate the amplifier
V_{CM^-}	The minimum common-mode input voltage that will not break down the amplifier
V_{CRH}	The minimum high-level voltage at the capacitor restore input required to insure that the capacitors are clamped i.e., the input threshold voltage is greater than 10 mV
V_{CRL}	The maximum low-level voltage at the capacitor restore input which will allow normal operation during the threshold test
V_{CSH}	The minimum high-level voltage at a channel select input required to insure that the total of the base currents of all unselected inputs is less than 1.0 μA
V_{CSL}	The maximum low-level voltage at a channel select input required to insure that the total of the base currents of all unselected inputs is less than 1.0 μA
V_{DM}	The maximum differential-mode input voltage that will not saturate the amplifier
V_{EE}	Negative power supply voltage
V_{EEH}	Maximum operating negative power supply voltage
V_{EEL}	Minimum operating negative power supply voltage
V_{OH}	Logic "1" state output voltage
V_{OL}	Logic "0" state output voltage
V_{SH}	The minimum high-level voltage at the strobe input which will allow normal operation during the threshold test
V_{SL}	The maximum low-level voltage at the strobe input which will result in V_{OH} at the output regardless of input signals
V_{th}	The minimum input signal ($e_{in\,1}$) required to drive the MTTL III gates to obtain the e_o waveform shown in Figure 4

TYPICAL CHARACTERISTICS

(T_A = +25°C unless otherwise noted)

FIGURE 9 – THRESHOLD VOLTAGE versus TEMPERATURE

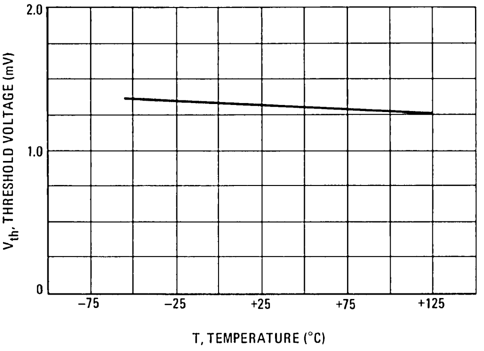


FIGURE 10 – THRESHOLD VOLTAGE versus POWER SUPPLIES

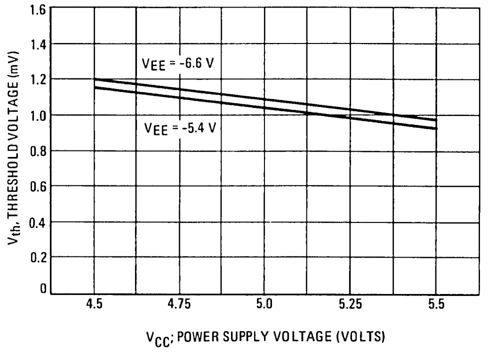


FIGURE 11 – THRESHOLD versus INPUT OFFSET VOLTAGE

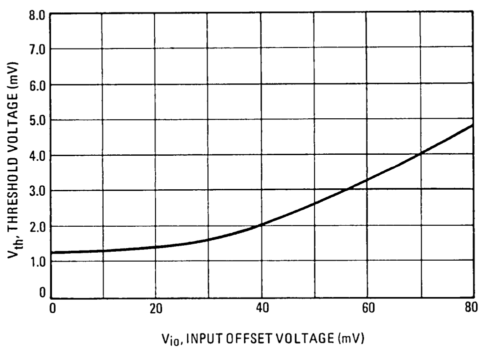


FIGURE 12 – THRESHOLD VOLTAGE versus PULSE WIDTH

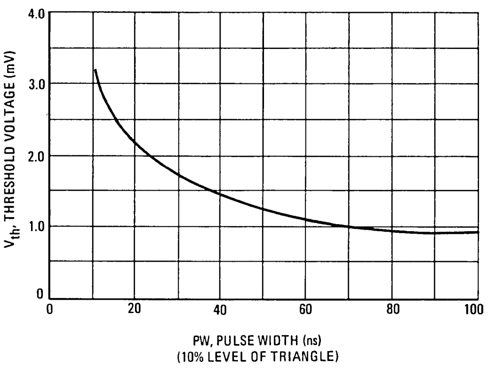


FIGURE 13 – OUTPUT VOLTAGE versus CURRENT and TEMPERATURE

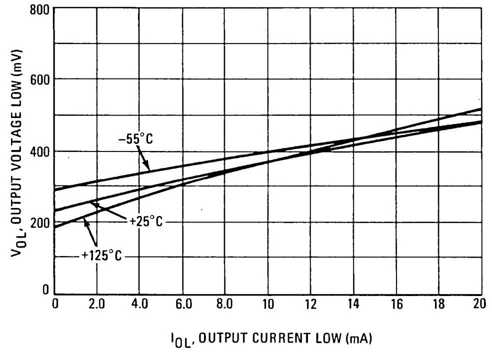
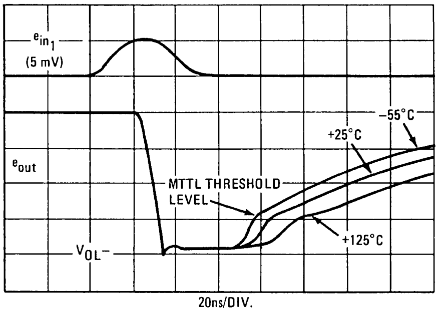


FIGURE 14 – SENSE AMPLIFIER RESPONSE versus TEMPERATURE (See Figures 3 and 5)



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TYPICAL CHARACTERISTICS (continued)

FIGURE 15 – INPUT IMPEDANCE versus FREQUENCY

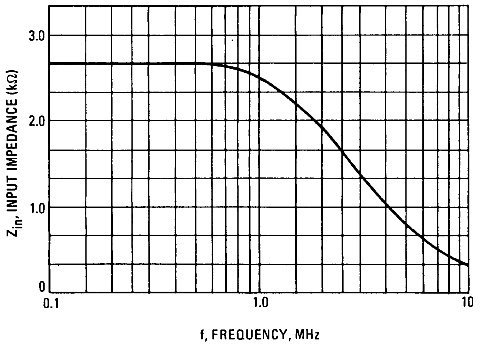


FIGURE 16 – CAPACITOR RESTORE TIME versus INPUT OFFSET VOLTAGE

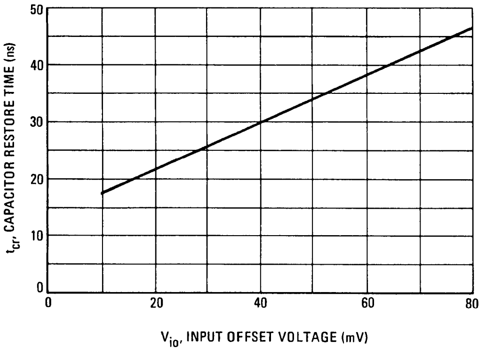


FIGURE 17 – AMPLIFIER INPUT TO OUTPUT TRANSFER CHARACTERISTIC

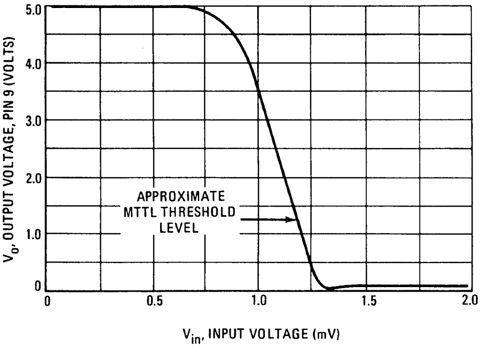


FIGURE 18 – STROBE TO OUTPUT TRANSFER CHARACTERISTICS

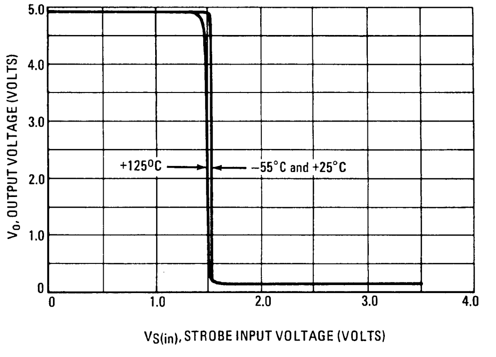


FIGURE 19 – CHANNEL SELECT A to OUTPUT TRANSFER CHARACTERISTICS

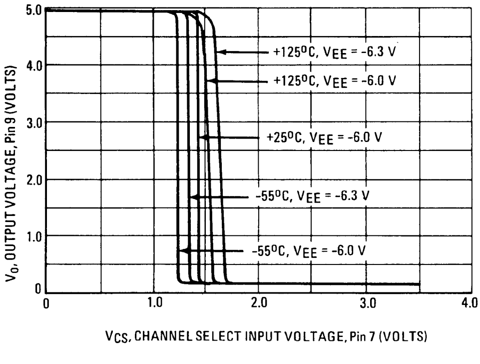


FIGURE 20 – CHANNEL SELECT B to OUTPUT TRANSFER CHARACTERISTICS

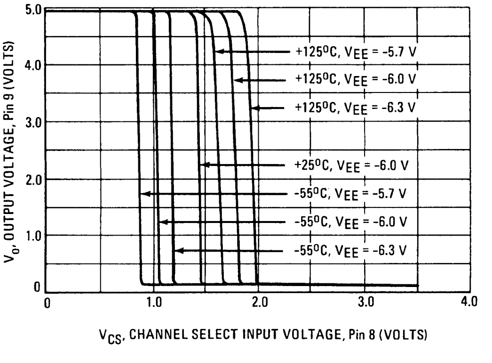


FIGURE 21 – COMMON-MODE CHARACTERISTICS

Note: The 5mV Input Signal (Differential) is superimposed on the Common-Mode Input and is shown separately for reference only.

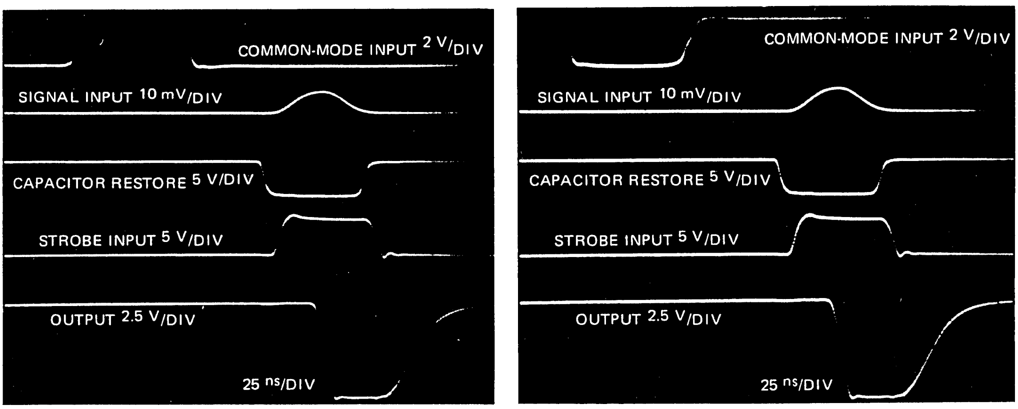
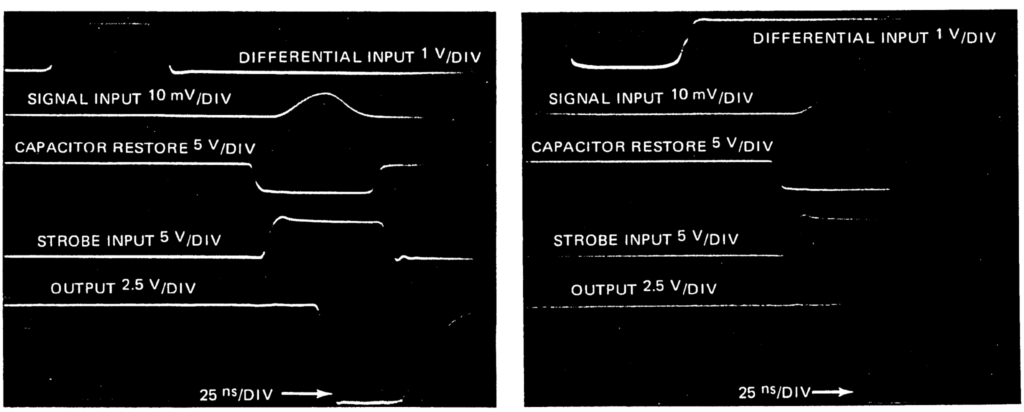


FIGURE 22 – DIFFERENTIAL-MODE CHARACTERISTICS

Note: The 5mV Input Signal is superimposed on the Differential Input and is shown separately for reference only.



MC1545
MC1445

GATE CONTROLLED TWO-CHANNEL-INPUT WIDEBAND AMPLIFIER

. . . designed for use as a general-purpose gated wideband-amplifier, video switch, sense amplifier, multiplexer, modulator, FSK circuit, limiter, AGC circuit, or pulse amplifier. See Application Notes AN475 and AN491 for design details.

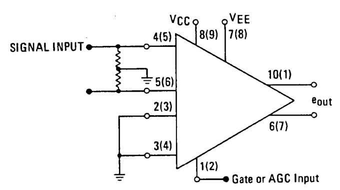
- Large Bandwidth; 75 MHz typical
- Channel-Select Time of 20 ns typical
- Differential Inputs and Differential Output

GATE CONTROLLED TWO-CHANNEL-INPUT WIDEBAND AMPLIFIER

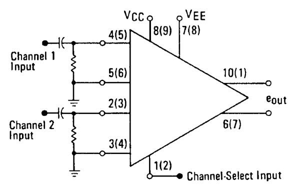
MONOLITHIC SILICON EPITAXIAL PASSIVATED

TYPICAL APPLICATIONS

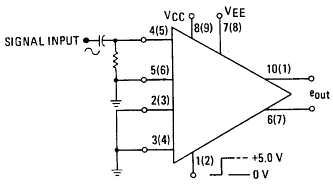
VIDEO SWITCH OR DIFFERENTIAL AMPLIFIER WITH AGC



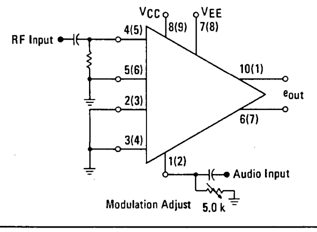
MULTIPLEX OR FSK



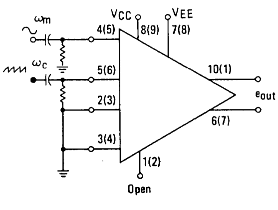
ANALOG SWITCH



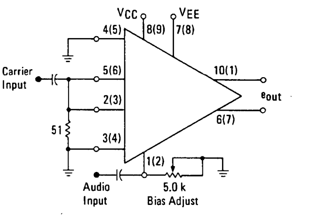
AMPLITUDE MODULATOR



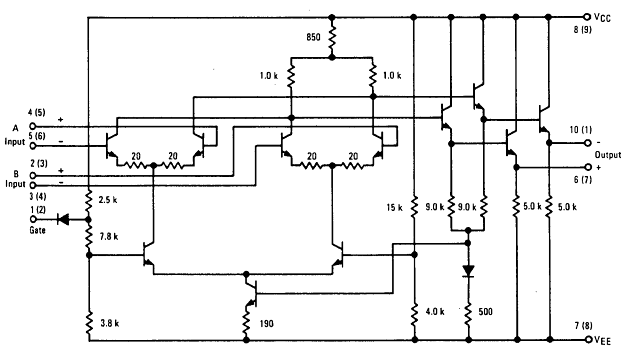
PULSE-WIDTH MODULATOR



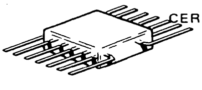
BALANCED MODULATOR



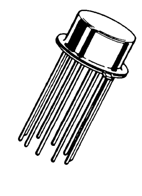
CIRCUIT SCHEMATIC



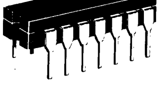
Number in parenthesis denotes pin for F and L packages, number at left in each case denotes corresponding pin for G package.



F SUFFIX
CERAMIC PACKAGE
CASE 607
TO-86



G SUFFIX
METAL PACKAGE
CASE 602A



L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

See Packaging Information Section for outline dimensions.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating		Symbol	Value	Unit
Power Supply Voltage		V_{CC} V_{EE}	+12 -12	Vdc Vdc
Differential Input Signal		V_{ID}	±5.0	Volts
Load Current		I_L	25	mA
Power Dissipation (Package Limitation)		P_D		
Flat Package			500	mW
Derate above T_A = +25°C			3.3	mW/°C
Ceramic Dual In-Line Package			625	mW
Derate above T_A = +25°C			5.0	mW/°C
Metal Can			680	mW
Derate above T_A = +25°C			4.6	mW/°C
Operating Temperature Range	MC1445 MC1545	T_A	0 to +75 -55 to +125	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 Vdc, V_{EE} = 5.0 Vdc, at T_A = +25°C, specifications apply to both input channels unless otherwise noted)

Characteristic		Fig. No.	Symbol*	Min	Typ	Max	Unit
Single-Ended Voltage Gain	MC1445 MC1545	1, 12	A_{vs}	16 16	19 18	22 20	dB
Bandwidth	MC1445 MC1545	1, 12	BW	– 50	75 75	– –	MHz
Input Impedance (f = 50 kHz)	MC1445 MC1545	5, 14	z_{is}	3.0 4.0	10 10	– –	k ohms
Output Impedance (f = 50 kHz)		6, 15	z_{os}	–	25	–	Ohms
Output Voltage Swing (R_L = 1.0 k ohm, f = 50 kHz)		4, 13	V_{OD}	1.5	2.5	–	V_{p-p}
Input Bias Current ($I_{IB} = (I_1 + I_2)/2$)	MC1445 MC1545	16	I_{IB}	– –	15 15	30 25	µAdc
Input Offset Current		16	$\lvert I_{IO}\rvert$	–	2.0	–	µAdc
Input Offset Voltage	MC1445 MC1545	17	$\lvert V_{IO}\rvert$	– –	– 1.0	7.5 5.0	mVdc
Quiescent Output dc Level		17	V_O	–	0.2	–	Vdc
Output dc Level Change (Gate Voltage Change: +5.0 V to 0 V)		17	$\lvert \Delta V_O \rvert$	–	15	–	mV
Common-Mode Rejection Ratio (f = 50 kHz)		9, 18	CMRR	–	85	–	dB
Input Common-Mode Voltage Swing		18	V_{ICR}	–	±2.5	–	V_p
Gate Characteristics		8					Vdc
Gate Voltage Low (See Note 1)	MC1445 MC1545		V_{GOL}	0.20 0.45	0.40 0.70	– –	
Gate Voltage High (See Note 2)	MC1445 MC1545		V_{GOH}	– –	1.3 1.5	3.0 2.2	
Gate Current Low (Gate Voltage = 0 V)	MC1445 MC1545	18	I_{GOL}	– –	– –	4.0 2.5	mA
Gate Current High (Gate Voltage = +5.0 V)	MC1445 MC1545	18	I_{GOH}	– –	– –	4.0 2.0	µA
Step Response (e_{in} = 20 mV)	MC1445 MC1545	19	t_{PLH}	– –	6.5 6.5	– 10	ns
	MC1445 MC1545		t_{PHL}	– –	6.3 6.3	– 10	
	MC1445 MC1545		t_r	– –	6.5 6.5	– 10	
	MC1445 MC1545		t_f	– –	7.0 7.0	– 10	
Wideband Input Noise (5.0 Hz – 10 MHz, R_S = 50 ohms)		10, 20	$V_{N(in)}$	–	25	–	µV(rms)
DC Power Dissipation	MC1445 MC1545	11, 20	P_D	– –	70 70	150 110	mW

Note 1 V_{GOL} is the gate voltage which results in channel A gain of unity or less and channel B gain of 16 dB or greater.
Note 2 V_{GOH} is the gate voltage which results in channel B gain of unity or less and channel A gain of 16 dB or greater.
*Symbols conform to JEDEC Engineering Bulletin No. 1 when applicable.

FIGURE 1 – SINGLE-ENDED VOLTAGE GAIN versus FREQUENCY

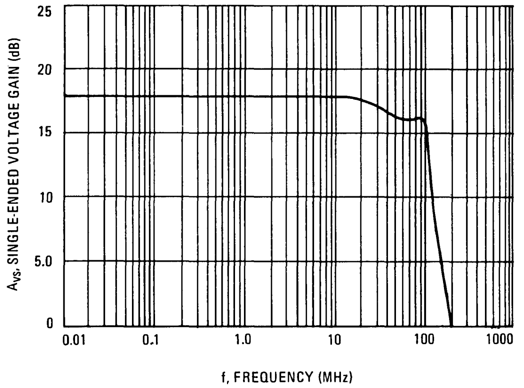


FIGURE 2 – SINGLE-ENDED VOLTAGE GAIN versus TEMPERATURE

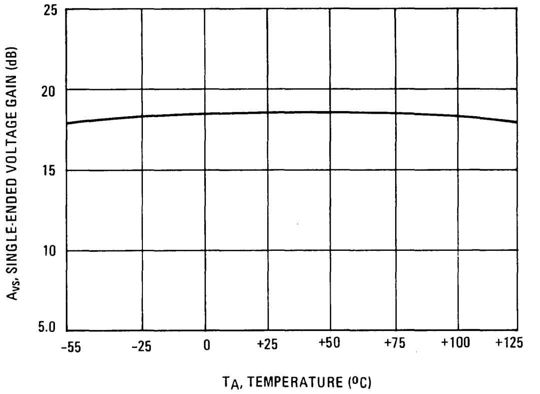


FIGURE 3 – VOLTAGE GAIN versus POWER SUPPLY VOLTAGES

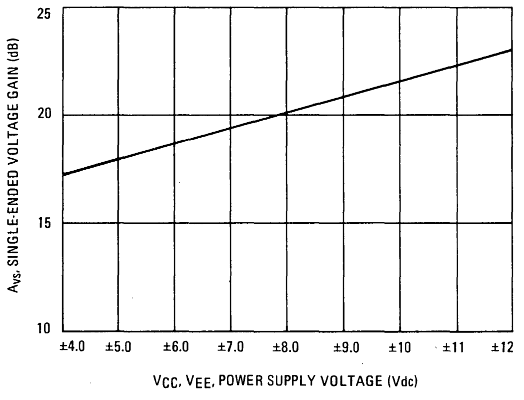


FIGURE 4 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

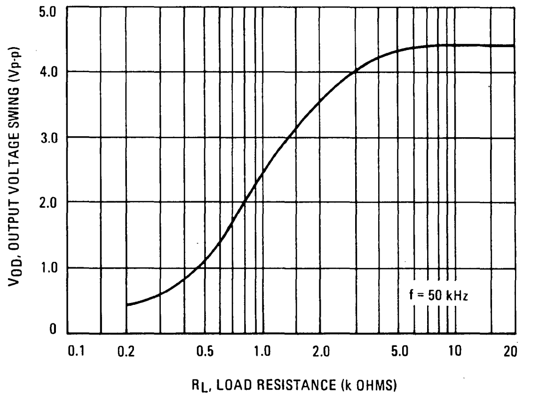


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FIGURE 5 – INPUT Cp AND Rp versus FREQUENCY (BOTH CHANNELS)

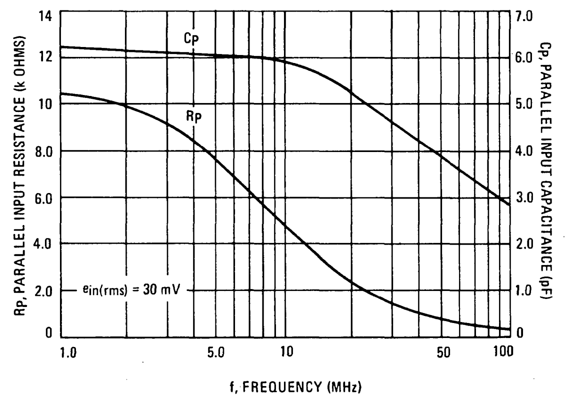


FIGURE 6 – OUTPUT IMPEDANCE versus FREQUENCY

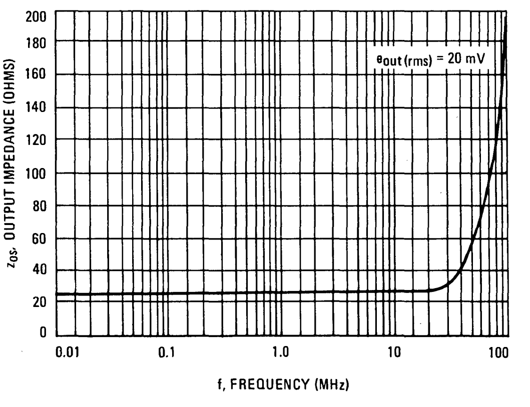


FIGURE 7 – CHANNEL SEPARATION versus FREQUENCY

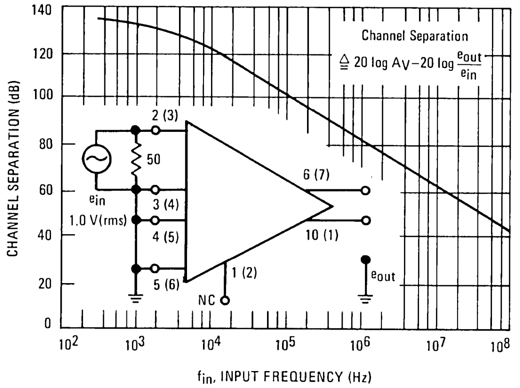


FIGURE 8 – GATE CHARACTERISTICS

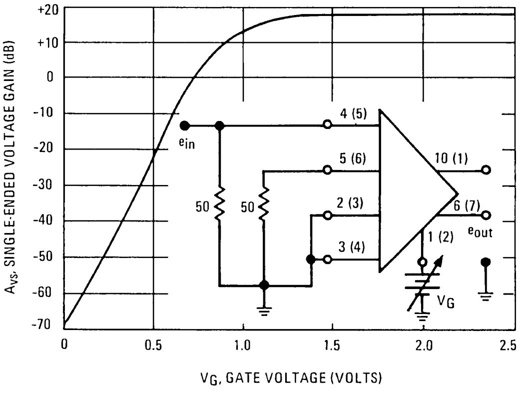


FIGURE 9 – COMMON MODE REJECTION RATIO versus FREQUENCY

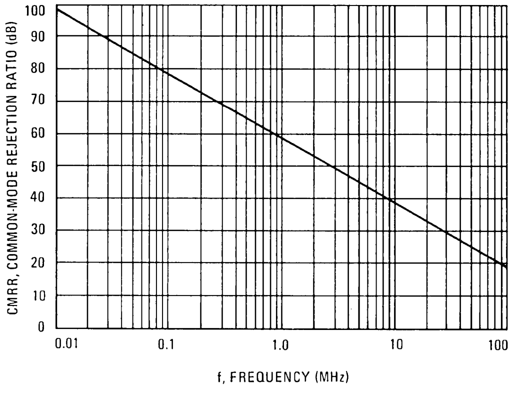


FIGURE 10 – INPUT WIDEBAND NOISE versus SOURCE RESISTANCE

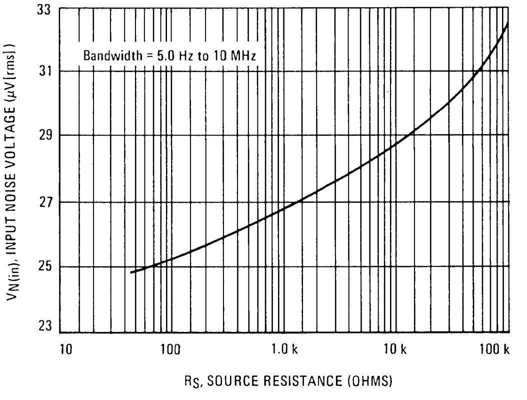


FIGURE 11 – POWER DISSIPATION versus POWER SUPPLY VOLTAGE

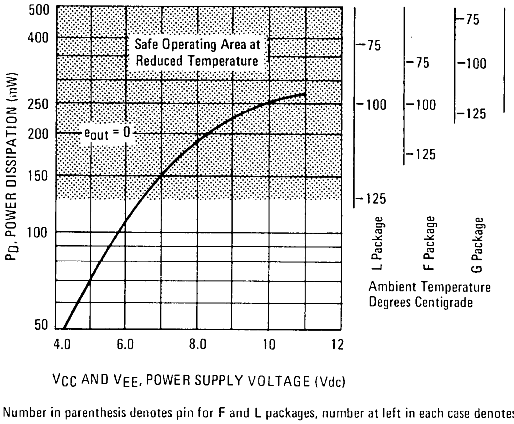
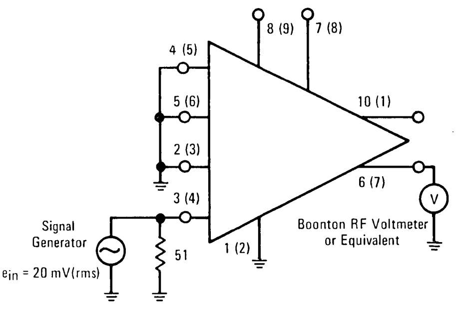


FIGURE 12 – SINGLE-ENDED VOLTAGE GAIN AND BANDWIDTH TEST CIRCUIT



Number in parenthesis denotes pin for F and L packages, number at left in each case denotes corresponding pin for G package.

FIGURE 13 – OUTPUT VOLTAGE SWING TEST CIRCUIT

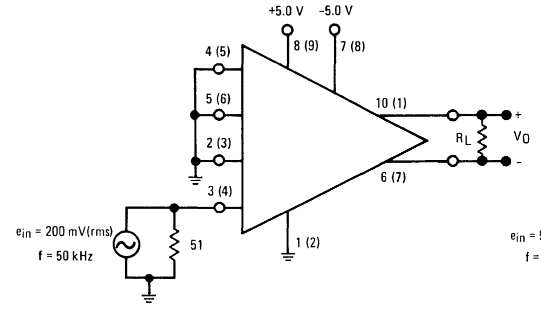


FIGURE 14 – INPUT IMPEDANCE TEST CIRCUIT

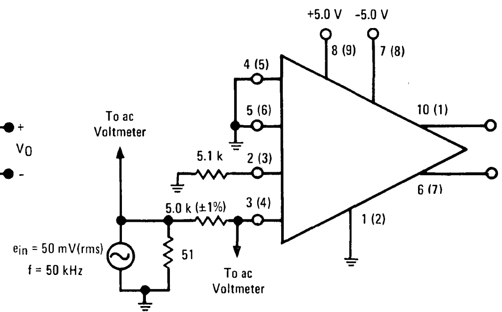


FIGURE 15 – OUTPUT IMPEDANCE TEST CIRCUIT

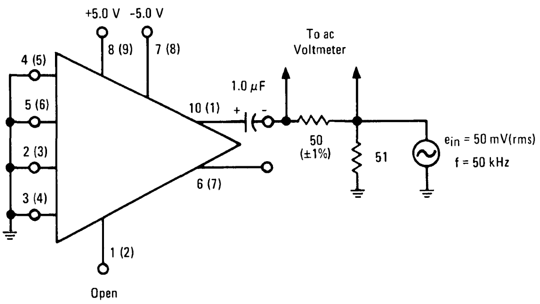


FIGURE 16 – INPUT BIAS CURRENT AND INPUT OFFSET CURRENT TEST CIRCUIT

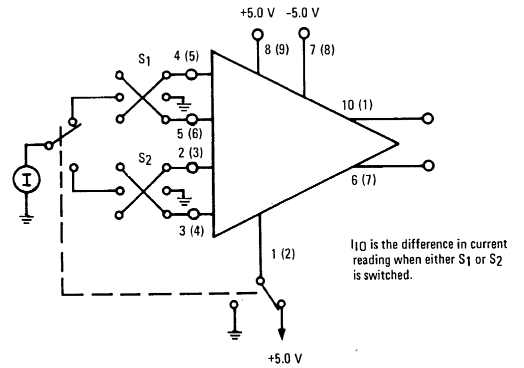


FIGURE 17 – INPUT OFFSET VOLTAGE AND QUIESCENT OUTPUT LEVEL TEST CIRCUIT

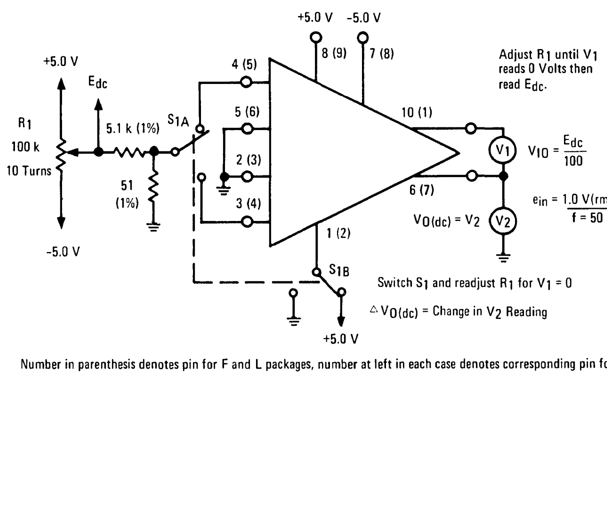
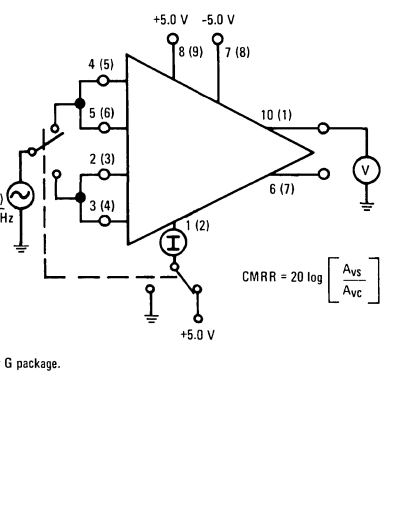
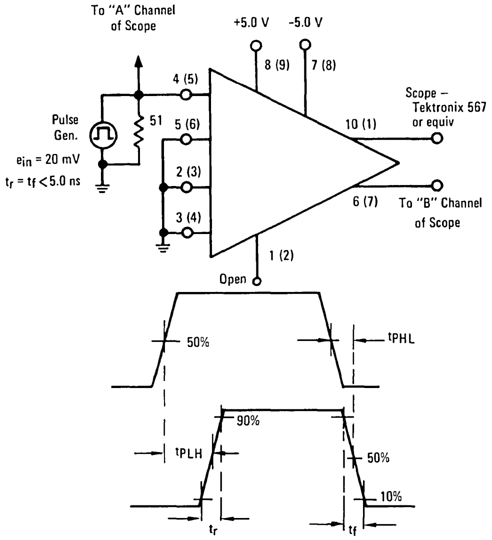


FIGURE 18 – GATE CURRENT (HIGH AND LOW), COMMON-MODE REJECTION AND COMMON-MODE INPUT RANGE TEST CIRCUIT



Number in parenthesis denotes pin for F and L packages, number at left in each case denotes corresponding pin for G package.

FIGURE 19 – PROPAGATION DELAY AND RISE AND FALL TIMES TEST CIRCUIT



Number in parenthesis denotes pin for F and L packages, number at left in each case denotes corresponding pin for G package.

FIGURE 20 – POWER DISSIPATION AND WIDEBAND INPUT NOISE TEST CIRCUIT

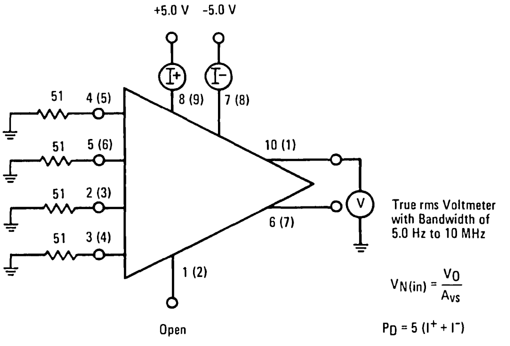
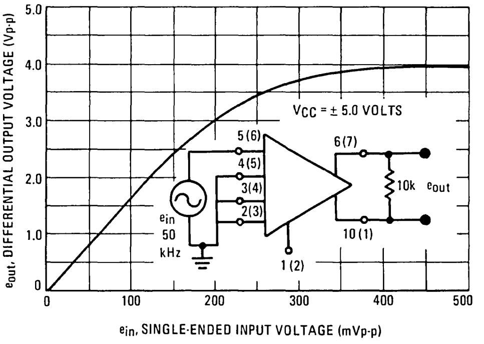


FIGURE 21 – LIMITING CHARACTERISTIC



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MC1546L
MC1446L

SENSE AMPLIFIERS

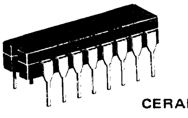
FOUR-CHANNEL PLATED-WIRE SENSE AMPLIFIER

. . . a sense amplifier designed to convert positive or negative 3.0 mV signals from plated-wire memories to transistor-transistor logic levels (MTTL). The problems encountered with ac-coupled plated-wire sense amplifiers are eliminated with this direct-coupled sense amplifier.

- Positive or Negative 3.0 mV Signal to Any of Four Input Channels Produces a Logic 1 or 0 Output (MC1446 – Positive or Negative 4.0 mV).
- Low Input Offset Voltages Apply to All Four Channels – 0.5 mV typ
- Wired "OR" Capability at Amplifier Output Results in Fewer Associated Circuits
- 2 by 4 Internal Decoder Simplifies Channel Selection
- Fast Recovery Time from Overload Signals – 40 ns typ
- Good Isolation Between ON and OFF Channels
- Channel Select and Strobe Operate from Standard MTTL Levels

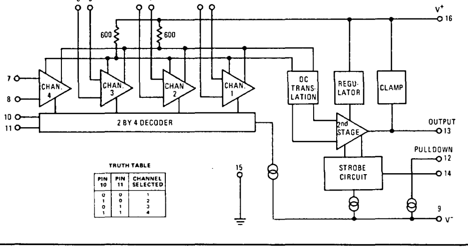
FOUR-CHANNEL PLATED-WIRE SENSE AMPLIFIER

MONOLITHIC SILICON EPITAXIAL PASSIVATED INTEGRATED CIRCUIT



CERAMIC PACKAGE
CASE 620

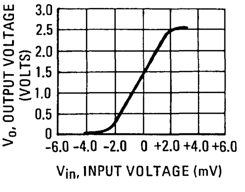
BLOCK DIAGRAM



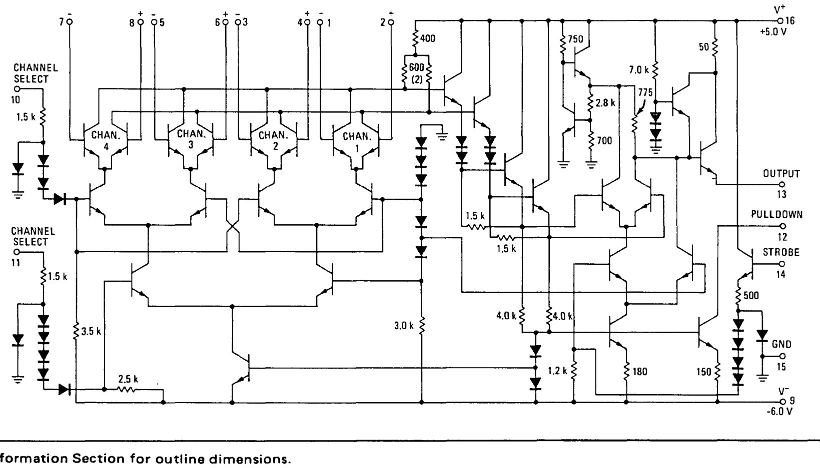
TRUTH TABLE

PIN 10	PIN 11	CHANNEL SELECTED
0	0	1
1	0	2
0	1	3
1	1	4

TRANSFER CHARACTERISTICS



CIRCUIT SCHEMATIC



See Packaging Information Section for outline dimensions.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating		Symbol	Value	Unit
Power Supply Voltage		V^+ V^-	+10 -10	Vdc
Differential Input Signal		V_{in}	±5.0	Volts
Common-Mode Input		CMV_{in}	±5.0	Volts
Output Current		I_{out}	25	mA
Power Dissipation (Package Limitation) Ceramic Package Derate above T_A = +25°C		P_D	 575 3.85	 mW mW/°C
Operating Temperature Range	MC1546L MC1446L	T_A	-55 to +125 0 to +75	°C
Storage Temperature Range	MC1546L MC1446L	T_{stg}	-65 to +175 -55 to +125	°C

ELECTRICAL CHARACTERISTICS
(V^+ = +5.0 Vdc ±1%, V^- = -6.0 Vdc ±1%, T_A = +25°C unless otherwise noted)

Characteristic	Fig.	Symbol	MC1546L			MC1446L			Unit
			Min	Typ	Max	Min	Typ	Max	
Voltage Gain	1	A_V	–	600	–	–	600	–	–
Output Voltage Level MC1546, MC1446 $T_A = T_{low}$* to T_{high}* { e_{in} = 0, 0 e_{in} = +3.0, +4.0 mV e_{in} = -3.0, -4.0 mV	2	V_o	 0.8 2.0 –	 1.4 – –	 2.0 – 0.4	 0.4 2.0 –	 1.4 – –	 2.4 – 0.4	Vdc
Input Bias Current	3	I_b	–	15	40	–	15	60	µA
Input Offset Current	3	I_{io}	–	0.1	2.0	–	0.1	4.0	µA
Channel Select Current High Level Low Level	4	 I_{CH} I_{CL}	 – –	 1.7 0.5	 2.4 0.9	 – –	 1.7 0.5	 2.6 1.0	mA
Channel Select Voltage High Level Low Level	5	 V_{CH} V_{CL}	 2.0 –	 – –	 – 0.8	 2.0 –	 – –	 – 0.8	Volts
Strobe Voltage High Level Low Level	5	 V_{SH} V_{SL}	 2.0 –	 – –	 – 0.8	 2.0 –	 – –	 – 0.8	Volts
Strobe Input Current	4	I_S	–	30	100	–	30	150	µA
Output Source Current	6	I_{o+}	5.0	8.0	–	4.0	8.0	–	mA
Output Sink Current	6	I_{o-}	-3.0	-4.0	–	-2.5	-4.0	–	mA
Positive Supply Current	6	I^+	–	19	25	–	19	27	mA
Negative Supply Current	6	I^-	–	-17	-22	–	-17	-24	mA
Input Common-Mode Voltage Range Channel Selected Channels Not Selected	7	$CMV_{(in)}$	 – – – –	 +2.7 -1.0 +2.7 -6.0	 – – – –	 – – – –	 +2.7 -1.0 +2.7 -6.0	 – – – –	Volts
Input Differential-Mode Voltage Range Channel Selected Channels Not Selected	7	$DMV_{(in)}$	 – –	 ±0.5 ±2.0	 – –	 – –	 ±0.5 ±2.0	 – –	Volts

*T_{low} = -55°C for MC1546, 0°C for MC1446; T_{high} = +125°C for MC1546, +75°C for MC1446

SWITCHING CHARACTERISTICS

Propagation Delay Time	8	t_{pd}	10	14	18	–	14	–	ns
Output Rise or Fall Time	8	t_r or t_f	–	30	–	–	30	–	ns
Strobe Delay Time	9	t_{dS}	–	14	18	–	14	–	ns
Strobe Width (min)	9	$t_{S(min)}$	–	20	–	–	20	–	ns
Channel Select Time	10	t_{Csel}	–	14	18	–	14	–	ns
Common-Mode Recovery Time (channel selected)	7	t_{CMR}	–	60	–	–	60	–	ns
Differential-Mode Recovery Time (channel selected)	8	t_{DMR}	–	40	–	–	40	–	ns

TEST CIRCUITS

FIGURE 1 – VOLTAGE GAIN

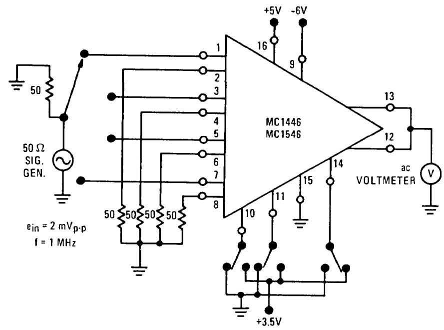


FIGURE 2 – OUTPUT DC LEVELS

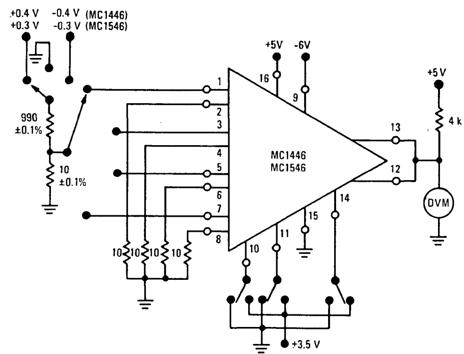


FIGURE 3 – INPUT CURRENTS

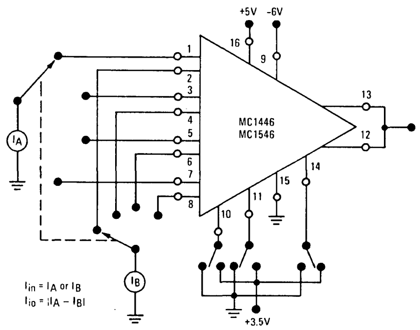


FIGURE 4 – CHANNEL SELECT AND STROBE INPUT CURRENTS

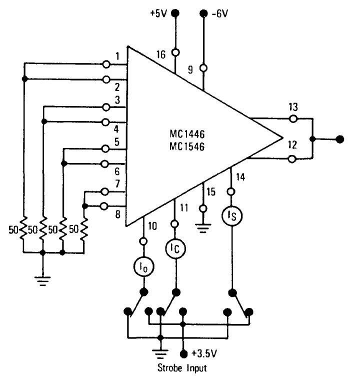


FIGURE 5 – CHANNEL SELECT TRANSFER CHARACTERISTICS

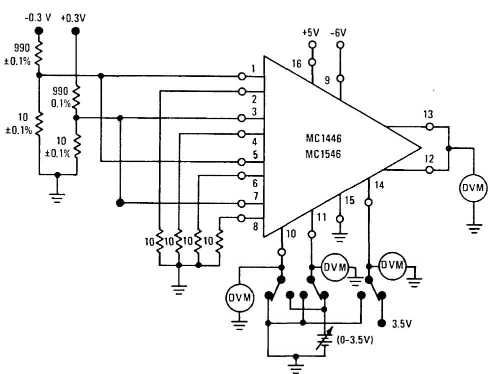


FIGURE 6 – OUTPUT CURRENTS

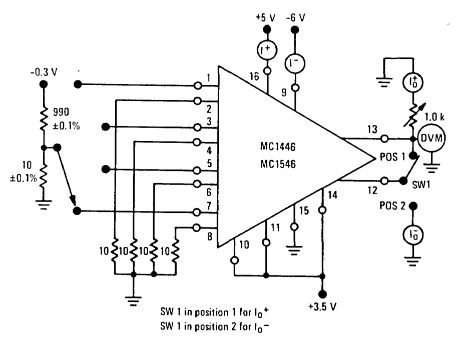


FIGURE 7 – INPUT COMMON-MODE CHARACTERISTICS

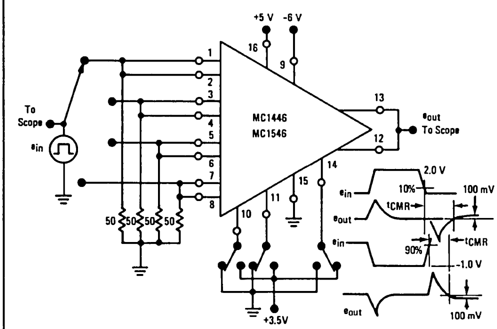


FIGURE 8 – CIRCUIT PROPAGATION DELAY, OUTPUT RISE AND FALL TIMES, AND DIFFERENTIAL-MODE RECOVERY TIME

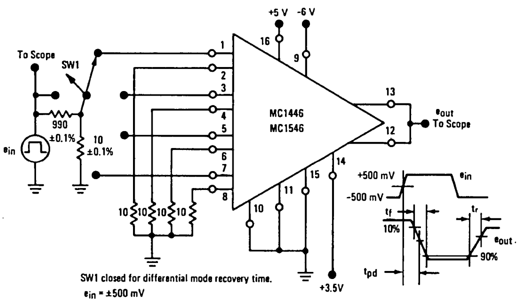


FIGURE 9 – STROBE CHARACTERISTICS

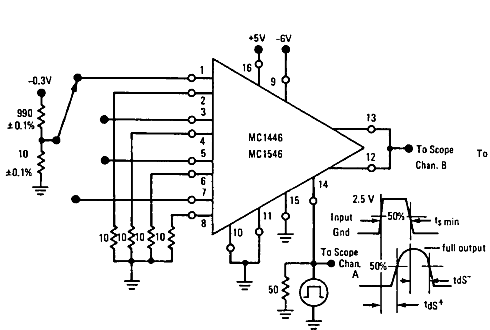
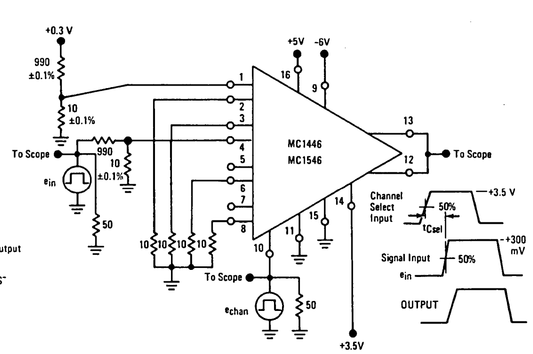


FIGURE 10 – CHANNEL SELECT TIME



6

TYPICAL RECOVERY TIME WAVEFORMS

FIGURE 11 – COMMON-MODE RECOVERY TIME

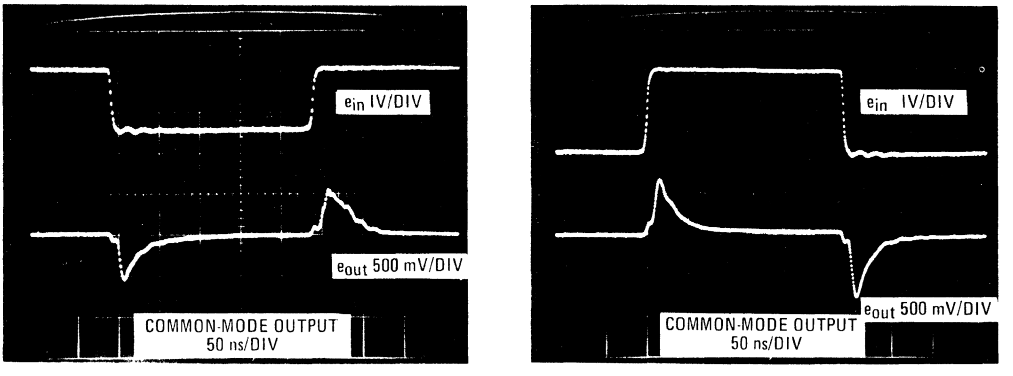


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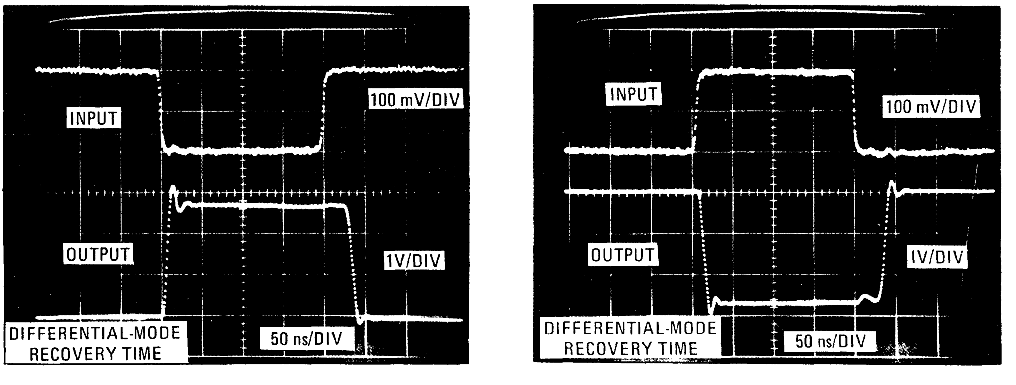
FIGURE 12 – DIFFERENTIAL-MODE RECOVERY TIME



TYPICAL CHARACTERISTICS

(T_A = +25°C unless otherwise noted)

FIGURE 13 – VOLTAGE GAIN versus TEMPERATURE

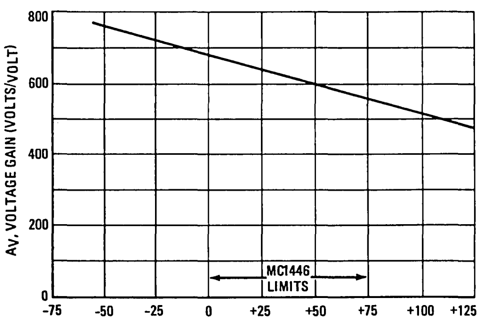


FIGURE 14 – DC OUTPUT VOLTAGE LEVEL versus TEMPERATURE (All Inputs Grounded)

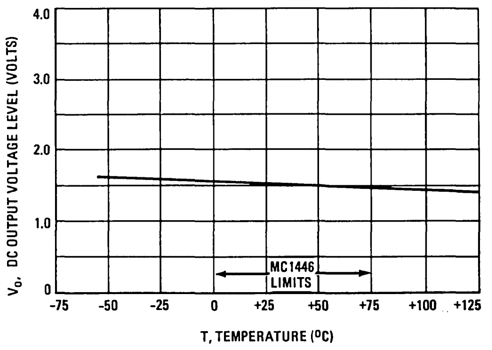


FIGURE 15 – AMPLIFIER TRANSFER CHARACTERISTICS

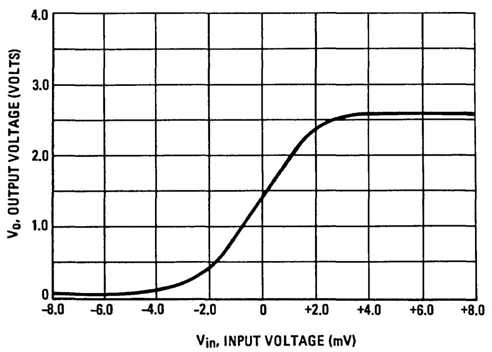


FIGURE 16 – CHANNEL SELECT versus OUTPUT TRANSFER CHARACTERISTICS

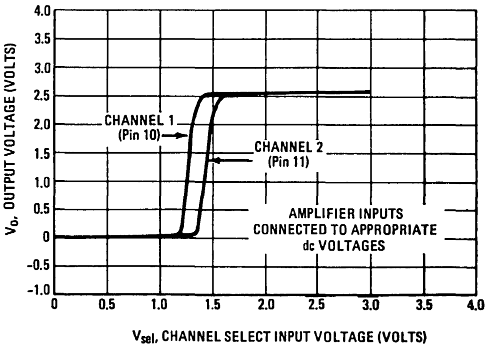


FIGURE 17 – STROBE INPUT TRANSFER CHARACTERISTICS (Input High)

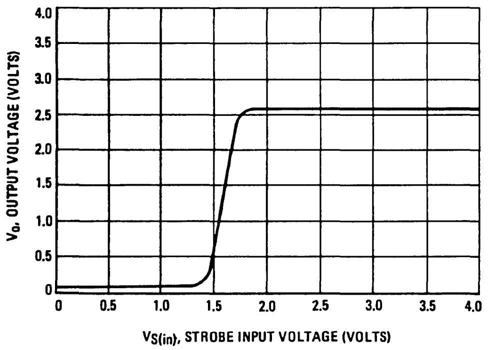
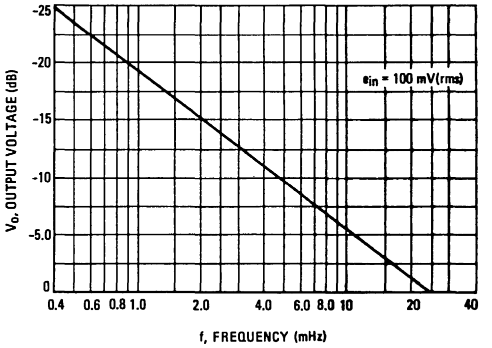


FIGURE 18 – COMMON-MODE GAIN versus FREQUENCY



TYPICAL CHARACTERISTICS (continued)

FIGURE 19 — VOLTAGE GAIN versus FREQUENCY

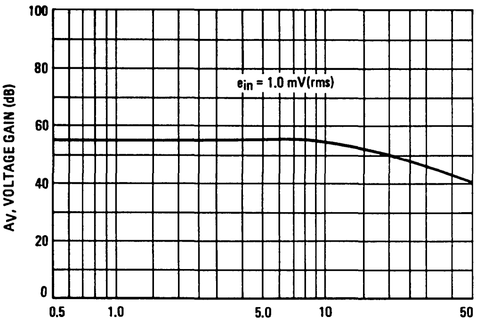
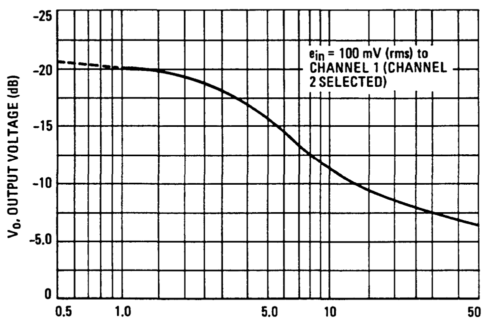


FIGURE 20 — ADJACENT CHANNEL ISOLATION versus FREQUENCY



CIRCUIT DESCRIPTION OF THE MC1546L/MC1446L

The MC1546L/MC1446L was designed to translate a positive 3.0 mV signal from a plated wire memory to an MTTL "1" level, or a negative 3.0 mV to an MTTL "0" level. This sense amplifier also eliminates the requirement for a bipolar switch in series with the plated wire because the bit selection is done inside the sense amplifier.

The circuit operation can be described in sections as follows:

1. All channels have been designed for low input offsets — 0.5 V typical.
2. Channel "ORing" is accomplished by using common collector load resistors for four differential amplifier pairs.
3. Channel selection is accomplished by current steering through the four differential pairs. The circuit below the four differential pairs forms a matrix tree which can be thought of as a 2-by-4 decode matrix. The bottom transistor is the current source for the first stage of gain.
4. DC translation between the first and second stages of gain is done through an emitter-follower stage, two diodes and another emitter follower for each side of the differential amplifier. The currents in these translator legs are combined and run through diodes to the negative supply. These diodes are used to bias both the first and second gain stages. This also gives the appropriate gain versus temperature and dc output level versus temperature characteristics.
5. The top of the second stage amplifier is regulated at a voltage equal to five diode drops above ground. It can be seen that if the 700 ohm resistor in the regulator has one diode (or V_{BE}) across it then the 2.8 k ohm resistor will have four diode drops across it. This makes a five diode drop voltage above ground that is fairly independent of the positive supply.
6. The current in the second stage of the amplifier is set by the 180-ohm resistor in the emitter of the current source. It can be seen that this resistor has one diode drop (approximately 750 mV) across it. Therefore, an analysis will show that the voltage drop across the 775-ohm load resistor in the second stage will be approximately two diodes when the differential amplifier is balanced. Accounting for the additional diode voltage drop of the emitter-follower output transistor will set the output dc level at two diodes above ground or very near the center of MTTL threshold.
7. The strobe circuit works by steering current in the second stage. When the strobe is low, the entire current of the second stage current source is steered through the 775-ohm load resistor. This clamps the output to a low state so that an input signal cannot cause an output. When the strobe is high, the current is steered through the second stage differential amplifier pair and the output will go to a level dictated by the presence of an input signal.
8. The output circuit of the sense amplifier may be thought of as a push-pull type. The emitter of the push transistor is brought out to a separate pin from the collector of the pull transistor. This will facilitate "Wire ORing" the outputs of several sense amplifiers. Several emitter outputs can be wired together along with only one collector pull-down transistor. The unused collectors of the pulldown transistor must be grounded. An example of the use of "Wire ORing" is to have four MC1546 devices wired-OR into a 16-channel sense amplifier in which a channel may be selected by selecting channels in parallel at the amplifier inputs and strobing the proper sense amplifier.

APPLICATIONS INFORMATION

The MC1546/MC1446 devices are designed to convert signals from plated-wire memories as small as positive or negative 3 mV to MTTL logic levels. The output level of the sense amplifier with no input signal present and with the strobe high is typically 1.4 volts (typical input threshold of MTTL logic). Hence, if the strobe goes high during the absence of an input signal from the plated-wire memory, the sense amplifier output will rise to 1.4 volts. This condition could cause false outputs; therefore careful considerations must be given to strobe timing. Figure 21 illustrates a typical timing sequence of the MC1546/MC1446 device as recommended for proper operation.

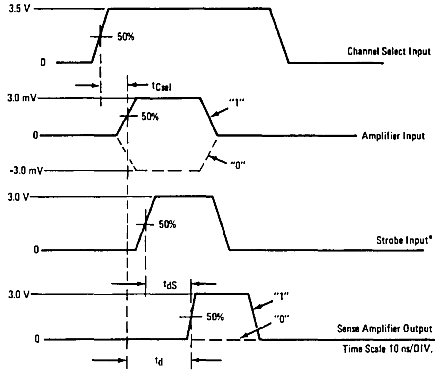
Figure 22 shows how these sense amplifiers are used in an N-word-line-by-32-bit basic memory plane organized as 4-N words of 8 bits each. During a read cycle, the read current is pulsed through a selected word-line and thus generates outputs to all of the 32-bit positions in the line. The internal one-of-four decoder selects the desired channels of the eight sense amplifiers for a particular system word. When the strobe goes high, the sense amplifier outputs switch according to the data present at the amplifier inputs. The data readout on the other 24-bit lines is not lost due to the Non-Destructive Read-Out properties of a plated-wire memory. On the next read cycle the decoder of the sense amplifier in combination with the selected word-line determines the 8-bits of data to read.

APPLICATIONS INFORMATION (continued)

Memory organizations that have more than four words per word-line require that the sense amplifier outputs be wired-OR. To wire-OR the outputs of several sense amplifiers all of the emitters of the output-pullup transistors are tied together. Only one collector of the pulldown transistors is tied to the wired-OR emitters of the pullup transistors. The remaining pulldown transistors must be grounded as noted in Figure 23. Ten or more sense amplifiers may be wired-OR together without any reduction in usable logic levels since only one sense amplifier per bit is on at any given time. Variations in propagation delay time (t_{pd}), versus the number of wired-OR sense amplifiers and the output capacitance are given in Figure 24.

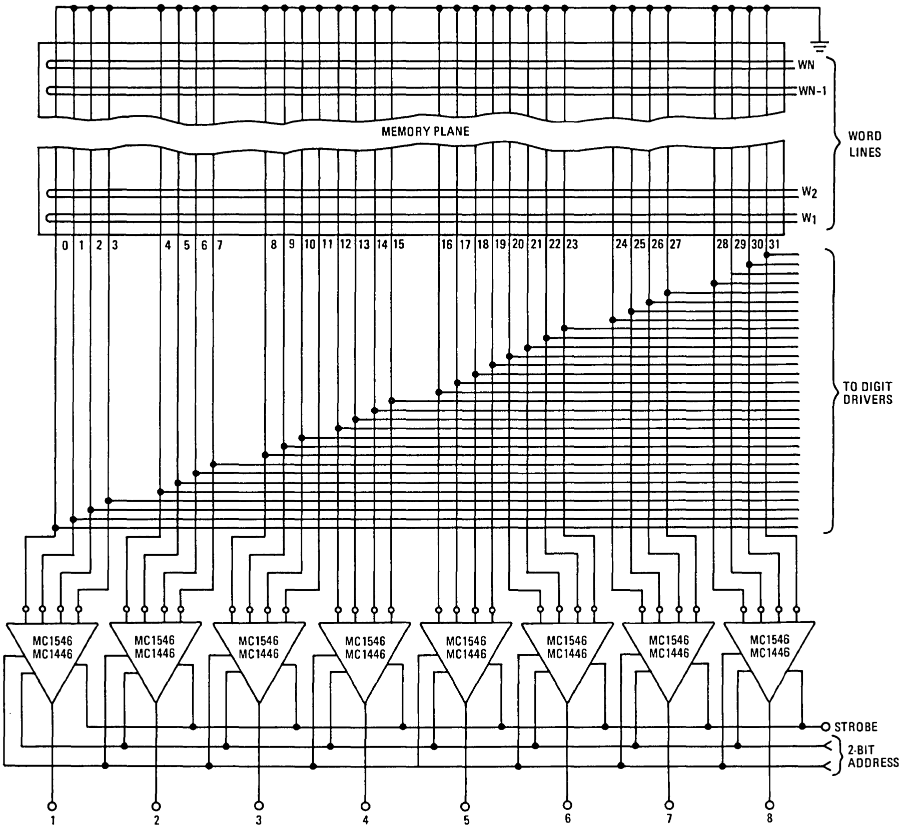
In Figure 25, eight are required for each bit of a 32-word/word-line memory. For those sense amplifiers that have wired-OR outputs, the strobe is used for decoding by attaching each strobe to a 3-bit-binary-to-1-of-8-bit decoder (MC4006). Thus only one sense amplifier per bit can be strobed at a given time. High fan-out gates are required on the channel select lines since a high current must be supplied to the select lines to drive them to the logic "1" level. The strobe current is low, thereby allowing many strobe lines to be driven with only one gate.

FIGURE 21 – TYPICAL TIMING SEQUENCE OF THE MC1546/MC1446



*The strobe pulse width is smaller than the amplifier input pulse width.

FIGURE 22 – N-WORD-LINE-BY-32-BIT MEMORY PLANE ORGANIZED AS 4-N WORDS OF 8 BITS EACH



APPLICATIONS INFORMATION (continued)

FIGURE 23 – WIRED "OR" MC1546/MC1446 DEVICES

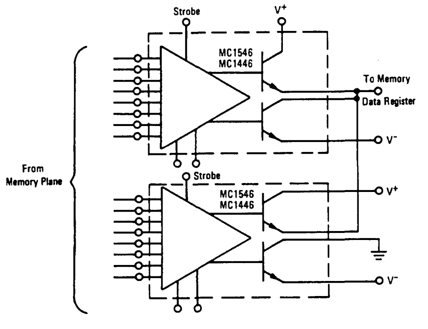


FIGURE 24 – TYPICAL PROPAGATION DELAY TIME VARIATION
(per number of devices at stated capacitance)

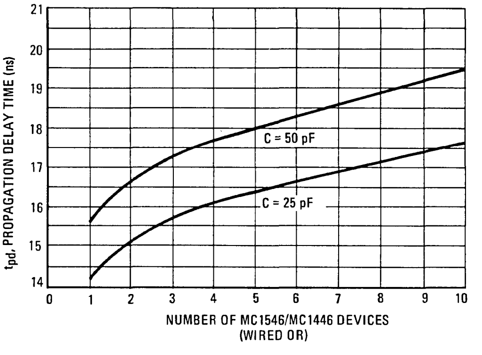
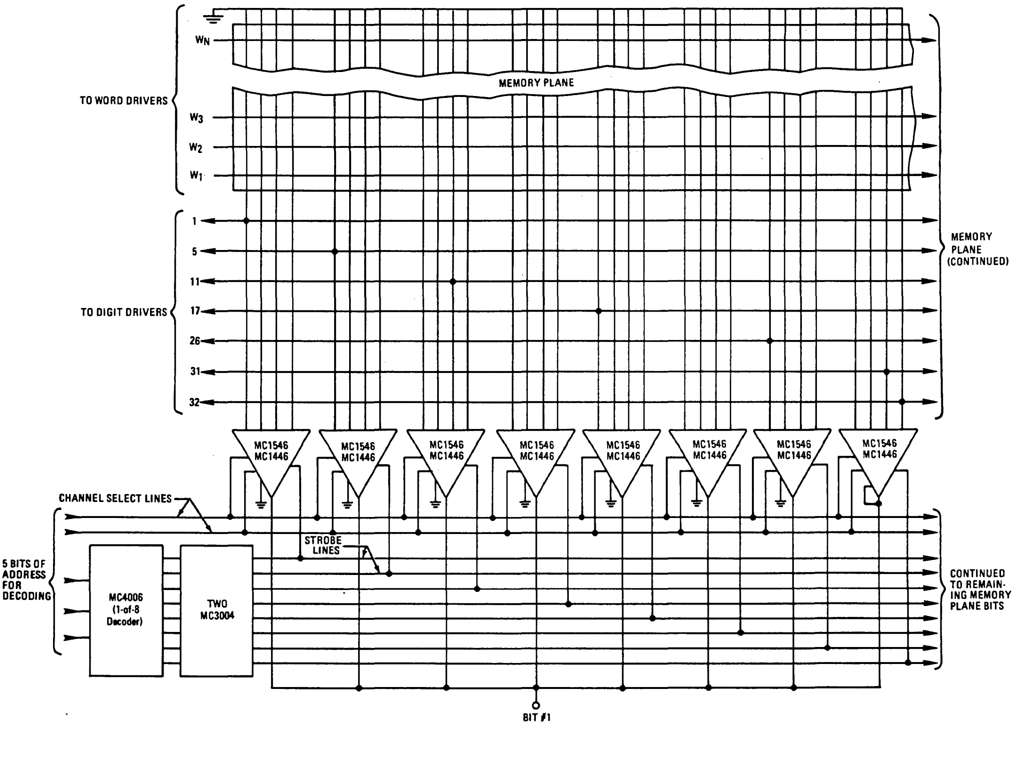


FIGURE 25 – 32 WORDS/WORD - LINE ORGANIZED MEMORY



DEFINITIONS

A_V — the voltage gain from a channel input to amplifier output (input signal is 2 mV peak-to-peak and the strobe is high)

CMV_{in} — maximum input common-mode voltage on any channel that will not cause the amplifier to saturate

DMV_{in} — maximum input differential-mode voltage on any channel signal that will not saturate the amplifier

I^+ — current from the positive supply with no load (pin 12 shorted to pin 13)

I^- — current into the negative supply with both channel select pins at +3.5 volts

I_b — input current into the base of any input transistor when the opposite transistor of the differential pair is at the same voltage

I_{CH} — input current at channel select pin when the channel select voltage is at V_{CH}

I_{CL} — input current at channel select pin when the channel select voltage is at V_{CL}

I_{io} — difference between base currents of any input differential pair of transistors

I_{o+} — output source current to a load with the output remaining above 2.4 volts, excluding the amplifier's own sink current

I_{o-} — the current that the amplifier will sink into pin 12

t_{CMR} — time required for the amplifier to recover from the maximum specified common-mode input, (recovery – output within 10% of its quiescent state)

$t_{C\,sel}$ — time between the 50% point of the channel gate input and the 50% point of the signal input that still allows a full width signal at the amplifier output

t_{DMR} — time required for the amplifier to recover from maximum specified differential-mode input, (recovery – output within 10% of its quiescent state)

t_{dS} — delay time from the 50% point of the strobe input leading or trailing edge to the corresponding 50% point of the output

t_f — time rise (and time fall) of the input signal must be less than 10 ns

t_{pd} — the delay time from the 50% point of a 5.0 mV input leading or trailing edge to the corresponding 50% point of the amplifier output

t_r — time from 10% to 90% of the rise and fall times respectively of the output signal with a 5.0 mV input signal

t_{Smin} — minimum pulse width at 50% points at strobe input allows a full output (pulse rise times of less than 10 ns, amplifier differential input equal to 3 mV)

V_{CH} — minimum voltage required at the channel select pin to cause a given channel to give 99% of the maximum gain through the amplifier

V_{CL} — maximum voltage allowable at the channel select pin to cause a given channel to give 1% or less of the gain when channel is fully selected

V_o — output dc level with inputs grounded and strobe high

V_{OH} — minimum output high level

V_{OL} — maximum output low level

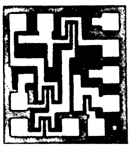
V_{SH} — the minimum voltage required at the strobe pin to allow 99% of a full output

V_{SL} — the maximum voltage allowable at the strobe pin to allow 1% or less of a full output

MC1550

HIGH-FREQUENCY CIRCUITS

INTEGRATED CIRCUIT LINEAR AMPLIFIER

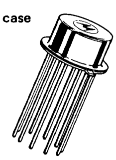


. . . a versatile, common-emitter, common base cascode circuit for use in communications applications. See Application Notes AN-215, AN-247 and AN-299 for additional information.

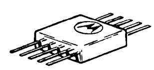
- Constant Input Impedance over entire AGC range
- Extremely Low y_{12} – 4.3 μmhos at 60 MHz
- High Power Gain – 30 dB @ 60 MHz (0.5 MHz BW)
- Good Noise Figure – 5 dB @ 60 MHz

RF – IF AMPLIFIER
INTEGRATED CIRCUIT
MONOLITHIC SILICON
EPITAXIAL PASSIVATED

Pin 7 connected to case



G SUFFIX
METAL PACKAGE
CASE 602B

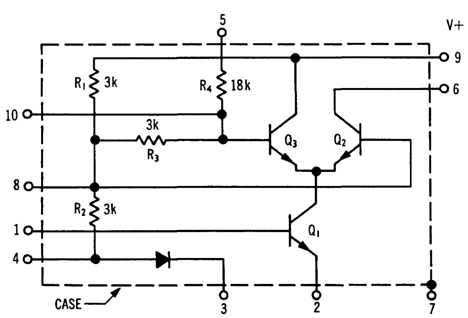


F SUFFIX
CERAMIC PACKAGE
CASE 606
TO-91

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage, Pin 9	V+	20	Vdc
AGC Supply Voltage	V_{AGC}	20	Vdc
Differential Input Voltage, Pin 1 to Pin 4 (R_S = 500 ohms)	V_{in}	±5.0	V(rms)
Power Dissipation (Package Limitation)	P_D		
Metal Can		680	mW
Derate above T_A = +25°C		4.6	mW/°C
Flat Package		500	mW
Derate above T_A = +25°C		3.3	mW/°C
Operating Temperature Range	T_A	-55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

CIRCUIT SCHEMATIC



CIRCUIT DESCRIPTION

The MC1550 is built with monolithic fabrication techniques utilizing diffused resistors and small-geometry transistors. Excellent AGC performance is obtained by shunting the signal through the AGC transistor Q_3 maintaining the operating point of the input transistor Q_1. This keeps the input impedance constant over the entire AGC range.

The amplifier is intended to be used in a common-emitter, common-base configuration (Q_1 and Q_2) with Q_3 acting as an AGC transistor. The input signal is applied between pins 1 and 4, where pin 4 is ac-coupled to ground. DC source resistance between pins 1 and 4 should be small (less than 100 ohms). Pins 2 and 3 should be connected together and grounded. Pins 8 and 10 should be bypassed to ground. The positive supply voltage is applied at pin 9 and at higher frequencies, pin 9 should also be bypassed to ground. The output is taken between pins 6 and 9. The substrate is connected to pin 7 and should be grounded. AGC voltage is applied to pin 5.

See Packaging Information Section for outline dimensions.

ELECTRICAL CHARACTERISTICS ($V^+ = +6$ Vdc, $T_A = +25^\circ C$)

Characteristic	Conditions	Figure	Symbol	Min	Typ	Max	Unit
DC CHARACTERISTICS							
Output Voltage	V_{AGC} = 0 Vdc V_{AGC} = +6 Vdc	1	V_O	3.80 5.90	– –	4.65 6.00	Vdc
Test Voltage	V_{AGC} = 0 Vdc V_{AGC} = +6 Vdc	1	V8	2.85 3.25	– –	3.40 3.80	Vdc
Supply Drain Current	V_{AGC} = 0 Vdc V_{AGC} = +6 Vdc	1	I_D	– –	– –	2.2 2.5	mAdc
AGC Supply Drain Current	V_{AGC} = 0 Vdc V_{AGC} = +6 Vdc	1	I_{AGC}	– –	– –	-0.2 0.18	mAdc
SMALL-SIGNAL CHARACTERISTICS							
Small-Signal Voltage Gain	f = 500 kHz	2	A_V	22	–	29	dB
Bandwidth	-3.0 dB	2	BW	22	–	–	MHz
Transducer Power Gain	f = 60 MHz, BW = 6 MHz f = 100 MHz, BW = 6 MHz	3	Ap	– –	25 21	– –	dB

TYPICAL CHARACTERISTICS

($V^+ = 6.0$ Vdc, $T_A = +25^\circ C$ unless otherwise noted)

FIGURE 1 – DC CHARACTERISTICS TEST CIRCUIT

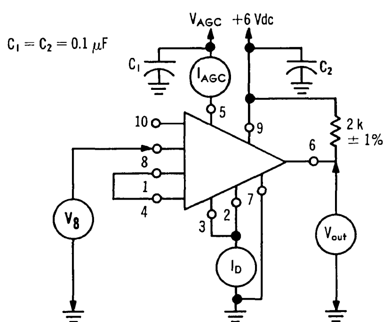


FIGURE 2 – VOLTAGE GAIN AND BANDWIDTH TEST CIRCUIT

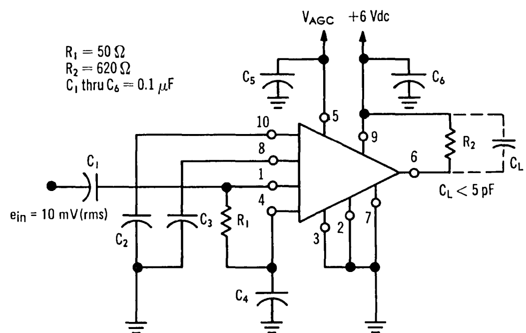


FIGURE 3 – POWER GAIN TEST CIRCUIT @ 60 MHz

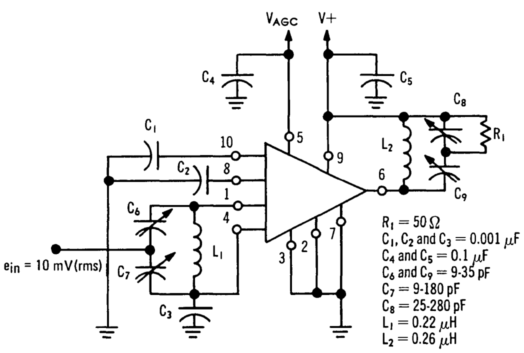
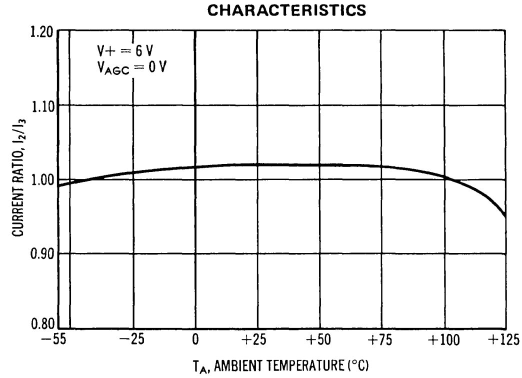


FIGURE 4 – DRAIN CURRENT TEMPERATURE CHARACTERISTICS



TYPICAL CHARACTERISTICS (continued)

FIGURE 5 – INPUT RESISTANCE AND CAPACITANCE versus FREQUENCY

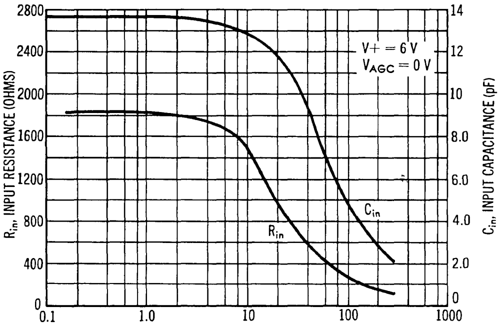


FIGURE 6 – INPUT RESISTANCE AND CAPACITANCE versus AGC VOLTAGE

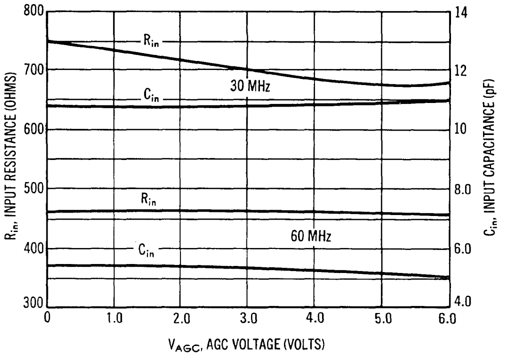


FIGURE 7 – OUTPUT RESISTANCE AND CAPACITANCE versus FREQUENCY

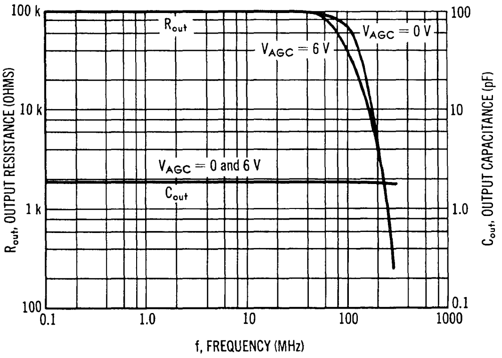


FIGURE 8 – OUTPUT RESISTANCE AND CAPACITANCE versus AGC VOLTAGE

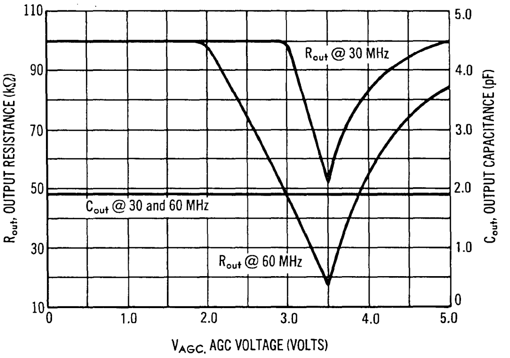


FIGURE 9 – MAXIMUM TRANSDUCER POWER GAIN versus FREQUENCY

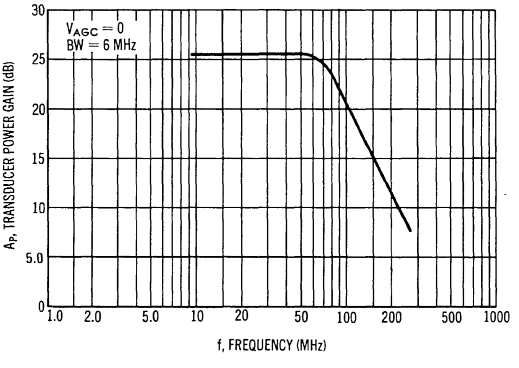
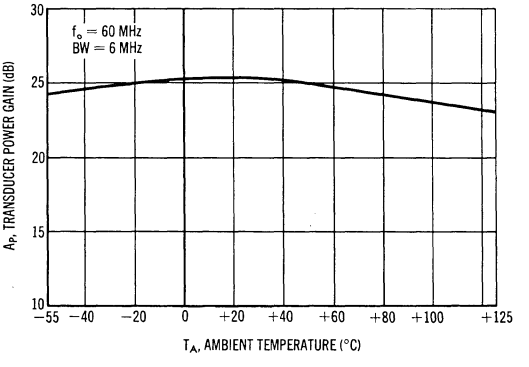


FIGURE 10 – TRANSDUCER POWER GAIN versus TEMPERATURE



6

TYPICAL CHARACTERISTICS (continued)

FIGURE 11 – TRANSDUCER POWER BANDWIDTH versus AGC VOLTAGE

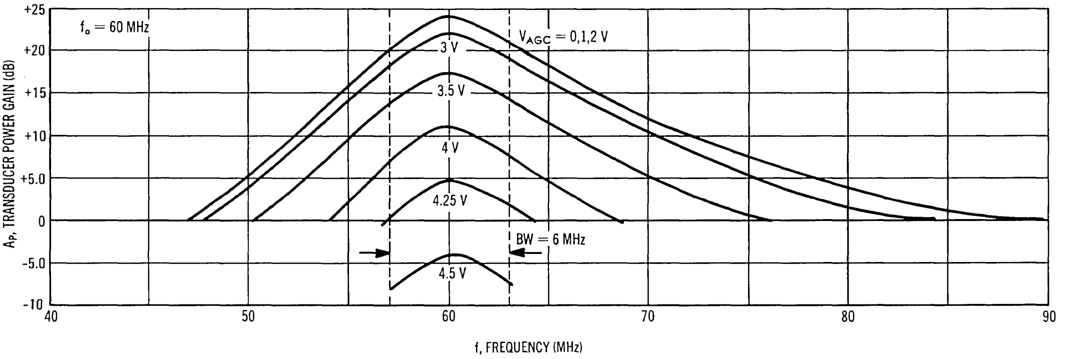


FIGURE 12 – NOISE FIGURE AND OPTIMUM SOURCE RESISTANCE versus FREQUENCY

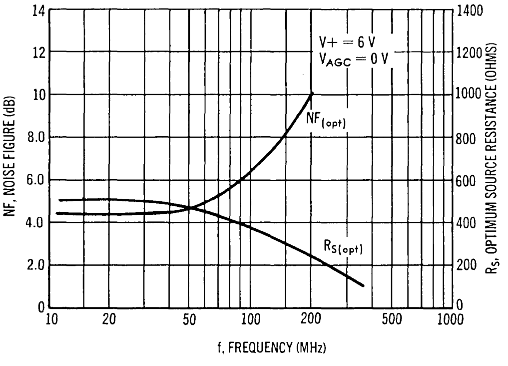


FIGURE 13 – NOISE FIGURE versus SOURCE RESISTANCE

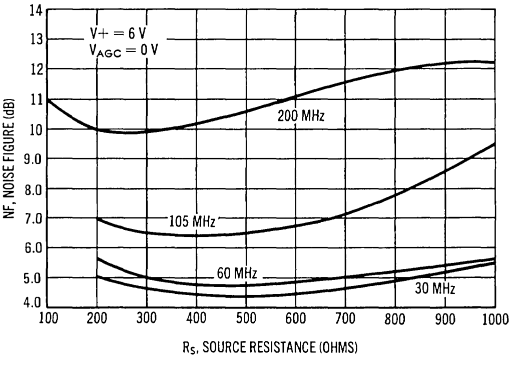


FIGURE 14 – y_{21}, FORWARD-TRANSFER ADMITTANCE versus FREQUENCY

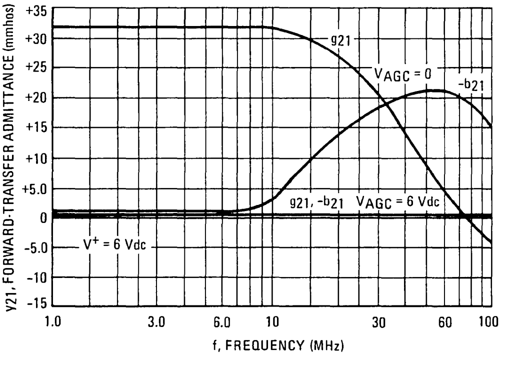
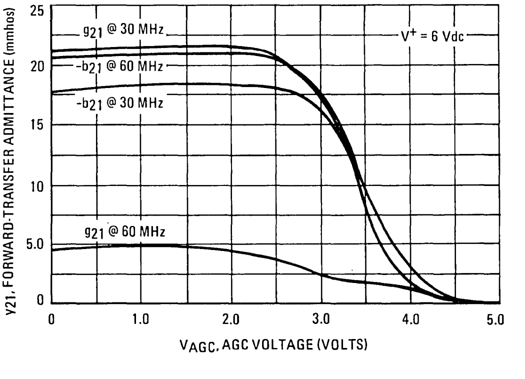


FIGURE 15 – y_{21}, FORWARD-TRANSFER ADMITTANCE versus AGC VOLTAGE



TYPICAL CHARACTERISTICS

($V^+ = 6.0$ Vdc, $T_A = +25^oC$ unless otherwise noted)

FIGURE 16 – y_{12}, REVERSE TRANSFER-ADMITTANCE versus FREQUENCY

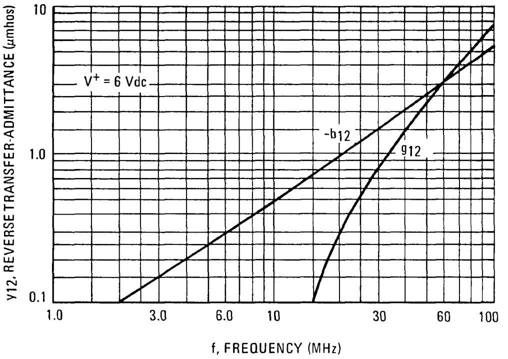
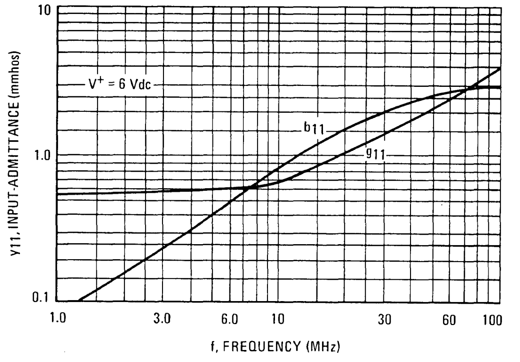


FIGURE 17 – y_{11}, INPUT-ADMITTANCE versus FREQUENCY



The y_{12} shown in Figure 16 illustrates the extremely low feedback of the MC1550 with no contribution from the external mounting circuitry. However, in many cases the external circuitry may contribute as much or more to the total feedback than does the MC1550.

To perform more accurate design calculations of gain, stability, and input - output impedances it is recommended that the designer first determine the total feedback of device plus circuitry.

This can be done in one of two ways:

(1) Measure the total y_{12} or s_{12} of the MC1550 installed in its mounting circuitry, or

(2) Measure the y_{12} of the circuitry alone (without the MC1550 installed) and add the circuit y_{12} to the y_{12} for the MC1550 given in Figure 16.

FIGURE 19 – s_{11} AND s_{22}, INPUT AND OUTPUT REFLECTION COEFFICIENT

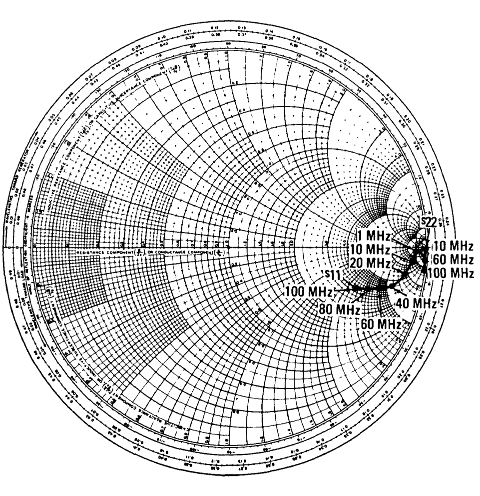
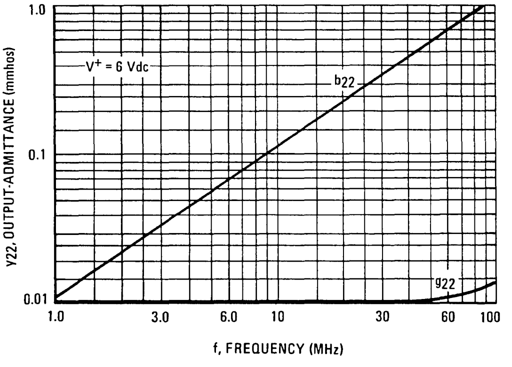


FIGURE 18 – y_{22}, OUTPUT-ADMITTANCE versus FREQUENCY



TYPICAL CHARACTERISTICS (continued)

(V^+ = 6.0 Vdc, T_A = +25°C unless otherwise noted)

FIGURE 20 – s_{11}, INPUT REFLECTION COEFFICIENT versus FREQUENCY

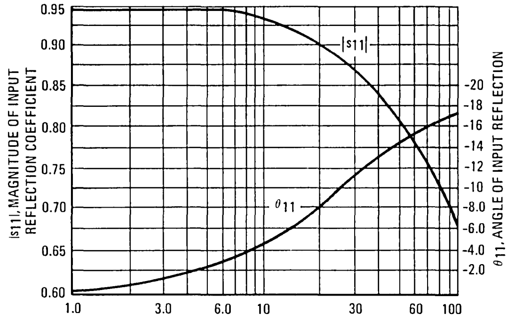


FIGURE 21 – s_{22}, OUTPUT REFLECTION COEFFICIENT versus FREQUENCY

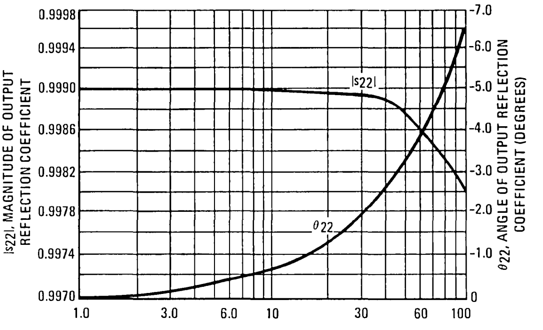


FIGURE 22 – s_{21}, FORWARD TRANSMISSION COEFFICIENT (GAIN)

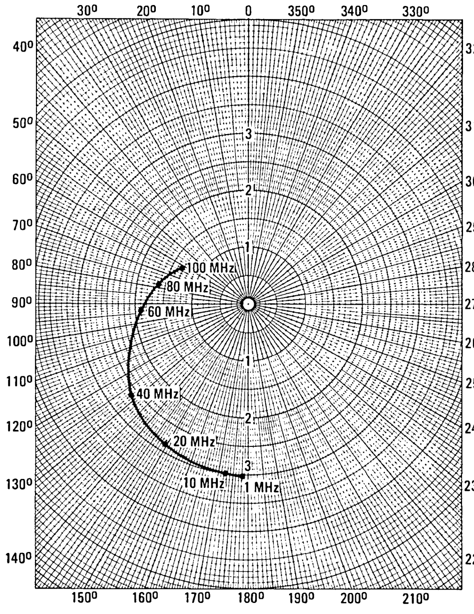
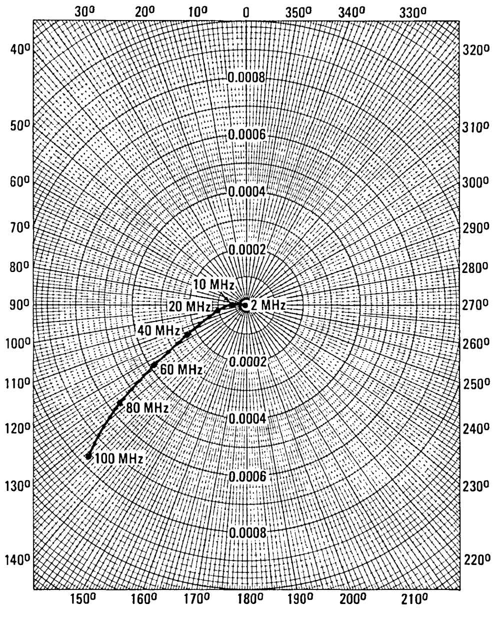


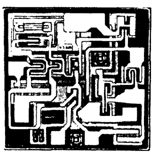
FIGURE 23 – s_{12}, REVERSE TRANSMISSION COEFFICIENT (FEEDBACK)



6

MC1552G
MC1553G

MONOLITHIC VIDEO AMPLIFIER

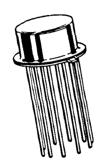


. . . a three-stage, direct-coupled, common-emitter cascade incorporating series-series feedback to achieve stable voltage gain, low distortion, and wide bandwidth. Employs a temperature-compensated dc feedback loop to stabilize the operating point and a current-biased emitter follower output. Intended for use as either a wide-band linear amplifier or as a fast rise pulse amplifier.

- High Gain – 34 dB ± 1 dB (MC1552)
  52 dB ± 1 dB (MC1553)
- Wide Bandwidth – 40 MHz (MC1552)
  35 MHz (MC1553)
- Low Distortion – 0.2% at 200 kHz
- Low Temperature Drift – ±0.002 dB/°C

HIGH FREQUENCY INTEGRATED CIRCUITS

SILICON EPITAXIAL PASSIVATED



METAL PACKAGE
CASE 602B

Pin 6 connected to case

MAXIMUM RATINGS ($T_A = +25°C$ unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage, Pin 9	V^+	9	Vdc
Input Voltage, Pin 1 to Pin 2 (R_S = 500 ohms)	V_{in}	1.0	V(rms)
Power Dissipation (Package Limitation) Derate above T_A = +25°C	P_D	680 4.6	mW mW/°C
Operating Temperature Range	T_A	-55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

CIRCUIT SCHEMATICS

FIGURE 1 – MC1552 (LOW GAIN)

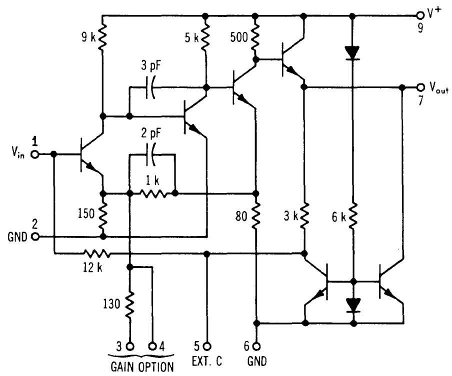
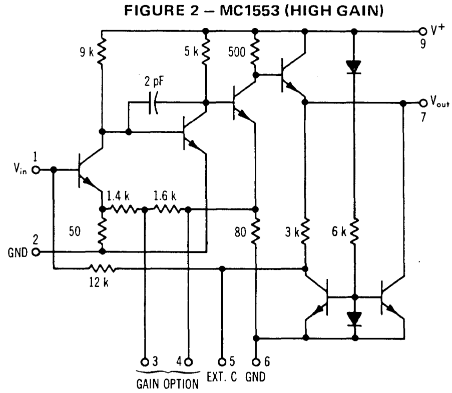


FIGURE 2 – MC1553 (HIGH GAIN)



See Packaging Information Section for outline dimensions.

ELECTRICAL CHARACTERISTICS ($V^+ = +6$ Vdc, $T_A = +25°C$ unless otherwise noted)

Characteristic		Fig. No.	Gain Option*	Symbol	Min	Typ	Max	Unit
Voltage Gain	MC1552	3	50 100	V_{out}/V_{in}	44 87	50 100	56 113	V/V
	MC1553		200 400		175 350	200 400	225 450	
Voltage Gain Variation (T_A = -55°C to +125°C)		3	All	—	—	±0.2	—	dB
Bandwidth	MC1552	3,6	50 100	BW	21 17	40 35	— —	MHz
	MC1553		200 400		17 7.5	35 15	— —	
Input Impedance (f = 100 kHz, R_L = 1 kΩ)		—	All	$\|Z_{in}\|$	7	10	—	kΩ
Output Impedance (f = 100 kHz, R_S = 50 Ω)		—	All	$\|Z_{out}\|$	—	16	50	Ω
DC Output Voltage		3	All	V_{out} (dc)	2.5	2.9	3.2	Vdc
DC Output Voltage Variation (T_A = -55°C to +125°C)		3	All	ΔV_{out} (dc)	—	±0.05	—	Vdc
Output Voltage Swing ($Z_L \geq$ 1 kΩ, V_{in} = 100 mV[rms])		3	All	V_{out}	3.6	4.2	—	Vp-p
Power Dissipation		—	All	P_D	—	75	120	mW
Delay Time	MC1552	3,4	50 100	t_{pd}	— —	8 9	— —	ns
	MC1553		200 400		— —	10 25	— —	
Rise Time	MC1552	3,4	50 100	t_r	— —	9 12	16 20	ns
	MC1553		200 400		— —	11 30	20 45	
Overshoot		3,4	All	$(V_{os}/V_p)100$	—	5	—	%
Noise Figure (R_S = 400 Ω, f_o = 30 MHz, BW = 3 MHz)		—	All	NF	—	5	—	dB
Total Harmonic Distortion (V_{out} = 2 Vp-p, f = 200 kHz, R_L = 1 kΩ)		—	All	THD	—	0.2	—	%

*To obtain the voltage-gain characteristic desired, use the following pin connections:

Type	Voltage Gain	Pin Connections
MC1552	50	Pin 3 Open
	100	Ground Pin 3
MC1553	200	Connect Pin 3 to Pin 4
	400	Pins 3 and 4 Open

NOTES

1. Ground Pin 6 as close to can as possible to minimize overshoot. Best results by directly grounding can.
2. If large input and output coupling capacitors are used, place shield between them to avoid input-output coupling.
3. A high-frequency capacitor must always be used to bypass the power supply. This capacitor should be as close to the circuit as possible.
4. Voltage gain can be adjusted to any value between 50 and 3000 by connecting an external resistor from Pin 4 to ground on MC1552, or from Pin 3 to ground on MC1553, as shown in Figure 8. Under these conditions, the following equations must be used to determine C_1 and C_2 rather than the circuits shown in Figure 5.

Fig. 5b $C_1 = \frac{1}{2\pi f_c (1.7 \times 10^4)}$ Farads; $C_2 = 8\,C_1 (V_{out}/V_{in})$ Farads

Fig. 5c $C_1 = \frac{V_{out}/V_{in}}{2\pi f_c (1.5 \times 10^4)}$ Farads

Fig. 5d $C_2 = \frac{V_{out}/V_{in}}{2\pi f_c (3 \times 10^3)}$ Farads

FIGURE 3 — TEST CIRCUIT

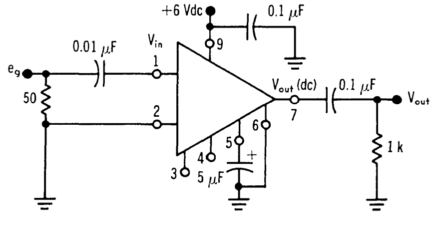
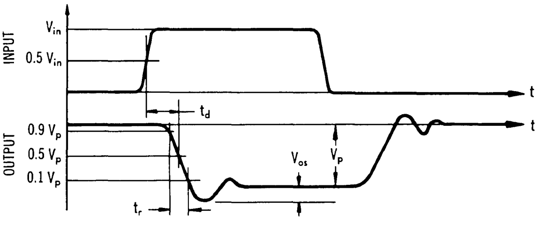


FIGURE 4 — PULSE RESPONSE DEFINITIONS



TYPICAL CHARACTERISTICS

$T_A = +25°C$

FIGURE 5a – FREQUENCY RESPONSE

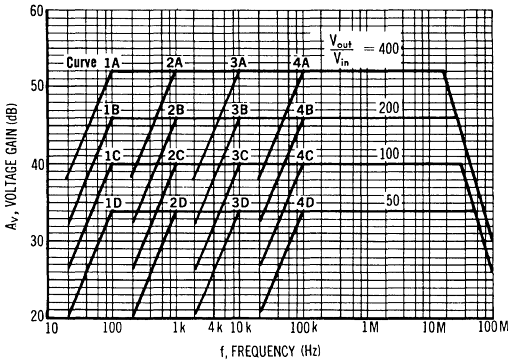
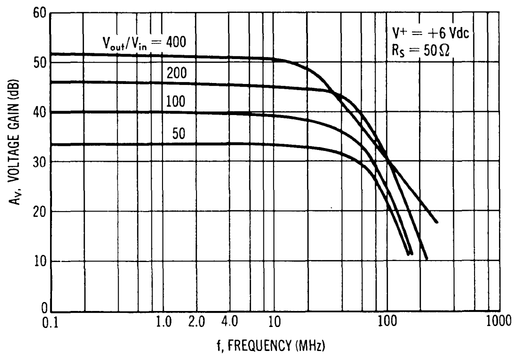
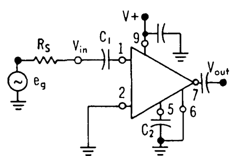


FIGURE 6 – VOLTAGE GAIN versus FREQUENCY



TEST CIRCUITS FOR FREQUENCY RESPONSE

FIGURE 5b – CAPACITIVE COUPLED INPUT (R_S < 5 kΩ)



Curve No.	C_1 (μF)	C_2 (μF)
1A	0.1	250
1B	0.1	150
1C	0.1	70
1D	0.1	40

Curve No.	C_1 (μF)	C_2 (μF)
2A	0.01	30
2B	0.01	18
2C	0.01	8.0
2D	0.01	4.0
	(pF)	
3A	1000	3.0
3B	1000	1.8
3C	1000	0.8
3D	1000	0.4
4A	100	0.3
4B	100	0.18
4C	100	0.08
4D	100	0.04

FIGURE 7 – MAXIMUM NEGATIVE SWING SLEW RATE versus LOAD CAPACITANCE

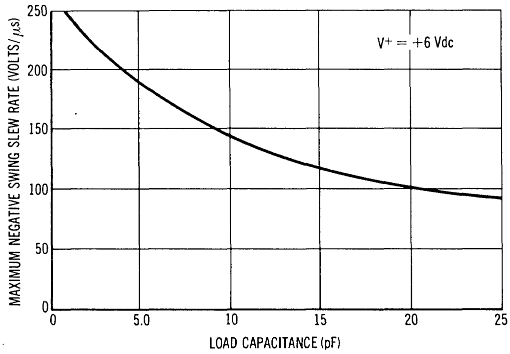
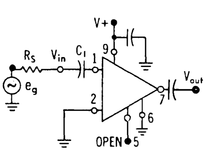


FIGURE 5c – CAPACITIVE COUPLED INPUT (R_S < 500 Ω)



Curve No.	C_1 (μF)	Curve No.	C_1 (μF)
1A	20	3A	0.4
1B	10	3B	0.2
1C	7.0	3C	0.1
1D	3.0	3D	0.06
2A	3.0	4A	0.04
2B	1.0	4B	0.02
2C	0.8	4C	0.01
2D	0.5	4D	0.007

FIGURE 8 – VOLTAGE GAIN ADJUSTMENT BY USE OF EXTERNAL RESISTOR

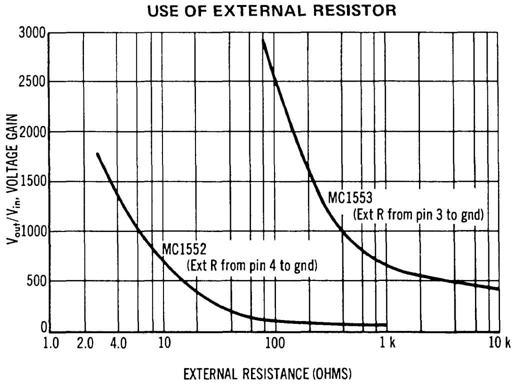
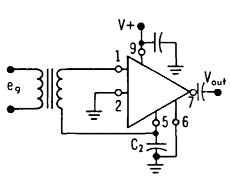


FIGURE 5d – TRANSFORMER COUPLED INPUT



Curve No.	C_2 (μF)	Curve No.	C_2 (μF)
1A	200	3A	2.0
1B	100	3B	1.0
1C	70	3C	0.7
1D	30	3D	0.3
2A	20	4A	0.2
2B	10	4B	0.1
2C	7.0	4C	0.07
2D	3.0	4D	0.03

INPUT ADMITTANCE

$V^+ = 6$ Vdc, $R_L = 1\ k\Omega$, $T_A = +25°C$

FIGURE 9 — GAIN = 50

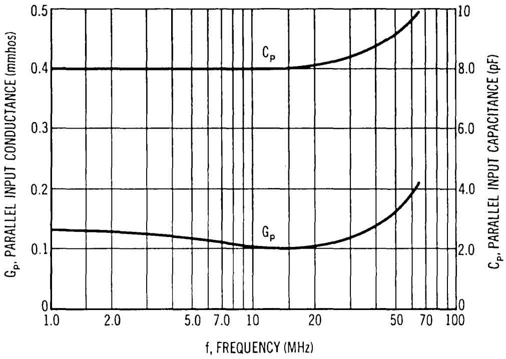


FIGURE 10 — GAIN = 100

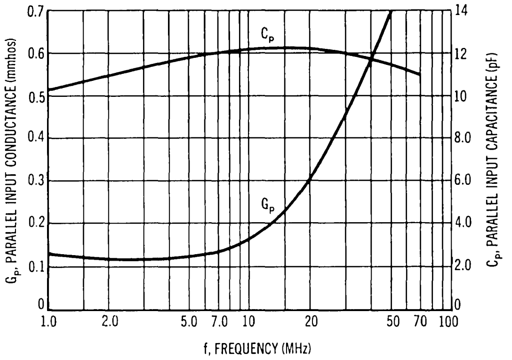


FIGURE 11 — GAIN = 200

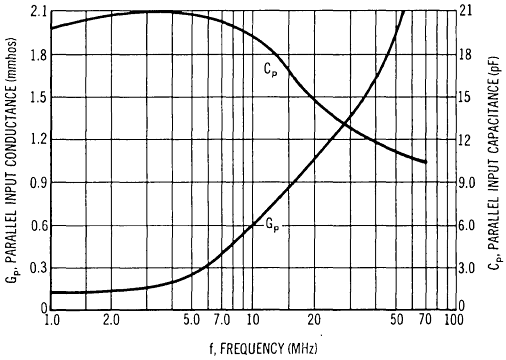


FIGURE 12 — GAIN = 400

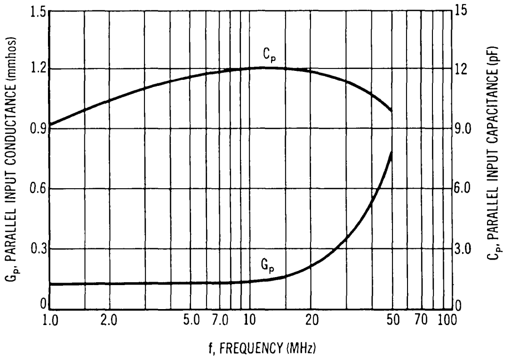


FIGURE 13 — OUTPUT IMPEDANCE versus FREQUENCY

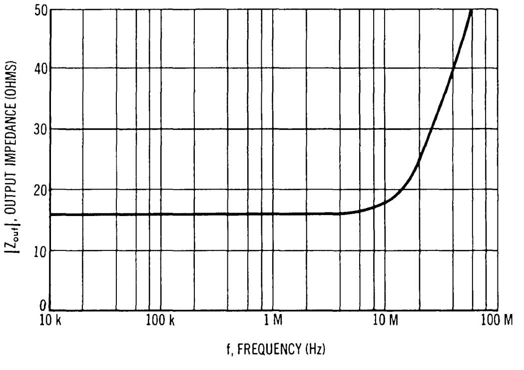
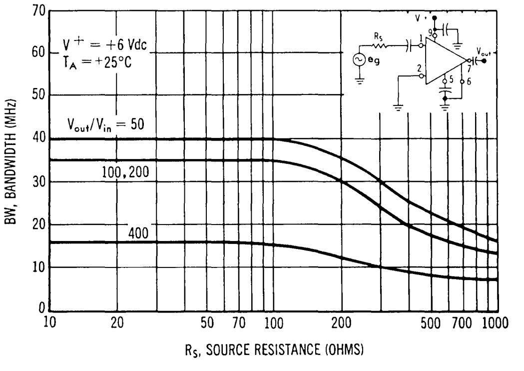


FIGURE 14 — BANDWIDTH versus SOURCE RESISTANCE

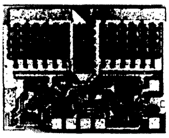


6

MC1554G
MC1454G

POWER AMPLIFIER

MONOLITHIC 1-WATT POWER AMPLIFIERS

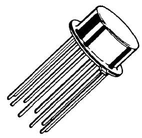


. . . designed to amplify signals to 300-kHz with 1-Watt delivered to a direct coupled or capacitively coupled load.

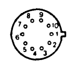
- Low Total Harmonic Distortion – 0.4% (Typ) @ 1 Watt
- Low Output Impedance – 0.2 Ohm
- Excellent Gain – Temperature Stability

1-WATT POWER AMPLIFIER INTEGRATED CIRCUIT

MONOLITHIC
SILICON EPITAXIAL PASSIVATED

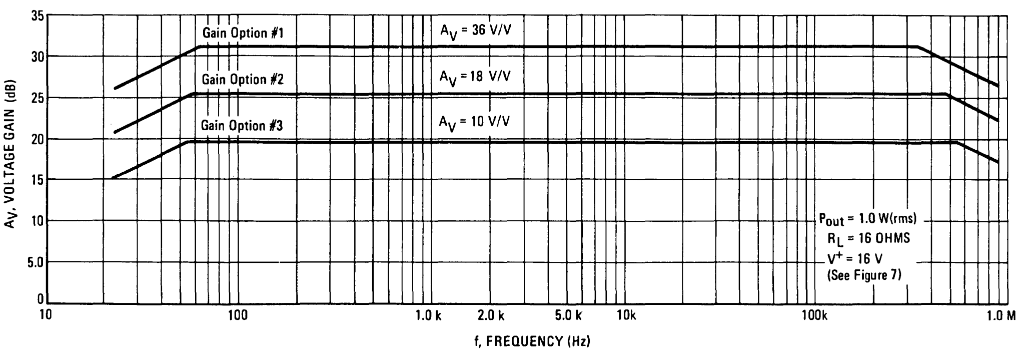


METAL PACKAGE
CASE 602B

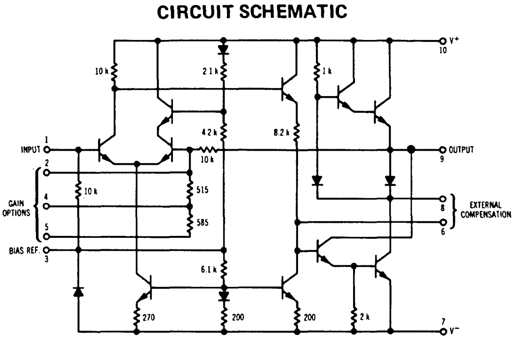


(bottom view)
Pin 7 connected to case

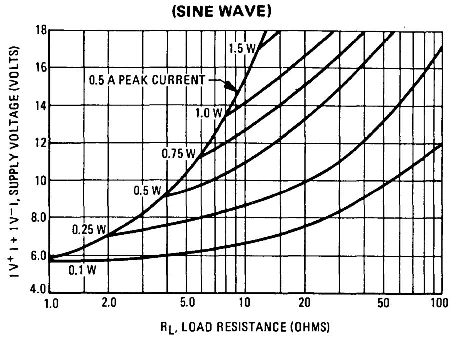
VOLTAGE GAIN versus FREQUENCY (R_L = 16 OHMS)



CIRCUIT SCHEMATIC



MAXIMUM AVAILABLE OUTPUT POWER (SINE WAVE)



See Packaging Information Section for outline dimensions.

ELECTRICAL CHARACTERISTICS (T_C = +25°C unless otherwise noted)
Frequency compensation shown in Figures 6 and 7.

Characteristic	Figure	R_L (Ohms)	Gain Option*	Symbol	MC1554 (-55 to +125°C) Min	Typ	Max	MC1454 (0 to +70°C) Min	Typ	Max	Unit
Output Power (for e_{out}<5.0% THD)	1	16	–	P_{out}	1.0	1.1	–	–	1.0	–	Watt
Power Dissipation (@ P_{out} = 1.0 W)	1	16	–	P_D	–	0.9	1.2	–	0.9	–	Watt
Voltage Gain	1	16	10	A_V	8.0	10	12	–	10	–	V/V
		16	18		–	18	–	–	18	–	
		16	36		–	36	–	–	36	–	
Input Impedance	1	–	10	Z_{in}	7.0	10	–	3.0	10	–	kΩ
Output Impedance	1	–	10	Z_{out}	–	0.2	–	–	0.4	–	Ω
Power Bandwidth (for e_{out}<5.0% THD)	2	16	10		–	270	–	–	270	–	kHz
		16	18		–	250	–	–	250	–	
		16	36		–	210	–	–	210	–	
Total Harmonic Distortion (for e_{in}<0.05% THD, f = 20 Hz to 20 kHz)	2			THD							%
P_{out} = 1.0 Watt (sinewave)		16	10		–	0.4	–	–	0.4	–	
P_{out} = 0.1 Watt (sinewave)		16	10		–	0.5	–	–	0.5	–	
Zero Signal Current Drain	3	∞	–	I_D	–	11	15	–	11	20	mAdc
Output Noise Voltage	3	16	10	V_n	–	0.3	–	–	0.3	–	mV(rms)
Output Quiescent Voltage (Split Supply Operation)	4	16	–	$V_{out}(dc)$	–	±10	±30	–	±10	–	mVdc
Positive Supply Sensitivity (V^- constant)	5	∞	–	S^+	–	-40	–	–	-40	–	mV/V
Negative Supply Sensitivity (V^+ constant)	5	∞	–	S^-	–	-40	–	–	-40	–	mV/V

*To obtain the voltage gain characteristic desired, use the following pin connections:

Voltage Gain	Pin Connection
10	Pins 2 and 4 open, Pin 5 to ac ground
18	Pins 2 and 5 open, Pin 4 to ac ground
36	Pin 2 connected to Pin 5, Pin 4 to ac ground

6

Characteristic Definitions
(Linear Operation)

FIGURE 1

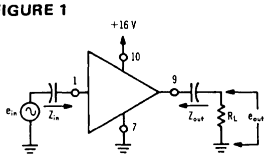


FIGURE 3

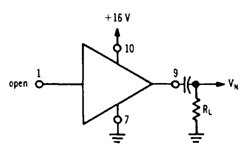


FIGURE 4

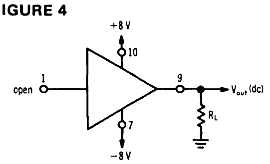


FIGURE 2

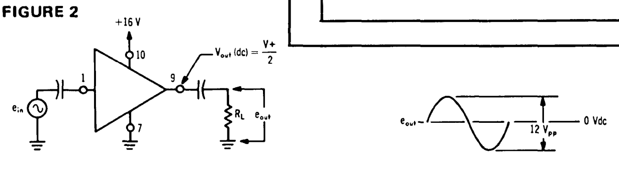
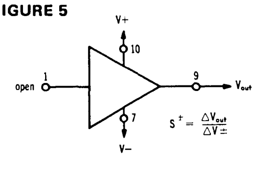


FIGURE 5



MAXIMUM RATINGS (T_C = +25°C unless otherwise noted)

Rating		Symbol	Value	Unit
Total Power Supply Voltage		$\lvert V^+\rvert + \lvert V^-\rvert$	18	Vdc
Peak Load Current		I_{out}	0.5	Ampere
Audio Output Power		P_{out}	1.8	Watts
Power Dissipation (package limitation)				
T_A = +25°C		P_D	600	mW
Derate above 25°C		$1/\theta_{JA}$	4.8	mW/°C
T_C = +25°C		P_D	1.8	Watts
Derate above 25°C		$1/\theta_{JC}$	14.4	mW/°C
Operating Temperature Range	MC1454	T_A	0 to +70	°C
	MC1554		-55 to +125	
Storage Temperature Range		T_{stg}	-55 to +150	°C

TYPICAL CONNECTIONS

FIGURE 6 – SPLIT SUPPLY OPERATION VOLTAGE GAIN (A_V) = 10, $f_{LOW} \approx$ 25 Hz

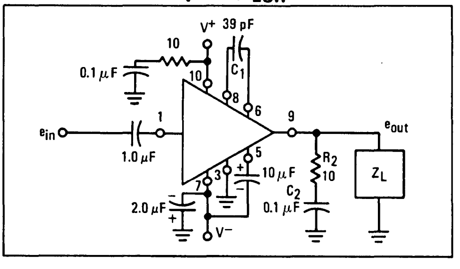
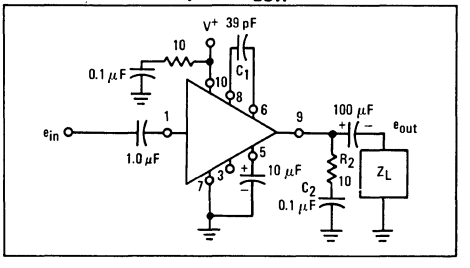


FIGURE 7 – SINGLE SUPPLY OPERATION VOLTAGE GAIN (A_V) = 10, $f_{LOW} \approx$ 100 Hz



RECOMMENDED OPERATING CONDITIONS

In order to avoid local VHF instability, the following set of rules must be adhered to:

1. An R-C stabilizing network (0.1 µF in series with 10 ohms) should be placed directly from pin 9 to ground, as shown in Figures 6 and 7, using short leads, to eliminate local VHF instability caused by lead inductance to the load.
2. Excessive lead inductance from the V+ supply to pin 10 can cause high frequency instability. To prevent this, the V+ by-pass capacitor should be connected with short leads from the V+ pin to ground. If this capacitor is remotely located a series R-C network (0.1 µF and 10 ohms) should be used directly from pin 10 to ground as shown in Figures 6 and 7.
3. Lead lengths from the external components to pins 7, 9, and 10 of the package should be as short as possible to insure good VHF grounding for these points.

Due to the large bandwidth of the amplifier, coupling must be avoided between the output and input leads. This can be assured by either (a) use of short leads which are well isolated, (b) narrow-banding the overall amplifier by placing a capacitor from pin 1 to ground to form a low-pass filter in combination with the source impedance, or (c) use of a shielded input cable. In applications which require upper band-edge control the input low-pass filter is recommended.

TYPICAL CHARACTERISTICS

FIGURE 8 – TOTAL HARMONIC DISTORTION versus LOAD RESISTANCE

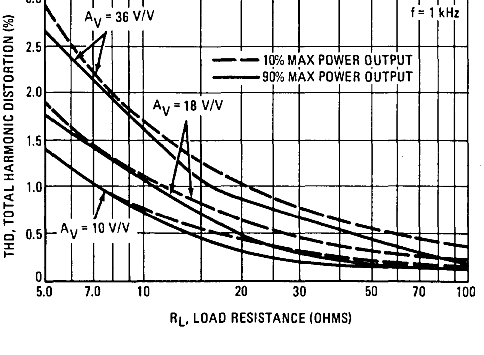
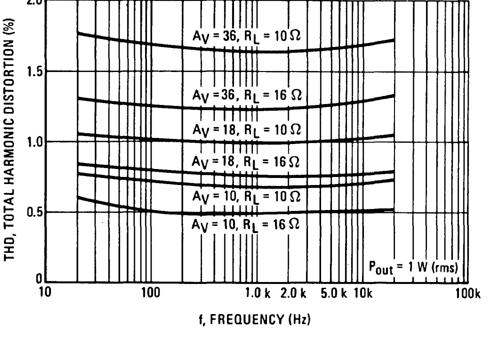


FIGURE 9 – TOTAL HARMONIC DISTORTION versus FREQUENCY



TYPICAL CHARACTERISTICS (continued)

FIGURE 10 — VOLTAGE GAIN versus TEMPERATURE

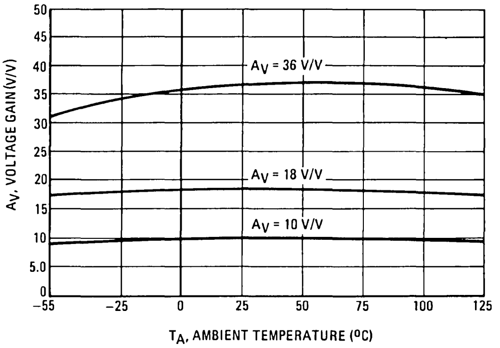


FIGURE 11 — OUTPUT VOLTAGE CHANGE

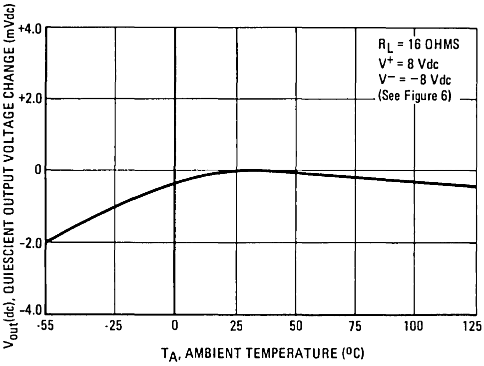


FIGURE 12 — VOLTAGE GAIN versus FREQUENCY ($R_L = \infty$)

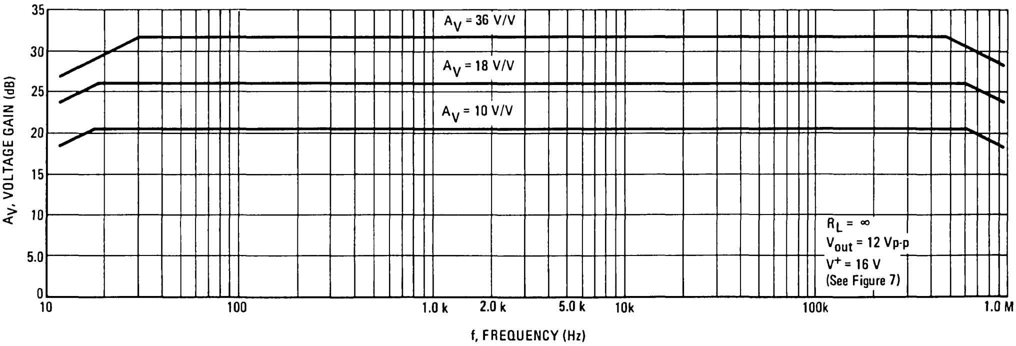
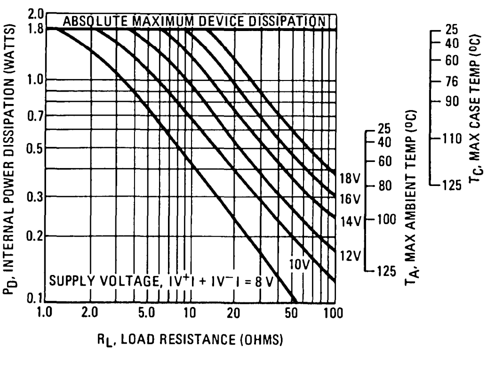


FIGURE 13 — MAXIMUM DEVICE DISSIPATION (SINE WAVE)



OPERATIONAL AMPLIFIERS

MC1556G
MC1456G
MC1456CG

INTERNALLY COMPENSATED, HIGH PERFORMANCE MONOLITHIC OPERATIONAL AMPLIFIER

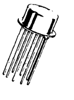
. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components. For detailed information, see Application Note AN-522.

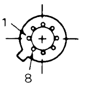
- Low Input Bias Current – 15 nA max
- Low Input Offset Current – 2.0 nA max
- Low Input Offset Voltage – 4.0 mV max
- Fast Slew Rate – 2.5 V/μs typ
- Large Power Bandwidth – 40 kHz typ
- Low Power Consumption – 45 mW max
- Offset Voltage Null Capability
- Output Short-Circuit Protection
- Input Over-Voltage Protection

OPERATIONAL AMPLIFIER INTEGRATED CIRCUIT

EPITAXIAL PASSIVATED

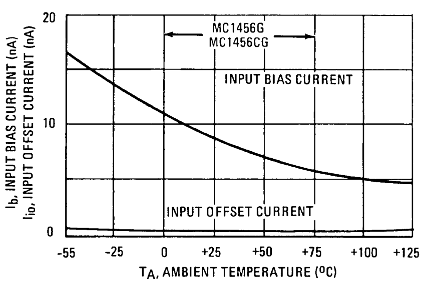
CASE 601
TO-99



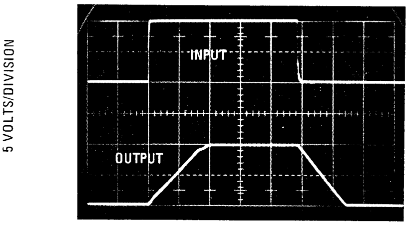


(bottom view)

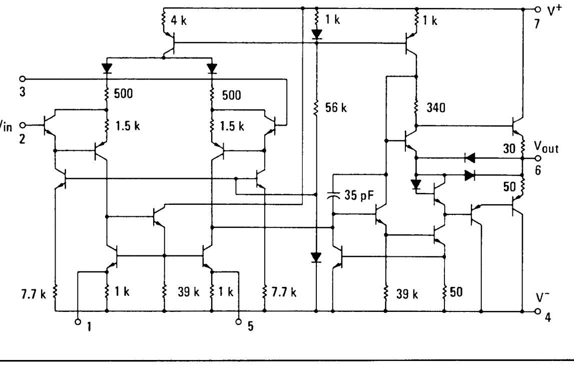
TYPICAL INPUT BIAS CURRENT AND INPUT OFFSET CURRENT versus TEMPERATURE for MC1556G



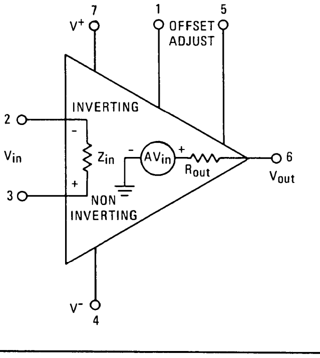
VOLTAGE-FOLLOWER PULSE RESPONSE



CIRCUIT SCHEMATIC



EQUIVALENT CIRCUIT



See Packaging Information Section for outline dimensions.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	MC1556G	MC1456G MC1456CG	Unit
Power Supply Voltage	V^+	+22	+18	Vdc
	V^-	-22	-18	
Differential Input Signal	V_{in}	$\pm V^+$		Volts
Common-Mode Input Swing	CMV_{in}	$\pm V^+$		Volts
Load Current	I_L	20		mA
Output Short Circuit Duration	t_S	Continuous		
Power Dissipation (Package Limitation)	P_D	680		mW
Derate above T_A = +25°C		4.6		mW/°C
Operating Temperature Range	T_A	-55 to +125	0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V^+ = +15 Vdc, V^- = -15 Vdc, T_A = +25°C unless otherwise noted)

Characteristic	Fig.	Symbol	MC1556G Min	MC1556G Typ	MC1556G Max	MC1456G Min	MC1456G Typ	MC1456G Max	MC1456CG Min	MC1456CG Typ	MC1456CG Max	Unit
Input Bias Current		I_b										nAdc
T_A = +25°C			–	8.0	15	–	15	30	–	15	90	
T_A = T_{low} to T_{high} (See Note 1)			–	–	30	–	–	40	–	–	–	
Input Offset Current		$\lvert I_{io} \rvert$										nAdc
T_A = +25°C			–	1.0	2.0	–	5.0	10	–	5.0	30	
T_A = +25°C to T_{high}			–	–	3.0	–	–	14	–	–	–	
T_A = T_{low} to +25°C			–	–	5.0	–	–	14	–	–	–	
Input Offset Voltage		$\lvert V_{io} \rvert$										mVdc
T_A = +25°C			–	2.0	4.0	–	5.0	10	–	5.0	12	
T_A = T_{low} to T_{high}			–	–	6.0	–	–	14	–	–	–	
Differential Input Impedance (Open-Loop, f = 20 Hz)												
Parallel Input Resistance		R_p	–	5.0	–	–	3.0	–	–	3.0	–	Megohms
Parallel Input Capacitance		C_p	–	6.0	–	–	6.0	–	–	6.0	–	pF
Common-Mode Input Impedance (f = 20 Hz)		Z_{in}	–	250	–	–	250		–	250	–	Megohms
Common-Mode Input Voltage Swing	1	CMV_{in}	±12	±13	–	±11	±12	–	±10.5	±12	–	V_{pk}
Equivalent Input Noise Voltage (A_V = 100, R_s = 10 k ohms, f = 1.0 kHz, BW = 1.0 Hz)	2	e_n	–	45			45	–	–	45	–	nV/(Hz)½
Common-Mode Rejection Ratio (f = 100 Hz)	3	CM_{rej}	80	110	–	70	110	–	–	110	–	dB
Open-Loop Voltage Gain, (V_{out} = ±10 V, R_L = 2.0 k ohms)	4,5,6	A_{VOL}										V/V
T_A = +25°C			100,000	200,000	–	70,000	100,000	–	25,000	100,000	–	
T_A = T_{low} to T_{high}			40,000	–	–	40,000	–	–	–	–	–	
Power Bandwidth (A_V = 1, R_L = 2.0 k ohms, THD≤5%, V_{out} = 20 Vp-p)	9	P_{BW}	–	40	–	–	40	–		40	–	kHz
Unity Gain Crossover Frequency (open-loop)	5	f_c	–	1.0	–	–	1.0	–	–	1.0	–	MHz
Phase Margin (open-loop, unity gain)	5,7		–	70	–	–	70	–	–	70	–	degrees
Gain Margin	5,7		–	18	–	–	18	–	–	18	–	dB
Slew Rate (Unity Gain)		dV_{out}/dt	–	2.5	–	–	2.5	–	–	2.5	–	V/µs
Output Impedance (f = 20 Hz)		Z_{out}	–	1.0	2.0	–	1.0	2.5	–	1.0	–	kohms
Short-Circuit Output Current	8	I_{SC}	–	-17, +9.0	–	–	-17, +9.0	–	–	-17, +9.0	–	mAdc
Output Voltage Swing (R_L = 2.0 k ohms)	10	V_{out}	±12	±13	–	±11	±12	–	±10	±12	–	V_{pk}
Power Supply Sensitivity												µV/V
V^- = constant, $R_s \leq$ 10 k ohms		S+		50	100	–	75	200	–	75	–	
V^+ = constant, $R_s \leq$ 10 k ohms		S–		50	100	–	75	200	–	75	–	
Power Supply Current		I_D+	–	1.0	1.5	–	1.3	3.0	–	1.3	4.0	mAdc
		I_D-	–	1.0	1.5	–	1.3	3.0	–	1.3	4.0	
DC Quiescent Power Dissipation (V_{out} = 0)	11	P_D	–	30	45	–	40	90	–	40	120	mW

Note 1: T_{low}: 0° for MC1456G and MC1456CG
-55°C for MC1556G

T_{high}: +75°C for MC1456G and MC1456CG
+125°C for MC1556G

TYPICAL CHARACTERISTICS

($V^+ = +15$ Vdc, $V^- = -15$ Vdc, $T_A = +25^oC$ unless otherwise noted)

FIGURE 1 – INPUT COMMON-MODE SWING versus POWER SUPPLY VOLTAGE

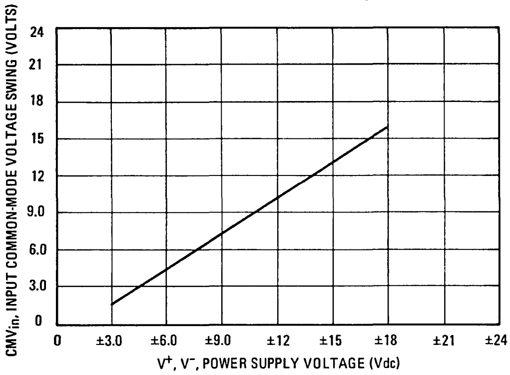


FIGURE 2 – SPECTRAL NOISE DENSITY

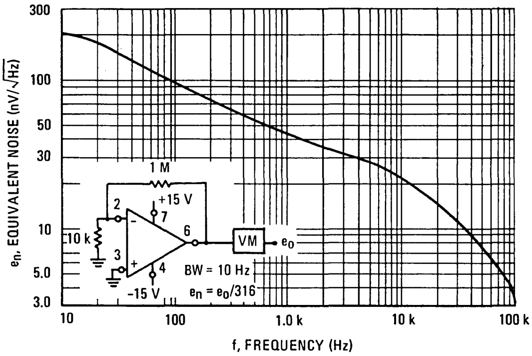


FIGURE 3 – COMMON-MODE REJECTION RATIO versus FREQUENCY

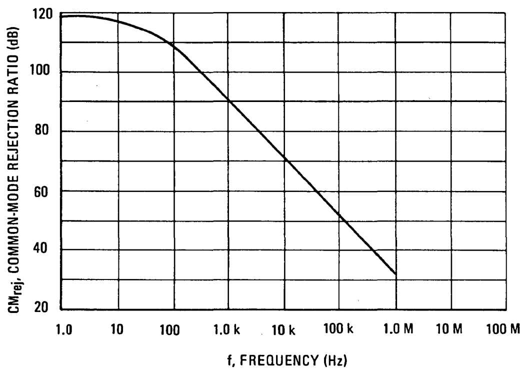


FIGURE 4 – OPEN-LOOP VOLTAGE GAIN versus TEMPERATURE

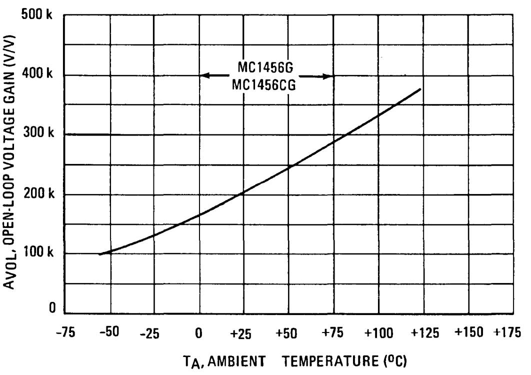


FIGURE 5 – OPEN-LOOP FREQUENCY RESPONSE

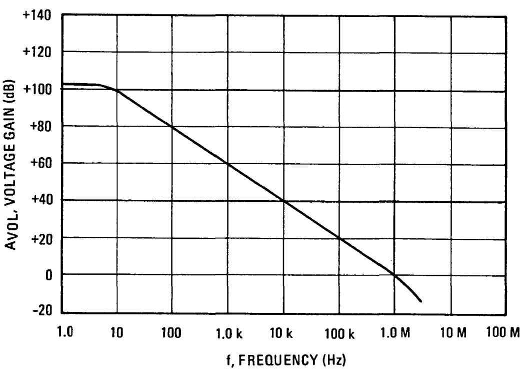
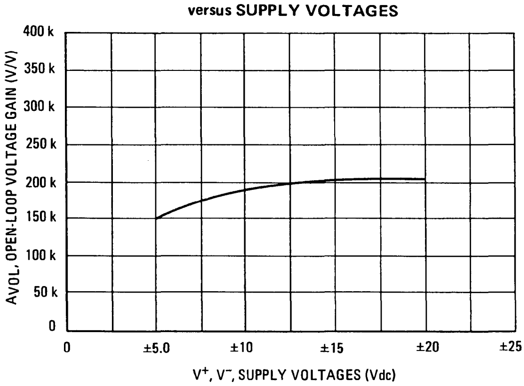


FIGURE 6 – OPEN-LOOP VOLTAGE GAIN versus SUPPLY VOLTAGES



TYPICAL CHARACTERISTICS (continued)

FIGURE 7 – OPEN-LOOP PHASE SHIFT

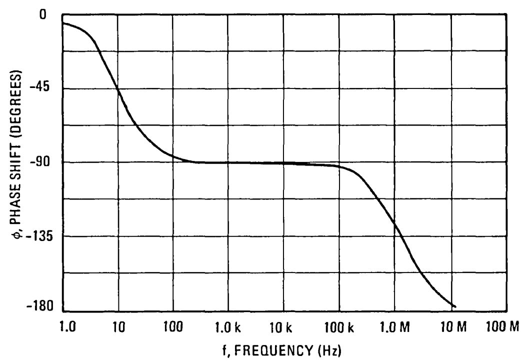


FIGURE 8 – OUTPUT SHORT-CIRCUIT CURRENT versus TEMPERATURE

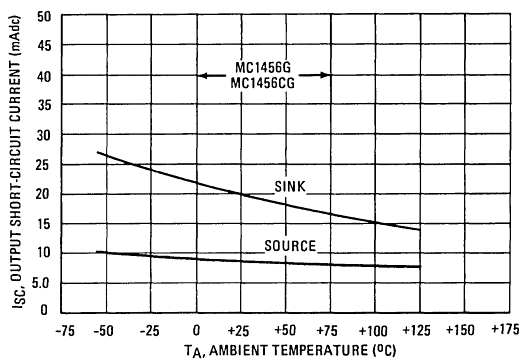


FIGURE 9 – POWER BANDWIDTH

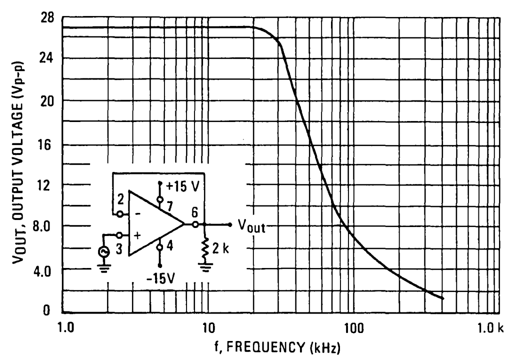


FIGURE 10 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

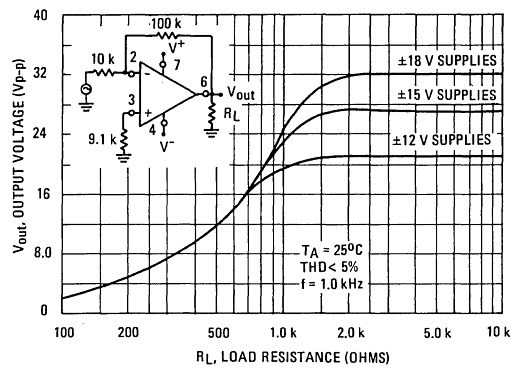
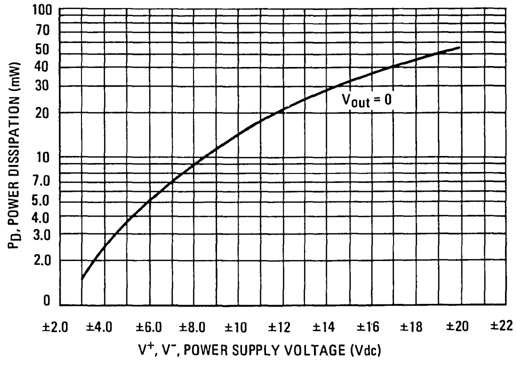


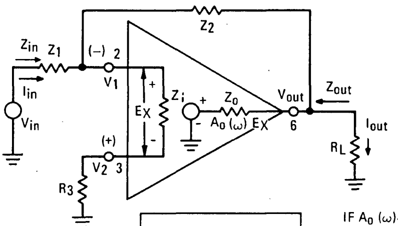
FIGURE 11 – POWER DISSIPATION versus POWER SUPPLY VOLTAGE



TYPICAL APPLICATIONS

Where values are not given for external components they must be selected by the designer to fit the requirements of the system.

FIGURE 12 – INVERTING FEEDBACK MODEL

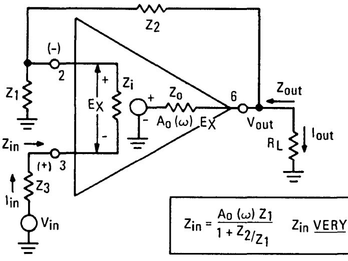


$Z_{out} = Z_0 \dfrac{1 + Z_2/Z_1}{A_0(\omega)}$

IF $A_0(\omega) \to \infty$ $\quad \dfrac{V_{out}}{V_{in}} = -\dfrac{Z_2}{Z_1}$

IF $R_3 \ll Z_1$ $\quad Z_{in} \approx Z_1$

FIGURE 13 – NON-INVERTING FEEDBACK MODEL



$Z_{in} = \dfrac{A_0(\omega)\,Z_1}{1 + Z_2/Z_1}$ $\quad Z_{in}$ VERY HIGH

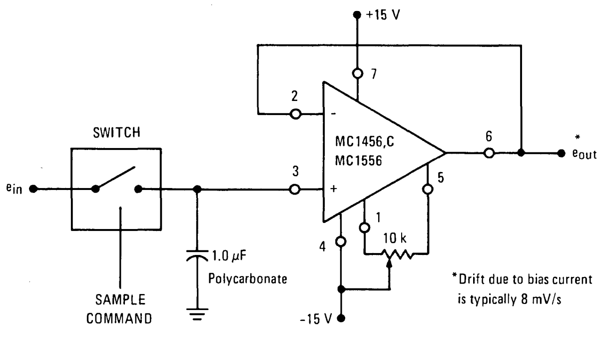
$A_0(\omega) \to \infty$

$Z_{out} = Z_0 \dfrac{1 + Z_2/Z_1}{A_0(\omega)}$

$\dfrac{V_{out}}{V_{in}} = 1 + Z_2/Z_1$

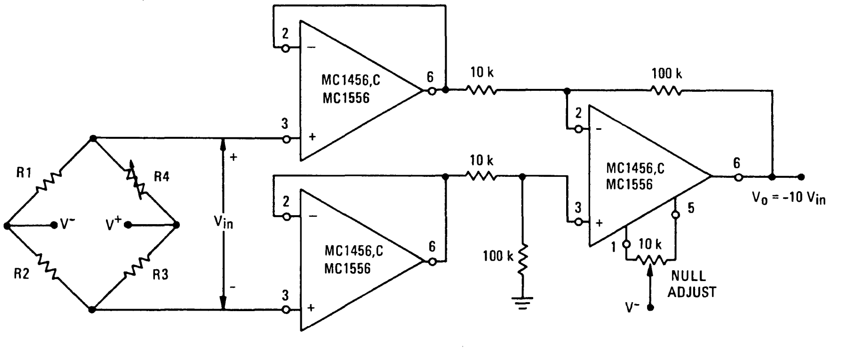
$Z_{out} \to 0$

FIGURE 14 – LOW-DRIFT SAMPLE AND HOLD



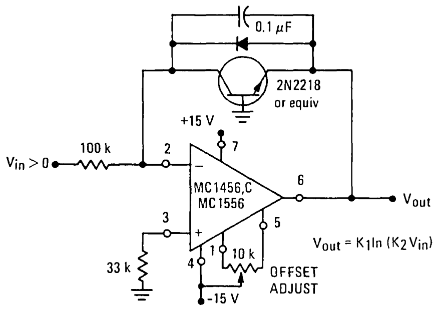
*Drift due to bias current is typically 8 mV/s

FIGURE 15 – HIGH IMPEDANCE BRIDGE AMPLIFIER



TYPICAL APPLICATIONS (continued)

FIGURE 16 — LOGARITHMIC AMPLIFIER



See Application Note AN-261 for further detail.

FIGURE 17 — VOLTAGE OFFSET NULL CIRCUIT

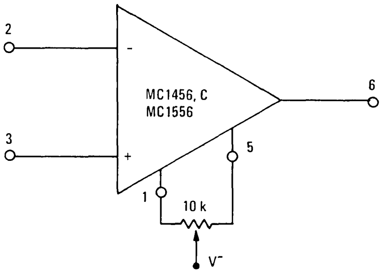
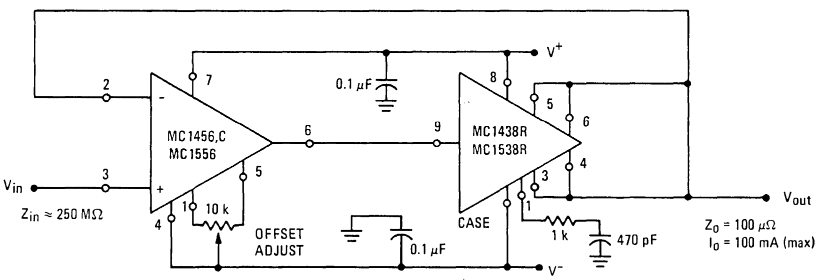


FIGURE 18 — HIGH INPUT IMPEDANCE, HIGH OUTPUT CURRENT VOLTAGE FOLLOWER



6

MC1558
MC1458
MC1458C

OPERATIONAL AMPLIFIERS

DUAL MC1741
INTERNALLY COMPENSATED, HIGH PERFORMANCE MONOLITHIC OPERATIONAL AMPLIFIER

. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

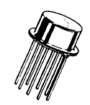
- No Frequency Compensation Required
- Short-Circuit Protection
- Wide Common-Mode and Differential Voltage Ranges
- Low-Power Consumption
- No Latch Up

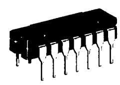
(DUAL MC1741)

DUAL OPERATIONAL AMPLIFIER

MONOLITHIC SILICON INTEGRATED CIRCUIT

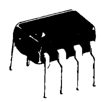
G SUFFIX
METAL PACKAGE
CASE 601
TO-99



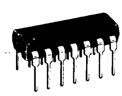


L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

P1 SUFFIX
PLASTIC PACKAGE
CASE 626
MC1458,C (only)



P2 SUFFIX
PLASTIC PACKAGE
CASE 605
MC1458,C (only)



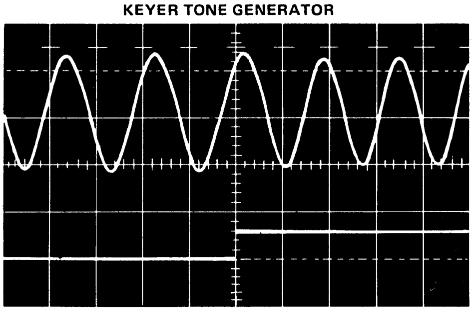
PIN CONNECTIONS

Schematic	A	B	C	D	E	F	G	H	I	J	K	L
G & P1 Packages	1	–	–	2	3	4	5	6	–	–	7	8
L & P2 Packages	2	3	4	5	6	7	8	9	10	11	12	14

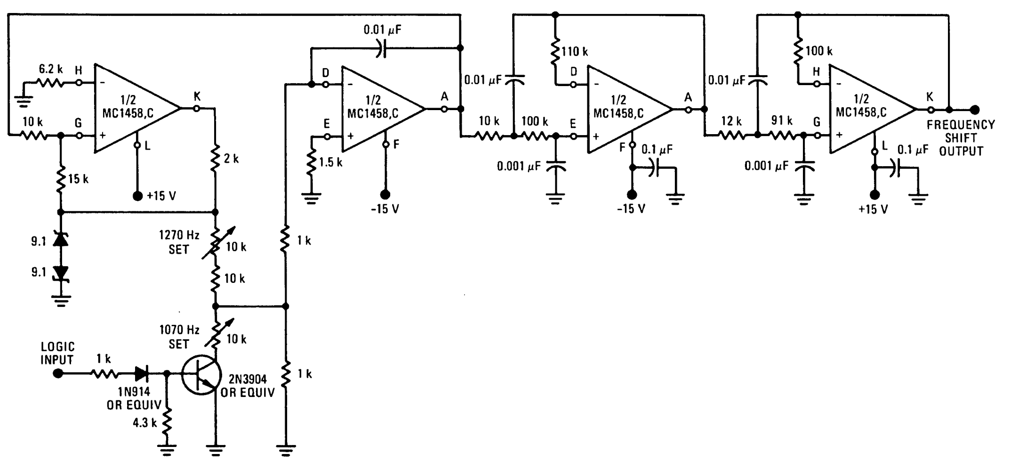
6

FIGURE 1 – TYPICAL FREQUENCY-SHIFT KEYER TONE GENERATOR

5.0 V/DIV.



0.5 ms/DIV.



See Packaging Information Section for outline dimensions.

See current MCC1558/1458 data sheet for standard linear chip information.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	MC1558	MC1458,C	Unit
Power Supply Voltage	V^+ V^-	+22 -22	+18 -18	Vdc
Differential Input Signal ①	V_{in}	±30		Volts
Common-Mode Input Swing ②	CMV_{in}	±15		Volts
Output Short Circuit Duration	t_S	Continuous		
Power Dissipation (Package Limitation)	P_D			
Metal Can		680		mW
Derate above T_A = +25°C		4.6		mW/°C
Plastic Dual In-Line Packages		625		mW
Derate above T_A = +25°C		5.0		mW/°C
Ceramic Dual In-Line Package		750		mW/°C
Derate above T_A = +25°C		6.0		mW/°C
Operating Temperature Range	T_A	-55 to +125	0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V^+ = +15 Vdc, V^- = -15 Vdc, T_A = +25°C unless otherwise noted)

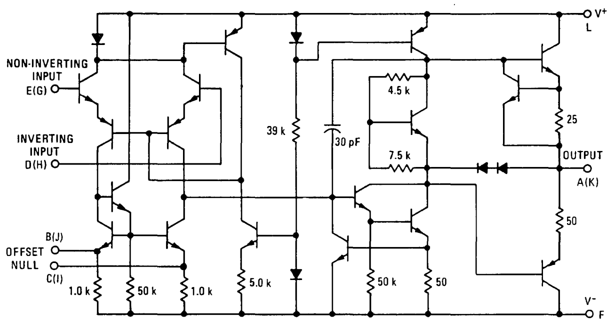
Characteristics	Symbol	MC1558			MC1458			MC1458C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Bias Current	I_b										µAdc
T_A = +25°C		–	0.2	0.5	–	0.2	0.5	–	0.2	0.7	
T_A = T_{low} to T_{high} ③		–	–	1.5	–	–	0.8	–	–	1.0	
Input Offset Current	$\lvert I_{io} \rvert$										µAdc
T_A = +25°C		–	0.03	0.2	–	0.03	0.2	–	0.03	0.3	
T_A = T_{low} to T_{high}		–	–	0.5	–	–	0.3	–	–	0.4	
Input Offset Voltage ($R_S \le 10$ k Ω)	$\lvert V_{io} \rvert$										mVdc
T_A = +25°C		–	1.0	5.0	–	2.0	6.0	–	2.0	10	
T_A = T_{low} to T_{high}		–	–	6.0	–	–	7.5	–	–	12	
Differential Input Impedance (Open-Loop, f = 20 Hz)											
Parallel Input Resistance	R_p	0.3	1.0	–	0.3	1.0	–	–	1.0	–	Megohm
Parallel Input Capacitance	C_p	–	6.0	–	–	6.0	–	–	6.0	–	pF
Common-Mode Input Impedance (f = 20 Hz)	$Z_{(in)}$	–	200	–	–	200		–	200		Megohms
Common-Mode Input Voltage Swing	CMV_{in}	±12	±13	–	±12	±13	–	±11	±13	–	V_{pk}
Equivalent Input Noise Voltage (A_V = 100, R_s = 10 k ohms, f = 1.0 kHz, BW = 1.0 Hz)	e_n	–	45	–	–	45	–	–	45	–	nV/(Hz)½
Common-Mode Rejection Ratio (f = 100 Hz)	CM_{rej}	70	90	–	70	90	–	60	90	–	dB
Open-Loop Voltage Gain	A_{VOL}										V/V
T_A = +25°C (V_o = ±10 V, R_L = 2.0 k ohms)		50,000	200,000	–	20,000	100,000	–	–	–	–	
T_A = T_{low} to T_{high} (V_o = ±10 V, R_L = 2.0 k ohms)		25,000	–	–	15,000	–	–	–	–	–	
T_A = +25°C (V_o = ±10 V, R_L = 10 k ohms)		–	–	–	–	–	–	20,000	100,000	–	
T_A = T_{low} to T_{high} (V_o = ±10 V, R_L = 10 k ohms)		–	–	–	–	–	–	15,000	–	–	
Power Bandwidth (A_V = 1, R_L = 2.0 k ohms, THD≤5%, V_o = 20 V p-p)	P_{BW}	–	14	–	–	14	–	–	14	–	kHz
Unity Gain Crossover Frequency (open-loop)	f_c	–	1.1	–	–	1.1	–	–	1.1	–	MHz
Phase Margin (open-loop, unity gain)		–	65	–	–	65	–	–	65	–	degrees
Gain Margin		–	11	–	–	11	–	–	11	–	dB
Slew Rate (Unity Gain)	dV_{out}/dt	–	0.8	–	–	0.8	–	–	0.8	–	V/µs
Output Impedance (f = 20 Hz)	Z_{out}	–	75	–	–	75	–	–	75	–	ohms
Short-Circuit Output Current	I_{SC}	–	20	–	–	20	–	–	20	–	mAdc
Output Voltage Swing (R_L = 10 k ohms)	V_o	±12	±14	–	±12	±14	–	±11	±14	–	Vpk
R_L = 2 k ohms (T_A = T_{low} to t_{high})		±10	±13	–	±10	±13	–	±9.0	±13	–	
Average Temperature Coefficient of Input Offset Voltage (R_S = 50 ohms, T_A = T_{low} to T_{high})	$\lvert TCV_{io} \rvert$	–	15	–	–	15	–	–	15	–	µV/°C
Power Supply Sensitivity											µV/V
V^- = constant, $R_s \le 10$ k ohms	S+	–	30	150	–	30	150	–	30	–	
V^+ = constant, $R_s \le 10$ k ohms	S-	–	30	150	–	30	150	–	30	–	
Power Supply Current	I_D^+	–	2.3	5.0	–	2.3	5.6	–	2.3	8.0	mAdc
	I_D^-	–	2.3	5.0	–	2.3	5.6	–	2.3	8.0	
DC Quiescent Power Dissipation (V_o = 0)	P_D	–	70	150	–	70	170	–	70	240	mW

① For supply voltages of less than ±15 V, the maximum differential input voltage is equal to $\pm(V^+ + |V^-|)$.

② For supply voltages of less than ±15 V, the maximum input voltage is equal to the supply voltage $(+V^+, -|V^-|)$.

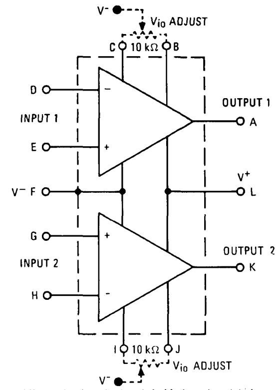
③ T_{low}: 0°C for MC1458,C
-55°C for MC1558
T_{high}: +75°C for MC1458,C
+125°C for MC1558

FIGURE 2 – CIRCUIT SCHEMATIC



The letters without parenthesis represent the pin numbers for 1/2 of the dual circuit, letters in parenthesis represent the pin numbers for the other half.

FIGURE 3 – EQUIVALENT CIRCUIT WITH OFFSET ADJUST



Offset Adjust is available only in 14-pin packaged devices.

PIN CONNECTIONS

Schematic	A	B	C	D	E	F	G	H	I	J	K	L
G & P1 Packages	1	–	–	2	3	4	5	6	–	–	7	8
L & P2 Packages	2	3	4	5	6	7	8	9	10	11	12	14

TYPICAL CHARACTERISTICS

($V^+ = +15$ Vdc, $V^- = -15$ Vdc, $T_A = +25^oC$ unless otherwise noted.)

FIGURE 4 – OPEN-LOOP VOLTAGE GAIN versus POWER-SUPPLY VOLTAGE

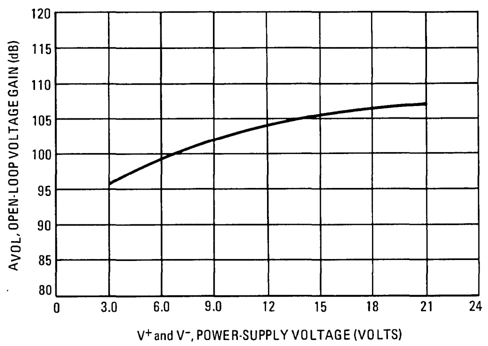


FIGURE 5 – OPEN-LOOP FREQUENCY RESPONSE

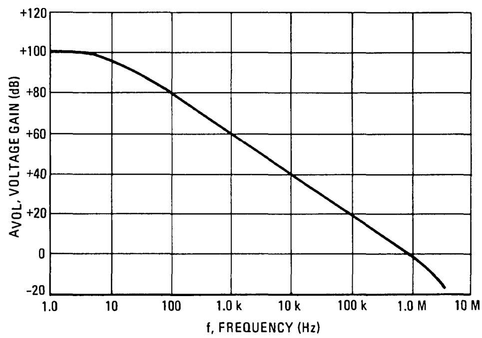


FIGURE 6 – POWER BANDWIDTH (LARGE SIGNAL SWING versus FREQUENCY)

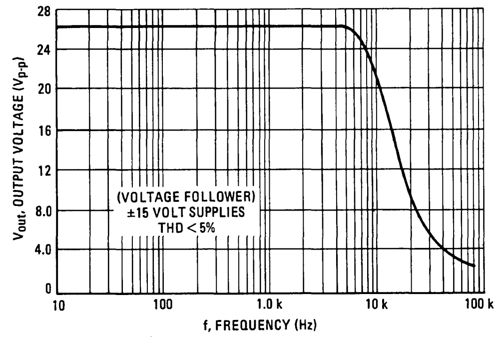
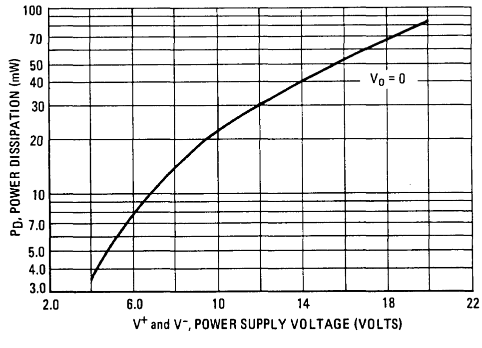


FIGURE 7 – POWER DISSIPATION versus POWER SUPPLY VOLTAGE



TYPICAL CHARACTERISTICS (continued)

($V^+ = +15$ Vdc, $V^- = -15$ Vdc, $T_A = +25^{\circ}C$ unless otherwise noted.)

FIGURE 8 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

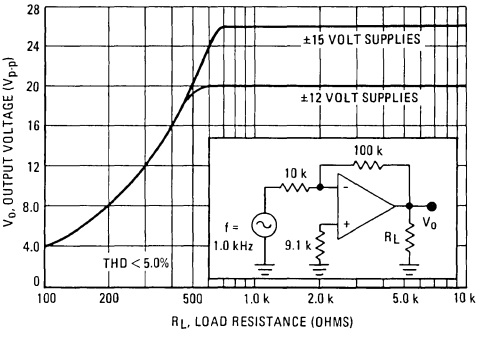


FIGURE 9 – OUTPUT NOISE versus SOURCE RESISTANCE

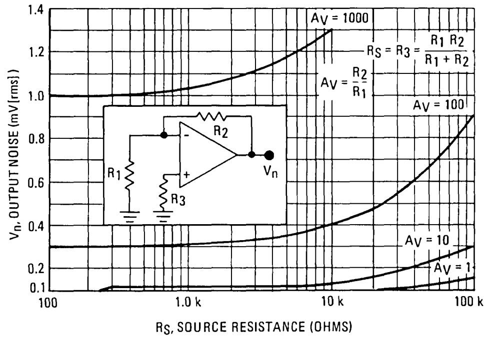
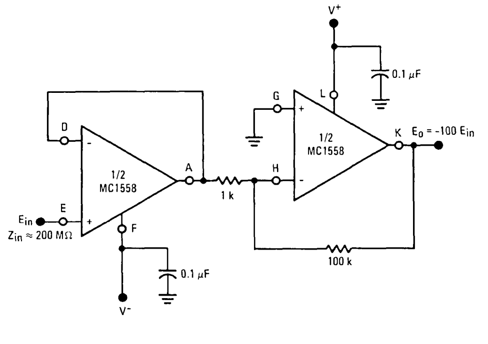


FIGURE 10 – HIGH-IMPEDANCE, HIGH-GAIN INVERTING AMPLIFIER



MC1560, MC1561
MC1460, MC1461

POSITIVE VOLTAGE REGULATORS

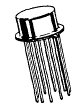
MONOLITHIC VOLTAGE REGULATOR

. . . designed to deliver continuous load current up to 500 mA without use of an external power transistor.

- Electronic "Shut-Down" Control and Short-Circuit Protection
- Excellent Load Regulation (Low Output Impedance = 20 milliohms typ from dc to 100 kHz)
- High Power Capability: To 17.5 Watts
- Excellent Transient Response and Temperature Stability
- High Ripple Rejection = 0.002 %/V typ
- Single External Transistor Can Boost Load Current to Greater than 10 Amperes
- Input Voltages to 40 Volts (MC1561)

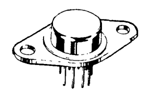
POSITIVE-POWER-SUPPLY VOLTAGE REGULATOR INTEGRATED CIRCUIT

EPITAXIAL PASSIVATED



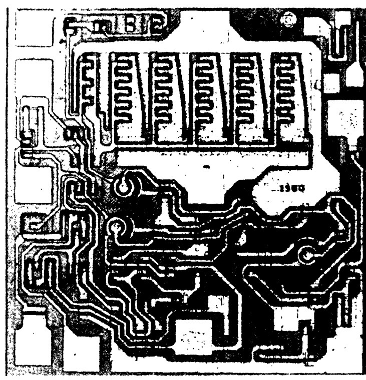
Pin 10 electrically connected to case through substrate.

G SUFFIX
METAL PACKAGE
CASE 602A

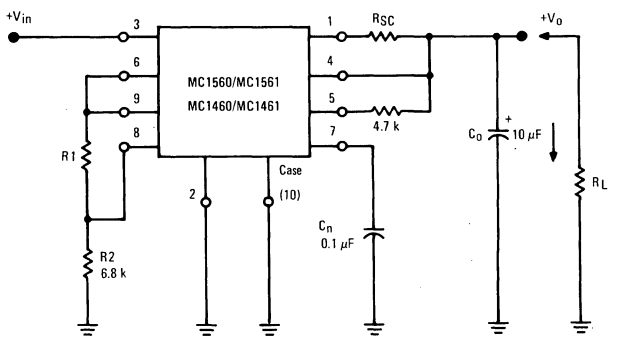


Case is ground terminal

R SUFFIX
METAL PACKAGE
CASE 614



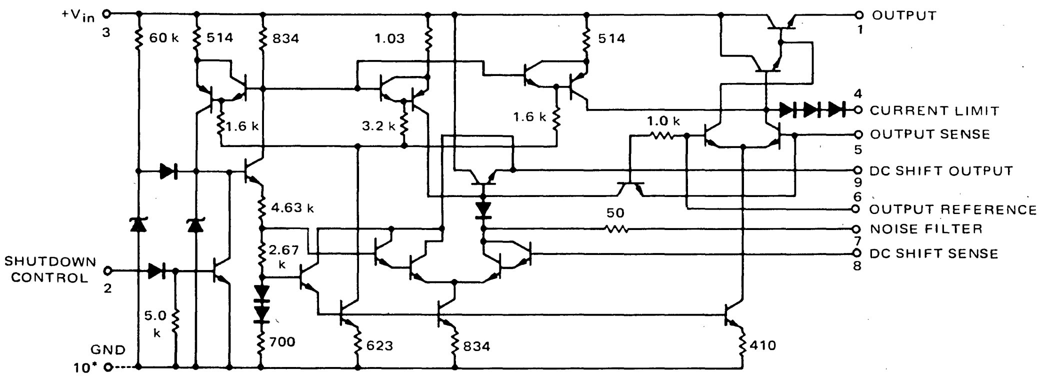
TYPICAL APPLICATION



Select R1 to give desired V_O:

$R1 \approx (2\,V_O - 7.0)\ k\Omega$

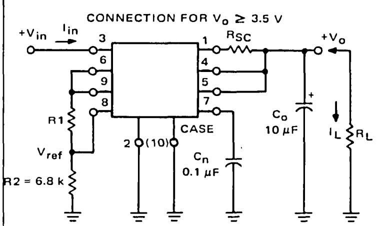
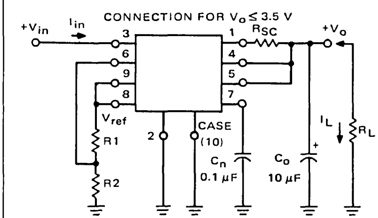
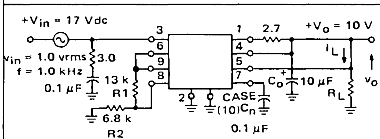
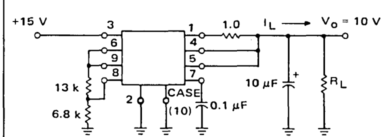
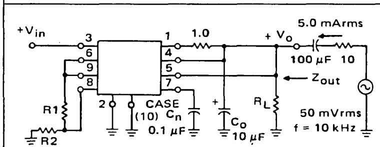
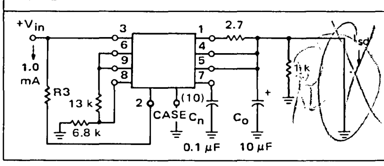
CIRCUIT SCHEMATIC



*"G" package – pin 10 is ground, "R" package – case is ground.

See Packaging Information Section for outline dimensions.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted) (Load Current = 100 mA for "R" Package device, = 10 mA for "G" Package device, unless otherwise noted)

Characteristic Definitions (linear operation)	Characteristic		Symbol	Min	Typ	Max	Units
(R_{SC} = 2.7 ohms unless otherwise noted)  Select R1 to give desired V_o: $R1 \approx (2\ V_o - 7)$ kΩ	Input Voltage (See Note 1)		V_{in}				Vdc
	(0 to +75°C)	MC1460		9.0	–	20	
	(-55°C to +125°C)	MC1560		8.5	–	20	
	(0 to +75°C)	MC1461		9.0	–	35	
	(-55°C to +125°C)	MC1561		8.5	–	40	
	Output Voltage Range	MC1460, MC1560	V_o	2.5	–	17	Vdc
		MC1461		2.5	–	32	
		MC1561		2.5	–	37	
	Reference Voltage (V_{in} = 15 V) (Pin 8 to ground)		V_{ref}	3.2	3.5	3.8	Vdc
 Select R2 to give desired V_o: $R2 \approx (2\ V_o)$ kΩ. Select R1: $R1 \approx (7.0\ k\Omega - R2)$ kΩ	Minimum Input-Output Voltage Differential (See Note 2) (R_{SC} = 0)	MC1460, MC1461	V_{in}-V_o	–	2.1	3.0	Vdc
		MC1560, MC1561		–	2.1	2.7	
	Bias Current (V_{in} = 15 V) (I_L = 1.0 mAdc, R_2 = 6.8 kΩ, $I_B = I_{in} - I_L$)	MC1460, MC1461	I_B	–	5.0	12	mAdc
		MC1560, MC1561		–	4.0	9.0	
	Output Noise (C_n = 0.1 µF, f = 10 Hz to 5.0 MHz)		v_n	–	0.150	–	mV (rms)
	Temperature Coefficient of Output Voltage (See Note 3) (0 to +75°C)	MC1460, MC1461	TC_{V_o}	–	±0.002	–	%/°C
	(-55° to +125°C)	MC1560, MC1561		–	±0.002	–	
	Operating Load Current Range*		I_L				mAdc
	($R_{SC} \leq$ 0.3 ohms) R Package			1.0	–	500	
	($R_{SC} \leq$ 2.0 ohms) G Package			1.0	–	200	
	Input Regulation (% change in output voltage per 1-volt change in input voltage) $Reg_{in} = \frac{v_o(rms)\ (100)}{v_{in}\ (rms)\ V_o}\ V_{in}\ (rms)$ (See Note 4)	MC1460, MC1461	Reg_{in}	–	0.003	0.030	%/V_o
		MC1560, MC1561		–	0.002	0.015	
	Load Regulation T_J = Constant (1.0 mA ≤ I_L ≤ 20 mA)	MC1460	Reg_{load}	–	0.5	2.0	mV
		MC1560		–	0.3	1.2	
		MC1461		–	0.7	2.4	
		MC1561		–	0.4	1.6	
	T_C = 25°C (See Note 5) (1.0 mA ≤ I_L ≤ 50 mA)	R Package		–	0.005	0.05	%
		G Package		–	0.01	0.13	
	Output Impedance (See Note 6) (R_{SC} = 1.0 ohms, f = 10 kHz, V_{in} = 14 Vdc)	MC1460	Z_{out}	–	25	100	milli-ohms
		MC1560		–	15	60	
	(I_L = 25 mAdc for G Package)	MC1461		–	35	120	
		MC1561		–	20	80	
	Shutdown Current (V_{in} = 20 Vdc)	MC1460	I_{sd}	–	80	300	µAdc
		MC1560		–	20	50	
	(V_{in} = 35 Vdc)	MC1461		–	140	500	
	$R_3 \approx \frac{V_{in} - 1.4}{1.0\ mA}$	MC1561		–	70	150	

*Operating Load Current is also limited by dc Safe Operating Area (see Figures 15A and 15B). Care must be taken not to exceed the dc Safe Operating Area at any time.

MAXIMUM RATINGS (T_C = +25°C unless otherwise noted)

Rating	Symbol	Value		Unit
Input Voltage — MC1460, MC1560	V_{in}	20		Vdc
MC1461		35		
MC1561		40		
		G Package	R Package	
Load Current	I_L	250	600	mA
Current, Pin 2	$I_{pin\ 2}$	10	10	mA
Current, Pin 9	$I_{pin\ 9}$	5.0	5.0	
Power Dissipation and Thermal Characteristics				
T_A = 25°C	P_D	0.68	3.0	Watts
Derate above T_A = 25°C	$1/\theta_{JA}$	5.44	24	mW/°C
Thermal Resistance, Junction to Air	θ_{JA}	184	41.6	°C/W
T_C = 25°C	P_D	1.8	17.5*	Watts
Derate above T_C = 25°C	$1/\theta_{JC}$	14.4	140	mW/°C
Thermal Resistance, Junction to Case	θ_{JC}	69.4	7.15	°C/W
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150		°C

*The MC1460R and MC1560R are limited to 12 watts maximum by the voltage and current maximum ratings.

OPERATING TEMPERATURE RANGE

Ambient Temperature	T_A		°C
MC1460, MC1461		0 to +75	
MC1560, MC1561		-55 to +125	

Note 1. "Minimum Input Voltage" is the minimum "total instantaneous input voltage" required to properly bias the internal zener reference diode. For output voltages greater than approximately 5.5 Vdc the minimum "total instantaneous input voltage" must increase to the extent that it will always exceed the output voltage by at least the "input-output voltage differential".

Note 2. This parameter states that the MC1560/1561 and MC1460/1461 will regulate properly with the input-output voltage differential ($V_{in} - V_O$) as low as 2.7 Vdc and 3.0 Vdc respectively. Typical units will regulate properly with ($V_{in} - V_O$) as low as 2.1 Vdc as shown in the typical column.

Note 3. "Temperature Coefficient of Output Voltage" is defined as:

MC1560, MC1561 $$TC_{V_O} = \frac{\pm (V_{O\ max} - V_{O\ min})(100)}{2\ (180°C)(V_O\ @\ 25°C)} = \%/°C$$

MC1460, MC1461 $$TC_{V_O} = \frac{\pm (V_{O\ max} - V_{O\ min})(100)}{2\ (75°C)(V_O\ @\ 25°C)} = \%/°C$$

The output-voltage adjusting resistors (R1 and R2) must have matched temperature characteristics in order to maintain a constant ratio independent of temperature.

Note 4. The input signal can be introduced by use of a transformer which will allow the output of an audio oscillator to be coupled in series with the dc input to the regulator. (The large ac input impedance of the regulator will not load the oscillator.) A 24 V, 1.0 ampere filament transformer with the audio oscillator connected to the 110 V primary winding is satisfactory for this test. $v_{in} \approx 1.0$ V (rms).

Note 5. Load regulation is specified for small ($\leq$ +17°C) changes in junction temperature. Temperature drift effect must be taken into account separately for conditions of high junction temperature changes due to the thermal feedback that exists on the monolithic chip.

$$\text{Load Regulation} = \frac{V_O|_{I_L = 1.0\ mA} - V_O|_{I_L = 50\ mA}}{V_O|_{I_L = 1.0\ mA}} \times 100$$

Note 6. The resulting low level output signal (v_o) will require the use of a tuned voltmeter to obtain a reading. Special care should be used to insure that the measurement technique does not include connection resistance, wire resistance, and wire lead inductance (i.e., measure close to the case). Note that No. 22 AWG hook-up wire has approximately 4.0 milliohms/in. dc resistance and an inductive reactance of approximately 10 milliohms/in. at 100 kHz. Avoid use of alligator clips or banana plug-jack combination.

GENERAL OPERATING INFORMATION

There is a general tendency to consider a voltage regulator as simply a dc circuit and to prepare breadboard construction accordingly. The excellent high-frequency performance and fast response capability of this integrated-circuit regulator, however, makes extra breadboarding care worthwhile when compared with the limited performance achieved in other regulators when low-frequency transistors are used in the feedback amplifier. Due to the use of VHF transistors in the integrated circuit, some VHF care (short, well-dressed leads) must be exercised in the construction and wiring of circuits ("printed-circuit" boards provide an excellent component interconnection technique).

The circuit must be grounded by a low-inductance connection to the case of the "R" package, or to pin 10 of the "G" package.

A series 4.7-kΩ resistor at Pin 5 (Figure 1) will eliminate any VHF instability problems which may result from lead lengths longer than a few inches at the regulator output. The resistor body should be as close to Pin 5 as physically possible (< 1/2 inch) although the length of the lead to the load is not critical. If temperature stability is of major concern, a 4.7-kΩ resistor should also be placed in series with Pin 6 in order to cancel any drift due to bias current changes.

If long input leads are used, it may be necessary to bypass Pin 3 with a 0.1-μF capacitor (to ground).

The "Shut-Down Control", Pin 2, can be actuated for all possible output voltages and any values of C_o and C_n with no damage to the circuit. The standard logic levels of RTL, DTL, or TTL can be used (see Figure 20). This control can be used to eliminate power consumption by circuit loads which can be put in a "standby" mode, as an ac and dc "squelch" control for communications circuits, and as a dissipation control to protect the regulator under sustained output short-circuiting (see Figures 21 and 25). As the magnitude of the input-threshold voltage at Pin 2 depends directly upon the junction temperature of the IC chip, a fixed dc voltage at Pin 2 will cause automatic shut-down for high junction temperatures (see Figure 23, a and b). This will protect the chip, independent of the heat sinking used, the ambient temperature, or the input or output voltage levels.

Due to the small value of input current at Pin 8, the external resistors, R1 and R2, can be selected with little regard to their parallel resistance. Further, no match to a diffused-resistor temperature coefficient is required; but R1 and R2 should have the same temperature coefficient to keep their ratio independent of temperature.

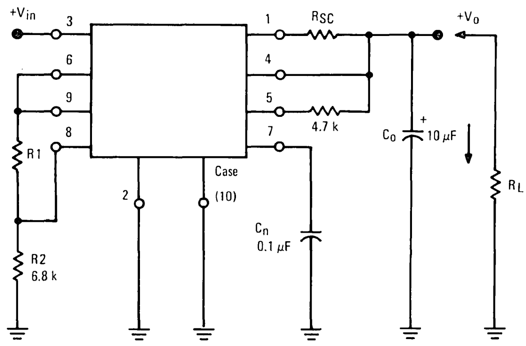
C_n values in excess of 0.1 μF are rarely needed to reduce noise. In cases where more output noise can be tolerated, a smaller capacitor can be used (C_n min. $\approx$ 0.001 μF).

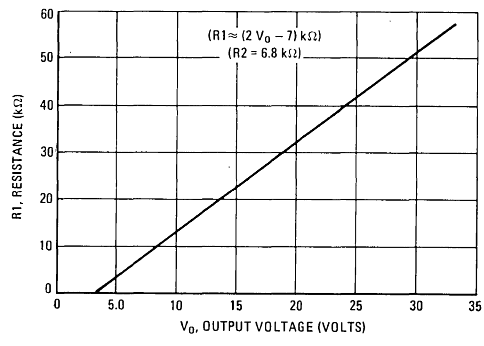
The connection to Pin 5 can be made by a separate lead directly to the load. Thus "remote sensing" can be achieved and undesired impedances (including that of a milliammeter used to measure I_L) can be greatly reduced in their effect on Z_{out}. A 10-ohm resistor placed from pin 1 to pin 5 (close to the IC) will eliminate undesirable lead-inductance effects.

Short-circuit current-limiting is achieved by selecting a value for R_{SC} which will threshold the internal diode string when the desired maximum load current flows (see Figure 5). If the device dissipation and dc safe area limits (Figure 15) are not exceeded, it can be continuously short-circuited at the output without damage.

TYPICAL CONNECTIONS

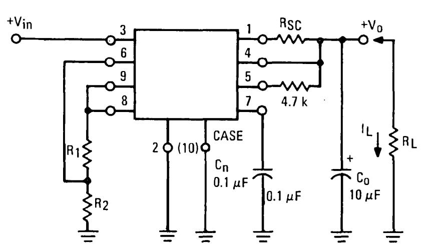
FIGURE 1 – CONNECTION FOR $V_o \geq 3.5$ V

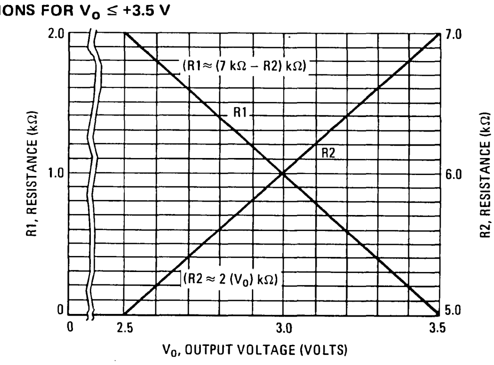




Select R1 to give desired V_o: R1 $\approx$ (2 V_o 7.0) kΩ

FIGURE 2 – CONNECTIONS FOR $V_o \leq +3.5$ V





Select R2 to give desired V_o:
R2 $\approx$ (2 V_o) kΩ
Select R1:
R1 $\approx$ 7.0 kΩ – R2

TYPICAL CHARACTERISTICS

Unless otherwise stated: C_n = 0.1 μF, C_o = 10 μF, $V_{o\ nom}$ = +5.0 Vdc, $V_{in\ nom}$ = +9.0 Vdc, T_C = +25°C, I_L > 200 mA for "R" Package only.

FIGURE 3 – INPUT TRANSIENT RESPONSE

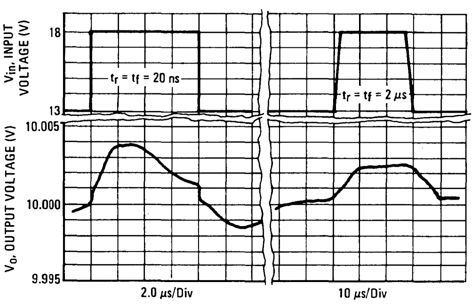


FIGURE 4 – LOAD TRANSIENT RESPONSE

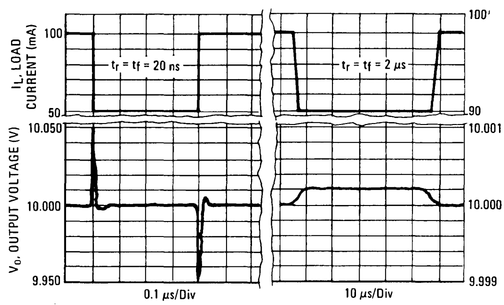


FIGURE 5 – SHORT-CIRCUIT CURRENT versus R_{SC}

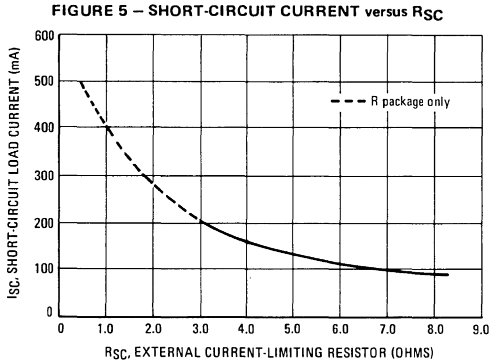


FIGURE 6 – CURRENT-LIMITING CHARACTERISTICS

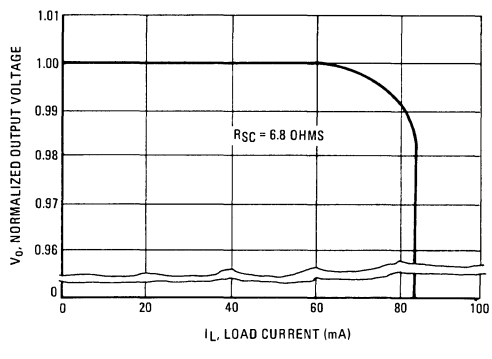


FIGURE 7 – FREQUENCY-DEPENDENCE OF OUTPUT IMPEDANCE

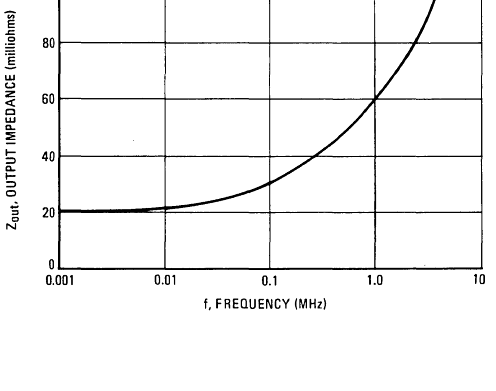
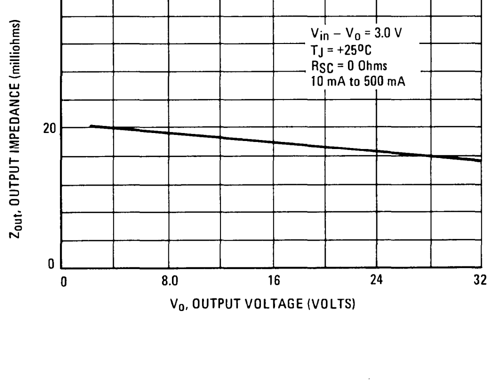


FIGURE 8 – DEPENDENCE OF OUTPUT IMPEDANCE ON OUTPUT VOLTAGE



TYPICAL CHARACTERISTICS (continued)

Unless otherwise stated: C_n = 0.1 μF, C_O = 10 μF, $V_{O\,nom}$ = +5.0 Vdc, $V_{in\,nom}$ = +9.0 Vdc, T_C = +25°C, I_L > 200 mA for "R" Package only.

FIGURE 9 – OUTPUT IMPEDANCE versus R_{SC}

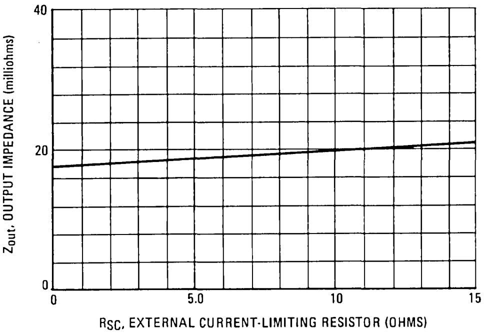


FIGURE 10 – FREQUENCY-DEPENDENCE OF INPUT REGULATION

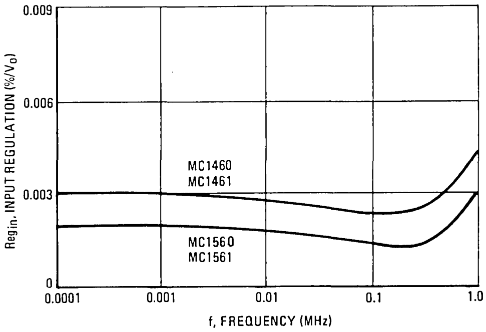


FIGURE 11 – BIAS CURRENT versus INPUT VOLTAGE

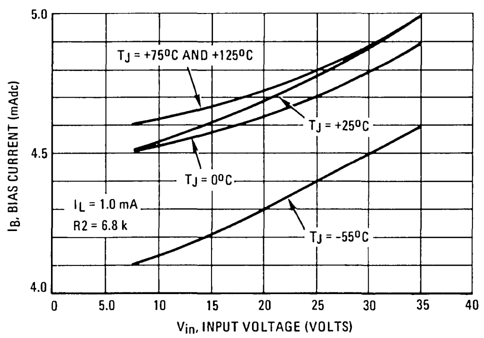


FIGURE 12 – EFFECT OF LOAD CURRENT ON INPUT-OUTPUT VOLTAGE DIFFERENTIAL

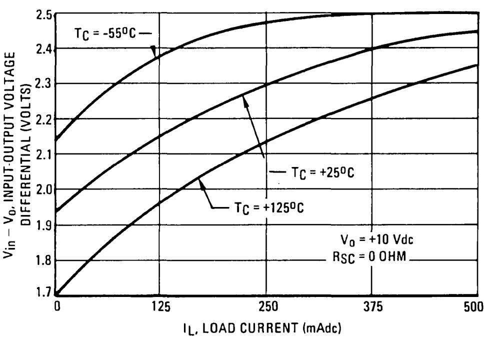


FIGURE 13 – EFFECT OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL ON INPUT REGULATION

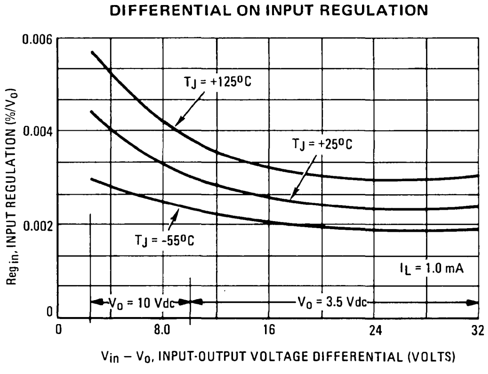
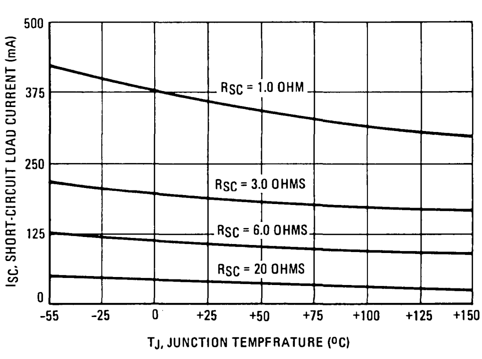


FIGURE 14 – TEMPERATURE DEPENDENCE OF SHORT-CIRCUIT LOAD CURRENT



TYPICAL CHARACTERISTICS (continued)

FIGURE 15a – DC SAFE OPERATING AREA ("G" PACKAGE)

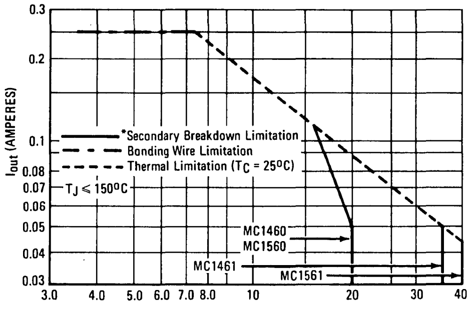
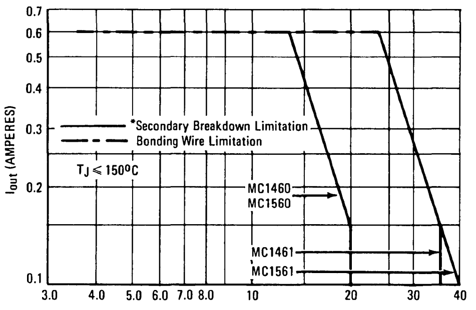


FIGURE 15b – DC SAFE OPERATING AREA ("R" PACKAGE)



*See Application Note AN-415 for an explanation of safe area and second breakdown.

TYPICAL APPLICATIONS

FIGURE 16 – A LABORATORY SUPPLY, 0 TO 25 V

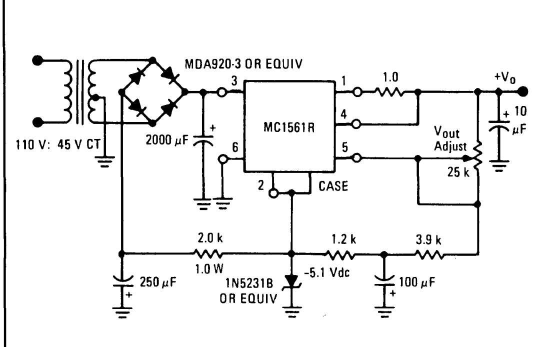


FIGURE 17 – PROVIDING TWO REGULATED OUTPUT VOLTAGES

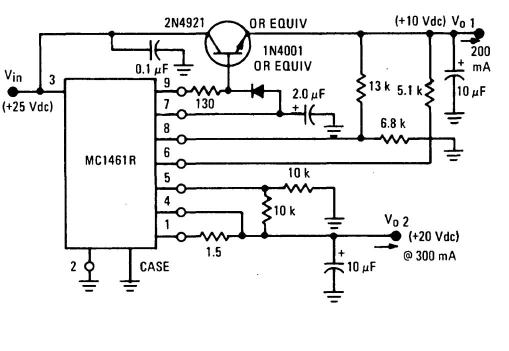
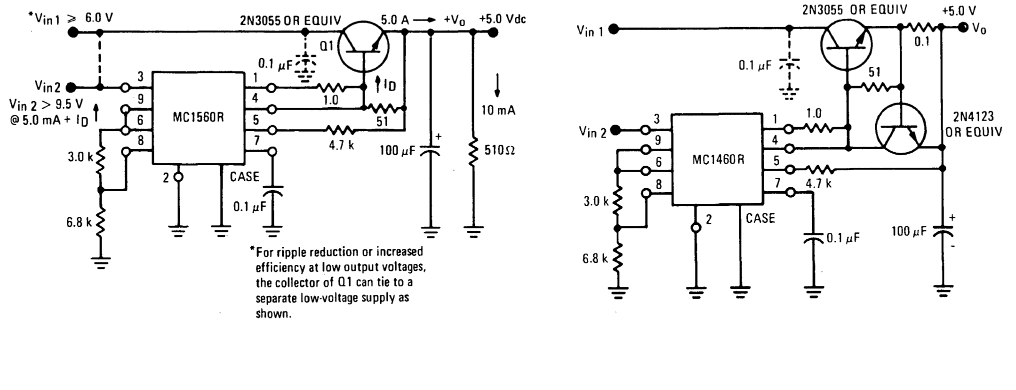


FIGURE 18 – NPN CURRENT BOOST CIRCUITS



TYPICAL APPLICATIONS (continued)

FIGURE 19 – PNP CURRENT BOOST CIRCUIT

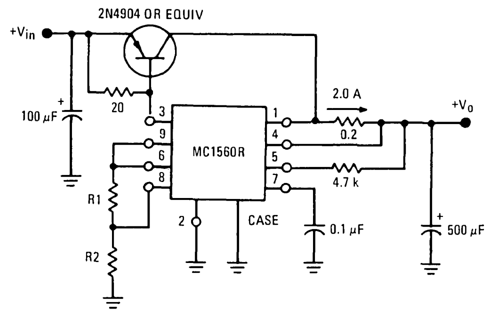


FIGURE 20 – ELECTRONIC SHUT-DOWN USING A MDTL GATE

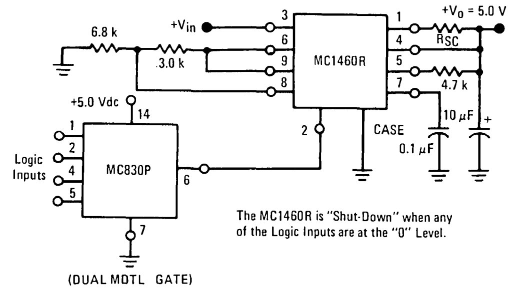
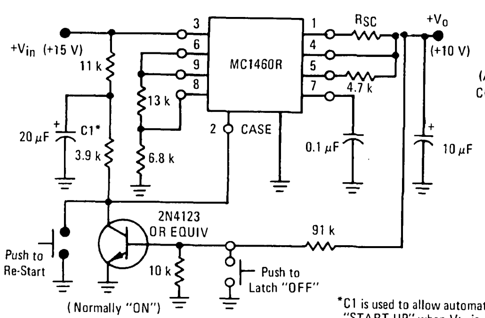


FIGURE 21 – AUTOMATIC LATCH INTO SHUT-DOWN WHEN OUTPUT IS SHORT-CIRCUITED WITH MANUAL RE-START



*C1 is used to allow automatic "START-UP" when V_{in} is first applied.

FIGURE 22 – SCR "CROWBAR" OVER VOLTAGE PROTECTION

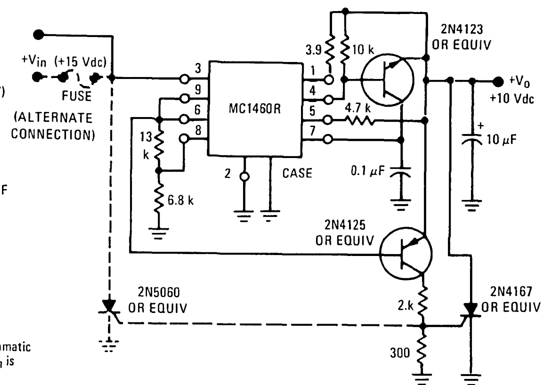
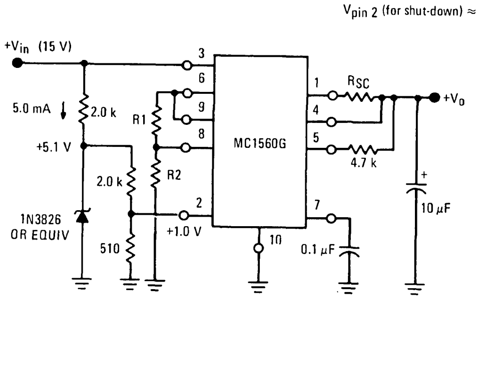


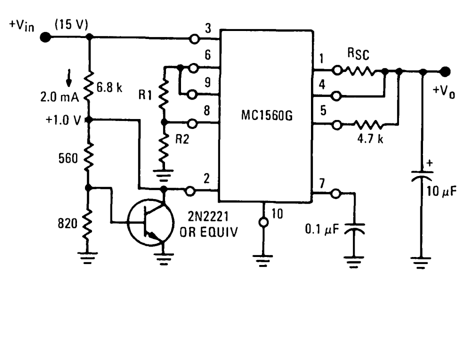
FIGURE 23 – LIMITING MAXIMUM JUNCTION TEMPERATURE

FIGURE a – USING A ZERO TC REFERENCE

FIGURE b – USING A T_A REFERENCE

$V_{pin\ 2}$ (for shut-down) $\approx 1.38 - 3.4 \times 10^{-3}\ (T_J - 25^{\circ}C)$





TYPICAL APPLICATIONS (continued)

FIGURE 24 – THERMAL SHUTDOWN WHEN USING EXTERNAL PASS TRANSISTOR

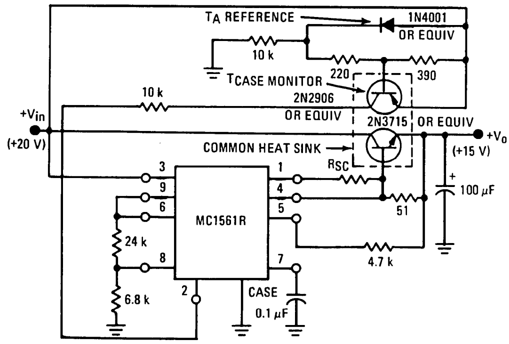


FIGURE 25 – LOW DUTY CYCLE SHORT CIRCUIT PROTECTION WITH AUTOMATIC RESET

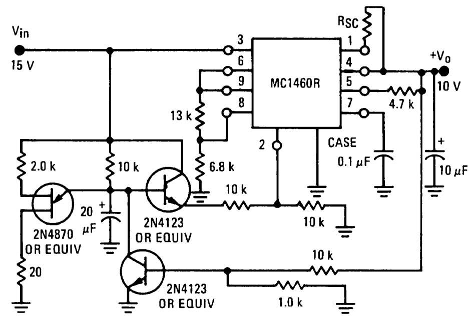


FIGURE 26 – CONNECTION FOR A NEGATIVE OUTPUT VOLTAGE

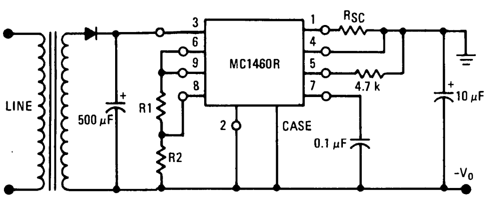


FIGURE 27 – DIGITALLY CONTROLLED 3-TERMINAL NEGATIVE REGULATOR

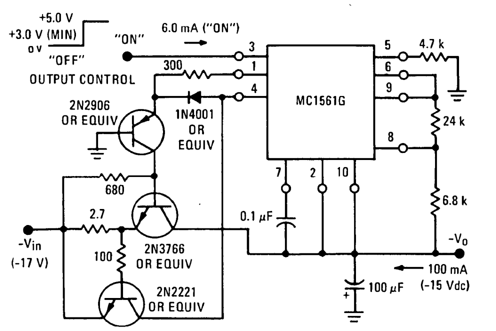
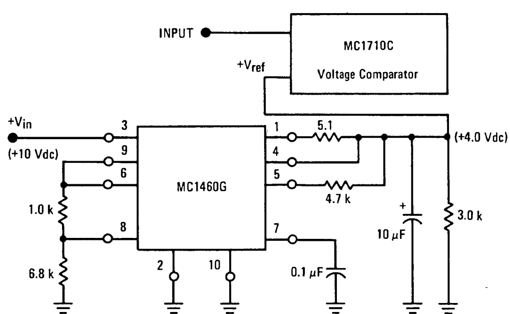


FIGURE 28 – A ZERO TC ADJUSTABLE "ZENER" REFERENCE



GENERAL INFORMATION

Latch-up of these and other regulators can occur if:

1. There are plus and minus voltages available
2. A load exists between Vo^+ and Vo^- (This "common load" may be something inconspicuous –e.g. an operational amplifier. Nearly everyone who uses + and - voltages will have a common load from V^+ to V^-).
3. V_{in}^+ and V_{in}^+ are not applied at the same time.

The above conditions result in one of the two outputs becoming reverse-biased which prevents the regulator from turning "on". Latch-up can be prevented by the circuit configurations shown in Figure 29 and 30.

FIGURE 29

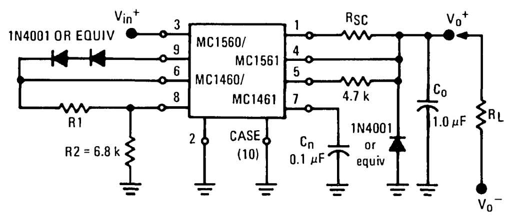
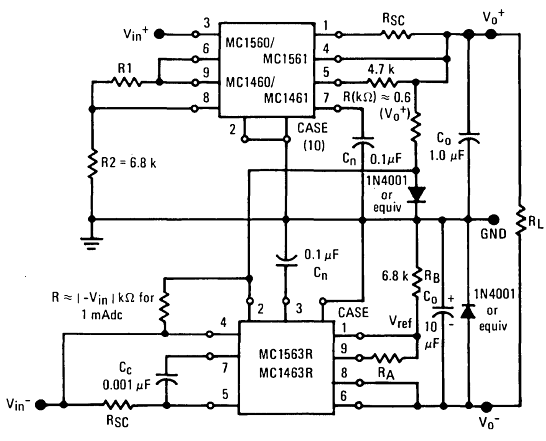


FIGURE 30



VOLTAGE REGULATOR CONSTRUCTION USING THE MC1460, MC1461, MC1560, MC1561 INTEGRATED CIRCUITS

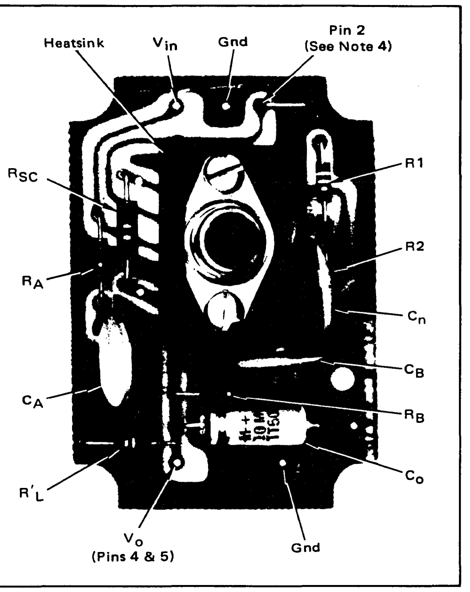


FIGURE 31 – Regulator Layout Using Power Package For Load Currents Up To 500 mA

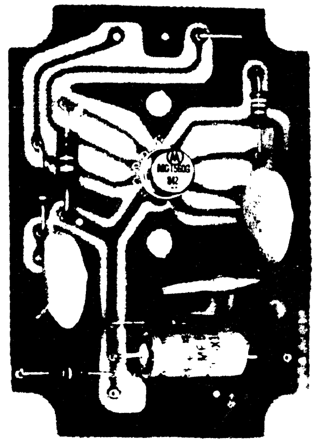


FIGURE 32 – Regulator Layout For Load Currents Up To 200 mA

There is a general tendency to consider a voltage regulator as simply a dc circuit and to prepare circuit layout accordingly. The excellent high-frequency performance and fast response capability of this integrated-circuit regulator, however, makes extra layout care worthwhile. Since short, well-dressed leads must be used, printed-circuit boards provide an excellent component interconnection technique.

The circuit layout, shown in Figure 31 for the "R" or power package IC, applies also to the lower power "G" package circuit shown in Figure 32. The R package circuits will deliver up to 500 mA into a load and the G package, 200 mA.

The circuit schematic, Figure 33, is for output voltages above 3.5 Vdc and the parts list is as follows:

PARTS LIST

Component	Value	Description
R1	Select	1/4 Watt Carbon – See Note 1
R2	6.8 kΩ	1/4 Watt Carbon – See Note 1
R_{SC}	Select	1/2 Watt Carbon – See Note 2
*R_A	3 Ω	1/4 Watt Carbon
*R_B	3 Ω	1/4 Watt Carbon
*R'_L	Select for current of 1 mA minimum	
C_o	10 μF	Sprague 1500 Series, Dickson D10C Series or Equivalent
C_n	0.1 μF	Ceramic Disc – Centralab DDA104, Sprague TG-P10, or Equivalent
*C_A	0.1 μF	Ceramic Disc – Centralab DDA104, Sprague TG-P10, or Equivalent
*C_B	0.1 μF	Ceramic Disc – Centralab DDA104, Sprague TG-P10, or Equivalent
*Heatsink	– Thermalloy #6168 – IERC LB 66B1-77U series	
*Socket	(Not Shown) Robinson Nugent #0001306 Electronic Molding Corp. #6341-210-1, 6348-188-1, 6349-188-1	

*Optional Parts, See Note 3 on next page.

VOLTAGE REGULATOR CONSTRUCTION (continued)

Note 1. The value of R1 is approximately (2 V_O - 7) kΩ, where V_O is the desired output voltage (3.5 V or greater). Optimum temperature stability can be achieved if R1 and R2 have the same temperature coefficient.

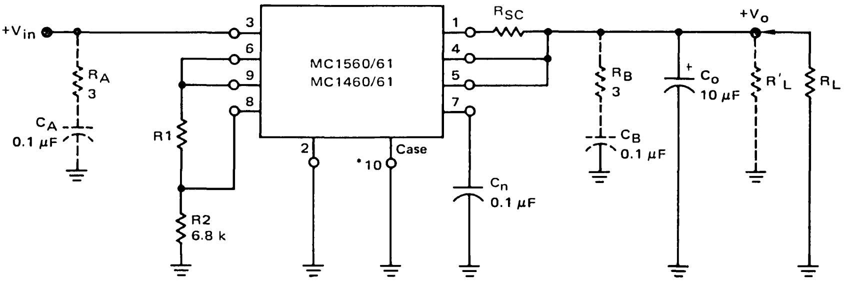
Note 2. R_{SC} is a current sensing resistor for short circuit protection. See Figure 5 for a "Short-Circuit Load Current versus R_{SC}" curve.

Note 3. In cases where long leads are used at the input or output of the regulator, bypass networks R_AC_A and R_BC_B might be necessary to eliminate parasitic oscillation.

With no load, it is possible for a charge to develop on C_O due to leakage currents. R'_L is recommended to insure a minimum load current of 1 mA.

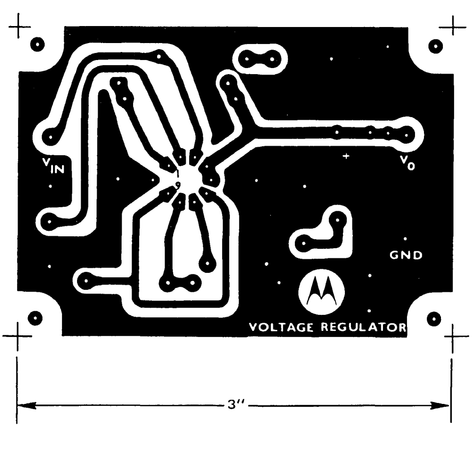
Note 4. It is recommended that Pin 2 (shut-down control) be grounded when not in use. When used, drive current to Pin 2 must be limited to 10 mA maximum.

FIGURE 33 — Schematic of Complete Regulator Showing Both Necessary and Optional Components



*G-Package Pin 10 is ground, R package Case is ground.

FIGURE 34 — Typical Printed Circuit Board Layout



MC1563
MC1463

NEGATIVE VOLTAGE REGULATORS

Specifications and Applications Information

MONOLITHIC NEGATIVE VOLTAGE REGULATOR

The MC1563/MC1463 is a "three terminal" negative regulator designed to deliver continuous load current up to 500 mAdc and provide a maximum negative input voltage of −40 Vdc. Output current capability can be increased to greater than 10 Adc through use of one or more external transistors.

Specifications and performance of the MC1563/MC1463 Negative Voltage Regulator are nearly identical to the MC1569/MC1469 Positive Voltage Regulator. For systems requiring both a positive and negative power supply, these devices are excellent for use as complementary regulators and offer the advantage of operating with a common input ground.

The MC1563R/MC1463R case can be mounted directly to a grounded heat sink which eliminates the need for an insulator.

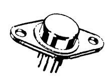
- Case is at Ground Potential (R package)
- Electronic "Shutdown" and Short-Circuit Protection
- Low Output Impedance – 20 Milliohms typ
- High Power Capability – 9.0 Watts
- Excellent Temperature Stability–$TCV_O = \pm 0.002\%/^{\circ}C$ typ
- High Ripple Rejection – 0.002% typ
- 500 mA Current Capability

NEGATIVE-POWER-SUPPLY VOLTAGE REGULATOR INTEGRATED CIRCUIT

SILICON EPITAXIAL PASSIVATED

Pin 4 electrically connected to case through substrate.

G SUFFIX
METAL PACKAGE
CASE 602A

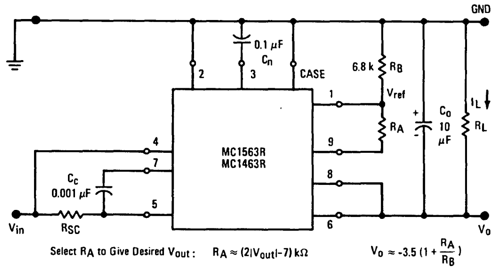


Case is ground terminal

R SUFFIX
METAL PACKAGE
CASE 614

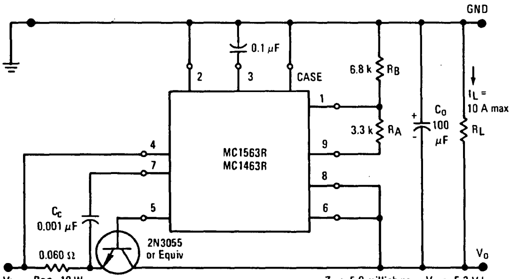
6

FIGURE 1 – TYPICAL CIRCUIT CONNECTION
$|-3.5| \le V_O \le |-37|$ Vdc, $1 \le I_L \le 500$ mA



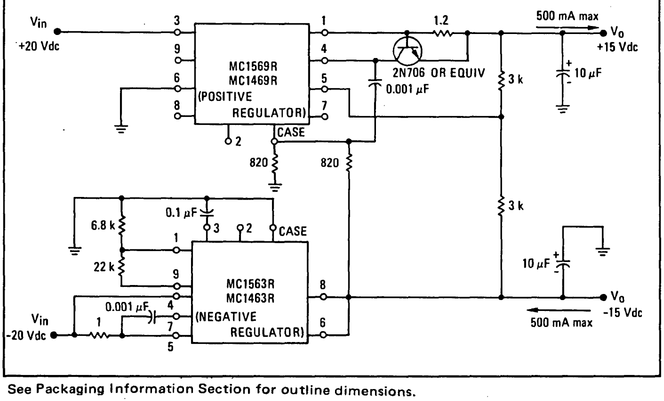
Select R_A to Give Desired V_{out}: $R_A \approx (2|V_{out}|-7)$ kΩ $\quad V_o \approx -3.5\,(1 + \frac{R_A}{R_B})$

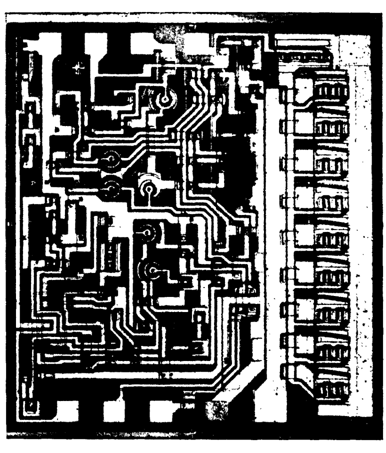
FIGURE 2 – TYPICAL NPN CURRENT BOOST CONNECTION
(V_o = −5.2 Vdc, I_L = 10 Adc [max])



$Z_o \approx 5.0$ milliohms $\quad V_o = -5.2$ Vdc

FIGURE 3 – ±15 V, ±400 mA COMPLEMENTARY TRACKING VOLTAGE REGULATOR





See Packaging Information Section for outline dimensions.
See current MCC1563/1463 data sheet for standard linear chip information.

MAXIMUM RATINGS (T_C = +25°C unless otherwise noted)

Rating	Symbol	Value		Unit
Input Voltage MC1463	V_{in}	−35		Vdc
Input Voltage MC1563	V_{in}	−40		Vdc
		G Package	R Package	
Peak Load Current	I_L pk	250	600	mA
Current, Pin 2	$I_{pin\ 2}$	10	10	mA
Power Dissipation and Thermal Characteristics				
T_A = 25°C	P_D	0.68	2.4	Watts
Derate above T_A = 25°C	$1/\phi_{JA}$	5.44	16	mW/°C
Thermal Resistance, Junction to Air	ϕ_{JA}	184	62	°C/W
T_C = 25°C	P_D	1.8	9.0	Watts
Derate above T_C = 25°C	$1/\phi_{JC}$	14.4	61	mW/°C
Thermal Resistance, Junction to Case	ϕ_{JC}	69.4	17	°C/W
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +175		°C

OPERATING TEMPERATURE RANGE

Ambient Temperature MC1463	T_A	0 to +75	°C
Ambient Temperature MC1563		-55 to +125	

ELECTRICAL CHARACTERISTICS (I_L = 100 mAdc, T_C = +25°C unless otherwise noted.)

Characteristic	Fig.	Note	Symbol	MC1563 Min	MC1563 Typ	MC1563 Max	MC1463 Min	MC1463 Typ	MC1463 Max	Unit
Input Voltage (T_A = T_{low} ① to T_{high} ②)	4	1	V_{in}	−8.5	–	−40	−9.0	–	−35	Vdc
Output Voltage Range	4	–	V_O	−3.6	–	−37	−3.8	–	−32	Vdc
Reference Voltage (Pin 1 to Ground)	4	–	V_{ref}	−3.4	−3.5	−3.6	−3.2	−3.5	−3.8	Vdc
Minimum Input-Output Voltage Differential (R_{SC} = 0)	4	2	$\|V_{in} - V_O\|$	–	1.5	2.7	–	1.5	3.0	Vdc
Bias Current (I_L = 1.0 mAdc, $I_b = I_{in} - I_L$)	4	–	I_b	–	7.0	11	–	7.0	14	mAdc
Output Noise (C_n = 0.1 µF, f = 10 Hz to 5.0 MHz)	4	–	v_n	–	120	–	–	120	–	µV(rms)
Temperature Coefficient of Output Voltage	4	3	TCV_O	–	±0.002	–	–	±0.002	–	%/°C
Operating Load Current Range	4	–	I_L							mAdc
(R_{SC} = 0.3 ohm) R Package				1.0	–	500	1.0	–	500	
(R_{SC} = 2.0 ohms) G Package				1.0	–	200	1.0	–	200	
Input Regulation	6	4	Reg_{in}	–	0.002	0.015	–	0.003	0.030	%/V_O
Load Regulation	7	5	Reg_L							
(T_J = Constant [1.0 mA ⩽ I_L ⩽ 20 mA])				–	0.4	1.6	–	0.7	2.4	mV
(T_C = +25°C [1.0 mA ⩽ I_L ⩽ 50 mA]) R Package				–	0.005	0.05	–	0.005	0.05	%/V_O
G Package				–	0.01	0.13	–	0.01	0.13	
Output Impedance (f = 1.0 kHz)	8	6	Z_O	–	20	80	–	35	120	milliohms
Shutdown Current (V_{in} = −35 Vdc)	9	–	I_{sd}	–	7.0	15	–	14	50	µAdc

① T_{low} = 0°C for MC1463
= -55°C for MC1563

② T_{high} = +75°C for MC1463
= +125°C for MC1563

Note 1. "Minimum Input Voltage" is the minimum "total instantaneous input voltage" required to properly bias the internal zener reference diode.

Note 2. This parameter states that the MC1563/MC1463 will regulate properly with the input-output voltage differential $|V_{in} - V_o|$ as low as 2.7 Vdc and 3.0 Vdc respectively. Typical units will regulate properly with $|V_{in} - V_o|$ as low as 1.5 Vdc as shown in the typical column.

Note 3. "Temperature Coefficient of Output Voltage" is defined as:

$$TC_{V_o} = \frac{\pm(V_{o\ max} - V_{o\ min})\ (100)}{\Delta\ T_A\ (V_o\ @\ T_A = +25^oC)}$$

where $\Delta\ T_A$ = +180°C for the MC1563
+75°C for the MC1463

The output-voltage adjusting resistors (R_A and R_B) must have matched temperature characteristics in order to maintain a constant ratio independent of temperature.

Note 4. The input signal can be introduced by use of a transformer which will allow the output of an audio oscillator to be coupled in series with the dc input to the regulator. (The large ac input impedance of the regulator will not load the oscillator.) A 24 V, 1.0 ampere filament transformer with the audio oscillator connected to the 110 V primary winding is satisfactory for this test. ($v_{in} \approx 1.0$ V [rms])

Note 5. Temperature drift effect must be taken into account separately for conditions of high junction temperature changes due to the thermal feedback that exists on the monolithic chip.

$$\text{Load Regulation} = \frac{V_o\,|\,I_L = 1.0\,\text{mA} - V_o\,|\,I_L = 50\,\text{mA}}{V_o|I_L = 1.0\,\text{mA}} \times 100$$

Note 6. The resulting low-level output signal (v_o) will require the use of a tuned voltmeter to obtain a reading. Special care should be used to insure that the measurement technique does not include connection resistance, wire resistance, and wire lead inductance (i.e., measure close to the case). Note that No. 22 AWG hook-up wire has approximately 4.0 milliohms/inch dc resistance and an inductive reactance of approximately 10 milliohms/inch at 100 kHz. Avoid use of alligator clips or banana plug-jack combination.

TEST CIRCUITS

(I_L = 100 mAdc, T_C = +25°C unless otherwise noted)

FIGURE 4 — GENERAL TEST CIRCUIT

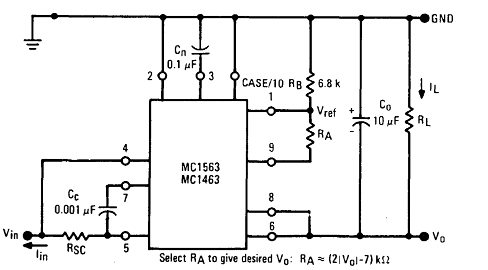


FIGURE 5 — LOAD TRANSIENT RESPONSE

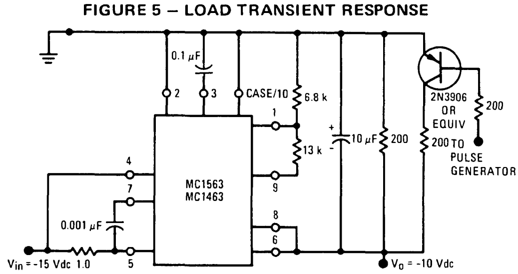


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FIGURE 6 — INPUT REGULATION

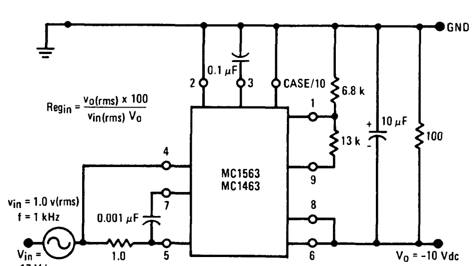


FIGURE 7 — LOAD REGULATION

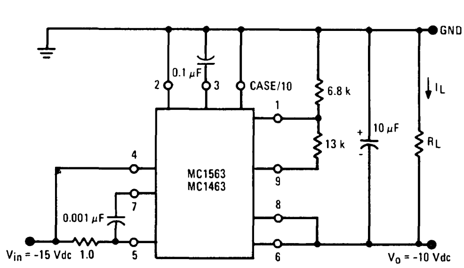


FIGURE 8 — OUTPUT IMPEDANCE

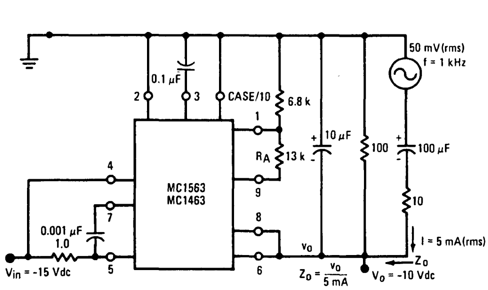
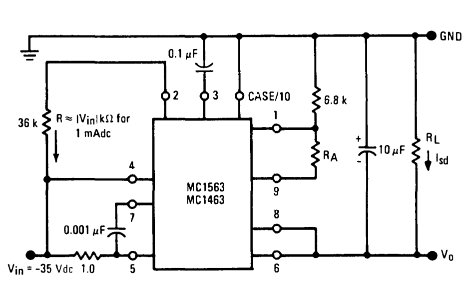


FIGURE 9 — SHUTDOWN CURRENT



GENERAL DESIGN INFORMATION

1. Output Voltage, V_O
   a) Output Voltage is set by resistors R_A and R_B (see Figure 10). Set R_B = 6.8 k ohms and determine R_A from the graph of Figure 11 or from the equation:

   $$R_A \approx (2|V_O|-7)\ k\Omega$$

   b) Output voltage can be varied by making R_A adjustable as shown in Figures 10 and 11.

   c) Output voltage, V_O, is determined by the ratio of R_A and R_B therefore optimum temperature performance can be achieved if R_A and R_B have the same temperature coefficient.

2. Short-Circuit Current, I_{SC}
   Short-Circuit Current, I_{SC}, is determined by R_{SC}. R_{SC} may be chosen with the aid of Figure 12 when using the typical circuit connection of Figure 10. See Figure 29 for current limiting during NPN current boost.

3. Compensation, C_c
   A 0.001 µF capacitor (C_c, see Figure 10), will provide adequate compensation in most applications, with or without current boost. Smaller values of C_c will reduce stability and larger values of C_c will degrade pulse response and output impedance versus frequency. The physical location of C_c should be close to the MC1563/MC1463 with short lead lengths.

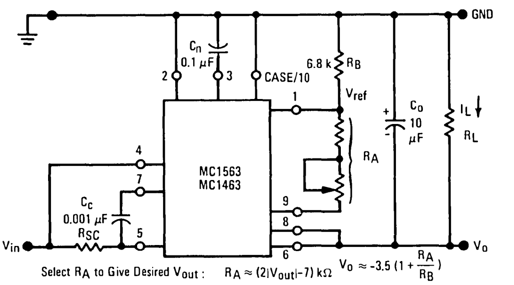
4. Noise Filter Capacitor, C_n
   A 0.1 µF capacitor, C_n, from pin 3 to ground will typically reduce the output noise voltage to 120 µV(rms). The value of C_n can be increased or decreased, depending on the noise voltage requirements of a particular application. A minimum value of 0.001 µF is recommended.

5. Output Capacitor, C_O
   The value of C_O should be at least 10 µF in order to provide good stability.

6. Shutdown Control
   One method of turning "OFF" the regulator is to draw 1 mA from pin 2 (see Figure 9). This control can be used to eliminate power consumption by circuit loads which can be put in "standby" mode. Examples include, an ac or dc "squelch" control for communications circuits, and a dissipation control to protect the regulator under sustained output short-circuiting. As the magnitude of the input-threshold voltage at pin 2 depends directly upon the junction temperature of the integrated circuit chip, a fixed dc voltage at pin 2 will cause automatic shutdown for high junction temperatures (see Figure 37). This will protect the chip, independent of the heat sinking used, the ambient temperature, or the input or output voltage levels. Standard logic levels of MECL, MRTL, MDTL or MTTL can also be used to turn the regulator "ON" or "OFF" (see Figures 32 and 33).

7. Remote Sensing
   The connection to pin 8 can be made with a separate lead direct to the load. Thus, "remote sensing" can be achieved and the effect of undesired impedances (including that of the milliammeter used to measure I_L) on Z_{out} can be greatly reduced (see Figure 35).

FIGURE 10 — TYPICAL CIRCUIT CONNECTION



Select R_A to Give Desired V_{out}: $R_A \approx (2|V_{out}|-7)\ k\Omega$ $V_O \approx -3.5\,(1 + \frac{R_A}{R_B})$

FIGURE 11 — R_A versus V_O

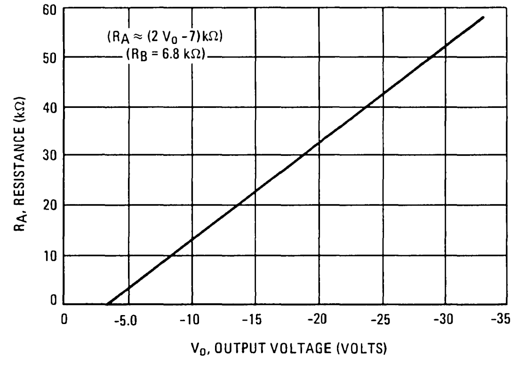
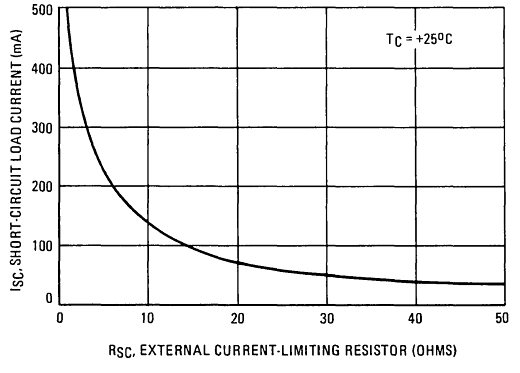


FIGURE 12 — I_{SC} versus R_{SC}



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TYPICAL CHARACTERISTICS

Unless otherwise noted: $C_n = 0.1\,\mu F$, $C_c = 0.001\,\mu F$, $C_o = 10\,\mu F$, $T_C = +25^oC$, $V_{in(nom)} = -15$ Vdc, $V_{o(nom)} = -10$ Vdc, $I_L = 100$ mAdc

FIGURE 13 – TEMPERATURE DEPENDENCE OF SHORT-CIRCUIT LOAD CURRENT

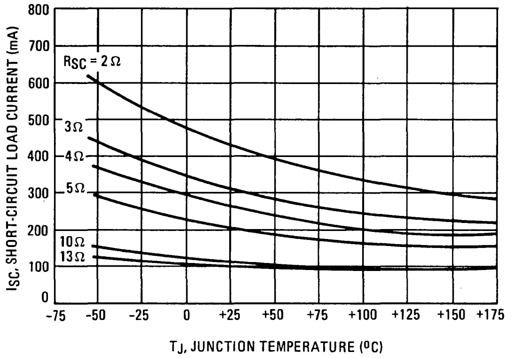


FIGURE 14 – FREQUENCY DEPENDENCE OF OUTPUT IMPEDANCE

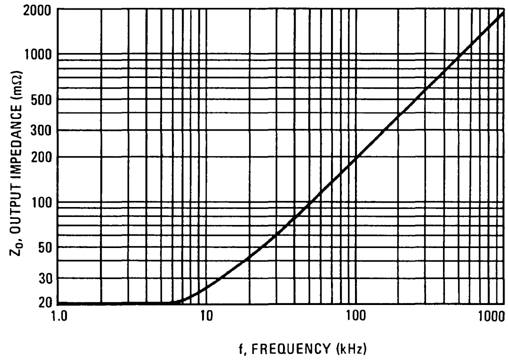


FIGURE 15 – DEPENDENCE OF OUTPUT IMPEDANCE ON OUTPUT VOLTAGE

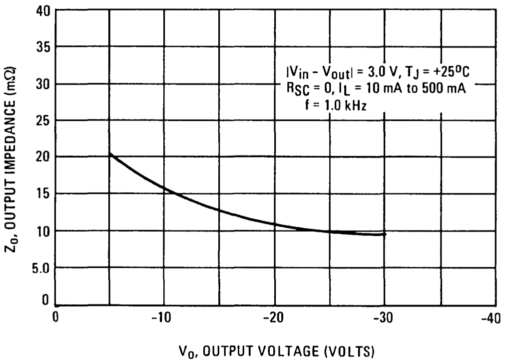


FIGURE 16 – OUTPUT IMPEDANCE versus R_{SC}

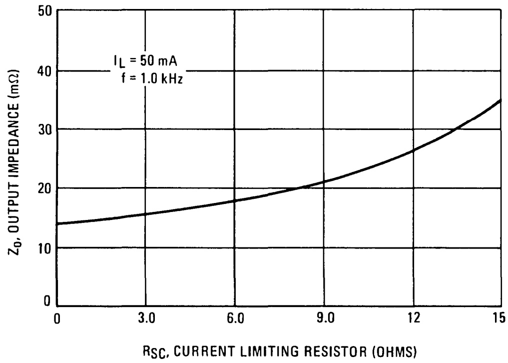


FIGURE 17 – FREQUENCY DEPENDENCE OF INPUT REGULATION

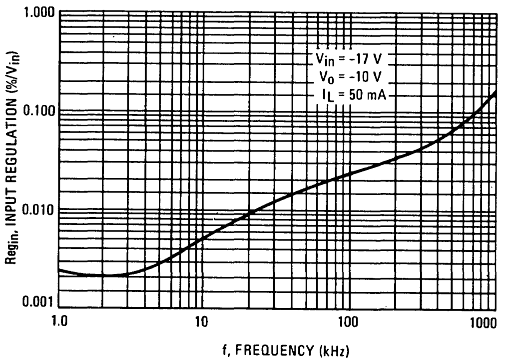


FIGURE 18 – CURRENT LIMITING CHARACTERISTICS

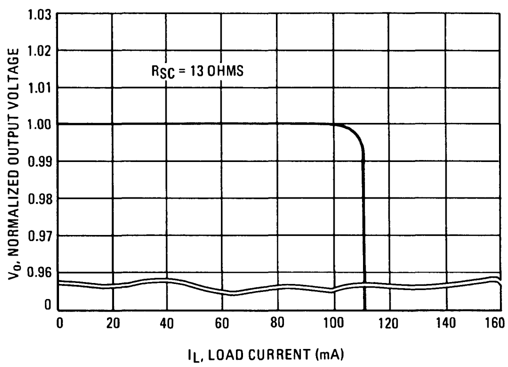


FIGURE 19 – BIAS CURRENT versus INPUT VOLTAGE

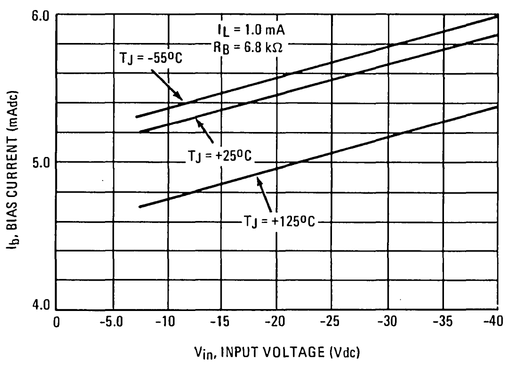


FIGURE 20 – EFFECTS OF LOAD CURRENT ON INPUT-OUTPUT VOLTAGE DIFFERENTIAL

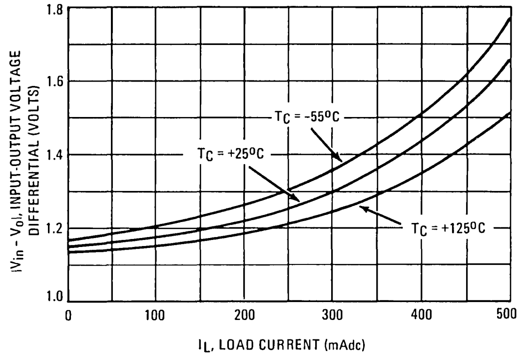


FIGURE 21 – EFFECT OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL ON INPUT REGULATION

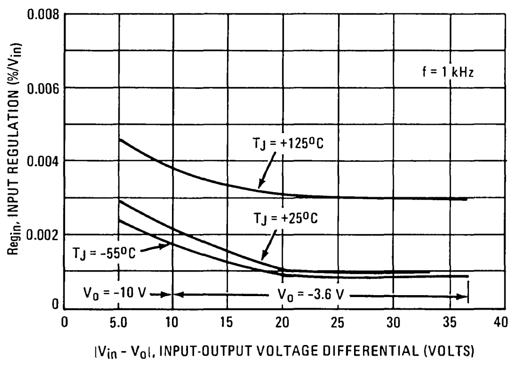


FIGURE 22 – INPUT TRANSIENT RESPONSE

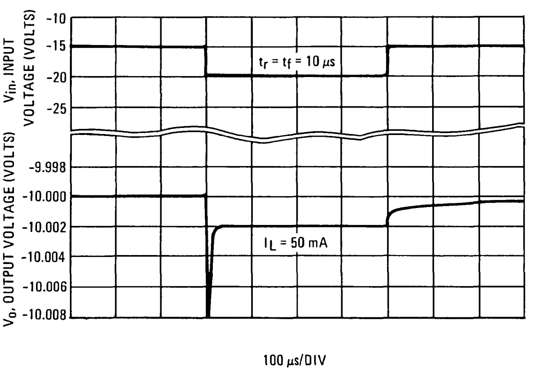


FIGURE 23 – LOAD TRANSIENT RESPONSE

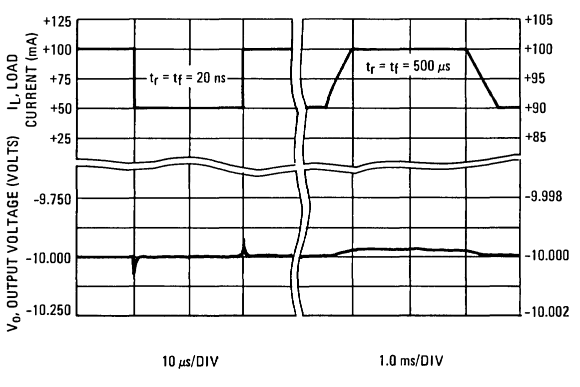
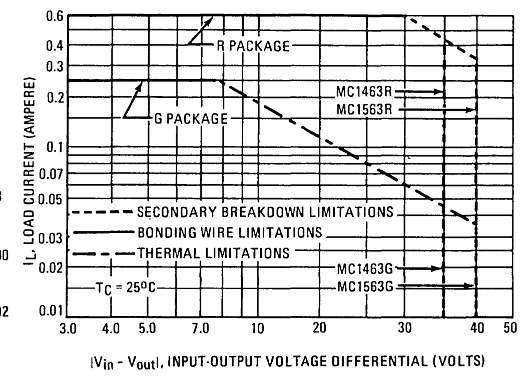


FIGURE 24 – DC SAFE OPERATING AREA



OPERATIONS AND APPLICATIONS

This section describes the operation and design of the MC1563 negative voltage regulator and also provides information on useful applications.

SUBJECT SEQUENCE

THEORY OF OPERATION

The usual series voltage regulator shown in Figure 25, consists of a reference voltage, an error amplifier, and a series control element. The error amplifier compares the output voltage with the reference voltage and adjusts the output accordingly until the error is essentially zero. For applications requiring output voltages larger than the reference, there are two options. The first is to use a resistive divider across the output and compare only a fraction of the output voltage to the reference. This approach suffers from reduced feedback to the error amplifier due to the attenuation of the resistive divider. This degrades load regulation especially at high voltage levels.

The alternative is to eliminate the resistive divider and to shift the reference voltage instead. To accomplish this, another amplifier is employed to amplify (or level shift) the reference voltage using an operational amplifier as shown in Figure 26. The gain-determining resistors may be external, enabling a wide range of output voltages. This is exactly the same approach used in the first option. That is, the output is being resistively divided to match the reference voltage. There is however, one big difference in that the output of this "regulator" is driving the input of another regulator (the error amplifier). The output of the reference amplifier has a relatively low impedance as compared to the input impedance of the error amplifier. Changes in the load of the output of the error amplifier are buffered to the extent that they have virtually no effect on the reference amplifier. If the feedback resistors are external (as they are on the MC1563) a wide range of reference voltages can be established.

The error amplifier can now be operated at unity gain to provide excellent regulation. In fact, this "regulator-within-a-regulator" concept permits the load regulation to be specified in terms of output impedance rather than as some percentage change of the output voltage. This approach was used in the design of the MC1563 negative voltage regulator.

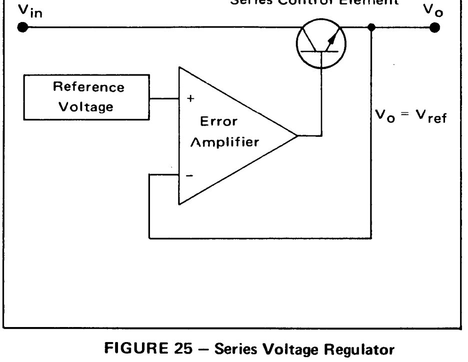


FIGURE 25 – Series Voltage Regulator

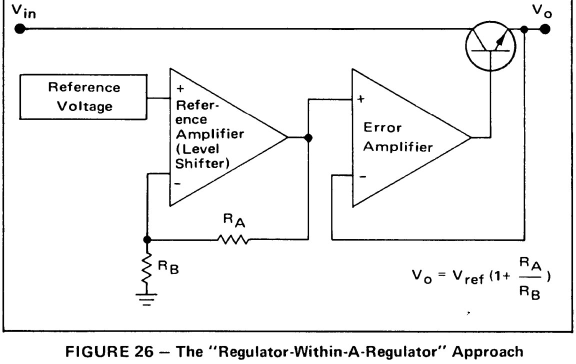
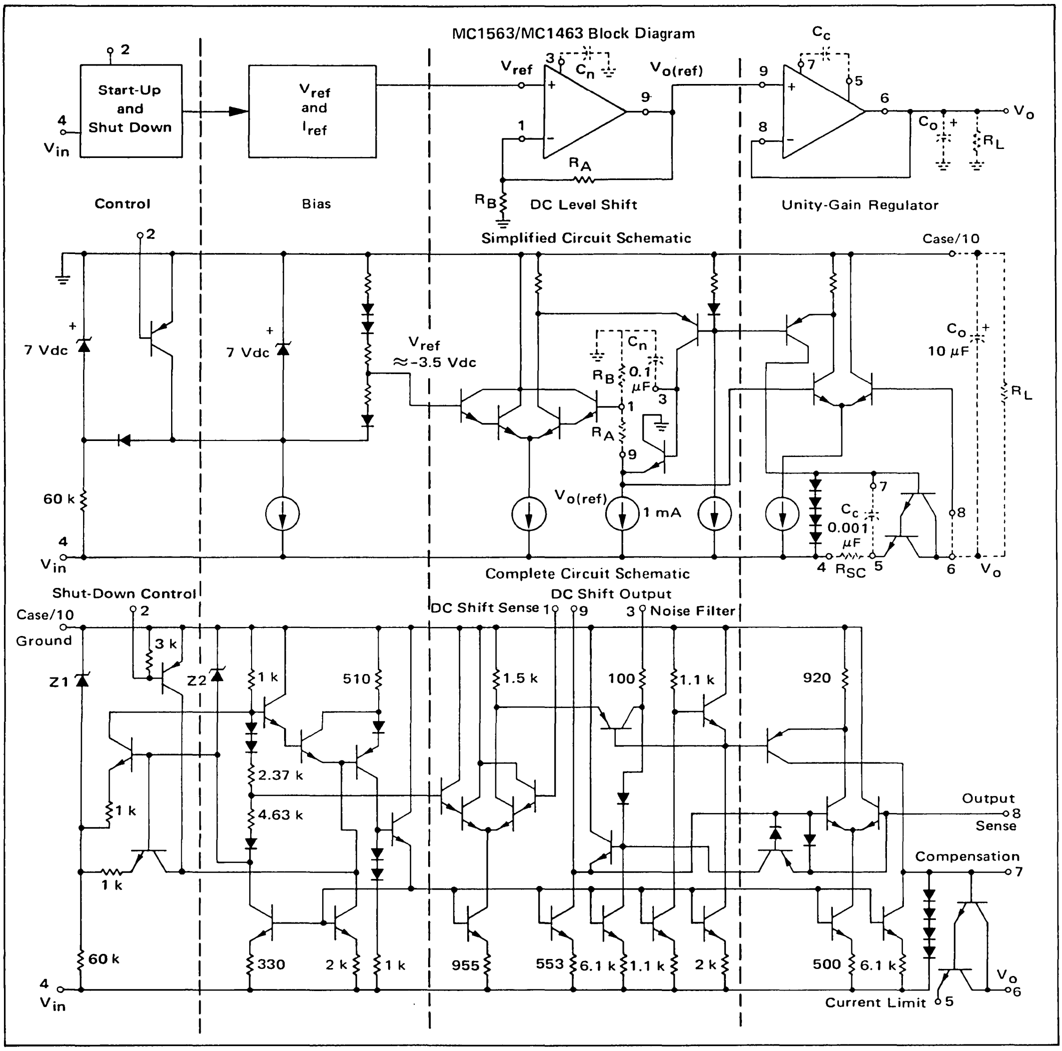


FIGURE 26 – The "Regulator-Within-A-Regulator" Approach

FIGURE 27
(Recommended External Circuitry is Depicted With Dotted Lines.)



MC1563 Operation

Figure 27 shows the MC1563 Negative Regulator block diagram, simplified schematic, and complete schematic. The four basic sections of the regulator are: Control, Bias, DC Level Shift, and Output (unity gain) Regulator. Each section is detailed in the following paragraphs.

Control

The control section involves two basic functions, start-up and shutdown. A start-up function is required since the biasing is essentially independent of the unregulated input voltage. It makes use of two zener diodes having the same breakdown voltage. A first or auxiliary zener is driven directly from the input voltage line through a resistor (60 kΩ) and permits the regulator to initially achieve the desired bias conditions. This permits the second, or reference zener to be driven from a current source. When the reference zener enters breakdown, the auxiliary zener is isolated from the rest of the regulator circuitry by a diode disconnect technique. This is necessary to keep the added noise and ripple of the auxiliary zener from degrading the performance of the regulator.

The shutdown control, in effect, consists of a PNP transistor across the reference zener diode. When this transistor is turned "ON", via pin 2, the reference voltage is reduced to essentially zero volts and the regulator is forced to shutdown. During shutdown the current drain of the complete IC regulator drops to $V_{in}/60\ k\Omega$ or 500 μA for a -30 V input.

Bias

A zener diode is the main reference element and forms the heart of the bias circuitry. Its positive temperature coefficient is balanced by the negative temperature coefficients of forward biased diodes in a ratio determined by the resistors in the diode string. The result is a reference voltage of approximately -3.5 Vdc with a typical temperature coefficient of 0.002%/°C. In addition, this circuit also provides a reference current which is used to bias all current sources in the remaining regulator circuitry.

DC Level Shift

The reference voltage is used as the input to a Darlington differential amplifier. The gain of this amplifier is quite high and it therefore may be considered to function as a conventional operational amplifier. Consequently, negative feedback can be employed using two external resistors (R_A and R_B) to set the closed-loop gain and to boost the reference voltage to the desired output voltage. A capacitor, C_n, is introduced externally into the level shift network (via pin 3) to stabilize the amplifier and to filter the zener noise. The recommended value for this capacitor is 0.1 μF and should have a voltage rating in excess of the desired output voltage. Smaller capacitors (0.001 μF minimum) may be used but will cause a slight increase in output noise. Larger values of C_n will reduce the noise as well as delay the start-up of the regulator.

Output Regulator

The output of the shift amplifier is fed internally to the noninverting input of the output error amplifier. The inverting input to this amplifier is the Output Sense connection (pin 8) of the regulator. A Darlington connected NPN power transistor is used to handle the load current. The short-circuit current limiting resistor, R_{SC}, is connected in the emitter of this transistor to sample the full load current. This connection enables a four-diode string to limit the drive current to the power transistors in a conventional manner. Four diodes are provided to accommodate the use of an external NPN transistor when used to boost the output current. There is approximately one diode drop across the external current limiting resistor, R_{SC}. When two NPN transistors are cascaded, an extra external diode must be added in series with pin 4 to compensate for the added V_{BE} drop.

Stability and Compensation

As has been seen, the MC1563 employs two amplifiers, each using negative feedback. This implies the possibility of frequency instability due to excessive phase shift at high frequencies. Since the error amplifier is normally used at unity gain (the worst case for stability) a high impedance node is brought out for compensation. For normal operation, a capacitor is connected between this point (pin 7) and pin 5. The recommended value of 0.001 μF will insure stability and still provide acceptable transient response (see Figure 23). It is also necessary to use an output capacitor, C_o, (typically 10 μF) directly from the output (pin 6) to ground. When an external transistor is used to boost the current, C_o = 100 μF is recommended (see Figure 28).

NPN CURRENT BOOSTING

For applications requiring more than 500 mA of load current, or for minimizing voltage variations due to temperature changes in the IC regulator arising from changes of the internal power dissipation, the NPN current-boost circuits of Figure 2 or 28, are recommended. The transistor shown in Figure 28, the 2N3771 (or MJ3771), can supply currents to 10 amperes (subject, of course, to the safe area limitations). This circuit, when used for a -10 V

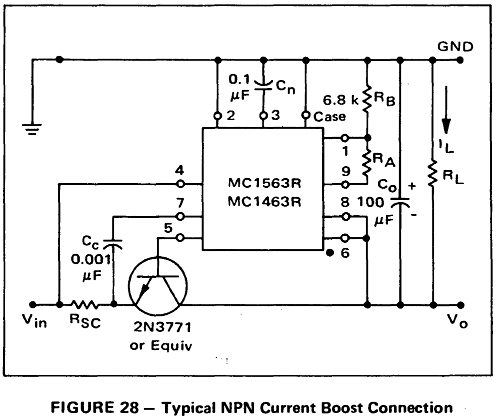


FIGURE 28 — Typical NPN Current Boost Connection

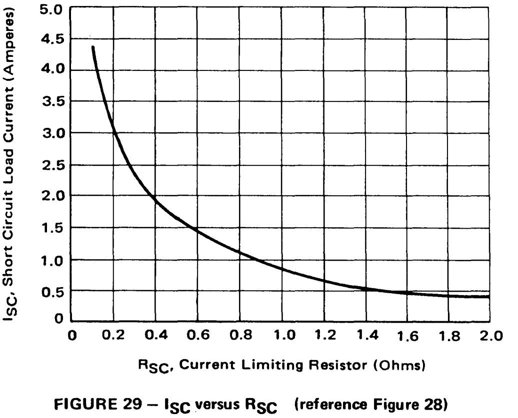


FIGURE 29 — I_{SC} versus R_{SC} (reference Figure 28)

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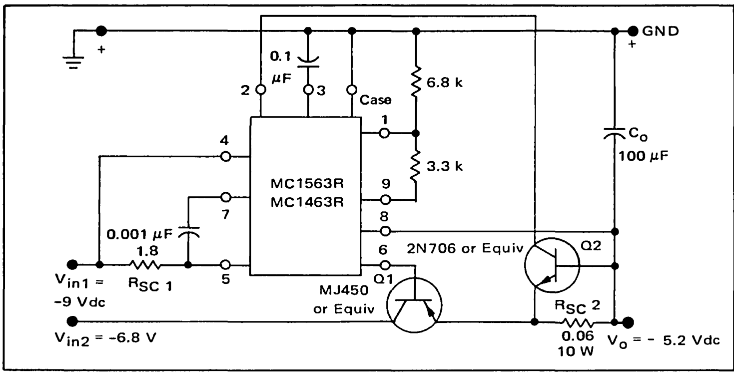

FIGURE 30 – PNP Current Boost Connection

output (R_A = 13 kΩ) supply and operating with a -15 V input, with a R_{SC} of 0.1 Ω, will yield a change in output voltage of only 26 mV over a load current range of from 1 mA to 3.5 A. This corresponds to a dc output impedance of only 7.5 milliohms or a percentage load regulation of 0.26% for a full 3.5-ampere load current change. Figure 29, indicates how the short circuit current varies with the value of R_{SC} for this circuit.

PNP CURRENT BOOSTING

A PNP power transistor can also be used to boost the load current capabilities. To improve the efficiency of the PNP boost configuration, particularly for small output voltages, the circuit of Figure 30, is recommended. An auxiliary -9 volt supply is used to power the IC regulator and the heavy load current is obtained from a second supply of lower voltage. For the 10-ampere regulator of Figure 30 this represents a savings of 22 watts when compared with operating the regulator from the single -9 V supply. It can supply current to 10 amperes while requiring an input voltage to the collector of the pass transistor of -6.8 volts minimum. The pass transistor is limited to 10 amperes by the added short-circuit current network in its emitter (R_{SC2}) and the IC regulator is limited to 400 mA in the conventional manner (R_{SC1}). The MJ450 exhibits a minimum h_{FE} of 30 at 10 amperes, thus requiring only 333 mA from the MC1563. Regulation of this circuit is comparable to that of the NPN boost configuration.

For higher output voltages the additional unregulated power supply is not required. The collector of the PNP boost transistor can tie directly to pin 5 and the internal current limit circuit will provide short-circuit protection using R_{SC} (see Figure 12). Transistor Q2 and R_{SC2} will not be required.

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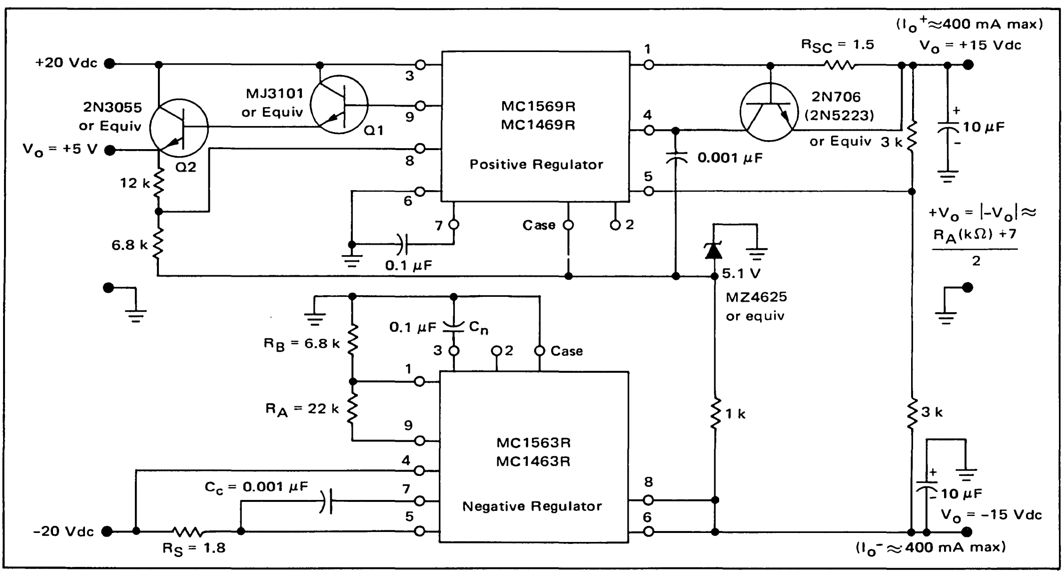
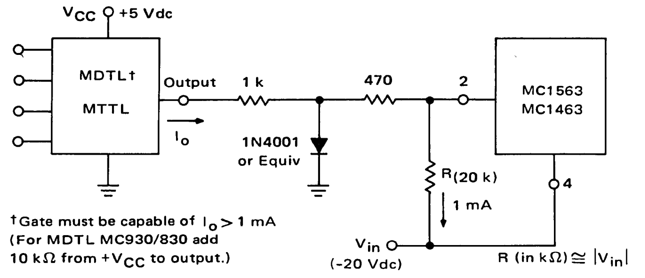


FIGURE 31 – A ±15 Vdc Complementary Tracking Regulator With Auxiliary +5.0 V Supply

FIGURE 32 – Saturated Logic Level Shutdown Circuit



POSITIVE AND NEGATIVE POWER SUPPLIES

If the MC1563 is driven from a floating source it is possible to use it as a positive regulator by grounding the negative output terminal. The MC1563 may also be used with the MC1569 to provide completely independent positive and negative power regulators with comparable performance.

Some applications may require complementary tracking in which both supplies arrive at the voltage level simultaneously, and variations in the magnitudes of the two voltages track. Figures 3 and 31 illustrate this approach. In this application, the MC1563 is used as the reference regulator, establishing the negative output voltage. The MC1569 positive regulator is used in a tracking mode by grounding one side of the differential amplifier (pin 6 of the MC1569) and using the other side (pin 5 of the MC1569) to sense the voltage developed at the junction of the two 3 k-ohm resistors. This differential amplifier controls the MC1569 series pass transistor such that the voltage at pin 5 will be zero. When the voltage at pin 5 equals zero, $+|V_O|$ must equal $-|V_O|$.

For the configuration shown in Figure 31, the level shift amplifier in the MC1569 is employed to generate an auxiliary +5 volt supply which is boosted to a 2-ampere capability by Q1 and Q2. (The +5 volt supply, as shown, is not short-circuit protected.) The -15 volt supply varies less than 0.1 mV over a zero to -300 mAdc current range and the +15 volt supply tracks this variation. The +15 volt supply varies 20 mV over the zero to +300 mAdc load current range. The +5 volt supply varies less than 5 mV for $0 \leqslant I_L \leqslant 200$ mA with the other two voltages remaining unchanged.

SHUTDOWN TECHNIQUES

Pin 2 of the MC1563 is provided for the express purpose of shutting the regulator "OFF". Referring to the schematic, it can be seen that pin 2 goes to the base of a PNP transistor; which, if turned "ON", will deny current to all the biasing current sources. This action causes the output to go to essentially zero volts and the only current drawn by the IC regulator will be the small start current through the 60 k-ohm start resistor (V_{in}/60 kΩ). This feature provides additional versatility in the applications of the MC1563. Various sub-systems may be placed in a "standby" mode to conserve power until actually needed. Or the power may be turned "OFF" in response to other occurrences such as over-heating, over-voltage, shorted output, etc.

As an illustration of the first case, consider a system consisting of both positive-supply logic (MTTL) and negative-supply logic (MECL). The MECL logic may be used in a high-speed arithmetic processor whose services are not continuously required. Substantial power may

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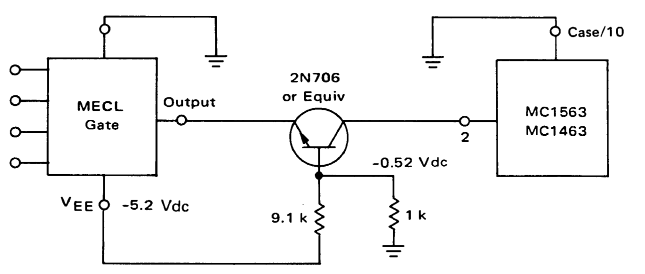
FIGURE 33 – MECL Logic Level Shutdown Circuit



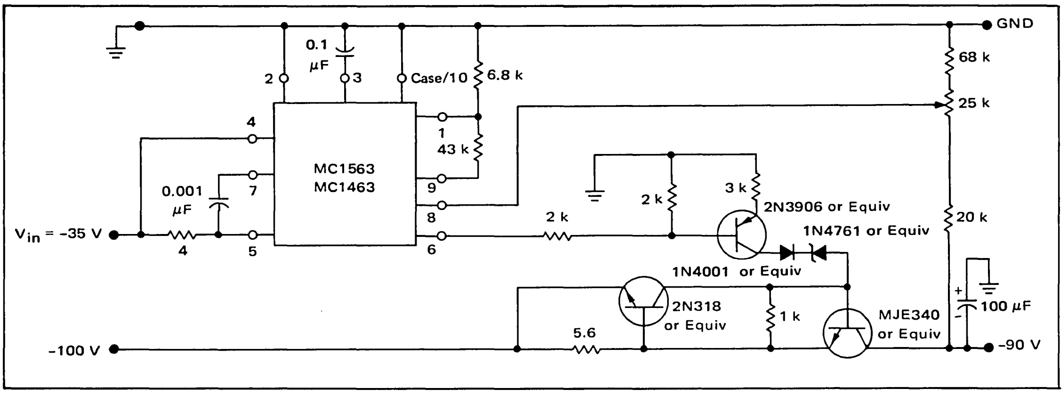


FIGURE 34 — Voltage Boosting Circuit

thus be conserved if the MECL circuitry remains unpowered except when needed. The negative regulator can be shutdown using any of the standard logic swings. For saturated logic control, Figure 32 shows a circuit that allows the normal positive output swing to cause the regulator to shutdown when the logic output is in the low voltage state. The negative output levels of a MECL gate can also be used for shutdown control as shown in Figure 33.

VOLTAGE BOOSTING

Some applications may require a high output voltage which may exceed the voltage rating of the MC1563. This must be solved by assuring that the IC regulator is operated within its limits. Three points in the regulator need to be considered:

1. The input voltage (pin 4),
2. the output voltage (pin 6) and,
3. the output sense lead (pin 8).

A reduced input voltage can be provided by using a separate supply. The output voltage may be zener-level shifted, and the sense line can tie to a portion of the output voltage through a resistive divider. The voltage boost circuit of Figure 34 uses this approach to provide a -90 volt supply. This circuit will exhibit regulation of 0.001% over a 100 mA load current range.

REMOTE SENSING

The MC1563 offers a remote sensing capability. This is important when the load is remote from the regulator, as the resistance of the interconnecting lines (V^- and GND) are added directly to the output impedance of the regulator. By remote sensing, this resistance is included inside the control loop of the regulator and is essentially eliminated. Figure 35 shows how remote sensing is accomplished using both a separate sense line from pin 8 and a separate ground line from the regulator to the remote load.

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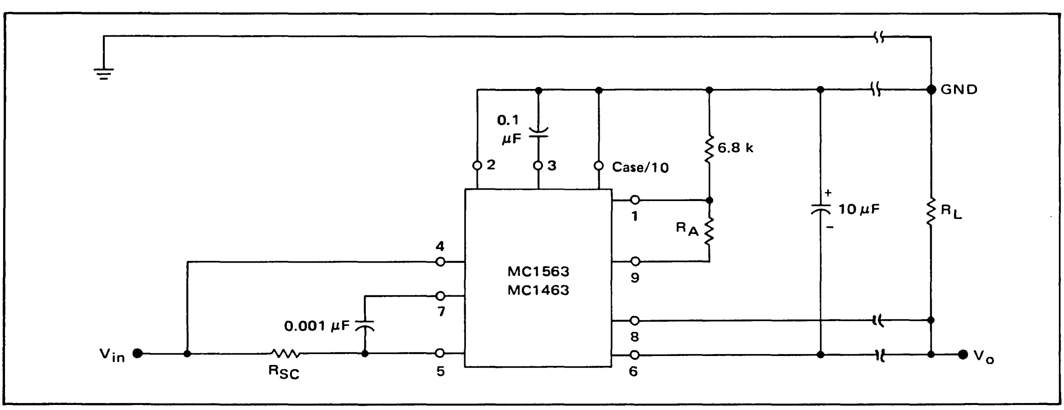


FIGURE 35 — Remote Sensing Circuit

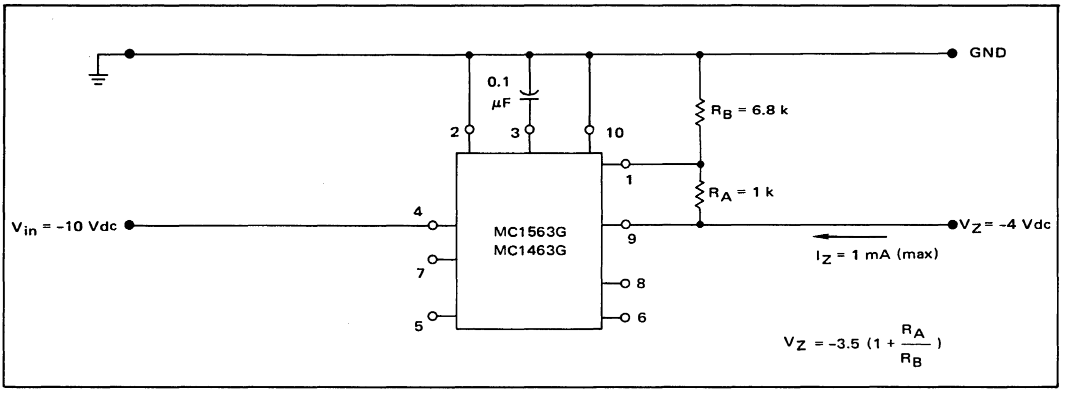


FIGURE 36 – An Adjustable "Zero-TC" Voltage Source

AN ADJUSTABLE ZERO-TEMPERATURE-COEFFICIENT (0-TC) VOLTAGE REFERENCE SOURCE

The MC1563, when used in conjunction with low-TC resistors, makes an excellent reference-voltage generator. If the -3.5 volt reference voltage of the IC regulator is a satisfactory value, then pins 1 and 9 can be tied together and no resistors are needed. This will provide a voltage reference having a typical temperature coefficient of 0.002%/°C. By adding two resistors, R_A and R_B, any voltage between -3.5 Vdc and -37 Vdc can be obtained with the same low TC (see Figure 36).

6

THERMAL SHUTDOWN

By setting a fixed voltage at pin 2, the MC1563 chip can be protected against excessive junction temperatures caused by power dissipation in the IC regulator. This is based on the negative temperature coefficient of the base-emitter junction of the shutdown transistor (-1.9 x 10^{-3}V/°C). By setting -0.61 Vdc externally, at pin 2, the regulator will shutdown when the chip temperature reaches approximately 140°C. Figure 37 shows a circuit that uses a zero-TC zener diode and a resistive divider to obtain this voltage.

In the case where an external pass transistor is employed; its temperature, rather than that of the IC regulator, requires control. A technique similar to the one just discussed can be used by directly monitoring the case temperature of the pass transistor as is indicated in Figure 38. The case of the normally "OFF" thermal monitoring transistor, Q2, should be in thermal contact with, but electrically isolated from, the case of the boost transistor, Q1.

THERMAL CONSIDERATIONS

Monolithic voltage regulators are subjected to internal heating similar to a power transistor. Since the degree of internal heating is a function of the specific application,

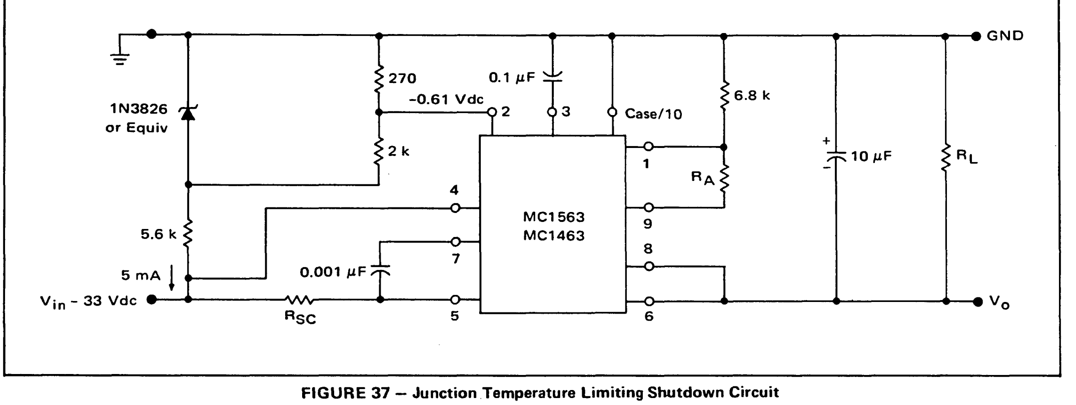


FIGURE 37 – Junction Temperature Limiting Shutdown Circuit

the designer must use caution not to exceed the specified maximum junction temperature (+175°C). Exceeding this limit will reduce reliability at an exponential rate. Good heatsinking not only reduces the junction temperature for a given power dissipation; it also tends to improve the dc stability of the output voltage by reducing the junction temperature change resulting from a change in the power dissipation of the IC regulator. By using the derating factors or thermal resistance values given in the Maximum Ratings Table of this data sheet, junction temperature can be computed for any given application in the same manner as for a power transistor*. A short-circuit on the output terminal can produce a "worst-case" thermal condition especially if the maximum input voltage is applied simultaneously with the maximum value of short-circuit load current (500 mA). Care should be taken not to exceed the maximum junction temperature rating during this fault condition and, in addition, the dc safe operating area limit (see Figure 24).

Thermal characteristics for a voltage regulator are useful in predicting performance since dc load and line regulation are affected by changes in junction temperature. These temperature changes can result from either a change in the ambient temperature, T_A, or a change in the power dissipated in the IC regulator. The effects of ambient temperature change on the dc output voltage can be estimated from the "Temperature Coefficient of Output Voltage" characteristic parameter shown as ±0.002%/°C, typical. Power dissipation is typically changed in the IC regulator by varying the dc load current. To estimate the dc change in output voltage due to a change in the dc load current, three effects must be considered:

1. junction temperature change due to the change in the power dissipation
2. output voltage decrease due to the finite output impedance of the control amplifier
3. thermal gradient on the IC chip.

A temperature differential does exist across a power IC chip and can cause a dc shift in the output voltage. A "gradient coefficient," GCV_O, can be used to describe this effect and is typically +0.03%/watt for the MC1563R. For an example of the relative magnitudes of these effects, consider the following conditions:

Given: MC1563

with V_{in} = -10 Vdc

V_O = -5 Vdc

and I_L = 100 mA to 200 mA

(ΔI_L = 100 mA)

assume T_A = 25°C

TO-66 Case with heatsink

*For more detailed information of methods used to compute junction temperature, see Motorola Application Note AN-226, Measurement of Thermal Properties of Semiconductors.

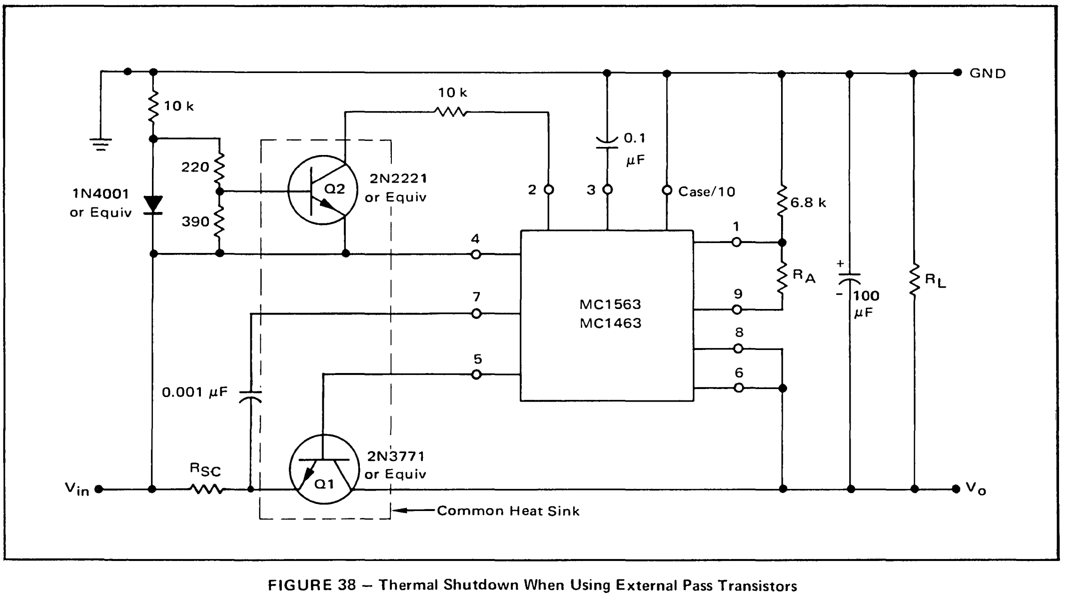


FIGURE 38 – Thermal Shutdown When Using External Pass Transistors

assume $\theta_{CS} = 0.2^oC/W$

and $\theta_{SA} = 2^oC/W$

It is desired to find the ΔV_O which results from this ΔI_L. Each of the three previously stated effects on V_O can now be separately considered.

1. ΔV_O due to ΔT_J

$$\Delta V_O = (V_O)(\Delta P_D)(TCV_O)(\theta_{JC} + \theta_{CS} + \theta_{SA})$$

OR

$$\Delta V_O = (5\ V)(5\ V \times 0.1\ A)(\pm 0.002\%/^oC)(19.2^oC/W)$$

$$\Delta V_O \approx \pm 1.0\ mV$$

2. ΔV_O due to Z_O

$$|\Delta V_O| = (-Z_O)(I_L)$$

$$|\Delta V_O| = -(2 \times 10^{-2})(10^{-1}) = -2\ mV$$

3. ΔV_O due to gradient coefficient, GCV_O

$$|\Delta V_O| = (GCV_O)(V_O)(\Delta P_D)$$

$$|\Delta V_O| = (+3 \times 10^{-4}/W)(5\ volts)(5 \times 10^{-1} W)$$

$$|\Delta V_O| = +0.8\ mV$$

Therefore the total ΔV_O is given by

$$|\Delta V_O\ total| = \pm 1.0 - 2.0 + 0.8\ mV$$

OR

$$-2.2\ mV \leqslant |V_O\ total| \leqslant -0.2\ mV$$

Other operating conditions may be substituted and computed in a similar manner to evaluate the relative effects of the parameters.

Typical Printed Circuit Board Layout

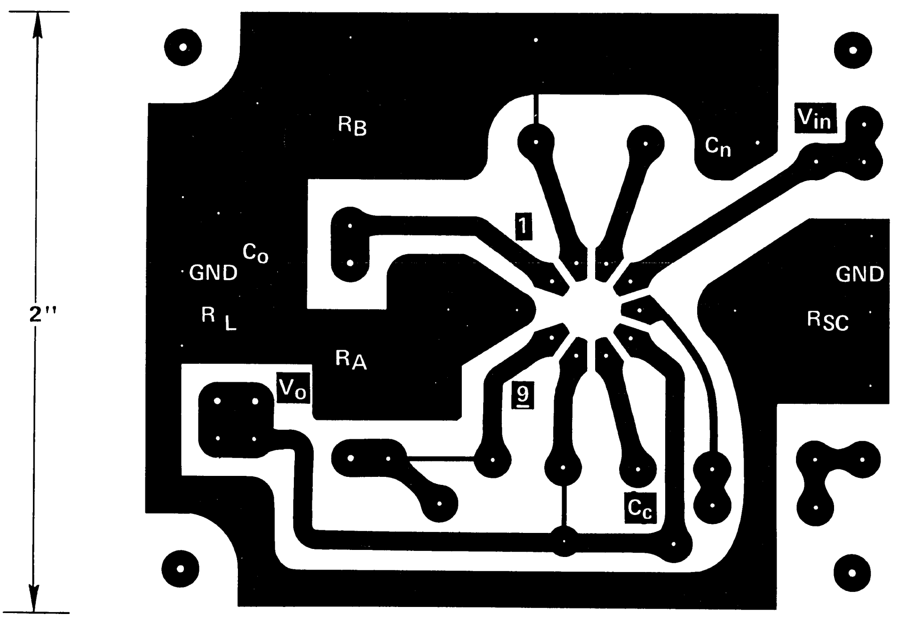
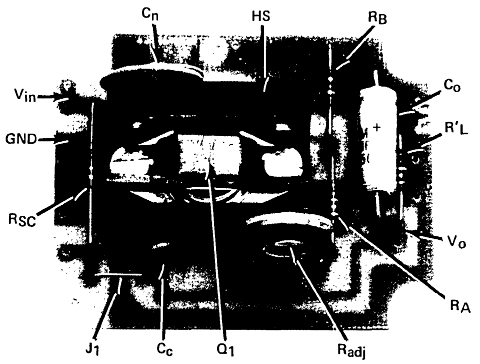


FIGURE 39 — Location of Components



Note 1:

When R_{adj} is used it is necessary to remove the copper which shorts out R_{adj}.

Note 2:

Extra holes are available in the circuit board to permit two resistors to be paralleled to obtain the desired value of R_{SC}.

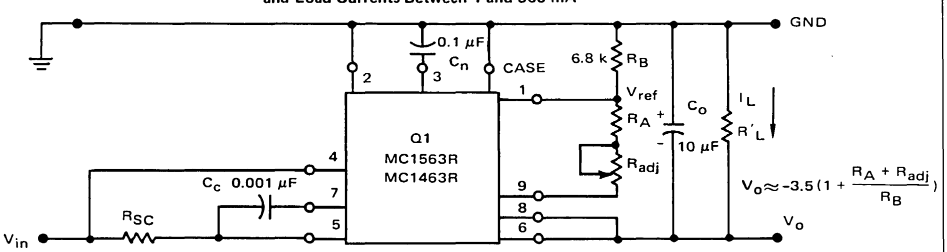
Note 3:

If pin 2 is used to shut down the regulator, remove the copper which shorts pin 2 to ground.

Note 4:

Remote sensing can be achieved by removing the copper which shorts pin 8 to pin 6 and connecting pin 8 directly to the "minus" load terminal. The circuit board ground should be connected to the unregulated power supply ground at the "plus" load terminal.

FIGURE 40 — Typical Circuit Connection for Output Voltages Between -3.5 and -37 Volts and Load Currents Between 1 and 500 mA



Select $R_A + R_{adj}$ to Give Desired V_{out}: $R_A + R_{adj} \approx (2|V_{out}| - 7)$ kΩ with R_B = 6.8 kΩ

PARTS LIST

Component	Value	Description
R_A	Select	1/4 or 1/2 watt carbon
R_B	6.8 k	1/4 or 1/2 watt carbon
R_{adj}	Select	IRC Model X-201, Mallory Model MTC-1 or equivalent
R_{SC}	Select	1/2 watt carbon
R'_L	Select	For minimum current of 1 mAdc
C_o	10 µF	Sprague 1500 Series, Dickson D10C series or equivalent
C_n	0.1 µF	Ceramic Disc — Centralab DDA104, Sprague TG-P10, or equivalent
C_C	0.001 µF	Ceramic Disc — Centralab DDA104, Sprague TG-P10, or equivalent
J_1		Jumper
Q1		MC1563R or MC1463R
*HS		Heatsink Thermalloy #6168B
*Socket	(Not Shown)	Robinson Nugent #0001306 Electronic Molding Corp. #6341-210-1, 6348-188-1, 6349-188-1
PC Board		Circuit DOT, Inc. #PC1113 1155 W. 23rd St. Tempe, Arizona 85281

*Optional

MC1566L
MC1466L

MULTI-PURPOSE REGULATORS

MONOLITHIC VOLTAGE AND CURRENT REGULATOR

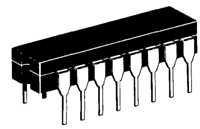
This unique "floating" regulator can deliver hundreds of volts – limited only by the breakdown voltage of the external series pass transistor. Output voltage and output current are adjustable. The MC1466/MC1566 integrated circuit voltage and current regulator is designed to give "laboratory" power-supply performance.

- Voltage/Current Regulation with Automatic Crossover
- Excellent Line Voltage Regulation, 0.01% +1.0 mV
- Excellent Load Voltage Regulation, 0.01% +1.0 mV
- Excellent Current Regulation, 0.1% +1.0 mA
- Short-Circuit Protection
- Output Voltage Adjustable to Zero Volts
- Internal Reference Voltage
- Adjustable Internal Current Source

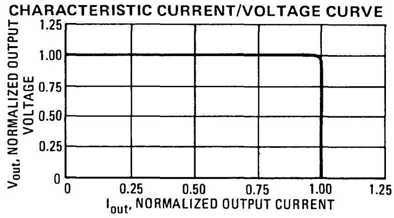
PRECISION WIDE-RANGE VOLTAGE and CURRENT REGULATOR

EPITAXIAL PASSIVATED

CERAMIC PACKAGE
CASE 632
TO-116

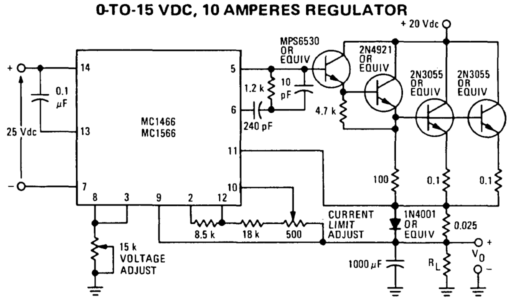


CHARACTERISTIC CURRENT/VOLTAGE CURVE

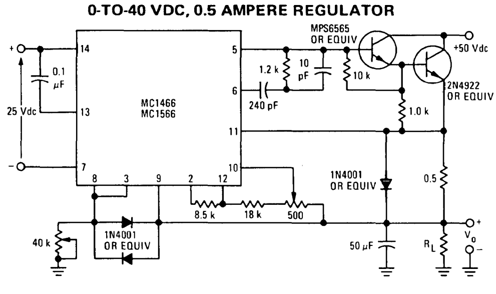


TYPICAL APPLICATIONS

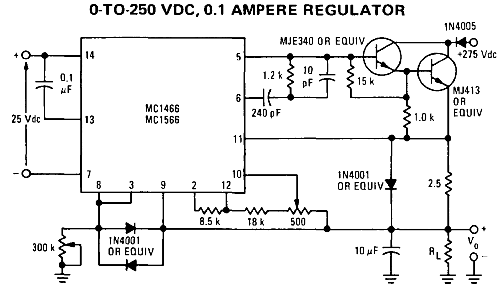
0-TO-15 VDC, 10 AMPERES REGULATOR



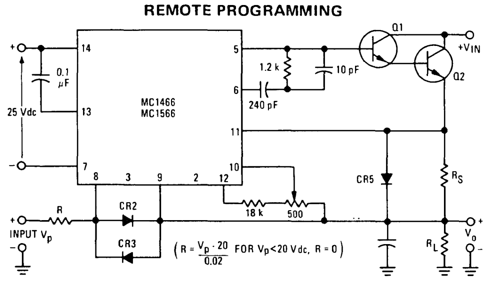
0-TO-40 VDC, 0.5 AMPERE REGULATOR



0-TO-250 VDC, 0.1 AMPERE REGULATOR



REMOTE PROGRAMMING

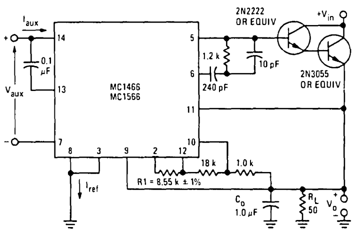
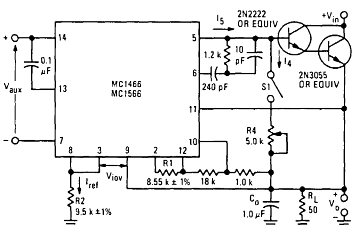
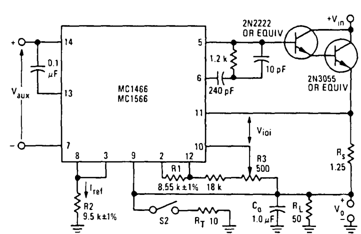


See Packaging Information Section for outline dimensions.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Auxiliary Voltage MC1466 MC1566	V_{aux}	 30 35	Vdc
Power Dissipation (Package Limitation) Derate above T_A = +50°C	P_D $1/\theta_{JA}$	750 6.0	mW mW/°C
Operating Temperature Range MC1466 MC1566	T_A	 0 to +75 −55 to +125	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{aux} = +25 Vdc unless otherwise noted)

Characteristic Definition	Characteristic	Symbol	Min	Typ	Max	Units
	Auxiliary Voltage (See Notes 1 & 2) (Voltage from pin 14 to pin 7) MC1466 MC1566	V_{aux}	 21 20	 – –	 30 35	Vdc
	Auxiliary Current MC1466 MC1566	I_{aux}	 – –	 9.0 7.0	 12 8.5	mAdc
	Internal Reference Voltage (Voltage from pin 12 to pin 7) MC1466 MC1566	V_{IR}	 17.3 18	 18.5 18.5	 19.7 19	Vdc
	Reference Current (See Note 3) MC1466 MC1566	I_{ref}	 0.8 0.9	 1.0 1.0	 1.2 1.1	mAdc
	Input Current-Pin 8 MC1466 MC1566	I_8	 – –	 6.0 3.0	 12 6.0	µAdc
	Power Dissipation MC1466 MC1566	P_D	 – –	 – –	 360 300	mW
	Input Offset Voltage, Voltage Control Amplifier (See Note 4) MC1466 MC1566	V_{iov}	 0 3.0	 15 15	 40 25	mVdc
	Load Voltage Regulation (See Note 5) MC1466 MC1566	ΔV_{iov}	 – –	 1.0 0.7	 3.0 1.0	mV
	MC1466 MC1566	$\Delta V_{ref}/V_{ref}$	– –	0.015 0.004	0.03 0.01	%
	Line Voltage Regulation (See Note 6) MC1466 MC1566	ΔV_{iov}	 – –	 1.0 0.7	 3.0 1.0	mV
	MC1466 MC1566	$\Delta V_{ref}/V_{ref}$	– –	0.015 0.004	0.03 0.01	%
	Temperature Coefficient of Output Voltage (T_A = 0 to +75°C) MC1466 (T_A = −55 to +25°C) MC1566 (T_A = +25 to +125°C) MC1566	TCV_o	 – – –	 0.01 0.006 0.004	 – – –	%/°C
	Input Offset Voltage, Current Control Amplifier (See Note 4) MC1466 (Voltage from pin 10 to pin 11) MC1566	V_{ioi}	 0 3.0	 15 15	 40 25	mVdc
	Load Current Regulation (See Note 7) MC1466 MC1566	$\Delta I_L/I_L$	 – –	 – –	 0.2 0.1	%
	MC1466 MC1566	ΔI_{ref}	– –	– –	1.0 1.0	mAdc

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NOTE 1:
The instantaneous input voltage, V_{aux}, must not exceed the maximum value of 30 Volts for the MC1466 or 35 Volts for the MC1566. The instantaneous value of V_{aux} must be greater than 20 Volts for the MC1566 or 21 Volts for the MC1466 for proper internal regulation.

NOTE 2:
The auxiliary supply voltage V_{aux}, must "float" and be electrically isolated from the unregulated high voltage supply, V_{IN}

NOTE 3:
Reference current may be set to any value of current less than 1.2 mAdc by applying the relationship:

$$I_{ref}\ (mA) = \frac{8.55}{R_1\ (k\Omega)}$$

NOTE 4:
A built-in offset voltage (15 mVdc nominal) is provided so that the power supply output voltage or current may be adjusted to zero.

NOTE 5:
Load Voltage Regulation is a function of two additive components, ΔV_{iov} and ΔV_{ref}, where ΔV_{iov} is the change in input offset voltage (measured between pins 8 and 9) and ΔV_{ref} is the change in voltage across R2 (measured between pin 8 and ground). Each component may be measured separately or the sum may be measured across the load. The measurement procedure for the test circuit shown is:

a. With S1 open (I_4 = 0) measure the value of $V_{iov\ (1)}$ and $V_{ref\ (1)}$

b. Close S1, adjust R4 so that I_4 = 500 μA and note $V_{iov\ (2)}$ and $V_{ref\ (2)}$.

Then $\Delta V_{iov} = V_{iov\ (1)} - V_{iov\ (2)}$

% Reference Regulation =

$$\frac{[V_{ref\ (1)} - V_{ref\ (2)}]}{V_{ref\ (1)}}\ (100\%) = \frac{\Delta V_{ref}}{V_{ref}}\ (100\%)$$

Load Voltage Regulation =

$$\frac{\Delta V_{ref}}{V_{ref}}\ (100\%) + \Delta V_{iov}$$

NOTE 6:
Line Voltage Regulation is a function of the same two additive components as Load Voltage Regulation, ΔV_{iov} and ΔV_{ref} (see note 5). The measurement procedure is:

a. Set the auxiliary voltage, V_{aux}, to the minimum specified value of 20 Volts for the MC1566 and 21 Volts for the MC1466. Read the value of $V_{iov\ (1)}$ and $V_{ref\ (1)}$.

b. Change the V_{aux} to 35 Volts for the MC1566 or 30 Volts for the MC1466 and note the value of $V_{iov\ (2)}$ and $V_{ref\ (2)}$. Then compute Line Voltage Regulation:

$\Delta V_{iov} = \Delta V_{iov\ (1)} - V_{iov\ (2)}$

% Reference Regulation =

$$\frac{[V_{ref\ (1)} - V_{ref\ (2)}]}{V_{ref\ (1)}}\ (100\%) = \frac{\Delta V_{ref}}{V_{ref}}\ (100\%)$$

Line Voltage Regulation =

$$\frac{\Delta V_{ref}}{V_{ref}}\ (100\%) + \Delta V_{iov}$$

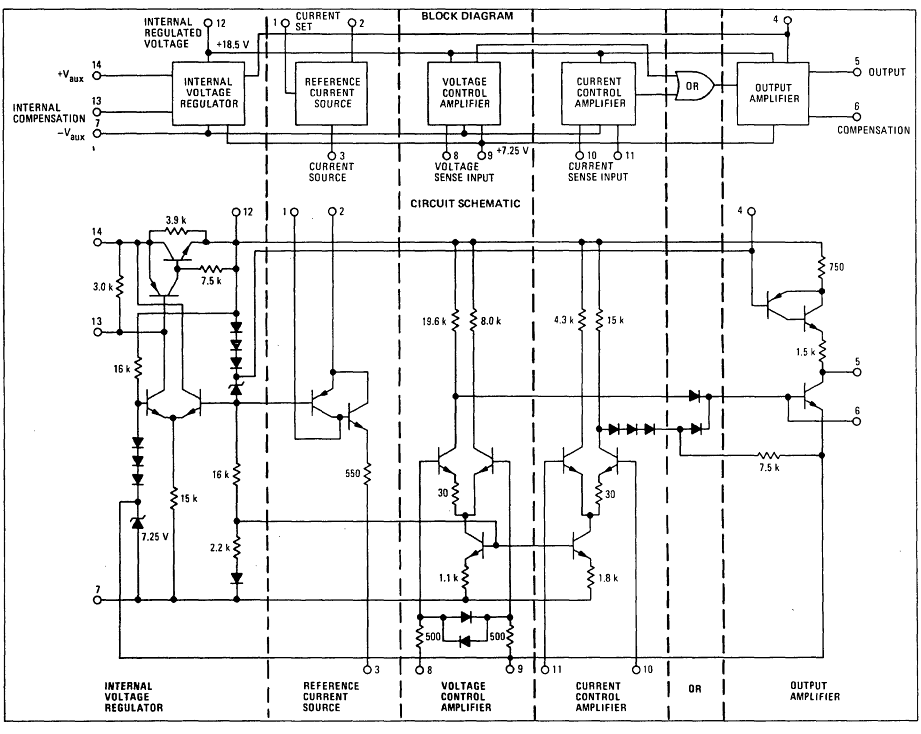
NOTE 7:
Load Current Regulation is measured by the following procedure:

a. With S2 open, adjust R3 for an initial load current, $I_{L(1)}$, such that V_o is 8.0 Vdc.

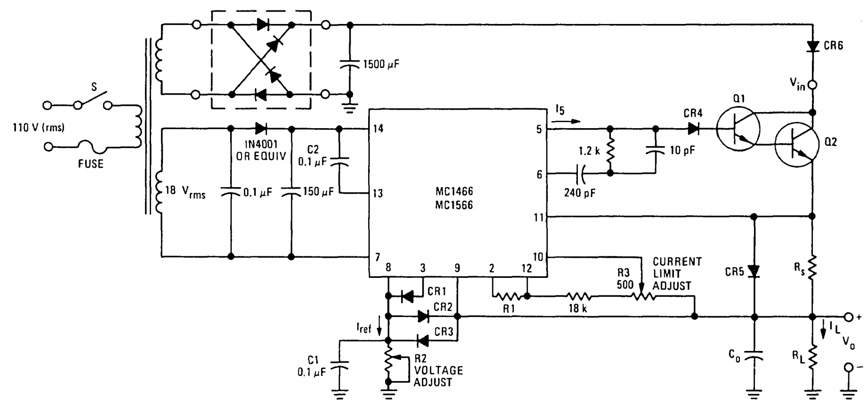
b. With S2 closed, adjust R_T for V_o = 1.0 Vdc and read $I_{L(2)}$. Then Load Current Regulation =

$$\frac{[I_{L(2)} - I_{L(1)}]}{I_{L(1)}}\ (100\%) + I_{ref}$$

where I_{ref} is 1.0 mAdc, Load Current Regulation is specified in this manner because I_{ref} passes through the load in a direction opposite that of load current and does not pass through the current sense resistor, R_s.



TYPICAL CIRCUIT CONNECTION



NORMAL DESIGN PROCEDURE AND DESIGN CONSIDERATIONS

1. Constant Voltage:
   For constant voltage operation, output voltage V_o is given by:
   $V_o = (I_{ref})\ (R_2)$
   where R2 is the resistance from pin 8 to ground and I_{ref} is the output current of pin 3.
   The recommended value of I_{ref} is 1.0 mAdc. Resistor R1 sets the value of I_{ref}:
   $I_{ref} = \frac{8.5}{R_1}$
   where R1 is the resistance between pins 2 and 12.
2. Constant Current:
   For constant current operation:
   (a) Select R_s for a 250 mV drop at the maximum desired regulated output current, I_{max}.
   (b) Adjust potentiometer R3 to set constant current output at desired value between zero and I_{max}.
3. If V_{in} is greater than 20 Vdc, CR2, CR3, and CR4 are necessary to protect the MC1466/MC1566 during short-circuit or transient conditions.
4. In applications where very low output noise is desired, R2 may be bypassed with C1 (0.1 µF to 2.0 µF). When R2 is bypassed, CR1 is necessary for protection during short-circuit conditions.
5. CR5 is recommended to protect the MC1466/MC1566 from simultaneous pass transistor failure and output short-circuit.
6. The RC network (10 pF, 240 pF, 1.2 k ohms) is used for compensation. The values shown are valid for all applications. However, the 10 pF capacitor may be omitted if f_T of Q1 and Q2 is greater than 0.5 MHz.
7. For remote sense applications, the positive voltage sense terminal (pin 9) is connected to the positive load terminal through a separate sense lead; and the negative sense terminal (the ground side of R2) is connected to the negative load terminal through a separate sense lead.
8. C_o may be selected by using the relationship:
   $C_o = (100\ \mu F)\ I_{L(max)}$, where $I_{L(max)}$ is the maximum load current in amperes.
9. C2 is necessary for the internal compensation of the MC1466/MC1566.
10. For optimum regulation, current out of pin 5, I_5, should not exceed 0.5 mAdc. Therefore select Q1 and Q2 such that:
    $\frac{I_{max}}{\beta 1 \beta 2} \leqslant 0.5$ mAdc
    where: I_{max} = maximum short-circuit load current (mAdc)
    $\beta 1$ = minimum beta of Q1
    $\beta 2$ = minimum beta of Q2
    Although Pin 5 will source up to 1.5 mAdc, $I_5 > 0.5$ mAdc will result in a degradation in regulation.
11. CR6 is recommended when $V_o > 150$ Vdc and should be rated such that Peak Inverse Voltage $> V_o$.

POSITIVE VOLTAGE REGULATORS

MC1569
MC1469

Specifications and Applications Information

MONOLITHIC VOLTAGE REGULATOR

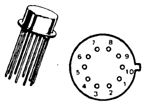
The MC1569/MC1469 is a positive voltage regulator designed to deliver continuous load current up to 500 mAdc. Output voltage is adjustable from 2.5 Vdc to 37 Vdc. The MC1569 is specified for use within the military temperature range (−55 to +125°C) and the MC1469 within the 0 to +70°C temperature range.

For systems requiring a positive regulated voltage, the MC1569 can be used with performance nearly identical to the MC1563 negative voltage regulator. Systems requiring both a positive and negative regulated voltage can use the MC1569 and MC1563 as complementary regulators with a common input ground.

- Electronic "Shut-Down" Control
- Excellent Load Regulation (Low Output Impedance – 20 milliohms typ)
- High Power Capability: up to 17.5 Watts
- Excellent Temperature Stability: ±0.002%/°C typ
- High Ripple Rejection: 0.002%/V typ

POSITIVE VOLTAGE REGULATOR INTEGRATED CIRCUIT

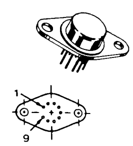
MONOLITHIC SILICON EPITAXIAL PASSIVATED



(Bottom View)

Pin 10 connected to case

CASE 602A
METAL PACKAGE
G SUFFIX



CASE 614
METAL PACKAGE
R SUFFIX

FIGURE 1 – TYPICAL CIRCUIT CONNECTION
($3.5 \le V_O \le 37$ Vdc, $1 \le I_L \le 500$ mA)

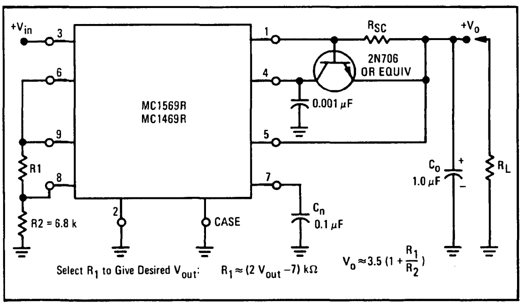


FIGURE 2 – TYPICAL NPN CURRENT BOOST CONNECTION
(V_O = 5.0 Vdc, I_L = 10 Adc [max])

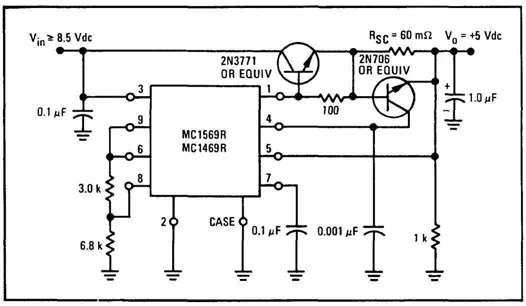
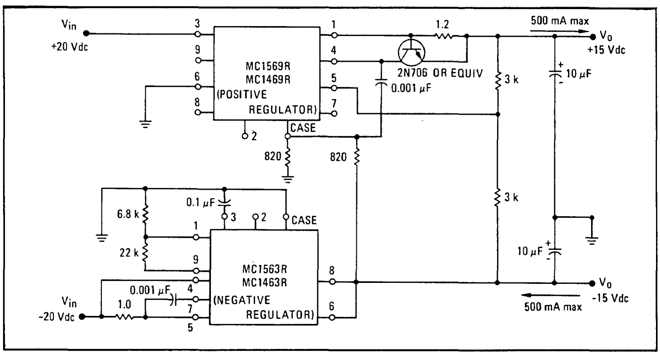
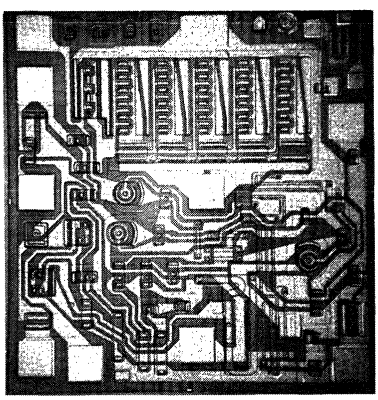


FIGURE 3 – ±15 V, ±400 mA COMPLEMENTARY TRACKING VOLTAGE REGULATOR





The index to the content of this data sheet appears on page 19.
See current MCC1569/1469 data sheet for standard linear chip information.
See Packaging Information Section for outline dimensions.

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MAXIMUM RATINGS (T_C = +25°C unless otherwise noted)

Rating	Symbol	Value		Unit
Input Voltage	V_{in}			Vdc
MC1469		35		
MC1569		40		
		G Package	R Package	
Peak Load Current	I_{pk}	250	600	mA
Current, Pin 2	$I_{pin\ 2}$	10	10	mA
Current, Pin 9	$I_{pin\ 9}$	5.0	5.0	
Power Dissipation and Thermal Characteristics				
T_A = 25°C	P_D	0.68	3.0	Watts
Derate above T_A = 25°C	$1/\theta_{JA}$	5.44	24	mW/°C
Thermal Resistance, Junction to Air	θ_{JA}	184	41.6	°C/W
T_C = 25°C	P_D	1.8	17.5	Watts
Derate above T_C = 25°C	$1/\theta_{JC}$	14.4	140	mW/°C
Thermal Resistance, Junction to Case	θ_{JC}	69.4	7.15	°C/W
Operating and Storage Junction Temperature	T_J, T_{stg}	-65 to +150		°C

OPERATING TEMPERATURE RANGE

Ambient Temperature	T_A		°C
MC1469		0 to +75	
MC1569		-55 to +125	

ELECTRICAL CHARACTERISTICS

(T_C = +25°C unless otherwise noted) (Load Current = 100 mA for "R" Package device, = 10 mA for "G" Package device, unless otherwise noted)

Characteristic	Fig.	Note	Symbol	MC1569 Min	MC1569 Typ	MC1569 Max	MC1469 Min	MC1469 Typ	MC1469 Max	Unit
Input Voltage (T_A = T_{low} ① to T_{high} ②)	4	1	V_{in}	8.5	–	40	9.0	–	35	Vdc
Output Voltage Range	4,5		V_o	2.5	–	37	2.5	–	32	Vdc
Reference Voltage (Pin 8 to Ground)	4		V_{ref}	3.4	3.5	3.6	3.2	3.5	3.8	Vdc
Minimum Input-Output Voltage Differential (R_{SC} = 0)	4	2	$V_{in} - V_o$	–	2.1	2.7	–	2.1	3.0	Vdc
Bias Current (I_L = 1.0 mAdc, R_2 = 6.8 k ohms, $I_b = I_{in} - I_L$)	4		I_b	–	4.0	9.0	–	5.0	12	mAdc
Output Noise (C_n = 0.1 µF, f = 10 Hz to 5.0 MHz)	4		v_n	–	0.150	–	–	0.150	–	mV(rms)
Temperature Coefficient of Output Voltage	4	3	TCV_o	–	±0.002	–	–	±0.002	–	%/°C
Operating Load Current Range										mAdc
(R_{SC} ≤0.3 ohms) R Package	4		I_L	1.0	–	500	1.0	–	500	
(R_{SC} ≤2.0 ohms) G Package				1.0	–	200	1.0	–	200	
Input Regulation	6	4	Reg_{in}	–	0.002	0.015	–	0.003	0.030	%/V_{in}
Load Regulation	7	5	Reg_{load}							
(T_J = Constant [1.0 mA≤I_L≤20 mA])				–	0.4	1.6	–	0.7	2.4	mV
(T_C = +25°C [1.0 mA≤I_L≤50 mA]) R Package				–	0.005	0.05	–	0.005	0.05	%/V_o
G Package				–	0.01	0.13	–	0.01	0.13	
Output Impedance (C_c = 0.001 µF, R_{SC} = 1.0 ohm, f = 1.0 kHz, V_{in} = +14 Vdc, V_o = +10 Vdc)	8	6	Z_{out}	–	20	80	–	35	120	milliohms
Shutdown Current (V_{in} = +35 Vdc)	9		I_{sd}	–	70	150	–	140	500	µAdc

① T_{low} = 0°C for MC1469
= -55°C for MC1569

② T_{high} = +75°C for MC1469
= +125°C for MC1569

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Note 1. "Minimum Input Voltage" is the minimum "total instantaneous input voltage" required to properly bias the internal zener reference diode. For output voltages greater than approximately 5.5 Vdc the minimum "total instantaneous input voltage" must increase to the extent that it will always exceed the output voltage by at least the "input-output voltage differential".

Note 2. This parameter states that the MC1569/MC1469 will regulate properly with the input-output voltage differential ($V_{in} - V_O$) as low as 2.7 Vdc and 3.0 Vdc respectively. Typical units will regulate properly with ($V_{in} - V_O$) as low as 2.1 Vdc as shown in the typical column. (See Figure 21.)

Note 3. "Temperature Coefficient of Output Voltage" is defined as:

$$\text{MC1569, } TC_{V_O} = \frac{\pm (V_{O\,max} - V_{O\,min})(100)}{(180^{\circ}C)(V_O \ @\ 25^{\circ}C)} = \%/^{\circ}C$$

$$\text{MC1469, } TC_{V_O} = \frac{\pm (V_{O\,max} - V_{O\,min})(100)}{(75^{\circ}C)(V_O \ @\ 25^{\circ}C)} = \%/^{\circ}C$$

The output-voltage adjusting resistors (R1 and R2) must have matched temperature characteristics in order to maintain a constant ratio independent of temperature.

Note 4. The input signal ($v_{in} \approx 1.0$ V[rms]) can be introduced by use of a transformer which will allow the output of an audio oscillator to be coupled in series with the dc input to the regulator. (See Figure 20.) Input regulation is the percentage change in output voltage per volt change in the input voltage and is expressed as

$$\text{Input Regulation} = \frac{\Delta V_O}{V_O\,(\Delta V_{in})}\ 100\ (\%/V_{in}),$$

where ΔV_O is the change in the output voltage V_O for the input change ΔV_{in}.

Note 5. Load regulation is specified for small ($\leqslant +17^{\circ}C$) changes in junction temperature. Temperature drift effect must be taken into account separately for conditions of high junction temperature changes due to the thermal feedback that exists on the monolithic chip.

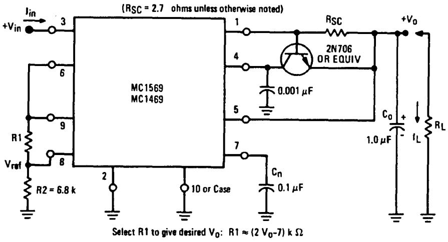
$$\text{Load Regulation} = \frac{\left[V_O|_{I_L = 1.0\,mA}\right] - \left[V_O|_{I_L = 50\,mA}\right]}{V_O|_{I_L = 1.0\,mA}} \times 100$$

Note 6. The resulting low level output signal (v_O) will require the use of a tuned voltmeter to obtain a reading. Special care should be used to insure that the measurement technique does not include connection resistance, wire resistance, and wire lead inductance (i.e., measure close to the case). Note that No. 22 AWG hook-up wire has approximately 4.0 milliohms/in. dc resistance and an inductive reactance of approximately 10 milliohms/in. at 100 kHz. Avoid use of alligator clips or banana plug-jack combination.

TEST CIRCUITS

FIGURE 4 – CONNECTION FOR $V_O \geq 3.5$ Vdc

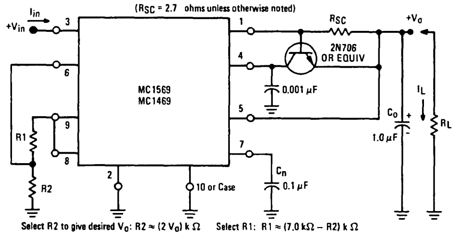
(R_{SC} = 2.7 ohms unless otherwise noted)



Select R1 to give desired V_O: R1 ≈ ($2V_O$–7) k Ω

FIGURE 5 – CONNECTION FOR 2.5 Vdc ≤ V_O ≤ 3.5 Vdc

(R_{SC} = 2.7 ohms unless otherwise noted)



Select R2 to give desired V_O: R2 ≈ ($2V_O$) k Ω   Select R1: R1 ≈ (7.0 kΩ – R2) k Ω

FIGURE 6 – INPUT REGULATION

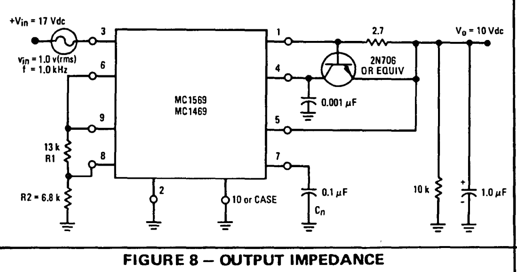


FIGURE 7 – LOAD REGULATION

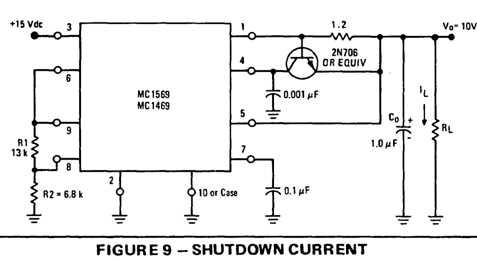


FIGURE 8 – OUTPUT IMPEDANCE

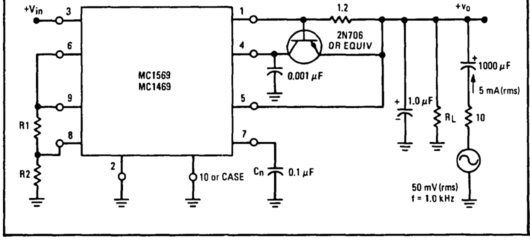
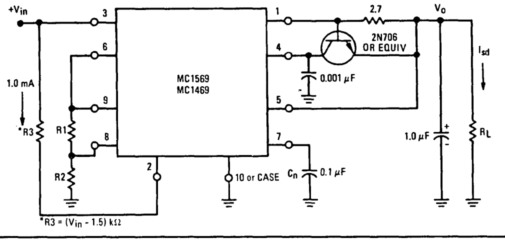


FIGURE 9 – SHUTDOWN CURRENT



*R3 = (V_{in} – 1.5) kΩ

GENERAL DESIGN INFORMATION

1. Output Voltage, V_O
   a) For $V_O \geq 3.5$ Vdc – Output voltage is set by resistors R1 and R2 (see Figure 4). Set R2 = 6.8 k ohms and determine R1 from the graph of Figure 10 or from the equation:

   $$R1 \approx (2\,V_O - 7)\ k\Omega$$

   b) For $2.5 \leq V_O \leq 3.5$ Vdc – Output voltage is set by resistors R1 and R2 (see Figure 5). Resistors R1 and R2 can be determined from the graph of Figure 11 or from the equations:

   $$R2 \approx 2\,(V_O)\ k\Omega$$
   $$R1 \approx (7\ k\Omega - R2)\ k\Omega$$

   c) Output voltage, V_O, is determined by the ratio of R1 and R2, therefore optimum temperature performance can be achieved if R1 and R2 have the same temperature coefficient.
   d) Output voltage can be varied by making R1 adjustable as shown in Figure 43.
   e) If V_O = 3.5 Vdc (to supply RTL for example), tie pins 6, 8 and 9 together. R1 and R2 are not needed in this case.
2. Short Circuit Current, I_{SC}
   Short Circuit Current, I_{SC}, is determined by R_{SC}. R_{SC} may be chosen with the aid of Figure 12 or the expression:

   $$R_{SC} \approx \frac{0.6}{I_{SC}}\ \text{ohms}$$

   where I_{SC} is measured in amperes. This expression is also valid when current is boosted as shown in Figures 2, 29 and 30.
3. Compensation, C_c
   A 0.001 μF capacitor, C_c, from pin 4 to ground will provide adequate compensation in most applications, with or without current boost. Smaller values of C_c will reduce stability and larger values of C_c will degrade pulse response and output impedance versus frequency. The physical location of C_c should be close to the MC1569/MC1469 with short lead lengths.
4. Noise Filter Capacitor, C_n
   A 0.1 μF capacitor, C_n, from pin 7 to ground will typically reduce the output noise voltage to 150 μV(rms). The value of C_n can be increased or decreased, depending on the noise voltage requirements of a particular application. A minimum value of 0.001 μF is recommended.
5. Output Capacitor, C_O
   The value of C_O should be at least 1.0 μF in order to provide good stability. The maximum value recommended is a function of current limit resistor R_{SC}:

   $$C_{O(max)} \approx \frac{250\ \mu F}{R_{SC}}$$

   where R_{SC} is measured in ohms. Values of C_O greater than this will degrade the pulse response characteristics and increase the settling time.
6. Shut-Down Control
   One method of turning "OFF" the regulator is to apply a dc voltage at pin 2. This control can be used to eliminate power consumption by circuit loads which can be put in "standby" mode. Examples include, an ac or dc "squelch" control for communications circuits, and a dissipation control to protect the regulator under sustained output short-circuiting (see Figures 34, 39 and 40). As the magnitude of the input-threshold voltage at Pin 2 depends directly upon the junction temperature of the integrated circuit chip, a fixed dc voltage at Pin 2 will cause automatic shut-down for high junction temperatures (see Figure 39). This will protect the chip, independent of the heat sinking used, the ambient temperature, or the input or output voltage levels. Standard logic levels of MRTL, MDTL or MTTL can also be used to turn the regulator "ON" or "OFF".
7. Remote Sensing
   The connection to Pin 5 can be made with a separate lead direct to the load. Thus, "remote sensing" can be achieved and the effect of undesired impedances (including that of the milliammeter used to measure I_L) on Z_{out} can be greatly reduced (see Figure 37).

FIGURE 10 – R1 versus V_O
($V_O \geq 3.5$ Vdc, See Figure 4)

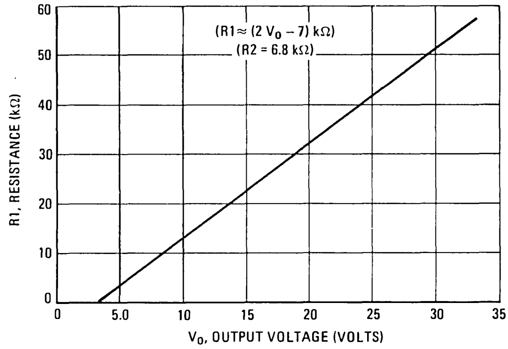


FIGURE 11 – R1 and R2 versus V_O
($2.5 \leq V_O \leq 3.5$ Vdc, See Figure 5)

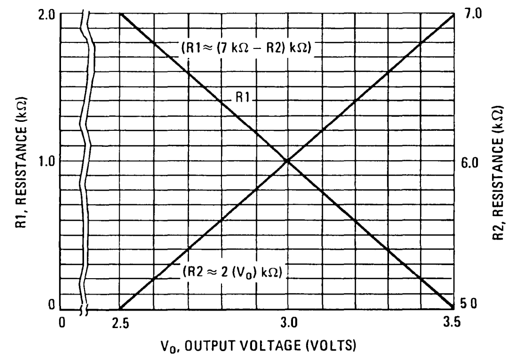
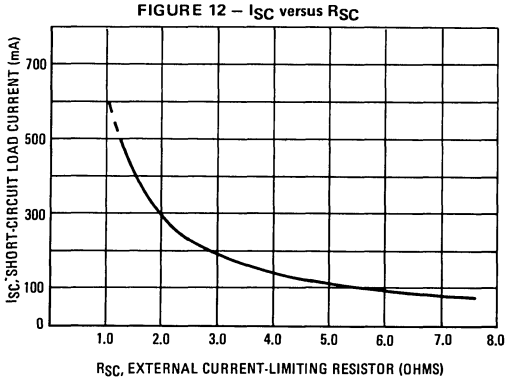


FIGURE 12 – I_{SC} versus R_{SC}



TYPICAL CHARACTERISTICS

Unless otherwise noted: $C_n = 0.1\ \mu F$, $C_c = 0.001\ \mu F$, $C_o = 1.0\ \mu F$, $T_C = +25^oC$, $V_{in(nom)} = +9.0$ Vdc, $V_{o(nom)} = +5.0$ Vdc

$I_L > 200$ mA for R package only.

FIGURE 13 – DEPENDENCE OF OUTPUT IMPEDANCE ON OUTPUT VOLTAGE

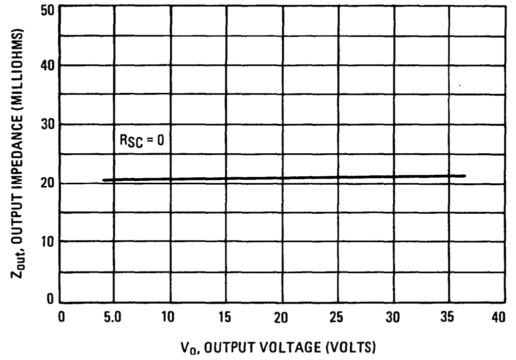


FIGURE 14 – OUTPUT IMPEDANCE versus R_{SC}

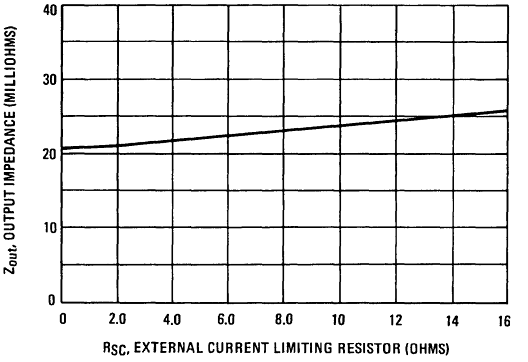


FIGURE 15 – FREQUENCY DEPENDENCE OF INPUT REGULATION, $C_o = 10\ \mu F$

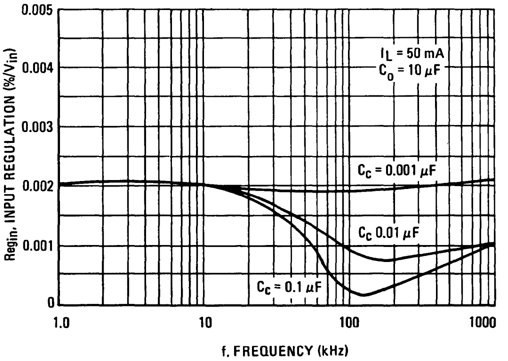


FIGURE 16 – FREQUENCY DEPENDENCE OF INPUT REGULATION, $C_o = 2.0\ \mu F$

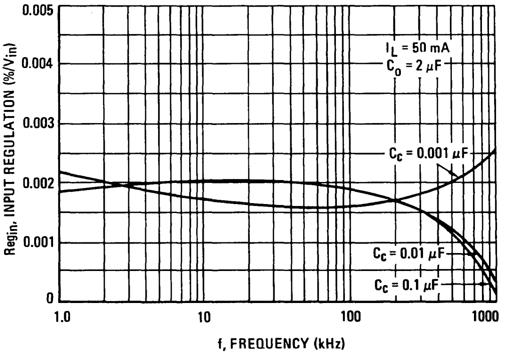


FIGURE 17 – CURRENT-LIMITING CHARACTERISTICS

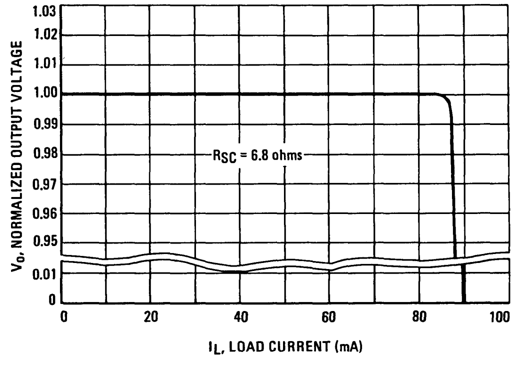
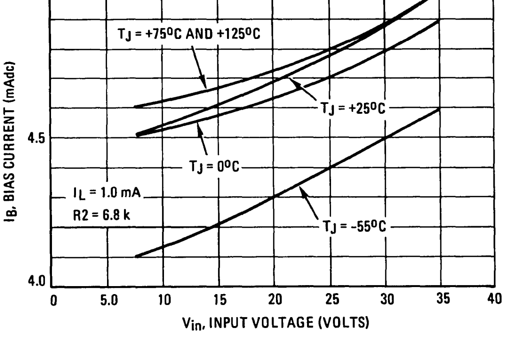


FIGURE 18 – BIAS CURRENT versus INPUT VOLTAGE



TYPICAL CHARACTERISTICS (continued)

Unless otherwise noted: $C_n = 0.1\ \mu F$, $C_c = 0.001\ \mu F$, $C_o = 1.0\ \mu F$, $T_C = +25^oC$, $V_{in(nom)} = +9.0$ Vdc, $V_{o(nom)} = +5.0$ Vdc

$I_L > 200$ mA for R package only.

FIGURE 19 – EFFECT OF LOAD CURRENT ON INPUT-OUTPUT VOLTAGE DIFFERENTIAL

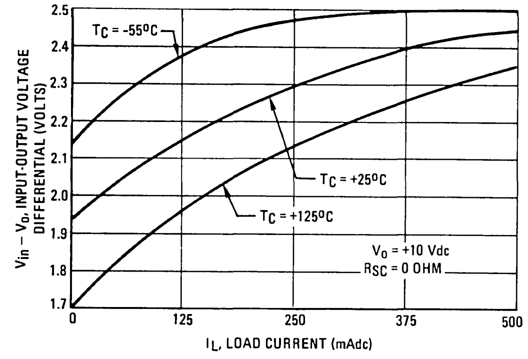


FIGURE 20 – EFFECT OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL ON INPUT REGULATION

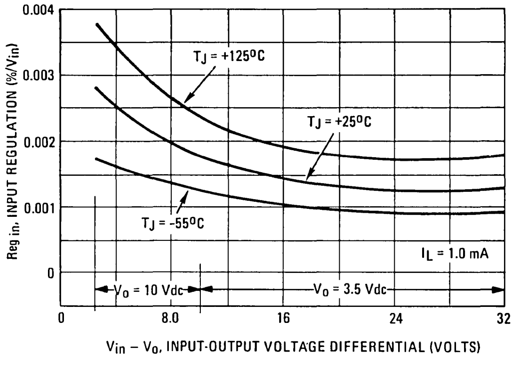


FIGURE 21 – INPUT TRANSIENT RESPONSE

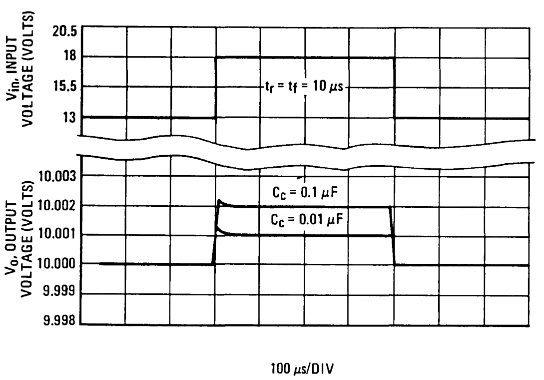


FIGURE 22 – TEMPERATURE DEPENDENCE OF SHORT-CIRCUIT LOAD CURRENT

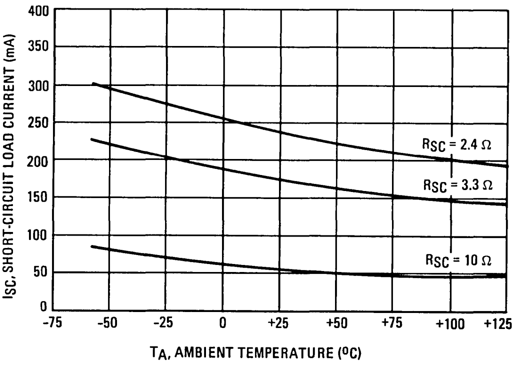


FIGURE 23 – FREQUENCY DEPENDENCE OF OUTPUT IMPEDANCE, $C_o = 10\ \mu F$

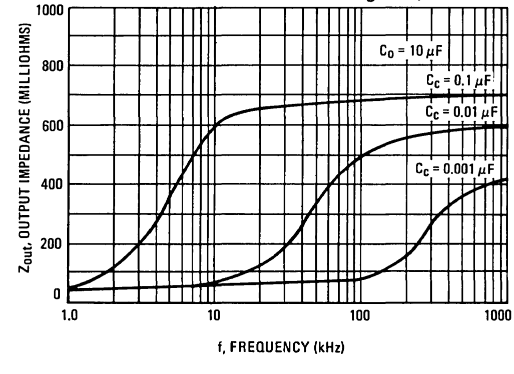
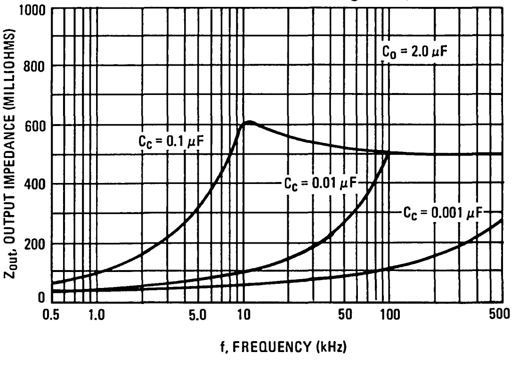


FIGURE 24 – FREQUENCY DEPENDENCE OF OUTPUT IMPEDANCE, $C_o = 2.0\ \mu F$



6

OPERATIONS AND APPLICATIONS

This section describes the operation and design of the MC1569 positive voltage regulator and also provides information on useful applications.

SUBJECT SEQUENCE

THEORY OF OPERATION

The usual series voltage regulator shown in Figure 25, consists of a reference voltage, an error amplifier, and a series control element. The error amplifier compares the output voltage with the reference voltage and adjusts the output accordingly until the error is essentially zero. For applications requiring output voltages larger than the reference, there are two options. The first is to use a resistive divider across the output and compare only a fraction of the output voltage to the reference. This approach suffers from reduced feedback to the error amplifier due to the attenuation of the resistive divider. This degrades load regulation especially at high voltage levels.

The alternative is to eliminate the resistive divider and to shift the reference voltage instead. To accomplish this, another amplifier is employed to amplify (or level shift) the reference voltage using an operational amplifier as shown in Figure 26. The gain-determining resistors may be external, enabling a wide range of output voltages. This is exactly the same approach used in the first option. That is, the output is being resistively divided to match the reference voltage. There is however, one big difference in that the output of this "regulator" is driving the input of another regulator (the error amplifier). The output of the reference amplifier has a relatively low impedance as compared to the input impedance of the error amplifier. Changes in the load of the output of the error amplifier are buffered to the extent that they have virtually no effect on the reference amplifier. If the feedback resistors are external (as they are on the MC1569) a wide range of reference voltages can be established.

The error amplifier can now be operated at unity gain to provide excellent regulation. In fact, this "regulator-within-a-regulator" concept permits the load regulation to be specified in terms of output impedance rather than as some percentage change of the output voltage. This approach was used in the design of the MC1569 positive-voltage regulator.

FIGURE 25 – SERIES VOLTAGE REGULATOR

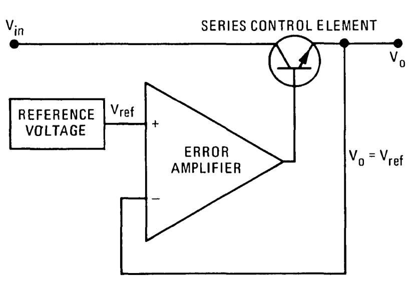


FIGURE 26 – THE "REGULATOR-WITHIN-A-REGULATOR" APPROACH

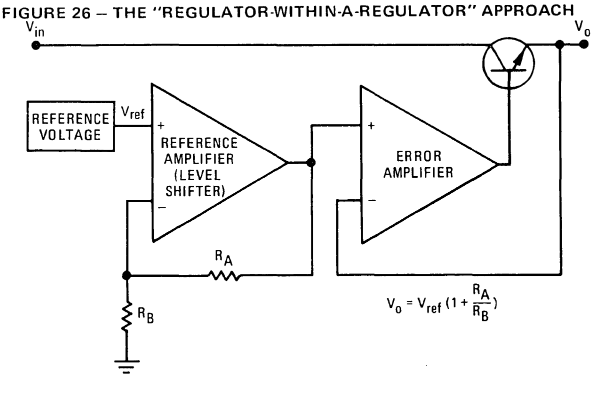
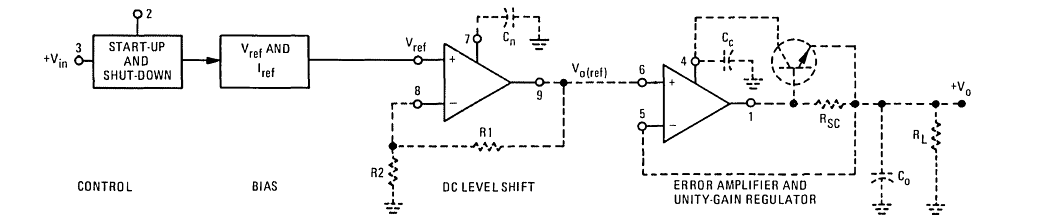
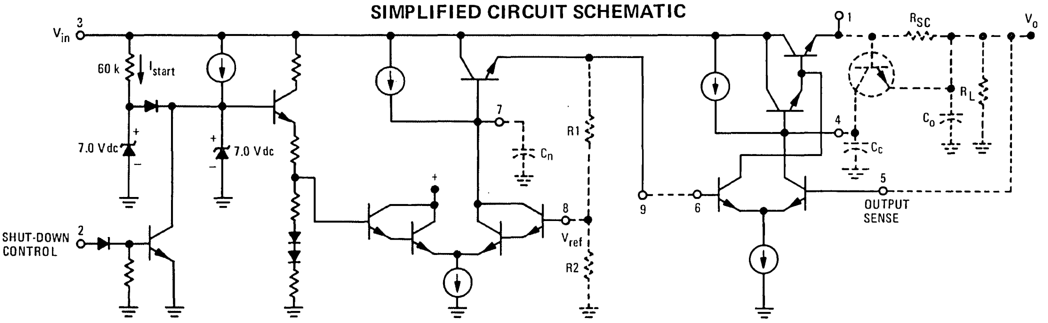


FIGURE 27
(Recommended External Circuitry is Depicted With Dotted Lines.)

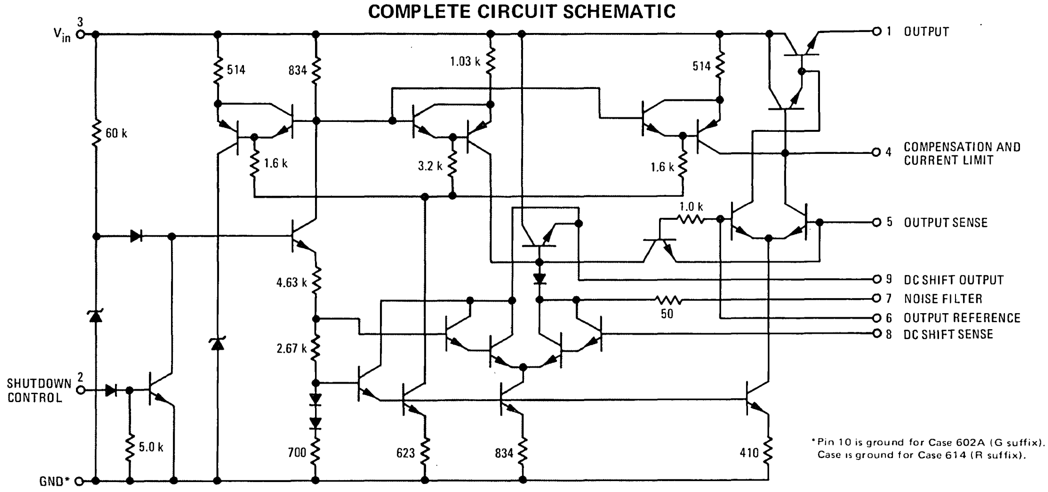
MC1569/MC1469 BLOCK DIAGRAM



SIMPLIFIED CIRCUIT SCHEMATIC



COMPLETE CIRCUIT SCHEMATIC



6

MC1569 Operation

Figure 27 shows the MC1569 Regulator block diagram, simplified schematic, and complete schematic. The four basic sections of the regulator are: Control, Bias, DC Level Shift, and Output (unity gain) Regulator. Each section is detailed in the following paragraphs.

Control

The control section involves two basic functions, start-up and shutdown. A start-up function is required since the biasing is essentially independent of the unregulated input voltage. It makes use of two zener diodes having the same breakdown voltage. A first or auxiliary zener is driven directly from the input voltage line through a resistor (60 kΩ) and permits the regulator to initially achieve the desired bias conditions. This permits the second, or reference zener to be driven from a current source. When the reference zener enters breakdown, the auxiliary zener is isolated from the rest of the regulator circuitry by a diode disconnect technique. This is necessary to keep the added noise and ripple of the auxiliary zener from degrading the performance of the regulator.

The shutdown control consists of an NPN transistor across the reference zener diode. When this transistor is turned "ON", via pin 2, the reference voltage is reduced to essentially zero volts and the regulator is forced to shutdown. During shutdown the current drain of the complete IC regulator drops to $V_{in}/60\ k\Omega$ or 500 μA for a 30 V input.

Bias

A zener diode is the main reference element and forms the heart of the bias circuitry. Its positive temperature coefficient is balanced by the negative temperature coefficients of forward biased diodes in a ratio determined by the resistors in the diode string. The result is a reference voltage of approximately 3.5 Vdc with a typical temperature coefficient of 0.002%/°C. In addition, this circuit also provides a reference current which is used to bias all current sources in the remaining regulator circuitry.

DC Level Shift

The reference voltage is used as the input to a Darlington differential amplifier. The gain of this amplifier is quite high and it therefore may be considered to function as a conventional operational amplifier. Consequently, negative feedback can be employed using two external resistors (R1 and R2) to set the closed-loop gain and to boost the reference voltage to the desired output voltage. A capacitor, C_n, is introduced externally into the level shift network (via pin 7) to stabilize the amplifier and to filter the zener noise. The recommended value for this capacitor is 0.1 μF and should have a voltage rating in excess of the desired output voltage. Smaller capacitors (0.001 μF minimum) may be used but will cause a slight increase in output noise. Larger values of C_n will reduce the noise as well as delay the start-up of the regulator.

Output Regulator

The output of the level shift amplifier (pin 9) is fed to the noninverting input (pin 6) of the output error amplifier. The inverting input to this amplifier is the Output Sense connection (pin 5) of the regulator. A Darlington connected NPN power transistor is used to handle the load current. The short-circuit current limiting resistor, R_{SC}, is connected in the emitter of this transistor to sample the full load current. By placing an external low-level NPN transistor across R_{SC} as shown in Figure 27, output current can be limited to a predetermined value:

$$I_{L(max)} \approx \frac{0.6}{R_{SC}} \text{ or } R_{SC} = \frac{0.6}{I_{L(max)}}$$

where $I_{L(max)}$ is the maximum load current (amperes) and R_{SC} is the value of the current limiting resistor (ohms).

Stability and Compensation

As has been seen, the MC1569 employs two amplifiers, each using negative feedback. This implies the possibility of instability due to excessive phase shift at high frequencies. Since the error amplifier is normally used at unity gain (the worst case for stability) a high impedance node is brought out for compensation. For normal operation, a capacitor is connected between this point (pin 4) and ground. The recommended value of 0.001 μF will insure stability and still provide acceptable transient response (see Figure 28, A and B). It is also necessary to use an output capacitor, C_o, (typically 1.0 μF) from the output, V_o, to ground. When an external transistor is used to boost the current, C_o = 1.0 μF is also recommended (see Figure 2).

FIGURE 28A — LOAD TRANSIENT RESPONSE

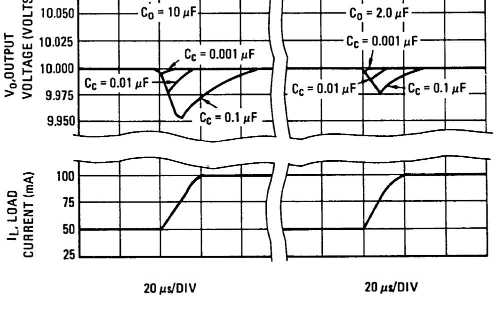
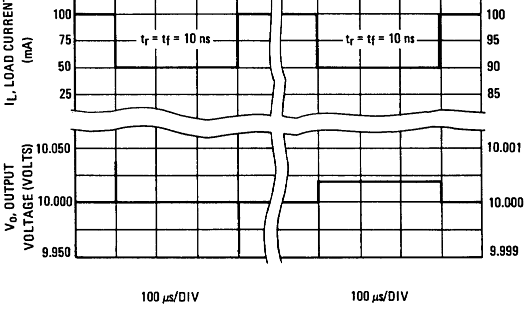


FIGURE 28B — LOAD TRANSIENT RESPONSE



TYPICAL NPN CURRENT BOOST CONNECTIONS

FIGURE 29A – 5 Vdc, 10 AMPERE REGULATOR

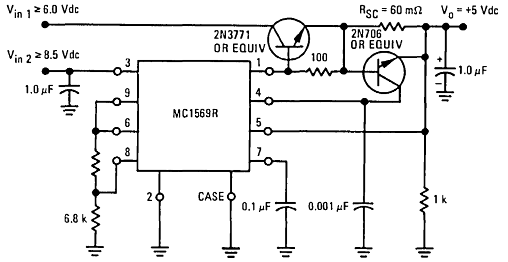


FIGURE 29B – 5-VOLT 5-AMPERE REGULATOR

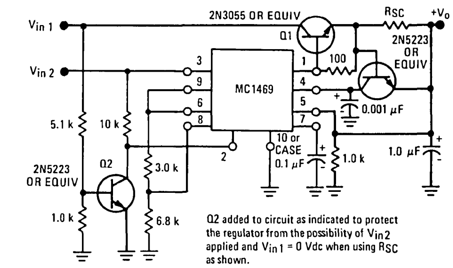
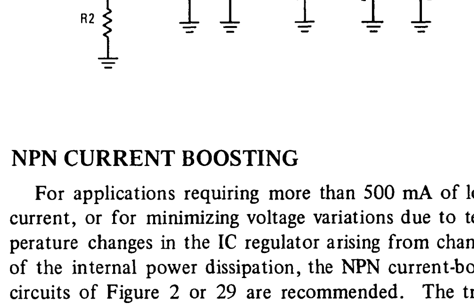


FIGURE 30 – PNP CURRENT BOOST CONNECTION



NPN CURRENT BOOSTING

For applications requiring more than 500 mA of load current, or for minimizing voltage variations due to temperature changes in the IC regulator arising from changes of the internal power dissipation, the NPN current-boost circuits of Figure 2 or 29 are recommended. The transistor shown in Figure 29A, the 2N3771 (or MJ3771), can supply currents to 10 amperes (subject, of course, to the safe area limitations). To improve the efficiency of the NPN boost configuration, particularly for small output voltages, the circuit of Figure 29 is recommended. An auxiliary 8.5-volt supply is used to power the IC regulator and the heavy load current is obtained from a second supply of lower voltage. For the 10-ampere regulator of Figure 29 this represents a savings of 25 watts when compared with operating the regulator from the single 8.5 V supply. It can supply current to 10 amperes while requiring an input voltage to the collector of the pass transistor of 6.0 volts minimum. The pass transistor is limited to 10 amperes by the added short-circuit current network in its emitter (R_{SC}).

PNP CURRENT BOOSTING

A typical PNP current boost circuit is shown in Figure 30. Voltages from 2.5 Vdc to 37 Vdc and currents of many amperes can be obtained with this circuit.

Since the PNP transistor must not be turned on by the MC1569 bias current (I_b) the resistor R_{in} must meet the following condition:

$$R_{in} < \frac{V_{BE}}{I_b}$$

where V_{BE} is the base-to-emitter voltage required to turn on the PNP pass transistor, (typically 0.6 Vdc for silicon and 0.2 Vdc for germanium).

For germanium pass transistors, a silicon diode may be placed in series with the emitter to provide an additional voltage drop. This allows a larger value of R_{in} than would be possible if the diode were omitted. The diode will, however, be required to carry the maximum load current.

SELF-OSCILLATING SWITCHING REGULATOR

In all of the current boosting circuits shown thus far it has been assumed that the input-output voltage differential can be minimized to obtain maximum efficiency in both the external pass element as well as the MC1569. This may not be possible in applications where only a single supply voltage is available and high current levels preclude zener diode pre-regulating approaches. In such applications a switching-mode voltage regulator is highly desirable since the pass device is either ON or OFF. The theoretical efficiency of an ideal switching regulator is 100%. Realizable efficiencies of 90% are within the realm of possibility thus obviating the need for large power dissipating components. The output voltage will contain a ripple component; however, this can be made quite small if the switching frequency is made relatively high so filtering techniques are effective. Figure 31 shows a functional diagram for a self-oscillating voltage regulator. The comparator-driver will sense the voltage across the inductor, this voltage being related to the load current, I_L, by

$$L\frac{dI_L}{dt} = V.$$

For a first approximation this can be assumed to be a linear relationship.

Initially, V_O will be low and Q1 will be ON. The voltage at the non-inverting input will approach $\beta_1 V_{in}$, where:

$$\beta_1 V_{in} = \frac{V_{ref}R_a}{R_a + R_b} + \frac{V_c R_b}{R_a + R_b}$$

When this output voltage is reached the comparator will switch, turning Q1 OFF. The diode, CR1, will now become forward biased and will supply a path for the inductor current. This current and the sense voltage will start to decrease until the output voltage reaches

$$\beta_2 V_{in} = \frac{V_{ref}R_a}{R_a + R_b}$$

where the comparator will again switch turning Q1 ON, and the cycle repeats. Thus the output voltage is approximately V_{ref} plus a ripple component.

The frequency of oscillation can be shown to be

$$f = \frac{V_{out}(V_{in} - V_{out})}{L\,V_C(I_{max} - I_o)} \qquad (1)$$

where

I_{max} = The maximum value of inductor current

I_o = The minimum inductor current.

Normally this frequency will be in the range of approximately 2 kHz to 6 kHz. In this range, inductor values can be small and are compatible with the switching times of the pass transistor and diode. The switching time of the comparator is quite fast since positive feedback aids both turn-on and turn-off times. The limiting factors are the diode and pass transistor rise and fall times which should be quite fast or efficiency will suffer.

Figure 32 shows a self oscillating switching regulator which in many respects is similar to the PNP current boost previously discussed. The 6.8 kΩ resistor in conjunction with R1 sets the reference voltage, V_{ref}. Q1 and CR1 are selected for fast switching times as well as the necessary power dissipation ratings. Since a linear inductor is assumed, the inductor cannot be allowed to saturate at maximum load currents and should be chosen accordingly. If core saturation does occur, peak transistor and diode currents will be large and power dissipation will increase.

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FIGURE 31 – BASIC SELF-OSCILLATING SWITCHING REGULATOR

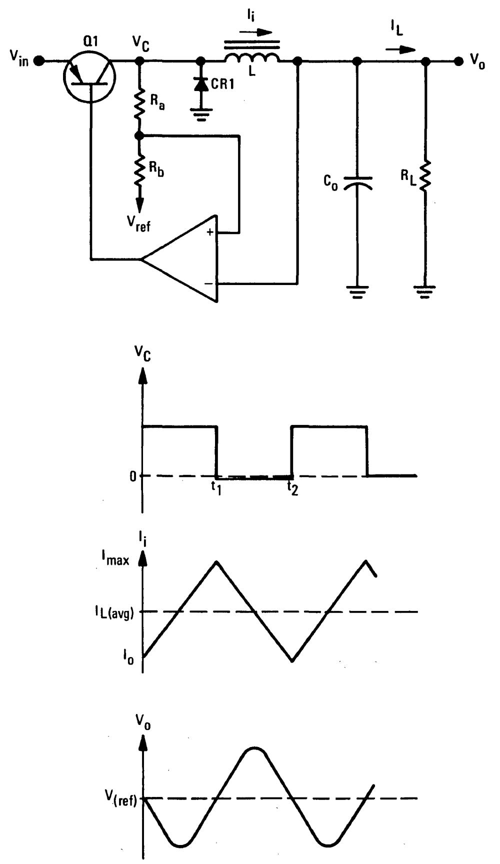
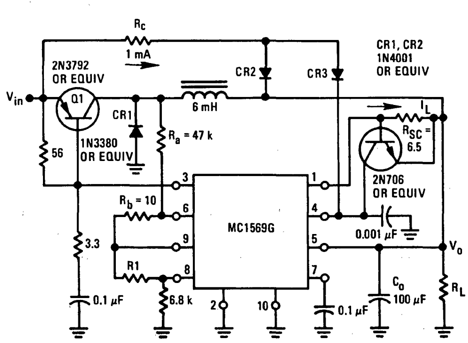


FIGURE 32 – MC1569 SELF-OSCILLATING SWITCHING REGULATOR



As a design center is required for a practical circuit, assume the following requirements:

$V_{in} = +28$ Volts

$V_{out} = +10$ Volts

$\Delta V_o = 50$ mV

$f \cong 5$ kHz

$I_{max} = 1.125$ A

$I_o = 1$ A

$$\Delta V \approx V_{in} \frac{R_b}{R_a}. \qquad (2)$$

Using Equation (1), the inductor value can be found:

$$L = \frac{(28-10)}{2(1.125-1)} \frac{10}{28} \left(\frac{1}{5 \times 10^3}\right)$$

$$\approx 7 \text{ mH}.$$

For the test circuit, a value of 6 mH was selected. Using for a first approximation

$$C_o = \frac{(V_{in} - V_{out})(V_{out})}{8L f^2 V_{in}(\Delta V)}$$

$$= \frac{(28 - 10)10}{8(7 \times 10^{-3})(5 \times 10^3)^2 (28)(50 \times 10^{-3})}$$

$$\approx 95\ \mu\text{F}.$$

As shown, a value of 100 μF was selected. Since little current is required at pin 6, R_a can be large. Assume R_a = 47 kΩ and then use Equation (2) to determine R_b:

$$50 \times 10^{-3} = \frac{28}{47\ \text{k}\Omega} R_b$$

$$R_b = \frac{47}{28} 50 \approx 85\Omega$$

Since the internal impedance presented by pin 9 is on the order of 60Ω, a value of R_b = 10Ω is adequate.

Diodes CR2, CR3, and R_c may be added to prevent saturation of the error amplifier to increase switching speed. When the output stage of the error amplifier approaches saturation, CR2 becomes forward biased and clamps the error amplifier. Resistor R_c should be selected to supply a total of 1 mAdc to CR2 and CR3.

To show correlation between the predicted and tested specifications the following data was obtained:

$V_{in} = +28\ (\pm 1\%)$ Volts

$V_{out} = +10$ Volts

$\Delta V_o = 60$ mV

$f = 7$ kHz

@ $I_L = 1$A

which checks quite well with the predicted values. R_b can be adjusted to minimize the ripple component as well as to trim the operating frequency. Also this frequency will change with varying loads as is normal with this type of circuit. Pin 2 can still be used for shut-down if so desired. R_{SC} should be set such that the ratio of load current to base drive current is 10:1 in this case $I_1 \approx 100$ mA and $R_{SC} = 6.5\Omega$.

POSITIVE AND NEGATIVE POWER SUPPLIES

If the MC1569 is driven from a floating source it is possible to use it as a negative regulator by grounding the positive output terminal. The MC1569 may also be used with the MC1563 to provide completely independent positive and negative voltage regulators with comparable performance.

Some applications may require complementary tracking in which both supplies arrive at the voltage level simultaneously, and variations in the magnitudes of the two voltages track. Figures 3 and 33 illustrate this approach. In this application, the MC1563 is used as the reference regulator, establishing the negative output voltage. The MC1569 positive regulator is used in a tracking mode by grounding one side of the differential amplifier (pin 6 of the MC1569) and using the other side (pin 5 of the MC1569) to sense the voltage developed at the junction of the two 3-k ohm resistors. This differential amplifier controls the MC1569 series pass transistor such that the voltage at pin 5 will be zero. When the voltage at pin 5 equals zero, $+V_O$ must equal $|-V_O|$.

For the configuration shown in Figure 33, the level shift amplifier in the MC1569 is employed to generate an auxiliary +5-volt supply which is boosted to a 2-ampere capability by Q1 and Q2. (The +5-volt supply, as shown, is not short-circuit protected.) The −15-volt supply varies less than 0.1 mV over a zero to −300 mAdc current range and the +15-volt supply tracks this variation. The +15-volt supply varies 20 mV over the zero to +300 mAdc load current range. The +5-volt supply varies less than 5 mV for $0 \le I_L \le 200$ mA with the other two voltages remaining unchanged.

SHUTDOWN TECHNIQUES

Pin 2 of the MC1569 is provided for the express purpose of shutting the regulator "OFF". Referring to the schematic, it can be seen that pin 2 goes to the base of an NPN transistor; which, if turned "ON", will turn the zener "OFF" and deny current to all the biasing current sources. This action causes the output to go to essentially zero volts and the only current drawn by the IC regulator will be the small start current through the 60-k ohm start resistor (V_{in}/60 kΩ). This feature provides additional versatility in the applications of the MC1569. Various subsystems may be placed in a "standby" mode to conserve power until actually needed. Or the power may be turned "OFF" in response to other occurrences such as overheating, over-voltage, shorted output, etc.

To activate shutdown, one simply applies a potential greater than two diode drops with a current capability of 1 mA. Note that if a hard supply (i.e., +3 V) is applied directly to pin 2, the shutdown circuitry will be destroyed since there is no inherent current limiting. Maximum rating for the drive current into pin 2 is 10 mA, while 1 mA is adequate for shutdown.

FIGURE 33 – A ±15 Vdc COMPLEMENTARY TRACKING REGULATOR WITH AUXILIARY +5.0 V SUPPLY

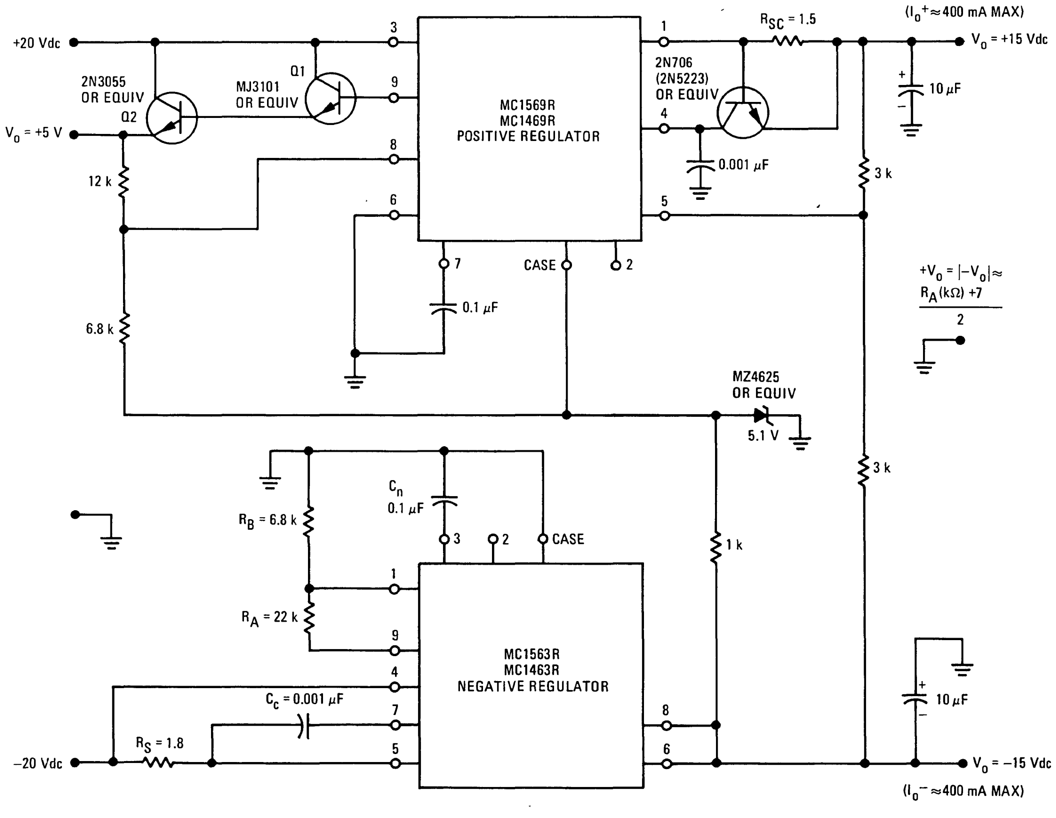


FIGURE 34 – ELECTRONIC SHUT-DOWN USING A MDTL GATE

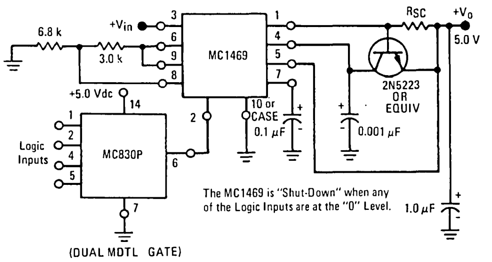


FIGURE 35 – AUTOMATIC LATCH INTO SHUT-DOWN WHEN OUTPUT IS SHORT-CIRCUITED WITH MANUAL RE-START

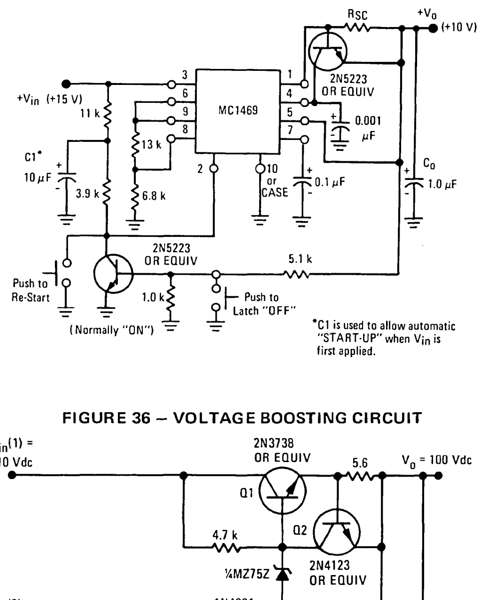


FIGURE 36 – VOLTAGE BOOSTING CIRCUIT

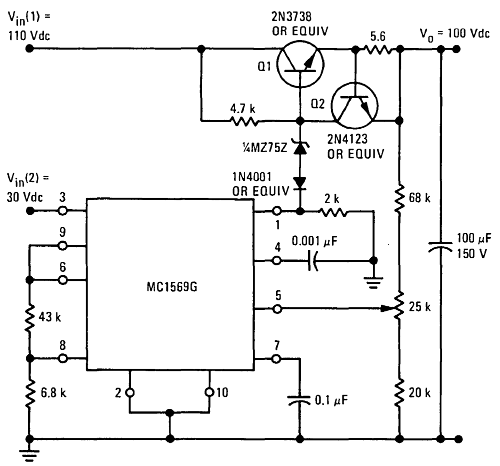


Figure 34 shows how the regulator can be controlled by a logic gate. Here, it is assumed that the regulator operates in its normal mode – as a positive regulator referenced to ground – and that the logic gate is of the saturating type, operating from a positive supply to ground. The high logic level should be greater than about 1.5 V and should source no more than 10 mA into pin 2.

The gate shown is of the MDTL type. MRTL and MTTL can also be used as long as the drive current is within safe limits (this is important when using MTTL, where the output stage uses an active pull-up).

In some cases a regulator can be designed which can handle the power dissipation resulting from normal operation but cannot safely dissipate the power resulting from a sustained short-circuit. The circuit of Figure 35 solves this problem by shutting down the regulator when the output is short-circuited.

VOLTAGE BOOSTING

The MC1569 has a maximum output voltage capability of 37 volts which covers the bulk of the user requirements. However, it is possible to obtain higher output voltages. One such voltage boosting circuit is shown in Figure 36.

Since high voltage NPN silicon devices are readily available, the only problem is the voltage limitations of the MC1569. This can be overcome by using voltage shift techniques to limit the voltage to 35 volts across the MC1569 while referencing to a higher output voltage.

The zener diode in the base lead of the NPN device is used to shift the output voltage of the MC1569 by approximately 75 volts to the desired high voltage level, in this case 100 volts. Another voltage shift is accomplished by the resistor divider on the output to accommodate the required 25 volt reference to the MC1569. The 2 kΩ resistor is used to bias the zener diode so the current through the 4.7 kΩ resistor can be controlled by the MC1569. The 1N4001 diode protects the MC1569 from supplying load current under short circuit conditions and Q2 serves to limit base current to Q1. For R_{SC} as shown, the short circuit current will be approximately 100 mA.

In order to use a single supply voltage, $V_{in}(2)$ can be derived from $V_{in}(1)$ with a zener diode, shunt pre-regulator.

It can be seen that loop gain has been reduced by the resistor divider and hence the closed loop bandwidth will be less. This of course will result in a more stable system, but regulator performance is degraded to some degree.

REMOTE SENSING

The MC1569 offers a remote sensing capability. This is important when the load is remote from the regulator,

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as the resistance of the interconnecting lines (V_O and GND) are added directly to the output impedance of the regulator. By remote sensing, this resistance is included inside the control loop of the regulator and is essentially eliminated. Figure 37 shows how remote sensing is accomplished using both a separate sense line from pin 8 and a separate ground line from the regulator to the remote load.

AN ADJUSTABLE ZERO-TEMPERATURE-COEFFICIENT (0-TC) VOLTAGE REFERENCE SOURCE

The MC1569, when used in conjunction with low TC resistors, makes an excellent reference-voltage generator. If the 3.5 volt reference voltage of the IC regulator is a satisfactory value, then pins 8 and 9 can be tied together and no resistors are needed. This will provide a voltage reference having a typical temperature coefficient of 0.002%/°C. By adding two resistors, R1 and R2, any voltage between 3.5 Vdc and 37 Vdc can be obtained with the same low TC (see Figure 38).

THERMAL SHUTDOWN

By setting a fixed voltage at pin 2, the MC1569 chip can be protected against excessive junction temperatures caused by power dissipation in the IC regulator. This is based on the negative temperature coefficient of the base-emitter junction of the shutdown transistor and the diode in series with pin 2 (-3.4×10^{-3}V/°C). By setting 1.0 Vdc externally at pin 2, the regulator will shutdown when the chip temperature reaches approximately +140°C. Figure 39 shows a circuit that uses a zero-TC zener diode and a resistive divider to obtain this voltage.

FIGURE 37 – REMOTE SENSING CIRCUIT

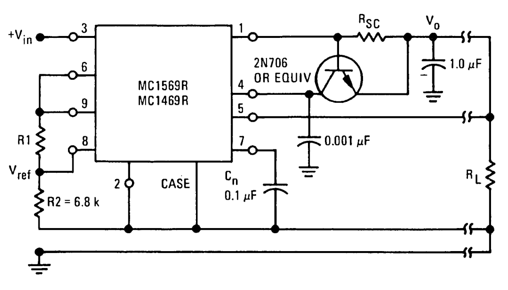
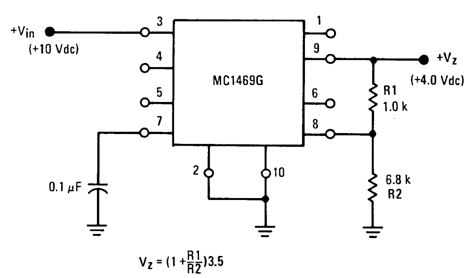


FIGURE 38 – AN ADJUSTABLE "ZERO-TC" VOLTAGE SOURCE



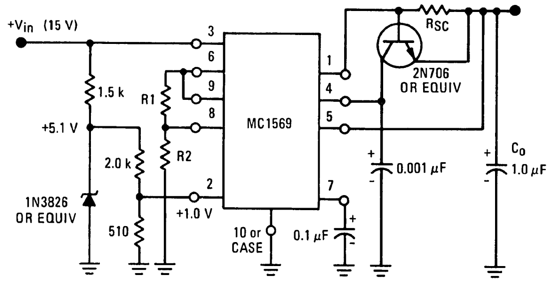
$V_Z = (1 + \frac{R1}{R2})3.5$

FIGURE 39 – JUNCTION TEMPERATURE LIMITING SHUTDOWN CIRCUIT

FIGURE 39A – USING A ZERO TC REFERENCE

FIGURE 39B – USING A T_A REFERENCE

$V_{pin\ 2}$ (for shut-down) $\approx 1.38 - 3.4 \times 10^{-3}\ (T_J - 25°C)$



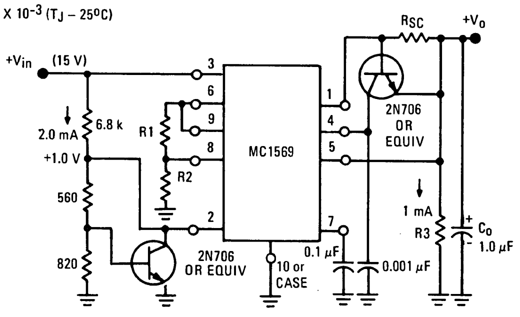


FIGURE 40 – THERMAL SHUTDOWN WHEN USING EXTERNAL PASS TRANSISTORS

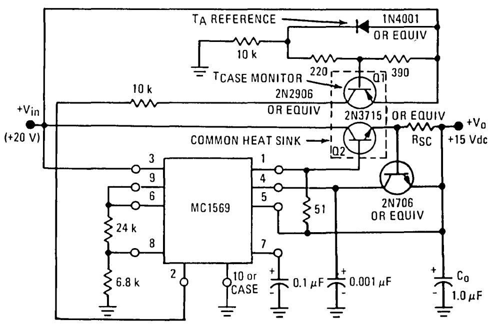
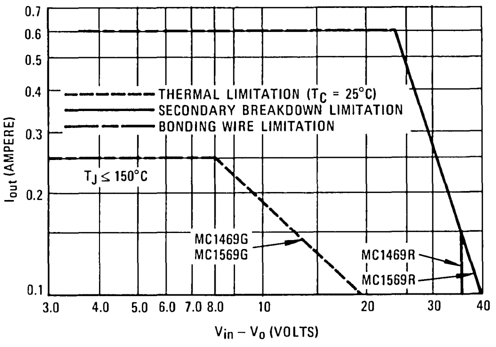


FIGURE 41 – DC SAFE OPERATING AREA



In the case where an external pass transistor is employed, its temperature, rather than that of the IC regulator, requires control. A technique similar to the one just discussed can be used by directly monitoring the case temperature of the pass transistor as is indicated in Figure 40. The case of the normally "OFF" thermal monitoring transistor, Q2, should be in thermal contact with, but electrically isolated from, the case of the boost transistor, Q1.

THERMAL CONSIDERATIONS

Monolithic voltage regulators are subjected to internal heating similar to a power transistor. Since the degree of internal heating is a function of the specific application, the designer must use caution not to exceed the specified maximum junction temperature (+150°C). Exceeding this limit will reduce reliability at an exponential rate. Good heatsinking not only reduces the junction temperature for a given power dissipation; it also tends to improve the dc stability of the output voltage by reducing the junction temperature change resulting from a change in the power dissipation of the IC regulator. By using the derating factors or thermal resistance values given in the Maximum Ratings Table of this data sheet, junction temperature can be computed for any given application in the same manner as for a power transistor*. A short-circuit on the output terminal can produce a "worst-case" thermal condition especially if the maximum input voltage is applied simultaneously with the maximum value of short-circuit load current. Care should be taken not to exceed the maximum junction temperature rating during this fault condition and, in addition, the dc safe operating area limit (see Figure 41).

*For more detailed information of methods used to compute junction temperature, see Motorola Application Note AN-226, Measurement of Thermal Properties of Semiconductors.

Thermal characteristics for a voltage regulator are useful in predicting performance since dc load and line regulation are affected by changes in junction temperature. These temperature changes can result from either a change in the ambient temperature, T_A, or a change in the power dissipated in the IC regulator. The effects of ambient temperature change on the dc output voltage can be estimated from the "Temperature Coefficient of Output Voltage" characteristic parameter shown as ±0.002%/°C, typical. Power dissipation is typically changed in the IC regulator by varying the dc load current. To estimate the dc change in output voltage due to a change in the dc load current, three effects must be considered:

1. junction temperature change due to the change in the power dissipation
2. output voltage decrease due to the finite output impedance of the control amplifier
3. thermal gradient on the IC chip.

A temperature differential does exist across a power IC chip and can cause a dc shift in the output voltage. A "gradient coefficient," GCV_O, can be used to describe this effect and is typically −0.06%/watt for the MC1569. For an example of the relative magnitudes of these effects, consider the following conditions:

Given MC1569

with $V_{in} = 10$ Vdc

$V_O = 5$ Vdc

6

and $I_L = 100$ mA to 200 mA

$(\Delta I_L = 100$ mA)

assume $T_A = 25^oC$

TO-66 Case with heatsink

assume $\theta_{CS} = 0.2^oC/W$

and $\theta_{SA} = 2^oC/W$

$\theta_{JC} = 7.15^oC/W$ (from maximum ratings table)

It is desired to find the ΔV_O which results from this ΔI_L. Each of the three previously stated effects on V_O can now be separately considered.

1. ΔV_o due to ΔT_J

$$\Delta V_o = (V_o)(\Delta P_D)(TCV_o)(\theta_{JC} + \theta_{CS} + \theta_{SA})$$

OR

$$\Delta V_o = (5\ V)(5\ V \times 0.1\ A)(\pm 0.002\%/^oC)(9.35^oC/W)$$

$$\Delta V_o \approx \pm 0.5\ mV$$

2. ΔV_o due to Z_o

$$|\Delta V_o| = (-Z_o)(I_L)$$

$$|\Delta V_o| = -(2 \times 10^{-2})(10^{-1}) = -2\ mV$$

3. ΔV_o due to gradient coefficient, GCV_o

$$|\Delta V_o| = (GCV_o)(V_o)(\Delta P_D)$$

$$|\Delta V_o| = (-6 \times 10^{-4}/W)(5\ volts)(5 \times 10^{-1} W)$$

$$|\Delta V_o| = -1.6\ mV$$

Therefore the total ΔV_o is given by

$$|\Delta V_o\ total| = \pm 0.5 - 2.0 - 1.6\ mV$$

OR

$$-4.1\ mV \leq |V_o\ total| \leq -3.1\ mV$$

Other operating conditions may be substituted and computed in a similar manner to evaluate the relative effects of the parameters.

TYPICAL PRINTED CIRCUIT BOARD LAYOUT

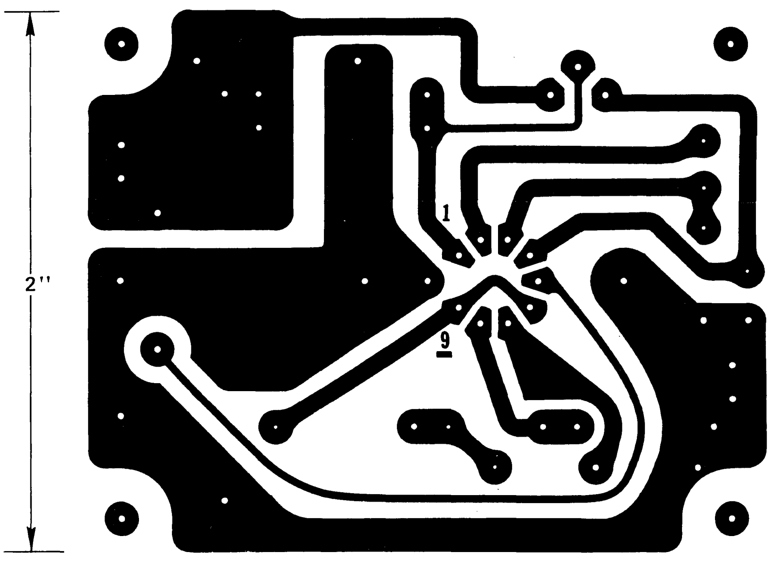


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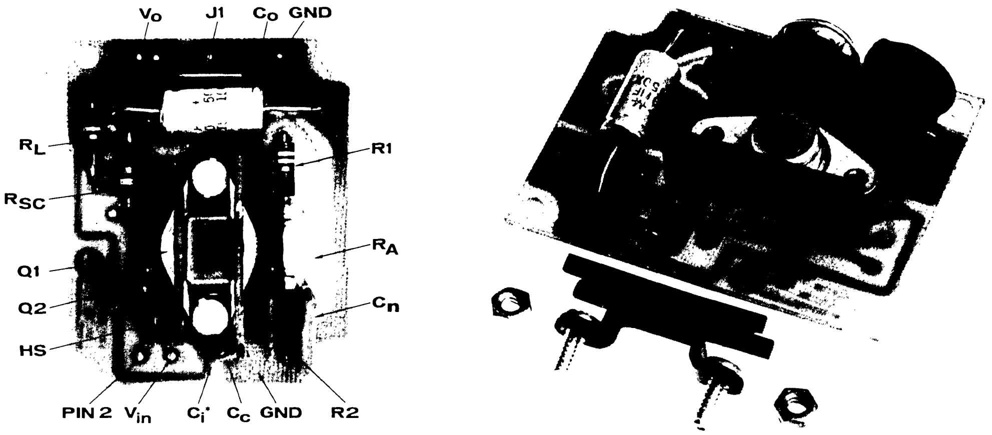
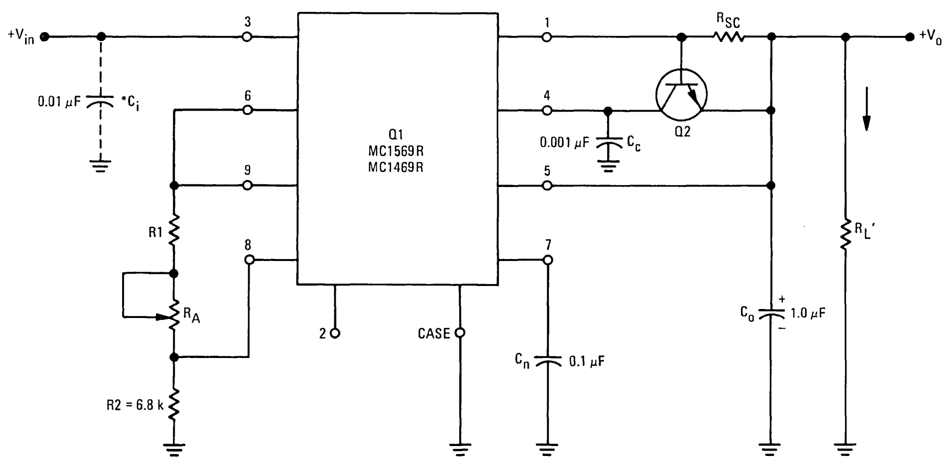
FIGURE 42 – LOCATION OF COMPONENTS



*Ci not shown

FIGURE 43 – CIRCUIT SCHEMATIC FOR PRINTED CIRCUIT BOARD (Pg. 17)
$3.5\ V \leq V_O \leq 37\ V,\ 1\ mA \leq I_L \leq 500\ mA$



Select R1 to give desired V_0: $R1 \approx (2\ V_0 - 7)\ k\Omega$

*C_i – May be required if long input leads are used.

PARTS LIST

Component	Value	Description
R1 R2	Select 6.8 k	1/4 or 1/2 watt carbon
*R_A	Select	IRC Model X-201 Mallory Model MTC-1 or equivalent
R_{SC}	Select	1/2 watt carbon
*R_L'	Select	For minimum current of 1 mAdc
C_o	1.0 μF	Sprague 1500 Series, Dickson D10C series or equivalent
C_n C_c *C_i	0.1 μF 0.001 μF 0.01 μF	Ceramic Disc – Centralab DDA104, Sprague TG-P10, or equivalent
Q1 Q2	MC1569R or MC1469R 2N5223, 2N706, or equivalent	
*HS	–	Heatsink Thermalloy #6168B
*Socket	(Not Shown)	Robinson Nugent #0001306 Electronic Molding Corp. #6341-210-1, 6348-188-1, 6349-188-1
PC Board	–	Circuit Dot, Inc. #PC1113 1155 W. 23rd St., Tempe, Ariz. 85281

*Optional

INDEX

MC1580L

MONOLITHIC DUAL LINE DRIVER/RECEIVER

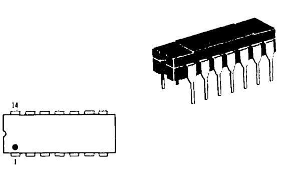
The output current of the MC1580L switches in response to a differential input voltage. A wide common-mode input and output voltage range makes this device ideal for transmission of digital information in a noisy environment. Typical applications include driving a twisted-pair transmission line, line sharing, voltage comparator, and logic level translation.

- High Input and Output Impedance – 5.0 k ohms at 10 MHz typ
- Low Propagation Delay – 18 ns max
- Wide Common-Mode Input and Output Voltage Range – ±3.5 V Input min and -3.0/+9.0 V Output min
- Input Gating Ability
- Bias Driver for MECL Applications, plus Interfacing Capability with MRTL, MDTL, and MTTL
- Compatible with Other Devices of the Line Driver/Receiver Series

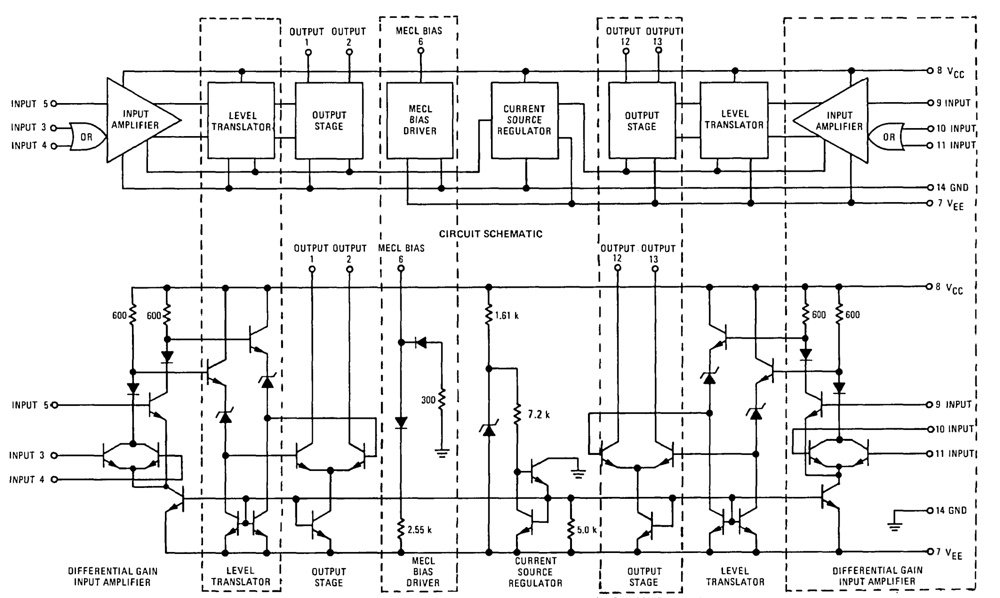
DUAL LINE DRIVER/RECEIVER INTEGRATED CIRCUIT

SILICON

EPITAXIAL PASSIVATED



Ceramic Package
Case 632
(TO-116)



See Packaging Information Section for outline dimensions.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+7.0 -7.0	Vdc
Differential–Mode Input Signal Voltage	V_{in}	±7.0	Volts
Common–Mode Input Signal Voltage	CMV_{in}	±10	Volts
Power Dissipation (Package Limitation) Ceramic Dual In-Line Package Derate above T_A = +25°C	P_D $1/\theta_{JA}$	 575 3.85	 mW mW/°C
Operating Temperature Range	T_A	–55 to +125	°C
Storage Temperature Range	T_{stg}	–65 to +175	°C

ELECTRICAL CHARACTERISTICS (Each Line Driver/Receiver, V_{CC} = +5.0 V, V_{EE} = –5.0 V, T_A = +25°C unless otherwise noted)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Operating Supply Currents	1	I_{CC} I_{EE}	– –	8.0 25	6.0 30	mA
Input Leakage Current	1	I_R	–	0.01	0.1	µA
Input Current T_A = –55°C T_A = +25°C T_A = +125°C	1	I_{in}	 – – –	 0.04 0.02 0.01	 0.2 0.1 0.1	mA
Output Leakage Current	1	I_{CEX}	–	0.8	5.0	µA
Output Load Current T_A = –55°C T_A = +25°C T_A = +125°C	1	I_{OL}	 6.5 6.9 6.8	 8.1 8.6 8.5	 9.8 10.4 10.2	mA
Output Load Current Match T_A = –55°C T_A = +25°C T_A = +125°C	6	ΔI_{OL}	 – – –	 0.25 0.2 0.15	 0.5 0.5 0.5	mA
Power Supply Operating Range		V_{CC} V_{EE}	+4.75 -4.75	+5.0 -5.0	+6.00 -6.00	Vdc
MECL Bias Voltage (V_{EE} = –5.2 Vdc)		V_{BB}	-1.11	–1.175	-1.24	Vdc
Input Voltage Transition Width* T_A = –55°C T_A = +25°C T_A = +125°C		V_{TR}	 – – –	 30 35 40	 50 50 50	mV
Switching Times Propagation Delay Time Rise Time Fall Time	2	 t_{pd+} t_{pd-} t_r t_f	 – – – –	 13 13 11 7.0	 18 18 – –	 ns
Parallel Impedance (f = 5.0 MHz) Input Capacitance Input Resistance Output Capacitance Output Resistance		 C_p (in) R_p (in) C_p (out) R_p (out)	 – – – –	 9.0 8.0 10 10	 – – – –	 pF k ohms pF k ohms
Common–Mode Voltage Range (–55 to +125°C) Input Output	 3 4	 $CMVR_{in}$ $CMVR_{out}$	 +3.5 -3.5 +9.0 –3.0	 +4.4 –4.2 +10 –3.3	 – – –	 Volts
Common–Mode Voltage Gain f = 60 MHz	5	A_{CMV}	 –	 –40	 –	dB
Power Dissipation		P_D	–	150	180	mW

*Measurement taken from points of Unity Gain.
Ground unused output pins and their corresponding inputs to assure correct device biasing.

CHARACTERISTIC DEFINITIONS

FIGURE 1 – TERMINAL CURRENTS

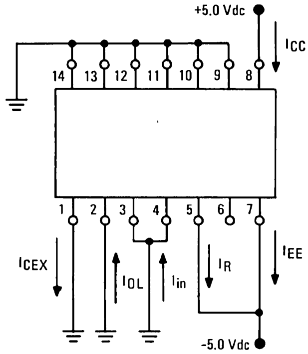


FIGURE 2 – TRANSIENT RESPONSE

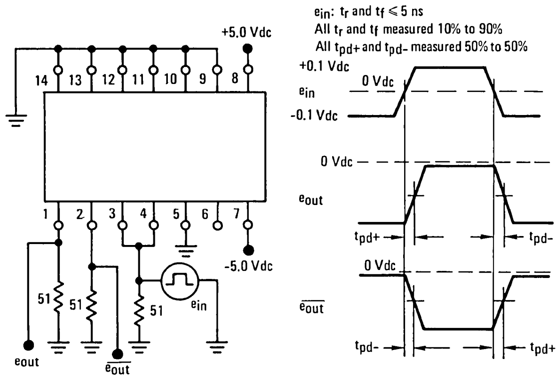


FIGURE 3 – COMMON-MODE INPUT VOLTAGE RANGE

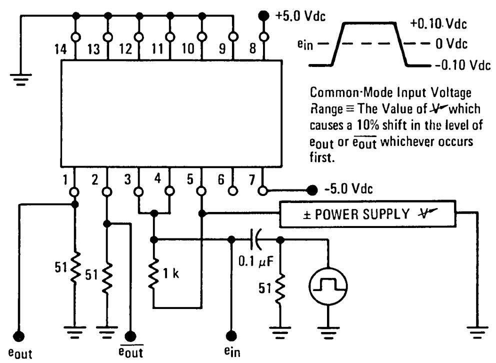


FIGURE 4 – COMMON-MODE OUTPUT VOLTAGE RANGE

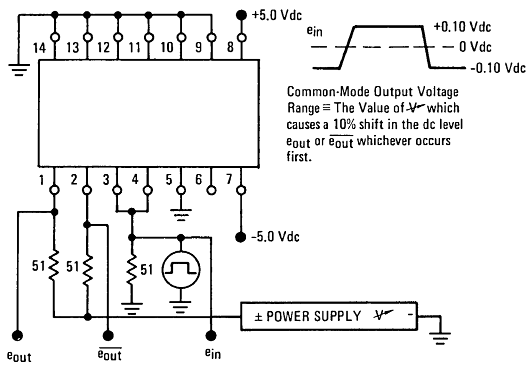


FIGURE 5 – COMMON-MODE VOLTAGE GAIN

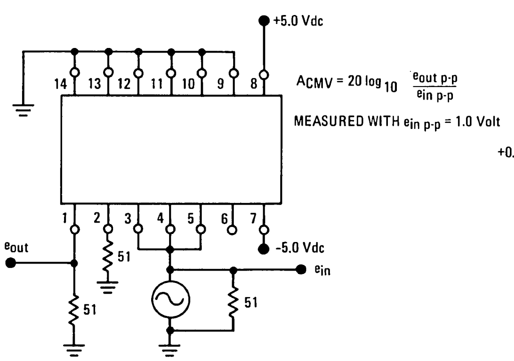
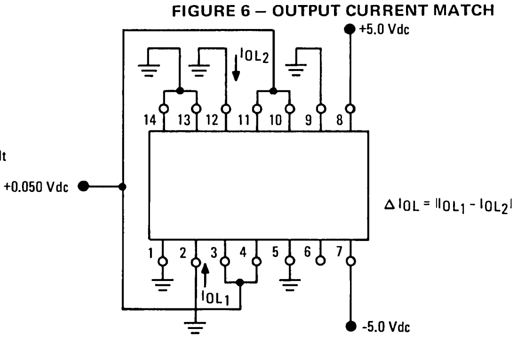


FIGURE 6 – OUTPUT CURRENT MATCH



TYPICAL CHARACTERISTICS

FIGURE 7 – OUTPUT LOAD CURRENT versus SUPPLY OPERATING VOLTAGE AND TEMPERATURE

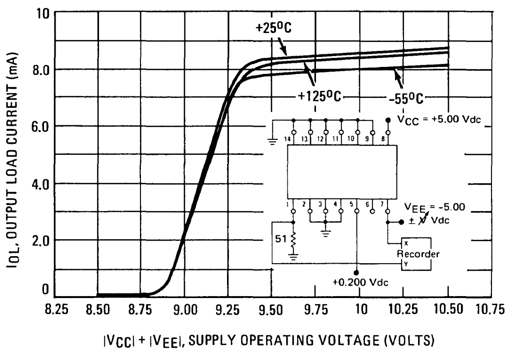


FIGURE 8 – EXPANDED OUTPUT LOAD CURRENT versus SUPPLY OPERATING VOLTAGE AT +25°C

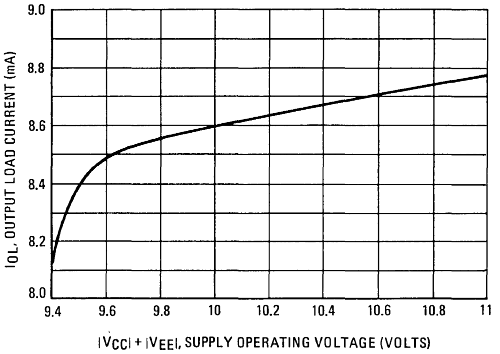


FIGURE 9 – OUTPUT LOAD CURRENT versus DIFFERENTIAL INPUT VOLTAGE AND TEMPERATURE

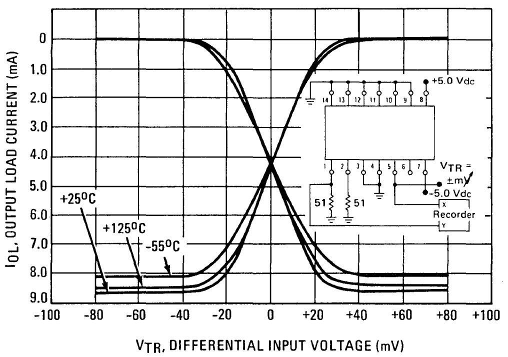


FIGURE 10 – PROPAGATION DELAY versus DIFFERENTIAL INPUT VOLTAGE

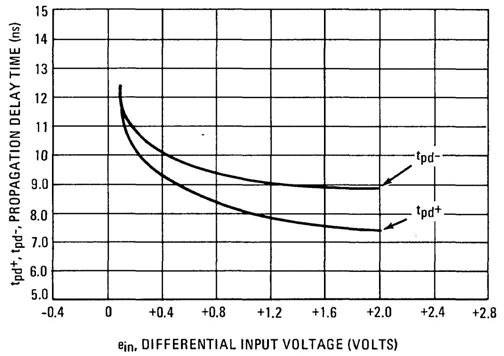
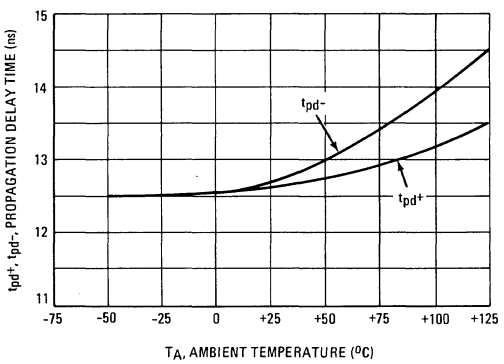


FIGURE 11 – PROPAGATION DELAY versus AMBIENT TEMPERATURE



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TYPICAL CHARACTERISTICS (continued)

FIGURE 12 – INPUT IMPEDANCE versus FREQUENCY

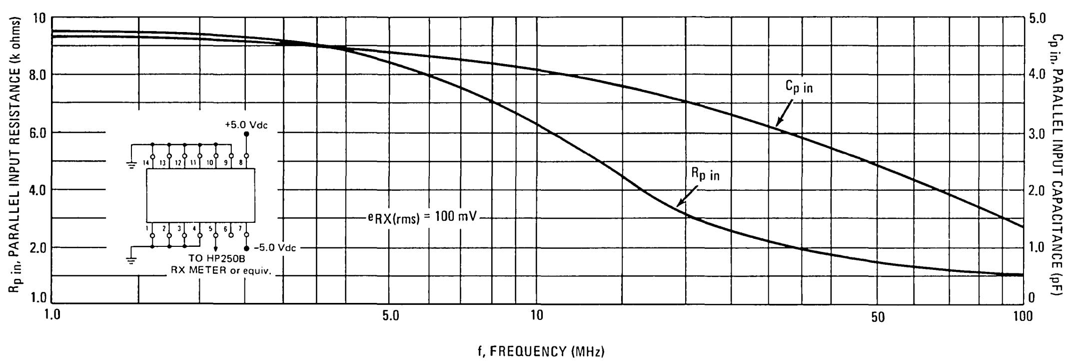


FIGURE 13 – OUTPUT IMPEDANCE versus FREQUENCY

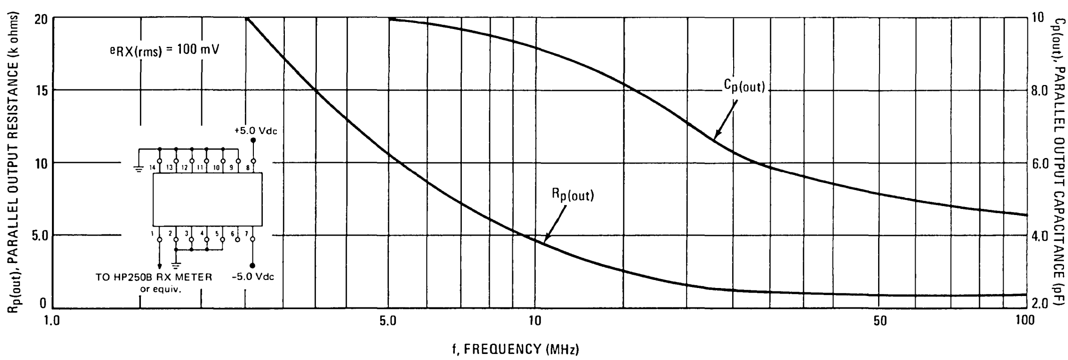
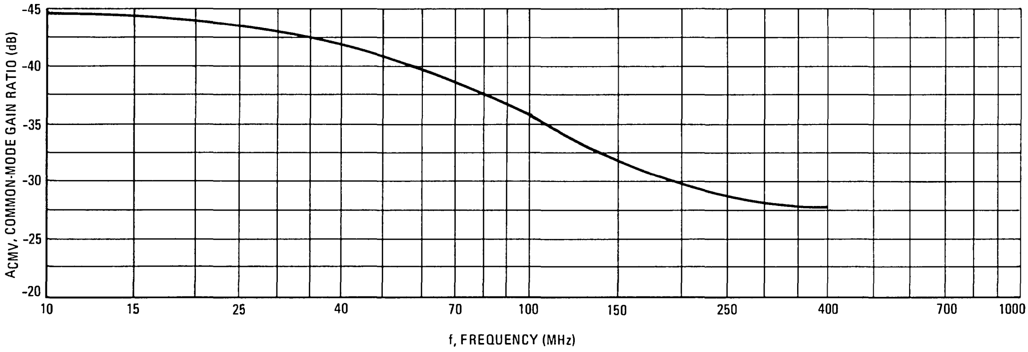


FIGURE 14 – COMMON-MODE GAIN RATIO versus FREQUENCY



6

APPLICATIONS INFORMATION

Line Driver/Receiver Family Characteristics

The Motorola line driver/receiver series provides interface circuits for driving digital data transmission lines e.g., coaxial cable or twisted pair. The digital data transmission is via a balanced differential mode. The line drivers and receivers are designed to provide high common-mode noise rejection, present high impedances to the transmission line and have low propagation times. A feature of the drivers is the capability to operate in a party-line mode whereby a number of drivers can be connected to a single line. This series provides drivers and receivers compatible with MRTL, MDTL, MTTL and MECL. The five circuits of the family are:

MC1580L	Dual Line Driver/Receiver
MC1581L	Dual MECL Receiver
MC1582L	Dual MDTL/MTTL Driver
MC1583L	Dual Receiver (Open Collector)
MC1584L	Dual Receiver (Active Pullup)

Figure 15 indicates line drivers and receivers recommended for interfacing with each of the various digital logic families. The MC1580L serves as a basic building block and can be used as a driver or receiver with any of the indicated digital logic families by adding the appropriate external components.

FIGURE 15

Digital Logic Family	Driver	Receiver
MECL	MC1580L	MC1581L
MDTL	MC1582L	MC1583L MC1584L
MTTL	MC1582L	MC1583L MC1584L
MRTL	MC1580L MC1582L	MC1583L

These five circuits are extremely useful in numerous applications other than line drivers and receivers. The differential amplifier input of the receiver makes it useful in applications such as voltage comparators, waveform generators and high-input-impedance buffers. The drivers and receivers are useful as logic level translators.

The MC1580L in Figure 16 serves as the line driver and line receiver for a balanced differential transmission line. The driver input and receiver outputs of Figure 16 are compatible with MRTL.

The output stage of the driver switches a current source between the two driver outputs in response to the input logic signals. Hence, a voltage differential that is a function of the line termination impedances is created on the twisted pair and at the input of the receiver. The receiver is designed to reject +3.5/−3.5 Volts of common-mode voltage signals which may be present due to ground loop currents and noise coupled from nearby transmission lines.

While common-mode noise is the major concern in a twisted pair transmission line; a good data transmission system must offer some immunity from differential-mode voltages that may be present due to mismatches in termination impedances. The drivers and receivers of the MC1580 Series are designed with this requirement in mind. The exact amount of noise immunity depends on line impedances but the following example shows how differential-mode noise immunity is calculated for a given system. For a line with a characteristic impedance of Z_O, calculate the minimum differential input voltage from the equation.

$$\pm V_{in} = \frac{I_O(min) \times Z_O}{4}$$

For a 170-ohm line, $V_{in} = \frac{(6.9)\ (170)}{4} = 0.29$ Volts.

Since the MC1580L requires 50 mV maximum input differential to maintain the output state, the worst case differential-mode noise immunity is 0.26 V. (See Figure 17).

FIGURE 17

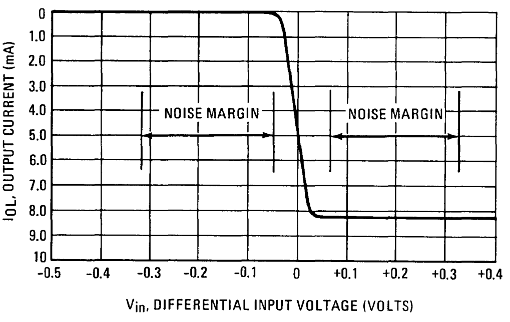
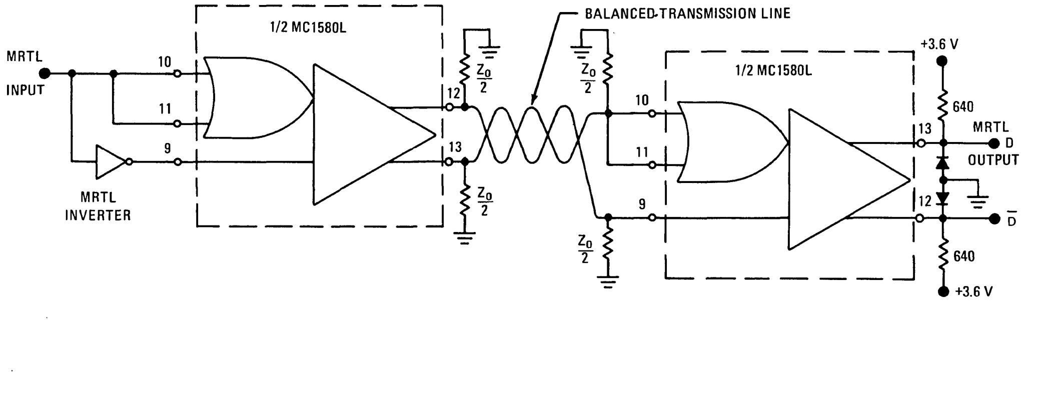


FIGURE 16



APPLICATIONS INFORMATION (continued)

Hence the direct coupling of the driver and receiver to the line provides a built-in differential-mode noise immunity. The direct coupling also matches the line at all frequencies (often a problem with ac coupling lines). The recovery problem in ac coupling devices at high-signal repetition rates is also eliminated.

High input and output impedances of the MC1580L minimize impedance discontinuities on the transmission line and allow many drivers and receivers to be connected to the line.

Use of the MC1580L in a bi-directional MECL compatible transmission system is shown in Figure 18. The MC1580L has an internal MECL bias network that allows the circuit to be used as a MECL line driver. The drivers of Figure 18 are connected so that the current sources from both drivers pull current from the same wire of the twisted pair when both drivers are transmitting logic "0" signals. The external current source, I_S, supplies the current required by one driver. The current for the other driver is drawn from the termination impedances, creating a voltage differential across the line. When either driver transmits a logic "1", a voltage difference of the opposite polarity is created across the line. For a system with two drivers the current source (I_S) can be supplied by a 600-ohm resistor connected to +5.0 Volts.

If additional drivers are connected to the line, a matching current source is connected for each added driver. The current sources are connected to the line so that when all drivers are transmitting logic "0"s, the difference in current drawn from the terminating resistors of the two wires in the twisted pair is equal to one current source (8.6 mA). The current sources should also be connected so that when any driver transmits a logic "1" then a current difference of the opposite polarity exists. The matching current source should be the companion circuit on the MC1580L driver chip. The difference in amplitude of the current sources on a single chip is specified to allow the system designer to calculate the maximum current source mismatch, ΔI_{OL}, and hence the maximum number of drivers that can be connected to a given transmission line.

The MC1580L has many other uses in a digital system. The high input impedance suggests its use as a buffer for delay lines and in waveform generation circuits. Figure 19 shows the MC1580L used as a differential comparator in a double-ended limit detector. When the input signal amplitude is between the two reference voltages, the output signal will be a logic "1"; otherwise a logic "0" output is obtained. The voltage transition region is typically less than 40 mV. External components R1 and CR1 establish an MDTL compatible signal.

FIGURE 18 – BI-DIRECTIONAL TRANSMISSION

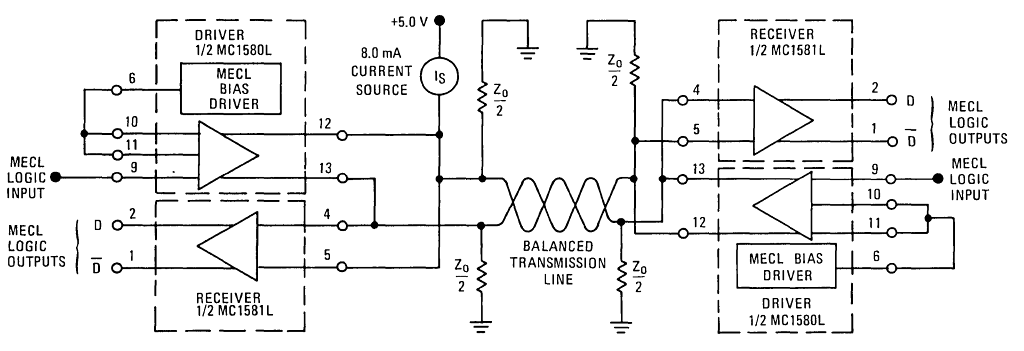
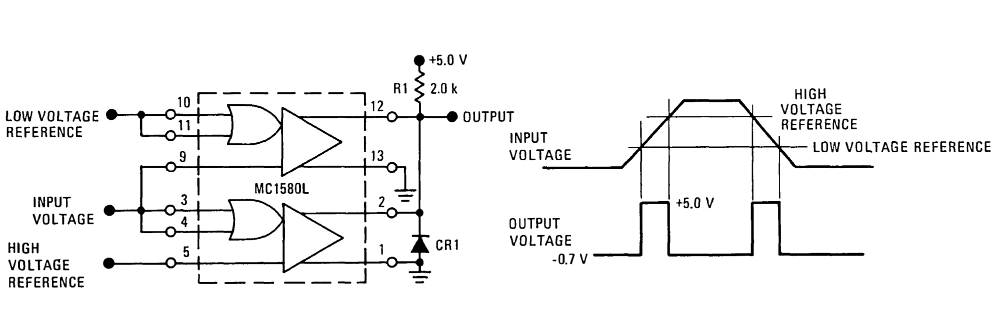


FIGURE 19 – DOUBLE-ENDED LIMIT DETECTOR

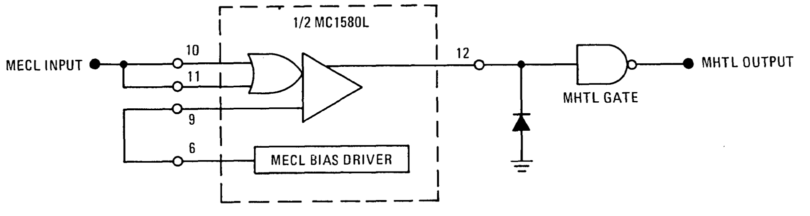


APPLICATIONS INFORMATION (continued)

Voltage Translator

Translation of voltage levels from MECL (best suited for the high-speed portion of a digital system) to MHTL (tailored for the noisy output portion of the system) is often required. The MC1580 performs this function as indicated in Figure 20.

FIGURE 20 – MECL TO MHTL VOLTAGE LEVEL TRANSLATOR



LINEAR/DIGITAL INTERFACE CIRCUITS

MC1581L

MONOLITHIC DUAL MECL LINE RECEIVER

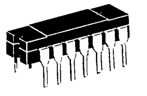
. . . designed with output emitter follower voltage levels that switch in response to a differential input voltage. The device output voltage levels are compatible with that of the MECL digital logic family. With its excellent common-mode input voltage range, the MC1581L is ideally suited for receiving digital data in noisy environments. Typical applications include line sharing, voltage comparator, and level translation.

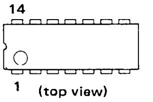
- High Input Impedance – 8.0 k ohms @ 10 MHz
- Low Propagation Delay Time – 20 ns max
- Wide Common-Mode Input Voltage Range – ±3.5 Vdc
- Device Compatability with Other Members of the Line Driver/Receiver Series

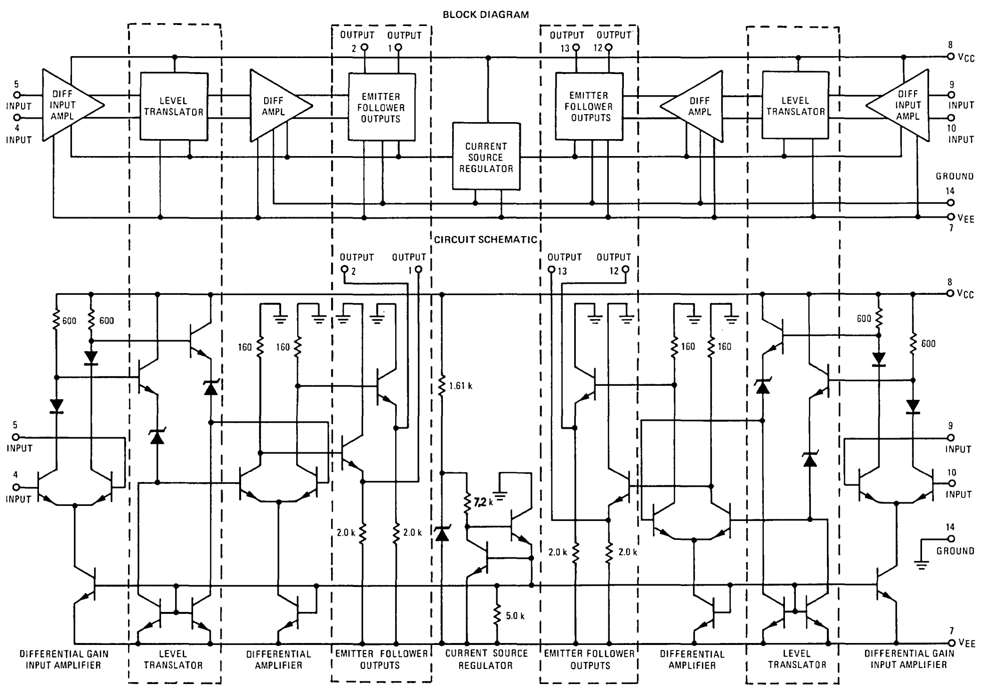
DUAL MECL LINE RECEIVER INTEGRATED CIRCUIT

MONOLITHIC SILICON EPITAXIAL PASSIVATED

CASE 632
CERAMIC PACKAGE
TO-116







See Packaging Information Section for outline dimensions.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+7.0 -7.0	Vdc
Differential-Mode Input Signal Voltage	V_{in}	±7.0	Volts
Common-Mode Input Signal Voltage	CMV_{in}	±10	Volts
Power Dissipation (Package Limitation) Ceramic Dual In-Line Package Derate above T_A = +25°C	P_D $1/\theta_{JA}$	 575 3.85	 mW mW/°C
Operating Temperature Range	T_A	-55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +175	°C

ELECTRICAL CHARACTERISTICS (Each Receiver, V_{CC} = +5.0 Vdc, V_{EE} = -5.2 Vdc, T_A = +25°C unless otherwise noted)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Operating Supply Currents	1	I_{CC} I_{EE}	– –	5.3 22.2	8.0 28.1	mA
Input Leakage Current	1	I_R	–	–	0.1	µA
Input Current T_A = -55°C T_A = +25°C T_A = +125°C	1	I_{in}	 – – –	 0.020 0.014 0.012	 0.1 0.1 0.1	mA
Output Voltage High T_A = -55°C T_A = +25°C T_A = +125°C	1	V_{OH}	 -0.825 -0.690 -0.535	 -0.900 -0.780 -0.62	 -0.990 -0.850 -0.700	Volt
Output Voltage Low T_A = -55°C T_A = +25°C T_A = +125°C	1	V_{OL}	 -1.580 -1.500 -1.380	 -1.83 -1.70 -1.73	 – – –	Volts
Input Voltage Transition Width* T_A = -55°C T_A = +25°C T_A = +125°C		V_{TR}	 – – –	 20 20 30	 50 50 50	mV
Switching Times Propagation Delay Time Rise Time Fall Time	2	 t_{pd+} t_{pd-} t_r t_f	 – – – –	 15 25 12 23	 20 30 – –	 ns
Parallel Input Impedance (f = 5.0 MHz) Capacitance Resistance		 C_p (in) R_p (in)	 – –	 4.5 14	 – –	 pF k ohms
Common-Mode Input Voltage Range (T_A = -55 to +125°C)	3	$CMVR_{in}$	+3.5 -3.5	+4.4 -4.2	– –	Volts
Power Supply Operating Range		V_{CC} V_{EE}	+4.75 -4.75	+5.0 -5.2	+6.00 -6.00	Vdc
Total Power Dissipation		P_D	–	145	185	mW

*Measurement taken from points of Unity Gain.
Ground unused inputs to assure correct device biasing.

6

CHARACTERISTIC DEFINITIONS

FIGURE 1 – TERMINAL CURRENTS AND VOLTAGES

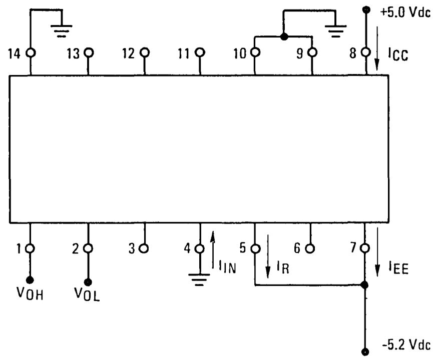


FIGURE 2 – TRANSIENT RESPONSE

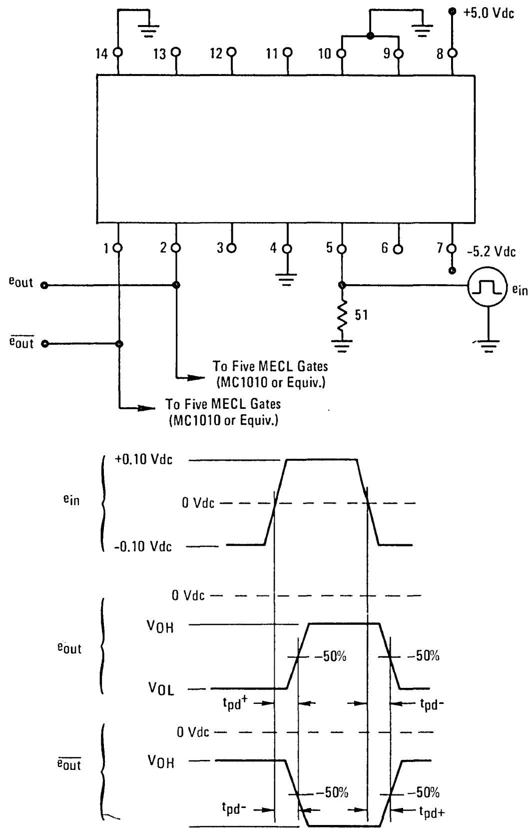
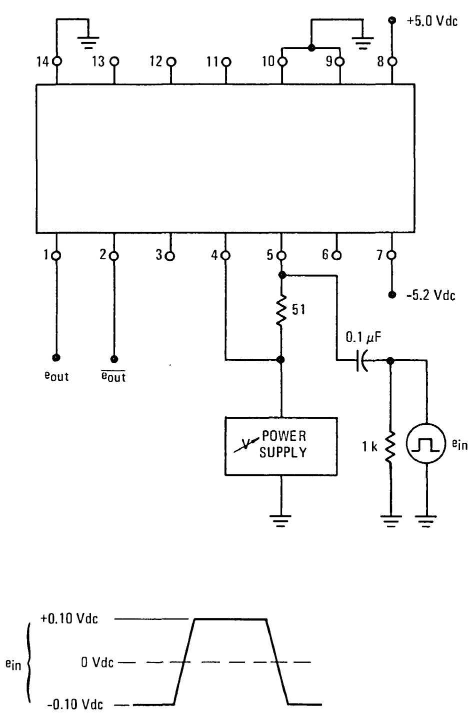


FIGURE 3 – COMMON-MODE INPUT VOLTAGE RANGE



Common-Mode Input Voltage Range is that value of the variable supply (V) which causes a 10% shift in e_{out} or $\overline{e_{out}}$ whichever occurs first.

TYPICAL CHARACTERISTICS

FIGURE 4 – OUTPUT VOLTAGE versus INPUT VOLTAGE AND TEMPERATURE

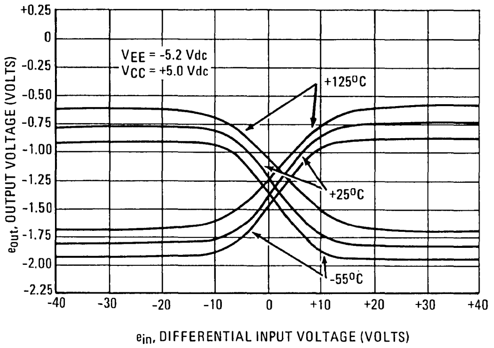


FIGURE 5 – OUTPUT VOLTAGE versus INPUT VOLTAGE AND SUPPLY VARIATION

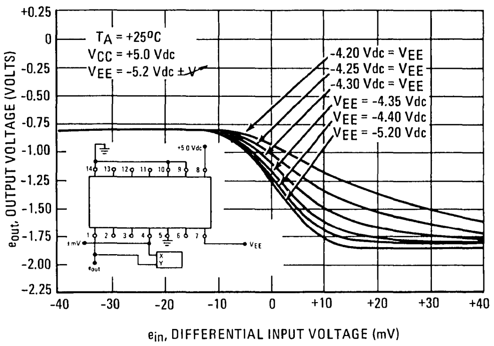


FIGURE 6 – PROPAGATION DELAY versus DIFFERENTIAL INPUT VOLTAGE

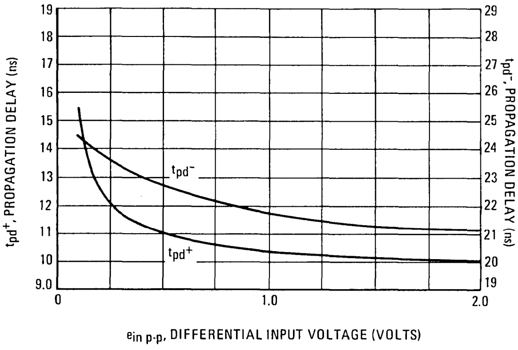


FIGURE 7 – PROPAGATION DELAY versus AMBIENT TEMPERATURE

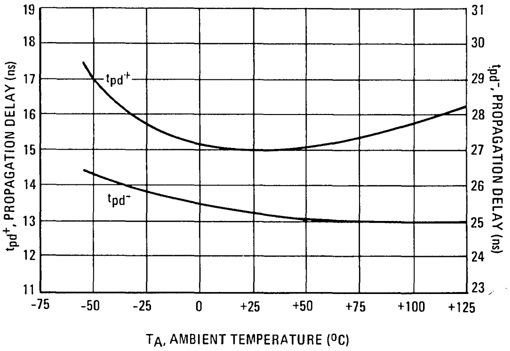
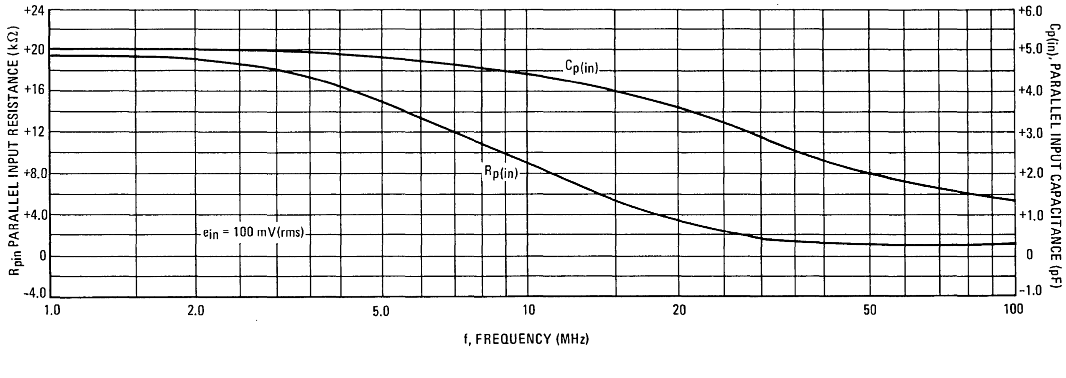


FIGURE 8 – PARALLEL INPUT IMPEDANCE versus FREQUENCY



APPLICATIONS INFORMATION

Line Driver/Receiver Family Characteristics

The Motorola line driver/receiver series provides interface circuits for driving digital data transmission lines, e.g., coaxial cable or twisted pair. The digital data transmission is via a balanced differential mode. The line drivers and receivers are designed to provide high common-mode noise rejection, present high impedances to the transmission line and have low propagation times. A feature of the drivers is the capability of operating in a party-line mode whereby a number of drivers can be connected to a single line. The series provides both drivers and receivers compatible with MRTL, MDTL, MTTL and MECL. The five circuits of the family are:

MC1580L	Dual Line Driver/Receiver
MC1581L	Dual MECL Receiver
MC1582L	Dual MDTL/MTTL Driver
MC1583L	Dual Receiver (Open Collector)
MC1584L	Dual Receiver (Active Pullup)

Figure 9 indicates the line drivers and receivers recommended for interfacing with each of the various digital logic families.

FIGURE 9

Digital Logic Family	Driver	Receiver
MECL	MC1580L	MC1581L
MDTL	MC1582L	MC1583L MC1584L
MTTL	MC1582L	MC1583L MC1584L
MRTL	MC1580L MC1582L	MC1583L

These five circuits are extremely useful in numerous applications other than line drivers and receivers. The differential amplifier input of the receiver makes it useful in such applications as voltage comparators, waveform generators and high-input impedance buffers. The drivers and receivers are useful as logic level translators.

The MC1581L in Figure 10 serves as the line receiver in a balanced differential transmission line. The outputs of the MC1581L receiver and the inputs to the MC1580L driver are compatible with MECL.

While common-mode noise is the major concern in a twisted pair transmission line, a good data transmission system must offer some immunity from differential-mode voltages that may be present due to mismatches in termination impedances. The drivers and receivers of the MC1580 series are designed with this requirement in mind. The exact amount of noise immunity depends on line impedances but the following example shows how differential-mode noise immunity is calculated for a given system. For a line with a characteristic impedance of Z_o, calculate the minimum differential input voltage from the equation:

$$\pm V_{in} = \frac{I_{o(min)} \times Z_o}{4}$$

For a 170-ohm line, $V_{in} \frac{(6.9)\ (170)}{4} = 0.29$ Volts

Since the MC1581L requires a 50 mV maximum input differential to maintain the output state, the worst case differential-mode noise immunity is 0.26 V, (see Figure 11).

FIGURE 11

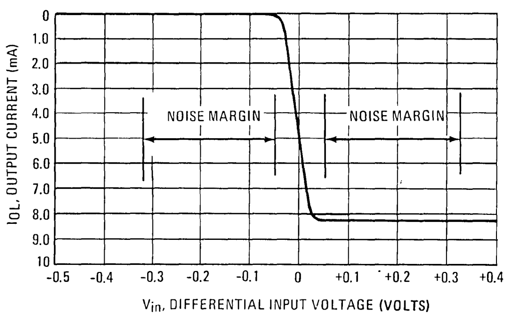
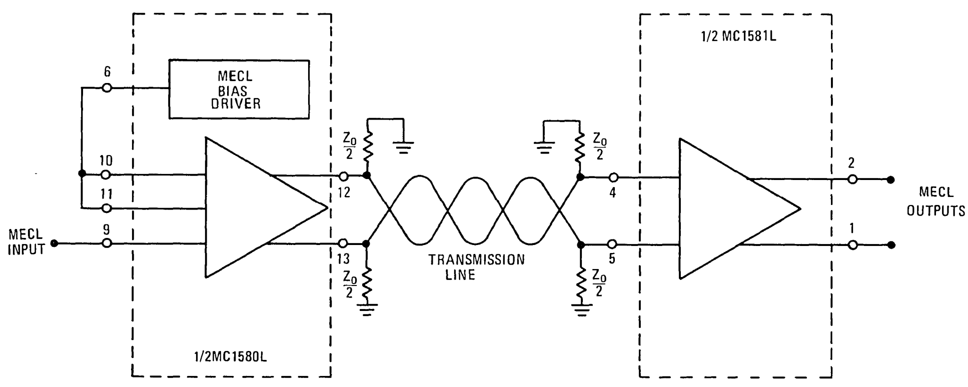


FIGURE 10 – MECL COMPATIBLE TRANSMISSION SYSTEM



The output stage of the driver switches a current source between the two driver outputs in response to the input logic signals. Hence, a voltage differential that is a function of the line termination impedances is created on the twisted pair and at the input of the receiver. The receiver is designed to reject +3.5/–3.5 volts of common-mode voltage signals which may be present due to ground loop currents and noise coupled from nearby transmission lines.

Hence the direct coupling of the driver and receiver to the line provides a built-in differential-mode noise immunity. The direct coupling also matches the line at all frequencies (often a problem with ac coupled lines). The recovery problem in ac coupling devices at high-signal repetition rates is also eliminated.

High input impedance of the MC1581L and high output impedance of the MC1580L minimize impedance discontinuities on the

APPLICATIONS INFORMATION (continued)

transmission line and allow many drivers and receivers to be connected to the line.

Use of the MC1581L and the MC1580L in a bi-directional MECL compatible transmission system is shown in Figure 12. The MC1580L has an internal MECL bias network that allows the circuit to be used as a MECL line driver. The drivers of Figure 12 are connected so that the current sources from both drivers pull current from the same wire of the twisted pair when both drivers are transmitting logic "0" signals. The external current source, I_S, supplies the current required by one driver. The current for the other driver is drawn from the termination impedances creating a voltage differential across the line. When either driver transmits a logic "1", a voltage difference of the opposite polarity is created across the line. For a system with two drivers the current source (I_S) can be supplied by a 600-ohm resistor connected to +5.0 Volts.

If additional drivers are connected to the line, a matching current source must be connected for each added driver. The current sources are connected to the line so that when all drivers are transmitting logic "0"s, the difference in current drawn from the terminating resistors of the two wires in the twisted pair is equal to one current source (8.6 mA). The current sources should also be connected so that when any driver transmits a logic "1" a current difference of the opposite polarity exists. The matching current source should be the companion circuit on the MC1580L driver chip. The difference in amplitude of the current sources on a single chip is specified to allow the system designer to calculate the maximum current source mismatch, ΔI_{OL}, and hence the maximum number of drivers that can be connected to a given transmission line.

Voltage Translator

Translation of voltage levels from MHTL (tailored for the noisy input/output system portions) to MECL (best suited for the high-speed logic circuits) is often required. The MC1581L performs this function as shown in Figure 13.

FIGURE 12 – BI-DIRECTIONAL TRANSMISSION

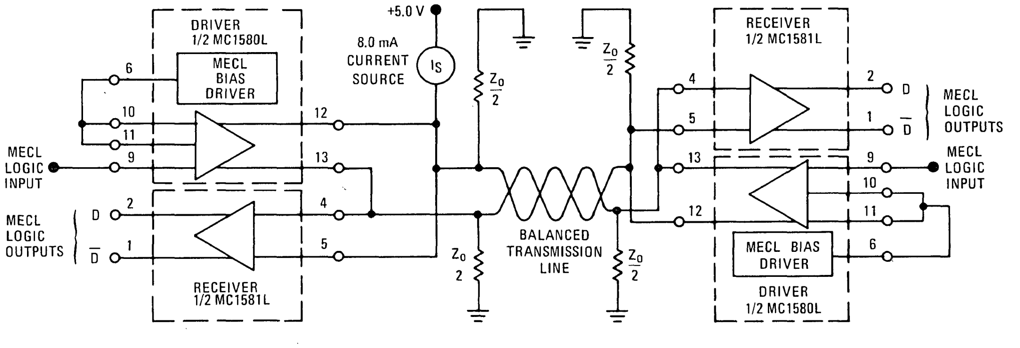
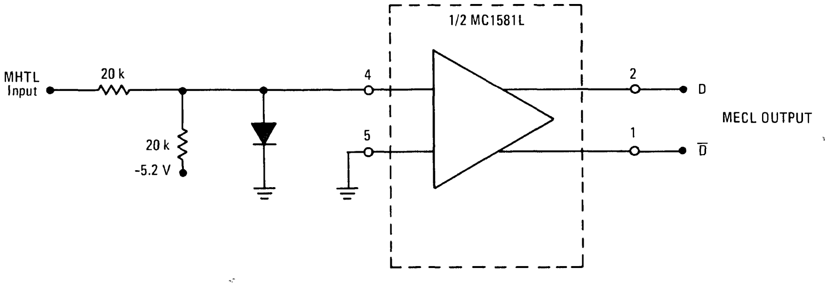


FIGURE 13 – MHTL-TO-MECL VOLTAGE LEVEL TRANSLATOR



MC1582L

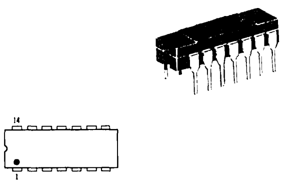
MONOLITHIC DUAL MDTL/MTTL LINE DRIVER

. . . designed with a three-input AND gate input circuit. The differential output current switches in response to an MDTL or MTTL compatible input voltage level. Typical applications include driving twisted-pair transmission lines, line sharing, and logic level translation.

- Low Propagation Delay Time – 20 ns max
- Wide Common-Mode Output Voltage Range – +9.0/-3.0 Volts
- High Output Impedance – 7.0 k Ohms @ 10 MHz
- 3-Input AND Gate
- Device Compatibility with Other Members of the Line Driver/Receiver Series

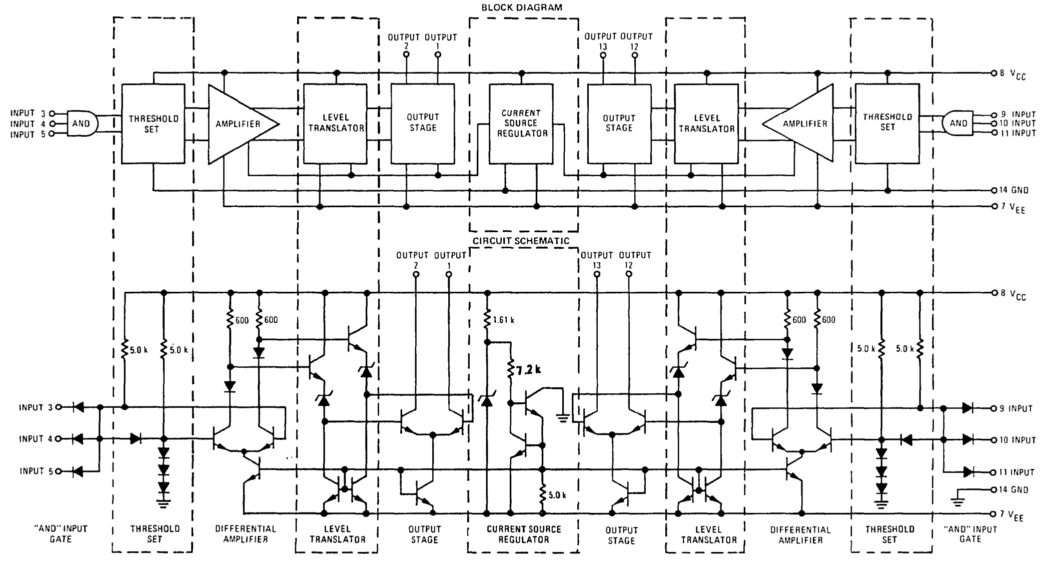
DUAL MDTL/MTTL LINE DRIVER INTEGRATED CIRCUIT

MONOLITHIC SILICON EPITAXIAL PASSIVATED



(top view)

CERAMIC PACKAGE
CASE 632
TO-116



See Packaging Information Section for outline dimensions.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+7.0 –7.0	Vdc
Input Signal Voltage	V_{in}	+30	Volts
Power Dissipation (Package Limitation) Ceramic Dual In-Line Package Derate above T_A = +25°C	P_D $1/\theta_{JA}$	 575 3.85	 mW mW/°C
Operating Temperature Range	T_A	–55 to +125	°C
Storage Temperature Range	T_{stg}	–65 to +175	°C

ELECTRICAL CHARACTERISTICS (Each Line Driver, V_{CC} = +5.0 Vdc, V_{EE} = –5.0 Vdc, T_A = +25°C unless otherwise noted)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Operating Supply Currents	1	I_{CC} I_{EE}	– –	8.0 25	10 30	mA
Input Leakage Current	1	I_R	–	0.04	0.1	µA
Input Current T_A = –55°C T_A = +25°C T_A = +125°C	1	I_{in}	 – – –	 0.72 0.70 0.63	 1.0 1.0 1.0	mA
Output Leakage Current	1	I_{CEX}	–	0.1	0.2	µA
Output Load Current T_A = –55°C T_A = +25°C T_A = +125°C	1	I_{OL}	 6.5 6.9 6.8	 8.1 8.6 8.5	 9.8 10.4 10.2	mA
Output Load Current Match T_A = –55°C T_A = +25°C T_A = +125°C	2	ΔI_{OL}	 – – –	 0.7 0.8 0.8	 – – –	mA
Input Voltage Transition Width* T_A = –55°C T_A = +25°C T_A = +125°C		V_{TR}	 – – –	 50 40 50	 – – –	mV
Switching Times Propagation Delay Time Rise Time Fall Time	 3	 t_{pd+} t_{pd-} t_r t_f	 – – – –	 15 13 8.0 7.0	 20 18 – –	 ns
Threshold Voltage T_A = –55°C T_A = +25°C T_A = +125°C	3	V_{TH}	 0.9 1.1 0.9	 1.74 1.45 1.16	 2.0 1.8 1.5	Volts
Parallel Output Impedance (f = 5.0 MHz) Capacitance Resistance		 $C_{p(out)}$ $R_{p(out)}$	 – –	 10 18	 – –	 pF k ohms
Common–Mode Output Voltage Range T_A = –55 to +125°C	4	$CMVR_{out}$	+9.0 –3.0	+10 –3.3	– –	Volts
Power Supply Operating Range		V_{CC} V_{EE}	+4.75 –6.0	+5.0 –5.0	+6.0 –4.75	Vdc
Input Breakdown Voltage		V_{IHH}	15	30	–	Volts
Power Dissipation		P_D	–	140	170	mW

*Measured from points of unity gain with a 50 ohm load.
Ground all unused input pins to assure correct device biasing.

CHARACTERISTIC DEFINITIONS

FIGURE 1 – TERMINAL CURRENTS

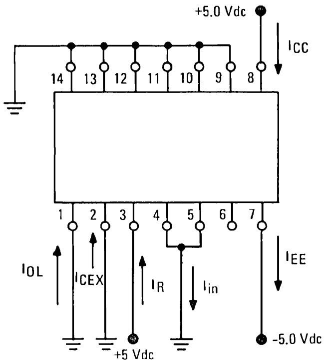


FIGURE 2 – OUTPUT CURRENT MATCH

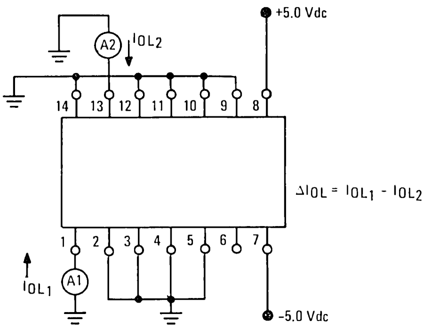


FIGURE 3 – TRANSIENT RESPONSE

All t_r and t_f measured 10% to 90%

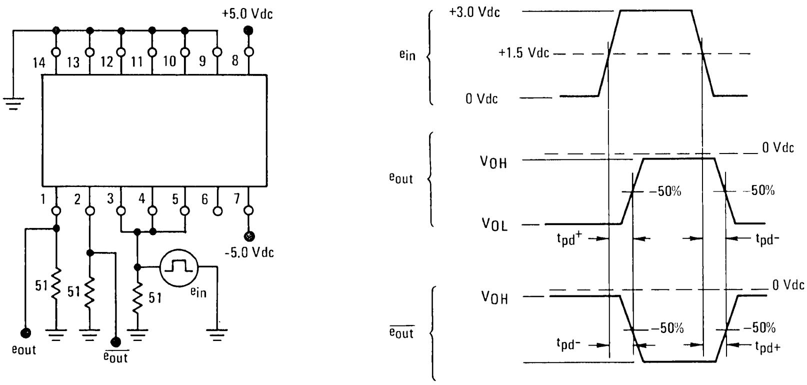
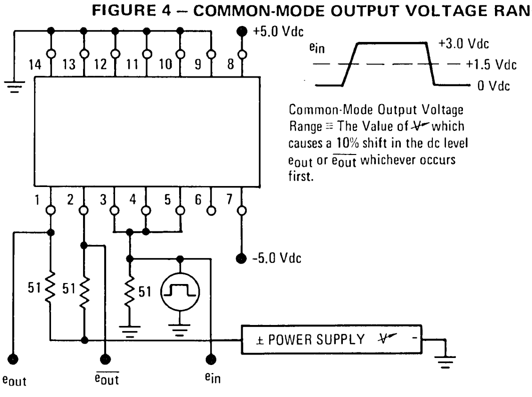


FIGURE 4 – COMMON-MODE OUTPUT VOLTAGE RANGE



Common-Mode Output Voltage Range ≡ The Value of V which causes a 10% shift in the dc level e_{out} or $\overline{e_{out}}$ whichever occurs first.

TYPICAL CHARACTERISTICS

FIGURE 5 – OUTPUT LOAD CURRENT versus SUPPLY OPERATING VOLTAGE AND TEMPERATURE

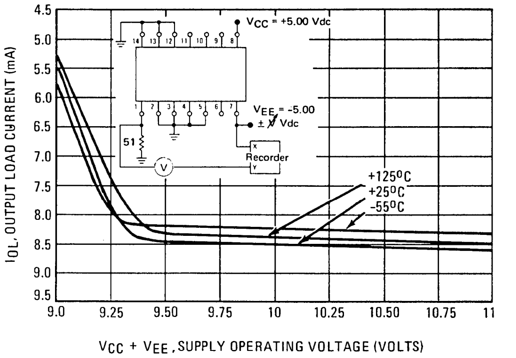


FIGURE 6 – OUTPUT LOAD CURRENT versus INPUT VOLTAGE AND TEMPERATURE

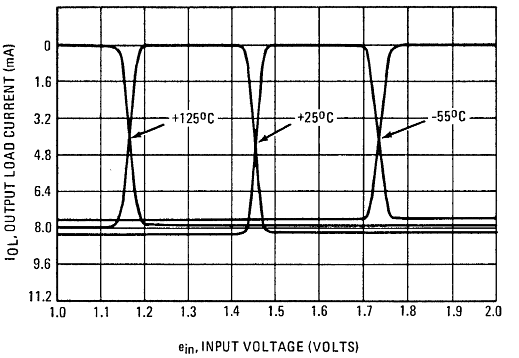


FIGURE 7 – PROPAGATION DELAY TIME versus AMBIENT TEMPERATURE

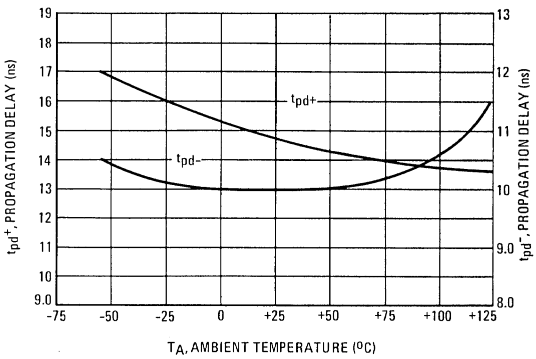
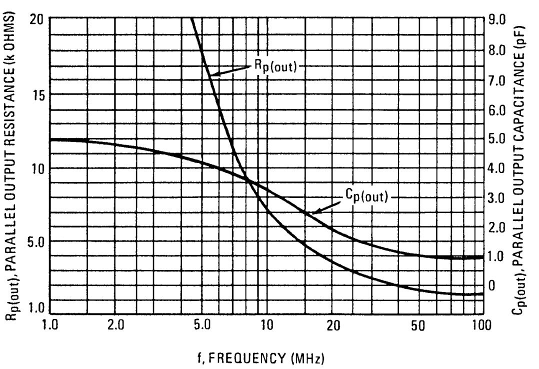


FIGURE 8 – PARALLEL OUTPUT IMPEDANCE versus FREQUENCY



6

APPLICATIONS INFORMATION

Line Driver/Receiver Family Characteristics

The Motorola line driver/receiver series provides interface circuits for driving digital data transmission lines e.g., coaxial cable or twisted pair. The digital data transmission is via a balanced differential mode. The line drivers and receivers are designed to provide high common-mode noise rejection, present high impedances to the transmission line and have low propagation times. A feature of the drivers is the capability to operate in a party-line mode whereby a number of drivers can be connected to a single line. This series provides drivers and receivers compatible with MRTL, MDTL, MTTL and MECL. The five circuits of the family are:

MC1580L	Dual Line Driver/Receiver
MC1581L	Dual MECL Receiver
MC1582L	Dual MDTL/MTTL Driver
MC1583L	Dual Receiver (Open Collector)
MC1584L	Dual Receiver (Active Pullup)

Figure 9 indicates line drivers and receivers recommended for interfacing with each of the various digital logic families.

FIGURE 9

Digital Logic Family	Driver	Receiver
MECL	MC1580L	MC1581L
MDTL	MC1582L	MC1583L MC1584L
MTTL	MC1582L	MC1583L MC1584L
MRTL	MC1580L MC1582L	MC1583L

These five circuits are extremely useful in numerous applications other than line drivers and receivers. The differential amplifier input of the receiver makes it useful in applications such as voltage comparators, waveform generators and high-input-impedance buffers. The drivers and receivers are useful as logic level translators.

The MC1582L in Figure 10 serves as the line driver for a balanced differential transmission line. The driver input and receiver outputs of the MC1584L receiver are compatible with MTTL circuits.

The output stage of the driver switches a current source between the two driver outputs in response to the input logic signals. Hence, a voltage differential that is a function of the line termination impedances is created on the twisted pair and at the input of the receiver. The receiver is designed to reject +3.5/−3.5 Volts of common-mode voltage signals which may be present due to ground loop currents and noise coupled from nearby transmission lines.

While common-mode noise is the major concern in a twisted pair transmission line; a good data transmission system must offer some immunity from differential-mode voltages that may be present due to mismatches in termination impedances. The drivers and receivers of the MC1580 Series are designed with this requirement in mind. The exact amount of noise immunity depends on line impedances but the following example shows how differential-mode noise immunity is calculated for a given system. For a line with a characteristic impedance of Z_o, calculate the minimum differential input voltage from the equation.

$$\pm V_{in} = \frac{I_o(\text{min}) \times Z_o}{4}$$

For a 170-ohm line, $V_{in} = \frac{(6.9)\ (170)}{4} = 0.29$ Volts.

Since the receivers recommended for use with the MC1582L driver require 50 mV maximum input differential to maintain the output state, the worst case differential-mode noise immunity is 0.26 V. (See Figure 11).

FIGURE 11

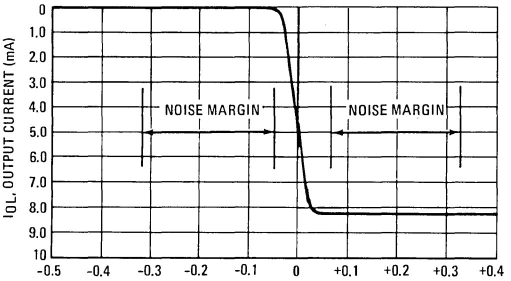
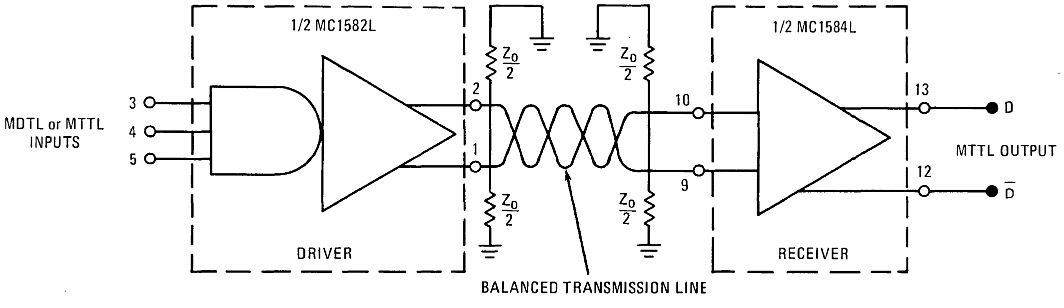


FIGURE 10 – MDTL, MTTL COMPATIBLE TRANSMISSION SYSTEM



APPLICATIONS INFORMATION (continued)

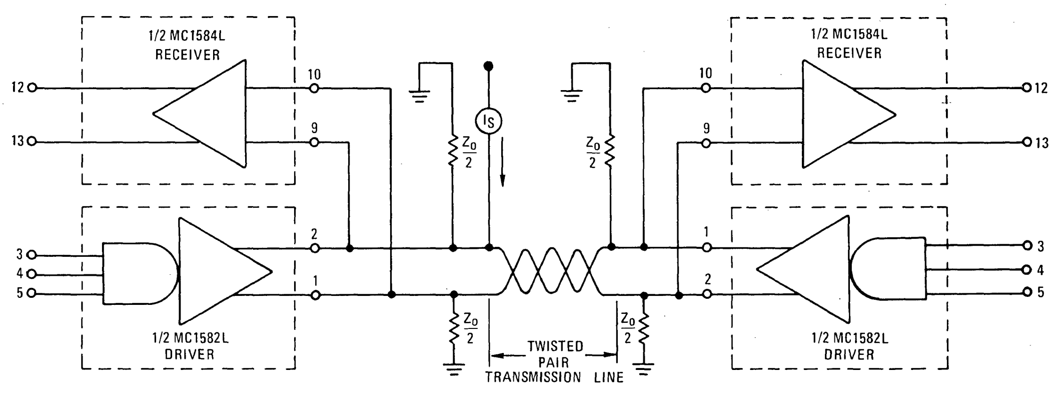
Hence the direct coupling of the driver and receiver to the line provides a built-in differential-mode noise immunity. The direct coupling also matches the line at all frequencies (often a problem with ac coupling lines). The recovery problem in ac coupling devices at high-signal repetition rates is also eliminated.

The high output impedance of the MC1582L and the high input impedances of the MC1584L drivers minimize impedance discontinuities on the transmission line and allow many drivers and receivers to be connected to the line.

Use of the MC1584L in a bi-directional MDTL or MTTL compatible transmission system is shown in Figure 12. The MC1582L drivers of Figure 12 are connected so that the current sources from both drivers pull current from the same wire of the twisted pair when both drivers are transmitting logic "0" signals. The external current source, I_S, supplies the current required by one driver. The current for the other driver is drawn from the termination impedances, creating a voltage differential across the line. When either driver transmits a logic "1", a voltage difference of the opposite polarity is created across the line. For a system with two drivers the current source (I_S) can be supplied by a 600-ohm resistor connected to +5.0 volts.

If additional drivers are connected to the line, a matching current source is connected for each added driver. The current sources are connected to the line so that when all drivers are transmitting logic "0"s, the difference in current drawn from the terminating resistors of the two wires in the twisted pair is equal to one current source (8.6 mA). The current sources should also be connected so that when any driver transmits a logic "1" then a current difference of the opposite polarity exists. The matching current source should be the companion circuit on the MC1580L driver chip. The difference in amplitude of the current sources on a single chip is specified to allow the system designer to calculate the maximum current source mismatch, ΔI_{OL}, and hence the maximum number of drivers that can be connected to a given transmission line.

FIGURE 12 – BI-DIRECTIONAL TRANSMISSION



MC1583L

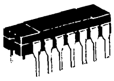
MONOLITHIC DUAL LINE RECEIVER

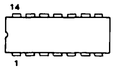
The MC1583L is a dual open collector output line receiver designed for use in line sharing, differential voltage comparator, and level translator applications. The output transistors switch in response to a differential input voltage. Output logic voltage levels are compatible with MTTL, MDTL, and MRTL logic levels when a suitable external pullup resistor is connected to the device output. Excellent common-mode input voltage range makes this device ideal for receiving digital data in a noisy environment.

- High Input Impedance — 12 Kilohms @ 5.0 MHz
- Low Propagation Delay Time — 40 ns max
- Excellent Common-Mode Input Voltage Range — ±3.5 V min
- Compatible with Other Members of the Line Driver/Receiver Series — MC1580 thru MC1584

DUAL SATURATED LOGIC RECEIVER (OPEN-COLLECTOR)
MONOLITHIC SILICON EPITAXIAL PASSIVATED

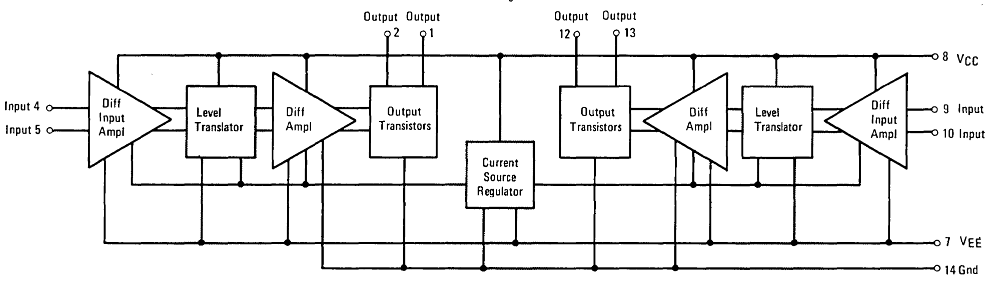
CERAMIC PACKAGE
CASE 632
TO-116



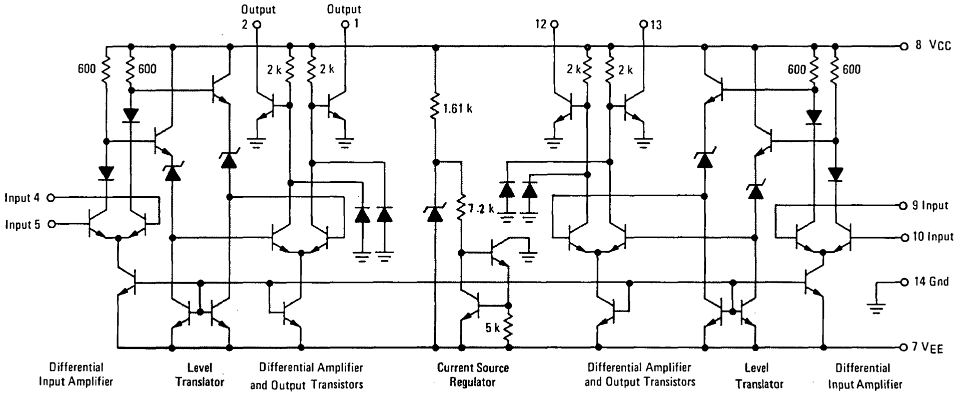


(top view)

Block Diagram



Circuit Schematic



See Packaging Information Section for outline dimensions.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+7.0 -7.0	Vdc
Differential-Mode Input Signal Voltage	V_{in}	±7.0	Vdc
Common-Mode Input Voltage	CMV_{in}	±10	Vdc
Static Output Load Current	I_{OL}	20	mA
Power Dissipation (Package Limitation) Derate above T_A = +25°C	P_D	575 3.85	mW mW/°C
Operating Temperature Range	T_A	-55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +175	°C

ELECTRICAL CHARACTERISTICS (Each Receiver)

(V_{CC} = +5.0 Vdc, V_{EE} = -5.0 Vdc, T_A = +25°C unless otherwise noted)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Operating Supply Currents	1	I_{CC} I_{EE}	– –	15 16	18 20	mA
Input Leakage Current	1	I_R	–	0.012	0.1	µA
Input Current T_A = -55°C T_A = +25°C T_A = +125°C	1	I_{in}	 – – –	 0.033 0.025 0.020	 0.1 0.1 0.1	mA
Output Leakage Current	1	I_{CEX}	–	0.8	5.0	µA
Output Voltage Low (I_{OL} = 20 mA) T_A = -55°C T_A = +25°C T_A = +125°C	1	V_{OL}	 – – –	 0.23 0.25 0.28	 0.40 0.40 0.40	Volt
Input Voltage Transition Width‡ T_A = -55°C T_A = +25°C T_A = +125°C		V_{TR}	 – – –	 12 4.0 8.0	 50 50 50	mV
Switching Times Propagation Delay Times Rise Time Fall Time	2	 t_{pd+} t_{pd-} t_r t_f	 – – – –	 24 34 16 5.0	 30 40 – –	ns
Parallel Input Impedance (f = 5.0 MHz) Parallel Input Capacitance Parallel Input Resistance		 C_p R_p	 – –	 4.0 12	 – –	 pF k ohms
Common-Mode Input Voltage Range T_A = -55°C to +125°C	3	CMV_{in}	+3.5 -3.5	+4.3 -4.2	– –	Volts
Power Supply Operating Range		V_{CC} V_{EE}	4.75 -6.0	5.0 -5.0	6.0 -4.75	Vdc
Total Power Dissipation		P_D	–	140	175	mW

Ground unused input pins to assure correct device biasing.

‡Measurement taken from points of Unity Gain with 3.9-kilohm load resistor.

TEST CIRCUITS AND TYPICAL CHARACTERISTICS

(V_{CC} = +5.0 Vdc, V_{EE} = -5.0 Vdc, T_A = +25°C unless otherwise noted)

FIGURE 1 – TERMINAL CURRENTS

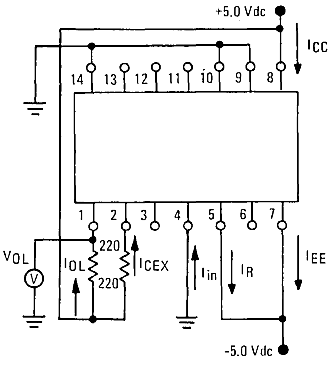


FIGURE 2 – TRANSIENT RESPONSE

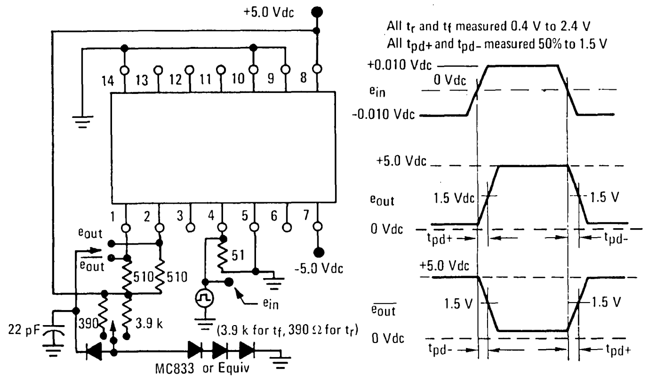


FIGURE 3 – COMMON-MODE INPUT VOLTAGE RANGE

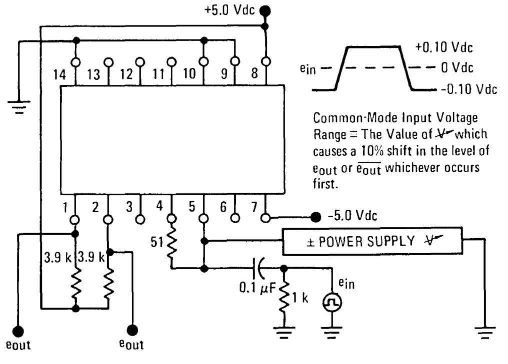


FIGURE 5 – OUTPUT VOLTAGE versus DIFFERENTIAL INPUT VOLTAGE AND TEMPERATURE

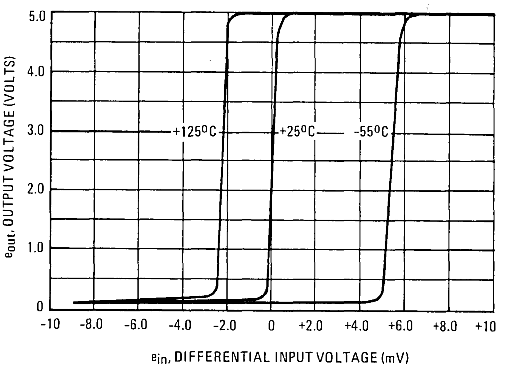
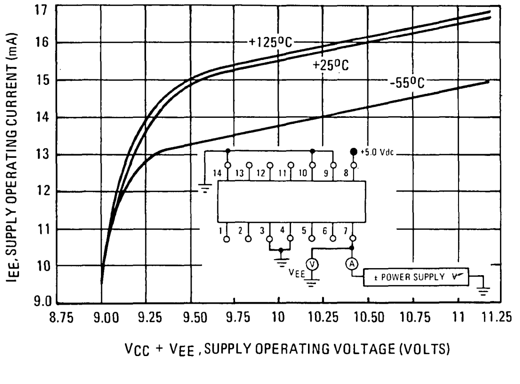
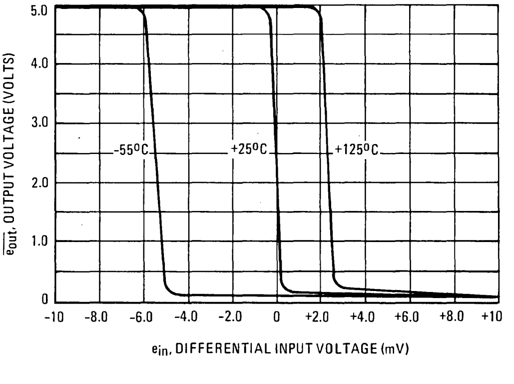


FIGURE 4 – SUPPLY OPERATING CURRENT versus SUPPLY OPERATING VOLTAGE AND TEMPERATURE





TYPICAL CHARACTERISTICS (continued)

(V_{CC} = +5.0 Vdc, V_{EE} = -5.0 Vdc, T_A = +25°C unless otherwise noted)

FIGURE 6 – OUTPUT SATURATION VOLTAGE versus OUTPUT LOAD CURRENT AND TEMPERATURE

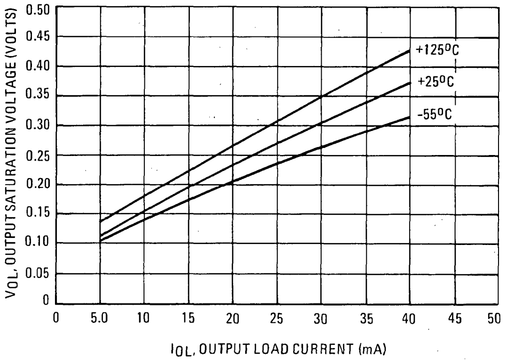


FIGURE 7 – PROPAGATION DELAY versus DIFFERENTIAL INPUT VOLTAGE

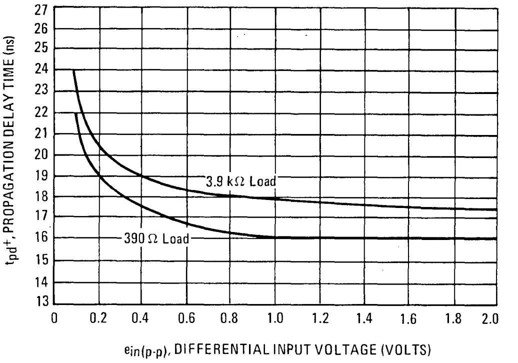


FIGURE 8 – PROPAGATION DELAY versus DIFFERENTIAL INPUT VOLTAGE

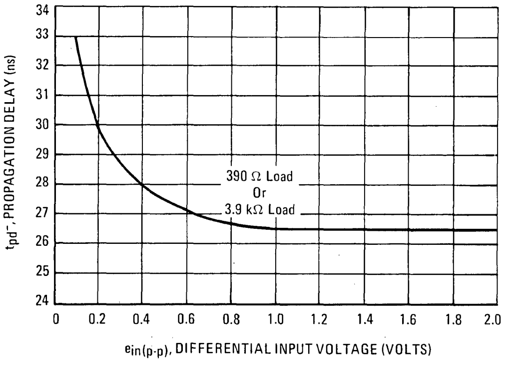


FIGURE 9 – PROPAGATION DELAY versus AMBIENT TEMPERATURE

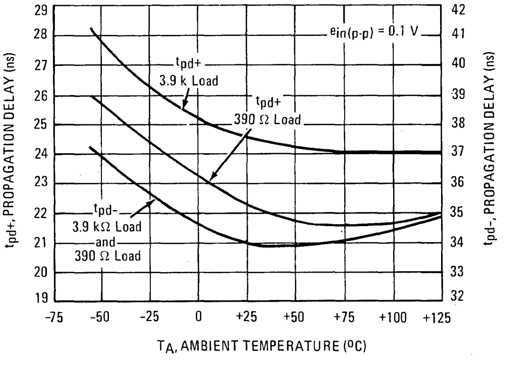
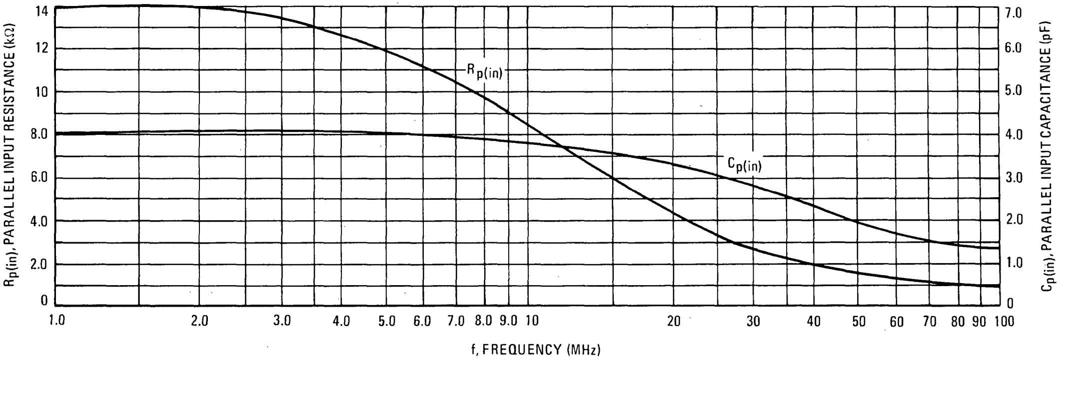


FIGURE 10 – PARALLEL INPUT IMPEDANCE versus FREQUENCY



6

APPLICATIONS INFORMATION

Line Driver/Receiver Family Characteristics

The Motorola line driver/receiver series provides interface circuits for driving digital data transmission lines e.g., coaxial cable or twisted pair. The digital data transmission is via a balanced differential mode. The line drivers and receivers are designed to provide high common-mode noise rejection, present high impedances to the transmission line and have low propagation times. A feature of the drivers is the capability to operate in a party-line mode whereby a number of drivers can be connected to a single line. This series provides drivers and receivers compatible with MRTL, MDTL, MTTL and MECL. The five circuits of the family are:

MC1580L	Dual Line Driver/Receiver
MC1581L	Dual MECL Receiver
MC1582L	Dual MDTL/MTTL Driver
MC1583L	Dual Receiver (Open Collector)
MC1584L	Dual Receiver (Active Pullup)

Figure 11 indicates line drivers and receivers recommended for interfacing with each of the various digital logic families.

These five circuits are extremely useful in numerous applications other than line drivers and receivers. The differential amplifier input of the receiver makes it useful in applications such as voltage comparators, waveform generators and high-input-impedance buffers. The drivers and receivers are useful as logic level translators.

FIGURE 11

Digital Logic Family	Driver	Receiver
MECL	MC1580L	MC1581L
MDTL	MC1582L	MC1583L MC1584L
MTTL	MC1582L	MC1583L MC1584L
MRTL	MC1580L MC1582L	MC1583L

The MC1583L in Figure 12 serves as a line receiver for a balanced differential transmission line. The driver inputs and receiver outputs of Figure 12 are compatible with MTTL and MDTL circuits. The MC1583L has an open collector output circuit which is designed to sink 20 mA. The open collector allows the user to interface with MRTL, MDTL, or MTTL by supplying the appropriate external resistor and power supply connection. A 9-volt BV_{CEO} rating on the open collector transistor allows the MC1583L to interface with MHTL also.

The MC1584L receiver can also be used to interface with MDTL and MTTL. The MC1584L contains an active pullup on the output device and hence eliminates the need for an external resistor for MTTL and MDTL compatible systems. The MC1584L has a 6-mA output sink current limitation.

The output stage of the MC1582L driver switches a current source between the two driver outputs in response to the input logic signals. Hence, a voltage differential that is a function of the line termination impedances is created on the twisted pair and at the input of the receiver. The receiver MC1583L is designed to reject +3.5/−3.5 Volts of common-mode voltage signals which may be present due to ground loop currents and noise coupled from nearby transmission lines.

While common-mode noise is the major concern in a twisted pair transmission line; a good data transmission system must offer some immunity from differential-mode voltages that may be present due to mismatches in termination impedances. The drivers and receivers of the MC1580 Series are designed with this requirement in mind. The exact amount of noise immunity depends on line impedances but the following example shows how differential-mode noise immunity is calculated for a given system. For a line with a characteristic impedance of Z_o, calculate the minimum differential input voltage from the equation.

$$\pm V_{in} = \frac{I_o(\text{min}) \times Z_o}{4}$$

For a 170-ohm line, $V_{in} = \frac{(6.9)\ (170)}{4} = 0.29$ Volts.

Since the MC1583L requires 50 mV maximum input differential to maintain the output state, the worst case differential-mode noise immunity is 0.26 V. (See Figure 13).

FIGURE 13

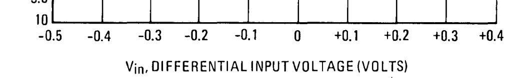
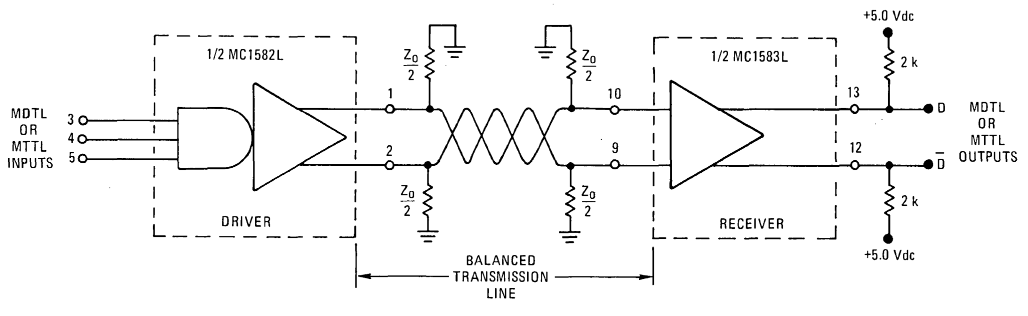


FIGURE 12 — MDTL, MTTL COMPATIBLE TRANSMISSION SYSTEM



APPLICATIONS INFORMATION (continued)

Hence the direct coupling of the driver and receiver to the line provides a built-in differential-mode noise immunity. The direct coupling also matches the line at all frequencies (often a problem with ac coupling lines). The recovery problem in ac coupling devices at high-signal repetition rates is also eliminated.

High input impedance of the MC1583L and high output impedances of the MC1582L minimize impedance discontinuities on the transmission line and allow many drivers and receivers to be connected to the line.

Using MC1580L as a driver and MC1583L as the receiver in a MRTL compatible transmission system is shown in Figure 14.

Use of the MC1583L in a bi-directional MDTL or MTTL compatible transmission system is shown in Figure 15. The MC1582L drivers of Figure 15 are connected so that the current sources from both drivers pull current from the same wire of the twisted pair when both drivers are transmitting logic "0" signals. The external current source, I_S, supplies the current required by one driver. The current for the other driver is drawn from the termination impedances creating a voltage differential across the line. When either driver transmits a logic "1", a voltage difference of the opposite polarity is created across the line. For a system with two drivers the current source (I_S) can be supplied by a 600-ohm resistor connected to +5.0 Volts. If additional drivers are connected to the line, a matching current source must be connected for each added driver. The current sources are connected to the line so that when all drivers are transmitting logic "0"s, the difference in current drawn from the terminating resistors of the two wires in the twisted pair is equal to one current source (8.6 mA). The current sources should also be connected so that when any driver transmits a logic "1" a current difference of the opposite polarity exists. The matching current source should be the companion circuit on the various driver chips. The difference in amplitude of the current sources on a single chip is specified to allow the system designer to calculate the maximum current source mismatch, ΔI_{OL}, and hence the maximum number of drivers that can be connected to a given transmission line.

FIGURE 14 – MRTL COMPATIBLE TRANSMISSION SYSTEM

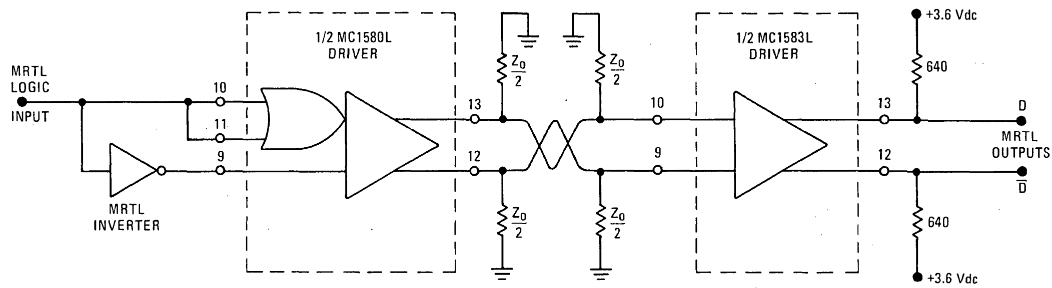
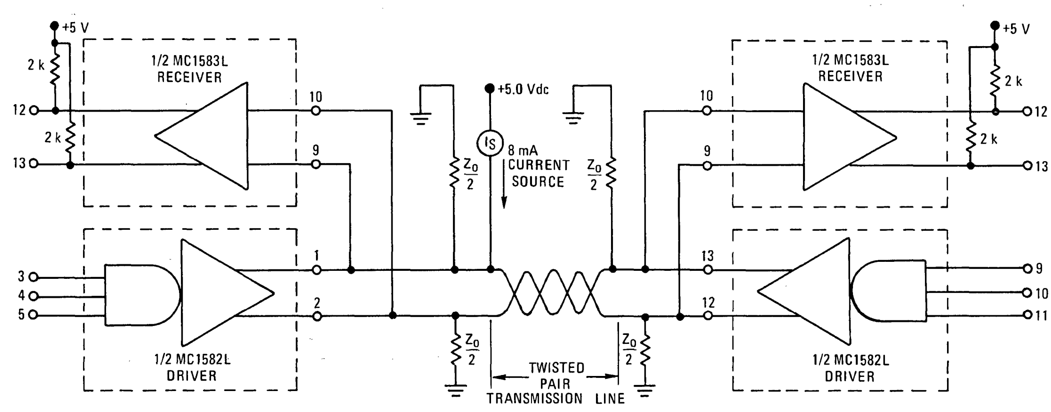


FIGURE 15 – BI-DIRECTIONAL TRANSMISSION



APPLICATIONS INFORMATION (continued)

The MC1583L has many other uses in a digital system. The high input impedance suggests its use as a buffer for delay lines and in waveform generation circuits. Figure 16 shows the MC1583L used as a differential comparator in a double-ended limit detector. When the input signal amplitude is between the two reference voltages, the output signal will be a logic "1"; otherwise a logic "0" output is obtained. The voltage transition region is typically 8 to 12 mV. External component R1 establishes an MDTL compatible output signal.

VOLTAGE TRANSLATOR

Translation of voltage levels from MECL (best suited for the high-speed portion of a digital system) to MHTL (tailored for the noisy output portion of the system) is often required. The MC1583L performs this function as indicated in Figure 17.

FIGURE 16 – DOUBLE-ENDED LIMIT DETECTOR

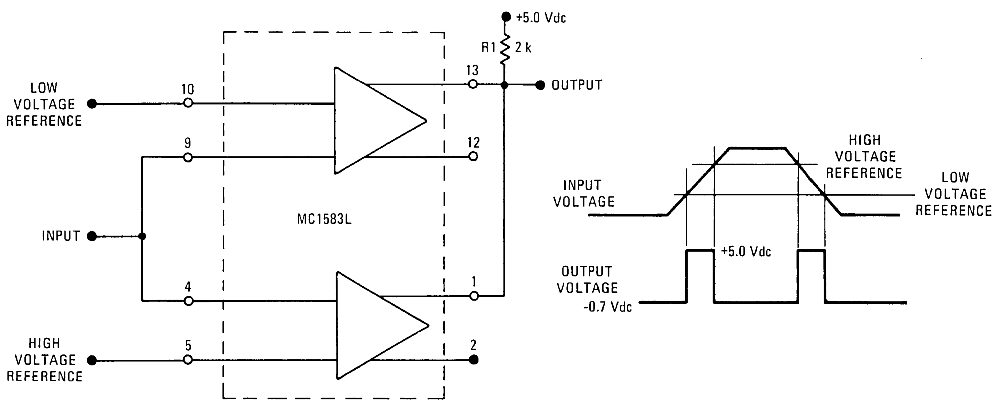
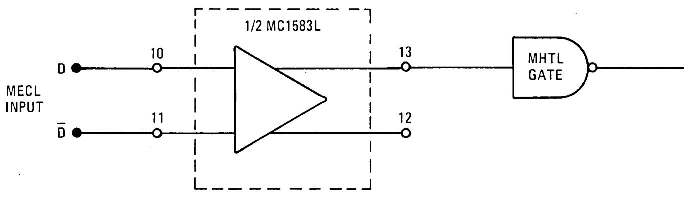


FIGURE 17 – MECL TO MHTL VOLTAGE LEVEL TRANSLATOR



MC1584L

MONOLITHIC DUAL MDTL/MTTL RECEIVER

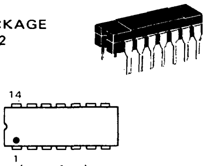
. . . designed with an active pull-up output that switches in response to a differential input voltage. This silicon device is compatible with the MDTL and MTTL digital logic families. Excellent common-mode input voltage range makes the device ideal for receiving digital information in a noisy environment. The "totem-pole" output (active pullup configuration) affords satisfactory response coupled with power savings for operation with a small number of unit loads. Typical applications include line sharing, voltage comparator, and logic level translation.

- High Input Impedance – 7.0 k ohms @ 10 MHz typ
- Low Propagation Delay Time – 37 ns max
- Wide Common–Mode Input Voltage Range ±3.5 Volts min
- Device Compatibility with other Members of the Line Driver/ Receiver Series

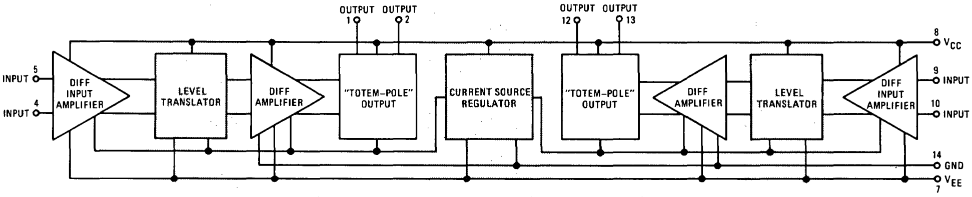
DUAL MDTL/MTTL RECEIVER (ACTIVE PULLUP) INTEGRATED CIRCUIT

EPITAXIAL PASSIVATED

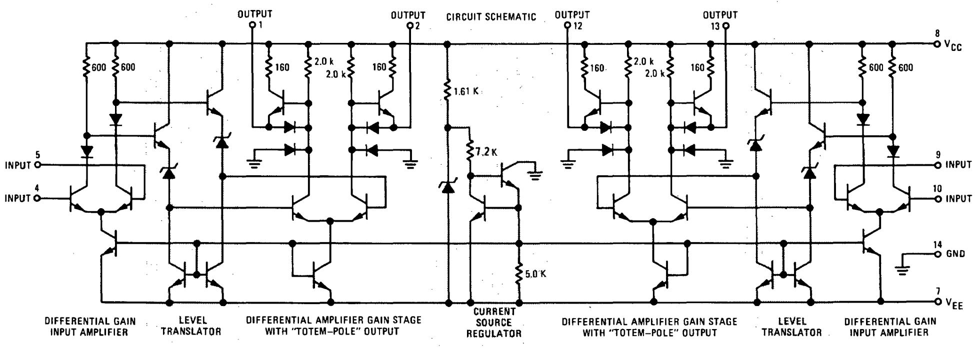
CERAMIC PACKAGE
CASE 632
TO-116



BLOCK DIAGRAM



CIRCUIT SCHEMATIC



See Packaging Information Section for outline dimensions.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+7.0 −7.0	Vdc
Differential–Mode Input Signal Voltage	V_{in}	±7.0	Volts
Common–Mode Input Signal Voltage	CMV_{in}	±10	Volts
Power Dissipation (Package Limitation) Ceramic Dual In-Line Package Derate above T_A = +25°C	P_D $1/\theta_{JA}$	 575 3.85	 mW mW/°C
Operating Temperature Range	T_A	−55 to +125	°C
Storage Temperature Range	T_{stg}	−65 to +175	°C

ELECTRICAL CHARACTERISTICS (Each Receiver, V_{EE} = +5.0 V, V_{CC} = −5.0 V, T_A = +25°C unless otherwise noted)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Operating Supply Currents	1	I_{CC} I_{EE}	– –	11.5 25	15 31	mA
Input Leakage Current	1	I_R	–	0.009	0.1	µA
Input Current T_A = −55°C T_A = +25°C T_A = +125°C	1	I_{in}	 – – –	 0.024 0.016 0.011	 0.1 0.1 0.1	mA
Output Voltage High (I_{OH} = −0.7 mA) T_A = −55°C T_A = +25°C T_A = +125°C	1	V_{OH}	 2.4 2.4 2.4	 4.0 4.0 4.0	 – – –	Volts
Output Voltage Low (I_{OL} = 4.0 mA) T_A = −55°C to +125°C	1	V_{OL}	 –	 100	 400	mV
Output Short–Circuit Current	1	I_{SC}	–	30	40	mA
Input Voltage Transition Width* T_A = −55°C T_A = +25°C T_A = +125°C		V_{TR}	 – – –	 20 25 30	 60 60 60	mV
Switching Times Propagation Delay Time Rise Time Fall Time	2	 $t_{pd}+$ $t_{pd}-$ t_r t_f	 – – – –	 32 28 14 12	 37 33 – –	 ns
Parallel Input Impedance (f = 5.0 MHz) Capacitance Resistance		 $C_{p(in)}$ $R_{p(in)}$	 – –	 5.0 11	 – –	 pF k ohms
Common–Mode Input Voltage Range T_A = −55 to +125°C	3	$CMVR_{in}$	+3.5 -3.5	+4.3 −4.2	– –	Volts
Power Supply Operating Range		V_{CC} V_{EE}	+4.75 -4.75	+5.0 −5.0	+6.0 -6.0	Vdc
Power Dissipation		P_D	–	170	200	mW

Ground all unused input pins to assure correct device biasing.
*Measured from points of unity gain.

CHARACTERISTIC DEFINITIONS

FIGURE 1 – TERMINAL CURRENTS

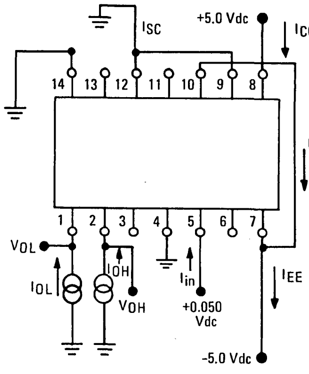


FIGURE 2 – TRANSIENT RESPONSE

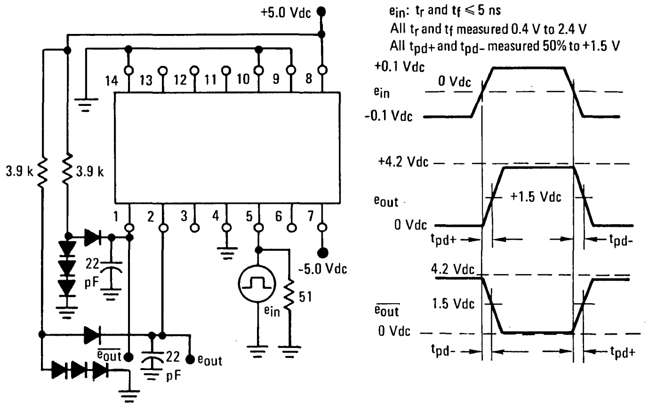
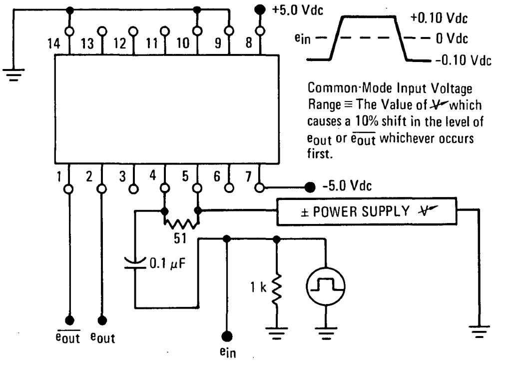


FIGURE 3 – COMMON-MODE INPUT VOLTAGE RANGE



TYPICAL CHARACTERISTICS

(V_{EE} = +5.0 Vdc, V_{CC} = -5.0 Vdc, T_A = +25°C unless otherwise noted)

FIGURE 4 – OUTPUT VOLTAGE HIGH versus SUPPLY OPERATING VOLTAGE AND TEMPERATURE

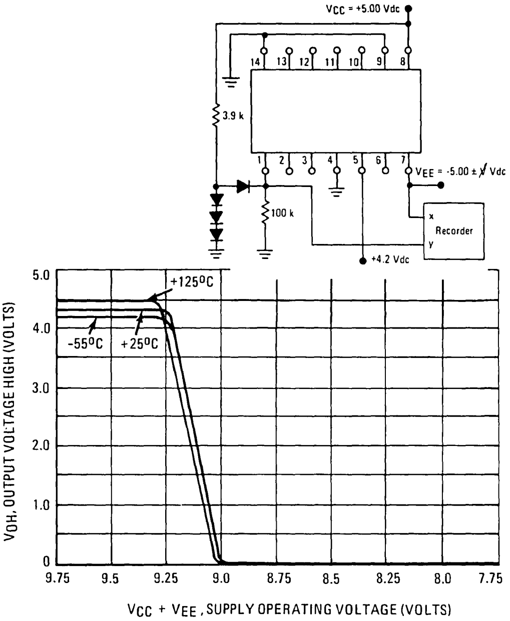


FIGURE 5 – OUTPUT VOLTAGE versus DIFFERENTIAL INPUT VOLTAGE AND TEMPERATURE

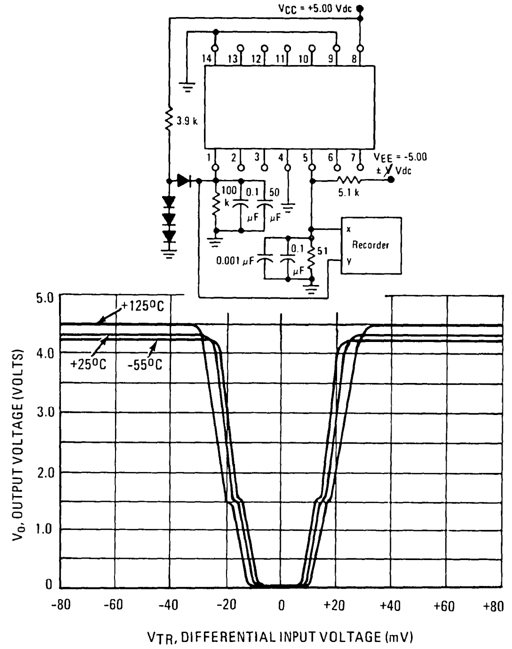


FIGURE 6 – OUTPUT VOLTAGE versus DIFFERENTIAL INPUT VOLTAGE AND VARIOUS LOADS

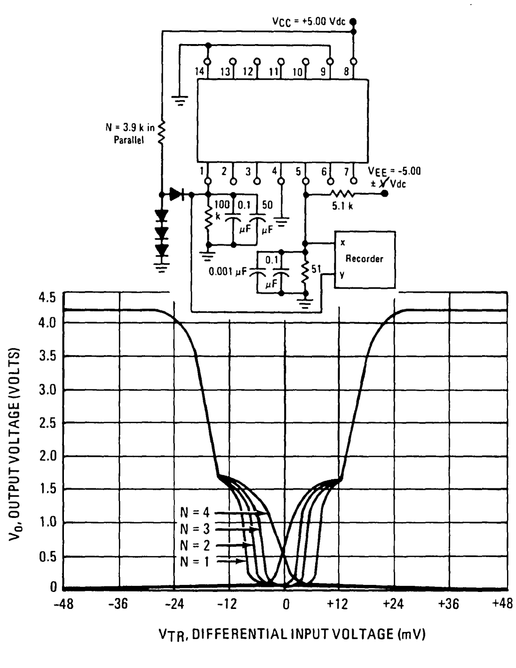
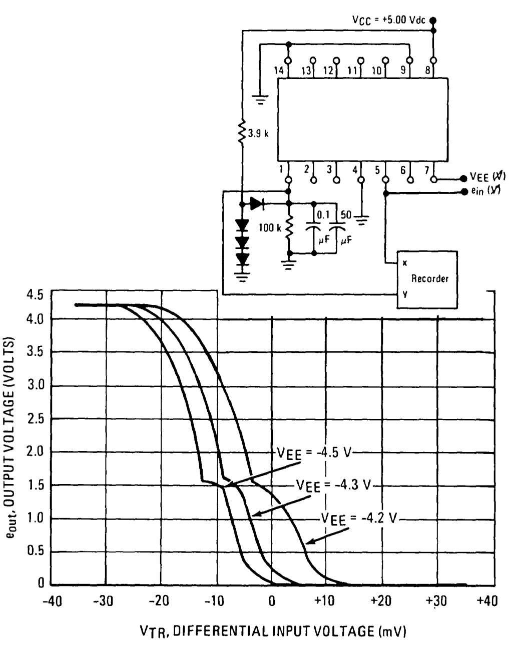


FIGURE 7 – OUTPUT VOLTAGE versus DIFFERENTIAL INPUT VOLTAGE AND VARIATIONS IN NEGATIVE SUPPLY



TYPICAL CHARACTERISTICS (continued)

FIGURE 8 – PROPAGATION DELAY versus DIFFERENTIAL INPUT VOLTAGE

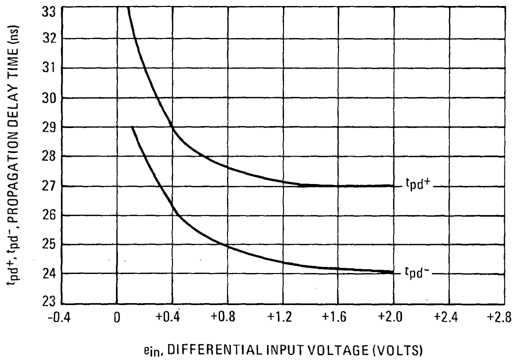


FIGURE 9 – PROPAGATION DELAY versus AMBIENT TEMPERATURE

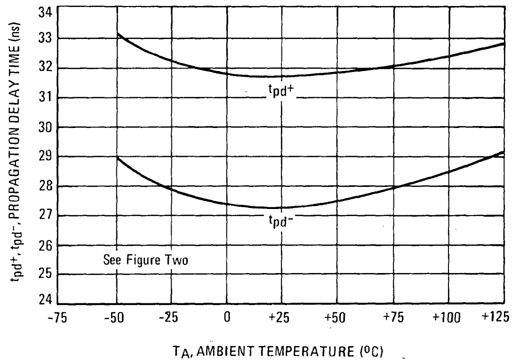
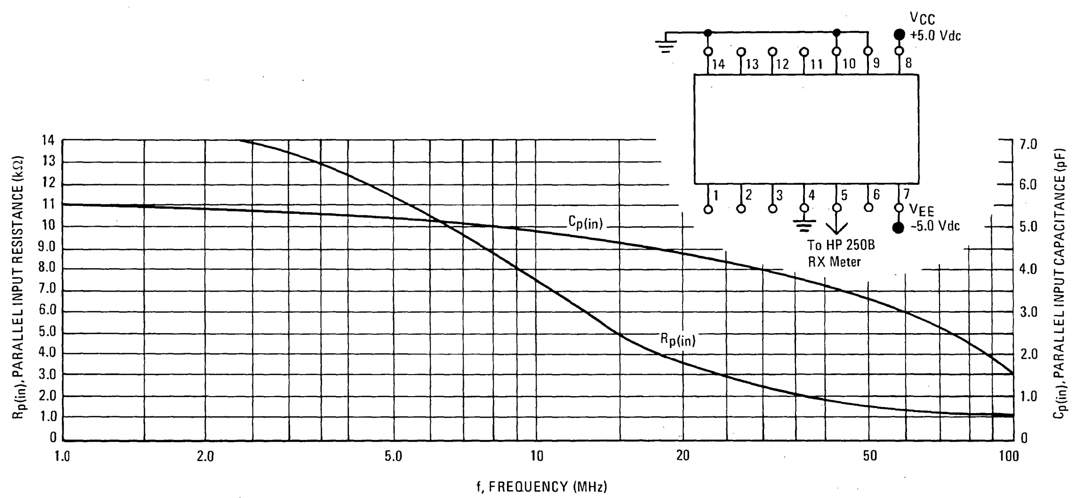


FIGURE 10 – PARALLEL INPUT IMPEDANCE versus FREQUENCY



APPLICATIONS INFORMATION

Line Driver/Receiver Family Characteristics

The Motorola line driver/receiver series provides interface circuits for driving digital data transmission lines, e.g., coaxial cable or twisted pair. The digital data transmission is via a balanced differential mode. The line drivers and receivers are designed to provide high common-mode noise rejection, present high impedances to the transmission line and have low propagation times. A feature of the drivers is the capability to operate in a party-line mode whereby a number of drivers can be connected to a single line. This series provides drivers and receivers compatible with MRTL, MDTL, MTTL and MECL. The five circuits of the family are:

MC1580L	Dual Line Driver/Receiver
MC1581L	Dual MECL Receiver
MC1582L	Dual MDTL/MTTL Driver
MC1583L	Dual Receiver (Open Collector)
MC1584L	Dual Receiver (Active Pullup)

Figure 11 indicates the line drivers and receivers recommended for interfacing with each of the various digital logic families.

These five circuits are extremely useful in numerous applications other than line drivers and receivers. The differential amplifier input of the receiver makes it useful in applications such as voltage comparators, waveform generators and high-input-impedance buffers. The drivers and receivers are useful as logic level translators.

FIGURE 11

Digital Logic Family	Driver	Receiver
MECL	MC1580L	MC1581L
MDTL	MC1582L	MC1583L MC1584L
MTTL	MC1582L	MC1583L MC1584L
MRTL	MC1580L MC1582L	MC1583L

The MC1584L in Figure 12 serves as the line receiver in a balanced differential transmission line. The outputs of the receiver and the inputs to the driver are compatible with MTTL and MDTL circuits. The MC1584L contains an active pullup circuit in the output stage. The MC1583L receiver can also be used for MTTL or MDTL systems. The open collector outputs of the MC1583L require external pullup resistors but is designed to sink up to 20 mA.

While common-mode noise is the major concern in a twisted pair transmission line; a good data transmission system must offer some immunity from differential-mode voltages that may be present due to mismatches in termination impedances. The drivers and receivers of the MC1580 Series are designed with this requirement in mind. The exact amount of noise immunity depends on line impedances but the following example shows how differential-mode noise immunity is calculated for a given system. For a line with a characteristic impedance of Z_0, calculate the minimum differential input voltage from the equation.

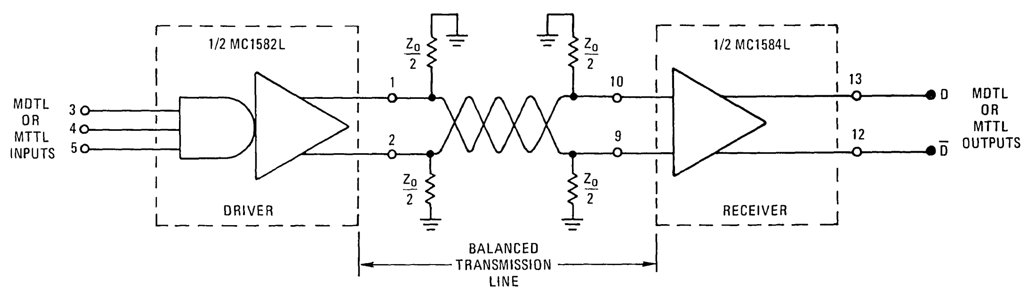
$$\pm V_{in} = \frac{I_o(\text{min}) \times Z_o}{4}$$

For a 170-ohm line, $V_{in} = \frac{(6.9)\ (170)}{4} = 0.29$ Volts.

Since the MC1584L requires a 50 mV maximum input differential to maintain the output state, the worst case differential-mode noise immunity is 0.26 V, (See Figure 13).

High input impedance of the MC1584L and high output impedance of the MC1582L minimize impedance discontinuities on the transmission line and allow many drivers and receivers to be connected to the line.

FIGURE 12 – MDTL, MTTL COMPATIBLE TRANSMISSION SYSTEM



APPLICATIONS INFORMATION (continued)

Use of the MC1584L in a bi-directional MDTL or MTTL compatible transmission system is shown in Figure 14. The drivers of Figure 14 are connected so that the current sources from both drivers pull current from the same wire of the twisted pair when both drivers are transmitting logic "0" signals. The external current source, I_S, supplies the current required by one driver. The current for the other driver is drawn from the termination impedances creating a voltage differential across the line. When either driver transmits a logic "1", a voltage difference of the opposite polarity is created across the line. For a system with two drivers the current source (I_S) can be supplied by a 600-ohm resistor connected to +5.0 Volts. If additional drivers are connected to the line, a matching current source must be connected for each added driver. The current sources are connected to the line so that when all drivers are transmitting logic "0"s, the difference in current drawn from the terminating resistors of the two wires in the twisted pair is equal to one current source (8.6 mA). The current sources should also be connected so that when any driver transmits a logic "1" a current difference of the opposite polarity exists. The matching current source should be the companion circuit on the various driver chips. The difference in amplitude of the two current sources on a single chip is specified to allow the system designer to calculate the maximum current source mismatch, ΔI_{OL}, and hence the maximum number of drivers that can be connected to a given transmission line.

The MC1584L has many other uses in a digital system. The high input impedance suggests its use as a buffer for delay lines and in waveform generation circuits.

FIGURE 13

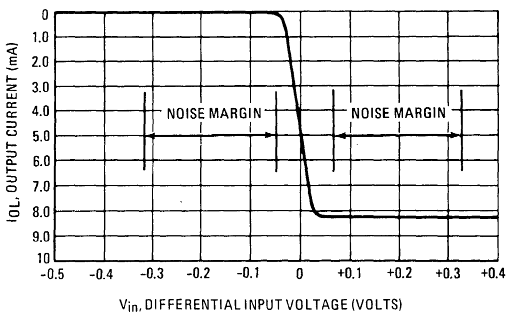
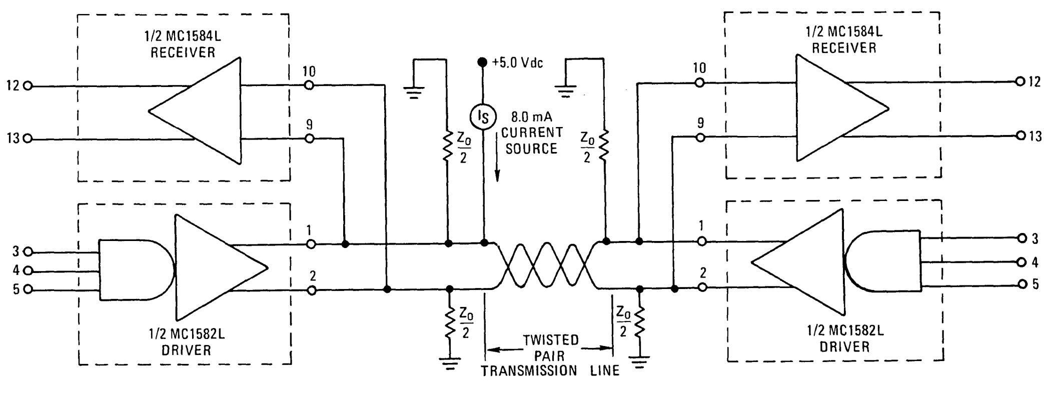


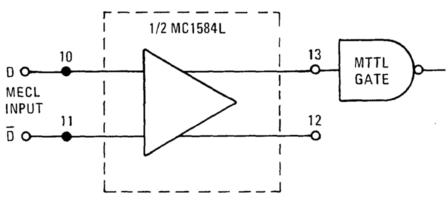
FIGURE 14 – BI-DIRECTIONAL TRANSMISSION SYSTEM



Voltage Translator

Translation of voltage levels from MECL (often used for the high-speed portion of a digital system) to MTTL (used in other slower portions of the system) is often required. The MC1584L can perform this function as indicated in Figure 15. The complements of the MECL input must be present unless a MECL bias source is available.

FIGURE 15 – MECL-TO-MTTL LEVEL TRANSLATOR



MONOLITHIC RF/IF/AUDIO AMPLIFIER

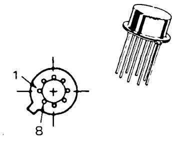
. . . an integrated circuit featuring wide-range AGC for use in RF/IF amplifiers and audio amplifiers over the temperature range, -55 to +125°C. (See application note AN 513 for design details.)

- High Power Gain – 50 dB typ at 10 MHz
  45 dB typ at 60 MHz
  35 dB typ at 100 MHz
- Wide-Range AGC – 60 dB min, dc to 60 MHz
- Low Reverse Transfer Admittance – <10 μmhos typ at 60 MHz
- 6.0 to 15-Volt Operation, Single-Polarity Power Supply

WIDEBAND AMPLIFIER WITH AGC

SILICON EPITAXIAL PASSIVATED

METAL PACKAGE
CASE 601
TO-99



(bottom view)

FIGURE 1 – UNNEUTRALIZED POWER GAIN versus FREQUENCY (Tuned Amplifier, see Figure 16)

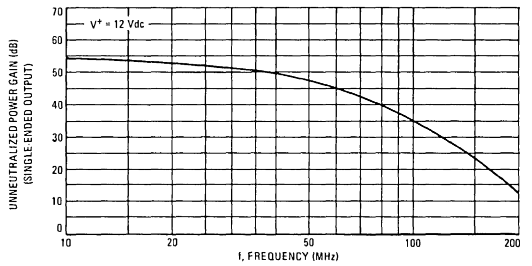
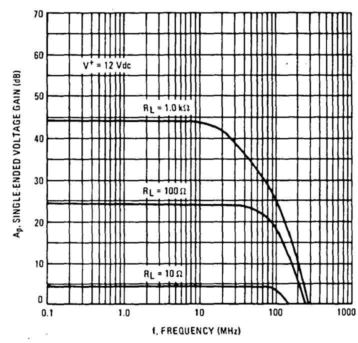
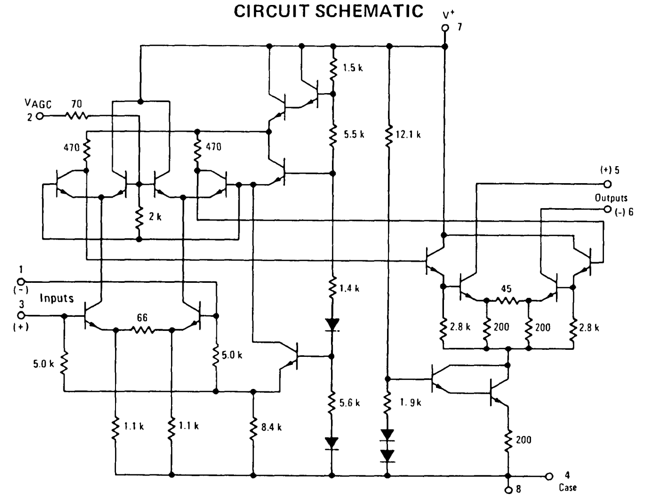


FIGURE 2 – VOLTAGE GAIN versus FREQUENCY (Untuned Amplifier, see Figure 17)

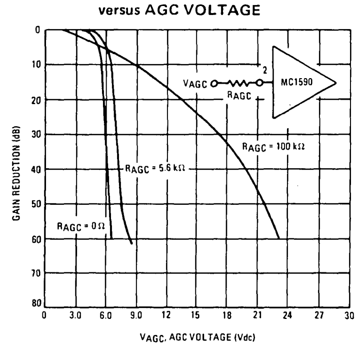


CIRCUIT SCHEMATIC



Pins 4 and 8 should both be connected to circuit ground.

FIGURE 3 – TYPICAL GAIN REDUCTION versus AGC VOLTAGE



See Packaging Information Section for outline dimensions.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+	+18	Vdc
Output Supply	V_5, V_6	+18	Vdc
AGC Supply	V_{AGC}	V^+	Vdc
Differential Input Voltage	V_{in}	5.0	Vdc
Power Dissipation (Package Limitation) Derate above T_A = +25°C	P_D	680 4.6	mW mW/°C
Operating Temperature Range	T_A	-55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V^+ = +12 Vdc, f = 60 MHz, BW = 1.0 MHz, T_A = +25°C unless otherwise noted, see Figure 16 for test circuit.)

Characteristic	Symbol	Min	Typ	Max	Unit
AGC Range, V_2 = 5.0 Vdc to 7.0 Vdc		60	68	–	dB
Single-Ended Power Gain	A_p	40	45	–	dB
Noise Figure (R_s = 50 ohms)	N_f	–	6.0	–	dB
Output Voltage Swing (Pin 5)	V_5				V_{p-p}
Differential Output – 0 dB AGC		–	14	–	
-30 dB AGC		–	6.0	–	
Single-Ended Output – 0 dB AGC		–	7.0	–	
-30 dB AGC		–	3.0	–	
Output Stage Current (Pins 5 and 6)	$I_5 + I_6$	–	5.6	–	mA
Total Supply Power Current (V_{out} = 0)	I_D	–	14	17	mAdc
Power Dissipation (V_{in} = 0)	P_D	–	168	200	mW

ADMITTANCE PARAMETERS (V^+ = 12 Vdc, T_A = +25°C)

Parameter	Symbol	Typ f = 30 MHz	Typ f = 60 MHz	Unit
Single-Ended Input Admittance	g_{11} b_{11}	0.4 1.2	0.75 3.4	mmhos
Single-Ended Output Admittance	g_{22} b_{22}	0.05 0.50	0.1 1.0	mmho
Forward Transfer Admittance (Pin 1 to Pin 5)	$\|Y_{21}\|$ θ_{21}	150 -45	150 -105	mmhos degrees
Reverse Transfer Admittance*	g_{12} b_{12}	-0 -5.0	-0 -10	μmhos

*The value of Reverse Transfer Admittance includes the feedback admittance of the test circuit used in the measurement. The total feedback capacitance (including test circuit) is 0.025 pF and is a more practical value for design calculations than the internal feedback of the device alone. (See Figure 6)

SCATTERING PARAMETERS (V^+ = +12 Vdc, T_A = +25°C, Z_o = 50 Ω)

Parameter	Symbol	Typ f = 30 MHz	Typ f = 60 MHz	Unit
Input Reflection Coefficient	$\|S_{11}\|$ θ_{11}	0.95 -7.3	0.93 -16	– degrees
Output Reflection Coefficient	$\|S_{22}\|$ θ_{22}	0.99 -3.0	0.98 -5.5	– degrees
Forward Transmission Coefficient	$\|S_{21}\|$ θ_{21}	16.8 128	14.7 64.3	– degrees
Reverse Transmission Coefficient	S_{12} θ_{12}	0.00048 84.9	0.00092 79.2	– degrees

TYPICAL CHARACTERISTICS

(V^+ = 12 Vdc, T_A = +25°C unless otherwise noted)

FIGURE 4 – FIXED TUNED POWER GAIN versus TEMPERATURE (See test circuit, Figure 16)

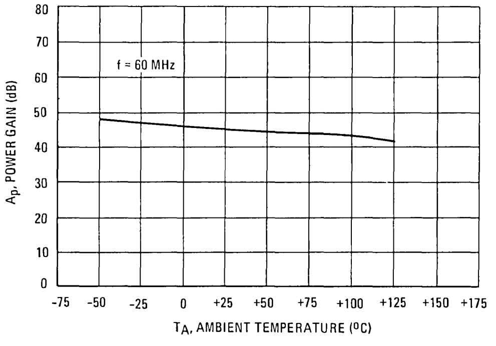


FIGURE 5 – POWER GAIN versus SUPPLY VOLTAGE (See test circuit, Figure 16)

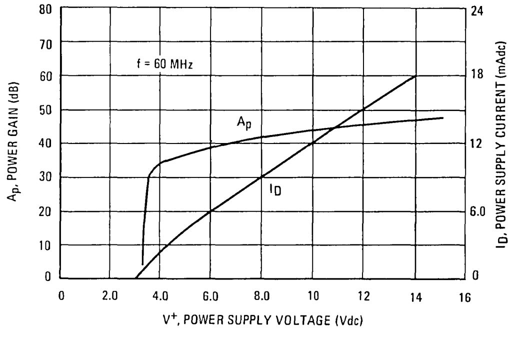


FIGURE 6 – REVERSE TRANSFER ADMITTANCE versus FREQUENCY (See Parameter Table, page 2 of MC1590 specification)

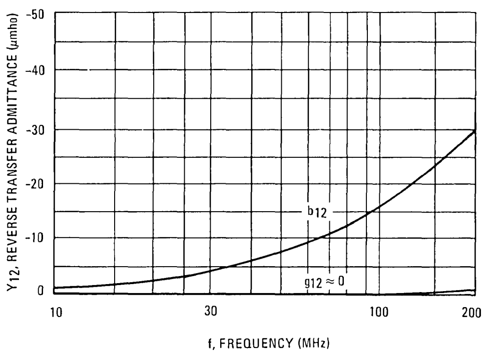


FIGURE 7 – NOISE FIGURE versus FREQUENCY

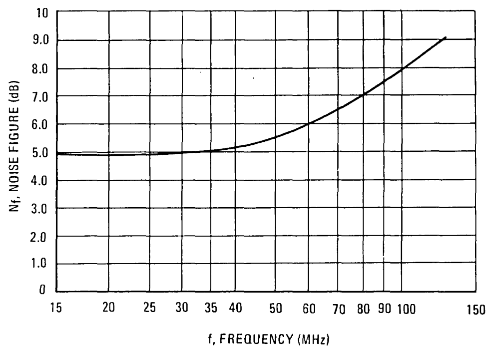


FIGURE 8 – SINGLE-ENDED OUTPUT ADMITTANCE

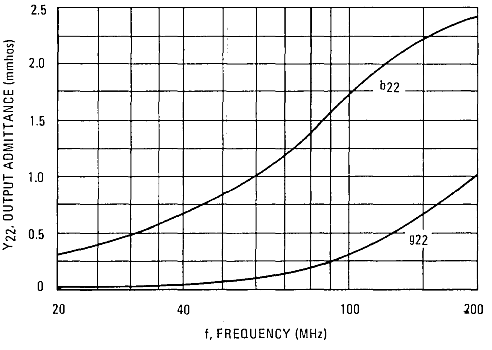
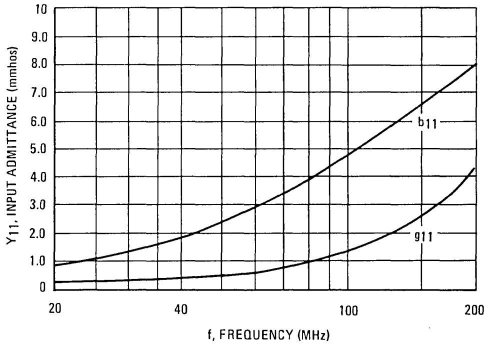


FIGURE 9 – SINGLE-ENDED INPUT ADMITTANCE



TYPICAL CHARACTERISTICS (continued)

FIGURE 10 – Y_{21}, FORWARD TRANSFER ADMITTANCE, RECTANGULAR FORM

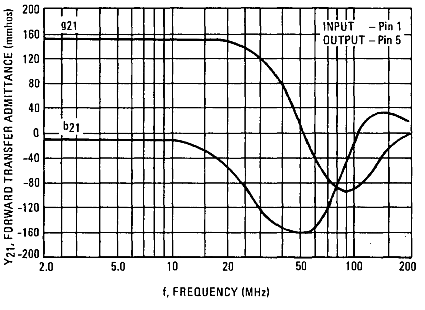


FIGURE 11 – Y_{21}, FORWARD TRANSFER ADMITTANCE, POLAR FORM

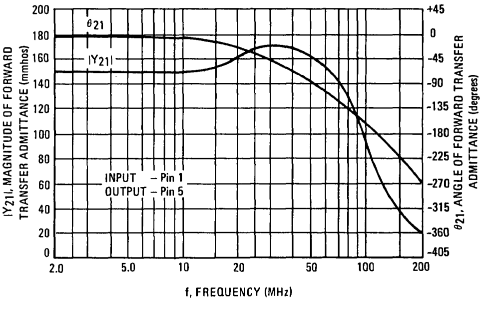


FIGURE 12 – S_{11} and S_{22}, INPUT AND OUTPUT REFLECTION COEFFICIENT

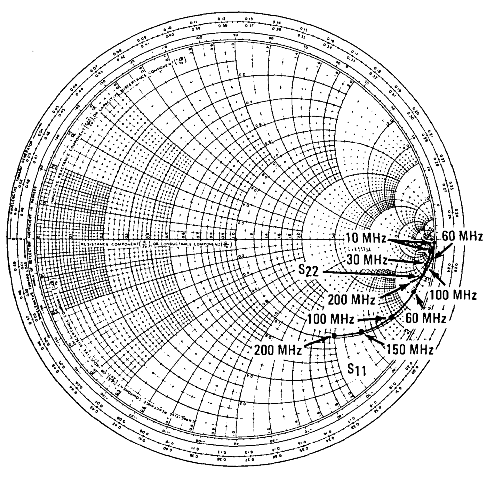
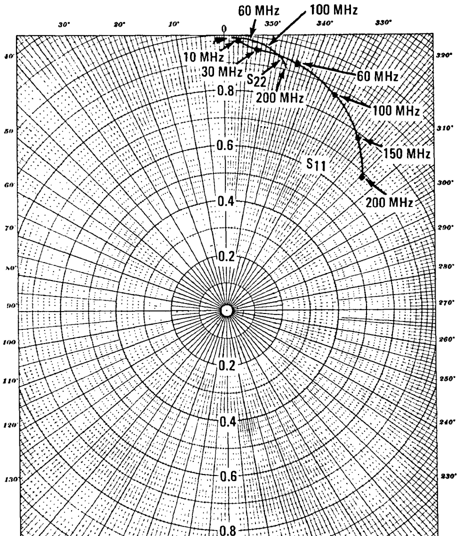


FIGURE 13 – S_{11}, and S_{22}, INPUT AND OUTPUT REFLECTION COEFFICIENT



TYPICAL CHARACTERISTICS (continued)

FIGURE 14 – S_{21}, FORWARD TRANSMISSION COEFFICIENT (GAIN)

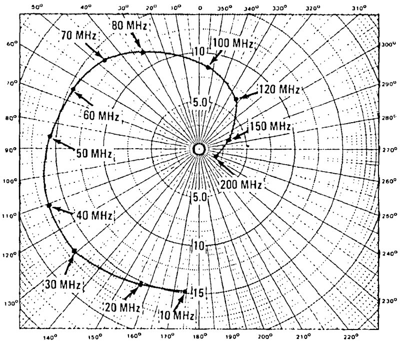
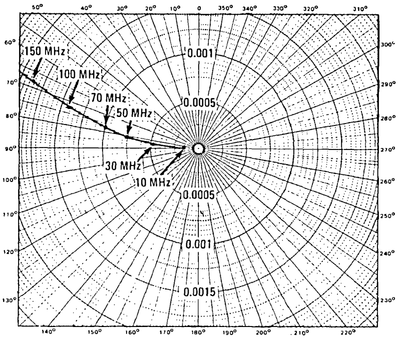
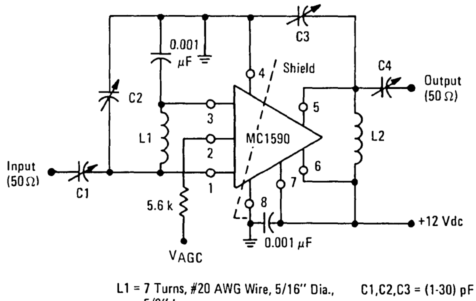


FIGURE 15 – S_{12}, REVERSE TRANSMISSION COEFFICIENT (FEEDBACK)



TYPICAL APPLICATIONS

FIGURE 16 – 60-MHz POWER GAIN TEST CIRCUIT



L1 = 7 Turns, #20 AWG Wire, 5/16" Dia., 5/8" Long
L2 = 6 Turns, #14 AWG Wire, 9/16" Dia., 3/4" Long

C1,C2,C3 = (1-30) pF
C4 = (1-10) pF

FIGURE 17 – VIDEO AMPLIFIER

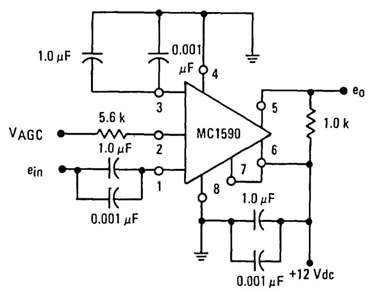
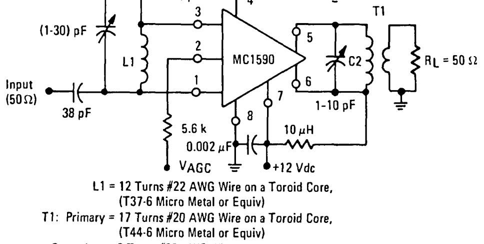
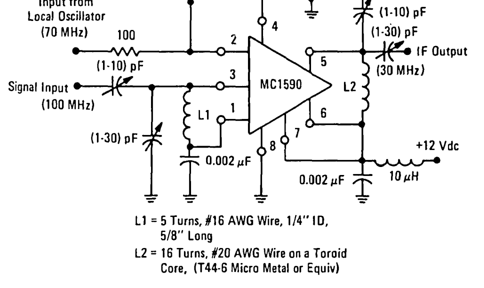


FIGURE 18 – 30-MHz AMPLIFIER
(Power Gain = 50 dB, BW ≈ 1.0 MHz)



L1 = 12 Turns #22 AWG Wire on a Toroid Core, (T37-6 Micro Metal or Equiv)
T1: Primary = 17 Turns #20 AWG Wire on a Toroid Core, (T44-6 Micro Metal or Equiv)
Secondary = 2 Turns #20 AWG Wire

FIGURE 19 – 100-MHz MIXER

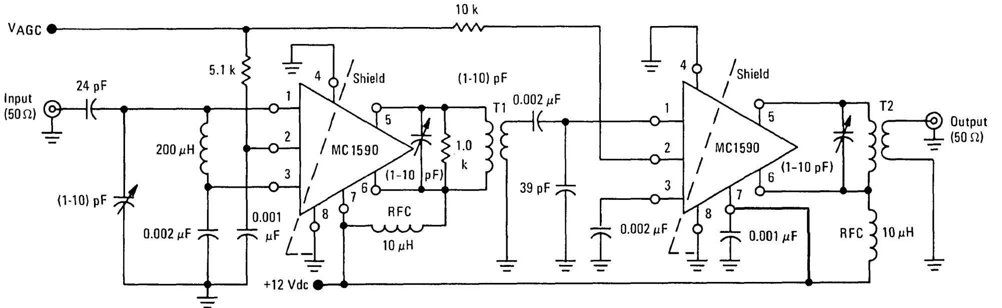


L1 = 5 Turns, #16 AWG Wire, 1/4" ID, 5/8" Long
L2 = 16 Turns, #20 AWG Wire on a Toroid Core, (T44-6 Micro Metal or Equiv)

6

TYPICAL APPLICATIONS (continued)

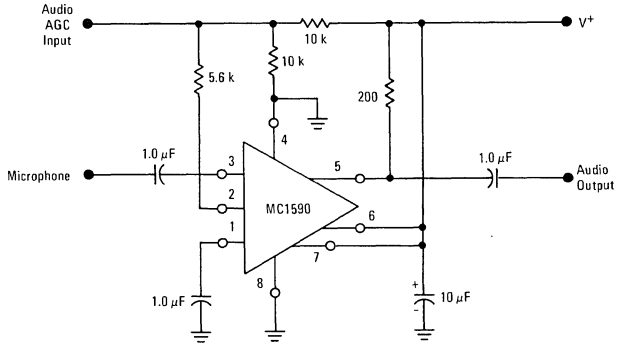
FIGURE 20 – TWO-STAGE 60 MHz IF AMPLIFIER (Power Gain ≈ 80 dB, BW ≈ 1.5 MHz)



T1: Primary Winding = 15 Turns, #22 AWG Wire, 1/4" ID Air Core
Secondary Winding = 4 Turns, #22 AWG Wire,
Coefficient of Coupling ≈ 1.0

T2: Primary Winding = 10 Turns, #22 AWG Wire, 1/4" ID Air Core
Secondary Winding = 2 Turns, #22 AWG Wire,
Coefficient of Coupling ≈ 1.0

FIGURE 21 – SPEECH COMPRESSOR



MC1594L
MC1494L

Specifications and Applications Information

MONOLITHIC FOUR-QUADRANT MULTIPLIER

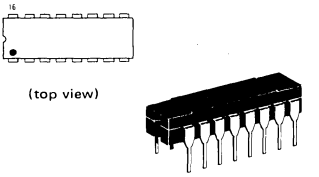
. . . designed for use where the output voltage is a linear product of two input voltages. Typical applications include: multiply, divide, square root, mean square, phase detector, frequency doubler, balanced modulator/demodulator, electronic gain control.

The MC1594/1494 is a variable transconductance multiplier with internal level-shift circuitry and voltage regulator. Scale factor, input offsets and output offset are completely adjustable with the use of four external potentiometers. Two complementary regulated voltages are provided to simplify offset adjustment and improve power-supply rejection.

- Operates With ±15 V Supplies
- Excellent Linearity – Maximum Error (X or Y): ± 0.5% (MC1594)
  ± 1.0% (MC1494)
- Wide Input Voltage Range – ±10 volts
- Adjustable Scale Factor, K (0.1 nominal)
- Single-Ended Output Referenced to Ground
- Simplified Offset Adjust Circuitry
- Frequency Response (3 dB Small-Signal) – 1.0 MHz
- Power Supply Sensitivity – 30 mV/V typical

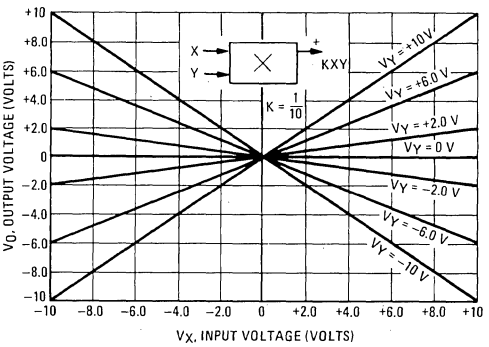
LINEAR FOUR-QUADRANT MULTIPLIER INTEGRATED CIRCUIT

MONOLITHIC SILICON EPITAXIAL PASSIVATED

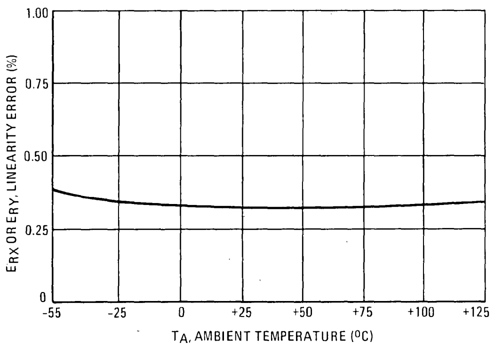


CERAMIC PACKAGE
CASE 620

FOUR-QUADRANT MULTIPLIER TRANSFER CHARACTERISTIC



TYPICAL LINEARITY ERROR versus TEMPERATURE



CONTENTS

See Packaging Information Section for outline dimensions.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+ V^-	+18 -18	Vdc
Differential Input Signal	$V_9 - V_6$ $V_{10} - V_{13}$	$\pm \|6 + I_1 R_Y\| < 30$ $\pm \|6 + I_1 R_X\| < 30$	Vdc
Common-Mode Input Voltage $V_{CMY} = V_9 = V_6$ $V_{CMX} = V_{10} = V_{13}$	 V_{CMY} V_{CMX}	 ±11.5 ±11.5	Vdc
Power Dissipation (Package Limitation) T_A = +25°C Derate above T_A = +25°C	 P_D $1/\theta_{JA}$	 750 5.0	 mW mW/°C
Operating Temperature Range MC1594 MC1494	T_A	 -55 to +125 0 to + 75	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V^+ = +15 V, V^- = -15 V, T_A = +25°C, R1 = 16 kΩ, R_X = 30 kΩ, R_Y = 62 kΩ, R_L = 47 kΩ, unless otherwise noted)

Characteristic	Fig.	Symbol	MC1594 Min	MC1594 Typ	MC1594 Max	MC1494 Min	MC1494 Typ	MC1494 Max	Unit
Linearity Output error in Percent of full scale $-10\ V < V_x < +10\ V$ ($V_y = \pm 10$ V) $-10\ V < V_y < +10\ V$ ($V_x = \pm 10$ V)	1	E_{RX} or E_{RY}							%
T_A = +25°C			–	± 0.3	± 0.5	–	± 0.5	± 1.0	
$T_A = T_{high}$ ①			–	–	± 0.8	–	–	± 1.3	
$T_A = T_{low}$ ②			–	–	± 0.8	–	–	± 1.3	
Input	2,3,4								
Voltage Range ($V_X = V_Y = V_{in}$)		V_{in}	±10	–	–	±10	–	–	V_{pk}
Resistance (X or Y Input)		R_{in}	–	300	–	–	300	–	MΩ
Offset Voltage (X Input) (Note 1)		$\|V_{iox}\|$	–	0.1	1.6	–	0.2	2.5	V
(Y Input) (Note 1)		$\|V_{ioy}\|$	–	0.4	1.6	–	0.8	2.5	
Bias Current (X or Y Input)		I_b	–	0.5	1.5	–	1.0	2.5	μA
Offset Current (X or Y Input)		$\|I_{io}\|$	–	28	150	–	50	400	nA
Output	3,4								
Voltage Swing Capability		V_o	±10	–	–	±10	–	–	V_{pk}
Impedance		R_o	–	850	–	–	850	–	kΩ
Offset Voltage (Note 1)		$\|V_{oo}\|$	–	0.8	1.6	–	1.2	2.5	V
Offset Current (Note 1)		$\|I_{oo}\|$	–	17	34	–	25	52	μA
Temperature Stability (Drift) $T_A = T_{high}$ to T_{low}									
Output Offset (X = 0, Y = 0) Voltage		$\|TCV_{oo}\|$	–	1.3	–	–	1.3	–	mV/°C
Current		$\|TCI_{oo}\|$	–	27	–	–	27	–	nA/°C
X Input Offset (Y = 0)		$\|TCV_{iox}\|$	–	0.3	–	–	0.3	–	mV/°C
Y Input Offset (X = 0)		$\|TCV_{ioy}\|$	–	1.5	–	–	1.5	–	
Scale Factor		$\|TCK\|$	–	0.07	–	–	0.07	–	%/°C
Total dc Accuracy Drift (X = 10, Y = 10)		$\|TCE\|$	–	0.09	–	–	0.09	–	
Dynamic Response	5								
Small Signal (3 dB) X		$BW_{3\,dB\,(X)}$	–	0.8	–	–	0.8	–	MHz
Y		$BW_{3\,dB\,(Y)}$	–	1.0	–	–	1.0	–	
Power Bandwidth (47 k)		P_{BW}	–	440	–	–	440	–	kHz
3° Relative Phase Shift		f_ϕ	–	240	–	–	240	–	
1% Absolute Error		f_θ	–	30	–	–	30	–	
Common Mode	6								
Input Swing (X or Y)		CMV	±10.5	–	–	±10.5	–	–	V_{pk}
Gain (X or Y)		A_{CM}	–	-65	–	–	-65	–	dB
Power Supply	7								
Current		I_d^+	–	6.0	9.0	–	6.0	12	mAdc
		I_d^-	–	6.5	9.0	–	6.5	12	
Quiescent Power Dissipation		P_d	–	185	260	–	185	350	mW
Sensitivity		S^+	–	13	50	–	13	100	mV/V
		S^-	–	30	100	–	30	200	
Regulated Offset Adjust Voltages	7								
Positive		V_R^+	+3.5	+4.3	+5.0	+3.5	+4.3	+5.0	Vdc
Negative		V_R^-	-3.5	-4.3	-5.0	-3.5	-4.3	-5.0	
Temperature Coefficient (V_R^+ or V_R^-)		TCV_R	–	0.03	–	–	0.03	–	mV/°C
Power Supply Sensitivity (V_R^+ or V_R^-)		S_R^+, S_R^-	–	0.6	–	–	0.6	–	mV/V

Note 1: Offsets can be adjusted to zero with external potentiometers.

① T_{high} = +125°C for MC1594, + 75°C for MC1494 ② T_{low} = - 55°C for MC1594, 0°C for MC1594

TEST CIRCUITS

FIGURE 1 – LINEARITY

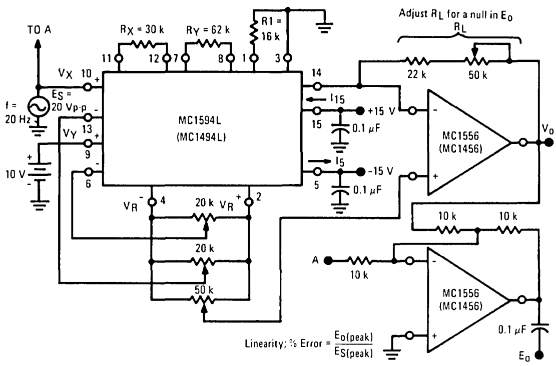
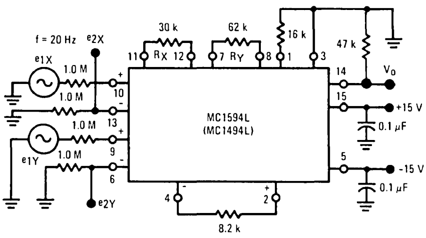


FIGURE 2 – INPUT RESISTANCE



$$R_{in}\,X = \left[\frac{e1X}{e2X} - 2\right] \text{ Megohm}$$

$$R_{in}\,Y = \left[\frac{e1Y}{e2Y} - 2\right] \text{ Megohm}$$

FIGURE 3 – OFFSET VOLTAGES, GAIN

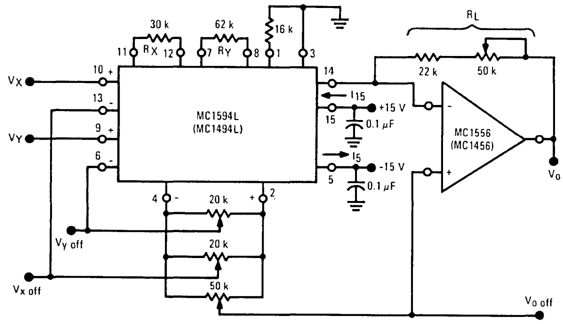


FIGURE 4 – INPUT BIAS CURRENT/INPUT OFFSET CURRENT, OUTPUT RESISTANCE

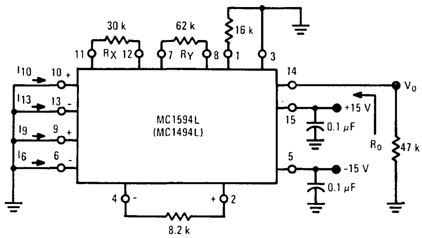


FIGURE 5 – FREQUENCY RESPONSE

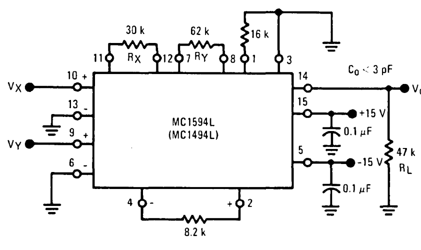


FIGURE 6 – COMMON-MODE

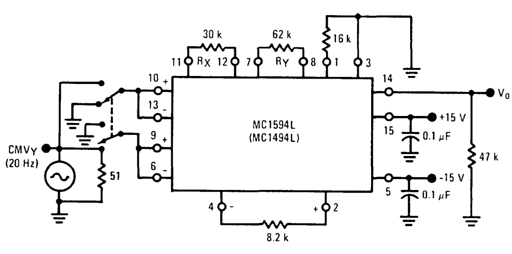


FIGURE 7 – POWER-SUPPLY SENSITIVITY

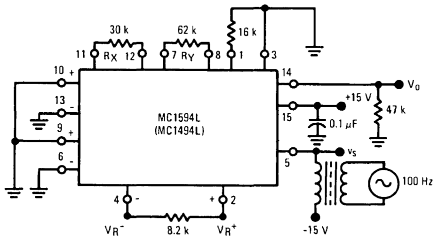
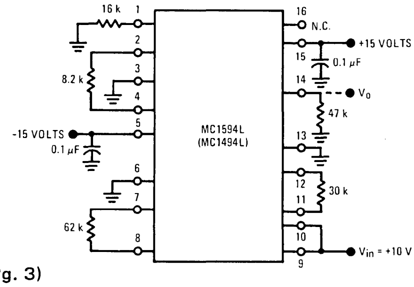


FIGURE 8 – BURN-IN



TYPICAL CHARACTERISTICS

(Unless otherwise noted, $V^+ = +15$ V, $V^- = -15$ V, R1 = 16 kΩ, R_X = 30 kΩ, R_Y = 62 kΩ, R_L = 47 kΩ, T_A = +25°C)

FIGURE 9 — FREQUENCY RESPONSE OF Y INPUT versus LOAD RESISTANCE

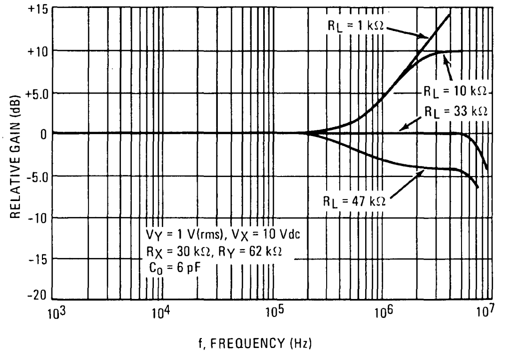


FIGURE 10 — FREQUENCY RESPONSE OF X INPUT versus LOAD RESISTANCE

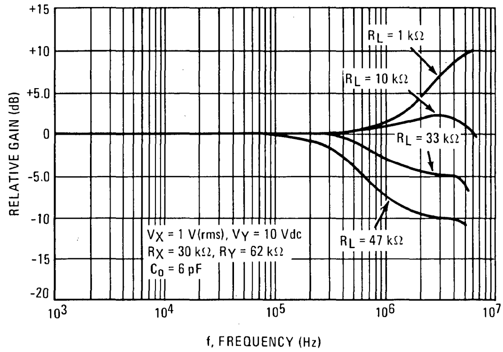


FIGURE 11 — LARGE SIGNAL VOLTAGE versus FREQUENCY

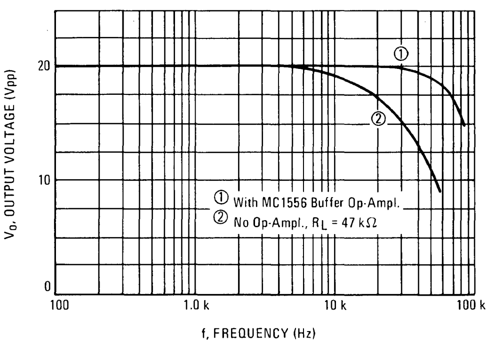


FIGURE 12 — LINEARITY versus R_X OR R_Y WITH K = 1/10

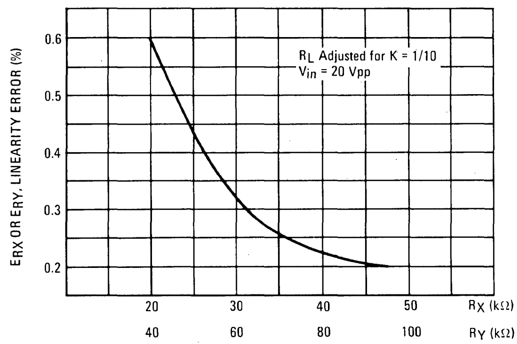


FIGURE 13 — LINEARITY versus R_X OR R_Y WITH K = 1

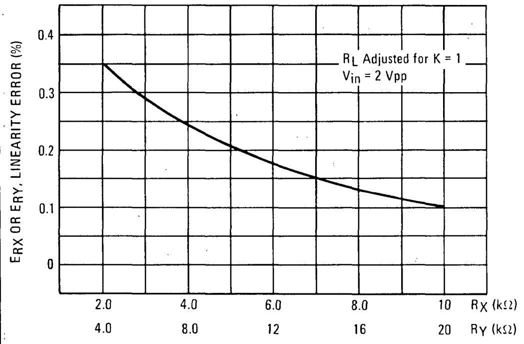
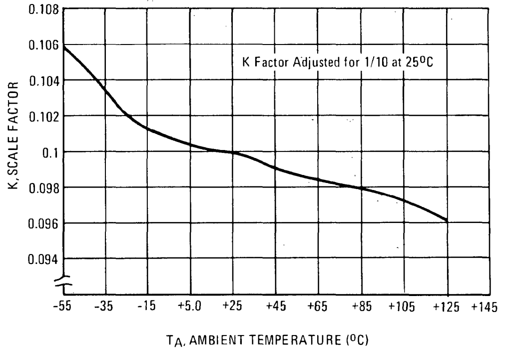


FIGURE 14 — SCALE FACTOR (K) versus TEMPERATURE



GENERAL INFORMATION

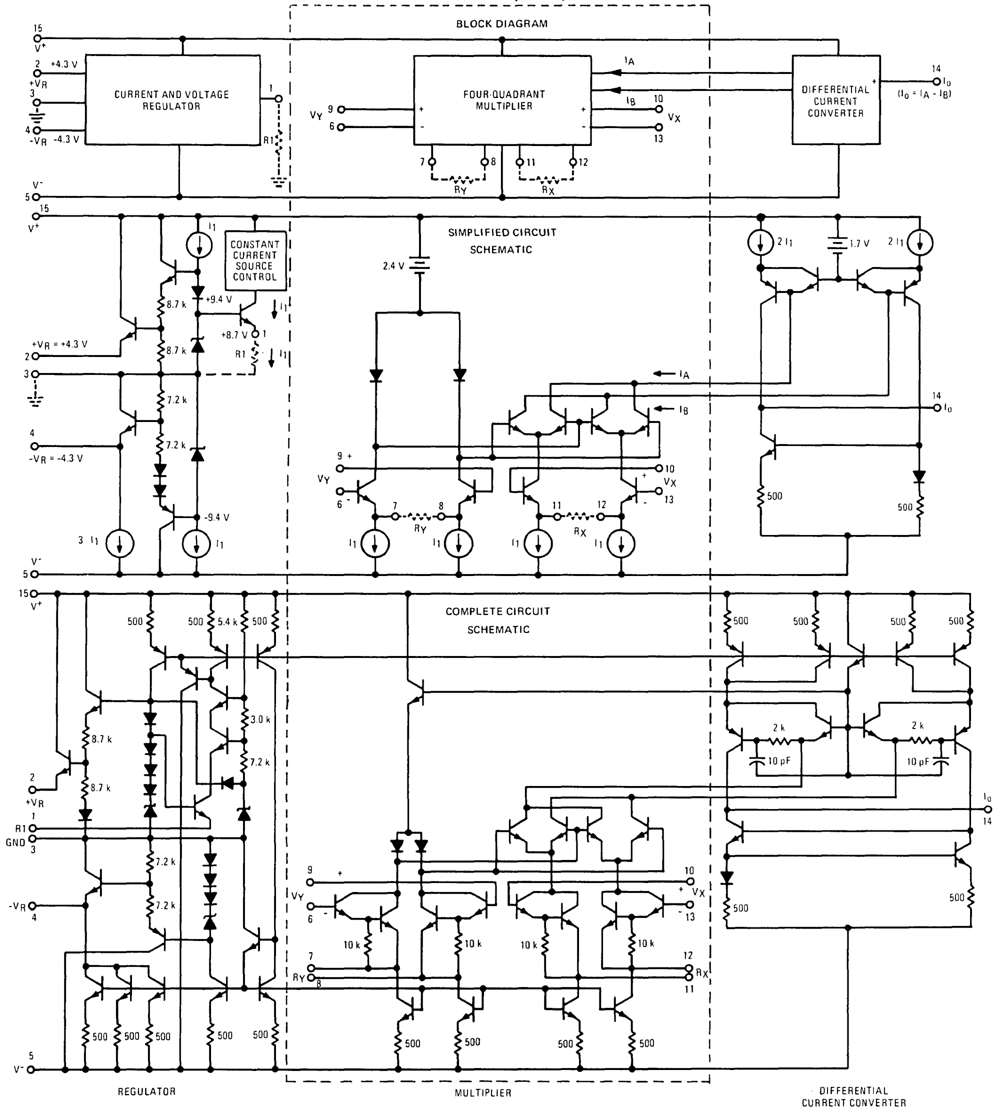
1. CIRCUIT DESCRIPTION

1.1 Introduction

The MC1594 is a monolithic, four-quadrant multiplier that operates on the principle of variable transconductance. It features a single-ended current output referenced to ground and provides two complementary regulated voltages for use with the offset adjust circuits to virtually eliminate sensitivity of the offset voltage nulls to changes in supply voltage.

As shown in Figure 15, the MC1594 consists of a multiplier proper and associated peripheral circuitry to provide these features.

FIGURE 15
(Recommended External Circuitry is Depicted With Dotted Lines)



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1.2 Regulator (Figure 15)

The regulator biases the entire MC1594 circuit making it essentially independent of supply variation. It also provides two convenient regulated supply voltages which can be used in the offset adjust circuitry. The regulated output voltage at pin 2 is approximately +4.3 V while the regulated voltage at pin 4 is approximately −4.3 V. For optimum temperature stability of these regulated voltages, it is recommended that $|I_2| = |I_4| = 1.0$ mA (equivalent load of 8.6 kΩ). As will be shown later, there will normally be two 20 k-ohm potentiometers and one 50 k-ohm potentiometer connected between pins 2 and 4.

The regulator also establishes a constant current reference that controls all of the constant current sources in the MC1594. Note that all current sources are related to current I_1 which is determined by R1. For best temperature performance, R1 should be 16 kΩ so that $I_1 \approx 0.5$ mA for all applications.

1.3 Multiplier (Figure 15)

The multiplier section of the MC1594 (center section of Figure 15) is nearly identical to the MC1595 and is discussed in detail in Application Note AN-489, "Analysis and Basic Operation of the MC1595". The result of this analysis is that the differential output current of the multiplier is given by:

$$I_A - I_B = \Delta I \approx \frac{2 V_X V_Y}{R_X R_Y I_1}$$

Therefore, the output is proportional to the product of the two input voltages.

1.4 Differential Current Converter (Figure 15)

This portion of the circuitry converts the differential output current $(I_A - I_B)$ of the multiplier to a single-ended output current (I_o):

$$I_o = I_A - I_B$$

or

$$I_o = \frac{2 V_X V_Y}{R_X R_Y I_1}$$

The output current can be easily converted to an output voltage by placing a load resistor R_L from the output (pin 14) to ground (Figure 17) or by using an op-ampl. as a current-to-voltage converter (Figure 16). The result in both circuits is that the output voltage is given by:

$$V_o = \frac{2 R_L V_X V_Y}{R_X R_Y I_1} = K V_X V_Y$$

$$\text{where K (scale factor)} = \frac{2 R_L}{R_X R_Y I_1}$$

2. DC OPERATION

2.1 Selection of External Components

For low frequency operation the circuit of Figure 16 is recommended. For this circuit, $R_X = 30$ kΩ, $R_Y = 62$ kΩ, R1 = 16 kΩ and hence $I_1 \approx 0.5$ mA. Therefore, to set the scale factor, K, equal to 1/10, the value of R_L can be calculated to be:

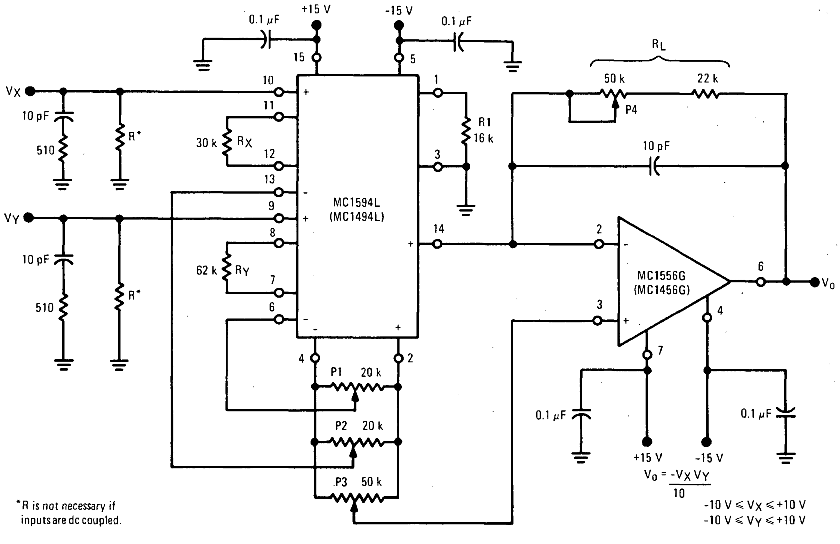
$$K = \frac{1}{10} = \frac{2 R_L}{R_X R_Y I_1}$$

$$\text{or} \quad R_L = \frac{R_X R_Y I_1}{(2)(10)} = \frac{(30\text{ k})(62\text{ k})(0.5\text{ mA})}{20}$$

$$R_L = 46.5\text{ k}$$

Thus, a reasonable accuracy in scale factor can be achieved by making R_L a fixed 47 kΩ resistor. However, if it is desired

FIGURE 16 – TYPICAL MULTIPLIER CONNECTION



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that the scale factor be exact, R_L can be comprised of a fixed resistor and a potentiometer as shown in Figure 16. It should be pointed out that there is nothing magic about setting the scale factor to 1/10. This is merely a convenient factor to use if the V_X and V_Y input voltages are expected to be large, say ±10 V. Obviously with $V_X = V_Y = 10$ V and a scale factor of unity, the device could not hope to provide a 100 V output, so the scale factor is set to 1/10 and provides an output scaled down by a factor of ten. For many applications it may be desirable to set K = 1/2 or K = 1 or even K = 100. This can be accomplished by adjusting R_X, R_Y and R_L appropriately.

The selection of R_L is arbitrary and can be chosen after resistors R_X and R_Y are found. Note in Figure 16 that R_Y is 62 kΩ while R_X is 30 kΩ. The reason for this is that the "Y" side of the multiplier exhibits a second order non-linearity whereas the "X" side exhibits a simple non-linearity. By making the R_Y resistor approximately twice the value of the R_X resistor, the linearity on both the "X" and "Y" sides are made equal. The selection of the R_X and R_Y resistor values is dependent upon the expected amplitude of V_X and V_Y inputs. To maintain a specified linearity, resistors R_X and R_Y should be selected according to the following equations:

$R_X \geq 3\ V_X$ (max) in kΩ when V_X is in volts

$R_Y \geq 6\ V_Y$ (max) in kΩ when V_Y is in volts

For example, if the maximum input on the "X" side is ±1 volt, resistor R_X can be selected to be 3 kΩ. If the maximum input on the "Y" side is also ±1 volt, then resistor R_Y can be selected to be 6 kΩ (6.2 kΩ nominal value). If a scale factor of K = 10 is desired, the load resistor is found to be 47 kΩ. In this example, the multiplier provides a gain of 20 dB.

2.2 Operational Amplifier Selection

The operational amplifier connection in Figure 16 is a simple but extremely accurate current-to-voltage converter. The output current of the multiplier flows through the feedback resistor R_L to provide a low impedance output voltage from the op-ampl. Since the offset current and bias currents of the op-ampl. will cause errors in the output voltage, particularly with temperature, one with very low bias and offset currents is recommended. The MC1556/MC1456 or MC1741/MC1741C are excellent choices for this application.

Since the MC1594 is capable of operation at much higher frequencies than the op-ampl., the frequency characteristics of the circuit in Figure 16 will be primarily dependent upon the op-ampl.

2.3 Stability

The current-to-voltage converter mode is a most demanding application for an operational amplifier. Loop gain is at its maximum and the feedback resistor in conjunction with stray or input capacitance at the multiplier output adds additional phase shift. It may therefore be necessary to add (particularly in the case of internally compensated op-ampls.) a small feedback capacitor to reduce loop gain at the higher frequencies. A value of 10 pF in parallel with R_L should be adequate to insure stability over production and temperature variations, etc.

An externally compensated op-ampl. might be employed using slightly heavier compensation than that recommended for unity-gain operation.

2.4 Offset Adjustment

The non-inverting input of the op-ampl. provides a convenient point to adjust the output offset voltage. By connecting this point to the wiper arm of a potentiometer (P3), the output offset voltage can be adjusted to zero (see offset and scale factor adjustment procedure).

The input offset adjustment potentiometers, P1 and P2 will be necessary for most applications where it is desirable to take advantage of the multiplier's excellent linearity characteristics. Depending upon the particular application, some of the potentiometers can be omitted (see Figures 17, 19, 22, 24 and 25).

2.5 Offset and Scale Factor Adjustment Procedure

The adjustment procedure for the circuit of Figure 16 is:

A. X Input Offset
- (a) connect oscillator (1 kHz, 5 Vpp sinewave) to the "Y" input (pin 9)
- (b) connect "X" input (pin 10) to ground
- (c) adjust X-offset potentiometer, P2 for an ac null at the output

B. Y Input Offset
- (a) connect oscillator (1 kHz, 5 Vpp sinewave) to the "X" input (pin 10)
- (b) connect "Y" input (pin 9) to ground
- (c) adjust Y-offset potentiometer, P1 for an ac null at the output

C. Output Offset
- (a) connect both "X" and "Y" inputs to ground
- (b) adjust output offset potentiometer, P3, until the output voltage V_O, is zero volts dc

D. Scale Factor
- (a) apply +10 Vdc to both the "X" and "Y" inputs
- (b) adjust P4 to achieve -10.00 V at the output
- (c) apply -10 Vdc to both "X" and "Y" inputs and check for V_O = -10.00 V

E. Repeat steps A through D as necessary.

The ability to accurately adjust the MC1594 is dependent on the offset adjust potentiometers. Potentiometers should be of the "infinite" resolution type rather than wirewound. Fine adjustments in balanced-modulator applications may require two potentiometers to provide "coarse" and "fine" adjustment. Potentiometers should have low temperature coefficients and be free from backlash.

2.6 Temperature Stability

While the MC1594 provides excellent performance in itself, overall performance depends to a large degree on the quality of the external components. Previous discussion shows the direct dependence on R_X, R_Y, and R_L and indirect dependence on R1 (through I_1). Any circuit subjected to temperature variations should be evaluated with these effects in mind.

2.7 Bias Currents

The MC1594 multiplier, like most linear IC's, requires a dc bias current into its input terminals. The device cannot be capacitively coupled at the input without regard for this bias current. If inputs V_X and V_Y are able to supply the small bias current (≈ 0.5 μA) resistors, R (Figure 16) can be omitted. If the MC1594 is used in an ac mode of operation and capacitive coupling is used the value of resistor R can be any reasonable value up to 100 kΩ. For minimum noise and optimum temperature performance, the value of resistor R should be as low as practical.

2.8 Parasitic Oscillation

When long leads are used on the inputs, oscillation may occur. In this event, an RC parasitic suppression network similar to the ones shown in Figure 16 should be connected directly to each input using short leads. The purpose of the network is to reduce the "Q" of the source-tuned circuits which cause the oscillation.

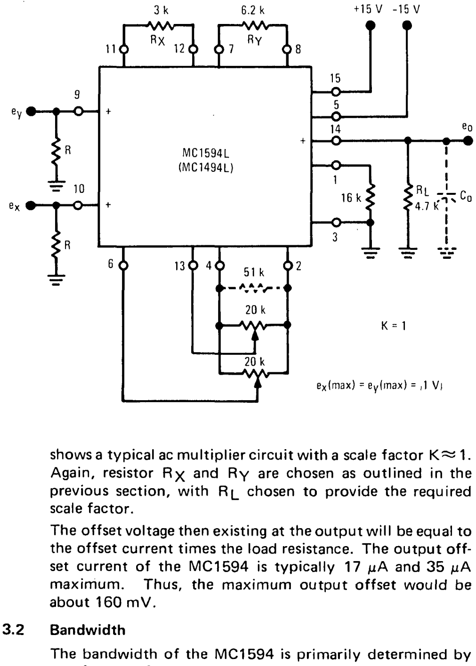
Inability to adjust the circuit to within the specified accuracy may be an indication of oscillation.

3. AC OPERATION

3.1 General

For ac operation, such as balanced modulation, frequency doubler, AGC, etc., the op-ampl. will usually be omitted as well as the output offset adjust potentiometer. The output offset adjust potentiometer is omitted since the output will normally be ac-coupled and the dc voltage at the output is of no concern providing it is close enough to zero volts that it will not cause clipping in the output waveform. Figure 17

FIGURE 17 – WIDEBAND MULTIPLIER



shows a typical ac multiplier circuit with a scale factor $K \approx 1$. Again, resistor R_X and R_Y are chosen as outlined in the previous section, with R_L chosen to provide the required scale factor.

The offset voltage then existing at the output will be equal to the offset current times the load resistance. The output offset current of the MC1594 is typically 17 μA and 35 μA maximum. Thus, the maximum output offset would be about 160 mV.

3.2 Bandwidth

The bandwidth of the MC1594 is primarily determined by two factors. First, the dominant pole will be determined by the load resistor and the stray capacitance at the output terminal. For the circuit shown in Figure 17, assuming a total output capacitance (C_O) of 10 pF, the 3 dB bandwidth would be approximately 3.4 MHz. If the load resistor were 47 kΩ, the bandwidth would be approximately 340 kHz.

Secondly, a "zero" is present in the frequency response characteristic for both the "X" and "Y" inputs which causes the output signal to rise in amplitude at a 6 dB/octave slope at frequencies beyond the breakpoint of the "zero". The "zero" is caused by the parasitic and substrate capacitance which is related to resistors R_X and R_Y and the transistors associated with them. The effect of these transmission "zeros" is seen in Figures 9 and 10. The reason for this increase in gain is due to the bypassing of R_X and R_Y at high frequencies. Since the R_Y resistor is approximately twice the value of the R_X resistor, the zero associated with the "Y" input will occur at approximately one octave below the zero associated with the "X" input. For R_X = 30 kΩ and R_Y = 62 kΩ, the zeros occur at 1.5 MHz for the "X" input and 700 kHz for the "Y" input. These two measured breakpoints correspond to a shunt capacitance of about 3.5 pF. Thus, for the circuit of Figure 17, the "X" input zero and "Y" input zero will be at approximately 15 MHz and 7 MHz respectively.

It should be noted that the MC1594 multiplies in the time domain, hence, its frequency response is found by means of complex convolution in the frequency (Laplace) domain. This means that if the "X" input does not involve a frequency, it is not necessary to consider the "X" side frequency response in the output product. Likewise, for the "Y" side. Thus, for applications such as a wideband linear AGC amplifier which has a dc voltage as one input, the multiplier frequency response has one zero and one pole. For applications which involve an ac voltage on both the "X" and "Y" side, such as a balanced modulator, the product voltage response will have two zeros and one pole, hence, peaking may be present in the output.

From this brief discussion, it is evident that for ac applications; (1) the value of resistors R_X, R_Y and R_L should be kept as small as possible to achieve maximum frequency response, and (2) it is possible to select a load resistor R_L such that the dominant pole (R_L, C_O) cancels the input zero (R_X, 3.5 pF or R_Y, 3.5 pF) to give a flat amplitude characteristic with frequency. This is shown in Figures 9 and 10. Examination of the frequency characteristics of the "X" and "Y" inputs will demonstrate that for wideband amplifier applications, the best tradeoff with frequency response and gain is achieved by using the "Y" input for the ac signal.

For ac applications requiring bandwidths greater than those specified for the MC1594, two other devices are recommended. For modulator-demodulator applications, the MC1596 may be used up to 100 MHz. For wideband multiplier applications, the MC1595 (using small collector loads and ac coupling) can be used.

3.3 Slew-Rate

The MC1594 multiplier is not slew-rate limited in the ordinary sense that an op-ampl. is. Since all the signals in the multiplier are currents and not voltages, there is no charging and discharging of stray capacitors and thus no limitations beyond the normal device limitations. However, it should be noted that the quiescent current in the output transistors is 0.5 mA and thus the maximum rate of change of the output voltage is limited by the output load capacitance by the simple equation:

$$\text{Slew-Rate}\ \frac{\Delta V_O}{\Delta T} = \frac{I_O}{C}$$

Thus, if C_O is 10 pF, the maximum slew-rate would be:

$$\frac{\Delta V_O}{\Delta T} = \frac{0.5 \times 10^{-3}}{10 \times 10^{-12}} = 50\ \text{V}/\mu\text{s}$$

This can be improved if necessary by addition of an emitter-follower or other type of buffer.

3.4 Phase-Vector Error

All multipliers are subject to an error which is known as the phase-vector error. This error is a phase error only and does not contribute an amplitude error per se. The phase-vector error is best explained by an example. If the "X" input is described in vector notation as

$$X = A \measuredangle 0^o$$

and the "Y" input is described as

$$Y = B \measuredangle 0^o$$

then the output product would be expected to be

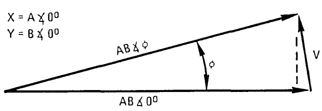
$$V_o = AB \measuredangle 0^o \text{ (see Figure 18)}$$

However, due to a relative phase shift between the "X" and "Y" channels, the output product will be given by

$$V_o = AB \measuredangle \phi$$

Notice that the magnitude is correct but the phase angle of the product is in error. The vector, V, associated with this error is the "phase-vector error". The startling fact about the phase-vector error is that it occurs and accumulates much more rapidly than the amplitude error associated with frequency response. In fact, a relative phase shift of only 0.57^o will result in a 1% phase-vector error. For most applications, this error is meaningless. If phase of the output product is not important, then neither is the phase-vector error. If phase is important, such as in the case of double sideband modulation or demodulation, then a 1% phase-vector error will represent a 1% amplitude error at the phase angle of interest.

FIGURE 18 – PHASE-VECTOR ERROR



3.5 Circuit Layout

If wideband operation is desired, careful circuit layout must be observed. Stray capacitance across R_X and R_Y should be avoided to minimize peaking (caused by a zero created by the parallel RC circuit).

4. DC APPLICATIONS

4.1 Squaring Circuit

If the two inputs are connected together, the resultant function is squaring:

$$V_o = KV^2$$

where K is the scale factor (see Figure 19).

However, a more careful look at the multiplier's defining equation will provide some useful information. The output voltage, without initial offset adjustments is given by:

$$V_o = K(V_x + V_{iox} - V_{x\,off})\,(V_y + V_{ioy} - V_{y\,off}) + V_{oo}$$

(See "Definitions" for an explanation of terms).

With $V_x = V_y = V$ (squaring) and defining

$$\epsilon_x = V_{iox} - V_{x\,off}$$

$$\epsilon_y = V_{ioy} - V_{y\,off}$$

The output voltage equation becomes

$$V_o = K\,V_x^2 + KV_x\,(\epsilon_x + \epsilon_y) + K\epsilon_x\epsilon_y + V_{oo}$$

This shows that all error terms can be eliminated with only three adjustment potentiometers, eliminating one of the input offset adjustments. For instance, if the "X" input offset adjustment is eliminated, ϵ_x is determined by the internal offset, V_{iox}, but ϵ_y is adjustable to the extent that the $(\epsilon_x + \epsilon_y)$ term can be zeroed. Then the output offset adjustment is used to adjust the V_{oo} term and thus zero the remaining error terms. An ac procedure for nulling with three adjustments is:

A. AC Procedure:

1. Connect oscillator (1 kHz, 15 Vpp) to input
2. Monitor output at 2 kHz with tuned voltmeter and adjust P4 for desired gain (Be sure to peak response of voltmeter)
3. Tune voltmeter to 1 kHz and adjust P1 for a minimum output voltage
4. Ground input and adjust P3 (output offset) for zero volts dc out
5. Repeat steps 1 through 4 as necessary.

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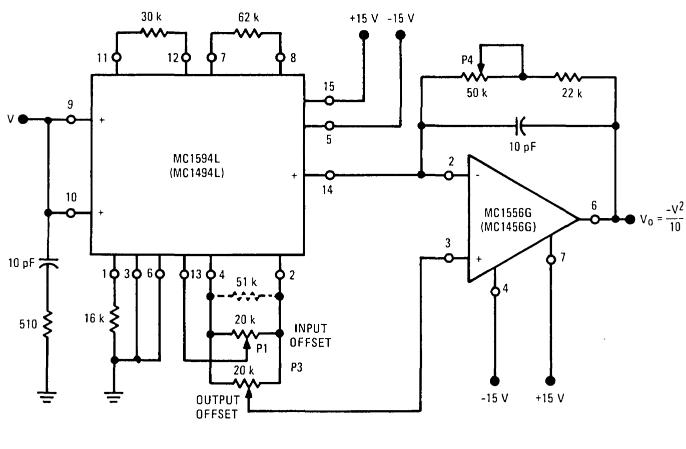
FIGURE 19 – MC1594 SQUARING CIRCUIT



B. DC Procedure:

1. Set $V_X = V_Y = 0$ V and adjust P3 (output offset potentiometer) such that $V_o = 0.0$ Vdc
2. Set $V_X = V_Y = 1.0$ V and adjust P1 (Y input offset potentiometer) such that the output voltage is -0.100 volts
3. Set $V_X = V_Y = 10$ Vdc and adjust P4 (load resistor) such that the output voltage is -10.00 volts
4. Set $V_X = V_Y = -10$ Vdc. Repeat steps 1 through 4 as necessary.

4.2 Divide

Divide circuits warrant a special discussion as a result of their special problems. Classic feedback theory teaches that if a multiplier is used as a feedback element in an operational amplifier circuit, the divide function results. Figure 20 illustrates the theoretical simplicity of such an approach and a practical realization is shown in Figure 21.

The characteristic "failure" mode of the divide circuit is latch-up. One way it can occur is if V_X is allowed to go negative or, in some cases, if V_X approaches zero.

Figure 20 illustrates why this is so. For $V_X > 0$ the transfer function through the multiplier is non-inverting. Its output is fed to the inverting input of the op-ampl. Thus, operation is in the negative feedback mode and the circuit is dc stable. Should V_X change polarity, the transfer function through the multiplier becomes inverting, the amplifier has positive feedback and latch-up results. The problem resulting from V_X being near zero is a result of the transfer through the multiplier being near zero. The op-ampl. is then operating with a very high closed loop gain and error voltages can thus become effective in causing latch-up.

The other mode of latch-up results from the output voltage of the op-ampl. exceeding the rated common-mode input voltage of the multiplier. The input stage of the multiplier becomes saturated, phase reversal results, and the circuit is latched up. The circuit of Figure 21 protects against this happening by clamping the output swing of the op-ampl. to approximately ± 10.7 volts. Five-percent tolerance, 10-volt zeners are used to assure adequate output swing but still limit the output voltage of the op-ampl. from exceeding the common-mode input range of the MC1594.

Setting up the divide circuit for reasonably accurate operation is somewhat different from the procedure for the multiplier itself. One approach, however, is to break the feedback loop, null out the multiplier circuit, and then close the loop.

A simpler approach, since it does not involve breaking the loop (thus making it more practical on a production basis), is:

1. Set $V_Z = 0$ volts and adjust the output offset potentiometer (P3) until the output voltage (V_O) remains at some (not necessarily zero) constant value as V_X is varied between +1.0 volt and +10 volts.
2. Maintain V_Z at 0 volts, set V_X at +10 volts and adjust the Y input offset potentiometer (P1) until $V_o = 0$ volts.
3. With $V_X = V_Z$, adjust the X input offset potentiometer (P2) until the output voltage remains at some (not necessarily - 10 volts) constant value as $V_Z = V_X$ is varied between +1.0 volt and +10 volts.
4. Maintain $V_X = V_Z$ and adjust the scale factor potentiometer (R_L) until the average value of V_o is -10 volts as $V_Z = V_X$ is varied between +1.0 volt and +10 volts.
5. Repeat steps 1 through 4 as necessary to achieve optimum performance.

Users of the divide circuit should be aware that the accuracy to be expected decreases in direct proportion to the denomi-

FIGURE 20 – BASIC DIVIDE CIRCUIT USING MULTIPLIER

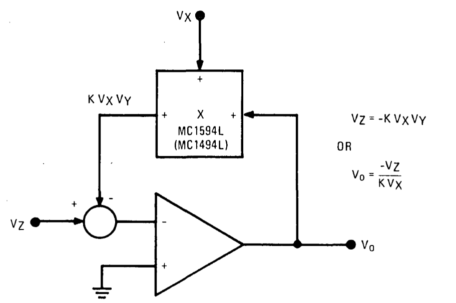


FIGURE 21 – PRACTICAL DIVIDE CIRCUIT

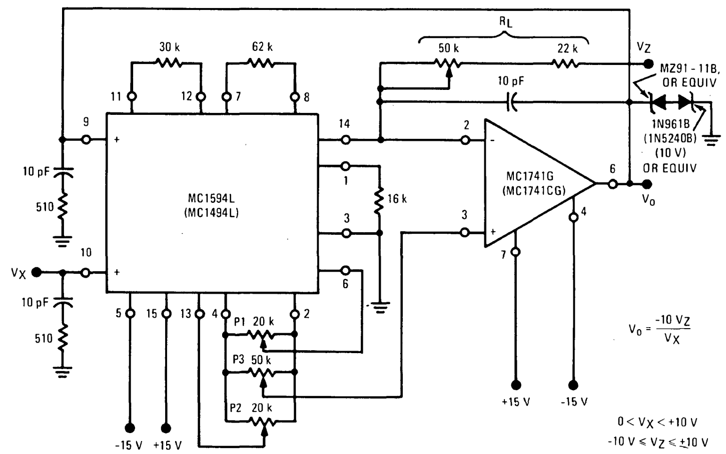
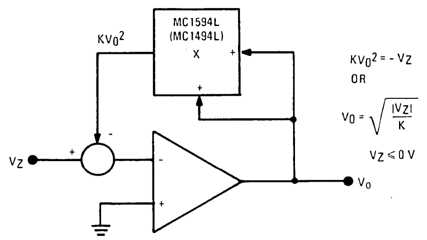


FIGURE 22 – BASIC SQUARE ROOT CIRCUIT



nator voltage. As a result, if V_X is set to 10 volts and 0.5% accuracy is available, then 5% accuracy can be expected when V_X is only 1 volt.

In accordance with an earlier statement, V_X may have only one polarity, positive, while V_Z may be either polarity.

4.3 Square Root

A special case of the divide circuit in which the two inputs to the multiplier are connected together results in the square root function as indicated in Figure 22. This circuit too may suffer from latch-up problems similar to those of the divide circuit. Note that only one polarity of input is allowed and diode clamping (see Figure 23) protects against accidental latch-up.

This circuit too, may be adjusted in the closed-loop mode:

1. Set V_Z = -0.1 Vdc and adjust P3 (output offset) for V_O = 0.316 Vdc.
2. Set V_Z to -0.9 Vdc and adjust P2 ("X" adjust) for V_O = +3 Vdc.
3. Set V_Z to -10 Vdc and adjust P4 (gain adjust) for V_O = +10 Vdc.

Steps 1 through 3 may be repeated as necessary to achieve desired accuracy.

Note: Operation near zero volts input may prove very inaccurate, hence, it may not be possible to adjust V_O to 0 but rather only to within 100 to 400 mV of zero.

5. AC APPLICATIONS

5.1 Wideband Amplifier With Linear AGC

If one input to the MC1594 is a dc voltage and a signal voltage is applied to the other input, the amplitude of the output signal can be controlled in a linear fashion by varying the dc voltage. Hence, the multiplier can function as a dc coupled, wideband amplifier with linear AGC control.

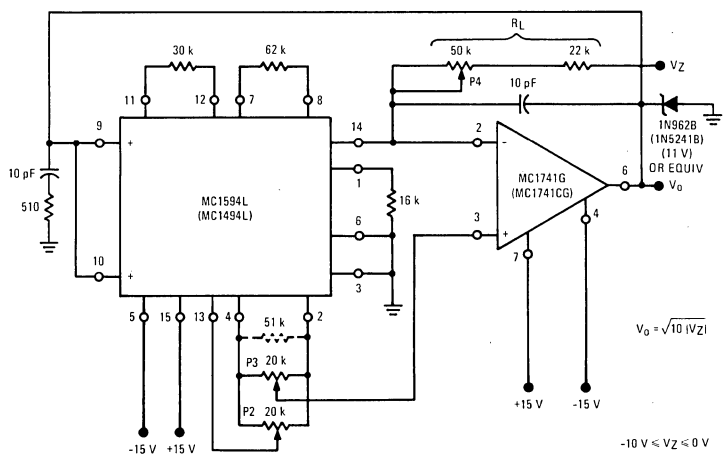
In addition to the advantage of Linear AGC control, the multiplier has three other distinct advantages over most other types of AGC systems. First, the AGC dynamic range is theoretically infinite. This stems from the basic fact that with zero volts dc applied to the AGC, the output will be zero regardless of the input. In practice, the dynamic range is limited by the ability to adjust the input offset adjust potentiometers. By using cermet multi-turn potentiometers, a dynamic range of 80 dB can be obtained. The second advantage of the multiplier is that variation of the AGC voltage has no effect on the signal handling capability of the signal port, nor does it alter the input impedance of the signal port. This feature is particularly important in AGC systems which are phase sensitive. A third advantage of the multiplier is that the output-voltage-swing capability and output impedance are unchanged with variations in AGC voltage.

The circuit of Figure 24 demonstrates the linear AGC amplifier. The amplifier can handle 1 V(rms) and exhibits a gain of approximately 20 dB. It is AGC'd through a 60 dB dynamic range with the application of an AGC voltage from 0 Vdc to 1 Vdc. The bandwidth of the amplifier is determined by the load resistor and output stray capacitance. For this reason, an emitter-follower buffer has been added to extend the bandwidth in excess of 1 MHz.

5.2 Balanced Modulator

When two-time variant signals are used as inputs, the result-

FIGURE 23 – SQUARE ROOT CIRCUIT



ing output is suppressed-carrier double-sideband modulation. In terms of sinusoidal inputs, this can be seen in the following equation:

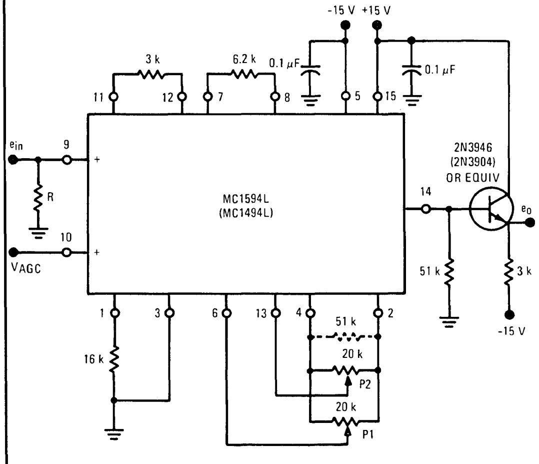
$$V_o = K(e_1 \cos\omega_m t)(e_2 \cos\omega_c t)$$

where ω_m is the modulation frequency and ω_c is the carrier frequency. This equation can be expanded to show the suppressed carrier or balanced modulation:

$$V_o = \frac{Ke_1e_2}{2}\left[\cos(\omega_c + \omega_m)t + \cos(\omega_c - \omega_m)t\right]$$

Unlike many modulation schemes, which are non-linear in nature, the modulation which takes place when using the MC1594 is linear. This means that for two sinusoidal inputs, the output will contain only two frequencies, the sum and difference, as seen in the above equation. There will be no spectrum centered about the second harmonic of the carrier, or any multiple of the carrier. For this reason, the filter requirements of a modulation system are reduced to the minimum. Figure 25 shows the MC1594 configuration to perform this function.

FIGURE 24 – WIDEBAND AMPLIFIER WITH LINEAR AGC

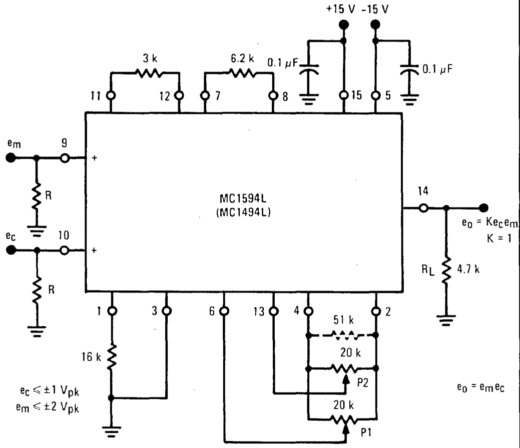


Notice that the resistor values for R_X, R_Y, and R_L have been modified. This has been done primarily to increase the bandwidth by lowering the output impedance of the MC1594 and then lowering R_X and R_Y to achieve a gain of 1. The e_c can be as large as 1 volt peak and e_m as high as 2 volts peak. No output offset adjust is employed since we are interested only in the ac output components.

The input R's are used to supply bias current to the multiplier inputs as well as provide matching input impedance. The output frequency range of this configuration is determined by the 4.7 k ohm output impedance and capacitive loading. Assuming a 6 pF load, the small-signal bandwidth is 5.5 MHz.

The circuit of Figure 25 will provide a typical carrier rejection of ≥70 dB from 10 kHz to 1.5 MHz.

FIGURE 25 – BALANCED MODULATOR



The adjustment procedure for this circuit is quite simple.

(1) Place the carrier signal at pin 10. With no signal applied to pin 9, adjust potentiometer P1 such that an ac null is obtained at the output.

(2) Place a modulation signal at pin 9. With no signal applied to pin 10, adjust potentiometer P2 such that an ac null is obtained at the output.

Again, the ability to make careful adjustment of these offsets will be a function of the type of potentiometers used for P1 and P2. Multiple turn cermet type potentiometers are recommended.

5.3 Frequency Doubler

If for Figure 25 both inputs are identical;

$$e_m = e_c = E\cos\omega t$$

Then the output is given by

$$e_o = e_m e_c = E^2\cos^2\omega t$$

which reduces to

$$e_o = \frac{E^2}{2}(1 + \cos 2\omega t)$$

This equation states that the output will consist of a dc term equal to one half the peak voltage squared and the second harmonic of the input frequency. Thus, the circuit acts as a frequency doubler. Two facts about this circuit are worthy of note. First, the second harmonic of the input frequency is the only frequency appearing at the output. The fundamental does not appear. Second, if the input is sinusoidal, the output will be sinusoidal and requires no filtering.

The circuit of Figure 25 can be used as a frequency doubler with input frequencies in excess of 2 MHz.

5.4 Amplitude Modulator

The circuit of Figure 25 is also easily used as an amplitude modulator. This is accomplished by simply varying the input offset adjust potentiometer (P1) associated with the modulation input. This procedure places a dc offset on the modulation input of the multiplier such that the carrier still passes thru the multiplier when the modulating signal is zero. The result is amplitude modulation. This is easily seen by examining the basic mathematical expression for amplitude modulation given below. For the case under discussion, with K = 1,

$$e_o = (E + E_m \cos\omega_m t)\,(E_c \cos\omega_c t)$$

where E is the dc input offset adjust voltage. This expression can be written as:

$$e_o = E_o\,[1 + M \cos\omega_c t]\,\cos\omega_c t$$

where $E_o = EE_c$

and $M = \frac{E_m}{E}$ = modulation index

This is the standard equation for amplitude modulation. From this, it is easy to see that 100% modulation can be achieved by adjusting the input offset adjust voltage to be exactly equal to the peak value of the modulation, E_m. This is done by observing the output waveform and adjusting the input offset potentiometer, P1, until the output exhibits the familiar amplitude modulation waveform.

5.5 Phase Detector

If the circuit of Figure 25 has as its inputs two signals of identical frequency but having a relative phase shift the output will be a dc signal which is directly proportional to the cosine of phase difference as well as the double frequency term.

$$e_c = E_c \cos\omega_c t$$

$$e_m = E_m \cos(\omega_c t + \phi)$$

$$e_o = e_c e_m = E_c E_m \cos\omega_c t \cos(\omega_c t + \phi)$$

or

$$e_o = \frac{E_c E_m}{2}\,[\cos\phi + \cos(2\omega_c t + \phi)]$$

The addition of a simple low pass filter to the output (which eliminates the second cosine term) and return of R_L to an offset adjustment potentiometer will result in a dc output voltage which is proportional to the cosine of the phase difference. Hence, the circuit functions as a synchronous detector.

6. DEFINITIONS OF SPECIFICATIONS

Because of the unique nature of a multiplier, i.e., two inputs and one output, operating specifications are difficult to define and interpret. Indeed the same specification may be defined in several completely different ways depending upon which manufacturer is doing the defining. In order to clear up some of this mystery, the following definitions and examples are presented.

6.1 Multiplier Transfer Function

The output of the multiplier may be expressed by this equation:

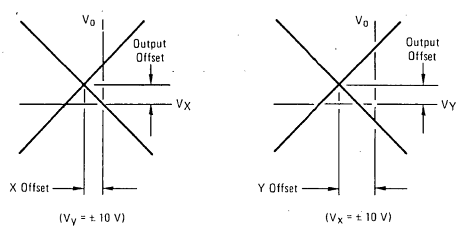
$$V_o = K\,(V_x \pm V_{iox} - V_{x\,off})\,(V_y \pm V_{ioy} - V_{y\,off}) \pm V_{oo} \quad (1)$$

where K = scale factor (see 6.5)

V_x = "x" input voltage
V_y = "y" input voltage
V_{iox} = "x" input offset voltage
V_{ioy} = "y" input offset voltage
$V_{x\,off}$ = "x" input offset adjust voltage
$V_{y\,off}$ = "y" input offset adjust voltage
V_{oo} = output offset voltage

The voltage transfer characteristic below indicates "X", "Y" and output offset voltages.

FIGURE 26



6.2 Linearity

Linearity is defined to be the maximum deviation of output voltage from a straight line transfer function. It is expressed as a percentage of full-scale output and is measured for V_x and V_y separately either using an "X-Y" plotter (and checking the deviation from a straight line) or by using the method shown in Figure 1. The latter method nulls the output signal with the input signal, resulting in distortion components proportional to the linearity.

Example: 0.35% linearity means

$$V_o = \frac{V_x V_y}{10} \pm (0.0035)\,(10 \text{ volts})$$

6.3 Input Offset Voltage

The input offset voltage is defined from Equation (1). It is measured for V_x and V_y separately and is defined to be that dc input offset adjust voltage ("x" or "y") that will result in minimum ac output when ac (5 Vpp, 1 kHz) is applied to the other input ("y" or "x" respectively). From Equation (1) we have:

$$V_{o(ac)} = K\,(0 \pm V_{iox} - V_{x\,off})\,(\sin\omega t)$$

adjust $V_{x\,off}$ so that $(\pm V_{iox} - V_{x\,off}) = 0$.

6.4 Output Offset Current and Voltage

Output offset current (I_{oo}) is the dc current flowing in the output lead when $V_x = V_y = 0$ and "X" and "Y" offset voltages are adjusted to zero.

Output offset voltage (V_{oo}) is:

$$V_{oo} = I_{oo} R_L$$

where R_L is the load resistance.

Note: Output offset voltage is defined by many manufacturers with all inputs at zero but without adjusting "X" and "Y" offset voltages to zero. Thus it includes input offset terms, an output offset term and a scale factor term.

6.5 Scale Factor

Scale factor is the K term in Equation (1). It determines the "gain" of the multiplier and is expressed approximately by the following equation.

$$K = \frac{2R_L}{R_x R_y I_1} \text{ where } R_x \text{ and } R_y \gg \frac{kT}{qI_1}$$

and I_1 is the current out of pin 1.

6.6 Total DC Accuracy

The total dc accuracy of a multiplier is defined as error in multiplier output with dc (±10 Vdc) applied to both inputs. It is expressed as a percent of full scale. Accuracy is not specified for the MC1594 because error terms can be nulled by the user.

6.7 Temperature Stability (Drift)

Each term defined above will have a finite drift with temperature. The temperature specifications are obtained by re-adjusting the multiplier offsets and scale factor at each new temperature (see previous definitions and the adjustment procedure) and noting the change.

Assume inputs are grounded and initial offset voltages have been adjusted to zero. Then output voltage drift is given by:

$$\Delta V_o = \pm[K \pm K\ (TCK)\ (\Delta T)\ ]\ [\ (TCV_{iox})\ (\Delta T)\ ]\ [\ (TCV_{ioy})\ (\Delta T)\ ]\ \pm\ (TCV_{oo})\ (\Delta T)$$

6.8 Total DC Accuracy Drift

This is the temperature drift in output voltage with 10 volts applied to each input. The output is adjusted to 10 volts at T_A = +25°C. Assuming initial offset voltages have been adjusted to zero at T_A = +25°C, then:

$$V_o = [K \pm K\ (TCK)\ (\Delta T)\ ]\ [10 \pm (TCV_{iox})\ (\Delta T)\ ]\ [10 \pm (TCV_{ioy})\ (\Delta T)\ ]\ \pm\ (TCV_{oo})\ (\Delta T)$$

6

6.9 Power Supply Rejection

Variation in power supply voltages will cause undesired variation of the output voltage. It is measured by superimposing a 1-volt, 100-Hz signal on each supply (±15 V) with each input grounded. The resulting change in the output is expressed in mV/V.

6.10 Output Voltage Swing

Output voltage swing capability is the maximum output voltage swing (without clipping) into a resistive load (note-output offset is adjusted to zero).

If an op-ampl. is used, the multiplier output becomes a virtual ground — the swing is then determined by the scale factor and the op-ampl. selected.

GENERAL INFORMATION INDEX

MULTIPLIERS

MC1595L
MC1495L

MONOLITHIC FOUR-QUADRANT MULTIPLIER

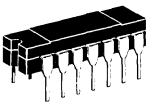
. . . designed for uses where the output voltage is a linear product of two input voltages. Typical applications include: multiply, divide*, square root*, mean square*, phase detector, frequency doubler, balanced modulator/demodulator, electronic gain control.

*When used with an operational amplifier

- Excellent Linearity — 1% max error on X-Input, 2% max error on Y-Input — MC1595L
- Excellent Linearity — 2% max error on X-Input, 4% max error on Y-Input — MC1495L
- Adjustable Scale Factor, K
- Excellent Temperature Stability
- Wide Input Voltage Range — ±10 Volts

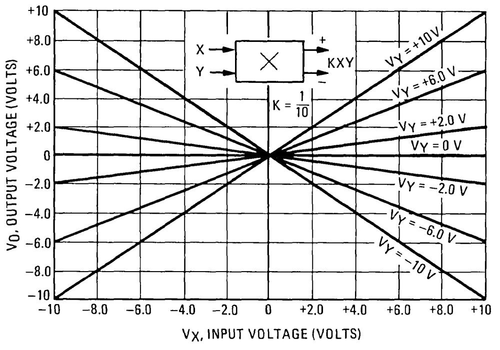
LINEAR FOUR-QUADRANT MULTIPLIER INTEGRATED CIRCUIT

MONOLITHIC SILICON EPITAXIAL PASSIVATED

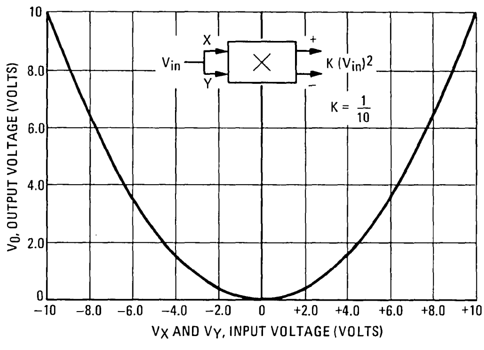


L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

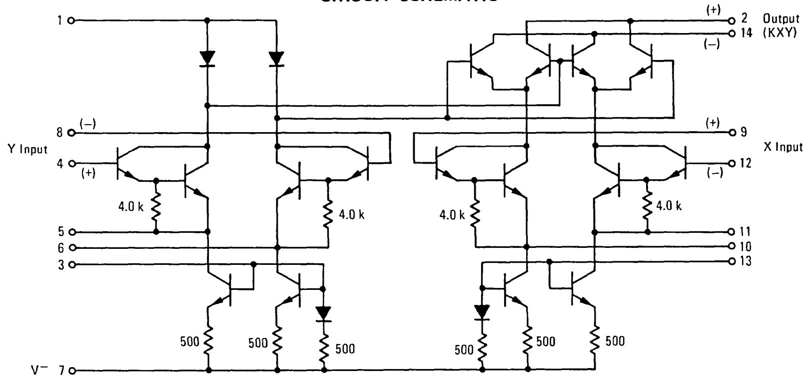
FOUR-QUADRANT MULTIPLIER TRANSFER CHARACTERISTIC



SQUARING MODE TRANSFER CHARACTERISTIC



CIRCUIT SCHEMATIC



See Packaging Information Section for outline dimensions.

See current MCC1595/1495 data sheet for standard linear chip information.

ELECTRICAL CHARACTERISTICS (V^+ = +32 V, V^- = −15 V, T_A = 25°C, $I_3 = I_{13}$ = 1 mA, $R_X = R_Y$ = 15 kΩ, R_L = 11 kΩ unless otherwise noted)

Characteristic	Figure	Note	Symbol	Min	Typ	Max	Unit
Linearity:							
Output Error in Percent of Full Scale:	1	4,6					%
T_A = 25°C							
$-10 < V_X < +10$ ($V_Y = \pm 10$ V) MC1495			E_{RX}	–	1.0	2.0	
MC1595				–	0.5	1.0	
$-10 < V_Y < +10$ ($V_X = \pm 10$ V) MC1495			E_{RY}	–	2.0	4.0	
MC1595				–	1.0	2.0	
T_A = 0 to +70°C MC1495							
$-10 < V_X < +10$ ($V_Y = \pm 10$ V)			E_{RX}	–	1.5	–	
$-10 < V_Y < +10$ ($V_X = \pm 10$ V)			E_{RY}	–	3.0	–	
T_A = −55°C to +125°C MC1595							
$-10 < V_X < +10$ ($V_Y = \pm 10$ V)			E_{RX}	–	0.75	–	
$-10 < V_Y < +10$ ($V_X = \pm 10$ V)			E_{RY}	–	1.50	–	
Squaring Mode Error:							
Accuracy in Percent of Full Scale After Offset and Scale Factor Adjustment	1	1,5,6,7	E_{SQ}				%
T_A = 25°C MC1495				–	0.75	–	
MC1595				–	0.5	–	
T_A = 0 to +70°C MC1495				–	1.0	–	
T_A = −55°C to +125°C MC1595				–	0.75	–	
Scale Factor (Adjustable) $\left(K = \frac{2R_L}{I_3 R_X R_Y}\right)$	1	2,7	K	–	0.1	–	–
Input Resistance (f = 20 Hz) MC1495	2	–	R_{INX}	–	20	–	MegOhms
MC1595				–	35	–	
MC1495			R_{INY}	–	20	–	
MC1595				–	35	–	
Differential Output Resistance (f = 20 Hz)	3	–	R_o	–	300	–	k Ohms
Input Bias Current							
$I_{bx} = \frac{(I_9 + I_{12})}{2}$, $I_{by} = \frac{(I_4 + I_8)}{2}$ MC1495	4	–	I_{bx}	–	2.0	12	μA
MC1595				–	2.0	8.0	
MC1495			I_{by}	–	2.0	12	
MC1595				–	2.0	8.0	
Input Offset Current							
$\lvert I_9 - I_{12} \rvert$ MC1495	4	–	$\lvert I_{iox} \rvert$	–	0.4	2.0	μA
MC1595				–	0.2	1.0	
$\lvert I_4 - I_8 \rvert$ MC1495			$\lvert I_{ioy} \rvert$	–	0.4	2.0	
MC1595				–	0.2	1.0	
Average Temperature Coefficient of Input Offset Current	4	–	$\lvert TC_{Iio} \rvert$				nA/°C
(T_A = 0 to +70°C) MC1495				–	2.0	–	
(T_A = −55°C to +125°C) MC1595				–	2.0	–	
Output Offset Current	4	–	$\lvert I_{oo} \rvert$				μA
$\lvert I_{14} - I_2 \rvert$ MC1495				–	20	100	
MC1595				–	10	50	
Average Temperature Coefficient of Output Offset Current	4	–	$\lvert TC_{Ioo} \rvert$				nA/°C
(T_A = 0 to +70°C) MC1495				–	20	–	
(T_A = −55°C to +125°C) MC1595				–	20	–	
Frequency Response							
3.0 dB Bandwidth	5	9	BW_{3dB}	–	3.0	–	MHz
3° Relative Phase Shift Between V_X and V_Y			f_ϕ	–	750	–	kHz
1% Absolute Error Due to Input-Output Phase Shift			f_θ	–	30	–	kHz
Common Mode Input Swing	6	–	CMV				Vdc
(Either Input) MC1495				±10.5	±12	–	
MC1595				±11.5	±13	–	
Common Mode Gain	6	–	A_{CM}				dB
(Either Input) MC1495				-40	-50	–	
MC1595				-50	-60	–	
Common Mode Quiescent Output Voltage	1	1,7	V_{o1}	–	21	–	Vdc
			V_{o2}	–	21	–	
Differential Output Voltage Swing Capability	1	7	V_{out}	–	±14	–	V_{peak}
Power Supply Sensitivity	7	3	S^+	–	5.0	–	mV/V
			S^-	–	10	–	
Power Supply Current	1	–	I_7	–	6.0	7.0	mA
DC Power Dissipation	1	8	P_D	–	135	170	mW

6

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Applied Voltage (V_2-V_1, $V_{14}-V_1$, V_1-V_9, V_1-V_{12}, V_1-V_4, V_1-V_8, $V_{12}-V_7$, V_9-V_7, V_8-V_7, V_4-V_7)	ΔV	30	Vdc
Differential Input Signal	$V_{12}-V_9$ V_4-V_8	$\pm(6+I_{13}R_X)$ $\pm(6+I_3R_Y)$	Vdc Vdc
Maximum Bias Current	I_3 I_{13}	10 10	mA
Power Dissipation (Package Limitation) Ceramic Package Derate above 25°C	P_D	 750 5.0	 mW mW/°C
Operating Temperature Range MC1495 MC1595	T_A	 0 to +70 -55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

NOTE 1: Typical Multiplier Operation

For most applications, the multiplier must be nulled as described in Note 7. If this is not done, dc errors will result which make the multiplier unusable for most applications.

Depending on the maximum input voltage desired and the external circuitry used with this multiplier, several different positive supply voltages are possible as indicated below.

The multiplier is normally used with external circuitry which is designed to remove the common mode output voltage. Four recommended circuits for doing this are shown in Figures 1, 10, 11 and 12. In Figure 1, the multiplier differential output is connected to an XY plotter that provides the common-mode rejection. This circuit is useful for measuring accuracy and linearity and is representative of applications where a differential load can be used. The circuits of Figures 10 and 11 both provide output dc level translation which removes the common-mode voltage and produces a single ended output. An operational amplifier is used in Figures 10 and 11 for level shifting and is more accurate than the discrete circuit of Figure 12. Figure 10 allows operation with maximum inputs of ±10 volts with a +32 V supply and ±5 V maximum inputs with a ±15 V supply. The op-amp circuit has the advantage of being rather simple and relatively temperature insensitive. It has the disadvantage of being frequency limited to about 50 kHz for large signal swings due to the slew rate of the operational amplifier. The circuit of Figure 11 has the full ±10 volt input – yet operates from ±15 V supplies. Figure 12 uses discrete components to perform the level shifting, which makes it very inexpensive, simple, and permits operation at higher frequencies (limited by the 7.5 k ohm resistor and stray capacitance associated with the output). The circuit of Figure 12 has the additional advantage of being able to handle larger input voltages (±10 V) while still operating from ±15 V supplies. This circuit has the disadvantage, however, of being temperature sensitive if the base-emitter junctions of the NPN and the PNP are not matched to track with temperature. This problem can be greatly reduced by using complementary-pair transistors mounted in the same package such as the Motorola MD6100. A second problem with this level shifting circuit is a high output impedance with little current drive capabilities. This problem can be solved by placing an operational amplifier at the output as shown or, if high frequency operation is desired, an emitter follower using a discrete transistor can be used to replace the op-amp.

NOTE 2: Scale Factor Calculation

The differential output voltage of the multiplier is given by:

$$V_{out} = V_{o1} - V_{o2} = \frac{2V_X V_Y R_L}{I_3\left(R_X + \frac{2kT}{qI_{13}}\right)\left(R_Y + \frac{2kT}{qI_3}\right)}.$$

$$= K V_X V_Y \qquad \text{(See Figure 1)}$$

where $\frac{kT}{q}$ = 26 mV at 25°C. The scale factor, K, (usually $\frac{1}{10}$) can be adjusted with a suitable choice of I_3, R_X, R_Y and R_L as described in Note 11.

Note that the value given for R_3 in Figures 10 to 13 is approximate; it should be adjusted to set the I_3 which will provide the exact gain (K-factor) desired. Note that I_3 not only controls the K-factor, but also controls the signal handling capability of the Y input and the voltage at pin 1 (relating to output swing capability). Its range should therefore be limited to small adjustments about the quiescent current value. For larger adjustments see Note 10 on R_L selection.

NOTE 3: Power Supply Sensitivity

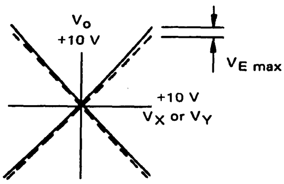
In some cases, it may be desirable to provide separate power supply regulation for I_3, since the multiplier gain is directly dependent on this current.

NOTE 4: Linearity

Linearity is measured for V_X and V_Y separately using an X-Y plotter with the circuit as shown in Figure 1. It is defined to be the maximum deviation of output voltage from a straight line transfer function expressed as error in percent of full scale; see figure below. For example, if the maximum deviation, $V_{E(max)}$, is 100 mV and the full scale output is 10 V, then the error is:

$$E_R = \frac{V_{E(max)}}{V_{o(max)}} \times 100 = \frac{100 \times 10^{-3}}{10\text{ V}} \times 100 = 1\%$$

To measure this, the X-Y plotter is set up first to plot V_{out} versus V_X in all four quadrants ($V_Y = \pm 10$ V, $-10\ V \leqslant V_X \leqslant +10$ V) then V_{out} versus V_Y ($V_X = \pm 10$ V, $-10\ V \leqslant V_Y \leqslant +10$ V). The maximum deviations for X and Y are then determined as shown below. It is desirable, but not necessary, to "zero out" the multiplier static error (see Note 7) before making this test.



NOTE 5: Squaring Mode Accuracy is defined as the maximum absolute deviation from a square law curve expressed as a percent of full scale output. This deviation may be measured by connecting the X and Y inputs together (squaring mode) and plotting output versus input, $-10\ V \leqslant V_X = V_Y \leqslant +10$ V, using an X-Y plotter as shown in Figure 1. Before performing this test, the multiplier static error must be "zeroed out" as in Note 7.

NOTE 6: Sources of Multiplier Error

a. The major source of error in the multiplier arises from voltage offsets and ohmic base resistances in the four output transistors and the base diodes. The static error adjustment procedure described in Note 7 removes as much of this error as possible by offsetting the input differential amplifiers to compensate for the output unbalance.

b. A second and usually small source of error can arise from large signal nonlinearity in the X and Y-input differential amplifiers. To avoid introducing error from this source, the emitter degeneration resistors R_X and R_Y must be chosen large enough so that nonlinear base-emitter voltage variation can be ignored. Figure 8 shows the error expected from this source as a function of the values of R_X and R_Y with an operating current of 1.0 mA in each side of the differential amplifiers (i.e., $I_3 = I_{13} = 1.0$ mA).

c. Care must also be taken to avoid aging and temperature drift in the external components used with the multiplier. This is especially important in the level translation circuitry of Figures 10, 11, and 12.

d. At high frequencies, relative phase differences between the X and Y channels will cause errors in the output product as discussed in Note 9.

NOTE 7: Static Error and Scale Factor Adjustment Procedure

To obtain usable absolute output accuracy, several adjustments must be made in the external multiplier circuitry. For small inputs, the differential output voltage for a typical unadjusted multiplier may be written as:

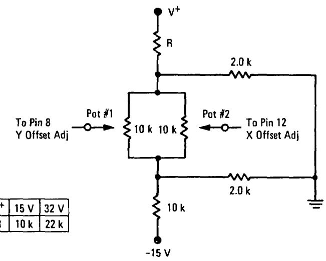
$$V_{out} = K\,(V_X \pm \phi_X \pm V_{X\ offset})\,(V_Y \pm \phi_Y \pm V_{Y\ offset}) \pm V_{o\ offset}$$

Where ϕ_X is an equivalent X input offset term
ϕ_Y is an equivalent Y input offset term
$V_{o\ offset}$ is an output offset that remains after the inputs are zeroed.

Following are three different adjustment procedures requiring:

1. an ac voltmeter or oscilloscope (Procedure I)
2. a digital voltmeter (Procedure II)
3. an X-Y plotter (Procedure III)

Each procedure allows the X and Y inputs to be "zeroed" first by setting $V_{X\ offset} = -\phi_X$ and $V_{Y\ offset} = -\phi_Y$. Next $V_{o\ offset}$ is removed by an output adjustment and K is adjusted for the correct gain. For these procedures the X, Y offset adjust circuitry shown below should be used.



V+	15 V	32 V
R	10 k	22 k

Procedure I (AC Voltmeter or Oscilloscope)

A. X-Y Offset Adjust

1. Connect an ac voltmeter or oscilloscope to the output.
2. Connect 1.0 kHz, 1.0 $V_{p\text{-}p}$ oscillator to Y input, ground X input, adjust X offset for an output null.
3. Connect 1.0 kHz, 1.0 $V_{p\text{-}p}$ oscillator to X input, ground Y input, adjust Y offset for an output null.

B. Output Offset Adjust

1. For the circuits of Figures 10, 11, and 12, adjust "output offset adjust" potentiometers for zero output.

C. Scale Factor Adjust

1. Set $V_X = +5.0$ Vdc, $V_Y = +5.0$ Vdc and adjust gain potentiometer (I_3) for +2.5 Vdc out.
2. To check, let $V_X = -5.0$ Vdc, $V_Y = -5.0$ Vdc and check for +2.5 Vdc out – if error occurs repeat steps A, B and C.

Procedure II (Digital Voltmeter)

A. X-Y Offset Adjust

1. Set $V_X = V_Y = 0$ volts. Adjust output offset potentiometer until the output reads zero volts.
2. Set $V_X = 5.000$ volts, $V_Y = 0.000$ volts and ad-

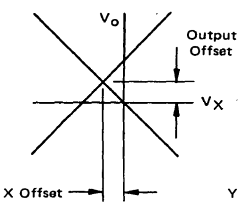
just the Y input offset potentiometer until output reads zero volts.

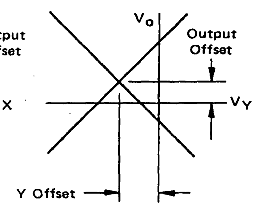
3. Set V_Y = 5.000 volts, V_X = 0.000 volts and adjust the X input offset potentiometer until output reads zero volts.
4. Repeat step 1.
5. Set $V_X = V_Y$ = 5.000 volts and adjust the K factor potentiometer until output reads +2.500 volts ($K = \frac{1}{10}$).
6. Set $V_X = V_Y$ = -5.000 volts and note the output. The output should again be +2.500 volts. If the error is appreciable (greater than 1 or 2 percent), repeat steps 1 thru 6.

Procedure III (X-Y Plotter)

A. X-Y Offset Adjust

1. Connect X-Y plotter to multiplier.
2. Plot V_{out} versus V_Y ($V_X = \pm 10$ V, $-10 \leqslant V_Y \leqslant +10$ V) and V_{out} versus V_X ($V_Y = \pm 10$ V, -10 V $\leqslant V_X \leqslant +10$ V).
3. See example curves below for X offset, Y offset and output offset.





4. Adjust X and Y offset to bring the above values to zero.

B. Output Offset – See Procedure I-B for methods to bring output offset to zero

C. See Procedure I-C.

When a high degree of accuracy is unnecessary, the adjustment procedure can be simplified by eliminating the V_o offset adjust. This normally results in a small (percentage) error for large output voltages, but a larger (percentage) error near zero.

NOTE 8: Power Dissipation

Because this circuit has no direct positive power supply connections, power dissipation, (P_D), within the actual IC package should be calculated as the sum of the voltage-current products at each port (ignore base current).

Under normal operating conditions, it is valid to assume:

$$I_2 = I_{14} = I_{13},\ I_1 = 2 I_3, \text{ and } V_2 = V_{14}$$

then

$$P_D = 2\,(V_2 - V_7)\,I_{13} + 2\,(V_1 - V_7)\,I_3 + (V_{13} - V_7)\,I_{13} + (V_3 - V_7)\,I_3$$

For the circuit in Figure 1, calculate:

$$P_D = 2\,(36)\,(10^{-3}) + 2\,(29)\,(10^{-3}) + (1.2)\,(10^{-3}) + (1.2)\,(10^{-3}) = 133 \text{ mW}$$

NOTE 9: Bandwidth and Phase

Bandwidth is primarily determined by the load resistors and the stray multiplier output capacitance and/or the operational amplifier used to level shift the output. If wideband operation is desired, low value load resistors and/or a wideband op-amp should be used.

Phase shift in the multiplier circuit results from two sources: phase shift common to both X and Y channels (due to the load resistor-output capacitance pole mentioned above) and relative phase shift between X and Y channels (due to differences in transadmittance in the X and Y channels). If the input to output phase shift is only 0.6°, the output product of two sine waves will exhibit a vector error of 1%. A 3° relative phase shift between V_X and V_Y results in a vector error of 5%.

NOTE 10: General Design Procedure

The method used to calculate the element values for the first entry in the table in Figure 10 is given below. This will illustrate a general design procedure. For this example, the inputs, outputs and scale factor are:

$$V_{out} = V_X V_Y/10,\ -10 \text{ V} \leqslant V_X \leqslant +10 \text{ V}$$

$$-10 \text{ V} \leqslant V_Y \leqslant +10 \text{ V},\ K = 1/10$$

Design Procedure (See Figure 1):

a. Currents I_3 and I_{13} are chosen at a convenient value (observing power dissipation limitation) between 0.5 mA and 2.0 mA, approximately 1.0 mA. Then R_X and R_Y can be determined by considering the input signal handling requirements.

$$V_{X(max)} < I_{13} R_X$$

$$V_{Y(max)} < I_3 R_Y$$

For $V_{X(max)} = V_{Y(max)}$ = 10 volts;

$$R_X = R_Y > \frac{10 \text{ V}}{1.0 \text{ mA}} = 10 \text{ k}\Omega$$

In order to insure that $R_X >> \frac{kT}{qI_{13}}$ and $R_Y >> \frac{kT}{qI_3}$ even with maximum input voltage, let $R_X = R_Y$ = 15 kΩ (see Note 6b and Figure 8).

b. Then from Note 2 the scale factor is approximately:

$$K \approx \frac{2R_L}{I_3 R_X R_Y}$$

and R_L is established for K = 1/10:

$$R_L = \frac{K\, I_3\, R_X\, R_Y}{2} = \frac{(10^{-3})(15 \times 10^3)(15 \times 10^3)}{(10)\,(2)}$$

$$= 11.25\ \text{k}\Omega$$

Select R_L = 11 kΩ.

c. The supply voltages are now selected. From the curve in Figure 9, for an input swing of ±10 V, voltage V_1 may have a minimum value of +12 volts. (This minimum V_1 is approximately two forward diode drops above $V_{X\,max}$ and one diode drop above $V_{Y\,max}$.) With a 1.5 volt safety margin, V_1 becomes 13.5 V. This voltage can be supplied by a separate power supply or obtained by a dropping resistor, R_1, from the positive supply according to the equation:

$$R_1 = \frac{V^+ - V_1}{2I_3}$$

The positive supply is determined from:

$$V^+ = V_1 + \left[\frac{K V_{X\,max}\, V_{Y\,max}}{2}\right]$$

$$+ I_{13} R_L + 2\ \text{V (safety margin)}$$

$$= 13.5 + 5 + 11 + 2\ \text{V}$$

$$= 31.5\ \text{(select nominal +32 V supply)}$$

Now R_1 can be found:

$$R_1 = \frac{V^+ - V_1}{2I_3} = \frac{32 - 13.5}{(2)\,(1.0\ \text{mA})} = 9.25\ \text{k}\Omega$$

Select R_1 = 9.1 kΩ.

The negative supply should be selected so that with maximum positive input voltage applied, the maximum voltage between the input and the negative supply does not exceed the 30 V breakdown limit.

In addition, the negative supply should be at least two volts more negative than the most negative input voltage. For V_{in} max (negative) = -10 V, select V^- = -15 V.

d. The currents I_{13} and I_3 are set by means of dropping resistors from ground to pins 13 and 3 respectively, according to the equations.

$$R_{13} = \frac{V_7 - \phi}{I_{13}} - 500\Omega$$

where $\phi = V_{BE} = 0.75$ at 25°C.

$$\text{Similarly: } R_3 = \frac{V_7 - \phi}{I_3} - 500\Omega$$

for $I_{13} = I_3$, $R_3 = R_{13}$ = 13.75 kΩ

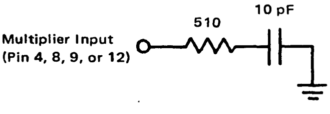
e. The common-mode voltage, V_{CM}, may be calculated from:

$$V_{CM} = V^+ - R_L I_{13} = 32 - 11 = 21\ \text{V}.$$

NOTE 11: Parasitic Oscillation

When long leads are used on the input, oscillation may occur. In this event, an R-C parasitic suppression network similar to the one shown below should be connected directly to each input using short leads. The purpose of the network is to reduce the Q of source-tuned circuits which cause the oscillation.

Another technique which is also adequate in most applications is to insert a 510Ω resistor in series with the multiplier inputs, pins 4, 8, 9, and 12.



6

TEST CIRCUITS

FIGURE 1 – TEST CIRCUIT FOR LINEARITY AND ACCURACY MEASUREMENT USING X-Y PLOTTER

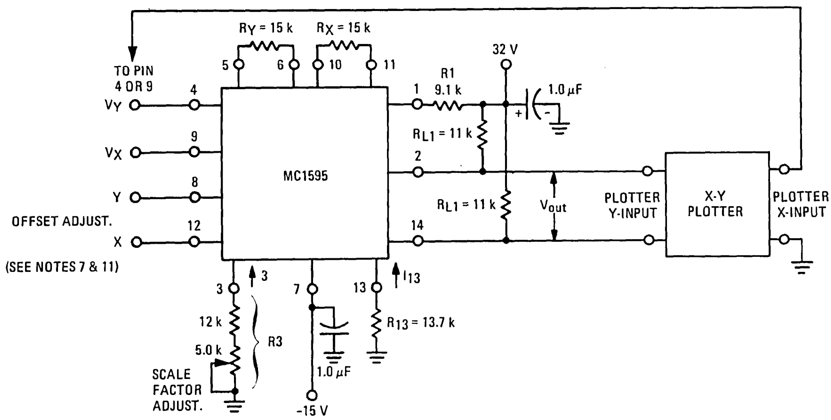


FIGURE 2 – INPUT RESISTANCE MEASUREMENT

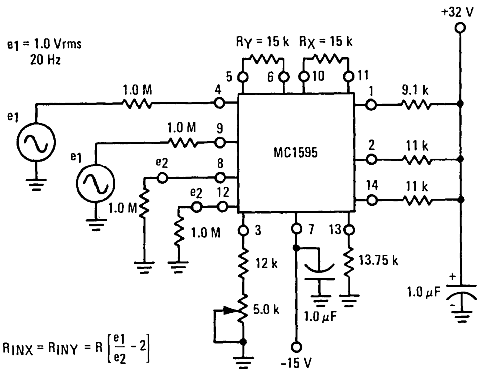


FIGURE 3 – OUTPUT RESISTANCE MEASUREMENT

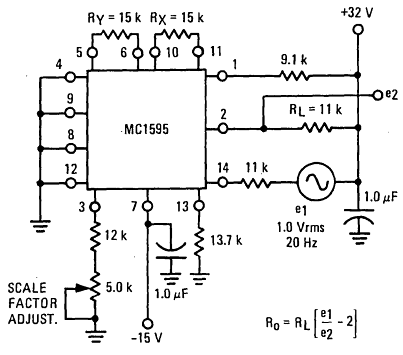


FIGURE 4 – INPUT AND OUTPUT CURRENT MEASUREMENT

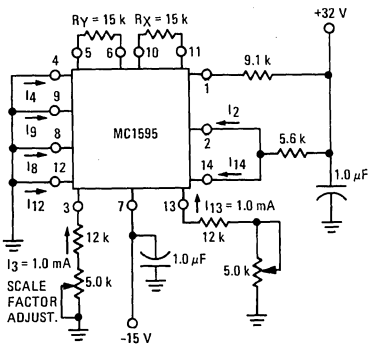
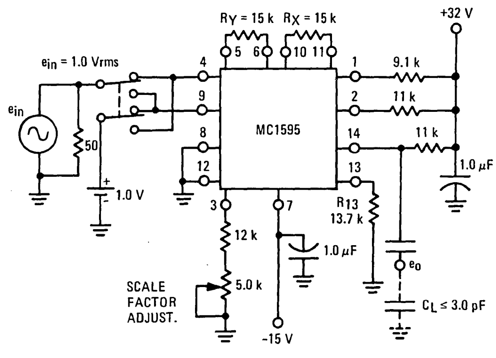


FIGURE 5 – BANDWIDTH MEASUREMENT



6

TEST CIRCUITS (Continued)

FIGURE 6 – COMMON MODE INPUT VOLTAGE AND GAIN MEASUREMENT

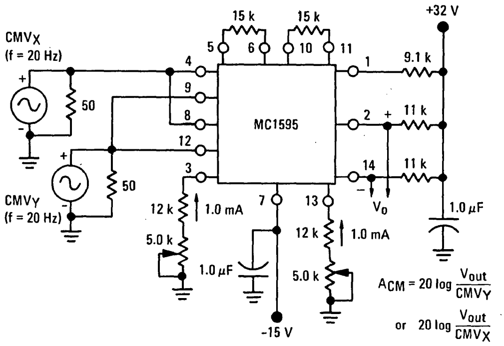
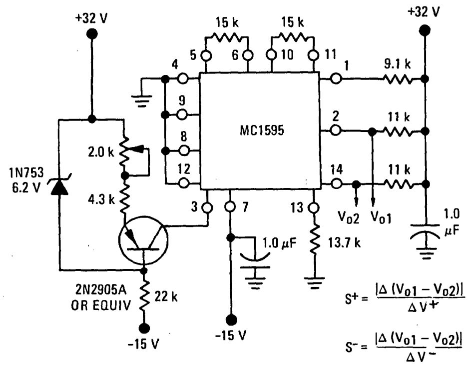


FIGURE 7 – POWER SUPPLY SENSITIVITY



TYPICAL CHARACTERISTICS

FIGURE 8A – ERROR CONTRIBUTED BY INPUT DIFFERENTIAL AMPLIFIER

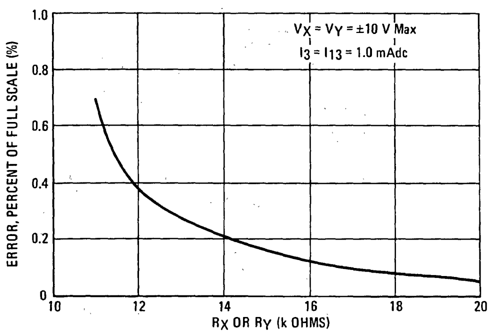


FIGURE 8B – ERROR CONTRIBUTED BY INPUT DIFFERENTIAL AMPLIFIER

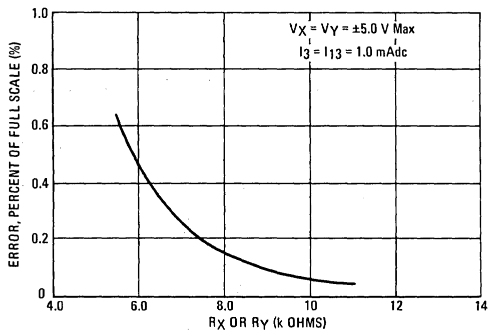
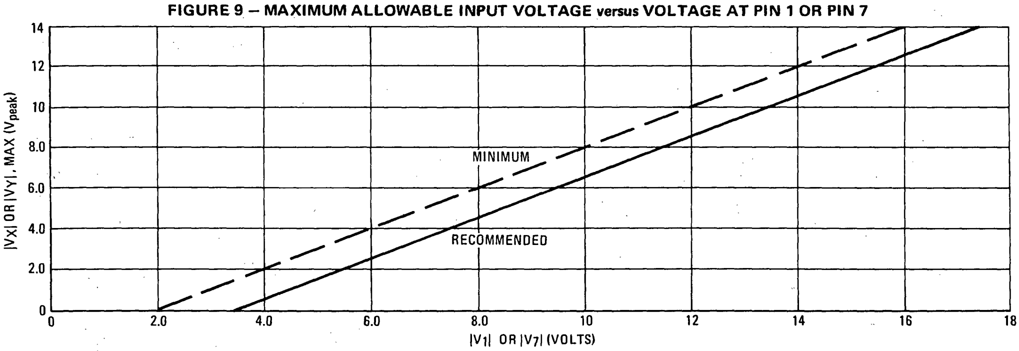
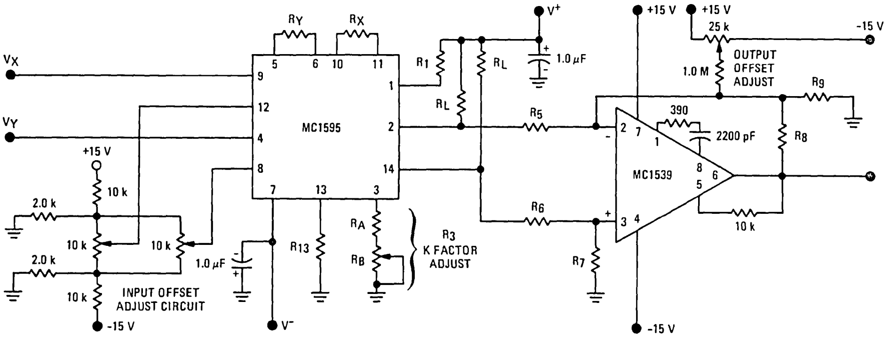


FIGURE 9 – MAXIMUM ALLOWABLE INPUT VOLTAGE versus VOLTAGE AT PIN 1 OR PIN 7



TYPICAL APPLICATIONS

FIGURE 10 – MULTIPLY WITH OP-AMP LEVEL SHIFT



RESISTOR	R_1	R_5	R_6	R_7	R_8	R_9	R_{13}	R_A	R_B	R_L	R_X	R_Y
UNIT	kΩ	kΩ	kΩ	kΩ	kΩ	kΩ	kΩ	kΩ	kΩ	kΩ	kΩ	kΩ
TOLERANCE	5%	1%	1%	1%	1%	1%	1%	5%	20%	0.5%	5%	5%
$V^+ = +32$ Vdc, $V^- = -15$ Vdc $-10\ V \le V_X \le +10\ V$, $10\ V \le V_Y \le +10\ V$	9.1	121	100	11	121	15	13.7	12	5.0	12	15	15
$V^+ = +15$ Vdc, $V^- = -15$ Vdc $-5\ V \le V_X \le +5\ V$, $-5\ V \le V_Y \le +5\ V$	3.0	300	100	100	300	∞	13.7	12	5.0	3.4	8.2	8.2

FIGURE 11 – MULTIPLY WITH OP-AMP LEVEL SHIFT

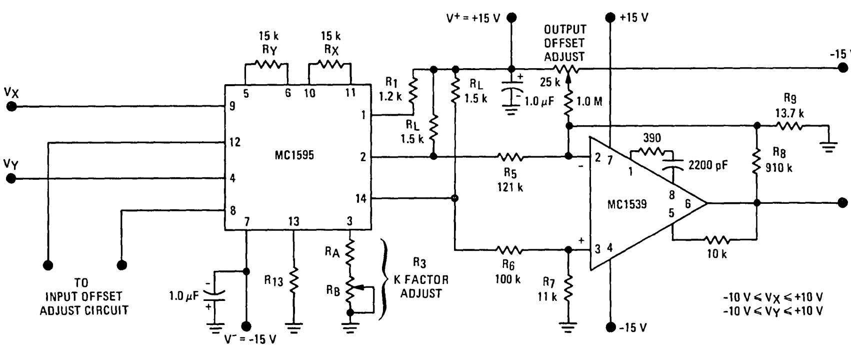
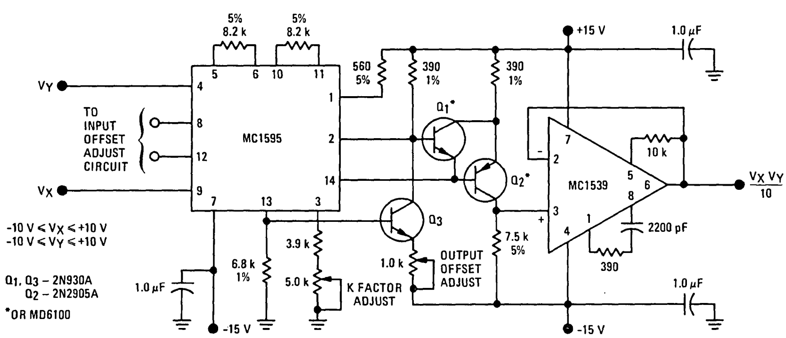


FIGURE 12 – MULTIPLY WITH DISCRETE LEVEL SHIFT



TYPICAL APPLICATIONS (continued)

FIGURE 13 – DIVIDE AND SQUARE ROOT

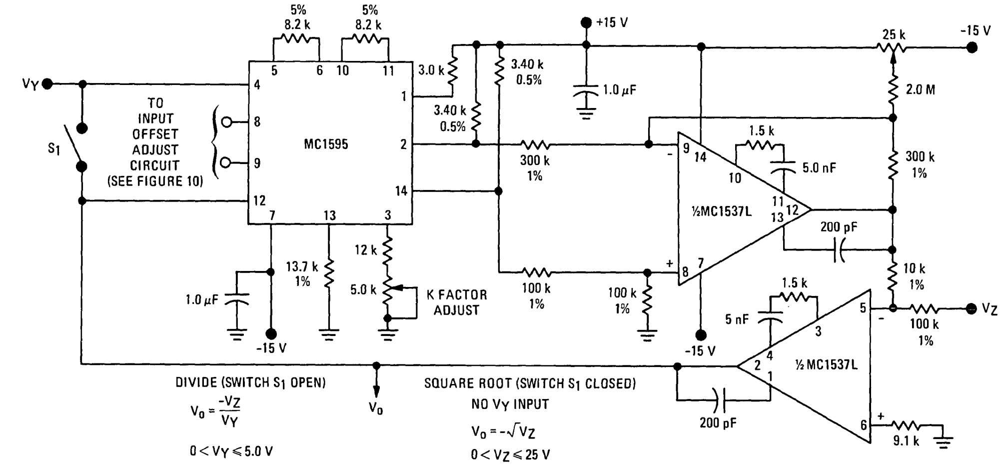


FIGURE 14 – FREQUENCY DOUBLER

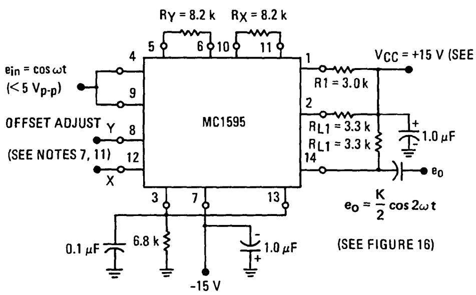
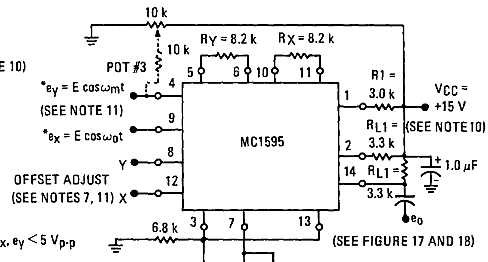


FIGURE 15 – BALANCED OR AMPLITUDE MODULATOR



BALANCED MODULATOR
(Pot #3 is not used)
1. Apply only e_y and adjust Pot #2 (Note 7) to null output.
2. Apply only e_x and adjust Pot #1 (Note 7) to null output.
3. Apply both e_y and e_x.

AMPLITUDE MODULATOR
1. Set up steps 1 thru 3 for balanced modulator.
2. Adjust Pot #3 until output is an amplitude modulated waveform. (See Figure 17)

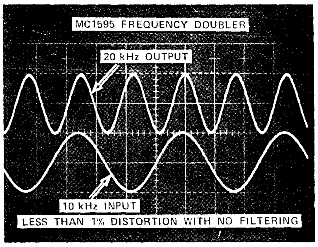


FIGURE 16 – FREQUENCY DOUBLER (OUTPUT WAVEFORM OF CIRCUIT SHOWN IN FIGURE 14)

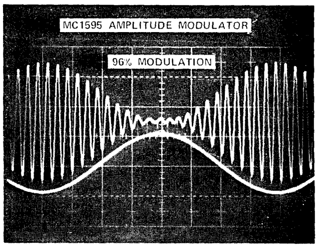


FIGURE 17 – AMPLITUDE MODULATOR (OUTPUT WAVEFORM OF CIRCUIT SHOWN IN FIGURE 15)

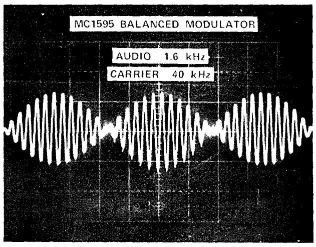


FIGURE 18 – BALANCED MODULATOR (OUTPUT WAVEFORM OF CIRCUIT SHOWN IN FIGURE 15)

6

Linear

MC1596
MC1496

BALANCED MODULATOR-DEMODULATOR

Specifications and Applications Information

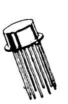
MONOLITHIC BALANCED MODULATOR – DEMODULATOR

. . . designed for use where the output voltage is a product of an input voltage (signal) and a switching function (carrier). Typical applications include suppressed carrier and amplitude modulation, synchronous detection, FM detection, phase detection, and chopper applications.

- Excellent Carrier Suppression – 65 dB typ @ 0.5 MHz
  – 50 dB typ @ 10 MHz
- Adjustable Gain and Signal Handling
- Balanced Inputs and Outputs
- High Common-Mode Rejection – 85 dB typ

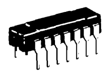
BALANCED MODULATOR – DEMODULATOR

INTEGRATED CIRCUIT SILICON EPITAXIAL PASSIVATED



Pin 10 electrically connected to case through substrate.

G SUFFIX
METAL PACKAGE
CASE 602A



Pin 14 electrically connected to substrate

L SUFFIX
CERAMIC PACKAGE
CASE 632 (TO-116)

FIGURE 1 – SUPPRESSED-CARRIER OUTPUT WAVEFORM

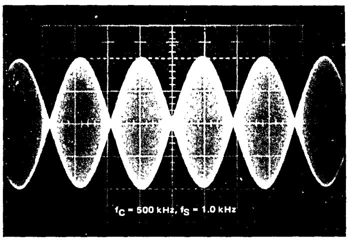


FIGURE 2 – AMPLITUDE-MODULATION OUTPUT WAVEFORM

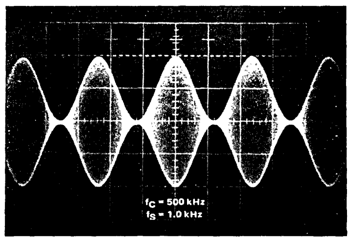


FIGURE 3 – SUPPRESSED-CARRIER SPECTRUM

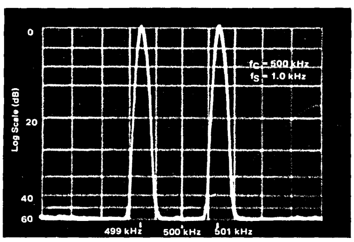


FIGURE 4 – AMPLITUDE-MODULATION SPECTRUM

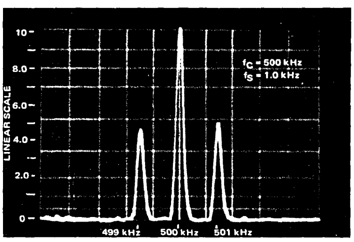
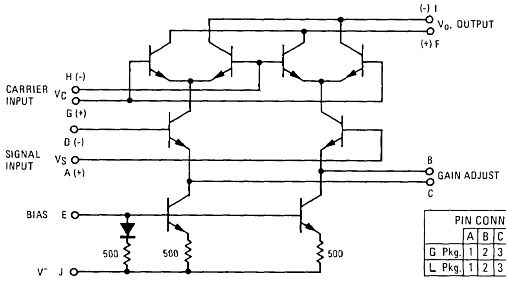
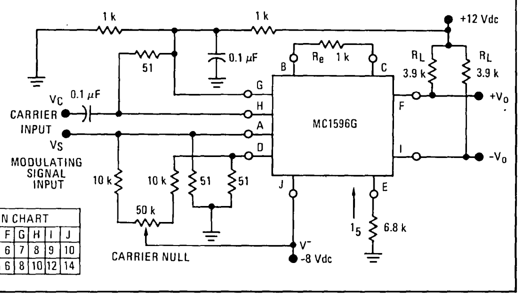


FIGURE 5 – CIRCUIT SCHEMATIC



PIN CONNECTION CHART	A	B	C	D	E	F	G	H	I	J
G Pkg.	1	2	3	4	5	6	7	8	9	10
L Pkg.	1	2	3	4	5	6	8	10	12	14

FIGURE 6 – TYPICAL MODULATOR CIRCUIT



See Packaging Information Section for outline dimensions.

MAXIMUM RATINGS* (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Applied Voltage ($V_6 - V_7, V_8 - V_1, V_9 - V_7, V_9 - V_8, V_7 - V_4, V_7 - V_1,$ $V_8 - V_4, V_6 - V_8, V_2 - V_5, V_3 - V_5$)	ΔV	30	Vdc
Differential Input Signal	$V_7 - V_8$ $V_4 - V_1$	+5.0 $\pm(5+I_5R_e)$	Vdc
Maximum Bias Current	I_5	10	mA
Power Dissipation (P[illegible]e Limitation) Ceramic Dual In-Line Package Derate above T_A = +25°C Metal Package Derate above T_A = +25°C	P_D	 575 3.85 680 4.6	 mW mW/°C mW mW/°C
Operating Temperature Range MC1496 MC1596	T_A	 0 to +70 -55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS* (V^+ = +12 Vdc, V^- = -8.0 Vdc, I_5 = 1.0 mAdc, R_L = 3.9 kΩ, R_e = 1.0 kΩ, T_A = +25°C unless otherwise noted) (All input and output characteristics are single-ended unless otherwise noted.)

				MC1596			MC1496			
Characteristic	Fig	Note	Symbol	Min	Typ	Max	Min	Typ	Max	Unit
Carrier Feedthrough	7	1	V_{CFT}							µV(rms)
V_C = 60 mV(rms) sine wave and offset adjusted to zero, f_C = 1.0 kHz				–	40	–	–	40	–	
f_C = 10 MHz				–	140	–	–	140	–	
V_C = 300 mVp-p square wave:										mV(rms)
offset adjusted to zero, f_C = 1.0 kHz				–	0.04	0.2	–	0.04	0.4	
offset not adjusted, f_C = 1.0 kHz				–	20	100	–	20	200	
Carrier Suppression f_S = 10 kHz, 300 mV(rms)	7	2	V_{CS}							dB
f_C = 500 kHz, 60 mV(rms) sine wave				50	65	–	40	65	–	
f_C = 10 MHz, 60 mV(rms) sine wave				–	50	–	–	50	–	k
Transadmittance Bandwidth (Magnitude) (R_L = 50 ohms)	10	8	BW_{3dB}							MHz
Carrier Input Port, V_C = 60 mV(rms) sine wave f_S = 1.0 kHz, 300 mV(rms) sine wave				–	300	–	–	300	–	
Signal Input Port, V_S = 300 mV(rms) sine wave $\|V_C\|$ = 0.5 Vdc				–	80	–	–	80	–	
Signal Gain V_S = 100 mV(rms), f = 1.0 kHz; $\|V_C\|$ = 0.5 Vdc	12	3	A_{VS}	2.5	3.5	–	2.5	3.5	–	V/V
Single-Ended Input Impedance, Signal Port, f = 5.0 MHz	8	–								
Parallel Input Resistance			r_{ip}	–	200	–	–	200	–	kΩ
Parallel Input Capacitance			c_{ip}	–	2.0	–	–	2.0	–	pF
Single-Ended Output Impedance, f = 10 MHz	8	–								
Parallel Output Resistance			r_{op}	–	40	–	–	40	–	kΩ
Parallel Output Capacitance			c_{op}	–	5.0	–	–	5.0	–	pF
Input Bias Current	9	–								µA
$I_{bS} = \frac{I_1 + I_4}{2}$; $I_{bC} = \frac{I_7 + I_8}{2}$			I_{bS}	–	12	25	–	12	30	
			I_{bC}	–	12	25	–	12	30	
Input Offset Current	9	–								µA
$I_{ioS} = I_1 - I_4$; $I_{ioC} = I_7 - I_8$			$\|I_{ioS}\|$	–	0.7	5.0	–	0.7	7.0	
			$\|I_{ioC}\|$	–	0.7	5.0	–	0.7	7.0	
Average Temperature Coefficient of Input Offset Current (T_A = -55°C to +125°C)	9	–	$\|TC_{Iio}\|$	–	2.0	–	–	2.0	–	nA/°C
Output Offset Current ($I_6 - I_9$)	9	–	$\|I_{oo}\|$	–	14	50	–	14	80	µA
Average Temperature Coefficient of Output Offset Current (T_A = -55°C to +125°C)	9	–	$\|TC_{Ioo}\|$	–	90	–	–	90	–	nA/°C
Common-Mode Input Swing, Signal Port, f_S = 1.0 kHz	11	4	CMV	–	5.0	–	–	5.0	–	Vp-p
Common-Mode Gain, Signal Port, f_S = 1.0 kHz, $\|V_C\|$ = 0.5 Vdc	11	–	ACM	–	-85	–	–	-85	–	dB
Common-Mode Quiescent Output Voltage (Pin 6 or Pin 9)	12	–	V_o	–	8.0	–	–	8.0	–	Vdc
Differential Output Voltage Swing Capability	12	–	V_{out}	–	8.0	–	–	8.0	–	Vp-p
Power Supply Current	9	6								mAdc
$I_6 + I_9$			I_D^+	–	2.0	3.0	–	2.0	4.0	
I_{10}			I_D^-	–	3.0	4.0	–	3.0	5.0	
DC Power Dissipation	9	5	P_D	–	33	–	–	33	–	mW

*Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for a ceramic packaged device refer to the PIN CONNECTION CHART on the first page of this specification.

GENERAL OPERATING INFORMATION *

Note 1 – Carrier Feedthrough

Carrier feedthrough is defined as the output voltage at carrier frequency with only the carrier applied (signal voltage = 0).

Carrier null is achieved by balancing the currents in the differential amplifier by means of a bias trim potentiometer (R_1 of Figure 7).

Note 2 – Carrier Suppression

Carrier suppression is defined as the ratio of each sideband output to carrier output for the carrier and signal voltage levels specified.

Carrier suppression is very dependent on carrier input level, as shown in Figure 24. A low value of the carrier does not fully switch the upper switching devices, and results in lower signal gain, hence lower carrier suppression. A higher than optimum carrier level results in unnecessary device and circuit carrier feedthrough, which again degenerates the suppression figure. The MC1596 has been characterized with a 60 mV(rms) sinewave carrier input signal. This level provides optimum carrier suppression at carrier frequencies in the vicinity of 500 kHz, and is generally recommended for balanced modulator applications.

Carrier feedthrough is independent of signal level, V_S. Thus carrier suppression can be maximized by operating with large signal levels. However, a linear operating mode must be maintained in the signal-input transistor pair – or harmonics of the modulating signal will be generated and appear in the device output as spurious sidebands of the suppressed carrier. This requirement places an upper limit on input-signal amplitude (see Note 3 and Figure 22). Note also that an optimum carrier level is recommended in Figure 24 for good carrier suppression and minimum spurious sideband generation.

At higher frequencies circuit layout is very important in order to minimize carrier feedthrough. Shielding may be necessary in order to prevent capacitive coupling between the carrier input leads and the output leads.

Note 3 – Signal Gain and Maximum Input Level

Signal gain (single-ended) at low frequencies is defined as the voltage gain,

$$A_{VS} = \frac{V_o}{V_S} = \frac{R_L}{R_e + 2r_e} \text{ where } r_e = \frac{26 \text{ mV}}{I_5 \text{ (mA)}}$$

A constant dc potential is applied to the carrier input terminals to fully switch two of the upper transistors "on" and two transistors "off" (V_C = 0.5 Vdc). This in effect forms a cascode differential amplifier.

Linear operation requires that the signal input be below a critical value determined by R_E and the bias current I_5

$$V_S \leq I_5 R_E \text{ (Volts peak)}$$

Note that in the test circuit of Figure 12, V_S corresponds to a maximum value of 1 volt peak.

Note 4 – Common-Mode Swing

The common-mode swing is the voltage which may be applied to both bases of the signal differential amplifier, without saturating the current sources or without saturating the differential amplifier itself by swinging it into the upper switching devices. This swing is variable depending on the particular circuit and biasing conditions chosen (see Note 6).

Note 5 – Power Dissipation

Power dissipation, P_D, within the integrated circuit package should be calculated as the summation of the voltage-current products at each port, i.e. assuming $V_9 = V_6$, $I_5 = I_6 = I_9$ and ignoring base current, $P_D = 2\ I_5\ (V_6 - V_{10}) + I_5\ (V_5 - V_{10})$ where subscripts refer to pin numbers.

Note 6 – Design Equations

The following is a partial list of design equations needed to operate the circuit with other supply voltages and input conditions. See Note 3 for R_e equation.

A. Operating Current

The internal bias currents are set by the conditions at pin 5. Assume:

$$I_5 = I_6 = I_9$$

$$I_B \ll I_C \text{ for all transistors}$$

then:

$$R_5 = \frac{V^- - \phi}{I_5} - 500\ \Omega$$

where: R_5 is the resistor between pin 5 and ground
ϕ = 0.75 V at T_A = +25°C

The MC1596 has been characterized for the condition I_5 = 1.0 mA and is the generally recommended value.

B. Common-Mode Quiescent Output Voltage

$$V_6 = V_9 = V^+ - I_5 R_L$$

Note 7 – Biasing

The MC1596 requires three dc bias voltage levels which must be set externally. Guidelines for setting up these three levels include maintaining at least 2 volts collector-base bias on all transistors while not exceeding the voltages given in the absolute maximum rating table;

$$30 \text{ Vdc} \geq [(V_6, V_9) - (V_7, V_8)] \geq 2 \text{ Vdc}$$

$$30 \text{ Vdc} \geq [(V_7, V_8) - (V_1, V_4)] \geq 2.7 \text{ Vdc}$$

$$30 \text{ Vdc} \geq [(V_1, V_4) - (V_5)] \geq 2.7 \text{ Vdc}$$

The foregoing conditions are based on the following approximations:

$$V_6 = V_9, \quad V_7 = V_8, \quad V_1 = V_4$$

Bias currents flowing into pins 1, 4, 7, and 8 are transistor base currents and can normally be neglected if external bias dividers are designed to carry 1.0 mA or more.

Note 8 – Transadmittance Bandwidth

Carrier transadmittance bandwidth is the 3-dB bandwidth of the device forward transadmittance as defined by:

$$y_{21C} = \left. \frac{i_o \text{ (each sideband)}}{v_s \text{ (signal)}} \right| V_o = 0$$

Signal transadmittance bandwidth is the 3-dB bandwidth of the device forward transadmittance as defined by:

$$y_{21S} = \left. \frac{i_o \text{ (signal)}}{v_s \text{ (signal)}} \right| V_c = 0.5 \text{ Vdc}, V_o = 0$$

*Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for a ceramic packaged device refer to the PIN CONNECTION CHART on the first page of this specification.

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Note 9 – Coupling and Bypass Capacitors C_1 and C_2

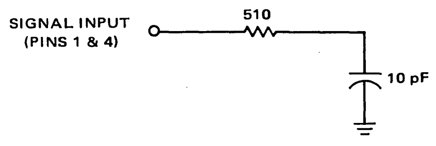
Capacitors C_1 and C_2 (Figure 7) should be selected for a reactance of less than 5.0 ohms at the carrier frequency.

Note 10 – Output Signal, V_o

The output signal is taken from pins 6 and 9, either balanced or single-ended. Figure 14 shows the output levels of each of the two output sidebands resulting from variations in both the carrier and modulating signal inputs with a single-ended output connection.

Note 11 – Signal Port Stability

Under certain values of driving source impedance, oscillation may occur. In this event, an RC suppression network should be connected directly to each input using short leads. This will reduce the Q of the source-tuned circuits that cause the oscillation.



An alternate method for low-frequency applications is to insert a 1 k-ohm resistor in series with the inputs, pins 1 and 4. In this case input current drift may cause serious degradation of carrier suppression.

TEST CIRCUITS

FIGURE 7 – CARRIER REJECTION AND SUPPRESSION

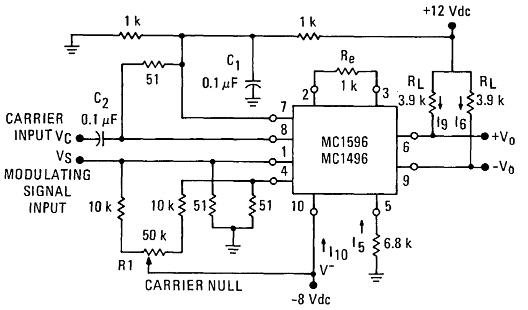


FIGURE 8 – INPUT-OUTPUT IMPEDANCE

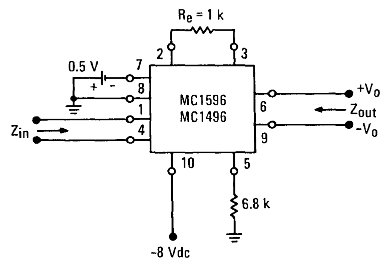


FIGURE 9 – BIAS AND OFFSET CURRENTS

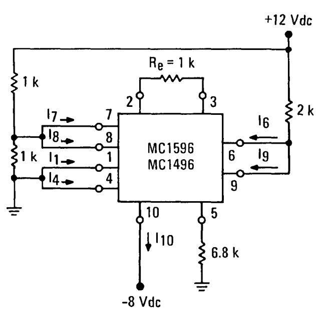
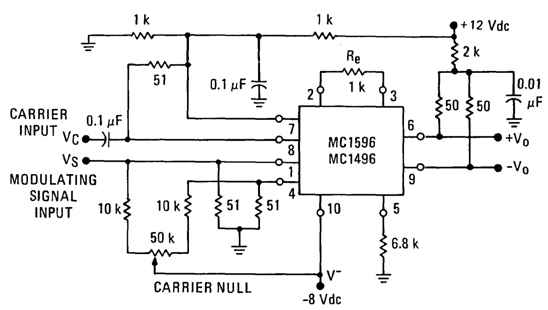


FIGURE 10 – TRANSCONDUCTANCE BANDWIDTH



Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for a ceramic packaged device refer to the PIN CONNECTION CHART on the first page of this specification.

TEST CIRCUITS (continued)

FIGURE 11 – COMMON-MODE GAIN

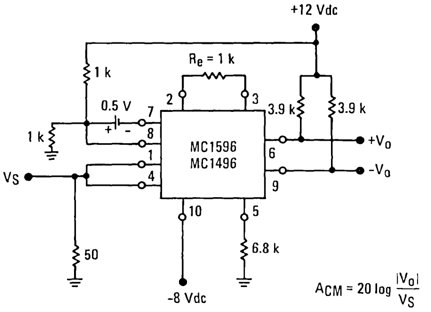
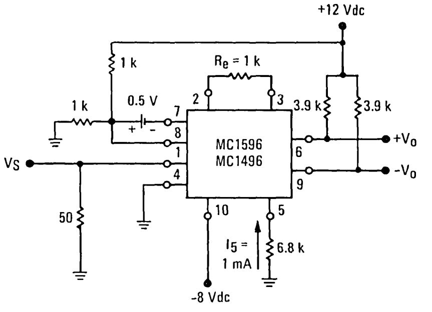


FIGURE 12 – SIGNAL GAIN AND OUTPUT SWING



Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for a ceramic packaged device refer to the PIN CONNECTION CHART on the first page of this specification.

TYPICAL CHARACTERISTICS

Typical characteristics were obtained with circuit shown in Figure 7, f_C = 500 kHz (sine wave), V_C = 60 mV(rms), f_S = 1 kHz, V_S = 300 mV(rms), T_A = +25°C unless otherwise noted.

FIGURE 13 – SIDEBAND OUTPUT versus CARRIER LEVELS

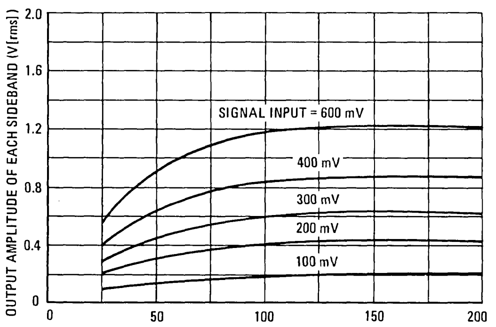


FIGURE 14 – SIGNAL-PORT PARALLEL-EQUIVALENT INPUT RESISTANCE versus FREQUENCY

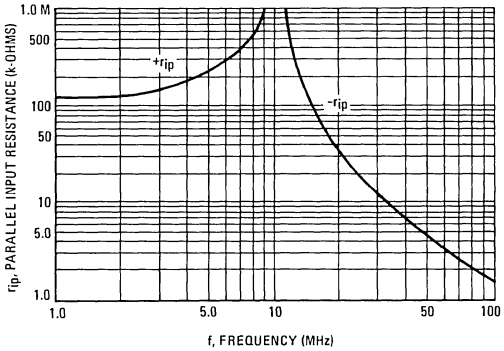


FIGURE 15 – SIGNAL-PORT PARALLEL-EQUIVALENT INPUT CAPACITANCE versus FREQUENCY

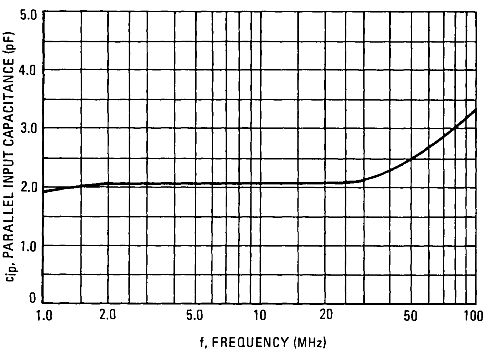
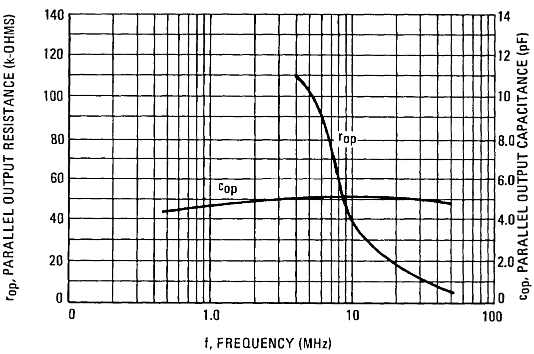


FIGURE 16 – SINGLE-ENDED OUTPUT IMPEDANCE versus FREQUENCY



TYPICAL CHARACTERISTICS (continued)

Typical characteristics were obtained with circuit shown in Figure 7, f_C = 500 kHz (sine wave), V_C = 60 mV(rms), f_S = 1 kHz, V_S = 300 mV(rms), T_A = +25°C unless otherwise noted.

FIGURE 17 – SIDEBAND AND SIGNAL PORT TRANSADMITTANCES versus FREQUENCY

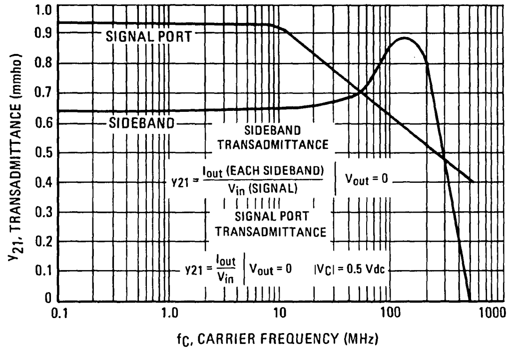


FIGURE 18 – CARRIER SUPPRESSION versus TEMPERATURE

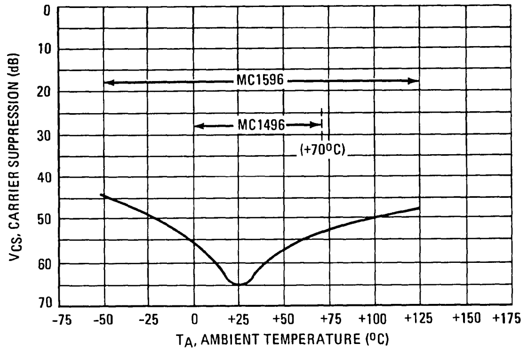


FIGURE 19 – SIGNAL-PORT FREQUENCY RESPONSE

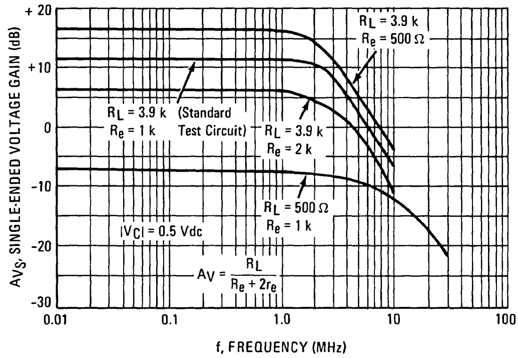


FIGURE 20 – CARRIER SUPPRESSION versus FREQUENCY

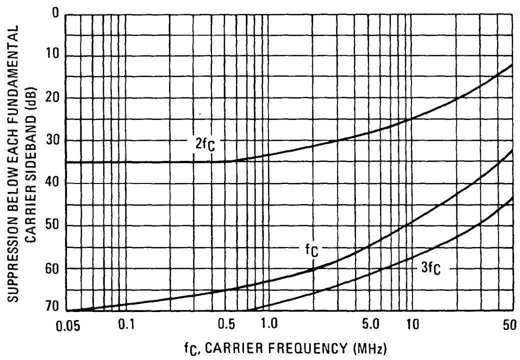


FIGURE 21 – CARRIER FEEDTHROUGH versus FREQUENCY

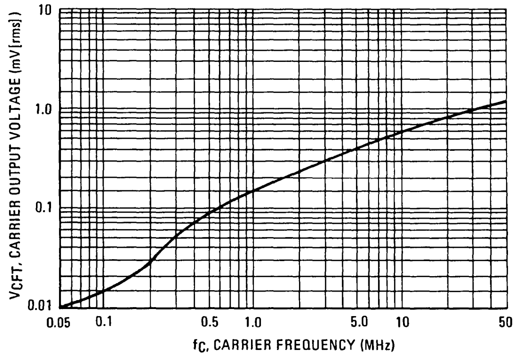
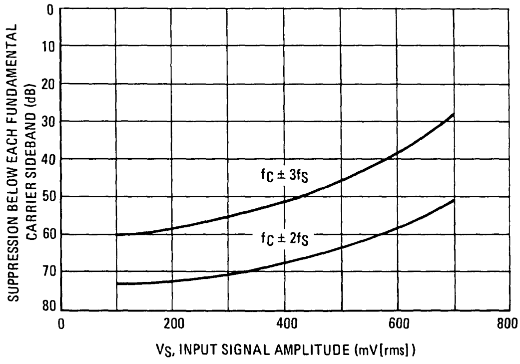


FIGURE 22 – SIDEBAND HARMONIC SUPPRESSION versus INPUT SIGNAL LEVEL



TYPICAL CHARACTERISTICS (continued)

FIGURE 23 – SUPPRESSION OF CARRIER HARMONIC SIDEBANDS versus CARRIER FREQUENCY

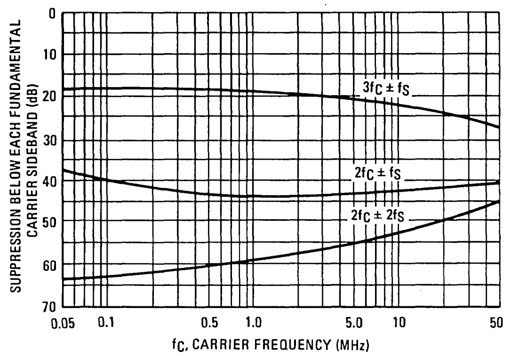
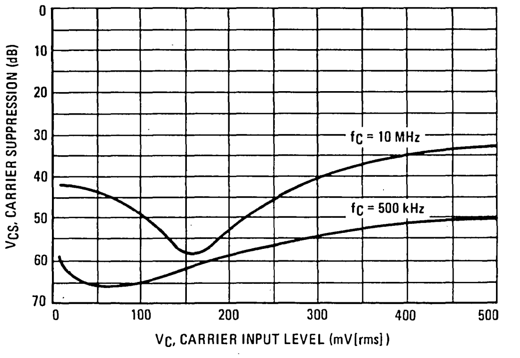


FIGURE 24 – CARRIER SUPPRESSION versus CARRIER INPUT LEVEL



OPERATIONS INFORMATION

The MC1596/MC1496, a monolithic balanced modulator circuit, is shown in Figure 5.

This circuit consists of an upper quad differential amplifier driven by a standard differential amplifier with dual current sources. The output collectors are cross-coupled so that full-wave balanced multiplication of the two input voltages occurs. That is, the output signal is a constant times the product of the two input signals.

Mathematical analysis of linear ac signal multiplication indicates that the output spectrum will consist of only the sum and difference of the two input frequencies. Thus, the device may be used as a balanced modulator, doubly balanced mixer, product detector, frequency doubler, and other applications requiring these particular output signal characteristics.

The lower differential amplifier has its emitters connected to the package pins so that an external emitter resistance may be used. Also, external load resistors are employed at the device output.

The upper quad differential amplifier may be operated either in a linear or a saturated mode. The lower differential amplifier is operated in a linear mode for most applications.

For low-level operation at both input ports, the output signal will contain sum and difference frequency components and have an amplitude which is a function of the product of the input signal amplitudes.

For high-level operation at the carrier input port and linear operation at the modulating signal port, the output signal will contain sum and difference frequency components of the modulating signal frequency and the fundamental and odd harmonics of the carrier frequency. The output amplitude will be a constant times the modulating signal amplitude. Any amplitude variations in the carrier signal will not appear in the output.

The linear signal handling capabilities of a differential amplifier are well defined. With no emitter degeneration, the maximum input voltage for linear operation is approximately 25 mV peak. Since the upper differential amplifier has its emitters internally connected, this voltage applies to the carrier input port for all conditions.

Since the lower differential amplifier has provisions for an external emitter resistance, its linear signal handling range may be adjusted by the user. The maximum input voltage for linear operation may be approximated from the following expression:

$$V = (I_5)(R_E) \text{ volts peak.}$$

This expression may be used to compute the minimum value of R_E for a given input voltage amplitude.

The gain from the modulating signal input port to the output is the MC1596/MC1496 gain parameter which is most often of interest to the designer. This gain has significance only when the lower differential amplifier is operated in a linear mode, but this includes most applications of the device.

As previously mentioned, the upper quad differential amplifier may be operated either in a linear or a saturated mode. Approximate gain expressions have been developed for the MC1596/MC1496 for a low-level modulating signal input and the following carrier input conditions:

1) Low-level dc
2) High-level dc
3) Low-level ac
4) High-level ac

These gains are summarized in Table 1, along with the frequency components contained in the output signal.

Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for a ceramic packaged device refer to the PIN CONNECTION CHART on the first page of this specification.

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OPERATIONS INFORMATION (continued)

FIGURE 25 – TABLE 1
VOLTAGE GAIN AND OUTPUT FREQUENCIES

Carrier Input Signal (V_C)	Approximate Voltage Gain	Output Signal Frequency(s)
Low-level dc	$\dfrac{R_L V_C}{2(R_E + 2r_e)\left(\frac{KT}{q}\right)}$	f_M
High-level dc	$\dfrac{R_L}{R_E + 2r_e}$	f_M
Low-level ac	$\dfrac{R_L V_C(\mathrm{rms})}{2\sqrt{2}\left(\frac{KT}{q}\right)(R_E + 2r_e)}$	$f_C \pm f_M$
High-level ac	$\dfrac{0.637\, R_L}{R_E + 2r_e}$	$f_C \pm f_M$, $3f_C \pm f_M$, $5f_C \pm f_M$, . . .

NOTES:
1. Low-level Modulating Signal, V_M, assumed in all cases. V_C is Carrier Input Voltage.
2. When the output signal contains multiple frequencies, the gain expression given is for the output amplitude of each of the two desired outputs, $f_C + f_M$ and $f_C - f_M$.
3. All gain expressions are for a single-ended output. For a differential output connection, multiply each expression by two.
4. R_L = Load resistance.
5. R_E = Emitter resistance between pins 2 and 3.
6. r_e = Transistor dynamic emitter resistance, at $+25^{\circ}C$;

$$r_e \approx \frac{26\ \mathrm{mV}}{I_5\ (\mathrm{mA})}$$

7. K = Boltzmann's Constant, T = temperature in degrees Kelvin, q = the charge on an electron.

$$\frac{KT}{q} \approx 26\ \mathrm{mV}\ \text{at room temperature.}$$

APPLICATION INFORMATION

Double sideband suppressed carrier modulation is the basic application of the MC1596/MC1496. The suggested circuit for this application is shown on the front page of this data sheet.

In some applications, it may be necessary to operate the MC1596/MC1496 with a single dc supply voltage instead of dual supplies. Figure 26 shows a balanced modulator designed for operation with a single +12 Vdc supply. Performance of this circuit is similar to that of the dual supply modulator.

AM Modulator

The circuit shown in Figure 27 may be used as an amplitude modulator with a minor modification.

All that is required to shift from suppressed carrier to AM operation is to adjust the carrier null potentiometer for the proper amount of carrier insertion in the output signal.

However, the suppressed carrier null circuitry as shown in Figure 27 does not have sufficient adjustment range. Therefore, the modulator may be modified for AM operation by changing two resistor values in the null circuit as shown in Figure 28.

Product Detector

The MC1596/MC1496 makes an excellent SSB product detector (see Figure 29).

This product detector has a sensitivity of 3.0 microvolts and a dynamic range of 90 dB when operating at an intermediate frequency of 9 MHz.

The detector is broadband for the entire high frequency range. For operation at very low intermediate frequencies down to 50 kHz the 0.1 μF capacitors on pins 7 and 8 should be increased to 1.0 μF. Also, the output filter at pin 9 can be tailored to a specific intermediate frequency and audio amplifier input impedance.

As in all applications of the MC1596/MC1496, the emitter resistance between pins 2 and 3 may be increased or decreased to adjust circuit gain, sensitivity, and dynamic range.

This circuit may also be used as an AM detector by introducing carrier signal at the carrier input and an AM signal at the SSB input.

The carrier signal may be derived from the intermediate frequency signal or generated locally. The carrier signal may be introduced with or without modulation, provided its level is sufficiently high to saturate the upper quad differential amplifier. If the carrier signal is modulated, a 300 mV(rms) input level is recommended.

Doubly Balanced Mixer

The MC1596/MC1496 may be used as a doubly balanced mixer with either broadband or tuned narrow band input and output networks.

The local oscillator signal is introduced at the carrier input port with a recommended amplitude of 100 mV(rms).

Figure 30 shows a mixer with a broadband input and a tuned output.

Frequency Doubler

The MC1596/MC1496 will operate as a frequency doubler by introducing the same frequency at both input ports.

Figures 31 and 32 show a broadband frequency doubler and a tuned output very high frequency (VHF) doubler, respectively.

Phase Detection and FM Detection

The MC1596/MC1496 will function as a phase detector. High-level input signals are introduced at both inputs. When both inputs are at the same frequency the MC1596/MC1496 will deliver an output which is a function of the phase difference between the two input signals.

An FM detector may be constructed by using the phase detector principle. A tuned circuit is added at one of the inputs to cause the two input signals to vary in phase as a function of frequency. The MC1596/MC1496 will then provide an output which is a function of the input signal frequency.

Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for a ceramic packaged device refer to the PIN CONNECTION CHART on the first page of this specification.

TYPICAL APPLICATIONS

FIGURE 26 – BALANCED MODULATOR (+12 Vdc SINGLE SUPPLY)

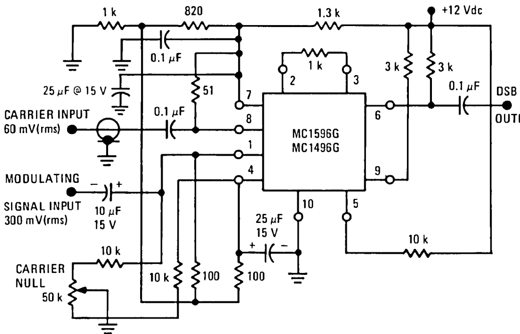


FIGURE 27 – BALANCED MODULATOR-DEMODULATOR

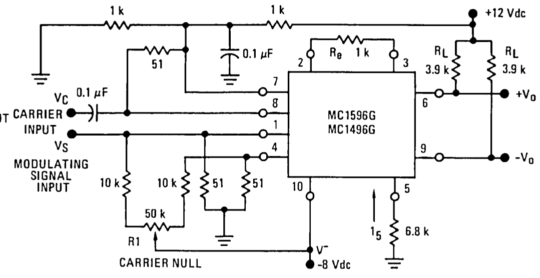


FIGURE 28 – AM MODULATOR CIRCUIT

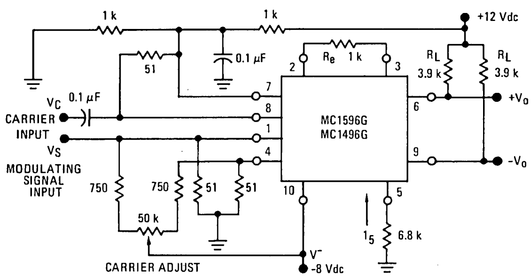


FIGURE 29 – PRODUCT DETECTOR (+12 Vdc SINGLE SUPPLY)

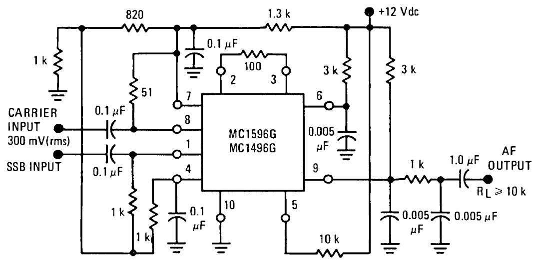
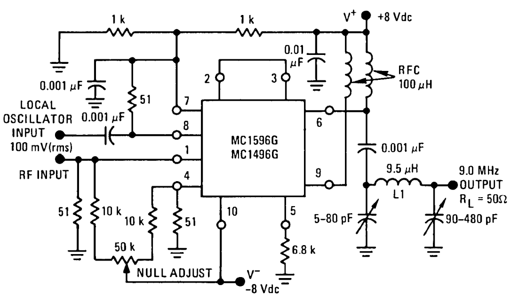
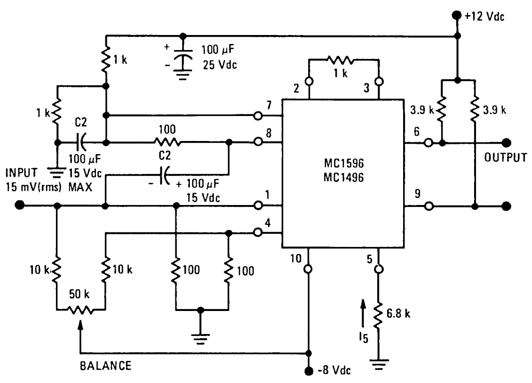


FIGURE 30 – DOUBLY BALANCED MIXER (BROADBAND INPUTS, 9.0 MHz TUNED OUTPUT)



L1 = 44 TURNS AWG NO. 28 ENAMELED WIRE, WOUND ON MICROMETALS TYPE 44-6 TOROID CORE.

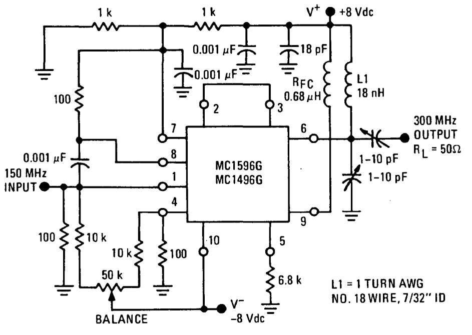
FIGURE 31 – LOW-FREQUENCY DOUBLER



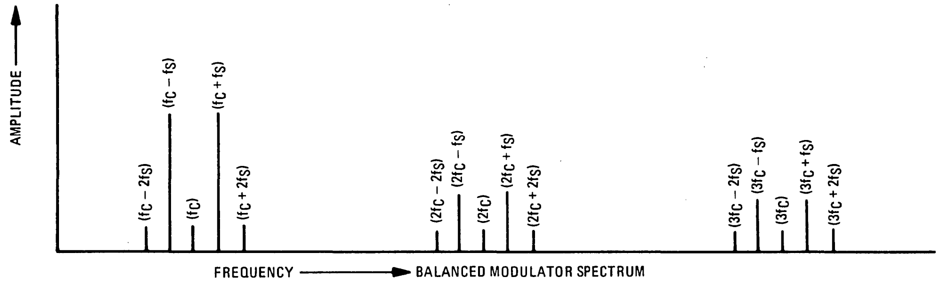
Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for a ceramic packaged device refer to the PIN CONNECTION CHART on the first page of this specification.

TYPICAL APPLICATIONS (continued)

FIGURE 32 – 150 to 300 MHz DOUBLER



DEFINITIONS

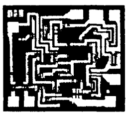


f_C	CARRIER FUNDAMENTAL	$f_C \pm nf_S$	FUNDAMENTAL CARRIER SIDEBAND HARMONICS
f_S	MODULATING SIGNAL	nf_C	CARRIER HARMONICS
$f_C \pm f_S$	FUNDAMENTAL CARRIER SIDEBANDS	$nf_C \pm nf_S$	CARRIER HARMONIC SIDEBANDS

MC1709
MC1709C

OPERATIONAL AMPLIFIERS

MONOLITHIC OPERATIONAL AMPLIFIER

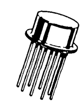


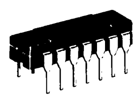
. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

- High-Performance Open Loop Gain Characteristics
  A_{VOL} = 45,000 typical
- Low Temperature Drift – ±3.0 μV/°C
- Large Output Voltage Swing – ±14 V typical @ ±15 V Supply
- Low Output Impedance – Z_{out} = 150 ohms typical

OPERATIONAL AMPLIFIER INTEGRATED CIRCUIT
MONOLITHIC SILICON

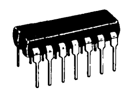
G SUFFIX
METAL PACKAGE
CASE 601
TO-99

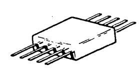




L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

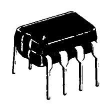
P2 SUFFIX
PLASTIC PACKAGE
CASE 605
TO-116
(MC1709C only)





F SUFFIX
CERAMIC PACKAGE
CASE 606
TO-91

P1 SUFFIX
PLASTIC PACKAGE
CASE 626
(MC1709C only)



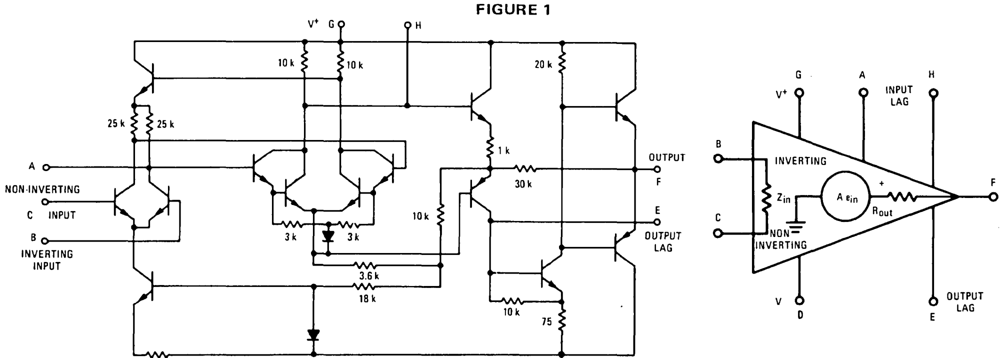
PIN CONNECTIONS

Schematic	A	B	C	D	E	F	G	H
"G" & "P1" Packages	1	2	3	4	5	6	7	8
"F" Package	2	3	4	5	6	7	8	9
"P2" & "L" Packages	3	4	5	6	9	10	11	12

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+ V^-	+18 -18	Vdc
Differential Input Signal	V_{in}	±5.0	Volts
Common Mode Input Swing	CMV_{in}	$\pm V^+$	Volts
Load Current	I_L	10	mA
Output Short Circuit Duration	t_S	5.0	s
Power Dissipation (Package Limitation) Metal Can Derate above T_A = +25°C Flat Package Derate above T_A = +25°C Plastic Dual In-Line Packages Derate above T_A = +25°C Ceramic Dual In-Line Package Derate above T_A = +25°C	P_D	 680 4.6 500 3.3 625 5.0 750 6.0	 mW mW/°C mW mW/°C mW mW/°C mW mW/°C
Operating Temperature Range MC1709 MC1709C	T_A	-55 to +125 0 to +75	°C
Storage Temperature Range Metal and Ceramic Packages Plastic Packages	T_{stg}	 -65 to +150 -55 to +125	°C

FIGURE 1



CIRCUIT SCHEMATIC

EQUIVALENT CIRCUIT

See Packaging Information Section for outline dimensions.

ELECTRICAL CHARACTERISTICS (V^+ = +15 Vdc, V^- = −15 Vdc, T_A = +25°C unless otherwise noted)

Characteristic	Symbol	MC1709			MC1709C			Unit
		Min	Typ	Max	Min	Typ	Max	
Open Loop Voltage Gain (R_L = 2.0 kΩ) (V_O = ±10 V, T_A = T_{low} to T_{high}) ②	A_{VOL}	25,000	45,000	70,000	15,000	45,000	–	–
Output Impedance (f = 20 Hz)	Z_{out}	–	150	–	–	150	–	Ω
Input Impedance (f = 20 Hz)	Z_{in}	150	400	–	50	250	–	kΩ
Output Voltage Swing (R_L = 10 kΩ) (R_L = 2.0 kΩ)	V_O	±12 ±10	±14 ±13	– –	±12 ±10	±14 ±13	– –	V_{peak}
Input Common-Mode Voltage Swing	CMV_{in}	±8	±10	–	±8.0	±10	–	V_{peak}
Common-Mode Rejection Ratio (f = 20 Hz)	CM_{rej}	70	90	–	65	90	–	dB
Input Bias Current (T_A = +25°C) (T_A = T_{low})	I_b	– –	0.2 0.5	0.5 1.5	– –	0.3 –	1.5 2.0	μA
Input Offset Current (T_A = +25°C) (T_A = T_{low}) (T_A = T_{high})	$\|I_{io}\|$	– – –	0.05 – –	0.2 0.5 0.2	– – –	0.1 – –	0.5 0.75 0.75	μA
Input Offset Voltage (T_A = +25°C) (T_A = T_{low} to T_{high})	$\|V_{io}\|$	– –	1.0 –	5.0 6.0	– –	2.0 –	7.5 10	mV
Step Response Gain = 100, 5.0% overshoot, R_1 = 1.0 kΩ, R_2 = 100 kΩ, R_3 = 1.5 kΩ, C_1 = 100 pF, C_2 = 3.0 pF	t_f t_{pd} dV_{out}/dt ①	– – –	0.8 0.38 12	– – –	– – –	0.8 0.38 12	– – –	μs μs V/μs
Gain = 10, 10% overshoot, R_1 = 1.0 kΩ, R_2 = 10 kΩ, R_3 = 1.5 kΩ, C_1 = 500 pF, C_2 = 20 pF	t_f t_{pd} dV_{out}/dt ①	– – –	0.6 0.34 1.7	– – –	– – –	0.6 0.34 1.7	– – –	μs μs V/μs
Gain = 1, 5.0% overshoot, R_1 = 10 kΩ, R_2 = 10 kΩ, R_3 = 1.5 kΩ, C_1 = 5000 pF, C_2 = 200 pF	t_f t_{pd} dV_{out}/dt ①	– – –	2.2 1.3 0.25	– – –	– – –	2.2 1.3 0.25	– – –	μs μs V/μs
Average Temperature Coefficient of Input Offset Voltage (R_S = 50 Ω, T_A = T_{low} to T_{high}) (R_S ≤ 10 kΩ, T_A = T_{low} to T_{high})	$\|TC_{Vio}\|$	– –	3.0 6.0	– –	– –	3.0 6.0	– –	μV/°C
DC Power Dissipation (Power Supply = ±15 V, V_O = 0)	P_D	–	80	165	–	80	200	mW
Positive Supply Sensitivity (V^- constant)	S^+	–	25	150	–	25	200	μV/V
Negative Supply Sensitivity (V^+ constant)	S^-	–	25	150	–	25	200	μV/V

① dV_{out}/dt = Slew Rate

② T_{high} = +75°C for MC1709C, +125°C for MC1709 T_{low} = 0°C for MC1709C, −55°C for MC1709

TYPICAL CHARACTERISTICS

FIGURE 2 – TEST CIRCUIT
V^+ = +15 Vdc, V^- = −15 Vdc, T_A = +25°C

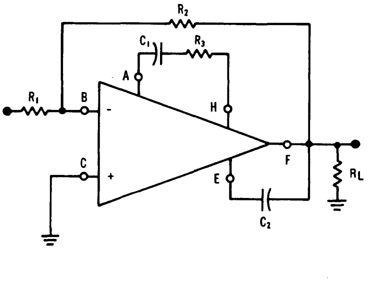


Fig. No.	Curve No.	Test Conditions				
		R_1 (Ω)	R_2 (Ω)	R_3 (Ω)	C_1 (pF)	C_2 (pF)
3	1	10 k	10 k	1.5 k	5.0 k	200
	2	10 k	100 k	1.5 k	500	20
	3	10 k	1.0 M	1.5 k	100	3.0
	4	1.0 k	1.0 M	0	10	3.0
4	1	1.0 k	1.0 M	0	10	3.0
	2	10 k	1.0 M	1.5 k	100	3.0
	3	10 k	100 k	1.5 k	500	20
	4	10 k	10 k	1.5 k	5.0 k	200
5	1	0	∞	1.5 k	5.0 k	200
	2	0	∞	1.5 k	500	20
	3	0	∞	1.5 k	100	3.0
	4	0	∞	0	10	3.0

TYPICAL CHARACTERISTICS (continued)

(V^+ = +15 Vdc, V^- = -15 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 3 – LARGE SIGNAL SWING versus FREQUENCY

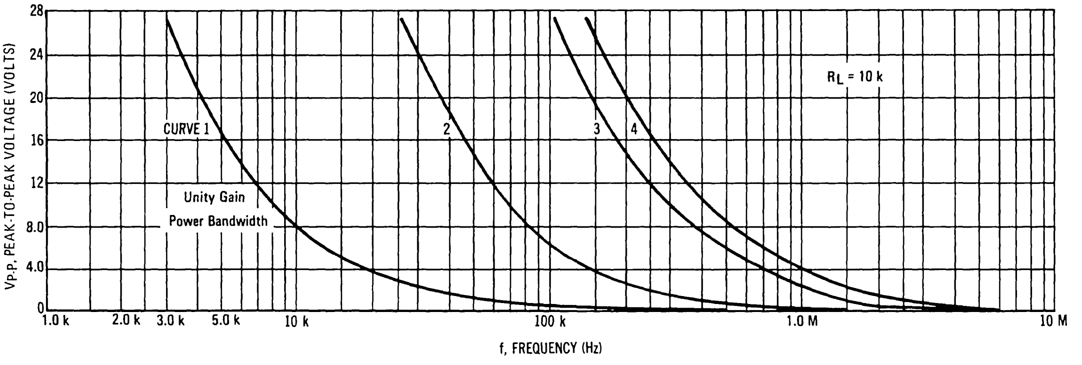


FIGURE 4 – VOLTAGE GAIN versus FREQUENCY

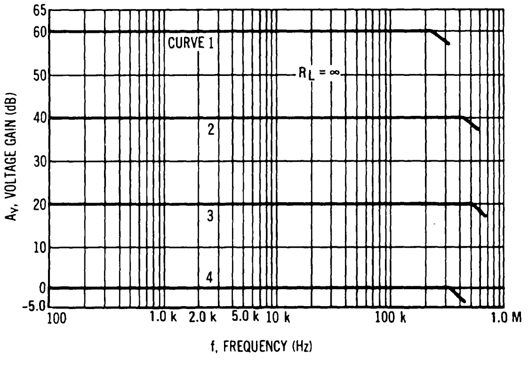


FIGURE 5 – OPEN LOOP VOLTAGE GAIN versus FREQUENCY

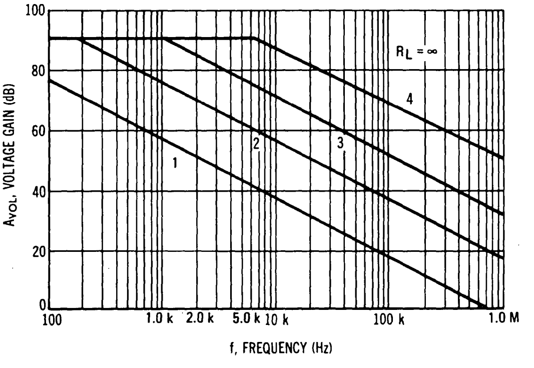


FIGURE 6 – VOLTAGE GAIN versus POWER SUPPLY VOLTAGE

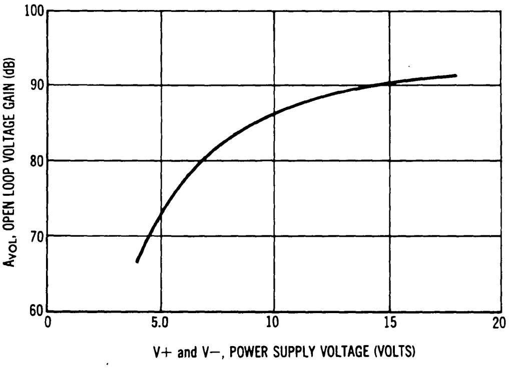
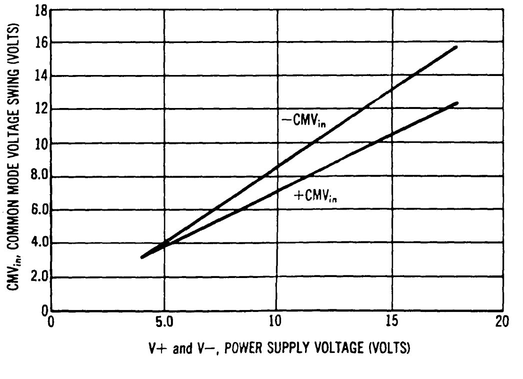


FIGURE 7 – COMMON SWING versus POWER SUPPLY VOLTAGE



TYPICAL CHARACTERISTICS (continued)

(V^+ = +15 Vdc, V^- = −15 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 8 – POWER DISSIPATION versus POWER SUPPLY VOLTAGE

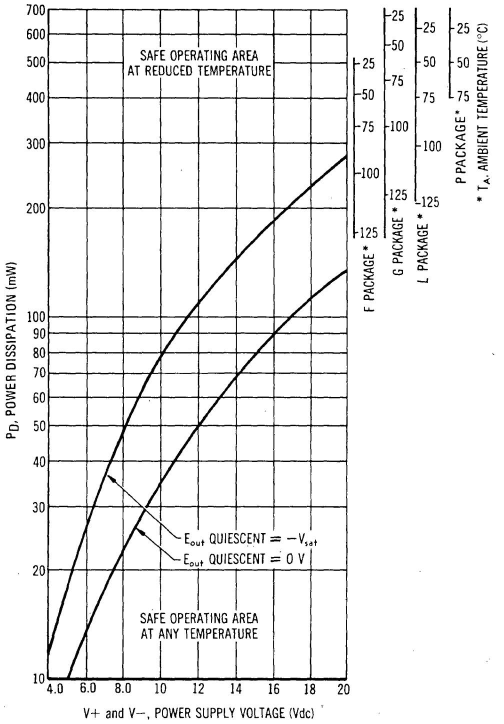


FIGURE 9 – INPUT OFFSET VOLTAGE versus TEMPERATURE

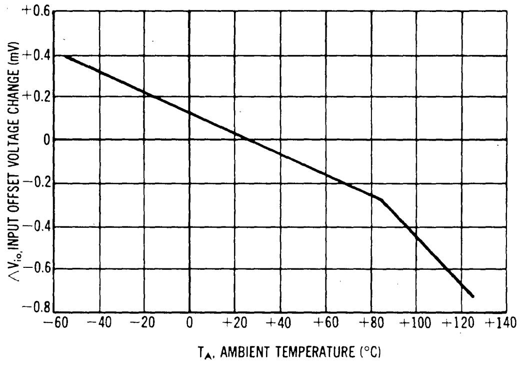
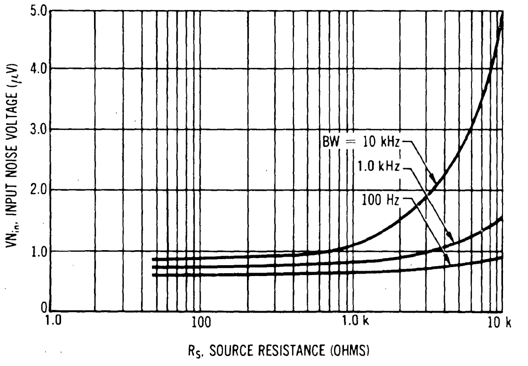


FIGURE 10 – INPUT NOISE VOLTAGE versus SOURCE RESISTANCE



See current MCC1709/1709C data sheet for standard linear chip information.
See current MCBC1709/MCB1709F data sheet for Beam-Lead device information.

MC1710

DIFFERENTIAL COMPARATOR

MONOLITHIC DIFFERENTIAL VOLTAGE COMPARATOR

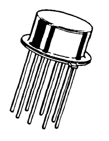
. . . designed for use in level detection, low-level sensing, and memory applications.

- Differential Input Characteristics –
  Input Offset Voltage = 1.0 mV
  Offset Voltage Drift = 3.0 $\mu V/^{o}C$
- Fast Response Time – 40 ns
- Output Compatible With All Saturating Logic Forms –
  V_{out} = +3.2 V to -0.5 V typical
- Low Output Impedance – 200 ohms

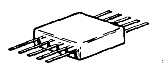
DIFFERENTIAL COMPARATOR INTEGRATED CIRCUIT

MONOLITHIC SILICON EPITAXIAL PASSIVATED

Lead 4 connected to case



G SUFFIX
METAL PACKAGE
CASE 601
TO-99



F SUFFIX
CERAMIC PACKAGE
CASE 606
TO-91

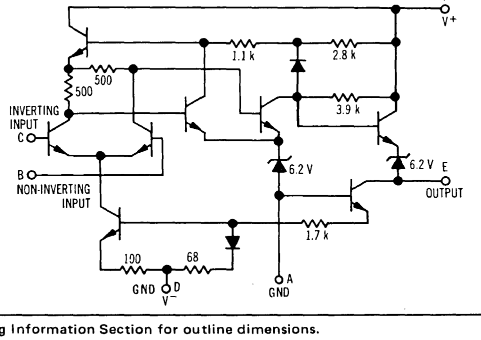
PIN CONNECTIONS

Schematic	A	B	C	D	E	F
"G" Package	1	2	3	4	7	8
"F" Package	1	2	3	5	6	8

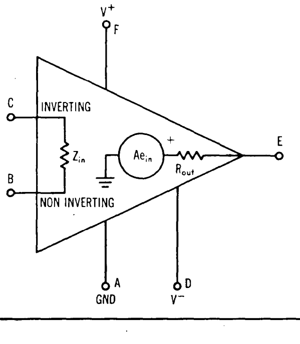
MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+ V^-	+14 -7.0	Vdc Vdc
Differential Input Signal	V_{in}	±5.0	Volts
Common Mode Input Swing	CMV_{in}	±7.0	Volts
Peak Load Current	I_L	10	mA
Power Dissipation (package limitations) Metal Can Derate above T_A = +25°C Flat Package Derate above T_A = +25°C	P_D	 680 4.6 500 3.3	 mW mW/°C mW mW/°C
Operating Temperature Range	T_A	-55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

CIRCUIT SCHEMATIC



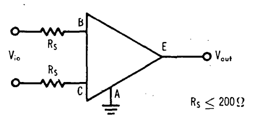
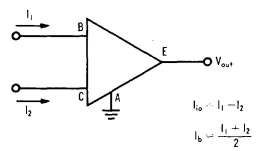
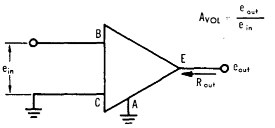
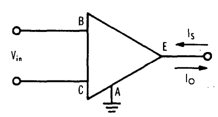
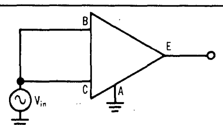
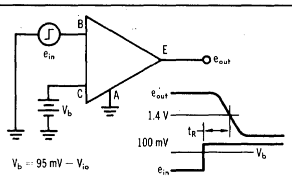
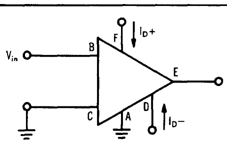
EQUIVALENT CIRCUIT



See Packaging Information Section for outline dimensions.

See current MCC1710/1710C data sheet for standard linear chip information.

ELECTRICAL CHARACTERISTICS ($V^+ = +12$ Vdc, $V^- = -6$ Vdc, $T_A = 25°C$ unless otherwise noted)

Characteristic Definitions (linear operation)	Characteristic	Symbol	Min	Typ	Max	Unit
	Input Offset Voltage $V_{out} = 1.4$ Vdc, $T_A = 25°C$ $V_{out} = 1.8$ Vdc, $T_A = -55°C$ $V_{out} = 1.0$ Vdc, $T_A = +125°C$	V_{io}	 - - -	 1.0 - -	 2.0 3.0 3.0	mVdc
	Temperature Coefficient of Input Offset Voltage	TC_{Vio}	-	3.0	-	$\mu V/°C$
	Input Offset Current $V_{out} = 1.4$ Vdc, $T_A = 25°C$ $V_{out} = 1.8$ Vdc, $T_A = -55°C$ $V_{out} = 1.0$ Vdc, $T_A = +125°C$	I_{io}	 - - -	 1.0 - -	 3.0 7.0 3.0	μAdc
	Input Bias Current $V_{out} = 1.4$ Vdc, $T_A = 25°C$ $V_{out} = 1.8$ Vdc, $T_A = -55°C$ $V_{out} = 1.0$ Vdc, $T_A = +125°C$	I_b	 - - -	 12 - -	 20 45 20	μAdc
	Open Loop Voltage Gain $T_A = 25°C$ $T_A = -55$ to $+125°C$	A_{VOL}	 1250 1000	 1700 -	 - -	V/V
	Output Resistance	R_{out}	-	200	-	ohms
	Differential Voltage Range	V_{in}	±5.0	-	-	Vdc
	Positive Output Voltage $V_{in} \geq 5.0$ mV, $0 \leq I_O \leq 5.0$ mA	V_{OH}	2.5	3.2	4.0	Vdc
	Negative Output Voltage $V_{in} \geq -5.0$ mV	V_{OL}	-1.0	-0.5	0	Vdc
	Output Sink Current $V_{in} \geq -5.0$ mV, $V_{out} \geq 0$, $T_A = 25°C$ $V_{in} \geq -5.0$ mV, $V_{out} \geq 0$, $T_A = -55°C$	I_s	 2.0 1.0	 2.5 2.0	 - -	mAdc
	Input Common Mode Range	CMV_{in}	±5.0	-	-	Volts
	Common Mode Rejection Ratio $V^- = -7.0$ Vdc, $R_S \leq 200\Omega$	CM_{rej}	80	100	-	dB
	Propagation Delay Time For Positive and Negative Going Input Pulse	t_{pd}	-	40	-	ns
	Power Supply Current $V_{out} \leq 0$ Vdc	I_D^+ I_D^-	- -	6.4 5.5	9.0 7.0	mAdc
	Power Consumption TO-99 Metal Can TO-91 Flat Package		 - -	 115 115	 150 150	mW

TYPICAL CHARACTERISTICS

FIGURE 1 – VOLTAGE TRANSFER CHARACTERISTICS

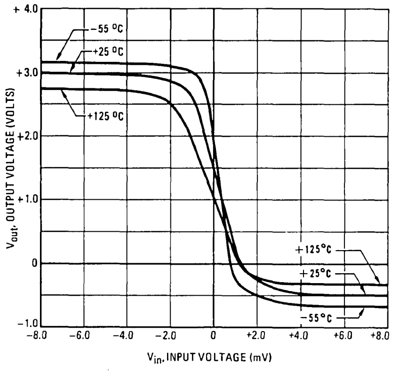


FIGURE 2 – INPUT OFFSET VOLTAGE versus TEMPERATURE

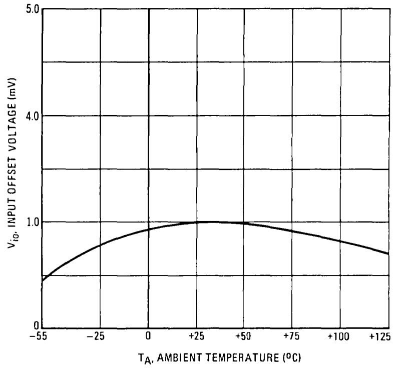


FIGURE 3 – INPUT OFFSET CURRENT versus TEMPERATURE

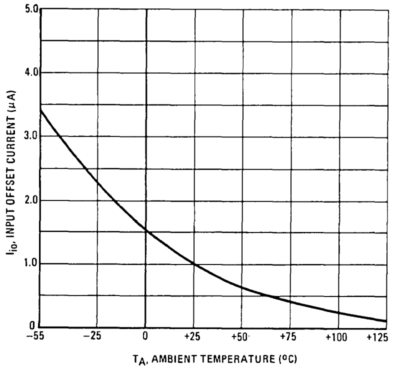


FIGURE 4 – INPUT BIAS CURRENT versus TEMPERATURE

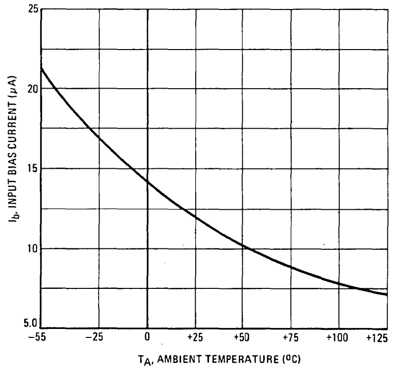


FIGURE 5 – GAIN VARIATION WITH POWER SUPPLY VOLTAGE

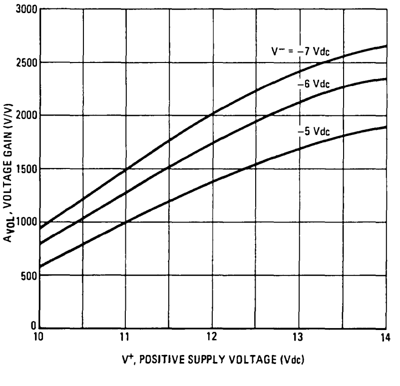


FIGURE 6 – VOLTAGE GAIN versus TEMPERATURE

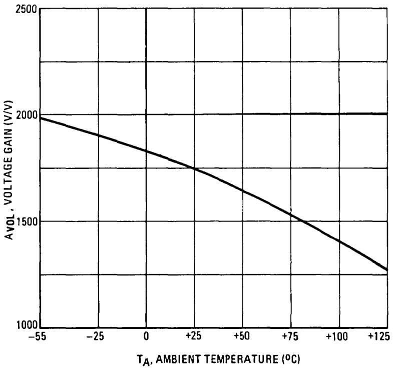


FIGURE 7 – RESPONSE TIME

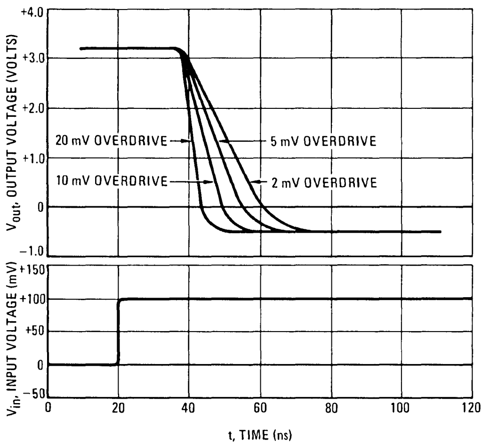


FIGURE 8 – POWER DISSIPATION versus TEMPERATURE

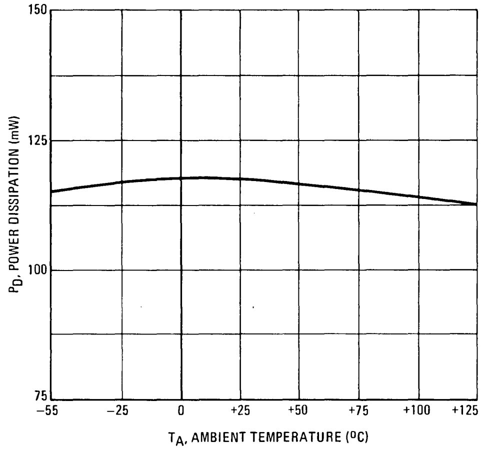


FIGURE 9 – RECOMMENDED SERIES RESISTANCE versus MRTL LOADS

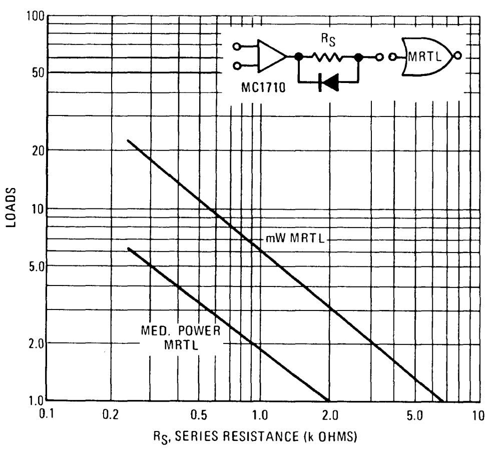
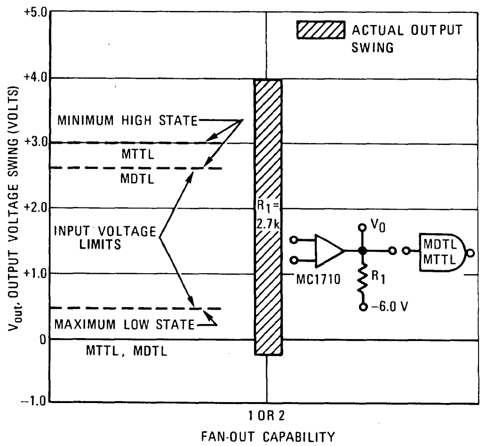


FIGURE 10 – FAN-OUT CAPABILITY WITH MDTL OR MTTL OUTPUT SWING



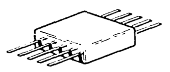
6

MC1710C

DIFFERENTIAL COMPARATOR

DIFFERENTIAL COMPARATOR

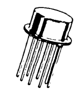
. . . designed for use in level detection, low-level sensing, and memory applications.



F SUFFIX
CERAMIC PACKAGE
CASE 606
TO-91

L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

Lead 4 connected to case



G SUFFIX
METAL PACKAGE
CASE 601
TO-99

Typical Amplifier Features:

- Differential Input Characteristics:
  Input Offset Voltage = 1.5 mV
  Offset Voltage Drift = 5.0 μV/^{o}C
- Fast Response Time — 40 ns
- Output Compatible with All Saturating Logic Forms
  V_{out} = +3.2 V to -0.5 V typical
- Low Output Impedance — 200 ohms

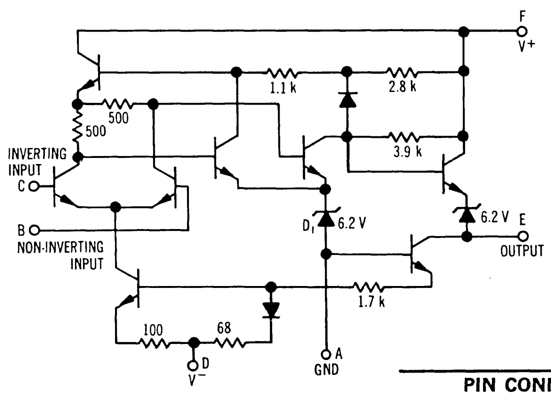
MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+ V^-	+14 -7.0	Vdc Vdc
Differential Input Signal	V_{in}	±5.0	Volts
Common Mode Input Swing	CMV_{in}	±7.0	Volts
Peak Load Current	I_L	10	mA
Power Dissipation (package limitation) Metal Can Derate above 25°C Flat Package Derate above 25°C Plastic Package Derate above 25°C	P_D	 680 4.6 500 3.3 400 3.3	 mW mW/°C mW mW/°C mW mW/°C
Operating Temperature Range*	T_A	0 to +75	°C
Storage Temperature Range Metal Can and Flat Package Plastic Package	T_{stg}	 -65 to +150 -65 to +125	°C

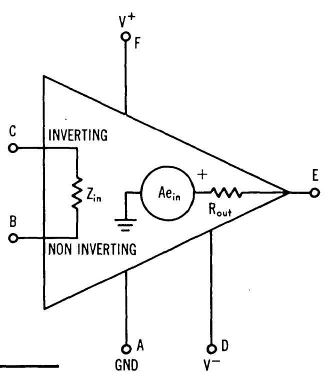
*For full temperature range (-55°C to + 125°C) and characteristic curves, see MC1710 data sheet.

6

CIRCUIT SCHEMATIC



EQUIVALENT CIRCUIT

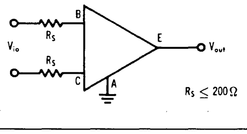
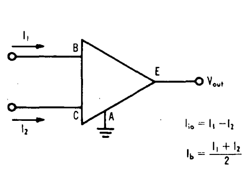
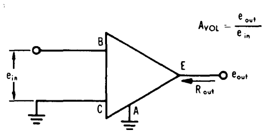
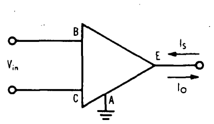
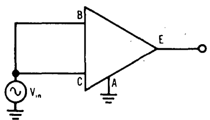
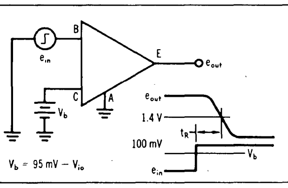
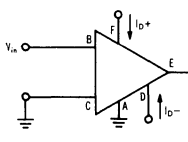


PIN CONNECTIONS

Schematic	A	B	C	D	E	F
"G" Package	1	2	3	4	7	8
"F" Package	1	2	3	5	6	8
"L" Package	2	3	4	6	9	11

See Packaging Information Section for outline dimensions.
See current MCC1710/1710C data sheet for standard linear chip information.

ELECTRICAL CHARACTERISTICS ($V^+ = +12$ Vdc, $V^- = -6$ Vdc, $T_A = 25°C$ unless otherwise noted)

Characteristic Definitions	Characteristic	Symbol	Min	Typ	Max	Unit
	Input Offset Voltage $V_{out} = 1.4$ Vdc, $T_A = 25°C$ $V_{out} = 1.5$ Vdc, $T_A = 0°C$ $V_{out} = 1.2$ Vdc, $T_A = +70°C$	V_{io}	 - - -	 1.5 - -	 5.0 6.5 6.5	mVdc
	Temperature Coefficient of Input Offset Voltage	TC_{Vio}	-	5.0	-	µV/°C
	Input Offset Current $V_{out} = 1.4$ Vdc, $T_A = 25°C$ $V_{out} = 1.5$ Vdc, $T_A = 0°C$ $V_{out} = 1.2$ Vdc, $T_A = +70°C$	I_{io}	 - - -	 1.0 - -	 5.0 7.5 7.5	µAdc
	Input Bias Current $V_{out} = 1.4$ Vdc, $T_A = 25°C$ $V_{out} = 1.5$ Vdc, $T_A = 0°C$ $V_{out} = 1.2$ Vdc, $T_A = +70°C$	I_b	 - - -	 15 25 -	 25 40 40	µAdc
	Voltage Gain $T_A = 25°C$ $T_A = 0$ to $+70°C$	A_{VOL}	 1000 800	 1500 -	 - -	V/V
	Output Resistance	R_{out}	-	200	-	ohms
	Differential Voltage Range	V_{in}	±5.0	-	-	Vdc
	Positive Output Voltage $V_{in} \geq 5.0$ mV, $0 \leq I_O \leq 5.0$ mA	V_{OH}	2.5	3.2	4.0	Vdc
	Negative Output Voltage $V_{in} \geq -5.0$ mV	V_{OL}	-1.0	-0.5	0	Vdc
	Output Sink Current $V_{in} \geq -5.0$ mV, $V_{out} \geq 0$ $T_A = 25°C$ $T_A = 0°C$	I_S	 1.6 0.5	 2.5 -	 - -	mAdc
	Input Common Mode Range $V^- = -7.0$ Vdc	CMV_{in}	±5.0	-	-	Volts
	Common Mode Rejection Ratio $R_S \leq 200\ \Omega$	CM_{rej}	70	100	-	dB
	Propagation Delay Time For Positive and Negative Going Input Pulse	t_{pd}	-	40	-	ns
	Power Supply Current $V_{out} \leq 0$ Vdc	I_D^+ I_D^-	- -	6.4 5.5	9.0 7.0	mAdc
	Power Consumption		-	110	150	mW

6

MC1711

DIFFERENTIAL COMPARATORS

MONOLITHIC DUAL DIFFERENTIAL VOLTAGE COMPARATOR

. . . designed for use in level detection, low-level sensing, and memory applications.

Typical Characteristics:

- Differential Input –
  Input Offset Voltage = 1.0 mV
  Offset Voltage Drift = 5.0 μV/^{o}C
- Fast Response Time – 40 ns
- Output Compatible with All Saturating Logic Forms –
  V_{out} = +4.5 V to -0.5 V Typical
- Low Output Impedance – 200 Ohms

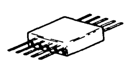
DUAL DIFFERENTIAL COMPARATOR INTEGRATED CIRCUIT

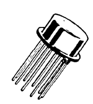
MONOLITHIC
SILICON EPITAXIAL PASSIVATED

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+ V^-	+14 -7.0	Vdc Vdc
Differential Input Signal	V_{in}	±5.0	Volts
Common Mode Input Swing	CMV_{in}	±7.0	Volts
Peak Load Current	I_L	50	mA
Power Dissipation (package limitation) Metal Can Derate above T_A = 25°C Ceramic Dual In-line Package Derate above T_A = 75°C Flat Package Derate above T_A = 25°C	P_D	 680 4.6 670 6.7 500 3.3	 mW mW/°C mW mW/°C mW mW/°C
Operating Temperature Range	T_A	-55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

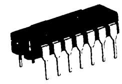
F SUFFIX
CERAMIC PACKAGE
CASE 606
TO-91





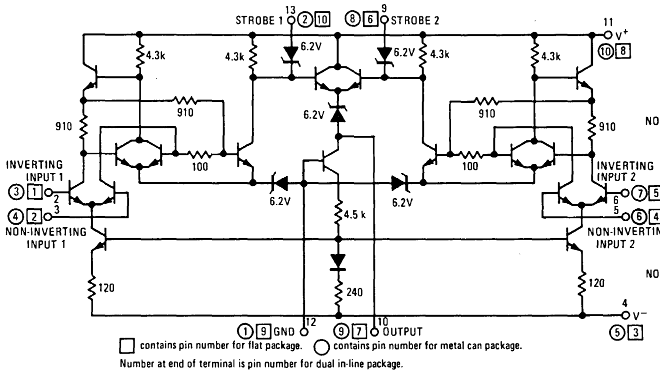
G SUFFIX
METAL PACKAGE
CASE 603-02
TO-100

L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116



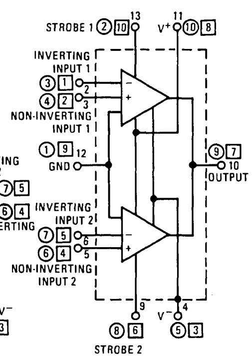
6

CIRCUIT SCHEMATIC



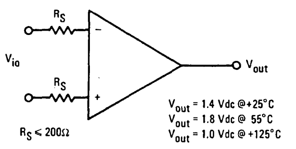
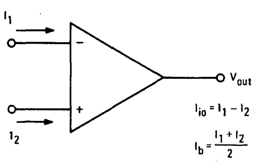
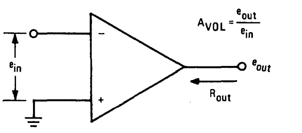
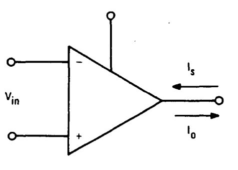
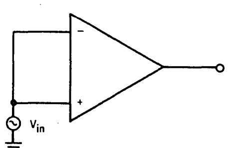
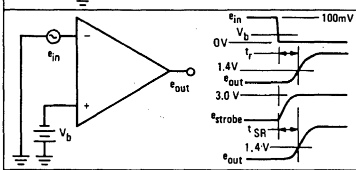
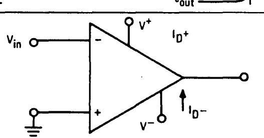
contains pin number for flat package. contains pin number for metal can package.
Number at end of terminal is pin number for dual in-line package.

EQUIVALENT CIRCUIT



See Packaging Information Section for outline dimensions.
See current MCC1711/1711C data sheet for standard linear chip information.

ELECTRICAL CHARACTERISTICS (each comparator) V^+ = +12 Vdc. V^- = −6.0 Vdc. T_A = 25°C unless otherwise noted)

Characteristic Definitions	Characteristic	Symbol	Min	Typ	Max	Unit
	Input Offset Voltage	V_{io}				mVdc
	CMV_{in} = 0 Vdc, T_A = +25°C		-	1.0	3.5	
	T_A = +25°C		-	1.0	5.0	
	CMV_{in} = 0 Vdc, T_A = -55 to +125°C		-	-	4.5	
	T_A = -55 to +125°C		-	-	6.0	
	Temperature Coefficient of Input Offset Voltage	TC_{Vio}	-	5.0	-	µV/°C
	Input Offset Current	I_{io}				µAdc
	V_{out} = 1.4 Vdc, T_A = +25°C		-	0.5	10	
	V_{out} = 1.8 Vdc, T_A = -55°C		-	-	20	
	V_{out} = 1.0 Vdc, T_A = +125°C		-	-	20	
	Input Bias Current	I_b				µAdc
	V_{out} = 1.4 Vdc, T_A = +25°C		-	25	75	
	V_{out} = 1.8 Vdc, T_A = -55°C		-	-	150	
	V_{out} = 1.0 Vdc, T_A = +125°C		-	-	150	
	Voltage Gain	A_{VOL}				V/V
	T_A = +25°C		750	1500	-	
	T_A = -55 to +125°C		500	-	-	
	Output Resistance	R_{out}	-	200	-	ohms
	Differential Voltage Range	V_{in}	±5.0	-	-	Vdc
	Positive Output Voltage V_{in} ≧ 10 mVdc, 0 ≦ I_o ≦ 5.0 mA	V_{OH}	2.5	3.2	5.0	Vdc
	Negative Output Voltage V_{in} ≧ -10 mVdc	V_{OL}	-1.0	-0.5	0	Vdc
	Strobed Output Level V_{strobe} ≦ 0.3 Vdc	$V_{OL(st)}$	-1.0	-	0	Vdc
	Output Sink Current V_{in} ≧ -10 mV, V_{out} ≧ 0	I_S	0.5	0.8	-	mAdc
	Strobe Current V_{strobe} = 100 mVdc	I_{st}	-	1.2	2.5	mAdc
	Input Common Mode Range V^- = -7.0 Vdc	CM_{Vin}	±5.0	-	-	Volts
	Response Time V_b = 5.0 mV + V_{io}	t_R	-	40	-	ns
	Strobe Release Time	t_{SR}	-	12	-	ns
	Power Supply Current V_{out} ≦ 0 Vdc	$I_D{}^+$	-	8.6	-	mAdc
		$I_D{}^-$	-	3.9	-	
	Power Consumption		-	130	200	mW

TYPICAL CHARACTERISTICS

FIGURE 1 – VOLTAGE TRANSFER CHARACTERISTICS

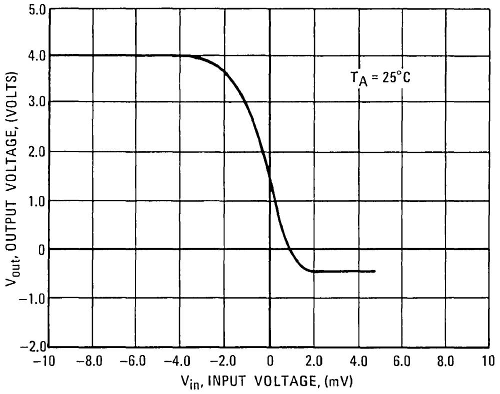


FIGURE 2 – INPUT BIAS CURRENT versus TEMPERATURE

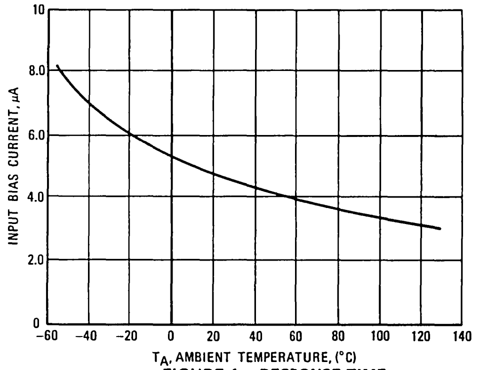


FIGURE 3 – VOLTAGE GAIN versus TEMPERATURE

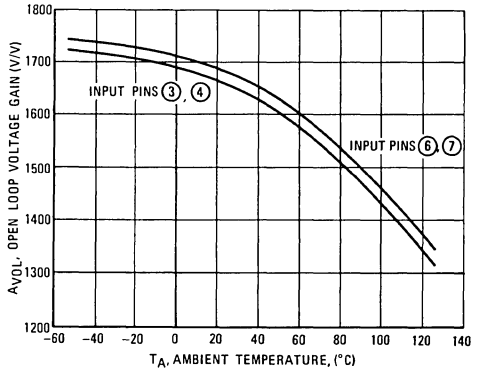


FIGURE 4 – RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

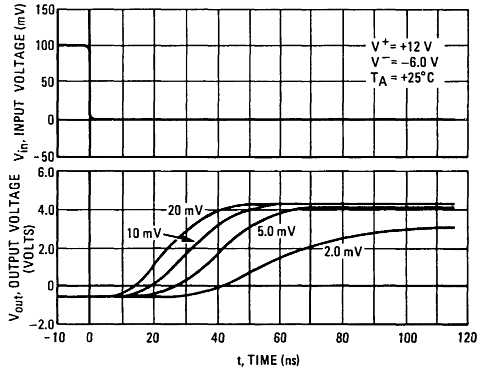


FIGURE 5 – POWER DISSIPATION versus TEMPERATURE

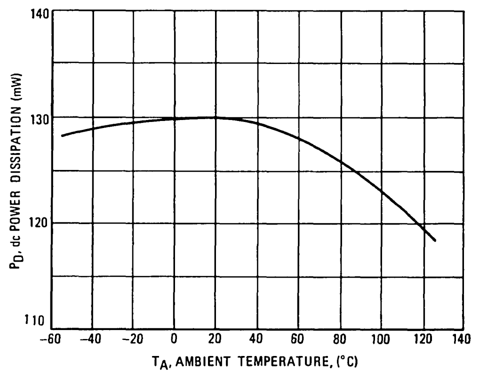


FIGURE 6 – STROBE RELEASE TIME FOR VARIOUS INPUT OVERDRIVES

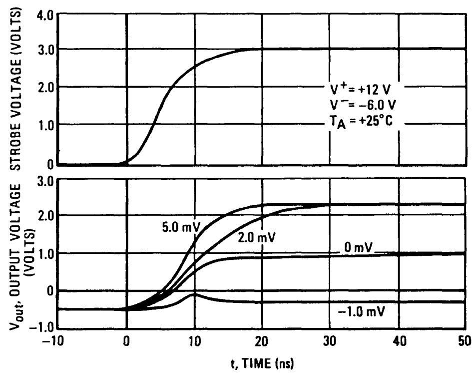


FIGURE 7 – COMMON MODE PULSE RESPONSE

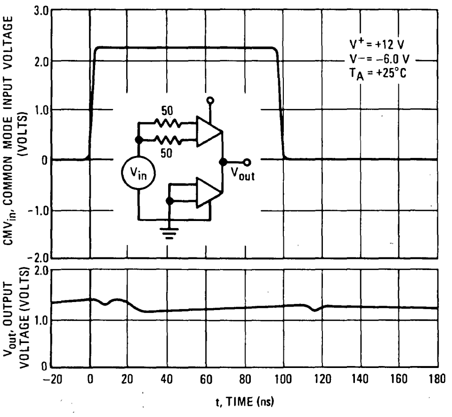


FIGURE 8 – OUTPUT PULSE STRETCHING WITH CAPACITIVE LOADING

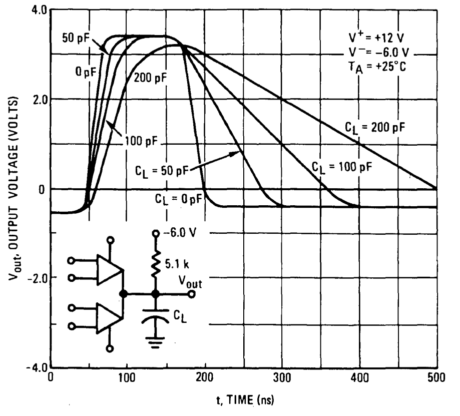


FIGURE 9 – SERIES RESISTANCE versus MRTL FAN-OUTS

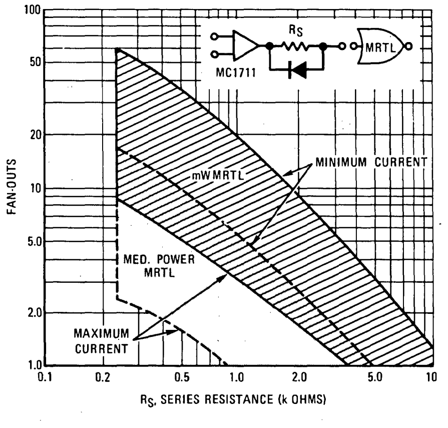
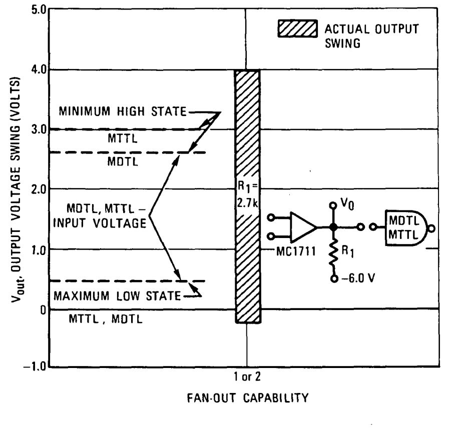


FIGURE 10 – FAN-OUT CAPABILITY WITH MDTL OR MTTL OUTPUT SWING



6

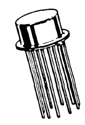
MC1711C

DIFFERENTIAL COMPARATORS

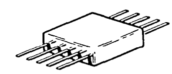
DUAL DIFFERENTIAL COMPARATOR

. . . designed for use in level detection, low level sensing, and memory applications.

Lead 5 connected to case



G SUFFIX
METAL PACKAGE
CASE 603-02
TO-100



F SUFFIX
CERAMIC PACKAGE
CASE 606
TO-91

L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

Typical Amplifier Features:

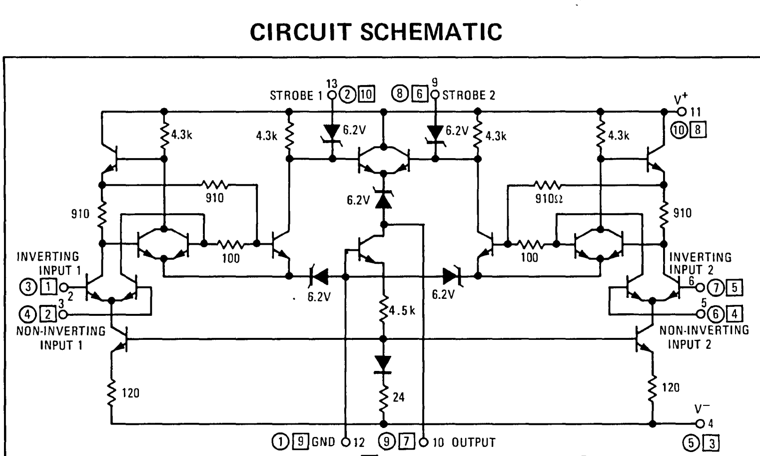
- Differential Input
  Input Offset Voltage = 1.0 mV
  Offset Voltage Drift = 5.0 μV/$^{\circ}$C
- Fast Response Time — 40 ns
- Output Compatible with All Saturating Logic Forms
  V_{out} = +4.5 V to -0.5 V typical
- Low Output Impedance — 200 ohms

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

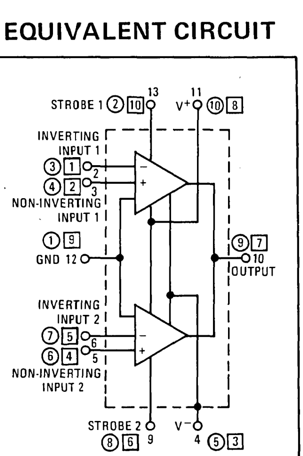
Rating	Symbol	Value	Unit
Power Supply Voltage	V^+ V^-	+14 -7.0	Vdc Vdc
Differential Input Signal	V_{in}	±5.0	Volts
Common Mode Input Swing	CMV_{in}	±7.0	Volts
Peak Load Current	I_L	50	mA
Power Dissipation (package limitation) Metal Can Derate above T_A = 25°C Flat Package Derate above T_A = 25°C Ceramic Dual In-Line Package Derate above T_A = 25°C	P_D	 680 4.6 500 3.3 1000 6 7	 mW mW/°C mW mW/°C mW mW/°C
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

6

CIRCUIT SCHEMATIC



EQUIVALENT CIRCUIT

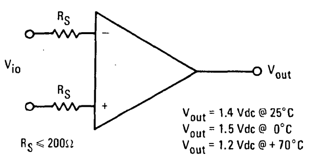
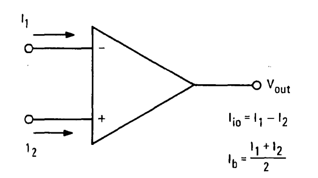
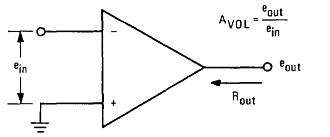
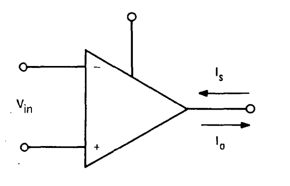
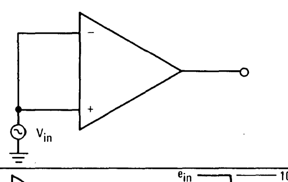
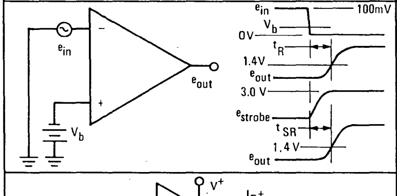
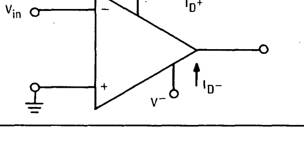


Number at end of terminal is pin number for dual in-line package. □ contains pin number for flat package. ○ contains pin number for metal can package.

See Packaging Information Section for outline dimensions.

See current MCC1711/1711C data sheet for standard linear chip information.

ELECTRICAL CHARACTERISTICS (each comparator) $V^+ = +12$ Vdc. $V^- = -6.0$ Vdc. $T_A = 25°C$ unless otherwise noted)

Characteristic Definitions	Characteristic	Symbol	Min	Typ	Max	Unit
	Input Offset Voltage	V_{io}				mVdc
	$CMV_{in} = 0$ Vdc, $T_A = +25°C$		-	1.0	5.0	
	$CMV_{in} \neq 0$ Vdc, $T_A = +25°C$		-	1.0	7.5	
	$CMV_{in} = 0$ Vdc, $T_A = 0$ to $+70°C$		-	-	6.0	
	$CMV_{in} \neq 0$ Vdc, $T_A = 0$ to $+70°C$		-	-	10	
	Temperature Coefficient of Input Offset Voltage	TC_{Vio}	-	5.0	-	µV/°C
	Input Offset Current	I_{io}				µAdc
	$V_{out} = 1.4$ Vdc, $T_A = +25°C$		-	0.5	15	
	$V_{out} = 1.5$ Vdc, $T_A = 0°C$		-	-	25	
	$V_{out} = 1.2$ Vdc, $T_A = +70°C$		-	-	25	
	Input Bias Current	I_b				µAdc
	$V_{out} = 1.4$ Vdc, $T_A = +25°C$		-	25	100	
	$V_{out} = 1.5$ Vdc, $T_A = 0°C$		-	-	150	
	$V_{out} = 1.2$ Vdc, $T_A = +70°C$		-	-	150	
	Voltage Gain	A_{VOL}				V/V
	$T_A = +25°C$		700	1500	-	
	$T_A = -55$ to $+125°C$		500	-	-	
	Output Resistance	R_{out}	-	200	-	ohms
	Differential Voltage Range	V_{in}	±5.0	-	-	Vdc
	Positive Output Voltage $V_{in} \geq 10$ mVdc, $0 \leq I_O \leq 5.0$ mA	V_{OH}	2.5	3.2	5.0	Vdc
	Negative Output Voltage $V_{in} \geq -10$ mVdc	V_{OL}	-1.0	-0.5	0	Vdc
	Strobed Output Level $V_{strobe} \leq 0.3$ Vdc	$V_{OL(st)}$	-1.0	-	0	Vdc
	Output Sink Current $V_{in} \geq -10$ mV, $V_{out} \geq 0$	I_S	0.5	0.8	-	mAdc
	Strobe Current $V_{strobe} = 100$ mVdc	I_{st}	-	1.2	2.5	mAdc
	Input Common Mode Range $V^- = -7.0$ Vdc	CM_{Vin}	±5.0	-	-	Volts
	Response Time $V_b = 5.0$ mV + V_{io}	t_R	-	40	-	ns
	Strobe Release Time	t_{SR}	-	12	-	ns
	Power Supply Current $V_{out} \leq 0$ Vdc	I_D+	-	8.6	-	mAdc
		I_D-	-	3.9	-	
	Power Consumption		-	130	200	mW

TYPICAL CHARACTERISTICS

FIGURE 1 – VOLTAGE TRANSFER CHARACTERISTICS

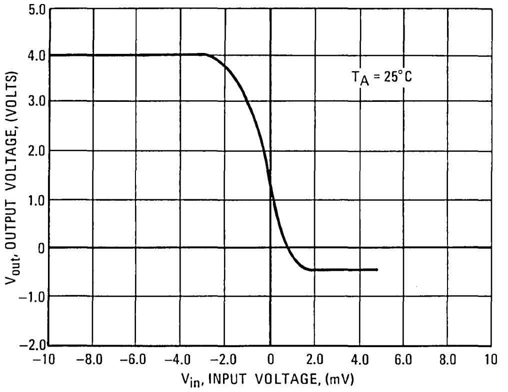


FIGURE 2 – INPUT BIAS CURRENT versus TEMPERATURE

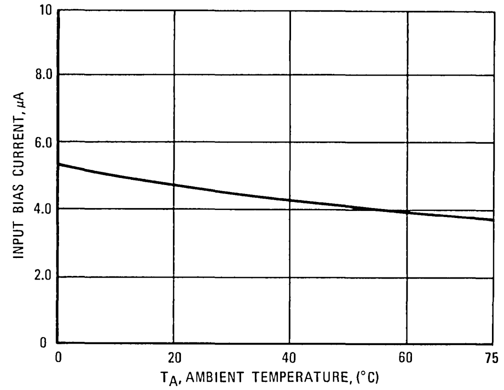


FIGURE 3 – VOLTAGE GAIN versus TEMPERATURE

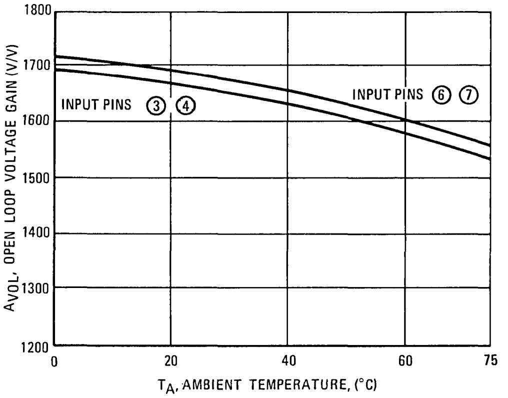


FIGURE 4 – RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

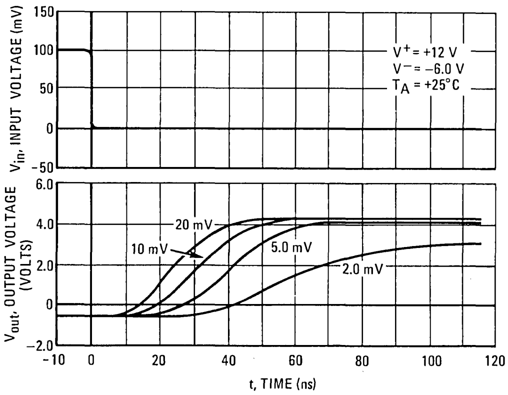


FIGURE 5 – POWER DISSIPATION versus TEMPERATURE

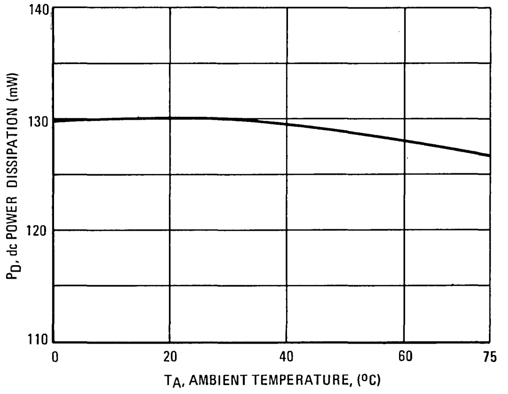


FIGURE 6 – STROBE RELEASE TIME FOR VARIOUS INPUT OVERDRIVES

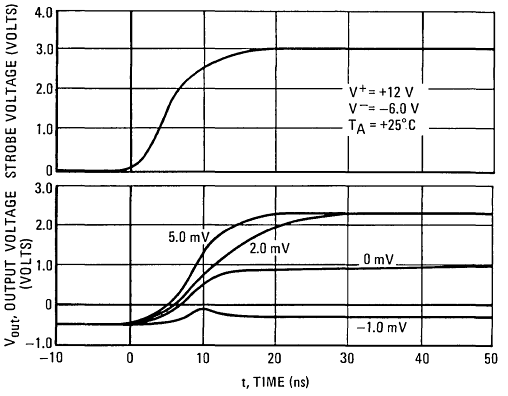


FIGURE 7 – COMMON MODE PULSE RESPONSE

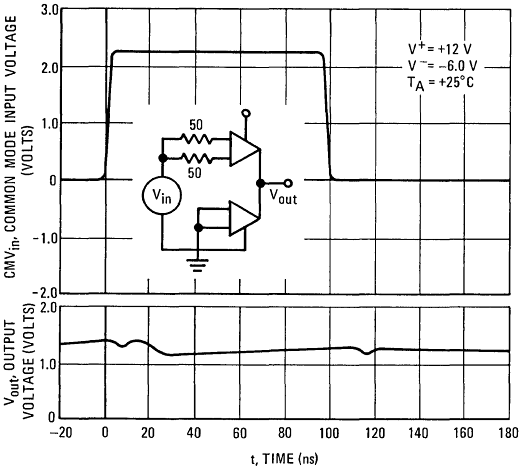


FIGURE 8 – OUTPUT PULSE STRETCHING WITH CAPACITIVE LOADING

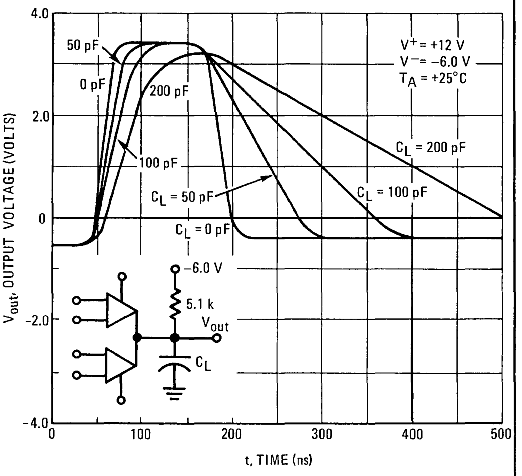


FIGURE 9 – SERIES RESISTANCE versus MRTL FAN-OUTS

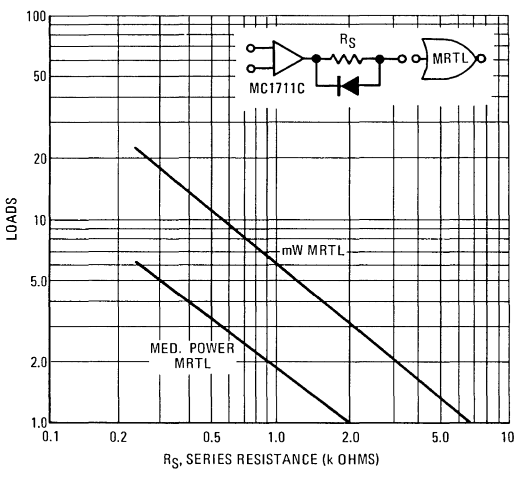
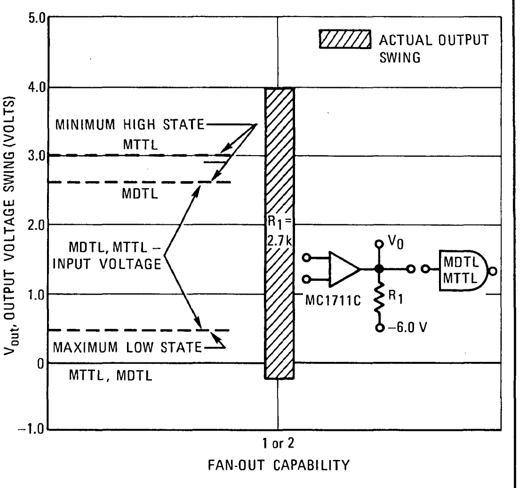


FIGURE 10 – FAN-OUT CAPABILITY WITH MDTL OR MTTL OUTPUT SWING



MC1712
MC1712C

OPERATIONAL AMPLIFIERS

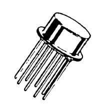
MONOLITHIC WIDEBAND DC AMPLIFIER

. . . designed for use as an operational amplifier utilizing operating characteristics as a function of the external feedback components.

- Open Loop Gain A_{VOL} = 3600 typical
- Low Temperature Drift – ±2.5 μV/°C
- Output Voltage Swing –
  ±5.3 V typical @ +12 V and -6 V Supplies
- Low Output Impedance – Z_{out} = 200 ohms typical

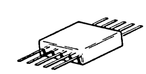
WIDEBAND DC AMPLIFIER INTEGRATED CIRCUIT

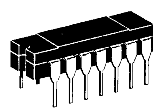
MONOLITHIC SILICON EPITAXIAL PASSIVATED



G SUFFIX
METAL PACKAGE
CASE 601
TO-99

F SUFFIX
CERAMIC PACKAGE
CASE 606
TO-91





L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

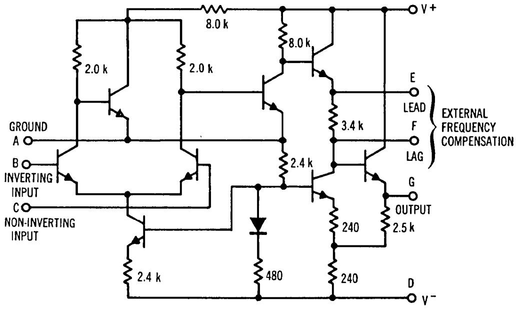
MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage (Total between V^+ and V^- terminals)	$\|V^+\|+\|V^-\|$	21	Vdc
Differential Input Signal	V_{in}	±5.0	Volts
Common Mode Input Swing	CMV_{in}	+1.5 -6.0	Volts
Peak Load Current	I_L	50	mA
Power Dissipation (Package Limitation)	P_D		
Metal Package		680	mW
Derate above T_A = +25°C		4.6	mW/°C
Flat Ceramic Package		500	mW
Derate above T_A = +25°C		3.3	mW/°C
Dual In-Line Ceramic Package		625	mW
Derate above T_A = +25°C		5.0	mW/°C
Operating Temperature Range MC1712 MC1712C	T_A	-55 to +125 0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

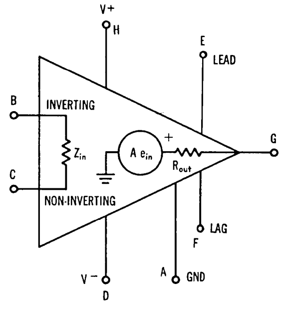
PIN CONNECTIONS

Schematic	A	B	C	D	E	F	G	H
"G" Package	1	2	3	4	5	6	7	8
"F" Package	2	3	4	5	6	7	8	10
"L" Package	3	4	5	6	9	10	12	13

CIRCUIT SCHEMATIC



EQUIVALENT CIRCUIT



See Packaging Information Section for outline dimensions.

MC1712, MC1712C (continued)

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted)

Characteristic	Symbol	MC1712 Min	MC1712 Typ	MC1712 Max	MC1712C Min	MC1712C Typ	MC1712C Max	Unit
Open-Loop Voltage Gain (R_L = 100 kΩ)	A_{VOL}							V/V
(V^+ = 6.0 Vdc, V^- = −3.0 Vdc, V_o = ±2.5 V)		600	900	1500	500	800	1500	
(V^+ = 12 Vdc, V^- = −6.0 Vdc, V_o = ±5.0 V)		2500	3600	6000	2000	3400	6000	
(V^+ = 12 Vdc, V^- = −6.0 Vdc, V_o = ±5.0 Vdc, T_A = T_{low} ①, T_{high} ①)		2000	–	7000	1500	–	7000	
(V^+ = 6.0 Vdc, V^- = −3.0 Vdc, V_o = ±2.5 V, T_A = T_{low} to T_{high})		500	–	1750	400	–	1750	
Output Impedance	Z_{out}							ohms
(V^+ = 6.0 Vdc, V^- = −3.0 Vdc, f = 20 Hz)		–	300	700	–	300	800	
(V^+ = 12 Vdc, V^- = −6.0 Vdc, f = 20 Hz)		–	200	500	–	200	600	
Input Impedance	Z_{in}							k ohms
(V^+ = 6.0 Vdc, V^- = −3.0 Vdc, f = 20 Hz)		22	70	–	16	55	–	
(V^+ = 6.0 Vdc V^- = −3.0 Vdc, f = 20 Hz, T_A = T_{low}, T_{high})		8.0	–	–	10	32	–	
(V^+ = 12 Vdc, V^- = −6.0 Vdc, f = 20 Hz)		16	40	–	–	–	–	
(V^+ = 12 Vdc, V^- = −6.0 Vdc, f = 20 Hz, T_A = T_{low}, T_{high})		6.0	–	–	–	–	–	
Output Voltage Swing	V_o							V_{peak}
(V^+ = 6.0 Vdc, V^- = −3.0 Vdc, R_L = 100 kΩ)		±2.5	±2.7	–	±2.5	±2.7	–	
(V^+ = 12 Vdc, V^- = −6.0 Vdc, R_L = 100 kΩ)		±5.0	±5.3	–	±5.0	±5.3	–	
(V^+ = +6.0 Vdc, V^- = −3.0 Vdc, R_L = 10 kΩ)		±1.5	±2.0	–	±1.5	±2.0	–	
(V^+ = +12 Vdc, V^- = −6.0 Vdc, R_L = 10 kΩ)		±3.5	±4.0	–	±3.5	±4.0	–	
Input Common-Mode Voltage Swing	CMV_{in}							V_{peak}
(V^+ = 6.0 Vdc, V^- = −3.0 Vdc)		+0.5	–	–	+0.5	–	–	
		−1.5	–	–	−1.5	–	–	
(V^+ = 12 Vdc, V^- = −6.0 Vdc)		+0.5	–	–	+0.5	–	–	
		−4.0	–	–	−4.0	–	–	
Common-Mode Rejection Ratio	CM_{rej}							dB
(V^+ = 6.0 Vdc, V^- = −3.0 Vdc, f ≤ 1.0 kHz)		80	100	–	70	95	–	
(V^+ = 12 Vdc, V^- = −6.0 Vdc, f ≤ 1.0 kHz)		80	100	–	70	95	–	
Input Bias Current $I_b = \frac{I_1 + I_2}{2}$, T_A = +25°C	I_b							μA
(V^+ = 6.0 Vdc, V^- = −3.0 Vdc)		–	1.2	3.5	–	1.5	5.0	
(V^+ = 12 Vdc, V^- = −6.0 Vdc)		–	2.0	5.0	–	2.5	7.5	
T_A = T_{low} (V^+ = 6.0 Vdc, V^- = −3.0 Vdc)		–	2.5	7.5	–	2.5	8.0	
(V^+ = 12 Vdc, V^- = −6.0 Vdc)		–	4.0	10	–	4.0	12	
Input Offset Current (I_{io} = $I_1 - I_2$)	$\lvert I_{io}\rvert$							μA
(V^+ = 6.0 Vdc, V^- = −3.0 Vdc)		–	0.1	0.5	–	0.3	2.0	
(V^+ = 6.0 Vdc, V^- = −3.0 Vdc, T_A = T_{low} to T_{high})		–	–	1.5	–	–	2.5	
(V^+ = 12 Vdc, V^- = −6.0 Vdc)		–	0.2	0.5	–	0.5	2.0	
(V^+ = 12 Vdc, V^- = −6.0 Vdc, T_A = T_{low} to T_{high})		–	–	1.5	–	–	2.5	
Input Offset Voltage (R_S = 2.0 kΩ)	$\lvert V_{io}\rvert$							mV
(V^+ = 6.0 Vdc, V^- = −3.0 Vdc)		–	1.3	3.0	–	1.7	6.0	
(V^+ = 6.0 Vdc, V^- = −3.0 Vdc, T_A = T_{low}, T_{high})		–	–	4.0	–	–	7.5	
(V^+ = 12 Vdc, V^- = −6.0 Vdc)		–	1.1	2.0	–	1.5	5.0	
(V^+ = 12 Vdc, V^- = −6.0 Vdc, T_A = T_{low}, T_{high})		–	–	3.0	–	–	6.5	
Step Response								
(V^+ = 12 Vdc, V^- = −6.0 Vdc	V_{os}	–	20	40	–	20	40	%
Gain = 100, V_{in} = 1.0 mV,	t_f	–	10	30	–	10	30	ns
R_1 = 1.0 kΩ, R_2 = 100 kΩ,	t_{pd}	–	10	–	–	10	–	ns
C_2 = 50 pF, R_3 = ∞, C_1 = open)	dV_{out}/dt ②	–	12	–	–	12	–	V/μs
(V^+ = 12 Vdc, V^- = −6.0 Vdc	V_{os}	–	10	50	–	10	50	%
Gain = 1.0, V_{in} = 10 mV,	t_f	–	25	120	–	25	120	ns
R_1 = 10 kΩ, R_2 = 10 kΩ,	t_{pd}	–	16	–	–	16	–	ns
C_1 = 0.01 μF, R_3 = 20Ω, C_2 = open)	dV_{out}/dt ②	–	1.5	–	–	1.5	–	V/μs
Average Temperature Coefficient of Input Offset Voltage (R_S = 50Ω)	$\lvert TC_{Vio}\rvert$							μV/°C
(T_A = +25°C to T_{high})		–	2.5	–	–	–	–	
(T_A = T_{low} to +25°C)		–	2.0	–	–	–	–	
(T_A = T_{low}, T_{high})		–	–	–	–	5.0	–	
Average Temperature Coefficient Input Offset Current	$\lvert TC_{Iio}\rvert$							nA/°C
(T_A = +25°C to T_{high})		–	0.05	–	–	4.0	–	
(T_A = T_{low} to +25°C)		–	1.5	–	–	6.0	–	
DC Power Dissipation	P_D							mW
(V_{out} = 0, V^+ = 6.0 Vdc, V^- = −3.0 Vdc)		–	17	30	–	17	30	
(V_{out} = 0, V^+ = 12 Vdc, V^- = −6.0 Vdc)		–	70	120	–	70	120	
Positive Supply Sensitivity (V^- constant = −6.0 Vdc, V^+ = 12 Vdc to 6.0 Vdc)	S^+	–	60	200	–	60	300	μV/V
Negative Supply Sensitivity (V^+ constant = 12 Vdc, V^- = −6.0 Vdc to −3.0 Vdc)	S^-	–	60	200	–	60	300	μV/V

① T_{low} = 0°C for MC1712C, T_{high} = +75°C for MC1712C
−55°C for MC1712 +125°C for MC1712

② dV_{out}/dt = Slew Rate

TYPICAL OUTPUT CHARACTERISTICS

(V^+ = 12 Vdc, V^- = -6.0 Vdc, T_A = +25°C)

FIGURE 1 – OPEN LOOP GAIN versus POWER SUPPLY VARIATIONS

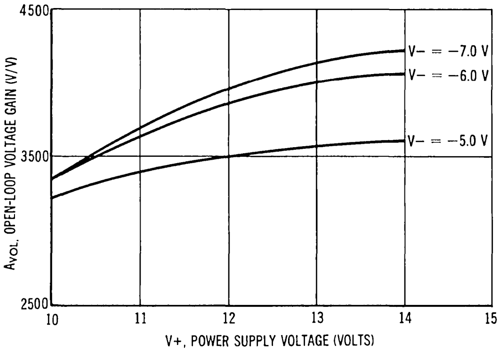


FIGURE 2 – OPEN LOOP VOLTAGE GAIN versus FREQUENCY

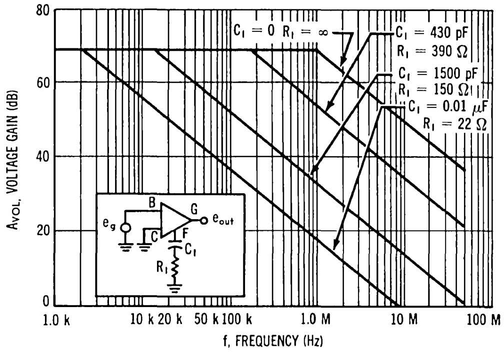


FIGURE 3 – VOLTAGE GAIN versus FREQUENCY

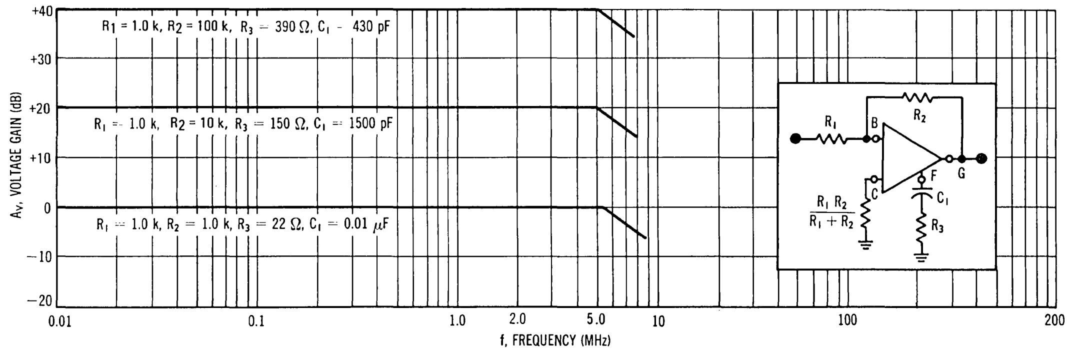


FIGURE 4 – MAXIMUM OUTPUT SWING versus FREQUENCY

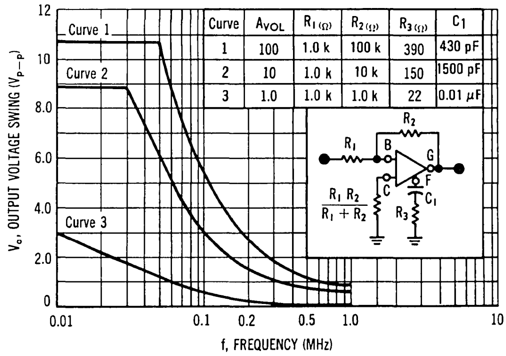
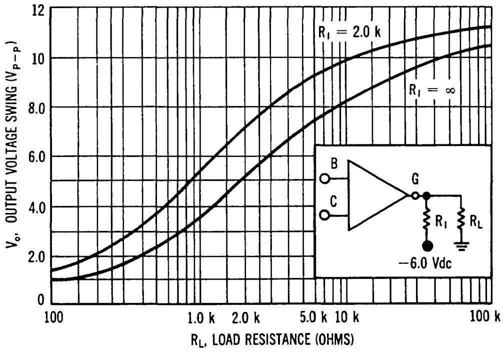


FIGURE 5 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE



TYPICAL CHARACTERISTICS (continued)

FIGURE 6 – INPUT BIAS CURRENT versus TEMPERATURE

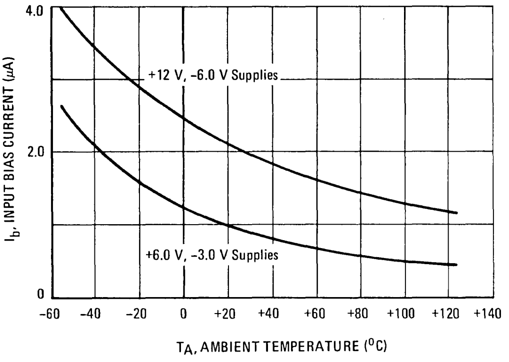


FIGURE 7 – INPUT OFFSET CURRENT versus TEMPERATURE

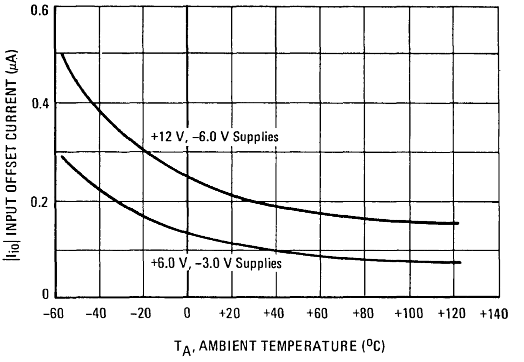


FIGURE 8 – INPUT OFFSET VOLTAGE versus TEMPERATURE

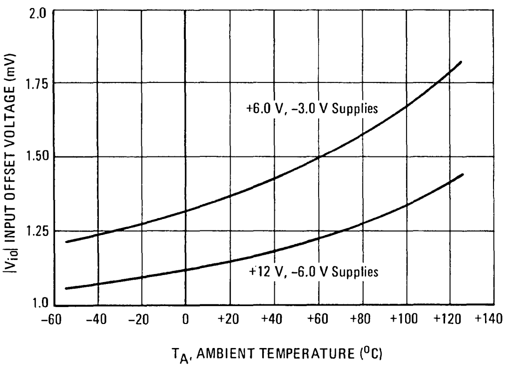
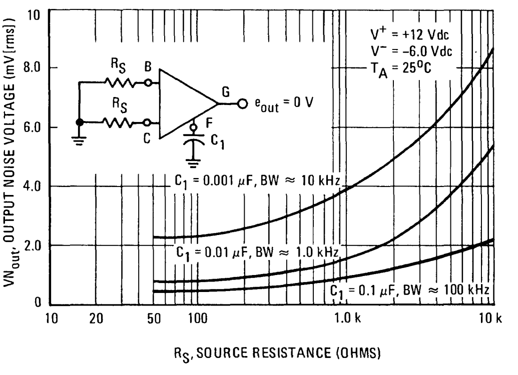


FIGURE 9 – OUTPUT NOISE VOLTAGE versus SOURCE IMPEDANCE



MC1723G
MC1723CG

POSITIVE VOLTAGE REGULATORS

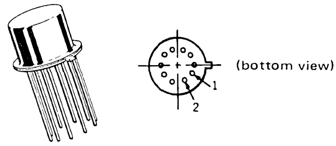
MONOLITHIC VOLTAGE REGULATOR

The MC1723 is a positive or negative voltage regulator designed to deliver load current to 150 mAdc. Output current capability can be increased to several amperes through use of one or more external pass transistors. MC1723 is specified for operation over the military temperature range (-55°C to +125°C) and the MC1723C over the commercial temperature range (0 to +75°C)

- Output Voltage Adjustable from 2 Vdc to 37 Vdc
- Output Current to 150 mAdc Without External Pass Transistors
- 0.01% Line and 0.03% Load Regulation
- Adjustable Short-Circuit Protection

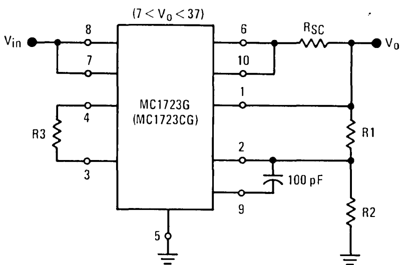
VOLTAGE REGULATOR

MONOLITHIC SILICON
EPITAXIAL PASSIVATED
INTEGRATED CIRCUIT



METAL PACKAGE
CASE 603-03

FIGURE 1 – TYPICAL CIRCUIT CONNECTION



$V_O \cong 7\left(\frac{R1 + R2}{R2}\right)$ $\quad I_{SC} = \frac{V_{sense}}{R_{SC}} = \frac{0.66}{R_{SC}}$ at $T_J = 25°C$

For best results 10 k < R2 < 100 k
For minimum drift R3 = R1||R2

FIGURE 2 – TYPICAL NPN CURRENT BOOST CONNECTION

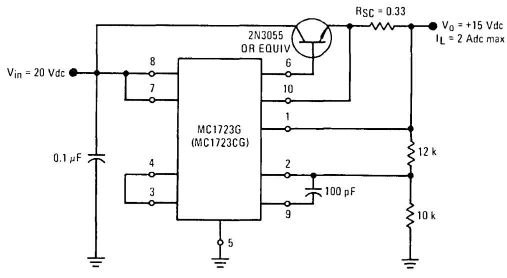
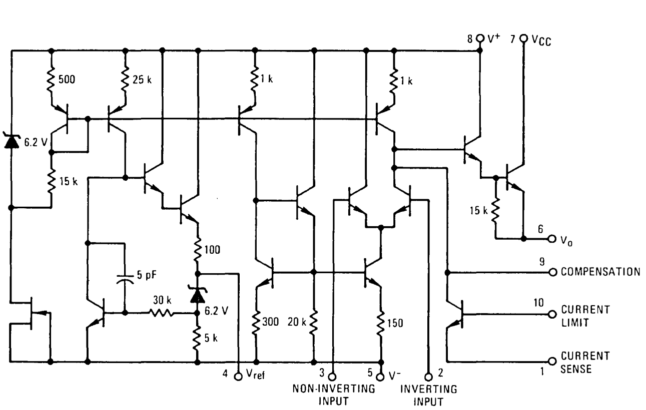
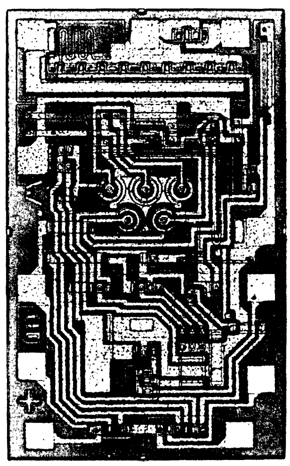


FIGURE 3 – CIRCUIT SCHEMATIC





See Packaging Information Section for outline dimensions.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Pulse Voltage from V^+ to V^- (50 ms) MC1723	$V_{in(p)}$	50	V_{peak}
Continuous Voltage from V^+ to V^-	V_{in}	40	Vdc
Input-Output Voltage Differential	$V_{in}-V_o$	40	Vdc
Maximum Output Current	I_L	150	mAdc
Current from V_{ref}	I_{ref}	15	mAdc
Power Dissipation and Thermal Characteristics			
T_A = +25°C	P_D	0.8	Watt
Derate above T_A = +25°C	$1/\theta_{JA}$	6.8	mW/°C
Thermal Resistance, Junction to Air	θ_{JA}	5.44	°C/W
T_C = +25°C	P_D	1.8	Watts
Derate above T_A = +25°C	$1/\theta_{JC}$	14.4	mW/°C
Thermal Resistance, Junction to Case	θ_{JC}	69.4	°C/W
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	°C

OPERATING TEMPERATURE RANGE

Ambient Temperature	T_A		°C
MC1723CG		0 to +75	
MC1723G		-55 to +125	

ELECTRICAL CHARACTERISTICS (Unless otherwise noted: T_A = +25°C, V_{in} = 12 Vdc, V_o = 5 Vdc, I_L = 1 mAdc, R_{SC} = 0, C1 = 100 pF, C_{ref} = 0 and divider impedance as seen by the error amplifier ≤ 10 kΩ connected as shown in Figure 1)

Characteristic	Symbol	MC1723			MC1723C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Voltage Range	V_{in}	9.5	–	40	9.5	–	40	Vdc
Output Voltage Range	V_o	2.0	–	37	2.0	–	37	Vdc
Input-Output Voltage Differential	$V_{in}-V_o$	3.0	–	38	3.0	–	38	Vdc
Reference Voltage	V_{ref}	6.95	7.15	7.35	6.80	7.15	7.50	Vdc
Standby Current Drain (I_L = 0, V_{in} = 30 V)	I_b	–	2.3	3.5	–	2.3	4.0	mAdc
Output Noise Voltage (f = 100 Hz to 10 kHz)	V_n							µV(rms)
C_{ref} = 0		–	20	–	–	20	–	
C_{ref} = 5.0 µF		–	2.5	–	–	2.5	–	
Average Temperature Coefficient of Output Voltage T_{low} ① < T_A < T_{high} ②	TCV_o	–	0.002	0.015	–	0.003	0.015	%/°C
Line Regulation	Reg_{in}							% V_o
(T_A = +25°C) 12 V < V_{in} < 15 V		–	0.01	0.1	–	0.01	0.1	
(T_A = +25°C) 12 V < V_{in} < 40 V		–	0.02	0.2	–	0.1	0.5	
(T_{low} ① < T_A < T_{high} ②) 12 V < V_{in} < 15 V		–	–	0.3	–	–	0.3	
Load Regulation (1.0 mA < I_L < 50 mA)	Reg_{load}							% V_o
T_A = +25°C		–	0.03	0.15	–	0.03	0.2	
T_{low} ① < T_A < T_{high} ②		–	–	0.6	–	–	0.6	
Ripple Rejection (f = 50 Hz to 10 kHz)	Rej_R							dB
C_{ref} = 0		–	74	–	–	74	–	
C_{ref} = 5.0 µF		–	86	–	–	86	–	
Short Circuit Current Limit (R_{SC} = 10 Ω, V_o = 0)	I_{SC}	–	65	–	–	65	–	mAdc
Long Term Stability	$\Delta V_o/\Delta t$	–	0.1	–	–	0.1	–	%/1000 hrs.

① T_{low} = 0°C for MC1723CG
= -55°C for MC1723G

② T_{high} = +75°C for MC1723CG
= +125°C for MC1723G

TYPICAL CHARACTERISTICS

(V_{in} = 12 Vdc, V_O = 5.0 Vdc, I_L = 1.0 mAdc, R_{SC} = 0, T_A = +25°C unless otherwise noted)

FIGURE 4 – MAXIMUM LOAD CURRENT AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL

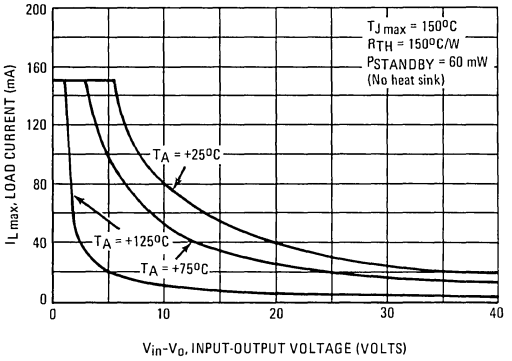


FIGURE 5 – LOAD REGULATION CHARACTERISTICS WITHOUT CURRENT LIMITING

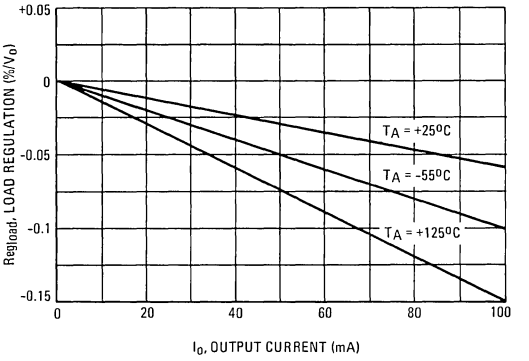


FIGURE 6 – LOAD REGULATION CHARACTERISTICS WITH CURRENT LIMITING

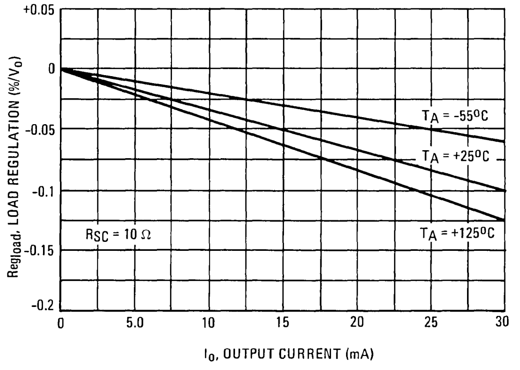


FIGURE 7 – LOAD REGULATION CHARACTERISTICS WITH CURRENT LIMITING

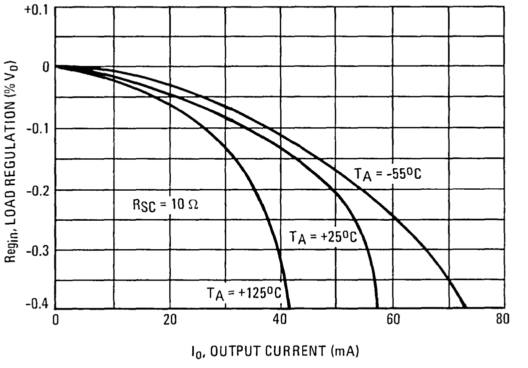


FIGURE 8 – CURRENT LIMITING CHARACTERISTICS

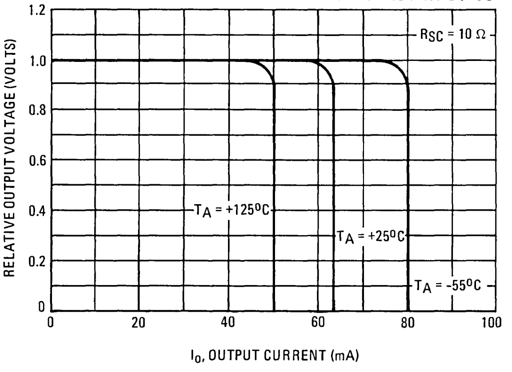
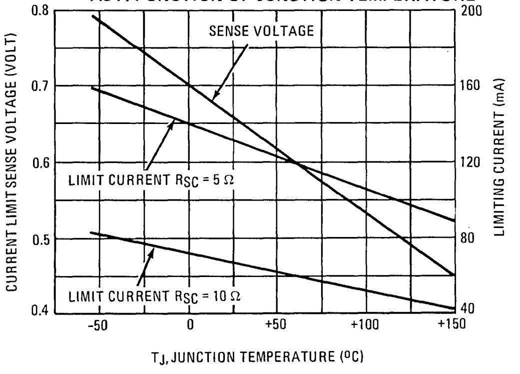


FIGURE 9 – CURRENT LIMITING CHARACTERISTICS AS A FUNCTION OF JUNCTION TEMPERATURE



TYPICAL CHARACTERISTICS (continued)

FIGURE 10 – LINE REGULATION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL

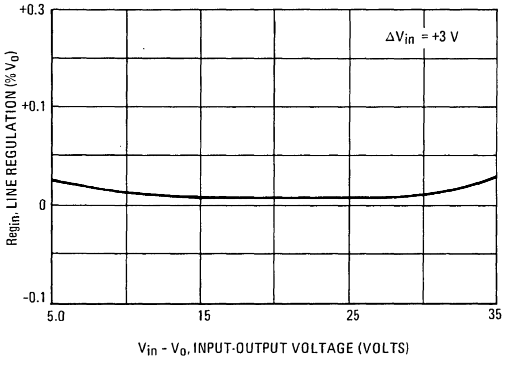


FIGURE 11 – LOAD REGULATION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL

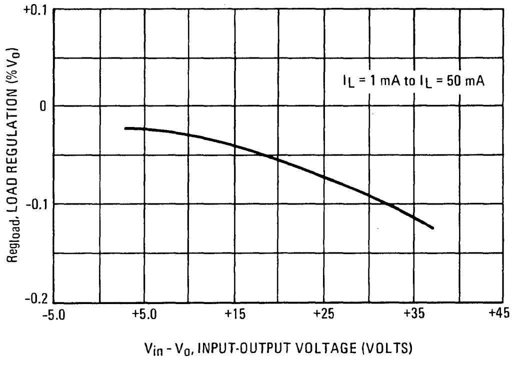


FIGURE 12 – STANDBY CURRENT DRAIN AS A FUNCTION OF INPUT VOLTAGE

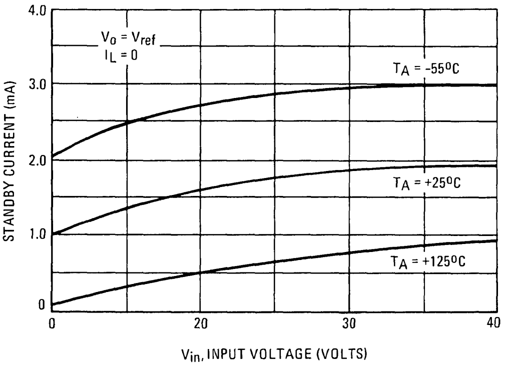


FIGURE 13 – LINE TRANSIENT RESPONSE

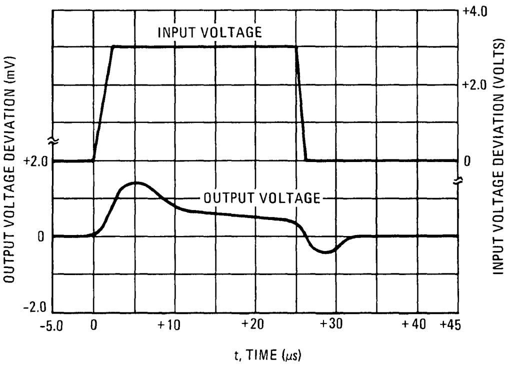


FIGURE 14 – LOAD TRANSIENT RESPONSE

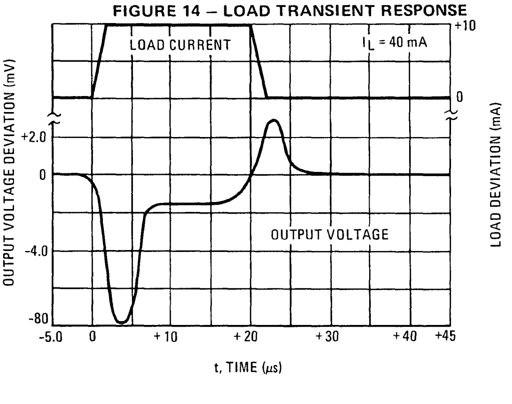
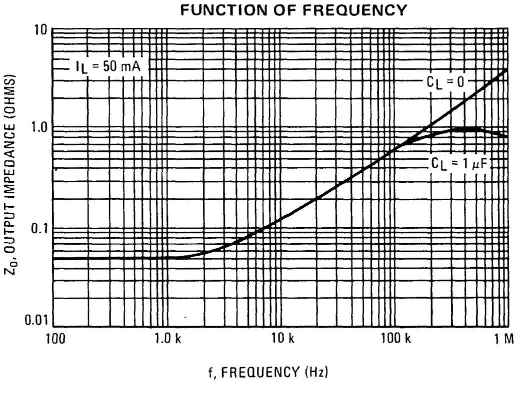
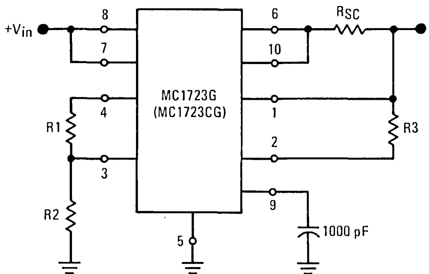


FIGURE 15 – OUTPUT IMPEDANCE AS FUNCTION OF FREQUENCY



TYPICAL APPLICATIONS

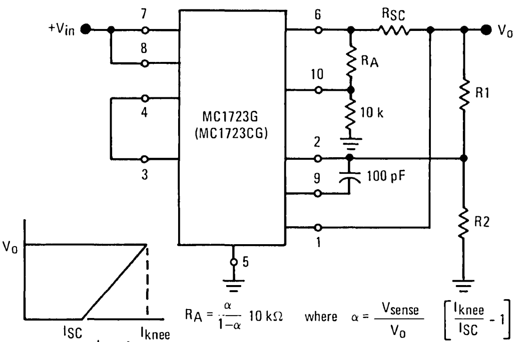
FIGURE 16 – TYPICAL CONNECTION FOR $2<V_O<7$



$V_O \cong 7\left[\frac{R2}{R1+R2}\right]$ $I_{SC} = \frac{V_{sense}}{R_{SC}} \cong \frac{0.66}{R_{SC}}$ at $T_J = +25^oC$

For best results 10 k < R1 + R2 < 100 k.
For minimum drift R3 = R1||R2.

FIGURE 17 – MC1723,C FOLDBACK CONNECTION



$R_A = \frac{\alpha}{1-\alpha}\ 10\ k\Omega$ where $\alpha = \frac{V_{sense}}{V_o}\left[\frac{I_{knee}}{I_{SC}} - 1\right]$

$R_{SC} = \frac{V_{sense}}{(1-\alpha)\,I_{SC}}$

FIGURE 18 – +5 V, 1-AMPERE SWITCHING REGULATOR

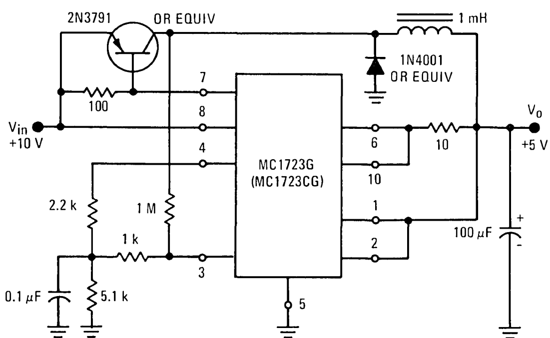


FIGURE 19 – +5 V, 1-AMPERE HIGH EFFICIENCY REGULATOR

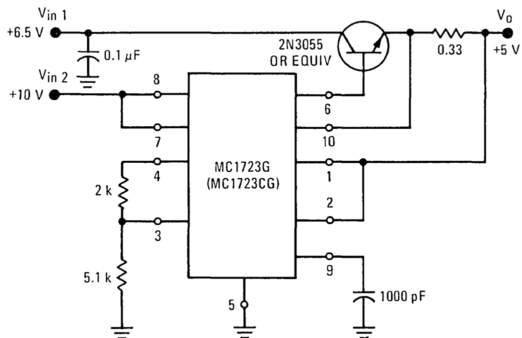


FIGURE 20 – +15 V, 1-AMPERE REGULATOR WITH REMOTE SENSE

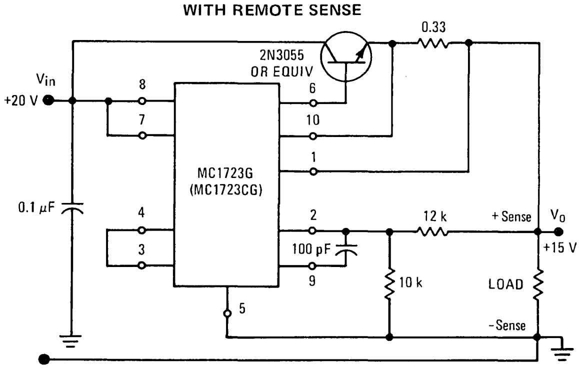
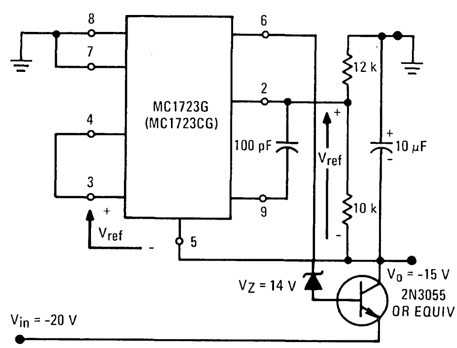
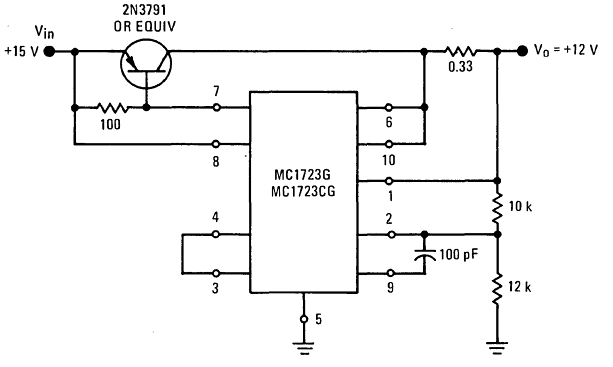


FIGURE 21 – -15 V NEGATIVE REGULATOR



TYPICAL APPLICATIONS (continued)

FIGURE 22 – +12 V, 1-AMPERE REGULATOR USING PNP CURRENT BOOST



See current MCC1723/1723C data sheet for standard linear chip information.

POSITIVE VOLTAGE REGULATORS

MC1723L
MC1723CL

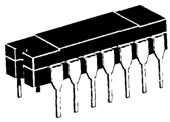
MONOLITHIC VOLTAGE REGULATOR

The MC1723 is a positive or negative voltage regulator designed to deliver load current to 150 mAdc. Output current capability can be increased to several amperes through use of one or more external pass transistors. MC1723 is specified for operation over the military temperature range (-55°C to +125°C) and the MC1723C over the commercial temperature range (0 to +75°C).

- Output Voltage Adjustable from 2 Vdc to 37 Vdc
- Output Current to 150 mAdc Without External Pass Transistors
- 0.01% Line and 0.03% Load Regulation
- Adjustable Short-Circuit Protection

VOLTAGE REGULATOR

MONOLITHIC SILICON EPITAXIAL PASSIVATED INTEGRATED CIRCUIT



CERAMIC PACKAGE
CASE 632

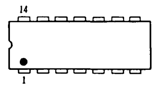
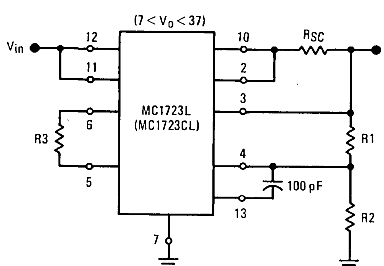


FIGURE 1 – TYPICAL CIRCUIT CONNECTION



$V_O \cong 7\left(\frac{R1 + R2}{R2}\right)$ $\quad I_{SC} = \frac{V_{sense}}{R_{SC}} = \frac{0.66}{R_{SC}}$ at $T_J = 25°C$

For best results $10\ k < R2 < 100\ k$
For minimum drift $R3 = R1 \| R2$

FIGURE 2 – TYPICAL NPN CURRENT BOOST CONNECTION

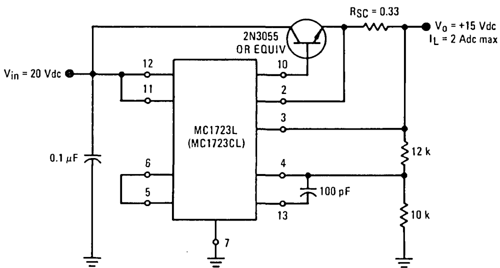
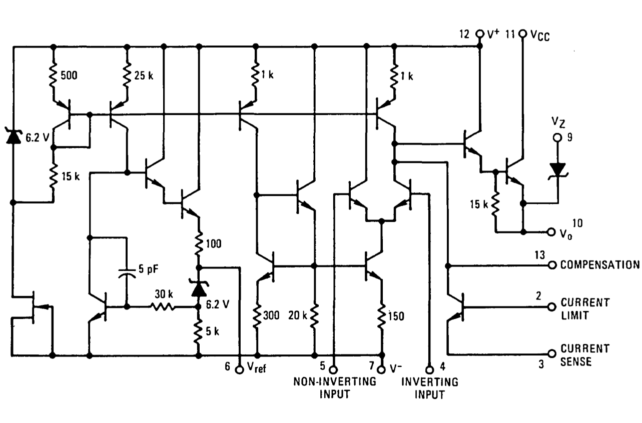
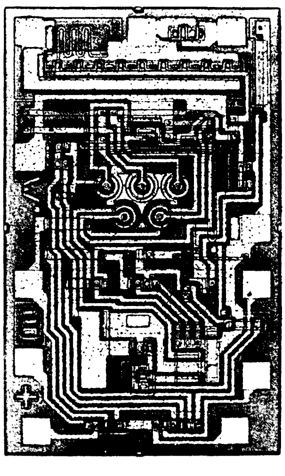


FIGURE 3 – CIRCUIT SCHEMATIC





This is advance information on a new introduction and specifications are subject to change without notice.
See Packaging Information Section for outline dimensions.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Pulse Voltage from V^+ to V^- (50 ms) MC1723L	$V_{in(p)}$	50	V_{peak}
Continuous Voltage from V^+ to V^-	V_{in}	40	Vdc
Input-Output Voltage Differential	$V_{in}-V_o$	40	Vdc
Maximum Output Current	I_L	150	mAdc
Current from V_{ref}	I_{ref}	15	mAdc
Power Dissipation and Thermal Characteristics			
Dual In-Line Ceramic Package	P_D	1.0	Watt
Derate above T_A = +25°C	$1/\theta_{JA}$	6.7	mW/°C
Thermal Resistance, Junction to Air	θ_{JA}	150	°C/W
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +175	°C

OPERATING TEMPERATURE RANGE

Ambient Temperature	T_A		°C
MC1723CL		0 to +75	
MC1723L		-55 to +125	

ELECTRICAL CHARACTERISTICS (Unless otherwise noted: T_A = +25°C, V_{in} = 12 Vdc, V_o = 5 Vdc, I_L = 1 mAdc, R_{SC} = 0, C1 = 100 pF, C_{ref} = 0 and divider impedance as seen by the error amplifier ≤ 10 kΩ connected as shown in Figure 1)

Characteristic	Symbol	MC1723			MC1723C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Voltage Range	V_{in}	9.5	–	40	9.5	–	40	Vdc
Output Voltage Range	V_o	2.0	–	37	2.0	–	37	Vdc
Input-Output Voltage Differential	$V_{in}-V_o$	3.0	–	38	3.0	–	38	Vdc
Reference Voltage	V_{ref}	6.95	7.15	7.35	6.80	7.15	7.50	Vdc
Standby Current Drain (I_L = 0, I_{ref} = 0, V_{in} = 30 V)	I_b	–	2.3	3.5	–	2.3	4.0	mAdc
Output Noise Voltage (f = 100 Hz to 10 kHz)	V_n							µV(rms)
C_{ref} = 0		–	20	–	–	20	–	
C_{ref} = 5.0 µF		–	2.5	–	–	2.5	–	
Average Temperature Coefficient of Output Voltage T_{low} ① < T_A < T_{high} ②	TCV_o	–	0.002	0.015	–	0.003	0.015	%/°C
Line Regulation	Reg_{in}							% V_o
(T_A = +25°C) 12 V < V_{in} < 15 V		–	0.01	0.1	–	0.01	0.1	
(T_A = +25°C) 12 V < V_{in} < 40 V		–	0.02	0.2	–	0.1	0.5	
(T_{low} ① < T_A < T_{high} ②) 12 V < V_{in} < 15 V		–	–	0.3	–	–	0.3	
Load Regulation (1.0 mA < I_L < 50 mA)	Reg_{load}							% V_o
T_A = +25°C		–	0.03	0.15	–	0.03	0.2	
T_{low} ① < T_A < T_{high} ②		–	–	0.6	–	–	0.6	
Ripple Rejection (f = 50 Hz to 10 kHz)	Rej_R							dB
C_{ref} = 0		–	74	–	–	74	–	
C_{ref} = 5.0 µF		–	86	–	–	86	–	
Short Circuit Current Limit (R_{SC} = 10 Ω, V_o = 0)	I_{SC}	–	65	–	–	65	–	mAdc
Long Term Stability	$\Delta V_o/\Delta t$	–	0.1	–	–	0.1	–	%/1000 hrs.

① T_{low} = 0°C for MC1723CL
= -55°C for MC1723L

② T_{high} = +75°C for MC1723CL
= +125°C for MC1723L

See current MCC1723/1723C data sheet for standard linear chip information.

MC1733
MC1733C

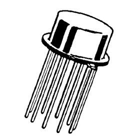
MONOLITHIC DIFFERENTIAL VIDEO AMPLIFIER

. . . a wideband amplifier with differential input and differential output. Gain is fixed at 10, 100, or 400 without external components or, with the addition of one external resistor, gain becomes adjustable from 10 to 400.

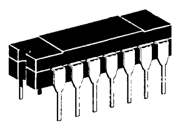
- Bandwidth — 120 MHz typical @ A_{vd} = 10
- Rise Time — 2.5 ns typical @ A_{vd} = 10
- Propagation Delay Time — 3.6 ns typical @ A_{vd} = 10

DIFFERENTIAL VIDEO WIDEBAND AMPLIFIER

MONOLITHIC SILICON INTEGRATED CIRCUIT



G SUFFIX
METAL PACKAGE
CASE 603-02
TO-100



L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

FIGURE 1 — BASIC CIRCUIT

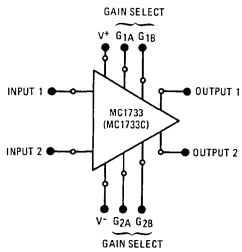


FIGURE 2 — VOLTAGE GAIN ADJUST CIRCUIT

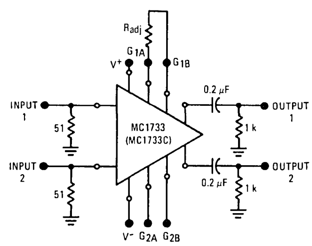
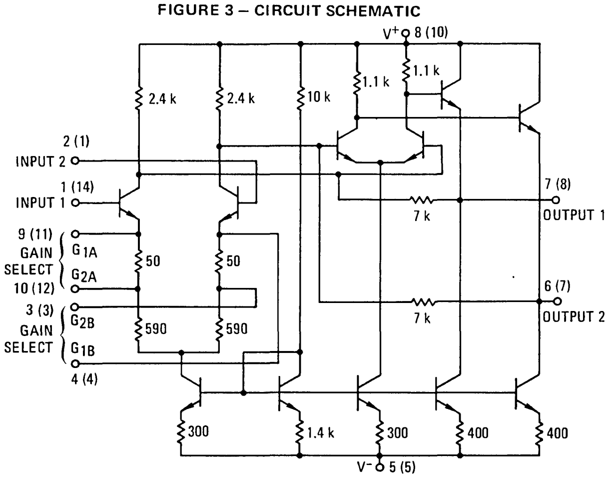
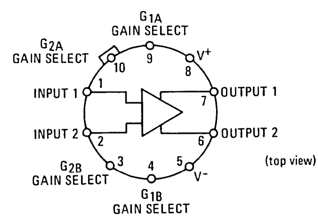


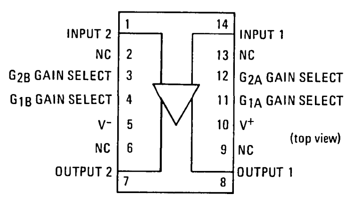
FIGURE 3 — CIRCUIT SCHEMATIC



CONNECTION DIAGRAMS



G SUFFIX, METAL PACKAGE
Pin 5 connected to case.



L SUFFIX, CERAMIC PACKAGE

See Packaging Information Section for outline dimensions.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+ V^-	+8.0 -8.0	Volts
Differential Input Voltage	V_{in}	±5.0	Volts
Common-Mode Input Voltage	CMV_{in}	±6.0	Volts
Output Current	I_o	10	mA
Internal Power Dissipation (Note 1) Metal Can Package Ceramic Dual In-Line Package	P_D	 500 500	mW
Operating Temperature Range MC1733C MC1733	T_A	0 to +75 -55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V^+ = +6.0 Vdc, V^- = -6.0 Vdc, at T_A = +25°C unless otherwise noted)

		MC1733			MC1733C			
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Differential Voltage Gain Gain 1 (Note 2) Gain 2 (Note 3) Gain 3 (Note 4)	A_{vd}	 300 90 9.0	 400 100 10	 500 110 11	 250 80 8.0	 400 100 10	 600 120 12	
Bandwidth (R_s = 50 Ω) Gain 1 Gain 2 Gain 3	BW	 – – –	 40 90 120	 – – –	 – – –	 40 90 120	 – – –	MHz
Rise Time (R_s = 50 Ω, V_o = 1 Vp-p) Gain 1 Gain 2 Gain 3	t_r	 – – –	 10.5 4.5 2.5	 – 10 –	 – – –	 10.5 4.5 2.5	 – 12 –	ns
Propagation Delay (R_s = 50 Ω, V_o = 1 Vp-p) Gain 1 Gain 2 Gain 3	t_{pd}	 – – –	 7.5 6.0 3.6	 – 10 –	 – – –	 7.5 6.0 3.6	 – 10 –	ns
Input Resistance Gain 1 Gain 2 Gain 3	R_{in}	 – 20 –	 4.0 30 250	 – – –	 – 10 –	 4.0 30 250	 – – –	kΩ
Input Capacitance (Gain 2)	C_{in}	–	2.0	–	–	2.0	–	pF
Input Offset Current	$\|I_{io}\|$	–	0.4	3.0	–	0.4	5.0	μA
Input Bias Current	I_b	–	9.0	20	–	9.0	30	μA
Input Noise Voltage (R_s = 50 Ω, BW = 1 kHz to 10 MHz)	V_n	–	12	–	–	12	–	μV(rms)
Input Voltage Range	V_{in}	±1.0	–	–	±1.0	–	–	V
Common-Mode Rejection Ratio Gain 2 (V_{CM} = ±1 V, f ≤ 100 kHz) Gain 2 (V_{CM} = ±1 V, f = 5 MHz)	CM_{rej}	 60 –	 86 60	 – –	 60 –	 86 60	 – –	dB
Supply Voltage Rejection Ratio Gain 2 (ΔV_s = ±0.5 V)	S^+, S^-	 50	 70	 –	 50	 70	 –	dB
Output Offset Voltage Gain 1 Gain 2 and Gain 3	V_{oo}	 – –	 0.6 0.35	 1.5 1.0	 – –	 0.6 0.35	 1.5 1.5	V
Output Common-Mode Voltage	CMV_o	2.4	2.9	3.4	2.4	2.9	3.4	V
Output Voltage Swing	V_o	3.0	4.0	–	3.0	4.0	–	Vp-p
Output Sink Current	I_o	2.5	3.6	–	2.5	3.6	–	mA
Output Resistance	R_{out}	–	20	–	–	20	–	Ω
Power Supply Current	I_D	–	18	24	–	18	24	mA

NOTES

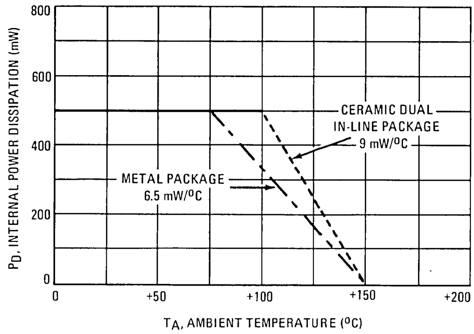
Note 1: Derate metal package at 6.5 mW/°C for operation at ambient temperatures above 75°C and dual in-line package at 9 mW/°C for operation at ambient temperatures above 100°C (see Figure 4). If operation at high ambient temperatures is required (MC1733) a heatsink may be necessary to limit maximum junction temperature to 150°C. Thermal resistance, junction-to-case, for the metal package is 69.4°C per Watt.

Note 2: Gain Select pins G_{1A} and G_{1B} connected together.

Note 3: Gain Select pins G_{2A} and G_{2B} connected together.

Note 4: All Gain Select pins open.

FIGURE 4 – MAXIMUM ALLOWABLE POWER DISSIPATION



TYPICAL CHARACTERISTICS

(V^+ = +6.0 Vdc, V^- = −6.0 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 5 – SUPPLY CURRENT versus TEMPERATURE

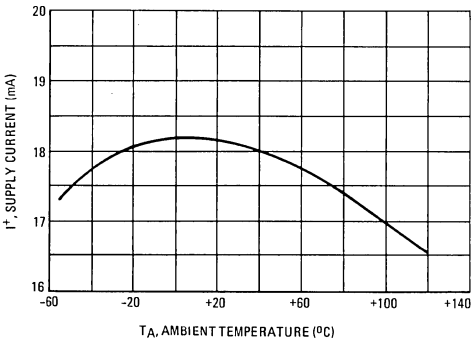
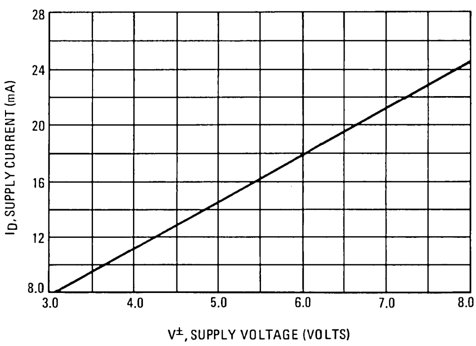


FIGURE 6 – SUPPLY CURRENT versus SUPPLY VOLTAGE



TYPICAL CHARACTERISTICS (continued)

(V^+ = +6.0 Vdc, V^- = -6.0 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 7 – GAIN verus TEMPERATURE

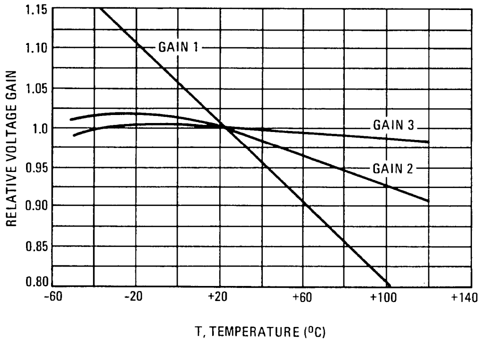


FIGURE 8 – GAIN versus FREQUENCY

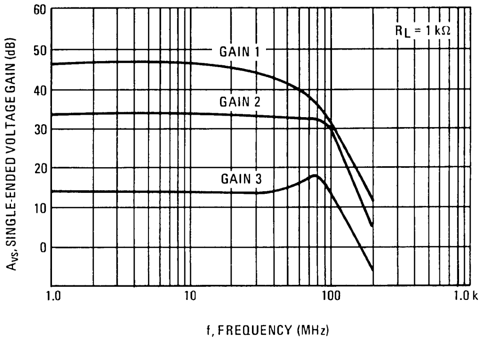


FIGURE 9 – GAIN versus SUPPLY VOLTAGE

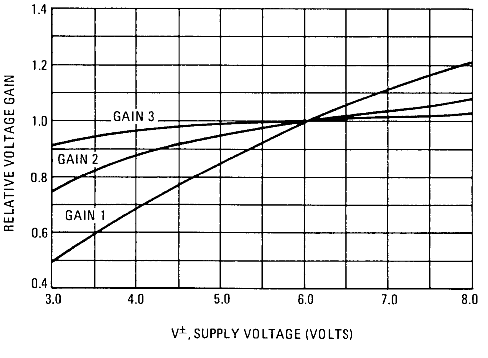


FIGURE 10 – GAIN versus R_{ADJUST}

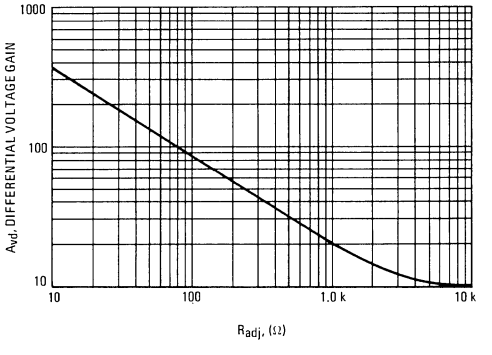


FIGURE 11 – GAIN versus FREQUENCY and SUPPLY VOLTAGE

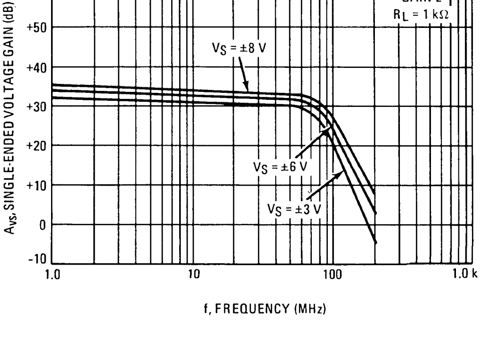
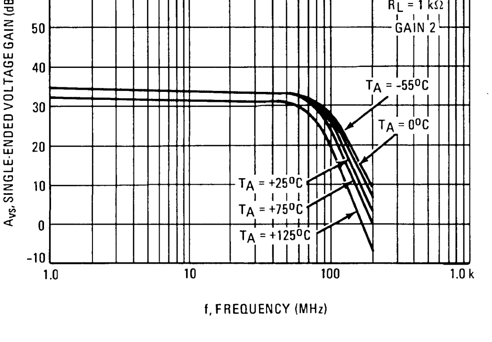


FIGURE 12 – GAIN versus FREQUENCY and TEMPERATURE



TYPICAL CHARACTERISTICS (continued)

(V^+ = +6.0 Vdc, V^- = -6.0 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 13 – PULSE RESPONSE versus GAIN

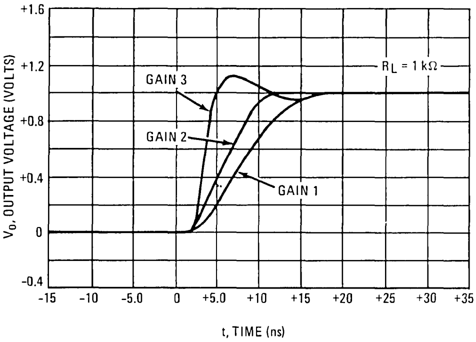


FIGURE 14 – PULSE RESPONSE versus SUPPLY VOLTAGE

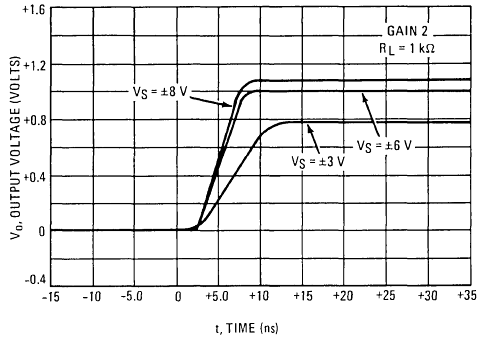


FIGURE 15 – PULSE RESPONSE versus TEMPERATURE

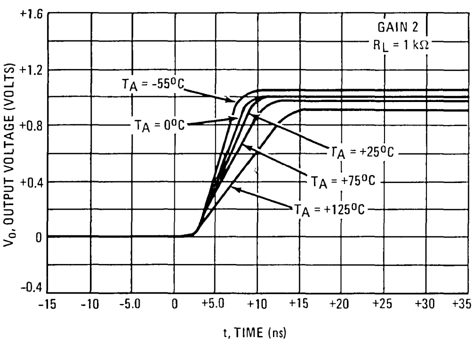


FIGURE 16 – DIFFERENTIAL OVERDRIVE RECOVERY TIME

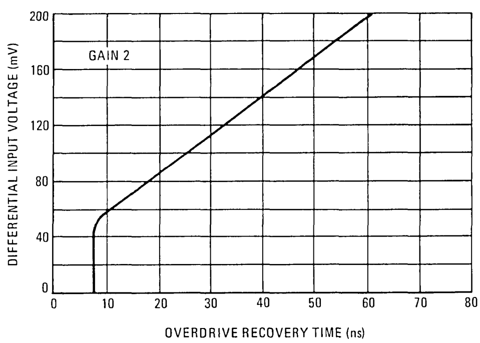


FIGURE 17 – PHASE SHIFT versus FREQUENCY

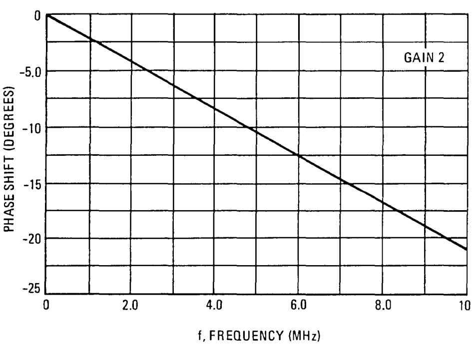
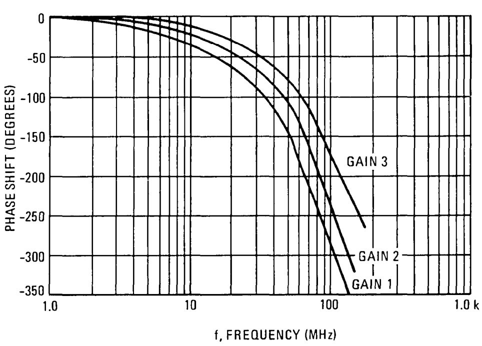


FIGURE 18 – PHASE SHIFT versus FREQUENCY



TYPICAL CHARACTERISTICS (continued)

(V^+ = +6.0 Vdc, V^- = -6.0 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 19 – INPUT RESISTANCE versus TEMPERATURE

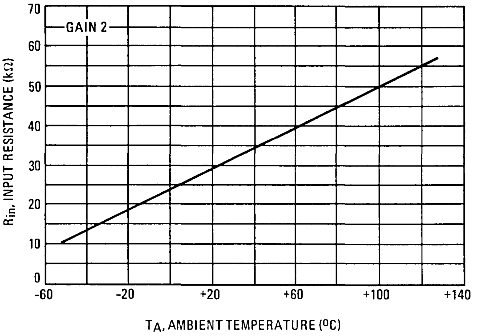


FIGURE 20 – INPUT NOISE VOLTAGE

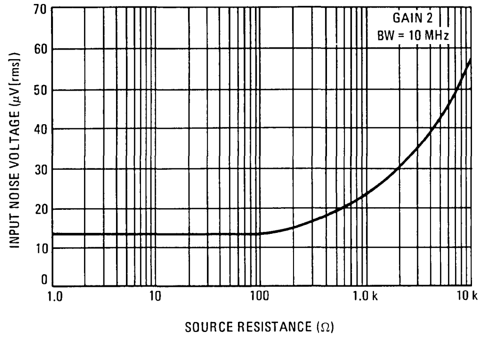


FIGURE 21 – OUTPUT VOLTAGE SWING and SINK CURRENT versus SUPPLY VOLTAGE

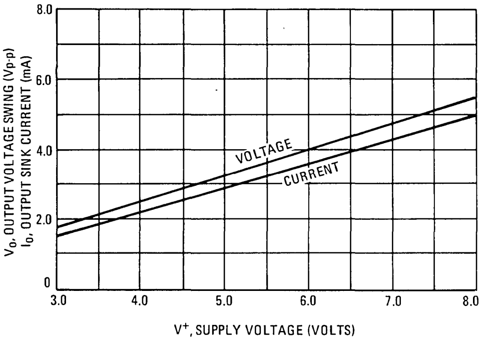


FIGURE 22 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

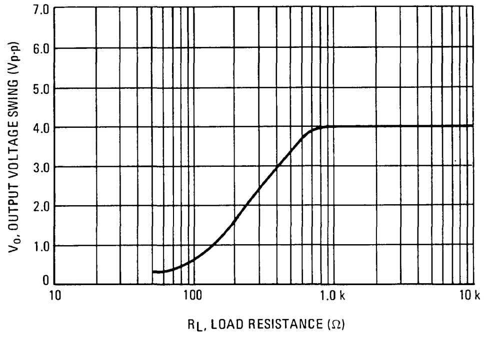


FIGURE 23 – OUTPUT VOLTAGE SWING versus FREQUENCY

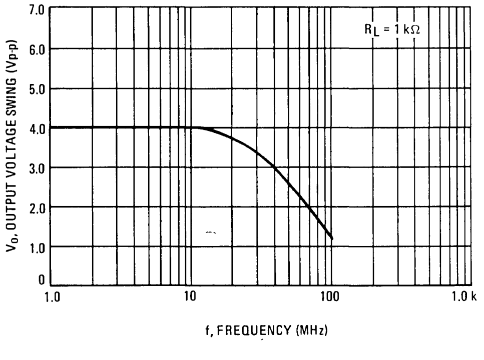
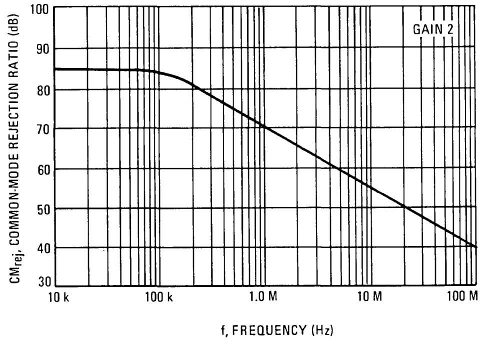


FIGURE 24 – COMMON-MODE REJECTION RATIO



MC1741
MC1741C

OPERATIONAL AMPLIFIERS

INTERNALLY COMPENSATED, HIGH PERFORMANCE MONOLITHIC OPERATIONAL AMPLIFIER

. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

- No Frequency Compensation Required
- Short-Circuit Protection
- Offset Voltage Null Capability
- Wide Common-Mode and Differential Voltage Ranges
- Low-Power Consumption
- No Latch Up

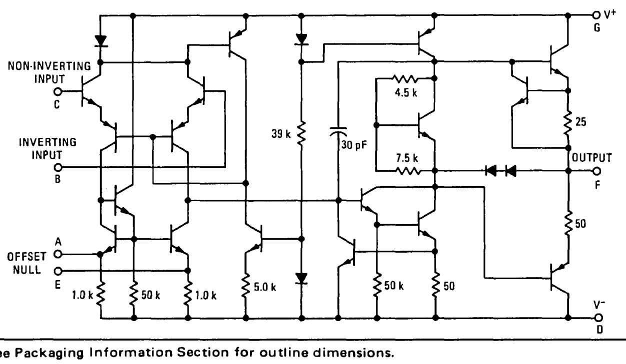
MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value		Unit
		MC1741C	MC1741	
Power Supply Voltage	V^+ V^-	+18 -18	+22 -22	Vdc Vdc
Differential Input Signal	V_{in}	±30		Volts
Common Mode Input Swing (Note 1)	CMV_{in}	±15		Volts
Output Short Circuit Duration (Note 2)	t_S	Continuous		
Power Dissipation (Package Limitation)	P_D			
Metal Can		680		mW
Derate above T_A = +25°C		4.6		mW/°C
Flat Package		500		mW
Derate above T_A = +25°C		3.3		mW/°C
Plastic Dual In-Line Packages		625		mW
Derate above T_A = +25°C		5.0		mW/°C
Ceramic Dual In-Line Package		750		mW/°C
Derate above T_A = +25°C		6.0		mW/°C
Operating Temperature Range	T_A	0 to +75	-55 to +125	°C
Storage Temperature Range	T_{stg}			°C
Metal, Flat and Ceramic Packages		-65 to +150		
Plastic Package		-55 to +125		

Note 1. For supply voltages less than ± 15 V, the absolute maximum input voltage is equal to the supply voltage.

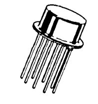
Note 2. Supply voltage equal to or less than 15 V.

CIRCUIT SCHEMATIC

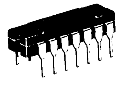


See Packaging Information Section for outline dimensions.

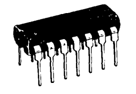
OPERATIONAL AMPLIFIER
MONOLITHIC SILICON INTEGRATED CIRCUIT



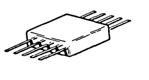
G SUFFIX
METAL PACKAGE
CASE 601
TO-99



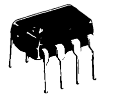
L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116



P2 SUFFIX
PLASTIC PACKAGE
CASE 605
TO-116
(MC1741C only)



F SUFFIX
CERAMIC PACKAGE
CASE 606
TO-91

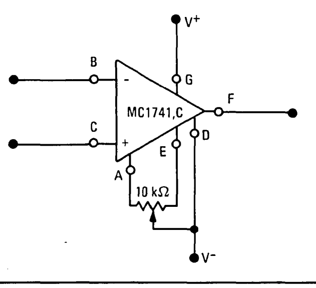


P1 SUFFIX
PLASTIC PACKAGE
CASE 626
(MC1741C only)

PIN CONNECTIONS

Schematic	A	B	C	D	E	F	G
"G" & "P1" Packages	1	2	3	4	5	6	7
"F" Package	2	3	4	5	6	7	8
"P2" & "L" Packages	3	4	5	6	9	10	11

FIGURE 1 – OFFSET ADJUST CIRCUIT



MC1741, MC1741C (continued)

ELECTRICAL CHARACTERISTICS (V^+ = +15 Vdc, V^- = 15 Vdc, T_A = +25°C unless otherwise noted)

Characteristic	Symbol	MC1741 Min	MC1741 Typ	MC1741 Max	MC1741C ④ Min	MC1741C ④ Typ	MC1741C ④ Max	Unit
Open Loop Voltage Gain (R_L = 2.0 kΩ) (V_o = ± 10 V, T_A = +25°C)	A_{VOL}	50,000	200,000	–	20,000	100,000	–	–
(V_o = ± 10 V, T_A = T_{low} ① to T_{high} ②)		25,000	–	–	15,000	–	–	
Output Impedance (f = 20 Hz)	Z_o	–	75	–	–	75	–	Ω
Input Impedance (f = 20 Hz)	Z_{in}	0.3	1.0	–	0.3	1.0	–	Meg Ω
Output Voltage Swing	V_o							V_{peak}
(R_L = 10 kΩ, T_A = +25°C)		±12	±14	–	±12	±14	–	
(R_L = 2.0 kΩ, T_A = +25°C)		±10	±13	–	±10	±13	–	
(R_L = 2.0 kΩ, T_A = T_{low} ① to T_{high} ②)		±10	–	–	±10	–	–	
Input Common-Mode Voltage Swing	CMV_{in}	±12	±13	–	±12	±13	–	V_{peak}
Common-Mode Rejection Ratio (f = 20 Hz)	CM_{rej}	70	90	–	70	90	–	dB
Input Bias Current	I_b							μA
(T_A = +25°C)		–	0.2	0.5	–	0.2	0.5	
(T_A = T_{low} ①)		–	0.5	1.5	–	–	0.8	
Input Offset Current	$\|I_{io}\|$							μA
(T_A = +25°C)		–	0.03	0.2	–	0.03	0.2	
(T_A = T_{low} ① to T_{high} ②)		–	–	0.5	–	–	0.3	
Input Offset Voltage (R_S = ≦ 10 kΩ)	$\|V_{io}\|$							mV
(T_A = +25°C)		–	1.0	5.0	–	2.0	6.0	
(T_A = T_{low} ① to T_{high} ②)		–	–	6.0	–	–	7.5	
Step Response Gain = 100, R_1 = 1.0 kΩ, R_2 = 100 kΩ, R_3 = 1.0 kΩ	t_f	–	29	–	–	29	–	μs
	t_{pd}	–	8.5	–	–	8.5	–	μs
	dV_{out}/dt ③	–	1.0	–	–	1.0	–	V/μs
Gain = 10, R_1 = 1.0 kΩ, R_2 = 10 kΩ, R_3 = 1.0 kΩ	t_f	–	3.0	–	–	3.0	–	μs
	t_{pd}	–	1.0	–	–	1.0	–	μs
	dV_{out}/dt ③	–	1.0	–	–	1.0	–	V/μs
Gain = 1, R_1 = 10 kΩ, R_2 = 10 kΩ, R_3 = 5.0 kΩ	t_f	–	0.6	–	–	0.6	–	μs
	t_{pd}	–	0.38	–	–	0.38	–	μs
	dV_{out}/dt ③	–	0.8	–	–	0.8	–	V/μs
Average Temperature Coefficient of Input Offset Voltage	$\|TC_{Vio}\|$							μV/°C
(R_S = 50 Ω, T_A = T_{low} ① to T_{high} ②)		–	3.0	–	–	3.0	–	
(R_S = 10 kΩ, T_A = T_{low} ① to T_{high} ②)		–	6.0	–	–	6.0	–	
Average Temperature Coefficient of Input Offset Current (T_A = T_{low} ① to T_{high} ②)	$\|TC_{Iio}\|$	–	50	–	–	50	–	pA/°C
DC Power Dissipation (Power Supply = ± 15 V, V_o = 0)	P_D	–	50	85	–	50	85	mW
Positive Supply Sensitivity (V^- constant)	S^+	–	30	150	–	30	150	μV/V
Negative Supply Sensitivity (V^+ constant)	S^-	–	30	150	–	30	150	μV/V
Power Bandwidth (A_V = 1, R_L = 2.0 kΩ, THD = 5%, V_o = 20 V_{p-p})	PBW	–	10	–	–	10	–	kHz

① T_{low} = 0°C for MC1741C = -55°C for MC1741

② T_{high} = +75°C for MC1741C = +125°C for MC1741

③ dV_{out}/dt = Slew Rate

④ Plastic package offered in limited temperature range only.

TYPICAL CHARACTERISTICS

(V^+ = +15 Vdc, V^- = -15 Vdc, T_A = +25°C unless otherwise noted)

FIGURE 2 – POWER BANDWIDTH (LARGE SIGNAL SWING versus FREQUENCY)

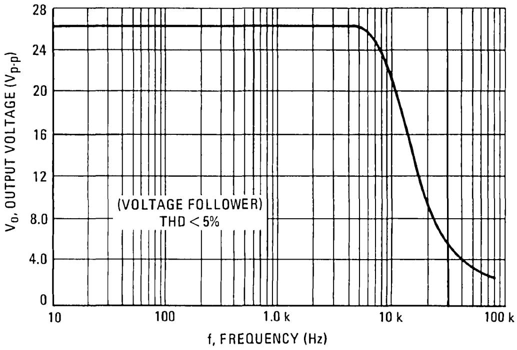


FIGURE 3 – OPEN LOOP FREQUENCY RESPONSE

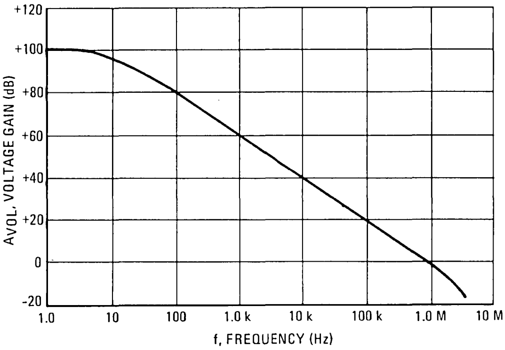


FIGURE 4 – OUTPUT NOISE versus SOURCE RESISTANCE

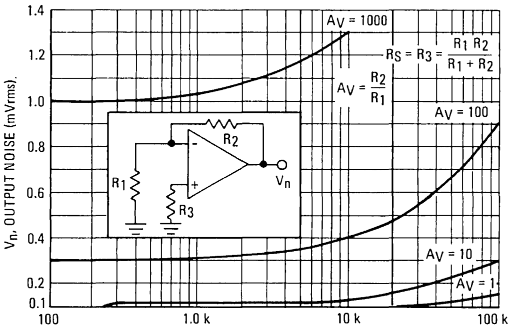


FIGURE 5 – INPUT OFFSET VOLTAGE versus TEMPERATURE

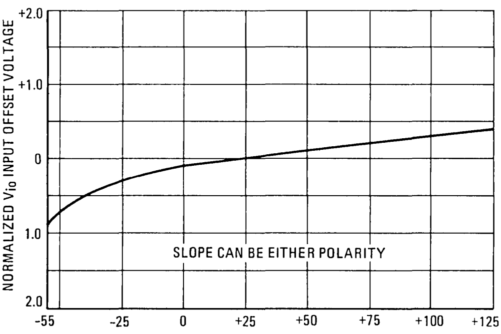


FIGURE 6 – INPUT OFFSET CURRENT versus TEMPERATURE

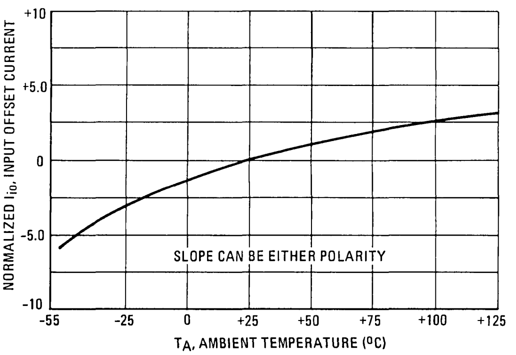


FIGURE 7 – INPUT BIAS CURRENT versus TEMPERATURE

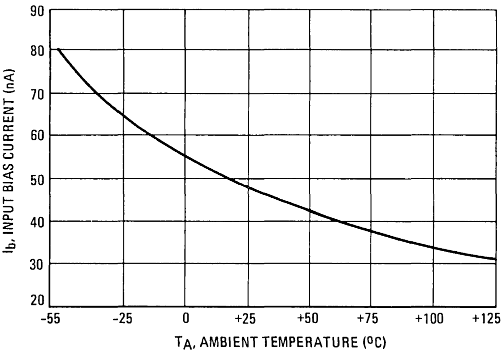


FIGURE 8 – POWER DISSIPATION versus POWER SUPPLY VOLTAGE

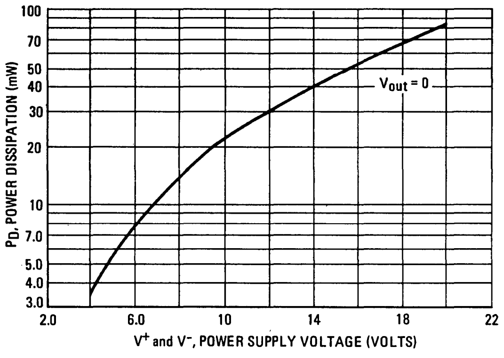


FIGURE 9 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

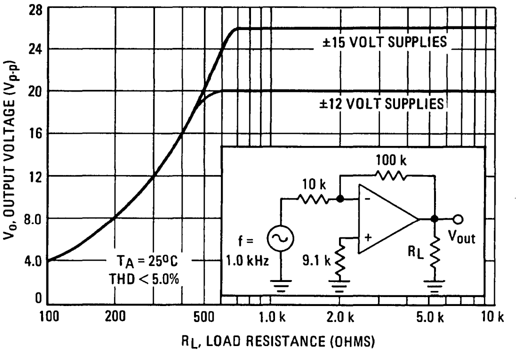
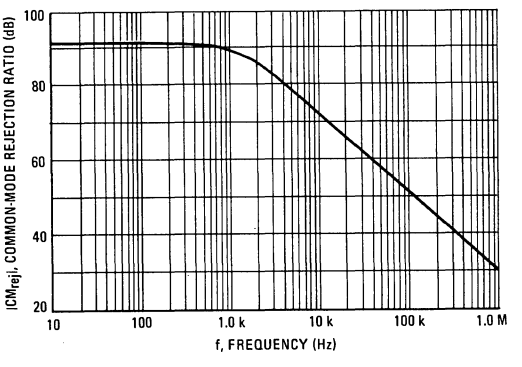


FIGURE 10 – COMMON-MODE REJECTION RATIO versus FREQUENCY



See current MCC1741/1741C data sheet for standard linear chip information.

OPERATIONAL AMPLIFIERS

MC1748G
MC1748CG

Advance Information

HIGH PERFORMANCE MONOLITHIC OPERATIONAL AMPLIFIER

. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

- Noncompensated MC1741G
- Single 30 pF Capacitor Compensation Required For Unity Gain
- Short-Circuit Protection
- Offset Voltage Null Capability
- Wide Common-Mode and Differential Voltage Ranges
- Low-Power Consumption
- No Latch Up

OPERATIONAL AMPLIFIER INTEGRATED CIRCUIT

MONOLITHIC SILICON EPITAXIAL PASSIVATED

METAL PACKAGE
CASE 601
TO-99

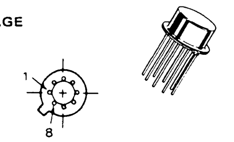


FIGURE 1 – POWER BANDWIDTH (LARGE SIGNAL SWING versus FREQUENCY)

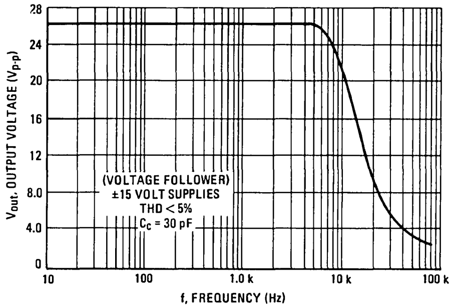


FIGURE 2 – OPEN LOOP FREQUENCY RESPONSE

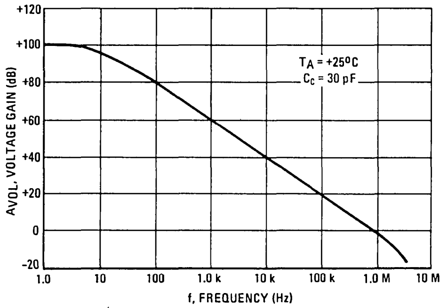


FIGURE 3 – CIRCUIT SCHEMATIC

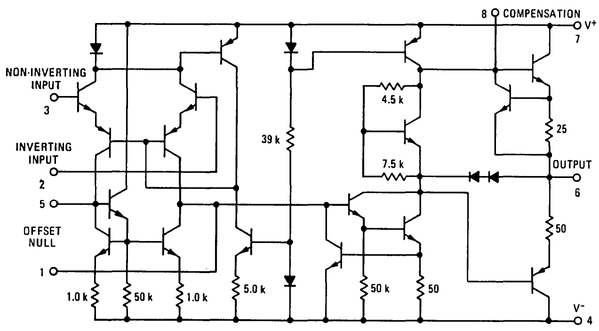
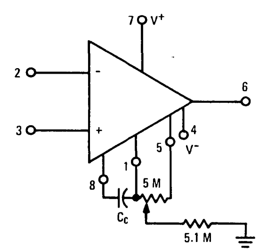


FIGURE 4 – OFFSET ADJUST AND FREQUENCY COMPENSATION



This is advance information and specifications are subject to change without notice.

See Packaging Information Section for outline dimensions.

See current MCC1748/1748C data sheet for standard linear chip information.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	MC1748G	MC1748CG	Unit
Power Supply Voltage	V^+ V^-	+22 -22	+18 -18	Vdc
Differential Input Signal	V_{in}	±30		Volts
Common-Mode Input Swing ①	CMV_{in}	±15		Volts
Output Short Circuit Duration	t_S	Continuous		
Power Dissipation (Package Limitation) Derate above T_A = +25°C	P_D	680 4.6		mW mW/°C
Operating Temperature Range	T_A	-55 to +125	0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V^+ = +15 Vdc, V^- = −15 Vdc, T_A = +25°C unless otherwise noted)

Characteristics	Symbol	MC1748G Min	MC1748G Typ	MC1748G Max	MC1748CG Min	MC1748CG Typ	MC1748CG Max	Unit
Input Bias Current	I_b							µAdc
T_A = +25°C		–	0.08	0.5	–	0.08	0.5	
T_A = T_{low} to T_{high} ②		–	0.3	1.5	–	–	0.8	
Input Offset Current	$\lvert I_{io}\rvert$							µAdc
T_A = +25°C		–	0.02	0.2	–	0.02	0.2	
T_A = T_{low} to T_{high}		–	0.08	0.5	–	–	0.3	
Input Offset Voltage ($R_S \leq 10$ k Ω)	$\lvert V_{io}\rvert$							mVdc
T_A = +25°C		–	1.0	5.0	–	1.0	6.0	
T_A = T_{low} to T_{high}		–	–	6.0	–	–	7.5	
Differential Input Impedance (Open-Loop, f = 20 Hz)								
Parallel Input Resistance	R_p	0.3	2.0	–	0.3	2.0	–	Megohm
Parallel Input Capacitance	C_p	–	1.4	–	–	1.4	–	pF
Common-Mode Input Impedance (f = 20 Hz)	$Z_{(in)}$	–	200	–	–	200		Megohms
Common-Mode Input Voltage Swing	CMV_{in}	±12	±13	–	±12	±13	–	V_{pk}
Common-Mode Rejection Ratio (f = 100 Hz)	CM_{rej}	70	90	–	70	90	–	dB
Open-Loop Voltage Gain, (V_O = ±10 V, R_L = 2.0 k ohms)	A_{VOL}							V/V
T_A = +25°C		50,000	200,000	–	20,000	200,000	–	
T_A = T_{low} to T_{high}		25,000	–	–	15,000	–	–	
Step Response (V_{in} = 20 mV, C_c = 30 pF, R_L = 2 kΩ, C_L = 100 pF)								
Rise Time	t_r	–	0.3	–	–	0.3	–	µs
Overshoot Percentage		–	5.0	–	–	5.0	–	%
Slew Rate	dV_{out}/dt	–	0.8	–	–	0.8	–	V/µs
Output Impedance (f = 20 Hz)	Z_{out}	–	75	–	–	75	–	ohms
Short-Circuit Output Current	I_{SC}	–	25	–	–	25	–	mAdc
Output Voltage Swing (R_L = 10 k ohms)	V_O	±12	±14	–	±12	±14	–	Vpk
R_L = 2 k ohms (T_A = T_{low} to t_{high})		±10	±13	–	±10	±13	–	
Power Supply Sensitivity								µV/V
V^- = constant, $R_s \leq 10$ k ohms	S+	–	30	150	–	30	150	
V^+ = constant, $R_s \leq 10$ k ohms	S-	–	30	150	–	30	150	
Power Supply Current	I_D^+	–	1.67	2.83	–	1.67	2.83	mAdc
	I_D^-	–	1.67	2.83	–	1.67	2.83	
DC Quiescent Power Dissipation	P_D							mW
(V_O = 0)		–	50	85	–	50	85	

① For supply voltages less than ±15 V, the Maximum Input Voltage is equal to the Supply Voltage.

② T_{low}: 0°C for MC1748CG
-55°C for MC1748G
T_{high}: +75°C for MC1748CG
+125°C for MC1748G

6

MC7520L thru MC7523L

DUAL SENSE AMPLIFIERS

Advance Information

MONOLITHIC DUAL SENSE AMPLIFIERS

These dual sense amplifiers are designed for high-speed core memory systems. Low-level pulses originating in the memory are converted to logic levels compatible with MTTL and MDTL circuits. Each of the two basic device functions has two different threshold specifications. The dual-input preamplifiers are connected to a common output stage, with each preamplifier output strobed independently.

The output circuit of the MC7520L/MC7521L is comprised of two cascaded NAND gates, each having an external gate input. The external gate inputs may be used to connect the $\bar{Q}$ output to the Gate Q input to achieve a flip-flop or register that responds to the sense and strobe input conditions. Output pulse stretching may be accomplished by resistive/capacitive coupling from the $\bar{Q}$ output to the Gate Q input.

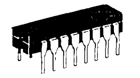
The output circuit of the MC7522L/MC7523L features an open-collector output, permitting the wired-OR function. Load resistor R_L may be used as the output pullup resistor.

- Adjustable Threshold Voltage Levels
- High Speed, Fast Recovery Time
- Time and Amplitude Signal Discrimination
- High dc Logic Noise Margin – 1.0 Volt typical
- Good Fanout Capability

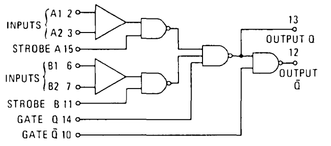
DUAL HIGH-SPEED SENSE AMPLIFIER INTEGRATED CIRCUITS

MONOLITHIC SILICON EPITAXIAL PASSIVATED

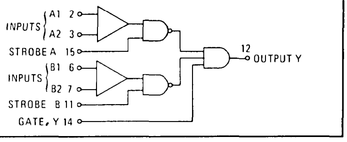
CERAMIC PACKAGE
CASE 620



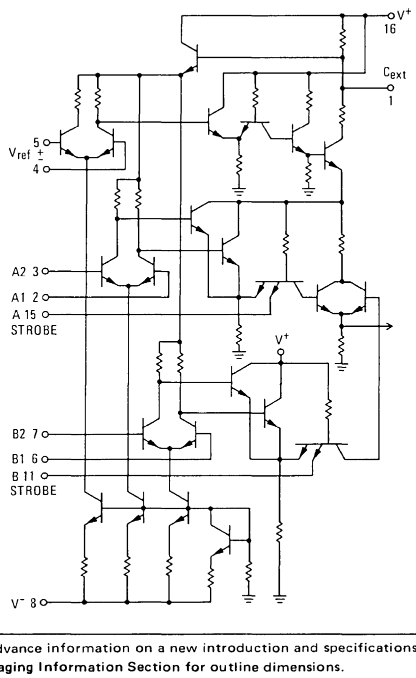
MC7520L and MC7521L



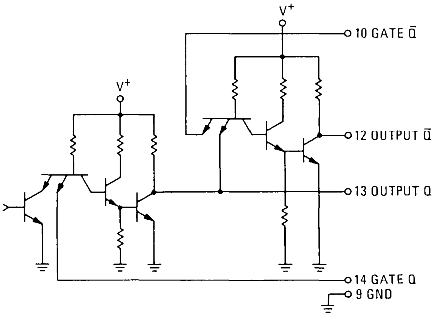
MC7522L and MC7523L



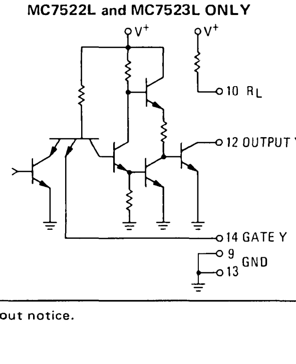
COMMON TO ALL DEVICES



MC7520L and MC7521 ONLY



MC7522L and MC7523L ONLY



This is advance information on a new introduction and specifications are subject to change without notice.

See Packaging Information Section for outline dimensions.

ELECTRICAL CHARACTERISTICS ($V^+ = 5.0$ V, $V^- = -5.0$ V, $T_A = 0$ to $+70^oC$ unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Input Threshold Voltage		V_{th}				mV
$V_{ref} = 15$ mV	MC7520L,MC7522L		11	15	19	
	MC7521L,MC7523L		8.0	15	22	
$V_{ref} = 40$ mV	MC7520L,MC7522L		36	40	44	
	MC7521L,MC7523L		33	40	47	
Common-Mode Input Firing Voltage		V_{CMF}	–	±3.0	–	Volts
Input Bias Current		I_{in}	–	30	75	µA
Input Offset Current		I_{io}	–	0.5	–	µA
Input Impedance (f = 1.0 kHz)		$Z_{(in)\ D}$	–	2.0	–	k ohms
Input Voltage Logic "1" Level (Strobe Inputs)	V_{in} "0" = 0.8 V	V_{in} "1"	2.0	–	–	Volts
Input Voltage Logic "0" Level (Strobe Inputs)	V_{in} "1" = 2.0 V	V_{in} "0"	–	–	0.8	Volt
Input Current Logic "0" Level (Strobe Inputs)	V_{in} "0" = 0.4 V	I_{in} "0"	–	–	-1.6	mA
Input Current Logic "1" Level (Strobe Inputs)	V_{in} "1" = 2.4 V	I_{in} "1"	–	–	40	µA
	V_{in} "1" = V^+		–	–	1.0	mA
Output Voltage Logic "1" Level	V_{in} "1" = 2.0 V	V_{out} "1"	2.4	3.9	–	Volts
Output Voltage Logic "0" Level	V_{in} "0" = 0.8 V	V_{out} "0"	–	0.25	0.4	Volt
Short-Circuit Output Current	Q Output MC7520L,MC7521L	I_{SC}	3.3	–	5.0	mA
	$\bar{Q}$ Output MC7520L,MC7521L		2.1	–	3.5	
	Output MC7522L,MC7523L		2.1	–	3.5	
V^+ Supply Current ($T_A = +25^oC$)	MC7520L,MC7521L	I^+	–	28	–	mA
	MC7522L,MC7523L		–	27	–	
V^- Supply Current ($T_A = +25^oC$)	MC7520L,MC7521L	I^-	–	-14	–	mA
	MC7522L,MC7523L		–	-15	–	

SWITCHING CHARACTERISTICS ($V^+ = 5.0$ V, $V^- = -5.0$ V, $T_A = +25^oC$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Differential-Mode Input Overload Recovery Time	$t_{OR\ DM}$	–	20	–	ns
Common-Mode Input Overload Recovery Time	$t_{OR\ CM}$	–	20	–	ns
Minimum Cycle Time	$t_{c\ (min)}$	–	200	–	ns

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MC7520L, MC7521L

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time					ns
(Differential Input to Q Output)	t_{pd} "1" DQ	–	20	40	
	t_{pd} "0" DQ	–	30	–	
(Differential Input to $\bar{Q}$ Output)	t_{pd} "1" D$\bar{Q}$	–	25	–	
	t_{pd} "0" D$\bar{Q}$	–	35	55	
(Strobe Input to Q Output)	t_{pd} "1" SQ	–	15	30	
	t_{pd} "0" SQ	–	25	–	
(Strobe Input to $\bar{Q}$ Output)	t_{pd} "1" S$\bar{Q}$	–	15	–	
	t_{pd} "0" S$\bar{Q}$	–	35	55	
(Gate Q Input to Q Output)	t_{pd} "1" G_QQ	–	10	20	
	t_{pd} "0" G_QQ	–	15	–	
(Gate Q Input to $\bar{Q}$ Output)	t_{pd} "1" $G_Q\bar{Q}$	–	15	–	
	t_{pd} "0" $G_Q\bar{Q}$	–	20	30	
(Gate $\bar{Q}$ Input to $\bar{Q}$ Output)	t_{pd} "1" $G_{\bar{Q}}\bar{Q}$	–	15	–	
	t_{pd} "0" $G_{\bar{Q}}\bar{Q}$	–	10	20	

MC7522L, MC7523L

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time					ns
(Differential Input to Output)	t_{pd} "1" D	–	20	–	
	t_{pd} "0" D	–	30	45	
(Strobe Input to Output)	t_{pd} "1" S	–	15	–	
	t_{pd} "0" S	–	25	40	
(Gate Input to Output)	t_{pd} "1" G	–	10	–	
	t_{pd} "0" G	–	15	25	

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Units
Power Supply Voltage	V^+ V^-	+7.0 -7.0	Vdc Vdc
Differential Input Signal Voltage	V_{in}	±5.0	Vdc
Strobe and Gate Input Voltage	$V_{in\,S,G}$	±5.5	Vdc
Power Dissipation Derate above T_A = +25°C	P_D	575 3.85	mW mW°C
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

MC7524L
MC7525L

DUAL SENSE AMPLIFIERS

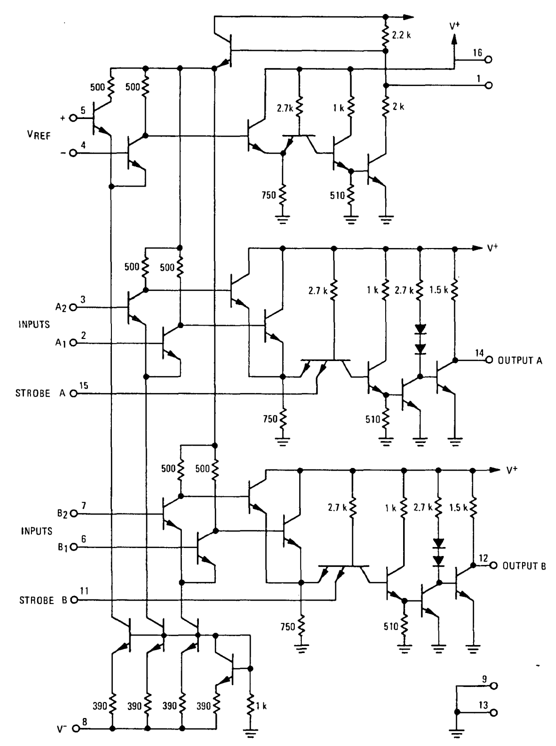
Advance Information

MONOLITHIC DUAL SENSE AMPLIFIERS

This dual sense amplifier is designed for use with high-speed memory systems. Low level pulses originating in the memory are converted to logic levels compatible with MDTL and MTTL circuits.

Features:

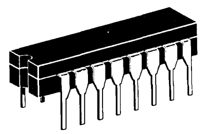
- Adjustable Threshold Voltage Levels
- High-Speed, Fast Recovery Time
- Time and Amplitude Signal Discrimination
- High dc Logic Noise Margin
  1.0 Volt typ
- Good Fan-Out Capability
- Independent Strobing
- Separate Logic Outputs



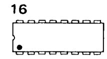
See Packaging Information Section for outline dimensions.

DUAL HIGH-SPEED SENSE AMPLIFIER INTEGRATED CIRCUIT

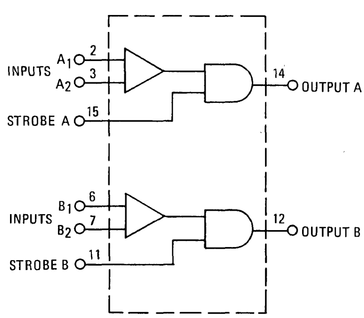
MONOLITHIC SILICON EPITAXIAL PASSIVATED



CERAMIC PACKAGE
CASE 620



Equivalent Circuit



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Units
Power Supply Voltage	V^+ V^-	+7.0 -7.0	Vdc Vdc
Differential Input Voltages	V_{in} or V_{ref}	±5.0	Vdc
Power Dissipation Derate above T_A = +25°C	P_D	575 3.85	mW mW°C
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

ELECTRICAL CHARACTERISTICS (V^+ = 5.0 V, V^- = -5.0 V, T_A = 0 to +70°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Input Threshold Voltage		V_{th}				mV
V_{ref} = 15 mV	MC7524L		11	15	19	
	MC7525L		8.0	15	22	
V_{ref} = 40 mV	MC7524L		36	40	44	
	MC7525L		33	40	47	
Common-Mode Input Firing Voltage		V_{CMF}	–	±3.0	–	Volts
Input Bias Current		I_{in}	–	30	75	μA
Input Offset Current		I_{io}	–	0.5	–	μA
Input Impedance (f = 1.0 kHz)		$Z_{(in)\ D}$	–	2.0	–	k ohms
Input Voltage Logic "1" Level (Strobe Inputs)	$V_{in(0)}$ = 0.8 V	$V_{in\ (1)}$	2.0	–	–	Volts
Input Voltage Logic "0" Level (Strobe Inputs)	$V_{in(1)}$ = 2.0 V	$V_{in\ (0)}$	–	–	0.8	Volt
Input Current Logic "0" Level (Strobe Inputs)	$V_{in(0)}$ = 0.4 V	$I_{in\ (0)}$	–	-1.0	-1.6	mA
Input Current Logic "1" Level (Strobe Inputs)	$V_{in(1)}$ = 2.4 V $V_{in(1)} = V^+$	$I_{in\ (1)}$	– –	– –	40 1.0	μA mA
Output Voltage Logic "1" Level	$V_{in(1)}$ = 2.0 V, $V_{in(0)}$ = 0.8 V	$V_{out\ (1)}$	2.4	3.9	–	Volts
Output Voltage Logic "0" Level	$V_{in(0)}$ = 0.8 V	$V_{out\ (0)}$	–	0.25	0.4	Volt
Short-Circuit Output Current		$I_{sc(out)}$	2.1	–	3.5	mA
V^+ Supply Current @ T_A = +25°C		I^+	–	25	–	mA
V^- Supply Current @ T_A = +25°C		I^-	–	-15	–	mA

SWITCHING CHARACTERISTICS (V^+ = 5.0 V, V^- = -5.0 V, T_A = +25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time (Differential Input to Output)	$t_{pd\ (1)\ D}$ $t_{pd\ (0)\ D}$	– –	15 40	40 –	ns
Propagation Delay Time (Strobe Input to Output)	$t_{pd\ (1)\ S}$ $t_{pd\ (0)\ S}$	– –	15 35	30 –	ns
Differential-Mode Input Overload Recovery Time	$t_{OR\ DM}$	–	20	–	ns
Common-Mode Input Overload Recovery Time	$t_{OR\ CM}$	–	20	–	ns
Minimum Cycle Time	$t_{c\ (min)}$	–	200	–	ns

OPERATIONAL AMPLIFIERS

MCC1536
MCC1436

Advance Information

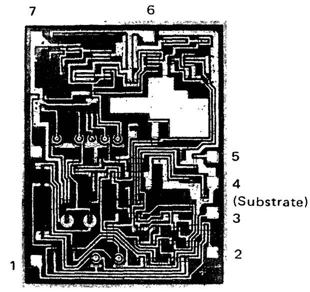
HIGH VOLTAGE, INTERNALLY COMPENSATED MONOLITHIC OPERATIONAL AMPLIFIER CHIP

. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

The MCC1536 and MCC1436 employ phosphorsilicate passivation that protects the entire die surface area, including metalization interconnects. All dice have a minimum gold-backed thickness of 4000 Angstroms. The interconnecting metalization and bonding pads are of evaporated aluminum.

- Maximum Supply Voltage – ±40 Vdc
- Output Voltage Swing –
  ±30 $V_{pk(min)}$ (V^+ = +36 V, V^- = -36 V)
  ±22 $V_{pk(min)}$ (V^+ = +28 V, V^- = -28 V)
- Input Bias Current – 20 nA max
- Input Offset Current – 3.0 nA max
- Fast Slew Rate – 2.0 V/μs typ
- Internally Compensated
- Offset Voltage Null Capability
- Input Over-Voltage Protection
- A_{VOL} – 500,000 typ
- Characteristics Independent of Power Supply Voltages – (±5.0 Vdc to ±36 Vdc)

OPERATIONAL AMPLIFIER CHIP
MONOLITHIC SILICON
INTEGRATED CIRCUIT
EPITAXIAL PASSIVATED



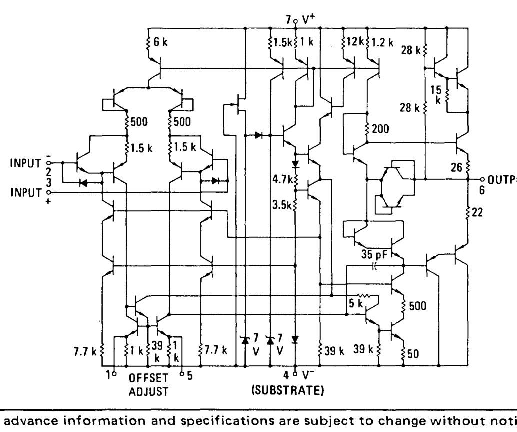
MCC1536/MCC1436

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

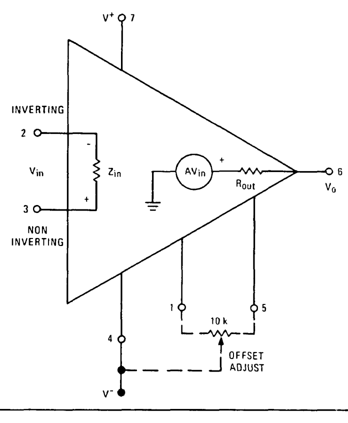
Rating	Symbol	MCC1536	MCC1436	Unit
Power Supply Voltage	V^+ V^-	+40 -40	+34 -34	Vdc
Differential Input Signal (1)	V_{in}	$\pm(V^+ + \|V^-\|-3)$		Volts
Common-Mode Input Swing	CMV_{in}	$+V^+, -(\|V^-\|-3)$		Volts
Output Short Circuit Duration ($V^+ = \|V^-\|$ = 28 Vdc, V_o = 0)	T_{SC}	5.0		s
Operating Temperature Range	T_A	-55 to +125		°C
Junction Temperature Range	T_{stg}	-65 to +150		°C

(1) The absolute voltage applied to either input terminal must not exceed $+V^+, -(|V^-|-3)$

CIRCUIT SCHEMATIC



EQUIVALENT CIRCUIT



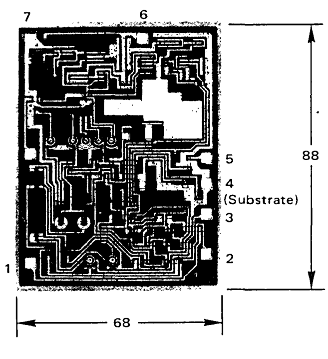
This is advance information and specifications are subject to change without notice.

ELECTRICAL CHARACTERISTICS (V^+ = +28 Vdc, V^- = -28 Vdc, T_A = +25°C unless otherwise noted)

Characteristics	Symbol	MCC1536 Min	MCC1536 Typ	MCC1536 Max	MCC1436 Min	MCC1436 Typ	MCC1436 Max	Unit
Input Bias Current	I_b	–	8.0	20	–	15	40	nAdc
Input Offset Current	$\lvert I_{io}\rvert$	–	1.0	3.0	–	5.0	10	nAdc
Input Offset Voltage	$\lvert V_{io}\rvert$	–	2.0	5.0	–	5.0	10	mVdc
Differential Input Impedance (Open-Loop, f ≤ 5.0 Hz)								
Parallel Input Resistance	R_p	–	10	–	–	10	–	Meg ohms
Parallel Input Capacitance	C_p	–	2.0	–	–	2.0	–	pF
Common-Mode Input Impedance (f ≤ 5.0 Hz)	$Z_{(in)}$	–	250	–	–	250		Meg ohms
Common-Mode Input Voltage Swing	CMV_{in}	–	±25	–	–	±25	–	V_{pk}
Common-Mode Rejection Ratio (dc)	CM_{rej}	–	110	–	–	110	–	dB
Large Signal dc Open Loop Voltage Gain	A_{VOL}							V/V
(V_o = ± 10 V, R_L = 100 k ohms)		100,000	500,000	–	70,000	500,000	–	
(V_o = ±10 V, R_L = 10 k ohms)		–	200,000	–	–	200,000	–	
Power Bandwidth (Voltage Follower) (A_V = 1, R_L = 5.0 k ohms, THD ≤ 5%, V_o = 40 Vp-p)	P_{BW}	–	23	–	–	23	–	kHz
Unity Gain Crossover Frequency (open-loop)		–	1.0	–	–	1.0	–	MHz
Phase Margin (open-loop, unity gain)		–	50	-	–	50	–	degrees
Gain Margin		–	18	–	–	18	–	dB
Slew Rate (Unity Gain)	dV_{out}/dt	–	2.0	–	–	2.0	–	V/µs
Output Impedance (f ≤ 5.0 Hz)	Z_{out}	–	1.0	–	–	1.0	–	k ohms
Short-Circuit Output Current	I_{SC}	–	±17	–	–	±17	–	mAdc
Output Voltage Swing (R_L = 5.0 k ohms)	V_o							V_{pk}
V^+ = +28 Vdc, V^- = -28 Vdc		±22	±23	–	±20	±22	–	
V^+ = +36 Vdc, V^- = -36 Vdc		±30	±32	–	–	–	–	
Power Supply Sensitivity (dc)								µV/V
V^- = constant, R_s ≤ 10 k ohms	S+	–	15	100	–	35	200	
V^+ = constant, R_s ≤ 10 k ohms	S-	–	15	100	–	35	200	
Power Supply Current	I_D+	–	2.2	4.0	–	2.6	5.0	mAdc
	I_D-	–	2.2	4.0	–	2.6	5.0	
DC Quiescent Power Dissipation (V_o = 0)	P_D	–	124	224	–	146	280	mW

See current MC1536/1436 data sheet for additional information.

MCC1536/MCC1436 BONDING DIAGRAM



All dimensions are nominal and in mils (10^{-3} inches).
Die Dimensions
Thickness = 8.0
Bonding Pads = 4.0 x 4.0

PACKAGING AND HANDLING

The MCC1536/MCC1436 operational amplifier is now available in die (chip) form. The phosphorsilicate passivation protects the metalization and active area of the die but care must be exercized when removing the dice from the shipping carrier to avoid scratching the bonding pads. A vacuum pickup is useful for the handling of dice. Tweezers are not recommended for this purpose.

The non-spill type shipping carrier consists of a compartmentalized tray and fitted cover. Die are placed in the carrier with geometry side up.

MCC1539
MCC1439

OPERATIONAL AMPLIFIERS

Advance Information

MONOLITHIC OPERATIONAL AMPLIFIER CHIP

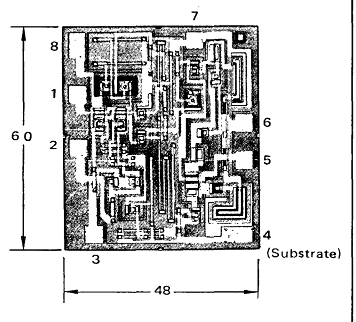
. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components. For detailed information see Motorola Application Note AN-439.

The MCC1539 and MCC1439 employ phosphorsilicate passivation that protects the entire die surface area, including metalization interconnects. All dice have a minimum gold-backed thickness of 4000 Angstroms. The interconnecting metalization and bonding pads are of evaporated aluminum.

- Low Input Offset Voltage – 3.0 mV max
- Low Input Offset Current – 60 nA max
- Large Power-Bandwidth – 20 V_{p-p} Output Swing at 20 kHz min
- Output Short-Circuit Protection
- Input Over-Voltage Protection
- Class AB Output for Excellent Linearity
- Slew Rate – 34 V/μs typ

OPERATIONAL AMPLIFIER CHIP INTEGRATED CIRCUIT

MONOLITHIC SILICON



All dimensions are nominal and in mils (10^{-3} inches).
Die Dimensions
Thickness = 8.0
Bonding Pads = 4.0 x 4.0

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+ V^-	+18 -18	Vdc Vdc
Differential Input Signal	V_{in}	$\pm[V^+ + \lvert V^- \rvert]$	Vdc
Common Mode Input Swing	CMV_{in}	$+V^+, -\lvert V^- \rvert$	Vdc
Load Current	I_L	15	mA
Output Short Circuit Duration	t_S	Continuous	
Operating Temperature Range	T_A	-55 to +125	°C
Junction Temperature Range	T_J	-65 to +150	°C

FIGURE 1 – CIRCUIT SCHEMATIC

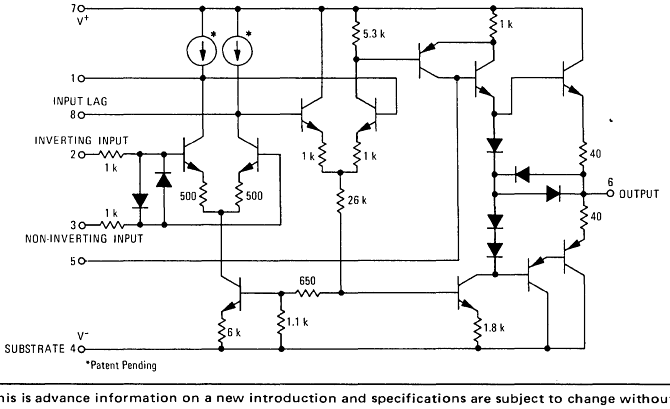
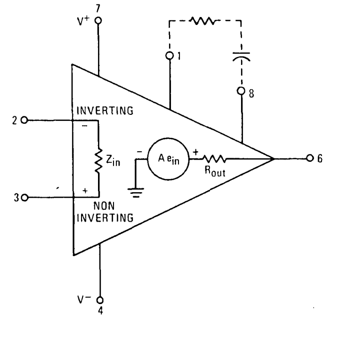


FIGURE 2 – EQUIVALENT CIRCUIT



This is advance information on a new introduction and specifications are subject to change without notice.

ELECTRICAL CHARACTERISTICS (V^+ = +15 Vdc, V^- = −15 Vdc, T_A = +25°C unless otherwise noted)

Characteristic	Symbol	MCC1539 Min	MCC1539 Typ	MCC1539 Max	MCC1439 Min	MCC1439 Typ	MCC1439 Max	Unit
Input Bias Current	I_b	–	0.20	0.50	–	0.20	1.0	µA
Input Offset Current	$\lvert I_{io} \rvert$	–	20	60	–	20	100	nA
Input Offset Voltage	$\lvert V_{io} \rvert$	–	1.0	3.0	–	2.0	7.5	mV
Average Temperature Coefficient of Input Offset Voltage (R_S = 50 Ω)	$\lvert TC_{Vio} \rvert$	–	3.0	–	–	3.0		µV/°C
Input Impedance	Z_{in}	–	300	–	–	300	–	kΩ
Input Common-Mode Voltage Swing	CMV_{in}	–	+12	–	–	+12	–	V_{pk}
Common Mode Rejection Ratio (f = 1.0 kHz)	CM_{rej}	–	110	–	–	110	–	dB
Open-Loop Voltage Gain (V_O = ±10 V, R_L = 10 kΩ, R_5 = ∞) (T_A = +25°C to T_{high})	A_{VOL}	50,000	120,000	–	15,000	100,000	–	–
(T_A = T_{low})		25,000	100,000	–	15,000	100,000	–	
Power Bandwidth (A_V = 1, THD ≤ 5%, V_O = 20 Vp-p, R_L = 1.0 kΩ)	PBW	–	50	–	–	50	–	kHz
Step Response								
Gain = 1000, no overshoot,	t_f	–	130	–	–	130	–	ns
	t_{pd}	–	190	–	–	190	–	ns
	dV_{out}/dt	–	6.0	–	–	6.0	–	V/µs
Gain = 1000, 15% overshoot,	t_f	–	80	–	–	80	–	ns
	t_{pd}	–	100	–	–	100	–	ns
	dV_{out}/dt	–	14	–	–	14	–	V/µs
Gain = 100, no overshoot,	t_f	–	60	–	–	60	–	ns
	t_{pd}	–	100	–	–	100	–	ns
	dV_{out}/dt	–	34	–	–	34	–	V/µs
Gain = 10, 15% overshoot,	t_f	–	120	–	–	120	–	ns
	t_{pd}	–	80	–	–	80	–	ns
	dV_{out}/dt	–	6.25	–	–	6.25	–	V/µs
Gain = 1, 15% overshoot,	t_f	–	160	–	–	160	–	ns
	t_{pd}	–	80	–	–	80	–	ns
	dV_{out}/dt	–	4.2	–	–	4.2	–	V/µs
Output Impedance (f = 20 Hz)	Z_{out}	–	4.0	–	–	4.0	–	kΩ
Output Voltage Swing	V_{out}							V_{pk}
(R_L = 2.0 kΩ, f = 1.0 kHz)		–	–	–	±10	±13	–	
(R_L = 1.0 kΩ, f = 1.0 kHz)		±10	±13	–	–	–	–	
Positive Supply Sensitivity (V^- constant)	S^+	–	50	150	–	50	200	µV/V
Negative Supply Sensitivity (V^+ constant)	S^-	–	50	150	–	50	200	µV/V
Power Supply Current (V_o = 0)	I_{D+}	–	3.0	5.0	–	3.0	6.7	mAdc
	I_{D-}	–	3.0	5.0	–	3.0	6.7	
DC Quiescent Power Dissipation (V_o = 0)	P_D	–	90	150	–	90	200	mW

See current MC1539/1439 data sheet for additional information.

PACKAGING AND HANDLING

The MCC1539/MCC1439 operational amplifier is now available as a single monolithic die or encapsulated in the TO-99 and TO-116 hermetic and plastic packages. The phosphorsilicate passivation protects the metalization and active area of the die but care must be exercised when removing the dice from the shipping carrier to avoid scratching the bonding pads. A vacuum pickup is useful for handling of dice. Tweezers are not recommended for this purpose.

The non-spill type shipping carrier consists of a compartmentalized tray and fitted cover. Die are placed in the carrier with geometry side up.

MCC1558
MCC1458

OPERATIONAL AMPLIFIERS

Advance Information

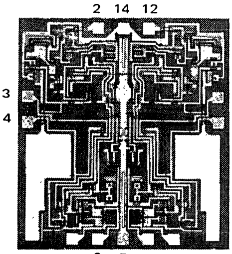
DUAL MC1741
INTERNALLY COMPENSATED, HIGH PERFORMANCE MONOLITHIC OPERATIONAL AMPLIFIER CHIP

. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

The MCC1558 and MCC1458 employ phosphorsilicate passivation that protects the entire die surface area, including metalization interconnects. All dice have a minimum gold-backed thickness of 4000 Angstroms. The interconnecting metalization and bonding pads are of evaporated aluminum.

- No Frequency Compensation Required
- Short-Circuit Protection
- Wide Common-Mode and Differential Voltage Ranges
- Low-Power Consumption
- No Latch Up

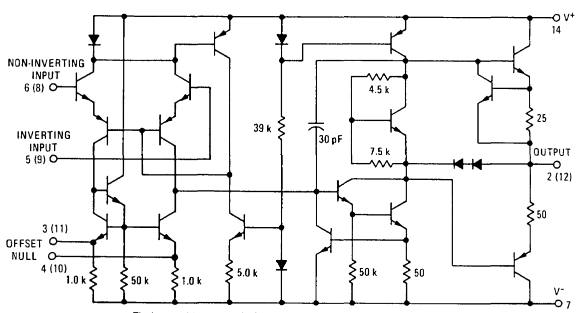
(DUAL MC1741)
DUAL
OPERATIONAL AMPLIFIER CHIP
INTEGRATED CIRCUIT
MONOLITHIC SILICON



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

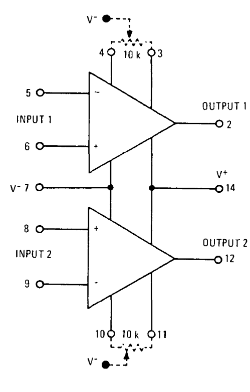
Rating	Symbol	MCC1558	MCC1458	Unit
Power Supply Voltage	V^+ V^-	+22 -22	+18 -18	Vdc
Differential Input Signal	V_{in}	±30		Volts
Common-Mode Input Swing	CMV_{in}	±15		Volts
Output Short Circuit Duration	t_S	Continuous		
Operating Temperature Range	T_A	-55 to +125		°C
Junction Temperature Range	T_J	-65 to +150		°C

FIGURE 1 – CIRCUIT SCHEMATIC



The letters without parenthesis represent the pin numbers for 1/2 of the dual circuit, letters in parenthesis represent the pin numbers for the other half.

FIGURE 2 – OFFSET ADJUST



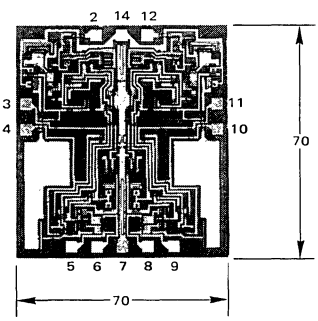
This is advance information on a new introduction and specifications are subject to change without notice.

ELECTRICAL CHARACTERISTICS (V^+ = +15 Vdc, V^- = -15 Vdc, T_A = +25°C unless otherwise noted)

Characteristic	Symbol	MCC1558 Min	MCC1558 Typ	MCC1558 Max	MCC1458 Min	MCC1458 Typ	MCC1458 Max	Unit
Input Bias Current	I_b	–	0.2	0.5	–	0.2	0.5	μAdc
Input Offset Current	$\|I_{io}\|$	–	0.03	0.2	–	0.03	0.2	μAdc
Input Offset Voltage ($R_S \leq 10$ k ohms)	$\|V_{io}\|$	–	1.0	5.0	–	2.0	6.0	mVdc
Differential Input Impedance (Open-Loop, f = 20 Hz)								
Parallel Input Resistance	R_p	–	1.0	–	–	1.0	–	Megohm
Parallel Input Capacitance	C_p	–	6.0	–	–	6.0	–	pF
Common-Mode Input Impedance (f = 20 Hz)	$Z_{(in)}$	–	200	–	–	200	–	Megohms
Common-Mode Input Voltage Swing	CMV_{in}	–	±13	–	–	±13	–	Vpk
Common-Mode Rejection Ratio (f = 100 Hz)	CM_{rej}	–	90	–	–	90	–	dB
Open-Loop Voltage Gain (V_o = ±10 V, R_L = 2.0 k ohms)	A_{VOL}	50,000	200,000	–	20,000	100,000	–	V/V
Power Bandwidth (A_V = 1, R_L = 2.0 k ohms, THD ≤ 5%, V_o = 20 $V_{p\text{-}p}$)	P_{BW}	–	14	–	–	14	–	kHz
Unity Gain Crossover Frequency (open-loop)		–	1.1	–	–	1.1		MHz
Phase Margin (open-loop, unity gain)		–	65	–	–	65	–	degrees
Gain Margin		–	11	–	–	11	–	dB
Slew Rate (Unity Gain)	dV_{out}/dt	–	0.8	–	–	0.8	–	V/μs
Output Impedance (f = 20 Hz)	Z_{out}	–	75	–	–	75	–	ohms
Short-Circuit Output Current	I_{SC}	–	20	–	–	20	–	mAdc
Output Voltage Swing (R_L = 10 k ohms)	V_o	±12	±14	–	±12	±14		Vpk
Power Supply Sensitivity								μV/V
V^- = constant, $R_s \leq 10$ k ohms	S^+	–	30	150	–	30	150	
V^+ = constant, $R_s \leq 10$ k ohms	S^-	–	30	150	–	30	150	
Power Supply Current	I_D^+	–	2.3	5.0	–	2.3	5.6	mAdc
	I_D^-	–	2.3	5.0	–	2.3	5.6	
DC Quiescent Power Dissipation (V_o = 0)	P_D	–	70	150	–	70	170	mW

See current MC1558/MC1458 data sheet for additional information.

MCC1558/MCC1458 BONDING DIAGRAM



All dimensions are nominal and in mils (10^{-3} inches).
Die Dimensions
Thickness = 8.0
Bonding Pads = 4.0 x 4.0

PACKAGING AND HANDLING

The MCC1558/MCC1458 dual operational amplifiers are now available as a single monolithic die or encapsulated in a variety of hermetic and plastic packages. The phosphorsilicate passivation protects the metalization and active area of the die but care must be exercised when removing the dice from the shipping carrier to avoid scratching the bonding pads. A vacuum pickup is useful for the handling of dice. Tweezers are not recommended for this purpose.

The non-spill type shipping carrier consists of a compartmentalized tray and fitted cover. Die are placed in the carrier with geometry side up.

MCC1563
MCC1463

NEGATIVE VOLTAGE REGULATORS

Advance Information

MONOLITHIC NEGATIVE VOLTAGE REGULATOR CHIP

The MCC1563/MCC1463 is a "three terminal" negative regulator designed to deliver continuous load current up to 500 mAdc and provide a maximum negative input voltage of -40 Vdc. Output current capability can be increased to greater than 10 Adc through use of one or more external transistors.

The MCC1563 and MCC1463 employ phosphorsilicate passivation that protects the entire die surface area, including metalization interconnects. All dice have a minimum gold-backed thickness of 4000 Angstroms. The interconnecting metalization and bonding pads are of evaporated aluminum.

- Electronic "Shutdown" and Short-Circuit Protection
- Low Output Impedance — 20 Milliohms typ
- Excellent Temperature Stability — $TCV_O = \pm 0.002\%/^{\circ}C$ typ
- High Ripple Rejection — 0.002% typ
- 500 mA Current Capability

NEGATIVE-POWER-SUPPLY VOLTAGE REGULATOR CHIP

MONOLITHIC SILICON INTEGRATED CIRCUIT

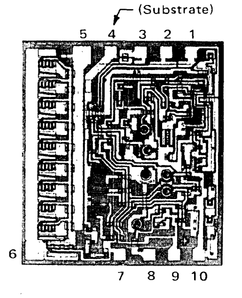


FIGURE 1 — TYPICAL CIRCUIT CONNECTION
$|-3.5| \le V_O \le |-37|$ Vdc, $1 \le I_L \le 500$ mA

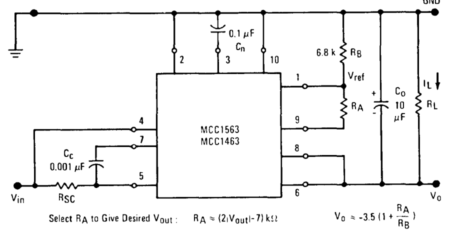


FIGURE 2 — TYPICAL NPN CURRENT BOOST CONNECTION
(V_O = -5.2 Vdc, I_L = 10 Adc [max])

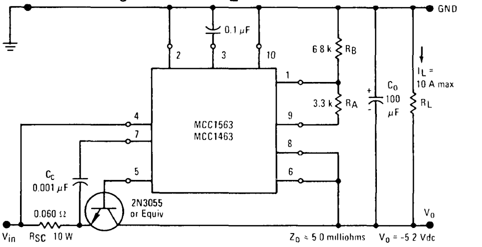
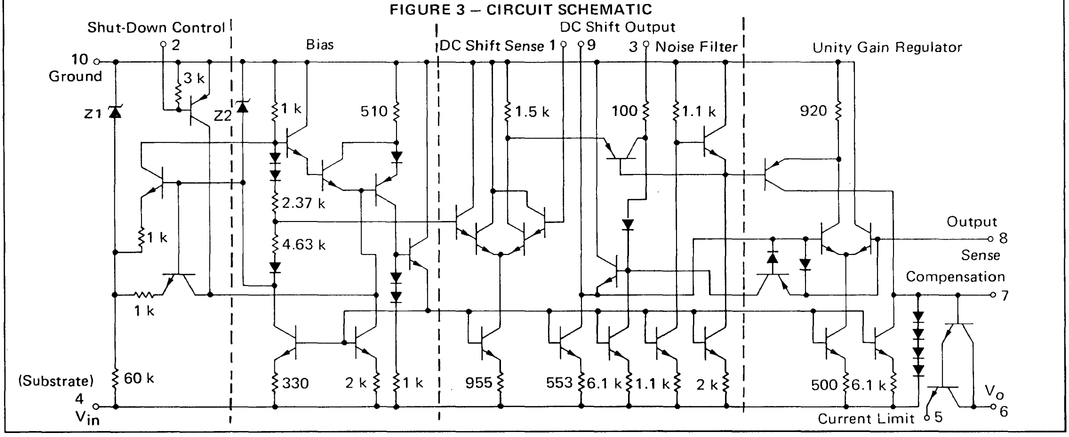


FIGURE 3 — CIRCUIT SCHEMATIC



This is advance information on a new introduction and specifications are subject to change without notice.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

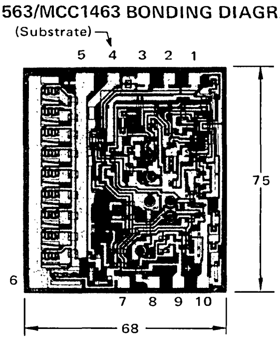
Rating	Symbol	MCC1563	MCC1463	Unit
Input Voltage	V_{in}	-40	-35	Vdc
Peak Load Current	I_L pk	600		mA
Current, Pin 2	$I_{pin\ 2}$	10		mA
Operating Temperature Range	T_A	-55 to +125		°C
Junction Temperature Range	T_J	-65 to +175		°C

ELECTRICAL CHARACTERISTICS (I_L = 100 mAdc, T_A = +25°C unless otherwise noted)

Characteristic	Symbol	MCC1563			MCC1463			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Voltage	V_{in}	–	–	-40	–	–	-35	Vdc
Output Voltage Range	V_O	-3.6	–	-37	-3.8	–	-32	Vdc
Reference Voltage (Pin 1 to Ground)	V_{ref}	-3.4	-3.5	-3.6	-3.2	-3.5	-3.8	Vdc
Minimum Input-Output Voltage Differential (R_{SC} = 0)	$\lvert V_{in} - V_O \rvert$	–	1.5	2.7	–	1.5	3.0	Vdc
Bias Current (I_L = 1.0 mAdc, $I_b = I_{in} - I_L$)	I_b	–	7.0	11	–	7.0	14	mAdc
Output Noise (C_n = 0.1 µF, f = 10 Hz to 5.0 MHz)	v_n	–	120	–	–	120	–	µV(rms)
Temperature Coefficient of Output Voltage	TCV_O	–	±0.002	–	–	±0.002	–	%/°C
Input Regulation	Reg_{in}	–	0.002	–	–	0.003	–	%/V_O
Load Regulation (T_J = Constant [1.0 mA ≤ I_L ≤ 20 mA])	Reg_L	–	0.4	–	–	0.7	–	mV
Output Impedance (f = 1.0 kHz)	Z_o	–	20	–	–	35	–	milliohms
Shutdown Current (V_{in} = -35 Vdc)	I_{sd}	–	7.0	15	–	14	50	µAdc

See current MC1563/1463 data sheet for additional information.

MCC1563/MCC1463 BONDING DIAGRAM



All dimensions are nominal and in mils (10^{-3} inches).
Die Dimensions
Thickness = 8.0
Bonding Pads = 4.0 x 4.0

PACKAGING AND HANDLING

The MCC1563/MCC1463 voltage regulator is now available as a single monolithic die or encapsulated in the Case 602A and Case 614 hermetic packages. The phosphorsilicate passivation protects the metalization and active area of the die but care must be exercised when removing the dice from the shipping carrier to avoid scratching the bonding pads. A vacuum pickup is useful for the handling of dice. Tweezers are not recommended for this purpose.

The non-spill type shipping carrier consists of a compartmentalized tray and fitted cover. Die are placed in the carrier with geometry side up.

MCC1569
MCC1469

POSITIVE VOLTAGE REGULATORS

Advance Information

MONOLITHIC VOLTAGE REGULATOR CHIP

The MCC1569 and MCC1469 are positive voltage regulators designed to deliver continuous load current up to 500 mAdc. Output voltage is adjustable from 2.5 Vdc to 37 Vdc. Systems requiring both a positive and negative regulated voltage can use the MCC1569 and MCC1563 as complementary regulators with a common input ground.

The MCC1569 and MCC1469 employ phosphorsilicate passivation that protects the entire die surface area, including metalization interconnects. All dice have a minimum gold-backed thickness of 4000 Angstroms. The interconnecting metalization and bonding pads are of evaporated aluminum.

- Electronic "Shut-Down" Control
- Excellent Load Regulation (Low Output Impedance – 20 milliohms typ)
- High Power Capability: Up to 17.5 Watts
- Excellent Temperature Stability: $\pm 0.002\%/^{\circ}C$ typ
- High Ripple Rejection: 0.002%/V typ

POSITIVE VOLTAGE REGULATOR CHIP INTEGRATED CIRCUIT

MONOLITHIC SILICON EPITAXIAL PASSIVATED

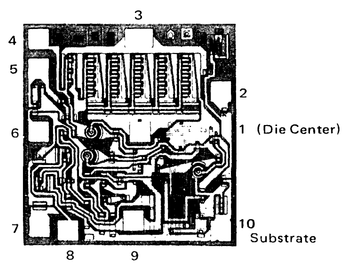
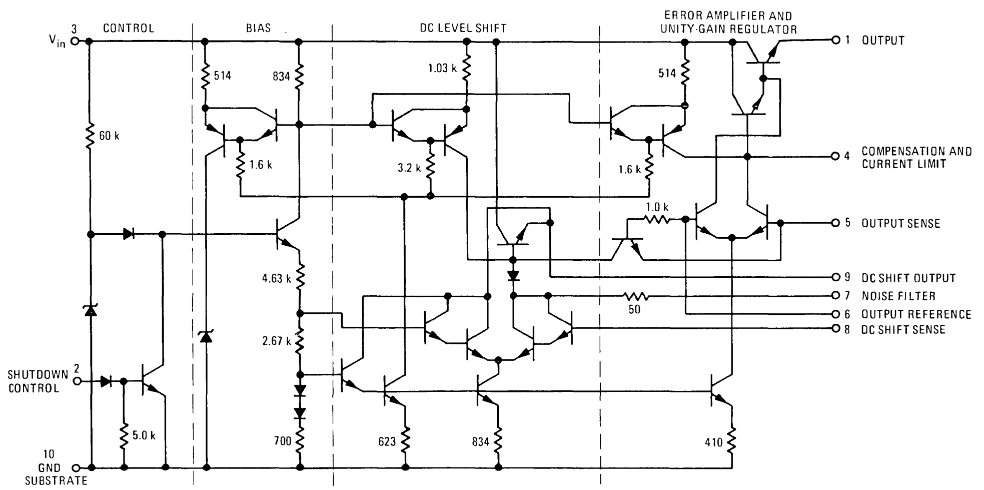


FIGURE 1 – CIRCUIT SCHEMATIC



This is advance information on a new introduction and specifications are subject to change without notice.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	MCC1569	MCC1469	Unit
Input Voltage	V_{in}	40	35	Vdc
Peak Load Current	I_{pk}	600		mA
Current, Pin 2 Current, Pin 9	$I_{pin\ 2}$ $I_{pin\ 9}$	10 5.0		mA
Operating Temperature Range	T_A	-55 to +125		°C
Junction Temperature Range	T_J	-65 to +150		°C

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted)

Characteristic	Symbol	MCC1569			MCC1469			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Voltage	V_{in}	–	–	40	–	–	35	Vdc
Output Voltage Range	V_O	2.5	–	37	2.5	–	32	Vdc
Reference Voltage (Pin 8 to Ground)	V_{ref}	3.4	3.5	3.6	3.2	3.5	3.8	Vdc
Minimum Input-Output Voltage Differential	$V_{in} - V_O$	–	2.1	2.7	–	2.1	3.0	Vdc
Bias Current (I_L = 1.0 mAdc, R_2 = 6.8 k ohms, $I_b = I_{in} - I_L$)	I_b	–	4.0	9.0	–	5.0	12	mAdc
Output Noise (C_n = 0.1 μF, f = 10 Hz to 5.0 MHz)	v_n	–	0.150	–	–	0.150	–	mV(rms)
Temperature Coefficient of Output Voltage	TCV_O	–	±0.002	–	–	±0.002	–	%/°C
Input Regulation	Reg_{in}	–	0.002	–	–	0.003	–	%/V_{in}
Output Impedance (C_c = 0.001 μF, R_{SC} = 1.0 ohm, f = 1.0 kHz, V_{in} = +14 Vdc, V_O = +10 Vdc)	Z_{out}	–	20	–	–	35	–	milliohms
Shutdown Current (V_{in} = +35 Vdc)	I_{sd}	–	70	150	–	140	500	μAdc

See current MC1569/1469 data sheet for additional information.

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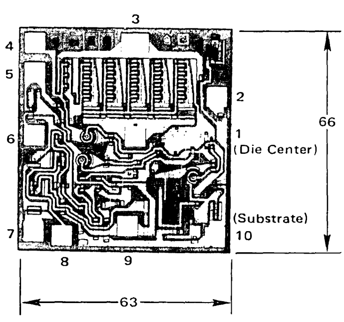
MCC1569/MCC1469 BONDING DIAGRAM



All dimensions are nominal and in mils (10^{-3} inches).
Die Dimensions
Thickness = 8.0
Bonding Pads = 4.0 x 4.0

PACKAGING AND HANDLING

The MCC1569/MCC1469 voltage regulator is now available as a single monolithic die or encapsulated in the Case 602A and Case 614 hermetic packages. The phosphorsilicate passivation protects the metalization and active area of the die but care must be exercised when removing the dice from the shipping carrier to avoid scratching the bonding pads. A vacuum pickup is useful for the handling of dice. Tweezers are not recommended for this purpose.

The non-spill type shipping carrier consists of a compartmentalized tray and fitted cover. Die are placed in the carrier with geometry side up.

MULTIPLIERS

MCC1595
MCC1495

Advance Information

MONOLITHIC FOUR-QUADRANT MULTIPLIER CHIP

. . . designed for uses where the output voltage is a linear product of two input voltages. Typical applications include: multiply, divide*, square root*, mean square*, phase detector, frequency doubler, balanced modulator/demodulator, electronic gain control.

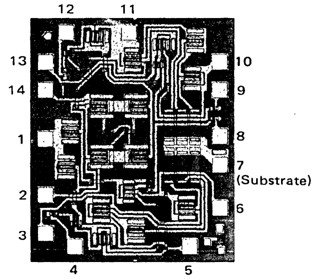
The MCC1595 and MCC1495 employ phosphorsilicate passivation that protects the entire die surface area, including metalization interconnects. All dice have a minimum gold-backed thickness of 4000 Angstroms. The interconnecting metalization and bonding pads are of evaporated aluminum.

*When used with an operational amplifier.

- Excellent Linearity – 0.5% typ Error on X-Input, 1% typ Error on Y-Input – MCC1595
- Excellent Linearity – 1% typ Error on X-Input, 2% typ Error on Y-Input – MCC1495
- Adjustable Scale Factor, K
- Excellent Temperature Stability
- Wide Input Voltage Range – ± 10 Volts

LINEAR FOUR-QUADRANT MULTIPLIER CHIP INTEGRATED CIRCUIT

MONOLITHIC SILICON EPITAXIAL PASSIVATED

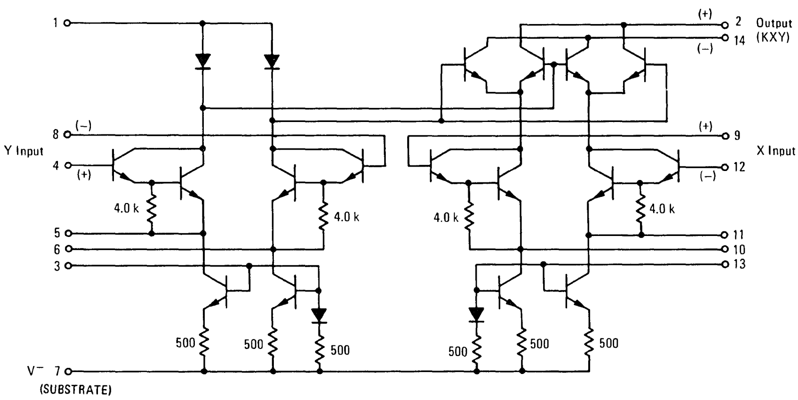


MCC1595/MCC1495 Die

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Applied Voltage (V_2-V_1, $V_{14}-V_1$, V_1-V_9, V_1-V_{12}, V_1-V_4, V_1-V_8, $V_{12}-V_7$, V_9-V_7, V_8-V_7, V_4-V_7)	ΔV	30	Vdc
Differential Input Signal	$V_{12}-V_9$ V_4-V_8	$\pm(6+I_{13} R_X)$ $\pm(6+I_3 R_Y)$	Vdc Vdc
Maximum Bias Current	I_3 I_{13}	10 10	mA
Operating Temperature Range	T_A	-55 to +125	°C
Junction Temperature Range	T_J	-65 to +150	°C

CIRCUIT SCHEMATIC



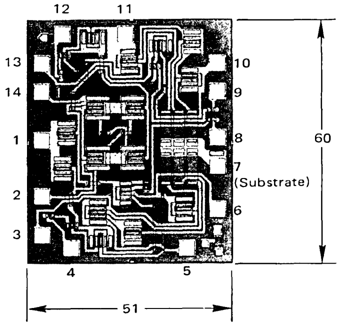
This is advance information on a new introduction and specifications are subject to change without notice.

ELECTRICAL CHARACTERISTICS (V^+ = +32 V, V^- = -15 V, T_A = 25°C, $I_3 = I_{13}$ = 1 mA, $R_X = R_Y$ = 15 kΩ, R_L = 11 kΩ unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Linearity:						
Output Error in Percent of Full Scale:						%
$-10 < V_X < +10$ ($V_Y = \pm 10$ V)	MCC1495	E_{RX}	–	1.0	–	
	MCC1595		–	0.5	–	
$-10 < V_Y < +10$ ($V_X = \pm 10$ V)	MCC1495	E_{RY}	–	2.0	–	
	MCC1595		–	1.0	–	
Squaring Mode Error: Accuracy in Percent of Full Scale After Offset and Scale Factor Adjustment		E_{SQ}				%
	MCC1495		–	0.75	–	
	MCC1595		–	0.5	–	
Scale Factor (Adjustable) $\left(K = \frac{2R_L}{I_3 R_X R_Y}\right)$		K	–	0.1	–	–
Input Resistance (f = 20 Hz)	MCC1495	R_{INX}	–	20	–	Megohms
	MCC1595		–	35	–	
	MCC1495	R_{INY}	–	20	–	
	MCC1595		–	35	–	
Differential Output Resistance (f = 20 Hz)		R_o	–	300	–	k Ohms
Input Bias Current $I_{bx} = \frac{(I_9 + I_{12})}{2}$, $I_{by} = \frac{(I_4 + I_8)}{2}$	MCC1495	I_{bx}	–	2.0	12	μA
	MCC1595		–	2.0	8.0	
	MCC1495	I_{by}	–	2.0	12	
	MCC1595		–	2.0	8.0	
Input Offset Current $\lvert I_9 - I_{12}\rvert$	MCC1495	$\lvert I_{iox}\rvert$	–	0.4	2.0	μA
	MCC1595		–	0.2	1.0	
$\lvert I_4 - I_8\rvert$	MCC1495	$\lvert I_{ioy}\rvert$	–	0.4	2.0	
	MCC1595		–	0.2	1.0	
Output Offset Current $\lvert I_{14} - I_2\rvert$		$\lvert I_{oo}\rvert$				μA
	MCC1495		–	20	100	
	MCC1595		–	10	50	
Frequency Response						
3.0 dB Bandwidth		BW_{3dB}	–	3.0	–	MHz
3° Relative Phase Shift Between V_X and V_Y		f_ϕ	–	750	–	kHz
1% Absolute Error Due to Input-Output Phase Shift		f_θ	–	30	–	kHz
Common Mode Input Swing (Either input)		CMV				Vdc
	MCC1495		–	±12	–	
	MCC1595		–	±13	–	
Common Mode Quiescent Output Voltage		V_{o1}	–	21	–	Vdc
		V_{o2}	–	21	–	
Differential Output Voltage Swing Capability		V_{out}	–	±14	–	V_{peak}
Power Supply Sensitivity		S^+	–	5.0	–	mV/V
		S^-	–	10	–	
Power Supply Current		I_7	–	6.0	7.0	mA
DC Power Dissipation		P_D	–	135	170	mW

See current MC1595/1495 data sheet for additional information.

MCC1595/MCC1495 BONDING DIAGRAM



PACKAGING AND HANDLING

The MCC1595/MCC1495 is the Four-Quadrant Multiplier now available in die (chip) form. The phosphorsilicate passivation protects the metalization and active area of the die but care must be exercized when removing the dice from the shopping carrier to avoid scratching the bonding pads. A vacuum pickup is useful for the handling of dice. Tweezers are not recommended for this purpose.

The non-spill type shipping carrier consists of a compartmentalized tray and fitted cover. Die are placed in the carrier with geometry side up.

All dimensions are nominal and in mils (10^{-3} inches).
Die Dimensions
Thickness = 8.0
Bonding Pads = 4.0 x 4.0

OPERATIONAL AMPLIFIERS

MCC1709
MCC1709C

Advance Information

MONOLITHIC OPERATIONAL AMPLIFIER CHIP

. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

The MCC1709 and MCC1709C employ phosphorsilicate passivation that protects the entire die surface area, including metalization interconnects. All dice have a minimum gold-backed thickness of 4000 Angstroms. The interconnecting metalization and bonding pads are of evaporated aluminum.

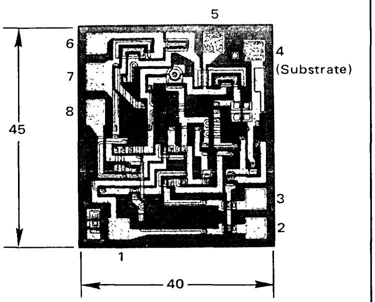
- High-Performance Open Loop Gain Characteristics
  A_{VOL} = 45,000 typical
- Low Temperature Drift – ±3.0 $\mu V/^{o}C$
- Large Output Voltage Swing – ±14 V typical @ ±15 V Supply
- Low Output Impedance – Z_{out} = 150 ohms typical

OPERATIONAL AMPLIFIER CHIP INTEGRATED CIRCUIT
MONOLITHIC SILICON

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+ V^-	+18 -18	Vdc
Differential Input Signal	V_{in}	±5.0	Volts
Common Mode Input Swing	CMV_{in}	$\pm V^+$	Volts
Load Current	I_L	10	mA
Output Short Circuit Duration	t_S	5.0	s
Operating Temperature Range	T_A	-55 to +125	°C
Junction Temperature Range	T_J	-55 to +150	°C

OUTLINE DIMENSIONS and BONDING DIAGRAM



All dimensions are nominal and in mils (10^{-3} inches).
Die Dimensions
Thickness = 8.0
Bonding Pads = 4.0 x 4.0

6

FIGURE 1 – CIRCUIT SCHEMATIC

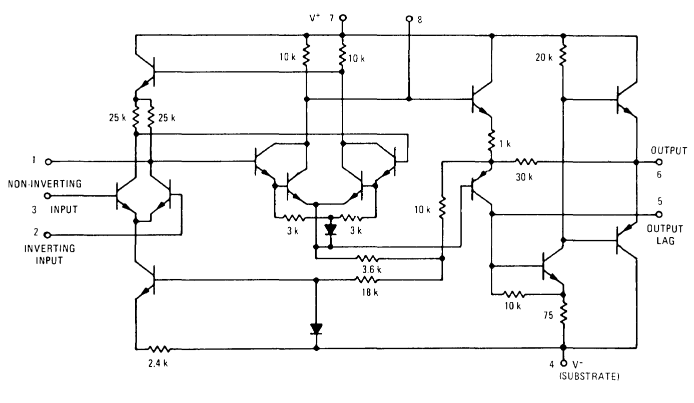
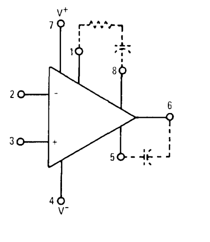


FIGURE 2 – EQUIVALENT CIRCUIT



This is advance information on a new introduction and specifications are subject to change without notice.

ELECTRICAL CHARACTERISTICS (V^+ = +15 Vdc, V^- = −15 Vdc, T_A = +25°C unless otherwise noted)

Characteristic	Symbol	MCC1709 Min	MCC1709 Typ	MCC1709 Max	MCC1709C Min	MCC1709C Typ	MCC1709C Max	Unit
Open Loop Voltage Gain (V_O = ±10 V)	A_{VOL}	25,000	45,000	70,000	15,000	45,000	–	–
Output Impedance (f = 20 Hz)	Z_{out}	–	150	–	–	150	–	Ω
Input Impedance (f = 20 Hz)	Z_{in}	–	400	–	–	250	–	kΩ
Output Voltage Swing	V_O							V_{peak}
(R_L = 10 kΩ)		±12	±14	–	±12	±14	–	
(R_L = 2.0 kΩ)		±10	±13	–	±10	±13	–	
Input Common-Mode Voltage Swing	CMV_{in}	–	±10	–	–	±10	–	V_{peak}
Common-Mode Rejection Ratio (f = 20 Hz)	CM_{rej}	–	90	–	–	90	–	dB
Input Bias Current	I_b	–	0.2	0.5	–	0.3	1.5	μA
Input Offset Current	$\|I_{io}\|$	–	0.05	0.2	–	0.1	0.5	μA
Input Offset Voltage	$\|V_{io}\|$	–	1.0	5.0	–	2.0	7.5	mV
Step Response								
Gain = 100, 5.0% overshoot	t_f	–	0.8	–	–	0.8	–	μs
	t_{pd}	–	0.38	–	–	0.38	–	μs
	dV_{out}/dt	–	12	–	–	12	–	V/μs
Gain = 10, 10% overshoot	t_f	–	0.6	–	–	0.6	–	μs
	t_{pd}	–	0.34	–	–	0.34	–	μs
	dV_{out}/dt	–	1.7	–	–	1.7	–	V/μs
Gain = 1, 5.0% overshoot	t_f	–	2.2	–	–	2.2	–	μs
	t_{pd}	–	1.3	–	–	1.3	–	μs
	dV_{out}/dt	–	0.25	–	–	0.25	–	V/μs
Power Supply Current	I_D^+	–	2.7	5.5	–	2.7	6.7	mAdc
	I_D^-	–	2.7	5.5	–	2.7	6.7	
DC Quiescent Power Dissipation (Power Supply = ±15 V, V_O = 0)	P_D	–	80	165	–	80	200	mW
Positive Supply Sensitivity (V^- constant)	S^+	–	25	150	–	25	200	μV/V
Negative Supply Sensitivity (V^+ constant)	S^-	–	25	150	–	25	200	μV/V

See current MC1709/1709C data sheet for additional information

PACKAGING AND HANDLING

The MCC1709/MCC1709C operational amplifier is now available as a single monolithic die or encapsulated in a variety of hermetic and plastic packages. The phosphorsilicate passivation protects the metalization and active area of the die but care must be exercised when removing the dice from the shipping carrier to avoid scratching the bonding pads. A vacuum pickup is useful for handling of dice. Tweezers are not recommended for this purpose.

The non-spill type shipping carrier consists of a compartmentalized tray and fitted cover. Die are placed in the carrier with geometry side up.

MCC1710
MCC1710C

DIFFERENTIAL COMPARATORS

Advance Information

MONOLITHIC DIFFERENTIAL VOLTAGE COMPARATOR CHIP

. . . designed for use in level detection, low-level sensing, and memory applications.

The MCC1710 and MCC1710C employ phosphorsilicate passivation that protects the entire die surface area, including metalization interconnects. All dice have a minimum gold-backed thickness of 4000 Angstroms. The interconnecting metalization and bonding pads are of evaporated aluminum.

- Differential Input Characteristics –
  Input Offset Voltage = 1.0 mV
  Offset Voltage Drift = 3.0 μV/^{o}C
- Fast Response Time – 40 ns
- Output Compatible With All Saturating Logic Forms –
  V_{out} = +3.2 V to -0.5 V typical
- Low Output Impedance – 200 ohms

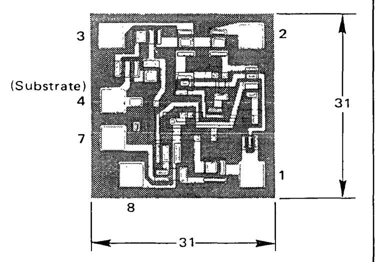
MAXIMUM RATINGS (T_A = 25^{o}C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+ V^-	+14 -7.0	Vdc
Differential Input Signal	V_{in}	±5.0	Volts
Common Mode Input Swing	CMV_{in}	±7.0	Volts
Peak Load Current	I_L	10	mA
Operating Temperature Range	T_A	-55 to +125	^{o}C
Junction Temperature Range	T_J	-65 to +150	^{o}C

DIFFERENTIAL COMPARATOR CHIP INTEGRATED CIRCUIT

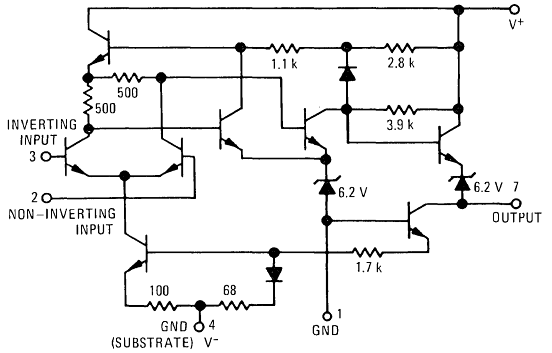
MONOLITHIC SILICON EPITAXIAL PASSIVATED

OUTLINE DIMENSIONS and BONDING DIAGRAM

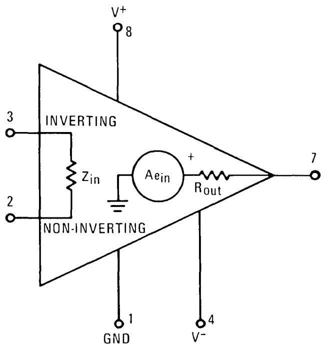


All dimensions are nominal and in mils (10^{-3} inches).
Die Dimensions
Thickness = 8.0
Bonding Pads = 4.0 x 4.0

CIRCUIT SCHEMATIC



EQUIVALENT CIRCUIT



This is advance information on a new introduction and specifications are subject to change without notice.

ELECTRICAL CHARACTERISTICS (V^+ = +12 Vdc, V^- = -6.0 Vdc, T_A = 25°C unless otherwise noted)

Characteristic	Symbol	MCC1710 Min	MCC1710 Typ	MCC1710 Max	MCC1710C Min	MCC1710C Typ	MCC1710C Max	Unit
Input Offset Voltage (V_O = 1.4 Vdc)	V_{io}	–	1.0	2.0	–	1.5	5.0	mVdc
Input Bias Current (V_O = 1.4 Vdc)	I_b	–	12	20	–	15	25	µAdc
Output Resistance	R_{out}	–	200	–	–	200	–	Ohms
Positive Output Voltage ($V_{in} \geq 5.0$ mV, $0 \leqq I_O \leqq 5.0$ mA)	V_{OH}	2.5	3.2	4.0	2.5	3.2	4.0	Vdc
Negative Output Voltage ($V_{in} \geqq -5.0$ mV)	V_{OL}	-1.0	-0.5	0	-1.0	-0.5	0	Vdc
Output Sink Current ($V_{in} \geqq -5.0$ mV, $V_{out} \geqq 0$)	I_s	2.0	2.5	–	2.0	2.5	–	mAdc
Common Mode Rejection Ratio (V^- = -7.0 Vdc, $R_S \leqq 200\ \Omega$)	CM_{rej}	–	100	–	–	100	–	dB
Propagation Delay Time For Positive and Negative Going Input Pulse	t_{pd}	–	40	–	–	40	–	ns
Power Supply Current ($V_{out} \leqq 0$ Vdc)	I_D^+	–	6.4	9.0	–	6.4	9.0	mAdc
	I_D^-	–	5.5	7.0	–	5.5	7.0	
DC Quiescent Power Dissipation	P_D	–	115	150	–	110	150	mW

See current MC1710/1710C data sheet for additional information.

6

PACKAGING AND HANDLING

The MCC1710/MCC1710C differential comparator is now available as a single monolithic die or encapsulated in the TO-91, TO-99, and TO-116 hermetic packages. The phosphorsilicate passivation protects the metalization and active area of the die but care must be exercised when removing the dice from the shipping carrier to avoid scratching the bonding pads. A vacuum pickup is useful for handling of dice. Tweezers are not recommended for this purpose.

The non-spill type shipping carrier consists of a compartmentalized tray and fitted cover. Die are placed in the carrier with geometry side up.

MCC1711
MCC1711C

DIFFERENTIAL COMPARATORS

Advance Information

MONOLITHIC DUAL DIFFERENTIAL VOLTAGE COMPARATOR CHIP

. . . designed for use in level detection, low-level sensing, and memory applications.

The MCC1711 and MCC1711C employ phosphorsilicate passivation that protects the entire die surface area, including metalization interconnects. All dice have a minimum gold-backed thickness of 4000 Angstroms. The interconnecting metalization and bonding pads are of evaporated aluminum.

- Differential Input –
  Input Offset Voltage = 1.0 mV
  Offset Voltage Drift = 5.0 μV/^{o}C
- Fast Response Time – 40 ns
- Output Compatible with All Saturating Logic Forms –
  V_{out} = +4.5 V to -0.5 V Typical
- Low Output Impedance – 200 Ohms

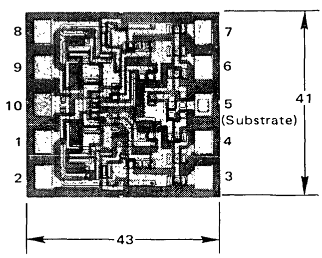
DUAL DIFFERENTIAL COMPARATOR CHIP INTEGRATED CIRCUIT

MONOLITHIC SILICON EPITAXIAL PASSIVATED

MAXIMUM RATINGS (T_A = 25^{o}C unless otherwise noted)

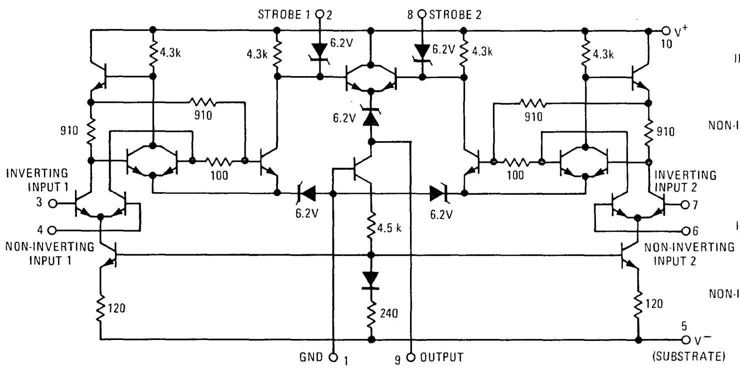
Rating	Symbol	Value	Unit
Power Supply Voltage	V^+	+14	Vdc
	V^-	-7.0	Vdc
Differential Input Signal	V_{in}	±5.0	Volts
Common Mode Input Swing	CMV_{in}	±7.0	Volts
Peak Load Current	I_L	50	mA
Operating Temperature Range	T_A	-55 to +125	^{o}C
Junction Temperature Range	T_J	-65 to +150	^{o}C

OUTLINE DIMENSIONS and BONDING DIAGRAM

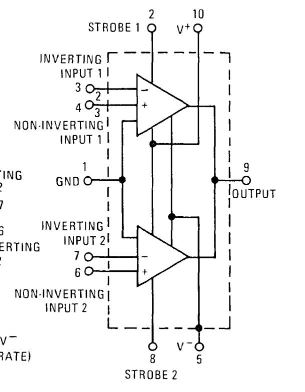


All dimensions are nominal and in mils (10^{-3} inches).
Die Dimensions
Thickness = 8.0
Bonding Pads = 4.0 x 4.0

CIRCUIT SCHEMATIC



EQUIVALENT CIRCUIT



This is advance information on a new introduction and specifications are subject to change without notice.

ELECTRICAL CHARACTERISTICS (each comparator) (V^+ = +12 Vdc, V^- = -6.0 Vdc, T_A = 25°C unless otherwise noted)

Characteristic	Symbol	MCC1711			MCC1711C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (V_O = 1.4 Vdc)	V_{io}	–	1.0	3.5	–	1.0	5.0	mVdc
Input Bias Current (V_O = 1.4 Vdc)	I_b	–	25	75	–	25	100	μAdc
Output Resistance	R_{out}	–	200	–	–	200	–	Ohms
Positive Output Voltage ($V_{in} \geqq 10$ mVdc, $0 \leqq I_O \leqq 5.0$ mA)	V_{OH}	2.5	3.2	5.0	2.5	3.2	5.0	Vdc
Negative Output Voltage ($V_{in} \geqq -10$ mVdc)	V_{OL}	-1.0	-0.5	0	-1.0	-0.5	0	Vdc
Strobed Output Level ($V_{strobe} \leqq 0.3$ Vdc)	$V_{OL(st)}$	-1.0	–	0	-1.0	–	0	Vdc
Output Sink Current ($V_{in} \geqq -10$ mV, $V_O \geqq 0$)	I_S	0.5	0.8	–	0.5	0.8	–	mAdc
Strobe Current (V_{strobe} = 100 mVdc)	I_{st}	–	1.2	2.5	–	1.2	2.5	mAdc
Response Time (V_b = 5.0 mV + V_{io})	t_R	–	40	–	–	40	–	ns
Strobe Release Time	t_{SR}	–	12	–	–	12	–	ns
Power Supply Current ($V_O \leqq 0$ Vdc)	I_D^+ I_D^-	– –	8.6 3.9	– –	– –	8.6 3.9	– –	mAdc
Power Consumption		–	130	200	–	130	200	mW

See current MC1711/1711C data sheet for additional information.

PACKAGING AND HANDLING

The MCC1711/MCC1711C dual differential comparator is now available as a single monolithic die or encapsulated in the TO-91, TO-100, and TO-116 hermetic packages. The phosphorsilicate passivation protects the metalization and active area of the die but care must be exercised when removing the dice from the shipping carrier to avoid scratching the bonding pads. A vacuum pickup is useful for handling of dice. Tweezers are not recommended for this purpose.

The non-spill type shipping carrier consists of a compartmentalized tray and fitted cover. Die are placed in the carrier with geometry side up.

MCC1723
MCC1723C

Advance Information

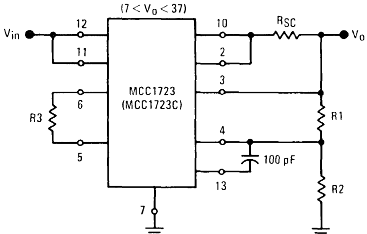
MONOLITHIC VOLTAGE REGULATOR CHIP

The MCC1723/MCC1723C is a positive or negative voltage regulator designed to deliver load current to 150 mAdc. Output current capability can be increased to several amperes through use of one or more external pass transistors.

The MCC1723 and MCC1723C employ phosphorsilicate passivation that protects the entire die surface area, including metalization interconnects. All dice have a minimum gold-backed thickness of 4000 Angstroms. The interconnecting metalization and bonding pads are of evaporated aluminum.

- Output Voltage Adjustable from 2 Vdc to 37 Vdc
- Output Current to 150 mAdc Without External Pass Transistors
- 0.01% Line Regulation
- Adjustable Short-Circuit Protection

FIGURE 1 – TYPICAL CIRCUIT CONNECTION

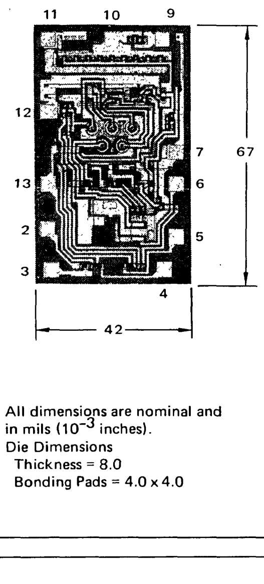


$V_o \cong 7\left(\frac{R1 + R2}{R2}\right)$ $I_{SC} = \frac{V_{sense}}{R_{SC}} = \frac{0.66}{R_{SC}}$ at $T_J = 25^oC$

For best results 10 k < R2 < 100 k
For minimum drift R3 = R1||R2

VOLTAGE REGULATOR CHIP

MONOLITHIC SILICON EPITAXIAL PASSIVATED INTEGRATED CIRCUIT



All dimensions are nominal and in mils (10^{-3} inches).
Die Dimensions
Thickness = 8.0
Bonding Pads = 4.0 x 4.0

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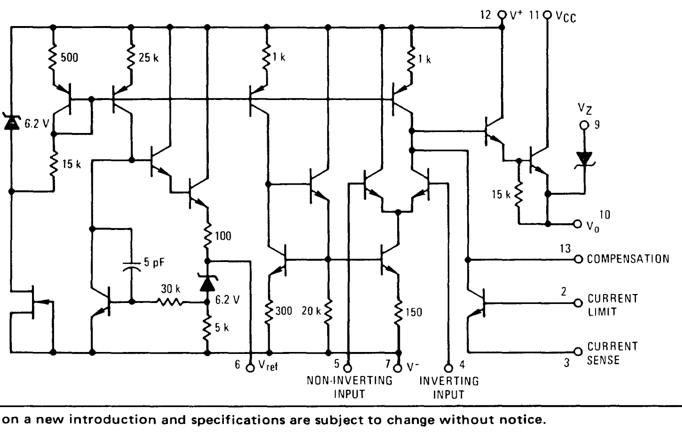
FIGURE 2 – CIRCUIT SCHEMATIC



This is advance information on a new introduction and specifications are subject to change without notice.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Pulse Voltage from V^+ to V^- (50 ms) MCC1723	$V_{in(p)}$	50	V_{peak}
Continuous Voltage from V^+ to V^-	V_{in}	40	Vdc
Input-Output Voltage Differential	$V_{in}-V_o$	40	Vdc
Maximum Output Current	I_L	150	mAdc
Current from V_{ref}	I_{ref}	15	mAdc
Operating Temperature Range	T_A	-55 to +125	°C
Junction Temperature Range	T_J	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise noted: T_A = +25°C, V_{in} = 12 Vdc, V_o = 5 Vdc, I_L = 1 mAdc, R_{SC} = 0, C1 = 100 pF, C_{ref} = 0 and divider impedance as seen by the error amplifier ≤ 10 kΩ connected as shown in Figure 1)

Characteristic	Symbol	MCC1723 Min	MCC1723 Typ	MCC1723 Max	MCC1723C Min	MCC1723C Typ	MCC1723C Max	Unit
Input Voltage Range	V_{in}	9.5	–	40	9.5	–	40	Vdc
Output Voltage Range	V_o	2.0	–	37	2.0	–	37	Vdc
Input-Output Voltage Differential	$V_{in}-V_o$	3.0	–	38	3.0	–	38	Vdc
Reference Voltage	V_{ref}	6.95	7.15	7.35	6.80	7.15	7.50	Vdc
Standby Current Drain (I_L = 0, V_{in} = 30 V)	I_{sb}	–	2.3	3.5	–	2.3	4.0	mAdc
Output Noise Voltage (f = 100 Hz to 10 kHz)	V_n							μV(rms)
C_{ref} = 0		–	20	–	–	20	–	
C_{ref} = 5.0 μF		–	2.5	–	–	2.5	–	
Line Regulation	Reg_{in}							% V_o
(12 V < V_{in} < 15 V)		–	0.01	0.1	–	0.01	0.1	
(12 V < V_{in} < 40 V)		–	0.02	0.2	–	0.1	0.5	
Load Regulation (1.0 mA < I_L < 50 mA)	Reg_{load}		0.03	0.15	–	0.03	0.2	% V_o
Ripple Rejection (f = 50 Hz to 10 kHz)	Rej_R							dB
C_{ref} = 0		–	74	–	–	74	–	
C_{ref} = 5.0 μF		–	86	–	–	86	–	
Short Circuit Current Limit (R_{SC} = 10 Ω, V_o = 0)	I_{SC}	–	65	–	–	65	–	mAdc

See current MC1723/1723C data sheet for additional information.

PACKAGING AND HANDLING

The MCC1723/MCC1723C voltage regulator is now available as a single monolithic die or encapsulated in the Motorola Case 603-03 hermetic package. The phosphorsilicate passivation protects the metalization and active area of the die but care must be exercised when removing the dice from the shipping carrier to avoid scratching the bonding pads. A vacuum pickup is useful for handling of dice. Tweezers are not recommended for this purpose.

The non-spill type shipping carrier consists of a compartmentalized tray and fitted cover. Die are placed in the carrier with geometry side up.

MCC1741
MCC1741C

OPERATIONAL AMPLIFIERS

Advance Information

INTERNALLY COMPENSATED, HIGH PERFORMANCE MONOLITHIC OPERATIONAL AMPLIFIER CHIP

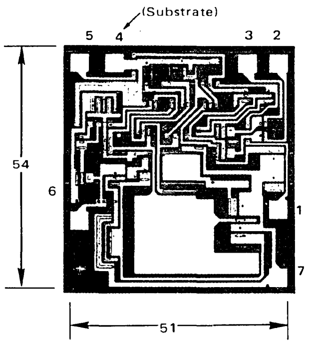
. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

The MCC1741 and MCC1741C employ phosphorsilicate passivation that protects the entire die surface area, including metalization interconnects. All dice have a minimum gold-backed thickness of 4000 Angstroms. The interconnecting metalization and bonding pads are of evaporated aluminum.

- No Frequency Compensation Required
- Short-Circuit Protection
- Offset Voltage Null Capability
- Wide Common-Mode and Differential Voltage Ranges
- Low-Power Consumption
- No Latch Up

OPERATIONAL AMPLIFIER CHIP
MONOLITHIC SILICON
INTEGRATED CIRCUIT

OUTLINE DIMENSIONS and BONDING DIAGRAM



All dimensions are nominal and in mils (10^{-3} inches).
Die Dimensions
Thickness = 8.0
Bonding Pads = 4.0 x 4.0

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value		Unit
		MCC1741C	MCC1741	
Power Supply Voltage	V^+	+18	+22	Vdc
	V^-	-18	-22	Vdc
Differential Input Signal	V_{in}	±30		Volts
Common Mode Input Swing (Note 1)	CMV_{in}	±15		Volts
Output Short Circuit Duration (Note 2)	t_S	Continuous		
Operating Temperature Range	T_A	-55 to +125		°C
Junction Temperature Range	T_J	-65 to +150		°C

Note 1. For supply voltages less than ± 15 V, the absolute maximum input voltage is equal to the supply voltage.

Note 2. Supply voltage equal to or less than 15 V.

FIGURE 1 – CIRCUIT SCHEMATIC

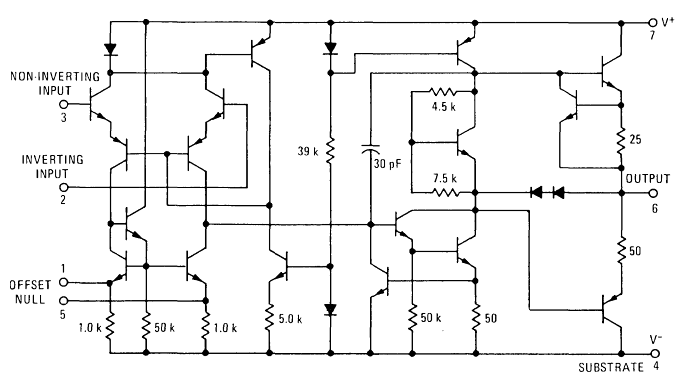
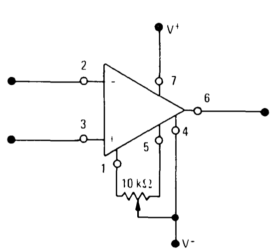


FIGURE 2 – OFFSET ADJUST CIRCUIT



This is advance information on a new introduction and specifications are subject to change without notice.

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ELECTRICAL CHARACTERISTICS ($V^+ = +15$ Vdc, $V^- = 15$ Vdc, $T_A = +25^oC$ unless otherwise noted)

Characteristic	Symbol	MCC1741 Min	MCC1741 Typ	MCC1741 Max	MCC1741C Min	MCC1741C Typ	MCC1741C Max	Unit
Open Loop Voltage Gain ($R_L = 2.0$ kΩ) ($V_o = \pm 10$ V)	A_{VOL}	50,000	200,000	–	20,000	100,000	–	–
Output Impedance (f = 20 Hz)	Z_o	–	75	–	–	75	–	Ω
Input Impedance (f = 20 Hz)	Z_{in}	–	1.0	–	–	1.0	–	Meg Ω
Output Voltage Swing	V_o							V_{peak}
(R_L = 10 kΩ)		±12	±14	–	±12	±14	–	
(R_L = 2.0 kΩ)		±10	±13	–	±10	±13	–	
Input Common-Mode Voltage Swing	CMV_{in}	–	±13	–	–	±13	–	V_{peak}
Common-Mode Rejection Ratio (f = 20 Hz)	CM_{rej}	–	90	–	–	90	–	dB
Input Bias Current	I_b	–	0.2	0.5	–	0.2	0.5	μA
Input Offset Current	$\lvert I_{io} \rvert$	–	0.03	0.2	–	0.03	0.2	μA
Input Offset Voltage ($R_S = \leq 10$ kΩ)	$\lvert V_{io} \rvert$	–	1.0	5.0	–	2.0	6.0	mV
Step Response Gain = 100	t_f	–	29	–	–	29	–	μs
	t_{pd}	–	8.5	–	–	8.5	–	μs
	dV_{out}/dt ①	–	1.0	–	–	1.0	–	V/μs
Gain = 10	t_f	–	3.0	–	–	3.0	–	μs
	t_{pd}	–	1.0	–	–	1.0	–	μs
	dV_{out}/dt ①	–	1.0	–	–	1.0	–	V/μs
Gain = 1	t_f	–	0.6	–	–	0.6	–	μs
	t_{pd}	–	0.38	–	–	0.38	–	μs
	dV_{out}/dt ①	–	0.8	–	–	0.8	–	V/μs
Power Supply Current	I_D^+	–	1.67	2.83	–	1.67	2.83	mA
	I_D^-	–	1.67	2.83	–	1.67	2.83	
DC Quiescent Power Dissipation (Power Supply = ± 15 V, V_o = 0)	P_D	–	50	85	–	50	85	mW
Positive Supply Sensitivity (V^- constant)	S^+	–	30	150	–	30	150	μV/V
Negative Supply Sensitivity (V^+ constant)	S^-	–	30	150	–	30	150	μV/V

① dV_{out}/dt = Slew Rate   See current MC1741/1741C data sheet for additional information.

PACKAGING AND HANDLING

The MCC1741/MCC1741C operational amplifier is now available as a single monolithic die or encapsulated in a variety of hermetic and plastic packages. The phosphorsilicate passivation protects the metalization and active area of the die but care must be exercised when removing the dice from the shipping carrier to avoid scratching the bonding pads. A vacuum pickup is useful for handling of dice. Tweezers are not recommended for this purpose.

The non-spill type shipping carrier consists of a compartmentalized tray and fitted cover. Die are placed in the carrier with geometry side up.

MCC1748
MCC1748C

OPERATIONAL AMPLIFIERS

Advance Information

HIGH PERFORMANCE MONOLITHIC OPERATIONAL AMPLIFIER CHIP

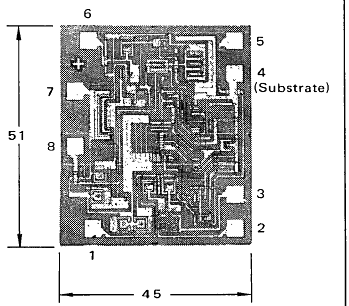
. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

The MCC1748 and MCC1748C employ phosphorsilicate passivation that protects the entire die surface area, including metalization interconnects. All dice have a minimum gold-backed thickness of 4000 Angstroms. The interconnecting metalization and bonding pads are of evaporated aluminum.

- Noncompensated MC1741G
- Single 30 pF Capacitor Compensation Required For Unity Gain
- Short-Circuit Protection
- Offset Voltage Null Capability
- Wide Common-Mode and Differential Voltage Ranges
- Low-Power Consumption
- No Latch Up

OPERATIONAL AMPLIFIER CHIP INTEGRATED CIRCUIT

MONOLITHIC SILICON EPITAXIAL PASSIVATED



All dimensions are nominal and in mils (10^{-3} inches).
Die Dimensions
Thickness = 8.0
Bonding Pads = 4.0 x 4.0

FIGURE 1 — CIRCUIT SCHEMATIC

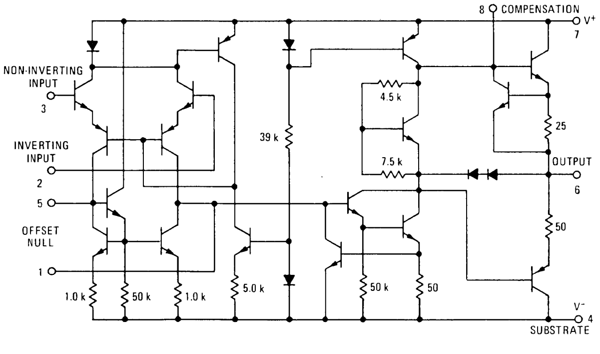
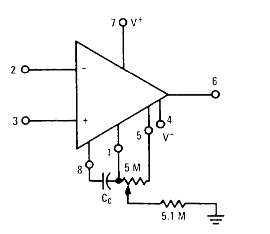


FIGURE 2 — OFFSET ADJUST AND FREQUENCY COMPENSATION



This is advance information on a new introduction and specifications are subject to change without notice.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	MCC1748	MCC1748C	Unit
Power Supply Voltage	V^+	+22	+18	Vdc
	V^-	-22	-18	
Differential Input Signal	V_{in}	±30		Volts
Common-Mode Input Swing ①	CMV_{in}	±15		Volts
Output Short Circuit Duration	t_S	Continuous		
Operating Temperature Range	T_A	-55 to +125		°C
Junction Temperature Range	T_J	-65 to +150		°C

ELECTRICAL CHARACTERISTICS (V^+ = +15 Vdc, V^- = -15 Vdc, T_A = +25°C unless otherwise noted)

		MCC1748			MCC1748C			
Characteristics	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Input Bias Current	I_b	–	0.08	0.5	–	0.08	0.5	µAdc
Input Offset Current	$\|I_{io}\|$	–	0.02	0.2	–	0.02	0.2	µAdc
Input Offset Voltage ($R_S \leq 10$ k Ω)	$\|V_{io}\|$	–	1.0	5.0	–	1.0	6.0	mVdc
Differential Input Impedance (Open-Loop, f = 20 Hz)								
Parallel Input Resistance	R_p	–	2.0	–	–	2.0	–	Megohm
Parallel Input Capacitance	C_p	–	1.4	–	–	1.4	–	pF
Common-Mode Input Impedance (f=20 Hz)	$Z_{(in)}$	–	200	–	–	200		Megohms
Common-Mode Input Voltage Swing	CMV_{in}	–	±13	–	–	±13	–	V_{pk}
Common-Mode Rejection Ratio (f = 100 Hz)	CM_{rej}	–	90	–	–	90	–	dB
Open-Loop Voltage Gain, (V_O = ±10 V, R_L = 2.0 k ohms)	A_{VOL}	50,000	200,000	–	20,000	200,000	–	V/V
Step Response (V_{in} = 20 mV, C_c = 30 pF, R_L = 2 kΩ, C_L = 100 pF)								
Rise Time	t_r	–	0.3	–	–	0.3	–	µs
Overshoot Percentage		–	5.0	–	–	5.0	–	%
Slew Rate	dV_{out}/dt	–	0.8	–	–	0.8	–	V/µs
Output Impedance (f = 20 Hz)	Z_{out}	–	75	–	–	75	–	ohms
Short-Circuit Output Current	I_{SC}	–	25	–	–	25	–	mAdc
Output Voltage Swing (R_L = 10 k ohms)	V_O	±12	±14	–	±12	±14	–	Vpk
R_L = 2 k ohms (T_A = T_{low} to t_{high})		±10	±13	–	±10	±13	–	
Power Supply Sensitivity								µV/V
V^- = constant, $R_s \leq 10$ k ohms	S+	–	30	150	–	30	150	
V^+ = constant, $R_s \leq 10$ k ohms	S-	–	30	150	–	30	150	
Power Supply Current	I_D^+	–	1.67	2.83	–	1.67	2.83	mAdc
	I_D^-	–	1.67	2.83	–	1.67	2.83	
DC Quiescent Power Dissipation (V_O = 0)	P_D	–	50	85	–	50	85	mW

① For supply voltages less than ±15 V, the Maximum Input Voltage is equal to the Supply Voltage. See current MC1748/1748C data sheet for additional information.

PACKAGING AND HANDLING

The MCC1748/MCC1748C operational amplifier is now available as a single monolithic die or encapsulated in the TO-99 hermetic package. The phosphorsilicate passivation protects the metalization and active area of the die but care must be exercised when removing the dice from the shipping carrier to avoid scratching the bonding pads. A vacuum pickup is useful for handling of dice. Tweezers are not recommended for this purpose.

The non-spill type shipping carrier consists of a compartmentalized tray and fitted cover. Die are placed in the carrier with geometry side up.

MCBC1709
MCB1709F

OPERATIONAL AMPLIFIERS

Advance Information

MONOLITHIC OPERATIONAL AMPLIFIER

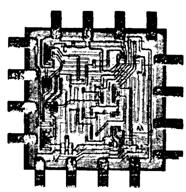
Beam-lead sealed-junction technology and fabrication make the MCBC1709 and MCB1709F devices excellent choices for military, aerospace, and commercial applications; usages requiring a high degree of reliability under environmental conditions of severe temperature extremes, mechanical shock, and high humidity. Beam-lead products employ a silicon-nitride dielectric that hermetically seals the chip, eliminating the need for a hermetic package. The beam leads are gold cantilevered structures extending from the chip. These beams bond readily to a gold metalized substrate providing one of the most reliable interconnection systems known for semiconductor devices.

- High-Performance Open Loop Gain Characteristics
  A_{VOL} = 45,000 typical
- Low Temperature Drift – ±3.0 μV/°C
- Large Output Voltage Swing – ±14 V typical @ ±15 V Supply
- Low Output Impedance – Z_{out} = 150 ohms typical

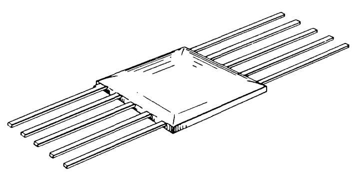
OPERATIONAL AMPLIFIER INTEGRATED CIRCUIT

MONOLITHIC SILICON

BEAM LEAD



BEAM-LEAD CHIP
MCBC1709

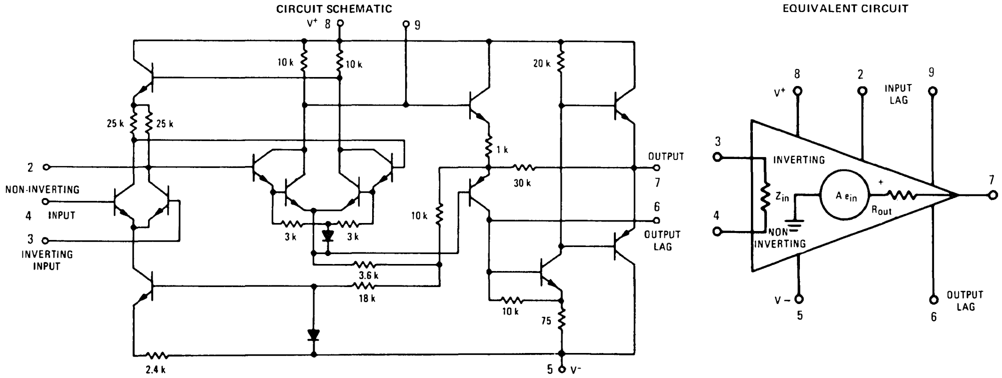


CASE 665
CERAMIC PACKAGE
MCB1709F

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+ V^-	+18 -18	Vdc
Differential Input Signal	V_{in}	±5.0	Volts
Common Mode Input Swing	CMV_{in}	$\pm V^+$	Volts
Load Current	I_L	10	mA
Output Short Circuit Duration	t_S	5.0	s
Power Dissipation Derate above T_A = +25°C	P_D	500 3.3	mW mW/°C
Operating Temperature Range	T_A	-55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

FIGURE 1



Pin numbers shown are for Case 665, refer to the chip bonding diagram for the corresponding beam connections.

This is advance information on a new introduction and specifications are subject to change without notice.

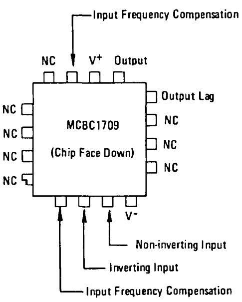
See Packaging Information Section for outline dimensions.

ELECTRICAL CHARACTERISTICS (V^+ = +15 Vdc, V^- = -15 Vdc, T_A = +25°C unless otherwise noted)

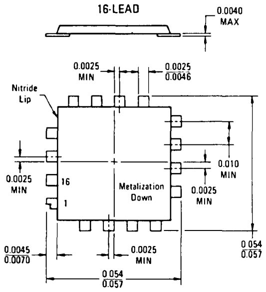
Characteristic	Symbol	MCBC1709 and MCB1709F Min	Typ	Max	Unit
Open Loop Voltage Gain (V_o = ±10 V, T_A = -55°C to +125°C)	A_{VOL}	25,000	45,000	70,000	–
Output Impedance (f = 20 Hz)	z_{out}	–	150	–	Ω
Input Impedance (f = 20 Hz)	z_{in}	150	400	–	kΩ
Output Voltage Swing (R_L = 10 kΩ) (R_L = 2.0 kΩ)	V_o	 ±12 ±10	 ±14 ±13	 – –	V_{peak}
Input Common-Mode Voltage Swing	CMV_{in}	±8.0	±10	–	V_{peak}
Common-Mode Rejection Ratio (f = 20 Hz)	CM_{rej}	70	90	–	dB
Input Bias Current (T_A = +25°C) (T_A = -55°C)	I_b	 – –	 0.2 0.5	 0.5 1.5	µA
Input Offset Current (T_A = +25°C) (T_A = -55°C) (T_A = +125°C)	$\|I_{io}\|$	 – – –	 0.05 – –	 0.2 0.5 0.2	µA
Input Offset Voltage (T_A = +25°C) (T_A = -55°C to +125°C)	$\|V_{io}\|$	 – –	 1.0 –	 5.0 6.0	mV
Step Response Gain = 100, 5.0% overshoot, R_1 = 1.0 kΩ, R_2 = 100 kΩ, R_3 = 1.5 kΩ, C_1 = 100 pF, C_2 = 3.0 pF	 t_f t_{pd} dV_{out}/dt ①	 – – –	 0.8 0.38 12	 – – –	 µs µs V/µs
Gain = 10, 10% overshoot, R_1 = 1.0 kΩ, R_2 = 10 kΩ, R_3 = 1.5 kΩ, C_1 = 500 pF, C_2 = 20 pF	t_f t_{pd} dV_{out}/dt ①	– – –	0.6 0.34 1.7	– – –	µs µs V/µs
Gain = 1, 5.0% overshoot, R_1 = 10 kΩ, R_2 = 10 kΩ, R_3 = 1.5 kΩ, C_1 = 5000 pF, C_2 = 200 pF	t_f t_{pd} dV_{out}/dt ①	– – –	2.2 1.3 0.25	– – –	µs µs V/µs
Average Temperature Coefficient of Input Offset Voltage (R_S = 50 Ω, T_A = -55°C to +125°C) ($R_S \leq$ 10 kΩ, T_A = -55°C to +125°C)	$\|TC_{Vio}\|$	 – –	 3.0 6.0	 – –	µV/°C
DC Power Dissipation (Power Supply = ±15 V, V_o = 0)	P_D	–	80	165	mW
Positive Supply Sensitivity (V^- constant)	S^+	–	25	150	µV/V
Negative Supply Sensitivity (V^+ constant)	S^-	–	25	150	µV/V

① dV_{out}/dt = Slew Rate

BONDING DIAGRAM



Silicon Thickness = 2.0 mils nominal



Leads true position within 0.002 total.

PACKAGING AND HANDLING

The MCBC1709 beam-lead sealed-junction linear integrated circuit is available in chip form (non-encapsulated) as shown in the outline dimensional drawing. The shipping carrier for chips is a 2" square glass plate on which the chips are placed. A thin layer of polymer film covers the plate and retains the chips in place. The chips do not adhere to the film when it is lifted to remove them from the carrier. Care must be exercised when removing the chips from the carrier to ensure that the beams are not bent. A vacuum pickup is useful for this purpose.

See MC1709, MC1709C data sheet for typical characteristics curves.

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MCBC1741
MCB1741F

OPERATIONAL AMPLIFIERS

Advance Information

MONOLITHIC OPERATIONAL AMPLIFIER

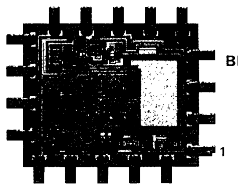
Beam-lead sealed-junction technology and fabrication make the MCBC1741 and MCB1741F devices excellent choices for military, aerospace, and commercial applications; usages requiring a high degree of reliability under environmental conditions of severe temperature extremes, mechanical shock, and high humidity. Beam-lead products employ a silicon-nitride dielectric that hermetically seals the chip, eliminating the need for a hermetic package. The beam leads are gold cantilevered structures extending from the chip. These beams bond readily to a gold metalized substrate providing one of the most reliable interconnection systems known for semiconductor devices.

- No Frequency Compensation Required
- Short-Circuit Protection
- Offset Voltage Null Capability
- Wide Common-Mode and Differential Voltage Ranges
- Low-Power Consumption
- No Latch Up

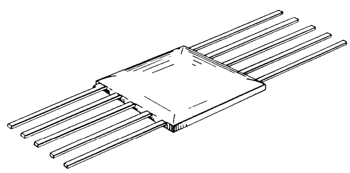
OPERATIONAL AMPLIFIER INTEGRATED CIRCUIT

MONOLITHIC SILICON

BEAM LEAD



BEAM-LEAD CHIP
MCBC1741



MCB1741F
CASE 665
CERAMIC PACKAGE

SCHEMATIC PIN CONNECTIONS

Chip	A	B	C	D	E	F	G
"F" Package	2	3	4	5	6	7	8

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+ V^-	+22 -22	Vdc
Differential Input Signal	V_{in}	±30	Volts
Common Mode Input Swing (Note 1)	CMV_{in}	±15	Volts
Output Short Circuit Duration (Note 2)	t_S	Continuous	
Power Dissipation Derate above T_A = +25°C (Flat Package)	P_D	500 3.3	mW mW/°C
Operating Temperature Range	T_A	-55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

Note 1. For supply voltages less than ± 15 V, the absolute maximum input voltage is equal to the supply voltage.
Note 2. Supply voltage equal to or less than 15 V.

FIGURE 1 — CIRCUIT SCHEMATIC

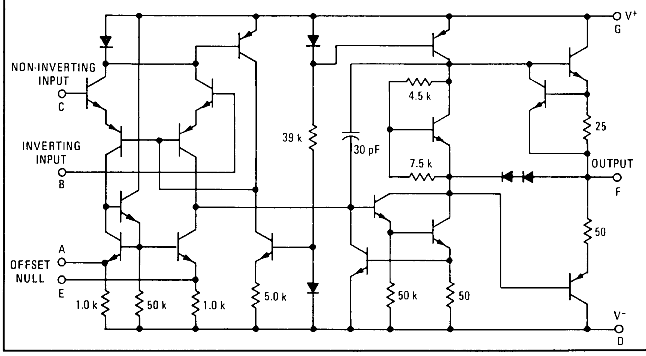
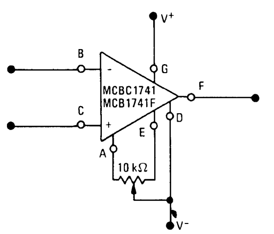


FIGURE 2 — OFFSET ADJUST CIRCUIT



This is advance information on a new introduction and specifications are subject to change without notice.
See Packaging Information Section for outline dimensions.

ELECTRICAL CHARACTERISTICS (V^+ = +15 Vdc, V^- = −15 Vdc, T_A = +25°C unless otherwise noted)

Characteristic	Symbol	MCBC1741, MCB1741F Min	Typ	Max	Unit
Open Loop Voltage Gain (R_L = 2.0 kΩ)	A_{VOL}				–
(V_O = ±10 V, T_A = +25°C)		50,000	200,000	–	
(V_O = ± 10 V, T_A = −55 to +125°C)		25,000	–	–	
Output Impedance (f = 20 Hz)	Z_o	–	75	–	Ω
Input Impedance (f = 20 Hz)	Z_{in}	0.3	1.0	–	MegΩ
Output Voltage Swing	V_o				V_{peak}
(R_L = 10 kΩ)		±12	±14	–	
(R_L = 2.0 kΩ)		±10	±13	–	
(R_L = 2.0 kΩ, T_A = −55 to +125°C)		±10	–	–	
Input Common-Mode Voltage Swing	CMV_{in}	±12	±13	–	V_{peak}
Common-Mode Rejection Ratio (f = 20 Hz)	CM_{rej}	70	90	–	dB
Input Bias Current	I_b				μA
(T_A = +25°C)		–	0.2	0.5	
(T_A = −55°C)		–	0.5	1.5	
Input Offset Current	$\|I_{io}\|$				μA
(T_A = +25°C)		–	0.03	0.2	
(T_A = −55 to +125°C)		–	–	0.5	
Input Offset Voltage	$\|V_{io}\|$				mV
(T_A = +25°C)		–	1.0	5.0	
(T_A = −55°C to +125°C)		–	–	6.0	
Step Response					
Gain = 100, R_1 = 1.0 kΩ, R_2 = 100 kΩ, R_3 = 1.0 kΩ	t_f	–	29	–	μs
	t_{pd}	–	8.5	–	μs
	dV_{out}/dt ①	–	1.0	–	V/μs
Gain = 10, R_1 = 1.0 kΩ, R_2 = 10 kΩ, R_3 = 1.0 kΩ	t_f	–	3.0	–	μs
	t_{pd}	–	1.0	–	μs
	dV_{out}/dt ①	–	1.0	–	V/μs
Gain = 1, R_1 = 10 kΩ, R_2 = 10 kΩ, R_3 = 5.0 kΩ	t_f	–	0.6	–	μs
	t_{pd}	–	0.38	–	μs
	dV_{out}/dt ①	–	0.8	–	V/μs
Average Temperature Coefficient of Input Offset Voltage	$\|TC_{Vio}\|$				μV/°C
(R_S = 50 Ω, T_A = −55°C to +125°C)		–	3.0	–	
(R_S = 10 kΩ, T_A = −55°C to +125°C)		–	6.0	–	
Average Temperature Coefficient of Input Offset Current (T_A = −55 to +125°C)	$\|TC_{Vio}\|$	–	50	–	pA/°C
DC Power Dissipation (Power Supply = ±15 V, V_o = 0)	P_D	–	50	85	mW
Positive Supply Sensitivity (V^- constant)	S^+	–	30	150	μV/V
Negative Supply Sensitivity (V^+ constant)	S^-	–	30	150	μV/V
Power Bandwidth (A_v = 1, R_L = 2.0 kΩ, THD = 5%, V_o = 20 V_{p-p})	PBW	–	10	–	kHz

① dV_{out}/dt = Slew Rate

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TYPICAL CHARACTERISTICS (continued)

(V^+ = +15 Vdc, V^- = -15 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 3 – POWER BANDWIDTH (LARGE SIGNAL SWING versus FREQUENCY)

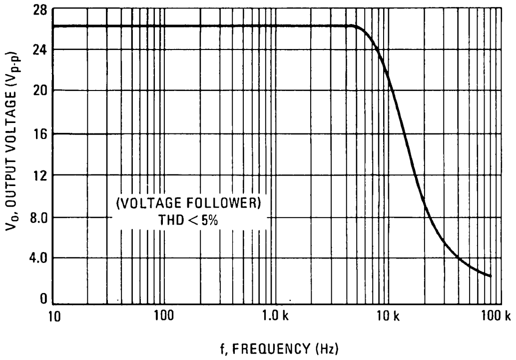


FIGURE 4 – OPEN LOOP FREQUENCY RESPONSE

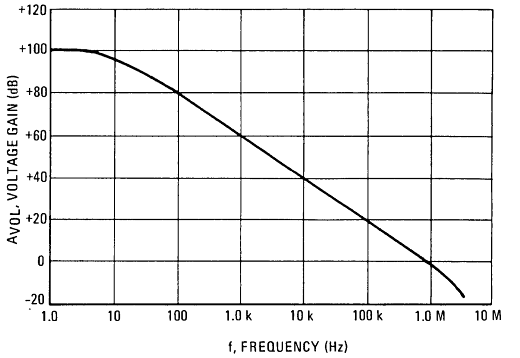


FIGURE 5 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

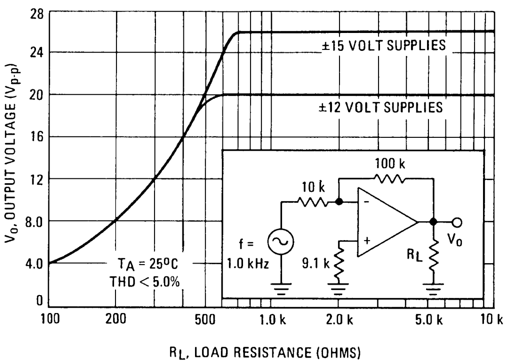


FIGURE 6 – COMMON-MODE REJECTION RATIO versus FREQUENCY

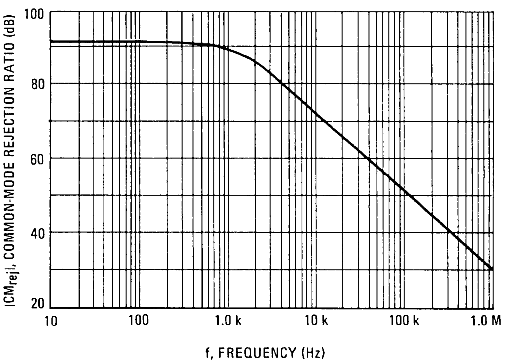


FIGURE 7 – INPUT OFFSET CURRENT versus TEMPERATURE

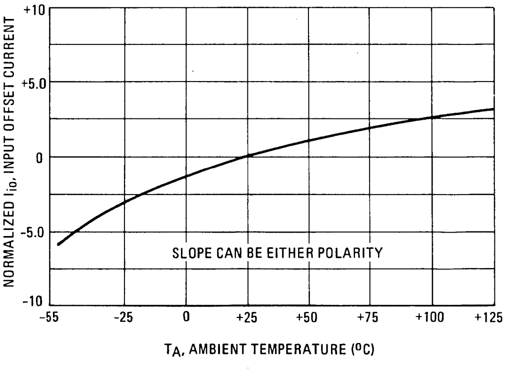
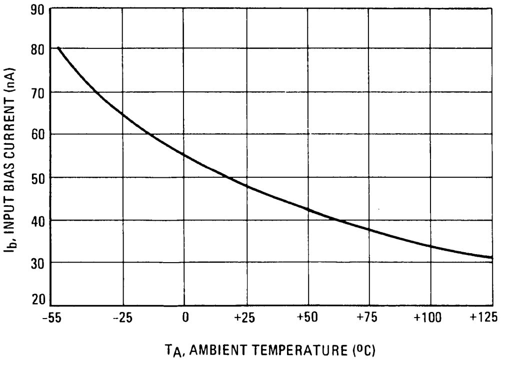


FIGURE 8 – INPUT BIAS CURRENT versus TEMPERATURE



6

TYPICAL CHARACTERISTICS (continued)

(V^+ = +15 Vdc, V^- = −15 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 9 – POWER DISSIPATION versus POWER SUPPLY VOLTAGE

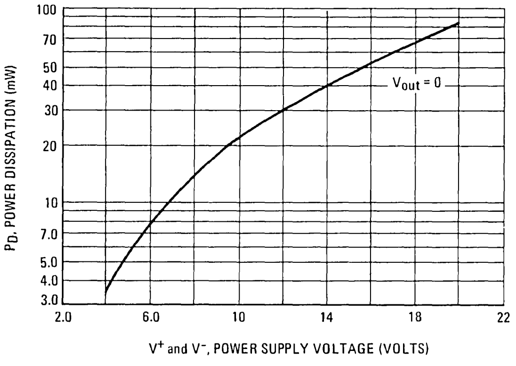


FIGURE 10 – OUTPUT NOISE versus SOURCE RESISTANCE

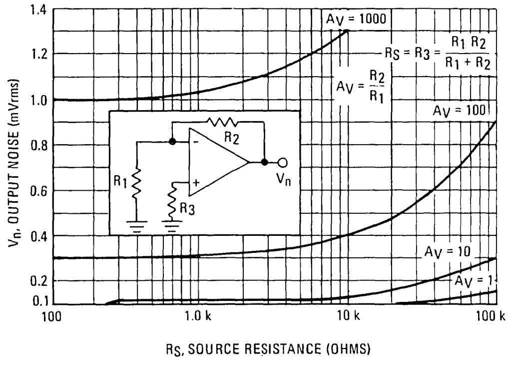
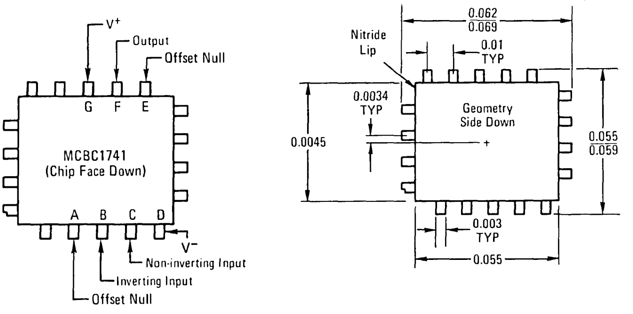


FIGURE 11 – BONDING DIAGRAM



Silicon Thickness = 2.0 mils nominal

PACKAGING AND HANDLING

The MCBC1741 beam-lead sealed-junction linear integrated circuit is available in chip form (non-encapsulated) as shown in the outline dimensional drawing. The shipping carrier for chips is a 2" square glass plate on which the chips are placed. A thin layer of polymer film covers the plate and retains the chips in place. The chips do not adhere to the film when it is lifted to remove them from the carrier. Care must be exercised when removing the chips from the carrier to ensure that the beams are not bent. A vacuum pickup is useful for this purpose.

MCH1002P

DUAL POWER DRIVER

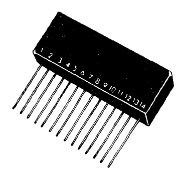
Advance Information

DUAL POWER DRIVER

. . . designed for magnetic relay and lamp-driving applications.

- MHTL Dual 4-Input Line Driver (MC662) for the Input Logic
- Output Current $-I_{OL}$ = 0.5 Adc (Max)
- Output Voltage – BV_{CEO} = 40 Vdc

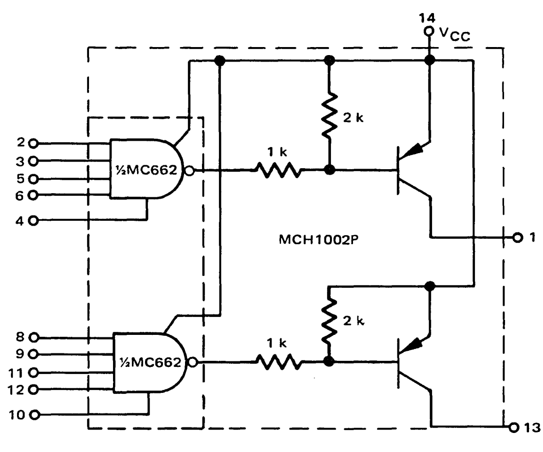
DUAL POWER DRIVER HYBRID MICROCIRCUIT



PLASTIC PACKAGE CASE 625

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	18	Vdc
Input Voltage	V_{in}	-1.0/+18	Vdc
Output Current	I_{OL}	0.5	Adc
Output Voltage	BV_{CEO}	40	Vdc
Input Current	I_{in}	30	mAdc
Power Dissipation Derate above T_A = 25°C	P_D	1.0 10	Watts mW/°C
Operating Temperature Range	T_A	-30 to +75	°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +125	°C



See Packaging Information Section for outline dimensions.

ELECTRICAL CHARACTERISTICS (Each Driver, T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Input					
Reverse Current (Each Input) (V_R = 16 Vdc, V_{CCL} = 14 Vdc)	I_R	–	–	2.0	μAdc
Forward Current (Each Input) (V_F = 1.5 V, V_{CCH} = 16 Vdc)	I_F	–	–	1.2	mAdc
Power Drain Current (Total Device) (I_L = 0 mAdc, V_{CCH} = 16 Vdc, V_{IL} = 6.5 V)	I_{CCL}	–	2.0	5.0	mAdc
Power Drain Current (Total Device) (I_L = 0 mAdc, V_{IH} = 8.5 V, V_{CCH} = 16 Vdc)	I_{CCH}	–	40	55	mAdc
Output					
Output Voltage (V_{IH} = 8.5 V, V_{CC} = 15 V, I_L = 500 mAdc)	V_{OH}	14.3	–	–	Vdc
Output Current (V_{IL} = 6.5 V, V_{CC} = 15 V)	I_L	–	–	1.0	μAdc
Collector-Emitter Breakdown Voltage of the Output Transistor (I_C = 10 mAdc)	BV_{CEO}	40	–	–	Vdc
Switching Times (See Note 1)					
Turn-On-Time (I_L = 500 mA, V_{IH} = 15 Vdc, V_{CC} = 15 Vdc)	t_{on}	–	115	–	ns
Turn-Off-Time (V_{IL} = 0, V_{CC} = 15 Vdc)	t_{off}	–	260	–	ns

Note 1: Measured at 50% points.

DEFINITIONS

I_{CCH}	V_{CC} current drain when all inputs are high
I_{CCL}	V_{CC} current drain when all inputs are low
I_F	Forward current of input diodes for unit input load
I_L	Test current flowing into output pin when input is low
I_R	Reverse current of input diodes with V_R applied
t_{off}	Turn-off delay time
t_{on}	Turn-on delay time
V_{CC}	Device power supply voltage
V_F	Input voltage when measuring I_F
V_{IH}	Threshold voltage for high input voltage state
V_{IL}	Threshold voltage for low input voltage state
V_{OH}	Output high voltage state with I_{OH} flowing out of pin
V_R	Reverse voltage for input diode leakage test
V_{CCL}	Low power supply voltage
V_{CCH}	High power supply voltage

MCH2005F

POWER DRIVER

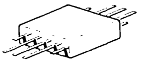
Advance Information

DARLINGTON POWER DRIVER

. . . designed for applications requiring large current pulses for a short duration.

- High Current Gain — h_{FE} = 1000 (Min) @ I_C = 5.0 A
- High Speed Saturated Switch —
  t_{on} = 350 ns (Max) @ I_C = 5.0 A
  t_{off} = 450 ns (Max) @ I_C = 5.0 A

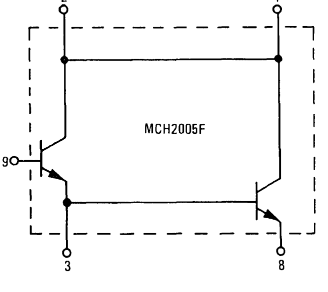
DARLINGTON POWER DRIVER HYBRID MICROCIRCUIT



CERAMIC PACKAGE
CASE 628
TO-91

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	30	Vdc
Collector-Base Voltage	V_{CB}	50	Vdc
Emitter-Base Voltage	V_{EB}	7.0	Vdc
Collector Current — Continuous	I_C	6.0	Adc
Total Device Dissipation @ T_A = 25°C Derate above T_A = 25°C	P_D	500 2.86	mW mW/°C
Total Device Dissipation @ T_C = 25°C Derate above T_A = 25°C	P_D	5.0 28.6	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C



This is advance information and specifications are subject to change without notice.
See Packaging Information Section for outline dimensions.

ELECTRICAL CHARACTERISTICS ($T_A = 25^oC$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage* (I_C = 10 mAdc)	BV_{CEO}*	30	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc)	BV_{EBO}	7.0	–	Vdc
Collector Cutoff Current (V_{CB} = 50 Vdc)	I_{CBO}	–	2.0	μAdc
ON CHARACTERISTICS				
DC Current Gain*	h_{FE}*			–
(I_C = 1.0 Adc, V_{CE} = 10 Vdc)		1000	–	
(I_C = 5.0 Adc, V_{CE} = 10 Vdc)		1000	–	
Collector-Emitter Saturation Voltage*	$V_{CE(sat)}$*			Vdc
(I_C = 1.0 Adc, I_B = 1.0 mAdc)		–	1.2	
(I_C = 5.0 Adc, I_B = 5.0 mAdc)		–	2.5	
Base-Emitter Saturation Voltage*	$V_{BE(sat)}$*			Vdc
(I_C = 1.0 Adc, I_B = 1.0 mAdc)		–	1.5	
(I_C = 5.0 Adc, I_B = 5.0 mAdc)		–	3.0	
SMALL-SIGNAL CHARACTERISTICS				
Current-Gain—Bandwidth Product (I_E = 100 mAdc, V_{CE} = 10 Vdc)	f_T	100	–	MHz
SWITCHING CHARACTERISTICS				
Turn-On Time* (V_{CC} = 6.75 Vdc, I_C = 5.0 Adc, I_B = 5.0 mAdc) Figure 1	t_{on}*	–	350	ns
Turn-Off Time* (V_{CC} = 6.75 Vdc, I_C = 5.0 Adc, I_B = 5.0 mAdc) Figure 1	t_{off}*	–	450	ns

*Pulse Test: Pulse Width ≤ 2.0 μs, Duty Cycle ≤ 2.0%.

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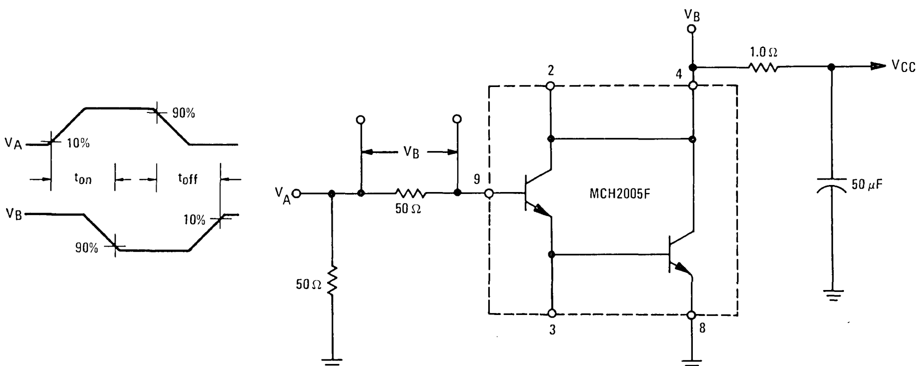
FIGURE 1



MCH2870MR
MCH2870CR

POWER OPERATIONAL AMPLIFIER

. . . designed as a high-gain internally-compensated hybrid power operational amplifier that can deliver load currents up to ±300 mAdc typ. This device is ideally suited for driving low impedance loads. Typical applications include buffer, line driver and servo/synchro amplifier or power amplifier with operating characteristics as a function of the external feedback components.

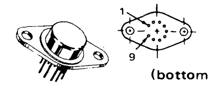
Output current is internally limited to 100 mA (typ) with an option of 200 mA (by shorting pins 2 and 4). With the addition of two external resistors, current can be limited to any value between 100 mA and 300 mA.

The MCH2870MR is specified over the military temperature range (-55°C to +125°C) and the MCH2870CR over the commercial temperature range (0°C to +75°C).

- High Current Capability to ±300 mA typ
- Internally Compensated
- High Open-Loop Voltage Gain – 200,000 typ
- Low Open Loop Output Impedance – 10 Ohms typ
- Offset Voltage Null Capability

POWER OPERATIONAL AMPLIFIER INTEGRATED CIRCUIT

SILICON EPITAXIAL PASSIVATED



CASE 614
METAL PACKAGE

TYPICAL APPLICATIONS

FIGURE 1 – POWER OPERATIONAL AMPLIFIER

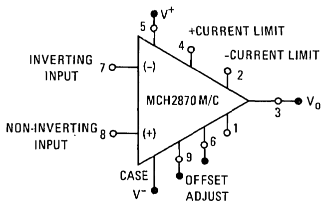


FIGURE 2 – VOLTAGE OFFSET NULL CIRCUIT

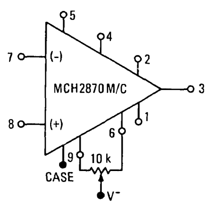
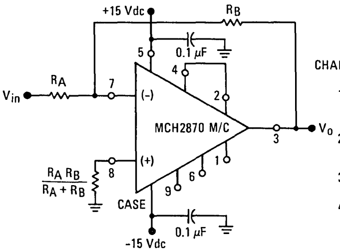
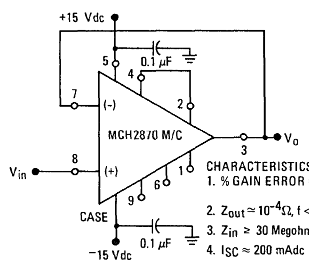


FIGURE 3 – TYPICAL INVERTING AMPLIFIER



CHARACTERISTICS
1. $A_V = \frac{-R_B}{R_A}$
2. $Z_{out} \approx \frac{R_A + R_B}{R_A} 10^{-4} \Omega$
3. $Z_{in} \approx R_A$
4. $I_{SC} \approx 200$ mA

FIGURE 4 – UNITY GAIN VOLTAGE FOLLOWER



CHARACTERISTICS:
1. % GAIN ERROR = $\frac{(V_0 - V_{in})}{V_{in}} 10^2 \approx 0.001\%$
2. $Z_{out} \approx 10^{-4} \Omega$, f < 20 Hz
3. $Z_{in} \geq 30$ Megohms, f < 20 Hz
4. $I_{SC} \approx 200$ mAdc

See Packaging Information Section for outline dimensions.

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MAXIMUM RATINGS (T_C = +25°C unless otherwise noted)

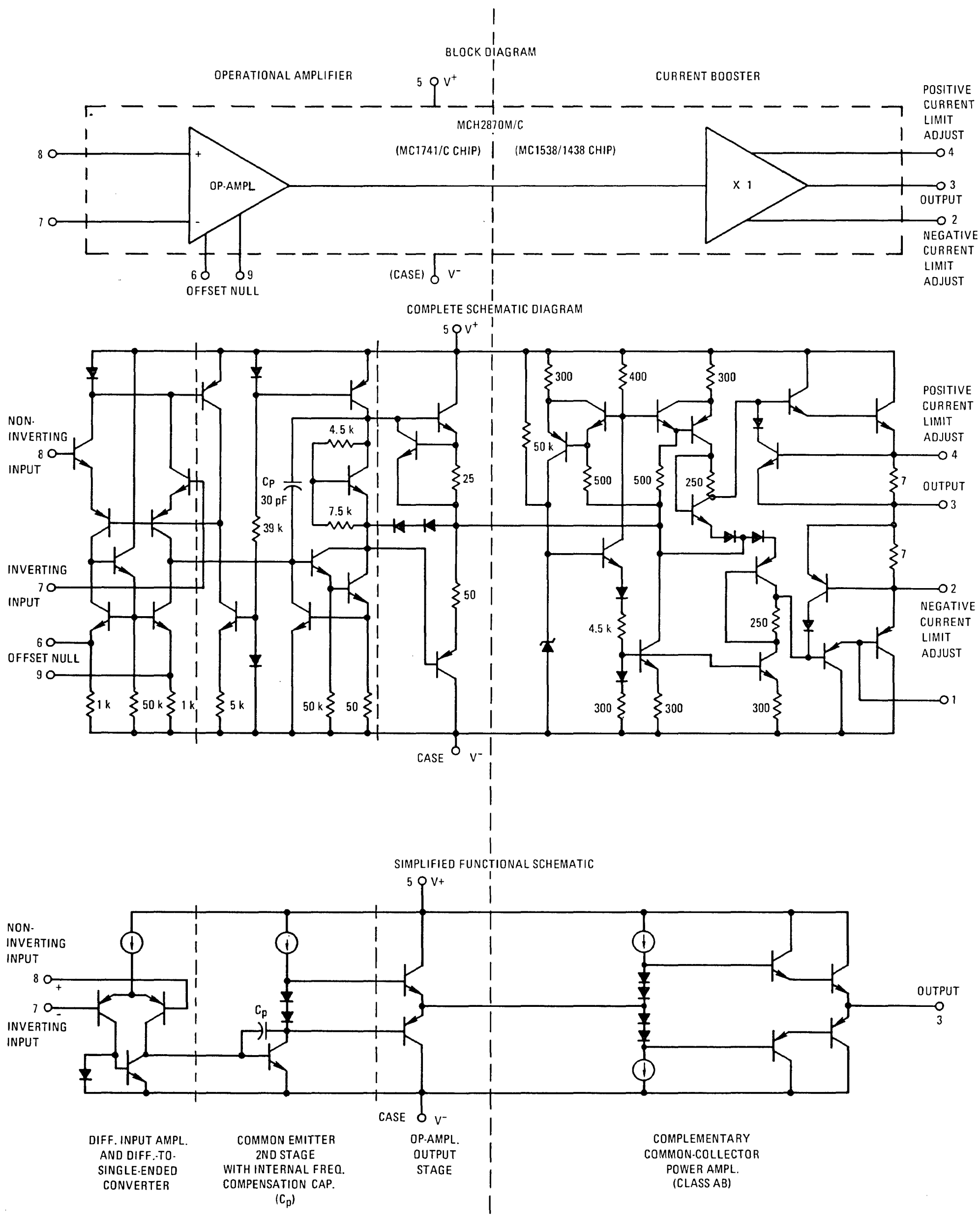
Rating	Symbol	MCH2870MR	MCH2870CR	Unit
Power Supply Voltage	V^+ V^-	+22 -22	+18 -18	Vdc
Differential Input Signal	V_{in}	±30		Volts
Common-Mode Input Swing	CMV_{in}	±15		Volts
Output Short Circuit Duration	t_S	Continuous		
Power Dissipation and Thermal Characteristics T_A = +25°C Derate above T_A = +25°C Thermal Resistance, Junction to Air	 P_D $1/\theta_{JA}$ θ_{JA}	 2.4 16 62		 Watts mW/°C °C/W
T_C = +25°C Derate above T_C = +25°C Thermal Resistance, Junction to Case	P_D $1/\theta_{JC}$ θ_{JC}	9.0 60 16.7		Watts mW/°C °C/W
Operating Temperature Range	T_A	-55 to +125	0 to +75	°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +175		°C

ELECTRICAL CHARACTERISTICS (V^+ = +15 Vdc, V^- = -15 Vdc, T_C = +25°C unless otherwise noted)

		MCH2870MR			MCH2870CR			
Characteristics	Symbol	Min	Typ	Max	Min	Typ	Max	Unit
Input Bias Current T_C = +25°C T_C = T_{low} to T_{high} (See Note 1)	I_b	 – –	 0.2 –	 0.5 1.5	 – –	 0.2 –	 0.5 0.8	μAdc
Input Offset Current T_C = +25°C T_C = T_{low} to T_{high}	$\|I_{io}\|$	 – –	 0.03 –	 0.2 0.5	 – –	 0.03 –	 0.2 0.3	μAdc
Input Offset Voltage ($R_S \leq$ 10 kΩ) T_C = +25°C T_C = T_{low} to T_{high}	$\|V_{io}\|$	 – –	 1.0 –	 5.0 6.0	 – –	 2.0 –	 6.0 7.5	mVdc
Differential Input Impedance (Open-Loop, f = 20 Hz) Parallel Input Resistance Parallel Input Capacitance	 R_p C_p	 0.3 –	 1.0 6.0	 – –	 0.3 –	 1.0 6.0	 – –	 Megohm pF
Common-Mode Input Impedance (f = 20 Hz)	Z_{in}	–	200	–	–	200	–	Megohms
Common-Mode Input Voltage Swing	CMV_{in}	±12	±13	–	±12	±13	–	V_{pk}
Equivalent Input Noise Voltage A_V = 100, R_s = 10 k ohms, f = 1.0 kHz, BW = 1.0 Hz	e_n	 –	 45	 –	 –	 45	 –	nV/(Hz)$^{1/2}$
Common-Mode Rejection Ratio (f = 100 Hz)	CM_{rej}	70	90	–	70	90	–	dB
DC Open-Loop Voltage Gain, (V_{out}=±10 V, R_L=300 ohms) T_C = +25°C T_C = T_{low} to T_{high}	A_{VOL}	 50,000 25,000	 200,000 –	 – –	 20,000 15,000	 100,000 –	 – –	V/V
Power Bandwidth A_V = 1, R_L = 300 ohms, THD ≤ 5%, V_{out} = 20 Vp-p	P_{BW}	 –	12	–	–	12	 –	kHz
Unity Gain Crossover Frequency (open-loop)		–	1.1	–	–	1.1	–	MHz
Phase Margin (closed loop, unity gain)		–	65	–	–	65	–	degrees
Gain Margin (closed loop, unity gain)		–	11	–	–	11	–	dB
Slew Rate (Unity Gain)	dV_{out}/dt	–	0.8	–	–	0.8	–	V/μs
Output Impedance (open loop f = 20 Hz)	Z_{out}	–	10	–	–	10	–	ohms
Short-Circuit Output Current (See Figure 6) R1 = R2 = ∞ Pins 2 and 4 shorted Adjustable Range	I_{SC}	 75 – –	 100 200 100-300	 125 – –	 65 – –	 100 200 100-300	 140 – –	mAdc
Output Voltage Swing R_L = 300 ohms R_L = 300 ohm (T_C = T_{low} to T_{high})	V_{out}	 ±12 ±10	 ±13 –	 – –	 ±11 ±10	 ±12 –	 – –	Vpk
Power Supply Sensitivity (dc) V^- = constant, $R_s \leq$ 10 k ohms V^+ = constant, $R_s \leq$ 10 k ohms	 S+ S-	 – –	 30 30	 150 150	 – –	 30 30	 200 200	μV/V
Power Supply Current	I_D^+ I_D^-	– –	7.7 7.7	13 13	– –	7.7 7.7	16.5 16.5	mAdc
DC Quiescent Power Dissipation V_{in} = 0	P_D	 –	 225	 390	 –	 225	 500	mW

Note 1: T_{low}: 0°C for MCH2870CR
-55°C for MCH2870MR
T_{high}: +75°C for MCH2870CR
+125°C for MCH2870MR

FIGURE 5 – MCH2870M/C DEVICE CONFIGURATION



TYPICAL CHARACTERISTICS

(V^+ = +15 Vdc, V^- = -15 Vdc, T_A = +25°C unless otherwise noted)

FIGURE 6 – SHORT-CIRCUIT CURRENT versus R1 OR R2 (100 mA TO 300 mA)

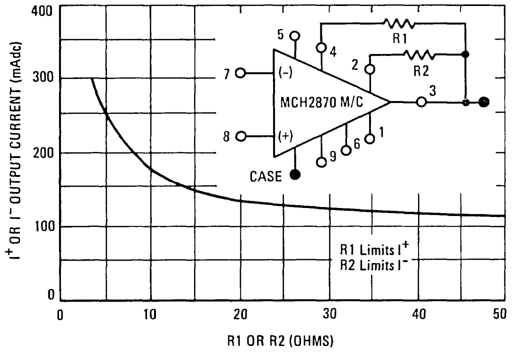


FIGURE 7 – DC SAFE OPERATING AREA

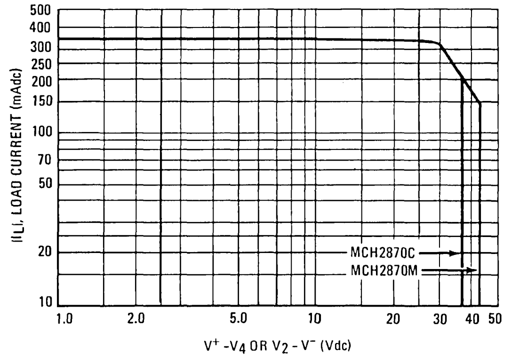


FIGURE 8 – POWER BANDWIDTH (LARGE SIGNAL SWING versus FREQUENCY)

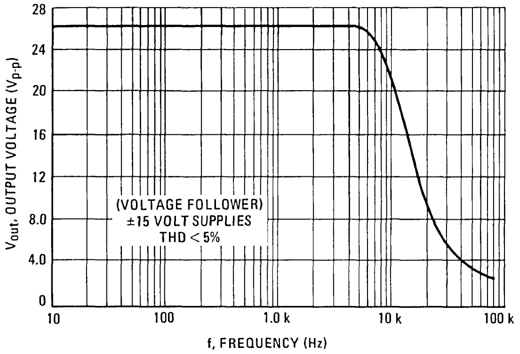


FIGURE 9 – OPEN LOOP FREQUENCY RESPONSE

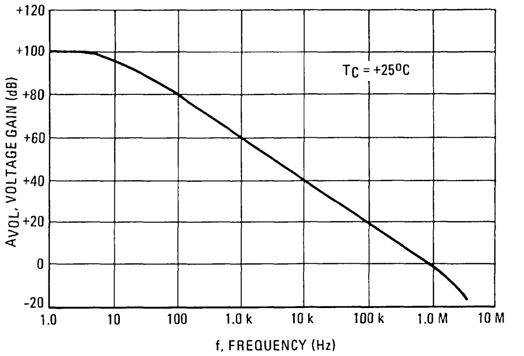


FIGURE 10 – OUTPUT NOISE versus SOURCE RESISTANCE

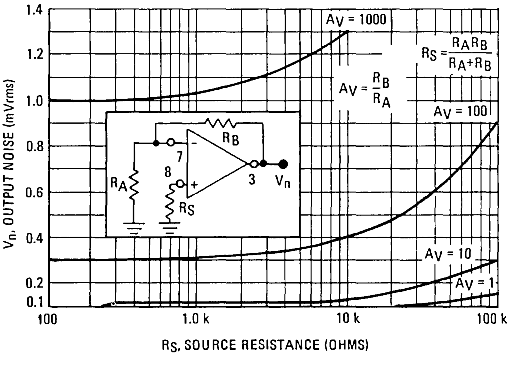
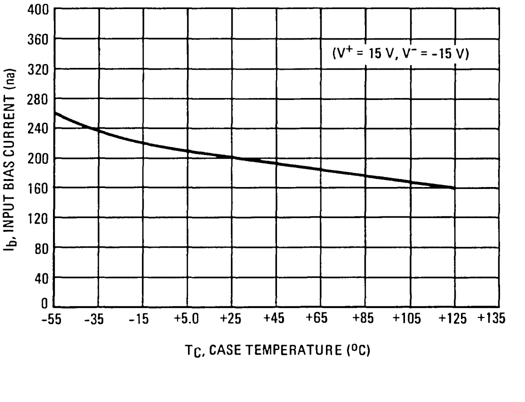


FIGURE 11 – INPUT BIAS CURRENT versus TEMPERATURE



TYPICAL CHARACTERISTICS (continued)

FIGURE 12 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

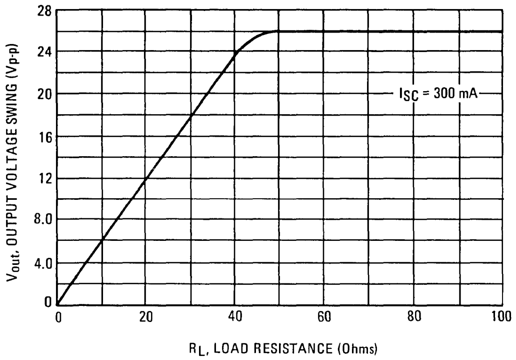
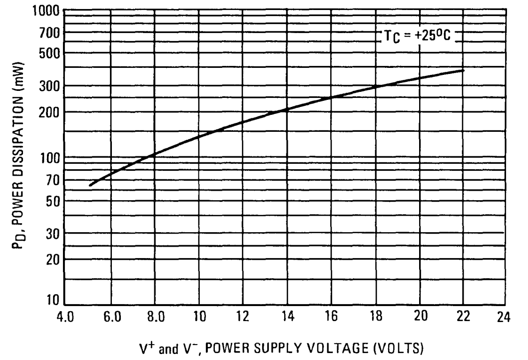


FIGURE 13 – POWER DISSIPATION versus POWER SUPPLY VOLTAGE



TYPICAL APPLICATIONS

FIGURE 14 – PROGRAMMABLE VOLTAGE SOURCE

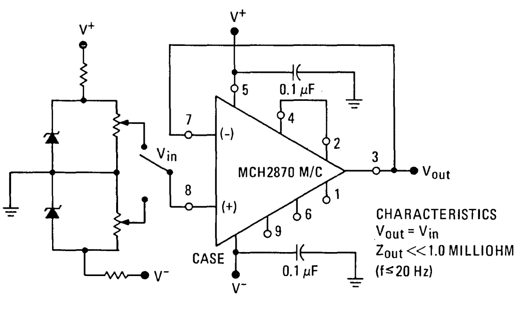


FIGURE 15 – CONSTANT CURRENT SOURCE OR TRANSCONDUCTANCE AMPLIFIER

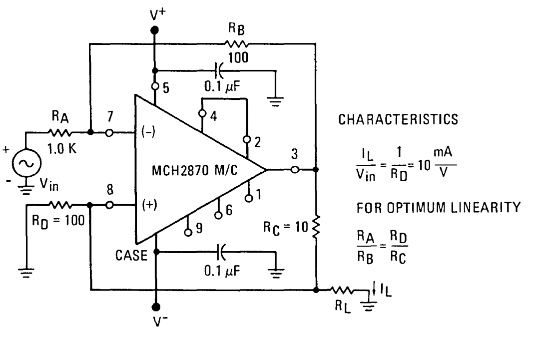


FIGURE 16 – POWER SUPPLY SPLITTER

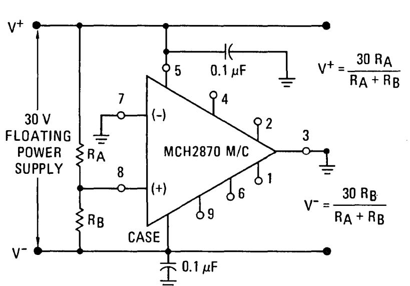
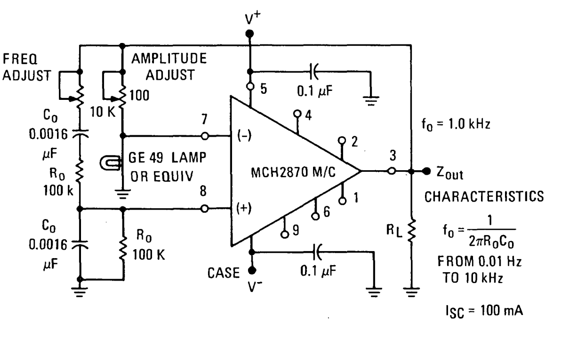
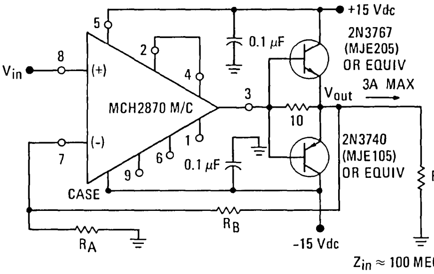


FIGURE 17 – WIEN BRIDGE OSCILLATOR



TYPICAL APPLICATIONS (continued)

FIGURE 18 — EXTERNAL CURRENT BOOSTING



$Z_{in} \approx$ 100 MEGOHMS

for $\frac{R_B}{R_A} \leqslant 100$

$A_V \approx \frac{1 + R_B}{R_A}$

$Z_{out} <$ 1 MILLIOHM

MCH2890R

DUAL POWER DRIVER

Advance Information

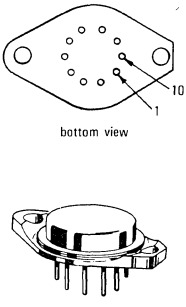
HYBRID DUAL POWER DRIVER

The MCH2890 Dual Power Driver is capable of driving a wide variety of inductive and resistive loads; included are hammer solenoids in high-speed digital printers, relays, lamps, paper-tape punches, and stepper motors in computer-operated plotters.

- High Current – to 6.0 Amperes
- High Breakdown Voltage – BV_{CEX} = 120 Volts min
- MTTL Compatibility
- Separate Integrated Circuit and Darlington Power Grounds
- Low V_{sat} at 3.0 and 6.0 Amperes
- Low Leakage Current – 0.1 μA typ

DUAL POWER DRIVER

HYBRID SILICON INTEGRATED CIRCUIT

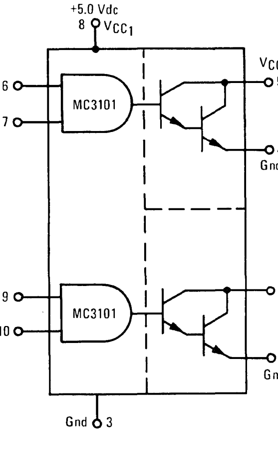


CASE 685
METAL PACKAGE

6

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector Current	I_C		A
Peak		8.0	
Continuous		1.0	
Collector Emitter Breakdown Voltage Minimum at $I_C \leqslant 0.5$ mA	BV_{CEX} (pins 1, 5)	120	Vdc
Power Supply Voltage (Integrated Circuit)	V_{CC1}	7.0	Vdc
Power Dissipation and Thermal Characteristics			
T_A = 25°C	P_D	3.75	Watts
Derate above T_A = 25°C	$1/\theta JA$	25	mW/°C
Thermal Resistance, Junction to Air	θ_{JA}	40	°C/W
T_C = 25°C	P_D	25	Watts
Derate above T_C = 25°C	$1/\theta_{JC}$	167	mW/°C
Thermal Resistance, Junction to Case	θ_{JC}	6.0	°C/W
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +175	°C

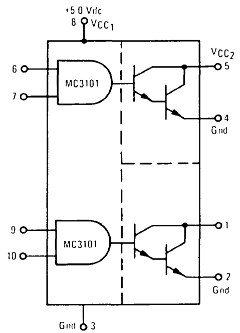


This is advance information on a new introduction and specifications are subject to change without notice.

See Packaging Information Section for outline dimensions.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one power driver. The other power driver is tested in the same manner.



TEST CURRENT/VOLTAGE VALUES

	AMPERES		mA			VOLTS								
	I_{OL1}	I_{OL2}	I_{in}	I_D	$I_{C(max)}$	V_{IH}	V_{IL}	V_F	V_R	V_{CC1}	V_{CC2}	V_{CCIL}	V_{CCIH}	V_{RH}
0°C	–	–	–	–	–	2.0	–	0.4	–	5.0	–	4.5	5.5	4.0
+25°C	3.0	6.0	1.0	−10	0.5	1.8	1.1	0.4	2.4	5.0	90	4.5	5.5	4.0
+75°C	–	–	–	–	–	1.8	–	0.4	–	5.0	–	4.5	5.5	4.0

TEST LIMITS

Characteristics	Symbol	Pin Under Test	0°C Min	0°C Max	+25°C Min	+25°C Typ	+25°C Max	+75°C Min	+75°C Max	Unit
Input Forward Current	I_F	6	–	−2.0	–	–	−2.0	–	−2.0	mAdc
Input Leakage Current	I_R	6	–	50	–	–	50	–	50	μAdc
Input Breakdown Voltage	BV_{in}	6	–	–	5.5	–	–	–	–	Vdc
Input Clamp Voltage	V_D	6	–	–	–	–	−1.5	–	–	Vdc
Output Voltage (See Figure 1)	V_{OL1}	5	–	–	–	–	1.5	–	–	Vdc
	V_{OL2}	5	–	–	–	–	2.5	–	–	
	BV_{CEX}	5	–	–	120	–	–	–	–	
Output Leakage Current	I_{CEX}	5	–	–	–	0.1	–	–	–	μAdc
Output Power Supply Drain Current	I_{PDL}	8	–	–	–	–	30	–	–	mAdc
Output Power Supply Drain Current	I_{PDH}	8	–	–	–	–	120	–	–	mAdc
Switching Parameters (See Figure 2) Turn-On Delay Time	t_{pd-}	5,6	–	–	–	0.26	–	–	–	μs
Turn-Off Delay Time	t_{pd+}	5,6	–	–	–	1.8	–	–	–	μs

TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:

Characteristics	I_{OL1}	I_{OL2}	I_{in}	I_D	$I_{C(max)}$	V_{IH}	V_{IL}	V_F	V_R	V_{CC1}	V_{CC2}	V_{CCIL}	V_{CCIH}	V_{RH}	GND
Input Forward Current	–	–	–	–	–	–	–	6	–	–	–	8	–	7	2,3,4
Input Leakage Current	–	–	–	–	–	–	–	–	6	–	–	–	8	–	2,3,4,7
Input Breakdown Voltage	–	–	6	–	–	–	–	–	–	–	–	–	8	–	2,3,4,7
Input Clamp Voltage	–	–	–	6	–	–	–	–	–	–	–	8	–	–	2,3,4
Output Voltage (See Figure 1) V_{OL1}	5	–	–	–	–	6	–	–	–	–	–	–	–	7	2,3,4
V_{OL2}	–	5	–	–	–	4	–	–	–	–	–	–	–	7	2,3,4
BV_{CEX}	–	–	–	–	5	–	–	6	–	–	–	–	–	7	2,3,4
Output Leakage Current	–	–	–	–	–	–	6	–	–	–	5	–	–	7	2,3,4
Output Power Supply Drain Current (I_{PDL})	–	–	–	–	–	–	–	–	–	8	–	–	–	–	2,3,4,6, 7,9,10
Output Power Supply Drain Current (I_{PDH})	–	–	–	–	–	–	–	–	–	8	–	–	–	6,7,9, 10	2,3,4
Switching Parameters (See Figure 2)			Pulse In	Pulse Out											
Turn-On Delay Time	5	–	6	5	–	–	–	–	–	8	5	–	–	7	2,3,4
Turn-Off Delay Time	5	–	6	5	–	–	–	–	–	8	5	–	–	7	2,3,4

TEST CIRCUITS

FIGURE 1 – V_{OL} TEST CIRCUIT

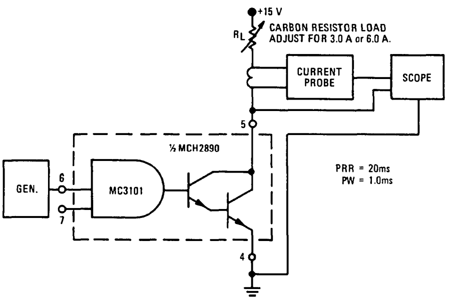
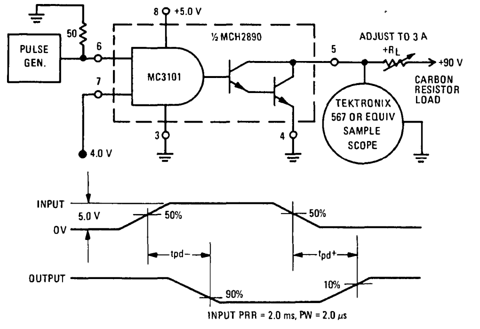


FIGURE 2 – PROPAGATION DELAY TIME TEST CIRCUIT



TYPICAL CHARACTERISTICS

FIGURE 3 – COLLECTOR-EMITTER VOLTAGE versus NEGATIVE EMITTER VOLTAGE

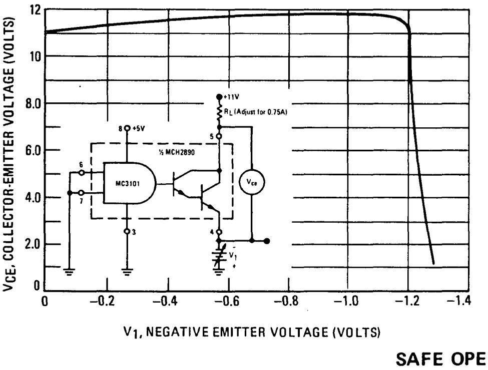
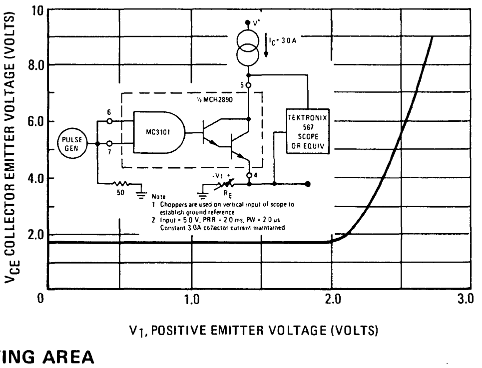


FIGURE 4 – COLLECTOR-EMITTER VOLTAGE versus POSITIVE EMITTER VOLTAGE



SAFE OPERATING AREA

FIGURE 5 – COLLECTOR-EMITTER VOLTAGE versus COLLECTOR CURRENT

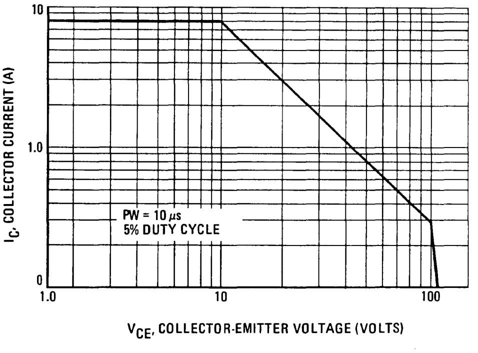
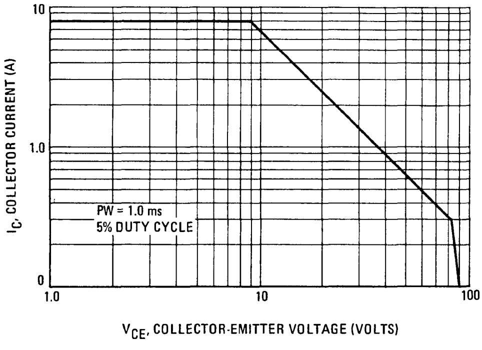
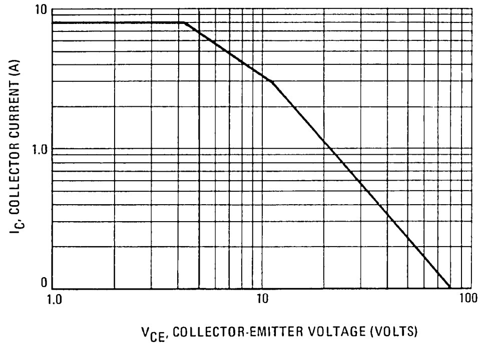


FIGURE 6 – COLLECTOR-EMITTER VOLTAGE versus COLLECTOR CURRENT



SAFE OPERATING AREA (Continued)

FIGURE 7 – COLLECTOR-EMITTER VOLTAGE versus COLLECTOR CURRENT



APPLICATIONS INFORMATION

The MCH2890 is designed for high-current and high-voltage applications such as hammer-drivers in high-speed printers, relay-drivers, lamp drivers, paper tape punches, stepping motors, and other high current inductive and resistive loads.

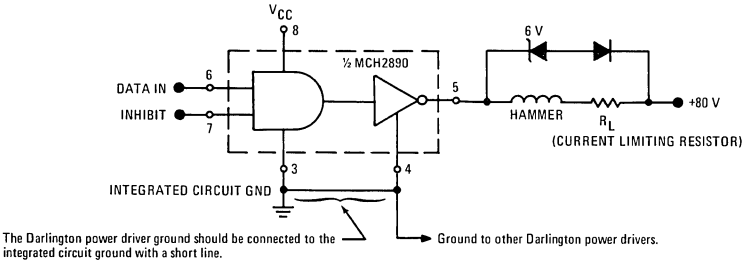
This dual hybrid driver, which consists of a monolithic MTTL "AND" gate and two power Darlington drivers, is capable of supplying up to 6.0 amperes at a maximum duty cycle of 10% with pulse widths up to 25 ms. In addition to the high-current drive capability the MCH2890 offers high collector-to-emitter breakdown (BV_{CEX} = 120 Volts min) which is desirable when driving inductive loads at high currents.

A typical high-speed hammer driver application is illustrated in Figure 8. The number of drivers per printer is large, and considerable electrical noise is generated when they are switched simultaneously. The ground line, which terminates all of the Darlington power drivers, may be several feet in length resulting in substantial inductance and series resistance. The effect of this inductance and resistance becomes appreciable at the high-current levels required of hammer drivers. When the Darlington power drivers are switched "off", even a small inductance at the Darlington ground generates a negative voltage spike which tends to turn the Darlington power driver "on" rather than "off". This negative excursion of the emitter can result in oscillations. The oscillation can be stopped by tieing the integrated circuit ground (pin 3) to the Darlington ground (pins 2 and 4) with as short a line as possible. (See Figure 8). This circuit configuration pulls the gate output lower when the negative spike is present on the power ground line which guarantees "turn off" of the Darlington power driver.

To insure that the Darlington power driver does not go into secondary breakdown and latch up, a diode clamp is employed as shown. For high-speed printers, the addition of a zener diode can aid in dissipating the stored inductive power (during "turn off") in the hammer solenoid.

Additional features of the MCH2890 include fast switching and low leakage for minimum standby power.

FIGURE 8 – TYPICAL HAMMER DRIVER APPLICATION



MFC4000B

AUDIO AMPLIFIER

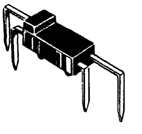
1/4-WATT AUDIO AMPLIFIER

. . . designed for the output stage of battery-powered portable radios.

- 250 mW of Audio Output Power
- Low Standby Current – 3.5 mA typical
- Low Harmonic Distortion
- Reduces Component Count in Portable Radios by Two Transformers and Two Transistors
- Eliminates Costly Component Matching Requirements

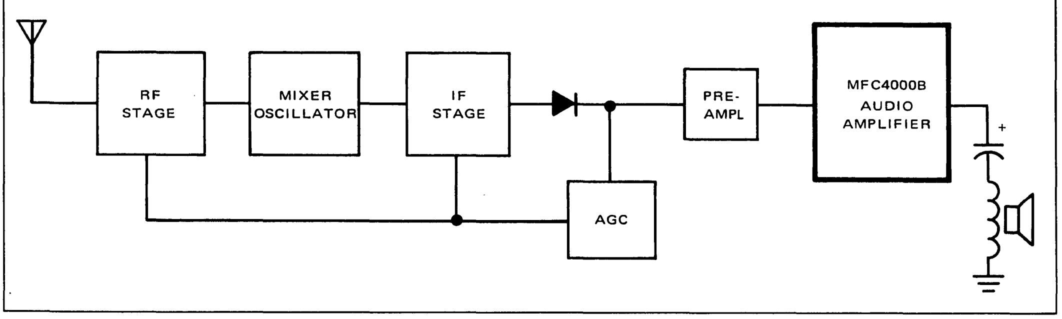
1/4-WATT AUDIO AMPLIFIER

SILICON MONOLITHIC FUNCTIONAL CIRCUIT



PLASTIC PACKAGE
CASE 206A

TYPICAL APPLICATION



MAXIMUM RATINGS ($T_A = 25^oC$ unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+	12	Vdc
Power Dissipation (Package Limitation) (Soldered on a circuit board and held in free air) Derate above $T_A = 25^oC$	P_D	1.0 10	Watt mW/^oC
Operating Temperature Range	T_A	-10 to +75	^oC

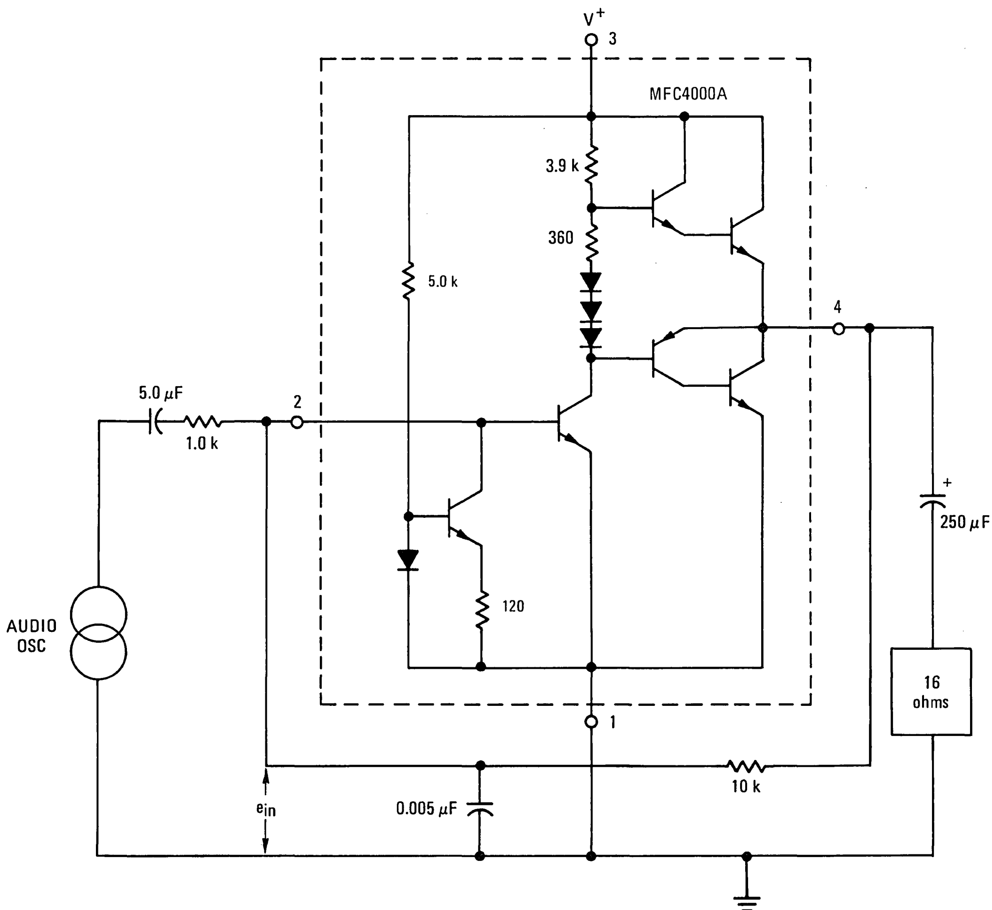
See Packaging Information Section for outline dimensions.

ELECTRICAL CHARACTERISTICS* (V^+ = 9.0 Vdc, R_L = 16 Ohms, T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Zero Signal Current Drain	I_D	–	3.5	6.0	mAdc
Sensitivity P_{out} = 50 mW(rms)	e_{in}	–	–	15	mV(rms)
Output Power Total Harmonic Distortion ≤ 10%	P_{out}	250	350	–	mW(rms)
Total Harmonic Distortion P_{out} = 50 mW(rms) P_{out} = 50 mW(rms), V^+ = 6.0 Vdc	THD	 – –	 0.7 4.5	 – –	%

*As measured in test circuit shown in Figure 1.

FIGURE 1 – TEST CIRCUIT



TOTAL HARMONIC DISTORTION versus OUTPUT POWER

FIGURE 2 – V^+ = 9.0 Vdc

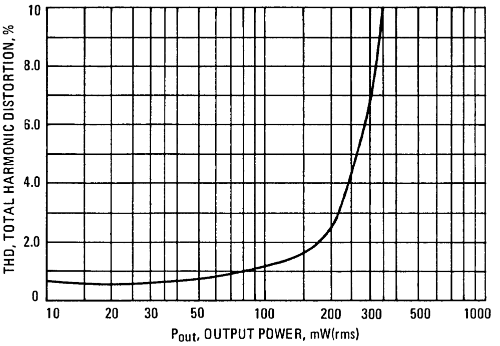


FIGURE 3 – V^+ = 6.0 Vdc

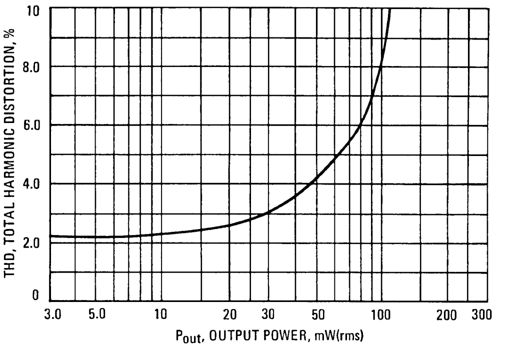


FIGURE 4 – CURRENT DRAIN versus OUTPUT POWER

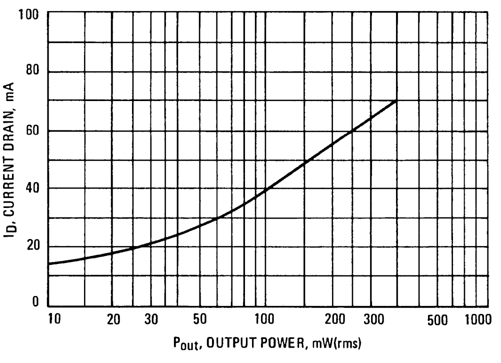


FIGURE 5 – TOTAL HARMONIC DISTORTION versus SUPPLY VOLTAGE

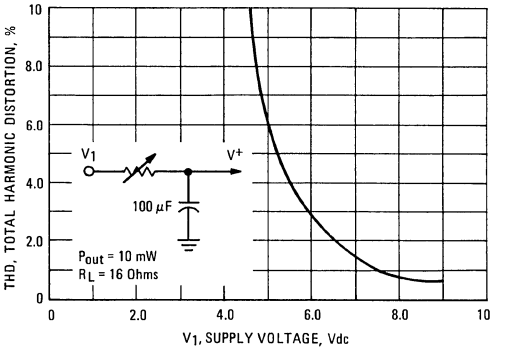
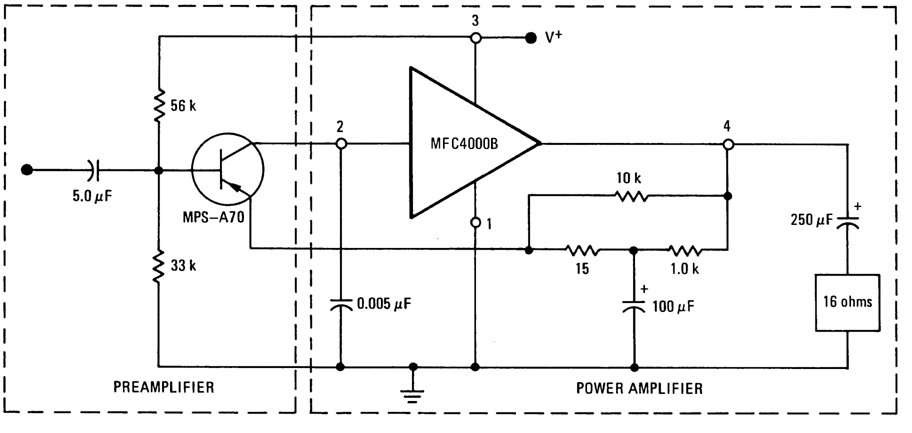


FIGURE 6 – TYPICAL CIRCUIT APPLICATION



MFC4010A

HIGH FREQUENCY CIRCUIT

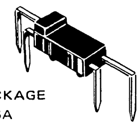
WIDE-BAND AMPLIFIER

. . . designed for FM/IF and low-level audio applications.

- High Audio Gain – 60 dB minimum
- Useful as a Microphone Amplifier and in Tape Recorders and Cassettes
- Excellent Performance as a 10.7 MHz FM/IF Amplifier
- High Transconductance (g_m) Ideally Suited to Low Impedance Ceramic Filters

WIDE-BAND AMPLIFIER

Silicon Monolithic Functional Circuit



PLASTIC PACKAGE
CASE 206A

TYPICAL APPLICATIONS

FIGURE 1 – FM/IF AMPLIFIER

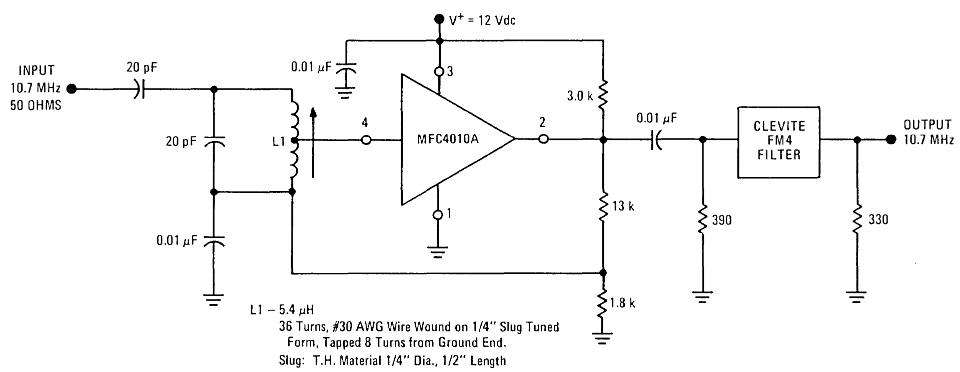
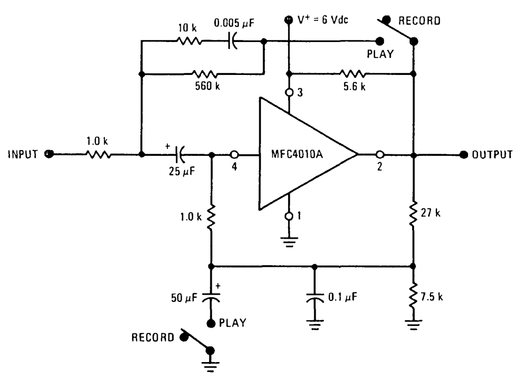


FIGURE 2 – RECORD/PLAY PREAMPLIFIER FOR CASSETTE AND PORTABLE TAPE RECORDERS



See Packaging Information Section for outline dimensions.

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+	18	Vdc
Power Dissipation @ T_A = 25°C (Package Limitation) Derate above 25°C	P_D	0.5 5.0	Watt mW/°C
Operating Temperature Range	T_A	-10 to +75	°C

ELECTRICAL CHARACTERISTICS (V^+ = 6.0 Vdc, T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Open Loop Voltage Gain (Figure 3) (f = 1.0 kHz)	A_{VOL}	60	68	–	dB
h Parameters (1) (f = 1.0 kHz)	h_{11}	–	1.0	–	k ohms
	h_{12}	–	10^{-6}	–	–
	h_{21}	–	1000	–	–
	h_{22}	–	10^{-5}	–	mhos
Output Noise Voltage (Figure 3) (BW = 20 Hz to 20 kHz, R_S = 1.0 k ohms)	$e_{n(out)}$	–	3.0	–	mV(rms)
Current Drain	I_D	–	3.0	–	mA

HIGH FREQUENCY CHARACTERISTICS (V^+ = 12 Vdc, f = 10.7 MHz, T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Power Gain (Figure 1) (e_{in} = 0.1 mVrms)	–	–	42	–	dB
Noise Figure (Figure 1) ($R_S \approx$ 740 Ohms)	NF	–	6.0	–	dB
y Parameters(1) (f = 10.7 MHz, I_2 = 2.0 mA)	y_{11}	–	1.3 + j1.5	–	mmhos
	y_{12}	–	-3.4 + j8.1	–	μmhos
	y_{21}	–	-0.33 + j0.68	–	mhos
	y_{22}	–	120 + j0	–	μmhos

(1)Device only, without external passive components.

FIGURE 3 — AUDIO TEST CIRCUIT

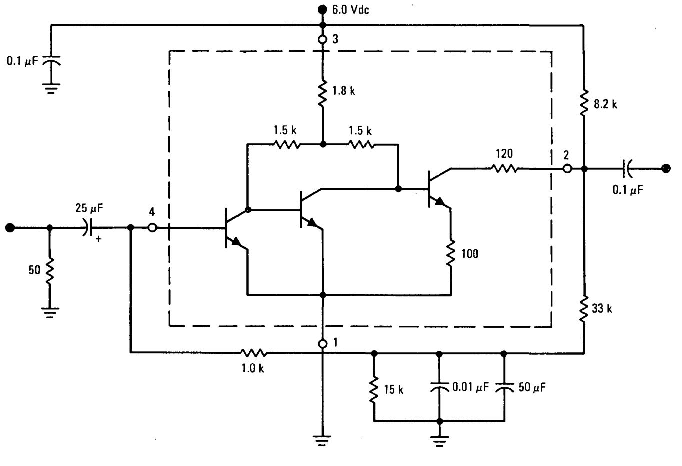
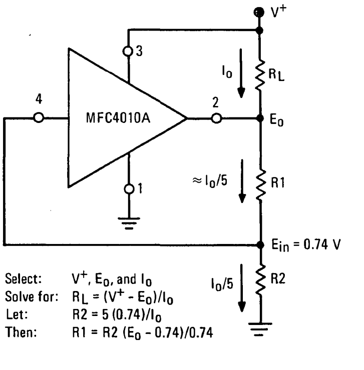


FIGURE 4 — BIASING RECOMMENDATIONS



AUDIO PERFORMANCE CHARACTERISTICS
(for Test Circuit Figure 3)

FIGURE 5 — VOLTAGE GAIN versus FREQUENCY

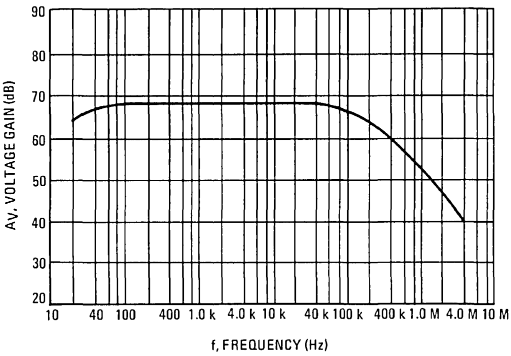
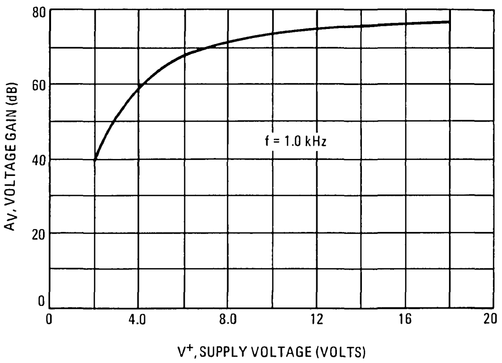


FIGURE 6 — VOLTAGE GAIN versus POWER SUPPLY



TAPE PREAMPLIFIER PERFORMANCE
(for Circuit Figure 2)

FIGURE 7 — RECORD VOLTAGE GAIN versus FREQUENCY

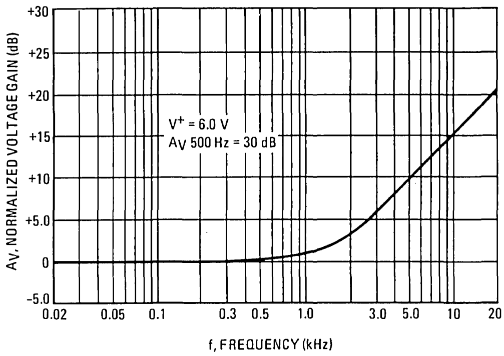
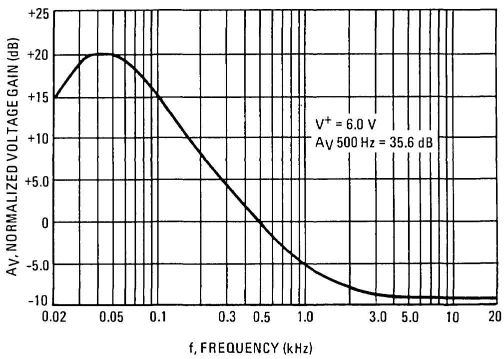


FIGURE 8 — PLAYBACK VOLTAGE GAIN versus FREQUENCY



Note:

The record/playback characteristics shown in Figures 8 and 9 were taken with the preamplifier driven by a 50 ohm source. The curves are typical of a desired response for the preamplifier; however, every type of tape recording and playback head is different and this circuit will not necessarily satisfy all requirements. No particular tape head was used as a basis for circuit design. The circuit is only an example showing the equalization network configuration.

The ideal preamplifier will have an input impedance approximately 10 times the highest impedance of the tape head and every preamplifier circuit must be designed using a test tape to verify the response of the design.

10.7 MHz y PARAMETERS

FIGURE 9 – INPUT ADMITTANCE

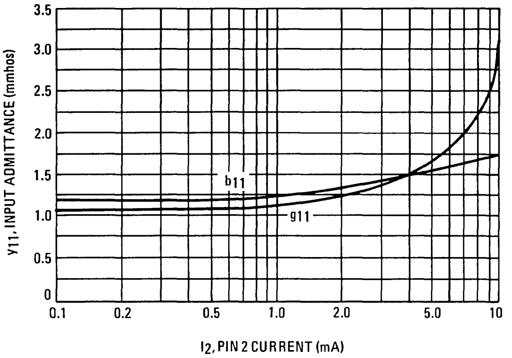


FIGURE 10 – REVERSE TRANSFER ADMITTANCE

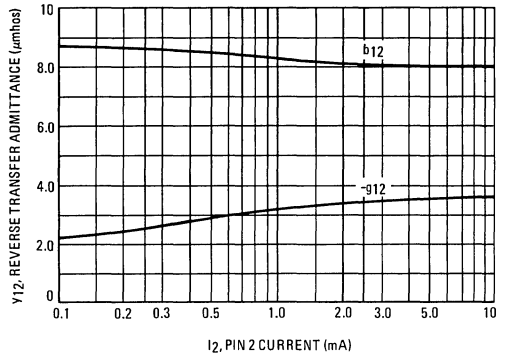


FIGURE 11 – FORWARD TRANSFER ADMITTANCE

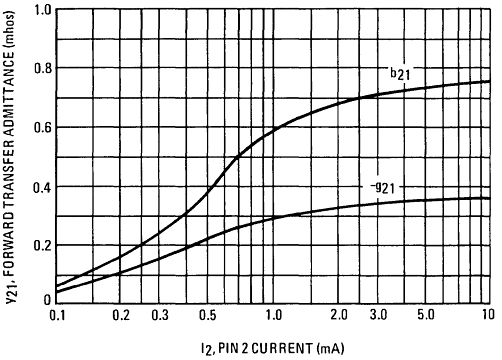
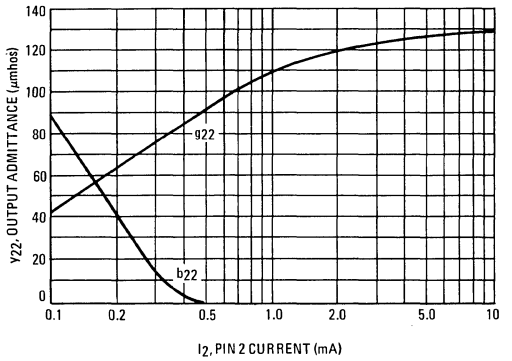


FIGURE 12 – OUTPUT ADMITTANCE



6

10.7 MHz PERFORMANCE
(Circuit of Figure 1)

FIGURE 13 – POWER GAIN versus SUPPLY VOLTAGE

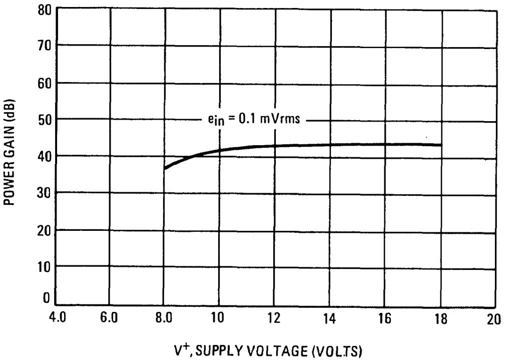
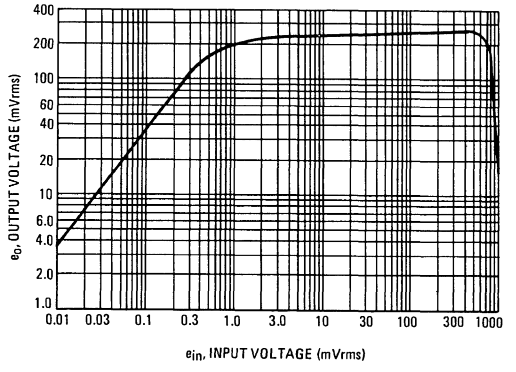


FIGURE 14 – VOLTAGE TRANSFER CHARACTERISTIC



MFC4050

AUDIO DRIVER

Advance Information

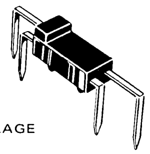
CLASS "A" AUDIO DRIVER

. . . designed for driving Class "A" PNP power output transistor stage applications.

- Drives to 4 Watts of Output Power
- Ideal for 12 Volt Automotive Equipment
- No Gain Selection of Power Transistors Necessary
- Economical 4-Lead Package

CLASS "A" AUDIO DRIVER

Silicon Monolithic Functional Circuit



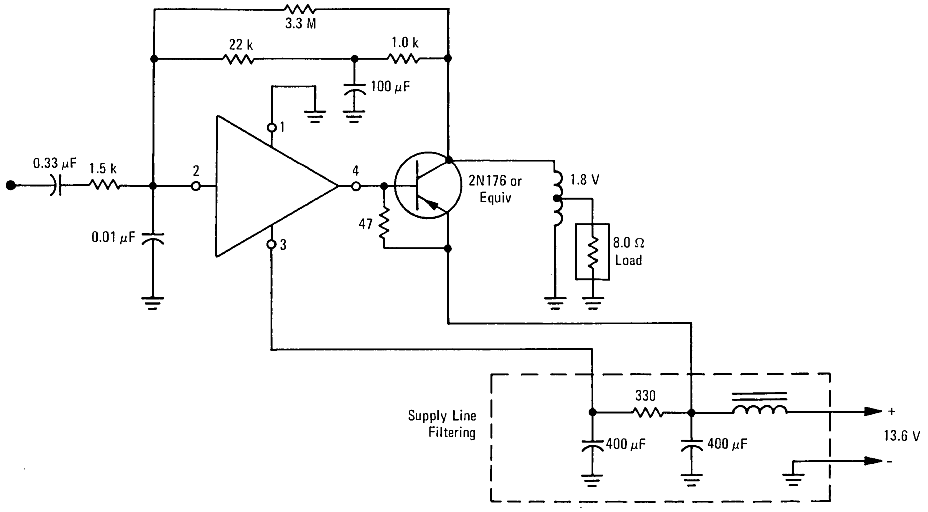
CASE 206A
PLASTIC PACKAGE

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+	18	Vdc
Power Dissipation @ T_A = 25°C (Package Dissipation)	P_D	1.0	Watt
Derate above 25°C	$1/\theta_{JA}$	10	mW/°C
Operating Temperature Range	T_A	-10 to +75	°C

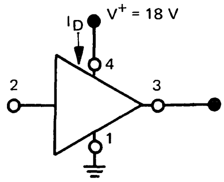
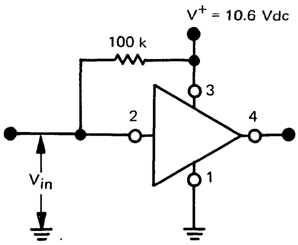
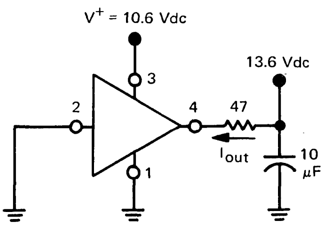
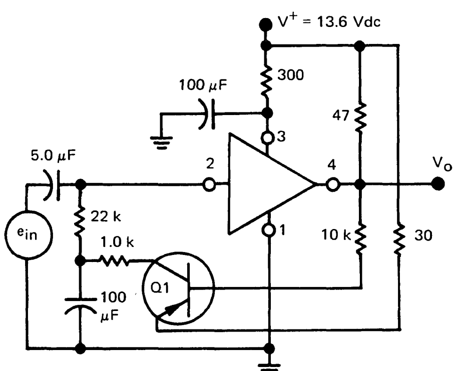
6

FIGURE 1 – TYPICAL 4-WATT AMPLIFIER CIRCUIT APPLICATION



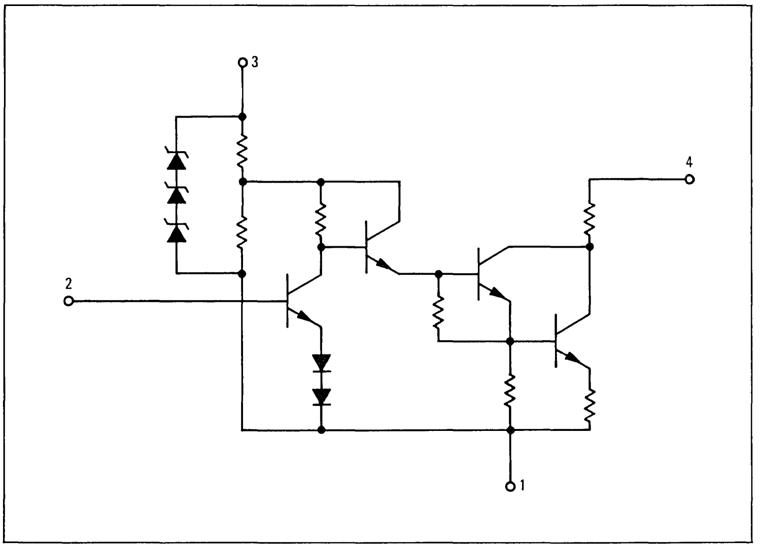
See Packaging Information Section for outline dimensions.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Circuit	Characteristic	Symbol	Min	Max	Unit
	Current Drain No Load	I_D	–	10	mA
	Input Voltage	V_{in}	1.9	2.5	Vdc
	Output Current (e_{in} = 1.0 mV(rms) @ 1.0 kHz)	I_{out}	30	–	mAdc
	Open Loop Voltage Gain (e_{in} = 1.0 mV(rms) @ 1.0 kHz) Q1: MPS6514 or equiv.	A_{VOL}	130	–	V/V

6

FIGURE 2 – CIRCUIT SCHEMATIC



MFC4060

POSITIVE VOLTAGE REGULATOR

Advance Information

VOLTAGE REGULATOR

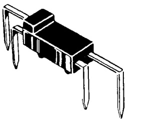
- Excellent Line and Load Regulation
- Economical Four Lead Package
- Industrial Quality Regulator

VOLTAGE REGULATOR

Silicon Monolithic Functional Circuit

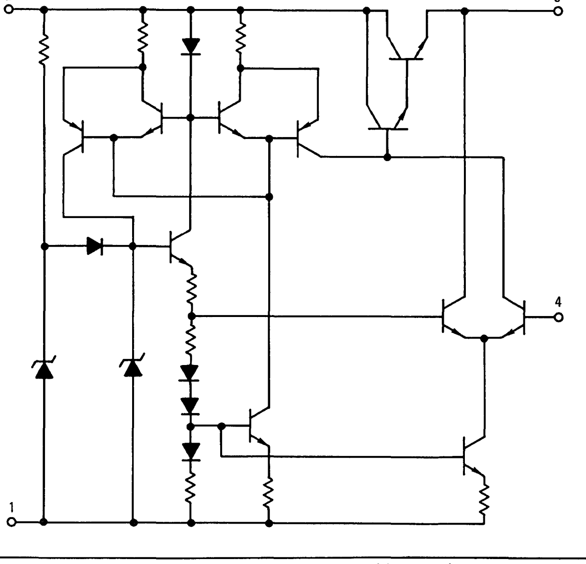
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage	V^+	38	Volts
Maximum Load Current	$I_{L\,(max)}$	200	mA
Power Dissipation Derate above $T_A = +25^oC$	P_D	1.0 10	Watt $mW/^oC$
Operating Temperature Range	T_A	-10 to +75	^oC



CASE 206A
PLASTIC PACKAGE

CIRCUIT SCHEMATIC

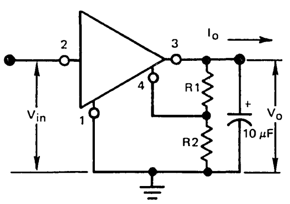
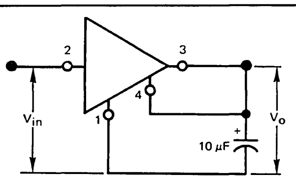


This is advance information on a new introduction and specifications are subject to change without notice.

See Packaging Information Section for outline dimensions.

MFC4060 (continued)

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted.)

Circuit	Characteristic	Symbol	Min	Typ	Max	Unit
	Load Regulation V_{in} = 30 Volts, Pin 2 V_o, Pin 3 ΔI_o = 50 to 100 mA $\frac{(V_{o1} - V_{o2})}{V_{o1}} \times 100 = \%V_o$	Reg_{load}	–	–	0.2	%
	Line Regulation V_{in1} = 12 Volts, Pin 2 V_{in2} = 30 Volts, Pin 2 V_o = 7.5 Volts, Pin 3 $\frac{\Delta V_o \times 100}{\Delta V_{in} \times V_o} = \%V_o/V_{in}$	Reg_{line}	–	–	0.03	%/V
	Temperature Coefficient V_{in} = 30 Volts, Pin 2 I_o = 10 mA V_o = 10 Volts, Pin 3 ΔT_A = 0°C to 50°C $\frac{V_{o1} - V_{o2}}{T_{A1} - T_{A2}} = TC$	TC	-3.0	–	+3.0	mV/°C
$\frac{V_o}{R1 + R2}$ = 2.0 mA min $\frac{V_o}{V_{ref}} = \frac{R1 + R2}{R1}$	Input Voltage Range	V_{in}	9.0	–	35	Vdc
	Input – Output Voltage Differential	$V_{in} - V_o$	3.0	–	–	Vdc
	Reference Voltage V_{in} = 10 Volts, Pin 2 V_{ref} Pin 3 Pin 4	V_{ref}	3.8	–	4.8	Vdc

MFC6010

FM IF AMPLIFIER

FM LIMITING IF AMPLIFIER

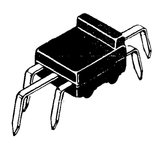
. . . a monolithic silicon integrated circuit designed especially for 10.7 MHz IF applications.

Highlights Include:

- High Stable Gain @ 10.7 MHz (40 dB typ)
- Low Feedback Capacitance ($|y_{12}|$ = 0.01 mmho typ)
- Non-Saturating Limiting (With Suitable Load)
- Compatible With CA3053 and μA703 (See Figures 7 and 8)

FM IF AMPLIFIER

Silicon Monolithic Functional Circuit



CASE 643A

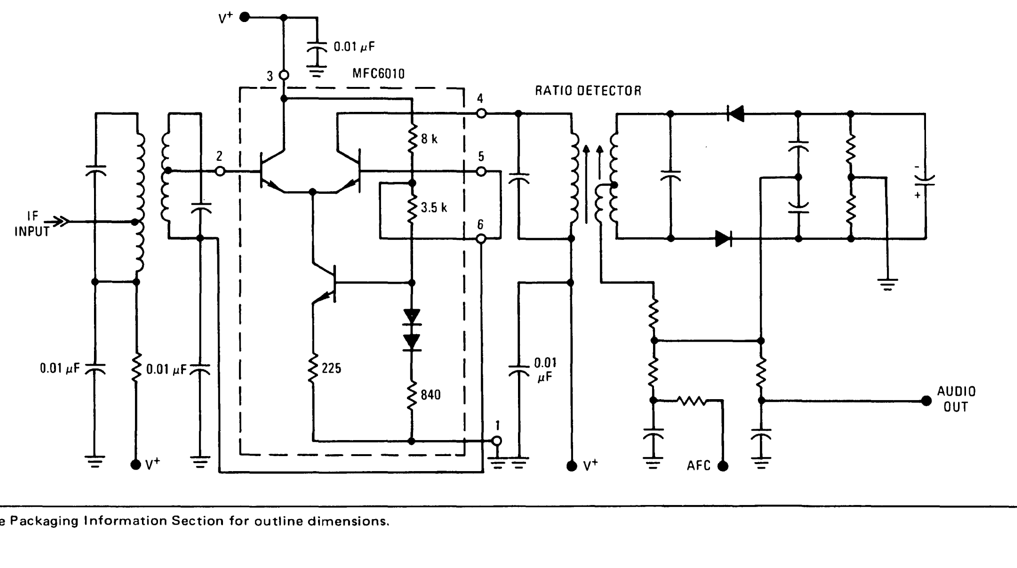
PLASTIC PACKAGE

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+	20	Vdc
Output Collector Voltage	V_4	20	Vdc
Input Voltage*	V_2, V_5	±5.0	Volts
Power Dissipation @ T_A = 25°C (Package Limitation)	P_D	1.0	Watt
Derate above 25°C	$1/\theta_{JA}$	10	mW/°C
Operating Temperature Range	T_A	-10 to +75	°C

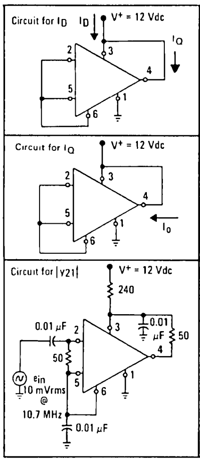
*Differential Voltage Swing.

FIGURE 1 — Typical Application (10.7 MHz Limiting Amplifier)



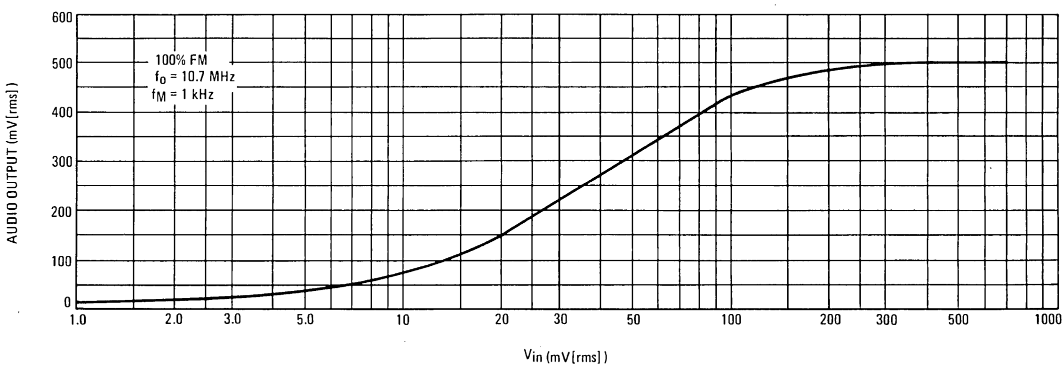
See Packaging Information Section for outline dimensions.

ELECTRICAL CHARACTERISTICS (V^+ = 12 Volts, f = 10.7 MHz, T_A = +25°C, unless otherwise noted.)



Characteristic	Symbol	Min	Typ	Max	Unit
Total Current Drain	I_D	–	–	10	mA
Output Quiescent Current	I_Q	1.75	3.2	5.0	mA
Output Saturation Voltage	V(sat)	–	3.5	–	Volts
Forward Transadmittance	$\lvert y_{21} \rvert$	25	–	–	mmhos
Reverse Transadmittance	$\lvert y_{12} \rvert$	–	0.01	–	mmho
Input Capacitance	C_{in}	–	6.0	–	pF
Input Conductance	G_{in}	–	0.4	–	mmho
Output Capacitance	C_{out}	–	2.5	–	pF
Output Conductance	G_{out}	–	35	–	μmhos
Noise Figure (R_S = 750 Ω)	N_F	–	7.0	–	dB
Maximum Stable Gain (Stern Factor = 3)	A_V	–	40	–	dB
Input Voltage (3.0 dB Limiting)	e_{in}	–	60	–	mV

FIGURE 2 – LIMITING CHARACTERISTICS



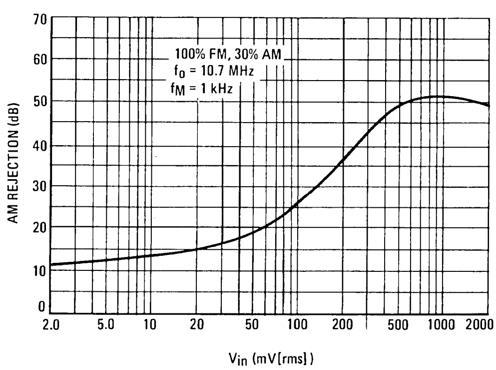
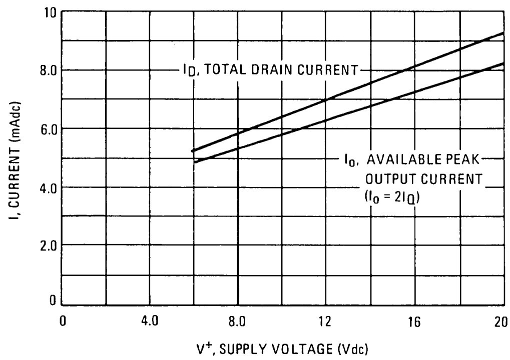


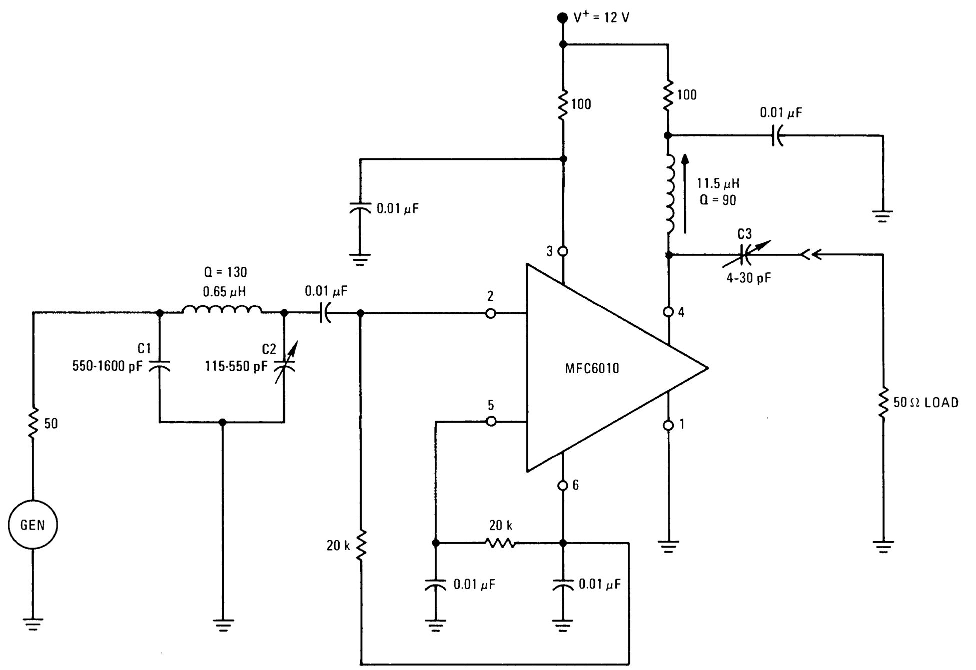
FIGURE 4 – CURRENT DRAIN AND OUTPUT CURRENT



6

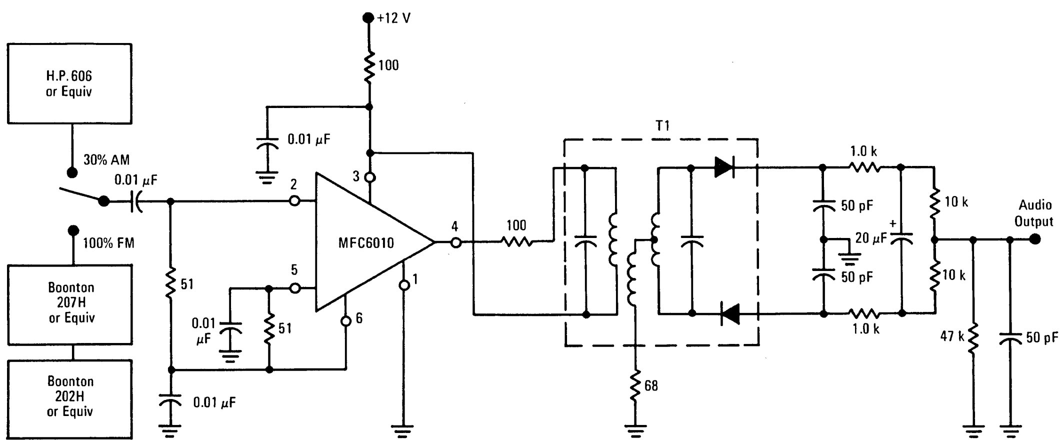
TEST CIRCUITS

FIGURE 5 — POWER-GAIN TEST CIRCUIT



Note: C1 (1000 pF nom), C2 (420 pF nom), C3 (20 pF nom) adjusted for maximum power gain.

FIGURE 6 — LIMITING AND AM REJECTION TEST CIRCUIT



T1 – Ratio Detector Primary Impedance ≈ 1.5 kΩ

APPLICATIONS INFORMATION

Because of the low reverse transfer admittance of the MFC6010, stability will be dependent mainly upon circuit layout. With careful design, very high gain (in the order of 40 dB) may be achieved at 10.7 MHz. The bias and supply currents may be varied from their normal values (shown in Figure 4) by shunting additional resistance from pin 6 to ground or to the supply line.

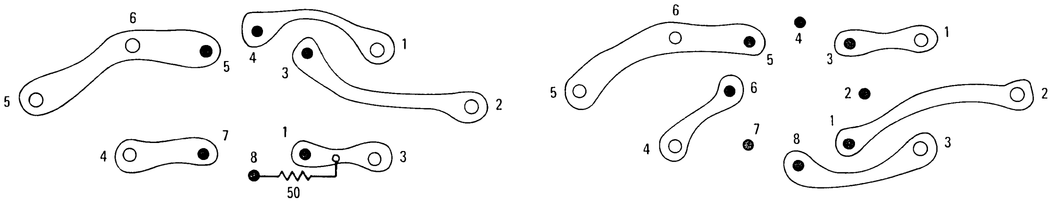
Although less gain may be realized when using the MFC6010 as a limiter, it is recommended that it be operated in a non-saturated mode. This mode of operation results in a high output impedance at limiting. Therefore the operation of the demodulator circuit is not subject to variable loading of the limiter output.

In order to avoid driving the amplifier transistor components of the MFC6010 into saturation, the load resistance must be chosen to ensure that current limiting occurs before the collector voltage drops to a value low enough to forward bias the collector-base junction. In a transformer coupled circuit, the maximum allowable load can be derived from

$$R_L = \frac{2\,(V^+ - V_5)}{I_o}$$

where values for I_o may be determined from Figure 4 (providing the bias currents have not been altered from their normal values).

In order to avoid degradation of AM rejection, the input signal should not exceed one volt (rms).



○ Motorola terminal and pin number position ● μA703 or CA3053 terminal and pin number position

*Foil patterns shown are intended to show pin-for-pin interconnection. Any change in the number of components is dictated by the requirements of the individual design.

MFC6030

POSITIVE VOLTAGE REGULATOR

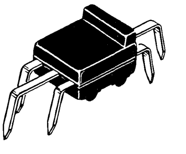
Advance Information

VOLTAGE REGULATOR

- Excellent Line and Load Regulation
- Current-Limit Feature Available
- Economical Six Lead Package
- Industrial Quality

VOLTAGE REGULATOR

Silicon Monolithic Functional Circuit

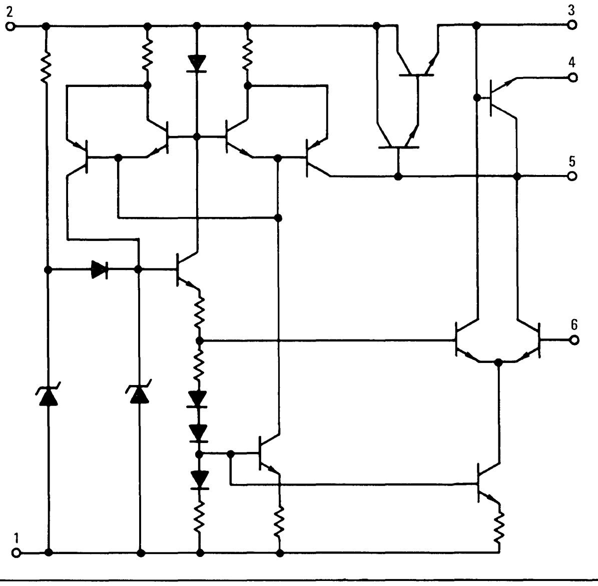


CASE 643A
PLASTIC PACKAGE

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage	V^+	38	Volts
Maximum Load Current	$I_{L(max)}$	200	mA
Power Dissipation Derate above $T_A = +25^oC$	P_D	1.0 10	Watt $mW/^oC$
Operating Temperature Range	T_A	-10 to +75	^oC

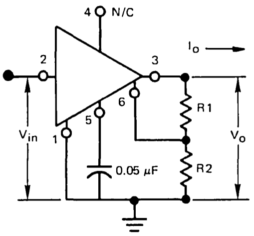
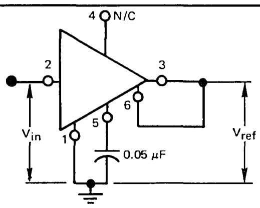
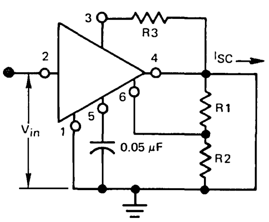
CIRCUIT SCHEMATIC



See Packaging Information Section for outline dimensions.

MFC6030 (continued)

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted)

Circuit	Characteristic	Symbol	Min	Typ	Max	Unit
	Load Regulation V_{in} = 30 Volts, Pin 2 V_o, Pin 3 ΔI_o = 50 to 100 mA $\frac{(V_{o1} - V_{o2})}{V_{o1}} \times 100 = \%V_o$	Reg_{load}	–	–	0.2	%
	Line Regulation V_{in1} = 12 Volts, Pin 2 V_{in2} = 30 Volts, Pin 2 V_o = 7.5 Volts, Pin 3 $\frac{\Delta V_o \times 100}{\Delta V_{in} \times V_o} = \%V_o/\Delta V_{in}$	Reg_{line}	–	–	0.03	%/Volt
$\frac{V_o}{R1 + R2}$ = 2.0 mA min $\frac{V_o}{V_{ref}} = \frac{R1 + R2}{R2}$	Temperature Coefficient V_{in} = 30 Volts, Pin 2 I_o = 10 mA V_o = 10 Volts, Pin 3 ΔT_A = 0°C to 50°C $\frac{V_{o1} - V_{o2}}{T_{A1} - T_{A2}} = TC$	TC	-3.0	–	+3.0	mV/°C
	Input Voltage Range	V_{in}	9.0	–	35	Vdc
	Input-Output Voltage Differential	$V_{in} - V_o$	3.0	–	–	Vdc
	Reference Voltage V_{in} = 10 Volts, Pin 2 V_{ref} Pin 6 Pin 1	V_{ref}	3.8	–	4.8	Vdc
	Short-Circuit Current $I_{SC} = \frac{0.7}{R3}$	I_{SC}	–	±5.0	–	%/I_{SC}
	R3 Usable Range	R3	3.5	–	6.8 k	ohms

ELECTRONIC ATTENUATOR

MFC6040

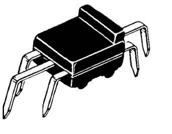
Advance Information

ELECTRONIC ATTENUATOR

- Designed for use in:
  - DC Operated Volume Control
  - Compression and Expansion Amplifier Applications
- Controlled by DC Voltage or External Variable Resistor
- Economical 6-Lead Plastic Package

ELECTRONIC ATTENUATOR

Silicon Monolithic Functional Circuit



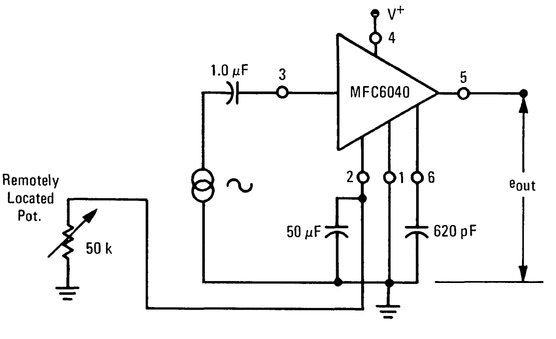
CASE 643A

PLASTIC PACKAGE

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+	21	Vdc
Power Dissipation @ T_A = 25°C (Package Limitation)	P_D	1.0	Watt
Derate above T_A = 25°C	$1/\theta_{JA}$	10	mW/°C
Operating Temperature Range	T_A	-10 to +75	°C

FIGURE 1 — TYPICAL DC "REMOTE" VOLUME CONTROL



See Packaging Information Section for outline dimensions.

ELECTRICAL CHARACTERISTICS (e_{in} = 100 mV, f = 1.0 kHz, R1 = 0, V^+ = 16 Vdc, T_A = 25°C unless otherwise noted)

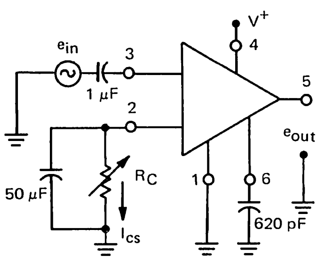
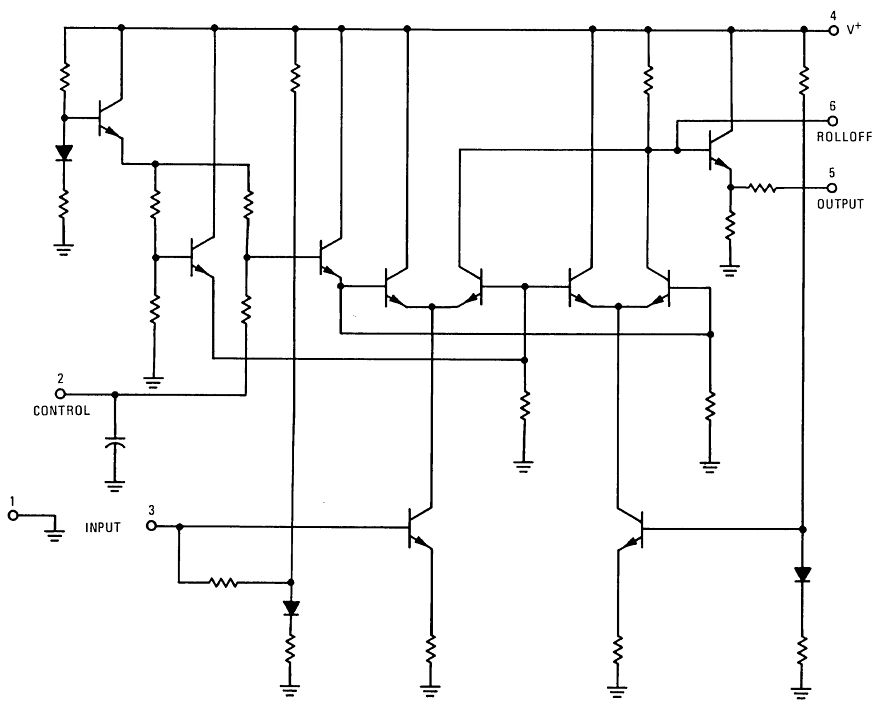
Circuit	Characteristic	Symbol	Min	Typ	Max	Unit
	Operating Power Supply Voltage	V^+	9.0	–	18	Vdc
	Control Terminal Sink Current (e_{in} = 0)	I_{cs}	–	–	2.0	mAdc
	Maximum Input Voltage	e_{in}	–	–	0.5	V(rms)
	Voltage Gain	A_V	11	13	–	dB
	Attenuation Range (R_C = 33 k ohms)		70	90	–	dB
	Total Harmonic Distortion (e_{in} = 100 mV, e_o = 100 mV)	THD	–	0.6	1.0	%

FIGURE 2 – CIRCUIT SCHEMATIC



TYPICAL ELECTRICAL CHARACTERISTICS

(V^+ = 16 Vdc, T_A = 25°C unless otherwise noted)

FIGURE 3 — ATTENUATION versus DC CONTROL VOLTAGE

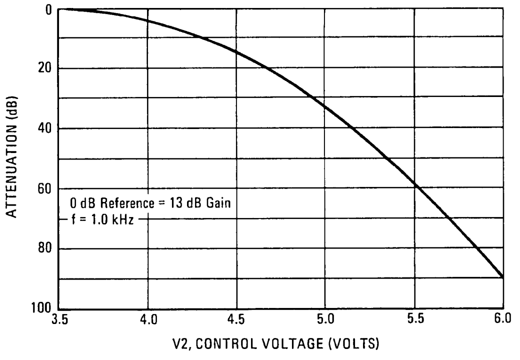


FIGURE 4 — ATTENUATION versus CONTROL RESISTOR

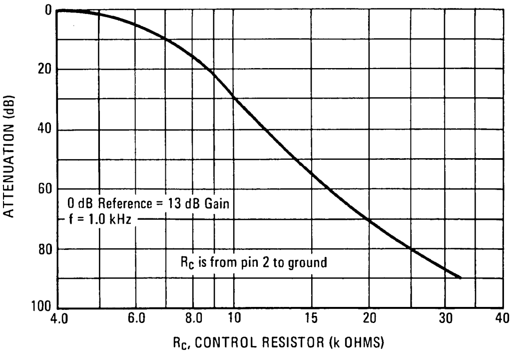


FIGURE 5 — FREQUENCY RESPONSE

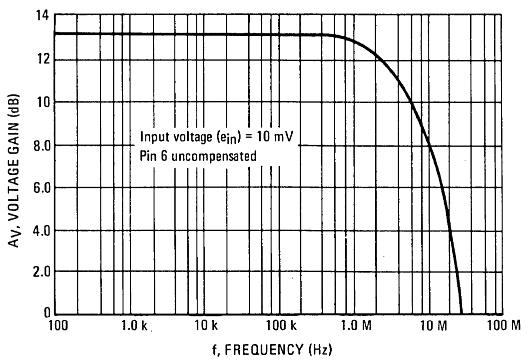


FIGURE 6 — OUTPUT VOLTAGE SWING

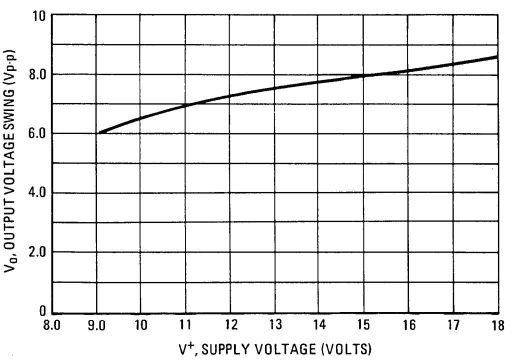
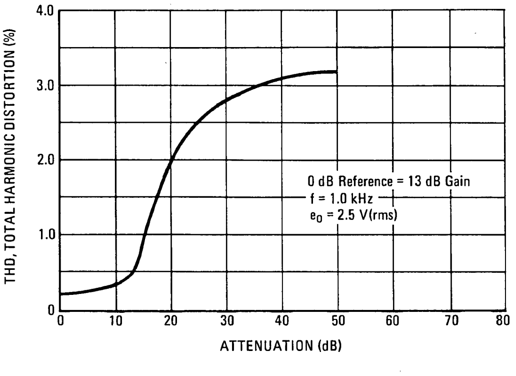


FIGURE 7 — TOTAL HARMONIC DISTORTION



MFC6070

AUDIO POWER AMPLIFIER

Advance Information

1-WATT AUDIO POWER AMPLIFIER

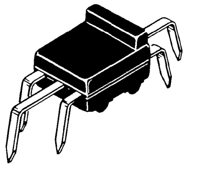
. . . designed primarily for low-cost audio amplifiers in phonograph, TV and radio applications.

- 100 mV Sensitivity for 1-Watt*
- Low Distortion – 1% @ 1-Watt typ*
- Short-Circuit Proof – Short Term (10 seconds typ)
- No Heatsink Required for 1-Watt Output at T_A = 55°C**
- Excellent Hum Rejection

*Circuit Dependent
**Voltage Dependent

1-WATT AUDIO POWER AMPLIFIER

Silicon Monolithic Functional Circuit



CASE 643A
PLASTIC PACKAGE

6

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+	20	Vdc
Power Dissipation Derate above T_A = +25°C	P_D $1/\theta_{JA}$	1.0 8.0	Watt mW/°C
Operating Temperature Range	T_A	-10 to +55	°C
Storage Temperature Range	T_{stg}	-40 to +150	°C

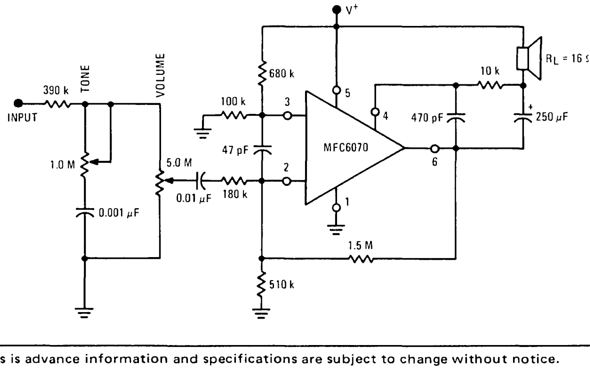
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	θ_{JA}*	125	°C/W

*Thermal resistance is measured in still air with fine wires connected to the leads, representing the "worst case" situation.

For a larger power requirement, pin 1 must be soldered to at least one sq. in. of copper foil on the printed circuit board. The θ_{JA} will be no greater than +90°C/W. Thus, 1.39 Watts could be dissipated at +25°C, which must be linearly derated at 11.1 mW/°C from +25°C to +150°C.

FIGURE 1 – TYPICAL 1-WATT PHONOGRAPH AMPLIFIER
(Ceramic cartridge input)

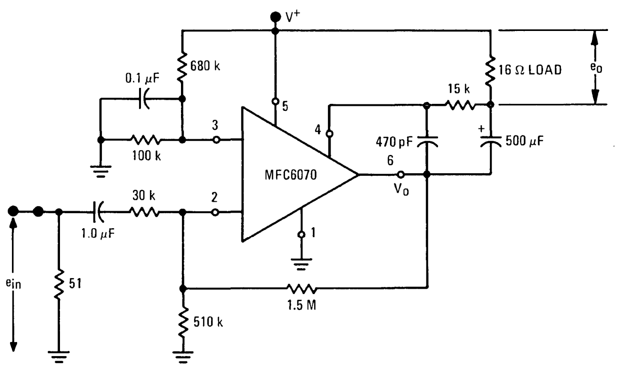


This is advance information and specifications are subject to change without notice.
See Packaging Information Section for outline dimensions.

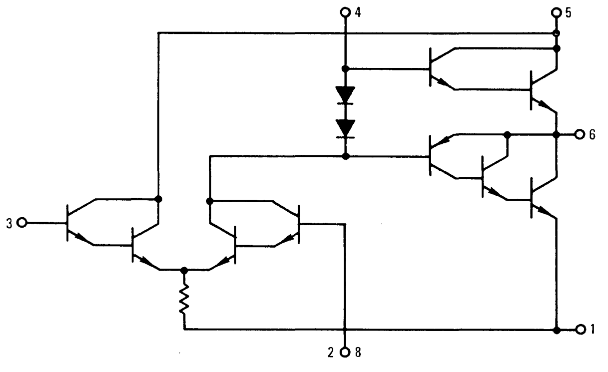
ELECTRICAL CHARACTERISTICS (V^+ = 16 Vdc, See Figure 2 for test circuit, T_A = +25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Quiescent Output Voltage	V_o	–	8.0	–	Vdc
Quiescent Drain Current (e_{in} = 0)	I_D	–	5.0	18	mA
Sensitivity, Input Voltage (e_{in} adjusted for e_o = 4.0 V(rms) @ 1.0 kHz, Power Output = 1.0 Watt)	e_{in}	–	100	150	mV
Total Harmonic Distortion	THD				%
(e_o = 4.0 V(rms) @ 1.0 kHz, Power Output = 1.0 Watt)		–	1.0	10	
(e_{in} adjusted for e_o = 1.26 V(rms) @ 1.0 kHz, Power Output = 100 mW)		–	1.0	3.0	
Hum and Noise (IHF Standard A201, 1966)	–	–	-40	–	dB

FIGURE 2 – 1-WATT AUDIO POWER AMPLIFIER TEST CIRCUIT



Circuit Schematic



TYPICAL CHARACTERISTICS

(V^+ = 16 Vdc, T_A = +25°C unless otherwise noted)

FIGURE 3 – TOTAL HARMONIC DISTORTION versus OUTPUT POWER

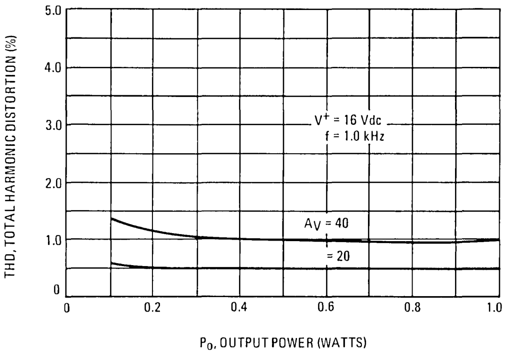


FIGURE 4 – POWER DISSIPATION versus OUTPUT POWER

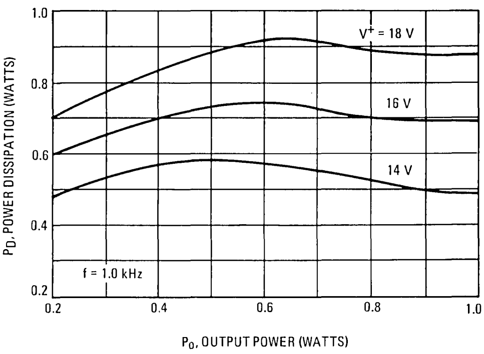
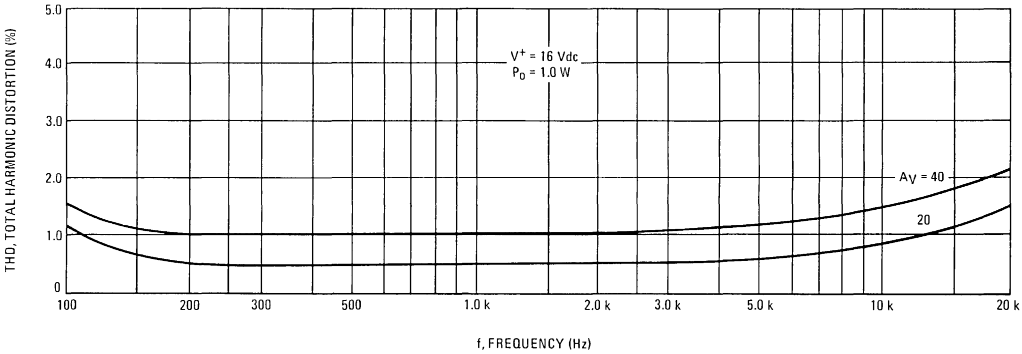


FIGURE 5 – TOTAL HARMONIC DISTORTION versus FREQUENCY



APPLICATIONS INFORMATION

Shown in Figures 7 and 11 are low cost 1 W phono amplifiers with a sensitivity (@ 1 kHz) of approximately 450 mV. The input impedance of both amplifiers is approximately equal to R4 and the gain is determined by (R7 + R10)/R5. To change the gain of the amplifier, change the value of R5 and hold (R7 + R10) between 1 M and 2.2 M. This allows the use of a small and less expensive capacitor for C2.

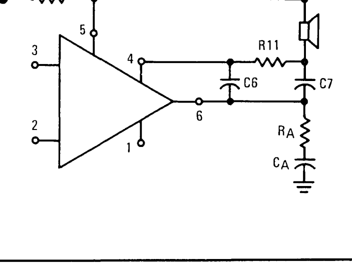
The bass boost effect shown in the frequency response curves (Figures 10 and 14) is provided by the parallel combination of C4 and R10 and can be eliminated by removing C4 and replacing (R7 + R10) with a 2.2 Megohm resistor. High frequency compensation is provided by C6 and the low frequency roll-off is determined by the impedance network of C2 and R5, C3 and R4, and C8 and the speaker. The series combination of R_A and C_A from pin 6 to ground may be required for stability, depending on printed circuit board layout, speaker reactance, and lead lengths.

Device ac short-circuit capability was tested in both the 8-ohm and 16-ohm amplifiers by shorting pin 6 thru a 500 microfarad capacitor to ground for a period of ten seconds with the amplifier operating at full rated output.

The speaker can be connected to V^+ (alternate connection shown below) or ground (Figures 7 and 11). Printed circuit board art work (1:1 pattern) is shown for both systems in Figures 16 and 18. A picture of the completed board for the grounded speaker system is shown in Figure 21.

ALTERNATE CONNECTION FOR SPEAKER TO V^+

(See Figure 20 for Parts List)



APPLICATIONS INFORMATION (continued)

(R_L = 8.0 ohms, T_A = +25°C unless otherwise noted)

FIGURE 6 – POWER SUPPLY

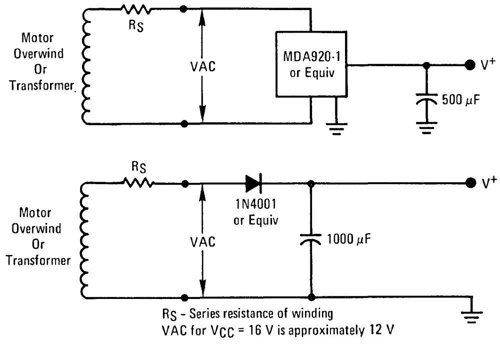


FIGURE 7 – PHONOGRAPH AMPLIFIER 1 WATT - 8 OHM
(See Figure 15 for Parts List)

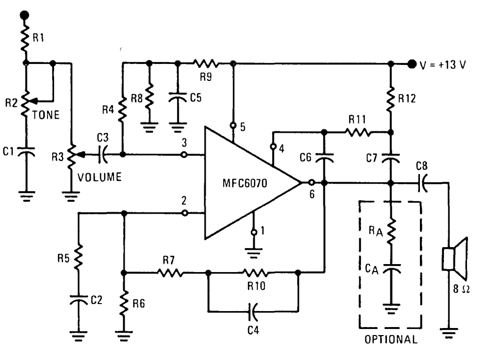


FIGURE 8 – TOTAL HARMONIC DISTORTION versus OUTPUT POWER FOR FIGURE 7

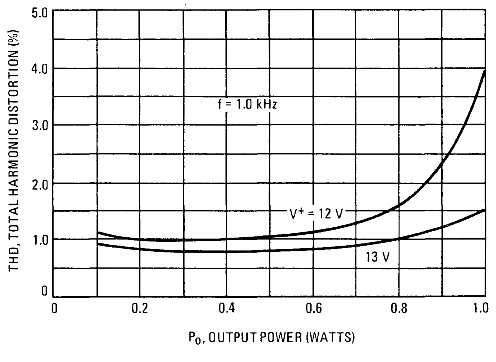


FIGURE 9 – TOTAL HARMONIC DISTORTION versus FREQUENCY FOR FIGURE 7

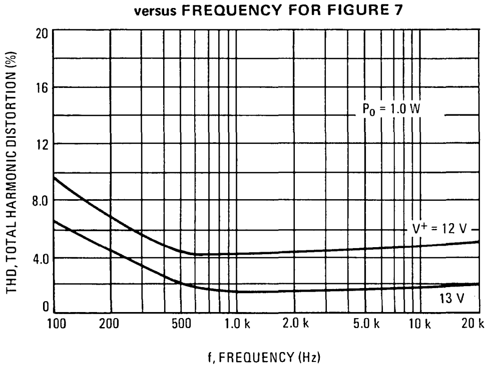
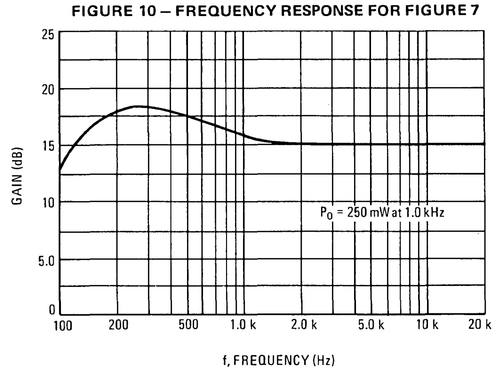


FIGURE 10 – FREQUENCY RESPONSE FOR FIGURE 7



APPLICATIONS INFORMATION (continued)

(R_L = 16 ohms, T_A = +25°C unless otherwise noted)

FIGURE 11 – 1.0 WATT, 16 OHM LOAD PHONOGRAPH AMPLIFIER
(See Figure 15 for Parts List)

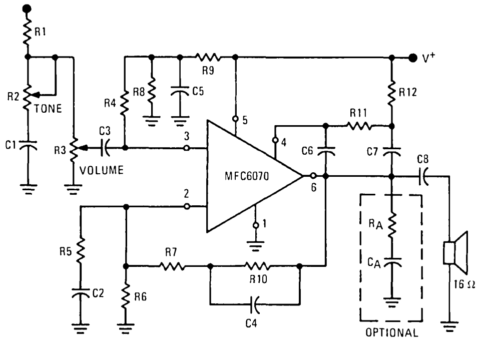


FIGURE 12 – TOTAL HARMONIC DISTORTION versus OUTPUT POWER FOR FIGURE 11

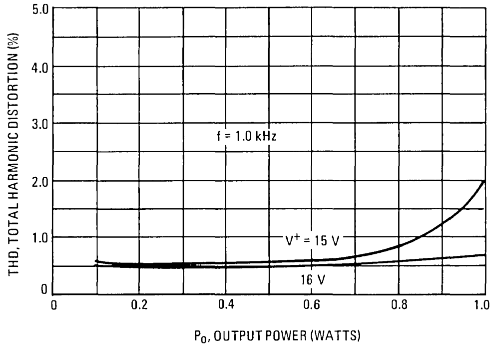


FIGURE 13 – TOTAL HARMONIC DISTORTION versus FREQUENCY FOR FIGURE 11

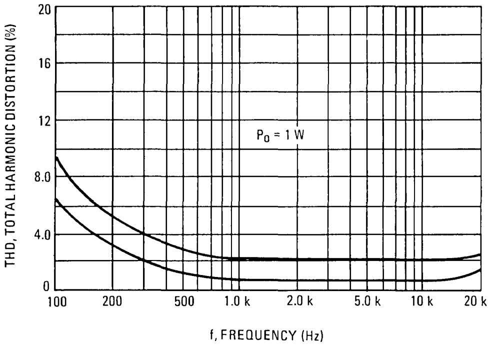


FIGURE 14 – FREQUENCY RESPONSE FOR FIGURE 11

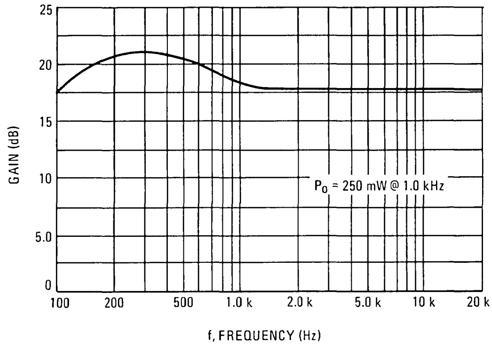


FIGURE 15 – PARTS LIST FOR FIGURES 7 AND 11

R1 = 180 k ohms	R9 = 1.0 Megohm	C3 = 0.05 μF
R2 = 5.0 Megohms	R10 = 1.5 Megohms	C4 = 470 pF
R3 = 5.0 Megohms	R11 = 6.8 kilohms	C5 = 0.1 μF
R4 = 1.0 Megohm	R12 = 6.8 kilohms	C6 = 470 pF
R5 = 150 k ohms*	R_A = 10 ohms**	C7 = 0.1 μF
R6 = 910 k ohms*	C1 = 470 pF	C8 = 500 μF*
R7 = 680 k ohms	C2 = 0.1 μF	C_A = 0.1 μF**
R8 = 180 k ohms		

*For Figure 11 (16-ohm load) change R5 to 100 k ohms, R6 to 820 k ohms and C8 to 250 μF.

**Optional – Not included on board. (See Applications Information Note)

APPLICATIONS INFORMATION (continued)

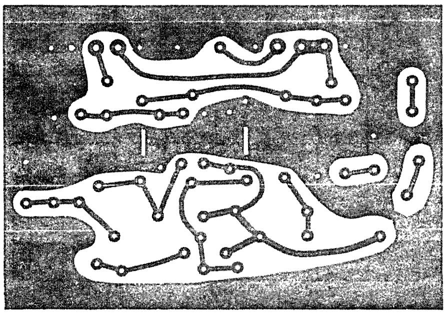


FIGURE 16 – PRINTED CIRCUIT BOARD (Foil Side)
1:1 PATTERN (Speaker Grounded)

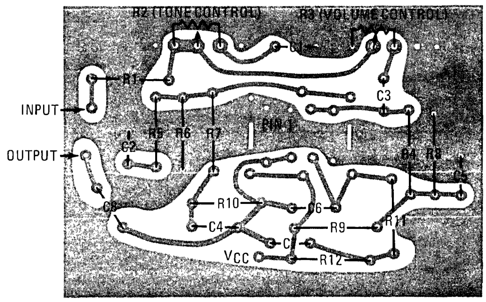


FIGURE 17 – COMPONENT DIAGRAM FOR FIGURE 16

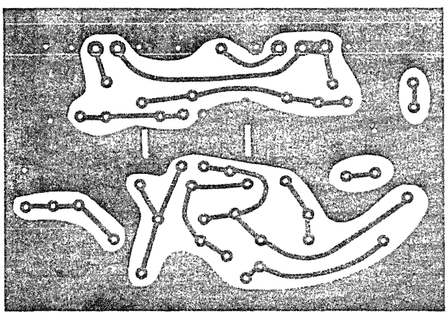


FIGURE 18 – PRINTED CIRCUIT BOARD (Foil Side)
1:1 PATTERN (Speaker to V^+)

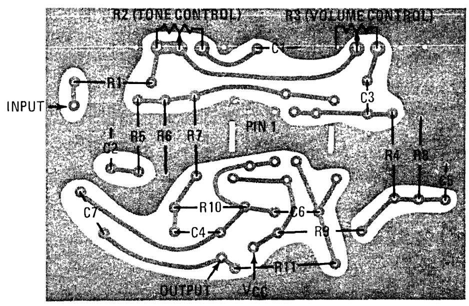
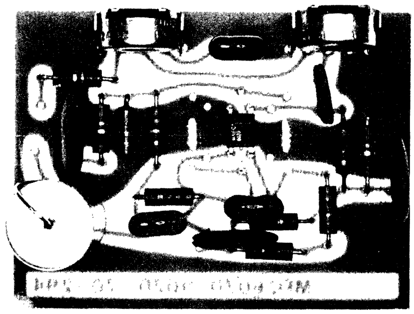


FIGURE 19 – COMPONENT DIAGRAM FOR FIGURE 18

FIGURE 20 – PARTS LIST FOR FIGURE 19
(See Applications Information Note)

R1 = 180 k ohms	C1,C4,C6 = 470 pF
R2,R3 = 5.0 Megohms	C2,C5 = 0.1 μF
R4,R9 = 1.0 Megohm	C3 = 0.05 μF
R5 = 82 k ohms	C7 = 250 μF
R6 = 820 k ohms	C_A = 0.1 μF*
R7 = 680 k ohms	*Optional - Not included on board. (See Applications Information Note)
R8 = 180 k ohms	
R10 = 1.5 Megohms	
R11 = 15 k ohms	
R_A = 10 ohms*	

FIGURE 21 – COMPLETED BOARD
(Speaker Grounded)



MFC8000
thru
MFC8002

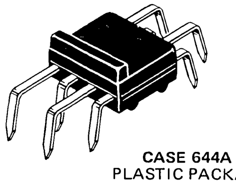
MONOLITHIC DUAL STEREO AMPLIFIER

. . . designed for the input stage of stereo power amplifiers.

- Excellent Channel Separation – 60 dB minimum
- High Gain – h_{FE} = 75 minimum
- Satisfies Both Channel Requirements with One Compact Package
- Selection of Breakdown Voltages to Meet the Particular Applications

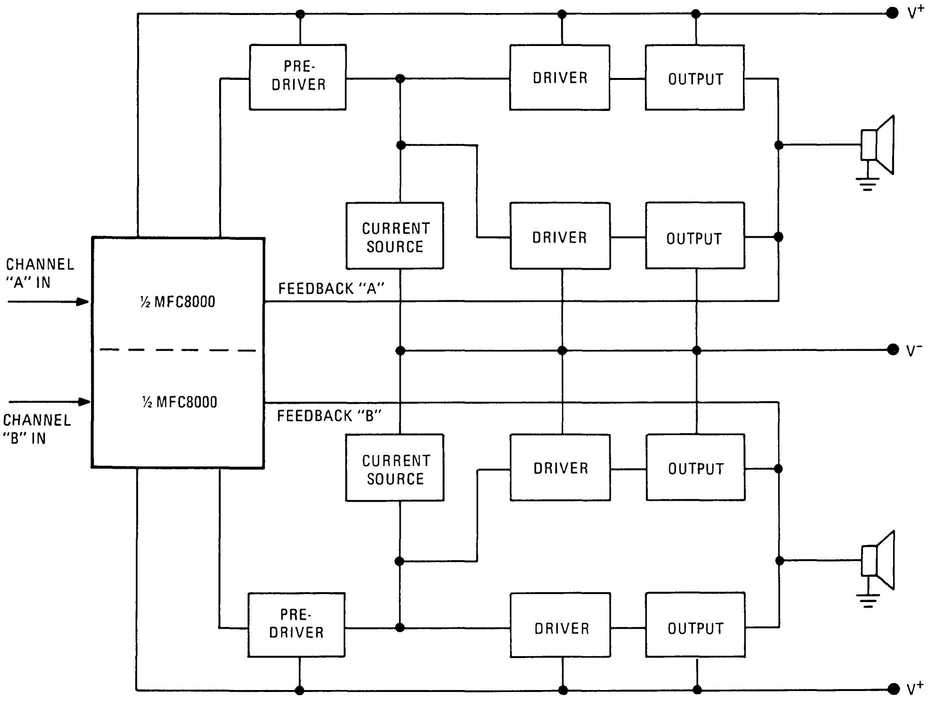
DUAL DIFFERENTIAL AMPLIFIER
(Stereo Input Amplifier)

SILICON MONOLITHIC CONSUMER CIRCUIT



CASE 644A
PLASTIC PACKAGE

TYPICAL APPLICATION



See Packaging Information Section for outline dimensions.

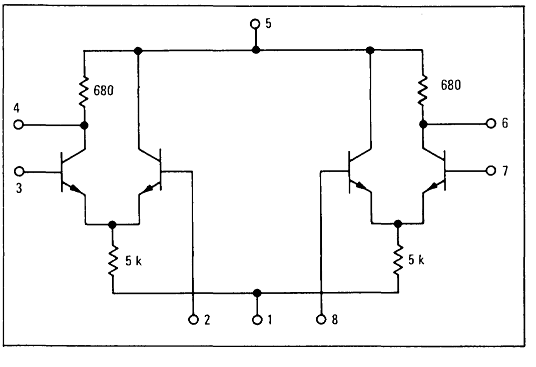
MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Maximum Supply Voltage – MFC8000 MFC8001 MFC8002	V^+	40 50 60	Vdc
Power Dissipation (Package Limitation) (Soldered on a circuit board) Derate above T_A = 25°C	P_D	1.0 10	Watt mW/°C
Operating Temperature Range	T_A	-10 to +75	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0) MFC8000 MFC8001 MFC8002	BV_{CEO}	 40 50 60	 – – –	 – – –	Vdc
DC Current Gain (V_{CE} = 20 Vdc, I_C = 1.0 mAdc)	h_{FE}	75	100	–	–
Base Differential Voltage (V_{CE} = 20 Vdc, I_C = 1.0 mAdc)	$\lvert\Delta V_{BE_3} - \Delta V_{BE_2}\rvert$ $\lvert\Delta V_{BE_8} - \Delta V_{BE_7}\rvert$	–	–	15	mVdc
Base Differential Current (V_{CE} = 20 Vdc, I_C = 1.0 mAdc)	$\lvert\Delta I_{B_3} - \Delta I_{B_2}\rvert$ $\lvert\Delta I_{B_8} - \Delta I_{B_7}\rvert$	–	–	1.0	μAdc
Channel Separation (Pins 2,3,8 grounded, signal at pin 7, $e_{out\,1}$ at pin 6, $e_{out\,2}$ at pin 4)	$\frac{e_{out\,1}}{e_{out\,2}}$	60	–	–	dB

CIRCUIT SCHEMATIC



MFC8010

AUDIO POWER AMPLIFIER

Advance Information

1-WATT AUDIO POWER AMPLIFIER

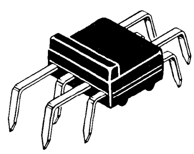
. . . designed to provide the complete audio system in television, radio and phonograph equipment.

- One Watt Continuous Sine Wave Power at +55°C
- High Gain – 10 mV (Max) for 1 Watt*
- Extremely Low Distortion – 1% @ 1 Watt (Typ)*
- Economical 8-Lead Plastic Package
- Short-Circuit Proof (Short Term)
- No Special Heat-Sinking Required

*Circuit Dependent.

1-WATT AUDIO POWER AMPLIFIER

Silicon Monolithic Functional Circuit

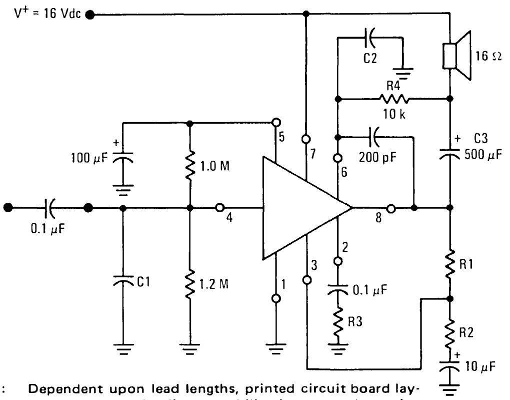


CASE 644A
PLASTIC PACKAGE

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

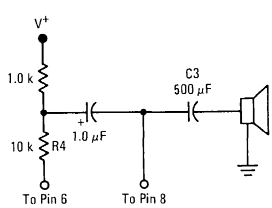
Rating	Symbol	Value	Unit
Power Supply Voltage	V^+	22	Vdc
Power Dissipation @ T_A = 25°C (Package Limitation)	P_D	1.2	Watt
Derate above T_A = 25°C	$1/\theta_{JA}$	10	mW/°C
Operating Temperature Range	T_A	-10 to +55	°C

FIGURE 1 – TYPICAL 1-WATT AUDIO POWER AMPLIFIER CIRCUIT



Sensitivity For 1 Watt mV	C1 pF	C2 pF	R1 k ohms	R2 ohms	R3 ohms
400	0	0	10	1.0 k	82
10	100	100	51	100	2.2 k

Alternate connection to permit connecting speaker to ground instead of to V^+:



NOTE: Dependent upon lead lengths, printed circuit board layout and output loading, a stabilization network consisting of a 0.1 µF capacitor in series with a 10 ohm resistor may be required from pin 8 to ground.

This is advance information and specifications are subject to change without notice.

See Packaging Information Section for outline dimensions.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

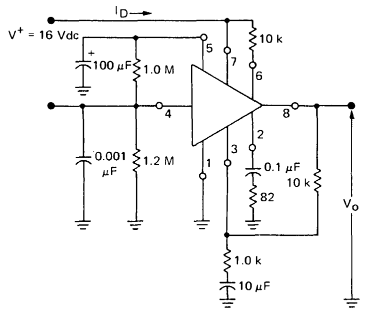
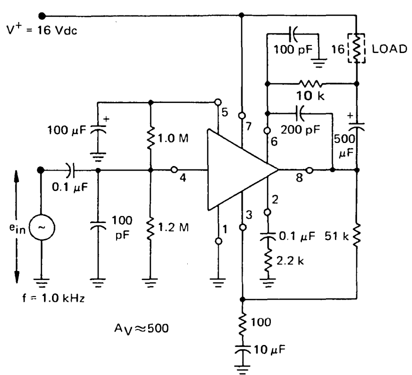
Circuit	Characteristic	Symbol	Min	Typ	Max	Unit
	Quiescent Output Voltage	V_o	7.0	8.0	9.0	Vdc
	Quiescent Drain Current	I_D	–	10	18	mAdc
	Sensitivity, Input Voltage (e_{in} adjusted for v_{out} = 4.0 V(rms) @ 1.0 kHz, Power Output = 1.0 Watt)	e_{in}	–	–	10	mV
	Total Harmonic Distortion (v_{out} = 4.0 Vrms @ 1.0 kHz, Power Output = 1.0 Watt)	THD	–	1.5	5.0	%
	(v_{in} adjusted for v_{out} = 2.8 V(rms) @ 1.0 kHz, Power Output = 500 mW)		–	1.0	1.5	
	Output Noise (e_{in} = 0)	$e_{n(out)}$	–	5.0	–	mV

FIGURE 2 – CIRCUIT SCHEMATIC

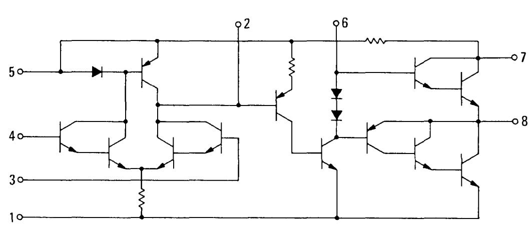


FIGURE 3 – DISTORTION

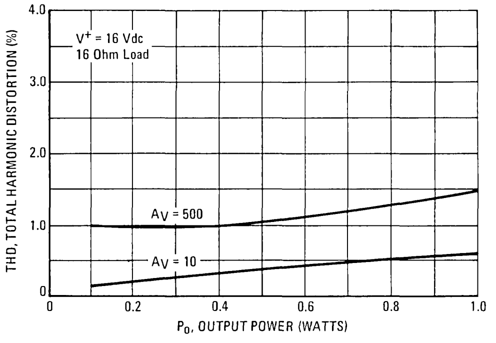


FIGURE 4 – DISTORTION

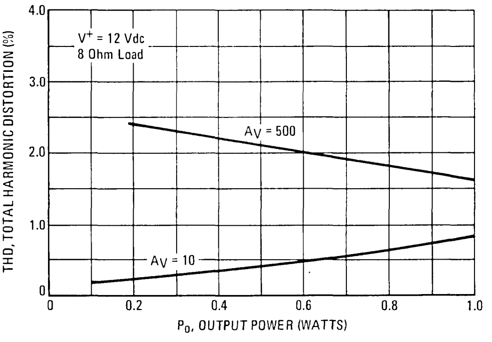


FIGURE 5 – EFFICIENCY

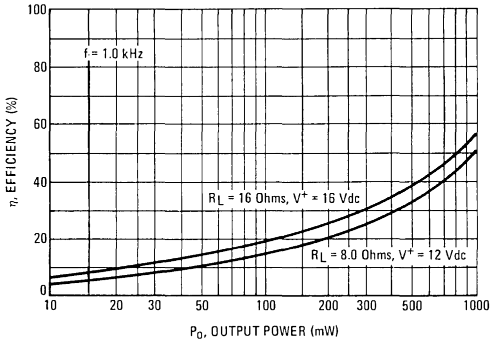
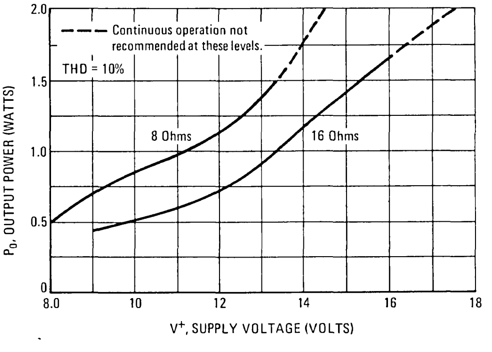


FIGURE 6 – POWER OUTPUT



6

MFC8020A

AUDIO DRIVER

Advance Information

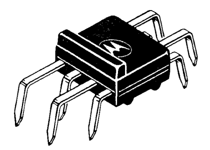
CLASS B AUDIO DRIVER

. . . designed as a preamplifier and driver circuit for complementary output transistors.

- Drives Up to 15-Watts Output (Four-Ohm Load)
- High Gain – 10 mV Input for Full Output
- High Input Impedance – 1 Meg Ohm Typ
- Output Biasing Diodes Included
- No Special h_{FE} Matching of Outputs Required

CLASS B AUDIO DRIVER

Silicon Monolithic
Functional Circuit

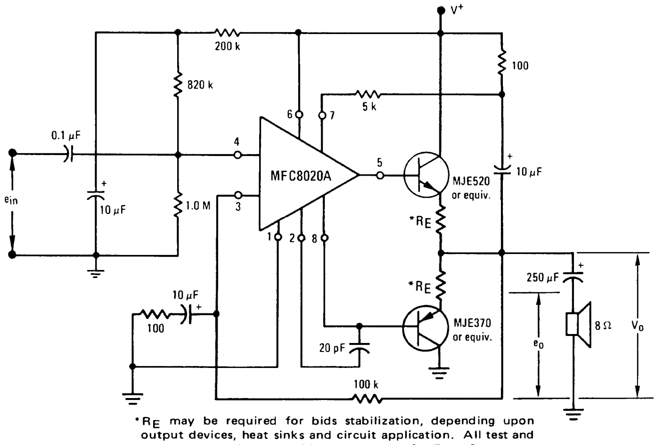


CASE 644A
PLASTIC PACKAGE

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+	35	Vdc
Thermal Resistance Derate above $T_A = +25^oC$	θ_{JA}	100 10	^oC/Watt mW/^oC
Operating Temperature	T_A	-10 to +75	^oC

FIGURE 1 – TYPICAL APPLICATION AND TEST CIRCUIT (10-WATT AMPLIFIER)



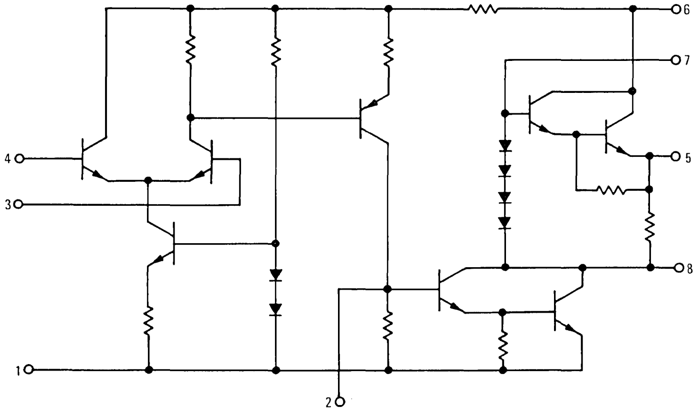
*R_E may be required for bids stabilization, depending upon output devices, heat sinks and circuit application. All test and measurements shown on this data sheet are for $R_E = 0$.

This is advance information and specifications are subject to change without notice.
See Packaging Information Section for outline dimensions.

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted) (See Figure 1)

Characteristic	Symbol	Min	Typ	Max	Unit
Drain Current (e_{in} = 0, V^+ = 32 Vdc)	I_D	–	10	30	mA
Sensitivity (f = 1.0 kHz, P_o = 10 W, e_o = 8.95 V[rms])	e_{in}	–	–	10	mV
Distortion @ 10 Watts Power Output (e_{in} adjusted to produce 10-Watts output, e_o = 8.95 V(rms), V^+ = 32 Vdc, f = 1.0 kHz)	THD	–	1.0	5.0	%
Quiescent Output Voltage (V^+ = 32 Vdc, e_{in} = 0)	V_o	15	16	17	Vdc

FIGURE 2 – CIRCUIT SCHEMATIC



MFC8030

HIGH FREQUENCY CIRCUIT

Advance Information

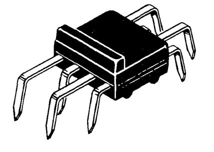
DIFFERENTIAL/CASCODE AMPLIFIER

. . . designed for applications requiring differential or cascode amplifiers.

- Extremely Flexible Amplifier
- Diode Available for Biasing
- Economical 8-Staggered Lead Package

DIFFERENTIAL/CASCODE AMPLIFIER

Silicon Monolithic Functional Circuit



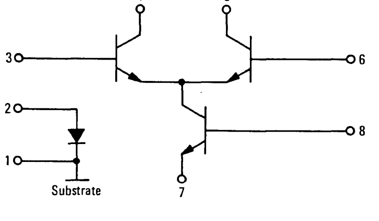
CASE 644A
PLASTIC PACKAGE

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+	20	Vdc
Differential Input Voltage	V_{in}	±5.0	Vdc
Power Dissipation @ T_A = 25°C (Package Limitation)	P_D	1.0	Watt
Derate above 25°C	$1/\theta_{JA}$	10	mW/°C
Operating Temperature Range	T_A	-10 to +75	°C

6

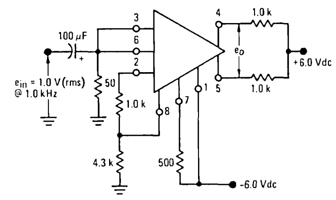
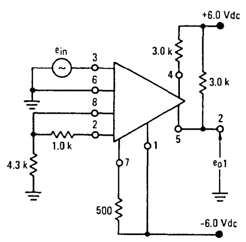
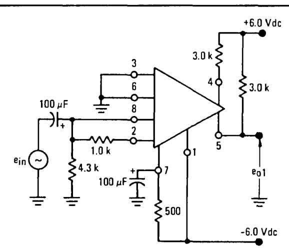
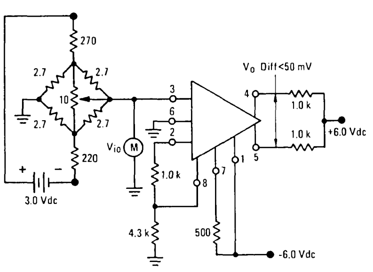
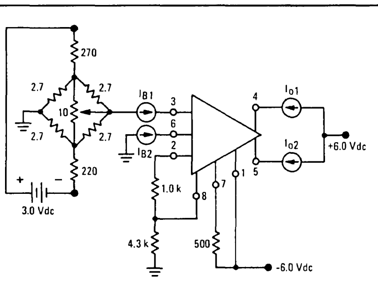
FIGURE 1 – CIRCUIT SCHEMATIC



See Packaging Information Section for outline dimensions.

MFC8030 (continued)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Circuit	Characteristic	Symbol	Min	Typ	Max	Unit
	AC Common-Mode Rejection $e_{4\text{-}5} = e_o$ $CMR = 20 \log \frac{(e_{in})}{(e_o)}$	CMR_{AC}	–	35	–	dB
	Differential-Mode Voltage Gain $A_V\ Diff = 20 \log \frac{(e_{o1})}{(e_{in})}$ (e_{in} = 1.0 kHz, 1.0 mV[rms]) (e_{in} = 10 MHz, 1.0 mV[rms]) (e_{in} = 50 MHz, 1.0 mV[rms])	$A_{V(dif)}$	 – – –	 32 26 10	 – – –	dB
	Cascode-Mode Voltage Gain $A_V\ Cascode = 20 \log \frac{(e_{o1})}{(e_{in})}$ (e_{in} = 1.0 kHz, 1.0 mV[rms]) (e_{in} = 10 MHz, 1.0 mV[rms]) (e_{in} = 50 MHz, 1.0 mV[rms])	$A_{V(cscd)}$	 – – –	 36 31.5 15	 – – –	dB
	Input Offset Voltage	V_{io}	–	5.0	10	mV
	DC Current Gain Match ($I_{01} = I_{02}$)	$\frac{h_{FE1}}{h_{FE2}}$	0.8	–	1.1	–

MFC8040

AUDIO PREAMPLIFIER

Advance Information

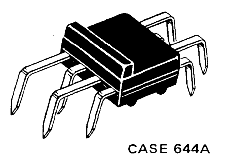
LOW NOISE AUDIO PREAMPLIFIER

. . . designed for high-gain, low-noise applications.

- Special Monolithic "State-of-the-Art" Process to Insure Low Noise – 1.0 μV (Typ)
- Can be Externally Equalized for NAB, RIAA
- Low Distortion – 0.1% (Typ) @ A_V = 100
- Large Dynamic Range – 7.0 V(rms) Out
- Low Output Impedance – 100 Ohms (Max)

LOW NOISE AUDIO PREAMPLIFIER

Silicon Monolithic Functional Circuit



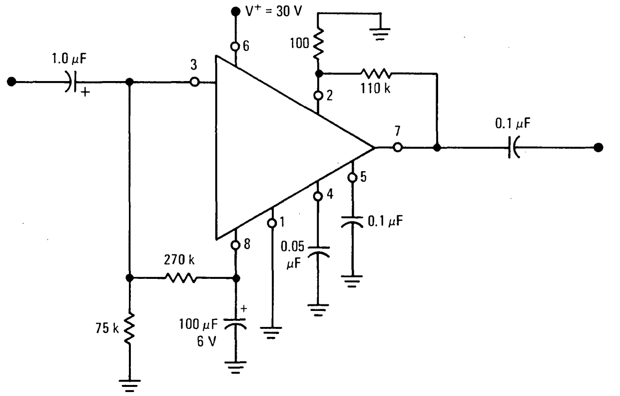
CASE 644A
PLASTIC PACKAGE

6

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+	33	Vdc
Power Dissipation @ T_A = 25°C (Package Limitation)	P_D	1.0	Watt
Derate above T_A = 25°C	$1/\theta_{JA}$	10	mW/°C
Operating Temperature Range	T_A	-10 to +75	°C

FIGURE 1 – TYPICAL WIDEBAND AMPLIFIER CIRCUIT (A_V = 60 dB)



See Packaging Information Section for outline dimensions.

ELECTRICAL CHARACTERISTICS ($T_A = 25^oC$ unless otherwise noted)

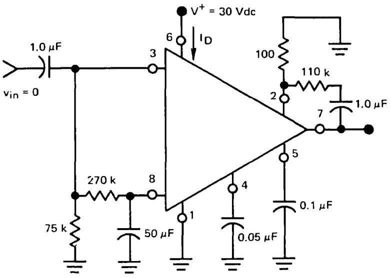
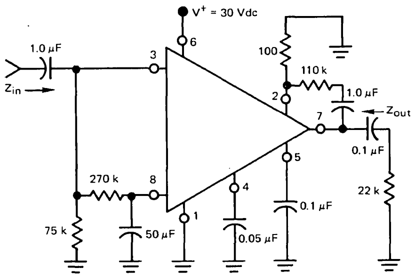
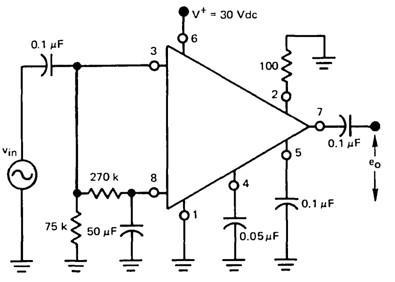
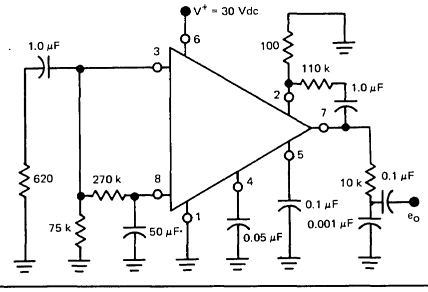
Circuit	Characteristic	Symbol	Min	Typ	Max	Unit
	Drain Current	I_D	–	8.0	12	mA
	Total Harmonic Distortion (v_o = 1.0 V, f = 1.0 kHz)	THD	–	<0.1	0.25	%
	Input Impedance	Z_{in}	–	75	–	k ohms
	Output Impedance	Z_{out}	–	100	–	ohms
	Open Loop Voltage Gain (v_{in} = 100 μV(rms) @ f = 1.0 kHz)	A_{VOL}	80	–	–	dB
	Wideband Input Noise (–3.0 dB Bandwidth, 10 Hz to 16 kHz, A_V = 60 dB @ 1.0 kHz, $\left(e_n = \frac{e_o}{A_V}\right)$	e_n	–	1.0	3.0	μV (rms)

FIGURE 2 – CIRCUIT SCHEMATIC

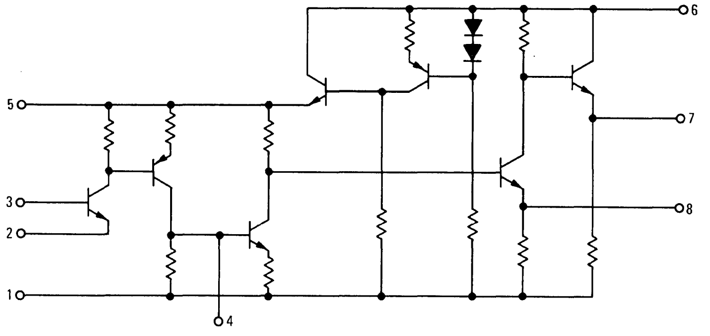


FIGURE 3 – INPUT NOISE

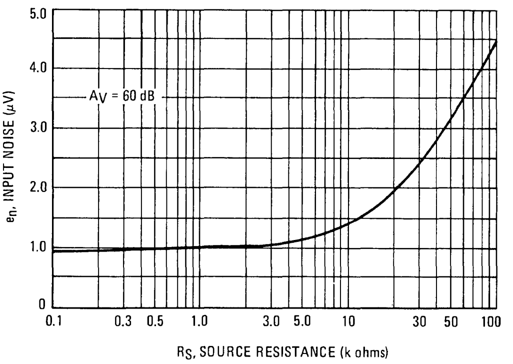


FIGURE 4 – OPEN LOOP TOTAL HARMONIC DISTORTION

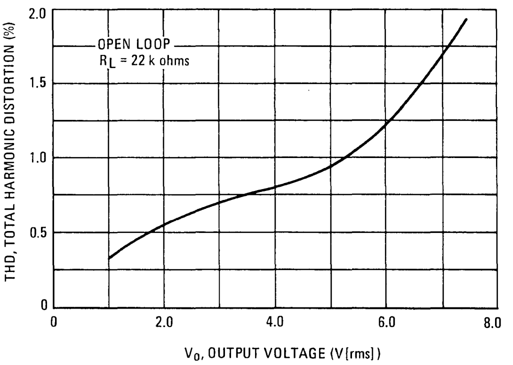
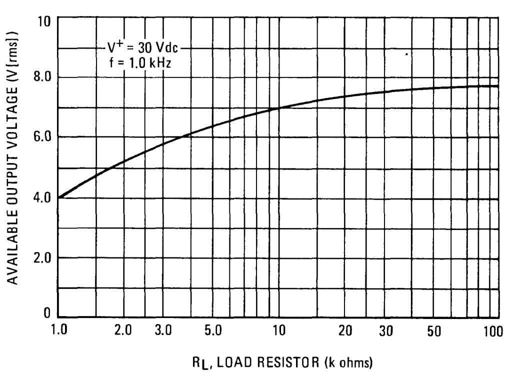


FIGURE 5 – AVAILABLE OUTPUT VOLTAGE



6

ZERO VOLTAGE SWITCH

MFC8070

Advance Information

ZERO VOLTAGE SWITCH

. . . designed for use in ac power switching applications with output drive capable of triggering triacs. Other operational features include:

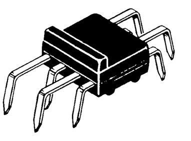
- A built-in voltage regulator that allows direct ac line operation
- A differential input with dual sensor inputs capable of testing the condition of two external sensors and controlling the gate pulse to a triac accordingly. Hysteresis or proportional control to this section may be added if desired.
- Sensor input "open and short" protection. This insures that the triac will never be turned "on" if either of the sensors are shorted or opened.
- A zero crossing detector that synchronizes the triac gate pulses with the zero crossing of the ac line voltage. This eliminates radio frequency interference (rfi) when used with resistive loads.

Typical Applications Include:

- Heater Controls
- Photo Controls
- Threshold Detector
- Lamp Driver
- Valve Control
- ON-OFF Power Controls
- Relay Driver
- Flasher Control

ZERO VOLTAGE SWITCH

Silicon Monolithic
Functional Circuit



PLASTIC PACKAGE
CASE 644A

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Voltage	V_{5-8}	15	Vdc
DC Voltage	V_{4-8}	15	Vdc
DC Voltage	V_{7-8}	15	Vdc
Power Dissipation @ T_A = 25°C Derate above 25°C	P_D $1/\theta_{JA}$	1.0 10	Watt mW/°C
Operating Temperature Range	T_A	-10 to +75	°C
Storage Temperature Range	T_{stg}	-55 to + 150	°C

This is advance information on a new introduction and specifications are subject to change without notice.
See Packaging Information Section for outline dimensions.

ELECTRICAL CHARACTERISTICS (T_A = 25° C unless otherwise noted)

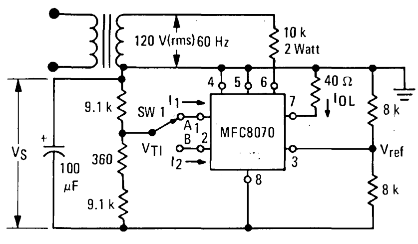
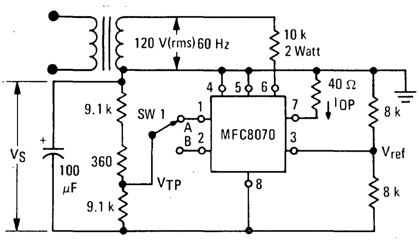
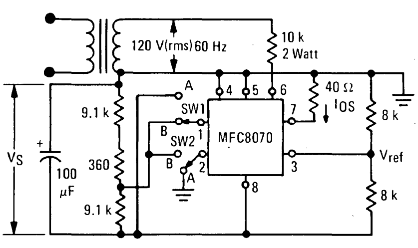
	Characteristic	Symbol	Min	Typ	Max	Unit
	V_S with Inhibit Output (Sw. 1: A or B)	V_{SI}	–	9.0	11	Vdc
	Output Leakage (Sw. 1: A or B)	I_{OL}	–	5.0	100	μA
	Input Current 1 (Sw. 1: A)	I_1	–	5.0	15	μA
	Input Current 2 (Sw. 1: B)	I_2	–	5.0	15	μA
	Inhibit Threshold (Sw. 1: A or B)	V_{TI}	V_{ref} +100 mV	V_{ref} +10 mV	–	Vdc
	V_S with Pulse Output (Sw. 1: A or B)	V_{SP}	6.0	8.5	–	Vdc
	Peak Output Current (Sw. 1: A or B)	I_{OP}	50	–	–	mA
	Pulse Threshold (Sw. 1: A or B)	V_{TP}	–	V_{ref} -10 mV	V_{ref} -100 mV	Vdc
	Output Pulse Width (Sw. 1: A or B) (See Figure 1)	τ_A, τ_B	–	70	–	μs
	Input Short Protection (Sw. 1: A; Sw. 2: B)	I_{OS}	–	5.0	100	μA
	Input Short Protection (Sw. 1: B; Sw. 2: A)	I_{OS}	–	5.0	100	μA

FIGURE 1 – OUTPUT PULSE DEFINITION

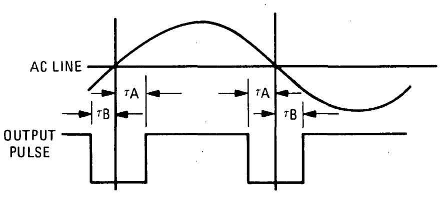


FIGURE 2 – CIRCUIT SCHEMATIC

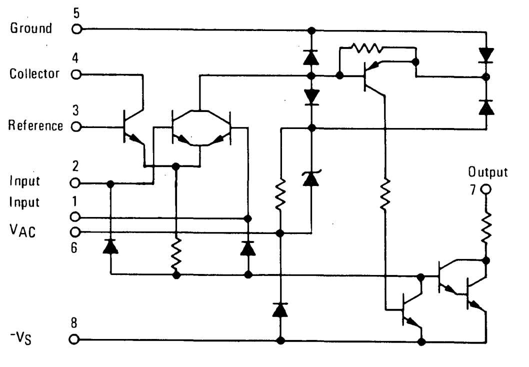


FIGURE 3 — CIRCUIT FOR MEASURING OUTPUT PULSE WIDTH versus SOURCE RESISTANCE

Suggested circuit to vary output pulse width by value of R_S (See Figure 4)

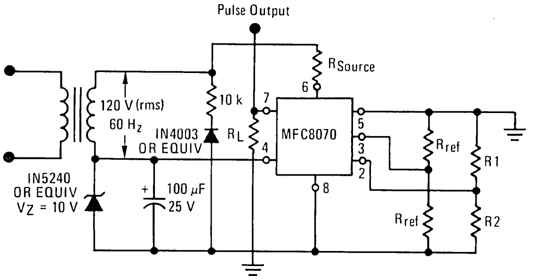
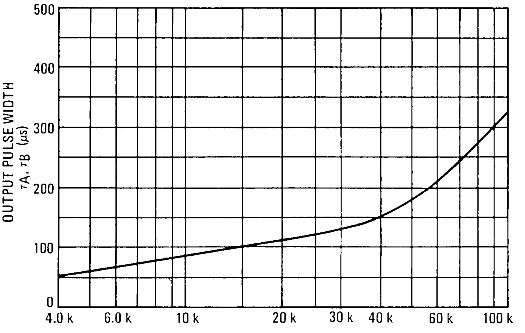
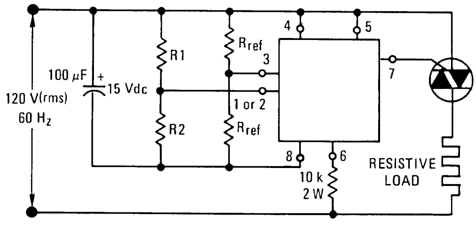


FIGURE 4 — OUTPUT PULSE WIDTH versus SOURCE RESISTANCE



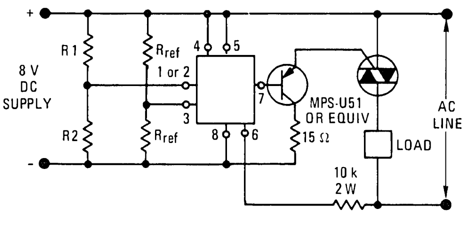
TYPICAL ZERO VOLTAGE SWITCH APPLICATIONS FOR TRIAC CONTROL

FIGURE 5 — TRIAC CONTROL CIRCUIT



Basic triac trigger circuit utilizing the zero crossing detector and the input comparator to control the gate of the triac.

FIGURE 6 — TRIAC CONTROL CIRCUIT WITH CURRENT BOOST UTILIZING DC SUPPLY

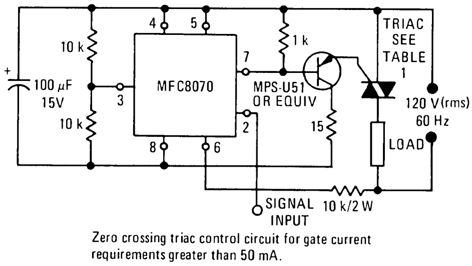


Basic DC trigger application using the input comparator to control a PNP capable of furnishing gate drive of approximately 0.5 Amp.

R1 is an external sensor

R2 must be the external sensor for the internal short and open protection to be operative.

FIGURE 7 — TRIAC CONTROL CIRCUIT WITH CURRENT BOOST UTILIZING AC SUPPLY



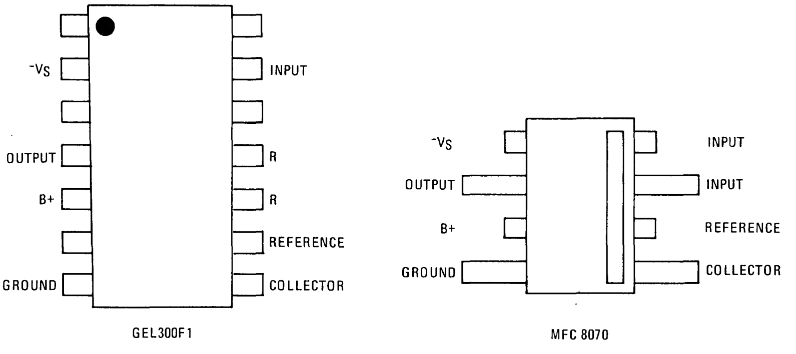
Zero crossing triac control circuit for gate current requirements greater than 50 mA.

Recommended Motorola triacs for use in circuit.

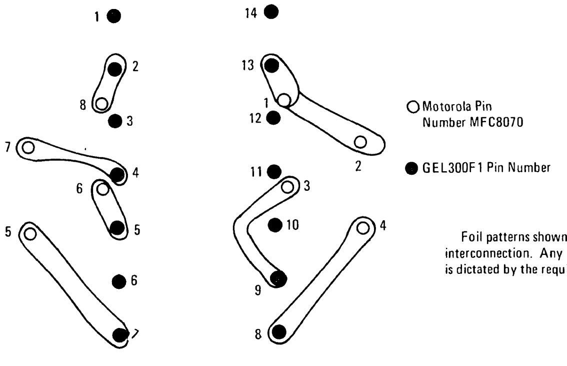
Maximum Continuous Current (Amp [rms])	Triac Family	Case No.
10	2N6154/2N6156 (MAC 10)	90 (Plastic)
10	2N6139/2N6144 (MAC 1, 2, 3)	85, 86, 87L
30	2N6157/2N6165 (MAC 35, 36)	174, 175

MFC8070 (continued)

PIN COMPARISON OF MFC8070 AND GEL300F1 (PA424)



COMPATIBLE PRINTED CIRCUIT FOIL PATTERN FOR MFC8070 AND GEL300F1 (PA424)



Foil patterns shown are intended to show pin-for-pin interconnection. Any change in the number of components is dictated by the requirements of the individual design.

MFC9020

AUDIO AMPLIFIER

Advance Information

2-WATT AUDIO AMPLIFIER

. . . designed to provide the complete audio system in television, radio and phonograph equipment.

- 2-Watts Continuous Sine Wave Power
- Minimal Heat-Sinking Required for Operation @ T_A = 55°C
- Short Circuit Proof (Short-Term)
- High Gain — 200 mV for 2-Watts Output Power
- High Input Impedance — 500 k Ohms

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+	24	Vdc
Output Peak Current	I_P	1.05	Amperes
Maximum Power Output T_A = 55°C (Free Air Mounting)	P_O	2.0	Watts

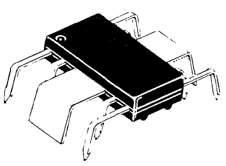
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance (Junction to Tab) Derate above 25°C	θ_{JC}	10 100	°C/W mW/°C
Thermal Resistance (Junction to Ambient) (1) Derate above 25°C	θ_{JA}	60 8.0	°C/W mW/°C

(1)Thermal resistance is measured in still air with fine wires connected to the leads, representing the "worst case" situation.
For a larger power requirement, the tab (pin 9) must be soldered to at least one square inch (effective area) of copper foil on the printed circuit board. The θ_{JA} will be no greater than +45°C/W. Thus, 2.0 Watts of audio power is allowable under "worst case" conditions at an ambient temperature of +65°C, which must be linearly derated at 22.2 mW/°C from +65°C to +150°C.

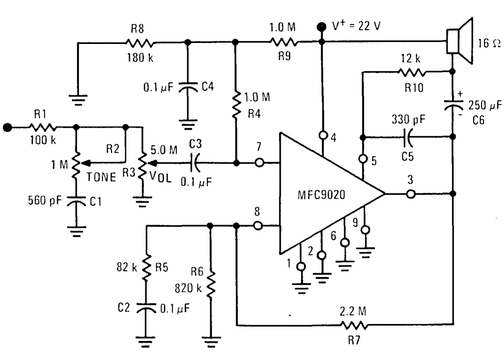
2-WATT AUDIO AMPLIFIER

Silicon Monolithic Functional Circuit



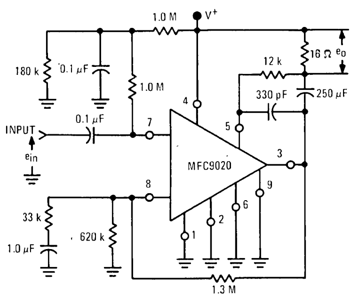
CASE 641
PLASTIC PACKAGE

FIGURE 1 — TYPICAL CIRCUIT APPLICATION



This is advance information and specifications are subject to change without notice.
See Packaging Information Section for outline dimensions.

ELECTRICAL CHARACTERISTICS (V^+ = 22 Vdc, T_A = 25°C unless otherwise specified)

Circuit	Characteristic	Symbol	Min	Typ	Max	Unit
	Quiescent Output Voltage	V_O	–	10	–	Vdc
	Quiescent Drain Current (e_{in} = 0)	I_D	–	12	20	mA
	Sensitivity Input Voltage (e_o = 4.0 V(rms) @ 1.0 kHz, P_O = 2.0 W)	e_{in}	–	–	200	mV
	Total Harmonic Distortion	THD				%
	(P_O = 2.0 W, 1.0 kHz)		–	1.0	10	
	(P_O = 100 mW, 1.0 kHz)		–	1.0	3.0	
	Hum and Noise *		–	-40	–	dB

*IHF STANDARD IHF-A-201 1966

Performance Curves for Circuit Shown Above.

FIGURE 2 – TOTAL HARMONIC DISTORTION

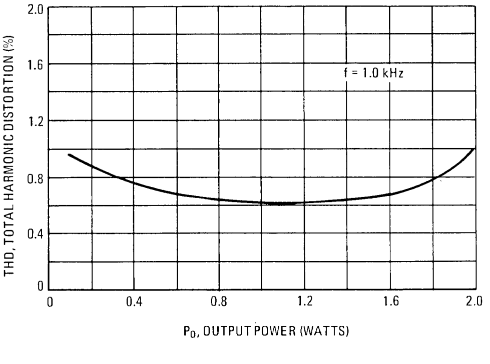


FIGURE 3 – POWER DISSIPATION

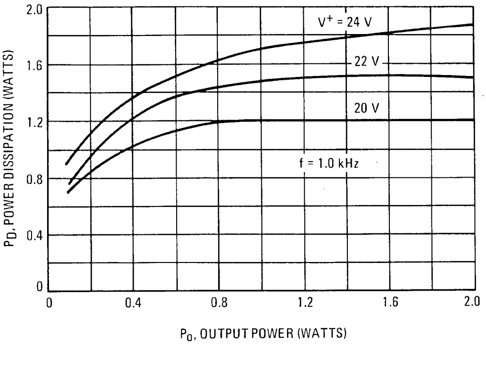


FIGURE 4 – TOTAL HARMONIC DISTORTION

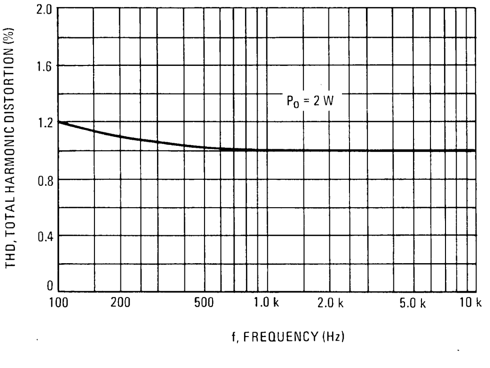
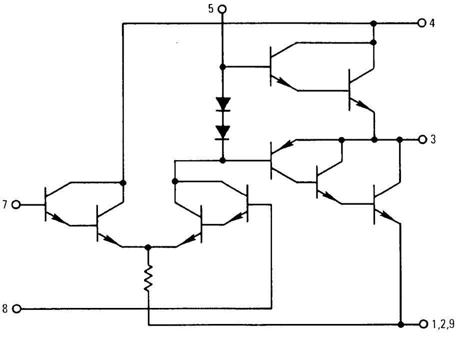


FIGURE 5 – CIRCUIT SCHEMATIC



Applications Information for Circuit Shown in Figure 1.

Figures 7 thru 11 pertain to the 2-watt amplifier with a 16-ohm load connected to V^+ as shown in Figure 1. The sensitivity of this amplifier is approximately 250 mV and the input impedance at 100 Hz is approximately 800 k ohms. R7/R5 determines the approximate gain that can be best altered by changing the value of R5 and holding R7 to a large value. This allows the use of a smaller and less expensive capacitor for C2.

The speaker can also be connected to ground as shown in Figure 6, and the printed circuit board art work (1:1 pattern) is shown in Figure 13.

The maximum operation voltage for the amplifier should reflect a consideration of at least a 10% high-line condition. Under high-line conditions, the power supply voltage should be less than the maximum rating of the device.

FIGURE 6 – ALTERNATE SPEAKER CONNECTION FOR SPEAKER TO GROUND

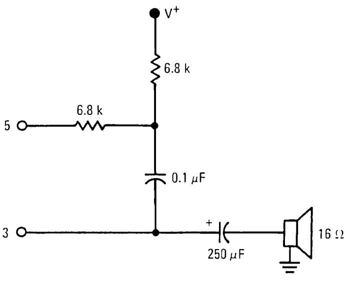


FIGURE 7 – TOTAL HARMONIC DISTORTION

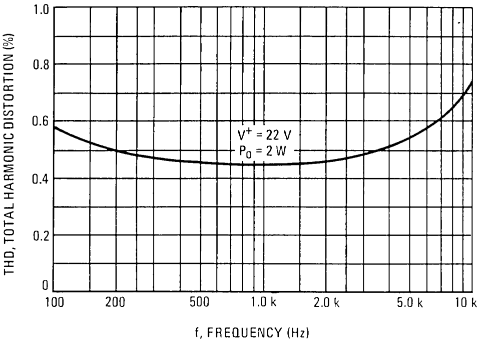


FIGURE 8 – POWER DISSIPATION

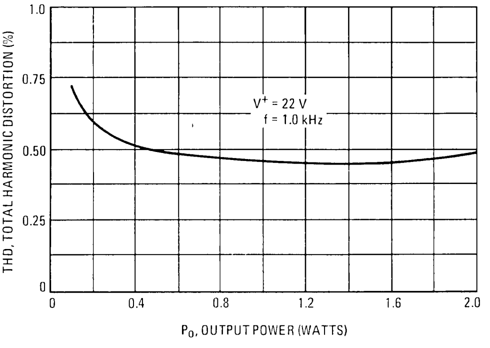


FIGURE 9 – FREQUENCY RESPONSE

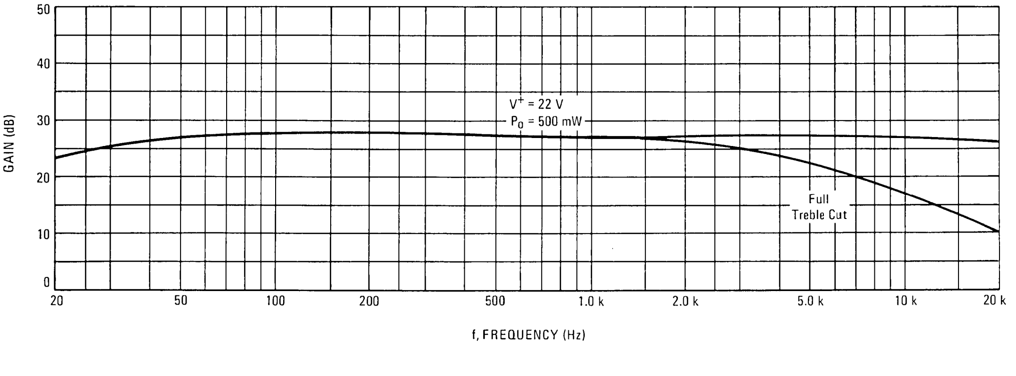


FIGURE 10 – PRINTED CIRCUIT BOARD
(Speaker to V+)

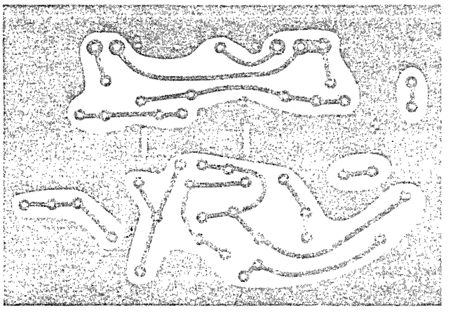


FIGURE 11 – COMPONENT DIAGRAM FOR FIGURE 10

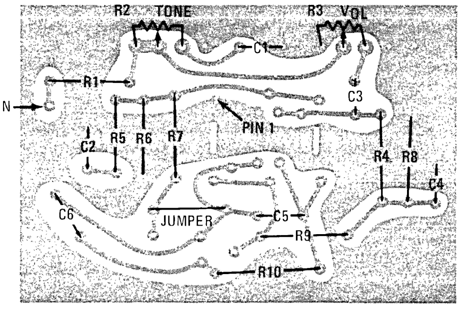


FIGURE 12 – COMPLETED BOARD
(Speaker to V+)

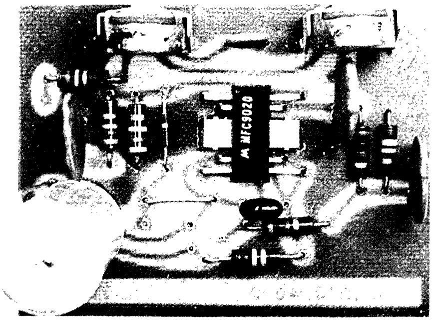
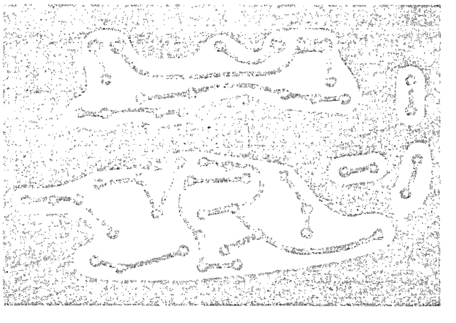


FIGURE 13 – PRINTED CIRCUIT BOARD
(Speaker to Ground)



MIC5830
MIC5830A
MIC5831

3dB QUADRATURE COUPLERS

MINIATURE 3 dB UHF QUADRATURE COUPLERS

. . . designed for use in applications such as power combining and dividing circuits, phase shifters, phase comparators, modulators and attenuators.

- Small Size – 1.25 x 1.25 x 0.140
- Low Insertion Loss – 0.25 dB (Max) to 0.35 dB (Max)
- High Isolation – 20 dB (Min)
- Small Coupling Variation

MINIATURE
3 dB UHF
QUADRATURE COUPLERS

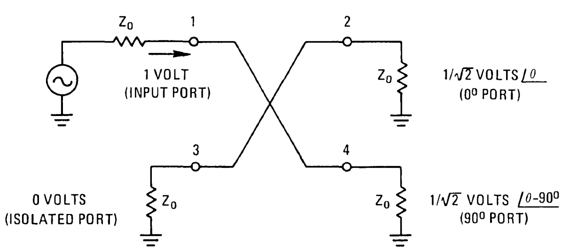
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

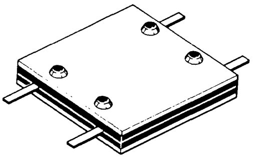
Model No.	Frequency Range (MHz)	Impedance (Ohms)	Isolation (dB) Min	Amplitude Balance (dB) Max	Phase Balance (°) Max	Insertion Loss (dB)	VSWR Input Max
MIC5830	225-400	50	20	±0.5	±1.5	0.25	1.2:1
MIC5830A	225-400	50	20	±0.7	±3.0	0.30	1.2:1
MIC5831	450-512	50	20	±0.5	±2.5	0.35	1.2:1

Maximum Input Power: 100 W Average
Operating Temperature: -55 to +100°C

6

SIGNAL RELATIONSHIPS IN A PROPERLY TERMINATED COUPLER





CASE 230

See Packaging Information Section for outline dimensions.

3 dB UHF QUADRATURE COUPLER PARAMETER DEFINITIONS

1. Insertion Loss - Coupler insertion loss is defined as losses in dB of one way transmission through the coupler with all ports terminated in 50 ohms.

   Insertion Loss in

   $$\text{dB} = 10 \log_{10} \frac{\text{(Input Power)}}{\text{(Power out of } 0^{\circ} \text{ port)} + \text{(Power out of } 90^{\circ} \text{ port)}}.$$

2. Isolation - Coupler isolation is defined as signal level difference in dB between input port and isolated port when the two output ports (0° port and 90° port) are terminated in 50 ohm loads.
3. Phase Balance - Coupler phase balance is defined as the phase difference between the two output signals minus 90°, with all ports terminated in 50 ohms.
4. Amplitude Balance - Amplitude balance is defined as the signal level difference (in dB) of the 0° port output and/or 90° port output referenced to the average output level.

   0° port Amplitude Balance in dB

   $$\text{dB} = 10 \log_{10} \frac{\text{(Power out of } 0^{\circ} \text{ port)}}{\dfrac{\text{(Power out of } 0^{\circ} \text{ port)} + \text{(Power out of } 90^{\circ} \text{ port)}}{2}}.$$

   90° port Amplitude Balance in dB

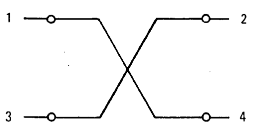
   $$\text{dB} = 10 \log_{10} \frac{\text{(Power out of } 90^{\circ} \text{ port)}}{\dfrac{\text{(Power out of } 0^{\circ} \text{ port)} + \text{(Power out of } 90^{\circ} \text{ port)}}{2}}.$$

APPLICATIONS INFORMATION

Motorola's 3 dB UHF couplers are stripline broadside couplers that are constructed from teflon fiberglass board and are sealed with a low loss, low dielectric compound. Small size is achieved by meandering the coupled lines.

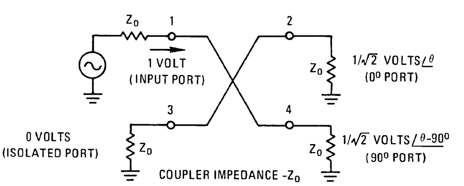
A 3dB UHF quadrature coupler is a four port network which can be depicted as shown in Figure 1. Application of a signal at

FIGURE 1 – 3 dB UHF Quadrature Coupler



any of the 4 ports (with all ports terminated in Z_0) results in equal signals at opposite port pairs with the adjacent port remaining isolated. For example, if a signal strength of one volt is applied to port 1 (see Figure 2), ideally the signals appearing at ports 2 and 4 will be $1/\sqrt{2}$ volts with a phase difference of 90°, none of the voltage will appear at port 3. Thus port 3 is called the isolated port.

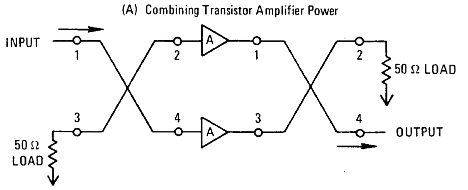
FIGURE 2 – Coupler driven by a signal source and terminated properly.



However if ports 2 and 4 are terminated in equal impedances other than Z_0 (examples would be open or short circuits) all of the reflected signal will appear at port 3 (isolated port). Thus the drive source would see a constant impedance of Z_0.

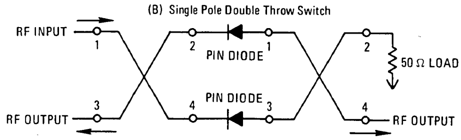
Applications - 3 dB UHF quadrature coupler applications are many, a few are given below.

(A) Combining Transistor Amplifier Power



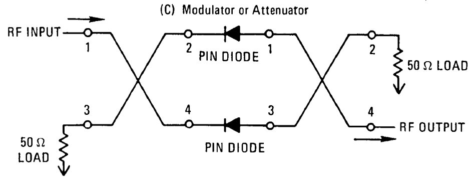
If the input impedances of the amplifiers are equal, reflected power will appear at port 3 resulting in a very low input VSWR. Output power at port 4 will be twice that of a single amplifier minus the coupler losses.

(B) Single Pole Double Throw Switch



By forward biasing the PIN diodes (low impedance mode) RF power can be switched to port 4. Reverse biasing the diodes (high impedance mode) results in power being switched to port 3 of the input coupler.

(C) Modulator or Attenuator



By changing the bias on the PIN diodes the level of RF appearing at port 4 of the output coupler can be controlled. For example, pulse modulation would result by switching the diodes off and on. An electrically controlled attenuator would be the result of varying the diodes between the off and on position.

6

MIC5830 and MIC5830A

FIGURE 3 – COUPLING versus FREQUENCY

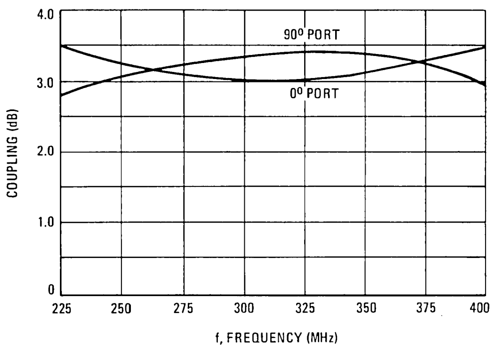


FIGURE 4 – INSERTION LOSS versus FREQUENCY

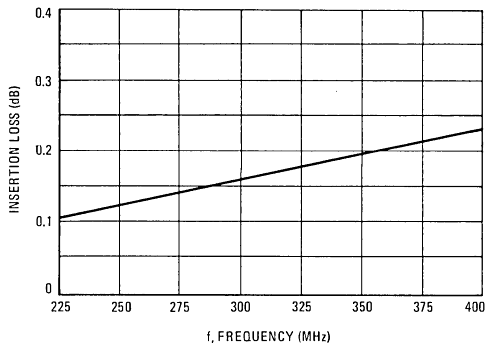


FIGURE 5 – ISOLATION versus FREQUENCY

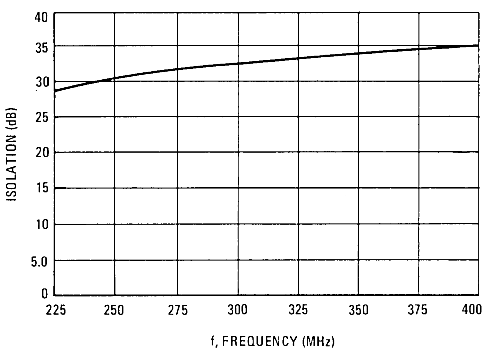


FIGURE 6 – INPUT VSWR versus FREQUENCY

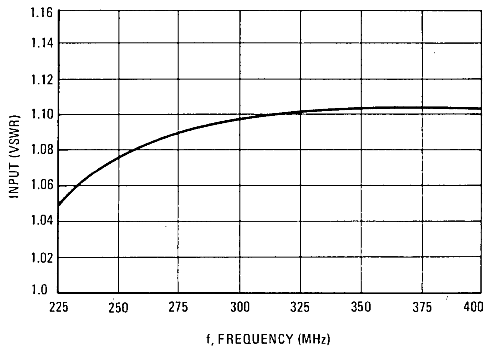
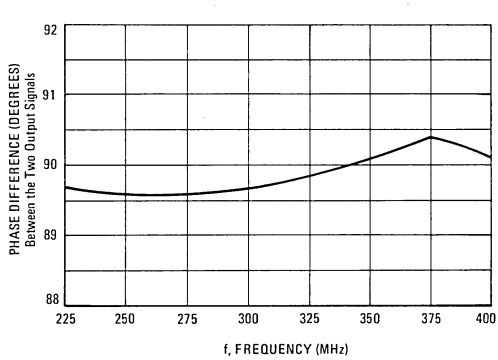


FIGURE 7 – PHASE DIFFERENCE versus FREQUENCY



MIC5831

FIGURE 8 – COUPLING versus FREQUENCY

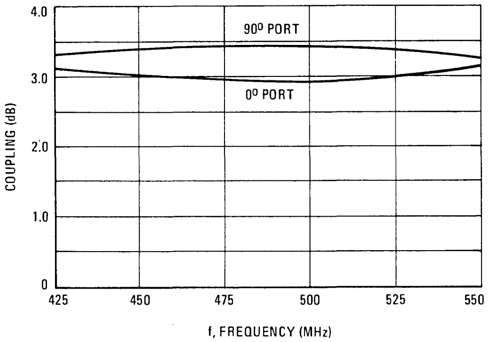


FIGURE 9 – INSERTION LOSS versus FREQUENCY

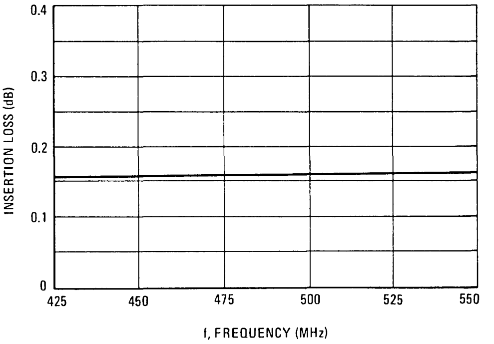


FIGURE 10 – ISOLATION versus FREQUENCY

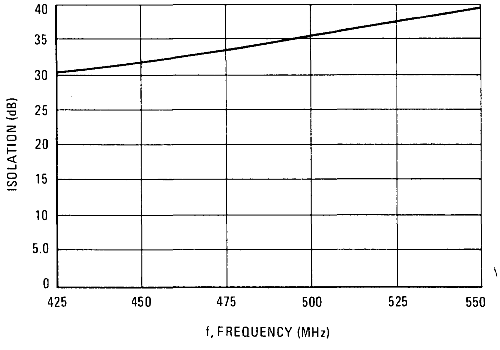


FIGURE 11 – INPUT VSWR versus FREQUENCY

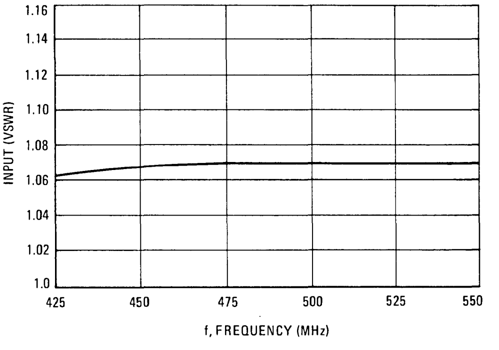
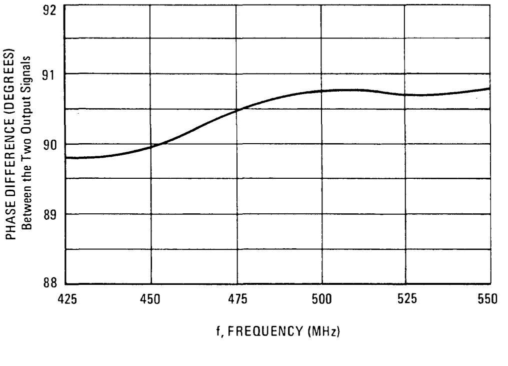


FIGURE 12 – PHASE DIFFERENCE versus FREQUENCY



MIC5840

POWER MODULE

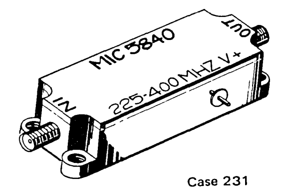
Advance Information

WIDEBAND POWER AMPLIFIER MODULE

The MIC5840 wideband solid-state amplifier is designed to operate as a driver or final amplifier in UHF military communications equipment. Thin-film inductors, ceramic capacitors and a special transistor carrier are utilized in this small size hermetically sealed module.

- Power Output —
  6 W (Min), f = 225 to 400 MHz
  7.5 W (Typ), f = 300 MHz
- Power Gain —
  5 dB (Min), f = 225 to 400 MHz
  8.5 dB (Typ), f = 300 MHz
- Capability For Amplitude Modulation
- Operating Temperature Range — -55 to +80°C

225 MHz to 400 MHz WIDEBAND POWER AMPLIFIER MODULE



Case 231

FIGURE 1 — SCHEMATIC DIAGRAM

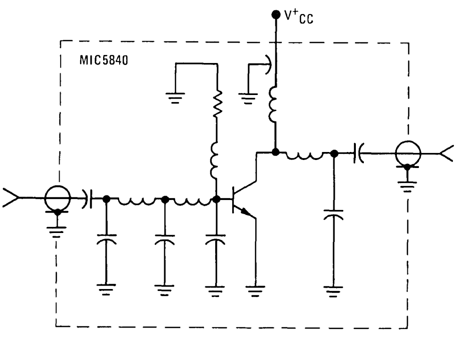
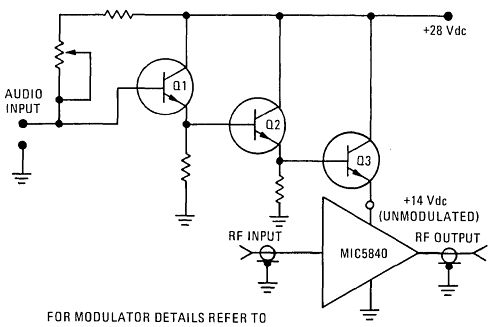


FIGURE 2 — AMPLITUDE MODULATION OF MIC5840 USING SERIES MODULATOR



FOR MODULATOR DETAILS REFER TO MOTOROLA APPLICATION NOTE AN-481

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Supply Current	I	1.5	Adc
Supply Voltage	V^+	35	Vdc
Power Dissipation (Total Module) Derate above T_A = 25°C	P_D	15 90	Watts mW/°C
Operating Temperature Range	T_A	-55 to +80	°C
Storage Temperature Range	T_{stg}	-65 to +125	°C

See Packaging Information Section for outline dimensions.

ELECTRICAL CHARACTERISTICS (V^+ = 26 Vdc, Frequency Range = 225 to 400 MHz, P_{out} = 6 Watts, T_A = 25°C unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency of Operation	f	225	–	400	MHz
Power Gain (50 Ohm Source and Load)	G_{PE}	5.0	7.0	–	dB
Collector Efficiency	η	30	–	–	%
Input Voltage Standing-Wave Ratio (f = 225 MHz to 275 MHz) (f = above 275 MHz)	VSWR	 – –	 – –	 9:1 3.5:1	–
Second Harmonic (referenced to fundamental) (f = 225 MHz to 275 MHz) (f = above 275 MHz)	–	 8.0 10	 – –	 – –	dB

TYPICAL CHARACTERISTICS

(V^+ = 26 V, P_{in} = 1.0 Watt, T_A = 25°C unless otherwise noted).

FIGURE 3 – OUTPUT POWER versus FREQUENCY

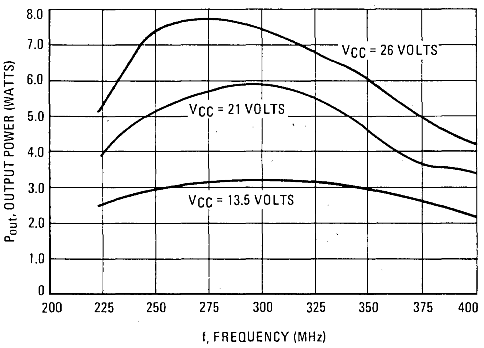


FIGURE 4 – OUTPUT POWER versus INPUT POWER

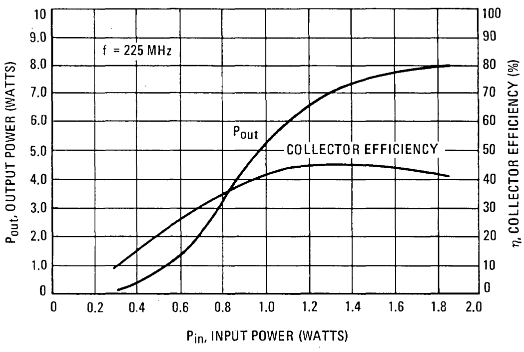


FIGURE 5 – OUTPUT POWER versus INPUT POWER

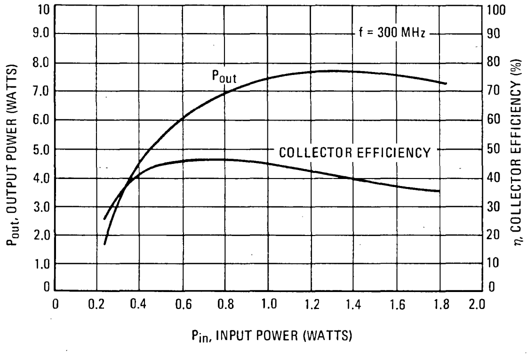
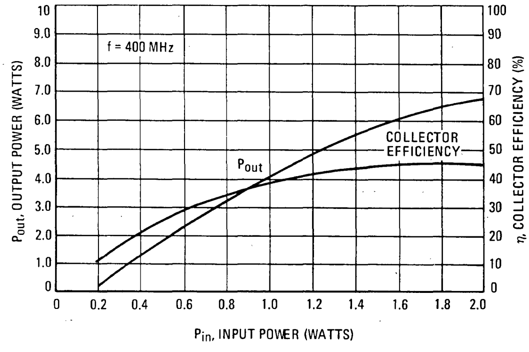


FIGURE 6 – OUTPUT POWER versus INPUT POWER



TYPICAL CHARACTERISTICS (continued)

(V^+ = 26 V, P_{in} = 1.0 Watt unless otherwise noted.)

FIGURE 7 – OUTPUT POWER versus SUPPLY VOLTAGE

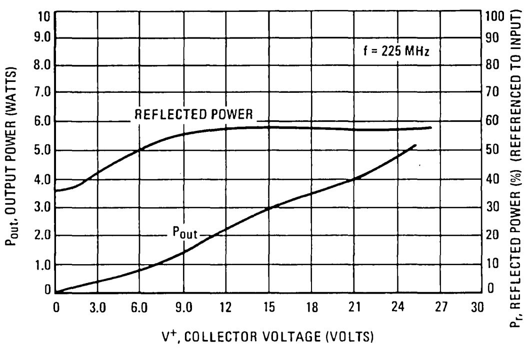


FIGURE 8 – OUTPUT POWER versus SUPPLY VOLTAGE

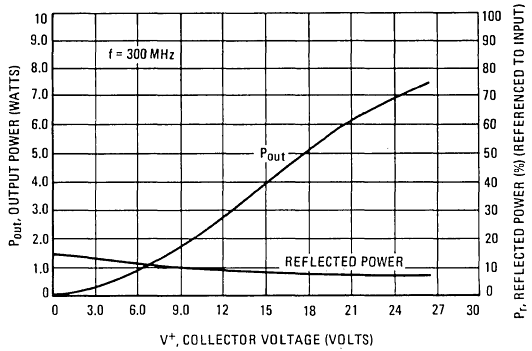


FIGURE 9 – OUTPUT POWER versus SUPPLY VOLTAGE

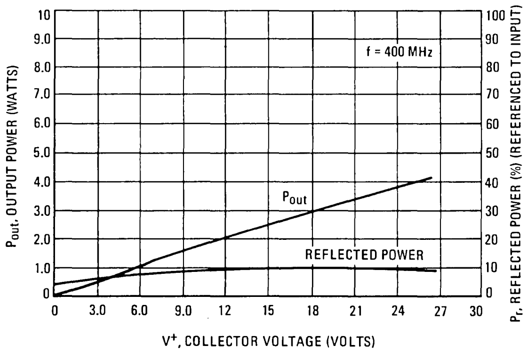
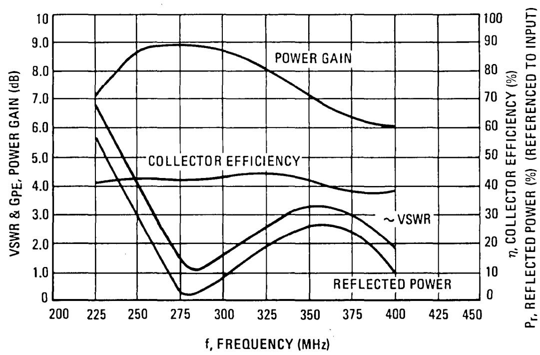


FIGURE 10 – COLLECTOR EFFICIENCY REFLECTED POWER VSWR AND POWER GAIN versus FREQUENCY



APPLICATIONS INFORMATION

The MIC5840 is a solid-state wideband amplifier module designed to operate as a driver or final amplifier in wideband UHF military communications equipment. The unit is capable of CW or AM operation. Its small size and electrical uniformity are achieved by using thin-film technology and a state-of-the-art NPN balanced-emitter UHF transistor. Unit weight≈ 1.0 ounce.

This hybrid module is hermetically sealed in an aluminum housing, with OSM®RF female connectors at the input and output terminals, and an internally RF bypassed pin for connection of the supply voltage (solder lug). Wideband input and output matching of the UHF transistor is accomplished by low loss thin-film inductors and ceramic chip capacitors mounted on alumina substrates. The transistor die is bonded to a beryllium oxide (BeO) carrier. These alumina substrates and the BeO carrier are then bonded to the aluminum chassis with all interconnections fabricated of gold ribbon or wire.

Figure 1 shows a schematic diagram of the MIC5840. RF drive from a 50-ohm source, a 50-ohm load impedance and a dc power source are required for CW operation from 225-400 MHz. Typical performance for this type of operation is shown in Figures 3 thru 10.

The MIC5840 can also be used for applications requiring high level amplitude modulation. As in most solid-state amplifiers of this type, the modulation is accomplished by varying the collector supply voltage in accordance with the modulating signal waveform. This arrangement is shown in Figure 2 where a series transistor modulator is used to vary the supply voltage applied to the MIC5840. The use of the series transistor modulator eliminates the need for a bulky audio power transformer. In this configuration, one half the dc supply voltage is dropped across Q3 of the modulator when no signal is applied to the audio input. When an audio signal is present at Q1, voltage applied to the MIC5840 is modulated. Since the gain of the MIC5840 is proportional to the applied voltage (Figures 7 thru 9) the RF output power is similarly modulated. During a modulating peak, care should be taken never to exceed the 35 Vdc maximum voltage rating. For the arrangement shown in Figure 2 up-modulation from a 14-volt quiescent value to peak value of 28 Vdc typically produces 50% up-modulation in the output power of the RF amplifier (3 W carrier). Since 100% up-modulation can seldom be achieved using only high level collector voltage modulation of a single stage amplifier, it is usually necessary to modulate the RF drive signal to some extent. Using driver stage modulation, the up-modulation capability of the MIC5840 can be made to approach 100%.

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6

MIC5890

DUPLEXER

Advance Information

MICROWAVE SOLID–STATE DUPLEXER

This unique solid-state circuit is designed to operate at frequencies between 400 MHz and 500 MHz with 40 Watts maximum input.

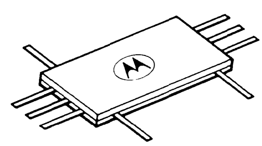
- High Input Power Capability – 40 Watts max
- Low Transmit-Mode Insertion Loss – 0.1 dB typ
- High Transmit-Mode Isolation – 25 dB typ
- Small, Lightweight Package

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

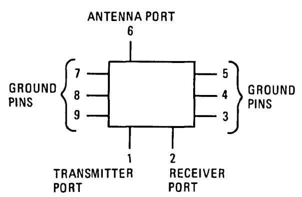
Rating	Symbol	Value	Unit
Forward dc Current (Pin 1)	I_F	0.10	Ampere
RF Power Input (Pin 1)	P_{in}	40	Watts
Operating Temperature Range	T_A	0 to +120	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

MICROWAVE SOLID–STATE DUPLEXER

INTEGRATED CIRCUIT

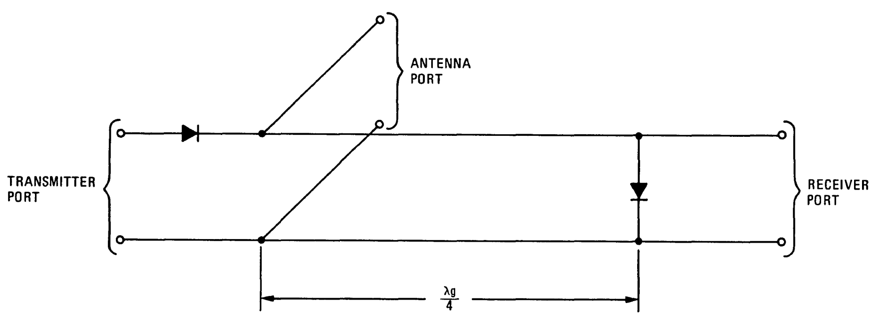


(Top View)



PLASTIC AND CERAMIC PACKAGE
CASE 631

PARALLEL WIRE REPRESENTATION



THE CHARACTERISTIC IMPEDANCE OF EACH ARM IS 50 OHMS.
λg IS THE WAVELENGTH.

See Packaging Information Section for outline dimensions.

ELECTRICAL CHARACTERISTICS (All ports terminated in a 50-ohm load, T_A = 25°C unless otherwise noted)

Characteristic	Min	Typ	Max	Unit
Isolation Between Transmitter Port and Receiver Port	20	25	–	dB
(P_{in} = 10 Watts, I_b* = 10 to 20 mA)				
f = 400 MHz, 460 MHz or 500 MHz				
(See Figure 1)				
Insertion Loss from Transmitter Port to Antenna				dB
(P_{in} = 10 Watts, I_b = 10 to 20 mA)				
f = 400 MHz	–	0.2	0.3	
f = 460 MHz	–	0.1	0.2	
f = 500 MHz	–	0.2	0.3	
(See Figure 1)				
Insertion Loss from Antenna Port to Receiver Port	–	0.4	0.6	dB
(P_{in} = −10 dBm, I_b = 0)				
f = 400 MHz, 460 MHz or 500 MHz				
(See Figure 2)				
Spurious Signal Level at Antenna Port				dB
(dB down from Transmitter Signal)				
(P_{in} = 10 Watts, I_b = 10 to 20 mA)				
f = 400 MHz { 2nd Harmonic	35	40	–	
f = 400 MHz { 3rd Harmonic	30	40	–	
f = 460 MHz { 2nd Harmonic	38	43	–	
f = 460 MHz { 3rd Harmonic	50	55	–	
f = 500 MHz { 2nd Harmonic	33	38	–	
f = 500 MHz { 3rd Harmonic	50	60	–	
(See Figure 1)				

*I_b = dc bias current applied to Pin 1 thru a 1.0 k ohm resistor.

FIGURE 1 – TRANSMIT–MODE TEST CIRCUIT

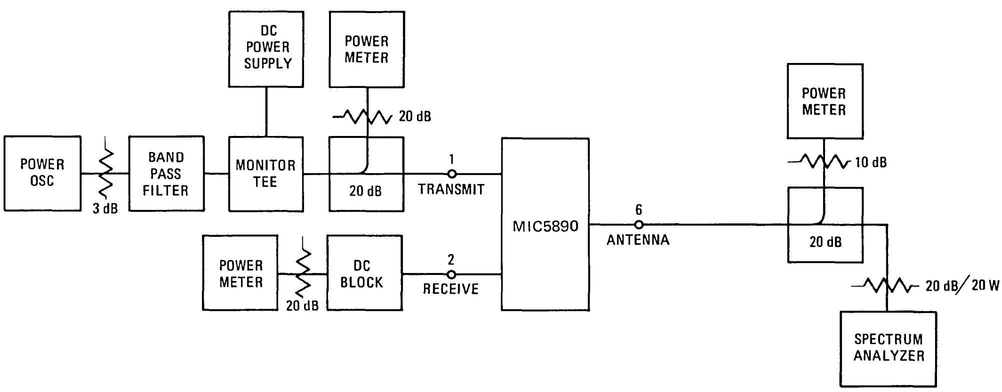
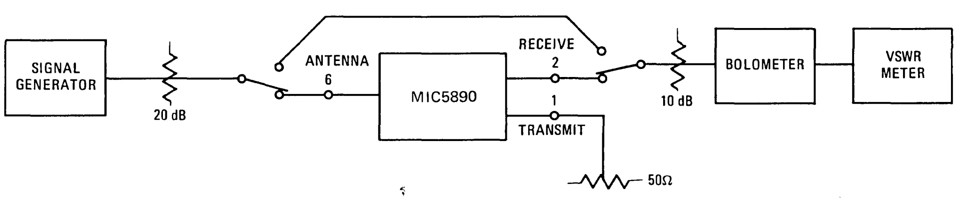


FIGURE 2 – RECEIVE–MODE TEST CIRCUIT



APPLICATIONS INFORMATION

The MIC5890 duplexer is a three port network (see Figure 3) that can be thought of as a single-pole double-throw switch connecting an antenna to a transmitter or receiver.

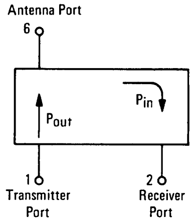


FIGURE 3 – THREE-PORT REPRESENTATION OF DUPLEXER

The MIC5890 is designed to operate from 400 MHz to 500 MHz, at an RF input power level of 40 Watts or less. The unit consists of two-step recovery diodes and a quarter-wave transmission line mounted on a 25-mil thick alumina substrate that is ½-inch wide and 1-inch long. A parallel-wire representation of the MIC5890 is shown in Figure 4, and a description of its operation follows.

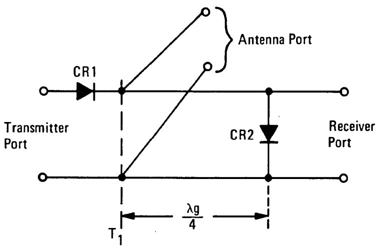
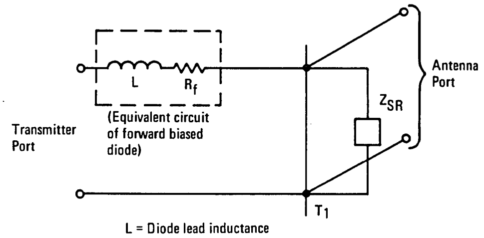


FIGURE 4 – PARALLEL WIRE REPRESENTATION OF THE MCH5890 DUPLEXER

The MIC5890 Duplexer has two modes of operation:

1. Transmit Mode – The antenna is connected to the transmitter and the receiver is disconnected.
2. Receiver Mode – The antenna is connected to the receiver and the transmitter is disconnected.

In the transmit mode the diodes are forward biased (by an external bias source of 10 mA to 20 mA) and are therefore low impedances. In this state of operation the transmitter is connected to the antenna via the low impedance of diode CR1. The receiver arm is effectively disconnected since diode CR2 (which is shunted across the receiver arm) appears as a high impedance when transformed a quarter-wavelength to the junction of all three arms (position T1 in Figure 4). Hence, the transmitted power is transferred to the antenna. An equivalent circuit of the duplexer in this mode of operation is shown in Figure 5.



L = Diode lead inductance

R_f = Diode forward bias resistance

Z_{SR} = Impedance looking into receiver arm at position T_1

$$Z_{SR} = \frac{Z_o^2}{Z_{rcvr} Z_{diode}/(Z_{rcvr} + Z_{diode})}$$

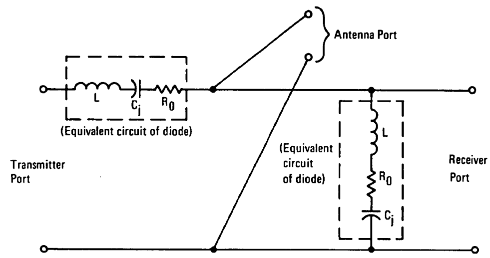
Z_o = Characteristic impedance of transmission line

Z_{diode} = Impedance of CR2 in forward-bias state.

Z_{rcvr} = Impedance of the receiver measured at the receiver port of the duplexer

FIGURE 5 – TRANSMIT MODE

Consider next the MIC5890 when operated in the receive mode. In this mode the bias is zero and the diodes appear as high capacitive reactances in series with resistors. Thus the effect is to disconnect the transmitter arm since diode CR1 appears as a large capacitive reactance. Diode CR2 does not appreciably load the receiver arm since it also appears as a large capacitive reactance. The equivalent circuit of the duplexer in this mode of operation is shown in Figure 6.



L = diode lead inductance

C_j = junction capacitance

R_0 = zero bias resistance

FIGURE 6 – PARALLEL-WIRE PRESENTATION OF DUPLEXER IN RECEIVE MODE OF OPERATION

The primary application of the duplexer is to connect the antenna either to the system receiver or transmitter. Another possible use for the MIC5890 is as a monitor network in a transmitter circuit. Using the duplexer in the transmit mode, the port usually designated as the "receiver" port can be used to monitor the frequency or output power level (if the port is previously calibrated) of the transmitter. An extension of this last application would be to use the MIC5890 duplexer as the sampling unit in an AFC or an AGC circuit. The energy from the "receiver" port can be fed back to appropriate comparatory circuits to establish an error signal for use in a feedback network. In a pulsed system, the pulse waveform could also be observed. Other applications will become apparent as the user becomes more familiar with the MIC5890.

MLM101AG
MLM201AG
MLM301AG

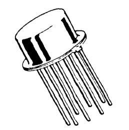
MONOLITHIC OPERATIONAL AMPLIFIER

The MLM101AG, MLM201AG, and MLM301AG are functionally, electrically, and pin-for-pin equivalent to the National Semiconductor LM101A, LM201A, and LM301A respectively.

- Low Input Offset Current – 20 nA maximum Over Temperature Range
- External Frequency Compensation for Flexibility
- Class AB Output Provides Excellent Linearity
- Output Short-Circuit Protection
- Guaranteed Drift Characteristics

OPERATIONAL AMPLIFIER

MONOLITHIC SILICON
INTEGRATED CIRCUIT



METAL PACKAGE
CASE 601
(TO-99)

Case connected to pin 4 through substrate

FIGURE 1 – STANDARD COMPENSATING AND OFFSET BALANCING CIRCUIT

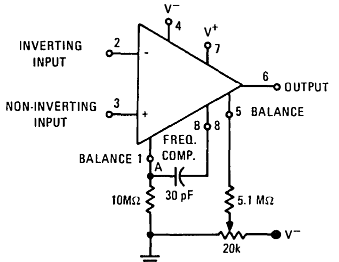


FIGURE 2 – FAST-SUMMING AMPLIFIER

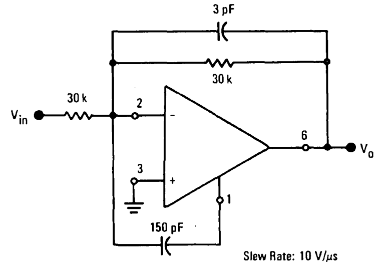


FIGURE 3 – DOUBLE-ENDED LIMIT DETECTOR

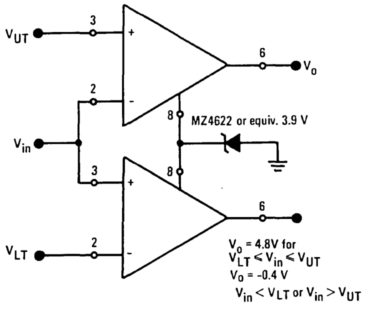
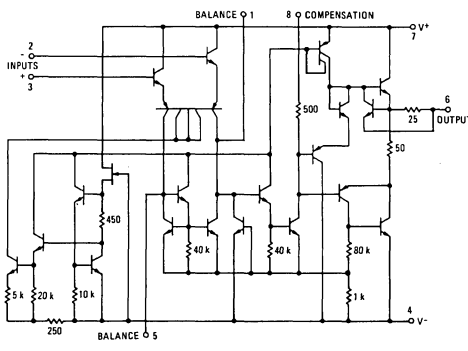


FIGURE 4 – CIRCUIT SCHEMATIC



See Packaging Information Section for outline dimensions.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	VALUE MLM101AG	MLM201AG	MLM301AG	Unit
Power Supply Voltage	V^+, V^-	±22	±22	±18	Vdc
Differential Input Voltage	V_{in}	←──── ±30 ────→			Volts
Common-Mode Input Swing (Note 1)	CMV_{in}	←──── ±15 ────→			Volts
Output Short Circuit Duration (Note 2)	t_{SC}	←──── Continuous ────→			
Power Dissipation (Package Limitation) Metal Can Derate above T_A = +75°C	P_D	 ←──── 500 ────→ ←──── 6.8 ────→			 mW mW/°C
Operating Temperature Range	T_A	-55 to +125	-25 to +85	0 to +70	°C
Storage Temperature Range	T_{stg}	←──── -65 to +150 ────→			°C

Note 1. For supply voltages less than ± 15 V, the absolute maximum input voltage is equal to the supply voltage.

Note 2. Unless otherwise specified, these specifications apply for supply voltages from ±5.0 V to ±20 V for the MLM101AG and MLM201AG, and from ±5.0 V to ±15V for the MLM301AG

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted, see Note 2 above.)

Characteristics	Symbol	MLM101AG MLM201AG Min	Typ	Max	MLM301AG Min	Typ	Max	Unit
Input Offset Voltage (R_S = ≤50 kΩ)	$\|V_{io}\|$	–	0.7	2.0	–	2.0	7.5	mV
Input Offset Current	$\|I_{io}\|$	–	1.5	10	–	3.0	50	nA
Input Bias Current	I_b	–	30	75	–	70	250	nA
Input Resistance	R_{in}	1.5	4.0	–	0.5	2.0	–	Megohms
Supply Current V_S = ±20 V V_S = ±15 V	I_D	 – –	 1.8 –	 3.0 –	 – –	 – 1.8	 – 3.0	mA
Large Signal Voltage Gain V_S = ±15 V, V_o = ±10 V, R_L>2.0 kΩ	A_V	50	160	–	25	160	–	V/mV

The following specifications apply over the operating temperature range.

Characteristics	Symbol	MLM101AG MLM201AG Min	Typ	Max	MLM301AG Min	Typ	Max	Unit
Input Offset Voltage (R_S≤ 50 kΩ)	$\|V_{io}\|$	–	–	3.0	–	–	10	mV
Input Offset Current	$\|I_{io}\|$	–	–	20	–	–	70	nA
Average Temperature Coefficient of Input Offset Voltage $T_{A(min)} \leq T_A \leq T_{A(max)}$	$\|TC_{V_{io}}\|$	–	3.0	15	–	6.0	30	µV/°C
Average Temperature Coefficient of Input Offset Current 25°C≤$T_A \leq T_{A(max)}$ $T_{A(min)} \leq T_A \leq$ 25°C	$\|TC_{I_{io}}\|$	 – –	 0.01 0.02	 0.1 0.2	 – –	 0.01 0.02	 0.3 0.6	nA/°C
Input Bias Current	I_b	–	–	100	–	–	300	nA
Large Signal Voltage Gain V_S = ±15 V, V_o = ±10 V, R_L>2.0 kΩ	A_V	25	–	–	15	–	–	V/mV
Input Voltage Range V_S = ±20 V V_S = ±15 V	V_{in}	 ±15 –	 – –	 – –	 – ±12	 – –	 – –	V
Common-Mode Rejection Ratio R_S≤50 kΩ	CM_{rej}	80	96	–	70	90	–	dB
Supply Voltage Rejection Ratio R_S≤50 kΩ	S^+, S^-	80	96	–	70	96	–	dB
Output Voltage Swing V_S = ±15 V, R_L = 10 kΩ R_L = 2.0 kΩ	V_o	 ±12 ±10	 ±14 ±13	 – –	 ±12 ±10	 +14 ±13	 – –	V
Supply Current (T_A = $T_{A(max)}$, V^+ = ± 20 V)	I_D	–	1.2	2.5	–	–	–	mA

APPLICATION NOTE ABSTRACTS

The application notes listed in this section have been prepared to acquaint the circuits and systems engineer with Motorola Linear integrated circuits and their applications. To obtain copies of the notes, simply list the AN number or numbers and send your request on your company letterhead to: Technical Information Center, Motorola Semiconductor Products Inc., P.O. Box 20924, Phoenix, Arizona 85036.

AN-204 High Performance Integrated Operational Amplifiers

Two new high performance monolithic operational amplifiers feature exceptionally high input impedance and high open loop gain. This note describes the function of each stage in the circuit, methods of frequency compensating and dc biasing. Four applications are discussed: a summing circuit, an integrator, a dc comparator, and transfer function simulation.

AN-247 An Integrated Circuit RF-IF Amplifier

A new, versatile integrated circuit for RF-IF applications is introduced which offers high gain, extremely low internal feedback and wide AGC range. The circuit is a common-emitter, common-base pair (the cascade connection) with an AGC transistor and associated biasing circuitry. The amplifier is built on a very small die and is economically comparable to a single transistor, yet it offers performance advantages unobtainable with a single device. This application note describes the AC and DC operation of the circuit, a discussion of Y-parameters for calculating optimum power and voltage gain, and a variety of applications as an IF single-tuned amplifier, IF stagger-tuned amplifier, oscillator, video-audio amplifier and modulator. A discussion of noise figure is also included.

AN-248 A High Voltage Monolithic Operational Amplifier

This note introduces a high voltage monolithic operational amplifier featuring high open loop gain, large common mode input signal, and low drift. The function of each stage in the circuit is analyzed, and methods for frequency compensating the amplifier are discussed. DC biasing parameters are also examined. Four applications using the amplifier are discussed: a source follower, a twin tee filter and oscillator, a voltage regulator, and a high input impedance voltmeter.

AN-261 Transistor Logarithmic Conversion Using an Operational Amplifier

The design of a log amplifier using a common base transistor configuration as the feedback element of an integrated circuit operational amplifier circuit is discussed in this application note. Six decades of logarithmic conversion are obtained with less than 1% error of output voltage. The possible causes of error are discussed followed by two applications: direct multiplication of two numbers, and solution of the equation $Z = X^n$.

AN-299 An IC Wideband Video Amplifier With AGC

This application describes the use of the MC1550 as a wideband video amplifier with AGC. The analysis of a single stage amplifier with 28 dB of gain and 22 MHz bandwidth is given with the results extended to a 78 dB video amplifier with 10 MHz bandwidth.

AN-400 An Operational Amplifier Tester

A simple and inexpensive tester for Motorola's line of operational amplifiers is described which will measure the open loop voltage gain, the equivalent input offset voltage, the maximum positive and negative output voltage swing, and a view of the transfer function which shows the linearity of the device.

Included is an elementary discussion of the parameters measured and their relationship to closed loop performance.

AN-401 The MC1554 One-Watt Monolithic Integrated Circuit Power Amplifier

This application note discusses four different applications for the MC1554, along with a circuit description including dc characteristics, frequency response, and distortion. A section of the note is also devoted to package power dissipation calculations including the use of the curves on the power amplifier data sheet.

AN-403 Single Power Supply Operation of IC Op Amps

A split zener biasing technique that permits use of the MC1530/1531, MC1533, and MC1709 operational amplifiers and their restricted temperature counterparts MC1430/1431, MC1433 and MC1709C from a single power supply voltage is discussed in detail. General circuit considerations as well as specific ac and dc device considerations are outlined to minimize operating and design problems.

AN-404 A Wideband Monolithic Video Amplifier

This note describes the basic principles of ac and dc operation of the MC1552G and MC1553G, characteristics obtained as a function of the device operating modes, and typical circuit applications.

AN-405 DC Comparator Operations Utilizing Monolithic IC Amplifiers

The use of the MC1533 operational amplifier and the MC1710 differential comparator are discussed. The capabilities and performance are given along with typical operating curves for both devices.

AN-407 A General Purpose IC Differential Output Operational Amplifier

This application note discusses four different applications for the MC1520 and a complete description of the device itself. The final sections of the note discuss such topics as operation from single and split power supplies, frequency compensation, and various feedback schemes.

AN-411 The MC1535 Monolithic Dual Op Amp

This note discusses two dual operational amplifier applications and an input compensation scheme for fast slew rate for the MC1535. A complete ac and dc circuit analysis is presented in addition to many of the pertinent electrical characteristics and how they might affect the system performance.

AN-421 Semiconductor Noise Figure Considerations

A summary of many of the important noise figure considerations related with the design of low noise amplifiers is presented. The basic fundamentals involving noise, noise figure, and noise figure-frequency characteristics are then discussed with the emphasis on characteristics common to all semiconductors. A brief introduction is made to various methods of data sheet presentation of noise figure and a summary is given for the various methods of measurement. A discussion of low noise circuit design, utilizing many of the previously discussed considerations, is included.

AN-432A A Monolithic Integrated FM Stereo Decoder System

This application note discusses the circuit approach that has been taken in the realization of the first monolithic integrated stereo multiplex decoder built for consumer usage, as well as some of the details concerning its incorporation in an FM stereo receiver.

AN-439 MC1539 Op Amp and its Applications

This application note discusses the MC1539, a second generation operational amplifier. The general use and operation of the amplifier is discussed with special mention made of improved operation over that of its first generation predecessor–the 709 type amplifier.

In addition to the detailed discussion on the dc and ac operation of the device, considerable emphasis is placed on operational performance. Many applications are offered to demonstrate the device capability, including a high frequency feed-forward scheme, and a source follower application.

AN-459 A Simple Technique for Extending Op Amp Power Bandwidth

The design of fast response amplifiers is presented without the use of "tricky" compensation procedures or calculations using data sheet information. Circuit analysis for compensation procedure is given.

AN-460 Using Transient Response to Determine Operational Amplifier Stability

This application note describes a technique for evaluating the stability of any particular feedback amplifier configuration by analyzing its response to a step-function input. A theoretical analysis is given along with an example.

AN-475 Using the MC1545 – A Monolithic, Gated-Video Amplifier

Because of the unique design of the MC1545, this amplifier can be used as a gated video amplifier, sense amplifier, amplitude modulator, frequency shift keyer, balanced modulator, pulse amplifier, and many other applications. This note describes the ac and dc operation of the circuit and presents applications of the device as a video switch, amplitude modulator, balanced modulator, pulse amplifier, and others.

AN-489 Analysis and Basic Operation of the MC1595

The MC1595 monolithic linear four-quadrant multiplier is discussed. The equations for the analysis are given along with performance that is characteristic of the device. A few basic applications are given to assist the designer in system design.

AN-490 Using the MC1595 Multiplier in Arithmetic Operations

This application note discusses the use of the MC1595 linear four quadrant multiplier in arithmetic operations. Included is a discussion of the MC1595 used in the multiply, divide, square and square root modes of operation. Actual circuits for these functions are shown with measured data and a discussion of the errors occurring in each mode.

AN-491 Gated Video Amplifier Applications The MC1545

This application note reviews the basic operation of the MC1545 and discusses some of the more popular applications for the MC1545. Included are several modulator types, temperature compensation of the active gate, AGC, gated oscillators, FSK systems, and single supply operation.

AN-513 A High Gain Integrated Circuit RF-IF Amplifier With Wide Range AGC

This note describes the operation and application of the MC1590G, a monolithic RF-IF amplifier. Included are several applications for IF amplifiers, a mixer, video amplifiers, single and two-stage RF amplifiers.

AN-522 The MC1556 Operational Amplifier and its Applications

This Application Note discusses the MC1556, a second generation, internally compensated monolithic operational amplifier. Particular emphasis is placed on its distinct advantages over the early 709-type amplifier and the more recent 741-type amplifier.

Along with a description of its operation this note presents a discussion on various applications of the MC1556, highlighting its capabilities, and points out its characteristics so the reader may make effective use of the device.

AN-531 MC1596 Balanced Modulator

The MC1596 monolithic circuit is a highly versatile communications building block. In this note, both theoretical and practical information are given to aid the designer in the use of this part. Applications include modulators for AM, SSB, and suppressed carrier AM; demodulators for the previously mentioned modulation forms; frequency doublers and HF/VHF double balanced mixers.

AN-533 Semiconductors for Plated-Wire Memories

An introduction to the operation and electrical characteristics of plated-wire memories is provided in conjunction with the applications of semiconductors that interface with the plated-wire memories.

Devices discussed include drivers, sense amplifiers, and decoders. Memory organization and memory-related semiconductor applications are also mentioned.

AN-543 Integrated Circuit IF Amplifiers for AM/FM and FM Radios

This application note discusses the design and performance of four IF amplifiers using integrated circuits. The IF amplifiers discussed include a high performance circuit, a circuit utilizing a quadrature detector, a composite AM/FM circuit, and an economy model for use with an external discriminator.

AN-544 A Printed Circuit VHF TV Tuner Using Tuning Diodes

A printed circuit VHF varactor tuner was designed and built in the Motorola Applications Laboratory. The design was centered around high capacitance tuning diodes, PIN band switching diodes, the dual-gate MOSFET, and a cascode mixer. This note describes the tuner, the design procedure, and the tuner performance.

AN-545 Television Video IF Amplifier Using Integrated Circuits

This applications note considers the requirements of the video IF amplifier section of a television receiver, and gives working circuit schematics using integrated circuits which have been specifically designed for consumer oriented products. The integrated circuits used are the MC1350, MC1352, MC1353 and the MC1330.

AN-546 Solid-State Linear Power Amplifier Design

Linear amplifier design techniques and new RF power transistors developed specifically for HF (2-30 MHz) linear amplifier services are discussed.

NOTES

6922 PRINTED IN USA 11-71 IMPERIAL LITHO B25540