MOTOROLA
Semiconductor Products Inc.

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Application Note

SYNCHRONIZING TWO MOTOROLA MC6802s ON ONE BUS

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The Motorola MC6802 Microprocessor is an extremely versatile system tool in many applications. One application that has presented some difficulty has been synchronizing two MC6802's on the same data bus. This application allows each MPU to operate during the half-cycle of $\phi 2$ (E) that the other MPU is disabled. This permits the added computing power of two MPU's while maintaining the system costs of one data bus. Furthermore, there is no time sacrificed since the half-cycle used would normally be "dead time" on the bus.

Normally, the Xtal and Extal inputs would have a 4 MHz crystal attached or a 4 MHz TTL signal going directly into the Extal TTL input (pin 39). The MPU, internally, divides the incoming frequency by four and derives the external "E" output from its internally generated $\phi 2$. Synchronizing cannot be accomplished if each MPU has its own crystal source. The "E" outputs will be asynchronous. If both MC6802s are driven directly from the same frequency source the enable (E) outputs may be 0^{o}, 90^{o}, 180^{o}, or 270^{o} apart in phasing. There is no synchronizing input pin on the part.

Three problems are inherent in construction of a cost effective Dual MC6802 system:

1. Developing a low cost frequency source to drive the MC6802's external inputs.
2. Phasing the "E" outputs of the MC6802's to be 180^{o} apart reliably before the start-up reset is disabled.
3. Insuring the internal propagation delays (sometimes called "slewing") are nearly identical to avoid overlapping of the "E" outputs when they are high.

The NAND gates labeled "A" and "B" on Figure I are used as an extremely low cost frequency source. This approach is reliable and always initializes. The frequency output is subject to the Temperature Coefficient and tolerance build-up of the parts used.

The MC6802's performance will not be degraded by this small frequency change, but it may be important in the rest of the system. If a better frequency source is needed—lower drift or tighter frequency tolerance—many standard circuits are available.

The NAND gates labeled "C" and "D" in Figure I function as a Phase Locked Loop and "D" synchronizes the phases of the enable outputs to be 180^{o} apart. Upon initialization, NAND gate "C" compares the state of the MC6802's enable outputs. If they are in contention (i.e., both outputs are high at the same time) gate "C" disables the oscillator frequency entering the Extal input to MC6802 unit #2. Gate "C" stops disabling gate "D" when MPU's #1 and #2 "E" outputs are 180^{o} out of phase (i.e., in synchronization—see Figure II). The worst case of synchronization will take $3\mu s$ to accomplish with a 4MHz input frequency (12 cycles of the input clock).

In order to avoid contentions once the MPU's are in synchronization, it is necessary to assure that the internal propagation delays (slew) are equal. There are two major factors controlling this propagation delay (Figure II). The most obvious is the package. The inherent body and lead frame difference between the plastic and ceramic packages offer different body capacitances to the chip. Since this is a consistent value, no problem will be encountered if the same package is used in both positions. Changes in the chip design will also cause a timing change. It is the nature of the state of the art in the NMOS IC business that the chip will be changed as time goes on. This problem can be avoided by using parts with matching date codes, thereby avoiding using two "different" MC6802's.

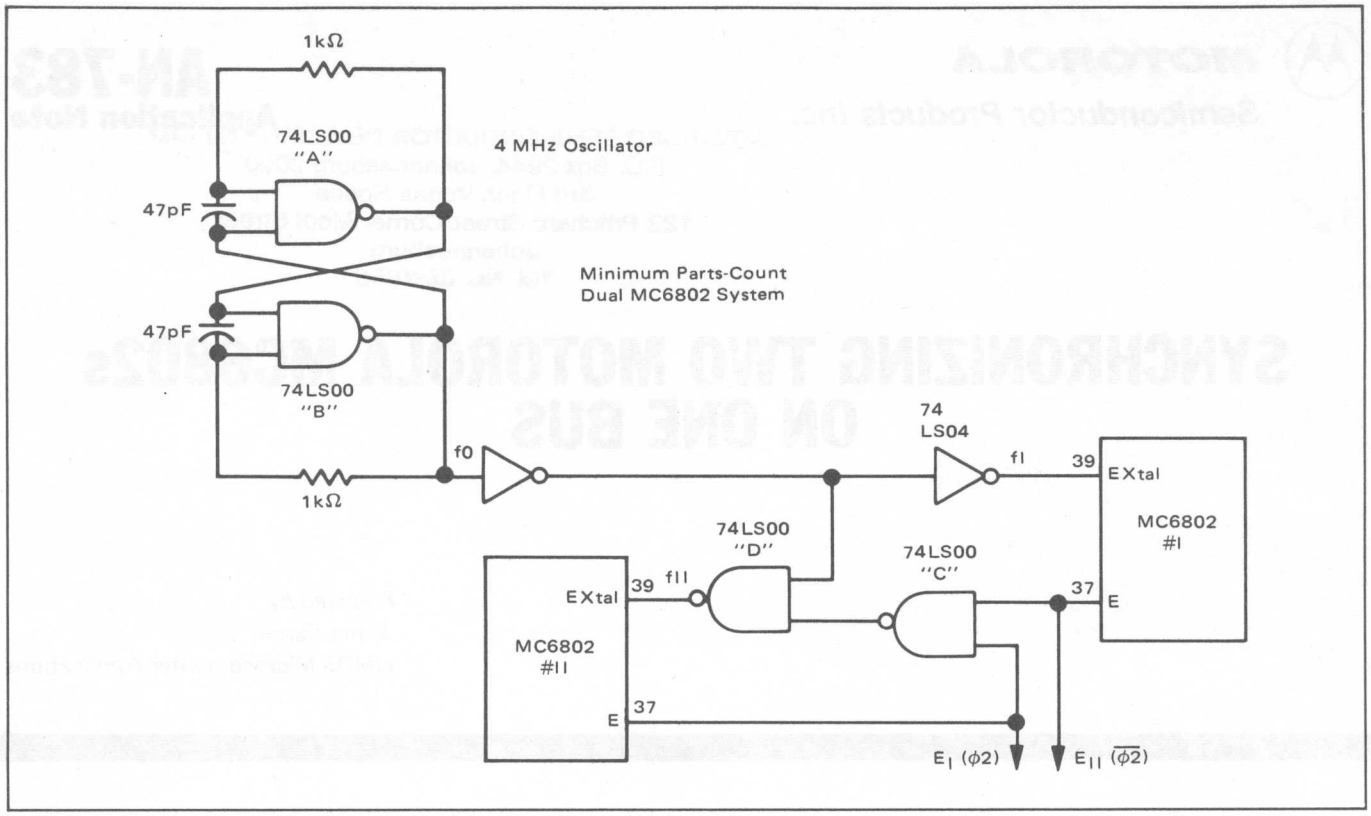

FIGURE I – 4 MHz Oscillator

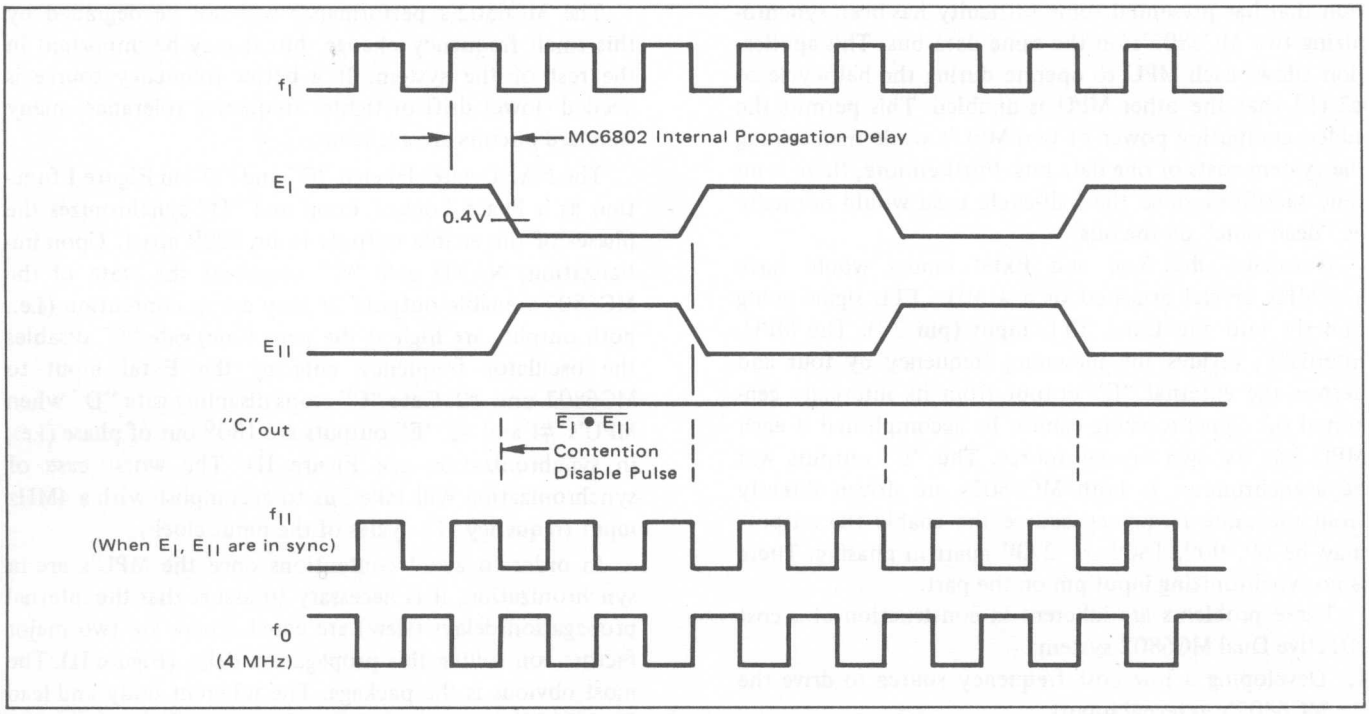

FIGURE II – Dual MC6802 Synchronizer Timing

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The data of Figure 1 applies for non-repetitive conditions and at a lead temperature of 25°C. If the duty cycle increases, the peak power must be reduced as indicated by the curves of Figure 2. Average power must be derated as the lead or ambient temperature rises above 25°C. The average power derating curve normally given on data sheets may be normalized and used for this purpose.

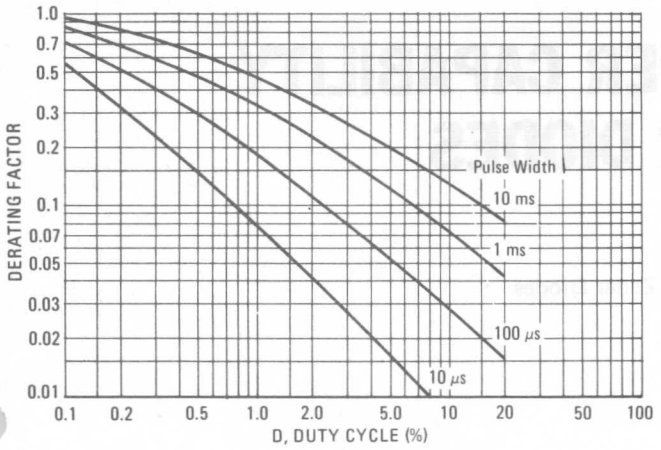

FIGURE 2 – Typical Derating Factor for Duty Cycle

When it is necessary to use a zener close to surge ratings, and a standard part having guaranteed surge limits is not suitable, a special part number may be created having a surge limit as part of the specification. Contact your nearest Motorola OEM sales office for capability, price, delivery, and minimum order quantities.

MATHEMATICAL MODEL

Since the power shown on the curves is not the actual transient power measured, but is the product of the peak current measured and the nominal zener voltage measured at the current used for voltage classification, the peak current can be calculated from:

$$I_{Z(PK)} = \frac{P_{(PK)}}{V_{Z(NOM)}} \quad (1)$$

The peak voltage at peak current can be calculated from:

$$V_{Z(PK)} = F_C \times V_{Z(NOM)} \quad (2)$$

where F_C is the clamping factor. The clamping factor is approximately 1.25 for all zener diodes having a nominal zener voltage greater than 12 volts, when operated at their pulse power limits. For example, a 10 watt, 20 volt zener can be expected to show a peak voltage of 25 volts regardless of whether it is handling 1250 watts for 0.1 ms or 160 watts for 10 ms. This occurs because the voltage is a function of junction temperature and IR drop. Heating of the junction is more severe at the longer pulse width, causing a higher voltage component due to temperature which is roughly offset by the smaller IR voltage component. Zener diodes with nominal voltages below 12 volts do not exhibit as consistent a behavior because of alloy junction nonuniformities; the clamping factor, however, rarely exceeds 1.5.

For modeling purposes, an approximation of the zener resistance is needed. It is obtained from:

$$R_{Z(NOM)} = \frac{V_{Z(NOM)}(F_C - 1)}{P_{PK(NOM)}/V_{Z(NOM)}} \quad (3)$$

The value is approximate because both the clamping factor and the actual resistance are a function of temperature.

CIRCUIT CONSIDERATIONS

It is important that as much impedance as circuit constraints allow be placed in series with the zener diode and the components to be protected. The result will be a lower clipping voltage and less zener stress. A capacitor in parallel with the zener is also effective in reducing the stress imposed by very short duration transients.

To illustrate use of the data, a common application will be analyzed. The transistor in Figure 3 drives a 50 mH solenoid which requires 5 amperes of current. Without some means of clamping the voltage from the inductor when the transistor turns off, it could be destroyed.

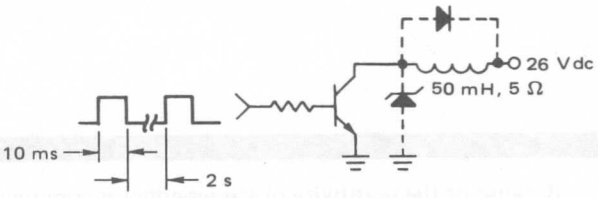

FIGURE 3 – CIRCUIT EXAMPLE

Used to select a zener diode having the proper voltage and power capability to protect the transistor.

The means most often used to solve the problem is to connect an ordinary rectifier diode across the coil; however, this technique may keep the current circulating through the coil for too long a time. Faster switching is achieved by allowing the voltage to rise to a level above the supply before being clamped. The voltage rating of the transistor is 60 V, indicating that approximately a 50 volt zener will be required.

The peak current will equal the on-state transistor current (5 amperes) and will decay exponentially as determined by the coil L/R time constant (neglecting the zener impedance). A rectangular pulse of width L/R (0.01 sec) and amplitude of I_{PK} (5 A) contains the same energy and may be used to select a zener diode. The nominal zener power rating therefore must exceed (5 A x 50) = 250 watts at 10 mS and a duty cycle of 0.01/2 = 0.5%. From Figure 2, the duty cycle factor is 0.62 making the single pulse power rating required equal to 250/0.62 = 403 watts. From Figure 1, one of the 1N6267 series zeners has the required capability. The 1N6287 is specified nominally at 47 volts and should prove satisfactory.

Although this series has specified maximum voltage limits, equation 3 will be used to determine the maximum zener voltage in order to demonstrate its use.

$$R_Z = \frac{47(1.25 - 1)}{500/47} = \frac{11.75}{10.64} = 1.1\Omega$$

at 5 amperes, the peak voltage will be 5.5 volts above nominal or 52.5 volts total which is safely below the 60 volt transistor rating.

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