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Application Note

TESTING MECL 10,000 INTEGRATED LOGIC CIRCUITS

Prepared by
Bill Blood
Applications Engineering

Circuit testing techniques become increasingly important as circuit speeds approach and exceed the 2 ns range. With MECL 10,000 and MECL III circuits it is possible to exploit their 50-ohm output drive capability to obtain highly accurate test data. This application note describes techniques for testing MECL 10,000 circuits for laboratory evaluation, and discusses key parameters which should be measured during incoming inspection rapid testing.

MOTOROLA Semiconductor Products Inc.

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INTRODUCTION

The use of high speed logic circuits can be very beneficial to the system manufacturer. High speed logic offers a better performance/cost ratio than slower logic types, and thus an advantage in the competitive market-place for digital equipment. Because of the high performance offered by logics such as MECL 10,000, it may be necessary for the user to adjust his test procedures to get good test correlation between his measurements and Motorola's device specifications. Initially, correlation is important in the laboratory evaluation performed by a potential circuit user. If data sheet performance can not be verified, it is difficult to design with or use the parts.

After a decision to purchase components has been made, the important test is "incoming inspection." This testing is often performed under conditions differing from data sheet specified operation. It is possible to modify incoming inspection test limits to compensate for temperature stabilization or air flow and still insure that parts meet data sheet specifications. Motorola uses such a technique in high speed final testing of the MECL 10,000 and MECL III circuits.

Circuit performance must also be tested under *system* operating conditions during system checkout and rework. This testing need not be as thorough as component evaluation, but it must not interfere with overall system operation. The tester should be aware of the effects of system loading on circuit performance and possible inaccuracies deriving from normal system checkout test equipment operating at MECL 10,000 circuit speeds.

This application note describes methods for testing MECL 10,000 circuits to obtain results which correlate with the data sheet specifications. Test fixtures will be described and examples of expected results from typical MECL 10,000 circuits will be given. The parameters tested, and deviations of these parameters from guaranteed values when circuits are tested in other than the data-sheet-specified environment, will also be discussed.

Factors Involved in Testing

With circuit speeds approaching and exceeding 2 ns, some of the methods used for testing and evaluating such circuits must be modified from techniques used with lower speed circuits. To determine circuit performance accurately it is necessary to minimize distortion from outside sources. The technique used with MECL 10,000 and MECL III circuits is to keep the complete test system in a controlled 50-ohm transmission-line environment.

The 50-ohm transmission line system provides several benefits. By terminating all interconnection lines, signal reflections are eliminated. This results in waveforms undistorted by overshoot or ringing.

With transmission line interconnections, the propagation delays of signal paths are easily controlled and matched. As an example of how critical this can be, it should be noted that at MECL 10,000 circuit speeds, signal lines mismatched by 1.5 inches of length can cause a 10% error in test results.

An additional advantage of the 50-ohm system is its capability to drive 50-ohm test equipment inputs directly (oscilloscopes, frequency counters, etc.). Generally, 50-ohm inputs are more accurate and consistent than high input impedance probes. Probe calibration is very critical when evaluating circuits to within 100 ps accuracies.

Other factors influencing test results include temperature and air flow. MECL 10,000 circuits are specified at 25°C ambient air temperature, with 500 linear feet per minute air flow (to simulate normal system operating conditions). The logic outputs are defined after the circuit temperature has stabilized under the above conditions. Because of a possible different ambient environment temperature during testing, MECL input and output logic levels may differ from specified values by predictable, small amounts due to a differing circuit temperature. For example, testing in still air would result in a higher junction temperature, which would affect dc test results slightly. In many cases this small change in parameter values can be ignored, because the parts have a sufficient guardband to remain within specification limits. In other cases the logic test levels should be altered to compensate for circuit temperature. Methods for calculating junction temperature and modified test logic levels will be shown in the section on high speed testing later in this note.

A MECL 10,000 Test Fixture

Figure 1 shows the schematics for typical MECL 10,000 test fixtures. A pulse generator capable of generating pulses with MECL 10,000 edge speeds is connected directly to the logic circuit input. The generator line then continues to the 50-ohm 'scope where it is properly terminated by the 'scope in its characteristic 50-ohm impedance. The junction point at the gate input is kept as short as possible (normally under 1/2 inch) to minimize any impedance discontinuities arising at this point. All interconnecting cables are 50-ohm coaxial cable. RG188AU or equivalent coax is commonly used because of its flexibility and thinness.

The output of the MECL circuit is connected to the other 50-ohm 'scope input with a similar 50-ohm cable. The cable from the circuit input to the 'scope, and the cable from the circuit output to the 'scope, are equal in length to eliminate propagation delay skew due to differing signal propagation delay times in the cables. Cable length from the pulse generator to gate input is not critical. Long cable lengths should be avoided because of bandwidth limitations which would arise from their excessive length. Up to 5-foot cable lengths can be used with MECL 10,000 circuits without problems.

An important feature of the test fixture is the use of 50-ohm terminated lines for all signal interconnections. Proper matched-impedance termination minimizes reading distortions which might be caused by signal reflections or crosstalk. The 50-ohm drive capability of the MECL 10,000 family and the fact that circuits are specified with 50-ohm loads are factors which aid in testing and evaluation of the parts. By eliminating high impedance probes, testing accuracy and repeatability of results becomes very good.

MECL 10,000 outputs are specified when driving 50-ohm loads to -2 Vdc (measured from ground). However, the 'scope input is itself a 50-ohm impedance to ground. For this reason, the normal -5.2 volt power supply for MECL is offset by 2.0 Vdc in the test fixture as shown in Figure 1a. V_{CC} is connected to +2.0 Vdc and V_{EE} to -3.2 Vdc. This permits terminating all signals in the system to ground.

The full military temperature range parts in the MECL 10,000 product line (MC10500 and MC10600) are specified for driving 100-ohm (minimum) loads. To test

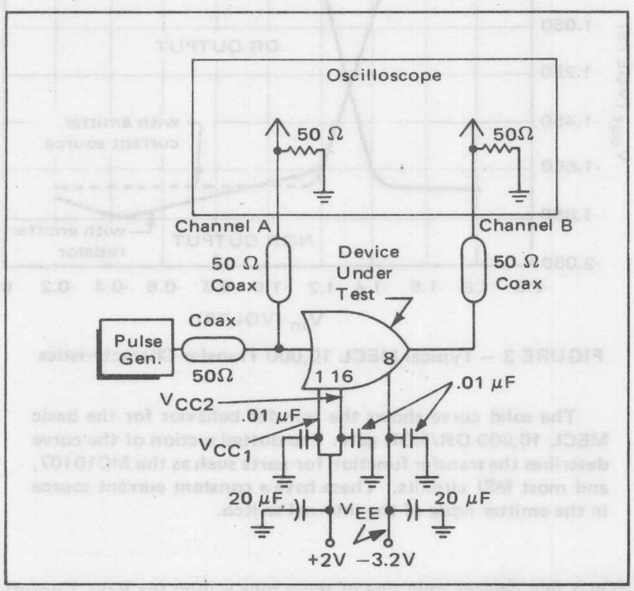

FIGURE 1A – MECL 10,000 Test Fixture Schematic

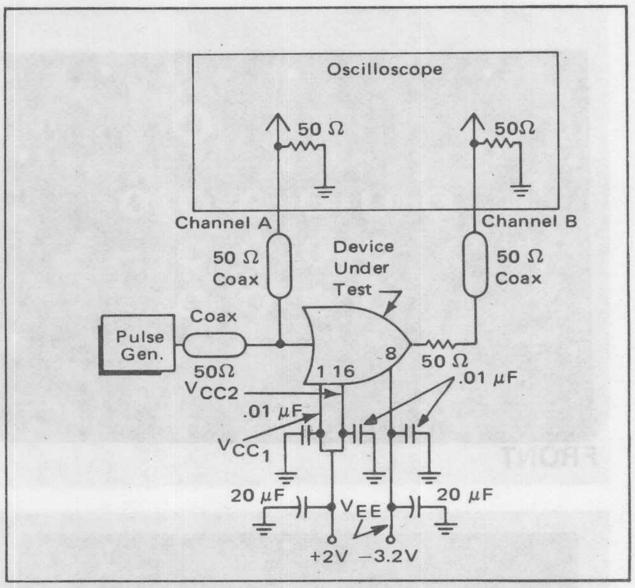

FIGURE 1B – Test Fixture Schematic for MC10,500 & 10,600 Series Parts

these parts, the test fixture is modified as shown in Figure 1b, by the addition of a 50-ohm series resistor on the gate output. This arrangement still allows use of the oscilloscope 50-ohm input, but does cause a 2-to-1 amplitude reduction which must be taken into consideration when interpreting 'scope readings.

Capacitor bypassing at IC sockets is used on both power supply lines to eliminate the possibility of voltage noise spikes. Such noise can be caused by the voltage source at the circuit responding to current fluctuations during circuit switching. The current fluctuations arise from unequal output current requirements between the logic levels, rather than from noise generated by switching in the basic MECL gate circuit. Supply voltage spikes could distort ac test information. They can be removed by heavy capacitor bypassing as shown in Figure 1. The 0.01 μF capacitors should be an RF (low inductance) type.

A MECL 10,000 test fixture for component evaluation is shown in Figure 2. The front view shows the miniature coaxial cable connectors for each circuit signal lead. The connectors are wired directly to the IC pins with semi-rigid 50-ohm coaxial cable*. These cables are matched in length for equal propagation delay. Outputs are easily observed by connecting a cable between the pin connector and the 'scope input. For best test results, unused circuit outputs should be terminated with 50-ohm loads at the connector.

The output from the pulse generator is connected to the pulse input connector of the test fixture. This signal is routed to a terminal near the circuit pins via semi-rigid coax cable (cf Figure 2B). A jumper runs to the desired IC input pin with a short wire. The jumper is soldered in as necessary to drive different input pins. A coaxial cable

*e.g., Precision Tube Co., "Coaxitube" AA50085, or equivalent.

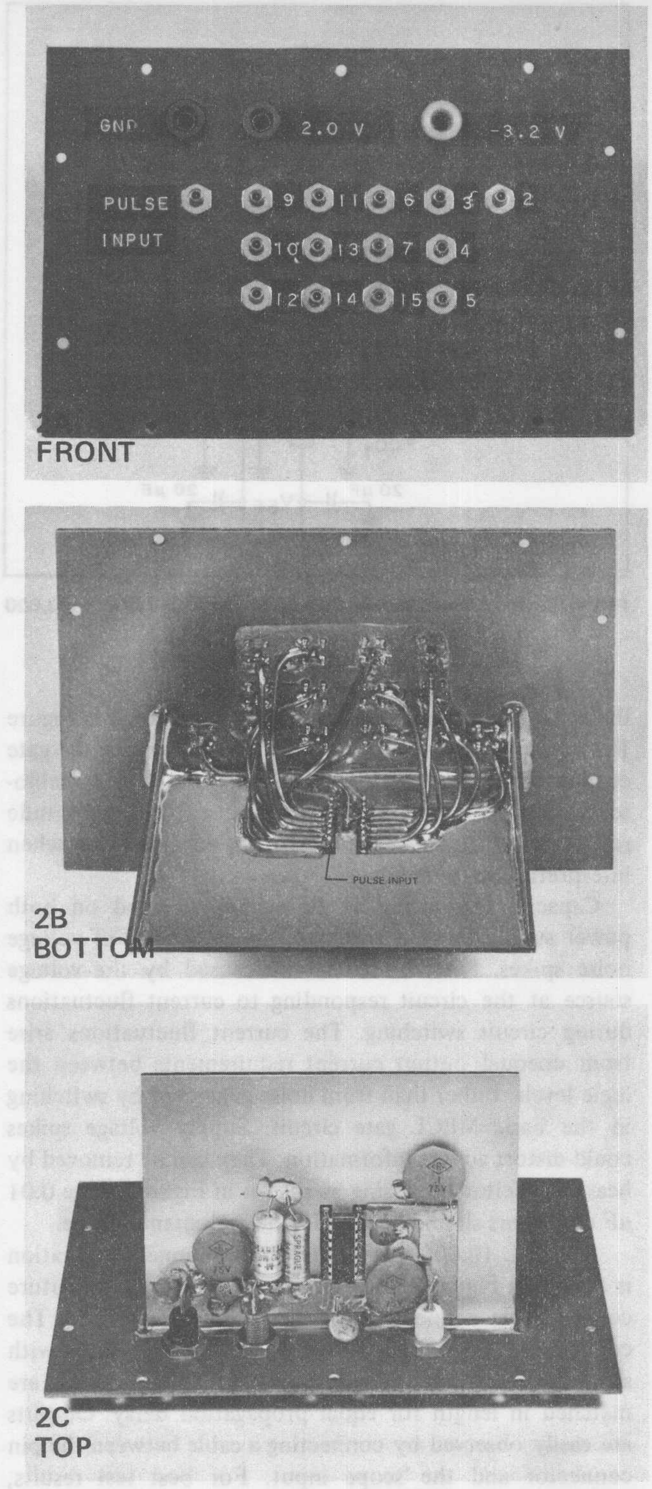

FIGURE 2 – Views of MECL 10,000 Test Fixture

from the IC input pin connector on the front panel of the test jig, to the 'scope input, provides for observing the input pulse and terminating the pulse generator.

The three power supply inputs are: ground; +2.0 Vdc; and -3.2 Vdc. The inputs are routed through standard banana plugs, for easy connection to power supplies. The ground input is connected to a reference voltage plane and to all coaxial cable or connector shields. The +2 Vdc input is bussed to pins 1 and 16 with a wide bus wire, or the metal of a circuit board. Both pins 1 and 16* are connected to the +2 Vdc bus close to the package. This line is well bypassed to ground. The V_{EE} line is similarly connected to pin 8 with a heavy bus and bypass capacitors.

The MECL 10,000 circuits should be plugged into a low-profile integrated circuit socket. An alternate approach is to remove the pins from a low-profile socket and connect these pins to the circuit board material from which the test set is built. (This approach has been found to be more appropriate when heavy use of the test fixture is expected.) The size of the test fixture is made compatible with the oven used for thermal testing.

This type of test fixture is easily constructed and is very good for low-volume laboratory evaluations. The fixture is acceptable for testing any 16-pin MECL 10,000 circuit, and the results will be very precise. The limitation of this type of test set comes in the handling of parts, and test equipment controls for large volume testing. For large volume testing an automated system is preferable.

Test Parameters

Circuit tests are usually performed to confirm data sheet specifications. These tests are of two general types: dc testing, and ac testing. DC testing measures logic levels or noise margins, circuit current, and input currents. AC testing measures propagation delays, edge speeds, and flip-flop toggle rates. It should be noted that MECL 10,000 dc parameters are specified with a grounded V_{CC}, -2 Vdc termination, and -5.2 Vdc on V_{EE} (as the parts are normally used in a system).

AC parameters are specified with the test fixture at +2.0 Vdc on V_{CC}, ground termination, and -3.2 Vdc on V_{EE} as discussed earlier. Other circuit parameters not included in the data sheets, but often measured, include: input capacitance, input impedance, and output impedance. The difficulty of performing these tests with

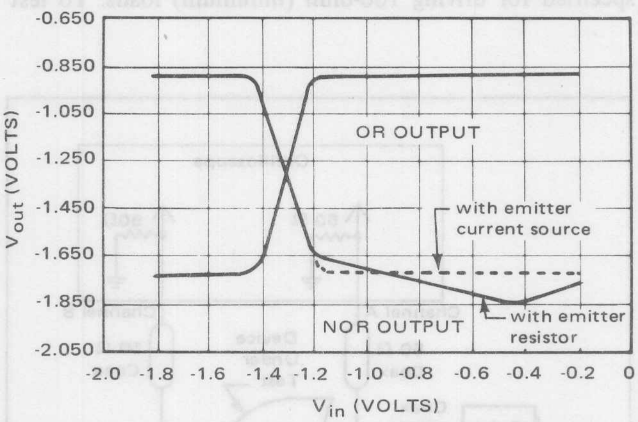

FIGURE 3 – Typical MECL 10,000 Transfer Characteristics

The solid curve shows the transfer behavior for the basic MECL 10,000 OR/NOR gate. The dotted section of the curve describes the transfer function for parts such as the MC10107, and most MSI circuits. These have a constant current source in the emitter node of the internal switch.

*On a few devices only one of these pins is used for V_{CC}. Consult specific part data sheets.

high-speed final test equipment makes specifying these parameters impractical for standard parts.

MECL circuit transfer characteristics are often plotted during device qualification. Plotting transfer characteristics is accomplished by putting a variable input voltage on the circuit input and measuring the output voltage. Figure 3 shows the typical transfer characteristics for MECL 10,000 logic functions. The test fixture previously described in this note may be used for transfer characteristic measurement by connecting a power supply to the input pin through the coaxial connector and loading all output pins with 50-ohm loads. The output of a selected load is then connected to a voltmeter. Loads other than 50-ohms may be used to evaluate circuit performance, but the data sheet values are specified with 50-ohm loads*. The 50-ohm load specification is a worst case test condition. With lighter loads, the MECL circuits will have a larger logic swing. Since the circuit will be operating in the linear transfer region during these measurements, a small capacitor (0.1 μF) on the output of the MECL circuit will eliminate any possible oscillation which could cause distorted readings.

DC transfer curves for circuits with internal feedback (such as the MECL master-slave flip-flops) cannot be measured. However, threshold points can be determined by measuring the input voltage at which switching occurs. This is commonly done by putting a ramp signal on the circuit input and observing the point at which the circuit switches with an oscilloscope.

Noise margin is a measure of the protection against adverse operating conditions built into MECL. Noise margin is specified as the voltage difference between the specified input thresholds ($V_{IHA\ min}$ or $V_{ILA\ max}$) and the guaranteed output thresholds ($V_{OHA\ min}$ or $V_{OLA\ max}$). As shown on the device data sheet the noise margin is 125 mV for a HIGH output logic level and 155 mV min for a LOW output logic level.

The noise margin values are found by calculating the difference between V_{IHA} and V_{OHA}, and between V_{ILA} and V_{OLA}, respectively. Further information may be found in reference 1 or 2. By setting the threshold voltages by means of a power supply, and using the same test fixture employed to measure the transfer characteristics, the output levels can be measured and noise margins calculated.

Propagation delays are measured by connecting a test circuit as shown in Figure 1. For all MECL circuits propagation delay is measured from the 50% amplitude point on the input signal to the 50% point on the output signal. Input signal levels for ac testing MECL 10,000 are specified in the data sheets as +1.11 Vdc for a HIGH level, and +0.31 Vdc for a LOW level. The input signal rise and fall times are set at 2.0 ns with a 20% to 80% measurement. This puts the 50% point at +0.71 volt, equal to the MECL 10,000 internal bias voltage V_{BB} when V_{CC} is at +2.0 volts.

*excepting military temperature range parts.

If a sampling oscilloscope with a digital readout is used, the test circuit waveforms for an OR gate function will look like Figure 4. The intensified zone on the waveform

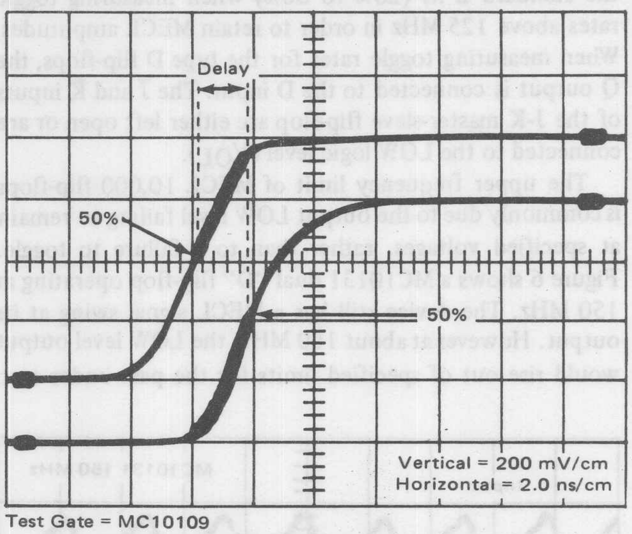

FIGURE 4 – MECL 10,000 Propagation Delay

shows the time interval of measurement – about 2 ns for the device under test. When a digital readout is not used, the delay time is determined from the scope traces by visual methods.

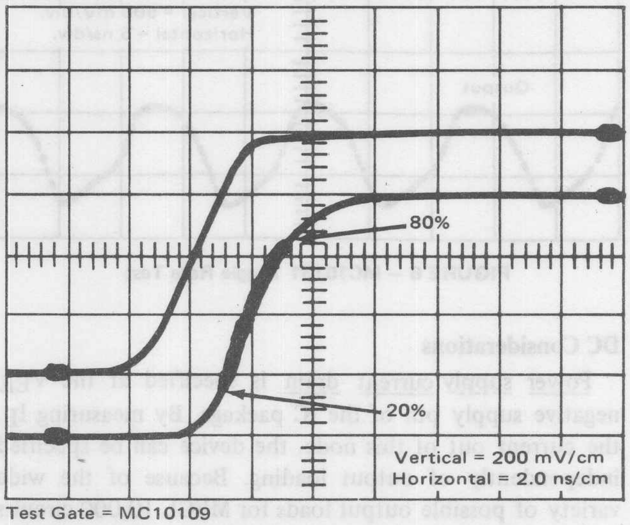

FIGURE 5 – MECL 10,000 Rise Time

Rise-time and fall-time testing is identical to propagation delay measuring except that the output waveform is measured for slope. With MECL 10,000 the output is specified from the 20% to the 80% points. The other MECL families are specified between 10% and 90%. Because of the designed-in rounding of the upper 20% of a MECL 10,000 waveshape, the 10% to 90% waveform is difficult to measure accurately. However, the 20% to 80% time is representative of the slope during the active transfer region of the MECL circuit input.

A typical rise-time test waveform for a MECL 10,000 circuit is shown in Figure 5. The intensified trace is shown for a 20% to 80% test and is approximately 2 ns. The 10% to 90% rise time would be about 3.2 ns.

Flip-flop toggle rates are measured by connecting a high speed pulse generator to the clock input. It may be necessary to decrease the pulse generator signal edge from the standard 2 ns (20% to 80%) when measuring toggle rates above 125 MHz in order to retain MECL amplitudes. When measuring toggle rates for the type D flip-flops, the $\overline{Q}$ output is connected to the D input. The $\overline{J}$ and $\overline{K}$ inputs of the J-K master-slave flip-flop are either left open or are connected to the LOW logic level (V_{OL}).

The upper frequency limit of MECL 10,000 flip-flops is commonly due to the output LOW level failing to remain at specified voltages, rather than to a failure to toggle. Figure 6 shows a MC10131 dual "D" flip-flop operating at 150 MHz. The device still has a MECL signal swing at its output. However at about 160 MHz, the LOW level output would rise out of specified limits for the part under test.

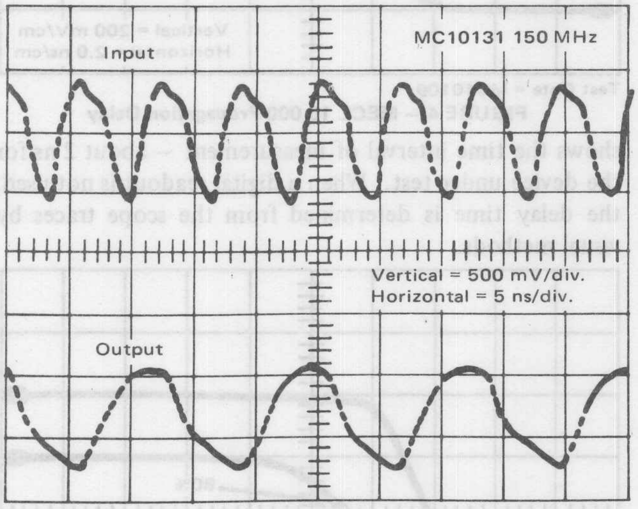

FIGURE 6 – MC10131 Toggle Rate Test

DC Considerations

Power supply current drain is specified at the V_{EE} negative supply pin of the IC package. By measuring I_E, the current out of this node, the device can be specified independently of output loading. Because of the wide variety of possible output loads for MECL 10,000 circuits in system operation, it is impossible to specify power for every possible loading situation. The power supply current drain defines power requirements for the logic current switches and bias drivers in the package. When calculating system power it is necessary to add power due to input current drain and output loading, to the specified power for the package based on $P_D = I_E \times V_{EE}$.

Input current requirements for a MECL 10,000 part depend on the use of the input. The basic specification of 265 μA (maximum) applies for a fan-in of one gate load. The input current for a HIGH logic level is divided between the internal input pulldown resistor and the current switch input of a MECL circuit. Since only one pulldown resistor is required for a multiple fan-in pin, input current is not directly proportional to the number of current switches being driven in the package. For example, a four-gate strobe input in the MC10101 is specified at a maximum of 550 μA, a value only slightly more than two single gate inputs.

Input current requirements for a LOW level logic signal is less than for the HIGH level. The signal must still drive the internal input pulldown resistor, but the MECL switch input current consists of only a small amount of reverse leakage current when the input transistor is off.

Other circuit parameters often tested but not specified on the data sheets include output impedance and input capacitance. The dc output impedance is measured by changing the loading of the MECL output and observing the change in output voltage. The change in output voltage divided by the change in output current gives an output impedance of about 7 ohms for a typical MECL 10,000 circuit.

Input capacitance is more difficult to measure and normally requires a time domain reflectometer, a stripline reflectometer setup, or a current probe transformer (e.g., Tektronix CT-1, or equivalent). Testing has shown the typical input capacitance for MECL 10,000 gate circuits to be about 2.9 pF. The details needed for testing input capacitance may be found in Chapter 7 of the MECL System Design Handbook, referenced at the end of this note.

High Speed Testing

High speed testing techniques are normally used when a large volume of parts must be checked. High speed testing usually involves a machine which automatically checks a part for all the tested parameters without manually setting controls for each test. To take advantage of the speed of such machines it is normally undesirable to provide air flow or to wait for the circuit under test to temperature stabilize*. Considering that the test will be performed with the chip temperature near 25°C, it may be necessary to compensate the test parameters so the circuit will be within the specifications at stabilized operating conditions. Each MECL 10,000 circuit is designed to have the same input and output logic levels at the specified ambient of 25°C and 500 linear feet per minute air flow, regardless of power levels within the package. Therefore, the amount of compensation for high speed testing will depend on the power dissipation of the circuit.

Junction temperature T_J (under normal system operation) may be calculated:

$$T_J = P_D \, \theta_{JA} + T_A,$$

where θ_{JA} is the thermal resistance of the package (junction to ambient) about 50° C/W with 500 linear feet per minute air flow, and T_A is the ambient temperature. From the above equation, the junction temperature for a 200 mW part will be 35°C for a 25°C ambient temperature. This results in a stabilized junction temperature 10°C above the high speed test temperature for the 200 mW part.

*In about 10-15 sec., the device will have reached 80% of equilibrium. A 5-minute delay prior to making measurements, is more than adequate to insure full stabilization.

For MECL 10,000 parts, the change in the HIGH logic level, V_{OH}, is about 1.4 mV/°C and the change in the LOW logic level, V_{OL}, is about 0.5 mW/°C. Using the above 200 mW part, the 10°C lower junction temperature would shift V_{OH} 14 mV more negative and V_{OL} 5 mV more negative.

The input signal requirements are controlled by the temperature tracking of the respective output levels. V_{IH} levels will be shifted by the V_{OH} factor of 1.4 mV/°C and the V_{IL} level will be shifted by the V_{OL} factor of 0.5 mV/°C. When calculating the power to determine thermal shifting, it is also necessary to include the power dissipated by the output devices, e.g. [P_{output} = (No. of outputs) × ($I_D \times V_D$)].

It can be seen that these small changes in output levels would not keep the majority of parts from meeting specified performance if the test parameters are not altered. There is sufficient noise margin built into the circuits, plus a safety factor between Motorola final test specifications and the limits specified on MECL 10,000 data sheets, to overcome most test environment differences. However, some of the more complex MSI functions can dissipate around 600 mW. If these parts are tested without allowing the circuits to temperature stabilize, the logic levels may be sufficiently different to offset incoming test yields. In such a case, test level compensation should be considered.

Test Equipment

The main factor when selecting test equipment to work with MECL circuits is the high frequency capability of the test units. Pulse generators must have 50-ohm output drive. In addition, edge speed and offset must be MECL compatible. The 50-ohm drive is characteristic of virtually all high speed pulse generators. It is necessary to drive coaxial cables or other 50-ohm lines at high speed without signal distortion due to improperly terminated lines.

When testing MECL 10,000, a pulse generator should be set to 2.0 ns 20% to 80% edge speeds. The offset and amplitude should be adjustable to MECL logic levels. When driving a test fixture with a +2.0 Vdc supply on V_{CC}, the logic levels are +1.11 volts and +0.31 volt. It is also desirable to have the pulse generator capable of interfacing with MECL 10,000 operating with grounded V_{CC}. In this mode of operation the logic levels are typically −0.89 volt and −1.69 volts.

The selection of an oscilloscope depends on where the 'scope is to be used. The requirements are different for component evaluation and for system checkout. A good sampling scope is normally needed for device qualification because of the accuracy requirements entailed when measuring 100 picosecond increments. However, 500 MHz real time 'scope will give good results. All of these 'scope can be purchased with 50-ohm inputs which are compatible with MECL 10,000 test fixtures.

When performing system checkout, a real time 'scope of at least 150 MHz bandwidth is normally adequate. While edge speed will be degraded by this bandwidth, and while some overshoot and ringing may be attenuated, the speed is sufficient to determine that the circuits are operating properly. Using oscilloscopes with less than 100 MHz bandwidth is not recommended because such 'scope will seriously degrade the presentation of the MECL signals and may not see signals which affect operation of the MECL circuits.

It is also possible (and usually desirable) to use high impedance probes during system checkout. However, the ground reference should be connected to the probe tip and kept near to the point under test. Having a separate ground wire from the 'scope to the system (in place of a probe ground) will cause distorted readings because of the length of the ground run in relation to signal speed.

Other types of laboratory equipment, such as power supplies and voltmeters, have no special performance requirements imposed on them when used for MECL testing. The ac response time of the power supply is not especially critical because of the large amount of capacitor bypassing used on a MECL test fixture. DC voltmeters are normally used to measure output logic levels during dc testing, because of their higher accuracy than an oscilloscope.

Conclusion

Testing MECL 10,000 circuits requires special techniques to insure accurate results. However, if these techniques are practiced, testing high speed integrated circuits is no more difficult than testing lower speed parts. The use of a transmission line system greatly improves the accuracy and consistency of high speed digital testing. By using test techniques consistent with Motorola's component evaluation and final test, the circuit user can obtain test results which correlate well with Motorola's data sheet and other test information.

References

1. "MECL System Design Handbook," Motorola Inc., 1971.
2. "MECL Integrated Circuits Data Book," Motorola Inc., 1971.

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