MOSTEK®

MD SERIES MICROCOMPUTER MODULES

Operations Manual

MDX-FLP FLEXIBLE DISK DRIVE CONTROLLER BOARD

OPERATIONS MANUAL

FOR

MDX - FLP

MK77652

Publications Number 79639

TABLE OF CONTENTS

TABLE OF CONTENTS (CONTD)

TABLE OF CONTENTS (CONTD)

TABLE OF CONTENTS (Contd.)

TABLE OF CONTENTS (Contd.)

LIST OF FIGURES

LIST OF TABLES

SECTION 1

GENERAL DESCRIPTION

1-1. INTRODUCTION

The MD series and the STD BUS were designed to satisfy the need for low cost OEM microcomputer modules. The STD BUS uses a motherboard interconnect system concept and is designed to handle any MD Series card in any slot. The modules for the STD Bus are a compact 4.5 x 6.5 inches providing for system partitioning by function (RAM, EPROM, I/O). This smaller module size makes system packaging easier, while increasing MOS-LSI densities provide high functionality per module.

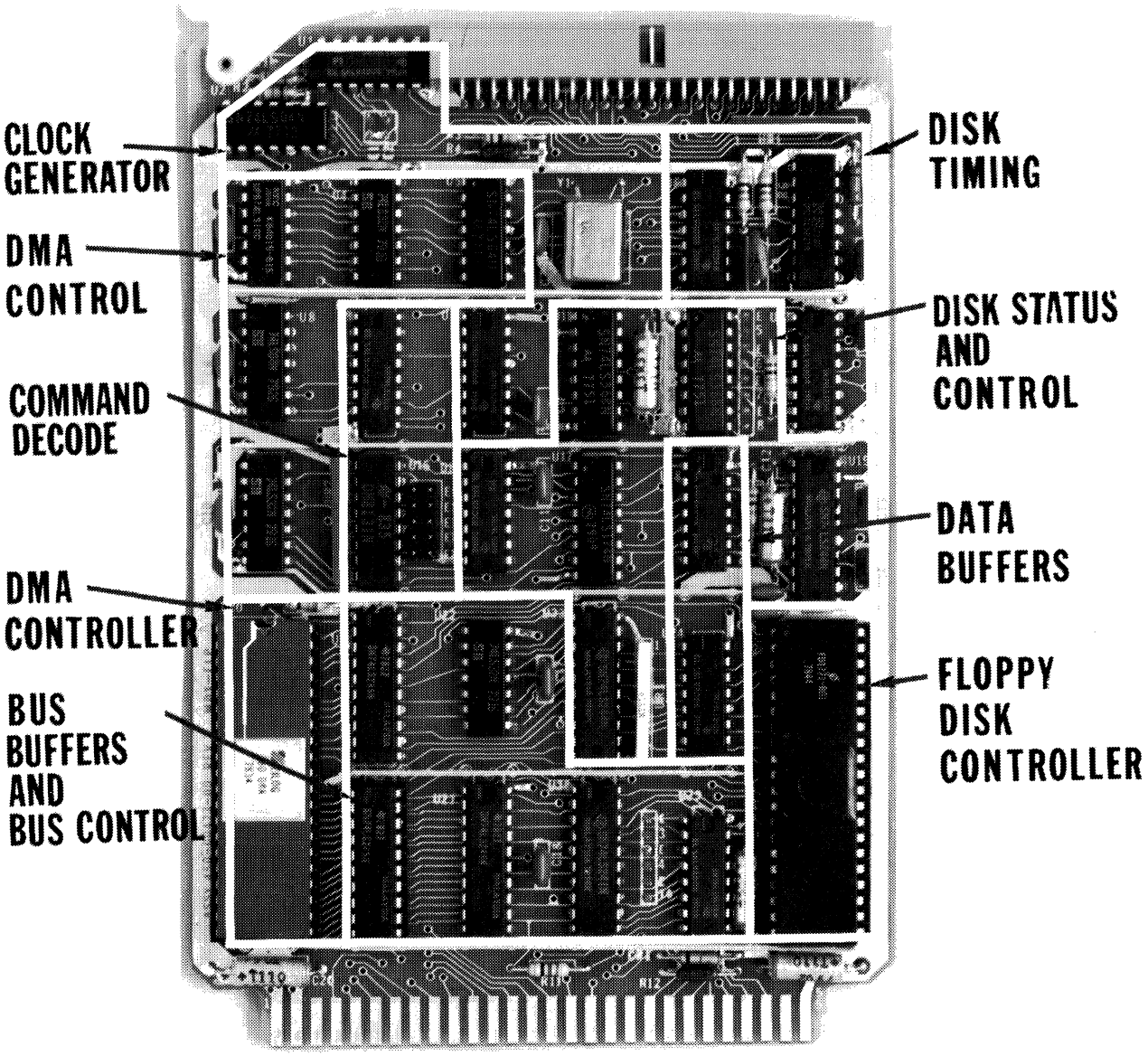
1-2. FEATURES

The MDX-FLP board (shown in Figure 1-1) embodies all required controlling-/formatting/interfacing logic between the STD-Z80 BUS and 1 to 4 floppy disk drives. The board is based around the Western Digital 1771 controller chip and MK3883 DMA controller, and offers the following features:

- 1 to 4 drives; 4 software controlled selected lines.
- 5" or 8" drives, single or dual sided, jumper selectable.
  All drives connected to one MDX-FLP board must be the same type.
- Single density operation
- Soft sector operation including variable length sectors.
- Compatibility with IBM 3740 or other formats.
- Single-sector, multi-sector or full track data transfers.
- Automatic track seek with verification capability.
- Diskette initialization/formatting capability.
- Software programmable step rate, head settling, and engage times.
- DMA or programmed data transfer.
- Interrupt-driven or polled operation.
- Automatic CRC checking on Read operations, CRC generation on Write.

- 8 inch drives supported under FLP80-DOS and MITE-80 software, 5 inch under MITE-80.
- Port addresses jumper-selectable to a block of 8 anywhere in the address space.
- 2.5 MHZ operation (system clock).
- Provision for DMA daisy chain operation (simultaneous operation of multiple DMA devices requires on-board jumper and backplane mod).

FIGURE 1-1. MDX-FLP BOARD



1-3. FUNCTIONAL BLOCK DESCRIPTION

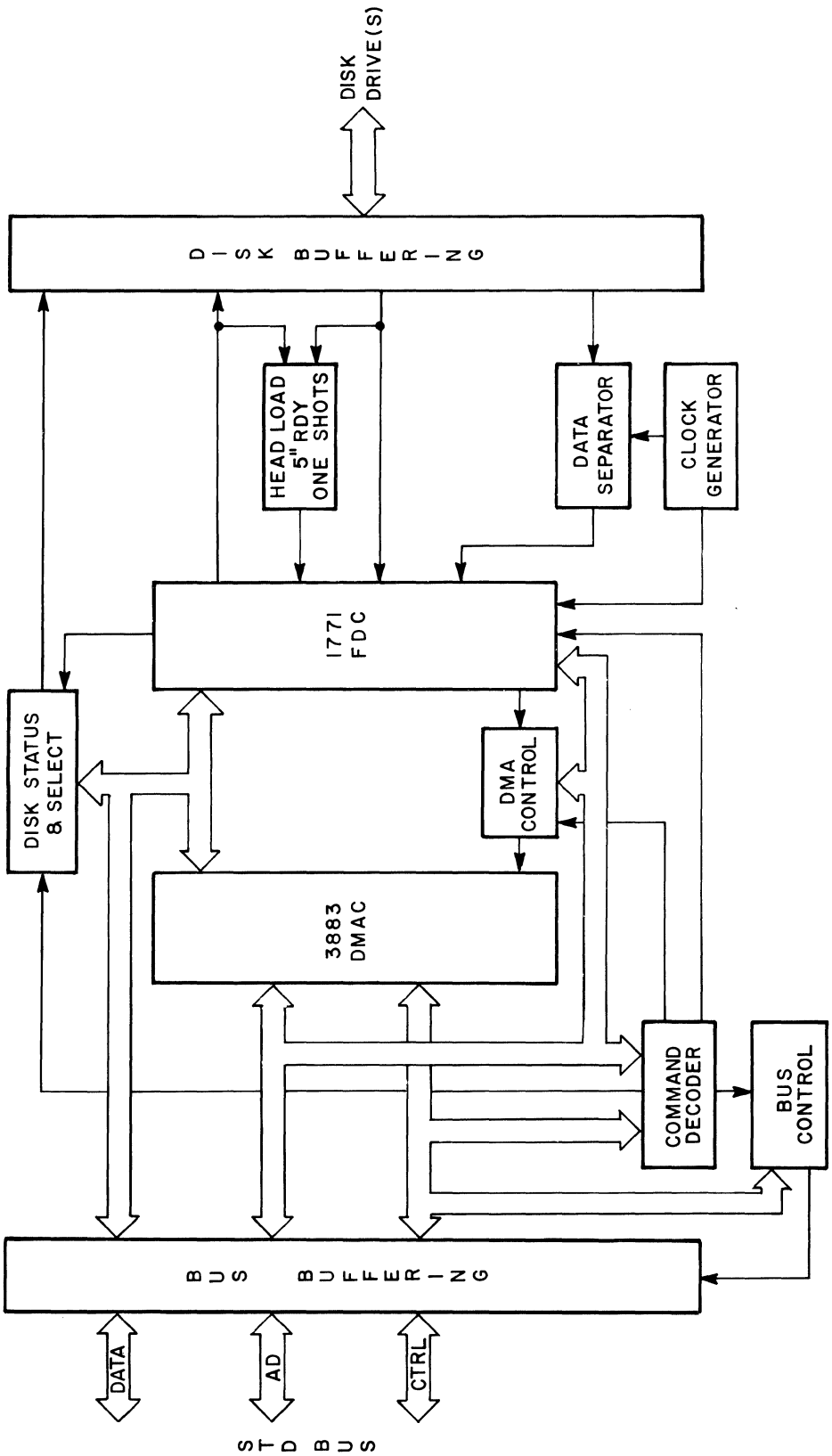
Figure 1-2 illustrates the functional blocks of the MDX-FLP. The basic blocks consist of:

- Bus Buffering
- Command Decode
- Bus Control
- Disk Status + Control
- 3883 DMA Controller
- DMA Control
- 1771 Floppy Disk Controller
- Clock Generator
- Data Separator
- Head Load, 5" Ready One Shots
- Disk Buffering

1-4. STD-Z80 BUS BUFFERS

This circuitry includes drivers, receivers, and tranceivers which perform no active logic function. The bus buffers consist of three 74LS245 transceivers, one 74LS241 transceiver, two 74LS242 inverting transceivers, and miscellaneous stages of LS04, LS125, LS244, and LS367 drivers and receivers. Bi-directional buffers are used for the Data Bus as well as the address bus and the control signal bus. The Data Buffers are bi-directional since data must be transmitted to and from the board. Since the MK3883 must talk to the system memory during data transfers, all sixteen bits of the address buffer are capable of driving the address bus. The lower eight bits of the address bus also receive data in order to address the MDX-FLP board. Several of the control signals normally received by the board are driven on to the bus during DMA transfers. The 74LS241 is connected in such a way as to allow bi-directional capability on these control lines.

FIGURE 1-2. MDX-FLP BLOCK DIAGRAM



1-5. COMMAND DECODER

This circuitry recognizes commands for the 3883 DMAC, 1771 FDC, and Disk Status and Select section, and generates appropriate control signals for these elements. Inputs include the 8 low-order address lines, $\overline{IORQ}$, $\overline{RD}$, and $\overline{WR}$. Outputs include $\overline{CS}$, $\overline{RE}$, and $\overline{WE}$ for the FDC, Chip Enable for the DMAC, load clock for the Disk Select Register, and enables for Disk Status.

The Command Decoder consists of the 8131 digital comparator, 74LS138 demultiplexer, 74LS32 gates, and the address straps. The digital comparator compares the address strapped at J3 with bits A3 thru A7 of the address bus. If A7 thru A3 contain the selected address, the output of the 8131 goes low. This recognition with A2 High (1) forms Chip Select for the 1771. Address recognition with A2 Low (0) enables the 74LS138 to decode the lower two address lines, and produce the low-active signals $\overline{PORT\emptyset, 2,3}$. $\overline{PORT\emptyset}$ is the Chip Enable for the 3883 DMAC. The address definitions for the MDX-FLP Board are shown in TABLE 1-1.

After this address-dependent circuitry has had time to settle, the processor (or DMAC) generates the low-active $\overline{IORQ}$, $\overline{RD}$, and WR signals. The low active signals $\overline{IORD}$ ($\overline{IORQ}$ and $\overline{RD}$) and $\overline{IOWR}$ ($\overline{IORQ}$ and $\overline{WR}$) form the Read Enable and Write Enable inputs to the 1771 FDC. ($\overline{IORD}$ and $\overline{PORT2}$) enables the "board status" onto the Data Bus; ($\overline{IOWR}$ and $\overline{PORT3}$) latches the contents of the Data Bus into the Drive Selection register; ($\overline{IORD}$ and $\overline{PORT3}$) enables the contents of the Drive Selection Register to be read back on the Data Bus.

TABLE 1-1.
BOARD ADDRESS DEFINITION

HEX CODE	DEFINITION
X0/X8	DMA Controller Chip
X1/X9	Unused
X2/XA	MDX-FLP Board Status
X3/XB	Drive Select Status and Control
X4/XC	Floppy Controller Chip Status/Command Register
X5/XD	" " " Track Register
X6/XE	" " " Sector Register
X7/XF	" " " Data Register

1-6. BUS CONTROL

This circuitry can be viewed as an extension of the command decoder, and comprises logic to control the bus buffering circuitry with the proper direction and timing for various operations. Inputs include $\overline{\text{IORD}}$, $\overline{\text{1771 Chip Select}}$, and address recognition from the Command Decoder; bus control signals $\overline{\text{WR}}$, $\overline{\text{INTAK}}$, $\overline{\text{PCI}}$, $\overline{\text{BUSAK}}$; and $\overline{\text{DMAC}}$ outputs $\overline{\text{IEO}}$ and $\overline{\text{BUSRQ}}$. Outputs include Direction Control for the various bus transceivers, and an Enable signal for the Data Bus transceivers.

The LS242 inverting transceivers which invert the internal data bus for the 1771 FDC normally receive the internal data bus and drive it toward the 1771. This direction is reversed only for a Read operation from the 1771 ($\overline{\text{IORD}}$ and $\overline{\text{1771 Chip Select}}$ both true/low).

The LS245 Address Bus tranceivers and LS241 tranceiver for the control signals $\overline{\text{WR}}$, $\overline{\text{RD}}$, $\overline{\text{IORQ}}$, $\overline{\text{MEMRQ}}$ normally receive from the STD-BUS and drive into the board. This direction is reversed when the 3883 DMAC is controlling the STD-BUS (bus signal $\overline{\text{BUSAK}}$ and 3883 output $\overline{\text{BUSRQ}}$ both low/true).

Direction control for the LS245 Data Bus tranceiver "normally" receives from the STD-BUS and drives the internal data bus. This direction is reversed, to drive the STD-BUS data lines, in any of three situations:

1. When the DMAC is controlling the bus and generates a Write signal (bus signal $\overline{\text{BUSAK}}$ and 3883 outputs $\overline{\text{BUSRQ}}$ and $\overline{\text{WR}}$ all low/true).

2. When the Processor (or DMAC) is reading an I/O Port on the board (Address Recognition and $\overline{\text{IORD}}$ both low/true).

3. When an interrupt vector is to be sent from the DMAC to the Processor (bus signal $\overline{\text{INTAK}}$ low/true, bus signal PCI high/true, 3883 output IEO low/false).

Last, a tri-state enable signal is required for the 74LS245 Data Bus Transceiver during DMAC control of the bus. The LS245 is always enabled when the on-board DMAC is not in control of the bus (when BUSAK and/or BUSRQ are high/false). When the DMAC is in control of the bus, the LS245 is enabled only during a Read or Write pulse (RD or WR low/true). This is to prevent the LS245 from driving spurious data onto the internal data bus between the read and write portions of a DMA cycle, and overriding the data bus latches in the DMAC.

1-7. DISK STATUS & SELECTION

This section consists of an LS174 hex flipflop which latches the drive selection from the data bus, and an LS244 dual quad tri-state gate plus one LS125 tri-state gate, to drive the drive selection or the "board status" onto the data bus. "Board status" consists of the E3 and E4 jumpers plus the INTRQ signal from the 1771. Gating signals are described in the COMMAND DECODER section. The significance of the various data bits is described in the Theory of Operation section.

1-8. 3883 DMA CONTROLLER

The basic functions of the DMA controller in the MDX-FLP Board are four in number:

1. The DMAC receives and interprets write commands on the Data Bus from the processor for setup and enabling.
2. When the 3883 is enabled and the RDY signal from the DMA control section comes true, the 3883 requests bus control from the processor. When that bus control is granted, it initiates a Read cycle on the bus, then a Write cycle on the bus. This may be a Read from the 1771 and a Write to system RAM, or a Read from system RAM and a Write to the 1771, depending on the direction of transfer with the disk. It then relinquishes bus control back to the Processor until RDY becomes true again.

3. If the DMAC was programmed for interrupt during setup, then when the number of DMA cycles programmed during setup has occurred, the DMAC requests interrupt to the processor. When the interrupt is acknowledged, it places the interrupt vector programmed during setup on the Data Bus.
4. It interprets Read commands from the Processor and sends back such information as its status, number of bytes transferred, and ending addresses.

Further information on the 3883 DMA Controller is presented in Paragraphs 3-1 thru 3-34.

1-9. DMA CONTROL

This logic generates the RDY and $\overline{\text{CE/WAIT}}$ inputs for the DMA Controller. RDY must be programmed as Active High during DMA setup. RDY is simply the OR of the 1771 FDC outputs Data Request (DRQ) and Interrupt Request (INTRQ). The 1771 clears DRQ when it is read from or written into as part of the DMA cycle initiated by RDY. INTRQ is not cleared by the DMA cycle. This allows the 3883 to generate an interrupt (which it knows only as "block complete") at the time of 1771 completion, if the DMAC is programmed for one more than the number of bytes to be transferred (e.g. 129). To enable interrupt at the completion of a non-transfer operation, the DMAC can be programmed for the minimum number of bytes (2). Note that this implementation of RDY prevents "lockup" of the DMAC when the 1771 does not present the expected number of Data Requests. Due to package constraints, the designers of the 3883 DMAC were forced to combine the Chip Enable function during Processor Read/Write of the DMAC, with the WAIT function for slow devices during DMA bus control, onto a single multiplexed pin. The 3883 should be programmed for "multiplexed $\overline{\text{CE/WAIT}}$" during setup. This circuitry gates the $\overline{\text{PORTO}}$ signal from the Command Decoder onto 3883 pin $\overline{\text{CE/WAIT}}$ when the $\overline{\text{BUSAK}}$ signal is high/false, and gates the bus signal $\overline{\text{WAIT}}$ onto the pin when $\overline{\text{BUSAK}}$ is low/true.

1-10. FD1771 FLOPPY CONTROLLER

The FD1771 is the heart of the MDX-FLP Board. All accesses to the Disc units, aside from drive/side selection, are made through this chip. The floppy controller chip furnishes timing pulses and control signals as well as data recognition and formatting. Data for initialization/formatting of the medium must be provided by the Z80 program. However, once the medium is initialized the 1771 controller performs sector and track recognition automatically. Selection between mini or regular floppy disc units requires changing jumper options as described in Section 3-88. For detailed description of operation and programming options of the 1771 controller, refers to Paragraphs 3-35 thru 3-83.

1-11. Clock Generator

This circuitry consists of a crystal-controlled 4MHZ oscillator, one package of LS74's for frequency division, and two jumpers to configure the clock frequency for 8" or 5" drive operation. Outputs are provided to the Data Separator and the 1771 FDC, as follows:

DRIVE:	8"	5"
Data Separator (LS193) Clock	4MHZ	2MHZ
1771 Clock	2 MHZ	1 MHZ

1-12. Data Separator

This circuitry transforms the RD DATA signal from the drive into the CLK and DATA inputs of the 1771, which is operated in "external separator" mode. The circuitry consists of an LS221 one-shot, one LS193 counter, 2 LS02 gates, and jumper E5. Every negative/low-going transition on RD DATA fires the one shot, the

pulse width of which should be 250 ns for 8" (E5 in) and 500 ns for 5" (E5 removed). This pulse is presented in positive form to either the CLK or DATA pin of the 1771, depending on the state of the D (high order) stage of the LS193 counter. The same pulse loads the value "D011" into the LS193 (where D is the previous value of the D stage), and freezes counting for the duration of the pulse. When the counter is released, it is counted down from the Clock Generator at a frequency of 1/16 the nominal bit cell time (clock and data). The net result is to present the next $\overline{\text{RD DATA}}$ transition to the "opposite" 1771 input if it occurs between 1/4 and 3/4 of the nominal bit rate, to the same input if it occurs between 3/4 and 5/4 of the bit rate, etc. Note that the 1771 pin designations CLK and DATA are arbitrary, and actual "clock" transitions in the recorded sector may be presented at DATA and vice-versa; the 1771 figures out which is which.

1-13. HEAD LOAD, 5" READY ONE-SHOTS

This circuitry includes 2 74LS123 one-shots (one package) and three jumpers. The Head Load one-shot time should be 35 msec for 8" drives (jumper E8 in) and 70 msec for 5" drives (E8 removed). The one-shot is triggered on a positive-going edge of the HLD output of the 1771, which causes the head to start loading on the drive. Its low-pulse output is connected to the high-active HLT (Head Loaded) input of the 1771. Thus, the one-shot determines the time for the head to load and stablize.

NOTE: This circuit does not provide for proper head load settling when switching drives unless the programming precautions described in the Theory of Operations section are followed. 8" drives provide a Drive Ready signal for connection to the RDY input of the 1771 FDC; 5" drives do not. Accordingly, the 5" Ready one-shot synthesizes a Ready signal from the Index hole pulse. A negative-going edge on the Index line (re-) triggers the one-shot, whose pulse length is longer than the rotational time of the medium. Thus the one-shot will stay triggered as long as the medium is going around. For a 5" drive, jumper E6 should be "in", E7 removed, so that the Q output of the one-shot provides RDY to the 1771.

1-14. DISK BUFFERING

This circuitry includes drivers and receivers for the signals to and from the drives. LS244 receivers plus 150 ohm termination resistors to + 5V are used for the input signals $\overline{\text{RD DATA}}$, $\overline{\text{INDEX}}$, $\overline{\text{TRACK 0}}$, $\overline{\text{WRITE PROTECT}}$ and $\overline{\text{RDY}}$. LS368 inverters are used to drive the output signals $\overline{\text{STEP}}$, $\overline{\text{WRITE DATA}}$, $\overline{\text{WRITE GATE}}$, $\overline{\text{DIRECTION}}$, $\overline{\text{HEAD LOAD}}$, DS1, DS2, DS3, DS4, and SS.

SECTION 2

INSTALLATION

2-1. TYPICAL DISK UNIT SETUP

While the MDX-FLP board is compatible with a number of manufacturer's floppy disk drives (see ¶ 4-16), installation data can only be meaningfully given for a particular drive. The Shugart SA800 is used as an example in this section. Tables 2-1 and 2-2 give the AC and DC requirements for a single SA800 Shugart drive unit. Table 2-3 describes the connectors necessary for hookup to the MDX-FLP Board. Figure 2-1 illustrates a typical system inter-connect diagram for the MDX-FLP, power supplies, and disc drives.

2-2. D.C. POWER

The D.C. Power is connected to the disc drives through connector J5 on the SA800. J5 (see figure 2-2a) is mounted on the non-component side of the PCB and is located below the AC motor capacitor of the disk drive unit. J5 is a six pin AMP Mate-N-LOK connector, P/N 1-380999-0. The recommended mating connector (P5) is AMP P/N 1-480270-0 utilizing AMP pins P/N 60619-1. J5 pins are labeled on the component side of the PCB with pin 5 located nearest J1/P1. Figure 2-2a illustrates J5 connector as seen on the drive PCB from non-component side.

2-3. A.C. POWER

A.C. Power is connected to the SA800 through connector J4. J4 (see figure 2-26) is mounted on the AC motor capacitor bracket and is located just below the capacitor of the disk drive unit. J4 connector is a three pin connector, AMP P/N 1-480305-0, with pins P/N 60620-1. The recommended mating connector (P4) is AMP P/N 1-480303-0 or 1-480304-0, both utilizing pins P/N 60619-1. Figure 2-2b

illustrates J5 connector as seen from the rear of the drive. The logic interconnect is made from J2 of the MDX-FLP through a 50 pin cable to J1 of the SA800 as shown in figure 2-3.

2-4. The AC, DC power for the flexible disk drives is shown for a single SHUGART SA800 drive in the following tables. Refer to the SA800 or SA850 DISKETTE STORAGE DRIVE OEM MANUAL for more details.

TABLE 2-1.
SHUGART SA800 AC REQUIREMENTS

SHUGART P4 PIN	60Hz		50Hz	
	115V (Standard)	208/230 V	110 V	220 V
1	85-127 VAC	170-253 VAC	85-127 VAC	170-253 VAC
2	Frame Gnd	Frame Gnd	Frame Gnd	Frame Gnd
3	85-127 Rtn	170-253 V Rtn	85-127 V Rtn	170-253 V Rtn
MAX CURRENT	0.5 Amps	0.4 Amps	0.6 Amps	0.4 Amps
FREQ TOLERANCE	±0.5 Hz		±0.5 Hz	

NOTE: Assure that the proper model has been selected to correspond to input voltage requirements.

TABLE 2-2

SHUAGRT SA800 DC REQUIREMENTS (EACH DRIVE)

P5 PIN	DC VOLTAGE	TOLERANCE	CURRENT	MAX RIPPLE (p to p)
1	+24 VDC	±1.2 VDC	1.7 A Max 1.3 A Typ	100 mv
2	+24 V Return			
3	- 5 V Return			
4	- 5 VDC	±0.25VDC	0.07 A Max 0.05 A Typ	50 mv
	Optional -7 to -16 VDC (Cut Trace 'L')	NA	0.10 A Max 0.07 A Typ	NA
5	+ 5 VDC	±0.25 VDC	1.0 A Max 0.8 A Typ	50 mv
6	+ 5 V Return			

TABLE 2-3.
MDX-FLP CONNECTORS

CONNECTOR	NO. OF PINS	CENTER (IN)	MATING CONNECTOR
BUS (P1)	56	0.125	Printed Circuit Viking 3VH28/1CE5 Wire Wrap Viking 3VH28/1CND5 Solder Lug Viking 3VH28/1CN5
DRIVE INTERCONNECT (J2)	50	0.100	ANSLEY 609-5000 W/O Strain Relief ANSLEY 609-5001 W Strain Relief

FIGURE 2-1. SYSTEM INTERCONNECTION DIAGRAM

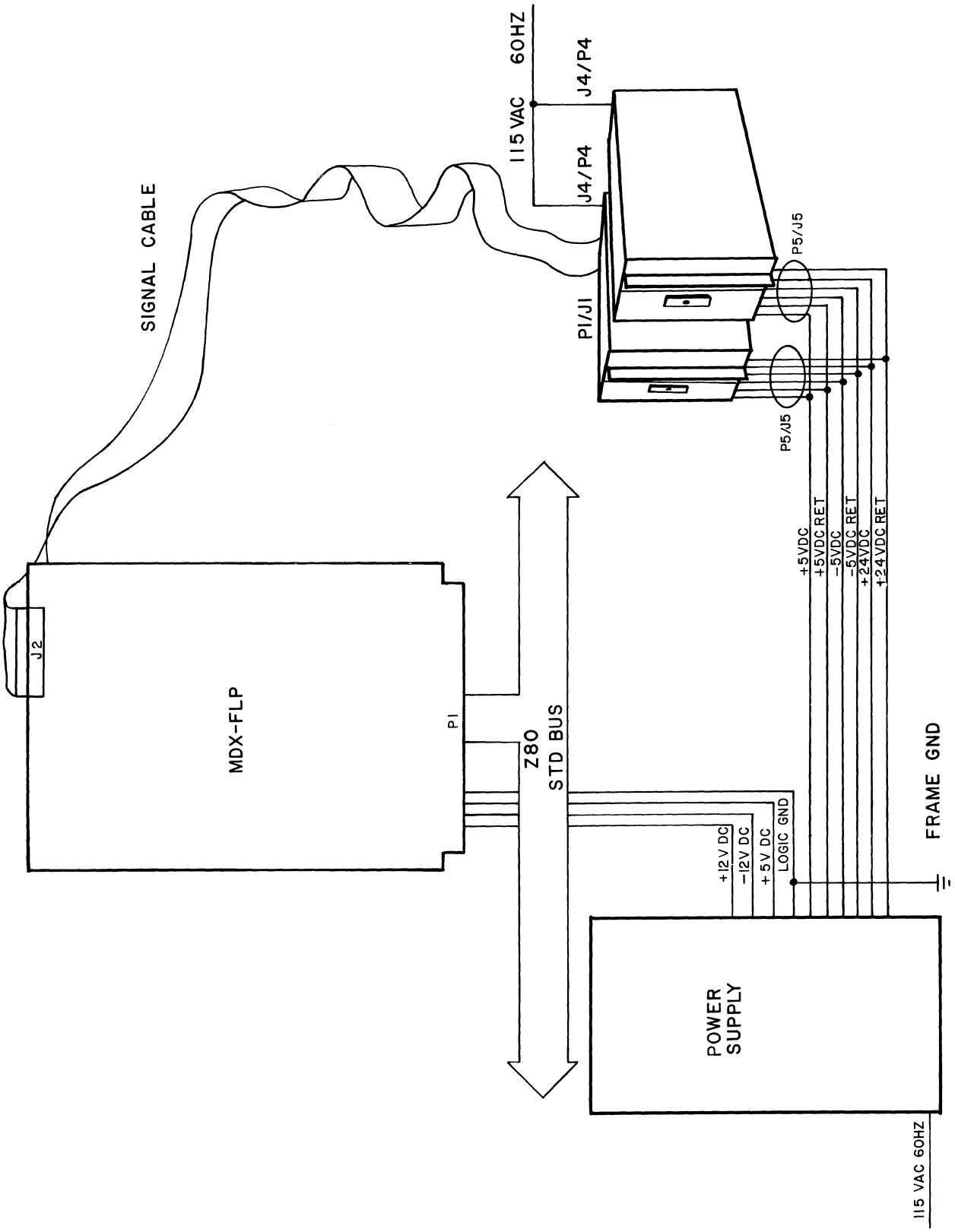


FIGURE 2-2a. SA800 J5 CONNECTOR

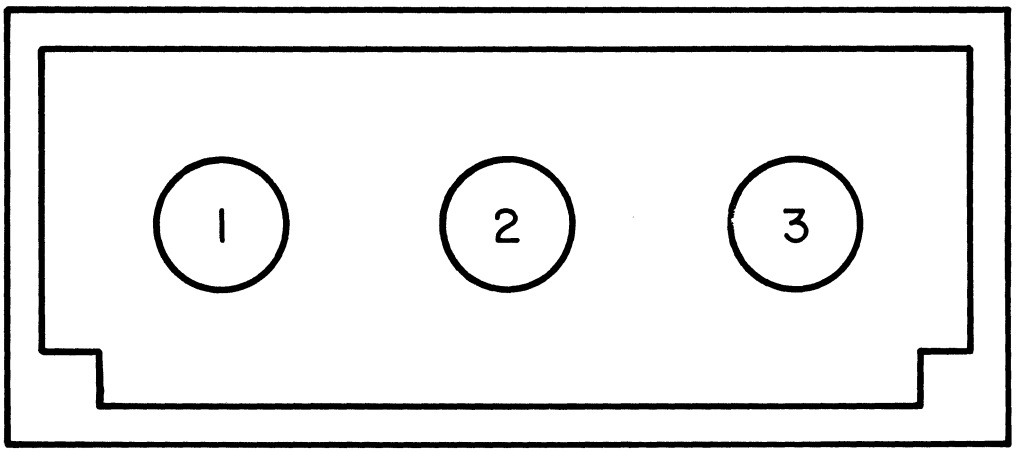


FIGURE 2-2b. SA800 J4 CONNECTOR

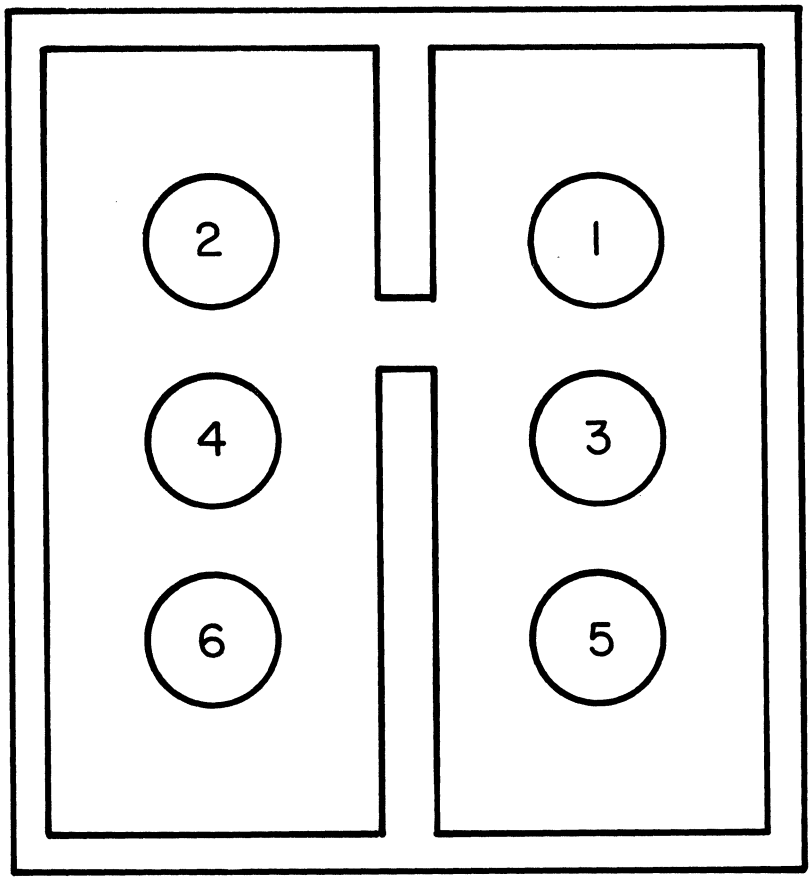
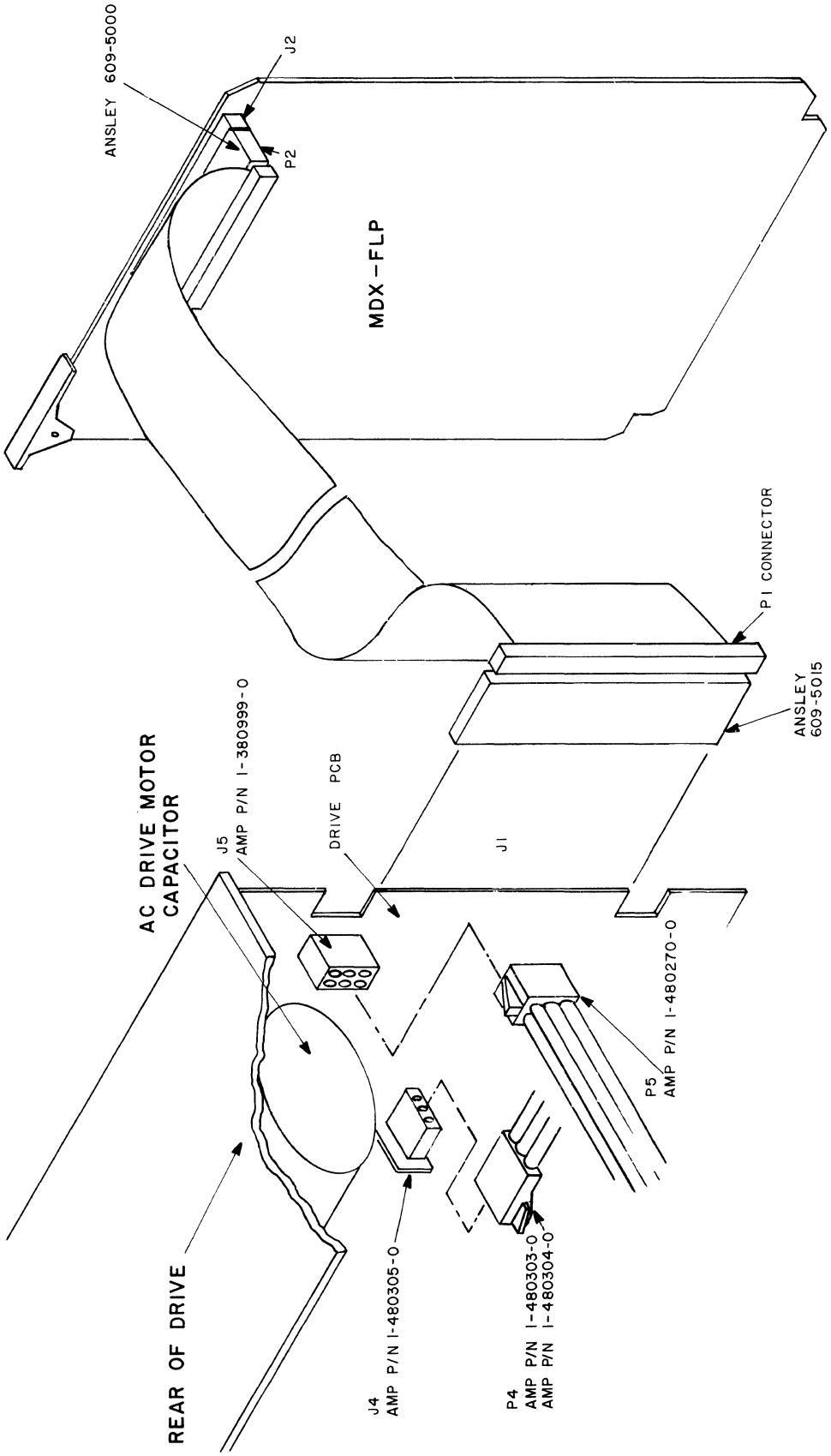


FIGURE 2-3. SA800 INTERFACE CONNECTORS



2-5. INITIAL CHECKOUT

The MDX-FLP board has been fully tested by MOSTEK prior to shipment. The following initial checkout procedure is simply a functional check of the board. If the board fails to perform any of the steps outlined, turn off the power, recheck the board hook up, and try the checkout procedure again. If the problem persists, contact MOSTEK for assistance.

2-6. UNPACKING

CAUTION Some of the integrated circuits in this assembly are high impedance MOS devices. Internal circuitry is included on each device to protect the inputs against damage due to static voltage; however, the assembly should be left in the conductive bag until ready for installation.

2-7. MINIMUM EQUIPMENT NEEDED

This check out procedure assumes the following minimum equipment available. For OEM applications with different CPU systems, principles will still apply.

1. A serial ASCII terminal i.e. TTY, Silent 700, or CRT.
2. MDX-CPU1, MDX-DEBUG, MDX-FLP
3. Power Supplies
   +12V @ 0.5 A
   + 5V @ 5.0 A
   -12V @ 0.5 A
   +24V @ 3.0 A

2-8. CONNECTIONS

Power should be supplied to the board per the following pin out:

POWER	CONNECTOR	PIN
+12V	P1	55
+ 5V	P1	1,2
GND	P1	3,4
-12V	P1	56

2-9. MDX-FLP CHECKOUT

Communication between the MDX-CPU1 and the MDX-FLP and MDX-DEBUG can be assured by executing the following tests. Throughout this manual the following symbol convention is used:

1. (CR) indicates CARRIAGE RETURN
2. ^ indicates CARAT or UP ARROW
3. ____ underline indicates portion of command entered by user as in:
   - M 5000 (CR) user entering command to display memory location 5000 followed by carriage return.
   - 5000 XX (CR) CPU1 responds with location 5000 and contents of location 5000, user enters carriage return. (XX as used here indicates current, unknown or don't care contents of memory location 5000)
4. a,b,c...u..xyz lower case letters used to indicate operands

Note that disk units may or may not be attached.

```
.P   E3(CR)
E3 XX FF^; Test for
E3 FF 00^; Communication
E3 E0 .  ; CPU1 to MDX-FLP

.P E2 (CR)   Check Status (READ ONLY)
```

E2 XX . If xx is FC, FD, FE, DC; It means:
FC = Single sided, no interrupt, Regular Drive (8")
FD = Double sided, no interrupt, Regular Drive (8")
FE = Single sided, interrupt, Regular Drive (8")
DC = Single sided, no interrupt, Mini Floppy (5")
Refer: to Paragraph 4-5 for further explanations
These are normal indications after a master clear condition

.P E5(CR)
E5 XX FF^
E5 FF ØØ^
E5 00 .
.P E6(CR)
E6 XX FF^
E6 FF ØØ^
E6 ØØ .
.P E7 (CR)
E7 XX FF^
E7 FF ØØ^
E7 ØØ .(CR)

The above three operations test communication to controller chip located within the MDX-FLP.

2-10. If the drive or drives are connected and a diskette is inserted, the following test can be performed.

.P E3 (CR)
E3 XX Ø1^Select Drive 1 (02 for Drive 2)
E3 E1 (CR)
E4 XX ØA^RESTORE (seek track 0) command*
E4 XX (CR)
E5 ØØ (CR) Track register should now contain zero
E6 XX (CR)

E7 XX 4C ^ Data register is loaded with desired track
E7 4C .
.P E4 (CR)
E4 04 1A ^ Head on disk unit should load and the drive should position to track 76.*
E4 XX 0A (CR) Head should restore to track zero.*

* An audible sound should be heard from the drive as it performs each task.

The above test checks the following items:

1. Selecting of a drive (Port E3)
2. Does a return to zero seek or restore.
3. Test Track Register for current position (zero after a restore).
4. Loads the data register with desired track location.
5. Does a head load and seek.

2-11. This test sets the Track Register with the current position of the Read/Write head and then sets the desired track value into the Data Register. The controller chip will update the Track register and issue stepping pulses to the selected drive in the appropriate direction until the contents of the Track register are equal to the contents of the Data Register; at which time motion stops.

2-12. Upon successful completion of the above tests, drive diagnostics may be run or operation can be attempted if no diagnostics are available.

SECTION 3

FUNCTIONAL DETAIL DESCRIPTION

3-1. Z80-DMA DETAIL DESCRIPTION

The Z80-DMA (MK3883) is used to perform disk/memory or memory/disk transfer operations on the MDX-FLP board. Before attempting to use the MDX-FLP board in this mode, the user should familiarize himself with the control functions of the MK3883 DMA.

3-2. REGISTER DESCRIPTION

The following DMA-internal registers are available to the programmer:

1. Control Registers: Hold DMA control information; such as, when to initiate an interrupt or pulse, what mode or class of operation to perform, etc. (Write Only) (8 Bits)
2. Timing Registers: Hold read/write timing parameters for the two ports. (Write Only) (8 Bits)
3. Interrupt Vector/Register: Holds the 8-bit vector that the DMA will put onto the data bus after receiving an IORQ during an interrupt acknowledge sequence if it is the highest priority device requesting an interrupt. (This register is "readable" only during interrupt acknowledge cycles.) (Read/Write) (8 bits)
4. Block Length/Register: Contains total block length of data to be searched and/or transferred. (Write Only) (16 Bits)
5. Byte Counter: Counts number of bytes transferred (or searched). On a Load or Continue the Byte Counter is reset to zero. Thereafter, each byte transfer operation increments it until it matches the contents of the Block Length Register, at which time End of Block is set in the status register and operation is suspended if programmed. Also, if so programmed, the DMA will generate an interrupt. (Read Only) (16 Bits)
6. Compare Register: Holds the byte for which a match is being sought in Search operations. (Write Only) (8 Bits)

7. Mask Register: Holds the 8 bit mask to determine which bits in the compare register are to be examined for a match. (Write Only) (8 Bits).
8. Starting Address Register/ (Port A and Port B): Holds the starting address (upper and lower 8 bits) for the two ports involved in Transfer operations. In Search Only operations, only one port address would have to be specified. Only memory starting addresses require both upper and lower 8-bits; I/O ports are generally addressed with only the lower 8-bits, and in this case the address contained in the register is generally a fixed address. (Write Only) (16 Bits each)
9. Address Counters (Port A and Port B): These counters are loaded with the contents of the corresponding Starting Address Registers whenever Searches or Transfers are initiated with a Load or Continue. They are incremented, decremented or remain fixed, as programmed. (Read Only) (16 Bits Each)
10. Pulse Control Register: Holds program supplied length (in bytes) of block after which the DMA will provide a signal pulse on the INT pin. (Since this occurs while both $\overline{\text{BUSRQ}}$ and $\overline{\text{BUSAK}}$ are active, the CPU will not interpret this as an interrupt request. Instead, the signal is used to communicate with a peripheral I/O device.) (Write Only) (16 Bits each)
11. Status Register: Match, End of Block, Ready Active, Interrupt Pending, and Transfer Occurred bits are included in DMA status. (Read Only) (8 Bits)

3-3. MODES OF OPERATION

The DMA may be programmed for one of three modes of operation. (See Command Byte 2B). In the BYTE AT A TIME mode, control is returned to the CPU after each one-byte cycle. The BURST mode operation continues as long as the DMA's RDY input is active, indicating that the relevant port is ready. Control returns to the CPU when RDY is inactive or at end of block or a match if so programmed. The CONTINUOUS mode causes the entire Search and/or Transfer of a block of data to be completed before control is returned to CPU. The MDX-FLP DMA should be programmed for BYTE AT A TIME operation.

3-4. CLASSES OF OPERATION

The DMA has three classes of operation: Transfer Only, Search Only and a combined Search-Transfer. (See Command Byte 1A). During a Transfer, data is read from one port and written to the other port, byte by byte. (The two ports with which the DMA operates are termed Port A and Port B.) The ports may be programmed to be either system main memory or peripheral I/O devices. Thus, a block of data might be written from one area in main memory to another, or from a peripheral to main memory. During a Search, data is read only, and compared byte by byte against two DMA-internal registers, one of which contains a match byte and the other an optional mask byte which allows only certain bits to be compared. If any byte of searched data matches, a DMA-internal status bit is set; if programmed to do so, the DMA will then suspend operation and/or generate an interrupt. The third class of operation is a combined Search-Transfer. In such an operation a block of data is transferred as described above until a match is found; then, as in a Search Only operation, the transfer may be suspended and/or an interrupt generated. The MDX-FLP DMA is normally programmed for Transfer operation.

3-5. ADDRESSING

The DMA's addressing of ports is either fixed or sequential, incrementing or decrementing from a starting address. The length of the operation (number of bytes minus one) is specified by the programmed contents of a block length register. The DMA can address block lengths of up to 64K bytes. During a transfer, two separate port addresses are generated, one during the Read cycle and one during the Write cycle.

3-6. OPERATING SEQUENCE

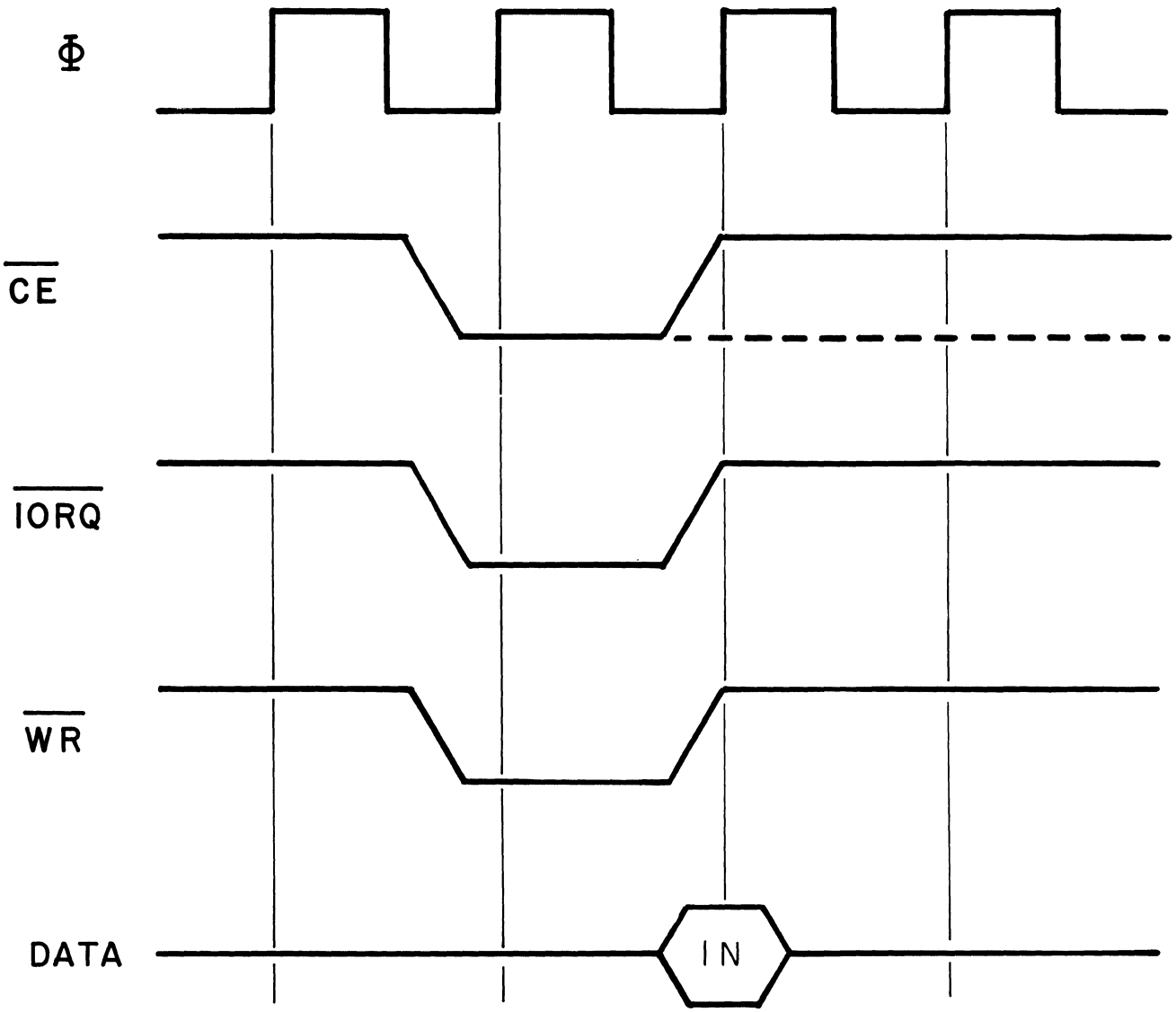
Once the DMA has been programmed it may be "Enabled" (Command Byte 2D). In the enabled condition, when Ready goes active; the DMA will request the bus by bringing $\overline{\text{BUSRQ}}$ low. The CPU will acknowledge this with a $\overline{\text{BUSACK}}$ which will normally be attached to $\overline{\text{BAI}}$. When the DMA receives $\overline{\text{BAI}}$ it will start its

programmed operation, releasing $\overline{BUSRQ}$ to a "high" state when it is through.

3-7. DMA COMMAND WRITE CYCLE TIMING

Figure 3-1 illustrates the timing associated with a command byte or control byte being written to the DMA which is to loaded into an internal register. Z80 Output instructions satisfy this timing.

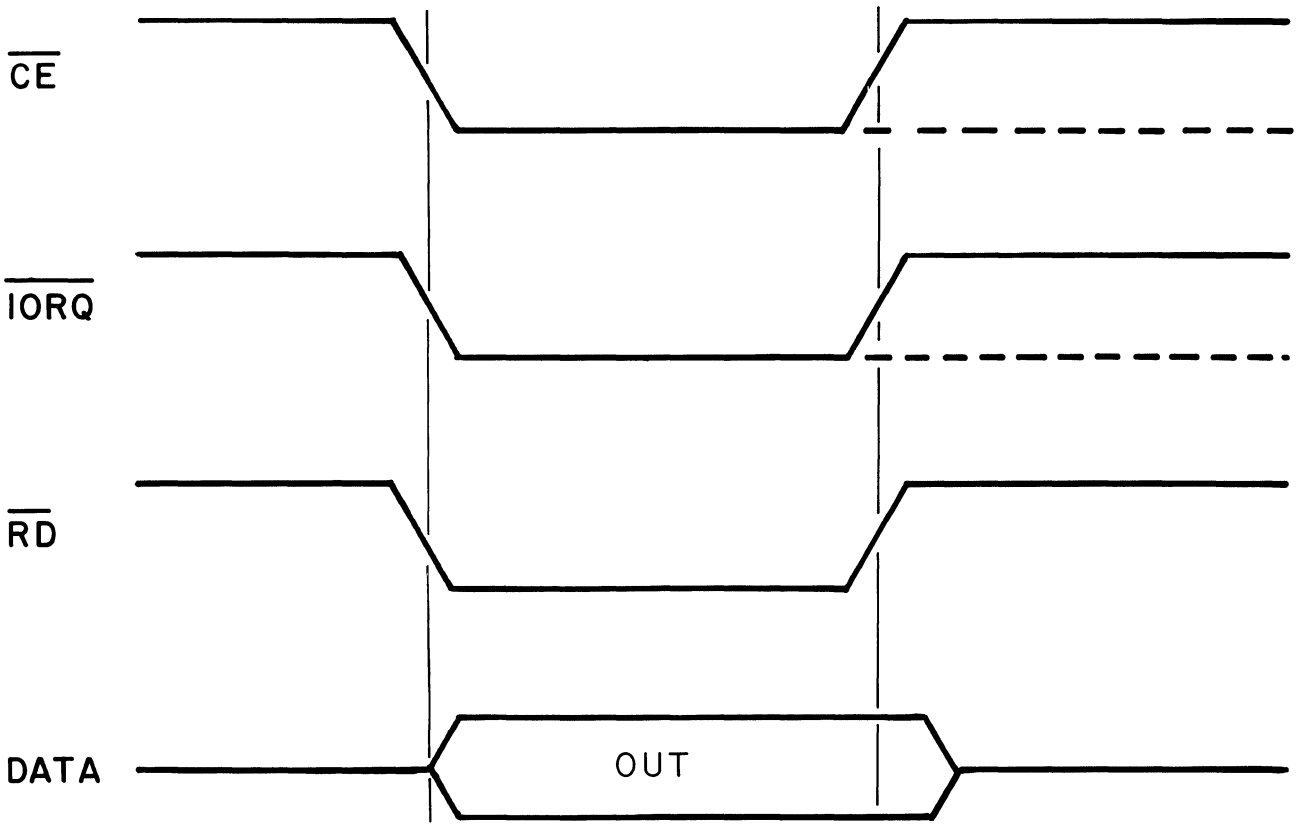
FIGURE 3-1. Z80-DMA COMMAND WRITE CYCLE



DMA REGISTER READ CYCLE

This timing (Illustrated in Figure 3-2) is used when a read operation is performed on the DMA to access the contents of the Status Register, Address Counter or other readable registers. Z80 input instructions satisfy this timing.

FIGURE 3-2. Z80-DMA REGISTER READ CYCLE

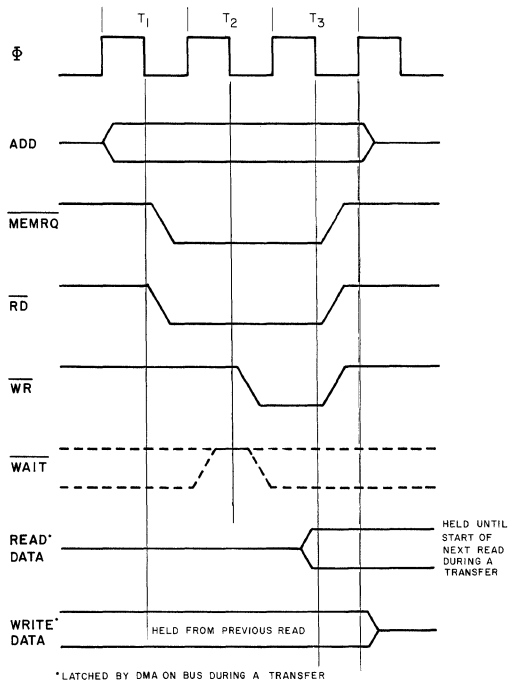


3-8. STANDARD MEMORY TIMING

This timing as shown in Figure 3-3 is exactly the same as used by the Z80-CPU to access system main memory, either in a Read or Write operation. The DMA should default to this timing after a power-on reset, or when a Reset command is written to it; and unless otherwise programmed, should use this timing during all Transfer or Search operations involving system main memory. The MDX-FLP DMA should utilize standard timing with memory. It is good programming practice to initialize the DMA Controller to standard timing via Reset Timing commands to both Ports, before commencing operations. During the memory Read portion of a transfer cycle, data is latched in the DMA on the negative edge of $\overline{\Phi}$ during T3 and held into the following Write cycle. During the memory Write portion of a transfer cycle, data is held from the previous Read cycle and released at the end of the present cycle.

NOTE: The DMA is normally programmed for a 3 T-cycle duration in memory transactions. But $\overline{WAIT}$ is sampled during negative transition of T2, and if it is low, T2 will be extended another T-cycle, after which $\overline{WAIT}$ will again be sampled. The duration of a memory transaction cycle may thus be indefinitely extended.

FIGURE 3-3. STANDARD MEMORY TIMING

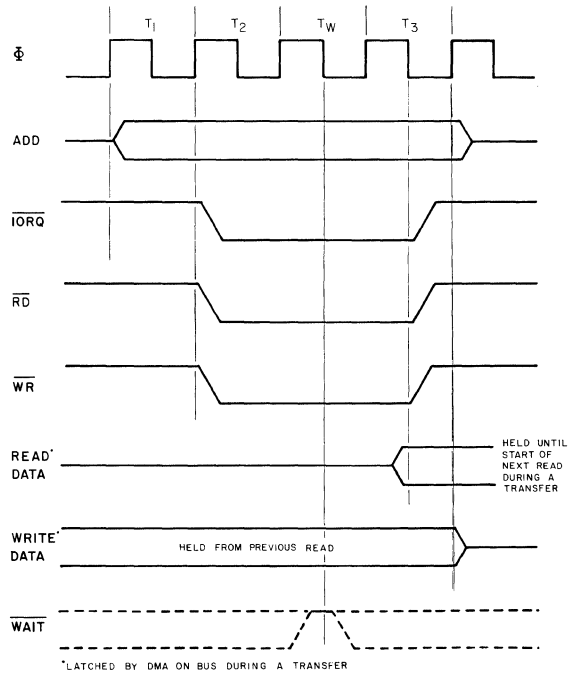


3-9. STANDARD PERIPHERAL TIMING

This timing as shown in Figure 3-4 is identical to the Z80-CPU's Read/Write timing to I/O peripheral devices. The DMA should default to this timing after a power-on reset, or when a Reset command is written to it; and unless otherwise programmed, will use this timing during all Transfer or Search operations involving I/O peripherals. The MDX-FLP should use standard timing with the 1771. It is good programming practice to initialize the DMA Controller to standard timing via Reset Timing command to both Ports, before commencing operations. During the I/O Read portion of a Transfer cycle, data is latched on the negative edge of Φ during T3 and is then held into the Write cycle. During and I/O Write, data is held from the previous Read cycle until the end of the Write cycle.

NOTE: If $\overline{WAIT}$ is low during the negative transition of TW*, then TW* will be extended another T-cycle and $\overline{WAIT}$ will again be sampled. The duration of a peripheral transaction cycle may thus be indefinitely extended.

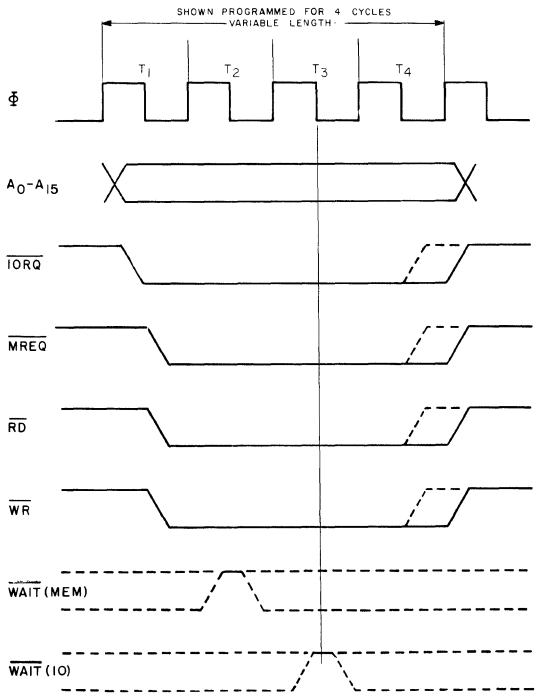
FIGURE 3-4. STANDARD PERIPHERAL TIMING



3-10. VARIABLE CYCLE TIMING

The Variable feature of the DMA shown in Figure 3-5 allows the user to program the DMA's memory or peripheral transaction timing to values different than given above in the standard default diagrams. This permits the designer to tailor his timing to the particular requirements of his system components, and maximizes the data transfer rate while eliminating external signal conditioning logic. Cycle length can be one to four T-cycles (more if $\overline{WAIT}$ is used). Signal timing can be varied as shown. During a transfer, data will be latched by the DMA on the clock edge causing the rising of $\overline{RD}$ and will be held on the data lines until the end of the following Write cycle.

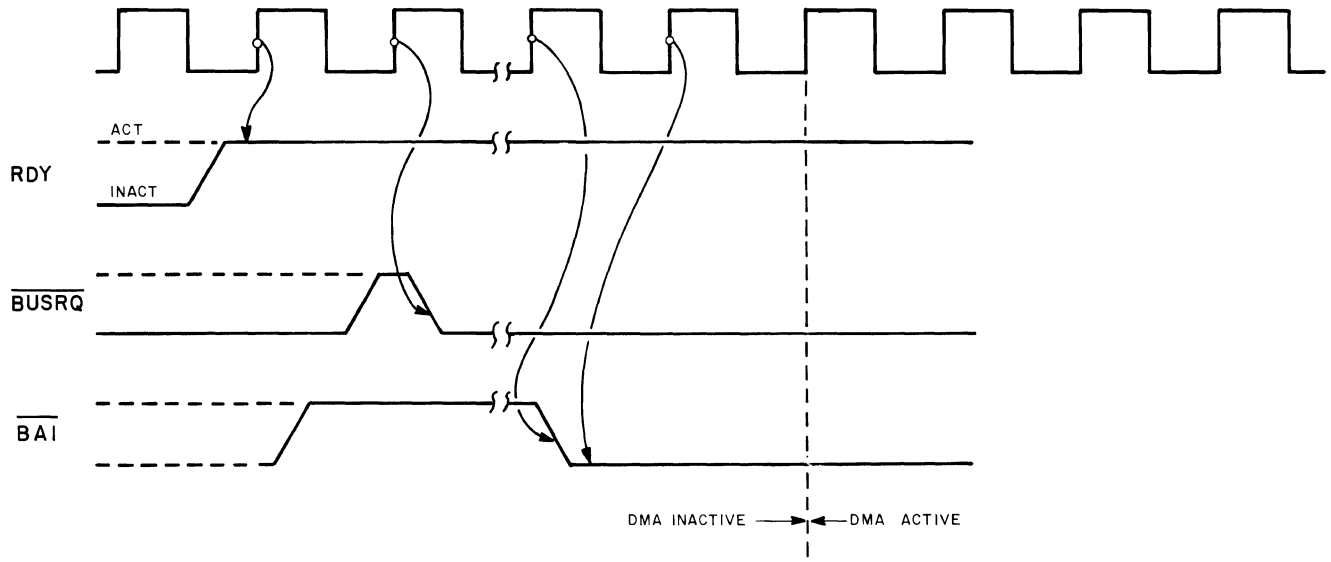
FIGURE 3-5. VARIABLE CYCLE TIMING



3-11. DMA BUS REQUEST AND ACCEPTANCE FOR BYTE-AT-A-TIME, BURST, AND CONTINUOUS MODE

Ready is sampled on every rising edge of $\underline{\Phi}$. When it is found to be active, the following rising edge of $\underline{\Phi}$ generates $\overline{\text{BUSRQ}}$. After receiving $\overline{\text{BUSRQ}}$ the CPU will grant a $\overline{\text{BUSAK}}$ which will be connected to $\overline{\text{BAI}}$ either directly or through the Bus Acknowledge Daisy Chain. When a low is detected on $\overline{\text{BAI}}$ (sampled on every rising edge of $\underline{\Phi}$), the next rising edge of $\underline{\Phi}$ will start an active DMA cycle. See Figure 3-6.

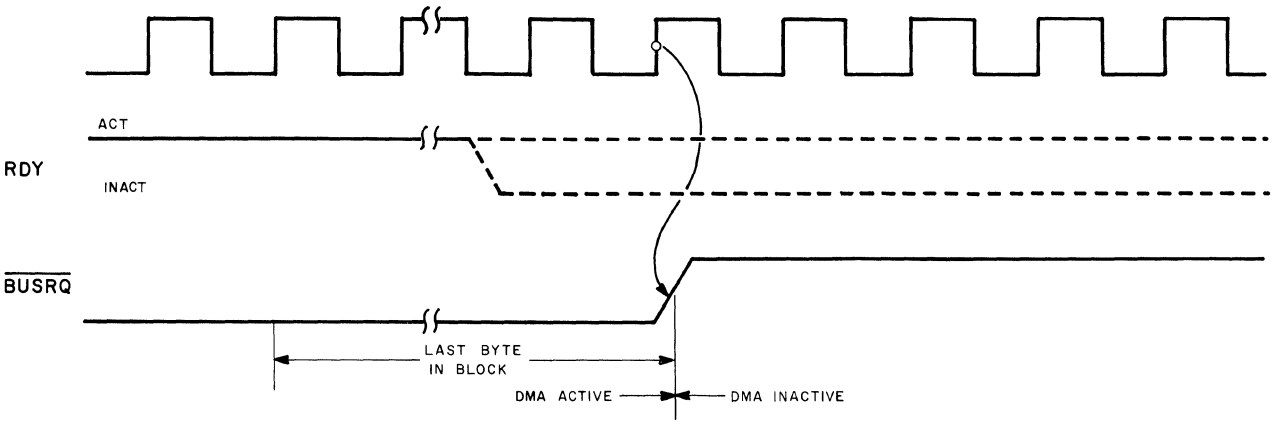
FIGURE 3-6. BUS REQUEST AND ACCEPTANCE FOR BYTE-AT-A-TIME, BURST, AND CONTINUOUS MODE



3-12. DMA BUS RELEASE TIMING

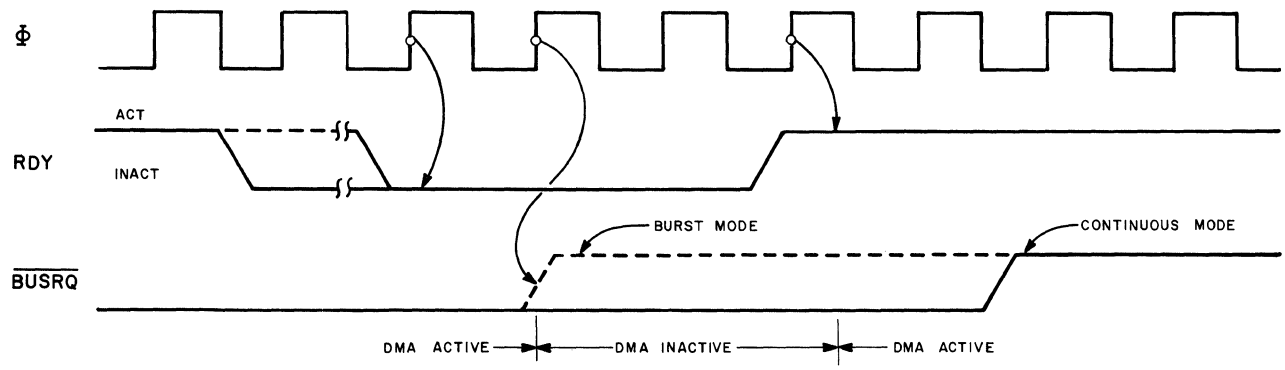
Timing for End of Block and DMA not programmed for Auto-restart during Burst or Continuous mode is shown in Figure 3-7.

FIGURE 3-7. BUS RELEASE AT END OF BLOCK



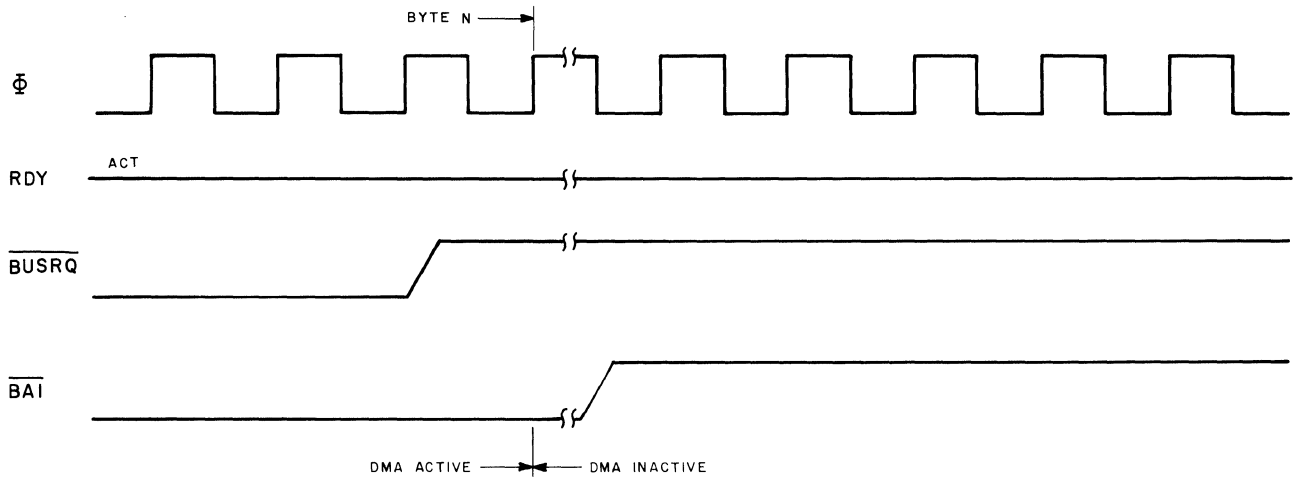
The DMA will relinquish the bus after RDY has gone inactive (Burst mode) or after an End of Block or a Match is found (Continuous Mode). With RDY inactive, the DMA in Continuous mode is inactive but maintains control of the bus ($\overline{\text{BUSRQ}}$ low) until the cycle is resumed when RDY goes active. See Figure 3-8.

FIGURE 3-8. BUS RELEASE WITH 'READY' FOR BURST AND CONTINOUS MODE



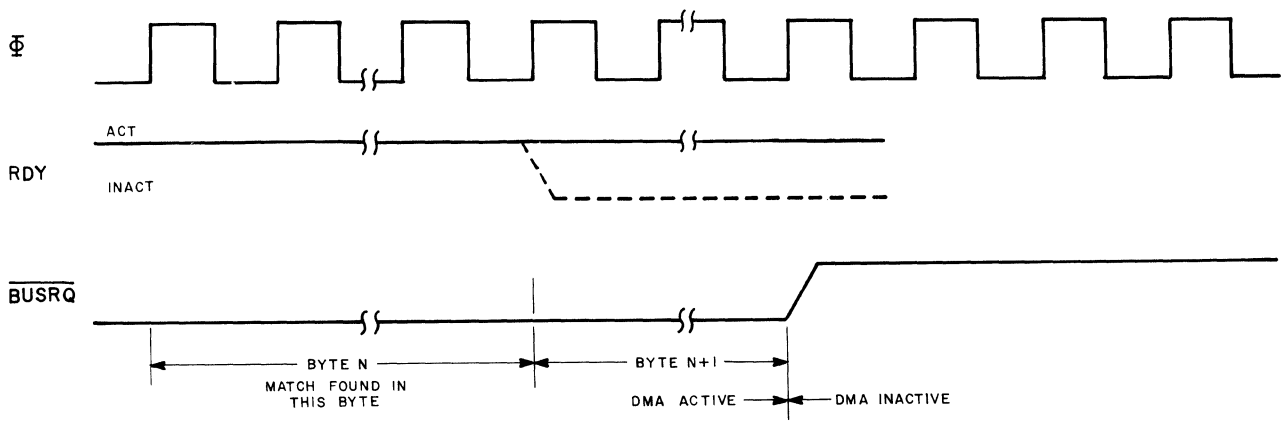
In the Byte mode the DMA will release BUSRQ on the rising edge of Φ prior to the end of each Read cycle in Search Only or each Write cycle in a Transfer, regardless of the state of RDY. The next bus request will come when RDY is active after both BUSRQ and BIA have returned high. Active-to-inactive-to-active transitions are not required to initiate a subsequent bus request; only the (possibly continued) active state of RDY. See Figure 3-9.

FIGURE 3-9. BUS RELEASE FOR BYTE-AT-A-TIME MODE



When a Match is found and the DMA is programmed to stop on Compare, the DMA performs an operation on the next byte and then releases the bus. See Figure 3-10.

FIGURE 3-10. BUS RELEASE WITH MATCH FOR BURST OR CONTINUOUS MODES



3-13. READING FROM THE DMA INTERNAL REGISTERS

The CPU can read seven internal DMA registers, always in the following order: Status, lower byte of the Block Length register, upper byte of the Block Length register, lower byte of the Port A Address, upper byte of the Port A Address, lower byte of the Port B Address and the upper byte of the Port B Address. The Read Mask register must be programmed to either include or exclude any of these seven registers by programming a 1 (include) or 0 (exclude) in the appropriate positions of the Read Mask register. After a Reset or Load, the read sequence must be initiated through an Initiate Read Sequence command (Command Byte 2D). The sequence of reading all registers that are not excluded by the Read Mask register must be completed before a new Initiate Read Sequence or RD Status command.

3-14. PROGRAMMING THE DMA

Previous sections of this document have indicated the various functions and modes of the DMA. The diagrams and charts below will show how the DMA is programmed to select among these functions and modes and to adapt itself to the requirements of the user system. More detailed programming information is available in the Z80-DMA Technical Manual. The Z80-DMA chip may be in an "enable" state, in which it can gain control of the system buses and direct the transfer of data between its ports, or in a "disable" state, when it can not gain control of the bus. Program commands can be written to it in either state, but writing a command to it automatically puts it in the disable state, which is maintained until an enable command is issued to the DMA. The CPU must program it in advance of any data search or transfer by addressing it as an I/O port and sending it a sequence of 8 bit command bytes via the system data bus using Output instructions. The Z80 OTIR instruction is recommended for such programming. When the DMA is powered up or reset by any means, the DMA will automatically be placed into a disable state, in which it can initiate neither bus requests, nor data transfers, nor interrupts.

The command bytes contain information to be loaded into the DMA's control and other registers and/or information to alter the state of the chip, such as an Enable Interrupt command. The command structure is designed so that certain bits in some commands can be set to alert the DMA to expect the next byte written to it to be for a particular internal register. The following gives the function of each bit in the six different command bytes. Two of these are defined as being from Group 1, and are termed command bytes 1A and 1B. These Group 1 commands contain the most basic DMA set-up information. The other four are categorized as Group 2, and are termed commands 2A, 2B, 2C, and 2D. Group 2 words specify more detailed set-up information.

3-15. COMMAND BYTE 1A

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	BLOCK LENGTH (UPPER) FOLLOWS	BLOCK LENGTH (LOWER) FOLLOWS	PORT A STARTING ADDRESS (UPPER) FOLLOWS	PORT A STARTING ADDRESS (LOWER) FOLLOWS	SOURCE PORT	CLASS CONTROL C_1	CLASS CONTROL C_0

SPECIFIES GROUP I

BYTE IA CANNOT BE 0(

C_1	C_0	Function
0	0	Not allowed. (Command Byte 1B)
0	1	Transfer Only.
1	0	Search Only.
1	1	Search and Transfer.

D_2=1 Port A is read from, Port B is written to (unless the Search Only Mode has been selected, in which case Port B is never addressed).

D_2=0 Port B is read from, Port A is written to (unless the Search Only Mode has been selected, in which case Port A is never addressed).

If more than one among bits D3-D6 are programmed as one, the order of following bytes should follow the order: Port A lower, Port A upper, Block Length Lower, Block Length upper. The DMA always transfers or searches one byte more than the number written into the Block Length registers. A "0" in the block length register results in transfer or search of 2^{16} + 1 bytes. The shortest programmable block length is thus two bytes, programmed by writing a 1 into the Block Length register.

3-16. COMMAND BYTE 1B

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	TIMING BYTE FOLLOWS	ADDRESS FIXED	ADDRESS INCREMENTS DECREMENTS	I/O OR MEMORY	PORT A OR B	0	0
SPECIFIES GROUP I						SPECIFIES BYTE 1B	

D_4=1 Address for this port increments after each byte.

D_4=0 Address for this port decrements after each byte.

D_3=1 This port addresses an I/O peripheral.

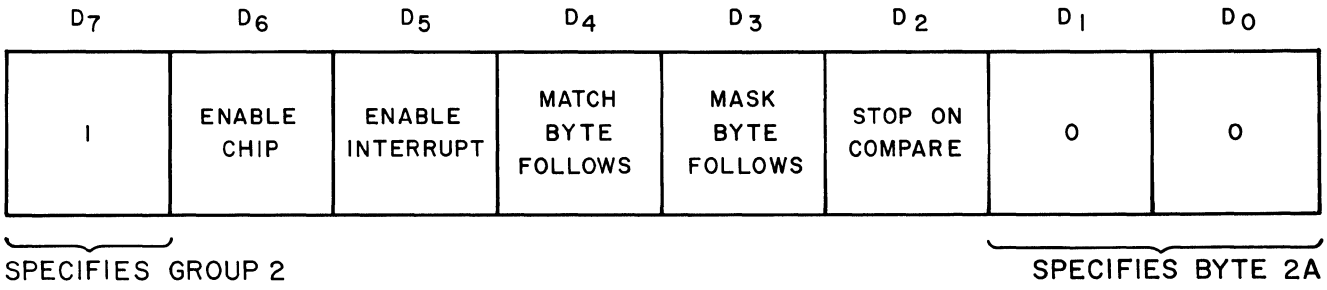
D_3=0 This port addresses main memory.

D_2=1 This word programs Port A.

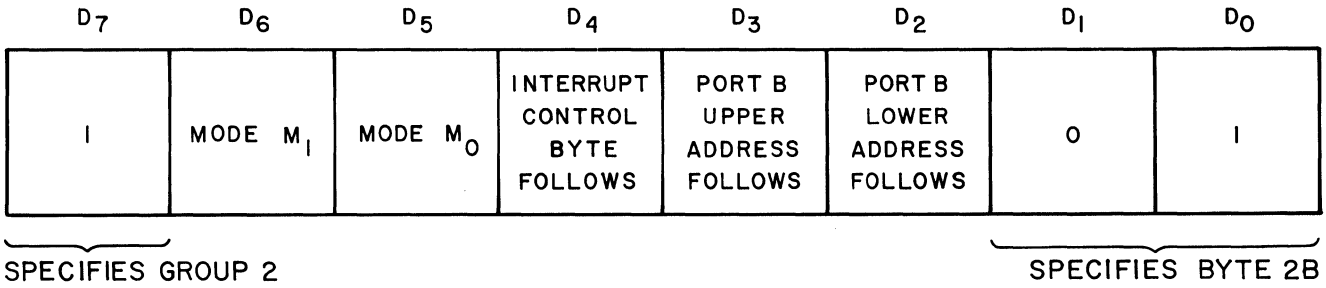
D_2=0 This word programs Port B.

For transfers, this byte is normally written twice, once for Port A and again for Port B.

3-17. COMMAND BYTE 2A



3-18. COMMAND BYTE 2B



M1	M0	Mode
0	0	Byte
0	1	Continuous
1	0	Burst
1	1	Do Not Program

If more than one among D2-D4 are programmed as one, the sequence of following bytes must follow the order: B Address lower, B Address upper, interrupt control byte.

3-19. COMMAND BYTE 2C

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	NOT USED	AUTOMATIC RESTART	$\overline{\text{WAIT}}$ MULTIPLEXED	READY HIGH/LOW	NOT USED	1	0
SPECIFIES GROUP 2						SPECIFIES BYTE 2C	

D_5=1 Automatically repeats entire operation when end of block is reached.

D_5=0 Operation stops when end of block is reached.

D_4=1 CE and WAIT multiplexed on same pin.

D_4=0 CE only.

D_3=1 Ready active high.

D_3=0 Ready active low.

The MDX-FLP DMA should be programmed "CE and WAIT multiplexed" and "Ready Active High".

3-20. COMMAND BYTE 2D

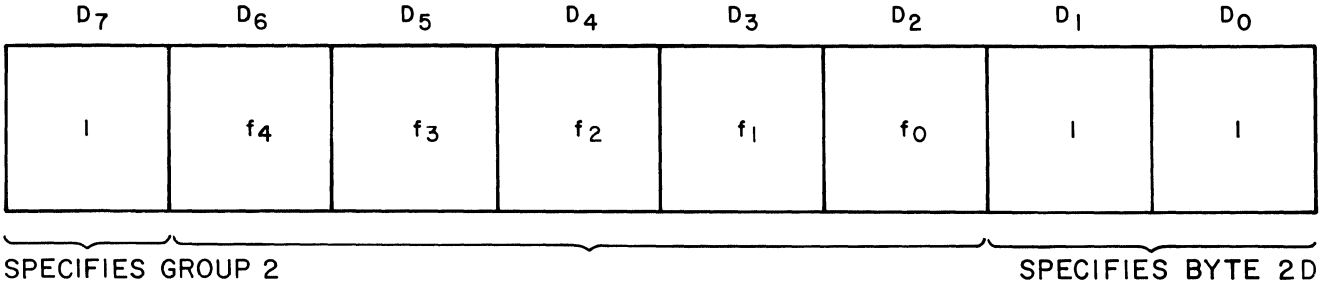


TABLE 3-1.

Hex	f_4	f_3	f_2	f_1	f_0	
C3	1	0	0	0	0	Reset
C7	1	0	0	0	1	Reset Port A Timing
CB	1	0	0	1	0	Reset Port B Timing
CF	1	0	0	1	1	Load
D3	1	0	1	0	0	Continue
AB	0	1	0	1	0	Enable Int
AF	0	1	0	1	1	Disable Int
A3	0	1	0	0	0	Reset Int
87	0	0	0	0	1	Enable DMA
83	0	0	0	0	0	Disable DMA
BB	0	1	1	1	0	Read Byte Follows
A7	0	1	0	0	1	Reset RD
BF	0	1	1	1	1	RD Status
B3	0	1	1	0	0	Force Ready
B7	0	1	1	0	1	Enable After RETI
8B	0	0	0	1	0	Reset Status

Z80-DMA COMMAND BYTE 2D SUMMARY

Reset:	Reset interrupt circuitry, disables interrupt and bus req. logic, unforce internal Ready condition, disable "MUXCE" and stop auto repeat.
Reset Timing A or B:	Resets timing for Port A or B to a standard Z80-CPU timing.
Load:	Zeros Byte Counter and loads Starting Address for both Ports.*
Continue:	Resets byte counter only. Addresses continue from present location.
Enable Interrupt:	Permits interrupt to occur.
Disable Interrupt:	Inhibits interrupt from occuring.
Reset Interrupt:	Resets and disables all interrupt circuits (similar to RETI) and unforces the internal Ready condition.
Enable DMA, Disable DMA:	Overall enable or disable for all operations except interrupts; does not reset any functions.
Read Byte Follows:	Next write to DMA will contain a mask to program which readable registers are to be read.
Reset RD:	Initiate Read sequence to the first register designated as readable by the Read Mask register.
RD Status:	Next read will be from status register.

Force Ready: Ready will be considered active regardless of the state of external RDY pin. Used for Mem-Mem operations where no RDY signal is needed. This command does not function in BYTE-AT-A-TIME mode.

Enable after RETI: DMA will not request bus until after it has received a RETI. Must be followed by an Enable DMA command.

RST Status: Resets Match and End of Block status bits.

*Loading Port Addresses. The "Load" command (CF in Command Byte 2D) loads a fixed address only into a port selected as the source, not into a port selected as the destination. Therefore, the destination address must be loaded by temporarily mislabeling the destination as the source. The following example is a set-up procedure for a transfer from Port A to Port B:

1. Command Byte 1A with B as source port.
2. Command Byte 2D with CF = load.
3. Command Byte 1A with A as source port.
4. Command Byte 2D with CF = load.
5. Command Byte 2D with 87 = Enable DMA

This manipulation is required only when the destination has a fixed address (Write disk operation in MDX-FLP).

3-21. READ BYTE

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
NOT USED	PORT B UPPER ADDR	PORT B LOWER ADDR	PORT A UPPER ADDR	PORT A LOWER ADDR	BYTE UPPER COUNT	BYTE LOWER COUNT	STATUS

A "1" in any bit position enables that register to be read.

Bytes will be read in "right to left" order per the above diagram.

3-22. INTERRUPT CONTROL BYTE

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
NO EFFECT	INTERRUPT BEFORE REQUESTING BUS	STATUS AFFECTS INTERRUPT VECTOR	INTERRUPT VECTOR FOLLOWS	PULSE COUNT FOLLOWS	PULSE GENERATED	INTERRUPT AT END OF BLOCK	INTERRUPT ON MATCH

A "1" in a bit position selects the option.

If both D3 and D4 are "1", the Pulse Count precedes the Interrupt Vector. If "Interrupt Before Requesting Bus" is selected (by a 1 in bit 6 of the Interrupt Control byte), the Z80 DMA does not request the bus until the following set of instructions has been received by the Z80 DMA:

- Enable after RETI command (B7 in Command byte 2D).
- Enable DMA command (87 in Command byte 2D).
- A RETI instruction that resets the IUS (Interrupt Under Service latch)in the Z80 DMA.

3-23. TIMING CONTROL BYTE

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
$\overline{WR}$ END	$\overline{RD}$ END	NOT USED	NOT USED	$\overline{MREQ}$ END	$\overline{IORQ}$ END	T_1	T_0

T_1	T_0	Cycle Length
0	0	4
0	1	3
1	0	2

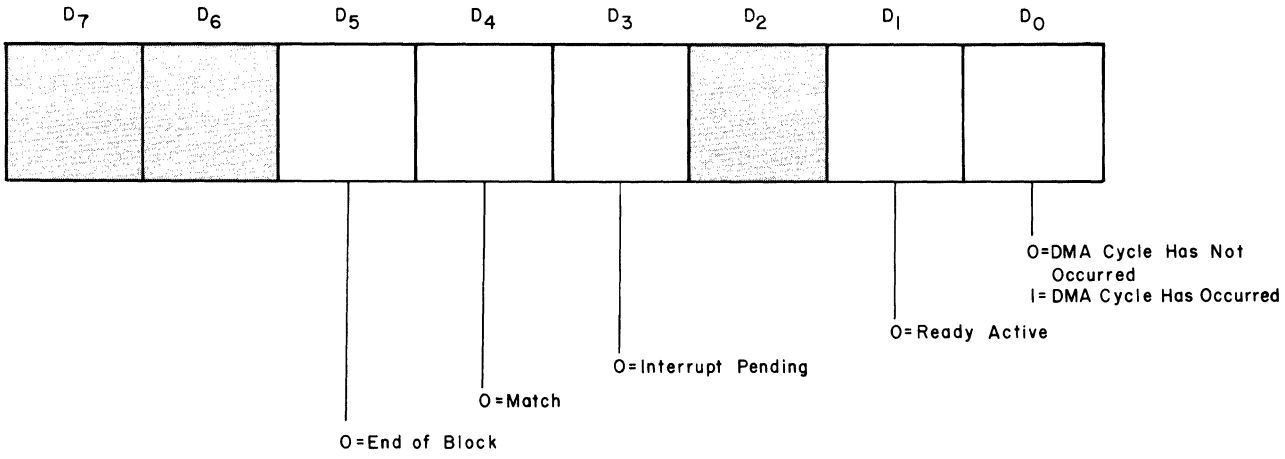
A "0" in D_2, D_3, D_6, or D_7 will cause the corresponding control

signal to end 1/2 clock time before the end of the cycle. Note: The total operation (Read and Write in Transfer or Read in Search) must be at least 2 cycles long.

3-24. MASK BYTE & MATCH BYTE

A zero in a given bit position will cause a compare to be performed between that bit position in the compare word register and the same bit position in the data being read. Up to an 8-bit word can be compared to D0 - D7 during a read.

3-25. STATUS BYTE (READ)



3-26. PULSE COUNT

This 8-bit word is loaded into a register. At the completion of each operation, the register is compared with the lower 8-bits of the byte counter. When it compares, the INT line is pulsed while BUSRQ and BUSAK are both low/active (no interrupt is generated).

3-27. INTERRUPT VECTOR

This 8-bit byte is supplied to the CPU during Interrupt acknowledge if the DMA is

the highest priority interrupting device. If bit 5 of the Interrupt Control Byte (Section 3-21) has been set and the DMA has been programmed to interrupt on a given status condition then D1 and D2 of the vector will be modified as follows:

Vector Bits	D2	D1	
	0	0	INT on RDY
	0	1	Match
	1	0	End of Blk
	1	1	Match, End of Blk

3-28. BYTE COUNT (READ)

This will be returned as one less than the number of bytes transferred. The ambiguous case of "0" result can be resolved by examination of D0 of the Status register.

3-29. A AND B ADDRESS READBACK

For an incremented or decremented address in the source port, the address returned will be that of the last (RAM) address transferred, plus or minus one respectively. For an incremented or decremented destination port, the address returned will be that of the last (RAM) address transferred.

3-30. SAMPLE DMA PROGRAMMING SEQUENCES FOR MDX-FLP

The following three Z80 examples are recommended for DMA setup with the MDX-FLP board. In each case, the command string can be output by the sequence:

```
LD      HL,DMASTn
LD      BC,DMASnL*256+PORT
OTIR
```

Where n is the example number 0-2, and PORT is equated to the first board address (DMA port).

The following points should be noted:

1. The DMA setup sequence should be output to the board before the 1771 command to initiate the disk operation is output.
2. The need for some of the initialization commands in the following sequences is debatable, if the previous setup and use of the DMA is known.

3-31. DMA SETUP STRING FOR WRITE OR READ DISK, NON-INTERRUPT

```
DMASTO:     DEFB    0C3H        ; (2D) RESET DMA
            DEFB    0C7H        ; (2D) RESET "A" TIMING
            DEFB    0CBH        ; (2D) RESET "B" TIMING
            DEFB     79H        ; (1A) XFER, B-->A AAD, LENGTH FOLLOW
ADO         DEFW    $-$         ; ** FILL IN RAM ADDRESS
LO          DEFW     127        ; ** FILL IN DATA LENGTH-1 IF NOT 128
                                                BYTE SECTOR
            DEFB    14H         ; (1B) A = MEMORY, INCREMENT
            DEFB    28H         ; (1B) B = IO, FIXED
                                ; (2A) NOT REQUIRED
            DEFB    85H         ; (2B) BYTE MODE, BAD LO FOLLOWS
            DEFB    PORT+7      ; 1771 DATA REG ADDRESS
            DEFB    9AH         ; (2C) CE/WAIT, RDY ACT HI
            DEFB    0CFH        ; (2D) LOAD ADS, CLEAR BYTE CTR
OMIT FOR    DEFB    05H         ; (1A) A-->B FOR WRITE DISK
READ DISK   DEFB    0CFH        ; (2D) LOAD AGAIN (See 3-21 NOTE)
            DEFB    87H         ; (2D) LAST COMMAND ENABLES DMA
DMASOL:     EQU     $-DMASTO    ; LENGTH OF STRING
```

3-32. DMA SETUP STRING FOR WRITE OR READ DISK, INTERRUPT AT COMPLETION

```
DMAST1:     DEFB    0C3H        ; (2D) RESET DMA
            DEFB    0A3H        ; (2D) RESET INTERRUPT
            DEFB    0C7H        ; (2D) RESET "A" TIMING
```

```
                DEFB    0CBH            ; (2D) RESET "B" TIMING
                DEFB    79H             ; (1A) XFER, B→A, AAD, LENGTH FOLLOW
AD1:            DEFW    $-$             ; ** FILL IN RAM AD
L1:             DEFW    128             ; FILL IN DATA LENGTH IF NOT
                                        ; 128  BYTE SECTOR

;  NOTE THAT # BYTES TRANSFERRED BY DMAC IS 1 MORE THAN SECTOR LENGTH,
;  SO INTERRUPT OCCURS ON INTRQ.

                DEFB    14H             ; (1B) A = MEMORY, INCREMENT
                DEFB    28H             ; (1B) B = IO, FIXED
                DEFB    0E0H            ; (2A) ENAB INT I
                DEFB    95H             ; (2B) BYTE, BADLO, INT FOLLOW
                DEFB    PORT+7          ; 1771 DATA REG ADDRESS
                DEFB    12H             ; INT AT EOB, VECTOR FOLLOWS
                DEFB    VECDSP          ; VECTOR DISPLACEMENT IN INT TABLE
                DEFB    9AH             ; (2C) CE/WAIT, RDY ACT HI
                DEFB    0CFH            ; (2D) LOAD ADS, CLEAR BYTE CTR
OMIT FOR        DEFB    05H             ; (1A) A→B  FOR WRITE DISK
READ DISK       DEFB    0CFH            ; (2D) LOAD AGAIN (SEE 3-21 NOTE)
                DEFB    0ABH            ; (2D) ENABLE INT II
                DEFB    87H             ; (2D) LAST COMMAND ENABLES CHIP
DMAS1L:         EQU     $-DMAST1        ; LENGTH OF STRING
```

3-33. DMA SETUP STRING FOR CONTROL OP, INTERRUPT AT COMPLETION

```
DMAST2:         DEFB    0C3H            ; (2D) RESET DMA
                DEFB    0A3H            ; (2D) RESET INTERRUPT
                DEFB    79H             ; (1A) XFER, B→A, AAD, LENGTH FOLLOW
                DEFW    DMAST2          ; ANY OLD RAM AD
                DEFW    1               ; MIN LENGTH = 2 BYTES
                DEFB    14H             ; (1B) A = MEM, INCR
                DEFB    28H             ; (1B) B = IO, FIXED
```

```
            DEFB    0E0H            ; (2A) ENAB INT I
            DEFB    0B5H            ; (2B) CONT, BAD LO, INT FOLLOW
            DEFB    PORT+7          ; WRITE 2 INTO 1771 DATA REG
            DEFB    12H             ; INT AT EOB, VECTOR FOLLOWS
            DEFB    VECDS2          ; VECTOR DISPLACEMENT IN INT TABLE
            DEFB    9AH             ; (2C) CE/WAIT, RDY ACT HI
            DEFB    0CFH            ; (2D) LOAD ADS, CLEAR BYTE CTR
            DEFB    05H             ; (1A) A→B TO WRITE DATA REG
            DEFB    0CFH            ; (2D) LOAD AGAIN (SEE 3-21 NOTE)
            DEFB    0ABH            ; (2D) ENABLE INT II
            DEFB    87H             ; (2D) LAST COMMAND ENABLES CHIP
DMAS2L      EQU     $-DMAST2        ; LENGTH OF STRING
```

3-34. READING DMA REGISTERS BACK

At the completion of a DMA transfer, the following instructions will accomplish reading back the status, byte count, and A side (RAM) address from the DMA Controller:

```
            LD  HL,DMARDC
            LD  BC,4*256+PORT
            OTIR
            LD  B,5
            INIR
            • CODE TO EXAMINE (DMAST, DMABC, DMAAD)
            •
            •
            •

                                ;  COMMAND STRING TO CONDITION DMA FOR READING

DMARDC:     DEFB    0BBH        ; (2D) READ MASK FOLLOWS
            DEFB    1FH         ; MASK = A AD HI/LO, BYTE CT HI/LO, STATUS
            DEFB    0BFH        ; (2D) SET READ STATUS
```

```
            DEFB    0A7H        ; (2D) INIT READ
                                ; STATUS AREA FOLLOWS IMMEDIATELY
DMAST:      DEFB    0           ; DMA STATUS
DMABC:      DEFW    0           ; BYTE COUNTER
DMAAD:      DEFW    0           ; A SIDE (RAM) TERM. ADDRESS
```

3-35. FLEXIBLE DISK CONTROLLER/FORMATTER CHIP

The MDX-FLP Flexible Disk Controller Board uses the Western Digital FD1771 programmable floppy disk formatter/controller chip to generate the majority of signals required to transfer data, status, and control between the CPU and disk drives.

3-36. The Flexible Disk controller chip block diagram is shown in Figure 3-11. The primary sections include the Processor/DMA Controller interface and the Floppy Disk interface.

3-37. DATA SHIFT REGISTER

This 8-bit register assembles serial data from the Read Data input during operations and transfers serial data to the Write data output during Write operations.

3-38. DATA REGISTER

This 8-bit register is used as a holding register during Disk Read and Write operations. In Disk Read operations, the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In Disk Write operations, information is transferred in parallel from the Data Register to the Data Shift Register. When executing the Seek command, the Data Register holds the address of the desired Track position. This register can be loaded from the Data Bus and gated onto the Data Bus under processor or DMA control.

3-39. TRACK REGISTER

This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head is stepped in (towards track 76) and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disk Read, Write and verify operations. The Track Register can be loaded from or transferred to the Data Bus. This Register should not be loaded when the 1771 is busy.

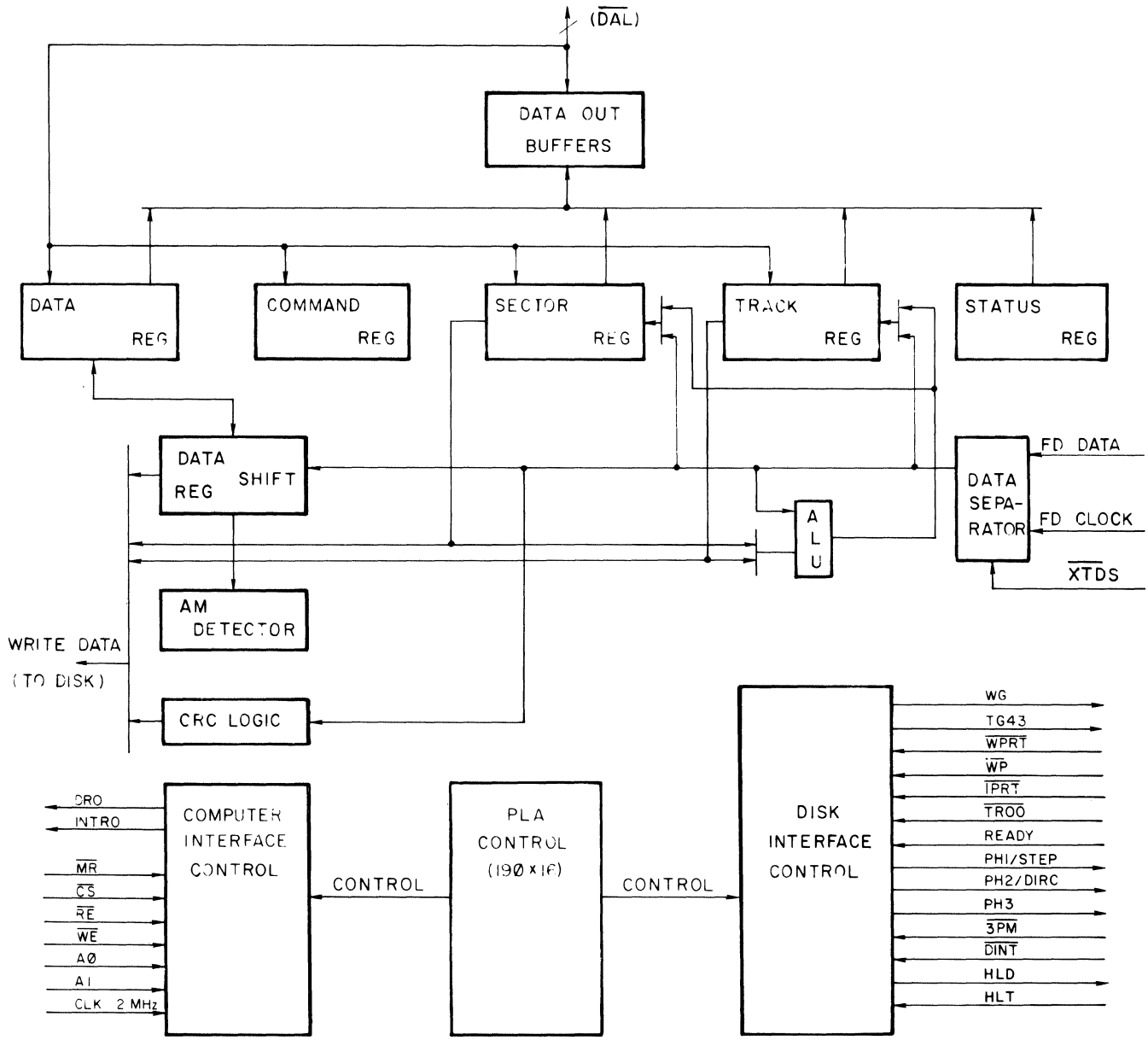
3-40. AM DETECTOR

The Address Mark detector is used to detect ID, Data, and Index address marks during Read and Write operations.

3-41. TIMING AND CONTROL

All computer and Floppy Disk Interface controls are generated through this logic. The internal device timing is generated from a crystal clock, at 2MHZ for 8" drives, 1MHZ for 5" drives.
NOTE: With 1MHZ clock, all references to timing in the following sections unless otherwise indicated should be doubled.

FIGURE 3-11. FLOPPY CONTROLLER CHIP BLOCK DIAGRAM



3-42. SECTOR REGISTER (SR)

This 8-bit register hold the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk Read or Write operations. The Sector Register contents can be loaded from or transferred to the Data Bus. This register should not be loaded when the 1771 is busy.

3-43. COMMAND REGISTER (CR)

This 8-bit register holds the command presently being executed. This register should not be loaded when the device is busy. The command register can be loaded from the Data Bus, but not read onto the Data Bus.

3-44. STATUS REGISTER (STR)

This 8-bit register holds device Status information. The meaning of the Status bits is a function of the contents of the Command Register. This register can be read onto the Data Bus, but not loaded from the Data Bus.

3-45. CRC LOGIC

This logic is used to check or generate the 16-bit Cyclic Redundancy Check (CRC). The polynomial is: $G(x) = x^{16} + x^{12} + x^{5} + 1$. The CRC includes all information starting with the address mark and up to the CRC characters. The CRC register is preset to ones prior to data being shifted through the circuit.

3-46. ARITHMETIC/LOGIC UNIT (ALU)

The ALU is a serial comparator, incrementer, and decrementer and is used for register modification and comparisons with the disk recorded ID field.

3-47. PROCESSOR/DMA CONTROLLER INTERFACE

The interface to the Processor and DMA Controller is accomplished through the

8-bit Data Bus, chip selection from the Address Bus bits 7-2, within-chip register selection from Address Bus bits 1 and 0, and Read Enable and Write Enable signals derived from STD-BUS signals IORQ, RD, and WR. When transfer of data, control, or status information is required by the Processor or DMA Controller, the device address is decoded and CS is made low. The least significant address bits A1 and A0, combined with the signals RE during a Read operation or WE during a Write operation are interpreted as selecting the following registers for strobing from, or gating onto, the Data Bus.

A1-A0	READ(RE)	WRITE(WE)
0 0	Status Register	Command Register
0 1	Track Register	Track Register
1 0	Sector Register	Sector Register
1 1	Data Register	Data Register

The Processor accesses all of these registers, while the DMA Controller accesses only the Data Register. During Direct Memory Access (DMA) types of data transfers between the Data Register of the FD1771 and the 3883, the Data Request (DRQ) output of the 1771 causes RDY indication to the 3883; the 3883 then transfers one byte to or from System RAM. DRQ also appears as status bit 1 during Read and Write operations. The Lost Data bit and certain other bits in the Status Register will activate the interrupt request (INTRQ) signal. The interrupt line is also activated with normal completion or abnormal termination of all controller operations. The INTRQ signal remains active until reset by reading the Status Register to the processor or by the loading of the Command Register. In addition, the INTRQ is generated if a Force Interrupt command condition is met. INTRQ can be sensed by the Processor via a Read command to "Port 2" of the board. INTRQ also sets RDY to the 3883 DMA Controller, and is not cleared by resultant transfer between the Data Register, the 3883, and system RAM. This implementation forces completion of the DMA block transfer and prevents "lockup" of the 3883 DMAC due to abnormal conditions which result in fewer Data Requests than expected.

-48. HEAD POSITIONING

our commands cause positioning of the Read/Write head. The period of each ositioning step is specified by the r field in bits 1 and 0 of the command word. fter the last directional step, an additional 10 milliseconds of head settling ime takes place. The four programmable stepping rates (rlr0) (refer to Table -3) are tabulated under the Type I Commands description. To accomplish head ovement, a step pulse of 4 microseconds width is produced on 1771 pin 15. Pin 16 s used for direction control with a High voltage indicating a Step In, and a Low oltage indicating a Step Out. The direction output is valid a minimum of 24 icroseconds prior to the activation of the step pulse. When a Seek, Step, or estore command is executed, an optional verification of Read/Write head position an be performed by setting bit 2 in the command word to logic 1. The erification operation begins at the end of the 35 millisecond settling time after he head is loaded against the media. The track number from the first encountered D Field is compared against the contents of the Track Register. If the track umbers compare and the ID Field Cyclic Redundancy Check (CRC) is correct, the erify operation is complete. If track comparison is not made but the CRC checks, NTRQ is activated, the Seek Error status bit (bit 4) is set, and the Busy status it is reset. If there is no track comparison nor a valid CRC, a step is made in he same direction as specified and the verify operation is repeated. The dditional stepping can be repeated twice to account for two defective tracks. If o verification is received at this point, Seek Error (bit 4) and CRC Error (bit) are set in the Status Register. The Head Load (HDL) output controls the ovement of the Read/Write head against the diskette for data recording or etrieval. It is activated at the beginning of a Read, Write (E flag on) or erify operation, or a Seek/Step operation with the head load bit (h) a logic igh; it remains activated until the third index pulse following the last peration which uses the Read/Write head. The operation is delayed 35 ms to allow ngagement of the head against the diskette. In the Seek and Step commands, the ead is loaded at the start of the command execution when the h bit is a logic 1. n a verify command, the head is loaded before stepping to the destination track n the diskette whenever the h bit is a logic 0.

3-49. DISK READ OPERATION

On disk read operations, data is received from the disk in a serial data stream, and transformed by the Data Separator circuitry into pulses on the CLK and DATA inputs of the 1771. The Data Request (DRQ) signal output is activated when an assembled serial input byte is transferred in parallel from the Data Shift Register to the Data Register. This bit is cleared when the Data Register is read by the DMA or the CPU. A (DRQ) signal initiates a Data Register read operation and clears the DRQ signal. If the Data Register is read after one or more characters are lost, by having new data transferred into the register prior to Processor or DMA readout, the lost data bit is set in the status register. The read operation continues until the end of sector is reached. The normal sector length for Read or Write operations with the IBM 3740 format is 128 bytes. This format or binary multiples of 128 bytes will be adopted by setting a logic 1 in Bit 3 of the Read Track and Write Track commands. Additionally, a variable sector length feature is provided which allows an indicator recorded in the ID Field to control the lenth of the sector. Variable sector lengths can be read or written in Read or Write commands respectively by setting a logic 0 in Bit 3 of the command word. The sector length indicator specifies the number of the 16 byte groups or 16 x N, where N is equal to 1 to 256 groups. An indicator of all zeros is interpreted as 256 sixteen byte groups.

3-50. DISK WRITE OPERATION

On disk write operations, the Data Request (DRQ) is activated at the start of the sector, and when the Data Register transfers its contents to the Data Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data. If new data is not loaded at the time the next serial byte is required by the flexible disk drive, a byte of zeros is written and the Lost Data bit is set in the Status Register. After data is loaded from the Processor into the Data Register, and is transferred to the Data Shift Register, data will be shifted serially through the Write Data (WD) output. Interlaced with each bit of data is a positive clock pulse of 0.5 microsecond duration. This output is

presented in inverted form to the disk drive (s). When Writing is to take place on the diskette, the Write Gate (WG) output is activated, allowing current flow into the Read/Write head. As a precaution to erroneous writing, the first data byte must be loaded into the Data Register in response to a Data Request before the Write Gate signal can be activated. Writing is inhibited when the Write Protect (WPRT) input is a logic 0, in which case any Write command is immediately terminated, INTRQ is activated, and the Write Protect status bit is set. Whenever a Read or Write command is received, the Controller chip samples the Ready input. If this input is logic 0, the command is not executed and INTRQ is activated. The Seek or Step commands are performed regardless of the state of the Ready input.

3-51. COMMANDS

The 1771 accepts and executes the eleven commands summarized in Table 3-2. Flags associated with these commands are summarized in Table 3-3. With the exception of the Force Interrupt command, a command word should be loaded into the internal Command Register only when bit 0 (Busy) of the Status Register is inactive (low). Whenever a command is being executed, the busy status bit is set high. When a command is completed or an error condition exists, the INTRQ signal is activated and the Busy status bit is reset low. The Status Register indicates whether a completed command is in error or was fault free. As indicated in Table 3-2, the eleven commands accepted and executed by the 1771 are divided into four types. The following paragraphs describe the eleven commands under these four divisions.

3-52. TYPE I COMMANDS

Type I Commands are basically head positioning commands and include the Restore, Seek, Step, Step-In, and Step-Out Commands. Each of the Type I Commands contains a rate (r1r0) field (bits 0 and 1) that determines the stepping motor rate as defined in Table 3-3.

TABLE 3-2.
FLOPPY CONTROLLER COMMAND SUMMARY

TYPE	COMMAND	7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r1	r0
I	Seek	0	0	0	1	h	V	r1	r0
I	Step	0	0	1	u	h	V	r1	r0
I	Step In	0	1	0	u	h	V	r1	r0
I	Step Out	0	1	0	u	h	V	r1	r0
II	Read Command	1	0	0	m	b	E	0	0
II	Write Command	1	0	1	m	b	E	a1	a0
III	Read Address	1	1	0	0	0	1	0	0
III	Read Track	1	1	1	0	0	1	0	s
III	Write Track	1	1	1	1	0	1	0	0
IV	Force Interrupt	1	1	0	1	I3	I2	I1	I0

TABLE 3-3.
FLOPPY CONTROLLER FLAG SUMMARY

TYPE I

h = Head Load Flag (Bit 3)

h=1, Load head at beginning

h=0, Do not load head at beginning

V = Verify Flag (Bit 2)

V=1, Verify on last track

V=0, No verify

r1r0 = Stepping Motor Rate (Bits 1-0)

r1	r0	CLK = 2 MHz (8" Drive)	CLK = 1 MHz (5" Drive)
0	0	6 ms	12 ms
0	1	6 ms	12 ms
1	0	10 ms	20 ms
1	1	20 ms	40 ms

u = Update Flag (Bit 4)

u=1, Update Track Register

u=0, No update

TYPE II

m = Multiple Record Flag (Bit 4)

m=0, Single Record

m=1, Multiple Records

b = Block Length Flag (Bit 3)

b=1, IBM format (128 to 1024 bytes)

b=0, Non-IBM format (16 to 4096 bytes)

E = Enable HLD and 10 msec Delay

E=1, Enable HLD, HLT and 10 msec Delay

E=0, Head is assumed Engaged and there is no 10 msec Delay

a1a0 = Data Address Mark (Bits 1-0)

a1a0=00, FB (Data Mark)

a1a0=01, FA (User defined)

a1a0=10, F9 (User defined)

a1a0-11, F8 (Deleted Data Mark)

TYPE III

s = Synchronize Flag (Bit 0)

s=0, Synchronize to AM

s=1, Do not synchronize to AM

TYPE IV

Ii = Interrupt Condition Flags (Bits 3-0)

I0=1, Not Ready to Ready Transition

I1=1, Ready to Not Ready Transition

I2=1, Index Pulse

I3=1, Immediate Interrupt

3-53. The Type I Commands contain a head load (h) flag (Bit 3) that determines whether or not the head is to be loaded at the beginning of the command. If h=1, the head is loaded at the beginning of the command (HLD output made active high). If h=0, the HLD output is made inactive/low. Once the head is loaded (HLD is active), the head will remain engaged until the controller receives a command that specifically disengages the head. If the Controller does not receive any commands after two revolutions of the disk, the head will be disengaged (HLD made inactive). The Head Load Timing (HLT) input is only sampled after a 10 millisecond delay, when actual reading or writing on the diskette is to occur. Note that a verification, described below, requires reading the diskette. Note further that many drives, with standard option strapping, requires the head to be loaded to perform Restore, Seek, and Step operations. Consult the drive vendor's literature for further details.

3-54. The Type I Commands also contain a verification (V) flag (Bit 2) that determines whether or not verification is to take place on the last track. If V=0, no verification is performed. If V=1, a verification is performed.

3-55. During verification, the head is loaded (HLD is active) and after an internal 10 millisecond delay, the HLT input is sampled. When the HLT input is active (high) the first encountered ID field is read from the disk. (Note that a external single shot is used to keep HLT inactive for 35 ms or greater). The track address of the ID field is then compared to the Track Register. If there is a match and a valid ID CRC, the verification is complete, INTRQ is activated, the Busy status bit is reset. If there is not a match but there is valid ID CRC, INTRQ is activated, the Seek Error status bit (Bit 4) is set high, and the Busy status bit is reset low.

If there is not a valid CRC, the CRC Error Status bit (Bit 3) is set high, and the next encountered ID field is read from the disk for verification. If an ID field with a valid CRC cannot be found after two revolutions of the disk the controller terminates the operation and activates the INTRQ signal.

3-56. The Step, Step In, and Step-Out commands an update (u) flag (Bit 4). When u=1, the Track Register is updated by one for each step. When u=0, the Track Register is not updated.

3-57. Restore (Seek Track 0). Upon receipt of this command, the Track 00 (TR00) input from the drive is sampled. If TR00 is active low (indicating the Read/Write head is positioned over Track 0), the Track Register is loaded with zeros and INTRQ is activated. If TR00 is not active low, stepping pulses at a rate specified by the r1r0 field (Bits 0 and 1) are issued until the TR00 is active low. At this time, the Track Register is loaded with zeros and INTRQ is activated. If the TR00 input does not go active low after 255 stepping pulses, the controller gives up and activates INTRQ with the Seek Error status bit set. Note that the Restore command is executed when the hardware Reset input goes from an active (low) to an inactive (high) state. A verification operation takes place if the V flag (Bit 2) is set. The setting of the h flag (Bit 3) allows the head to be loaded at the start of the command.

3-58. Seek. This command assumes that the Track Register contains the track number of the current position of the Read/Write head and that the Data Register contains the desired number. The controller will update the Track Register and issue stepping pulses in the appropriate direction until the contents of the Track Register are equal to the contents of the Data Register. A verification operation takes place if the V flag (Bit 2) is set. The set of the h flag (Bit 3) allows the head to be loaded at the start of the command. INTRQ is activated at the completion of the command.

3-59. Step. Upon receipt of this command, the controller issues one stepping pulse to the floppy disk drive. The stepping motor direction is the same as in

the previous step command. After a delay determined by the r1r0 field (Bits 0 and 1),a verification takes place if the V flag (bit 2) is set. If the u flag (Bit 4) is set, the Track Register is updated. The setting of the h flag (Bit 3) allows the head to be loaded at the start of the command. INTRQ is activated at the completion of the command.

3-60. Step-In. Upon receipt of this command, the controller issues one stepping pulse in the direction towards track 76. If the u flag (Bit 4) is set, the Track Register is decremented by one. After a delay determined by the r1r0 field (Bits 0 and 1), a verification takes place if the V flag (Bit 2) is set. The setting of the h flag (Bit 3) allows the head to be loaded at the start of the command. INTRQ is activated at the completion of the command.

3-61. Step-Out. Upon receipt of the command, the controller issues one stepping pulse in the direction towards track 0. If the u flag (Bit 4) is set, the Track Register is decremented by one. After a delay determined by the r1r0 field (Bits 0 and 1), a verification takes place if the V flag (Bit 2) is on. The setting of the h flag (Bit 3) allows the head to be loaded at the start of the command. INTRQ is activated at the completion of the command.

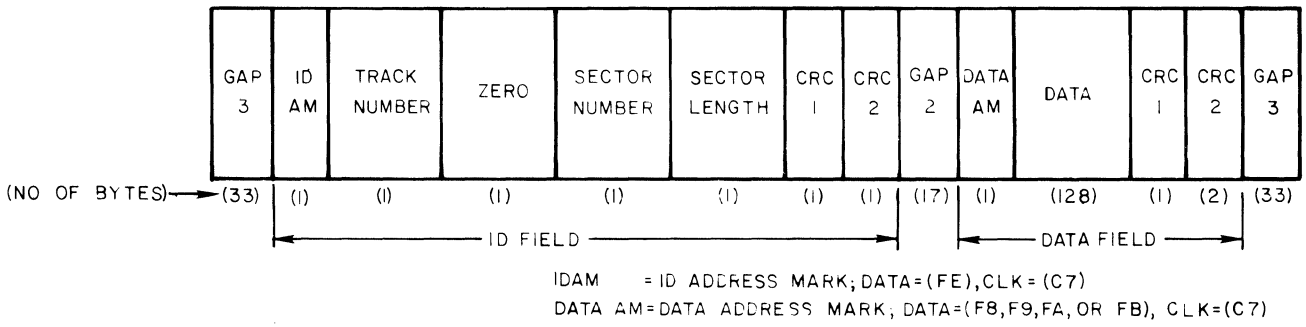
3-62. TYPE II COMMANDS

The Type II Commands include the Read sector(s) and Write sector(s) commands. Prior to loading the Type II Commands into the Command Register, the Processor must load the Sector Register with the desired sector number. Upon receipt of the Type II Commands, the Busy status bit is set. If the E flag (Bit 2) = 1 (this is the normal case), HLD is made active and HLT is sampled after an internal 10 millisecond delay. If the E flag = 0, the head is assumed engaged and there is no internal 10 millisecond delay.

3-63. Each sector is composed of an ID Field and Data Field as shown in Figure 3-12. When an ID Field is located on the diskette, the controller compares the Track Number of the ID Field with the Track Register. If there is not a match,

the next encountered ID Field is read and a comparison is made. If there is a match, the sector number of the ID Field is then compared with the Sector Register. If there is not a sector match, the next encountered ID Field is read and a comparison is made. If there is a match, the CRC field is read. (The polynomial for the CRC is $G(x) = x^{16} + x^{12} + x^{5} + 1$. The CRC includes all the information starting with the address mark and up to the CRC characters.) If there is a CRC error, the CRC Error status bit is set and the next ID Field is read off the diskette and comparisons are made. If the ID Field CRC is correct, the data field is located and will be either written or read, depending upon command. The controller must find an ID Field with a valid track number, sector number, and CRC within two revolutions of the disk; otherwise, the Record Not Found status bit (Bit 4) is set and the command is terminated with INTRQ activated.

FIGURE 3-12. IBM 3740 ID FIELD AND DATA FIELD FORMATS



3-64. Each of the Type II Commands contain a (b) flag (Bit 3), which in conjuction with the sector length field contents of the ID, determines the length (number of characters) of the data field. For IBM 3740 compatibility, the b flag (Bit 3) should equal 1. The numbers of bytes in the data field (sector) is then 128×2^n where n = 0, 1, 2, or 3.

For b = 1:

SECTOR LENGTH FIELD (HEX)	NUMBER OF BYTES IN SECTOR (DECIMAL)
00	128
01	256
02	512
03	1024

When the b flag (Bit 3) equals zero, the sector length field (n) multiplied by 16 determines the number of bytes in the sector or data field as shown below:

For b = 0:

SECTOR LENGTH FIELD (HEX)	NUMBER OF BYTES IN SECTOR (DECIMAL)
01	16
02	32
03	48
04	64
•	•
•	•
•	•
FF	4080
00	4096

3-65. Each of the Type II Commands also contains an m flag (Bit 4) that determines whether multiple records (sectors) are to be read or written; depending upon the command. If m=0, a single sector is read or written and INTRQ is activated at the completion of the command. If m=1, multiple records are read or written with the Sector Register internally updated so that an address verification can occur on the next record. The controller continues to read or write multiple records and update the Sector Register until the Sector Register exceeds the number of sectors on the track or until the Force Interrupt command is loaded into the Command Register. When either of these occurs, the command is terminated and INTRQ is activated.

3-66. Read Command. Upon receipt of this command, the Read/Write head is loaded and the Busy status bit is set. Then when an ID field is encountered that has the correct track number, correct sector number, and correct CRC, the data field is transferred to system RAM via the DMA Controller or Processor. The Data Address Mark of the data field must be found within 28 bytes of the correct ID field. If not, the Record Not Found status bit is set and the operation is terminated. When the first character or byte of the data field has been shifted through the Data Shift Register, it is transferred to the Data Register and a Data Request (DRQ) output is generated. When the next byte is loaded into the Data Shift Register, it is transferred to the Data Register and another DRQ output is generated, provided that the CPU or DMA Controller has previously read the Data Register. If one or more characters are lost, the Lost Data status bit is set. This sequence continues until the entire data field has been transferred. If there is a CRC error in the data field, the CRC Error status bit is set, and the command is terminated (even if it is a multiple record command). At the end of the operation, the type of Data Address Mark encountered in the data field is recorded in the Status Register (Bits 5 and 6) as shown below:

STATUS BIT 5	STATUS BIT 6	DATA AM (HEX)
0	0	FB
0	1	FA
1	0	F9
1	1	F8

3-67. Write Command. Upon receipt of this command, the Read/Write head is loaded (HLD active) and the Busy status bit is set. When an ID Field is encountered that has the correct track number, correct sector number and correct CRC, a DRQ output is generated. The controller counts off 11 bytes from the CRC field and the Write Gate (WG) output is made active if the DRQ has been serviced (i.e., the Data Register has been loaded by the Processor or DMA Controller). If the DRQ has not been serviced, the command is terminated and the Lost Data status bit is set. If the DRQ has been serviced, the WG is made active and six bytes of all Zero levels are then written on the diskette. At this time, the Data Address Mark is then written on the diskette, as determined by the a1a0 field (Bits 0 and 1) of the command as shown below:

a_1	a_0	DATA MARK (HEX)	CLOCK MARK (HEX)
0	0	FB	C7
0	1	FA	C7
1	0	F9	C7
1	1	F8	C7

The controller then writes the data field by generating DRQ outputs to the CPU/DMA Controller. If the DRQ is not serviced in time, the Lost Data status bit is set and a byte of zeros is written on the diskette. The command is not terminated. After the last byte has been written on the diskette, the two byte CRC has been computed internally and written on the disk followed by one byte of all One levels. WG is then made inactive.

3-68. TYPE III COMMANDS

3-69. Read Address. Upon receipt of this command, the head is loaded and the Busy status bit is set. The next encountered ID Field is then read in from the diskette, and the six data bytes of the ID Field are assembled and transferred to the Data Register, and a DRQ output is generated for each byte. (The six bytes of the ID Field are shown in Figure 3-12.)

3-70. Although the CRC characters are transferred to the computer, the controller checks for validity and the CRC Error status bit is set if there is a CRC error. The Sector Address of the ID Field is written into the Sector Register. At the end of the operation, INTRQ is activated and the Busy status is reset.

3-71. Read Track. Upon receipt of this command, the head is loaded and the Busy status bit is set. Reading starts with the leading edge of the first encountered index mark and continues until the next index pulse. As each byte is assembled, it is transferred to the Data Register and the Data Request (DRQ) output is generated for each byte. No CRC checking is performed. Gaps are included in the input data stream. If the s flag (Bit 0) of the command is low, the accumulation of bytes is synchronized to each Address Mark encountered. Upon completion of the command, the INTRQ is activated.

3-72. The controller handles single density frequency modulated (FM) data. Refer to Figure 3-13 and 3-14. Each data cell is defined by clock pulses. A pulse recorded between clock pulses indicates the presence of a logic 1 bit; the absence of this pulse is interpreted as a logic 0 bit. The Address Marks for Index, ID, and Data are identified by a particular pattern not repeated in the remainder of the ID Field or Data Field. This is accomplished by reading patterns that are recorded with missing clock bits (logic 0) as shown below:

Index Address Mark	Data 1 1 1 1 1 1 0 0 = FC
	Clock1 1 0 1 0 1 1 1 = D7
ID Address Mark	Data 1 1 1 1 1 1 1 0 = FE
	Clock1 1 0 0 0 1 1 1 = C7
Data Address Mark	Data 1 1 1 1 1 0 1 1 = F9 - FB
	Clock1 1 0 0 0 1 1 1 = C7
Deleted	Data 1 1 1 1 1 0 0 0 = F8
Data Address Mark	Clock1 1 0 0 0 1 1 1 = C7
Spare	Data 1 1 1 1 1 1 0 1 = FD
	Clock (User designated)

3-73. These patterns are used as synchronization code by the controller when reading data and are recorded by the formatting command (Write Track) when the controller is presented with data F8 through FE. The special code F7 as data in a Write Track operation is not itself recorded but serves as a command to the controller to write the accumulated CRC.

3-74. Write Track. Upon receipt of this command, the head is loaded and the Busy status bit is set. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse, at which time INTRQ is activated. The Data Request output is activated immediately upon receiving the command and writing does not start until after the first byte has been loaded into the Data Register. If the Data Register has not been loaded by the second index pulse, the operation is terminated. This sets the Not Busy and Lost Data status bits, and activates INTRQ. If a byte is not present in the Data Register when needed, a byte of zeros is substituted. Address Marks and CRC characters are written on the diskette by detecting certain data byte patterns in the data stream as shown above. The CRC generator is initialized to all Ones when any data byte from F8 to FE is about to be transferred from the Data Register to the Data Shift Register.

FIGURE 3-13. SINGLE DENSITY FM DATA PATTERN

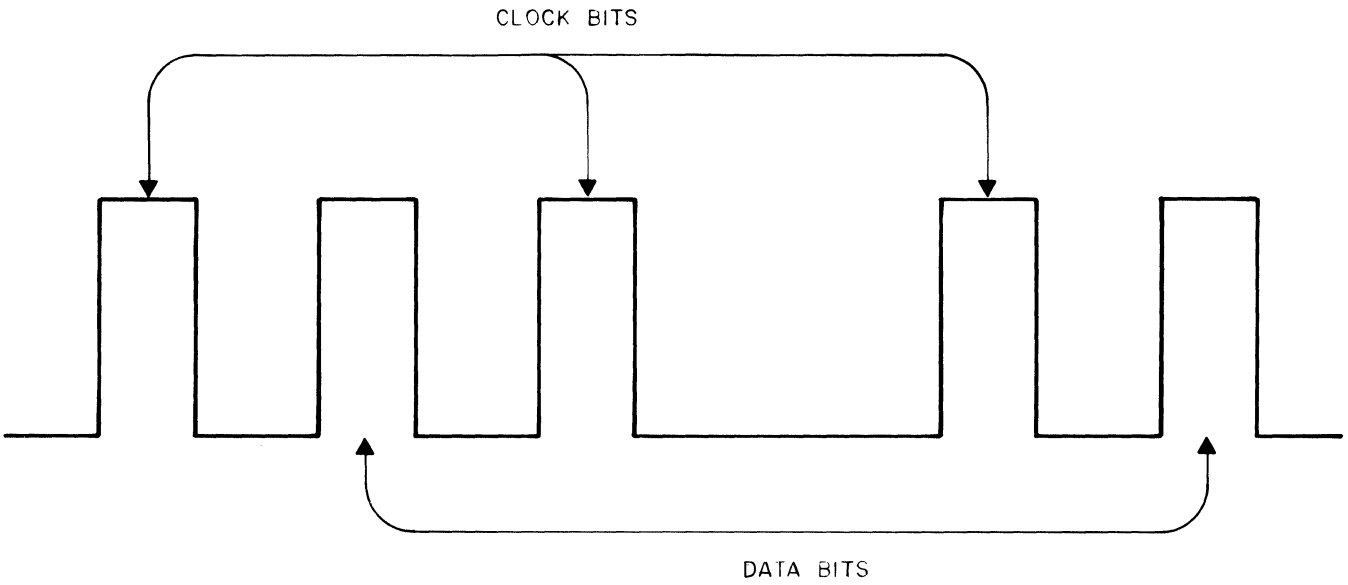
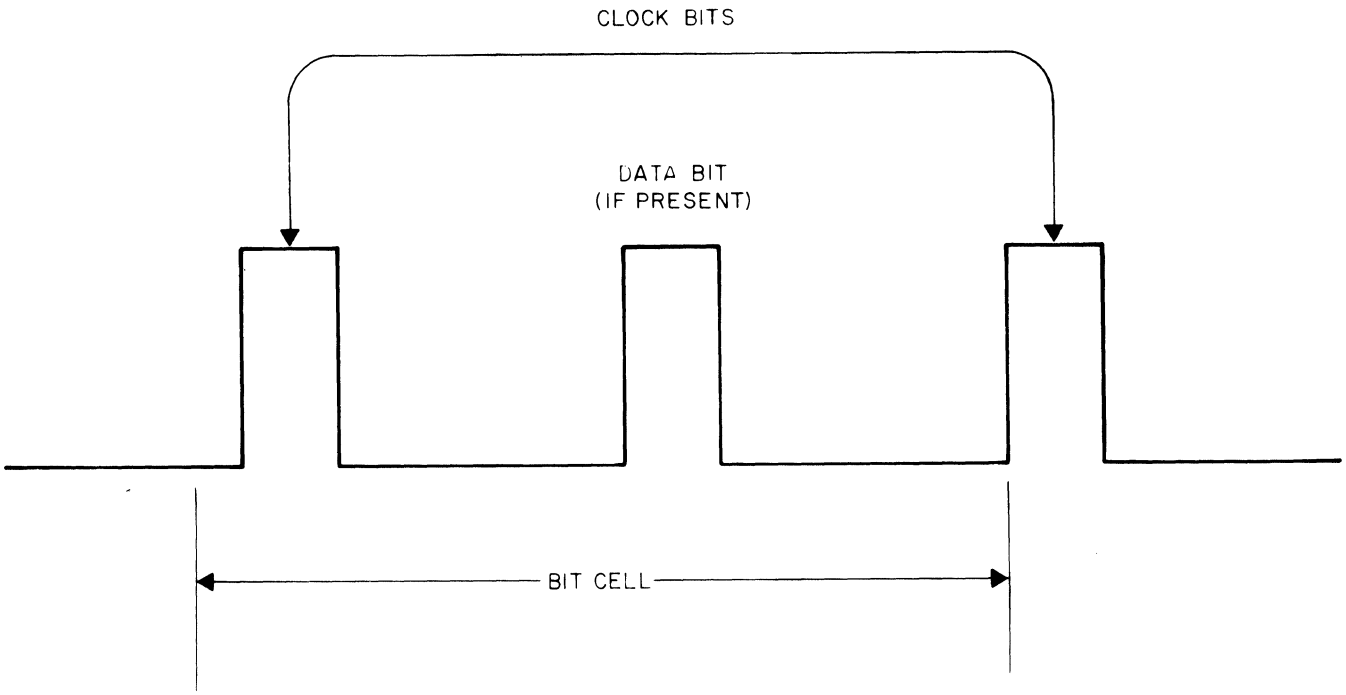


FIGURE 3-14. SINGLE DENSITY FM BIT CELL DEFINITION



CONTROL BYTES FOR INITIALIZATION

DATA PATTERN (HEX)	INTERPRETATION	CLOCK MARK (HEX)
F7	Write CRC Char.	FF
F8	Data Addr. Mark	C7
F9	Data Addr. Mark	C7
FA	Data Addr. Mark	C7
FB	Data Addr. Mark	C7
FC	Index Addr. Mark	D7
FD	Spare	
FE	ID Addr. Mark	C7

The Write Track command does not execute if the DINT input is grounded. Instead, the Write Protect status bit is set and INTRQ is activated. One F7 pattern in the Data Register generates 2 CRC characters.

3-75. TYPE IV COMMANDS

The force interrupt command can be loaded into the Command Register at any time. If there is a current command under execution (Busy status bit is set), the command is terminated and INTRQ is activated when the condition specified in the I_0 through I_3 field (Bits 0 through 3) is detected. More than one condition may be specified. The interrupt conditions are indicated below:

I_0 = Not Ready-to-Ready Transition
I_1 = Ready-to-Not-Ready Transition
I_2 = Every Index Pulse
I_3 = Interrupt occurs within 1 to 10 milliseconds and every 10 milliseconds thereafter

NOTE: If I_0 through I_3 = 0, no interrupt is generated; however, the current command is terminated and the Busy status bit is reset. Even when not busy, this command is useful to force the Status Register to "after Type I" mode.

3-76. STATUS REGISTER

An 8 bit register is provided in the controller to hold device status information. The status varies according to the type of command executed last. Tables 3-4, 3-5 and 3-6 summarize the information which can be read into the data bus by a read operation.

TABLE 3-4.
STATUS REGISTER SUMMARY

BIT	ALL TYPE I COMMANDS	READ ADDRESS	READ	READ TRACK	WRITE	WRITE TRACK
7	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY
6	WRITE PROTECT	0	RECORD TYPE	0	WRITE PROTECT	WRITE PROTECT
5	HEAD ENGAGED	0	RECORD TYPE	0	0	0
4	SEEK ERROR	ID NOT FOUND	RECORD NOT FOUND	0	RECORD NOT FOUND	0
3	CRC ERROR	CRC ERROR	CRC ERROR	0	CRC ERROR	0
2	TRACK 0	LOST DATA	LOST DATA	LOST DATA	LOST DATA	LOST DATA
1	INDEX	DRQ	DRQ	DRQ	DRQ	DRQ
0	BUSY	BUSY	BUSY	BUSY	BUSY	BUSY

TABLE 3-5.
STATUS BITS FOR TYPE I COMMANDS

BIT	NAME	MEANING
7	Not Ready	This bit when set indicates the drive is not ready. When reset it indicates that the drive is ready. This bit is an inverted copy of the READY input and logically 'ored' with Master Reset.
6	PROTECTED	When set, indicates Write Protect is activated. This bit is an inverted copy of WRPT input.
5	HEAD LOADED	When set, it indicates the head is loaded and engaged. The bit is a logical "and" of HLD and HLT signals.
4	SEEK ERROR	When set, the desired track was not verified. This bit is reset to 0 by loading a new command and by Master Reset.
3	CRC ERROR	When set, there was one or more CRC errors encountered on an unsuccessful track verification operation. This bit is reset to 0 by loading a new command and by Master Reset.
2	Track 00	When set, indicates Read Write head is positioned to Track 0. This bit is an inverted copy of the TR00 input.
1	INDEX	When set, indicates index mark detected from drive. This bit is an inverted copy of the IP input.
0	BUSY	When set command is in progress. When reset no command is in progress.

TABLE 3-6.
STATUS BITS FOR TYPE II AND III COMMANDS

	BIT NAME	MEANING
7	NOT READY	This bit when set indicates the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the READY input and 'ored' with Master Reset. The TYPE II and III Commands will not execute unless the drive is ready.
6	RECORD TYPE/ WRITE PROTECT	On Read Record: It indicates the MSB of record-type code from data field address mark. On Read Track: Not used. On Write or Write Track: It indicates Write Protection. This bit is reset by loading a new command and by Master Reset.
5	RECORD TYPE	On Read Record: It indicates the LSB of record-type code from data field address mark. On Read Track: Not used. This bit is reset by loading a new command or by Master Reset.
4	RECORD NOT FOUND	When set, it indicates that the desired track and sector were not found with correct CRC. This bit is reset by loading a new command or by Master Reset.
3	CRC ERROR	If S4 is set, an error is found in one or more ID fields; otherwise it indicates error in data field. This bit is reset by loading a new command or by Master Reset.
2	LOST DATA	When set, it indicates the computer did not respond to DRQ in one byte time. This bit is reset by loading a new command or by Master Reset.
1	DATA REQUEST	This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Read operation or the DR is empty on a Write operation. This bit is reset to zero by loading a new command or by Master Reset.
0	BUSY	When set, command is under execution. When reset, no command is under execution.

3-77. DATA PATH DESCRIPTION

During a Read or Write transfer, data is passed between the 1771 Controller and the Processor or DMA Controller via the 8-bit Data Bus.

3-78. The controller chip transforms 8-bit parallel data to or from single density frequency modulated (FM) data i.e. each data bit recorded has an associated clock bit associated with it. This information is sent to the flexible drive over the WRT DATA line on a write operation. On a read operation the data is received from the selected drive over the RD DATA line.

3-79. On a write operation, a byte of data is converted to serial data by the controller, then transferred to the disc drive with bit 0 first and bit 7 being transferred last.

3-80. On a read operation, bit 0 of each byte is transferred first with bit 7 last.

3-81. Read data entering the MDX-FLP controller is separated into clocks and data by the separator circuit and presented to the controller chip on pin 27 (FDDATA) and pin 26 (FDCLK). Note that it is not required that the separator circuit distinguish between presenting data or clocks to respective pins as long as a separation is made.

3-82. FORMATTING THE DISKETTE

Formatting the disk (See Table 3-7) is accomplished by first building a track image in memory, positioning the head over the desired track, issuing a write

track command and transferring the image to the desired track. The track image consists of the following format (sent to controller) for use with IBM format of 128 bytes/sector:

TABLE 3-7.
BYTE WRITE SEQUENCE TO BUILD A TRACK

	NUMBER OF BYTES		HEX VALUE OF BYTE WRITTEN
	40		00 or FF
	6	Gap	00
	1		FC (Index Mark)
	26		00 or FF
	6*		00
Each	1	ID	FE (ID Address Mark)
Sector	1	Field	Track Number (00 thru TT)
	1		00
	1		Sector Number (01 thru SS)
	1		00
	1		F7 (2 CRC's written by Controller Chip. See paragraph 4-61)
	11		00 or FF
	6		00
	1	Data	FB (Data Address Mark)
	128	Field	Data (IBM uses E5) May not be F7-FE.
	1		F7 (2 CRC's written by controller chip. See paragraph 4-61)
	27		00 or FF
	247**		00 or FF

* Write bracketed field SS times

** The length may vary due to track length tolerances.
For 8", TT=4CH, SS=1AH. For 5", TT=22H, SS=10H.

3-83. The Writing sequence continues from one index mark to the next index mark. Normally whatever data pattern appears in the Data Register is written on the disk with a clock mark of $(FF)_{16}$. However, if the controller detects a data pattern of F7 thru FE in the Data Register, this is interpreted as data address marks with missing clocks or CRC generation. For instance an FE pattern will be interpreted as an ID address mark (DATA FE, CLK C7) and the CRC will be intialized. An F7 pattern will generate two CRC characters. As a consequence, the patterns F7 thru FE must not appear in the gaps, data fields, or ID fields when using the Write Track command.

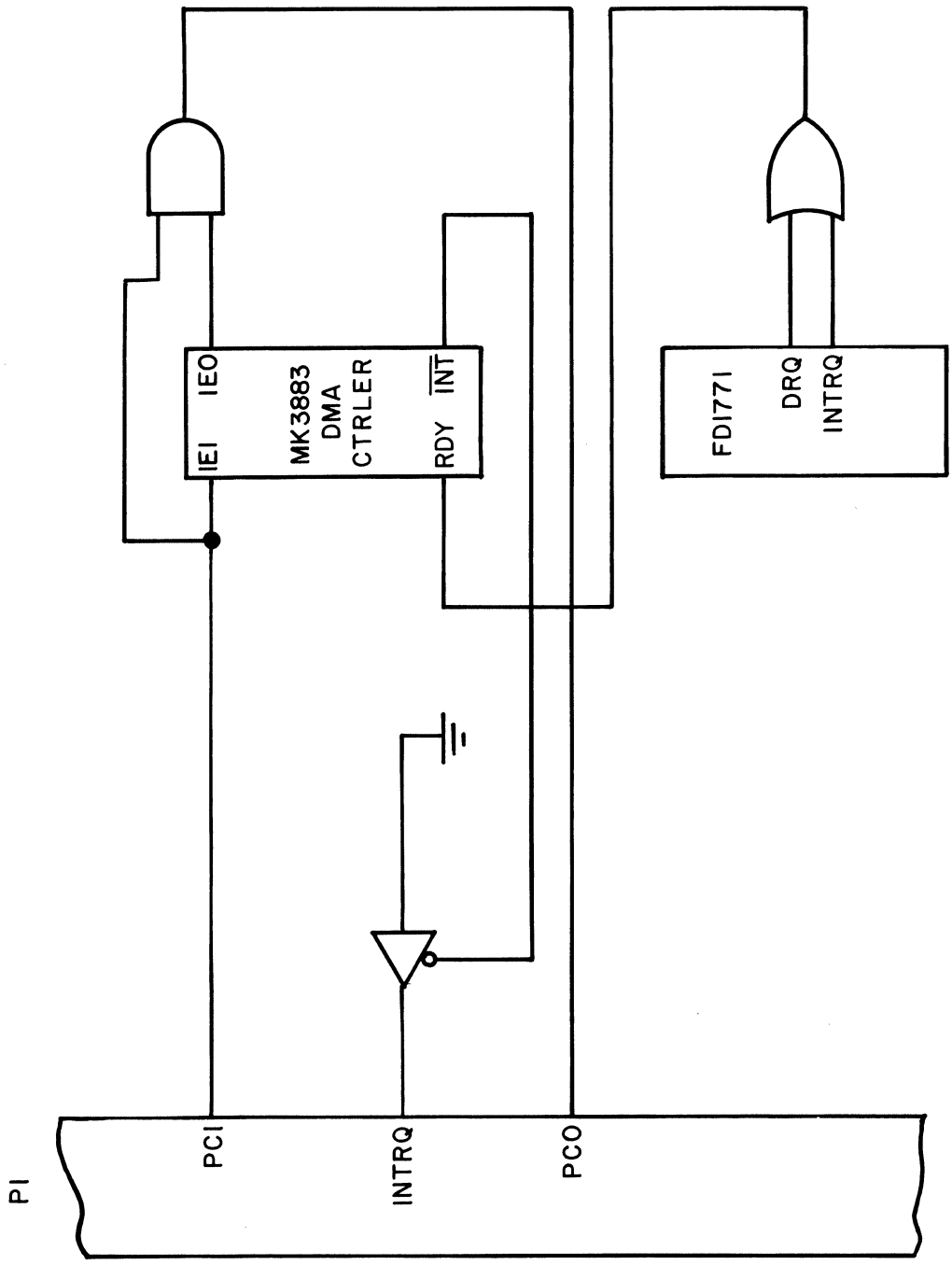
3-84. Z80 INTERRUPTS

The purpose of an interrupt is to allow an external event/device to suspend CPU operation in an orderly manner and force the CPU to start/resume a peripheral service routine. Usually this service routine is involved with the exchange of data, or status and control information, between the CPU and the peripheral. Once the service routine is completed, the CPU returns to the operation from which it was interrupted. The block diagram of this portion of MDX-FLP is shown in Figure 3-15. Mode 2 interrupts are supported by the MDX-FLP. This mode is the Z80's most powerful interrupt response mode. With a single 8-bit byte from the user an indirect call can be made to any memory location. With this mode the programmer maintains a table of 16 bit starting addresses for every interrupt service routine. This table may be located at any 256-byte boundary in memory. When an interrupt is accepted, a 16 bit pointer must be formed to obtain the desired interrupt service routine starting address from the table. The upper 8 bits of this pointer are formed from the contents of the I register. The lower eight bits of the pointer must be supplied by the interrupting device.

3-85. INTERRUPT PROCESS

When a command has been completed by the DMA controller chip, the chip will request an interrupt of the CPU. During this time the common interrupt line (INTRQ) will be pulled active low by the controller requesting the interrupt.

FIGURE 3-15. MDX-FLP INTERRUPT CIRCUITRY



Sometime later the CPU will send out an interrupt acknowledge INTAK. During INTAK the interrupt logic of the STD Bus and peripheral chips will determine the highest priority device which is requesting an interrupt. This device then places the contents of its 8-bit interrupt vector on the data bus for the CPU, and then releases its INTRQ. The MK3883 Device will inhibit lower priority interrupts until it decodes a RETI instruction or is given a RETI command.

If more than one peripheral chip requests interrupt service at the same time, a priority status is established. Priority is determined by the interrupt enable lines- IEI and IEO - and internal logic on each peripheral chip. The following table defines interrupt priority status:

IEI	IEO	STATUS
0	0	Higher priority device requesting interrupt
0	1	Undefined (not allowed)
1	0	Requesting interrupt with highest priority
1	1	No interrupt requested by this device

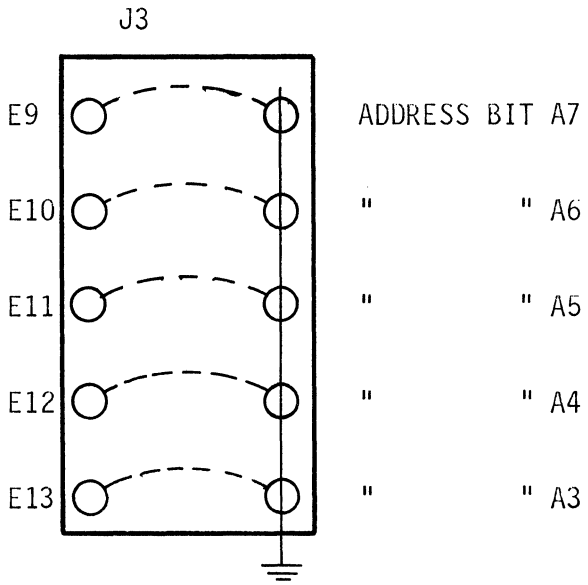
3-86. DAISY CHAIN

All Z80 peripheral devices include daisy chain priority interrupt logic that automatically supplies the programmed vector (from the highest priority interrupt in peripheral) to the CPU during interrupt acknowledge. To ensure that a number of such devices (from a speed standpoint) can be included in the interrupt priority loop, "look-ahead" logic has been implemented on the board.

3-87. ADDRESS STRAP OPTIONS

The board address is selected using wire wrap connections to ground the desired inputs in an 8131 digital comparator. These optional jumpers are located on J3. Table 3-8 below illustrates the possible address selection available. (Also see Figure 3-16)

TABLE 3-8.
ADDRESS STRAPPING



NOTE: CONNECTING A STRAP CAUSES THE BOARD TO RESPOND TO A LOGIC "0" IN THAT ADDRESS BIT, OTHERWISE TO A LOGIC "1". J3 IS SHIPPED WITH NO JUMPERS INSTALLED.

3-88. MINI/REGULAR DRIVE STRAP OPTIONS

The MDX-FLP board as shipped is configured for operation with 8" floppy disk drives. A set of jumper options must be selected for operation as a mini (5") controller. The Data Separator and Floppy Controller frequency is divided by two for a 5" drive by connecting the jumper located at E1 and disconnecting the jumper

located at E2. Since the Mini drive does not supply a 'Ready' signal it must be derived from the index pulse. This also requires a strap insertion, located at E6, and removal located at E7. In addition the Head Load timing must be extended for the 5" drive by removal of jumper E5. Last, the drive must be identified to software as a mini-floppy, by insertion of jumper E3. These jumpers are summarized in Table 3-9 and illustrated in Figure 3-16.

FIGURE 3-16. BOARD PHOTO SHOWING JUMPER OPTIONS

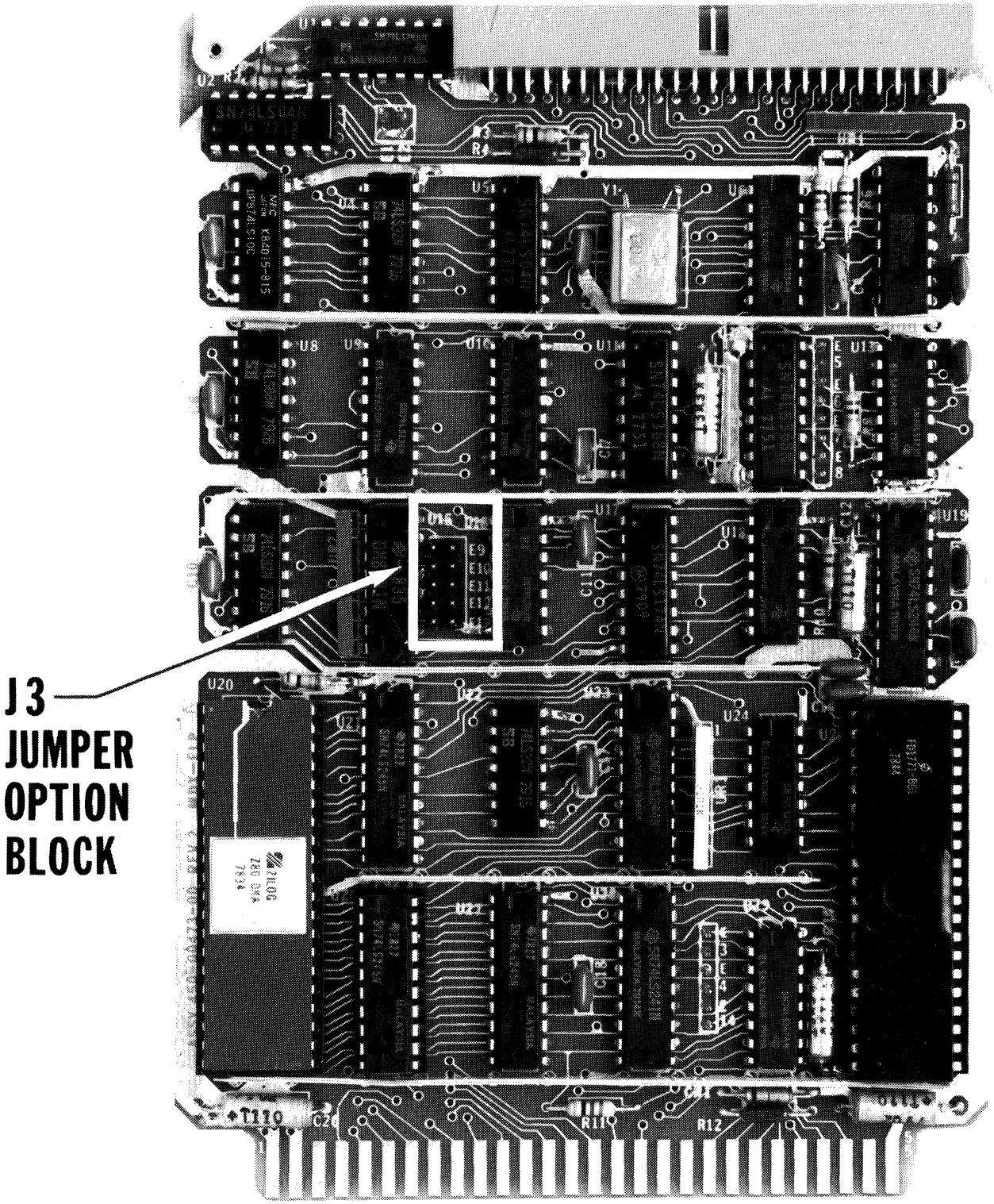


TABLE 3-9.
DRIVE-TYPE STRAPPING

DRIVE: JUMPER:	8"	5"
E1 E2 E3 E5 E6 E7 E8	OUT IN OUT IN OUT IN IN	IN OUT IN OUT IN OUT OUT
DRIVE: E4	SINGLE SIDED IN	DOUBLE SIDED OUT

3-89. SINGLE/DOUBLE SIDED STRAP OPTION

The MDX-FLP board as shipped is configured for operation with single-sided drives. Dual-Sided drives can be identified as such to software by removal of jumper E4. See Table 3-9 and Figure 3-16.

3-90. BUS GRANT DAISY CHAIN OPTION

The STD BUS does not allow for use of the daisy chain for multiple DMA devices on the same BUS. However, if the user is willing to give up the Status 0 pin (pin 40) the option exists on the MDX Series of Boards. On boards which do not control the bus, pins 40 and 41 may be jumpered to continue the chain. On the MDX-FLP Board the BUSAK signal is processed by the DMA controller and if it does not have the BUSRQ line pulled low, returns the signal BAO to the bus through a jumper option, to pin 40. This allows a Daisy chain similar to the interrupt chain (PCI, PCO) to be implemented if the user is willing to give up some compatibility to the STD BUS. This jumper is located at E14 on the MDX-FLP Board (Also shown in Figure 3-13).

SECTION 4

THEORY OF OPERATION

4-1. INTRODUCTION

Figure 1-2 is the general block diagram of the MDX-FLP board. Referring to this figure, notice the processor interface consists of a 8 bit bi-directional bus for data, status and control word transfer. An input buffer prevents excessive electrical loading on the STD-BUS. The floppy disk controller chip performs the control/transfer of data, status, and control information to the disk unit as well as communication with the STD-BUS. Data Transfer between the floppy disk controller and RAM on the STD-BUS is handled by the DMA controller.

4-2. I/O PORTS

The MDX-FLP board occupies a block of 8 contiguous I/O port addresses. This block can be located anywhere in the I/O port address space, by jumper option as described in paragraph 3-87. Thus, the value of port address bits A7-A3, to which the board responds, is determined by jumpers E9-E13 respectively. The following discussion deals only with the 3 least significant bits (A2-A0), as 000,001 ...111. Table 4-1 shows the utilization of the 8 ports.

TABLE 4-1. PORT UTILIZATION

A2:0	READ								WRITE							
000	MK3883 DMA CONTROLLER								MK3883 DMA CONTROLLER							
001	UNUSED								UNUSED							
010			8/5 INCH				1771 INT	2/1 SIDED	UNUSED							
011				SIDE SEL	DRV 4 MOTOR	DRV 3	DRV 2	DRV 1				SIDE SEL	DRV 4	DRV 3	DRV 2	DRV 1
100	1771 STATUS								1771 COMMAND							
101	1771 TRACK REG								1771 TRACK REG							
110	1771 SECTOR REG								1771 SECTOR REG							
111	1771 DATA REG								1771 DATA REG							

4-3. Port 000 is assigned to the 3883 DMA Controller chip. For a DMA data transfer operation, the DMA controller must be set up appropriately. For a control or programmed data transfer (e.g. Seek) operation in a polled (non-interrupt-driven) environment, the DMA Controller need not be set up. For a control operation in an interrupt driven environment, the DMA Controller must be set up for interrupt, because it is the only source of interrupts (1771 INTERRUPT presents Ready to the DMA Controller). Setup and handling of the DMA Controller is covered in Paragraphs 3-1 thru 3-34.

4-4. Port 001 is unused, but the MDX-FLP board will "answer" a Read command to this port (resulting data is undefined), so this port may not be used for any other purpose.

4-5. Port 010 is a read/input-only port which presents three bits of information to the processor (other bits are undefined).

B5: 1 = 8 inch drives; 0 = 5 inch drives.

B1: 1 = Interrupt request from 1771.

B0: 1 = Double sided drives; 0 = single sided,

B5 and B0 reflect jumper options E3 and E4 respectively. These are advisory flags to permit standard software/firmware to operate for all types of drives. If standard software is utilized, which senses B0 to determine the number of sides, all of the drives connected to one MDX-FLP board should have the same number of sides/heads. However, a double sided drive will operate correctly in single-sided mode.

The 1771 Interrupt Request (INTRQ) signal goes to a 1 at the completion or termination of any operation. This bit is redundant with the 1771 Status Register Busy bit (B0 in Read Port 100), with respect to sensing operation completion in a polled environment. INTRQ goes to a 1 less than one instruction time after BUSY goes to a 0. INTRQ is cleared by reading 1771 status (Port 100), and must be cleared by this means before an operation using the DMA Controller is initiated, since INTRQ is OR'ed with 1771 Data Request to activate (request) the DMA controller. Thus, in an interrupt-driven environment or when INTRQ is polled to sense completion, Port 100 should be read to clear INTRQ. One would probably want to do this anyway for error-checking.

When BUSY is polled to sense completion, one further Read of Port 100 should be done after the one which shows BUSY = 0, and before the next operation is initiated, to ensure that INTRQ is cleared. This could be a "front-end" check for Drive Ready before initiating the operation (see Port 100 Read description).

4-6. Port 011 is written into for drive selection and control, and can be read back to retrieve the same five bits of information (other bits are undefined on input, ignored on output). Since drives can be jumpered to interpret drive selection and control signals in various ways, the formal definition of these bits is as follows:

B4: 1 = activates (lowers) drive connector pin 14 and 16
B3: 1 = " " " " 32
B2: 1 = " " " " 30
B1: 1 = " " " " 28
B0: 1 = " " " " 26

A 0 in a bit position deactivates (raises) its signal.

4-7. PORT 011 STANDARD INTERPRETATION

Standard interpretation and drive jumpering is as follows:

B4: 1 = second side of 2-sided diskette, 0 = first side
B3: for 8", Drive Select 4
for 5", 1 = motor on; 0 = motor off
B2: Drive select 3
B1: " " 2
B0: " " 1

B4: Has no effect on single-sided drive.

B3: For 5" drives with standard jumpering, a 1 turns on the motor of all connected drives. When this bit is first set, a delay of one second is required before drives can be used. DRIVE SELECT lines are used by setting the bit corresponding to the desired drive to a one, the other bits to 0. Thus up to four 8" drives or three 5" drives can be connected to the one MDX-FLP board. The Drive Select signals are cleared to all 0/high by power-up or System Reset; thus a write to Port 011 to select the drive must be done before any operation can be initiated. The 1771 Floppy Disk Controller knows nothing about selection and reselection of drives, which can cause problems if certain programming disciplines are not observed, as follows:

1. The drive selected should not be changed while an operation is in progress.
2. When a particular drive is first selected, a Restore or Read Address operation should be performed, before any other operations, to fix the head position.
3. When changing drive selection in a multi-drive system, the following steps are recommended:
   a. Output the new drive selection to Port 011.
   b. Wait 35 milliseconds. (70ms for 5" drive) This delay allows the Head Load output of the 1771 (if true) to become effective on the new drive. Note the 35 ms one-shot controlling Head Load timing

is not effective in the case of drive reselection with the 1771 Head Load output true.

c. Issue a Read Address command to Port 100. This is a data-transfer command, and DMA or programmed I/O provision must be made to read 6 bytes of data.

d. On completion, if there are no errors, output the first byte of data read (track number) to Port 101, the 1771 Track Register. If there were errors, issue a Restore command to Port 100.

4-8. Port 100 is read to clear INTRQ and/or to acquire the 1771 Status register; the contents of which can vary depending on the previously performed operation. The two bits which are invariant regardless of previous operation are:

B7: 1 = Drive Not Ready; 0 = Ready

B0: 1 = 1771 Busy; 0 = Not Busy

See paragraph 3-76 for further description of 1771 Status contents.

4-9. Port 100 is written to send a command to the 1771. See paragraphs 3-51 thru 3-75 for 1771 commands. If the DMA controller is used (DMA read/write and/or interrupt at completion), it must be set up before the 1771 command is output. All commands except Force Interrupt with no conditions (0D0H) cause the BUSY bit in 1771 Status to set for a time; when the operation is completed, BUSY in Port 100 is cleared, INTRQ in Port 010 is set, and if the DMA Controller was so programmed, an interrupt is generated. A command should not be issued while a previous operation is in progress. While the 1771 allows the Force Interrupt with no conditions (0D0H) command to abort an operation in progress, the practice is discouraged in general, particularly for Write operations where it can lead to unreadable sectors. Note that it is not possible to read back the Command register from the 1771. If postoperation knowledge of the Command is required, it must be saved by the program.

4-10. Port 101 enables reading or writing of the 1771 Track Register. The Track Register can be read at any time, although its contents during a Restore operation are not actual track numbers. The Track Register should only be written into when reselecting drives as described in a previous section. In particular, writing into the Track Register does not accomplish seeking/head motion.

4-11. Port 110 enables reading or writing of the 1771 Sector Register. The desired (starting) sector number should be output to Port 110 before a Read or Write command is issued. The Sector Register is not updated by the 1771 except in "multiple sector" mode. It can be read at any time. The first sector on a track is 01.

4-12. Port 111 enables reading or writing of the 1771 Data Register. When the DMA Controller is used to handle data transfers between the 1771 Data Register and RAM on the STD-BUS, the only use of Port 111 by the Z80 program is to write the destination track number into the Data Register prior to initiating a Seek command.

4-13. NON-DMA DATA TRANSFER PROGRAMMING EXAMPLE

If the processor program can handle the data rate of the drive, it is possible to bypass the DMA Controller entirely and do data transfers directly between the processor and the Data Register. This is accomplished by disabling (not enabling) the DMA Controller via Port 000, issuing the 1771 Type II or III command to Port 100, monitoring the DRQ bit in Port 100 Status, and reading or writing Port 111 as appropriate when DRQ appears. Reading or writing Port 111 clears DRQ.

In this fashion, a tightly programmed loop with interrupts disabled can handle the data rate for a 5" (64 usec/byte) or 8" (32 usec/byte) on either a 2.5 MHZ or 4MHZ processor. Examples of Read and Write loops follow.

These examples assume:

- Drive Ready
- Controller Not Busy
- Seek done if required
- Track and Sector registers loaded
- Read or Write command issued to Command Reg.

```
; TRANSFER W/O DMA FOR WRITE DISK

      LD   HL,xfer ad          ; WHERE DATA LIVES IN RAM
      LD   D,0F6H              ; STATUS MASK
      LD   B,128               ; SECTOR LENGTH
      LD   C,PORT+7            ; PORT # OF 1771 DATA REG

WX:   IN   A, (PORT+4)         ; GET 1771 STATUS
      AND  D                   ; MASK TO IGNORE BUSY, CRC ER
      JR   Z, WX-$             ; LOOP IF NO INTERESTING FLAG
      OUTI                     ; OUTPUT (HL), STEP HL, DECR B
      JP   NZ, WX              ; LOOP IF (B) NOT DOWN TO 0

;  ON EXIT, WAIT FOR DONE, CHECK STATUS

;  TRANSFER W/O DMA FOR READ DISK

      LD   HL, xfer ad         ; WHERE DATA IS TO GO IN RAM
      LD   D, 3                ; STATUS MASK FOR DRQ, BUSY
      LD   E, 1                ; MASK TO COMPLEMENT BUSY
      LD   B, 128              ; SECTOR LENGTH
      LD   C, PORT+7           ; PORT # OF 1771 DATA REG

RX:   IN   A, (PORT+4)         ; GET 1771 STATUS
      XOR  E                   ; COMPL. BUSY TO "DONE"
```

```
      AND   D                       ; MASK TO DRQ AND DONE
      JR    Z, RX-$                 ; LOOP IF NEITHER DRQ NOR DONE
      INI                           ; INPUT (HL), STEP HL, DECR B
      JP    NZ, RX                  ; LOOP
; ON EXIT, WAIT FOR DONE, CHECK STATUS
```

4-14. INTERFACES

4-15. **PROCESSOR INTERFACE.** The interface to the processor is the STD-Z80-BUS. The following signals are used by the MDX-FLP board. Input/Output designations are referenced to the MDX-FLP board.

STD-Z80 BUS DESCRIPTION

BUS PIN	MNEMONIC	DESCRIPTION
1	+5V	+5Vdc system power
2	+5V	+5Vdc system power
3	GND	Ground-System signal ground and DC return
4	GND	Ground-System signal ground and DC return
5	-5V	-5VDC system power (NOT USED BY MDX-FLP)
6	-5V	-5VDC system power (NOT USED BY MDX-FLP)
7	D3	
8	D7	
9	D2	Data Bus (Tri-state, input/output,active high). D0-D7
10	D6	constitute an 8-bit bi-directional data bus. The data
11	D1	bus is used for data exchange with memory and I/O
12	D5	devices.
13	D4	
14	D3	
15	A7	
16	A15	
17	A6	
18	A14	
19	A5	
20	A13	Address Bus (Tri-state, input, output, active high).
21	A4	A0-A15 make up a 16-bit address bus.The address bus
22	A12	provides the address for memory (up to 65K bytes)data
23	A3	exchanges for I/O device data exchanges. I/O addressing
24	A11	uses the lower 8 address bits to allow the user to
25	A2	directly select up to 256 input or 256 output ports.
26	A10	A0 is the least significant address bit. During refresh
27	A1	time, the lower 7 bits contain a valid refresh address for dynamic memories.

BUS	PIN	DESCRIPTION
28	A9	
29	A0	
30	A8	
31	$\overline{WR}$	Write (Tri-state, input/output, active low) WR indicates that the CPU data bus holds valid data to be stored in the addressed memory or I/O device.
32	$\overline{RD}$	Read (Tri-state, input/output active low). RD indicates that the CPU wants to read data from memory or an I/O device. The addressed I/O device or memory should use this signal to gate data onto the CPU data bus.
33	$\overline{IORQ}$	Input/Output Request (Tri-state, input/output, active low). The IORQ signal indicates that the lower half of the address bus holds a valid I/O address for an I/O read or write operation. An IORQ signal is also generated with an M1 signal when an interrupt is being acknowledged to indicate that an interrupt response vector can be placed on the data bus. Interrupt Acknowledge operations occur during M1 time, while I/O operations never occur during M1 time.
34	$\overline{MEMRQ}$	Memory Request (Tri-state, output, active low). Not used by MDX-FLP. The MEMRQ signal indicates that the address bus holds a valid address for a memory read or memory write operation.
35	$\overline{IOEXP}$	I/O Expansion, not used on MDX cards. Not used by MDX-FLP. (Normally strapped to ground on the MOSTEK motherboard).
36	$\overline{MEMEX}$	Memory Expansion, not used on Mostek MDX cards. Not used by MDX-FLP. (Normally strapped to ground on the MOSTEK motherboard).

BUS	PIN	DESCRIPTION
37	$\overline{\text{REFRESH}}$	REFRESH (Tri-state, output, active low). REFRESH indicates that the lower 7 bits of the address bus contain a refresh address for dynamic memories and the MEMRQ signal should be used to perform a refresh cycle for all dynamic RAMs in the system. During the refresh cycle A7 is a logic 0 and the upper 8 bits of the address bus contains the I register
38	$\overline{\text{MCSYNC}}$	Not generated on the MOSTEK MDX-CPU1. Not used by MDX-FLP. Can be generated by gating the following signals: RD+WR+INTAK. By connecting a jumper on the MDX-CPU1, this line becomes DEBUG (Input). DEBUG is used in conjunction with the DDT-80 operating system on the MDX-DEBUG card, and the MDX-SST card for implementing a hardware single step function. When pulled low, the DEBUG line will set an address modification latch which will force the upper three address lines A15, A14, and A13 to a logic 1. These address lines will remain at a logic 1 until reset by performing any I/O operation.
39	$\overline{\text{STATUS 1}}$ (M1)	Machine Cycle one. (Tri-state, input active low). M1 indicates that the current machine cycle is in the op code fetch cycle of an instruction. Note that during the execution of two-byte op-codes M1 will be generated as each op-code is fetched. These two-byte op-codes always begin with a CBH, DDH, EDH, or FDH. M1 also occurs with IORQ to indicate an interrupt acknowledge cycle.
40	$\overline{\text{STATUS 0}}$	Normally not used on Mostek MDX cards. Can be connected by on-card jumper E14 to Bus Acknowledge Out (Output, active low).

BUS	PIN	DESCRIPTION
41	$\overline{\text{BUSAK}}$	Bus Acknowledge (Input, active low). Bus Acknowledge is used to indicate to the requesting device that the CPU address bus, data bus, and control bus signals have been set to their high impedance state and the external device can now control the bus.

NOTE: If more than one DMA device is to be operated simultaneously, the backplane should be modified as follows: cut the BUSAK trace between the slots for the first (i-th) and second (i+1-st) DMA board, and wire STATUS0 from the first (i-th) board slot to the BUSAK for the second (i-th) slot. To preserve slot independence, the BUSAK trace can be completely removed, and pin 40 of each connector can be connected to pin 41 of the next, in the same direction as pin 51 (PCO) to pin 52 (PCI) respectively.

42	$\overline{\text{BUSRQ}}$	Bus Request (Output,active low). The BUSRQ signal is used to request the CPU address bus, data bus, and control signal bus to go to a high impedance state so that other devices can control those buses. When BUSRQ is activated, the CPU will set these buses to a high impedance state as soon as the current CPU machine cycle is terminated and the BUSAK signal is activated.
43	$\overline{\text{INTAK}}$	Interrupt Acknowledge (Tri-state, input, active low). The INTAK signal indicates that an interrupt acknowledge cycle is in progress,and the interrupting device should place its response vector on the data bus. The INTAK signal is equivalent to an IORQ during an M1.
44	$\overline{\text{INTRQ}}$	Interrupt Request (Output,active low). The Interrupt Request signal is generated by I/O devices. A request will be honored at the end of the current instruction

BUS	PIN	DESCRIPTION
		if the internal software controlled interrupt enable flip flop (IFF) is enabled and if the BUSRQ signal is not active. When the CPU accepts the interrupt, an interrupt acknowledge signal INTAK (IORQ during an M1) is sent out at the beginning of the next instruction.
45	$\overline{\text{WAITRQ}}$	Wait Request (Input, active low). Wait Request indicates to the CPU/DMA that the addressed memory or I/O device is not ready for a data transfer. The CPU continues to enter wait states for a long as this signal is active. This signal allows memory or I/O devices of any speed to be synchronized to the CPU/DMA. Use of this signal postpones refresh as long as it held active.
46	$\overline{\text{NMIRQ}}$	Non-Maskable Interrupt Request (input, negative edge triggered). Not used by MDX-FLP. The Non-Maskable Interrrupt Request line has a higher priority than the INTRQ line and is always recognized at the end of the current instruction, independent of the status of the interrupt enable flip-flop. NMIRQ automatically forces the CPU to restart to location 0066h. The program counter is automatically saved in the external stack so that the user can return to the program that was interrupted. Note that continuous WAIT cycles can prevent the current instruction from ending and that a BUSRQ will override a NMIRQ.
47	$\overline{\text{SYSRESET}}$	System Reset (Input, active low). System Reset line indicates that a reset has been generated either from an external reset or the power on reset circuit. The system reset will occur only once per reset request

		and will be approximately 2 microseconds in duration. A system reset will also force the CPU program counter to zero,disable interrupts, set the I register to 00H, set the R register to 00H, and set Interrupt Mode 0.
48	$\overline{\text{PBRESET}}$	Push Button Reset (Input, active low). Not used by MDX-FLP. The Push Button Reset will generate a debounced system reset.
49	$\overline{\text{CLOCK}}$	Processor Clock (Input, active low). Single phase system clock.
50	$\overline{\text{CNTRL}}$	Not used on MOSTEK MDX cards.
51	$\overline{\text{PCO}}$	Priority Chain Output (Output, active high). The signal is used to form a priority-interrupt daisy chain when more than one interrupt driven device is being used. A high level on this pin indicates that no other devices of higher priority are being serviced by a CPU interrupt service routine.
52	$\overline{\text{PCI}}$	Priority Chain In (Input, active high). This signal is used to form a priority-interrupt daisy chain when more than one interrupt-driven device is being used. A high level on this pin indicates that no other devices of higher priority are being serviced by a CPU interrupt service routine.
53	AUX GND	Auxiliary Ground (Bussed)
54	AUX GND	Auxiliary Ground (Bussed)
55	+12V	+12Vdc system power
56	-12V	-12Vdc system power

4-16. DRIVE INTERFACE

MDX-FLP is compatible with the following floppy disk drives:

Siemens FDD 100-8, 200-8, 100C, 200C.
Shugart Associates SA800, SA850, SA450.
Pertec FD600, FD650, FD200, FD250.
Memorex 550, 552.

and with any equivalent drive which utilizes the following signals: (All signals are TTL; directions are referenced to the board.)

MDX-FLP CONNECTOR: 50 pin, Ansley 609-5000 or equivalent.

SIGNAL	DIRECTION	MDX-FLP PIN
Drive Select 1,2,3,4	O	26, 28, 30, 32
Side Select	O	14 and 16
Step	O	36
Write Data	O	38
Write Gate	O	40
Direction	O	34
Head Load	O	18
Read Data	I	46
Index	I	24 (5") or 20 (8")
Track 0	I	42
Write Protect	I	44
Drive Ready	I	22

The MDX-FLP can control up to four 8" drives or up to three 5" drives.

4-17. The drive interface consists of signal buses daisy chained from drive to drive with termination on the last drive. The interface driver/receivers are diagrammed in Figure 4-1. The driver is an open collector output buffer with pull up resistor on the last daisy chained drive serving as a terminator. The DRIVE SEL lines determine which flexible disk drive will respond to the bus. Jumpers on each individual drive determines the unit number configuration. A diagram showing a typical selection scheme is shown in Figure 4-2.

4-18. For 5" drives, the role of the Drive Select 4 signal is changed to Motor On. When Motor On is asserted low/true, the motor(s) of (all) connected drive(s) run. When Motor On is first asserted, the program must wait 1 second to allow drive(s) to come up to speed. No hardware timing is provided for Motor On or Off.

4-19. The method of motion control is by sending a level over the DIRECTION line and pulses over the STEP line to determine the motion and stepping rate for the step-direction motor within the flexible disk drive unit.

4-20. The head is loaded against the media (diskette) by the HLD (HEAD LOAD) signal. A read or write does not occur until a time out delay of 35 to 40 ms has occurred after head load. Note that the flexible disk drive does not load the head upon being selected, instead a separate head load signal (HLD) is used. (8" only). The Mini disk drives load the head when selected, ignoring the HLD signal.

4-21. When reading serial data from the disk, the MDX-FLP will look for the desired sector to be read, check its ID field and locate its data address mark. All subsequent serial data is assembled in parallel form and output to the DMA CTLR or processor. The serial data read from the flexible diskette drive is input to the MDX-FLP in the form of composite data in which the data and clocks are

FIGURE 4-1. DRIVE MULTIPLEXED SIGNALS

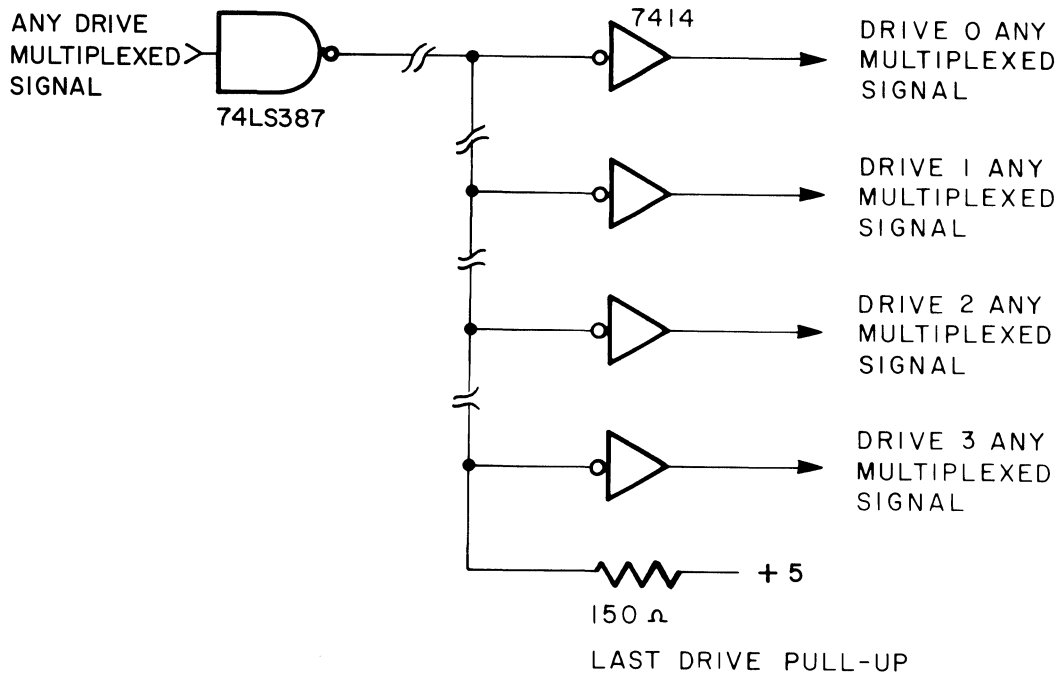
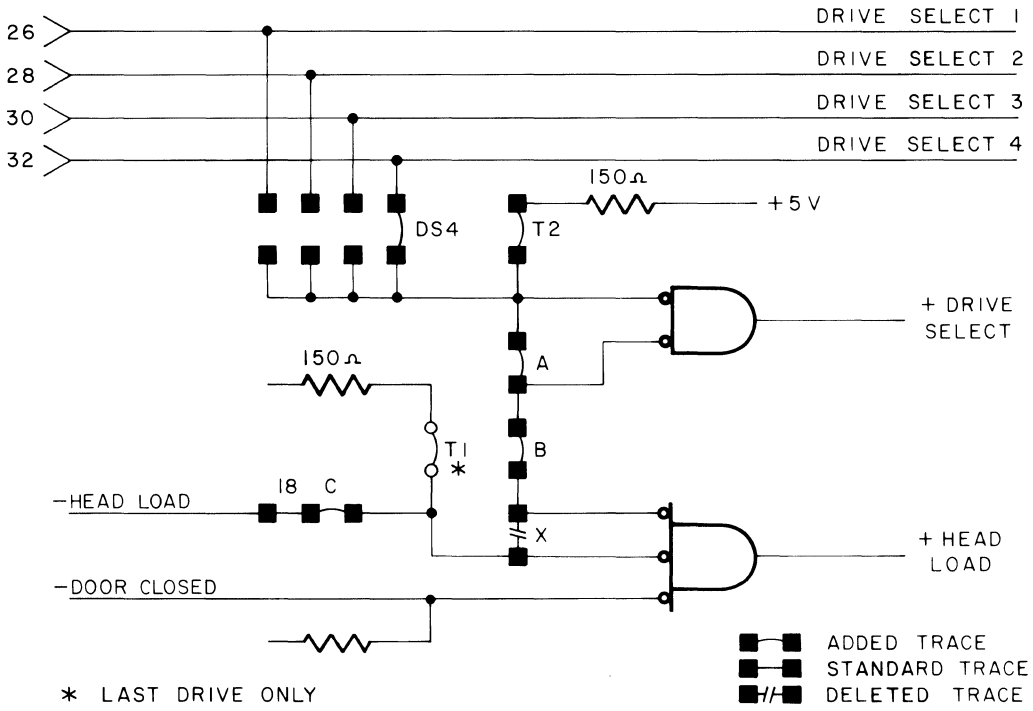


FIGURE 4-2. TYPICAL SELECTION LOGIC (IN DRIVE)



presented to the RD DATA input. a separator within the MDX-FLP separates the data and clocks then presents them separately to the controller chip.

4-22. When writing, information is presented as composite of serial clock and data pulses. With data present at the WRT DATA output, the WRT GATE signal is activated to allow write current to flow in the Read/Write head.

4-23. The remaining interface lines concern status information. The INDEX signal indicates when the index mark is encountered once per revolution. The (TR00) Track 00 signal indicates when the Read/Write head is located over Track 00. The (WPRT) WRITE PROTECT signal when active prevents the executing of a write command when a read-only diskette is installed. For 8" drives, the READY signal indicates the flexible drive readiness and an inactive signal prevents any read or write command from being executed. For 5" drives, the READY condition is synthesized from the presence of index pulses.

4-24. FLEXIBLE DISK DRIVES OPTIONS

The flexible disk drives must be configured to the correct options for use with the MDX-FLP hardware and system software. See the drive manufacturer's literature for details. The features that should be installed in the drives used with the MDX-FLP are the following:

1. Multiplexed I/O lines with up to four separate drive select lines.
2. Soft Sectoring
3. Step/direction stepper motor interface.

Drive features which are optional to the MDX-FLP.

1. Activity light.
2. Door lock.
3. Drive select and enable stepper without loading head option.

Features not supported by MDX-FLP board but found on some manufacturers disc units:

1. WRITE FAULT indication
2. Double track density
3. Data separator in drive
4. Power Saver
5. Double track indication
6. Diskette type indication
7. Track 43 (low current)

SECTION 5

SPECIFICATIONS

5-1. ELECTRICAL SPECIFICATIONS

DATA BUS - 8 bits, bidirectional

ADDRESS BUS - 16 bits, lower 8 bidirectional, upper 8 output during DMA activity

SYSTEM BUS - STD-Z80 Compatible (See Table A-1)

Inputs - One 74 LS Load Max

Outpus - I_{OH} = -15 mA min at 2.5V

I_{OL} = -24 mA min at .5V

SYSTEM CLOCK

MDX-FLP - 2.5 MHz

I/O ADDRESSING

8 ports on board selectable to any of 32 - 8 port slots by Jumper options.

MEM ADDRESSING

On board DMA capable of addressing any memory address (Note: MDX-CPU1 does not allow external addressing of its scratch pad memory).

POWER REQUIREMENTS

+12 $\pm$ 5% @ 10 mA max

+5V $\pm$ 5% @ 1.2 max

-12V $\pm$ 5% (-5V derived from this supply) @ 4mA max

OPERATING TEMPERATURE

0°C to 50°C

5-2. MECHANICAL SPECIFICATIONS

CARD DIMENSIONS

4.5 in (11.43 cm) high by 6.50 in (16.51 cm) long

0.48 in (1.22 cm) maximum profile thickness

0.062 in (.16 cm) printed circuit board thickness

CONNECTORS	#PINS	CENTER (IN.)	MATING CONNECTOR
STD BUS (P1)	56	.125	P.C. 3VH28/ICE5 (Viking) Soldertail 3VH28/ICN5 (Viking) W. W. 3VH28/ICND5 (Viking)
DRIVE INTERCONNECT (J2)	50	.100	(Ansley)609-5000 W/O Strain Relief (Ansley)609-5001 with Strain Relief

APPENDIX A

FACTORY REPAIR WARRANTY

APPENDIX A

FACTORY REPAIR SERVICE

In the event that difficulty is encountered with this unit, it may be returned directly to MOSTEK for repair. This service will be provided free of charge if the unit is returned within the warranty period. However, units which have been modified or abused in any way will not be accepted for service, or will be repaired at the owner's expense. When returning a circuit board, place it inside the conductive plastic bag in which it was delivered to protect the MOS devices from electrostatic discharge. THE CIRCUIT BOARD MUST NEVER BE PLACED IN CONTACT WITH SYTROFOAM MATERIAL. Enclose a letter containing the following information with the returned circuit board.

Name, address, and phone number of purchaser
Data and place of purchase
Brief description of the difficulty

Mail a copy of this letter SEPARATELY to:

In USA:

MOSTEK Corporation
Microcomputer Service Manager
1215 West Crosby Road
Carrollton TX, 75006

OUTSIDE USA:

Please address the letter and board to the Mostek office or representtive in your country.

Securely package and mail the circuit board, prepaid and insured, to the same address.

LIMITED WARRANTY

MOSTEK warrants this product against defective materials and workmanship for a period of 90 days. This warranty does not apply to any product that has been subjected to misuse, accident, improper installation, improper application, or improper operation, nor does it apply to any product that has been repaired or altered by other than an authorized factory representative.

There are no warranties which extend beyond those herein specifically given.

NOTICE

This antistatic bag is provided for shipment of the Mostek PC boards to prevent damage to the components due to electrostatic discharge.

Failure to use this bag is shipment will VOID the warranty.

TABLE A-1 P1 CONNECTOR PINOUT (STD Z80 BUS)

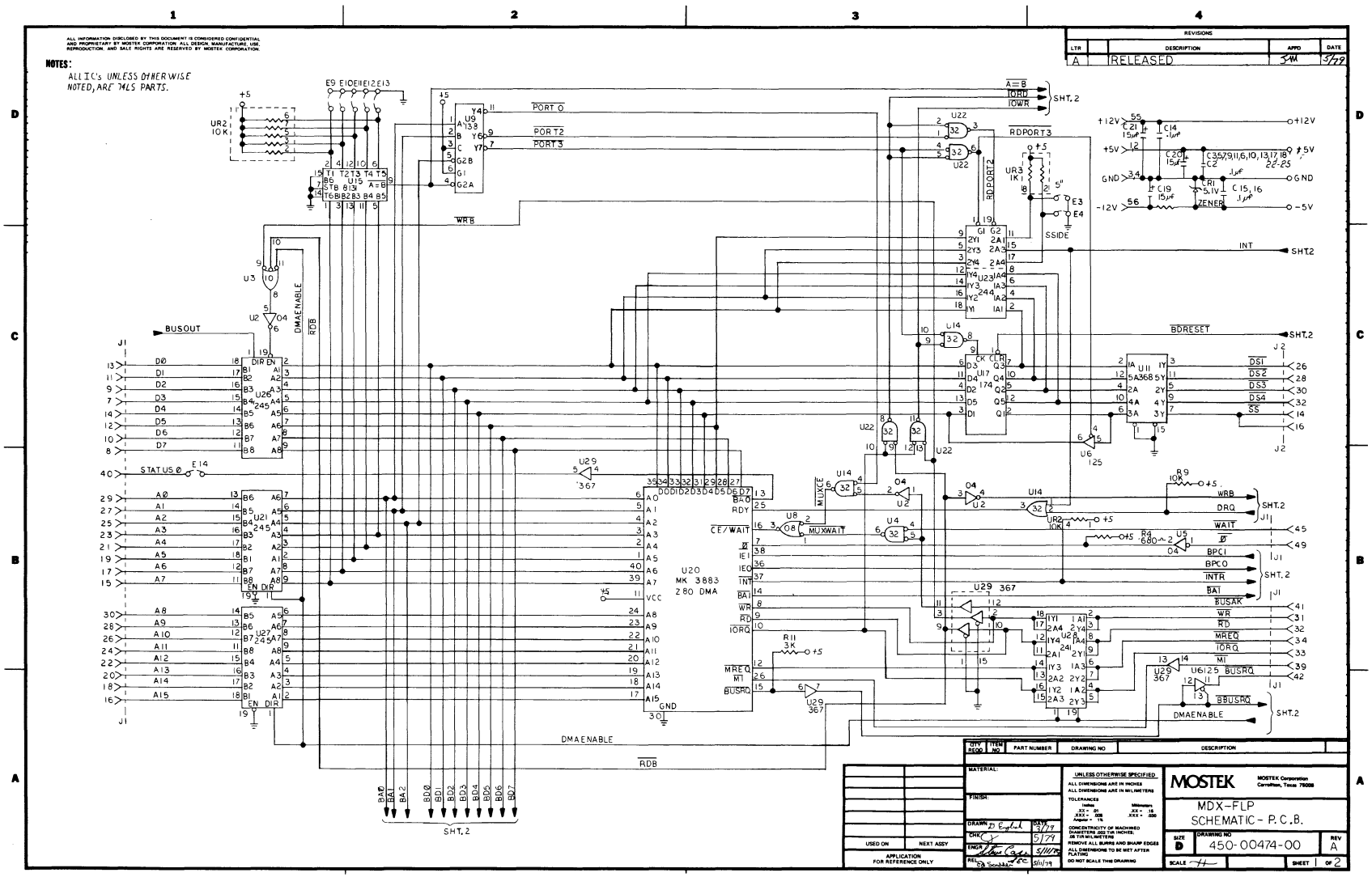
	Component Side				Circuit Side			
	Pin	Mnemonic	Signal Flow	Description	Pin	Mnemonic	Signal Flow	Description
Logic Power	1	+5V	In	+5 Volts DC (Bussed)	2	+5V	In	+5 Volts DC (Bussed)
	3	GND	In	Digital Ground (Bussed)	4	GND	In	Digital Ground (Bussed)
					6			
Data Bus	7	D3	In/Out	Low Order Data Bus	8	D7	In/Out	High Order Data Bus
	9	D2	In/Out	Low Order Data Bus	10	D6	In/Out	High Order Data Bus
	11	D1	In/Out	Low Order Data Bus	12	D5	In/Out	High Order Data Bus
	13	D0	In/Out	Low Order Data Bus	14	D4	In/Out	High Order Data Bus
Address Bus	15	A7	In/Out	Low Order Address Bus	16	A15	Out	High Order Address Bus
	17	A6	In/Out	Low Order Address Bus	18	A14	Out	High Order Address Bus
	19	A5	In/Out	Low Order Address Bus	20	A13	Out	High Order Address Bus
	21	A4	In/Out	Low Order Address Bus	22	A12	Out	High Order Address Bus
	23	A3	In/Out	Low Order Address Bus	24	A11	Out	High Order Address Bus
	25	A2	In/Out	Low Order Address Bus	26	A10	Out	High Order Address Bus
	27	A1	In/Out	Low Order Address Bus	28	A9	Out	High Order Address Bus
	29	A0	In/Out	Low Order Address Bus	30	A8	Out	High Order Address Bus
Control Bus	31	$\overline{WR}$	In/Out	Write to Memory or I/O	32	$\overline{RD}$	In/Out	Read to Memory or I/O
	33	$\overline{IORQ}$	In/Out	I/O Address Select	34	$\overline{MEMRQ}$	In/Out	Memory Address Select
	35							
	37							
	39	$\overline{STATUS\ 1}$	In	CPU Status (M1)				
	41	$\overline{BUSAK}$	In	Bus Acknowledge	42	$\overline{BUSRQ}$	Out	Bus Request

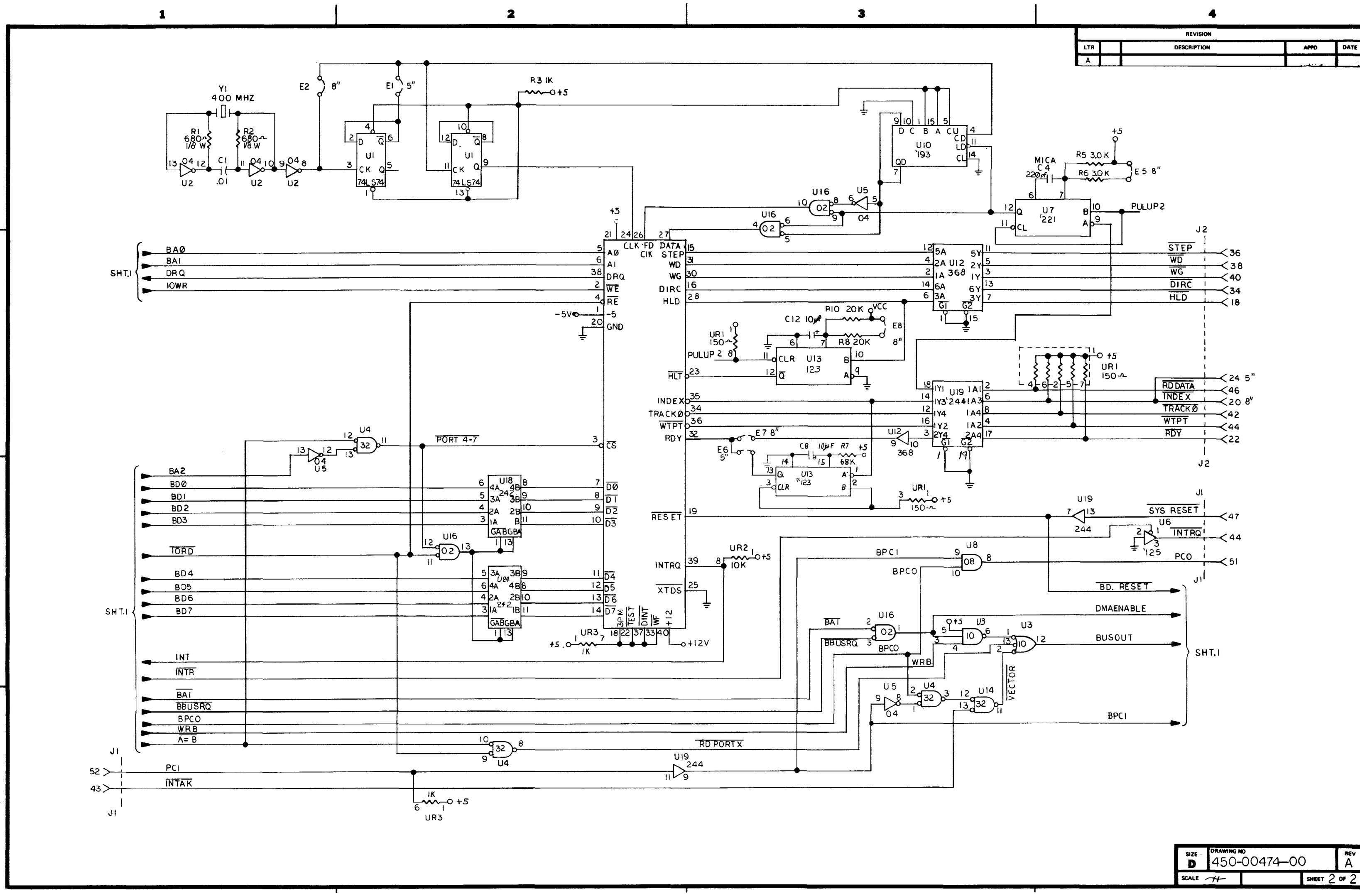
TABLE A-1 P1 CONNECTOR PINOUT (STD Z80 BUS)

Component Side					Circuit Side			
	Pin	Mnemonic	Signal Flow	Description	Pin	Mnemonic	Signal Flow	Description
	43	$\overline{\text{INTAK}}$	In	Interrupt Acknowledge	44	$\overline{\text{INTRQ}}$	Out	Interrupt Request
	45	$\overline{\text{WAITRQ}}$	In	Wait Request	46			
	47	$\overline{\text{SYSRESET}}$	In	System Reset	48			
	49	$\overline{\text{CLOCK}}$	In	Clock from Processor	50			
	51	PCO	OUT	Priority Chain Out	52	PCI	In	Priority Chain In
Power	53				54			
Bus	55	AUX+V	In	+12 Volts DC	56	AUX-V	In	+12 Volts DC

APPENDIX B

SCHEMATIC

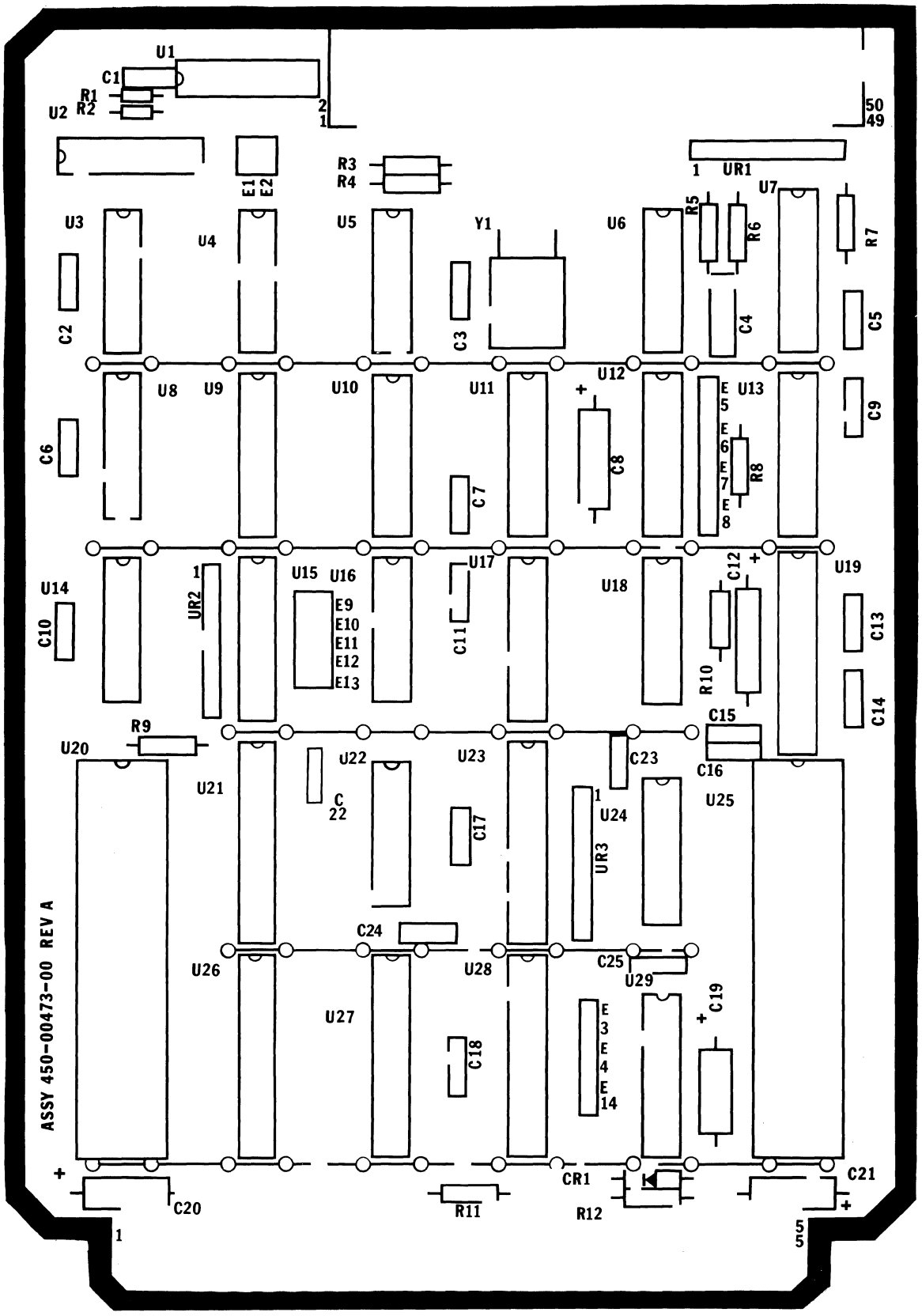

ALL INFORMATION DISCLOSED BY THIS DOCUMENT IS CONSIDERED CONFIDENTIAL AND PROPRIETARY BY MOSTEK CORPORATION. ALL DESIGN, MANUFACTURE, USE, REPRODUCTION, AND SALE RIGHTS ARE RESERVED BY MOSTEK CORPORATION.
NOTES:
ALL IC's UNLESS OTHERWISE NOTED, ARE 74LS PARTS.
REVISIONS
LTR DESCRIPTION APPD DATE
A RELEASED 5/79
PORT 0
PORT 2
PORT 3
WR8
RD8
BUSOUT
STATUS 0
DMAENABLE
RDB
SHT. 2
U20 MK 3883 Z80 DMA
MUXWAIT
BUSRQ
INT
RDPORT3
RDPORT2
SSIDE
BDRESET
MOSTEK
MOSTEK Corporation Carrollton, Texas 75006
MDX-FLP SCHEMATIC - P.C.B.
DRAWING NO 450-00474-00
SIZE D
REV A
SHEET 1 OF 2


REVISION
LTR
DESCRIPTION
APPD
DATE
A
Y1
400 MHZ
R1 680 1/8 W
R2 680 1/8 W
C1 .01
E2 8"
E1 5"
R3 1K
+5
U1
74LS74
U2
U4
U5
U7
'221
U10
'193
U12
368
U13
123
U16
U18
244
U19
244
U3
U6
'125
U8
U14
MICA
C4
220pF
R5 3.0K
R6 3.0K
E5 8"
PULUP2
SHT.1
BA0
BA1
DRQ
IOWR
BA2
BD0
BD1
BD2
BD3
IORD
BD4
BD5
BD6
BD7
INT
INTR
BAI
BBUSRQ
BPCO
WRB
A=B
PORT 4-7
CLK FD CIK
DATA
STEP
WD
WG
DIRC
HLD
HLT
INDEX
TRACK0
WTPT
RDY
RESET
INTRQ
XTDS
CS
GND
-5V
+12V
C12 10µF
R10 20K
R8 20K
VCC
E8 8"
UR1 150Ω
PULUP
E7 8"
E6 5"
C8 10µF
R7 68K
UR2 10K
UR3 1K
J2
STEP
WD
WG
DIRC
HLD
RDDATA
INDEX
TRACK0
WTPT
RDY
24 5"
20 8"
J1
SYS RESET
INTRQ
PCO
BPCI
BPCO
BD. RESET
DMAENABLE
BUSOUT
BAT
BBUSRQ
VECTOR
RD PORTX
PCI
INTAK
52
43
SIZE D
DRAWING NO 450-00474-00
REV A
SCALE
SHEET 2 OF 2

APPENDIX C

ASSEMBLY DRAWING
PARTS LIST

ASSEMBLY DRAWING



PARTS LIST

0000001		ASSY 450-00473-00 REVA1	AZ:MDX-FLP	77652
0000002		SCH 450-00474-00 REV A	AZ:MDX-FLP	77652
4150075	1	CAPACITOR .01UF	C1	77652
4150092	1	CAPACITOR 220PF	C4	77652
4150111	18	CAPACITOR .1UF	C2,3,5-7,9-11,13-18,22-25	77652
4150140	3	CAPACITOR 15UF	C19,20,21	77652
4150166	2	CAPACITOR 10UF	C8,12	77652
4210144	1	HEADER 10 PIN	E9-13	77652
4210229	1	HEADER 50 PIN RIGHT <	J1	77652
4210232	2	BUS BAR 3 SPACE	Z	77652
4210233	3	BUS BAR 5 SPACE	Z	77652
4230018	1	CRYSTAL 4MHZ	Y1	77652
4280007	18	AUGAT STAKE PINS	E1-8,14	77652
4280155	1	EJECTOR CARD EDGE	B	77652
4313288	2	IC 74LS04	U2,5	77652
4313289	1	IC 74LS08	U8	77652
4313296	1	IC 74LS138	U9	77652
4313300	1	IC 74LS02	U16	77652
4313301	1	IC 74LS10	U3	77652
4313305	1	IC 74LS174	U17	77652
4313409	1	IC 74LS241	U28	77652
4313411	3	IC 74LS32	U4,14,22	77652
4313413	1	IC 74LS74	U1	77652
4313420	1	IC FD1771	U25	77652
4313464	1	IC 74LS367	U29	77652
4313507	2	IC 74LS244	U19,23	77652
4313508	3	IC 74LS245	U21,26,27	77652
4313566	2	IC 74LS368	U11,12	77652
4313636	1	IC MK3883	U20	77652
4313638	1	IC 74LS221	U7	77652
4313639	2	IC 74LS242	U18,24	77652
4313640	1	IC 74LS123	U13	77652
4313641	1	IC 74LS125	U6	77652
4313642	1	IC 74LS193	U10	77652
4313749	1	IC DM8131	U15	77652
4313769	1	MK6281 (PGMD 2716)	Z:NOTE SHIPPED NOT ASSEMBLED	77652
4470069	2	RESISTOR 680 OHM 1/4W	R4,12	77652
4470073	1	RESISTOR 1K OHM 1/4W	R3	77652
4470084	3	RESISTOR 3K OHM 1/4W	R5,6,11	77652
4470097	1	RESISTOR 10K OHM 1/4W	R9	77652
4470104	2	RESISTOR 20K OHM 1/4W	R8,10	77652
4470117	1	RESISTOR 68K OHM 1/4W	R7	77652
4470179	1	SIP 8 PIN 1K	UR3	77652
4470275	1	SIP 8 PIN 150 OHM	UR1	77652
4470276	1	SIP 8 PIN 10K	UR2	77652
4470277	2	RESISTOR 680 OHM 1/8W	R1,2	77652
4480047	1	ZENER 1N751	CR1	77652
4610136	1	FAB 450-00472-00 REV A	AZ:PC BOARD MDX-FLP	77652
4620019	2	SOCKET IC 40 PIN	X20,25	77652
4620100	1	SOCKET IC 20 PIN	X26	77652
5013004	2	BAG ANTISTATIC	Z: SHIPPED NOT ASSEMBLED	77652
5013204	1	BOX SHIPPING	Z: SHIPPED NOT ASSEMBLED	77652
5025266	1	TRAVELER WIP	Z: NOTE IN HOUSE USE ONLY	77652
::::::::::::::		SHIPPING LIST MDX-FLP	\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	77652
MK78409	1	FACTORY REPAIR SHEET	\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	77652
MK78410	1	LIMITED WARRANTY SHEET	\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	77652
MK78411	1	FACTORY REPAIR SHEET	\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	77652
MK78425	1	ANTISTATIC NOTICE	\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	77652
MK79639	1	MDX-FLP OPS MANUEL	\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	77652
MK79763	1	MD SERIES BROCHURE	\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	77652
NOTE	**********	NOTE **********	ZA:CABLE USAGE WILL BE	77652
NOTE	**********	NOTE **********	ZB:PLANNED FOR 90% 77963	77652
NOTE	**********	NOTE **********	ZC:AND 10% 77964.	77652

APPENDIX D

MDX - DISK CONTROLLER FIRMWARE (MDX-DCF)

D-1. GENERAL DESCRIPTION

D-2. INTRODUCTION

D-3. SCOPE. This appendix details the user interfaces to the MOSTEK MDX Disk Controller Firmware (MDX-DCF) package and outlines programming guidelines for those users electing to design their own DCF Package.

D-4. MDX - DCF is the MOSTEK Disk Controller Firmware package for the MDX Floppy Disk Controller Card (MDX-FLP). The firmware package is designed to work with the following minimum hardware configuration.

1. MOSTEK MDX-CPU1 Card.
2. MOSTEK MDX-FLP Card.
3. 1 to 4 soft sectored 8 inch flexible disk units.
4. MOSTEK MDX-DRAM8 Card or equivalent Read/Write memory.

D-5. OVERVIEW. The MDX Disk Controller Firmware (DCF) is designed to interface from the FLP-80DOS/MDX Flexible Disk Handler (FDH) to the MOSTEK MDX Floppy Disk Controller Card (MDX-FLP). However, the FDH can be substituted by a user provided equivalent FDH function. Input to the DCF consist of request codes, unit number, track number, and sector number. Control of the hardware is exercised via an MK3883 DMA Controller Chip and a WD1771 Disk Controller Chip, both of which reside on the MDX-FLP Card. Several DCF request codes are available to the user for moving data to and from the flexible disk drive and for inquiring events status. A loader is also provided in MDX-DCF.

D-6. REFERENCE DOCUMENTS

MDX-CPU1 Operations Manual	MK79612
FLP-80DOS/MDX Operations Manual	MK79668

D-7. DEFINITION OF SYMBOLS USED IN THIS APPENDIX

D-8. The following conventions are used throughout this appendix.

1. All hexadecimal numbers are identified by the character "H" following the hexadecimal numbers.
2. aaaa means any hexadecimal number.

D-9. APPENDIX FORMAT

D-10. The following sections detail the user interfaces to the MDX-DCF including the areas of service request input codes, service request responses, data structures, and error handling.

D-11. FUNCTIONAL DESCRIPTION

D-12. This section outlines the functional operations of MDX-DCF.

D-13. SOFTWARE CONFIGURATION

D-14. RESIDENCE. The MDX-DCF is provided in on 2716 PROM and must be located at address EC00H. The PROM can reside on one of the following MDX Cards whose address strapping is configured to the MDX-DCF requirement.

1. MDX - CPU1 Card
2. MDX - CPU2 Card
3. MDX - EPROM/UART Card
4. MDX - UMC Card
5. MDX - SC/D Card

D-15. SIZE. The MDX-DCF is approximately 1K bytes long. The remaining 1K bytes of the PROM are available for user programs. User programs should start at address E800H and can occupy PROM up to address EBFFH. (Lower half of PROM is available to user, upper half is for MDX-DCF).

D-16. VERSION. The version of MDX-DCF provided is for a 10 millisecond drive stepping rate.

D-17. CONTROLLER OVERVIEW

D-18. OPERATION. The calling address for the MDX-DCF is EC00H. All requests are made via the 48 byte Input/Output Control System (IOCS) parameter vector. A brief overview of this vector is provided in the following sections. After each MDX-DCF request is processed, return is made to the caller. This is not an interrupt driven program, rather, the operation is completed before further processing can take place. However, a user designed DCF can take advantage of the interrupt capability of the MDX-FLP Card. All I/O to the disk is done via the DMA and Disk Controller circuitry. All registers except the flags register are preserved by MDX-DCF. After an operation is completed, the zero flag is reset if no error occurred. If any error occured, then bit zero of the vector ERRC parameter is also set.

D-19. SECTOR DEFINITION

The MDX-DCF sector is defined as 128 bytes of data, of which 124 bytes are allocated for user data and 4 bytes are for MDX-DCF sector linkage requirements. The DCF sector linkage is a double-linked list containing the last and next track and sector numbers.

D-20. DATA TRANSFER. The data transfer operation occurs as follows. For Read operations, the first 124 bytes of the user specified unit, track, and sector are read from disk and placed into the user specified buffer area. The remaining 4 bytes are read and placed in the IOCS vector. For Write operations, the first 124

bytes from the user specified buffer area are written to disk at the user specified unit, track and sector number. The remaining 4 bytes are written to disk from the data in the IOCS vector.

D-21. USER PROVISION. Prior to calling MDX-DCF with a read or write service request, the user buffer area (write only) and the IOCS vector fields must be set up by the user. The sector's total 128 bytes are available to the user with the only requirements being that on the read and write operations, the data split of 124 and 4 bytes are adhered to (124 in the buffer area and 4 in the IOCS vector). If the user does not elect to use a doubly linked list concept, then the 4 bytes in the IOCS vector can be used for whatever the user desires. Regardless of the use of the 4 bytes, their contents and those of the 124 bytes in the buffer area are all set up and maintained by the user.

D-22. DATA STRUCTURES

D-23. OVERVIEW

D-24. MDX-DCF works off of user provided information located in the Input/Output Control System (IOCS) vector. The vector is 48 bytes long (30H). Bytes 0-29 are the user interface to IOCS. Bytes 30-39 are reserved for I/O device handlers usage. Bytes 40-47 are reserved for IOCS usage. In FLP-80DOS/MDX, the vector is used by system programs to interface to IOCS; by IOCS to interface to device handlers; and by the Flexible Disk Handler (FDH) to interface to the MDX-DCF.

D-25. IOCS VECTOR STRUCTURE

D-26. The following table specifies the contents of the IOCS vector along with designation of those vector parameters required by MDX-DCF. For a complete definition of the vector, refer to Section 9 of the FLP-80DOS Operations Manual.

D-27. VECTOR FIELD DEFINITIONS

TABLE D-1.

IOCS VECTOR DEFINITION

FIELD#	#BYTES	OFFSET	NAME	DESCRIPTION	DATA TYPE	USED BY MDX-DCF
1	1	(IY+0)	LUNIT	Logical Unit Number	Binary	-
2	2	(IY+1)	DVCE	Device Mnemonic	ASCII	-
3	1	*(IY+3)	UNIT	Unit Number	ASCII	X
4	6	(IY+4)	FNAM	File Name	ASCII	-
5	3	(IY+10)	FEXT	File Name Extension	ASCII	-
6	1	(IY+13)	VERS	File Version	Binary	-
7	1	(IY+14)	USER	User Number	Binary	-
8	1	*(IY+15)	RQST	Request Code	Binary	X
9	1	(IY+16)	FMAT	I/O Format	Binary	-
10	2	(IY+17)	HADDR	Device Handler Address	Binary	-
11	2	(IY+19)	ERRA	User Specified Error Return Address	Binary	-
12	1	(IY+21)	CFLGS	Control Flags	Binary	-
13	1	(IY+22)	SFLGS	Status Flags	Binary	-
14	1	(IY+23)	ERRC	Error Code	Binary	X
15	1	(IY+24)	PBFFR	Physical Buffer Number	Binary	-
16	2	*(IY+25)	UBFFR	User's Buffer Address	Binary	X
17	2	*(IY+27)	USIZE	User's Buffer Size	Binary	-
18	1	(IY+29)	NREC	Number of Records	Binary	-
19	10	*(IY+30)	HSCR	Device Handler Scratch	--	X
20	8	(IY+40)	ISCR	IOCS Scratch	--	-

An * indicates the parameter is to be set up by the user prior to calling MDX-DCF, dependent on MDX-DCF Service Request Code (RQST). IY is the IY Register set up by the user which points to the first field of the vector. X indicates field used by MDX-DCF.

D-28. UNIT. The UNIT field specifies one of the four disk drive devices. This field's valid data range is 00H to 03H (drive unit #0 to drive unit #3).

D-29. RQST. The RQST field is the request code. MDX-DCF supports several service request codes, and are as follows:

RQST CODE (HEX)	NAME	DESCRIPTION
10	STATUS	Read disk drive Status.
11	READ	Read a sector of data to memory.
12	WRITE	Write a sector of data from memory.
13	SEEK	Position disk head to specified track.
14	RESTORE	Initialize disk unit.
15	READ ID	Read next available sector ID and track.
16	WRITE DEL	Write a deleted sector of data.
17	FORMAT	Format specified track.

The above Request Codes are further described in detail in a later section. This field's valid data range is 10H to 17H.

D-30. ERRC. The ERRC field is the error code inserted by MDX-DCF upon detection of an error. Whenever an error occurs, Bit 0 of this field is set. An error code is placed into location FF09H to indicate the type of error as follows:

BIT	ERROR IF SET
7	Invalid drive, track or sector
6	Disk unit not ready
5	Track seek error
4	Sector not found
3	CRC error
2	Data lost
1	Disk is write protected
0	Attempt to read a deleted sector

ERRC should be interrogated after each call to an MDX-DCF service request.

D-31. UBFFR. The UBFFR (user buffer) field is specified by the user to direct MDX-DCF where to locate the I/O data. The buffer address is entered least significant byte first. This field's valid data range is 0000H to FFFFH.

D-32. HSCR. The HSCR field is the MDX-DCF's handler scratch area used for user and DCF specifying of disk parameters. This field is defined as follows, and only six of the ten bytes are used.

FIELD#	#BYTES	OFFSET	NAME	DESCRIPTION	DATA TYPE
19a	1	*(IY+30)	SCTR	Sector Number	Binary
19b	1	*(IY+31)	TRK	Track Number	Binary
19c	1	(IY+32)	LSCTR	Last Sector Pointer	Binary
19d	1	(IY+33)	LTRK	Last Track Pointer	Binary
19e	1	(IY+34)	NSCTR	Next Sector Pointer	Binary
19f	1	(IY+35)	NTRK	Next Track Pointer	Binary

An * indicates the parameter is to be set up by the user prior to calling MDC-DCF.

D-33. SCTR. The SCTR field is the user specified sector number of where the read or write operation is to start. This field's valid data range is 01H to 1AH (1 to 26 decimal).

D-34. TRK. The TRK field is the user specified track number of where the read, write, or seek operation is to start. This field's valid data range is 00H to 4CH (0 to 76 decimal) for single-sided 8" disks, and 00H to 99H (0 to 153 decimal) for double-sided 8" disks.

D-35. LSCTR. The LSCTR field is the DCF provided last sector pointer number. This field's valid data range is the same as the SCTR field.

D-36. LTRK. The LTRK field is the DCF provided last track number. This field's valid data range is the same as the TRK field.

D-37. NSCTR. The NSCTR field is the DCF provided next sector number. This field's valid data range is the same as the SCTR field.

D-38. NTRK. The NTRK field is the DCF provided next track number. This field's valid data range is the same as the TRK field.

D-39. MEMORY REQUIREMENT

Each IOCS vector requires 48 bytes of memory. However, MDX-DCF only requires the first 36 bytes of the vector. If a user application does not require the remaining 12 bytes of the IOCS vector information, then a 36 byte vector can be used. That is, an abbreviated vector can be used to minimize the vector's memory requirement.

D-40. SERVICE REQUEST CODES

The eight MDX-DCF Request Codes that are provided via the RQST field are described in detail in the following sections.

D-41. STATUS (10H). The Status request returns the status of the user specified drive (UNIT): disk not ready and/or disk drive write protected. These status indications are provided in the ERRC field and in location FF09H.

D-42. READ (11H). The Read request transfers a sector of data from the user specified unit, track and sector number (UNIT, TRK, SCTR) to the user specified buffer area (UBFFR).

D-43. WRITE (12H). The Write request transfers a sector of data from the user specified buffer area (UBFFR) to the user specified unit, track and sector number (UNIT TRK, SCTR).

D-44. SEEK (13H). The Seek request positions the user specified disk unit (UNIT) head to the user specified track number (TRK).

D-45. RESTORE (14H). The Restore request initializes the user specified disk unit (UNIT) and positions the head to track 0 (outermost track).

D-46. READ ID (15H). The Read ID request reads the next available sector and track number and places the sector number in location FF08H and track number in FF0AH.

D-47. WRITE DEL (16H). The Write Deleted request is identical to the WRITE REQUEST (12H) except that a deleted address mark replaces a regular data address mark.

D-48. FORMAT (17H). The Format request formats the user specified unit and track number (UNIT, TRK) to IBM 3740 specification.

D-49. REQUEST CODE VECTOR REQUIREMENTS. The following Table lists the vector fields required for each of the MDX-DCF request codes.

Service Request	Vector Field: UNIT	RQST	ERRC	UBFR	SCTR	TRK	LSCTR	LTRK	NSCTR	NTRK
Status (10H)	X	X	0	-	X	X	-	-	-	-
Read (11H)	X	X	0	0	X	X	0	0	0	0
Write (12H)	X	X	0	X	X	X	X	X	X	X
Seek (13H)	X	X	0	-	X	X	-	-	-	-
Restore (14H)	X	X	0	-	X	X	-	-	-	-
Read ID (15H)	X	X	0	-	X	X	-	-	-	-
Write Del (16H)	X	X	0	-	X	X	-	-	-	-
Format (17H)	X	X	0	-	X	X	-	-	-	-

Where: X = User Input
0 = DCF Output
- = Not Used

D-50. LOADER

D-51. OVERVIEW

D-52. A Loader is provided with MDX-DCF. The Loader accesses the disk at a given track and sector and loads data from the disk until the last sector is found. The Loader requires that the file to be loaded is in a linked file structure, that is, the sector's first 124 bytes are user data and the remaining 4 bytes are the doubly linkage information.

D-53. USEAGE REQUIREMENTS

D-54. The following sections outline the user set-up requirements and resultant responses of the Loader.

D-55. INPUT. Prior to calling the Loader, set up an IOCS vector with the specified fields of:

1. Unit number (UNIT)
2. Starting track number (TRK)
3. Starting sector number (SCTR)
4. Starting buffer area (UBFFR)

D-56. PROCESS. To start the Loader perform:

1. Set up IOCS vector address in register IY.
2. Call Loader at entry address EC03H.

D-57. OUTPUT. The Loader will respond with:

1. Z Flag set if load process successful (the data from the file loaded will be in the user buffer area) or
2. Z Flag reset if load process unsuccessful after 10 retries.

D-58. SET-UP REQUIREMENTS

D-59. OVERVIEW

D-60. In order for MDX-DCF to operate properly, the following hardware and software configurations must be set up prior to use.

D-61. HARDWARE CONFIGURATION

A. MDX-FLP Card's port addresses must start at E0H.

B. The MDX-DCF program must be located at address EC00H, lower half of PROM starts at E800H.

D-62. SOFTWARE CONFIGURATION

A. All devices having interrupt capability must be disabled, reset, or otherwise rendered incapable of interrupting prior to calling the DCF. DCF does an Enable Interrupt (EI) instruction.

B. DCF outputs an 01 to port 7DH to stop CTC Timer #1 on MDX-CPU1 and PU2.

C. The IOCS vector structure must be adhered to for all MDX-DCF service requests.

D. The system clock rate must be loaded into location FFE0H.

   1. Load 00h for 2.5MHz system.

E. The following locations must be available for MDX-DCF RAM usage; all locations are inclusive:

   1. FF24H, must be initialized to zero.
   2. FFE2H - FFE3H
   3. FEFDH - FEFFH
   4. FF07H - FF0BH
   5. FF00H - FF01H must be initialized to an <u>odd</u> RAM address at which address minus 2 and 3 a 2-byte field is available for the DCF's interrupt vector. One possibility for the contents of FF00H - FF01H is the address of the last byte of RAM.

D-63. PROGRAMMING GUIDELINE

D-64. OVERVIEW

D-65. The following sections provide a functional overview of the sequence of events required to be performed for the DCF request codes. Users who elect to design their own DCF can use this section as a guideline. The sequence of events provided are for each of the MDX-DCF request codes. The user should be aware that each of the events equate to several detailed functional events; consult the earlier MDX-FLP Card Operations Manual sections for complete definition of the DMA and WD1771 controller commands. The MDX-FLP port involved in each of the events is provided in parenthesis.

D-66. SERVICES SEQUENCE OF EVENTS

D-67. STATUS (10H).

1. Select the unit. (Port E2H)
2. Issue a read status command (Port E4H)
3. Wait for completion (Port E4H)

D-68. READ (11H).

1. Select the unit. (Port E2H)
2. Select the sector. (Port E6H)
3. Select the track. (Port E7H)
4. Select side of disk if required. (Port E3H)
5. Seek, if required, and verify (optional). (Port E4H)
6. Set up the DMA. (Port E0H)
7. Load head if required. (Port E4H)
8. Issue read data transfer command. (Port E4H)
9. Wait for completion, and then check for errors and status (Port E4H)

D-69. WRITE (12H).

1. Select the unit. (Port E2H)
2. Select the sector. (Port E6H)
3. Select the track. (Port E7H)
4. Select side of disk if required. (Port E3H)
5. Seek if required, and verify (optional). (Port E4H)
6. Set up the DMA. (Port EOH)
7. Load head if required. (Port E4HO
8. Issue write data transfer command. (Port E4H)
9. Wait for completion, and then check for errors and status (Port E4H)

D-70. SEEK (13H)

1. Select the unit. (Port E2H)
2. Select the track. (Port E7H)
3. Issue seek command. (Port E4H)
4. Wait for completion, and then check for errors and status (Port E4H)

D-71. RESTORE (14H).

1. Select the unit. (Port E2H)
2. Issue restore command. (Port E4H)
3. Wait for completion, and then check for errors and status (Port E4H)

D-72. READ ID (15H).

1. Select the unit. (Port E2H)
2. Load head if required. (Port E4H)
3. Issue read ID command. (Port E4H)
4. Wait for completion, and then check for errors and status (Port E4H)

D-73. WRITE DEL (16H).

1. Select the unit. (Port E2H)
2. Select the sector. (Port E6H)
3. Select the track. (Port E7H)
4. Select the side of disk if required. (Port E3H)
5. Seek if required, and verify (optional). (Port E4H)
6. Set up the DMA. (Port EOH)

7. Load head if required. (Port E4H)
8. Issue write delete command. (Port E4H)
9. Wait for completion, and then check for errors and status (Port E4H)

D-74. FORMAT (17H).

1. Select the unit. (Port E2H)
2. Select the track. (Port E7H)
3. Select the other side of disk if required. (Port E3H)
4. Seek if required. (Port E4H)
5. Set up the DMA. (Port EOH)
6. Load head if required. (Port E4H)
7. Issue format command. (Port E4H)
8. Wait for completion, and then check for errors and status (Port E4H)

D-75. SUMMARY

D-76. IOCS VECTOR

FIELD#	#BYTES	OFFSET	NAME	DESCRIPTION	DATA RANGE
1	1	(IY+0)	LUNIT	Logical Unit Number	-
2	2	(IY+1)	DVCE	Device Mnemonic	-
3*	1	(IY+3)	UNIT	Unit Number	00H - 3H
4	6	(IY+4)	FNAM	File Name	-
5	3	(IY+10)	FEXT	File Name Extension	-
6	1	(IY+13)	VERS	File Version	-
7	1	(IY+14)	USER	User Number	-
8*	1	(IY+15)	RQST	Request Code	10H - 17H
9	1	(IY+16)	FMAT	I/O Format	-
10	2	(IY+17)	HADDR	Device Handler Address	-
11	2	(IY+19)	ERRA	User Specified Error Return Address	-
12	1	(IY+21)	CFLGS	Control Flags	-
13	1	(IY+22)	SFLGS	Status Flags	-
14*	1	(IY+23)	ERRC	Error Code	00H - 01H
15	1	(IY+24)	PBFFR	Physical Buffer Number	-
16*	2	(IY+25)	UBFFR	User's Buffer Address	aaaa
17	2	(IY+27)	USIZE	User's Buffer Size	-
18	1	(IY+29)	NREC	Number of Records	-
19a*	1	(IY+30)	STRK	Sector Number	01H - 1AH
19b*	1	(IY+31)	TRK	Track Number	00H - 4CH
19c*	1	(IY+32)	LSCTR	Last Sector Number	01H - 1AH
19d*	1	(IY+33)	LTRK	Last Track Number	00H - 4CH

FIELD#	#BYTES	OFFSET	NAME	DESCRIPTION	DATA RANGE
19e*	1	(IY+34)	NSCTR	Next Sector Number	01H - 1AH
19f*	1	(IY+35)	NTRK	Next Track Number	00H - 4CH
19g*	4	(IY+36)	HSCR	Reminder of Handler Scratch	-
20	8	(IY+40)	ISCR	IOCS Scratch	-

NOTE: * indicates field required by MDX-DCF. Fields 19a - g represent the detailed HSCR Field for MDX-DCF.

D-77. REQUEST CODES

CODE (HEX)	REQUEST
10	Status
11	Read
12	Write
13	Seek
14	Restore
15	Read ID
16	Write Delete
17	Format

MOSTEK®
Z80·F8 Covering the full spectrum of
3870 microcomputer applications.

1215 W. Crosby Rd. • Carrollton, Texas 75006 • 214/323-6000
In Europe, Contact: MOSTEK Brussels
150 Chaussee de la Hulpe, B1170, Belgium;
Telephone: 660.69.24

PRINTED IN USA December 1979
Publication No. MK79639
STD No. 8023-79639-0505