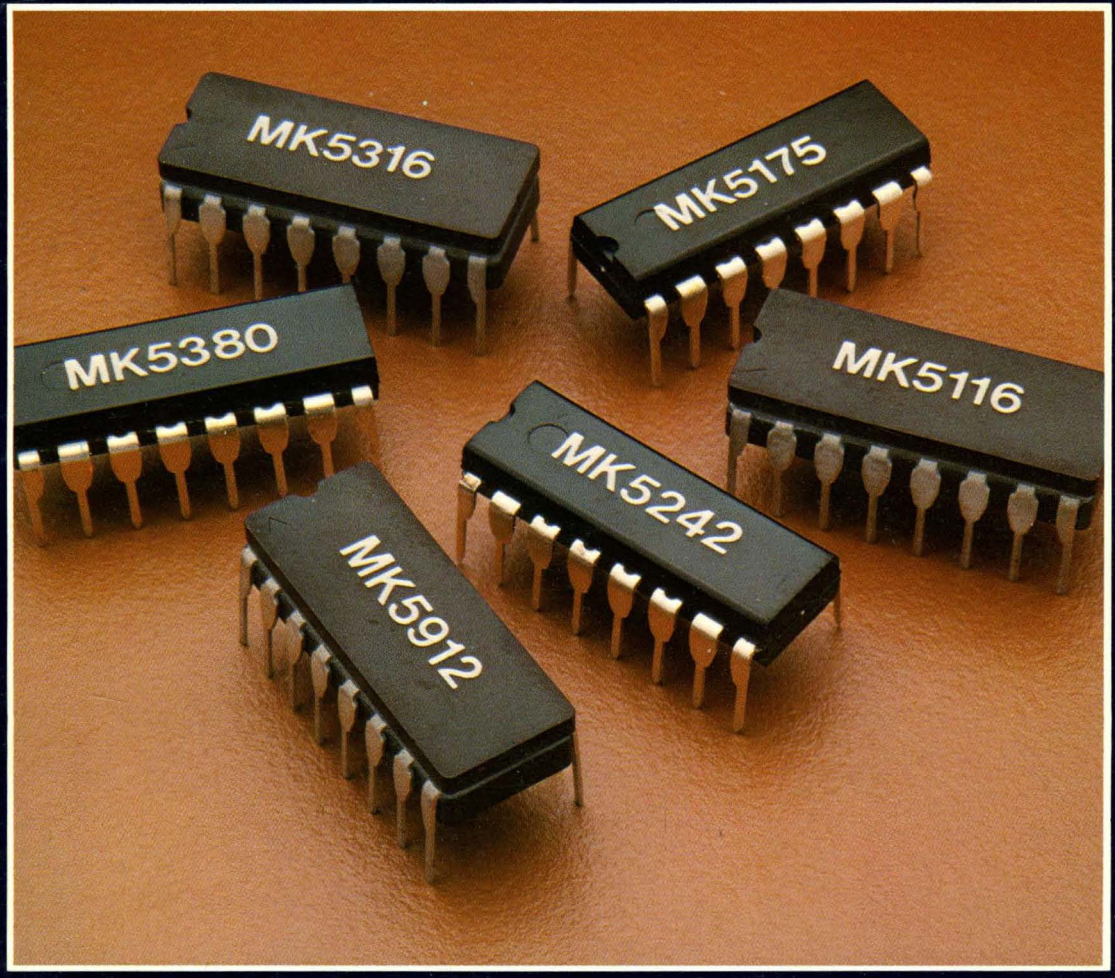
MOSTEK 1982

TELECOMMUNICATIONS DATA BOOK



1982
TELECOMMUNICATION
PRODUCTS DATA BOOK

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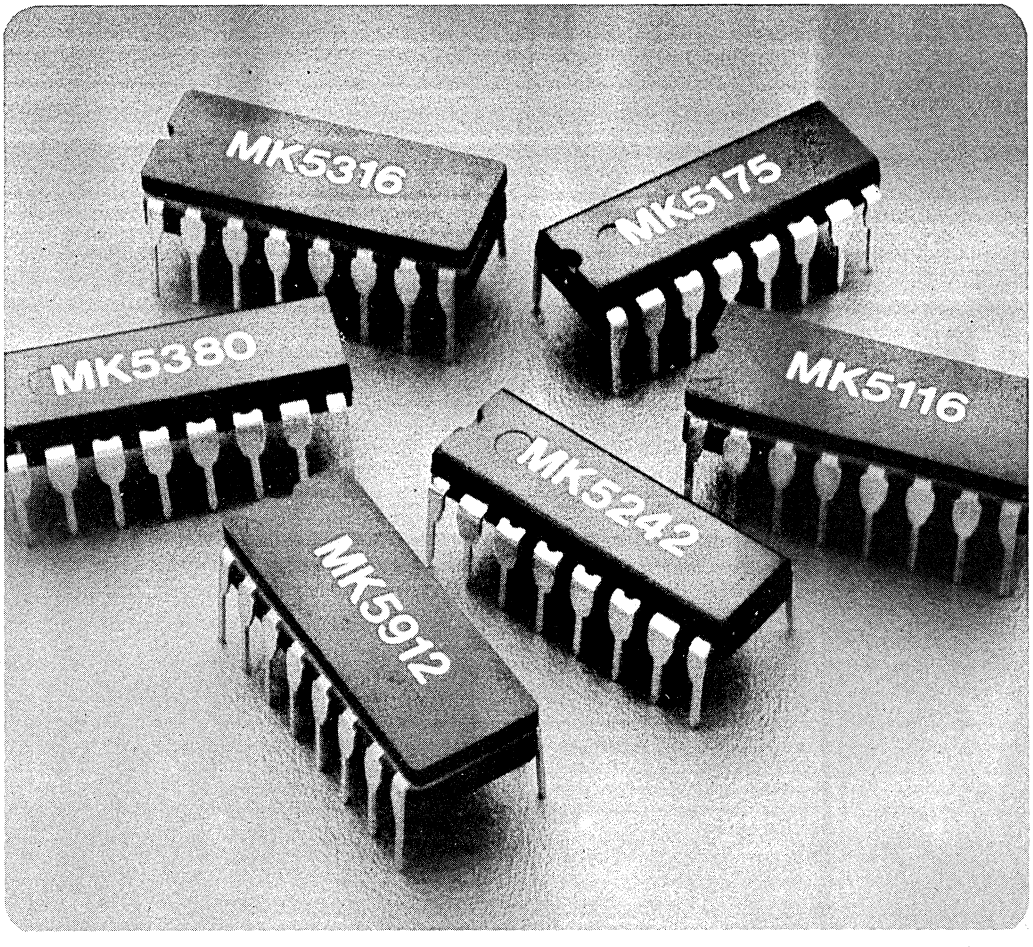

Telecommunications

Mostek offers a broad line of telecommunications circuits aimed at cost-effective solutions for large or small systems. At Mostek, you have a choice. Tone dialers, pulse dialers, repertory dialers, tone decoders, CODECs, and PCM filters are available in volume now.

Mostek made its commitment to telecommunications products in 1974, the year we produced our first tone dialer. Since 1974, we have shipped over nine million tone dialers and we have earned our reputation as a dependable source for reliable products. Our extensive testing and quality control procedures all assure reliable systems in the field.

Some excellent examples of Mostek's technological leadership are the recently introduced ten-number repertory dialer and the switched-capacitor PCM filter. In an application where space and power are the most critical parameters, Mostek's CODEC and PCM filter offer industry's lowest power.

MOSTEK®

TELECOMMUNICATION PRODUCTS

Telecommunications Terms

BALANCED LINE: A line or circuit utilizing two identical conductors, each having the same electro-magnetic characteristics with respect to other conductors and ground. A balanced line is preferred in circumstances where minimum noise and crosstalk are desired.

BALANCING NETWORK: An arrangement of impedances connected to one branch of hybrid to match the impedance of a line connected to the opposite branch.

BASEBAND: The total frequency band occupied by the aggregate of all the information signals used to modulate a carrier (multiplex or radio).

CARRIER: A form of communication using waves that can be modulated by changing their amplitude, frequency, or phase so that they can "carry" intelligence. Carrier communication is used as a means of transmitting one or more messages over a single open-wire pair, cable pair, or radio circuit.

CENTRAL OFFICE (CO): A place or building where telephone calls are switched or connected, either automatically or manually.

C-MESSAGE: A frequency weighting which evaluates the effects of noise corresponding to its annoyance to the "typical" subscriber of standard telephone service. This weighting is also used to evaluate the effects of noise (background and impulse) on voice-grade data services.

C-NOTCHED: A frequency weighting similar to C-Message weighting except for the addition of a narrow stopband or notch at 1010 Hz. Used in making noise-with-tone measurements.

CODEC: A circuit comprised of an encoder and decoder in the same device.

COMPANDOR: A compandor is an electronic circuit used in carrier systems to provide better signal-to-noise ratios. The name is a contraction of two—compressor and expandor, which describe the actions of the two types of circuits in the equipment—a speech compressor at the transmitting end and a speech expandor at the receiving end.

COMPRESSOR: The part of a compandor that is used to compress the intensity range of signals at the transmitting end of a circuit. It amplifies weak signals and attenuates strong signals.

CONTROL OFFICE: The control office is the location designated on the circuit order card as having the responsibility for maintaining the overall circuit. This office is sometimes referred to as the control point. In most cases, this is the office which coordinates all activities on a circuit with the customer.

CORNER EFFECT: The rounding off of the attenuation vs. frequency characteristic of a filter at the extremes (or corners) of the passband.

CROSS MODULATION: A type of intermodulation due to the modulation of the carrier of the desired signal by an undesired signal wave.

CROSSTALK: Crosstalk is the presence of unwanted voice currents. It may or may not be intelligible, but it can be heard. There are two general forms of crosstalk, near-end and far-end.

CVSD: Continuously Variable Slope Delta Modulation.

dBm: dBm is a transmission level referenced to a specified impedance. For instance, 0 dBm/600 Ω is a power of 1 milliwatt across a 600 Ω impedance. (0 dBm = 1 mW)

dBm0: The power expressed in dBm measured at, or referenced to, a point of zero transmission level.

dBm0p: Based upon 1.0 milliwatt at the 0.0 dBm TLP, psophometrically weighted.

dBrn: dBrn is used for noise measurement on telephone lines. Reference noise is -90 dBm (0 dBrn).

dBrnc0: A C-Message weighted value based upon -90.0 dBmC referenced to a point of zero transmission level ie., 0.0 dBrnc0 = -90.0 dBmC0.

DELTA MODULATION: A means of encoding analog signals in control and communication systems. The output of the delta encoder is a single-weighted digital pulse train which may be decoded at the receiving end to reconstruct the original analog signal.

DESENSITIZATION: The tendency of a receiver to fail to recognize valid DTMF signals in the presence of such factors as dial tone, pilot signals, or data signals.

DROP CHANNEL: This refers to a type of operation where one or more channels of a multichannel system are terminated (dropped) at some point intermediate between the end terminals of the system.

DROPOUT: Short interruptions of service where the transmitted signal experiences a sudden large drop in power; often, the signal becomes undetectable. Present standards define a dropout as a decrease in signal level of 12 dB with a duration greater than 10 ms.

DRY LINE: A telephone line without battery voltage present.

ECHO: The result of impedance mismatches, hybrid unbalance, and time delay. Depending upon the location of impedance irregularities and the propagation characteristics of a facility, echo may interfere with the

talker or listener, or both. The greater out-of-phase the currents are, the greater the interfering effect.

ECHO RETURN LOSS(ERL): Is a weighted average of the return losses at all frequencies between 500 and 2500 Hz.

ECHO SUPPRESSOR: Echo Suppressors are used to minimize the effect of echo. They work in such a way as to block the echo return currents. They are voice-operated gates which allow communication one way at a time.

ENVELOPE DELAY DISTORTION: Envelope delay is the derivative of the circuit phase shift (in radians) with respect to frequency (radians p .r second). The deviation of this derivative at any frequency from the derivative's value at a prescribed frequency (usually 1800 Hz) is called envelope delay distortion (EDD).

EQUALIZER: An electrical network in which attenuation (or gain) varies with frequency and is used to provide equalization of a frequency-dependent transmission line.

EXPANDOR: A part of a compandor. It is used at the receiving end of a circuit to return the compressed signal to its original form. It amplifies strong signals.

FOUR-WIRE CIRCUIT: A four-wire circuit is considered to be one which terminates at the customer's premises in four wires. Transmission is done over one pair and reception is done over the other pair. The circuit is four-wire throughout and may include repeaters, carrier, or both. When carrier is used, the circuit is sometimes referred to as "equivalent four-wire" since different transmitting frequencies may be superimposed in the same cable pair or open-wire.

FREQUENCY RESPONSE: The frequency response of a circuit refers to its overall transmission characteristics. The frequencies to be measured and their limits are shown on the circuit order card.

FREQUENCY SHIFT: A fixed offset in each received frequency of a signal relative to the transmitted signal, due to differences in the inserted carrier frequencies in the receivers and transmitters of transmission systems.

FULL DUPLEX: Telegraph or signaling circuits arranged for transmission in both directions at the same time.

GAIN TRACKING: Loss deviation (1000 Hz reference) over the range of levels of interest.

HALF DUPLEX: Transmission in one direction at a time over a single channel. Thus, in a half-duplex telegraph system, information can be transmitted in only one direction at a time.

HOOKSWITCH: The switch on the telephone set which is activated by placing the receiver on the hook. The two conditions are defined as off-hook and on-hook conditions, corresponding to busy and idle circuits respectively.

HYBRID: A bridge-type circuit or connecting device that combines the function of providing impedance matching between certain circuits and isolation between other circuits. A hybrid is often used to connect four-wire lines to a two-wire line so that in both directions of transmission the four-wire lines are isolated from each other, but are connected to the two-wire line.

HYBRID COIL: A hybrid coil is a transformer arrangement used to convert a two-way, two-wire circuit into two separate two-wire circuits (four-wire operation).

IMPULSE NOISE: Characterized by large excursions of the total noise waveform which are much higher than the normal peaks of the message circuit noise.

LOOP RESISTANCE: The loop resistance of a cable pair is the dc resistance from the telephone office to a distant point. It may include a coil at the far end. If no coil is present, a short must be placed across the tip and ring. Corrections for temperature variations from 68°F must be made to the measured dc resistance in order to determine if the loop resistance is correct.

LOSS: End-to-end circuit attenuation usually measured at 1000 Hz.

MESSAGE CIRCUIT NOISE: Background noise measured between two balanced lines. Also called "Metallic Noise".

MODEM: A single unit of equipment which combines the functions of modulator and demodulator. Connects end-user's equipment with telephone system.

MULTIPLEX: A means of transmitting two or more signals over the same medium.

NET LOSS: The net loss of a circuit is the transmission loss at 1000 cycles in dB between two locations. The greater the number, the poorer the circuit. It is sometimes referred to as the specified equivalent or the card loss.

NETWORK: Network, as generally used, refers to an impedance matching device associated with a hybrid coil or terminating set. It is used to balance the derived two-wire circuit (line) for maximum return loss. Networks are of two broad types—precision and compromise. Networks of this type may be referred to as a balancing net, precision net, comp. net, or net.

NOISE FIGURE: The noise figure expresses the amount of noise introduced by a piece of equipment over the basic thermal noise that is present. It represents the relationship of the signal-to-noise ratio at the input of the device to the signal-to-noise ratio at its output.

NOISE IMMUNITY: A measure of a DTMF receiver's ability to prevent valid signals from being rejected as noise. It is sometimes specified as the ability of the receiver to operate under conditions of gaussian noise in dBrnC.

NOISE-TO-GROUND: A noise measurement where the noise is measured from a balanced line to ground.

NOISE WEIGHTING: Noise weighting is used to give the proper interfering effect when noise currents are converted to sound. The weighting networks integrate the noise power over the frequency range by giving each small band of frequencies a weighting proportional to its contribution to the total interfering effect.

NONLINEAR DISTORTION: The generation of new signal components not present in the original transmitted signal. This usually happens when the loss on a channel is nonlinear with respect to input level.

PABX: Private Automatic Branch Exchange. Has the same usage as a PBX except that calls within the system are completed automatically by dialing. An attendant at an attendant's board may be required to route and complete incoming calls from the central office. Stations within the system are connected to the central office by dialing directly, or they are made to go through the attendant as company policy dictates.

PBX: Private Branch Exchange. A telephone system located on the premises of a business and requiring an attendant to complete all calls. It is usually owned by the telephone company and is equipped with trunks to a telephone company central office.

PCM: Pulse-Code Modulation - pulse modulation in which the signal is sampled periodically and each sample is quantized and transmitted as a digital binary code.

PHASE JITTER: The undesired component of a received signal which appears as phase (or frequency) modulation.

PHASE HIT: A sudden change (+ or –) in the received signal phase (or frequency).

PRIVATE LINE CIRCUIT: A private line circuit is a connection between two or more stations for the exclusive use of a customer. It may or may not have access to the nationwide telephone network.

PSOPHOMETRIC-WEIGHTED: A frequency weighting similar to C-Message weighting, which is used as the standard for European telephone system testing.

QUANTIZING NOISE: Signal-correlated noise generally associated with the quantizing error introduced by analog-digital and digital-analog conversions in digital transmission systems.

REPEATER: A repeater is an amplifier. Some repeaters use separate amplifiers for each direction of transmission while others use one amplifier for both directions.

REPEATING COIL: A repeating coil is a transformer. There are numerous impedance ratios available to match a variety of telephone cable and equipment impedances. A repeating coil is sometimes called a repeat coil or coil.

RETURN LOSS (R.L.): The return loss of a circuit is a measure of the amount of transmitting current which is transferred to the receiver at the same location due to impedance mismatches. The higher the ratio in dB, the better the return loss. See ERL and SRL.

RINGDOWN SIGNALING: The 90 V at 20 Hz signal used to operate the ringer in a subscriber's telephone set.

RINGER: The signaling bell in a telephone set.

SENSITIVITY: Generally expressed in dBm at a specified impedance (usually 600 Ω), sensitivity is a measure of the lowest DTMF signal level that a receiver can detect. It represents an absolute threshold below which detection of a single frequency is not generated.

SHORT: A circuit is said to be "short" when the net loss is less than the limits allow. This may create "singing" (oscillation).

SINGING: Singing means a circuit is oscillating because it has too much gain. It can sing at any frequency, but the effect is worse at those frequencies within the usable band.

SINGING POINT (S.P.): The singing point of a circuit is the threshold at which it goes into oscillation. It is a measure of stability and is a function of return loss. It is measured in dB and the larger the number, the greater the stability.

SINGING RETURN LOSS (SRL): Weighted average of the return losses at all frequencies in a frequency band. There is a low frequency test covering the 200 to 500 Hz band (SRL-LO) and a high frequency test covering the 2500 to 3000 Hz band (SRL-HI).

SKEW: A measure (expressed in percent) of the departure of each individually received signal frequency from its nominal value. A function of component tolerances, aging, environmental conditions, and certain types of transmission-multiplexing equipment, skew is measured at the DTMF receiver.

SLEEVE (S): Sleeve is a term to describe the frame or body portion of a telephone plug or jack. See tip and ring.

SUBSCRIBER'S SUBSET: The telephone instrument on the subscriber's premises.

TALK-OFF: The tendency of a DTMF system to respond falsely to other-than-valid DTMF signals. Talk-off criteria are generally specified very subjectively — sometimes in such broad terms as "good" or "poor".

TERMINATING CONNECTION: A measurement that substitutes the internal resistance of the measuring instrument for the subscriber's subset or other equipment. If the measuring instrument does not have the desired impedance, an external resistor must be placed across the input terminals.

TERMINATING SET: A terminating set is used at the terminals of an equivalent four-wire circuit for converting to two-wire operation. The transformer arrangement is similar to a hybrid coil. The set is sometimes referred to as a four-wire term set or term set.

TIP AND RING: Tip (T) and ring (R) are terms used to identify the two conductors of a circuit. They originate from switchboard terminology pertaining to cord circuits. A four-wire circuit is designated T_1, T_2 and R_1 and R_2.

TWIST: The difference (in decibels) between the DTMF high-group and low-group signal levels, mathematically defined as 10 log [(high-group power)/(low-group power)]. Measured at the DTMF receiver, it's a function of both the level difference generated by the signal source and the gain-frequency characteristic of the transmission facility.

TWO-WIRE CIRCUIT: A two-wire circuit is one which terminates at the customer's premises in two wires. It may, however, contain some facilities which are four-wire, such as a repeater or carrier.

VARLEY: A varley (varley loop test) is made with a Wheatstone bridge and is used to detect a difference (unbalance) in the dc resistance of the tip and ring conductors.

WET LINE: A telephone line with battery voltage present.

WHITE NOISE: Random noise whose constant energy per unit bandwidth is independent of the central frequency at the band. The name is taken from the analogous definition of white light.

ZERO TRANSMISSION LEVEL POINT (OTLP): An arbitrary point in a transmission system to which all relative levels at other points in the system are referred. The OTLP is usually the transmitting toll switchboard or testboard.

Definitions of Data Sheet Designations

PRODUCT PROFILE

A Product Profile is an initial disclosure of a new product's features and general information. A "PRODUCT PROFILE" designation on a Mostek literature item indicates that the product is not yet available and that the specification goals have not yet been fully established. The information given in the Product Profile is subject to change and is not guaranteed. Mostek reserves the right to make changes in the Product Profile at any time and without notice.

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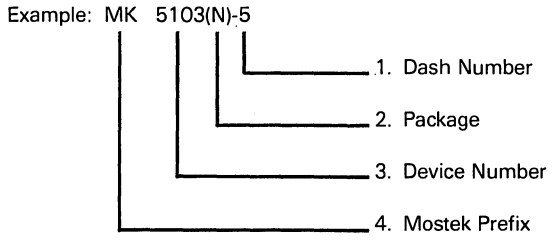
ORDER INFORMATION
TELECOMMUNICATION PRODUCTS

Factory orders for parts described in this book should include a four-part number as explained below:



1. Dash Number

   One or two numerical characters defining specific device performance characteristic.

2. Package

   P - Gold side-brazed ceramic DIP
   J - CER-DIP
   N - Epoxy DIP (Plastic)
   K - tin side-brazed ceramic DIP
   T - Ceramic DIP with transparent lid
   E - Ceramic leadless chip carrier

3. Device number

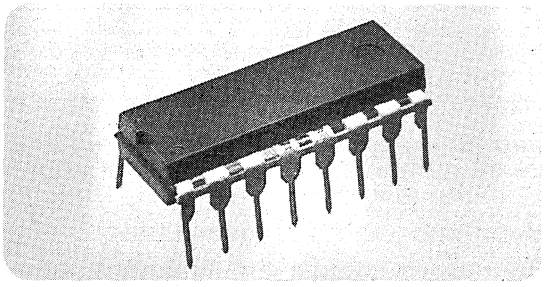
   1XXX or 1XXXX - Shift Register, ROM
   2XXX or 2XXXX - ROM, EPROM
   3XXX or 3XXXX - ROM, EPROM
   38XX - Microcomputer Components
   4XXX or 4XXXX - RAM
   5XXX or 5XXXX - Telecommunications and Industrial
   7XXX or 7XXXX - Microcomputer Systems

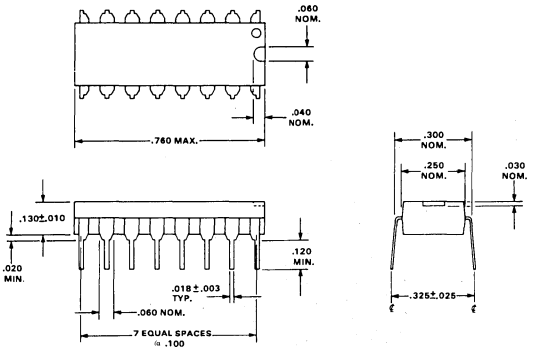
4. Mostek Prefix

   MK-Standard Prefix

   MKB-100% 883B screening, with final electrical test at low, room and high-rated temperatures.

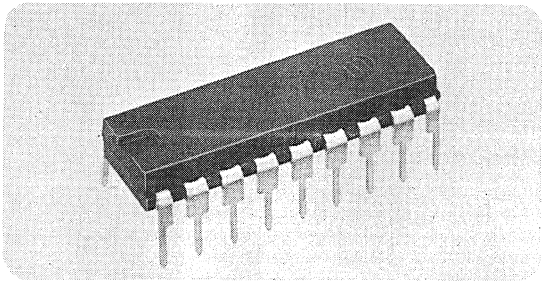
Plastic Dual-In-Line Package (N)
16-Pin

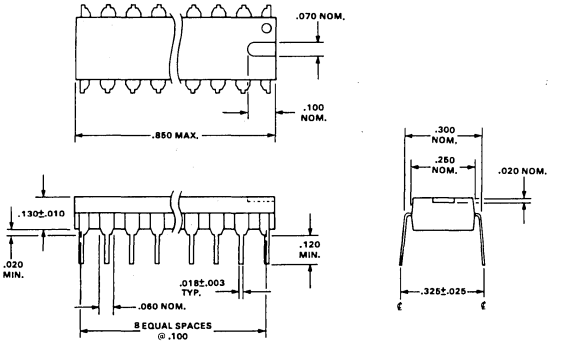




NOTE: Overall length includes .005 flash on either end of package

Plastic Dual-In-Line Package (N)
18-Pin





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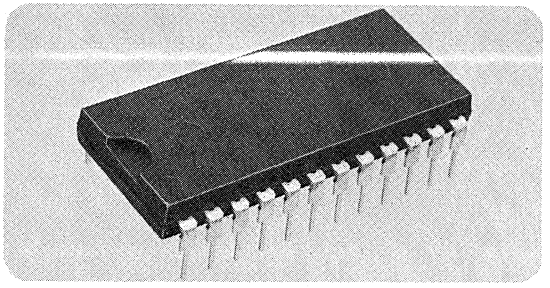

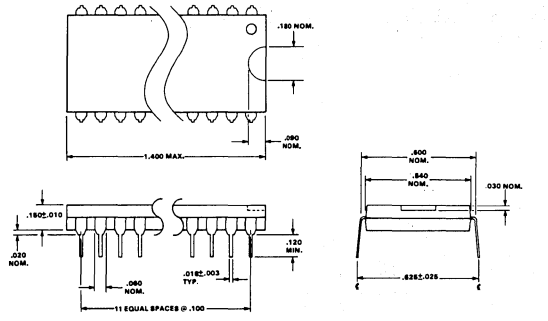

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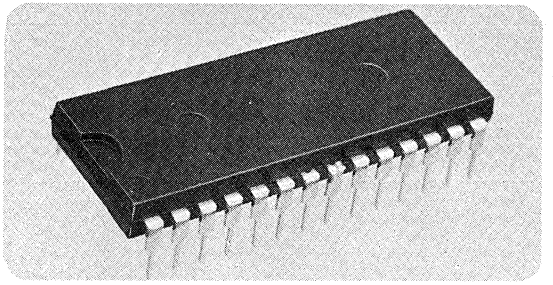
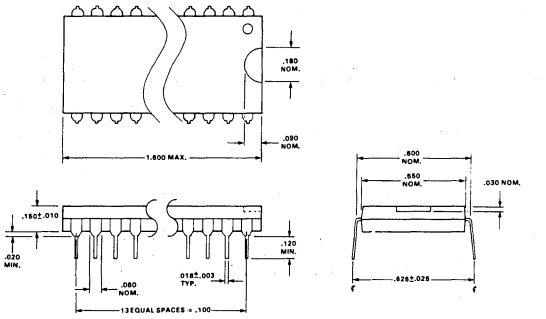
Plastic Dual-In-Line Package (N)
28-Pin





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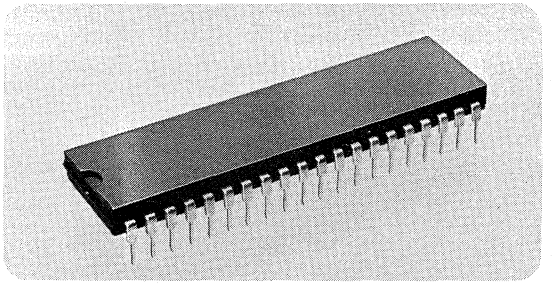

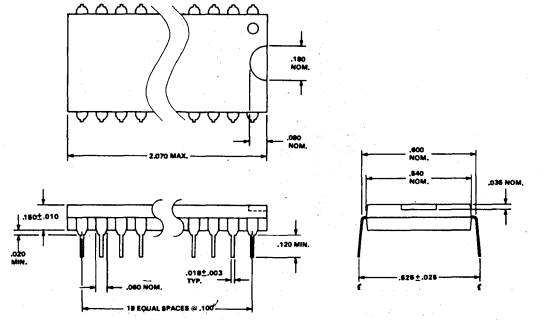

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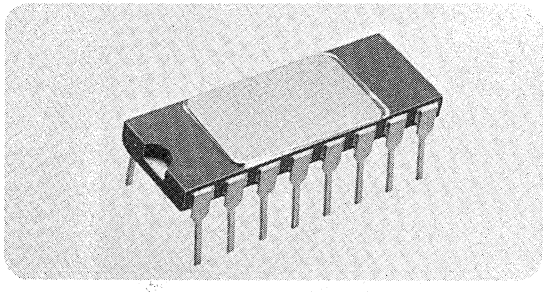

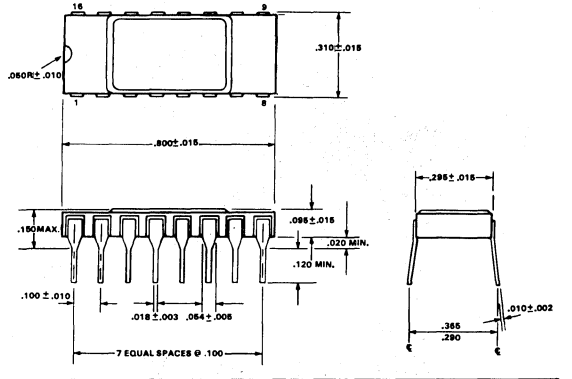

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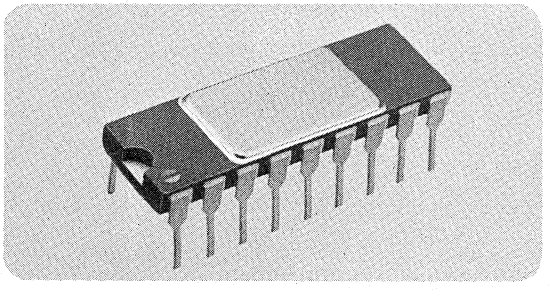

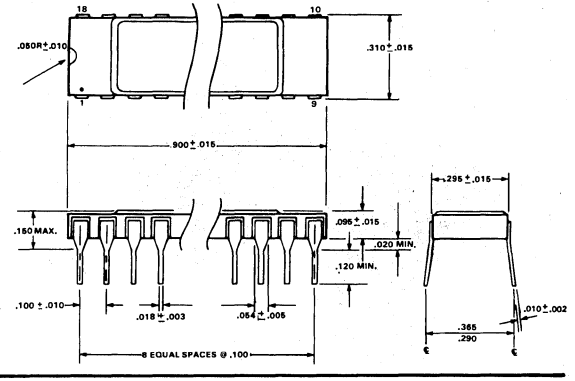

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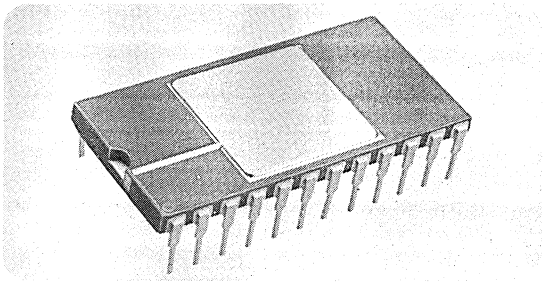

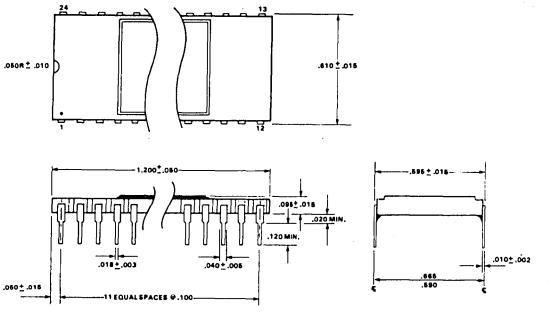

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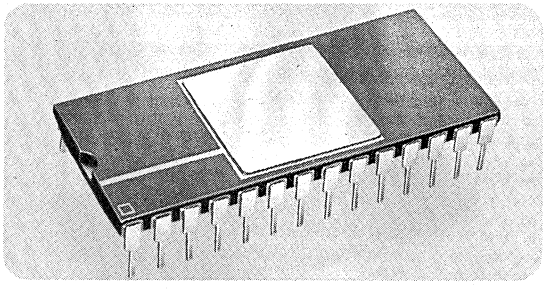

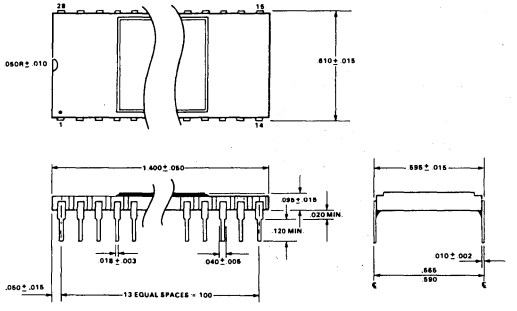

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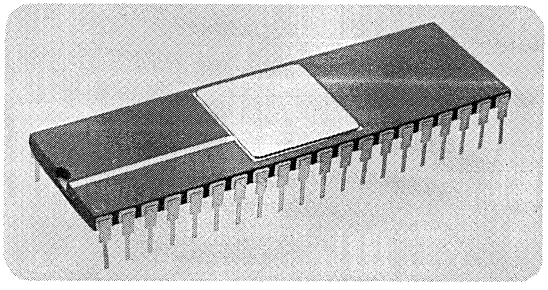

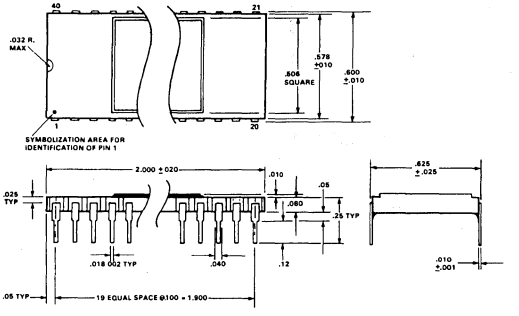

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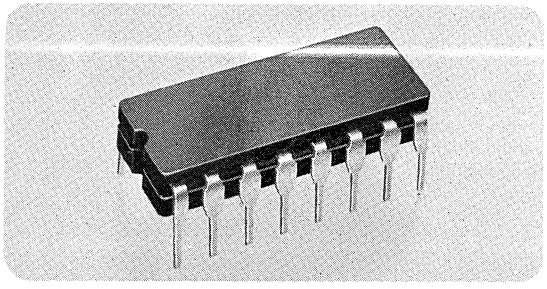

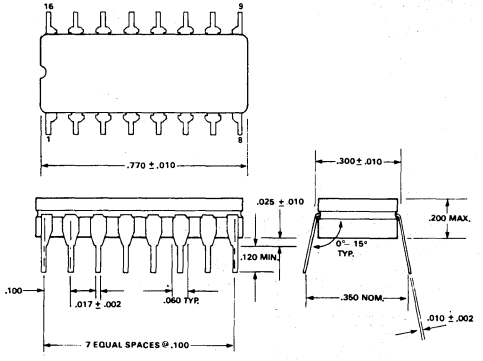

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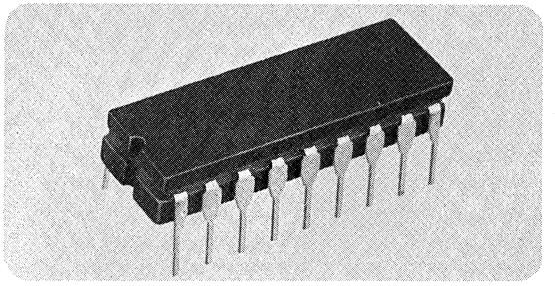

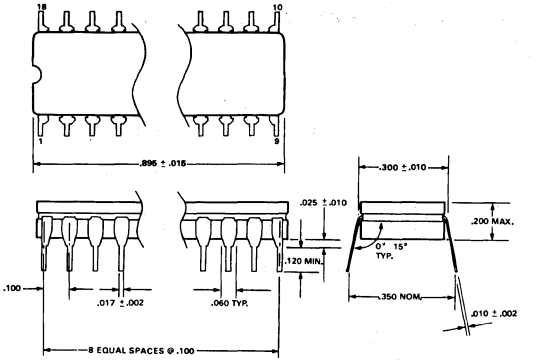

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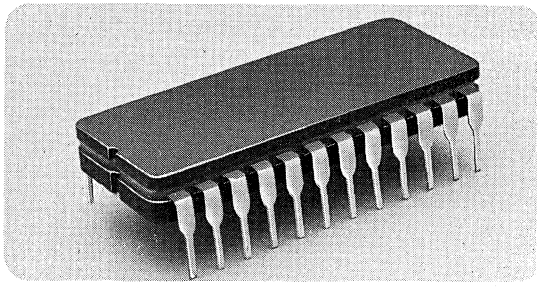

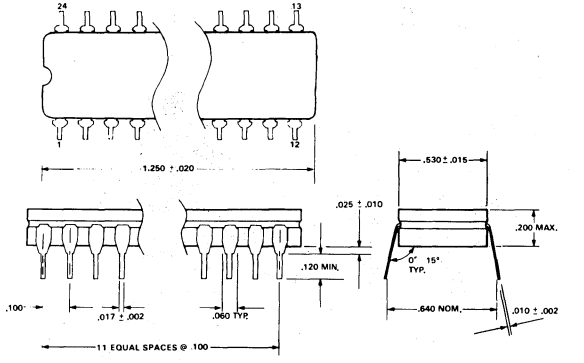

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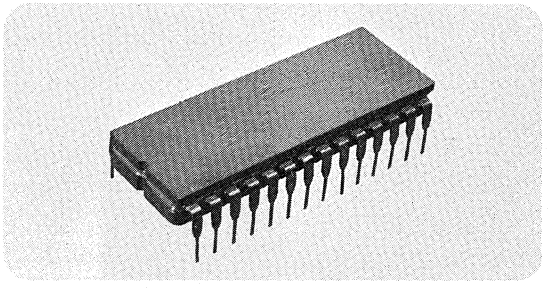

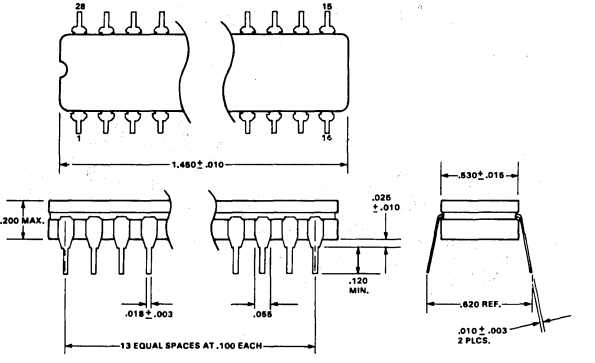

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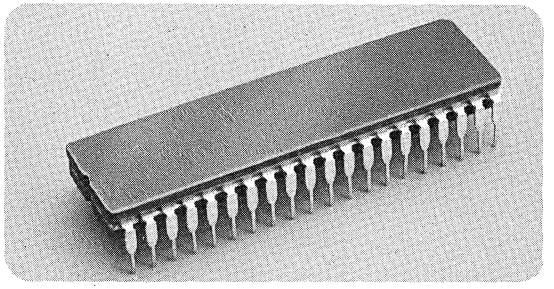
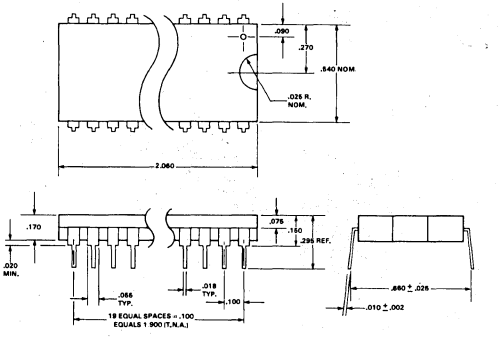
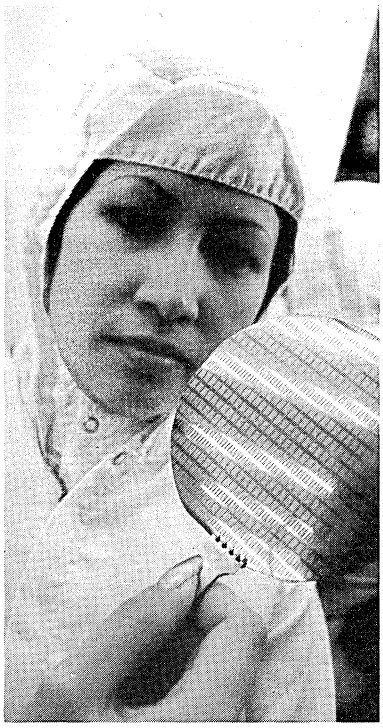
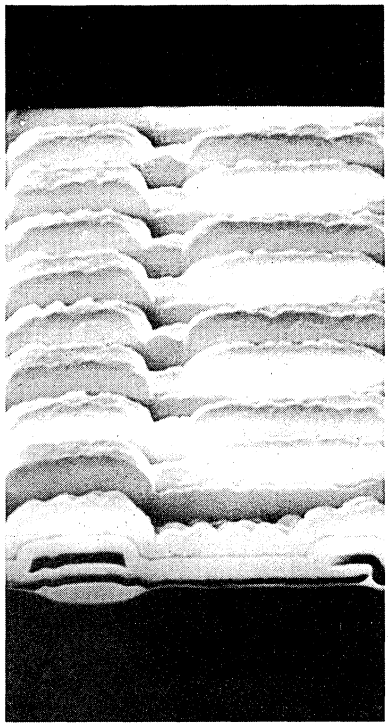


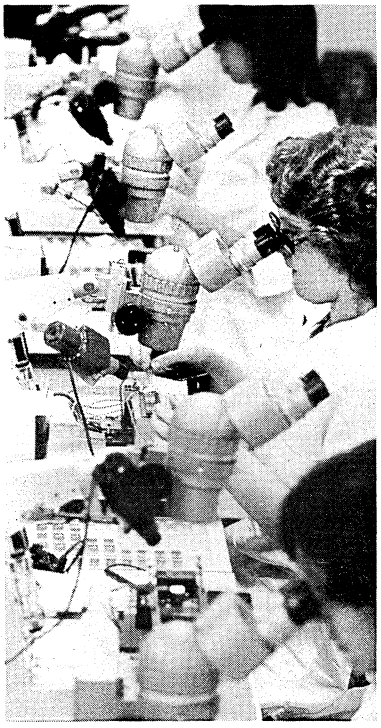


1982 TELECOMMUNICATION PRODUCTS DATA BOOK

Mostek - Technology For Today And Tomorrow







TECHNOLOGY

From its beginning, Mostek has been an innovator. From the developments of the 1K dynamic RAM and the single-chip calculator in 1970 to the current 64K dynamic RAM, Mostek technological breakthroughs have proved the benefits and cost-effectiveness of metal oxide semiconductors. Today, Mostek represents one of the industry's most productive bases of MOS/LSI technology, including Direct-Step-on-Wafer processing and ion-implantation techniques.

The addition of the Microelectronics Research Center in Colorado Springs adds a new dimension to Mostek circuit design capabilities. Using the latest computer-aided design techniques, center engineers will be keeping ahead of the future with new technologies and processes.

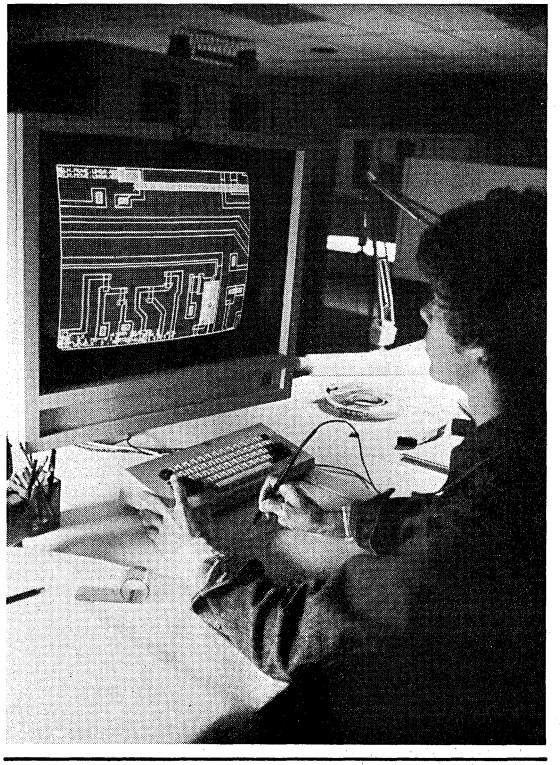
QUALITY

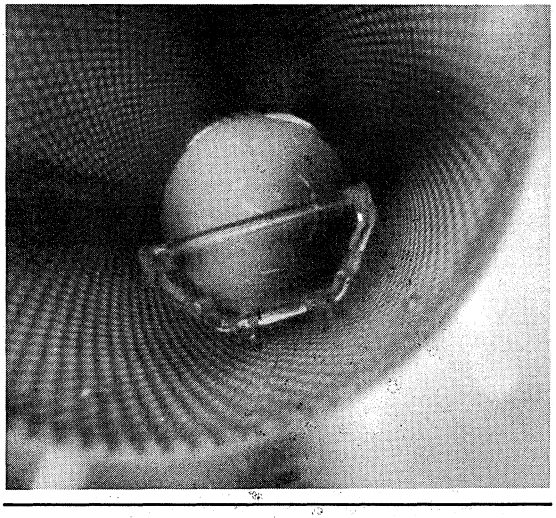
The worth of a product is measured by how well it is designed, manufactured and tested and by how well it works in your system.

In design, production and testing, the Mostek goal is meeting specifications the first time on every product. This goal requires strict discipline from the company and from its individual employees. Discipline, coupled with very personal pride, has enabled Mostek to build in quality at every level of production.

PRODUCTION CAPABILITY

The commitment to increasing production capability has made Mostek the world's largest manufacturer of dynamic RAMs. We entered the telecommunications market in 1974 with a tone dialer, and have shipped millions of telecom circuits since then. More than two million of our MK3870 single-chip microprocessors are in use throughout the world. To meet the demand, production capability is being constantly increased. Recent construction in Dallas, Ireland and Colorado Springs has added some 50 percent to the Mostek manufacturing capacity.





THE PRODUCTS

Telecommunication Products

Mostek is the leading supplier of tone dialers, pulse dialers, and CODEC devices. As each new generation of telecommunications systems emerges, Mostek is ready with new generation components, including PCM filters, tone decoders, repertory dialers, new integrated tone dialers, and pulse dialers.

These products, many of them using CMOS technology, represent the most modern advancements in telecommunications component design.

Industrial Products

Mostek's line of Industrial Products offers a high degree of versatility per device. This family of components includes various microprocessor-compatible A/D converters, a counter/time-base circuit for the division of clock signals, and combined counter/display decoders. As a result of the low parts count involved, an economical alternative to discrete logic systems is provided.

Memory Products

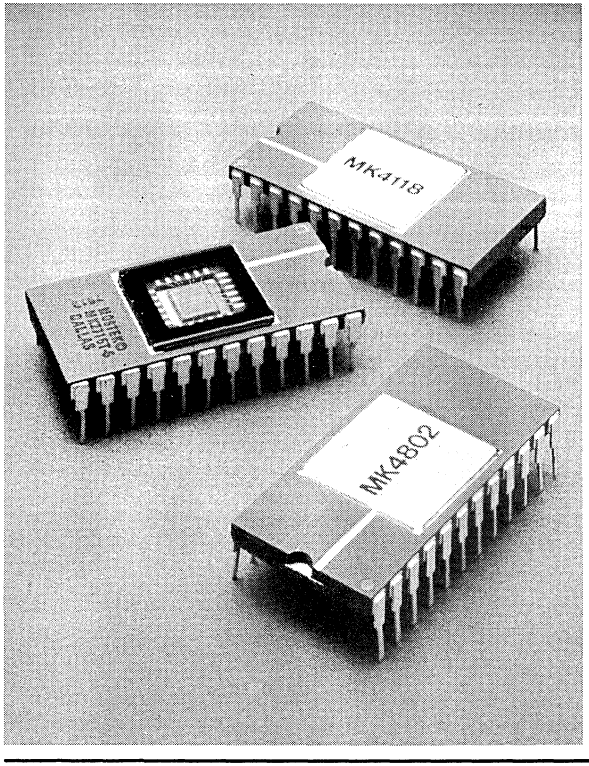
Through innovations in both circuit design, wafer processing and production, Mostek has become the industry's leading supplier of memory products.

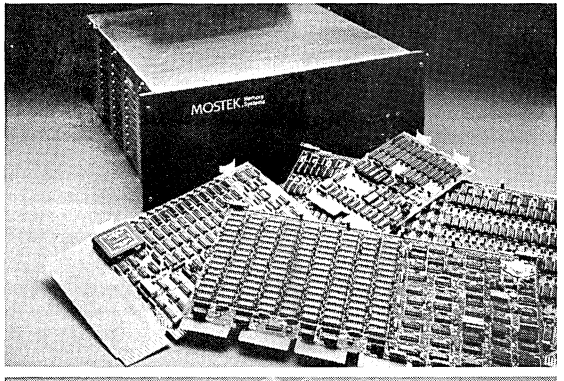
An example of Mostek leadership is our new BYTEWYDE™ family of static RAMs, ROMs, and EPROMs. All provide high performance, N words x 8-bit organization and common pin configurations to allow easy system upgrades in density and performance. Another important product area is fast static RAMs. With major advances in technology, Mostek static RAMs now feature access times as low as 55 nanoseconds. With high density ROMs and PROMs, static RAMs, dynamic RAMs and pseudostatic RAMs, Mostek now offers one of industry's broadest and most versatile memory product lines.

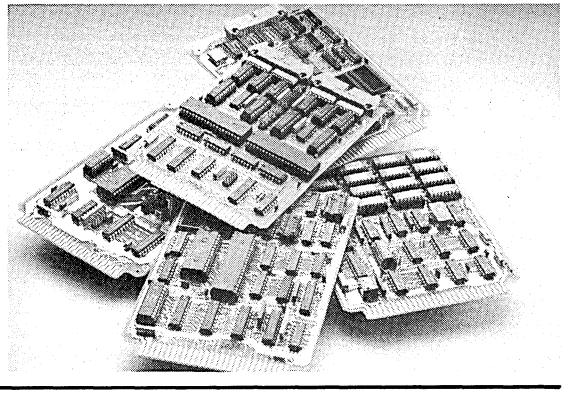
Microcomputer Components

Mostek's microcomputer components are designed for a wide range of applications.

Our Z80 family is today's industry standard 8-bit microcomputer. The MK3870 family is one of the industry's most popular 8-bit single-chip microcomputers, offering upgrade options in ROM, RAM and I/O, all in the same socket. The 38P7X EPROM versions support and prototype the entire family.







Microcomputer Systems

Complementing the component product line is the powerful MATRIX™ microcomputer development system, a Z80-based, dual floppy-disk system that is used to develop and debug software and hardware for all Mostek microcomputers.

A software operating system, FLP-80DOS, speeds and eases the design cycle with powerful commands. BASIC, FORTRAN, and PASCAL are also available for use on the MATRIX.

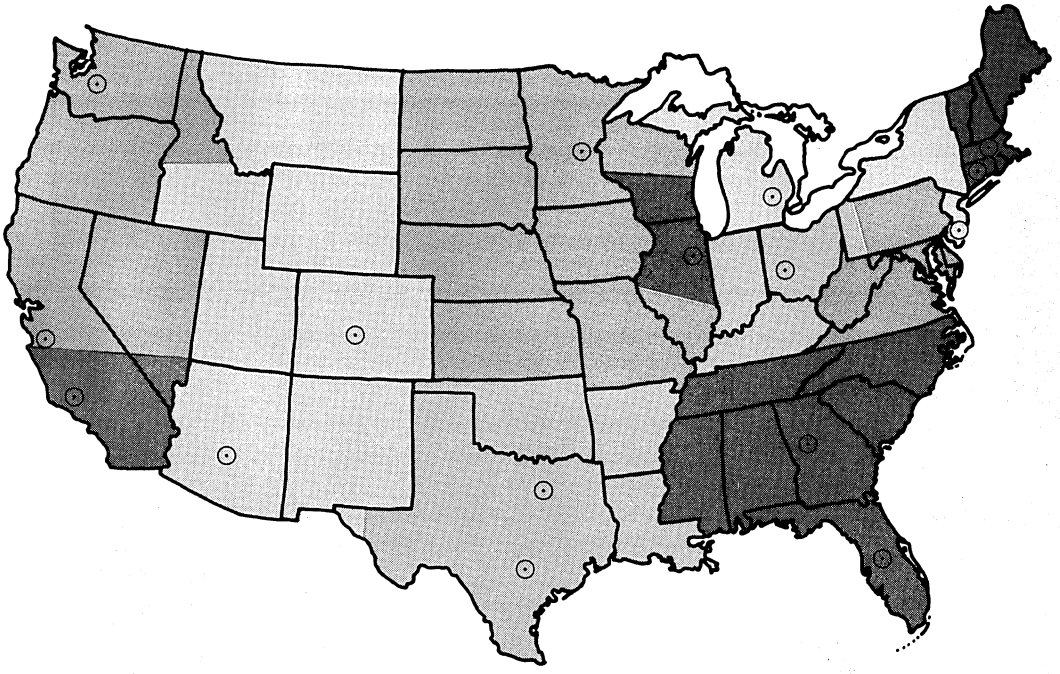
Mostek's MD Series™ features both stand-alone microcomputer boards and expandable microcomputer boards. The expandable boards are modularized by function, reducing system cost because the designer buys only the specific functional modules his system requires. All MDX boards are STD-Z80 BUS compatible.

Memory Systems

Taking full advantage of our leadership in memory components technology, Mostek Memory Systems offers a broad line of products, all with the performance and reliability to match our industry-standard circuits. Mostek Memory Systems offers add-in memory boards for popular DEC and Data General minicomputers.

Mostek also offers special purpose and custom memory boards for special applications.

U.S. AND CANADIAN SALES OFFICES



CORPORATE HEADQUARTERS

Mostek Corporation
1215 W. Crosby Rd.
P. O. Box 169
Carrollton, Texas 75006

REGIONAL OFFICES

Northeastern Area
Mostek
49 W. Putnam, 3rd Floor
Greenwich, Conn. 06830
203/622-0955
TWX 710-579-2928

Northeast U.S.
Mostek
29 Cummings Park, Suite #426
Woburn, Mass. 01801
617/935-0635
TWX 710-348-0459

Southeastern Area
Mostek
4001B Greentree Executive Campus
Route #73
Marlton, New Jersey 08053
609/596-9200
TWX 710-940-0103

Southeast U.S.
Mostek
13907 N. Dale Mabry Highway
Suite 201
Tampa, Florida 33618
813/962-8338
TWX 810-876-4611

Atlanta Region
2 Exchange Place
2300 Peachford Rd. #2105
Atlanta, GA 30338
404/458-7922
TWX 810-757-4231

Upstate NY Region
Mostek
4651 Crossroads Park Dr., Suite 201
Liverpool, NY 13088
315/457-2160
TWX 710-545-0255

Florida Region
Mostek
22521 Southwest 66th Ave.
Apt. A211
Boca Raton, FL 33433
305/483-2483

Chicago Region
Mostek
Two Crossroads of Commerce
Suite 360
Rolling Meadows, Ill. 60008
312/577-9870
TWX 910-291-1207

North Central U.S.
Mostek
6101 Green Valley Dr.
Bloomington, Mn. 55438
612/831-2322
TWX 910-576-2802

South Central U.S.
Mostek
3400 S. Dixie Ave.
Suite 101
Kettering, Ohio 45439
513/299-3405
TWX 810-459-1625

Michigan
Mostek
Orchard Hill Place
21333 Haggerty Road
Suite 321
Novi, MI 48050
313/348-8360
TWX 810-242-1471

Central U.S.
Mostek
4100 McEwen Road
Suite 151
Dallas, Texas 75234
214/386-9340
TWX 910-860-5437

Southwest Region
Mostek
4100 McEwen Road
Suite 237
Dallas, Texas 75234
214/386-9141
TWX 910-860-5437

Chevy Chase #4
7715 Chevy Chase Dr., Suite 116
Austin, TX 78752
512/458-5226
TWX 910-874-2007

Western Region
Northern California
Mostek
1762 Technology Drive
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San Jose, Calif. 95110
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TWX 910-338-7338

Seattle Region
Mostek
1107 North East 45th St.
Suite 411
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TWX 910-444-4030

Southern California
Mostek
18004 Skypark Circle
Suite 140
Irvine, Calif. 92714
714/549-0397
TWX 910-595-2513

Arizona Region
Mostek
2150 East Highland Ave.
Suite 101
Phoenix, AZ 85016
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TWX 910-957-4581

Denver Region
3333 Quebec Street, #9090
Denver, CO 80207
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TWX 910-931-2583

U.S. AND CANADIAN REPRESENTATIVES

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205/881-5031
TWX 810-726-2136

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FLORIDA
Conley & Associates, Inc.*
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235 S. Central
Oviedo, FL 32765
305/365-3283
TWX 810-856-3520

Conley & Associates, Inc.
4021 W. Waters
Suite 2
Tampa, FL 33614
813/885-7658
TWX 810-876-9136

Conley & Associates, Inc.
P.O. Box 700
1612 N.W. 2nd Avenue
Boca Raton, FL 33432
305/395-6108
TWX 510-953-7548

GEORGIA
Conley & Associates, Inc.
3951 Pleasantdale Road
Suite 201
Doraville, GA 30340
404/447-6992
TWX 810-766-0488

ILLINOIS
Carlson Electronic Sales*
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INDIANA
Rich Electronic Marketing*
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Rich Electronic Marketing
3448 West Taylor St.
Fort Wayne, IN 46804
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TWX 810-332-1404

IOWA
Carlson Electronic Sales
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Cedar Rapids, IA 52402
319/377-6341
TWX 910-222-1819

REP Associates
980 Areca Ave.
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107 N. Chester Street
Olathe, KN 66061
913/764-2700
Wichita 316/683-0206
TWX 910-749-6404

KENTUCKY
Rich Electronic Marketing
5910 Bardstown Road
P. O. Box 91147
Louisville, KY 40291
502/239-2747
TWX 810-535-3757

MARYLAND
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Ellicott City, MD 21043
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TWX 710-862-1874

MASSACHUSETTS
New England Technical Sales*
135 Cambridge Street
Burlington, MA 01803
617/272-0434
TWX 710-332-0435

MICHIGAN
Action Components
21333 Haggerty Road
Suite 201
Novi, MI 48050
313/349-3940

MINNESOTA
Cahill, Schmitz & Cahill, Inc.*
315 N. Pierce
St. Paul, MN 55104
612/646-7217
TWX 910-563-3737

MISSOURI
Rush & West Associates
481 Melanie Meadows Lane
Ballwin, MO 63011
314/394-7271

NORTH CAROLINA
Conley & Associates, Inc.
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Raleigh, NC 27609
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TWX 510-928-1829

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Precision Sales Corp.
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Drake Road
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141 E. Aurora Road
Northfield, Ohio 44067
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TWX 810-427-9210

OREGON
Northwest Marketing Assoc.
9999 S.W. Wilshire St.
Suite 124
Portland OR 97225
503/297-2581
TELEX 36-0465 (AMAPORT PTL)

TENNESSEE
Conley & Associates, Inc.
1128 Tusculum Blvd.
Suite D
Greenville, TN 37743
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TEXAS
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Addison, TX 75001
214/387-2489
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Southern States Marketing, Inc.
7745 Chevy Chase
Suite 219
Austin, TX 78752
512/452-9459

Southern States Marketing, Inc.
9730 Town Park Drive, Suite 105
Houston, Texas 77036
713/988-0991
TWX 910-881-1630

UTAH
Waugaman Associates
2520 S. State Street
Suite #159
Salt Lake City, UT 84115
801/467-4263
TWX 910-925-4073

WASHINGTON
Northwest Marketing Assoc.*
12835 Bellevue-Redmond Rd.
Suite 203E
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TWX 910-443-2445

WISCONSIN
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CANADA
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1573 Laperriere Ave.
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Canada K1Z 7T3
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83 Galaxy Blvd., Unit 1A
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TWX 610-492-2655

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Kierulff Electronics
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TWX 910/936-0770

CONNECTICUT
Arrow Electronics
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203/265-7741
TWX 710/476-0162

Schweber Electronics
Finance Drive
Commerce Industrial Park
Danbury, CT 06810
203/792-3500
TWX 710/456-9405

FLORIDA
Arrow Electronics
1001 N.W. 62nd St.
Suite 108
Ft. Lauderdale, FL 33309
305/776-7790
TWX 510/955-9456

Arrow Electronics
115 Palm Bay Road, NW
Suite 10, Bldg. 200
Palm Bay, FL 32905
305/725-1480
TWX 510-959-6337

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1982 TELECOMMUNICATION PRODUCTS DATA BOOK

Integrated Tone Dialer
MK5087(N/P/J)

FEATURES

- Pin-for-pin compatible with MK5085 with improved performance
- Direct telephone-line operation with no external power supply
- Auxiliary switching functions on chip
- Low standby power
- Minimum external parts count
- Uses inexpensive 3.579545 MHz television color-burst crystal to provide high-accuracy tones
- On-chip regulation of dual-and single-tone amplitudes
- Uses low-cost calculator-type keyboard (Form A contact) or standard 2-of-8 keyboard
- Multiple key entry pin-selectable to either single tone or no tone

DESCRIPTION

The MK5087 is a monolithic integrated circuit fabricated using the complementary-symmetry MOS (CMOS) process. A member of the TONE II* family of integrated tone dialers, the MK5087 uses an inexpensive crystal reference to provide eight different audio sinusoidal frequencies, which are mixed to provide tones suitable for Dual-Tone-Multi-Frequency (DTMF) telephone dialing.

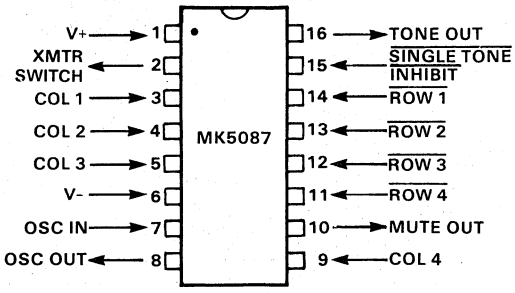
The MK5087 was designed specifically for integrated tone-dialer applications that require the following: wide-supply operation with regulated output, auxiliary switching functions, single-contact keyboard inputs, and Single Tone Inhibit option.

Keyboard entries to the TONE II* family of integrated tone dialers cause the selection of the proper divide ratio to obtain the required two audio frequencies from the 3.579545 MHz reference oscillator. D-to-A conversion is accomplished on-chip by a conventional R-2R ladder network. The tone output is a stairstep approximation to a sine wave and requires little or no filtering for low-distortion applications. The same operational amplifier that accomplishes the current-to-voltage transformation necessary for the D-to-A converter also mixes the low and high-group signals. Frequency stability of this type of tone generator is such that no frequency adjustment is needed to meet standard DTMF specifications.

* Trademark of Mostek Corporation

PIN CONNECTIONS

Figure 1



Pin connections are shown in Figure 1 and a block diagram is shown in Figure 2.

FUNCTIONAL DESCRIPTION

V+, Pin 1

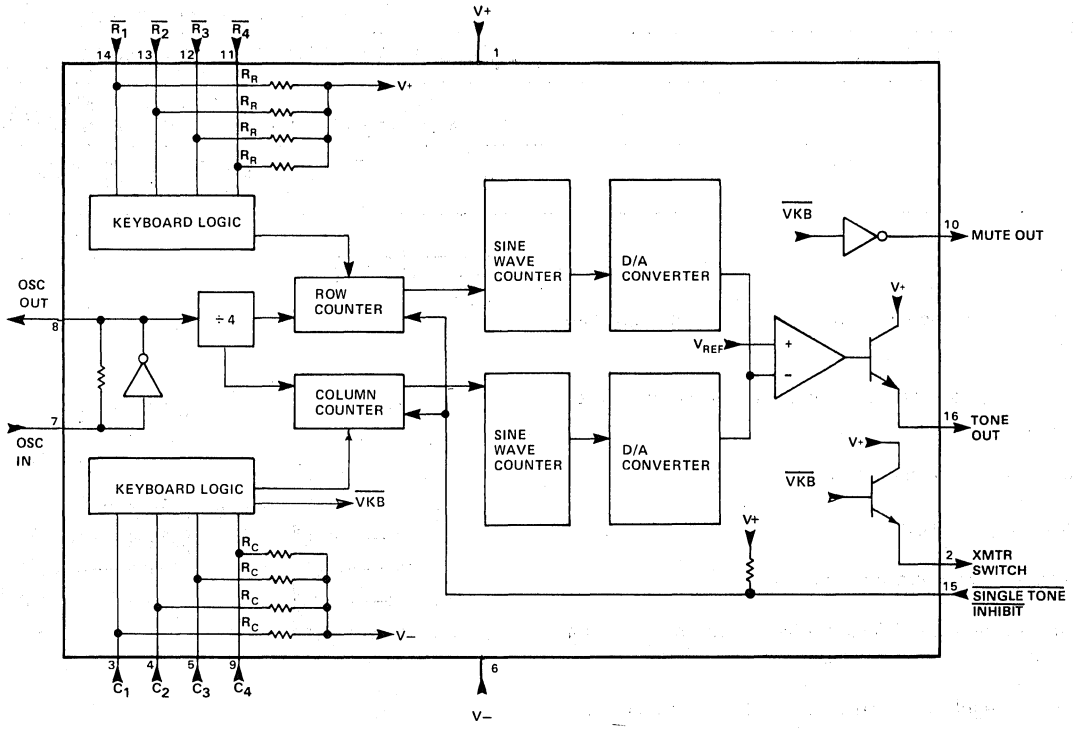
Pin 1 is the positive supply pin. The voltage on Pin 1 should be between 3.5 and 10.0 volts, measured relative to V- (Pin 6).

XMTR SWITCH, Pin 2

Pin 2 is connected to the emitter of an on-chip bipolar transistor whose collector is connected to V+. With no keyboard input this transistor is turned on and pulls Pin 2 up to within V_{BE} of the V+ supply. When a keyboard entry is sensed, this output goes open circuit (high impedance). The XMTR Switch output switches regardless of the state of the Single Tone Inhibit input.

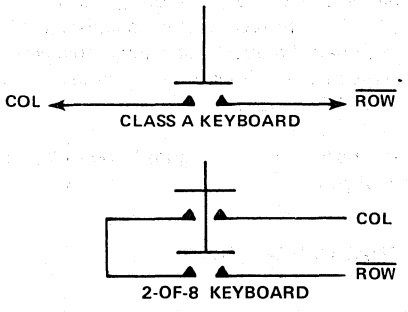
MK5087 BLOCK DIAGRAM

Figure 2



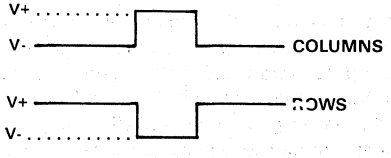
KEYBOARD CONFIGURATIONS

Figure 3



ELECTRONIC INPUT

Figure 4



ROW-COL INPUTS, Pins 3, 4, 5, 9, 11, 12, 13, 14

The MK5087 features inputs compatible with the standard 2-of-8 keyboard, the inexpensive single-contact (Form A) keyboard, and electronic input. Figure 3 shows how to connect to the two keyboard types and Figure 4 shows waveforms for electronic input. The inputs are static, i.e. there is no noise generation as occurs with scanned or dynamic inputs.

The internal structure of the MK5087 inputs is shown in Figure 5. R_R and R_C pull in opposite directions and hold their associated input sensing circuit turned off. When one or more row or column inputs are tied together, however, the input sensing circuits sense the "½ Level" and deliver a logic signal to the internal circuitry of the MK5087 and cause the proper tone or tones to be generated.

When operating with a keyboard, normal operation is for dual-tone generation when any single button is pushed, and single-tone operation when one or more buttons in the same row or column is pushed. Activation of diagonal buttons will result in no tones being generated.

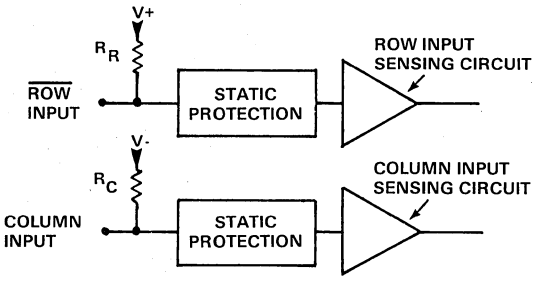
When the inputs to the MK5087 are electronically activated, per Figure 4, input to a single row and column will result in that dual-tone digit's being generated. Input to a

single column will result in that column tone being generated. Input to multiple columns will result in no tone being generated.

Activation of a single row is not sensed by the internal circuitry of the MK5087. If a single-row tone is desired, two columns must be activated along with the desired row.

ROW AND COLUMN INPUTS

Figure 5



V-, Pin 6

Pin 6 is the power supply return pin and it is the measurement reference for V+ (Pin 1).

OSC IN, Pin 7; OSC OUT, Pin 8

The MK5087 contains an on-board inverter with sufficient loop-gain to provide oscillation when working with a low-cost television color-burst crystal. The inverter's input is Osc In (Pin 7) and output is Osc Out (Pin 8). The circuit is designed to work with a crystal cut to 3.579545 MHz to give the frequencies in Table 1. The oscillator is disabled whenever a keyboard input is not sensed.

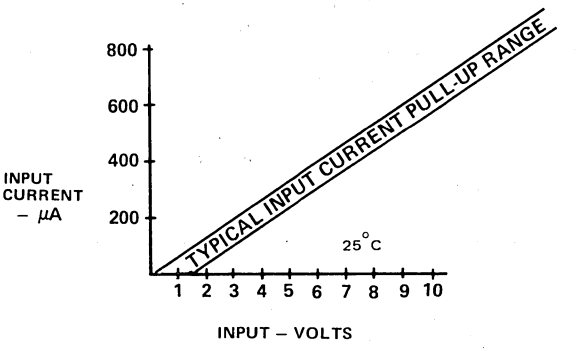
Any crystal frequency deviation from 3.579545 MHz will be reflected in the tone output frequency. Most crystals do not vary more than ± .02%.

MUTE OUT, Pin 10

The Mute output is a conventional CMOS gate that pulls to V– with no keyboard input and pulls to the V+ supply when a keyboard entry is sensed. This output is used to control auxiliary switching functions that are required to actuate upon keyboard input. The Mute output switches regardless of the state of the $\overline{\text{Single Tone Inhibit}}$ input.

INPUT CURRENT VS. INPUT VOLTAGE

Graph 1



OUTPUT FREQUENCY DEVIATION

Table 1

		Standard DTMF (Hz)	Tone Output Frequency Using 3.579545 MHz Crystal	% Deviation From Standard	
ROW	f_1	697	701.3	+0.62	LOW GROUP
	f_2	770	771.4	+0.19	
	f_3	852	857.2	+0.61	
	f_4	941	935.1	-0.63	
COL	f_5	1209	1215.9	+0.57	HIGH GROUP
	f_6	1336	1331.7	-0.32	
	f_7	1477	1471.9	-0.35	
	f_8	1633	1645.0	+0.73	

$\overline{\text{SINGLE TONE INHIBIT}}$, Pin 15

The $\overline{\text{Single Tone Inhibit}}$ input is used to inhibit the generation of other than dual tones. It has a pull-up to the V+ supply and, when left floating or tied to V+, single or dual tones may be generated as described in the paragraph under row-column inputs. When forced to the V– supply, any input situation that would normally result in a single tone will now result in no tone, with all other chip functions operating normally.

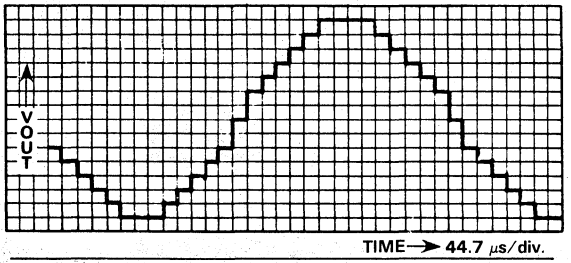
TONE OUT, Pin 16

The output pin is connected internally in the MK5087 to the emitter of an npn transistor whose collector is tied to V+. The input to this transistor is the on-chip operational amplifier which mixes the row and column tones together.

The level of a dual-tone output is the sum of the levels of a single-row and a single-column output. This level is controlled by an on-chip reference which is not sensitive to variations in the supply voltage.

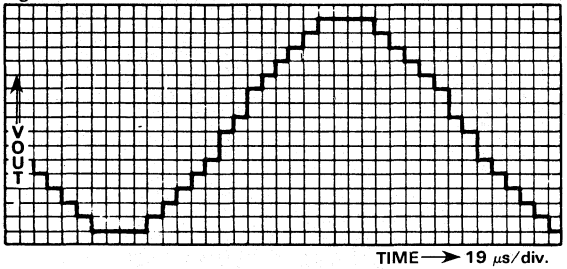
ROW 2 TONE OUTPUT

Figure 6



COLUMN 4 TONE OUTPUT

Figure 7



OUTPUT WAVEFORM

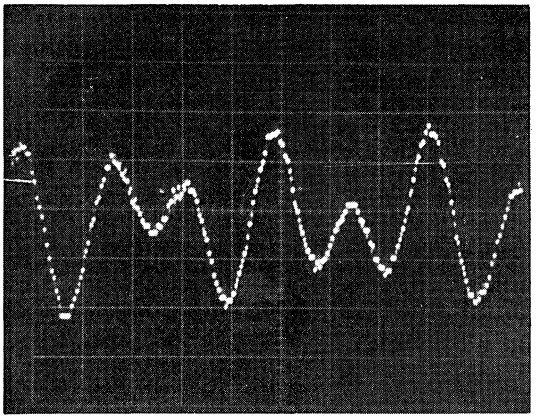
The row and column output waveforms are shown in Figures 6 and 7. These waveforms are digitally-synthesized using on-chip D-to-A converters. Distortion measurement of these unfiltered waveforms will show a typical distortion of 9% or less.

The on-chip operational amplifier of the MK5087 mixes the row and column tones to result in a dual-tone waveform. Spectral analysis of this waveform will show that typically all harmonic and intermodulation distortion components will be -30 dB when referenced to the strongest fundamental (column tone).

A commonly quoted method of dual-tone distortion measurement is the comparison of total power in the unwanted components (i.e. intermodulation and harmonic components) with the total power in the two fundamentals. For the MK5087 dual-tone waveform, THD is -20 dB maximum.

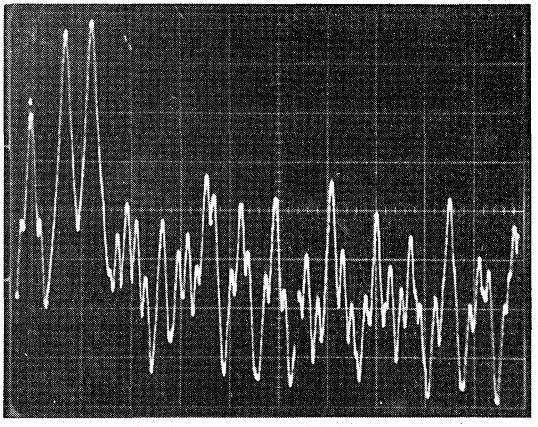
TYPICAL DUAL-TONE WAVEFORM (ROW 1, COL. 1)

Figure 8



SPECTRAL ANALYSIS OF WAVEFORM IN FIG. 8 (Vert-10 dB/div., Horizontal-1 kHz/div.)

Figure 9



A simpler measurement may be made directly from the screen of a spectrum analyzer by relating any component to one of the fundamentals. The MK5087 dual-tone spectrum will show all individual harmonic and IMD components are typically at least -30 dB with respect to the column tone.

Figures 8 and 9 show a typical dual-tone waveform and its spectral analysis.

TYPICAL APPLICATION

Figure 11 shows an application of the MK5087 in a standard telephone set that uses the standard 2500-type network. The tone levels and loop compensation that result from this application meet the requirements of the U.S. telephone systems.

ABSOLUTE MAXIMUM RATINGS*

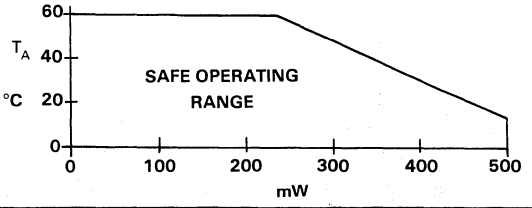
DC Supply Voltage V+ ..... 10.5 Volts
Any Input Relative to V+ ..... +0.30 Volts
Any Input Relative to V– ..... –0.30 Volts
Operating Temperature ..... –30°C to +60°C
Storage Temperature ..... –55°C to +85°C
Maximum Circuit Power Dissipation ..... 500 mW @ 25°C (see derating curve below)

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

POWER DISSIPATION DERATING CURVE

Figure 10



ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS

(-30°C ≤ T_A ≤ 60°C)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V+	DC Operating Voltage	3.5		10.0	V	1
V_{IL}	Input Voltage Low - "0"	V–		30% of V+	V	1, 11
V_{IH}	Input Voltage High - "1"	70% of V+		V+	V	1, 12
$R_{IP\overline{STI}}$	Input Pull-up Resistance, $\overline{STI}$	20		100	kΩ	3

AC CHARACTERISTICS

(–30°C ≤ T_A ≤ 60°C; 3.0 V ≤ V+ ≤ 10.0 V)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
I_{SSB}	Supply Current-Standby (Pin 6, V+ = 3.5 V) (Pin 6, V+ = 10.0 V)		 0.25 0.50	 100 200	 μA μA	 2,7 2,7
I_{SO}	Supply Current-Operating (V+ = 3.5 V) (V+ = 10.0 V)		 1.0 5.0	 2.0 15.0	 mA mA	 2,6,8,9 2,6,8,9
I_{OHX}	Output Drive, XMTR Switch-No Entry (V+ = 3.5 V, V_{OHX} = 2.5 V) (V+ = 10.0 V, V_{OHX} = 8.0 V)	 –15 –40	 –25 –100		 mA mA	
I_{OLX}	Output Drive, XMTR Switch-Valid Entry (V+ = 10.0 V, Output = 0.0 V)		0.1	10.0	μA	
I_{OHM}	Output Drive, MUTE - Valid Entry (V+ = 3.5 V, V_{OH} = 3.0 V) (V+ = 10.0 V, V_{OH} = 9.5 V)		 0.5 1.0	 2.0 4.0	 mA mA	
I_{OLM}	Output Drive, MUTE - No Entry (V+ = 3.5 V, V_{OL} = 0.5 V) (V+ = 10.0 V, V_{OL} = 0.5 V)		 0.5 1.0	 2.0 4.0	 mA mA	
Input Current Rows and Columns - SEE GRAPH 1						

AC CHARACTERISTICS (Continued)

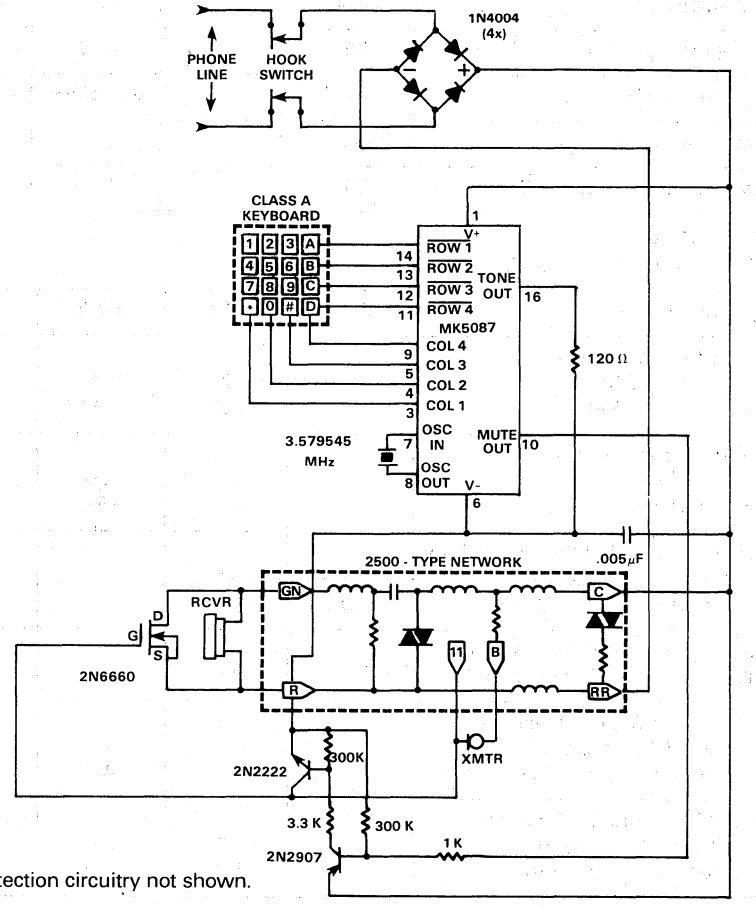
SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{NKD}	Tone Output-No Key Down			-80	dBm	
t_{RISE}	Tone Output Rise Time		3.0	5.0	ms	5,9
V_{OUT}	Tone Output Voltage Row Tone (R_L = 1K, 620 Ω, 330 Ω) Col Tone (R_L = 1K, 620 Ω, 330 Ω)	 317 396	 400 500	 504 630	 mVRMS mVRMS	 1,3,6 1,3,6
PE_{HB}	Pre-Emphasis, High Band	1.0	2.0	3.0	dB	
DIS	Output Distortion			-20	dB	4,10

NOTES:

1. All voltages referenced to V–.
2. All outputs unloaded.
3. T_A = 25°C.
4. Any row plus any column at V+ ≥ 4 volts.
5. Time from a valid keystroke with no bounce to allow wave to go from minimum to 90% of the final magnitude of either frequency.
6. True RMS Readings
7. Current Out Of Pin 6 No Key Depressed.
8. Current Out Of Pin 6 One Key Depressed.
9. Crystal parameters $R_S \leq 100\ \Omega$, L_M = 96 mH, C_M = 0.02 pF, C_h = 5 pF, f = 3.579545 MHz, C_L = 18 pF.
10. Output Distortion measured in terms of total out-of-band power relative to the sum of Row and Column fundamental power.
11. Column inputs require a voltage low (0) of 10% of V+ (max).
12. $\overline{\text{Row}}$ inputs require a voltage high (1) of 90% of V+ (min).

TYPICAL APPLICATION IN 2500-TYPE TELEPHONE

Figure 11



NOTE: Transient protection circuitry not shown.

Integrated Tone Dialer
MK5089(N/P/J)

FEATURES

- Minimum external parts count
- High-accuracy tones
- Digital divider logic, resistive ladder network, and CMOS operational amplifier on single chip
- Uses inexpensive 3.579545 MHz television color-burst crystal
- Multiple key entry pin selectable to either single tone or no tone
- Interfaces easily in electronic or μP dialing applications
- $\overline{\text{Tone Disable}}$ inhibits tone generation without defeating the Any Key Down output

DESCRIPTION

The MK5089 is a monolithic integrated circuit fabricated using the complementary-symmetry MOS (CMOS) process. A member of the TONE II* family of integrated tone dialers, the MK5089 uses an inexpensive crystal reference to provide eight different audio sinusoidal frequencies which are mixed to provide tones suitable for Dual-Tone Multi-Frequency (DTMF) telephone dialing.

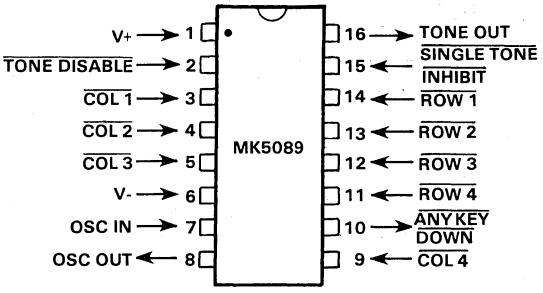
The MK5089 was designed specifically for integrated tone dialer applications that require the following: fixed supply operation, a negative-true keyboard input, $\overline{\text{Tone Disable}}$ input, stable output tone level, and an $\overline{\text{Any Key Down}}$ output that is open circuit when no keyboard buttons are pushed and pulls to the V– supply when a button is pushed.

Keyboard entries to the TONE II* family of integrated tone dialers cause the selection of the proper divide ratio to obtain the required two audio frequencies from the 3.579545 MHz reference oscillator. D-to-A conversion is accomplished on-chip by a conventional R-2R ladder network. The tone output is a stairstep approximation to a sine wave and requires little filtering for low-distortion applications. The same operational amplifier that accomplishes the current-to-voltage transformation necessary for the D-to-A converter also mixes the low- and high-group signals. Frequency stability of this type of tone generation is such that no frequency adjustment is needed to meet standard DTMF specifications.

*Trademark of Mostek Corporation

PIN CONNECTIONS

Figure 1



Pin connections are shown in Figure 1 and a block diagram is shown in Figure 2.

FUNCTIONAL DESCRIPTION

V+, Pin 1

Pin 1 is the positive supply pin. The voltage on Pin 1 should be between 3.0 and 10.0 volts, measured relative to V– (Pin 6).

$\overline{\text{TONE DISABLE}}$, Pin 2

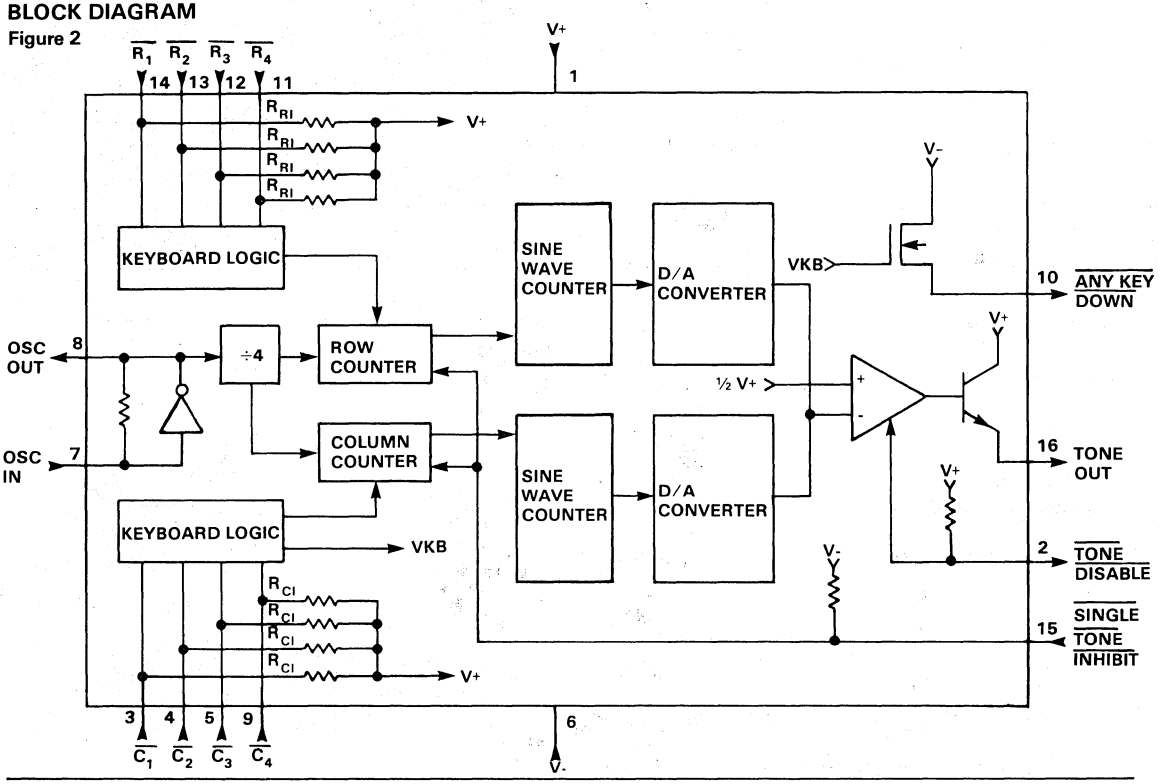
The $\overline{\text{Tone Disable}}$ input is used to defeat tone generation when the keyboard is used for other functions besides DTMF signaling. It has a pull-up to the V+ supply and, when tied to the V– supply, tones are inhibited. All other chip functions operate normally.

ROW-COLUMN INPUTS, Pins 3, 4, 5, 9, 11, 12, 13, 14

With $\overline{\text{Single Tone Inhibit}}$ at V+, connection of V– to a single column will cause the generation of that column tone. Connection of V– to more than one column will result in no

BLOCK DIAGRAM

Figure 2



FUNCTIONAL DESCRIPTION (Continued)

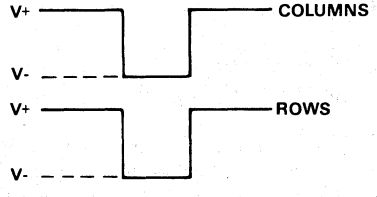
tones being generated. The application of V– to only a row pin or pins has no effect on the circuit. There must always be at least one column connected to V– for row tones to be generated. If a single-row tone is desired, it may be generated by tying any two column pins and the desired row pin to V–. Dual tones will be generated if a single-row pin and a single-column pin are connected to V–. When $\overline{\text{Single Tone Inhibit}}$ is tied to V–, only dual tones will be generated.

Each keyboard input is standard CMOS with a pull-up resistor to the V+ supply. These inputs may be controlled by a keyboard or electronic means. Open-collector TTL or standard CMOS (operated off same supply as the MK5089) may be used for electronic control. Refer to Figures 3 and 4.

The switch contacts used in the keyboards may be void of precious metals, due to the CMOS network's ability to recognize resistance up to 1 kΩ as a valid key closure.

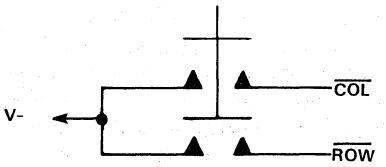
ELECTRONIC INPUT

Figure 3



2-OF-8 KEYBOARD

Figure 4



V–, Pin 6

Pin 6 is the power supply return pin and it is the measurement reference for V+ (Pin 1).

OSC IN, Pin 7; OSC OUT, Pin 8

The MK5089 contains an on-board inverter with sufficient loop-gain to provide oscillation when working with a low-cost television color-burst crystal. The inverter's input is Osc In (Pin 7) and output is Osc Out (Pin 8). The circuit is designed to work with a crystal cut to 3.579545 MHz to give the frequencies in Table 1. The oscillator is disabled whenever a keyboard input is not sensed.

Any crystal frequency deviation from 3.579545 MHz will be reflected in the tone output frequency. Most crystals do not vary more than ± .02%.

OUTPUT FREQUENCY DEVIATION

Table 1

		Standard DTMF (Hz)	Tone Output Frequency Using 3.579545 MHz Crystal	% Deviation From Standard	
Row	f_1	697	701.3	+0.62	Low Group
	f_2	770	771.4	+0.19	
	f_3	852	857.2	+0.61	
	f_4	941	935.1	-0.63	
Col	f_5	1209	1215.9	+0.57	High Group
	f_6	1336	1331.7	-0.32	
	f_7	1477	1471.9	-0.35	
	f_8	1633	1645.0	+0.73	

$\overline{\text{ANY KEY DOWN}}$, Pin 10

The $\overline{\text{Any Key Down}}$ output is used for electronic control of receiver and/or transmitter switching and other desired functions. It switches to the V- supply when a keyboard button is pushed, and is open-circuited when not. The $\overline{\text{AKD}}$ output switches regardless of the $\overline{\text{Tone Disable}}$ and $\overline{\text{Single Tone Inhibit}}$ inputs.

$\overline{\text{SINGLE TONE INHIBIT}}$, Pin 15

The $\overline{\text{Single Tone Inhibit}}$ input is used to inhibit the generation of other than dual tones. It has a pull down to the V- supply and when floating or tied to V-, any input situation that would normally result in a single tone will now result in no tone, with all other chip functions operating normally.

When forced to the V+ supply, single or dual tones may be generated as described in the paragraph under Row-Column Inputs.

TONE OUT, Pin 16

The tone output pin is connected internally in the MK5089 to the emitter of an npn transistor whose collector is tied to V+. The input to this transistor is the on-chip operational amplifier which mixes the row and column tones together and provides output level regulation.

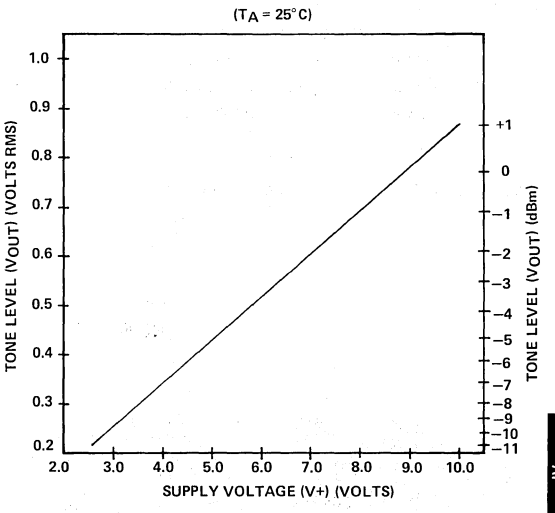
The output tone level of the MK5089 is a function of supply voltage. Figure 5 is a plot of the typical output level of a single-tone output vs. supply voltage. The level of a dual-tone output is the sum of the levels of a single-row and a single-column output.

The row and column output waveforms are shown in Figures 6 and 7. These waveforms are digitally-synthesized using on-chip D-to-A converters. Distortion measurement of these unfiltered waveforms will show a typical distortion of 7% or less.

The on-chip operation amplifier of the MK5089 mixes the row and column tones to result in a dual-tone waveform. Spectral analysis of this waveform will show that typically

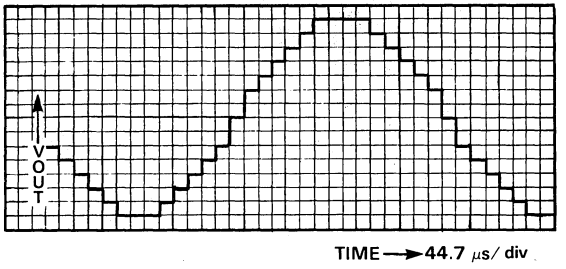
TYPICAL SINGLE-ROW LEVEL VS. SUPPLY VOLTAGE

Figure 5



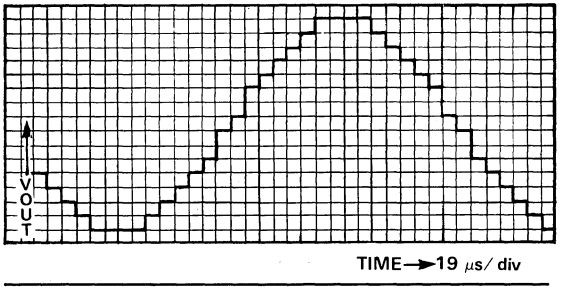
ROW 2 TONE OUTPUT

Figure 6



COLUMN 4 TONE OUTPUT

Figure 7



all harmonic and intermodulation distortion components will be -30 dB down when referenced to the strongest fundamental (column tone).

A commonly-quoted method of dual-tone distortion measurement is the comparison of total power in the unwanted components (i.e. intermodulation and harmonic components) with the total power in the two fundamentals.

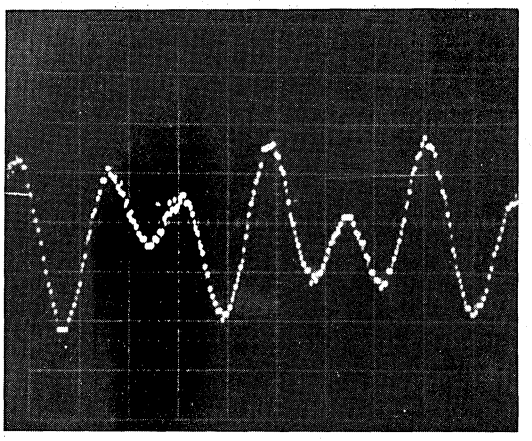
For the MK5089 dual-tone waveform, THD is -20 dB maximum.

A simpler measurement may be made directly from the screen of a spectrum analyzer by relating any component to one of the fundamentals. The MK5089 dual-tone spectrum will show all individual harmonic and IMD components are typically at least 30 dB down with respect to the column tone.

Figures 8 and 9 show a typical dual-tone waveform and its spectral analysis.

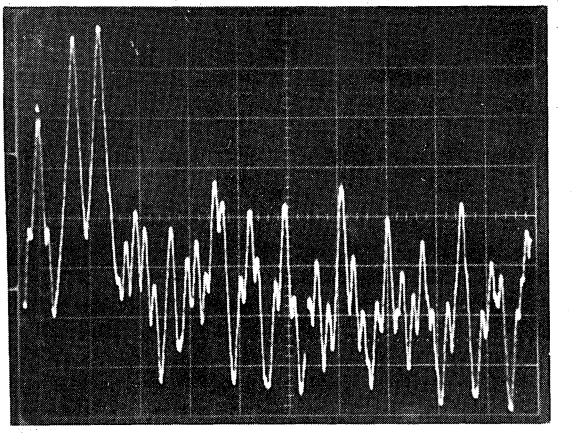
TYPICAL DUAL-TONE WAVEFORM (ROW 1, COL. 1)

Figure 8



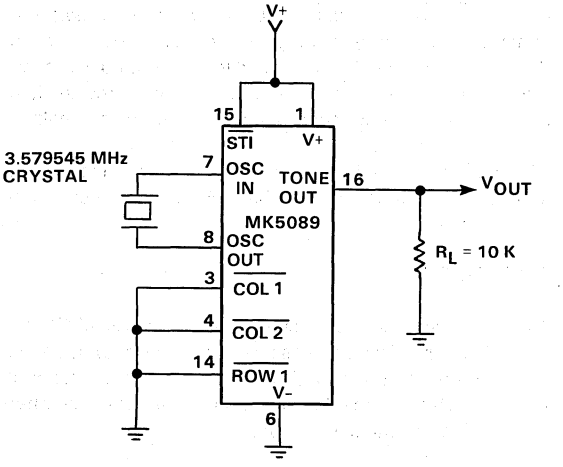
SPECTRAL ANALYSIS OF WAVEFORM IN FIG. 8 (Vert-10 dB/div, Horizontal-1kHz/div)

Figure 9



TONE LEVEL TEST CIRCUIT

Figure 10



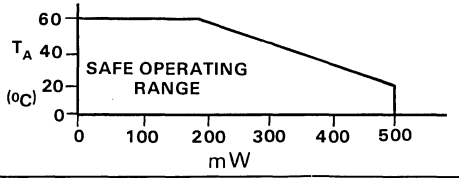
NOTE: Keyboard connections shown are for Row tone level test. Only $\overline{\text{Col 1}}$ (Pin 3) should be connected to V- for Column tone level test.

ABSOLUTE MAXIMUM RATINGS*

DC Supply Voltage V+ ..... 10.5 Volts
Any Input Relative to V+ ..... +0.30 Volts
Any Input Relative to V– ..... –0.30 Volts
Operating Temperature ..... –30°C to +60°C
Storage Temperature ..... –55°C to +85°C
Maximum Circuit Power Dissipation ..... 500 mW @ 25°C (see derating curve below)

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

POWER DISSIPATION DERATING CURVE



DERATE AT 9 mW/°C WHEN SOLDERED INTO PC BOARD.

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS

(–30°C ≤ T_A ≤ 60°C)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V+	Supply Voltage	3.0		10.0	V	
V_{IL}	Input "0"	V–		30% of V+	V	
V_{IH}	Input "1"	70% of V+		V+	V	
R_I	Input Pull-Up Resistor	20		100	kΩ	

AC CHARACTERISTICS

(–30°C ≤ T_A ≤ 60°C; 3.0 V ≤ V+ ≤ 10.0 V)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{OUT}	Tone Output (R_{LOAD} = 10 K)	-10		-7	dBm	1,7
PE_{HB}	Pre-Emphasis, High Band	2.4	2.7	3	dB	
DIS	Output Distortion			-20	dB	2,6
t_{RISE}	Rise Time		2.8	5.0	ms	3
$I_{\overline{AKD}}$	$\overline{\text{Any Key Down}}$ Sink Current to V–	500			μA @5 V	
$I_{\overline{AKDO}}$	$\overline{\text{AKD}}$ Off-Leakage			2.0	μA@5 V	
I_{SO}	Supply Current-Operating			2.0	mA@3.5 V	5
I_{SST}	Supply Current-Standby			200	μA@10.0 V	4
V_{NKD}	Tone Output - No Key Down (R_{LOAD} = 10 kΩ)			-80	dBm	

NOTES

1. Single-tone, low-group. Any V+ between 3.4 and 3.6 V. 0dBm = .775 V.
2. Any dual-tone. Any V+ between 3.4 and 10.0 V. See Figure 10 and Figure 11.
3. Time from a valid keystroke with no bounce to allow the waveform to go from min. to 90% of the final magnitude of either frequency. Crystal parameters: R_S ≤ 100 Ω, L_M = 96 mH, C_M = 0.02 pF, C_h = 5 pF, f = 3.579545 MHz ± 0.02%, C_L = 18 pF.
4. Stand-by condition is defined as no keys activated, $\overline{TD}$ = Logical 1, $\overline{\text{Single Tone Inhibit}}$ = Logical 0.
5. One key depressed only. Outputs unloaded.
6. Output Distortion measured in terms of total out-of-band power relative to the sum of Row and Column fundamental power.
7. For 3.4 V ≤ V+ ≤ 10.0 V, Tone Output is typically [0.0855 (V+) ± 1 dB] mV_{rms}. Refer to Figures 5 and 10.

MOSTEK®

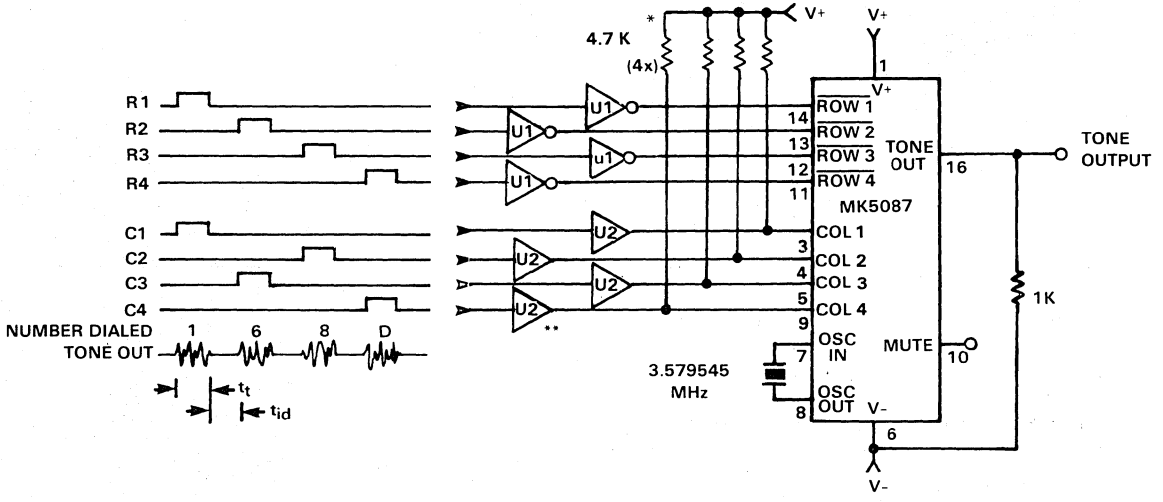
TELECOMMUNICATIONS

MK5087/89 Electronic Drive

The purpose of this application brief is to provide information as to the various means by which the MK5087 and MK5089 keyboard inputs may be electronically driven.

The MK5087 keyboard inputs can be driven by both CMOS and TTL logic. With the MK5087, the row inputs must be pulled low for a valid key entry. Since the MK5087 has internal pull-up resistors on the rows and pull-down resistors on the columns, external pull-ups are only needed when driving the column inputs with TTL open-collector logic. The circuit diagram in Figure 1 shows the interface for electronically driving the MK5087.

Figure 1



* Only needed when using TTL open-collector logic

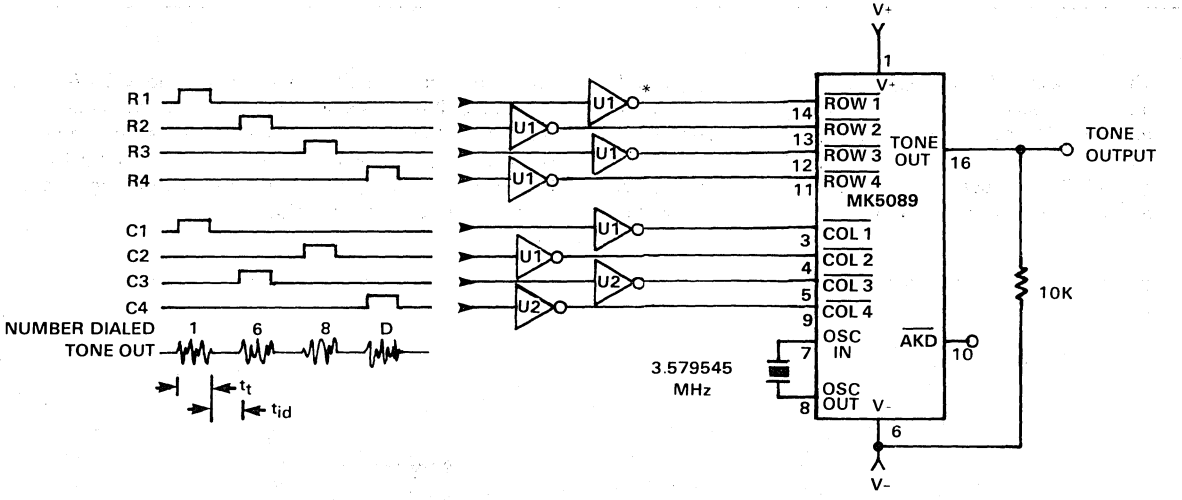
** Inverters and buffers are not needed if the driving signals R1 - R4 are inverted and R1 - C4 can drive a 4.7 kΩ load.

NOTE:

U1 is a hex inverter (TTL - 7404, 74LS04; TTL open-collector - 7405, 74LS05; CMOS - 4049)
U2 is a hex buffer (TTL open-collector - 7407, 74LS07, 7417, 74LS17; CMOS - 4050)
$t_t \geq 50$ ms and 45 ms $\geq t_{id} \geq 3$ s to meet Bell Specifications PUB 47001, section 4.3
t_t = tone duration time
t_{id} = interdigit time

The MK5089 row and column inputs must be pulled low for a valid key entry. The MK5089 has internal pull-up resistors for both the rows and columns. Therefore, the MK5089 keyboard inputs may be driven by CMOS, TTL, and TTL open-collector logic without the requirement for external pull-up resistors. The interface for electronically driving the MK5089 is shown in Figure 2.

Figure 2



* Inverters are not needed if the driving signals R1 - C4 are inverted and can drive a 20 kΩ load.

NOTE:

U1 and U2 are hex inverters (TTL - 7404, 74LS04; TTL open-collector - 7405, 74LS05; CMOS - 4049)
$t_t \geq 50$ ms and 45 ms $\geq t_{id} \geq 3$ s to meet Bell Specifications PUB 47001, section 4.3
t_t = tone duration time
t_{id} = interdigit time

V+ and V- on the MK5087 and MK5089 should be typically connected to the supply used for the electronic drive circuitry. However, care must be taken to ensure that V+ does not exceed the 10 volt maximum as specified in the MK5087 and MK5089 data sheets. The logic levels present at the MK5087 and MK5089 inputs must meet the criteria specified in the respective data sheets and repeated in Table 1. The high logic level must not exceed V+ and the low logic level must not be more negative than V-.

LOGIC LEVEL REQUIREMENTS

Table 1

	MK5087	MK5089
Column High	≥ .7 V+	≥ .7 V+
Column Low	≤ .1 V+	≤ .3 V+
Row High	≥ .9 V+	≥ .7 V+
Row Low	≤ .3 V+	≤ .3 V+

Integrated Tone Dialer

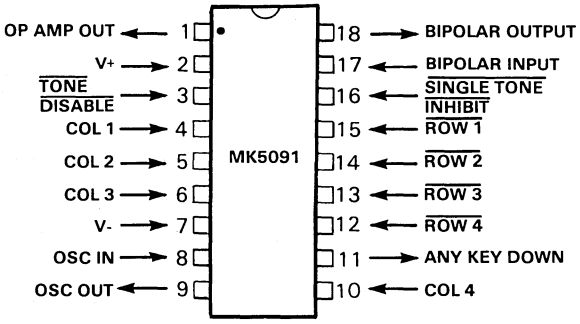
MK5091(N)

FEATURES

- CEPT Compatible
- High Accuracy tones
- Digital divider logic, resistive ladder network, CMOS operational amplifier, and Bipolar driver on chip
- Uses inexpensive 3.579545 MHz television color-burst crystal
- Invalid key entry can result in either single tone or no tone
- Designed for use with calculator type (Class A contact) keyboards or 2-of-8 keyboards
- Low standby power for continuous on line operation

PIN OUT

Figure 1



DESCRIPTION

The MK5091 is a monolithic integrated circuit fabricated using the complementary-symmetry MOS (CMOS) process. A member of the TONE II family of integrated tone dialers, and designed specifically to meet European CEPT specifications, the MK5091 uses an inexpensive crystal reference to provide eight different audio sinusoidal frequencies, which are mixed to provide tones suitable for Dual-Tone Multi-Frequency (DTMF) telephone dialing.

The keyboard entries select the proper digital dividers to divide the 3.579545 MHz to obtain the unique audio frequencies required. These digital signals are then processed by a R-2R ladder network, and current-to-voltage transformation is made by an on-chip amplifier. This is a conventional D-to-A converter and yields sine waves of sufficient purity that filtering is easily accomplished. The same amplifier accomplishes summing of the low-and-high group tones to obtain the required dual-tone signal. Frequency accuracy of the network is obtained via the crystal reference which eliminates any need for frequency adjustment.

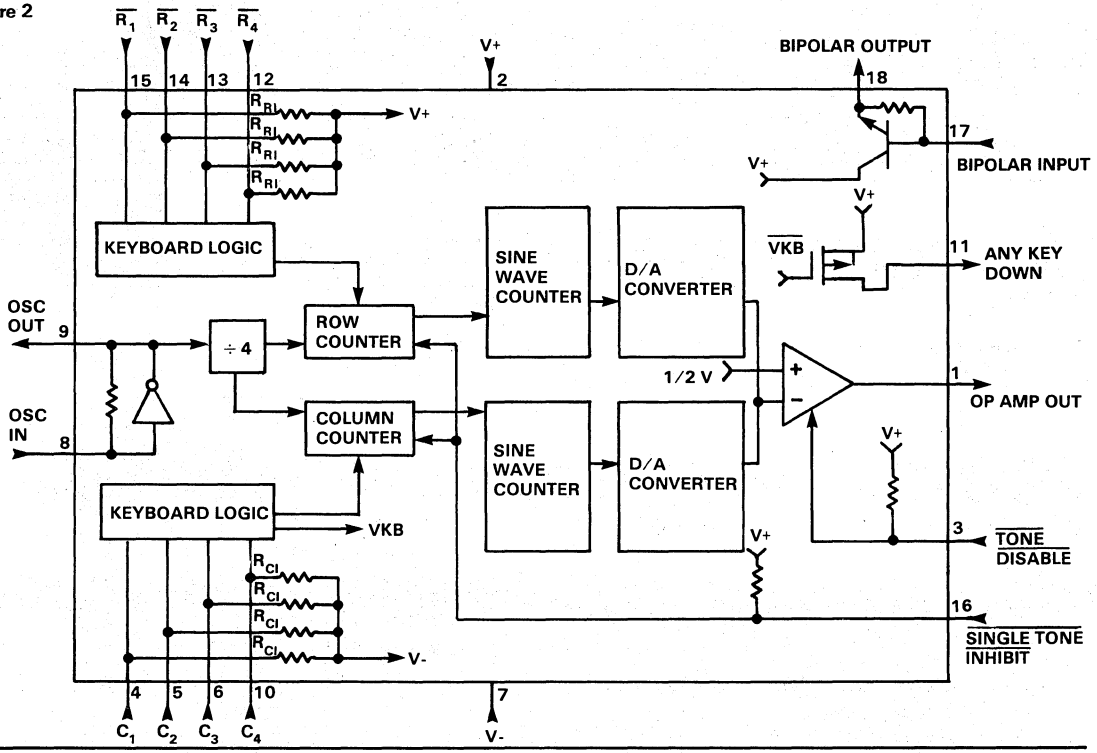
The MK5091 meets the following integrated tone dialer application requirements: compatibility with European CEPT specifications, regulated-supply operation, single contact keyboard input, Tone Disable input ($\overline{TD}$), Single Tone Inhibit input ($\overline{STI}$), stable output tone level, and an Any Key Down output (AKD) that is open circuit when no keyboard buttons are pushed, and pulls to the V+ supply when a button is pushed.

Supplied in an 18-pin plastic package, the MK5091 provides two pins for tone filtering of the multiple stairstep output sine wave. Typically, only three resistors, and two capacitors are needed to produce sine waves of sufficient purity to meet the CEPT harmonic distortion specification.

The MK5091 high group pre-emphasis before filtering is typically 2.0 dB. Output level meets European applications.

BLOCK DIAGRAM OF MK5091

Figure 2



OUTPUT TONE LEVELS

The output tone level of the MK5091 is proportional to the applied DC supply voltage. Operation will normally be with a regulated supply. This results in enhanced temperature stability, since the supply voltage may be made temperature stable.

DISTORTION

The dual tone harmonic requirement of the European CEPT specification is as follows:

The level of any individual unwanted frequency component relative to the fundamental of the low group shall not exceed the following limits. (OdBm = 0.775 Volts).

In the frequency band 300 to 3400 Hz - 33 dBm.

In the frequency band 3.4 to 50 kHz - 33 dBm at 3.4 kHz falling at 12 dB per octave to 50 kHz.

In the frequency band above 50 kHz - 80 dBm.

A two-pole filter is required to fulfill the above distortion requirements. This filter may be constructed using the bi-polar transistor available at pins 17 and 18 of the MK5091. The two poles should be placed at approximately 3.4 kHz. Additional margin may be obtained by reducing the frequency of these poles, but a practical limit is reached when the amount of pre-emphasis becomes altered.

$\overline{\text{TONE DISABLE}}$, Pin 3

The $\overline{\text{Tone Disable}}$ input is used to disable tone generation when the keyboard is used for other functions besides DTMF signaling. This input has a pull up to the V+ supply, and when left floating or connected to V+, tones are generated normally. When forced to the V- supply, tone generation is disabled. All other chip functions operate normally.

ANY KEY DOWN, Pin 11

The Any Key Down output is used for electronic control of receiver and/or transmitter switching and other desired functions. It switches to the V+ supply when a keyboard button is pushed, and is open circuited when not. The mute output switches regardless of the $\overline{\text{Tone Disable}}$ and $\overline{\text{Single-Tone Inhibit}}$ inputs.

$\overline{\text{SINGLE TONE INHIBIT}}$, Pin 16

The $\overline{\text{Single Tone Inhibit}}$ input is used to inhibit the generation of other than dual tones. It has a pull up to the V+ supply and when left floating or tied to V+, single or dual tones may be generated as described in the paragraph under row-column inputs. When forced to the V-supply, any

input situation that would normally result in a single tone will now result in no tone, with all other chip functions operating normally.

OSCILLATOR

The network contains an on-board inverter with sufficient loop-gain to provide oscillation when working with a low cost television color-burst crystal. The inverter's input is OSC IN (pin 8) and output is OSC OUT (pin 9). The circuit is designed to work with a crystal cut to 3.579545 MHz to give the frequencies in Table 1.

Any crystal frequency deviation from 3.579545 MHz will be reflected in the tone output frequency. Most crystals do not vary more than ± .02%.

OUTPUT FREQUENCY DEVIATION

Table 1

	Standard DTMF (Hz)	Tone Output Frequency Using 3.579545 MHz Crystal	% Deviation From Standard
ROW f_1	697	701.3	+0.62
ROW f_2	770	771.4	+0.19 LOW
ROW f_3	852	857.2	+0.61 GROUP
ROW f_4	941	935.1	-0.63
COL f_5	1209	1215.9	+0.57
COL f_6	1336	1331.7	-0.32 HIGH
COL f_7	1477	1471.9	-0.35 GROUP
COL f_8	1633	1645.0	+0.73

OP AMP OUT, Pin 1

The op amp out pin is connected internally in the MK5091 to the CMOS output transistor of an operational amplifier. This operational amplifier mixes an output level referenced to the supply voltage.

BIPOLAR INPUT, Pin 17

The bipolar input pin is connected internally in the MK5091 to the base of a un-committed on-chip bipolar transistor. This transistor is generally used to construct a multi-pole filter for low distortion applications.

BIPOLAR OUTPUT, Pin 18

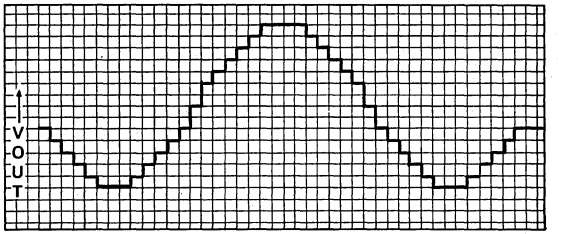
The bipolar output pin is connected internally in the MK5091 to the emitter of the bipolar transistor described by the paragraph Bipolar Input, above.

OUTPUT WAVEFORM

The row column output waveforms are shown in Figures 3 and 4. These waveforms are digitally synthesized using on-chip D-to-A converters. Distortion measurements of these unfiltered waveforms will show a typical distortion of 7% or less.

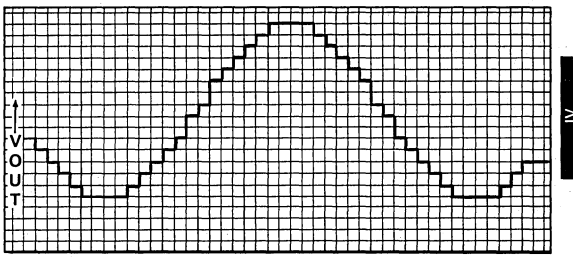
ROW 2 TONE OUTPUT

Figure 3



COLUMN 4 TONE OUTPUT

Figure 4

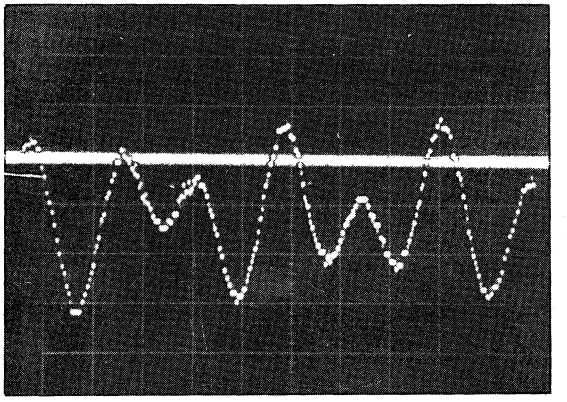


The on-chip operational amplifier of the MK5091 mixes the row and column tones together to result in a dual-tone waveform. Spectral analysis of this waveform will show that typically all harmonic and intermodulation distortion components will be -30 dB down when referenced to the strongest fundamental (column tone).

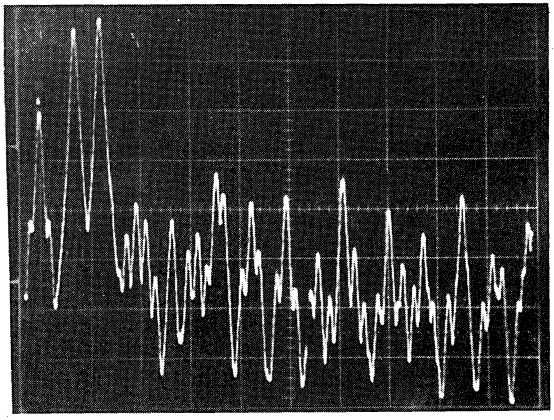
Figures 5 and 6 show a typical dual tone waveform and its spectral analysis.

TYPICAL DUAL TONE WAVEFORM (ROW 1, COL 1)

Figure 5



SPECTRAL ANALYSIS OF WAVEFORM
(Vert-10 dB/div, Horizontal-1 kHz/div)
Figure 6



ROW AND COLUMN INPUTS

The MK5091N features inputs compatible with the standard 2-of-8 keyboard, the inexpensive single contact (form A) keyboard, and electronic input. Figure 7 shows how to connect to the two keyboard types and Figure 8 shows waveforms for electronic input. The inputs are static, i.e. there is no noise generation as occurs with scanned or dynamic inputs.

The internal structure of the MK5091N inputs is shown in Figure 9. R_{RI} and R_{CI} pull in opposite directions and hold their associated input sensing circuit turned off. When one or more row or column inputs are tied together, however, the Input Sensing Circuits sense the "1/2 Level" and deliver a logic signal to the internal circuitry of the MK5091 and cause the proper tone or tones to be generated.

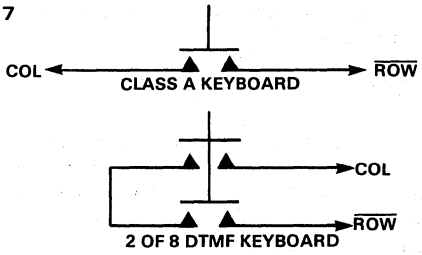
When operating with a keyboard, normal operation would be with $\overline{STI}$ floating or at V+. This allows single-tone operation when more than one button is activated. Activation of diagonal buttons will result in no tones being generated.

If a single tone is desired for test, but is not desired for operation, $\overline{STI}$ can be connected to V-. This allows dual-tone operation with single key closure, but prevents any output tones when more than one button in the same row or column is activated.

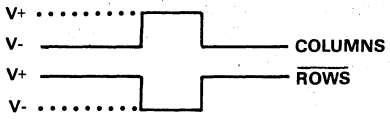
When the inputs to the MK5091 are electronically activated, per Figure 8, input to a single row and column will result in that dual-tone digit's being generated. Input to a single column will result in that column-tone being generated. Input to multiple columns will result in no tone being generated.

Activation of a single row is not sensed by the internal circuitry of the MK5091N. If a single row tone is desired, two columns must be activated along with the desired row.

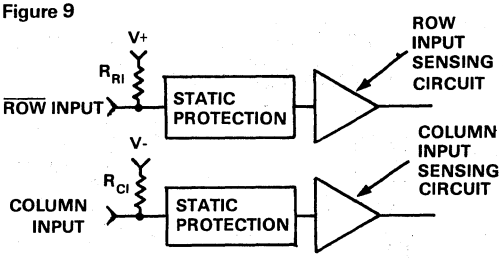
KEYBOARD CONFIGURATION
Figure 7



ELECTRONIC INPUT
Figure 8

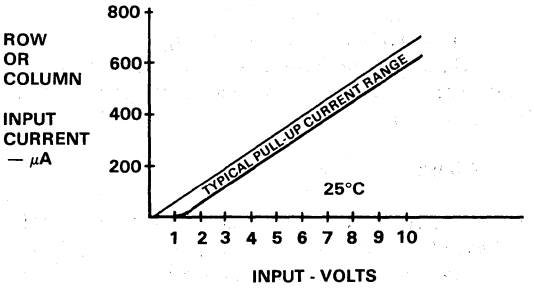


ROW AND COLUMN INPUTS
Figure 9

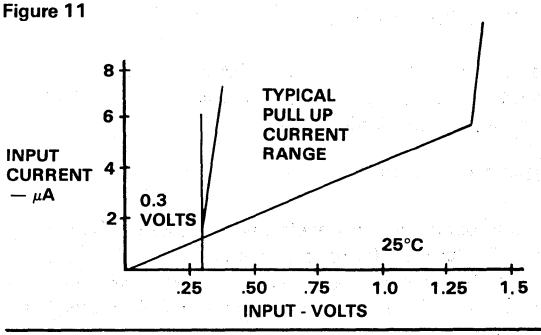


Typical input impedances of row and column pull-up resistors may be inferred from Figures 10 and 11.

INPUT-VOLTS
Figure 10



ROW OR COLUMN INPUT VOLTS
Figure 11

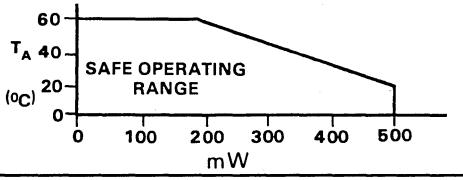


ABSOLUTE MAXIMUM RATINGS*

Supply Voltage V+ ..... 10.5 Volts
Voltage on any pin relative to V- ..... -0.3 Volts
Voltage on any pin relative to V+ ..... +0.3 Volts
Operating Temperature, T_A ..... -30°C to +60°C
Storage Temperature ..... -55°C to +85°C
Maximum circuit power dissipation ..... 500 mW, @ 25°C, See derating curve

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

POWER DISSIPATION DERATING CURVE



DERATE AT 9 mW/°C WHEN SOLDERED INTO PC BOARD.

OPERATING CHARACTERISTICS

-30°C ≤ T_A ≤ +60°C; all voltages referenced to V- = 0.0 volts

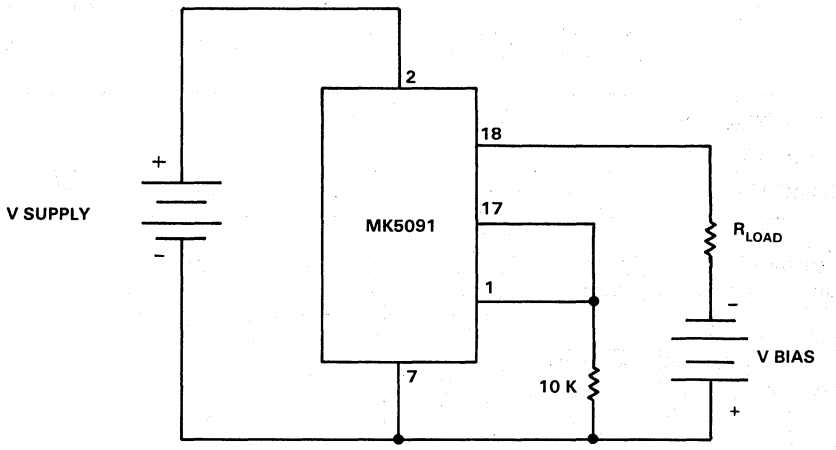
SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
	Supply Voltage					
V+	Operating (Generating Tones)	3.0		10.0	V	
V+	Standby (DC Switching Only)	2.0		10.0	V	1
	Inputs:					
	$\overline{\text{Tone Disable}}$, $\overline{\text{Single Tone Inhibit}}$					
V_{IH}	Input High (Logic 1)	.7 V+		V+	V	
V_{IL}	Input Low (Logic 0)	0.0		.3 V+	V	
	Columns (1-4)					
V_{CIH}	Input High (Column ON)	.7 V+		V+	V	
V_{CIL}	Input Low (Column OFF)	0.0		.1 V+	V	
	Row (1-4)					
V_{RIH}	Input High (Row OFF)	.9 V+		V+	V	
V_{RIL}	Input Low (Row ON)	0.0		.3 V+	V	
R_I	Input Resistance ($\overline{\text{TD}}$ & $\overline{\text{STI}}$ only)	20		100	kΩ	10
V_{OUT}	Tone Output Level, Pin 1	-10.0	-8.5	-7.0	dBm	2,11
PE_{HB}	Pre-Emphasis, Highband (Unfiltered)	1.0	2.0	3.0	dB	3,11
DIS	Output distortion measured in terms of out of band power relative to RMS sum of row and column fundamental power			-20	dB	4,11
t_{RISE}	Rise Time			5	ms	5
$I_{AKD_{ON}}$	Any Key Down Source Current to V+	500			μA	6
$I_{AKD_{OFF}}$	Any Key Down Off Leakage			10	μA	7
I_{OP}	Supply Current - Operating @ 3.5 V @ 10.0 V		1.0 5.0	2.0	mA mA	8
I_{SB}	Supply Current - Standby @ 10.0 V		1.0	200	μA	9
V_{NKD}	Tone Output - No Key Down			-80	dBm	
R_{OA}	Op Amp Output Resistor		10		kΩ	12
I_{OA}	Op Amp Output Current @ 3.0 V	250			μA	12

NOTES

1. Voltage at which mute output will respond to any key closure, chip disable = 0.
2. Single tone, low group. Any supply voltage between 3.4 V and 3.6 V. Output amplitude is linearly proportional to supply voltage. This condition valid for $-30°C < T_A < 60°C$. See test circuit.
3. High group output level relative to low group level. Valid for $-30°C < T_A < 60°C$.
4. Any supply voltage between 3.4 V and 10.0 V. See test circuit.
5. Time from a valid keystroke with no bounce to allow the output waveform to go from its minimum to 90% of the final magnitude of either frequency. Crystal parameters are defined to be Rs = 100 Ω, Lm = 96 mH, CM = 0.02 pF, and Ch = 5 pF. F = 3.579545 MHz. Any $-30°C < T_A < +60°C$.
6. AKD is open drain P-channel transistor. Minimum current defined is valid with V+ = 3.5 volts, V_{AKD} = 3.0 volts. AKD pulls to V+ when valid key is depressed.
7. V+ = 10 volts, V_{AKD} = 0 volts.
8. For any ambient temperature in the range -30°C to +60°C. Single key depressed only. Crystal as in Note 5. Measured at Pin 6. Outputs open circuited.
9. Standby condition is defined to be no keys activated, $\overline{TD}$ = logical 0, single tone inhibit = logical 1. Outputs and inputs open circuited.
10. 25°C.
11. R_{LOAD} (pin 18) = 620 Ω @ 3.4 V ≤ V+ ≤ 10 V. See test circuit.
12. Op Amp Output Resistor size is determined by the capacitance on Pin 1. The 10 kΩ resistor shown in test circuit is correct for typical filter circuit. If capacitance at this pin is too large, a smaller value or resistance will be required.

TEST CIRCUIT

Figure 12



V BIAS = .5 V WHEN V SUPPLY ≤ 4.0 V

V BIAS = 0 V WHEN V SUPPLY > 4.0 V

Integrated Tone Dialer

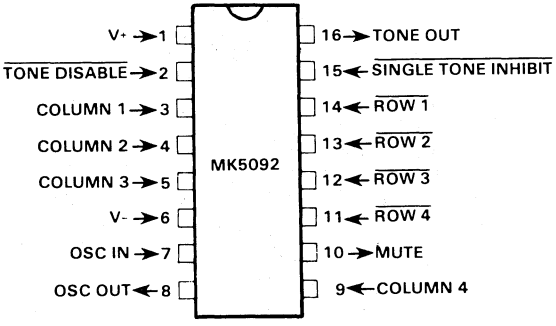
MK5092(N)

FEATURES

- Designed for use with hybrid network
- Internal regulation of tone amplitudes
- Tone frequencies within 0.65% for 12 standard frequencies
- Meets or exceeds U.S. Telephone Specifications for tone levels and distortion
- Internal loop compensation and pre-emphasis
- Uses inexpensive 3.579545 MHz television color-burst crystal for accurate tones
- Tone-disable capability
- Uses either calculator-type (Form A Contact) or 2-of-8 dual-contact keyboard
- Pin-selectable single-tone capability
- MUTE output for electronic switching
- Minimum external parts count

PIN CONNECTIONS

Figure 1



DESCRIPTION

The MK5092 is a monolithic integrated circuit fabricated using the complementary-symmetry MOS (CMOS) process. A member of the Tone II* family of integrated tone dialers, the MK5092 uses an inexpensive crystal reference to provide the eight standard signaling frequencies which are mixed to provide Dual-Tone-Multi-Frequency (DTMF) telephone dialing.

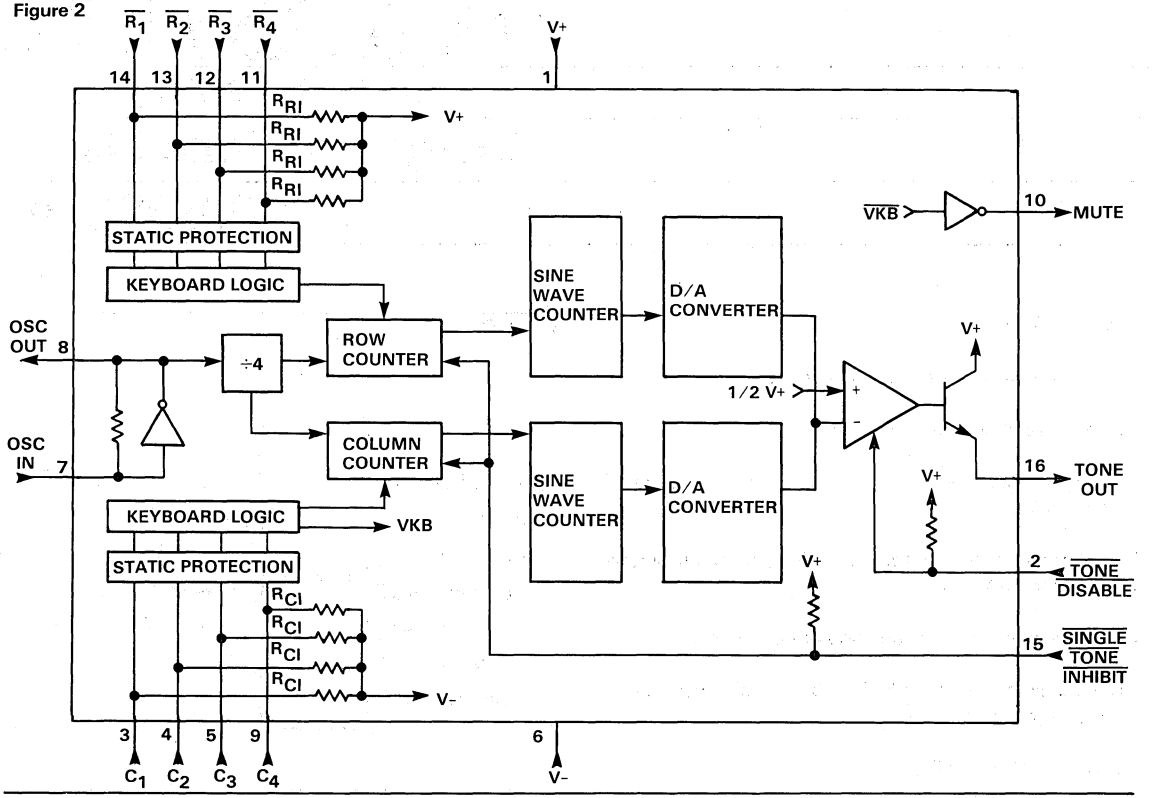
The MK5092 was designed for tone-dialer applications that require the following characteristics: wide range supply operation with loop-compensated tone regulation, single-contact keyboard capability, tone-disable capability, and a mute output that pulls to V– until a keyboard entry is detected and then pulls to V+.

Any valid keyboard entry to the Tone II* family of integrated tone dialers causes the selection of the proper divisor to obtain the required frequency from the internal 3.579545 MHz oscillator. Digital-to-analog conversion of the resultant frequency is done internally with a conventional R-2R ladder network. The tone output is a stairstep approximation of a sinusoid and requires little filtering for low-distortion applications.

*Trademark of Mostek Corp.

BLOCK DIAGRAM

Figure 2



FUNCTIONAL DESCRIPTION

(Refer to Figure 2 for Block Diagram)

V+, Pin 1

Pin 1 connects the positive supply to the MK5092.

$\overline{\text{TONE DISABLE}}$, Pin 2

$\overline{\text{TONE DISABLE}}$ disables the summing operational amplifiers and is used to inhibit tone generation to allow the keyboard to be used for functions other than DTMF signaling. The $\overline{\text{TONE DISABLE}}$ input has an internal pull-up resistor and, when left unconnected or connected to V+, allows normal generation of tones. When connected to V–, $\overline{\text{TONE DISABLE}}$ inhibits the tone output. MUTE and other functions operate normally, regardless of the status of Pin 2.

$\overline{\text{ROW}}$ AND COLUMN INPUTS, Pins 3, 4, 5, 9, 11, 12, 13, 14

The MK5092 features inputs compatible with the standard 2-of-8 keyboard, the inexpensive single-contact (Form A) keyboard, and electronic inputs.

Figure 4 shows how to connect to the two keyboard types and Figure 5 shows waveforms for electronic input. The inputs are static, i.e. there is no noise generation as occurs with scanned or dynamic inputs.

The internal structure of the MK5092 inputs is shown in Figures 2 and 3. R_{RI} and R_{CI} pull in opposite directions and hold their associated input sensing circuit turned off. When one or more row or column inputs are tied together, however, the input sensing circuits sense the "½ level" and deliver a logic signal to the internal circuitry of the MK5092 and cause the proper tone or tones to be generated.

When operating with a keyboard, normal operation is for dual-tone generation when any single button is pushed and single-tone operation when more than one button in the same row or column is pushed. Activation of diagonal buttons will result in no tones being generated.

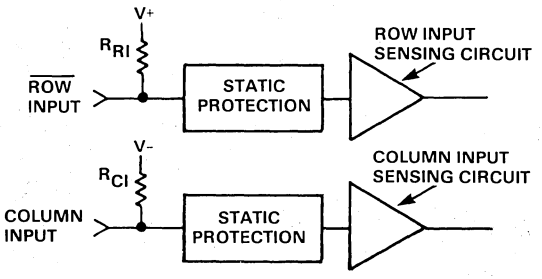
When the inputs to the MK5092 are electronically activated, per Figure 5, an input to a single row and a single column will result in that dual-tone digit being generated. Input to multiple columns only will result in no tone being generated.

Activation of a single row is not sensed by the internal

circuitry of the MK5092. If a single-row is desired, two columns must be activated along with the desired row.

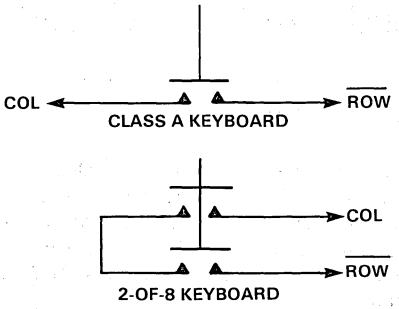
ROW AND COLUMN INPUT CIRCUITRY

Figure 3



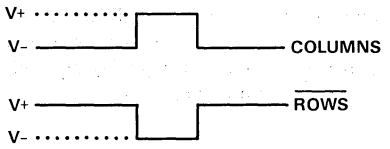
KEYBOARD CONFIGURATION

Figure 4



ELECTRONIC INPUT

Figure 5



V-, Pin 6

V- is the return for the MK5092 supply. All MK5092 voltages and signals are referenced to V-.

OSC IN, Pin 7; OSC OUT, Pin 8

The MK5092 contains an on-board inverter with sufficient loop gain to provide oscillation using a crystal. The inverter input is OSC IN and the output is OSC OUT. When using a 3.579545 MHz crystal, the MK5092 will produce the frequencies in Table 1. Crystal frequency deviation, usually less than ±0.02%, will be reflected in the tone output frequency.

MUTE, Pin 10

The MUTE output is used for electronic control of receiver and/or transmitter switching. The MUTE output is connected to V- when no keyboard input is present and switches to V+ upon recognition of a keyboard input. MUTE switches regardless of the condition of $\overline{\text{SINGLE TONE INHIBIT}}$ and $\overline{\text{TONE DISABLE}}$ inputs.

$\overline{\text{SINGLE TONE INHIBIT}}$, Pin 15

The $\overline{\text{SINGLE TONE INHIBIT}}$ input is used to control the generation of single tones. It has an internal pull-up resistor to V+ and when not connected or connected to V+, either single or dual tones may be produced as described in the paragraphs on row and column inputs. With $\overline{\text{SINGLE TONE INHIBIT}}$ connected to V-, any input situations that would normally produce a single tone will produce no tone.

TONE OUT, Pin 16

An internal operational amplifier mixes the row and column tones and regulates the output level. The output of this amplifier is connected to the base of a npn transistor. The collector of this internal transistor is connected to V+ and the emitter is brought out to TONE OUT.

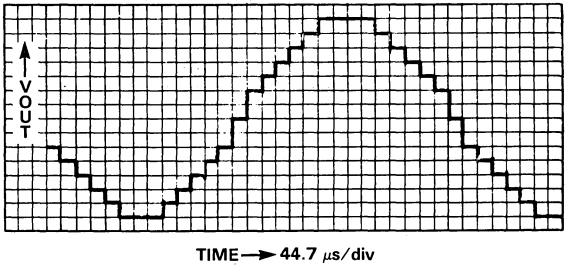
OUTPUT FREQUENCY DEVIATION

Table 1

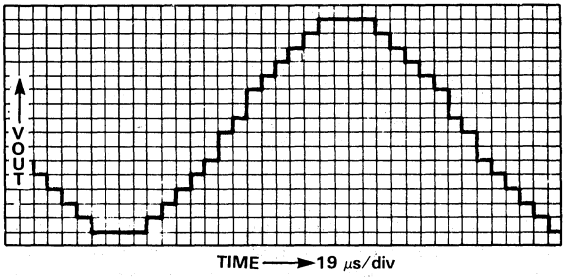
	Standard DTMF (Hz)	Tone Output Frequency Using 3.579545 MHz Crystal	% Deviation From Standard	
ROW f_1	697	701.3	+0.62	
ROW f_2	770	771.4	+0.19	LOW GROUP
ROW f_3	852	857.2	+0.61	LOW GROUP
ROW f_4	941	935.1	-0.63	
COL f_5	1209	1215.9	+0.57	
COL f_6	1336	1331.7	-0.32	HIGH GROUP
COL f_7	1477	1471.9	-0.35	HIGH GROUP
COL f_8	1633	1645.0	+0.73	

ROW 2 TONE OUTPUT

Figure 6



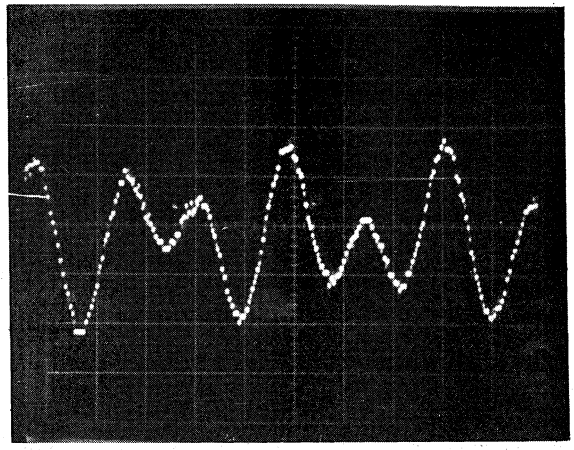
COLUMN 4 TONE OUTPUT
Figure 7



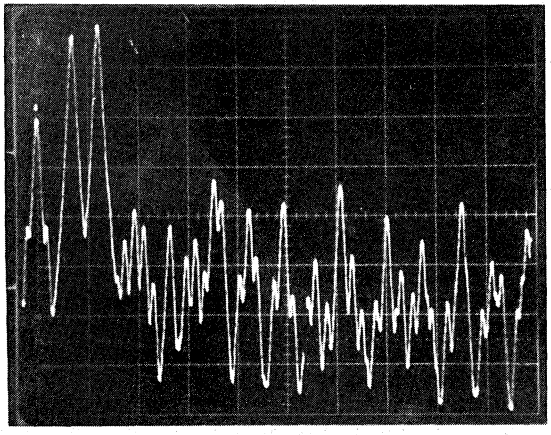
OUTPUT WAVEFORM

The row and column output waveforms, shown in Figures 6 and 7, are digitally synthesized sinusoids produced by internal dividers and digital-to-analog converters. Distortion measurement, discussed in the next section, of these unfiltered output waveforms shows a typical total harmonic distortion of 7% or less. Spectral analysis of the dual-tone waveforms shows that all harmonic and intermodulation distortion components are typically at least -30 dB when referenced to the strongest fundamental. Figures 8 and 9 show a dual-tone waveform and its spectral plot.

TYPICAL DUAL-TONE WAVEFORM (ROW 1, COL. 1)
Figure 8



SPECTRAL ANALYSIS OF WAVEFORM IN FIGURE 8 (Vert-10 dB/div, Horizontal-1 kHz/div)
Figure 9



DISTORTION MEASUREMENTS

A commonly used method of dual-tone distortion measurement is the comparison of total power in the unwanted components (i.e. intermodulation and harmonic components) with the total power in the two fundamentals. For the MK5092 dual-tone waveforms, THD is -20 dB maximum.

A simpler measurement may be made directly from the screen of a spectrum analyzer by relating any component to one of the fundamentals. The MK5092 dual-tone spectrum shows all individual harmonic and intermodulation distortion components are typically at least -30 dB with respect to the column tone.

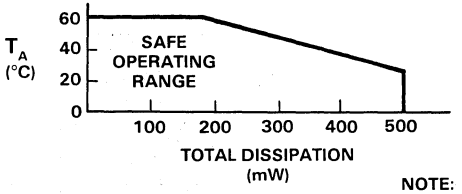
ABSOLUTE MAXIMUM RATINGS*

See Note 1

Supply Voltage V+ ..... +10.5 Volts
Voltage on any Pin Relative to V+ ..... +0.3 Volts
Voltage on any Pin Relative to V– ..... –0.3 Volts
Operating Temperature ..... 0°C to +60°C
Storage Temperature ..... –35°C to +85°C
Maximum Circuit Power Dissipation ..... 500 mW @ 25°C (See Derating Curve)

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

POWER DISSIPATION DERATING CURVE



NOTE: Derate 9 mW/°C from 500 mW @ 25°C.

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS

($0°C \leq T_A \leq 60°C$)

See Note 1

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V+	Supply Voltage					
	Operating (Generating tones) (Telephone loop supply)	3.5		10.0	V	13
	Operating (Generating tones) (Fixed voltage supply)	3.8		10.0	V	13
	Standby (dc switching only)	3.0		10.0	V	2,13
	$\overline{\text{CHIP DISABLE}}$, $\overline{\text{SINGLE TONE INHIBIT}}$					
V_{IH}	Input High (Logic 1)	70% of V+		V+	V	
V_{IL}	Input Low (Logic 0)	0.0		30% of V+	V	
	Columns (1-4)					
V_{IH}	Input High (on)	70% of V+		V+	V	
V_{IL}	Input Low (off)	0.0		10% of V+	V	
	Rows (1-4)					
V_{IH}	Input High (off)	90% of V+		V+	V	
V_{IL}	Input Low (on)	0.0		30% of V+	V	
	Pull-Up/Down Resistors					
R_{RI}	Row Inputs		15		kΩ	7,12
R_{CI}	Column Inputs		15		kΩ	7,12
	$\overline{\text{TONE DISABLE}}$	20	60	125	kΩ	7,13
	$\overline{\text{SINGLE TONE INHIBIT}}$	20	60	125	kΩ	7,13

AC CHARACTERISTICS

($0°C \leq T_A \leq 60°C$)

See Note 1

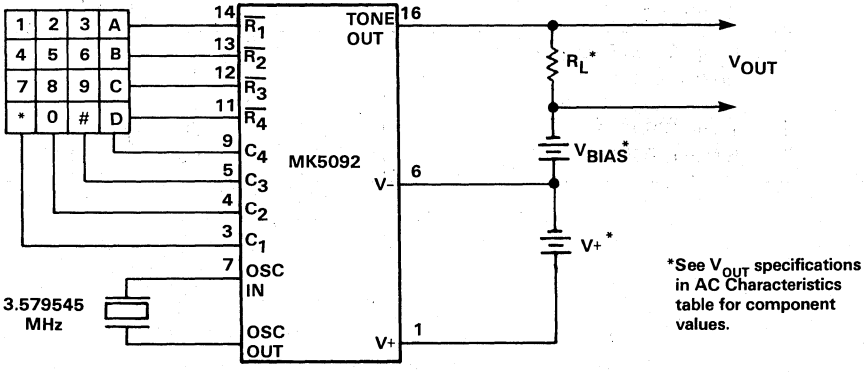
SYM	PARAMETER		MIN	TYP	MAX	UNITS	NOTES
	Tone Output (R_L = 600 Ω, V+ = 3.8 V, V_{BIAS} = 1.5 V)						
V_{OUT}	Row Tone		422		531	mV_{rms}	7,8,9
V_{OUT}	Column Tone		528		664	mV_{rms}	7,8,9
	Tone Output (R_L = 320 Ω, V+ = 10.0 V, V_{BIAS} = 3.5 V)						
V_{OUT}	Row Tone		441		555	mV_{rms}	7,8,9
V_{OUT}	Column Tone		551		693	mV_{rms}	7,8,9
	MUTE current						
I_M	Source	V+ = 10.0 V	0.50			mA	4,13
		V+ = 3.0 V	0.20			mA	5,13
I_M	Sink	V+ = 10.0 V	-0.50			mA	3
		V+ = 3.0 V	-0.20			mA	3
	Supply Current (Outputs unloaded)						
I_{SO}	Operating	V+ = 3.5 V		1.0	2.0	mA	7,13
I_{SO}	Operating	V+ = 10.0 V		5.0	10.0	mA	13
I_{SS}	Standby	V+ = 10.0 V		0.5	200	μA	6,7
PE_{HB}	Pre-Emphasis, High Band		1.0	2.0	3.0	dB	
DIS	Output Distortion, total out of band power Relative to rms sum of row and column fundamental power				-20	dB	10
t_{RISE}	Rise Time, Tone Output				5	ms	11
V_{NKD}	Tone Output (no key activated)				-80	dBm	

NOTES

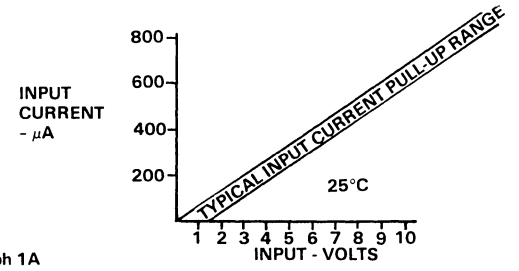
1. All voltages referenced to V–.
2. Voltage at which MUTE will respond to key input, $\overline{\text{TONE DISABLE}}$ = V–.
3. V_{OUT} (MUTE) = 0.5 V
4. V_{OUT} (MUTE) = 9.5 V
5. V_{OUT} (MUTE) = 2.5 V
6. Current into Pin 6 with no key input.
7. At T_A = 25°C.
8. True rms reading.
9. See test circuit, Figure 10.
10. Any row plus any column, V+ ≥ 5.0 V.
11. Time from a valid keystroke with no bounce to allow the waveform to go from min. to 90% of the final magnitude of either frequency. Crystal parameters defined as R_S = 100 Ω, L = 96 mH, C_M = 0.02 pF, and C_H = 5 pF. Any V+ between 3.8 and 10.0 V. F = 3.579545 MHz.
12. See Graphs 1A and 1B.
13. With valid keyboard input.

TEST CIRCUIT

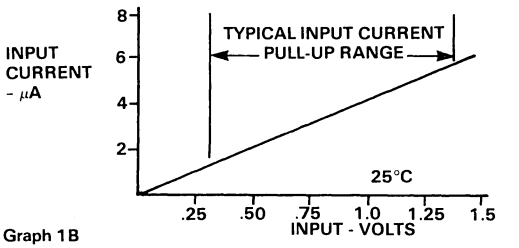
Figure 10



Graph 1A & 1B - INPUT CURRENT VS. INPUT VOLTAGE



Graph 1A



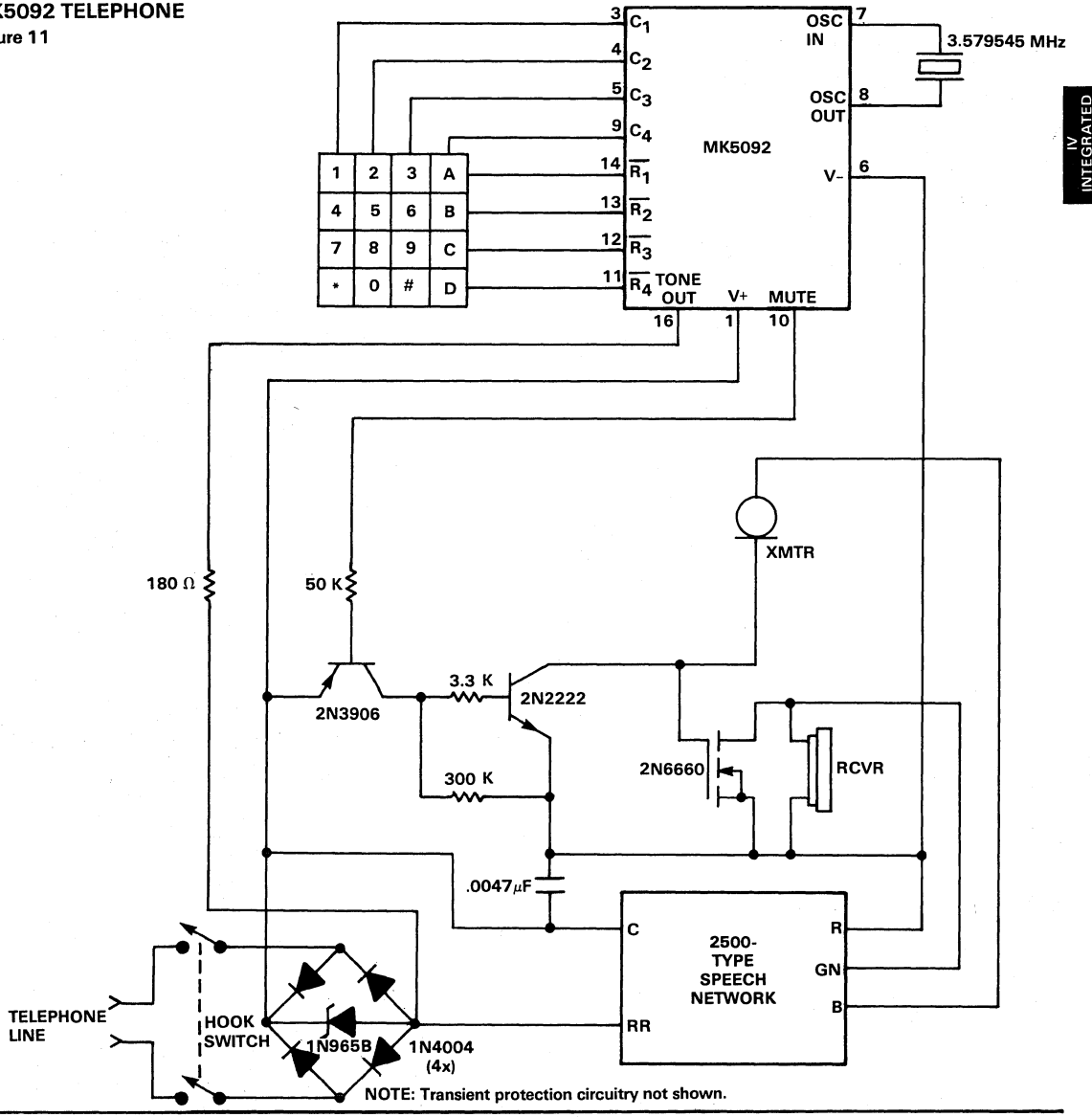
Graph 1B

APPLICATION

Figure 11 shows the MK5092 used with a 2500-Type Speech Network. The tone levels and distortion measurements of this application meet U.S. Telephone Specifications.

MK5092 TELEPHONE

Figure 11



NOTE: Transient protection circuitry not shown.

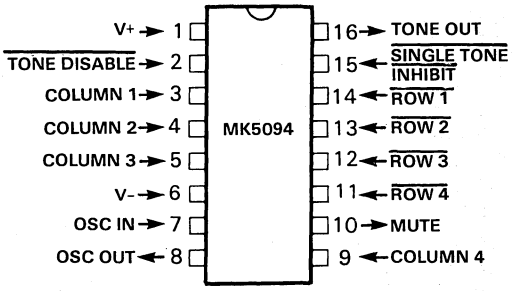
Integrated Tone Dialer
MK5094(N)

FEATURES

- Designed for use with hybrid network
- Internal regulation of tone amplitudes
- Tone frequencies within 0.65% for 12 standard frequencies
- Internal loop compensation and pre-emphasis
- Uses inexpensive 3.579545 MHz television color-burst crystal for accurate tones
- Tone-disable capability
- Uses either calculator-type (Form A Contact) or 2-of-8 dual-contact keyboard
- Pin-selectable single-tone capability
- MUTE output for electronic switching
- Minimum external parts count

PIN CONNECTIONS

Figure 1



DESCRIPTION

The MK5094 is a monolithic integrated circuit fabricated using the complementary-symmetry MOS (CMOS) process. A member of the Tone II* family of integrated tone dialers, the MK5094 uses an inexpensive crystal reference to provide the eight standard signaling frequencies which are mixed to provide Dual-Tone-Multi-Frequency (DTMF) telephone dialing.

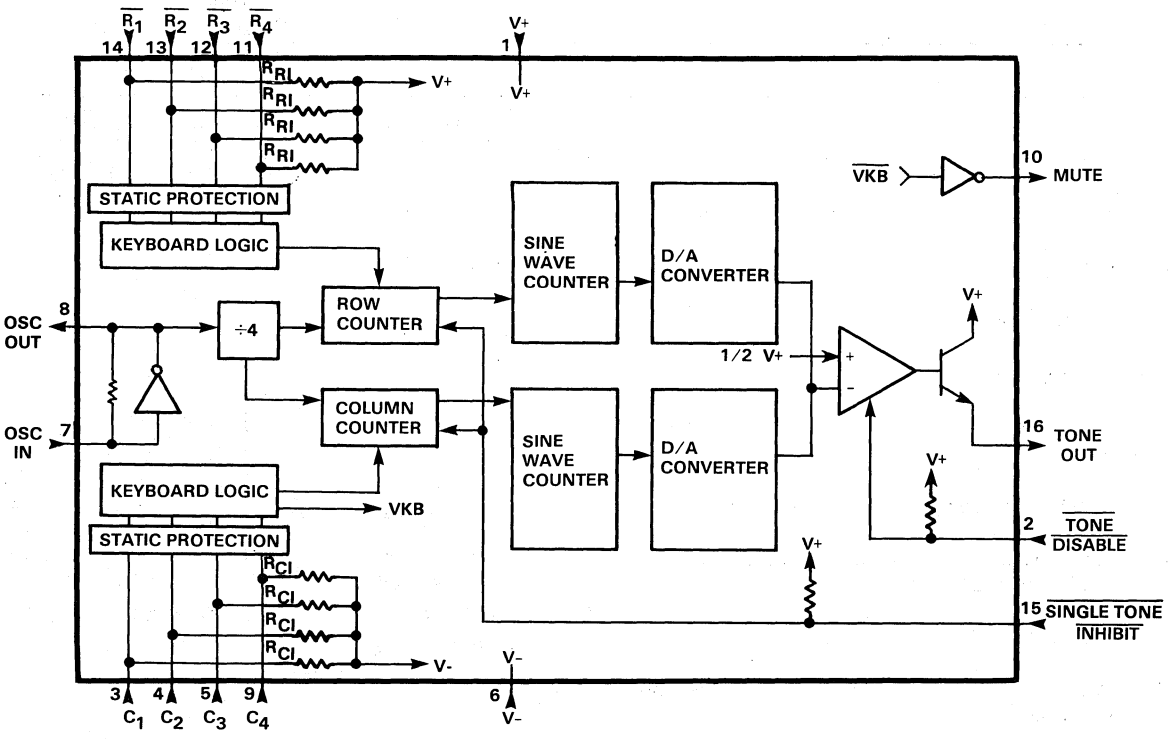
The MK5094 was designed for tone-dialer applications that require the following characteristics: wide range supply operation with loop-compensated tone regulation, single-contact keyboard capability, tone-disable capability, and a mute output that pulls to V- until a keyboard entry is detected and then pulls to V+.

Any valid keyboard entry to the Tone II* family of integrated tone dialers causes the selection of the proper divisor to obtain the required frequency from the internal 3.579545 MHz oscillator. Digital-to-analog conversion of the resultant frequency is done internally with a conventional R-2R ladder network. The tone output is a stairstep approximation of a sinusoid and requires little filtering for low-distortion applications.

*Trademark of Mostek Corp.

BLOCK DIAGRAM

Figure 2



FUNCTIONAL DESCRIPTION

(Refer to Figure 2 for Block Diagram)

V+, Pin 1

Pin 1 connects the positive supply to the MK5094.

$\overline{\text{TONE DISABLE}}$, Pin 2

$\overline{\text{TONE DISABLE}}$ disables the summing operational amplifier and is used to inhibit tone generation to allow the keyboard to be used for functions other than DTMF signaling. The $\overline{\text{TONE DISABLE}}$ input has an internal pull-up resistor and, when left unconnected or connected to V+, allows normal generation of tones. When connected to V–, $\overline{\text{TONE DISABLE}}$ inhibits the tone output. MUTE and other functions operate normally, regardless of the status of Pin 2.

$\overline{\text{ROW}}$ AND COLUMN INPUTS, Pins 3, 4, 5, 9, 11, 12, 13, 14

The MK5094 features inputs compatible with the standard 2-of-8 keyboard, the inexpensive single-contact (Form A) keyboard, and electronic inputs.

Figure 4 shows how to connect to the two keyboard types and Figure 5 shows waveforms for electronic input. The inputs are static, i.e. there is no noise generation as occurs with scanned or dynamic inputs.

The internal structure of the MK5094 inputs is shown in Figures 2 and 3. R_{RI} and R_{CI} pull in opposite directions and hold their associated input sensing circuit turned off. When one or more row or column inputs are tied together, however, the input sensing circuits sense the "½ level" and deliver a logic signal to the internal circuitry of the MK5094 and cause the proper tone or tones to be generated.

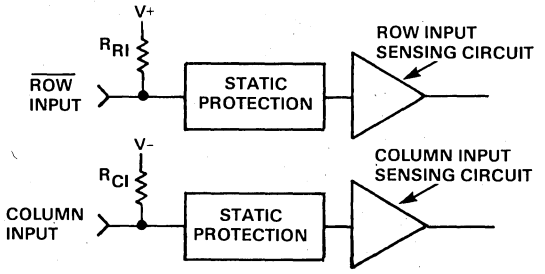
When operating with a keyboard, normal operation is for dual-tone generation when any single button is pushed and single-tone operation when more than one button in the same row or column is pushed. Activation of diagonal buttons will result in no tones being generated.

When the inputs to the MK5094 are electronically activated, per Figure 5, an input to a single row and a single column will result in that dual-tone digit being generated. Input to multiple columns only will result in no tone being generated.

Activation of a single row is not sensed by the internal circuitry of the MK5094. If a single row is desired, two columns must be activated along with the desired row.

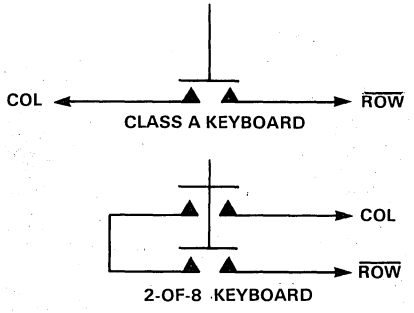
ROW AND COLUMN INPUT CIRCUITRY

Figure 3



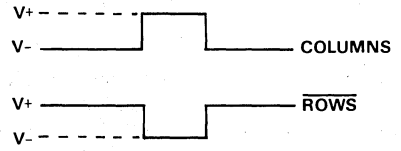
KEYBOARD CONFIGURATION

Figure 4



ELECTRONIC INPUT

Figure 5



V-, Pin 6

V- is the return for the MK5094 supply. All MK5094 voltages and signals are referenced to V-.

OSC IN, Pin 7; OSC OUT, Pin 8

The MK5094 contains an on-board inverter with sufficient loop gain to provide oscillation using a crystal. The inverter input is OSC IN and the output is OSC OUT. When using a 3.579545 MHz crystal, the MK5094 will produce the frequencies in Table 1. Crystal frequency deviation, usually less than ±0.02%, will be reflected in the tone output frequency.

MUTE, Pin 10

The MUTE output is used for electronic control of receiver and/or transmitter switching. The MUTE output is connected to V- when no keyboard input is present and switches to V+ upon recognition of a keyboard input. MUTE switches regardless of the condition of $\overline{\text{SINGLE TONE INHIBIT}}$ and $\overline{\text{TONE DISABLE}}$ inputs.

$\overline{\text{SINGLE TONE INHIBIT}}$, Pin 15

The $\overline{\text{SINGLE TONE INHIBIT}}$ input is used to control the generation of single tones. It has an internal pull-up resistor to V+ and when not connected or connected to V+, either single or dual tones may be produced as described in the paragraphs on row and column inputs. With $\overline{\text{SINGLE TONE INHIBIT}}$ connected to V-, any input situation that would normally produce a single tone will produce no tone.

TONE OUT, Pin 16

An internal operational amplifier mixes the row and column tones and regulates the output level. The output of this amplifier is connected to the base of a npn transistor. The collector of this internal transistor is connected to V+ and the emitter is brought out to TONE OUT.

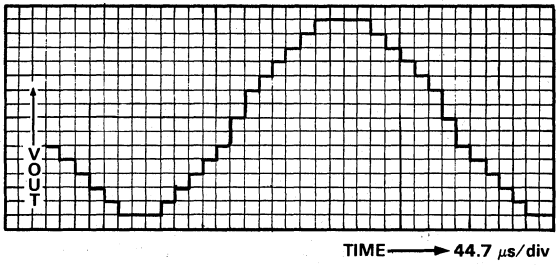
OUTPUT FREQUENCY DEVIATION

Table 1

		Standard DTMF (Hz)	Tone Output Frequency Using 3.579545 MHz Crystal	% Deviation From Standard	
Row	f_1	697	701.3	+0.62	
	f_2	770	771.4	+0.19	Low
	f_3	852	857.2	+0.61	Group
	f_4	941	935.1	-0.63	
Col	f_5	1209	1215.9	+0.57	
	f_6	1336	1331.7	-0.32	High
	f_7	1477	1471.9	-0.35	Group
	f_8	1633	1645.0	+0.73	

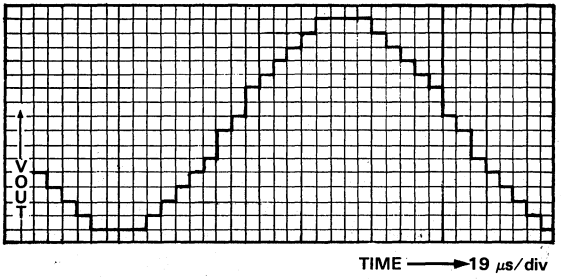
ROW 2 TONE OUTPUT

Figure 6



COLUMN 4 TONE OUTPUT

Figure 7



OUTPUT WAVEFORM

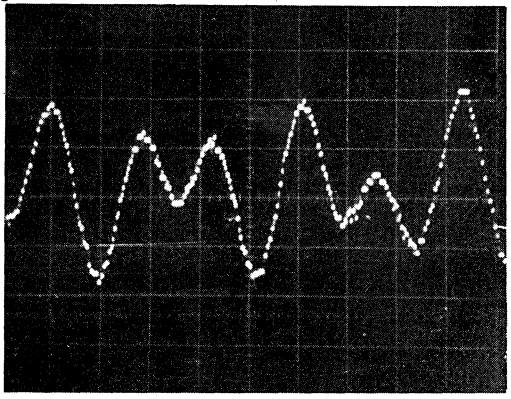
The row and column output waveforms, shown in Figures 6 and 7, are digitally synthesized sinusoids produced by internal dividers and digital-to-analog converters. Distortion measurement, discussed in the next section, of these unfiltered output waveforms shows a typical total harmonic distortion of 7% or less. Spectral analysis of the dual-tone waveforms shows that all harmonic and intermodulation distortion components are typically at least -30 dB when referenced to the strongest fundamental. Figures 8 and 9 show a dual-tone waveform and its spectral plot.

DISTORTION MEASUREMENTS

A commonly used method of dual-tone distortion measurement is the comparison of total power in the unwanted components (i.e. intermodulation and harmonic components) with the total power in the two fundamentals.

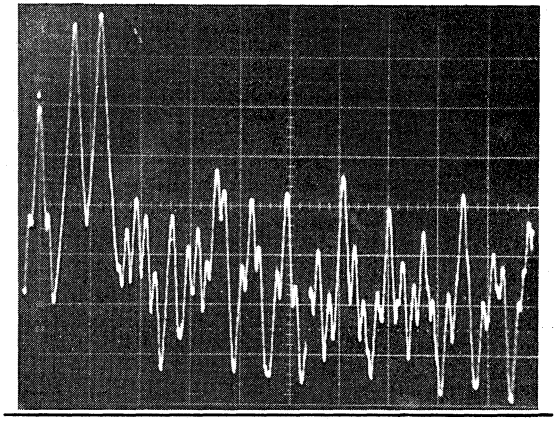
TYPICAL DUAL-TONE WAVEFORM (ROW 1, COL. 1)

Figure 8



SPECTRAL ANALYSIS OF WAVEFORM IN FIG. 8 (Vert-10 dB/div, Horizontal-1 kHz/div)

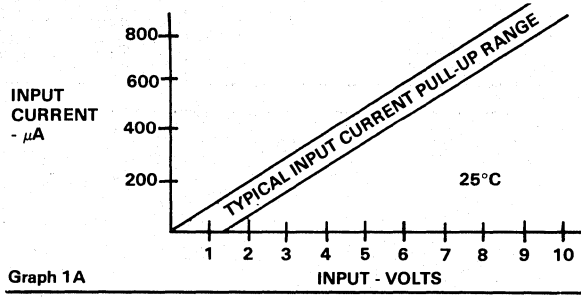
Figure 9



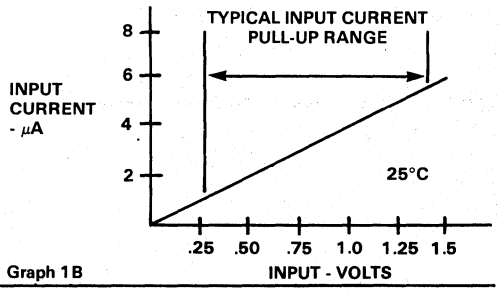
For the MK5094 dual-tone waveforms, THD is –20 dB maximum.

A simpler measurement may be made directly from the screen of a spectrum analyzer by relating any component to one of the fundamentals. The MK5094 dual-tone spectrum shows all individual harmonic and intermodulation distortion components are typically at least -30 dB with respect to the column tone.

Graph 1A & 1B INPUT CURRENT VS. INPUT VOLTAGE



Graph 1A



Graph 1B

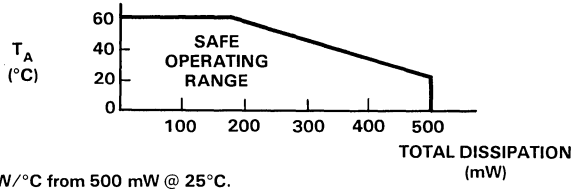
ABSOLUTE MAXIMUM RATINGS*

See Note 1

Supply Voltage V+ ..... +10.5 Volts
Voltage on any Pin Relative to V+ ..... +0.3 Volts
Voltage on any Pin Relative to V– ..... –0.3 Volts
Operating Temperature ..... 0°C to +60°C
Storage Temperature ..... –35°C to +85°C
Maximum Circuit Power Dissipation ..... 500 mW @ 25°C (See Derating Curve)

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

POWER DISSIPATION DERATING CURVE



NOTE: Derate 9 mW/°C from 500 mW @ 25°C.

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS

($0°C \leq T_A \leq 60°C$)

See Note 1

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V+	Supply Voltage					
	Operating (Generating tones) (Telephone loop supply)	3.5		10.0	V	13
	Operating (Generating tones) (Fixed voltage supply)	3.8		10.0	V	13
	Standby (dc switching only)	3.0		10.0	V	2,13
	Tone Disable, Single Tone Inhibit					
V_{IH}	Input High (Logic 1)	70% of V+		V+	V	
V_{IL}	Input Low (Logic 0)	0.0		30% of V+	V	
	Columns (1-4)					
V_{IH}	Input High (on)	70% of V+		V+	V	
V_{IL}	Input Low (off)	0.0		10% of V+	V	
	Rows (1-4)					
V_{IH}	Input High (off)	90% of V+		V+	V	
V_{IL}	Input Low (on)	0.0		30% of V+	V	
	Pull-Up/Down Resistors					
R_{RI}	Row Inputs		15		kΩ	7,12
R_{CI}	Column Inputs		15		kΩ	7,12
	$\overline{\text{TONE DISABLE}}$	20	60	125	kΩ	7,13
	$\overline{\text{SINGLE TONE INHIBIT}}$	20	60	125	kΩ	7,13

AC CHARACTERISTICS
($0°C \leq T_A \leq 60°C$)

See Note 1

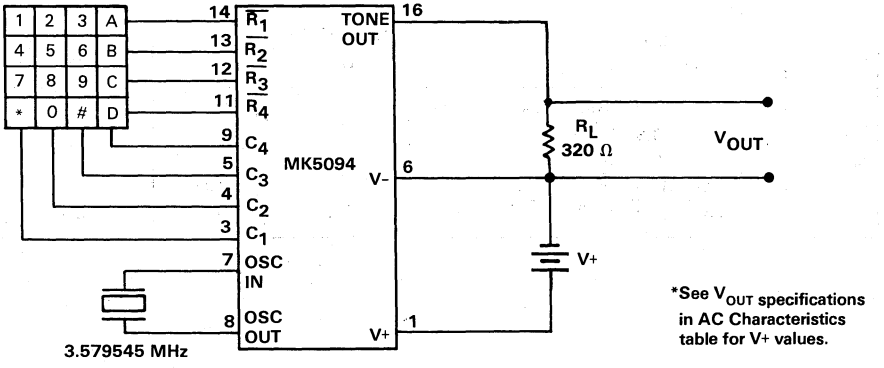
SYM	PARAMETER		MIN	TYP	MAX	UNITS	NOTES
	Tone Output (R_L = 320 Ω, V+ = 3.8 V)						
V_{OUT}	Row Tone		360		453	mV_{rms}	7,8,9
V_{OUT}	Column Tone		452		569	mV_{rms}	7,8,9
	Tone Output (R_L = 320 Ω, V+ = 10.0 V)						
V_{OUT}	Row Tone		387		487	mV_{rms}	7,8,9
V_{OUT}	Column Tone		486		612	mV_{rms}	7,8,9
	MUTE current						
I_M	Source	V+ = 10.0 V	0.50			mA	4,13
		V+ = 3.0 V	0.20			mA	5,13
I_M	Sink	V+ = 10.0 V	–0.50			mA	3
		V+ = 3.0 V	–0.20			mA	3
	Supply Current (Outputs unloaded)						
I_{SO}	Operating	V+ = 3.5 V		1.0	2.0	mA	13,7
I_{SO}	Operating	V+ = 10.0 V		5.0	15	mA	13
I_{SS}	Standby	V+ = 10.0 V		0.5	200	μA	6, 7
PE_{HB}	Pre-Emphasis, High Band		1.0	2.0	3.0	dB	
DIS	Output Distortion, total out of band power Relative to rms sum of row and column Fundamental Power				–20	dB	10
t_{RISE}	Rise Time, Tone Output				5	ms	11
V_{NKD}	Tone Output (no key activated)				–80	dBm	

NOTES

1. All voltages referenced to V–.
2. Voltage at which MUTE will respond to key input, $\overline{\text{TONE DISABLE}}$ = V–.
3. V_{OUT} (MUTE) = 0.5 V
4. V_{OUT} (MUTE) = 9.5 V
5. V_{OUT} (MUTE) = 2.5 V
6. Current out of Pin 6 with no key input.
7. At T_A = 25°C.
8. True rms reading.
9. See test circuit, Figure 10.
10. Any row plus any column, V+ ≥ 5.0 V.
11. Time from a valid keystroke with no bounce to allow the waveform to go from min. to 90% of the final magnitude of either frequency. Crystal parameters defined as R_S = 100 Ω, L = 96 mH, C_M = 0.02 pF, and C_H = 5 pF. Any V+ between 3.8 and 10.0 V. F = 3.579545 MHz.
12. See Graphs 1A and 1B.
13. With valid keyboard input.

TEST CIRCUIT

Figure 10

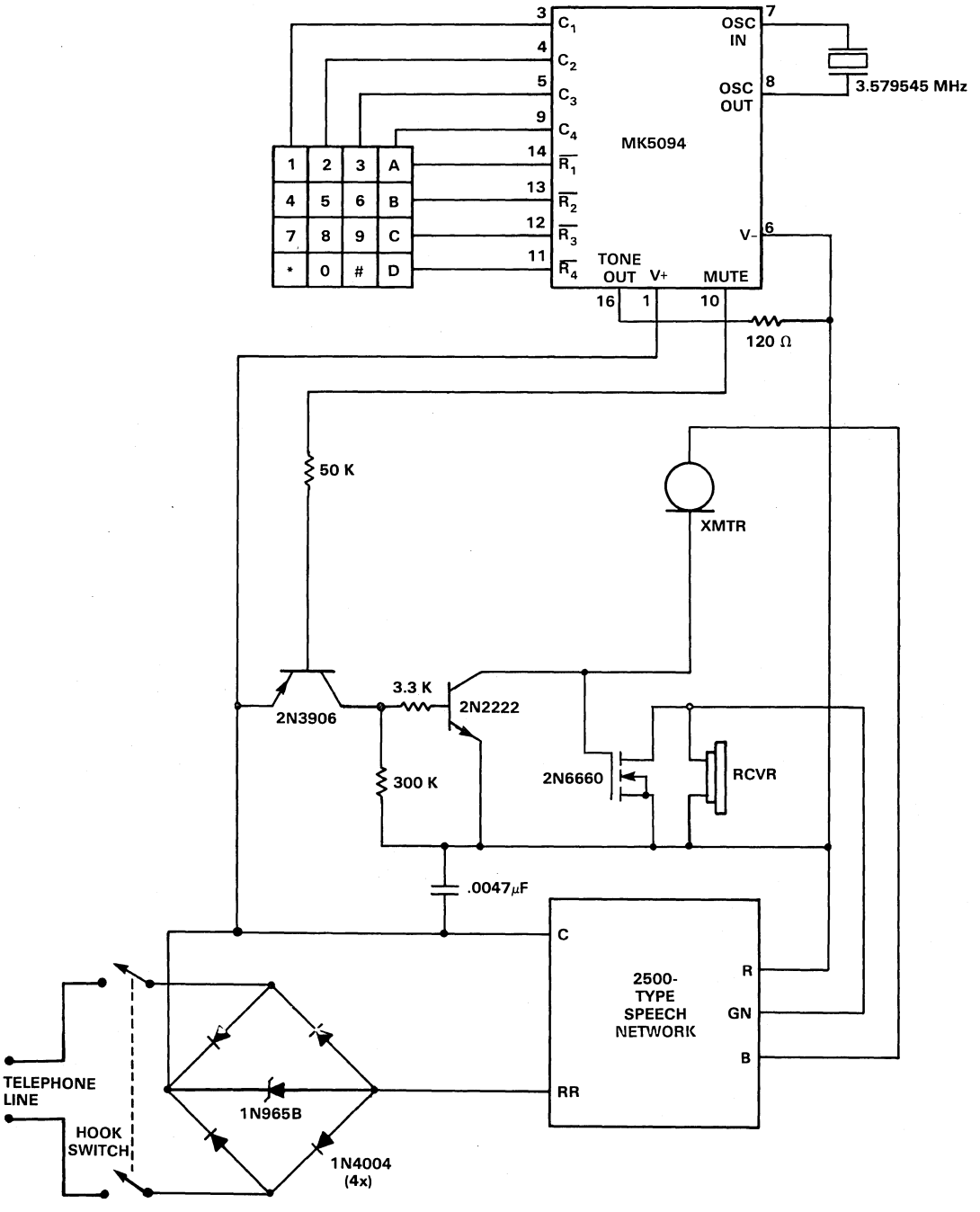


APPLICATION

Figure 11 shows the MK5094 used with a 2500-Type Speech Network.

MK5094 TELEPHONE

Figure 11



NOTE: Transient protection circuitry not shown.

MOSTEK®

TELECOMMUNICATIONS

Integrated Tone Dialer

MK5380(N/P/J)

FEATURES

- Low standby power
- Minimum external parts count
- Uses inexpensive 3.579545 MHz television color-burst crystal to provide high-accuracy tones
- Improved loop compensation
- Distortion lower than industry standards
- Low voltage operation - 2.5 volts
- Uses low-cost calculator-type keyboard (Form A contact) or standard 2-of-8 keyboard
- Auxiliary switching functions on chip
- Multiple key entry pin-selectable to either single tone or no tone

DESCRIPTION

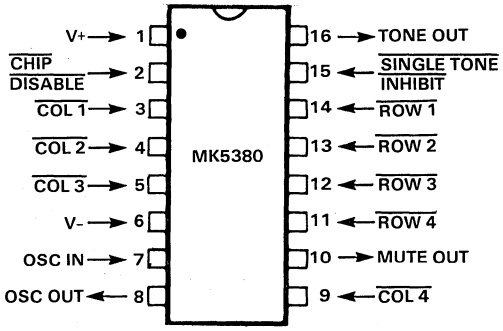
The MK5380 is a monolithic integrated circuit fabricated using Mostek's Silicon Gate CMOS process. A member of the Tone III* family of integrated tone dialers, the MK5380 uses an inexpensive crystal reference to provide eight different audio sinusoidal frequencies, which are mixed to provide tones suitable for Dual-Tone-Multi-Frequency (DTMF) telephone dialing.

The MK5380 was designed specifically for integrated tone-dialer applications that require the following: wide-supply operation with regulated output, scanned keyboard inputs, auxiliary switching functions, and a $\overline{\text{Chip Disable}}$ input.

Keyboard entries to the MK5380 integrated tone dialer cause the selection of the proper divide ratio to obtain the required two audio frequencies from the 3.579545 MHz reference oscillator.

PIN CONNECTIONS

Figure 1



D-to-A conversion for synthesis of the tones is accomplished on chip by a sinusoidally tapped resistor tree.

Pin connections are shown in Figure 1 and a block diagram is shown in Figure 2.

FUNCTIONAL DESCRIPTION

V+, Pin 1

Pin 1 is the positive supply pin. The voltage on Pin 1 should be between 2.5 and 10.0 volts, measured relative to V- (Pin 6).

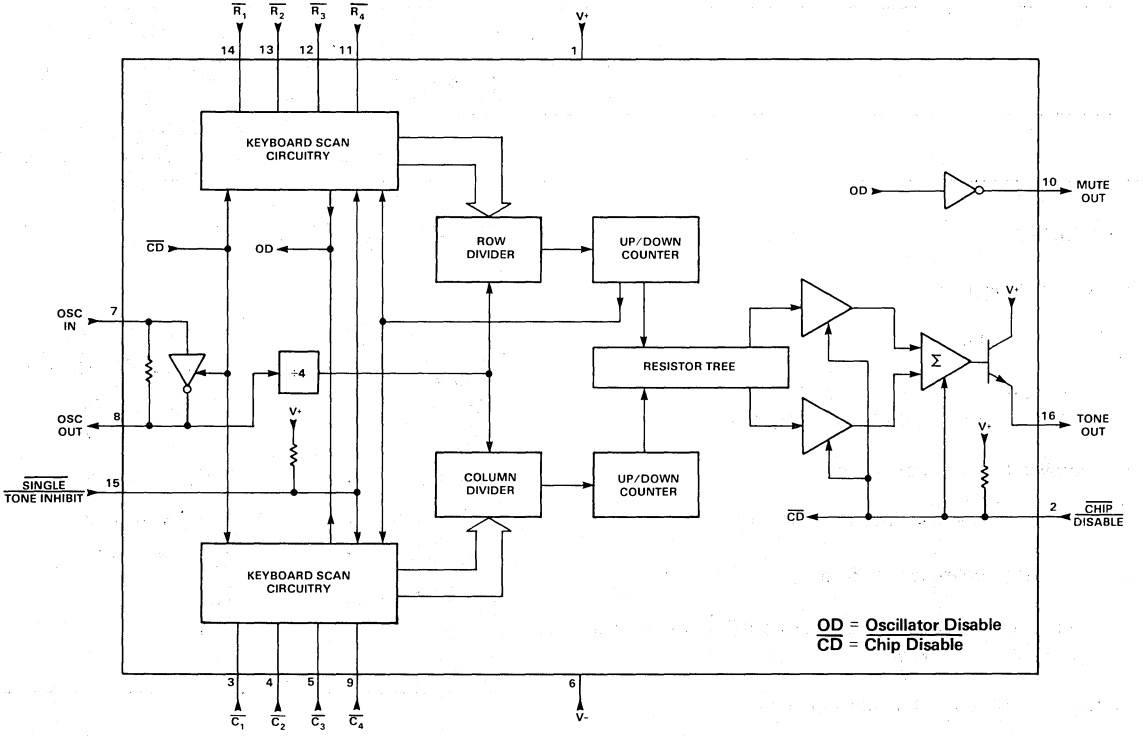
$\overline{\text{CHIP DISABLE}}$, Pin 2

When the $\overline{\text{Chip Disable}}$ input is connected to the V- supply, tone generation will be inhibited, the keyboard inputs will go to a high impedance state, and the amplifiers and oscillator will be powered down. The $\overline{\text{Chip Disable}}$ input has a pull-up resistor to the V+ supply and when floating or tied to V+, the MK5380 will operate normally.

*Trademark of Mostek Corporation

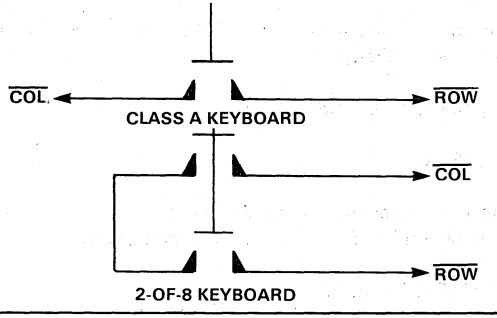
MK5380 BLOCK DIAGRAM

Figure 2



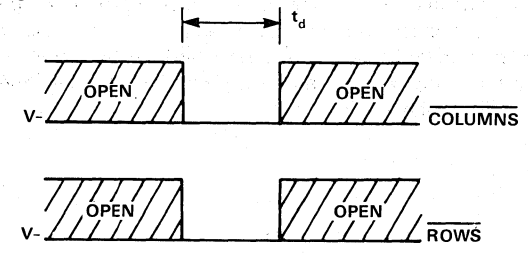
KEYBOARD CONFIGURATION

Figure 3



ELECTRONIC INPUT

Figure 4



NOTE: t_d is minimum tone duration minus oscillator start up time (t_{RISE})

DESCRIPTION (Continued)

ROW-COL INPUTS, Pins 3, 4, 5, 9, 11, 12, 13, 14

The MK5380 features inputs compatible with the standard 2-of-8 keyboard, the inexpensive single-contact (Form A) keyboard, and electronic input. Figure 3 shows how to connect to the two keyboard types and Figure 4 shows waveforms for electronic input.

The internal structure of the MK5380 Row and Column inputs is shown in Figure 5. These inputs are designed to sense a connection between Row and Column, or an electronic input as shown in Figure 4. Table 1 is a functional truth table for these inputs. Note that at least one Row and one Column must be active to generate a valid output.

When operating with a keyboard, normal operation is for dual-tone generation when any single button is pushed, and single-tone operation when more than one button in the same row or column is pushed. Activation of two or more diagonal buttons will result in no tones being generated.

V-, Pin 6

Pin 6 is the power supply return pin and it is the measurement reference for V+ (Pin 1).

FUNCTIONAL TRUTH TABLE

Table 1

ACTIVE LOW INPUTS		
$\overline{\text{ROW}}$	$\overline{\text{COLUMN}}$	OUTPUT
One	One	Dual Tone
Two or More	One	Column Tone
One	Two or More	Row Tone
Two or More	Two or More	No Tone

NOTE: $\overline{\text{STI}}$ is floating or tied to V+.
$\overline{\text{CD}}$ is floating or tied to V+.

OSC IN, Pin 7; OSC OUT, Pin 8

The MK5380 contains an on-board inverter with sufficient loop gain to provide oscillation when working with a low-cost television color-burst crystal. The inverter's input is Osc In (Pin 7) and output is Osc Out (Pin 8). The circuit is designed to work with a crystal cut to 3.579545 MHz to give the frequencies in Table 2. The oscillator is disabled whenever a keyboard input is not sensed.

Any crystal frequency deviation from 3.579545 MHz will be reflected in the tone output frequency. Most crystals do not vary more than ± .02%.

OUTPUT FREQUENCY DEVIATION

Table 2

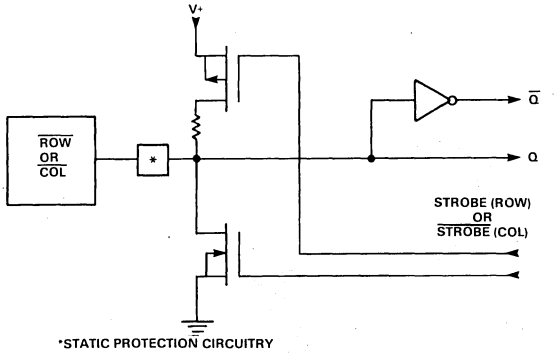
		Standard DTMF (Hz)	Tone Output Frequency Using 3.579545 MHz Crystal	% Deviation From Standard	
$\overline{\text{ROW}}$	f_1	697	699.1	+0.31	Low Group
	f_2	770	766.2	-0.49	
	f_3	852	847.4	-0.54	
	f_4	941	948.0	+0.74	
$\overline{\text{COL}}$	f_5	1209	1215.9	+0.57	High Group
	f_6	1336	1331.7	-0.32	
	f_7	1477	1471.9	-0.35	
	f_8	1633	1645.0	+0.73	

MUTE OUT, Pin 10

The Mute output is a conventional CMOS inverter that pulls to V– with no keyboard input and pulls to the V+ supply when a keyboard entry is sensed. This output is used to control auxiliary switching functions that are required to actuate upon keyboard input. The Mute output switches regardless of the state of the Single Tone Inhibit input. Mute output is not affected by keyboard inputs when $\overline{\text{CD}}$ is tied to V–.

$\overline{\text{ROW}}$ AND $\overline{\text{COLUMN}}$ INPUTS

Figure 5



NOTE: $\overline{\text{Chip Disable}}$ is floating or tied to V+.
When $\overline{\text{CD}}$ is tied to V–, $\overline{\text{Row}}$ and $\overline{\text{Column}}$ inputs go to a high impedance state.

SINGLE TONE INHIBIT, Pin 15

The Single Tone Inhibit input is used to inhibit the generation of other than dual tones. It has a pull-up to the V+ supply and, when floating or tied to V+, single or dual tones may be generated as described in the paragraph under Row-Column inputs.

When forced to the V– supply, any time two or more rows (or columns) are activated, no tone will result.

TONE OUT, Pin 16

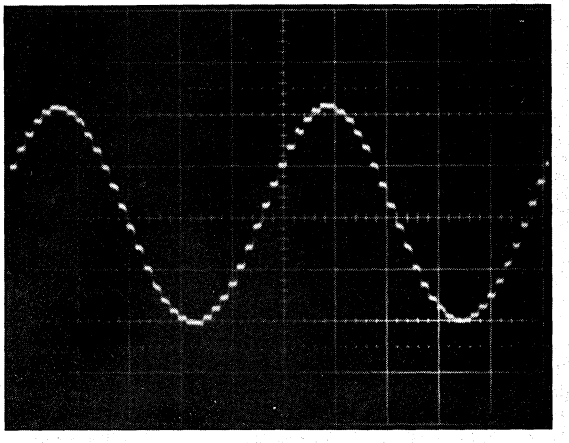
The Tone output pin is connected internally in the MK5380 to the emitter of an npn transistor whose collector is tied to V+. The base of this transistor is the output of the on-chip operational amplifier which mixes the row and column tones together.

The level of a dual tone output is the sum of the levels of a single row and a single column output. This level is controlled by an on-chip reference which is not sensitive to variations in the supply voltage.

A typical single tone sine wave output is shown in Figure 6. This waveform is synthesized using a resistor tree with sinusoidally weighted taps.

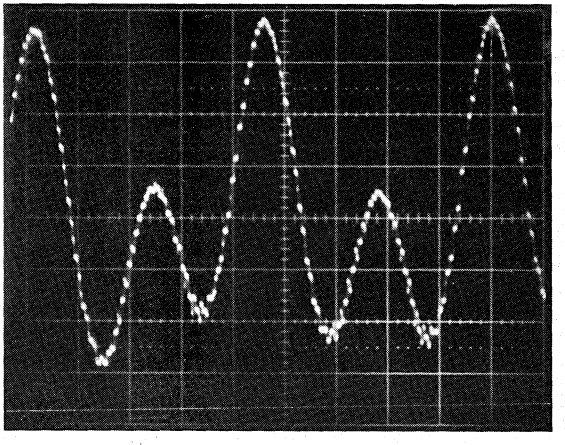
A simple measurement of distortion may be made directly from the screen of a spectrum analyzer by comparing any component to one of the fundamentals.

TYPICAL SINE WAVE OUTPUT - SINGLE TONE
Figure 6

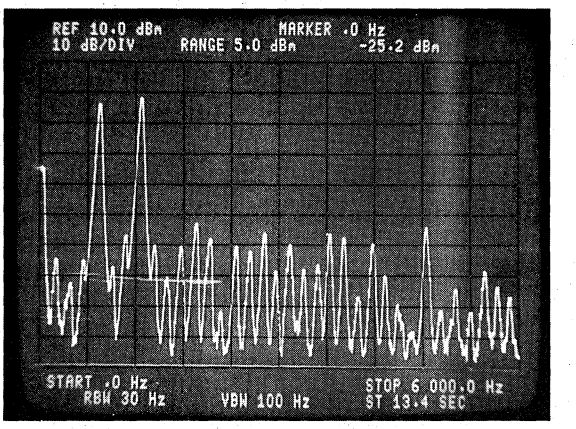


Figures 7 and 8 show a typical dual-tone waveform and its spectral analysis.

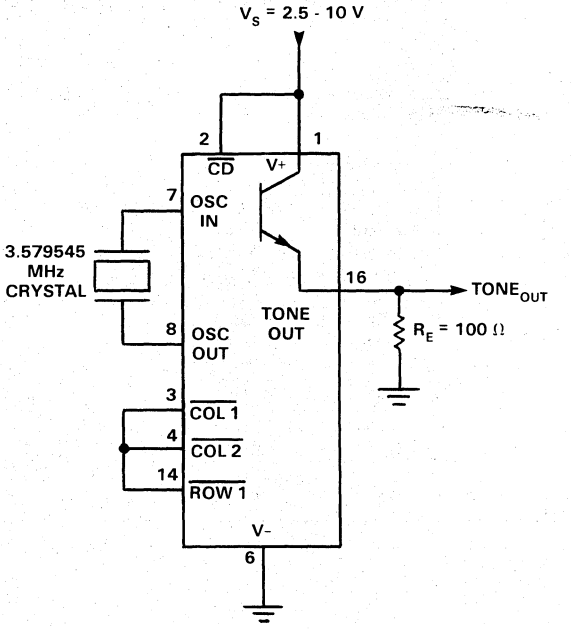
TYPICAL DUAL-TONE WAVEFORM (Row 1, Col 1)
Figure 7



SPECTRAL ANALYSIS OF WAVEFORM IN FIG. 7
(Vert-10 dB/div. Horizontal - 600 Hz/div.)
Figure 8



TONE LEVEL TEST CIRCUIT
Figure 9



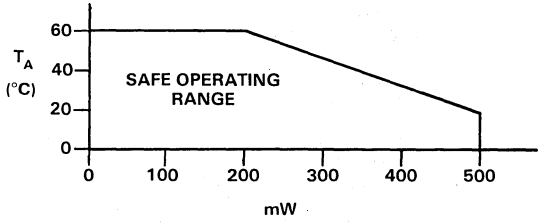
NOTE: The above circuit connections are for a Row 1 single tone test. For a Col 1 single-tone test, connect Row 1 (Pin 14) and Row 2 (Pin 13) to Col 1 (Pin 3).

ABSOLUTE MAXIMUM RATINGS*

DC Supply Voltage V+ ..... 10.5 volts
Any Input Relative to V+ ..... +0.30 volts
Any Input Relative to V– ..... –0.30 volts
Operating Temperature ..... –30°C to +60°C
Storage Temperature ..... –55°C to +125°C
Maximum Circuit Power Dissipation ..... 500mW @ 25°C (see derating curve below)

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

POWER DISSIPATION DERATING CURVE



DERATE AT 9 mW/°C WHEN SOLDERED INTO PC BOARD.

ELECTRICAL CHARACTERISTICS
DC CHARACTERISTICS

($-30°C \leq T_A \leq 60°C$)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V+	DC Operating Voltage	2.5		10.0	V	1
V_{IL}	Input Voltage Low - "0"	V–		30% of V+	V	1
V_{IH}	Input Voltage High - "1"	70% of V+		V+	V	1
R_{IP}	Input Pull-Up Resistance, $\overline{STI}$, $\overline{CD}$	20		100	kΩ	
I_{SSB}	Supply Current - Standby and $\overline{CD}$ tied to V–		10	150	μA	3,4,6
			10	250		3,4,7
I_{SO}	Supply Current - Operating ($\overline{CD}$ floating or tied to V+)		1.0	2.0	mA	3,5,6
			5.0	10		3,5,7
R_{KPU}	Keyboard Pull-Up Resistance $\overline{CD}$ tied to V+		100		kΩ	8
	$\overline{CD}$ tied to V–		10		MΩ	
R_{KPD}	Keyboard Pull-Down Resistance $\overline{CD}$ tied to V+		4.0		kΩ	8
	$\overline{CD}$ tied to V–		10		MΩ	
I_{OLM}	Output Drive, MUTE - No Entry	0.5	2.0		mA	9
		1.0	4.0			10
I_{OHM}	Output Drive, MUTE - Valid Entry	0.5	2.0		mA	11
		1.0	4.0			12

AC CHARACTERISTICS

($-30°C \leq T_A \leq 60°C$; $2.5\ V \leq V+ \leq 10.0\ V$)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
t_{RISE}	Tone Output Rise Time			5.0	ms	13,14
$TONE_{NKD}$	Tone Output-No Key Down or $\overline{CD}$ tied to V–			-80	dBm (600 Ω)	2
$TONE_{OUT}$	Tone Output Voltage (Key Down and $\overline{CD}$ floating or tied to V+)		155		mV_{rms}	15,16,17,18
PE_{HB}	Pre-Emphasis, High Band		2.0		dB	16
DIS	Output Distortion		5.0	10.0	%	16
f_{KBS}	Keyboard Scan Frequency	699		948	Hz	8

NOTES

1. All voltages referenced to V– (Pin 6).
2. $2.5\ V \leq V+ \leq 10.0\ V$.
3. All outputs unloaded.
4. Current out of Pin 6, no key depressed.
5. Current out of Pin 6, one key depressed.
6. V+ = 2.5 V.
7. V+ = 10.0 V.
8. When $\overline{Row}$ or $\overline{Column}$ inputs are sensed, the keyboard inputs are alternately strobed. When a $\overline{Row}$ is strobed, the $\overline{Row}$ pull-down and $\overline{Column}$ pull-up resistances are enabled. This strobing alternates in the frequency range of 699 to 948 Hz depending on which row is selected. When no inputs exist, either a $\overline{Row}$ or a $\overline{Column}$ input will be statically sensed.
9. V+ = 2.5 V, V_{OLM} = 0.5 V.
10. V+ = 10.0 V, V_{OLM} = 0.5 V.
11. V+ = 2.5 V, V_{OHM} = 2.0 V.
12. V+ = 10.0 V, V_{OHM} = 9.5 V.
13. Time from a valid keystroke with no bounce to allow wave to go from minimum to 90% of final magnitude of either frequency.
14. Crystal parameters: $R_S \leq 100\ \Omega$, L_M = 96 mH, C_M = 0.02 pF, C_h = 5 pF, f = 3.579545 MHz, C_L = 18 pF.
15. Single-tone, low-group $T_A = 25°C$.
16. $2.5\ V \leq V+ \leq 10.0\ V$, $R_E = 100\ \Omega$ (See Figure 9).
17. $TONE_{OUT}$ measured at Pin 16 (See Figure 9).
18. The tone level, when used in a subscriber set, is a function of the output resistor R_E and the telephone ac resistance (R_L). The low-group single-tone output amplitude is a function of R_E and R_L by the relationship:

$$\frac{V_o}{TONE_{OUT}} = \frac{1}{0.2 + \frac{R_E}{R_L}}$$

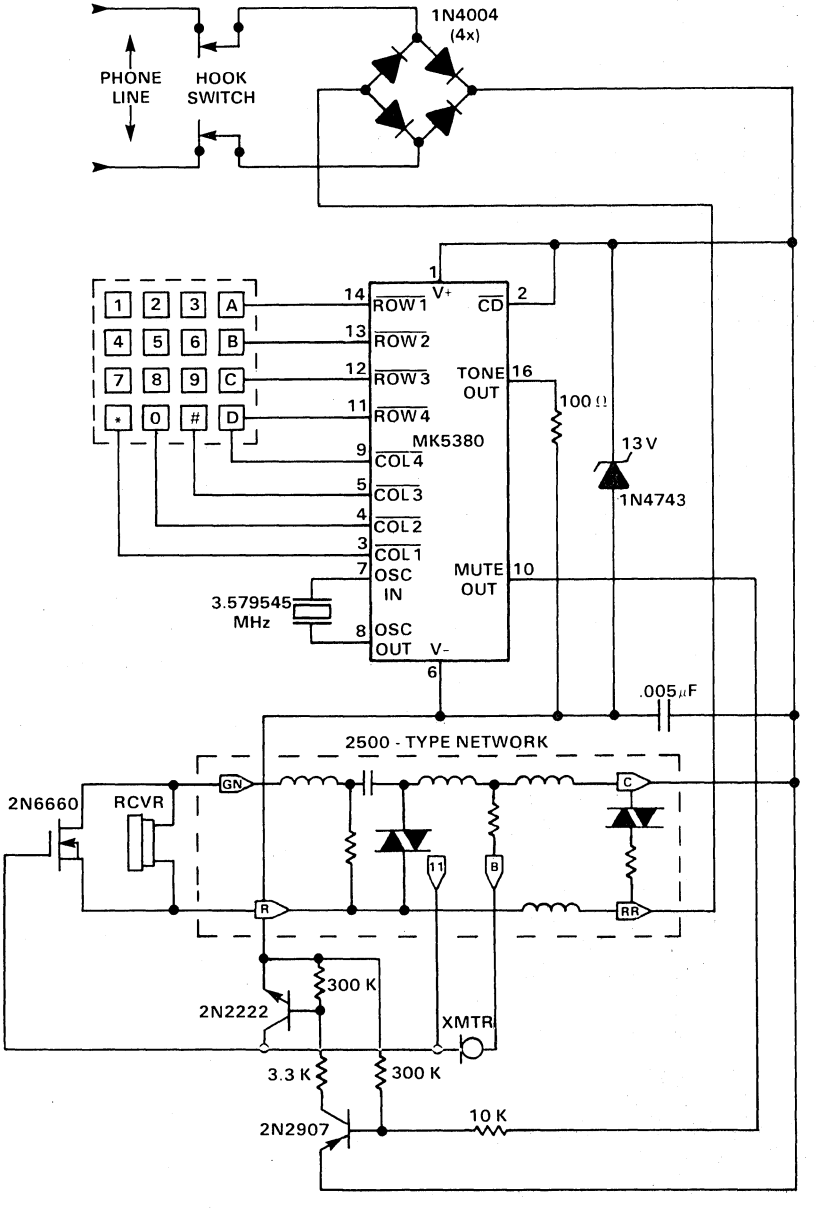
where V_o is the tone output amplitude at the phone line, and R_L is the equivalent ac impedance in shunt with the tone generator (R_L typically varies with loop current). R_E is the resistor value from $TONE_{OUT}$ to V–. In a 2500-Type application R_L will typically vary from 200 to 500 Ω. Thus, at the phone line tone output levels will range from 200 to 400 mV_{rms}, depending on loop current.

TYPICAL APPLICATION

Figure 10 shows an application of the MK5380 in a standard telephone set that uses the standard 2500-Type Network.

TYPICAL APPLICATION IN 2500-TYPE TELEPHONE

Figure 10



NOTE: Transient protection circuitry not shown.

PRODUCT PROFILE

MOSTEK®

TELECOMMUNICATION PRODUCTS

Integrated Tone Dialer With Redial

MK5382(N/P/J)

FEATURES

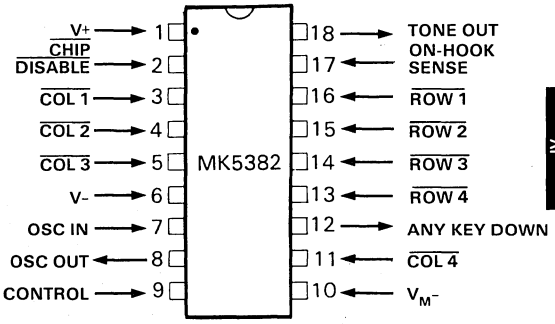
- Low standby power
- Uses inexpensive 3.579545 MHz television color-burst crystal to provide high-accuracy tones
- Distortion lower than industry standards
- Low voltage operation - 2.5 volts
- Uses low-cost calculator-type keyboard (Form A contact) or standard 2-of-8 keyboard
- 16-digit last number redial
- Up to 2 PBX access digits may be dialed before using last number redial function
- Off-hook store into memory without dialing
- On-chip power-up-clear and memory-loss-detect circuitry
- Low memory retention current
- 12/16 keyboard or external control key redial access

DESCRIPTION

The MK5382 is a monolithic integrated circuit fabricated using the complementary - symmetry MOS (CMOS) process. A member of the Tone III* family of integrated tone dialers, the MK5382 uses an inexpensive crystal reference to provide eight different audio sinusoidal frequencies, which are mixed to provide tones suitable for Dual-Tone-Multi-Frequency (DTMF) telephone dialing.

PIN CONNECTIONS

Figure 1



The MK5382 was designed specifically for integrated tone-dialer applications that require the following: wide-supply operation with regulated output, scanned keyboard inputs which recognize either negative-true or Class A closures, a $\overline{\text{Chip Disable}}$ input, and an Any Key Down output that is high impedance with no keyboard entry and pulls to the V+ supply when a keyboard button is pushed.

The MK5382 will redial 3 to 16 digits. The redial function may be employed immediately after going off-hook, after dialing one PBX access digit, or after dialing two PBX access digits. An "off-hook store" function allows a number to be entered into the last number dial memory for later use with no tones emitted during entry.

On-chip power-up-clear circuitry and memory-loss-detection circuitry insure that no false numbers, due to power loss, can be redialed.

*Trademark of Mostek Corporation

MOSTEK®

TELECOMMUNICATION PRODUCTS

Integrated Dialer Comparison-Tone II vs Tone III

The purpose of this Application Brief is to define the major differences between Mostek's Tone II* and Tone III* series of integrated tone dialers.

The Tone III series was developed as an improvement over Tone II. The minimum operating dc voltage of Tone III has been reduced and loop compensation of the tones generated has been improved. Distortion has also been reduced due to a scheme in which DTMF tones are synthesized using a sinusoidally tapped resistor tree.

The Tone III family of integrated tone dialers is fabricated using Mostek's Silicon Gate CMOS process. Tone III devices use a scanned keyboard scheme with which various keyboard types or electronic input may be used. Tone III dialers also have a Chip Disable feature which causes tone generation to be inhibited, the keyboard inputs to go to a high-impedance state, and the amplifiers and oscillator to be powered down.

The following is a comparison of the major differences between the MK5087 and MK5089 (Tone II), and the MK5380 (Tone III).

KEYBOARD TYPE

- ☐ MK5087 - Class A; 2-of-7 or 2-of-8 (K/B common floating)
- ☐ MK5089 - 2-of-7 or 2-of-8 (K/B common tied to V-)
- ☐ MK5380 - Class A; 2-of-7 or 2-of-8 (K/B common floating or tied to V-)

AUXILIARY FUNCTIONS

- ☐ Pin 2
  - MK5087 - Bipolar XMTR SW (no key = 1; key input = open)
  - MK5089 - $\overline{\text{Tone Disable}}$
  - MK5380 - $\overline{\text{Chip Disable}}$
- ☐ Pin 10
  - MK5087/5380 - CMOS MUTE SW (no key = 0; key input = 1)
  - MK5089-N-Chnl MUTE SW ($\overline{\text{AKD}}$) (no key = open; key input = 0)

*Trademark of Mostek Corporation

DC OPERATING VOLTAGE

- ☐ MK5087 - 3.5 to 10.0 V
- ☐ MK5089 - 3.0 to 10.0 V
- ☐ MK5380 - 2.5 to 10.0 V

TONE OUTPUT

- ☐ MK5089 - Low Group: .0855 $V_{DD} \pm 1$ dB V_{rms} into 10 kΩ load
  High Group: 2.7 dB above low group

The following are designed to deliver U.S. telephone system tone levels in a telephone. On a fixed supply the levels will be:

- ☐ MK5087 - Low Group: 317-504 mV_{rms} into 1 kΩ load
  High Group: 2.0 dB above low group
- ☐ MK5380 - Low Group: 245 mV_{rms} typically (see notes 1 and 2)
  High Group: 2.0 dB above low group

TYPICAL APPLICATIONS

- ☐ MK5087 (Uses fixed supply or modulating supply in telephone)
  - Telephone tone-dialer applications
- ☐ MK5089 (Uses fixed or regulated supply in telephone)
  - Electronic or μP-dialing applications
  - European telephone applications
- ☐ MK5380 (Uses fixed supply or modulating supply in telephone)
  - Telephone tone-dialer applications
  - Electronic or μP-dialing applications

NOTES:

1. $TONE_{OUT}$ (measured at Pin 16 in loop applications) = 155 mV_{rms} (typical). $R_E = 100\ \Omega$.
2. In loop applications, the low-group single-tone output amplitude is a function of R_E and R_L by the relationship:

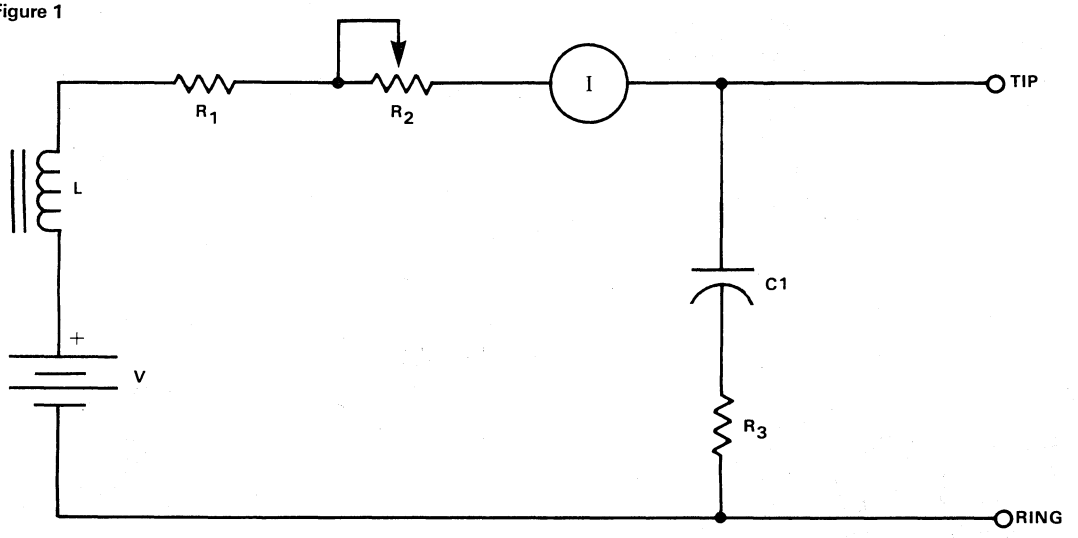
$$\frac{V_o}{TONE_{OUT}} = \frac{1}{0.2 + \frac{R_E}{R_L}}$$

where V_o is the tone output amplitude at the phone line and R_L is the equivalent ac impedance in shunt with the tone generator (R_L typically varies with loop current), R_E is the resistor value from $TONE_{OUT}$ to V-. In a 2500-Type application R_L will typically vary from 200 to 500 Ω. Thus, at the phone line, tone output levels will range from 200 to 400 mV_{rms}, depending on loop current.

Loop Simulator

The following is a simple circuit which can be used to simulate a telephone loop for most testing purposes. Potentiometer R2 may be varied to provide various loop currents simulating different loop lengths. Normal loop currents range between 20 and 80 mA. Resistor R1 is used to limit the loop current to a maximum of approximately 120 mA (Tip and Ring short-circuited). An ammeter, I, is used to measure the loop current and capacitor C1 and resistor R3 are used to simulate the 600 Ω impedance of the telephone line. Inductor L provides a high impedance in series with the power supply so that the impedance across Tip and Ring is effectively 600 Ω.

Figure 1



V = 48 V (power supply or battery)

R1 = 250 Ω (5 Watts)

R2 = 2 kΩ (2 Watts)

R3 = 600 Ω ±1% (¼ Watt)

I = Ammeter (100 mA full scale)

C1 = 500 μF, -10%, +50%, (50 V)

L ≥ 10 H up to 150 mA dc
($R_L \approx 150\ \Omega$)

1982 TELECOMMUNICATION PRODUCTS DATA BOOK

MOSTEK®

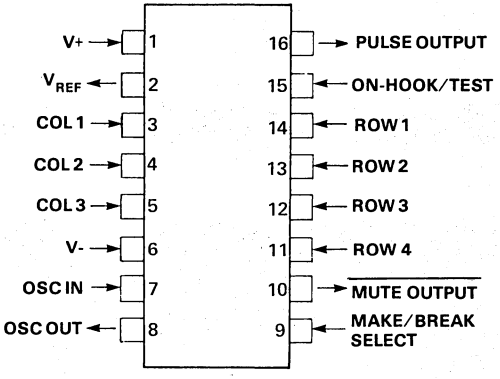
INTEGRATED PULSE DIALER WITH REDIAL

MK50981(N)

FEATURES

- ☐ Direct telephone-line operation
- ☐ CMOS technology is used for low-voltage, low-power operation
- ☐ Uses either a standard 2-of-7 matrix keyboard with pos. true common or the inexpensive Form A-type keyboard
- ☐ Ceramic resonator used as frequency reference for guaranteed accuracy
- ☐ Make/Break ratio pin-selectable
- ☐ Redial with either a * or # input
- ☐ Provision for rapid testing
- ☐ On-chip voltage regulator
- ☐ Power-Up-Clear circuitry

PIN CONNECTIONS



DESCRIPTION

The MK50981 is a monolithic CMOS integrated circuit which converts keyboard inputs into pulse signal outputs simulating a rotary telephone dial. It is designed to operate directly from the telephone line and can be interfaced properly to meet telephone specifications in systems utilizing loop-disconnect signalling. Two outputs, one to pulse the telephone line and one to mute the receiver, are provided to implement the pulse dialer function. Accurate timing is accomplished by using a ceramic resonator as the frequency reference for the on-chip oscillator.

The MK50981 is in either the on-hook or off-hook mode as determined by the input to the pin designated "On-Hook/Test." In order to accept any key inputs, the MK50981 must be in the off-hook state. Upon sensing a key input, the normally static oscillator is enabled and the row and column inputs are alternately strobed to verify that the keyboard input is valid. The decoded input is then entered into an on-chip memory. The memory will store up to 17 digits and allows keystrokes to be entered at rates comparable to tone dialing telephones. Entering the first digit (except * or #) clears the memory buffer and starts the outpulsing sequence. As additional digits are entered, they are stored in the memory and outpulsed in turn. The memory has a FIFO—(first-in-first-out) type architecture and more than 17 digits may be dialed in any number sequence. The limitation is that there can never be more than 17 digits remaining to be outpulsed.

The MK50981 also features the redial function. Any 17-digit number sequence may be redialed with a * or # key input, providing that the circuit enters the on-hook mode for a finite time, t_{OH} (refer to discussion on the On-Hook/Test Pin).

An on-chip "Power-Up-Clear" circuit insures reliable operation of the MK50981. If the supply to the circuit should become insufficient to retain data in the memory (see electrical specifications), a "Power-Up-Clear" will occur upon regaining a proper supply level. This function will prevent the "Redial" or spontaneous outpulsing of incorrect data. A new number sequence may then be entered in normal fashion.

Functions of the individual pins are described below.

V+, Pin 1

This is the positive supply input to the part and is measured relative to V- (Pin 6). The voltage on this pin must be regulated to less than 6 volts using either the on-chip reference circuitry or an external form of regulation.

V_{REF}, Pin 2

The V_{REF} output provides a negative reference voltage relative to the V+ supply. Its magnitude is a function of the

ABSOLUTE MAXIMUM RATINGS*

DC Supply Voltage, V+ ..... 6.2 Volts
Operating Temperature ..... -30°C to +60°C
Storage Temperature ..... -55°C to +85°C
Maximum Power Dissipation 25°C 500mW
Maximum Voltage on any Pin ..... (V+) + 0.3; (V–) –0.3 Volts

*Stresses above these listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

$-30°C \leq T_A \leq 60°C$

DC CHARACTERISTICS

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V+	DC Operating Voltage	2.5		6.0	V	
I_{MR}	Memory Retention Current		0.7	2.5	μA	1
I_{OP}	DC Operating Current		100	150	μA	2
V_{REF}	Magnitude of (V+ - V_{REF}) I_{SUPPLY} = 150μA	1.5	2.5	3.5	V	
I_M	Mute Sink Current: V+ = 2.5V, Vo = 0.5V	0.5	2.0		mA	
I_P	Pulse Sink Current: V+ = 2.5V, Vo = 0.5V	1.0	4.0		mA	
I_{LKG}	Mute and Pulse Leakage: V+ = 6.0V, Vo = 6.0V		0.001	1.0	μA	
R_{KI}	Keyboard Contact Resistance			1.0	kΩ	
C_{KI}	Keyboard Capacitance			30	pF	
K_{IL}	"0" Logic Level	V–		20% of V+	V	
K_{IH}	"1" Logic Level	80% of V+		V+	V	
K_{RU}	Keyboard Pull-Up Resistance		4.0		kΩ	3
K_{RD}	Keyboard Pull-Down Resistance		100		kΩ	3
R_{OH}	On-Hook Pull-Up Resistance		100		kΩ	

NOTES

Typical values are to be used as a design aid and are not subject to production testing.

1. Current necessary for memory to be maintained. All outputs unloaded. On-Hook mode.
2. Current required for proper circuit function. Off-Hook Mode. Valid key input, V_{REF} tied to V–.
3. Keyboard to be scanned at 500Hz when oscillator enabled. Row and Column to alternately pull high and low.

AC CHARACTERISTICS

(The Timing Relationships are shown in Figure 3)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
f_{OSC}	Oscillator Frequency (antiresonant mode)		480		kHz	1
t_{DB}	Keyboard Debounce Time		10		ms	
t_{KD}	Time for Valid Key Entry	40			ms	
t_{OS}	Oscillator Start-Up Time		6.0		ms	
P_R	Pulse Rate		10.0		pps	
t_B	Break Time: Pin 9 tied to V+/ tied to V–		61.0/67.0		ms	
t_{IDP}	Interdigital Pause		800		ms	

NOTES

"Typical" values are exact values with a nominal 480 kHz frequency reference (except for oscillator start-up time).

1. Ceramic resonator should have the following equivalent values: R<20 Ω, R_A ≥ 70 kΩ. Co ≤ 500 pF.

internal parameters which define the minimum operating voltage of each part. In a typical application, as shown in Figure 4, the V_{REF} pin is simply tied to V– (Pin 6). The internal circuit with its associated I-V characteristic is shown in Figure 1.

KEYBOARD INPUTS, Pins 3, 4, 5, 11, 12, 13, 14

The MK50981 incorporates an innovative keyboard scheme that allows either the standard 2-of-7 keyboard with positive common or the inexpensive single-contact (Form A) keyboard to be used, as shown in Figure 2.

A valid key entry is defined by either a single row being connected to a single column or V+ being simultaneously presented to both a single row and column.

When in the On-Hook mode, the row and column inputs are held high and no keyboard inputs are accepted. When Off Hook, the keyboard is completely static until the initial valid key input is sensed. The oscillator is then enabled and the row and columns are alternately scanned (pulled high, then low) to verify the input is valid. The input must remain valid continuously for 10ms of debounce time to be accepted.

V–, Pin 6

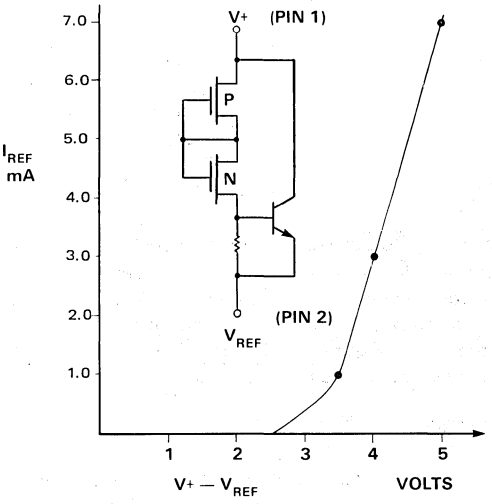
This pin is the negative supply pin input.

OSCILLATOR IN, OUT, Pin 7, 8

The MK50981 contains an on-chip inverter with sufficient gain to provide oscillation when working with a low-cost 480kHz ceramic resonator (anti-resonant mode). In addition to the resonator, two external capacitors are required.

TYPICAL I—V CHARACTERISTICS

Figure 1



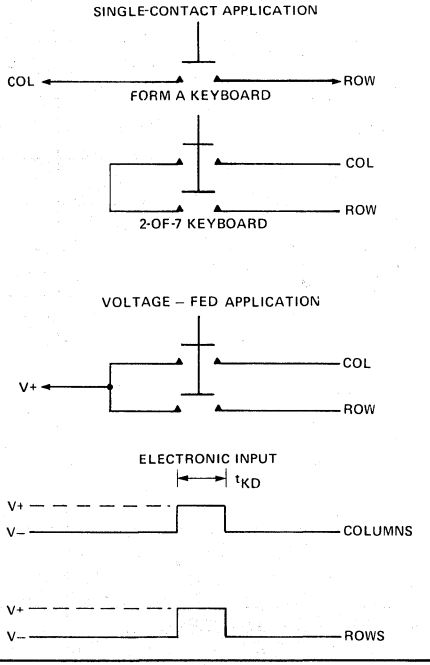
Suggested equivalent values for the resonator are given in the timing specification section. These values will insure proper oscillator operation in the specified voltage range. The MK50981 may be driven externally with a 480kHz signal on Pin 7.

MAKE/BREAK SELECT, Pin 9

The Make/Break ratio may be selected by connecting the pin to either the V+ or V– supply. Table 1 indicates the two popular ratios from which the user can choose.

KEYBOARD CONFIGURATION

Figure 2



MAKE/BREAK RATIO SELECTION

Table 1

Input To Make/Break Pin	Pulse Output	
	Make	Break
V+ (Pin 1)	39%	61%
V– (Pin 6)	33%	67%

$\overline{\text{MUTE OUTPUT}}$, Pin 10

The $\overline{\text{Mute Output}}$ consists of an open-drain N-channel transistor. It provides the logic necessary to mute the receiver while the telephone line is being pulsed. A typical way to interface this output is shown in the application diagram in Figure 4. Figure 3 shows the timing characteristics of the $\overline{\text{Mute}}$ Output.

ON-HOOK/TEST, Pin 15

The "Test" or "On-Hook" input of the MK50981 has a 100kΩ pull-up to the positive supply. A V+ input or allowing the pin to float sets the circuit in its On-Hook or test mode, while a V– input sets it in the Off-Hook or Normal Mode.

When Off-Hook, the MK50981 will accept key inputs and outpulse the digits in normal fashion. Upon completion of the last digit, the oscillator is disabled and the circuit stands by for additional inputs.

Switching the MK50981 to On-Hook while it is outpulsing causes the remaining digits to be outpulsed at 100 x the normal rate (M/B ratio is then 50/50). This feature provides a means of rapidly testing the device and is also an efficient method by which the circuitry is reset. When the outpulsing in this mode, which can take up to 300ms, is completed, the circuit is deactivated and will require only the current necessary to sustain the memory and Power-Up-Clear detect circuitry (refer to the electrical specifications).

Upon returning Off-Hook, if the first key entry is either * or #, the number sequence stored on-chip will be outpulsed. Any other valid key entries will clear the memory and outpulse the new number sequence.

PULSE OUTPUT, Pin 16

The Pulse output is an open-drain N-channel transistor. This output provides the logic necessary to pulse the telephone line with the correct Make/Break, pulse rate, and interdigital pause timings. The timing characteristics of the Pulse output are shown in Figure 3.

TYPICAL APPLICATION

The schematic diagram in Figure 4 shows one method which can be used to interface the pulse dialer with the telephone line. In the approach shown, the pulse dialer circuitry is in parallel with the speech network.

A current source of some type is desired to present a high impedance to the telephone line while guaranteeing sufficient current to power the MK50981 ($\geq 150\mu A$). The current is sourced by the collector of transistor Q2. Its magnitude is determined by the voltage drop across R1, caused by the forward-biased diodes, D1 and D2. Transistor Q1 provides the quiescent current for the diodes and base drive for Q2.

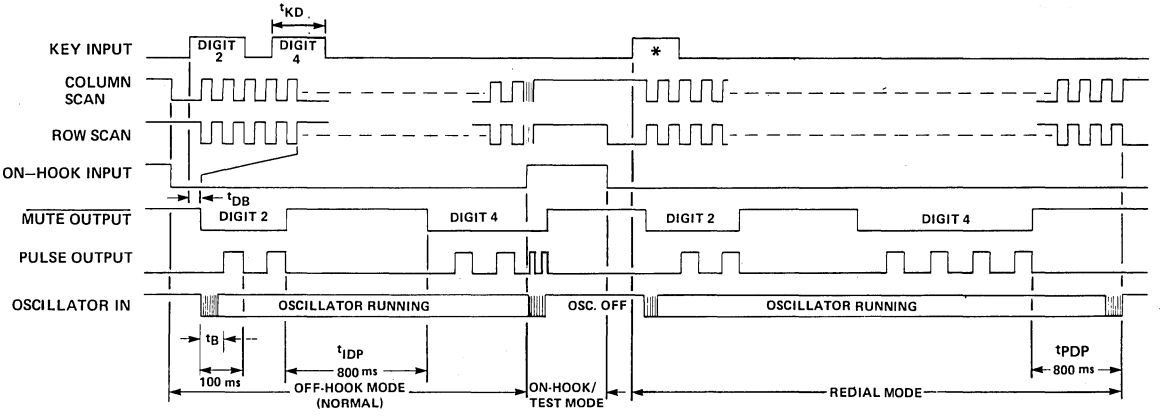
When in the On-Hook mode, S1 and S2 are open. This disables the current source and eliminates any excess current flow through the base-emitter junction of Q1 by allowing the emitter to be pulled to V+ through On-Hook. A large-value resistor, R3, allows a small amount of current to maintain the memory on the MK50981.

To return Off-Hook S1 and S2 are closed, thus tying the On-Hook pin to V–. The pulse and mute outputs drive external transistors to perform the outpulsing function. The speech network is connected through transistor Q5 to the telephone line. $\overline{\text{Mute}}$ holds this transistor on until outpulsing begins. The first break occurs when $\overline{\text{Mute}}$ switches low and the speech network is removed from the line. The pops caused by breaking the line are then isolated from the receiver. The pulse output drives Darlington pair Q3 and Q4 to make and break the line until the digit has been completely pulsed. $\overline{\text{Mute}}$ then switches high, returning the speech network to the line.

Other implementations may consider a constant current diode for the current source or muting the network with a Darlington. If your application requires muting the network with a relay, request information on our MK50991 outpulser.

TIMING CHARACTERISTICS

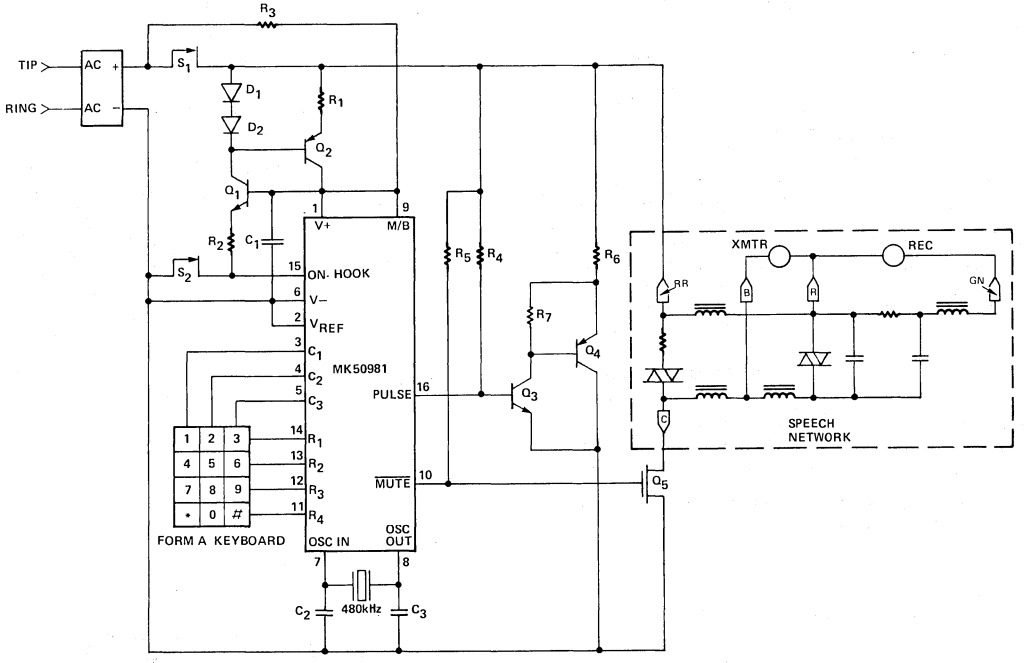
Figure 3



NOTE: Pulse Output goes high for Make, low for Break.

TYPICAL APPLICATION

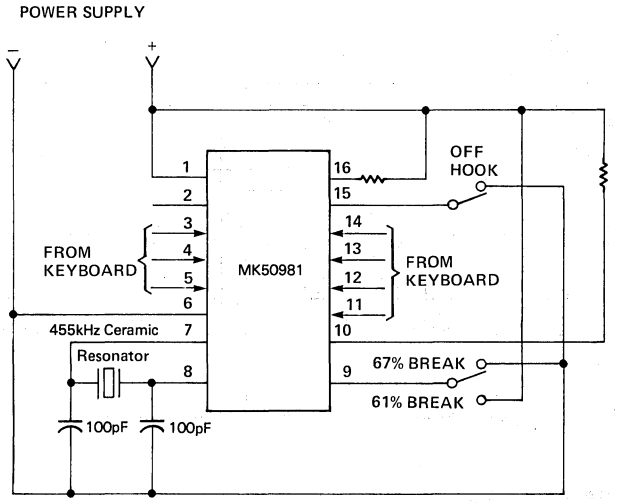
Figure 4



Q_1 2N5550	Q_5 2N6661	C_2 100pF ±20%	R_3 22MΩ
Q_2 2N5401	D_1 1N914	C_3 100pF ± 20%	R_4 390kΩ
Q_3 2N5550	D_2 1N914	R_1 2.7kΩ	R_5 1MΩ
Q_4 2N5401	C_1 20μF (LOW LEAKAGE)	R_2 75kΩ	R_6 150Ω
			R_7 100kΩ

TEST CIRCUIT

Figure 5



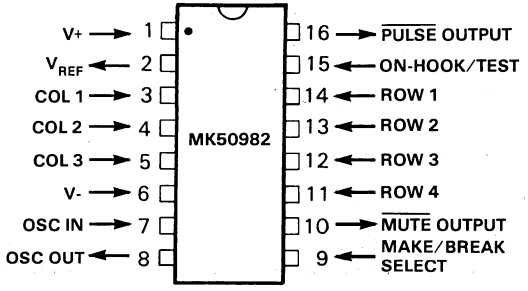
INTEGRATED PULSE DIALER WITH REDIAL

MK50982(N)

FEATURES

- Direct telephone-line operation
- CMOS technology is used for low-voltage, low-power operation
- Uses standard 2-of-7 matrix with pos. true common or the inexpensive Form A-type keyboard
- Ceramic resonator used as frequency reference for guaranteed accuracy
- Make/Break ratio pin-selectable
- Redial with either * or #
- Provision for rapid testing
- On-chip voltage regulator
- Power-Up-Clear circuitry

PIN CONNECTIONS



DESCRIPTION

The MK50982 is a monolithic CMOS integrated circuit which converts keyboard inputs into pulse signal outputs simulating a rotary telephone dial. It is designed to operate directly from the telephone line and can be interfaced properly to meet telephone specifications in systems utilizing loop-disconnect signalling. Two outputs, one to pulse the telephone line and one to mute the receiver, are provided to implement the pulse dialer function. Accurate timing is accomplished by using a ceramic resonator as the frequency reference for the on-chip oscillator.

The MK50982 is in either the on-hook or off-hook mode as determined by the input to the pin designated, "On-Hook/Test." In order to accept any key inputs, the MK50982 must be in the off-hook state.

Refer to Figure 1 for a block diagram. Upon sensing a key input, the normally static oscillator is enabled and the row and column inputs are alternately strobed to verify that the keyboard input is valid. The decoded input is then entered into an on-chip memory. The memory will store up to 17 digits and allows keystrokes to be entered at rates comparable to tone dialing telephones. Entering the first digit (except* or #) clears the memory buffer and starts the outpulsing sequence. As additional digits are entered, they are stored in the memory and outpulsed in turn. The memory has FIFO-(first-in-first-out) type architecture and more than 17 digits may be dialed in any number sequence. The limitation is that there can never be more than 17 digits remaining to be outpulsed.

The MK50982 also features the redial function. Any 17-digit number sequence may be redialed with an* or # key input, providing that the circuit enters the on-hook mode for a finite time, t_{OH} (refer to discussion on the On-Hook/Test Pin).

An on-chip "Power-Up-Clear" circuit insures reliable operation of the MK50982. If the supply to the circuit should become insufficient to retain data in the memory (see electrical specifications), a "Power-Up-Clear" will occur upon regaining a proper supply level. This function will prevent the "Redial" or spontaneous outpulsing of incorrect data. A new number sequence may be entered in normal fashion.

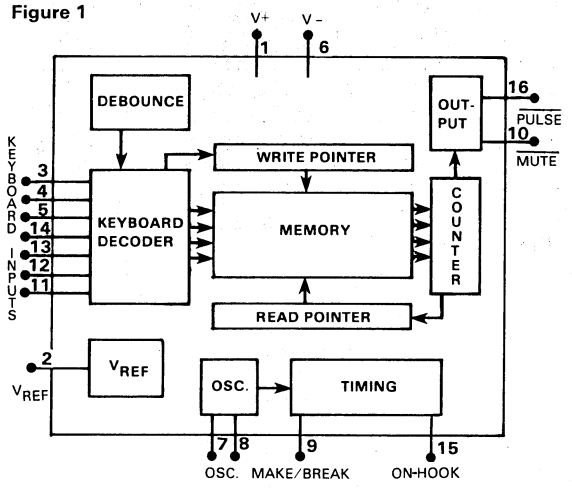
FUNCTIONAL DESCRIPTION

V+, Pin 1

This is the positive supply input to the part and is measured relative to V- (pin 6). The voltage on this pin must be regulated to less than 6 volts using either the on-chip reference circuitry or an external form of regulation.

BLOCK DIAGRAM

Figure 1

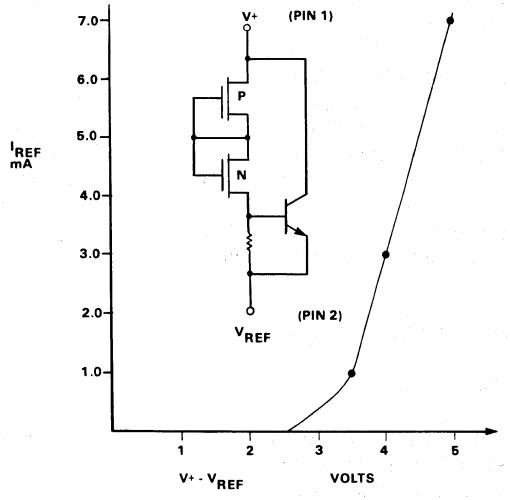


V_{REF}, Pin 2

The V_{REF} output provides a negative reference voltage relative to the V+ supply. Its magnitude is a function of the internal parameters which define the minimum operating voltage of each part. In a typical application, as shown in Figure 5, the V_{REF} pin is simply tied to V-(Pin 6). The internal circuit with its associated I-V characteristic is shown in Figure 2.

TYPICAL I-V CHARACTERISTICS

Figure 2



V-, Pin 6

This is the negative supply pin to which V_{REF} is normally tied (see V_{REF} paragraph).

KEYBOARD INPUTS, Pins 3, 4, 5, 11, 12, 13, 14

The MK50982 incorporates an innovative keyboard scheme that allows either the standard 2-of-7 keyboard with positive common or the inexpensive single-contact (Form A) keyboard to be used, as shown in Figure 3.

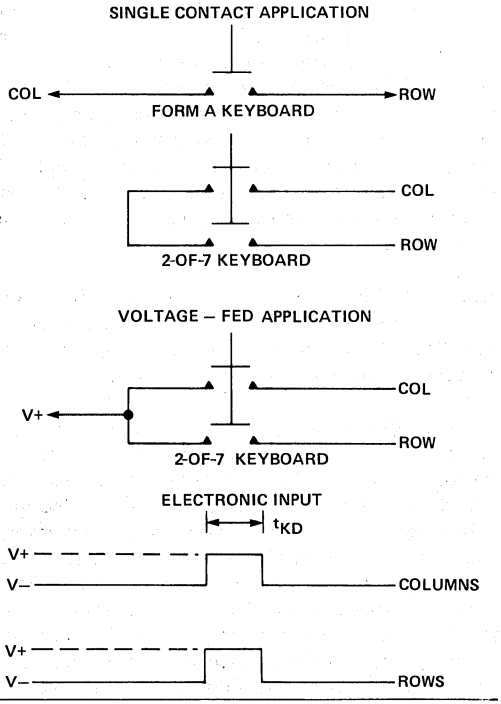
A valid key entry is defined by either a single row being connected to a single column or V+ being simultaneously presented to both a single row and column.

When in the On-Hook mode, the row and column inputs are held high and no keyboard inputs are accepted, thus preventing any accidental key contacts from causing excessive current flow.

When Off-Hook, the keyboard is completely static until the initial valid key input is sensed. The oscillator is then enabled and the row and columns are alternately scanned (pulled high, then low) to verify the input is valid. The input must remain valid continuously for 10ms of debounce time to be accepted.

KEYBOARD CONFIGURATION

Figure 3



OSCILLATOR IN, OUT, Pins 7, 8

The MK50982 contains an on-chip inverter with sufficient gain to provide oscillation when used with a low-cost 480kHz ceramic resonator (anti-resonant mode). In addition to the resonator, two external capacitors are required. Suggested equivalent values for the resonator are given in the timing specification section. These values will insure proper oscillator operation in the specified voltage range. The MK50982 may be driven externally with a 480kHz signal on Pin 7.

MAKE/BREAK SELECT, Pin 9

The Make/Break ratio may be selected by connecting the pin to either the V+ or V- supply. Table 1 indicates the two popular ratios from which the user can choose.

MAKE/BREAK RATIO SELECTION
Table 1

Input to Make/Break Pin	Pulse Output	
	MAKE	BREAK
V+ (Pin 1)	39%	61%
V- (Pin 6)	33%	67%

$\overline{\text{MUTE}}$ OUTPUT, Pin 10

The $\overline{\text{Mute}}$ output consists of an open-drain N-channel transistor. It provides the logic necessary to mute the receiver while the telephone line is being pulsed. A typical method of interfacing this output is shown in the application diagram in Figure 5. Figure 6 shows the timing characteristics of the $\overline{\text{Mute}}$ output.

ON-HOOK/TEST, Pin 15

The "Test" or "On-Hook" input of the MK50982 has a 100kΩ pull-up to the positive supply. A V+ input or allowing the pin to float sets the circuit in its On-Hook or test mode, while a V- input sets it in the Off-Hook or Normal Mode. Any digits to be tested in the "On-Hook/Test" mode must be entered while "Off-Hook."

When Off-Hook, the MK50982 will accept key inputs and outpulse the digits in normal fashion. Upon completion of the last digit, the oscillator is disabled and the circuit stands by for additional inputs.

Switching the MK50982 to On-Hook while it is outpulsing causes the remaining digits to be outpulsed at 100 x the normal rate (M/B ratio is then 50/50). This feature provides a means of rapidly testing the device and is also an efficient method by which the circuitry is reset. When the outpulsing in this mode, which can take up to 300ms, is completed, the circuit is deactivated and will require only the current necessary to sustain the memory and Power-Up-Clear detect circuitry (refer to the electrical specifications).

Upon returning Off-Hook, if the first key entry is either * or #, the number sequence stored on-chip will be outpulsed. Any other valid entries will clear the memory and outpulse the new number sequence.

$\overline{\text{PULSE}}$ OUTPUT, Pin 16

The $\overline{\text{Pulse}}$ output is an open-drain N-Channel transistor designed to drive an external bipolar transistor. These transistors would normally be used to pulse the telephone line by controlling the loop current through the network. The timing characteristics of the $\overline{\text{Pulse}}$ output are shown in Figure 6.

TEST CIRCUIT

A test circuit is shown in Figure 4. This circuit can be used to demonstrate the basic operation of the MK50982.

TYPICAL APPLICATION

The schematic diagram in Figure 5 shows one method which can be used to interface the pulse dialer with the telephone line. In the approach shown, the pulse dialer circuitry is in series with the speech network.

A current source of some type is desired to present a high impedance to the telephone line while guaranteeing sufficient current to power the MK50982 ($\geq$ 150 μA). The current source shown is constructed with two components, Q2 and R1. The current is regulated by the negative feedback provided by R1 to the gate of Q2. Several other implementations can be considered, such as a constant current diode, or a configuration using bipolar transistors.

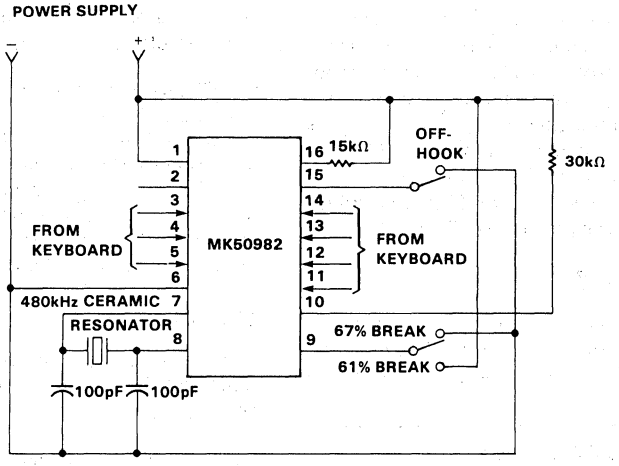
The purpose of transistor Q1 is to take the place of an additional hookswitch contact. When S1 closes, Q1 is turned on and On-Hook (pin 15) is pulled to V-. This sets the MK50982 in the normal mode, ready to accept key inputs.

When going On-Hook, S1 is opened, causing Q1 to be turned off. An on-chip resistor pulls pin 15 to V+ and the current source is disabled. The purpose of D1 is to limit any reverse current flow through the current source. A large-value resistor, R3, allows a small amount of current to maintain the memory on MK50982.

To return Off-Hook, S1 is closed, causing Q1 to be turned on thus tying the On-Hook pin to V-. The $\overline{\text{Pulse}}$ and $\overline{\text{Mute}}$ outputs drive external transistors to perform the outpulsing function. The receiver is connected through transistor Q6 to the speech network. $\overline{\text{Mute}}$ causes the transistor to be held on until outpulsing begins. When $\overline{\text{Mute}}$ switches low, the receiver is removed from the speech network. The pops caused by breaking the line are then isolated from the receiver. The $\overline{\text{Pulse}}$ output drives transistors Q3 and Q5 to make and break the line until the digit has been completely outpulsed. $\overline{\text{Mute}}$ then switches high, returning the receiver to the speech network.

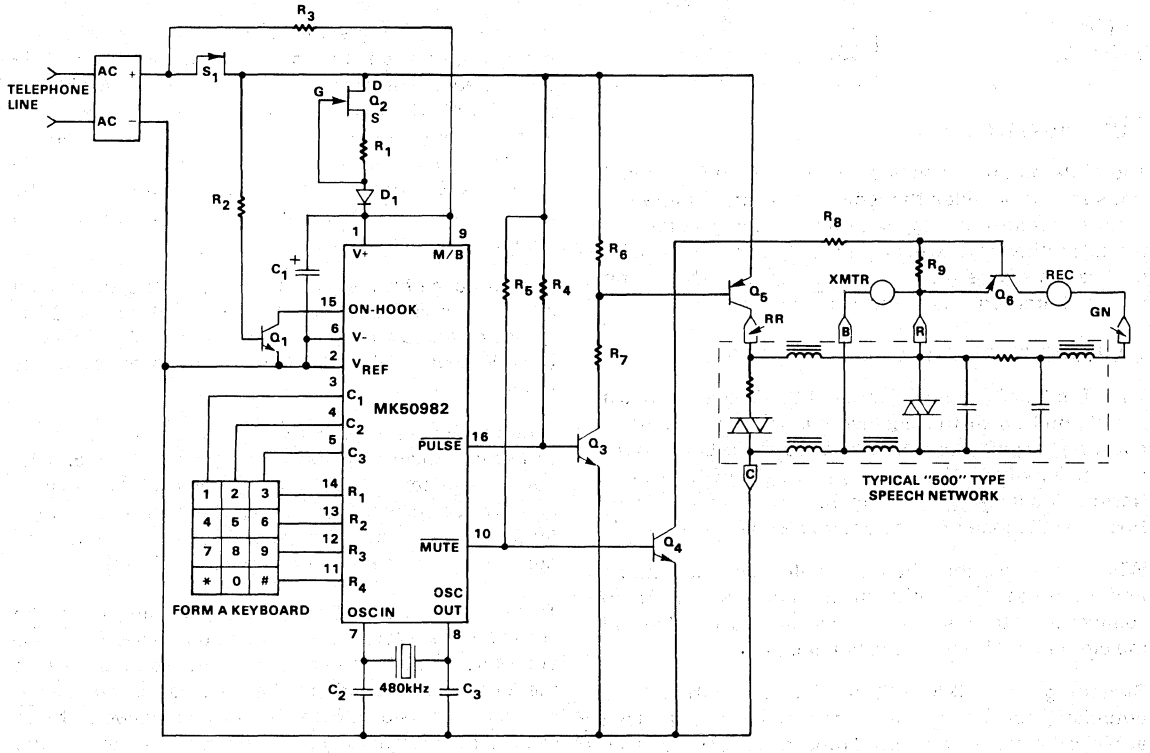
TEST CIRCUIT

Figure 4



TYPICAL APPLICATION

Figure 5



Q1, 3, 4 = 2N5550
Q5, 6 = 2N5401
Q2 = 2N3822

D1 = 1N914
C1 = 20μF (low leakage)
C2, 3 = 100pF ± 20%

R1 = 8kΩ
R2 = 500kΩ
R3 = 22MΩ

R4, 5 = 390kΩ
R6, 9 = 100kΩ
R7, 8 = 3kΩ

ABSOLUTE MAXIMUM RATINGS*

DC Supply Voltage, V+ ..... 6.2 Volts
Operating Temperature ..... -30°C to +60°C
Storage Temperature ..... -55°C to +85°C
Maximum Power Dissipation (25°C) 500mW
Maximum Voltage on any Pin ..... (V+) +0.3; (V-) -0.3 Volts

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($-30°C \leq T_A \leq 60°C$)

DC CHARACTERISTICS

SYM	PARAMETER: SPECIFIC CONDITIONS	MIN	TYP*	MAX	UNITS
$V+$	DC Supply Voltage	2.5		6.0	V
I_{MR}	Memory Retention Current: Note 1		0.7	2.5	μA
I_{OP}	DC Operating Current: Note 2		100	150	μA
V_{REF}	Magnitude of (V+ - V_{REF}): I_{SUPPLY} = 150 μA	1.5	2.5	3.5	V
I_M	Mute Sink Current: V+ = 2.5, V_O = 0.5V	0.5	2.0		mA
I_P	Pulse Sink Current: V+ = 2.5V, Vo = 0.5V	1.0	4.0		mA
I_{LKG}	Mute and Pulse Leakage: V+ = 6.0V, Vo = 6.0V		0.001	1.0	μA
R_{KI}	Keyboard Contact Resistance			1.0	kΩ
C_{KI}	Keyboard Capacitance			30	pF
K_{IL}	"0" Logic Level	V-		20% of V+	V
K_{IH}	"1" Logic Level	80% of V+		V+	V
K_{RU}	Keyboard Pull-Up Resistance: Note 3		4.0		kΩ
K_{RD}	Keyboard Pull-Down Resistance: Note 3		100		kΩ
R_{OH}	On-Hook Pull-Up Resistance		100		kΩ

NOTES
*Typical values are to be used as a design aid and are not subject to production testing.
1. Current necessary for memory to be maintained. All outputs unloaded. On-Hook mode.
2. Current required for proper circuit function. Off-Hook mode, Valid Key input, V_{REF} tied to V-.
3. Keyboard to be scanned at 500Hz when oscillator enabled. Row and Column to alternately pull high and low.

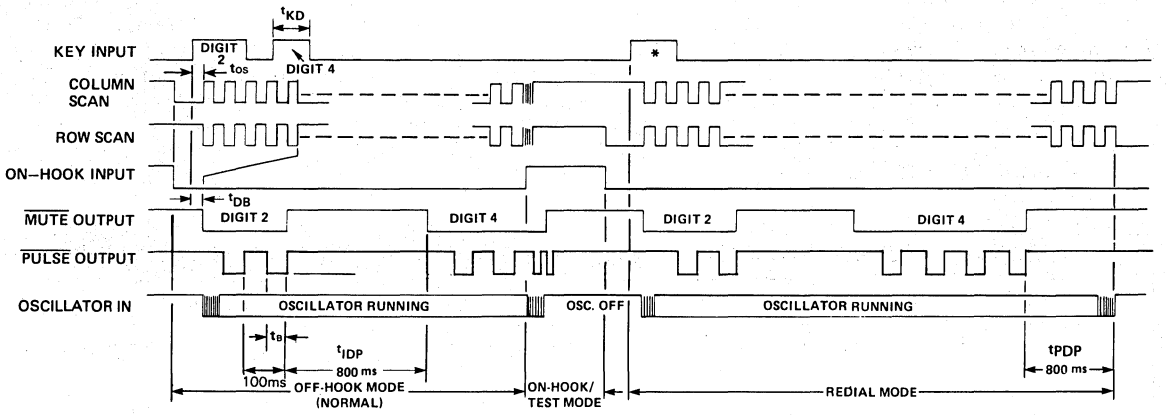
AC CHARACTERISTICS* (The timing Relationships are shown in Figure 6)

SYM	PARAMETER: SPECIFIC CONDITIONS	MIN	TYP	MAX	UNITS
f_{OSC}	Oscillator Frequency (antiresonant mode): Note 1		480		kHz
t_{DB}	Keyboard Debounce Time		10		ms
t_{KD}	Time for Valid Key Entry	40			ms
t_{OS}	Oscillator Start-Up Time		6.0		ms
P_R	Pulse Rate		10.0		pps
t_B	Break Time: Pin 9 Tied to V+/Tied to V-		61.0/67.0		ms
t_{IDP}	Interdigital Pause		800		ms

NOTES:
*Typical values are exact with a nominal 480 kHz frequence reference (except for oscillator start-up time).

Ceramic resonator should have the following equivalent values R <20Ω, $R_A \geq$ 70k Ω, Co ≤ 500pF.

TIMING CHARACTERISTICS
Figure 6



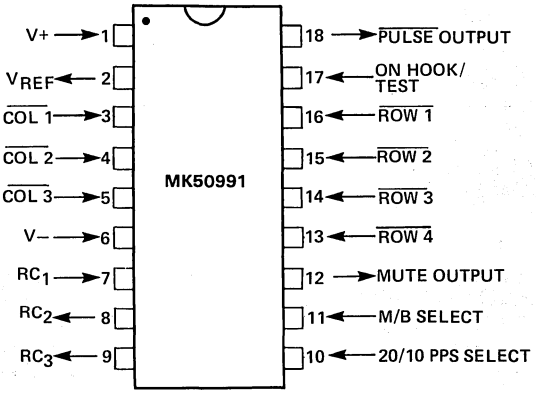
INTEGRATED PULSE DIALER WITH REDIAL

MK50991(N)

FEATURES

- Direct telephone-line operation
- CMOS technology is used for low-voltage, low-power operation
- Uses either a standard 2-of-7 matrix keyboard or the inexpensive Form A-type keyboard
- Inexpensive RC oscillator used as frequency reference
- Redial with either a * or # input
- Make/Break ratio and pulse rate are pin-selectable
- Provision for rapid testing
- On-chip voltage regulator
- Power-up-clear circuitry

PIN CONNECTIONS



DESCRIPTION

The MK50991 is a monolithic CMOS integrated circuit which converts keyboard inputs into pulse signal outputs simulating a rotary telephone dial. It is designed to operate directly from the telephone line and can be interfaced properly to meet telephone specifications in systems utilizing loop-disconnect signalling. Two outputs are provided to implement the pulse dialer function, one to pulse the line and another to mute the receiver. The mute output can be interfaced with a bistable latching relay in applications with this requirement.

The MK50991 is in either the on-hook or off-hook mode as determined by the input to the pin designated "On-Hook/Test." In order to accept any key inputs, the MK50991 must be in the off-hook state. Upon sensing a key input, the normally static oscillator is enabled and the row and column inputs are alternately strobed to verify that the keyboard input is valid. The decoded input is then entered into an on-chip memory. The memory will store up to 17 digits and allows keystrokes to be entered at rates comparable to tone dialing telephones. Entering the first digit (except * or #) clears the memory buffer and starts the outpulsing sequence. As additional digits are entered, they are stored in the memory and outpulsed in turn. The memory has a FIFO—(first-in-first-out) type architecture and more than 17 digits may be dialed in any number sequence. The limitation is that there can never be more than 17 digits remaining to be outpulsed.

The MK50991 also features the redial function. Any 17-digit number sequence may be redialed with a * or # key input, providing that the circuit enters the on-hook mode for a finite time, t_{OH} (refer to discussion on the On-Hook/Test pin).

An on-chip "Power-Up-Clear" circuit insures reliable operation of the MK50991. If the supply to the circuit should become insufficient to retain data in the memory (see electrical specifications), a "Power-Up-Clear" will occur upon regaining a proper supply level. This function will prevent the "Redial" or spontaneous outpulsing of incorrect data. A new number sequence may then be entered in normal fashion.

ABSOLUTE MAXIMUM RATINGS*

DC Supply Voltage, V+ ..... 6.2 Volts
Operating Temperature ..... -30°C to +60°C
Storage Temperature ..... -55°C to +85°C
Maximum Power Dissipation 25°C 500mW
Maximum Voltage on any Pin ..... (V+) + 0.3; (V–) – 0.3 Volts

*Stresses above these listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS

$-30°C \leq T_A \leq 60°C$

SYM	PARAMETER	MIN	TYP*	MAX	UNITS
V+	DC Operating Voltage	2.5		6.0	Volts
I_{MR}	Memory Retention Current: (Note 1)		0.7	2.5	μA
I_{OP}	DC Operating Current: (Note 2)		100	150	μA
V_{REF}	Magnitude of (V+ - V_{REF}): I_{supply} = 150μA	1.5	2.5	3.5	Volts
I_{ML}	Mute Sink Current: V+ = 2.5V, Vo = 0.5V	0.5	2.0		mA
I_{MH}	Mute Source Current: V+ = 2.5V, Vo = 2.0V	0.5	2.0		mA
I_P	Pulse Sink Current: V+ = 2.5V, Vo = 0.5V	1.0	4.0		mA
I_{LKG}	Mute and Pulse Leakage: V+ = 6.0V, Vo = 6.0V		0.001	1.0	μA
R_{KI}	Keyboard Contact Resistance			1.0	kΩ
C_{KI}	Keyboard Capacitance			30	pF
K_{IL}	Keyboard "0" Logic Level	V–		20% of V+	Volts
K_{IH}	Keyboard "1" Logic Level	80% of V+		V+	Volts
K_{RU}	Keyboard Pull-Up Resistance: (Note 3)		100		kΩ
K_{RD}	Keyboard Pull-Down Resistance: (Note 3)		4.0		kΩ
R_{OH}	On-Hook Pull-Up Resistance		100		kΩ

NOTES:

*Typical values are to be used as a design aid and are not subject to production testing.

1. Current necessary for memory to be maintained. All outputs unloaded. On-Hook mode. V_{REF} tied to V–.
2. Current required for proper circuit function. Off-Hook Mode. Valid key input, V_{REF} tied to V–.
3. Keyboard to be scanned at 500Hz when oscillator enabled. Row and Column to alternately pull high and low.

AC CHARACTERISTICS
(The Timing Relationships are shown in Figure 4)

SYM	PARAMETER	MIN	TYP	MAX	UNITS
f_{OSC}	Oscillator Frequency (Note 1)		4.0		kHz
Δf_{OSC1}	Frequency Stability: 2.5 to 3.5V (Note 2)		± 4		%
Δf_{OSC2}	Frequency Stability: 3.5 to 6.0V (Note 2)		± 4		%
Δf_{OSC3}	Frequency Stability: 150→500 μA (Note 3)		± 3		%
P_R	Pulse Rate: Pin 10 tied to V+/V-		20/10		pps
t_{DB}	Keyboard Debounce Time		10		ms
t_{KD}	Time for Valid Key Entry	40			ms
t_B	Break Time: Pin 9 tied to V+/ tied to V-		66.0/60.0		ms
t_{IDP}, t_{PDP}	Interdigital Pause, Predigital Pause (Note 4)		800+ t_M		ms
t_{MO}	Mute Overlap of Pulse		5		ms

NOTES:

"Typical" values are exact assuming a 4kHz frequency reference.

1. A change in the frequency will result in a proportional change in all circuit timing.
2. For stated voltages, the given "typical" Δf_{OSC} holds from part to part over the stated operating temperature range.
3. Using V_{REF} in conjunction with a current source results in the given "typical" Δf_{OSC} from part to part over the stated operating temperature and current.
4. Time from last break to next break, t_M = 100ms-t_B = make time.

Functions of the individual pins are described below:

V+, Pin 1

This is the positive supply input to the part and is measured relative to V- (pin 6). The voltage on this pin must be regulated to less than 6 volts using either the on-chip reference circuitry or an external form of regulation.

V_{REF}, Pin 2

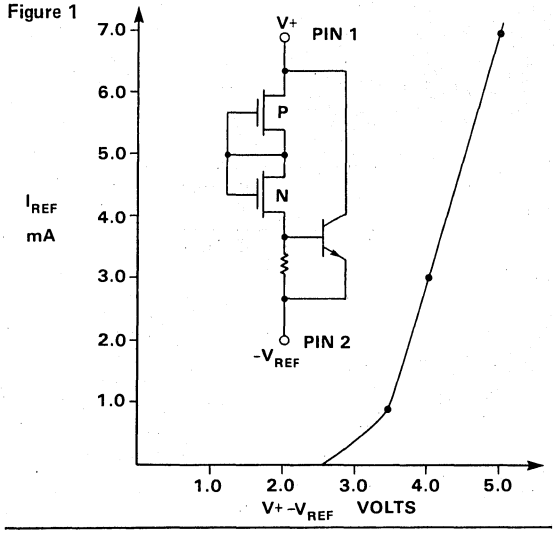
The V_{REF} output provides a negative reference voltage relative to the V+ supply. Its magnitude is a function of the internal parameters which define the minimum operating voltage of each part. In a typical application, as shown in Figure 5, the V_{REF} pin is simply tied to V-(Pin 6). The internal circuit with its associated I-V characteristic is shown in Figure 1.

KEYBOARD INPUTS, Pins 3, 4, 5, 13, 14, 15, 16

The MK50991 incorporates an innovative keyboard

V_{REF} TYPICAL I–V CHARACTERISTICS

Figure 1



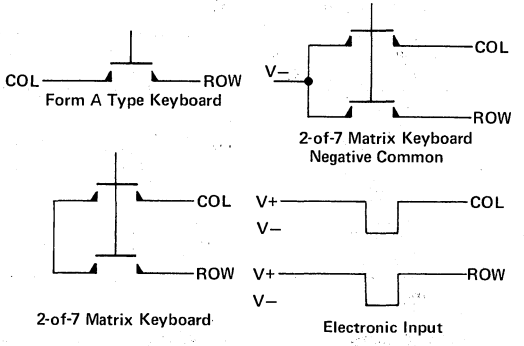
scheme that allows either the standard 2-of-7 keyboard with positive common or the inexpensive single contact (Form A) keyboard to be used.

A valid key entry is defined by either a single row being connected to a single column or V- being simultaneously presented to both a single row and column.

When in the On-Hook mode, the row and column inputs are held high and no keyboard inputs are accepted. When Off-Hook, the keyboard is completely static until the initial valid key input is sensed. The oscillator is then enabled and the rows and columns are alternately scanned (pulled high, then low) to verify the input is valid. The input must remain valid continuously for 10 ms of debounce time to be accepted.

KEYBOARD CONFIGURATIONS

Figure 2



RC OSCILLATOR, Pins 7, 8, 9

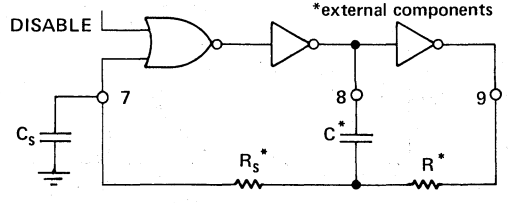
The MK50991 contains on-chip inverters to provide an oscillator which will operate with a minimum of external components. Figure 3 shows the on-chip configuration with the necessary external components. Optimum stability occurs with the ratio $K = R_S/R$ equal to 10. The oscillator period is given by:

$$T = RC \left[1.386 + \frac{3.5KCs}{C} - \frac{2K}{K+1} \ln \left(\frac{K}{1.5K + 0.5} \right) \right]$$

where C_S is the stray capacitance on Pin 7. Accuracy and stability will be enhanced with the capacitance minimized.

OSCILLATOR CONFIGURATION

Figure 3



20/10 PPS SELECT, Pin 10

Tying this input to either V+ (Pin 1) or V- (Pin 6) will select a pulse rate of either 20 or 10 pps respectively.

MAKE/BREAK SELECT, Pin 11

The Make/Break ratio may be selected by connecting the pin to either the V+ or V- supply. The table below indicates the two popular ratios from which the user can choose.

MAKE/BREAK RATIO SELECTION

Table 1

INPUT TO MAKE/BREAK PIN	PULSE OUTPUT	
	MAKE	BREAK
V+ (Pin 1)	34%	66%
V– (Pin 6)	40%	60%

MUTE OUTPUT, Pin 12

The Mute output consists of a complementary pair of CMOS transistors. It provides the logic necessary to be interfaced with a bistable latching relay to Mute the speech network. Upon coming off-hook, a negative transition on Mute will insure the speech network is properly connected to the telephone line. When outpulsing begins, a positive transition will switch the relay, continuously muting the network until the entire number sequence entered is outpulsed. Figure 4 shows, in detail, the timing diagram of the Mute Output.

ON-HOOK/TEST, Pin 17

The "Test" or "On-Hook" input of the MK50991 has a 100kΩ pull-up to the positive supply. A V+ input or allowing the pin to float sets the circuit in its On-Hook or test mode while a V- input sets it in the Off-Hook or Normal Mode.

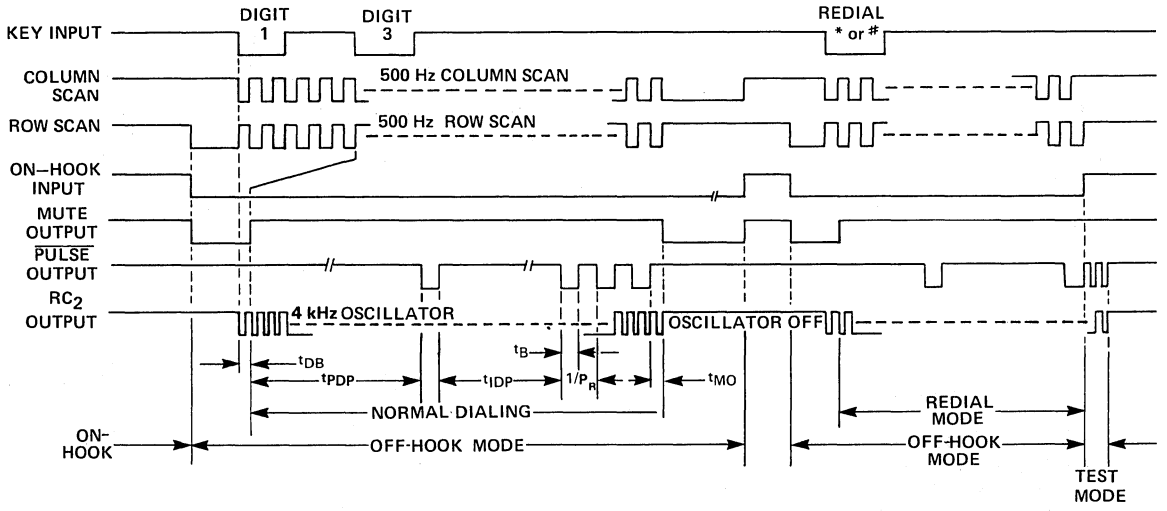
When Off-Hook, the MK50991 will accept key inputs and outpulse the digits in normal fashion. Upon completion of the last digit, the oscillator is disabled and the circuit stands by for additional inputs.

Switching the MK50991 to On-Hook while it is outpulsing causes the remainingdigits to be outpulsed at 100 x the normal rate (M/B ratio is then 50/50). This feature provides a means of rapidly testing the device and is also an efficient method by which the circuitry is reset. When the outpulsing in this mode, which can take up to 300ms, is completed, the circuit is deactivated and will require only the current necessary to sustain the memory and Power-Up-Clear detect circuitry (refer to the electrical specifications).

Upon returning Off-Hook, a negative transistion on the Mute Output will insure the speech network is connected to the line. If the first key entry is either a * or #, the number sequence stored on-chip will be outpulsed. Any other valid key entries will clear the memory and outpulse the new number sequence.

TIMING CHARACTERISTICS

Figure 4



PULSE OUTPUT, Pin 18

The Pulse Output consists of an open-drain N-channel transistor. This output provides the logic necessary to pulse the telephone line with the correct Make/Break, pulse rate, and interdigital pause timings. The timing characteristic of the Pulse Output is shown in Figure 4 above.

TYPICAL APPLICATION

The schematic diagram in Figure 5 shows one method which can be used to interface the MK50991 with the telephone line. In this approach, the speech network is connected directly to the telephone line through a metallic relay contact. The pulse signalling circuitry is in parallel with the speech network.

A current source of some type is desired to present a high impedance to the telephone line while guaranteeing sufficient current to power the MK50991 (>150μA). Transistor Q_2 provides the source current to the device. The magnitude of this current is determined by the voltage on R_1 due to the forward-biased diodes D_1 and D_2. Transistor Q_1 provides a regulated bias current to the diodes as well as Q_2.

When in the On-Hook mode, S_1 and S_2 are open. The current source is disabled in this manner and only a small amount of current, supplied through R_3, is needed to maintain data in the memory. The relay is open, thereby disconnecting the speech network from the telephone line.

When coming Off-Hook, switches S1 and S_2 close, connecting the On-Hook input to V–. Immediately the output of Mute switches low. This transition pulses the relay through Q_5 and Q_6, latching it in the closed position. The speech network is now attached directly to the telephone line for normal conversation. Diode D3 will hold the pulsing Darlington composed of transistors Q_3 and Q_4 off.

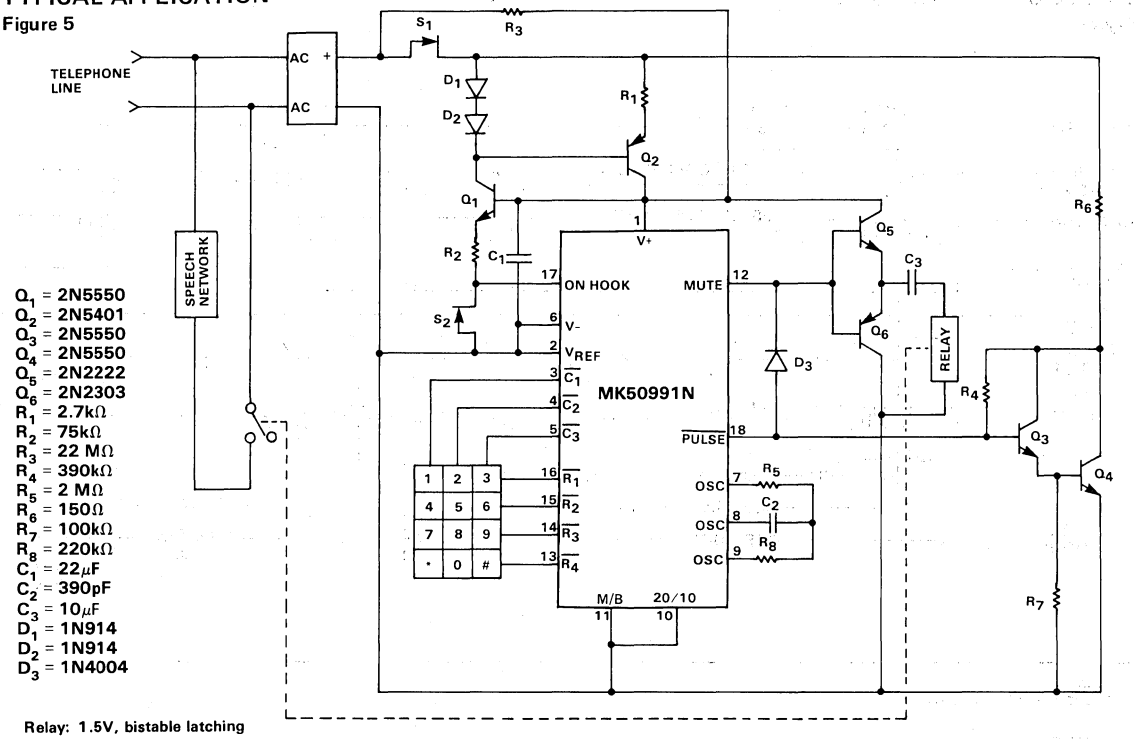
Upon receiving a valid key entry, Mute switches high. This transition pulses the relay to its open state, thereby muting the network. The loop current is still passed through the Darlington pair, Q_3 and Q_4, for a predigital pause time of approximately 840ms. (t_{PDP}). Break is accomplished when the Pulse output switches low, cutting the Darlington off. During break, current flow is limited to the current source and the Pulse pullup resistor R_4, insuring a high impedence in this interval. Pulsing of the complete digit continues in this manner. Each digit in the number sequence dialed is separated by standard interdigital pauses (t_{IDP}).

After the final digit is outpulsed, the Mute Output returns low and the speech network is connected back to the telephone line through the relay contact for normal conversation. Returning On-Hook causes Mute to switch high, removing the network from the line.

Applications which do not require operation with a bistable relay may use our MK50981 pulse dialer to better advantage.

TYPICAL APPLICATION

Figure 5

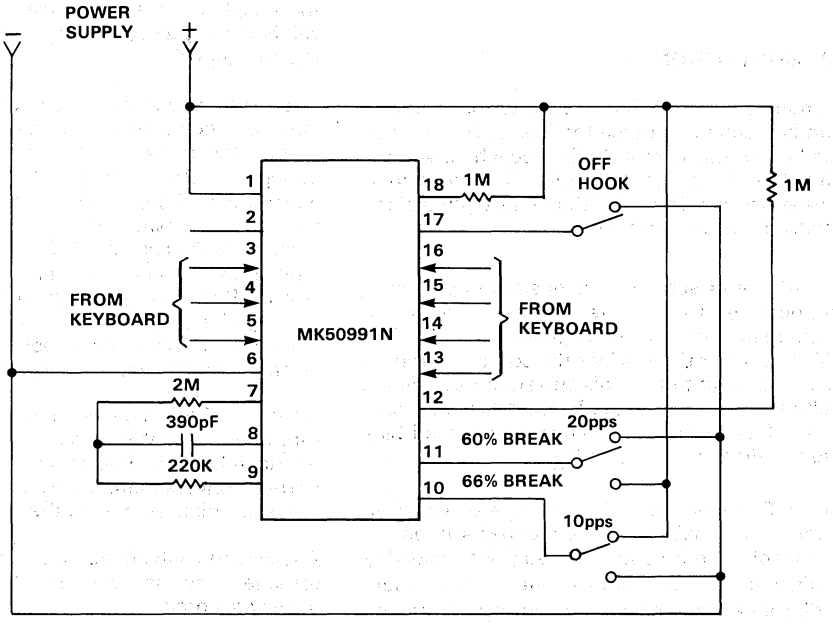


Q_1 = 2N5550
Q_2 = 2N5401
Q_3 = 2N5550
Q_4 = 2N5550
Q_5 = 2N2222
Q_6 = 2N2303
R_1 = 2.7kΩ
R_2 = 75kΩ
R_3 = 22 MΩ
R_4 = 390kΩ
R_5 = 2 MΩ
R_6 = 150Ω
R_7 = 100kΩ
R_8 = 220kΩ
C_1 = 22μF
C_2 = 390pF
C_3 = 10μF
D_1 = 1N914
D_2 = 1N914
D_3 = 1N4004

Relay: 1.5V, bistable latching

TEST CIRCUIT

Figure 6



MOSTEK®

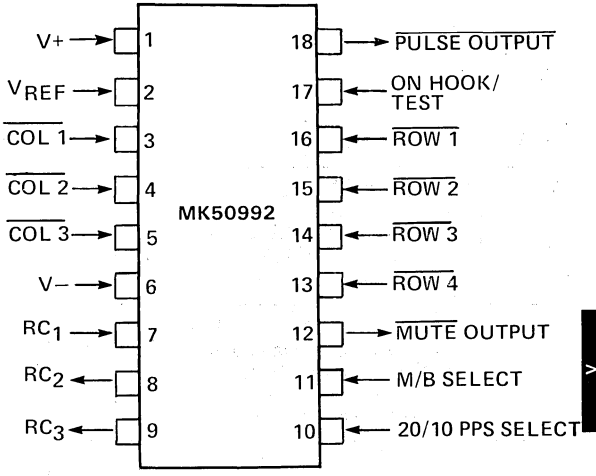
INTEGRATED PULSE DIALER WITH REDIAL

MK50992(N)

FEATURES

- Direct Telephone Line Operation
- Uses standard 2-of-7 matrix with neg. true common or the inexpensive Form A-type keyboard
- CMOS Technology for Low-Voltage, Low-Power Operation
- Supply Voltage Range 2.5 to 6 volts
- MAKE/BREAK Ratio Pin-Selectable
- 20/10 pps Pin-selectable
- Redial with # or *
- Continuous Mute
- Inexpensive RC Oscillator

PIN CONNECTIONS



DESCRIPTION

The MK50992 is a monolithic CMOS integrated circuit which uses an inexpensive RC oscillator for its frequency reference and provides all the features required for implementing a pulse dialer with redial. It operates directly off the telephone line supply and converts 2-of-7 keyboard inputs into pulse signals simulating a rotary telephone dial. When not outpulsing, the MK50992 consumes only micro-amperes of current.

When off-hook, the MK50992 senses a key down condition, verifies that only one key is depressed and then enters the key's code into an on-chip memory.

The memory will store up to 17 digits, and allows keystrokes to be entered at rates comparable to tone dialing telephones. Entering the first digit starts a predigital pause counter and clears the memory buffer. At the end of the predigital pause, outpulsing begins. As digits are entered during the outpulsing period they will also be stored in the memory. Outpulsing will continue until all entered digits have been dialed. The first 17 digits entered will be stored in the on-chip redial memory and can be redialed by pressing either # or *, provided that the receiver has gone on-hook for the minimum t_{OH} (refer to the electrical specifications section).

When on-hook, key inputs will not be recognized because the oscillator is disabled. This oscillator inhibit prevents the circuit from drawing excessive current when on-hook.

ABSOLUTE MAXIMUM RATINGS*

DC Supply Voltage, V+ ..... 6.2 Volts
Operating Temperature ..... -30° to +60°C
Storage Temperature ..... -55°C to +85°C
Maximum Power Dissipation @ 25°C 500mW
Maximum Voltage on any Pin Relative to V- ..... -0.3 Volts
Maximum Voltage on any Pin Relative to V+ ..... +0.3 Volts

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

$-30°C \leq T_A \leq 60°C$

DC CHARACTERISTICS

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V+	DC Supply Voltage	2.5		6.0	V	
R_{KI} C_{KI}	Key Input (R1 - 4R, C1 - C3) Contact Resistance Keyboard Capacitance			1 30	kΩ pF	
K_{IL} K_{IH}	Key Input Level (R1 - R4, C1 - C3) 2-of-7 input mode and all electronic switching	V- 80% of V+		20% of V+ V+	V V	
K_{IRU}	Keyboard Pull-Up Resistance		100		kΩ	
K_{IRD}	Keyboard Pull-Down Resistance		4.0		kΩ	
I_M	Mute Sink Current @ V_O = 0.5V, V+ = 2.5V	500			μA	
I_P	Pulse Output Sink Current @ V_O = 0.5V, V+ = 2.5V	1.0			mA	
I_{MR}	Memory Retention Current		0.7	2.5	μA	7
I_{OP}	Operating Current		100	150	μA	1
I_{LKG}	Mute or Pulse Off Leakage V+ = 6.0V V_O = 6.0V		.001	1	μA	
I_{REF}	V_{REF} Output Source Current (V_{REF} = -6.0V REF to V+)	1	7		mA	8

Functions of the individual pins are described below.

V+ (Pin 1)

This is the positive supply pin. The voltage on this pin is measured relative to V- and is supplied from a 150 μA current source. This voltage must be regulated to less than 6.0 volts.

V_{REF} (Pin 2)

The V_{REF} output provides a reference voltage that tracks internal parameters of the MK50992. V_{REF} provides a negative voltage reference to the V+ supply. Its magnitude will be approximately 0.6 volt greater than the minimum operating voltage of each particular MK50992.

The typical application would be to connect the V_{REF} pin to the V-pin (Pin 6). The supply to the V+ pin (Pin 1) should then be regulated to 150μA (I_{OP} max). With this amount of supply current, operation of the MK50992 is guaranteed.

The internal circuit of the V_{REF} function is shown in Figure 1 with its associated I-V characteristic.

AC CHARACTERISTICS

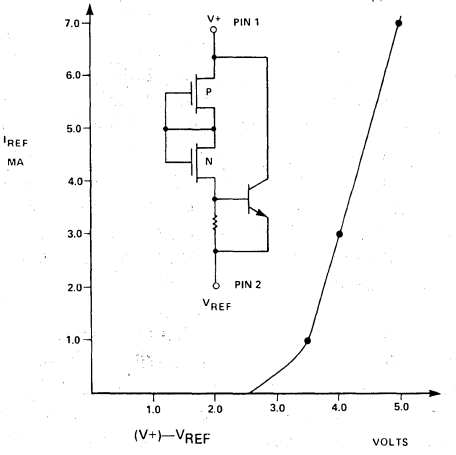
SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
F_{OSC}	Oscillator Frequency		4		kHz	4
t_{DB}	Key Input Debounce Time		10		ms	3,6
t_{KD}	Key Down time for Valid Entry	40			ms	2,3
t_{KR}	Key Down Time During Two-Key Roll Over	5			ms	3
t_{OS}	Oscillator Start-Up Time (V+ = 2.5V)		1		ms	
t_{MO}	Mute Valid After Last Outpulse		5		ms	3,6
P_R	Pulse Output Pulse Rate		10		pps	5
t_{OH}	On-Hook Time Required to Clear Memory	300			ms	3
t_{PDP}	Pre-Digital pause		800		ms	3,6
t_{IDP}	Inter-Digital Pause		800		ms	3,6
Δf	Frequency Stability (2.5V - 3.5V)		±4		%	
Δf	Frequency Stability (3.5V - 6.0V)		±4		%	
Δf	Frequency Stability (with V_{REF} used) (I_{REF} = 250μA - 500μA)		±2.5		%	

NOTES:

1. Output and V_{REF} unloaded.
2. Debounce plus oscillator startup time ≤ 40ms.
3. These times are directly proportional to the oscillator frequency.
4. R_S = 2MΩ, R = 220KΩ, C = 390pF. See oscillator paragraph.
5. If pin 10 is tied to V+, the Pulse Output Pulse Rate will be 20pps.
6. If the 20pps option is selected, the time will be ½ these shown.
7. Current necessary for memory to be maintained. All outputs unloaded.
8. Refer to Figure 1

V_{REF} TYPICAL I-V CHARACTERISTICS

Figure 1



KEYBOARD INPUTS (Pins 3, 4, 5, 13, 14, 15, 16)

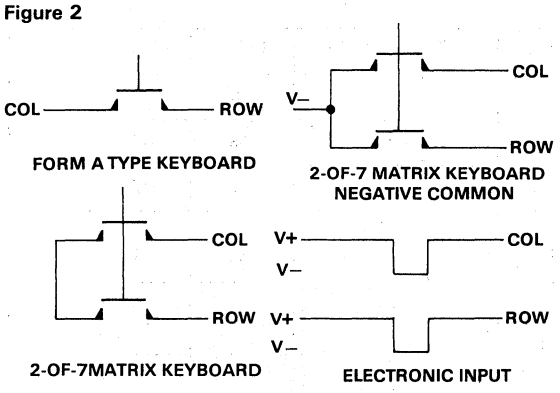
The MK50992 incorporates an innovative keyboard scheme that allows either the standard 2-of-7 keyboard with negative common or the inexpensive single contact (Form A) keyboard to be used.

A valid key entry is defined by either a single row being connected to a single column or V- being simultaneously presented to both a single row and column.

When in the On-Hook mode, the row and column inputs are held high and no keyboard inputs are accepted. When Off-Hook, the keyboard is completely static until the initial valid key input is sensed. The oscillator is then enabled and the rows and columns are alternately scanned (pulled high, then low) to verify the input is valid. The input must remain valid continuously for 10ms of debounce time to be accepted.

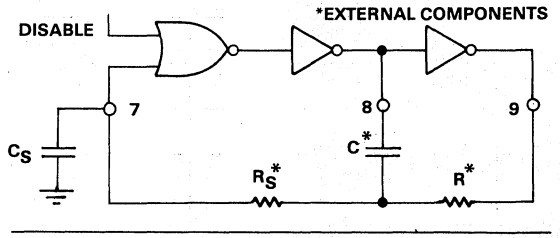
KEYBOARD CONFIGURATIONS

Figure 2



OSCILLATOR CONFIGURATION

Figure 3



OSCILLATOR (Pins 7, 8, 9)

The MK50992 contains on-chip inverters to provide an oscillator which will operate with a minimum of external components. Figure 3 shows the on-chip configuration with the necessary external components. Optimum stability occurs with the ratio $K = R_S/R$ equal to 10. The oscillator period is given by:

$$T=RC[1.386+(3.5KCs)/C-(2K/(K+1))\ln(K/(1.5K+0.5))]$$

where C_S is the stray capacitance on Pin 7. Accuracy and stability will be enhanced with this capacitance minimized.

V- (Pin 6)

This is the negative supply pin and is normally tied to V_{REF} (see V_{REF} paragraph).

20/10 PPS (Pin 10)

Tying this pin to V- will select an Output Pulse Rate of 10pps. Tying the pin to V+ will select an Output Pulse Rate of 20pps.

MAKE/BREAK (Pin 11)

The MAKE/BREAK pin controls the MAKE/BREAK ratio of the pulse output. The MAKE/BREAK ratio is controlled by connecting V+ or V- to this pin as shown in the following table.

MAKE/BREAK RATIO SELECTION

Table 1

Input To Make/Break Pin	Pulse Output	
	Make	Break
V+ (Pin 1)	34%	66%
V- (Pin 6)	40%	60%

$\overline{\text{MUTE}}$ OUTPUT (Pin 12)

The $\overline{\text{Mute}}$ output is an open-drain N-channel transistor designed to drive an external bipolar transistor. This circuitry is usually used to mute the receiver during outpulsing.

As shown in Figure 4, the MK50992 $\overline{\text{Mute}}$ output turns on (pulls to the V- supply) at the beginning of the predigital pause and turns off (goes to an open circuit) following the last break. The delay from the end of the last break until the $\overline{\text{Mute}}$ output turns off is mute overlap and is specified as t_{MO}.

TEST/ON HOOK (Pin 17)

The "Test" or "On-Hook" input of the MK50992 has a 100kΩ pull-up to the positive supply. A V+ input or allowing the pin to float sets the circuit in its On-Hook or test mode while a V- input sets it in the Off-Hook or Normal Mode.

When Off-Hook, the MK50992 will accept key inputs and outpulse the digits in normal fashion. Upon completion of the last digit, the oscillator is disabled and the circuit stands by for additional inputs.

Switching the MK50992 to On-Hook while it is outpulsing causes the remaining digits to be outpulsed at 100 x the normal rate (M/B ratio is then 50/50). This feature provides a means of rapidly testing the device and is also an efficient method by which the circuitry is reset. When the outpulsing in this mode, which can take up to 300ms, is completed, the circuit is deactivated and will require only the current necessary to sustain the memory and Power-Up-Clear detect circuitry (refer to the electrical specifications).

Upon returning Off-Hook, a negative transistion on the Mute Output will insure the speech network is connected to the line. If the first key entry is either a * or #, the number sequence stored on-chip will be outpulsed. Any other valid key entries will clear the memory and outpulse the new number sequence.

$\overline{\text{PULSE}}$ OUTPUT (Pin 18)

The $\overline{\text{Pulse}}$ output is an open drain N-channel tranistor designed to drive an external bipolar transistor. These transistors would normally be used to pulse the telephone line by disconnecting and connecting the network.

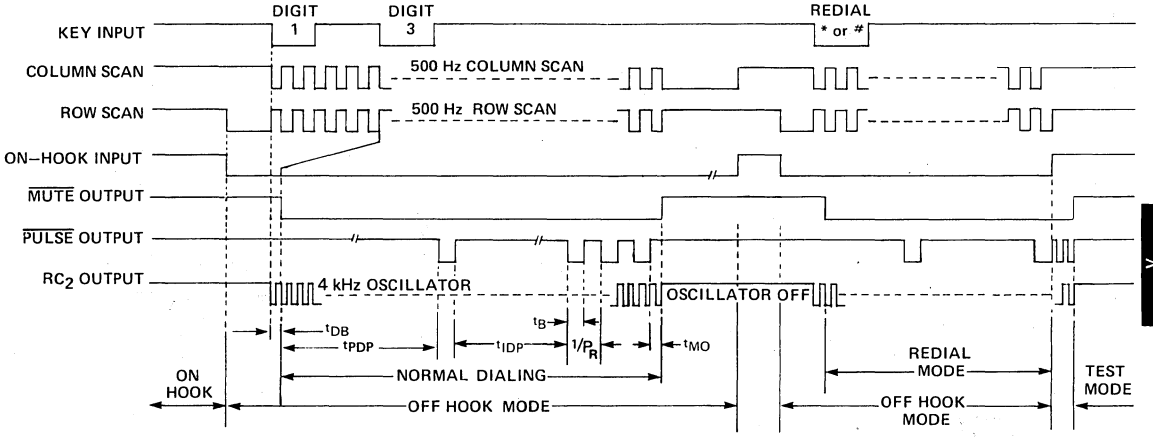
The MK50992 $\overline{\text{Pulse}}$ output is an open circuit during make and pulls to the V- supply during break.

As shown in Figure 4, outpulsing starts with a make before break.

A typical application is shown in Figure 6. This circuit will produce the timing shown in Figure 4.

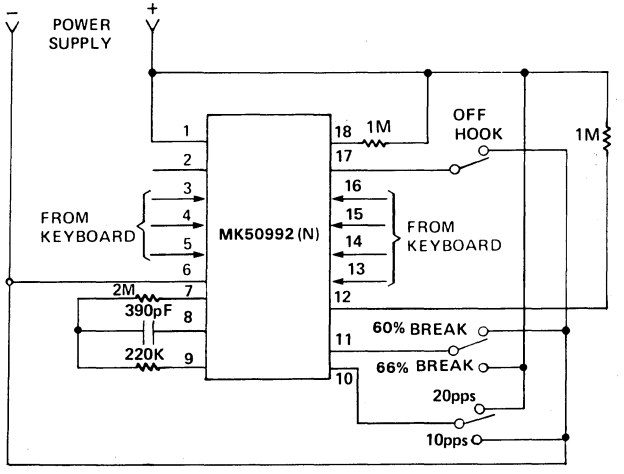
TIMING CHARACTERISTICS

Figure 4



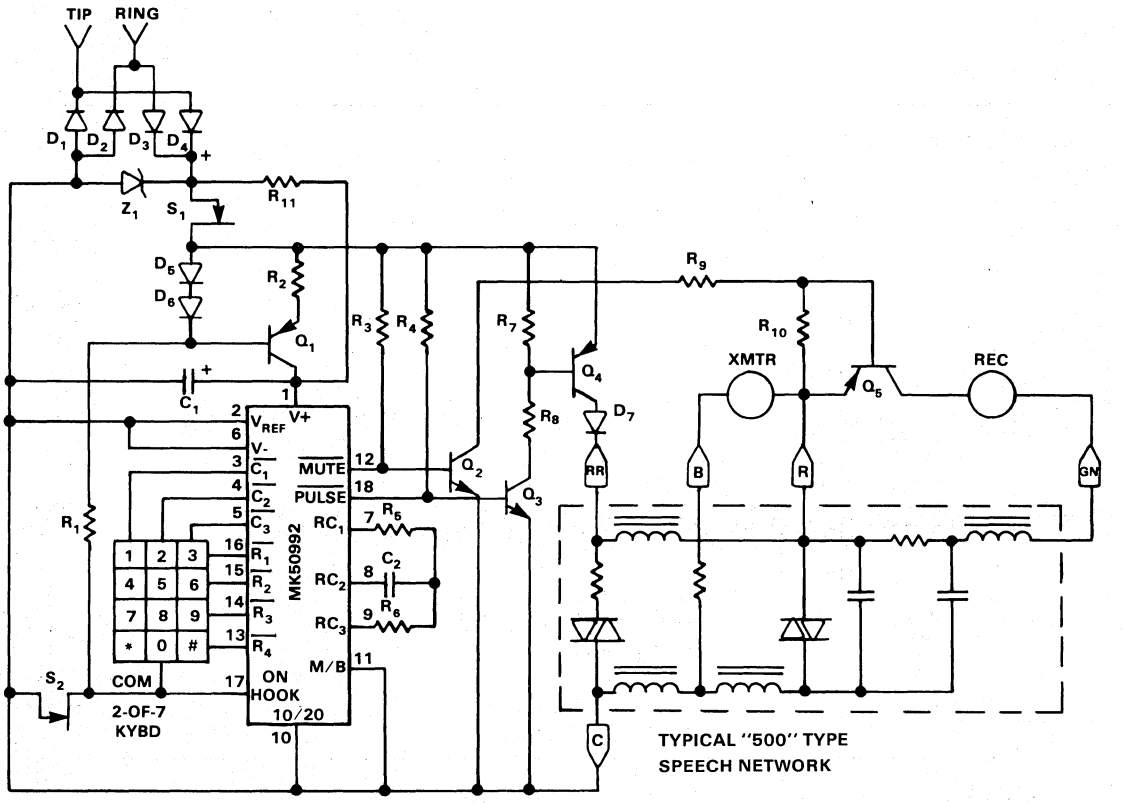
TEST CIRCUIT

Figure 5



TYPICAL APPLICATION

Figure 6



R1 = 560kΩ
R2 = 1.4kΩ
R3 = 470kΩ
R4 = 330kΩ
R5 = 2MΩ
R6 = 220kΩ

R7 = 100kΩ
R8 = 3kΩ
R9 = 3kΩ
R10 = 100kΩ
R11 = 10MΩ

Q1 = 2N5401
Q2 = 2N5550
Q3 = 2N5550
Q4 = 2N5401
Q5 = 2N5401

D1 = IN4004
D2 = IN4004
D3 = IN4004
D4 = IN4004
D5 = IN914
D6 = IN914
D7 = IN4004

C1 = 68μF (Low Leakage)
C2 = 390pF
S1 = HOOK SWITCH
S2 = HOOK SWITCH
Z1 = 120-volt, 1-watt zener

MOSTEK®

TELECOMMUNICATION PRODUCTS

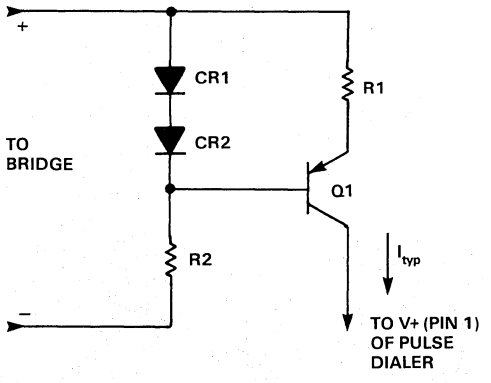
Current Sources

The purpose of this application brief is to discuss the use of constant current sources in pulse-dialer application circuits. Current sources serve two important purposes in pulse-dialer applications. First, they provide a relatively constant current to the pulse dialer so that it may operate consistently during pulsing. Secondly, constant current sources help maintain the high break impedance that is required by U.S. telephone specifications for loop disconnect dialers.

There are various configurations of current sources which can be used to achieve these goals. In this application brief, three different configurations will be examined. All of these current sources are interchangeable.

One of the most commonly used configurations consists of two diodes, one transistor, and two resistors. This configuration is used in the MK50992 typical application. A schematic of this current source is shown in Figure 1.

Figure 1



The operation of this type of current source is as follows. Diodes CR1 and CR2 ensure that the base of transistor Q1 is biased at two diode drops below the voltage at the positive side of the bridge. Resistor R2 provides bias current for diodes CR1 and CR2 and transistor Q1. R2 must be carefully selected to bias CR1 and CR2 past the knee of the current-voltage curve, yet still satisfy break impedance requirements. The emitter-to-base voltage of Q1 is approximately equal to one diode drop ($V_{CR} \approx 0.4$ - 0.7 V). Therefore, the voltage drop across R1 is also approximately equal to one diode drop. The current through Q1 is determined by the value of R1 according to the equation:

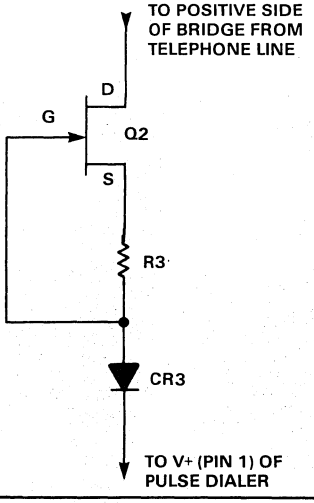
$$I_{typ} \approx \frac{V_{CR1}}{R1}$$

For a typical pulse-dialer application, the following components are recommended:

Q1 = 2N5401
CR1 = CR2 = 1N914
R1 = 1.5 kΩ
R2 = 560 kΩ

Another frequently used current source configuration consists of an N-channel JFET, one resistor, and one diode. This configuration is used in the MK50982 typical application circuit and is shown in Figure 2.

Figure 2



With this type of configuration, the value of resistor R3 and the characteristics of transistor Q2 determine the amount of current that flows to the pulse dialer. As current through R3 increases, the voltage across it (which corresponds to V_{GS} of the FET) also increases, thus regulating the amount of current that flows through Q2.

Diode CR3 is used to block reverse-current flow through the current source to the pulse dialer.

For a typical pulse-dialer application, the recommended components are:

Q2 = 2N3822
R3 = 12 kΩ
CR3 = 1N914

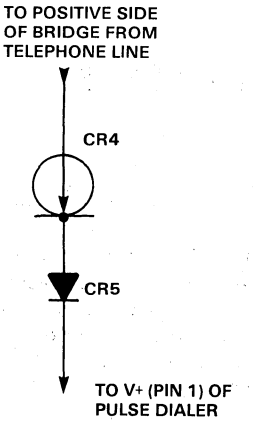
This current source scheme can also be constructed using different types of FETs. The position of R3 will depend upon the type of FET selected.

This type of current source has two main disadvantages over the type shown in Figure 1. The first disadvantage is cost. The FET selected must have a V_{DS} high enough to withstand open-circuit, telephone-line voltage (100 V max), and will be more expensive than a comparable bipolar transistor. The second disadvantage is poor stability. The current that flows through Q2 will vary with changes in the V_P (pinch-off voltage) of the FET. Careful selection of the FET used for Q2 and the tolerance of R3 will decrease the variability of this current source.

A third type of current source in common use is the constant current or regulator diode. This type of current source configuration is shown in Figure 3.

The constant current diode is composed of a transistor similar to the one shown in Figure 2, but with a built-in resistor and feedback loop. These constant current diodes operate according to the same principles as the current source shown in Figure 2.

Figure 3



For this type of current source configuration, the recommended silicon diode (CR5) is a 1N914. A germanium diode, such as the 1N270, may be used for CR3 and CR5 in Figures 2 and 3 respectively if a smaller voltage drop across the current source is desired. This will enable the pulse dialer to operate with a slightly lower voltage present at the telephone line. The constant current diode (CR4) can be any commercially available regulator diode such as the Siliconix CR022, the Siliconix J522, or the Teledyne TCR500. Any constant current diode can be used as long as it provides the minimum current required for operation of the selected Mostek dialer.

Pulse Dialer Comparison

The purpose of this Application Brief is to define the major differences between Mostek's pulse dialers.

The first Mostek pulse dialers were the MK5098 and the MK5099. Later, the MK50981 and MK50991 were developed to meet other requirements which the MK5098 and MK5099 did not meet. However, these are not direct replacements for the MK5098 and MK5099. Therefore, the improved MK50982 and MK50992 were designed to directly replace the MK5098 and MK5099, respectively. All of Mostek's pulse dialers, except the MK5098, have the last-number-redial feature.

The following is a comparison of all of the major differences between Mostek pulse dialers.

KEYBOARD TYPE

- MK5098/981/982 - Class A or 2-of-7 (K/B common floating or tied to V+)
- MK5099 - 2-of-7 (K/B common tied to V–)
- MK50991/992 - Class A or 2-of-7 (K/B common floating or tied to V–)

MEMORY RETENTION CURRENT

- MK5098 - Does not have last-number redial: $I_{SS} \leq 15$ μA at 2.5 V
- MK5099 - ≤ 20 μA at 2.5 V
- MK50981/982/991/992 - 0.7 μA typical and 2.5 μA maximum

OSCILLATOR

- MK5098/981/982 - 480 kHz Ceramic Resonator (anti-resonant mode) plus two 100 pF capacitors
- MK5099/991/992 - RC Oscillator consisting of 2 resistors and one capacitor

PIN-SELECTABLE OPTIONS

- Make/Break Ratio

  MK5098/981/982 - Pin 9 tied to V+ = 39%/61%
  Pin 9 tied to V– = 33%/67%

  MK5099 - Pin 11 tied to V+ = 39%/61%
  Pin 11 tied to V– = 33%/67%

  MK50991/992 - Pin 11 tied to V+ = 34%/66%
  Pin 11 tied to V– = 40%/60%

- Pulse Rate
  MK5098/981/982 - 10 pps
  MK5099/991/992 - Pin 10 tied to V+ = 20 pps
  Pin 10 tied to V– = 10 pps

OUTPUT LOGIC LEVELS

- Pulse

  MK5098/982/99/991/992 - $\overline{\text{Pulse}}$ output (active low, 0 - true output level)

  MK50981 - Pulse output (active high, 1 - true output level)

- Mute

  MK5098/981/982/99/992 - $\overline{\text{Mute}}$ output (active low, 0 - true output level)

  MK50991 - Mute output (active high, 1 - true output level)

TYPICAL APPLICATION

- MK5098/982/99/992 - The mute and pulse outputs of these pulse dialers have logic levels and timing characteristics such that they are easily used in applications requiring pulsing in series with the speech network.
- MK50981/991 - The mute and pulse outputs of these pulse dialers have logic levels and timing characteristics that make them more suitable for use in applications requiring pulsing in parallel with the speech network. The mute output of the MK50991 provides the logic necessary for interface with a bistable latching relay to mute the speech network.

1982 TELECOMMUNICATION PRODUCTS DATA BOOK

MOSTEK®

REPERTORY DIALER

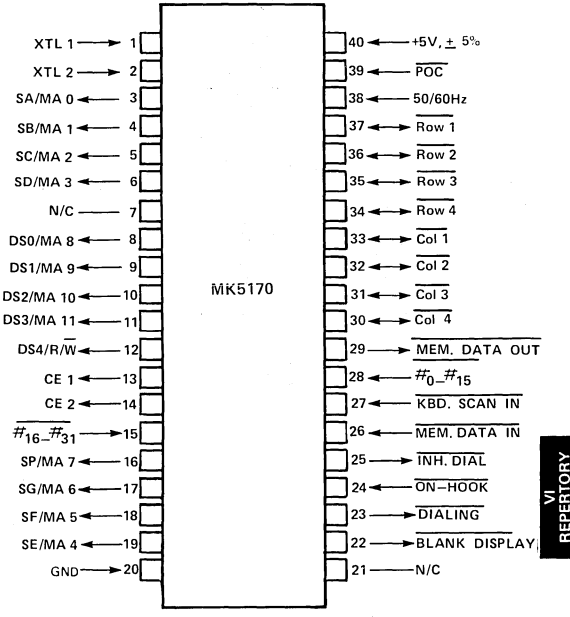
MK5170

FEATURES

- ☐ Repertory of 10, 24, 50, or 100 20-digit call numbers
- ☐ Repertory size determined automatically by the amount of memory installed
- ☐ Speed dialing of the desired call number
- ☐ Repertory easily updated by user
- ☐ Each call number has an associated address code. Display drive is provided to display the address code and the 20-digit call number
- ☐ When a phone number is manually dialed, the digits will be displayed as they are entered
- ☐ Any number in the repertory can be displayed
- ☐ The last number dialed is retained in an internal dial buffer for redialing
- ☐ Single-button dialing, with up to 32 numbers in two 16-number groups
- ☐ Controls either a tone dialer or a pulse dialer
- ☐ On-chip segment encoding
- ☐ Will interface 2102 or MK4104 static memory
- ☐ Digital real-time, 12/24-hour, 50/60 Hz clock
- ☐ 100-hour timer
- ☐ Two keyboard options
- ☐ Operates on an inexpensive TV color-burst crystal
- ☐ Single +5 volt ± 5% power supply

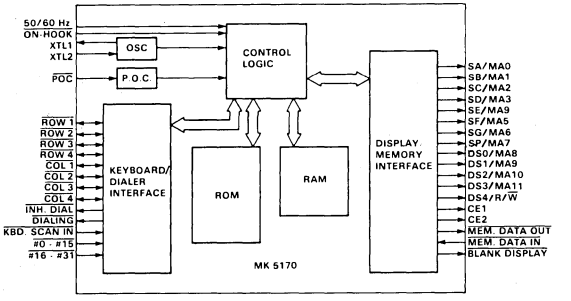
PIN CONNECTIONS

Figure 1



BLOCK DIAGRAM

Figure 2



DESCRIPTION

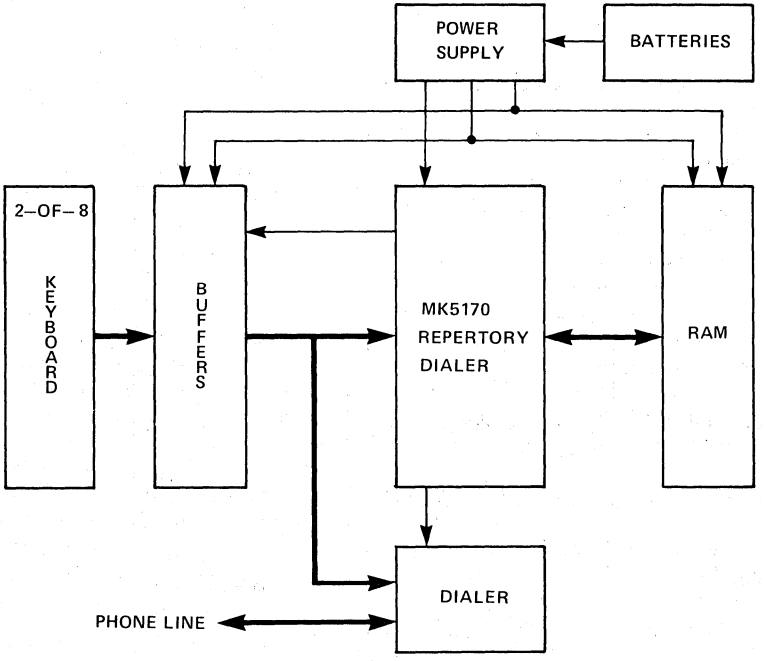
The MK5170 is a multi-function Repertory Dialer circuit utilizing ion-implanted, N-channel silicon gate technology and advanced circuit design techniques to provide maximum cost-effectiveness and flexibility. Pin connections are shown in Figure 1, and a block diagram is shown in Figure 2.

Several different modes of operation are possible. For minimal component count, the system of Figure 3 can be used with the keyboard configuration shown in Figure 4. This configuration is ideally suited to a 10-number repertory system and places the function control buttons on column 4 of a standard telephone keypad. For systems with more features, the system of Figure 5 can be used with the input matrix shown in

Figure 6. Note that the input matrix of Figure 6 permits the use of a calculator-type 1-of-N keyboard. The matrix includes both push-buttons and diode-selectable options. The options are selected by connecting a diode between the appropriate digit strobe and the keyboard scan input. Digit strobes are generated by an external decoder which is driven by the MK5170 (See Figure 7). Figure 8 provides two single-key dialing configurations. Up to 32 individual dial entry keys (#0 - #31) are possible.

BASIC REPERTORY DIALER SYSTEM

Figure 3



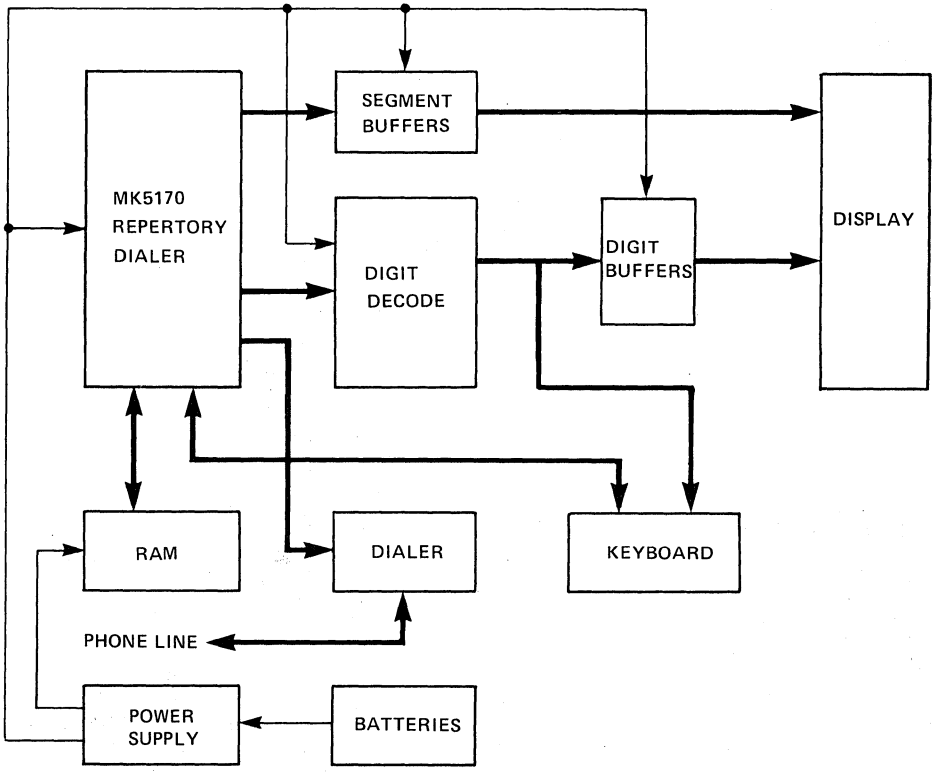
BASIC SYSTEM KEYBOARD CONFIGURATION

Figure 4

1	ABC 2	DEF 3	ENTER / DIAL	ROW 1
GHI 4	JKL 5	MNO 6	STORE	ROW 2
PRS 7	TUV 8	WXY 9	INF. PAUSE	ROW 3
*	OPER. 0	#	CLEAR	ROW 4
COL 1	COL 2	COL 3	COL 4	

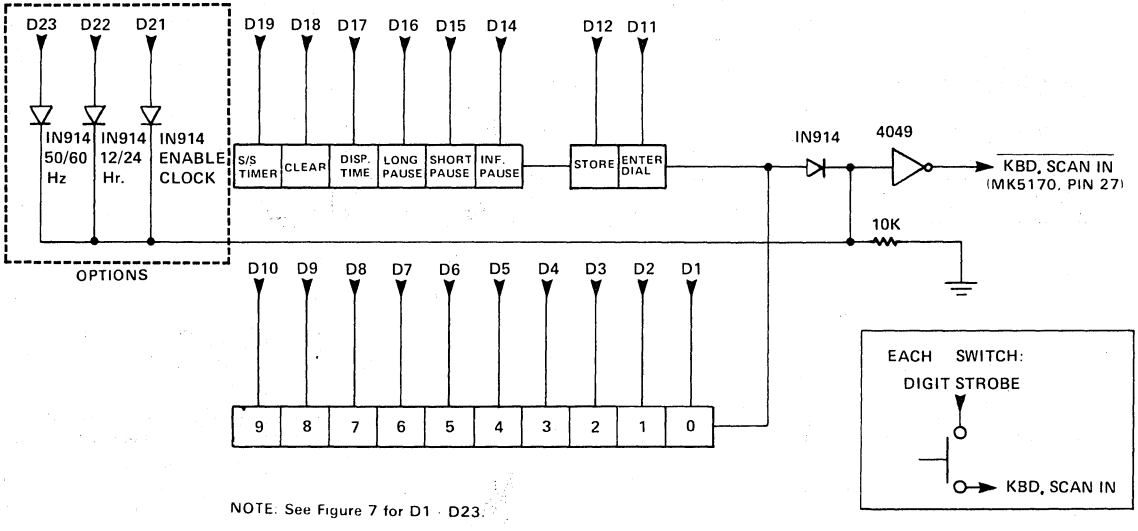
FULL FEATURE REPERTORY DIALER SYSTEM

Figure 5



FULL FEATURE KEYBOARD

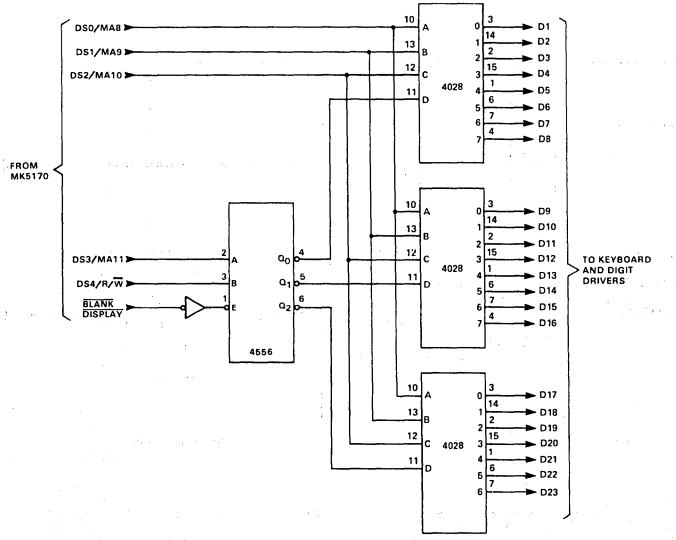
Figure 6



NOTE. See Figure 7 for D1 - D23.

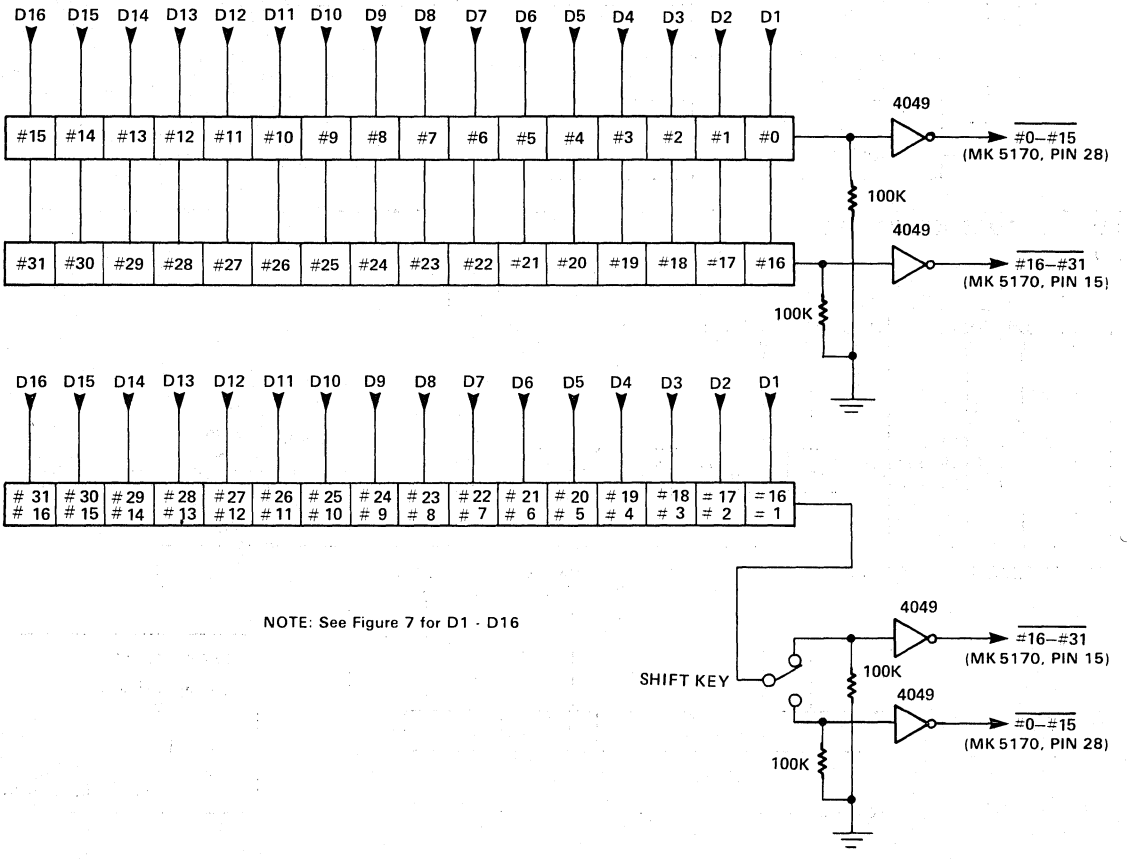
DIGIT SELECT ENCODER

Figure 7



TWO CONFIGURATIONS FOR SINGLE-KEY DIALING

Figure 8



NOTE: See Figure 7 for D1 - D16

Four types of functions are used to control the dialer: (1) ENTER/DIAL allows entry and dialing of telephone numbers, (2) STORE enables storage of entered numbers, (3) CLEAR clears erroneous entries or begins a data entry sequence and (4) PAUSE provides for inter-group pauses while dialing. Note that one of three lengths of pause may be selected:

(a.) Infinite pause which is terminated either by pressing the ENTER/DIAL button or by pressing one of the #0 through #31 keys; (b.) Short pause (1.5 seconds) which is terminated either by a 1.5-second time-out or by the means described in (a.); and (c.) Long pause (5 seconds) which is terminated either by a 5-second timeout or by the means described in (a.).

Two additional buttons are used to control the clock and the timer. DISP. TIME causes the MK5170 to display the current time. If this button is pressed and held for more than 3 seconds, then the MK5170 will enter the set time mode. During the 3-second timeout, the colons will stop flashing. At the conclusion of the timeout, the colons will resume flashing and the time can be set via the number keys. S/S TIMER provides for displaying the timer as well as starting and stopping it. If S/S TIMER is pressed and the timer is not being displayed, the display will change to show the timer count. If the timer is being displayed when S/S TIMER is pressed, the timer will start if it is not running and will stop if it is running.

An additional feature of the MK5170 is that, once a minute, the current time is stored in external RAM. The storage occurs on the minute transition. For example, as the time changes from 1:02 to 1:03, 1:02 will be stored. If AC power is then lost between 1:03:00 and 1:03:59, the clock will power up at 1:02:00 when AC power is restored. To further explain the operation of the Mk5170, a few examples are given below:

EXAMPLE 1: Storing a Number to be Dialed Later Using ENTER/DIAL

1. With the phone on-hook, press the ENTER/DIAL key. Digits 21 and 22 (See Figure 9), the address code, will show only decimal points. The remainder of the display will show the contents of the dial buffer. If the dial buffer is empty, only decimal points will be shown in digits 1 through 20.

2. Enter the address code. As the address code is entered it will be displayed in digits 21 and 22. If only 1K of memory has been installed, the first digit will be entered into digit 21 and digit 22 will be zero. Otherwise, the first entry will be displayed in digit 22 and the second entry will be displayed in digit 21. After a number has been entered in digit 21, the memory contents referenced by the address code will be shown on the display. If nothing has been stored in the referenced location, only decimal points will show in digits 1 through 20.

3. If digits 1 through 20 are not blank, press the CLEAR key. Enter the number to be dialed. As the digits are entered, they will appear on the display beginning at digit 20. If a pause is required, press the appropriate pause key. The code corresponding to the key, as shown in Figure 10, will appear on the display.

4. Press the STORE key. The telephone number shown in digits 1 through 20 will be stored in the memory location specified by the address code.

EXAMPLE 2: Dialing a Stored Number Using ENTER/DIAL

1. Lift the receiver and press the ENTER/DIAL key. Digits 21 and 22, the address code, will show only decimal points.

2. Enter the address code. Entry will be as described in Step 2 of Example 1. The dialing sequence will begin when the number is recalled from memory.

3. If the call wasn't completed, hang up the receiver. To redial the number, lift the receiver and press the ENTER/DIAL key twice.

EXAMPLE 3: Storing a Dialed Number Using ENTER/DIAL

1. Lift the receiver and dial the number. As the keys are pressed their corresponding code will appear on the display. The address code will show only decimal points. If the keyboard of Figure 4 is used, * and # can be dialed. If a pause key is pressed, its code will appear on the display but the pause will not occur. If the number is redialed or stored and recalled from memory, the pause will be executed when it is encountered.

2. Before going on-hook, press the ENTER/DIAL key followed by the desired address code. Entry will be as described in Step 2 of Example 1. After digit 21 is entered, press the STORE key. The telephone number will be stored in the location specified by the address code.

EXAMPLE 4: Storing a Number to be Dialed Later using #0 - #31

1. With the phone on-hook, press the button (#0 - #31) corresponding to the desired number. The address code will be two digits corresponding to the pressed button.

2. Proceed as described in Steps 3 and 4 of Example 1.

EXAMPLE 5: Dialing a Stored Number Using #0 - #31

1. Lift the receiver and press the button (#0 - #31) corresponding to the desired number. The address code will be two digits corresponding to the pressed button. As soon as the number is recalled from memory, the dialing sequence will begin.

2. If the call was not completed, proceed as described in Step 3 of Example 2.

EXAMPLE 6: Setting the Clock

1. Press the DISP. TIME button and hold for 3 seconds. While the key is held, the colons will not flash. After the 3-second timeout, the colons will resume flashing.

2. Press the CLEAR key. The time will be reset to 1 a.m.

3. Enter the desired time via the number keys. Illegal entries will be ignored. If an error is made, repeat step 2. Only the first 4 entries will be accepted.

4. After the correct data has been entered, press the DISP. TIME key. Clock setting will then be disabled.

EXAMPLE 7: Displaying the Clock

1. Press the DISP. TIME button. The clock will be displayed but cannot be set unless the sequence shown in Example 6 is followed.

2. If the CLOCK ENABLE diode has been installed (see Figure 6), the clock will automatically be displayed 10 seconds after dialing is completed.

EXAMPLE 8: Operating the Timer

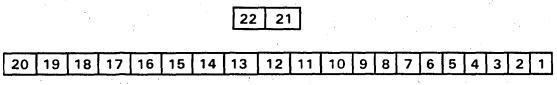
1. Whenever it is desired to display the timer, press the S/S TIMER button.

2. If the timer is being displayed when the S/S TIMER button is pressed, one of the following actions will result: a. If the timer is running, it will stop
   b. If the timer is stopped, it will start

3. If the timer is being displayed when the CLEAR button is pressed, it will be cleared to 00.00.00.

DISPLAY ORGANIZATION

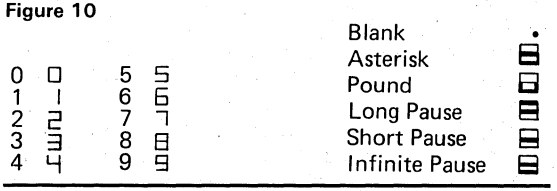
Figure 9



Digits 22 & 21 - Address Code (Rep Dialer Mode)
Digits 20 - 1 - Dial Buffer Contents (Rep Dialer Mode)
Digits 20 - 15 - Real time - H.M.S. (Clock Mode)
Digits 20 - 15 - Elapsed Time - H.M.S. (Timer Mode)
Digits 19 & 17 - Decimal Points (Flashing in Clock Mode; Fixed in Timer Mode)

CHARACTER FONT

Figure 10



FUNCTIONAL PIN DESCRIPTION

Pin 1, XTL1 and Pin 2, XTL2

These pins are the time-base inputs. With a crystal connected between these pins, the MK5170 will provide the Row/Column timing shown in the AC characteristics section. No other oscillator components are required.

Pin 3, SA/MA0

This output normally has segment A information for the display. During memory access, this output drives the LSB of the memory address.

Pin 4, SB/MA1

This output normally has segment B information for the display. During memory access, this output drives the 2nd LSB of the memory address.

Pin 5, SC/MA2

This output normally has segment C information for the display. During memory access, this output drives the 3rd LSB of the memory address.

Pin 6, SD/MA3

This output normally has segment D information for the display. During memory access, this output drives the 4th LSB of the memory address.

Pin 7, N/C

This pin has no user-accessible function but it should not be used as a tie point.

Pin 8, DS0/MA8

This output normally has the LSB of the digit select code. During memory access, this output drives the 4th MSB of the memory address.

Pin 9, DS1/MA9

This output normally has the 2nd LSB of the digit select code. During memory access, this output drives the 3rd MSB of the memory address.

Pin 10, DS2/MA10

This output normally has the 3rd LSB of the digit select code. During memory access, this output drives the 2nd MSB of the memory address.

Pin 11, DS3/MA11

This output normally has the 2nd MSB of the digit select code. During memory access, this output drives the MSB of the memory address.

Pin 12, DS4/R/$\overline{W}$

This output normally has the MSD of the digit select code. During memory access, this output drives the memory read/write line. A low on this pin enables the write mode; a high allows the memory to be read.

Pin 13, CE1

This output enables the least significant memory chip.

Pin 14, CE2

This output enables the most significant memory chip.

Pin 15, $\overline{\#16 - \#31}$

This input is used to interrogate single-key ENTER/DIAL keys 16 through 31. As shown in Figure 8, these keys are tied to digit strobes 1 through 16, respectively.

Pin 16, SP/MA7

This output normally has segment P (decimal point) information for the display. During memory access, the output drives the 5th MSB of the memory address.

Pin 17, SG/MA6

This output normally has segment G information for the display. During memory access, this output drives the 6th MSB of the memory address.

Pin 18, SF/MA5

This output normally has segment F information for the display. During memory access, this output drives the 6th LSB of the memory address.

Pin 19, SE/MA4

This output normally has segment E information for the display. During memory access, this output drives the 5th LSB of the memory address.

Pin 20, GND

This pin is logic and circuit ground.

Pin 21, N/C

This pin has no user-accessible function but it should not be used as a tie point.

Pin 22, $\overline{\text{Blank Display}}$

This signal goes low to blank the display by inhibiting an external digit select decoder.

Pin 23, $\overline{\text{Dialing}}$

This output goes low during a dialing cycle and is used to disable the 2-of-8 keyboard.

Pin 24, $\overline{\text{On-Hook}}$

If this pin is pulled low, the telephone is on-hook and the ENTER/DIAL key functions as an ENTER key. If this input goes low during dialing, dialing is terminated and the dialer resorts to its normal scanning routine. If this pin is high, the telephone is off-hook and dialing can occur.

Pin 25, $\overline{\text{Inh. Dial}}$

This pin goes low during data entry to inhibit the MK5090 or MK5098 and prevent tones or pulses from being generated.

Pin 26, $\overline{\text{MEM. DATA IN}}$

The dialer uses this pin to read data from the external memory.

Pin 27, $\overline{\text{KBD. SCAN IN}}$

This is the input for the function keys, options and number keys. The use of the options is described below:

50/60 Hz (D23) (See Figure 6)

If a diode is not installed, the MK5170 will require a 60 Hz timebase for the clock and timer. Installing a diode indicates that a 50Hz timebase is to be used.

12/24 HR (D22) (See Figure 6)

If a diode is not installed, the MK5170 will display the clock in 12-hr format. Installing a diode will cause the clock to be displayed in 24-hr format with leading zeroes.

Enable Clock (D21) (See Figure 6)

10 seconds after the MK5170 completes a dialing cycle, one of two actions will occur: (1) If the Enable Clock diode is installed, the MK5170 will display the clock or (2) If the diode is not installed, the display will be blanked. Pressing any key will unblank the display.

The use of the remaining keys is described in Table 1. State Control Sequence for the MK5170 Repertory Dialer.

Pin 28, $\overline{\#0 - \#15}$

This input is used to interrogate single-key ENTER/DIAL keys 0 through 15. As shown in Figure 8, these keys are tied to digit strobes 1 through 16, respectively.

Pin 29, $\overline{\text{MEM. DATA OUT}}$

This output is used to transmit data to the external memory.

Pin 30 through Pin 33, $\overline{\text{COL 4}}$ through $\overline{\text{COL 1}}$

These pins are used to interrogate the keyboard columns and to drive the column inputs of the MK5090 tone dialer or MK5098 pulse dialer.

Pin 34 through Pin 37, $\overline{\text{ROW 4}}$ through $\overline{\text{ROW 1}}$

These pins are used to interrogate the keyboard rows and to drive the row inputs of the MK5090 tone dialer or MK5098 pulse dialer.

Pin 38, 50/60 Hz

This input provides the time base for the real time clock.

Pin 39, $\overline{\text{POC}}$

This input can be used to force a power-on-clear.

Pin 40, V_{CC}

+5V, ± 5%

STATE CONTROL SEQUENCE FOR THE MK5170 REPERTORY DIALER
Table 1

STATE	LAST FUNCTION ENTERED	PRESENT FUNCTION	RESULTS
Power Up	None	None	Display all decimal points; digits blanked
	None	Disp. Time	Display clock. Will show 1.00.00 if memory power has failed or if this is the first application of power. Otherwise, it will show the time at which AC power was lost.
	None	S/S Timer	Display timer. 00.00.00. Timer not running
	None	E/D	Display phone number. Display will not change.
	None	Digits, *, #, Long/Short/Inf. Pause	Display the symbol for each digit or function as it is is entered. Any entries above 20 digits are ignored.
	None	Clear	No change
	None	Store	No Change
	None	#0 - #31	Show the number stored in the corresponding memory location. If nothing has been stored, display all decimal points with digits blanked, except for address code. If off-hook, dial the number.

Table 1 Continued

STATE	LAST FUNCTION ENTERED	PRESENT FUNCTION	RESULTS
Display Clock	Disp. Time	Disp. Time	No change. Colons will not flash while Disp. Time switch is held. If switch is held for more than three seconds, the colons will start flashing and the MK5170 will enter the set clock state.
		S/S Timer	Display timer. Colons not flashing.
		E/D	Blank address code, display phone number.
		Long/Short/Inf. Pause, Clear, Store	No change
		#0 - #31	Show the number stored in the corresponding memory location. If off-hook, dial the number.
		Digits, *, #	Display the digit or function when it is entered. Start manual entry sequence.
Display Timer	S/S Timer	S/S Timer	If timer was running, stop. If timer was not running, start.
		Clear	Clear timer.
		Disp. Time	Display clock.
		Long/Short/Inf. Pause, Store	No change
		Digits, #, *	Display the digit or function when it is entered. Start manual entry sequence.
		E/D	Blank address code, display phone number
		#0 - #31	Show the number stored in the corresponding memory location. If off-hook, dial the number.
Manual Entry	Digits, *, #	Digits, #, * Long/Short/Inf. Pause	Display the symbol for each digit or function as it is entered. Entries above 20 digits are ignored.
		Clear	Clear the display
		Disp. Time	Display clock
		Store, E/D	No change
		#0 - #31	Display the number stored in the corresponding memory location. If off-hook, dial the number
Display Phone Number	E/D	None	Blank address code, display phone number.

Table 1 Continued

STATE	LAST FUNCTION ENTERED	PRESENT FUNCTION	RESULTS
Display Phone Number Continued		Digit	Enter digit into address code. If 1K of memory is installed, enter digit into LSD and recall phone number from memory. If off-hook, dial the number.
		S/S Timer	Display timer
		Disp. Time	Display clock
		Store, Long/ Short/Inf. Pause, *, #	No change
		Clear	Clear display
		#0 - #31	Display the number stored in the corresponding memory location. If off-hook, dial the number.
	Digit	Digit	If second digit and more than 1K of memory is installed, store digit in LSD of address code and recall phone number from memory. If off-hook, dial number. If second digit and 1K of memory is installed, store digit in MSD of phone number. If not second digit, store in next location in phone no.
		*, #, Long/Short/ Inf. Pause	If second digit and more than 1K of memory is installed, ignore. If not second digit, store in next location in phone number.
		Clear	If address code is incomplete, clear address code and phone number. If address code is complete, clear only the phone number.
		Store	If address code is complete, store the phone number. Otherwise, ignore.
		#0 - #31	Display the number stored in the corresponding memory location. If off-hook, dial the number.
	E/D	E/D	Dial the number in the dial buffer (redial).
	Digit	S/S Timer	Display timer
		Disp. Time	Display clock
Set Clock	Disp. Time for greater than 3 seconds	Digit	Legal digit will be entered into next location. Illegal digit will be ignored.
		Clear	Set time to 1.00.00 a.m.

Table 1 Continued

STATE	LAST FUNCTION ENTERED	PRESENT FUNCTION	RESULTS
Set Clock Continued		Store, *, #, Long/ Short/Inf. Pause	No change
		#0 - #31	Display the number stored in the corresponding memory location. If off-hook, dial the number.
		E/D	Display phone number
		S/S Timer	Display timer
		Disp. Time	Display clock, leave set clock mode.

APPLICATION INFORMATION

The Basic Repertory Dialer System of Figure 3 represents the minimum number of components required to implement a repertory dialer system using MK5170. A 2-of-8 keyboard, using the interface shown in Figure 11, provides the system control functions of number entry, Enter/Dial, Store, Inf. Pause and Clear. A quad comparator, an LM2901 or equivalent, is used as a buffer between the keyboard and the MK5170. The non-inverting input of each comparator is biased at ½ +5M and the appropriate non-inverting inputs are tied to their assigned row or column. A key closure will pull two of the non-inverting inputs within two diode drops of ground, thus causing the associated comparator outputs to go low. The MK5170 then senses these two low levels and, after identifying the key, drives the $\overline{\text{DIALING}}$ output low, which pulls the inverting inputs within one diode drop of ground and causes all of the comparator output transistors to turn off, thus isolating the keyboard from the MK5170 so that the MK5170 can apply row and column information to the dialer without interference from the keyboard.

The dialer interfaces shown in Figure 12 and Figure 13 include level conversion circuitry as well as an Inhibit Dial feature. The active - low row and column signals (ROW 1 - COL 3) are applied to the bases of NPN transistors. Because the power supply to the tone dialer can vary between 3.4 volts and 10.5 volts and the power supply to the pulse dialer can vary between 2.5 and 5 volts, level conversion is required between the 0 - to 5 - volt row and column signals and the corresponding inputs to the MK5090 or MK5098. This required level conversion is provided by the 7 NPN transistors. When the MK5170 is required to isolate the dialer from the 2-of-8 keyboard (i.e. during data entry), it does so by driving the $\overline{\text{INH. DIAL}}$ line low. The $\overline{\text{INH. DIAL}}$ signal is inverted and used to turn all of the NPN transistors on so that the signals applied to the row and column inputs of the MK5090 and MK5098 will be at their inactive level. When the MK5170 starts a dialing cycle, the $\overline{\text{INH. DIAL}}$ line will go high and the required sequence of row and column signals will be applied to the bases of the NPN level converters. The 4050 buffers and 4049 inverting buffers shown in the dialer interface schematics are powered from the phone line and provide the buffering and logic inversion necessary to meet the input requirements of the MK5090 and MK5098, as well as permitting the use of 1 megohm pull up resistors at the collectors of the NPN level converters. Using large - value pullup resistors reduces the amount of current that the buffer circuitry draws from the phone line.

The Full-Feature Repertory Dialer System of Figure 5 implements all the features provided by the MK5170 by placing all of the keys and option diodes in a 3 x 24 matrix shown in Figure 6 and Figure 8. $\overline{\text{KBD. SCAN IN}}$, #0 - #15 and #16 - #31 are scanned by the MK5170. When an active low level is detected on any of the three scan lines, the MK5170 determines which key has been pressed and takes appropriate action. Digit strobes for scanning the input matrix are generated by the circuit shown in Figure 7, which encodes the 5-bit digit select code (DS0 - DS4) into 1 of 23 digit strobes (D1 - D23). These positive pulses are then used to drive the bipolar digit drivers for the display as well as for scanning the input matrix. A $\overline{\text{BLANK DISPLAY}}$ input is provided to inhibit the generation of digit strobes during memory access, since the segment and digit encoding lines are shared by memory addresses and read/write control (See Figure 7).

The Power Supply and Timebase Reference circuit shown in Figure 14 provides two independent 5-volt power supplies: (1) +5L which powers the MK5170 and the display circuitry and (2) +5M which powers the memory, the memory protect logic and the keyboard buffers and is provided with a battery backup which consists of 6 NiCd cells and a charging circuit. The

Timebase Reference consists of a comparator with hysteresis so that power line noise will not reach the MK5170.

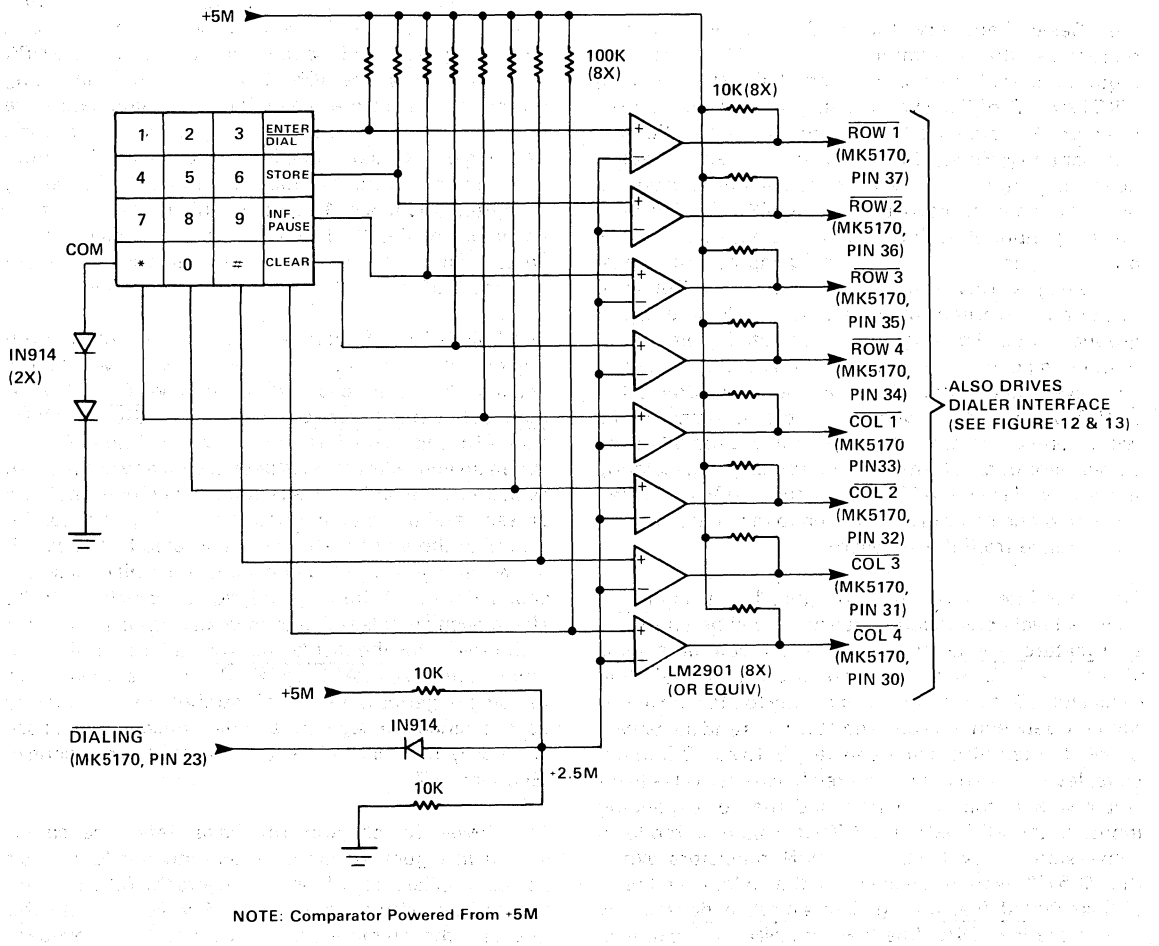
The Memory Protect Logic shown in Figure 15 provides two functions: (1) The MK5170 will be reset whenever its power supply dips to 4.75V and (2) on power up and during a power supply dip to 4.75V, $\overline{CE1}$ and $\overline{CE2}$ will be forced high so that no memory chip selects can be generated. This insures that data stored in the MK4104 will not be destroyed. If a 2102 memory is used, the memory protect latch is not required. Note, however, that CE1 and CE2 must still be inverted to enable the memory. $\overline{CE1}$ and $\overline{CE2}$ will be enabled after $\overline{POC}$ is removed from the MK5170 and CE1 goes high.

Repertory size is determined automatically by the amount of memory installed so all that is required to alter the size of the repertory is to install memory devices as shown in Figure 16.

Figure 17 shows the suggested LED drive circuitry.

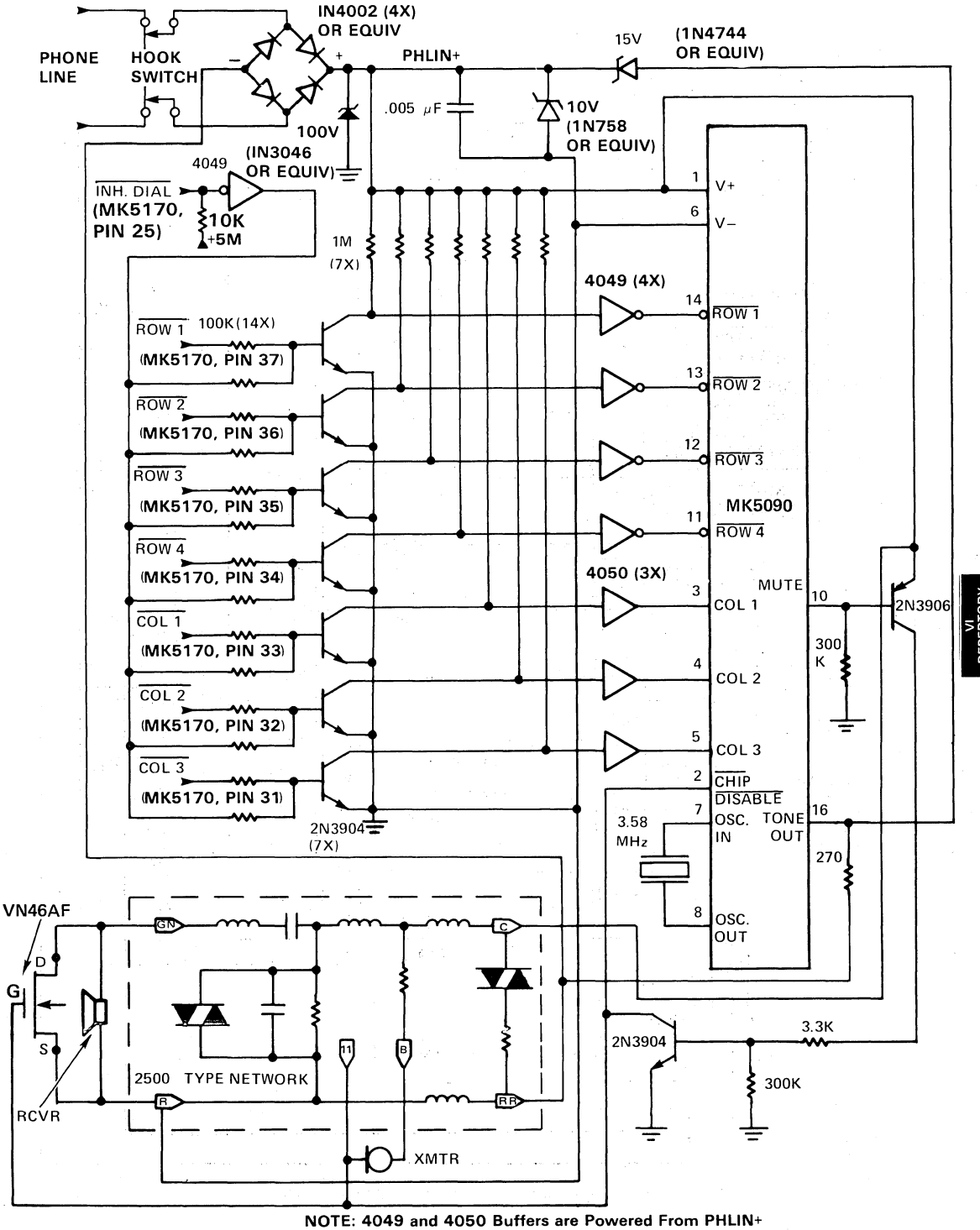
A special "on-hook" circuit, Figure 18, is shown for use with PBX systems. This circuit prevents the MK5170 from seeing the momentary line-disconnect exhibited by a PBX system as it switches to out-of-plant lines.

2 OF 8 KEYBOARD TERMINAL
Figure 11



TONE DIALER INTERFACE

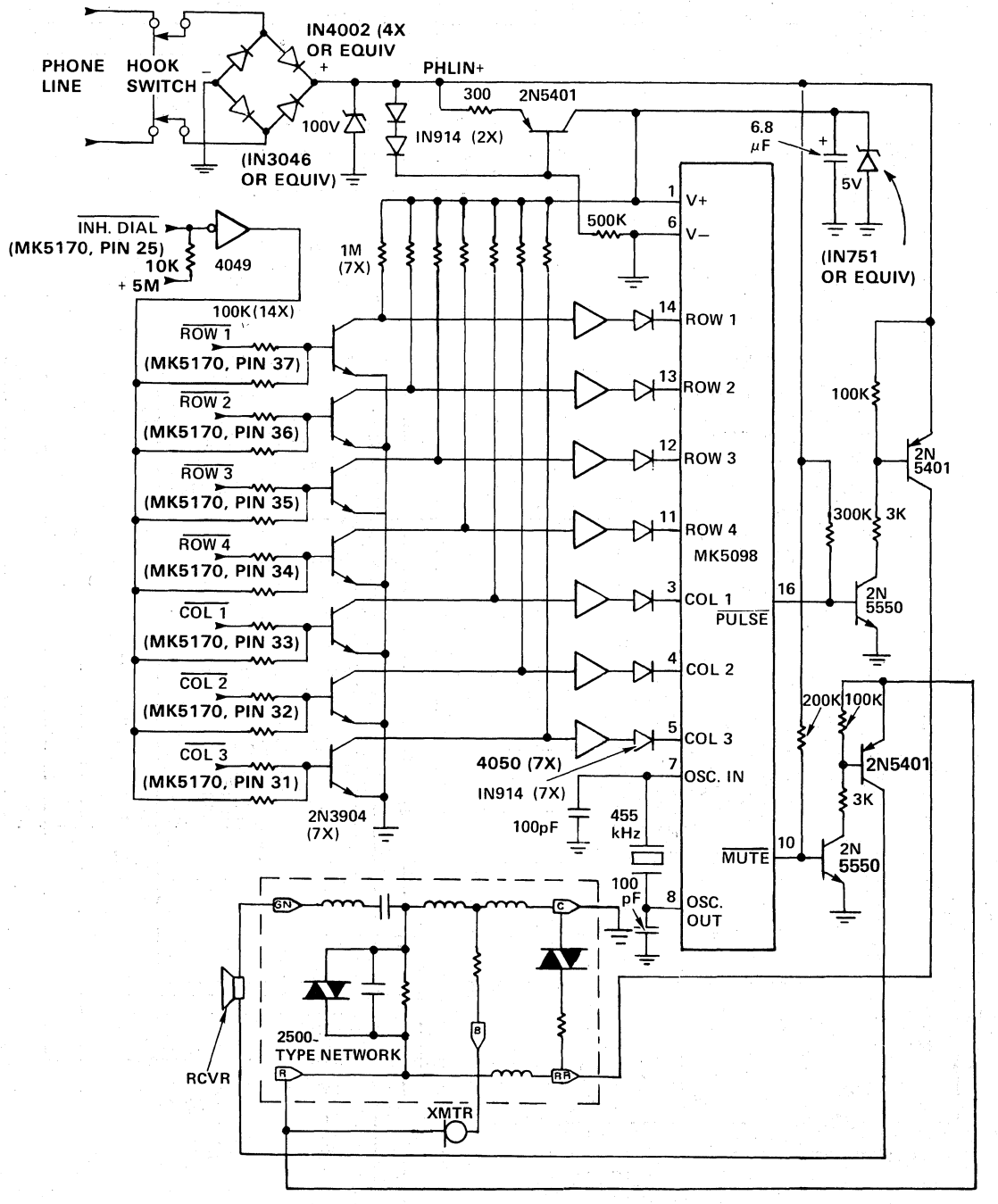
Figure 12



NOTE: 4049 and 4050 Buffers are Powered From PHLIN+

PULSE DIALER INTERFACE

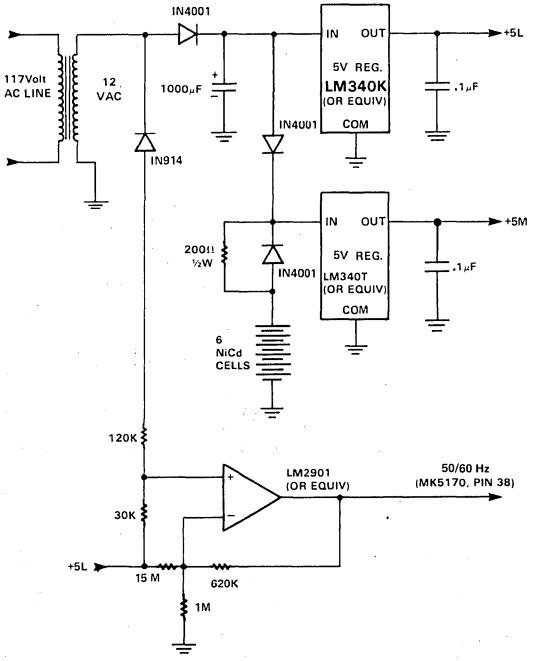
Figure 13



NOTE: 4049 and 4050 Buffers are Powered From PHLIN+

POWER SUPPLY AND TIMEBASE REFERENCE

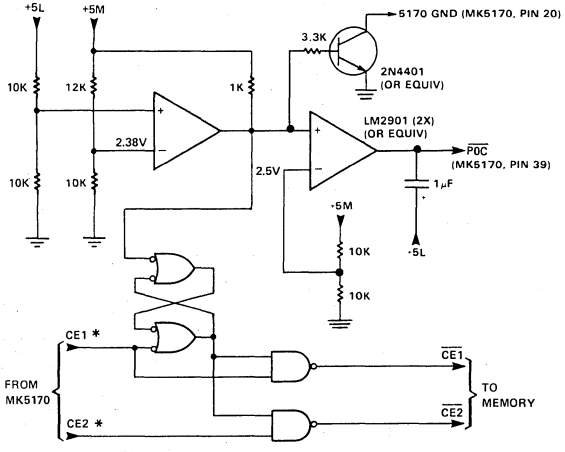
Figure 14



NOTE: COMPARATOR POWERED FROM +5M

MEMORY PROTECT LOGIC

Figure 15



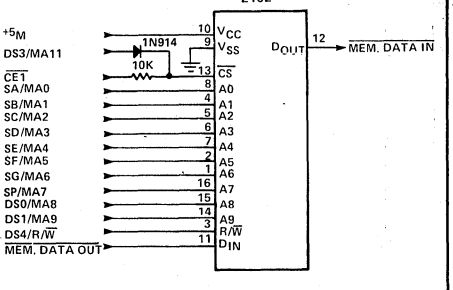
* CE1 & CE2 must be inverted to enable memory.

NOTE: ALL ACTIVE DEVICES POWERED FROM +5M

MEMORY CONNECTIONS TO MK5170

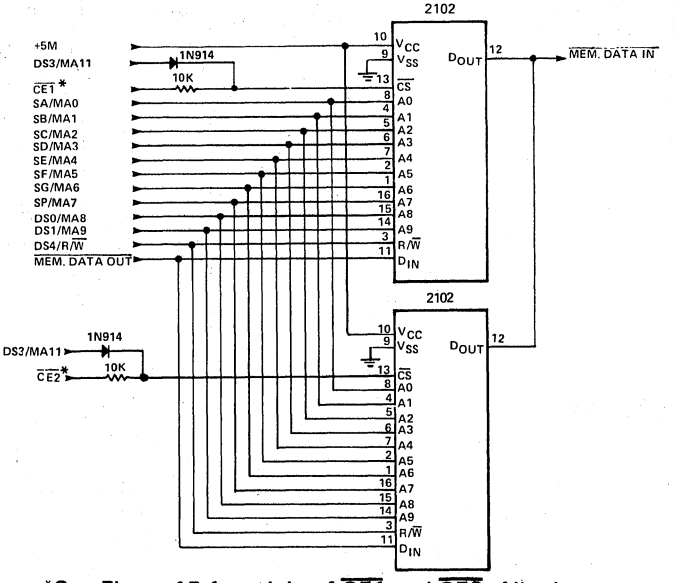
Figure 16

a. 12 - NUMBER REPERTORY



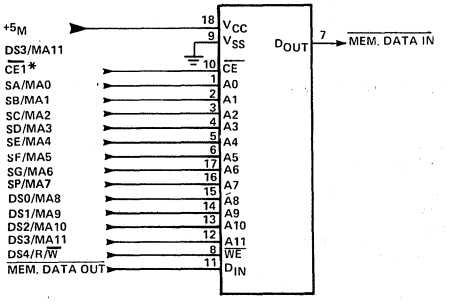
*See Figure 15 for origin of $\overline{CE1}$. All other signals interface directly with MK5170.

b. 24 - NUMBER REPERTORY



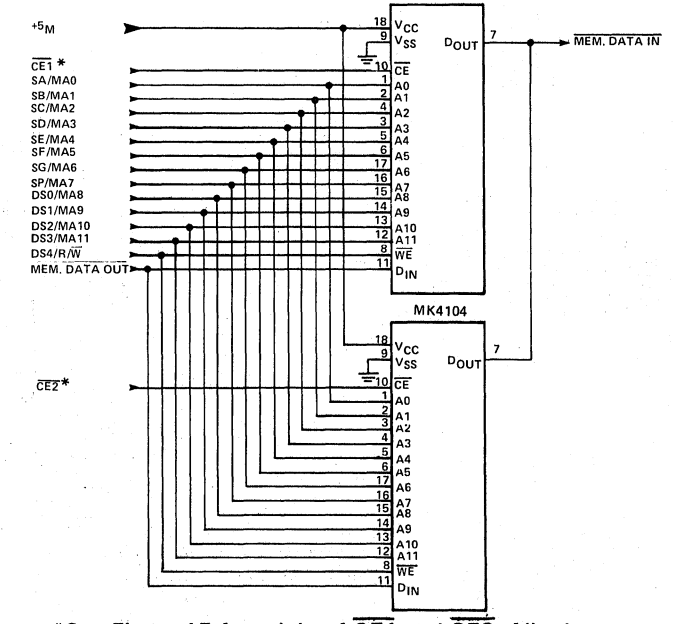
*See Figure 15 for origin of $\overline{CE1}$ and $\overline{CE2}$. All other signals interface directly with MK5170.

c. 50 - NUMBER REPERTORY



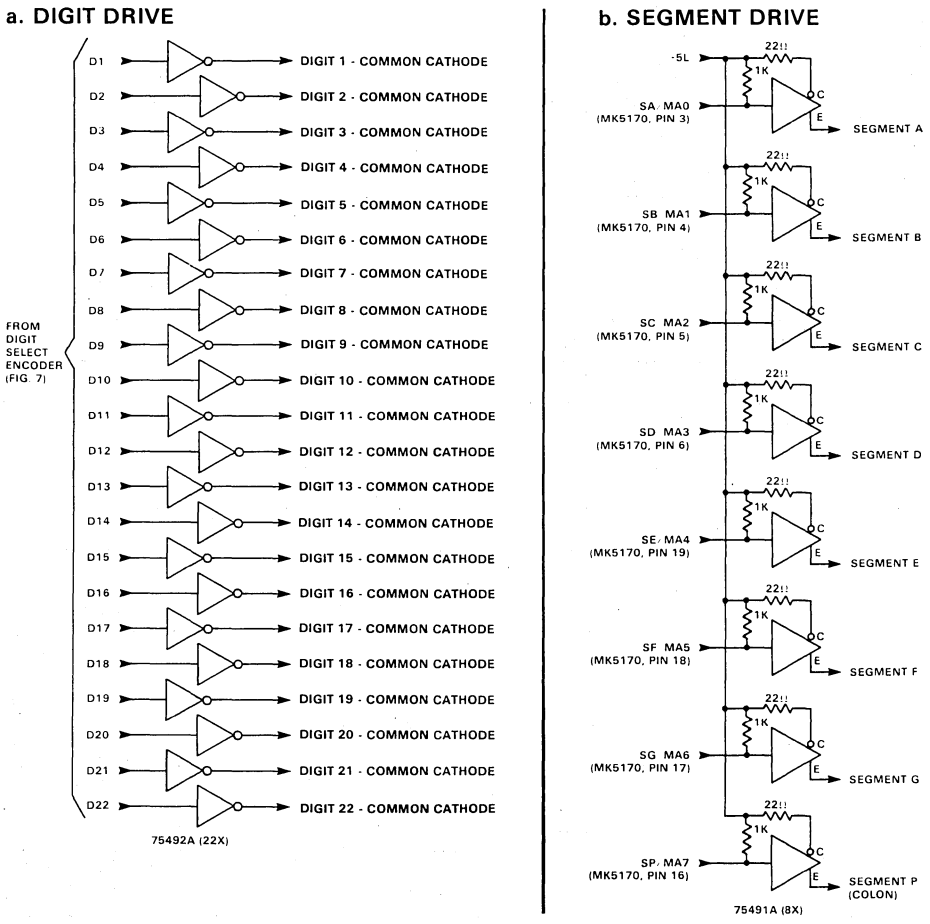
*See Figure 15 for origin of $\overline{CE1}$. All other signals interface directly with MK5170.

d. 100 - NUMBER REPERTORY

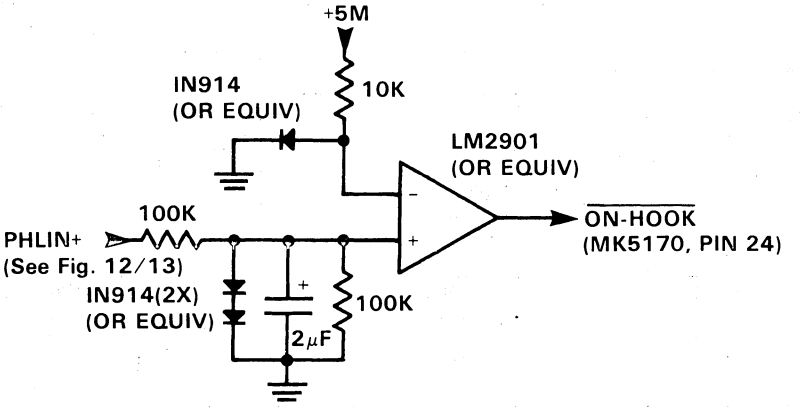


*See Figure 15 for origin of $\overline{CE1}$ and $\overline{CE2}$. All other signals interface directly with MK5170.

LED DRIVE CIRCUITRY
Figure 17



ON-HOOK CIRCUITRY
Figure 18



NOTE: Comparator is powered from +5M

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS*

Temperature under bias ..... 0°C to 70°C
Storage temperature ..... -65°C to 150°C
Voltage on any pin with respect to ground ..... -1.0V to +7V
Power dissipation 1.0W

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and function operation of the device at these or any other condition above these indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ± 5%

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
I_{CC}	Power Supply Current		55	77	mA	Output Open
P_D	Power Dissipation		275	385	mW	Outputs Open
V_{IH}	Input High Level	2.0		5.8	V	
V_{IL}	Input Low Level	-0.3		0.8	V	
I_{IH}	Input High Current			100	μA	V_{IH}=2.4V Internal Pull-Up
I_{IL}	Input Low Current			-1.6	mA	V_{IL}=0.4V
I_{OH}	Output High Current	-100			μA	V_{OH}=2.4V
I_{OL}	Output Low Current	1.8			mA	V_{OL}=0.4V
R_{IP}	Internal Pull-up Resistor		6		kΩ	Output transistor off

AC CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ± 5%

SIGNAL	SYMBOL	PARAMETER	MIN	MAX	UNIT	COMMENTS
	t_O(XTL)	Time base period, Crystal mode	250	279	ns ns	4MHz crystal 3.58 MHz crystal
0	t_0	Internal 0 clock period	500	558	ns	
POC	t_{RH}	POC hold time, Low	3.75 4.10		μs μs	4MHz crystal 3.58MHz crystal
50/60Hz	t_{EH}	50/60Hz hold time, High	3.75 4.10		μs μs	4MHz crystal 3.58MHz crystal
Row/Col	t_{RC}	Row/Column output duration & off time	68	76	ms ms	4MHz crystal 3.58MHz crystal
	t_{ACC}	Memory Access Time	10		μs	
	t_{DP}	Digit Period		10.8	ms	3.58MHz crystal
	t_{DON}	Digit On Time		490	μs	3.58MHz crystal
	D.C.	Display Duty Cycle	3.2	3.2	%	

CAPACITANCE

T_A = 25°C, f_{XTL} = 4MHz

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITIONS
C_{IN}	Input capacitance, all pins except XTL1, XTL2		7	pF	Unmeasured pins returned to ground
C_{XTL}	Input capacitance, XTL1, XTL2	18	23	pF	

MOSTEK®

TELECOMMUNICATIONS

Ten-Number Repertory Dialer

MK5175(N)

FEATURES

- Silicon Gate CMOS process for low-voltage (2.0 V to 10.0 V) and low-power operation
- Stores ten 16-digit telephone numbers
- Line operation off-hook, battery operation on-hook
- Stand-alone Pulse dialer
- Interfaces with Mostek's Tone generators
- PABX pause key input
- Last-number-dialed memory
- Last number dialed may be transferred to any one of nine other locations
- Make/break ratio is pin-selectable in the Pulse mode
- Uses either the inexpensive Form A-type keyboard or the standard 2-of-7 matrix keyboard with common V– (Tone mode may use SPST switch control key in 13-key mode to avoid redundancies in key entries)

DESCRIPTION

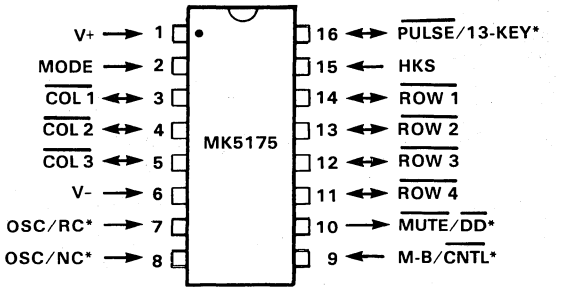
The MK5175 is a monolithic integrated ten-number repertory dialer manufactured using Mostek's Silicon Gate CMOS process. The circuit accepts keyboard inputs and provides the Pulse and Mute logic levels required for loop-disconnect signaling. For DTMF signaling, the MK5175 may be interfaced with one of Mostek's new Tone generators with minimum additional circuitry.

The dialer will function in either Tone or Pulse mode, dependent upon the logic level presented to Pin 2, the "Mode Select" pin. The interpretation of several inputs and outputs is dependent upon the mode selected.

In Pulse mode, the time base for the circuit is a ceramic resonator which is low-cost, yet provides an accurate reference. In Tone mode, a single-pin RC oscillator provides the frequency reference for the circuit. This provides the least expensive means to adequately control the tone output rate. The block diagram in Figure 2 illustrates the general internal structure of the MK5175.

PIN CONNECTIONS

Figure 1



*Dual pin designations correspond to the pulse/tone modes, respectively

VI REPERTORY DIALERS

An on-chip RAM is capable of storing ten sixteen-digit telephone numbers including the last number dialed. When used in a PABX system, a pause (# key) may be stored in the number sequence. The repertory dialer will recognize this pause when automatically dialing and stop until any key input is received.

The MK5175 repertory dialer uses a standardized pinout scheme common to all Mostek Tone and Pulse dialers. This will facilitate the design of a family of telephone products using common PC boards and circuit components.

FUNCTIONAL DESCRIPTION

V+, Pin 1

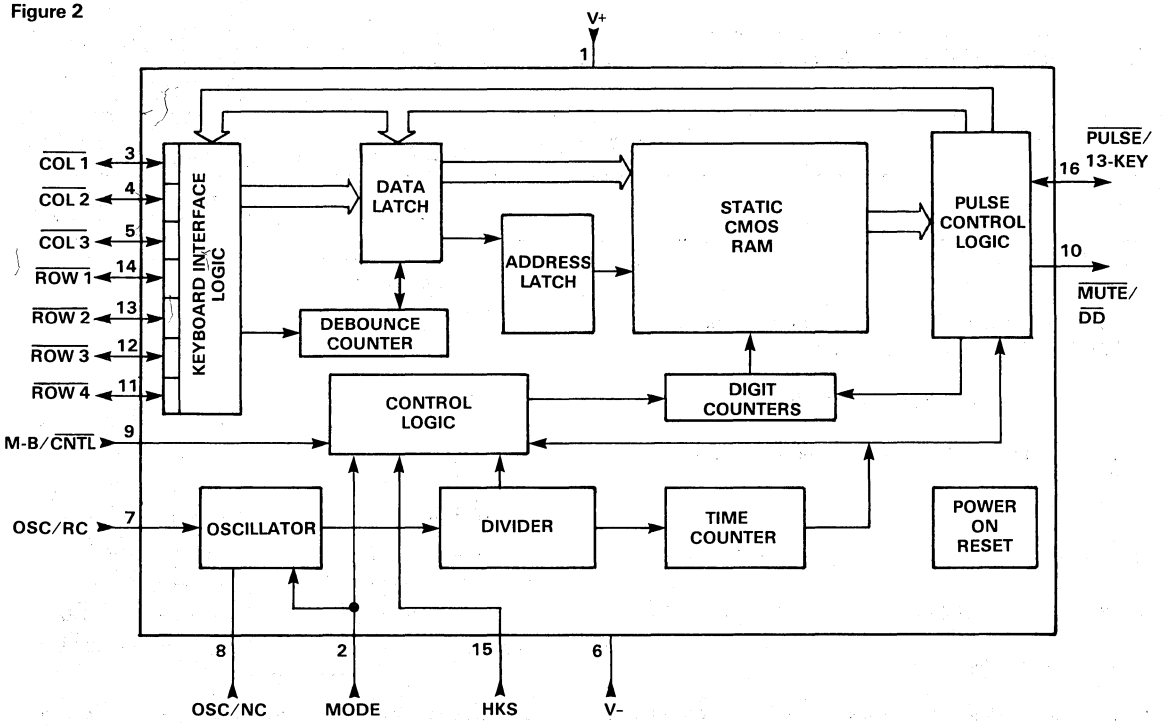
Pin 1 is the positive supply input to the part and is measured relative to V– (Pin 6). The voltage on this pin should not exceed 10 volts. On-chip zener diodes will provide protection from supply transients in most applications.

MODE, Pin 2

The MK5175 will function in either Tone or Pulse mode, dependent upon the logic level presented to Pin 2. For Pulse mode operation, this pin must be tied to V– (Pin 6). For Tone mode, it should be tied to V+ (Pin 1). The interpretation of Pins 7, 8, 9, 10, and 16 are dependent upon the mode selected.

MK5175 BLOCK DIAGRAM

Figure 2



KEYBOARD INPUTS, Pins 3, 4, 5, 11, 12, 13, 14

The MK5175 incorporates an innovative keyboard scheme that allows either the standard 2-of-7 keyboard with negative common or the inexpensive single-contact (Form A) keyboard to be used, as shown in Figure 3.

A valid key entry is defined by either a single row being connected to a single column or V- being simultaneously presented to both a single row and column.

In the Tone mode, the MK5175 features a bidirectional keyboard scheme. In this scheme, the MK5175 simulates key closures so that a tone dialer will perform the repertory tone-dialing function. As the MK5175 passively monitors the key inputs, they are debounced, decoded, and stored in the on-chip LND (Last Number Dialed) buffer. The repertory dialer will disable the tone generator and scan the keyboard whenever a command key entry is detected, as shown in Figure 4.

In the Pulse mode, the MK5175 keyboard inputs are totally static until an initial valid key input is sensed. The oscillator is then enabled and the rows and columns are alternately scanned (pulled high, then low) to verify the input is valid. Keyboard bounce is ignored for 32 ms after the initial key down is detected. A key input is accepted if it is valid after this initial debounce time. This scheme allows any valid key input to be recognized in less than 40 ms after the initial key closure. This does not affect the normal functioning of the tone generator, which begins signaling immediately.

V-, Pin 6

Pin 6 is the power supply return pin and is the measurement reference for V+ (Pin 1).

OSCILLATOR, Pins 7, 8

In the Tone mode, only a resistor and a capacitor are needed to provide the frequency reference for the MK5175. The resistor should be connected from Pin 7 (OSC/RC) to V+ (Pin 1) and the capacitor from Pin 7 to V- (Pin 6). Pin 8 (OSC/NC) should be connected to V+. A nominal frequency of 8 kHz will provide a tone rate of 100 ms on and 100 ms off. This tone rate is directly proportional to the oscillator frequency.

In the Pulse mode, an accurate frequency reference is obtained using an on-chip inverter with sufficient gain to provide oscillation when used with a low-cost 480 kHz ceramic resonator (antiresonant mode). In addition to the resonator, two external capacitors are required, as shown in Figure 6.

M-B/$\overline{\text{CNTL}}$, Pin 9

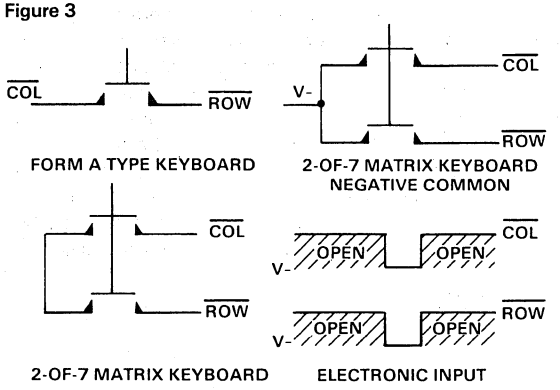
In the 13-key Tone mode, Pin 9 can be used as a $\overline{\text{Control}}$

input by connecting a control key (n.o. SPST switch) from this pin to V– (Pin 6). This feature allows the * and # key entries to be interpreted simply as DTMF signals. When not used as a key input, this pin should be connected to V+ (Pin 1). (See 13-Key Tone Mode)

In the Pulse mode, the make/break ratio may be selected by connecting this pin to either the V+ or V– supply. Table 1 indicates the two popular ratios from which the user can choose.

KEYBOARD CONFIGURATIONS

Figure 3



FORM A TYPE KEYBOARD

2-OF-7 MATRIX KEYBOARD NEGATIVE COMMON

2-OF-7 MATRIX KEYBOARD

ELECTRONIC INPUT

MAKE/BREAK RATIO SELECTION

Table 1

Input to Make/Break Pin	Pulse Output	
	MAKE	BREAK
V+ (Pin 1)	40%	60%
V– (Pin 6)	32%	68%

$\overline{\text{MUTE}}/\overline{\text{DD}}$, Pin 10

Pin 10 is the output of an open-drain N-channel transistor. In the Tone mode, Pin 10 is used to provide the tone dialer with a Dialer-Disable signal. This signal is used to inhibit the generation of tones by pulling to V– when command entries are being made.

In the Pulse mode, Pin 10 is the $\overline{\text{Mute}}$ output. It provides the logic necessary to mute the receiver while the telephone line is being pulsed. A typical method of interfacing this output is shown in the application diagram in Figure 6. Figure 5 shows the timing characteristics of the $\overline{\text{Mute}}$ output.

HKS, Pin 15

Pin 15 is the hook switch input pin. Pin 15 requires an external pull-up resistor to the positive supply. A V+ input sets the circuit in its on-hook mode, while a V– input sets it in the off-hook or dialing mode.

$\overline{\text{PULSE}}$/13-KEY, Pin 16

In the Tone mode, a V+ level at Pin 16 sets the MK5175 in a mode in which a control key (n.o. SPST) connected from Pin 9 to V– is used to initiate control functions. With Pin 16 tied to V–, the MK5175 is set in the 12-key mode and the * and # keys are used in control functions.

In the Pulse mode, Pin 16 is the $\overline{\text{Pulse}}$ output. It consists of an open-drain N-channel transistor designed to drive an external transistor. These transistors could typically be used to pulse the telephone line by controlling the loop current through the network. The timing characteristics of the $\overline{\text{Pulse}}$ output are shown in Figure 5.

OPERATION

During normal dialing, each digit is stored in the LND (Last Number Dialed) buffer, location 0. The telephone number dialed can be left in this temporary LND buffer for later use or it can be copied into any of the other nine permanent memory locations.

STORAGE

Telephone numbers to be automatically dialed by the MK5175 may be entered into the LND buffer while either on-hook or off-hook. However, the MK5175 must be in the on-hook mode for a number to be copied into a permanent memory location. A number may be copied and stored by entering the key sequence [*][*], followed by the address (1-9) of the memory location in which the number is to be stored. This operation requires 400 ms before going off-hook or reinitiating the store function. Information present in the LND buffer when new data is entered is replaced and cannot be recalled.

AUTOMATIC DIALING

The automatic dialing function is implemented by going off-hook and entering a *, followed by the address (1-9) of the desired telephone number. Dialing will begin with the release of the address key and can be interrupted by initiating a new redial command. The LND buffer will contain the information last entered. A key sequence of [*], [0] will cause the last number entered to be redialed. More than one number sequence may be automatically dialed from memory without returning on-hook.

PAUSE/CONTINUE COMMAND

The MK5175 has a feature which allows an indefinite pause to be programmed into the first 15 digits of a number sequence by entering a # key at the point in the sequence where a pause is desired. When the number is automatically dialed, the circuit will stop dialing when the pause is encountered. Any key entry after the interdigital pause (except * key) will cause the MK5175 to continue dialing the remainder of the number. If more than one pause was originally programmed into the number

sequence, a corresponding number of continue commands must be made in order for the number to be completely dialed.

NORMAL DIALING

When dialing normally in the Pulse mode, the key entry rate may exceed the dialing rate. The memory has a FIFO (first-in-first-out) architecture and any length number sequence may be dialed as long as the key entered is not more than 16 entries ahead of the digit being outpulsed.

In order to dial a * or # DTMF signal when in the Tone mode, the * or # key must be depressed twice consecutively.[1] This will cause the MK5175 to enable the tone dialer to generate the corresponding tone. However, the MK5175 will not store a * or # as a DTMF signaling digit.

Examples:

1. On-Hook, enter 323-6000
   Then enter [*][*][5]
   323-6000 is stored in location 5
   •
   •
   •
   Come off-hook
   Enter [*][5]
   323-6000 is automatically dialed

2. Off-Hook, dial 42 (PBX access code)
   While waiting for dial tone, enter #
   Dial 1-214-323-6000
   Busy/Hang up
   Enter [*][*][3]
   (Number is stored in location 3)
   •
   •
   •
   Come off-hook
   Enter [*][3]
   42 is dialed
   Wait for dial tone
   Enter 3 (continue command)
   1-214-323-6000 is dialed

13-KEY TONE MODE

An extra feature available on the MK5175 is the ability to use the entire keyboard for normal signaling such that when any key is depressed once, including * and #, the proper DTMF signal is generated. This feature is activated by connecting Pin 16 to V+. In order to utilize this function, an extra control key (n.o. SPST) connected from Pin 9 (M-B/$\overline{\text{CNTL}}$) to V– is required.

All digit entries, except * and #, are stored in the LND buffer as they are entered, whether off-hook or on-hook. However, the MK5175 must be in the on-hook mode for a number to be copied from the LND buffer into a permanent memory location. A number may be copied and stored into a permanent memory location by entering the key sequence [C][N] (where C is the control key and N is the location, 1-9, in which the number is to be stored). An indefinite pause may be programmed into a number by entering a [C][#] key sequence at the point desired.

In order to automatically dial a number in memory, the key sequence [C][N] must be entered after going off-hook, where N is the address of the number to be dialed. Last-number redial is accomplished by dialing [C][O]. If a pause has been programmed into the number to be automatically dialed, the number will be dialed up to the point where a pause is encountered. Any key entry will cause the MK5175 to continue dialing the remainder of the number. If more than one pause was programmed into the number, a corresponding number of continue commands must be made in order for the number to be completely redialed.

Examples:

1. On-hook, enter 555-2525
   Enter [C][5] (C is a control key)
   555-2525 is stored in location 5
   •
   •
   •
   Come off-hook
   Enter [C][5]
   555-2525 is automatically dialed

2. Off-hook, dial 9 (PBX access code)
   Enter [C][#] (a pause is programmed in, with no tones emitted)
   Once dial tone is established
   Dial 1-214-323-6000
   Busy/Hang up
   Enter [C][2]
   (Number is stored in location 2)
   •
   •
   •
   Come off-hook
   Enter [C][2]
   9 is dialed
   Establish dial tone
   Enter 2 (continue command)
   1-214-323-6000 is dialed

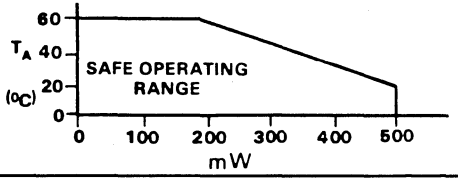
[1]True only for 12-Key Tone Mode

ABSOLUTE MAXIMUM RATINGS*

DC Supply Voltage, V+ ..... 10.5 Volts
Operating Temperature ..... -30°C to +60°C
Storage Temperature ..... -55°C to +85°C
Maximum Power Dissipation (25°C) ..... 500 mW
Maximum Voltage on any Pin ..... (V+) +0.3; (V–) -0.3 Volts

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

POWER DISSIPATION DERATING CURVE



DERATE AT 9 mW/°C WHEN SOLDERED INTO PC BOARD.

ELECTRICAL CHARACTERISTICS
DC CHARACTERISTICS

$-30°C \leq T_A \leq 60°C$

SYM	PARAMETER	MIN	TYP*	MAX	UNITS	NOTES
V+	DC Supply Voltage	2.0		10.0	V	
I_{MR}	Memory Retention Current		0.5	2.0	μA	1
I_{OP}	DC Operating Current (Tone Mode)		50	100	μA	2
I_{OP}	DC Operating Current (Pulse Mode)		100	200	μA	2
I_{ML}	Mute Sink Current: V+ = 2.0 V, Vo = 0.5 V	0.5	2.0		mA	
I_P	Pulse Sink Current: V+ = 2.0 V, Vo = 0.5 V	1.0	4.0		mA	
I_{LKG}	Mute and Pulse Leakage: V+ = 10.0 V, Vo = 10.0 V		0.001	1.0	μA	
R_{KI}	Keyboard Contact Resistance			1.0	kΩ	
C_{KI}	Keyboard Capacitance			30	pF	
K_{IL}	"0" Logic Level	V–		20% of V+	V	
K_{IH}	"1" Logic Level	80% of V+		V+	V	
K_{RU}	Keyboard Pull-Up Resistance		100		kΩ	3
K_{RD}	Keyboard Pull-Down Resistance		5.0		kΩ	3
R_{HKS}	HKS Pull-Up Resistance		100		kΩ	
R_{CNTL}	CNTL Pull-Up Resistance		100		kΩ	

NOTES

*Typical values are to be used as a design aid and are not subject to production testing.

1. Current necessary for memory to be maintained. All outputs unloaded. On-hook mode.
2. Current required for proper circuit function with a valid key input, off-hook or on-hook mode. V+ = 3.0 V.
3. Keyboard to be scanned at 125 Hz when oscillator enabled Row and Column to alternately pull high and low.

AC CHARACTERISTICS (The timing Relationships are shown in Figures 4 and 5)

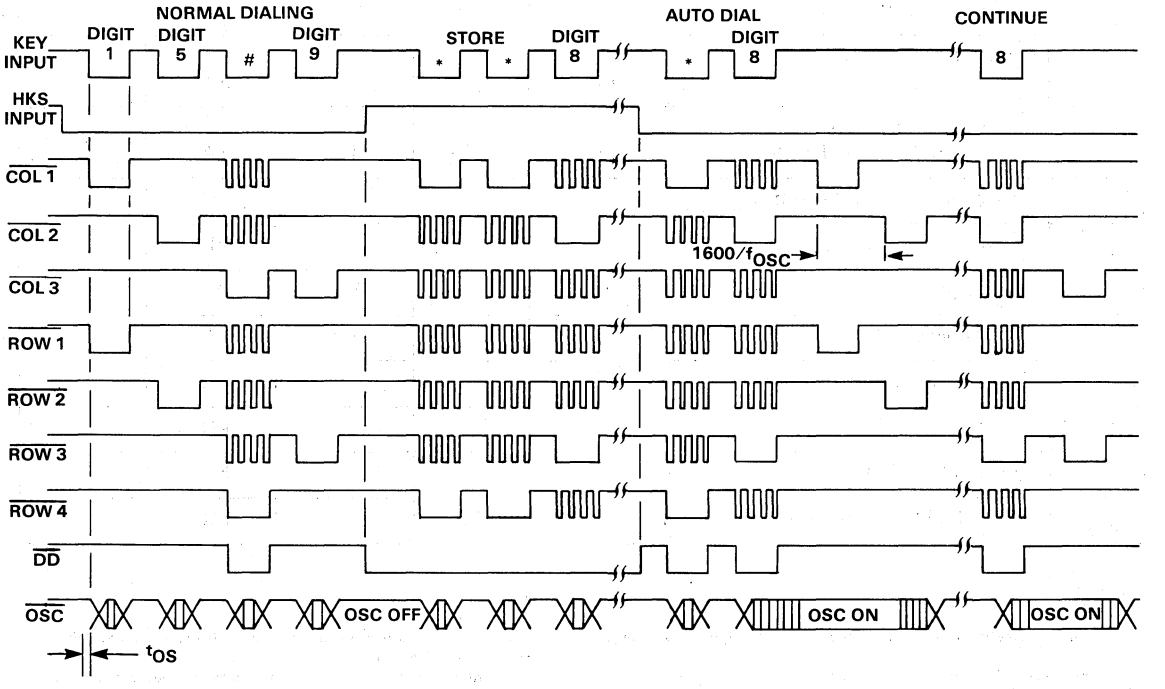
SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
f_{OSC}	Oscillator Frequency (antiresonant mode) (Pulse Mode)		480		kHz	1
t_{DB}	Keyboard Debounce Time		32		ms	2
t_{OS}	Oscillator Start-Up Time			8.0	ms	
P_R	Pulse Rate (Pulse Mode)		10.0		pps	
t_B	Break Time: Pin 9 Tied to V+/Tied to V- (Pulse Mode)		60/68		ms	
t_{IDP}	Interdigital Pause (Pulse Mode)		840		ms	
f_{OSC}	Oscillator Frequency (Tone Mode)		8.0		kHz	3
T_R	Tone Out Rate		$f_{OSC}/1600$		tones/sec	

NOTES

1. Ceramic resonator should have the following equivalent values: $R < 20\ \Omega$, $R_A \geq 70\ k\Omega$, $Co \leq 500$ pF.
2. A key entry must be present after 32 ms to be valid (oscillator on).
3. $f_{OSC} = 1/R_1C_1$, and for $R_1 = 250\ k\Omega$ and $C_1 = 500$ pF, $f_{OSC} = 8$ kHz

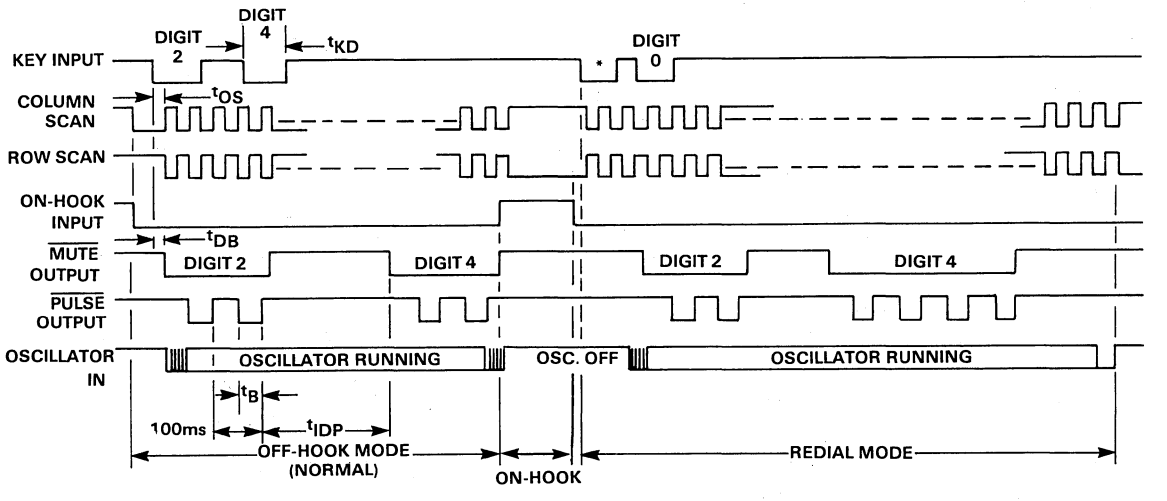
TIMING CHARACTERISTICS TONE MODE

Figure 4



TIMING CHARACTERISTICS PULSE MODE

Figure 5



TYPICAL APPLICATIONS

REPERTORY PULSE DIALER

The schematic diagram in Figure 6 shows one method which can be used to interface the MK5175 with the telephone line. In the approach shown, the MK5175 is in the pulse-dialer mode and the pulsing circuitry is in series with the speech network.

A current source of some type is desired to present a high impedance to the telephone line while guaranteeing sufficient current to power the MK5175 while off-hook and dialing. The current source shown is constructed using diodes D1 and D2, resistors R1 and R2, and transistor Q1 Other implementations, such as a constant current diode, may be considered.

A diode bridge is used to insure the proper voltage polarity for the MK5175, and hook switch S1 is used to connect the circuit to the telephone line. Hook switch S2 is used to provide the logic level necessary at Pin 15 to set the MK5175 in its off-hook mode.

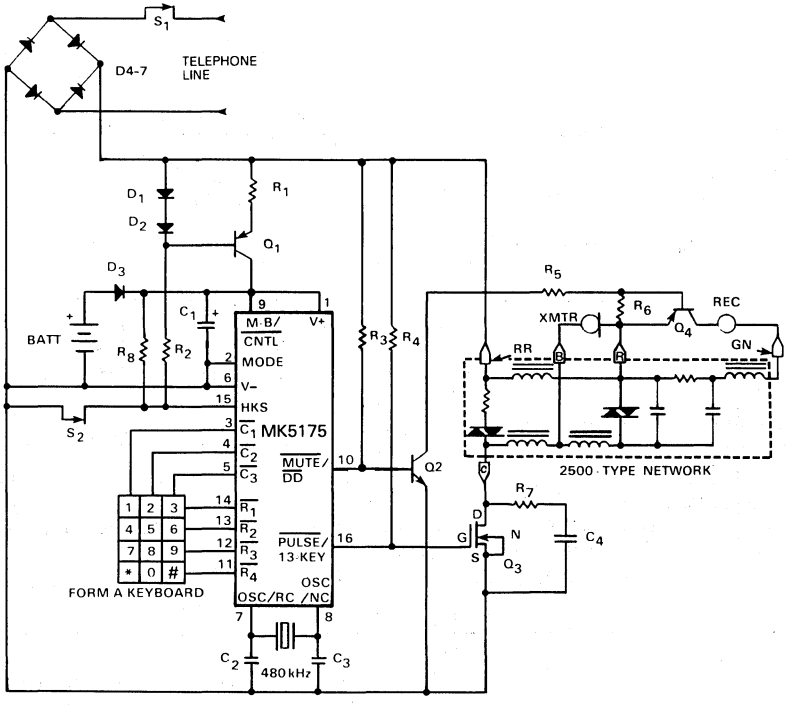
Pin 2 (MODE) is connected to V– to set the MK5175 in the Pulse dialer mode. In this mode, Pins 7 and 8 are defined as the oscillator pins and Pins 9, 10, and 16 are defined as M-B, $\overline{\text{Mute}}$, and $\overline{\text{Pulse}}$, respectively.

The $\overline{\text{Pulse}}$ and $\overline{\text{Mute}}$ outputs drive external transistors to perform the outpulsing function. Resistor R7 and capacitor C4 are connected across transistor Q3 for suppression of noise-producing sharp voltage rises generated during outpulsing. The receiver is connected to the speech network through transistor Q4. $\overline{\text{Mute}}$ causes the transistor to be held on until outpulsing begins. When $\overline{\text{Mute}}$ switches low, the receiver is removed from the network. The transients caused by breaking the line are then isolated from the receiver. The $\overline{\text{Pulse}}$ output drives transistor Q3 to make and break the line until the digit has been completely outpulsed. $\overline{\text{Mute}}$ then switches high, returning the receiver to the speech network.

A 3-volt battery has been included in the circuit to provide current to the MK5175 to retain the numbers stored in memory and to provide the power necessary for the on-hook entry and storage of numbers.

TYPICAL APPLICATION PULSE MODE

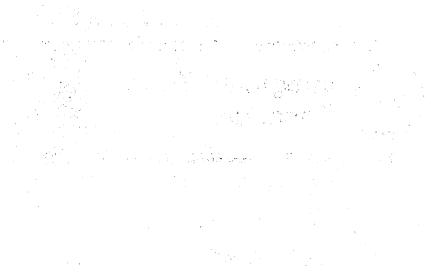
Figure 6



Q1, 4 = 2N5401	D1, 2 = 1N914	C2, 3 = 100 pF ± 20%	R4 = 4.7 MΩ
Q2 = 2N5550	D3 = 1N270	C4 = 0.1 μF	R5 = 3 kΩ
Q3 = 2N6660	D4-7 = 1N4004	R1 = 1.5 kΩ	R6 = 100 kΩ
BATT. = 3 V battery	C1 = 10 μF @ 16 V Low Leakage	R2 = 820 kΩ	R7 = 330 kΩ
S1,2 = Hook Switch		R3 = 470 kΩ	R8 = 100 kΩ

NOTE: Transient protection circuitry not shown.

1982 TELECOMMUNICATION PRODUCTS DATA BOOK



MOSTEK®

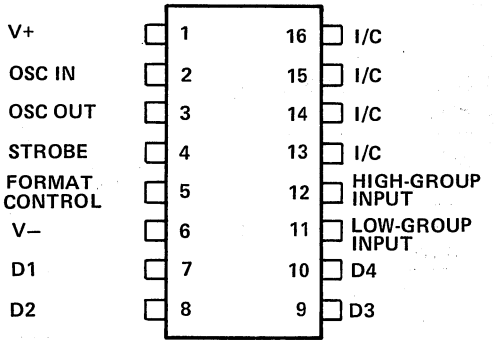
INTEGRATED TONE RECEIVER

MK5102(N)-5

FEATURES

- ☐ Detects all 16 standard DTMF digits
- ☐ Requires minimum external parts count for minimum system cost
- ☐ Uses inexpensive 3.579545 MHz crystal for reference
- ☐ Digital counter detection with period averaging insures minimum false response
- ☐ 16-pin package for high system density
- ☐ Single supply 5 Volts ± 10%
- ☐ Output in either 4-bit binary code or dual 2-bit row/column code
- ☐ Latched outputs

MK5102 PIN OUT



DESCRIPTION

The MK5102 is a monolithic integrated circuit fabricated using the complementary-symmetry MOS (CMOS) process. Using an inexpensive 3.579545 MHz television colorburst crystal for reference, the MK5102 detects and decodes the 8 standard DTMF frequencies used in telephone dialing. The requirement of only a single supply and its construction in a 16-pin package make the MK5102 ideal for applications requiring minimum size and external parts count.

The MK5102 detects the high and low group DTMF tones after band splitting using a digital counting method. The zero crossings of the incoming tones are counted over several periods and the results averaged over a longer period. When a minimum of 33 milliseconds of a valid DTMF digit is detected, the proper data is latched into the outputs and the output strobe goes high. When a valid digit is no longer detected, the strobe will return low and the data will remain latched into the outputs. Minimum interdigit time is 35 milliseconds.

The MK5102 is designed to interface with the MK5099 Integrated Pulse Dialer with only one additional DIP Package. These two parts working together form a DTMF-to-Pulse converter that meets the recognized telephone standards.

ABSOLUTE MAXIMUM RATINGS*

DC Supply Voltage V+ (Referenced to V–) . . . . . +6.0 Volts
Operating Temperature . . . . . 0°C to 70°C
Storage Temperature . . . . . –55°C to 100°C
Maximum Circuit Power Dissipation . . . . . 300 mW
Voltage on any pin, with respect to V– . . . . . –0.3 Volt
Voltage on any pin, with respect to V+ . . . . . +0.3 Volt

*Operation Above Absolute Maximum Ratings May Damage The Device

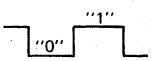
ELECTRICAL CHARACTERISTICS

0° C ≤ T_A ≤ 70° C V– = 0 Volts

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage (V+)	(V– = 0)	4.5		5.5	Volts	
Lo Group & Hi Group Inputs	50% Duty Cycle Square Wave	0.9		V+	Volts Peak-to-Peak	1,2
STROBE D1, D2, D3, D4 OUTPUTS	"0" Level	0.0		0.4	Volt @ 1.6 mA	
	"1" Level	(V+)–1		V+	Volts @ 0.1 mA	
FORMAT CONTROL Input	"0" Level	0.0		0.5	Volt @ 700μA	
	"1" Level	(V+)–0.5		V+	Volt @ 700μA	
Frequency Detect Band Width		± 2.0	± 2.5	± 2.9	% of f_o	
Tone Coincidence Duration		33			ms	4
Interdigit Interval		35			ms	4
Signal to Noise Ratio		18			dB	3
Supply Current @ 5.5V	Inputs and Outputs Unloaded		5	10	mA	

NOTES:

1. Due to internal biasing, this input must be capacitively coupled with a low leakage .05 μF capacitor.
2. No coupling capacitor is needed if the DTMF square wave meets the following criteria:



   a. Logic "0" level = 1 Volt (max)
   b. Logic "1" level = 4 Volts (min)

3. Signal-To-Noise Ratio is defined as:
   $SN = 20 \log \frac{SA}{NA}$
   where SA = RMS Amplitude of single tone being detected.
   NA = RMS white noise in the band from 300Hz to 3.4KHz.
4. Tone coincidence duration and interdigit interval measured at High- and Low-group inputs. Filter and/or limiter or comparator characteristics will affect the overall detect time.

OSCILLATOR

The MK5102 contains an on-board inverter with sufficient gain to provide oscillation when working with a low cost television "color burst" crystal. The inverter input is OSC IN (pin 2) and output is OSC OUT (pin 3). The circuit is designed to work with a crystal cut to 3.579545 MHz to give detection of the standard DTMF frequencies.

FORMAT CONTROL (PIN 5)

The Control pin is used to control the output format of Pins D1 through D4. This three-state input selects a 4-Bit Binary Code, a Dual 2-Bit Row/Column code, or high-impedance output for use with bus-structured circuitry. This three-state input is controlled as follows:

FORMAT CONTROL INPUT	OUTPUT DATA FORMAT
V–	High Impedance
V+	4-Bit Binary
Floating	Dual 2-Bit Row/Column

FORMAT CONTROL (Continued)

The following table describes the two output codes.

Table 1

	4-Bit Binary				Dual 2-Bit Row/Column			
					Row		Column	
Digit	D1	D2	D3	D4	D1	D2	D3	D4
1	0	0	0	1	0	1	0	1
2	0	0	1	0	0	1	1	0
3	0	0	1	1	0	1	1	1
4	0	1	0	0	1	0	0	1
5	0	1	0	1	1	0	1	0
6	0	1	1	0	1	0	1	1
7	0	1	1	1	1	1	0	1
8	1	0	0	0	1	1	1	0
9	1	0	0	1	1	1	1	1
0	1	0	1	0	0	0	1	0
*	1	0	1	1	0	0	0	1
#	1	1	0	0	0	0	1	1
A	1	1	0	1	0	1	0	0
B	1	1	1	0	1	0	0	0
C	1	1	1	1	1	1	0	0
D	0	0	0	0	0	0	0	0

Figure 1 shows the relationship between the data output code shown in Table 1 and the standard DTMF keyboard.

DTMF DIALING MATRIX

Figure 1

	Col 1	Col 2	Col 3	Col 4
Row 1	1	2	3	A
Row 2	4	5	6	B
Row 3	7	8	9	C
Row 4	*	0	#	D

Note: Column 4 is for special applications and is not normally used in telephone dialing.

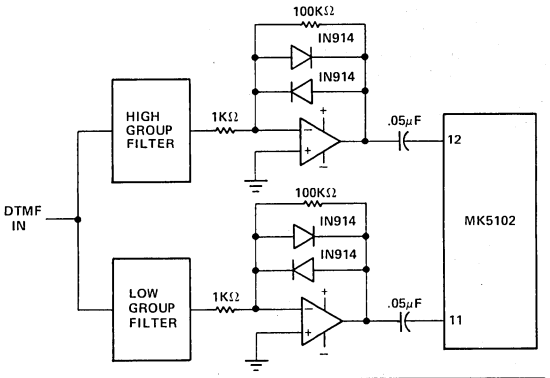
DETECTION FREQUENCY

Table 2

Low Group f_o	High Group f_o
Row 1 = 697 Hz	Column 1 = 1209 Hz
Row 2 = 770 Hz	Column 2 = 1336 Hz
Row 3 = 852 Hz	Column 3 = 1477 Hz
Row 4 = 941 Hz	Column 4 = 1633 Hz

SUGGESTED INPUT LIMITER CIRCUIT

Figure 2



OUTPUTS D1 THRU D4 (PINS 7 THRU 10)

Outputs D1 thru D4 are CMOS push-pull when enabled and open-circuited (high impedance) when disabled by the format control pin.

D1 thru D4 are the data out lines. The output data can be in two formats as described in the section about the format control pin (pin 5).

The Dual 2-Bit Row/Column code decodes with D1 and D2 indicating the row selected, and D3 and D4 indicating the column selected.

The two output codes allow the user to obtain either 1-of-16 or 2-of-8 output data by using only a single additional package.

I/C (PINS 13 THRU 16)

Pins 13 thru 16 are internally connected and are intended to be left floating.

STROBE (Pin 4)

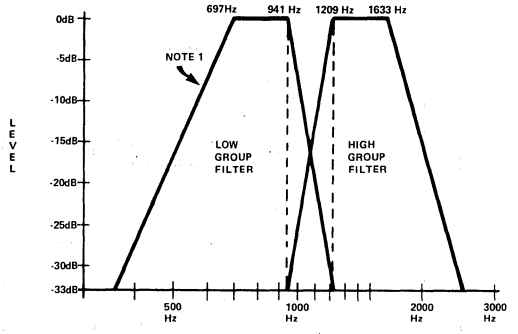
The STROBE output goes to a "1" when 33 miliseconds of a valid DTMF signal is detected and remains at a "1" until an interdigit interval has been detected. The data at D1-D4 are already valid when STROBE goes to a "1" and will remain unchanged until the next DTMF digit is detected.

LOW-GROUP INPUT (Pin 11) and HIGH-GROUP INPUT (Pin 12)

The low- and high-group inputs are comparators that can detect capacitively-coupled square-wave signals as small as 0.9 volts peak-to-peak. The circuitry driving these inputs would typically use back-to-back silicon diodes as symmetrical limiters to regulate this level.

These inputs are biased to the midpoint of the supply with a resistive divider. Nominal input impedience is 100K Ω.

INPUT BAND SPLIT REQUIREMENTS



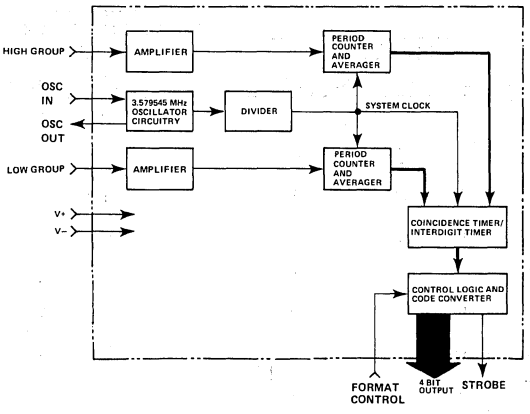
RELATIVE INPUT LEVEL VS FREQUENCY

NOTES:

1. Dial tone notch filter adequate to maintain S/N ratio of $\geqslant$ 18dB in above pass bands.

2. Filter response described above will normally result in operation to 6dB of twist with 18dB S/N.

MK5102 BLOCK DIAGRAM



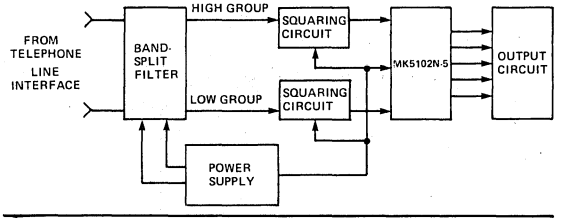
This application note will describe all of the requirements for building a high-quality DTMF receiver using the MK5102N-5 and hybrid filters. The following topics will be discussed:

1. Power supply requirements
2. Band separation filter requirements
3. Squaring circuit requirements
4. Squaring circuit-to-decoder coupling requirements
5. Receiver testing
6. Output formatting
7. Other system considerations

Since the MK5102N-5 is intended to be a portion of a tone receiver SYSTEM, SYSTEM requirements must be met before a satisfactory decoder can be constructed. A block diagram of a typical system is shown in Figure 1. Each portion of the block diagram is discussed in succeeding paragraphs.

TYPICAL DTMF RECEIVER

Figure 1



POWER SUPPLY REQUIREMENTS

For proper operation of the MK5102N-5, the V+ power supply must be between 4.5 VDC and 5.5 VDC, with V- grounded. A power supply decoupling capacitor (typically .1uF) should be connected between V+ and V- to insure that no high-frequency noise is present on the V+ supply. Typically, a 1-volt peak-to-peak signal may be applied to V+ and the MK5102N-5 will function properly.

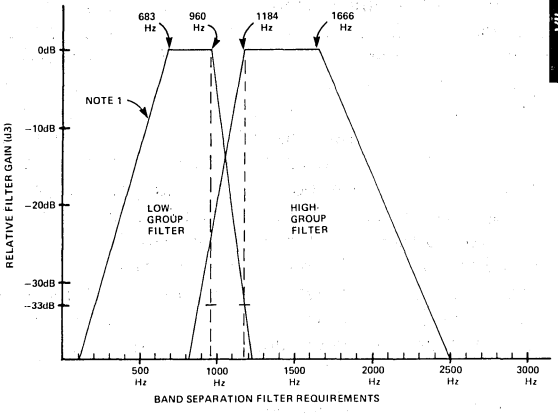
FILTER REQUIREMENTS

For proper operation of the MK5102N-5, an external band separation filter must be provided to split the DTMF signal into its high-group and low-group components. However, the band separation requirements are not as stringent for the MK5102N-5 as they are for competing designs. As shown in figure 2, the MK5102N-5 requires a band separation of only 33dB in an average application. The 33dB requirement allows for a S/N ratio of 18dB, 6dB of twist, and a detection bandwidth of at least ± 2%. A reduction of twist margin or S/N requirements will result in a corresponding lower requirement for band separation. For example, if there is not a requirement for twist margin, the band separation can be reduced to 27dB. In a system with no noise and no twist, the band separation can be 22dB.

The plot shown in Figure 2 depicts corner frequencies of 683Hz, 960Hz, 1184Hz and 1666Hz. These represent a 2% deviation from the DTMF frequencies of 697Hz, 941Hz, 1209Hz and 1633Hz, respectively. This deviation is necessary because of the requirement that a DTMF receiver must detect frequencies which are 2% higher or lower than the nominal DTMF frequency. Table 1 lists the 8 DTMF frequencies and the corresponding frequencies which a DTMF decoder is required to detect.

BAND SEPARATION FILTER REQUIREMENTS

Figure 2



NOTES:

1. Dial tone notch filter must maintain S/N ratio ≥ 18dB
2. Filter response shown will allow operation to 6dB of twist with 18dB S/N.

TABLE I

8 STANDARD DTMF FREQUENCIES AND CORRESPONDING UPPER AND LOWER REQUIRED DETECTION FREQUENCIES

DTMF FREQUENCY (HZ)	LOWER DETECTION FREQUENCY LIMIT (HZ)	UPPER DETECTION FREQUENCY LIMIT (HZ)
697	683	711
770	755	786
852	834	869
941	922	960
1209	1184	1233
1336	1309	1363
1477	1447	1507
1633	1600	1666

DETECTION ALGORITHM

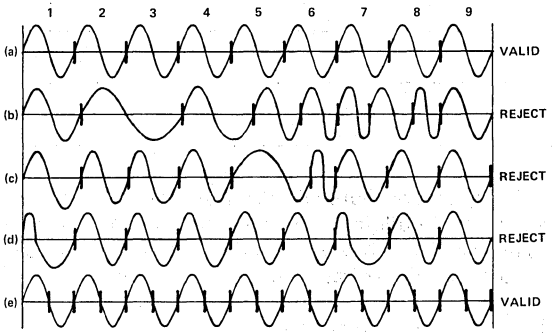
The detection approach used in the MK5102N-5 utilizes zero-crossing detection and digital period-counting. To increase the rejection of random noise and the residue from out-of-band components, an averaging scheme is used. Figure 3(a) shows nine cycles of a symmetrical sine wave. If zero-crossings were the only detection criteria, and if the average period-count obtained over nine periods were acceptable, then the signal in Figure 3(a) represents a valid tone. The jitter of the zero-crossings is integrated out by the nine-period average. However, based on the simple nine-period average, the signal shown in Figure 3(b) would be accepted as a valid tone. To improve rejection of this speech-type waveform, the nine-period detection time can be broken into three period-averaged sub-groups as indicated by the dashed lines in Figure 3(b). By combining the nine-period average and the sub-group average criteria, 200 false hits are obtained on 30 minutes of a standard speech tape. Figure 3(c) represents a type of waveform that would produce a hit based on the nine-period and sub-group average algorithm. To improve rejection of this waveform, requirements must be placed on every single period in addition to the nine-period average and the sub-group average. However, the waveform of Figure 3(d) will be detected using only these three criteria. Therefore an additional requirement must be placed on each half-period of the waveform. Figure 3(e) shows the only type of signal which will be accepted by a detection algorithm which requires the following:

1. Valid nine-period average
2. Three valid sub-group averages
3. Valid single-period
4. Valid half-period

Using these four criteria, the number of hits on a standard speech tape can be reduced to less than six.

POSSIBLE INPUT WAVEFORMS

Figure 3

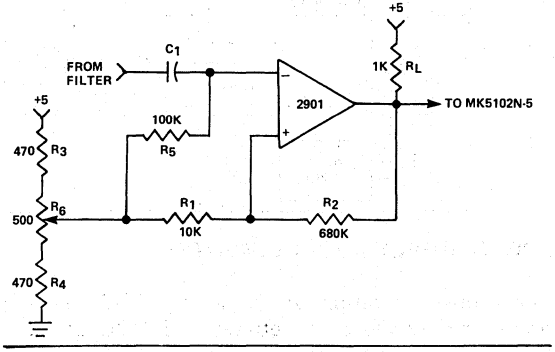


INPUT SQUARING CIRCUITS

As described above, to minimize the number of false hits, a detection algorithm must place stringent requirements on each half-period of the input waveform (high group or low group). To successfully meet these requirements, the duty cycle of the input waveform must be between 49% and 51%. The input squaring circuit must therefore provide an output which accurately tracks the input without adversely affecting the duty cycle. Such a circuit, an inverting comparator with hysteresis, is illustrated in Figure 4.

INPUT SQUARING CIRCUIT

Figure 4



C_1 is used to ac couple the filter output to the squaring circuit so that DC bias present at the filter output will not affect the performance of the squaring circuit. R_3, R_4, and R_6 establish a bias level at about 2.5 Volts, and R_5 is used to provide the same bias level at the inverting input of the comparator used in the squaring circuit. The maximum input bias current for the LM2901 is 500nA, so the DC bias level at the inverting input is effectively the same as the voltage at the wiper of R_6. R_6 must be adjusted so that, for an input signal level of -28dBm, the output duty cycle will be 50%. This adjustment compensates for

the input offset voltage of the LM2901. R_L is the pullup resistor for the open-collector output of the comparator. R_1 and R_2 set the hysteresis level. Their values are determined by the following approximate relationships:

$$V_{UT} = 2.5 + \frac{(2.5)(R_1)}{(R_1 + R_2 + R_L)}$$

where V_{UT} is the upper threshold

$$V_{LT} = \frac{(2.5 - V_{OL})(R_2)}{(R_1 + R_2)}$$

where V_{LT} is the lower threshold and V_{OL} is the output saturation voltage

In both cases, any variation due to the current in R_5 is ignored.

For central office applications, the tone receiver system must operate over an input signal level range of -26dBm to +6dBm. The squaring circuit, therefore, must respond to signal levels of -26dBm or greater but is not required to respond to lower signal levels.

To allow for signal attenuation through the band separation filter, the squaring circuit should be set to respond to signal levels of -28dBm or greater. The -28dBm cutoff point corresponds to a peak-to-peak voltage of 87.1mV. For a 50% duty-cycle output waveform, V_{UT} should be set 43.5mV above and V_{LT} should be set 43.5mV below the DC bias point. The passive components for the squaring circuit are then selected as follows:

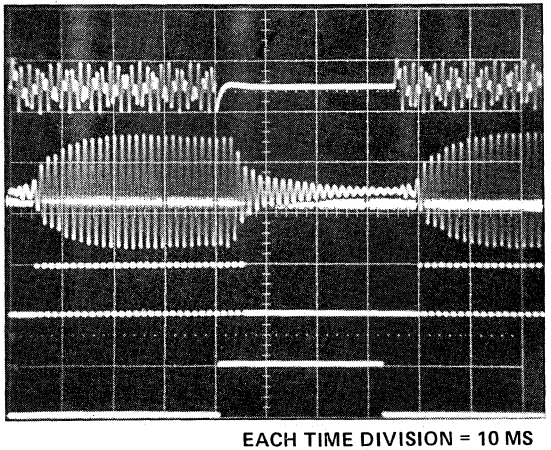
$R_L = 1k\Omega$	Chosen value.
$R_2 = 680k\Omega$	Chosen value.
$R_1 = 12k\Omega$	Calculated value.
$R_3 = R_4 = 470\Omega$	Chosen value for DC bias.
$R_5 = 100k\Omega$	Chosen value. Tradeoff effect on DC bias vs. drop across R_5 due to 2901 input bias current.
$C_1 = 1\mu F$	Chosen value. Must be low impedance over frequency range of 683Hz to 1666Hz.

To achieve proper operation at low signal levels, R_1 must be 10kΩ. The discrepancy between the calculated value and the actual required value results from component tolerances.

Since many commercially-available filters exhibit a ringing characteristic at their output, as shown in Figure 5 and Figure 6, additional circuitry is required to detect the beginning of ringing and squelch the output of the squaring circuit. The required circuitry, an envelope detector, is shown in Figure 7. The detector consists of two precision rectifiers, two sample-and-hold circuits, and a comparator. C_3 is used to couple the low-group filter output to the envelope detector. Z1a, D_1, C_1, R_2, and R_3 then rectify the incoming signal and store a peak value. The $R_2/R_3/C_1$ time constant is set for 20ms so that the voltage at the inverting input of Z_2 will represent ½ the peak value of the incoming signal. Z1b, D_2, R_1 and C_2 also rectify the incoming signal and store a peak value, but the time constant is set for 1.4ms so that the voltage at the non-inverting input of Z_2 will represent the instantaneous peak value of the incoming waveform. As long as the instantaneous value is greater than ½ of the peak value, the comparator output will be high. However, as soon as the instantaneous value decreases to less than ½ the peak value (this will occur as ringing begins), the comparator output will go low and inhibit the output of the squaring circuit. It is necessary to provide only one envelope detector since the MK5102N-5 will treat the absence of a valid low-group/high-group tone combination as interdigit time.

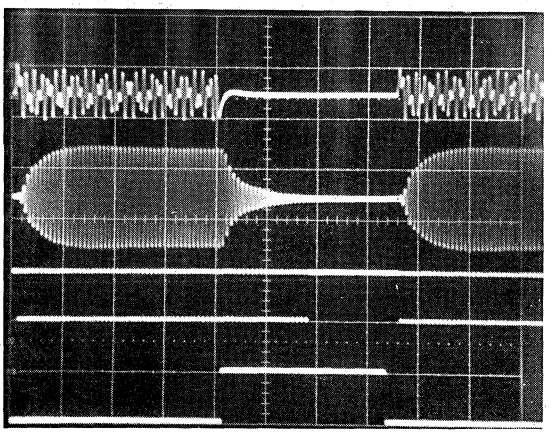
LOW-GROUP FILTER RESPONSE (3044)

Figure 5



HIGH–GROUP FILTER RESPONSE (3045)

Figure 6



EACH TIME DIVISION = 10 ms

DTMF INPUT TO FILTER (5V/DIV.)

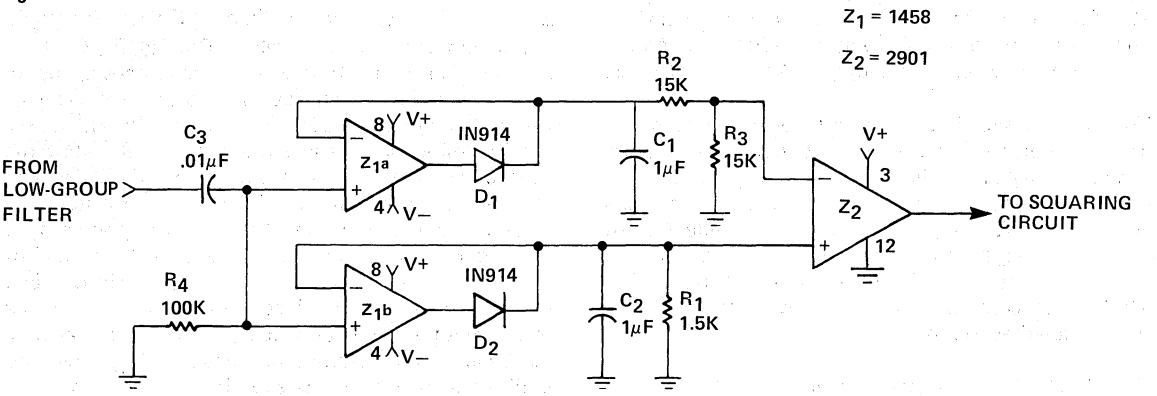
LOW-GROUP
FILTER OUTPUT (IV/DIV.)

SQUARING CIRCUIT
OUTPUT (5V/DIV.)

STROBE FROM MK5102N-5
(5V/DIV.)

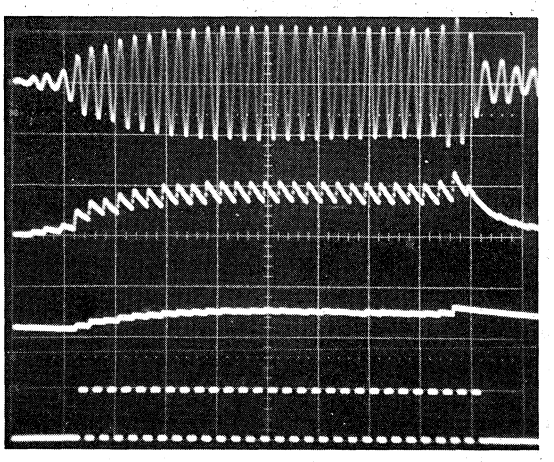
ENVELOPE DECAY DETECTOR

Figure 7



ENVELOPE DETECTOR OPERATION

Figure 8



LOW-GROUP
FILTER OUTPUT (IV/DIV.)

INSTANTANEOUS PEAK
DETECTOR (IV/DIV.)

AVERAGE PEAK
DETECTOR (IV/DIV.)

LOW-GROUP INPUT
TO 5102N-5 (5V/DIV.)

SQUARING CIRCUIT-TO-DECODER COUPLING

The output of the squaring circuit may be tied directly to the MK5102N-5 if it meets the following requirements:

Logic 1 ⩾ 4 volts
Logic 0 ⩽ 1 volt

A squaring circuit with an output that does not meet these requirements must be capacitively coupled to the MK5102N-5 with a 0.05μF capacitor. The value of the coupling capacitor is critical because of the impedance of the bias circuit at the high-group or low-group input. As shown in Figure 9, the sudden appearance of a tone burst causes the DC bias point to shift upward. Until the DC bias returns to its normal level, the input comparator will not switch and the input signal will be ignored, causing an increase in the dual-tone detection time. Using a 0.05μF capacitor will minimize the effect of this DC level shift. The peak-to-peak value of the coupled signal must be greater than .9 volts but less than V+ volts.

OUTPUT SIGNALS

D1, D2, D3, and D4 are the data output lines. The output format present on these pins is determined by the format control (pin 5) as shown in Table 2.

FORMAT CONTROL FUNCTIONS
TABLE 2

Format Control Input	Data Output Format
V–	High Impedance
V+	4-Bit Binary
Floating	Dual 2-Bit Row/Column

SHIFT IN DC BIAS LEVEL CAUSED BY APPLICATION OF TONE BURST

Figure 9

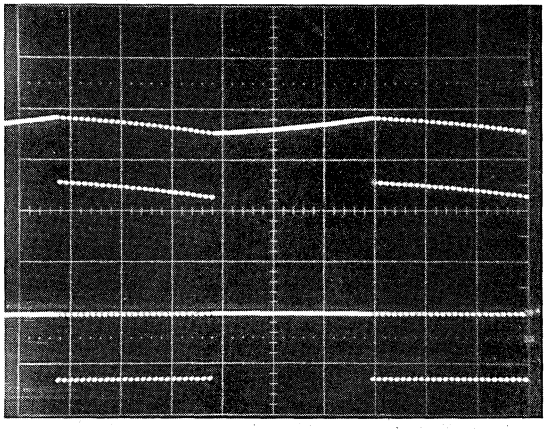


Table 3 describes the two output codes available.

TABLE 3

OUTPUT FORMAT

			4-Bit Binary				Dual 2-Bit Row/Column			
							Row		Column	
Key	Row	Col.	D1	D2	D3	D4	D1	D2	D3	D4
1	1	1	0	0	0	1	0	1	0	1
2	1	2	0	0	1	0	0	1	1	0
3	1	3	0	0	1	1	0	1	1	1
4	2	1	0	1	0	0	1	0	0	1
5	2	2	0	1	0	1	1	0	1	0
6	2	3	0	1	1	0	1	0	1	1
7	3	1	0	1	1	1	1	1	0	1
8	3	2	1	0	0	0	1	1	1	0
9	3	3	1	0	0	1	1	1	1	1
0	4	2	1	0	1	0	0	0	1	0
*	4	1	1	0	1	1	0	0	0	1
#	4	3	1	1	0	0	0	0	1	1
A	1	4	1	1	0	1	0	1	0	0
B	2	4	1	1	1	0	1	0	0	0
C	3	4	1	1	1	1	1	1	0	0
D	4	4	0	0	0	0	0	0	0	0

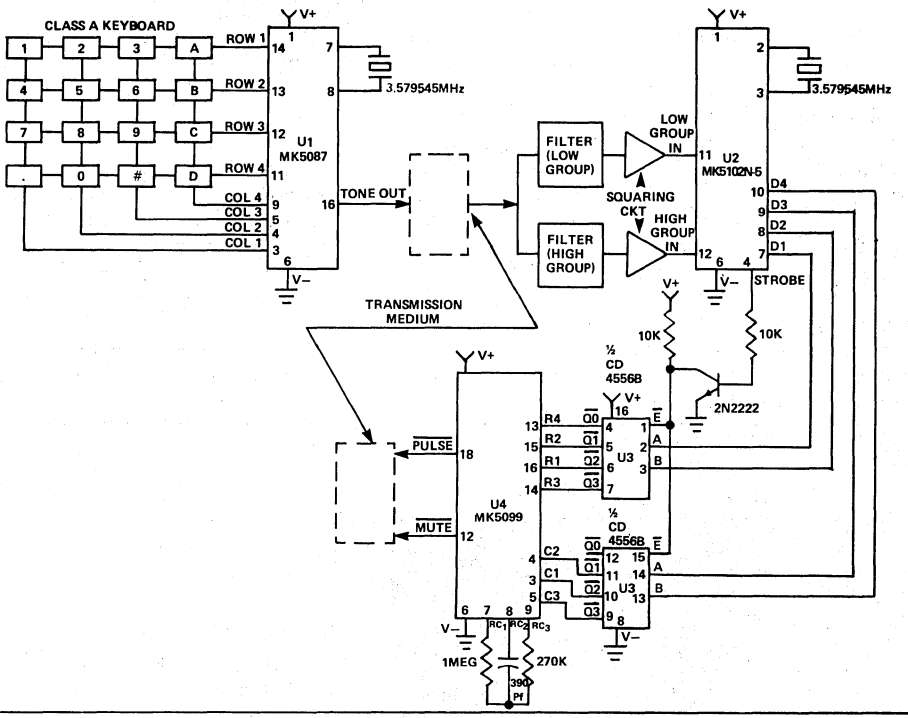
When all detection criteria are present, the MK-5102N-5 will latch the proper data into its outputs and strobe will go high. After an interdigit time has been detected, strobe will go low, but the data will remain on D1 through D4.

The dual 2-bit row/column code is useful when interfacing a key-to-pulse converter, as shown in Figure 10. On this circuit, the MK5102N-5, CD4556 and MK 5099 combine to form a tone-to-pulse converter, which allows the use of DTMF telephones in rotary exchanges. The DTMF tones are detected by the MK 5102N-5, which then generates the corresponding row/column code. Each CD4556 then uses this 2-bit code to select 1 of 4 active-low outputs. The MK5099 then interprets these signals as a valid key closure and generates a corresponding series of pulses.

For simple remote-control applications, the circuit of Figure 11 is useful. After a valid tone is detected, strobe will go high and one of the 16 outputs on the binary-to-1-of-16 encoder will go true. Thus, a DTMF transmitter and 16-key keyboard can be used to control 1 of 16 functions in a DTMF receiver. Each control pulse will have its width controlled by Strobe.

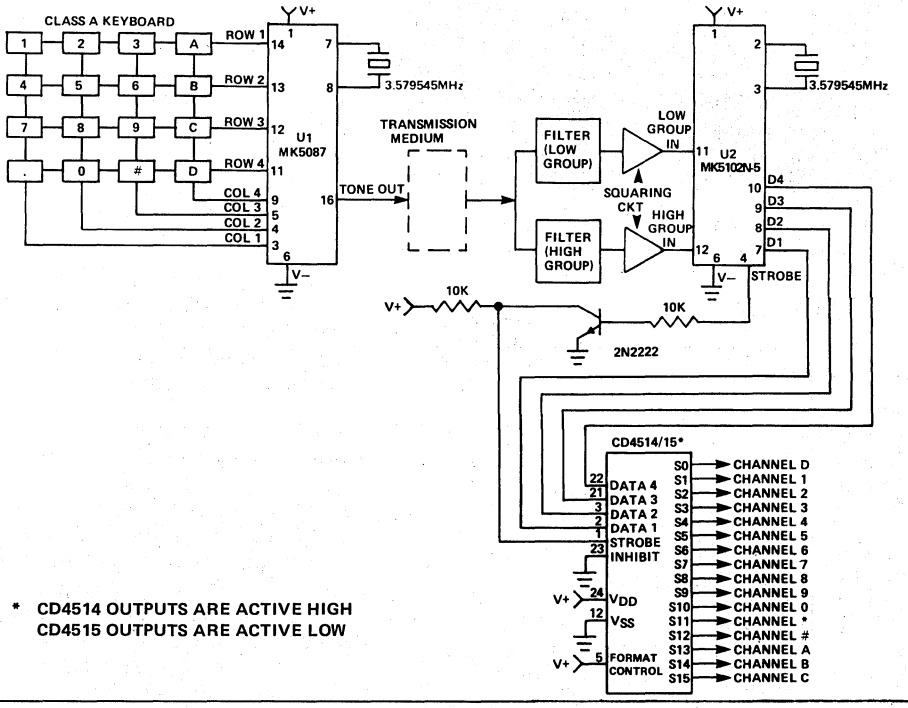
TONE-TO-PULSE CONVERTER

Figure 10



16-CHANNEL REMOTE CONTROL

Figure 11



* CD4514 OUTPUTS ARE ACTIVE HIGH
CD4515 OUTPUTS ARE ACTIVE LOW

RECEIVER TESTING

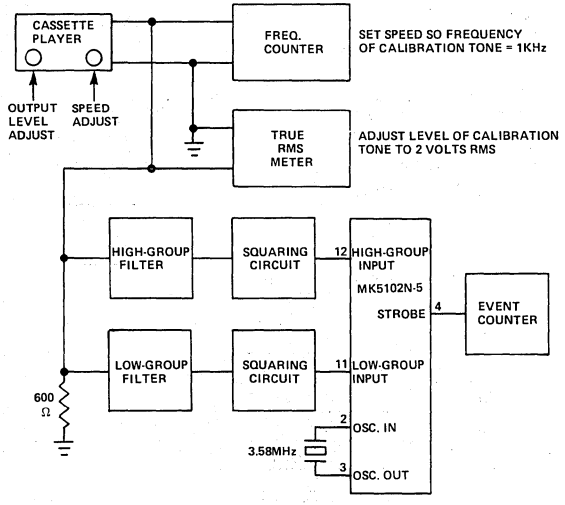
Equipment connections for testing a DTMF receiver are shown in Figure 12. The setup consists of a cassette player (ideally with a speed adjustment), a digital frequency counter, and a voltmeter. A Mitel CM7290 Tone Receiver Test Cassette was used in all the receiver tests described below. This cassette checks receiver detection bandwidth, maximum acceptable amplitude ratio (twist), receiver guard time, dynamic range and acceptable signal-to-noise ratio. It also evaluates the receiver talk-off rate with a condensed speech recording equivalent to many hours of receiver exposure. The CM7290 is available from Mitel at the locations listed.

Mitel International
Shannon Industrial Estate
Shannon, Ireland
Telephone. 061-61433
Telex: 32208

Mitel Corp.
P.O. Box 13089 Kanata
Ottawa, Ontario, Canada
K2K1X3
Telephone: 613-592-2122
Telex: 053-4596
Cable Mitelcan
Twx: 610-562-8529

Mitel Inc.
St. Lawrence Industrial Park
Ogdensburg, New York 13669
Telephone: 315-393-1212
Twx: 510-259-4071

EQUIPMENT CONNECTIONS FOR RECEIVER EVALUATION
Figure 12



There are several considerations in setting up a receiver test. First, the recorder should have a speed adjustment and an output level adjustment. Each side of the CM7290 contains a 1kHz calibration tone. To set up properly for the test, the speed of the recorder should be adjusted so that the tone frequency is 1kHz and the cassette player output level should be adjusted to 2 volts RMS. The cassette player must be able to provide the 2-volt output level without clipping. If a speed adjustment is not available, printed instructions included with the CM7290 provide a formula for correcting some of the test results. Second, the strobe output of the MK5102N-5 should be tied to the input of the event counter and the counter's sensitivity input adjusted so as to prevent false triggering. This can easily be done by repeating test 2a on the CM7290 until consistent results are obtained. Third, any sources of environmental noise (electric motors, speed controls, etc) should be eliminated so that they will not introduce count errors on the event counter.

FILTER EVALUATION

Two commercially-available filters, the CH1295 and CH1296 from Cermetek and the 3044 and 3045 from ITT North Electric Microsystems, were evaluated. The addresses of these two filter vendors are listed below:

Cermetek, Inc.
660 National Avenue
Mt. View, CA 94043
Telephone: 415-969-9433
Twx: 910-379-6931

ITT North Microsystems Division
700 Hillsboro Plaza
Deerfield Beach, FL 33441
Telephone: 305-421-8450
Twx: 510-953-7523

Figure 13 and Table 5 show the test circuit and test results for the Cermetek filters. The test circuit and test results for the North Electric filters are shown in Figure 13 and Table 4. The tests were performed using the equipment setup shown in Figure 12. Figures 14 through 17 show the spectral response of the filters.

TEST CIRCUIT FOR CERMETEK AND NORTH ELECTRIC FILTERS

Figure 13

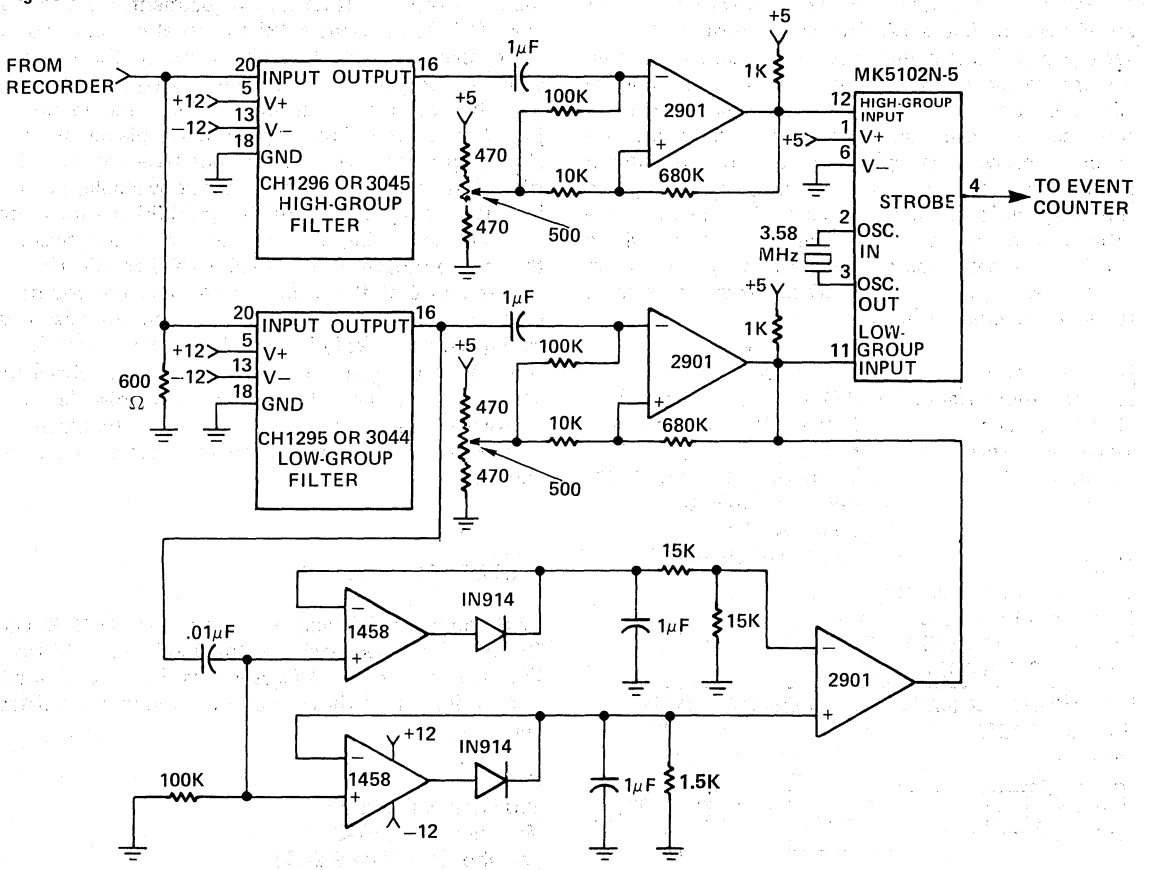


TABLE 4
MITEL TAPE TEST RESULTS FOR NORTH ELECTRIC FILTERS

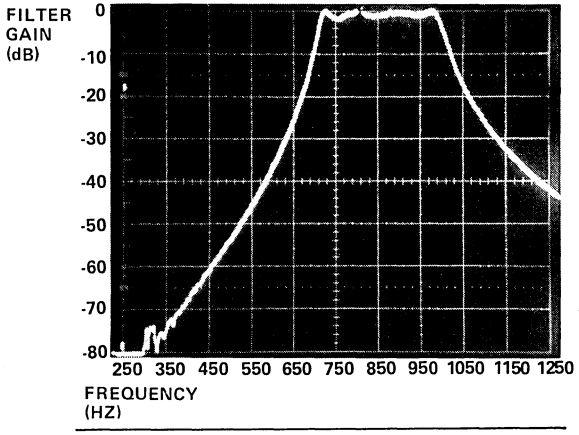
TEST#	RESULTS
2a, b	BW = 4.7 % of fo
2c, d	BW = 5.2 % of fo
2e, f	BW = 5.1 % of fo
2g, h	BW = 5.1 % of fo
2i, j	BW = 5.1 % of fo
2k, l	BW = 4.9 % of fo
2m, n	BW = 5.5 % of fo
2o, p	BW = 5.0 % of fo
3	159 decodes
4	Acceptable Amplitude Ratio = 13.1dB
5	Dynamic Range = 31.33 dB
6	Guard Time = 34.23 ms
7	99.8 % Successful Decode at N/S Ratio of -12dbV
8	3 Hits on Talk-Off Test

TABLE 5
MITEL TAPE TEST RESULTS FOR CERMETEK FILTERS

TEST#	RESULTS
2a, b	BW = 5.6 % of fo
2c, d	BW = 5.7 % of fo
2e, f	BW = 5.0 % of fo
2g, h	BW = 5.3 % of fo
2i, j	BW = 5.2 % of fo
2k, l	BW = 5.0 % of fo
2m, n	BW = 5.5 % of fo
2o, p	BW = 5.0 % of fo
3	158 decodes
4	Acceptable Amplitude Ratio = 12.6dB
5	Dynamic Range = 31.67 dB
6	Guard Time = 33.4 ms
7	98.33 % Successful Decode at N/S Ratio of -12dbV
8	3 Hits on Talk-Off Test

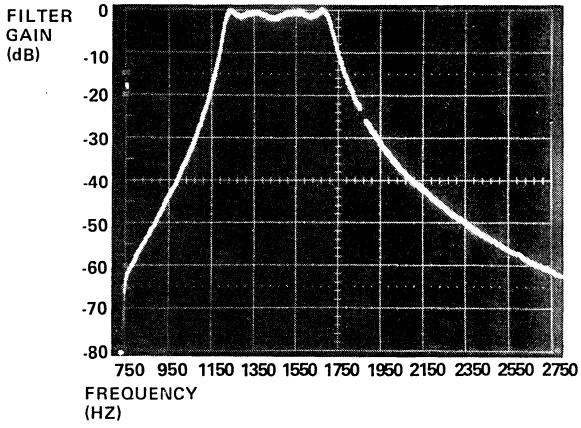
SPECTRAL RESPONSE OF CH1295 LOW-GROUP FILTER

Figure 14



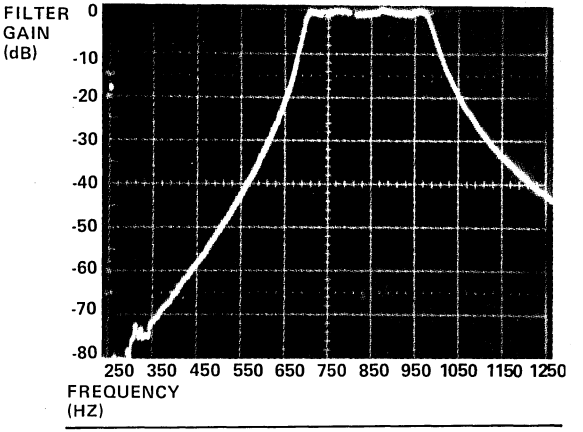
SPECTRAL RESPONSE OF CH1296 HIGH-GROUP FILTER

Figure 15



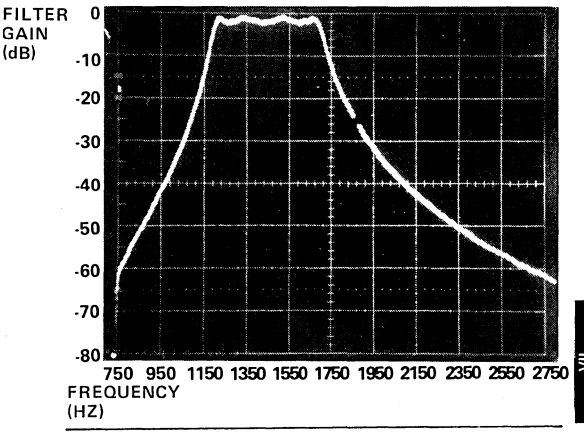
SPECTRAL RESPONSE OF 3044 LOW-GROUP FILTER

Figure 16



SPECTRAL RESPONSE OF 3045 HIGH-GROUP FILTER

Figure 17



OTHER SYSTEM CONSIDERATIONS

System noise will affect the operation of the MK5102N-5 by causing the detection bandwidth to shrink. The instantaneous value of the low-group or high-group waveform is represented by the following approximate relationship, $a = a_T \sin w_T t + a_N \sin w_N t$, where a is the instantaneous amplitude of the overall waveform, a_T is the amplitude of the high-group or low-group component, and a_N is the amplitude of the noise. If the highly-simplified noise term ($a_N \sin w_N t$) were removed, then the remaining term would represent a pure sine wave and the zero crossings of the waveform would be repeatable from cycle to cycle. All detection criteria would be present and the DTMF tone would be detected within a ± 2.0% to ± 2.9% bandwidth. However, adding the noise term introduces instantaneous amplitude variations which will effectively alter the duty cycle of the sine wave by causing the zero crossing points to jitter. If 0.5% jitter is caused by system noise, detection bandwidth will be decreased by .5%. Therefore, as the system noise level increases, the detection bandwidth will decrease.

As noted in the Filter Requirements paragraph, the 33dB band separation requirement allows for a S/N ratio of 18dB, with 6dB of twist, which means that the algorithm in the MK5102N-5 has been set up to provide a ± 2% minimum detection bandwidth in the presence of noise which is 18dB below the signal level and in the presence of high-group and low-group signals with an amplitude difference of 6dB.

SUMMARY

The MK5102N-5 provides a high-performance solution for DTMF detection at a lower cost than competing approaches. Band separation requirements for the MK5102N-5 are not as stringent as for competing designs, and, as was seen in the test results of Table 4 and Table 5, the MK5102N-5 provides excellent talk-off rejection. When used in conjunction with either the Cermetek or the North Electric filters, the MK5102N-5 will give the user a high-quality DTMF receiver which may be used in myriad applications.

MOSTEK®

TELECOMMUNICATION PRODUCTS

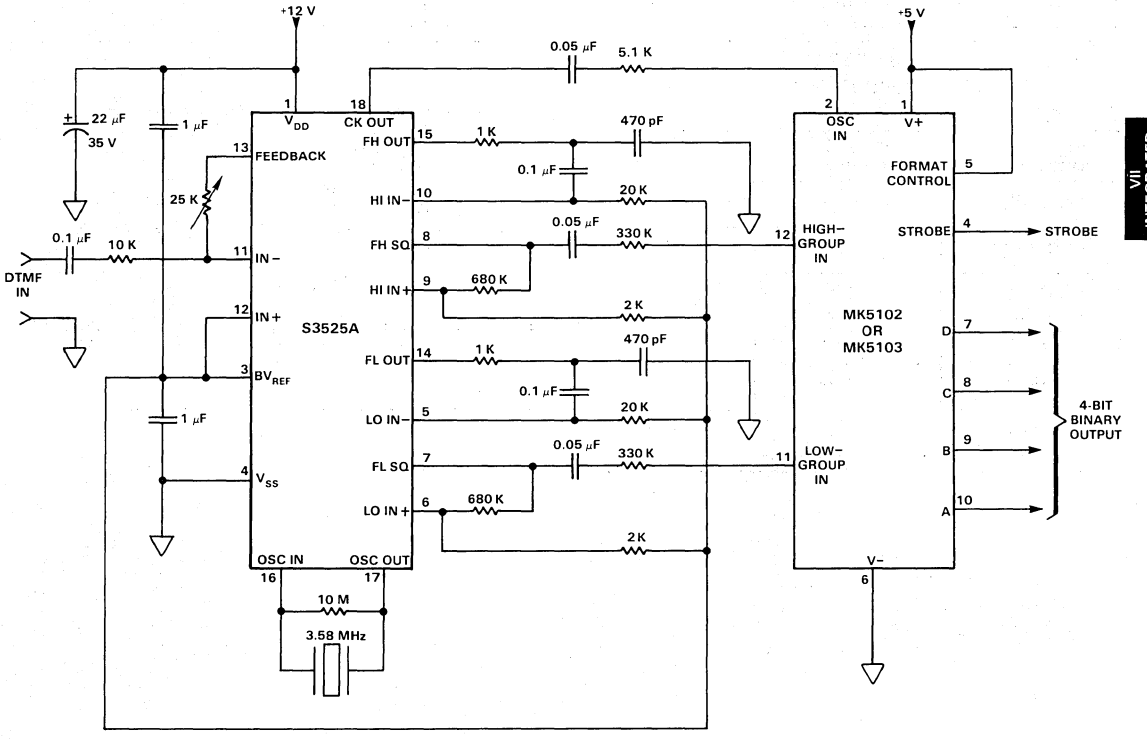
MK5102/S3525A
DTMF Receiver System

An inexpensive DTMF receiver system with a low parts count may be constructed using the Mostek MK5102 or MK5103 Tone Decoder with the AMI S3525A Bandsplit Filter. The S3525A is an 18-pin monolithic CMOS switched-capacitor filter. It uses a 3.58 MHz crystal as a time base and has a buffered clock output to drive the oscillator of the MK5102/3. The S3525A also has on-chip comparators which can be used to construct adjustable squaring circuits.

Using the circuit shown in Figure 1, the duty cycle of the signals provided to the MK5102 should be within the 50 ± 1% range which is required for reliable operation. (Since the MK5103 requires a 50 ± 3% duty cycle, the input signals will be well within its range.) With the potentiometer adjusted so that the filter has unity gain, the results listed in Tables 1, 2, and 3 should be obtained. Tables 1 and 2 show the Mitel test tape (CM7291) results for the DTMF receiver system using the S3525A and the MK5102 or MK5103, respectively. Table 3 shows the Minimum Tone Coincidence Duration for the system using the MK5102 and MK5103 at various input levels.

The operation of the circuit shown in Figure 1 has been verified at temperatures of 0°C, 25°C, and 70°C. However, Tables 1, 2, and 3 show only the data for circuit operation at 25°C.

MK5102/S3525A DTMF RECEIVER SYSTEM
Figure 1



MK5102 WITH AMI S3525A MITEL TAPE (CM7291) TEST RESULTS

Table 1

TEST #	RESULTS
2a, b	BW = 4.6% of fo
2c, d	BW = 4.9% of fo
2e, f	BW = 4.7% of fo
2g, h	BW = 5.0% of fo
2i, j	BW = 4.8% of fo
2k, l	BW = 4.7% of fo
2m, n	BW = 4.8% of fo
2o, p	BW = 4.7% of fo
3	160 decodes
4	Acceptable Amplitude Ratio = 18.2 dB
5	Dynamic Range = 32 dB
6	Guard Time = 34.8 ms
7	99.0% Successful Decode at S/N Ratio of 12 dB
8	1 Hit on Talk-Off Test

MK5103 WITH AMI S3525A MITEL TAPE (CM7291) TEST RESULTS

Table 2

TEST #	RESULTS
2a, b	BW = 5.0% of fo
2c, d	BW = 5.1% of fo
2e, f	BW = 4.9% of fo
2g, h	BW = 5.2% of fo
2i, j	BW = 5.1% of fo
2k, l	BW = 5.0% of fo
2m, n	BW = 5.2% of fo
2o, p	BW = 5.1% of fo
3	160 decodes
4	Acceptable Amplitude Ratio = 19.1 dB
5	Dynamic Range = 32 dB
6	Guard Time = 32.5 ms
7	99.9% Successful Decode at S/N Ratio of 12 dB
8	1 Hit on Talk-Off Test

MK5102/3 WITH AMI S3525A MINIMUM TONE COINCIDENCE DURATION

Table 3

Input Level dBm (600 Ω)	MK5102 Decode Time	MK5103 Decode Time
-28 dBm	43.4 ms	38.9 ms
-25 dBm	37.4 ms	34.7 ms
-20 dBm	37.0 ms	34.7 ms
-10 dBm	36.3 ms	28.8 ms
0 dBm	37.3 ms	28.8 ms
+6 dBm	36.5 ms	28.9 ms

NOTES:

1. More information regarding the S3525A is available from:
   American Microsystems Inc.
   3800 Homestead Rd.
   Santa Clara, CA 95051
   Telephone: (408) 246-0330
   TWX: 910-338-0018
2. More information regarding the MK5102 and MK5103 is available from:
   Mostek Telecom Dept.
   1215 W. Crosby Rd.
   Carrollton, Texas 75006
   Telephone: (214) 323-1000
3. The AMI S3525A used in this evaluation was a typical part. Slightly different results may be obtained depending upon the particular S3525A used.

MOSTEK®

INTEGRATED TONE DECODER

MK5103(N)-5

FEATURES

- Detects all 16 standard DTMF digits
- Requires minimum external parts count for minimum system cost
- Uses inexpensive 3.579545 MHz crystal for reference
- Digital counter detection with period averaging insures minimum false response
- 16-pin package for high system density
- Single supply: 5 volts ±10%
- Output in either 4-bit binary code or dual 2-bit row/column code
- Will operate at 14dB S/N ratio under worst-case signal conditions
- Latched outputs

DESCRIPTION

The MK5103 is a monolithic integrated circuit fabricated using the complementary-symmetry MOS (CMOS) process. Using an inexpensive 3.579545 MHz television color-burst crystal for reference, the MK5103 detects and decodes the 8 standard DTMF frequencies used in telephone dialing. The requirement of only a single supply and its construction in a 16-pin package make the MK5103 ideal for applications requiring minimum size and external parts count.

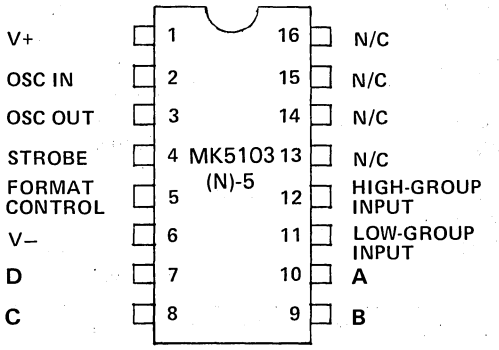
The MK5103 detects the high- and low-group DTMF tones after band splitting using a digital counting method. The zero crossings of the incoming tones are counted over several periods and the results averaged over a longer period. When a minimum of 30 milliseconds of a valid DTMF digit is detected, the proper data is latched into the outputs and the output strobe goes high. When a valid digit is no longer detected, the strobe will return low and the data will remain latched into the outputs. Minimum interdigit time is 35 milliseconds.

The MK5103 is designed to interface with the MK5099 Integrated Pulse Dialer with only one additional DIP package. These two parts working together form a DTMF-to-Pulse converter that meets the recognized telephone standards.

A block diagram of the MK5103 is shown in Figure 2. Functions of the individual pins are described beginning on page 2.

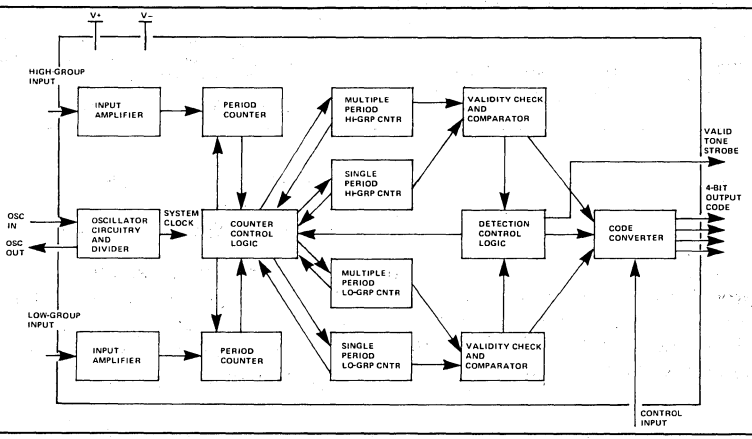
PIN CONNECTIONS

Figure 1



BLOCK DIAGRAM

Figure 2



ABSOLUTE MAXIMUM RATINGS*

DC Supply Voltage V+ (Referenced to V-) ..... +6.0 Volts
Operating Temperature ..... 0°C to 70°C
Storage Temperature ..... -55°C to 100°C
Maximum Circuit Power Dissipation 300mW
Voltage on any pin, with respect to V- ..... -0.3 Volt
Voltage on any pin, with respect to V+ ..... +0.3 Volt

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

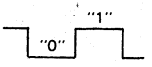
ELECTRICAL CHARACTERISTICS

$0°C \leq T_A \leq 70°C$ V- = **0 Volts**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage (V+)	(V- = 0)	4.5		5.5	Volts	
Lo Group & Hi Group Inputs	47% - 53% Duty Cycle Rectangular Wave	0.9		V+	Volts Peak-to-Peak	1,2
STROBE, A, B, C, D OUTPUTS	"0" Level	0.0		0.4	Volt @ 1.6 mA	
	"1" Level	(V+)-1		V+	Volts @ 0.1 mA	
FORMAT CONTROL INPUT	"0" Level	0.0		0.5	Volt @ 700μA	
	"1" Level	(V+)-0.5		V+	Volt @ 700μA	
Frequency Detect Band Width		± 2.0	± 2.5	± 2.9	% of f_o	
Tone Coincidence Duration		30			ms	4
Interdigit Interval		35			ms	4
Signal-to-Noise Ratio		14			dB	3,5
Supply Current @ 5.5V	Inputs and Outputs Unloaded		2	5	mA	

NOTES:

1. Due to internal biasing, this input must be capacitively coupled with a low-leakage 0.05 μF capacitor.
2. No coupling capacitor is needed if the DTMF rectangular wave meets the following criteria:



A. Logic "0" level = 1 Volt (max)
B. Logic "1" level = 4 Volts (min)

3. Signal-To-Noise Ratio is defined as:
$SN = 20 \log \frac{SA}{NA}$
where SA = RMS Amplitude of single tone being detected.
NA = RMS white noise in the band from 300Hz to 3.4KHz.
4. Tone coincidence duration and interdigit interval measured at High- and Low-group inputs. Filter and/or limiter or comparator characteristics will affect the overall detect time.
5. Signal-To-Noise Ratio with 33db Filter Separation.

FUNCTIONAL DESCRIPTION

OSCILLATOR

The MK5103 contains an on-board inverter with sufficient gain to provide oscillation when working with a low-cost television "color-burst" crystal. The inverter input is OSC IN (pin 2) and output is OSC OUT (pin 3). The circuit is designed to work with a crystal cut to 3.579545 MHz to give detection of the standard DTMF frequencies.

FORMAT CONTROL (PIN 5)

The Control pin is used to control the output format of Pins 7 through 10. This three-state input selects a 4-bit Binary Code, a Dual 2-Bit Row/Column code, or high-impedance output for use with bus-structured circuitry. This three-state input is controlled as follows:

FORMAT CONTROL FUNCTIONS
Table 1

FORMAT CONTROL INPUT	OUTPUT DATA FORMAT
V-	High Impedance
V+	4-Bit Binary
Floating	Dual 2-Bit Row/Column

The following table describes the two output codes.

Table 2

Digit	4-Bit Binary D	C	B	A	Dual 2-Bit Row D	C	Column B	A
1	0	0	0	1	0	1	0	1
2	0	0	1	0	0	1	1	0
3	0	0	1	1	0	1	1	1
4	0	1	0	0	1	0	0	1
5	0	1	0	1	1	0	1	0
6	0	1	1	0	1	0	1	1
7	0	1	1	1	1	1	0	1
8	1	0	0	0	1	1	1	0
9	1	0	0	1	1	1	1	1
0	1	0	1	0	0	0	1	0
*	1	0	1	1	0	0	0	1
#	1	1	0	0	0	0	1	1
A	1	1	0	1	0	1	0	0
B	1	1	1	0	1	0	0	0
C	1	1	1	1	1	1	0	0
D	0	0	0	0	0	0	0	0

Figure 3 shows the relationship between the data output code shown in Table 2 and the standard DTMF keyboard.

DTMF DIALING MATRIX
Figure 3

	Col 1	Col 2	Col 3	Col 4
Row 1	1	2	3	A
Row 2	4	5	6	B
Row 3	7	8	9	C
Row 4	*	0	#	D

Note: Column 4 is for special applications and is not normally used in telephone dialing.

Table 3 shows the detection frequency associated with each row or column:

DETECTION FREQUENCY
Table 3

Low Group fo	High Group fo
Row 1 = 697 Hz	Column 1 = 1209 Hz
Row 2 = 770 Hz	Column 2 = 1336 Hz
Row 3 = 852 Hz	Column 3 = 1477 Hz
Row 4 = 941 Hz	Column 4 = 1633 Hz

OUTPUTS A THRU D (PINS 7 THRU 10)

Outputs A thru D are CMOS push-pull when enabled and open-circuited (high impedance) when disabled by the format control pin.

A thru D are the data out lines. The output data can be in in two formats as described in the section about the format control pin (pin 5).

The Dual 2-Bit Row/Column code decodes with A and B indicating the column selected, and C and D indicating the row selected.

The two output codes allow the user to obtain either 1-of-16 or 2-of-8 output data by using only a single additional package.

N/C (PINS 13 THRU 16)

Pins 13 thru 16 are not internally connected and may be used as tie points.

STROBE (PIN 4)

The STROBE output goes to a "1" when 30 milliseconds of a valid DTMF signal is detected and remains at a "1" until an interdigit interval has been detected. The data at A-D are already valid when STROBE goes to a "1" and will remain unchanged until the next DTMF digit is detected.

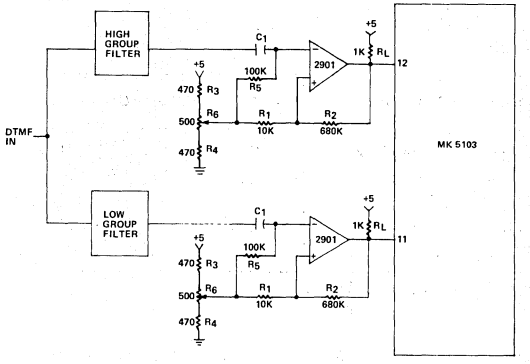
LOW-GROUP INPUT (PIN 11) AND HIGH-GROUP INPUT (PIN 12)

The circuitry driving these inputs, as shown in Figure 4, should be squaring circuits which use resistive dividers to set the output duty cycle to 50%. The squaring circuit shown was designed to provide hysteresis and allow the circuit to respond to signal levels of -28dBm or greater, where -28dBm corresponds to a peak-to-peak voltage of 87.1mV. Any squaring circuit providing a 47% - 53% duty cycle over the receiver and dynamic range is sufficient.

The high-group and low-group signals are provided by the high-group filter and the low-group filter, as shown in Figure 4. These filters have the response characteristics shown in Figure 5 and are used to separate the DTMF signal into its high-group and low-group components.

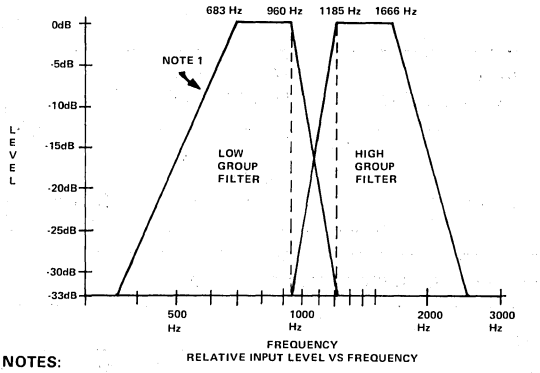
SUGGESTED INPUT LIMITER CIRCUIT

Figure 4



INPUT BAND SEPARATION FILTER

Figure 5



RELATIVE INPUT LEVEL VS FREQUENCY

NOTES:

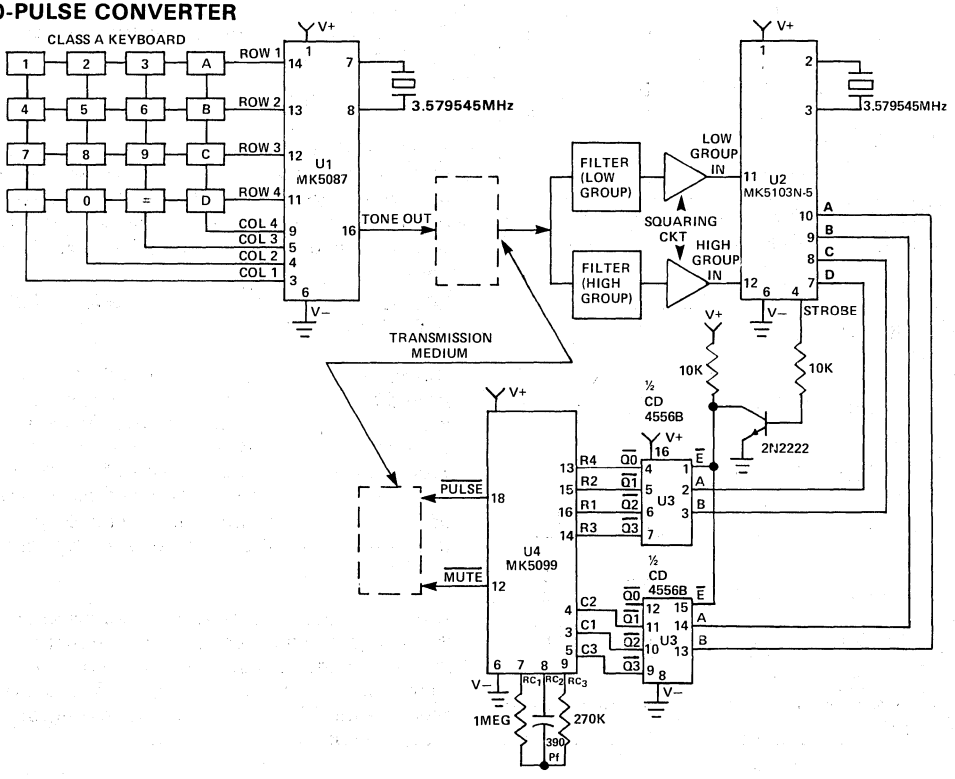
APPLICATIONS

Two possible applications of the MK5103 are shown in Figure 6 and Figure 7. The dual 2-bit row/column code is useful when interfacing a key-to-pulse converter, as shown in Figure 6. On this circuit, the MK5103N-5, CD4556 and MK5099 combine to form a tone-to-pulse converter, which allows the use of DTMF telephones in rotary exchanges. The DTMF tones are detected by the MK5103N-5, which then generates the corresponding row/column code. Each CD4556 then uses this 2-bit code to select 1 of 4 active-low outputs. The MK5099 then interprets these signals as a valid key closure and generates a corresponding series of pulses.

For simple remote-control applications, the circuit of Figure 7 is useful. After a valid tone is detected, strobe will go high and one of the 16 outputs on the binary-to-1-of-16 encoder will go true. Thus, a DTMF transmitter and 16-key keyboard can be used to control 1 of 16 functions in a DTMF receiver.

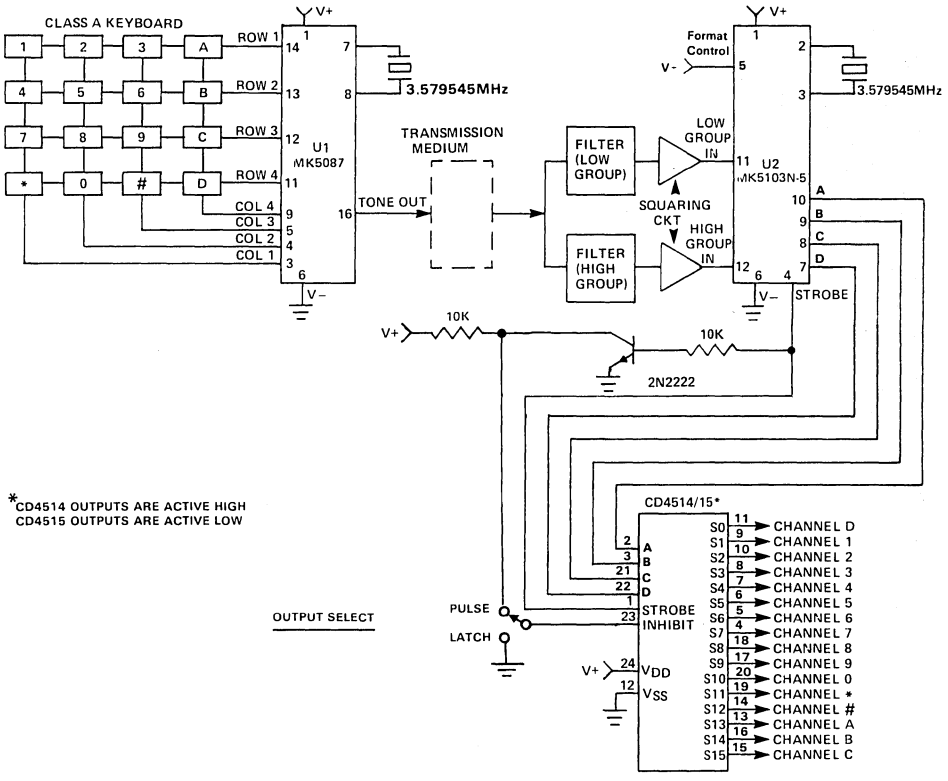
TONE-TO-PULSE CONVERTER

Figure 6



16-CHANNEL REMOTE CONTROL

Figure 7



MOSTEK®

TELECOMMUNICATIONS

DTMF Receiver System

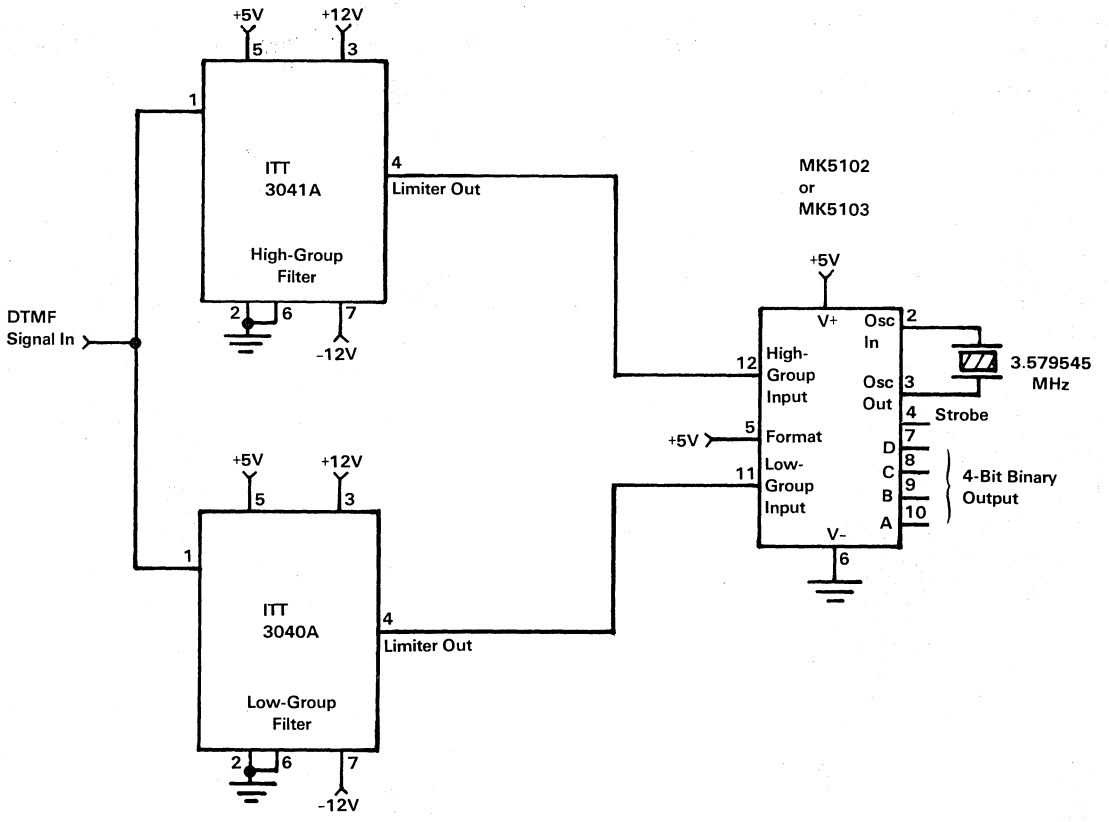
A DTMF receiver system with a low parts count may be constructed using the MK5102 or MK5103 tone decoder and the ITT 3040A and ITT 3041A hybrid filter[1]. The ITT 3040A and ITT 3041A filters have on-chip limiters so that external squaring circuits are not needed. An alternate design allowing precise adjustment of external squaring circuits is described in another Mostek Application Note[2]. Tables 1 and 2 show the MITEL (CM7290) tape results using the ITT 3040A/41A with the MK5102 and MK5103, respectively.

NOTES:

(1) ITT 3040A and ITT 3041A filters with limiters may be obtained from:
ITT North Microsystems Division
700 Hillsboro Plaza
Deerfield Beach, Florida 33441
Telephone: 305-421-8450
TWX: 510-953-7523

(2) MK5102N-5 DTMF Decoder Application Note, "Design Considerations for a DTMF Receiver System" is available from:
Mostek • Telecom Dept.
1215 W. Crosby Rd.
Carrollton, Texas 75006
Telephone: 214-323-6000

Figure 1



MK5102 with ITT 3040A and ITT 3041A
MITEL TAPE (CM7290) TEST RESULTS
Table 1

TEST #	RESULTS
2a, b	BW = 4.7 % of fo
2c, d	BW = 4.8 % of fo
2e, f	BW = 5.4 % of fo
2g, h	BW = 4.9 % of fo
2i, j	BW = 5.3 % of fo
2k, l	BW = 5.4 % of fo
2m, n	BW = 5.6 % of fo
2o, p	BW = 4.9 % of fo
3	159 decodes
4	Acceptable Amplitude Ratio = 19.7 dB
5	Dynamic Range = 25 dB
6	Guard Time = 32.9 ms
7	99.9% Successful Decode at S/N Ratio of 12 dB
8	3 Hits on Talk-Off Test

MK5103 with ITT 3040A and ITT 3041A
MITEL TAPE (CM7290) TEST RESULTS
Table 2

TEST #	RESULTS
2a, b	BW = 5.3 % of fo
2c, d	BW = 5.2 % of fo
2e, f	BW = 5.0 % of fo
2g, h	BW = 5.4 % of fo
2i, j	BW = 5.6 % of fo
2k, l	BW = 5.3 % of fo
2m, n	BW = 5.4 % of fo
2o, p	BW = 5.6 % of fo
3	159 decodes
4	Acceptable Amplitude Ratio = 19.9 dB
5	Dynamic Range = 30 dB
6	Guard Time = 23.3 ms
7	99.9% Successful Decode at S/N Ratio of 12 dB
8	9 Hits on Talk-Off Test

1982 TELECOMMUNICATION PRODUCTS DATA BOOK

PRODUCT PROFILE

MOSTEK®

TELECOMMUNICATION PRODUCTS

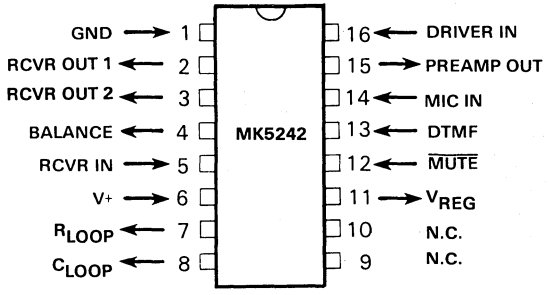
Active Speech Network

MK5242

FEATURES

- Direct telephone-line operation with no external power supply
- Minimum external parts count
- Interfaces directly with Mostek dialers
- Low voltage operation — 3.2 volts (Tip to Ring)
- On-chip loop current regulation
- Automatically adjusted equalization for loop-length compensation
- Direct interface to low-cost transducers

PIN CONNECTIONS



DESCRIPTION

The MK5242 is a monolithic integrated active speech network manufactured using a bipolar process. The MK5242 performs the 2-to-4 wire conversion function typically accomplished using a hybrid transformer-type speech network. In replacing the conventional speech network, the MK5242 also provides the capability of interface with low-cost transducers for the transmitter and receiver.

The MK5242 is designed such that it may interface with Mostek tone dialers with minimal external circuitry. It provides a voltage regulated output for tone-dialer applications which require fixed supply operation. The MK5242 will also interface with Mostek pulse dialers.

The MK5242 operates directly from the telephone line with no external power supply and requires a minimal amount of external components. It features on-chip loop-current regulation and will compensate for loop length with automatically adjusted equalization.

1982 TELECOMMUNICATION PRODUCTS DATA BOOK

μ-255 Law Companding CODEC
MK5116(J/P)

FEATURES

- ± 5-Volt Power Supplies
- Low Power Dissipation - 30mW (Typ)
- Follows the μ-255 Companding Law
- Synchronous or Asynchronous Operation
- On-Chip Sample and Hold
- On-Chip Offset Null Circuit Eliminates Long-Term Drift Errors and Need for Trimming
- Single 16-Pin Package
- Minimal External Circuitry Required
- Serial Data Output of 64kb/s—2.1Mb/s at 8kHz Sampling Rate
- Separate Analog and Digital Grounding Pins Reduce System Noise Problems

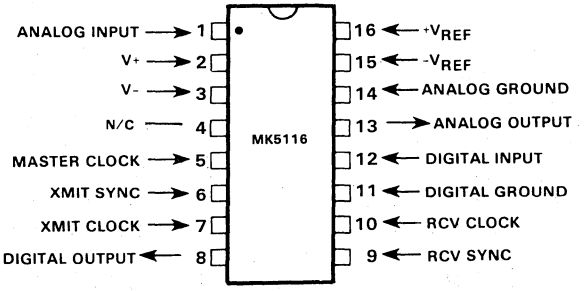
DESCRIPTION

The MK5116 is a monolithic CMOS companding CODEC which contains two sections: (1) An analog-to-digital converter which has a transfer characteristic conforming to the μ-255 companding law and (2) a digital-to-analog converter which also conforms to the μ-255 law.

These two sections form a coder-decoder which is designed to meet the needs of the telecommunications industry for per-channel voice-frequency codecs used in telephone digital switching and transmission systems. Digital input and output are in serial format. Actual transmission and reception of 8-bit data words containing the analog information is done at a 64kb/s-2.1 Mb/s rate with analog signal sampling occuring at an 8kHz rate. A sync pulse input is provided for synchronizing transmission and reception of multi-channel information being multiplexed over a single transmission line.

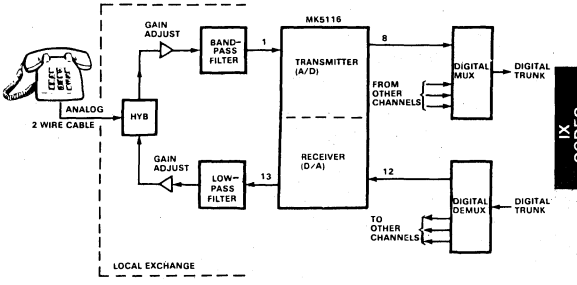
The pin configuration of the MK5116 is shown in Figure 1.

PIN CONNECTIONS
Figure 1



A block diagram of a PCM system using the MK5116 is shown in Figure 2.

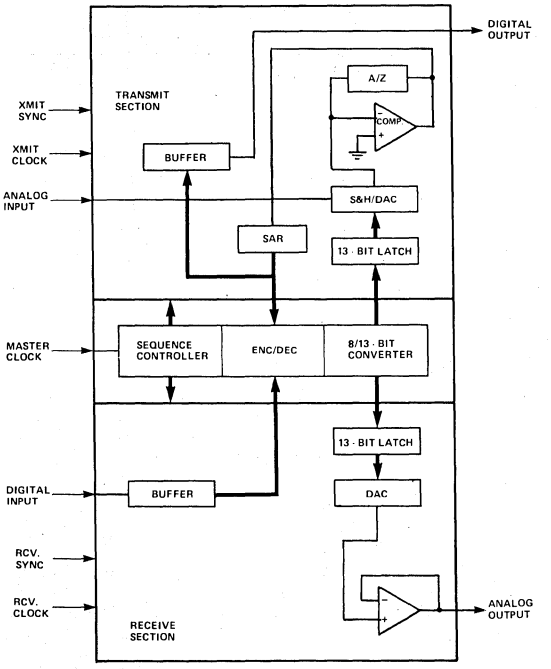
PCM SYSTEM BLOCK DIAGRAM
Figure 2



FUNCTIONAL DESCRIPTION: (Refer to Figure 3 for a Block Diagram)

MK5116 BLOCK DIAGRAM

Figure 3



POSITIVE AND NEGATIVE REFERENCE VOLTAGES ($+V_{REF}$ and $-V_{REF}$) Pins 16 and 15

These inputs provide the conversion references for the digital-to-analog converters in the MK5116. $+V_{REF}$ and $-V_{REF}$ must maintain 100ppM/°C regulation over the operating temperature range. Variation of the reference directly affects system gain.

ANALOG INPUT, Pin 1

Voice-frequency analog signals which are bandwidth-limited to 4kHz are input at this pin. Typically, they are then sampled at an 8kHz rate (Refer to Figure 4). The analog input must remain between $+V_{REF}$ and $-V_{REF}$ for accurate conversion. The recommended input interface circuit is shown in Figure 9.

MASTER CLOCK, Pin 5

This signal provides the basic timing and control signals required for all internal conversions. It does not have to be synchronized with RCV. SYNC, RCV. CLOCK, XMIT SYNC or XMIT CLOCK and is not internally related to them.

XMIT SYNC, Pin 6 (Refer to Figure 10 for the Timing Diagram)

This input is synchronized with XMIT CLOCK. When XMIT SYNC goes high, the digital output is activated and the A/D conversion begins on the next positive edge of MASTER CLOCK. The conversion by MASTER CLOCK can be asynchronous with XMIT CLOCK. The serial output data is clocked out by the positive edges of XMIT CLOCK. The negative edge of XMIT SYNC causes the digital output to become three-state. XMIT SYNC may remain high longer than 8 XMIT CLOCK cycles, but must go low for at least 1 master clock prior to the transmission of the next digital word(Refer to Figure 12).

XMIT CLOCK, Pin 7 (Refer to Figure 10 for the Timing Diagram)

The on-chip 8-bit output shift register of the MK5116 is unloaded at the clock rate present on this pin. Clock rates of 64kHz-2.1MHz can be used for XMIT CLOCK. The positive edge of the INTERNAL CLOCK transfers the data from the master to the slave of a master-slave flip-flop (Refer to Figure 5). If the positive edge of XMIT SYNC occurs after the positive edge of XMIT CLOCK, XMIT SYNC will determine when the first positive edge of INTERNAL CLOCK will occur. In this event, the hold time for the first clock pulse is measured from the positive edge of XMIT SYNC.

RCV. SYNC, Pin 9 (Refer to Figure 11 for the Timing diagram)

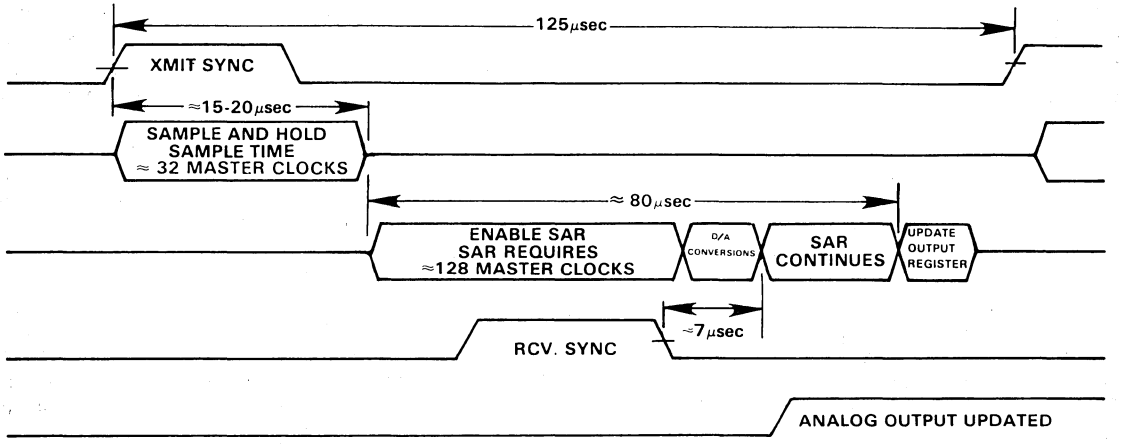
This input is synchronized with RCV. CLOCK and serial data is clocked in by RCV. CLOCK. Duration of the RCV. SYNC pulse is approximately 8 RCV. CLOCK periods. The conversion from digital-to-analog starts after the negative edge of the RCV. SYNC pulse (Refer to Figure 4). The negative edge of RCV. SYNC should occur before the 9th positive clock edge to insure that only eight bits are clocked in. RCV. SYNC must stay low for 17 MASTER CLOCKS (min.) before the next digital word is to be received (Refer to Figure 13).

RCV CLOCK, Pin 10 (Refer to Figure 11 for Timing Diagram)

The on-chip 8-bit shift register for the MK5116 is loaded at the clock rate present on this pin. Clock rates of 64kHz-2.1MHz can be used for RCV. CLOCK. Valid data should be applied to the digital input before the positive edge of the internal clock (Refer to Figure 5). This set up time, t_{RDS}, allows the data to be transferred into the MASTER of a master-slave flip-flop. The positive edge of the INTERNAL CLOCK transfers the data to the SLAVE of the master-slave flip-flop. A hold time, t_{RDH}, is required to complete this transfer. If the rising edge of RCV. SYNC occurs after the first rising edge of RCV. CLOCK, RCV. SYNC will determine when the first positive edge of INTERNAL CLOCK will occur. In this event, the set up and hold times for the first clock pulse should be measured from the positive edge of RCV. SYNC.

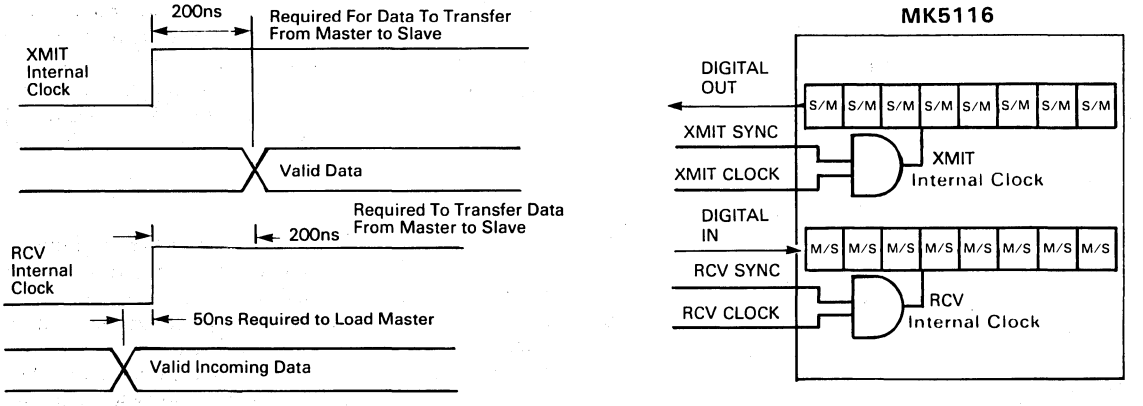
A/D, D/A CONVERSION TIMING

Figure 4



DATA INPUT/OUTPUT TIMING

Figure 5



DIGITAL OUTPUT, Pin 8

The MK5116 output register stores the 8-bit encoded sample of the analog input. This 8-bit word is shifted out under control of XMIT SYNC and XMIT CLOCK. When XMIT SYNC is low, the DIGITAL OUTPUT is an open circuit. When XMIT SYNC is high, the state of the DIGITAL OUTPUT is determined by the value of the output bit in the serial shift register. The output is composed of a Sign Bit, 3 Chord Bits, and 4 Step Bits. The Sign Bit indicates the polarity of the analog input while the Chord and Step Bits indicate the magnitude. In the first Chord, the Step Bit has a value of 0.6mV. In the second Chord, the Step Bit has a value of 1.2mV. This doubling of the step value continues for each of the six successive Chords.

Each Chord has a specific value and the Step Bits, 16 in each Chord, specify the displacement from that value. (Refer to Table 1). Thus the output, which follows the μ-255 law, has resolution that is proportional to the input level rather than to full scale. This provides the resolution of a 12-bit A/D converter at low input levels and that of a 6-bit converter as the input approaches full scale. The transfer characteristic of the A/D converter (μ-law Encoder) is shown in Figure 6.

DIGITAL OUTPUT CODE μ-LAW

Table 1

	Chord Code	Chord Value	Step Value
1.	000	0.0mV	0.613mV
2.	001	10.11mV	1.226mV
3.	010	30.3mV	2.45mV
4.	011	70.8mV	4.90mV
5.	100	151.7mV	9.81mV
6.	101	313mV	19.61mV
7.	110	637mV	39.2mV
8.	111	1.284V	78.4mV

EXAMPLE:

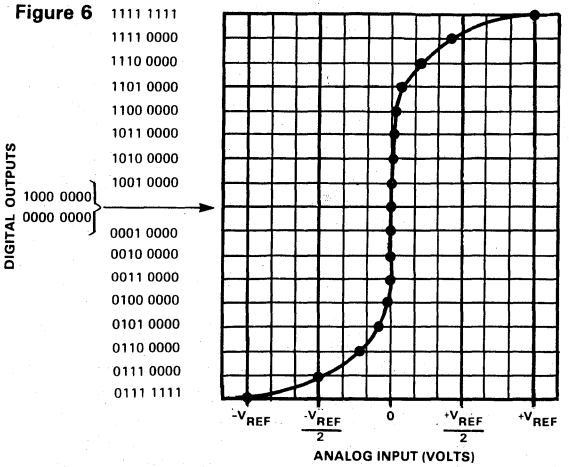
1 011 0010 = + 70.8mV + (2 x 4.90mV)

Sign Bit Chord Step Bits

If the sign bit were a zero, then both plus signs would be changed to minus signs.

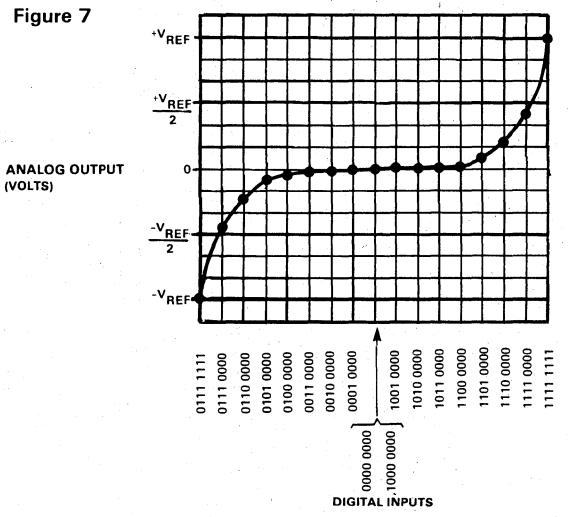
A/D CONVERTER (μ-Law Encoder) TRANSFER CHARACTERISTIC

Figure 6



D/A CONVERTER (μ-Law Decoder) TRANSFER CHARACTERISTIC

Figure 7



DIGITAL INPUT, Pin 12

The MK5116 input register accepts the 8-bit sample of an analog value and loads it under control of RCV. SYNC and RCV. CLOCK. The timing diagram is shown in Figure 11. When RCV. SYNC goes high, the MK5116 uses RCV. CLOCK to clock the serial data into its input register. RCV. SYNC goes low to indicate the end of serial input data. The 8 bits of the input data have the same functions described for the DIGITAL OUTPUT. The transfer characteristic of the D/A converter (μ-law Decoder) is shown in Figure 7.

ANALOG OUTPUT, Pin 13

The analog output is in the form of voltage steps (100% duty cycle) having amplitude equal to the analog sample which was encoded. This waveform is then filtered with an external low-pass filter with sinx/x correction to recreate the sampled voice signal.

OPERATION OF CODEC WITH 64kHz XMIT/RCV CLOCK FREQUENCIES

XMIT/RCV. SYNC must not be allowed to remain at a logic "1" state. XMIT SYNC is required to be at a logic "0" state for 1 master clock period (min.) before the next digital word is transmitted. RCV. SYNC is required to be at a logic "0" state for 17 master clock periods (min.) before the next digital word is received (Refer to Figures 12 and 13).

OFFSET NULL

The offset null feature of the MK5116 eliminates long-term drift errors and conversion errors due to temperature changes by going through an offset adjustment cycle before every conversion, thus guaranteeing accurate A/D conversion for inputs near ground. There is no offset adjust of the output amplifier because, since the output is intended to be AC - coupled to the external filter, the resultant DC error ($V_{OFFSET\ O}$) will have no effect. The sign bit is not used to null the analog input. Therefore, for an analog input of 0 volts, the sign bit will be stable.

PERFORMANCE EVALUATION

The equipment connections shown in Figure 8 can be used to evaluate the performance of the MK5116. An analog signal provided by the HP3551A Transmission Test Set is connected to the Analog Input (Pin 1) of the MK5116. The Digital Output of the CODEC is tied back to the Digital Input and the Analog Output is fed through a low-pass filter to the HP3551A. Remaining pins of the MK5116 are connected as follows:

(1) RCV. SYNC is tied to XMIT SYNC
(2) XMIT CLOCK is tied to MASTER CLOCK. The signal is inverted and tied to RCV. CLOCK.

The following timing signals are required:

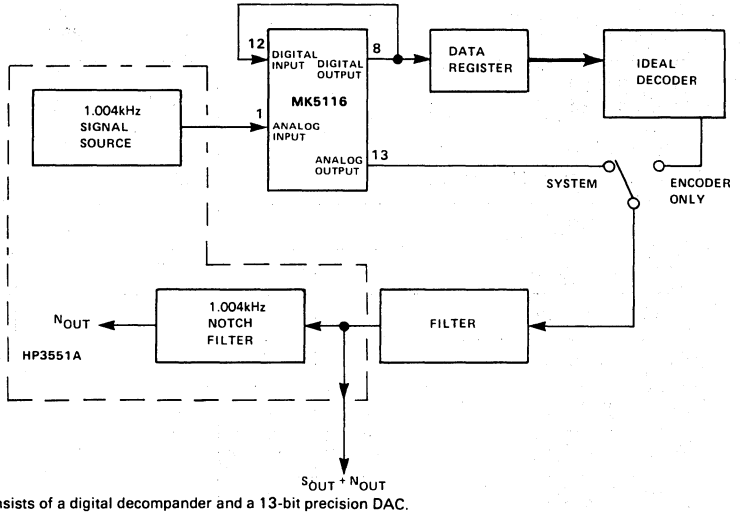
(1) MASTER CLOCK = 1.536 MHz
(2) XMIT SYNC repetition rate = 8kHz
(3) XMIT SYNC width = 8 XMIT CLOCK periods

When all the above requirements are met, the setup of Figure 8 permits the measurement of synchronous system performance over a wide range of analog inputs. The data register and ideal decoder provide a means of checking the encoder portion of the MK5116 independently of the decoder section. To test the system in the asynchronous mode, MASTER CLOCK should be separated from XMIT CLOCK and MASTER CLOCK should be separated from RCV. CLOCK. XMIT and RCV. CLOCKS are separated also.

Some experimental results obtained with the MK5116 are shown in Figure 14 and Figure 15. In each case, both the measured results and the corresponding D3 Channel Bank specifications are shown. The MK5116 exceeds the requirements for Signal-to-Distortion ratio (Figure 14) and for Gain Tracking (Figure 15).

SYSTEM CHARACTERISTICS TEST CONFIGURATION

Figure 8



NOTE: The ideal decoder consists of a digital decompander and a 13-bit precision DAC.

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage, V+ ..... +6V
DC Supply Voltage, V– ..... –6V
Ambient Operating Temperature, T_A ..... 0°C to 70°C
Storage Temperature ..... –55°C to +125°C
Package Dissipation at 25°C (Derated 9mW/°C when soldered into PCB) 500mW
Digital Input ..... $-0.5V \leq V_{IN} \leq V+$
Analog Input ..... $V- \leq V_{IN} \leq V+$
$+V_{REF}$ ..... $-0.5V \leq +V_{REF} \leq V+$
$-V_{REF}$ ..... $V- \leq -V_{REF} \leq +0.5V$

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL OPERATING CHARACTERISTICS
POWER SUPPLY REQUIREMENTS

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V+	Positive Supply Voltage	4.75	5.0	5.25	V	
V–	Negative Supply Voltage	–5.25	–5.0	–4.75	V	
$+V_{REF}$	Positive Reference Voltage	2.375	2.5	2.625	V	1
$-V_{REF}$	Negative Reference Voltage	–2.625	–2.5	–2.375	V	1

TEST CONDITIONS: V+ = 5.0V, V– = –5.0V, + V_{REF} = 2.5V, $-V_{REF}$ = –2.5V, T_A = 0°C to 70°C

DC CHARACTERISTICS

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
R_{INAS}	Analog Input Resistance During Sampling		2		kΩ	2
R_{INANS}	Analog Input Resistance Non-Sampling		100		MΩ	
C_{INA}	Analog Input Capacitance		150	250	pF	2
$V_{OFFSET/I}$	Analog Input Offset Voltage		±1	± 8	mV	2
R_{OUTA}	Analog Output Resistance		20	50	Ω	
I_{OUTA}	Analog Output Current	0.25	0.5		mA	
$V_{OFFSET/O}$	Analog Output Offset Voltage		–200	± 850	mV	
I_{INLOW}	Logic Input Low Current (V_{IN} = 0.8V) Digital Input, Clock Input, Sync Input		± 0.1	± 10	μA	3
I_{INHIGH}	Logic Input High Current (V_{IN} = 2.4V) Digital Input, Clock Input, Sync Input		–0.25	–0.8	mA	3
C_{DO}	Digital Output Capacitance		8	12	pF	
I_{DOL}	Digital Output Leakage Current		± 0.1	±10	μA	
V_{OUTLOW}	Digital Output Low Voltage			0.4	V	4
$V_{OUTHIGH}$	Digital Output High Voltage	3.9			V	4
I+	Positive Supply Current		4	10	mA	5
I–	Negative Supply Current		2	6	mA	5
I_{REF+}	Positive Reference Current		4	20	μA	
I_{REF-}	Negative Reference Current		4	20	μA	

AC CHARACTERISTICS (Refer to Figure 10 and Figure 11)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
F_M	Master Clock Frequency	1.5	1.544	2.1	MHz	
F_R, F_X	XMIT, RCV. Clock Frequency	0.064	1.544	2.1	MHz	
PW_{CLK}	Clock Pulse Width (MASTER, XMIT, RCV.)	200			ns	
t_{RC},t_{FC}	Clock Rise, Fall Time(MASTER, XMIT, RCV.)			25% of PW_{CLK}	ns	
t_{RS}, t_{FS}	Sync Rise, Fall Time (XMIT, RCV.)			25% of PW_{CLK}	ns	
t_{DIR}, t_{DIF}	Data Input Rise, Fall Time			25% of PW_{CLK}	ns	
t_{WSX}, t_{WSR}	Sync Pulse Width (XMIT RCV.)		$\frac{8}{F_X(F_R)}$		μs	
t_{PS}	Sync Pulse Period (XMIT, RCV.)		125		μs	
t_{XCS}	XMIT Clock-to-XMIT Sync Delay	50% of t_{FC} (t_{RS})			ns	6

AC CHARACTERISTICS (Refer to Figure 10 and Figure 11)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
t_{XCSN}	XMIT Clock-to-XMIT Sync (Negative Edge) Delay	200			ns	
t_{XSS}	XMIT Sync Set-Up Time	200			ns	
t_{XDD}	XMIT Data Delay	0		200	ns	4
t_{XDP}	XMIT Data Present	0		200	ns	4
t_{XDT}	XMIT Data Three State			150	ns	4
t_{DOF}	Digital Output Fall Time		50	100	ns	4
t_{DOR}	Digital Output Rise Time		50	100	ns	4
t_{SRC}	RCV. Sync-to-RCV. Clock Delay	50% of t_{RC} (t_{FS})			ns	6
t_{RDS}	RCV. Data Set-Up Time	50			ns	7
t_{RDH}	RCV. Data Hold Time	200			ns	7
t_{RCS}	RCV. Clock-to-RCV. Sync Delay	200			ns	
t_{RSS}	RCV. Sync Set-Up Time	200			ns	7
t_{SAO}	RCV. Sync-to-Analog Output Delay		7		μs	
SLEW+	Analog Output Positive Slew Rate		1		V/μs	
SLEW-	Analog Output Negative Slew Rate		1		V/μs	
DROOP	Analog Output Droop Rate		25		μV/μs	

SYSTEM CHARACTERISTICS (Refer to Figures 14 and 15)

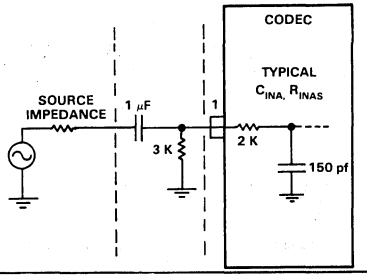
SYM	PARAMETER	MIN	TYP	MAX	UNITS	TEST COND.
S/D	Signal-to-Distortion Ratio	35 29 24	39 34 29		dB dB dB	Analog Input=0 to -30dBm0 Analog Input=-40dBm0 Analog Input=-45dm0
GT	Gain Tracking	-0.4 -0.8 -2.5	±0.1 ±0.1 ±0.2	+0.4 +0.8 +2.5	dB dB dB	Analog Input=+3 to -37dBm0 Analog Input=-37 to -50dBm0 Analog Input=-50 to -55dBm0
N_{IC}	Idle Channel Noise		10	18	dBrnc0	Analog Input=0 Volts; note 2
TLP	Transmission Level Point		+4		dB	600Ω

NOTES:

1. $+V_{REF}$ and $-V_{REF}$ must be matched within ± 1% in order to meet system requirements.
2. Sampling is accomplished by charging an internal capacitor; therefore, the designer should avoid excessive source impedance. Input related device characteristics are derived using the Recommended Analog Input Circuit. See Figure 9.
3. When a transition from a "1" to a "0" takes place, the user must sink the "1" current until reaching the "0" level.
4. Driving 30pF with $I_{OH} = -100\mu A$, $I_{OL} = 500\mu A$.
5. Results in 30 mW typical power dissipation (clocks applied) under normal operating conditions.
6. This delay is necessary to avoid overlapping CLOCK and SYNC.
7. The first bit of data is loaded when the Sync and Clock are both "1" during bit time 1 as shown on RCV. timing diagram.

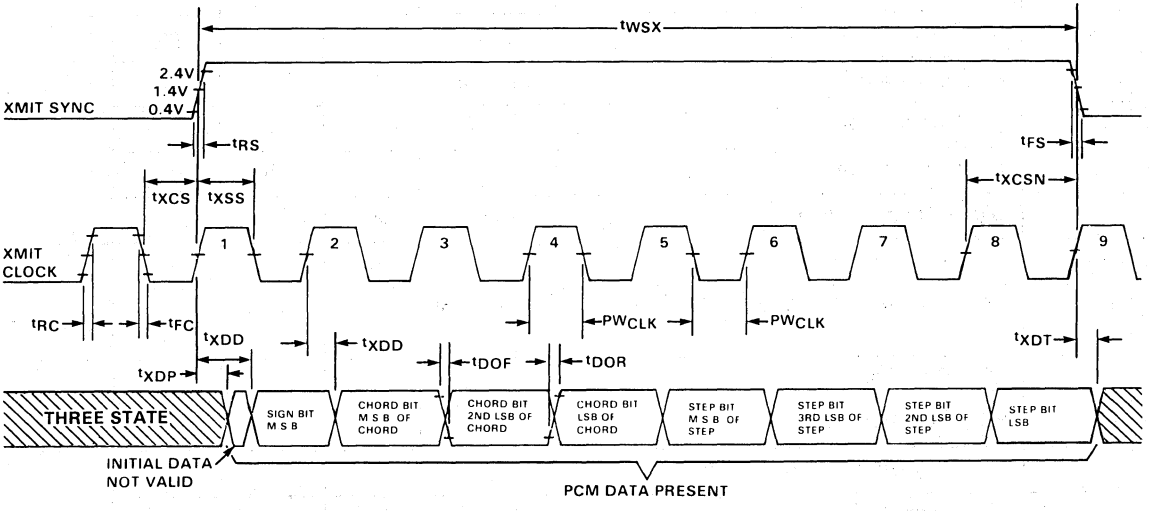
RECOMMENDED ANALOG INPUT CIRCUIT

Figure 9



TRANSMITTER SECTION TIMING

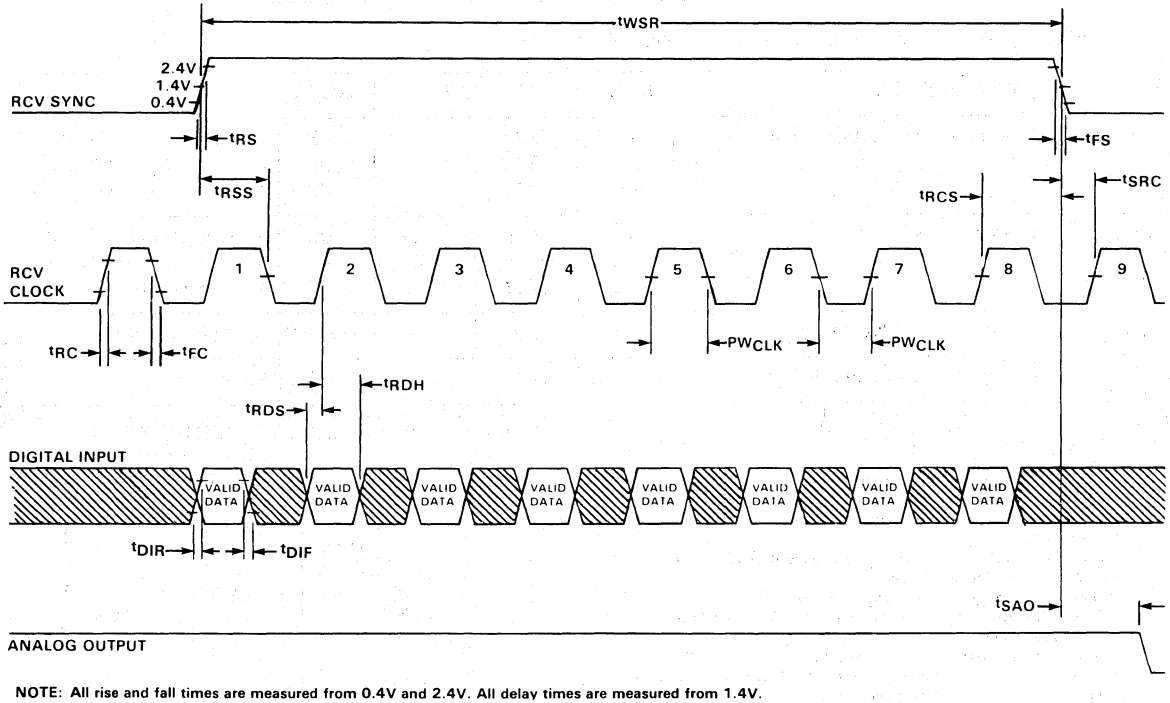
Figure 10



NOTE: All rise and fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

RECEIVER SECTION TIMING

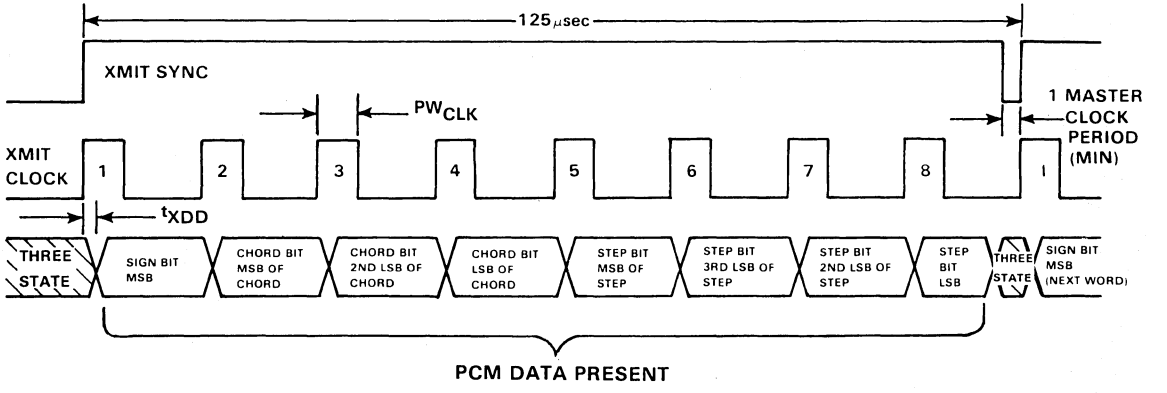
Figure 11



NOTE: All rise and fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

64kHz OPERATION, TRANSMITTER SECTION TIMING

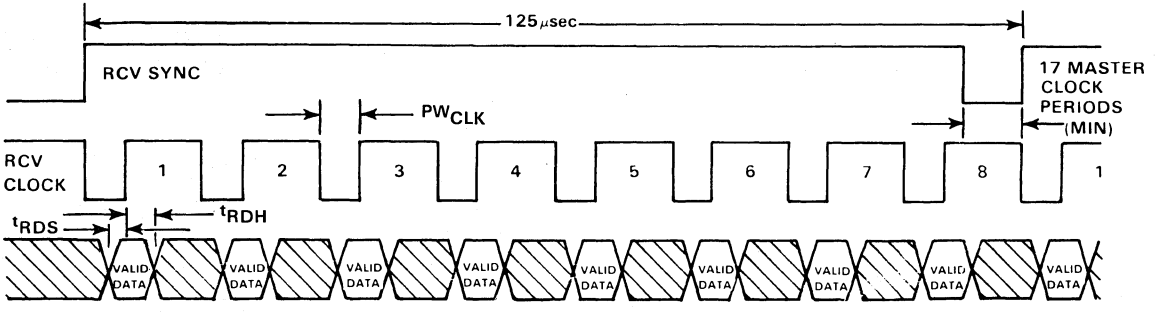
Figure 12



NOTE: All rise and fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

64kHz OPERATION, RECEIVER SECTION TIMING

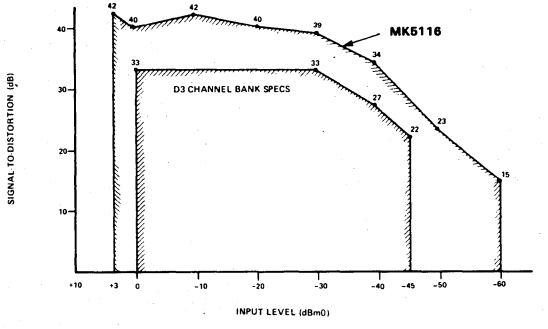
Figure 13



NOTE: All rise and fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

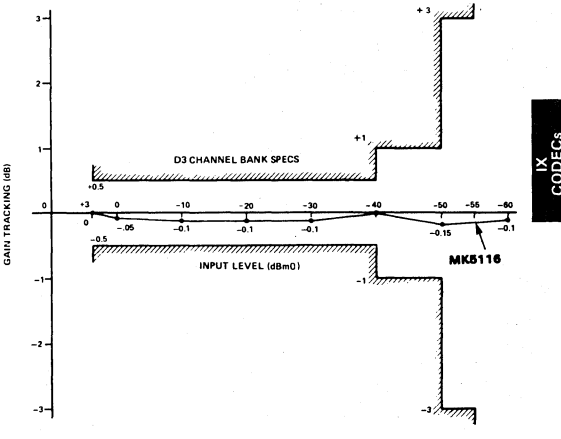
MK5116 S/D RATIO VS: INPUT LEVEL

Figure 14



MK5116 GAIN TRACKING PERFORMANCE

Figure 15



μ-255 Law Companding CODEC
MK5151(J/P)

FEATURES

- ±5-Volt Power Supplies
- Low Power Dissipation - 30mW (Typ)
- **Follows the μ-255 Companding Law**
- Zero Code Suppression and Sign-Magnitude Data Format
- On-Chip Sample and Hold
- On-Chip Offset Null Circuit Eliminates Long-Term Drift Errors and Need for Trimming
- Single 24-Pin Package
- Minimal External Circuitry Required
- Serial Data Output of 64kb/s - 2.1Mb/s at 8kHz Sampling Rate
- Separate Analog and Digital Grounding Pins Reduce System Noise Problems

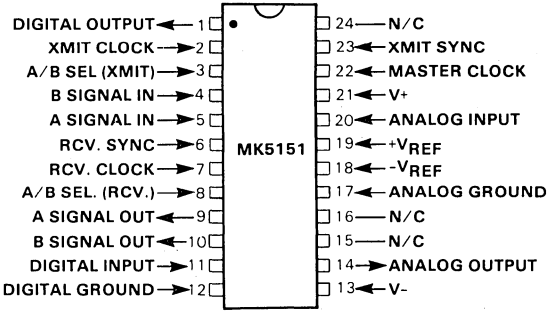
DESCRIPTION

The MK5151 is a monolithic CMOS companding CODEC which contains two sections: (1) An analog-to-digital converter which has a transfer characteristic conforming to the μ-255 companding law and (2) a digital-to-analog converter which also conforms to the μ-255 law.

These two sections form a coder-decoder which is designed to meet the needs of the telecommunications industry for per-channel voice-frequency codecs used in telephone digital switching and transmission systems. Digital input and output are in serial format. Actual transmission and reception of 8-bit data words containing the analog information is done at a 64kb/s-2.1 Mb/s rate with analog signal sampling occuring at an 8kHz rate. A sync pulse input is provided for synchronizing transmission and reception of multi-channel information being multiplexed over a single transmission line.

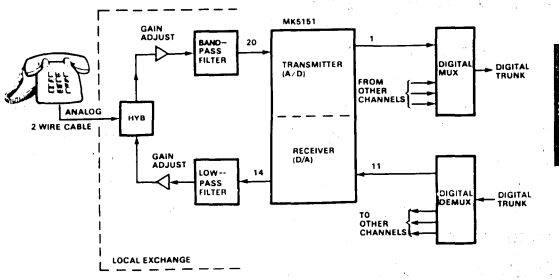
The pin configuration of the MK5151 is shown in Figure 1.

PIN CONNECTIONS
Figure 1



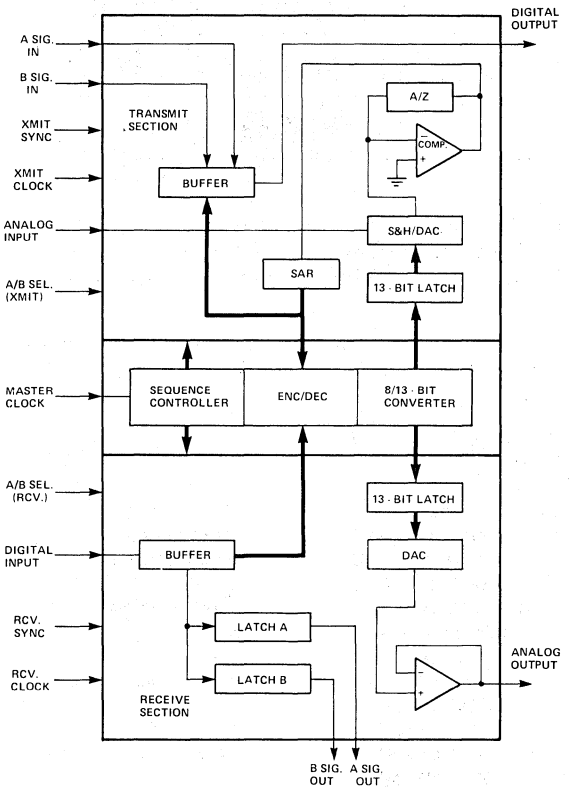
A block diagram of a PCM system using the MK5151 is shown in Figure 2.

PCM SYSTEM BLOCK DIAGRAM
Figure 2



FUNCTIONAL DESCRIPTION: (Refer to Figure 3 for a Block Diagram)

MK5151 BLOCK DIAGRAM
Figure 3



POSITIVE AND NEGATIVE REFERENCE VOLTAGES ($+V_{REF}$ and $-V_{REF}$) Pins 19 and 18

These inputs provide the conversion references for the digital-to-analog converters in the MK5151. $+V_{REF}$ and $-V_{REF}$ must maintain 100ppM/°C regulation over the operating temperature range. Variation of the reference directly affects system gain.

ANALOG INPUT, Pin 20

Voice-frequency analog signals which are bandwidth-limited to 4kHz are input at this pin. Typically, they are then sampled at an 8kHz rate (Refer to Figure 4.). The analog input must remain between $+V_{REF}$ and $-V_{REF}$ for accurate conversion. The recommended input interface circuit is shown in Figure 11.

MASTER CLOCK, Pin 22

This signal provides the basic timing and control signals required for all internal conversions. It does not have to be synchronized with RCV. SYNC, RCV. CLOCK, XMIT SYNC or XMIT CLOCK and is not internally related to them.

XMIT SYNC, Pin 23 (Refer to Figure 12 for the Timing Diagram)

This input is synchronized with XMIT CLOCK. When XMIT SYNC goes high, the digital output is activated and the A/D conversion begins on the next positive edge of MASTER CLOCK. The conversion by MASTER CLOCK can be asynchronous with XMIT CLOCK. The serial output data is clocked out by the positive edges of XMIT CLOCK. The negative edge of XMIT SYNC causes the digital output to become three-state. XMIT SYNC must go low for at least 1 master clock prior to the transmission of the next digital word. (Refer to Figure 14).

XMIT CLOCK, Pin 2 (Refer to Figure 12 for the Timing Diagram)

The on-chip 8-bit output shift register of the MK5151 is unloaded at the clock rate present on this pin. Clock rates of 64kHz-2.1MHz can be used for XMIT CLOCK. The positive edge of the INTERNAL CLOCK transfers the data from the master to the slave of a master-slave flip-flop (Refer to Figure 5). If the positive edge of XMIT SYNC occurs after the positive edge of XMIT CLOCK, XMIT SYNC will determine when the first positive edge of INTERNAL CLOCK will occur. In this event, the hold time for the first clock pulse is measured from the positive edge of XMIT SYNC.

RCV. SYNC, Pin 6 (Refer to Figure 13 for the timing diagram)

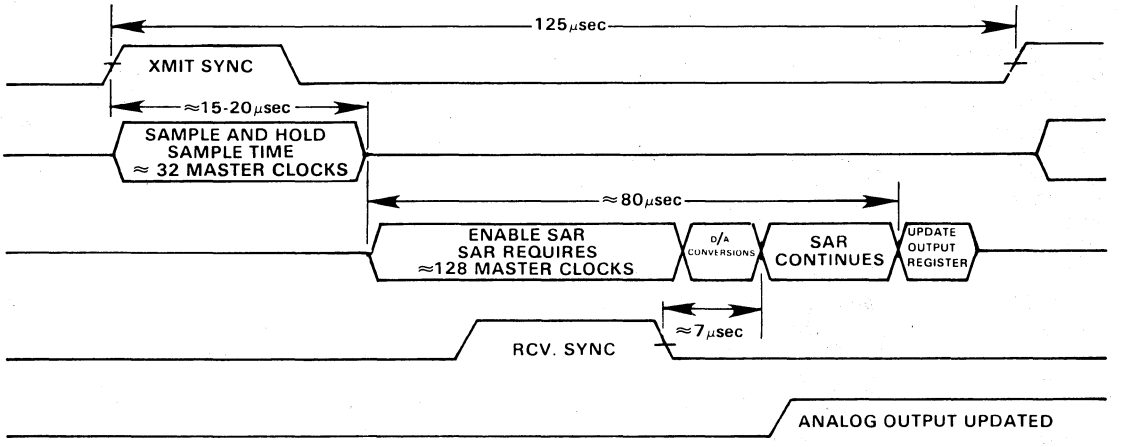
This input is synchronized with RCV. CLOCK and serial data is clocked in by RCV. CLOCK. Duration of the RCV. SYNC pulse is approximately 8 RCV. CLOCK periods. The conversion from digital-to-analog starts after the negative edge of the RCV. SYNC pulse (Refer to Figure 4). The negative edge of RCV. SYNC should occur before the 9th positive clock edge to insure that only eight bits are clocked in. RCV. SYNC must stay low for 17 MASTER CLOCKS (min.) before the next digital word is to be received (Refer to Figure 15).

RCV CLOCK, Pin 7 (Refer to Figure 13 for Timing Diagram)

The on-chip 8-bit shift register for the MK5151 is loaded at the clock rate present on this pin. Clock rates of 64kHz-2.1MHz can be used for RCV. CLOCK. Valid data should be applied to the digital input before the positive edge of the internal clock (Refer to Figure 5). This set up time, t_{RDS}, allows the data to be transferred into the MASTER of a master-slave flip-flop. The positive edge of the INTERNAL CLOCK transfers the data to the SLAVE of the master-slave flip-flop. A hold time, t_{RDH}, is required to complete this transfer. If the rising edge of RCV. SYNC occurs after the first rising edge of RCV. CLOCK, RCV. SYNC will determine when the first positive edge of INTERNAL CLOCK will occur. In this

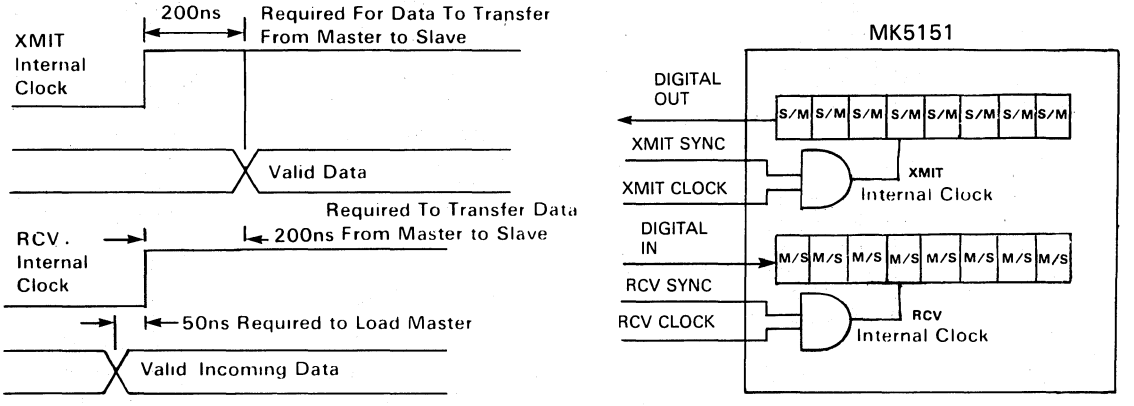
A/D, D/A CONVERSION TIMING

Figure 4



DATA INPUT/OUTPUT TIMING

Figure 5



event, the set-up and hold times for the first clock pulse should be measured from the positive edge of RCV. SYNC.

DIGITAL OUTPUT, Pin 1

The MK5151 output register stores the 8-bit encoded sample of the analog input. This 8-bit word is shifted out under control of XMIT SYNC and XMIT CLOCK. When XMIT SYNC is low, the DIGITAL OUTPUT is an open circuit. When XMIT SYNC is high, the state of the DIGITAL OUTPUT is determined by the value of the output bit in the serial shift register. The output is composed of a Sign Bit, 3 Chord Bits, and 4 Step Bits. The Sign Bit indicates the polarity of the analog input while the Chord and Step Bits indicate the magnitude. In the first Chord, the Step Bit has a value of 0.6mV. In the second Chord, the Step Bit has a value of 1.2mV. This doubling of the step value continues for each of the six successive Chords.

Each Chord has a specific value and the Step Bits, 16 in each Chord, specify the displacement from that value (Refer to Table 1). Thus the output, which follows the μ-255 law, has resolution that is proportional to the input level rather than to full scale. This provides the resolution of a 12-bit A/D converter at low input levels and that of a 6-bit converter as the input approaches full scale. The transfer characteristic of the A/D converter (μ-law Encoder) is shown in Figure 6.

DIGITAL OUTPUT CODE μ-LAW

Table 1

	Chord Code	Chord Value	Step Value
1.	111	0.0mV	0.613mV
2.	110	10.11mV	1.226mV
3.	101	30.3mV	2.45mV
4.	100	70.8mV	4.90mV
5.	011	151.7mV	9.81mV
6.	010	313mV	19.61mV
7.	001	637mV	39.2mV
8.	000	1.284V	78.4mV

EXAMPLE:

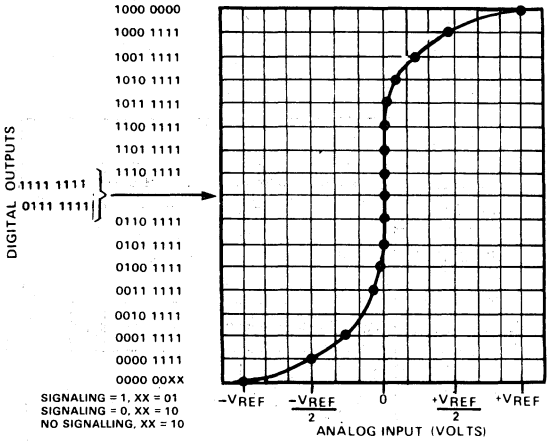
1 100 1101 = +70.8mV + (2 x 4.90mV)

Sign Bit Chord Step Bits

If the sign bit were a zero, then both plus signs would be changed to minus signs.

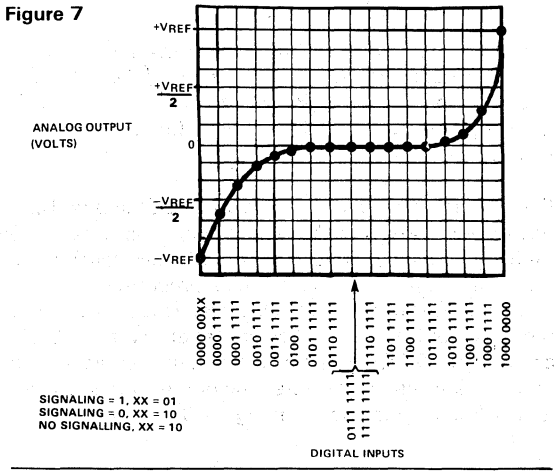
A/D CONVERTER (μ-Law Encoder) TRANSFER CHARACTERISTIC

Figure 6



D/A CONVERTER (μ-Law Decoder) TRANSFER CHARACTERISTIC

Figure 7



DIGITAL INPUT, Pin 11

The MK5151 input register accepts the 8-bit sample of an analog value and loads it under control of RCV. SYNC and RCV. CLOCK. The timing diagram is shown in Figure 13. When RCV. SYNC goes high, the MK5151 uses RCV. CLOCK to clock the serial data into its input register. RCV. SYNC goes low to indicate the end of serial input data. The 8 bits of the input data have the same functions described for the SERIAL OUTPUT. The transfer characteristic of the D/A converter (μ-law Decoder) is shown in Figure 7.

ANALOG OUTPUT, Pin 14

The analog output is in the form of voltage steps (100% duty cycle) having amplitude equal to the analog sample which was encoded. This waveform is then filtered with an external low-pass filter with sinx/x correction to recreate the sampled voice signal. When the 8th bit of the word is a signalling bit, it is assigned a value of ½ step. This results in a lower system quantization error rate than would result if the bit were arbitarily set to 0 (no step) or 1 (full step).

OPERATION OF CODEC WITH 64kHz XMIT/RCV. CLOCK FREQUENCIES

XMIT/RCV. SYNC must not be allowed to remain at a logic "1" state. XMIT SYNC is required to be at a logic "0" state for 1 master clock period (min.) before the next digital word is transmitted. RCV. SYNC is required to be at a logic "0" state for 17 master clock periods (min.) before the next digital word is received (Refer to Figures 14 and 15).

A/B SIGNAL IN, Pins 4 and 5

These two pins allow insertion of signalling information into the transmitted data stream. The inserted information occurs as the 8th bit (LSB) in the transmitted word. A positive transition occuring on A/B SEL (XMIT) selects A SIGNAL IN while a negative transition selects B SIGNAL IN.

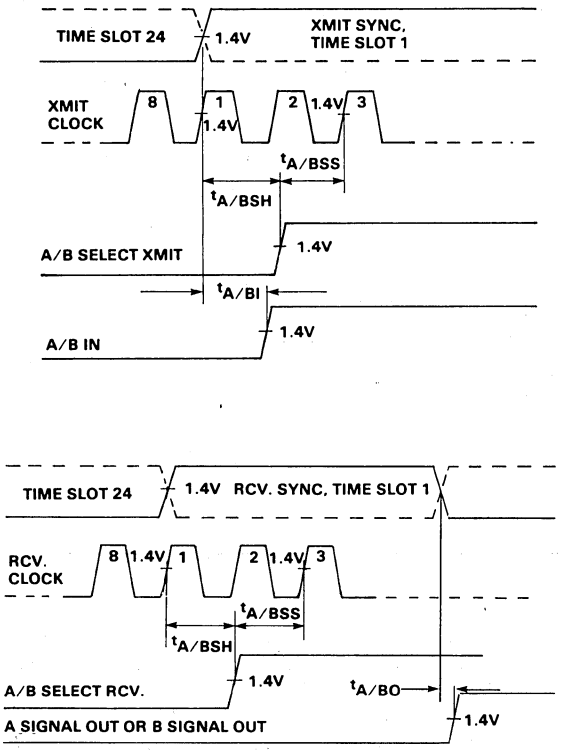
A/B SIGNAL OUT, Pins 9 and 10

These two pins are provided to output received signalling information. A positive transition on A/B SEL (RCV.) routes the signal bit to A SIGNAL OUT while a negative transition routes the signal bit (bit 8) to B SIGNAL OUT. Refer to Figure 8.

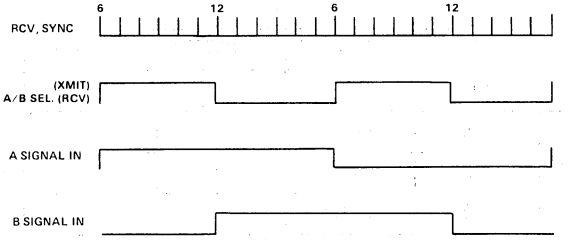
A/B SEL (XMIT), Pin 3

This input selects either A SIGNAL IN or B SIGNAL IN as described in the A/B SIGNAL IN paragraph above, and should be changed only at the start of the 6th and 12th frames as shown in Figure 9.

A/B SELECT TIMING
Figure 8



SIGNALLING TIMING REQUIREMENTS FOR PERFORMANCE EVALUATION
Figure 9



A/B SEL (RCV.), Pin 8

This input routes the signalling bit, bit 8, either to A SIGNAL OUT or to B SIGNAL OUT as described in the A/B SIGNAL OUT paragraph above, and should be changed only at the start of the 6th and 12th frames as shown in Figure 9.

OFFSET NULL

The offset null feature of the MK5151 eliminates long-term drift errors and conversion errors due to temperature changes by going through an offset adjustment cycle before every conversion, thus guaranteeing accurate A/D conversion for inputs near ground. There is no offset adjust of the output amplifier because, since the output is intended to be AC - coupled to the external filter, the resultant DC error ($V_{OFFSET/O}$) will have no effect. The sign bit is not used to null the analog input. Therefore, for an analog input of 0 volts, the sign bit will be stable.

PERFORMANCE EVALUATION

The equipment connections shown in Figure 10 can be used to evaluate the performance of the MK5151. An analog signal provided by the HP3551A Transmission Test Set is connected to the Analog Input (Pin 20) of the MK5151. The Digital Output of the CODEC is tied back to the Digital Input and the Analog Output is fed through a low-pass filter to the HP3551A. Remaining pins of the MK5151 are connected as follows:

(1) A/B SEL. (RCV.) is tied to A/B SEL. (XMIT).
(2) RCV. SYNC is tied to XMIT SYNC.
(3) XMIT CLOCK is tied to MASTER CLOCK. The signal is inverted and tied to RCV. CLOCK.

The following timing signals are required:

(1) MASTER CLOCK = 1.536 MHz
(2) XMIT SYNC repetition rate = 8kHz
(3) XMIT SYNC width = 8 MASTER CLOCK periods

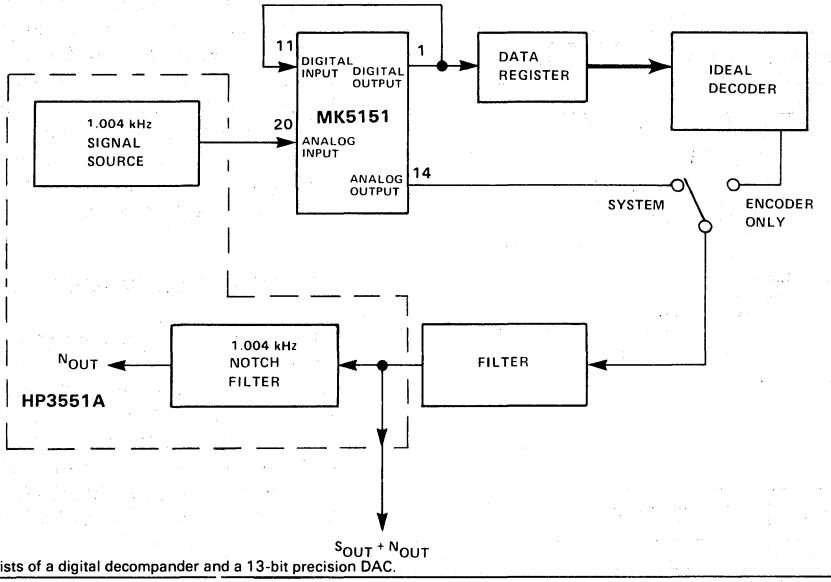
Additional timing signals are shown in Figure 9.

When all the above requirements are met, the setup of Figure 10 permits the measurement of synchronous system performance over a wide range of analog inputs. The data register and ideal decoder provide a means of checking the encoder portion of the MK5151 independently of the decoder section. To test the system in the asynchronous mode, MASTER CLOCK should be separated from XMIT CLOCK and MASTER CLOCK should be separated from RCV. CLOCK. XMIT CLOCK and RCV. CLOCK are separated also.

Some experimental results obtained with the MK5151 are shown in Figure 16 and Figure 17. In each case, both the measured results and the corresponding D3 Channel Bank specifications are shown. The MK5151 exceeds the requirements for Signal-to-Distortion ratio (Figure 17) and for Gain Tracking (Figure 16).

SYSTEM CHARACTERISTICS TEST CONFIGURATION

Figure 10



NOTE: The ideal decoder consists of a digital decompander and a 13-bit precision DAC.

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage, V+ ..... +6V
DC Supply Voltage, V– ..... –6V
Ambient Operating Temperature, T_A ..... 0°C to 70°C
Storage Temperature ..... –55°C to +125°C
Package Dissipation at 25°C (Derated 9mW/°C when soldered into PCB) 500mW
Digital Input ..... $-0.5V \leq V_{IN} \leq V+$
Analog Input ..... $V- \leq +V_{IN} \leq V+$
$+V_{REF}$ ..... $-0.5V \leq +V_{REF} \leq V+$
$-V_{REF}$ ..... $V- \leq -V_{REF} \leq 0.5V$

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL OPERATING CHARACTERISTICS

POWER SUPPLY REQUIREMENTS

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V+	Positive Supply Voltage	4.75	5.0	5.25	V	
V–	Negative Supply Voltage	–5.25	–5.0	–4.75	V	
$+V_{REF}$	Positive Reference Voltage	2.375	2.5	2.625	V	1
$-V_{REF}$	Negative Reference Voltage	–2.625	–2.5	–2.375	V	1

TEST CONDITIONS: V+ = 5.0 V, V- = -5.0 V, + V_{REF} = 2.5 V, -V_{REF} = -2.5 V, T_A = 0°C to 70°C

DC CHARACTERISTICS

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
R_{INAS}	Analog Input Resistance During Sampling		2		kΩ	2
R_{INANS}	Analog Input Resistance Non-Sampling		100		MΩ	
C_{INA}	Analog Input Capacitance		150	250	pF	2

DC CHARACTERISTICS CONTINUED

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
$V_{OFFSET/I}$	Analog Input Offset Voltage		±1	±8	mV	2
R_{OUTA}	Analog Output Resistance		20	50	Ω	
I_{OUTA}	Analog Output Current	0.25	0.5		mA	
$V_{OFFSET/O}$	Analog Output Offset Voltage		-200	± 850	mV	
I_{INLOW}	Logic Input Low Current (V_{IN} = 0.8V) Digital Input, Clock Input, Sync Input		± 0.1	±10	μA	3
I_{INHIGH}	Logic Input High Current (V_{IN} = 2.4V) Digital Input, Clock Input, Sync Input		-0.25	-0.8	mA	3
C_{DO}	Digital Output Capacitance		8	12	pF	
I_{DOL}	Digital Output Leakage Current		± 0.1	±10	μA	
V_{OUTLOW}	Logic Output Low Voltage Digital Output, A/B Signal Out			0.4	V	4
$V_{OUTHIGH}$	Logic Output High Voltage Digital Output, A/B Signal Out	3.9			V	4
I+	Positive Supply Current		4	10	mA	5
I-	Negative Supply Current		2	6	mA	5
I_{REF+}	Positive Reference Current		4	20	μA	
I_{REF-}	Negative Reference Current		4	20	μA	

AC CHARACTERISTICS (Refer to Figure 12 and Figure 13)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
F_M	Master Clock Frequency	1.5	1.544	2.1	MHz	
F_R, F_X	Receive, Transmit Clock Frequency	0.064	1.544	2.1	MHz	
PW_{CLK}	Clock Pulse Width (MASTER, XMIT, RCV.)	200			ns	
t_{RC}	Clock Rise Time (MASTER, XMIT, RCV.)			25% of PW_{CLK}	ns	
t_{RS},t_{FS}	Sync Fall, Rise Time (XMIT, RCV.)			25% of PW_{CLK}	ns	
t_{DIR}, t_{DIF}	Digital Input Rise, Fall Time			25% of PW_{CLK}	ns	
t_{WSX}, t_{WSR}	Sync Pulse Width (XMIT, RCV.)		$\frac{8}{F_X(F_R)}$		μs	
t_{PS}	Sync Pulse Period (XMIT, RCV.)		125		μs	
t_{XCS}	XMIT Clock-to-XMIT Sync Delay	50%of t_{FC} (t_{RS})			ns	6
t_{XCSN}	XMIT Clock-to-XMIT Sync (Negative Edge) Delay	200			ns	
t_{XSS}	XMIT Sync Set-Up Time	200			ns	
t_{XDD}	XMIT Data Delay	0		200	ns	4
t_{XDP}	XMIT Data Present	0		200	ns	4
t_{XDT}	XMIT Data Three State			150	ns	4
t_{DOF}	Digital Output Fall Time		50	100	ns	4
t_{DOR}	Digital Output Rise Time		50	100	ns	4

AC CHARACTERISTICS CONTINUED (Refer to Figure 12 and 13)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
t_{SRC}	RCV. Sync-to-RCV. Clock Delay	50% of t_{RC} (t_{FS})			ns	6
t_{RDS}	RCV. Data Set-Up Time	50			ns	7
t_{RDH}	RCV. Data Hold Time	200			ns	7
t_{RCS}	RCV. Clock-to-RCV. Sync Delay	200			ns	
t_{RSS}	RCV. Sync Set-Up Time	200			ns	7
t_{SAO}	RCV. Sync-to-Analog Output Delay		7		μs	
$t_{A/BI}$	A/B Signalling Input Setup Time			200	ns	
$t_{A/BSH}$	A/B Select Hold Time	200			ns	
$t_{A/BSS}$	A/B Select Setup Time	400			ns	
$t_{A/BO}$	A/B Signalling Output Delay		200	400	ns	
SLEW+	Analog Output Positive Slew Rate		1		V/μs	
SLEW–	Analog Output Negative Slew Rate		1		V/μs	
DROOP	Analog Output Droop Rate		25		μV/μs	

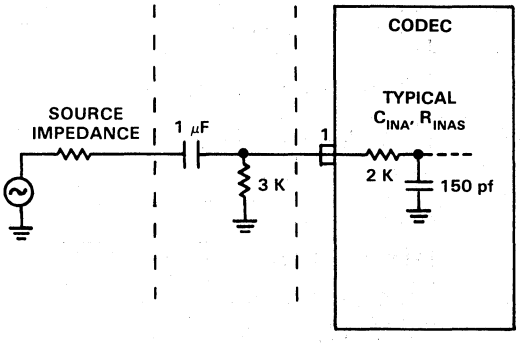
SYSTEM CHARACTERISTICS (Refer to Figures 16 and 17)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	TEST COND.
S/D	Signal-to-Distortion Ratio	35 29 24	39 34 29		dB dB dB	Analog Input=0 to -30dBm0 Analog Input=-40dBm0 Analog Input=-45dm0
GT	Gain Tracking	-0.4 -0.8 -2.5	±0.1 ±0.1 ±0.2	+0.4 +0.8 +2.5	dB dB dB	Analog Input=+3 to -37dBm0 Analog Input=-37 to -50dBm0 Analog Input=-50 to -55dBm0
N_{IC}	Idle Channel Noise		10	18	dBrnc0	Analog Input=0 Volts Note 2
TLP	Transmission Level Point		+4		dB	600Ω

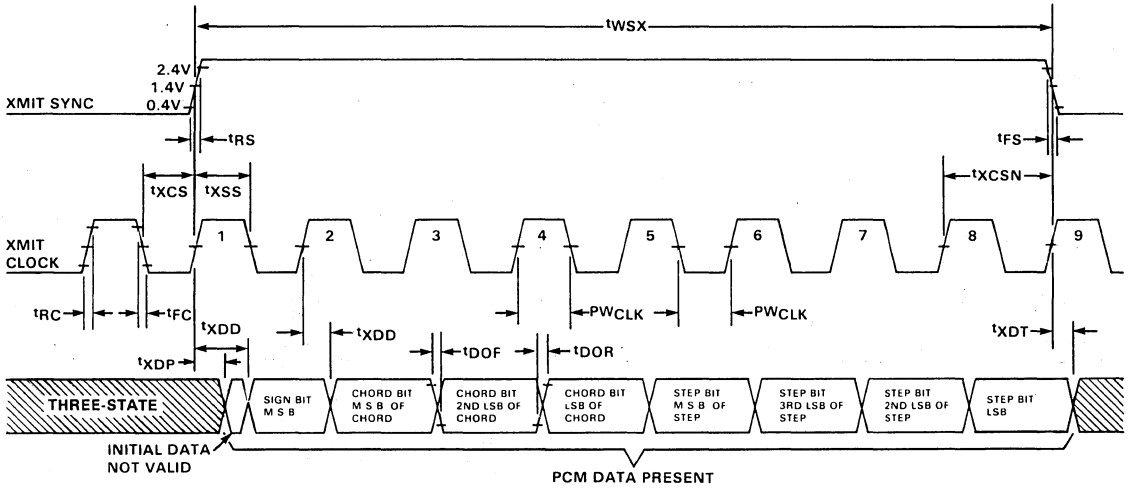
NOTES:

1. $+V_{REF}$ and $-V_{REF}$ must be matched within ± 1% in order to meet system requirements.
2. Sampling is accomplished by charging an internal capacitor; therefore, the designer should avoid excessive source impedance. Input related device characteristics are derived using the Recommended Analog Input Circuit. See Figure 11.
3. When a transistion from a "1" to a "0" takes place, the user must sink the "1" current until reaching the "0" level.
4. Driving 30pF with I_{OH} = -100μA, I_{OL} = 500μA.
5. Results in 30 mW typical power dissipation (clocks applied) under normal operating conditions.
6. This delay is necessary to avoid overlapping CLOCK and SYNC.
7. The first bit of data is loaded when the Sync and Clock are both "1" during bit time 1 as shown on RCV timing diagram.

RECOMMENDED ANALOG INPUT CIRCUIT
Figure 11

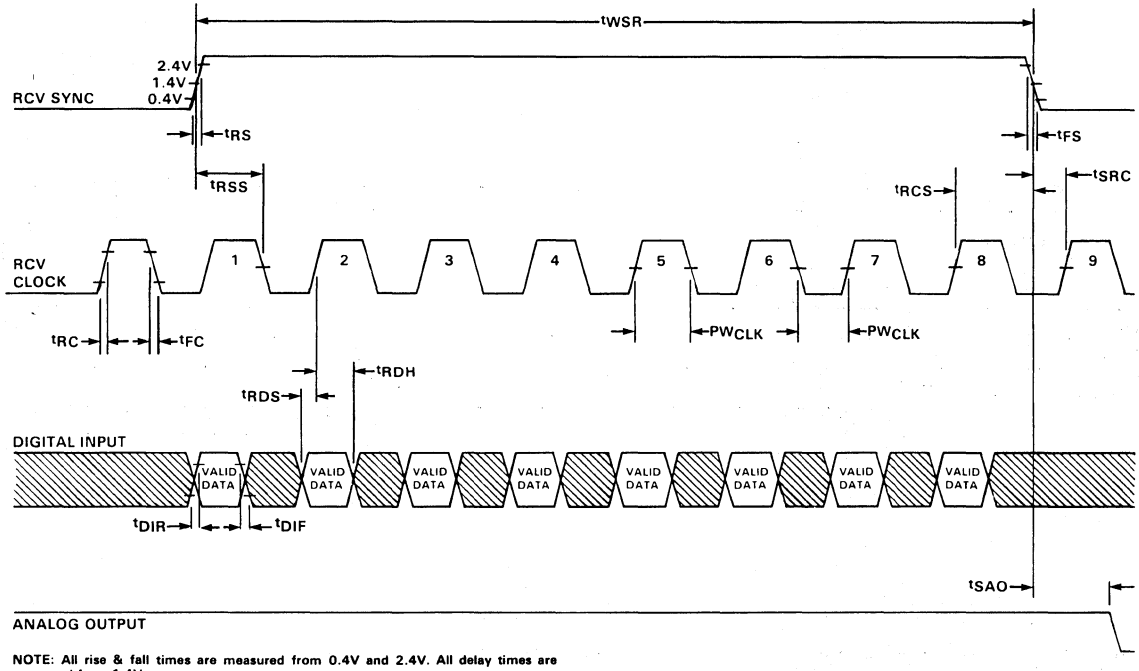


TRANSMITTER SECTION TIMING
Figure 12



NOTE: All rise and fall times are measured from 0.4V and 2.4V.
All delay times are measured from 1.4V.

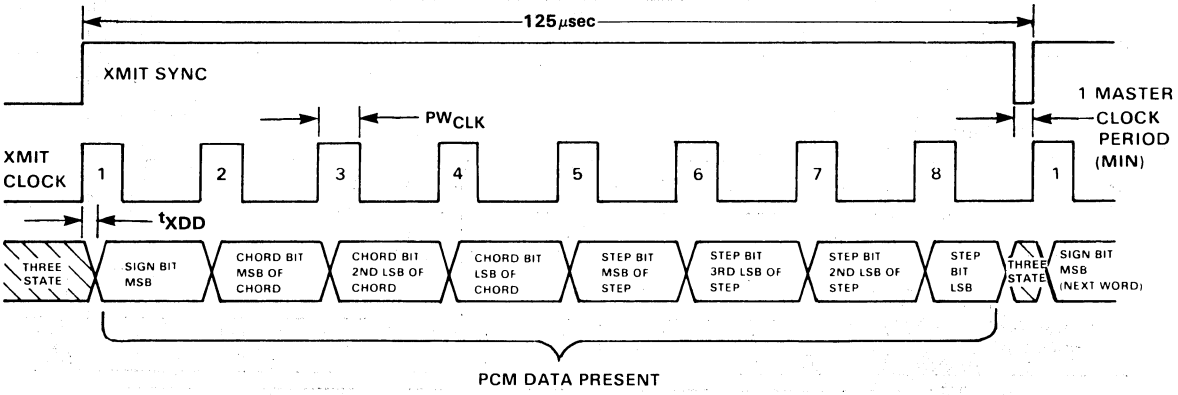
RECEIVER SECTION TIMING
Figure 13



NOTE: All rise & fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

64kHz OPERATION, TRANSMITTER SECTION TIMING

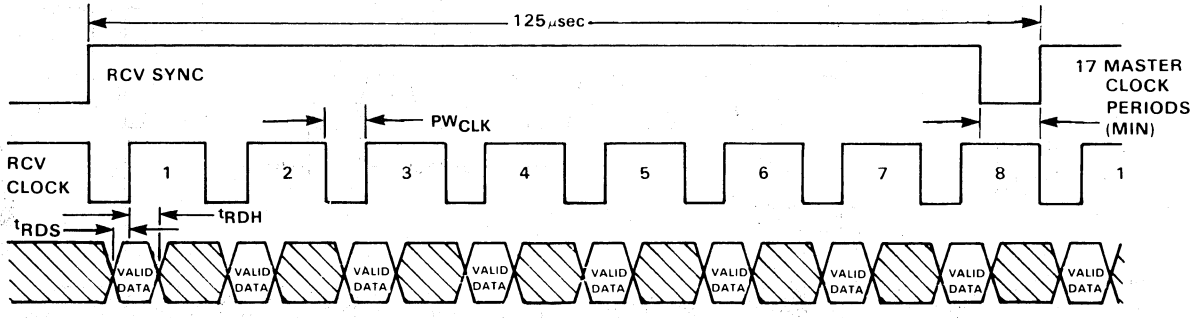
Figure 14



NOTE: All rise and fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

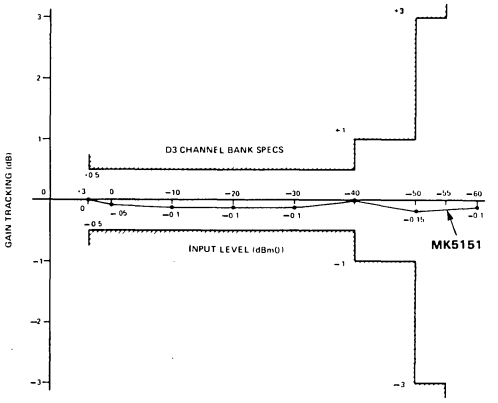
64kHz OPERATION, RECEIVER SECTION TIMING

Figure 15

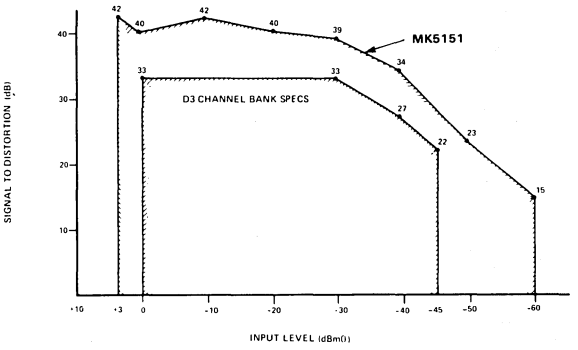


NOTE: All rise and fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

MK5151 GAIN TRACKING PERFORMANCE
Figure 16



MK5151 S/D RATIO VS. INPUT LEVEL
Figure 17



A-Law Companding CODEC
MK5156(J/P)

FEATURES

- ±5-Volt Power Supplies
- Low Power Dissipation - 30mW (Typ)
- Follows the A-Law Companding Code
- Includes CCITT Recommended Even-Order-Bit Inversion
- Synchronous or Asynchronous Operation
- On-Chip Sample and Hold
- On-Chip Offset Null Circuit Eliminates Long-Term Drift Errors and Need for Trimming
- Single 16-Pin Package
- Minimal External Circuitry Required
- Serial Data Output of 64kb/s-2.1 Mb/s at 8kHz Sampling Rate
- Separate Analog and Digital Grounding Pins Reduce System Noise Problems

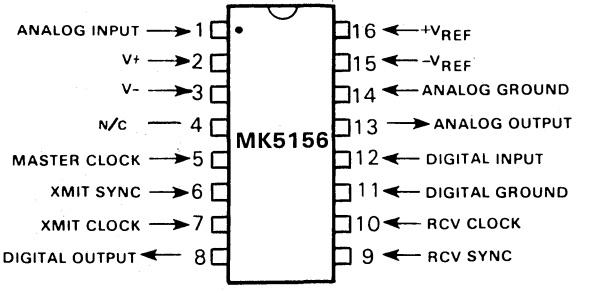
DESCRIPTION

The MK5156 is a monolithic CMOS companding CODEC which contains two sections: (1) An analog-to-digital converter which has a transfer characteristic conforming to the A-law companding code and (2) a digital-to-analog converter which also conforms to the A-law code.

These two sections form a coder-decoder which is designed to meet the needs of the telecommunications industry for per-channel voice-frequency codecs used in digital switching and transmission systems. Digital input and output are in serial format. Actual transmission and reception of 8-bit data words containing the analog information is done at a 64kb/s-2.1 Mb/s rate with analog signal sampling occuring at an 8kHz rate. A sync pulse input is provided for synchronizing transmission and reception of multi-channel information being multiplexed over a single transmission line.

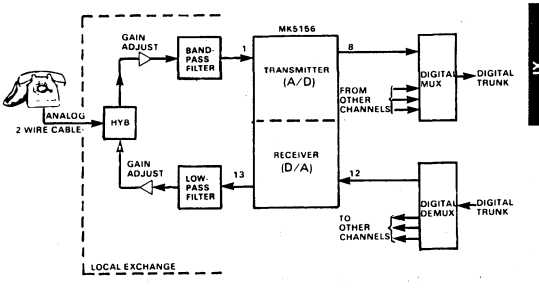
The pin configuration of the MK5156 is shown in Figure 1.

PIN CONNECTIONS
Figure 1



A block diagram of a PCM system using the MK5156 is shown in Figure 2.

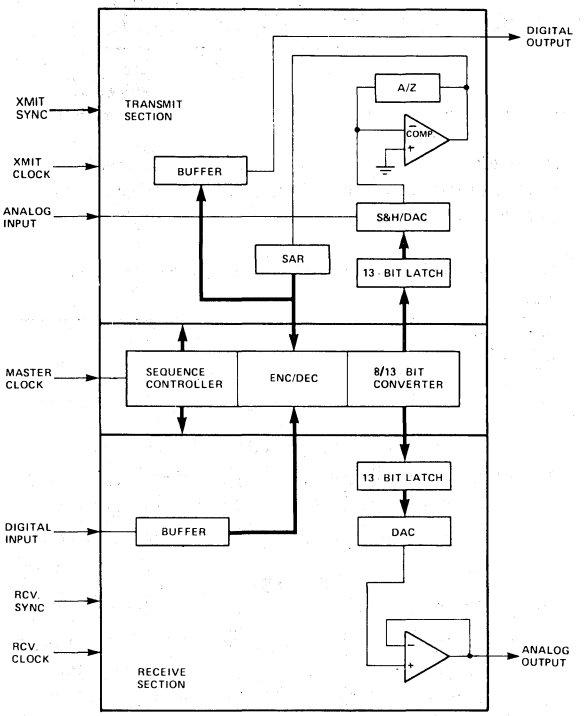
PCM SYSTEM BLOCK DIAGRAM
Figure 2



FUNCTIONAL DESCRIPTION: (Refer to Figure 3 for a Block Diagram)

MK5156 BLOCK DIAGRAM

Figure 3



POSITIVE AND NEGATIVE REFERENCE VOLTAGES ($+V_{REF}$ and $-V_{REF}$) Pins 16 and 15

These inputs provide the conversion references for the digital-to-analog converters in the MK5156. $+V_{REF}$ and $-V_{REF}$ must maintain 100ppM/°C regulation over the operating temperature range. Variation of the reference directly affects system gain.

ANALOG INPUT, Pin 1

Voice-frequency analog signals which are bandwidth-limited to 4kHz are input at this pin. Typically, they are then sampled at an 8kHz rate (Refer to Figure 4.). The analog input must remain between $+V_{REF}$ and $-V_{REF}$ for accurate conversion. The recommended input interface circuit is shown in Figure 9.

MASTER CLOCK, Pin 5

This signal provides the basic timing and control signals required for all internal conversions. It does not have to be synchronized with RCV. SYNC, RCV. CLOCK, XMIT SYNC or XMIT CLOCK and is not internally related to them.

XMIT SYNC, Pin 6 (Refer to Figure 10 for the Timing Diagram)

This input is synchronized with XMIT CLOCK. When XMIT SYNC goes high, the digital output is activated and the A/D conversion begins on the next positive edge of MASTER CLOCK. The conversion by MASTER CLOCK can be asynchronous with XMIT CLOCK. The serial output data is clocked out by the positive edges of XMIT CLOCK. The negative edge of XMIT SYNC causes the digital output to become three-state. XMIT SYNC must go low for at least 1 master clock prior to the transmission of the next digital word (Refer to Figure 12).

XMIT CLOCK, Pin 7 (Refer to Figure 10 for the Timing Diagram)

The on-chip 8-bit output shift register of the MK5156 is unloaded at the clock rate present on this pin. Clock rates of 64kHz-2.1MHz can be used for XMIT CLOCK. The positive edge of the INTERNAL CLOCK transfers the data from the master to the slave of a master-slave flip-flop (Refer to Figure 5). If the positive edge of XMIT SYNC occurs after the positive edge of XMIT CLOCK, XMIT SYNC will determine when the first positive edge of INTERNAL CLOCK will occur. In this event, the hold time for the first clock pulse is measured from the positive edge of XMIT SYNC.

RCV. SYNC, Pin 9 (Refer to Figure 11 for the Timing Diagram)

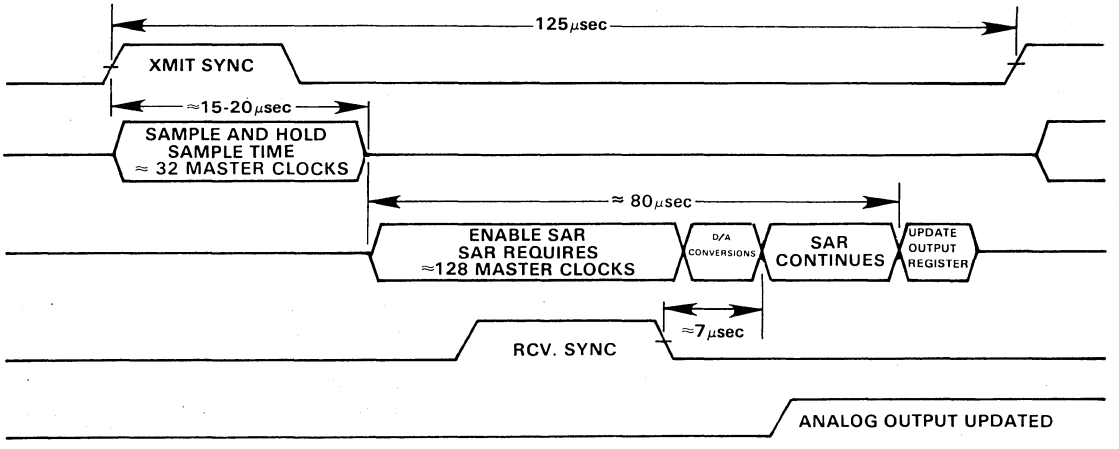
This input is synchronized with RCV. CLOCK and serial data is clocked in by RCV. CLOCK. Duration of the RCV SYNC pulse is approximately 8 RCV. CLOCK periods. The conversion from digital-to-analog starts after the negative edge of the RCV. SYNC pulse (Refer to Figure 4). The negative edge of RCV. SYNC should occur before the 9th positive clock edge to insure that only eight bits are clocked in. RCV. SYNC must stay low for 17 MASTER CLOCKS (min.) before the next digital word is to be received (Refer to Figure 13).

RCV CLOCK, Pin 10 (Refer to Figure 11 for Timing Diagram)

The on-chip 8-bit shift register for the MK5156 is loaded at the clock rate present on this pin. Clock rates of 64kHz-2.1MHz can be used for RCV. CLOCK. Valid data should be applied to the digital input before the positive edge of the internal clock (Refer to Figure 5). This set up time, t_{RDS}, allows the data to be transferred into the MASTER of a master-slave flip-flop. The positive edge of the INTERNAL CLOCK transfers the data to the SLAVE of the master-slave flip-flop. A hold time, t_{RDH}, is required to complete this transfer. If the rising edge of RCV. SYNC occurs after the first rising edge of RCV. CLOCK, RCV. SYNC will determine when the first positive edge of INTERNAL CLOCK will occur. In

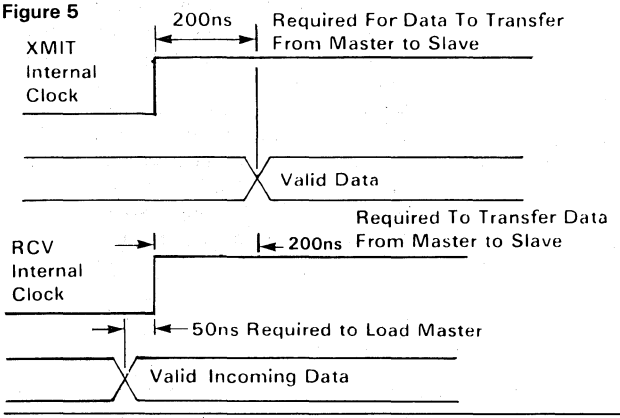
A/D, D/A CONVERSION TIMING

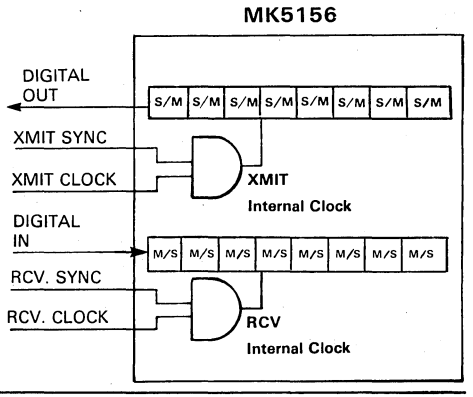
Figure 4



DATA INPUT/OUTPUT TIMING

Figure 5





this event, the set-up and hold times for the first clock pulse should be measured from the positive edge of RCV. SYNC.

DIGITAL OUTPUT, Pin 8

The MK5156 output register stores the 8-bit encoded sample of the analog input. This 8-bit word is shifted out under control of XMIT SYNC and XMIT CLOCK. When XMIT SYNC is low, the DIGITAL OUTPUT is an open circuit. When XMIT SYNC is high, the state of the DIGITAL OUTPUT is determined by the value of the output bit in the serial shift register. The output is composed of a Sign Bit, 3 Chord Bits, and 4 Step Bits. The Sign Bit indicates the polarity of the analog input while the Chord and Step Bits indicate the magnitude. In the first two Chords, the Step Bit has a value of 1.2mV. In the third Chord, the Step Bit has a value of 2.4mV. This doubling of the step value continues for each of the five successive Chords.

Each Chord has a specific value and the Step Bits, 16 in each Chord, specify the displacement from that value (Refer to Table 1). Thus the output, which follows the A-law, has resolution that is proportional to the input level rather than to full scale. This provides the resolution of a 12-bit A/D converter at low input levels and that of a 6-bit converter as the input approaches full scale. The transfer characteristic of the A/D converter (A-law Encoder) is shown in Figure 6.

DIGITAL INPUT, Pin 12

The MK5156 input register accepts the 8-bit sample of an analog value and loads it under control of RCV. SYNC and RCV. CLOCK. The timing diagram is shown in Figure 11. When RCV. SYNC goes high, the MK5156 uses RCV. CLOCK to clock the serial data into its input register. RCV. SYNC goes low to indicate the end of serial input data. The 8 bits of the input data have the same functions described for the DIGITAL OUTPUT. The

DIGITAL OUTPUT CODE: A LAW

Table 1

	Chord Code	Chord Value	Step Value
1.	101	0.0mV	1.221mV
2.	100	20.1mV	1.221mV
3.	111	40.3mV	2.44mV
4.	110	80.6mV	4.88mV
5.	001	161.1mV	9.77mV
6.	000	332mV	19.53mV
7.	011	645mV	39.1mV
8.	010	1.289V	78.1mV

EXAMPLE:

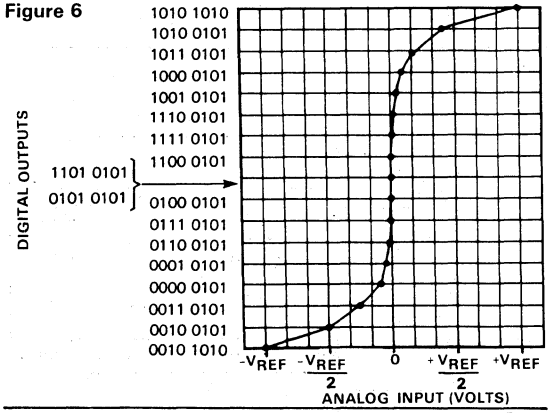
1 110 0111= +80.6mV+ (2 x 4.88mV)

Sign Bit Chord Step Bits

If the sign bit were a zero, then both plus signs would be changed to minus signs.

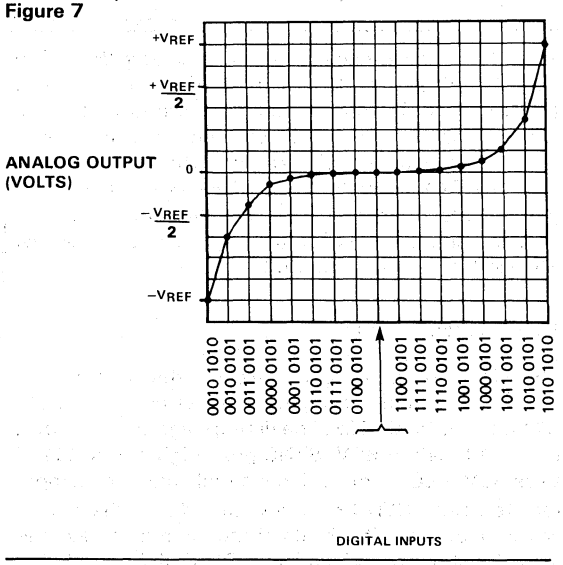
A/D CONVERTER (A-Law Encoder) TRANSFER CHARACTERISTIC

Figure 6



D/A CONVERTER (A-Law Decoder) TRANSFER CHARACTERISTIC

Figure 7



transfer characteristic of the D/A converter (A-law Decoder) is shown in Figure 7.

ANALOG OUTPUT, Pin 13

The analog output is in the form of voltage steps (100% duty cycle) having amplitude equal to the analog sample which was encoded. This waveform is then filtered with an external low-pass filter with sinx/x correction to recreate the sampled voice signal.

OPERATION OF CODEC WITH 64kHz XMIT/RCV. CLOCK FREQUENCIES

XMIT/RCV. SYNC must not be allowed to remain at a logic "1" state. XMIT SYNC is required to be at a logic "0" state for 1 master clock period (min.) before the next digital word is transmitted. RCV. SYNC is required to be at a logic "0" state for 17 master clock periods (min.) before the next digital word is received (Refer to Figures 12 and 13).

OFFSET NULL

The offset null feature of the MK5156 eliminates long-term drift errors and conversion errors due to temperature changes by going through an offset adjustment cycle before every conversion, thus guaranteeing accurate A/D conversion for inputs near ground. There is no offset adjust of the output amplifier because, since the output is intended to be AC - coupled to the external filter, the resultant DC error ($V_{OFFSET/O}$) will have no effect. The sign bit is not used to null the analog input. Therefore, for an analog input of 0 volts, the sign bit will be stable.

PERFORMANCE EVALUATION

The equipment connections shown in Figure 8 can be used to evaluate the performance of the MK5156. An analog signal provided by the HP3552A Transmission Test Set is connected to the Analog Input (Pin 1) of the MK5156. The Digital Output of the CODEC is tied back to the Digital Input and the Analog Output is fed through a low-pass filter to the HP3552A. Remaining pins of the MK5156 are connected as follows:

(1) RCV. SYNC is tied to XMIT SYNC
(2) XMIT CLOCK is tied to MASTER CLOCK. The signal is inverted and tied to RCV. CLOCK.

The following timing signals are required:

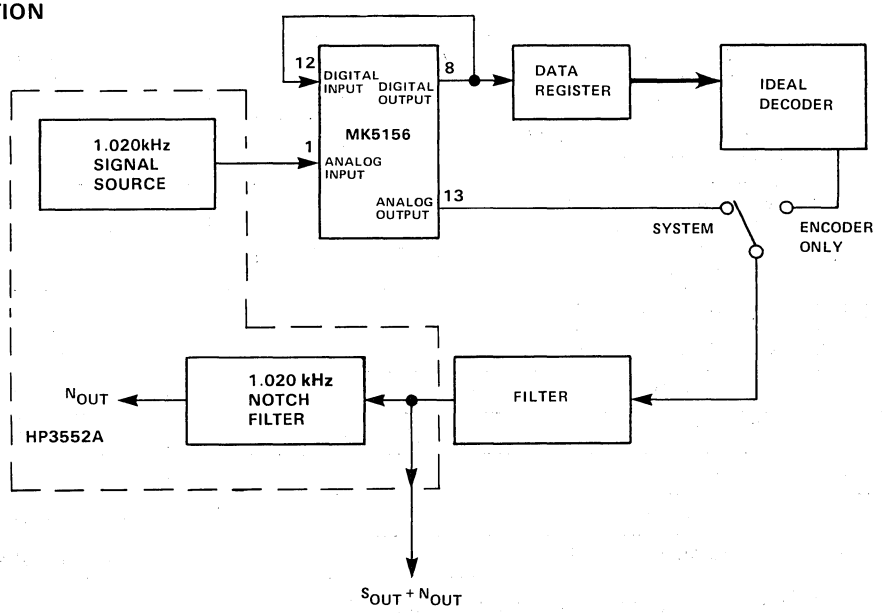
(1) MASTER CLOCK = 1.536 MHz
(2) XMIT SYNC repetition rate = 8kHz
(3) XMIT SYNC width = 8 XMIT CLOCK periods

When all the above requirements are met, the setup of Figure 8 permits the measurement of synchronous system performance over a wide range of analog inputs.

The data register and ideal decoder provide a means of checking the encoder portion of the MK5156 independently of the decoder section. To test the system in the asynchronous mode, MASTER CLOCK should be separated from XMIT CLOCK and MASTER CLOCK should be separated from RCV. CLOCK. XMIT CLOCK and RCV. CLOCK are separated also. Some experimental results obtained with the MK5156 are shown in Figures 14 and 15.

SYSTEM CHARACTERISTICS TEST CONFIGURATION

Figure 8



NOTE: The ideal decoder consists of a digital decompander and a 13-bit precision DAC.

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage, V+ ..... +6V
DC Supply Voltage, V– ..... –6V
Ambient Operating Temperature, T_A ..... 0°C to 70°C
Storage Temperature ..... –55°C to +125°C
Package Dissipation at 25°C (Derated 9mW/°C when soldered into PCB) 500mW
Digital Input ..... $-0.5V \leq V_{IN} \leq V+$
Analog Input ..... $V- \leq V_{IN} \leq V+$
$+V_{REF}$ ..... $-0.5V \leq +V_{REF} \leq V+$
$-V_{REF}$ ..... $V- \leq -V_{REF} \leq +0.5V$

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL OPERATING CHARACTERISTICS
POWER SUPPLY REQUIREMENTS

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V+	Positive Supply Voltage	4.75	5.0	5.25	V	
V–	Negative Supply Voltage	–5.25	–5.0	–4.75	V	
$+V_{REF}$	Positive Reference Voltage	2.375	2.5	2.625	V	1
$-V_{REF}$	Negative Reference Voltage	–2.625	–2.5	–2.375	V	1

TEST CONDITIONS: V+ = 5.0V, V- = -5.0V, + V_{REF} = 2.5V, -V_{REF} = -2.5V, T_A = 0°C to 70°C

DC CHARACTERISTICS

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
R_{INAS}	Analog Input Resistance During Sampling		2		kΩ	2
R_{INANS}	Analog Input Resistance Non-Sampling		100		MΩ	
C_{INA}	Analog Input Capacitance		150	250	pF	2
$V_{OFFSET/I}$	Analog Input Offset Voltage		±1	± 8	mV	2
R_{OUTA}	Analog Output Resistance		20	50	Ω	
I_{OUTA}	Analog Output Current	0.25	0.5		mA	
($V_{OFFSET/O}$)	Analog Output Offset Voltage		-200	± 850	mV	
I_{INLOW}	Logic Input Low Current (V_{IN} = 0.8V) Digital Input, Clock Input, Sync Input		± 0.1	±10	μA	3
I_{INHIGH}	Logic Input High Current (V_{IN} = 2.4V) Digital Input, Clock Input, Sync Input		-0.25	-0.8	mA	3
C_{DO}	Digital Output Capacitance		8	12	pF	
I_{DOL}	Digital Output Leakage Current		± 0.1	±10	μA	
V_{OUTLOW}	Digital Output Low Voltage			0.4	V	4
$V_{OUTHIGH}$	Digital Output High Voltage	3.9			V	4
I+	Positive Supply Current		4	10	mA	5
I–	Negative Supply Current		2	6	mA	5
I_{REF+}	Positive Reference Current		4	20	μA	
I_{REF-}	Negative Reference Current		4	20	μA	

AC CHARACTERISTICS (Refer to Figure 10 and Figure 11)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
F_M	Master Clock Frequency	1.5	2.048	2.1	MHz	
F_R, F_X	XMIT, RCV. Clock Frequency	0.064	2.048	2.1	MHz	
PW_{CLK}	Clock Pulse Width (MASTER, XMIT, RCV.)	200			ns	
t_{RC}, t_{FC}	Clock Rise, Fall Time (MASTER, XMIT, RCV.)			25% of PW_{CLK}	ns	
t_{RS},t_{FS}	Sync Rise, Fall Time (XMIT, RCV.)			25% of PW_{CLK}	ns	
t_{DIR},t_{DIF}	Data Input Rise, Fall Time			25% of PW_{CLK}	ns	
t_{WSX}, t_{WSR}	Sync Pulse Width (XMIT, RCV.)		$\frac{8}{F_X(F_R)}$		μs	
t_{PS}	Sync Pulse Period (XMIT, RCV.)		125		μs	
t_{XCS}	XMIT Clock-to-XMIT Sync Delay	50% of t_{FC}(t_{RS})			ns	6
t_{XCSN}	XMIT Clock-to-XMIT Sync (Negative Edge) Delay	200			ns	

AC CHARACTERISTICS CONTINUED (Refer to Figure 10 and Figure 11)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
t_{XSS}	XMIT Sync Set-Up Time	200			ns	
t_{XDD}	XMIT Data Delay	0		200	ns	4
t_{XDP}	XMIT Data Present	0		200	ns	4
t_{XDT}	XMIT Data Three State			150	ns	4
t_{DOF}	Digital Output Fall Time		50	100	ns	4
t_{DOR}	Digital Output Rise Time		50	100	ns	4
t_{SRC}	RCV. Sync-to-RCV. Clock Delay	50% of t_{RC} (t_{FS})			ns	6
t_{RDS}	RCV. Data Set-Up Time	50			ns	7
t_{RDH}	RCV. Data Hold Time	200			ns	7
t_{RCS}	RCV. Clock-to-RCV. Sync Delay	200			ns	
t_{RSS}	RCV. Sync Set-Up Time	200			ns	7
t_{SAO}	RCV. Sync-to-Analog Output Delay		7		μs	
SLEW+	Analog Output Positive Slew Rate		1		V/μs	
SLEW–	Analog Output Negative Slew Rate		1		V/μs	
DROOP	Analog Output Droop Rate		25		μV/μs	

SYSTEM CHARACTERISTICS (Refer to Figures 14 and 15)

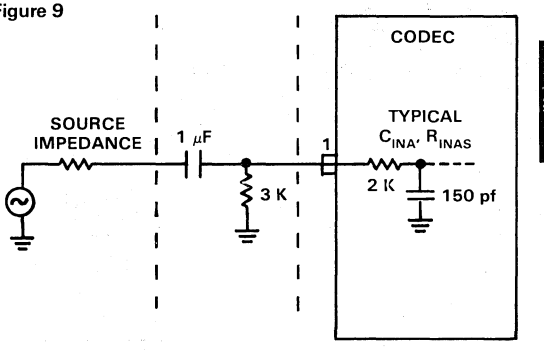
SYM	PARAMETER	MIN	TYP	MAX	UNITS	TEST COND.
S/D	Signal-to-Distortion Ratio	35 29 24	39 34 29		dB dB dB	Analog Input=0 to -30dBm0 Analog Input=-40dBm0 Analog Input=-45dm0
GT	Gain Tracking	-0.4 -0.8 -2.5	±0.1 ±0.1 ±0.2	+0.4 +0.8 +2.5	dB dB dB	Analog Input=+3 to -37dBm0 Analog Input=-37 to -50dBm0 Analog Input=-50 to -55dBm0
N_{IC}	Idle Channel Noise		-80	-68	dBm0p	Analog Input=0 Volts; note 2.
TLP	Transmission Level Point		+4		dB	600Ω

NOTES:

1. $+V_{REF}$ and $-V_{REF}$ must be matched within ± 1% in order to meet system requirements.
2. Sampling is accomplished by charging an internal capacitor; therefore, the designer should avoid excessive source impedance. Input related device characteristics are derived using the Recommended Analog Input Circuit. See Figure 9.
3. When a transition from a "1" to a "0" takes place, the user must sink the "1" current until reaching the "0" level.
4. Driving 30pF with I_{OH} = -100 μA, I_{OL} = 500 μA.
5. Results in 30 mW typical power dissipation (clocks applied) under normal operating conditions.
6. This delay is necessary to avoid overlapping Clock and Sync.
7. The first bit of data is loaded when Sync and Clock are both "1" during bit time 1 as shown on RCV. timing diagram.

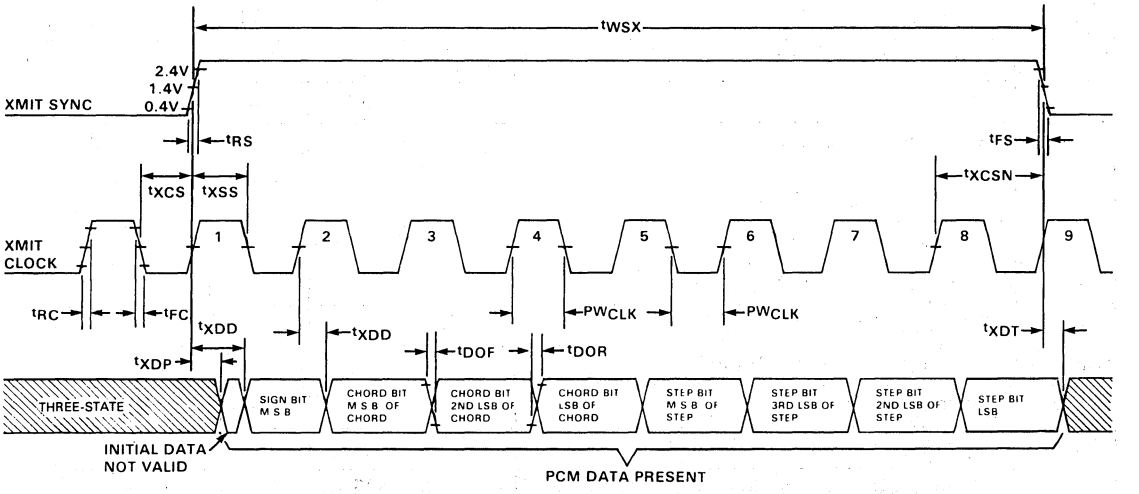
RECOMMENDED ANALOG INPUT CIRCUIT

Figure 9



TRANSMITTER SECTION TIMING

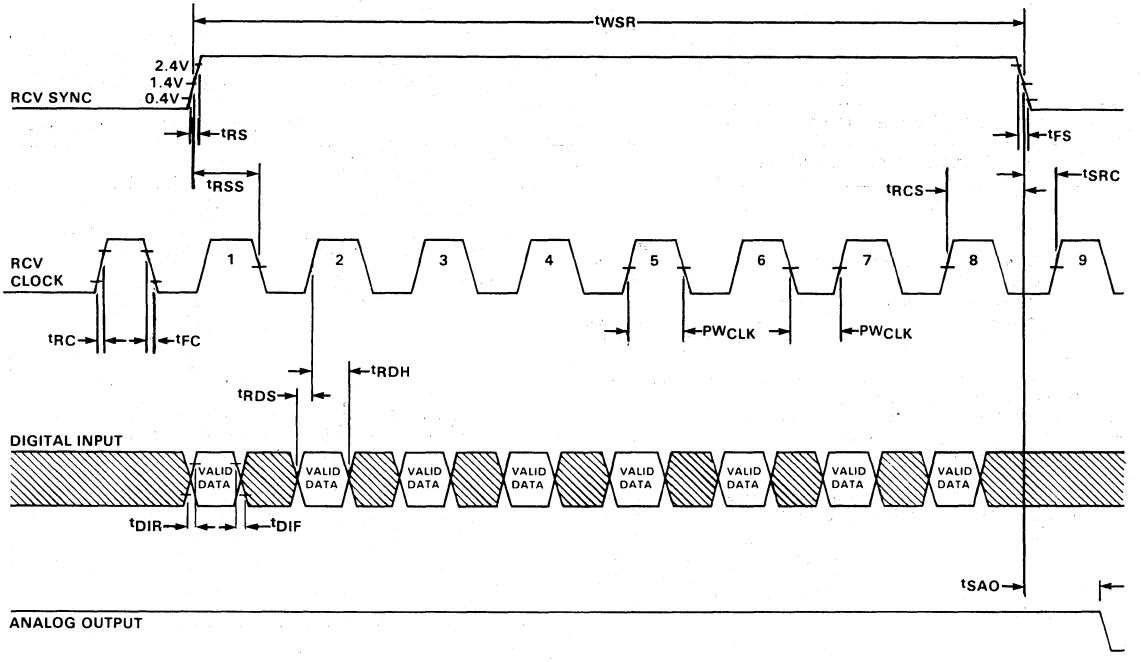
Figure 10



NOTE: All rise and fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

RECEIVER SECTION TIMING

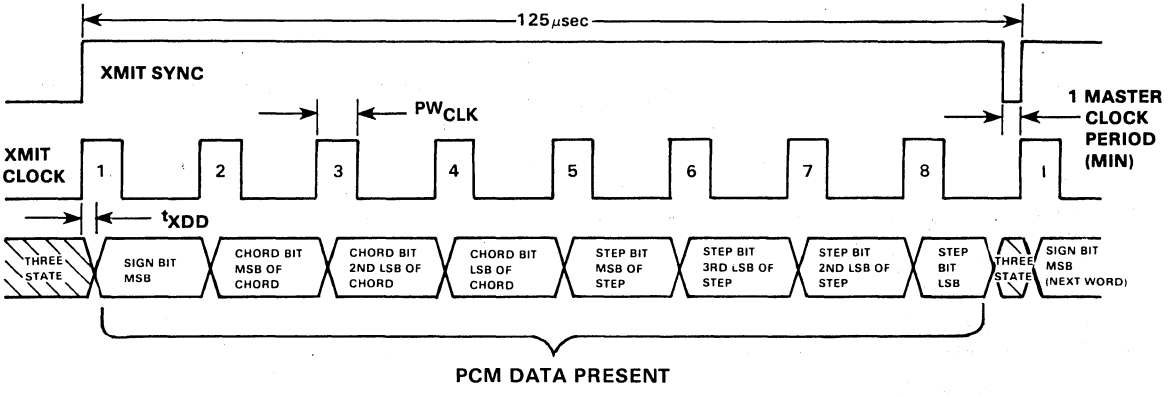
Section 11



NOTE: All rise and fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

64kHz OPERATION, TRANSMITTER SECTION TIMING

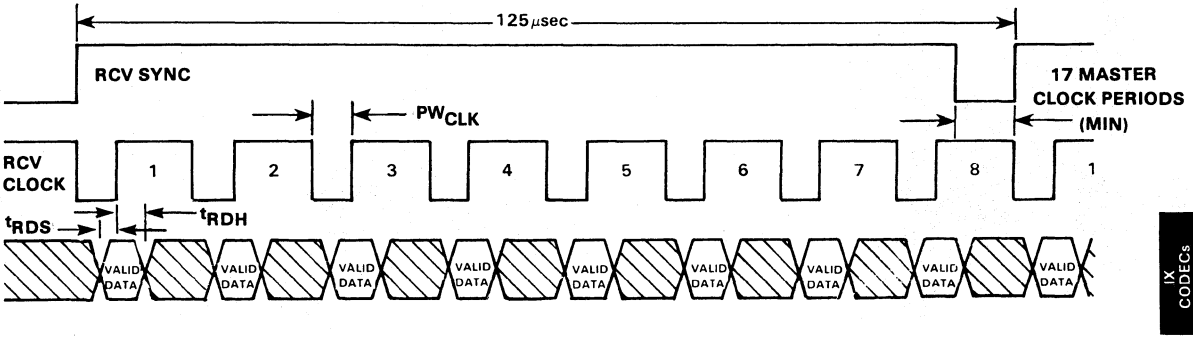
Figure 12



NOTE: All rise and fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

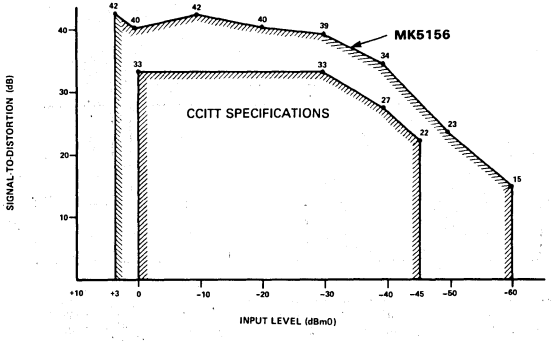
64kHz OPERATION, RECEIVER SECTION TIMING

Figure 13

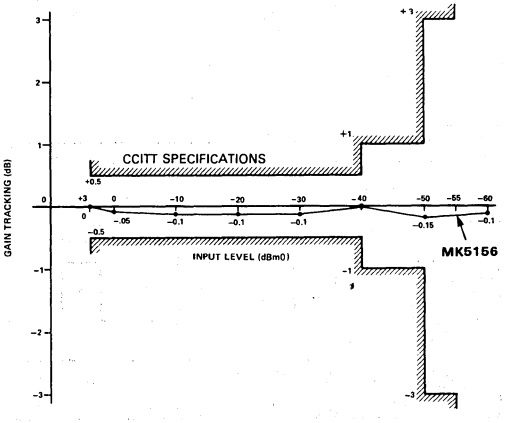


NOTE: All rise and fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

MK5156 S/D RATIO VS. INPUT LEVEL
Figure 14



M5156 GAIN TRACKING PERFORMANCE
Figure 15



PRODUCT PROFILE

MOSTEK®

TELECOMMUNICATION PRODUCTS

Companding CODEC with Filters

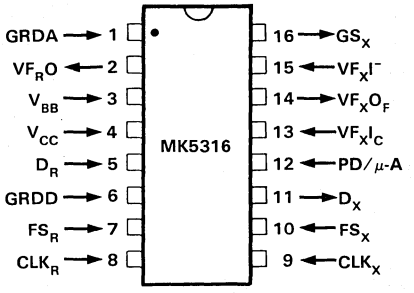
MK5316(J)

FEATURES

- ☐ Per-channel, single-chip CODEC with filters
- ☐ AT&T D3/D4 and CCITT compatible
- ☐ Pin-programmable μ-law/A-law/power-down
- ☐ On-chip stable voltage reference
- ☐ ±5 volt power supplies, ± 5%
- ☐ Low power dissipation
  - 40 mW operating (typ)
  - 100 μW standby (typ)
- ☐ TTL/CMOS-compatible digital inputs and outputs
- ☐ Gain adjust available at the transmit and receive filter stages
- ☐ Synchronous or asynchronous operation
- ☐ Serial data rate from 64 kb/s to 4.096 Mb/s
- ☐ Separate internal analog and digital grounds reduce system noise problems
- ☐ Single 16-pin package
- ☐ Minimal external component count

PIN CONNECTIONS

Figure 1



DESCRIPTION

The MK5316 is a monolithic device containing a companding CODEC and PCM filters on a single chip. This device has been designed to meet the needs of the telecommunications industry for per-channel, voice-frequency CODECs and PCM filters. Both the transmit and receive sections have been incorporated into a single package with negligible loss of crosstalk immunity. Typical device applications are PBX systems, central offices, channel banks, and other telephone digital switching and transmission systems.

The MK5316 transmit section is composed of an input amplifier, a band-pass filter, and a compressing A/D converter. The operational amplifier's output is available for use in an inverting gain configuration at the transmit stage. By disabling the amplifier, this output can be used as a noninverting high-impedance input to the band-pass filter. The band-pass, switched-capacitor filter provides rejection of the 50-60 Hz power line frequency and the band-limiting required for an 8 kHz sampling system. The A/D converter transforms the band-limited, voice-frequency signals into 8-bit words using one of two selectable companding laws. The encoded data is transmitted in a serial format under the control of the transmit clock and transmit synchronization inputs.

The receive section of the MK5316 is composed of an expanding D/A converter and a low-pass filter. The D/A converter receives 8-bit words in a serial format under control of the receive clock and receive synchronization inputs. The low-pass, switched-capacitor filter smooths the voltage steps of the D/A converter and provides compensation for the sinx/x decoder response. The receive filter output may then be adjusted to system levels by use of a voltage divider network.

The MK5316 also features a stable on-chip voltage reference. This reference provides excellent gain stability over a wide temperature range and under various supply voltage conditions.

INTRODUCTION

A general trend towards the conversion of voice signals to digital information is currently occurring. TDM PCM is the most popular form of digital transmission.

Today there are several important applications for this TDM scheme:

1. A high speed digital data link between central offices to pass many conversations over one pair of wires.
2. The electronic connection of two different circuit paths.
3. Concentrators

Traditionally this connection had been done by electromechanical crossreed switches. Very low "on" resistance, low crosstalk, and immunity from the large ringing or transient voltages were required. Since the electromechanical technique was deemed to be of lower reliability, an all electronic approach was desired. Electronic cross point switches were designed and built, but because the electrical requirements mentioned above are extremely difficult to meet, the results were not entirely satisfying.

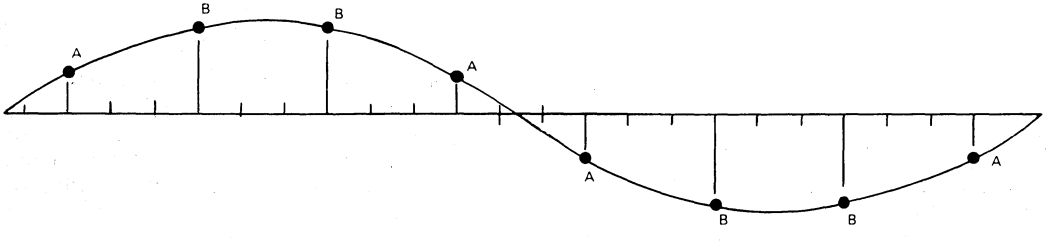
The digital approach obviates the analog switch problem by first performing an A to D conversion, then assigning a time slot for each voice channel. For the D3 channel bank, 24 channels of digital data of 8 bits per word are transmitted in a serial bit stream at 1.544 Mbits/sec. Each voice channel is sampled at an 8kHz rate so this signal must be bandlimited to less than 4kHz in order to prevent undesirable aliasing.

Figure 1 shows how a 1kHz input signal is sampled every 125 μsec. At each of these sampling times, the analog information is converted into an eight-bit digital word that is later sent out in serial format at the 1.544 Mbits/sec rate.

Figure 2 shows how the 24 voice channels are time division multiplexed onto one wire (for simplicity only simplex operation is shown).

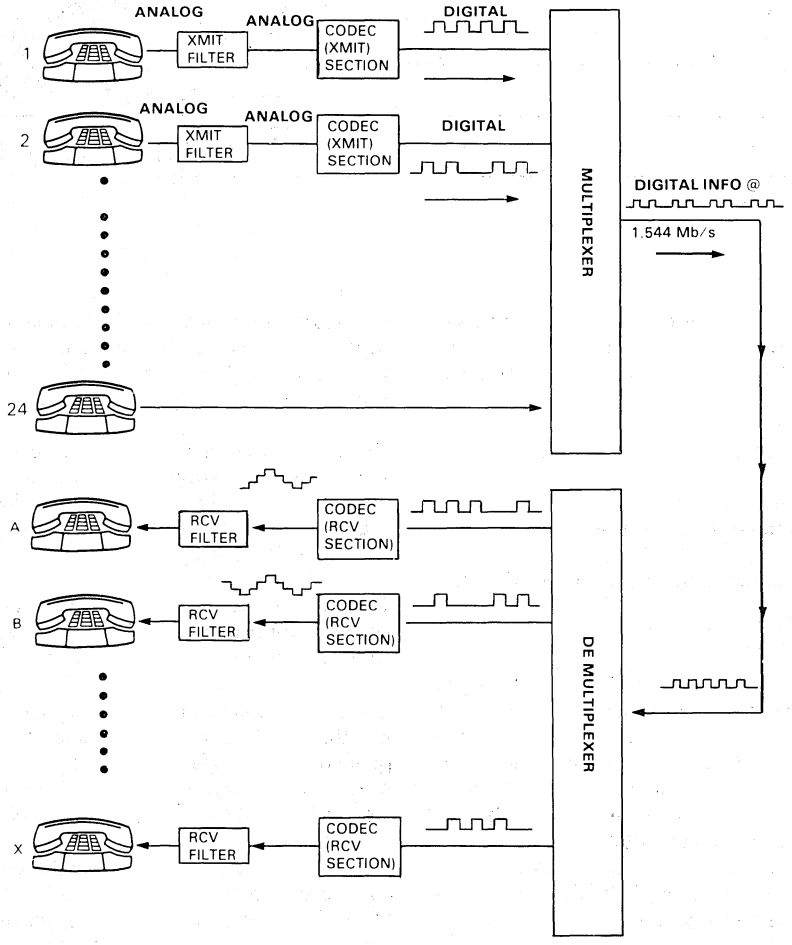
Channel 1 analog information is first bandlimited to less than 4kHz, then sampled and converted to a companded digital code. This 8 bit word is serially transmitted to a multiplexer where digital information from all the other channels are assimalated. The final bit stream of 1.544mbit/sec is sent to the demultiplexer where the appropriate alphanumeric channel is connected to numeric channel. This control (selection) is done by the main computer or processor. One may see that any numeric channel could be connected to any alphanumeric channel by means of a different time slot assignment. This completes the switching in a completely digital manner.

8kHz SAMPLING SYSTEM
Figure 1



24 CHANNEL MULTIPLEXING

Figure 2



For T1 carrier systems, the digital PCM information might be transmitted between central offices. For PBX applications, the PCM technique is used to allow the switching to be done digitally. The accuracy of the subsequent D-A conversion preserves the voice quality so that insertion loss is not a problem.

We selected the metal gate CMOS process for several reasons. First it is extremely low power, which is of great concern. Secondly, it allows for high-quality, matched capacitors in a minimum of chip size. Critical analog circuit design is done well in CMOS: for example, high gain amplifiers and comparators. Also, the metal gate CMOS process is one that is well proven in high volume production.

By using the CMOS process, only two supplies are necessary, plus and minus five volts. To minimize power, all the digital logic is run from the plus 5V supply to ground, and only the analog section operates from ± 5 volts.

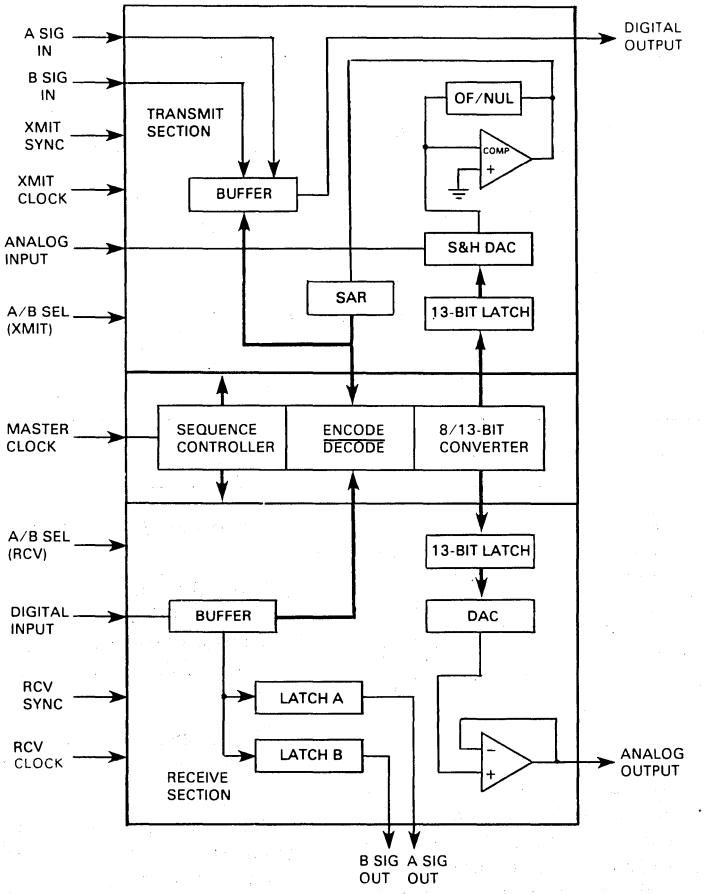
CHIP ARCHITECTURE

Figure 3 shows the block diagram representation of the CODEC chip. The important features of the scheme used are listed below:

1. Two independent DAC's for encode and decode functions provide system isolation not achievable using shared DAC approach. The capacitive two DAC approach also eliminates external sample/hold capacitors as well as an external filter for offset which is required in the shared DAC approach. This minimizes the external components required.
2. Complete signalling compatibility with D3 channel bank requirements.
3. Since the companding law is implemented using 8 to 13 bit converter, the DAC is a linear DAC thus minimizing the number of analog components to only the minimum required for system implementation, namely two: one comparator and only one op-amp on the entire chip. Minimizing the linear

CODEC BLOCK DIAGRAM

Figure 3



components helps reduce system operating power which was the overriding consideration in chip design. Using the CMOS process, the digital portions dissipate power only during transitions. The linear sections consume power continuously.

4. The digital companding section allows easy conversion from mu-law to A-law. The CODEC allows data input/output rates from 64kHz to 2.1MHz.
5. Asynchronous or synchronous operation.

MODES OF OPERATION

The XMIT and Receive function are completely independent of each other and of the master clock. Thus the chip can operate in synchronous/asynchronous mode at various input/output clock rates. The chip timing diagram is shown in Figure 4 and the Receive and XMIT modes of operation are described in detail below:

(a) Receive Mode of Operation

In the receive mode of operation, the serial input data is shifted into the input buffer at the receive clock rate during the period receive sync. is high. The encode process is halted after the falling edge of receive sync pulse) for about 5 to 7μs, and the translated data from 8 to 13 bit converter is latched into the 13 bit receive latch which updates the output of the receive DAC with 100% duty cycle. The receive DAC acts as a sample and hold and is buffered by the unity gain op amp to the output.

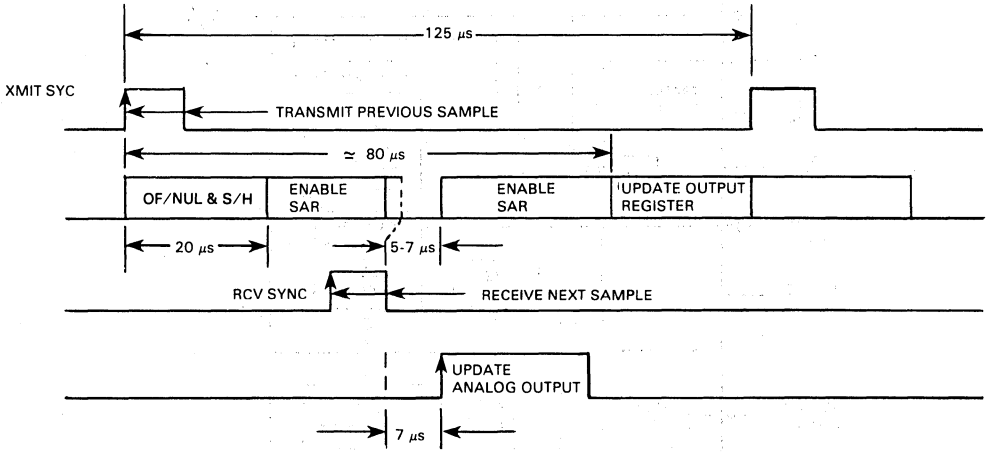
During the signalling frame a 7 bit decode is performed and the 8th data bit is latched into the SigA/SigB output latch as selected by the A/B Select (RCV) input. When the eight bit of a word is a signalling bit, it is assigned the value of ½ step. This results in a lower S/D ratio than if it were arbitrarily set to either a one or zero.

(b) Transmit Mode of Operation:

In this mode of operation the analog signal is sampled in the input sample/hold which performs the offset-null function simultaneously as described in the circuit operation section. Following the hold mode, the encoding process is completed using successive approximation technique. The operation of the XMIT DAC is similar to the operation of the receive DAC as described earlier. After the encode

A/D AND D/A CONVERSION TIMING

Figure 4



process is completed, the output of the SAR is loaded into the output buffer. The data is transmitted serially at the output clock rate during the period the XMIT SYNC is high. During the signalling frame, signalling information (SigA/SigB) is inserted into the output bit stream in place of the 8th data bit as selected by the A/B select (SMIT) input.

CIRCUIT DESCRIPTION

The system timing is controlled by the sequence controller which operates at master clock rate of 1.5 - 2.1 MHz. All necessary signals, e.g. and S&H, SAR clock Encode/Decode control, etc; are generated in this section. To insure proper encode operation, decode interrupt is allowed only when the internal SAR clock is low thus resulting in a variable (5-7μs) decode interrupt interval.

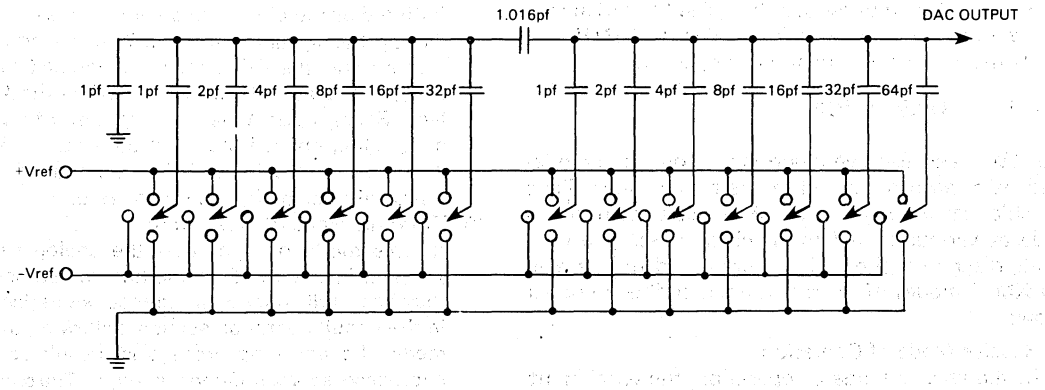
The 8 to 13 bit converter gives a one-to-one translation between 8 bit companded code at its input to a 13 bit linear code at its output thus allowing the use of a linear DAC in the digital-to-analog conversion process.

The 13-bit linear DAC operates on the charge distribution principal of a binary weighted capacitor ladder.

As shown in Figure 5, the capacitor ladder has two sections of 7 bits (7 most significant bits) and 6 bits (6 least significant bits) connected by a 64:1 capacitor divider. The equivalent circuit of the two sections can be drawn as shown in Figure 6.

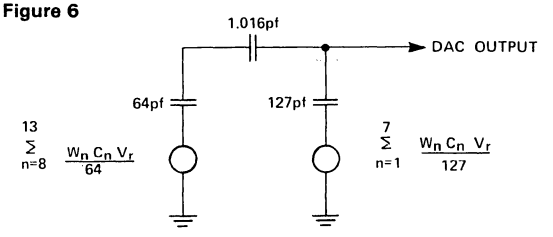
CAPACITOR LADDER

Figure 5



CAPACITOR LADDER EQUIVALENT CIRCUIT

Figure 6



WHERE W_n = 0 or 1 for the n th bit.
C_n = n th bit capacitor.
V_r = Reference Voltage ($+V_{ref}$ or $-V_{ref}$)

The output of the DAC can be written as:

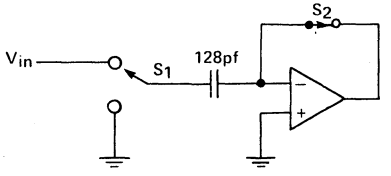
$$V_{DAC} = \frac{V_r}{128}\left[\sum_{n=1}^{7} W_n C_n + \sum_{n=8}^{13} W_n (C_n/64)\right]$$

which is equivalent to the output of a 13 bit DAC with an equivalent output capacitance of 128pF.

In the encode section this equivalent capacitor of 128pF is also employed to perform the additional function of offset-null and sample-hold as shown in Figure 7.

OFFSET NULL/SAMPLE HOLD

Figure 7



Initially S_1 is connected to V_{in} and S_2 is closed. The op. amp. is operating as a unity gain follower and its offset voltage (V_{off}), along with the analog input voltage, is stored on the capacitor.

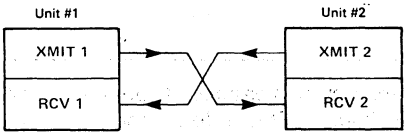
Then switch S_2 is opened and S_1 is switched to analog ground. The voltage at the inverting input of the op-amp is now V_{off}-V_{in}. Thus when the amplifier operates with S_2 open it acts as a comparator with effectively zero offset and $-V_{in}$ applied on its inverting input. The other end of the capacitor can now be operated as a DAC. Thus the capacitor ladder performs all the necessary functions of offset-null sample-hold as well as a DAC in the encode section of the chip.

EXPERIMENTAL RESULTS

The set up of Figure 8 was used to evaluate the chip performance.

CHIP PERFORMANCE

Figure 8

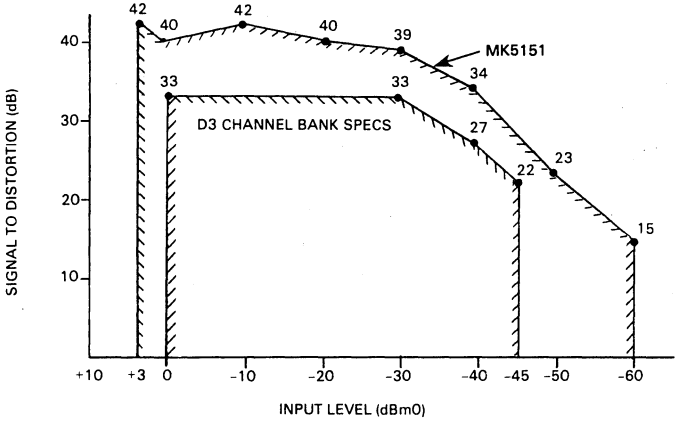


The MK5151 CODEC performance exceeds the AT&T D3 channel bank specifications. Figure 9 shows the signal-to-quantizing distortion as a function of input level.

Idle channel noise of 13-14dBrnC0 is better than the D3 spec by 9-10dB. Gain tracking is shown in Figure 10.

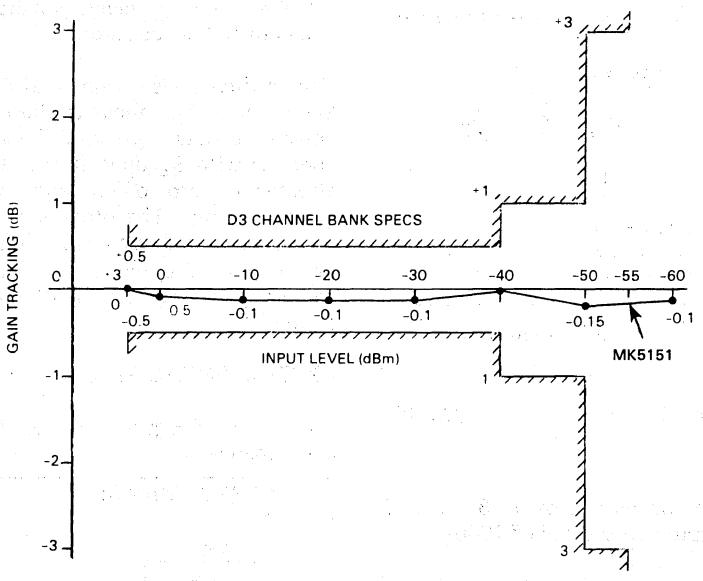
SIGNAL-TO-NOISE RATIO

Figure 9



GAIN TRACKING

Figure 10



Operating power measured at room temperature typically is 30mW. This is low enough that a stand-by mode is not deemed necessary. The European A-law version of the CODEC is also available and is simply a metal mask variation of this product. Chip size is 170 x 184 mils.

1982 TELECOMMUNICATION PRODUCTS DATA BOOK

PRELIMINARY

MOSTEK®

TELECOMMUNICATION PRODUCTS

PCM Transmit/Receive Filters

MK5912(J)-3

FEATURES

- ☐ Monolithic device includes both transmit and receive filters
- ☐ Transmit filter includes 50/60Hz rejection
- ☐ Receive filter includes sin x/x compensation
- ☐ External gain adjustment, both transmit and receive filters
- ☐ Low power consumption:
  - 35 mW typical without power amplifiers
  - <1 mW typical in power-down mode
- ☐ Direct interface with transformer or electronic telephone hybrids
- ☐ ± 5% power supplies; +5 V, -5 V
- ☐ Standard 16-pin package
- ☐ Industry standard pin connections

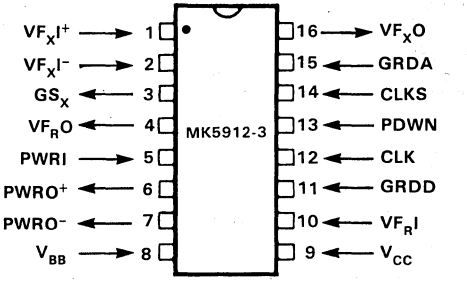
DESCRIPTION

The MK5912-3 is a monolithic device containing the two filters required for use in telephone digital switching and transmission systems. The device has been designed to minimize power dissipation, maximize reliability and provide a low-cost alternative to hybrid filters. A block diagram is shown in Figure 3, with the pin connections in Figure 1. The device consists of two switched-capacitor filters, transmit and receive, and power amplifiers which may be used to drive a transformer hybrid (2-to-4 wire converter) or an electronic hybrid (SLIC). If an electronic hybrid is used, the power amplifiers are not needed and may be deactivated to minimize power dissipation. The transmit filter is a band-pass filter which will pass frequencies between 300 Hz and 3200 Hz and provides rejection of the 50/60 Hz power line frequency as well as the antialiasing needed in an 8 kHz sampling system. The receive filter is a low-pass filter which smooths the voltage steps present in the CODEC output waveform and provides the sin x/x correction necessary to give unity gain in the passband for the CODEC-decoder-and-receive-filter pair. A typical line termination is shown in Figure 2.

The MK5912-3 is designed to be used with the Mostek family of CODECS (MK5116, MK5156, and MK5151).

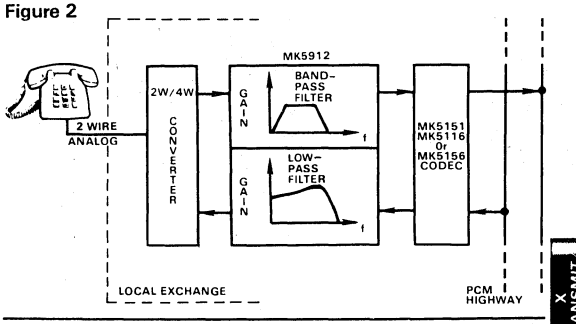
PIN CONNECTIONS

Figure 1



TYPICAL LINE TERMINATION

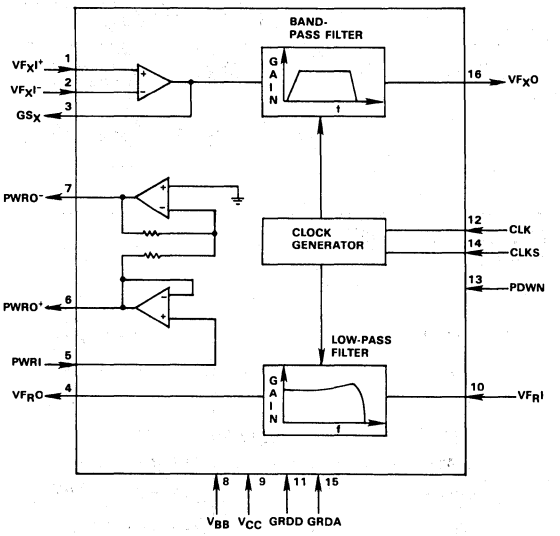
Figure 2



X TRANSMIT/RECEIVE FILTER

MK5912-3 BLOCK DIAGRAM

Figure 3



FUNCTIONAL DESCRIPTION

VF_XI^+, Pin 1

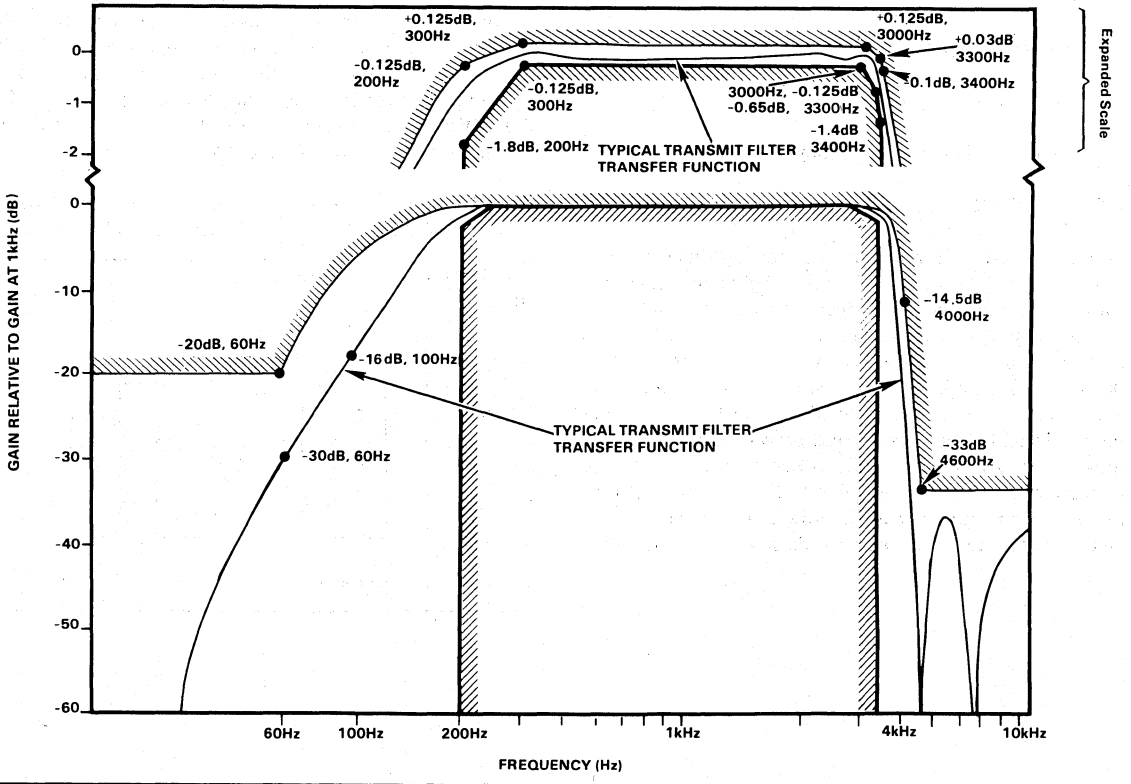
Pin 1 is the non-inverting input of the gain adjustment op amp in the transmit filter section. The signal applied to this pin typically comes from the transmit leg of a 2-to-4 wire hybrid. This input may be ac or dc coupled. This signal passes through the op amp to the transmit (band-pass) switched-capacitor, filter which will pass frequencies between 300 and 3200 Hz, will provide rejection of the 50/60 Hz power line frequency and will provide antialiasing for an 8 kHz sampling system. The transmit filter transfer characteristics and specifications are shown in Figure 4.

VF_XI^-, Pin 2

Pin 2 is the inverting input of the gain adjustment op amp on the transmit filter. A return path for the op amp output is provided by GS_X, Pin 3. Pins 2 and 3 may be used to provide gain up to 20 dB without degrading the noise performance of the filters.

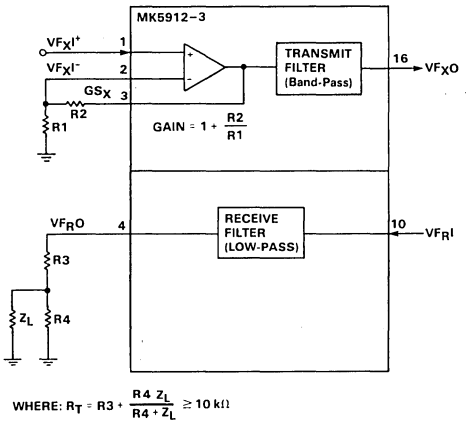
TRANSMIT FILTER TRANSFER CHARACTERISTICS

Figure 4



TRANSMIT AND RECEIVE GAIN ADJUSTMENT

Figure 5



This op amp has a common mode range of ± 1.77 V, low dc offset (2.5 mV typ.) and can provide a voltage gain greater than 2000. The unity gain bandwidth is approximately 2 MHz. The transmit filter, excluding the input op amp, provides a gain of +3 dB in the passband.

GS_X, Pin 3

Pin 3 is connected to the output of the gain-adjustment op amp in the transmit filter section. For proper operation, the load impedance connected to the GS_X output should be greater than 10 kΩ in parallel with 20 pF (Refer to Figure 5).

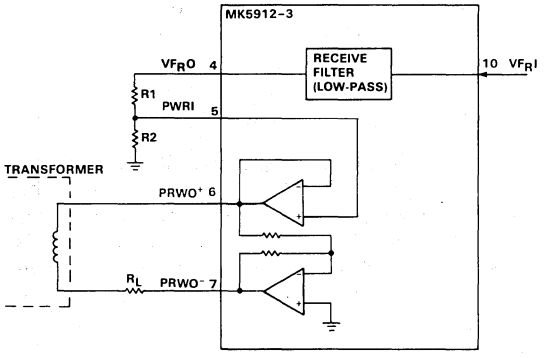
VF_RO, Pin 4

Pin 4 is the output of the receive (low-pass) filter and is capable of driving high impedance electronic hybrids. The gain of the receive signal may be attenuated by using a resistor divider as shown in Figure 5. The resistive load connected to VF_RO should be greater than 10 kΩ. The maximum output voltage range is ±2.5 V and the output offset is less than 200 mV.

If the receive filter is to drive a transformer hybrid, VF_RO should be connected to PWRI (Pin 5) as shown in Figure 6.

TYPICAL CONNECTION OF THE OUTPUT POWER AMPLIFIER STAGE

Figure 6



WHERE: R1, R2 = GAIN SETTING RESISTORS
R_L = SERIES LOAD RESISTOR

PWRI, Pin 5

Pin 5 provides the input to the power driver amplifiers which interface the receive filter to a transformer hybrid. PWRI is a high impedance input which can be driven by VF_RO directly. The input voltage range is ± 2.5 V and the gain for a bridged output is 6 dB. The power amplifiers may be deactivated when not being utilized by tying PWRI to V_{BB}.

$PWRO^+$ and $PWRO^-$, Pins 6 and 7

This balanced differential-output amplifier stage is provided to drive low impedance loads directly. The gain of the receive signal may be adjusted by a voltage divider as shown in Figure 6. The series impedance of a load resistor and the hybrid transformer should present an ac load impedance of 600 Ω (min.) to the amplifiers in a bridged configuration. With a 600 Ω load between pins 6 and 7, the maximum voltage swing across the load is ± 5.0 volts. These amplifiers may also be used to drive loads which are connected to ground.

Power consumption is cut significantly by tying PWRI to V_{BB} which deactivates the power amplifiers.

V_{BB}, Pin 8

Pin 8 is the negative supply pin. The voltage supplied to this pin should be -5 V ± 5%.

V_{CC}, Pin 9

Pin 9 is the positive supply pin. The voltage supplied to this pin should be +5 V ± 5%.

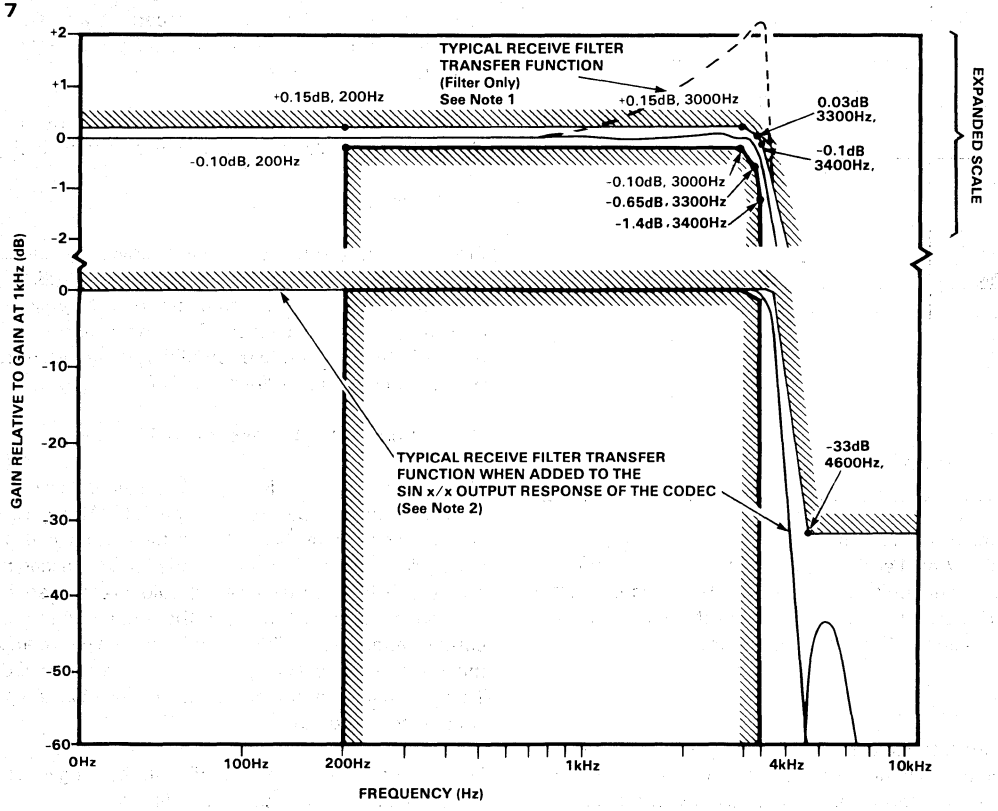
VF_RI, Pin 10

Pin 10 is the analog input to the receive filter. The receive signal is typically generated by the decoder section of a μ or A-law companding CODEC. The receive filter is a low-pass switched-capacitor filter which will pass frequencies up to 3200 Hz and provides the sin x/x correction needed to give the CODEC decoder and receive filter pair unity gain over the passband.

The receive filter transfer characteristics and specifications, including the sin x/x response introduced by the decoder, are shown in Figure 7.

RECEIVE FILTER TRANSFER CHARACTERISTICS

Figure 7



NOTES

1. The broken line shows the x/sinx response of the filter only. This response corrects the sin x/x response of the sample and hold output of the CODEC and provides unity gain in the passband.
2. The typical filter transfer function shown is the combined response of the CODEC and the receive filter. The combined response meets the stated specifications.

GRDD, Pin 11

Pin 11 serves as the digital ground return for the internal clock. The digital ground is not internally connected to the analog ground. The digital and analog grounds should be tied together as close as practical to the system supply ground.

INPUT CLOCK SELECT

Table 1

CODEC Clock	Clock Bits/ Frame	MK5912-3 CLK Input Pin 12	MK5912-3 CLKS Input Pin 14
1.536 MHz	192	1.536 MHz	V_{BB}, -5 V
1.544 MHz	192	*	V_{BB}, -5 V
2.048 MHz	256	2.048 MHz	V_{CC}, +5 V
2.560 MHz	320	2.560 MHz	Open Circuit

*The MK5912-3 can be used with a 1.544 MHz clock in the mode shown above. This is accomplished by externally suppressing every 193rd bit from the incoming train of 1.544 MHz clock bits.

CLK, Pin 12

The digital clock signal should be supplied to Pin 12. Four clock frequencies (1.536 MHz, 1.544 MHz, 2.048 MHz, or 2.560 MHz) may be used. The desired clock frequency is selected by the CLKS input (Refer to Table 1). For proper operation this clock should be tied to the receive clock of the CODEC.

PDWN, Pin 13

This control input is used to place the MK5912-3 in the standby power-down mode. Power down occurs when the signal on this input is pulled high. Standard TTL levels may be used. An internal pull up to the positive supply is provided. A settling time of 15 ms (typ.) should be allowed after power is restored.

CLKS, Pin 14

The voltage level on this pin will select the desired clock frequency to drive Pin 12. Table 1 defines the clock

selection. When using the open circuit (2.560 MHz clock frequency) mode, the capacitance to adjacent signal lines should be minimized.

GRDA, Pin 15

Pin 15 serves as the ground return for the analog circuits of the transmit and receive sections. The analog ground is not internally connected to the digital ground. The digital and analog ground should be tied together as close as practical to the system supply ground.

VF_XO, Pin 16

Pin 16 is the analog output of the transmit filter. The output voltage range is ± 2.5 volts and the dc offset is less than 250 mV. This output should be ac coupled to the transmit (encoder) section of the CODEC.

DECOUPLING RECOMMENDATIONS

PC board decoupling should be sufficient to prevent power supply transients (including turn on and turn off) from exceeding the absolute maximum rating of the device. A minimum of 1 μF is recommended for each power supply.

A 0.05 μF bypassing capacitor should also be connected from each power supply to GRDA at the MK5912-3 device. However, this decoupling may be reduced depending on board design and performance.

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias ..... -10°C to +80°C
Storage Temperature ..... -65°C to +125°C
Supply Voltage with Respect to V_{BB} ..... -0.3 V to +12.0 V
All Input and Output Voltages with Respect to V_{BB} ..... -0.3 V to +12.0 V
All Output Currents ..... ± 50 mA
Package Dissipation at 25°C (Derated 9 mW/°C when soldered into PCB) ..... 500 mW

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC AND OPERATING CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = +5 V ± 5%, V_{BB} = -5 V ± 5%, GRDA = 0 V, GRDD = 0 V, unless otherwise specified.

DIGITAL INTERFACE

SYM	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
I_{LIC}	Input Load Current			10	µA	V_{IN} = V_{IL} min to V_{IH} max
I_{LIO}	Input Load Current, CLKS			50	µA	V_{IN} = V_{BB} to V_{IH} max
I_{LIP}	Input Load Current, PDWN			-40	µA	V_{IN} = V_{IL} min to V_{IH} max
V_{IL}	Input Low Voltage (except CLKS)	-0.3		0.8	V	
V_{IH}	Input High Voltage (except CLKS)	2.2		V_{CC}+ 0.25	V	
V_{ILO}	Input Low Voltage, CLKS	V_{BB}		V_{BB}+ 0.5	V	
V_{IHO}	Input High Voltage, CLKS	V_{CC}-0.5		V_{CC}	V	

POWER DISSIPATION

Analog inputs = 0 V, outputs unloaded, unless otherwise specified.

SYM	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{CC0}	V_{CC} Standby Current			100	μA	PDWN = V_{IH} min
I_{BB0}	V_{BB} Standby Current			100	μA	PDWN = V_{IH} min
I_{CC1}	V_{CC} Operating Current, Power Amplifiers Inactive		3.5		mA	PWRI = V_{BB}
I_{BB1}	V_{BB} Operating Current, Power Amplifiers Inactive		3.5		mA	PWRI = V_{BB}
I_{CC2}	V_{CC} Operating Current		6		mA	
I_{BB2}	V_{BB} Operating Current		6		mA	

DC AND OPERATING CHARACTERISITCS

T_A = 0°C to +70°C, V_{CC} = +5 V ± 5%, V_{BB} = -5 V ± 5%, GRDA = 0 V, GRDD = 0 V, unless otherwise specified.

ANALOG INTERFACE, TRANSMIT FILTER GAIN SETTING AMPLIFIER

SYM	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
I_{BXI}	Input Leakage Current, VF_XI^+, VF_XI^-			200	nA	$-1.7\ V < V_{IN} < 1.7\ V$
R_{IXI}	Input Resistance, VF_XI^+, VF_XI^-	8			MΩ	
V_{OSXI}	Input Offset Voltage, VF_XI^+, VF_XI^-			25	mV	$-1.7\ V < V_{IN} < 1.7\ V$
$CMRR_1$	Common Mode Rejection, VF_XI^+, VF_XI-	45			dB	Input at VF_XI^+; VF_XI^- tied to GS_X ($-1.25\ V < V_{IN} < 1.25\ V$) or 0dBm0=0.88 V_{RMS}
$CMRR_2$	Common Mode Rejection, VF_XI^+, VF_XI^-	40			dB	$-1.7\ V < V_{IN} < 1.7\ V$
A_{VOL}	DC Open Loop Voltage Gain, GS_X		2000			
f_C	Open Loop Unity Gain Bandwidth, GS_X		2		MHz	
V_{OXI}	Output Voltage Swing, GS_X	±1.77			V	$R_L \geq 10\ k\Omega$
C_{LXI}	Load Capacitance, GS_X			20	pF	
R_{LXI}	Minimum Load Resistance, GS_X	10			kΩ	Minimum R_L

ANALOG INTERFACE, TRANSMIT FILTER

SYM	PARAMETER		MIN	TYP	MAX	UNIT	TEST CONDITIONS
R_{OX}	Output Resistance, VF_XO				100	Ω	
V_{OSX}	Output DC Offset, VF_XO				250	mV	VF_XI^+ Connected to GRDA, Input Op Amp at Unity Gain
$PSRR_1$	Power Supply Rejection of V_{CC} at VF_XO	1 kHz 3 kHz 20 kHz	30 18 30	35 25 45		dB	Input Op Amp at Unity Gain. V_{BB}=-5 V; V_{CC}=+5 V with 70 mV_{RMS} injected

ANALOG INTERFACE, TRANSMIT FILTER (Cont'd)

SYM	PARAMETER		MIN	TYP	MAX	UNIT	TEST CONDITIONS
$PSRR_2$	Power Supply Rejection of V_{BB} at VF_XO	1 kHz 3 kHz 20 kHz	25 14 20	30 18 30		dB	Input Op Amp at Unity Gain. V_{CC}=+5 V; V_{BB}=-5 V with 70 mV_{RMS} injected
C_{LX}	Load Capacitance, VF_XO				20	pF	
R_{LX}	Minimum Load Resistance, VF_XO		3			kΩ	Minimum R_L
V_{OX}	Output Voltage Swing, 1 kHz, VF_X		± 2.5			V	$R_L \geq 3k\Omega$

ANALOG INTERFACE, RECEIVE FILTER

SYM	PARAMETER		MIN	TYP	MAX	UNIT	TEST CONDITIONS
I_{BR}	Input Leakage Current, VF_RI				2.5	μA	$-2.5\ V < V_{IN} < 2.5\ V$
R_{IR}	Input Resistance, VF_RI		1			MΩ	
R_{OR}	Output Resistance, VF_RO				100	Ω	
V_{OSR}	Output DC Offset, VF_RO				200	mV	VF_RI Connected to GRDA
$PSRR_3$	Power Supply Rejection of V_{CC} at VF_RO	1 kHz 3 kHz 20 kHz	30 20 30	35 30 45		dB	V_{BB}=-5 V; V_{CC}=+5 V with 70 mV_{RMS} injected
$PSRR_4$	Power Supply Rejection of V_{BB} at VF_RO	1 kHz 3 kHz 20 kHz	30 13 25	35 18 30		dB	V_{CC}=+5 V; V_{BB}=-5V with 70 mV_{RMS} injected
C_{LR}	Load Capacitance, VF_RO				20	pF	
R_{LR}	Minimum Load Resistance, VF_RO		10			kΩ	Minimum R_L
V_{OR}	Output Voltage Swing, VF_RO		± 2.5			V	R_L = 10 kΩ

DC AND OPERATING CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = +5 V ± 5%, V_{BB} = –5 V ± 5%, GRDA = 0 V, GRDD = 0 V, unless otherwise specified.

ANALOG INTERFACE, RECEIVE FILTER DRIVER AMPLIFIER STAGE

SYM	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
I_{BRA}	Input Leakage Current, PWRI			200	nA	$-2.5\ V < V_{IN} < 2.5\ V$
R_{IRA}	Input Resistance, PWRI	1			MΩ	
R_{ORA}	Output Resistance, $PWRO^+$, $PWRO^-$		4		Ω	$\lvert I_{OUT} \rvert < 10$ mA $-2.5\ V < V_{OUT} < 2.5\ V$
V_{OSRA}	Output DC offset, $PWRO^+$, $PWRO^-$			50	mV	PWRI Connected to GRDA
C_{LRA}	Load Capacitance, $PWRO^+$, $PWRO^-$			100	pF	

ANALOG INTERFACE, RECEIVE FILTER DRIVER AMPLIFIER STAGE (Cont'd)

SYM	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
V_{ORA1}	Output Voltage Swing Across R_L, $PWRO^+$, $PWRO^-$ Single Ended Connection; R_L Connected to GRDA	± 2.5			V	R_L = 300 Ω
V_{ORA2}	Differential Output Voltage Swing Across R_L. $PWRO^+$, $PWRO^-$ Balanced Output Connection; R_L Connected Between PWRO+ and $PWRO^-$	± 5.0			V	R_L = 600 Ω

AC CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = +5 V ± 5%, V_{BB} = -5 V ± 5%, GRDA = 0 V, GRDD = 0 V, unless otherwise specified.
Clock Input Frequency: CLK = 1.536 MHz ± 0.1%, CLKS = V_{ILO} (Tied to V_{BB})
CLK = 2.048 MHz ± 0.1%, CLKS = V_{IHO} (Tied to V_{CC})
CLK = 2.560 MHz ± 0.1%, CLKS = Open Circuit

TRANSMIT FILTER TRANSFER CHARACTERISTICS

SYM	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
G_{RX}	Gain Relative to Gain at 1 kHz					0 dBmO Input Signal
	Below 50 Hz			-28	dB	Gain Setting Op Amp at
	50 Hz	-35	-29.5	-28	dB	Unity Gain
	60 Hz	-30		-26	dB	
	200 Hz	-1.8		-.125	dB	0 dBmO Signal=.88 V_{RMS},
	300 Hz to 3000 Hz	-0.125		+0.125	dB	Input at VF_XI^+
	3300 Hz	-0.65		0.03	dB	
	3400 Hz	-1.4		-0.1	dB	Output at VF_XO
	4000 Hz			-14.5	dB	is = 1.25 V_{RMS}
	4600 Hz and Above			-33	dB	
G_{AX}	Absolute Passband Gain at 1 kHz, VF_XO	2.85	3.0	3.15	dB	Gain Setting Op Amp at Unity Gain; 25°C
G_{AXT}	Gain Variation with Temperature at 1 kHz		.0005		dB/°C	0 dBmO Signal Level
G_{AXS}	Gain Variation with Supplies at 1 kHz		0.05		dB/V	0 dBmO Signal Level, Supplies ± 5%
CT_{RT}	Cross Talk, Receive to Transmit, Measured at VF_XO			-60	dB	VF_RI = 1.25 V_{RMS} at 1 kHz. VF_XI^+ to GRDA. VF_XI^- to GS_X. GS_X through 10 kΩ to GRDA
N_{CX1}	Total C Message Noise at Output, VF_XO		6	12	dBrnC0	Gain Setting Op Amp at Unity Gain, TLP=+4 dB
			10	16	dBrnC	at VF_XO

TRANSMIT FILTER TRANSFER CHARACTERISTICS (Cont'd)

SYM	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
N_{CX2}	Total C Message Noise at Output, VF_XO		10 14	14 18	dBrnC0 dBrnC	Gain Setting Op Amp at 20 dB Gain, TLP=+4 dB at VF_XO
D_{DX}	Differential Envelope Delay, VF_XO 1 kHz to 2.6 kHz		40		μs	
D_{AX}	Absolute Delay at 1 kHz, VF_XO		195		μs	
DP_{X1}	Single Frequency Distortion Products			-48	dB	0 dBm Input Signal at 1 kHz
DP_{X2}	Single Frequency Distortion Products at Maximum Signal Level of +3 dBm0 at VF_XO			-45	dB	0.125 V_{RMS} 1 kHz Input Signal at VF_XI^+. Gain Setting Op Amp at 20 dB Gain. The +3 dBm0 signal at VF_XO is 1.77 V_{RMS}.

AC CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = +5 V ± 5%, V_{BB} = -5 V ± 5%, GRDA = 0 V, GRDD = 0 V, unless otherwise specified.

Clock Input Frequency: CLK = 1.536 MHz ± 0.1%, CLKS = V_{ILO} (Tied to V_{BB})
CLK = 2.048 MHz ± 0.1%, CLKS = V_{IHO} (Tied to V_{CC})
CLK = 2.560 MHz ± 0.1%, CLKS = Open Circuit

RECEIVE FILTER TRANSFER CHARACTERISTICS

SYM	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
G_{RR}	Gain Relative to Gain at 1 kHz with sin x/x correction; CODEC and filter					0 dBmO Input Signal
	Below 200 Hz			0.15	dB	0 dBmO Signal $\cong 1.25\,V_{RMS}X\left(\mathrm{Sin}\left(\frac{\pi f}{8000}\right)\Big/\left(\frac{\pi f}{8000}\right)\right)$
	200 Hz	-0.10		0.15	dB	
	300 Hz to 3000Hz	-0.10		0.15	dB	
	3300 Hz	-0.65		0.03	dB	
	3400 Hz	-1.4		-0.1	dB	Input at VF_RI
	4000 Hz			-14.5	dB	
	4600 Hz and Above			-32	dB	
G_{AR}	Absolute Passboard Gain at 1 kHz with sin x/x correction; CODEC and filter	-0.15	0	+0.15	dB	25°C
G_{ART}	Gain Variation with Temperature at 1 kHz		0.0005		dB/°C	0 dBmO Signal Level
G_{ARS}	Gain Variation with Supplies at 1 kHz		0.05		dB/V	0 dBmO Signal Level, Supplies ± 5%

RECEIVE FILTER TRANSFER CHARACTERISTICS (Cont'd)

SYM	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
CT_{TR}	Cross Talk, Transmit to Receive, Measured at VF_RO			-60	dB	VF_XI^+ = .88 V_{RMS} at 1 kHz. Gain Setting Op Amp at Unity Gain. VF_RI connected to GRDA.
N_{CR}	Total C Message Noise at Output, VF_RO		6 10	14 18	dBrnC0 dBrnC	VF_RO Output or $PWRO^+$ and $PWRO^-$; Connected with Unity Gain, TLP=+4 dB at VF_RI
D_{DR}	Differential Envelope Delay, VF_RO, 1 kHz to 2.6 kHz		120		μs	
D_{AR}	Absolute Delay at 1 kHz, VF_RO		125		μs	
DP_{R1}	Single Frequency Distortion Products			-48	dB	0dBm Input Signal at 1 kHz
DP_{R2}	Single Frequency Distortion Products at Maximum Signal Level of +3 dBmO at VF_RO			-45	dB	+3 dBmO Signal Level of 1.77 V_{RMS}, 1kHz Input at VF_RO

CODEC/Filter Demo Board

INTRODUCTION

Mostek's CODEC and filter series consists of four parts: the MK5151 and MK5116 μ-255 law companding CODECs, the MK5156 A-law companding CODEC, and the MK5912 filter which contains both transmit and receive filters. Any one of these CODECs and a MK5912 filter make up a complete interface circuit for use in a digital Central Office or PBX switching system. This interface circuit performs the necessary filtering, A/D conversions, and D/A conversions to interface the voice-frequency signals at the telephone line input to the digital bus of the switching system.

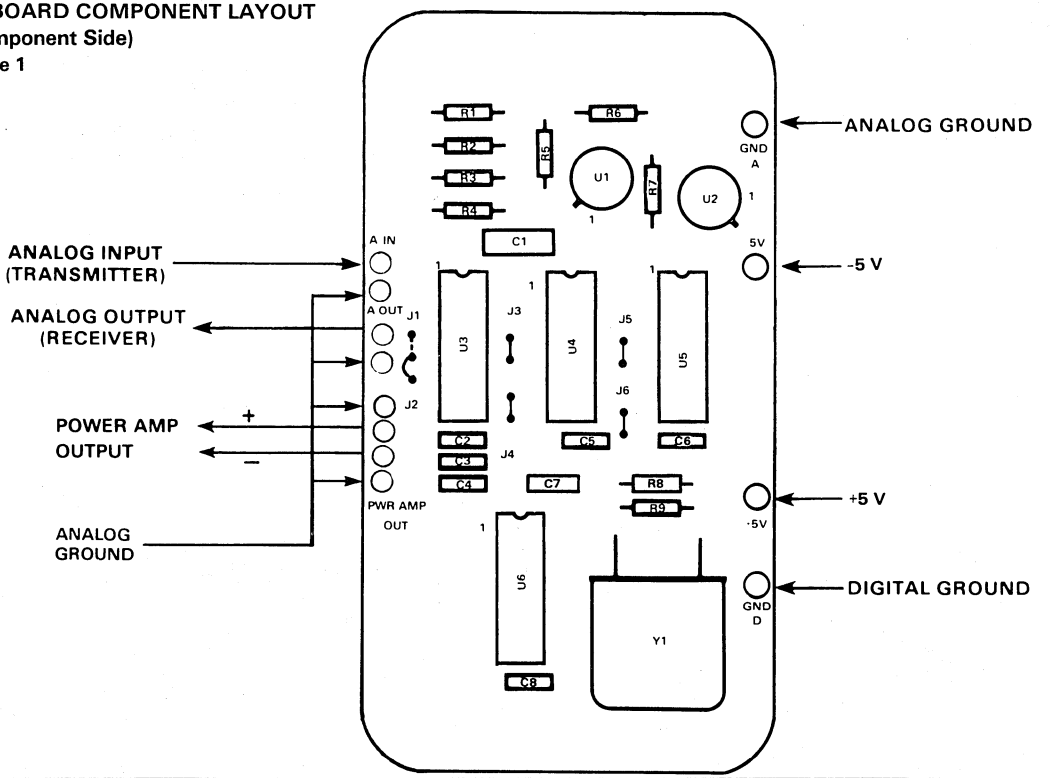
This demonstration board shows the basic operation and performance of the CODEC/filter pair. The board also shows the small number of external components that are required for a typical system.

BOARD DESCRIPTION (Refer to Figure 1)

This demonstration board uses the MK5912 filter in conjunction with the MK5116 CODEC. However, the MK5156 may be substituted for the MK5116 due to the identical pin assignments.

A 2.048 MHz crystal oscillator provides the master clock for both the MK5912 and the CODEC. A dual binary counter supplies the CODEC with the necessary transmit/receive clock and sync pulses. Although the CODEC transmit/receive clock rate may be any frequency between 64kHz and 2.1MHz, a clock rate of 128kHz is used for simplicity. Two LM 10 op amps, which have an on-chip low-voltage reference, are used to provide the ± 2.5V reference required by the CODEC. The gain of the LM 10 is set to match the +2.5V reference within 1% of the -2.5V reference. In an actual system, the clock and reference may be shared by many CODECs and filters.

PC BOARD COMPONENT LAYOUT
(Component Side)
Figure 1



There are also a few more external components required by the CODEC/filter series. One of the external components is an AC coupling capacitor, C1, which is required to block any DC offset voltage present at the transmit filter output. An external resistor, R4 is also required to provide a DC path from the analog input of the CODEC to ground. The resistance of R4 should be 3kΩ. The receive side requires similar circuitry with R8 being 50kΩ and C7 being 0.1μF. External resistors R2 and R3 may be used to adjust the gain of the transmit filter input op amp. No other external components are required except the recommended bypass capacitors which are connected to the two power supplies.

CIRCUIT OPERATION (Refer to Figure 2)

The analog input signal applied to pin 1 of the MK5912 passes through the input gain-adjustment op amp to the transmit band-pass filter, which passes frequencies between 300Hz and 3200Hz. The transmit filter of the MK5912, excluding the gain of the input op amp, has 3dB of gain in the passband. The output of the transmit filter is AC coupled to the input of the CODEC, which performs the A/D conversion. The resulting 8-bit words are shifted out of pin 8 of the CODEC by the positive transitions of the transmit clock while the transmit sync is high. With jumpers J4, J5, and J6 in place, the 8-bit words are shifted into the digital input by the positive transitions of the receive clock, which is inverted with respect to the transmit clock. The data is converted back to an analog signal by the receive section of the CODEC and is fed to the MK5912 receive filter input, pin 10. The receive filter is a low-pass filter which smooths the voltage steps of the CODEC analog output and also provides (sinx)/x correction to give the CODEC/filter pair unity gain in the passband. The output of the receive filter is capable of driving a 10kΩ load.

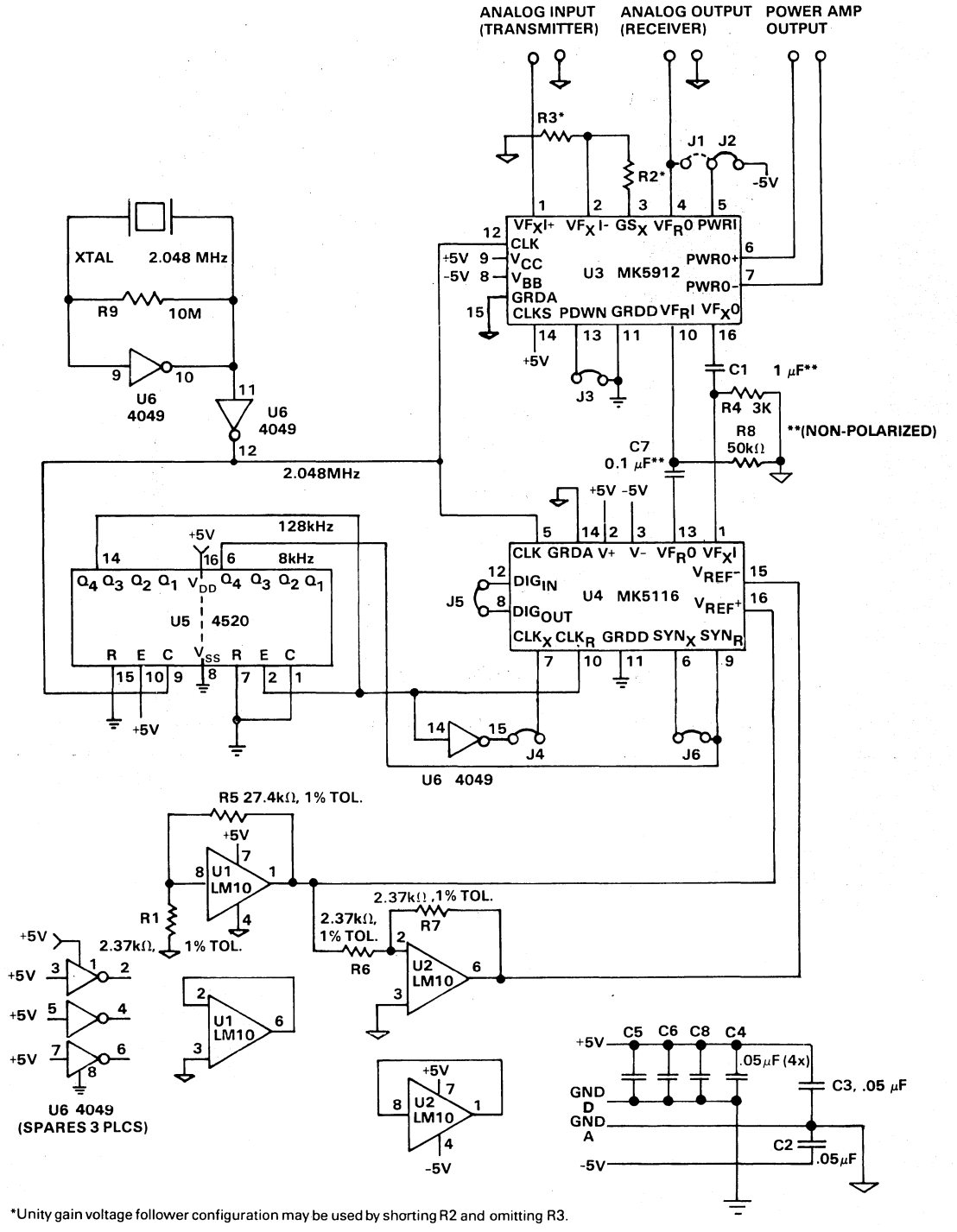
Jumper J1 can be used to connect the receive filter output to the input of the power-driver amplifiers. The differential output of the power amplifiers is capable of driving low-impedance loads such as the receive leg of a hybrid transformer. If the power amplifiers are not needed, they may be deactivated to reduce power consumption. This is accomplished by jumper J2 which connects the power amplifier input to V_{BB}. Internal logic sets the power amplifiers in the deactivated mode when the power supply is connected to the filter.

Jumper J3 controls the power-down input, pin 13, of the MK5912. When this pin is pulled high or left open circuit, the MK5912 goes into a power-down mode which reduces the power dissipation of the chip to less than 1mW.

This circuit operates on ± 5V ± 5% power supplies. The analog and digital grounds should be connected together at the power supply.

CIRCUIT DIAGRAM

Figure 2

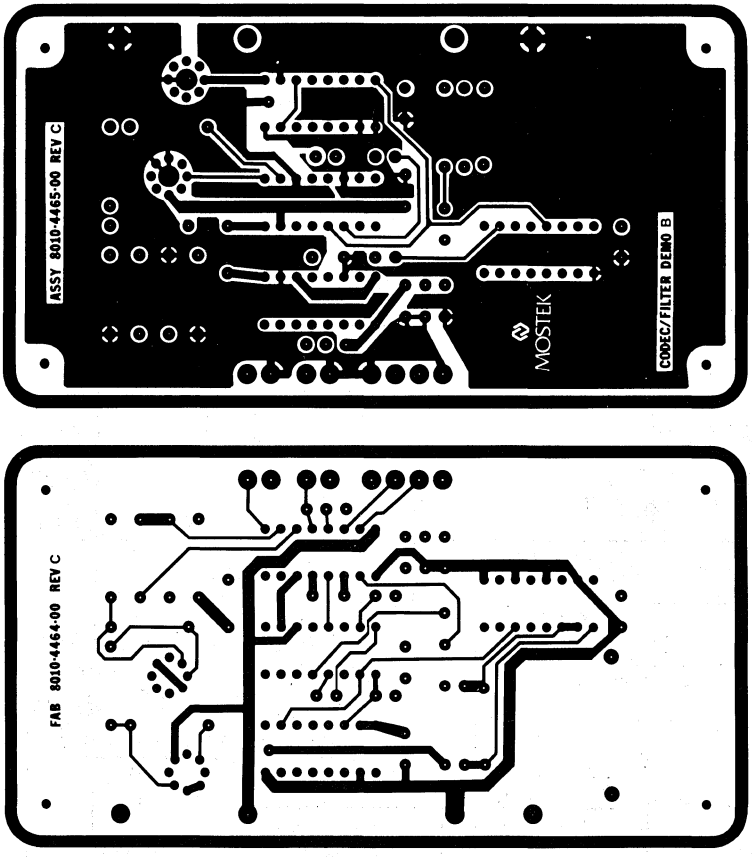


*Unity gain voltage follower configuration may be used by shorting R2 and omitting R3.

PC BOARD LAYOUT

Figure 3

COMPONENT SIDE



UNITED TECHNOLOGIES MOSTEK

Mostek Corporation, 1215 West Crosby Rd.
Carrollton, Texas 75006 USA; (214) 323-6000
In Europe, Contact: Mostek Brussels
270-272 Avenue de Tervuren (BTE21)
B-1150 Brussels, Belgium; Telephone: 762.18.80

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