MOSEL 1990 CMOS Data Book

MOSEL

MEMORIES
F O R
TOMORROW

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MOSEL CORPORATION

1990 DATA BOOK

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HOW TO USE THE DATA BOOK

This book has been organized by product families, beginning with general information on the company and products. The products begin with Static RAMs, then Specialty Memories, ROMs, Voice ROMs, and Cache Products. Within each section, data sheets are arranged in the order of densities except Specialty Memories and Cache Products. Application Notes and Package Diagrams then follow, and finally the MOSEL Sales Network.

LIFE SUPPORT POLICY

MOSEL products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of MOSEL Corporation.

1. Life support devices or systems are devices or systems which, are intended for surgical implant into the body to support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or to affect its safety or effectiveness.

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MOSEL COMPANY BACKGROUND

1

Overview

MOSEL was founded in 1983 with the mission to develop Static RAM and specialty memory products for the office automation, communications, instrumentation, and consumer products industries. The company offers a selection of standard and specialty memory products including SRAMs, ROMs, Latch RAMs, Cache Data RAMs, Video Color Palette RAMs, FIFOs, Dual Port SRAMs and Voice ROMs with additional product families scheduled for release in 1990. With product sales up 100% in 1988 and again in 1989, the company is one of the fastest growing in the semiconductor industry.

Memories For Tomorrow

At MOSEL, we hold the view that tomorrow's memories will not be simply larger, faster versions of today's products. In the future, an entire new generation of memory product architectures will be required, the **Memories For Tomorrow**.

Just as ASIC (application specific) logic products have replaced standard logic devices, application specific specialty memory products will replace standard memory products in many applications. System designers are rejecting the traditional memory architectures, which impose severe limitations on system performance and/or require use of additional external logic. These designers are crying out for a whole new generation of memory products which incorporate an increasing level of functional integration.

At MOSEL, our primary mission is to pioneer new families of specialty memory solutions that overcome these limitations and provide system designers with the memory solutions for tomorrow.

Products and Technology

MOSEL's current product offerings are divided into standard CMOS SRAMs, ROMs, and Specialty Memory Products and late in 1990, MOSEL will introduce our first DRAM products.

In the CMOS SRAM area MOSEL currently offers a family of JEDEC standard slow and high speed bytewide devices ranging in density from 16K to 256K bits and has begun sampling a 1 megabit SRAM. These standard memory products serve as the company's technology driver, and provide a solid foundation for continued growth.

In the CMOS ROM area, MOSEL offers Programmable Mask ROMs ranging in densities from 128K to 8 Mega bits. The Company also offers speech synthesizer chips or Voice ROMs in various durations. Voice ROMs have a variety of applications, including toy, office automation and automotive applications.

Specialty Memory Products currently include such products as dual-port SRAMs, high-speed FIFOs (First-In, First-Out memories), Latch RAMs, Cache Data RAMs, Video RAMDACs. Planned or under development are extensions to these product families and new families including Cache Controllers, Quad DataRAMS, Cache Tag RAMs and parity RAMs.

MOSEL has to date, successfully introduced 4 generations of CMOS memory technology (2.0, 1.5, 1.2, and 1.0 micron). Under development, the company has sub-micron CMOS and BiCMOS processes. A strong technology integration team provides highly manufacturable, low-cost production processes.

Manufacturing

MOSEL has entered into strategic alliances with several established semiconductor companies. The company has licensed proprietary process technology to these partners, and then contracted with them for manufacturing services. This strategy gives MOSEL access to nearly $1 billion in manufacturing facilities, providing high volume manufacturing capability, fast growth rates and a dependable source of supply for its customers, while allowing MOSEL to focus its initial investments on product and process development. Through the use of these strategic alliances, MOSEL has achieved its initial sales and profitability goals.

In 1990, MOSEL will break ground on its own $100,000,000 fab line which will be built in Hsin-Chu Science Industrial Park, Taiwan. This facility is scheduled for production beginning 1991. This fab line will significantly enhance the company's market position by allowing for greatly reduced process and product development cycles. It will also permit for the introduction of new product features which depend upon proprietary process enhancements. MOSEL will continue to rely on strategic partnerships to supply high volume production requirements.

QUALITY & RELIABILITY ASSURANCE POLICY

MOSEL maintains the highest standards for the integrity of its product line. Each product is subjected to the most stringent quality and reliability screening beginning with initial product design.

Product quality and reliability are achieved by implementing a "Total Consideration" philosophy from inception through production.

This "Total Consideration" philosophy consists of:

- Reliability being built into every design;
- Quality being built into every process step;
- Stringent inspection after critical process steps and the final product and;
- Careful analysis of field data to further enhance the overall quality and reliability

Product flow and test procedures correspond to MIL-STD-833 or are in accordance with standard industry practices for the manufacture and test of high quality micro circuits (see Table I).

NEW PRODUCT ACCEPTANCE

Product reliability begins with design. At MOSEL, conformance to process design rules ensures adequate circuit margins and ease of manufacture. Simulation results are carefully reviewed before the design is committed to masking.

Upon receipt of "first silicon", the design is completely characterized to insure parametric distribution during manufacturing.

Once the design is proven, MOSEL imposes a New Product Qualification Test procedure on each new product to verify the design, process and packaging procedures (see Table II).

RELIABILITY MONITOR PROGRAM

After the product is transferred to production, the Reliability Monitor Program provides for periodic testing to insure that all MOSEL products comply with established reliability levels. This program monitors specific product and process families and requires detailed failure analysis for reliability improvement and/or corrective action as indicated by the analysis results (see Table III).

VENDOR CERTIFICATION

Vendors to MOSEL take ownership of the products and services they supply. Certification begins with a Plant Survey of the quality and reliability procedures and practices. Each supplier then performs to his internal procedures and QRA program with periodic on-site reviews by MOSEL. Internal data is forwarded to MOSEL as required for review.

SUMMARY

You, the customer, are invited to review the total QRA program at MOSEL. We are happy to answer any questions you may have.

TABLE I PRODUCT SCREENING FLOWS

SCREEN	MIL-STD-883 METHOD	PLASTIC PACKAGE (1)
Internal visual	2010	0.4% AQC
Burn-in		
Pre-burn-in electrical	25°C and power supply extreme	100%
Burn-in	Per device specification	100%
Final Electrical		
Functional, switching, dynamic (AC) and	(1) at 25°C and power supply extreme	100%
static (DC) test	(2) at temperature and power supply extremes	100%
MOSEL Quality Lot Acceptance		
External visual	2009	0.65% AQL
Final electrical conformance	Per device specification	0.1% AQL

TABLE II NEW PRODUCT QUALIFICATION TEST

TEST	MIL-STD-883 METHOD	CONDITIONS	LTPD	Periodicity (Max.)
High temperature operation life test	1005	Ta=125°C, V_{CC} = 5.5V cond. D, 1000 hrs.	5	consecutive 3 lots
Steady State Life Test	1005	Ta=125°C, V_{CC} = 5.5V cond. D, 1000 hrs.	5	consecutive 3 lots
Pressure pot		121°C, 15 psi, 100% 216 hrs.	7	consecutive 3 lots
Humidity with Bias		V_{CC} = 5.5V, 85°C/85%RH, 5 Static	7	consecutive 3 lots
External visual examination	2009		15	
Physical Dimension	2016		15	
Lead Fatigue	2004	Cond. B2	10	
Temperature Cycling	1010	Cond. C 50, 100, 200 cycles	5	consecutive 3 lots
Thermal Shock	1011	Cond. C 50, 100, 200 cycles	5	consecutive 3 lots
ESD sensitivity	3015	1000V	15	
Solderability	2003	Temp. 260°C±10°C	15	

TABLE III RELIABILITY MONITOR TEST

TEST	MIL-STD-883 METHOD	CONDITIONS	LTPD
Temperature Cycling	1010	–65°C to +150°C Air to Air No Bias, 200 cycles	7
Humidity		85°C/85% RH 5.5V Static 1000 HRS	7
Operating Life	1005	T_A = 125°C, V_{CC} = 5.5V Dynamic	7
Pressure Cooker		121°C, 100% RH 15 PSIG	7

Note:
1. The tests shown in the above Tables are typical requirements. Additional tests and the test sequence may vary by product.

PRODUCT SELECTION GUIDE

	Density	Part Number	Speed(s)	Icc Max. mA	Iccsb Max. mA	Package*
Static RAMs	2K x 8	MS6516	90, 100, 120 ns	70	2	P,S
	8K x 8	MS6264A	45, 55 ns	100	15	N, P, S
	8K x 8	MS6264C	80, 100, 150 ns	60	2	F, N, P
	8K x 8	MS6264	70, 100 ns	85	3	F, P
	32K x 8	MS62256A	25, 35, 45, 55 ns	120	20	P
	32K x 8	MS62256B	70, 100, 120, 150 ns	60	1	F, N, P
	32K x 8	MS62256	70, 85, 100 ns	85	15	F, P
	128K x 8	MS88128	100, 120 ns	95	15	Module
	128K x 8	MS621000	80, 100, 120 ns	80	3	F, P
	512Kx8	MS6M8512	85, 100, 120 ns	–	0.5	Module
Cache Data RAM	2 x 2K x 16	MS82C308	35, 45, 55 ns	150		J
Cache Tag RAM	2K x 20	MS8202	20, 22, 25 ns			J
Dual Port	1K x 8	MS6130	70, 90	120	0.01	D, P
Video Color Palette	256 x 18	MS176	40, 50 MHz	180		J, P
	256 x 18	MS177	40, 50 MHz	180	2	J
Latch RAM	8K x 8	MS6395	45, 70, 100 ns	90	3	F, P
	12K x 8	MS6397	45, 70, 100 ns	90	3	F, P
	16K x 8	MS6398	45, 70, 100 ns	90	3	F, P
Parity RAM	32K x 9	MS64100	25, 35 ns	130/110	25	
	32K x 9	MS64101	25, 35 ns	130/110	25	
FIFOs	256 x 9	MS7200	25, 35, 50, 80 ns	80	0.5	F, J, N, P
	512 x 9	MS7201A	25, 35, 50, 80 ns	80	0.5	F, J, N, P
	1024 x 9	MS7202A	25, 35, 50, 80 ns	80	0.5	F, J, N, P
	2048 x 9	MS7203	35, 50, 80 ns	125	2	F, J, N, P
	4096 x 9	MS7204	35, 50, 80 ns	125	2	F, J, N, P
	256 x 16	MS72105	25, 50, 80 ns	80	0.5	F, N
	512 x 16	MS72115	25, 50, 80 ns	80	0.5	F, N

D = 600 mil Sidebraze
F = 330 mil SOG
J = PLCC
N = 300 mil PDIP
P = 600 mil PDIP
S = 300 mil SOG
X = Die

PRODUCT SELECTION GUIDE (Continued)

1

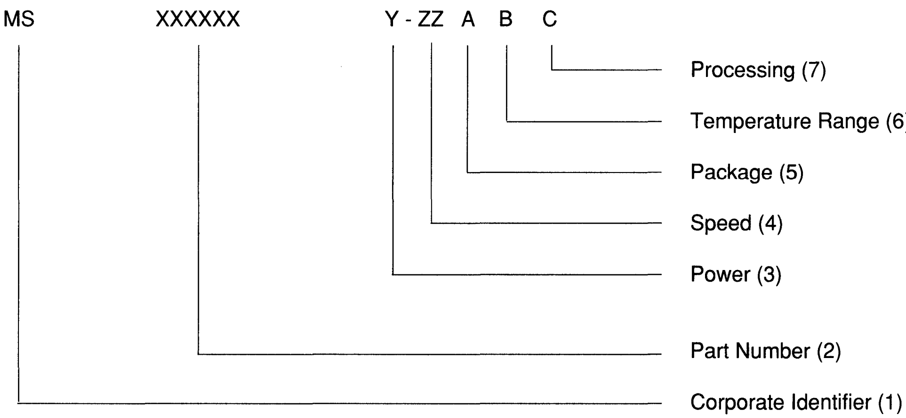
	Density Duration	Part Number	Speed(s)	Icc Max. mA	Iccsb Max. mA	Package*
ROMs	16K x 8	MS310128	150 ns	30		P
	32K x 8	MS310256	150 ns	30		P
	64K x 8	MS310512	150 ns	30		P
	128K x 8	MS311002	150, 200 ns	40	3	
	128K x 8	MS311024	150, 200 ns	40		P
	128K x 8	MS311025	100, 120, 150 ns	40	1.5	P
	128K x 8	MS311026	100, 120, 150 ns	40	1.5	P
	256K x 8	MS312001	150, 200 ns	40	1.5	P
	256K x 8	MS312002	200 ns	40	3	P
	512K x 8	MS314001	120, 150 ns	40	1.5	P
	512K x 8	MS314002	250 ns	50	3	P
	256K x 16/ 512K x 8	MS314003	250 ns	50	3	P
	1024K x 8	MS318002	200 ns	50	1	P, Q
	512K x 16/ 1024K x 8	MS318003	200 ns	50	1	P
Voice ROMs	1.5 sec	MSS0151				X
	2.8 sec	MSS0281				X
	3 sec	MSS0301				X
	6 sec	MSS0601				X
	15 sec	MSS1501				X
	20 sec	MSS2001				X

P = 600 mil PDIP
Q = Quad Flatpack
X = Die

ORDERING INFORMATION

MOSEL's ordering code number identifies the basic product, power, speed, package(s) available, operating temperature and processing method. The ordering code number is comprised of a series of alpha-numeric characters. Please refer to the following example:

Example:



(1) " MS" is the corporate identifier for MOS Electronic Corporation .

(2) Part number consists of maximum 6 alpha-numeric characters.

(3) A device power identifier. It is represented by "S" or blank as standard power consumption; or "L" as low power consumption.

(4) A device speed identifier. Its unit is either in nanoseconds or megahertz.

(5) Package types and codes:

N	—	P DIP 300 mil
P	—	P DIP 600 mil
T	—	Cer DIP 300 mil
D	—	Cer DIP 600 mil
L	—	LCC
J	—	PLCC
S	—	SOJ/SOG 300 mil
F	—	SOG 330 mil
Q	—	Quad Flatpack
X	—	Unpackaged Die
Y	—	Waffle Pack
Z	—	Plastic Zig-Zag In-Line

(6) Temperature Ranges:

C	=	Commercial	0°C to 70°C
L	=	Limited	-20°C to 85°C
I	=	Industrial	-40°C to 85°C
M	=	Military	-55°C to 125°C

(7) Processing method identifier. The use of this code is optional.

SRAM CROSS REFERENCE

1

DEVICE	MANUFACTURER	PART NUMBER	MOSEL PART NO.
2K x 8	Fujitsu	MB8416	MS6516
	Goldstar	GM76C28	MS6516
	Hitachi	HM6116	MS6516
	Hitachi	HM6216	MS6516
	Hyundai	HY6116	MS6516
	IDT	IDT6116	MS6516
	NEC	µPD446	MS6516
	RCA	CDM6116	MS6516
	SGS Thomson	MK48T02B	MS6516
	Toshiba	TC5517	MS6516
	Toshiba	TMM2016	MS6516
	Toshiba	TMM2018	MS6516
	UMC	UM6116	MS6516
	Winbond	W2416	MS6516
8K x 8	Asahi	AKM6264	MS6264
	Fujitsu	MB8464	MS6264
	Hitachi	HM6264	MS6264
	Hyundai	HY6264	MS6264
	IDT	IDT7165	MS6264A
	IDT	IDT7C165	MS6264A
	IDT	IDT7164	MS6264A
	Micron	MT5C6408	MS6264A
	Mitsubishi	M5M5165	MS6264
	Mitsubishi	M5M5178	MS6264
	Mitsubishi	M5M6165	MS6264
	Motorola	MCM6064	MS6264
	Motorola	MCM6164	MS6264A
	NEC	µPD4364	MS6264
	NEC	µPD4464	MS6264
	Samsung	KM6264	MS6264
	SGS Thomson	MK48H65	MS6264A
	SGS Thomson	MK48H74	MS6264A
	Sharp	LH5164	MS6264
	SMOS	SRM2064	MS6264
	Sony	CXK5864	MS6264
	Sony	CXX5863	MS6264
	Toshiba	TC5563	MS6264
	Toshiba	TC5564	MS6264
	Toshiba	TC5565	MS6264
	Toshiba	TC5588	MS6264
	Toshiba	TMM2063	MS6264
	Toshiba	TMM2064	MS6264
	Toshiba	TMM2088	MS6264
	Toshiba	TMM2089	MS6264
	UMC	UM6264	MS6264
	Winbond	W2464	MS6264

DEVICE	MANUFACTURER	PART NUMBER	MOSEL PART NO.
32K x 8	Fujitsu	MB84256	MS62256
	Hitachi	HM62256	MS62256
	IDT	IDT71256	MS62256
	Inova	S32K8	MS62256
	Mitsubishi	M5M5256	MS62256
	Motorola	MCM60L256	MS62256
	NEC	µPD43256	MS62256
	Samsung	KM62256	MS62256
	Sharp	LH52256	MS62256
	SMOS	SRM20256	MS62256
	Sony	CXK58257	MS62256
	Toshiba	TC55256	MS62256
	Toshiba	TC55257	MS62256
	Winbond	W24256	MS62256

FIFO CROSS REFERENCE

AMD	MOSEL
AM7200-25PC	7200-25PC
AM7200-35PC	7200-35PC
AM7200-50PC	7200-50PC
AM7200-65PC	7200-50PC
AM7200-80PC	7200-80PC
AM7200-25JC	7200-25JC
AM7200-35JC	7200-35JC
AM7200-50JC	7200-50JC
AM7200-65JC	7200-50JC
AM7200-80JC	7200-80JC
AM7200-25RC	7200-25NC
AM7200-35RC	7200-35NC
AM7200-50RC	7200-50NC
AM7200-65RC	7200-50NC
AM7200-80RC	7200-80NC
AM7201-25PC	7201A-25PC
AM7201-35PC	7201A-35PC
AM7201-50PC	7201A-50PC
AM7201-65PC	7201A-50PC
AM7201-80PC	7201A-80PC
AM7201-25JC	7201A-25JC
AM7201-35JC	7201A-35JC
AM7201-50JC	7201A-50JC
AM7201-65JC	7201A-50JC
AM7201-80JC	7201A-80JC
AM7201-25RC	7201A-25NC
AM7201-35RC	7201A-35NC
AM7201-50RC	7201A-50NC
AM7201-65RC	7201A-50NC
AM7201-80RC	7201A-80NC
AM7202-25PC	7202A-25PC
AM7202-35PC	7202A-35PC
AM7202-50PC	7202A-50PC
AM7202-65PC	7202A-50PC
AM7202-80PC	7202A-80PC
AM7202-25JC	7202A-25JC
AM7202-35JC	7202A-35JC
AM7202-50JC	7202A-50JC
AM7202-65JC	7202A-50JC
AM7202-80JC	7202A-80JC
AM7202-25RC	7202A-25NC
AM7202-35RC	7202A-35NC
AM7202-50RC	7202A-50NC
AM7202-65RC	7202A-50NC
AM7202-80RC	7202A-80NC
AM7203-35PC	7203-35PC
AM7203-50PC	7203-50PC
AM7203-65PC	7203-50PC
AM7203-80PC	7203-80PC
AM7203-35JC	7203-35JC
AM7203-50JC	7203-50JC
AM7203-65JC	7203-50JC
AM7203-80JC	7203-80JC
AM7204-35PC	7204-35PC
AM7204-50PC	7204-50PC
AM7204-65PC	7204-50PC
AM7204-80PC	7204-80PC
AM7204-120PC	7204-80PC
AM7204-35JC	7204-35JC
AM7204-50JC	7204-50JC
AM7204-65JC	7204-50JC
AM7204-80JC	7204-80JC
AM7204-120JC	7204-80JC

CYPRESS	MOSEL
CY7C420-30PC	7201A-25PC
CY7C420-40PC	7201A-35PC
CY7C420-65PC	7201A-50PC
CY7C421-30PC	7201A-25NC
CY7C421-40PC	7201A-35NC
CY7C421-65PC	7201A-50NC
CY7C421-30JC	7201A-25JC
CY7C421-40JC	7201A-35JC
CY7C421-65JC	7201A-50JC
CY7C424-30PC	7202A-25PC
CY7C424-40PC	7202A-35PC
CY7C424-65PC	7202A-50PC
CY7C425-30PC	7202A-25NC
CY7C425-40PC	7202A-35NC
CY7C425-65PC	7202A-50NC
CY7C425-30JC	7202A-25JC
CY7C425-40JC	7202A-35JC
CY7C425-65JC	7202A-50JC
CY7C428-40PC	7203-35PC
CY7C428-65PC	7203-50PC
CY7C429-40PC	7203-35NC
CY7C429-65PC	7203-50NC
CY7C429-40JC	7203-35JC
CY7C429-65JC	7203-50JC

DALLAS	MOSEL
DS2009-35	7201A-35PC
DS2009-50	7201A-50PC
DS2009-65	7201A-50PC
DS2009-80	7201A-80PC
DS2009R-35	7201A-35JC
DS2009R-50	7201A-50JC
DS2009R-65	7201A-50JC
DS2009R-80	7201A-80JC
DS2010-35	7202A-35PC
DS2010-50	7202A-50PC
DS2010-65	7202A-50PC
DS2010-80	7202A-80PC
DS2010R-35	7202A-35JC
DS2010R-50	7202A-50JC

DS2010R-65	7202A-50JC
DS2010R-80	7202A-80JC
DS2011-35	7203A-35PC
DS2011-50	7203A-50PC
DS2011-65	7203A-50PC
DS2011-80	7203A-80PC
DS2011R-35	7203A-35JC
DS2011R-50	7203A-50JC
DS2011R-65	7203A-50JC
DS2011R-80	7203A-80JC

IDT	**MOSEL**
IDT7200L25TP	7200L-25NC
IDT7200L35TP	7200L-35NC
IDT7200L50TP	7200L-50NC
IDT7200L65TP	7200L-50NC
IDT7200L80TP	7200L-80NC
IDT7200L120TP	7200L-80NC
IDT7200L25J	7200L-25JC
IDT7200L35J	7200L-35JC
IDT7200L50J	7200L-50JC
IDT7200L65J	7200L-50JC
IDT7200L80J	7200L-80JC
IDT7200L120J	7200L-80JC
IDT7200L25SO	7200L-25FC
IDT7200L35SO	7200L-35FC
IDT7200L50SO	7200L-50FC
IDT7200L65SO	7200L-50FC
IDT7200L80SO	7200L-80FC
IDT7200L120SO	7200L-80FC
IDT7200S25TP	7200-25NC
IDT7200S35TP	7200-35NC
IDT7200S50TP	7200-50NC
IDT7200S65TP	7200-50NC
IDT7200S80TP	7200-80NC
IDT7200S120TP	7200-80NC
IDT7200S25J	7200-25JC
IDT7200S35J	7200-35JC
IDT7200S50J	7200-50JC
IDT7200S65J	7200-50JC
IDT7200S80J	7200-80JC
IDT7200S120J	7200-80JC
IDT7200S25SO	7200-25FC
IDT7200S35SO	7200-35FC
IDT7200S50SO	7200-50FC
IDT7200S65SO	7200-50FC
IDT7200S80SO	7200-80FC
IDT7200S120SO	7200-80FC
IDT7201L50P	7201AL-50PC
IDT7201L65P	7201AL-50PC
IDT7201L80P	7201AL-80PC
IDT7201L120P	7201AL-80PC
IDT7201L50J	7201AL-50JC
IDT7201L65J	7201AL-50JC
IDT7201L80J	7201AL-80JC
IDT7201L120J	7201AL-80JC
IDT7201LA25P	7201AL-25PC
IDT7201LA35P	7201AL-35PC
IDT7201LA50P	7201AL-50PC
IDT7201LA65P	7201AL-50PC
IDT7201LA80P	7201AL-80JC
IDT7201LA120P	7201AL-80JC
IDT7201LA25TP	7201AL-25NC
IDT7201LA35TP	7201AL-35NC
IDT7201LA50TP	7201AL-50NC
IDT7201LA65TP	7201AL-50NC
IDT7201LA80TP	7201AL-80NC
IDT7201LA120TP	7201AL-80NC
IDT7201LA25J	7201AL-25JC
IDT7201LA35J	7201AL-35JC
IDT7201LA50J	7201AL-50JC
IDT7201LA65J	7201AL-50JC
IDT7201LA80J	7201AL-80JC
IDT7201LA120J	7201AL-80JC
IDT7201LA25SO	7201AL-25FC
IDT7201LA35SO	7201AL-35FC
IDT7201LA50SO	7201AL-50FC
IDT7201LA65SO	7201AL-50FC
IDT7201LA80SO	7201AL-80FC
IDT7201LA120SO	7201AL-80FC
IDT7201S50P	7201A-50PC
IDT7201S65P	7201A-50PC
IDT7201S80P	7201A-80PC
IDT7201S120P	7201A-80PC
IDT7201S50J	7201A-50JC
IDT7201S65J	7201A-50JC
IDT7201S80J	7201A-80JC
IDT7201S120J	7201A-80JC
IDT7201SA25P	7201A-25PC
IDT7201SA35P	7201A-35PC
IDT7201SA50P	7201A-50PC
IDT7201SA65P	7201A-50PC
IDT7201SA80P	7201A-80PC
IDT7201SA120P	7201A-80PC
IDT7201SA25TP	7201A-25NC
IDT7201SA35TP	7201A-35NC
IDT7201SA50TP	7201A-50NC
IDT7201SA65TP	7201A-50NC
IDT7201SA80TP	7201A-80NC
IDT7201SA120TP	7201A-80NC
IDT7201SA25J	7201A-25JC
IDT7201SA35J	7201A-35JC
IDT7201SA50J	7201A-50JC
IDT7201SA65J	7201A-50JC
IDT7201SA80J	7201A-80JC
IDT7201SA120J	7201A-80JC
IDT7201SA25SO	7201A-25FC
IDT7201SA35SO	7201A-35FC
IDT7201SA50SO	7201A-50FC
IDT7201SA65SO	7201A-50FC
IDT7201SA80SO	7201A-80FC
IDT7201SA120SO	7201A-80FC
IDT7202L50P	7202AL-50PC
IDT7202L65P	7202AL-50PC

FIFO CROSS REFERENCE

IDT7202L80P	7202AL-80PC
IDT7202L120P	7202AL-80PC
IDT7202L50J	7202AL-50JC
IDT7202L65J	7202AL-50JC
IDT7202L80J	7202AL-80JC
IDT7202L120J	7202AL-80JC
IDT7202LA25P	7202AL-25PC
IDT7202LA35P	7202AL-35PC
IDT7202LA50P	7202AL-50PC
IDT7202LA65P	7202AL-50PC
IDT7202LA80P	7202AL-80PC
IDT7202LA120P	7201AL-80PC
IDT7202LA25TP	7202AL-25NC
IDT7202LA35TP	7202AL-35NC
IDT7202LA50TP	7202AL-50NC
IDT7202LA65TP	7202AL-50NC
IDT7202LA80TP	7202AL-80NC
IDT7202LA120TP	7202AL-80NC
IDT7202LA25J	7202AL-25JC
IDT7202LA35J	7202AL-35JC
IDT7202LA50J	7202AL-50JC
IDT7202LA65J	7202AL-50JC
IDT7202LA80J	7202AL-80JC
IDT7202LA120J	7202AL-80JC
IDT7202LA25SO	7202AL-25FC
IDT7202LA35SO	7202AL-35FC
IDT7202LA50SO	7202AL-50FC
IDT7202LA65SO	7202AL-50FC
IDT7202LA80SO	7202AL-80FC
IDT7202LA120SO	7202AL-80FC
IDT7202S50P	7202A-50PC
IDT7202S65P	7202A-50PC
IDT7202S80P	7202A-80PC
IDT7202S120P	7202A-80PC
IDT7202S50J	7202A-50JC
IDT7202S65J	7202A-50JC
IDT7202S80J	7202A-80JC
IDT7201S120J	7202A-80JC
IDT7202SA25P	7202A-25PC
IDT7202SA35P	7202A-35PC
IDT7202SA50P	7202A-50PC
IDT7202SA65P	7202A-50PC
IDT7202SA80P	7202A-80PC
IDT7202SA120P	7202A-80PC
IDT7202SA25TP	7202A-25NC
IDT7202SA35TP	7202A-35NC
IDT7202SA50TP	7202A-50NC
IDT7202SA65TP	7202A-50NC
IDT7202SA80TP	7202A-80NC
IDT7202SA120TP	7202A-80NC
IDT7202SA25J	7202A-25JC
IDT7202SA35J	7202A-35JC
IDT7202SA50J	7202A-50JC
IDT7202SA65J	7202A-50JC
IDT7202SA80J	7202A-80JC
IDT7202SA120J	7202A-80JC
IDT7202SA25SO	7202A-25FC
IDT7202SA35SO	7202A-35FC
IDT7202SA50SO	7202A-50FC
IDT7202SA65SO	7202A-50FC
IDT7202SA80SO	7202A-80FC
IDT7202SA120SO	7202A-80FC
IDT7203L35P	7203L-35PC
IDT7203L50P	7203L-50PC
IDT7203L65P	7203L-50PC
IDT7203L80P	7203L-80PC
IDT7203L120P	7203L-80PC
IDT7203L35J	7203L-35JC
IDT7203L50J	7203L-50JC
IDT7203L65J	7203L-50JC
IDT7203L80J	7203L-80JC
IDT7203L120J	7203L-80JC
IDT7203S35P	7203-35PC
IDT7203S50P	7203-50PC
IDT7203S65P	7203-50PC
IDT7203S80P	7203-80PC
IDT7203S120P	7203-80PC
IDT7203S35J	7203-35JC
IDT7203S50J	7203-50JC
IDT7203S65J	7203-50JC
IDT7203S80J	7203-80JC
IDT7203S120J	7203-80JC
IDT7204L35P	7204L-35PC
IDT7204L50P	7204L-50PC
IDT7204L65P	7204L-50PC
IDT7204L80P	7204L-80PC
IDT7204L120P	7204L-80PC
IDT7204L35J	7204L-35JC
IDT7204L50J	7204L-50JC
IDT7204L65J	7204L-50JC
IDT7204L80J	7204L-80JC
IDT7204L120J	7204L-80JC
IDT7204S35P	7204-35PC
IDT7204S50P	7204-50PC
IDT7204S65P	7204-50PC
IDT7204S80P	7204-80PC
IDT7204S120P	7204-80PC
IDT7204S35J	7204-35JC
IDT7204S50J	7204-50JC
IDT7204S65J	7204-50JC
IDT7204S80J	7204-80JC
IDT7204S120J	7204-80JC
IDT72105L50TP	72105-50NC
IDT72105L80TP	72105-80NC
IDT72105L120TP	72105-80NC
IDT72105L50SO	72105-50FC
IDT72105L80SO	72105-80FC
IDT72105L120SO	72105-80FC
IDT72105L50J	72105-50JC
IDT72105L80J	72105-80JC
IDT72105L120J	72105-80JC
IDT72115L50TP	72115-50NC
IDT72115L80TP	72115-80NC
IDT72115L120TP	72115-80NC

IDT72115L50SO	72115-50FC
IDT72115L80SO	72115-80FC
IDT72115L120SO	72115-80FC
IDT72115L50J	72115-50JC
IDT72115L80J	72115-80JC
IDT72115L120J	72115-80JC

MOSTEK	**MOSEL**
MK4501-10N	7201A-80PC
MK4501-12N	7201A-80PC
MK4501-15N	7201A-80PC
MK4501-20N	7201A-80PC
MK4501-65N	7201A-50PC
MK4501-80N	7201A-80PC
MK4503-10N	7203A-80PC
MK4503-12N	7203A-80PC
MK4503-15N	7203A-80PC
MK4503-20N	7203A-80PC
MK4503-65N	7203A-50PC
MK4503-80N	7203A-80PC

SAMSUNG	**MOSEL**
KM75C01AP-25	7201A-25PC
KM75C01AP-35	7201A-35PC
KM75C01AP-80	7201A-80PC
KM75C01AJ-25	7201A-25JC
KM75C01AJ-35	7201A-35JC
KM75C01AJ-80	7201A-80JC
KM75C01AN-25	7201A-25NC
KM75C01AN-35	7201A-35NC
KM75C01AN-80	7201A-80NC
KM75C02AP-25	7202A-25PC
KM75C02AP-35	7202A-35PC
KM75C02AP-80	7202A-80PC
KM75C02AJ-25	7202A-25JC
KM75C02AJ-35	7202A-35JC
KM75C02AJ-80	7202A-80JC
KM75C02AN-25	7202A-25NC
KM75C02AN-35	7202A-35NC
KM75C02AN-80	7202A-80NC
KM75C03AP-35	7203A-35PC
KM75C03AP-80	7203A-80PC
KM75C03AJ-35	7203A-35JC
KM75C03AJ-80	7203A-80JC
KM75C03AN-35	7203A-35NC
KM75C03AN-80	7203A-80NC

SHARP	**MOSEL**
LH5495D-25	7200-25NC
LH5495D-35	7200-35NC
LH5495D-45	7200-35NC
LH5496-35	7201A-35PC
LH5496-50	7201A-50PC
LH5496D-35	7201A-35NC
LH5496D-50	7201A-50NC
LH5497-35	7202A-35PC
LH5497-50	7202A-50PC
LH5497D-35	7202A-35NC
LH5497D-50	7202A-50NC
LH5498-35	7203-35PC
LH5498-50	7203-50PC
LH5498D-35	7203-35NC
LH5498D-50	7203-50NC

TI	**MOSEL**
SN74ACT7201A-35N	7201AL-35PC
SN74ACT7201A-50N	7201AL-50PC
SN74ACT7202-35N	7202AL-35PC
SN74ACT7202-50N	7202AL-50PC

DUAL PORTS CROSS REFERENCE

IDT	**MOSEL**
IDT7130LA55P	6130L-55PC
IDT7130LA70P	6130L-70PC
IDT7130LA90P	6130L-90PC
IDT7130SA55P	6130L-55PC
IDT7130SA70P	6130L-70PC
IDT7130SA90P	6130L-90PC

General Information

Static RAMs (Random Access Memory) 2

ROMs (Read Only Memory)

Voice ROMs

Cache Products

MOSEL Sales Network

BYTEWIDE STATIC RAMS

MOSEL has developed a broad line of slow and fast bytewide static RAMs from 16K bits to 4 megabits, including monolithic products at 16K, 64K, 256K and 1 megabit (sampling) and module products at 1 megabit and 4 megabits. SRAM products are offered in JEDEC standard plastic dip and/or plastic surface mount packages.

PRODUCTION PRODUCTS

At the 256K density, MOSEL offers the 32K x 8 MS62256L, MS62256AL and the MS62256BL products, with speeds of 45, 55, 70, 85 and 100ns available today in the 600 mil dip and 330 SOG packages. Future product enhancements are planned for 1991 to provide faster speeds (15 to 25ns), lower power, additional package options including the 300 mil dip package, and reduced costs.

At the 64K density, Mosel offers the 8K x 8 MS6264L, MS6264AL and MS6264CL products with speeds of 45, 55, 70, 85 and 100 ns available today in the 300 mil DIP (45-70ns only), 600 mil DIP and 330 SOIC package. Future product enhancements are planned for 1991 to provide faster speeds (15 to 25ns) and to reduce power consumption.

At the 16K density, the 2K x 8 MS6516 is offered at 100ns speed in the 600 mil dip package. Future product enhancements are planned to reduce the active power and to offer surface mount of 300 mil dip packages.

DEVELOPMENT PRODUCTS

MOSEL has successfully developed and has recently begun sampling the MS621000 monolithic 1 megabit 128K x 8 SRAM, with speeds of 80 to 100ns. Production release is scheduled for late 1990. Also under development are higher speed 1 megabit devices (20 to 25ns) and the 4 megabit 512K x 8 SRAM.

MODULE PRODUCTS

In module form, MOSEL, offers the MS88128 128K x 8 and has recently begun sampling the MS6M8512 512K x 8 SRAM module. These JEDEC pin out devices provide a prototype and pilot production vehicle for designers who want to use future generation density products today.

SRAM TECHNOLOGY

Since 1983, MOSEL has developed and transferred to production 4 generations of CMOS SRAM technology at 2.0, 1.5, 1.2 and 1.0 micron geometries. Currently, 0.8 and 0.55 micron technologies are under development. During this time period, the size of the SRAM memory cell has been reduced from 815 square microns at 2 micron geometry, to 70 at 1 micron and on to 19 at 0.55 micron, a 40 fold reduction. These technology advances have permitted product density to increase from 16K at 2 micron to 1 megabit at 1 micron and on to 4 Megabits at 0.55 microns. Meanwhile, product access times have been reduced from 70ns at 2 micron, to 20ns at 1 micron and on to 10ns at 0.55 micron.

SUMMARY

MOSEL is committed to continue to build our bytewide static RAM product offering and advance our SRAM manufacturing technology. This includes plans to strengthen our support of older products such as the slow speed 16K 2K x 8, 64K 8K x 8 and 256K 32K x 8 SRAMs by redesigning using 1 megabit 0.8 micron technology which cuts costs, improve product specifications and extends product life. It also includes plans to increase density of our products to 1 and 4 megabits and to improve performance of existing products.

If you are interested in more information about our SRAM products, please contact your local MOSEL sales representative or franchised distributors listed in this book.

MOSEL MS6516

2K x 8 CMOS Static RAM

2

FEATURES

- Available in 100 and 120 ns (Max.) versions
- Automatic power-down when chip disabled
- Low power consumption (L-version):
  - 385mW (Max.) Operating
  - 11mW (Max.) Standby
  - 275µW (Max.) Power-down
- TTL compatible interface levels
- Single 5V power supply
- Fully static operation
- Three state outputs
- Chip enable for simple memory expansion
- Data retention as low as 2V

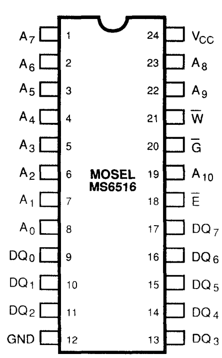
DESCRIPTION

The MOSEL MS6516 is a high performance, low power CMOS static RAM organized as 2048 words by 8 bits. The device supports easy memory expansion with an active LOW chip enable ($\overline{E}$) as well as an active LOW output enable ($\overline{G}$) and three-state outputs. An automatic power-down feature is included which reduces the chip power by 85% in TTL standby mode, and by over 99% in full power-down mode.

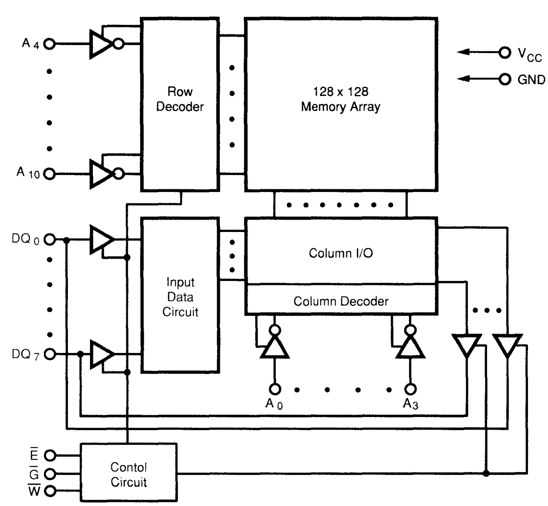
The device is manufactured in MOSEL's high performance CMOS process and operates from a single 5V power supply. All inputs and outputs are TTL compatible. Data is retained to as low as V_{CC} = 2V.

The MOSEL MS6516 is available in the JEDEC standard 24 pin 600 mil wide DIP and small outline package.

PIN CONFIGURATIONS



FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

A_0 - A_{10} Address Inputs

These 11 address inputs select one of the 2048 8-bit words in the RAM.

$\overline{E}$ Chip Enable Input

$\overline{E}$ is active LOW. The chip enable must be active to read from or write to the device. If it is not active, the device is deselected and is in a standby power mode. The DQ pins will be in the high-impedance state when deselected.

$\overline{G}$ Output Enable Input

The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when $\overline{G}$ is inactive.

$\overline{W}$ Write Enable Input

The write enable input is active LOW and controls read and write operations. With the chip enabled, when $\overline{W}$ is HIGH and $\overline{G}$ is LOW, output data will be present at the DQ pins; when $\overline{W}$ is LOW, the data present on the DQ pins will be written into the selected memory location.

DQ_0 - DQ_7 Data Input/Output Ports

These 8 bidirectional ports are used to read data from or write data into the RAM.

V_{CC} Power Supply

GND Ground

TRUTH TABLE

MODE	$\overline{E}$	$\overline{G}$	$\overline{W}$	I/O OPERATION
Standby	H	X	X	High Z
Read	L	L	H	D_{OUT}
Read	L	H	H	High Z
Write	L	X	L	D_{IN}

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	PARAMETER		RATING	UNITS
V_{CC} • GND	Supply Voltage		-0.3 to 7	
V_{IN}	Input Voltage		-0.3 to 7	V
$V_{I/O}$	Input/Output Voltage Applied		-0.3 to V_{CC} + 0.3	
T_{BIAS}	Temperature Under Bias	Plastic	-10 to +85	°C
T_{STG}	Storage Temperature	Plastic	-40 to +125	°C
P_D	Power Dissipation		1.0	W
I_{OUT}	DC Output Current		50	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

OPERATING RANGE

RANGE	AMBIENT TEMPERATURE	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

DC ELECTRICAL CHARACTERISTICS (over the commercial operating range)

PARAMETER NAME	PARAMETER	TEST CONDITIONS	MS6516L MIN.	MS6516L TYP.(1)	MS6516L MAX.	MS6516S MIN.	MS6516S TYP.(1)	MS6516S MAX.	UNITS
V_{IL}	Guaranteed Input Low Voltage(2)		-0.3	-	+0.8	-0.3	-	+0.8	V
V_{IH}	Guaranteed Input High Voltage(2)		2.2	-	V_{CC}+ 0.3	2.2	-	V_{CC}+ 0.3	V
I_{IL}	Input Leakage Current	V_{CC} = Max, V_{IN} = 0V to V_{CC}	-	-	10	-	-	10	μA
I_{OL}	Output Leakage Current	V_{CC} = Max, $\overline{E}$ = V_{IH}, or $\overline{G}$ = V_{IH}, V_{IN} = 0V to V_{CC}	-	-	10	-	-	10	μA
V_{OL}	Output Low Voltage	V_{CC} = Min, I_{OL} = 4mA	-	0.21	0.4	-	0.21	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min, I_{OH} = -1.0mA	2.4	3.5	-	2.4	3.5	-	V
I_{CC}	Operating Power Supply Current	V_{CC} = Max, $\overline{E}$ = V_{IL}, $I_{I/O}$ = 0mA, F_{max}(3)	-	40	70	-	60	90	mA
I_{CCSB}	Standby Power Supply Current	V_{CC} = Max, $\overline{E}$ = V_{IH}, $I_{I/O}$ = 0mA	-	0.5	2	-	2	10	mA
I_{CCSB1}	Power Down Power Supply Current	V_{CC} = Max, $\overline{E}$ > V_{CC} - 0.2V, $\overline{G}$ > V_{CC} - 0.2V V_{IN} > V_{CC} - 0.2V or V_{IN} < 0.2V	-	1	10	-	10	100	μA

1. Typical characteristics are at V_{CC} = 5V, T_A = 25°C.
2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
3. F_{MAX} = $1/t_{RC}$.

CAPACITANCE(1) (T_A = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$ = 0V	10	pF

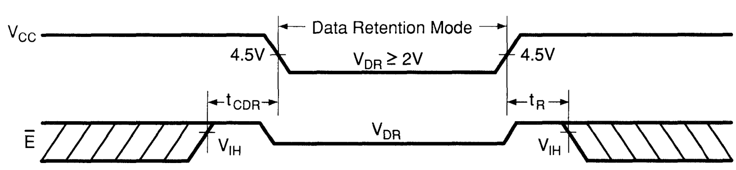
1. This parameter is guaranteed and not tested.

DATA RETENTION CHARACTERISTICS (over the commercial operating range)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.(2)	MAX(3)	UNITS
V_{DR}	V_{CC} for Data Retention	$\overline{E}$ = V_{CC}	2.0	-	-	V
I_{CCDR}	Data Retention Current	V_{IN} = 0V or V_{CC}	-	2	10	μA
t_{CDR}	Chip Deselect to Data Retention Time	V_{CC} = 2.0V, $\overline{E}$ = V_{CC}	0	-	-	ns
t_R	Operation Recovery Time	V_{IN} = 0V or V_{CC}	t_{RC}(2)	-	-	ns

1. V_{CC} = 2V, T_A = +25°C
2. t_{RC} = Read Cycle Time

TIMING WAVEFORM LOW V_{CC} DATA RETENTION WAVEFORM

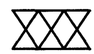
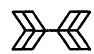


2

AC TEST CONDITIONS

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Level	1.5V

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

AC TEST LOADS AND WAVEFORMS

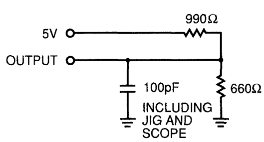


Figure 1a

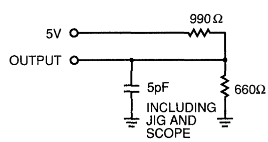
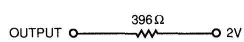


Figure 1b

Equivalent to:

THEVENIN EQUIVALENT



ALL INPUT PULSES

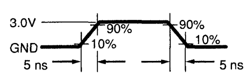


Figure 2

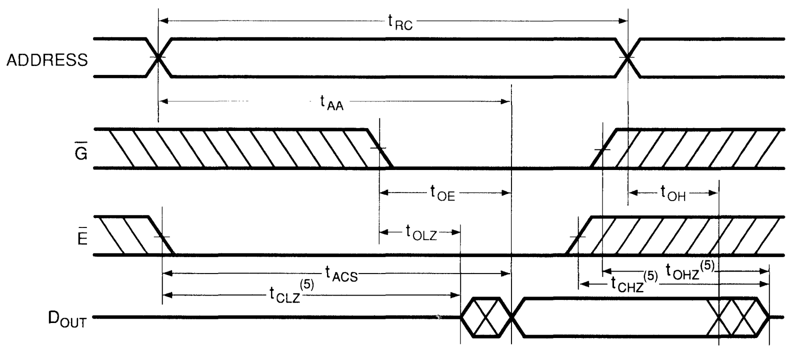
AC ELECTRICAL CHARACTERISTICS (over the commercial operating range)

READ CYCLE

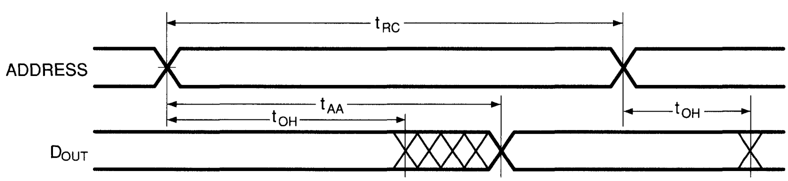
JEDEC PARAMETER NAME	PARAMETER NAME	PARAMETER	-10 MIN.	-10 MAX.	-12 MIN.	-12 MAX.	UNIT
t_{AVAX}	t_{RC}	Read Cycle Time	100	-	120	-	ns
t_{AVQV}	t_{AA}	Address Access Time	-	100	-	120	ns
t_{ELQV}	t_{ACS}	Chip Enable Access Time	-	100	-	120	ns
t_{GLQV}	t_{OE}	Output Enable to Output Valid	-	50	-	50	ns
t_{ELQX}	t_{CLZ}	Chip Enable to Output Low Z	5	-	10	-	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z	5	-	10	-	ns
t_{EHQZ}	t_{CHZ}	Chip Disable to Output in High Z	0	40	0	40	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z	0	35	0	40	ns
t_{AXQX}	t_{OH}	Output Hold from Address Change	5	-	10	-	ns

SWITCHING WAVEFORMS (READ CYCLE)

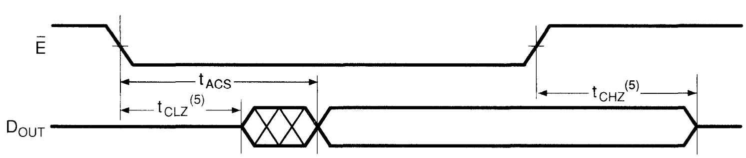
READ CYCLE 1[(1)]



READ CYCLE 2[(1, 2, 4)]



READ CYCLE 3[(1, 3, 4)]



NOTES:
1. $\overline{W}$ is High for READ Cycle.
2. Device is continuously selected $\overline{E} = V_{IL}$.
3. Address valid prior to or coincident with $\overline{E}$ transition low.
4. $\overline{G} = V_{IL}$.
5. Transition is measured ± 500mV from steady state with C_L = 5pF as shown in Figure 1b on page 4. This parameter is guaranteed and not 100% tested.

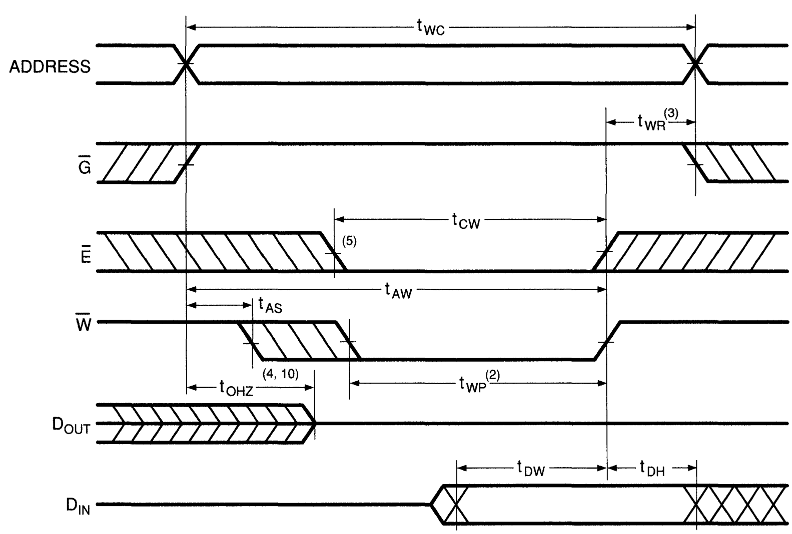
AC ELECTRICAL CHARACTERISTICS (over the commercial operating range)

WRITE CYCLE

JEDEC PARAMETER NAME	PARAMETER NAME	PARAMETER	-10 MIN.	-10 MAX.	-12 MIN.	-12 MAX.	UNIT
t_{AVAX}	t_{WC}	Write Cycle Time	100	-	120	-	ns
t_{ELWH}	t_{CW}	Chip Enable to End of Write	55	-	70	-	ns
t_{AVWL}	t_{AS}	Address Set up Time	0	-	0	-	ns
t_{AVWH}	t_{AW}	Address Valid to End of Write	80	-	85	-	ns
t_{WLWH}	t_{WP}	Write Pulse Width	50	-	70	-	ns
t_{WHAX}	t_{WR}	Write Recovery Time	0	-	0	-	ns
t_{WLQZ}	t_{WHZ}	Write to Output in High Z	-	35	-	50	ns
t_{DVWH}	t_{DW}	Data Valid to End of Write	30	-	35	-	ns
t_{WHDX}	t_{DH}	Data Hold from Write Time	0	-	0	-	ns
t_{GHZQ}	t_{OHZ}	Output Disable to Output in High Z	0	35	0	40	ns
t_{WHQX}	t_{OW}	Output Active from End of Write	0	-	5	-	ns

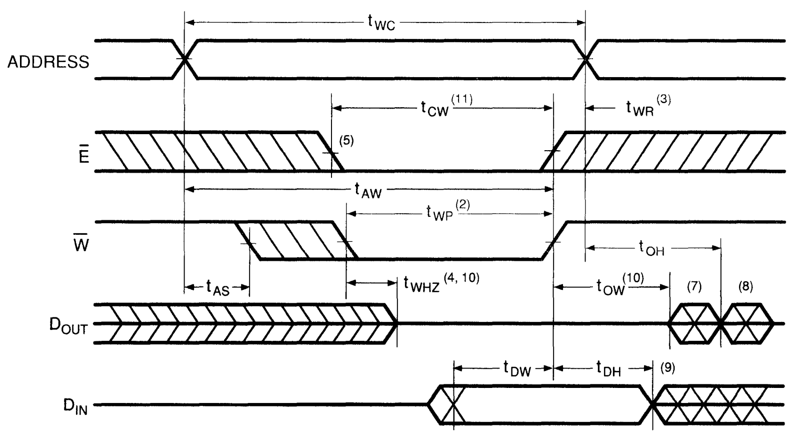
SWITCHING WAVEFORMS (WRITE CYCLE)

WRITE CYCLE 1[1]



SWITCHING WAVEFORMS (WRITE CYCLE)

WRITE CYCLE 2(1,6)



NOTES:

1. $\overline{W}$ must be high during address transitions.
2. The internal write time of the memory is defined by the overlap $\overline{E}$ active and $\overline{W}$ low. Both signals must be active to initiate and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
3. T_{WR} is measured from the earlier of $\overline{E}$ or $\overline{W}$ going high at the end of write cycle.
4. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{E}$ low transition occurs simultaneously with the $\overline{W}$ low transitions or after the $\overline{W}$ low transition, outputs remain in a high impedance state.
6. $\overline{G}$ is continuously low ($\overline{G} = V_{IL}$).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\overline{E}$ is low during this period, DQ pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured ±500mV from steady state with C_L = 5pF as shown in Figure 1b on page 4. This parameter is guaranteed and not 100% tested.
11. t_{CW} is measured from $\overline{E}$ going low to the end of write.

ORDERING INFORMATION

SPEED (ns)	ORDERING PART NUMBER	PACKAGE REFERENCE NO.	TEMPERATURE RANGE
100	MS6516L-10PC	P24-1	0°C to +70°C
100	MS6516S-10PC		0°C to +70°C
120	MS6516S-12SC	S24-1	0°C to +70°C

8K x 8 CMOS Static RAM

FEATURES

- Available in 70/100 ns (Max.)
- Automatic power-down when chip disabled
- Lower power consumption:

  MS6264
  – 300mW (Typ.) Operating
  – 100µW (Typ.) Standby
  MS6264L
  – 275mW (Typ.) Operating
  – 50µW (Typ.) Standby
- TTL compatible interface levels
- Single 5V power supply
- Fully static operation
- Three state outputs
- Two chip enable ($\overline{E}_1$ and E_2) for simple memory expansion
- Data retention as low as 2V

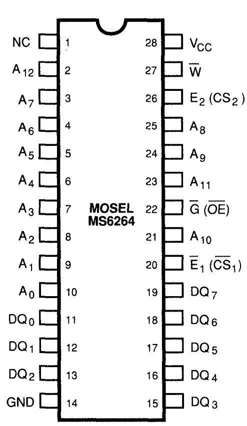
DESCRIPTION

The MOSEL MS6264 is a high performance, low power CMOS static RAM organized as 8192 words by 8 bits. The device supports easy memory expansion with both an active LOW chip enable ($\overline{E}_1$) and an active High chip enable (E_2), as well as an active LOW output enable ($\overline{G}$) and tri-state outputs. An automatic power-down feature is included which reduces the chip power by 80% in TTL standby mode, and by over 95% in full power-down mode.

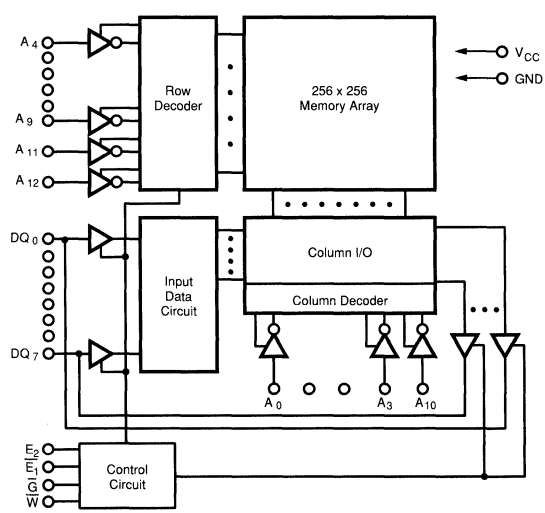
The device is manufactured in MOSEL's high performance CMOS process and operates from a single 5V power supply. All inputs and outputs are TTL compatible. Data is retained to as low as V_{CC} = 2V.

The MOSEL MS6264 is packaged in the JEDEC standard 28 pin 600 mil wide DIP and 330 mil wide SOP.

PIN CONFIGURATIONS



FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

A_0 - A_{12} Address Inputs

These 13 address inputs select one of the 8192 8-bit words in the RAM.

$\overline{E}_1$ Chip Enable 1 Input

E_2 Chip Enable 2 Input

$\overline{E}_1$ is active LOW and E_2 is active HIGH. Both chip enables must be active to read from or write to the device. If either chip enable is not active, the device is deselected and is in a standby power mode. The DQ pins will be in the high-impedance state when the device is deselected.

$\overline{G}$ Output Enable Input

The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when $\overline{G}$ is inactive.

$\overline{W}$ Write Enable Input

The write enable input is active LOW and controls read and write operations. With the chip selected, when $\overline{W}$ is HIGH and $\overline{G}$ is LOW, output data will be present at the DQ pins; when $\overline{W}$ is LOW, the data present on the DQ pins will be written into the selected memory location.

DQ_0 - DQ_7 Data Input/Output Ports

These 8 bidirectional ports are used to read data from or write data into the RAM.

V_{CC} Power Supply

GND Ground

TRUTH TABLE

MODE	$\overline{W}$	$\overline{E}_1$	E_2	$\overline{G}$	I/O OPERATION	V_{CC} CURRENT
Not Selected	X	H	X	X	High Z	I_{CCSB}, I_{CCSB1}
(Power Down)	X	X	L	X	High Z	I_{CCSB}, I_{CCSB1}
Output Disabled	H	L	H	H	High Z	I_{CC}
Read	H	L	H	L	D_{OUT}	I_{CC}
Write	L	L	H	X	D_{IN}	I_{CC}

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	PARAMETER	RATING	UNITS
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_{BIAS}	Temperature Under Bias	-10 to +125	°C
T_{STG}	Storage Temperature	-60 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	20	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

RANGE	AMBIENT TEMPERATURE	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

CAPACITANCE(1) (T_A = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{DQ}	Input/Output Capacitance	$V_{I/O}$ = 0V	8	pF

1. This parameter is guaranteed and not tested.

DC ELECTRICAL CHARACTERISTICS (over the operating range)

PARAMETER NAME	PARAMETER	TEST CONDITIONS	MS6264 MIN.	MS6264 TYP.(1)	MS6264 MAX.	MS6264L MIN.	MS6264L TYP.(1)	MS6264L MAX.	UNITS
V_{IL}	Guaranteed Input Low Voltage(2)		-0.5	-	+0.8	-0.5	-	+0.8	V
V_{IH}	Guaranteed Input High Voltage(2)		2.2	3.5	6.0	2.2	3.5	6.0	V
I_{IL}	Input Leakage Current	V_{CC} = Max, V_{IN} = 0V to V_{CC}	-	-	2	-	-	2	µA
I_{OL}	Output Leakage Current	V_{CC} = Max, $\bar{E}_1 = V_{IH}$, or $E_2 = V_{IL}$, or $\bar{G} = V_{IH}$, V_{IN} = 0V to V_{CC}	-	-	2	-	-	2	µA
V_{OL}	Output Low Voltage	V_{CC} = Min, I_{OL} = 4mA	-	-	0.4	-	-	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min, I_{OH} = -1mA	2.4	-	-	2.4	-	-	V
I_{CC}	Operating Power Supply Current	V_{CC} = Max, $\bar{E}_1 = V_{IL}$, $E_2 = V_{IH}$, I_{DQ} = 0mA, $F = F_{max}$(3)	-	50	90	-	45	85	mA
I_{CCSB}	Standby Power Supply Current	V_{CC} = Max, $\bar{E}_1 = V_{IH}$, or $E_2 = V_{IL}$, I_{DQ} = 0mA	-	-	15	-	-	3	mA
I_{CCSB1}	Power Down Power Supply Current	V_{CC} = Max, $\bar{E}_1 > V_{CC}$ - 0.2V, $E_2 < 0.2V$ $V_{IN} > V_{CC}$ - 0.2V or $V_{IN} < 0.2V$	-	.02	2	-	.01	0.1	mA

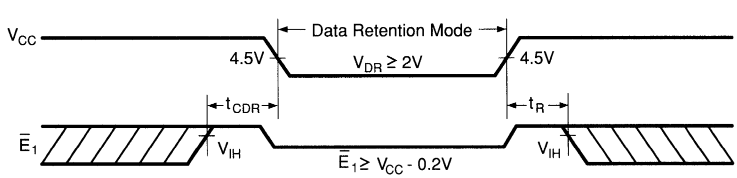
1. Typical characteristics are at V_{CC} = 5V, T_A = 25°C.
2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
3. $F_{MAX} = 1/t_{RC}$.

DATA RETENTION CHARACTERISTICS (T_A = 0 to +70°C)

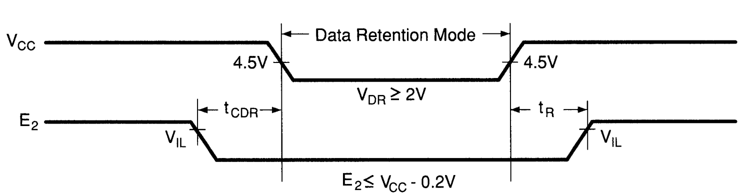
SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.(1)	MAX.	UNITS
V_{DR}	V_{CC} for Data Retention	$\bar{E}_1 \geq V_{CC}$ - 0.2V, $E_2 \leq 0.2V$, $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq 0.2V$	2.0	-	-	V
I_{CCDR}	Data Retention Current	$\bar{E}_1 \geq V_{CC}$ - 0.2V, $E_2 \leq 0.2V$, $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq 0.2V$	-	2	50	µA
t_{CDR}	Chip Deselect to Data Retention Time	See Retention Waveform	0	-	-	ns
t_R	Operation Recovery Time		t_{RC}(2)	-	-	ns

1. V_{CC} = 2V, T_A = +25°C
2. t_{RC} = Read Cycle Time

LOW V_{CC} DATA RETENTION WAVEFORM (1) ($\bar{E}_1$ Controlled)



LOW V_{CC} DATA RETENTION WAVEFORM (2) (E_2 Controlled)



AC TEST CONDITIONS

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Level	1.5V

AC TEST LOADS AND WAVEFORMS

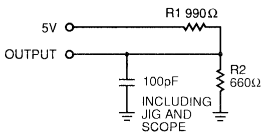


Figure 1a

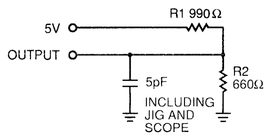
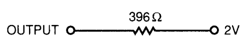


Figure 1b

Equivalent to:

THEVENIN EQUIVALENT



ALL INPUT PULSES

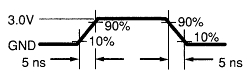
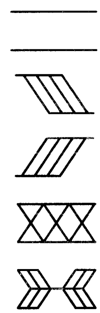


Figure 2

KEY TO SWITCHING WAVEFORMS



WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

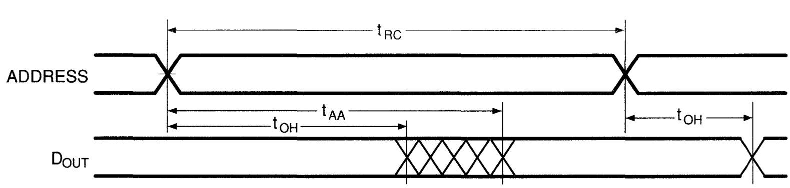
AC ELECTRICAL CHARACTERISTICS (over the operating range)

READ CYCLE

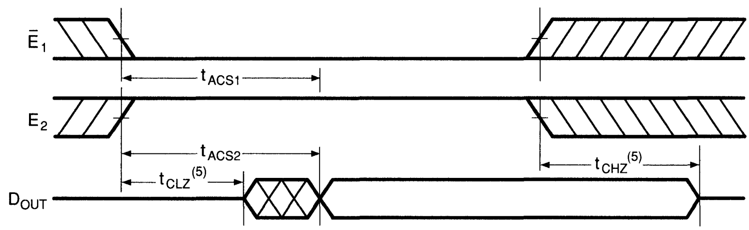
JEDEC PARAMETER NAME	PARAMETER NAME	PARAMETER		MS6264-70 MS6264L-70 MIN.	TYP.	MAX.	MS6264-10 MS6264L-10 MIN.	TYP.	MAX.	UNIT
t_{AVAX}	t_{RC}	Read Cycle Time		70	-	-	100	-	-	ns
t_{AVQV}	t_{AA}	Address Access Time		-	-	70	-	-	100	ns
t_{E1LQV}	t_{ACS1}	Chip Select Access Time	$\overline{E}_1$	-	-	70	-	-	100	ns
t_{E2HQV}	t_{ACS2}	Chip Select Access Time	E_2	-	-	70	-	-	100	ns
t_{GLQV}	t_{OE}	Output Enable to Output Valid		-	-	35	-	-	50	ns
t_{E1LQX}	t_{CLZ1}	Chip Select to Output Low Z	$\overline{E}_1$	5	-	-	5	-	-	ns
t_{E2HQX}	t_{CLZ2}	Chip Select to to Output Low Z	E_2	5	-	-	5	-	-	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z		5	-	-	5	-	-	ns
t_{E1HQZ}	t_{CHZ1}	Chip Deselect to Output in High Z	$\overline{E}_1$	0	-	35	0	-	35	ns
t_{E2HQZ}	t_{CHZ2}	Chip Deselect to Output in High Z	E_2	0	-	35	0	-	35	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z		0	-	30	0	-	35	ns
t_{AXQX}	t_{OH}	Output Hold from Address Change		5	-	-	5	-	-	ns

SWITCHING WAVEFORMS (READ CYCLE)

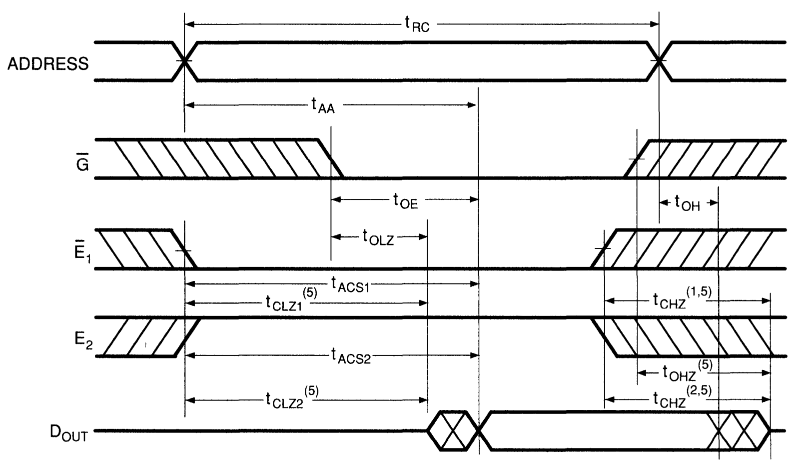
READ CYCLE 1$^{(1,2,4)}$



READ CYCLE 2(1,3,4)



READ CYCLE 3(1,4)



NOTES:
1. $\overline{W}$ is high for READ Cycle.
2. Device is continuously selected $\overline{E}_1 = V_{IL}$ and $E_2 = V_{IH}$.
3. Address valid prior to or coincident with $\overline{E}_1$ transition low and/or E_2 transition high.
4. $\overline{G} = V_{IL}$.
5. Transition is measured ± 500mV from steady state with C_L = 5pF as shown in Figure 1b. This parameter is guaranteed but not 100% tested.

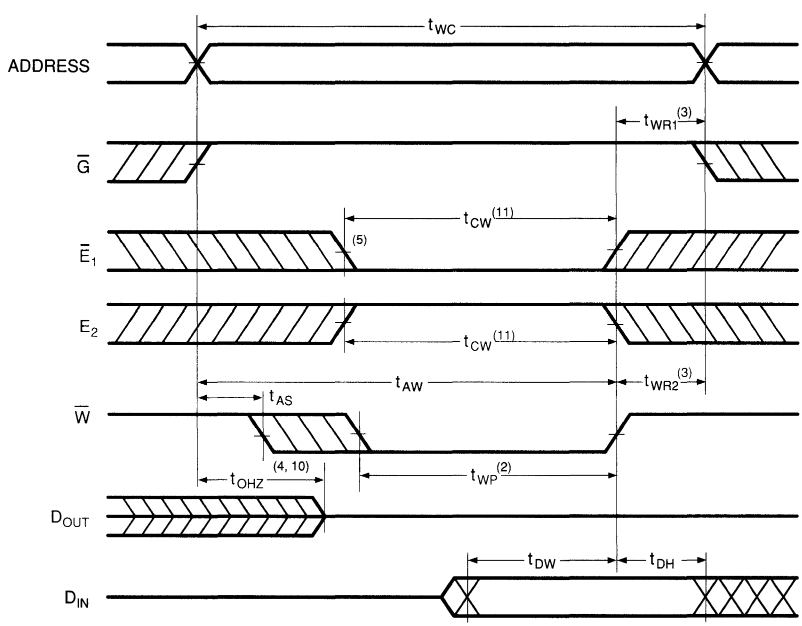
AC ELECTRICAL CHARACTERISTICS (over the operating range)

WRITE CYCLE

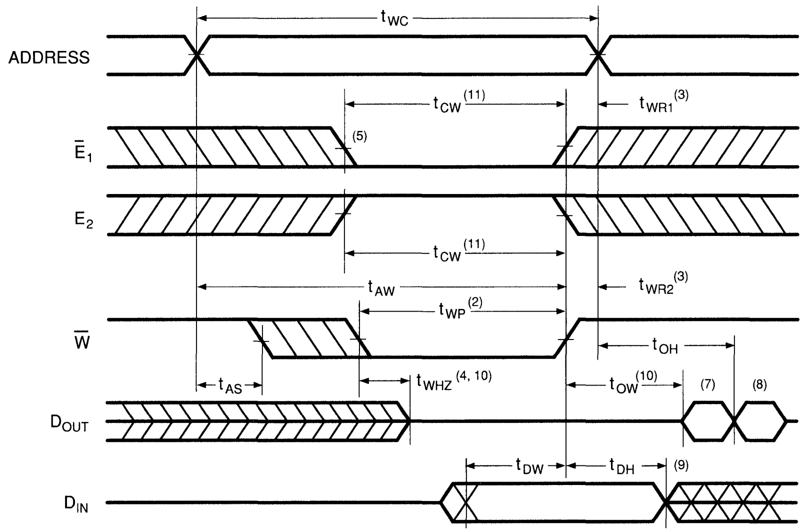
JEDEC PARAMETER NAME	PARAMETER NAME	PARAMETER		MS6264-70 MS6264L-70 MIN.	TYP.	MAX.	MS6264-10 MS6264L-10 MIN.	TYP.	MAX.	UNIT
t_{AVAX}	t_{WC}	Write Cycle Time		70	-	-	100	-	-	ns
t_{E1LWH}	t_{CW}	Chip Select to End of Write		45	-	-	80	-	-	ns
t_{AVWL}	t_{AS}	Address Set up Time		0	-	-	0	-	-	ns
t_{AVWH}	t_{AW}	Address Valid to End of Write		65	-	-	80	-	-	ns
t_{WLWH}	t_{WP}	Write Pulse Width		45	-	-	60	-	-	ns
t_{WHAX}	t_{WR1}	Write Recovery Time	$\overline{E}_1$, $\overline{W}$	5	-	-	5	-	-	ns
t_{E2LAX}	t_{WR2}	Write Recovery Time	E_2	5	-	-	5	-	-	ns
t_{WLQZ}	t_{WHZ}	Write to Output in High Z		0	-	30	-	-	35	ns
t_{DVWH}	t_{DW}	Data to Write Time Overlap		30	-	-	40	-	-	ns
t_{WHDX}	t_{DH}	Data Hold from Write Time		0	-	-	0	-	-	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z		0	-	30	0	-	35	ns
t_{WHQX}	t_{OW}	End of Write to Output Active		5	-	-	5	-	-	ns

SWITCHING WAVEFORMS (WRITE CYCLE)

WRITE CYCLE 1[1]



WRITE CYCLE 2[1,6]



NOTES:

1. $\overline{W}$ must be high during address transitions.
2. The internal write time of the memory is defined by the overlap of $\overline{E}_1$ and E_2 active and $\overline{W}$ low. All signals must be active to initiate a write and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
3. T_{WR} is measured from the earlier of $\overline{E}_1$ or $\overline{W}$ going high or E_2 going low at the end of write cycle.
4. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{E}_1$ low transition or the E_2 high transition occurs simultaneously with the $\overline{W}$ low transitions or after the $\overline{W}$ transition, outputs remain in a high impedance state.
6. $\overline{G}$ is continuously low ($\overline{G} = V_{IL}$).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\overline{E}_1$ is low and E_2 is high during this period, DQ pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured ±500mV from steady state with C_L = 5pF as shown in Figure 1b on page 4. This parameter is guaranteed but not 100% tested.
11. t_{CW} is measured from the later of $\overline{E}_1$ going low or E_2 going high to the end of write.

ORDERING INFORMATION

SPEED (ns)	ORDERING PART NUMBER	PACKAGE REFERENCE NO.	TEMPERATURE RANGE
70	MS6264-70PC	P28-1	0°C to +70°C
70	MS6264-70FC	S28-2	0°C to +70°C
70	MS6264L-70PC	P28-1	0°C to +70°C
70	MS6264L-70FC	S28-2	0°C to +70°C
100	MS6264-10PC	P28-1	0°C to +70°C
100	MS6264-10FC	S28-2	0°C to +70°C
100	MS6264L-10PC	P28-1	0°C to +70°C
100	MS6264L-10FC	S28-2	0°C to +70°C

8K x 8 High Speed CMOS Static RAM

FEATURES

- High speed – 45/55 ns (Max.)
- Automatic power-down when chip disabled
- Lower power consumption:
  - 550mW (Max.) Operating
  - 85mW (Max.) Standby
  - 550μW (Max.) Power-down
- TTL compatible interface levels
- Single 5V power supply
- Fully static operation
- Three state outputs
- Two chip enables ($\overline{E}_1$ and E_2) for simple memory expansion
- Data retention as low as 2V

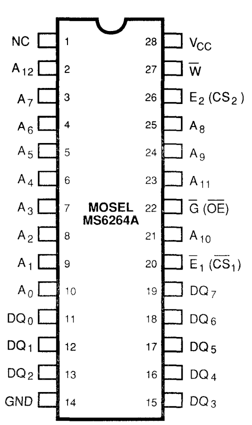
DESCRIPTION

The MOSEL MS6264A is a high performance, low power CMOS static RAM organized as 8192 words by 8 bits. The device supports easy memory expansion with both an active LOW chip enable ($\overline{E}_1$) and an active High chip enable (E_2), as well as an active LOW output enable ($\overline{G}$) and three-state outputs. An automatic power-down feature is included which reduces the chip power by 85% in TTL standby mode, and by over 99% in full power-down mode.

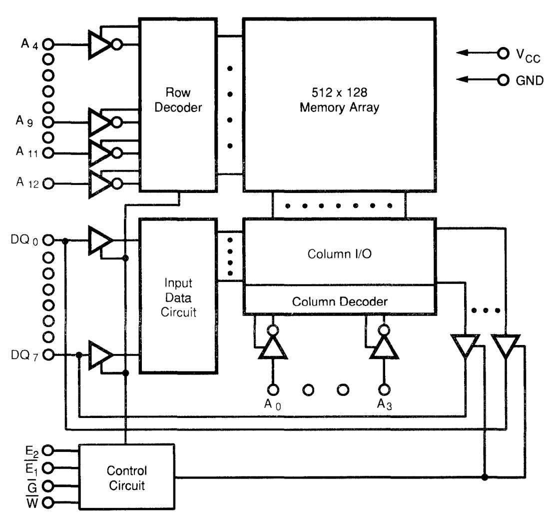
The device is manufactured in MOSEL's high performance CMOS process and operates from a single 5V power supply. All inputs and outputs are TTL compatible. Data is retained to as low as V_{CC} = 2V.

The MOSEL MS6264A is available in the JEDEC standard 28 pin 600 mil wide DIP, in the space saving 300 mil wide DIP, and in surface mount packages.

PIN CONFIGURATIONS



FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

A_0 - A_{12} Address Inputs

These 13 address inputs select one of the 8192 8-bit words in the RAM.

$\overline{E}_1$ Chip Enable 1 Input

E_2 Chip Enable 2 Input

$\overline{E}_1$ is active LOW and E_2 is active HIGH. Both chip enables must be active to read from or write to the device. If either chip enable is not active, the device is deselected and is in a standby power mode. The DQ pins will be in the high-impedance state when the device is deselected.

$\overline{G}$ Output Enable Input

The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when $\overline{G}$ is inactive.

$\overline{W}$ Write Enable Input

The write enable input is active LOW and controls read and write operations. With the chip selected, when $\overline{W}$ is HIGH and $\overline{G}$ is LOW, output data will be present at the DQ pins; when $\overline{W}$ is LOW, the data present on the DQ pins will be written into the selected memory location.

DQ_0 - DQ_7 Data Input/Output Ports

These 8 bidirectional ports are used to read data from or write data into the RAM.

V_{CC} Power Supply

GND Ground

TRUTH TABLE

MODE	$\overline{W}$	$\overline{E}_1$	E_2	$\overline{G}$	I/O OPERATION	V_{CC} CURRENT
Not Selected	X	H	X	X	High Z	I_{CCSB}, I_{CCSB1}
(Power Down)	X	X	L	X	High Z	I_{CCSB}, I_{CCSB1}
Output Disabled	H	L	H	H	High Z	I_{CC}
Read	H	L	H	L	D_{OUT}	I_{CC}
Write	L	L	H	X	D_{IN}	I_{CC}

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	PARAMETER	RATING	UNITS
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_{BIAS}	Temperature Under Bias	–0 to +125	°C
T_{STG}	Storage Temperature	–60 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	20	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

RANGE	AMBIENT TEMPERATURE	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

2

DC ELECTRICAL CHARACTERISTICS (over the operating range)

PARAMETER NAME	PARAMETER	TEST CONDITIONS	MS6264AL MIN.	TYP.[1]	MAX.	UNITS
V_{IL}	Guaranteed Input Low Voltage [2]		–0.5	-	0.8	V
V_{IH}	Guaranteed Input High Voltage[2]		2.0	-	6.0	V
I_{IL}	Input Leakage Current	V_{CC} = Max, V_{IN} = 0V to V_{CC}	-	-	2	µA
I_{OL}	Output Leakage Current	V_{CC} = Max, $\overline{E}_1 = V_{IH}$, or $E_2 = V_{IL}$, or $\overline{G} = V_{IH}$, V_{IN} = 0V t o V_{CC}	-	-	2	µA
V_{OL}	Output Low Voltage	V_{CC} = Min, I_{OL} = 8mA	-	-	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min, I_{OH} = –4mA	2.4	-	-	V
I_{CC}	Operating Power Supply Current	V_{CC} = Max, $\overline{E}_1 = V_{IL}$, $E_2 = V_{IH}$, I_{DQ} = 0mA, F = $F_{max}^{(3)}$	-	-	100	mA
I_{CCSB}	Standby Power Supply Current	V_{CC} = Max, $\overline{E}_1 = V_{IH}$, or $E_2 = V_{IL}$, I_{DQ} = 0mA	-	-	15	mA
I_{CCSB1}	Power Down Power Supply Current	V_{CC} = Max, $\overline{E}_1 > V_{CC} - 0.2V$, $E_2 < 0.2V$ $V_{IN} > V_{CC} - 0.2V$ or $V_{IN} < 0.2V$	-	-	100	µA

1. Typical characteristics are at V_{CC} = 5V, T_A = 25°C.
2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
3. $F_{MAX} = 1/t_{RC}$.

CAPACITANCE[1] (T_A = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{DQ}	Input/Output Capacitance	$V_{I/O}$ = 0V	8	pF

1. This parameter is guaranteed and not tested.

AC TEST CONDITIONS

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Level	1.5V

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

AC TEST LOADS AND WAVEFORMS

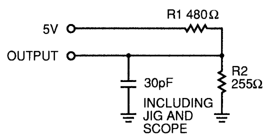


Figure 1a

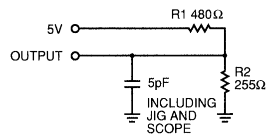
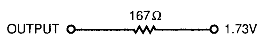


Figure 1b

Equivalent to:

THEVENIN EQUIVALENT



ALL INPUT PULSES

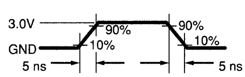


Figure 2

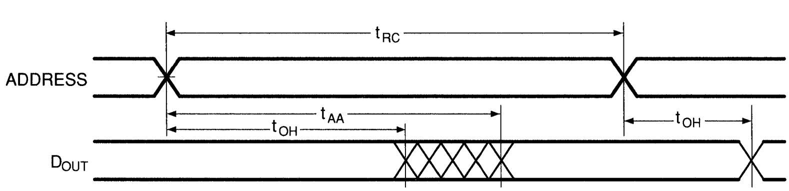
AC ELECTRICAL CHARACTERISTICS (over the operating range)

READ CYCLE

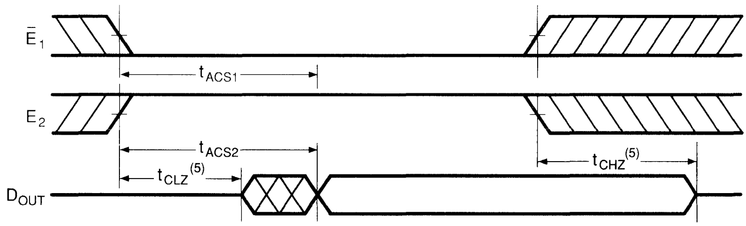
JEDEC PARAMETER NAME	PARAMETER NAME	PARAMETER		MS6264AL-45 MIN.	TYP.	MAX.	MS6264AL-55 MIN.	TYP.	MAX.	UNIT
t_{AVAX}	t_{RC}	Read Cycle Time		45	-	-	55	-	-	ns
t_{AVQV}	t_{AA}	Address Access Time		-	-	45	-	-	55	ns
t_{E1LQV}	t_{ACS1}	Chip Enable Access Time	$\overline{E}_1$	-	-	45	-	-	55	ns
t_{E2HQX}	t_{ACS2}	Chip Enable Access Time	E_2	-	-	45	-	-	55	ns
t_{GLQV}	t_{OE}	Output Enable to Output Valid		-	-	20	-	-	25	ns
t_{E1LQX}	t_{CLZ1}	Chip Enable to Output Low Z	$\overline{E}_1$	5	-	-	5	-	-	ns
t_{E2HQX}	t_{CLZ2}	Chip Enable to to Output Low Z	E_2	5	-	-	5	-	-	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z		5	-	-	5	-	-	ns
t_{E1HQZ}	t_{CHZ1}	Chip Disable to Output in High Z	$\overline{E}_1$	0	-	20	0	-	20	ns
t_{E2LQZ}	t_{CHZ2}	Chip Disable to Output in High Z	E_2	0	-	20	0	-	20	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z		0	-	20	0	-	20	ns
t_{AXQX}	t_{OH}	Output Hold from Address Change		5	-	-	5	-	-	ns

SWITCHING WAVEFORMS (READ CYCLE)

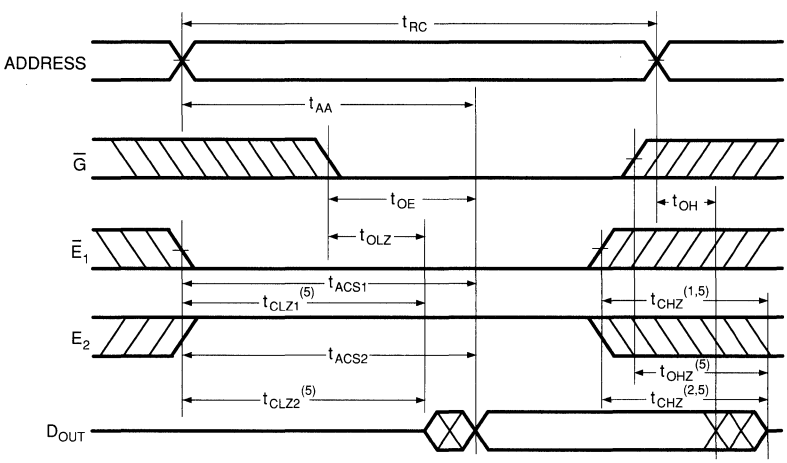
READ CYCLE 1(1,2,4)



READ CYCLE 2(1,3,4)



READ CYCLE 3(1,4)



NOTES:
1. $\overline{W}$ is high for READ Cycle.
2. Device is continuously selected $\overline{E}_1 = V_{IL}$ and $E_2 = V_{IH}$.
3. Address valid prior to or coincident with $\overline{E}_1$ transition low and/or E_2 transition high.
4. $\overline{G} = V_{IL}$.
5. Transition is measured ± 500mV from steady state with C_L = 5pF as shown in Figure 1b. This parameter is guaranteed but not 100% tested.

2

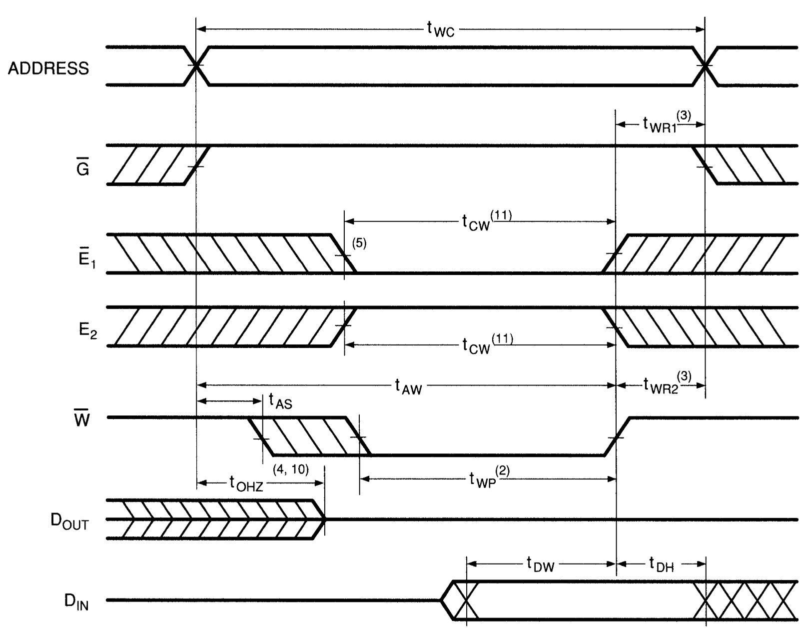
AC ELECTRICAL CHARACTERISTICS (over the operating range)

WRITE CYCLE

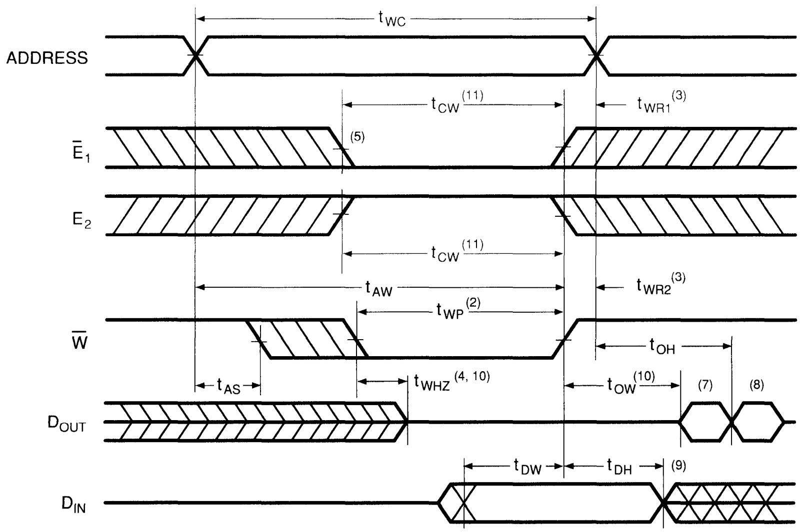
JEDEC PARAMETER NAME	PARAMETER NAME	PARAMETER		MS6264AL-45 MIN.	TYP.	MAX.	MS6264AL-55 MIN.	TYP.	MAX.	UNIT
t_{AVAX}	t_{WC}	Write Cycle Time		45	-	-	55	-	-	ns
t_{E1LWH}	t_{CW}	Chip Enable to End of Write		35	-	-	40	-	-	ns
t_{AVWL}	t_{AS}	Address Set up Time		0	-	-	0	-	-	ns
t_{AVWH}	t_{AW}	Address Valid to End of Write		35	-	-	50	-	-	ns
t_{WLWH}	t_{WP}	Write Pulse Width		30	-	-	35	-	-	ns
t_{WHAX}	t_{WR1}	Write Recovery Time	$\overline{E}_1,\overline{W}$	0	-	-	3	-	-	ns
t_{E2LAX}	t_{WR2}	Write Recovery Time	E_2	0	-	-	3	-	-	ns
t_{WLQZ}	t_{WHZ}	Write to Output in High Z		0	-	20	0	-	20	ns
t_{DVWH}	t_{DW}	Data to Write Time Overlap		20	-	-	25	-	-	ns
t_{WHDX}	t_{DH}	Data Hold from Write Time		0	-	-	0	-	-	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z		0	-	20	0	-	25	ns
t_{WHQX}	t_{OW}	Output Active from End of Write		5	-	-	5	-	-	ns

SWITCHING WAVEFORMS (WRITE CYCLE)

WRITE CYCLE 1(1)



WRITE CYCLE 2(1,6)



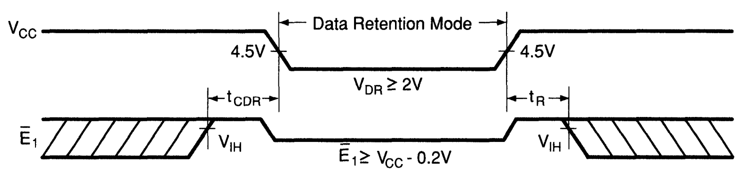
NOTES:
1. $\overline{W}$ must be high during address transitions.
2. The internal write time of the memory is defined by the overlap of $\overline{E}_1$ and E_2 active and $\overline{W}$ low. All signals must be active to initiate a write and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
3. T_{WR} is measured from the earlier of $\overline{E}_1$ or $\overline{W}$ going high or E_2 going low at the end of write cycle.
4. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{E}_1$ low transition or the E_2 high transition occurs simultaneously with the $\overline{W}$ low transitions or after the $\overline{W}$ transition, outputs remain in a high impedance state.
6. $\overline{G}$ is continuously low ($\overline{G} = V_{IL}$).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\overline{E}_1$ is low and E_2 is high during this period, DQ pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured ±500mV from steady state with C_L = 5pF as shown in Figure 1b on page 4. This parameter is guaranteed but not 100% tested.
11. t_{CW} is measured from the later of $\overline{E}_1$ going low or E_2 going high to the end of write.

DATA RETENTION CHARACTERISTICS (T_A = 0 to +70°C)

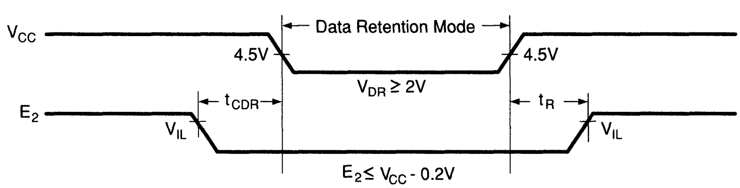
SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.(1)	MAX.	UNITS
V_{DR}	V_{CC} for Data Retention	$\overline{E}_1 \geq V_{CC} - 0.2V$, $E_2 \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	2.0	-	-	V
I_{CCDR}	Data Retention Current	$\overline{E}_1 \geq V_{CC} - 0.2V$, $E_2 \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	-	2	50	µA
I_{IL}	Input Leakage Current		-	-	2	µA
t_{CDR}	Chip Deselect to Data Retention Time	See Retention Waveform	0	-	-	ns
t_R	Operation Recovery Time	See Retention Waveform	t_{RC}(2)	-	-	ns

1. V_{CC} = 2V, T_A = +25°C
2. t_{RC} = Read Cycle Time

LOW V_{CC} DATA RETENTION WAVEFORM (1) ($\overline{E}_1$ Controlled)



LOW V_{CC} DATA RETENTION WAVEFORM (2) (E_2 Controlled)



ORDERING INFORMATION

SPEED (ns)	ORDERING PART NUMBER	PACKAGE REFERENCE NO.	TEMPERATURE RANGE
45	MS6264AL-45NC	P28-2	0°C to +70°C
45	MS6264AL-45PC	P28-1	0°C to +70°C
45	MS6264AL-45SC	S28-1	0°C to +70°C
55	MS6264AL-55NC	P28-2	0°C to +70°C
55	MS6264AL-55PC	P28-1	0°C to +70°C
55	MS6264AL-55SC	S28-1	0°C to +70°C

8K x 8 Low Power CMOS SRAM

FEATURES

- Available in 80/100/150 ns (Max.)
- Automatic power-down when chip disabled
- Lower power consumption:

  MS6264C
  - 1mA (Max.) Data Retention Current
  - 11mW (Max.) Standby

  MS6264CL
  - 25µA (Max.) Data Retention Current
  - 0.55mW (Max.) Standby

  MS6264CLL
  - 2µA (Max.) Data Retention Current
  - 0.55mW (Max.) Standby
- TTL compatible interface levels
- Single 5V power supply
- Fully static operation, no clock required
- Three state outputs
- Two chip enable ($\overline{E}_1$ and E_2) for simple memory expansion
- Data retention as low as 2V

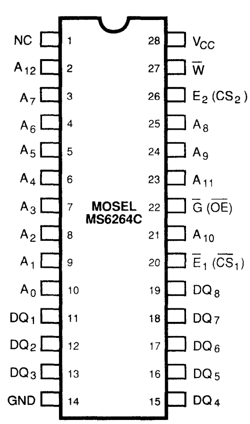
DESCRIPTION

The MOSEL MS6264C is a high performance, low power CMOS static RAM organized as 8192 words by 8 bits. The device supports easy memory expansion with both an active LOW chip enable ($\overline{E}_1$) and an active High chip enable (E_2), as well as an active LOW output enable ($\overline{G}$) and tri-state outputs. An automatic power-down feature is included which reduces the chip power by 80% in TTL standby mode, and by over 95% in full power-down mode.

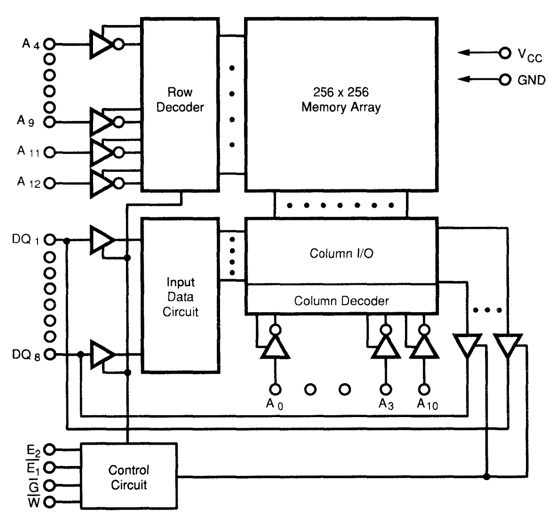
The device is manufactured in MOSEL's high performance CMOS process and operates from a single 5V power supply. All inputs and outputs are TTL compatible. Data is retained to as low as V_{CC} = 2V.

The MOSEL MS6264C is packaged in the JEDEC standard 28 pin 600 mil wide DIP, 330 mil wide SOP and 28 pin 300 mil thin DIP.

PIN CONFIGURATIONS



FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

A_0 - A_{12} Address Inputs

These 13 address inputs select one of the 8192 8-bit words in the RAM.

$\overline{E}_1$ Chip Enable 1 Input

E_2 Chip Enable 2 Input

$\overline{E}_1$ is active LOW and E_2 is active HIGH. Both chip enables must be active to read from or write to the device. If either chip enable is not active, the device is deselected and is in a standby power mode. The DQ pins will be in the high-impedance state when the device is deselected.

$\overline{G}$ Output Enable Input

The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when $\overline{G}$ is inactive.

$\overline{W}$ Write Enable Input

The write enable input is active LOW and controls read and write operations. With the chip selected, when $\overline{W}$ is HIGH and $\overline{G}$ is LOW, output data will be present at the DQ pins; when $\overline{W}$ is LOW, the data present on the DQ pins will be written into the selected memory location.

DQ_1 - DQ_8 Data Input/Output Ports

These 8 bidirectional ports are used to read data from or write data into the RAM.

V_{CC} Power Supply

GND Ground

TRUTH TABLE

MODE	$\overline{W}$	$\overline{E}_1$	E_2	$\overline{G}$	I/O OPERATION	V_{CC} CURRENT
Not Selected	X	H	X	X	High Z	I_{CCSB}, I_{CCSB1}
(Power Down)	X	X	L	X	High Z	I_{CCSB}, I_{CCSB1}
Output Disabled	H	L	H	H	High Z	I_{CC}
Read	H	L	H	L	D_{OUT}	I_{CC}
Write	L	L	H	X	D_{IN}	I_{CC}

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	PARAMETER	RATING	UNITS
V_{TERM}	Terminal Voltage with Respect to GND	−0.5 to +7.0	V
T_{BIAS}	Temperature Under Bias	−10 to +85	°C
T_{STG}	Storage Temperature	−60 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	20	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

CAPACITANCE(1) (T_A = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{DQ}	Input/Output Capacitance	$V_{I/O}$ = 0V	8	pF

1. This parameter is guaranteed and not tested.

DC ELECTRICAL CHARACTERISTICS (over the operating range)

PARAMETER NAME	PARAMETER	TEST CONDITIONS	MS6264C-80/10/15 MIN.		MAX.	MS6264CL/LL-80/10/15 MIN.		MAX.	UNITS
V_{IL}	Guaranteed Input Low Voltage(2)		–2.0	-	+0.8	–2.0	-	+0.8	V
V_{IH}	Guaranteed Input High Voltage(2)		2.2		V_{CC}+ 0.3	2.2	-	V_{CC}+ 0.3	V
I_{IL}	Input Leakage Current	V_{CC} = Max, V_{IN} = 0V to V_{CC}	–1	-	2	–1	-	2	µA
I_{OL}	Output Leakage Current	V_{CC} = Max, $\overline{E}_1 = V_{IH}$, or $E_2 = V_{IL}$, or $\overline{G} = V_{IH}$, V_{IN} = 0V t o V_{CC}	–2	-	2	–2	-	2	µA
V_{OL}	Output Low Voltage	V_{CC} = Min, I_{OL} = 4mA	-	-	0.4	-	-	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min, I_{OH} = -1mA	2.4	-	-	2.4	-	-	V
I_{CC}	Operating Power Supply Current	V_{CC} = Max, $\overline{E}_1 = V_{IL}$, $E_2 = V_{IH}$, I_{DQ} = 0mA, $F = F_{max}$(3)	-	-	60	-	-	60	mA
I_{CCSB}	Standby Power Supply Current	V_{CC} = Max, $\overline{E}_1 = V_{IH}$, or $E_2 = V_{IL}$, I_{DQ} = 0mA	-	-	2	-	0.001	0.1	mA
I_{CCSB1}	Power Down Power Supply Current	V_{CC} = Max, $\overline{E}_1 > V_{CC}$ - 0.2V, E_2 < 0.2V $V_{IN} > V_{CC}$ - 0.2V or V_{IN} < 0.2V	-	-	3	-	-	3	mA

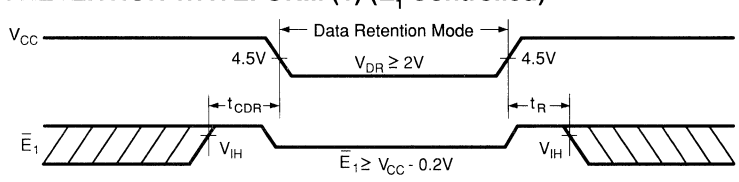
1. Typical characteristics are at V_{cc} = 5V, T_A = 25°C.
2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
3. –2.0V Min. for pulse width less than 20 ns. (V_{IL} Min. = –0.3V at DC level)
4. $F_{MAX} = 1/t_{RC}$.

DATA RETENTION CHARACTERISTICS (T_A = 0 to +70°C)

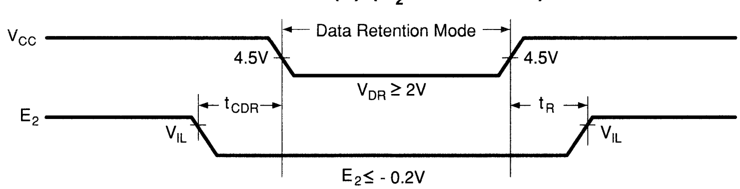
SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.(1)	MAX.	UNITS
V_{DR}	V_{CC} for Data Retention	$\overline{E}_1 \geq V_{CC}$ - 0.2V, $E_2 \leq$ 0.2V, $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V		2.0	-	5.5	V
I_{CCDR}	Data Retention Current	$\overline{E}_1 \geq V_{CC}$ - 0.2V, $E_2 \leq$ 0.2V, $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V	Standard	-	-	1.0	mA
			L-Version	-	1.0	2.5	µA
			LL-Version (3)	-	1.0	2.0	µA
t_{CDR}	Chip Deselect to Data Retention Time	See Retention Waveform		0	-	-	ns
t_R	Operation Recovery Time			t_{RC}(2)	-	-	ns

1. V_{cc} = 2V, T_A = +25°C
2. t_{RC} = Read Cycle Time
3. V_{DR} = 3.0V, T_A = 0°C to 40°C

LOW V_{CC} DATA RETENTION WAVEFORM (1) ($\overline{E}_1$ Controlled)



LOW V_{CC} DATA RETENTION WAVEFORM (2) (E_2 Controlled)

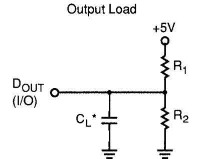


AC TEST LOADS AND WAVEFORMS

- Input Pulse Levels: 0.6V to 2.4V
- Input Pulse Rise and Fall Times: 5ns (Transient Time between 0.8V and 2.2V)
- Timing Reference Levels: Input: V_{IL} = 0.8V, V_{IH} = 2.2V; Output: V_{OL} = 0.8V, V_{OH} = 2.0V
- Output Load:

	R_1	R_2	C_L	Parameter Measured
Load I	1.8KΩ	990Ω	100pF	except t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WLZ}, and t_{WHZ}
Load II	1.8KΩ	990Ω	5pF	t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WLZ}, and t_{WHZ}

Output Load



*Including Jig and Stray Capacitance

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

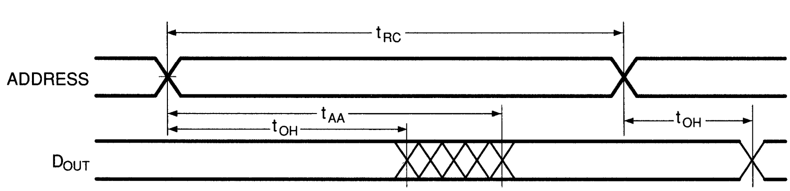
AC ELECTRICAL CHARACTERISTICS (over the operating range)

READ CYCLE

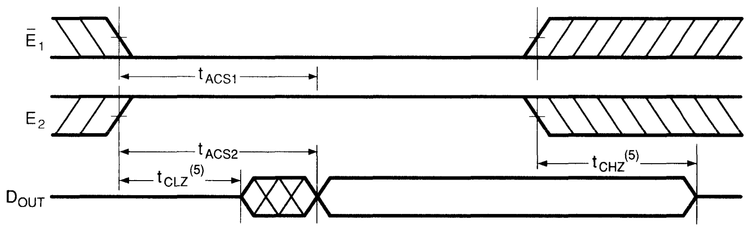
JEDEC PARAMETER NAME	PARAMETER NAME	PARAMETER		MS6264C-80 MS6264CL-80 MS6264CLL-80 MIN.	TYP.	MAX.	MS6264C-10 MS6264CL-10 MS6264CLL-10 MIN.	TYP.	MAX.	MS6264C-15 MS6264CL-15 MS6264CLL-15 MIN.	TYP.	MAX.	UNIT
t_{AVAX}	t_{RC}	Read Cycle Time		80	-	-	100	-	-	150	-	-	ns
t_{AVQV}	t_{AA}	Address Access Time		-	-	80	-	-	100	-	-	150	ns
t_{E1LQV}	t_{ACS1}	Chip Select Access Time	$\bar{E}_1$	-	-	80	-	-	100	-	-	150	ns
t_{E2HQV}	t_{ACS2}	Chip Select Access Time	E_2	-	-	80	-	-	100	-	-	150	ns
t_{GLQV}	t_{OE}	Output Enable to Output Valid		-	-	35	-	-	45	-	-	55	ns
t_{E1LQX}	t_{CLZ1}	Chip Select to Output Low Z	$\bar{E}_1$	10	-	-	10	-	-	10	-	-	ns
t_{E2HQX}	t_{CLZ2}	Chip Select to to Output Low Z	E_2	10	-	-	10	-	-	10	-	-	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z		5	-	-	5	-	-	5	-	-	ns
t_{E1HQZ}	t_{CHZ1}	Chip Deselect to Output in High Z	$\bar{E}_1$	-	-	35	-	-	35	-	-	40	ns
t_{E2HQZ}	t_{CHZ2}	Chip Deselect to Output in High Z	E_2	-	-	35	-	-	35	-	-	40	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z		-	-	30	-	-	35	-	-	40	ns
t_{AXQX}	t_{OH}	Output Hold from Address Change		10	-	-	10	-	-	10	-	-	ns

SWITCHING WAVEFORMS (READ CYCLE)

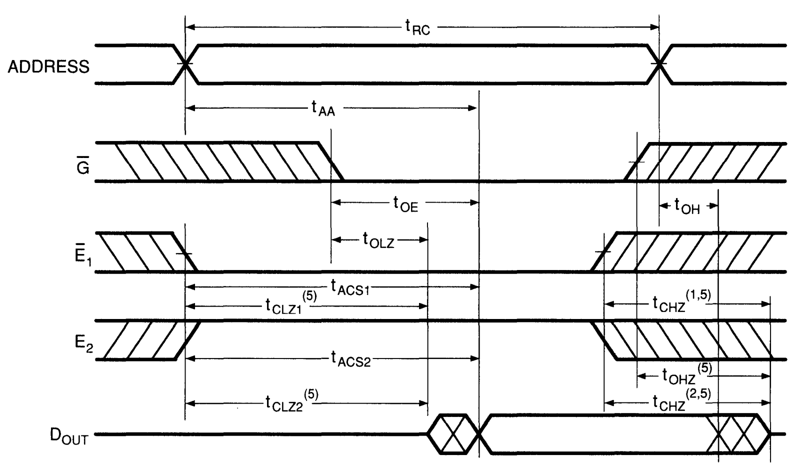
READ CYCLE 1(1,2,4)



READ CYCLE 2(1,3,4)



READ CYCLE 3(1,4)



NOTES:
1. $\overline{W}$ is high for READ Cycle.
2. Device is continuously selected $\overline{E}_1 = V_{IL}$ and $E_2 = V_{IH}$.
3. Address valid prior to or coincident with $\overline{E}_1$ transition low and/or E_2 transition high.
4. $\overline{G} = V_{IL}$.
5. Transition is measured ± 500mV from steady state with C_L = 5pF as shown in Figure 1b. This parameter is guaranteed but not 100% tested.

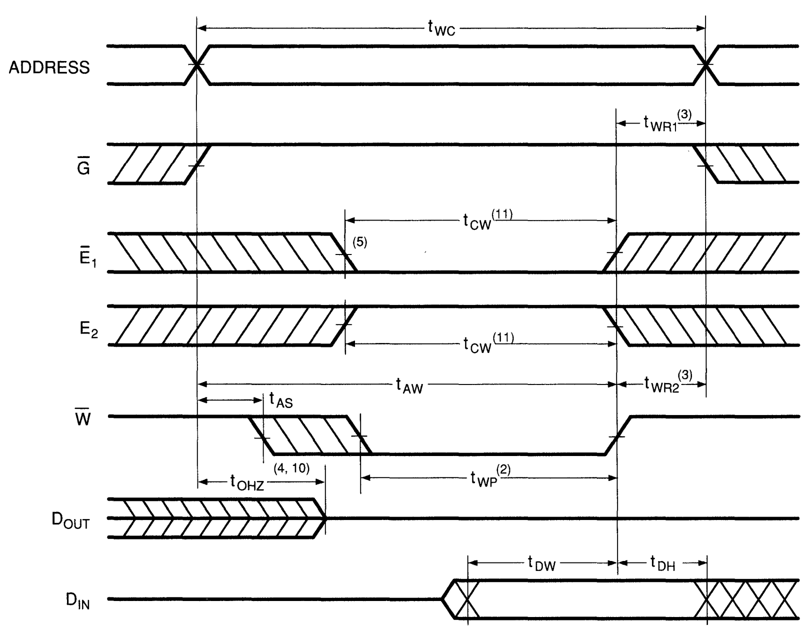
AC ELECTRICAL CHARACTERISTICS (over the operating range)

WRITE CYCLE

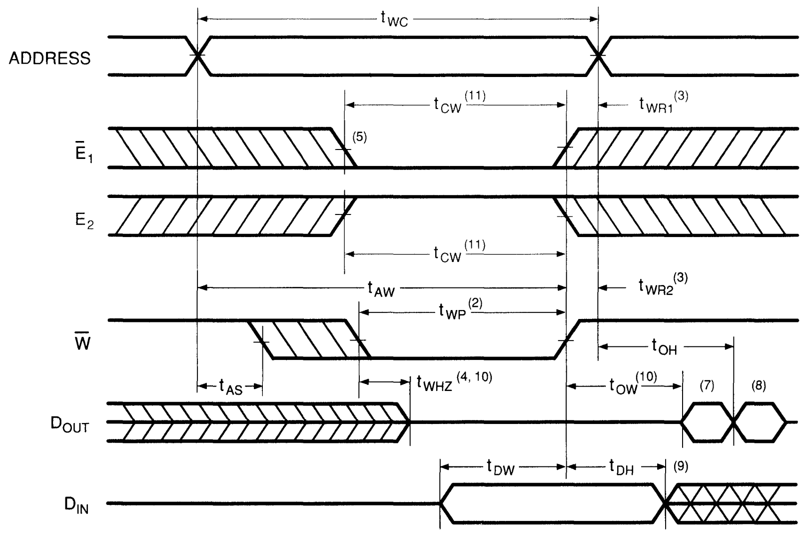
JEDEC PARAMETER NAME	PARAMETER NAME	PARAMETER	MS6264C-80 MS6264CL-80 MS6264CLL-80 MIN.	TYP.	MAX.	MS6264C-10 MS6264CL-10 MS6264CLL-10 MIN.	TYP.	MAX.	MS6264C-15 MS6264CL-15 MS6264CLL-15 MIN.	TYP.	MAX.	UNIT
t_{AVAX}	t_{WC}	Write Cycle Time	80	-	-	100	-	-	150	-	-	ns
t_{E1LWH}	t_{CW}	Chip Select to End of Write	60	-	-	80	-	-	100	-	-	ns
t_{AVWL}	t_{AS}	Address Set up Time	0	-	-	0	-	-	0	-	-	ns
t_{AVWH}	t_{AW}	Address Valid to End of Write	60	-	-	80	-	-	100	-	-	ns
t_{WLWH}	t_{WP}	Write Pulse Width	60	-	-	70	-	-	90	-	-	ns
t_{WHAX}	t_{WR1}	Write Recovery Time $\overline{E}_1,\overline{W}$	10	-	-	10	-	-	10	-	-	ns
t_{E2LAX}	t_{WR2}	Write Recovery Time E_2	10	-	-	10	-	-	10	-	-	ns
t_{WLQZ}	t_{WHZ}	Write to Output in High Z	-	-	30	-	-	35	-	-	40	ns
t_{DVWH}	t_{DW}	Data to Write Time Overlap	30	-	-	35	-	-	40	-	-	ns
t_{WHDX}	t_{DH}	Data Hold from Write Time	5	-	-	5	-	-	5	-	-	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z										ns
t_{WHQX}	t_{OW}	End of Write to Output Active										ns

SWITCHING WAVEFORMS (WRITE CYCLE)

WRITE CYCLE 1[1]



WRITE CYCLE 2(1,6)



NOTES:
1. $\overline{W}$ must be high during address transitions.
2. The internal write time of the memory is defined by the overlap of $\overline{E}_1$ and E_2 active and $\overline{W}$ low. All signals must be active to initiate a write and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
3. T_{WR} is measured from the earlier of $\overline{E}_1$ or $\overline{W}$ going high or E_2 going low at the end of write cycle.
4. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{E}_1$ low transition or the E_2 high transition occurs simultaneously with the $\overline{W}$ low transitions or after the $\overline{W}$ transition, outputs remain in a high impedance state.
6. $\overline{G}$ is continuously low ($\overline{G} = V_{IL}$).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\overline{E}_1$ is low and E_2 is high during this period, DQ pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured ±500mV from steady state with C_L = 5pF as shown in Figure 1b on page 4. This parameter is guaranteed but not 100% tested.
11. t_{CW} is measured from the later of $\overline{E}_1$ going low or E_2 going high to the end of write.

ORDERING INFORMATION

SPEED (ns)	ORDERING PART NUMBER	PACKAGE REFERENCE NO.	TEMPERATURE RANGE
80	MS6264C-80PC	P28-4	0°C to +70°C
80	MS6264C-80NC	P28-5	0°C to +70°C
80	MS6264C-80FC	S28-5	0°C to +70°C
100	MS6264C-10PC	P28-4	0°C to +70°C
100	MS6264C-10NC	P28-5	0°C to +70°C
100	MS6264C-10FC	S28-5	0°C to +70°C
150	MS6264C-15PC	P28-4	0°C to +70°C
150	MS6264C-15NC	P28-5	0°C to +70°C
150	MS6264C-15FC	S28-5	0°C to +70°C

Note 1: For the low power part number, add "L" after the "B" and before the "-". Example MS6264BL-80PC.
Note 2: For the low/low power part number, add "LL" after the "B" and before the "-". Example MS6264BLL-80PC.

MOSEL MS62256

32K x 8 CMOS Static RAM

FEATURES

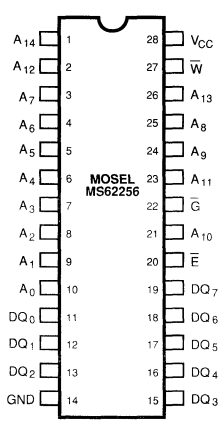
- High-speed – 70/85/100 ns
- Low Power dissipation:
  MS62256L
    225mW (Typ.) Operating
    30μW (Typ.) Standby
- Fully static operation
- All inputs and outputs directly TTL compatible
- Three state outputs
- Ultra low data retention supply current at V_{CC} = 2V

DESCRIPTION

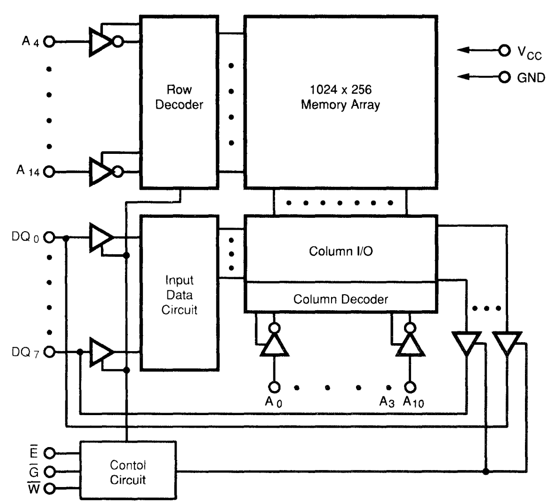
The MOSEL MS62256 is a 262,144-bit static random access memory organized as 32,768 words by 8 bits and operates from a single 5 volt supply. It is built with MOSEL's high performance twin tub CMOS process. Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures. The MS62256 is available in a standard 28-pin 600 mil plastic DIP package and 330 mil SOP.

2

PIN CONFIGURATIONS



FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

A_0 - A_{14} Address Inputs

These 15 address inputs select one of the 32768 8-bit words in the RAM.

$\overline{E}$ Chip Enable Input

$\overline{E}$ is active LOW. The chip enable must be active to read from or write to the device. If it is not active, the device is deselected and is in a standby power mode. The DQ pins will be in the high-impedance state when deselected.

$\overline{G}$ Output Enable Input

The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when $\overline{G}$ is inactive.

$\overline{W}$ Write Enable Input

The write enable input is active LOW and controls read and write operations. With the chip enabled, when $\overline{W}$ is HIGH and $\overline{G}$ is LOW, output data will be present at the DQ pins; when $\overline{W}$ is LOW, the data present on the DQ pins will be written into the selected memory location.

DQ_0 - DQ_7 Data Input/Output Ports

These 8 bidirectional ports are used to read data from or write data into the RAM.

V_{CC} Power Supply

GND Ground

TRUTH TABLE

MODE	$\overline{W}$	$\overline{E}$	$\overline{G}$	I/O OPERATION
Standby	H	X	X	High Z
Read	L	L	H	D_{OUT}
Read	L	H	H	High Z
Write	L	X	L	D_{IN}

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	PARAMETER		RATING	UNITS
V_{CC}	Supply Voltage		-0.3 to 7	V
V_{IN}	Input Voltage		-0.3 to 7	V
V_{DQ}	Input/Output Voltage Applied		-0.3 to 6	V
T_{BIAS}	Temperature Under Bias	Plastic	-10 to +125	°C
T_{STG}	Storage Temperature	Plastic	-40 to +150	°C
P_D	Power Dissipation		1.0	W
I_{OUT}	DC Output Current		50	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

OPERATING RANGE

RANGE	AMBIENT TEMPERATURE	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

2

DC ELECTRICAL CHARACTERISTICS (over the commercial operating range)

PARAMETER NAME	PARAMETER	TEST CONDITIONS		-70, -85 MIN.	TYP.(1)	MAX.	-10 MIN.	TYP.(1)	MAX.	UNITS
V_{IL}	Guaranteed Input Low Voltage(2)(3)			-0.3	-	+0.8	-0.3	-	+0.8	V
V_{IH}	Guaranteed Input High Voltage(2)			2.2	-	6.0	2.2	-	6.0	V
I_{IL}	Input Leakage Current	V_{CC} = Max, V_{IN} = 0V to V_{CC}		-	-	2	-	-	2	μA
I_{OL}	Output Leakage Current	V_{CC} = Max, $\overline{E}$ = V_{IH}, or $\overline{G}$ = V_{IH}, V_{IN} = 0V to V_{CC}		-	-	2	-	-	2	μA
V_{OL}	Output Low Voltage	V_{CC} = Min, I_{OL} = 4mA		-	-	0.4	-	-	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min, I_{OH} = -1mA		2.4	3.5	-	2.4	3.5	-	V
I_{CC}	Operating Power Supply Current	V_{CC} = Max, $\overline{E}$ = V_{IL}, $I_{I/O}$ = 0mA, F_{max}(4)		-	-	85	-	-	70	mA
I_{CCSB}	Standby Power Supply Current	V_{CC} = Max, $\overline{E}$ = V_{IH}, $I_{I/O}$ = 0mA		-	-	3	-	-	3	mA
I_{CCSB1}	Power Down Power Supply Current	V_{CC} = Max, $\overline{E}$ > V_{CC} - 0.2V	MS62256L	-	-	0.1	-	-	0.1	mA
		V_{IN} > V_{CC} - 0.2V or V_{IN} < 0.2V	MS62256	-	-	1	-	-	1	mA

1. Typical characteristics are at V_{CC} = 5V, T_A = 25°C.
2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
3. V_{IL} (Min.) = –3.0V for pulse width ≤ 20ns
3. $F_{MAX} = 1/t_{RC}$.

CAPACITANCE(1) (T_A = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$ = 0V	10	pF

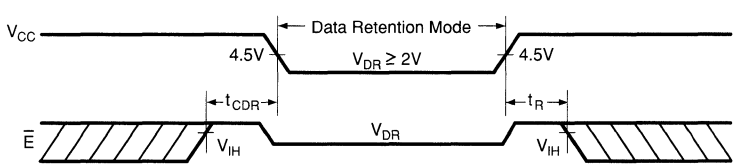
1. This parameter is guaranteed and not tested.

DATA RETENTION CHARACTERISTICS (over the commercial operating range)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.(2)	MAX(3)	UNITS
V_{DR}	V_{CC} for Data Retention	$\overline{E}$ ≥ V_{CC}-0.2V, $\overline{G}$ ≥ V_{CC} -0.2V, V_{IN} ≥ V_{CC}-0.2V or V_{IN} ≤ 0.2V	2.0	-	-	V
I_{CCDR}	Data Retention Current	$\overline{E}_1$ ≥ V_{CC}-0.2V, $\overline{G}$ ≥ V_{CC} -0.2V, V_{IN} ≥ V_{CC}-0.2V or V_{IN} ≤ 0.2V	-	2	50	μA
t_{CDR}	Chip Deselect to Data Retention Time	See Retention Waveform	0	-	-	ns
t_R	Operation Recovery Time		t_{RC}(4)	-	-	ns

1. Applies to L verion only
2. V_{CC} = 2V, T_A = +25°C
3. V_{CC} = 3V
4. t_{RC} = Read Cycle Time

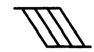
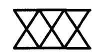
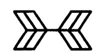
TIMING WAVEFORM LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5ns
Timing Reference Level	1.5V

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

AC TEST LOADS AND WAVEFORMS

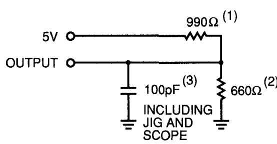


Figure 1a

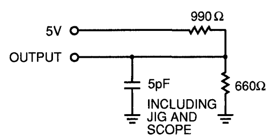
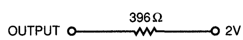


Figure 1b

Equivalent to:

THEVENIN EQUIVALENT



ALL INPUT PULSES

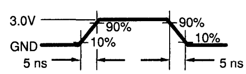


Figure 2

1. For 100 ns version, 1000Ω
2. For 100 ns version, 670Ω
3. For 100 ns version, 100pF

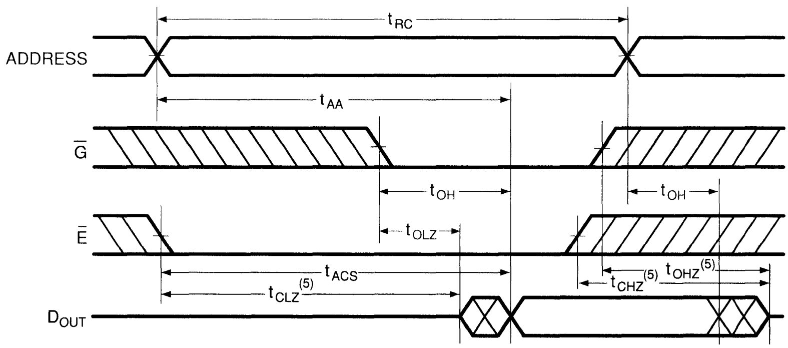
AC ELECTRICAL CHARACTERISTICS (over the commercial operating range)

READ CYCLE

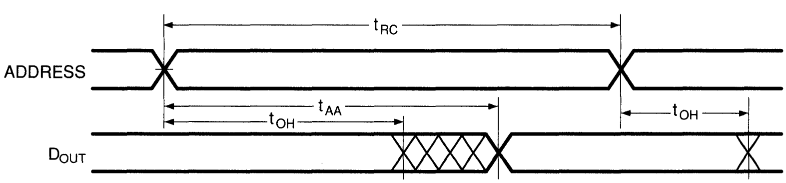
JEDEC PARAMETER NAME	PARAMETER NAME	PARAMETER	MS62256L-70 MIN.	TYP.	MAX.	MS82256L-85 MIN.	TYP.	MAX.	MS82256L-10 MIN.	TYP.	MAX.	UNIT
t_{AVAX}	t_{RC}	Read Cycle Time	70		-	85		-	100		-	ns
t_{AVQV}	t_{AA}	Address Access Time	-		70	-		85	-		100	ns
t_{ELQV}	t_{ACS}	Chip Enable Access Time	-		70	-		85	-		100	ns
t_{GLQX}	t_{OE}	Output Enable to Output Valid	-		35	-		40	-		50	ns
t_{EHQZ}	t_{CLZ}	Chip Enable to Output Low Z	5		-	5		-	10		-	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z	5		-	5		-	10		-	ns
t_{EHQZ}	t_{CHZ}	Chip Disable to Output in High Z	0		30	0		35	0		35	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z	0		30	0		35	0		35	ns
t_{AXQX}	t_{OH}	Output Hold from Address Change	10		-	10		-	10		-	ns

SWITCHING WAVEFORMS (READ CYCLE)

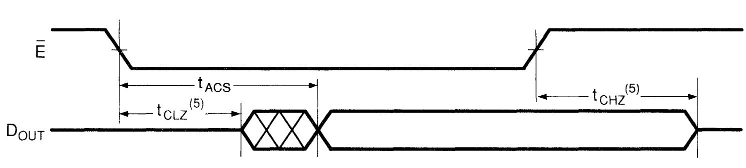
READ CYCLE 1(1)



READ CYCLE 2(1, 2, 4)



READ CYCLE 3(1, 3, 4)



NOTES:
1. $\overline{W}$ is High for READ Cycle.
2. Device is continuously selected $\overline{E} = V_{IL}$.
3. Address valid prior to or coincident with $\overline{E}$ transition low.
4. $\overline{G} = V_{IL}$.
5. Transition is measured ± 500mV from steady state with C_L = 5pF as shown in Figure 1b on page 4. This parameter is guaranteed and not 100% tested.

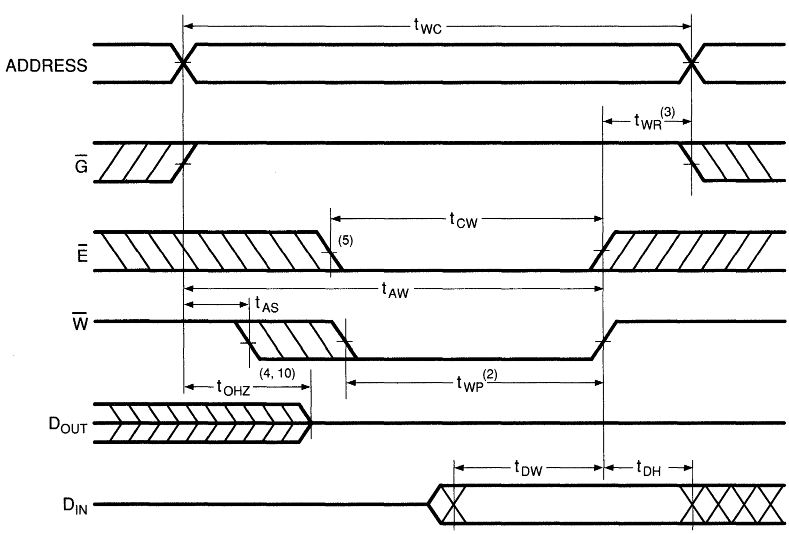
AC ELECTRICAL CHARACTERISTICS (over the commercial operating range)

WRITE CYCLE

JEDEC PARAMETER NAME	PARAMETER NAME	PARAMETER	MS62256L-70			MS82256L-85			MS82256L-10			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
t_{AVAX}	t_{WC}	Write Cycle Time	70	-	-	85	-	-	100	-	-	ns
t_{ELWH}	t_{CW}	Chip Enable to End of Write	45	-	-	60	-	-	70	-	-	ns
t_{AVWL}	t_{AS}	Address Set up Time	0	-	-	0	-	-	0	-	-	ns
t_{AVWH}	t_{AW}	Address Valid to End of Write	65	-	-	65	-	-	70	-	-	ns
t_{WLWH}	t_{WP}	Write Pulse Width	40	-	-	40	-	-	50	-	-	ns
t_{WHAX}	t_{WR}	Write Recovery Time	5	-	-	5	-	-	0	-	-	ns
t_{WLQZ}	t_{WHZ}	Write to Output in High Z	0	-	25	0	-	30	0	-	35	ns
t_{DVWH}	t_{DW}	Data Valid to End of Write	30	-	-	30	-	-	30	-	-	ns
t_{WHDX}	t_{DH}	Data Hold from Write Time	5	-	-	5	-	-	0	-	-	ns
t_{GHZQ}	t_{OHZ}	Output Disable to Output in High Z	0	-	25	0	-	30	0	-	35	ns
t_{WHQX}	t_{OW}	Output Active from End of Write	5	-	-	5	-	-	5	-	-	ns

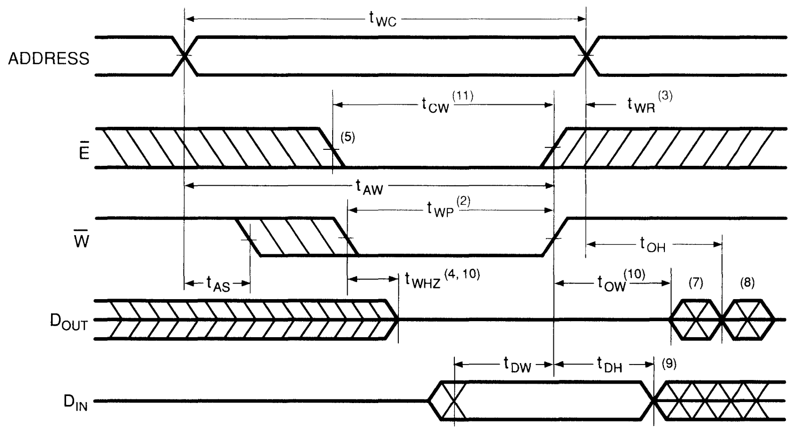
SWITCHING WAVEFORMS (WRITE CYCLE)

WRITE CYCLE 1[(1)]



SWITCHING WAVEFORMS (WRITE CYCLE)

WRITE CYCLE 2(1,6)



NOTES:
1. $\overline{W}$ must be high during address transitions.
2. The internal write time of the memory is defined by the overlap $\overline{E}$ active and $\overline{W}$ low. Both signals must be active to initiate and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
3. T_{WR} is measured from the earlier of $\overline{E}$ or $\overline{W}$ going high at the end of write cycle.
4. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{E}$ low transition occurs simultaneously with the $\overline{W}$ low transitions or after the $\overline{W}$ low transition, outputs remain in a high impedance state.
6. $\overline{G}$ is continuously low ($\overline{G} = V_{IL}$).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\overline{E}$ is low during this period, DQ pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured ±500mV from steady state with C_L = 5pF as shown in Figure 1b on page 4. This parameter is guaranteed and not 100% tested.
11. t_{CW} is measured from $\overline{E}$ going low to the end of write.

ORDERING INFORMATION

SPEED (ns)	ORDERING PART NUMBER	PACKAGE REFERENCE NO.	TEMPERATURE RANGE
70	MS62256L-70FC	S28-3	0°C to +70°C
70	MS62256L-70PC	P28-1	0°C to +70°C
85	MS62256L-85FC	S28-3	0°C to +70°C
85	MS62256L-85PC	P28-1	0°C to +70°C
100	MS62256L-10FC	S28-2	0°C to +70°C
100	MS62256L-10PC	P28-1	0°C to +70°C

PRELIMINARY

32K x 8 High Speed CMOS Static RAM

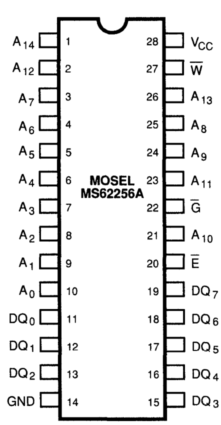
FEATURES

- High-speed – 25/35/45/55 ns
- Low Power dissipation:
  MS62256AL
  225mW (Typ.) Operating
  30µW (Typ.) Standby
- Fully static operation
- All inputs and outputs directly TTL compatible
- Three state outputs
- Ultra low data retention supply current at V_{CC} = 2V

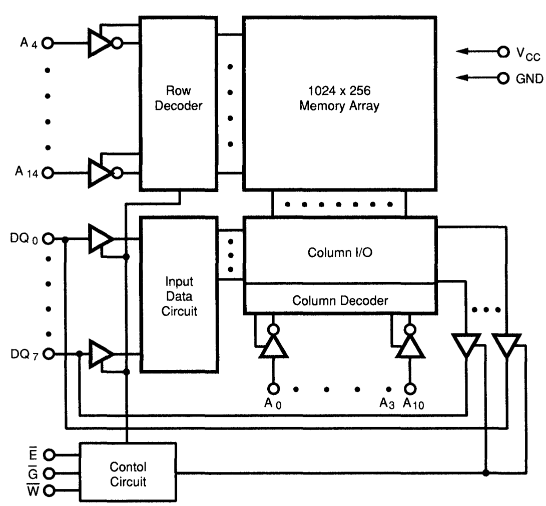
DESCRIPTION

The MOSEL MS62256A is a 262,144-bit static random access memory organized as 32,768 words by 8 bits and operates from a single 5 volt supply. It is built with MOSEL's high performance twin tub CMOS process. Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures. The MS62256A is available in a standard 28-pin 600 mil plastic DIP package.

PIN CONFIGURATIONS



FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

A_0 - A_{14} Address Inputs

These 15 address inputs select one of the 32768 8-bit words in the RAM.

$\overline{E}$ Chip Enable Input

$\overline{E}$ is active LOW. The chip enable must be active to read from or write to the device. If it is not active, the device is deselected and is in a standby power mode. The DQ pins will be in the high-impedance state when deselected.

$\overline{G}$ Output Enable Input

The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when $\overline{G}$ is inactive.

$\overline{W}$ Write Enable Input

The write enable input is active LOW and controls read and write operations. With the chip enabled, when $\overline{W}$ is HIGH and $\overline{G}$ is LOW, output data will be present at the DQ pins; when $\overline{W}$ is LOW, the data present on the DQ pins will be written into the selected memory location.

DQ_0 - DQ_7 Data Input/Output Ports

These 8 bidirectional ports are used to read data from or write data into the RAM.

V_{CC} Power Supply

GND Ground

TRUTH TABLE

MODE	$\overline{E}$	$\overline{G}$	$\overline{W}$	I/O OPERATION
Standby	H	X	X	High Z
Read	L	L	H	D_{OUT}
Read	L	H	H	High Z
Write	L	X	L	D_{IN}

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	PARAMETER		RATING	UNITS
V_{CC}	Supply Voltage		-0.3 to 7	V
V_{IN}	Input Voltage		-0.3 to 7	V
V_{DQ}	Input/Output Voltage Applied		-0.3 to 6	V
T_{BIAS}	Temperature Under Bias	Plastic	-10 to +125	°C
T_{STG}	Storage Temperature	Plastic	-40 to +150	°C
P_D	Power Dissipation		1.0	W
I_{OUT}	DC Output Current		50	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

OPERATING RANGE

RANGE	AMBIENT TEMPERATURE	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

DC ELECTRICAL CHARACTERISTICS (over the commercial operating range)

PARAMETER NAME	PARAMETER	TEST CONDITIONS	MS62256A MIN.	TYP.[1]	MAX.	UNITS
V_{IL}	Guaranteed Input Low Voltage[2,3]		–0.3	-	0.8	V
V_{IH}	Guaranteed Input High Voltage[2]		2.2	-	6.0	V
I_{IL}	Input Leakage Current	V_{CC} = Max, V_{IN} = 0V to V_{CC}	-	-	2	µA
I_{OL}	Output Leakage Current	V_{CC} = Max, $\overline{E} = V_{IH}$ or $\overline{G} = V_{IH}$, V_{IN} = 0V t o V_{CC}	-	-	2	µA
V_{OL}	Output Low Voltage	V_{CC} = Min, I_{OL} = 4mA	-	-	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min, I_{OH} = –1.0mA	2.4	-	-	V
I_{CC}	Operating Power Supply Current	V_{CC} = Max, $\overline{E} = V_{IL}$, I_{DQ} = 0mA, F = F_{max}[4]	-	-	120	mA
I_{CCSB}	Standby Power Supply Current	V_{CC} = Max, $\overline{E} = V_{IH}$, I_{DQ} = 0mA	-	-	20	mA
I_{CCSB1}	Power Down Power Supply Current	V_{CC} = Max, $\overline{E} > V_{CC} - 0.2V$	-	-	2	mA
		$V_{IN} > V_{CC} - 0.2V$ or $V_{IN} < 0.2V$	-	-	.1[5]	

1. Typical characteristics are at V_{CC} = 5V, T_A = 25°C.
2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
3. V_{IL} (Min.) = –3.0V for pulse width ≤ 20ns
4. $F_{MAX} = 1/t_{RC}$.
5. L version only.

CAPACITANCE[1] (T_A = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$ = 0V	10	pF

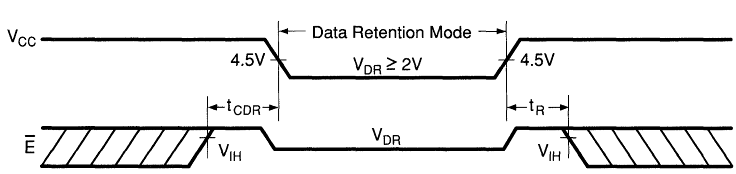
1. This parameter is guaranteed and not tested.

DATA RETENTION CHARACTERISTICS (over the commercial operating range)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.[1]	MAX[2]	UNITS
V_{DR}	V_{CC} for Data Retention	$\overline{E} \geq V_{CC} - 0.2V$, $\overline{G} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	2.0	-	-	V
I_{CCDR}	Data Retention Current	$\overline{E} \geq V_{CC} - 0.2V$, $\overline{G} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	-	2	50	µA
t_{CDR}	Chip Deselect to Data Retention Time	See Retention Waveform	0	-	-	ns
t_R	Operation Recovery Time		t_{RC}[3]	-	-	ns

1. V_{CC} = 2V, T_A = +25°C
2. V_{CC} = 3V
3. t_{RC} = Read Cycle Time

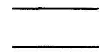
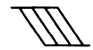
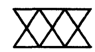
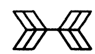
TIMING WAVEFORM LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5ns
Timing Reference Level	1.5V

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

AC TEST LOADS AND WAVEFORMS

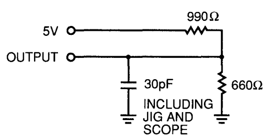


Figure 1a

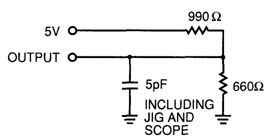
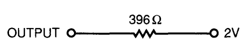


Figure 1b

Equivalent to:

THEVENIN EQUIVALENT



ALL INPUT PULSES

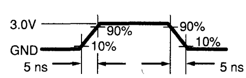


Figure 2

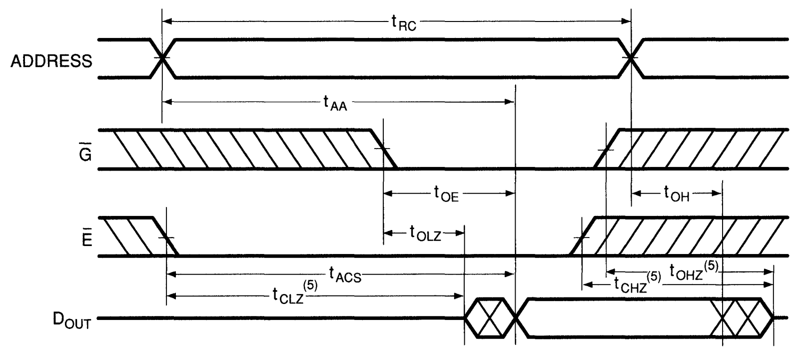
AC ELECTRICAL CHARACTERISTICS (over the commercial operating range)

READ CYCLE

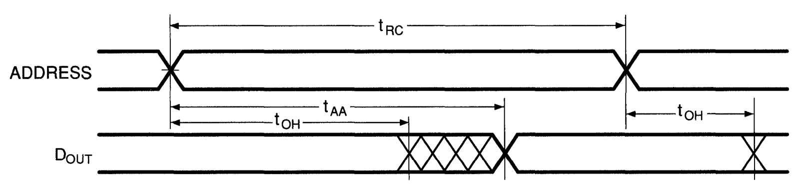
JEDEC PARAMETER NAME	PARAMETER NAME	PARAMETER	MS62256A-25 MIN.	MS62256A-25 MAX.	MS62256A-35 MIN.	MS62256A-35 MAX.	MS62256A-45 MIN.	MS62256A-45 MAX.	MS62256A-55 MIN.	MS62256A-55 MAX.	UNIT
t_{AVAX}	t_{RC}	Read Cycle Time	25	-	35	-	45	-	55	-	ns
t_{AVQV}	t_{AA}	Address Access Time	-	25	-	35	-	45	-	55	ns
t_{ELQV}	t_{ACS}	Chip Enable Access Time	-	25	-	35	-	45	-	55	ns
t_{GLQX}	t_{OE}	Output Enable to Output Valid	-	15	-	20	-	20	-	25	ns
t_{EHQZ}	t_{CLZ}	Chip Enable to Output Low Z	5	-	5	-	5	-	5	-	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z	0	-	0	-	0	-	0	-	ns
t_{EHQZ}	t_{CHZ}	Chip Disable to Output in High Z	-	15	-	20	-	20	0	25	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z	-	15	-	20	-	20	0	25	ns
t_{AXQX}	t_{OH}	Output Hold from Address Change	5	-	5	-	5	-	5	-	ns

SWITCHING WAVEFORMS (READ CYCLE)

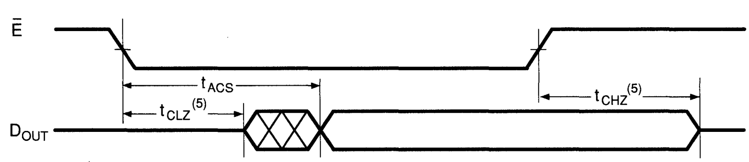
READ CYCLE 1[1]



READ CYCLE 2[1, 2, 4]



READ CYCLE 3[1, 3, 4]



NOTES:
1. $\overline{W}$ is High for READ Cycle.
2. Device is continuously selected $\overline{E} = V_{IL}$.
3. Address valid prior to or coincident with $\overline{E}$ transition low.
4. $\overline{G} = V_{IL}$.
5. Transition is measured ± 500mV from steady state with C_L = 5pF as shown in Figure 1b on page 4. This parameter is guaranteed and not 100% tested.

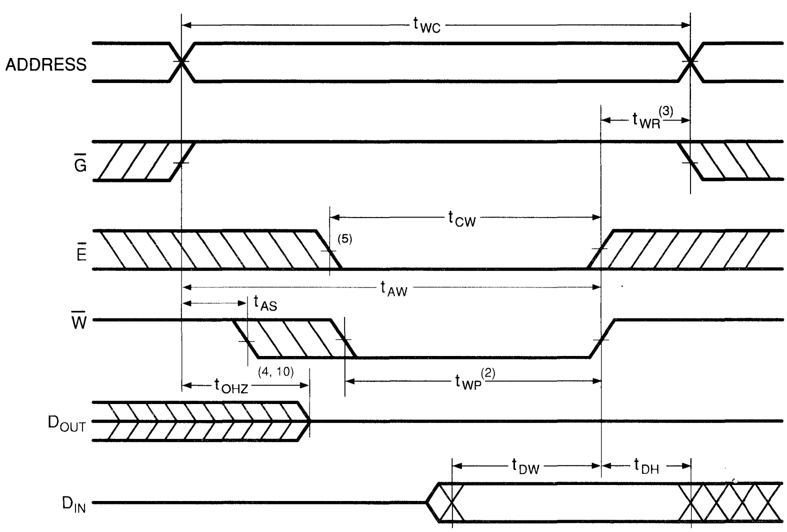
AC ELECTRICAL CHARACTERISTICS (over the commercial operating range)

WRITE CYCLE

JEDEC PARAMETER NAME	PARAMETER NAME	PARAMETER	MS62256A-25		MS62256A-35		MS62256A-45		MS62256A-55		UNIT
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{AVAX}	t_{WC}	Write Cycle Time	25	-	35	-	45	-	55	-	ns
t_{ELWH}	t_{CW}	Chip Enable to End of Write	20	-	30	-	40	-	50	-	ns
t_{AVWL}	t_{AS}	Address Set up Time	0	-	0	-	0	-	0	-	ns
t_{AVWH}	t_{AW}	Address Valid to End of Write	20	-	30	-	40	-	50	-	ns
t_{WLWH}	t_{WP}	Write Pulse Width	20	-	25	-	30	-	35	-	ns
t_{WHAX}	t_{WR}	Write Recovery Time	0	-	3	-	3	-	3	-	ns
t_{WLQZ}	t_{WHZ}	Write to Output in High Z	0	15	0	20	0	25	0	30	ns
t_{DVWH}	t_{DW}	Data to Write Time Overlap	15	-	20	-	20	-	25	-	ns
t_{WHDX}	t_{DH}	Data Hold from Write Time	0	-	0	-	0	-	0	-	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z	0	15	0	20	0	20	0	25	ns
t_{WHQX}	t_{OW}	Output Active from End of Write	5	-	5	-	5	-	5	-	ns

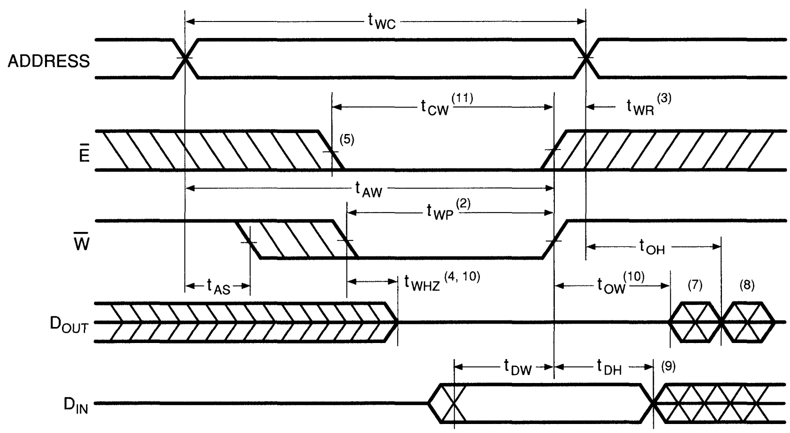
SWITCHING WAVEFORMS (WRITE CYCLE)

WRITE CYCLE 1[1]



SWITCHING WAVEFORMS (WRITE CYCLE)

WRITE CYCLE 2(1,6)



NOTES:
1. $\overline{W}$ must be high during address transitions.
2. The internal write time of the memory is defined by the overlap $\overline{E}$ active and $\overline{W}$ low. Both signals must be active to initiate and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
3. T_{WR} is measured from the earlier of $\overline{E}$ or $\overline{W}$ going high at the end of write cycle.
4. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{E}$ low transition occurs simultaneously with the $\overline{W}$ low transitions or after the $\overline{W}$ low transition, outputs remain in a high impedance state.
6. $\overline{G}$ is continuously low ($\overline{G} = V_{IL}$).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\overline{E}$ is low during this period, DQ pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured ±500mV from steady state with C_L = 5pF as shown in Figure 1b on page 4. This parameter is guaranteed and not 100% tested.
11. t_{cw} is measured from $\overline{E}$ going low to the end of write.

ORDERING INFORMATION

SPEED (ns)	ORDERING PART NUMBER	PACKAGE REFERENCE NO.	TEMPERATURE RANGE
25	MS62256A-25PC	P28-1	0°C to +70°C
25	MS62256AL-25PC		0°C to +70°C
35	MS62256A-35PC		0°C to +70°C
35	MS62256AL-35PC		0°C to +70°C
45	MS62256A-45PC		0°C to +70°C
45	MS62256AL-45PC		0°C to +70°C
55	MS62256A-55PC		0°C to +70°C
55	MS62256AL-55PC		0°C to +70°C

MS62256B

ADVANCE INFORMATION

32K x 8 CMOS Static RAM

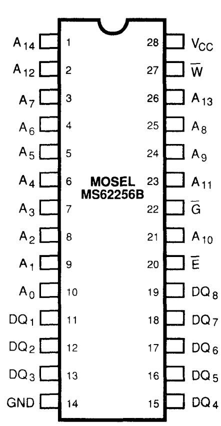
FEATURES

- High-speed – 70/100/120/150 ns
- Low Power dissipation:
  - 440mW (Max) Operating
  - 16.5mW (Max) Standby
  - 5.5mW (Max) Power-down (MS62256B)
  - 0.55mW (Max) Power-down (MS62256BL/BLL)
- Fully static operation
- All inputs and outputs directly TTL compatible
- Three state outputs
- Ultra low data retention supply current at V_{CC} = 2V

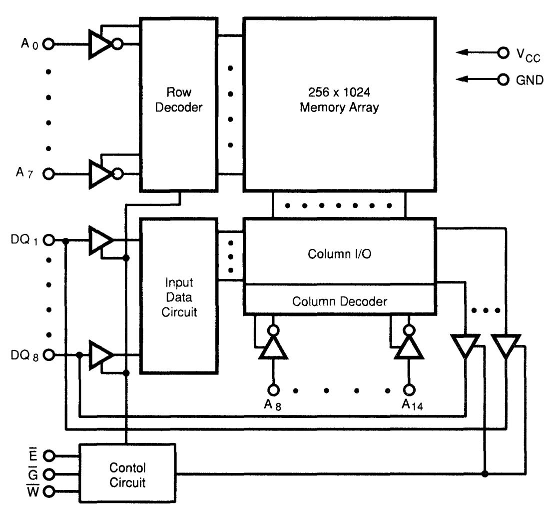
DESCRIPTION

The MOSEL MS62256B is a 262,144-bit static random access memory organized as 32,768 words by 8 bits and operates from a single 5 volt supply. It is built with MOSEL's high performance twin tub CMOS process. Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures. The MS62256B is available in a standard 28-pin 600 mil plastic DIP package and 330 mil SOP.

PIN CONFIGURATIONS



FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

A_0 - A_{14} Address Inputs

These 15 address inputs select one of the 32768 8-bit words in the RAM.

$\overline{E}$ Chip Enable Input

$\overline{E}$ is active LOW. The chip enable must be active to read from or write to the device. If it is not active, the device is deselected and is in a standby power mode. The DQ pins will be in the high-impedance state when deselected.

$\overline{G}$ Output Enable Input

The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when $\overline{G}$ is inactive.

$\overline{W}$ Write Enable Input

The write enable input is active LOW and controls read and write operations. With the chip enabled, when $\overline{W}$ is HIGH and $\overline{G}$ is LOW, output data will be present at the DQ pins; when $\overline{W}$ is LOW, the data present on the DQ pins will be written into the selected memory location.

DQ_1 - DQ_8 Data Input/Output Ports

These 8 bidirectional ports are used to read data from or write data into the RAM.

V_{CC} Power Supply

GND Ground

TRUTH TABLE

MODE	$\overline{E}$	$\overline{G}$	$\overline{W}$	I/O OPERATION
Standby	H	X	X	High Z
Read	L	L	H	D_{OUT}
Read	L	H	H	High Z
Write	L	X	L	D_{IN}

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply Voltage	–0.5 to 7	V
V_{IN}	Input Voltage	–0.5 to 7	
V_{DQ}	Input/Output Voltage Applied	–0.5 to V_{CC} +0.5	
T_{BIAS}	Temperature Under Bias	–10 to +85	°C
T_{STG}	Storage Temperature	–40 to +125	°C
P_D	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	25	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

2

DC ELECTRICAL CHARACTERISTICS (over the commercial operating range)

PARAMETER NAME	PARAMETER	TEST CONDITIONS		-70 MIN.	-70 TYP.(1)	-70 MAX.	-10/12/15 MIN.	-10/12/15 TYP.(1)	-10/12/15 MAX.	UNITS
V_{IL}	Guaranteed Input LOW Voltage(2)(3)			–0.3	-	+0.8	–0.3	-	+0.8	V
V_{IH}	Guaranteed Input HIGH Voltage(2)			2.2	-	V_{CC} + 0.3	2.2	-	V_{CC} + 0.3	V
I_{IL}	Input Leakage Current	V_{CC} = Max, V_{IN} = 0V to V_{CC}		–1	-	1	–1	-	1	µA
I_{OL}	Output Leakage Current	V_{CC} = Max, $\overline{E} = V_{IH}$, V_{IN} = 0V t o V_{CC}		–1	-	1	–1	-	1	µA
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 2.1mA		-	-	0.4	-	-	0.4	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = –1mA		2.4	3.5	-	2.4	3.5	-	V
I_{CC}	Operating Power Supply Current	V_{CC} = Max, $\overline{E} = V_{IL}$, $I_{I/O}$ = 0mA, $F=F_{max}$(4)		-	-	80	-	-	70	mA
I_{CCSB}	Standby Power Supply Current	V_{CC} = Max, $\overline{E} = V_{IH}$, $I_{I/O}$ = 0mA		-	-	3	-	-	3	mA
I_{CCSB1}	Power Down Power Supply Current	V_{CC} = Max, $\overline{E} > V_{CC} - 0.2V$	MS62256BL/LL	-	-	0.1	-	-	0.1	mA
			MS62256B	-	-	1.0	-	-	1.0	

1. Typical characteristics are at V_{cc} = 5V, T_A = 25°C.
2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
3. V_{IL} (Min.) = –3.0V for pulse width ≤ 20ns
3. $F_{MAX} = 1/t_{RC.}$

CAPACITANCE(1) (T_A = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	7	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$ = 0V	8	pF

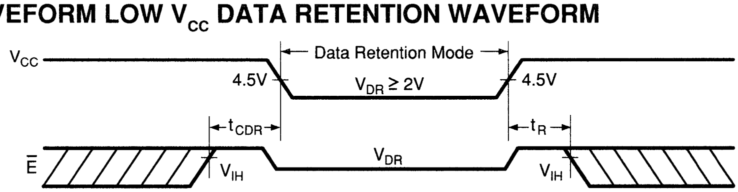
1. This parameter is guaranteed and not tested.

DATA RETENTION CHARACTERISTICS (over the commercial operating range)

SYMBOL	PARAMETER		TEST CONDITIONS	MIN.	TYP.(1)	MAX	UNITS
V_{DR}	V_{CC} for Data Retention		$\overline{E} \geq V_{CC}$-0.2V	2.0	-	5.5	V
I_{CCDR}	Data Retention Current	MS62256B		-	2	1.0	mA
		MS62256BL	V_{DR} = 3.0V, $\overline{E} \geq V_{DR} - 0.2V$ (2)	-	1.0	50	µA
		MS62256BLL		-	1.0	5.0	µA
t_{CDR}	Chip Deselect to Data Retention Time		See Retention Waveform	0	-	-	ns
t_R	Operation Recovery Time			t_{RC}(3)	-	-	ns

1. V_{cc} = 2V, T_A = +25°C
2. T_A = 40°C
3. t_{RC} = Read Cycle Time

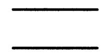
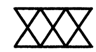
TIMING WAVEFORM LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5ns
Timing Reference Level	1.5V

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

AC TEST LOADS AND WAVEFORMS

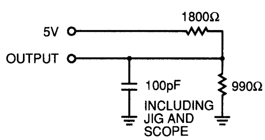


Figure 1a

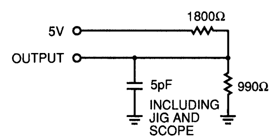
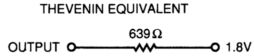


Figure 1b

Equivalent to:

THEVENIN EQUIVALENT



ALL INPUT PULSES

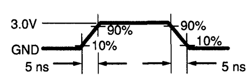


Figure 2

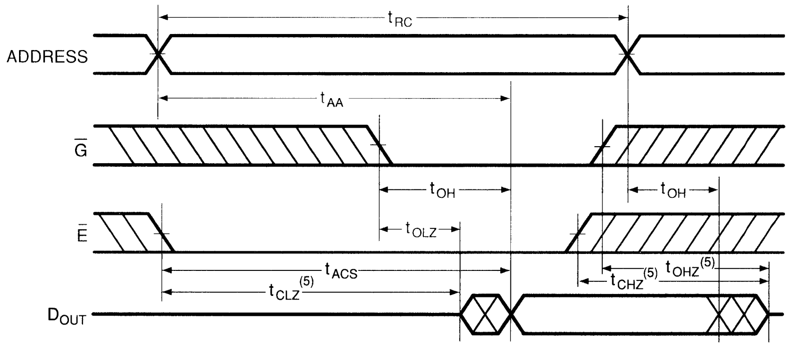
AC ELECTRICAL CHARACTERISTICS (over the commercial operating range)

READ CYCLE

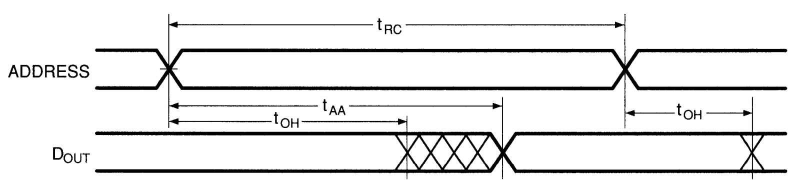
JEDEC PARAMETER NAME	PARAMETER NAME	PARAMETER	MS62256B-70			MS62256B-10			MS62256B-12			MS62256B-15			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
t_{AVAX}	t_{RC}	Read Cycle Time	70		-	100		-	120		-	150		-	ns
t_{AVQV}	t_{AA}	Address Access Time	-		70	-		100	-		120	-		150	ns
t_{ELQV}	t_{ACS}	Chip Enable Access Time	-		70	-		100	-		120	-		150	ns
t_{GLQX}	t_{OE}	Output Enable to Output Valid	-		35	-		50	-		50	-		60	ns
t_{EHQZ}	t_{CLZ}	Chip Enable to Output Low Z	5		-	10		-	10		-	10		-	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z	5		-	10		-	10		-	10		-	ns
t_{EHQZ}	t_{CHZ}	Chip Disable to Output in High Z	0		30	0		35	0		40	-		50	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z	0		30	0		35	0		40	-		50	ns
t_{AXQX}	t_{OH}	Output Hold from Address Change	10		-	10		-	20		-	20		-	ns

SWITCHING WAVEFORMS (READ CYCLE)

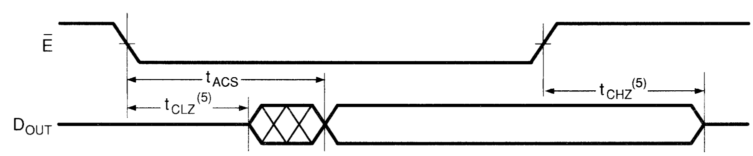
READ CYCLE 1(1)



READ CYCLE 2(1, 2, 4)



READ CYCLE 3(1, 3, 4)



NOTES:
1. $\overline{W}$ is High for READ Cycle.
2. Device is continuously selected $\overline{E} = V_{IL}$.
3. Address valid prior to or coincident with $\overline{E}$ transition low.
4. $\overline{G} = V_{IL}$.
5. Transition is measured ± 500mV from steady state with C_L = 5pF as shown in Figure 1b on page 4. This parameter is guaranteed and not 100% tested.

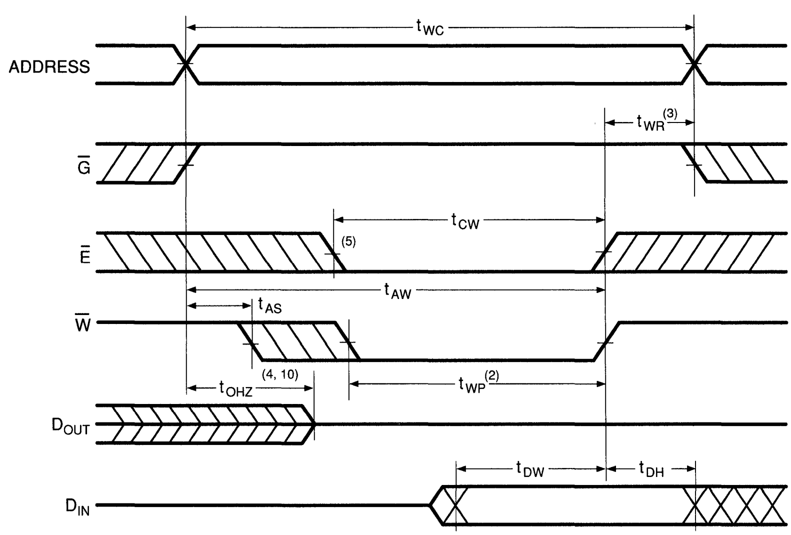
AC ELECTRICAL CHARACTERISTICS (over the commercial operating range)

WRITE CYCLE

JEDEC PARAMETER NAME	PARAMETER NAME	PARAMETER	MS62256B-70 MIN.	TYP.	MAX.	MS62256B-10 MIN.	TYP.	MAX.	MS62256B-12 MIN.	TYP.	MAX.	MS62256B-15 MIN.	TYP.	MAX.	UNIT
t_{AVAX}	t_{WC}	Write Cycle Time	70		-	100		-	120		-	100		-	ns
t_{ELWH}	t_{CW}	Chip Enable to End of Write	45		-	70		-	85		-	100		-	ns
t_{AVWL}	t_{AS}	Address Set up Time	0		-	0		-	0		-	0		-	ns
t_{AVWH}	t_{AW}	Address Valid to End of Write	65		-	70		-	85		-	180		-	ns
t_{WLWH}	t_{WP}	Write Pulse Width	40		-	50		-	70		-	90		-	ns
t_{WHAX}	t_{WR}	Write Recovery Time	5		-	5		-	5		-	5		-	ns
t_{WLQZ}	t_{WHZ}	Write to Output in High Z	0		25	0		35	0		40	-		50	ns
t_{DVWH}	t_{DW}	Data Valid to End of Write	30		-	30		-	45		-	50		-	ns
t_{WHDX}	t_{DH}	Data Hold from Write Time	5		-	10		-	0		-	0		-	ns
t_{GHZQ}	t_{OHZ}	Output Disable to Output in High Z	0		25	0		35	0		40			45	ns
t_{WHQX}	t_{OW}	Output Active from End of Write	5		-	5		-	5		-	5			ns

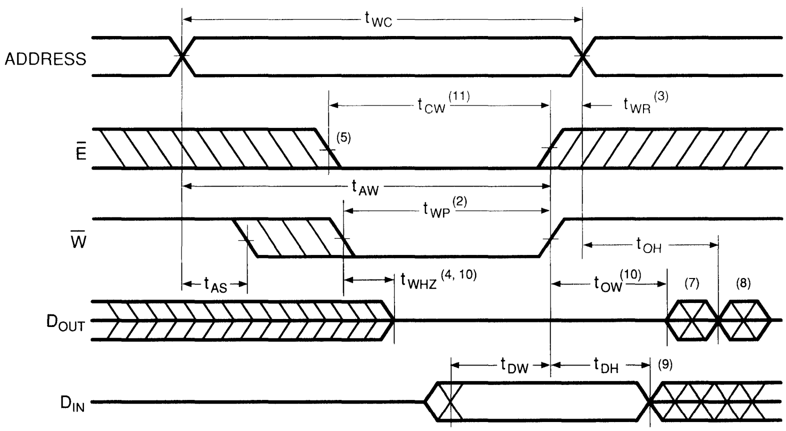
SWITCHING WAVEFORMS (WRITE CYCLE)

WRITE CYCLE 1(1)



SWITCHING WAVEFORMS (WRITE CYCLE)

WRITE CYCLE 2(1,6)



NOTES:

1. $\overline{W}$ must be high during address transitions.
2. The internal write time of the memory is defined by the overlap $\overline{E}$ active and $\overline{W}$ low. Both signals must be active to initiate and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
3. T_{WR} is measured from the earlier of $\overline{E}$ or $\overline{W}$ going high at the end of write cycle.
4. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{E}$ low transition occurs simultaneously with the $\overline{W}$ low transitions or after the $\overline{W}$ low transition, outputs remain in a high impedance state.
6. $\overline{G}$ is continuously low ($\overline{G} = V_{IL}$).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\overline{E}$ is low during this period, DQ pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured ±500mV from steady state with C_L = 5pF as shown in Figure 1b on page 4. This parameter is guaranteed and not 100% tested.
11. t_{CW} is measured from $\overline{E}$ going low to the end of write.

ORDERING INFORMATION

SPEED (ns)	ORDERING PART NUMBER	PACKAGE REFERENCE NO.	TEMPERATURE RANGE
70	MS62256B-70PC	P28-4	0°C to +70°C
70	MS62256B-70FC	S28-5	0°C to +70°C
100	MS62256B-10PC	P28-4	0°C to +70°C
100	MS62256B-10FC	S28-5	0°C to +70°C
120	MS62256B-12PC	P28-4	0°C to +70°C
120	MS62256B-12FC	S28-5	0°C to +70°C
150	MS62256B-15PC	P28-4	0°C to +70°C
150	MS62256B-15FC	S28-5	0°C to +70°C

Note 1: For the low power part number, add an L after the "B" and before the "-". Example MS62256BL-70PC
Note 2: For the low/low power part number, add an "LL" after the "B" and before the "-". Example MS62256BLL-70PC.

128K x 8 CMOS Static RAM Module

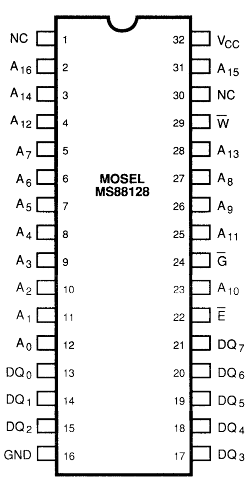
FEATURES

- Compatible with JEDEC standard pinout for monolithic megabit 128K x 8
- 600 mil wide JEDEC footprint
- Available in 100/120 ns versions
- Low Power dissipation:
  - 250mW (Typ.) Operating
  - 10mW (Typ.) Standby
- Fully static operation
- All inputs and outputs directly TTL compatible
- Three state outputs

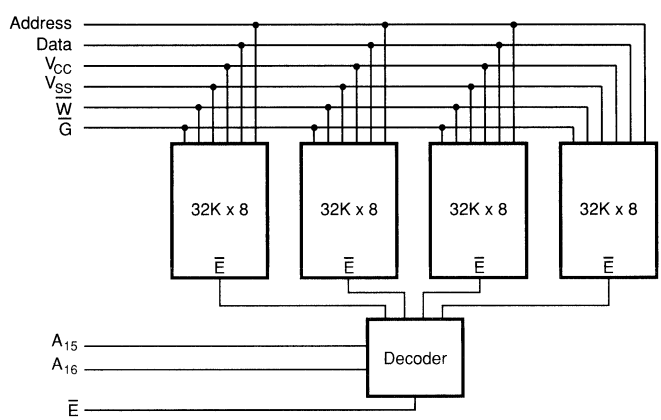
DESCRIPTION

The Mosel MS88128 is a 1 Megabit (1,048,576 bits) static random access memory module organized as 128K (131,072) words by 8 bits. It is built using four surface mounted 32K x 8 static RAMs and a single surface mounted 1 of 4 decoder buried in the substrate to provide compatibility with the JEDEC 128K x 8 pin definitions. The MS88128 is offered in a 600 mil wide 32 pin dual-in-line package.

PIN CONFIGURATIONS



FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

A_0 - A_{16} Address Inputs

These 17 address inputs select one of the 131,072 8-bit words in the RAM.

$\overline{E}$ Chip Enable Input

$\overline{E}$ is active LOW. The chip enable must be active to read from or write to the device. If it is not active, the device is deselected and is in a standby power mode. The DQ pins will be in the high-impedance state when deselected.

$\overline{G}$ Output Enable Input

The output enable inputs are active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when $\overline{G}$ is inactive.

$\overline{W}$ Write Enable Input

The write enable input is active LOW and controls read and write operations. With the chip enabled, when $\overline{W}$ is HIGH and $\overline{G}$ is LOW, output data will be present at the DQ pins; when $\overline{W}$ is LOW, the data present on the DQ pins will be written into the selected memory location.

DQ_0 - DQ_7 Data Input/Output Ports

These 8 bidirectional ports are used to read data from or write data into the RAM.

V_{CC} Power Supply
GND Ground

TRUTH TABLE

MODE	$\overline{E}$	$\overline{G}$	$\overline{W}$	I/O OPERATION
Standby	H	X	X	High Z
Read	L	L	H	D_{OUT}
Output Disabled	L	H	H	High Z
Write	L	X	L	D_{IN}

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	PARAMETER		RATING	UNITS
V_{CC}	Supply Voltage		-0.3 to 7	V
V_{IN}	Input Voltage		-0.3 to 7	
V_{DQ}	Input/Output Voltage Applied		-0.3 to 6	
T_{BIAS}	Temperature Under Bias	Plastic	-10 to +125	°C
T_{STG}	Storage Temperature	Plastic	-65 to +150	°C
P_D	Power Dissipation		1.0	W
I_{OUT}	DC Output Current		20	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

RANGE	AMBIENT TEMPERATURE	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

2

DC ELECTRICAL CHARACTERISTICS (over the commercial operating range)

PARAMETER NAME	PARAMETER	TEST CONDITIONS	MS88128 MIN.	TYP. (1)	MAX.	UNITS
V_{IL}	Guaranteed Input Low Voltage(2)		-0.3	-	+0.8	V
V_{IH}	Guaranteed Input High Voltage(2)		2.2	-	6.0	V
I_{IL}	Input Leakage Current	V_{CC} = Max, V_{IN} = 0V to V_{CC}	-	-	10	µA
I_{OL}	Output Leakage Current	V_{CC} = Max, $\overline{E} = V_{IH}$, or $\overline{G} = V_{IH}$, V_{IN} = 0V to V_{CC}	-	-	10	µA
V_{OL}	Output Low Voltage	V_{CC} = Min, I_{OL} = 2.1mA	-	-	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min, I_{OH} = -1.0mA	2.4	-	-	V
I_{CC}	Operating Power Supply Current	V_{CC} = Max, $\overline{E} = V_{IL}$, $I_{i/o}$ = 0mA, F_{max}(3)	-	50	95	mA
I_{CCSB}	Standby Power Supply Current	V_{CC} = Max, $\overline{E} \geq V_{IH}$	-	2	15	mA
I_{CCSB1}	Power Down Power Supply Current	V_{CC} = Max, $\overline{E} > V_{CC}$ - 0.2V, $V_{IN} > V_{CC}$ - 0.2V or V_{IN} < 0.2V	-	50	500	µA

1. Typical characteristics are at V_{cc} = 5V, T_A = 25°C.
2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
3. $F_{MAX} = 1/t_{RC}$.

CAPACITANCE(1) (T_A = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	PINS	MAX.	UNIT
C_I	Input Capacitance (except D/Q)	$\overline{G}$, A_0-A_{16}	TBD	pF
$C_{D/Q}$	Capacitance on DQ pins	DQ_0-DQ_7	TBD	pF
C_C	Input Capacitance Control Lines	$\overline{E}$	TBD	pF
C_W	Input Capacitance W Line	$\overline{W}$	TBD	pF

1. This parameter is guaranteed and not tested.

AC TEST CONDITIONS

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Level	1.5V

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

AC TEST LOADS AND WAVEFORMS

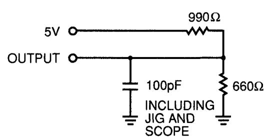


Figure 1a

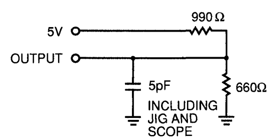
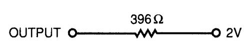


Figure 1b

Equivalent to:

THEVENIN EQUIVALENT



ALL INPUT PULSES

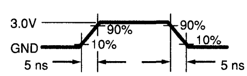


Figure 2

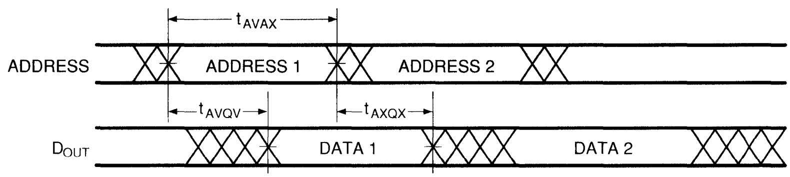
AC ELECTRICAL CHARACTERISTICS (over the commercial operating range)

READ CYCLE

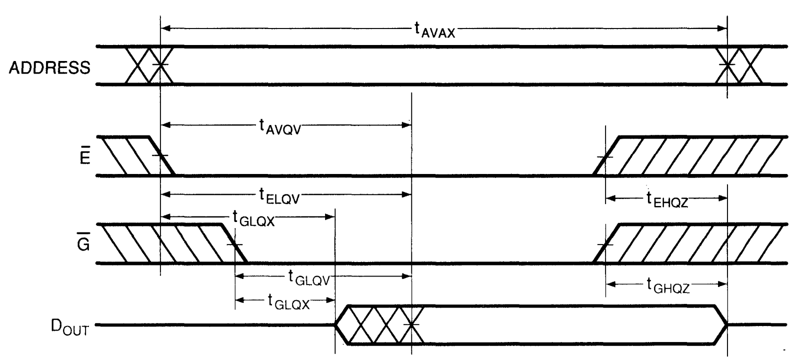
JEDEC PARAMETER NAME	PARAMETER NAME	PARAMETER	MS88128-10 MIN.	MS88128-10 MAX.	MS88128-12 MIN.	MS88128-12 MAX.	UNIT
t_{AVAX}	t_{RC}	Read Cycle Time	100	-	120	-	ns
t_{AVQV}	t_{AA}	Address Access Time	-	100	-	120	ns
t_{ELQV}	t_{ACS}	Chip Enable Access Time	-	100	-	120	ns
t_{GLQV}	t_{OE}	Output Enable to Output Valid	-	50	-	60	ns
t_{ELQX}	t_{CLZ}	Chip Enable to Output Low Z	30	-	30	-	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z	10	-	10	-	ns
t_{EHQZ}	t_{CHZ}	Chip Disable to Output in High Z	-	30	-	40	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z	-	30	-	40	ns
t_{AXQX}	t_{OH}	Output Hold from Address Change	10	-	10	-	ns

SWITCHING WAVEFORMS (READ CYCLE)

READ CYCLE 1
$\overline{W}$ HIGH, $\overline{G}$, $\overline{E}$ LOW



READ CYCLE 2
$\overline{W}$ HIGH



2

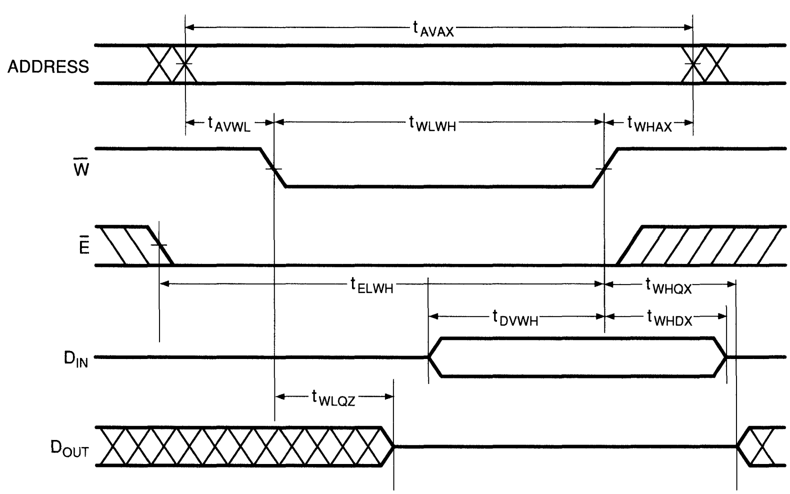
AC ELECTRICAL CHARACTERISTICS (over the commercial operating range)

WRITE CYCLE

JEDEC PARAMETER NAME	PARAMETER NAME	PARAMETER	MS88128-10 MIN.	MS88128-10 MAX.	MS88128-12 MIN.	MS88128-12 MAX.	UNIT
t_{AVAX}	t_{WC}	Write Cycle Time	100	-	120	-	ns
t_{ELWH}	t_{CW}	Chip Enable to End of Write	80	-	90	-	ns
t_{AVWL}	t_{AS}	Address Set up Time	20	-	20	-	ns
t_{WLWH}	t_{WP}	Write Pulse Width	60	-	70	-	ns
t_{WHAX}	t_{WR}	Write Recovery Time	0	-	0	-	ns
t_{WLQZ}	t_{WHZ}	Write to Output in High Z	0	35	0	40	ns
t_{DVWH}	t_{DW}	Data to Write Time Overlap	35	-	40	-	ns
t_{WHDX}	t_{DH}	Data Hold from Write Time	20	-	20	-	ns
t_{WHQX}	t_{OW}	Output Active from End of Write	0	-	0	-	ns

SWITCHING WAVEFORMS (WRITE CYCLE)

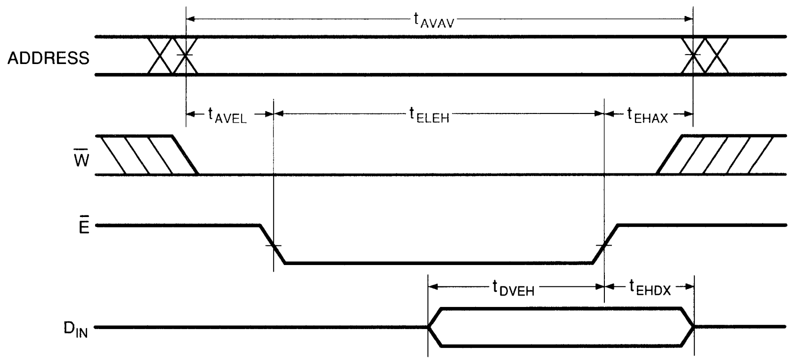
WRITE CYCLE 1



2

SWITCHING WAVEFORMS (WRITE CYCLE)

WRITE CYCLE 2
EARLY WRITE
$\overline{E}$ CONTROLLED

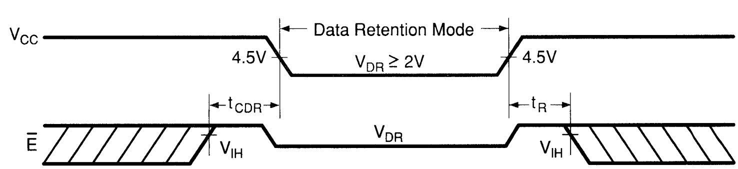


DATA RETENTION CHARACTERISTICS (over the commercial operating range)

SYMBOL	PARAMETER	TEST CONDITIONS	MS88128 MIN.	TYP.(2)	MAX(2)	UNITS
V_{DR}	VCC for Data Retention	$\overline{E} \geq V_{CC}$-0.2V, $\overline{G} \geq V_{CC}$ -0.2V, $V_{IN} \geq V_{CC}$-0.2V or $V_{IN} \leq 0.2V$	2.0	-	-	V
I_{CCDR}	Data Retention Current	$\overline{E}_1 \geq V_{CC}$-0.2V, $\overline{G} \geq V_{CC}$ -0.2V, $V_{IN} \geq V_{CC}$-0.2V or $V_{IN} \leq 0.2V$	-	20	100	µA
t_{CDR}	Chip Deselect to Data Retention Time	See Retention Waveform	0	-	-	ns
t_R	Operation Recovery Time		t_{RC}(4)	-	-	ns

1. V_{CC} = 2V, T_A = +25°C
2. V_{CC} = 3V
3. t_{RC} = Read Cycle Time

TIMING WAVEFORM LOW V_{CC} DATA RETENTION WAVEFORM



ORDERING INFORMATION

SPEED (ns)	ORDERING PART NUMBER	PACKAGE REFERENCE NO.	TEMPERATURE RANGE
100	MS88128-10PC	M-1	0°C to +70°C
120	MS88128-12PC		0°C to +70°C

ADVANCE INFORMATION

1048576 (131,072 x 8) CMOS Static RAM with Data Retention and Low Power

FEATURES

- Available in 80/100/120 ns (Max.)
- Automatic power-down when chip disabled
- Lower power consumption:
  MS621000
  – 5.5µW (Typ.) Standby
  MS621000L
  – 1.1mA (Typ.) Standby
- TTL compatible interface levels
- Single 5V power supply
- Fully static operation
- Three state outputs
- Two chip enable ($\overline{E}_1$ and E_2) for simple memory expansion
- Data retention as low as 2V

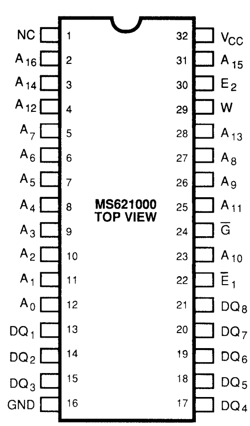
DESCRIPTION

The MOSEL MS621000 is a high performance, low power CMOS static RAM organized as 131,072 words by 8 bits. The device supports easy memory expansion with both an active LOW chip enable ($\overline{E}_1$) and an active High chip enable (E_2), as well as an active LOW output enable ($\overline{G}$) and tri-state outputs. An automatic power-down feature is included which reduces the chip power by 80% in TTL standby mode, and by over 95% in full power-down mode.

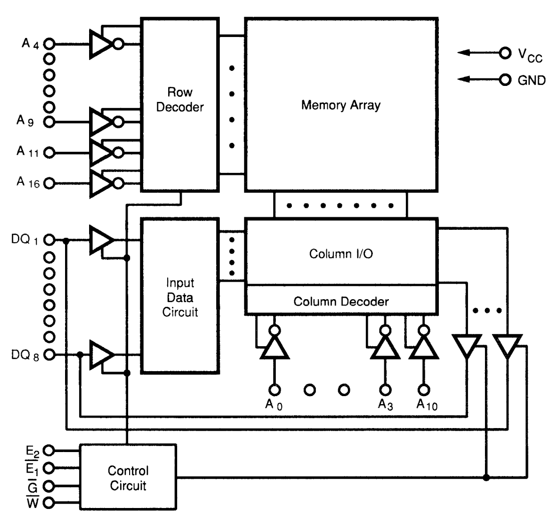
The device is manufactured in MOSEL's high performance CMOS process and operates from a single 5V power supply. All inputs and outputs are TTL compatible. Data is retained to as low as V_{CC} = 2V.

The MOSEL MS621000 is packaged in the JEDEC standard 32 pin 600 mil wide DIP and 525 mil wide SOP.

PIN CONFIGURATIONS



FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

A_0 - A_{16} Address Inputs

These 17 address inputs select one of the 131,072 8-bit words in the RAM.

$\overline{E}_1$ Chip Enable 1 Input

E_2 Chip Enable 2 Input

$\overline{E}_1$ is active LOW and E_2 is active HIGH. Both chip enables must be active to read from or write to the device. If either chip enable is not active, the device is deselected and is in a standby power mode. The DQ pins will be in the high-impedance state when the device is deselected.

$\overline{G}$ Output Enable Input

The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when $\overline{G}$ is inactive.

$\overline{W}$ Write Enable Input

The write enable input is active LOW and controls read and write operations. With the chip selected, when $\overline{W}$ is HIGH and $\overline{G}$ is LOW, output data will be present at the DQ pins; when $\overline{W}$ is LOW, the data present on the DQ pins will be written into the selected memory location.

DQ_1 - DQ_8 Data Input/Output Ports

These 8 bidirectional ports are used to read data from or write data into the RAM.

V_{CC} Power Supply

GND Ground

TRUTH TABLE

MODE	$\overline{W}$	$\overline{E}_1$	E_2	$\overline{G}$	I/O OPERATION	V_{CC} CURRENT
Not Selected	X	H	X	X	High Z	I_{CCSB}, I_{CCSB1}
(Power Down)	X	X	L	X	High Z	I_{CCSB}, I_{CCSB1}
Output Disabled	H	L	H	H	High Z	I_{CC}
Read	H	L	H	L	D_{OUT}	I_{CC}
Write	L	L	H	X	D_{IN}	I_{CC}

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	PARAMETER	RATING	UNITS
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_{BIAS}	Temperature Under Bias	–10 to +85	°C
T_{STG}	Storage Temperature	–40 to +125	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	20	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

CAPACITANCE(1) (T_A = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{DQ}	Input/Output Capacitance	$V_{I/O}$ = 0V	10	pF

1. This parameter is guaranteed and not tested.

2

DC ELECTRICAL CHARACTERISTICS (over the operating range)

PARAMETER NAME	PARAMETER	TEST CONDITIONS	MS621000 MIN.	MS621000 TYP.(1)	MS621000 MAX.	MS621000L MIN.	MS621000L TYP.(1)	MS621000L MAX.	UNITS
V_{IL}	Guaranteed Input Low Voltage(2)		–0.3	-	+0.8	–0.3	-	+0.8	V
V_{IH}	Guaranteed Input High Voltage(2)		2.2	-	+0.3	2.2	-	+0.3	V
I_{IL}	Input Leakage Current	V_{CC} = Max, V_{IN} = 0V to V_{CC}	–1	-	1	–1	-	1	µA
I_{OL}	Output Leakage Current	V_{CC} = Max, $\overline{E}_1 = V_{IH}$, or $E_2 = V_{IL}$, or $\overline{G} = V_{IH}$, V_{IN} = 0V to V_{CC}	–2	-	2	–2	-	2	µA
V_{OL}	Output Low Voltage	V_{CC} = Min, I_{OL} = 4mA	-	-	0.4	-	-	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min, I_{OH} = –1mA	2.4	-	-	2.4	-	-	V
I_{CC}	Operating Power Supply Current	V_{CC} = Max, $\overline{E}_1 = V_{IL}$, $E_2 = V_{IH}$, I_{DQ} = 0mA, $F = F_{max}$(3)	-	-	80	-	-	80	mA
I_{CCSB}	Standby Power Supply Current	V_{CC} = Max, $\overline{E}_1 = V_{IH}$, or $E_2 = V_{IL}$, I_{DQ} = 0mA	-	-	3	-	-	3	mA
I_{CCSB1}	Power Down Power Supply Current	V_{CC} = Max, $\overline{E}_1 > V_{CC} - 0.2V$, $E_2 < 0.2V$ $V_{IN} > V_{CC} - 0.2V$ or $V_{IN} < 0.2V$	-	-	1	-	-	0.2	mA

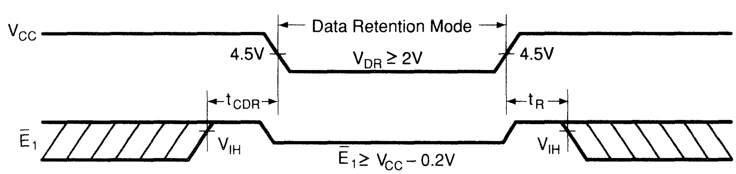
1. Typical characteristics are at V_{CC} = 5V, T_A = 25°C.
2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
3. $F_{MAX} = 1/t_{RC}$.

DATA RETENTION CHARACTERISTICS (T_A = 0 to +70°C)

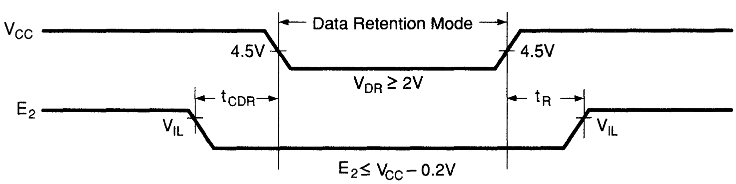
SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.(1)	MAX.	UNITS
V_{DR}	V_{CC} for Data Retention	$\overline{E}_1 \geq V_{CC}$ - 0.2V, $E_2 \leq$ 0.2V, $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V	2.0	-	5.5	V
I_{CCDR}(1)	Data Retention Current	MS621000	-	-	0.5	mA
		MS621000L	-	-	0.1	mA
t_{CDR}	Chip Deselect to Data Retention Time	See Retention Waveform	0	-	-	ns
t_R	Operation Recovery Time		t_{RC}(2)	-	-	ns

1. $V_{CC} = V_{DR}$ = 3V
   $\overline{E}_1 \geq V_{DR}$ = 0.2V, $E_2 \geq V_{DR}$ – 0.2V or $E_2 \leq$ 0.2V (at E_1 controlled)
2. t_{RC} : Read Cycle Time

LOW V_{CC} DATA RETENTION WAVEFORM (1) ($\overline{E}_1$ Controlled)



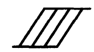
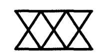
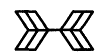
LOW V_{CC} DATA RETENTION WAVEFORM (2) (E_2 Controlled)



AC TEST CONDITIONS

Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	5ns
Input and Output	IN V_{IL} = 0.8, V_{IH} = 2.2V
Timing Reference Level	OUT V_{OL} = 0.8, V_{OH} = 2.0V

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

AC TEST LOADS AND WAVEFORMS

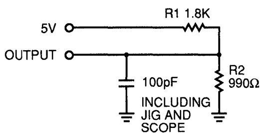


Figure 1a

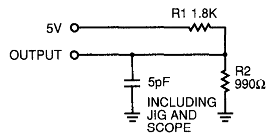
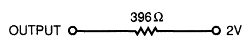


Figure 1b

Equivalent to:

THEVENIN EQUIVALENT



ALL INPUT PULSES

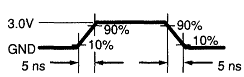


Figure 2

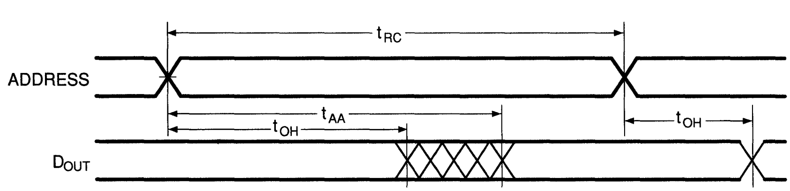
AC ELECTRICAL CHARACTERISTICS (over the operating range)

READ CYCLE

JEDEC PARAMETER NAME	PARAMETER NAME	PARAMETER		MS621000/L -80 MIN.	TYP.	MAX.	MS621000/L -10 MIN.	TYP.	MAX.	MS621000/L -12 MIN.	TYP.	MAX.	UNIT
t_{AVAX}	t_{RC}	Read Cycle Time		80	-	-	100	-	-	120	-	-	ns
t_{AVQV}	t_{AA}	Address Access Time		-	-	80	-	-	100	-	-	120	ns
t_{E1LQV}	t_{ACS1}	Chip Select Access Time	$\overline{E}_1$	-	-	80	-	-	100	-	-	120	ns
t_{E2HQV}	t_{ACS2}	Chip Select Access Time	E_2	-	-	80	-	-	100	-	-	120	ns
t_{GLQV}	t_{OE}	Output Enable to Output Valid		-	-	35	-	-	40	-	-	50	ns
t_{E1LQX}	t_{CLZ1}	Chip Select to Output Low Z	$\overline{E}_1$	10	-	-	10	-	-	10	-	-	ns
t_{E2HQX}	t_{CLZ2}	Chip Select to to Output Low Z	E_2	10	-	-	10	-	-	10	-	-	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z		5	-	-	5	-	-	5	-	-	ns
t_{E1HQZ}	t_{CHZ1}	Chip Deselect to Output in High Z	$\overline{E}_1$	0	-	30	0	-	35	0	-	40	ns
t_{E2HQZ}	t_{CHZ2}	Chip Deselect to Output in High Z	E_2	0	-	30	0	-	35	0	-	40	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z		0	-	30	0	-	30	0	-	40	ns
t_{AXQX}	t_{OH}	Output Hold from Address Change		10	-	-	10	-	-	10	-	-	ns

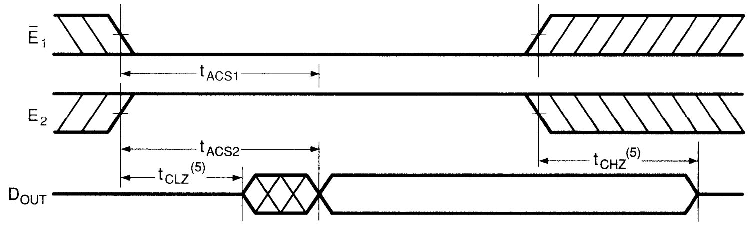
SWITCHING WAVEFORMS (READ CYCLE)

READ CYCLE 1(1,2,4)

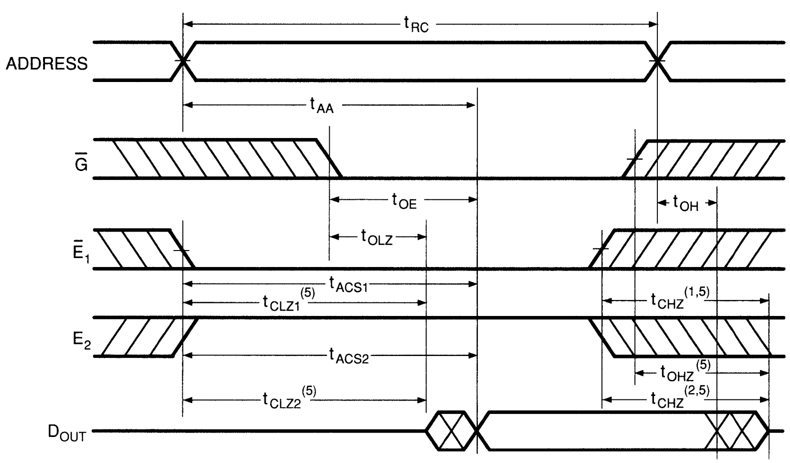


2

READ CYCLE 2[1,3,4]



READ CYCLE 3[1,4]



NOTES:
1. $\overline{W}$ is high for READ Cycle.
2. Device is continuously selected $\overline{E}_1 = V_{IL}$ and $E_2 = V_{IH}$.
3. Address valid prior to or coincident with $\overline{E}_1$ transition low and/or E_2 transition high.
4. $\overline{G} = V_{IL}$.
5. Transition is measured ± 500mV from steady state with C_L = 5pF as shown in Figure 1b. This parameter is guaranteed but not 100% tested.

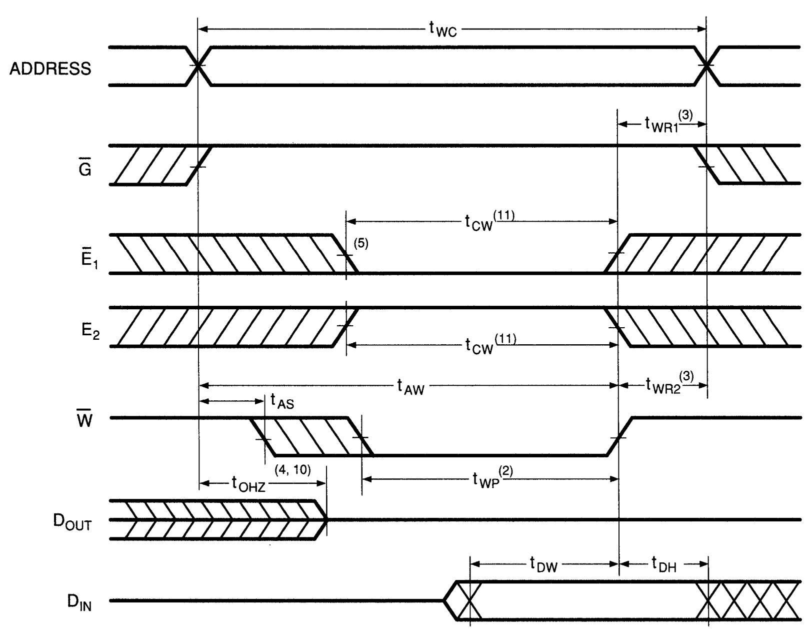
AC ELECTRICAL CHARACTERISTICS (over the operating range)

WRITE CYCLE

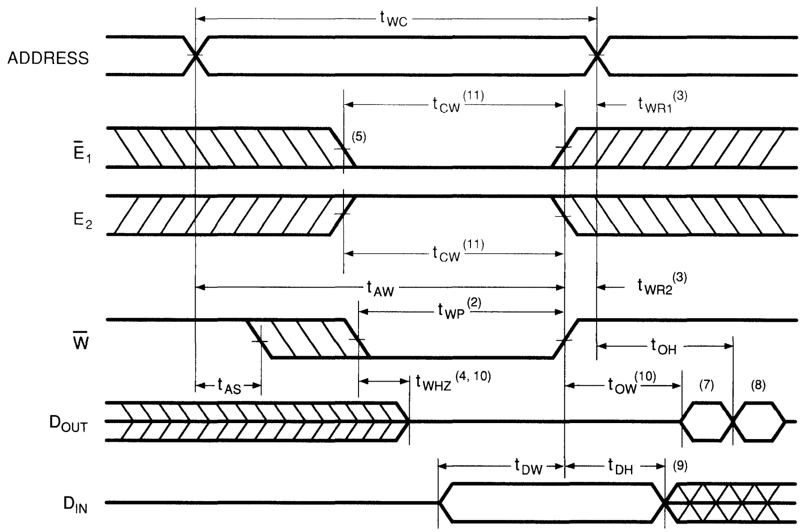
JEDEC PARAMETER NAME	PARAMETER NAME	PARAMETER		MS621000/L -80 MIN.	TYP.	MAX.	MS621000/L -10 MIN.	TYP.	MAX.	MS621000/L -12 MIN.	TYP.	MAX.	UNIT
t_{AVAX}	t_{WC}	Write Cycle Time		80	-	-	100	-	-	120	-	-	ns
t_{E1LWH}	t_{CW}	Chip Select to End of Write		60	-	-	80	-	-	85	-	-	ns
t_{AVWL}	t_{AS}	Address Set up Time		0	-	-	0	-	-	0	-	-	ns
t_{AVWH}	t_{AW}	Address Valid to End of Write		60	-	-	80	-	-	85	-	-	ns
t_{WLWH}	t_{WP}	Write Pulse Width		50	-	-	60	-	-	70	-	-	ns
t_{WHAX}	t_{WR1}	Write Recovery Time	$\overline{E}_1,\overline{W}$	5	-	-	5	-	-	5	-	-	ns
t_{E2LAX}	t_{WR2}	Write Recovery Time	E_2	5	-	-	5	-	-	5	-	-	ns
t_{WLQZ}	t_{WHZ}	Write to Output in High Z		0	-	30	-	-	35	-	-	40	ns
t_{DVWH}	t_{DW}	Data to Write Time Overlap		30	-	-	40	-	-	45	-	-	ns
t_{WHDX}	t_{DH}	Data Hold from Write Time		0	-	-	0	-	-	0	-	-	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z		0	-	30	0	-	35	-	-	40	ns
t_{WHQX}	t_{OW}	End of Write to Output Active		5	-	-	5	-	-	5	-	-	ns

SWITCHING WAVEFORMS (WRITE CYCLE)

WRITE CYCLE 1(1)



WRITE CYCLE 2(1,6)



NOTES:
1. $\overline{W}$ must be high during address transitions.
2. The internal write time of the memory is defined by the overlap of $\bar{E}_1$ and E_2 active and $\overline{W}$ low. All signals must be active to initiate a write and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
3. T_{WR} is measured from the earlier of $\bar{E}_1$ or $\overline{W}$ going high or E_2 going low at the end of write cycle.
4. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\bar{E}_1$ low transition or the E_2 high transition occurs simultaneously with the $\overline{W}$ low transitions or after the $\overline{W}$ transition, outputs remain in a high impedance state.
6. $\overline{G}$ is continuously low ($\overline{G} = V_{IL}$).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\bar{E}_1$ is low and E_2 is high during this period, DQ pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured ±500mV from steady state with C_L = 5pF as shown in Figure 1b on page 4. This parameter is guaranteed but not 100% tested.
11. t_{CW} is measured from the later of $\bar{E}_1$ going low or E_2 going high to the end of write.

ORDERING INFORMATION

SPEED (ns)	ORDERING PART NUMBER	PACKAGE REFERENCE NO.	TEMPERATURE RANGE
80	MS621000-80PC	P32-2	0°C to +70°C
80	MS621000-80FC	S32-1	0°C to +70°C
80	MS621000L-80PC	P32-2	0°C to +70°C
80	MS621000L-80FC	S32-1	0°C to +70°C
100	MS621000-10PC	P32-2	0°C to +70°C
100	MS621000-10FC	S32-1	0°C to +70°C
100	MS621000L-10PC	P32-2	0°C to +70°C
100	MS621000L-10FC	S32-1	0°C to +70°C
120	MS621000-12PC	P32-2	0°C to +70°C
120	MS621000-12FC	S32-1	0°C to +70°C
120	MS621000L-12PC	P32-2	0°C to +70°C
120	MS621000L-12FC	S32-1	0°C to +70°C

128K x 8 CMOS Static RAM

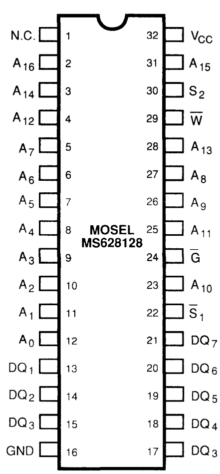
FEATURES

- High-speed – 70/85/100 ns
- Low Power dissipation:
  MS628128L
  10μW (Typ.) Standby
- Fully static operation
- All inputs and outputs directly TTL compatible
- Three state outputs
- Ultra low data retention supply current at V_{CC} = 2V

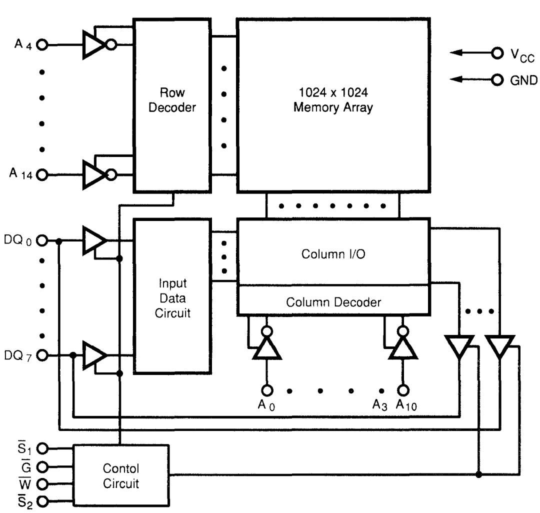
DESCRIPTION

The MOSEL MS628128 is a 1 Megabit static random access memory organized as 131,072 words by 8 bits and operates from a single 5 volt supply. It is built with MOSEL's high performance twin tub CMOS process. Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures. The MS628128 is available in a standard 32-pin 600 mil plastic DIP package and 525 mil SOP.

PIN CONFIGURATIONS



FUNCTIONAL BLOCK DIAGRAM



MOSEL MS6M8512

PRELIMINARY

512K x 8 CMOS Static RAM Module

FEATURES

- 4Mb SRAM module compatible with JEDEC standard pinout for 512k x 8 SRAM
- Available in 100/120 ns access times
- Fully static operation
- All inputs and outputs directly TTL compatible
- Three state outputs
- Single 5V power supply
- Low Power dissipation:

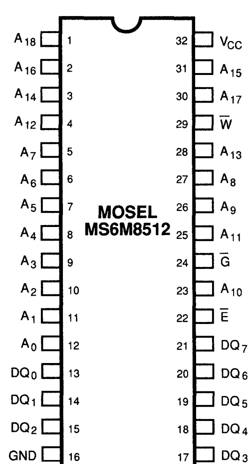
  350 mW (typ.) Operating
  25 mW (typ.) Standby
  50 µW (typ.) Power-Down
- 2V battery backup/data retention
- Packaged in JEDEC 600 mil PDIP

DESCRIPTION

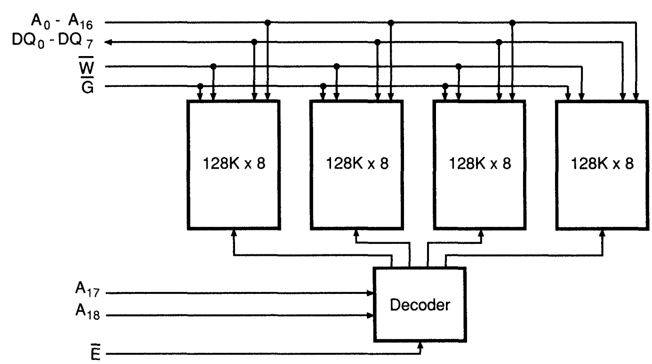
The Mosel MS6M8512 is a 4 Megabit (4,194,304 bits) static random access memory module organized as 512K (524,288) words by 8 bits. It is built using four surface mounted 128K x 8 static RAMs and a single surface mounted decoder. The device provides both an active LOW chip enable ($\overline{E}$) and an active LOW output enable ($\overline{G}$). An automatic power-down feature is included which reduces the chip power by 90% in TTL standby mode, and by over 99% in full power-down mode.

The MOSEL MS6M8512 is available in the JEDEC standard 32 pin 600 mil wide DIP package, and matches the JEDEC standard footprint and pin configuration for a monolithic 512K x 8 SRAM.

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

A_0 - A_{18} Address Inputs

These 19 address inputs select one of the 524,288 8-bit words in the RAM.

$\overline{E}$ Chip Enable Input

$\overline{E}$ is active LOW. The chip enable must be active to read from or write to the device. If it is not active, the device is deselected and is in a standby power mode. The DQ pins will be in the high-impedance state when deselected.

$\overline{G}$ Output Enable Input

The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when $\overline{G}$ is inactive.

$\overline{W}$ Write Enable Input

The write enable input is active LOW and controls read and write operations. With the chip enabled, when $\overline{W}$ is HIGH and $\overline{G}$ is LOW, output data will be present at the DQ pins; when $\overline{W}$ is LOW, the data present on the DQ pins will be written into the selected memory location.

DQ_0 - DQ_7 Data Input/Output Ports

These 8 bidirectional ports are used to read data from or write data into the RAM.

V_{CC} Power Supply

GND Ground

2

TRUTH TABLE

MODE	$\overline{E}$	$\overline{G}$	$\overline{W}$	I/O OPERATION
Standby	H	X	X	High Z
Output Disabled	L	H	H	High Z
Read	L	L	H	D_{OUT}
Write	L	X	L	D_{IN}

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SPECIALTY MEMORIES

MOSEL is developing a comprehensive family of specialty memory products, including second sources of popular architectures of FIFOs, Dual Port SRAMs, and Video Color Palette products. In addition, MOSEL is pioneering new memory standards such as the Latch RAM for microcontroller applications shown in this section, Parity RAMs, Cache products (Section 6), and Voice ROM products (Section 5), with more specialty memory families to follow in the future.

FIFOS

In FIFOs, MOSEL offers the widest range of x9 devices available, ranging from the 256 x 9 to the 4K x 9. We offer both low and standard power versions as well as a variety of speeds ranging from 10 to 30MHz. All of MOSEL's standard x9 FIFOs are cascadable in depth and width and are pin and function compatible, making density upgrades simple. Two DIP (300 & 600mils) and surface mount (32-pin PLCC & 330mil SOG) package types are offered. Plus MOSEL is one of the first companies in the industry to offer the 4K x 9 in a 300mil DIP and 330mil SOG. MOSEL also offers two parallel-to-serial FIFOs, the MS72105 (256 x 16 to 1) and the MS72115 (512 x 16 to 1). These FIFOs are well suited for any serial data output buffers such as are found in laser printers, fax machines, LANs, video frame buffers, disk and tape controllers.

DUAL PORT

Presently, MOSEL offers one Dual Port SRAM in the 1K x 8 size. However, we plan on offering further extensions to the product line later this year starting with an 8K x 8. Dual Ports provide two independent ports with separate control, address and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature, controlled by chip enable, permits the on-chip circuitry of each port to enter a very low standby power mode. The 1K x 8 is offered in a 48-pin DIP.

LATCH RAM

The Latch RAM family of products is a new line of SRAMs with on-chip transparent address latches that retain memory address information. These devices were created to interface with microcontrollers that have multiplexed address and data on the same pins (such as the Intel 8051). Because the typical microcontroller application is usually price sensitive, MOSEL will offer finer gradations of memory sizes that include a 4K x 8, 8K x 8, 12K x 8, 16K x 8 and 32K x 8. This allows the designer to purchase only the amount of memory necessary for the application. All of the products are offered in multiple speeds with power down chip enable and are packaged in both 28 pin 300mil DIP and 330mil SOG.

VIDEO COLOR PALETTE

MOSEL's MS176 is an Inmos IMSG176/171 compatible Video Color Palette typically used for VGA graphics applications. The MS176 is offered at 35 and 50 MHz in 600 mil DIP and 44 pin PLCC packages. The MS177 currently under development is function compatible with the MS176, but offers a power down mode to significantly reduce standby power for portable computer applications.

PARITY RAMs

For years systems designers have requested memory products that would facilitate designing memory subsystems that support parity. For years semiconductor suppliers have resisted. This year, MOSEL is introducing two Parity RAM products. The MS64100 is a 32K x 8 SRAM (32K x 9 internal) with on board parity generation and checking along with a Parity Error Signal. The MS64101 is a 32K x 9 SRAM for application where parity is generated and checked externally. Both products are offered at 25 and 35 ns, making them suitable for a variety of applications including high speed cache.

SUMMARY

With advances in memory technology, a single memory chip is enough for an increasing number of system applications. Previously, when multiple memory chips were required for these applications, the path to improving price performance was to increase the density of memory chip until only one memory chip was needed. For these applications, the path to future price performance improvement is to increase the level of functional integration, That is, to add logic and/or analog functions on chip with the memory array and in the process create new specialty memory architectures.

MOSEL is committed to pioneering and second sourcing new specialty memory architectures to create new standards for applications specific memory products. If you would like more information about MOSEL's specialty memory products, please contact your local MOSEL sales representative or franchise distributor listed in this book.

256 x 18 Video Color Palette

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FEATURES

- RGB analog outputs, 6-bit DAC per channel with composite blank.
- Combines high speed Color Palette RAM and Triple Video DAC.
- Displays 256 colors simultaneously from a palette of 256K colors.
- Supports pixel rates up to 50 MHz.
- Direct replacement for INMOS G171 and G176.
- Up to 6-bit per pixel resolution.
- Directly drives singly or doubly terminated 75Ω transmission lines.
- Pixel word mask for single cycle color updates.
- Asynchronous microprocessor compatible interface.
- TTL compatible inputs, single 5V ± 10% power supply.
- Packaged in JEDEC standard 28 pin 600 mil DIP and 44 pin PLCC packages.

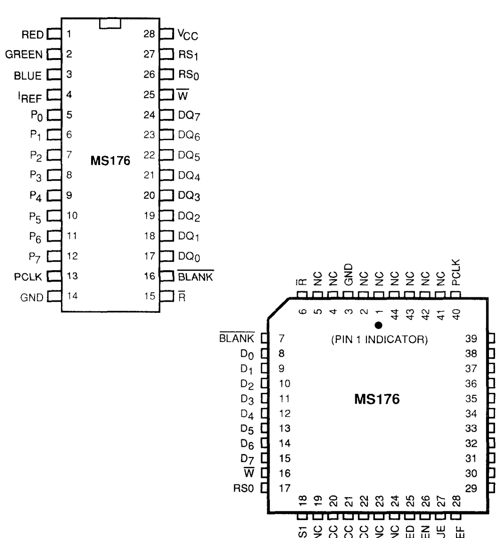
GENERAL DESCRIPTION

The MOSEL MS176 is a high speed RAMDAC designed for video graphics applications. It combines a 256 x 18 color look-up table, triple 6-bit video digital to analog converters and an asynchronous bidirectional microprocessor interface into a single device.

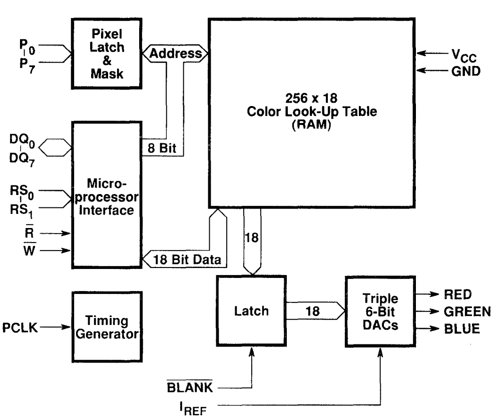
The MS176 can display 256 colors selected from a total of 256K colors. The on-chip pixel word mask allows displayed colors to be changed in a single write cycle rather than by modifying the color look-up table. Each of the RED, GREEN and BLUE analog output signals can drive a single or doubly terminated 75Ω transmission line directly.

Intended for high-resolution graphics applications, the MOSEL MS176 is available with pixel rates ranging from 40 MHz to 50 MHz. It is a direct pin and function replacement for the Inmos G-171 and G-176, and is fully compatible with VGA industry standards. The MS176 is offered in a JEDEC standard 28-pin, 600 mil plastic DIP and 44 pin PLCC packages.

PIN CONFIGURATIONS



FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

ANALOG INTERFACE

RED, GREEN, BLUE Color Signal Outputs

These three signals are the outputs of the three 6 bit video DACs. These signals drive a singly or doubly terminated (75Ω) transmission line. Each DAC is composed of a number of current sources whose outputs are summed. The number of active current sources is controlled by the applied binary value. A compatible monitor or video amplifier can be directly driven by these color signals.

I_{REF} Reference Current

I_{REF} provides a reference for the internal video DACs. I_{REF} must be driven by an external current sink providing a regulated current. The reference current drawn from V_{CC} through the I_{REF} pin determines the current sourced by each of the DACs current sources.

PIXEL INTERACE

PCLK Pixel Clock Input

The Pixel Clock is a positive edge triggered signal. It is used to latch the pixel addresses and the blanking signal. This clock also controls the three-stage pipeline of the color palette and DAC to the outputs. Each Pixel Clock period corresponds to one pixel displayed on the monitor.

P_0–P_7 Pixel Address Inputs

These 8 inputs are latched on the rising edge of PCLK. The value of these 8 inputs are ANDed with the corresponding bits of the Pixel Mask Register. The resulting address is used to specify the desired RAM word in the color look-up table. This 18 bit wide color value is then output to the DACs.

$\overline{\text{BLANK}}$ Blanking Control Input

The blanking control input is active LOW, and is latched on the rising edge of PCLK. The $\overline{\text{BLANK}}$ signal is used for blanking the display during retrace. When $\overline{\text{BLANK}}$ is LOW the color value from the look-up table is ignored and the DAC outputs are forced to the blanking level. $\overline{\text{BLANK}}$ has the same pipeline delay as P_0–P_7.

DIGITAL INTERFACE

$\overline{R}$ Read Enable Input

The read enable input is active LOW. When active, output data will be present at the DQ pins. The values of the register select inputs are latched on the falling edge of $\overline{R}$ and are decoded to determine the source of the output data. When $\overline{R}$ is HIGH, the DQ pins will be in the high-impedance state.

$\overline{W}$ Write Enable Input

The write enable input is active LOW. When active, data present at the DQ pins will be written into the device. The values of the register select inputs are latched on the falling edge of $\overline{W}$ and are decoded to determine the destination of the write data.

RS_0–RS_1 Register Select Inputs

The value of these inputs specifies which of the internal registers is to be read or written. The values of these inputs are latched at the beginning of a read or write cycle. The cycle begins on the falling edge of either the $\overline{R}$ or $\overline{W}$ input.

DQ_0–DQ_7 Data Input/Output Ports

These 8 bidirectional ports are used to read data from or write data to the device internal registers. The Pixel Address Register and the Pixel Mask Register use all 8 bits, the Color Value Register uses only the lower six bits (DQ_0–DQ_5).

V_{CC} Positive Power Supply

GND Ground

TABLE 1. REGISTER SELECT TRUTH TABLE

RS_1	RS_0	REGISTER ASSIGNMENT
0	0	Pixel Address Register (RAM Write)
1	1	Pixel Address Register (RAM Read)
0	1	Color Value Register
1	0	Pixel Mask Register

FUNCTIONAL DESCRIPTION

The MOSEL MS176 is designed for use as the output stage of a raster scan video system. This high speed video color palette combines a 256 x 18 color look-up table, triple 6-bit video digital to analog converters and an asynchronous bidirectional microprocessor interface into a single compact package.

The MS176 consists of three distinct sections. The first section includes the pixel address, timing and $\overline{\text{BLANK}}$ information. The second section contains the color look-up table and the three video DACs, while the third section is the digital microprocessor interface.

Video Path

The pixel address inputs P_0–P_7 are latched on the rising edge of PCLK. The value of these 8 inputs are ANDed with the corresponding bits of the pixel mask register before being passed as an address to the color look-up table. The contents of the specified location are then transferred to the video DACs.

The $\overline{\text{BLANK}}$ signal is used to blank the display during retrace. The $\overline{\text{BLANK}}$ input is latched at the same time as P_0–P_7, and is delayed internally so that it arrives at the analog outputs synchronized with the pixel stream. When $\overline{\text{BLANK}}$ is LOW the color value from the look-up table is ignored and the video DAC outputs are forced to the blanking level.

Microprocessor Interface

The microprocessor interface is used to read to and write from the color look-up table as well as the pixel mask register. The microprocessor interface is internally synchronized so that operations may occur at any time without waiting for retrace. Table 1 shows the microprocessor interface registers and how they are addressed.

Writing to the Color Look-Up Table

In order to define a new color value, the desired address in the color look-up table must first be written to the Pixel Address Register (RAM write). The appropriate values are set on the register select pins (RS_0–RS_1). This is latched on the falling edge of $\overline{W}$. The desired address is set on pins DQ_0–DQ_7 and is loaded into the Pixel Address Register. Following this, the values for the red, green and blue intensities are then written into the Color Value Register. This is accomplished by three additional write cycles (with the Color Value Register selected by the register select inputs). The Color Value Register loads only the values on DQ_0–DQ_5.

After the blue value is loaded on the third write cycle, the contents of the Color Value Register are written to the selected address in the color look-up table, and the Pixel Address Register is automatically incremented. This allows color values to be defined for sequential locations with no need to rewrite the Pixel Address Register.

3

Reading from the Color Look-Up Table

To read a color value contained in the look-up table the desired address must first be written to the Pixel Address Register (RAM read). The appropriate values are set on the register select pins (RS_0–RS_1). This is latched on the falling edge of $\overline{W}$. The desired address is set on pins DQ_0–DQ_7 and is loaded into the Pixel Address Register. The contents of the specified location are written into the Color Value Register and the Pixel Address Register is automatically incremented.

The red, green and blue values are then read by a sequence of three read cycles (with the Color Value Register Selected by the register select inputs). The values are output on DQ_0–DQ_5. After the blue value is read on the third cycle, the contents of the location specified by the Pixel Address Register (which has already been incremented) are written into the Color Value Register. This allows color values to be read for sequential locations with no need to rewrite the Pixel Address Register.

Reading and Writing the Pixel Mask Register

The Pixel Mask Register is written to in a similar fashion as the Pixel Address Register. The appropriate values for selecting the Pixel Mask Register are set on the register select pins, the desired contents are placed on DQ_0–DQ_7, and a single write cycle is executed. The contents of the Pixel Mask Register may be read by placing the appropriate values on the register select pins and executing a single read cycle. The contents of the Pixel Mask Register can then be read on DQ_0–DQ_7.

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	PARAMETER	VALUE	UNITS
V_{CC}	V_{CC} Supply Voltage	7.0	V
V_{TERM}	Voltage on All Other Pins	−1.0 to V_{CC} +0.5	V
t_{BIAS}	Temperature Under Bias	−40 to +85	°C
t_{STG}	Storage Temperature	−60 to +150	°C
I_{REF}	Reference Current	−15	mA
I_O	Analog Output Current [2]	45	mA
I_{OUT}	DC Digital Output Current [3]	25	mA
P_D	Power Dissipation	1	W

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Per output
3. One output at a time, maximum one second duration.

OPERATING RANGE

RANGE	AMBIENT TEMPERATURE	V_{CC}
Commercial	0°C to 70°C	5V ± 10%

CAPACITANCE [1,2]

SYMBOL	PARAMETER	CONDITIONS	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN}=0V	7	pF
C_{DQ}	Digital Input/Output Capacitance	V_{DQ}=0V $\overline{R}$=V_{IH}	7	pF
C_{OA}	Analog Output Capacitance	V_{OA}=0V $\overline{BLANK}$=V_{IL}	10	pF

1. This parameter is guaranteed and not tested.
2. T_A = 25°C, f = 1.0 MHz.

DC ELECTRICAL CHARACTERISTICS (over the operating range)

DIGITAL INTERFACE

PARAMETER NAME	PARAMETER	TEST CONDITIONS	MIN.	TYP. [1]	MAX.	UNITS
V_{IL}	Guaranteed Input LOW Voltage [2][3]		−0.5	—	+0.8	V
V_{IH}	Guaranteed Input HIGH Voltage [2]		2.0	—	V_{CC}+0.5	V
I_{REF}	Reference Current		−7.0	−8.88	−10	mA
V_{REF}	Voltage I_{REF} Input (pin 4)		V_{CC}−3	—	V_{CC}	V
V_{OL}	Output LOW Voltage	V_{CC}=Min, I_{OL}=5mA	—	—	0.4	V
V_{OH}	Output HIGH Voltage	V_{CC}=Min, I_{OH}=−5mA	2.4	—	—	V
I_{IN}	Input Leakage Current	V_{CC}=Max, V_{SS}≤V_{IN}≤V_{CC}	—	—	±10	µA
I_{OLK}	Output Leakage Current	V_{CC} = Max, V_{SS}≤V_{IN}≤V_{CC}, $\overline{R}$≥V_{IH}	—	—	±50	µA
I_{CC}	Operating Power Supply Current	V_{CC}=Min, I_O=Max, I_{DQ}=0mA, F=F_{MAX} [4]	—	120	180	mA

ANALOG INTERFACE

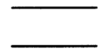
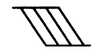
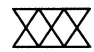
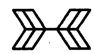
PARAMETER NAME	PARAMETER	TEST CONDITIONS	MIN.	TYP. [1]	MAX.	UNITS
V_O (max)	Analog Output Voltage	I_O≤10mA	—	—	1.5	V
I_O (max)	Analog Output Current	V_O≤1V	21	—	—	mA
	Full Scale Error	[5, 6]	—	—	±5	%
	DAC to DAC Correlation	[6, 7, 11]	—	—	±2	%
	Integral Non-Linearity	[8, 11]	±0.5	—	—	LSB
	Full Scale Settling Time	MS176-50 [9, 10, 11]	—	—	20	ns
		MS176-40 [9, 10, 11]	—	—	28	ns
	Rise Time (10% to 90%)	[10, 11]	—	—	6	ns
	Glitch Energy	[10, 11]	—	—	200	pV_{SEC}

NOTES:
1. Typical characteristics are at V_{CC} = 5.0V, T_A = 25°C.
2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
3. V_{IL} (min) = −1.0V for pulse width < 10ns.
4. F_{MAX} = $1/t_{CHCH}$
5. Full scale error is measured from the value derived from the design equation.
6. R_L = 37.5Ω, I_{REF} = −8.88 mA.
7. About the mid-point of the distribution of the three DACs measured at full scale deflection.
8. Measured from least squares best fit line. Monotonicity is guaranteed.
9. Measured from a 2% change in the output voltage until settling to within 2% of the final value.
10. I_{REF} = −8.88 mA, R_L = 37.5Ω, C_L = 30pF as shown in Figure 2a.
11. This parameter is sampled but not 100% tested.

AC TEST CONDITIONS

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times (10% to 90%)	3ns
Digital Input Timing Reference Level	1.5V
Digital Output Timing Reference Level	0.8V and 2.4V

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

AC TEST LOADS AND WAVEFORMS

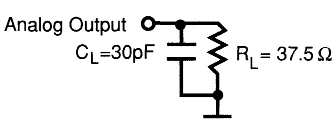


Figure 1a

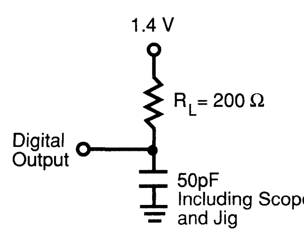


Figure 1b

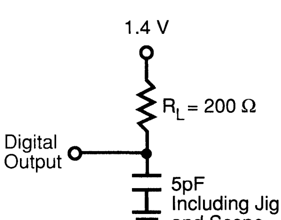


Figure 1c

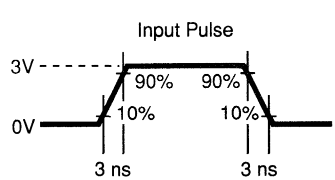


Figure 2

AC ELECTRICAL CHARACTERISTICS (over the operating range)

VIDEO OPERATION

NO.	PARAMETER NAME	PARAMETER	MS176-50 MIN.	MS176-50 MAX.	MS176-40 MIN.	MS176-40 MAX.	UNITS
1	t_{CHCH}	PCLK Period	20	—	25	—	ns
2	t_{CLCH}	PCLK Width LOW	6	—	9	—	ns
3	t_{CHCL}	PCLK Width HIGH	6	—	7	—	ns
4	Δt_{CHCH}	PCLK Jitter (1)	—	±2.5	—	±2.5	%
5	t_{PVCH}	Pixel Word Setup Time (2)	4	—	4	—	ns
6	t_{CHPX}	Pixel Word Hold Time (2)	4	—	4	—	ns
7	t_{BVCH}	$\overline{\text{BLANK}}$ Setup Time	4	—	4	—	ns
8	t_{CHBX}	$\overline{\text{BLANK}}$ Hold Time	4	—	4	—	ns
9	t_{CHAV}	PCLK to DAC Output Valid (3)	5	30	5	30	ns
10	Δt_{CHAV}	DAC to DAC Skew (4)	—	2	—	2	ns

READ CYCLE

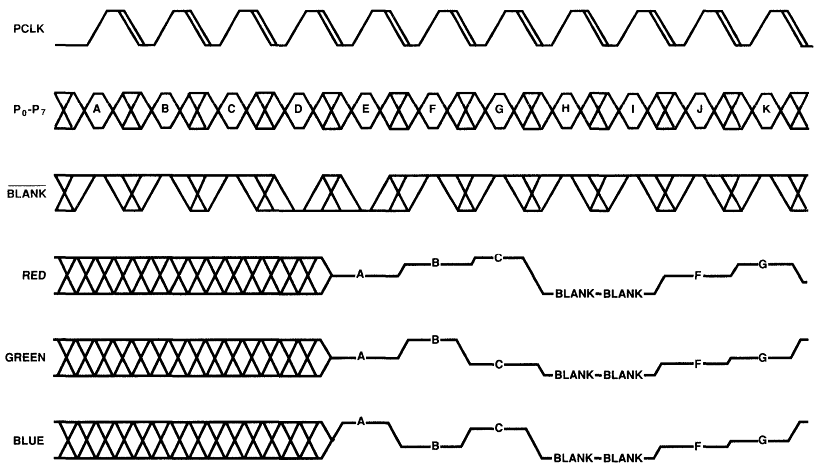
NO.	PARAMETER NAME	PARAMETER	MS176-50 MIN.	MS176-50 MAX.	MS176-40 MIN.	MS176-40 MAX.	UNITS
11	t_{RLRH}	Read Pulse Width	50	—	50	—	ns
12	t_{SVRL}	Register Select Setup Time	10	—	15	—	ns
13	t_{RLSX}	Register Select Hold Time	10	—	15	—	ns
14	t_{RLQX}	Read Enable to Output in Low Z	5	—	5	—	ns
15	t_{RLQV}	Read Enable to Output Valid	—	40	—	40	ns
16	t_{RHQX}	Output Hold Time	5	—	5	—	ns
17	t_{RHQZ}	Read Disable to Output in High Z (5)	—	20	—	20	ns
18	t_{RHRL1}	Successive Read Interval (6)	$3(t_{CHCH})$	—	$3(t_{CHCH})$	—	ns
19	t_{RHWL1}	Read Write Interval (6)	$3(t_{CHCH})$	—	$3(t_{CHCH})$	—	ns
20	t_{RHRL2}	Read After Color Read Interval (6)	$6(t_{CHCH})$	—	$6(t_{CHCH})$	—	ns
21	t_{RHWL2}	Write After Color Read Interval (6)	$6(t_{CHCH})$	—	$6(t_{CHCH})$	—	ns

WRITE CYCLE

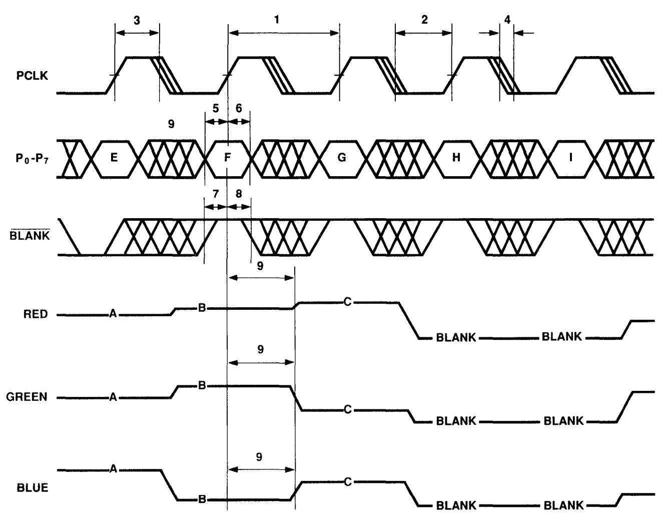
NO.	PARAMETER NAME	PARAMETER	MS176-50 MIN.	MS176-50 MAX.	MS176-40 MIN.	MS176-40 MAX.	UNITS
22	t_{WLWH}	Write Pulse Width	50	—	50	—	ns
23	t_{SVWL}	Register Select Setup Time	10	—	15	—	ns
24	t_{WLSX}	Register Select Hold Time	10	—	15	—	ns
25	t_{DVWH}	Data Setup to $\overline{\text{W}}$ High	10	—	15	—	ns
26	t_{WHDX}	Data Hold From $\overline{\text{W}}$ High	5	—	5	—	ns
27	t_{WHWL1}	Successive Write Interval (6)	$3(t_{CHCH})$	—	$3(t_{CHCH})$	—	ns
28	t_{WHRL1}	Write to Read Interval (6)	$3(t_{CHCH})$	—	$3(t_{CHCH})$	—	ns
29	t_{WHWL2}	Write After Color Write Interval (6)	$3(t_{CHCH})$	—	$3(t_{CHCH})$	—	ns
30	t_{WHRL2}	Read After Color Write Interval (6)	$3(t_{CHCH})$	—	$3(t_{CHCH})$	—	ns
31	t_{WHRL3}	Read After Read Address Write (6)	$6(t_{CHCH})$	—	$6(t_{CHCH})$	—	ns

NOTES:
1. This parameter is the allowed pixel clock frequency variation. It does not permit the pixel clock to vary outside the minimum value for PCLK period (t_{CHCH}).
2. Pixel address inputs must be set to a valid logic level with the appropriate setup and hold time at each rising edge of PCLK (this requirement includes the blanking period).
3. Valid DAC output is measured at the 50% point between successive DAC values.
4. Between different analog outputs on the same device.
5. Transition is measured ±200mV from steady state output voltage with C_L = 5pF as shown in Figure 1C. This parameter is guaranteed and not 100% tested.
6. This parameter allows synchronization between operations on the microprocessor interface and the pixel stream being processed by the color palette.

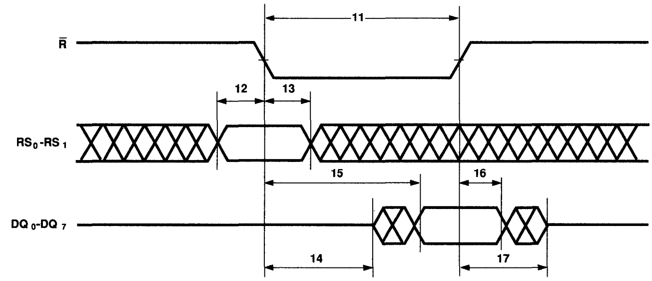
SYSTEM TIMING DIAGRAM



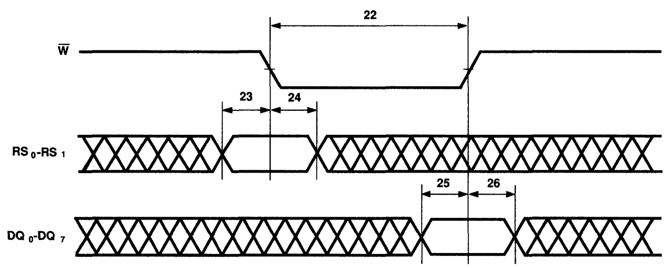
TIMING DIAGRAM DETAILING TIMING SPECIFICATIONS



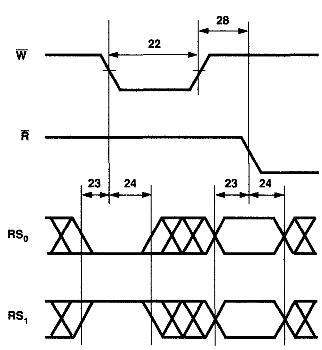
BASIC READ CYCLE



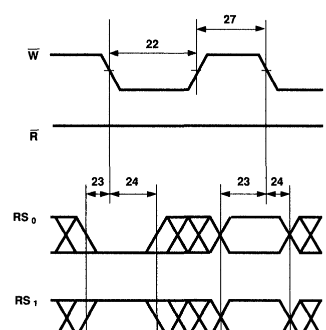
BASIC WRITE CYCLE



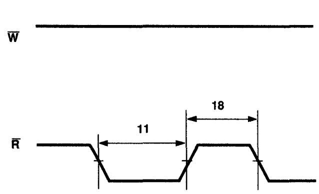
WRITE TO PIXEL MASK REGISTER FOLLOWED BY READ



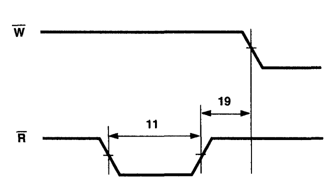
WRITE TO PIXEL MASK REGISTER FOLLOWED BY WRITE



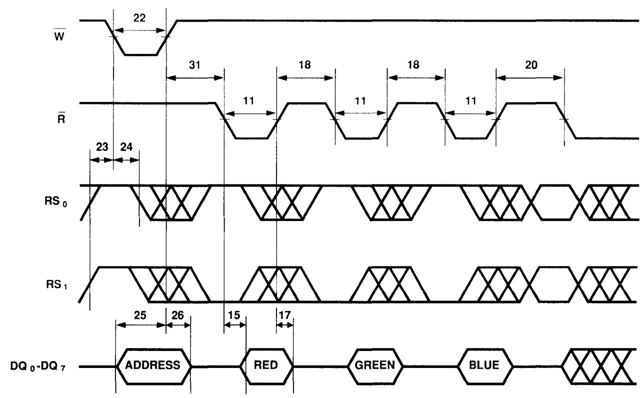
READ FROM PIXEL MASK OR PIXEL ADDRESS REGISTER (READ OR WRITE MODE) FOLLOWED BY READ



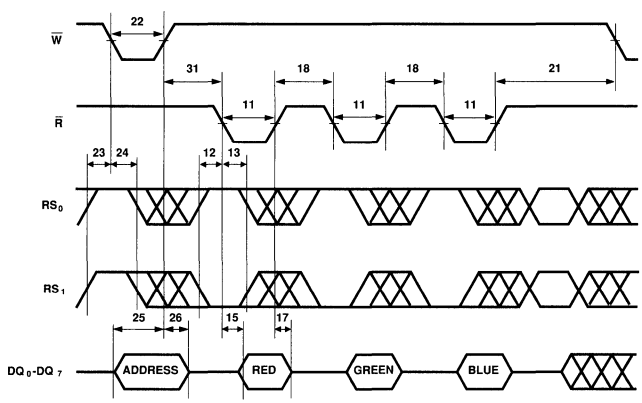
READ FROM PIXEL MASK OR PIXEL ADDRESS REGISTER (READ OR WRITE MODE) FOLLOWED BY WRITE



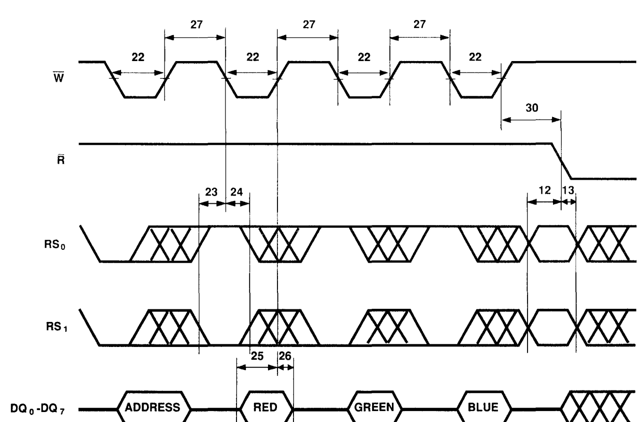
COLOR VALUE READ FOLLOWED BY ANY READ



COLOR VALUE READ FOLLOWED BY ANY WRITE

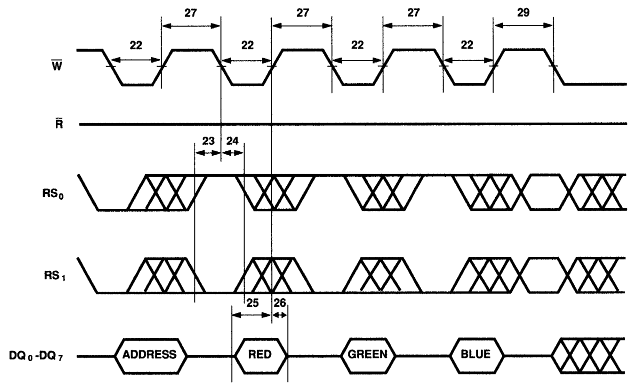


COLOR VALUE WRITE FOLLOWED BY ANY READ

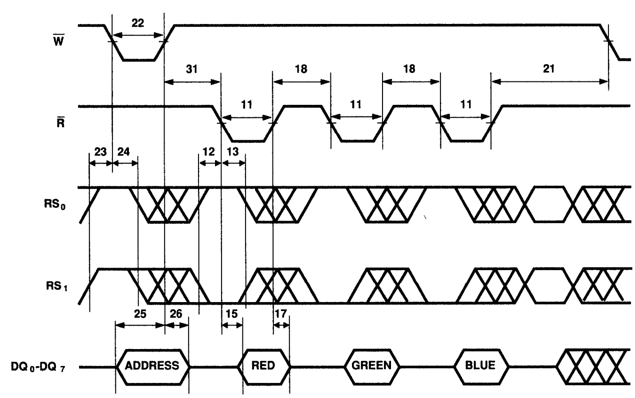


3

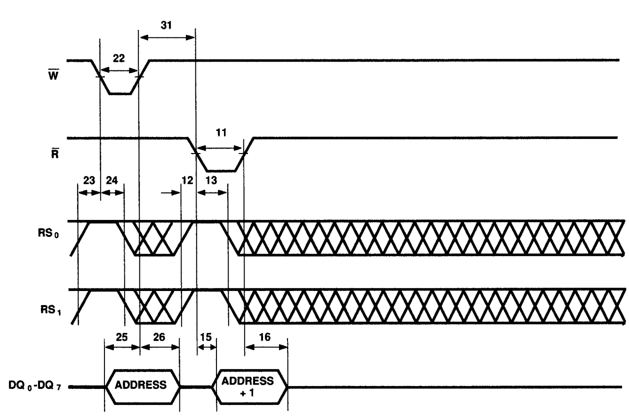
COLOR VALUE WRITE FOLLOWED BY ANY WRITE



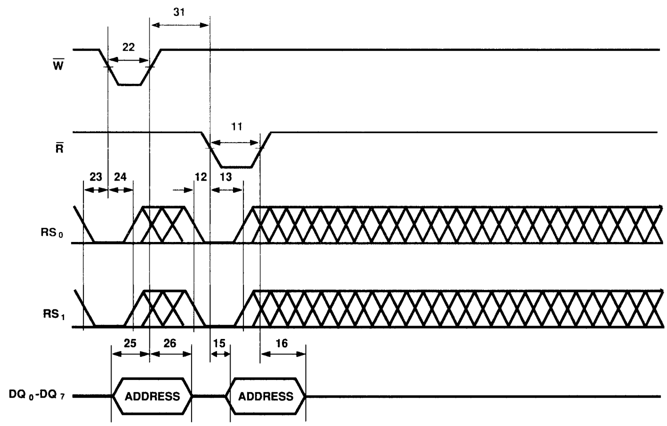
READ COLOR VALUE THEN READ PIXEL ADDRESS REGISTER (RAM READ)



WRITE AND READ BACK PIXEL ADDRESS REGISTER (READ MODE)



WRITE AND READ BACK PIXEL ADDRESS REGISTER (RAM WRITE)



SYSTEM APPLICATIONS NOTES

Current Reference Decoupling

The DACs in the MOSEL MS176 are composed of switched current sources which are based around a current mirror. The total current output of each DAC is determined by the number of active current sources and the reference current I_{REF}. I_{REF} develops a voltage reference relative to V_{CC} for the current mirror. Voltage variation in V_{CC} not managed by the current reference circuit will result in variations in the DAC output current. If the bandwidth of the current reference circuit is not sufficient to track these V_{CC} variations, it is recommended that a high frequency capacitor in parallel with a larger capacitor be used to couple the I_{REF} input to V_{CC}. This will enable the current source to track both high and low frequency variations of V_{CC}. (A coupling capacitor in the range of 47 to 100 µF is appropriate for most applications.) If the variations of V_{CC} are minor, or are controlled by the reference circuit, then a coupling capacitor should not be used.

Power Supply

The MOSEL MS176 is a high speed device. During operation it may draw large transient currents from the power supply. To ensure proper operation good high frequency board layout techniques and power supply distribution should be used.

ORDERING INFORMATION

SPEED	ORDERING PART NUMBER	PACKAGE REFERENCE NO.	TEMPERATURE RANGE
40 MHZ	MS176-40JC	J44-2	0°C to + 70°C
40 MHZ	MS176-40PC	P28-1	0°C to + 70°C
50 MHZ	MS176-50JC	J44-2	0°C to + 70°C
50 MHZ	MS176-50PC	P28-1	0°C to + 70°C

PRELIMINARY

256 x 18 Video Color Palette with Power Down

FEATURES

- Combines high speed Color Palette RAM and Triple Video DAC.
- Power-Down mode requires only 2mA max. supply current. Excellent for laptop or battery backup systems.
- Displays 256 colors simultaneously from a palette of 256K colors.
- RGB analog outputs, 6-bit DAC per channel with composite blank.
- Supports pixel rates up to 65 MHz.
- Operates with either current or voltage reference
- Up to 6-bit per pixel resolution.
- Directly drives singly or doubly terminated 75Ω transmission lines.
- Pixel word mask for single cycle color updates.
- Asynchronous microprocessor compatible interface.
- TTL compatible inputs, single 5V ± 10% power supply.
- Packaged in JEDEC standard 44 pin PLCC package.

GENERAL DESCRIPTION

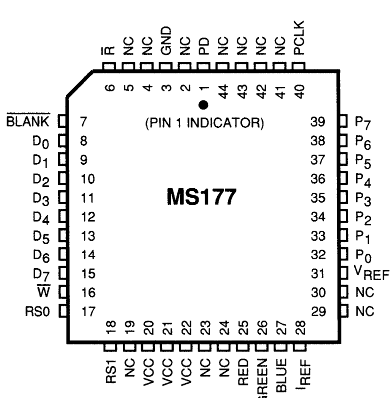
The MOSEL MS177 is a high speed RAMDAC designed for video graphics applications. It combines a 256 x 18 color look-up table, triple 6-bit video digital to analog converters and an asynchronous bidirectional microprocessor interface into a single device.

Designed to support laptop and battery backed-up systems, the MS177 offers a special power-down mode. In this mode the palette clock and analog current sources are shut down, reducing supply current to only 2 mA maximum. It also supports both current and voltage reference modes, and offers differential and integral linearity errors of less than 0.5 LSB over the full temperature and voltage range.

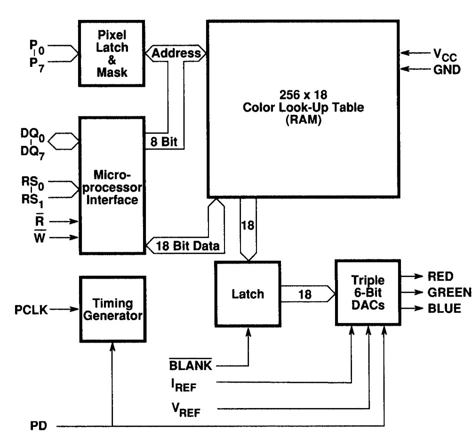
The MS177 can display 256 colors selected from a total of 256K colors. The on-chip pixel word mask allows displayed colors to be changed in a single write cycle rather than by modifying the color look-up table. Each of the RED, GREEN and BLUE analog output signals can drive a single or doubly terminated 75Ω transmission line directly.

Intended for high-resolution graphics applications, the MOSEL MS177 is available with pixel rates ranging from 40 MHz to 65 MHz. and is fully compatible with VGA industry standards. It is pin compatible with the Brooktree Bt471 and can replace that device when overlay registers are not used. The MS177 is offered in the JEDEC standard 44 pin PLCC package.

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



MOSEL Corporation 914 West Maude Avenue, Sunnyvale, CA 94086 U.S.A. 408-733-4556

MOSEL MS6130

1K x 8 CMOS Dual Port SRAM

3

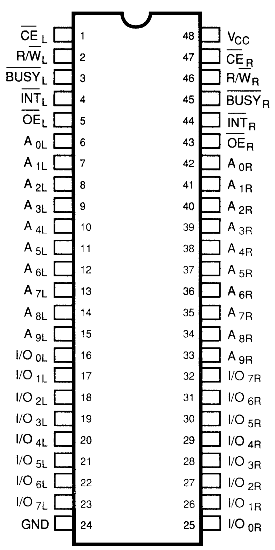
FEATURES

- High-speed–55/70/90ns (Max.)
- Low Power dissipation
  325mW (Typ.) Operation
  5 μW (Typ.) Standby
- Single 5V power supply
- Fully static operation
- All inputs and outputs directly TTL compatible
- Three state outputs
- Data retention supply voltage: 2.0-5.5V
- Fully asynchronous operation from either port
- On-chip arbitration logic
- Interrupt ($\overline{INT}$) and busy ($\overline{BUSY}$) flags
- Open drain outputs – $\overline{BUSY}$ and $\overline{INT}$

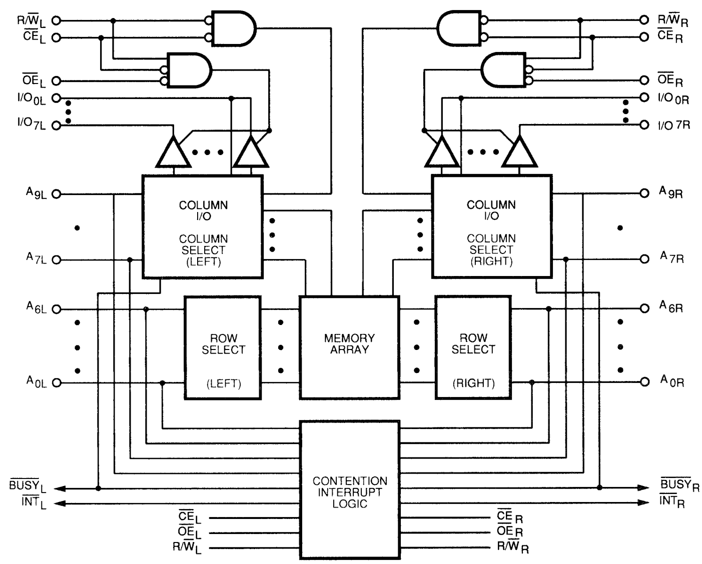
DESCRIPTION

The MOSEL MS6130 is a 8,192 bit dual port static random access memory organized as 1,024 words by 8 bits. It is built with MOSEL's high performance twin tub CMOS process. Eight-transistor full CMOS memory cell provides low standby current and high reliability. The low power (L) version offers a battery backup data retention capability where the circuit typically consumes only 2 μW off a 2V battery. The MS6130 is packaged in a 48-pin 600 mil-DIP.

PIN CONFIGURATIONS



FUNCTIONAL BLOCK DIAGRAM



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PIN DESCRIPTIONS

LEFT PORT	RIGHT PORT	NAMES
$\overline{CE}_L$	$\overline{CE}_R$	CHIP ENABLE
$R/\overline{W}_L$	$R/\overline{W}_R$	READ/WRITE ENABLE
$\overline{OE}_L$	$\overline{OE}_R$	OUTPUT ENABLE
$\overline{BUSY}_L$	$\overline{BUSY}_R$	BUSY FLAG
$\overline{INT}_L$	$\overline{INT}_R$	INTERRUPT FLAG
A_{0L}-A_{9L}	A_{0R}-A_{9R}	ADDRESS
I/O_{0L}-I/O_{7L}	I/O_{0R}-I/O_{7R}	DATA INPUT/OUTPUT
V_{CC}		POWER
GND		GROUND

OPERATING RANGE

RANGE	AMBIENT TEMPERATURE	Vcc
Commercial	0°C to + 70°C	5V ± 10%

FUNCTIONAL DESCRIPTION

The MS6130 provides two ports with separate controls, address and I/O that permit independent access for reads or writes to any location in memory. The MS6130 has an automatic power-down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power-down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ($\overline{OE}$). In the read mode, the port's $\overline{OE}$ turns on the output drivers when set LOW. Non-contention READ/WRITE conditions are illustrated in Table 1.

The interrupt ($\overline{INT}$) permits communication between ports or systems. If the user chooses to use the interrupt function a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ($\overline{INT}_L$) is set when the right port writes to memory location 3FE (HEX). The left port clears the interrupt by reading address location 3FE. Likewise, the right port interrupt flag ($\overline{INT}_R$) is set when the left port writes to memory location 3FF (HEX) and to clear the interrupt flag ($\overline{INT}_R$), the right port must read the memory location 3FF. The message (8-bits) at 3FE or 3FF is user-defined. If the interrupt function is not used, address location 3FE and 3FF are not used as mail boxes but as part of the random access memory. Refer to Table II for the interrupt operation. The $\overline{INT}$s have open drain drivers to allow OR-tied operation.

ARBITRATION LOGIC, FUNCTIONAL DESCRIPTION:

The arbitration logic will resolve an address match or a chip enable match down to 5ns minimum and determine which port has access. In all cases, an active $\overline{BUSY}$ flag will be set for the delayed port.

The $\overline{BUSY}$ flags are provided for the situation when both ports simultaneously access the same memory location. When this situation occurs, on-chip arbitration logic will determine which port has access and sets the delayed port's $\overline{BUSY}$ flag. $\overline{BUSY}$ is set at speeds that permit the processor to hold the operation and its respective address and data. It is important to note that the WRITE operation is invalid for the port that has $\overline{BUSY}$ set LOW. Both ports have READ access (valid data output) even the port that has $\overline{BUSY}$ set LOW. The delayed port will have access for WRITE operation when $\overline{BUSY}$ goes inactive.

Contention occurs when both left and right ports are active and both addresses match. When this situation occurs, the on-chip arbitration logic determines access. Two modes of arbitration are provided: (1) if the addresses match and are valid before $\overline{CE}$, on-chip control logic arbitration between $\overline{CE}_L$ and $\overline{CE}_R$ for access (refer to Table III, $\overline{CE}$ Arbitration); or (2) if the $\overline{CE}$s are low before an address match, on-chip control logic arbitrates between left and right addresses for access (refer to Table IV, Address Arbitration). In either mode of arbitration, the delayed port's $\overline{BUSY}$ flag is set and will reset when the port granted access completes its operation. The BUSYs are open drain outputs allowing OR-tied operation.

TRUTH TABLES

TABLE I – NON-CONTENTION READ/WRITE CONTROL

LEFT PORT INPUTS [(1)]			RIGHT PORT INPUT [(1)]			FLAGS[(2)]		
$R/\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	$R/\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	$\overline{BUSY}_L$	$\overline{BUSY}_R$	FUNCTION
X	H	X	X	X	X	H	H	Left Port in Power Down Mode
X	X	X	X	H	X	H	H	Right Port in Power Down Mode
L	L	X	X	X	X	H	H	Data on Left Port Written Into Memory
H	L	L	X	X	X	H	H	Data in Memory Output on Left Port
X	X	X	L	L	X	H	H	Data on Right Port Written Into Memory
X	X	X	H	L	L	H	H	Data in Memory Output on Right Port

NOTES:
1. $A_{0L} - A_{9L} \neq A_{0R} - A_{9R}$
2. $\overline{INT}$ Flags DON'T CARE
H = HIGH, L = LOW, X = DON'T CARE

TABLE II – INTERRUPT FLAG

LEFT PORT						RIGHT PORT						
$R/\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	A_{0L}-A_{9L}	$\overline{BUSY}_L$	$\overline{INT}_L$	$R/\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	A_{0R}-A_{9R}	$\overline{BUSY}_R$	$\overline{INT}_L$	FUNCTION
L	L	X	3FF	H	X	X	X	X	X	X	L	Set Right $\overline{INT}_R$ Flag
X	X	X	X	X	X	H	L	L	3FF	H	H	Reset Right $\overline{INT}_R$ Flag
X	X	X	X	X	L	L	L	X	3FE	H	X	Set Left $\overline{INT}_L$ Flag
H	L	L	3FE	H	H	X	X	X	X	X	X	Reset Left $\overline{INT}_L$ Flag

NOTE:
H = HIGH, L = LOW, X = DON'T CARE

TABLE III – $\overline{CE}$ ARBITRATION WITH ADDRESS MATCH BEFORE $\overline{CE}$

LEFT PORT				RIGHT PORT				FLAGS[(1)]		
$R/\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	A_{0L}-A_{9L}	$R/\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	A_{0R}-A_{9R}	$\overline{BUSY}_L$	$\overline{BUSY}_R$	FUNCTION
X	LBR	X	MATCH	X	L	X	MATCH	H	L	Left Operation Permitted Right WRITE Not Permitted
X	L	X	MATCH	X	LBL	X	MATCH	L	H	Left WRITE Not Permitted Right Operation Permitted
X	LST	X	MATCH	X	LST	X	MATCH	H	L	Arbitration Resolved

NOTE:
1. $\overline{INT}$ Flags DON'T CARE
X = DON'T CARE, L = LOW, H = HIGH, LST = Low Same Time, LBR = Low Before Right, LBL = Low Before Left.

TABLE IV – ADDRESS ARBITRATION WITH $\overline{CE}$ LOW BEFORE ADDRESS MATCH

LEFT PORT				RIGHT PORT				FLAGS[(1)]		
$R/\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	A_{0L}-A_{9L}	$R/\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	A_{0R}-A_{9R}	$\overline{BUSY}_L$	$\overline{BUSY}_R$	FUNCTION
X	L	X	VBR	X	L	X	VALID	H	L	Left Operation Permitted Right WRITE Not Permitted
X	L	X	VALID	X	L	X	VBL	L	H	Left WRITE Not Permitted Right Operation Permitted
X	L	X	VST	X	L	X	VST	H	L	Arbitration Resolved

NOTE:
1. $\overline{INT}$ Flags DON'T CARE
X = DON'T CARE, L = LOW, H = HIGH, VST = Valid Same Time, VBR = Valid Before Right, VBL = Valid Before Left.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	CONDITION	UNIT
V_{TERM}	Terminal Voltage with Repect to GND	–0.5 to +7.0	V
T_{BIAS}	Temperature Under Bias	–10 to +125	°C
T_{STG}	Storage Temperature	–40 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	20	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = 0 to +70°C)

SYMBOL	PARAMETER	TEST CONDITIONS	MS6130 MIN.	MS6130 TYP. [1]	MS6130 MAX.	MS6130L MIN.	MS6130L TYP. [1]	MS6130L MAX.	UNITS
$\lvert I_{LI}\rvert$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	—	10	—	—	5	µA
$\lvert I_{LO}\rvert$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0Vt o V_{CC}	—	—	10	—	—	5	µA
V_{IH}	Input High Voltage		2.2	—	6.0	2.2	—	6.0	V
V_{IL}	Input Low Voltage		–0.5	—	0.8	–0.5	—	0.8	V
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL}, Outputs Open	—	65	170	—	65	120	mA
I_{SB1}	Standby Current (Both Ports Standby)	$\overline{CE}_L$ and $\overline{CE}_R \geq V_{IH}$	—	25	40	—	25	30	mA
I_{SB2}	Standby Current (One Port Standby)	$\overline{CE}_L$ and $\overline{CE}_R \geq V_{IH}$ Active Port Outputs Open	—	40	110	—	40	75	mA
I_{SB3}	Full Standby Current (Both Ports Full Standby)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC}$ – 0.2V $V_{IN} \geq V_{CC}$ – 0.2V or $V_{IN} \leq$ 0.2V	—	0.001	0.5	—	0.001	0.1	mA
I_{SB4}	Full Standby Current (One Port Full Standby)	One Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC}$ – 0.2V $V_{IN} \geq V_{CC}$ – 0.2V or $V_{IN} \leq$ 0.2V Active Port Outputs Open	—	40	90	—	35	65	mA
V_{OL}	Output Low Voltage (I/O_0 - I/O_7)	I_{OL} = 3.5mA	—	—	0.4	—	—	0.4	V
		I_{OL} = 8mA	—	—	0.5	—	—	0.5	
V_{OL}	Open Drain Output Low Voltage ($\overline{BUSY}$, $\overline{INT}$)	I_{OL} = 16mA	—	—	0.5	—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = –4mA	2.4	—	—	2.4	—	—	V

NOTE:
1. V_{CC} = 5.0V, T_A = +25°C.

CAPACITANCE[1] (T_A = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}	Input/Output Capacitance	V_{OUT} = 0V	10	pF

1. This parameter is guaranteed and not 100% tested.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = 0 to +70°C, unless otherwise noted)[3]

SYMBOL	PARAMETER	MS6130-55 MS6130L-55 MIN.	TYP.	MAX.	MS6130-70 MS6130L-70 MIN.	TYP.	MAX.	MS6130-90 MS6130L-90 MIN.	TYP.	MAX.	UNITS
READ CYCLE											
t_{RD}	Read Cycle Time	55		—	70		—	90		—	ns
t_{AA}	Address Access Time	—		55	—		70	—		90	ns
t_{ACE}	Chip Enable Access Time	—		55	—		70	—		90	ns
t_{AOE}	Output Enable Access Time	—		30	—		35	—		40	ns
t_{OH}	Output Hold From Address Change	5		—	10		—	10		—	ns
t_{LZ}	Output Low Z Time[1,2]	5		—	5		—	5		—	ns
t_{HZ}	Output High Z Time[1,2]	—		30	—		35	—		40	ns
t_{PU}	Chip Enable to Power Up Time[2]	0		—	0		—	0		—	ns
t_{PD}	Chip Disable to Power Down Time[2]	—		35	—		40	—		50	ns
WRITE CYCLE											
t_{WC}	Write Cycle Time	55		—	70		—	90		—	ns
t_{EW}	Chip Enable to End of Write	50		—	65		—	85		—	ns
t_{AW}	Address Valid to End of Write	50		—	65		—	85		—	ns
t_{AS}	Address Setup Time	0		—	0		—	0		—	ns
t_{WP}	Write Pulse Width	40		—	45		—	60		—	ns
t_{WR}	Write Recovery Time	0		—	0		—	0		—	ns
t_{DW}	Data Valid to End of Write	30		—	35		—	40		—	ns
t_{HZ}	Output High Z Time[1,2]	—		30	—		35	—		40	ns
t_{DH}	Data Hold Time	0		—	0		—	0		—	ns
t_{WZ}	Write Enabled to Output in High Z[1,2]	0		30	0		35	0		40	ns
t_{OW}	Output Active From End of Write [1,2]	0		—	0		—	0		—	ns
BUSY TIMING											
t_{RC}	Read Cycle Time	55		—	70		—	90		—	ns
t_{WC}	Write Cycle Time	55		—	70		—	90		—	ns
t_{BAA}	$\overline{\text{BUSY}}$ Access Time to Address	—		30	—		35	—		45	ns
t_{BDA}	$\overline{\text{BUSY}}$ Disable Time to Address	—		30	—		35	—		45	ns
t_{BAC}	$\overline{\text{BUSY}}$ Access Time to Chip Enable	—		30	—		35	—		45	ns
t_{BDC}	$\overline{\text{BUSY}}$ Disable Time to Chip Enable	—		30	—		35	—		45	ns
t_{APS}	Arbitration Priority Set Up Time	5		—	5		—	5		—	ns
INTERRUPT TIMING											
t_{AS}	Address Set Up Time	0		—	0		—	0		—	ns
t_{WR}	Write Recovery Time	0		—	0		—	0		—	ns
t_{INS}	Interrupt Set Time	—		40	—		45	—		55	ns
t_{INR}	Interrupt Reset Time	—		40	—		45	—		55	ns

NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1, 2 & 3).
2. This parameter guaranteed but not tested.
3. A minimum 0.5 ms time delay is required after application of V_{CC} (5V) before device operation is achieved.

3

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5 ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1, 2, and 3

*Including scope and jig.

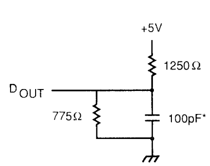


Figure 1
Output Load

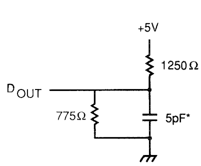


Figure 2
Output Load
(for t_{HZ}, t_{LZ}, and t_{OW})

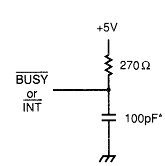
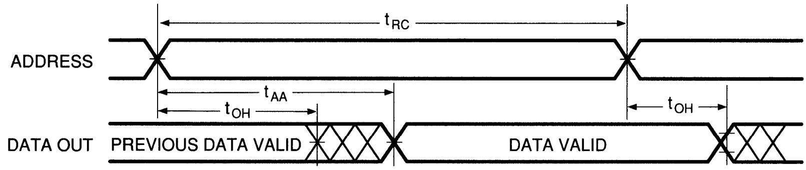


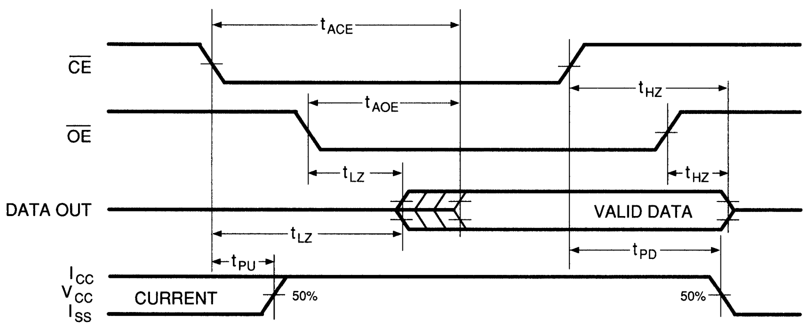
Figure 2
BUSY and INT
Output Load

TIMING WAVEFORMS

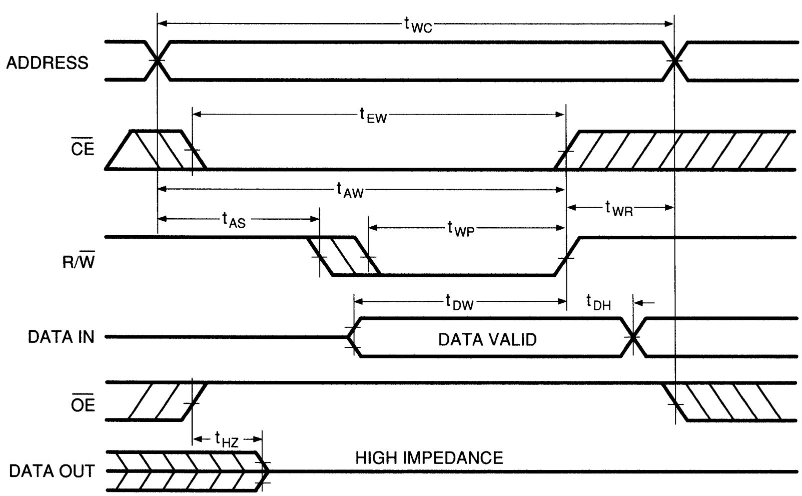
READ CYCLE NO. 1 EITHER SIDE (1,2,6)



READ CYCLE NO. 2 EITHER SIDE (1,3)

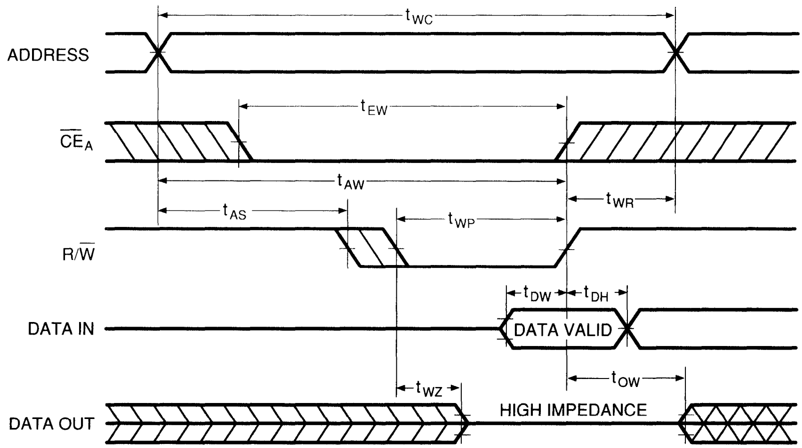


WRITE CYCLE NO. 1 EITHER SIDE (4,7)



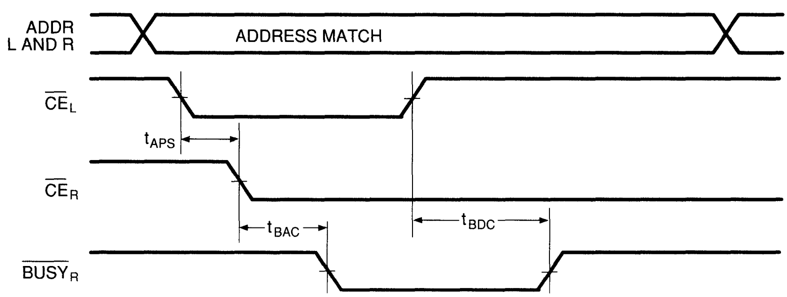
TIMING WAVEFORMS

WRITE CYCLE NO. 2 EITHER SIDE (4,7)

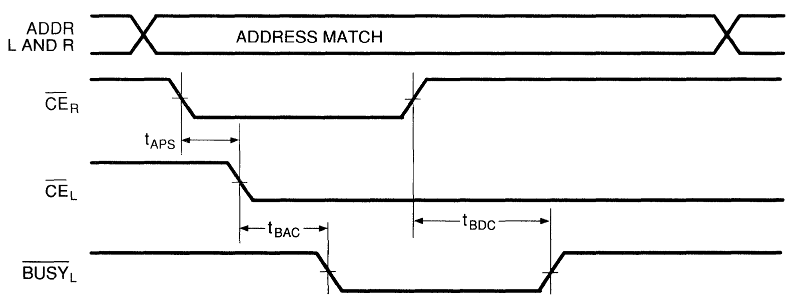


CONTENTION CYCLE NO. 1 $\overline{CE}$ ARBITRATION

$\overline{CE}_L$ VALID FIRST:



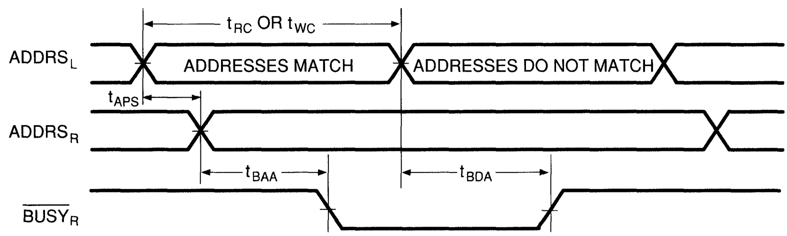
$\overline{CE}_R$ VALID FIRST:



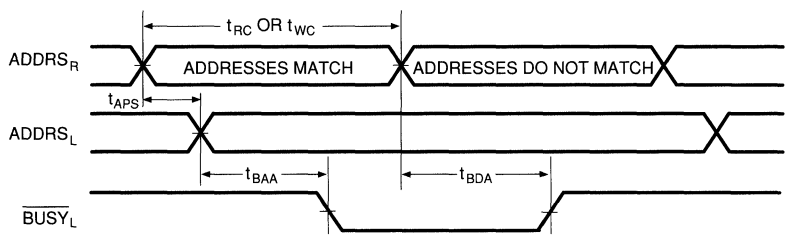
TIMING WAVEFORMS

CONTENTION CYCLE NO. 2 ADDRESS VALID ARBITRATION(5)

LEFT ADDRESS VALID FIRST:

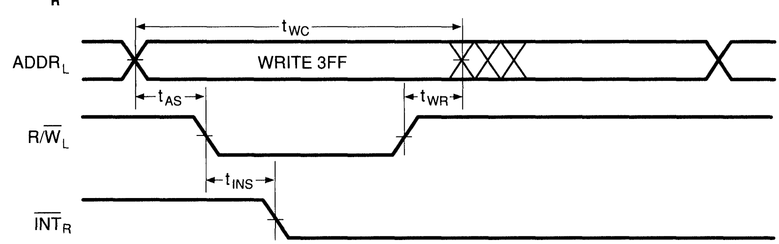


RIGHT ADDRESS VALID FIRST:

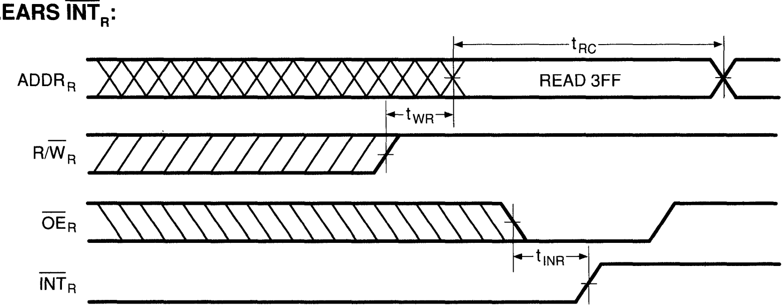


INTERRUPT MODE(5,8)

LEFT SIDE SETS $\overline{INT}_R$:

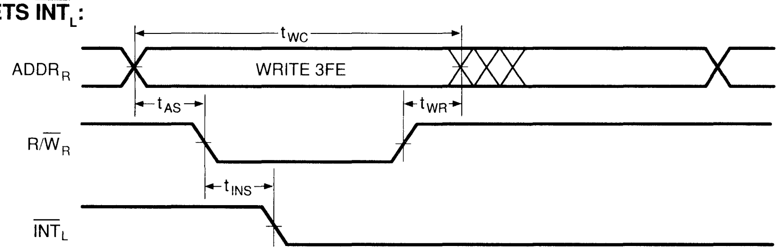


RIGHT SIDE CLEARS $\overline{INT}_R$:

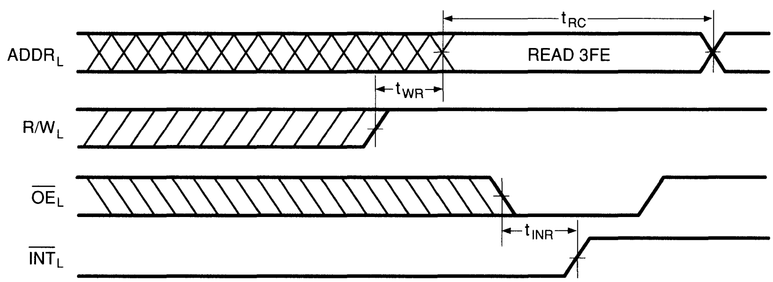


TIMING WAVEFORMS

RIGHT SIDE SETS $\overline{INT}_L$:



LEFT SIDE CLEARS $\overline{INT}_L$:



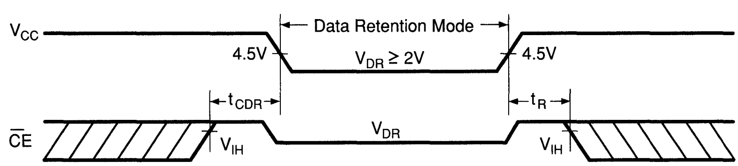
NOTES:
1. R/W is high for Read Cycles.
2. Device is continuously enabled, $\overline{CE} = V_{IL}$.
3. Addresses valid prior to or coincident with $\overline{CE}$ transition low.
4. If $\overline{CE}$ goes high simultaneously with R/$\overline{W}$ high, the outputs remain in the high impedance state.
5. $\overline{CE}_L = \overline{CE}_R = V_{IL}$.
6. $\overline{OE} = V_{IL}$.
7. R/$\overline{W}$ = V_{IH} during address transition.
8. $\overline{INT}_R$ and $\overline{INT}_L$ are reset (high) during power up.

DATA RETENTION CHARACTERISTICS (T_A = 0 to +70°C, L Version Only)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP. (1)	MAX.	UNIT
V_{DR}	V_{CC} for Data Retention		2.0	—	—	V
I_{CCDR}	Data Retention Current	V_{CC} = 2.0V	—	1.0	20	µA
t_{CDR}	Chip Deselect to Data Retention Time	$CS \geq V_{CC} - 2.0V$	0	—	—	ns
t_R	Operation Recovery Time	$V_{IN} \geq V_{CC} - 2.0V$ or $\leq 0.2V$	t_{RC}(2)	—	—	ns

NOTES:
1. T_A = 25°C
2. t_{RC} = Read Cycle Time

LOW V_{CC} DATA RETENTION WAVEFORM



ORDERING INFORMATION

SPEED (ns)	ORDERING PART NUMBER	PACKAGE REFERENCE NO.	TEMPERATURE RANGE
55	MS6130-55PC	P48-1	0°C to +70°C
55	MS6130L-55PC		0°C to +70°C
55	MS6130-55DC	D48-1	0°C to +70°C
55	MS6130L-55DC		0°C to +70°C
70	MS6130-70PC	P48-1	0°C to +70°C
70	MS6130L-70PC		0°C to +70°C
70	MS6130-70DC	D48-1	0°C to +70°C
70	MS6130L-70DC		0°C to +70°C
90	MS6130-90PC	P48-1	0°C to +70°C
90	MS6130L-90PC		0°C to +70°C
90	MS6130-90DC	D48-1	0°C to +70°C
90	MS6130L-90DC		0°C to +70°C

MOSEL

MS6134

ADVANCED INFORMATION

8K x 8 Dual-Port Static RAM

FEATURES

- High-speed access: 45/55/70ns available
- Low Power consumption

  Both ports active: 660mW
  Both ports standby: 1.1mW
- Wider word widths of 16-bits or more can easily be created by using the Master/Slave chip select and cascading more than one device
- On-chip arbitration logic
- Single $\overline{BE}$ pin for Master or Slave operation
- $\overline{INT}$ flag for port-to-port communication
- Fully asynchronous operation from either port
- Battery backup operation: 2 volts data retention
- TTL compatible, single 5V (± 10% power supply
- Available in a 64-lead gull wing plastic flatpack with 40mil lead spacing

DESCRIPTION

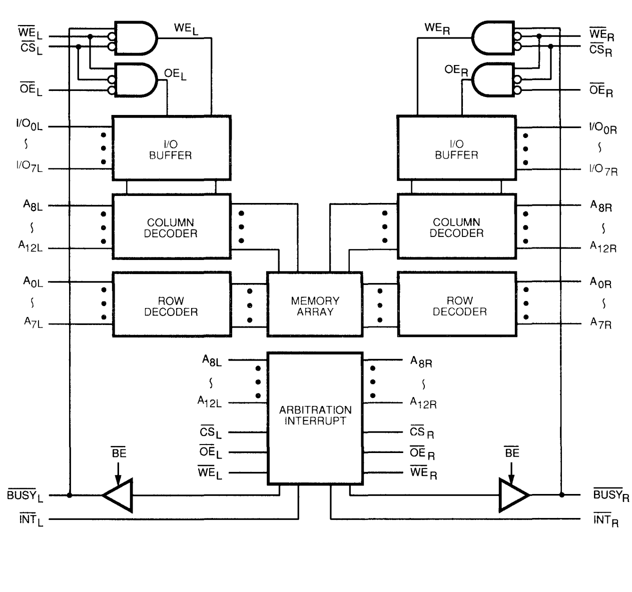
The MOSEL MS6134 is a high-speed 8K x 8 dual-port SRAM. The MS6134 is designed to be used as a stand-alone 64K-bit dual-port or as a combination Master/Slave dual-port for 16-bit or more word width systems. By grounding the Busy Output Enable ($\overline{BE}$) pin to designate it as the Master and programming all others high as Slaves, error free operation is possible without any additional logic.

Both devices provide two independent ports with separate control, address and I/O pins that permit asynchronous operation from either port. In situations where a memory location is accessed simultaneously from both ports, arbitration logic decides which port has priority access and a busy signal (BUSY) is provided for the other port that is denied access. These parts also have port-to-port communication capability which uses two message registers each paired with an Interrupt Flag ($\overline{INT}$).

Fabricated using Mosel's high performance CMOS technology, these devices operate at a maximum of 120mA of supply current. These devices also have dual chip-select power down capability with a maximum of 200µA standby current. This allows for battery back-up data retention for low power applications.

The MS6134 is packaged in a 64-lead gull-wing plastic flatpack with 40 mil lead spacing and operates over the commercial product temperature range.

FUNCTIONAL BLOCK DIAGRAM



MOSEL

MS6394/6395

PRELIMINARY

4K x 8 and 8K x 8 SRAMs with Address Latch and Chip Enable for Microcontroller Applications

FEATURES

- Supports direct interface to high-speed micro-controllers with multiplexed address and data.
- On-chip transparent address latches
- 45/70/100 ns access times available support high-speed microcontrollers
- Chip enable for powerdown 3 mA current
- Output enable for easy bus access
- Low power consumption: 350 mW (typ.) Operating
- Fully static operation
- Three-state outputs
- Packaged in 28 pin 300 mil PDIP and 330 mil SOG

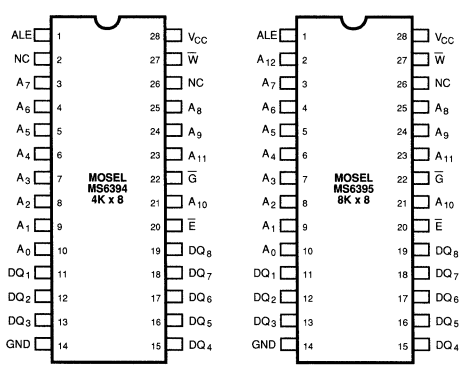
DESCRIPTION

The MOSEL MS6394 and MS6395 are CMOS static RAMs optimized for use with high-speed microcontrollers with multiplexed addresses (such as the Intel 8051). The devices are organized as 4096 words by 8 bits and 8192 words by 8 bits, and contain on-chip transparent address latches to retain memory address information. One device can replace a SRAM and an octal latch. These configurations offer a significant density and cost advantage over discrete implementations.

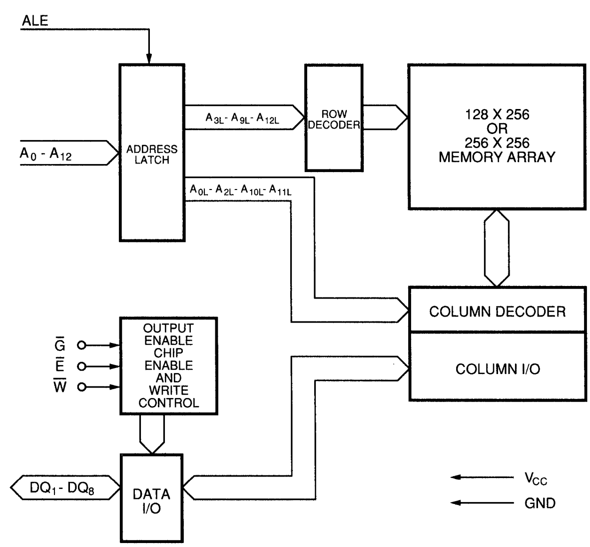
The MS6394 and MS6395 are manufactured in MOSEL's high performance CMOS technology and operate from a single 5V power supply. All inputs and outputs are TTL compatible. The devices are available packaged in a space saving 28 pin 300 mil DIP and in a standard 330 mil SO package.

PIN CONFIGURATIONS

28 PIN DIP and SOG



FUNCTIONAL BLOCK DIAGRAM (MS6394/6395)



MOSEL Corporation 914 West Maude Avenue, Sunnyvale, CA 94086 U.S.A 408-733-4556

PIN DESCRIPTIONS

A_0 - A_{12} Address Inputs

These 12 or 13 address inputs select one of the 4096 or 8192 8-bit words in the RAM.

ALE Address Latch Enable

This active HIGH pin controls the internal transparent latches on pins A_0 - A_{12}. When ALE is HIGH the latch is transparent and the inputs on the address pins are applied to the memory array. On the falling edge of ALE the current input states of pins A_0 - A_{12} are latched and remain applied to the memory array until ALE returns to the HIGH state.

$\overline{G}$ Output Enable

The output enable input is active LOW. If the output enable is active and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high-impedance state when $\overline{G}$ is inactive.

$\overline{E}$ Chip Enable

$\overline{E}$ is active LOW. The chip enable must be active to read from or write to the device. If the chip enable is not active, the device is deselected and is in a standby power mode. The DQ pins will be in the high-impedance state when the device is deselected.

$\overline{W}$ Write Enable Input

The write enable input is active LOW and controls read and write operations. When $\overline{W}$ is HIGH and $\overline{G}$ is LOW, output data will be present at the DQ pins; when $\overline{W}$ is LOW, the data present on the DQ pins will be written into the selected memory location.

DQ_1 - DQ_8 Data Input/Output Ports

These 8 bidirectional ports are used to read data from or write data into the RAM.

V_{CC} Power Supply

GND Ground

3

TRUTH TABLE

MODE	$\overline{W}$	$\overline{E}$	$\overline{G}$	I/O OPERATION	V_{CC} CURRENT
Power Down	X	H	X	High Z	I_{CCSB}, I_{CCSB1}
Output Disabled	H	L	H	High Z	I_{CC}
Read	H	L	L	D_{OUT}	I_{CC}
Write	L	L	X	D_{IN}	I_{CC}

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	PARAMETER	VALUE	UNITS
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_{BIAS}	Temperature Under Bias	-10 to +125	°C
T_{STG}	Storage Temperature	-60 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	20	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Esposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

RANGE	AMBIENT TEMPERATURE	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

DC ELECTRICAL CHARACTERISTICS (over the commercial operating range)

PARAMETER NAME	PARAMETER	TEST CONDITIONS	MS6394/6395 MIN.	TYP. [1]	MAX.	UNITS
V_{IL}	Guaranteed Input Low Voltage[2]		-0.3	-	+0.8	V
V_{IH}	Guaranteed Input High Voltage[2]		2.2	3.5	6.0	V
I_{IL}	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = GND to V_{CC}	-	-	5	µA
I_{OL}	Output Leakage Current	V_{CC} = Max, $\overline{G}$ = $\overline{E}$= V_{IH}, V_{IN} = 0V toV_{CC}	-	-	5	µA
V_{OL}	Output Low Voltage	V_{CC} = Min, I_{OL} = 4mA	-	-	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min, I_{OH} = -1mA	2.4	-	-	V
I_{CC}	Operating Power Supply Current	V_{CC} = Max, $\overline{E}$ = V_{IL}, I_{DQ} = 0mA , F = F_{max}[3]	-	-	90	mA
I_{CCSB1}	Standby Power Supply Current	V_{CC} = Max, $\overline{E}$ = V_{IH}, I_{DQ} = 0mA	-	8	15	mA
I_{CCSB2}	Power Down Power Supply Current	V_{CC} = Max, $\overline{E} \geq V_{CC}$ - 0.2V, I_{DQ} = 0mA, $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V	-	0.2	3	mA

1. Typical characteristics are at V_{cc} = 5V, T_A = 25°C.
2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
3. $F_{MAX} = 1/t_{RC}$.

CAPACITANCE[1] (T_A = 25°C, f = 1.0MHz)

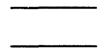
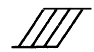
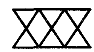
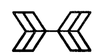
SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{DQ}	Input/Output Capacitance	V_{DQ} = 0V	8	pF

1. This parameter is guaranteed and not tested.

AC TEST CONDITIONS

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	≤5ns
Input and Output Timing Reference Level	1.5V

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

AC TEST LOADS AND WAVEFORMS

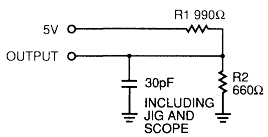


Figure 1a

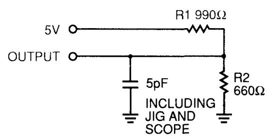
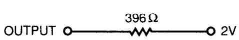


Figure 1b

Equivalent to:

THEVENIN EQUIVALENT



ALL INPUT PULSES

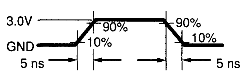


Figure 2

AC ELECTRICAL CHARACTERISTICS (over the commercial operating range)

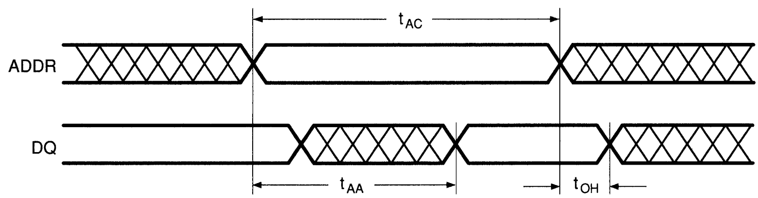
READ CYCLE

JEDEC PARAMETER NAME	PARAMETER NAME	PARAMETER	MS6394-45 MS6395-45 MIN.	MAX.	MS6394-70 MS6395-70 MIN.	MAX.	MS6394-10 MS6395-10 MIN.	MAX.	UNIT
t_{AVAX}	t_{RC}	Read Cycle Time	45	-	70	-	100		ns
t_{AVQV}	t_{AA}	Address Access Time	-	45	-	70	-	100	ns
t_{ELQV}	t_{ACE}	Chip Enable Access Time	-	45	-	70	-	100	ns
t_{GLQV}	t_{OE}	Output Enable to Output Valid	-	25	-	30	-	30	ns
t_{ELQX}	t_{CLZ}	Chip Enable to Output in Low Z	5	-	5	-	5	-	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z	5	-	5	-	5	-	ns
t_{EHQZ}	t_{CHZ}	Chip Disenable to Output in HighZ	-	35	-	35	-	35	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z	-	30	-	30	-	30	ns
t_{AXQX}	t_{OH}	Output Hold from Address Change	5	-	5	-	5	-	ns
	t_{AS}	Address Latch Setup Time	3	-	3	-	3	-	ns
	t_{AH}	Address Latch Hold Time	15	-	15	-	20	-	ns
	t_{CPWL}	ALE Width Low	15	-	20	-	30	-	ns
	t_{CPWH}	ALE Width High	15	-	20	-	30	-	ns
	t_{AALE}	Access Time from ALE	-	55	-	70	-	100	ns

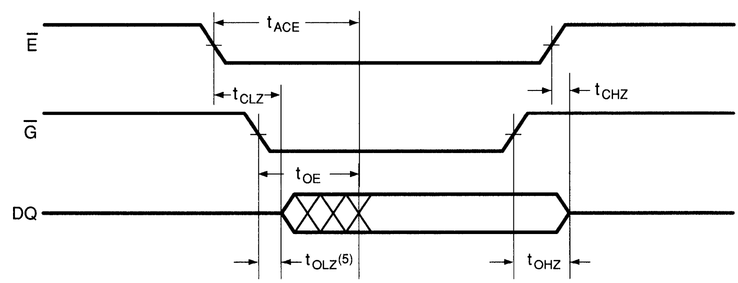
3

SWITCHING WAVEFORMS (READ CYCLE)

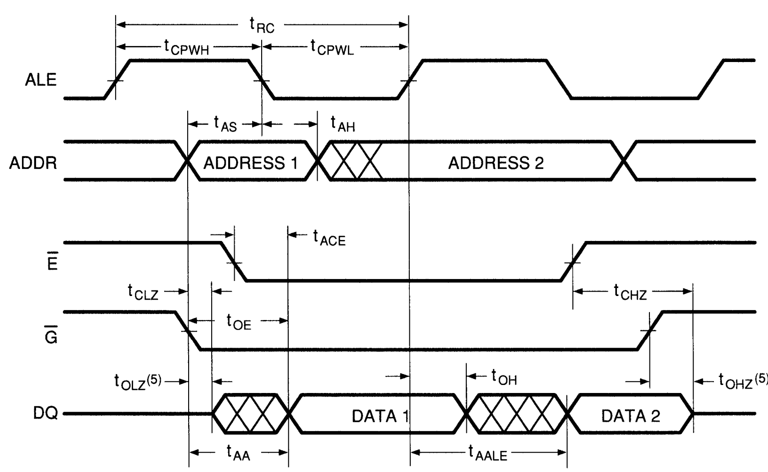
READ CYCLE 1[1,2,3] (ADDRESS ACCESS TIME - NON-PIPELINED)



READ CYCLE 2[1,4] (CHIP ENABLE AND OUTPUT ENABLE ACCESS)



READ CYCLE 3[1] (PIPELINED)



Notes:
1. $\overline{W}$ is high during all read cycles.
2. ALE must be high during non-pipelined cycles.
3. Output is continuously enabled.
4. Address must be valid sufficiently before $\overline{G}$ transition low to ensure address access specification not violated.
5. Transition is measured ±500mV from steady state with C_L = 5pF as shown in Figure 1b on page 4. This parameter is guaranteed and not 100% tested.

AC ELECTRICAL CHARACTERISTICS (over the commercial operating range)

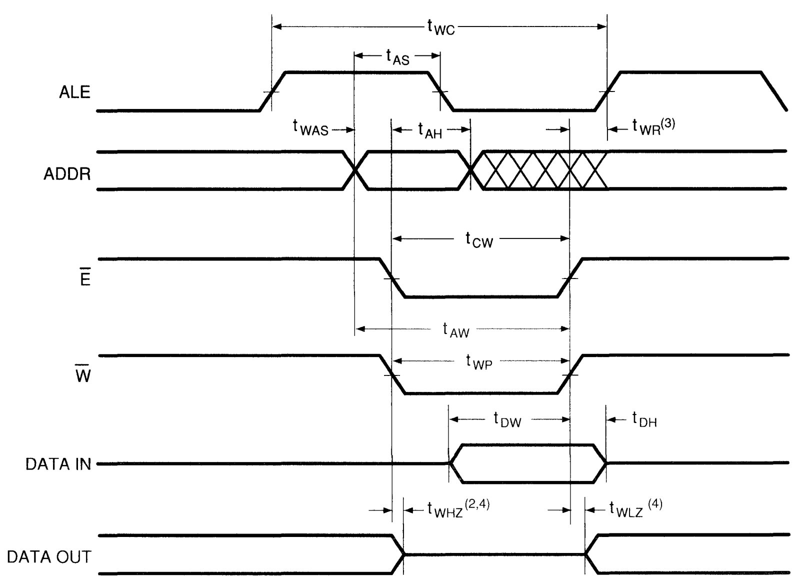
WRITE CYCLE

JEDEC PARAMETER NAME	PARAMETER NAME	PARAMETER	MS6394-45 MS6395-45 MIN.	MAX.	MS6394-70 MS6395-70 MIN.	MAX.	MS6394-10 MS6395-10 MIN.	MAX.	UNIT
t_{AVAX}	t_{WC}	Write Cycle Time	45	-	70	-	100	-	ns
t_{ELWH}	t_{CW}	Chip Enable to End of Write	40	-	60	-	80	-	ns
t_{WLWH}	t_{WP}	Write Pulse Width	35	-	50	-	50	-	ns
t_{WHQL}	t_{WLZ}	Write to Output in Low Z	5	-	5	-	5	-	ns
t_{WLQZ}	t_{WHZ}	Write to Output in High Z	-	30	-	30	-	35	ns
t_{DVWH}	t_{DW}	Data Valid to End of Write	20	-	30	-	40	-	ns
t_{WHDX}	t_{DH}	Data Hold from WriteTime	0	-	0	-	0	-	ns
	t_{AW}	Address Valid to End of Write	40	-	60	-	80	-	ns
t_{AVWL}	t_{WAS}	Address to Write Setup Time	8	-	10	-	15	-	ns
t_{WHAX}	t_{WR}	Write Recovery Time	0	-	0	-	0	-	ns
	t_{AS}	Address Latch Setup Time	3	-	3	-	3	-	ns
	t_{AH}	Address Latch Hold Time	15	-	15	-	20	-	ns

3

SWITCHING WAVEFORMS (WRITE CYCLE)

WRITE CYCLE 1 (1)



Notes:
1. $\overline{W}$ must be high during address transitions.
2. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
3. D_{OUT} is the same phase of write data of this write cycle.
4. Transition is measured ±500mV from steady state with C_L = 5pF as shown in Figure 1b on page 4. This parameter is guaranteed and not 100% tested.

ORDERING INFORMATION

MS6394 (4K x 8 Latch RAM)

SPEED (ns)	ORDERING PART NUMBER	PACKAGE REFERENCE NO.	TEMPERATURE RANGE
45	MS6394-45NC	P28-2	0°C to +70°C
70	MS6394-70NC		0°C to +70°C
100	MS6394-10NC		0°C to +70°C
45	MS6394-45FC	S28-2	0°C to +70°C
70	MS6394-70FC		0°C to +70°C
100	MS6394-10FC		0°C to +70°C

MS6395 (8K x 8 Latch RAM)

SPEED (ns)	ORDERING PART NUMBER	PACKAGE REFERENCE NO.	TEMPERATURE RANGE
45	MS6395-45NC	P28-2	0°C to +70°C
70	MS6395-70NC		0°C to +70°C
100	MS6395-10NC		0°C to +70°C
45	MS6395-45FC	S28-2	0°C to +70°C
70	MS6395-70FC		0°C to +70°C
100	MS6395-10FC		0°C to +70°C

PRELIMINARY

12K x 8 SRAM with Address Latch and Chip Enable for Multiplexed Microcontroller Applications

FEATURES

- Supports direct interface to high-speed micro-controllers with multiplexed address and data.
- On-chip transparent address latches
- 96K static RAM replaces 5 discrete chips
- 45/70/100 ns access times available support high-speed microcontrollers
- Chip enable for powerdown 3 mA current
- Output enable for easy bus access
- Low power consumption: 350 mW (typ.) Operating
- Fully static operation
- Three-state outputs
- Packaged in 28 pin 300 mil PDIP and 330 mil SOG

DESCRIPTION

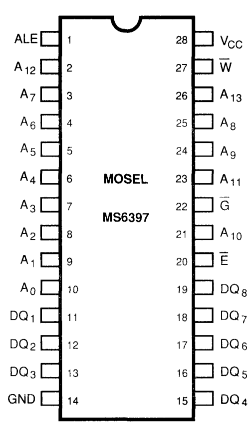
The MOSEL MS6397 is a CMOS static RAM optimized for use with high-speed microcontrollers with multiplexed addresses (such as the Intel 8051). The device is organized as 12288 words by 8 bits, and contains on-chip transparent address latches to retain memory address information. One MS6397 can replace an 8K x 8 SRAM, two 2K x 8 SRAMs and 2 octal latches. This configuration offers a significant density and cost advantages over a discrete implementation.

The MS6397 is manufactured in MOSEL's high performance CMOS technology and operates from a single 5V power supply. All inputs and outputs are TTL compatible. The device is available packaged in a space saving 28 pin 300 mil DIP and in a standard 330 mil SO package.

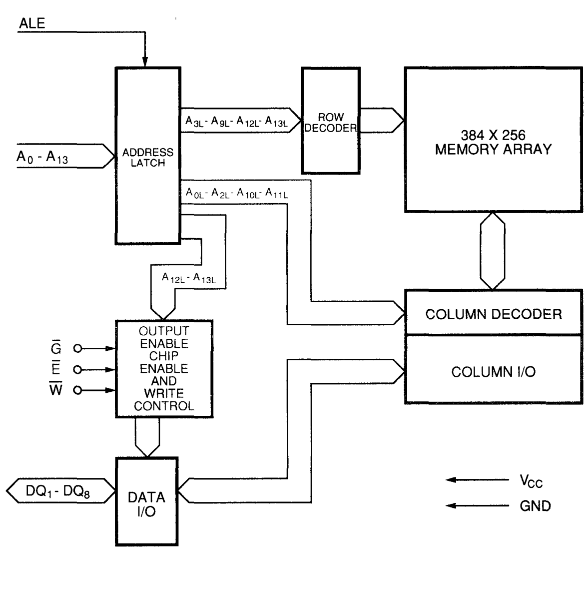
3

PIN CONFIGURATIONS

28 PIN DIP and SOG



FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

A_0 - A_{13} Address Inputs
These 14 address inputs select one of the 12288 8-bit words in the RAM.

ALE Address Latch Enable
This active HIGH pin controls the internal transparent latches on pins A_0 - A_{13}. When ALE is HIGH the latch is transparent and the inputs on the address pins are applied to the memory array. On the falling edge of ALE the current input states of pins A_0 - A_{13} are latched and remain applied to the memory array until ALE returns to the HIGH state.

$\overline{G}$ Output Enable
The output enable input is active LOW. If the output enable is active and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high-impedance state when $\overline{G}$ is inactive.

$\overline{E}$ Chip Enable
$\overline{E}$ is active LOW. The chip enable must be active to read from or write to the device. If the chip enable is not active, the device is deselected and is in a standby power mode. The DQ pins will be in the high-impedance state when the device is deselected.

$\overline{W}$ Write Enable Input
The write enable input is active LOW and controls read and write operations. When $\overline{W}$ is HIGH and $\overline{G}$ is LOW, output data will be present at the DQ pins; when $\overline{W}$ is LOW, the data present on the DQ pins will be written into the selected memory location.

DQ_1 - DQ_8 Data Input/Output Ports
These 8 bidirectional ports are used to read data from or write data into the RAM.

V_{CC} Power Supply

GND Ground

TRUTH TABLE

MODE	$\overline{W}$	$\overline{E}$	$\overline{G}$	I/O OPERATION	V_{CC} CURRENT
Power Down	X	H	X	High Z	I_{CCSB}, I_{CCSB1}
Output Disabled	H	L	H	High Z	I_{CC}
Read	H	L	L	D_{OUT}	I_{CC}
Write	L	L	X	D_{IN}	I_{CC}

MEMORY BLOCK SELECT

A_{13}	A_{12}	DQ Status; Memory Block Selected
H	H	High Z; Chip Deselected
H	L	Active; Top 4K block
L	H	Active; Mid 4K block
L	L	Active; Low 4K block

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	PARAMETER	VALUE	UNITS
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_{BIAS}	Temperature Under Bias	-10 to +125	°C
T_{STG}	Storage Temperature	-60 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	20	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Esposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

RANGE	AMBIENT TEMPERATURE	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

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DC ELECTRICAL CHARACTERISTICS (over the commercial operating range)

PARAMETER NAME	PARAMETER	TEST CONDITIONS	MS6397 MIN.	TYP. (1)	MAX.	UNITS
V_{IL}	Guaranteed Input Low Voltage(2)		-0.3	-	+0.8	V
V_{IH}	Guaranteed Input High Voltage(2)		2.2	3.5	6.0	V
I_{IL}	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = GND to V_{CC}	-	-	5	µA
I_{OL}	Output Leakage Current	V_{CC} = Max, $\overline{G} = \overline{E} = V_{IH}$, V_{IN} = 0V to V_{CC}	-	-	5	µA
V_{OL}	Output Low Voltage	V_{CC} = Min, I_{OL} = 4mA	-	-	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min, I_{OH} = -1mA	2.4	-	-	V
I_{CC}	Operating Power Supply Current	V_{CC} = Max, $\overline{E} = V_{IL}$, I_{DQ} = 0mA , $F = F_{max}$(3)	-	-	90	mA
I_{CCSB1}	Standby Power Supply Current	V_{CC} = Max, $\overline{E} = V_{IH}$, I_{DQ} = 0mA	-	8	15	mA
I_{CCSB2}	Power Down Power Supply Current	V_{CC} = Max, $\overline{E} \geq V_{CC} - 0.2V$, I_{DQ} = 0mA, $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq 0.2V$	-	0.2	3	mA

1. Typical characteristics are at V_{cc} = 5V, T_A = 25°C.
2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
3. $F_{MAX} = 1/t_{RC}$

CAPACITANCE(1) (T_A = 25°C, f = 1.0MHz)

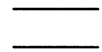
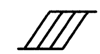
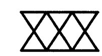
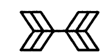
SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{DQ}	Input/Output Capacitance	V_{DQ} = 0V	8	pF

1. This parameter is guaranteed and not tested.

AC TEST CONDITIONS

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	≤5ns
Input and Output Timing Reference Level	1.5V

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

AC TEST LOADS AND WAVEFORMS

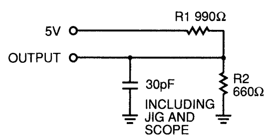


Figure 1a

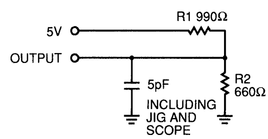
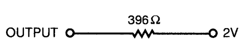


Figure 1b

Equivalent to:

THEVENIN EQUIVALENT



ALL INPUT PULSES

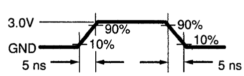


Figure 2

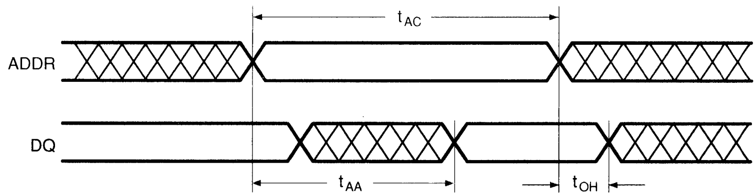
AC ELECTRICAL CHARACTERISTICS (over the commercial operating range)

READ CYCLE

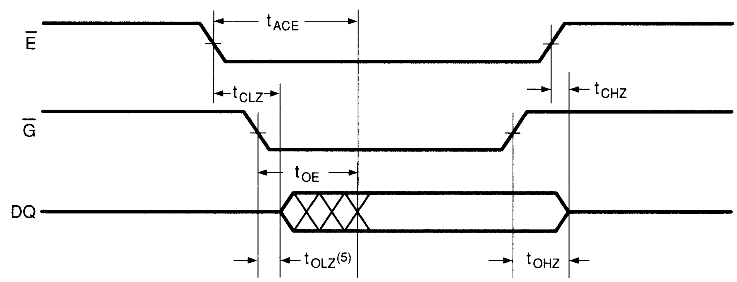
JEDEC PARAMETER NAME	PARAMETER NAME	PARAMETER	MS6397-45 MIN.	MS6397-45 MAX.	MS6397-70 MIN.	MS6397-70 MAX.	MS6397-10 MIN.	MS6397-10 MAX.	UNIT
t_{AVAX}	t_{RC}	Read Cycle Time	45	-	70	-	100		ns
t_{AVQV}	t_{AA}	Address Access Time	-	45	-	70	-	100	ns
t_{ELQV}	t_{ACE}	Chip Enable Access Time	-	45	-	70	-	100	ns
t_{GLQV}	t_{OE}	Output Enable to Output Valid	-	25	-	30	-	30	ns
t_{ELQX}	t_{CLZ}	Chip Enable to Output in Low Z	5	-	5	-	5	-	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z	5	-	5	-	5	-	ns
t_{EHQZ}	t_{CHZ}	Chip Disenable to Output in HighZ	-	35	-	35	-	35	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z	-	30	-	30	-	30	ns
t_{AXQX}	t_{OH}	Output Hold from Address Change	5	-	5	-	5	-	ns
	t_{AS}	Address Latch Setup Time	3	-	3	-	3	-	ns
	t_{AH}	Address Latch Hold Time	15	-	15	-	20	-	ns
	t_{CPWL}	ALE Width Low	15	-	20	-	30	-	ns
	t_{CPWH}	ALE Width High	15	-	20	-	30	-	ns
	t_{AALE}	Access Time from ALE	-	55	-	70	-	100	ns

SWITCHING WAVEFORMS (READ CYCLE)

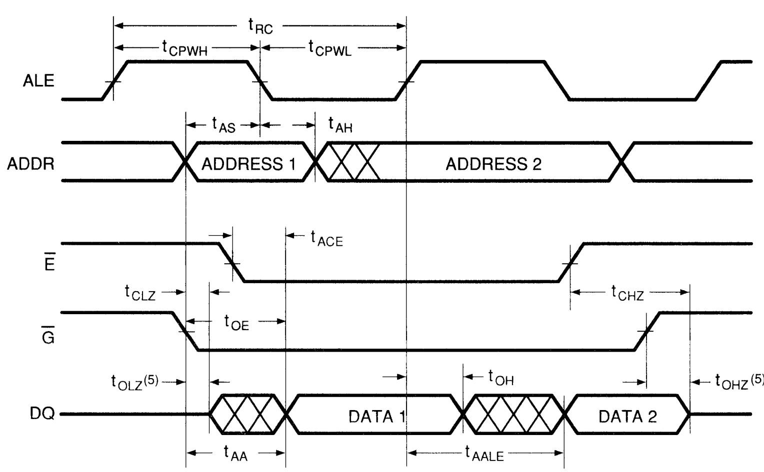
READ CYCLE 1[1,2,3] (ADDRESS ACCESS TIME - NON-PIPELINED)



READ CYCLE 2[1,4] (CHIP ENABLE AND OUTPUT ENABLE ACCESS)



READ CYCLE 3[1] (PIPELINED)



Notes:
1. $\overline{W}$ is high during all read cycles.
2. ALE must be high during non-pipelined cycles.
3. Output is continuously enabled.
4. Address must be valid sufficiently before $\overline{G}$ transition low to ensure address access specification not violated.
5. Transition is measured ±500mV from steady state with C_L = 5pF as shown in Figure 1b on page 4. This parameter is guaranteed and not 100% tested.

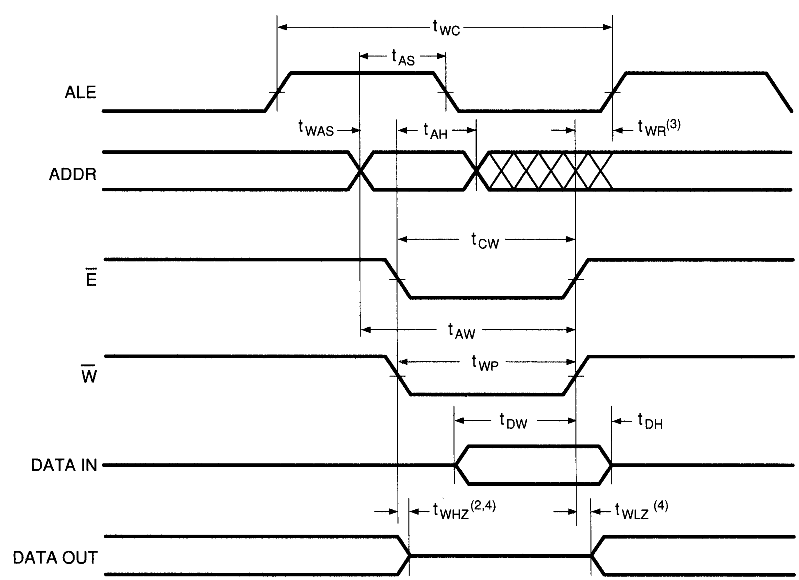
AC ELECTRICAL CHARACTERISTICS (over the commercial operating range)

WRITE CYCLE

JEDEC PARAMETER NAME	PARAMETER NAME	PARAMETER	MS6397-45 MIN.	MS6397-45 MAX.	MS6397-70 MIN.	MS6397-70 MAX.	MS6397-10 MIN.	MS6397-10 MAX.	UNIT
t_{AVAX}	t_{WC}	Write Cycle Time	45	-	70	-	100	-	ns
t_{ELWH}	t_{CW}	Chip Enable to End of Write	40	-	60	-	80	-	ns
t_{WLWH}	t_{WP}	Write Pulse Width	35	-	50	-	50	-	ns
t_{WHQL}	t_{WLZ}	Write to Output in Low Z	5	-	5	-	5	-	ns
t_{WLQZ}	t_{WHZ}	Write to Output in High Z	-	30	-	30	-	35	ns
t_{DVWH}	t_{DW}	Data Valid to End of Write	20	-	30	-	40	-	ns
t_{WHDX}	t_{DH}	Data Hold from WriteTime	0	-	0	-	0	-	ns
	t_{AW}	Address Valid to End of Write	40	-	60	-	80	-	ns
t_{AVWL}	t_{WAS}	Address to Write Setup Time	8	-	10	-	15	-	ns
t_{WHAX}	t_{WR}	Write Recovery Time	0	-	0	-	0	-	ns
	t_{AS}	Address Latch Setup Time	3	-	3	-	3	-	ns
	t_{AH}	Address Latch Hold Time	15	-	15	-	20	-	ns

SWITCHING WAVEFORMS (WRITE CYCLE)

WRITE CYCLE 1 (1)



Notes:
1. $\overline{W}$ must be high during address transitions.
2. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
3. D_{OUT} is the same phase of write data of this write cycle.
4. Transition is measured ±500mV from steady state with C_L = 5pF as shown in Figure 1b on page 4. This parameter is guaranteed and not 100% tested.

ORDERING INFORMATION

SPEED (ns)	ORDERING PART NUMBER	PACKAGE REFERENCE NO.	TEMPERATURE RANGE
45	MS6397-45NC	P28-2	0°C to +70°C
70	MS6397-70NC		0°C to +70°C
100	MS6397-10NC		0°C to +70°C
45	MS6397-45FC	S28-2	0°C to +70°C
70	MS6397-70FC		0°C to +70°C
100	MS6397-10FC		0°C to +70°C

PRELIMINARY

16K x 8 SRAM with Address Latch and Chip Enable for Microcontroller Applications

FEATURES

- Supports direct interface to high-speed micro-controllers with multiplexed address and data.
- On-chip transparent address latches
- 45/70/100 ns access times available support high-speed microcontrollers
- Chip enable for powerdown 3 mA current
- Output enable for easy bus access
- Low power consumption: 350 mW (typ.) Operating
- Fully static operation
- Three-state outputs
- Packaged in 28 pin 300 mil PDIP and 330 mil SOG

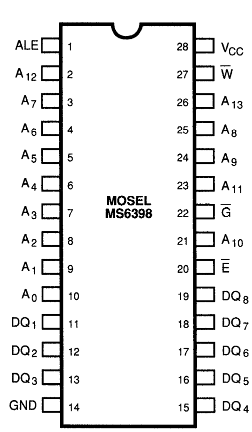
DESCRIPTION

The MOSEL MS6398 is a CMOS static RAM optimized for use with high-speed microcontrollers with multiplexed addresses (such as the Intel 8051). The device is organized as 16384 words by 8 bits, and contain on-chip transparent address latches to retain memory address information. One device can replace a combination of SRAMs, and an octal latch. This configuration offers a significant density and cost advantage over a discrete implementation.

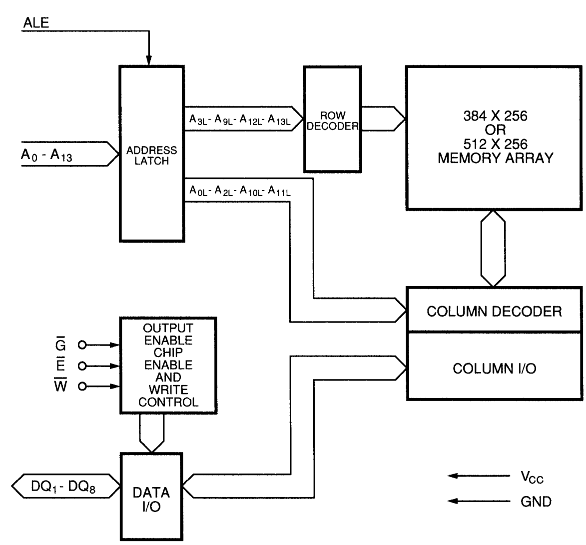
The MS6398 is manufactured in MOSEL's high performance CMOS technology and operate from a single 5V power supply. All inputs and outputs are TTL compatible. The device is available packaged in a space saving 28 pin 300 mil DIP and in a standard 330 mil SO package.

PIN CONFIGURATIONS

28 PIN DIP and SOG



FUNCTIONAL BLOCK DIAGRAM



MOSEL Corporation 914 West Maude Avenue, Sunnyvale, CA 94086 U.S.A 408-733-4556

PIN DESCRIPTIONS

A_0 - A_{13} Address Inputs

These 14 address inputs select one of the 16384 8-bit words in the RAM.

ALE Address Latch Enable

This active HIGH pin controls the internal transparent latches on pins A_0 - A_{13}. When ALE is HIGH the latch is transparent and the inputs on the address pins are applied to the memory array. On the falling edge of ALE the current input states of pins A_0 - A_{13} are latched and remain applied to the memory array until ALE returns to the HIGH state.

$\overline{G}$ Output Enable

The output enable input is active LOW. If the output enable is active and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high-impedance state when $\overline{G}$ is inactive.

$\overline{E}$ Chip Enable

$\overline{E}$ is active LOW. The chip enable must be active to read from or write to the device. If the chip enable is not active, the device is deselected and is in a standby power mode. The DQ pins will be in the high-impedance state when the device is deselected.

$\overline{W}$ Write Enable Input

The write enable input is active LOW and controls read and write operations. When $\overline{W}$ is HIGH and $\overline{G}$ is LOW, output data will be present at the DQ pins; when $\overline{W}$ is LOW, the data present on the DQ pins will be written into the selected memory location.

DQ_1 - DQ_8 Data Input/Output Ports

These 8 bidirectional ports are used to read data from or write data into the RAM.

V_{CC} Power Supply

GND Ground

3

TRUTH TABLE

MODE	$\overline{W}$	$\overline{E}$	$\overline{G}$	I/O OPERATION	V_{CC} CURRENT
Power Down	X	H	X	High Z	I_{CCSB}, I_{CCSB1}
Output Disabled	H	L	H	High Z	I_{CC}
Read	H	L	L	D_{OUT}	I_{CC}
Write	L	L	X	D_{IN}	I_{CC}

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	PARAMETER	VALUE	UNITS
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_{BIAS}	Temperature Under Bias	-10 to +125	°C
T_{STG}	Storage Temperature	-60 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	20	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Esposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

RANGE	AMBIENT TEMPERATURE	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

DC ELECTRICAL CHARACTERISTICS (over the commercial operating range)

PARAMETER NAME	PARAMETER	TEST CONDITIONS	MS6398 MIN.	TYP. [1]	MAX.	UNITS
V_{IL}	Guaranteed Input Low Voltage[2]		-0.3	-	+0.8	V
V_{IH}	Guaranteed Input High Voltage[2]		2.2	3.5	6.0	V
I_{IL}	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = GND to V_{CC}	-	-	5	μA
I_{OL}	Output Leakage Current	V_{CC} = Max, $\overline{G}$ = $\overline{E}$= V_{IH}, V_{IN} = 0V toV_{CC}	-	-	5	μA
V_{OL}	Output Low Voltage	V_{CC} = Min, I_{OL} = 4mA	-	-	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min, I_{OH} = -1mA	2.4	-	-	V
I_{CC}	Operating Power Supply Current	V_{CC} = Max, $\overline{E}$ = V_{IL}, I_{DQ} = 0mA , F = F_{max}[3]	-	-	90	mA
I_{CCSB1}	Standby Power Supply Current	V_{CC} = Max, $\overline{E}$ = V_{IH}, I_{DQ} = 0mA	-	8	15	mA
I_{CCSB2}	Power Down Power Supply Current	V_{CC} = Max, $\overline{E} \geq V_{CC}$ - 0.2V, I_{DQ} = 0mA, $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V	-	0.2	3	mA

1. Typical characteristics are at V_{cc} = 5V, T_A = 25°C.
2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
3. $F_{MAX} = 1/t_{RC}$.

CAPACITANCE[1] (T_A = 25°C, f = 1.0MHz)

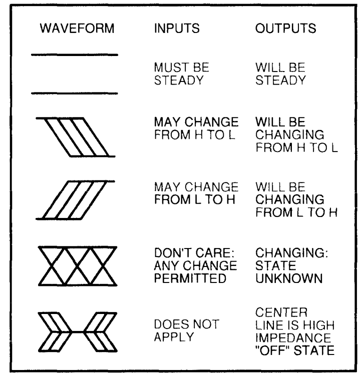
SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{DQ}	Input/Output Capacitance	V_{DQ} = 0V	8	pF

1. This parameter is guaranteed and not tested.

AC TEST CONDITIONS

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	≤5ns
Input and Output Timing Reference Level	1.5V

KEY TO SWITCHING WAVEFORMS



3

AC TEST LOADS AND WAVEFORMS

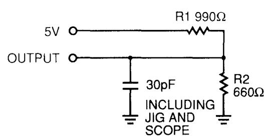


Figure 1a

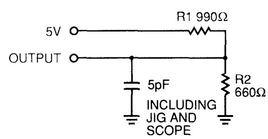
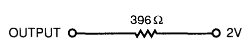


Figure 1b

Equivalent to:

THEVENIN EQUIVALENT



ALL INPUT PULSES

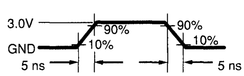


Figure 2

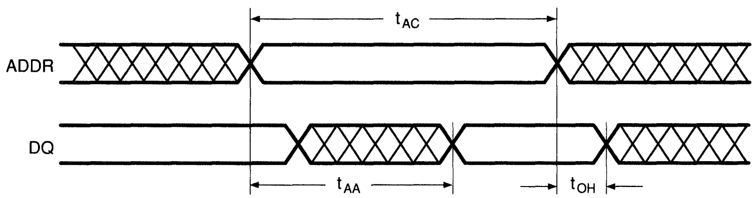
AC ELECTRICAL CHARACTERISTICS (over the commercial operating range)

READ CYCLE

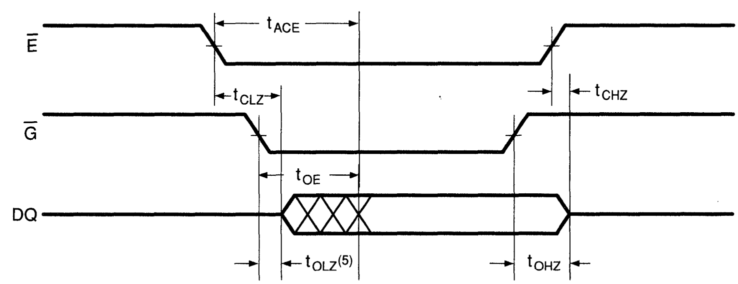
JEDEC PARAMETER NAME	PARAMETER NAME	PARAMETER	MS6398-45 MIN.	MS6398-45 MAX.	MS6398-70 MIN.	MS6398-70 MAX.	MS6398-10 MIN.	MS6398-10 MAX.	UNIT
t_{AVAX}	t_{RC}	Read Cycle Time	45	-	70	-	100		ns
t_{AVQV}	t_{AA}	Address Access Time	-	45	-	70	-	100	ns
t_{ELQV}	t_{ACE}	Chip Enable Access Time	-	45	-	70	-	100	ns
t_{GLQV}	t_{OE}	Output Enable to Output Valid	-	25	-	30	-	30	ns
t_{ELQX}	t_{CLZ}	Chip Enable to Output in Low Z	5	-	5	-	5	-	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z	5	-	5	-	5	-	ns
t_{EHQZ}	t_{CHZ}	Chip Disenable to Output in HighZ	-	35	-	35	-	35	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z	-	30	-	30	-	30	ns
t_{AXQX}	t_{OH}	Output Hold from Address Change	5	-	5	-	5	-	ns
	t_{AS}	Address Latch Setup Time	3	-	3	-	3	-	ns
	t_{AH}	Address Latch Hold Time	15	-	15	-	20	-	ns
	t_{CPWL}	ALE Width Low	15	-	20	-	30	-	ns
	t_{CPWH}	ALE Width High	15	-	20	-	30	-	ns
	t_{AALE}	Access Time from ALE	-	55	-	70	-	100	ns

SWITCHING WAVEFORMS (READ CYCLE)

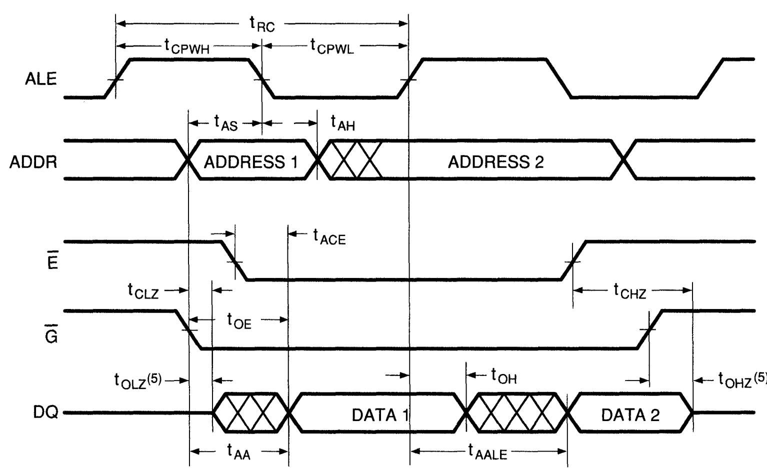
READ CYCLE 1[1,2,3] (ADDRESS ACCESS TIME - NON-PIPELINED)



READ CYCLE 2[1,4] (CHIP ENABLE AND OUTPUT ENABLE ACCESS)



READ CYCLE 3[1] (PIPELINED)



Notes:
1. $\overline{W}$ is high during all read cycles.
2. ALE must be high during non-pipelined cycles.
3. Output is continuously enabled.
4. Address must be valid sufficiently before $\overline{G}$ transition low to ensure address access specification not violated.
5. Transition is measured ±500mV from steady state with C_L = 5pF as shown in Figure 1b on page 4. This parameter is guaranteed and not 100% tested.

AC ELECTRICAL CHARACTERISTICS (over the commercial operating range)

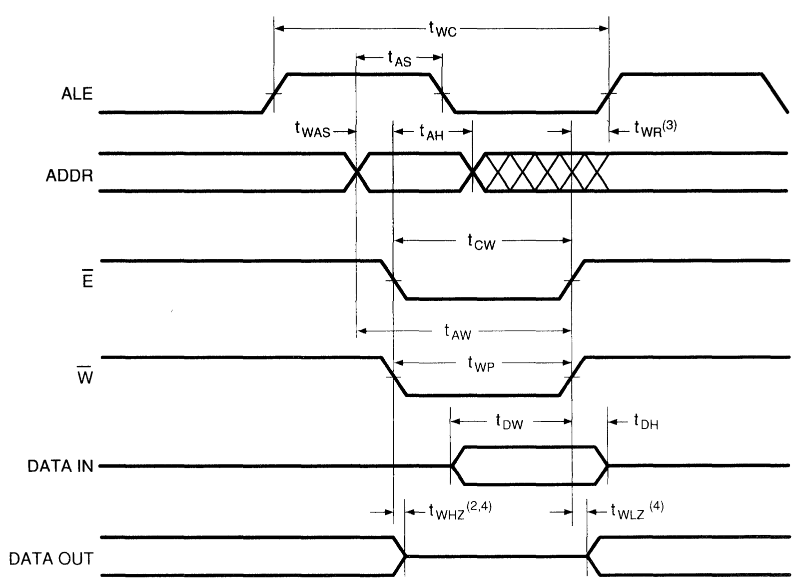
WRITE CYCLE

JEDEC PARAMETER NAME	PARAMETER NAME	PARAMETER	MS6398-45 MIN.	MS6398-45 MAX.	MS6398-70 MIN.	MS6398-70 MAX.	MS6398-10 MIN.	MS6398-10 MAX.	UNIT
t_{AVAX}	t_{WC}	Write Cycle Time	45	-	70	-	100	-	ns
t_{ELWH}	t_{CW}	Chip Enable to End of Write	40	-	60	-	80	-	ns
t_{WLWH}	t_{WP}	Write Pulse Width	35	-	50	-	50	-	ns
t_{WHQL}	t_{WLZ}	Write to Output in Low Z	5	-	5	-	5	-	ns
t_{WLQZ}	t_{WHZ}	Write to Output in High Z	-	30	-	30	-	35	ns
t_{DVWH}	t_{DW}	Data Valid to End of Write	20	-	30	-	40	-	ns
t_{WHDX}	t_{DH}	Data Hold from WriteTime	0	-	0	-	0	-	ns
	t_{AW}	Address Valid to End of Write	40	-	60	-	80	-	ns
t_{AVWL}	t_{WAS}	Address to Write Setup Time	8	-	10	-	15	-	ns
t_{WHAX}	t_{WR}	Write Recovery Time	0	-	0	-	0	-	ns
	t_{AS}	Address Latch Setup Time	3	-	3	-	3	-	ns
	t_{AH}	Address Latch Hold Time	15	-	15	-	20	-	ns

3

SWITCHING WAVEFORMS (WRITE CYCLE)

WRITE CYCLE 1 (1)



Notes:
1. $\overline{W}$ must be high during address transitions.
2. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
3. D_{OUT} is the same phase of write data of this write cycle.
4. Transition is measured ±500mV from steady state with C_L = 5pF as shown in Figure 1b on page 4. This parameter is guaranteed and not 100% tested.

ORDERING INFORMATION

SPEED (ns)	ORDERING PART NUMBER	PACKAGE REFERENCE NO.	TEMPERATURE RANGE
45	MS6398-45NC	P28-2	0°C to +70°C
70	MS6398-70NC		0°C to +70°C
100	MS6398-10NC		0°C to +70°C
45	MS6398-45FC	S28-2	0°C to +70°C
70	MS6398-70FC		0°C to +70°C
100	MS6398-10FC		0°C to +70°C

ADVANCE INFORMATION

32K x 8 Parity Ram

3

FEATURES

- High speed – 25/35 ns (Max.)
- 32K x 8 external; 32K x 9 internal
- On chip parity generation and checking
- Automatic power-down when chip disabled
- Lower power consumption:
  - 715mW (Max.) Operating
  - 138mW (Max.) Standby
- TTL compatible interface levels
- Single 5V power supply
- Fully static operation
- Three state outputs
- Two chip enables ($\overline{E}_1$ and E_2) for simple memory expansion
- Fast E_2 access time (14ns) to support cache applications

DESCRIPTION

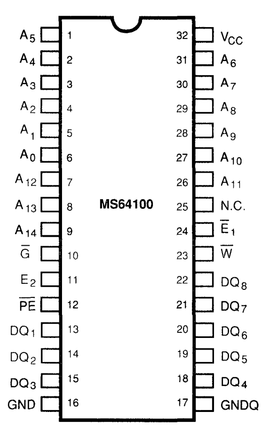
The MOSEL MS64100 Parity RAM is a high speed, CMOS Static RAM with on board parity generation and parity error detection circuitry. It is organized as 32,768 words of 8 bits each externally. Internally the organization is 32,768 x 9; the 9th parity bit is generated and checked on chip.

The MS64100 is ideal for use in cache or main memory applications for high reliability systems that require extra system diagnostic capability and/or protection from soft errors. Such applications Include financial transaction processing, medical or military systems.

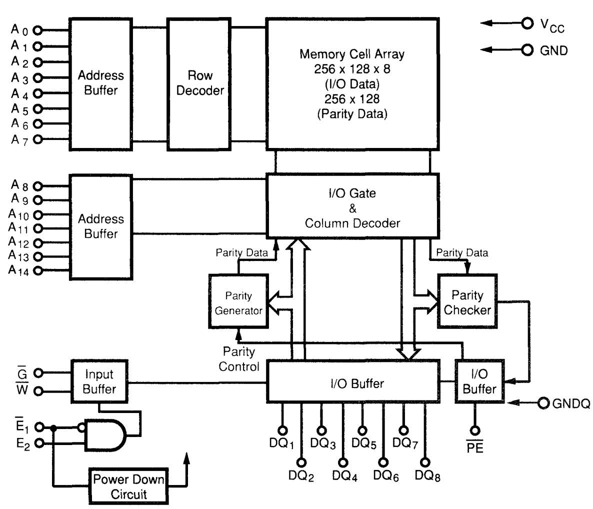
The MS64100 insures the detection of all single bit errors, providing several orders of magnitude of increased protection against alpha-particle induced soft errors and other bit error mechanisms. In a cache application the correct data can be retrieved from main memory in the event of an error.

The MS64100 operates from a single 5 volt power supply. All inputs and outputs are TTL compatible. The MOSEL MS64100 is packaged in a space saving 32 pin 300 mil plastic DIP package and 330 mil SO package.

PIN CONFIGURATIONS



FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

A_0 - A_{12} Address Inputs

These 13 address inputs select one of the 8192 8-bit words in the RAM.

$\overline{E}_1$ Chip Enable 1 Input

E_2 Chip Enable 2 Input

$\overline{E}_1$ is active LOW and E_2 is active HIGH. Both chip enables must be active to read from or write to the device. If either chip enable is not active, the device is deselected and is in a standby power mode. The DQ pins will be in the high-impedance state when the device is deselected.

$\overline{G}$ Output Enable Input

The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when $\overline{G}$ is inactive.

$\overline{PE}$ Parity Error

During a read cycle, the $\overline{PE}$ goes low to signal that a parity error has occurred, or remains in the high Z state if there is no parity error. During a write cycle, the MS64100 generates a 9th parity bit on chip which is written into the memory array. If the $\overline{PE}$ pin is forced low during the write, a false entry will be made for the parity bit. This will result in a parity error signal during subsequent read cycles.

$\overline{W}$ Write Enable Input

The write enable input is active LOW and controls read and write operations. With the chip selected, when $\overline{W}$ is HIGH and $\overline{G}$ is LOW, output data will be present at the DQ pins; when $\overline{W}$ is LOW, the data present on the DQ pins will be written into the selected memory location.

DQ_1 - DQ_8 Data Input/Output Ports

These 8 bidirectional ports are used to read data from or write data into the RAM.

V_{CC} Power Supply

GND Ground

TRUTH TABLE

$\overline{E}_1$	E_2	$\overline{W}$	$\overline{G}$	MODE	SUPPLY CURRENT	I/O, PE STATE
H	X	X	X	Standby	I_{SB}	High Z
L	L	X	X	Deselect	I_{CC}	High Z
L	H	H	H	D_{OUT} Disable	I_{CC}	High Z
L	H	H	L	Read	I_{CC}	D_{OUT}
L	H	L	X	Write	I_{CC}	D_{IN}

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	PARAMETER	RATING	UNITS
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_{BIAS}	Temperature Under Bias	–0 to +85	°C
T_{STG}	Storage Temperature	–45 to +125	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	20	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

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DC ELECTRICAL CHARACTERISTICS (over the operating range)

PARAMETER NAME	PARAMETER	TEST CONDITIONS		MS64100 MIN.	TYP.[1]	MAX.	UNITS
V_{IL}	Guaranteed Input Low Voltage[2]			–2.0	-	0.8	V
V_{IH}	Guaranteed Input High Voltage[2]			2.2	-	6.0	V
I_{IL}	Input Leakage Current	V_{CC} = Max, V_{IN} = 0V to V_{CC}		–5	-	5	µA
I_{OL}	Output Leakage Current	V_{CC} = Max, $\overline{E}_1 = V_{IH}$, or $E_2 = V_{IL}$, or $\overline{G} = V_{IH}$, V_{IN} = 0V to V_{CC}		–5	-	5	µA
V_{OL}	Output Low Voltage	V_{CC} = Min, I_{OL} = 8mA		-	-	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min, I_{OH} = –4mA		2.4	-	-	V
I_{CC}	Operating Power Supply Current	V_{CC} = Max, $\overline{E}_1 = V_{IL}$, $I_{I/O}$ = 0mA, F = F_{max}[3]	25 ns	-	-	130	mA
			35 ns	-	-	110	
I_{CCSB}	Standby Power Supply Current	V_{CC} = Max, $\overline{E}_1 = V_{IH}$, $I_{I/O}$ = 0mA , $V_{IN} \le 0.2V$		-	-	25	mA
I_{CCSB1}	Power Down Power Supply Current	V_{CC} = Max, $\overline{E}_1 > V_{CC} - 0.2V$ $V_{IN} > V_{CC} - 0.2V$ or $V_{IN} < 0.2V$		-	-	15	mA

1. Typical characteristics are at V_{cc} = 5V, T_A = 25°C.
2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included; –2.0 V_{IL} min for pulse width of less than 20ns: V_{IL} min = –0.5V at DC levels
3. $F_{MAX} = 1/t_{RC}$.

CAPACITANCE[1] (T_A = 25°C, f = 1.0MHz)

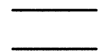
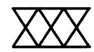
SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	7	pF
C_{DQ}	Input/Output Capacitance	$V_{I/O}$ = 0V	8	pF

1. This parameter is guaranteed and not tested.

AC TEST CONDITIONS

Input Pulse Levels	0.6 to 2.4V
Input Rise and Fall Times	3 ns
Input and Output Timing Reference Level	Input : V_{IL} = 0.8V, V_{IH} = 2.2V Output: V_{IL} = 0.8V, V_{OH} = 2.2V

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

AC TEST LOADS AND WAVEFORMS

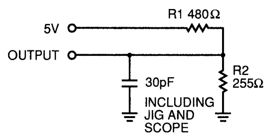


Figure 1a

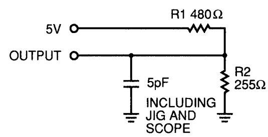
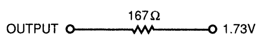


Figure 1b

Equivalent to:

THEVENIN EQUIVALENT



ALL INPUT PULSES

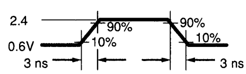


Figure 2

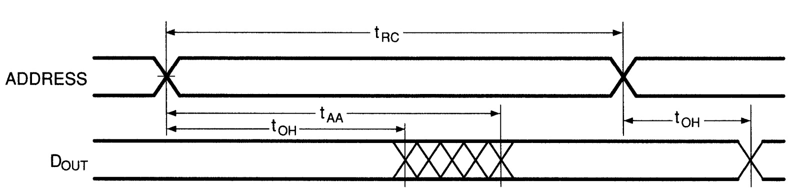
AC ELECTRICAL CHARACTERISTICS (over the operating range)

READ CYCLE

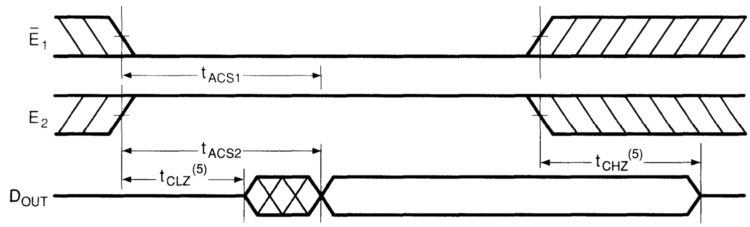
JEDEC PARAMETER NAME	PARAMETER NAME	PARAMETER		MS64100-25 MIN.	TYP.	MAX.	MS64100-35 MIN.	TYP.	MAX.	UNIT
t_{AVAX}	t_{RC}	Read Cycle Time		25	-	-	35	-	-	ns
t_{AVQV}	t_{AA}	Address Access Time		-	-	25	-	-	35	ns
t_{E1LQV}	t_{ACS1}	Chip Enable Access Time	$\overline{E}_1$	-	-	25	-	-	35	ns
t_{E2HQX}	t_{ACS2}	Chip Enable Access Time	E_2	-	-	14	-	-	15	ns
t_{GLQV}	t_{OE}	Output Enable to Output Valid		-	-	12	-	-	14	ns
t_{E1LQX}	t_{CLZ1}	Chip Enable to Output Low Z	$\overline{E}_1$	5	-	-	8	-	-	ns
t_{E2HQX}	t_{CLZ2}	Chip Enable to to Output Low Z	E_2	2	-	-	3	-	-	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z		2	-	-	3	-	-	ns
t_{E1HQZ}	t_{CHZ1}	Chip Disable to Output in High Z	$\overline{E}_1$	1	-	15	1	-	15	ns
t_{E2LQZ}	t_{CHZ2}	Chip Disable to Output in High Z	E_2	1	-	15	1	-	15	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z		1	-	15	1	-	15	ns
t_{AXQX}	t_{OH}	Output Hold from Address Change		3	-	-	3	-	-	ns

SWITCHING WAVEFORMS (READ CYCLE)

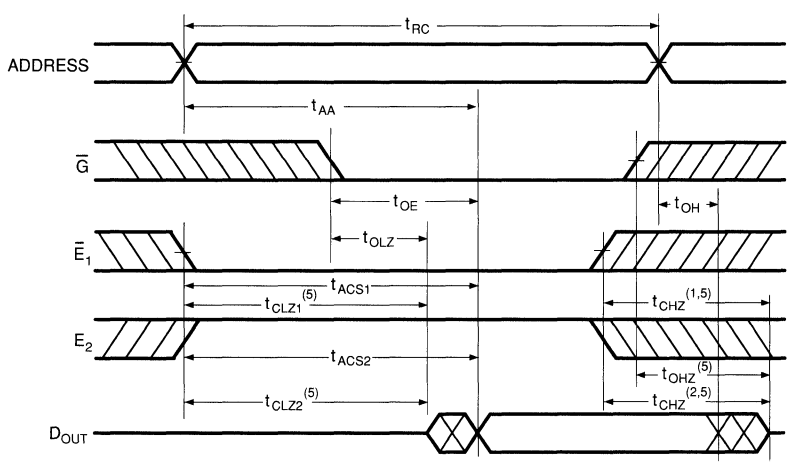
READ CYCLE 1(1,2,4)



READ CYCLE 2[1,3,4]



READ CYCLE 3[1,4]



NOTES:
1. $\overline{W}$ is high for READ Cycle.
2. Device is continuously selected $\overline{E}_1 = V_{IL}$ and $E_2 = V_{IH}$.
3. Address valid prior to or coincident with $\overline{E}_1$ transition low and/or E_2 transition high.
4. $\overline{G} = V_{IL}$.
5. Transition is measured ± 500mV from steady state with C_L = 5pF as shown in Figure 1b. This parameter is guaranteed but not 100% tested.

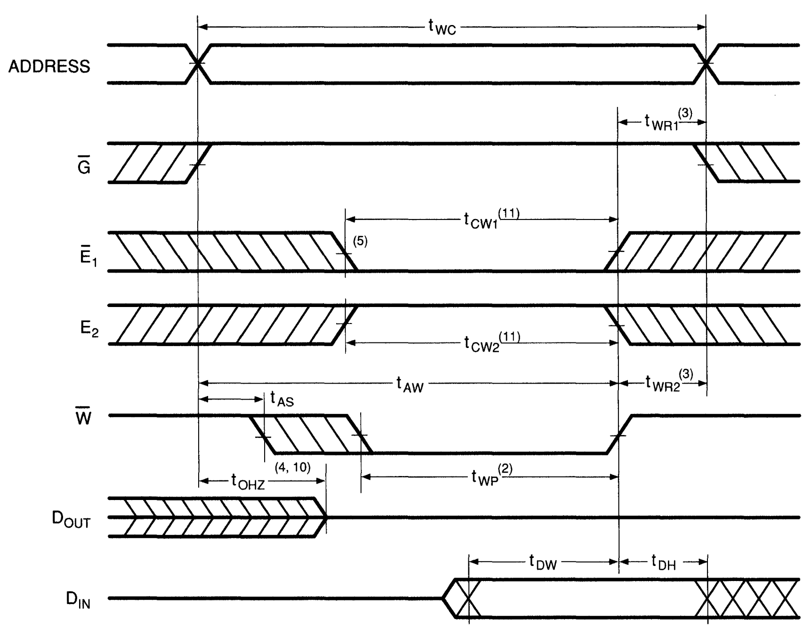
AC ELECTRICAL CHARACTERISTICS (over the operating range)

WRITE CYCLE

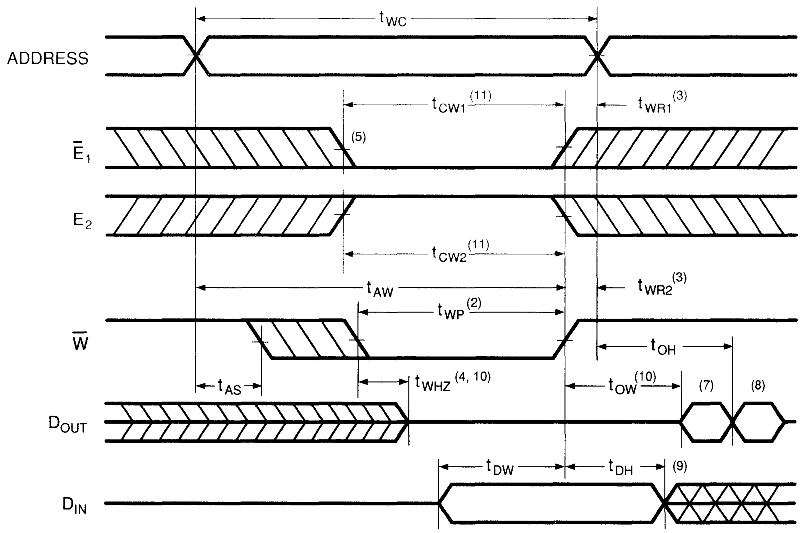
JEDEC PARAMETER NAME	PARAMETER NAME	PARAMETER		MS64100-25 MIN.	TYP.	MAX.	MS64100-35 MIN.	TYP.	MAX.	UNIT
t_{AVAX}	t_{WC}	Write Cycle Time		25	-	-	35	-	-	ns
t_{E1LWH}	t_{CW1}	Chip Enable to End of Write		16	-	-	26	-	-	ns
t_{E2LWH}	t_{CW2}	Chip Enable to End of Write		13	-	-	20	-	-	ns
t_{AVWL}	t_{AS}	Address Set up Time		0	-	-	0	-	-	ns
t_{AVWH}	t_{AW}	Address Valid to End of Write		18	-	-	28	-	-	ns
t_{WLWH}	t_{WP}	Write Pulse Width		15	-	-	20	-	-	ns
t_{WHAX}	t_{WR1}	Write Recovery Time	$\overline{E}_1,\overline{W}$	0	-	-	0	-	-	ns
t_{E2LAX}	t_{WR2}	Write Recovery Time	E_2	0	-	-	0	-	-	ns
t_{WLQZ}	t_{WHZ}	Write to Output in High Z		0	-	8	0	-	14	ns
t_{DVWH}	t_{DW}	Data to Write Time Overlap		8	-	-	12	-	-	ns
t_{WHDX}	t_{DH}	Data Hold from Write Time		0	-	-	0	-	-	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z		1	-	15	1	-	15	ns
t_{WHQX}	t_{OW}	Output Active from End of Write		0	-	-	0	-	-	ns

SWITCHING WAVEFORMS (WRITE CYCLE)

WRITE CYCLE 1[1]



WRITE CYCLE 2(1,6)



NOTES:

1. $\overline{W}$ must be high during address transitions.
2. The internal write time of the memory is defined by the overlap of $\bar{E}_1$ and E_2 active and $\overline{W}$ low. All signals must be active to initiate a write and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
3. T_{WR} is measured from the earlier of $\bar{E}_1$ or $\overline{W}$ going high or E_2 going low at the end of write cycle.
4. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\bar{E}_1$ low transition or the E_2 high transition occurs simultaneously with the $\overline{W}$ low transitions or after the $\overline{W}$ transition, outputs remain in a high impedance state.
6. $\overline{G}$ is continuously low ($\overline{G} = V_{IL}$).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\bar{E}_1$ is low and E_2 is high during this period, DQ pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured ±500mV from steady state with C_L = 5pF as shown in Figure 1b on page 4. This parameter is guaranteed but not 100% tested.
11. t_{CW1} is measured from $\bar{E}_1$ going low to the end of write; t_{CW2} is measured from E_2 going high to the end of write.

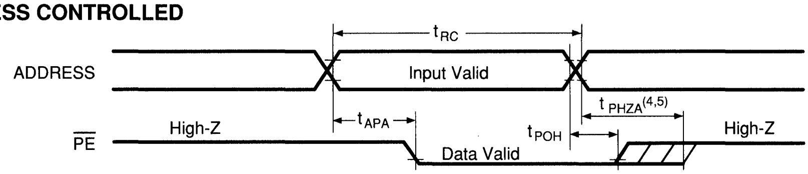
AC CHARACTERISTIC - Parity Read Cycle[1] (over the operating range)

PARAMETER NAME	PARAMETER	MS64100-25 MIN.	TYP.	MAX.	MS64100-35 MIN.	TYP.	MAX.	UNIT
t_{RC}	Read Cycle Time	25	-	-	35	-	-	ns
t_{APA}	Parity Error Access from Address[2]	-	-	28	-	-	40	ns
t_{APCS1}	Parity Error Access from $\overline{E}_1$[3] $\overline{E}_1$	-	-	28	-	-	40	ns
t_{APCS2}	Parity Error Access from E_2[3] E_2	-	-	14	-	-	15	ns
t_{APOE}	Parity Error Access from $\overline{G}$	-	-	12	-	-	14	ns
t_{POH}	Parity Error Hold from Address Change $\overline{E}_1$	3	-	-	3	-	-	ns
t_{PHZA}	Parity Error Disable from Address Change[4,5] E_2	1	-	20	1	-	25	ns
t_{PHZ1}	Parity Error Disable from $\overline{E}_1$[4,5]	1	-	15	1	-	15	ns
t_{PHZ2}	Parity Error Disable from E_2[4,5] $\overline{E}_1$	1	-	15	1	-	15	ns
t_{POHZ}	Parity Error Disable from $\overline{G}$[4,5] E_2	1	-	15	1	-	15	ns

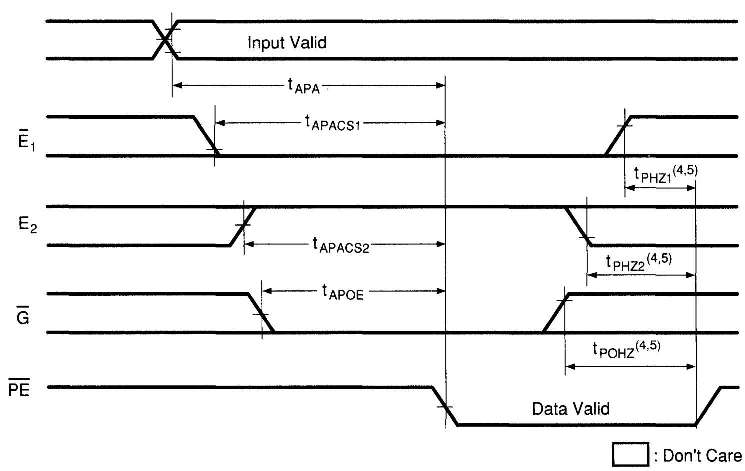
NOTES:
1. $\overline{W}$ is high for the Read Cycle.
2. Device is continuously selected, $\overline{E}_1 = V_{IL}$, $E_2 = V_{IH}$ and $\overline{G} = V_{IL}$.
3. Address valid prior to or coincident with $\overline{E}_1$ transition low, E_2 transition high.
4. Transition is specified at the point of ±500mV from steady state voltage.
5. This parameter is specified with Load II in Fig. 2.

PARITY READ FUNCTION TIMING DIAGRAM[1,6]

1) ADDRESS CONTROLLED



2) E_1, E_2 CONTROLLED[3]



NOTES:
1. $\overline{W}$ is high for the Read Cycle.
2. Device is continuously selected, $\overline{E}_1$ = "L", E_2 = "H" and $\overline{G}$ = "L".
3. Address valid prior to or coincident with $\overline{E}_1$ transition low, E_2 transition high.
4. Transition is specified at the point of ±500mV from steady state voltage.
5. This parameter is specified with Load II in Fig. 2.
6. When error occurred, $\overline{PE}$ pin outputs "L". But when no error, $\overline{PE}$ pin is in High-Z state.

ORDERING INFORMATION

SPEED (ns)	ORDERING PART NUMBER	PACKAGE REFERENCE NO.	TEMPERATURE RANGE
25	MS64100-25NC	P32-3	0°C to +70°C
25	MS64100-25FC		0°C to +70°C
35	MS64100-35NC	S32-1	0°C to +70°C
35	MS64100-35FC		0°C to +70°C

ADVANCE INFORMATION

32K x 9 High Speed CMOS Static RAM

FEATURES

- High speed – 25/35 ns (Max.)
- 9th bit for parity
- Automatic power-down when chip disabled
- Lower power consumption:
  - 715mW (Max.) Operating
  - 138mW (Max.) Standby
- TTL compatible interface levels
- Single 5V power supply
- Fully static operation
- Three state outputs
- Two chip enables ($\overline{E}_1$ and E_2) for simple memory expansion
- Fast E_2 access time (14ns) to support cache applications.

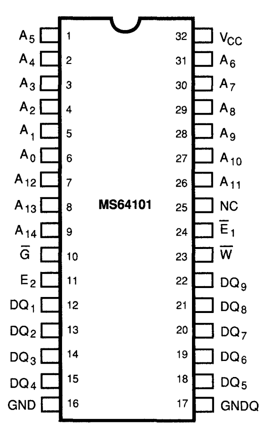
DESCRIPTION

The MOSEL MS64101 is a high performance, low power CMOS static RAM organized as 32768 words by 9 bits. The device supports easy memory expansion with both an active LOW chip enable ($\overline{E}_1$) and an active High chip enable (E_2), as well as an active LOW output enable ($\overline{G}$) and three-state outputs. An automatic power-down feature is included which reduces the chip power significantly.

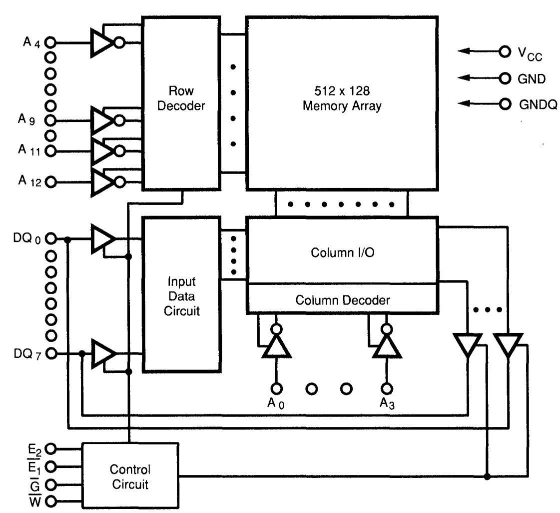
The device operates from a single 5 Volt power supply. All inputs and outputs are TTL compatible.

The MOSEL MS6287 is packaged in a space saving 32 pin 300 mil plastic DIP package and 330 mil SO package.

PIN CONFIGURATIONS



FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

A_0 - A_{12} Address Inputs

These 13 address inputs select one of the 8192 8-bit words in the RAM.

$\overline{E}_1$ Chip Enable 1 Input

E_2 Chip Enable 2 Input

$\overline{E}_1$ is active LOW and E_2 is active HIGH. Both chip enables must be active to read from or write to the device. If either chip enable is not active, the device is deselected and is in a standby power mode. The DQ pins will be in the high-impedance state when the device is deselected.

$\overline{G}$ Output Enable Input

The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when $\overline{G}$ is inactive.

$\overline{W}$ Write Enable Input

The write enable input is active LOW and controls read and write operations. With the chip selected, when $\overline{W}$ is HIGH and $\overline{G}$ is LOW, output data will be present at the DQ pins; when $\overline{W}$ is LOW, the data present on the DQ pins will be written into the selected memory location.

DQ_1 - DQ_8 Data Input/Output Ports

These 8 bidirectional ports are used to read data from or write data into the RAM.

V_{CC} Power Supply

GND Ground

3

TRUTH TABLE

$\overline{E}_1$	E_2	$\overline{W}$	$\overline{G}$	MODE	SUPPLY CURRENT	I/O STATE
H	X	X	X	Standby	I_{SB}	High Z
L	L	X	X	Deselect	I_{CC}	High Z
L	H	H	H	D_{OUT} Disable	I_{CC}	High Z
L	H	H	L	Read	I_{CC}	D_{OUT}
L	H	L	X	Write	I_{CC}	D_{IN}

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	PARAMETER	RATING	UNITS
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_{BIAS}	Temperature Under Bias	–0 to +85	°C
T_{STG}	Storage Temperature	–45 to +125	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	20	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

DC ELECTRICAL CHARACTERISTICS (over the operating range)

PARAMETER NAME	PARAMETER	TEST CONDITIONS		MS64101 MIN.	TYP.(1)	MAX.	UNITS
V_{IL}	Guaranteed Input Low Voltage(2)			–2.0	-	0.8	V
V_{IH}	Guaranteed Input High Voltage(2)			2.2	-	6.0	V
I_{IL}	Input Leakage Current	V_{CC} = Max, V_{IN} = 0V to V_{CC}		–5	-	5	µA
I_{OL}	Output Leakage Current	V_{CC} = Max, $\overline{E}_1 = V_{IH}$, or $E_2 = V_{IL}$, or $\overline{G} = V_{IH}$, V_{IN} = 0V t o V_{CC}		–5	-	5	µA
V_{OL}	Output Low Voltage	V_{CC} = Min, I_{OL} = 8mA		-	-	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min, I_{OH} = –4mA		2.4	-	-	V
I_{CC}	Operating Power Supply Current	V_{CC} = Max, $\overline{E}_1 = V_{IL}$, $I_{I/O}$ = 0mA, F = F_{max}(3)	25 ns	-	-	130	mA
			35 ns	-	-	110	
I_{CCSB}	Standby Power Supply Current	V_{CC} = Max, $\overline{E}_1 = V_{IH}$, $I_{I/O}$ = 0mA , $V_{IN} \leq 0.2V$		-	-	25	mA
I_{CCSB1}	Power Down Power Supply Current	V_{CC} = Max, $\overline{E}_1 > V_{CC} - 0.2V$ $V_{IN} > V_{CC} - 0.2V$ or $V_{IN} < 0.2V$		-	-	15	mA

1. Typical characteristics are at V_{cc} = 5V, T_A = 25°C.
2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included; –2.0 V_{IL} min for pulse width of less than 20ns: V_{IL} min = –0.5V at DC levels
3. $F_{MAX} = 1/t_{RC}$.

CAPACITANCE(1) (T_A = 25°C, f = 1.0MHz)

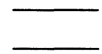
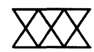
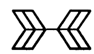
SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	7	pF
C_{DQ}	Input/Output Capacitance	$V_{I/O}$ = 0V	8	pF

1. This parameter is guaranteed and not tested.

AC TEST CONDITIONS

Input Pulse Levels	0.6 to 2.4V
Input Rise and Fall Times	3 ns
Input and Output Timing Reference Level	Input : V_{IL} = 0.8V, V_{IH} = 2.2V Output: V_{IL} = 0.8V, V_{IH} = 2.2V

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

AC TEST LOADS AND WAVEFORMS

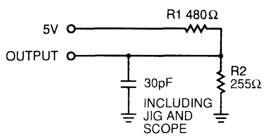


Figure 1a

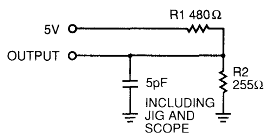
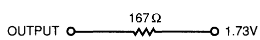


Figure 1b

Equivalent to:

THEVENIN EQUIVALENT



ALL INPUT PULSES

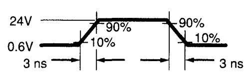


Figure 2

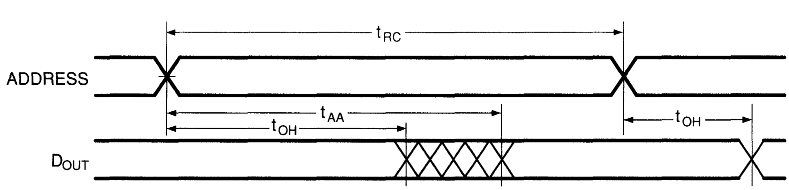
AC ELECTRICAL CHARACTERISTICS (over the operating range)

READ CYCLE

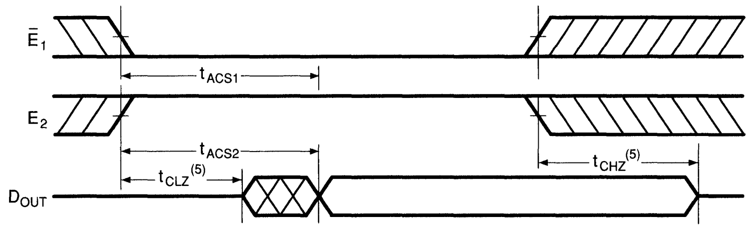
JEDEC PARAMETER NAME	PARAMETER NAME	PARAMETER		MS64101-25			MS64101-35			UNIT
				MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
t_{AVAX}	t_{RC}	Read Cycle Time		25	-	-	35	-	-	ns
t_{AVQV}	t_{AA}	Address Access Time		-	-	25	-	-	35	ns
t_{E1LQV}	t_{ACS1}	Chip Enable Access Time	$\overline{E}_1$	-	-	25	-	-	35	ns
t_{E2HQV}	t_{ACS2}	Chip Enable Access Time	E_2	-	-	14	-	-	15	ns
t_{GLQV}	t_{OE}	Output Enable to Output Valid		-	-	12	-	-	14	ns
t_{E1LQX}	t_{CLZ1}	Chip Enable to Output Low Z	$\overline{E}_1$	5	-	-	8	-	-	ns
t_{E2HQX}	t_{CLZ2}	Chip Enable to to Output Low Z	E_2	2	-	-	3	-	-	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z		2	-	-	3	-	-	ns
t_{E1HQZ}	t_{CHZ1}	Chip Disable to Output in High Z	$\overline{E}_1$	1	-	15	1	-	15	ns
t_{E2LQZ}	t_{CHZ2}	Chip Disable to Output in High Z	E_2	1	-	15	1	-	15	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z		1	-	15	1	-	15	ns
t_{AXQX}	t_{OH}	Output Hold from Address Change		3	-	-	3	-	-	ns

SWITCHING WAVEFORMS (READ CYCLE)

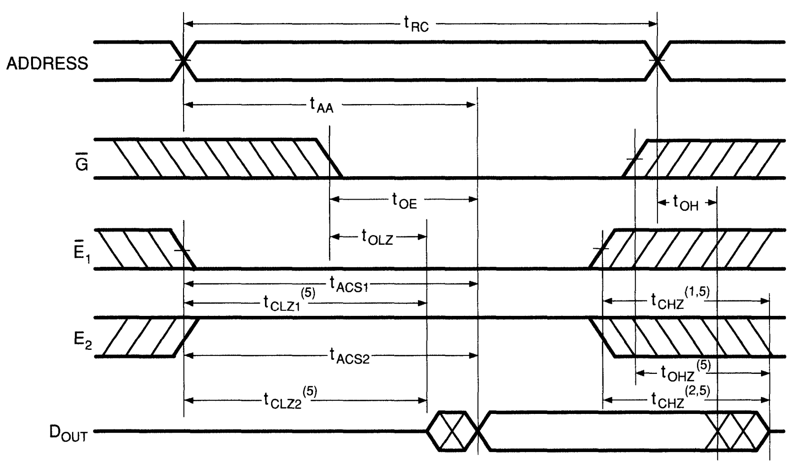
READ CYCLE 1(1,2,4)



READ CYCLE 2(1,3,4)



READ CYCLE 3(1,4)



NOTES:
1. $\overline{W}$ is high for READ Cycle.
2. Device is continuously selected $\overline{E}_1 = V_{IL}$ and $E_2 = V_{IH}$.
3. Address valid prior to or coincident with $\overline{E}_1$ transition low and/or E_2 transition high.
4. $\overline{G} = V_{IL}$.
5. Transition is measured ± 500mV from steady state with C_L = 5pF as shown in Figure 1b. This parameter is guaranteed but not 100% tested.

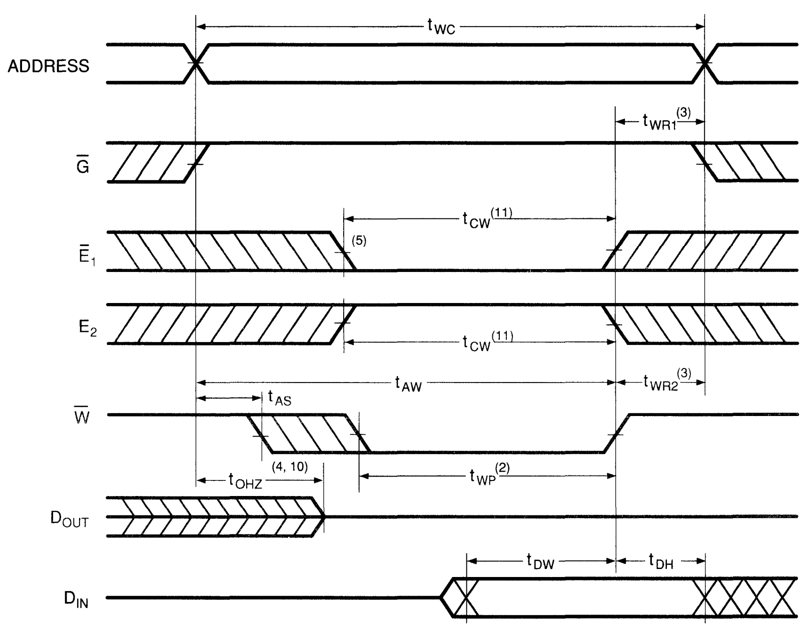
AC ELECTRICAL CHARACTERISTICS (over the operating range)

WRITE CYCLE

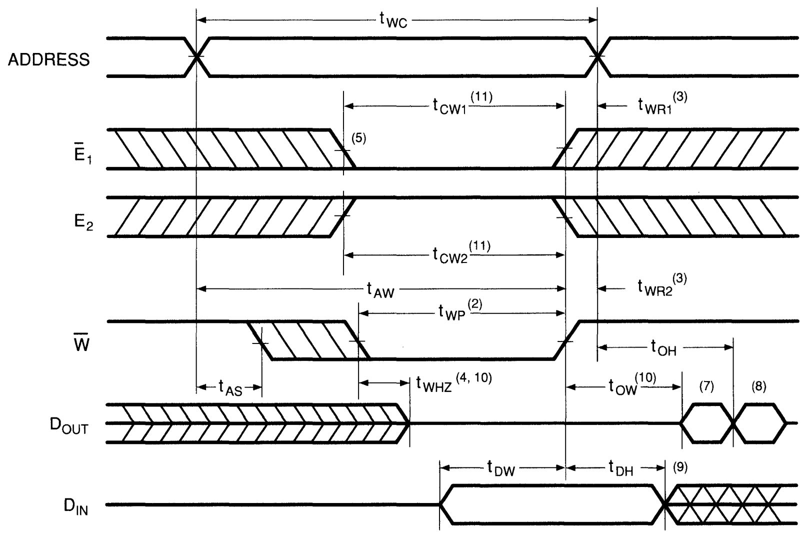
JEDEC PARAMETER NAME	PARAMETER NAME	PARAMETER		MS64101-25 MIN.	TYP.	MAX.	MS64101-35 MIN.	TYP.	MAX.	UNIT
t_{AVAX}	t_{WC}	Write Cycle Time		25	-	-	35	-	-	ns
t_{E1LWH}	t_{CW1}	Chip Enable to End of Write		16	-	-	26	-	-	ns
t_{E2LWH}	t_{CW2}	Chip Enable to End of Write		13	-	-	20	-	-	ns
t_{AVWL}	t_{AS}	Address Set up Time		0	-	-	0	-	-	ns
t_{AVWH}	t_{AW}	Address Valid to End of Write		18	-	-	28	-	-	ns
t_{WLWH}	t_{WP}	Write Pulse Width		15	-	-	20	-	-	ns
t_{WHAX}	t_{WR1}	Write Recovery Time	$\overline{E}_1,\overline{W}$	0	-	-	0	-	-	ns
t_{E2LAX}	t_{WR2}	Write Recovery Time	E_2	0	-	-	0	-	-	ns
t_{WLQZ}	t_{WHZ}	Write to Output in High Z		0	-	8	0	-	14	ns
t_{DVWH}	t_{DW}	Data to Write Time Overlap		8	-	-	12	-	-	ns
t_{WHDX}	t_{DH}	Data Hold from Write Time		0	-	-	0	-	-	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z		1	-	15	1	-	15	ns
t_{WHQX}	t_{OW}	Output Active from End of Write		0	-	-	0	-	-	ns

SWITCHING WAVEFORMS (WRITE CYCLE)

WRITE CYCLE 1[1]



WRITE CYCLE 2(1,6)



NOTES:

1. $\overline{W}$ must be high during address transitions.
2. The internal write time of the memory is defined by the overlap of $\overline{E}_1$ and E_2 active and $\overline{W}$ low. All signals must be active to initiate a write and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
3. T_{WR} is measured from the earlier of $\overline{E}_1$ or $\overline{W}$ going high or E_2 going low at the end of write cycle.
4. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{E}_1$ low transition or the E_2 high transition occurs simultaneously with the $\overline{W}$ low transitions or after the $\overline{W}$ transition, outputs remain in a high impedance state.
6. $\overline{G}$ is continuously low ($\overline{G} = V_{IL}$).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\overline{E}_1$ is low and E_2 is high during this period, DQ pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured ±500mV from steady state with C_L = 5pF as shown in Figure 1b on page 4. This parameter is guaranteed but not 100% tested.
11. t_{CW1} is measured from $\overline{E}_1$ going low to the end of write; t_{CW2} is measured from E_2 going high to the end of write,

ORDERING INFORMATION

SPEED (ns)	ORDERING PART NUMBER	PACKAGE REFERENCE NO.	TEMPERATURE RANGE
25	MS64101-25NC	P32-3	0°C to +70°C
35	MS64101-35NC		0°C to +70°C
25	MS64101-25FC	S32-1	0°C to +70°C
35	MS64101-35FC		0°C to +70°C

MOSEL

MS7200/ 7201A/ 7202A

256 x 9, 512 x 9, 1K x 9 CMOS FIFO

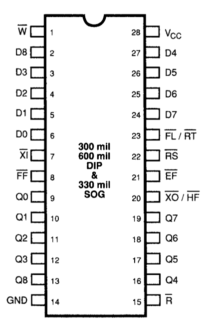
PRELIMINARY

FEATURES

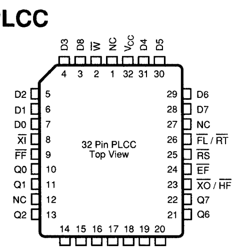
- First-In/First-Out static RAM based dual port memory
- Three densities in a x9 configuration
- Low power versions
- Includes empty, full, and half full status flags
- Direct replacement for industry standard Mostek and IDT
- Ultra high-speed 30 MHz FIFOs available with 33 ns cycle times.
- Fully expandable in both depth and width
- Simultaneous and asynchronous read and write
- Auto retransmit capability
- TTL compatible interface, single 5V ± 10% power supply
- Available in 28 pin 300 mil and 600 mil plastic DIP, 32 Pin PLCC and 330 mil SOG

PIN CONFIGURATIONS

28-PIN PDIP



32-PIN PLCC



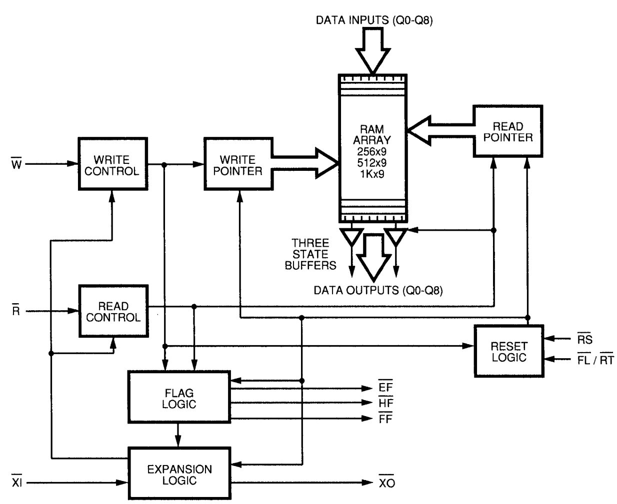
DESCRIPTION

The MOSEL MS7200/7201A/7202A are dual-port static RAM based CMOS First-In/First-Out (FIFO) memories organized in nine-bit wide words. The devices are configured so that data is read out in the same sequential order that it was written in. Additional expansion logic is provided to allow for unlimited expansion of both word size and depth.

The dual-port RAM array is internally sequenced by independent Read and Write pointers with no external addressing needed. Read and write operations are fully asynchronous and may occur simultaneously, even with the device operating at full speed. Status flags are provided for full, empty, and half-full conditions to eliminate data underflow and overflow. The x9 architecture provides an additional bit which may be used as a parity or control bit. In addition, the devices offer a retransmit capability which resets the Read pointer and allows for retransmission from the beginning of the data.

The MS7200/7201A/7202A are available in a range of frequencies from 10 to 30 MHz (33 - 100 ns cycle times). A low power version with a 500µA power down supply current is available. They are manufactured on MOSEL's high performance 1.2µ CMOS process and operate from a single 5V power supply.

BLOCK DIAGRAM



SIGNAL DESCRIPTIONS

INPUTS:

Data In (D_0 - D_8)

These data inputs accept 9-bit data words for sequential storage in the FIFO during write operations.

CONTROLS:

Reset ($\overline{RS}$)

The reset input is active LOW. When asserted, the device is asynchronously reset, and both the read and write internal pointers are set to the first location in the FIFO. A Reset is required after power-up before a write operation can occur. Both Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) must be HIGH during Reset.

Read Enable ($\overline{R}$)

The read enable input is active LOW. As long as the Empty Flag ($\overline{EF}$) is not set, the read cycle is started on the falling edge of this signal. The data is accessed on a First-In/First-Out basis, independent of any write activity, and is presented on the Data Output pins (Q0 - Q8). When $\overline{R}$ goes HIGH the Data Output pins return to the high impedance state, and the read pointer is incremented. When the FIFO is empty or all of the data has been read, the Empty Flag will be set and further read operations are inhibited until a valid write operation has been performed.

Write Enable ($\overline{W}$)

The write enable input is active LOW. As long as the Full Flag ($\overline{FF}$) is not set, the write cycle is started on the falling edge of this signal. The data present on the Data Input pins (D0 - D8) is stored sequentially, independent of any read activity. When $\overline{W}$ goes HIGH the write cycle is terminated and the write pointer is incremented. When the maximum capacity of the FIFO has been reached the Full Flag will be set, and further write operations are inhibited until a valid read operation has been performed.

Expansion In ($\overline{XI}$)

This input pin serves two purposes. When grounded, it indicates that the device is being operated in the single device mode. In Depth Expansion mode, this pin is connected to the Expansion Out Output ($\overline{XO}$) of the previous device.

First Load/Retransmit ($\overline{FL}/\overline{RT}$)

This is a dual-purpose input. In single device mode (when Expansion In ($\overline{XI}$) is grounded) this pin acts as the retransmit input. A LOW pulse on this will reset the read pointer to the first memory location of the FIFO. The write pointer is unaffected. Both the read enable ($\overline{R}$) and write enable ($\overline{W}$) inputs must remain HIGH during the retransmit cycle.

In Depth Expansion mode this pin acts as a first load indicator. It must be grounded on the first device in the chain to indicate which device is the first to receive data.

OUTPUTS:

Data Output (Q_0 - Q_8)

A 9 bit data word from the FIFO is output on these pins during read operations. They are in the high impedance state whenever $\overline{R}$ is HIGH.

Empty Flag ($\overline{EF}$)

This output is active LOW. When all of the data has been read from the FIFO (defined as when the Read pointer is one location behind the Write pointer) this flag will be set. The Data Output pins will be forced into the high impedance state, and all further read operations will be inhibited until a valid write operation has been performed (which will reset this flag).

Full Flag ($\overline{FF}$)

This output is active LOW. To prevent data overflow, when the maximum capacity of the FIFO has been reached (defined as when the Write pointer is one location behind the Read pointer) this flag will be set. All further write operations will be inhibited until a valid read operation has been performed (which will reset this flag).

Expansion Out/Half Full Flag ($\overline{XO}/\overline{HF}$)

This dual-purpose output is active LOW. In single device mode (when Expansion In ($\overline{XI}$) is grounded) this flag will be set at the falling edge of the next write operation after the FIFO has reached one-half of its maximum capacity. This flag will remain set as long as the difference between the read pointer and the write pointer is greater than one-half of the maximum capacity of the FIFO.

In Depth Expansion mode, this output is connected to the Expansion In Input of the next device in the chain. The Expansion Out pin provides a pulse to the next device in the chain when the last memory location has been reached.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	CONDITION	UNIT
V_{TERM}	Terminal Voltage with Repect to GND	-0.5 to +7.0	V
T_{BIAS}	Temperature Under Bias	-10 to +125	°C
T_{STG}	Storage Temperature	-60 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	20	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

RANGE	AMBIENT TEMPERATURE	Vcc
Commercial	0°C to + 70°C	5V ± 10%

CAPACITANCE[1] (T_A = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	4	pF
C_Q	Output Capacitance	V_{DQ} = 0V	6	pF

DC ELECTRICAL CHARACTERISTICS (over the commercial operating range)

PARAMETER NAME	PARAMETER	TEST CONDITIONS	MS7200/7201A 7202A (-25, -35) MIN.	TYP.	MAX.	MS7200/7201A 7202A (-50, -80) MIN.	TYP.	MAX.	UNITS
V_{IL}	Input Low Voltage		-	-	0.8	-	-	0.8	V
V_{IH}	Input High Voltage		2.0	-	-	2.0	-	-	V
I_{IL}	Input Leakage Current	V_{CC} = Max, V_{IN} = 0Vto V_{CC}	-1		1	-1		1	µA
I_{OL}	Output Leakage Current	V_{CC} = Max, $\overline{R}$= V_{IH}, V_{IN} = 0V toV_{CC}	-10		10	-10		10	µA
V_{OL}	Output Low Voltage	V_{CC} = Min, I_{OL} = 8mA	-	-	0.4	-	-	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min, I_{OH} = -2mA	2.4	-	-	2.4	-	-	V
I_{CC1}	Operating Power Supply Current	V_{CC} = Max, $I_{I/O}$ = 0mA, F = F_{max}	-	-	125	-	50	80	mA
I_{CC2}	Average Standby Current	V_{CC} = Max, $\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL}$ / $\overline{RT}$ = V_{IH}, $I_{I/O}$ = 0mA	-	-	15	-	5	8	mA
$I_{CCSB(S)}$	Power Down Supply Current (Standard Power)	V_{CC} = Max, $\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL}$ / $\overline{RT}$ > V_{CC} - 0.2V, V_{IN} > V_{CC}-0.2V or V_{IN} < 0.2V	-	-	5	-	-	5	mA
$I_{CCSB(L)}$	Power Down Supply Current (Low Power)	V_{CC} = Max, $\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL}$ / $\overline{RT}$ > V_{CC} - 0.2V, V_{IN} > V_{CC}-0.2V or V_{IN} < 0.2V	-	-	500	-	-	500	µA

TRUTH TABLES

SINGLE DEVICE CONFIGURATION/WIDTH EXPANSION MODE

MODE	INPUTS			INTERNAL STATUS		OUTPUTS		
	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location Zero	Location Zero	0	1	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X
Read/Write	1	1	0	Increment [1]	Increment [1]	X	X	X

NOTE:
1. Pointer will increment if flag is high.

DEPTH EXPANSION/COMPOUND EXPANSION MODE

MODE	INPUTS			INTERNAL STATUS		OUTPUTS	
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset-First Device	0	0	(1)	Location Zero	Location Zero	0	1
Reset all Other Devices	0	1	(1)	Location Zero	Unchanged	0	1
Read/Write	1	X	(1)	X	X	X	X

NOTE:
1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device. See Figure 15.
RS = Reset Input. $\overline{FL}/\overline{RT}$ = First Load/Retransmit. $\overline{EF}$ = Empty Flag Output. $\overline{FF}$ Full Flag Output. $\overline{XI}$ = Expansion Input.

AC ELECTRICAL CHARACTERISTICS (over the commercial operating range)

PARAMETER NAME	PARAMETER	MS7200-25 MS7201A-25 MS7202A-25 Min.	Max.	MS7200-35 MS7201A-35 MS7202A-35 Min.	Max.	MS7200-50 MS7201A-50 MS7202A-50 Min.	Max.	MS7200-80 MS7201A-80 MS7202A-80 Min.	Max.	UNITS
f_S	Shift Frequency	--	30	--	22.2	--	15	--	10	MHz
READ CYCLE										
t_{RC}	Read Cycle Time	33	--	45	--	65	--	100	--	ns
t_A	Access Time	--	25	--	35	--	50	--	80	ns
t_{RPW}	Read Pulse Width	25	--	35	--	50	--	80	--	ns
t_{RR}	Read Recovery Time	8	--	10	--	15	--	20	--	ns
t_{RLZ}(2)	Read Pulse Low to Data Bus at Low Z	5	--	5	--	10	--	10	--	ns
t_{RHZ}(2,3)	Read Pulse High to Data Bus at High Z	--	18	--	20	--	30	--	30	ns
t_{DV}	Data Valid from Read Pulse High	5	--	5	--	5	--	5	--	ns
WRITE CYCLE										
t_{WC}	Write Cycle Time	33	--	45	--	65	--	100	--	ns
t_{WPW}(1)	Write Pulse Width	25	--	35	--	50	--	80	--	ns
t_{WR}	Write Recovery Time	8	--	10	--	15	--	20	--	ns
t_{DS}	Data Setup Time	15	--	18	--	30	--	40	--	ns
t_{DH}	Data Hold Time	0	--	0	--	5	--	10	--	ns
t_{WLZ}(2,3)	Write Pulse High to Data Bus at Low Z	5	--	10	--	15	--	20	--	ns
FLAG TIMING										
t_{REF}	Read Low to Empty Flag Low	--	25	--	30	--	45	--	60	ns
t_{RHF}	Read High to Half Full Flag High	--	33	--	45	--	65	--	100	ns
t_{RFF}	Read High to Full Flag High	--	25	--	30	--	45	--	60	ns
t_{WEF}	Write High to Empty Flag High	--	25	--	30	--	45	--	60	ns
t_{WFF}	Write Low to Full Flag Low	--	25	--	30	--	45	--	60	ns
t_{WHF}	Write Low to Half Full Flag Low	--	33	--	45	--	65	--	100	ns
t_{RPE}	Read Pulse Width After $\overline{EF}$ High	25	--	35	--	50	--	80	--	ns
t_{WPF}	Write Pulse Width After $\overline{FF}$ High	25	--	35	--	50	--	80	--	ns
RESET TIMING										
t_{RSC}	Reset Cycle Time	33	--	45	--	65	--	100	--	ns
t_{RS}(1)	Reset Pulse Width	25	--	35	--	50	--	80	--	ns
t_{RSS}	Reset Set Up Time	25	--	35	--	50	--	80	--	ns
t_{RSR}	Reset Recovery Time	8	--	10	--	15	--	20	--	ns
t_{EFL}	Reset to Empty Flag Low	--	33	--	45	--	65	--	100	ns
t_{HFH}	Reset to Half Full Flag High	--	33	--	45	--	65	--	100	ns
t_{FFH}	Reset to Full Flag High	--	33	--	45	--	65	--	100	ns
RETRANSMIT TIMING										
t_{RTC}	Retransmit Cycle Time	33	--	45	--	65	--	100	--	ns
t_{RT}(1)	Retransmit Pulse Width	25	--	35	--	50	--	80	--	ns
t_{RTS}	Retransmit Set up Time	25	--	35	--	50	--	80	--	ns
t_{RTR}	Retransmit Recovery Time	8	--	10	--	15	--	20	--	ns
EXPANSION TIMING										
t_{XOL}	Read/Write to $\overline{XO}$ Low	--	25	--	35	--	50	--	80	ns
t_{XOH}	Read/Write to $\overline{XO}$ High	--	25	--	35	--	50	--	80	ns
t_{XI}	$\overline{XI}$ Pulse Width	25	--	35	--	50	--	80	--	ns
t_{XIS}	$\overline{XI}$ Set up Time	15	--	15	--	15	--	15	--	ns
t_{XIR}	$\overline{XI}$ Recovery Time	8	--	10	--	10	--	10	--	ns

NOTES:
1. Pulse widths less than minimum value are not allowed.
2. Values guaranteed by design, not currently tested.
3. Only applies to read data flow-through mode.

AC TEST CONDITIONS

Input Pulse Levels	0V~ 3.0V
Input Rise and Fall Times	5 ns
Timing Reference Level	1.5V

AC TEST LOADS AND WAVEFORMS

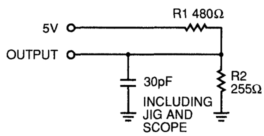


Figure 1a

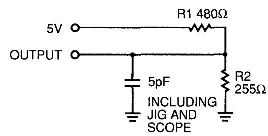
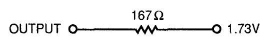


Figure 1b

Equivalent to:

THEVENIN EQUIVALENT



ALL INPUT PULSES

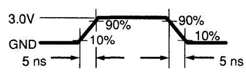


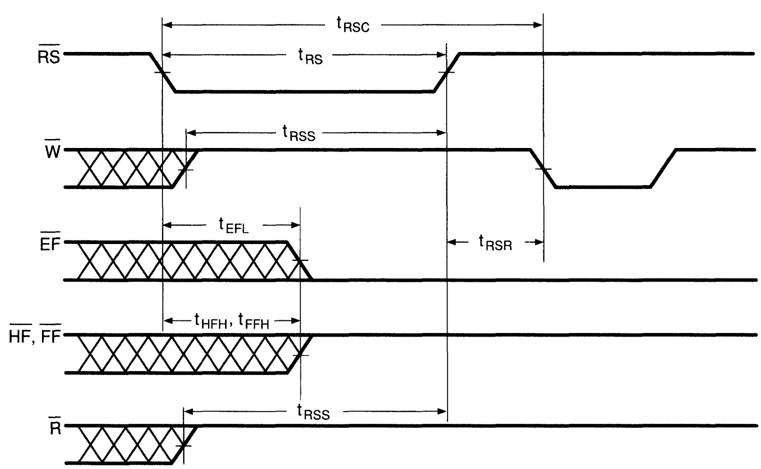
Figure 2

KEY TO SWITCHING WAVEFORMS

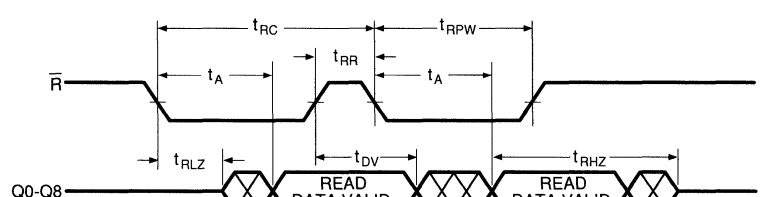
WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

TIMING WAVEFORMS

RESET

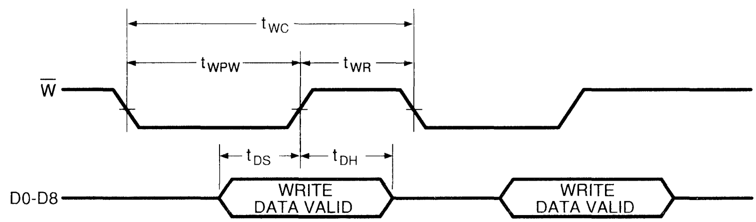


ASYNCHRONOUS READ OPERATION

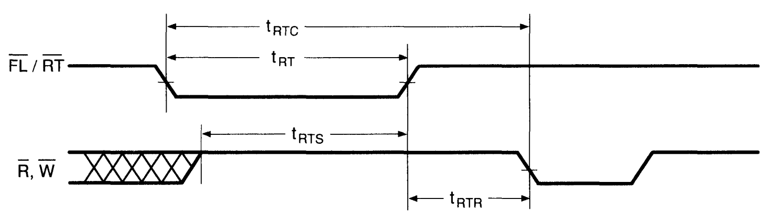


TIMING WAVEFORMS

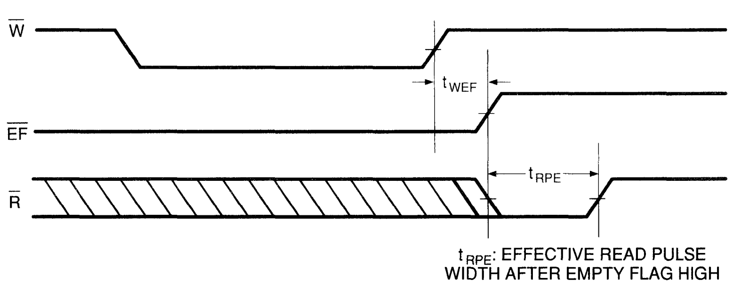
ASYNCHRONOUS WRITE OPERATION



RETRANSMIT

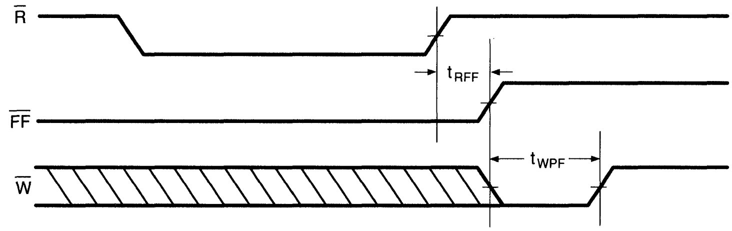


EMPTY FLAG TIMING



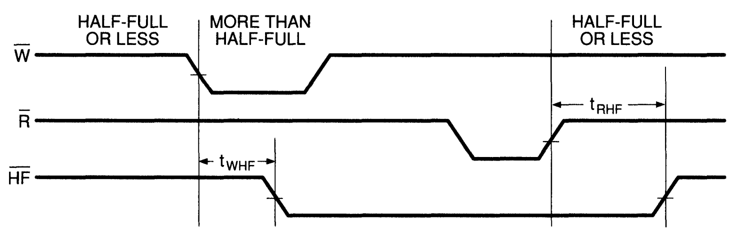
TIMING WAVEFORMS

FULL FLAG TIMING

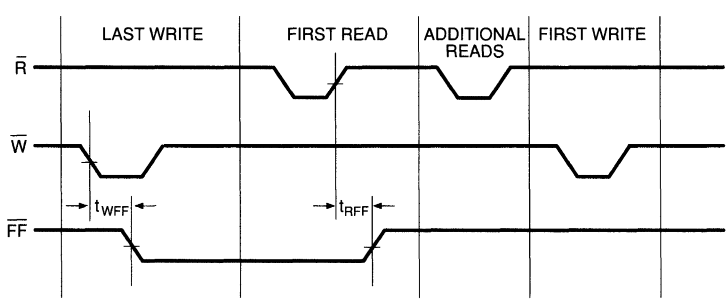


t_{WPF} : EFFECTIVE WRITE PULSE WIDTH AFTER FULL FLAG HIGH

HALF-FULL FLAG TIMING

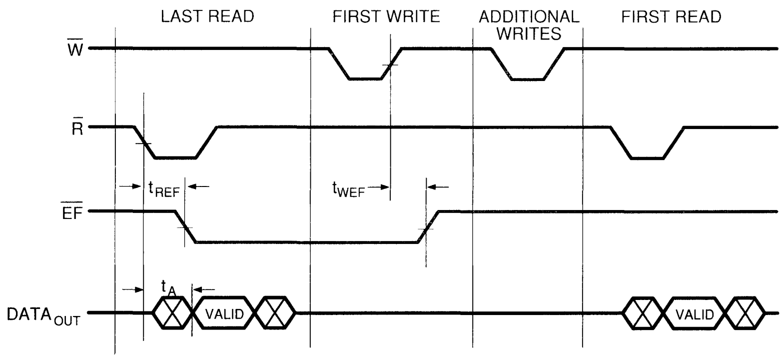


FULL FLAG FROM LAST WRITE TO FIRST READ

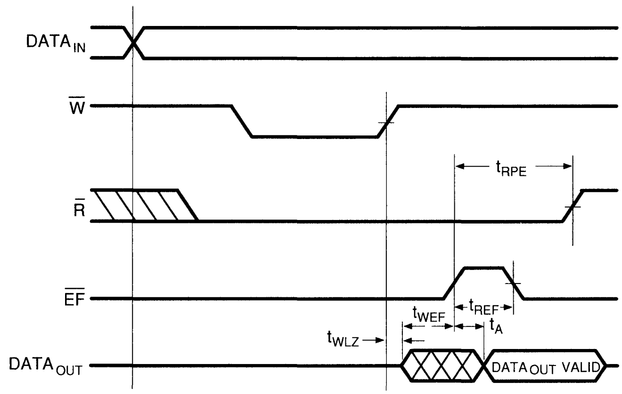


TIMING WAVEFORMS

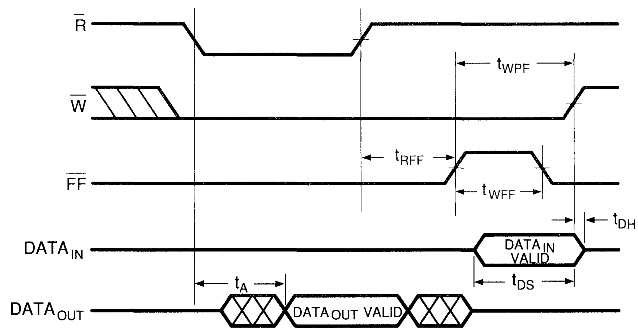
EMPTY FLAG FROM LAST READ TO FIRST WRITE



READ DATA FLOW-THROUGH MODE



WRITE DATA FLOW-THROUGH MODE



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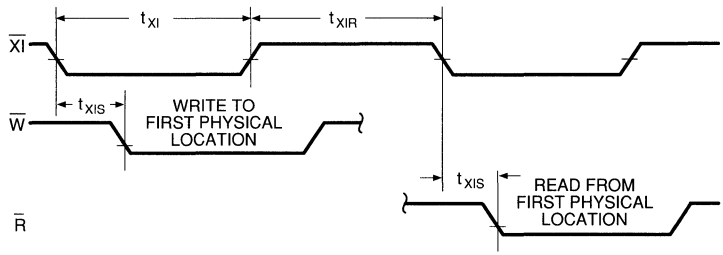
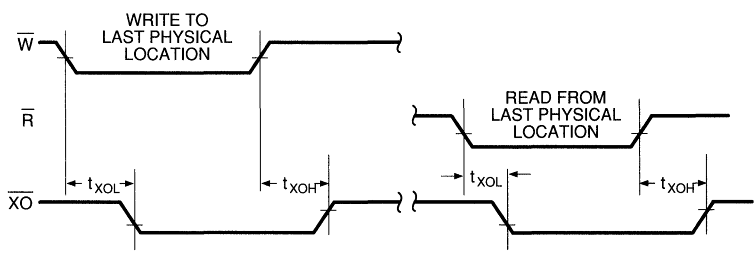
PID022

TIMING WAVEFORMS

EXPANSION IN



EXPANSION OUT



OPERATING MODES:

(Note: The7201A is used as example - these figures apply to all three devices, MS7200/7201A/7202A

SINGLE DEVICE MODE

When one MS7201A is used standalone in Single Device Mode, the Expansion In (XI) control input pin must be grounded. See Figure 3.

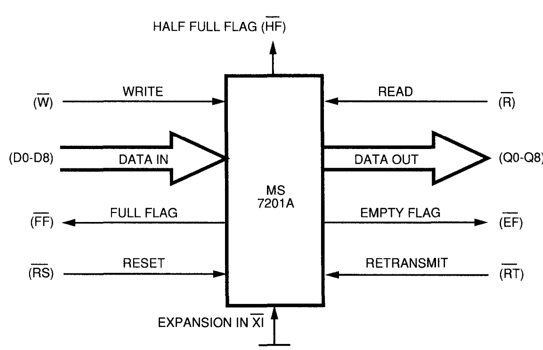


Figure 3. Single Device Mode

WIDTH EXPANSION MODE

Word width may be expanded by connecting the corresponding control input signals of multiple devices together. The EMPTY, HALF FULL and FULL FLAGS (EE, HF and FF) can be detected by any particular device. Figure 4 shows an 18 bit wide configuration using two devices. They may be configured to any word width in this manner.

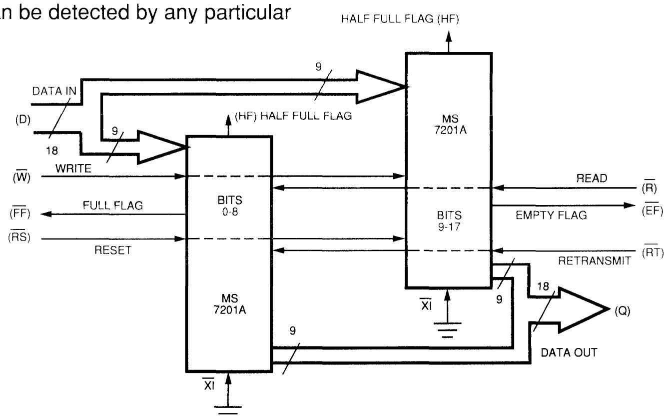


Figure 4. Width Expansion Mode

NOTES:

Flag detection is accomplished by monitoring the EF, HF and EF pins on the device used in the Width Expansion Mode. Do not connect output control signals together.

DEPTH EXPANSION (DAISY CHAIN) MODE

Word depths may be expanded in multiples of 512 words by Daisy Chaining the devices together as follows:

1. The FIRST LOAD (FL) control signal of the first device must be grounded. This FIFO represents word 1-512.
2. All other devices in the Daisy Chain must have the FIRST LOAD (FL) control signal tied to V_{CC} in the inactive-high state.
3. The EXPANSION OUT (XO) pin of each device must be connected to the EXPANSION IN (XI) pin of the next device as shown in Figure 5.
4. External logic is required to generate a common FULL FLAG (FF) and EMPTY FLAG (EF) signal by ORing all of the FFs together and ORing all of the EFs together.
5. The RETRANSMIT (RT) fuction and HALF FULL FLAG (HF) are not available in Daisy Chain Mode.

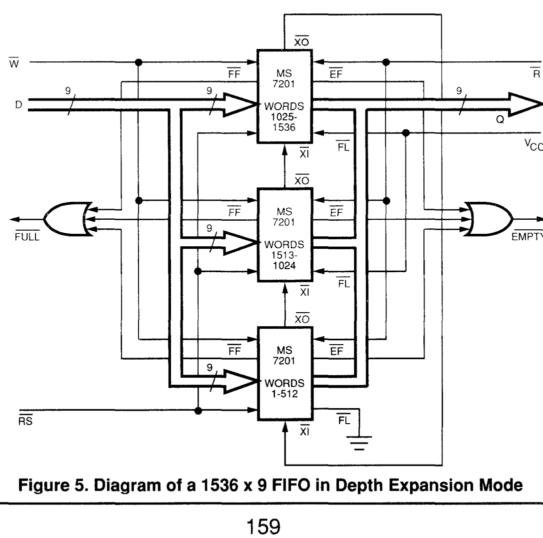


Figure 5. Diagram of a 1536 x 9 FIFO in Depth Expansion Mode

3

BIDIRECTIONAL MODE

Data buffering between two systems can be achieved by pairing two FIFO arrays as shown in Figure 6. This allows each system to READ and WRITE shared data. The FULL FLAG ($\overline{FF}$) must be monitored on the FIFO where WRITE ENABLE ($\overline{W}$) is used and the EMPTY FLAG ($\overline{EF}$) must be monitored on the FIFO where READ ENABLE ($\overline{R}$) is used. Both Width Expansion and Depth Expansion Modes may be used in combination with Bidirectional Mode.

COMPOUND EXPANSION MODE:

Both Width Expansion Mode and Depth Expansion (Daisy Chain) Mode can be used together to configure a large FIFO array (See Figure 4 and 5).

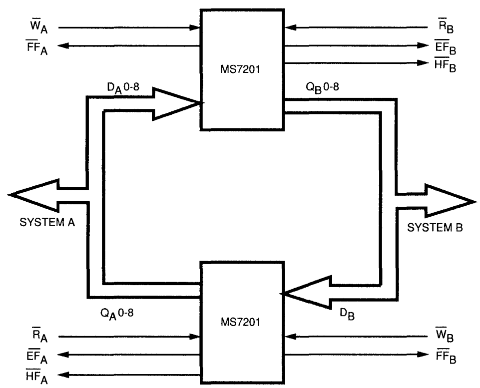


Figure 6. BiDirectional FIFO Mode

ORDERING INFORMATION

SPEED (ns)	ORDERING PART NUMBER (1)			PACKAGE REFERENCE NO.	TEMPERATURE RANGE
25		MS7201A-25PC	MS7202A-25PC	P28-1	0°C to +70°C
25	MS7200-25NC	MS7201A-25NC	MS7202A-25NC	P28-2	0°C to +70°C
25	MS7200-25JC	MS7201A-25JC	MS7202A-25JC	J32-1	0°C to +70°C
25	MS7200-25FC	MS7201A-25FC	MS7202A-25FC	S28-2	0°C to +70°C
35		MS7201A-35PC	MS7202A-35PC	P28-1	0°C to +70°C
35	MS7200-35NC	MS7201A-35NC	MS7202A-35NC	P28-2	0°C to +70°C
35	MS7200-35JC	MS7201A-35JC	MS7202A-35JC	J32-1	0°C to +70°C
35	MS7200-35FC	MS7201A-35FC	MS7202A-35FC	S28-2	0°C to +70°C
50		MS7201A-50PC	MS7202A-50PC	P28-1	0°C to +70°C
50	MS7200-50NC	MS7201A-50NC	MS7202A-50NC	P28-2	0°C to +70°C
50	MS7200-50JC	MS7201A-50JC	MS7202A-50JC	J32-1	0°C to +70°C
50	MS7200-50FC	MS7201A-50FC	MS7202A-50FC	S28-2	0°C to +70°C
80		MS7201A-80PC	MS7202A-80PC	P28-1	0°C to +70°C
80	MS7200-80NC	MS7201A-80NC	MS7202A-80NC	P28-2	0°C to +70°C
80	MS7200-80JC	MS7201A-80JC	MS7202A-80JC	J32-1	0°C to +70°C
80	MS7200-80FC	MS7201A-80FC	MS7202A-80FC	S28-2	0°C to +70°C

(1) For the low power version, add L after part number and before dash information. For example, MS7200L-25PC.

PRELIMINARY

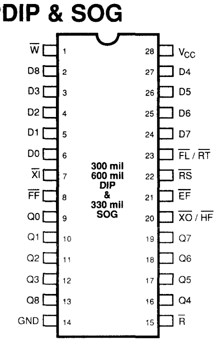
2K x 9, 4K x 9 CMOS FIFO

FEATURES

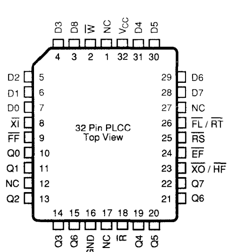
- First-In/First-Out static RAM based dual port memory
- Two densities (2K and 4K) in a x9 configuration
- Low power versions
- Includes empty, full, and half full status flags
- Direct replacement for industry standard IDT plus 300 mil DIP and 330 mil SOG
- Ultra high-speed 22.2 MHz FIFOs available with 45 ns cycle times.
- Fully expandable in both depth and width
- Simultaneous and asynchronous read and write
- Auto retransmit capability
- TTL compatible interface, single 5V ± 10% power supply
- Available in 28 pin 300 mil and 600 mil plastic DIP, 28 Pin 330 mil SOG and 32 Pin PLCC

PIN CONFIGURATIONS

28-PIN PDIP & SOG



32-PIN PLCC



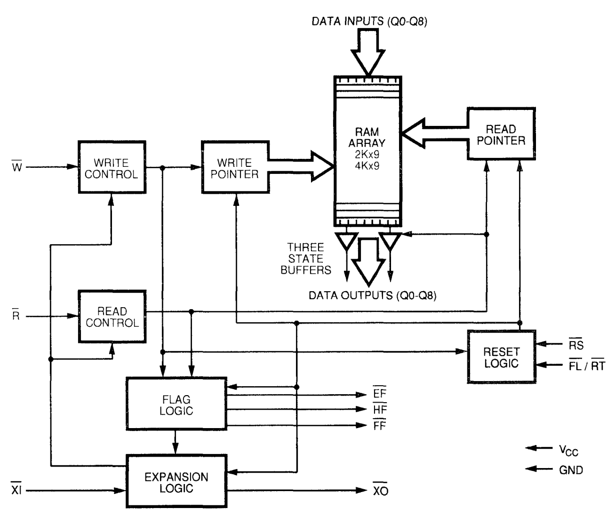
DESCRIPTION

The MOSEL MS7203/7204 are dual-port static RAM based CMOS First-In/First-Out (FIFO) memories organized in nine-bit wide words. The devices are configured so that data is read out in the same sequential order that it was written in. Additional expansion logic is provided to allow for unlimited expansion of both word size and depth.

The dual-port RAM array is internally sequenced by independent Read and Write pointers with no external addressing needed. Read and write operations are fully asynchronous and may occur simultaneously, even with the device operating at full speed. Status flags are provided for full, empty, and half-full conditions to eliminate data underflow and overflow. The x9 architecture provides an additional bit which may be used as a parity or control bit. In addition, the devices offer a retransmit capability which resets the Read pointer and allows for retransmission from the beginning of the data.

The MS7203/7204 are available in a range of frequencies from 10 to 22.2 MHz (45 - 100 ns cycle times). A low power version with a 500μA power down supply current is available. They are manufactured on MOSEL's high performance 1.2μ CMOS process and operate from a single 5V power supply.

BLOCK DIAGRAM



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SIGNAL DESCRIPTIONS

INPUTS:

Data In (D_0 - D_8)

These data inputs accept 9-bit data words for sequential storage in the FIFO during write operations.

CONTROLS:

Reset ($\overline{RS}$)

The reset input is active LOW. When asserted, the device is asynchronously reset, and both the read and write internal pointers are set to the first location in the FIFO. A Reset is required after power-up before a write operation can occur. Both Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) must be HIGH during Reset.

Read Enable ($\overline{R}$)

The read enable input is active LOW. As long as the Empty Flag ($\overline{EF}$) is not set, the read cycle is started on the falling edge of this signal. The data is accessed on a First-In/First-Out basis, independent of any write activity, and is presented on the Data Output pins (Q0 - Q8). When $\overline{R}$ goes HIGH the Data Output pins return to the high impedance state, and the read pointer is incremented. When the FIFO is empty or all of the data has been read, the Empty Flag will be set and further read operations are inhibited until a valid write operation has been performed.

Write Enable ($\overline{W}$)

The write enable input is active LOW. As long as the Full Flag ($\overline{FF}$) is not set, the write cycle is started on the falling edge of this signal. The data present on the Data Input pins (D0 - D8) is stored sequentially, independent of any read activity. When $\overline{W}$ goes HIGH the write cycle is terminated and the write pointer is incremented. When the maximum capacity of the FIFO has been reached the Full Flag will be set, and further write operations are inhibited until a valid read operation has been performed.

Expansion In ($\overline{XI}$)

This input pin serves two purposes. When grounded, it indicates that the device is being operated in the single device mode. In Depth Expansion mode, this pin is connected to the Expansion Out Output ($\overline{XO}$) of the previous device.

First Load/Retransmit ($\overline{FL}/\overline{RT}$)

This is a dual-purpose input. In single device mode (when Expansion In ($\overline{XI}$) is grounded) this pin acts as the retransmit input. A LOW pulse on this will reset the read pointer to the first memory location of the FIFO. The write pointer is unaffected. Both the read enable ($\overline{R}$) and write enable ($\overline{W}$) inputs must remain HIGH during the retransmit cycle.

In Depth Expansion mode this pin acts as a first load indicator. It must be grounded on the first device in the chain to indicate which device is the first to receive data.

OUTPUTS:

Data Output (Q_0 - Q_8)

A 9 bit data word from the FIFO is output on these pins during read operations. They are in the high impedance state whenever $\overline{R}$ is HIGH.

Empty Flag ($\overline{EF}$)

This output is active LOW. When all of the data has been read from the FIFO (defined as when the Read pointer is one location behind the Write pointer) this flag will be set. The Data Output pins will be forced into the high impedance state, and all further read operations will be inhibited until a valid write operation has been performed (which will reset this flag).

Full Flag ($\overline{FF}$)

This output is active LOW. To prevent data overflow, when the maximum capacity of the FIFO has been reached (defined as when the Write pointer is one location behind the Read pointer) this flag will be set. All further write operations will be inhibited until a valid read operation has been performed (which will reset this flag).

Expansion Out/Half Full Flag ($\overline{XO}/\overline{HF}$)

This dual-purpose output is active LOW. In single device mode (when Expansion In ($\overline{XI}$) is grounded) this flag will be set at the falling edge of the next write operation after the FIFO has reached one-half of its maximum capacity. This flag will remain set as long as the difference between the read pointer and the write pointer is greater than one-half of the maximum capacity of the FIFO.

In Depth Expansion mode, this output is connected to the Expansion In Input of the next device in the chain. The Expansion Out pin provides a pulse to the next device in the chain when the last memory location has been reached.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	CONDITION	UNIT
V_{TERM}	Terminal Voltage with Repect to GND	-0.5 to +7.0	V
T_{BIAS}	Temperature Under Bias	-10 to +125	°C
T_{STG}	Storage Temperature	-60 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	20	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

RANGE	AMBIENT TEMPERATURE	Vcc
Commercial	0°C to + 70°C	5V ± 10%

CAPACITANCE[1] (T_A = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	4	pF
C_Q	Output Capacitance	V_{DQ} = 0V	6	pF

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DC ELECTRICAL CHARACTERISTICS (over the commercial operating range)

PARAMETER NAME	PARAMETER	TEST CONDITIONS	MS7203, MS7204 (-35, -50, -80) MIN.	TYP.	MAX.	UNITS
V_{IL}	Input Low Voltage		-	-	0.8	V
V_{IH}	Input High Voltage		2.0	-	-	V
I_{IL}	Input Leakage Current	V_{CC} = Max, V_{IN} = 0Vto V_{CC}	-1		1	µA
I_{OL}	Output Leakage Current	V_{CC} = Max, $\overline{R}$ = V_{IH}, V_{IN} = 0V toV_{CC}	-10		10	µA
V_{OL}	Output Low Voltage	V_{CC} = Min, I_{OL} = 8mA	-	-	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min, I_{OH} = -2mA	2.4	-	-	V
I_{CC1}	Operating Power Supply Current	V_{CC} = Max, $I_{I/O}$ = 0mA, F = F_{max}	-	-	125	mA
I_{CC2}	Average Standby Current	V_{CC} = Max, $\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL}$ / $\overline{RT}$ = V_{IH}, $I_{I/O}$ = 0mA	-	-	15	mA
$I_{CCSB(S)}$	Power Down Power Supply Current (Standard Power)	V_{CC} = Max, $\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL}$ / $\overline{RT}$ > V_{CC}-0.2V, V_{IN} > V_{CC}-0.2V or V_{IN} < 0.2V	-	-	8	mA
$I_{CCSB(L)}$	Power Down Power Supply Current (Low Power)	V_{CC} = Max, $\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL}$ / $\overline{RT}$ > V_{CC}-0.2V, V_{IN} > V_{CC}-0.2V or V_{IN} < 0.2V	-	-	2	mA

TRUTH TABLES

SINGLE DEVICE CONFIGURATION/WIDTH EXPANSION MODE

MODE	INPUTS			INTERNAL STATUS		OUTPUTS		
	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location Zero	Location Zero	0	1	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X
Read/Write	1	1	0	Increment[1]	Increment[1]	X	X	X

NOTE:
1. Pointer will increment if flag is high.

DEPTH EXPANSION/COMPOUND EXPANSION MODE

MODE	INPUTS			INTERNAL STATUS		OUTPUTS	
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset-First Device	0	0	(1)	Location Zero	Location Zero	0	1
Reset all Other Devices	0	1	(1)	Location Zero	Unchanged	0	1
Read/Write	1	X	(1)	X	X	X	X

NOTE:
1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device. See Figure 5.
$\overline{RS}$ = Reset Input. $\overline{FL}/\overline{RT}$ = First Load/Retransmit. $\overline{EF}$ = Empty Flag Output. $\overline{FF}$ Full Flag Output. $\overline{XI}$ = Expansion Input.

AC ELECTRICAL CHARACTERISTICS (over the commercial operating range)

PARAMETER NAME	PARAMETER	MS7203-35 MS7204-35 MIN.	MAX.	MS7203-50 MS7204-50 MIN.	MAX.	MS7203-80 MS7204-80 MIN.	MAX.	UNITS
t_S	Shift Frequency	--	22.2	--	15.3	--	10	MHz
READ CYCLE								
t_{RC}	Read Cycle Time	45	--	65	--	100	--	ns
t_A	Access Time	--	35	--	50	--	80	ns
t_{RPW}	Read Pulse Width	35	--	50	--	80	--	ns
t_{RR}	Read Recovery Time	10	--	15	--	20	--	ns
t_{RLZ}(2)	Read Pulse Low to Data Bus at Low Z	5	--	10	--	10	--	ns
t_{RHZ}(2,3)	Read Pulse High to Data Bus at High Z	--	20	--	30	--	30	ns
t_{DV}	Data Valid from Read Pulse High	5	--	5	--	5	--	ns
WRITE CYCLE								
t_{WC}	Write Cycle Time	45	--	65	--	100	--	ns
t_{WPW}(1)	Write Pulse Width	35	--	50	--	80	--	ns
t_{WR}	Write Recovery Time	10	--	15	--	20	--	ns
t_{DS}	Data Setup Time	18	--	30	--	40	--	ns
t_{DH}	Data Hold Time	0	--	5	--	10	--	ns
t_{WLZ}(2,3)	Write Pulse High to Data Bus at Low Z	10	--	15	--	20	--	ns
FLAG TIMING								
t_{REF}	Read Low to Empty Flag Low	--	30	--	45	--	60	ns
t_{RHF}	Read High to Half Full Flag High	--	45	--	65	--	100	ns
t_{RFF}	Read High to Full Flag High	--	30	--	45	--	60	ns
t_{WEF}	Write High to Empty Flag High	--	30	--	45	--	60	ns
t_{WFF}	Write Low to Full Flag Low	--	30	--	45	--	60	ns
t_{WHF}	Write Low to Half Full Flag Low	--	45	--	65	--	100	ns
t_{RPE}	Read Pulse Width After EF High	35	--	50	--	80	--	ns
t_{WPF}	Write Pulse Width After $\overline{FF}$ High	35	--	50	--	80	--	ns
RESET TIMING								
t_{RSC}	Reset Cycle Time	45	--	65	--	100	--	ns
t_{RS}(1)	Reset Pulse Width	35	--	50	--	80	--	ns
t_{RSS}	Reset Set Up Time	35	--	50	--	80	--	ns
t_{RSR}	Reset Recovery Time	10	--	15	--	20	--	ns
t_{EFL}	Reset to Empty Flag Low	--	45	--	65	--	100	ns
t_{HFH}	Reset to Half Full Flag High	--	45	--	65	--	100	ns
t_{FFH}	Reset to Full Flag High	--	45	--	65	--	100	ns
RETRANSMIT TIMING								
t_{RTC}	Retransmit Cycle Time	45	--	65	--	100	--	ns
t_{RT}(1)	Retransmit Pulse Width	35	--	50	--	80	--	ns
t_{RTS}	Retransmit Set up Time	35	--	50	--	80	--	ns
t_{RTR}	Retransmit Recovery Time	10	--	15	--	20	--	ns
EXPANSION TIMING								
t_{XOL}	Read/Write to $\overline{XO}$ Low	--	35	--	50	--	80	ns
t_{XOH}	Read/Write to $\overline{XO}$ High	--	35	--	50	--	80	ns
t_{XI}	$\overline{XI}$ Pulse Width	35	--	50	--	80	--	ns
t_{XIS}	$\overline{XI}$ Set up Time	15	--	15	--	15	--	ns
t_{XIR}	$\overline{XI}$ Recovery Time	10	--	10	--	10	--	ns

NOTES:

1. Pulse widths less than minimum value are not allowed.
2. Values guaranteed by design, not currently tested.
3. Only applies to read data flow-through mode.

AC TEST CONDITIONS

Input Pulse Levels	0V~ 3.0V
Input Rise and Fall Times	5 ns
Timing Reference Level	1.5V

AC TEST LOADS AND WAVEFORMS

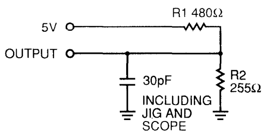


Figure 1a

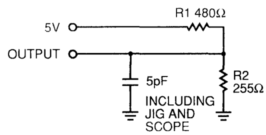
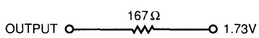


Figure 1b

Equivalent to:

THEVENIN EQUIVALENT



ALL INPUT PULSES

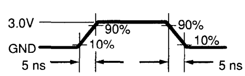


Figure 2

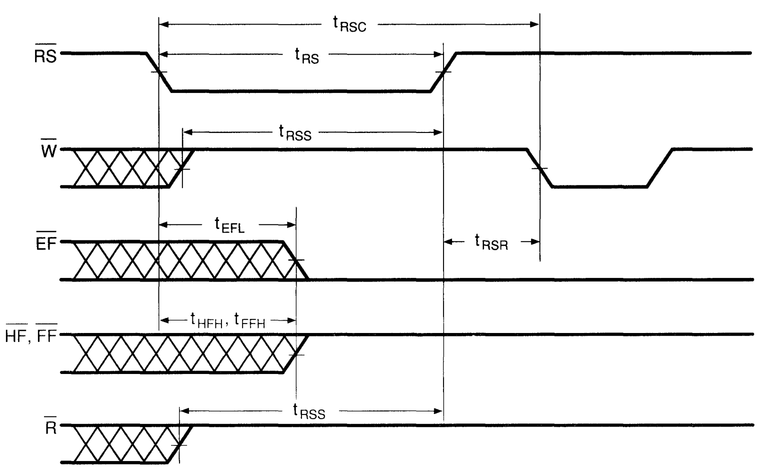
KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

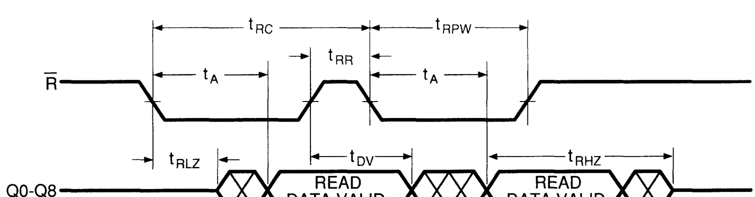
3

TIMING WAVEFORMS

RESET

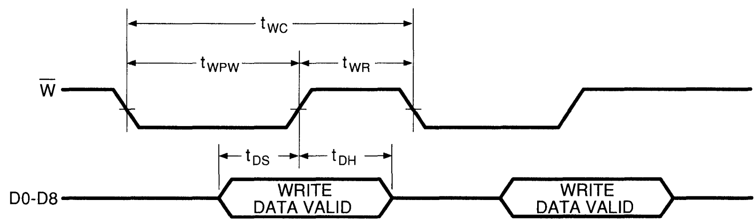


ASYNCHRONOUS READ OPERATION

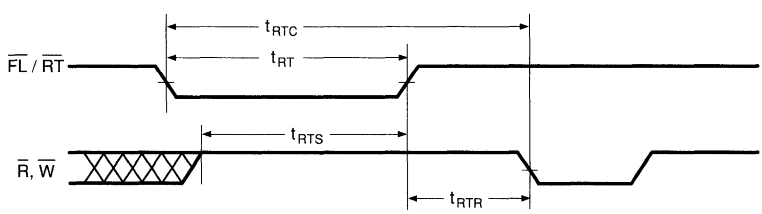


TIMING WAVEFORMS

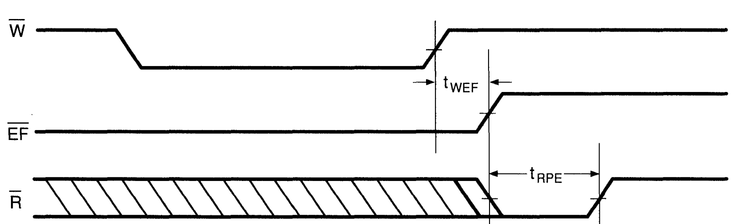
ASYNCHRONOUS WRITE OPERATION



RETRANSMIT



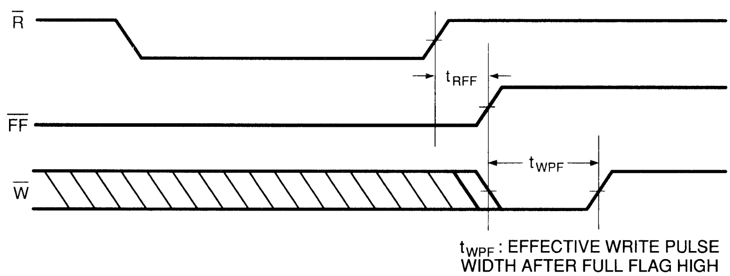
EMPTY FLAG TIMING



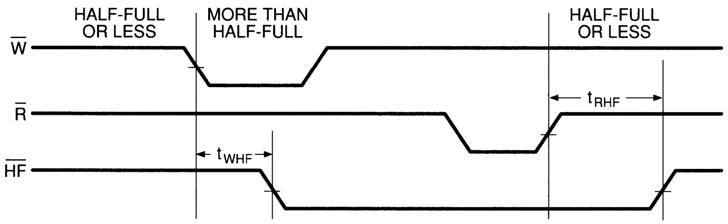
t_{RPE}: EFFECTIVE READ PULSE WIDTH AFTER EMPTY FLAG HIGH

TIMING WAVEFORMS

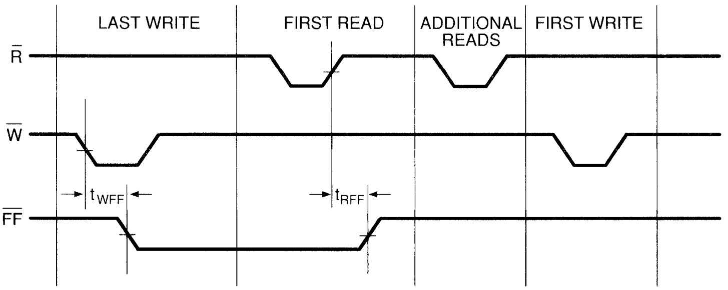
FULL FLAG TIMING



HALF-FULL FLAG TIMING

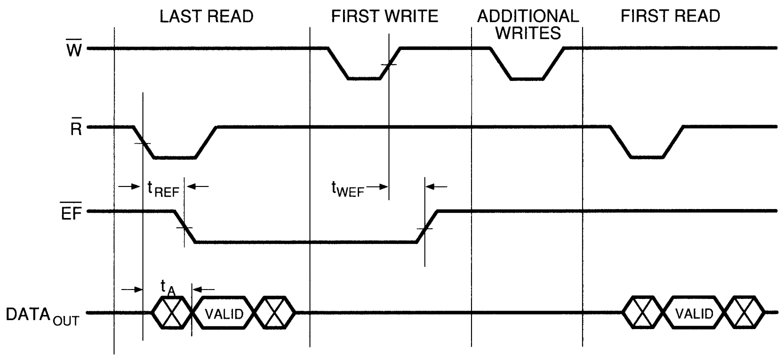


FULL FLAG FROM LAST WRITE TO FIRST READ

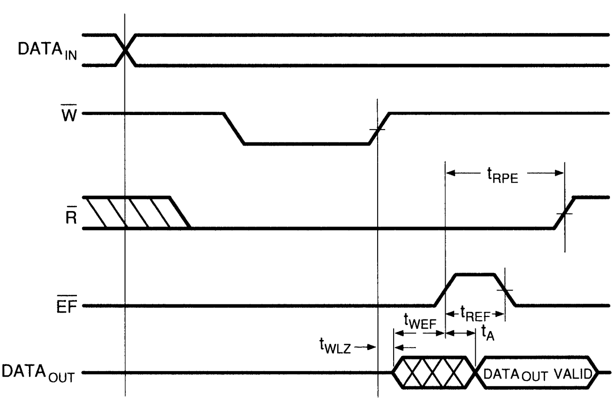


TIMING WAVEFORMS

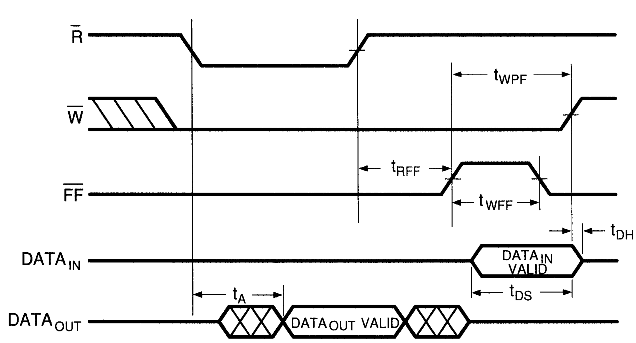
EMPTY FLAG FROM LAST READ TO FIRST WRITE



READ DATA FLOW-THROUGH MODE

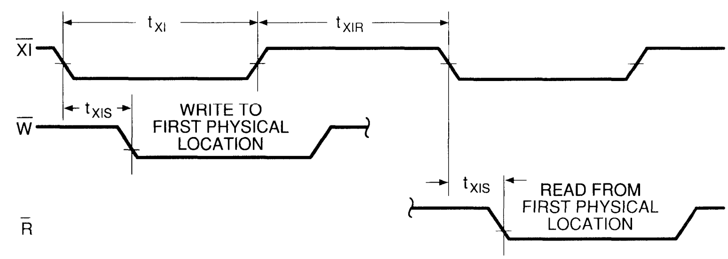


WRITE DATA FLOW-THROUGH MODE

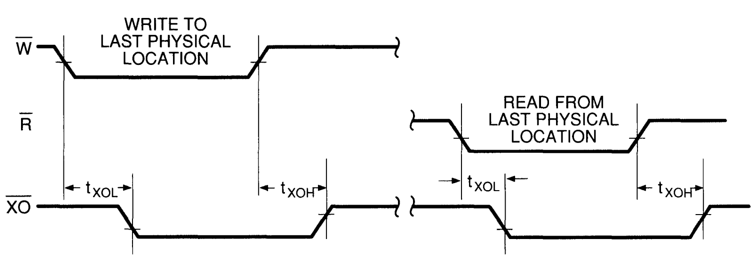


TIMING WAVEFORMS

EXPANSION IN



EXPANSION OUT



OPERATING MODES:

(Note: The7204 is used as example - these figures apply to both devices, MS7203/7204.

SINGLE DEVICE MODE

When one MS7204 is used standalone in Single Device Mode, the Expansion In ($\overline{XI}$) control input pin must be grounded. See Figure 3.

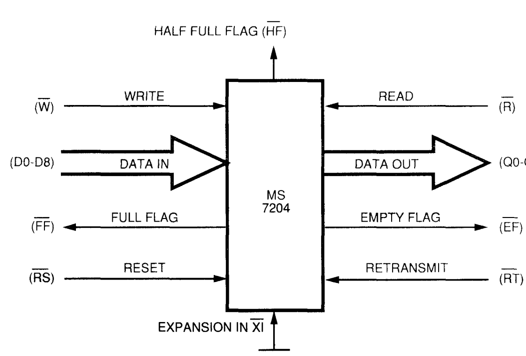


Figure 3. Single Device Mode

WIDTH EXPANSION MODE

Word width may be expanded by connecting the corresponding control input signals of multiple devices together. The EMPTY, HALF FULL and FULL FLAGS ($\overline{EE}$, $\overline{HF}$ and $\overline{FF}$) can be detected by any particular device. Figure 4 shows an 18 bit wide configuration using two devices. They may be configured to any word width in this manner.

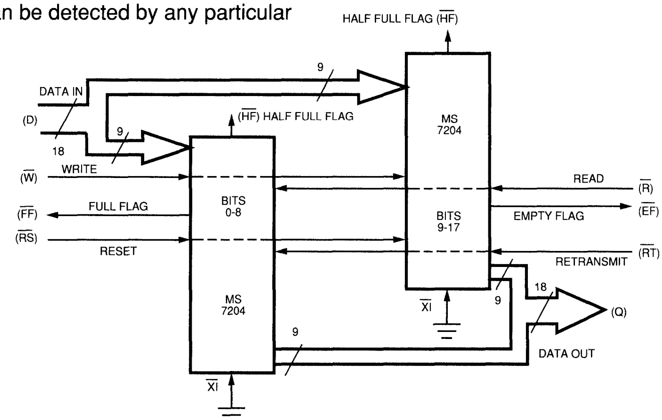


Figure 4. Width Expansion Mode

NOTES:

Flag detection is accomplished by monitoring the $\overline{EF}$, $\overline{HF}$ and $\overline{EF}$ pins on the device used in the Width Expansion Mode. Do not connect output control signals together.

DEPTH EXPANSION (DAISY CHAIN) MODE

Word depths may be expanded in multiples of 4096 words by Daisy Chaining the devices together as follows:

1. The FIRST LOAD ($\overline{FL}$) control signal of the first device must be grounded. This FIFO represents word 1-4096.
2. All other devices in the Daisy Chain must have the FIRST LOAD ($\overline{FL}$) control signal tied to V_{CC} in the inactive-high state.
3. The EXPANSION OUT ($\overline{XO}$) pin of each device must be connected to the EXPANSION IN ($\overline{XI}$) pin of the next device as shown in Figure 5.
4. External logic is required to generate a common FULL FLAG ($\overline{FF}$) and EMPTY FLAG ($\overline{EF}$) signal by ORing all of the $\overline{FF}$s together and ORing all of the $\overline{EF}$s together.
5. The RETRANSMIT ($\overline{RT}$) fuction and HALF FULL FLAG ($\overline{HF}$) are not available in Daisy Chain Mode.

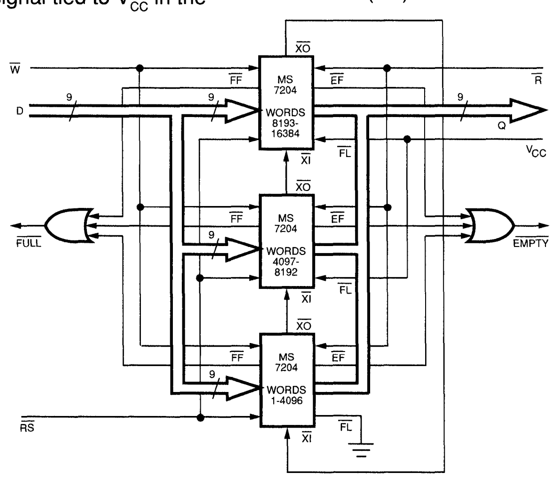


Figure 5. Diagram of a 16384 x 9 FIFO in Depth Expansion Mode

BIDIRECTIONAL MODE

Data buffering between two systems can be achieved by pairing two FIFO arrays as shown in Figure 6. This allows each system to READ and WRITE shared data. The FULL FLAG ($\overline{FF}$) must be monitored on the FIFO where WRITE ENABLE ($\overline{W}$) is used and the EMPTY FLAG ($\overline{EF}$) must be monitored on the FIFO where READ ENABLE ($\overline{R}$) is used. Both Width Expansion and Depth Expansion Modes may be used in combination with Bidirectional Mode.

COMPOUND EXPANSION MODE:

Both Width Expansion Mode and Depth Expansion (Daisy Chain) Mode can be used together to configure a large FIFO array (See Figure 4 and 5).

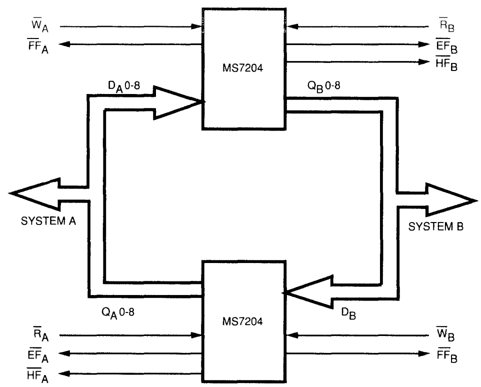


Figure 6. BiDirectional FIFO Mode

ORDERING INFORMATION

SPEED (ns)	ORDERING PART NUMBER [1]		PACKAGE REFERENCE NO.	TEMPERATURE RANGE
35	MS7203-35PC	MS7204-35PC	P28-1	0°C to +70°C
35	MS7203-35NC	MS7204-35NC	P28-2	0°C to +70°C
35	MS7203-35JC	MS7204-35JC	J32-1	0°C to +70°C
35	MS7203-35FC	MS7204-35FC	S28-2	0°C to +70°C
50	MS7203-50PC	MS7204-50PC	P28-1	0°C to +70°C
50	MS7203-50NC	MS7204-50NC	P28-2	0°C to +70°C
50	MS7203-50JC	MS7204-50JC	J32-1	0°C to +70°C
50	MS7203-50FC	MS7204-50FC	S28-2	0°C to +70°C
80	MS7203-80PC	MS7204-80PC	P28-1	0°C to +70°C
80	MS7203-80NC	MS7204-80NC	P28-2	0°C to +70°C
80	MS7203-80JC	MS7204-80JC	J32-1	0°C to +70°C
80	MS7203-80FC	MS7204-80FC	S28-2	0°C to +70°C

[1] For the low power version, add L after part number and before dash information. For example, MS7200L-25PC.

MOSEL

MS72105/ 72115

PRELIMINARY

256x16 & 512x16 Parallel-to-Serial FIFOs

FEATURES

- 25ns parallel port access time
- 50MHz serial output port shift rate
- Easily expandable in both word width and depth
- Asynchronous and simultaneous read/write operation
- Five memory status flags: Empty, Full, Half-full, Almost-empty and Almost-full
- Least Significant or Most Significant bit first read selectable for two sided printing
- Low power, power down capability
- Dual port RAM architecture with zero fall through time
- Available in 28-pin 300mil plastic DIP or 330mil SOIC gull wing

DESCRIPTION

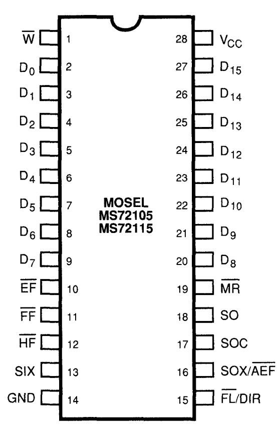
The MS72105 and MS72115 are high-speed, low power 16-bit parallel-to-serial FIFOs. These FIFOs are well suited for any serial date output buffering such as are found in laser printers, FAX machines, local area networks, video frame buffers, disk and tape controllers. They are fully asynchronous and allow simultaneous read and write operations.

Wider and deeper FIFOs can be assembled using multiple devices. MOSEL's on-chip expansion logic (SIX, SOX & $\overline{FL}$/DIR) makes this possible and requires no external components. The serial output is clocked out by signalling the serial output clock pin (SOC) and data is available on the serial out pin (SO). The Least Significant or Most Significant bit can be read first by programming the DIR pin after Reset.

The device has five flags: empty, full, half full, almost-empty and almost-full. The empty and full flags prevent data underflow or overflow. The empty, full and half-full flags are available in both single device and expansion configurations. The almost-empty and almost-full are only available in the single device configuration.

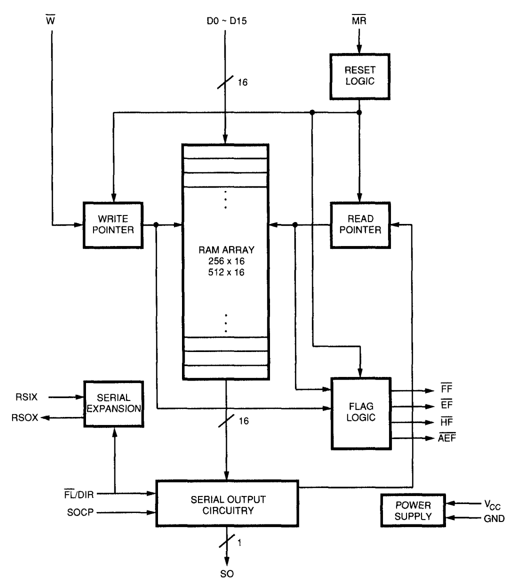
The MS72105 and MS72115 designs are based on a self addressing dual port RAM architecture. This allows for a zero fall through delay and quick flag logic response. The MS72105 and MS72115 are fabricated on MOSEL's full CMOS process.

PIN CONFIGURATIONS



DIP/SOIC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



MOSEL Corporation 914 West Maude Avenue, Sunnyvale, CA 94086 U.S.A 408-733-4556

PIN DESCRIPTIONS

D_0 - D_{15} Inputs

Data inputs for 16-bit wide data.

$\overline{MR}$ Master Reset

When $\overline{MR}$ is set low, internal READ and WRITE pointers are set to the first location of the RAM array. $\overline{FF}$ and $\overline{HF}$ go HIGH. $\overline{EF}$ and $\overline{AEF}$ go LOW. A master reset is required before an initial WRITE after power-up. $\overline{W}$ must be high during the $\overline{MR}$ cycle. Also the First Load pin ($\overline{FL}$/) is progammed only during Reset.

$\overline{W}$ Write

A write cycle is initiated on the falling edge of WRITE if the Full Flag ($\overline{FF}$) is not set. Data set-up and hold times must be adhered to with respect to the rising edge of WRITE. Data is stored in the RAM array sequentially and independently of any ongoing read operation.

SOC Serial Output Clock

A serial bit read cycle is initiated on the rising edge of SOC if the Empty Flag ($\overline{EF}$) is not set. In both Depth and Serial Word Width Expansion modes, all of the SOC pins are tied together.

$\overline{FL}$/DIR First Load/Direction

This is a dual purpose input used in the width and depth expansion configurations. The First Load ($\overline{FL}$) function is programmed only during Master Reset ($\overline{MR}$) and a LOW on $\overline{FL}$ indicates the first device to be loaded with a byte of data. All other devices should be programmed HIGH. The Direction (DIR) function is programmed during operation after MASTER Reset and tells the device whether to read out the Least Significant or Most Significant bit first.

SIX Read Serial in Expansion

In the single device configuration, SIX is set HIGH. In depth expansion or daisy chain expansion. SIX is connected to SOX (expansion out) of the previous device.

SO Serial Output

Serial data is output on the Serial Output (SO) pin. Data is clocked out LSB or MSB depending on the Direction pin programming. During Expansion the SO pins are tied together.

$\overline{FF}$ Full Flag

When $\overline{FF}$ goes low, the device is full and further WRITE operations are inhibited. When $\overline{FF}$ is high, the device is not full.

$\overline{EF}$ Empty Flag

When $\overline{EF}$ goes low, the device is empty and further READ operations are inhibited. When $\overline{EF}$ is high, the device is not empty.

3

$\overline{HF}$ Half Full Flag

When $\overline{HF}$ is LOW, the device is more than half full. When $\overline{HF}$ is HIGH, the device is empty to half full.

SOX/$\overline{AEF}$ Serial Out Expansion, Almost Empty, Almost Full Flag

This is a dual purpose output. In the single device configuration (RSIX HIGH), this is an $\overline{AEF}$ output pin. When $\overline{AEF}$ is LOW, the device is empty to 1/8 full - 1 or 7/8 full + 1 to full. When $\overline{AEF}$ is HIGH, the device is 1/8 full up to 7/8 full. In the Expansion configuration (SOX connected to SIX of the next device) a pulse is sent from SOX to SIX to coordinate the width, depth or daisy chain expansion.

V_{CC} Power Supply

Single power supply of 5V.

GND Ground

Single ground of 0V.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	RATING	COMMERCIAL	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	50	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to ABSOLUTE MAXIMUM RATINGS for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.0	-	-	V
V_{IL}[1]	Input Low Voltage	-	-	0.8	V

1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS (Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

SYMBOL	PARAMETER	MS72105 MS72115 MIN.	TYP.	MIAX.	UNITS
I_{IL}[1]	Input Leakage Current (Any Input)	–1	-	1	µA
I_{OL}[2]	Output Leakage Current	–10	-	10	µA
V_{OH}	Output Logic "1" Voltage I_{OUT} = –2mA [%]	-	-	-	V
V_{OL}	Output Logic "0" Voltage I_{OUT} = 8mA [6]	-	-	0.4	V
I_{CC1}[3]	Power Supply Current	-	90	140	mA
I_{CC2}[3]	Average Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL}$/DIR = V_{IH})	-	8	12	mA
I_{CC3} (L)[3, 4]	Power Down Current	-	-	8	mA

1. Measurements with $0.4 \leq V_{IN} \leq V_{OUT}$.
2. $\overline{MR} \leq V_{IL}$, $0.4 \leq V_{OUT} \leq V_{CC}$
3. I_{CC} measurements are made with outputs open.
4. $\overline{MR}$ = $\overline{FL}$/DIR = $\overline{W}$ = $\overline{SOC}$ = V_{CC} –0.2V; all other inputs ≥ V_{CC} –0.2V or ≤ 0.2V.
5. For SO, I_{OUT} = –4mA
6. For SO, I_{OUT} = 16mA

STATUS FLAGS

NUMBER OF WORDS IN FIFO MS72105	MS72115	$\overline{FF}$	$\overline{AEF}$	$\overline{HF}$	$\overline{EF}$
0	0	H	L	H	L
1–31	1–63	H	L	H	H
32–128	64–256	H	H	H	H
129–224	257–448	H	H	L	H
225–255	449–511	H	L	L	H
256	512	L	L	L	H

AC ELECTRICAL CHARACTERISTICS (Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

SYMBOL	PARAMETER	MS72105 MS72115 25 MIN.	MAX.	MS72105 MS72115 50 MIN.	MAX.	MS72105 MS72115 80 MIN.	MAX.	UNITS
t_S	Parallel Shift Frequency	-	22.2	-	15	-	10	MHz
t_{SOCP}	Serial Shift Frequency	-	50	-	40	-	28	MHz
t_{WC}	Write Cycle Time	35	-	65	-	100	-	ns
t_{WPW}	Write Pulse Width	25	-	50	-	80	-	ns
t_{WR}	Write Recovery Time	10	-	15	-	20	-	ns
t_{DS}	Data Set-up Time	10	-	15	-	15	-	ns
t_{DH}	Data Hold Time	0	-	5	-	5	-	ns
t_{SOCP}	Serial Clock Cycle Time	20	-	25	-	35	-	ns
t_{SOCW}	Serial Clock Width High/Low	8	-	10	-	15	-	ns
t_{SOPD}	SOC Rising Edge to SO Valid Data	-	10	-	12	-	17	ns
t_{SOHZ}	SOC Rising Edge to SO at High Z(1)	3	10	3	12	3	17	ns
t_{SOLZ}	SOC Rising Edge to SO at Low Z(1)	3	10	3	12	3	17	ns
t_{WEF}	Write High to $\overline{EF}$ High	-	20	-	25	-	35	ns
t_{WFF}	Write Low to $\overline{FF}$ Low	-	30	-	40	-	50	ns
t_{WF}	Write Low to Transitioning $\overline{HF}$, $\overline{AEF}$	-	30	-	40	-	50	ns
t_{WPF}	Write Pulse Width After $\overline{FF}$ High	25	-	50	-	80	-	ns
t_{SOCEF}	SOC Rising Edge to $\overline{EF}$ Low	-	20	-	25	-	35	ns
t_{SOCFF}	SOC Rising Edge to $\overline{FF}$ High	-	30	-	40	-	50	ns
t_{SOCF}	SOC Rising Edge to Transitioning $\overline{HF}$, $\overline{AEF}$	-	30	-	40	-	50	ns
t_{REFSO}	SOC Delay After $\overline{EF}$ High	35	-	65	-	100	-	ns
t_{RSC}	Reset Cycle Time	35	-	65	-	100	-	ns
t_{RS}	Reset Pulse Width	25	-	50	-	80	-	ns
t_{RSS}	Reset Set-up Time	25	-	50	-	80	-	ns
t_{RSR}	Reset Recovery Time	10	-	15	-	20	-	ns
t_{FLS}	$\overline{FL}$ Set-up Time to $\overline{RS}$ Rising Edge	5	-	7	-	10	-	ns
t_{FLH}	$\overline{FL}$ Hold Time to $\overline{RS}$ Rising Edge	0	-	0	-	5	-	ns
t_{DIRS}	DIR Set-up Time to SOCPRising Edge	5	-	7	-	10	-	ns
t_{DIRH}	DIR Hold Time from SOC Rising Edge	0	-	0	-	5	-	ns
t_{SOXD1}	SOC Rising Edge to SOX Rising Edge	3	11	3	15	3	20	ns
t_{SOXD2}	SOC Rising Edge to SOX Falling Edge	3	11	3	15	3	20	ns
t_{SIXS}	SIX Set-up Time to SOC Rising Edge	5	-	7	-	10	-	ns
t_{SIXH}	SIX Hold Time from SOC Rising Edge	0	-	0	-	5	-	ns

1. Guaranteed by design minimum times, not tested.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure A

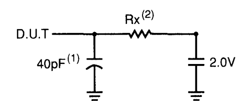


Figure A. Output Load

1. Includes jig and scope capacitances.
2. For SO, Rx = 100Ω. For all other outputs, Rx = 200Ω

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER [1]	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF

1. This parameter is sampled and not 100% tested.

FUNCTIONAL DESCRIPTION

Parallel Data Input

The device must be reset before beginning operation so that all flags are set to location zero. In width or depth expansion the First Load pin (FL/) must be programmed to indicate the first device.

The data is written into the FIFO in parallel through the D_{0-15} input data lines. A write cycle is initiated on the falling edge of the Write ($\overline{W}$) signal provided the Full Flag ($\overline{FF}$) is not asserted. If the $\overline{W}$ signal changes from HIGH-to-LOW and the Full Flag ($\overline{FF}$) is already set, the write line is inhibited internally from incrementing the write pointer and no write operation occurs.

Data set-up and hold times must be met with respect to the rising edge of Write. The data is written to the RAM at the write pointer. On the rising edge of $\overline{W}$, the write pointer is incremented. Write operations can occur simultaneously or asynchronously with read operations.

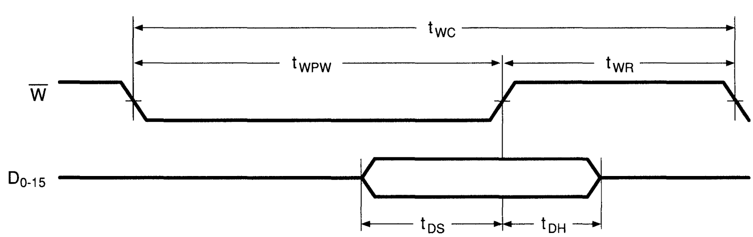


Figure 1. Write Operation

Serial Data Output

The serial data is output on the SO pin. The data is clocked out on the rising edge of SOC providing the Empty Flag ($\overline{EF}$) is not asserted. If the Empty Flag is asserted then the next data word is inhibited from moving to the output register and being clocked out by SOC.

The serial word is shifted out Least Significant Bit or Most Significant Bit first depending on the $\overline{FL}$/DIR level during operation. A LOW on DIR will cause the Least Significant Bit to be read out first. A HIGH on DIR will cause the Most Significant Bit to be read out first.

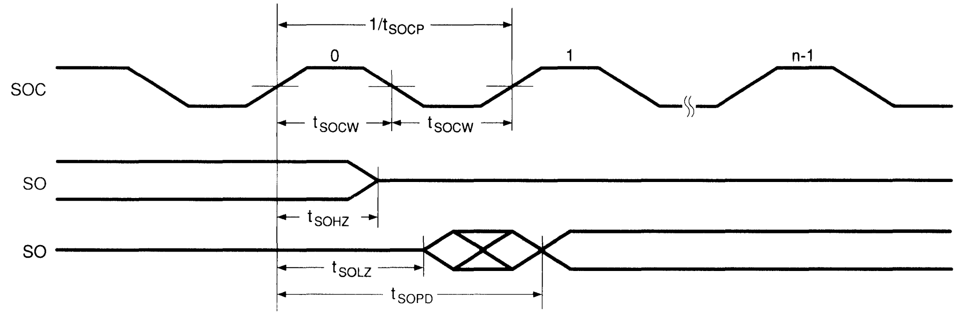


Figure 2. Read Operation

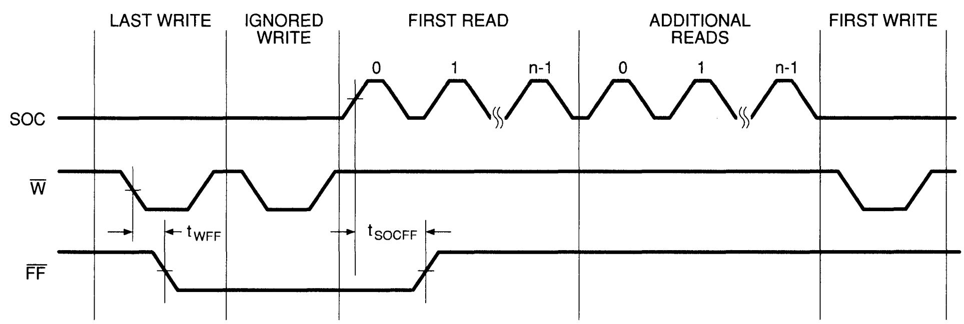


Figure 3. Full Flag from Last Write to First Read

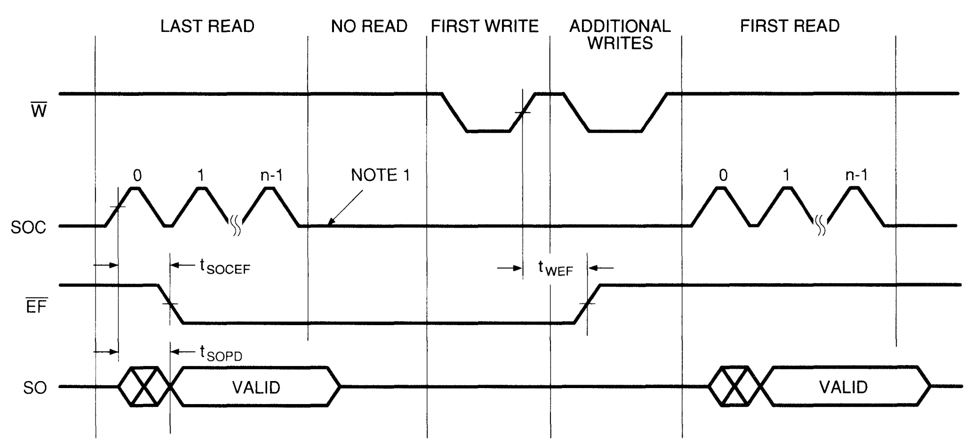


Figure 4. Empty Flag from Last Read to First Write

Note:

1. SOC should not be clocked until $\overline{EF}$ goes high.

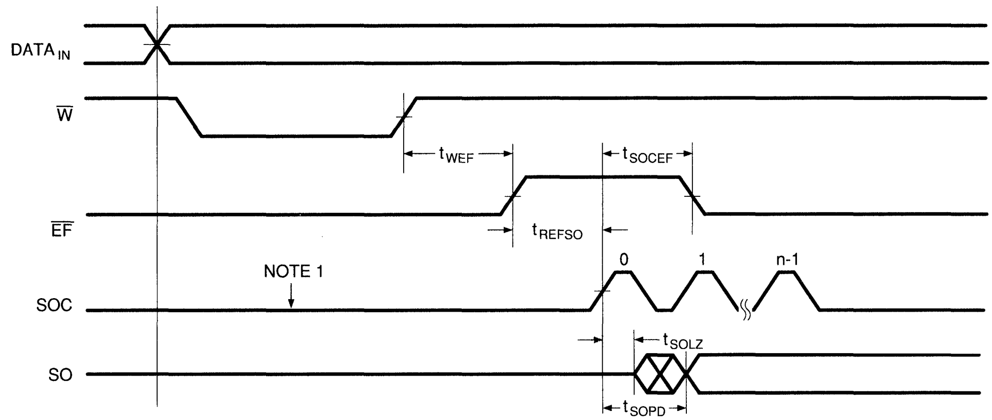


Figure 5. Empty Boundry Condition Timing

Note:
1. SOC should not be clocked until $\overline{EF}$ goes high.

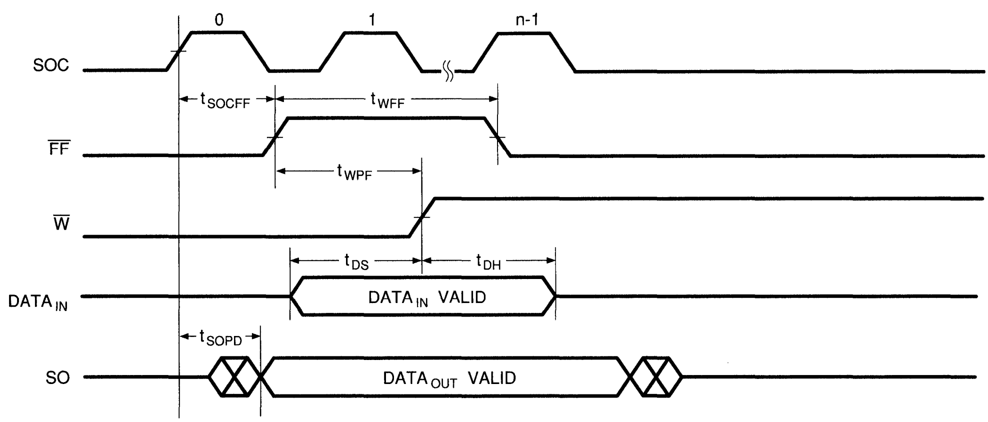


Figure 6. Full Boundary Condition Timing

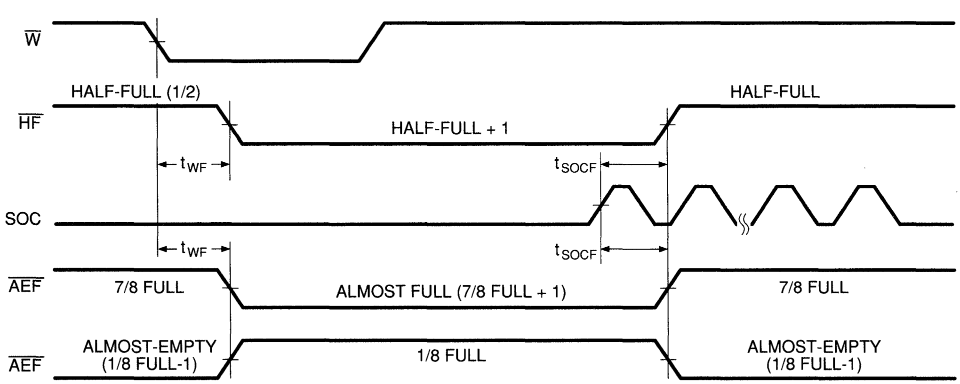


Figure 7. Half Full, Almost Full and Almost Empty Timings

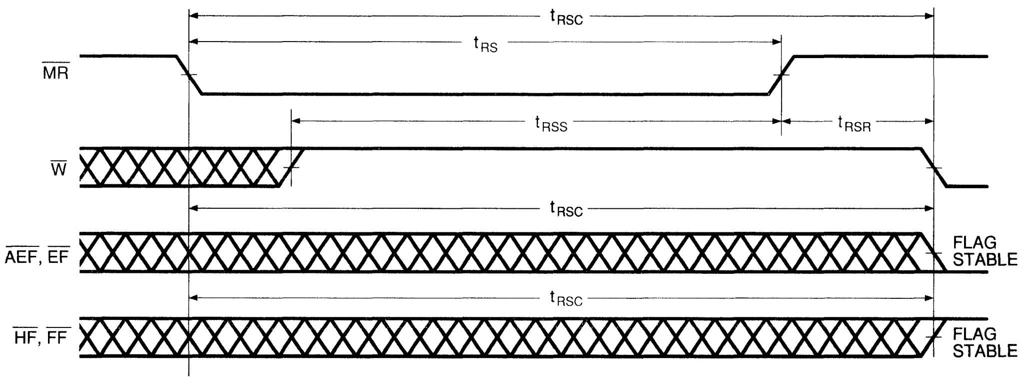


Figure 8. Master Reset

Note:
1. $\overline{EF}$, $\overline{FF}$, $\overline{HF}$ and $\overline{AEF}$ may change status during Master Reset, but flags will be valid at t_{RSC}.

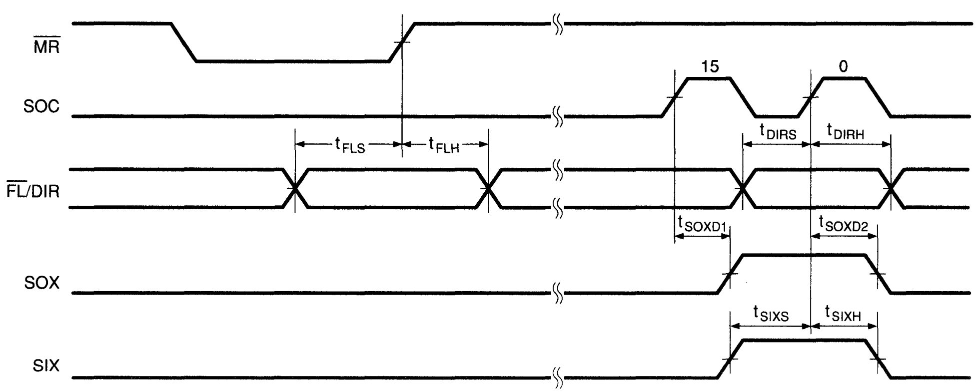


Figure 9. Serial Read Expansion

OPERATING CONFIGURATIONS

Single Device Mode

The device must be reset before beginning operation so that all flags are set to location zero. In the standalone case, the SIX line is tied HIGH and indicates single device operation to the device. The SOX/$\overline{AEF}$ pin defaults to $\overline{AEF}$ and outputs the Almost Empty and Almost Full Flag.

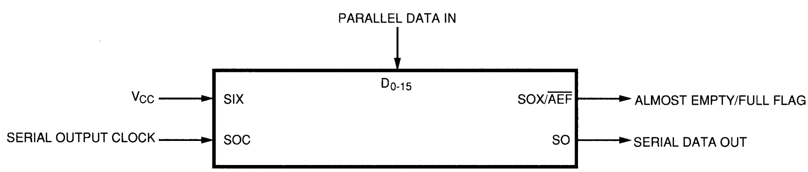


Figure 10. Single Device Configuration

TABLE 1: MASTER RESET AND FIRST LOAD TRUE TABLE– SINGLE DEVICE CONFIGURATION

MODE	INPUTS			INTERNAL STATUS		OUTPUTS		
	$\overline{MR}$	$\overline{FL}$	DIR	READ POINTER	WRITE POINTER	$\overline{AEF}$, $\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	X	Location Zero	Location Zero	0	1	1
Read/Write	1	X	0, 1	Increment [1]	Increment [1]	X	X	X

1. Pointer will increment if appropriate flag is HIGH.

Width Expansion Mode

In the cascaded case, word widths of more than 16 bits can be achieved by using more than one device. By tying the SOX and SIX pins together as shown in Figure 11 and programming which is the Least Significant Device, a cascaded serial word is achieved. The Least Significant Device is programmed by a LOW on the $\overline{FL}$/DIR pin during reset. All other devices should be programmed HIGH on the $\overline{FL}$/DIR pin at reset.

The Serial Data Output (SO) of each device in the serial word must be tied together. Since the SO pin is three stated, only the device which is currently shifting out is enabled and driving the 1-bit bus. NOTE: After reset, the level on the $\overline{FL}$/DIR pin decides if the Least Significant or Most Significant Bit is read first out of each device.

The three flag outputs, Empty ($\overline{EF}$), Half Full ($\overline{HF}$) and Full ($\overline{FF}$), should be taken from the Most Significant Device (in the example, FIFO #2). The Almost Empty and Almost Full Flag is not available due to using the SOX pin for expansion.

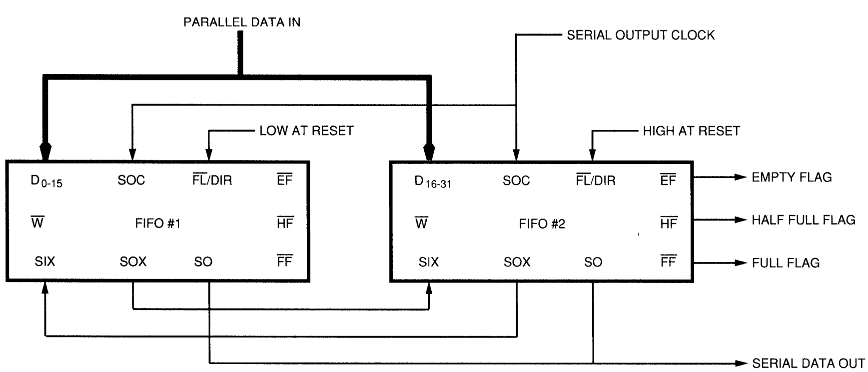


Figure 11. Width Expansion for 32-bit Parallel Data In

Depth Expansion (Daisy Chain) Mode

The MS72105/72115 can easily be adapted to applications where the requirements are for greater than 512 words. Figure 12 demonstrates Depth Expansion using three MS72115 and an Address Decoder. Any depth can be attained by adding additional devices. The Address Decoder is necessary to determine which FIFO to write data into. A byte of data should be written sequentially into each FIFO so that the SOX/SIX handshake can control reading out the data in the correct sequence. The MS72105/72115 operate in the Depth Expansion Mode when the following conditions are met:

1. The first device must be designated by programming $\overline{FL}$ LOW at Reset. All other devices to be programmed HIGH.
2. The Serial Out Expansion (SOX) of each device must be tied to the Serial In Expansion (SIX of the next device in the manner shown).
3. External logic is needed to generate composite Empty, Half Full and Full Flags. This requires the OR-ing of all $\overline{EF}$, $\overline{HF}$ and $\overline{FF}$ Flags.
4. The Almost Empty and Almost Full Flag is not available due to using the SOX pin for expansion.

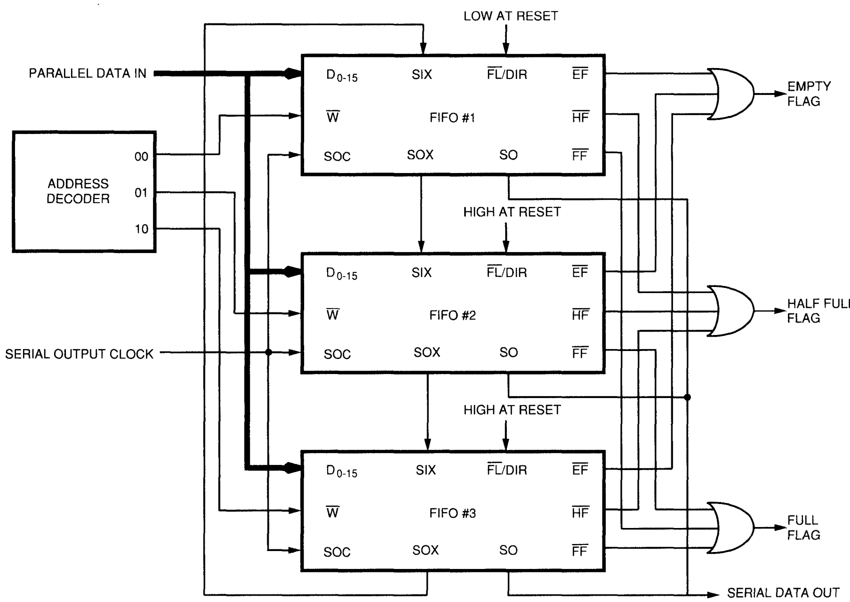


Figure 12. A 1536 x 16 Parallel-to-Serial FIFO using the MS72115

TABLE 2: MASTER RESET AND FIRST LOAD TRUE TABLE–WIDTH/DEPTH COMPOUND EXPANSION MODE

MODE	INPUTS			INTERNAL STATUS		OUTPUTS	
	$\overline{MR}$	$\overline{FL}$	$\overline{DIR}$	READ POINTER	WRITE POINTER	$\overline{EF}$	$\overline{HF}$, $\overline{FF}$
Reset-First Device	0	0	X	Location Zero	Location Zero	0	1
Reset all Other Devices	0	1	X	Location Zero	Location Zero	0	1
Read/Write	1	X	0, 1	X	X	X	X

1. $\overline{MR}$ = Master Reset , $\overline{FL}$/DIR = First Load/Direction, $\overline{EF}$ = Empty Flag Output, $\overline{HF}$ = Half Full Flag Output, $\overline{FF}$ = Full Flag Output

Compound Expansion (Daisy Chain) Mode

The MS72105/72115 can be expanded in both depth and width as Figure 13 indicates:

1. The SOX-to-SIX expansion signals are wrapped around sequentially.
2. The write ($\overline{W}$) signal is expanded in width.
3. Flag signals are only taken from the Most Significant Devices.
4. The Least Significant device in the array must be programmed with a LOW on $\overline{FL}$/DIR during reset.

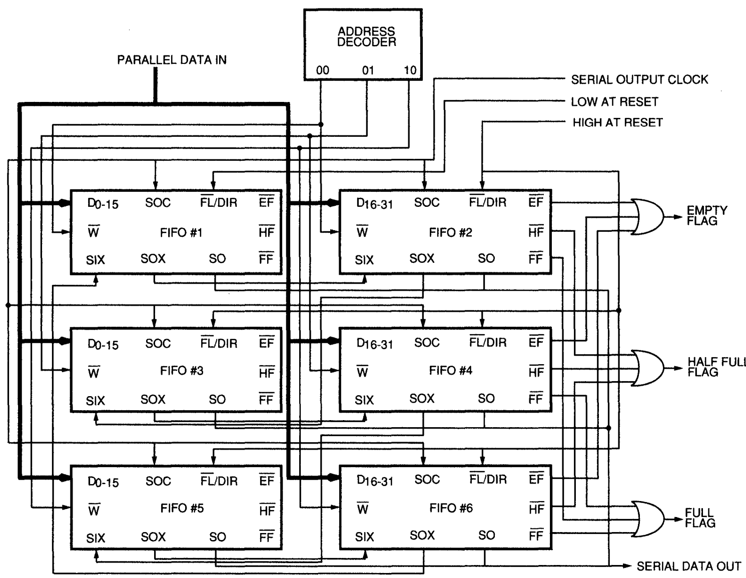


Figure 13. A 1536 x 32 Parallel-to-Serial FIFO using the MS72115

ORDERING INFORMATION

SPEED (ns)	ORDERING PART NUMBER	PACKAGE REFERENCE NO.	TEMPERATURE RANGE
25	MS72105-25NC	P28-2	0°C to + 70°C
25	MS72115-25NC		0°C to + 70°C
25	MS72105-25FC	S28-2	0°C to + 70°C
25	MS72115-25FC		0°C to + 70°C
50	MS72105-50NC	P28-2	0°C to + 70°C
50	MS72115-50NC		0°C to + 70°C
50	MS72105-50FC	S28-2	0°C to + 70°C
50	MS72115-50FC		0°C to + 70°C
80	MS72105-80NC	P28-2	0°C to + 70°C
80	MS72115-80NC		0°C to + 70°C
80	MS72105-80FC	S28-2	0°C to + 70°C
80	MS72115-80FC		0°C to + 70°C

MS72215/16 & MS72225/26

ADVANCE INFORMATION

512 x 18 & 1024 x 18 Parallel Synchronous FIFOs

FEATURES

- Full CMOS clocked synchronous FIFOs
- Read and write clocks can be synchronous or asynchronous
- Master / Slave devices make depth and width expansion easy
- Two densities: 512 x 18 and 1024 x 18
- 20ns read / write cycle time
- Dual port memory architecture
- Five Flags for memory status:
  - Empty and Full Flags
  - Two Programmable Flags
  - Half Full Flag available in single device configuration
- Master device supplies all flag outputs in depth expansion
- Output Enable puts output in high impedance
- Available in 68-lead pin grid array (PGA), and plastic leaded chip carrier (PLCC)

DESCRIPTION

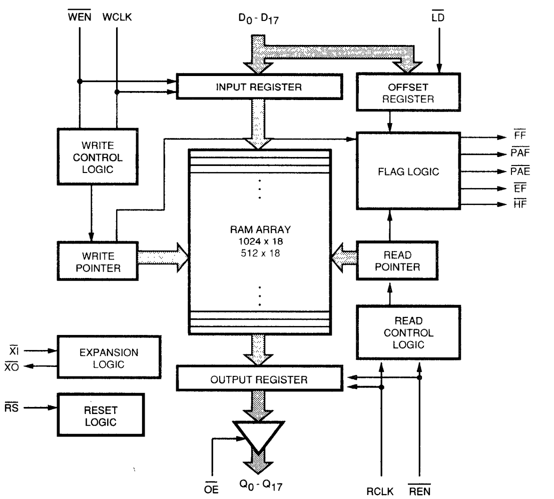
The MS72215/16 and MS72225/26 are clocked registered FIFOs that are particularly useful in synchronous design applications. This architecture allows for a user friendly part with a very high speed cycle time of 50MHz. The MS72215 and MS72225 are the master versions and the MS72216 and MS72226 are the slave versions. Typical applications for these designs are data buffering for workstation graphics, interprocessor communications, and high speed LANs.

All four devices have 18-bit wide parallel data inputs and outputs. The input port is controlled by a free running clock (WCLK), and a write enable pin (WEN). Data is written into the FIFO only when both the lock pin and write enable are active. The output port is controlled by separate clock (RCLK) and a read enable (REN) pins. The read clock can be tied to the write clock for single clock operation or the two clocks can run independently. The devices also have an output enable (OE) for three-state control of the output.

These FIFOs have a total of five flags. That is two fixed flags, Empty (EF) and Full (FF), two programmable flags, (PAE) and (PAF), plus a Half Full (HF) flag available in single device operation. The programmable flags are programmed by asserting the Load (LD) pin and clocking in the next two words on the inputs.

The MS72215 and MS72225 are both width and depth expandable. The pins XI and XO are required to expand the FIFOs in depth. To permit programmable flags in depth expansion, a master device (MS72215/25) controls the flags, and the flags are ignored on all the other slave devices (MS72216/26).

FUNCTIONAL BLOCK DIAGRAM



MOSEL Corporation 914 West Maude Avenue, Sunnyvale, CA 94086 U.S.A 408-733-4556

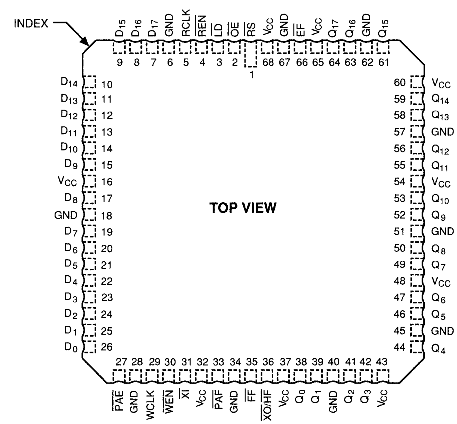
PIN CONFIGURATIONS

PGA TOP VIEW

	A	B	C	D	E	F	G	H	I	J	K
11		V_{CC}	Q_3	GND	Q_0	$\overline{XO/HF}$	GND	V_{CC}	$\overline{WEN}$	GND	
10	GND	Q_4	Q_2	Q_1	V_{CC}	$\overline{FF}$	$\overline{PAF}$	$\overline{XI}$	WCLK	$\overline{PAE}$	D_0
09	Q_6	Q_5								D_2	D_1
08	Q_7	V_{CC}								D_4	D_3
07	GND	Q_8								D_6	D_5
06	Q_{10}	Q_9								GND	D_7
05	Q_{11}	V_{CC}								V_{CC}	D_8
04	GND	Q_{12}								D_{10}	D_9
03	Q_{14}	Q_{13}								D_{12}	D_{11}
02	V_{CC}	Q_{15}	Q_{16}	V_{CC}	GND	$\overline{RS}$	$\overline{LD}$	RCLK	D_{17}	D_{14}	D_{13}
01		GND	Q_{17}	$\overline{EF}$	V_{CC}	$\overline{OE}$	$\overline{REN}$	GND	D_{16}	D_{15}	

PIN 1 Designator

PLCC TOP VIEW



PIN DESCRIPTIONS

D_0-D_{17} Data Inputs
Data inputs for 18-bit wide data.

$\overline{RS}$ Reset
When $\overline{RS}$ is set low, internal read and write pointers are set to the first location of the RAM array, $\overline{FF}$ and $\overline{PAF}$ go high , and $\overline{PAE}$ and $\overline{EF}$ go low. A reset is required before an initial WRITE after power-up.

WCLK Write Clock
When $\overline{WEN}$ is enabled (low), a write cycle is initiated on the low-to-high transition of every WCLK clock, if the FIFO is not full.

$\overline{WEN}$ Write Enable
When $\overline{WEN}$ is low, data can be loaded into the FIFO on the low-to-high transition of every WCLK clock. When $\overline{WEN}$ is high, the FIFO holds the previous data. When the FIFO is full ($\overline{FF}$ = low), the internal WRITE operation is blocked.

RCLK Read Clock
When $\overline{REN}$ is enabled (low) , data can be read on the outputs on the low-to-high transition of the read clock RCLK if the FIFO is not empty.

$\overline{REN}$ Read Enable
When $\overline{REN}$ is (low), data can be read from the FIFO on the low-to-high transition of every RCLK clock. When $\overline{REN}$ is high, the output register holds the previous data. When the FIFO is empty ($\overline{EF}$ = low), the internal READ operation is blocked.

$\overline{OE}$ Output Enable
When $\overline{OE}$ is enabled (low), the parallel output buffers receive data from the output register. When $\overline{OE}$ is disabled (high), the Q output bus is in a high impedance state.

$\overline{LD}$ Load
When $\overline{LD}$ is low, data on the inputs D_0-D_{17} is written to the offset and depth registers on the low-to-high transition of the WCLK.

$\overline{XI}$ Expansion Input
In the single device or width expansion configuration, $\overline{XI}$ is grounded. In the depth expansion configuration, $\overline{XI}$ is connected to $\overline{XO}$ (expansion out) of the previous device.

$\overline{FF}$ Full Flag
When $\overline{FF}$ goes low, the device is full and further WRITE operations are inhibited. When $\overline{FF}$ is high, the device is not full. $\overline{FF}$ is synchronized with WCLK.

$\overline{EF}$ Empty Flag
When $\overline{EF}$ goes low, the device is empty and further READ operations are inhibited. When $\overline{EF}$ is high, the device is not empty. $\overline{EF}$ is synchronized with RCLK.

$\overline{PAF}$ Programmable Almost-Full Flag
When $\overline{PAF}$ is low, the device is almost full based on the programmable full offset. If there is no offset specified, the device is 7/8 full or more.

$\overline{PAE}$ Programmable Almost-Empty Flag
When $\overline{PAE}$ is low, the device is almost empty based on the programmable empty offset. If there is no offset specified, the device is empty to 1/8 full.

$\overline{XO/HF}$ Expansion Out/Half-Full Flag
In the single device or width expansion configuration, the device is more than half full when $\overline{HF}$ is low. In the depth expansion configuration, a pulse is sent from $\overline{XO}$ to $\overline{XI}$ when the last location in the FIFO is filled.

Q_0-Q_{17} Outputs
Data outputs for 18-bit wide data.

V_{CC} Power Supply
Nine +5V power supply pins.

GND Ground
Ten ground pins

General Information 1

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Cache Products 6

Application Notes 7

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MOSEL Sales Network 9

CMOS STATIC ROMS

MOSEL has developed a broad line of CMOS ROMs (read only memory) from 128K to 8 megabits, including products at 128K, 256K, 512K, 1024K, 2048K, 4096K and 8192K in density. All standard packages are available including 28, 32 and 40 pin plastic dips and 28 or 32 pin SOG packages. MOSEL offers fast turnaround of four to six weeks for engineering samples and/or first production units.

PRODUCTION PRODUCTS

At the 1 megabit density, MOSEL offers the 1 megabit 128K x 8 MS311024 and MS311002, with speeds of 100, 120, 150 and 200ns, available today in the 600 mil 28 and 32 pin DIP packages and 28 and 32 pin SOG packages. The CMOS MS311024 provides significant power savings as compared with the NMOS products, with typical standby power below 10µA.

MOSEL also offers products at 512K, the 64K x 8 MS310512, at 256K, the 32K x 8 MS310256, and 128K, the 16K x 8 MS310128. These products are available in 150ns, and provide similar standby power savings as the megabit product as compared with NMOS designs. Both 28 pin dip and surface mount packages are supported.

DEVELOPMENT PRODUCTS

MOSEL is now supplying or has under development 2, 4, and 8 Megabit ROM products at speeds of 120 to 200ns including:

The 256K x 8 MS312001 at 120-150ns in a 32 pin DIP.

The 256K x 8 MS312002 at 200ns in a 32 pin DIP.

The 256K x 16 / 512K x 8 MS314003 at 200ns in a 40 pin DIP and 64 pin PQFP.

The 512K x 8 MS314001 at 100-150ns in a 32 pin DIP.

The 512K x 8 MS314002 at 200ns in a 32 pin DIP.

The 1024K x 8 MS318002 at 200ns in a 32 pin DIP.

The 512K x 16 / 1024K x 8 MS318003 at 200ns in a 40 pin DIP and 64 pin PQFP.

SUMMARY

MOSEL offers a broad family of high speed low power CMOS ROM products.

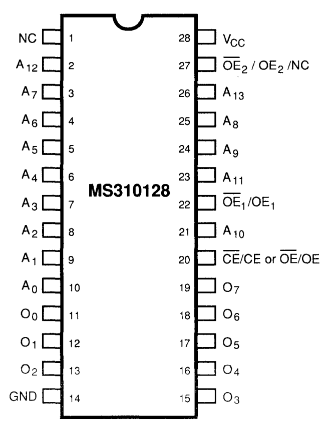
If you are interested in more information about MOSEL's ROM products, such as information about our quick turn service, special speed or power screening or other special handling, please contact your local sales representatives or franchise distributors listed in this book.

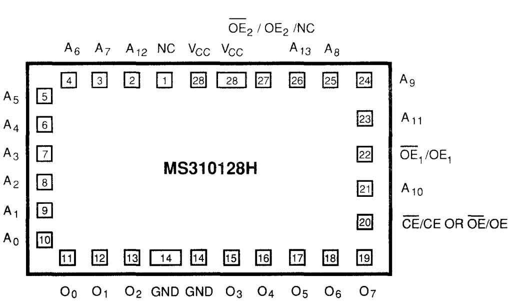
16,384x8 CMOS Mask Programmable ROM

FEATURES

- Access time: 150ns max
- Low Power operation:
  - Operating: 30mA max.
  - Standby: 30µA max.
- Fully static operation
- Automatic power down
- TTL compatible inputs outputs
- 3-state outputs for wired-OR expansion
- EPROMs accepted as program data input
- Ultra low data retention supply
- Pin 20/22/27 controls (sense and type)

PIN CONFIGURATIONS



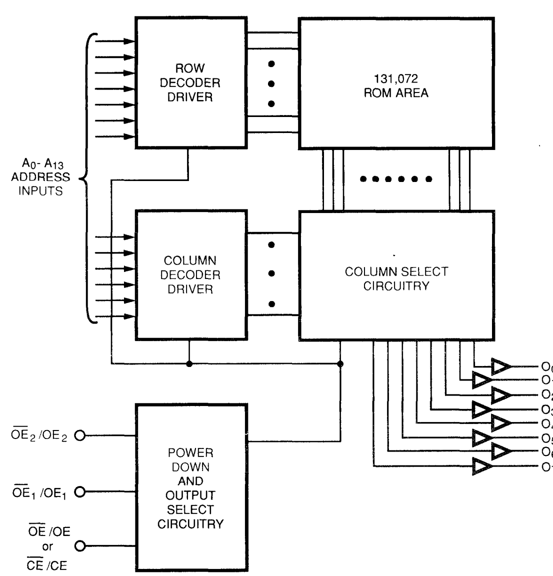


DESCRIPTION

The MS310128 is a high performance Read Only Memory organized as 16,384 words by eight bits with an access time of 150 ns. It is designed to be compatible with all microprocessors and similar applications where high performance mass storage and simple interfacing are important design considerations.

The MS310128 offers automatic powerdown with powerdown controlled by the Chip Enable ($\overline{CE}$/CE) inputs. When $\overline{CE}$/CE goes HIGH/LOW the device will automatically power down and remain in a low power standby mode as long as $\overline{CE}$/CE remains HIGH/LOW. This unique feature provides system level power savings of as much as 99%. The function of Pin 22 and Pin 27 are $\overline{OE_1}$/OE_1 and $\overline{OE_2}$/OE_2/NC, respectively. Pin 20 may also be programmed as $\overline{OE}$/OE (active HIGH or LOW) in order to eliminate bus contention in multiple bus microprocessor systems. Pins 22 and 27 can be programmed to allow decoding of four 16k x 8 parts for 1/2 megabit ROM emulation.

BLOCK DIAGRAM



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PIN DESCRIPTIONS

PIN NO.	SYMBOL	FUNCTION
2-10, 21, 23-26	A_0 - A_{13}	Address Input
11-13, 15-19	O_0 - O_7	Data Output
14	GND	Ground
28	V_{CC}	Power Supply
20	$\overline{CE}$/CE or $\overline{OE}$/OE	Chip Enable Input or Output Enable
22	$\overline{OE}_1$/OE_1	Additional Output Enable Pin
27	$\overline{OE}_2$/OE_2	Additional Output Enable Pin

ABSOLUTE MAXIMUM RATINGS[1]

Ambient Operating Temperature	–10°C to +80°C
Storage Temperature	–65°C to +150°C
Supply Voltage to Ground Potential	–0.5V to +7.0V
Applied Output Voltage	–0.5V to +7.0V
Applied Input Voltage	–0.5V to +7.0V
Power Dissipation	300 mW
Soldering Temperature and Time	260°C , 10 sec

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not recommended. Exposure to ABSOLUTE MAXIMUM RATINGS for extended periods may affect device reliability.

OPERATING RANGE

RANGE	AMBIENT TEMPERATURE	Vcc
Commercial	0°C to + 70°C	5V ± 10%

DC ELECTRICAL CHARACTERISTICS (over the commercial operating range)

PARAMETER NAME	PARAMETER	TEST CONDITIONS	MS310128 MIN.	TYP.	MAX.	UNITS
V_{IL}	Input Low Voltage		–0.5	—	0.8	V
V_{IH}	Input High Voltage		2.2		V_{CC}+ 0.3	V
I_{IL}	Input Leakage Current	V_{CC} = Max, V_{IN} = 0V to V_{CC}	—	—	10	μA
I_{OL}	Output Leakage Current	V_{OUT} = 0 V to V_{CC}	—	—	10	μA
V_{OL}	Output Low Voltage	V_{CC} = Min, I_{OL} = 3.2mA	—	—	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min, I_{OH} = –1mA	2.4	—	V_{CC}	V
I_{CC}	Operating Power Supply Current [1]		—	10	30	mA
I_{CCSB}	Standby Power Supply Current	$\overline{CE}$ = V_{IH}, CE = V_{IL}	—	10	30	mA
I_{OS}	Output Short Circuit Current [2]		—	—	70	mA

1. Measured with device selected and outputs unloaded.
2. For a duration not to exceed 30 seconds.

CAPACITANCE (Ta=25°C, f=1.0MHz)[1]

SYMBOL	PARAMETER	CONDITION	MAX.	UNIT
C_I	Input Capacitance	T_A = 25°C	10	pF
C_O	Output Capacitance	F = 1.0MHz	10	pF

1. This parameter is guaranteed but not 100% tested.

TRUTH TABLE

PIN 20 CE	PIN 22 OE_1	PIN 27 OE_2	OUTPUTS O_0 - O_7	MODE
I	X	X	High Z	Power Down
A	I	X	High Z	Output Disable
A	X	I	High Z	Output Disable
A	A	A	Output Data	Read

AC TEST CONDITIONS

Input Pulse Levels	0.4 ~ 2.4V
Input Rise and Fall Times	10 ns
Timing Measurement Level	V_{IL} = 0.8V V_{IH} = 2.2V
Reference	V_{OL} = 0.8V V_{OH} = 2.0V
Output Load	See Figure 1

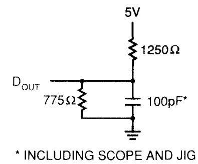


Figure 1 Output Load Circuit

AC ELECTRICAL CHARACTERISTICS (over the operating range)

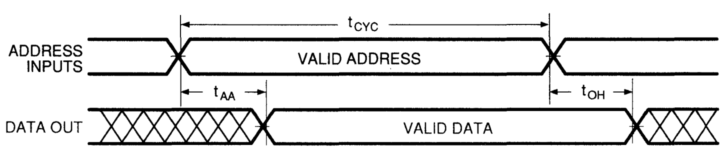
PARAMETER NAME	PARAMETER	MS310128 MIN.	MAX.	UNIT
t_{CYC}	Cycle Time	120	—	ns
t_{AA}	Address Access Time	—	150	ns
t_{ACE}	Chip Enable Access Time	—	150	ns
t_{ACS}	Chip Select Access Time	—	70	ns
t_{LZ}	Output LOW Z Delay (1)	10	—	ns
t_{HZ}	Output HIGH Z Delay (2)	0	70	
t_{OH}	Output Hold from Address Change	10	—	ns
t_{PU}	Power-Up Time	0	—	ns
t_{PD}	Powerdown Time	—	85	ns

1. Output LOW impedance delay (t_{LZ}) is measured from $\overline{CE}$/CE or $\overline{OE}$/OE going active.
2. Output HIGH impedance delay (t_{HZ}) is measured from the earlier of $\overline{CE}$/CE or $\overline{OE}$/OE going active.

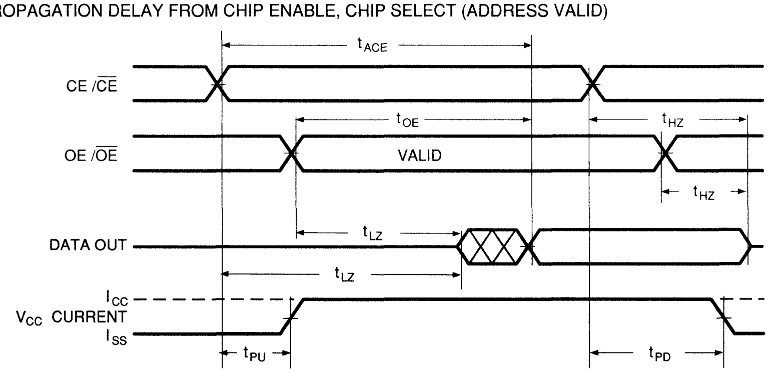
4

TIMING DIAGRAMS

PROPAGATION DELAY FROM ADDRESS (CE/$\overline{CE}$ = ACTIVE, OE/$\overline{OE}$ = ACTIVE)



PROPAGATION DELAY FROM CHIP ENABLE, CHIP SELECT (ADDRESS VALID)



ORDERING INFORMATION

SPEED (ns)	ORDERING PART NUMBER	PACKAGE REFERENCE NO.	TEMPERATURE RANGE
150	MS310128-15PC	P28-3	0°C to + 70°C
150	MS310128-15XC	Chip	0°C to + 70°C

32,768x8 CMOS Mask Programmable ROM

FEATURES

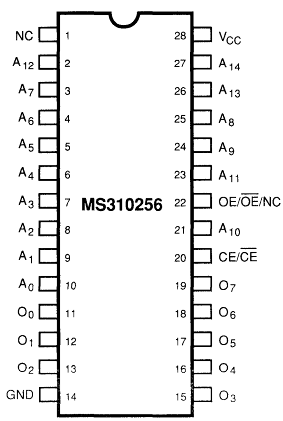
- Access time: 150ns max
- Low Power operation:
  - Operating: 30mA max.
  - Standby: 30μA max.
- Fully static operation
- Automatic power down
- TTL compatible inputs and outputs
- 3-state outputs for wired-OR expansion
- EPROMs accepted as program data input
- Ultra low data retention supply

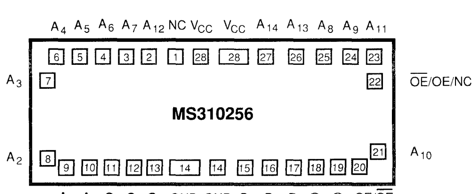
DESCRIPTION

The MS310256 is a high performance Read Only Memory organized as 32,768 words by 8 bits. It is designed to be compatible with all microprocessors and similar applications where high performance mass storage and simple interfacing are important design considerations.

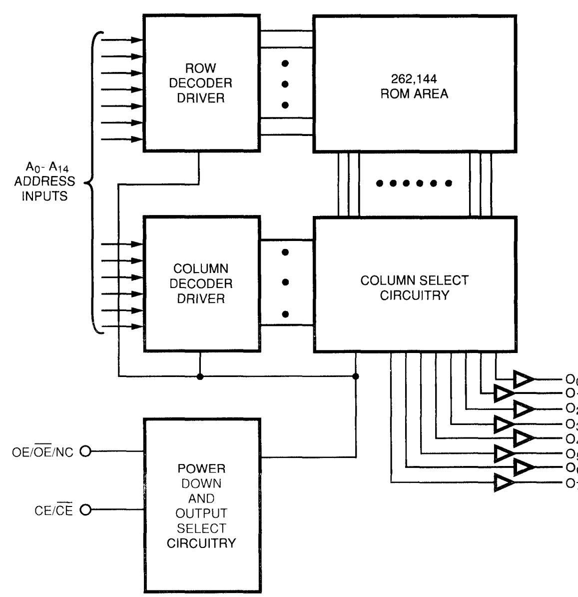
The MS310256 offers automatic powerdown with powerdown controlled by the Chip Enable ($\overline{CE}$/CE) input. When $\overline{CE}$/CE goes HIGH/LOW the device will automatically power down and remain in a low power standby mode as long as $\overline{CE}$/CE remains HIGH/LOW. Pin 22 may be mask programmed as $\overline{OE}$/OE/NC (active HIGH, active LOW or no connection). In order to eliminate bus contention in multiple bus microprocessor systems.

PIN CONFIGURATIONS





BLOCK DIAGRAM



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PIN DESCRIPTIONS

PIN NO.	SYMBOL	FUNCTION
2-10, 21, 23-27	A_0 - A_{14}	Address Input
11-13, 15-19	O_0 - O_7	Data Output
14	GND	Ground
28	V_{CC}	Power Supply
20	$\overline{CE}$/CE	Chip Enable Input
22	$\overline{OE}$/OE/NC	Output Enable Input /No Connection
1	NC	No Connection

OPERATING RANGE

RANGE	AMBIENT TEMPERATURE	Vcc
Commercial	0°C to + 70°C	5V ± 10%

ABSOLUTE MAXIMUM RATINGS(1)

Ambient Operating Temperature	–10°C to +80°C
Storage Temperature	–65°C to +150°C
Supply Voltage to Ground Potential	–0.5V to +7.0V
Output Voltage	–0.5V to V_{CC} + 0.5V
Input Voltage	–0.5V to V_{CC} + 0.5V
Power Dissipation	400 mW
Soldering Temperature and Time	260°C , 10 sec

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not recommended. Exposure to ABSOLUTE MAXIMUM RATINGS for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS (over the commercial operating range)

PARAMETER NAME	PARAMETER	TEST CONDITIONS	MS311024 MIN.	TYP.	MAX.	UNITS
V_{IL}	Input Low Voltage		–0.5	—	0.8	V
V_{IH}	Input High Voltage		2.2		V_{CC}+ 0.3	V
$\lvert I_{IL}\rvert$	Input Leakage Current	V_{CC} = Max, V_{IN} = 0V to V_{CC}	—	—	10	µA
$\lvert I_{OL}\rvert$	Output Leakage Current	V_{OUT} = 0 V to V_{CC}	—	—	10	µA
V_{OL}	Output Low Voltage	V_{CC} = Min, I_{OL} = 3.2mA	—	—	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min, I_{OH} = –1mA	2.4	—	V_{CC}	V
I_{CC}	Operating Power Supply Current (1)		—	15	30	mA
I_{CCSB}	Standby Power Supply Current	$\overline{CE}$ = V_{IH}, CE = V_{IL}	—	0.2	1.5	mA
I_{CCSB1}	Super Standby Power Supply Current	$\overline{CE}$ = V_{CC} - 0.2V, CE = 0.2V	—	10	30	µA
I_{OS}	Output Short Circuit Current (2)		—	—	70	mA

1. Measured with device selected and outputs unloaded.
2. For a duration not to exceed 30 seconds.

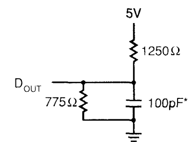
CAPACITANCE (Ta=25°C, f=1.0MHz)(1)

SYMBOL	PARAMETER	CONDITION	MAX.	UNIT
C_I	Input Capacitance	T_A = 25°C	10	pF
C_O	Output Capacitance	F = 1.0MHz	10	pF

1. This parameter is guaranteed but not 100% tested.

AC TEST CONDITIONS

Input Pulse Levels	0.4 ~ 2.4V
Input Rise and Fall Times	10 ns
Timing Measurement Level	V_{IL} = 0.8V V_{IH} = 2.2V
Reference	V_{OL} = 0.8V V_{OH} = 2.0V
Output Load	See Figure 1



* INCLUDING SCOPE AND JIG

Figure 1 Output Load Circuit

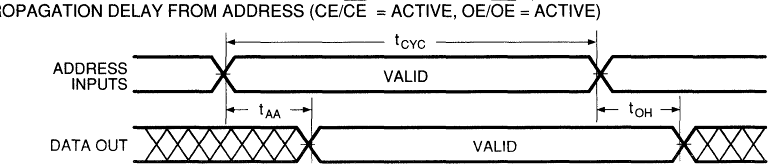
AC ELECTRICAL CHARACTERISTICS (over the operating range)

PARAMETER NAME	PARAMETER	MS310256-15 MIN.	MAX.	UNIT
t_{CYC}	Cycle Time	150	—	ns
t_{AA}	Address Access Time	—	150	ns
t_{ACE}	Chip Enable Access Time	—	150	ns
t_{ACS}	Output Enable Access Time	—	85	ns
t_{LZ}	Output LOW Z Delay$^{(1)}$	10	—	ns
t_{HZ}	Output HIGH Z Delay$^{(2)}$	0	85	
t_{OH}	Output Hold After Address Change	10	—	ns
t_{PU}	Power-Up Time	0	—	ns
t_{PD}	Powerdown Time	—	85	ns

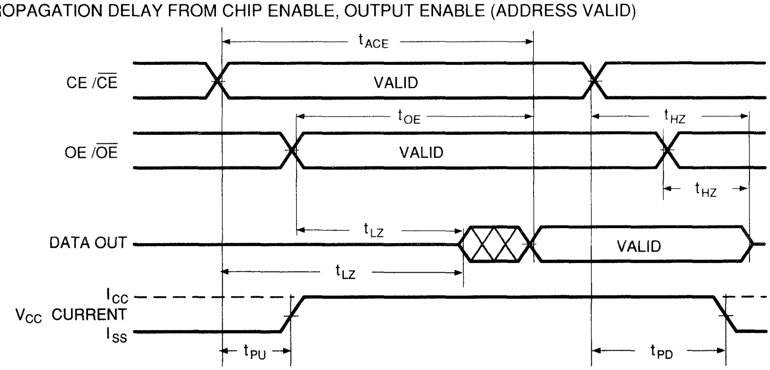
1. Output LOW impedance delay (t_{LZ}) is measured from CE/$\overline{CE}$ or OE/$\overline{OE}$ going active.
2. Output HIGH impedance delay (t_{HZ}) is measured from the earlier of CE/$\overline{CE}$ or OE/$\overline{OE}$ going inactive.

TIMING DIAGRAMS

PROPAGATION DELAY FROM ADDRESS (CE/$\overline{CE}$ = ACTIVE, OE/$\overline{OE}$ = ACTIVE)



PROPAGATION DELAY FROM CHIP ENABLE, OUTPUT ENABLE (ADDRESS VALID)



ORDERING INFORMATION

SPEED (ns)	ORDERING PART NUMBER	PACKAGE REFERENCE NO.	TEMPERATURE RANGE
150	MS310256-15PC	P28-3	0°C to + 70°C
150	MS310256-15XC	Chip	0°C to + 70°C

65,536x8 CMOS Mask Programmable ROM

FEATURES

- Access time: 150ns max
- Low Power operation:
  - Operating: 30mA max.
  - Standby: 30µA max.
- Masked Programmed for chip enable (power-down) CE/$\overline{\text{CE}}$ and output enable OE/$\overline{\text{OE}}$/NC
- Fully static operation
- Automatic power down
- TTL compatible inputs outputs
- Available in 28 pin DIP package (MS310512) or in chip form (MS310512H)
- 3-state outputs for wired-OR expansion
- EPROMs accepted as program data input
- Ultra low data retention supply

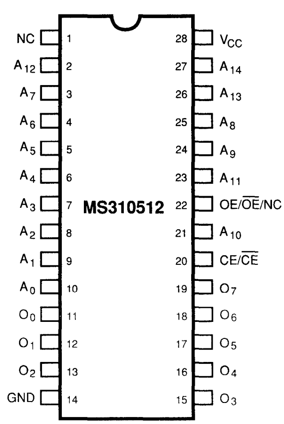
DESCRIPTION

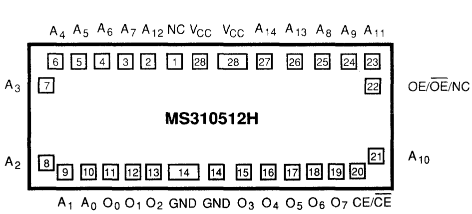
The MS310512 is a high-performance Read Only Memory organized as 65,536 words by 8 bits. It is designed to be compatible with all microprocessors and similar applications where high performance mass storage and simple interfacing are important design considerations.

The MS310512 offers automatic powerdown with power-down controlled by the Chip Enable $\overline{\text{CE}}$/CE input. When $\overline{\text{CE}}$/CE goes HIGH/LOW the device will automatically power down and remain in a low power standby mode as long as $\overline{\text{CE}}$/CE remains HIGH/LOW. Pin 22 may be mask programmed as $\overline{\text{OE}}$/OE/NC (active HIGH, active LOW or no connection). In order to eliminate bus contention in multiple bus microprocessor systems.

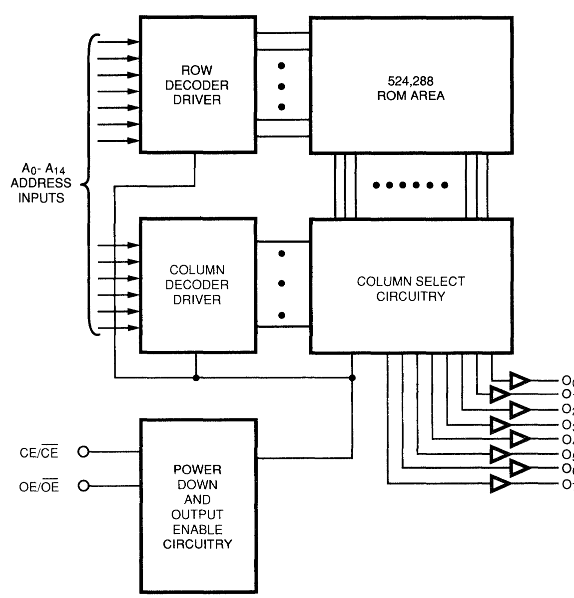
4

PIN CONFIGURATIONS





BLOCK DIAGRAM



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PIN DESCRIPTIONS

PIN NO.	SYMBOL	FUNCTION
2-10, 21, 23-27	A_0 - A_{15}	Address Input
11-13, 15-19	O_0 - O_7	Data Output
14	GND	Ground
28	V_{CC}	+5V Power Supply
20	$\overline{CE}$/CE	Chip Enable Input
22	$\overline{OE}$/OE/NC	Output Enable Input /No Connection
1	NC	No Connection

ABSOLUTE MAXIMUM RATINGS[1]

Ambient Operating Temperature	–10°C to +80°C
Storage Temperature	–65°C to +150°C
Supply Voltage to Ground Potential	–0.5V to +7.0V
Output Voltage	–0.5V to V_{CC} + 0.5V
Applied Input Voltage	–0.5V to V_{CC} + 0.5V
Power Dissipation	400 mW
Soldering Temperature and Time	260°C , 10 sec

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not recommended. Exposure to ABSOLUTE MAXIMUM RATINGS for extended periods may affect device reliability.

OPERATING RANGE

RANGE	AMBIENT TEMPERATURE	Vcc
Commercial	0°C to + 70°C	5V ± 10%

DC ELECTRICAL CHARACTERISTICS (over the commercial operating range)

PARAMETER NAME	PARAMETER	TEST CONDITIONS	MS310512 MIN.	TYP.	MAX.	UNITS
V_{IL}	Input Low Voltage		–0.5	—	0.8	V
V_{IH}	Input High Voltage		2.2		V_{CC}+ 0.3	V
I_{IL}	Input Leakage Current	V_{CC} = Max, V_{IN} = 0V to V_{CC}	—	—	10	µA
I_{OL}	Output Leakage Current	V_{OUT} = 0 V to V_{CC}	—	—	10	µA
V_{OL}	Output Low Voltage	V_{CC} = Min, I_{OL} = 3.2mA	—	—	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min, I_{OH} = –1mA	2.4	—	V_{CC}	V
I_{CC}	Operating Power Supply Current [1]		—	15	30	mA
I_{CCSB}	Standby Power Supply Current	$\overline{CE}$ = V_{IH}, CE = V_{IL}	—	0.2	1.5	mA
I_{CCSB1}	Super Standby Power Supply Current	$\overline{CE}$ = V_{CC} - 0.2V, CE = 0.2V	—	10	30	µA
I_{OS}	Output Short Circuit Current [2]		—	—	70	mA

1. Measured with device selected and outputs unloaded.
2. For a duration not to exceed 30 seconds.

CAPACITANCE (Ta=25°C, f=1.0MHz)[1]

SYMBOL	PARAMETER	CONDITION	MAX.	UNIT
C_I	Input Capacitance	T_A = 25°C	10	pF
C_O	Output Capacitance	F = 1.0MHz	10	pF

1. This parameter is guaranteed but not 100% tested.

TRUTH TABLE

PIN 20 ($\overline{CE}$/CE)	PIN 22 $\overline{OE}$/OE/NC	OUTPUTS O_0 - O_7	MODE
I	X	HI-Z	Power Down
A	I	HI-Z	Output Disable
A	A	LO-Z	Read

1. If mask programmable pin, pin 22, is customer-specified at NC (no-connection) state, the input state of pin 22 will be internally fixed at active state.

AC TEST CONDITIONS

Input Pulse Levels	0.4 ~ 2.4V
Input Rise and Fall Times	10 ns
Timing Measurement Level Reference	V_{IL} = 0.8V V_{IH} = 2.2V V_{OL} = 0.8V V_{OH} = 2.0V
Output Load	See Figure 1

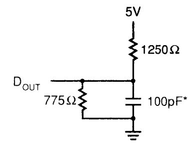


Figure 1 Output Load Circuit

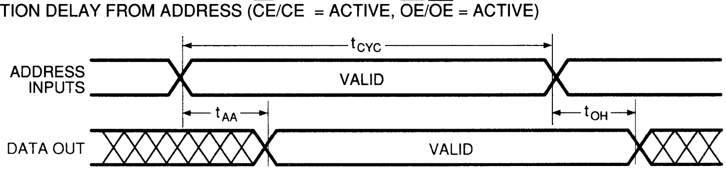
AC ELECTRICAL CHARACTERISTICS (over the operating range)

PARAMETER NAME	PARAMETER	MS310512 MIN.	MAX.	UNIT
t_{CYC}	Cycle Time	150	—	ns
t_{AA}	Address Access Time	—	150	ns
t_{ACE}	Chip Enable Access Time	—	150	ns
t_{ACS}	Output Enable Access Time	—	85	ns
t_{LZ}	Output LOW Z Delay (1)	10	—	ns
t_{HZ}	Output HIGH Z Delay (2)	0	85	
t_{OH}	Output Hold After Address Change	10	—	ns
t_{PU}	Power-Up Time	0	—	ns
t_{PD}	Powerdown Time	—	85	ns

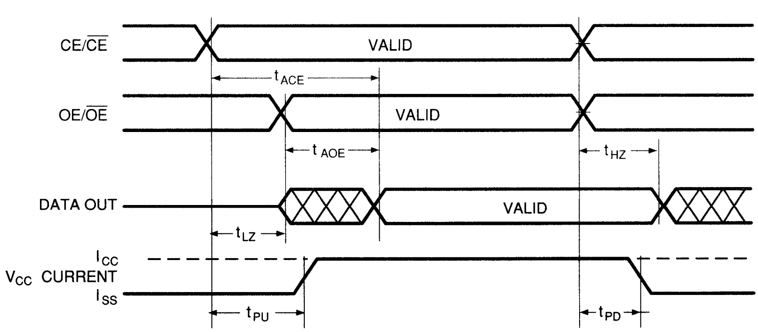
1. Output LOW impedance delay (t_{LZ}) is measured from $\overline{CE}$/CE or OE/$\overline{OE}$ going active.
2. Output HIGH impedance delay (t_{HZ}) is measured from the earlier of $\overline{CE}$/E or OE/$\overline{OE}$ going inactive.

TIMING DIAGRAMS

PROPAGATION DELAY FROM ADDRESS ($\overline{CE}$/CE = ACTIVE, $\overline{OE}$/$\overline{OE}$ = ACTIVE)



PROPAGATION DELAY FROM CHIP ENABLE or OUTPUT ENABLE (ADDRESS VALID)



ORDERING INFORMATION

SPEED (ns)	ORDERING PART NUMBER	PACKAGE REFERENCE NO.	TEMPERATURE RANGE
150	MS310512-15PC	P28-3	0°C to + 70°C
150	MS310512-15XC	Chip	0°C to + 70°C

MOSEL MS311002

131,072 X 8 CMOS Mask Programmable ROM 28 Pin DIP

FEATURES

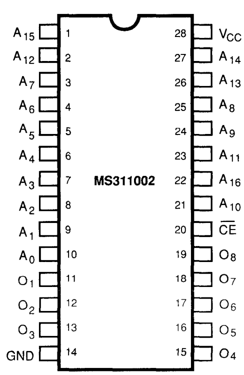
- Access time: 150ns / 200ns
- Low Power operation:
  - 40mA max. Operating
  - 50µA max. Standby
- Fully static operation
- Automatic power down ($\overline{CE}$)
- Complete TTL compatibility
- EPROMs accepted as program data input
- Ultra low data retention supply
- Standard 28 pin DIP

DESCRIPTION

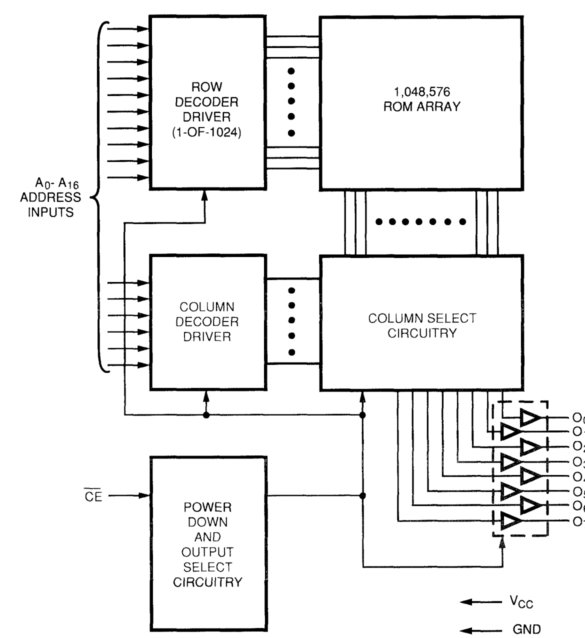
The MS311002 high performance Read Only Memory is organized as 131,072 bytes by 8 bits. It is designed to be compatible with all microprocessors and similar applications where high performance, low cost, mass storage and simple interfacing are important design considerations.

The MS311002 offer automatic powerdown with powerdown controlled by the Chip Enable ($\overline{CE}$) inputs. When $\overline{CE}$ goes HIGH the device will automatically power down and remain in a low power standby mode as long as $\overline{CE}$ remains HIGH. The MS311002 is available in a 28 pin package.

PIN CONFIGURATIONS



BLOCK DIAGRAM



PIN DESCRIPTIONS

SYMBOL	PIN NO.	FUNCTION
A_0 - A_{16}	1-10, 21-27	Address Input
O_0 - O_7	11-13, 15-19	Data Output
$\overline{CE}$	20	
GND	14	Ground
V_{CC}	28	Power Supply

ABSOLUTE MAXIMUM RATINGS[1]

Temperature Under Bias	–10°C to +85°C
Storage Temperature	–45°C to +125°C
Supply Voltage to Ground Potential	–0.3V to +7.0V
Applied Output Voltage	–0.5V to V_{CC} +0.5
Applied Input Voltage	–0.5V to V_{CC} +0.5

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not recommended. Exposure to ABSOLUTE MAXIMUM RATINGS for extended periods may affect device reliability.

OPERATING RANGE

RANGE	AMBIENT TEMPERATURE	Vcc
Commercial	0°C to + 70°C	5V ± 10%

DC ELECTRICAL CHARACTERISTICS (over the commercial operating range)

PARAMETER NAME	PARAMETER	TEST CONDITIONS	MS311002 MIN.	TYP.	MAX.	UNITS
V_{IL}	Input Low Voltage		–0.3	-	0.8	V
V_{IH}	Input High Voltage		2.2		V_{CC}+ 0.3	V
I_{IL}	Input Leakage Current	V_{CC}=Max, V_{IN}=0V to V_{CC}	-	-	10	µA
I_{OL}	Output Leakage Current	V_{OUT}=0 V to V_{CC}	-	-	10	µA
V_{OL}	Output Low Voltage	V_{CC}=Min, I_{OL}=2.1mA	-	-	0.4	V
V_{OH}	Output High Voltage	V_{CC}=Min, I_{OH}=–400mA	2.4	-	V_{CC}	V
I_{CC}	Operating Power Supply Current[1]		-	-	40	mA
I_{CCSB}	Standby Power Supply Current	$\overline{CE}$=V_{IH}, CE=V_{IL}	-	-	3	mA
I_{CCSB1}	Super Standby Power Supply Current	$\overline{CE}$=V_{CC}–0.2V, CE = 0.2V	-	-	50	µA

1. Measured with device selected and outputs unloaded.

CAPACITANCE (Ta=25°C, f=1.0MHz)[1]

SYMBOL	PARAMETER	CONDITION	MAX.	UNIT
CI	Input Capacitance	V_{IN}= 0V	10	pF
CO	OutputCapacitance	V_{OUT}= 0V	7	pF

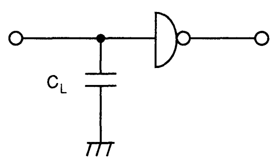
1. This parameter is guaranteed but not 100% tested.

TRUTH TABLE

MODE	$\overline{CE}$	OUTPUT OPERATION
Steady	H	High Z
Read	L	D_{OUT}

AC TEST CONDITIONS

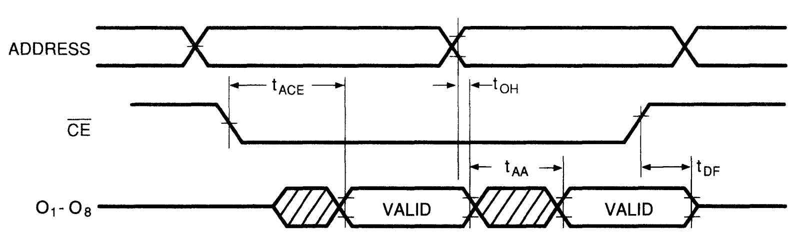
Input Pulse Levels	0.6~ 2.4V
Input Rise and Fall Times	10 ns
Timing Measurement Level	$V_{IL} = 0.8V$ $V_{IH} = 2.2V$
Reference	$V_{OL} = 0.8V$ $V_{OH} = 2.0V$
Output Load	1 TTL Gate + 100 pF



AC ELECTRICAL CHARACTERISTICS (over the operating range)

PARAMETER NAME	PARAMETER	MS311002-15 MIN.	MS311002-15 MAX.	MS311002-20 MIN.	MS311002-20 MAX.	UNIT
t_{AA}	Address Access Time	-	150	-	200	ns
t_{ACE}	Chip Enable Access Time	-	150	-	200	ns
t_{DF}	Output Disable Time	-	60	-	60	ns
t_{OH}	Output Hold Time	0	-	0	-	ns

TIMING DIAGRAMS



ORDERING INFORMATION

SPEED (ns)	ORDERING PART NUMBER	PACKAGE REFERENCE NO.	TEMPERATURE RANGE
100	MS31002-12PC	P28-4	0°C to + 70°C
120	MS31002-15PC	P28-4	0°C to + 70°C

MOSEL MS311024

131,072 X 8 CMOS Mask Programmable ROM

FEATURES

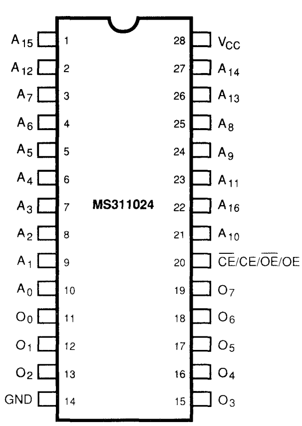
- Access time: 150ns/200ns max
- Low Power operation:
  - 40mA max. Operating
  - 30μA max. Standby
- Fully static operation
- Automatic power down ($\overline{OE}$/OE)
- Complete TTL compatibility
- 3-state outputs for wired-OR expansion
- EPROMs accepted as program data input
- Ultra low data retention supply
- Pin 20 control options (sense and type)

DESCRIPTION

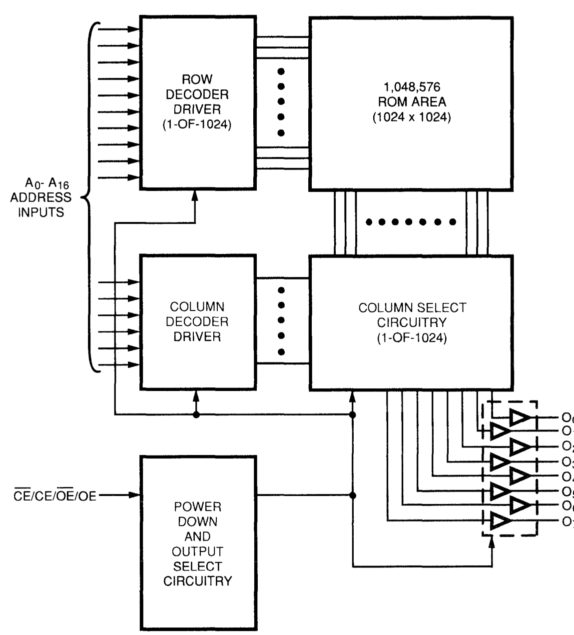
The MS311024 high performance Read Only Memory is organized as 131,072 bytes by 8 bits. It is designed to be compatible with all microprocessors and similar applications where high performance, low cost, mass storage and simple interfacing are important design considerations.

The MS311024 offers automatic powerdown with powerdown controlled by the Chip Enable ($\overline{OE}$/OE) inputs. When $\overline{OE}$/OE goes HIGH/LOW the device will automatically power down and remain in a low power standby mode as long as $\overline{OE}$/OE remains HIGH/LOW. Pin 20 may also be programmed as $\overline{CE}$/CE (active LOW or HIGH), output enable, in order to eliminate bus contention in multiple bus microprocessor systems.

PIN CONFIGURATIONS



BLOCK DIAGRAM



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PIN DESCRIPTIONS

PIN NO.	SYMBOL	FUNCTION
1-10, 21-27	A_0 - A_{16}	Address Input
11-13, 15-19	O_0 - O_7	Data Output
14	GND	Ground
28	Vcc	Power Supply
20	$\overline{OE}$/OE/$\overline{CE}$/CE	Chip Enable Inputs, Output Enable Inputs

OPERATING RANGE

RANGE	AMBIENT TEMPERATURE	Vcc
Commercial	0°C to + 70°C	5V ± 10%

ABSOLUTE MAXIMUM RATINGS[1]

Ambient Operating Temperature	-10°C to +80°C
Storage Temperature	-65°C to +150°C
Supply Voltage to Ground Potential	-0.5V to +7.0V
Applied Output Voltage	-0.5V to +7.0V
Applied Input Voltage	-0.5V to +7.0V
Power Dissipation	300 mW
Soldering Temperature and Time	260°C , 10 seconds

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not recommended. Exposure to ABSOLUTE MAXIMUM RATINGS for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS (over the commercial operating range)

PARAMETER NAME	PARAMETER	TEST CONDITIONS	MS311024 MIN.	TYP.	MAX.	UNITS
V_{IL}	Input Low Voltage		–0.5	—	0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC}+ 0.3	V
I_{IL}	Input Leakage Current	V_{CC} = Max, V_{IN} = 0V to V_{CC}	—	—	10	µA
I_{OL}	Output Leakage Current	V_{OUT} = 0 V to V_{CC}	—	—	10	µA
V_{OL}	Output Low Voltage	V_{CC} = Min, I_{OL} = 3.2mA	—	—	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min, I_{OH} = -1mA	2.4	—	V_{CC}	V
I_{CC}	Operating Power Supply Current (1)		—	—	40	mA
I_{CCSB}	Standby Power Supply Current	$\overline{E}$ = V_{IH}, E = V_{IL}	—	—	1.5	mA
I_{CCSB1}	Super Standby Power Supply Current	$\overline{E}$ = V_{CC} - 0.2V, E = 0.2V	—	—	50	µA
I_{OS}	Output Short Circuit Current (2)		—	—	70	mA

1. Measured with device selected and outputs unloaded.
2. For a duration not to exceed 30 seconds.

CAPACITANCE (Ta=25°C, f=1.0MHz)[1]

SYMBOL	PARAMETER	CONDITION	MAX.	UNIT
CI	Input Capacitance	V_{IN} = 0V	10	pF
CO	Output Capacitance	V_{OUT} = 0V	10	pF

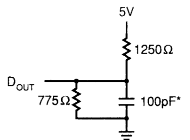
1. This parameter is guaranteed but not 100% tested.

TRUTH TABLE

PIN 20	$\overline{CE}$	$\overline{OE}$	MODE	D_0-D_7	SUPPLY CURRENT
Chip Select Operation	L/H	—	Selected	D_{OUT}	Operating (I_{CC})
	H/L	—	Non selected	High Z	Standby
Output Enable Operation	—	L/H	Selected	D_{OUT}	Operating (I_{CC})
	—	H/L	Non selected	High Z	

AC TEST CONDITIONS

Input Pulse Levels	0.4 ~ 2.4V
Input Rise and Fall Times	10 ns
Timing Measurement Level Reference	$V_{IL} = 0.8V$ $V_{IH} = 2.2V$ $V_{OL} = 0.8V$ $V_{OH} = 2.0V$
Output Load	See Figure 1



* INCLUDING SCOPE AND JIG

Figure 1 Output Load Circuit

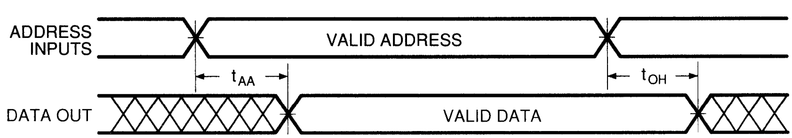
AC ELECTRICAL CHARACTERISTICS (over the operating range)

PARAMETER NAME	PARAMETER	MS311024-15 MIN.	MS311024-15 MAX.	MS311024-20 MIN.	MS311024-20 MAX.	UNIT
t_{CYC}	Cycle Time	150	—	200	—	ns
t_{AA}	Address Access Time	—	150	—	200	ns
t_{ACE}	Chip Enable Access Time	—	150	—	200	ns
t_{OE}	Output Enable Access Time	—	85	—	100	ns
t_{LZ}	Output LOW Z Delay (1)	10	–	10	—	ns
t_{HZ}	Output HIGH Z Delay (2)	0	85	0	100	ns
t_{OH}	Output Hold After Address Change	10	—	10	—	ns
t_{PU}	Power-Up Time	0	—	0	—	ns
t_{PD}	Powerdown Time	—	85	—	100	ns

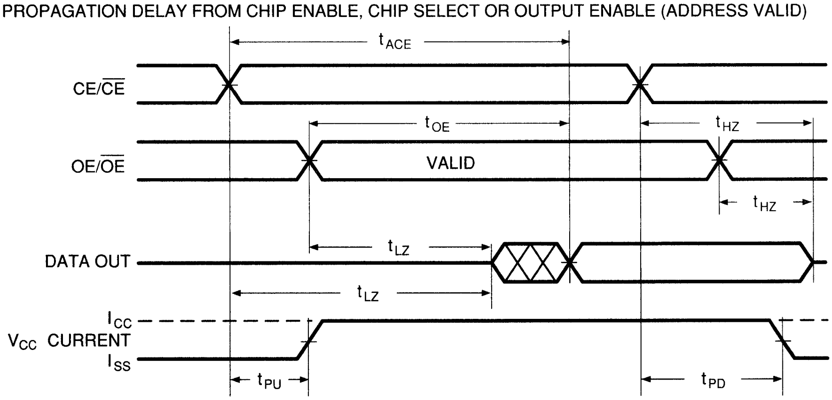
1. Output LOW impedance delay (t_{LZ}) is measured from OE/$\overline{OE}$ or CE/$\overline{CE}$ going active.
2. Output HIGH impedance delay (t_{HZ}) is measured from the earlier of OE/$\overline{OE}$ or CE/$\overline{CE}$ going active.

TIMING DIAGRAMS

PROPAGATION DELAY FROM ADDRESS ($\overline{OE}$/OE = ACTIVE, $\overline{CE}$/CE = ACTIVE)



PROPAGATION DELAY FROM CHIP ENABLE, CHIP SELECT OR OUTPUT ENABLE (ADDRESS VALID)



ORDERING INFORMATION

SPEED (ns)	ORDERING PART NUMBER	PACKAGE REFERENCE NO.	TEMPERATURE RANGE
150	MS311024-15PC	P28-3	0°C to + 70°C
200	MS311024-20PC		0°C to + 70°C
150	MS311024-15FC	S28-4	0°C to +70°C
200	MS311024-20FC		0°C to +70°C

High Speed 131,072 X 8 CMOS Mask Programmable ROM Compatible with All 32 Pin DIP EPROMs

FEATURES

- Access time: 100ns/120ns/150ns
- Low Power operation:
  - 40mA max. Operating
  - 50µA max. Standby
- Fully static operation
- Automatic power down ($\overline{CE}$/CE)
- Complete TTL compatibility
- 3-state outputs for wired-OR expansion
- EPROMs accepted as program data input
- Ultra low data retention supply
- Pins 2, 22, 30, 31 control options (sense and type)

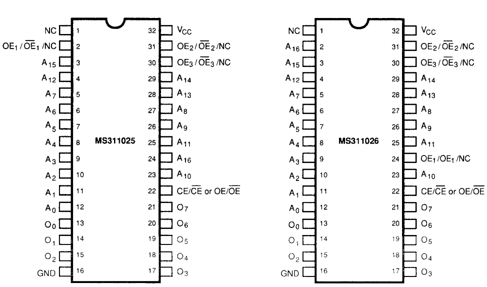
DESCRIPTION

The MS311025/311026 high performance Read Only Memory is organized as 131,072 bytes by 8 bits. It is designed to be compatible with all microprocessors and similar applications where high performance, low cost, mass storage and simple interfacing are important design considerations.

The MS311025/311026 offer automatic powerdown with powerdown controlled by the Chip Enable ($\overline{CE}$/CE) inputs. When $\overline{CE}$/CE goes HIGH/LOW the device will automatically power down and remain in a low power standby mode as long as $\overline{CE}$/CE remains HIGH/LOW. Pins 2, 22, 30, 31 allow Chip Select (CE_N) or Output Enable (OE_N) or No Connect (NC) operations from 1 to 8 devices to eliminate bus contention in multiple bus microprocessor systems.

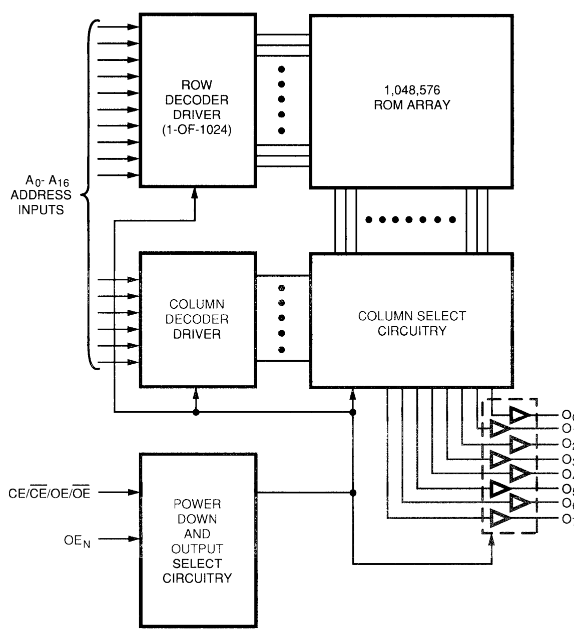
4

PIN CONFIGURATIONS



(A) (B)

BLOCK DIAGRAM



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PIN DESCRIPTIONS

PIN NO.	SYMBOL	FUNCTION
3-12, 23, 25-29	A_0 - A_{15}	Address Input
13-15, 17-21	O_0 - O_7	Data Output
16	GND	Ground
32	V_{CC}	Power Supply
1	NC	No Connection
22	CE/CE/$\overline{OE}$/OE	Chip Select/Chip Enable or Input [1] or
2	OE_1/$\overline{OE}_1$/NC (-A)	Output Enable 1 [2]
	A_{16} (-B)	Address Input
24	A_{16} (-A)	Address Input
	OE_1/OE_1/NC (-B)	Output Enable 1 [2]
31	OE_2/OE_2/NC	Output Enable 2 [2]
30	OE_3/OE_3/NC	Output Enable 3 [2]

1. This pin is user-definable as active high or active low.
2. N/C is "No Connection".

ABSOLUTE MAXIMUM RATINGS[1]

Ambient Operating Temperature	–10°C to +80°C
Storage Temperature	–65°C to +150°C
Supply Voltage to Ground Potential	–0.5V to +7.0V
Applied Output Voltage	–0.5V to +7.0V
Applied Input Voltage	–0.5V to +7.0V
Power Dissipation	300 mW
Soldering Temperature and Time	260°C , 10 sec

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not recommended. Exposure to ABSOLUTE MAXIMUM RATINGS for extended periods may affect device reliability.

OPERATING RANGE

RANGE	AMBIENT TEMPERATURE	Vcc
Commercial	0°C to + 70°C	5V ± 10%

DC ELECTRICAL CHARACTERISTICS (over the commercial operating range)

PARAMETER NAME	PARAMETER	TEST CONDITIONS	MS312001 MIN.	TYP.	MAX.	UNITS
V_{IL}	Input Low Voltage		–0.5	-	0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC}+ 0.3	V
I_{IL}	Input Leakage Current	V_{CC}=Max, V_{IN}=0V to V_{CC}	-	-	10	µA
I_{OL}	Output Leakage Current	V_{OUT}=0 V to V_{CC}	-	-	10	µA
V_{OL}	Output Low Voltage	V_{CC}=Min, I_{OL}=3.2mA	-	-	0.4	V
V_{OH}	Output High Voltage	V_{CC}=Min, I_{OH}=-1mA	2.4	-	V_{CC}	V
I_{CC}	Operating Power Supply Current [1]		-	-	40	mA
I_{CCSB}	Standby Power Supply Current	$\overline{CE}$=V_{IH}, CE=V_{IL}	-	-	1.5	mA
I_{CCSB1}	Super Standby Power Supply Current	$\overline{CE}$=V_{CC}–0.2V, CE = 0.2V	-	-	30	µA
I_{OS}	Output Short Circuit Current [2]		-	-	70	mA

1. Measured with device selected and outputs unloaded.
2. For a duration not to exceed 30 seconds.

CAPACITANCE (Ta=25°C, f=1.0MHz)[1]

SYMBOL	PARAMETER	CONDITION	MAX.	UNIT
CI	Input Capacitance	V_{IN}= 0V	10	pF
CO	OutputCapacitance	V_{OUT}= 0V	10	pF

1. This parameter is guaranteed but not 100% tested.

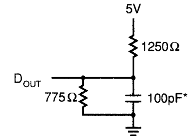
TRUTH TABLE

CE	OE_1 MS311025 (Pin 2) MS311026 (Pin 24)	OE_2	OE_3	O_0 - O_7	MODE
A	A	A	A	Output Data	Read
I	X	X	X	HI - Z	Power Down
A	I	X	X	HI - Z	Output Disable
A	X	I	X	HI - Z	Output Disable
A	X	X	I	HI - Z	Output Disable

1. CE/$\overline{CE}$, OE_1/$\overline{OE}_1$/NC, OE_2/$\overline{OE}_2$/NC, OE_3/$\overline{OE}_3$/NC are mask programmable which can be selected for active low, active high or no connection.
2. "A" means "Active." "I" means "Inactive." "X" means "Don't Care."
3. If CE/$\overline{CE}$ is a no-connection, the input level will be internally pulled high.

AC TEST CONDITIONS

Input Pulse Levels	0.4 ~ 2.4V
Input Rise and Fall Times	10 ns
Timing Measurement Level	V_{IL} = 0.8V V_{IH} = 2.2V
Reference	V_{OL} = 0.8V V_{OH} = 2.0V
Output Load	See Figure 1



* INCLUDING SCOPE AND JIG

Figure 1 Output Load Circuit

4

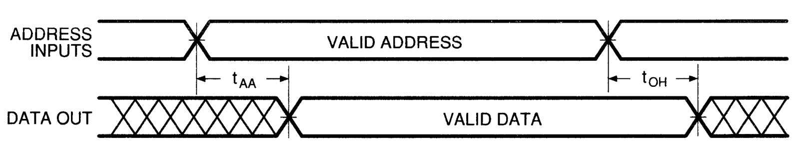
AC ELECTRICAL CHARACTERISTICS (over the operating range)

PARAMETER NAME	PARAMETER	MS311025 MS311026 -10 MIN.	MAX.	MS311025 MS311026 -12 MIN.	MAX.	MS311025 MS311026 -15 MIN.	MAX.	UNIT
t_{CYC}	Cycle Time	100	-	120	-	150	-	ns
t_{AA}	Chip Access Time	-	100	-	120	-	150	ns
t_{ACE}	Chip Enable Access Time	-	100	-	120	-	150	ns
t_{ACS}	Chip Select Access Time	-	75	-	85	-	100	ns
t_{AOE}	Output Enable Access Time	-	50	-	60	-	90	ns
t_{OH}	Output Hold After Address Change	10	-	10	-	10	-	ns
t_{HZ}	Output High Z Delay(1)	-	50	-	50	-	50	ns
t_{LZ}	Output Low Z Delay	10	-	10	-	10	-	ns
t_{PU}	Power-Up Time	0	-	0	-	0	-	ns
t_{PD}	Power-Down Time	-	50	-	50	-	50	ns

1. Output HIGH impedance delay (t_{HZ}) is measured from the earlier of CE/$\overline{CE}$ or OE/$\overline{OE}$ going active.

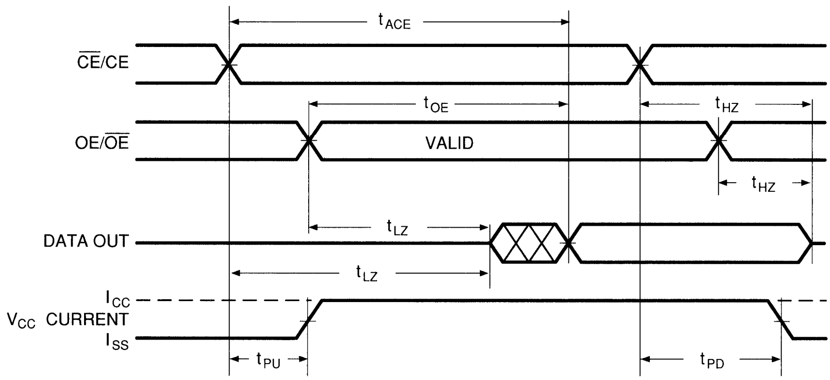
TIMING DIAGRAMS

PROPAGATION DELAY FROM ADDRESS ($\overline{CE}$/CE = LOW/HIGH, $\overline{OE}$/OE = ACTIVE)



TIMING DIAGRAMS

PROPAGATION DELAY FROM CHIP ENABLE, CHIP SELECT OR OUTPUT ENABLE (ADDRESS VALID)



ORDERING INFORMATION

SPEED (ns)	ORDERING PART NUMBER	PACKAGE REFERENCE NO.	TEMPERATURE RANGE
100	MS311025-10PC	P32-1	0°C to + 70°C
120	MS311025-12PC		0°C to + 70°C
150	MS311025-15PC		0°C to +70°C
100	MS311026-10PC		0°C to + 70°C
120	MS311026-12PC		0°C to + 70°C
150	MS311026-15PC		0°C to +70°C

High Speed 262,144 X 8 CMOS Mask Programmable ROM Compatible with All 32 Pin DIP EPROMs

FEATURES

- Access time: 100ns/120ns
- Low Power operation:
  - 40mA max. Operating
  - 30µA max. Standby
- Fully static operation
- Automatic power down ($\overline{CE}$/CE)
- Complete TTL compatibility
- 3-state outputs for wired-OR expansion
- EPROMs accepted as program data input
- Ultra low data retention supply
- Pins 2, 22, 31 control options (sense and type)

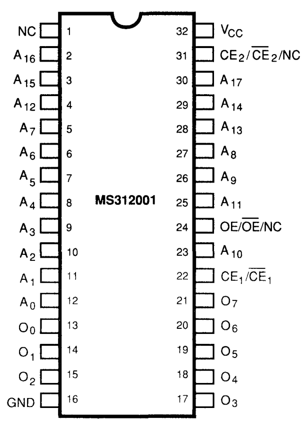
DESCRIPTION

The MS312001 high performance Read Only Memory is organized as 262,144 bytes by 8 bits. It is designed to be compatible with all microprocessors and similar applications where high performance, low cost, mass storage and simple interfacing are important design considerations.

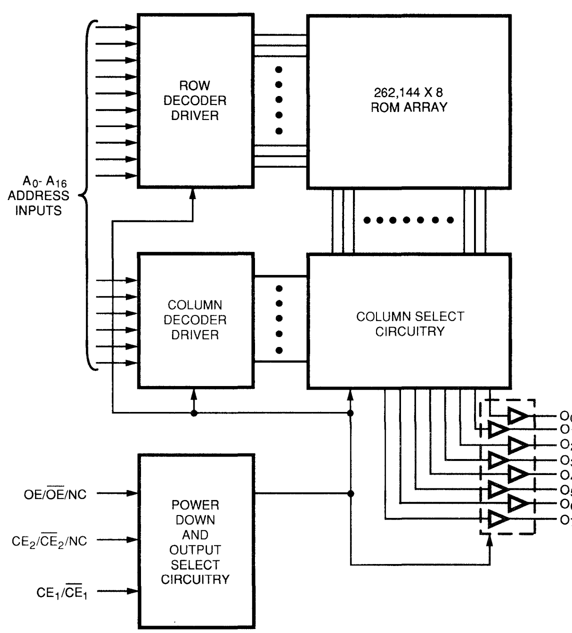
The MS312001 offer automatic powerdown with powerdown controlled by the Chip Enable ($\overline{CE}$/CE) inputs. When $\overline{CE}$/CE goes HIGH/LOW the device will automatically power down and remain in a low power standby mode as long as $\overline{CE}$/CE remains HIGH/LOW. Pins 2, 22, 31 allow Chip Select ($\overline{CE}_N$) or Output Enable ($\overline{OE}_N$) or No Connect (NC) operations from 1 to 8 devices to eliminate bus contention in multiple bus microprocessor systems.

4

PIN CONFIGURATIONS



BLOCK DIAGRAM



PIN DESCRIPTIONS

PIN NO.	SYMBOL	FUNCTION
2-12, 23, 25-30	A_0 - A_{17}	Address Input
13-15, 17-21	O_0 - O_7	Data Output
16	GND	Ground
32	V_{CC}	Power Supply
1	NC	No Connection
22	CE/$\overline{CE}$	Chip Select/Chip Enable or Input [1]
24	$\overline{OE}_1$/OE_1/NC	Output Enable 1 [2]
31	OE_2/$\overline{OE}_2$/NC	Output Enable 2 [2]

1. This pin is user-definable as active high or active low.
2. N/C is "No Connection".

ABSOLUTE MAXIMUM RATINGS[1]

Ambient Operating Temperature	–10°C to +80°C
Storage Temperature	–65°C to +150°C
Supply Voltage to Ground Potential	–0.5V to +7.0V
Applied Output Voltage	–0.5V to +7.0V
Applied Input Voltage	–0.5V to +7.0V
Power Dissipation	300 mW
Soldering Temperature and Time	260°C , 10 sec

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not recommended. Exposure to ABSOLUTE MAXIMUM RATINGS for extended periods may affect device reliability.

OPERATING RANGE

RANGE	AMBIENT TEMPERATURE	Vcc
Commercial	0°C to + 70°C	5V ± 10%

DC ELECTRICAL CHARACTERISTICS (over the commercial operating range)

PARAMETER NAME	PARAMETER	TEST CONDITIONS	MS312001 MIN.	TYP.	MAX.	UNITS
V_{IL}	Input Low Voltage		–0.5	-	0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC}+ 0.3	V
I_{IL}	Input Leakage Current	V_{CC}=Max, V_{IN}=0V to V_{CC}	-	-	10	µA
I_{OL}	Output Leakage Current	V_{OUT}=0 V to V_{CC}	-	-	10	µA
V_{OL}	Output Low Voltage	V_{CC}=Min, I_{OL}=3.2mA	-	-	0.4	V
V_{OH}	Output High Voltage	V_{CC}=Min, I_{OH}=-1mA	2.4	-	V_{CC}	V
I_{CC}	Operating Power Supply Current [1]		-	-	40	mA
I_{CCSB}	Standby Power Supply Current	$\overline{CE}$=V_{IH}, CE=V_{IL}	-	-	1.5	mA
I_{CCSB1}	Super Standby Power Supply Current	$\overline{CE}$=V_{CC}–0.2V, CE = 0.2V	-	-	30	µA
I_{OS}	Output Short Circuit Current [2]		-	-	70	mA

1. Measured with device selected and outputs unloaded.
2. For a duration not to exceed 30 seconds.

CAPACITANCE (Ta=25°C, f=1.0MHz)[1]

SYMBOL	PARAMETER	CONDITION	MAX.	UNIT
CI	Input Capacitance	V_{IN}= 0V	10	pF
CO	OutputCapacitance	V_{OUT}= 0V	10	pF

1. This parameter is guaranteed but not 100% tested.

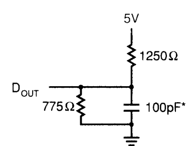
TRUTH TABLE

$CE_1/\overline{CE}_1$	$CE_2/\overline{CE}_2$/NC	$OE/\overline{OE}$/NC	O_0 - O_7	MODE
A	A	A	Output Data	Read
I	X	X	HI - Z	Power Down
X	I	X	HI - Z	Output Disable
A	A	I	HI - Z	Output Disable

1. $CE_1/\overline{CE}_1$/NC, $CE_2/\overline{CE}_2$/NC, $OE/\overline{OE}$/NC are mask programmable which can be selected for active low, active high or no connection.
2. "A" means "Active." "I" means "Inactive." "X" means "Don't Care."
3. If $CE/\overline{CE}$ is a no-connection, the input level will be internally pulled high.

AC TEST CONDITIONS

Input Pulse Levels	0.4 ~ 2.4V
Input Rise and Fall Times	10 ns
Timing Measurement Level Reference	V_{IL} = 0.8V V_{IH} = 2.2V V_{OL} = 0.8V V_{OH} = 2.0V
Output Load	See Figure 1



* INCLUDING SCOPE AND JIG

Figure 1 Output Load Circuit

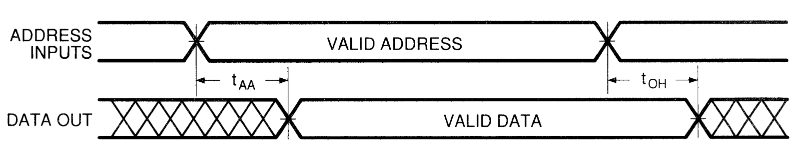
AC ELECTRICAL CHARACTERISTICS (over the operating range)

PARAMETER NAME	PARAMETER	MS312001 -12 MIN.	MS312001 -12 MAX.	MS312001 -15 MIN.	MS312001 -15 MAX.	UNIT
t_{CYC}	Cycle Time	120	-	150	-	ns
t_{AA}	Chip Access Time	-	120	-	150	ns
t_{ACE}	Chip Enable Access Time	-	120	-	150	ns
t_{ACS}	Chip Select Access Time	-	85	-	100	ns
t_{AOE}	Output Enable Access Time	-	60	-	85	ns
t_{OH}	Output Hold After Address Change	10	-	10	-	ns
t_{HZ}	Output High Z Delay(1)	-	60	-	85	ns
t_{LZ}	Output Low Z Delay	10	-	10	-	ns
t_{PU}	Power-Up Time	0	-	0	-	ns
t_{PD}	Power-Down Time	-	60	-	85	ns

1. Output HIGH impedance delay (t_{HZ}) is measured from the earlier of $CE/\overline{CE}$ or $OE/\overline{OE}$ going active.

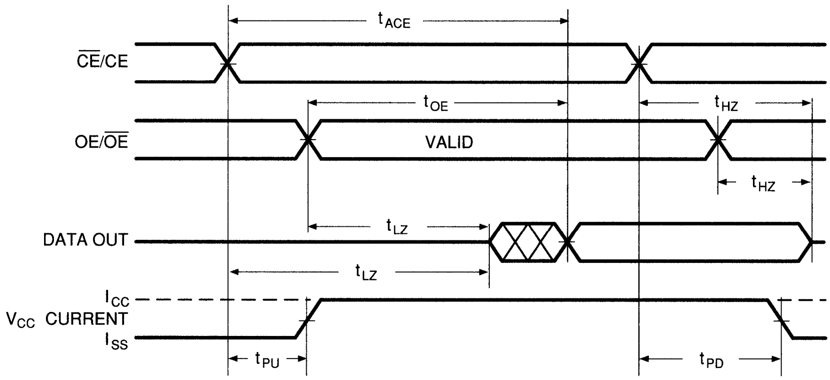
TIMING DIAGRAMS

PROPAGATION DELAY FROM ADDRESS ($\overline{CE}$/CE = LOW/HIGH, $\overline{OE}$/OE = ACTIVE)



TIMING DIAGRAMS

PROPAGATION DELAY FROM CHIP ENABLE, CHIP SELECT OR OUTPUT ENABLE (ADDRESS VALID)



ORDERING INFORMATION

SPEED (ns)	ORDERING PART NUMBER	PACKAGE REFERENCE NO.	TEMPERATURE RANGE
120	MS312001-12PC	P32-1	0°C to + 70°C
150	MS312001-15PC		0°C to +70°C

262,144 X 8 CMOS Mask Programmable ROM 32 Pin DIP

FEATURES

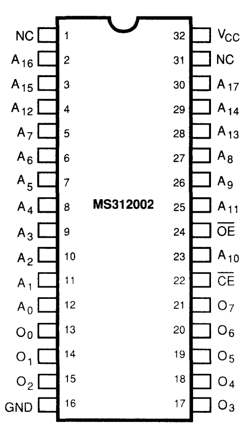
- Access time: 200ns
- Low Power operation:
  - 40mA max. Operating
  - 50µA max. Standby
- Fully static operation
- Automatic power down ($\overline{CE}$)
- Complete TTL compatibility
- 3-state outputs for wired-OR expansion
- EPROMs accepted as program data input
- 32 Pin DIP Package

DESCRIPTION

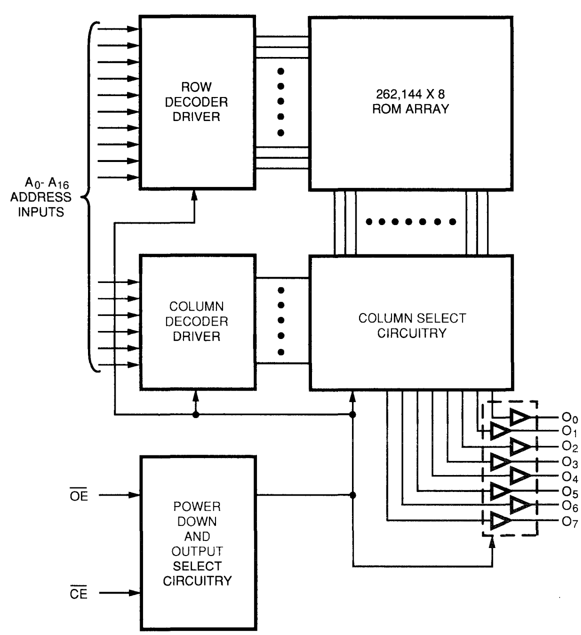
The MS312002 high performance Read Only Memory is organized as 262,144 bytes by 8 bits. It is designed to be compatible with all microprocessors and similar applications where high performance, low cost, mass storage and simple interfacing are important design considerations.

The MS312002 offer automatic powerdown with powerdown controlled by the Chip Enable ($\overline{CE}$) inputs. When $\overline{CE}$ goes HIGH the device will automatically power down and remain in a low power standby mode as long as $\overline{CE}$ remains HIGH.

PIN CONFIGURATIONS



BLOCK DIAGRAM



PIN DESCRIPTIONS

SYMBOL	PIN NO.	FUNCTION
A_0 - A_{17}	2-12, 25-30	Address Input
O_0 - O_7	13-15, 17-21	Data Output
GND	16	Ground
V_{CC}	32	Power Supply
NC	1, 31	No Connection
$\overline{CE}$	22	Chip Enable
$\overline{OE}$	24	Output Enable 1 (2)

ABSOLUTE MAXIMUM RATINGS(1)

Storage Temperature Under Bias	–10°C to +85°C
Storage Temperature	–45°C to +125°C
Supply Voltage to Ground Potential	–0.3V to +7.0V
Applied Output Voltage	–0.5V to V_{CC} +0.5
Applied Input Voltage	–0.5V to V_{CC} +0.5

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not recommended. Exposure to ABSOLUTE MAXIMUM RATINGS for extended periods may affect device reliability.

OPERATING RANGE

RANGE	AMBIENT TEMPERATURE	Vcc
Commercial	0°C to + 70°C	5V ± 10%

DC ELECTRICAL CHARACTERISTICS (over the commercial operating range)

PARAMETER NAME	PARAMETER	TEST CONDITIONS	MS312002 MIN.	TYP.	MAX.	UNITS
V_{IL}	Input Low Voltage		–0.3	-	0.8	V
V_{IH}	Input High Voltage		2.2		V_{CC}+ 0.3	V
I_{IL}	Input Leakage Current	V_{CC}=Max, V_{IN}=0V to V_{CC}	-	-	10	µA
I_{OL}	Output Leakage Current	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IH}	-	-	10	µA
V_{OL}	Output Low Voltage	V_{CC}=Min, I_{OL}=2.1mA	-	-	0.4	V
V_{OH}	Output High Voltage	V_{CC}=Min, I_{OH}=–400mA	2.4	-	-	V
I_{CC}	Operating Power Supply Current (1)	$\overline{CE}$=V_{IL}, Min. Cyc.	-	-	40	mA
I_{CCSB}	Standby Power Supply Current	$\overline{CE}$=V_{IH}	-	-	3	mA
I_{CCSB1}	Super Standby Power Supply Current	$\overline{CE}$ = V_{IH}= V_{CC}, V_{SS} or V_{CC}	-	-	50	µA

CAPACITANCE (Ta=25°C, f=1.0MHz)(1)

SYMBOL	PARAMETER	CONDITION	MAX.	UNIT
CI	Input Capacitance	V_{IN}= 0V	10	pF
CO	Output Capacitance	V_{OUT}= 0V	15	pF

1. This parameter is guaranteed but not 100% tested.

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	MODE	OUTPUT	POWER MODE
H	X	Not Selected	High-Z	Standby
L	H	Not Selected	High-Z	Active
L	L	Selected	Data Out	Active

AC TEST CONDITIONS

Input Pulse Levels	0.6 to 2.4V
Input Rise and Fall Times	5 ns
Timing Measurement Level	$V_{IL} = 0.8V$ $V_{IH} = 2.2V$
Reference	$V_{OL} = 0.8V$ $V_{OH} = 2.2V$
Output Load	1 TTL Load and 100pF

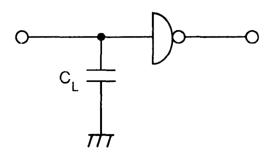


Figure 1. Output Load Circuit

4

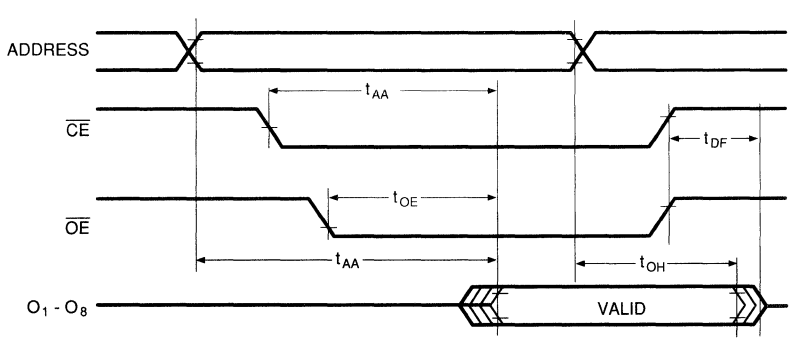
AC ELECTRICAL CHARACTERISTICS (over the operating range)

PARAMETER NAME	PARAMETER	TEST CONDITION	MS312001-12 MIN.	TYP.	MAX.	UNIT
t_{AA}	Address Access Time	$\overline{CE} = \overline{OE} = V_{IL}$	-		200	ns
t_{ACE}	CE Access Time	$\overline{OE} = V_{IL}$	-		200	ns
t_{OE}	OE Access Time	Note 1	-		100	ns
t_{DF}	Output Disable Time	Note 2	-		60	ns
t_{OH}	Output Hold Time	$\overline{CE} = \overline{OE} = V_{IL}$	0		-	ns

Note 1: $\overline{OE}$ may be delayed up to (t_A-t_{OE}) after the falling edge of $\overline{CE}$ without impact on t_{ACE}.

Note 2: t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs earlier.

TIMING DIAGRAM



ORDERING INFORMATION

SPEED (ns)	ORDERING PART NUMBER	PACKAGE REFERENCE NO.	TEMPERATURE RANGE
200	MS312001A-20PC	P32-2	0°C to + 70°C

MOSEL MS314001

PRELIMINARY

524,288 X 8 CMOS Mask Programmable ROM Compatible with All 32 Pin DIP EPROMs

FEATURES

- Access time: 120ns/150ns
- Low Power operation:
  - 50mA max. Operating
  - 30µA max. Standby
- Fully static operation
- Automatic power down ($\overline{CE}$/CE)
- Complete TTL compatibility
- 3-state outputs for wired-OR expansion
- EPROMs accepted as program data input
- Ultra low data retention supply
- Pin 22 Chip Enable
- Pin 24 Output Enable OE/$\overline{OE}$
- Pin 1 Optional Output Enable

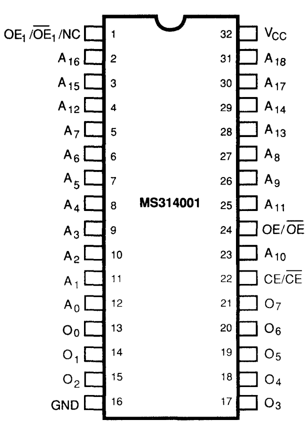
DESCRIPTION

The MS314001 high performance Read Only Memory is organized as 524,288 bytes by 8 bits. It is designed to be compatible with all microprocessors and similar applications where high performance, low cost, mass storage and simple interfacing are important design considerations.

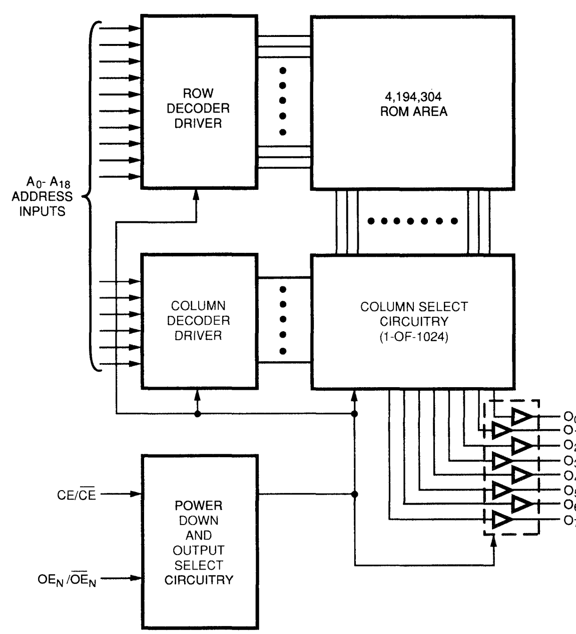
The MS314001 offer automatic powerdown with powerdown controlled by the Chip Enable ($\overline{CE}$/CE) inputs. When $\overline{CE}$/CE goes HIGH/LOW the device will automatically power down and remain in a low power standby mode as long as $\overline{CE}$/CE remains HIGH/LOW. Pins 1 and 24 allow output enable selections for control of up to 4 devices to eliminate bus contention in multiple bus microprocessor systems.

4

PIN CONFIGURATIONS



BLOCK DIAGRAM



PIN DESCRIPTIONS

PIN NO.	SYMBOL	FUNCTION
2-12, 23, 25-31	A_0 - A_{18}	Address Input
13-15, 17-21	O_0 - O_7	Data Output
16	GND	Ground
32	V_{CC}	Power Supply
1	$OE_1/\overline{OE}_1$/NC	Optional Output Enable $_1$ (2)
22	CE/$\overline{CE}$	Chip Enable
24	OE/$\overline{OE}$	Output Enable

1. This pin is user-definable as active high or active low.
2. N/C is "No Connection".

ABSOLUTE MAXIMUM RATINGS(1)

Ambient Operating Temperature	–10°C to +80°C
Storage Temperature	–65°C to +150°C
Supply Voltage to Ground Potential	–0.5V to +7.0V
Applied Output Voltage	–0.5V to +7.0V
Applied Input Voltage	–0.5V to +7.0V
Power Dissipation	800 mW
Soldering Temperature and Time	260°C , 10 sec

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not recommended. Exposure to ABSOLUTE MAXIMUM RATINGS for extended periods may affect device reliability.

OPERATING RANGE

RANGE	AMBIENT TEMPERATURE	Vcc
Commercial	0°C to + 70°C	5V ± 10%

DC ELECTRICAL CHARACTERISTICS (over the commercial operating range)

PARAMETER NAME	PARAMETER	TEST CONDITIONS	MS314001 MIN.	TYP.	MAX.	UNITS
V_{IL}	Input Low Voltage		–0.5	-	0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC}+ 0.3	V
I_{IL}	Input Leakage Current	V_{CC}=Max, V_{IN}=0V to V_{CC}	-	-	10	µA
I_{OL}	Output Leakage Current	V_{OUT}=0 V to V_{DD} , CE=V_{IH}	-	-	10	µA
V_{OL}	Output Low Voltage	V_{CC}=Min, I_{OL}=3.2mA	-	-	0.4	V
V_{OH}	Output High Voltage	V_{CC}=Min, I_{OH}=-1mA	2.4	-	V_{CC}	V
I_{CC}	Operating Power Supply Current (1)		-	-	40	mA
I_{CCSB}	Standby Power Supply Current	$\overline{CE}$=V_{IH}, CE=V_{IL}	-	-	1.5	mA
I_{CCSB1}	Super Standby Power Supply Current	$\overline{CE}$=V_{CC}–0.2V, CE = 0.2V	-	-	30	µA
I_{OS}	Output Short Circuit Current (2)		-	-	50	mA

1. Measured with device selected and outputs unloaded.
2. For a duration not to exceed 30 seconds.

CAPACITANCE (Ta=25°C, f=1.0MHz)(1)

SYMBOL	PARAMETER	CONDITION	MAX.	UNIT
CI	Input Capacitance	V_{IN}= 0V	10	pF
CO	OutputCapacitance	V_{OUT}= 0V	10	pF

1. This parameter is guaranteed but not 100% tested.

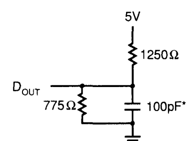
TRUTH TABLE

CE	OE_1	OE_2	O_0 - O_7	MODE
A	A	A	Output Data	Read
I	X	X	HI - Z	Power Down
A	I	X	HI - Z	Output Disable
A	X	I	HI - Z	Output Disable
A	X	X	HI - Z	Output Disable

1. CE/$\overline{CE}$, OE_1/$\overline{OE}_1$/NC, are mask programmable which can be selected for active low, active high or no connection.
2. "A" means "Active." "I" means "Inactive." "X" means "Don't Care."
3. If CE/$\overline{CE}$ is a no-connection, the input level will be internally pulled high.

AC TEST CONDITIONS

Input Pulse Levels	0.4 ~ 2.4V
Input Rise and Fall Times	10 ns
Timing Measurement Level	V_{IL} = 0.8V V_{IH} = 2.2V
Reference	V_{OL} = 0.8V V_{OH} = 2.0V
Output Load	See Figure 1



* INCLUDING SCOPE AND JIG

Figure 1 Output Load Circuit

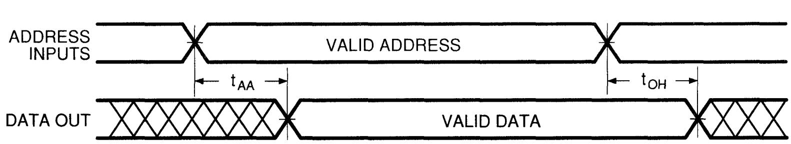
AC ELECTRICAL CHARACTERISTICS (over the operating range)

PARAMETER NAME	PARAMETER	MS314001 -12 MIN.	MS314001 -12 MAX.	MS314001 -15 MIN.	MS314001 -15 MAX.	UNIT
t_{CYC}	Cycle Time	120	-	150	-	ns
t_{AA}	Chip Access Time	-	120	-	150	ns
t_{ACE}	Chip Enable Access Time	-	120	-	150	ns
t_{AOE}	Output Enable Access Time	-	45	-	45	ns
t_{OH}	Output Hold After Address Change	10	-	10	-	ns
t_{HZ}	Output High Z Delay (1)	-	45	-	45	ns
t_{LZ}	Output Low Z Delay	10	-	10	-	ns
t_{PU}	Power-Up Time	0	-	0	-	ns
t_{PD}	Power-Down Time	-	50	-	50	ns

1. Output HIGH impedance delay (t_{HZ}) is measured from the earlier of CE/$\overline{CE}$ or OE/$\overline{OE}$ going active.

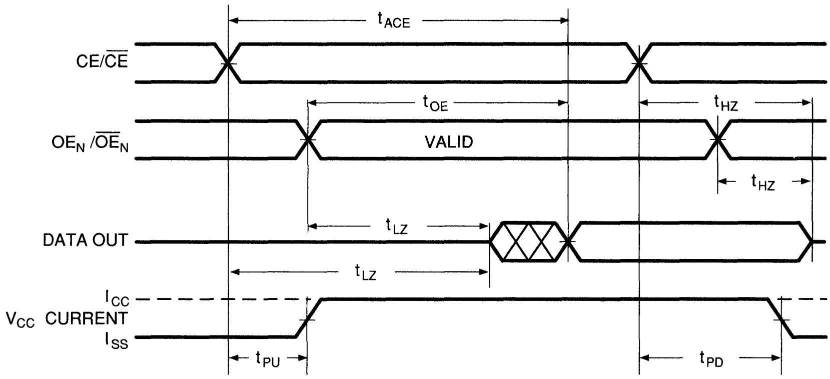
TIMING DIAGRAMS

PROPAGATION DELAY FROM ADDRESS ($\overline{CE}$/CE = LOW/HIGH, $\overline{OE}_N$/OE_N = ACTIVE)



TIMING DIAGRAMS

PROPAGATION DELAY FROM CHIP ENABLE, CHIP SELECT OR OUTPUT ENABLE (ADDRESS VALID)



ORDERING INFORMATION

SPEED (ns)	ORDERING PART NUMBER	PACKAGE REFERENCE NO.	TEMPERATURE RANGE
120	MS314001-12PC	P32-1	0°C to + 70°C
150	MS314001-15PC		0°C to +70°C

524,288 X 8 CMOS Mask Programmable ROM Compatible with All 32 Pin DIP EPROMs

FEATURES

- Access time: 200ns
- Ultra Low Power operation:
  - 275mW max., Operating
  - 5.5mW max., Standby, TTL input level
  - 275μW max., Standby, CMOS input level
- Fully static operation
- Automatic power down ($\overline{CE}$)
- Complete TTL compatibility
- 3-state outputs for wired-OR expansion
- EPROMs accepted as program data input
- Ultra low data retention supply

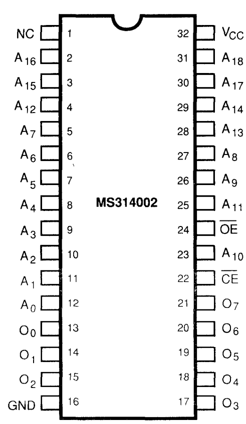
DESCRIPTION

The MS314002 high performance Read Only Memory is organized as 524,288 bytes by 8 bits. It is designed to be compatible with all microprocessors and similar applications where high performance, low cost, mass storage and simple interfacing are important design considerations.

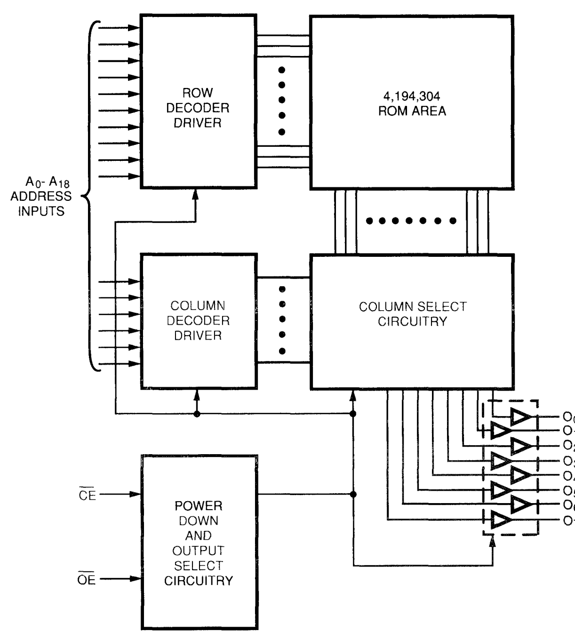
The MS314002 offer automatic powerdown with powerdown controlled by the Chip Enable ($\overline{CE}$) inputs. When $\overline{CE}$ goes LOW the device will automatically power down and remain in a low power standby mode as long as $\overline{CE}$ remains LOW.

4

PIN CONFIGURATIONS



BLOCK DIAGRAM



PIN DESCRIPTIONS

PIN NO.	SYMBOL	FUNCTION
2-12, 23, 25-31	$A_0 - A_{18}$	Address Input
13-15, 17-21	$O_0 - O_7$	Data Output
16	GND	Ground
32	V_{CC}	Power Supply
1	NC	No Connection
22	$\overline{CE}$	Chip Enable
24	$\overline{OE}$	Output Enable

ABSOLUTE MAXIMUM RATINGS(1)

Temperature Under Bias	–10°C to +85°C
Storage Temperature	–45°C to +125°C
Supply Voltage to Ground Potential	–0.5V to +7.0V
Applied Output Voltage	–0.5V to V_{CC} + 0.5
Applied Input Voltage	–0.5V to V_{CC} + 0.5
Power Dissipation	220 mW

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not recommended. Exposure to ABSOLUTE MAXIMUM RATINGS for extended periods may affect device reliability.

OPERATING RANGE

RANGE	AMBIENT TEMPERATURE	Vcc
Commercial	0°C to + 70°C	5V ± 10%

DC ELECTRICAL CHARACTERISTICS (over the commercial operating range)

PARAMETER NAME	PARAMETER	TEST CONDITIONS	MS314002 MIN.	TYP.	MAX.	UNITS
V_{IL}	Input Low Voltage		–0.3	-	0.8	V
V_{IH}	Input High Voltage		2.2		V_{CC}+ 0.3	V
I_{IL}	Input Leakage Current	V_{IN}=0V to V_{CC}	-	-	10	µA
I_{OL}	Output Leakage Current	$\overline{CE}=V_{IH}$, $\overline{OE}=V_{IH}$	–10	-	10	µA
V_{OL}	Output Low Voltage	2.1mA	-	-	0.4	V
V_{OH}	Output High Voltage	I_{OH}=–400µA	2.4	-	-	V
I_{CC}	Operating Power Supply Current (1)		-	-	40	mA
I_{CCSB}	Standby Power Supply Current	$\overline{CE}=V_{IH}$	-	-	1	mA
I_{CCSB1}	Super Standby Power Supply Current	$\overline{CE}=V_{CC}$–0.2V, V_{IH}, GND	-	-	50	µA
I_{OS}	Output Short Circuit Current (2)		-	-	50	mA

1. Measured with device selected and outputs unloaded.
2. For a duration not to exceed 30 seconds.

CAPACITANCE (Ta=25°C, f=1.0MHz)(1)

SYMBOL	PARAMETER	CONDITION	MAX.	UNIT
CI	Input Capacitance	V_{IN}= 0V	10	pF
CO	Output Capacitance	V_{OUT}= 0V	15	pF

1. This parameter is guaranteed but not 100% tested.

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	MODE	OUTPUT	POWER DISSIPATION MODE
L	L	Selected	Output Data	Active
L	H	Not Selected	High-Z	Active
H	X	Not Selected	High-Z	Standby

AC TEST CONDITIONS

Input Pulse Levels	0.6 to 2.4V
Input Rise and Fall Times	t_R = 5 ns
Timing Measurement Level	V_{IL} = 0.8V V_{IH} = 2.2V
Reference	V_{OL} = 0.8V V_{OH} = 2.0V
Output Load	See Figure 1

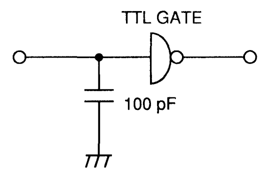


Figure 1. Output Load Circuit

4

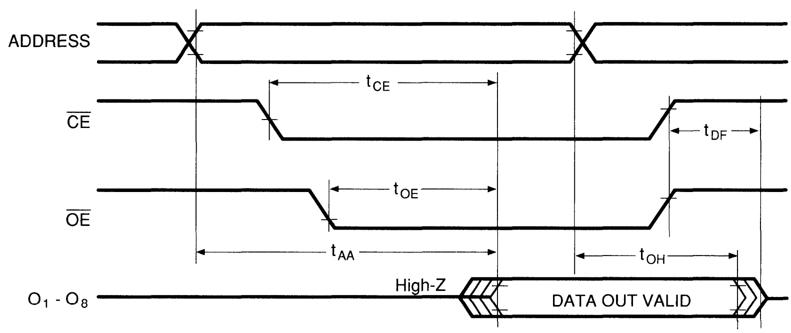
AC ELECTRICAL CHARACTERISTICS (over the operating range)

PARAMETER NAME	PARAMETER	TEST CONDITION	MS314002–25 MIN.	MAX.	UNIT
t_{AA}	Chip Access Time	$\overline{CE} = \overline{OE} = V_{IL}$	-	200	ns
t_{CE}	Chip Enable Access Time	$\overline{OE} = V_{IL}$	-	200	ns
t_{OE}	Output Enable Access Time	Note 1	-	80	ns
t_{OH}	Output Disable	$\overline{CE} = \overline{OE} = V_{IL}$	0	60	ns
t_{DF}	Output Hold After Address Change	Note 2	-		ns

Note 1: Maximum $\overline{OE}$ delay which does not affect t_{AA} is $t_{AA}-t_{OE}$

Note 2: t_{DF} is specified by either of $\overline{CE}$ or $\overline{OE}$ changing to HIGH earlier.

TIMING DIAGRAMS



ORDERING INFORMATION

SPEED (ns)	ORDERING PART NUMBER	PACKAGE REFERENCE NO.	TEMPERATURE RANGE
200	MS314002-20 PC	P32-2	0°C to + 70°C

MOSEL

MS314003

ADVANCE INFORMATION

256K X 16, 512K X 8 CMOS Mask Programmable ROM

FEATURES

- Two organizations selectable by $\overline{\text{BYTE}}$ pin
  262,144 words x 16 bits
  524,288 words x 8 bits
- Access time: 150ns
- Low Power operation:
  275mW max. Operating
  5.5mW max. Standby, TTL input level
  275µW max. Standby, CMOS input level
- Fully static operation
- Automatic power down (CE/CE)
- Complete TTL compatibility
- 3-state outputs for wired-OR expansion
- Single 5V power supply
- Standard 40-pin Plastic DIP
- 64-pin Plastic Flat package

DESCRIPTION

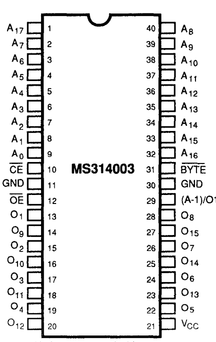
The MS314003 is a CMOS SI-gate mask-programmable static read only memory organized as 262,144 words by 16 bits. (524,288 words by 8 bits).

The MS314003 has TTL-compatible I/O 3-state output level with fully-static operation (i.e. no need of clock signal) and single +5V power supply. Also, the MB834200 is designed for applications such as character generator or program storage which require large memory capacity and high-speed/low-power operation.

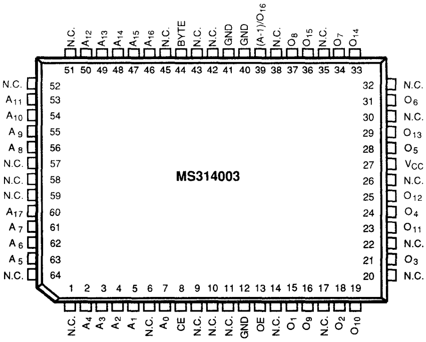
Memory organization of MS314003 is changeable between 16 bits and 8 bits. (ex. The system using 8 bits CPU and 16 bits CPU can use common data on the same chip.)

4

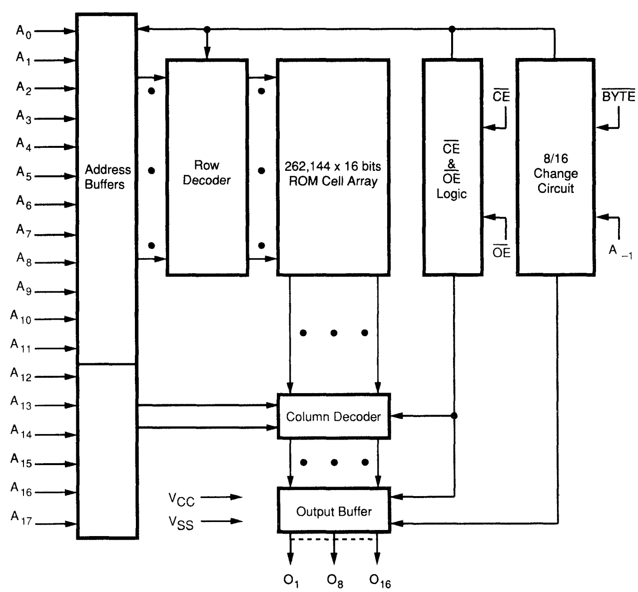
PIN CONFIGURATIONS



( ) shows a case of 8 bit outputs



BLOCK DIAGRAM



MOSEL Corporation 914 West Maude Avenue, Sunnyvale, CA 94086 U.S.A 408-733-4556

PIN DESCRIPTIONS

SYMBOL	FUNCTION
A_0 - A_{18}	Address Input
O_0 - O_{16}	Data Output
GND	Ground
V_{CC}	Power Supply
NC	No Connection
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{BYTE}$	Selects 16 or 8 bit Data Out

ABSOLUTE MAXIMUM RATINGS(1)

Temperature Under Bias	–10°C to +80°C
Storage Temperature	–65°C to +150°C
Supply Voltage to Ground Potential	–0.5V to +7.0V
Applied Output Voltage	–0.5V to +7.0V
Applied Input Voltage	–0.5V to +7.0V
Power Dissipation	275mW

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not recommended. Exposure to ABSOLUTE MAXIMUM RATINGS for extended periods may affect device reliability.

OPERATING RANGE

RANGE	AMBIENT TEMPERATURE	Vcc
Commercial	0°C to + 70°C	5V ± 10%

DC ELECTRICAL CHARACTERISTICS (over the commercial operating range)

PARAMETER NAME	PARAMETER	TEST CONDITIONS	MS314003 MIN.	TYP.	MAX.	UNITS
V_{IL}	Input Low Voltage		–0.5	-	0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC}+ 0.3	V
I_{IL}	Input Leakage Current	V_{IN}=0V to V_{CC}	-	-	10	µA
I_{OL}	Output Leakage Current	$\overline{CE}=V_{IH}$, $\overline{OE}=V_{IH}$	–10	-	10	µA
V_{OL}	Output Low Voltage	I_{OL}=2.1mA	-	-	0.4	V
V_{OH}	Output High Voltage	I_{OH}=–400µA	2.4	-	-	V
I_{CC}	Operating Power Supply Current (1)		-	-	50	mA
I_{CCSB}	Standby Power Supply Current	$\overline{CE}=V_{IH}$	-	-	3	mA
I_{CCSB1}	Super Standby Power Supply Current	$\overline{CE}=V_{CC}-0.2$, V_{IH}, GND	-	-	50	µA
I_{OS}	Output Short Circuit Current (2)		-	-	70	mA

1. Measured with device selected and outputs unloaded.
2. For a duration not to exceed 30 seconds.

CAPACITANCE (Ta=25°C, f=1.0MHz)(1)

SYMBOL	PARAMETER	CONDITION	MAX.	UNIT
CI	Input Capacitance	V_{IN}= 0V	10	pF
CO	OutputCapacitance	V_{OUT}= 0V	15	pF

1. This parameter is guaranteed but not 100% tested.

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	MODE	OUTPUT	POWER DISSIPATION MODE
H	X	Not Selected	High-Z	Standby
L	X	Not Selected	High-Z	Active
L	L	Selected	D_{OUT}	Active

OUTPUT SELECTION MODE

A_{-1}	$\overline{BYTE}$	O_1 to O_8	O_9 to O_{15}	O_{16}
X	H	O_1 to O_8	O_9 to O_{15}	D_{15}
L	L	O_1 to O_8	High-Z	A_{-1}
H	L	O_9 to O_{16}	High-Z	A_{-1}

AC TEST CONDITIONS

Input Pulse Levels	0.6 ~ 2.4V
Input Rise and Fall Times	5 ns
Timing Measurement Level Reference	V_{IL} = 0.8V V_{IH} = 2.2V V_{OL} = 0.8V V_{OH} = 2.0V
Output Load	See Figure 1

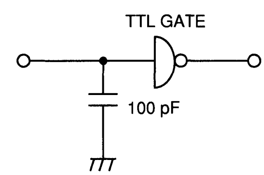


Figure 1. Output Load Circuit

4

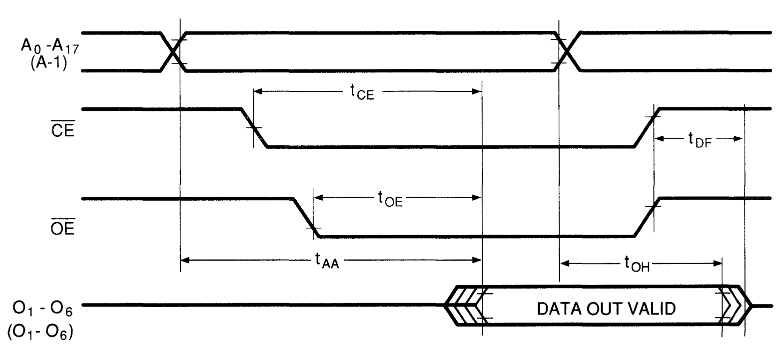
AC ELECTRICAL CHARACTERISTICS (over the operating range)

PARAMETER NAME	PARAMETER	TEST CONDITION	MS314003-25 MIN.	MAX.	UNIT
t_{AA}	Chip Access Time	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	-	250	ns
t_{CE}	Chip Enable Access Time	$\overline{OE}$ = V_{IL}	-	250	ns
t_{OE}	Output Enable Access Time	Note 1	-	100	ns
t_{OH}	Output Hold After Address Change	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0	-	ns
t_{DF}	Output Disable	Note 2	-	60	ns

Note 1: Maximum $\overline{OE}$ delay which does not affect t_{AA} is $t_{AA}-t_{OE}$

Note 2: t_{DF} is specified by either of $\overline{CE}$ or $\overline{OE}$ changing to HIGH earlier.

TIMING DIAGRAMS



( ) shows a case of 8 bit outputs

ORDERING INFORMATION

SPEED (ns)	ORDERING PART NUMBER	PACKAGE REFERENCE NO.	TEMPERATURE RANGE
250	MS314003-25PC	P40-1	0°C to + 70°C
250	MS314003-25QC	Q64-1	0°C to +70°C

MOSEL

MS318002

ADVANCE INFORMATION

1,048,576 X 8 CMOS Mask Programmable ROM 32 Pin DIP

FEATURES

- Access time: 200ns
- Low Power operation:
  - 257mW (Active)
  - 5.5mW Standby TTL levels
  - 275µW Standby CMOS levels
- Fully static operation
- Automatic power down ($\overline{CE}$)
- Complete TTL compatibility
- 3-state outputs for wired-OR expansion
- EPROMs accepted as program data input
- 32 Pin DIP

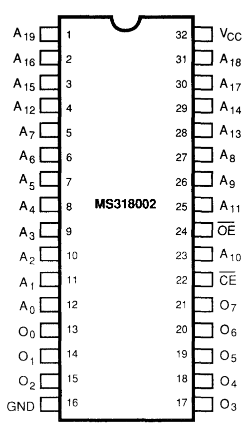
DESCRIPTION

The MS318002 high performance Read Only Memory is organized as 1,048,576 bytes by 8 bits. It is designed to be compatible with all microprocessors and similar applications where high performance, low cost, mass storage and simple interfacing are important design considerations.

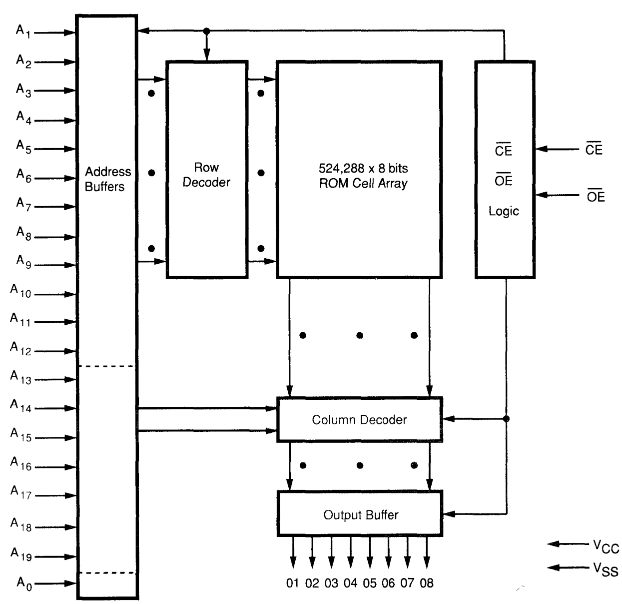
The MS318002 offer automatic powerdown with powerdown controlled by the Chip Enable ($\overline{CE}$) input. When $\overline{CE}$ goes HIGH the device will automatically power down and remain in a low power standby mode as long as $\overline{CE}$ remains HIGH.

4

PIN CONFIGURATIONS



BLOCK DIAGRAM



PIN DESCRIPTIONS

SYMBOL	FUNCTION
A_0 - A_{18}	Address Input
O_0 - O_7	Data Output
GND	Ground
V_{CC}	Power Supply
NC	No Connection
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable

1. This pin is user-definable as active high or active low.
2. N/C is "No Connection".

ABSOLUTE MAXIMUM RATINGS(1)

Temperature Under Bias	–10°C to +85°C
Storage Temperature	–45°C to +125°C
Supply Voltage to Ground Potential	–0.3V to +7.0V
Applied Output Voltage	–0.5V to V_{CC} + 0.5
Applied Input Voltage	–0.5V to V_{CC} + 0.5

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not recommended. Exposure to ABSOLUTE MAXIMUM RATINGS for extended periods may affect device reliability.

OPERATING RANGE

RANGE	AMBIENT TEMPERATURE	Vcc
Commercial	0°C to + 70°C	5V ± 10%

DC ELECTRICAL CHARACTERISTICS (over the commercial operating range)

PARAMETER NAME	PARAMETER	TEST CONDITIONS	MS318002 MIN.	TYP.	MAX.	UNITS
V_{IL}	Input Low Voltage		–0.3	-	0.8	V
V_{IH}	Input High Voltage		2.2		V_{CC}+ 0.3	V
I_{IL}	Input Leakage Current	V_{CC}=Max, V_{IN}=0V to V_{CC}	-	-	10	μA
I_{OL}	Output Leakage Current	V_{OUT}=0 V to V_{DD} , $\overline{CE}$=V_{IH}, $\overline{OE}$ = V_{IH}	-	-	10	μA
V_{OL}	Output Low Voltage	V_{CC}=Min, I_{OL}=2.1mA	-	-	0.4	V
V_{OH}	Output High Voltage	V_{CC}=Min, I_{OH}=–400mA	2.4	-	-	V
I_{CC}	Operating Power Supply Current (1)	$\overline{CE}$=V_{IL}, Minimum Cycle	-	-	50	mA
I_{CCSB}	Standby Power Supply Current	$\overline{CE}$=V_{IH}, CE=V_{IL}	-	-	1	mA
I_{CCSB1}	Super Standby Power Supply Current	$\overline{CE}$=V_{CC}–0.2V, CE = 0.2V	-	-	50	μA

1. Measured with device selected and outputs unloaded.

CAPACITANCE (Ta=25°C, f=1.0MHz)(1)

SYMBOL	PARAMETER	CONDITION	MAX.	UNIT
CI	Input Capacitance	V_{IN} = 0V	10	pF
CO	Output Capacitance	V_{OUT}= 0V	15	pF

1. This parameter is guaranteed but not 100% tested.

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	MODE	OUTPUT	POWER DISSIPATION MODE
H	X	Not Selected	High-Z	Standby
L	H	Not Selected	High-Z	Active
L	L	Selected	Data Out	Active

AC TEST CONDITIONS

Input Pulse Levels	0.6 to 2.4V
Input Rise and Fall Times	5 ns
Timing Measurement Level Reference	V_{IL} = 0.8V V_{IH} = 2.2V V_{OL} = 0.8V V_{OH} = 2.0V
Output Load	1 TTL Gate and 100pF

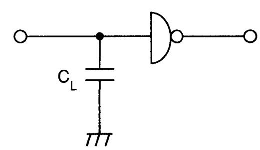


Figure 1. Output Load Circuit

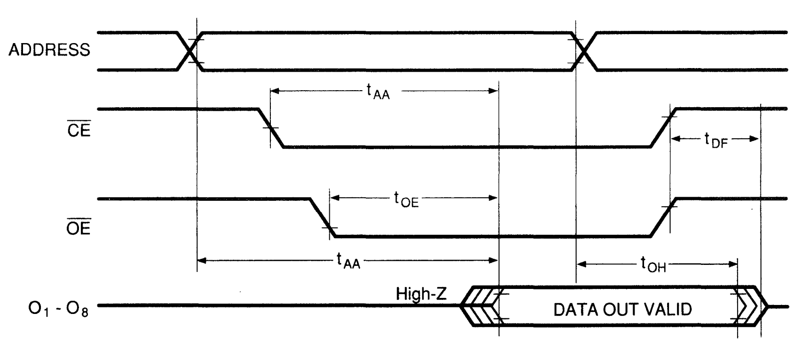
AC ELECTRICAL CHARACTERISTICS (over the operating range)

PARAMETER NAME	PARAMETER	TEST CONDITION	MIN.	MAX.	UNIT
t_{AA}	Address Access Time	$\overline{CE} = \overline{OE} = V_{IL}$	-	200	ns
t_{ACE}	Chip Enable Access Time	$\overline{OE} = V_{IL}$	-	200	ns
t_{OE}	Output Enable Access Time	Note 1	-	80	ns
t_{DF}	Output Disable Time	Note 2	-	80	ns
t_{OH}	Output Hold Time	$\overline{CE} = \overline{OE} = V_{IL}$	0	-	ns

Note 1: Maximum $\overline{OE}$ delay which does not affect t_{ACE} is t_{ACE}–t_{OE}.

Note 2: t_{DP} is specified by either of $\overline{CE}$ or $\overline{OE}$ changing to Hih earlier.

TIMING DIAGRAMS



ORDERING INFORMATION

SPEED (ns)	ORDERING PART NUMBER	PACKAGE REFERENCE NO.	TEMPERATURE RANGE
200	MS318002-20 PC	P32-2	0°C to + 70°C

ADVANCE INFORMATION

512K X 16, 1 MEG X 8 CMOS Mask Programmable ROM

FEATURES

- Access time: 200ns max.
- Low Power dissipation:
  - 275mW max. (Active)
  - 5.5mW max. (Standby, TTL input level)
  - 275μW max. (Standby, CMOS input level)
- Fully static operation, no clock required
- Automatic power down ($\overline{CE}$/CE)
- Complete TTL compatibility
- 3-state outputs for wired-OR expansion
- EPROMs accepted as program data input
- Ultra low data retention supply
- Organization (selectable by $\overline{BYTE}$ pin):
  - 524,288 words x 16 bits
  - 1,048,576 words x 8 bits
- 42 pin PDIP package
- 64 pin Quad Flat package

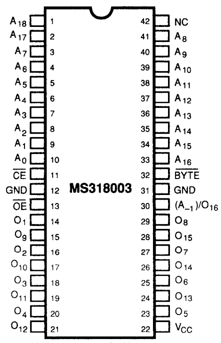
DESCRIPTION

The MOSEL MS318003 is a CMOS SI-gate mask-programmable static read only memory organized as 524,288 words by 16 bits, or 1,048,576 words by 8 bits.

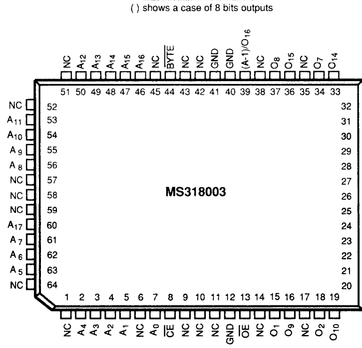
The MS318003 has TTL compatible I/O 3-state output level with full-static operation (i.e. no need of clock signal) and single +5V power supply. Also, the MS318003 is designed for applications such as character generator or program storage which require large memory capacity and high-speed/low-power operation.

Memory output organization of MS318003 is selectable between 16 bits and 8 bits. (ex. The system using 8 bit CPU and 16 bit CPU can use common data from ROM.)

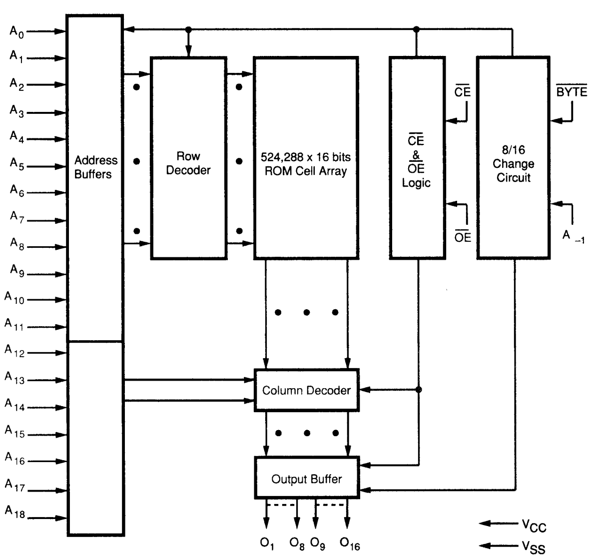
PIN CONFIGURATIONS



( ) shows a case of 8 bits outputs



BLOCK DIAGRAM



MOSEL Corporation 914 West Maude Avenue, Sunnyvale, CA 94086 U.S.A 408-733-4556

PIN DESCRIPTIONS

SYMBOL	FUNCTION
A_0 - A_{18}	Address Input
O_0 - O_{16}	Data Output
GND	Ground
V_{CC}	Power Supply
NC	No Connection
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{BYTE}$	Selects 16 or 8 bit Data Out

ABSOLUTE MAXIMUM RATINGS(1)

Temperature Under Bias	–10°C to +85°C
Storage Temperature	–45°C to +125°C
Supply Voltage to Ground Potential	–0.3V to +7.0V
Applied Output Voltage	–0.5V to V_{CC}+0.5V
Applied Input Voltage	–0.5V to V_{CC}+0.5V
Power Dissipation	275 mW

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not recommended. Exposure to ABSOLUTE MAXIMUM RATINGS for extended periods may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	Vcc
Commercial	0°C to + 70°C	5V ± 10%

DC ELECTRICAL CHARACTERISTICS (over the commercial operating range)

PARAMETER NAME	PARAMETER	TEST CONDITIONS	MS318003 MIN.		MAX.	UNITS
V_{IL}	Input Low Voltage		–0.3	-	0.8	V
V_{IH}	Input High Voltage		2.2		V_{CC}+ 0.3	V
I_{IL}	Input Leakage Current	V_{IN}=0V to V_{CC}	–10	-	10	µA
I_{OL}	Output Leakage Current	CE=V_{IH}, OE=V_{IH}	–10	-	10	µA
V_{OL}	Output Low Voltage	I_{OL}=2.1mA	-	-	0.4	V
V_{OH}	Output High Voltage	I_{OH}=–400µA	2.4	-	-	V
I_{CC}	Operating Power Supply Current (1)		-	-	50	mA
I_{CCSB}	Standby Power Supply Current	$\overline{CE}$=V_{IH}	-	-	1	mA
I_{CCSB1}	Super Standby Power Supply Current	$\overline{CE}$=V_{CC}–0.2, V_{IH}, GND	-	-	50	µA

1. Measured with device selected and outputs unloaded.

CAPACITANCE (Ta=25°C, f=1.0MHz)(1)

SYMBOL	PARAMETER	CONDITION	MAX.	UNIT
CI	Input Capacitance	V_{IN}= 0V	10	pF
CO	Output Capacitance	V_{OUT}= 0V	15	pF

1. This parameter is guaranteed but not 100% tested.

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	MODE	OUTPUT	POWER DISSIPATION MODE
H	X	Not Selected	High-Z	Standby
L	H	Not Selected	High-Z	Active
L	L	Selected	D_{OUT}	Active

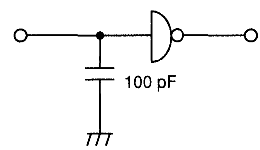
OUTPUT SELECTION MODE

A_{-1}	$\overline{BYTE}$	O_1 to O_8	O_9 to O_{15}	O_{16}
X	H	O_1 to O_8	O_9 to O_{15}	D_{15}
L	L	O_1 to O_8	High-Z	A_{-1}
H	L	O_9 to O_{16}	High-Z	A_{-1}

AC TEST CONDITIONS

Input Pulse Levels	0.6 ~ 2.4V
Input Rise and Fall Times	t_R = 5 ns
Timing Measurement Level	V_{IL} = 0.8V V_{IH} = 2.2V
Reference	V_{OL} = 0.8V V_{OH} = 2.0V

* Output Load



4

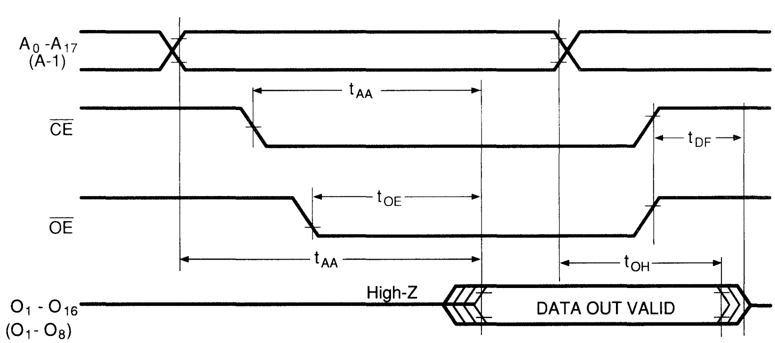
AC ELECTRICAL CHARACTERISTICS (over the operating range)

PARAMETER NAME	PARAMETER	TEST CONDITION	MS318003-20 MIN.	MAX.	UNIT
t_{AA}	Chip Access Time	$\overline{CE} = \overline{OE} = V_{IL}$	-	200	ns
t_{ACE}	Chip Enable Access Time	$\overline{OE} = V_{IL}$	-	200	ns
t_{OE}	Output Enable Access Time	Note 1	-	80	ns
t_{OH}	Output Hold After Address Change	$\overline{CE} = \overline{OE} = V_{IL}$	0	-	ns
t_{DF}	Output Disable	Note 2	-	60	ns

Note 1: Maximum $\overline{OE}$ delay which does not affect t_{AA} is $t_{AA}-t_{OE}$

Note 2: t_{DF} is specified by either of $\overline{CE}$ or $\overline{OE}$ changing to HIGH earlier.

TIMING DIAGRAMS



( ) shows a case of 8 bit outputs

ORDERING INFORMATION

SPEED (ns)	ORDERING PART NUMBER	PACKAGE REFERENCE NO.	TEMPERATURE RANGE
200	MS318003-20PC	P42-1	0°C to + 70°C
200	MS318003-20QC	Q64-1	0°C to +70°C

General Information

ROMs (Read Only Memory)

Voice ROMs 5

Cache Products

MOSEL Sales Network

VOICE ROM

MOSEL's Voice Rom products are a CMOS VLSI solution to PCM speech synthesis. A wide variety of speech lengths and controls offer a choice of unit price and complexity as well as speech duration. PCM sound allows all types of audio signals to be frozen in a solid-state ROM memory.

Voice, animal sounds, noises, machine sounds, music and lyrics are all producible with this technology. With the addition of a battery, a switch mechanism and a speaker or buzzer, the sound unit can be placed in a toy, gift, book or magazine, electronic clock, thermostat, or any compact electronic module.

These CMOS devices work on voltages down to 2 volts, shut down automatically after the programmed sound terminates and can be made to repeat, mute, and restart using metal mask options on most of the control inputs.

The family members now allow durations of 1.5 seconds to 20 seconds. A new 28 second device will be available in 2nd half of 1990.

MOSEL supports the Voice Rom product by converting the customer's sound to EPROM data, demonstrates digitized sound, makes 15 samples of the actual VLSI device for evaluation and starts chip production to meet a customer' s critical delivery schedule. MOSEL will also assume prime contractor status to manage the assembly of modules containing the speech chip for the most economical and reliable solution.

Speech Synthesizer (Voice ROM)

FEATURES

- Single power can operate at 2.4V through 5V.
- Direct drive buzzer and one current output to drive speaker.
- Total maximum duration is 1.5/2.8 seconds, speech + mute is about 6 seconds.
- Automatic power down.
- Repeat function that can repeat up to 8 times.
- Cascade function that can extend the speech duration by 2.8 x n seconds with n pieces of MSS0281.
- Bonding option for edge trigger (CDS photo-resistor application) or level trigger.

DESCRIPTION

The MSS0281 is a single-chip speech synthesizing CMOS VLSI that can synthesize voice and other sounds up to 2.8 seconds. The chip contains most of the necessary circuitry such as the RC oscillator, ROM, D/A, buzzer buffer, control and timing logic. Sound generation is possible with a minimum of external components. Several chips can be cascaded to reach longer voice duration (longer than 1.5/2.8 seconds). Customer speech data will be edited and programmed into ROM by changing only one mask during the device fabrication. MOSEL provides sound analysis, digitizing and editing from customer provided audio tapes.

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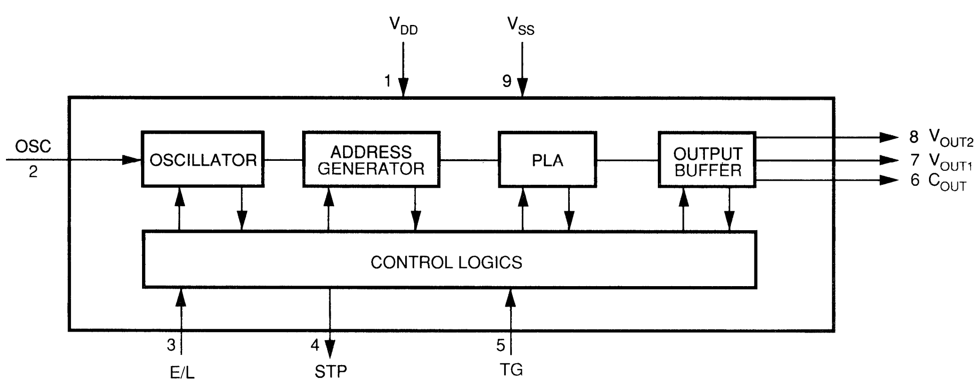
BLOCK DIAGRAM



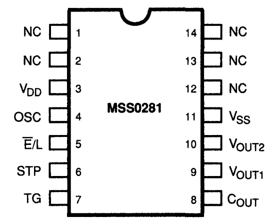
MOSEL Corporation 2 FL., No. 9, Industrial E. IV. Rd., Science-Based Industrial Park, Hsinchu, Taiwan (035) 773-187
914 West Maude Avenue, Sunnyvale, CA 94086 U.S.A 408-733-4556

PIN DESCRIPTIONS (DIE BONDING PADS)

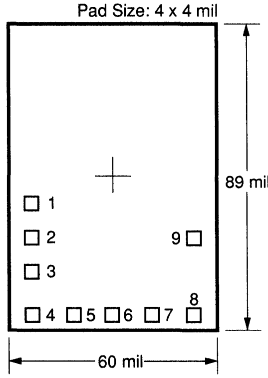
PIN NO.	SYMBOL	FUNCTION
1	V_{DD}	Positive power supply
2	OSC	RC oscillator input
3	E/L	Open, edge trigger; pull high, level trigger
4	STP/TST	One-shot stop signal output/Test mode, active high; (for production test only)
5	TG	Trigger input, active high
6	C_{OUT}	Current output for driving speaker
7	V_{OUT1}	Speech signal voltage output (for buzzer)
8	V_{OUT2}	Speech signal voltage output (for buzzer)
9	V_{SS}	Negative power supply

Note: Substrate is V_{DD}

PIN CONFIGURATION



BONDING DIAGRAM



1. V_{DD} (–575 , –299.7)
2. OSC (–575 –497.7)
3. E/L (–575 , –738)
4. STP (–548 , –936)
5. TG (–275.5, –936)
6. C_{OUT} (12.2, –936)
7. V_{OUT1} (272 , –936)
8. V_{OUT2} (548 , –936)
9. V_{SS} (575 , –481.5)

Note: Substrate is V_{DD} Unit: µM

ABSOLUTE MAXIMUM RATINGS

SYMBOL	RATING	UNITS
V_{DD} - V_{SS}	–0.5 ~ +7.0	V
V_{IN} (TG - E/L)	V_{SS}–0.3 < V_{IN} < V_{DD}+0.3	V
V_{OUT} (STP)	V_{SS} < V_{OUT} < V_{DD}	V
T(Operating)	–10 ~ +60	°C
T(Storage)	–55 ~ +125	°C

DC ELECTRICAL CHARACTERISTICS

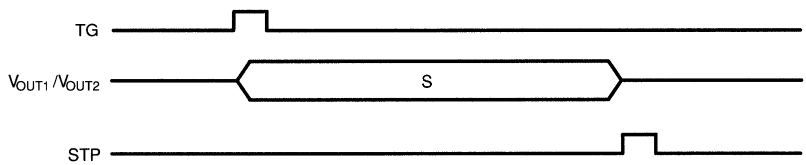
PARAMETER NAME	PARAMETER		TEST CONDITIONS	MSS0151/0281 MIN.	TYP.	MAX.	UNITS
V_{DD}	Operating Voltage			2.4	4.5	5	V
I_{SB}	Supply Current	Stand by	V_{DD} = 4.5V	-	-	0.1	μA
I_{OP}		Operating	I/O Open	-	-	70	
V_{IH}	Input Voltage (TG)		V_{DD} = 4.5V	4	4.5	5	V
V_{IL}				–0.3	0	0.3	
I_{IH}	Input Current (TG)		V_{DD} = 4.5V	-	-	5	μA
I_{IL}				-	0	-	
I_{IH}	Input Current (E/L)		V_{DD} = 4.5V	-	-	10	μA
I_{IL}				-	0	-	
I_{OH}	O/P Current (V_{OUT1}, V_{OUT2})	Drive	V_{DD} = 4.5V, $V_{O/P}$ = 4V	-	–5	-	mA
I_{OL}		Sink	V_{DD} = 4.5V, $V_{O/P}$ = 0.5V	-	5	-	
I_{OH}	Output Current (STP)		V_{DD} = 4.5V, $V_{O/P}$ = 4V	-	–1	-	mA
I_{OL}			V_{DD} = 4.5V, $V_{O/P}$ = 0.5V	-	1	-	
T_{STP}	Pulse Width (STP)		V_{DD} = 4.5V	-	-	5	μS
I_{CO}	Output Current (C_{OUT})		V_{DD} = 4.5V	-	–1	-	mA
ΔF/F	Frequency Stability		$\frac{F_{OSC}(4.5V) - F_{OSC}(4V)}{F_{OSC}(4.5V)}$	-	-	5	%
ΔF/F	Frequency Variation		V_{DD} = 4.5V, R_{OSC} = 1.2MΩ	-	-	15	%

5

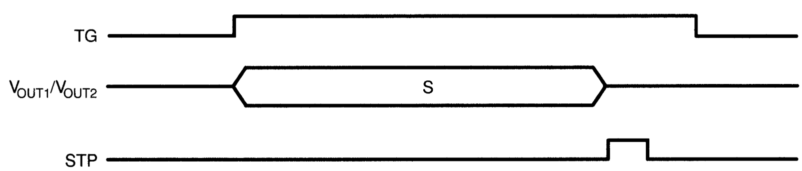
TIMING WAVEFORMS

I. Edge Mode

1. Edge trigger

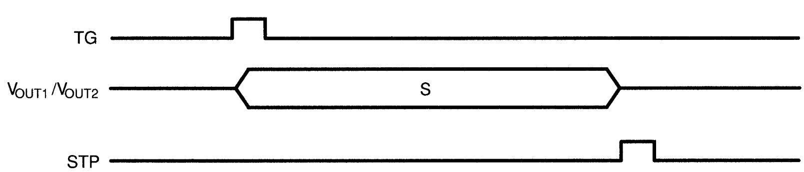


2. Level trigger

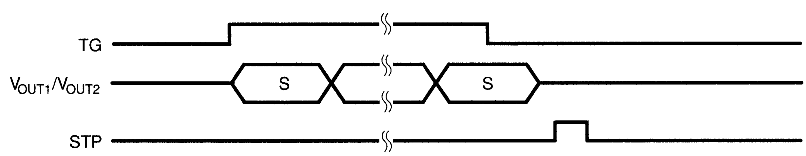


II. Level Mode

1. Edge trigger

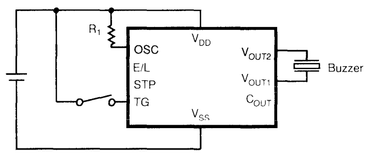


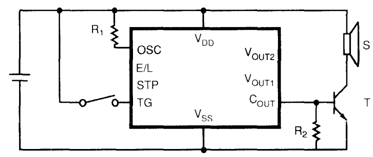
2. Level trigger



APPLICATION CIRCUITS

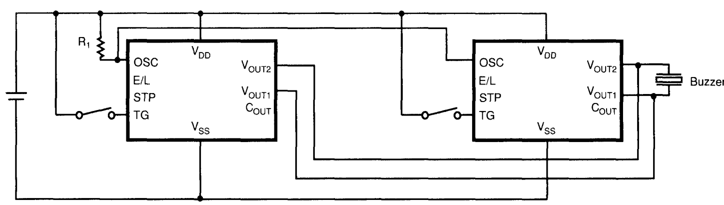
1. Typical application

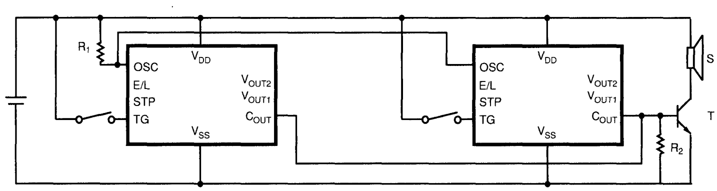




2. Parallel application

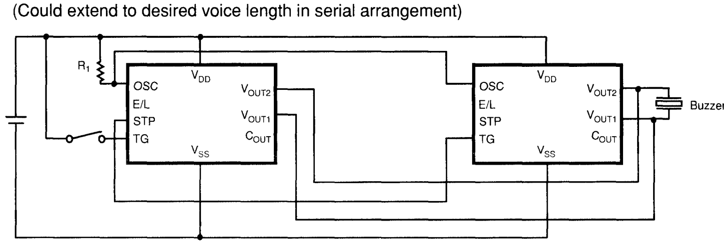
(Could extend up to desired voice sections in parallel arrangement)

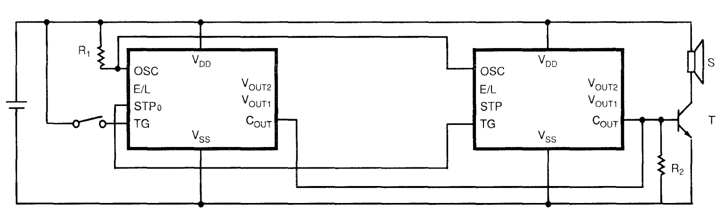




3. *Cascade application*

(Could extend to desired voice length in serial arrangement)





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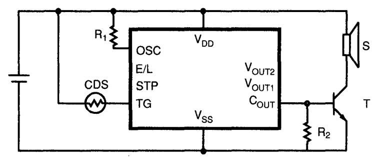
APPLICATION CIRCUITS

4. CDS Application



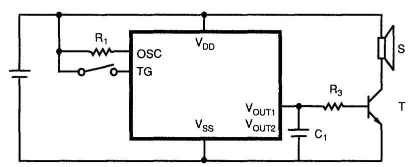
Notes:

a. R1 (resistor) = 1.2MΩ, R2 = 470Ω, T (transistor) = ß > 150, S (speaker) = 1/4W, 8Ω, CDS = Resistance variaton range (50K to 1.5M); all typical.

b. Piezzo buzzer resonant frequency is around 1KHz.

c. It is recommended to add a capacitor (0.1µf typical) between trigger pad and ground for noise immunity purpose.

5. Use V_{OUT1} to drive speaker.



Note:

R3 = 1K typical, C1 = 0.1µf typical.

Speech Synthesizer (Voice ROM)

FEATURES

- Single power supply can operate at 2.4V through 5V.
- 3 seconds speech duration that can be separated into 4 sections.
- Duration of the 4 sections can be different and the total maximum duration is about 3 seconds.
- Automatic power down.
- Repeat function that can repeat up to 16 times for each selected section.
- Cascade function that can extend the speech duration by 3 x n seconds with n pieces of MSS0301.
- Mask option for edge trigger (CDS photo-Resistor Application) or level trigger.

DESCRIPTION

The MSS0301 is a single-chip speech synthesizing CMOS VLSI that can synthesize voice and other sounds up to 3 seconds. The chip contains most of the necessary circuit such as the RC oscillator, ROM, D/A , buzzer buffer, control and timing logic. Sound generation is possible with a minimum of external components. Several chips can be cascaded to reach longer voice duration (longer than 3 seconds). Customer speech data will be edited and programmed into ROM by changing only one mask during the device fabrication. MOSEL provides sound analysis, digitizing and editing from customer provided audio tapes.

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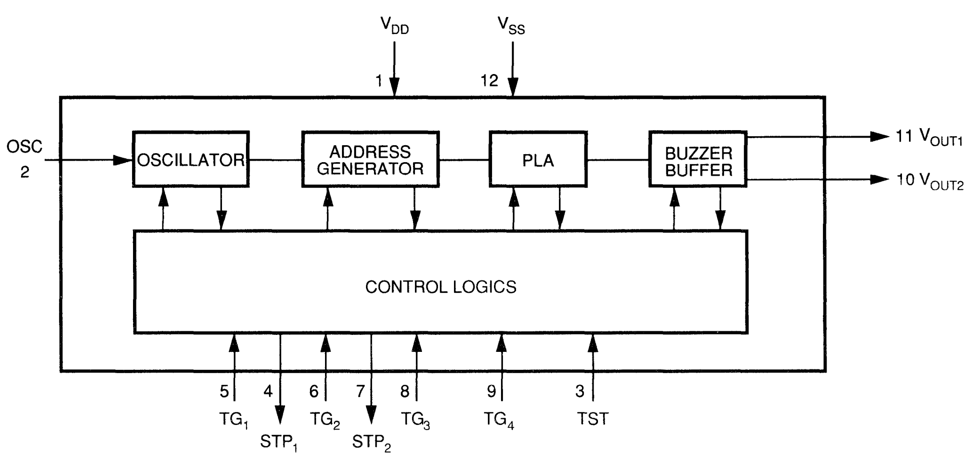
BLOCK DIAGRAM



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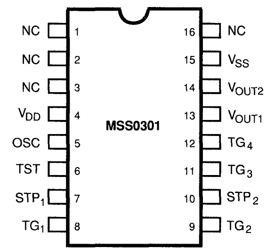
PIN DESCRIPTIONS

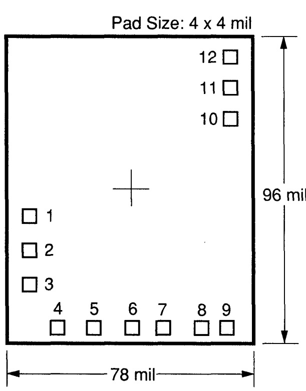
PIN NO.	SYMBOL	FUNCTION
1	V_{DD}	Positive power supply
2	OSC	RC oscillator input
3	TST	Test mode for production test only
4	STP_1	Section 1 one-shot stop signal output
5	TG_1	Section 1 trigger input, active high
6	TG_2	Section 2 trigger input, active high
7	STP_2	Section 2 one-shot stop signal output
8	TG_3	Section 3 trigger input, active high
9	TG_4	Section 4 trigger input, active high
10	V_{OUT1}	Speech signal voltage output (for buzzer)
11	V_{OUT2}	Speech signal voltage output (for buzzer)
12	V_{SS}	Negative power supply

Note: Substrate is V_{DD}

PIN CONFIGURATION



BONDING DIAGRAM



1. V_{DD} (–838.6, –145.3)
2. OSC (–766.1, –478.5)
3. TST (–766.1, –766.3)
4. STP_1 (–589.0, –1020.6)
5. TG_1 (–304.0, –1011.2)
6. TG_2 (–16.2, –1011.2)
7. STP_2 (–266.4, –1020.6)
8. TG_3 (472.3, –1011.2)
9. TG_4 (760.1, –1011.2)
10. V_{OUT1} (781.4, –430.3)
11. V_{OUT2} (781.4, –733.4)
12. V_{SS} (765.7, 1002.5)

Note: Substrate is V_{DD} Unit: μM

ABSOLUTE MAXIMUM RATINGS

SYMBOL	RATING	UNITS
$V_{DD} - V_{SS}$	$-0.5 \sim +0.7$	V
V_{IN} ($TG_1 \sim TG_4$)	$V_{SS}-0.3 < V_{IN} < V_{DD}+0.3$	V
V_{OUT} ($STP_1 \sim STP_2$)	$V_{SS} < V_{OUT} < V_{DD}$	V
T(Operating)	$-10 \sim +60$	°C
T(Storage)	$-55 \sim +125$	°C

DC ELECTRICAL CHARACTERISTICS

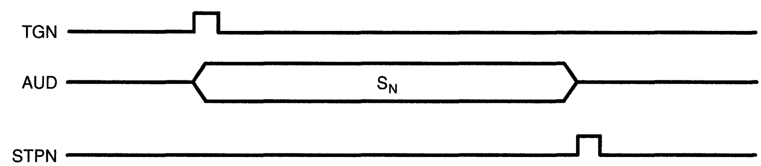
PARAMETER NAME	PARAMETER		TEST CONDITIONS	MSS0301 MIN.	TYP.	MAX.	UNITS
V_{DD}	Operating Voltage			2.4	4.5	5	V
I_{SB}	Supply Current	Stand by	$V_{DD} = 4.5V$	-	-	0.1	μA
I_{OP}		Operating	I/O Open	-	-	70	
V_{IH}	Input Voltage ($TG_1 \sim TG_4$)		$V_{DD} = 4.5$	4	4.5	5	V
V_{IL}				-0.3	0	0.3	
I_{IH}	Input Current ($TG_1 \sim TG_4$)		$V_{DD} = 4.5$	-	-	5	μA
I_{IL}				-	0	-	
I_{OH}	O/P Current V_{OUT1}, V_{OUT2}	Drive	$V_{DD} = 4.5V$, $V_{O/P} = 4V$	-	-5	-	mA
I_{OL}		Sink	$V_{DD} = 4.5V$, $V_{O/P} = 0.5V$	-	5	-	
I_{OH}	Output Current $STP_1 \sim STP_2$		$V_{DD} = 4.5V$, $V_{O/P} = 4V$	-	-1	-	mA
I_{OL}			$V_{DD} = 4.5V$, $V_{O/P} = 0.5V$	-	1	-	
T_{STP}	STP_1, STP_2 Pulse Width		$V_{DD} = 4.5V$	-	-	5	μS
$\Delta F/F$	Frequency Stability		$\frac{F_{OSC}(4.5V)-F_{OSC}(4V)}{F_{OSC}(4.5V)}$	-	-	5	%
$\Delta F/F$	Frequency Variation		$V_{DD} = 4.5V$, $R_{OSC} = 1.2M\Omega$	-	-	15	%

TIMING WAVEFORMS

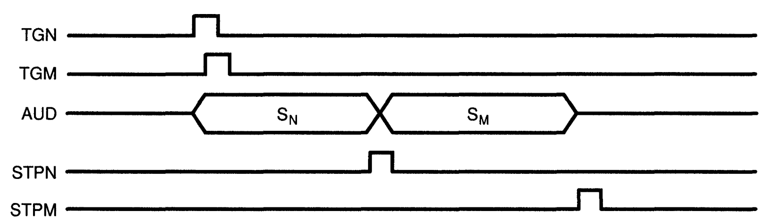
I. Edge Mode

1. Edge trigger

a.

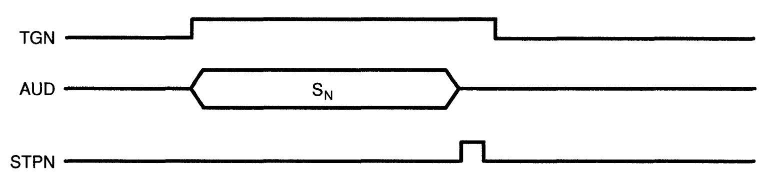


b.

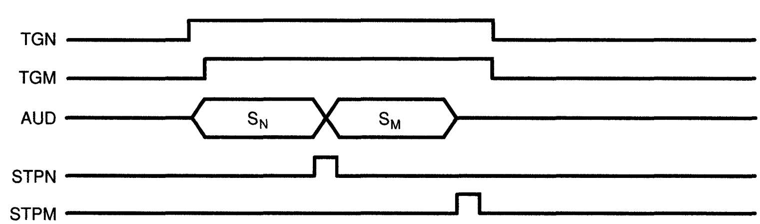


2. Level trigger

a.



b.

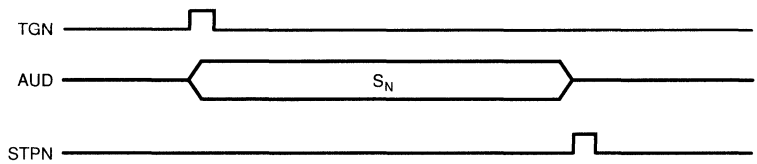


TIMING WAVEFORMS

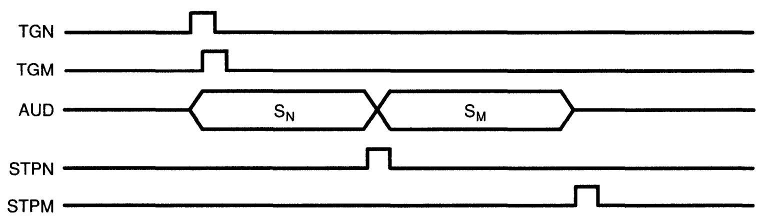
II. Level Mode

1. Edge trigger

a.

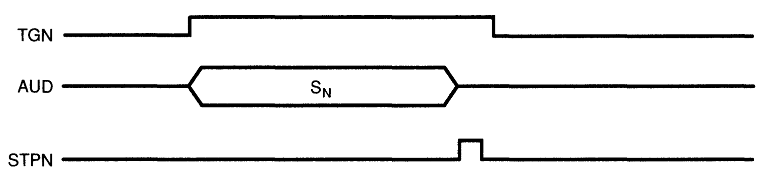


b.

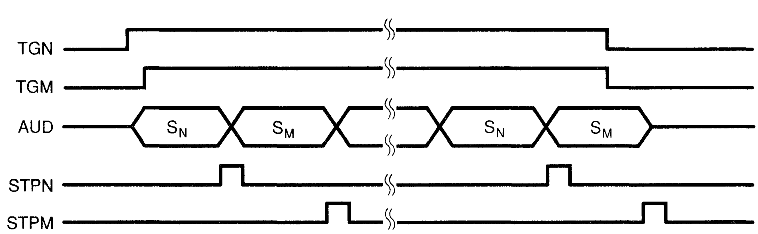


2. Level trigger

a.



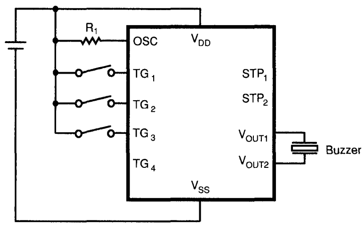
b.

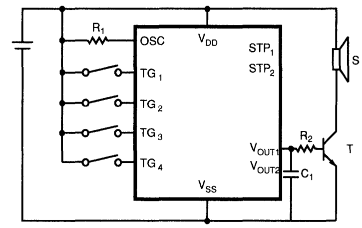


Notes:
a. TGN and TGM could be any one of TG_1 ~ TG_4.
b. AUD is the speech signal output V_{OUT1}, V_{OUT2}.
c. STPN and STPM could be any one of STP_1 or STP_2.

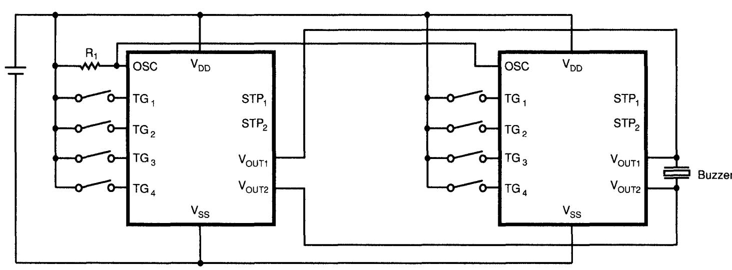
APPLICATION CIRCUITS

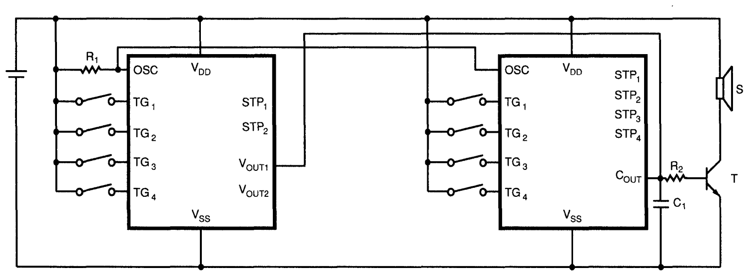
1. **Typical application**





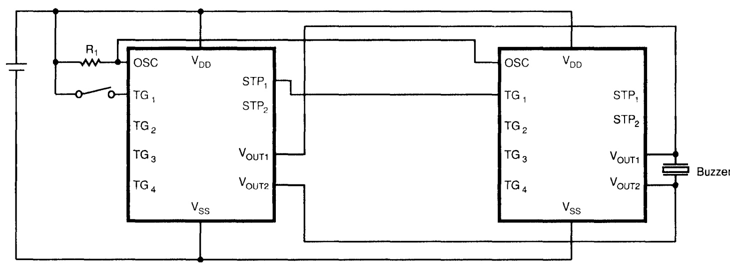
2. **Parallel application**
(Could extend up to desired voice sections in parallel arrangement)

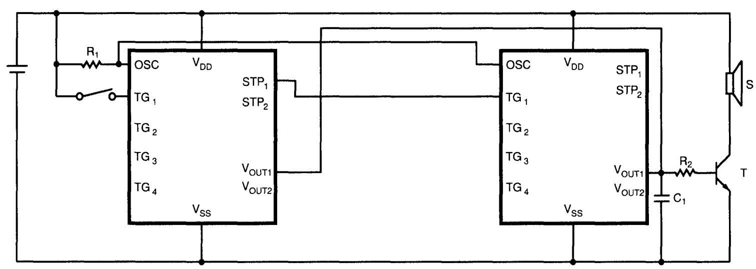




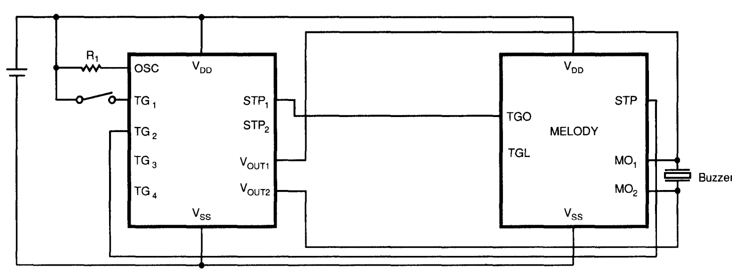
APPLICATION CIRCUITS

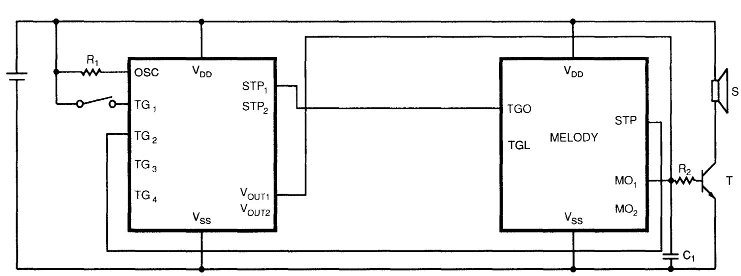
3. Cascade application
(Could extend to desired voice length in serial arrangement)





4. Speech with melody application
(Interface with melody IC could have desired voice/melody system)

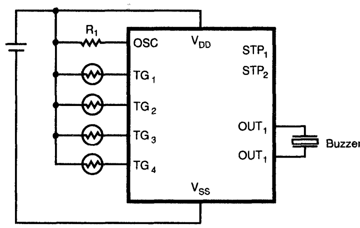


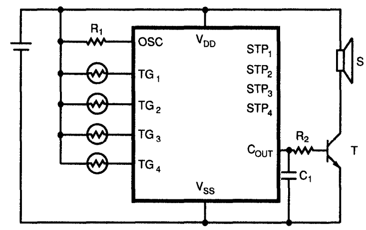


Note: For some melody IC which needs longer pulse to trigger, a delay circuit is needed.

APPLICATION CIRCUITS

5. CDS Application





Notes:

a. R1 = 1.2MΩ, R2 = 1KΩ, C1 = 0.1µf, T (transistor) = ß > 150, S (speaker) = 1/4W, 8Ω, all typical.

b. In the melody cascade application, melody I.C. must have tristate output.

c. Piezzo buzzer resonant frequency is around 1KHz.

d. It is recommended to bond all the unused trigger pad to ground and add a capacitor (0.1µf typical) between used trigger pad and ground for noise immunity purpose.

Speech Synthesizer (Voice ROM)

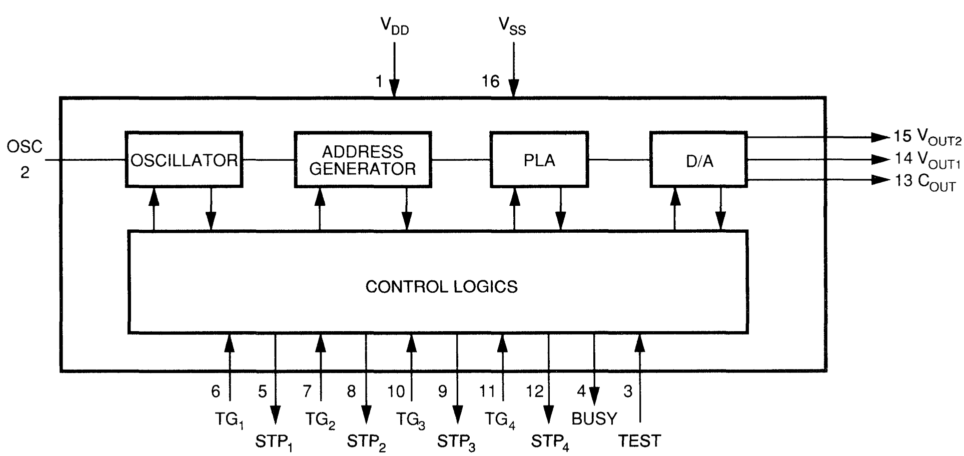
FEATURES

- Single power supply can operate at 2.4V through 5V.
- Direct drive buzzer and one current output to drive speaker.
- 6 seconds speech duration that can be separated into 4 sections.
- Duration of the 4 sections that can be different and the total maximum duration is about 6 seconds.
- Automatic power down.
- Repeat function that can repeat up to 16 times for each selected section.
- Cascade function that can extend the speech duration by 6 x n seconds with n pieces of MSS0601.
- Mask option for edge trigger (CDS photo-Resistor Application) or level trigger.
- BUSY signal indicates that the device is operating.

DESCRIPTION

The MSS0601 is a single-chip speech synthesizing CMOS VLSI that can synthesize voice and other sounds up to 6 seconds. The chip contains most of the necessary circuit such as the RC oscillator, ROM, D/A converter, output buffer control and timing logic. Sound generation is possible with a minimum of external components. Several chips can be cascaded to reach longer voice duration (longer than 6 seconds). Customer speech data will be edited and programmed into ROM by changing only one mask during the device fabrication. MOSEL provides sound analysis, digitizing and editing from customer provided audio tapes.

BLOCK DIAGRAM



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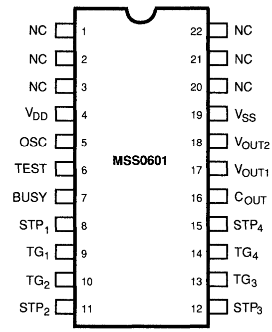
PIN DESCRIPTIONS

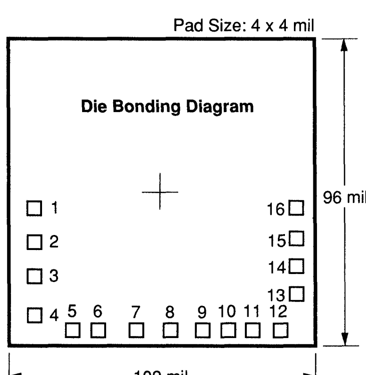
PIN NO.	SYMBOL	FUNCTION
1	V_{DD}	Positive power supply
2	OSC	RC oscillator input
3	TEST	Test mode for production test only
4	BUSY	Active high
5	STP_1	Section 1 one-shot stop signal output
6	TG_1	Section 1 trigger input, active high
7	TG_2	Section 2 trigger input, active high
8	STP_2	Section 2 one-shot stop signal output
9	STP_3	Section 3 one-shot stop signal output
10	TG_3	Section 3 trigger input, active high
11	TG_4	Section 4 trigger input, active high
12	STP_4	Section 4 one-shot stop signal output
13	C_{OUT}	Speech signal current output (for speaker)
14	V_{OUT1}	Speech signal voltage output (for buzzer)
15	V_{OUT2}	Speech signal voltage output (for buzzer)
16	V_{SS}	Negative power supply

Note: Substrate is V_{DD}

PIN CONFIGURATION



BONDING DIAGRAM



1.	V_{DD}	(–1145.7,	–141.4)
2.	OSC	(–1097.4,	–375.6)
3.	TEST	(–1092.2,	–663.4)
4.	BUSY	(–1095.0,	–935.9)
5.	STP_1	(–793.0,	–1020.4)
6.	TG_1	(–586.1,	–1012.5)
7.	TG_2	(–298.3,	–1017.8)
8.	STP_2	(–25.8,	–1020.4)
9.	STP_3	(278.1,	–1020.4)
10.	TG_3	(485.1,	–1012.5)
11.	TG_4	(773.0,	–1017.8)
12.	STP_4	(1045.6,	–1020.4)
13.	C_{OUT}	(1085.4,	–801.4)
14.	V_{OUT1}	(1054.9,	–590.6)
15.	V_{OUT2}	(1054.9,	–382.8)
16.	V_{SS}	(1131.7,	131.3)

Note: Substrate is V_{DD} Unit: µM

ABSOLUTE MAXIMUM RATINGS

SYMBOL	RATING	UNITS
V_{DD} - V_{SS}	–0.5 ~ +0.7	V
V_{IN} (TG_1 ~ TG_4)	V_{SS}–0.3 < V_{IN} < V_{DD}+0.3	V
V_{OUT} (STP_1 ~ STP_4)	V_{SS} < V_{OUT} < V_{DD}	V
T(Operating)	–10 ~ +60	°C
T(Storage)	–55 ~ +125	°C

DC ELECTRICAL CHARACTERISTICS

PARAMETER NAME	PARAMETER		TEST CONDITIONS	MSS0601 MIN.	TYP.	MAX.	UNITS
V_{DD}	Operating Voltage			2.4	4.5	5	V
I_{SB}	Supply Current	Stand by	V_{DD} = 4.5V	-	-	0.1	µA
I_{OP}		Operating	I/O Open	-	-	70	
V_{IH}	Input Voltage (TG_1 ~ TG_4)		V_{DD} = 4.5	4	4.5	4.5	V
V_{IL}				–0.3	0	0.3	
I_{IH}	Input Current (TG_1 ~ TG_4)		V_{DD} = 4.5	-	-	5	µA
I_{IL}				-	0	-	
I_{OH}	O/P Current V_{OUT1}, V_{OUT2}	Drive	V_{DD} = 4.5V, $V_{O/P}$ = 4V	-	–5	-	mA
I_{OL}		Sink	V_{DD} = 4.5V, $V_{O/P}$ = 0.5V	-	5	-	
I_{CO}	Output Current (cout)		V_{DD} = 4.5V	-	–1	-	mA
I_{OH}	Output Current STP_1 ~ STP_4		V_{DD} = 4.5V, $V_{O/P}$ = 4V	-	–1	-	mA
I_{OL}			V_{DD} = 4.5V, $V_{O/P}$ = 0.5V	-	1	-	
T_{STP}	Pulse Width STP_1 ~ STP_4		V_{DD} = 4.5V	-	-	5	µS
ΔF/F	Frequency Stability		$\frac{F_{OSC}(4.5V) - F_{OSC}(4V)}{F_{OSC}(4.5V)}$	-	-	5	%
ΔF/F	Frequency Variation		V_{DD} = 4.5V, R_{OSC} = 1.2MΩ	-	-	15	%

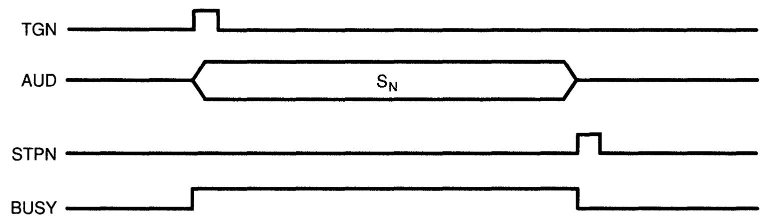
5

TIMING WAVEFORMS

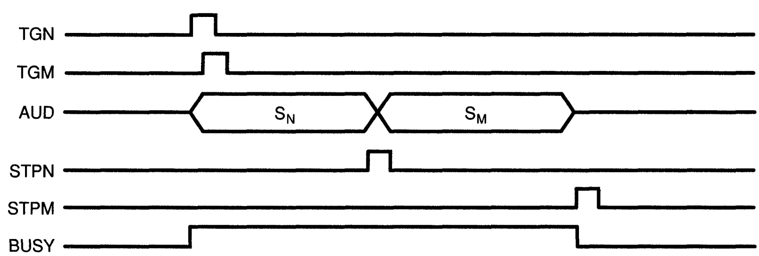
I. Edge Mode

1. Edge trigger

a.

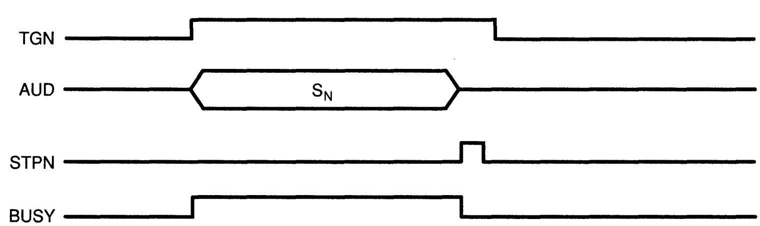


b.

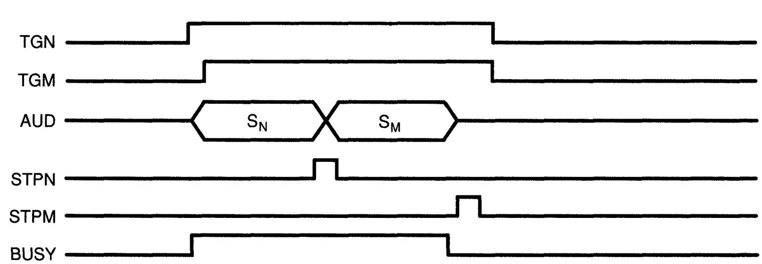


2. Level trigger

a.



b.

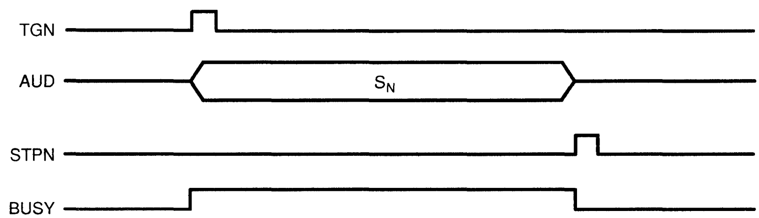


TIMING WAVEFORMS

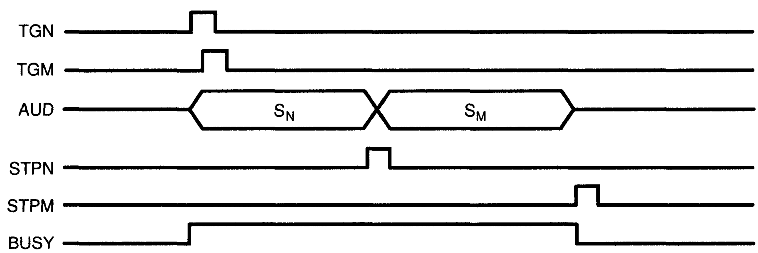
II. Stand-alone Edge Mode

1. Edge trigger

a.

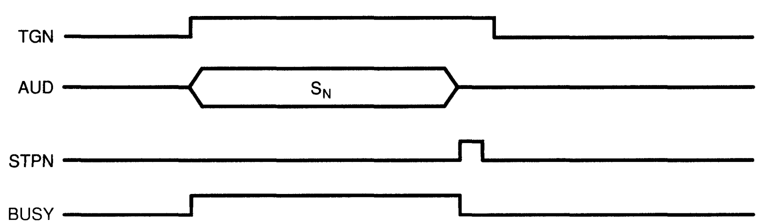


b.

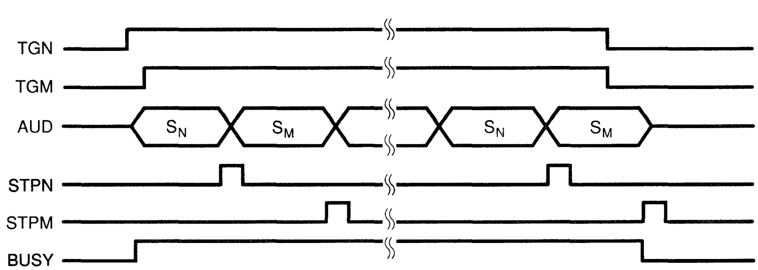


2. Level trigger

a.



b.

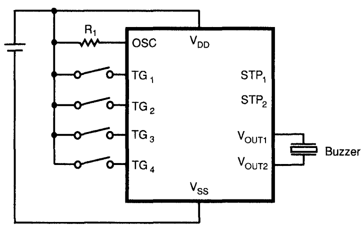


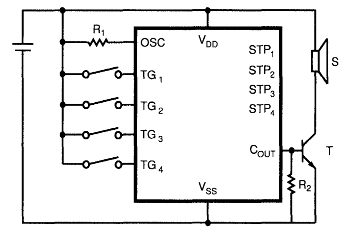
Notes:
a. TGN and TGM could be any one of $TG_1 \sim TG_4$.
b. AUD is the speech signal output V_{OUT1}, V_{OUT2} or C_{OUT}.
c. STPN and STPM could be any one of $STP_1 \sim STP_4$.

5

APPLICATION CIRCUITS

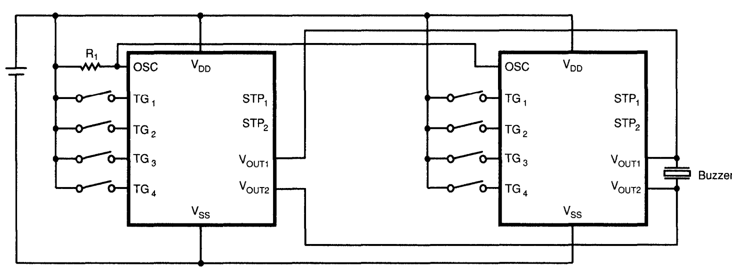
1. Typical application

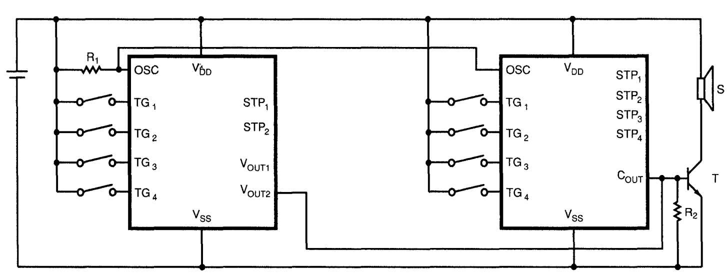




2. Parallel application

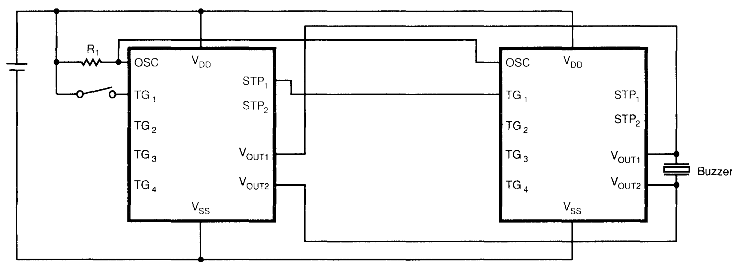
(Could extend up to desired voice sections in parallel arrangement)

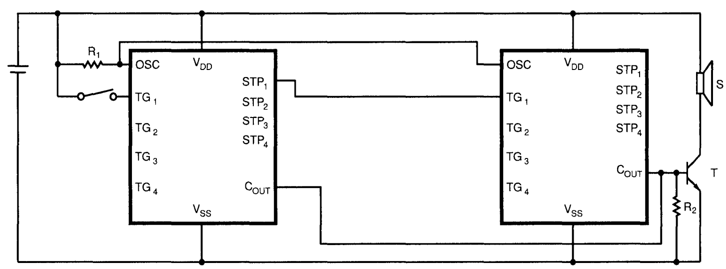




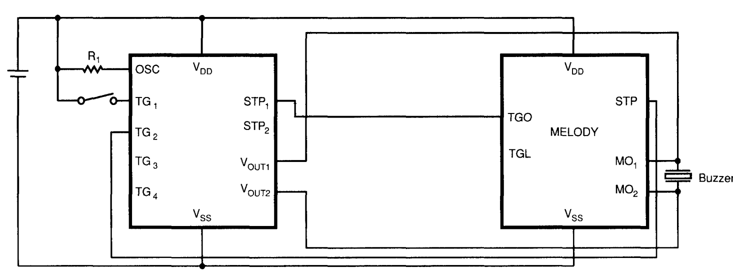
APPLICATION CIRCUITS

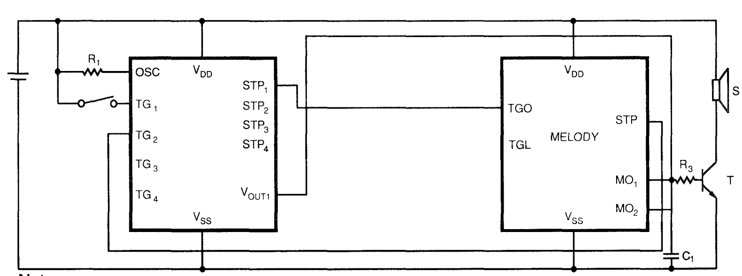
3. Cascade application (for long sentence)
(Could extend to desired voice length in serial arrangement)





4. Speech with melody application



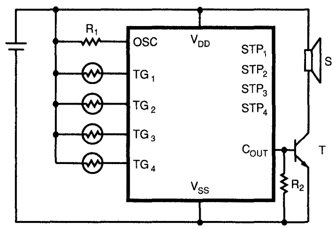


Note:
a. For some melody IC which needs longer pulse trigger, a delay circuit is needed.
b. R3 = 1KΩ typical.

5

APPLICATION CIRCUITS

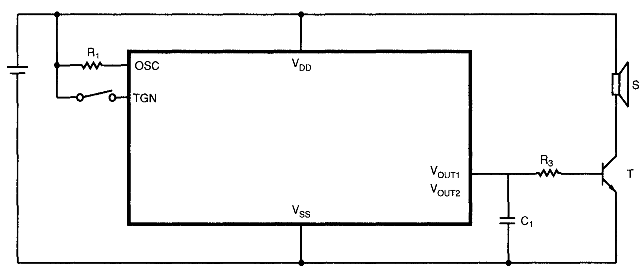
5. CDS Application



Notes:

a. R1 = 1.2MΩ, R2 = 470Ω, C1 = 0.1µf, T (transistor) = with ß > 150, S (speaker) = 1/4W, 8Ω, CDS = Resistance variation range (50K ~ 1.5M), all typical.
b. Piezzo buzzer resonant frequency is around 1KHz.
c. In the melody cascade application, melody I.C. must have tristate output.
d. It is recommended to bond all the unused trigger pad to ground and add a capacitor (0.1µf typical) between used trigger pad and ground for noise immunity purpose.

6. Use V_{OUT1} to drive speaker.



Note: R3 = 1KΩ, C1 = 0.1µf typical

Speech Synthesizer (Voice ROM)

FEATURES

- Can synthesize human voices and most animal sounds
- Direct drive buzzer and one current output combined with a single transistor can drive the speaker
- Up to 15 second speech duration that can be separated into 64 sections for μp mode, 8 sections for SA (stand alone) mode, 16 repetitive sections (in addition to original 8 sections) for both TT (Table Trigger) or RT (Ring Trigger) mode.
- Duration of the 64 (8) sections can be different and determined by customer's voice content of each section, the total maximum duration is about 15 seconds.
- Mute is available for each section up to 48 seconds.
- Expandable, can extend the speech duration by 15 x n seconds with n pieces of MSS1501
- Single power supply can operate at 2.4V through 6.0V.
- Automatic power down function: (selected by bonding option). Starts operating upon receiving a speech synthesis command, and powers down upon conclusion (unvoiced).

DESCRIPTION

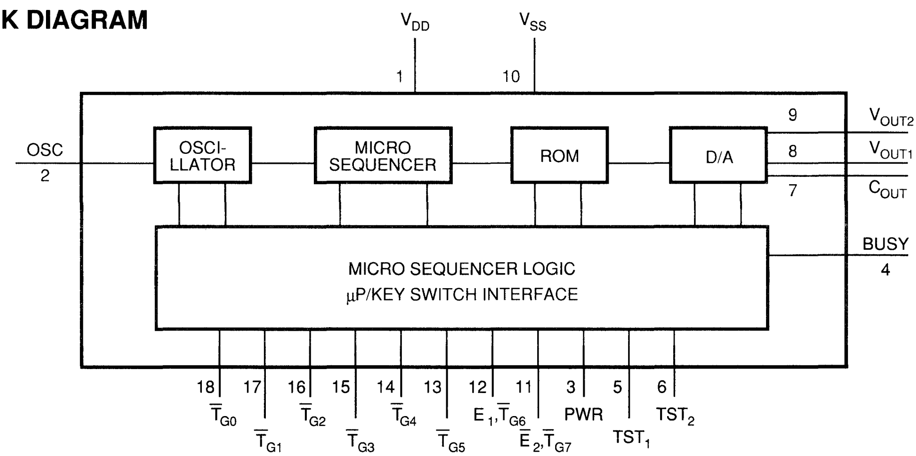
The MSS1501 is a CMOS single-chip speech synthesizing ROM that can synthesize up to 15 seconds of voice using the PCM Quantified Coding method.

The chip contains most of the necessary circuit such as the Oscillator, ROM, D/A converter, sequence control logic and interface circuit for key switches and microcomputers. Application to widely used voice systems with minimum external parts is possible. Micro-Processor (μP) mode, Stand-Alone (SA) mode, Table trigger (TT) mode and Ring trigger (RT) mode are available and selected by mask option. Up to 64 sections of speech are available for μp mode, up to 8 sections are available for SA mode, and up to 16 repetitive sections (in addition to original 8 sections) are available for both TT or RT mode. Several chips can be combined to reach longer voice duration (longer than 15 seconds). Customer speech data is edited and programmed into ROM with a single mask during the device fabrication.

TT mode means with original 8 sections, it could be masked as 16 repetitive sections with jump function, all the masked sections will play out consecutively with one trigger signal. RT mode means with origional 8 sections, it could be masked as 16 repetitive sections with jump function, the masked sections will play out one section by one trigger signal consecutively. TT mode and RT mode could return back to SA mode by bonding option.

5

BLOCK DIAGRAM



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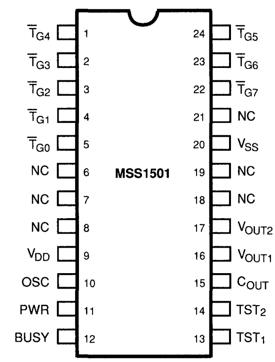
914 West Maude Avenue, Sunnyvale, CA 94086 U.S.A 408-733-4556

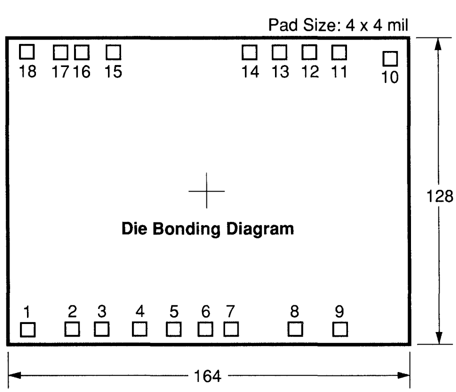
PIN DESCRIPTIONS

PIN NO.	SYMBOL	FUNCTION
1	V_{DD}	Positive power supply
2	OSC	Oscillator input
3	PWR	Active high for non-power down
4	BUSY	Busy signal output, active high
5	TST_1	Test mode, active high
6	TST_2	Test mode, active high
7	C_{OUT}	Audio current output
8	V_{OUT1}	Audio voltage output
9	V_{OUT2}	Audio voltage output
10	V_{SS}	Negative power supply
11	$\overline{E}_2$, $\overline{T}_{G7}$	Enable 2 / Trigger 7, active low
12	E_1, $\overline{T}_{G6}$	Trigger 6, active low Enable 1, active high
13	$\overline{T}_{G5}$	Trigger 5 / address 5, active low
14	$\overline{T}_{G4}$	Trigger 4 / address 4, active low
15	$\overline{T}_{G3}$	Trigger 3 / address 3, active low
16	$\overline{T}_{G2}$	Trigger 2 / address 2, active low
17	$\overline{T}_{G1}$	Trigger 1 / address 1, active low
18	$\overline{T}_{G0}$	Trigger 0 / address 0, active low

PIN CONFIGURATION



BONDING DIAGRAM



1. VDD (-1841.3, -1328.5)
2. OSC (-1394.8, -1375.8)
3. PWR (-1105.2, -1370.6)
4. BUSY (-783.1, -1382.0)
5. TST_1 (-510.5 -1375.8)
6. TST_2 (-220.9, -1370.6)
7. C_{OUT} (-15.4, -1370.6)
8. V_{OUT1} (712.4, -1378.2)
9. V_{OUT2} (1188.7, -1378.2)
10. V_{SS} (-1809.9, -1318.5)
11. $\overline{T}_{G7}$ (1054.9, 1373.5)
12. $\overline{T}_{G6}$ (765.3, 1368.3)
13. $\overline{T}_{G5}$ (560.1, 1373.5)
14. $\overline{T}_{G4}$ (270.5, 1363.3)
15. $\overline{T}_{G3}$ (-1061.0, 1373.5)
16. $\overline{T}_{G2}$ (-1350.6, 1368.3)
17. $\overline{T}_{G1}$ (-1555.8, 1373.5)
18. $\overline{T}_{G0}$ (-1845.4, 1323.3)

ABSOLUTE MAXIMUM RATINGS

SYMBOL	RATING	UNITS
V_{DD} - V_{SS}	-0.5 ~ +0.7	V
V_{IN} ($\overline{T}_{G0}$-$\overline{T}_{G7}$, E_1, $\overline{E}_2$, PWR)	V_{SS}-0.3 < V_{IN} < V_{DD}+0.3	V
V_{OUT} (BUSY)	V_{SS} < V_{OUT} < V_{DD}	V
T(Operating)	-10 ~ +60	°C
T(Storage)	-55 ~ +125	°C

DC ELECTRICAL CHARACTERISTICS

PARAMETER NAME	PARAMETER		TEST CONDITIONS	MSS1501 MIN.	TYP.	MAX.	UNITS
V_{DD}	Operating Voltage			2.4	4.5	5	V
I_S	Supply Current	Stand by	V_{DD} = 4.5, I/O open	-	-	0.6	µA
I_O		Operating		-	-	100	
V_{IH}	Input Voltage ($\overline{T}_{G0}$ - $\overline{T}_{G7}$, E_1, $\overline{E}_2$, PWR)		V_{DD} = 4.5	4	4.5	4.5	V
V_{IL}				-0.3	0	0.3	
I_{IL}	Input Current ($\overline{T}_{G0}$ - $\overline{T}_{G7}$)		V_{DD} = 4.5	-	-	5	µA
I_{IH}				-	0	-	
I_{IH}	Input Current for PWR		V_{DD} = 4.5	-	-	10	µA
I_{IL}				-	0	-	
I_{OH}	O/P Current V_{OUT1}, V_{OUT2}	Drive	V_{DD} = 4.5V, $V_{O/P}$ = 4V	-	-5	-	mA
I_{OL}		Sink	V_{DD} = 4.5V, $V_{O/P}$ = 0.5V	-	5	-	
I_{OH}	Output Current (BUSY)		V_{DD} = 4.5V, $V_{O/P}$ = 4V	-	-1	-	mA
I_{CL}			V_{DD} = 4.5V, $V_{O/P}$ = 0.5V	-	1	-	
ΔF/F	Frequency Stability		$\frac{F_{OSC}(4.5V)-F_{OSC}(4V)}{F_{OSC}(4.5V)}$	-	-	5	%
ΔF/F	Frequency Variation		V_{DD} = 4.5V, R_{OSC} = 1M	-	-	15	%
I_{CO}	Output Current (C_{OUT})		V_{DD} = 4.5V	-	-1		mA

AC ELECTRICAL CHARACTERISTICS

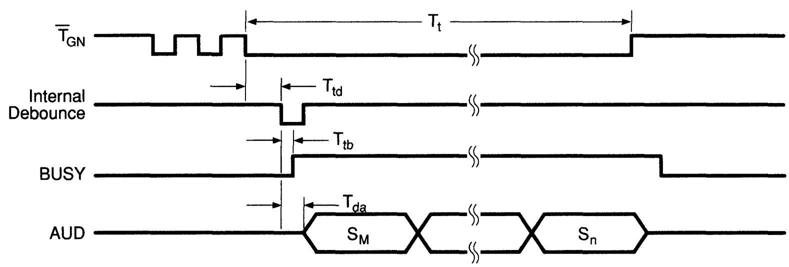
Stand - alone Mode				Micro - processor Mode			
PARAMETER NAME	PARAMETER	MIN.	MAX.	PARAMETER NAME	PARAMETER	MIN.	MAX.
T_t	Trigger pulse width	15 ms		T_w	Write Enable pulse width	300 ns	
T_{td}	Trigger to Debounce delay time		10 ms	T_h	Trigger address hold time	80 ns	
T_{db}	Debounce to BUSY delay time		200 µs	T_{wb}	Write Enable to BUSY delay time		200 µs
T_{da}	Debounce to Audio delay time		250 µs	T_{wa}	Write Enable to Audio delay time		250 µs

5

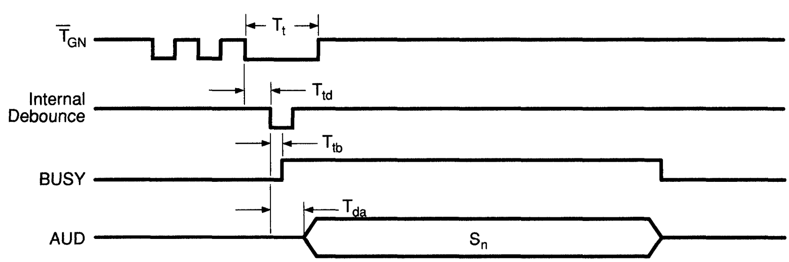
TIMING WAVEFORMS

I. Stand-alone level Mode

1. Level trigger

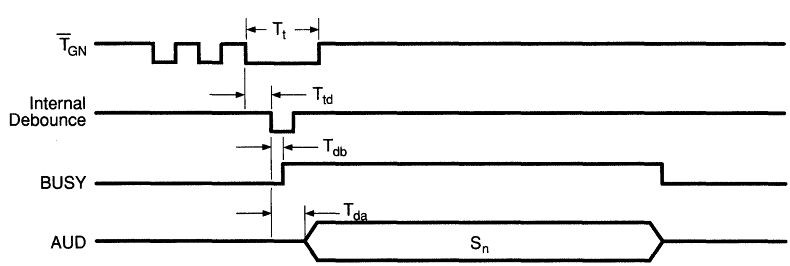


2. Edge trigger



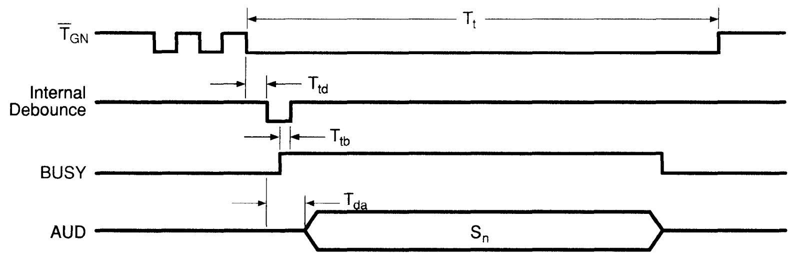
II. Stand-alone Edge Mode

1. Pulse-Mode Edge trigger



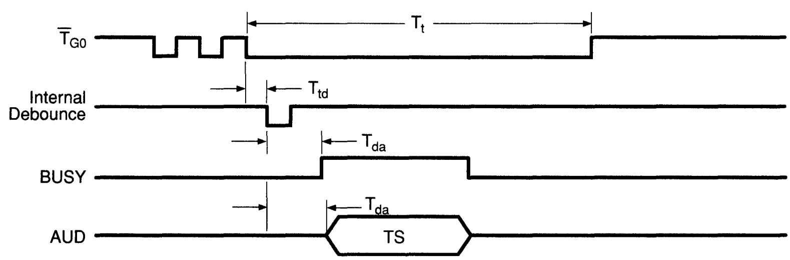
TIMING WAVEFORMS

2. Level trigger

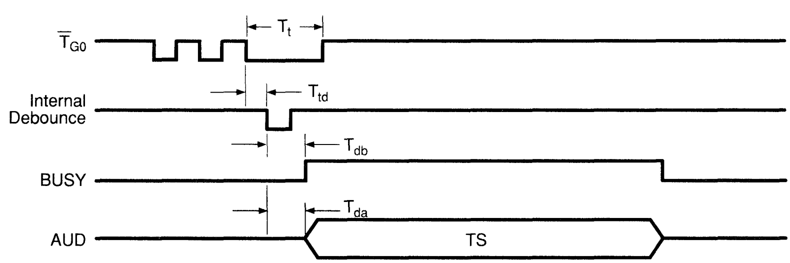


III. Stand-alone TT mode

1. Level trigger



2. Edge trigger

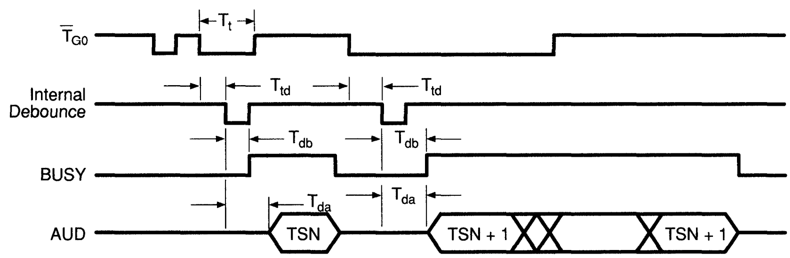


5

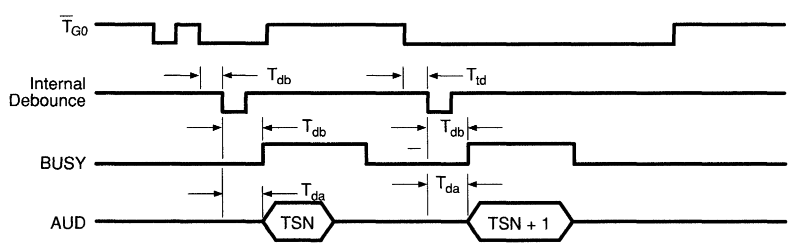
TIMING WAVEFORMS

IV. Stand-alone RT mode

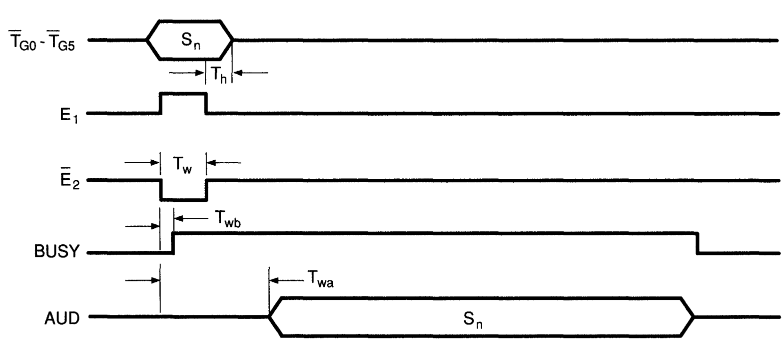
1. Level mode



2. Edge mode



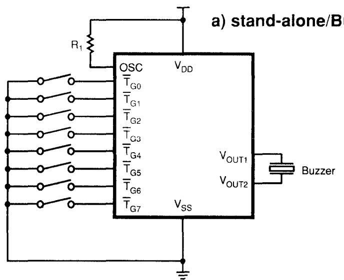
V. CPU mode



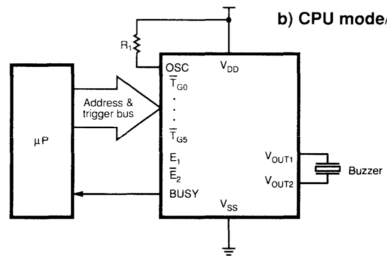
APPLICATION CIRCUITS

1. Typical application

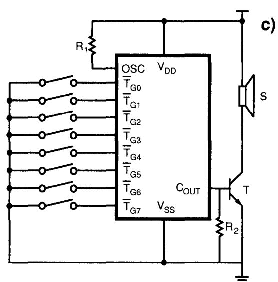
a) stand-alone/Buzzer



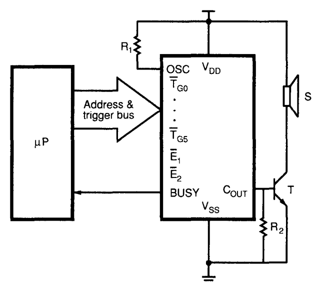
b) CPU mode/Buzzer



c) stand-alone/ Speaker

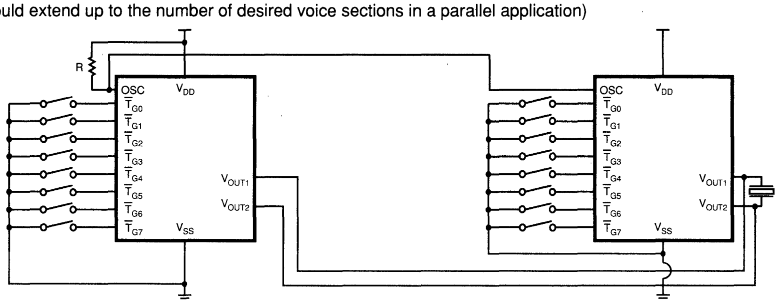


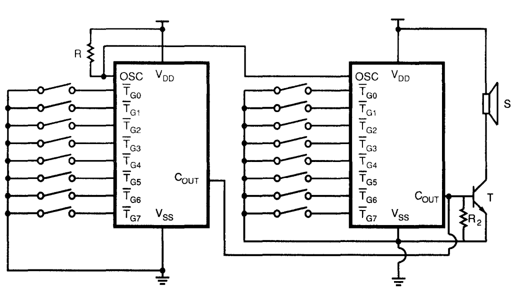
d) CPU mode/Speaker



2. Parallel application

(Could extend up to the number of desired voice sections in a parallel application)

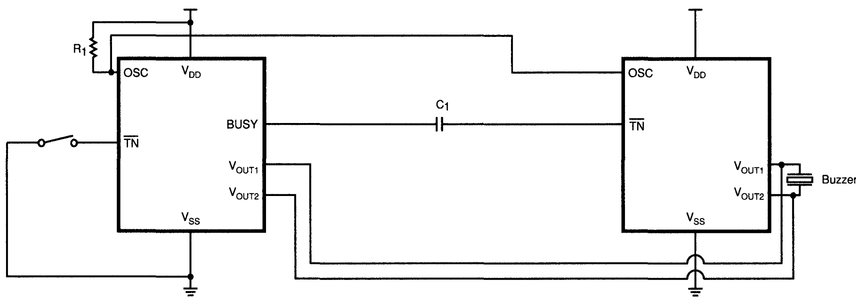


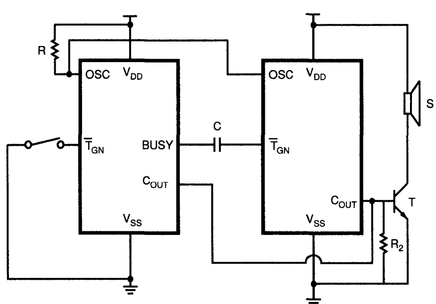


APPLICATION CIRCUITS

3. Cascade application

(Could extend to a desired voice length in serial arrangement)

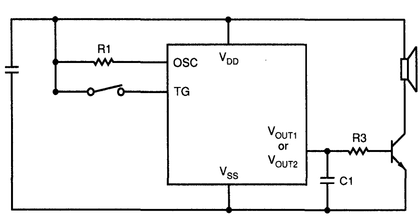




Notes:

1. R_1 = 1.2M OHM, C = 0.1µf, R_2 = 470Ω, T = Transistor with ß > 150, S = 1/4W, 8Ω; all typical
2. In UP Mode cascade and parallel application is acceptable.
3. All applications for buzzer are the same as above just substitute speaker by connecting buzzer to V_{OUT1} and V_{OUT2}.

4. Using VOUT1 or VOUT2 output pads, another speaker driving circuit could be used for increasing sound volume.



Note:

1. R3 = 1K, C1 = 0.1µf; all typical

APPLICATION CIRCUIT DEFINITIONS

1. Sn = Sth speech section, TS = all section of speech in table
2. $\overline{T}_{GN}$ means $\overline{T}_{G0}$ - $\overline{T}_{G7}$, AUD means C_{OUT}, V_{OUT1}, V_{OUT2}.
3. $\overline{T}_{G0}$ - $\overline{T}_{G5}$, $\overline{T}_{G6}$, $\overline{E}_2$, $\overline{T}_{G7}$ are internally pulled high.
4. For stand alone mode $\overline{T}_{G0}$ - $\overline{T}_{G7}$ use as section trigger input (low active)
5. For cpu mode, $\overline{T}_{G0}$ - $\overline{T}_{G5}$ use as section address bus, E_1, $\overline{E}_2$ use as trigger input.
6. No matter what status the chip is, every retrigger action will reload address and play the speech from beginning.

Speech Synthesizer (Voice ROM)

FEATURES

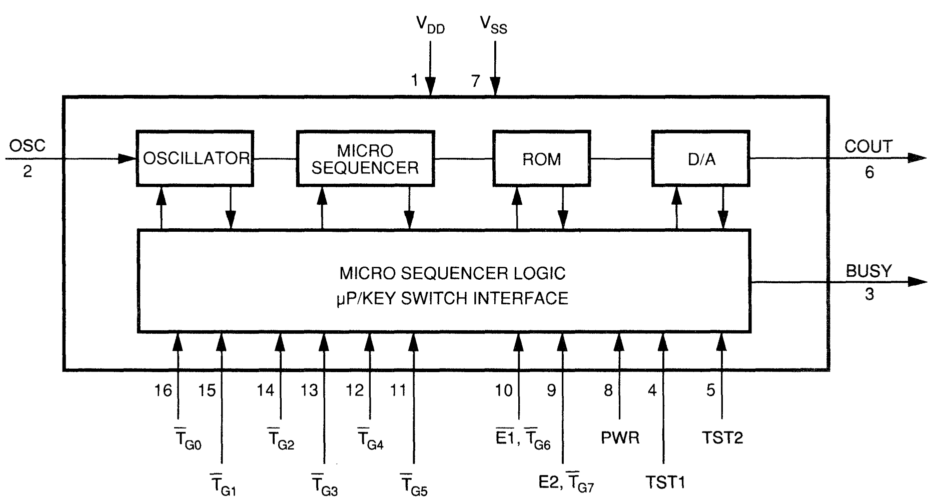
- Can synthesize human voices and most animal sounds.
- Direct current output combined with a single transistor can drive a speaker.
- Up to 20 seconds speech duration that can be separated into 64 sections for µp mode, 8 sections for SA (Standalone) mode.
- Duration of the 64 (8) sections can be different and determined by customer's voice content of each section, the total maximum duration is about 20 seconds.
- Mute is available for each section up to 48 seconds.
- Expandable, can extend the speech duration by 15 x n seconds with n pieces of MSS2001.
- Single power supply can operate at 2.4V through 6.0V.
- Automatic power down function: (selected by bonding option). Starts operating upon receiving a speech synthesis command, and powers down upon conclusion (unvoiced).

DESCRIPTION

The MSS2001 is a CMOS single-chip speech synthesizing ROM that can synthesize up to 20 seconds of voice using the PCM Quantified Coding method.
The chip contains most of the necessary circuit such as the Oscillator, ROM, D/A converter, sequence control logic and interface circuit for key switches and microcomputers. Application to widely used voice systems with minimum external parts is possible. Up to 64 sections of speech are available for µp mode, up to 8 sections are available for SA mode. Several chips can be combined to reach longer voice duration (longer than 20 seconds). Customer speech data is edited and programmed into ROM with a single mask during the device fabrication.

5

BLOCK DIAGRAM



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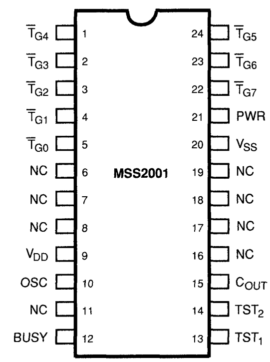
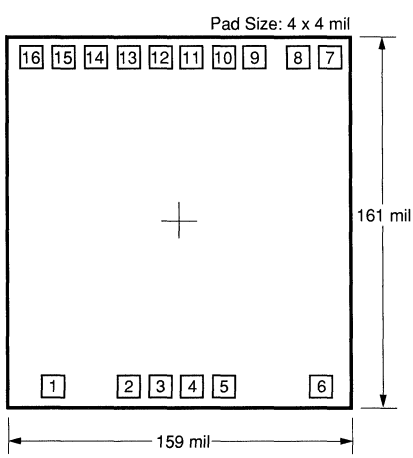
PIN DESCRIPTION

PIN NO.	SYMBOL	FUNCTION
1	V_{DD}	Positive power supply
2	OSC	Oscillator Input
3	BUSY	Busy signal output; active high
4	TST1	Test mode production test only
5	TST2	Test mode, production test only
6	C_{OUT}	Speech signal current outputs
7	V_{SS}	Negative power supply
8	P_{WR}	Active high for non-power down
9	E2, $\overline{T}_{G7}$	Enable 2; active high, Trigger 7; active low
10	$\overline{E1}$, $\overline{T}_{G6}$	Enable 1/Trigger 6; active low
11	$\overline{T}_{G5}$	Trigger/Address 5; active low
12	$\overline{T}_{G4}$	Trigger/Address 4; active low
13	$\overline{T}_{G3}$	Trigger/Address 3; active low
14	$\overline{T}_{G2}$	Trigger/Address 2; active low
15	$\overline{T}_{G1}$	Trigger/Address 1; active low
16	$\overline{T}_{G0}$	Trigger/Address 0; active low

PIN CONFIGURATION



BONDING DIAGRAM



PIN NO.	DESIGNATION	X	Y
1.	V_{DD}	–1778.3	–1701.6
2.	OSC	–455.3	–1764.5
3.	BUSY	–171.8	–1785.6
4.	TST_1	125.0	–1764.5
5.	TST_2	416.8	–1764.5
6.	COUT	1612.2	1762.9
7.	V_{SS}	1737.0	1762.9
8.	PWR	1442.2	1765.5
9.	$\overline{T}_{G7}$, E2	944.9	1765.5
10.	$\overline{T}_{G6}$, $\overline{E1}$	551.4	1765.6
11.	$\overline{T}_{G5}$	253.7	1764.7
12.	$\overline{T}_{G4}$	–188.2	764.6
13.	$\overline{T}_{G3}$	–486.0	765.5
14.	$\overline{T}_{G2}$	–927.9	1764.6
15.	$\overline{T}_{G1}$	–1225.7	1765.5
16.	$\overline{T}_{G0}$	–1627.2	1765.5

*Note: Substrate is V_{DD}

Unit: µM

ABSOLUTE MAXIMUM RATINGS

SYMBOL	RATING	UNITS
V_{DD} - V_{SS}	–0.5 ~+0.7	V
V_{IN} ($\overline{T}_{G0}$ ~ $\overline{T}_{G7}$, P_{WR})	V_{SS}–0.3 < V_{IN} < V_{DD}+0.3	V
V_{OUT} (BUSY)	V_{SS} < V_{OUT} < V_{DD}	V
T(Operating)	–10 ~ +60	°C
T(Storage)	–55 ~ +125	°C

DC ELECTRICAL CHARACTERISTICS

PARAMETER NAME	PARAMETER		TEST CONDITIONS	MSS2001 MIN.	TYP.	MAX.	UNITS
V_{DD}	Operating Voltage			2.4	4.5	5	V
I_{SB}	Supply Current	Stand by	V_{DD} = 4.5, I/O Open	-	-	0.6	μA
I_{OP}		Operating		-	-	120	
V_{IH}	Input Voltage ($\overline{T}_{G0}$ ~ $\overline{T}_{G7}$, E1, E2, P_{WR})		V_{DD} = 4.5V	4	4.5	5	V
V_{IL}				–0.3	0	0.3	
I_{IL}	Input Current ($\overline{T}_{G0}$ ~ $\overline{T}_{G7}$)		V_{DD} = 4.5V	-	-	5	μA
I_{IH}				-	0	-	
I_{CO}	Output Current (C_{OUT})		V_{DD} = 4.5V	-	–1	-	mA
I_{IH}	Input Current for PWR		V_{DD} = 4.5V	-	-	10	μA
I_{IL}				-	0	-	
I_{OH}	Output Current (BUSY)		V_{DD} = 4.5V, $V_{O/P}$ = 4V	-	–1	-	mA
I_{OL}			V_{DD} = 4.5V, $V_{O/P}$ = 0.5V	-	1	-	
ΔF/F	Frequency Stability		F_{OSC}(4.5V)–F_{OSC}(4V) / F_{OSC}(4.5V)	-	-	5	%
ΔF/F	Frequency Variation		V_{DD} = 4.5V, R_{OSC} = 1.2MΩ	-	-	15	%

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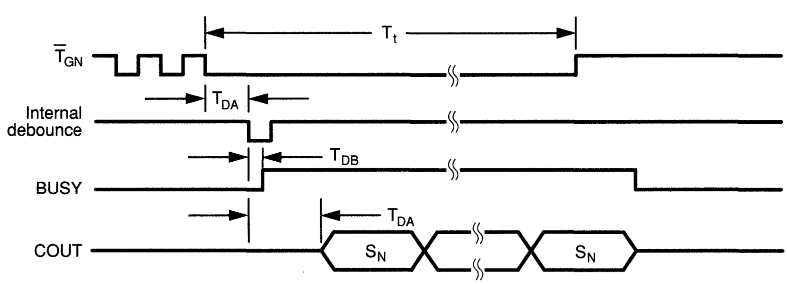
AC ELECTRICAL CHARACTERISTICS

STANDALONE MODE			
TIMING		MIN.	MAX.
T_T	Trigger pulse width	15ms	
T_{TD}	Trigger to Debounce delay time		10ms
T_{DB}	Debounce to BUSY delay time		200µs
T_{DA}	Debounce to Audio delay time		250µs
MICROPROCESSOR MODE			
TIMING		**MIN.**	**MAX.**
T_W	Write Enable pulse width	30ns	
T_H	Trigger address hold time	80ns	
T_{WB}	Write Enable to BUSY delay time		200µs
T_{WA}	Write Enable to Audio delay time		250µs

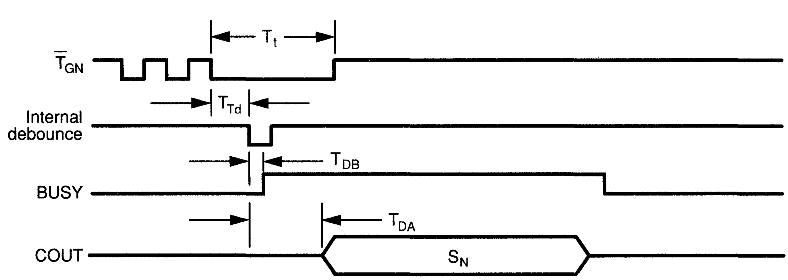
TIMING WAVEFORMS

I. Standalone-Level Mode

1. Level Trigger



2. Edge Trigger

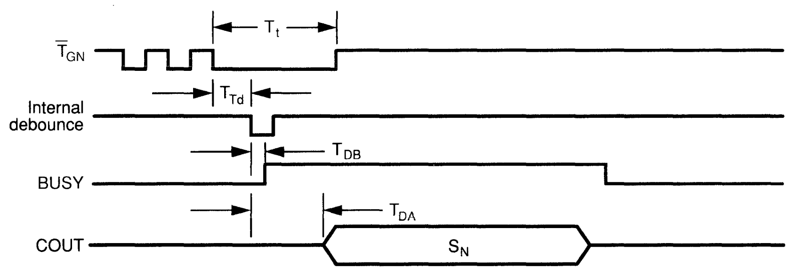


Notes:
1. $\overline{T}_{G0} \sim \overline{T}_{G7}$ are low active.
2. $\overline{T}_{G0} \sim \overline{T}_{G7}$ are internal pull high.

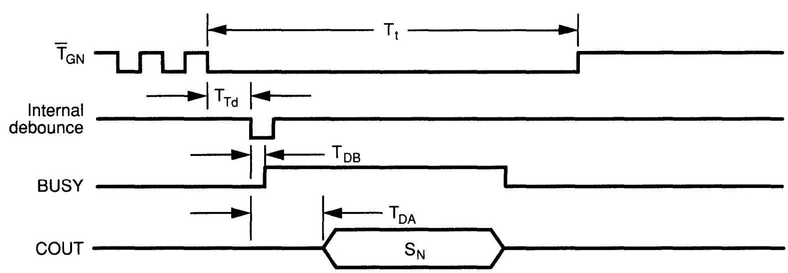
TIMING WAVEFORMS

II. Standalone-Edge Mode

1. Edge Trigger

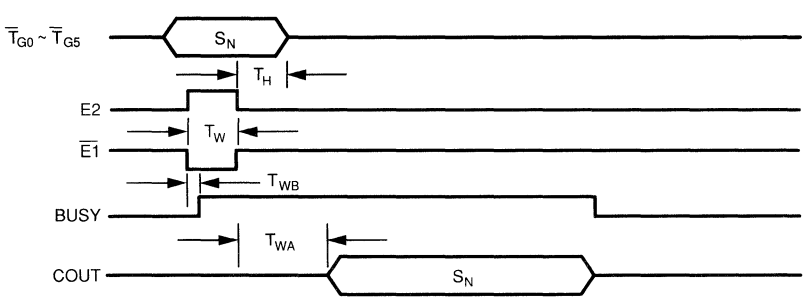


2. Level trigger



Note:
$\overline{T}_{G0}$ ~ $\overline{T}_{G7}$ are internal pull high.

III. CPU Mode

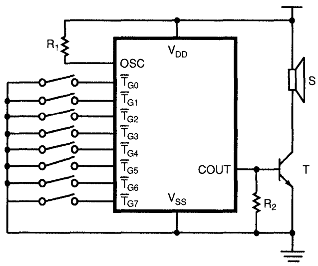


Notes:
1. $\overline{T}_{G0}$ ~ $\overline{T}_{G5}$ are used as address bus.
2. $\overline{E1}$, E2, are used as trigger input.
3. $\overline{T}_{G0}$ ~ $\overline{T}_{G5}$, $\overline{E1}$, E2, are internally pulled high.
4. Every retrigger action will reload address and play the speech from the beginning.
5. In CPU mode to avoid unwanted noise caused by abrupt change between different sections of voice messages, it is recommended to program PWR pin to high (V_{DD}) during voice processing.

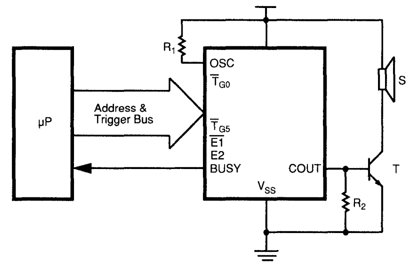
APPLICATION CIRCUITS

1. **Typical application**

a. Standalone

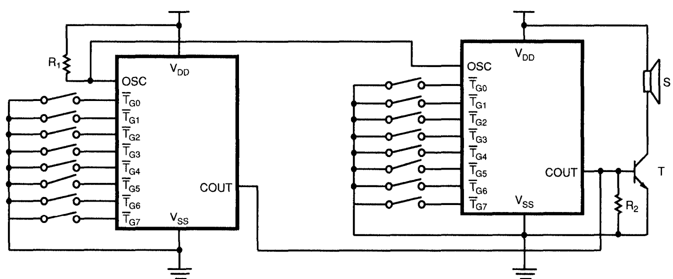


b. CPU Mode



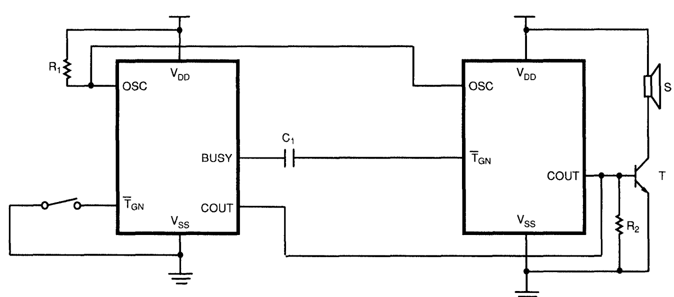
2. **Parallel application**

(Could extend up to desired number of voice sections in parallel arrangement)



3. **Cascade application**

(Could extend to desired voice length in serial arrangement)



Notes:

a. R1 (resistor) = 1.2MΩ, R2 = 470Ω, T (transistor) = ß > 150, S (speaker) = 1/4W, 8Ω, C1 = 0.1µf; all typical.

b. Both cascade and parallel application can apply to CPU mode.

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CACHE PRODUCTS

CACHE PRODUCTS

MOSEL is developing a family of high performance cache products for microprocessor based applications, including Data RAM, Cache Tag RAM, and Cache Controller products.

As microprocessors advance, faster memory is needed to tap the increasing performance potential. Slow DRAM memory requires wait states that reduce processor performance. In order to keep microprocessors running at full speed, system designers are using high speed SRAM caches.

Traditional SRAM memory product architectures can be used to implement crude cache solutions, although many chips are required to implement even simple cache architectures. By developing specialized memory architectures for the cache application, it is possible to implement sophisticated new features that increase system performance. Three distinct functions are needed to implement a cache solution:

1. Cache Data RAM and Burst RAM:	Stores the data required by the microprocessor.
2. Cache Tag or Directory:	Keeps track of what data is stored in the cache.
3. Controller:	Control logic that provides all the signals to make it work. Often the controllers include Tag RAM.

MOSEL is developing specialized products that perform each of these functions.

When used together, MOSEL's products provide complete cache subsystem solution for many microprocessor applications.

CACHE DATA RAM PRODUCTS

One of the first such products offered, MOSEL's MS82C308 Cache Data RAM architecture provides an efficient cost effective cache subsystem building block. Designed for use with first generation cache controllers such as the Intel 82285 or the Chips & Technologies 82C307/82C327, the 2K x 16 x 2 set MS82C308 provides a minimum chip count solution for 2 set cache implementation, with 20 and 25 MHz versions offered today, and a shrink version at 33 MHz scheduled for later this year.

Now under development is a totally new generation architecture for Cache Data RAM products, the Quad Data RAM family, which sets a new platform for cache performance. The pioneering dual ported 16K x 9 Quad Data RAM architecture supports a whole new generation of Cache features: simultaneous processor/main memory transactions, reduced capacitive loading on processor, burst mode quad fetch, support for parity. Scheduled for production release in late 1990, the Quad Data RAM products will be offered in 25 and 33 MHz versions with later performance upgrade to 40 and 50 MHz.

CACHE TAG RAM PRODUCTS

The 2K x 20 MS8202 Cache Tag RAM provides a high integration cache subsystem building block for custom cache implementations. With high speed 20, 22 and 25ns match times, the MS8202 supports many popular microprocessor families.

Now under development is our new generation Expansion Tag RAM family, a new concept in Tag RAM. Designed for use with MOSEL's cache controller products, the Expansion Tag RAM serves as a tag array extension for the controller to permit larger cache sizes without large line sizes that degrade system performance. As a stand alone Tag RAM for custom cache implementations, the expansion Tag RAM provides new features such as a snoop bus for cache coherency and a synchronous interface for simplified design.

CACHE CONTROLLER PRODUCTS

MOSEL has three cache chipsets currently under development: the MS82C440 for 80486 systems; the MS82C330 for 80386 systems with write-through cache; and the MS82C340 chipset for 80386 systems with write-back cache.

These products represent a new generation in cache control, supporting new features such as simultaneous processor/main memory transactions, burst mode quad fetch with demand word priority and abort option, write back and/or write through option. Other features include: a snoop bus for cache coherency, on chip support for noncacheable regions, and math co-processors, cache sizes of 64K bytes to 256K bytes. All three products are scheduled for production release in 1991.

2K x 20 Cache Tag RAM

FEATURES

- Pin for pin compatible with SGS-Thomson MK4202 Cache Tag RAM
- High Speed Match (to 20ns) supports high performance processors including 68020, 68030, 68040, 80386 and 80486
- High Integration 2K x 20 Tag array provides single chip tag RAM solution for direct map cache applications or one chip per set in multiple set cache implementations.
- Multiple chip selects permit building of deeper cache using multiple tag RAMs
- Clear function facilitates development of virtual memory cache
- Low Power: 250mA max. active; 50mA max. standby
- Significantly reduces board real estate required for custom cache controller implementations

DESCRIPTION

The MOSEL MS8202 is a high performance CMOS Cache Tag RAM optimized for use in microprocessor cache applications.

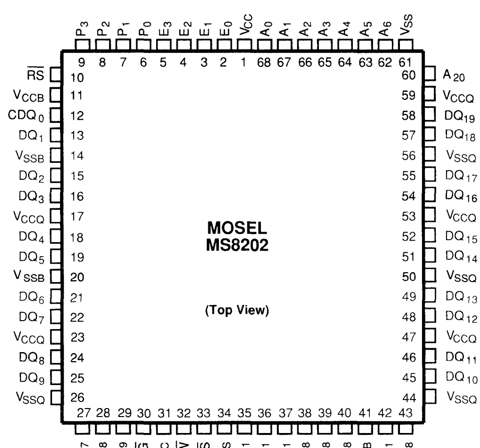
The 2K x 20 Tag RAM array is an ideal building block for custom direct map or multiple set caches having sufficient depth (2K) and width (x 20) to provide a single chip Tag RAM solution (per set) for most cache implementations.

The MS8202 is available with fast match access times down to 20ns (max) which facilitates use with many popular high performance microprocessor families including Motorola's 68xxx series (68020, 68030 and 68040) and Intel's iAPX86 series (80286, 80386 and 80486).

Each 8202 replaces 4-6 traditional Cache Tag RAMs (4K x 4, 512 x 9, etc.) plus additional discrete logic. This offers significant reduction in board real estate, power, cost and capacitive loading.

The MS8202 is manufactured using a high performance CMOS process and operates from a single 5 volt power supply. All inputs and outputs are TTL compatible. The device is supplied in a space saving JEDEC standard 68 pin PLCC package.

PIN CONFIGURATION



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PIN DESCRIPTIONS

A_0 - A_{10} Index Address Inputs

These 11 address inputs select one of 2048 21 bit Tag Array words.

$\overline{S}$ Chip Select Input

This pin is active LOW. When active, it enables the read and write operations.

E_0 - E_3 Chip Enable Inputs

These four enable pins are selectable to be either active HIGH or active LOW. All four enable pins must be active to enable the chip. The DQ pins will be in the high impedance state when any one of the enable pins is not active.

P_0 - P_3 Chip Enable Program Inputs

These four pins are used to select the polarity of the corresponding chip enable pins E_0-E_3. For example, if P_0 is tied HIGH, E_0 will be active HIGH; if P_0 is tied LOW, E_0 will be active LOW.

$\overline{G}$ Output Enable Input

The output enable is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be output on pins DQ_1 through DQ_{19} and CDQ_0. DQ_1 - DQ_{19} and CDQ_0 will be in the high-impedance state when $\overline{G}$ is inactive.

$\overline{W}$ Write Enable Input

The write enable input is active LOW and controls read and write operations. With the chip selected and enabled, when $\overline{W}$ is HIGH and $\overline{G}$ is LOW, output data will be presented at the DQ pins; when $\overline{W}$ is LOW, the data present on the DQ pins will be written into the addressed memory location.

$\overline{CG_0}$ - $\overline{CG_1}$ Compare Output Enable Inputs

These inputs are active LOW. CG_0 enables the C_0 compare output hit or miss signal. CG_1 enables the C_1 compare output signal.

$\overline{H}_0$ - $\overline{H}_1$ Force Hit Inputs

These pins are active LOW and are used to force the compare outputs HIGH (signifying a hit). H_0 controls compare output C_0 and H_1 controls compare output C_1

$\overline{M}_0$ - $\overline{M}_1$ Force Miss Inputs

These pins are active LOW and are used to force the compare outputs LOW (signifying a miss). M_0 controls compare output C_0 and $\overline{M}_1$ controls compare output C_1.

$\overline{RS}$ Reset Input

This reset pin is active LOW. When active it resets the 2048 bits in CDQ_0 to a logic zero.

C_0 - C_1 Compare Outputs

When the chip is in compare mode ($\overline{W}$ and $\overline{G}$ HIGH and E_0 - E_3 enabled), C_0 and C_1 will be HIGH signaling a cache hit if the data inputs DQ_1 - DQ_{19} and CDQ_0 match the contents of the Tag RAM array stored at address A_0-A_{10}. C_0 and C_1 will be LOW signalling a cache miss if the aforementioned data does not match. Signals $\overline{CG_0}$ and $\overline{CG_1}$ must be low to enable the compare signals C0 and C1. When $\overline{CG_0}$ or $\overline{CG_1}$ are high, the C_0 and C_1 outputs will be in the high impedence state.

CDQ_0 Clearable Tag Data Input / Output Port

This bidirectional port is used in conjunction with DQ_1 - DQ_{19} to read data from or write data to the tag RAM array. In addition, during a Reset cycle all 2048 internal RAM bits accessed by CDQ_0 are cleared to a logic zero. This output can be used as a tag valid bit.

DQ_1 - DQ_{19} Tag Data Input / Output Ports

These 19 bidirectional ports are used to read data from or write data into the tag RAM array.

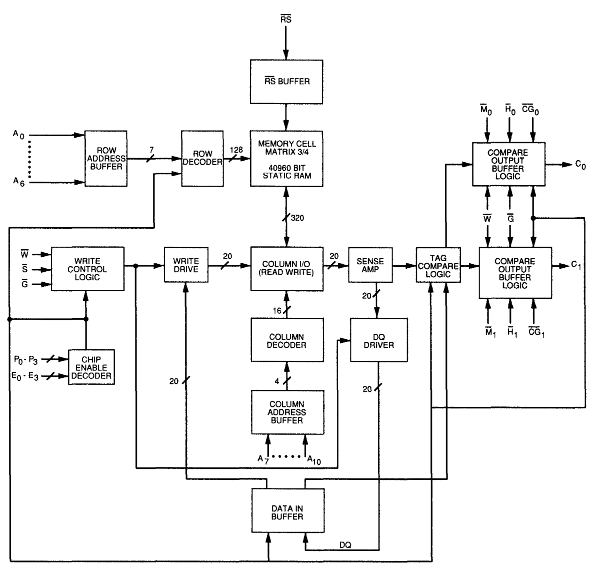
V_{CC} Power Supply

V_{CC0} Output Power Supply

V_{SS} Ground

V_{SS0} Output Ground

FUNCTIONAL BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION AND FEATURES

The MOSEL MS8202 is designed to be connected directly to a high performance 32 bit microprocessor, allowing the elimination of the logic delays associated with collecting Hit or Miss outputs into a subsequent gate or the RC delays associated with wired-OR open collector match outputs.

The MS8202 cache tag RAM has four major features that allow direct connection:

1. Wide enough for almost any tag RAM application without requiring multiple chip width expansion and the delays that would result.
2. Four (4) programmable chip enable inputs, allowing depth expansion without any of the attendant chip enable decode delays that would otherwise be required.
   P_0-P_3 should be tied directly to V_{CC} or V_{SS}, or through pull-up or pull-down resistors. The MS8202 is selected when E_0-E_3 equals P_0-P_3 in a binary match. (Example: E_0-E_1 = 0110, P_0-P_3 = 0110.)
3. Three-state compare outputs, allowing all Compare outputs to be bused together so the Address-to-Compare access time for a depth expanded application is identical to that of a single device. The programmable chip enables prevent bus contention by assuring that only one tag RAM at a time drives each Compare bus when in Compare mode.
4. Dual compare outputs (C_0 and C_1) and forced hit ($\overline{H}_0$ and $\overline{H}_1$) and forced miss ($\overline{M}_0$ and $\overline{M}_1$) inputs for each. The arrangement allows direct connection of the tag RAM to two separate processor inputs (such as $\overline{\text{BERR}}$ and $\overline{\text{HALT}}$ on the 68030), and connection of all signals that would otherwise have been connected to those processor inputs to be passed through the tag RAM; eliminating the need for a subsequent gate to collect the COMPARE output and other BERR or $\overline{\text{HALT}}$ signal sources to the processor. The net effect is that the Address-to-Compare access time demonstrated by the MS8202 is the only delay the user must consider. The alternative approach, using narrow tag RAMs with open collector outputs or narrow tag RAMs with 2-state outputs and a 10ns programmable logic device, requires that the narrow tag RAMs demonstrate a 10ns Address-to-Compare access time to yield the same performance in a user's system that the MS8202 provides.

TRUTH TABLE

$\overline{RS}$	$\overline{S}$	E	$\overline{W}$	$\overline{G}$	$\overline{M}_X$	$\overline{H}_X$	$\overline{CG}_X$	Mode	C_X	DQ	Notes
H	–	X	–	–	L	X	X	Force Miss	Low	–	1
H	–	X	–	–	H	L	X	Force Hit	High	–	1
H	–	X	–	–	H	H	H	Comp disable	Hi-Z	–	1
H	X	F	X	X	H	H	H	Standby	Hi-Z	Hi-Z	
H	X	T	H	H	H	H	H	Compare	Hi-Z	D in	
H	X	T	H	H	H	H	L	Compare	Hi or Lo	D in	
H	H	T	L	X	H	H	L	Hit	High	Hi-Z	
H	H	T	X	L	H	H	L	Hit	High	Hi-Z	
H	L	T	L	X	H	H	L	Write	High	D in	
H	L	T	H	L	H	H	L	Read	High	D Out	
L	H	X	X	X	–	–	–	Reset	–	Hi-Z	
L	X	F	X	X	–	–	–	Reset	–	Hi-Z	
L	X	X	H	H	–	–	–	Reset	–	Hi-Z	
L	X	X	H	L	–	–	–	Reset	–	Lo-Z	
L	L	T	L	X	–	–	–	Not Allowed	–	Hi-Z	2
L	X	T	H	H	H	H	L	Reset	L	D in	3

Key:
- X = Don't Care
- $\overline{H}_X$ = $\overline{H}_0$ or $\overline{H}_1$
- $\overline{M}_X$ = $\overline{M}_0$ or $\overline{M}_1$
- $\overline{CG}_X$ = $\overline{CG}_0$ or $\overline{CG}_1$
- F = (False) E_0-E_0 pattern DOES NOT match P_0-P_3 pattern.
- T = (True) E_0-E_0 pattern DOES match P_0-P_3 pattern.
- – = Not related to identified mode of operation.

Notes:
1. Force hit /miss operations independent of other RAM operations
2. May disrupt Reset, will not damage device.
3. Reset will force C_X low during a valid compare when CDQ_0 is D_{IN} = HIGH.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	–0.3 to 7.0	V
T_{STG}	Storage Temperature	–55 to 125	°C
P_T	Device Power Dissipation	2.5	Watts
I_{OUT}	DC Output Current (per Pin)	25	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

RANGE	AMBIENT TEMPERATURE	Vcc
Commercial	0°C to + 70°C	5V ± 10%

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = 0 to +70°C)

PARAMETER NAME	PARAMETER	TEST CONDITIONS	MIN.	TYP. [1]	MAX.	UNITS
V_{IL}	Guaranteed Input LOW Voltage		–0.3	–	0.8	V
V_{IH}	Guaranteed Input HIGH Voltage		2.2	–	V_{CC} + 0.3	V
I_{IL}	Input Leakage Current	V_{CC} = Max, V_{IN} = 0Vto V_{CC}	–1	–	+1	µA
I_{OL}	Output Leakage Current[2]	V_{CC} = Max, V_{IN} = 0V toV_{CC}	–10	–	+10	µA
V_{OL}	Output LOW Voltage[3]	V_{CC} = Min, I_{OL} = 8mA	–	–	0.4	V
V_{OH}	Output HIGH Voltage[3]	V_{CC} = Min, I_{OH} = – 4mA	2.4	–	–	V
I_{CC}	Average Power Supply Current[4]				250	mA
I_{CCA}	Active Power Supply Current (f=0)[4]				200	mA
I_{CCSB}	Standby Power Supply Current[4]				50	mA

1. Typical characteristics are at V_{CC} = 5.0V, t_A = 25°C
2. Measured at CDQ_0, DQ_1-DQ_{19}, C_0 and C_1.
3. All voltages referenced to V_{SSQ}.
4. Measured with outputs open. V_{CC} max.

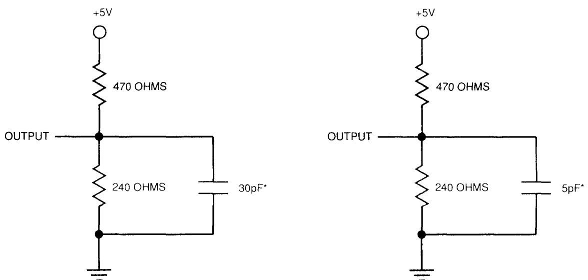
CAPACITANCE[1] (T_A = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	VALUE	UNIT
		Max.	
C_{IN}	Input Capacitance	4	pF
C_{OUT}	Output Capacitance	10	pF

1. This parameter is guaranteed but not tested.

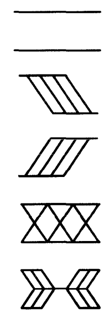
AC TEST CONDITIONS

Input Levels	0V to 3V
Transition Times	5ns
Input and Output Timing Reference Level	1.5V



*Includes scope and test JIG.

KEY TO SWITCHING WAVEFORMS



WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

READ MODE

The MS8202 is in the Read mode whenever $\overline{W}$ is HIGH, and $\overline{G}$ is LOW provided Chip Select ($\overline{S}$) is LOW and a true Chip Enable pattern (E_0 - E_3) is applied. The 11 address inputs (A_0-A_{10}) define a unique index address giving access to 20 of 40,960 bits of data in the static memory array. Valid data will be present at the 20 output pins within t_{AVQV} of the last stable address provided Chip Enable, Chip Select ($\overline{S}$), and Output Enable ($\overline{G}$) access times have been met. If Chip Enable, $\overline{S}$, or $\overline{G}$ access times are not met, data access will measured from the latter falling edge or limiting parameter (t_{EVQV}, t_{SLQV}, or t_{GLQV}). The state of the tag data I/O pins is controlled by the (E_0 - E_3), $\overline{S}$, $\overline{G}$, and $\overline{W}$ input pins. The data lines may be indeterminate at t_{EVQX}, or t_{SLQX}, or t_{GLQX}, but will always have valid data at t_{AVQV}.

AC ELECTRICAL CHARACTERISTICS (over the operating range)

READ CYCLE

JEDEC PARAMETER NAME	PARAMETER NAME	PARAMETER	-20		-22		-25		UNIT	NOTES
			Min.	Max.	Min.	Max.	Min.	Max.		
t_{AVAV}	t_C	Cycle Time	25		25		30		ns	
t_{AVQV}	t_{AA}	Address Access Time		25		25		30	ns	
t_{AXQX}	t_{AOH}	Address Output Hold Time	5		5		5		ns	
t_{EVQV}	t_{EA}	Chip Enable Access Time		25		25		30	ns	
t_{EXQX}	t_{EOH}	Chip Enable Output Hold Time	4		4		4		ns	
t_{EVQX}	t_{ELZ}	Chip Enable TRUE to Low-Z	4		4		4		ns	
t_{EXQZ}	t_{EHZ}	Chip Enable FALSE to High-Z		8		8		10	ns	
t_{SLQV}	t_{SA}	Chip Select Access Time		15		15		18	ns	
t_{SHQX}	t_{SOH}	Chip Select Output Hold Time	2		2		2		ns	
t_{SLQX}	t_{SLZ}	Chip Select to Low-Z	3		3		3		ns	
t_{SHQZ}	t_{SHZ}	Chip Select to High-Z		4		4		6	ns	
t_{GLQV}	t_{GA}	Output Enable Access Time		13		13		15	ns	
t_{GHQX}	t_{GOH}	Output Enable Output Hold Time	2		2		2		ns	
t_{GLQX}	t_{GLZ}	Output Enable to Low-Z	2		2		2		ns	
t_{GHQZ}	t_{GHZ}	Output Enable to High-Z		5		5		8	ns	

READ CYCLE

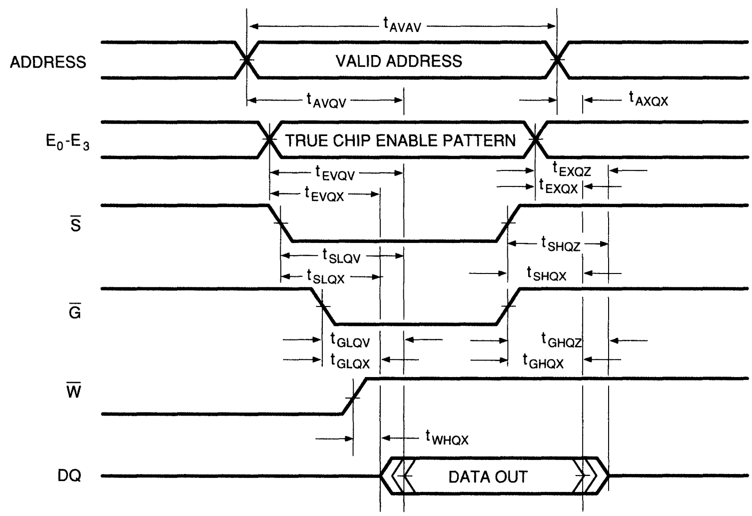


Figure 1

ADDRESS READ CYCLE

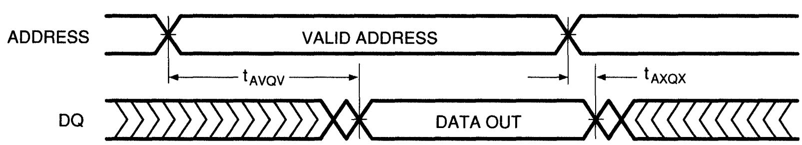


Figure 2

CHIP ENABLE READ CYCLE

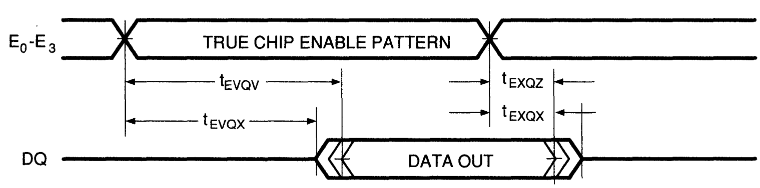


Figure 3

CHIP SELECT READ CYCLE

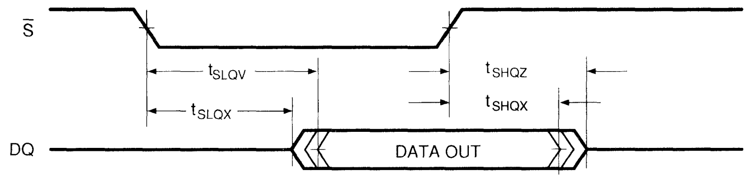


Figure 4

OUTPUT ENABLE READ CYCLE

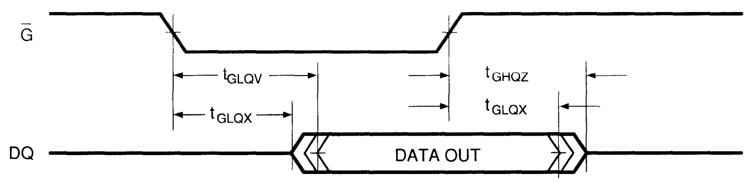


Figure 5

WRITE MODE

The MS8202 is in the Write mode whenever $\overline{W}$ is LOW provided Chip Select ($\overline{S}$) is LOW and a true Chip Enable pattern (E_0 - E_3) is applied ($\overline{G}$ may be in either logic state). Addresses must be held valid throughout a write cycle, with either $\overline{W}$ or $\overline{S}$ inactive HIGH during address transitions. $\overline{W}$ may fall with stable addresses, but must remain valid for t_{WLWH}. Since the write begins with the concurrence of $\overline{W}$ and $\overline{S}$, should $\overline{W}$ become active first, then t_{SLSH} must be satisfied. Either $\overline{W}$ or $\overline{S}$ can terminate the write cycle, therefore t_{DVWH} or t_{DVSH} must be satisfied before the earlier rising edge. If the outputs are active with $\overline{G}$ and $\overline{S}$ asserted LOW and with true Chip Enable, then $\overline{W}$ will return the outputs to high impedance within t_{WLHZ} of its falling edge.

ELECTRICAL CHARACTERISTICS (over the operating range)

WRITE CYCLE

JEDEC PARAMETER NAME	PARAMETER NAME	PARAMETER	-20		-22		-25		UNIT	NOTES
			Min.	Max.	Min.	Max.	Min.	Max.		
t_{AVAV}	t_C	Cycle Time	25	–	25		30		ns	
t_{AVWL}	t_{AS}	Address Set-up Time to $\overline{W}$ LOW	0	–	0		0		ns	
t_{WHAX}	t_{AH}	Address Hold Time from $\overline{W}$ HIGH	0	–	0		0		ns	
t_{AVSL}	t_{AS}	Address Set-up Time to $\overline{S}$ LOW	0	–	0		0		ns	
t_{SHAX}	t_{AH}	Address Hold Time from $\overline{S}$ HIGH	0	–	0		0		ns	
t_{EVWL}	t_{ES}	Chip Enable Set-up Time to $\overline{W}$ LOW	3	–	3		3		ns	
t_{WHEX}	t_{EH}	Chip Enable Hold Time from $\overline{W}$ HIGH	0	–	0		0		ns	
t_{EVSL}	t_{ES}	Chip Enable Set-up Time to $\overline{S}$ LOW	3	–	3		3		ns	
t_{SHEX}	t_{EH}	Chip Enable Hold Time to $\overline{S}$ HIGH	0	–	0		0		ns	
t_{WLWH}	t_{WW}	Write Pulse Width	15	–	15		18		ns	
t_{SLSH}	t_{SW}	Chip Select Pulse Width	16	–	16		20		ns	
t_{DVWH}	t_{DS}	Data Set-up Time to $\overline{W}$ HIGH	12	–	12		15		ns	
t_{WHDX}	t_{DH}	Data Hold Time from $\overline{W}$ HIGH	0	–	0		0		ns	
t_{DVSH}	t_{DS}	Data Set-up Time to $\overline{S}$ HIGH	12	–	12		15		ns	
t_{SHDX}	t_{DH}	Data Hold Time from $\overline{S}$ HIGH	0	–	0		0		ns	
t_{WLQZ}	t_{WZ}	Outputs Hi-Z from $\overline{W}$ LOW	–	8		8		10	ns	
t_{WHQX}	t_{WL}	Outputs Low-Z from $\overline{W}$ HIGH	5	–	5		5		ns	

6

WRITE ENABLE CONTROLLED WRITE CYCLE

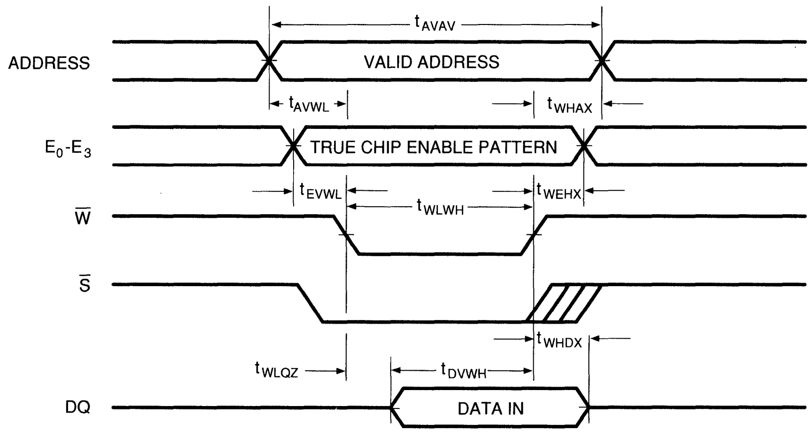


Figure 6

CHIP SELECT CONTROLLED WRITE CYCLE

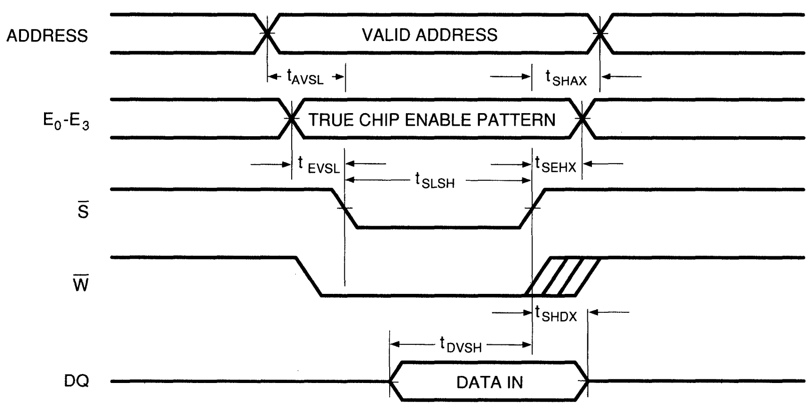


Figure 7

COMPARE MODE

The MS8202 is in the Compare mode whenever $\overline{W}$ and $\overline{G}$ are HIGH provided a true Chip Enable (E_0 - E_3) pattern is applied. Chip Select ($\overline{S}$) is regarded as a don't care since the user is not concerned with the data outputs, but only with the Compare (C_X) outputs. $\overline{M}_X$ and $\overline{H}_X$ must be HIGH, and CG_X active LOW to enable the Compare outputs for a valid compare hit or miss.

The 11 index address inputs (A_0-A_{10}) define a unique location in the static RAM array. The data presented on the Data Inputs (DQ_1-DQ_{19} and CDQ_0) as Tag Data is compared to the internal RAM data as specified by the index. If all bits are equal (match) then a hit condition occurs (C_X = HIGH). If at least one bit is not equal, then a miss occurs (C_X = LOW).

The Compare output will be valid t_{AVCV} from stable address, or t_{DVCV} from valid tag data provided Chip Enable is true, and CG_X is active LOW. Should the address be stable with valid tag data, and Chip Enable false, then compare access will be within t_{EVCV} from true Chip Enable. When executing a write-to-compare cycle ($\overline{W}$ = LOW, and $\overline{G}$ = LOW or HIGH, C_X will be valid t_{WHCV} or t_{GHCV} from the latter rising edge of W or G respectively. Finally, when gating the C_X output in the compare mode with CG_X, the compare output will be valid $t_{CGL\text{-}CV}$ from the falling edge of CG_X.

ELECTRICAL CHARACTERISTICS (over the operating range)

COMPARE CYCLE

JEDEC PARAMETER NAME	PARAMETER NAME	PARAMETER	-20 Min.	-20 Max.	-22 Min.	-22 Max.	-25 Min.	-25 Max.	UNIT	NOTES
t_{AVCV}	t_{ACA}	Cycle Address Compare Access Time		20		22		25	ns	
t_{AXCX}	t_{ACOH}	Address Compare Output Hold Time	5		5		5		ns	
t_{DVCV}	t_{DCA}	Tag Data Compare Access Time		16		18		20	ns	
$t_{DX\,CX}$	t_{DCH}	Tag Data Compare Hold Time	2		2		2		ns	
t_{WLCH}	t_{WCH}	$\overline{W}$ LOW to Compare HIGH		10		11		12	ns	
t_{WHCH}	t_{WCOH}	$\overline{W}$ Compare Output hold Time	3		3		3		ns	
t_{WLCX}	t_{WLCZ}	$\overline{W}$ to Compare HOLD	3		3		3		ns	
t_{WHCV}	t_{WCV}	$\overline{W}$ to Compare Valid		10		10		12	ns	
t_{GLCH}	t_{GCH}	$\overline{G}$ Low to Compare HIGH		10		11		12	ns	
t_{GHCX}	t_{CGOH}	$\overline{G}$ Compare Output Hold Time	3		3		3		ns	
t_{GLCX}	t_{GLCZ}	$\overline{G}$ to Compare to HOLD	3		3		3		ns	
t_{GHCV}	t_{GCV}	$\overline{G}$ to Compare Valid		10		10		12	ns	
t_{EVCV}	t_{ECA}	E True to Compare Access Time		20		22		25	ns	
t_{EXCX}	t_{ECOH}	E False Compare Hold Time	4		4		4		ns	
t_{EVCX}	t_{ECLZ}	E True to Compare Low-Z	4		4		4		ns	
t_{EXCZ}	t_{ECHZ}	E False to Compare high-Z		8		8		10	ns	
$t_{CGL\text{-}CV}$	t_{CGA}	$\overline{CG}_X$ to Compare Access Time		8		8		10	ns	
$t_{CGH\text{-}CX}$	t_{CGOH}	$\overline{CG}_X$ to Compare Hold Time	2		2		2		ns	
$t_{CGL\text{-}CX}$	t_{CGLZ}	$\overline{CG}_X$ LOW to Compare low-Z	2		2		2		ns	
$t_{CGH\text{-}CZ}$	t_{CGHZ}	$\overline{CG}_X$ HIGH to Compare High-Z		8		8		10	ns	

6

SUMMARY COMPARE CYCLE

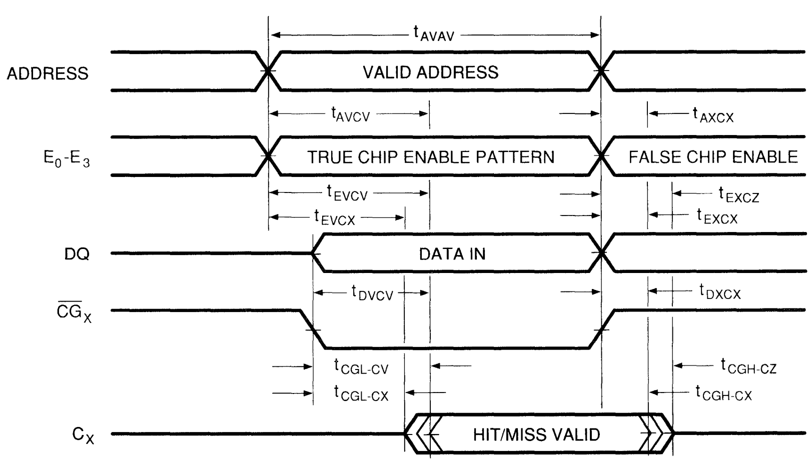


Figure 8

Note:

$\overline{W}$ and $\overline{G}$ are both assumed to be HIGH.

$\overline{H}_x$ and $\overline{M}_x$ are both assumed to be HIGH.

COMPARE CYCLE

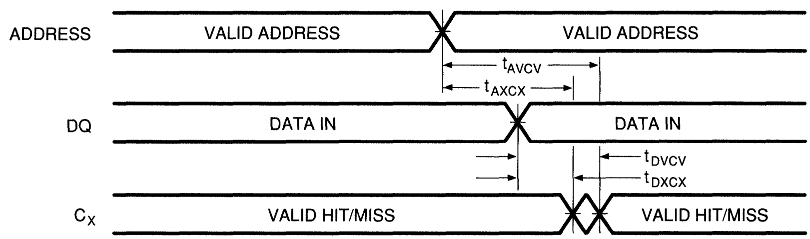


Figure 9

Note:
$\overline{W}$ and $\overline{G}$ are both HIGH, $\overline{CG_X}$ is LOW, and a true Chip Enable pattern is present. $\overline{H_X}$ and $\overline{M_X}$ are both assumed to be HIGH.

RESET MODE

The MS8202 allows an asynchronous reset whenever $\overline{RS}$ is LOW regardless of the logic state on the other input pins. Reset clears all internal RAM bits in CDQ_0 (2048 bits) to a logic zero. This output can be used as a valid tag bit to insure a valid compare miss or hit. It should be noted that a valid write cycle is not allowed during a reset cycle ($\overline{W}$ = LOW, $\overline{S}$ = LOW, $\overline{RS}$ = LOW, and Chip Enable is true). The state of the data outputs is determined by the input control logic pins: Chip Enable, $\overline{S}$, $\overline{G}$, and $\overline{W}$ (see truth table). Should a reset occur during a valid compare cycle, and the CDQ_0 valid tag bit is set to a logic (1), then C_X will go LOW at t_{RSL-CL} from the falling edge of $\overline{RS}$.

ELECTRICAL CHARACTERISTICS (over the operating range)

RESET CYCLE

JEDEC PARAMETER NAME	PARAMETER NAME	PARAMETER	-20 Min.	-20 Max.	-22 Min.	-22 Max.	-25 Min.	-25 Max.	UNIT	NOTES
$t_{RLSL-AV}$	t_{RSC}	Reset Cycle Time	20		25		30		ns	
$t_{RSL-RSH}$	t_{RSW}	Reset pulse Width	25		25		30		ns	
t_{RSL-CL}	t_{RSCL}	RS LOW to Compare Output LOW		25		25		30	ns	
t_{RSH-AV}	t_{RSR}	Address Recovery Time	0		0		0		ns	
t_{RSH-EV}	t_{RSR}	Chip Enable Recovery Time	0		0		0		ns	

RESET CYCLE

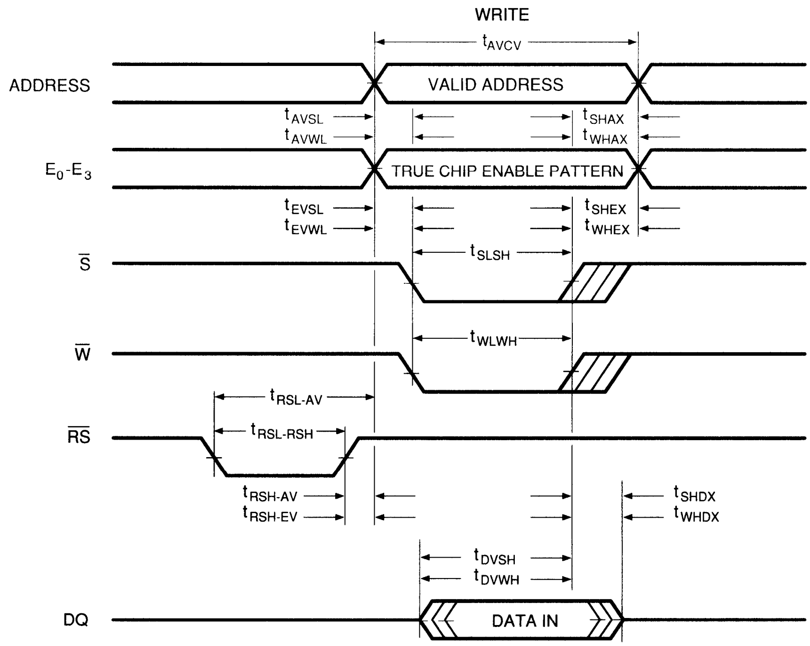


Figure 10

Note: Reset during an active write cycle is not allowed. A write cycle may disrupt Reset, but will not damage device.

VALID COMPARE - RESET

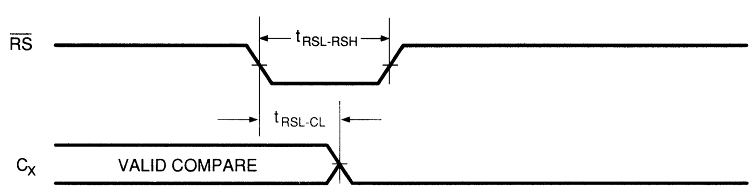


Figure 11

Note: CDQ_0 is presumed to be HIGH.

6

FORCE HIT AND FORCE MISS

The MS8202 can force either a miss or hit condition on the C_X output by asserting $\overline{M}_X$ or $\overline{H}_X$ LOW. A Force Miss overrides a Force Hit condition and is not dependent upon Compare Output Enable ($\overline{CG}_X$) (see truth table).

The $\overline{C}_X$ output will go HIGH within $t_{\overline{HLCH}}$ from the falling edge of $\overline{H}_X$ or $\overline{C}_X$ will go LOW within $t_{\overline{MLCL}}$ from the falling edge of $\overline{M}_X$. All $\overline{M}_X$ and $\overline{H}_X$ inputs must be HIGH during a valid compare cycle.

ELECTRICAL CHARACTERISTICS (over the operating range)

FORCE HIT OR MISS CYCLE

JEDEC PARAMETER NAME	PARAMETER NAME	PARAMETER	-20 Min.	-20 Max.	-22 Min.	-22 Max.	-25 Min.	-25 Max.	UNIT	NOTES
t_{HLCH}	t_{HA}	$\overline{H}_X$ to Force Hit Access Time		8		8		10	ns	
t_{HHCV}	t_{HHZ}	$\overline{H}_X$ to Compare High-Z		5		5		8	ns	
$t_{HL\text{-}CGX}$	t_{HS}	Force hit to $\overline{CG}_X$ don't care	2		2		2		ns	
$t_{HH\text{-}CGH}$	t_{HR}	Force hit to $\overline{CG}_X$ recognized	2		2		2		ns	
t_{MLCL}	t_{MA}	$\overline{M}_X$ to Force Miss Access Time		8		8		10	ns	
t_{MHCZ}	t_{MHZ}	$\overline{M}_X$ to Compare to high-Z		5		5		8	ns	
$t_{ML\text{-}CGX}$	t_{MS}	Force Miss to $\overline{CG}_X$ don't care	2		2		2		ns	
$t_{MH\text{-}CGH}$	t_{MR}	Force Miss to $\overline{CG}_X$ recognized	2		2		2		ns	
t_{MLHX}	t_{MHS}	Force Miss to $\overline{H}_X$ don't care	2		2		2		ns	
t_{MHHH}	t_{MHR}	Force Miss to $\overline{H}_X$ recognized	2		2		2		ns	

FORCE HIT AND FORCE MISS

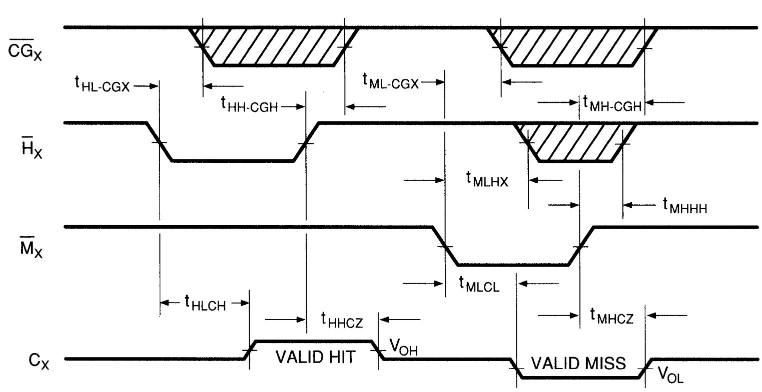


Figure 12

LATE WRITE - HIT CYCLE

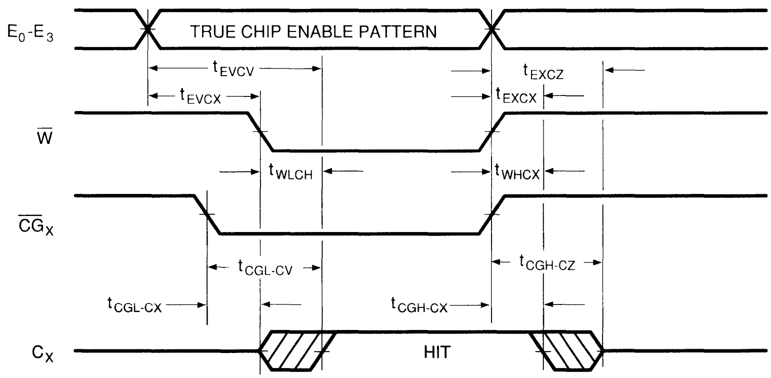


Figure 13

Note: $\overline{G}$ is HIGH and aValid Address is present, $\overline{H}_x$ and $\overline{M}_x$ are both assumed to be HIGH, with $\overline{CG}_x$ LOW.

COMPARE - WRITE HIT - COMPARE CYCLE

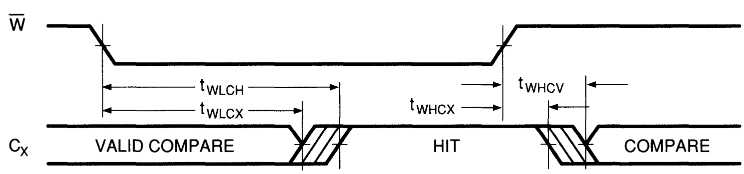


Figure 14

Note: $\overline{G}$ is HIGH and a Valid Address is present, $\overline{H}_x$ and $\overline{M}_x$ are both assumed to be HIGH, with $\overline{CG}_x$ LOW, with $\overline{CG}_x$ LOW.

6

LATE READ - HIT CYCLE

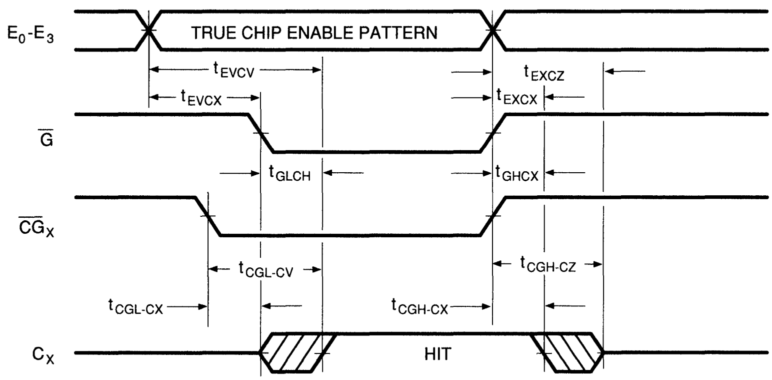


Figure 15

Note: $\overline{W}$ is HIGH and a Valid Address is present, $\overline{H}_x$ and $\overline{M}_x$ are both assumed to be HIGH, (with $\overline{CG}_x$ LOW.)

COMPARE - READ HIT - COMPARE CYCLE

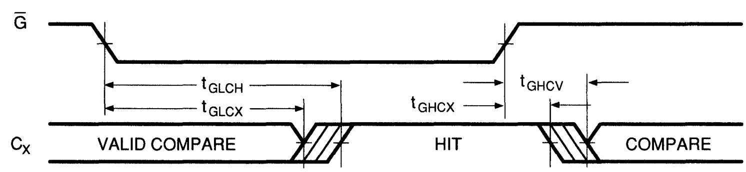


Figure 16

Note: $\overline{W}$ is HIGH and a Valid Address is present, $\overline{H}_x$ and $\overline{M}_x$ are both assumed to be HIGH, with $\overline{CG}_x$ LOW.

EARLY WRITE - HIT CYCLE

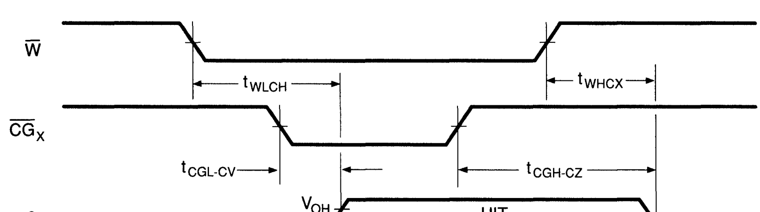


Figure 17

Note: $\overline{G}$ is HIGH and a Valid Address is present, with $(E_0 - E_3)$ = True. $\overline{H}_x$ and $\overline{M}_x$ are both assumed to be HIGH.

EARLY READ - HIT CYCLE

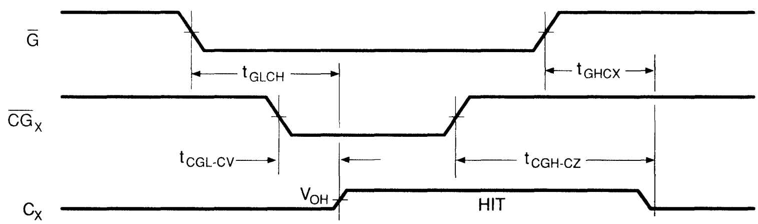


Figure 18

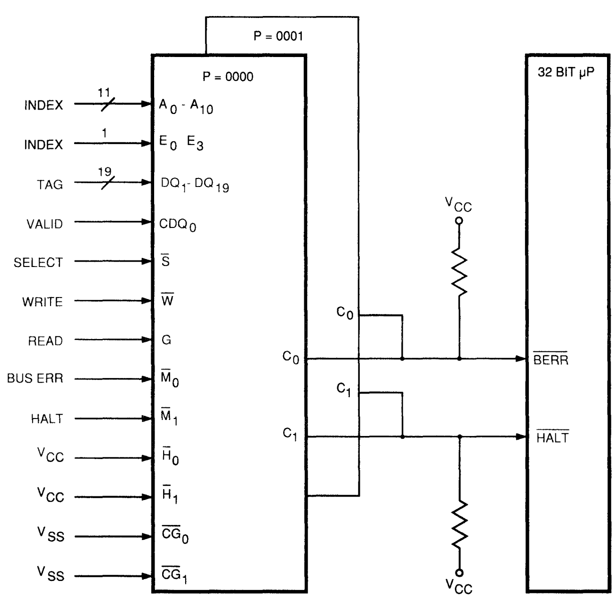
Note: $\overline{W}$ is HIGH and a Valid Address is present, with ($E_0 - E_3$) = True. $\overline{H}_x$ and $\overline{M}_x$ are both assumed to be HIGH.

POWER DISTRIBUTION

The MOSEL MS8202 being a 20 output device, obviously requires the use of good power bussing techniques. The MS8202 has been designed in such a way as to allow the user to minimize the effects of switching transients on overall circuit operation. Of particular interest is the separate bussing of the V_{CC} and V_{SS} lines to the output drivers. The advantage provided by these separate power pins, designated V_{CCQ} and V_{SSQ}, is that voltage sags and ground bumps seen on these pins are not reflected into the other portions of the chip, particularly the input structures. As a result, switching noise in the supply has much less effect on input levels, providing the user with more noise margin than would otherwise be available.

Of course V_{CC} and V_{CCQ} must always be at the same DC potential. V_{SS} and V_{SSQ} must match as well. Differences between them due to AC effects are expected, but must be minimized through the adequate use of bussing and bypassing. All specifications and testing are done with $V_{SS} = V_{SSQ} \pm 10$mV RMS, $V_{CC} = V_{CCQ} \pm 10$mV RMS with instantaneous peak differences not exceeding 50 mV.

APPLICATION BLOCK SCHEMATIC



ORDERING INFORMATION

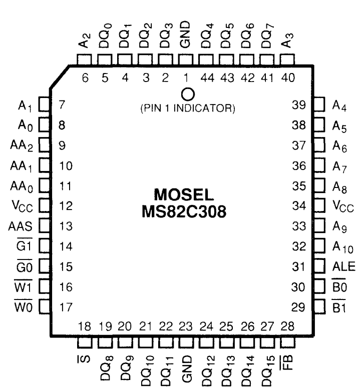
SPEED (ns)	ORDERING PART NUMBER	PACKAGE REFERENCE NO.	TEMPERATURE RANGE
20	MS8202-20JC	J68-1	0°C to + 70°C
22	MS8202-22JC		0°C to + 70°C
25	MS8202-25JC		0°C to + 70°C

2 x 2K x 16 Cache Data RAM

FEATURES

- Supports 16 bit wide 80286 and 32 bit wide 80386 system cache data requirements directly.
- High speed access supports 16/20/25 MHz 80386 systems.
- On-board x16 SRAM organized as 2 sets of 2K x 16.
- On-board address latches support pipelined accesses with no external components.
- Easliy supports 2-way and 4-way set associative cache subsystems.
- Supports both pipelined and non-pipelined cycles.
- 16 bit bi-directional data path.
- Built-in alternate address multiplexer allows quick word selection during line replacement.
- Interfaces directly with Intel 82385, Chips & Technologies 82C307/82C327 and other cache controllers.
- Significantly reduces board real estate required for cache data storage.
- Packaged in JEDEC standard 44 terminal PLCC.

PIN CONFIGURATIONS



DESCRIPTION

The MOSEL 82C308 is a high performance CMOS static RAM optimized for use as cache subsystem data buffers in 80386 and 80286 systems. The device has a full 16 bit wide bi-directional data path, and is configured as 2 banks of 2K x 16 memory. This configuration offers significant design, density and power advantages over designs using traditional RAM architectures in caches for these systems.

The MS82C308 is available with fast address access times down to 35ns (max), and with very fast output enable times (12ns max.), and supports 80386 systems up to 25 MHz. The MS82C308 contains all the logic on-board to interface directly with the Intel 82385, Chips & Technologies 82C307/82C327 and other cache controllers. Its' on-board address latches allow it to support both pipelined and non-pipelined memory accesses. An additional on-board alternate address multiplexer is provided to allow fast selection or words during line replacement.

For a 32 bit 80386 system with a 16KB cache, only 2 devices are needed. For a 32 bit 80386 system with a full 32KB cache, only 4 MS82C308 devices are needed, replacing the standard requirement of 16 4K x 4 SRAMS and additional discrete logic. This offers a significant reduction in board real estate, power, cost and capacitive loading.

The MS82C308 is manufactured in MOSEL's high performance CMOS process and operates from a single 5V power supply. All inputs and outputs are TTL compatible. The device is supplied in a space saving JEDEC standard 44 terminal PLCC package.

SPEED SELECTION

80386 SPEED	RECOMMENDED MS82C308
16MHz	–55
20MHz	–45
25MHz	–35

PIN DESCRIPTIONS

A_0 - A_{10} Address Inputs

These 11 address inputs select one of the 2048 16-bit words in each RAM bank.

AA_0 - AA_2 Alternate Address Inputs

These 3 alternate address inputs are used to select words within the same page. They are used in conjuction with AAS.

AAS Alternate Address Select

This pin is active high. When LOW, address inputs A_0-A_2 will be input to the array; when HIGH, alternate address inputs AA_0-AA_2 will be input to the array.

ALE Address Latch Enable

This active HIGH pin controls the internal transparent latches on pins A_0-A_{11}. When ALE is HIGH the latch is transparent and the inputs on the address pins are applied to the memory array. On the falling edge of ALE the current input states of pins A_0-A_{11} are latched and remain applied to the memory array until ALE returns to the active HIGH state.

$\overline{G0}$ Output Enable 0 Input
$\overline{G1}$ Output Enable 1 Input

These output enables are active LOW. $\overline{G}_0$ active will enable data output from Bank 0, while $\overline{G}_1$ will enable data output from Bank 1. These two pins can not both be active simultaneously. The DQ pins will be in the high-impedance state when deselected.

$\overline{S}$ Chip Select Input

This pin is active low. The DQ pins will be in the high-impedance state when deselected.

$\overline{B0}$ Byte Enable 0 Input
$\overline{B1}$ Byte Enable 1 Input

These pins are active LOW. During a write operation, these pins select whether the upper or lower byte of the addressed 16-bit word will be written.

$\overline{FB}$ Force Byte Enable Input

This pin is active LOW. If the $\overline{FB}$ pin is active during a write operation, both the upper and low bytes of the addressed 16-bit word will be written.

$\overline{W0}$ Write Enable 0 Input
$\overline{W1}$ Write Enable 1 Input

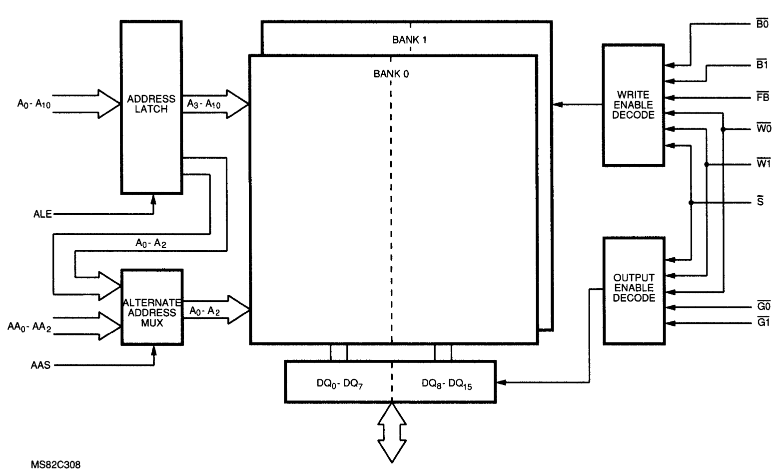
The chip is selected and either byte enable input or the force byte enable input is active, bring a write enable pin active will cause the data present on the DQ pins to be written into the selected bank.

DQ_0-DQ_{15} Data Input/Output Ports

These 16 bidirectional ports are used to read data from or write data into the RAM.

V_{CC} Power Supply
GND Ground

FUNCTIONAL BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The MS82C308 is a high performance CMOS static RAM intended for use as a data buffer in caches for 80386 or 80286 systems. A two byte wide data path is provided for use in 16 and 32 bit systems. The array is configured as two banks to allow a fast output enable to be generated by a search of the cache directory concurrent with the data buffer access. It replaces four 4K x 4 or 2K x 8 chips and several TTL MSI and SSI chips with a small footprint 44 pin PLCC. In addition, power, cost and capacitive loading are significantly reduced.

Two chips are needed for a 32 bit 80386 system with a 16KB cache while a single chip can be used to implement and 8KB 80286 cache. The arrays could be doubled to implement a 4-way set associative system if desired.

For a 32 bit 80386 system with a full 32KB cache, four MS82C308 chips would be needed. The cache depth can be expanded as desired. For example, for a system with a 64KB cache, 8 MS82C308's are needed.

Address Latch

An on-board address latch is used to store the address directly from the 80386 local address bus. Two different modes of operations (pipelined cycle vs. non-pipelined cycle) are possible in an 80386 based system. The transparent address latch is enabled by the ALE pin. In non-pipelined accesses, the address will change during the ALE cycle. In pipelined accesses the address will change before the rising edge of ALE.

The access time in non-pipelined cycles will be determined by address access time, while it will be measured from the rising edge of ALE in pipe-lined cycles.

Alternate Address Multiplexer

A 3 bit multiplexer is provided to allow selection of words within the same block of 2, 4 or 8 words. This is necessary in cache systems when the line or sub-line (unit of memory that is replaced) is greater than one word.

RAM Array

The RAM is logically configured as two banks of 2K words of 2 bytes. Both banks are always accessed simultaneously; the two output enables are used to select which word is outputted to the data bus.

Output Enable Decode

Two $\overline{G}$ inputs are provided, one for each bank. $\overline{G0}$ will gate the data from first bank and $\overline{G1}$ will gate the data from second bank. If either of the two write enable signals are active, the output enable signals will be overridden to prevent the 82C308 from driving the bus. Two $\overline{G}$'s ($\overline{G0}$ and $\overline{G1}$) inputs can not be active at the same time. Otherwise, undetermined results would appear at the 16 data outputs.

Write Enable Decode

Two $\overline{W}$ inputs are provided, one for each bank. When either of the write enables are asserted, the array outputs are disabled to prevent driver conflicts. Individual byte enables are provided that control the writes in either or both of the two bytes of the 82C308. The $\overline{FB}$ input is provided to allow forcing both byte write enables during a move-in (fetch) operation. This eliminates the external gating of write enable required in a store-in cache implementation.

Array Expansion

A chip select input ($\overline{S}$) is provided to allow for expansion of the cache array in the vertical (more words) dimension. The access time from chip select is less than the address to data time to allow for external decoding circuitry.

Set Associativity

While the MS82C308 is intended to be used in a two-way set associative cache implementation, it is very simple to increase the size of the cache by increasing the associativity to 4 or more ways by paralleling MS82C308's (2 for 4 way, 4 for 8 way, etc).

TRUTH TABLE

	INPUTS										OUTPUTS		FUNCTION
	ALE	AAS	$\overline{G0}$	$\overline{G1}$	$\overline{S}$	$\overline{B0}$	$\overline{B1}$	$\overline{FB}$	$\overline{W0}$	$\overline{W1}$	DQ_0-DQ_7	DQ_8-DQ_{15}	
1	X	X	X	X	H	X	X	X	X	X	HI-Z	HI-Z	Deselected
2	X	X	H	H	L	H	H	H	H	H	HI-Z	HI-Z	Outputs Disabled
3	L	X	–	–	–	–	–	–	–	–	–	–	Address Latch Enabled
4	H	X	–	–	–	–	–	–	–	–	–	–	Address Latch Transparent
5	X	H	–	–	–	–	–	–	–	–	–	–	Alternate Address Selected
6	H	X	L	H	L	H	H	H	H	H	D_{OUT}	D_{OUT}	Read Current Address (Bank 0)
7	H	X	H	L	L	H	H	H	H	H	D_{OUT}	D_{OUT}	Read Current Address (Bank 1)
8	L	L	L	H	L	H	H	H	H	H	D_{OUT}	D_{OUT}	Read Latched Address (Bank 0)
9	L	L	H	L	L	H	H	H	H	H	D_{OUT}	D_{OUT}	Read Latched Address (Bank 1)
10	X	H	L	H	L	H	H	H	H	H	D_{OUT}	D_{OUT}	Read Alternate Address (Bank 0)
11	X	H	H	L	L	H	H	H	H	H	D_{OUT}	D_{OUT}	Read Alternate Address (Bank 1)
12	H	X	X	X	L	L	H	H	L	H	D_{IN}	HI-Z	Write to Lower Byte of Current Address (Bank 0)
13	H	X	X	X	L	H	L	H	L	H	HI-Z	D_{IN}	Write to Upper Byte of Current Address (Bank 0)
14	H	X	X	X	L	L	L	H	L	H	D_{IN}	D_{IN}	Write to Both Bytes of Current Address (Bank 0)
15	H	X	X	X	L	X	X	L	L	H	D_{IN}	D_{IN}	Write to Both Bytes of Current Address (Bank 0)
16	H	X	X	X	L	L	H	H	H	L	D_{IN}	HI-Z	Write to Lower Byte of Current Address (Bank 1)
17	H	X	X	X	L	H	L	H	H	L	HI-Z	D_{IN}	Write to Upper Byte of Current Address (Bank 1)
18	H	X	X	X	L	L	L	H	H	L	D_{IN}	D_{IN}	Write to Both Bytes of Current Address (Bank 1)
19	H	X	X	X	L	X	X	L	H	L	D_{IN}	D_{IN}	Write to Both Bytes of Current Address (Bank 1)
20	L	L	X	X	L	L	H	H	L	H	D_{IN}	HI-Z	Write to Lower Byte of Latched Address (Bank 0)
21	L	L	X	X	L	H	L	H	L	H	HI-Z	D_{IN}	Write to Upper Byte of Latched Address (Bank 0)
22	L	L	X	X	L	L	L	H	L	H	D_{IN}	D_{IN}	Write to Both Bytes of Latched Address (Bank 0)
23	L	L	X	X	L	X	X	L	L	H	D_{IN}	D_{IN}	Write to Both Bytes of Latched Address (Bank 0)
24	X	H	X	X	L	L	H	H	L	H	D_{IN}	HI-Z	Write to Lower Byte of Alternate Address (Bank 0)
25	X	H	X	X	L	H	L	H	L	H	HI-Z	D_{IN}	Write to Upper Byte of Alternate Address (Bank 0)
26	X	H	X	X	L	L	L	H	L	H	D_{IN}	D_{IN}	Write to Both Bytes of Alternate Address (Bank 0)
27	X	H	X	X	L	X	X	L	L	H	D_{IN}	D_{IN}	Write to Both Bytes of Alternate Address (Bank 0)
28	L	L	X	X	L	L	H	H	H	L	D_{IN}	HI-Z	Write to Lower Byte of Latched Address (Bank 1)
29	L	L	X	X	L	H	L	H	H	L	HI-Z	D_{IN}	Write to Upper Byte of Latched Address (Bank 1)
30	L	L	X	X	L	L	L	H	H	L	D_{IN}	D_{IN}	Write to Both Bytes of Latched Address (Bank 1)
31	L	L	X	X	L	X	X	L	H	L	D_{IN}	D_{IN}	Write to Both Bytes of Latched Address (Bank 1)
32	X	H	X	X	L	L	H	H	H	L	D_{IN}	HI-Z	Write to Lower Byte of Alternate Address (Bank 1)
33	X	H	X	X	L	H	L	H	H	L	HI-Z	D_{IN}	Write to Upper Byte of Latched Address (Bank 1)
34	X	H	X	X	L	L	L	H	H	L	D_{IN}	D_{IN}	Write to Both Bytes of Alternate Address (Bank 1)
35	X	H	X	X	L	X	X	L	H	L	D_{IN}	D_{IN}	Write to Both Bytes of Alternate Address (Bank 1)

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	CONDITION	UNIT
V_{TERM}	Terminal Voltage with Repect to GND	–0.5 to +7.0	V
t_{BIAS}	Temperature Under Bias	–10 to +125	°C
t_{STG}	Storage Temperature	–60 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	20	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

RANGE	AMBIENT TEMPERATURE	Vcc
Commercial	0°C to + 70°C	5V ± 5%

DC ELECTRICAL CHARACTERISTICS (over the commercial operating range)

PARAMETER NAME	PARAMETER	TEST CONDITIONS	MIN.	TYP. (1)	MAX.	UNITS
V_{IL}	Guaranteed Input Low Voltage (2)(3)		–0.5	–	0.8	V
V_{IH}	Guaranteed Input High Voltage(2)		2.0	–	6.0	V
I_{IL}	Input Leakage Current	V_{CC} = Max, V_{IN} = 0V to V_{CC}	–	–	2	µA
I_{OL}	Output Leakage Current	V_{CC} = Max, $\overline{G0} = V_{IH}$, $\overline{G1} = V_{IH}$, V_{IN} = 0V to V_{CC}	–	–	10	µA
V_{OL}	Output Low Voltage	V_{CC} = Min, I_{OL} = 8mA	–	–	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min, I_{OH} = – 4mA	2.4	–	–	V
I_{CC}	Operating Power Supply Current	V_{CC} = Max, $\overline{G0} = V_{IL}$ or $\overline{G1} = V_{IL}$, $\overline{S} = V_{IL}$ $I_{I/O}$ = 0mA, F = F_{MAX}(4)	–	–	150	mA

NOTES:
1. Typical characteristics are at V_{CC} = 5.0V, t_A = 25°C.
2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
3. $V_{IL(MIN)}$ = –3.0 for pulse width < 20ns.
4. $F_{MAX} = 1/t_{RC}$

CAPACITANCE[1] (T_A = 25°C, f = 1.0MHz)

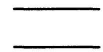
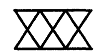
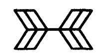
SYMBOL	PARAMETER	CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{DQ}	Input/Output Capacitance	V_{DQ} = 0V	8	pF

1. This parameter is guaranteed and not tested.

AC TEST CONDITIONS

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5 ns
Input and Output Timing Reference Level	1.5V

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

AC TEST LOADS AND WAVEFORMS

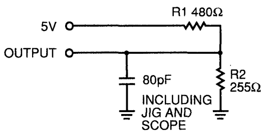


Figure 1a

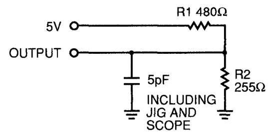
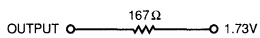


Figure 1b

Equivalent to:

THEVENIN EQUIVALENT



ALL INPUT PULSES

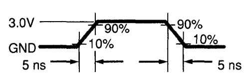


Figure 2

AC ELECTRICAL CHARACTERISTICS (over the operating range)

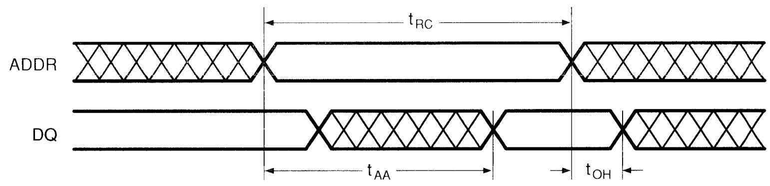
READ CYCLE

JEDEC PARAMETER NAME	PARAMETER NAME	PARAMETER	MS82C308-35			MS82C308-45			MS82C308-55			UNITS
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
t_{AVAX}	t_{RC}	Read Cycle Time	35		–	45		–	55		–	ns
t_{AVQV}	t_{AA}	Address Access Time			35			45			55	ns
t_{SLQV}	t_{ACS}	Chip Select Access Time			25			35			45	ns
t_{GLQV}	t_{OE}	Output Enable to Output Valid			12			15			18	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output Low Z	2		10	2		15	2		20	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z	2		15	2		15	2		15	ns
t_{SLQX}	t_{CLZ}	Chip Select to Output in Low Z	2		10	2		15	2		20	ns
t_{SHQZ}	t_{CHZ}	Chip Deselect to Output in High Z	0		20	0		20	0		20	ns
t_{AXQX}	t_{OH}	Output Hold from Address Change	5		–	5		–	5		–	ns
	t_{CPWH}	ALE Width High	10		–	12		–	15		–	ns
	t_{CPWL}	ALE Width Low	10		–	12		–	15		–	ns
	t_{AS}	Address Latch Setup Time	3		–	3		–	3		–	ns
	t_{AH}	Address Latch Hold Time	5		–	5		–	5		–	ns
	t_{AALE}	Access Time from ALE	–		45	–		55	–		55	ns
	t_{SAA}	AAS to Alternate Address Setup Time	3		–	3		–	3		–	ns
	t_{AAA}	Access Time from AAS or Alternate Address	–		35	–		35	–		35	ns
	t_{OHAA}	Output Hold from AA, AAS Change	3		–	3		–	3		–	ns

SWITCHING WAVEFORMS (READ CYCLE)

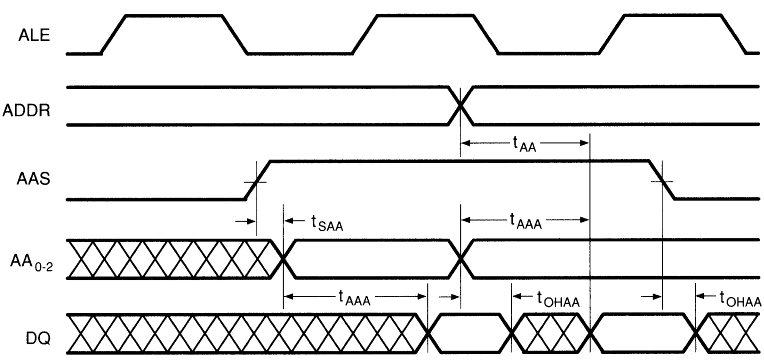
READ CYCLE 1 (1,2,3,4,5)

ADDRESS ACCESS TIME - NON-PIPELINE



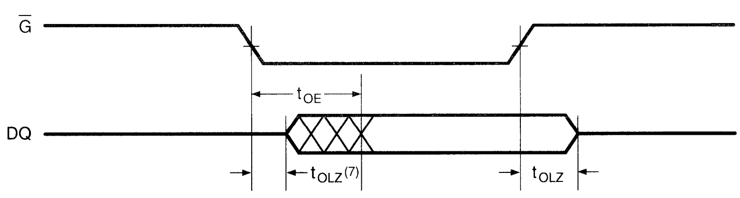
READ CYCLE 2 (1,3,4)

ALTERNATE ADDRESS ACCESS



READ CYCLE 3 (1,3,6)

OUTPUT ENABLE ACCESS

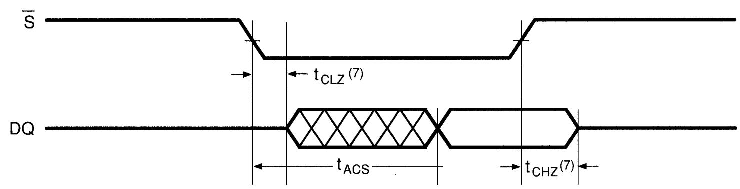


6

SWITCHING WAVEFORMS (READ CYCLE)

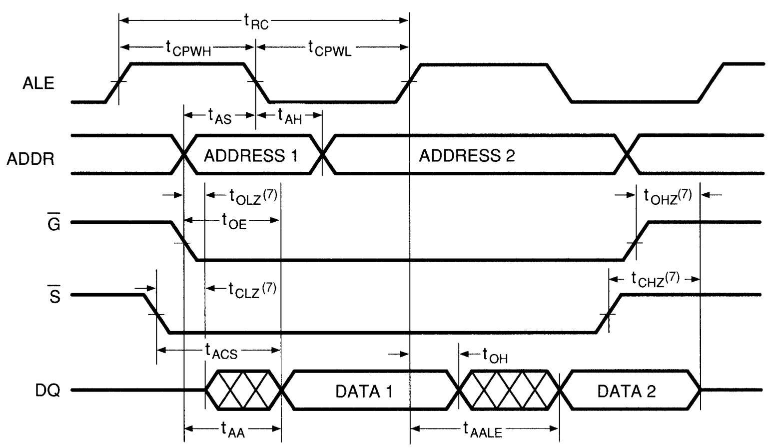
READ CYCLE 4(1,4,6)

CHIP SELECT ACCESS



READ CYCLE 5(1)

PIPELINED



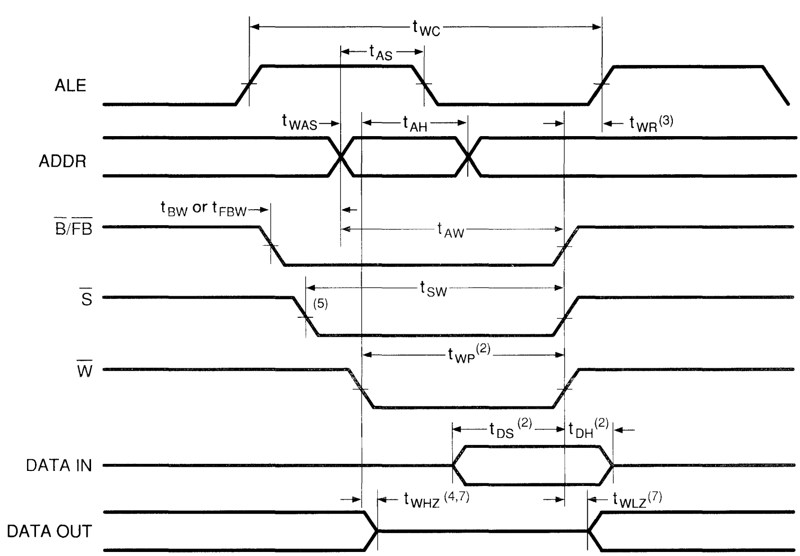
NOTES:

1. $\overline{W0}$, $\overline{W1}$ and $\overline{FB}$ are high during all read cycles.
2. ALE must be high during non-pipelined cycles.
3. Device is continuously selected: $\overline{S} = V_{IL}$
4. Output is continuously enabled: either $\overline{G0} = V_{IL}$ or $\overline{G1} = V_{IL}$ (but not both).
5. AAS may not change during cycle.
6. Address must be valid sufficiently before $\overline{G}$ or $\overline{S}$ transition low to ensure address access specification not violated.
7. Transition is measured ± 500 mV from steady state with C_L = 5pF as shown in Figure 1b on page 6. This parameter is guaranteed and not 100% tested.

AC ELECTRICAL CHARACTERISTICS (over the operating range)
WRITE CYCLE

JEDEC PARAMETER NAME	PARAMETER NAME	PARAMETER	MS82C308-35 MIN.	MS82C308-35 TYP.	MS82C308-35 MAX.	MS82C308-45 MIN.	MS82C308-45 TYP.	MS82C308-45 MAX.	MS82C308-55 MIN.	MS82C308-55 TYP.	MS82C308-55 MAX.	UNITS
t_{AVAX}	t_{WC}	Write Cycle Time	35		–	45		–	55		–	ns
t_{WLWH}	t_{WP}	Write Pulse Width	20		–	20		–	25		–	ns
t_{WLQZ}	t_{WHZ}	Write to Output in High Z	2		15	2		15	2		15	ns
t_{WHQL}	t_{WLZ}	Write to Output in Low Z	2		15	2		15	2		15	ns
t_{DVWH}	t_{DS}	Data Setup Time	8		–	10		–	10		–	ns
t_{WHDX}	t_{DH}	Data Hold from Write Time	3		–	5		–	5		–	ns
	t_{AS}	Address Latch Setup Time	3		–	3		–	3		–	ns
	t_{AH}	Address Latch Hold Time	5		–	5		–	5		–	ns
t_{AVWL}	t_{WAS}	Address to Write Setup Time	3		–	5		–	5		–	ns
	t_{SAA}	AAS to Alternate Address Setup Time	3		–	3		–	3		–	ns
	t_{WAAS}	Alt Address Setup Time	6		–	6		–	6		–	ns
	t_{WAAH}	Alt Address Hold Time	2		–	2		–	2		–	ns
	t_{BW}	Byte Enable to Write Pulse Setup	0		–	0		–	0		–	ns
	t_{FW}	Force Byte Enable to Write Pulse Setup	0		–	0		–	0		–	ns
	t_{AW}	Address Valid to End of Wtrite	30		–	35		–	40		–	ns
t_{SLWH}	t_{SW}	Chip Select to Wtrite Pulse End	20		–	25		–	30		–	ns
t_{WHAX}	t_{WR}	Write Recovery Time	2		–	2		–	2		–	ns

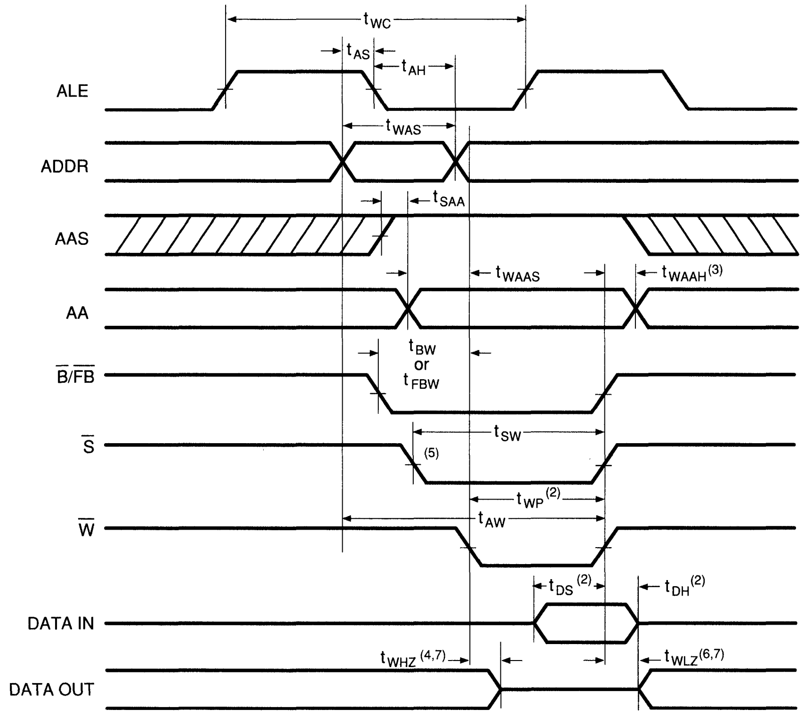
SWITCHING WAVEFORMS (WRITE CYCLE)
WRITE CYCLE 1(1)



6

SWITCHING WAVEFORMS (WRITE CYCLE)

WRITE CYCLE 2[1]



NOTES:

1. $\overline{W}$ must be high during address transitions.
2. The internal write time of the memory is defined by the overlap of $\overline{B}$ or $\overline{FB}$ low, $\overline{S}$ low and $\overline{W}$ low. All signals must be active to initiate a write and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
3. t_{WR} or t_{WAAH} is measured from the earlier of $\overline{B}$ or $\overline{FB}$, or $\overline{S}$ or $\overline{W}$ going high at the end of write cycle.
4. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied
5. If the $\overline{S}$ low transition occurs simultaneously with the $\overline{W}$ low transitions or after the $\overline{W}$ transition, outputs remain in a high impedance state.
6. D_{OUT} is the same phase of write data of this write cycle.
7. Transition is measured ± 500 mV from steady state with C_L = 5pF as shown in Figure 1b on page 6. This parameter is guaranteed and not 100% tested.

ORDERING INFORMATION

SPEED (ns)	ORDERING PART NUMBER (1)	PACKAGE REFERENCE NO.	TEMPERATURE RANGE
35	MS82C308-35JC	J44-1	0°C to +70°C
45	MS82C308-45JC		0°C to +70°C
55	MS82C308-55JC		0°C to +70°C

6

MOSEL Product Brief MS82C330

Cache Chipset for 80386 Systems with Write-Thru Cache

FEATURES

- Highly integrated VLSI components offer complete cache solution
  - MS82C331 Cache Controller
  - MS82C332 Expansion Tag RAM
  - MS82C333 Quad Data RAM
- Tightly coupled 80386 interface
  - Caches full 4GB memory space
  - Full speed support for 80386 non-pipelined operations
- Performance match for 20, 25 and 33 MHz processors
  - Future migration to 40 and 50 MHz
- Supports 32, 64, 128 or 256 Kbyte caches
  - Controller integrates 64Kbyte tag directory on-board
  - For larger caches each expansion tag ram offers additional 64 KB true vertical cache expansion for highest hit rates
- Direct mapped, 2-way and 4-way set associative cache mapping options supported
- Quad fetch mode uses 16 byte subblocks for improved hit rate
  - Demand word fetch first strategy reduces miss penalty
  - Line abort capability eliminates penalty for back-to-back misses
- Write-thru replacement strategy with control for write buffer
  - LRU cache line replacement
  - Allows buffered or non-buffered I/O writes
- Flexible on-chip support for 4 non-cachable regions
- On-chip Gate A20 support
- On-chip decoding for 80387 and Weitek 3167 co-processors
- Asynchronous snoop bus ensures cache coherency
- Direct interface to standard SRAMs or unique MOSEL Quad Data RAM.
  - Quad Data RAM offers maximum performance by allowing cache hits and memory fetches to be done in parallel

The MOSEL MS82C330 Chip Set is the industry's first complete solution for high performance 80386 systems with write-thru cache. This solution allows the processor to run at full speed by providing virtually 0 wait state memory accesses at only a small additional cost. The MS82C331 cache controller incorporates enhanced capabilities such as multiple cache associativity options, quad fetch with demand word fetch priority, main memory burst fill and line abort capability to ensure high hit rates and optimum performance. Highly integrated designs incorporate support for non-cachable regions, co-processors and other functions into the chipset, requiring a minimum of external logic and offering significant reductions in system chip count and board space requirements.

MOSEL's advanced memory technology and expertise has allowed the development of an innovative high speed data path offering significantly improved performance and higher integration. The proprietary dual-access architecture of the MS82C333 Quad DataRAM allows for processor memory accesses and main memory fetches to occur in parallel, offering major improvements in hit rates and processor performance. Addition of the (optional) MS82C332 Expansion Tag RAM allows true vertical cache expansion up to 256 KB for highest performance without increased miss penalty as with other controllers.

This unique scalable architecture offers maximum performance at every density, while allowing the system designer flexibility to select optimum tradeoffs of cost and performance. It also allows for product families and significant product differentiation - no cookie-cutter systems here!

Cache Benefits

As microprocessor speeds continue to increase, these powerful CPUs are hampered by slow access times of main-memory built from inexpensive DRAMs. The addition of a cache subsystem dramatically improves overall system performance by reducing processor wait states and system bus accesses.

Cache Considerations

The two most important factors which influence system performance are cache hit rate and cache management policies. Hit rate is a function of cache size, cache organization, line size, and sub-block size, as well as external factors relating to software design. Cache management policies include such considerations as memory mapping, memory write mechanism, cache miss handling, line replacement and cache coherency.

The MS82C330 Cache Chipset optimizes the tradeoffs between these factors for an 80386 system with write-thru cache. Its' enhanced capabilities and innovative features offer superior performance, design flexibility and integration to the designer while being extremely economical and easy to use.

MS82C331 Cache Controller and MS82C332 Expansion Tag RAM

The MS82C331 is a sophisticated second generation cache controller for designers wanting a write-thru cache. It supports direct-mapped, 2-way and 4-way set-associative cache mapping and provides all management logic for a high-performance cache. The 82C331 integrates 64 KB tag directory with 2 K entries on-chip. Addition of the MS82C332 Expansion Tag RAM allows true vertical cache expansion up to 256 KB for highest performance without increased miss penalty as with other controllers.

In order to increase hit rate, the 82C331 normally operates in quad fetch mode. In this mode each cache miss results in the requested word and the three adjacent words being loaded into the cache. Unlike other controllers, demand word fetch priority ensures that the necessary data is returned to the processor first to minimize processor wait states. Additionally, line abort capability allows quad fetch to be terminated. These features significantly improve the hit rate while virtually eliminating additional miss penalties.

The MS82C331 uses a write-thru memory write scheme. In this method main memory is updated for every processor write cycle. Additional performance is gained by allowing for "buffered" write which enables the processor to continue executing while the main memory write is being performed. Bus snooping is used to maintain cache coherency.

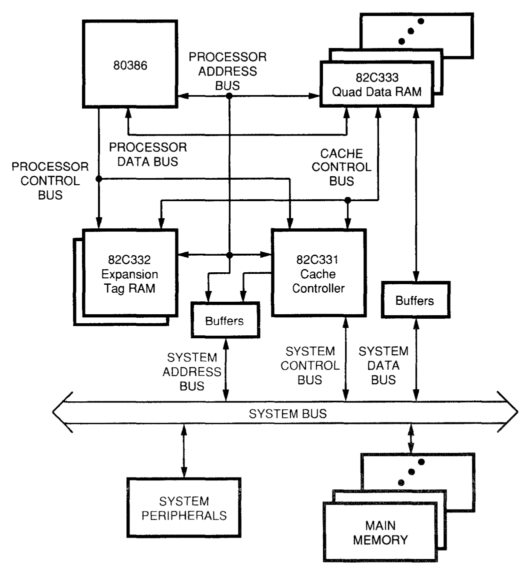
Non-cachable memory is supported with four general purpose non-cachable regions on-chip. These eliminate the need for fast external logic. Two of these regions may be specified as non-writable to support ROM or BIOS caching. Additional support is included for the 80387 and Weitek 3167 co-processors.

MS82C333 Quad DataRAM

While the 82C331 and 82C332 provide excellent performance when used with standard SRAMs, the use of the 82C333 Quad DataRAM offers a dramatic performance improvement. The advanced dual-port architecture of the Quad DataRAM isolates the processor and system data buses. Since the cache will typically be operating at hit rates >95%, this allows main memory operations to proceed simultaneously with processor cache accesses.

This innovative approach offers a quantum leap improvement in data path architecture, removing a major bottleneck to increased performance.

SYSTEM BLOCK DIAGRAM



6

Cache Chipset for 80386 Systems with Write-Back Cache

FEATURES

- Highly integrated VLSI components offer complete cache solution
  - MS82C341 Cache Controller
  - MS82C342 Expansion Tag RAM
  - MS82C343 Quad Data RAM
- Write-back cache update strategy
  - 0 wait-state write hit and miss cycles
  - Improves system bus utilization
  - Speeds up DMA operations
  - Maintains cache coherency in multi-processor systems
  - LRU cache line replacement
- Tightly coupled 80386 interface
  - Caches full 4GB memory space
  - Full speed support for 80386 non-pipelined operations
- Performance match for 20, 25 and 33 MHz processors.
  - Future migration to 40 and 50 MHz
- Supports 32, 64, 128 or 256 Kbyte caches
  - Controller integrates 64 Kbyte tag directory on-board
  - For larger caches each ExpansionTag RAM offers additional 64 KB true vertical cache expansion for highest hit rates
- Direct mapped, 2-way and 4-way set associative cache mapping options supported
- Quad fetch mode uses 16 byte sub-blocks for improved hit rate
  - Demand word fetch first strategy reduces miss penalty
  - Line abort capability eliminates penalty for back-to-back misses and system bus access
- Flexible on-chip support for 4 non-cachable regions
- On-chip Gate A20 support
- On-chip decoding for 80387 and Weitek 3167 co-processors
- Bus snooping ensures cache coherency
- Direct interface to standard SRAMs or unique Mosel Quad DataRAM
  - Quad DataRAM offers maximum performance by allowing cache hits and memory fetches to be done in parallel
  - Quad DataRAM allows write-back line replacement cycles to be hidden from processor, providing 8x performance improvement over alternative implementations.

The MOSEL MS82C340 Chip Set is the industry's first complete solution for high performance 80386 systems with write-back cache. This solution allows the processor to run at full speed by providing virtually 0 wait state memory accesses at only a small additional cost. The MS82C341 cache controller incorporates enhanced capabilities such as multiple cache associativity options, quad fetch with demand word fetch priority, main memory burst fill, and line abort capability to ensure high hit rates and optimum performance. It uses a write-back cache update strategy, which improves system bus utilization, speeds up DMA operations, and assures cache coherency without performance degradation in high-performance multiprocessor systems. Highly integrated designs incorporate support for non-cachable regions, co-processors and other functions into the chipset, requiring a minimum of external logic and offering significant reductions in system cost, chip count, and board space requirements.

Mosel's advanced memory technology and expertise has allowed the development of an innovative high speed data path offering significantly improved performance and higher integration. The proprietary dual-access architecture of the MS82C343 Quad DataRAM allows for processor accesses and main memory accesses to occur in parallel, offering major improvements in hit rates and processor performance. Addition of the (optional) MS82C342 Expansion Tag RAM allows true vertical cache expansion up to 256 KB for highest performance without increased miss penalty as with other controllers.

This unique scalable architecture offers the highest performance at every density, while allowing the system designer flexibility to select optimum tradeoffs of cost and performance. It also allows for product families and significant product differentiation. The MS82C340 cache chipset offers maximum performance with a minimum of cost and board space.

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Cache Benefits

As microprocessor speeds continue to increase, these powerful CPUs are hampered by slow access times of main-memory built from inexpensive DRAMs. The addition of a cache subsystem dramatically improves overall system performance by reducing processor wait states and system bus accesses.

Cache Considerations

The two most important factors which influence system performance are cache hit rate and cache management policies. Hit rate is a function of cache size, cache organization, line size, and sub-block size, as well as external factors relating to software design. Cache management policies include such considerations as memory mapping, memory write mechanism, cache miss handling, line replacement, cache coherency and non-cachable memory.

In a write-thru cache, every write operation from the processor is treated as a miss and written to main memory. This provides a simple mechanism for maintaining cache coherency, but sacrifices performance (since writes to main memory take more cycles) and bus bandwidth (since the system bus is occupied with processor writes). In contrast, a write-back cache reduces system bus traffic by writing to main memory only when a cache line which has been modified by the CPU is about to be replaced by new data from main memory. This drastically reduces the frequency of main memory write accesses, and frees up system bus bandwidth for DMA operations and other system accesses.

The MS82C340 Cache Chipset optimizes the tradeoffs between these factors for an 80386 system with write-back cache. Its' enhanced capabilities and innovative features offer superior performance, design flexibility and integration to the designer while being economical and easy to use.

MS82C341 Cache Controller and MS82C342 Expansion Tag RAM

The MS82C341 is a sophisticated second generation write-back cache controller. It supports direct-mapped, 2-way and 4-way set-associative cache mapping and provides all management logic for a high-performance cache. The MS82C341 integrates 64KB tag directory with 2K entries on-chip. Addition of the MS82C342 Expansion Tag RAM allows true vertical cache expansion up to 256 KB for highest performance without increased miss penalty as with other controllers.

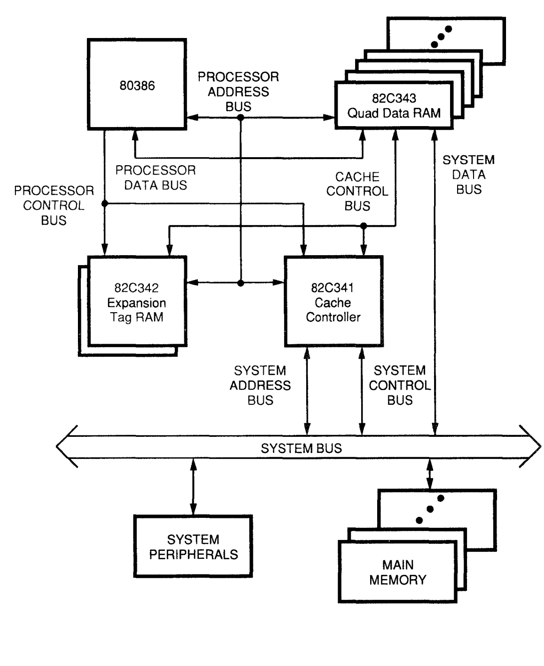
In order to increase hit rate, the MS82C341 normally operates in quad fetch mode. In this mode each cache miss results in the requested word and the three adjacent words being loaded into the cache. Unlike other controllers, demand word fetch priority ensures that the requested data is returned to the processor immediately. Additionally, line abort capability allows the quad fetch to be terminated on a subsequent miss to immediately fetch the newly requested data. These features significantly improve the hit rate while virtually eliminating additional miss penalties.

The MS82C341 uses a write-back memory write strategy with an 8 line block size. Bus snooping is included to maintain cache coherency. Non-cachable memory is supported with four general purpose non-cachable regions on-chip. These eliminate the need for fast external logic. Two of these regions may be specified as non-writable to support ROM or BIOS caching. Additional support is included for the 80387 and Weitek 3167 co-processors.

MS82C343 Quad DataRAM

While the MS82C341 and MS82C342 provide excellent performance when used with standard SRAMs, the use of the MS82C343 Quad DataRAM offers a dramatic performance improvement. The advanced dual-access architecture of the Quad DataRAM isolates the processor and system data buses. Since the cache will typically be operating at hit rates >95%, this allows main memory operations to proceed simultaneously with processor cache accesses. Write-back line replacement cycles are hidden from the processor, providing up to an 8X performance improvement in miss processing over other cache implementations. This innovative approach offers a quantum leap improvement in data path architecture, removing a major bottleneck to increased performance.

SYSTEM BLOCK DIAGRAM



6

MOSEL Product Brief MS82C440

Cache Chipset for 80486 Systems

FEATURES

- Highly integrated VLSI components offer complete solution for secondary cache for 80486 systems
  - MS82C441 Cache Controller
  - MS82C442 Expansion Tag RAM
  - MS82C443 Burst RAM
- Supports true 80486 burst reads with 0 wait states
- Write-back cache update strategy with 16 byte sub-blocks
  - 0 wait-state read hits, write hits and write misses
  - Improves system bus utilization
  - Speeds up DMA operations
  - Maintains cache coherency in multi-processor systems
  - LRU cache line replacement
- Supports burst reads and writes between cache and main memory
  - Allows both sequential and 80486 burst sequence memory requests
  - With Burst RAM allows use of standard cost-effective 32 bit main memory organization (No bank interleaving required). Automatically handles resequencing of data back to 80486
- Tightly coupled 80486 interface
  - Caches full 4GB memory space
  - Cache invalidation cycles supported back to the 80486
- Performance match for 25 and 33 MHz processors.
  - Future migration to 40 and 50 MHz
- Supports 32, 64, 128 , 256 Kbyte and larger caches
  - Controller integrates 64 Kbyte tag directory on-board
  - For larger caches each Expansion Tag RAM offers additional 64 KB true vertical cache expansion for highest hit rates without extending line size
- Direct mapped, 2-way and 4-way set associative cache mapping options supported
- Flexible on-chip support for 4 non-cachable regions. Full support for KEN#.
- On-chip Gate A20 support
- Supports Weitek 4167 co-processor
- Bus snooping ensures cache coherency.
- Direct interface to standard SRAMs or unique Mosel Burst RAMs
  - Burst RAMs offer maximum performance by allowing cache hits and memory accesses to be done in parallel
  - x9 width of Burst RAM allows use of parity functions offered by 80486
  - Burst RAMs allow write-back line replacement cycles to be hidden from processor, providing up to 8x performance improvement over alternative implementations.

The MOSEL MS82C440 Chip Set is the industry's first complete solution for high performance 80486 systems. This solution allows the processor to run at full speed by providing virtually 0 wait state memory accesses at only a small additional cost. The MS82C441 cache controller incorporates enhanced capabilities such as full support for 80486 burst reads, multiple cache associativity options and burst reads and writes between cache and main memory. It uses a write-back cache update strategy, which improves system bus utilization, speeds up DMA operations, and assures cache coherency without performance degradation in high-performance systems. Highly integrated designs incorporate support for non-cachable regions, co-processors and other functions into the chipset, requiring a minimum of external logic and offering significant reductions in system cost, chip count and board space requirements.

Mosel's advanced memory technology and expertise has allowed the development of an innovative high speed data path offering significantly improved performance and higher integration. The proprietary dual-access architecture of the MS82C443 Burst RAM allows for processor accesses and main memory accesses to occur in parallel, offering major improvements in system performance. Addition of the (optional) MS82C442 Expansion Tag RAM allows true vertical cache expansion to 256 KB and beyond for highest performance without increased miss penalty or lengthy line replacement cycle times.

This unique scalable architecture offers the highest performance at every density, while allowing the system designer flexibility to select optimum tradeoffs of cost and performance. It also allows for product families and significant product differentiation. The MOSEL MS82C440 cache chipset offers maximum performance with a minimum of cost and board space.

Cache Benefits

As microprocessor speeds continue to increase, these powerful CPUs are hampered by slow access times of main-memory built from inexpensive DRAMs. The addition of a cache subsystem dramatically improves overall system performance by reducing processor wait states and system bus accesses.

Cache Considerations

The two most important factors which influence system performance are cache hit rate and cache management policies. Hit rate is a function of cache size, cache organization, line size, and sub-block size, as well as external factors relating to software design. Cache management policies include such considerations as memory mapping, memory write mechanism, cache miss handling, line replacement, cache coherency and non-cachable memory.

In a write-thru cache, every write operation from the processor is treated as a miss and written to main memory. This provides a simple mechanism for maintaining cache coherency, but sacrifices performance (since writes to main memory take more cycles) and bus bandwidth (since the system bus is occupied with processor writes). In contrast, a write-back cache reduces system bus traffic by writing to main memory only when a cache line which has been modified by the CPU is about to be replaced by new data from main memory. This drastically reduces the frequency of main memory write accesses, and frees up system bus bandwidth for DMA operations and other system accesses.

The MS82C440 Cache Chipset optimizes the tradeoffs between these factors for an 80486 system. Its' enhanced capabilities and innovative features offer superior performance, design flexibility and integration to the designer while being economical and easy to use

MS82C441 Cache Controller and MS82C442 Expansion Tag RAM

The MS82C441 is a sophisticated second generation write-back cache controller for use with the Intel 80486 microprocessor. It supports direct-mapped, 2-way and 4-way set-associative cache mapping and provides all management logic for a high-performance cache. The MS82C441 integrates 64KB tag directory with 2K entries on-chip. Addition of the MS82C442 Expansion Tag RAM allows true vertical cache expansion up to 256 KB and beyond for highest performance without increased miss penalty or extending cache line length (which can severely impact performance).

Full support for the 80486 is provided by the MS82C441 cache controller, including 0 wait state burst reads and non-cachable regions through KEN#. It also supports burst reads and writes between cache and main memory, and can handle both sequential and 80486 burst sequence memory organizations.

The MS82C441 uses a write-back memory write strategy with an 8 line sub-block size. Bus snooping is included to maintain cache coherency. Non-cachable memory is supported with four general purpose non-cachable regions on-chip. These eliminate the need for fast external logic. Two of these regions may be specified as non-writable to support ROM or BIOS caching. Additional support is included for the Weitek 4167 co-processor.

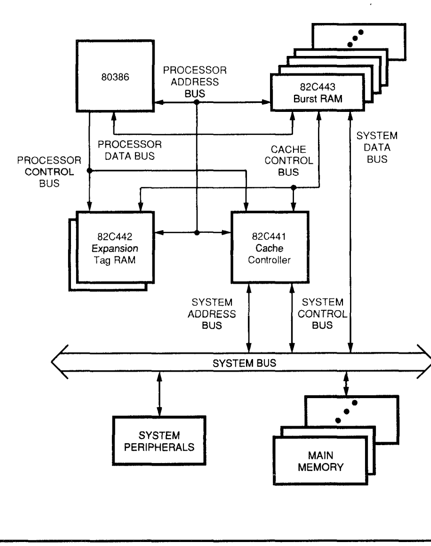
MS82C443 Burst RAM

While the MS82C441 and MS82C442 provide excellent performance when used with standard SRAMs, the use of the MS82C443 Burst RAM offers an additional dramatic performance improvement. The advanced dual-access architecture of the Burst RAM isolates the processor and system data buses. Since the cache will typically be operating at hit rates >96%, this allows main memory operations to proceed simultaneously with processor cache accesses. Write-back line replacement cycles are hidden from the processor, providing up to an 8X performance improvement in miss processing over other implementations. This innovative approach offers a quantum leap improvement in data path architecture, removing a major bottleneck to increased performance.

The MS82C443 Burst RAM also allows the use of standard, cost-effective 32 bit main memory designs. In conjunction with the MS82C441 cache controller, standard sequential DRAM access modes can be used, and the data will automatically be resequenced into the proper order for the 80486. This unique capability eliminates the need to develop complex and expensive memory architectures such as 64 bit memory buses or bank interleaved memory, while providing maximum performance.

6

SYSTEM BLOCK DIAGRAM



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Using the MOSEL MS82C308 Cache Data RAM with the Intel 82385 Cache Controller

High speed 80386 systems place severe demands on memory designers to develop economical methods to maintain processor throughput without incurring enormous costs. One proven, effective solution is to use a relatively small high speed SRAM cache in addition to the large DRAM main memory to achieve high average memory bandwidth with only small additional cost. Memory systems incorporating a cache can eliminate wait states for well over 90% of all memory accesses at only a small fraction of the cost of a complete high speed memory system.

The Intel 82385 is an integrated cache controller which provides all of the control signals needed to add a high speed cache to an 80386 system. It supports direct-mapped and 2-way set associative caches of up to 32KB. When used in conjuction with the Mosel MS82C308 Cache Data Ram, a complete 32KB 2-way set associative cache can be implemented with only 5 chips. Earlier methods required from 18-28 chips to perform the same function. The result is a dramatic reduction in design complexity and board space, as well as a significant cost savings.

The Mosel MS82C308 Cache Data Ram is a high speed SRAM device optimized for cache applications. Each device is organized as 2 sets on-chip, with each set being 2K x 16. In addition, the address latches, data transceivers and control functions are all integrated onto the device. Versions are currently available to support up to 25 MHz 80386 systems, with even faster versions under development.

BUILDING A 32KB CACHE

Interfacing with MS82C308 with the Intel 82385 cache controller for a 32KB cache is an easy task. Figure 1 shows the connection diagram for a 32KB 2-way set associative cache. Address inputs A0-A10 on the 4 cache data rams are connected in parallel to addresses A2-A12 of the 80386 local address bus. The data input/output pins of the 4 data rams are then connected to DQ0-DQ31 of the 80386 local data bus. (In Figure 1, devices A and C provide the high order bits of set 0 and 1, respectively). The 4 chip select outputs from the 82385 are connected to the byte enables on the data rams. The output enables and write enables for sets 0 and 1 from the 82385 (COEA#, COEB#, CWEA#, CWEB#) are then connected to the appropriate enable pin on each of the 4 data rams. The CALEN output from the 82385 is connected to the ALE pin on each data ram. Finally, the force byte enable ($\overline{FB}$) on each device should tied HIGH, and the alternate address select pin (AAS) on each data ram should be tied LOW. (These enhanced functions are not supported by the 82385).

The last step needed is to decode between the upper and lower segments of the cache memory. For this, address A13 is brought out from the 80386 and is latched (using a 74F373 or similar latch). The output of the latch is used to drive the chip select ($\overline{S}$) pins of the data rams. One set of data rams (in this case devices A and B) are designated as the lower segment and their chip selects are driven directly by the latched output; the other set (devices C and D) are the upper segment and their chip selects are driven by the invert of the latched output.

BUILDING A 16KB CACHE

There may be occasions when the designer chooses to implement a smaller cache for the system. Reasons for this may include such factors as system cost or board space considerations. Figure 2 shows how a 16KB 2-way set associative cache can be implemented with just 2 Mosel MS82C308 Cache Data Rams and the Intel 82385 cache controller. With the exception of the select circuit, all of the connections are the same as for the 32KB cache. The primary difference is that since there is only one memory segment, the data rams are continuously enabled. Therefore the chip select (S) pins on the data rams should be tied LOW.

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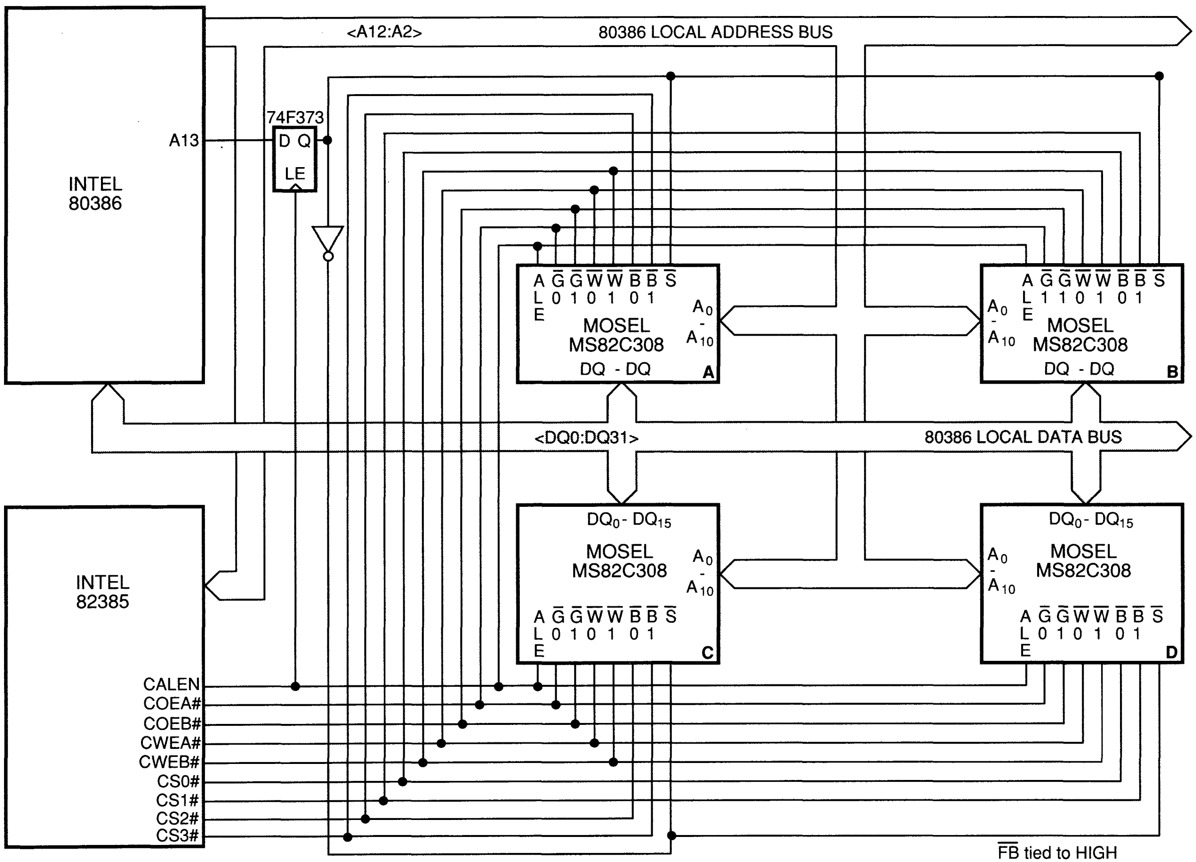

FIGURE 1 - 32K BYTE 2-WAY SET ASSOCIATIVE CACHE

$\overline{FB}$ tied to HIGH

AAS tied LOW

PID014A

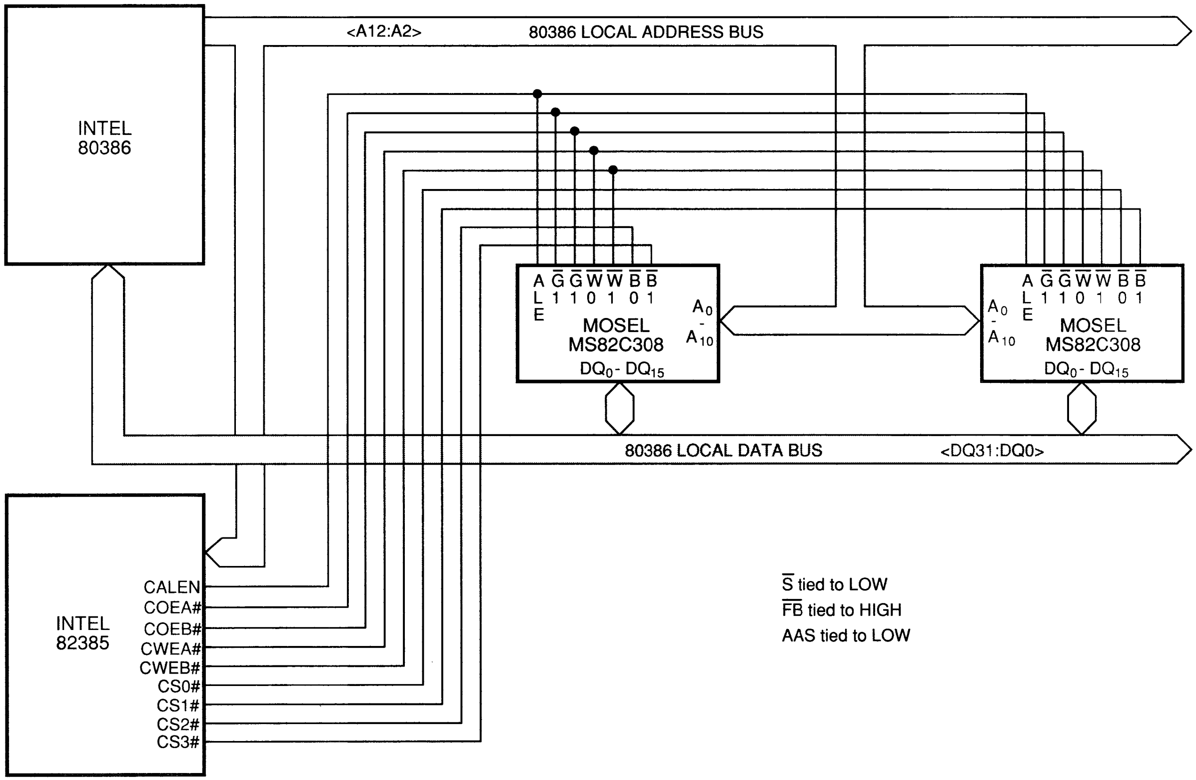

FIGURE 2 - 16KB 2-WAY SET ASSOCIATIVE CACHE

General Information 1

Static RAMs (Random Access Memory) 2

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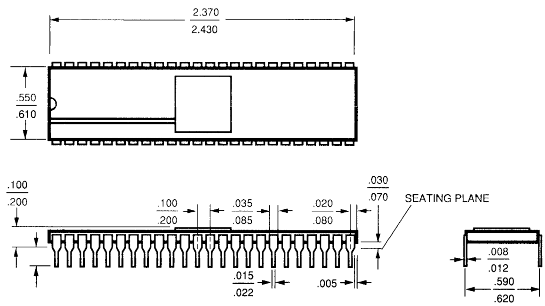
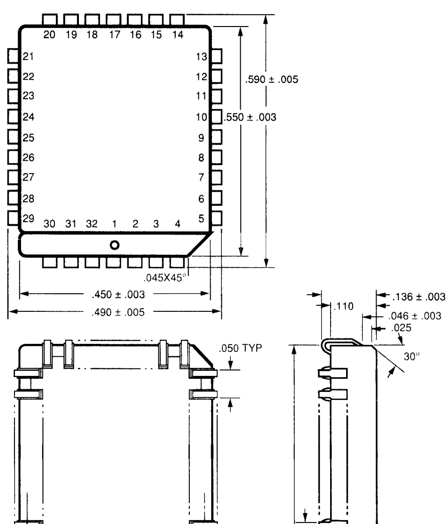
PACKAGE DIAGRAMS

D48-1 48 pin Sidebraze

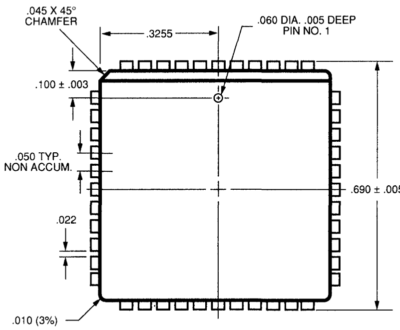


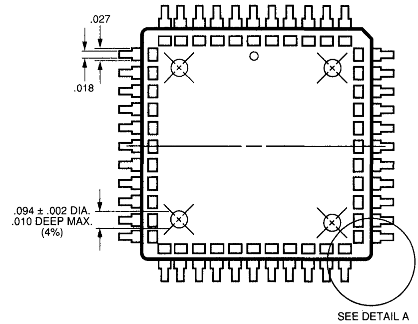
J32-1 32 pin Plastic Leaded Chip Carrier

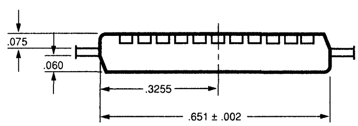


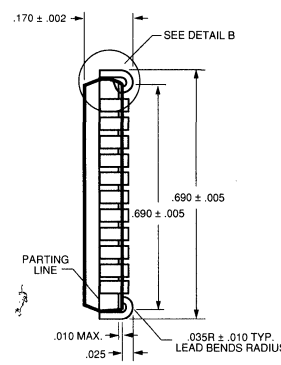
PACKAGE DIAGRAMS

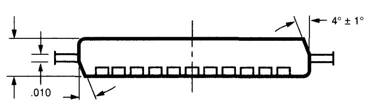
J44-1 44 pin Plastic Leaded Chip Carrier

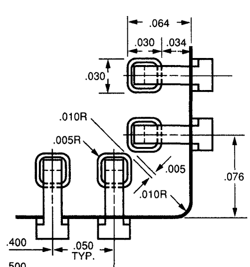




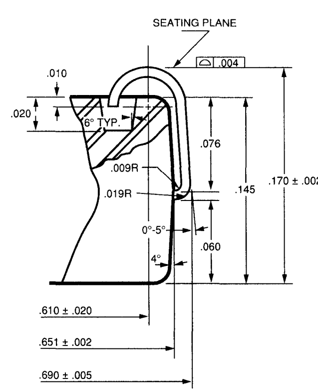








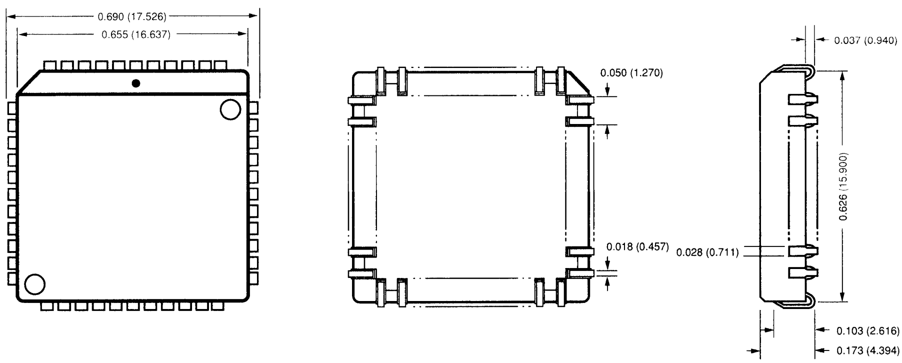
DETAIL A



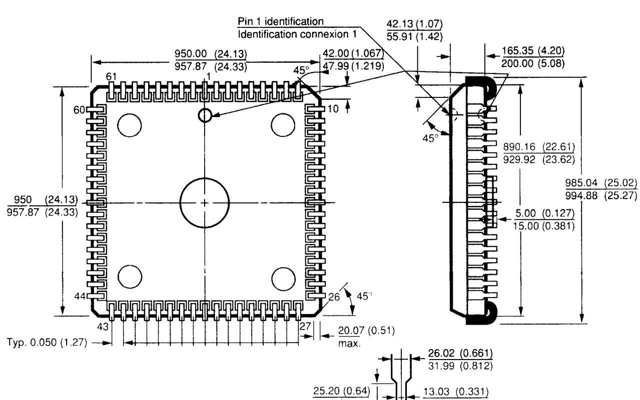
DETAIL B

PACKAGE DIAGRAMS

J44-2 44 pin Plastic Leaded Chip Carrier



J68-1 68 pin Plastic Leaded Chip Carrier



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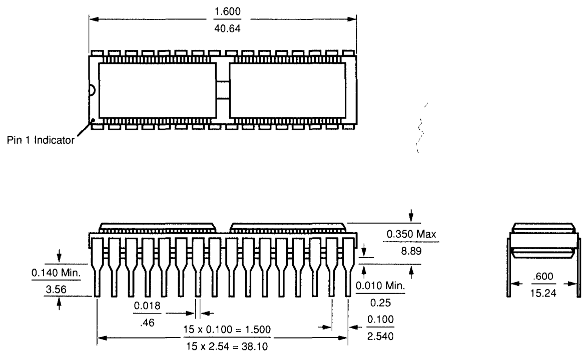
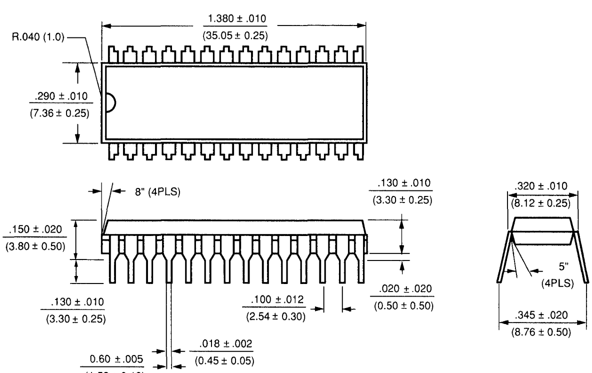
PACKAGE DIAGRAMS

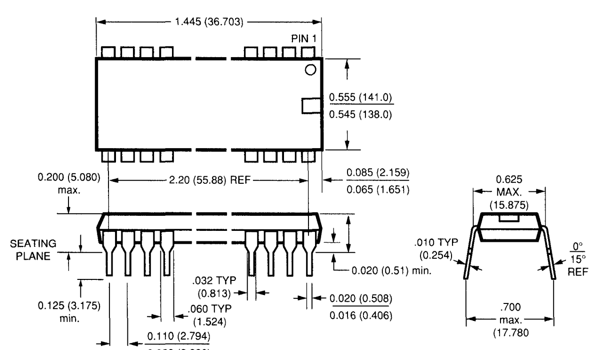
M-1 32 pin Module



P24-1 24 pin Plastic Dual-in-line - 600 mil

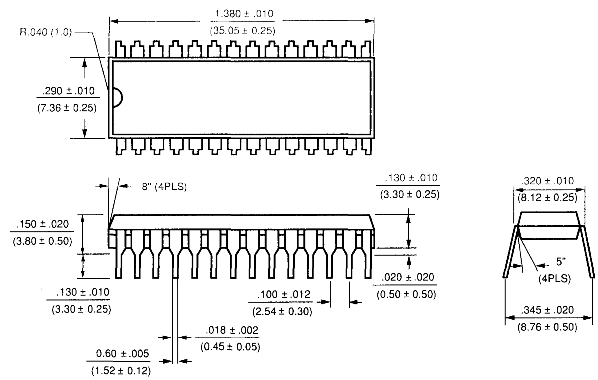


P28-1 28 pin Plastic Dual-in-line - 600 mil

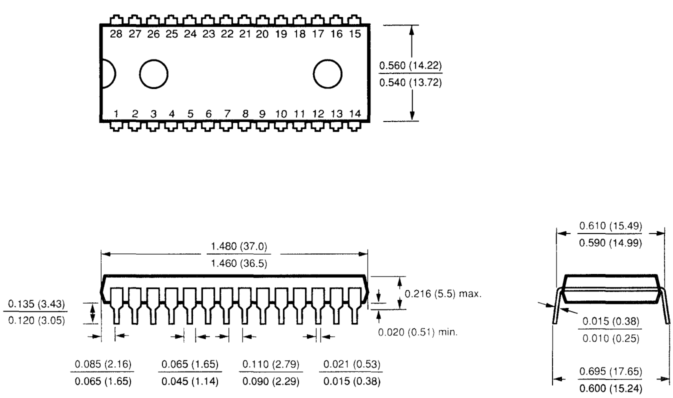


PACKAGE DIAGRAMS

P28-2 28 pin Plastic Dual-in-line - 300 mil



P28-3 28 pin Plastic Dual-in-line - 600 mil



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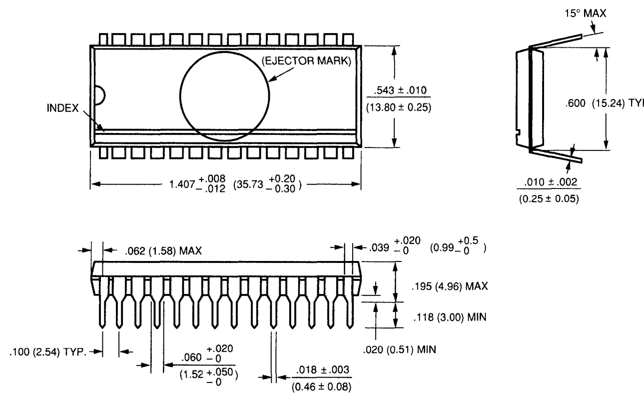
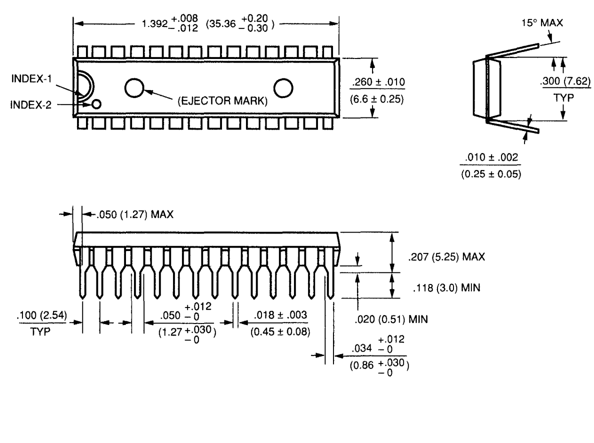
PACKAGE DIAGRAMS

P28-4 28 pin Plastic Dual-in-line Package

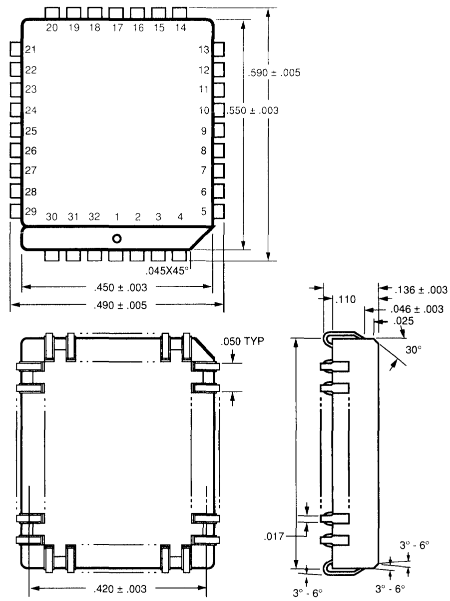


P28-5 28 pin Plastic Dual-in-line Package

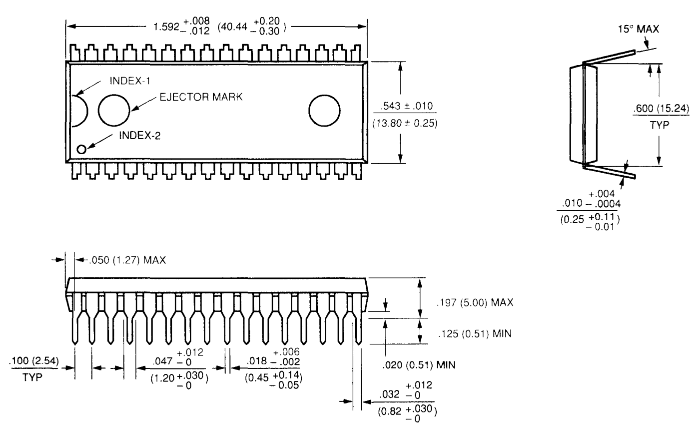


PACKAGE DIAGRAMS

P32-1 **32 pin Plastic Dual-in-line - 600 mil**



P32-2 **32 pin Plastic Dual-in-line Package**



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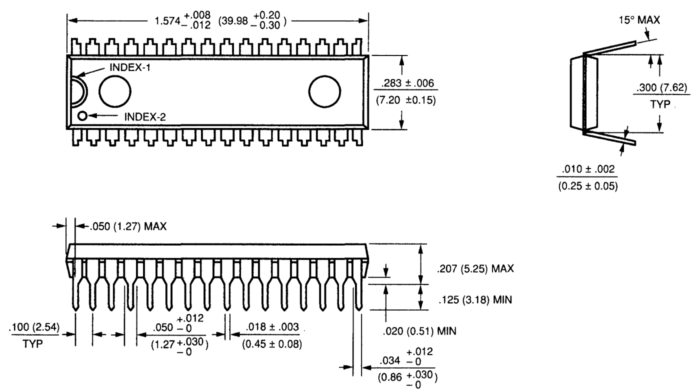
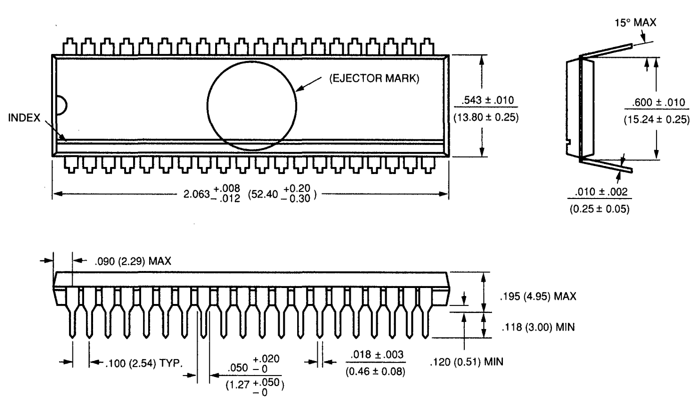
PACKAGE DIAGRAMS

P32-3 32 pin Plastic Dual-in-line Package

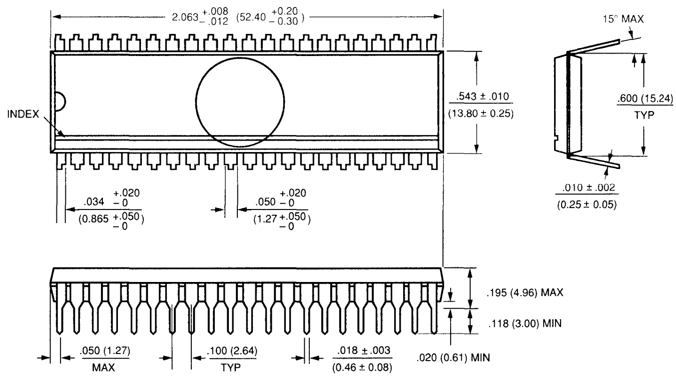


P40-1 40 pin Plastic Dual-in-line Package

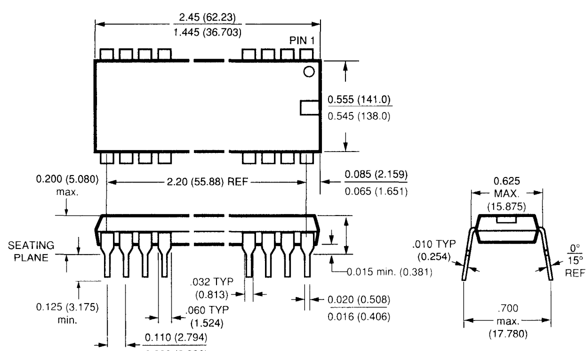


PACKAGE DIAGRAMS

P42-1 42 pin Dual-in-line Package



P48-1 48 pin Plastic Dual-in-line - 600 mil



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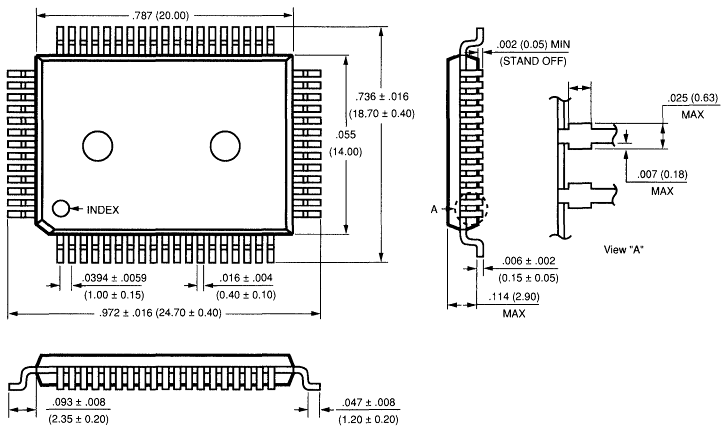
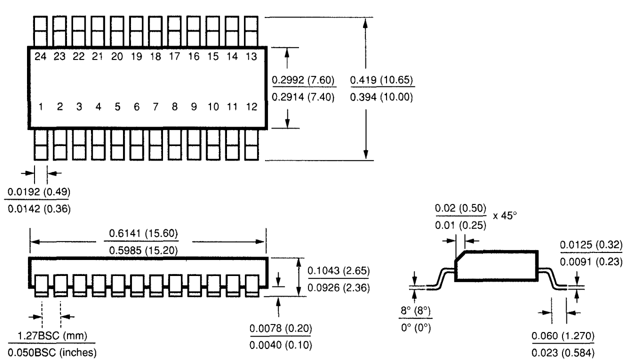
PACKAGE DIAGRAMS

Q64-1 64 pin Plastic Flat Package

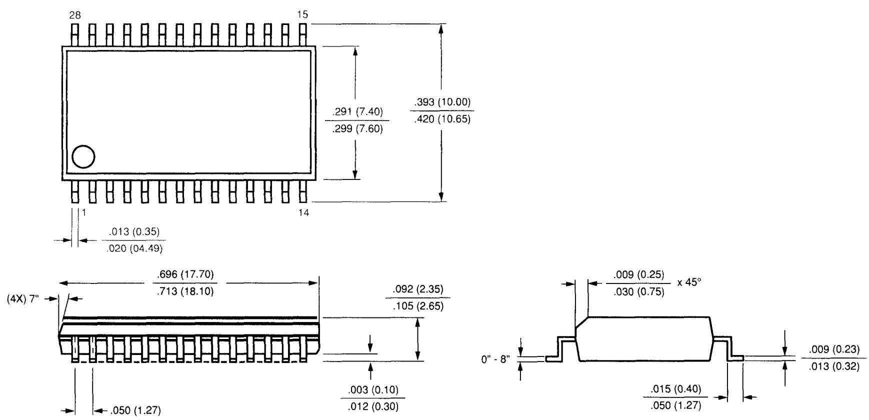


S24-1 24 pin Small Outline Package - 600 mil

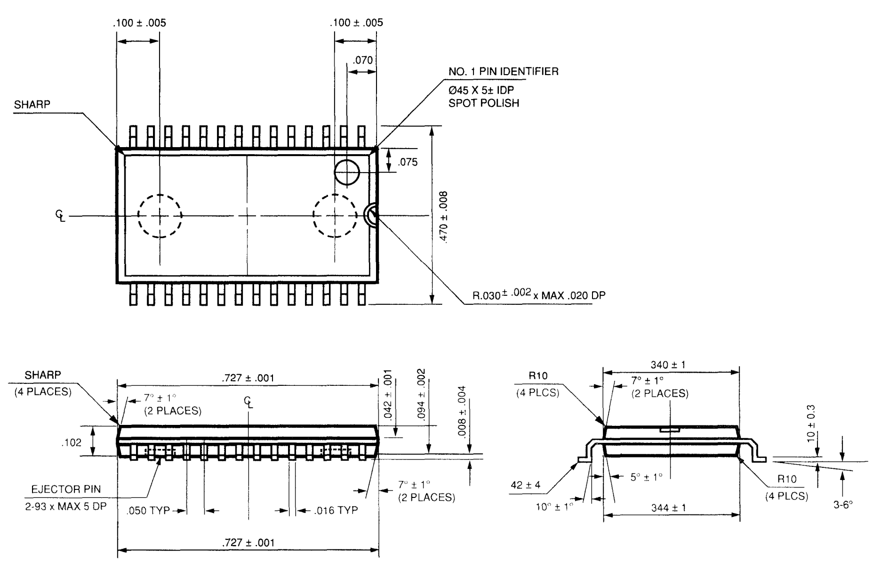


PACKAGE DIAGRAMS

S28-1 28 pin Small Outline Package - 300 mil



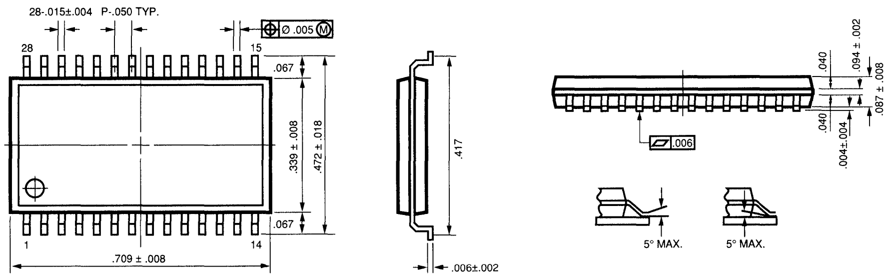
S28-2 28 pin Small Outline Package - 330 mil



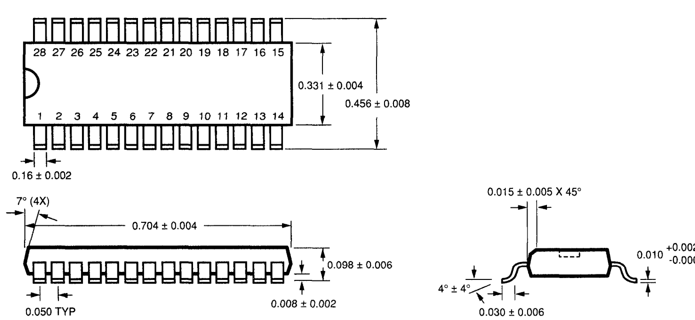
NOTE:
1. MATTE SURFACE: TOP AND BOTTOM SURFACE ONLY VDI 21.
2. LEADS ARE COPPER ALLOY EITHER TIN PLATED OR SOLDER COATED.
3. ALL TOLERANCES ARE ±2 UNLESS OTHERWISE SPECIFIED.

PACKAGE DIAGRAMS

S28-3 28 pin Small Outline Package - 330 mil

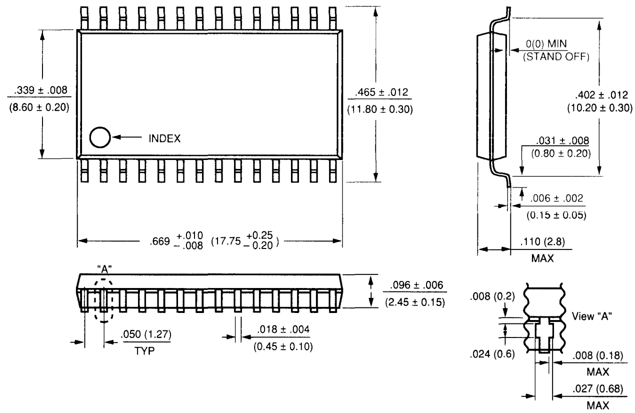


S28-4 28 pin Small Outline Package - 330 mil

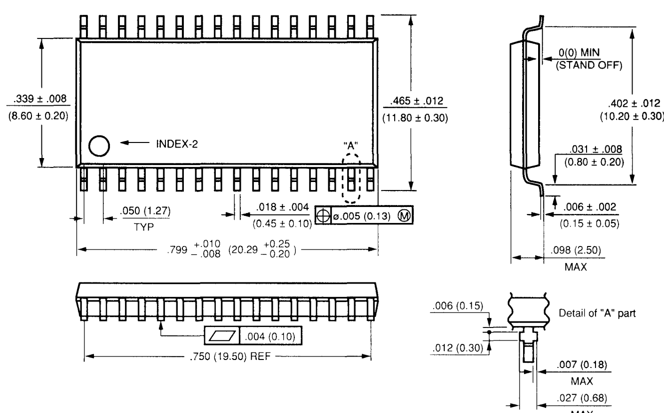


PACKAGE DIAGRAMS

S28-5 28 pin Small Outline Gull Wing



S32-1 32 pin Plastic Small Outline Package



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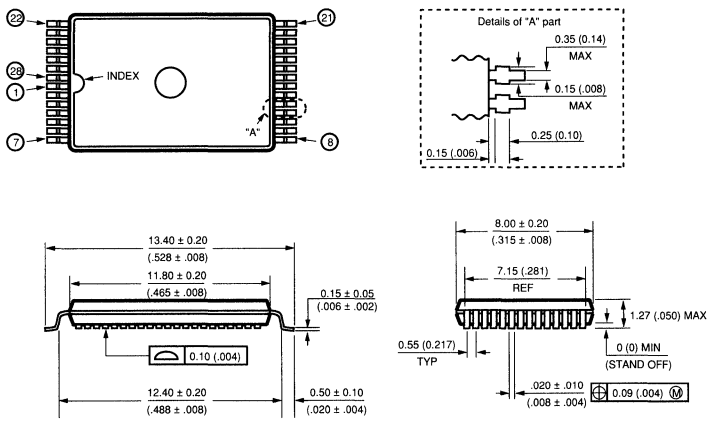
PACKAGE DIAGRAMS

V28-1 28 pin Very Small Outline Package



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