

High Performance 1024 x 4 PROM Ti-W PROM Family

53/63S440 53/63S441 53/63S441A

Features/Benefits

- 24 ns typical access time
- Reliable Titanium-Tungsten fuses (Ti-W) guarantees greater than 98% programming yields
- Low voltage generic programming
- Pin compatible with standard Schottky PROMs
- PNP inputs for low input current
- Open collector and three-state outputs

Applications

- Microprogram control stores
- Microprocessor program store
- Look-up table
- Character generator
- Code converter
- Programmable logic element (PLE™) 10 inputs, 4 outputs, 1024 product terms

Description

The 53/63S440 and 53/63S441/A are 1024 x 4 bipolar PROMs featuring low input current PNP inputs, full Schottky clamping with open collector or three-state outputs. The titanium-tungsten fuses store a logical low and are programmed to the high-state. Special on-chip circuitry and extra fuses provide preprogramming testing which assures high programming yields and high reliability.

The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges.

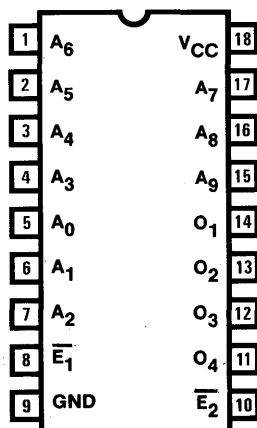
Programming

The 53/63S440 and 53/63S441/A PROMs are programmed with the same programming algorithm as all other Monolithic Memories' generic Ti-W PROMs. For details refer to Monolithic Memories' LSI Data Book.

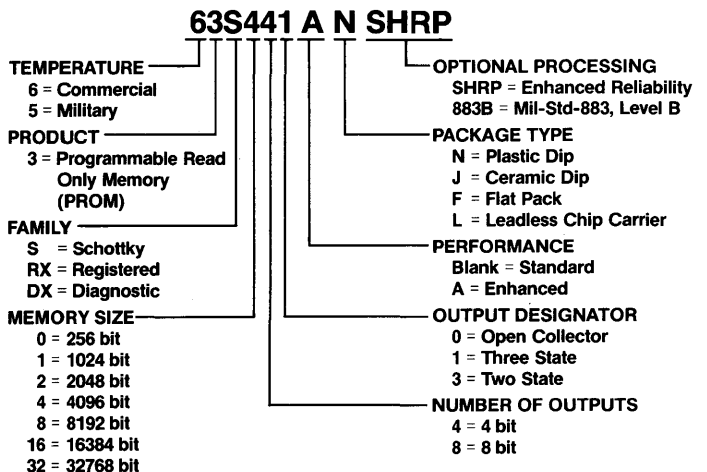
Selection Guide

MEMORY		PACKAGE		PERFORMANCE	OUTPUT	PART NUMBER	
SIZE	ORGANIZATION	PINS	TYPE			0° C to +75° C	-55° C to +125° C
4 K	1024 x 4	18 (20)	N,J,F W,(L)	Enhanced	TS	63S441A	53S441A
				Standard	TS	63S441	53S441
					OC	63S440	53S440

Pin Configuration



Part Numbering System



PLE™ is a registered trademark of Monolithic Memories.

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TWX: 910-338-2374

Monolithic Memories

Absolute Maximum Ratings

	Operating	Programming
Supply voltage V_{CC}	-0.5 V to 7 V	12 V
Input voltage	-1.5 V to 7 V	7 V
Off-state output voltage	0.5 V to 5.5 V	12 V
Storage temperature	-65° to +150°C	

Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	-55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION		MIN TYP† MAX		UNIT	
V_{IL}	Low-level input voltage				0.8	V	
V_{IH}	High-level input voltage			2		V	
V_{IC}	Input clamp voltage	$V_{CC} = \text{MIN}$	$I_I = -18 \text{ mA}$		-1.5	V	
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}$	$V_I = 0.4 \text{ V}$		-0.25	mA	
I_{IH}	High-level input current	$V_{CC} = \text{MAX}$	$V_I = V_{CC} \text{ MAX}$		40	μA	
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}$	$I_{OL} = 16 \text{ mA}$	MIL	0.5	V	
				COM	0.45		
V_{OH}	High-level output voltage*	$V_{CC} = \text{MIN}$	MIL $I_{OH} = -2 \text{ mA}$	2.4		V	
			COM $I_{OH} = -3.2 \text{ mA}$				
I_{OZL}	Off-state output current*	$V_{CC} = \text{MAX}$	$V_O = 0.4 \text{ V}$		-40	μA	
I_{OZH}			$V_O = 2.4 \text{ V}$		40		
I_{CEX}	Open collector output current	$V_{CC} = \text{MAX}$	$V_O = 2.4 \text{ V}$		40	μA	
			$V_O = 5.5 \text{ V}$		100		
I_{OS}	Output short-circuit current**	$V_{CC} = 5 \text{ V}$	$V_O = 0 \text{ V}$		-20	-90	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX}$ All inputs grounded. All outputs open.			95	140	mA

Switching Characteristics Over Operating Conditions (See standard test load)

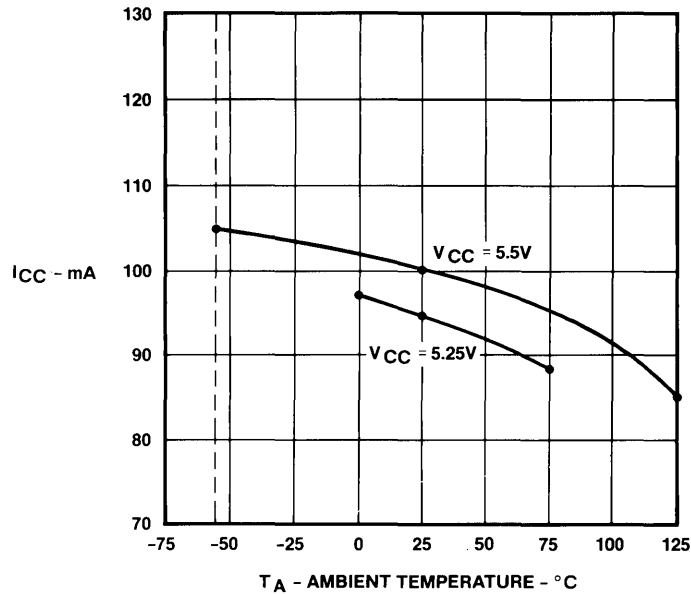
OPERATING CONDITIONS	DEVICE TYPE	t_{AA} (ns) ADDRESS ACCESS TIME		t_{EA} AND t_{ER} (ns) ENABLE ACCESS TIME RECOVERY TIME		UNIT
		TYP†	MAX	TYP†	MAX	
		COMMERCIAL	63S441A	24	35	
63S440, 63S441	24		45	16	25	
MILITARY	53S441A	24	50	16	30	
	53S440, 53S441	24	55	16	30	

* Three-state only.

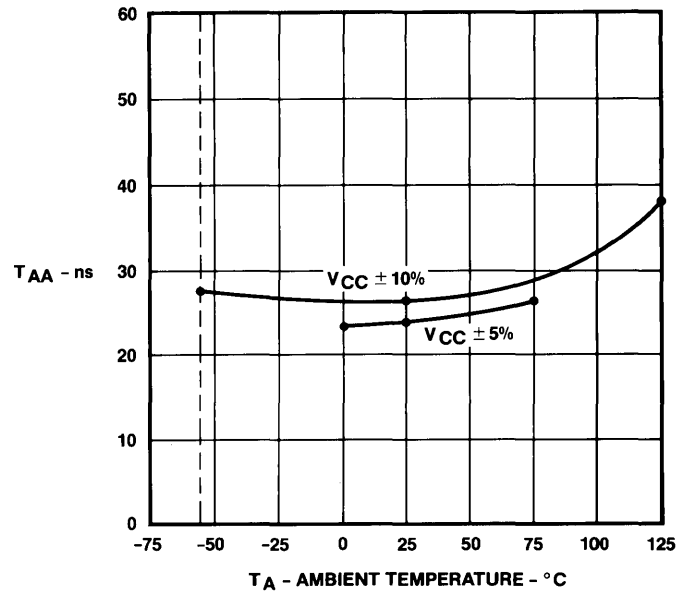
** Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

† Typical at 5.0 V V_{CC} and 25°C TAA.

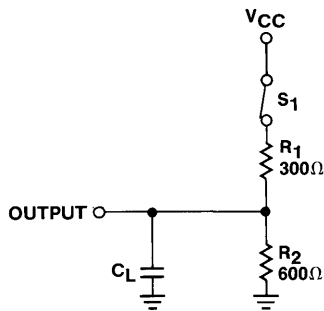
Typical I_{CC} vs Temperature



Typical T_{AA} vs Temperature



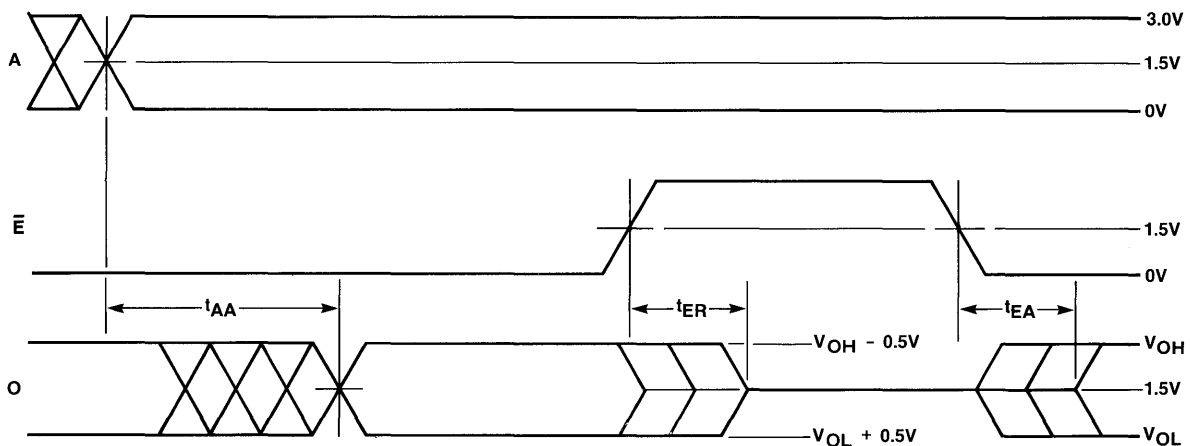
Switching Test Load



Definition of Timing Diagram

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE; CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	NOT APPLICABLE	CENTER LINE IS HIGH IMPEDANCE STATE
	MUST BE STEADY	WILL BE STEADY

Definition of Waveforms



- NOTES:
1. Input pulse amplitude 0 V to 3.0 V.
 2. Input rise and fall times 2-5 ns from 0.8 V to 2.0 V.
 3. Input access measured at the 1.5 V level.
 4. t_{AA} and t_{EA} are tested with switch S_1 closed, $C_L = 30$ pF and measured at 1.5 V output level.
 5. t_{ER} is tested with $C_L = 5$ pF and S_1 closed. "1" to high-impedance test is measured at $V_{OH} - 0.5$ V output level, "0" to high-impedance test is measured at $V_{OL} + 0.5$ V output level.

Commercial Programmers

Monolithic Memories PROMs are designed and tested to give a programming yield greater than 98%. If your programming yield is lower, check your programmer. It may not be properly calibrated.

Programming is final manufacturing — it must be quality-controlled. Equipment must be calibrated as a regular

routine, ideally under the actual conditions of use. Each time a new board or a new programming module is inserted, the whole system should be checked. Both timing and voltages must meet published specifications for the device.

Remember — The best PROMs available can be made unreliable by improper programming techniques.

PROM PROGRAMMING EQUIPMENT INFORMATION

SOURCE AND LOCATION

Data I/O Corp.
10525 Willows Rd. N.E
C-46
Redmond, WA 98052

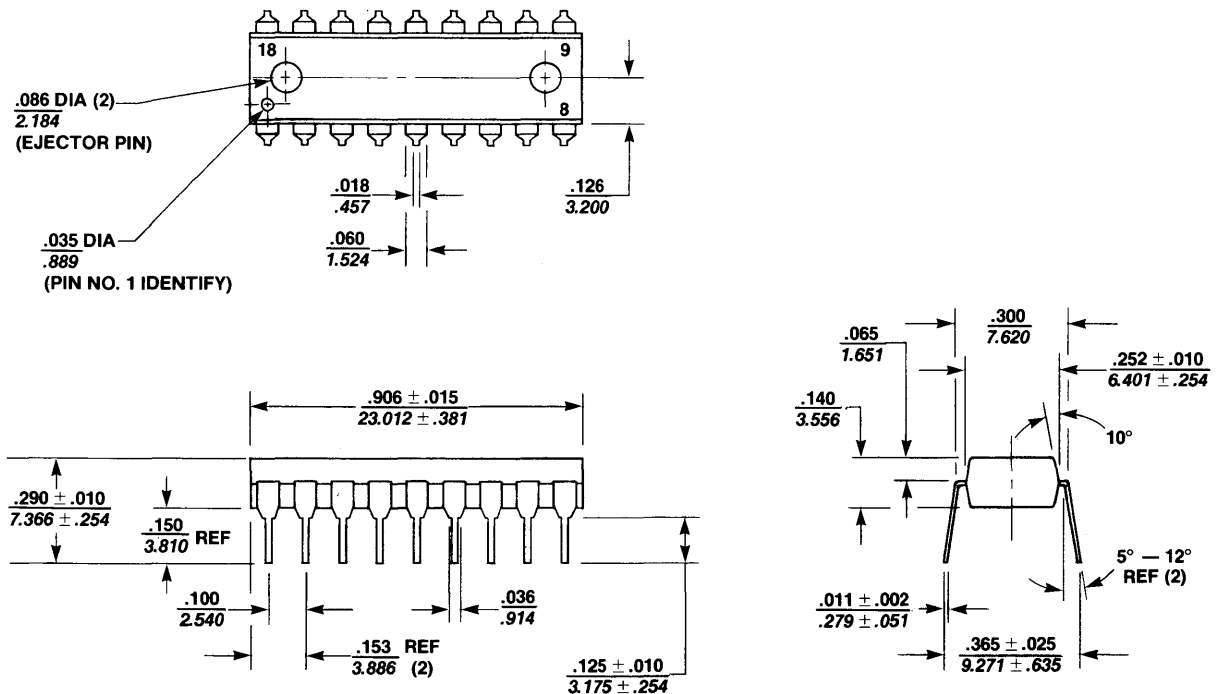
Digelec Inc.
7335 E. Acoma DR
Suite 103
Scottsdale, AZ 85260

Kontron Electronic, Inc.
630 Price Ave.
Redwood City, CA 94036

Stag Systems Inc.
1120 San Antonio Rd.
Palo Alto, CA 94303

Package Drawings

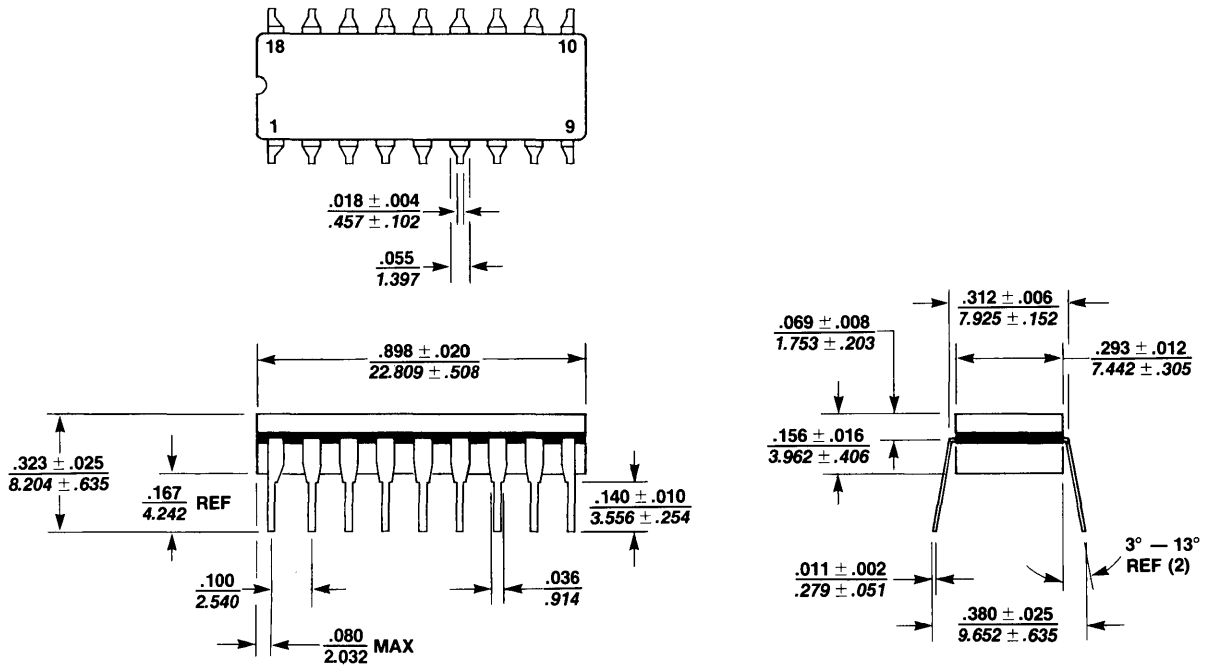
N18 Molded DIP



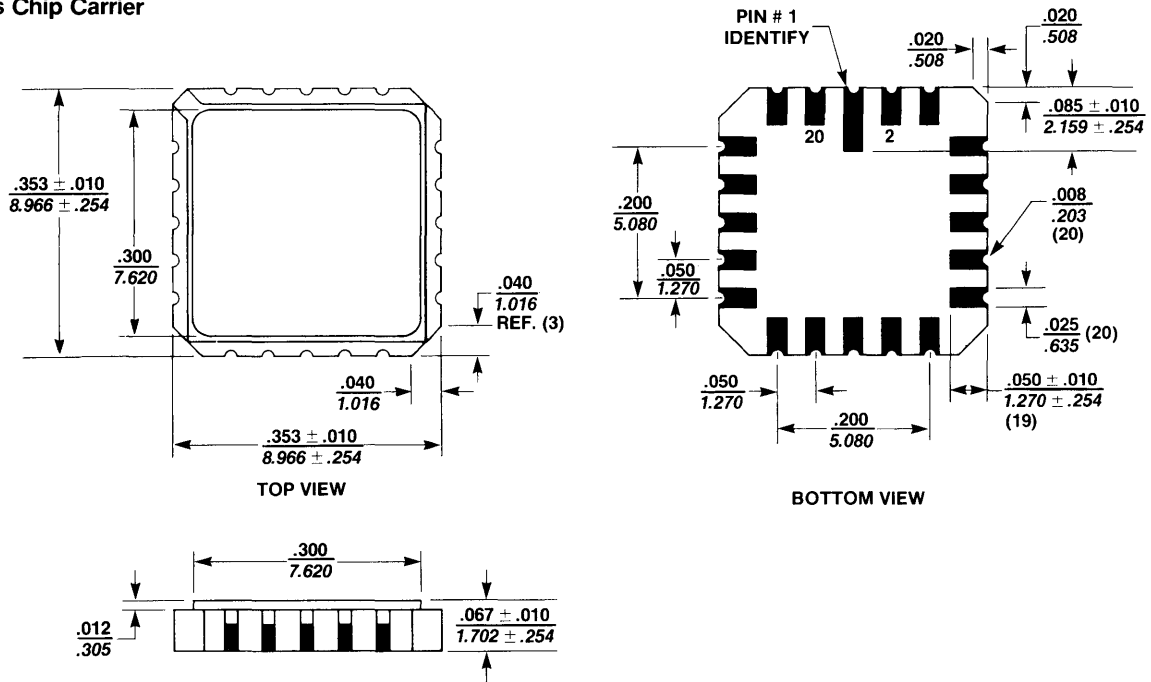
UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS

Package Drawings

J18 Ceramic DIP



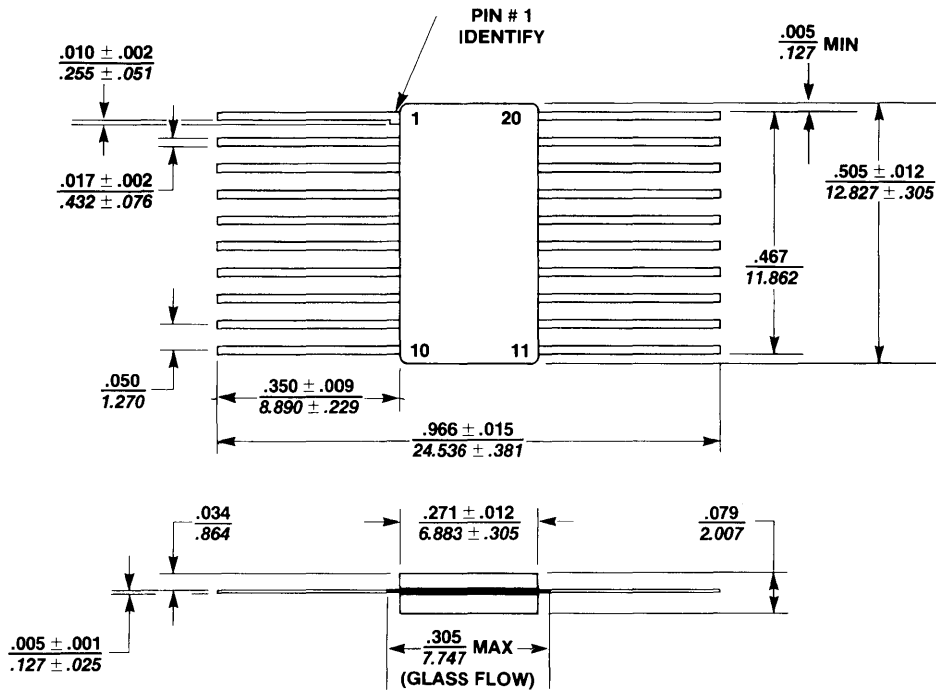
L20 Leadless Chip Carrier



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 ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS

Package Drawings

W20 CERPACK



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