M3880x Group

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M3880x group is made up of 8-bit microcomputers based on the MELPS 740 core.

The M3880x group is designed for office automation equipment, household appliances and include three timers, serial I/O function.

The various microcomputers in the M3880x group include variations of internal memory size and packaging. For details, see the section on part numbering.

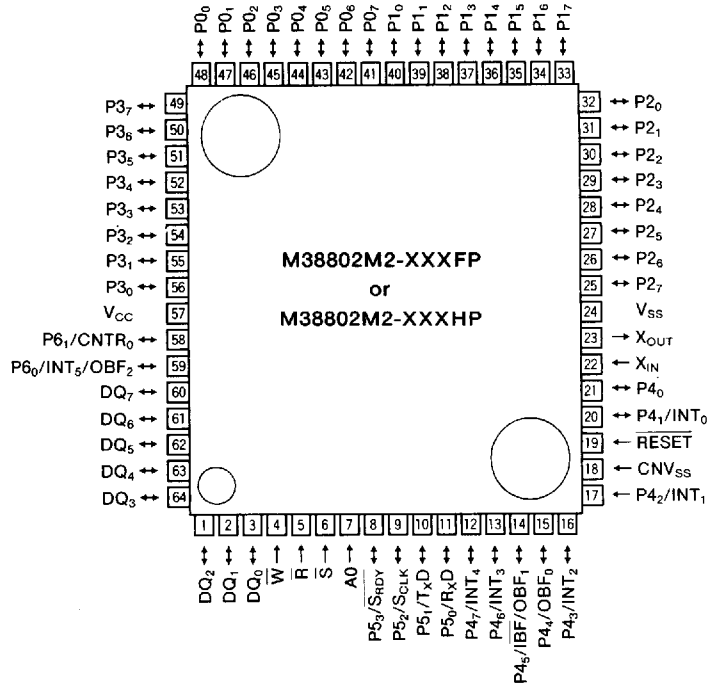
FEATURES

- Basic machine-language instructions 71
- Instruction execution time 0.5μs
  (fastest instructions at 8MHz oscillation frequency)
- Memory size
  ROM ..... 4K to 32K bytes
  RAM ..... 192 to 4096 bytes
- Programmable input/output ports 46
- Interrupts ..... 16 sources, 16 vectors
- Timers ..... 8-bit×3
- Serial I/O ..... 8-bit×1(UART or Clock-synchronized)
- Comparator circuit ..... 4-bit×8-input
- Bus interface 1byte
- Key-on wakeup 8-input
- Clock generation circuit ..... Internal feedback amplifier
  (connect to external ceramic resonator or quartz crystal)
- Supply voltage
  at 8MHz oscillation frequency ..... 4.0 to 5.5V
  at 4MHz oscillation frequency ..... 2.7 to 5.5V
- Low power dissipation 40mW
- Operating temperature range ..... −20 to 85℃

APPLICATIONS

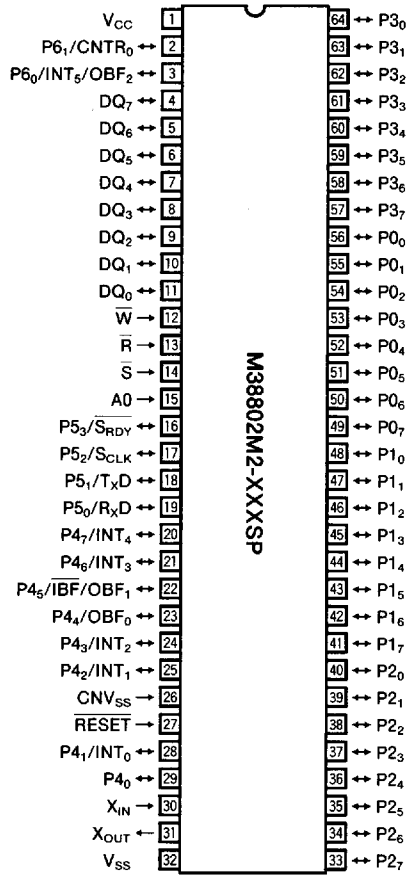
Office automation, factory automation, household appliances, and other consumer applications, etc.

PIN CONFIGURATION (TOP VIEW)



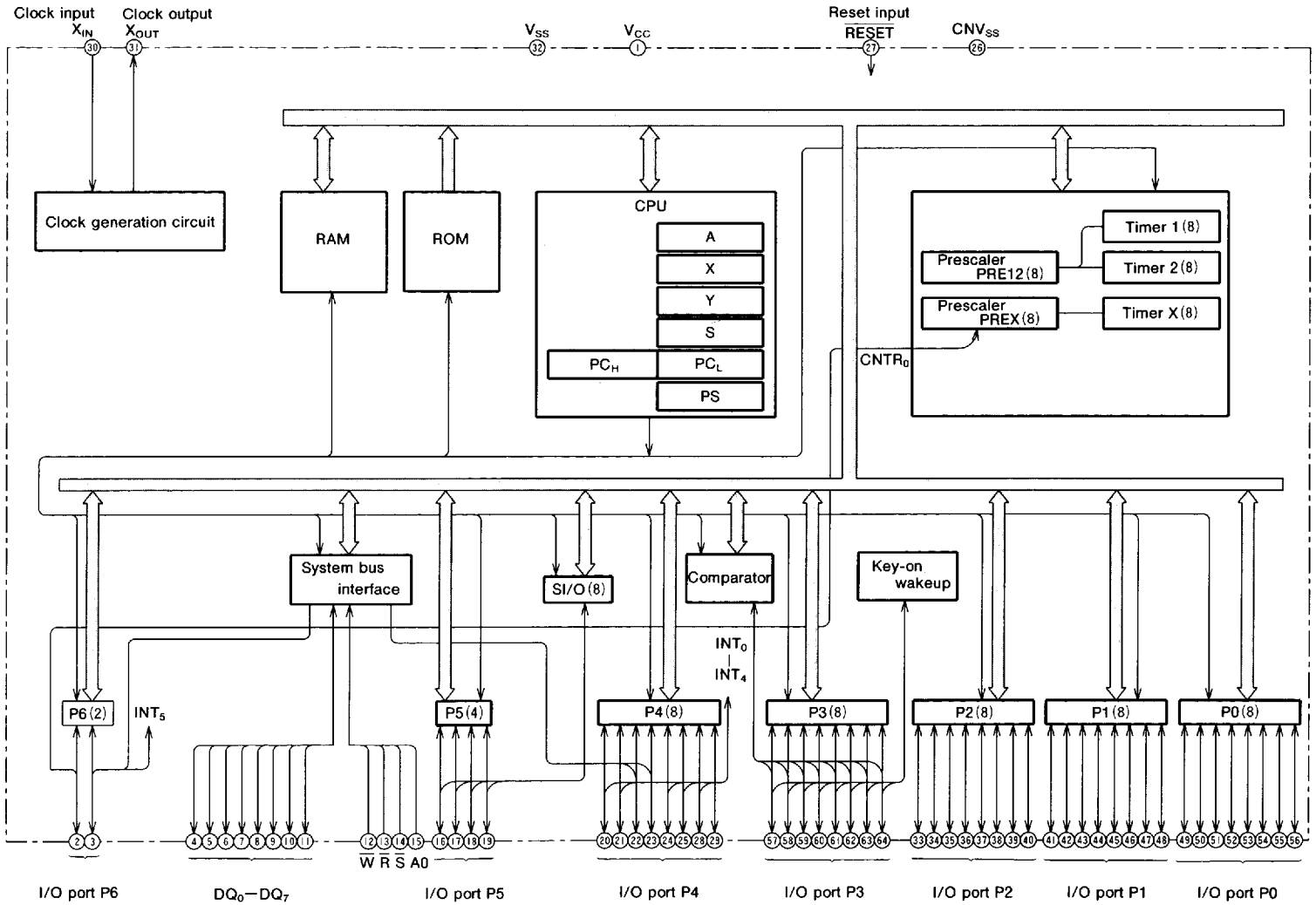
Package type : 64P6N-A/64P6D-A
64-pin plastic-molded QFP

PIN CONFIGURATION (TOP VIEW)



Package type : 64P4B
64-pin shrink plastic-molded DIP

FUNCTIONAL BLOCK DIAGRAM (Package : 64P4B)



PIN DESCRIPTION

Pin	Name	Function	Alternate Function
V_{CC}, V_{SS}	Power supply	Power supply inputs 2.7 to 5.5V to V_{CC}, and 0V to V_{SS}.	
CNV_{SS}	CNV_{SS}	This pin controls the operation mode of the chip. Normally connected to V_{SS}.	
$\overline{RESET}$	Reset input	To reset the microcomputer, this pin should be kept at an "L" level for more than 2μs under normal operating conditions.	
X_{IN}	Clock input	Input and output signals for the internal clock generation circuit. Connect a ceramic resonator or quartz crystal between the X_{IN} and X_{OUT} pins to set the oscillation frequency. If an external clock is used, connect the clock source to the X_{IN} pin and leave the X_{OUT} pin open.	
X_{OUT}	Clock output		
$P0_0$—$P0_7$	I/O port P0	An 8-bit I/O port. An I/O direction register allows each pin to be individually programmed as either input or output. The output structure of this port is CMOS 3-state, and the input levels are CMOS compatible.	
$P1_0$—$P1_7$	I/O port P1		
$P2_0$—$P2_7$	I/O port P2	An 8-bit I/O port. An I/O direction register allows each pin to be individually programmed as either input or output. The output structure of this port is CMOS 3-state, and the input levels are CMOS compatible. $P2_4$—$P2_7$ (4 bits) are enabled to output large current for LED drive.	
$P3_0$—$P3_7$	I/O port P3	An 8-bit I/O port. An I/O direction register allows each pin to be individually programmed as either input or output. The output structure of this port is CMOS 3-state, and the input levels are CMOS compatible. Pull-up control is enabled.	Key-on wakeup input pins Analog input pins
$P4_0$	I/O port P4	An 8-bit I/O port with the same function as port P0. Switching of CMOS/TTL input level is enabled. The output structure of this port is enabled to switch CMOS 3-state/N-channel open drain. In spite of setting input or output port, input of each pin is enabled.	
$P4_1/INT_0$, $P4_2/INT_1$, $P4_3/INT_2$			Interrupt input pins
$P4_4/OBF_0$, $P4_5/\overline{IBF}/OBF_1$			Data bus buffer function pins
$P4_6/INT_3$, $P4_7/INT_4$			Interrupt input pins
$P5_0/R_XD$, $P5_1/T_XD$, $P5_2/S_{CLK}$, $P5_3/\overline{S_{RDY}}$	I/O port P5	A 4-bit I/O port with the same function as port P0. The output structure of this port is CMOS 3-state, and the input levels are CMOS compatible.	Serial I/O function pins
$P6_0/INT_5/OBF_2$	I/O port P6	A 2-bit I/O port with the same function as port P0. The output structure of this port is CMOS 3-state, and the input levels are CMOS compatible.	Interrupt input pin/ Data bus buffer function pin
$P6_1/CNTR_0$			Timer X function pin
A0, $\overline{S}$, E/$\overline{R}$, R/$\overline{W}$/$\overline{W}$	Input port	Control bus for host CPU. Switching of CMOS/TTL input level is enabled.	
DQ_0—DQ_7	I/O port	An 8-bit data bus for host CPU. Switching of CMOS/TTL input level is enabled.	

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PART NUMBERING

Product name M3880 2 M 2 - XXX SP

Package type
- SP: 64P4B package
- FP: 64P6N package
- SS: 64S1B package
- FS: 64D0 package
- HP: 64P6D package

ROM number
- Omitted in some types.

ROM/PROM size
- 1 : 4096 bytes
- 2 : 8192 bytes
- 3 : 12288 bytes
- 4 : 16384 bytes
- 5 : 20480 bytes
- 6 : 24576 bytes
- 7 : 28672 bytes
- 8 : 32768 bytes

The first 128 bytes and the last two bytes of ROM are reserved areas; they can not be used.

Memory type
- M: Mask ROM version
- E : EPROM or one-time programmable version

RAM size

0 : 192 bytes	8 : 1536 bytes
1 : 256 bytes	9 : 2048 bytes
2 : 384 bytes	A : 3072 bytes
3 : 512 bytes	B : 4096 bytes
4 : 640 bytes	
5 : 768 bytes	
6 : 896 bytes	
7 : 1024 bytes	

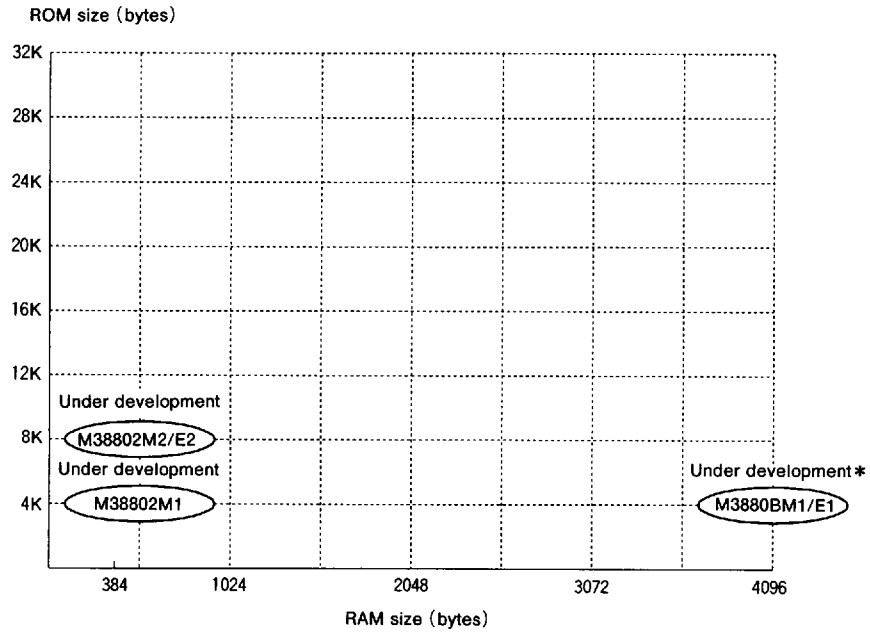
GROUP EXPANSION

Mitsubishi plans to expand the M3880x group as follows:

(1) Support for mask ROM, one-time programmable, and EPROM versions
ROM/PROM capacity ..... 4K to 8K bytes
RAM capacity ..... 384 to 4096 bytes

(2) Packages
64P4B ..... Shrink plastic molded DIP
64P6N ..... 0.8mm-pitch plastic molded QFP
64P6D ..... 0.5mm-pitch plastic molded QFP
64S1B ..... Shrink ceramic DIP
64D0 ..... 0.8mm-pitch ceramic LCC

Memory expansion plan



* : These products are supported in only 64P6N package.

The development schedule and other details of products under development may be revised without notice.

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FUNCTIONAL DESCRIPTION

Central Processing Unit (CPU)

Microcomputers of the M3880x group use the standard MELPS 740 instruction set. Refer to the table of MELPS 740 addressing modes and machine instructions or the MELPS 740 Software Manual for details on the instruction set.

Machine-resident MELPS 740 instructions are as follows:

The FST and SLW instructions are not available for use.

The STP, WIT, MUL, and DIV instructions can be used.

CPU Mode Register

The CPU mode register (address $003B_{16}$) contains the stack page select bit.

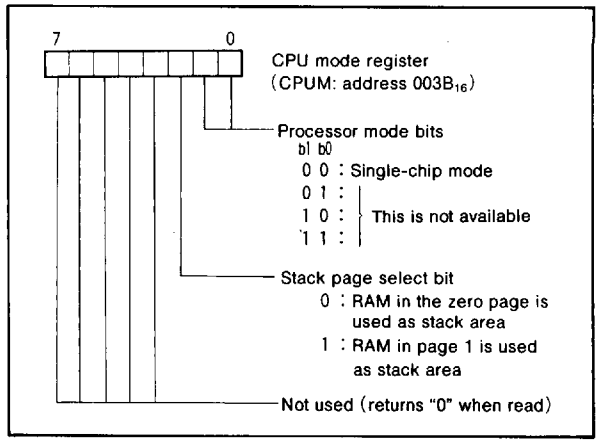

Fig. 1 Structure of CPU mode register

MEMORY

Special Function Register (SFR) Area

The Special Function Register area contains registers which control functions such as I/O ports and timers, and is located in the zero page area.

RAM

RAM is used for data storage as well for stack area.

ROM

The first 128 bytes and the last two bytes of ROM are reserved for device testing and the rest is user area for storing programs.

Interrupt Vector Area

The interrupt vector area contains reset and interrupt vectors.

Zero Page

The 256 bytes from addresses 0000_{16} to $00FF_{16}$ are called the zero page area. The internal RAM and the special function registers (SFR) are allocated to this area.

The zero page addressing mode can be used to specify memory and register addresses in the zero page area. This dedicated zero page addressing mode enables access to this area with only 2 bytes.

Special Page

The 256 bytes from addresses $FF00_{16}$ to $FFFF_{16}$ are called the special page area. The special page addressing mode can be used to specify memory addresses in the special page area. This dedicated special page addressing mode enables access to this area with only 2 bytes.

RAM area

RAM capacity (bytes)	Address $XXXX_{16}$
192	$00FF_{16}$
256	$013F_{16}$
384	$01BF_{16}$
512	$023F_{16}$
640	$02BF_{16}$
768	$033F_{16}$
896	$03BF_{16}$
1024	$043F_{16}$
1536	$063F_{16}$
2048	$083F_{16}$
3072	$0C3F_{16}$
4096	$103F_{16}$

ROM area

ROM capacity (bytes)	Address $YYYY_{16}$	Address $ZZZZ_{16}$
4096	$F000_{16}$	$F080_{16}$
8192	$E000_{16}$	$E080_{16}$
12288	$D000_{16}$	$D080_{16}$
16384	$C000_{16}$	$C080_{16}$
20480	$B000_{16}$	$B080_{16}$
24576	$A000_{16}$	$A080_{16}$
28672	9000_{16}	9080_{16}
32768	8000_{16}	8080_{16}

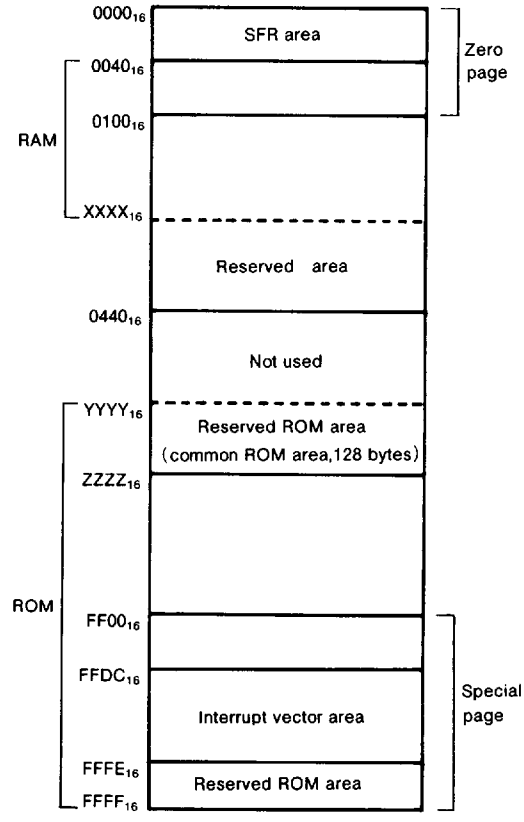

Fig. 2 Memory map diagram

0000_{16}	Port P0 (P0)
0001_{16}	Port P0 direction register (P0D)
0002_{16}	Port P1 (P1)
0003_{16}	Port P1 direction register (P1D)
0004_{16}	Port P2 (P2)
0005_{16}	Port P2 direction register (P2D)
0006_{16}	Port P3 (P3)
0007_{16}	Port P3 direction register (P3D)
0008_{16}	Port P4 (P4)
0009_{16}	Port P4 direction register (P4D)
$000A_{16}$	Port P5 (P5)
$000B_{16}$	Port P5 direction register (P5D)
$000C_{16}$	Port P6 (P6)
$000D_{16}$	Port P6 direction register (P6D)
$000E_{16}$	
$000F_{16}$	
0010_{16}	
0011_{16}	
0012_{16}	
0013_{16}	Port P3 pull-up control register (PULLP3)
0014_{16}	Port P4 input register (P4I)
0015_{16}	Port P4 control register (P4C)
0016_{16}	
0017_{16}	
0018_{16}	Transmit/receive buffer (TB/RB)
0019_{16}	Serial I/O status register (SIOSTS)
$001A_{16}$	Serial I/O control register (SIOCON)
$001B_{16}$	UART control register (UARTCON)
$001C_{16}$	Baud rate generator (BRG)
$001D_{16}$	
$001E_{16}$	
$001F_{16}$	

0020_{16}	Prescaler 12 (PRE12)
0021_{16}	Timer 1 (T1)
0022_{16}	Timer 2 (T2)
0023_{16}	Timer X mode register (TM)
0024_{16}	Prescaler X (PREX)
0025_{16}	Timer X (TX)
0026_{16}	
0027_{16}	
0028_{16}	Data bus buffer register (DBB)
0029_{16}	Data bus buffer status register (DBBSTS)
$002A_{16}$	Data bus buffer control register (DBBCON)
$002B_{16}$	
$002C_{16}$	
$002D_{16}$	
$002E_{16}$	
$002F_{16}$	
0030_{16}	Comparator control register (CMPCON)
0031_{16}	Comparator data register (CMPD)
0032_{16}	
0033_{16}	
0034_{16}	
0035_{16}	
0036_{16}	
0037_{16}	
0038_{16}	
0039_{16}	
$003A_{16}$	Interrupt edge selection register (INTEDGE)
$003B_{16}$	CPU mode register (CPUM)
$003C_{16}$	Interrupt request register 1 (IREQ1)
$003D_{16}$	Interrupt request register 2 (IREQ2)
$003E_{16}$	Interrupt control register 1 (ICON1)
$003F_{16}$	Interrupt control register 2 (ICON2)

Fig. 3 Memory map of special function register (SFR)

I/O PORTS

Direction Registers

The M3880x group microprocessors have 46 programmable I/O pins arranged in seven I/O ports (ports P0 to P6). The I/O ports have direction registers which determine the input/output direction of each individual pin. Each bit in a direction register corresponds to one pin, each pin can be set to be input or output. When "0" is written to the bit corresponding to a pin, that pin becomes an input pin. When "1" is written to that bit, that pin becomes an output pin.

If data is read from a pin which is set for output, the value of the port output latch is read, not the value of the pin itself. Pins set to input are floating. If a pin set to input is written to, only the port output latch is written to and the pin remains floating.

As the special function only port P4, in spite of setting input port or output port, the value of pin can be read by reading port P4 input register (address 0014_{16}).

Pin	Name	Input/Output	I/O Format	Non-Port Function	Related SFRs	Ref. No.
$P0_0$—$P0_7$	Port P0	Input/output, individual bits	CMOS 3-state output CMOS level input			(1)
$P1_0$—$P1_7$	Port P1	Input/output, individual bits	CMOS 3-state output CMOS level input			
$P2_0$—$P2_7$	Port P2	Input/output, individual bits	CMOS 3-state output CMOS level input			
$P3_0$—$P3_7$	Port P3	Input/output, individual bits	CMOS 3-state output CMOS level input	Key-on wakeup input Analog input	Port P3 pull-up control register	(2)
$P4_0$	Port P4	Input/output, individual bits	CMOS/N-channel open-drain output CMOS/TTL level input			(3)
$P4_1/INT_0$, $P4_2/INT_1$, $P4_3/INT_2$				External interrupt input	Interrupt edge selection register	(4)
$P4_4/\overline{OBF_0}$, $P4_5/\overline{IBF}$/ $\overline{OBF_1}$				Data bus buffer function output	Data bus buffer control register	(5) (6)
$P4_6/INT_3$, $P4_7/INT_4$				External interrupt input	Interrupt edge selection register	(4)
$P5_0/R_XD$, $P5_1/T_XD$, $P5_2/S_{CLK}$, $P5_3/\overline{S_{RDY}}$	Port P5	Input/output, individual bits	CMOS 3-state output CMOS level input	Serial I/O function input/output	Serial I/O control register	(7) (8) (9) (10)
$P6_0/INT_5/\overline{OBF_2}$	Port P6	Input/output, individual bits	CMOS 3-state output CMOS level input	External interrupt input Data bus buffer function output	Interrupt edge selection register Data bus buffer control register	(11)
$P6_1/CNTR_0$				Timer X function input/output		(12)

Note : For details of the functions of ports PO to P3 in modes other than sigle-chip mode, and how to use double-function ports as function I/O ports. See the applicable sections.

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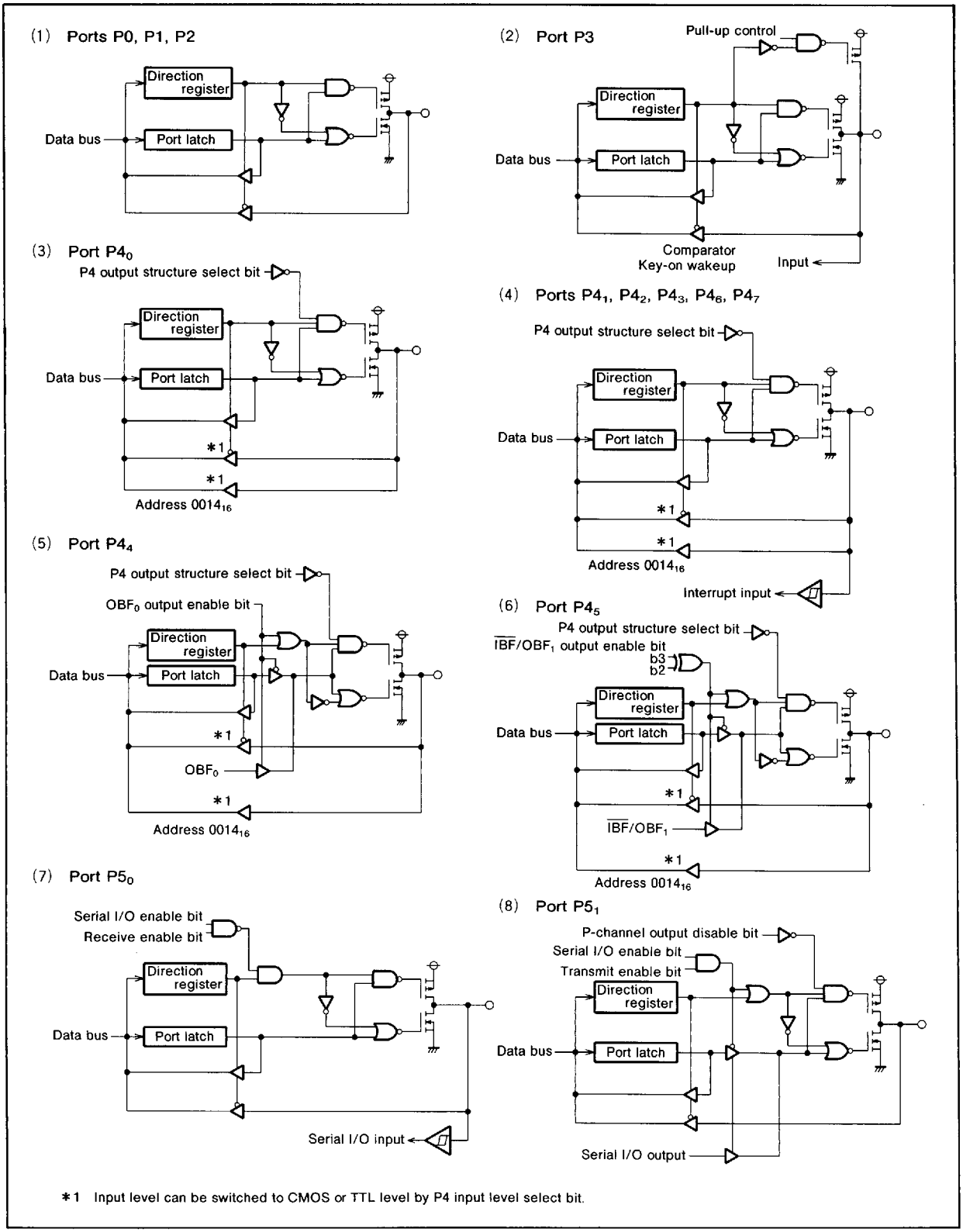
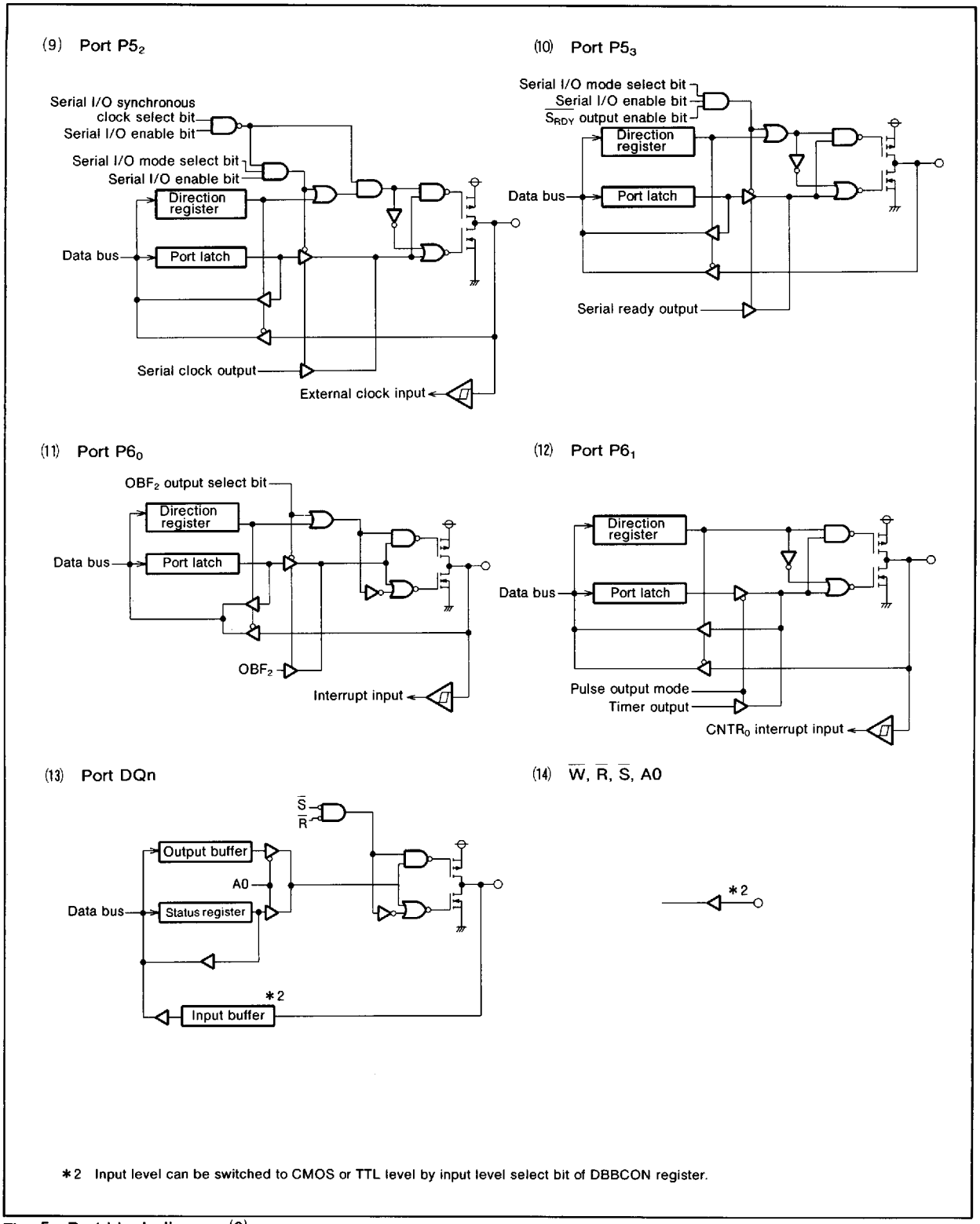


*1 Input level can be switched to CMOS or TTL level by P4 input level select bit.

Fig. 4 Port block diagram (1)



*2 Input level can be switched to CMOS or TTL level by input level select bit of DBBCON register.

Fig. 5 Port block diagram (2)

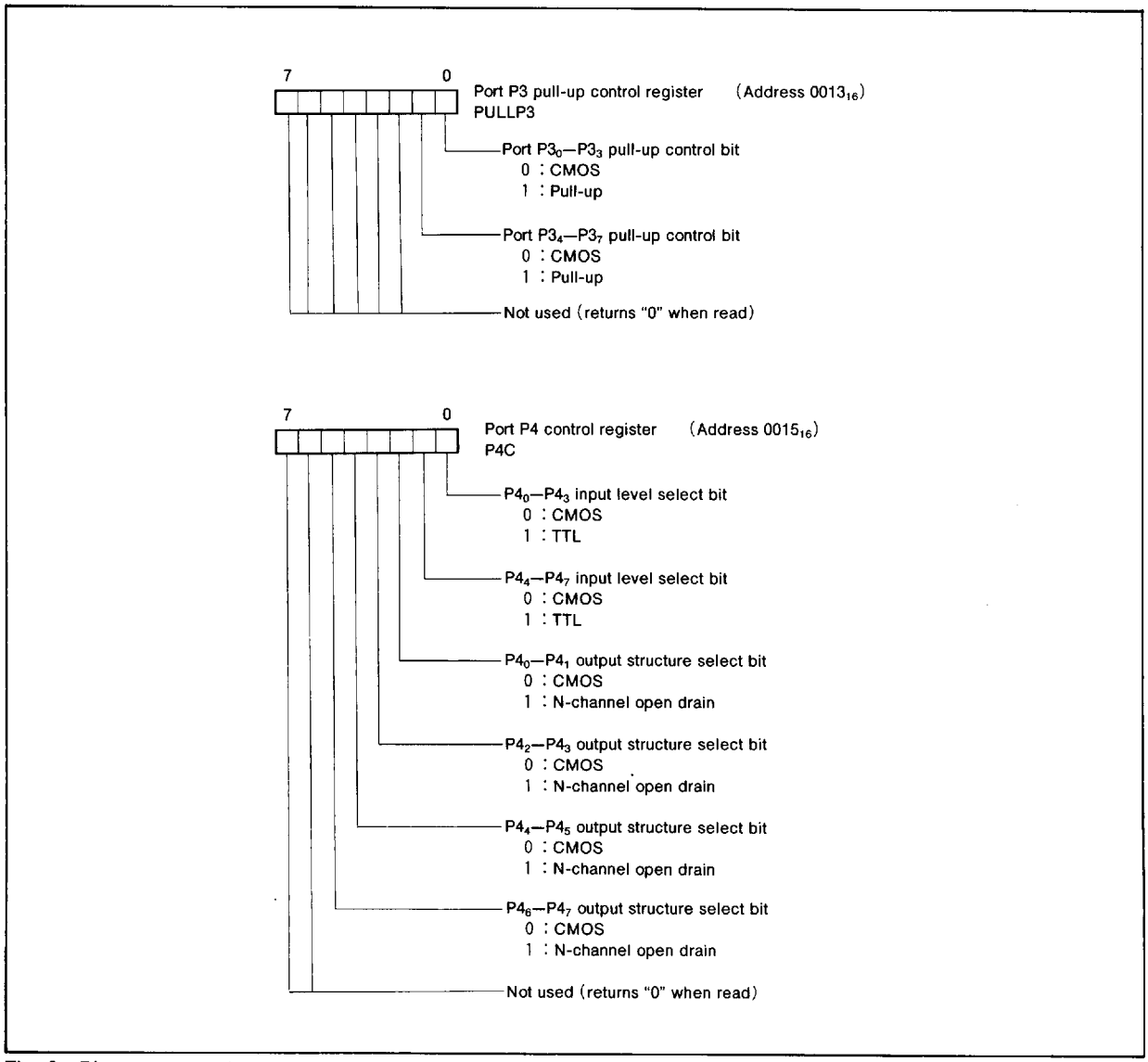


Fig. 6 Bits structure of port I/O related registers

INTERRUPTS

A total of 16 sources can generate interrupts: 8 external, 7 internal, and 1 software.

Interrupt Control

Each interrupt is controlled by an interrupt request bit, an interrupt enable bit, and the interrupt disable flag-except for the software interrupt set by the BRK instruction. An interrupt is generated if the corresponding interrupt request and enable bits are "1" and the interrupt disable flag is "0".

Interrupt enable bits can be set or cleared by software.

Interrupt request bits can be cleared by software, but cannot be set by software.

The I flag disables all interrupts except for the BRK instruction interrupt.

Interrupt Operation

When an interrupt is received, the program counter and processor status register are automatically pushed onto the stack. The interrupt disable flag is set to inhibit other interrupts from interfering. The corresponding interrupt request bit is cleared and the interrupt jump destination address is read from the vector table into the program counter.

Notes on Use

If you will change interrupt edge selection from rising edge to falling edge (INT_0 to INT_5, $CNTR_0$), interrupt request bit will be set to "1" automatically. Therefore, please make following process;

(1) Disable interrupts.
(2) Set the interrupt edge selection register (timer X mode register when using $CNTR_0$).
(3) Clear interrupt request which is selected.
(4) Enable interrputs.

Table 1 Interrupt vector addresses and priorities

Interrupt cause	Priority	Vector address (Note 1)		Interrupt request generation conditions	Remarks
		High	Low		
Reset (Note 2)	1	$FFFD_{16}$	$FFFC_{16}$	At reset	Non-maskable
Input buffer full (IBF)	2	$FFFB_{16}$	$FFFA_{16}$	At writing input data bus buffer	
Output buffer empty (OBE)	3	$FFF9_{16}$	$FFF8_{16}$	At reading output data bus buffer	
INT_0	4	$FFF7_{16}$	$FFF6_{16}$	At detection of either rising or falling edge of INT_0 input	External interrupt (active edge selectable)
Serial I/O reception	5	$FFF5_{16}$	$FFF4_{16}$	At end of serial I/O data reception	Valid when serial I/O is selected
Serial I/O transmission	6	$FFF3_{16}$	$FFF2_{16}$	At end of serial I/O transfer shift or when transmission buffer is empty	Valid when serial I/O is selected
Timer X	7	$FFF1_{16}$	$FFF0_{16}$	At timer X overflow	
Timer 1	8	$FFEF_{16}$	$FFEE_{16}$	At timer 1 overflow	STP release timer overflow
Timer 2	9	$FFED_{16}$	$FFEC_{16}$	At timer 2 overflow	
$CNTR_0$	10	$FFEB_{16}$	$FFEA_{16}$	At detection of either rising or falling edge of $CNTR_0$ input	External interrupt (active edge selectable)
INT_1	11	$FFE9_{16}$	$FFE8_{16}$	At detection of either rising or falling edge of INT_1 input	External interrupt (active edge selectable)
INT_2	12	$FFE7_{16}$	$FFE6_{16}$	At detection of either rising or falling edge of INT_2 input	External interrupt (active edge selectable)
INT_3	13	$FFE5_{16}$	$FFE4_{16}$	At detection of either rising or falling edge of INT_3 input	External interrupt (active edge selectable)
INT_4	14	$FFE3_{16}$	$FFE2_{16}$	At detection of either rising or falling edge of INT_4 input	External interrupt (active edge selectable)
INT_5	15	$FFE1_{16}$	$FFE0_{16}$	At detection of either rising or falling edge of INT_5 input	External interrupt (active edge selectable)
Key-on wakeup	16	$FFDF_{16}$	$FFDE_{16}$	At falling of AND of port P3 input logic level	External interrupt (Valid when falling is detected)
BRK instruction	17	$FFDD_{16}$	$FFDC_{16}$	At BRK instruction execution	Non-maskable software interrupt

Note 1 : Vector addresses contain interrupt jump destination addresses.
2 : Reset function in the same way as an interrupt with the highest priority.

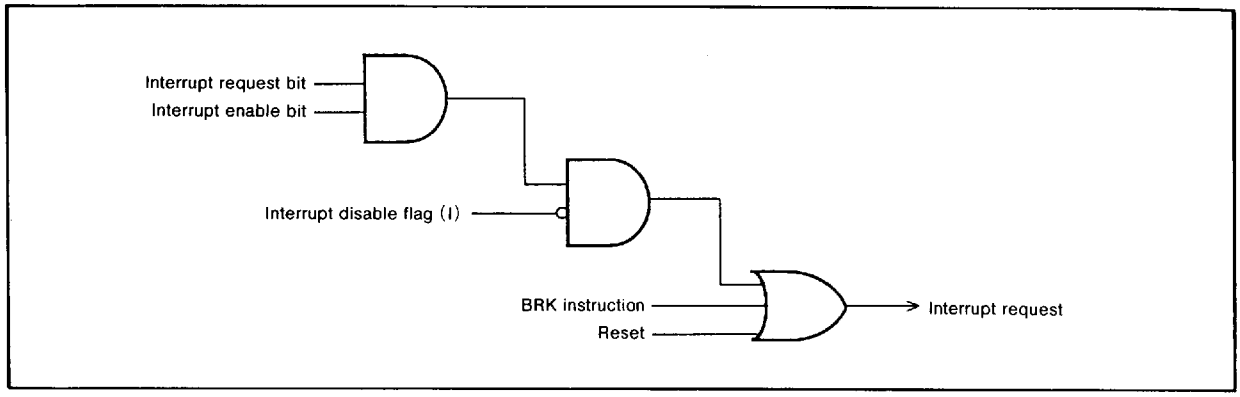


Fig. 7 Interrupt control

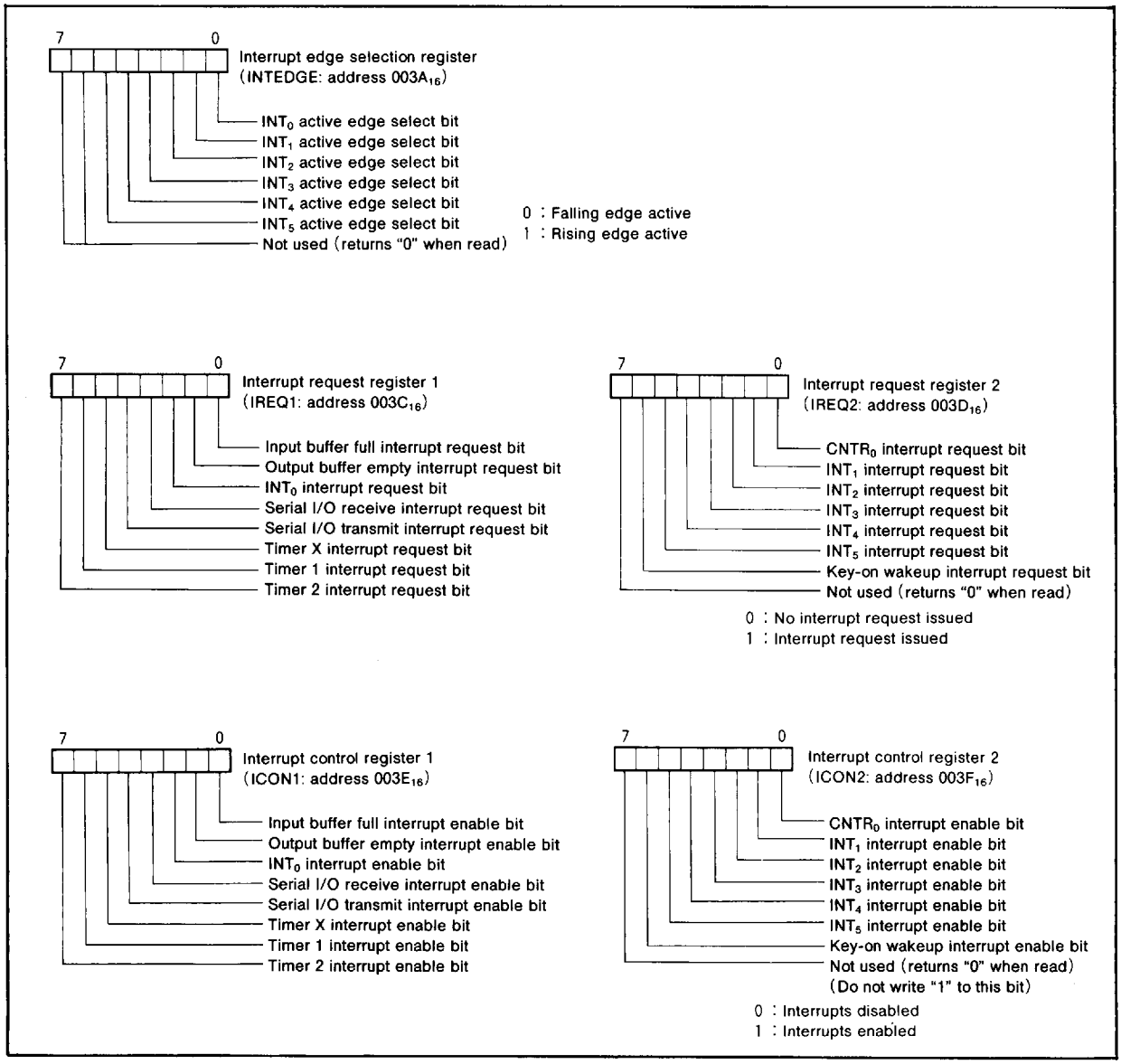


Fig. 8 Structure of interrupt-related registers

KEY-ON WAKEUP

A key-on wakeup interrupt request is generated by applying "L" level to any pin of port P3 that have been set to input mode. In other words, it is generated when AND of input level goes from "1" to "0". An example of using a key-on wakeup interrupt is shown in Figure 9, where an interrupt request is generated by pressing one of the keys consisted as an active-low key matrix which inputs to ports $P3_0$—$P3_3$.

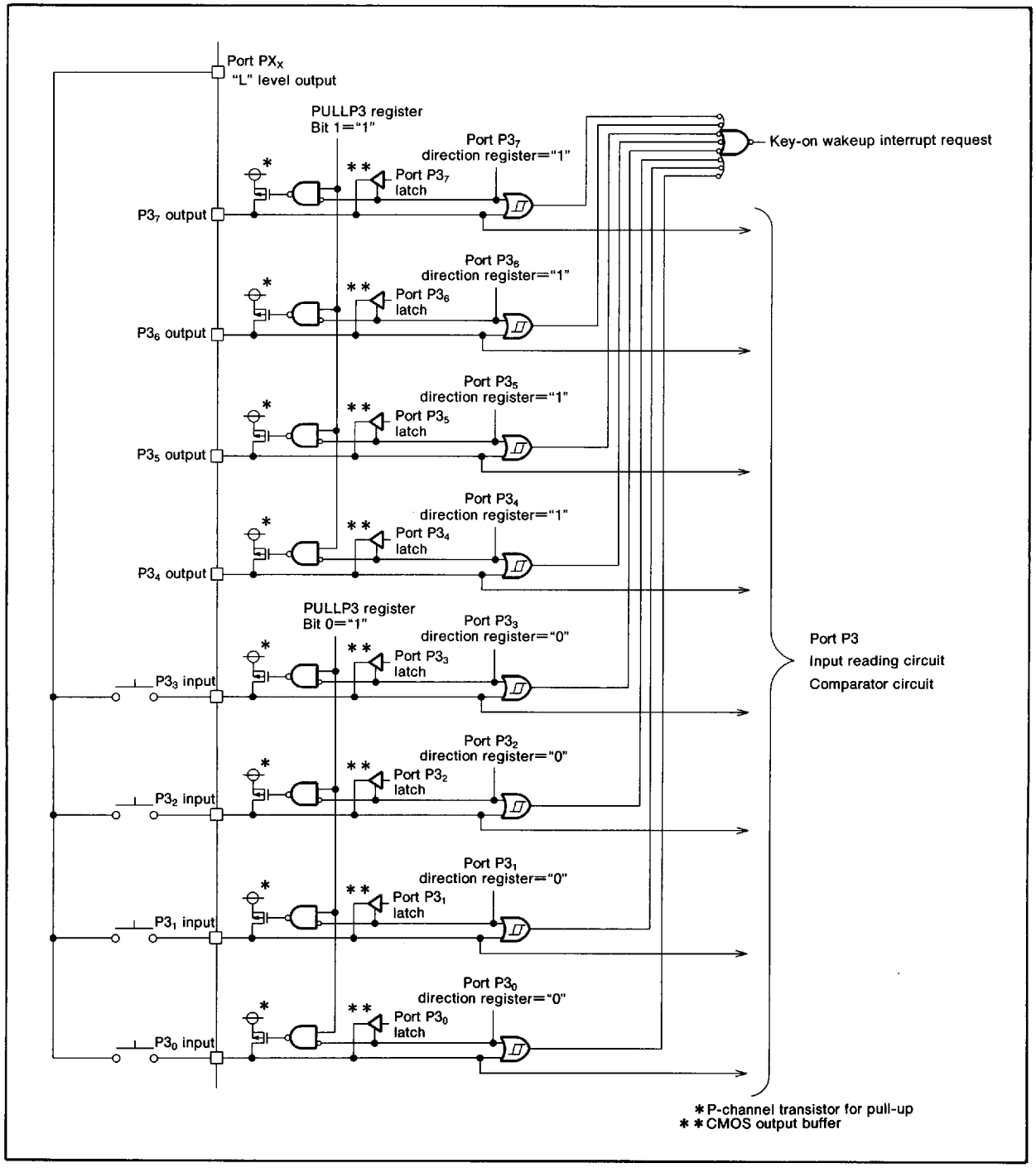


Fig. 9 Connection example when using key-on wakeup interrupt and port P3 block diagram

TIMERS

Microcomputers of the M3880x group have 3 timers: timer X, timer 1, and timer 2.

The timers count down. Once a timer reaches 00_{16}, the next count pulse reloads the contents of the corresponding timer latch into the timer, and sets the corresponding interrupt request bit to 1.

The division ratio of each timer or prescaler is given by $1/(n+1)$, where n is the value in the corresponding timer or prescaler latch.

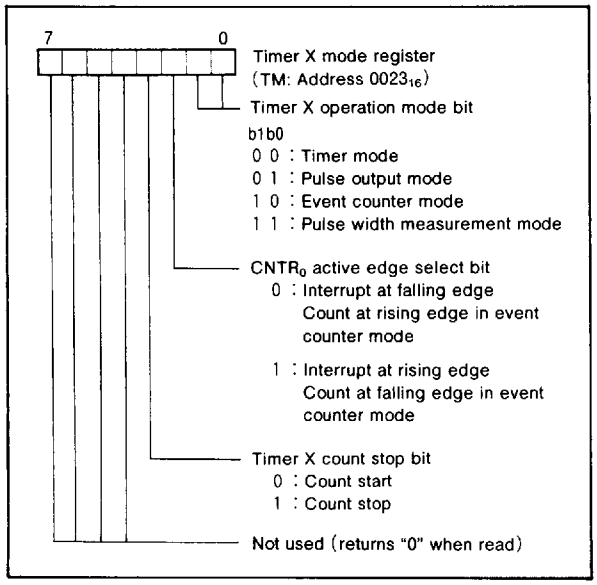


Fig. 10 Structure of timer X register

Timer 1 and Timer 2

The count source of prescaler 12 is the oscillation frequency divided by 16. The output of prescaler 12 is counted by timer 1 and timer 2, and a timer overflow sets the interrupt request bit.

Timer X

Timer X can be set to operate in one of four operating modes by setting the timer X mode register.

Timer mode

In timer mode, the timer counts a signal that is the oscillation frequency divided by 16.

Pulse output mode

Timer X counts a signal which is the oscillation frequency divided by 16. Whenever the contents of the timer reach "0", the signal output from the $CNTR_0$ pin is inverted. If the $CNTR_0$ active edge select bit is "0", output begins at "H". If it is "1", output starts at "L". When using a timer in this mode, set the corresponding port $P6_1$ direction register to output mode.

Event counter mode

Operation in event counter mode is the same as in timer mode, except the timer counts signals input through the $CNTR_0$ pin.

Pulse width measurement mode

If the $CNTR_0$ active edge select bit is "0", the timer counts at the oscillation frequency divided by 16 while the $CNTR_0$ pin is at "H". If the $CNTR_0$ active edge select bit is "1", the count continues during the time that the $CNTR_0$ pin is at "L".

In all of these modes, the count can be stopped by setting the timer X count stop bit to "1". Every time a timer overflows, the corresponding interrupt request bit is set.

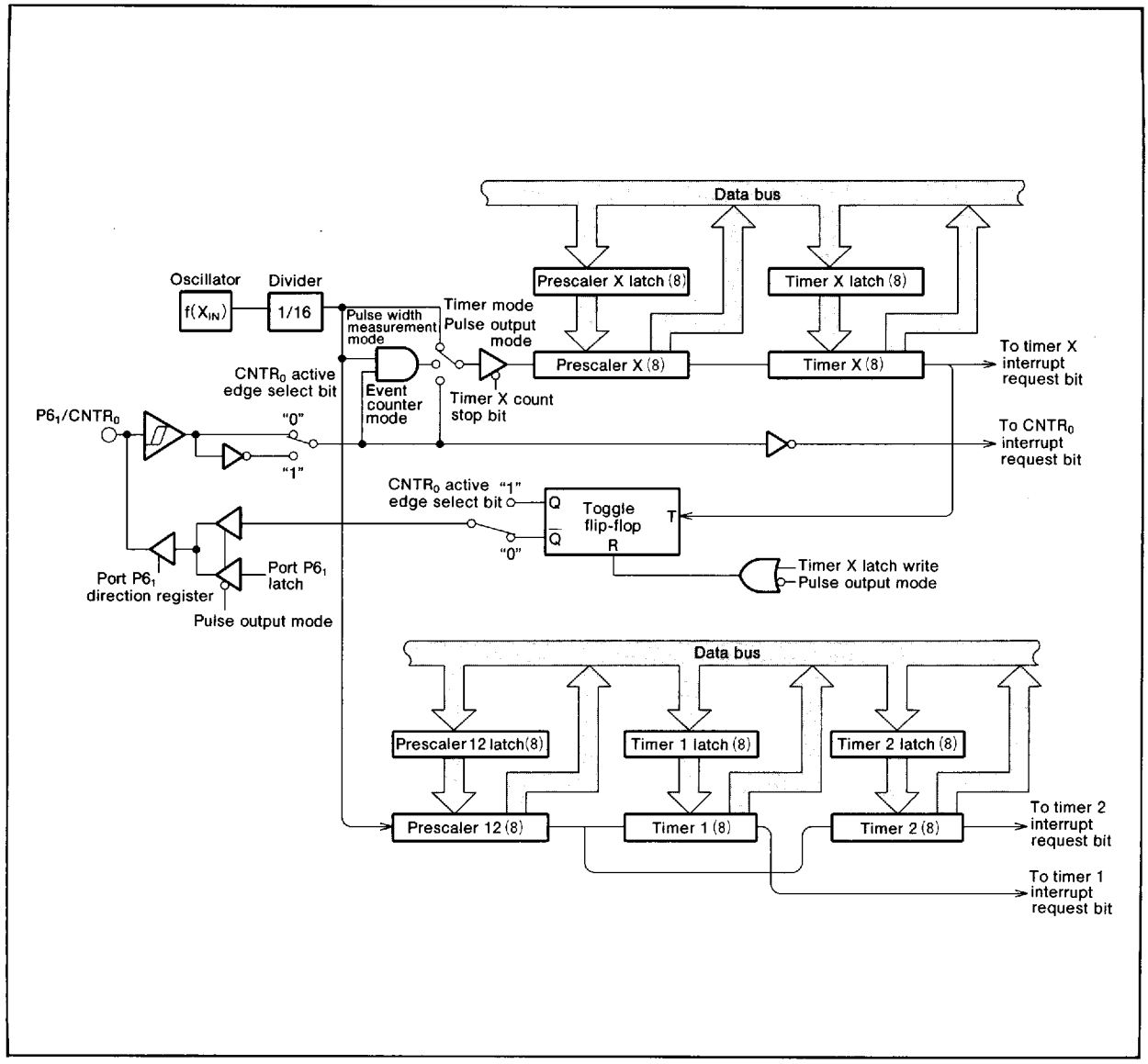


Fig. 11 Block diagram of timer X, timer 1 and timer 2

SERIAL I/O

Serial I/O can be used as either clock synchronous or asynchronous (UART) serial I/O. A dedicated timer is also provided for baud rate generation.

Clock Synchronous Serial I/O Mode

Clock synchronous serial I/O mode can be selected by setting the serial I/O mode select bit of the serial I/O control register to "1".

For clock synchronous serial I/O, the transmitter and the receiver must use the same clock. If an internal clock is used, transfer is started by a write signal to the transmit or receive buffer.

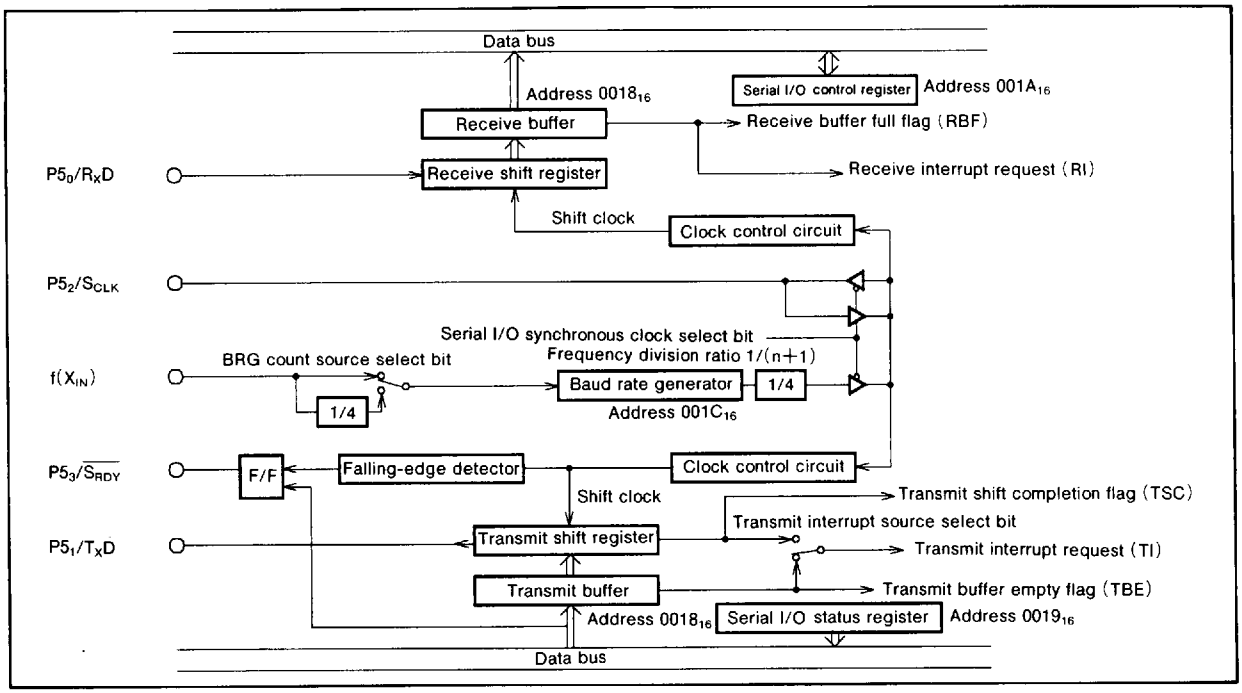
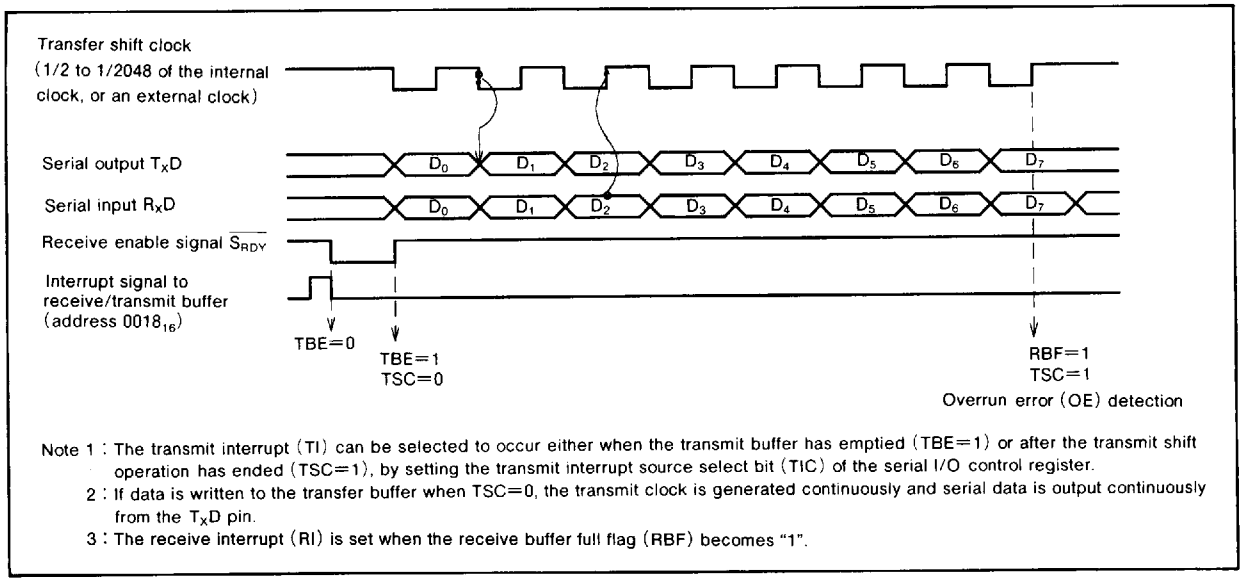


Fig. 12 Block diagram of clock synchronous serial I/O



Note 1 : The transmit interrupt (TI) can be selected to occur either when the transmit buffer has emptied (TBE=1) or after the transmit shift operation has ended (TSC=1), by setting the transmit interrupt source select bit (TIC) of the serial I/O control register.
2 : If data is written to the transfer buffer when TSC=0, the transmit clock is generated continuously and serial data is output continuously from the TxD pin.
3 : The receive interrupt (RI) is set when the receive buffer full flag (RBF) becomes "1".

Fig. 13 Operation of clock synchronous serial I/O function

Asynchronous Serial I/O (UART) Mode

Clock asynchronous serial I/O mode (UART) can be selected by clearing the serial I/O mode select bit of the serial I/O control register to "0".

Eight serial data transfer formats can be selected, and the transfer formats used by a transmitter and receiver must be identical.

The transmit and receive shift registers each have a buffer, but the two buffers have the same address in memory. Since the shift register cannot be written to or read from directly, transmit data is written to the transmit buffer, and receive data is read from the receive buffer. The transmit buffer can also hold the next data to be transmitted, and the receive buffer can hold a character while the next character is being received.

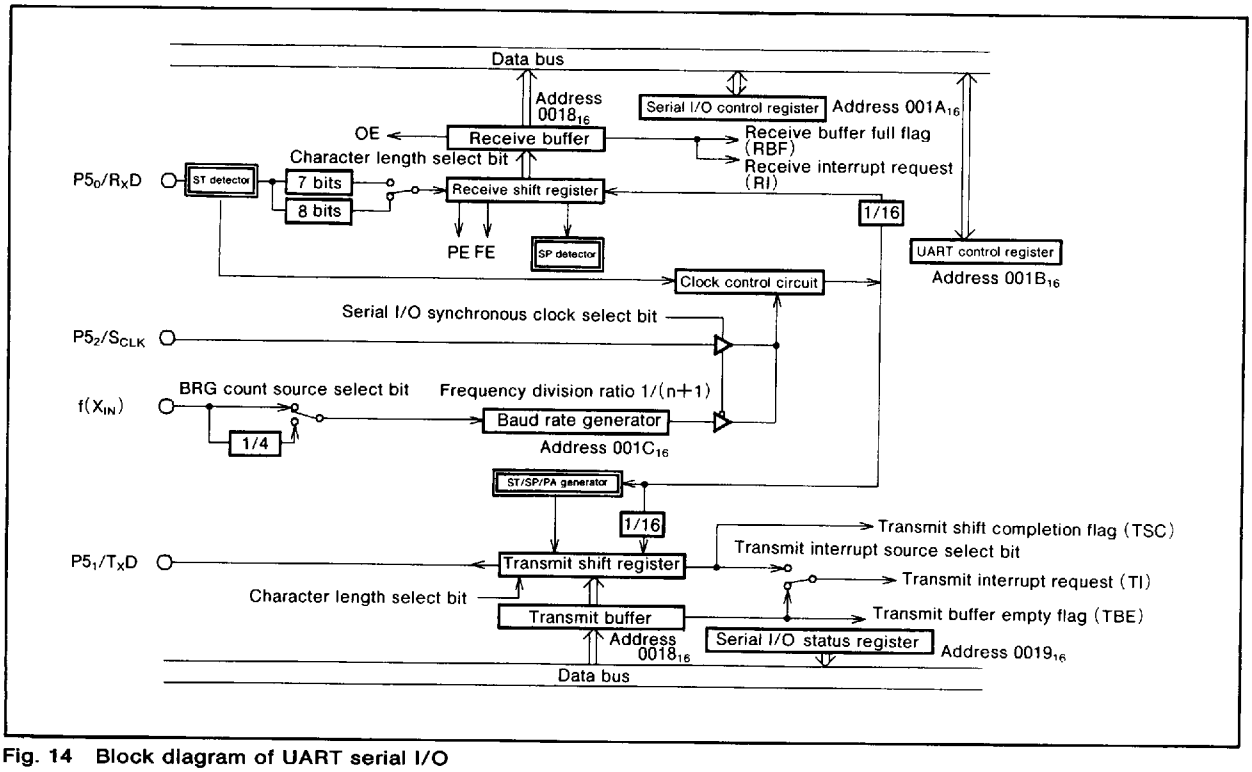
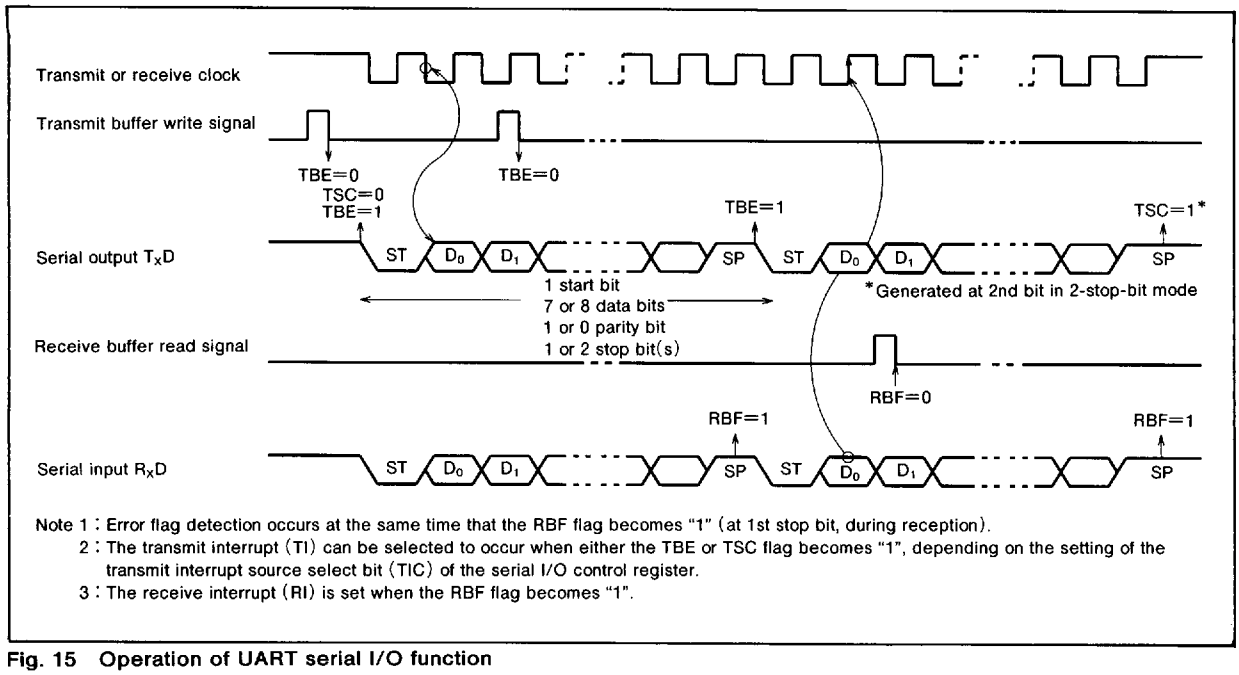


Fig. 14 Block diagram of UART serial I/O



Note 1 : Error flag detection occurs at the same time that the RBF flag becomes "1" (at 1st stop bit, during reception).
2 : The transmit interrupt (TI) can be selected to occur when either the TBE or TSC flag becomes "1", depending on the setting of the transmit interrupt source select bit (TIC) of the serial I/O control register.
3 : The receive interrupt (RI) is set when the RBF flag becomes "1".

Fig. 15 Operation of UART serial I/O function

Serial I/O Control Register (SIOCON) $001A_{16}$

The serial I/O control register contains 8 control bits for the serial I/O function.

UART Control Register (UARTCON) $001B_{16}$

The UART control register consists of 4 control bits (bits 0 to 3) which are valid when asynchronous serial I/O is selected and set the data format of data transfer. One bit in this register (bit 4) is always valid and sets the output structure of the $P5_1/T_xD$ pin.

Serial I/O Status Register (SIOSTS) 0019_{16}

The read-only serial I/O status register consists of 7 flags (bits 0 to 6) which indicate the operating status of the serial I/O function and various errors.

3 of the flags (bits 4 to 6) are valid only in UART mode.

The receive buffer full flag (bit 1) is cleared to "0" when the receive buffer is read.

If there is an error, it is detected at the same time that data is transferred from the receive shift register to the receive buffer, and the receive buffer full flag is set. A write to the serial I/O status register clears all the error flags OE, PE, FE, and SE (bit 3 to bit 6, respectively). Writing "0" to the serial I/O enable bit SIOE (bit 7 of the Serial I/O Control Register) also clears all the status flags, including the error flags.

All bits of the serial I/O status register are initialized to "0" at reset, but if the transmit enable bit (bit 4) of the serial I/O control register has been set to "1", the transmit shift completion flag (bit 2) and the transmit buffer empty flag (bit 0) become "1".

Transmit Buffer/Receive Buffer (TB/RB) 0018_{16}

The transmit buffer and the receive buffer are located at the same address. The transmit buffer is write-only and the receive buffer is read-only. If a character bit length is 7 bits, the MSB of data stored in the receive buffer is "0".

Baud Rate Generator (BRG) $001C_{16}$

The baud rate generator determines the baud rate for serial transfer.

The baud rate generator divides the frequency of the count source by $1/(n+1)$, where n is the value written to the Baud Rate Generator.

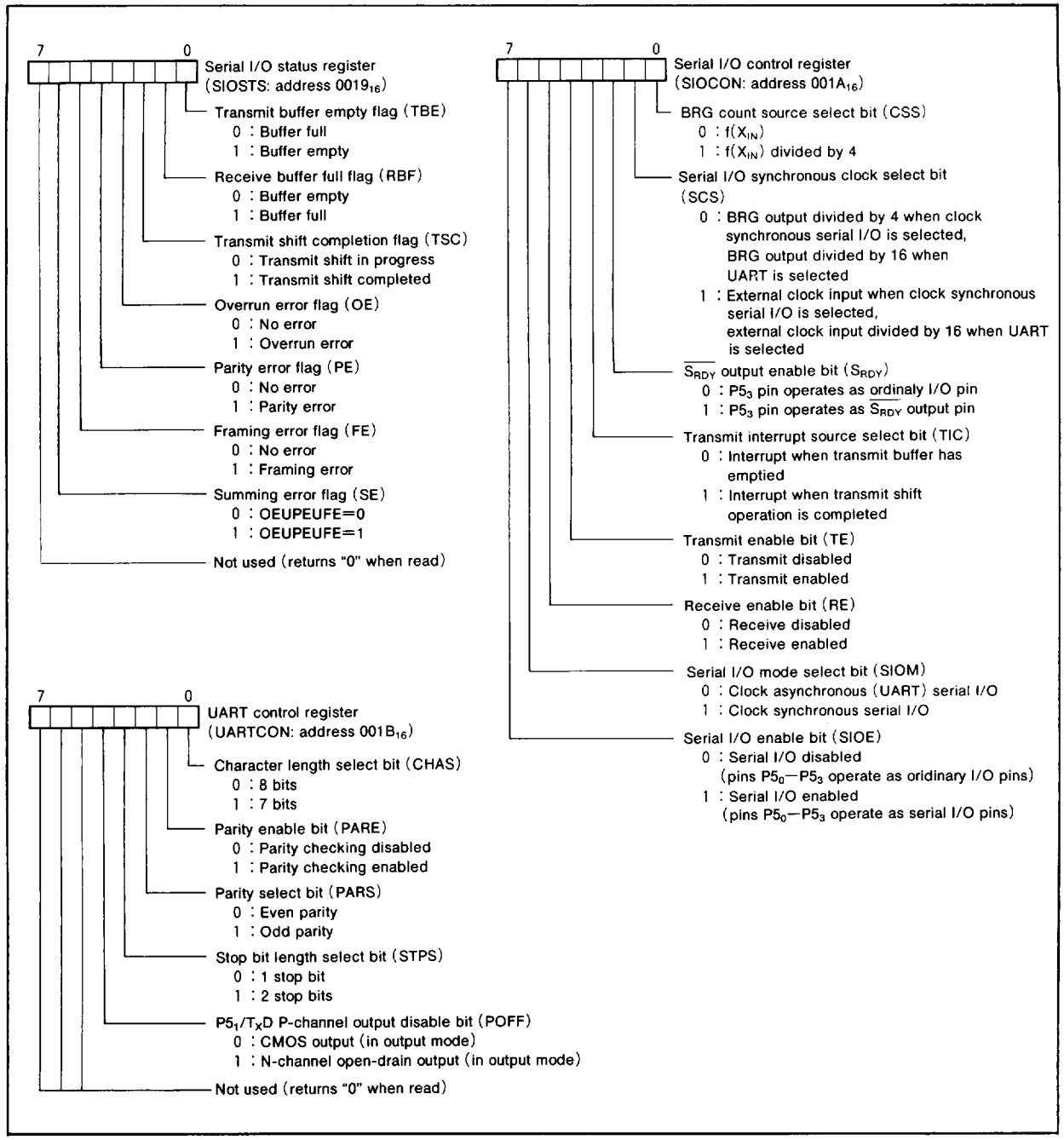


Fig. 16 Structure of serial I/O control registers

COMPARATOR CIRCUIT

Comparator Configuration

The comparator circuit consists of a switch tree, ladder resistors, a comparator, a comparator control circuit, a comparator control register (address 0030_{16}),comparator data register (address 0031_{16}), and an analog input pin ($P3_0$—$P3_7$). The analog input pin ($P3_0$—$P3_7$) also functions as an ordinary digital port.

The comparator control register is a 4-bit register of which bits 0 to 3 can be used to generate internal reference voltages in steps of 1/16 V_{CC}. The result of the comparison between the analog input voltage and an internal reference voltage is stored in comparator data register. The value in comparator control register cannot be read.

Comparator Operation

To activate the comparator, first set port P3 to input mode by setting the corresponding direction register (address 0007_{16}) to "0"—this ensures that port P3 is used as an analog input pin. Then write a digital value corresponding to the internal reference voltage into bits 0 to 3 of the comparator control register (address 0030_{16}). This write operation immediately activates the comparison. After 14 cycles of the system clock ϕ (the time required for the comparison), the comparison result is stored in comparator data register (address 0031_{16}).

If the analog input voltage is greater than the internal reference voltage, each bit of comparator data register is "1"; if it is less than the internal reference voltage, each bit of comparator data register is "0" by the state of corresponding port $P3_0$ — $P3_7$. To perform another comparison, the comparator must be written to again, even if the same internal reference voltage is to be used.

Make sure that the result is not read out until at least 14 cycles have elapsed after the comparator starts operation.

During the 14 cycles necessary for the comparison, the ladder resistors are on and the reference voltage is generated. While the comparator is not actually operating, the ladder resistors are turned off in order to prevent that current is wasted unnecessarily.

The comparator consisted of capacity coupling will lose power if its clock frequency is low. Make sure that the clock frequency of the comparator in operation is at least 1 MHz.

Do not execute the STP instruction, WIT instruction, and port P3 I/O instructions.

Table 2 Correspondence between bits 0 to 3 of the comparator control register and internal reference voltage

Comparator control register				Internal reference voltage
Bit 3	Bit 2	Bit 1	Bit 0	
0	0	0	0	$1/32V_{CC}$
0	0	0	1	$1/16V_{CC}+1/32V_{CC}$
0	0	1	0	$2/16V_{CC}+1/32V_{CC}$
0	0	1	1	$3/16V_{CC}+1/32V_{CC}$
0	1	0	0	$4/16V_{CC}+1/32V_{CC}$
0	1	0	1	$5/16V_{CC}+1/32V_{CC}$
0	1	1	0	$6/16V_{CC}+1/32V_{CC}$
0	1	1	1	$7/16V_{CC}+1/32V_{CC}$
1	0	0	0	$8/16V_{CC}+1/32V_{CC}$
1	0	0	1	$9/16V_{CC}+1/32V_{CC}$
1	0	1	0	$10/16V_{CC}+1/32V_{CC}$
1	0	1	1	$11/16V_{CC}+1/32V_{CC}$
1	1	0	0	$12/16V_{CC}+1/32V_{CC}$
1	1	0	1	$13/16V_{CC}+1/32V_{CC}$
1	1	1	0	$14/16V_{CC}+1/32V_{CC}$
1	1	1	1	$15/16V_{CC}+1/32V_{CC}$

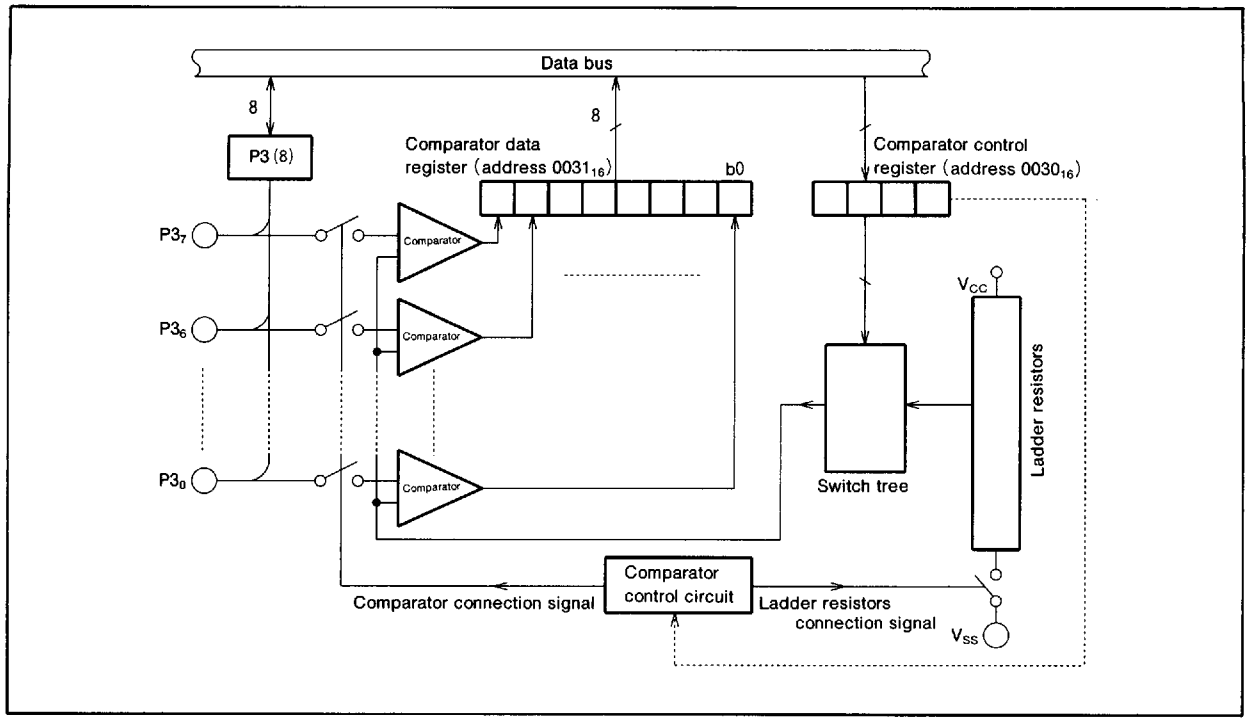


Fig. 17 Comparator circuit

BUS INTERFACE

The M3880x group has an internal bus interface function that is basically the same as that of the MELPS 8-41 series, and thus it can be operated in slave mode by control signals from the host CPU.

The bus interface can be connected directly to either an R/$\overline{W}$ type of CPU or a CPU with separated $\overline{RD}$ and $\overline{WR}$ signals. A block diagram of the bus interface function is shown in Figure19.

Slave mode is selected by bit 7 of the data bus buffer control register (address $002A_{16}$), as shown in Figure 18.

When data is written to the microcomputer from the host CPU, an input buffer full interrupt request is generated. Similarly, when data is read from the host CPU, an output buffer empty interrupt request is generated.

When the bus interface is operating, $DQ_0 - DQ_7$ become a 3-state data bus that sends and receives data, commands, and statuses to and from the CPU. At the same time, $\overline{W}$, $\overline{R}$, $\overline{S}$, and A0 become host CPU control signal input pins.

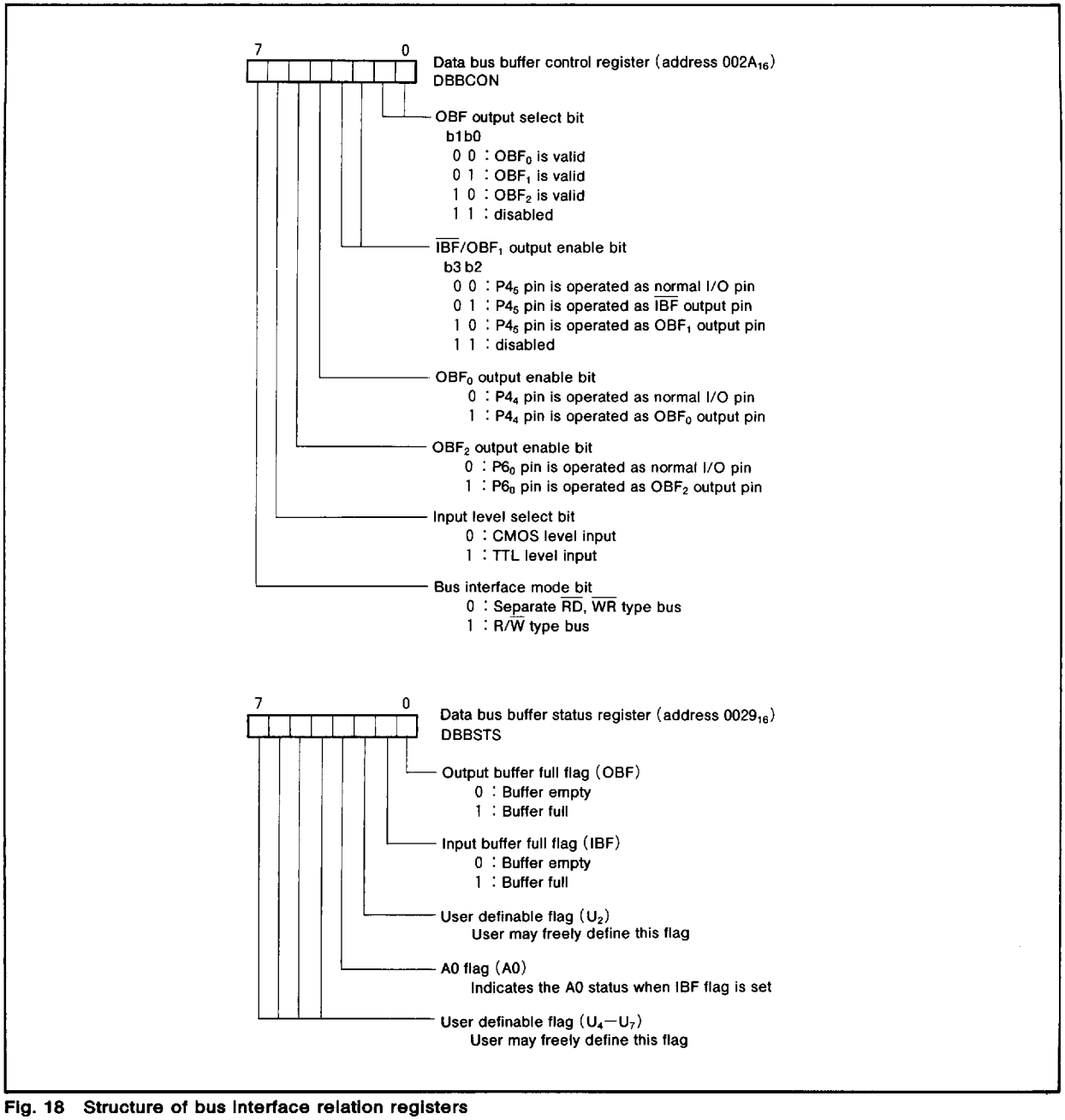


Fig. 18 Structure of bus interface relation registers

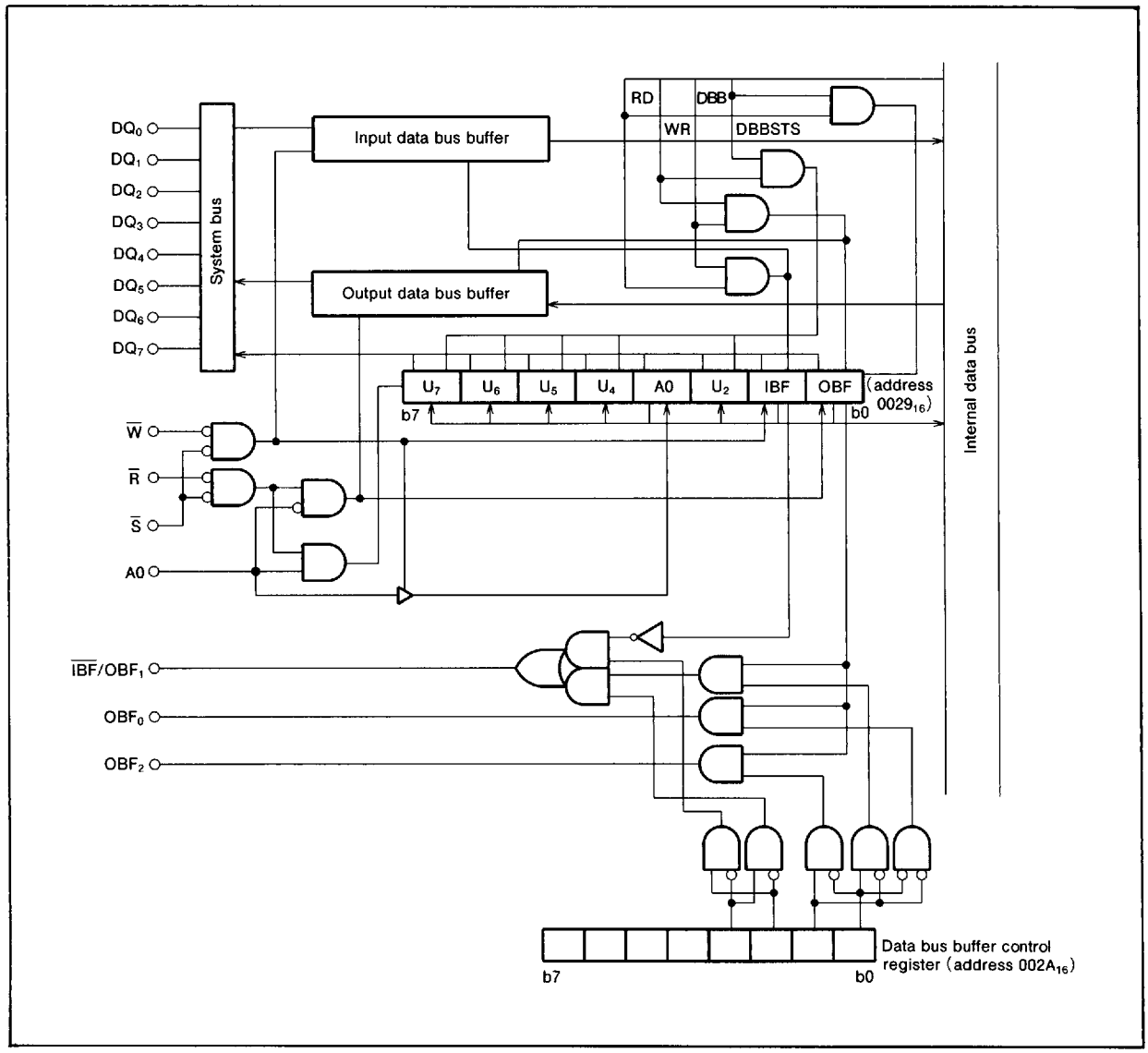


Fig. 19 Bus interface circuit diagram

Data Bus Buffer Status Register (DBBSTS) 0029_{16}

The data bus buffer status register is an 8-bit register that indicates the data bus status, with bits 0, 1, and 3 being dedicated read-only bits. Bits 2, 4, 5, 6,and 7 are programmable and can be set to act as read-only user definable flags. These bits can only be read when A0 pin is set to "H" by the host CPU.

Output buffer full flag (OBF)

The OBF flag is set to "1" when data is written to the output data bus buffer, and is cleared to "0" when data is read by the host CPU.

Input buffer full flag (IBF)

The IBF flag is set to "1" when data is written to the input data bus buffer by the host CPU, and is cleared to "0" when data is read by the slave CPU.

A0 flag

The level of the A0 pin is latched when data has been written from the host CPU to the input data bus buffer.

Input Data Bus Buffer Register (DBBIN)

Data on the data bus is latched into DBBIN by a write request from the host CPU. The data in DBBIN can be read from the data bus buffer register (address 0028_{16}) on the SFR.

Output Data Bus Buffer Register (DBBOUT)

Data is set in DBBOUT by writing to the data bus buffer register (address 0028_{16}) on the SFR. The data in DBBOUT is output to the data bus by a read request that sets the A0 pin to "L".

Table 3 Control I/O pin functions when bus interface function is selected

Pin	Name	Bus interface mode bit	OBF output select bit	$\overline{IBF}/OBF_1$ output enable bit	OBF_0 output select bit	OBF_2 output select bit	Input / Output	Function
A0	A0	—	——	——	—	—	Input	Address input. Used to select between DBBSTS and DBBOUT during host CPU read. Also used to identify commands and data during write.
$\overline{S}$	$\overline{S}$	—	——	——	—	—	Input	Chip select input. Used to select the data bus buffer. Select when "L".
$E/\overline{R}$	$\overline{R}$	0	——	——	—	—	Input	Timing signal used by the host CPU to read data from the data bus buffer.
	E	1	——	——	—	—	Input	Input a timing signal E or inverse of ϕ.
$R/\overline{W}/\overline{W}$	$\overline{W}$	0	——	——	—	—	Input	Timing signal used by the host CPU to read data from the data bus buffer.
	$R/\overline{W}$	1	——	——	—	—	Input	Input $R/\overline{W}$ signal used to control the data transfer direction. When this signal is "L", data bus buffer write is synchronized with the E signal. When it is "H", data bus buffer read is synchronized with the E signal.
$P4_4/OBF_0$	OBF_0	—	00	——	1	—	Output	Status output signal. OBF_0 signal is output.
$P4_5/\overline{IBF}/OBF_1$	$\overline{IBF}$	—	——	01	—	—	Output	Status output signal. $\overline{IBF}$ signal is output.
	OBF_1	—	01	10	—	—	Output	Status output signal. OBF_1 signal is output.
$P6_0/INT_5/OBF_2$	OBF_2	—	10	——	—	1	Output	Status output signal. OBF_2 signal is output.

RESET CIRCUIT

A microcomputer in the M3880x group is reset if the $\overline{\text{RESET}}$ pin is held at "L" level for at least 2μs then is returned to "H" level (the power supply voltage should be between 4.0V and 5.5V). After the reset is completed, the program starts from the address contained in address $FFFD_{16}$ (upper byte) and address $FFFC_{16}$ (lower byte).

Make sure that the reset input voltage is no more than 0.8V for a power supply voltage of 4.0V.

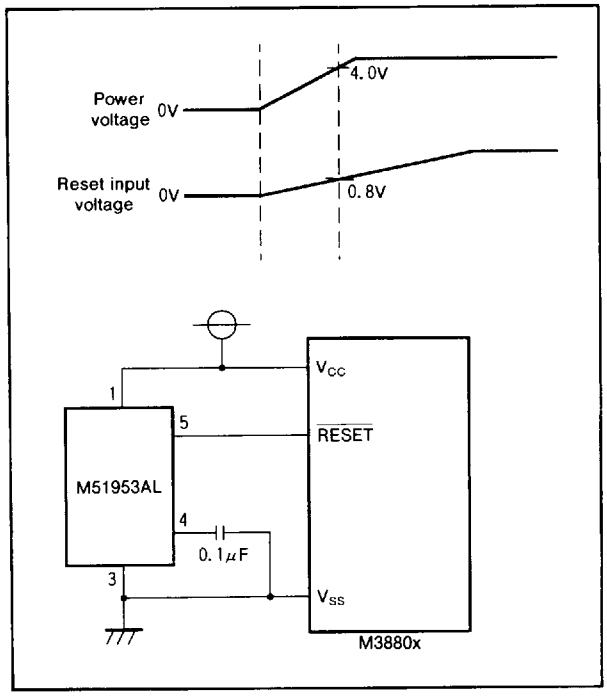


Fig. 20 Example of reset circuit

		Address	Register contents
(1)	Port P0 direction register	$(0\,0\,0\,1_{16})\cdots$	00_{16}
(2)	Port P1 direction register	$(0\,0\,0\,3_{16})\cdots$	00_{16}
(3)	Port P2 direction register	$(0\,0\,0\,5_{16})\cdots$	00_{16}
(4)	Port P3 direction register	$(0\,0\,0\,7_{16})\cdots$	00_{16}
(5)	Port P4 direction register	$(0\,0\,0\,9_{16})\cdots$	00_{16}
(6)	Port P5 direction register	$(0\,0\,0\,B_{16})\cdots$	00_{16}
(7)	Port P6 direction register	$(0\,0\,0\,D_{16})\cdots$	00_{16}
(8)	Port P3 pull-up control register	$(0\,0\,1\,3_{16})\cdots$	00_{16}
(9)	Port P4 control register	$(0\,0\,1\,5_{16})\cdots$	00_{16}
(10)	Serial I/O status register	$(0\,0\,1\,9_{16})\cdots$	1 0 0 0 0 0 0 0
(11)	Serial I/O control register	$(0\,0\,1\,A_{16})\cdots$	00_{16}
(12)	UART control register	$(0\,0\,1\,B_{16})\cdots$	1 1 1 0 0 0 0 0
(13)	Prescaler 12	$(0\,0\,2\,0_{16})\cdots$	FF_{16}
(14)	Timer 1	$(0\,0\,2\,1_{16})\cdots$	01_{16}
(15)	Timer 2	$(0\,0\,2\,2_{16})\cdots$	FF_{16}
(16)	Timer X mode register	$(0\,0\,2\,3_{16})\cdots$	00_{16}
(17)	Prescaler X	$(0\,0\,2\,4_{16})\cdots$	FF_{16}
(18)	Timer X	$(0\,0\,2\,5_{16})\cdots$	FF_{16}
(19)	Data bus buffer control register	$(0\,0\,2\,A_{16})\cdots$	00_{16}
(20)	Data bus buffer status register	$(0\,0\,2\,9_{16})\cdots$	00_{16}
(21)	Comparator control register	$(0\,0\,3\,0_{16})\cdots$	00_{16}
(22)	Interrupt edge selection register	$(0\,0\,3\,A_{16})\cdots$	00_{16}
(23)	CPU mode register	$(0\,0\,3\,B_{16})\cdots$	00_{16}
(24)	Interrupt control register 1	$(0\,0\,3\,E_{16})\cdots$	00_{16}
(25)	Interrupt control register 2	$(0\,0\,3\,F_{16})\cdots$	00_{16}
(26)	Processor status register	$(P\,S)\cdots$	X X X X X 1 X X
(27)	Program counter	$(P\,C_H)\cdots$	Contents of address $FFFD_{16}$
		$(P\,C_L)\cdots$	Contents of address $FFFC_{16}$

Note : X : Undefined
The contents of all other registers and RAM are undefined after a reset, so they must be initialized by software.

Fig. 21 Internal status of microcomputer after reset

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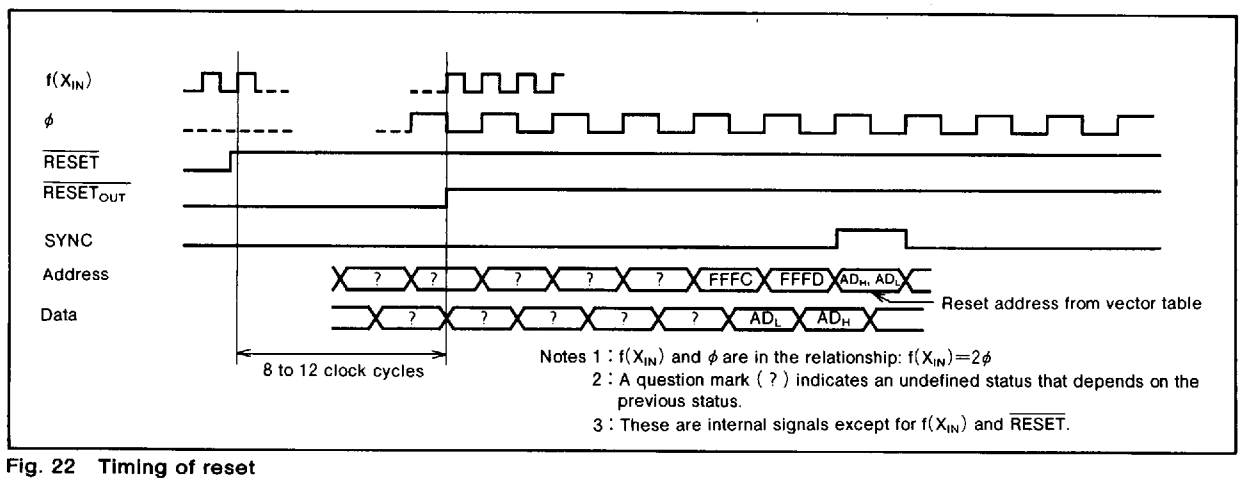

Fig. 22 Timing of reset

CLOCK GENERATION CIRCUIT

An oscillation circuit can be created by connecting a resonator between X_{IN} and X_{OUT}. When using an external clock signal, input the clock signal to the X_{IN} pin and leave the X_{OUT} pin open.

Oscillation Control

Stop mode

If the STP instruction is executed, oscillation stops with the internal clock ϕ at "H". Timer 1 is set to "01_{16}" and prescaler 12 is set to "FF_{16}".

Oscillation restarts when an external interrupt is received, but the internal clock ϕ remains at "H" until timer 1 overflows.

This allows time for the clock circuit oscillation to stabilize. If oscillation is restarted by a reset, no wait time is generated, so keep the $\overline{RESET}$ pin at "L" level until oscillation has stabilized.

Wait mode

If the WIT instruction is executed, the internal clock ϕ stops at "H" level, but the oscillator itself does not stop. The internal clock restarts if a reset occurs or when an interrupt is received.

Since the oscillator does not stop, normal operation can be started immediately after the clock is restarted.

To ensure that interrupts will be received to release the STP or WIT state, interrupt enable bits must be set to "1" before the STP or WIT instruction is executed.

When the STP status is released, prescaler 12 and timer 1 will start counting and reset will not be released until timer 1 overflows, so set the timer 1 interrupt enable bit to "0" before the STP instruction is executed.

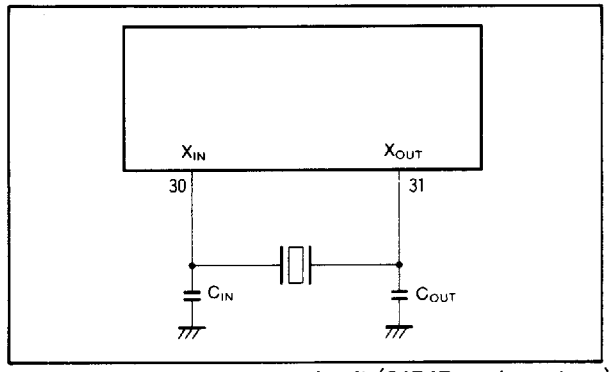

Fig. 23 Ceramic resonator circuit (64P4B package type)

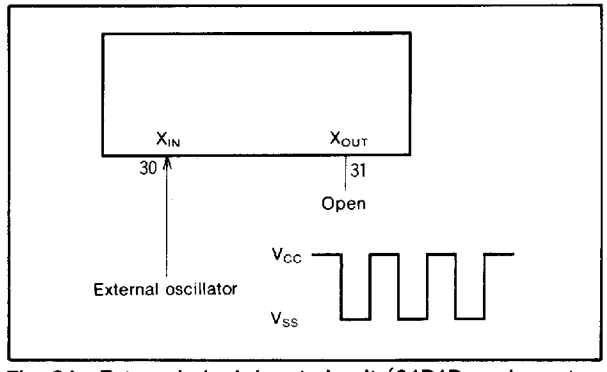

Fig. 24 External clock input circuit (64P4B package type)

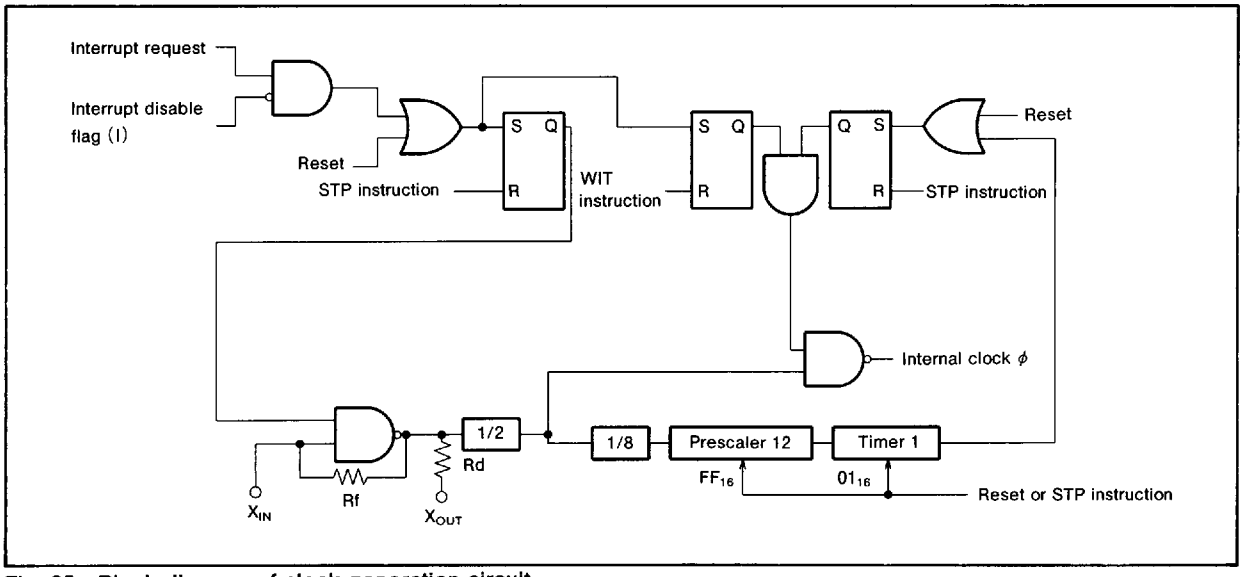

Fig. 25 Block diagram of clock generation circuit

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NOTES ON PROGRAMMING

Processor Status Register

The contents of the processor status register (PS) after a reset are undefined, except for the interrupt disable flag (I) which is "1". Therefore, flags that affect program execution must be initialized after a reset.
In particular, it is essential to initialize the T and D flags because of their effect on calculations.

Interrupts

The contents of the interrupt request bits do not change immediately after they have been written. After writing to an interrupt request bit, execute at least one instruction before executing the BBC or BBS instruction.

Decimal Calculations

To calculate in decimal notation, set the decimal mode flag (D) to "1", then execute the ADC or SBC instruction. Only the ADC and SBC instructions yield proper decimal results. After executing the ADC or SBC instruction, execute at least one instruction before executing the SEC, CLC, or CLD instruction.

In decimal mode, the values of the negative (N), overflow (V), and zero (Z) flags are invalid.
The carry flag can be used to indicate whether a carry or borrow has occurred, but must be initialized before each calculation. Clear the carry flag before the ADC instruction and set the flag before the SBC instruction.

Timers

If a value n (between 0 and 255) is written to a timer latch, the frequency division ratio is 1/(n+1).

Multiplication and Division Instructions

The MUL and DIV instructions do not affect the T and D flags.
The execution of these instructions does not change the contents of the processor status register.

Ports

The contents of the port direction registers cannot be read. Programs can not use the value of a direction register as an index, or bit-test a direction register (BBC or BBS instruction), or perform a read-modify-write instruction such as the ROR, CLB, or SEB instruction. Use instructions such as the LDM and STA instructions to set the port direction registers.

Serial I/O

In clock synchronous serial I/O, if the receive side is using an external clock and it is to output the $\overline{S_{RDY}}$ signal, set the transmit enable bit, the receive enable bit, and the $\overline{S_{RDY}}$ output enable bit to "1".
Serial I/O continues to output the final bit from the T_XD pin after transmission is completed.

Instruction Execution Time

The instruction execution time is obtained by multiplying the frequency of the internal clock ϕ by the number of cycles needed to execute an instruction.
The number of cycles required to execute an instruction is shown in the list of machine instructions.
The frequency of the internal clock ϕ is half of the X_{IN} frequency.

DATA REQUIRED FOR MASK ORDERS

The following materials are necessary when ordering a mask ROM production:

1. Mask ROM Order Confirmation Form
2. Mark Specification Form
3. Data to be written to ROM, in EPROM form (three identical copies)

ROM Writing Method

The built-in PROM of the blank one-time programmable version and built-in EPROM version can be read from and written to with an normal PROM writer using a special write adapter. Set the address of PROM writer to user ROM area.

Package	Name of Write Adapter
64P4B, 64S1B	PCA4738S-64
64P6N	PCA4738F-64
64D0	PCA4738L-64
64P6D	PCA4738H-64

The PROM of the blank one-time programmable version is not tested or screened after assembly. To ensure proper operation after writing, the procedure shown in Figure 26 is recommended to verify programming.

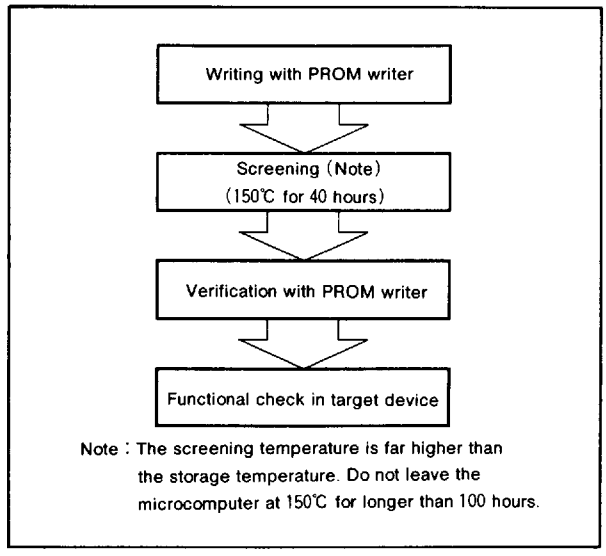

Fig. 26 Writing and testing of one-time programmable version

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	All voltages measured with reference to the V_{SS} pin, output transistors isolated.	−0.3 to 7.0	V
V_I	Input voltage $P0_0$−$P0_7$, $P1_0$−$P1_7$, $P2_0$−$P2_7$, $P3_0$−$P3_7$, $P4_0$−$P4_7$, $P5_0$−$P5_3$, $P6_0$, $P6_1$, DQ_0−DQ_7, $\overline{W}$, $\overline{R}$, $\overline{S}$, A0		−0.3 to V_{CC}+0.3	V
V_I	Input voltage $\overline{RESET}$, X_{IN}		−0.3 to V_{CC}+0.3	V
V_I	Input voltage CNV_{SS}		−0.3 to 13	V
V_O	Output voltage $P0_0$−$P0_7$, $P1_0$−$P1_7$, $P2_0$−$P2_7$, $P3_0$−$P3_7$, $P4_0$−$P4_7$, $P5_0$−$P5_3$, $P6_0$, $P6_1$, X_{OUT}, DQ_0−DQ_7		−0.3 to V_{CC}+0.3	V
P_d	Power dissipation	T_a = 25℃	1000(Note)	mW
T_{opr}	Operating temperature		−20 to 85	℃
Tstg	Storage temperature		−40 to 125	℃

Note : 300mW in case of the flat package.

RECOMMENDED OPERATING CONDITIONS (V_{CC} = 2.7 to 5.5V, T_a = −20 to 85℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V_{CC}	Supply voltage (when operating at 8MHz)	4.0	5.0	5.5	V
	Supply voltage (when operating at 4MHz)	2.7	5.0	5.5	
V_{SS}	Supply voltage		0		V
V_{IH}	"H" input voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P5_0$–$P5_3$, $P6_0$, $P6_1$	0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage (when selecting CMOS input level) $P4_0$–$P4_7$, DQ_0–DQ_7, $\overline{W}$, $\overline{R}$, $\overline{S}$, A0	0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage (when selecting TTL input level) $P4_0$–$P4_7$, DQ_0–DQ_7, $\overline{W}$, $\overline{R}$, $\overline{S}$, A0 (Note 1)	2.0		V_{CC}	V
V_{IH}	"H" input voltage $\overline{RESET}$, X_{IN}, CNV_{SS}	0.8V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P5_0$–$P5_3$, $P6_0$, $P6_1$	0		0.2V_{CC}	V
V_{IL}	"L" input voltage (when selecting CMOS input level) $P4_0$–$P4_7$, DQ_0–DQ_7, $\overline{W}$, $\overline{R}$, $\overline{S}$, A0	0		0.2V_{CC}	V
V_{IL}	"L" input voltage (when selecting TTL input level) $P4_0$–$P4_7$, DQ_0–DQ_7, $\overline{W}$, $\overline{R}$, $\overline{S}$, A0 (Note 1)	0		0.8	V
V_{IL}	"L" input voltage $\overline{RESET}$, CNV_{SS}	0		0.2V_{CC}	V
V_{IL}	"L" input voltage X_{IN}	0		0.16V_{CC}	V
$\Sigma I_{OH(peak)}$	"H" total peak output current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$ (Note 2)			−80	mA
$\Sigma I_{OH(peak)}$	"H" total peak output current $P4_0$–$P4_7$, $P5_0$–$P5_3$, $P6_0$, $P6_1$, DQ_0–DQ_7 (Note 2)			−80	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_3$, $P3_0$–$P3_7$ (Note 2)			80	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current $P2_4$–$P2_7$ (Note 2)			80	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current $P4_0$–$P4_7$, $P5_0$–$P5_3$, $P6_0$, $P6_1$, DQ_0–DQ_7 (Note 2)			80	mA
$\Sigma I_{OH(avg)}$	"H" total average output current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$ (Note 2)			−40	mA
$\Sigma I_{OH(avg)}$	"H" total average output current $P4_0$–$P4_7$, $P5_0$–$P5_3$, $P6_0$, $P6_1$, DQ_0–DQ_7 (Note 2)			−40	mA
$\Sigma I_{OL(avg)}$	"L" total average output current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_3$, $P3_0$–$P3_7$ (Note 2)			40	mA
$\Sigma I_{OL(avg)}$	"L" total average output current $P2_4$–$P2_7$ (Note 2)			40	mA
$\Sigma I_{OL(avg)}$	"L" total average output current $P4_0$–$P4_7$, $P5_0$–$P5_3$, $P6_0$, $P6_1$, DQ_0–DQ_7 (Note 2)			40	mA
$I_{OH(peak)}$	"H" peak output current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_3$, $P6_0$, $P6_1$, DQ_0–DQ_7 (Note 3)			−10	mA
$I_{OL(peak)}$	"L" peak output current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_3$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_3$, $P6_0$, $P6_1$, DQ_0–DQ_7 (Note 3)			10	mA
$I_{OL(peak)}$	"L" peak output current $P2_4$–$P2_7$ (Note 3)			20	mA
$I_{OH(avg)}$	"H" average output current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_3$, $P6_0$, $P6_1$, DQ_0–DQ_7 (Note 4)			−5	mA
$I_{OL(avg)}$	"L" average output current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_3$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_3$, $P6_0$, $P6_1$, DQ_0–DQ_7 (Note 4)			5	mA
$I_{OL(avg)}$	"L" average output current $P2_4$–$P2_7$ (Note 4)			15	mA
$f(X_{IN})$	Internal clock oscillation frequency (V_{CC}=4.0 to 5.5V) (Note 5)			8	MHz
	Internal clock oscillation frequency (V_{CC}=2.7 to 5.5V) (Note 5)			4	

Notes 1 : It is the case V_{CC} is 4.0 to 5.5V, and input levels of INT_0-INT_2 functions are excepted.
2 : The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100ms. The total peak current is the peak value of all the currents.
3 : The peak output current is the peak current flowing in each port.
4 : The average output current I_{OL} (avg), I_{OH} (avg) is an average value measured over 100ms.
5 : When the oscillation frequency has a duty cycle of 50%.

ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7 to 5.5V, V_{SS} = 0V, T_a = −20 to 85℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	"H" output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_3$, $P6_0$, $P6_1$, DQ_0–DQ_7 (Note 1)	I_{OH}=−10mA, V_{CC}=4.0 to 5.5V	V_{CC}−2.0			V
		I_{OH}=−1.0mA, V_{CC}=2.7 to 5.5V	V_{CC}−1.0			
V_{OL}	"L" output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_3$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_3$, $P6_0$, $P6_1$, DQ_0–DQ_7	I_{OL}=10mA, V_{CC}=4.0 to 5.5V			2.0	V
		I_{OL}=1.0mA, V_{CC}=2.7 to 5.5V			1.0	
V_{OL}	"L" output voltage $P2_4$–$P2_7$	I_{OL}=20mA, V_{CC}=4.0 to 5.5V			2.0	V
		I_{OL}=10mA, V_{CC}=2.7 to 5.5V			1.0	
V_{T+}−V_{T-}	Hysteresis $CNTR_0$, INT_0–INT_5, $P3_0$–$P3_7$			0.4		V
V_{T+}−V_{T-}	Hysteresis R_XD, S_{CLK}			0.5		V
V_{T+}−V_{T-}	Hysteresis $\overline{RESET}$			0.5		V
I_{IH}	"H" input current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_3$, $P6_0$, $P6_1$, DQ_0–DQ_7, $\overline{W}$, $\overline{R}$, $\overline{S}$, A0	V_I=V_{CC}			5.0	μA
I_{IH}	"H" input current $\overline{RESET}$, CNV_{SS}	V_I=V_{CC}			5.0	μA
I_{IH}	"H" input current X_{IN}	V_I=V_{CC}		4		μA
I_{IL}	"L" input current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$ (No pull-up), $P4_0$–$P4_7$, $P5_0$–$P5_3$, $P6_0$, $P6_1$, DQ_0–DQ_7, $\overline{W}$, $\overline{R}$, $\overline{S}$, A0	V_I=V_{SS}			−5.0	μA
I_{IL}	"L" input current $P3_0$–$P3_7$ (at pull-up)	V_I=V_{SS}, V_{CC}=4.0 to 5.5V	−20	−60	−120	μA
		I_I=V_{SS}, V_{CC}=2.7 to 5.5V	−10			μA
I_{IL}	"L" input current $\overline{RESET}$, CNV_{SS}	V_I=V_{SS}			−5.0	μA
I_{IL}	"L" input current X_{IN}	V_I=V_{SS}		−4		μA
V_{RAM}	RAM hold voltage	With clock stopped	2.0		5.5	V
I_{CC}	Supply current	f(X_{IN})=8MHz, V_{CC}=5V		6.4	13.0	mA
		f(X_{IN})=4MHz, V_{CC}=2.7V		1.6	3.2	
		When WIT instruction is executed with f(X_{IN})=8MHz		1.5		
		When STP instruction is executed with clock stopped, output transistors isolated. T_a=25℃ (Note2)		0.1	1	μA
		When STP instruction is executed with clock stopped, output transistors isolated. T_a=85℃ (Note2)			10	

Notes 1 : $P5_1$ is measured when the $P5_1/T_XD$ P-channel output disable bit of the UART control register (bit 4 of address $001B_{16}$) is "0".
2 : It is the value with output transistors isolated and comparator having completed comparison, and analog input mode.

COMPARATOR CHARACTERISTICS (V_{CC}=2.7 to 5.5V, V_{SS}=0V, T_a=−20 to 85℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				4	Bits
—	Absolute accuracy				1/2	LSB
T_{CONV}	Conversion time	Operating at 8MHz			3.5	μs
		Operating at 4MHz			7	
V_{IA}	Analog input voltage		0		V_{CC}	V
I_{IA}	Analog port input current				5.0	μA
R_{LADDER}	Ladder resistor		30	40	50	kΩ

TIMING REQUIREMENTS 1 (V_{CC}=4.0 to 5.5V, V_{SS}=0V, T_a=−20 to 85℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{W(\overline{RESET})}$	Reset input "L" pulse width	2			μs
$t_{C(X_{IN})}$	External clock input cycle time	125			ns
$t_{WH(X_{IN})}$	External clock input "H" pulse width	50			ns
$t_{WL(X_{IN})}$	External clock input "L" pulse width	50			ns
$t_{C(CNTR)}$	$CNTR_0$ input cycle time	200			ns
$t_{WH(CNTR)}$	$CNTR_0$, INT_0–INT_5 input "H" pulse width	80			ns
$t_{WL(CNTR)}$	$CNTR_0$, INT_0–INT_5 input "L" pulse width	80			ns
$t_{C(S_{CLK})}$	Serial I/O clock input cycle time (Note)	800			ns
$t_{WH(S_{CLK})}$	Serial I/O clock input "H" pulse width (Note)	370			ns
$t_{WL(S_{CLK})}$	Serial I/O clock input "L" pulse width (Note)	370			ns
$t_{SU(R_XD-S_{CLK})}$	Serial I/O input set up time	220			ns
$t_{h(S_{CLK}-R_XD)}$	Serial I/O input hold time	100			ns

Note : When $f(X_{IN})$=8MHz and bit 6 of address $001A_{16}$ is "1" (clock synchronous mode). Divide this value by four when $f(X_{IN})$=8MHz and bit 6 of address $001A_{16}$ is "0" (UART mode).

TIMING REQUIREMENTS 2 (V_{CC}=2.7 to 5.5V, V_{SS}=0V, T_a=−20 to 85℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{W(\overline{RESET})}$	Reset input "L" pulse width	2			μs
$t_{C(X_{IN})}$	External clock input cycle time	250			ns
$t_{WH(X_{IN})}$	External clock input "H" pulse width	100			ns
$t_{WL(X_{IN})}$	External clock input "L" pulse width	100			ns
$t_{C(CNTR)}$	$CNTR_0$ input cycle time	500			ns
$t_{WH(CNTR)}$	$CNTR_0$, INT_0–INT_5 input "H" pulse width	230			ns
$t_{WL(CNTR)}$	$CNTR_0$, INT_0–INT_5 input "L" pulse width	230			ns
$t_{C(S_{CLK})}$	Serial I/O clock input cycle time (Note)	2000			ns
$t_{WH(S_{CLK})}$	Serial I/O clock input "H" pulse width (Note)	950			ns
$t_{WL(S_{CLK})}$	Serial I/O clock input "L" pulse width (Note)	950			ns
$t_{SU(R_XD-S_{CLK})}$	Serial I/O input set up time	400			ns
$t_{h(S_{CLK}-R_XD)}$	Serial I/O input hold time	200			ns

Note : When $f(X_{IN})$=8MHz and bit 6 of address $001A_{16}$ is "1" (clock synchronous mode). Divide this value by four when $f(X_{IN})$=8MHz and bit 6 of address $001A_{16}$ is "0" (UART mode).

Master CPU bus interface timing ($\overline{R}$ and $\overline{W}$ separation type mode)

(DBBM= 0) (V_{CC}=4.0 to 5.5V, V_{SS}=0V, T_a=−20 to 85℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{su(S-R)}$	$\overline{S}$ set up time	0			ns
$t_{su(S-W)}$	$\overline{S}$ set up time	0			ns
$t_{h(R-S)}$	$\overline{S}$ hold time	0			ns
$t_{h(W-S)}$	$\overline{S}$ hold time	0			ns
$t_{su(A-R)}$	A0 set up time	10			ns
$t_{su(A-W)}$	A0 set up time	10			ns
$t_{h(R-A)}$	A0 hold time	0			ns
$t_{h(W-A)}$	A0 hold time	0			ns
$t_{W(R)}$	Read pulse width	120			ns
$t_{W(W)}$	Write pulse width	120			ns
$t_{su(D-W)}$	Date input set up time before write	50			ns
$t_{h(W-D)}$	Date input hold time after write	0			ns

Master CPU bus interface timing ($\overline{R}$ and $\overline{W}$ separation type mode)

(DBBM= 0) (V_{CC}=2.7 to 5.5V, V_{SS}=0V, T_a=−20 to 85℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{su(S-R)}$	$\overline{S}$ set up time	0			ns
$t_{su(S-W)}$	$\overline{S}$ set up time	0			ns
$t_{h(R-S)}$	$\overline{S}$ hold time	0			ns
$t_{h(W-S)}$	$\overline{S}$ hold time	0			ns
$t_{su(A-R)}$	A0 set up time	30			ns
$t_{su(A-W)}$	A0 set up time	30			ns
$t_{h(R-A)}$	A0 hold time	0			ns
$t_{h(W-A)}$	A0 hold time	0			ns
$t_{W(R)}$	Read pulse width	250			ns
$t_{W(W)}$	Write pulse width	250			ns
$t_{su(D-W)}$	Date input set up time before write	130			ns
$t_{h(W-D)}$	Date input hold time after write	0			ns

Master CPU bus interface timing (R/$\overline{W}$ type mode)

(DBBM= 1) (V_{CC}=4.0 to 5.5V, V_{SS}=0V, T_a=−20 to 85℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{su(S-E)}$	$\overline{S}$ set up time	0			ns
$t_{h(E-S)}$	$\overline{S}$ hold time	0			ns
$t_{su(A-E)}$	A0 set up time	10			ns
$t_{h(E-A)}$	A0 hold time	0			ns
$t_{su(RW-E)}$	R/$\overline{W}$ set up time	10			ns
$t_{h(E-RW)}$	R/$\overline{W}$ hold time	10			ns
$t_{w(EL)}$	Enable clock "L" pulse width	120			ns
$t_{w(EH)}$	Enable clock "H" pulse width	120			ns
$t_{r(E)}$	Enable clock rising time			25	ns
$t_{f(E)}$	Enable clock falling time			25	ns
$t_{su(D-E)}$	Data input set up time before write	50			ns
$t_{h(E-D)}$	Data input hold time after write	0			ns

Master CPU bus interface timing (R/$\overline{W}$ type mode)

(DBBM= 1) (V_{CC}=2.7 to 5.5V, V_{SS}=0V, T_a=−20 to 85℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{su(S-E)}$	$\overline{S}$ set up time	0			ns
$t_{h(E-S)}$	$\overline{S}$ hold time	0			ns
$t_{su(A-E)}$	A0 set up time	30			ns
$t_{h(E-A)}$	A0 hold time	0			ns
$t_{su(RW-E)}$	R/$\overline{W}$ set up time	20			ns
$t_{h(E-RW)}$	R/$\overline{W}$ hold time	20			ns
$t_{w(EL)}$	Enable clock "L" pulse width	250			ns
$t_{w(EH)}$	Enable clock "H" pulse width	250			ns
$t_{r(E)}$	Enable clock rising time			40	ns
$t_{f(E)}$	Enable clock falling time			40	ns
$t_{su(D-E)}$	Data input set up time before write	130			ns
$t_{h(E-D)}$	Data input hold time after write	0			ns

SWITCHING CHARACTERISTICS 1 (V_{CC} = 4.0 to 5.5V, V_{SS} = 0V, T_a = −20 to 85°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{WH(S_{CLK})}$	Serial I/O clock output "H" pulse width	$t_{C(S_{CLK})}/2-30$			ns
$t_{WL(S_{CLK})}$	Serial I/O clock output "L" pulse width	$t_{C(S_{CLK})}/2-30$			ns
$t_{d(S_{CLK}-T_XD)}$	Serial I/O output delay time (Note 1)			140	ns
$t_{v(S_{CLK}-T_XD)}$	Serial I/O output valid time (Note 1)	−30			ns
$t_{r(S_{CLK})}$	Serial I/O clock output rising time			30	ns
$t_{f(S_{CLK})}$	Serial I/O clock output falling time			30	ns
$t_{r(CMOS)}$	CMOS output rising time (Note 2)		10	30	ns
$t_{f(CMOS)}$	CMOS output falling time (Note 2)		10	30	ns

Notes 1 : When the $P5_1/T_XD$ P-channel output disable bit of the UART control register (bit 4 of address $001B_{16}$) is "0".
2 : X_{OUT} pin excluded.

SWITCHING CHARACTERISTICS 2 (V_{CC} = 2.7 to 5.5V, V_{SS} = 0V, T_a = −20 to 85°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{WH(S_{CLK})}$	Serial I/O clock output "H" pulse width	$t_{C(S_{CLK})}/2-50$			ns
$t_{WL(S_{CLK})}$	Serial I/O clock output "L" pulse width	$t_{C(S_{CLK})}/2-50$			ns
$t_{d(S_{CLK}-T_XD)}$	Serial I/O output delay time (Note 1)			350	ns
$t_{v(S_{CLK}-T_XD)}$	Serial I/O output valid time (Note 1)	−30			ns
$t_{r(S_{CLK})}$	Serial I/O clock output rising time			50	ns
$t_{f(S_{CLK})}$	Serial I/O clock output falling time			50	ns
$t_{r(CMOS)}$	CMOS output rising time (Note 2)		20	50	ns
$t_{f(CMOS)}$	CMOS output falling time (Note 2)		20	50	ns

Notes 1 : When the $P5_1/T_XD$ P-channel output disable bit of the UART control register (bit 4 of address $001B_{16}$) is "0".
2 : X_{OUT} pin excluded.

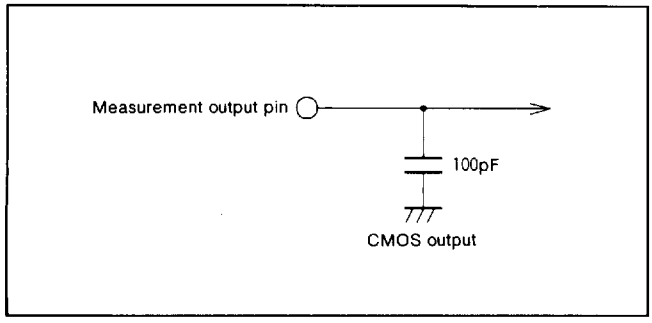


Fig. 27 Circuit for measuring output switching characteristics (1)

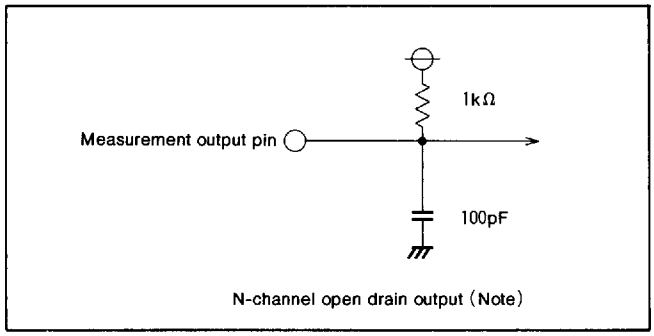


Fig. 28 Circuit for measuring output switching characteristics (2)

Note : When the bit 4 of UART control register (address $001B_{16}$) is "1".
(N-channel open-drain output mode)

Master CPU bus interface ($\overline{R}$ and $\overline{W}$ separation type mode)

(DBBM=0) (V_{CC}=4.0 to 5.5V, V_{SS}=0V, T_a=−20 to 85℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{a(R-D)}$	Data output enable time after read			80	ns
$t_{v(R-D)}$	Data output disable time after read	0		30	ns
$t_{PLH(R-OBF)}$	OBF output transmission time after read			150	ns
$t_{PLH(W-\overline{IBF})}$	$\overline{IBF}$ output transmission time after write			150	ns

Master CPU bus interface ($\overline{R}$ and $\overline{W}$ separation type mode)

(DBBM=0) (V_{CC}=2.7 to 5.5V, V_{SS}=0V, T_a=−20 to 85℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{a(R-D)}$	Data output enable time after read			130	ns
$t_{v(R-D)}$	Data output disable time after read	0		85	ns
$t_{PLH(R-OBF)}$	OBF output transmission time after read			300	ns
$t_{PLH(W-\overline{IBF})}$	$\overline{IBF}$ output transmission time after write			300	ns

Master CPU bus interface (R/$\overline{W}$ type mode)

(DBBM=1) (V_{CC}=4.0 to 5.5V, V_{SS}=0V, T_a=−20 to 85℃, unless otherwise noted)

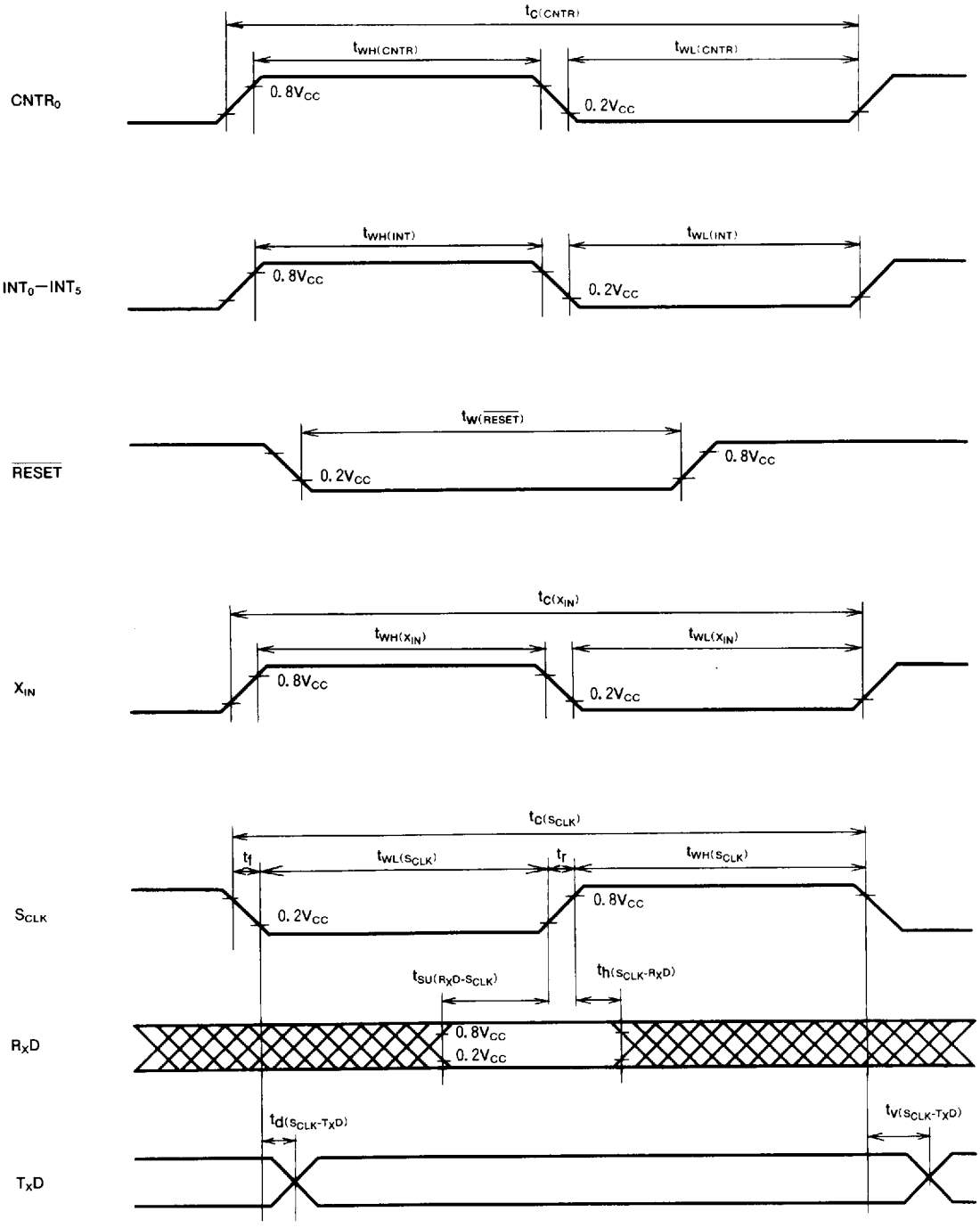
Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{a(E-D)}$	Data output enable time after read			80	ns
$t_{v(E-D)}$	Data output disable time after read	0		30	ns
$t_{PLH(E-OBF)}$	OBF output transmission time after E clock			150	ns
$t_{PLH(E-\overline{IBF})}$	$\overline{IBF}$ output transmission time after E clock			150	ns

Master CPU bus interface (R/$\overline{W}$ type mode)

(DBBM=1) (V_{CC}=2.7 to 5.5V, V_{SS}=0V, T_a=−20 to 85℃, unless otherwise noted)

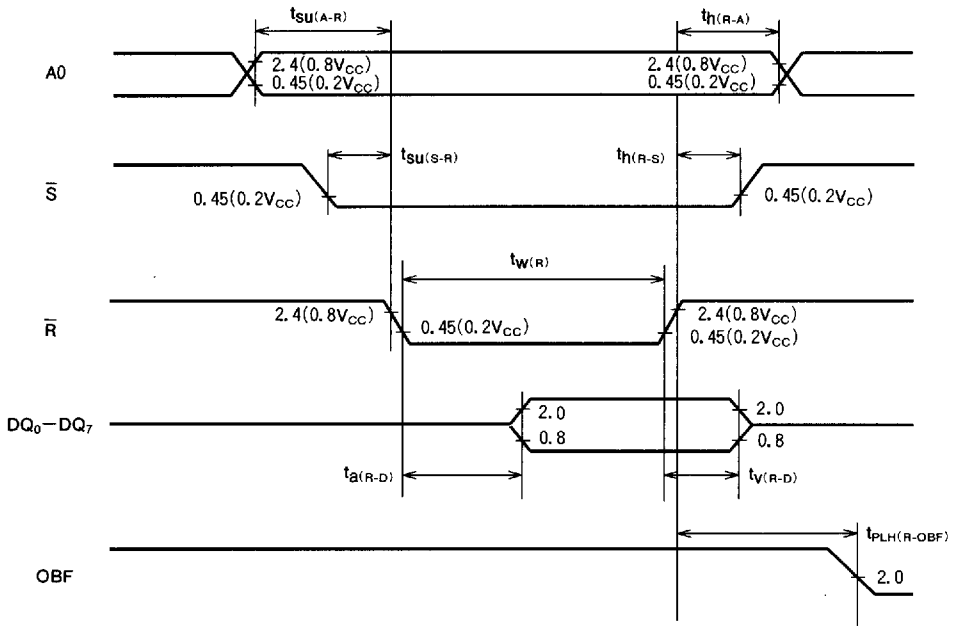
Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{a(E-D)}$	Data output enable time after read			130	ns
$t_{v(E-D)}$	Data output disable time after read	0		85	ns
$t_{PLH(E-OBF)}$	OBF output transmission time after E clock			300	ns
$t_{PLH(E-\overline{IBF})}$	$\overline{IBF}$ output transmission time after E clock			300	ns

TIMING CHART

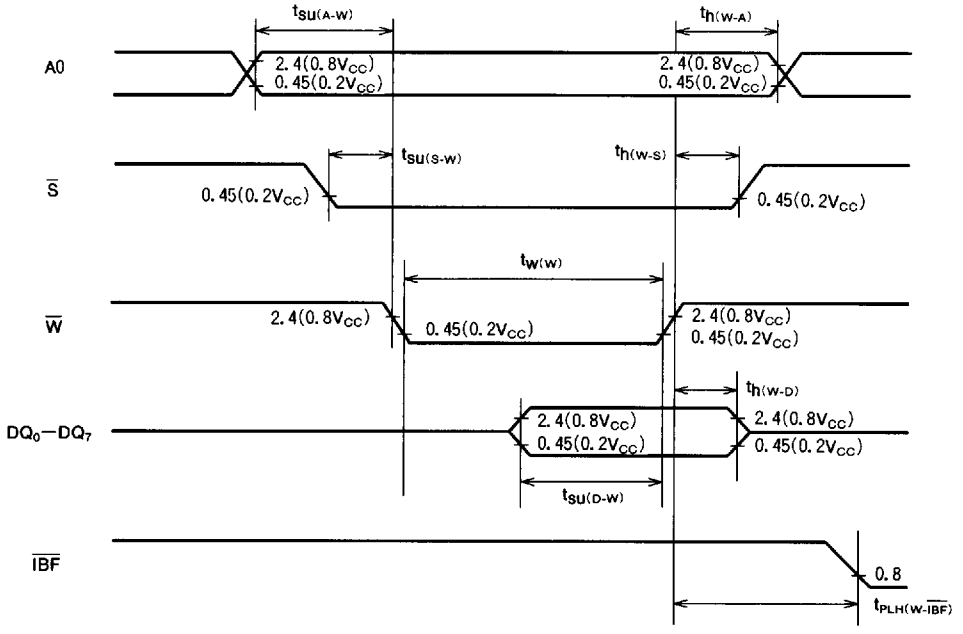


Master CPU bus interface/$\overline{RD}$ and $\overline{WR}$ separation type timing diagram

Read



Write

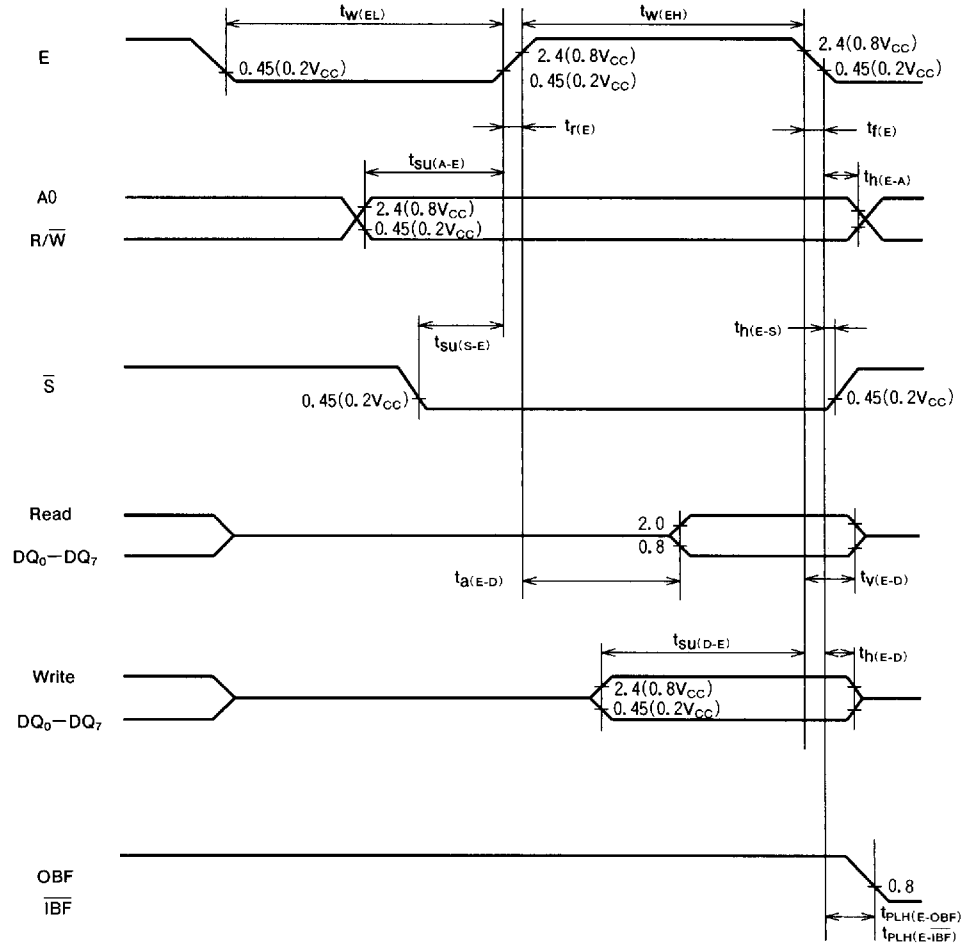


TTL input outside of ( )

CMOS input inside of ( )

MITSUBISHI ELECTRIC

Master CPU bus interface/R/$\overline{W}$ type timing diagram



TTL input outside of ( )

CMOS input inside of ( )

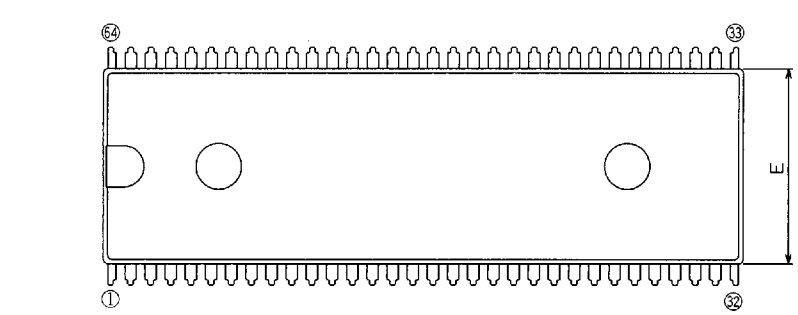
PACKAGE OUTLINE

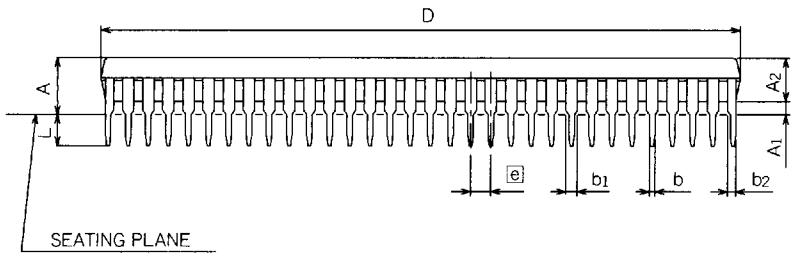
64P4B

Plastic 64pin 750mil SDIP

EIAJ Package Code	JEDEC Code	Weight(g)
SDIP064-P-0750	–	7.9

Scale : 1.5/1





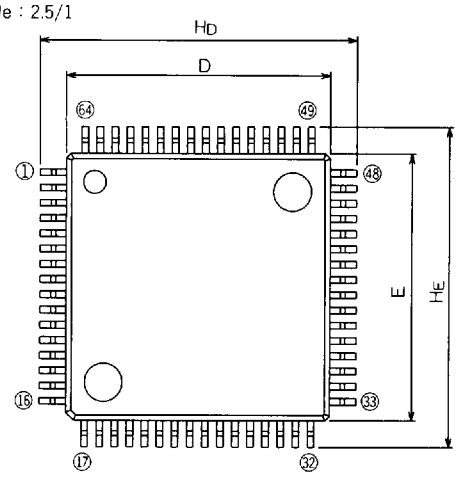
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	5.08
A_1	0.38	–	–
A_2	–	3.8	–
b	0.4	0.5	0.6
b_1	0.9	1.0	1.3
b_2	0.65	0.75	1.05
c	0.2	0.25	0.32
D	56.2	56.4	56.6
E	16.85	17.0	17.15
e	–	1.778	–
e1	–	19.05	–
L	2.8	–	–
θ	0°	–	15°

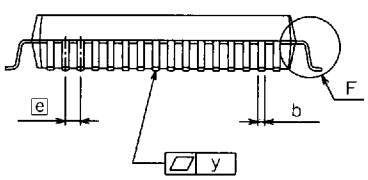
64P6N-A

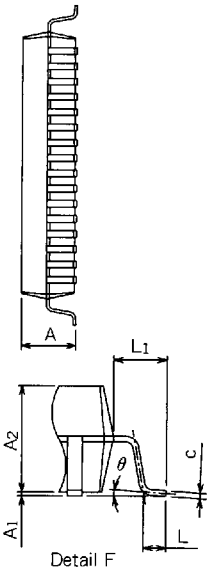
Plastic 64pin 14×14mm body QFP

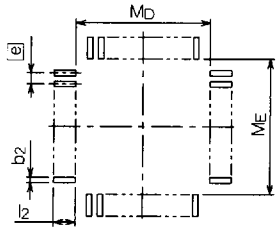
EIAJ Package Code	JEDEC Code	Weight(g)
*QFP064-P-1414	–	1.11

Scale : 2.5/1









Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	3.05
A_1	0	0.1	0.2
A_2	–	2.8	–
b	0.3	0.35	0.45
c	0.13	0.15	0.2
D	13.8	14.0	14.2
E	13.8	14.0	14.2
e	–	0.8	–
HD	16.5	16.8	17.1
HE	16.5	16.8	17.1
L	0.4	0.6	0.8
L_1	–	1.4	–
y	–	–	0.1
θ	0°	–	10°
b_2	–	0.5	–
l_2	–	1.3	–
MD	–	14.6	–
ME	–	14.6	–

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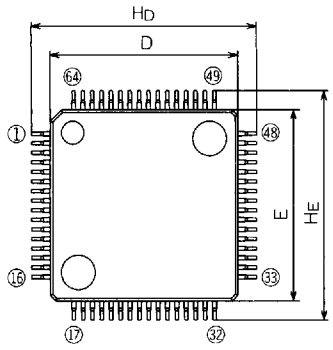
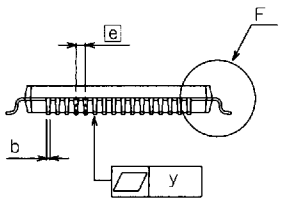
64P6D−A

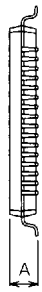
Plastic 64pin 10×10mm body QFP(FP)

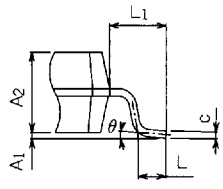
EIAJ Package Code	JEDEC Code	Weight(g)
*QFP64-P-1010	–	0.32

Scale : 2.5/1

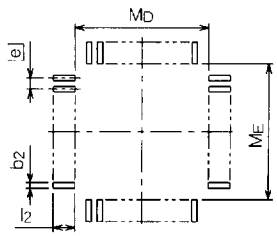








Detail F



Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.7
A_1	0	0.1	0.2
A_2	–	1.4	–
b	0.13	0.18	0.28
c	0.105	0.125	0.175
D	9.9	10.0	10.1
E	9.9	10.0	10.1
e	–	0.5	–
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
L	0.3	0.5	0.7
L_1	–	1.0	–
y	–	–	0.1
θ	0°	–	10°
b_2	–	0.225	–
l_2	–	1.0	–
M_D	–	10.4	–
M_E	–	10.4	–