MICRON
SEMICONDUCTOR, INC.

MICRON
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SRAM DATA BOOK

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ABOUT THE COVER:

Front — A variety of features highlights Micron's SRAM product line, shown here before a close-up of a 256K SRAM wafer. Pictured are a 5 volt 32K x 8 SRAM in a 300 mil plastic SOJ package, a 5-volt 64K x 16 SRAM in a 44-pin, 400 mil SOJ package and a 3.3-volt 32K x 36 SyncBurst™ SRAM in a 100-pin TQFP package.

Back — Micron's Boise, Idaho headquarters.

IMPORTANT NOTICE

Micron Semiconductor, Inc., reserves the right to change products or specifications without notice. Customers are advised to obtain the latest versions of product specifications, which should be considered in evaluating a product's appropriateness for a particular use. There is no assurance that Micron's semiconductors are appropriate for any application by a customer.

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MICRON'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF MICRON SEMICONDUCTOR, INC., AS USED HEREIN:

A. LIFE SUPPORT DEVICES OR SYSTEMS ARE DEVICES OR SYSTEMS WHICH (1) ARE INTENDED FOR SURGICAL IMPLANT INTO THE BODY, OR (2) SUPPORT OR SUSTAIN LIFE AND WHOSE FAILURE TO PERFORM WHEN PROPERLY USED IN ACCORDANCE WITH INSTRUCTIONS FOR USE PROVIDED IN THE LABELING CAN BE REASONABLY EXPECTED TO RESULT IN A SIGNIFICANT INJURY TO THE USER.

B. CRITICAL COMPONENT IS ANY COMPONENT OF A LIFE SUPPORT DEVICE OR SYSTEM WHOSE FAILURE TO PERFORM CAN BE REASONABLY EXPECTED TO CAUSE THE FAILURE OF THE LIFE SUPPORT DEVICE OR SYSTEM OR TO AFFECT ITS SAFETY OR EFFECTIVENESS.

Dear Customer:

Micron Semiconductor, Inc., is dedicated to the design, manufacture and marketing of high-quality, highly-reliable memory components. Our corporate mission is:

"To be a world-class team developing advantages for our customers."

At Micron, we are investing time, talent and resources to bring you the finest DRAMs, SRAMs, VRAMs and other specialty memory products. We have developed a unique intelligent burn-in system, AMBYX®, which evaluates and reports the quality level of each and every component we produce.

We are dedicated to continuous improvement of all our products and services. This means continual reduction of electrical and mechanical defect levels. It also means the addition of new services such as "just-in-time" delivery and electronic data interchange programs. And, when you have a design or application question, you can get the answers you need from the source through one of Micron's applications engineers.

We're proud of our products, our progress and our performance. And we're pleased that you're choosing Micron as your memory supplier.

The Micron Team

ADVANTAGES

Micron Semiconductor brings quality, productivity and innovation together to provide advantages for our customers. Our products feature some of the industry's fastest speeds and smallest die sizes. And we establish delivery standards based on your expectations, including JIT programs, made possible by ever-increasing product reliability.

COMPONENT INTEGRATED CIRCUITS

Micron Semiconductor entered the memory market in 1978, first designing, then manufacturing dynamic random access memory (DRAM). From there, we developed high-performance fast static RAM (SRAM), multiport DRAM (VRAM and triple-port DRAM), and a variety of other memory products.

As we bring innovative memory solutions to our customers, we enjoy recognition for our achievements. Micron's Triple-Port DRAM was the first IC ever to incorporate a second, independent serial access port, allowing unparalleled flexibility in data manipulation. Micron's Triple-Port received the 1990 "Product of the Year" award from *Electronic Products* magazine.

SPECIALTY MEMORY PRODUCTS

Beyond our standard component memory, Micron is introducing many revolutionary products that we expect will follow the triple-port's tradition. From synchronous burst SRAMs to programmable products, Micron continues to forge ahead into new and exciting frontiers.

We are pleased to be first to market with our compact, easy-to-install 88-pin DRAM card. Ideal for laptop, notebook and other portable systems, Micron's DRAM Card offers both high density and low power within JEDEC and JEIDA specifications.*

DIE SALES

In addition to our durable packaging, Micron also provides memory devices in bare die form. These are increasingly in demand for commercial and military use in highly specialized applications. Micron's bare die products are available both in 6" wafers and singulated die form.

CUSTOM MANUFACTURING SERVICES

For total project management, Micron offers value-added services. These include both standard contract manufacturing services for system-level products including design, assembly, customer kitted assembly, comprehensive quality testing or shipping as well as complete turnkey services covering all phases of production. Our component and system-level manufacturing facilities are centrally located in Boise, Idaho, so the components products you need are readily available.

MICRON DATAFAX

When you can't afford to wait for critical product information or specifications, Micron offers a convenient solution available 24 hours a day, every day. Micron DataFax enables you to make automated requests for data sheets, product literature, and other information from your fax machine. Just dial 208-368-5800 from your fax machine and Micron DataFax will give you instructions on how to order documents, including an index of documents. Once your order is placed, Micron DataFax will process you order, faxing up to two documents per call to your fax machine.

QUALITY

Without a doubt, quality is the most important thing we provide to every Micron customer with each shipment. We believe that quality must be internalized consistently at every level of our company. We provide every Micron team member with the training and motivation needed to make Micron's quality philosophy a reality.

One way we have measurably improved both productivity and product quality is through our own quality improvement program, "The Micron Challenge," formed by individuals throughout the company. Micron quality teams get together to address a wide range of issues within their areas. We regularly perform a company-wide self-assessment based on the Malcolm Baldrige National Quality Award criteria. We've also implemented statistical process controls to evaluate every facet of the memory design, fabrication, assembly and shipping process. And our AMBYX intelligent burn-in and test system** gives Micron a unique edge in product reliability

*See NOTE, page v.
**For more information on Micron's AMBYX, see Section 6.

ABOUT THIS BOOK

CONTENT

The *1994 SRAM Data Book* from Micron Semiconductor provides complete specifications on all standard SRAMs and SRAM modules as well as specialty and derivative products based on our SRAM production process.

The *SRAM Data Book* is one of three product data books Micron currently publishes. Its two companion volumes include our *DRAM Data Book* and *Specialty DRAM Data Book*. As our product lines continue to diversify, more data books will be released.

SECTION ORGANIZATION

Micron's 1993 *SRAM Data Book* contains a detailed "Table of Contents" with sequential and numerical indexes of products as well as a complete product selection guide. The data book is organized into 8 sections:

- **Sections 1–4:** Individual product families. Each contains a product selection guide followed by data sheets.
- **Section 5:** Application/technical notes.
- **Section 6:** Summary of Micron's unique quality and reliability programs and testing operation, including our AMBYX intelligent burn-in and test system.*
- **Section 7:** Packaging information.
- **Section 8:** Product ordering information, including a list of sales representatives and distributors worldwide.

DATA SHEET SEQUENCE

Data sheets in this book are ordered first by width and second by depth. For example, the SRAM section begins with the 16 Meg x 1 followed by 64 Meg x 1 and all other x1 configurations in order of ascending depth. Next come the x4 products, followed by x8, etc., as applicable to the specific product family.

DATA SHEET DESIGNATIONS

As detailed in the table below, each Micron product data sheet is classified as either "Advance," "Preliminary" or "Final." In addition, product data sheets that are new additions are designated with a "New" indicator in the tab area of the front page.

SURVEY

We have included a removable, postage-paid survey form in the front of this book. Your time in completing and returning this survey will enhance our efforts to continually improve our product literature.

For more information on Micron product literature, or to order additional copies of this publication, contact:

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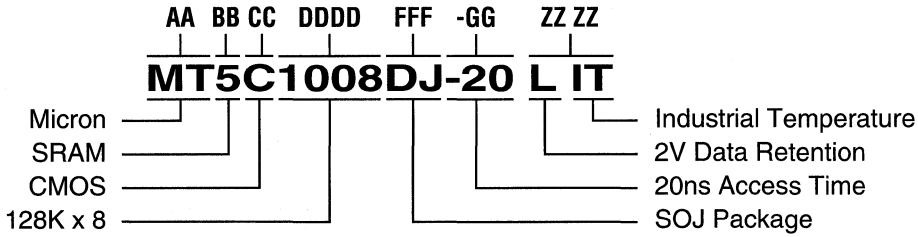
DATA SHEET DESIGNATIONS

DATA SHEET MARKING	DEFINITION
Advance	This data sheet contains initial descriptions of products still under development.
Preliminary	This data sheet contains initial characterization limits that are subject to change upon full characterization of production devices.
No Marking (Final)	This data sheet contains minimum and maximum limits specified over the complete power supply and temperature range for production devices. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.
New	This data sheet (which may be either Advance, Preliminary or Final) is a new addition to the data book.

NOTE: Micron uses acronyms to refer to certain industry-standard-setting bodies. These are defined below for your reference:
EIA/JEDEC—Electronics Industry Association/Joint Electron Device Engineering Council.
JEIDA—Japanese Electronics Industry Development Association.
PCMCIA—Personal Computer Memory Card International Association.

*Micron's *Quality/Reliability Handbook* is available by calling 208-368-3900.

CURRENT COMPONENT EXPANDED NUMBERING SYSTEM



AA – PRODUCT LINE IDENTIFIER

Micron Product ..... MT

BB – PRODUCT FAMILY

DRAM 4
DPDRAM (VRAM) 42
TPDRAM 43
SRAM 5
Synchronous SRAM 58

CC – PROCESS TECHNOLOGY

CMOS C
Low Voltage CMOS LC

DDDD – DEVICE NUMBER

(Can be modified to indicate variations)

DRAM ..... Width, Density
DPDRAM (VRAM) ..... Width, Density
TPDRAM ..... Width, Density
SRAM ..... Total Bits, Width
Synchronous SRAM ..... Density, Width

E – DEVICE VERSIONS

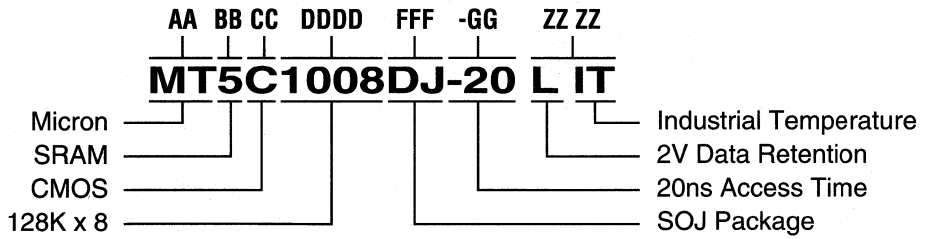
(Alphabetic characters only; located between D and F when required.)

JEDEC Test Mode (4 Meg DRAM) ..... J
Errata on Base Part ..... Q

FFF – PACKAGE CODES

PLASTIC
DIP ..... Blank
DIP (Wide Body) ..... W
ZIP ..... Z
LCC ..... EJ
SOP/SOIC ..... SG
QFP ..... LG
TSOP (Type II) ..... TG
TSOP (Reversed) ..... RG
TSOP (Longer) ..... TL
SOJ ..... DJ
SOJ (Reversed) ..... DR
SOJ (Longer) ..... DL

CURRENT COMPONENT EXPANDED NUMBERING SYSTEM (continued)



GG – ACCESS TIME

-5	5ns or 50ns
-6	6ns or 60ns
-7	7ns or 70ns
-8	8ns or 80ns
-10	10ns or 100ns
-12	12ns or 120ns
-15	15ns or 150ns
-17	17ns
-20	20ns
-25	25ns
-35	35ns
-45	45ns
-50 (SRAM only)	50ns
-53	53ns
-55	55ns
-70 (SRAM only)	70ns

ZZ ZZ – PROCESSING CODES

(Multiple processing codes are separated by a space and are listed in hierarchical order.)

Example:
A DRAM supporting low power, extended refresh (L); low voltage (V) and the industrial temperature range (IT) would be indicated as V L IT.

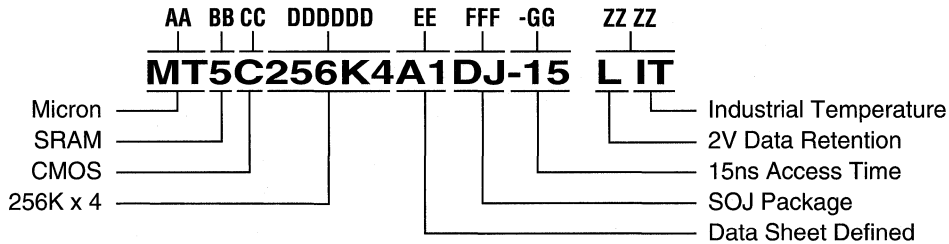
Interim	I
Low Voltage	V

ZZ ZZ – PROCESSING CODES (continued)

DRAMs	
Low Power (Extended Refresh)	L
Low Voltage, Low Power (Extended Refresh)	VL
Low Power (Self Refresh)	S
Low Voltage, Low Power (Self Refresh)	VS
SRAMs	
Low Volt Data Retention	L
Low Power	P
Low Power, Low Volt Data Retention	LP
Low Voltage, Low Power	VP
Low Voltage, Low Volt Data Retention	VL
Low Voltage, Low Volt Data Retention, Low Power	VB
EPI Wafer	E
Commercial Testing	
0°C to +70°C	Blank
-40°C to +85°C	IT
-40°C to +125°C	AT
-55°C to +125°C	XT
Special Processing	
Engineering Sample	ES
Mechanical Sample	MS
Sample Kit*	SK
Tape-and-Reel*	TR
Bar Code*	BC

* Used in device order codes; this code is not marked on device.

NEW COMPONENT NUMBERING SYSTEM



AA – PRODUCT LINE IDENTIFIER

Micron Product ..... MT

BB – PRODUCT FAMILY

DRAM 4
DPDRAM (VRAM) 42
TPDRAM 43
Synchronous DRAM 48
SRAM 5
Synchronous SRAM 58

CC – PROCESS TECHNOLOGY

CMOS C
Low Voltage CMOS LC
BiCMOS ..... B
Low Voltage BiCMOS ..... LB

DDDDDD – DEVICE NUMBER

Depth, Width

Example:
1M16 = 1 megabit deep by 16 bits wide = 16 megabits of total memory.

No Letter ..... Bits
K ..... Kilobits
M ..... Megabits
G ..... Gigabits

EE – DEVICE VERSIONS

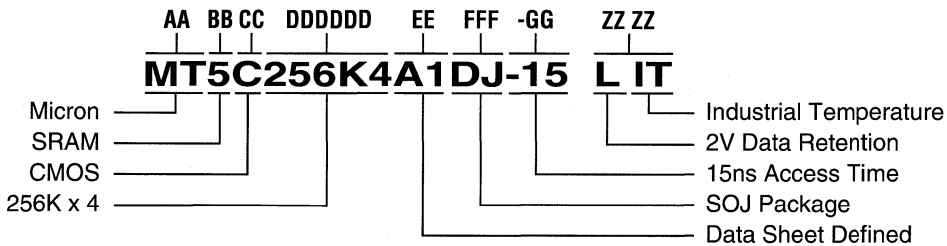
(The first character is an alphabetic character only; the second character is a numeric character only.)
Specified by individual data sheet.

FFF – PACKAGE CODES

Plastic

DIP ..... Blank
DIP (Wide Body) ..... W
ZIP ..... Z
LCC ..... EJ
SOP/SOIC ..... SG
QFP ..... LG
TSOP (Type II) ..... TG
TSOP (Reversed) ..... RG
TSOP (Longer) ..... TL
SOJ ..... DJ
SOJ (Wide) ..... DW
SOJ (Reversed) ..... DR
SOJ (Longer) ..... DL

NEW COMPONENT NUMBERING SYSTEM (continued)



GG – ACCESS TIME

-5	5ns or 50ns
-6	6ns or 60ns
-7	7ns or 70ns
-8	8ns or 80ns
-9	9ns or 90ns
-10	10ns or 100ns
-12	12ns or 120ns
-15	15ns or 150ns
-17	17ns
-20	20ns
-25	25ns
-35	35ns
-45	45ns
-53	53ns
-55	55ns

ZZ ZZ – PROCESSING CODES

(Multiple processing codes are separated by a space and are listed in hierarchical order.)

Example:
A DRAM supporting low power, extended refresh (L); low voltage (V) and the industrial temperature range (IT) would be indicated as V L IT.

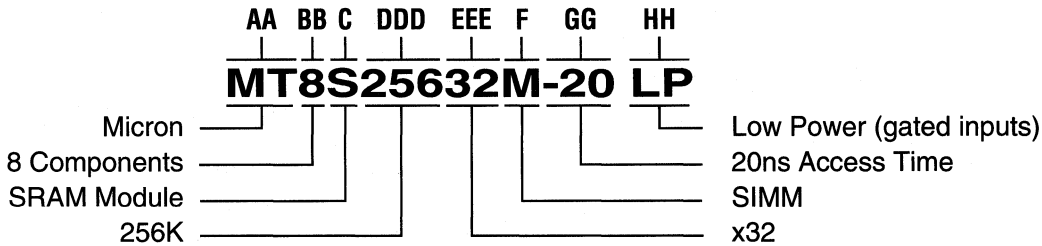
Interim	I
Low Voltage	V

ZZ ZZ – PROCESSING CODES (continued)

DRAMs	
Low Power (Extended Refresh)	L
Low Voltage, Low Power (Extended Refresh)	VL
Low Power (Self Refresh)	S
Low Voltage, Low Power (Self Refresh)	VS
SRAMs	
Low Volt Data Retention	L
Low Power	P
Low Volt Data Retention, Low Power	LP
EPI Wafer	E
Commercial Testing	
0°C to +70°C	Blank
-40°C to +85°C	IT
-40°C to +125°C	AT
-55°C to +125°C	XT
Special Processing	
Engineering Sample	ES
Mechanical Sample	MS
Sample Kit*	SK
Tape-and-Reel*	TR
Bar Code*	BC

* Used in device order codes; this code is not marked on device.

MODULE NUMBERING SYSTEM



AA – PRODUCT LINE IDENTIFIER
- Micron Product ..... MT

BB – NUMBER OF MEMORY COMPONENTS

C – RAM FAMILY
- SRAM ..... S
- DRAM ..... D
- 3.3V SRAM ..... LS
- 3.3V DRAM ..... LD

DDD – DEPTH

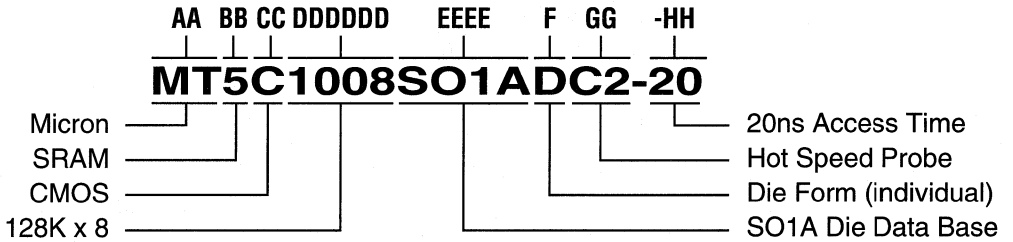
EEE – WIDTH

F – PACKAGE CODE
- DIP ..... D
- ZIP ..... Z
- SIMM ..... M
- SIP ..... N
- Gold SIMM ..... G

GG – ACCESS TIME
- -10 ..... 10ns
- -12 ..... 12ns
- -15 ..... 15ns
- -20 ..... 20ns
- -25 ..... 25ns
- -30 ..... 30ns
- -35 ..... 35ns

HH – SPECIAL DESIGNATOR
- Low Volt, Data Retention L
- Low Power (gated inputs) ..... LF

DIE PRODUCT NUMBERING SYSTEM



AA – PRODUCT LINE IDENTIFIER

Component Product ..... MT

BB – PRODUCT FAMILY

SRAM 5
DRAM 4
Synchronous SRAM 58
DPDRAM (VRAM) 42

CC – PROCESS TECHNOLOGY

CMOS C
Low Voltage CMOS LC

DDDDDD – DEVICE NUMBER

When *no* alpha character appears as part of this section, the section is defined as:

DRAM ..... Width, Density
VRAM ..... Width, Density
SRAM ..... Total Bits, Width
Synchronous SRAM ..... Depth, Width

When an alpha character occurs as part of this section, the section is defined as:
Depth, Width

Example:
1M16 = 1 megabit deep by 16 bits wide = 16 megabits of total memory.

No Letter ..... Bits
K ..... Kilobits
M ..... Megabits
G ..... Gigabits

EEEE – DIE DATA BASE REVISION

F – FORM

Die Form ..... D
Wafer Form (6" Wafer) ..... W

GG – TESTING LEVELS

Standard Probe (0° to 70°C) C1
Hot Speed Probe (0° to 70°C) C2
Standard Probe (-55° to 125°C) X1
Hot Speed Probe (-55° to 125°C) X2

HH – ACCESS TIME

(Applicable for C2 and C3 only)

-5 ..... 5ns or 50ns
-6 ..... 6ns or 60ns
-7 ..... 7ns or 70ns
-8 ..... 8ns or 80ns
-9 ..... 9ns or 90ns
-10 ..... 10ns or 100ns
-12 ..... 12ns or 120ns
-15 ..... 15ns or 150ns
-17 ..... 17ns
-20 ..... 20ns
-25 ..... 25ns
-35 ..... 35ns
-45 ..... 45ns
-50 (SRAM only) 50ns

5V SRAMS

CE ..... CHIP ENABLE
BE ..... BYTE ENABLE
REVOLUTIONARY PINOUT ..... CENTER PIN POWER AND GROUND
OE ..... OUTPUT ENABLE
LP ..... LOW POWER, LOW VOLTAGE DATA RETENTION

3.3V SRAMS

CE ... CHIP ENABLE
BE ... BYTE ENABLE
REVOLUTIONARY PINOUT ... CENTER PIN POWER AND GROUND
OE ... OUTPUT ENABLE
LP ... LOW VOLTAGE, LOW VOLTAGE DATA RETENTION and LOW POWER

5/3.3V SYNCHRONOUS SRAMS

SR ... SYNCHRONOUS READS
DSCE ... DUAL SYNCHRONOUS CHIP ENABLE
BW ... BYTE WRITE
STW ... SELF-TIMED WRITES
SWE ... SYNCHRONOUS WRITE ENABLE
SCE ... SYNCHRONOUS CHIP ENABLE

SRAM MODULES

TECHNICAL NOTES

PRODUCT RELIABILITY

PACKAGE INFORMATION

SALES INFORMATION

NUMERICAL INDEX

NUMERICAL INDEX (continued)

5V SRAM PRODUCT SELECTION GUIDE

Memory Configuration	Control Functions	Part Number	Access Time (ns)	Package and Number of Pins			Page
				PDIP	SOJ	TSOP	
16K x 1	$\overline{CE}$ only	MT5C1601	9, 10, 12, 15, 20, 25	20	24	-	1-1
64K x 1	$\overline{CE}$ only	MT5C6401	9, 10, 12, 15, 20, 25	22	24	-	1-11
256K x 1	$\overline{CE}$ only	MT5C2561	10, 12, 15, 20, 25, 35	24	24	-	1-21
1 Meg x 1	$\overline{CE}$ only	MT5C1001	12, 15, 17, 20, 25, 35	28	28	-	1-31
4K x 4	$\overline{CE}$ only	MT5C1604	9, 10, 12, 15, 20, 25	20	24	-	1-41
4K x 4	$\overline{CE}$ and $\overline{OE}$	MT5C1605	9, 10, 12, 15, 20, 25	22	24	-	1-51
16K x 4	$\overline{CE}$ only	MT5C6404	9, 10, 12, 15, 20, 25	22	24	-	1-61
16K x 4	$\overline{CE}$ and $\overline{OE}$	MT5C6405	9, 10, 12, 15, 20, 25	24	24	-	1-71
64K x 4	$\overline{CE}$ only	MT5C2564	10, 12, 15, 20, 25, 35	24	24	-	1-81
64K x 4	$\overline{CE}$ and $\overline{OE}$	MT5C2565	10, 12, 15, 20, 25, 35	28	28	-	1-91
256K x 4	$\overline{CE}$ and $\overline{OE}$	MT5C1005	12, 15, 17, 20, 25, 35	28	28	-	1-101
256K x 4	$\overline{CE}$, $\overline{OE}$ and Revolutionary Pinout	MT5C256K4A1	12, 15, 20, 25	-	32	-	1-111
1 Meg x 4	$\overline{CE}$, $\overline{OE}$ and Revolutionary Pinout	MT5C1M4B2	12, 15, 20, 25, 35	-	32	32	1-121
2K x 8	$\overline{CE}$ and $\overline{OE}$	MT5C1608	9, 10, 12, 15, 20, 25	24	24	-	1-131
8K x 8	$\overline{CE1}$, CE2 and $\overline{OE}$	MT5C6408	9, 10, 12, 15, 20, 25	28	28	-	1-141
32K x 8	$\overline{CE}$ and $\overline{OE}$	MT5C2568	10, 12, 15, 20, 25, 35	28	28	-	1-151
128K x 8	$\overline{CE1}$, CE2 and $\overline{OE}$	MT5C1008	12, 15, 17, 20, 25, 35	32	32	-	1-161
128K x 8	$\overline{CE}$, $\overline{OE}$ and Revolutionary Pinout	MT5C128K8A1	12, 15, 20, 25	-	32	-	1-171
512K x 8	$\overline{CE}$, $\overline{OE}$ and Revolutionary Pinout	MT5C512K8B2	12, 15, 20, 25, 35	-	36	36	1-181
128K x 9	$\overline{CE}$ and $\overline{OE}$	MT5C1189	15*, 17, 20, 25, 35	-	32	-	1-191
64K x 16	$\overline{CE}$, $\overline{OE}$, Byte Enable and Revolutionary Pinout	MT5C64K16A1	12, 15, 20, 25	-	44	44	1-201
256K x 16	$\overline{CE}$, $\overline{OE}$, Byte Enable	MT5C256K16B2	12, 15, 20, 25, 35	-	54	54	1-211

NOTE: 1. Many Micron components are available in bare die form. Contact Micron Semiconductor, Inc., for more information.
*Preliminary

3.3V SRAM PRODUCT SELECTION GUIDE

Memory Configuration	Control Functions	Part Number	Access Time (ns)	Package and Number of Pins			Page
				PDIP	SOJ	TSOP	
256K x 1	$\overline{CE}$ only with separate I/O	MT5LC2561	12, 15, 20, 25, 35	24	24	-	2-1
1 Meg x 1	$\overline{CE}$ only with separate I/O	MT5LC1001	15, 17, 20, 25, 35, 45	28	28	-	2-9
64K x 4	$\overline{CE}$ only	MT5LC2564	12, 15, 20, 25, 35	24	24	-	2-17
64K x 4	$\overline{CE}$ and $\overline{OE}$	MT5LC2565	12, 15, 20, 25, 35	28	28	-	2-25
256K x 4	$\overline{CE}$ and $\overline{OE}$	MT5LC1005	15, 17, 20, 25, 35, 45	28	28	-	2-33
256K x 4	$\overline{CE}$ and Revolutionary Pinout	MT5LC256K4D4	15, 20, 25	-	32	32	2-41
1 Meg x 4	$\overline{CE}$, $\overline{OE}$ and Revolutionary Pinout	MT5LC1M4D4	12, 15, 20, 25, 35	-	32	32	2-51
32K x 8	$\overline{CE}$ and $\overline{OE}$	MT5LC2568	12, 15, 20, 25, 35	28	28	-	2-59
128K x 8	$\overline{CE1}$, CE2 and $\overline{OE}$	MT5LC1008	15, 17, 20, 25, 35, 45	32	32	-	2-67
128K x 8	$\overline{CE}$, $\overline{OE}$ and Revolutionary Pinout	MT5LC128K8D4	15, 20, 25	-	32	32	2-75
512K x 8	$\overline{CE}$, $\overline{OE}$ and Revolutionary Pinout	MT5LC512K8D4	12, 15, 20, 25, 35	-	36	36	2-85
64K x 16	$\overline{CE}$, $\overline{OE}$, Byte Enable and Revolutionary Pinout	MT5LC64K16D4	15, 20, 25	-	44	44	2-93
256K x 16	$\overline{CE}$, $\overline{OE}$, Byte Enable	MT5LC256K16D4	12, 15, 20, 25, 35	-	54	54	2-103

NOTE: 1. Many Micron components are available in bare die form. Contact Micron Semiconductor, Inc., for more information.

5/3.3V SYNCHRONOUS SRAM PRODUCT SELECTION GUIDE

Memory Configuration	Supply Voltage	Control Functions	Part Number	Access Time (ns)	Cycle Time (ns)	Package and Number of Pins				Page
						SOJ	PLCC	TQFP	DIE	
128K x 9	5V	SPARC® architecture	MT58C1289	6,8,10	12*,16.6,20	32	-	-	CD1/CD2	3-1
64K x 18	3.3V	Intel Burst	MT58LC64K18B2	9,10,12,17	15,15,20,25	-	52	100	CD1/CD2	3-11
64K x 18	3.3V	Intel Burst, Pipelined	MT58LC64K18C4	7,10,12,15	15,20,25,30	-	52	100	CD1/CD2	3-23
64K x 18	3.3V	Linear Burst	MT58LC64K18M1	9,10,12,17	15,15,20,25	-	52	100	CD1/CD2	3-37
64K x 18	3.3V	Linear Burst, Pipelined	MT58LC64K18A6	7,10,12,15	15,20,25,30	-	52	100	CD1/CD2	3-49
32K x 36	3.3V	Intel Burst	MT58LC32K36B2	9,10,12,17	15,15,20,25	-	-	100	CD1/CD2	3-61
32K x 36	3.3V	Intel Burst, Pipelined	MT58LC32K36C4	7,10,12,15	15,20,25,30	-	-	100	CD1/CD2	3-75
32K x 36	3.3V	Linear Burst	MT58LC32K36M1	9,10,12,17	15,15,20,25	-	-	100	CD1/CD2	3-89
32K x 36	3.3V	Linear Burst, Pipelined	MT58LC32K36A6	7,10,12,15	15,20,25,30	-	-	100	CD1/CD2	3-103

NOTE: 1. Many Micron components are available in bare die form. Contact Micron Semiconductor, Inc., for more information.
*Preliminary

SRAM MODULE PRODUCT SELECTION GUIDE

Memory Configuration	Optional Access Cycle	Part Number	Access Time (ns)	Package and No. of Pins		Page
				ZIP	SIMM	
16K x 32	$\overline{CE}$ and $\overline{OE}$	MT8S1632	10*, 12, 15, 20, 25	64	64	4-1
64K x 32	$\overline{CE}$ and $\overline{OE}$	MT8S6432	12*, 15, 20, 25, 30, 35	64	64	4-9
64K x 32	$\overline{CE}$ and $\overline{OE}$	MT8LS6432	17, 20, 25, 35	64	64	4-17
128K x 32	$\overline{CE}$ and $\overline{OE}$	MT4S12832	15*, 20, 25, 35	64	64	4-25
128K x 32	$\overline{CE}$ and $\overline{OE}$	MT4LS12832	17, 20, 25, 35	64	64	4-33
256K x 32	$\overline{CE}$ and $\overline{OE}$	MT8S25632	15*, 20, 25, 35	64	64	4-41
256K x 32	$\overline{CE}$ and $\overline{OE}$	MT8LS25632	17, 20, 25, 35	64	64	4-49

*Preliminary

TECHNICAL NOTE SELECTION GUIDE

Technical Note	Title	Page
TN-00-01	Moisture Absorption in Plastic Packages	5-1
TN-00-02	Tape-and-Reel Procedures	5-3
TN-05-02	SRAM Bus Contention Design Considerations	5-9
TN-05-03	SRAM Capacitive Loading	5-13
TN-05-06	1 Meg Fast SRAM Typical Operating Curves	5-15
TN-05-07	256K Fast SRAM Typical Operating Curves	5-17
TN-05-08	64K Fast SRAM Typical Operating Curves	5-21
TN-05-13	1 Meg Low-Power SRAMs	5-23
TN-05-14	SRAM Thermal Design Considerations	5-27
TN-05-15	Design Tips: 32K x 36 Synchronous SRAM	5-33
TN-05-16	A Designer's Guide to 3.3V SRAMs	5-39

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5V SRAM PRODUCT SELECTION GUIDE

Memory Configuration	Control Functions	Part Number	Access Time (ns)	Package and Number of Pins			Page
				PDIP	SOJ	TSOP	
16K x 1	$\overline{CE}$ only	MT5C1601	9, 10, 12, 15, 20, 25	20	24	-	1-1
64K x 1	$\overline{CE}$ only	MT5C6401	9, 10, 12, 15, 20, 25	22	24	-	1-11
256K x 1	$\overline{CE}$ only	MT5C2561	10, 12, 15, 20, 25, 35	24	24	-	1-21
1 Meg x 1	$\overline{CE}$ only	MT5C1001	12, 15, 17, 20, 25, 35	28	28	-	1-31
4K x 4	$\overline{CE}$ only	MT5C1604	9, 10, 12, 15, 20, 25	20	24	-	1-41
4K x 4	$\overline{CE}$ and $\overline{OE}$	MT5C1605	9, 10, 12, 15, 20, 25	22	24	-	1-51
16K x 4	$\overline{CE}$ only	MT5C6404	9, 10, 12, 15, 20, 25	22	24	-	1-61
16K x 4	$\overline{CE}$ and $\overline{OE}$	MT5C6405	9, 10, 12, 15, 20, 25	24	24	-	1-71
64K x 4	$\overline{CE}$ only	MT5C2564	10, 12, 15, 20, 25, 35	24	24	-	1-81
64K x 4	$\overline{CE}$ and $\overline{OE}$	MT5C2565	10, 12, 15, 20, 25, 35	28	28	-	1-91
256K x 4	$\overline{CE}$ and $\overline{OE}$	MT5C1005	12, 15, 17, 20, 25, 35	28	28	-	1-101
256K x 4	$\overline{CE}$, $\overline{OE}$ and Revolutionary Pinout	MT5C256K4A1	12, 15, 20, 25	-	32	-	1-111
1 Meg x 4	$\overline{CE}$, $\overline{OE}$ and Revolutionary Pinout	MT5C1M4B2	12, 15, 20, 25, 35	-	32	32	1-121
2K x 8	$\overline{CE}$ and $\overline{OE}$	MT5C1608	9, 10, 12, 15, 20, 25	24	24	-	1-131
8K x 8	$\overline{CE1}$, CE2 and $\overline{OE}$	MT5C6408	9, 10, 12, 15, 20, 25	28	28	-	1-141
32K x 8	$\overline{CE}$ and $\overline{OE}$	MT5C2568	10, 12, 15, 20, 25, 35	28	28	-	1-151
128K x 8	$\overline{CE1}$, CE2 and $\overline{OE}$	MT5C1008	12, 15, 17, 20, 25, 35	32	32	-	1-161
128K x 8	$\overline{CE}$, $\overline{OE}$ and Revolutionary Pinout	MT5C128K8A1	12, 15, 20, 25	-	32	-	1-171
512K x 8	$\overline{CE}$, $\overline{OE}$ and Revolutionary Pinout	MT5C512K8B2	12, 15, 20, 25, 35	-	36	36	1-181
128K x 9	$\overline{CE}$ and $\overline{OE}$	MT5C1189	15*, 17, 20, 25, 35	-	32	-	1-191
64K x 16	$\overline{CE}$, $\overline{OE}$, Byte Enable and Revolutionary Pinout	MT5C64K16A1	12, 15, 20, 25	-	44	44	1-201
256K x 16	$\overline{CE}$, $\overline{OE}$, Byte Enable	MT5C256K16B2	12, 15, 20, 25, 35	-	54	54	1-211

NOTE: 1. Many Micron components are available in bare die form. Contact Micron Semiconductor, Inc., for more information.
*Preliminary

SRAM

16K x 1 SRAM

FEATURES

- High speed: 9, 10, 12, 15, 20 and 25ns
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ option
- All inputs and outputs are TTL-compatible

OPTIONS / MARKING

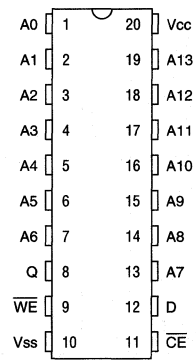
• Timing		
9ns access		- 9
10ns access		-10
12ns access		-12
15ns access		-15
20ns access		-20
25ns access		-25
• Packages		
Plastic DIP (300 mil)		None
Plastic SOJ (300 mil)		DJ
• 2V data retention		L
• Temperature		
Commercial	(0°C to +70°C)	None
Industrial	(-40°C to +85°C)	IT
Automotive	(-40°C to +125°C)	AT
Extended	(-55°C to +125°C)	XT

- Part Number Example: MT5C1601DJ-12 L

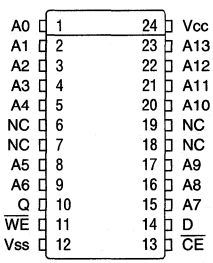
NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

20-Pin DIP (SA-1)



24-Pin SOJ (SD-1)



GENERAL DESCRIPTION

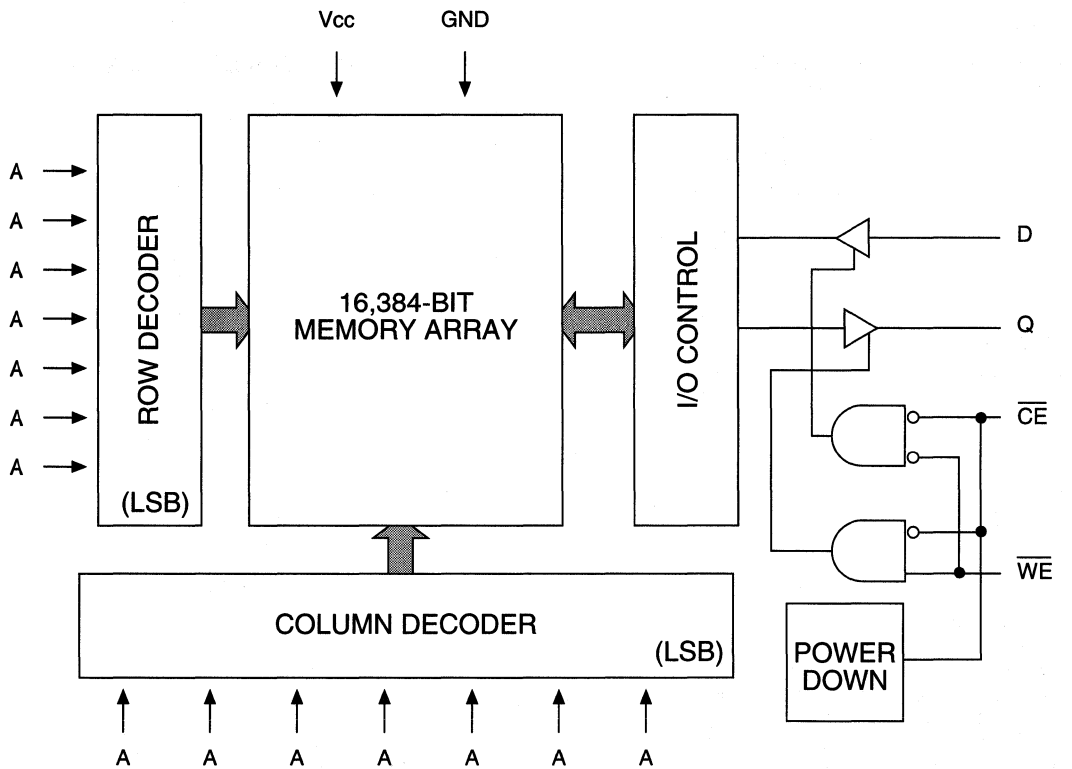
The MT5C1601 is organized as a 16384 x 1 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) with all organizations. This enhancement can place the outputs in High-Z for additional flexibility in system design. The x1 configuration features separate data input and output.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL-compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	INPUT	OUTPUT	POWER
STANDBY	H	X	DON'TCARE	HIGH-Z	STANDBY
READ	L	H	DON'TCARE	Q	ACTIVE
WRITE	L	L	DATA-IN	HIGH-Z	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA
Voltage on Any Pin Relative to V_{SS} ..... -1V to V_{CC} +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

				MAX							
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-9	-10	-12	-15	-20	-25	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	125	190	185	175	165	140	130	mA	3, 13
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	22	60	50	45	40	35	35	mA	13
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	0.5	3	3	3	3	3	5	mA	13

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	7	pF	4
Output Capacitance	V_{CC} = 5V	C_O	7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION		-9		-10		-12		-15		-20		-25			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle															
READ cycle time	^tRC	9		10		12		15		20		25		ns	
Address access time	^tAA		9		10		12		15		20		25	ns	
Chip Enable access time	^tACE		9		9		10		12		15		20	ns	
Output hold from address change	^tOH	3		3		3		3		3		3		ns	
Chip Enable to output in Low-Z	^tLZCE	2		2		2		2		2		2		ns	7, 14
Chip disable to output in High-Z	^tHZCE		5		5		6		7		8		8	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		0		0		ns	
Chip disable to power-down time	^tPD		9		10		12		15		20		25	ns	
WRITE Cycle															
WRITE cycle time	^tWC	9		10		12		15		20		25		ns	
Chip Enable to end of write	^tCW	7		8		10		12		15		20		ns	
Address valid to end of write	^tAW	7		8		10		12		15		20		ns	
Address setup time	^tAS	0		0		0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		0		0		ns	
WRITE pulse width	^tWP	6		7		8		10		12		15		ns	
Data setup time	^tDS	5		6		7		8		9		10		ns	
Data hold time	^tDH	1		1		1		1		1		1		ns	
Write disable to output in Low-Z	^tLZWE	2		2		2		2		2		2		ns	7
Write Enable to output in High-Z	^tHZWE		4		5		5		6		8		8	ns	6, 7

INDUSTRIAL TEMPERATURE SPECIFICATIONS (IT)

The following specifications are to be used for Industrial Temperature (IT) MT5C1601 SRAMs.
(-40°C ≤ T_A ≤ 85°C)

			MAX						
DESCRIPTION	**CONDITIONS**	**SYMBOL**	**-10**	**-12**	**-15**	**-20**	**-25**	**UNITS**	**NOTES**
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	195	185	175	150	140	mA	3, 13
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	60	50	45	40	40	mA	13
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	5	5	5	5	5	mA	13

DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	**CONDITIONS**		**SYMBOL**	**TYP**	**MAX**	**UNITS**	**NOTES**
Data Retention Current	$\overline{CE}$ ≥ (V_{CC} -0.2V) V_{IN} ≥ (V_{CC} -0.2V) or ≤ 0.2V	V_{CC} = 2V	I_{CCDR}	130	300	µA	14
		V_{CC} = 3V	I_{CCDR}	210	550	µA	14

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

Refer to commercial temperature timing parameters for specifications not listed here.
(Notes 5, 14) (-40°C ≤ T_A ≤ 85°C)

DESCRIPTION		-12		-15		-20		-25			
	SYM	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ Cycle											
Output hold from address change	^tOH	2		2		2		2		ns	
Chip Enable to output in Low-Z	^tLZCE	1		1		1		1		ns	7
WRITE Cycle											
Write disable to output in Low-Z	^tLZWE	1		1		1		1		ns	7

AUTOMOTIVE AND EXTENDED TEMPERATURE SPECIFICATIONS (AT AND XT)

The following specifications are to be used for Automotive Temperature (AT) and Extended Temperature (XT) MT5C1601 SRAMs. (-40°C ≤ T_A ≤ 125°C - AT) (-55°C ≤ T_A ≤ 125°C - XT)

			MAX					
DESCRIPTION	**CONDITIONS**	**SYMBOL**	**-12**	**-15**	**-20**	**-25**	**UNITS**	**NOTES**
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	185	175	150	140	mA	3, 13
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	50	45	40	40	mA	13
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	5	5	5	5	mA	13

DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	**CONDITIONS**		**SYMBOL**	**TYP**	**MAX**	**UNITS**	**NOTES**
Data Retention Current	$\overline{CE}$ ≥ (V_{CC} -0.2V) V_{IN} ≥ (V_{CC} -0.2V) or ≤ 0.2V	V_{CC} = 2V	I_{CCDR}	130	300	µA	14
		V_{CC} = 3V	I_{CCDR}	210	550	µA	14

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

Refer to commercial temperature timing parameters for specifications not listed here.
(Notes 5, 14) (-40°C ≤ T_A ≤ 125°C; -55°C ≤ T_A ≤ 125°C; V_{CC} = 5V ±10%)

DESCRIPTION		-12		-15		-20		-25			
	SYM	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ Cycle											
Output hold from address change	^tOH	2		2		2		2		ns	
Chip Enable to output in Low-Z	^tLZCE	1		1		1		1		ns	7
WRITE Cycle											
Write disable to output in Low-Z	^tLZWE	1		1		1		1		ns	7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

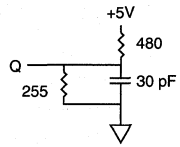


Fig. 1 OUTPUT LOAD EQUIVALENT

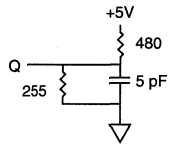


Fig. 2 OUTPUT LOAD EQUIVALENT

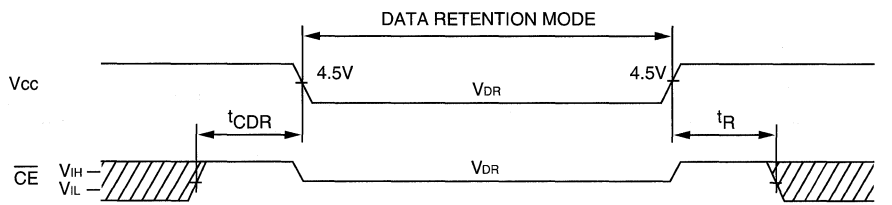
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < ^{t}RC/2ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Typical values are measured at 5V, 25°C and 15ns cycle time.
14. Typical currents are measured at 25°C.

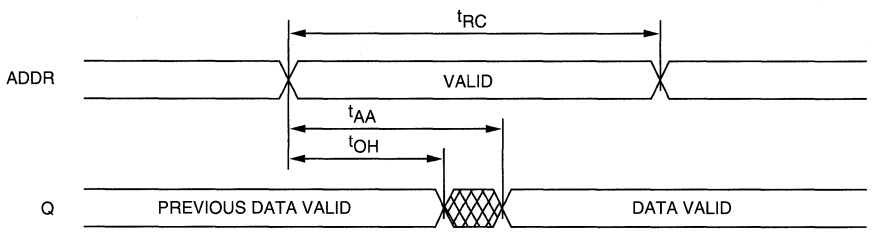
DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2			V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	ICCDR		130	300	µA	14
		Vcc = 3V	ICCDR		210	400	µA	14
Chip Deselect to Data Retention Time			^{t}CDR	0			ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

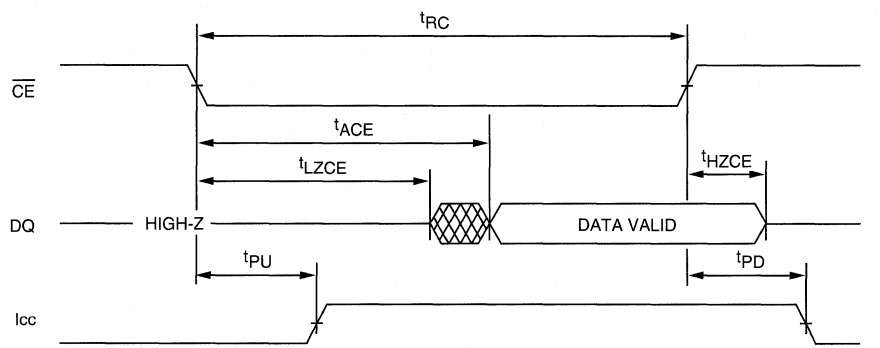
LOW Vcc DATA RETENTION WAVEFORM



READ CYCLE NO. 1 [8, 9]



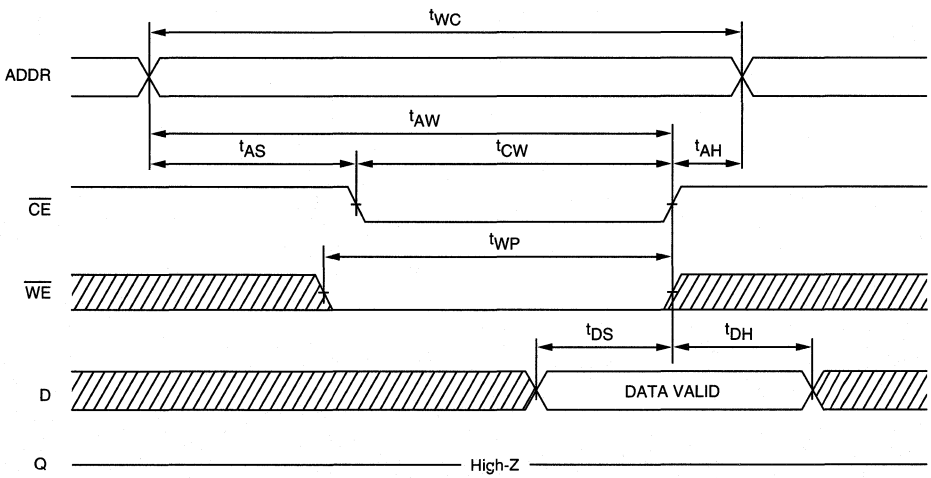
READ CYCLE NO. 2 [7, 8, 10]



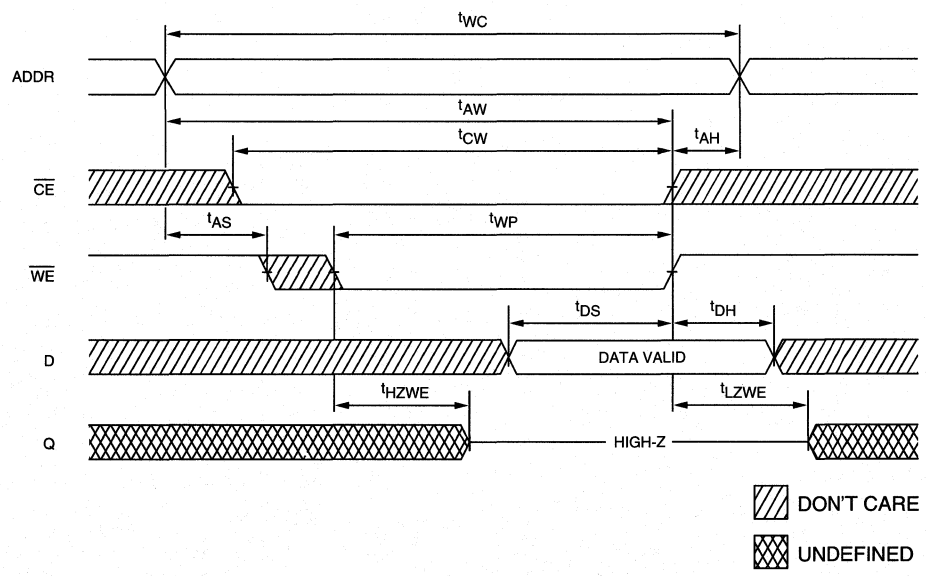
DON'T CARE

UNDEFINED

WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)



WRITE CYCLE NO. 2 [7, 12]
(Write Enable Controlled)



SRAM

64K x 1 SRAM

FEATURES

- High speed: 9, 10, 12, 15, 20 and 25ns
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ option
- All inputs and outputs are TTL-compatible

OPTIONS

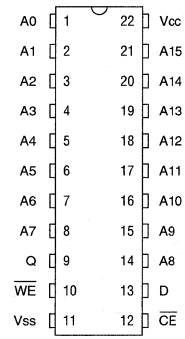
	MARKING
• Timing	
9ns access	- 9
10ns access	-10
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
• Packages	
Plastic DIP (300 mil)	None
Plastic SOJ (300 mil)	DJ
• 2V data retention	L
• Temperature	
Commercial (0°C to +70°C)	None
Industrial (-40°C to +85°C)	IT
Automotive (-40°C to +125°C)	AT
Extended (-55°C to +125°C)	XT

- Part Number Example: MT5C6401DJ-10 L

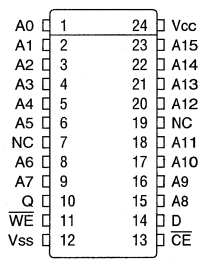
NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

22-Pin DIP
(SA-2)



24-Pin SOJ
(SD-1)



GENERAL DESCRIPTION

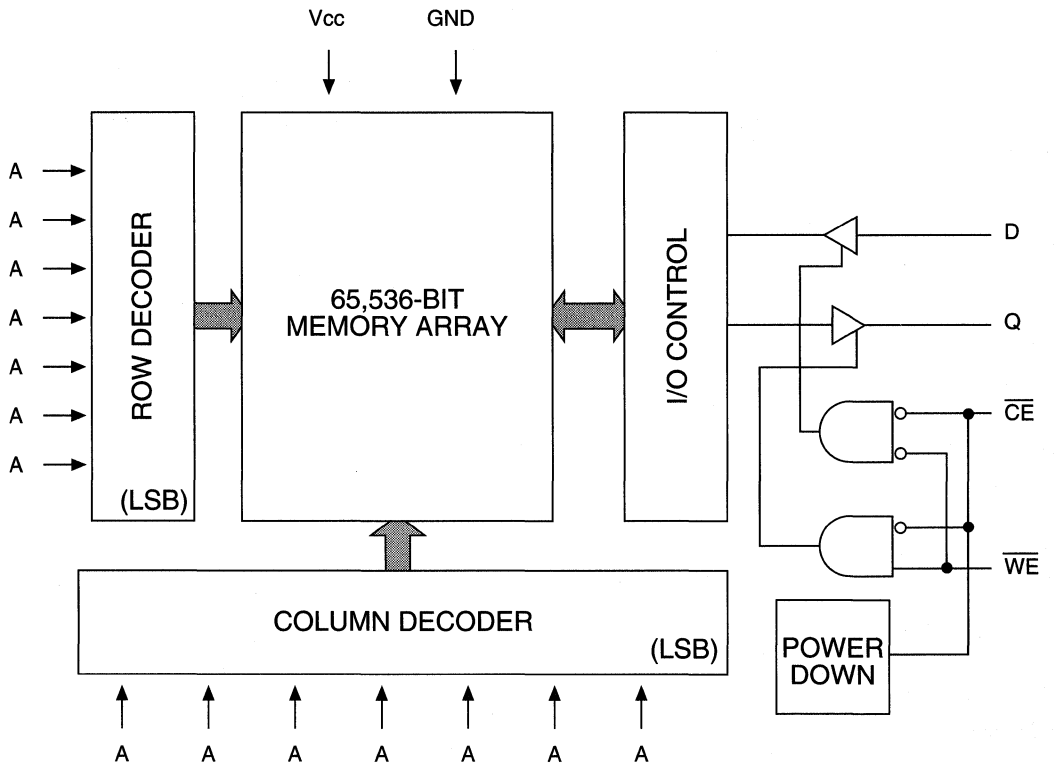
The MT5C6401 is organized as a 65,556 x 1 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) with all organizations. This enhancement can place the outputs in High-Z for additional flexibility in system design. The x1 configuration features separate data input and output.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL-compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	INPUT	OUTPUT	POWER
STANDBY	H	X	DON'T CARE	HIGH-Z	STANDBY
READ	L	H	DON'T CARE	Q	ACTIVE
WRITE	L	L	DATA-IN	HIGH-Z	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA
Voltage on Any Pin Relative to V_{SS} ..... -1V to V_{CC} +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

				MAX							
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-9	-10	-12	-15	-20	-25	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	125	190	185	175	165	140	130	mA	3, 13
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	22	60	50	45	40	35	35	mA	13
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	0.5	3	3	3	3	3	5	mA	13

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	7	pF	4
Output Capacitance	V_{CC} = 5V	C_O	7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION		-9		-10		-12		-15		-20		-25			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle															
READ cycle time	^tRC	9		10		12		15		20		25		ns	
Address access time	^tAA		9		10		12		15		20		25	ns	
Chip Enable access time	^tACE		9		9		10		12		15		20	ns	
Output hold from address change	^tOH	3		3		3		3		3		3		ns	
Chip Enable to output in Low-Z	^tLZCE	2		2		2		2		2		2		ns	7, 14
Chip disable to output in High-Z	^tHZCE		5		5		6		7		8		8	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		0		0		ns	
Chip disable to power-down time	^tPD		9		10		12		15		20		25	ns	
WRITE Cycle															
WRITE cycle time	^tWC	9		10		12		15		20		25		ns	
Chip Enable to end of write	^tCW	7		8		10		12		15		20		ns	
Address valid to end of write	^tAW	7		8		10		12		15		20		ns	
Address setup time	^tAS	0		0		0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		0		0		ns	
WRITE pulse width	^tWP	6		7		8		10		12		15		ns	
Data setup time	^tDS	5		6		7		8		9		10		ns	
Data hold time	^tDH	1		1		1		1		1		1		ns	
Write disable to output in Low-Z	^tLZWE	2		2		2		2		2		2		ns	7
Write Enable to output in High-Z	^tHZWE		4		5		5		6		8		8	ns	6, 7

INDUSTRIAL TEMPERATURE SPECIFICATIONS (IT)

The following specifications are to be used for Industrial Temperature (IT) MT5C6401 SRAMs.
(-40°C ≤ T_A ≤ 85°C)

			MAX						
DESCRIPTION	**CONDITIONS**	**SYMBOL**	**-10**	**-12**	**-15**	**-20**	**-25**	**UNITS**	**NOTES**
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	195	185	175	150	140	mA	3, 13
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	60	50	45	40	40	mA	13
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	5	5	5	5	5	mA	13

DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	**CONDITIONS**		**SYMBOL**	**TYP**	**MAX**	**UNITS**	**NOTES**
Data Retention Current	$\overline{CE}$ ≥ (V_{CC} -0.2V) V_{IN} ≥ (V_{CC} -0.2V) or ≤ 0.2V	V_{CC} = 2V	I_{CCDR}	130	300	µA	14
		V_{CC} = 3V	I_{CCDR}	210	550	µA	14

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

Refer to commercial temperature timing parameters for specifications not listed here.
(Notes 5, 14) (-40°C ≤ T_A ≤ 85°C)

DESCRIPTION		-12		-15		-20		-25			
	SYM	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ Cycle											
Output hold from address change	^tOH	2		2		2		2		ns	
Chip Enable to output in Low-Z	^tLZCE	1		1		1		1		ns	7
WRITE Cycle											
Write disable to output in Low-Z	^tLZWE	1		1		1		1		ns	7

AUTOMOTIVE AND EXTENDED TEMPERATURE SPECIFICATIONS (AT AND XT)

The following specifications are to be used for Automotive Temperature (AT) and Extended Temperature (XT) MT5C6401 SRAMs. (-40°C ≤ T_A ≤ 125°C - AT) (-55°C ≤ T_A ≤ 125°C - XT)

			MAX					
DESCRIPTION	**CONDITIONS**	**SYMBOL**	**-12**	**-15**	**-20**	**-25**	**UNITS**	**NOTES**
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	185	175	150	140	mA	3, 13
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	50	45	40	40	mA	13
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	5	5	5	5	mA	13

DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	**CONDITIONS**		**SYMBOL**	**TYP**	**MAX**	**UNITS**	**NOTES**
Data Retention Current	$\overline{CE}$ ≥ (V_{CC} -0.2V) V_{IN} ≥ (V_{CC} -0.2V) or ≤ 0.2V	V_{CC} = 2V	I_{CCDR}	130	300	µA	14
		V_{CC} = 3V	I_{CCDR}	210	550	µA	14

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

Refer to commercial temperature timing parameters for specifications not listed here.
(Notes 5, 14) (-40°C ≤ T_A ≤ 125°C; -55°C ≤ T_A ≤ 125°C; V_{CC} = 5V ±10%)

DESCRIPTION		-12		-15		-20		-25			
	SYM	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ Cycle											
Output hold from address change	^tOH	2		2		2		2		ns	
Chip Enable to output in Low-Z	^tLZCE	1		1		1		1		ns	7
WRITE Cycle											
Write disable to output in Low-Z	^tLZWE	1		1		1		1		ns	7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

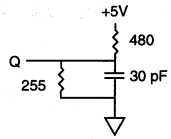


Fig. 1 OUTPUT LOAD EQUIVALENT

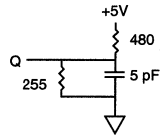


Fig. 2 OUTPUT LOAD EQUIVALENT

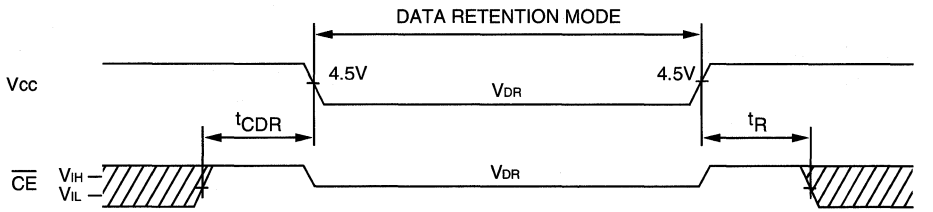
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE and ^{t}HZWE is less than ^{t}LZWE
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Typical values are measured at 5V, 25°C and 15ns cycle time.
14. Typical currents are measured at 25°C.

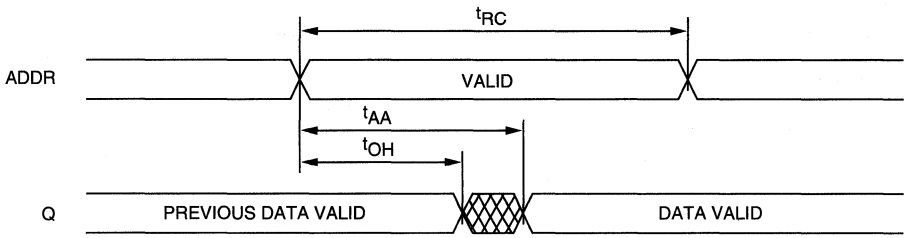
DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2			V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	ICCDR		130	300	µA	14
		Vcc = 3V	ICCDR		210	400	µA	14
Chip Deselect to Data Retention Time			^{t}CDR	0			ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

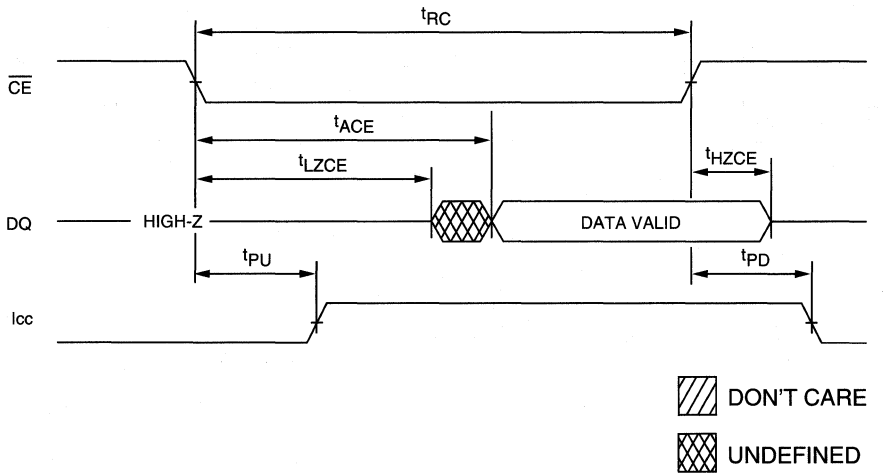
LOW Vcc DATA RETENTION WAVEFORM



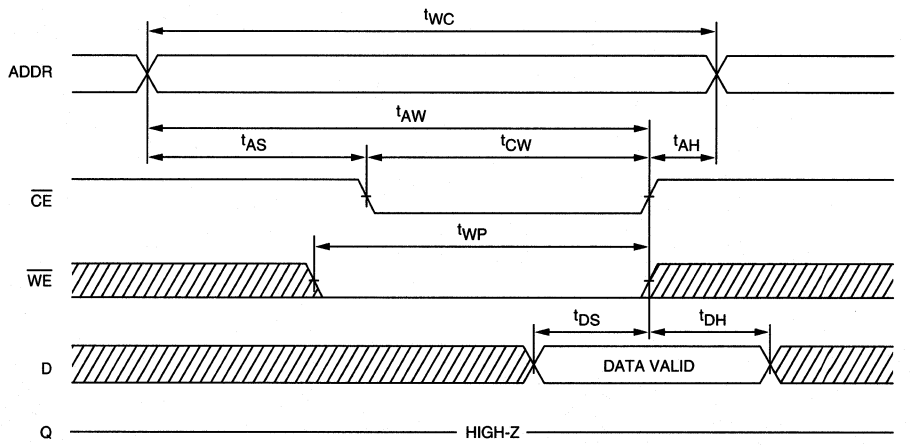
READ CYCLE NO. 1 [8, 9]



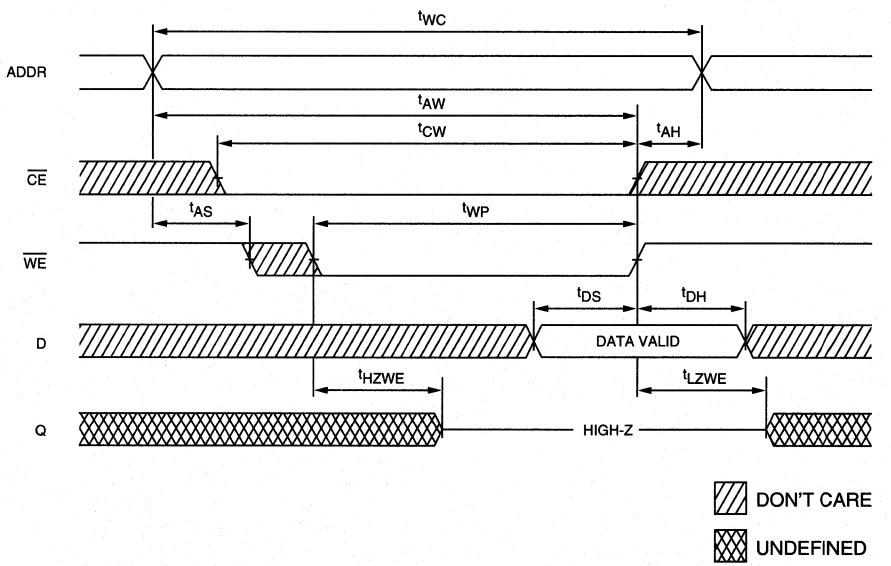
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)



WRITE CYCLE NO. 2 [7, 12]
(Write Enable Controlled)



SRAM

256K x 1 SRAM

FEATURES

- High speed: 10, 12, 15, 20, 25 and 35ns
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ option
- All inputs and outputs are TTL-compatible

OPTIONS

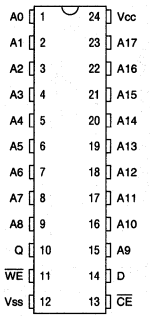
	MARKING
• Timing	
10ns access	-10
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
35ns access	-35
• Packages	
Plastic DIP (300 mil)	None
Plastic SOJ (300 mil)	DJ
• 2V data retention	L
• Low power	P
• Temperature	
Commercial (0°C to +70°C)	None
Industrial (-40°C to +85°C)	IT
Automotive (-40°C to +125°C)	AT
Extended (-55°C to +125°C)	XT

- Part Number Example: MT5C2561DJ-15 P

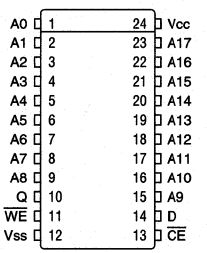
NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

24-Pin DIP
(SA-3)



24-Pin SOJ
(SD-1)



GENERAL DESCRIPTION

The MT5C2561 is organized as a 262,144 x 1 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

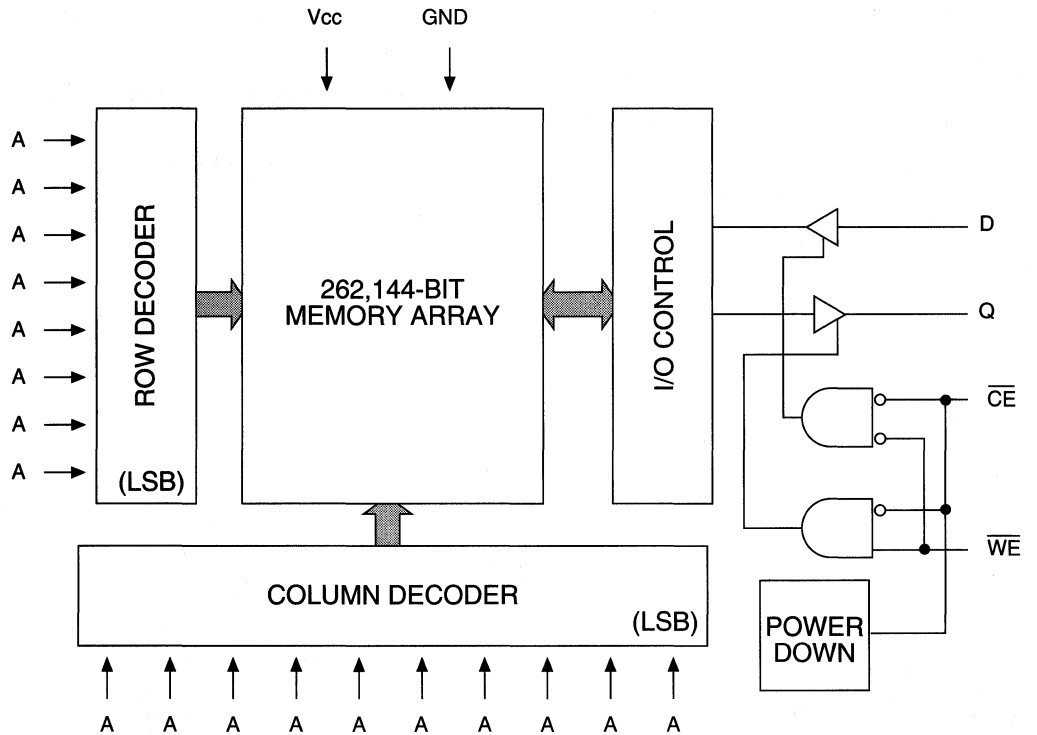
For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) with all organizations. This enhancement can place the outputs in High-Z for additional flexibility in system design. The x1 configuration features separate data input and output.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

The "P" version provides a reduction in both operating current (I_{CC}) and TTL standby current (I_{SB1}). The latter is achieved through the use of gated inputs on the $\overline{WE}$ and address lines, which also facilitates the design of battery backed systems. That is, the gated inputs simplify the design effort and circuitry required to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL-compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	INPUT	OUTPUT	POWER
STANDBY	H	X	DON'T CARE	HIGH-Z	STANDBY
READ	L	H	DON'T CARE	Q	ACTIVE
WRITE	L	L	DATA-IN	HIGH-Z	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA
Voltage on Any Pin Relative to V_{SS} ..... -1V to V_{CC} +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

					MAX							
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-10**	-12**	-15	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	103	190	170	150	130	125	120	mA	3, 13
	P version	I_{CC}	96	-	-	135	125	120	115	mA	3, 13
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	24	55	50	45	40	35	35	mA	13
	P version	I_{SB1}	1.4	-	-	4	4	4	4	mA	13
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	0.6	5	5	5	5	5	7	mA	13
	P version	I_{SB2}	0.4	-	-	3	3	3	3	mA	13

**P version not available with this speed.

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	6	pF	4
Output Capacitance	V_{CC} = 5V	C_O	6	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) ($0°C \le T_A \le 70°C$; $V_{CC} = 5V \pm 10\%$)

DESCRIPTION	SYM	-10		-12		-15		-20		-25		-35		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
READ Cycle															
READ cycle time	tRC	10		12		15		20		25		35		ns	
Address access time	tAA		10		12		15		20		25		35	ns	
Chip Enable access time	tACE		10		12		15		20		25		35	ns	
Output hold from address change	tOH	3		3		3		3		3		3		ns	
Chip Enable to output in Low-Z	tLZCE	3		3		3		3		3		3		ns	7
Chip disable to output in High-Z	tHZCE		5		6		8		9		9		15	ns	6, 7
Chip Enable to power-up time	tPU	0		0		0		0		0		0		ns	
Chip disable to power-down time	tPD		10		12		15		20		25		35	ns	
WRITE Cycle															
WRITE cycle time	tWC	10		12		15		20		25		35		ns	
Chip Enable to end of write	tCW	7		8		10		12		15		20		ns	
Address valid to end of write	tAW	7		8		10		12		15		20		ns	
Address setup time	tAS	0		0		0		0		0		0		ns	
Address hold from end of write	tAH	1		1		1		1		1		1		ns	
WRITE pulse width	tWP	7		8		10		12		15		20		ns	
Data setup time	tDS	6		7		7		10		10		15		ns	
Data hold time	tDH	0		0		0		0		0		0		ns	
Write disable to output in Low-Z	tLZWE	2		2		2		2		2		2		ns	7
Write Enable to output in High-Z	tHZWE		5		6		7		8		10		12	ns	6, 7

*Preliminary

INDUSTRIAL TEMPERATURE SPECIFICATIONS (IT)

The following specifications are to be used for Industrial Temperature (IT) MT5C2561 SRAMs.
(-40°C ≤ T_A ≤ 85°C)

			MAX							
DESCRIPTION	**CONDITIONS**	**SYM**	**-10**	**-12**	**-15**	**-20**	**-25**	**-35**	**UNITS**	**NOTES**
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	200	180	155	140	135	135	mA	3, 13
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	65	60	50	45	40	40	mA	13
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	6	6	6	6	6	7	mA	13

DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP versions only)

DESCRIPTION	**CONDITIONS**		**SYMBOL**	**MAX**	**UNITS**	**NOTES**
Data Retention Current	$\overline{CE}$ ≥ (V_{CC} -0.2V) V_{IN} ≥ (V_{CC} -0.2V) or ≤ 0.2V	V_{CC} = 2V	I_{CCDR}	400	µA	
		V_{CC} = 3V	I_{CCDR}	600	µA	
Data Retention Current LP version	$\overline{CE}$ ≥ (V_{CC} -0.2V)	V_{CC} = 2V	I_{CCDR}	400	µA	
		V_{CC} = 3V	I_{CCDR}	600	µA	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

Refer to commercial temperature timing parameters for specifications not listed here.
(Notes 5, 13) (-40°C ≤ T_A ≤ 85°C)

DESCRIPTION		-12		-15		-20		-25		-35			
	SYM	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ Cycle													
Output hold from address change	^tOH	2		2		2		2		2		ns	
Chip Enable to output in Low-Z	^tLZCE	2		2		2		2		2		ns	7

AUTOMOTIVE AND EXTENDED TEMPERATURE SPECIFICATIONS (AT AND XT)

The following specifications are to be used for Automotive Temperature (AT) and Extended Temperature (XT) MT5C2561 SRAMs.
(-40°C ≤ T_A ≤ 125°C - AT) (-55°C ≤ T_A ≤ 125°C - XT)

			MAX						
DESCRIPTION	**CONDITIONS**	**SYMBOL**	**-12**	**-15**	**-20**	**-25**	**-35**	**UNITS**	**NOTES**
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	180	155	140	135	135	mA	3, 13
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	60	50	45	40	40	mA	13
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	7	7	7	7	7	mA	13

DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP versions only)

DESCRIPTION	**CONDITIONS**		**SYMBOL**	**MAX**	**UNITS**	**NOTES**
Data Retention Current	$\overline{CE}$ ≥ (V_{CC} -0.2V) V_{IN} ≥ (V_{CC} -0.2V) or ≤ 0.2V	V_{CC} = 2V	I_{CCDR}	500	µA	
		V_{CC} = 3V	I_{CCDR}	800	µA	
Data Retention Current LP version	$\overline{CE}$ ≥ (V_{CC} -0.2V)	V_{CC} = 2V	I_{CCDR}	500	µA	
		V_{CC} = 3V	I_{CCDR}	800	µA	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

Refer to commercial temperature timing parameters for specifications not listed here.
(Notes 5, 13) (-40°C ≤ T_A ≤ 125°C; -55°C ≤ T_A ≤ 125°C; V_{CC} = 5V ± 10%)

DESCRIPTION		-12		-15		-20		-25		-35			
	SYM	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ Cycle													
Output hold from address change	^tOH	2		2		2		2		2		ns	
Chip Enable to output in Low-Z	^tLZCE	2		2		2		2		2		ns	7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

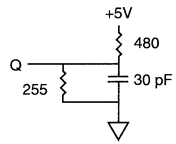


Fig. 1 OUTPUT LOAD EQUIVALENT

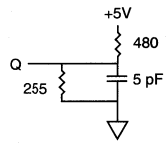


Fig. 2 OUTPUT LOAD EQUIVALENT

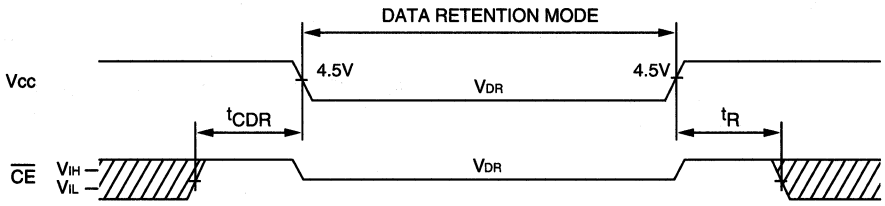
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE, and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Typical values are measured at 5V, 25°C and 15ns cycle time.
14. Typical currents are measured at 25°C.

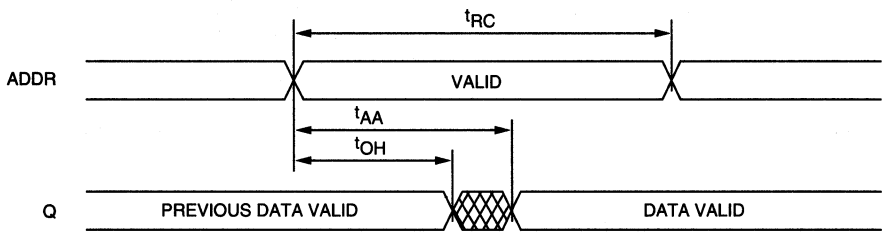
DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP versions only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2			V	
Data Retention Current L version	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	ICCDR		175	300	µA	14
		Vcc = 3V	ICCDR		250	500	µA	14
Data Retention Current LP version	$\overline{CE}$ ≥ (Vcc -0.2V)	Vcc = 2V	ICCDR		175	300	µA	14
		Vcc = 3V	ICCDR		250	500	µA	14
Chip Deselect to Data Retention Time			^{t}CDR	0			ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

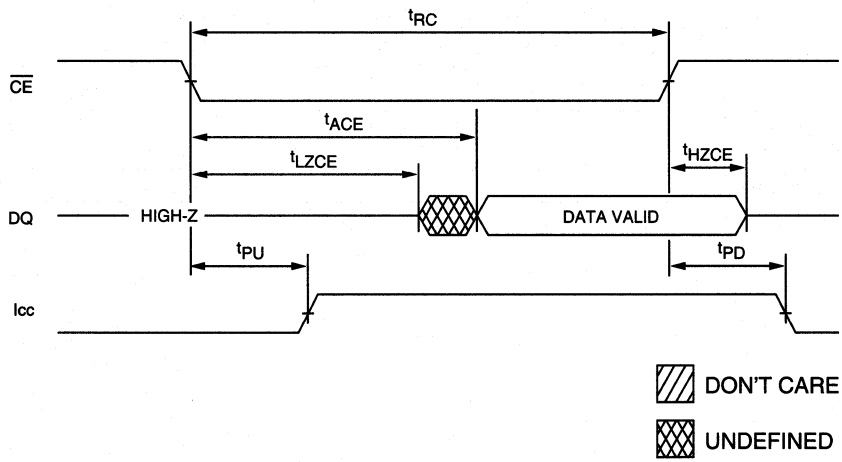
LOW Vcc DATA RETENTION WAVEFORM



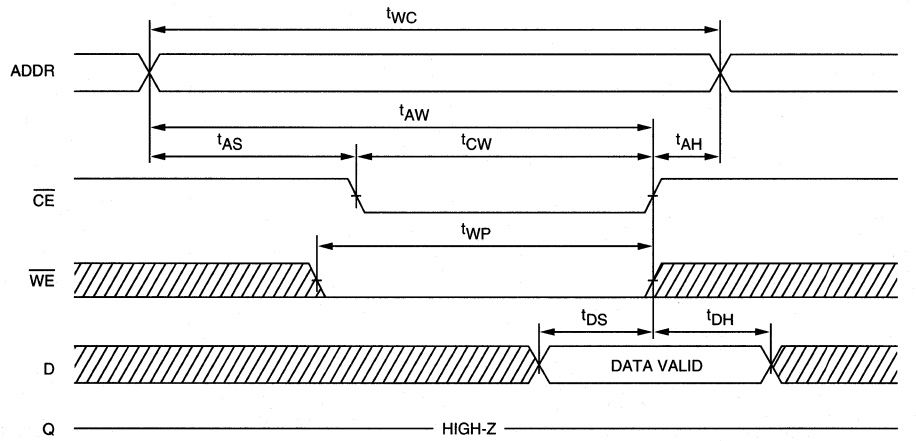
READ CYCLE NO. 1 [8, 9]



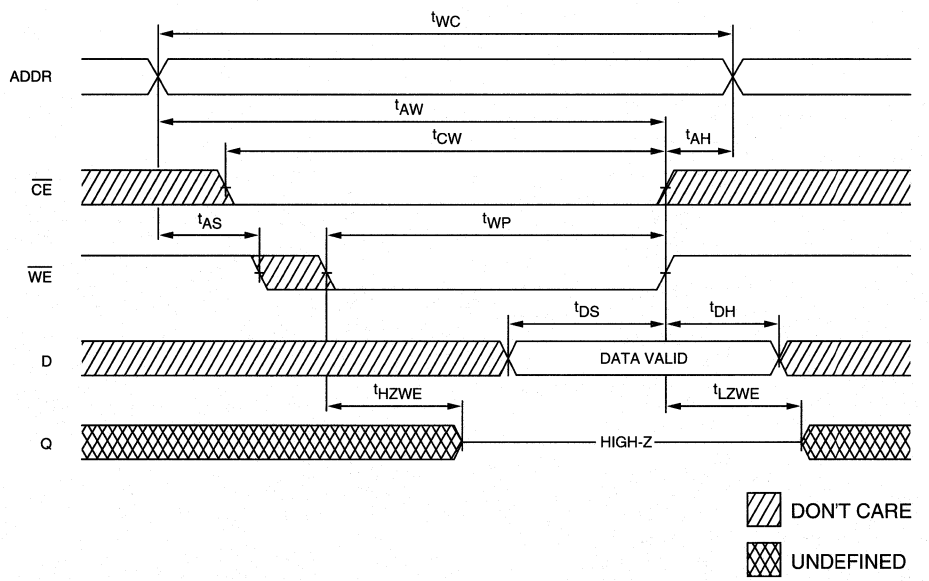
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)



WRITE CYCLE NO. 2 [7, 12]
(Write Enable Controlled)



SRAM

1 MEG x 1 SRAM

FEATURES

- High speed: 12, 15, 17, 20, 25 and 35
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ option
- All inputs and outputs are TTL-compatible

OPTIONS MARKING

- Timing

12ns access	-12
15ns access	-15
17ns access	-17
20ns access	-20
25ns access	-25
35ns access	-35

- Packages

Plastic DIP (400 mil)	None
Plastic SOJ (400 mil)	DJ
Plastic SOJ (300 mil)	SJ

- 2V data retention — L
- 2V data retention, low power — LP
- Temperature

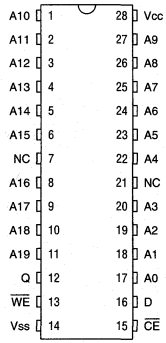
Commercial	(0°C to +70°C)	None
Industrial	(-40°C to +85°C)	IT
Automotive	(-40°C to +125°C)	AT
Extended	(-55°C to +125°C)	XT

- Part Number Example: MT5C1001DJ-20 IT

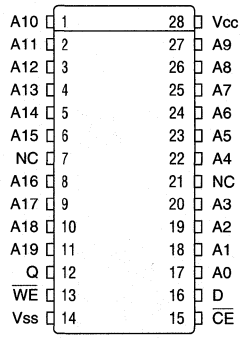
NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

28-Pin DIP
(SA-5)



28-Pin SOJ
(SD-2)
(SD-3)



GENERAL DESCRIPTION

The MT5C1001 is organized as a 1,048,576 x 1 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

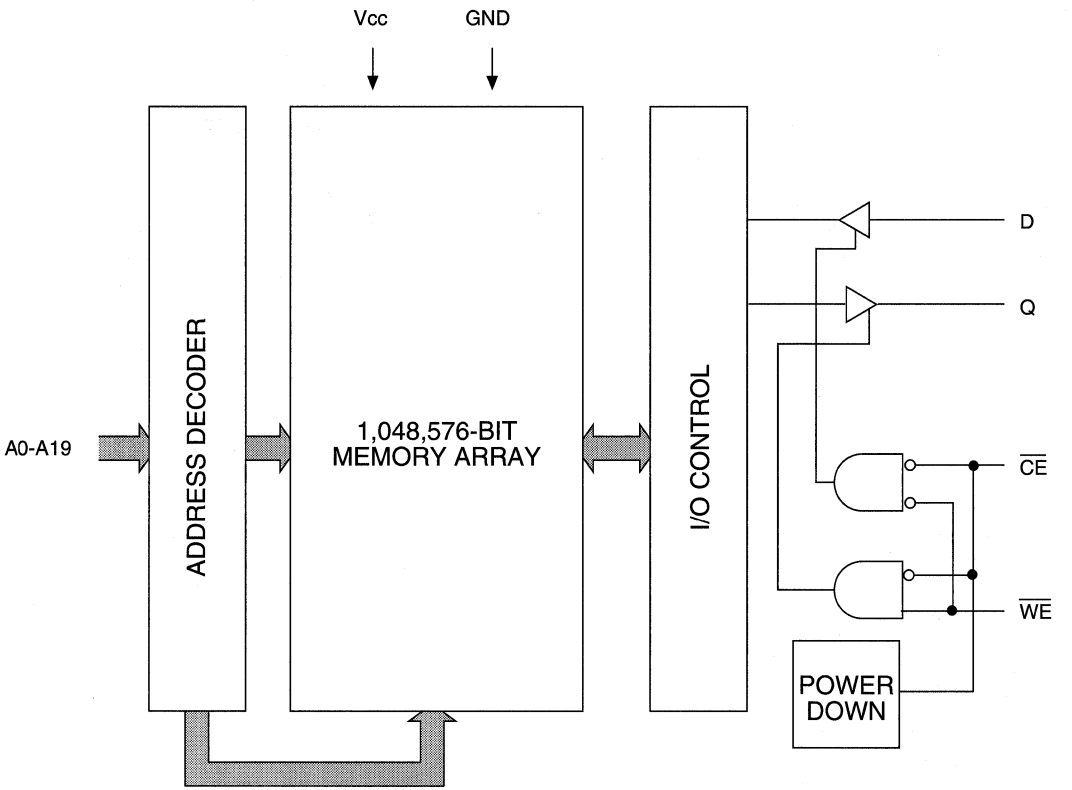
For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) capability. This enhancement can place the outputs in High-Z for additional flexibility in system design. The x1 configuration features separate data input and output.

Writing to this device is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH while $\overline{CE}$ goes LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

The "L" and "LP" versions each provide a 70 percent reduction in CMOS standby current (I_{SB2}) over the standard version. The LP version also provides a 90 percent reduction in TTL standby current (I_{SB1}) through the use of gated inputs on the $\overline{WE}$ and address lines, which also facilitates the design of battery backed systems. That is, the gated inputs simplify the design effort and circuitry required to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL-compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	INPUT	OUTPUT	POWER
STANDBY	H	X	DON'T CARE	HIGH-Z	STANDBY
READ	L	H	DON'T CARE	Q	ACTIVE
WRITE	L	L	DATA-IN	HIGH-Z	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA
Voltage on Any Pin Relative to V_{SS} ..... -1V to V_{CC} +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

				MAX							
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-12	-15	-17	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	95	190	165	155	140	125	115	mA	3, 13
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	17	45	40	40	35	30	25	mA	13
	LP version only	I_{SB1}	1.3	3	3	3	3	3	3	mA	13
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ Vss +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	0.4	5	5	5	5	5	5	mA	13
	L and LP versions only	I_{SB2}	0.3	1.5	1.5	1.5	1.5	1.5	1.5	mA	13

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	8	pF	4
Output Capacitance	V_{CC} = 5V	C_O	8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION	SYM	-12		-15		-17		-20		-25		-35		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
READ Cycle															
READ cycle time	^tRC	12		15		17		20		25		35		ns	
Address access time	^tAA		12		15		17		20		25		35	ns	
Chip Enable access time	^tACE		12		15		17		20		25		35	ns	
Output hold from address change	^tOH	3		3		3		3		5		5		ns	
Chip Enable to output in Low-Z	^tLZCE	3		5		5		5		5		5		ns	7
Chip disable to output in High-Z	^tHZCE		5		6		7		8		10		15	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		0		0		ns	
Chip disable to power-down time	^tPD		12		15		17		20		25		35	ns	
WRITE Cycle															
WRITE cycle time	^tWC	12		15		17		20		25		35		ns	
Chip Enable to end of write	^tCW	8		10		12		12		15		20		ns	
Address valid to end of write	^tAW	8		10		12		12		15		20		ns	
Address setup time	^tAS	0		0		0		0		0		0			
Address hold from end of write	^tAH	0		0		0		0		0		0		ns	
WRITE pulse width	^tWP	8		9		12		12		15		20		ns	
Data setup time	^tDS	6		7		8		8		10		15		ns	
Data hold time	^tDH	0		0		0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	3		3		3		3		3		3		ns	7
Write Enable to output in High-Z	^tHZWE		5		6		7		8		10		15	ns	6, 7

INDUSTRIAL TEMPERATURE SPECIFICATIONS (IT)

The following specifications are to be used for Industrial Temperature (IT) MT5C1001 SRAMs.
(-40°C ≤ T_A ≤ 85°C)

				MAX					
DESCRIPTION	**CONDITIONS**	**SYMBOL**	**TYP**	**-20**	**-25**	**-35**	**-45**	**UNITS**	**NOTES**
Power Supply Current: Operating	CE2 ≥ V_{IH}; $\overline{CE1}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	95	150	135	125	120	mA	3, 13
Power Supply Current: Standby	CE2 ≤ V_{IH} or $\overline{CE1}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	17	35	30	25	25	mA	13
	CE2 ≤ V_{SS} +0.2V; $\overline{CE1}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	0.4	5	5	5	5	mA	13
L version only	CE2 ≤ V_{SS} +0.2V; $\overline{CE1}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	0.3	2	2	2	2	mA	13

DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	**CONDITIONS**		**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**NOTES**
Data Retention Current	$\overline{CE1}$ ≥ (V_{CC} -0.2V) or CE2 ≤ (V_{SS} +0.2V) V_{IN} ≥ (V_{CC} -0.2V) or ≤ 0.2V	V_{CC} = 2V	I_{CCDR}		35	170	µA	14
		V_{CC} = 3V	I_{CCDR}		60	325	µA	14

AUTOMOTIVE AND EXTENDED TEMPERATURE SPECIFICATIONS (AT AND XT)

The following specifications are to be used for Automotive Temperature (AT) and Extended Temperature (XT) MT5C1001 SRAMs.
(-40°C ≤ T_A ≤ 125°C - AT) (-55°C ≤ T_A ≤ 125°C - XT)

				MAX					
DESCRIPTION	**CONDITIONS**	**SYMBOL**	**TYP**	**-20**	**-25**	**-35**	**-45**	**UNITS**	**NOTES**
Power Supply Current: Operating	CE2 ≥ V_{IH}; $\overline{CE1}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	95	150	135	125	120	mA	3, 13
Power Supply Current: Standby	CE2 ≤ V_{IH} or $\overline{CE1}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	17	45	40	35	32	mA	13
	CE2 ≤ V_{SS} +0.2V; $\overline{CE1}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	0.4	7	7	7	7	mA	13
L version only	CE2 ≤ V_{SS} +0.2V; $\overline{CE1}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	0.3	5	5	5	5	mA	13

DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	**CONDITIONS**		**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**NOTES**
Data Retention Current	$\overline{CE1}$ ≥ (V_{CC} -0.2V) or CE2 ≤ (Vss +0.2V) V_{IN} ≥ (V_{CC} -0.2V) or ≤ 0.2V	V_{CC} = 2V	I_{CCDR}		35	1,000	µA	14
		V_{CC} = 3V	I_{CCDR}		60	1,500	µA	14

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

Refer to commercial temperature timing parameters for specifications not listed here.
(Notes 5, 14) (-40°C ≤ T_A ≤ 125°C; -55°C ≤ T_A ≤ 125°C; V_{CC} = 5V ±10%)

DESCRIPTION		-20		-25		-35		-45			
	SYM	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ Cycle											
Output hold from address change	^tOH	3		3		3		3		ns	
Chip Enable to output in Low-Z	^tLZCE	3		3		3		3		ns	7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

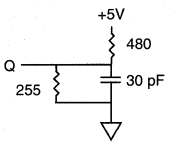


Fig. 1 OUTPUT LOAD EQUIVALENT

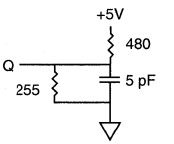


Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

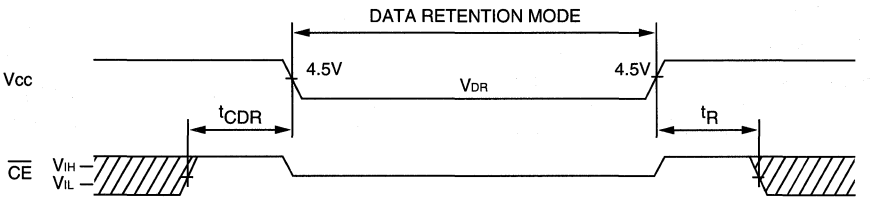
1. All voltages referenced to Vss (GND).
2. -3V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE, and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Typical values are measured at 5V, 25°C and 25ns cycle time.
14. Typical currents are measured at 25°C.

DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP versions only)

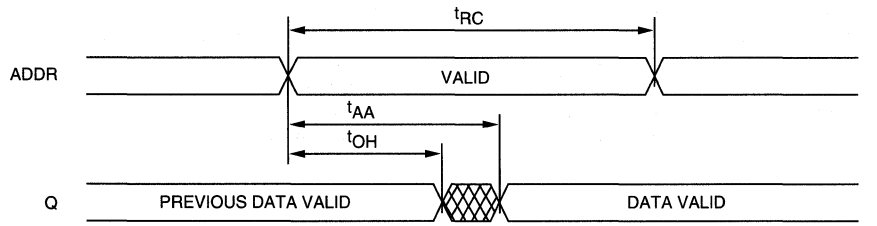
DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2			V	
Data Retention Current L version	$\overline{CE}$ ≥ (Vcc -0.2V)	Vcc = 2V	ICCDR		35	150	µA	14
	VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 3V	ICCDR		60	250	µA	14
		Vcc = 3V*	ICCDR		30	100	µA	14
Data Retention Current LP version	$\overline{CE}$ ≥ (Vcc -0.2V)	Vcc = 2V	ICCDR		35	150	µA	14
		Vcc = 3V	ICCDR		60	250	µA	14
Chip Deselect to Data Retention Time			^{t}CDR	0			ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

*Advance

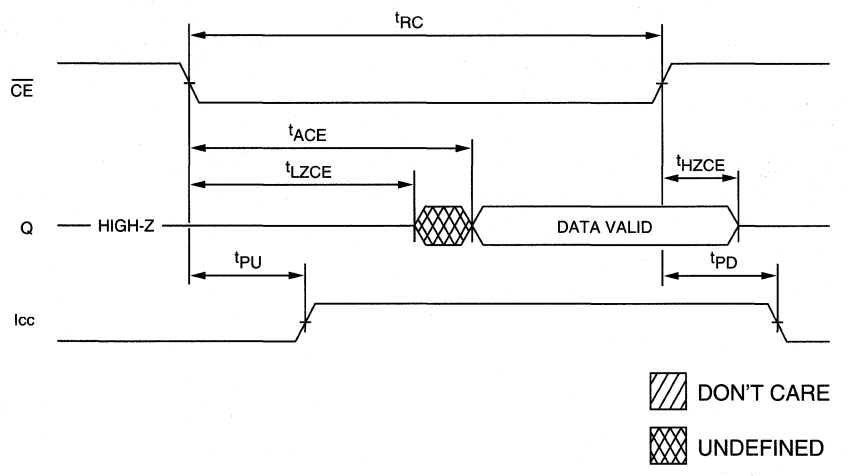
LOW Vcc DATA RETENTION WAVEFORM



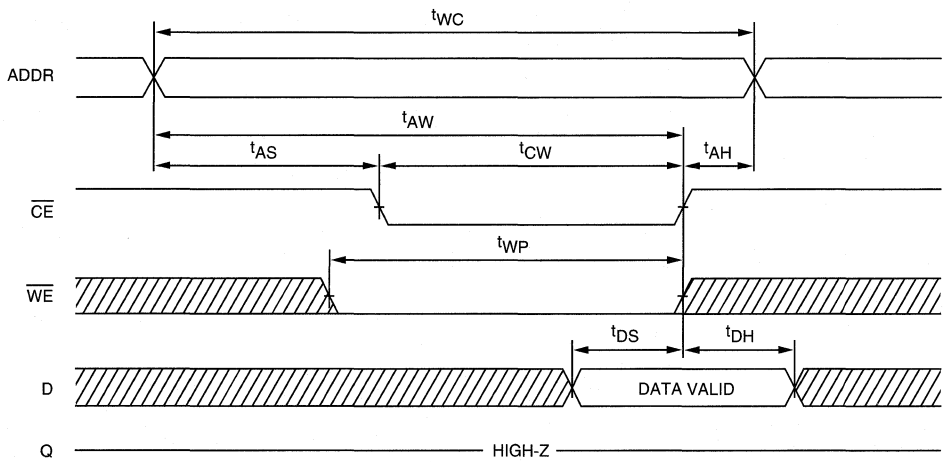
READ CYCLE NO. 1 [8, 9]



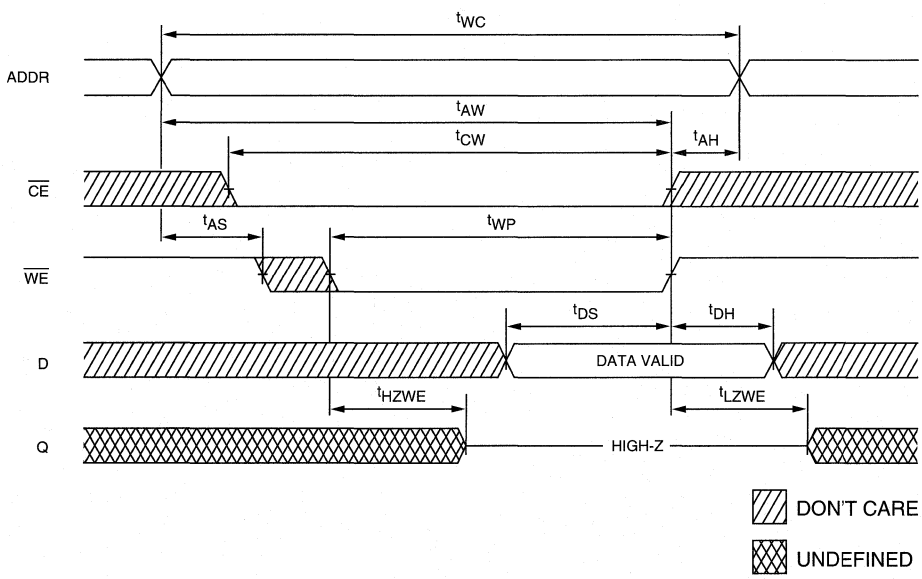
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)



WRITE CYCLE NO. 2 [7, 12]
(Write Enable Controlled)



SRAM

4K x 4 SRAM

FEATURES

- High speed: 9, 10, 12, 15, 20 and 25ns
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ option
- All inputs and outputs are TTL-compatible

OPTIONS

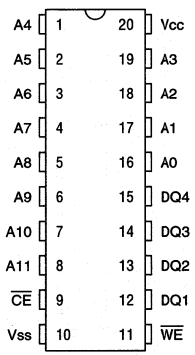
	MARKING
• Timing	
9ns access	- 9
10ns access	-10
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
• Packages	
Plastic DIP (300 mil)	None
Plastic SOJ (300 mil)	DJ
• 2V data retention	L
• Temperature	
Commercial (0°C to +70°C)	None
Industrial (-40°C to +85°C)	IT
Automotive (-40°C to +125°C)	AT
Extended (-55°C to +125°C)	XT

- Part Number Example: MT5C1604DJ-10 L

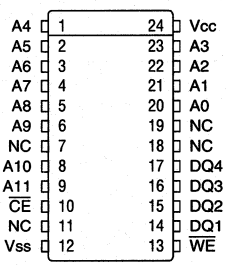
NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

20-Pin DIP
(SA-1)



24-Pin SOJ
(SD-1)



GENERAL DESCRIPTION

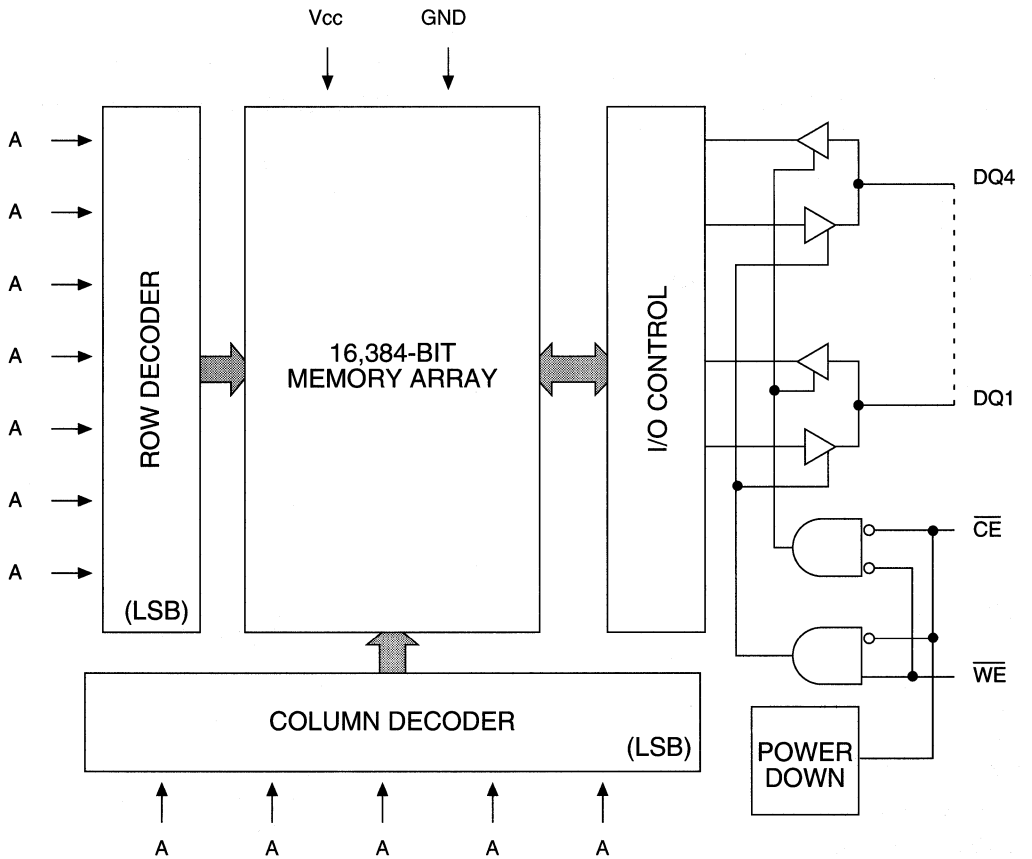
The MT5C1604 is organized as a 4,096 x 4 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) with all organizations. This enhancement can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL-compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	H	X	HIGH-Z	STANDBY
READ	L	H	Q	ACTIVE
WRITE	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA
Voltage on Any Pin Relative to V_{SS} ..... -1V to V_{CC} +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; V_{CC} = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

				MAX							
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-9	-10	-12	-15	-20	-25	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	125	190	185	175	165	140	130	mA	3, 13
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	22	60	50	45	40	35	35	mA	13
	$\overline{CE} \ge V_{CC}$ -0.2V; V_{CC} = MAX $V_{IN} \le V_{SS}$ +0.2V or $V_{IN} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	0.5	3	3	3	3	3	5	mA	13

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	5	pF	4
Output Capacitance	V_{CC} = 5V	C_O	7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

DESCRIPTION		-9		-10		-12		-15		-20		-25			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle															
READ cycle time	^tRC	9		10		12		15		20		25		ns	
Address access time	^tAA		9		10		12		15		20		25	ns	
Chip Enable access time	^tACE		9		9		10		12		15		20	ns	
Output hold from address change	^tOH	3		3		3		3		3		3		ns	
Chip Enable to output in Low-Z	^tLZCE	2		2		2		2		2		2		ns	7, 14
Chip disable to output in High-Z	^tHZCE		5		5		6		7		8		8	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		0		0		ns	
Chip disable to power-down time	^tPD		9		10		12		15		20		25	ns	
WRITE Cycle															
WRITE cycle time	^tWC	9		10		12		15		20		25		ns	
Chip Enable to end of write	^tCW	7		8		10		12		15		20		ns	
Address valid to end of write	^tAW	7		8		10		12		15		20		ns	
Address setup time	^tAS	0		0		0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		0		0		ns	
WRITE pulse width	$^tWP1$	6		7		8		10		12		15		ns	
WRITE pulse width	$^tWP2$	8		9		10		14		18		20		ns	
Data setup time	^tDS	5		6		7		8		9		10		ns	
Data hold time	^tDH	1		1		1		1		1		1		ns	
Write disable to output in Low-Z	^tLZWE	2		2		2		2		2		2		ns	7
Write Enable to output in High-Z	^tHZWE		4		5		5		6		8		8	ns	6, 7

INDUSTRIAL TEMPERATURE SPECIFICATIONS (IT)

The following specifications are to be used for Industrial Temperature (IT) MT5C1604 SRAMs.
(-40°C ≤ T_A ≤ 85°C)

			MAX						
DESCRIPTION	**CONDITIONS**	**SYMBOL**	**-10**	**-12**	**-15**	**-20**	**-25**	**UNITS**	**NOTES**
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	195	185	175	150	140	mA	3, 13
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	60	50	45	40	40	mA	13
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	5	5	5	5	5	mA	13

DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	**CONDITIONS**		**SYMBOL**	**TYP**	**MAX**	**UNITS**	**NOTES**
Data Retention Current	$\overline{CE}$ ≥ (V_{CC} -0.2V) V_{IN} ≥ (V_{CC} -0.2V) or ≤ 0.2V	V_{CC} = 2V	I_{CCDR}	130	300	µA	14
		V_{CC} = 3V	I_{CCDR}	210	550	µA	14

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

Refer to commercial temperature timing parameters for specifications not listed here.
(Notes 5, 14) (-40°C ≤ T_A ≤ 85°C)

DESCRIPTION		-12		-15		-20		-25			
	SYM	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ Cycle											
Output hold from address change	^tOH	2		2		2		2		ns	
Chip Enable to output in Low-Z	^tLZCE	1		1		1		1		ns	7
WRITE Cycle											
Write disable to output in Low-Z	^tLZWE	1		1		1		1		ns	7

AUTOMOTIVE AND EXTENDED TEMPERATURE SPECIFICATIONS (AT AND XT)

The following specifications are to be used for Automotive Temperature (AT) and Extended Temperature (XT) MT5C1604 SRAMs. (-40°C ≤ T_A ≤ 125°C - AT) (-55°C ≤ T_A ≤ 125°C - XT)

			MAX					
DESCRIPTION	**CONDITIONS**	**SYMBOL**	**-12**	**-15**	**-20**	**-25**	**UNITS**	**NOTES**
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	185	175	150	140	mA	3, 13
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	50	45	40	40	mA	13
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	5	5	5	5	mA	13

DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	**CONDITIONS**		**SYMBOL**	**TYP**	**MAX**	**UNITS**	**NOTES**
Data Retention Current	$\overline{CE}$ ≥ (V_{CC} -0.2V) V_{IN} ≥ (V_{CC} -0.2V) or ≤ 0.2V	V_{CC} = 2V	I_{CCDR}	130	300	µA	14
		V_{CC} = 3V	I_{CCDR}	210	550	µA	14

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

Refer to commercial temperature timing parameters for specifications not listed here.
(Notes 5, 14) (-40°C ≤ T_A ≤ 125°C; -55°C ≤ T_A ≤ 125°C; V_{CC} = 5V ±10%)

DESCRIPTION		-12		-15		-20		-25			
	SYM	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ Cycle											
Output hold from address change	^tOH	2		2		2		2		ns	
Chip Enable to output in Low-Z	^tLZCE	1		1		1		1		ns	7
WRITE Cycle											
Write disable to output in Low-Z	^tLZWE	1		1		1		1		ns	7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

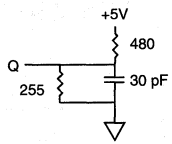


Fig. 1 OUTPUT LOAD EQUIVALENT

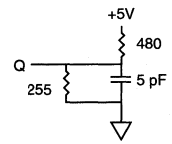


Fig. 2 OUTPUT LOAD EQUIVALENT

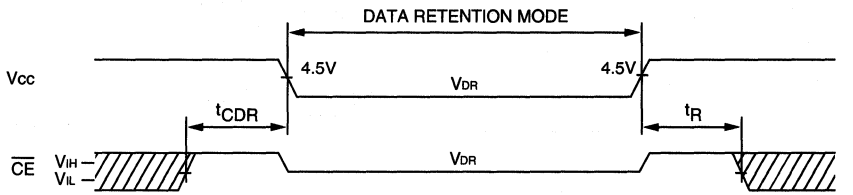
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Typical values are measured at 5V, 25°C and 15ns cycle time.
14. Typical currents are measured at 25°C.

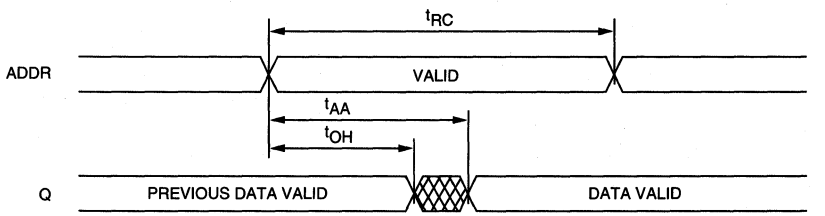
DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2			V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	ICCDR		130	300	µA	14
		Vcc = 3V	ICCDR		210	400	µA	14
Chip Deselect to Data Retention Time			^{t}CDR	0			ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 10

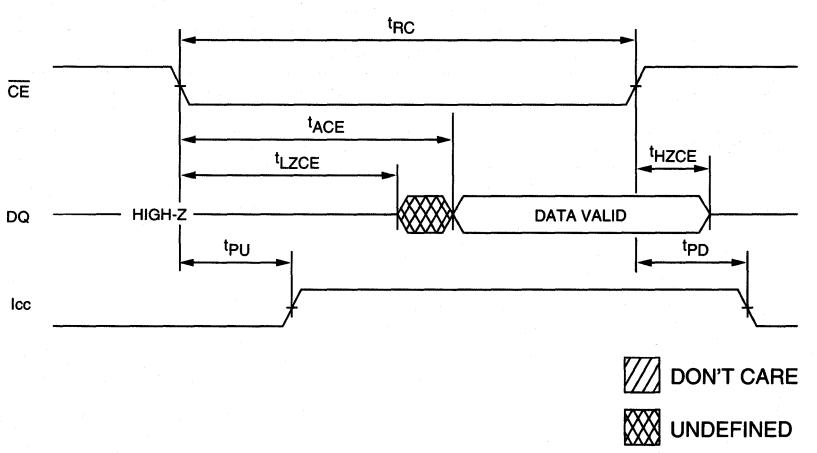
LOW Vcc DATA RETENTION WAVEFORM



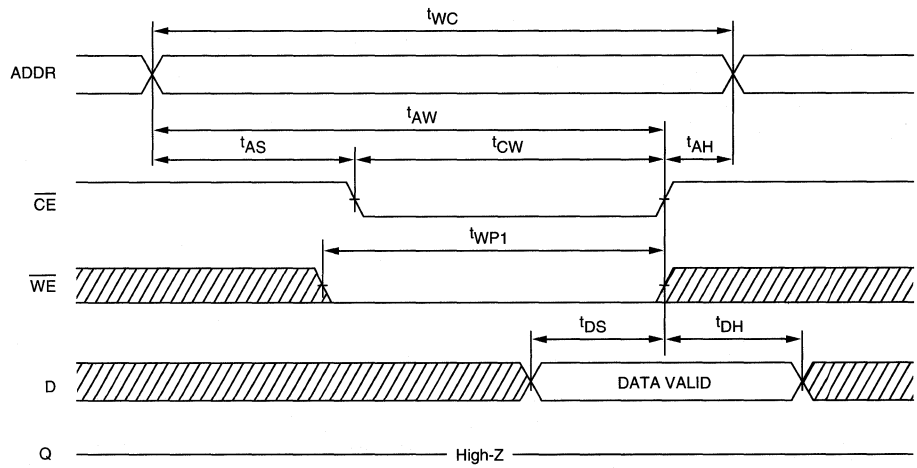
READ CYCLE NO. 1 [8, 9]



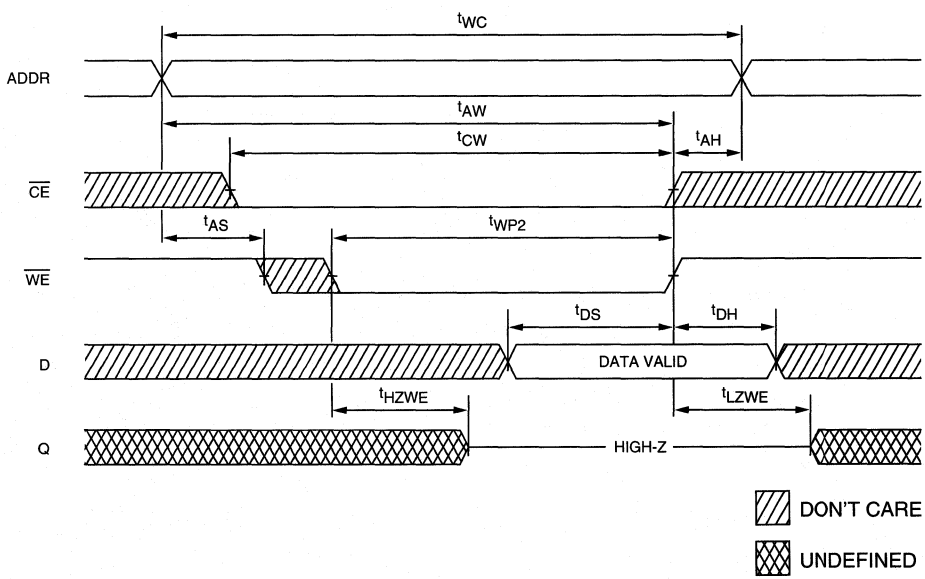
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1
(Chip Enable Controlled)



WRITE CYCLE NO. 2 [7, 12]
(Write Enable Controlled)



SRAM

4K x 4 SRAM

WITH OUTPUT ENABLE

FEATURES

- High speed: 9, 10, 12, 15, 20 and 25ns
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- All inputs and outputs are TTL-compatible

OPTIONS — MARKING

- Timing

9ns access	- 9
10ns access	-10
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25

- Packages

Plastic DIP (300 mil)	None
Plastic SOJ (300 mil)	DJ

- 2V data retention — L

- Temperature

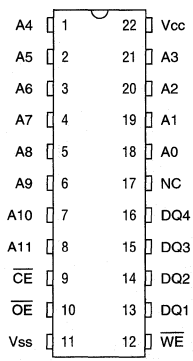
Commercial	(0°C to +70°C)	None
Industrial	(-40°C to +85°C)	IT
Automotive	(-40°C to +125°C)	AT
Extended	(-55°C to +125°C)	XT

- Part Number Example: MT5C1605DJ-15 IT

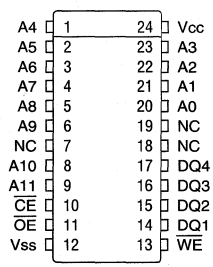
NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

22-Pin DIP
(SA-2)



24-Pin SOJ
(SD-1)



GENERAL DESCRIPTION

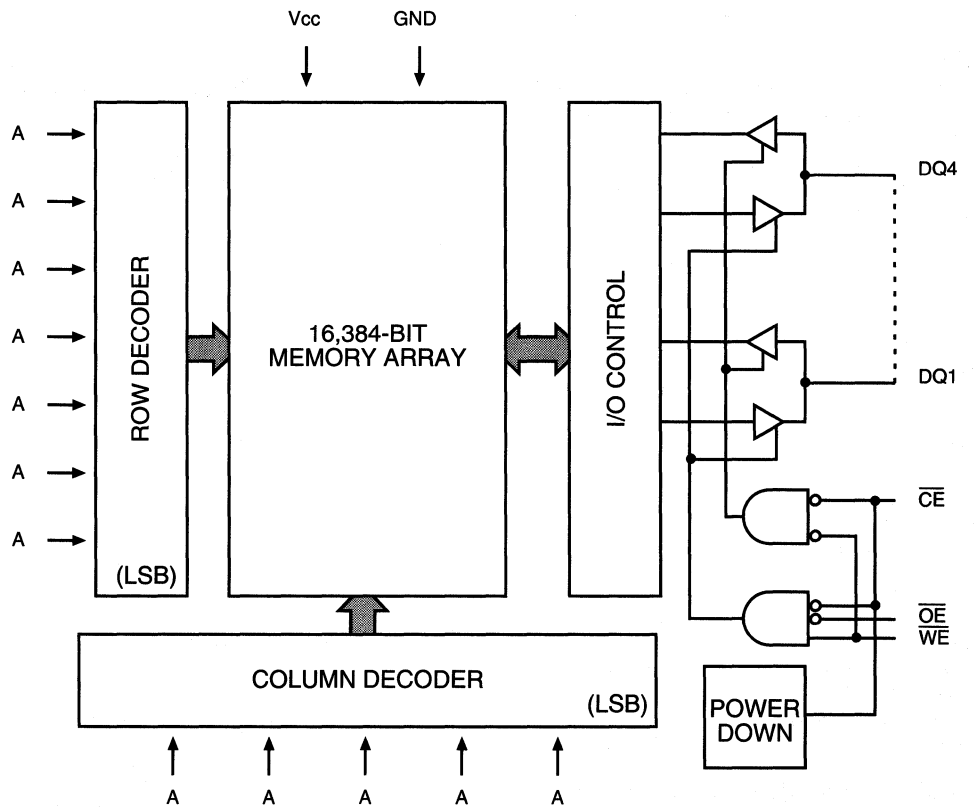
The MT5C1605 is organized as a 4,096 x 4 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) with this organization. This enhancement can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{OE}$ and $\overline{CE}$ go LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL-compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA
Voltage on Any Pin Relative to V_{SS} ..... -1V to V_{CC} +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

				MAX							
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-9	-10	-12	-15	-20	-25	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	125	190	185	175	165	140	130	mA	3, 13
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	22	60	50	45	40	35	35	mA	13
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	0.5	3	3	3	3	3	5	mA	13

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	5	pF	4
Output Capacitance	V_{CC} = 5V	C_O	7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION		-9		-10		-12		-15		-20		-25			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle															
READ cycle time	^tRC	9		10		12		15		20		25		ns	
Address access time	^tAA		9		10		12		15		20		25	ns	
Chip Enable access time	^tACE		9		9		10		12		15		20	ns	
Output hold from address change	^tOH	3		3		3		3		3		3		ns	
Chip Enable to output in Low-Z	^tLZCE	2		2		2		2		2		2		ns	7, 14
Chip disable to output in High-Z	^tHZCE		5		5		6		7		8		8	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		0		0		ns	
Chip disable to power-down time	^tPD		9		10		12		15		20		25	ns	
Output Enable access time	^tAOE		4.5		5		6		7		8		8	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		0		0		ns	
Output disable to output in High-Z	^tHZOE		4.5		5		5		6		7		8	ns	6
WRITE Cycle															
WRITE cycle time	^tWC	9		10		12		15		20		25		ns	
Chip Enable to end of write	^tCW	7		8		10		12		15		20		ns	
Address valid to end of write	^tAW	7		8		10		12		15		20		ns	
Address setup time	^tAS	0		0		0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		0		0		ns	
WRITE pulse width	$^tWP1$	6		7		8		10		12		15		ns	
WRITE pulse width	$^tWP2$	8		9		10		14		18		20		ns	
Data setup time	^tDS	5		6		7		8		9		10		ns	
Data hold time	^tDH	1		1		1		1		1		1		ns	
Write disable to output in Low-Z	^tLZWE	2		2		2		2		2		2		ns	7
Write Enable to output in High-Z	^tHZWE		4		5		5		6		8		8	ns	6, 7

INDUSTRIAL TEMPERATURE SPECIFICATIONS (IT)

The following specifications are to be used for Industrial Temperature (IT) MT5C1605 SRAMs.
(-40°C ≤ T_A ≤ 85°C)

			MAX						
DESCRIPTION	**CONDITIONS**	**SYMBOL**	**-10**	**-12**	**-15**	**-20**	**-25**	**UNITS**	**NOTES**
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	195	185	175	150	140	mA	3, 13
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	60	50	45	40	40	mA	13
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	5	5	5	5	5	mA	13

DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	**CONDITIONS**		**SYMBOL**	**TYP**	**MAX**	**UNITS**	**NOTES**
Data Retention Current	$\overline{CE}$ ≥ (V_{CC} -0.2V) V_{IN} ≥ (V_{CC} -0.2V) or ≤ 0.2V	V_{CC} = 2V	I_{CCDR}	130	300	µA	14
		V_{CC} = 3V	I_{CCDR}	210	550	µA	14

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

Refer to commercial temperature timing parameters for specifications not listed here.
(Notes 5, 14) (-40°C ≤ T_A ≤ 85°C)

DESCRIPTION		-12		-15		-20		-25			
	SYM	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ Cycle											
Output hold from address change	^tOH	2		2		2		2		ns	
Chip Enable to output in Low-Z	^tLZCE	1		1		1		1		ns	7
WRITE Cycle											
Write disable to output in Low-Z	^tLZWE	1		1		1		1		ns	7

AUTOMOTIVE AND EXTENDED TEMPERATURE SPECIFICATIONS (AT AND XT)

The following specifications are to be used for Automotive Temperature (AT) and Extended Temperature (XT) MT5C1605 SRAMs. (-40°C ≤ T_A ≤ 125°C - AT) (-55°C ≤ T_A ≤ 125°C - XT)

			MAX					
DESCRIPTION	**CONDITIONS**	**SYMBOL**	**-12**	**-15**	**-20**	**-25**	**UNITS**	**NOTES**
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	185	175	150	140	mA	3, 13
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	50	45	40	40	mA	13
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	5	5	5	5	mA	13

DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	**CONDITIONS**		**SYMBOL**	**TYP**	**MAX**	**UNITS**	**NOTES**
Data Retention Current	$\overline{CE}$ ≥ (V_{CC} -0.2V) V_{IN} ≥ (V_{CC} -0.2V) or ≤ 0.2V	V_{CC} = 2V	I_{CCDR}	130	300	µA	14
		V_{CC} = 3V	I_{CCDR}	210	550	µA	14

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

Refer to commercial temperature timing parameters for specifications not listed here.
(Notes 5, 14) (-40°C ≤ T_A ≤ 125°C; -55°C ≤ T_A ≤ 125°C; V_{CC} = 5V ±10%)

DESCRIPTION		-12		-15		-20		-25			
	SYM	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ Cycle											
Output hold from address change	^tOH	2		2		2		2		ns	
Chip Enable to output in Low-Z	^tLZCE	1		1		1		1		ns	7
WRITE Cycle											
Write disable to output in Low-Z	^tLZWE	1		1		1		1		ns	7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

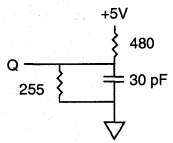


Fig. 1 OUTPUT LOAD EQUIVALENT

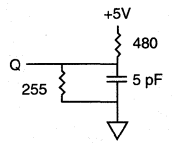


Fig. 2 OUTPUT LOAD EQUIVALENT

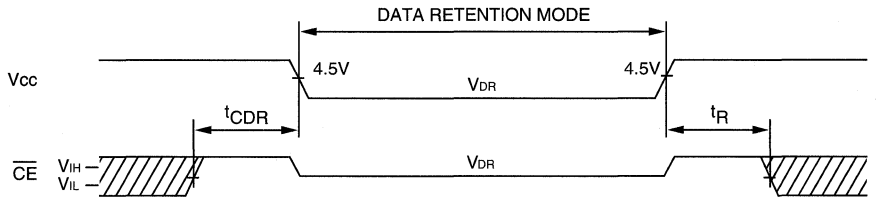
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZWE and ^{t}HZOE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Typical values are measured at 5V, 25°C and 15ns cycle time.
14. Typical currents are measured at 25°C.
15. Output enable ($\overline{OE}$) is inactive (HIGH).
16. Output enable ($\overline{OE}$) is active (LOW).

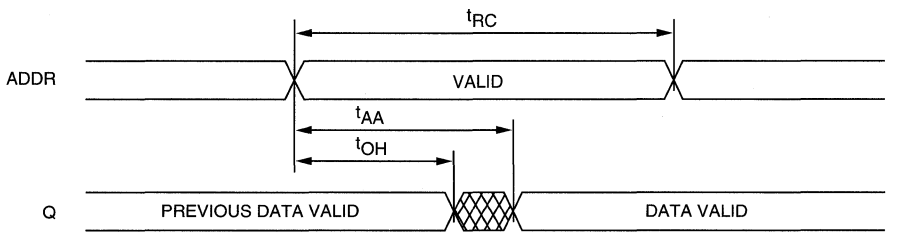
DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2			V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	ICCDR		130	300	µA	14
		Vcc = 3V	ICCDR		210	400	µA	14
Chip Deselect to Data Retention Time			^{t}CDR	0			ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

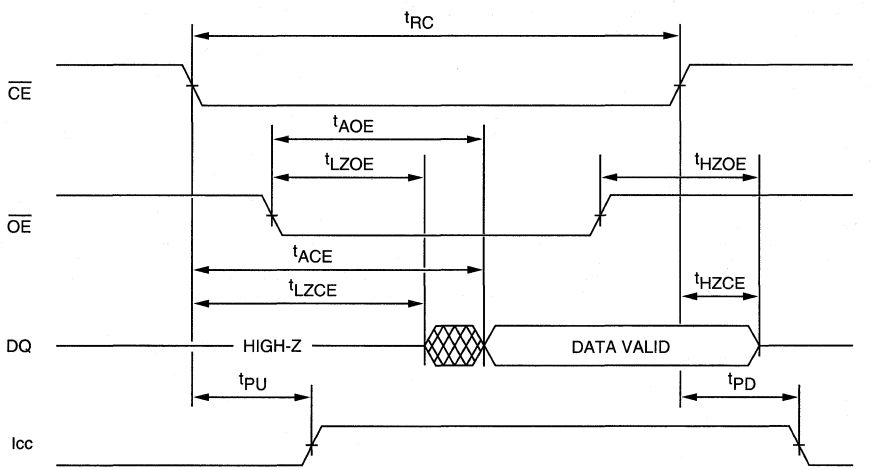
LOW Vcc DATA RETENTION WAVEFORM



READ CYCLE NO. 1 [8, 9]



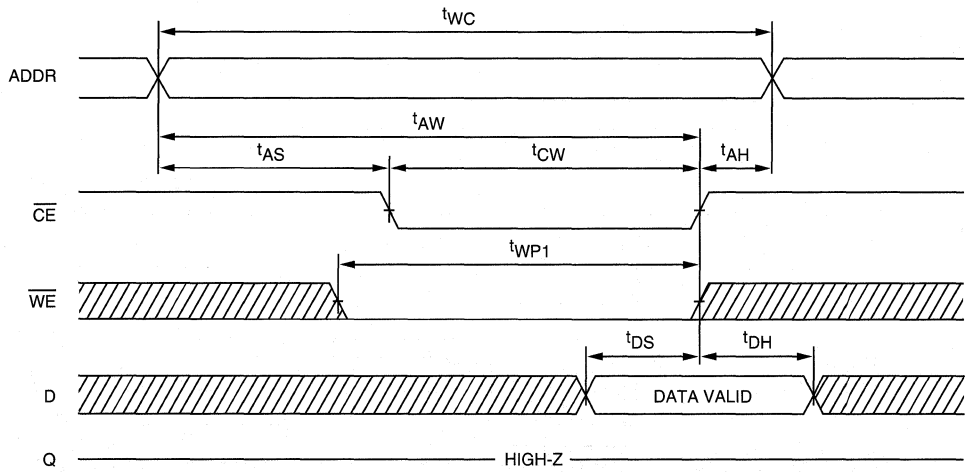
READ CYCLE NO. 2 [7, 8, 10]



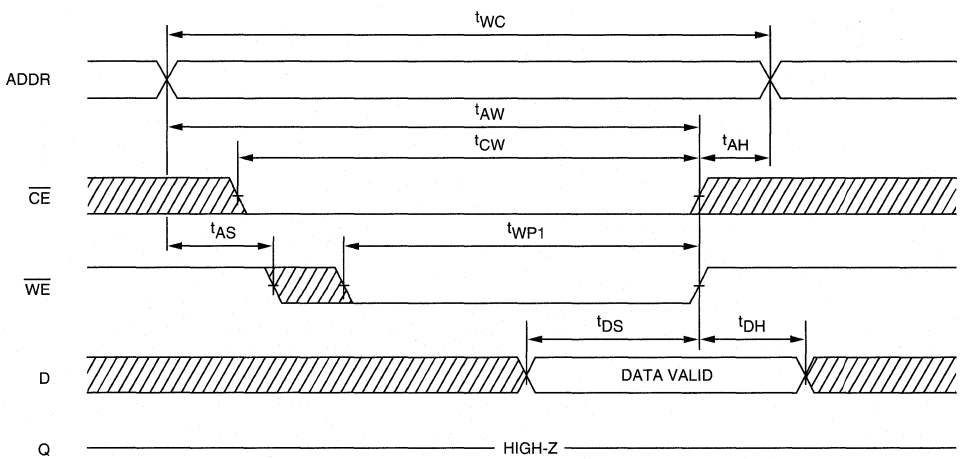
DON'T CARE

UNDEFINED

WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)



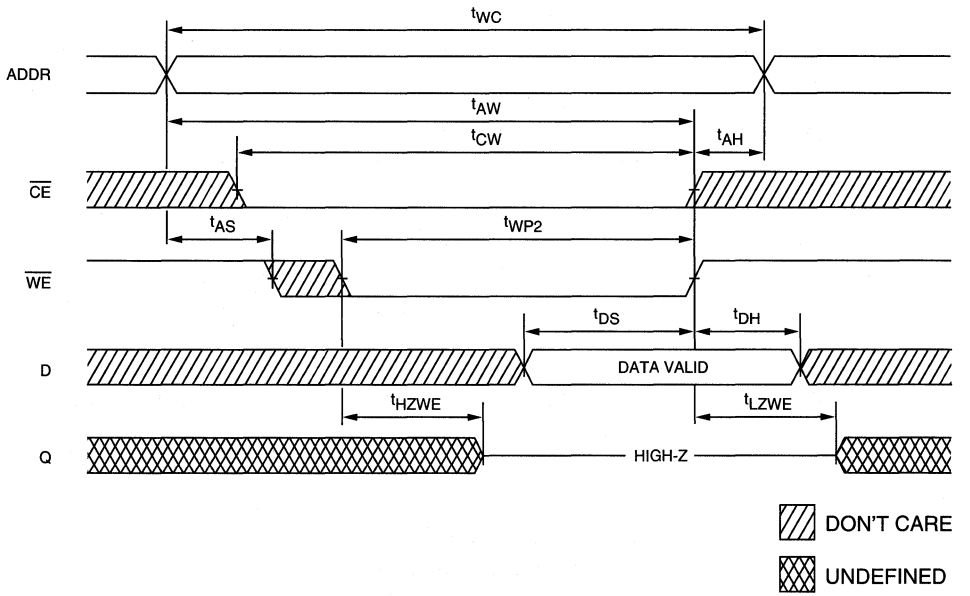
WRITE CYCLE NO. 2 [12, 15]
(Write Enable Controlled)



DON'T CARE

UNDEFINED

WRITE CYCLE NO. 3 [7, 12, 16]
(Write Enable Controlled)



SRAM

16K x 4 SRAM

FEATURES

- High speed: 9, 10, 12, 15, 20 and 25ns
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ option
- All inputs and outputs are TTL-compatible

OPTIONS

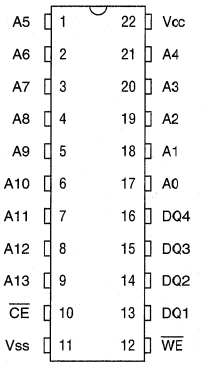
	MARKING
• Timing	
9ns access	- 9
10ns access	-10
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
• Packages	
Plastic DIP (300 mil)	None
Plastic SOJ (300 mil)	DJ
• 2V data retention	L
• Temperature	
Commercial (0°C to +70°C)	None
Industrial (-40°C to +85°C)	IT
Automotive (-40°C to +125°C)	AT
Extended (-55°C to +125°C)	XT

- Part Number Example: MT5C6404DJ-15 L

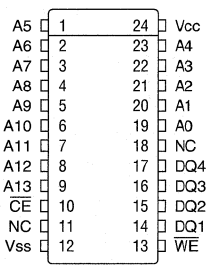
NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

22-Pin DIP
(SA-2)



24-Pin SOJ
(SD-1)



GENERAL DESCRIPTION

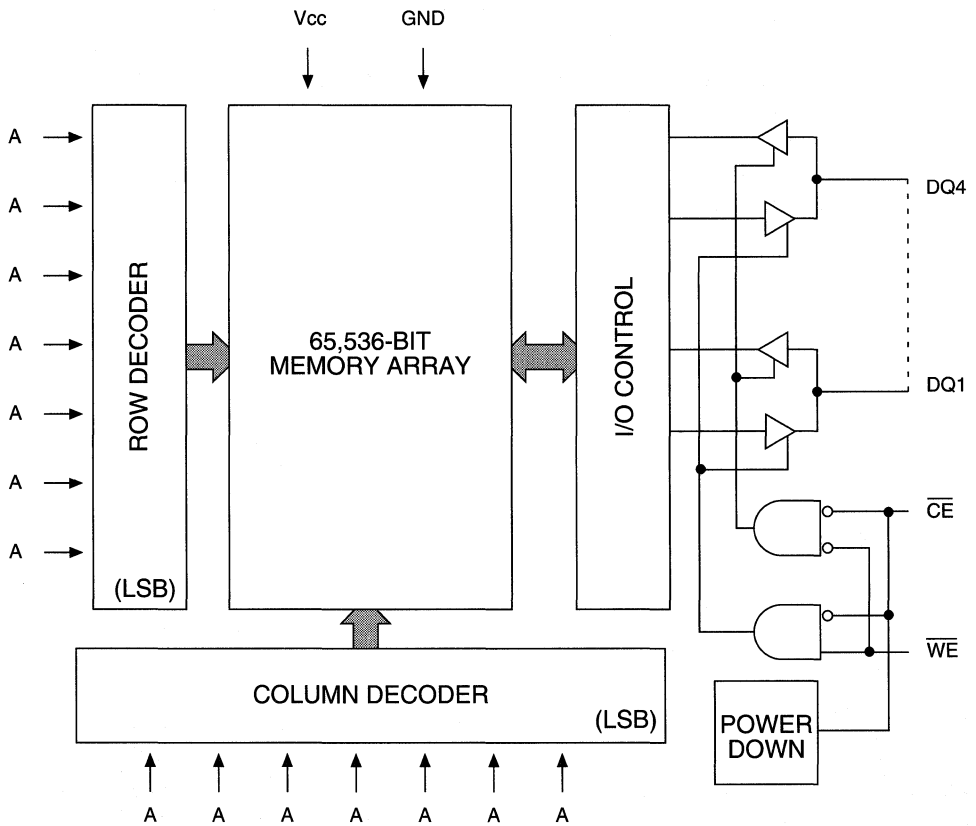
The MT5C6404 is organized as a 16,384 x 4 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) with all organizations. This enhancement can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL-compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	H	X	HIGH-Z	STANDBY
READ	L	H	Q	ACTIVE
WRITE	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA
Voltage on Any Pin Relative to V_{SS} ..... -1V to V_{CC} +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

				MAX							
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-9	-10	-12	-15	-20	-25	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	125	190	185	175	165	140	130	mA	3, 13
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	22	60	50	45	40	35	35	mA	13
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	0.5	3	3	3	3	3	5	mA	13

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	5	pF	4
Output Capacitance	V_{CC} = 5V	C_O	7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION		-9		-10		-12		-15		-20		-25			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle															
READ cycle time	^tRC	9		10		12		15		20		25		ns	
Address access time	^tAA		9		10		12		15		20		25	ns	
Chip Enable access time	^tACE		9		9		10		12		15		20	ns	
Output hold from address change	^tOH	3		3		3		3		3		3		ns	
Chip Enable to output in Low-Z	^tLZCE	2		2		2		2		2		2		ns	7, 14
Chip disable to output in High-Z	^tHZCE		5		5		6		7		8		8	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		0		0		ns	
Chip disable to power-down time	^tPD		9		10		12		15		20		25	ns	
WRITE Cycle															
WRITE cycle time	^tWC	9		10		12		15		20		25		ns	
Chip Enable to end of write	^tCW	7		8		10		12		15		20		ns	
Address valid to end of write	^tAW	7		8		10		12		15		20		ns	
Address setup time	^tAS	0		0		0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		0		0		ns	
WRITE pulse width	$^tWP1$	6		7		8		10		12		15		ns	
WRITE pulse width	$^tWP2$	8		9		10		14		18		20		ns	
Data setup time	^tDS	5		6		7		8		9		10		ns	
Data hold time	^tDH	1		1		1		1		1		1		ns	
Write disable to output in Low-Z	^tLZWE	2		2		2		2		2		2		ns	7
Write Enable to output in High-Z	^tHZWE		4		5		5		6		8		8	ns	6, 7

INDUSTRIAL TEMPERATURE SPECIFICATIONS (IT)

The following specifications are to be used for Industrial Temperature (IT) MT5C6404 SRAMs.
(-40°C ≤ T_A ≤ 85°C)

			MAX						
DESCRIPTION	**CONDITIONS**	**SYMBOL**	**-10**	**-12**	**-15**	**-20**	**-25**	**UNITS**	**NOTES**
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	195	185	175	150	140	mA	3, 13
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	60	50	45	40	40	mA	13
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	5	5	5	5	5	mA	13

DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	**CONDITIONS**		**SYMBOL**	**TYP**	**MAX**	**UNITS**	**NOTES**
Data Retention Current	$\overline{CE}$ ≥ (V_{CC} -0.2V) V_{IN} ≥ (V_{CC} -0.2V) or ≤ 0.2V	V_{CC} = 2V	I_{CCDR}	130	300	µA	14
		V_{CC} = 3V	I_{CCDR}	210	550	µA	14

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

Refer to commercial temperature timing parameters for specifications not listed here.
(Notes 5, 14) (-40°C ≤ T_A ≤ 85°C)

DESCRIPTION		-12		-15		-20		-25			
	SYM	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ Cycle											
Output hold from address change	^tOH	2		2		2		2		ns	
Chip Enable to output in Low-Z	^tLZCE	1		1		1		1		ns	7
WRITE Cycle											
Write disable to output in Low-Z	^tLZWE	1		1		1		1		ns	7

AUTOMOTIVE AND EXTENDED TEMPERATURE SPECIFICATIONS (AT AND XT)

The following specifications are to be used for Automotive Temperature (AT) and Extended Temperature (XT) MT5C6404 SRAMs. (-40°C ≤ T_A ≤ 125°C - AT) (-55°C ≤ T_A ≤ 125°C - XT)

			MAX					
DESCRIPTION	**CONDITIONS**	**SYMBOL**	**-12**	**-15**	**-20**	**-25**	**UNITS**	**NOTES**
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	185	175	150	140	mA	3, 13
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	50	45	40	40	mA	13
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	5	5	5	5	mA	13

DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	**CONDITIONS**		**SYMBOL**	**TYP**	**MAX**	**UNITS**	**NOTES**
Data Retention Current	$\overline{CE}$ ≥ (V_{CC} -0.2V) V_{IN} ≥ (V_{CC} -0.2V) or ≤ 0.2V	V_{CC} = 2V	I_{CCDR}	130	300	µA	14
		V_{CC} = 3V	I_{CCDR}	210	550	µA	14

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

Refer to commercial temperature timing parameters for specifications not listed here.
(Notes 5, 14) (-40°C ≤ T_A ≤ 125°C; -55°C ≤ T_A ≤ 125°C; V_{CC} = 5V ±10%)

DESCRIPTION		-12		-15		-20		-25			
	SYM	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ Cycle											
Output hold from address change	^tOH	2		2		2		2		ns	
Chip Enable to output in Low-Z	^tLZCE	1		1		1		1		ns	7
WRITE Cycle											
Write disable to output in Low-Z	^tLZWE	1		1		1		1		ns	7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3 ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

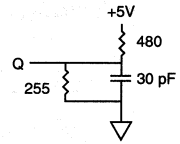


Fig. 1 OUTPUT LOAD EQUIVALENT

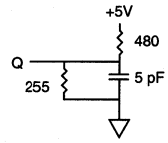


Fig. 2 OUTPUT LOAD EQUIVALENT

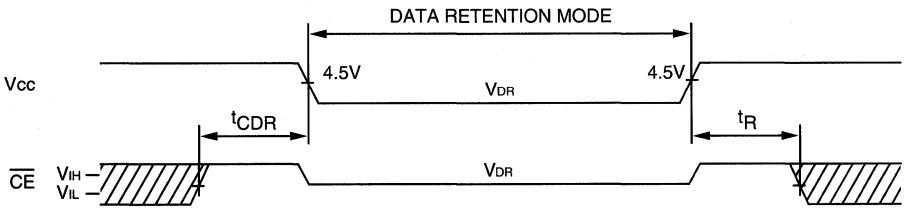
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Typical values are measured at 5V, 25°C and 15ns cycle time.
14. Typical currents are measured at 25°C.

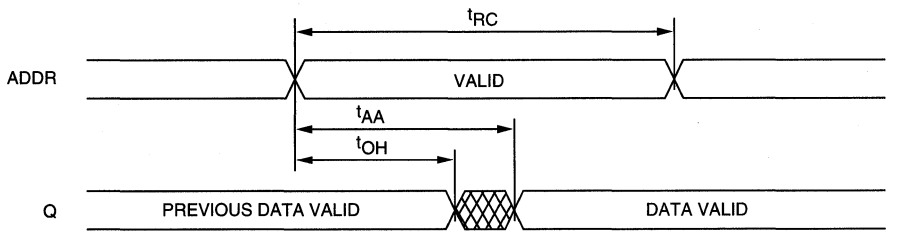
DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2			V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	ICCDR		130	300	µA	14
		Vcc = 3V	ICCDR		210	400	µA	14
Chip Deselect to Data Retention Time			^{t}CDR	0			ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

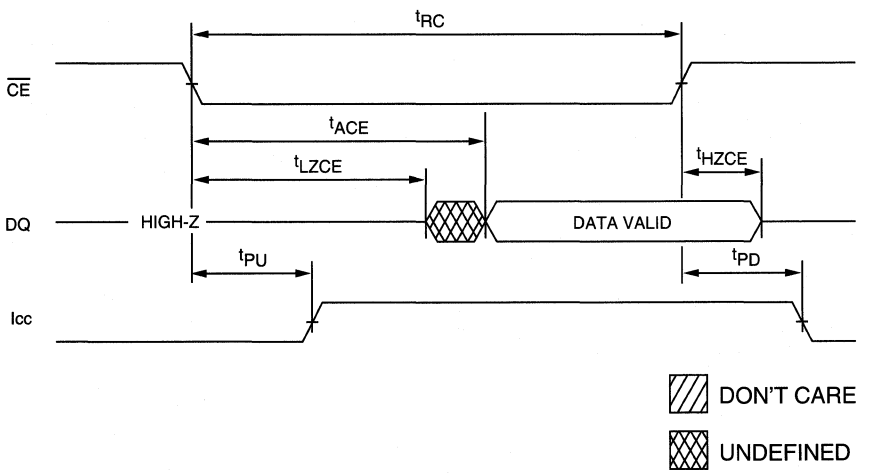
LOW Vcc DATA RETENTION WAVEFORM



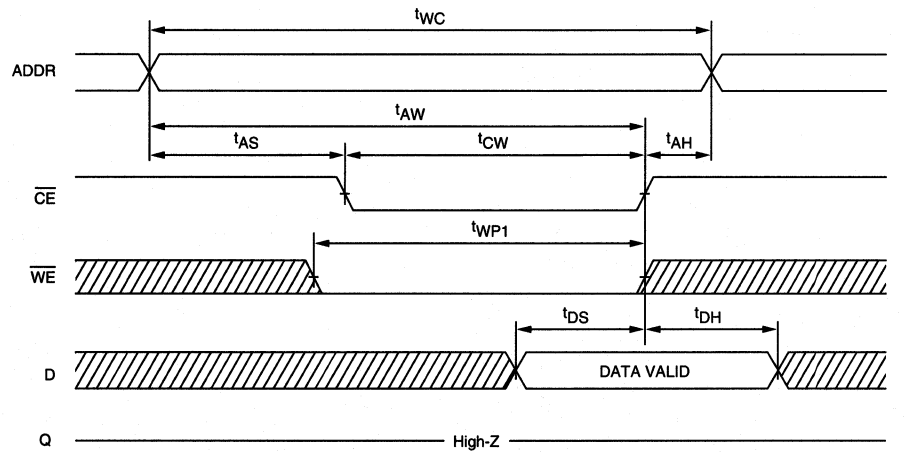
READ CYCLE NO. 1 [8, 9]



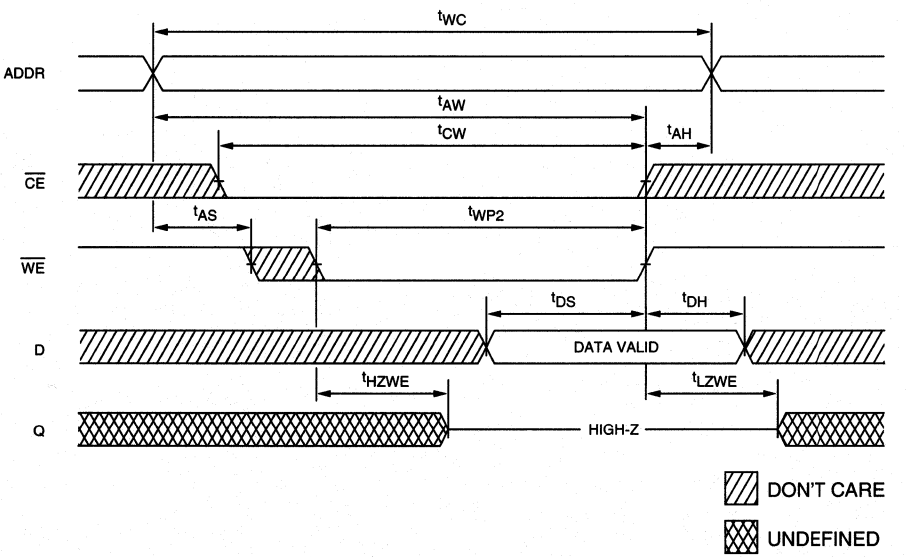
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1
(Chip Enable Controlled)



WRITE CYCLE NO. 2 [7, 12]
(Write Enable Controlled)



SRAM

16K x 4 SRAM

WITH OUTPUT ENABLE

FEATURES

- High speed: 9, 10, 12, 15, 20 and 25ns
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- All inputs and outputs are TTL-compatible

OPTIONS — MARKING

- Timing

9ns access	- 9
10ns access	-10
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25

- Packages

Plastic DIP (300 mil)	None
Plastic SOJ (300 mil)	DJ

- 2V data retention — L

- Temperature

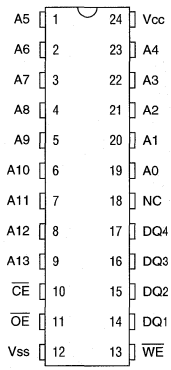
Commerical	(0°C to +70°C)	None
Industrial	(-40°C to +85°C)	IT
Automotive	(-40°C to +125°C)	AT
Extended	(-55°C to +125°C)	XT

- Part Number Example: MT5C6405DJ-15 L

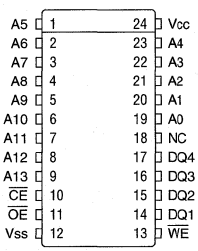
NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

24-Pin DIP
(SA-3)



24-Pin SOJ
(SD-1)



GENERAL DESCRIPTION

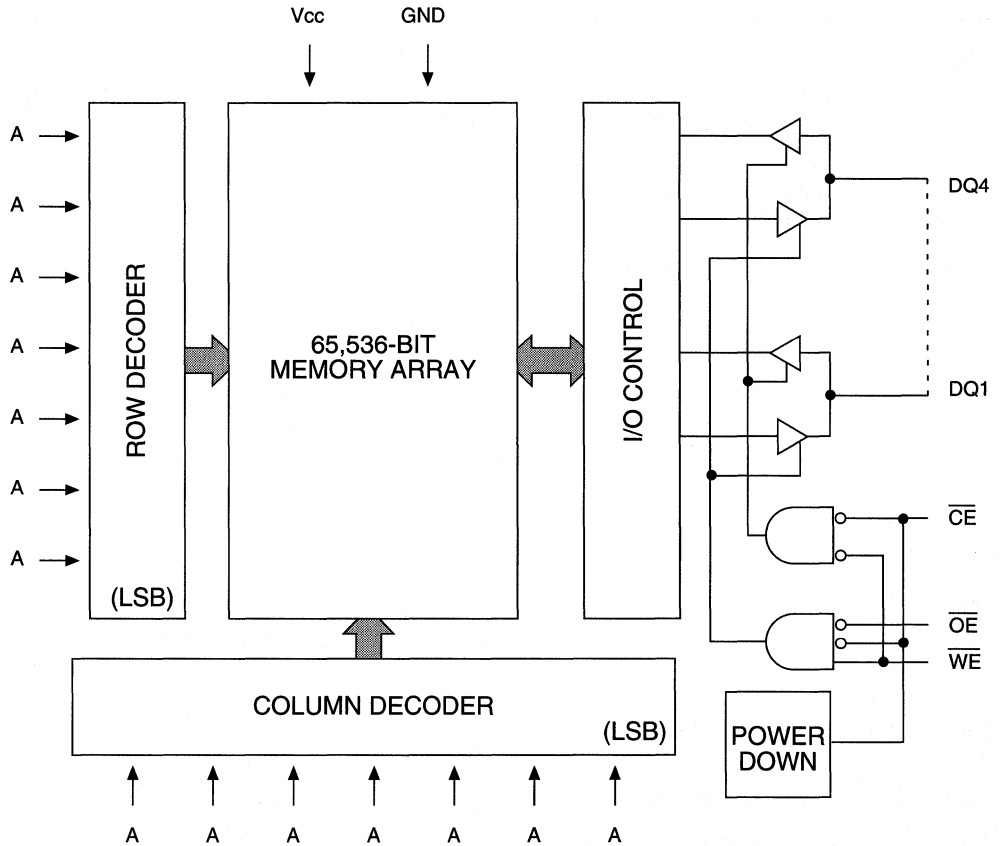
The MT5C6405 is organized as a 16,384 x 4 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) with this organization. This enhancement can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{OE}$ and $\overline{CE}$ go LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL-compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA
Voltage on Any Pin Relative to V_{SS} ..... -1V to V_{CC} +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; V_{CC} = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

				MAX							
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-9	-10	-12	-15	-20	-25	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	125	190	185	175	165	140	130	mA	3, 13
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	22	60	50	45	40	35	35	mA	13
	$\overline{CE} \ge V_{CC}$ -0.2V; V_{CC} = MAX $V_{IN} \le V_{SS}$ +0.2V or $V_{IN} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	0.5	3	3	3	3	3	5	mA	13

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	5	pF	4
Output Capacitance	V_{CC} = 5V	C_O	7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION		-9		-10		-12		-15		-20		-25			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle															
READ cycle time	^tRC	9		10		12		15		20		25		ns	
Address access time	^tAA		9		10		12		15		20		25	ns	
Chip Enable access time	^tACE		9		9		10		12		15		20	ns	
Output hold from address change	^tOH	3		3		3		3		3		3		ns	
Chip Enable to output in Low-Z	^tLZCE	2		2		2		2		2		2		ns	7, 14
Chip disable to output in High-Z	^tHZCE		5		5		6		7		8		8	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		0		0		ns	
Chip disable to power-down time	^tPD		9		10		12		15		20		25	ns	
Output Enable access time	^tAOE		4.5		5		6		7		8		8	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		0		0		ns	
Output disable to output in High-Z	^tHZOE		4.5		5		5		6		7		8	ns	6
WRITE Cycle															
WRITE cycle time	^tWC	9		10		12		15		20		25		ns	
Chip Enable to end of write	^tCW	7		8		10		12		15		20		ns	
Address valid to end of write	^tAW	7		8		10		12		15		20		ns	
Address setup time	^tAS	0		0		0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		0		0		ns	
WRITE pulse width	$^tWP1$	6		7		8		10		12		15		ns	
WRITE pulse width	$^tWP2$	8		9		10		14		18		20		ns	
Data setup time	^tDS	5		6		7		8		9		10		ns	
Data hold time	^tDH	1		1		1		1		1		1		ns	
Write disable to output in Low-Z	^tLZWE	2		2		2		2		2		2		ns	7
Write Enable to output in High-Z	^tHZWE		4		5		5		6		8		8	ns	6, 7

INDUSTRIAL TEMPERATURE SPECIFICATIONS (IT)

The following specifications are to be used for Industrial Temperature (IT) MT5C6405 SRAMs.
(-40°C ≤ T_A ≤ 85°C)

			MAX						
DESCRIPTION	**CONDITIONS**	**SYMBOL**	**-10**	**-12**	**-15**	**-20**	**-25**	**UNITS**	**NOTES**
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	195	185	175	150	140	mA	3, 13
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	60	50	45	40	40	mA	13
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	5	5	5	5	5	mA	13

DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	**CONDITIONS**		**SYMBOL**	**TYP**	**MAX**	**UNITS**	**NOTES**
Data Retention Current	$\overline{CE}$ ≥ (V_{CC} -0.2V) V_{IN} ≥ (V_{CC} -0.2V) or ≤ 0.2V	V_{CC} = 2V	I_{CCDR}	130	300	µA	14
		V_{CC} = 3V	I_{CCDR}	210	550	µA	14

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

Refer to commercial temperature timing parameters for specifications not listed here.
(Notes 5, 14) (-40°C ≤ T_A ≤ 85°C)

DESCRIPTION		-12		-15		-20		-25			
	SYM	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ Cycle											
Output hold from address change	^tOH	2		2		2		2		ns	
Chip Enable to output in Low-Z	^tLZCE	1		1		1		1		ns	7
WRITE Cycle											
Write disable to output in Low-Z	^tLZWE	1		1		1		1		ns	7

AUTOMOTIVE AND EXTENDED TEMPERATURE SPECIFICATIONS (AT AND XT)

The following specifications are to be used for Automotive Temperature (AT) and Extended Temperature (XT) MT5C6405 SRAMs. (-40°C ≤ T_A ≤ 125°C - AT) (-55°C ≤ T_A ≤ 125°C - XT)

			MAX					
DESCRIPTION	**CONDITIONS**	**SYMBOL**	**-12**	**-15**	**-20**	**-25**	**UNITS**	**NOTES**
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	185	175	150	140	mA	3, 13
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	50	45	40	40	mA	13
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	5	5	5	5	mA	13

DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	**CONDITIONS**		**SYMBOL**	**TYP**	**MAX**	**UNITS**	**NOTES**
Data Retention Current	$\overline{CE}$ ≥ (V_{CC} -0.2V) V_{IN} ≥ (V_{CC} -0.2V) or ≤ 0.2V	V_{CC} = 2V	I_{CCDR}	130	300	µA	14
		V_{CC} = 3V	I_{CCDR}	210	550	µA	14

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

Refer to commercial temperature timing parameters for specifications not listed here.
(Notes 5, 14) (-40°C ≤ T_A ≤ 125°C; -55°C ≤ T_A ≤ 125°C; V_{CC} = 5V ±10%)

DESCRIPTION		-12		-15		-20		-25			
	SYM	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ Cycle											
Output hold from address change	^tOH	2		2		2		2		ns	
Chip Enable to output in Low-Z	^tLZCE	1		1		1		1		ns	7
WRITE Cycle											
Write disable to output in Low-Z	^tLZWE	1		1		1		1		ns	7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

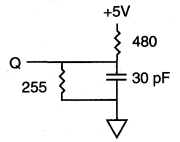


Fig. 1 OUTPUT LOAD EQUIVALENT

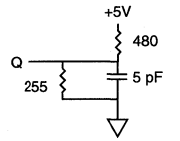


Fig. 2 OUTPUT LOAD EQUIVALENT

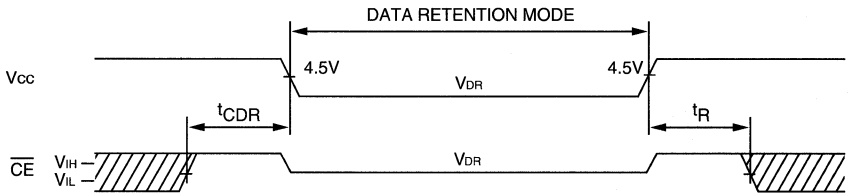
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZWE and ^{t}HZOE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Typical values are measured at 5V, 25°C and 15ns cycle time.
14. Typical currents are measured at 25°C.
15. Output enable ($\overline{OE}$) is inactive (HIGH).
16. Output enable ($\overline{OE}$) is active (LOW).

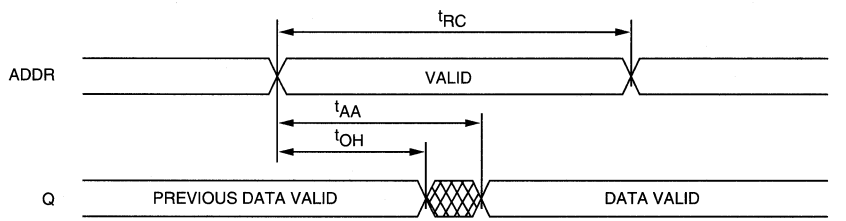
DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			V_{DR}	2			V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	I_{CCDR}		130	300	µA	14
		Vcc = 3V	I_{CCDR}		210	400	µA	14
Chip Deselect to Data Retention Time			^{t}CDR	0			ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

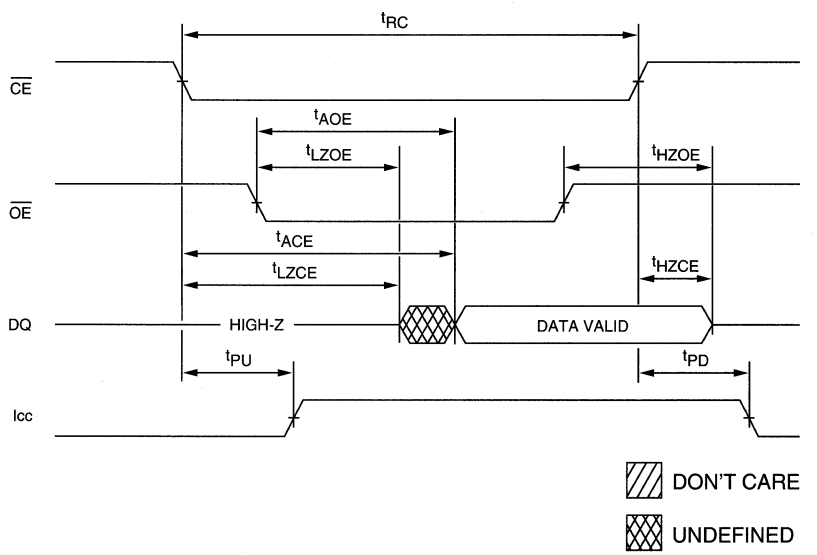
LOW Vcc DATA RETENTION WAVEFORM



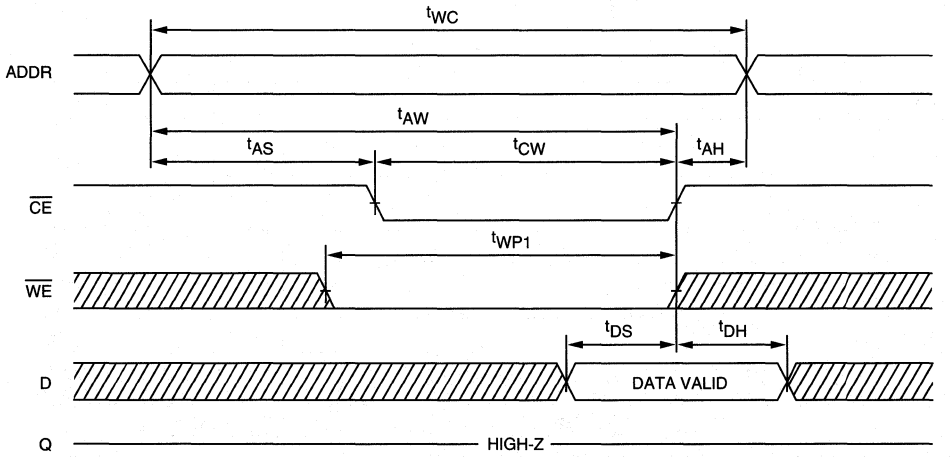
READ CYCLE NO. 1 [8, 9]



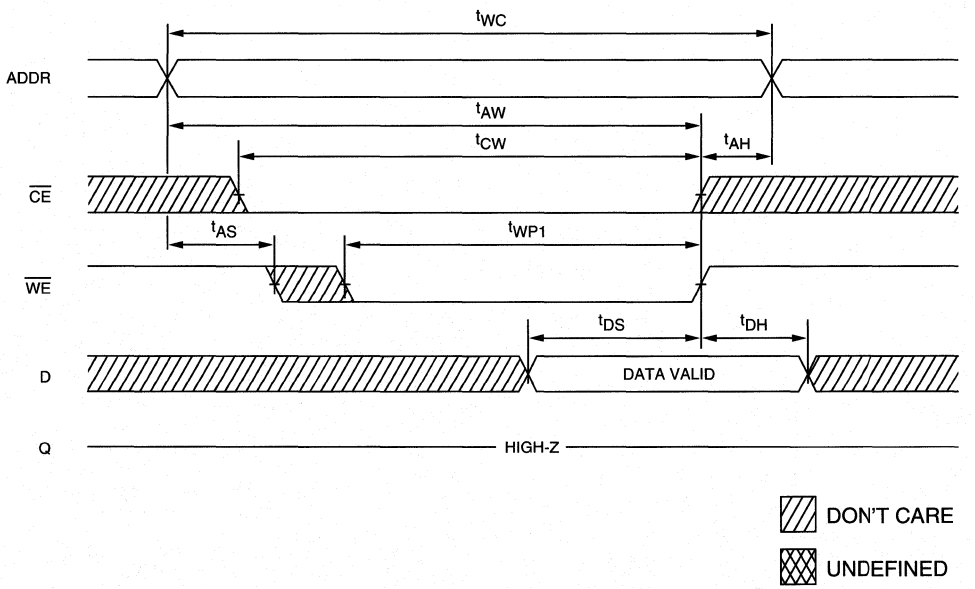
READ CYCLE NO. 2 [7, 8, 10]



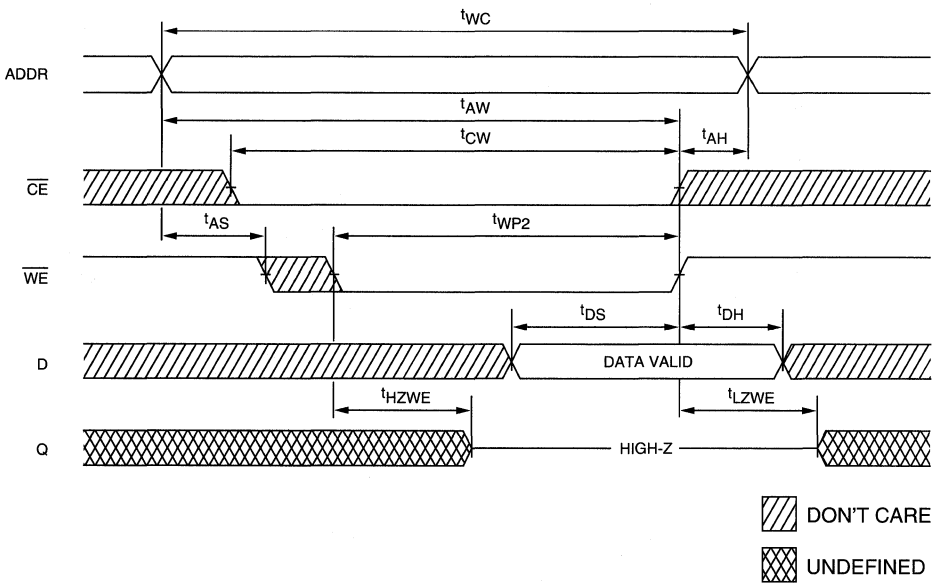
WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)



WRITE CYCLE NO. 2 [7, 12, 15]
(Write Enable Controlled)



WRITE CYCLE NO. 3 [12, 16]
(Write Enable Controlled)



SRAM

64K x 4 SRAM

FEATURES

- High speed: 10, 12, 15, 20, 25 and 35ns
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ option
- All inputs and outputs are TTL-compatible

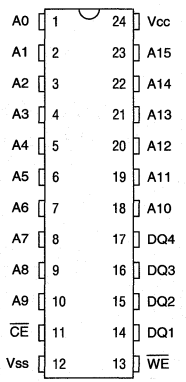
OPTIONS — MARKING

- Timing
  - 10ns access — -10
  - 12ns access — -12
  - 15ns access — -15
  - 20ns access — -20
  - 25ns access — -25
  - 35ns access — -35
- Packages
  - Plastic DIP (300 mil) — None
  - Plastic SOJ (300 mil) — DJ
- 2V data retention — L
- Low power — P
- Temperature
  - Commercial (0°C to +70°C) — None
  - Industrial (-40°C to +85°C) — IT
  - Automotive (-40°C to +125°C) — AT
  - Extended (-55°C to +125°C) — XT
- Part Number Example: MT5C2564DJ-35 L

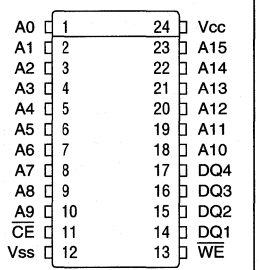
NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

24-Pin DIP (SA-3)



24-Pin SOJ (SD-1)



GENERAL DESCRIPTION

The MT5C2564 is organized as a 65,536 x 4 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

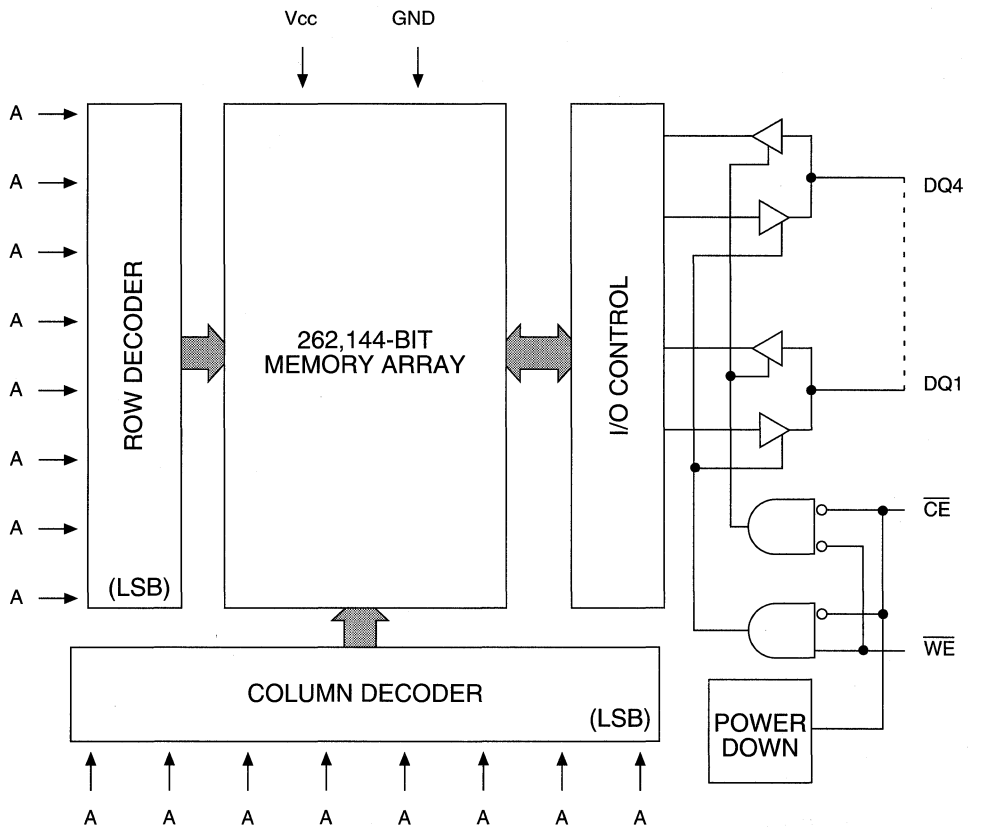
For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) with all organizations. This enhancement can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

The "P" version provides a reduction in both operating current (I_{CC}) and TTL standby current (I_{SB1}). The latter is achieved through the use of gated inputs on the $\overline{WE}$ and address lines, which also facilitates the design of battery backed systems. That is, the gated inputs simplify the design effort and circuitry required to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL-compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	H	X	HIGH-Z	STANDBY
READ	L	H	Q	ACTIVE
WRITE	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA
Voltage on Any Pin Relative to V_{SS} ..... -1V to V_{CC} +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

					MAX							
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-10**	-12**	-15	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	103	190	170	150	130	125	120	mA	3, 13
	P version	I_{CC}	96	-	-	135	125	120	115	mA	3, 13
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	24	55	50	45	40	35	35	mA	13
	P version	I_{SB1}	1.4	-	-	4	4	4	4	mA	13
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	0.6	5	5	5	5	5	7	mA	13
	P version	I_{SB2}	0.4	-	-	3	3	3	3	mA	13

**P version not available with this speed.

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	6	pF	4
Output Capacitance	V_{CC} = 5V	C_O	6	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION		-10		-12		-15		-20		-25		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle															
READ cycle time	^tRC	10		12		15		20		25		35		ns	
Address access time	^tAA		10		12		15		20		25		35	ns	
Chip Enable access time	^tACE		10		12		15		20		25		35	ns	
Output hold from address change	^tOH	3		3		3		3		3		3		ns	
Chip Enable to output in Low-Z	^tLZCE	3		3		3		3		3		3		ns	7
Chip disable to output in High-Z	^tHZCE		5		6		8		9		9		15	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		0		0		ns	
Chip disable to power-down time	^tPD		10		12		15		20		25		35	ns	
WRITE Cycle															
WRITE cycle time	^tWC	10		12		15		20		25		35		ns	
Chip Enable to end of write	^tCW	7		8		10		12		15		20		ns	
Address valid to end of write	^tAW	7		8		10		12		15		20		ns	
Address setup time	^tAS	0		0		0		0		0		0		ns	
Address hold from end of write	^tAH	1		1		1		1		1		1		ns	
WRITE pulse width	$^tWP1$	7		8		10		12		15		20		ns	
WRITE pulse width	$^tWP2$	10		12		12		15		15		20		ns	
Data setup time	^tDS	6		7		7		10		10		15		ns	
Data hold time	^tDH	0		0		0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	2		2		2		2		2		2		ns	7
Write Enable to output in High-Z	^tHZWE		5		6		7		8		10		12	ns	6, 7

INDUSTRIAL TEMPERATURE SPECIFICATIONS (IT)

The following specifications are to be used for Industrial Temperature (IT) MT5C2564 SRAMs.
(-40°C ≤ T_A ≤ 85°C)

			MAX							
DESCRIPTION	**CONDITIONS**	**SYM**	**-10**	**-12**	**-15**	**-20**	**-25**	**-35**	**UNITS**	**NOTES**
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	200	180	155	140	135	135	mA	3, 13
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	65	60	50	45	40	40	mA	13
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	6	6	6	6	6	7	mA	13

DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP versions only)

DESCRIPTION	**CONDITIONS**		**SYMBOL**	**MAX**	**UNITS**	**NOTES**
Data Retention Current	$\overline{CE}$ ≥ (V_{CC} -0.2V) V_{IN} ≥ (V_{CC} -0.2V) or ≤ 0.2V	V_{CC} = 2V	I_{CCDR}	400	µA	
		V_{CC} = 3V	I_{CCDR}	600	µA	
Data Retention Current LP version	$\overline{CE}$ ≥ (V_{CC} -0.2V)	V_{CC} = 2V	I_{CCDR}	400	µA	
		V_{CC} = 3V	I_{CCDR}	600	µA	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

Refer to commercial temperature timing parameters for specifications not listed here.
(Notes 5, 13) (-40°C ≤ T_A ≤ 85°C)

DESCRIPTION		-12		-15		-20		-25		-35			
	SYM	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ Cycle													
Output hold from address change	^tOH	2		2		2		2		2		ns	
Chip Enable to output in Low-Z	^tLZCE	2		2		2		2		2		ns	7

AUTOMOTIVE AND EXTENDED TEMPERATURE SPECIFICATIONS (AT AND XT)

The following specifications are to be used for Automotive Temperature (AT) and Extended Temperature (XT) MT5C2564 SRAMs. (-40°C ≤ T_A ≤ 125°C - AT) (-55°C ≤ T_A ≤ 125°C - XT)

			MAX						
DESCRIPTION	**CONDITIONS**	**SYMBOL**	**-12**	**-15**	**-20**	**-25**	**-35**	**UNITS**	**NOTES**
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	180	155	140	135	135	mA	3, 13
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	60	50	45	40	40	mA	13
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	7	7	7	7	7	mA	13

DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP versions only)

DESCRIPTION	**CONDITIONS**		**SYMBOL**	**MAX**	**UNITS**	**NOTES**
Data Retention Current	$\overline{CE}$ ≥ (V_{CC} -0.2V) V_{IN} ≥ (V_{CC} -0.2V) or ≤ 0.2V	V_{CC} = 2V	I_{CCDR}	500	µA	
		V_{CC} = 3V	I_{CCDR}	800	µA	
Data Retention Current LP version	$\overline{CE}$ ≥ (V_{CC} -0.2V)	V_{CC} = 2V	I_{CCDR}	500	µA	
		V_{CC} = 3V	I_{CCDR}	800	µA	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

Refer to commercial temperature timing parameters for specifications not listed here.
(Notes 5, 13) (-40°C ≤ T_A ≤ 125°C; -55°C ≤ T_A ≤ 125°C; V_{CC} = 5V ± 10%)

DESCRIPTION		-12		-15		-20		-25		-35			
	SYM	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ Cycle													
Output hold from address change	^tOH	2		2		2		2		2		ns	
Chip Enable to output in Low-Z	^tLZCE	2		2		2		2		2		ns	7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

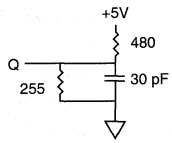


Fig. 1 OUTPUT LOAD EQUIVALENT

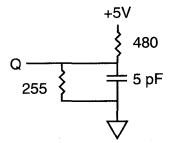


Fig. 2 OUTPUT LOAD EQUIVALENT

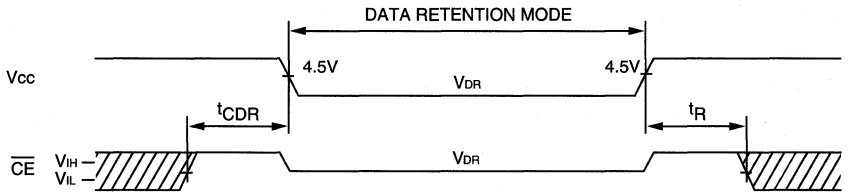
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE, and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Typical values are measured at 5V, 25°C and 15ns cycle time.
14. Typical currents are measured at 25°C.

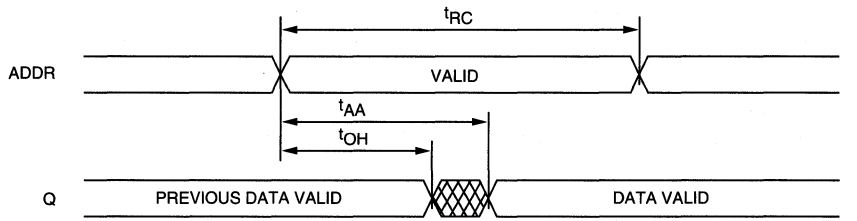
DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP versions only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2			V	
Data Retention Current L version	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	ICCDR		175	300	µA	14
		Vcc = 3V	ICCDR		250	500	µA	14
Data Retention Current LP version	$\overline{CE}$ ≥ (Vcc -0.2V)	Vcc = 2V	ICCDR		175	300	µA	14
		Vcc = 3V	ICCDR		250	500	µA	14
Chip Deselect to Data Retention Time			^{t}CDR	0			ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 10

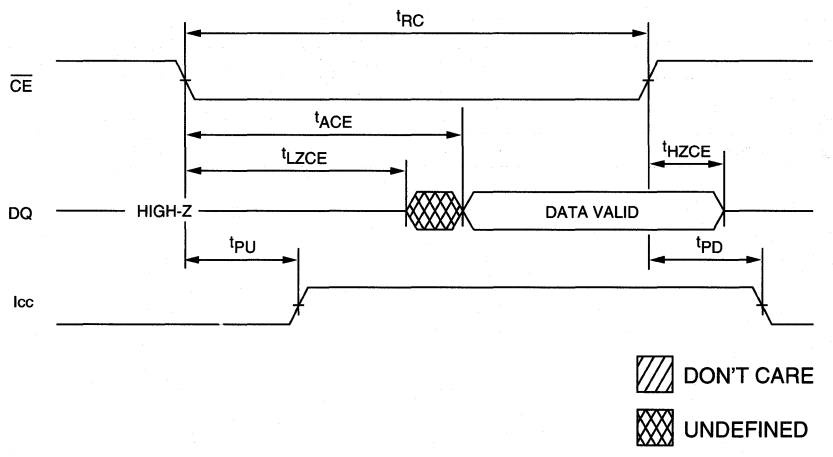
LOW Vcc DATA RETENTION WAVEFORM



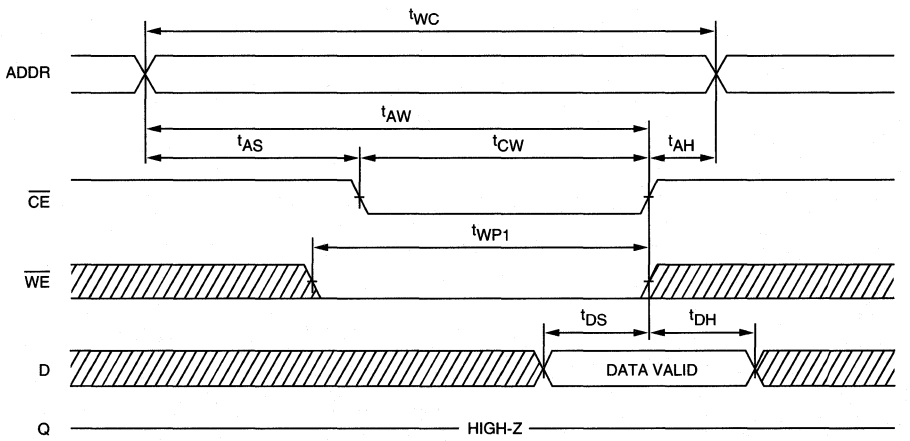
READ CYCLE NO. 1 [8, 9]



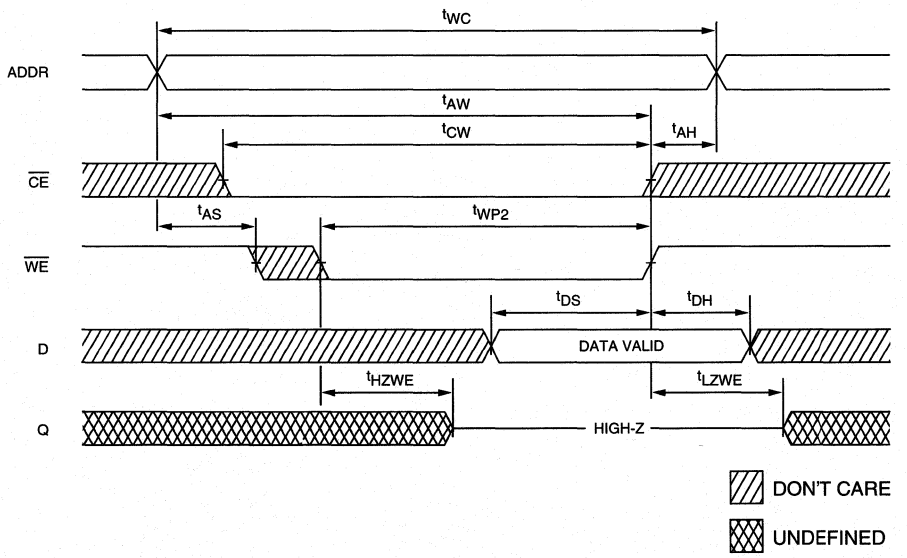
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1
(Chip Enable Controlled)



WRITE CYCLE NO. 2 [7, 12]
(Write Enable Controlled)



SRAM

64K x 4 SRAM
WITH OUTPUT ENABLE

FEATURES
- High speed: 10, 12, 15, 20, 25 and 35ns
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- All inputs and outputs are TTL-compatible

OPTIONS — MARKING

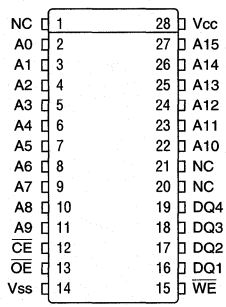
• Timing	
10ns access	-10
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
35ns access	-35
• Packages	
Plastic DIP (300 mil)	None
Plastic SOJ (300 mil)	DJ
• 2V data retention	L
• Low power	P
• Temperature	
Commercial (0°C to +70°C)	None
Industrial (-40°C to +85°C)	IT
Automotive (-40°C to +125°C)	AT
Extended (-55°C to +125°C)	XT

- Part Number Example: MT5C2565DJ-35 P

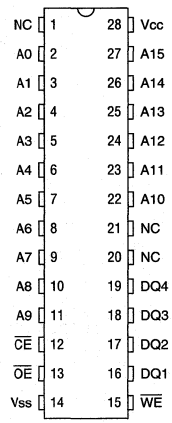
NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

28-Pin SOJ (SD-2)



28-Pin DIP (SA-4)



GENERAL DESCRIPTION

The MT5C2565 is organized as a 65,536 x 4 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

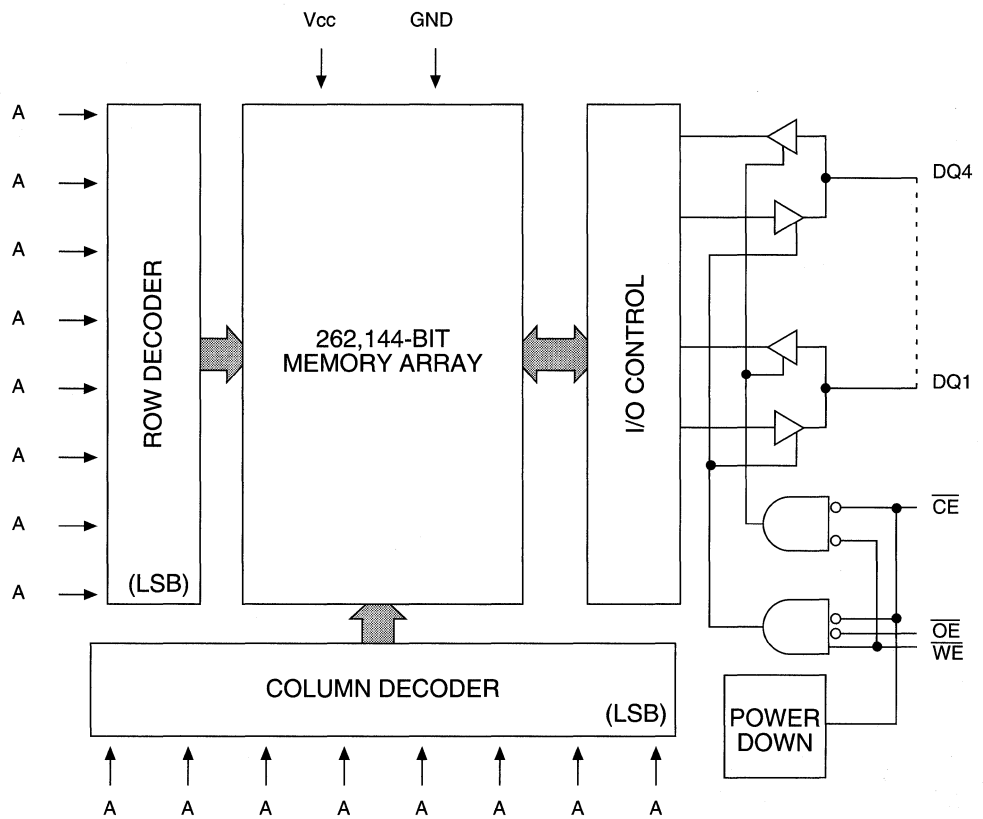
For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) with this organization. These enhancements can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ and $\overline{OE}$ go LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

The "P" version provides a reduction in both operating current (I_{CC}) and TTL standby current (I_{SB1}). The latter is achieved through the use of gated inputs on the $\overline{WE}$, $\overline{OE}$ and address lines, which also facilitates the design of battery backed systems. That is, the gated inputs simplify the design effort and circuitry required to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL-compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA
Voltage on Any Pin Relative to V_{SS} ..... -1V to V_{CC} +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

					MAX							
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-10**	-12**	-15	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	103	190	170	150	130	125	120	mA	3, 13
	P version	I_{CC}	96	-	-	135	125	120	115	mA	3, 13
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	24	55	50	45	40	35	35	mA	13
	P version	I_{SB1}	1.4	-	-	4	4	4	4	mA	13
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	0.6	5	5	5	5	5	7	mA	13
	P version	I_{SB2}	0.4	-	-	3	3	3	3	mA	13

**P version not available with this speed.

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	6	pF	4
Output Capacitance	V_{CC} = 5V	C_O	6	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION		-10		-12		-15		-20		-25		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle															
READ cycle time	^tRC	10		12		15		20		25		35		ns	
Address access time	^tAA		10		12		15		20		25		35	ns	
Chip Enable access time	^tACE		10		12		15		20		25		35	ns	
Output hold from address change	^tOH	3		3		3		3		3		3		ns	
Chip Enable to output in Low-Z	^tLZCE	3		3		3		3		3		3		ns	7
Chip disable to output in High-Z	^tHZCE		5		6		8		9		9		15	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		0		0		ns	
Chip disable to power-down time	^tPD		10		12		15		20		25		35	ns	
Output Enable access time	^tAOE		5		6		8		8		8		12	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		0		0		ns	
Output disable to out put in High-Z	^tHZOE		5		6		6		7		7		12	ns	6
WRITE Cycle															
WRITE cycle time	^tWC	10		12		15		20		25		35		ns	
Chip Enable to end of write	^tCW	7		8		10		12		15		20		ns	
Address valid to end of write	^tAW	7		8		10		12		15		20		ns	
Address setup time	^tAS	0		0		0		0		0		0		ns	
Address hold from end of write	^tAH	1		1		1		1		1		1		ns	
WRITE pulse width	$^tWP1$	7		8		10		12		15		20		ns	
WRITE pulse width	$^tWP2$	10		12		12		15		15		20		ns	
Data setup time	^tDS	6		7		7		10		10		15		ns	
Data hold time	^tDH	0		0		0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	2		2		2		2		2		2		ns	7
Write Enable to output in High-Z	^tHZWE		5		6		7		8		10		12	ns	6, 7

INDUSTRIAL TEMPERATURE SPECIFICATIONS (IT)

The following specifications are to be used for Industrial Temperature (IT) MT5C2565 SRAMs.
(-40°C ≤ T_A ≤ 85°C)

			MAX							
DESCRIPTION	**CONDITIONS**	**SYM**	**-10**	**-12**	**-15**	**-20**	**-25**	**-35**	**UNITS**	**NOTES**
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	200	180	155	140	135	135	mA	3, 13
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	65	60	50	45	40	40	mA	13
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	6	6	6	6	6	7	mA	13

DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP versions only)

DESCRIPTION	**CONDITIONS**		**SYMBOL**	**MAX**	**UNITS**	**NOTES**
Data Retention Current	$\overline{CE}$ ≥ (V_{CC} -0.2V) V_{IN} ≥ (V_{CC} -0.2V) or ≤ 0.2V	V_{CC} = 2V	I_{CCDR}	400	µA	
		V_{CC} = 3V	I_{CCDR}	600	µA	
Data Retention Current LP version	$\overline{CE}$ ≥ (V_{CC} -0.2V)	V_{CC} = 2V	I_{CCDR}	400	µA	
		V_{CC} = 3V	I_{CCDR}	600	µA	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

Refer to commercial temperature timing parameters for specifications not listed here.
(Notes 5, 13) (-40°C ≤ T_A ≤ 85°C)

DESCRIPTION		-12		-15		-20		-25		-35			
	SYM	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ Cycle													
Output hold from address change	^tOH	2		2		2		2		2		ns	
Chip Enable to output in Low-Z	^tLZCE	2		2		2		2		2		ns	7

AUTOMOTIVE AND EXTENDED TEMPERATURE SPECIFICATIONS (AT AND XT)

The following specifications are to be used for Automotive Temperature (AT) and Extended Temperature (XT) MT5C2565 SRAMs. (-40°C ≤ T_A ≤ 125°C - AT) (-55°C ≤ T_A ≤ 125°C - XT)

			MAX						
DESCRIPTION	**CONDITIONS**	**SYMBOL**	**-12**	**-15**	**-20**	**-25**	**-35**	**UNITS**	**NOTES**
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	180	155	140	135	135	mA	3, 13
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	60	50	45	40	40	mA	13
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	7	7	7	7	7	mA	13

DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP versions only)

DESCRIPTION	**CONDITIONS**		**SYMBOL**	**MAX**	**UNITS**	**NOTES**
Data Retention Current	$\overline{CE}$ ≥ (V_{CC} -0.2V) V_{IN} ≥ (V_{CC} -0.2V) or ≤ 0.2V	V_{CC} = 2V	I_{CCDR}	500	µA	
		V_{CC} = 3V	I_{CCDR}	800	µA	
Data Retention Current LP version	$\overline{CE}$ ≥ (V_{CC} -0.2V)	V_{CC} = 2V	I_{CCDR}	500	µA	
		V_{CC} = 3V	I_{CCDR}	800	µA	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

Refer to commercial temperature timing parameters for specifications not listed here.
(Notes 5, 13) (-40°C ≤ T_A ≤ 125°C; -55°C ≤ T_A ≤ 125°C; V_{CC} = 5V ± 10%)

DESCRIPTION		**-12**		**-15**		**-20**		**-25**		**-35**			
	SYM	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ Cycle													
Output hold from address change	^tOH	2		2		2		2		2		ns	
Chip Enable to output in Low-Z	^tLZCE	2		2		2		2		2		ns	7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

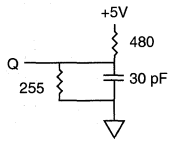


Fig. 1 OUTPUT LOAD EQUIVALENT

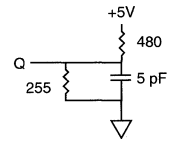


Fig. 2 OUTPUT LOAD EQUIVALENT

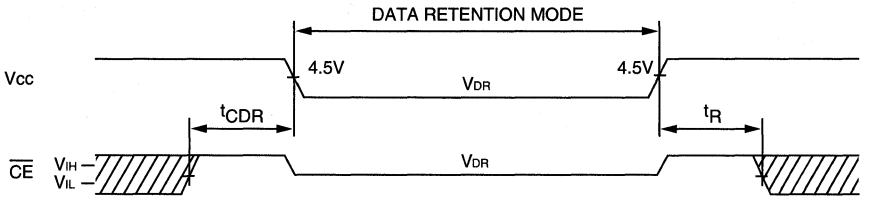
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZOE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE, and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Typical values are measured at 5V, 25°C and 15ns cycle time.
14. Typical currents are measured at 25°C.
15. Output enable ($\overline{OE}$) is inactive (HIGH).
16. Output enable ($\overline{OE}$) is active (LOW).

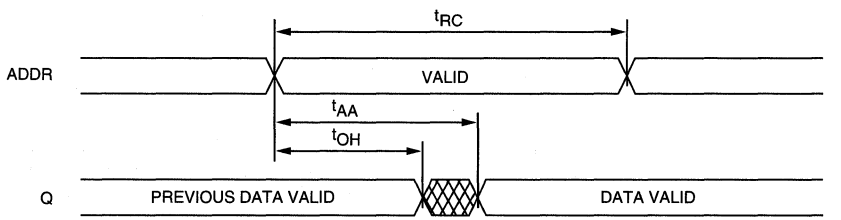
DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP versions only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2			V	
Data Retention Current L version	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	ICCDR		175	300	µA	14
		Vcc = 3V	ICCDR		250	500	µA	14
Data Retention Current LP version	$\overline{CE}$ ≥ (Vcc -0.2V)	Vcc = 2V	ICCDR		175	300	µA	14
		Vcc = 3V	ICCDR		250	500	µA	14
Chip Deselect to Data Retention Time			^{t}CDR	0			ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

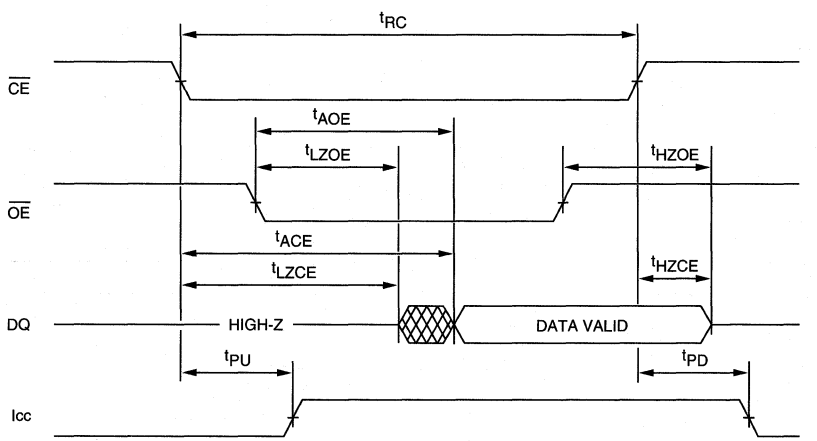
LOW Vcc DATA RETENTION WAVEFORM



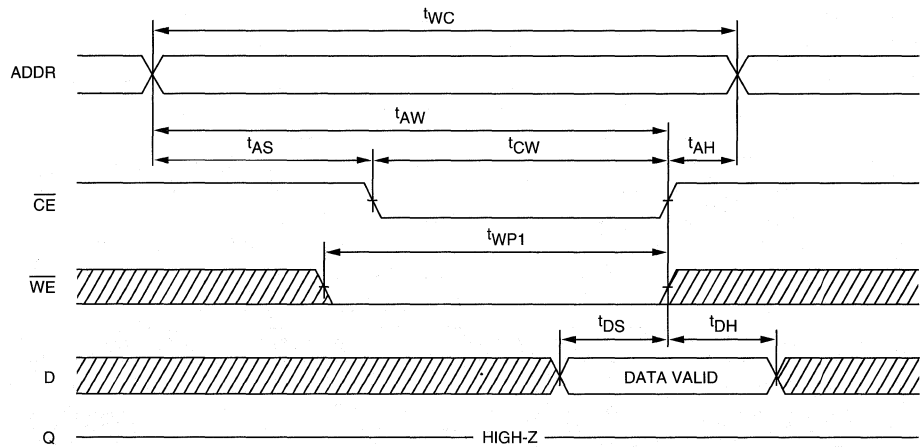
READ CYCLE NO. 1 [8, 9]



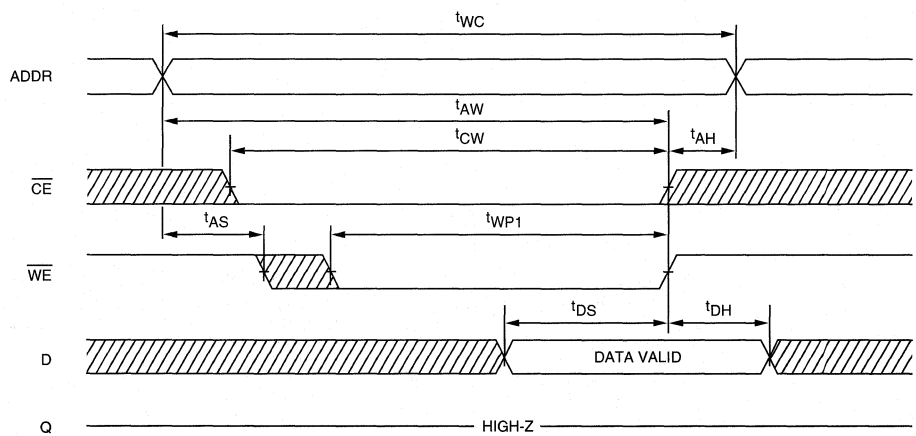
READ CYCLE NO. 2 [7, 8, 10]



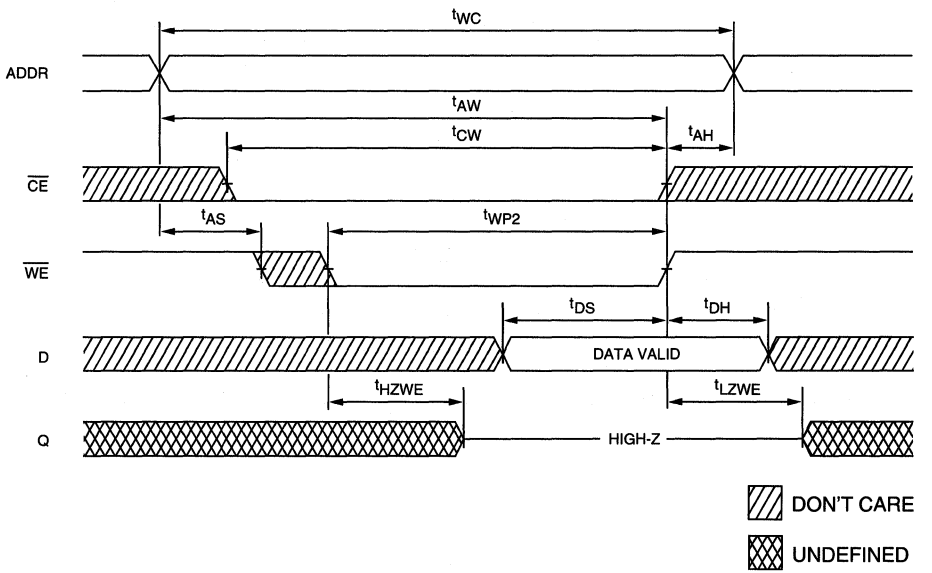
WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)



WRITE CYCLE NO. 2 [7, 12, 15]
(Write Enable Controlled)



WRITE CYCLE NO. 3 [7, 12, 16]
(Write Enable Controlled)



SRAM

256K x 4 SRAM

WITH OUTPUT ENABLE

FEATURES

- High speed: 12, 15, 17, 20, 25 and 35
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- All inputs and outputs are TTL-compatible
- Fast $\overline{OE}$ access time: 8ns

OPTIONS

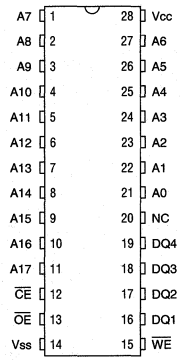
	MARKING
• Timing	
12ns access	-12
15ns access	-15
17ns access	-17
20ns access	-20
25ns access	-25
35ns access	-35
• Packages	
Plastic DIP (400 mil)	None
Plastic SOJ (400 mil)	DJ
Plastic SOJ (300 mil)	SJ
• 2V data retention	L
• 2V data retention, low power	LP
• Temperature	
Commercial (0°C to +70°C)	None
Industrial (-40°C to +85°C)	IT
Automotive (-40°C to +125°C)	AT
Extended (-55°C to +125°C)	XT

- Part Number Example: MT5C1005DJ-25 IT

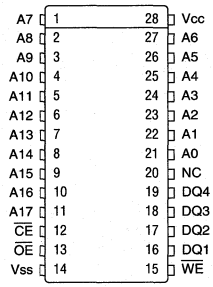
NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

28-Pin DIP
(SA-5)



28-Pin SOJ
(SD-2)
(SD-3)



GENERAL DESCRIPTION

The MT5C1005 is organized as a 262,144 x 4 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

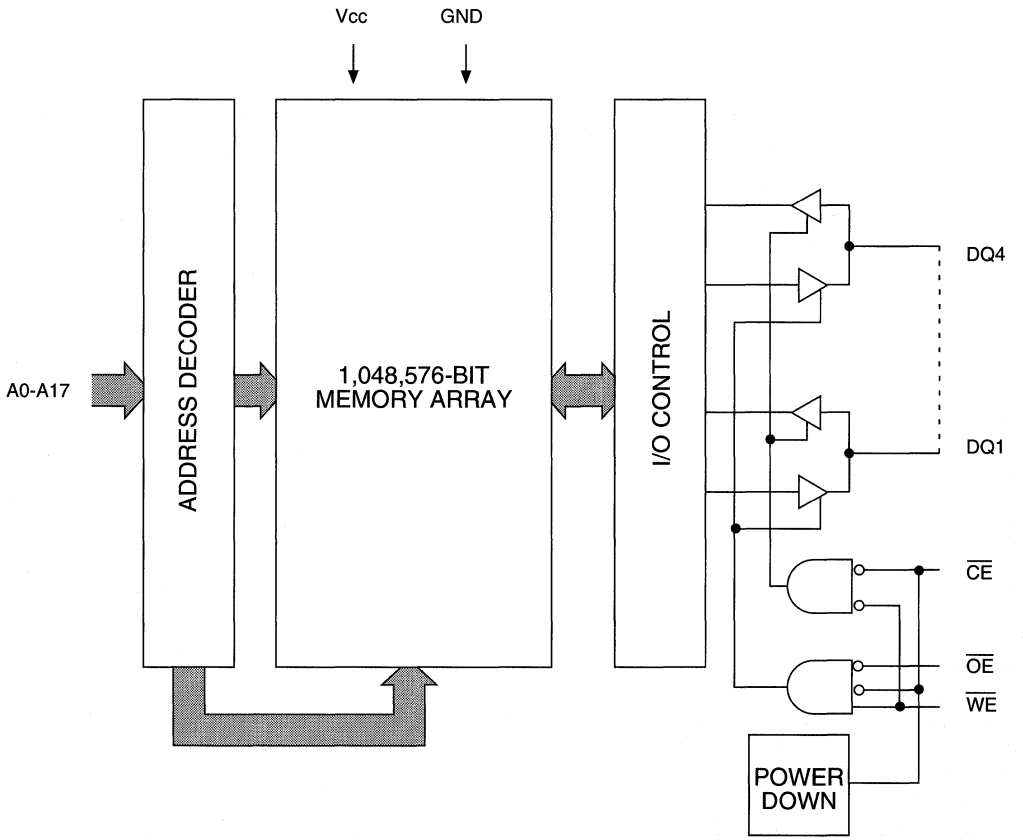
For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) with this organization. This enhancement can place the outputs in High-Z for additional flexibility in system design.

Writing to this device is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH while output enable ($\overline{OE}$) and $\overline{CE}$ go LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

The "L" and "LP" versions each provide a 70 percent reduction in CMOS standby current (I_{SB2}) over the standard version. The LP version also provides a 90 percent reduction in TTL standby current (I_{SB1}) through the use of gated inputs on the $\overline{WE}$, $\overline{OE}$ and address lines, which also facilitates the design of battery backed systems. That is, the gated inputs simplify the design effort and circuitry required to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL-compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA
Voltage on Any Pin Relative to V_{SS} ..... -1V to V_{CC} +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; V_{CC} = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

				MAX							
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-12	-15	-17	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	95	190	165	155	140	125	115	mA	3, 13
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	17	45	40	40	35	30	25	mA	13
	LP version only	I_{SB1}	1.3	3	3	3	3	3	3	mA	13
	$\overline{CE} \ge V_{CC}$ -0.2V; V_{CC} = MAX $V_{IN} \le V_{SS}$ +0.2V or $V_{IN} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	0.4	5	5	5	5	5	5	mA	13
	L and LP versions only	I_{SB2}	0.3	1.5	1.5	1.5	1.5	1.5	1.5	mA	13

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	8	pF	4
Output Capacitance	V_{CC} = 5V	C_O	8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) ($0°C \le T_A \le 70°C$; $V_{CC} = 5V \pm 10\%$)

DESCRIPTION	SYM	-12		-15		-17		-20		-25		-35		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
READ Cycle															
READ cycle time	tRC	12		15		17		20		25		35		ns	
Address access time	tAA		12		15		17		20		25		35	ns	
Chip Enable access time	tACE		12		15		17		20		25		35	ns	
Output hold from address change	tOH	3		3		3		3		5		5		ns	
Chip Enable to output in Low-Z	tLZCE	3		5		5		5		5		5		ns	7
Chip disable to output in High-Z	tHZCE		5		6		7		8		10		15	ns	6, 7
Chip Enable to power-up time	tPU	0		0		0		0		0		0		ns	
Chip disable to power-down time	tPD		12		15		17		20		25		35	ns	
Output Enable access time	tAOE		4		5		5		6		8		12	ns	
Output Enable to output in Low-Z	tLZOE	0		0		0		0		0		0		ns	
Output disable to output in High-Z	tHZOE		4		5		5		6		10		12	ns	6
WRITE Cycle															
WRITE cycle time	tWC	12		15		17		20		25		35		ns	
Chip Enable to end of write	tCW	8		10		12		12		15		20		ns	
Address valid to end of write	tAW	8		10		12		12		15		20		ns	
Address setup time	tAS	0		0		0		0		0		0		ns	
Address hold from end of write	tAH	0		0		0		0		0		0		ns	
WRITE pulse width	tWP1	8		9		12		12		15		20		ns	
WRITE pulse width	tWP2	10		12		13		15		15		20		ns	
Data setup time	tDS	6		7		8		8		10		15		ns	
Data hold time	tDH	0		0		0		0		0		0		ns	
Write disable to output in Low-Z	tLZWE	3		3		3		3		3		3		ns	7
Write Enable to output in High-Z	tHZWE		5		6		7		8		10		15	ns	6, 7

INDUSTRIAL TEMPERATURE SPECIFICATIONS (IT)

The following specifications are to be used for Industrial Temperature (IT) MT5C1005 SRAMs.
(-40°C ≤ T_A ≤ 85°C)

				MAX					
DESCRIPTION	**CONDITIONS**	**SYMBOL**	**TYP**	**-20**	**-25**	**-35**	**-45**	**UNITS**	**NOTES**
Power Supply Current: Operating	CE2 ≥ V_{IH}; $\overline{CE1}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	95	150	135	125	120	mA	3, 13
Power Supply Current: Standby	CE2 ≤ V_{IH} or $\overline{CE1}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	17	35	30	25	25	mA	13
	CE2 ≤ V_{SS} +0.2V; $\overline{CE1}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	0.4	5	5	5	5	mA	13
L version only	CE2 ≤ V_{SS} +0.2V; $\overline{CE1}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	0.3	2	2	2	2	mA	13

DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	**CONDITIONS**		**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**NOTES**
Data Retention Current	$\overline{CE1}$ ≥ (V_{CC} -0.2V) or CE2 ≤ (V_{SS} +0.2V) V_{IN} ≥ (V_{CC} -0.2V) or ≤ 0.2V	V_{CC} = 2V	I_{CCDR}		35	170	µA	14
		V_{CC} = 3V	I_{CCDR}		60	325	µA	14

AUTOMOTIVE AND EXTENDED TEMPERATURE SPECIFICATIONS (AT AND XT)

The following specifications are to be used for Automotive Temperature (AT) and Extended Temperature (XT) MT5C1005 SRAMs. (-40°C ≤ T_A ≤ 125°C - AT) (-55°C ≤ T_A ≤ 125°C - XT)

				MAX					
DESCRIPTION	**CONDITIONS**	**SYMBOL**	**TYP**	**-20**	**-25**	**-35**	**-45**	**UNITS**	**NOTES**
Power Supply Current: Operating	CE2 ≥ V_{IH}; $\overline{CE1}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	95	150	135	125	120	mA	3, 13
Power Supply Current: Standby	CE2 ≤ V_{IH} or $\overline{CE1}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	17	45	40	35	32	mA	13
	CE2 ≤ V_{SS} +0.2V; $\overline{CE1}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	0.4	7	7	7	7	mA	13
L version only	CE2 ≤ V_{SS} +0.2V; $\overline{CE1}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	0.3	5	5	5	5	mA	13

DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	**CONDITIONS**		**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**NOTES**
Data Retention Current	$\overline{CE1}$ ≥ (V_{CC} -0.2V) or CE2 ≤ (V_{SS} +0.2V) V_{IN} ≥ (V_{CC} -0.2V) or ≤ 0.2V	V_{CC} = 2V	I_{CCDR}		35	1,000	µA	14
		V_{CC} = 3V	I_{CCDR}		60	1,500	µA	14

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

Refer to commercial temperature timing parameters for specifications not listed here.
(Notes 5, 14) (-40°C ≤ T_A ≤ 125°C; -55°C ≤ T_A ≤ 125°C; V_{CC} = 5V ±10%)

DESCRIPTION		-20		-25		-35		-45			
	SYM	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ Cycle											
Output hold from address change	^tOH	3		3		3		3		ns	
Chip Enable to output in Low-Z	^tLZCE	3		3		3		3		ns	7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

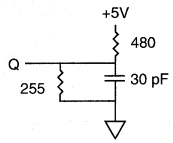


Fig. 1 OUTPUT LOAD EQUIVALENT

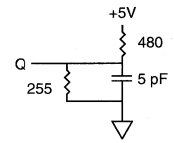


Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

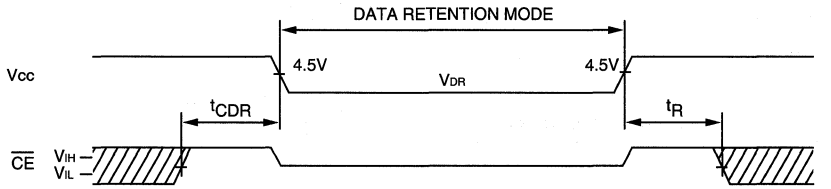
1. All voltages referenced to Vss (GND).
2. -3V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZOE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE, and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables and output enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Typical values are measured at 5V, 25°C and 25ns cycle time.
14. Typical currents are measured at 25°C.
15. Output enable ($\overline{OE}$) is inactive (HIGH).
16. Output enable ($\overline{OE}$) is active (LOW).

DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP versions only)

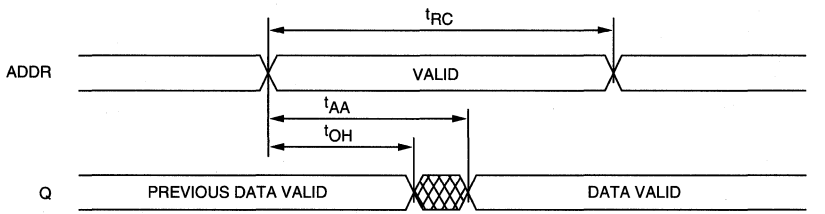
DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2			V	
Data Retention Current L version	$\overline{CE}$ ≥ (Vcc -0.2V)	Vcc = 2V	ICCDR		35	150	µA	14
	VIN ≥ (Vcc -0.2V)	Vcc = 3V	ICCDR		60	250	µA	14
	or ≤ 0.2V	Vcc = 3V*	ICCDR		30	100	µA	14
Data Retention Current LP version	$\overline{CE}$ ≥ (Vcc -0.2V)	Vcc = 2V	ICCDR		35	150	µA	14
		Vcc = 3V	ICCDR		60	250	µA	14
Chip Deselect to Data Retention Time			^{t}CDR	0			ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

*Advance

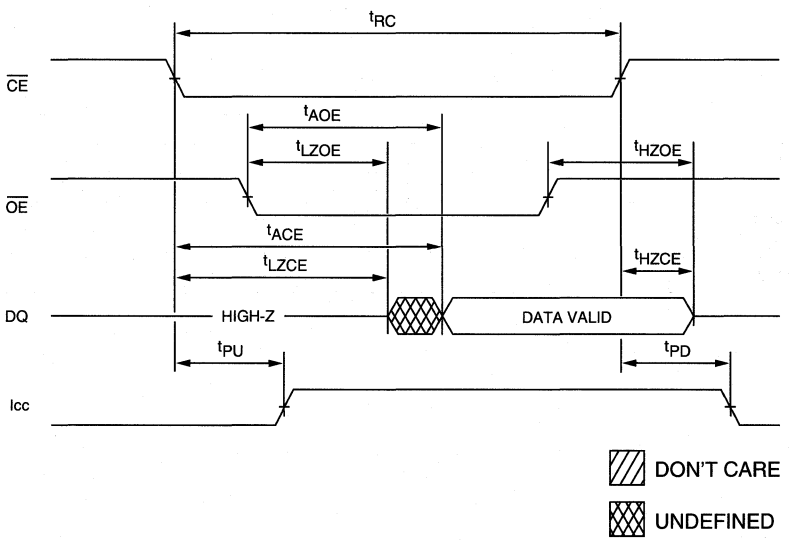
LOW Vcc DATA RETENTION WAVEFORM



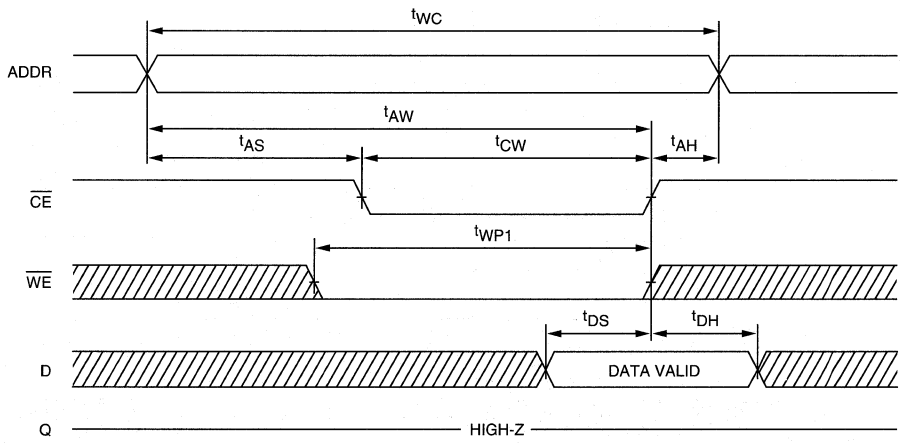
READ CYCLE NO. 1 [8, 9]



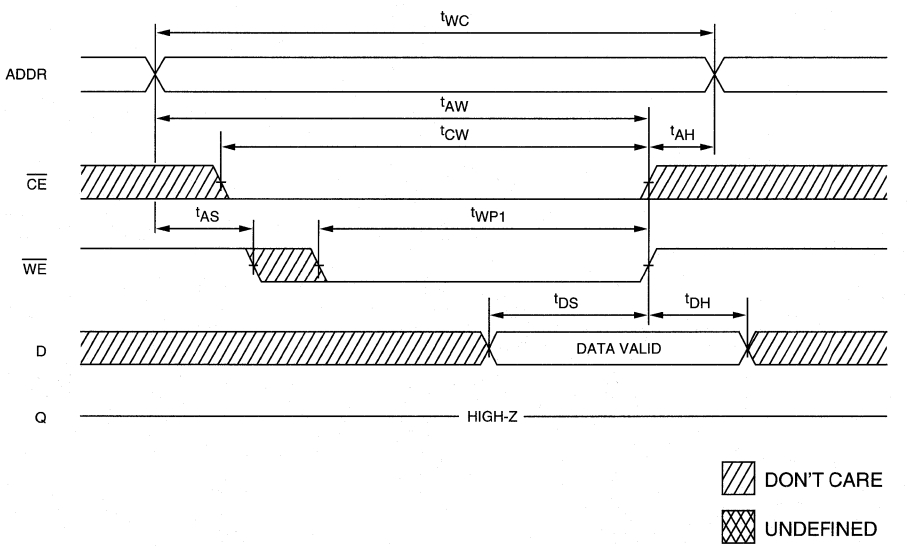
READ CYCLE NO. 2 [7, 8, 10]



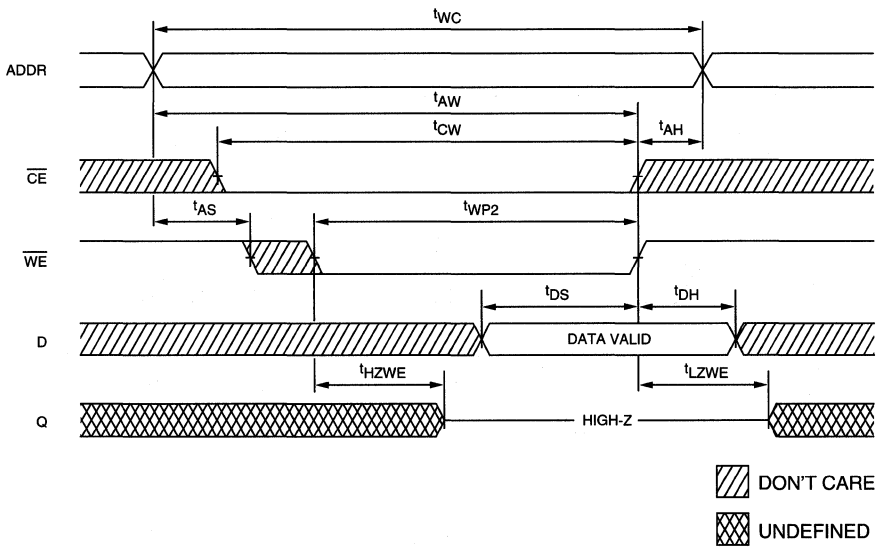
WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)



WRITE CYCLE NO. 2 [12, 15]
(Write Enable Controlled)



WRITE CYCLE NO. 3 [7, 12, 16]
(Write Enable Controlled)



MICRON SEMICONDUCTOR, INC.

MT5C256K4A1
REVOLUTIONARY PINOUT 256K x 4 SRAM

SRAM

256K x 4 SRAM

WITH SINGLE CHIP ENABLE, REVOLUTIONARY PINOUT

FEATURES

- High speed: 12, 15, 20 and 25ns
- Multiple center power and ground pins for greater noise immunity
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- Automatic $\overline{CE}$ power down
- All inputs and outputs are TTL-compatible
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Fast $\overline{OE}$ access times: 6, 8, 10 and 12ns

OPTIONS

	MARKING
• Timing	
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
• Packages	
32-pin SOJ (400 mil)	DJ
• 2V data retention	L
• Temperature	
Commercial (0°C to +70°C)	None
Industrial (-40°C to +85°C)	IT*
Automotive (-40°C to +125°C)	AT*
Extended (-55°C to +125°C)	XT*

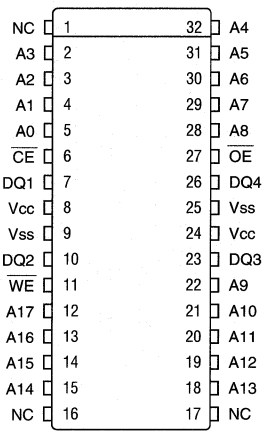
- Part Number Example: MT5C256K4A1DJ-15

*Contact the factory for specifications and availability.

NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

32-Pin SOJ
(SD-5)



GENERAL DESCRIPTION

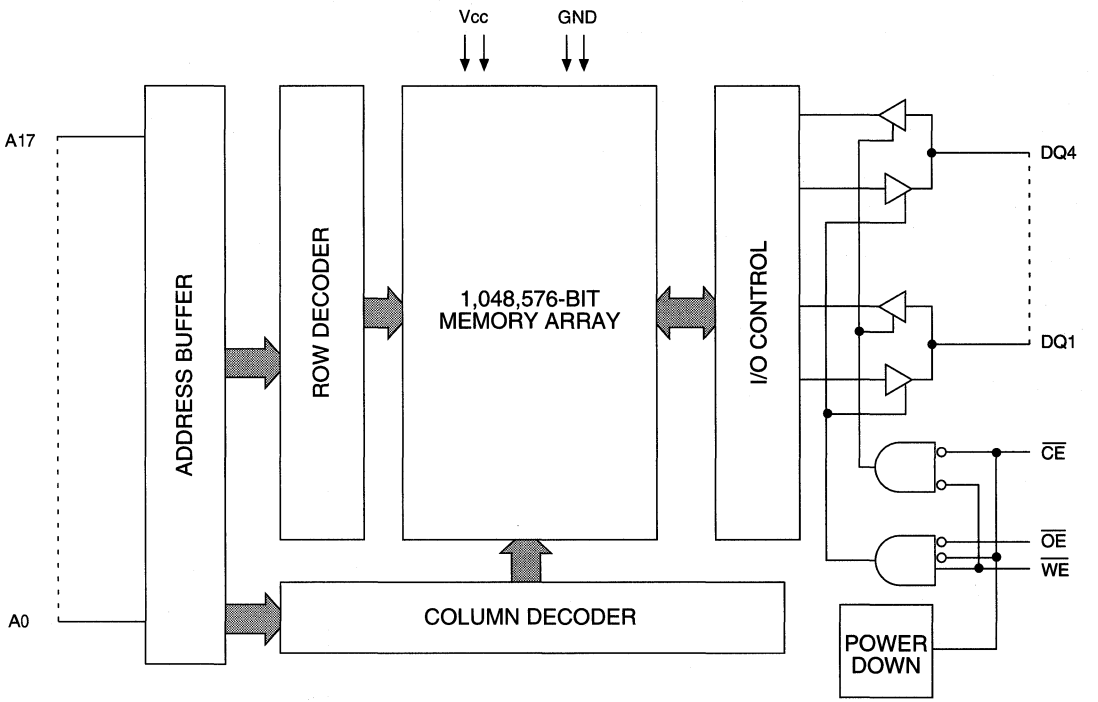
The MT5C256K4A1 is organized as a 262,144 x 4 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

This device offers multiple center power and ground pins for improved performance. For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) with this organization. This enhancement can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{OE}$ and $\overline{CE}$ go LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL-compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

PIN DESCRIPTIONS

SOJ PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
5, 4, 3, 2, 32, 31, 30, 29, 28, 22, 21, 20, 19, 18, 15, 14, 13, 12	A0-A17	Input	Address Inputs: These inputs determine which cell is addressed.
11	$\overline{WE}$	Input	Write Enable: This input determines if the cycle is a READ or WRITE cycle. $\overline{WE}$ is LOW for a WRITE cycle and HIGH for a READ cycle.
6	$\overline{CE}$	Input	Chip Enable: This active LOW input is used to enable the device. When $\overline{CE}$ is HIGH, the chip is disabled and automatically goes into standby power mode.
27	$\overline{OE}$	Input	Output Enable: This active LOW input enables the output drivers.
7, 10, 23, 26	DQ1-DQ4	Input/ Output	SRAM Data I/O: Data inputs and tristate data outputs.
8, 24	Vcc	Supply	Power Supply: 5V ±10%
9, 25	Vss	Supply	Ground: GND
1, 16, 17	NC	-	No Connect: These signals are not internally connected.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply relative to Vss ..... -1V to +7V
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1.7W
Short Circuit Output Current 50mA
Voltage on Any Pin Relative to V_{SS} ..... -1V to Vcc +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

				MAX					
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-12	-15	-20	-25	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	150	300	260	220	200	mA	3
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	25	50	45	40	35	mA	
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	0.5	5	5	5	5	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	6	pF	4
Output Capacitance	V_{CC} = 5V	C_O	6	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 5, 13) ($0°C \le T_A \le 70°C$; $V_{CC} = 5V \pm 10\%$)

DESCRIPTION		-12		-15		-20		-25			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle											
READ cycle time	^tRC	12		15		20		25		ns	
Address access time	^tAA		12		15		20		25	ns	
Chip Enable access time	^tACE		12		15		20		25	ns	
Output hold from address change	^tOH	4		4		5		5		ns	
Chip Enable to output in Low-Z	^tLZCE	4		5		5		5		ns	7
Chip disable to output in High-Z	^tHZCE		6		6		8		8	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		ns	
Chip disable to power-down time	^tPD		12		15		20		25	ns	
Output Enable access time	^tAOE		6		8		10		12	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		ns	
Output disable to output in High-Z	^tHZOE		6		6		8		8	ns	6
WRITE Cycle											
WRITE cycle time	^tWC	12		15		20		25		ns	
Chip Enable to end of write	^tCW	10		12		13		15		ns	
Address valid to end of write	^tAW	8		9		12		14		ns	
Address setup time	^tAS	0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		ns	
WRITE pulse width	$^tWP1$	8		9		10		12		ns	
WRITE pulse width	$^tWP2$	8		9		10		12		ns	
Data setup time	^tDS	6		8		10		10		ns	
Data hold time	^tDH	0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	1		1		1		1		ns	7
Write Enable to output in High-Z	^tHZWE		6		6		8		8	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

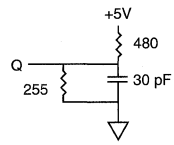


Fig. 1 OUTPUT LOAD EQUIVALENT

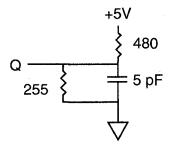


Fig. 2 OUTPUT LOAD EQUIVALENT

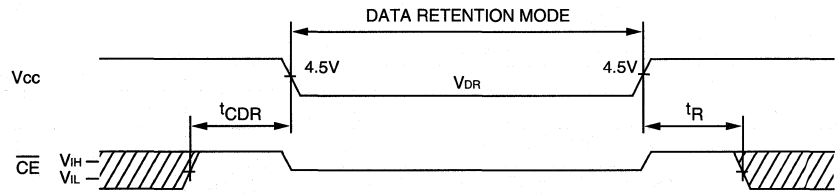
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < $^{t}RC/2$.
3. Icc is dependent on output loading and cycle rates. The specified value applies with the outputs unloaded, and $f = \frac{1}{^{t}RC\ (MIN)}$ Hz.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. $^{t}HZCE$, $^{t}HZOE$ and $^{t}HZWE$ are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, $^{t}HZCE$ is less than $^{t}LZCE$, and $^{t}HZWE$ is less than $^{t}LZWE$.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. Chip enable and output enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Contact Micron for IT/AT/XT timing and current specifications; they may differ from the commercial temperature range specifications shown in this data sheet.
14. Typical currents are measured at 25°C.
15. Output enable ($\overline{OE}$) is inactive (HIGH).
16. Output enable ($\overline{OE}$) is active (LOW).

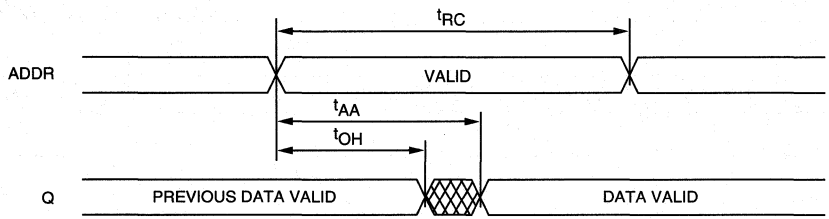
DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2			V	
Data Retention Current L version	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	ICCDR		TBD	TBD	µA	14
		Vcc = 3V	ICCDR		TBD	TBD	µA	14
Chip Deselect to Data Retention Time			^{t}CDR	0			ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

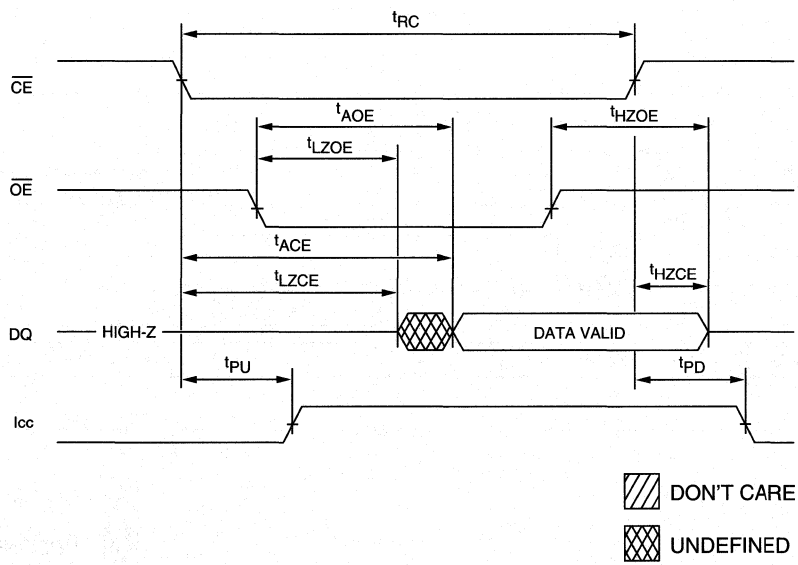
LOW Vcc DATA RETENTION WAVEFORM



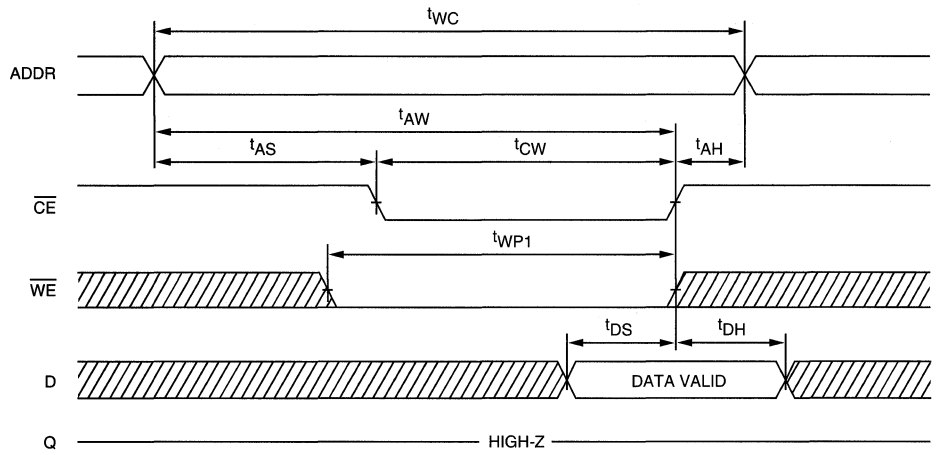
READ CYCLE NO. 1 [8, 9]



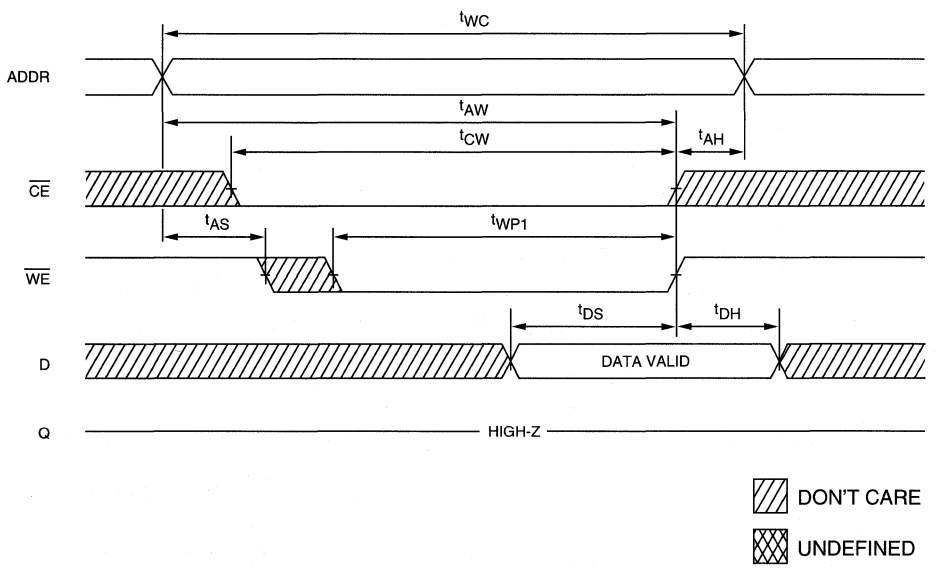
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)

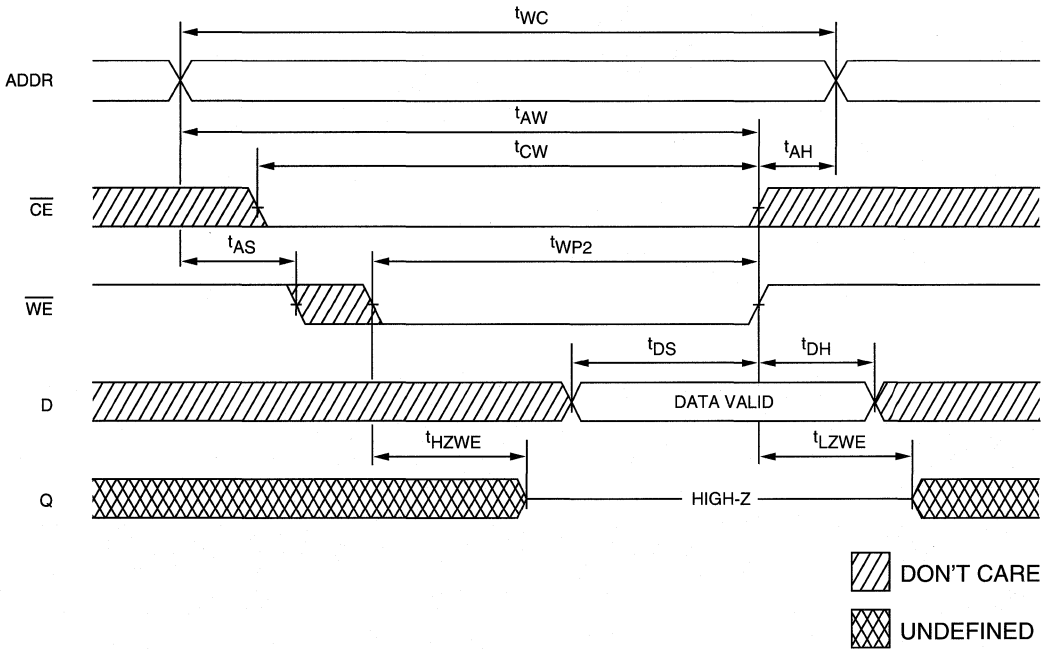


WRITE CYCLE NO. 2 [12, 15]
(Write Enable Controlled)



WRITE CYCLE NO. 3 [7, 12, 16]

(Write Enable Controlled)



MICRON SEMICONDUCTOR, INC.

MT5C256K4A1
REVOLUTIONARY PINOUT 256K x 4 SRAM

SRAM

1 MEG x 4 SRAM

WITH OUTPUT ENABLE

FEATURES

- High speed: 12, 15, 20, 25 and 35ns
- High-performance, low-power, CMOS double-metal process
- Multiple center power and ground pins for improved noise immunity
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- All inputs and outputs are TTL-compatible
- Fast $\overline{OE}$ access time: 6, 8, 10, 12 and 15ns

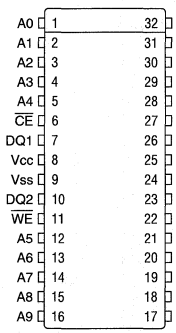
OPTIONS / MARKING

- Timing
  - 12ns access: -12
  - 15ns access: -15
  - 20ns access: -20
  - 25ns access: -25
  - 35ns access: -35
- Packages
  - Plastic SOJ (400 mil): DJ
  - Plastic TSOP (400 mil): TG
- 2V data retention: L
- Low power: P
- Temperature
  - Commercial (0°C to +70°C): None
  - Industrial (-40°C to +85°C): IT
  - Automotive (-40°C to +125°C): AT
  - Extended (-55°C to +125°C): XT
- Part Number Example: MT5C1M4B2DJ-35 L

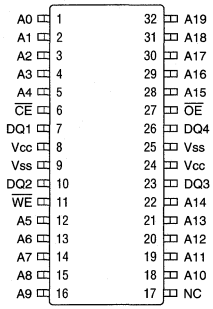
NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

32-Pin SOJ (SD-5)



32-Pin TSOP (SE-1)



GENERAL DESCRIPTION

The MT5C1M4B2 is organized as a 1,048,576 x 4 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron 4 Meg SRAMs are fabricated using double-layer metal, triple-layer polysilicon technology.

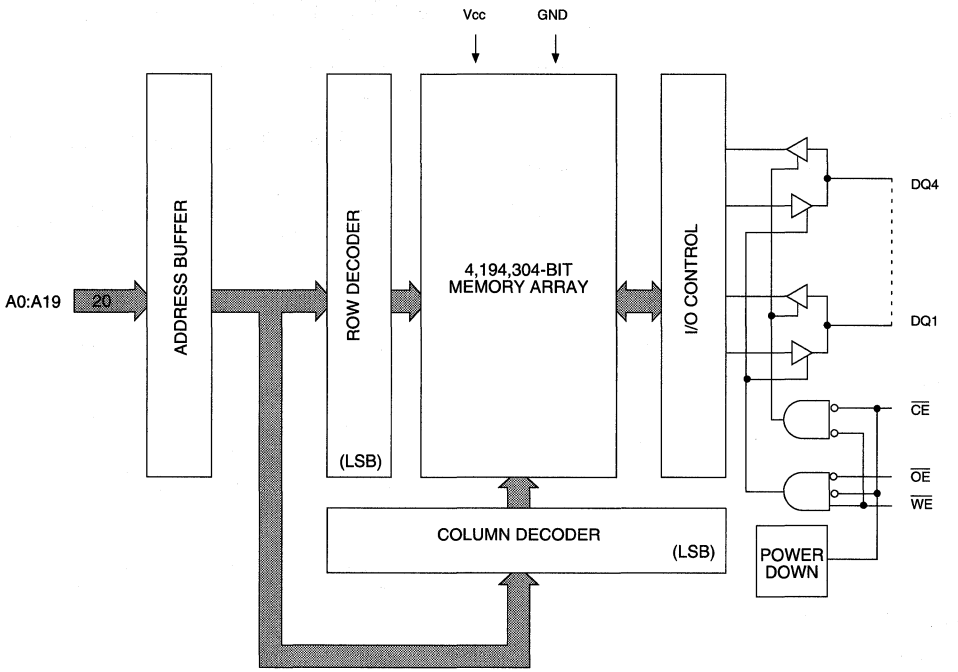
This device offers multiple center power and ground pins for improved performance. For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) with this configuration. These enhancements can place the outputs in High-Z for additional flexibility in system design.

Writing to this device is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH while output enable ($\overline{OE}$) and $\overline{CE}$ go LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

The "P" version provides a 90 percent reduction in TTL standby current (I_{SB1}) through the use of gated inputs on the $\overline{WE}$, $\overline{OE}$ and address lines, which also facilitates the design of battery backed systems. That is, the gated inputs simplify the design effort and circuitry required to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL-compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

THERMAL IMPEDENCE (EST)[16]

PACKAGE	NUMBER OF PINS	θ_{JC}* (°C/W)	θ_{JA}* (°C/W)
SOJ	32	15	60
TSOP	32	5	70

*The thermal impedence numbers assume the device is socketted on a PC board and air flow is zero.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Storage Temperature (plastic) ..... -55°C to +150°C
Short Circuit Output Current 50mA
Voltage on any pin relative to V_{SS} ..... -1V to V_{CC}+1
Junction Temperature** ..... +150°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Maximum junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow. See the Application Information section at the end of this data sheet for more information.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-2	2	µA	
Output Leakage Current	Output(s) disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-2	2	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

			MAX						
DESCRIPTION	CONDITIONS	SYMBOL	-12	-15	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	200	180	175	170	160	mA	3
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	35	30	25	25	20	mA	
	P version only	I_{SB1}	2	2	2	2	2	mA	
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	2	2	2	2	2	mA	
	P version only	I_{SB2}	2	2	2	2	2	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	5	pF	4
Output Capacitance	V_{CC} = 5V	C_O	7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 5, 13) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION		-12		-15		-20		-25		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle													
READ cycle time	^tRC	12		15		20		25		35		ns	
Address access time	^tAA		12		15		20		25		35	ns	
Chip Enable access time	^tACE		12		15		20		25		35	ns	
Output hold from address change	^tOH	3		3		3		3		3		ns	
Chip Enable to output in Low-Z	^tLZCE	3		3		5		5		5		ns	7
Chip disable to output in High-Z	^tHZCE		6		7		8		10		15	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		0		ns	
Chip disable to power-down time	^tPD		12		15		20		25		35	ns	
Output Enable access time	^tAOE		6		8		10		12		15	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		0		ns	
Output disable to output in High-Z	^tHZOE		5		6		7		10		12	ns	6
WRITE Cycle													
WRITE cycle time	^tWC	12		15		20		25		35		ns	
Chip Enable to end of write	^tCW	8		10		12		15		20		ns	
Address valid to end of write	^tAW	8		10		12		15		20		ns	
Address setup time	^tAS	0		0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		0		ns	
WRITE pulse width	$^tWP1$	8		9		10		15		20		ns	
WRITE pulse width	$^tWP2$	9		11		12		17		22		ns	
Data setup time	^tDS	6		7		8		10		15		ns	
Data hold time	^tDH	0		0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	3		3		4		5		5		ns	7
Write Enable to output in High-Z	^tHZWE		5		6		8		10		15	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

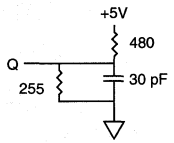


Fig. 1 OUTPUT LOAD EQUIVALENT

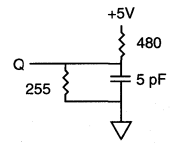


Fig. 2 OUTPUT LOAD EQUIVALENT

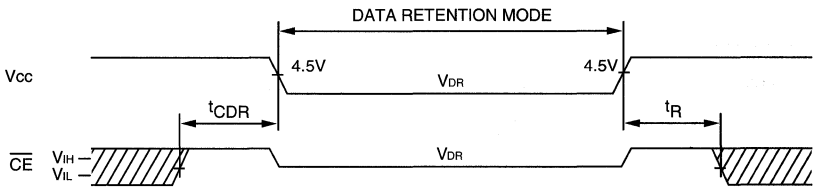
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZOE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE, and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. Chip enable and output enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Contact Micron for IT/AT/XT timing and current specifications; they may differ from the commercial temperature range specifications shown in this data sheet.
14. Output enable ($\overline{OE}$) is inactive (HIGH).
15. Output enable ($\overline{OE}$) is active (LOW).
16. Micron does not warrant functionality nor reliability of any product in which the junction temperature exceeds 150°C. Care should be taken to limit power to acceptable levels.

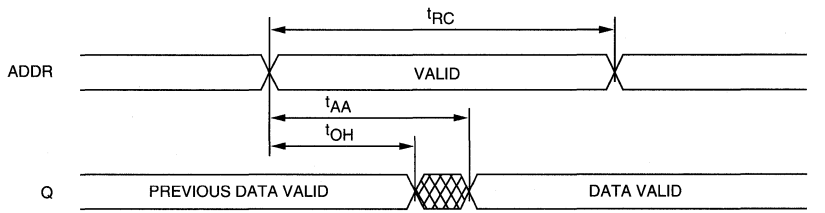
DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP versions only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2		V	
Data Retention Current L version	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	ICCDR		1	mA	
		Vcc = 3V	ICCDR		1.5	mA	
Data Retention Current LP version	$\overline{CE}$ ≥ (Vcc -0.2V)	Vcc = 2V	ICCDR		1	mA	
		Vcc = 3V	ICCDR		1.5	mA	
Chip Deselect to Data Retention Time			^{t}CDR	0		ns	4
Operation Recovery Time			^{t}R	^{t}RC		ns	4, 11

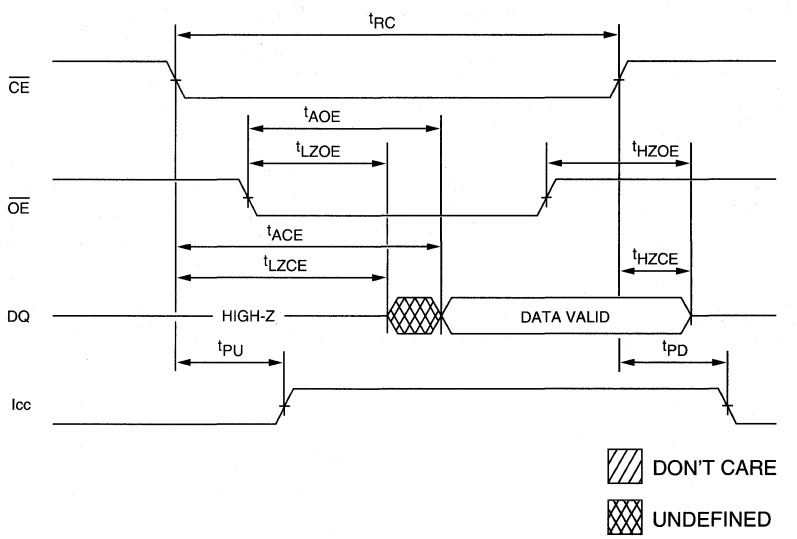
LOW Vcc DATA RETENTION WAVEFORM



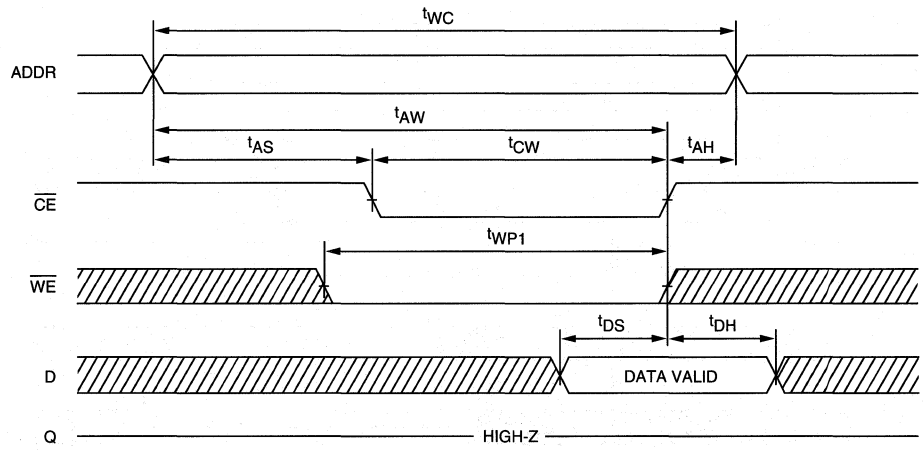
READ CYCLE NO. 1 [8, 9]



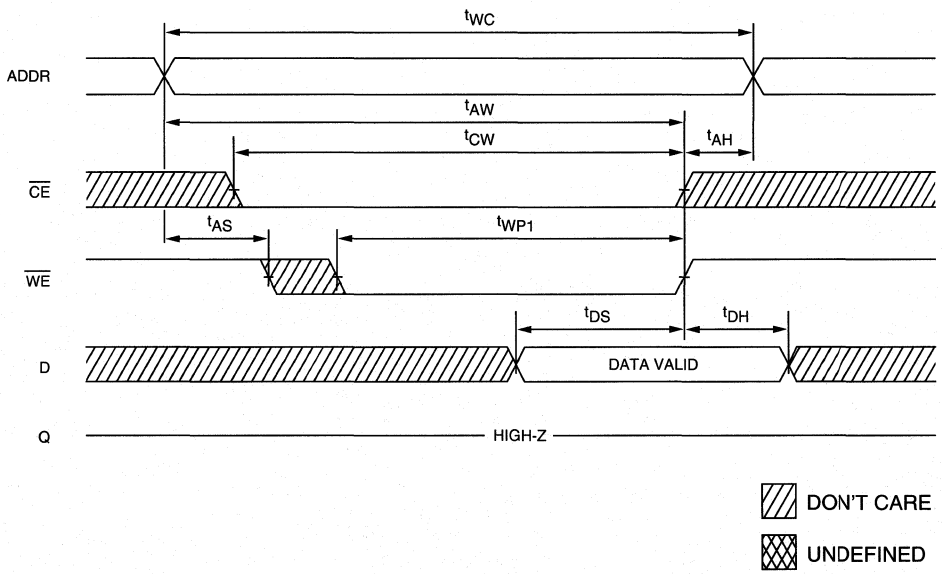
READ CYCLE NO. 2 [7, 8, 10]



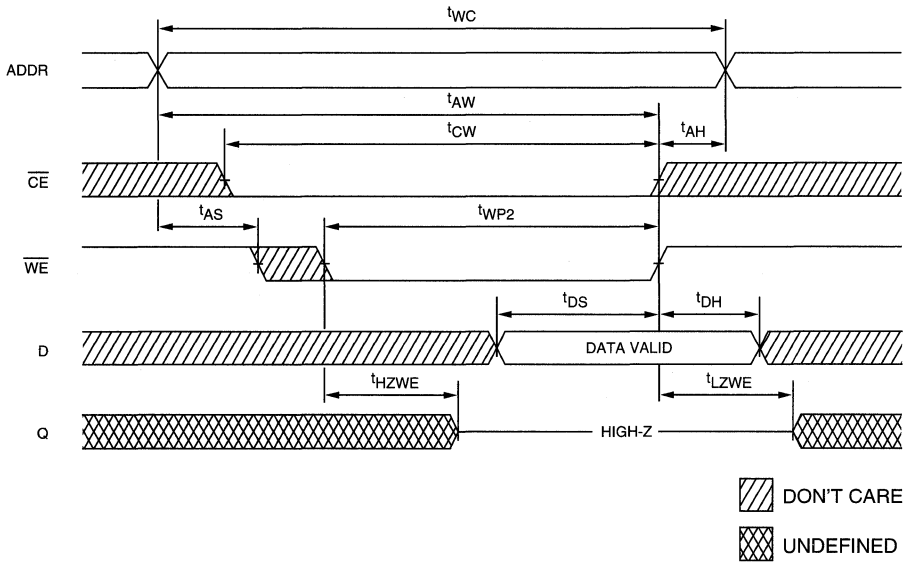
WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)



WRITE CYCLE NO. 2 [12, 14]
(Write Enable Controlled)



WRITE CYCLE NO. 3 [7, 12, 15]
(Write Enable Controlled)



APPLICATION INFORMATION

THERMAL CONSIDERATIONS

This section describes how to determine the junction temperature during operating conditions. It is essential that the maximum junction temperature of the 4 Meg SRAM is not exceeded. If this temperature is exceeded it is necessary to add external cooling such as forced airflow or change the operating conditions. The maximum junction temperature for Micron SRAMs is 150°C. The limiting temperature factor is not the SRAM but the mold compound which prevents reliable operating temperatures significantly about 150°C. However, it is advisable to run the part as cool as possible since reliability (FIT rates) are exponentially dependent upon junction temperature.

The calculation of the actual junction temperature begins with the power calculation and then the junction temperation calculation. Equations 1 and 2 below show how T_j is determined using the ambient temperature, thermal resistance and operating power. If an airflow is introduced into a system then Equation 2 should be used with an airflow thermal multiplier. Specific thermal resistances are given in Micron technical note "SRAM Thermal Design Considerations" and in individual data sheets.

$$T_j = T_A + P * \theta_{JA} \quad (1)$$

$$T_j = T_A + P * \theta_{JA} * \theta_M \quad (2)$$

T_j = Junction temperature of the active portion of the silicon die (°C)
T_A = Ambient air temperature (°C) at which the device is operated
P = Average power dissipation of the device (W)
θ_{JA} = Junction to ambient thermal resistance (°C/W)
θ_M = Airflow multiplier. This value changes for different values of airflow over the part (fpm).

To solve the above equations the average operating power must be calculated. Total power has three separate components (P_1, P_2 and P_3). P_1 is the operating power dissipated by the chip, P_2 is the AC output power due to the capacitive load and P_3 is the DC output power due to TTL DC load current (P_3 is usually negligible). For this example we have chosen P_2 such that outputs are switching from a logic LOW state to a logic HIGH state which gives the worst case output AC current. A complete description of these equations and their derivation is given in Micron technical note "Design Tips: 32K x 36 SRAM."

$$P_1 = V_{CC} I_{CC}$$

$$P_2 = \frac{C_L}{T} (V_{CC} [V_{OH} - V_{OL}] - 0.5 [V_{OH}^2 - V_{OL}^2]) N_S$$

$$P_3 = (V_{CC} - V_{OH}) I_O N_H + V_{OL} I_I N_L.$$

V_{CC} = Supply voltage
I_{CC} = Supply current
C_L = Capacitive output loading
T = Clock period
V_{OH} = Output high voltage
V_{OL} = Output low voltage
I_O = Output current on DQ lines which are high
I_I = Input current on DQ lines which are low
N_H = Number of DQ lines which are high
N_L = Number of DQ lines which are low.

Table 1
EFFECTS OF AIRFLOW ON 4 MEG SRAM SOJ PACKAGES

Package	Air Flow	θ_M Multiplier
PSOJ	200 fpm	0.7 - 0.75
PSOJ	500 fpm	0.55 - 0.65

ADDITIONAL INFORMATION

For more information on thermal considerations see Micron's technical notes, "SRAM Thermal Design Considerations" and "Design Tips: 32K x 36 SRAM." These notes explain how to calculate thermal resistance and how to improve thermal performance in much greater detail. Also available is Micron's *Quality and Reliability Handbook,* which gives an explanation of how thermal impedances are calculated.

SRAM

2K x 8 SRAM

FEATURES

- High speed: 9, 10, 12, 15, 20 and 25ns
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- All inputs and outputs are TTL-compatible

OPTIONS

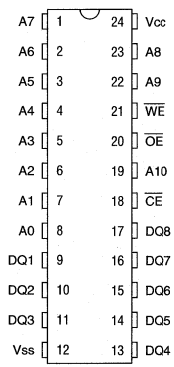
	MARKING
• Timing	
9ns access	- 9
10ns access	-10
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
• Packages	
Plastic DIP (300 mil)	None
Plastic SOJ (300 mil)	DJ
• 2V data retention	L
• Temperature	
Commercial (0°C to +70°C)	None
Industrial (-40°C to +85°C)	IT
Automotive (-40°C to +125°C)	AT
Extended (-55°C to +125°C)	XT

- Part Number Example: MT5C1608DJ-15 IT

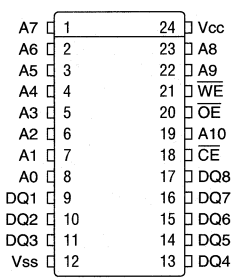
NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

24-Pin DIP
(SA-3)



24-Pin SOJ
(SD-1)



GENERAL DESCRIPTION

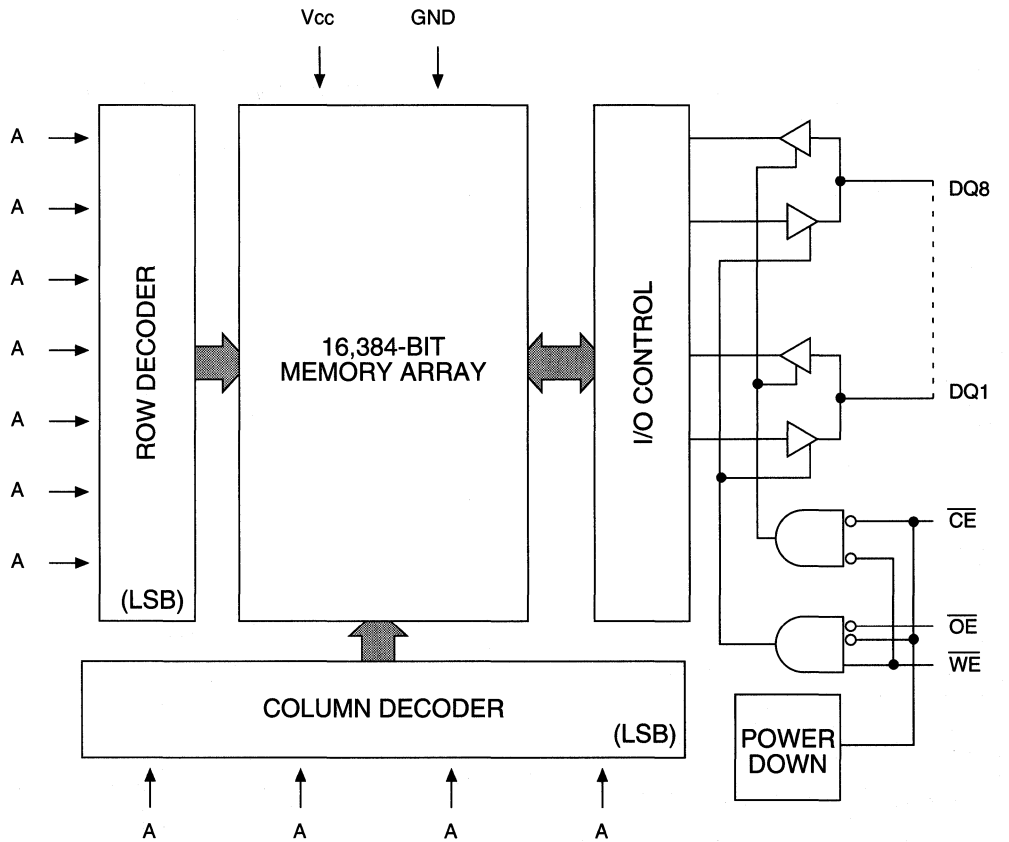
The MT5C1608 is organized as a 2,048 x 8 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) with this organization. This enhancement can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{OE}$ and $\overline{CE}$ go LOW. The device offers a reduced power standby mode when disabled. This allows system designers to achieve their low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL-compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA
Voltage on Any Pin Relative to V_{SS} ..... -1V to V_{CC} +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; V_{CC} = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

				MAX							
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-9	-10	-12	-15	-20	-25	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	125	190	185	175	165	140	130	mA	3, 13
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	22	60	50	45	40	35	35	mA	13
	$\overline{CE} \ge V_{CC}$ -0.2V; V_{CC} = MAX $V_{IN} \le V_{SS}$ +0.2V or $V_{IN} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	0.5	3	3	3	3	3	5	mA	13

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	5	pF	4
Output Capacitance	V_{CC} = 5V	C_O	7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION		-9		-10		-12		-15		-20		-25			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle															
READ cycle time	^tRC	9		10		12		15		20		25		ns	
Address access time	^tAA		9		10		12		15		20		25	ns	
Chip Enable access time	^tACE		9		9		10		12		15		20	ns	
Output hold from address change	^tOH	3		3		3		3		3		3		ns	
Chip Enable to output in Low-Z	^tLZCE	2		2		2		2		2		2		ns	7, 14
Chip disable to output in High-Z	^tHZCE		5		5		6		7		8		8	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		0		0		ns	
Chip disable to power-down time	^tPD		9		10		12		15		20		25	ns	
Output Enable access time	^tAOE		4.5		5		6		7		8		8	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		0		0		ns	
Output disable to output in High-Z	^tHZOE		4.5		5		5		6		7		8	ns	6
WRITE Cycle															
WRITE cycle time	^tWC	9		10		12		15		20		25		ns	
Chip Enable to end of write	^tCW	7		8		10		12		15		20		ns	
Address valid to end of write	^tAW	7		8		10		12		15		20		ns	
Address setup time	^tAS	0		0		0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		0		0		ns	
WRITE pulse width	$^tWP1$	6		7		8		10		12		15		ns	
WRITE pulse width	$^tWP2$	8		9		10		14		18		20		ns	
Data setup time	^tDS	5		6		7		8		9		10		ns	
Data hold time	^tDH	1		1		1		1		1		1		ns	
Write disable to output in Low-Z	^tLZWE	2		2		2		2		2		2		ns	7
Write Enable to output in High-Z	^tHZWE		4		5		5		6		8		8	ns	6, 7

INDUSTRIAL TEMPERATURE SPECIFICATIONS (IT)

The following specifications are to be used for Industrial Temperature (IT) MT5C1608 SRAMs.
(-40°C ≤ T_A ≤ 85°C)

			MAX						
DESCRIPTION	**CONDITIONS**	**SYMBOL**	**-10**	**-12**	**-15**	**-20**	**-25**	**UNITS**	**NOTES**
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	195	185	175	150	140	mA	3, 13
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	60	50	45	40	40	mA	13
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	5	5	5	5	5	mA	13

DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	**CONDITIONS**		**SYMBOL**	**TYP**	**MAX**	**UNITS**	**NOTES**
Data Retention Current	$\overline{CE}$ ≥ (V_{CC} -0.2V) V_{IN} ≥ (V_{CC} -0.2V) or ≤ 0.2V	V_{CC} = 2V	I_{CCDR}	130	300	µA	14
		V_{CC} = 3V	I_{CCDR}	210	550	µA	14

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

Refer to commercial temperature timing parameters for specifications not listed here.
(Notes 5, 14) (-40°C ≤ T_A ≤ 85°C)

DESCRIPTION		-12		-15		-20		-25			
	SYM	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ Cycle											
Output hold from address change	^tOH	2		2		2		2		ns	
Chip Enable to output in Low-Z	^tLZCE	1		1		1		1		ns	7
WRITE Cycle											
Write disable to output in Low-Z	^tLZWE	1		1		1		1		ns	7

AUTOMOTIVE AND EXTENDED TEMPERATURE SPECIFICATIONS (AT AND XT)

The following specifications are to be used for Automotive Temperature (AT) and Extended Temperature (XT) MT5C1608 SRAMs. (-40°C ≤ T_A ≤ 125°C - AT) (-55°C ≤ T_A ≤ 125°C - XT)

			MAX					
DESCRIPTION	**CONDITIONS**	**SYMBOL**	**-12**	**-15**	**-20**	**-25**	**UNITS**	**NOTES**
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	185	175	150	140	mA	3, 13
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	50	45	40	40	mA	13
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	5	5	5	5	mA	13

DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	**CONDITIONS**		**SYMBOL**	**TYP**	**MAX**	**UNITS**	**NOTES**
Data Retention Current	$\overline{CE}$ ≥ (V_{CC} -0.2V) V_{IN} ≥ (V_{CC} -0.2V) or ≤ 0.2V	V_{CC} = 2V	I_{CCDR}	130	300	µA	14
		V_{CC} = 3V	I_{CCDR}	210	550	µA	14

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

Refer to commercial temperature timing parameters for specifications not listed here.
(Notes 5, 14) (-40°C ≤ T_A ≤ 125°C; -55°C ≤ T_A ≤ 125°C; V_{CC} = 5V ±10%)

DESCRIPTION		-12		-15		-20		-25			
	SYM	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ Cycle											
Output hold from address change	^tOH	2		2		2		2		ns	
Chip Enable to output in Low-Z	^tLZCE	1		1		1		1		ns	7
WRITE Cycle											
Write disable to output in Low-Z	^tLZWE	1		1		1		1		ns	7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

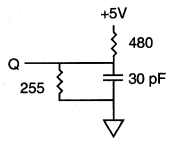


Fig. 1 OUTPUT LOAD EQUIVALENT

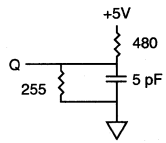


Fig. 2 OUTPUT LOAD EQUIVALENT

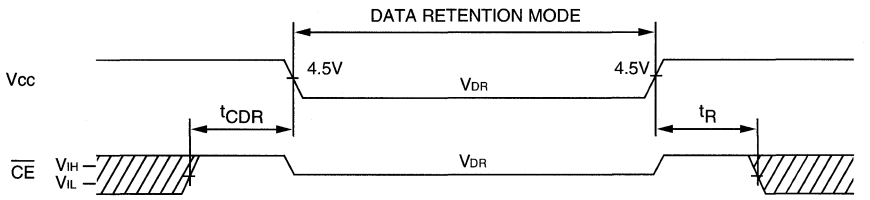
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZWE and ^{t}HZOE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Typical values are measured at 5V, 25°C and 15ns cycle time.
14. Typical currents are measured at 25°C.
15. Output enable ($\overline{OE}$) is inactive (HIGH).
16. Output enable ($\overline{OE}$) is active (LOW).

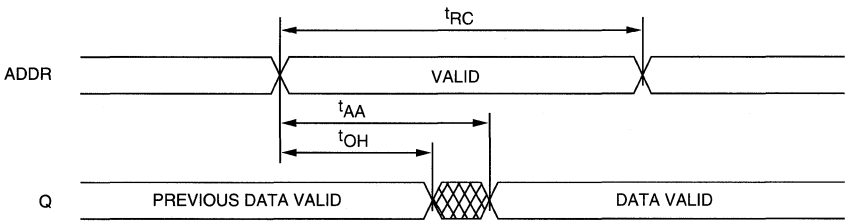
DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			V_{DR}	2			V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	I_{CCDR}		130	300	µA	14
		Vcc = 3V	I_{CCDR}		210	400	µA	14
Chip Deselect to Data Retention Time			^{t}CDR	0			ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

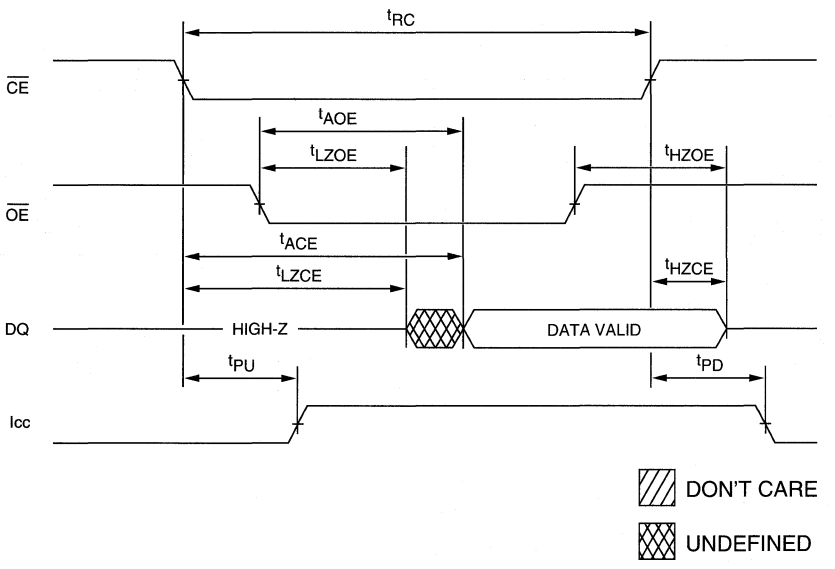
LOW Vcc DATA RETENTION WAVEFORM



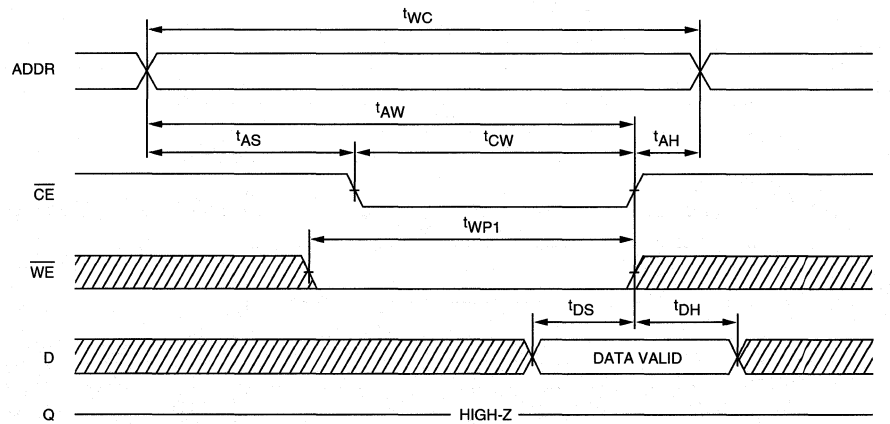
READ CYCLE NO. 1 [8, 9]



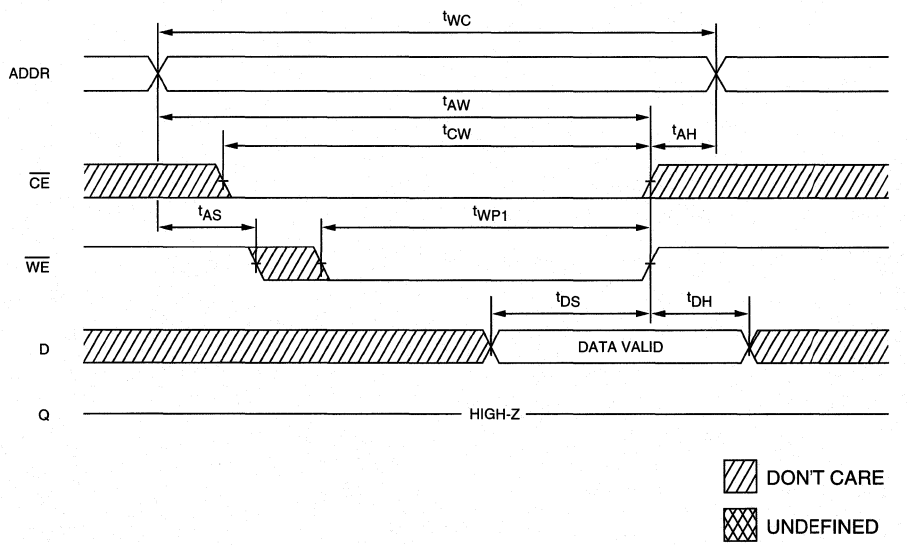
READ CYCLE NO. 2 [7, 8, 10]



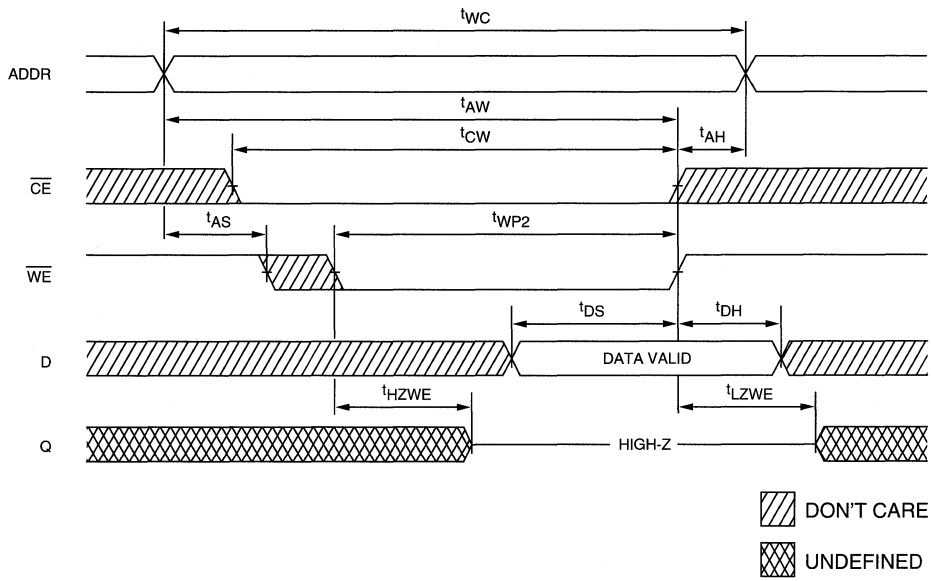
WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)



WRITE CYCLE NO. 2 [12, 15]
(Write Enable Controlled)



WRITE CYCLE NO. 3 [7, 12, 16]
(Write Enable Controlled)



SRAM

8K x 8 SRAM

FEATURES

- High speed: 9, 10, 12, 15, 20 and 25ns
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE1}$, CE2 and $\overline{OE}$ options
- All inputs and outputs are TTL-compatible

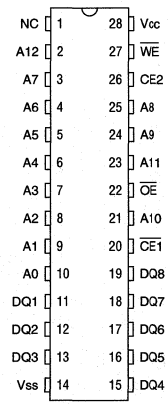
OPTIONS — MARKING

- Timing
  - 9ns access — -9
  - 10ns access — -10
  - 12ns access — -12
  - 15ns access — -15
  - 20ns access — -20
  - 25ns access — -25
- Packages
  - Plastic DIP (300 mil) — None
  - Plastic SOJ (300 mil) — DJ
- 2V data retention — L
- Temperature
  - Commercial (0°C to +70°C) — None
  - Industrial (-40°C to +85°C) — IT
  - Automotive (-40°C to +125°C) — AT
  - Extended (-55°C to +125°C) — XT
- Part Number Example: MT5C6408DJ-15 AT

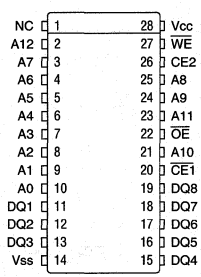
NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

28-Pin DIP (SA-4)



28-Pin SOJ (SD-2)



GENERAL DESCRIPTION

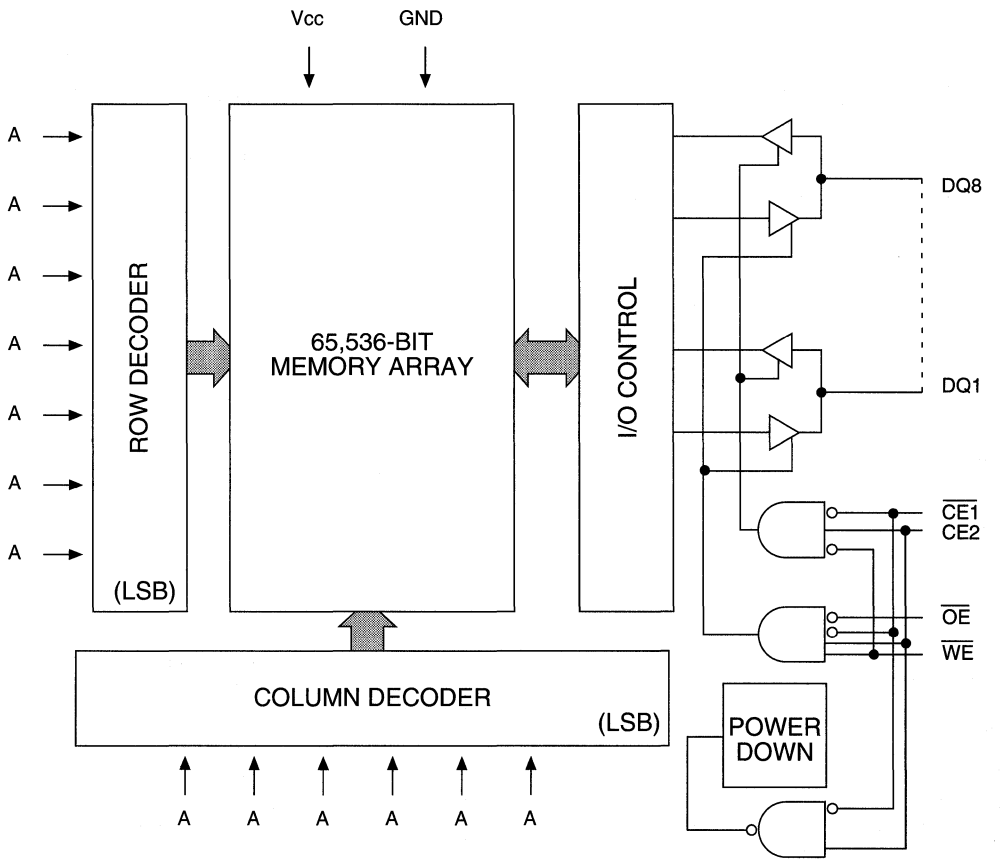
The MT5C6408 is organized as a 8,192 x 8 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high-speed memory applications, Micron offers two chip enables and an output enable on the x8 organizations. This enhancement can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE1}$ inputs are LOW and CE2 is HIGH. Reading is accomplished when $\overline{WE}$ and CE2 remain HIGH and $\overline{CE}$ and $\overline{OE}$ go LOW. The device offers a reduced power standby mode when disabled. This allows system designers to achieve their low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL-compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE1}$	CE2	$\overline{WE}$	$\overline{OE}$	DQ	POWER
STANDBY	H	X	X	X	HIGH-Z	STANDBY
STANDBY	X	L	X	X	HIGH-Z	STANDBY
READ	L	H	H	L	Q	ACTIVE
NOT SELECTED	L	H	H	H	HIGH-Z	ACTIVE
WRITE	L	H	L	X	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1V to +7V
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA
Voltage on Any Pin Relative to V_{SS} ..... -1V to V_{CC} +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

				MAX							
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-9	-10	-12	-15	-20	-25	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	125	190	185	175	165	140	130	mA	3, 14
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	22	60	50	45	40	35	35	mA	14
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	0.5	3	3	3	3	3	5	mA	14

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	5	pF	4
Output Capacitance	V_{CC} = 5V	C_O	7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION		-9		-10		-12		-15		-20		-25			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle															
READ cycle time	^tRC	9		10		12		15		20		25		ns	
Address access time	^tAA		9		10		12		15		20		25	ns	
Chip Enable access time	^tACE		9		9		10		12		15		20	ns	
Output hold from address change	^tOH	3		3		3		3		3		3		ns	
Chip Enable to output in Low-Z	^tLZCE	2		2		2		2		2		2		ns	7, 15
Chip disable to output in High-Z	^tHZCE		5		5		6		7		8		8	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		0		0		ns	
Chip disable to power-down time	^tPD		9		10		12		15		20		25	ns	
Output Enable access time	^tAOE		4.5		5		6		7		8		8	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		0		0		ns	
Output disable to output in High-Z	^tHZOE		4.5		5		5		6		7		8	ns	6
WRITE Cycle															
WRITE cycle time	^tWC	9		10		12		15		20		25		ns	
Chip Enable to end of write	^tCW	7		8		10		12		15		20		ns	
Address valid to end of write	^tAW	7		8		10		12		15		20		ns	
Address setup time	^tAS	0		0		0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		0		0		ns	
WRITE pulse width	$^tWP1$	6		7		8		10		12		15		ns	
WRITE pulse width	$^tWP2$	8		9		10		14		18		20		ns	
Data setup time	^tDS	5		6		7		8		9		10		ns	
Data hold time	^tDH	1		1		1		1		1		1		ns	
Write disable to output in Low-Z	^tLZWE	2		2		2		2		2		2		ns	7
Write Enable to output in High-Z	^tHZWE		4		5		5		6		8		8	ns	6, 7

INDUSTRIAL TEMPERATURE SPECIFICATIONS (IT)

The following specifications are to be used for Industrial Temperature (IT) MT5C6408 SRAMs.
(-40°C ≤ T_A ≤ 85°C)

			MAX						
DESCRIPTION	**CONDITIONS**	**SYMBOL**	**-10**	**-12**	**-15**	**-20**	**-25**	**UNITS**	**NOTES**
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	195	185	175	150	140	mA	3, 13
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	60	50	45	40	40	mA	13
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	5	5	5	5	5	mA	13

DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	**CONDITIONS**		**SYMBOL**	**TYP**	**MAX**	**UNITS**	**NOTES**
Data Retention Current	$\overline{CE}$ ≥ (V_{CC} -0.2V) V_{IN} ≥ (V_{CC} -0.2V) or ≤ 0.2V	V_{CC} = 2V	I_{CCDR}	130	300	µA	14
		V_{CC} = 3V	I_{CCDR}	210	550	µA	14

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

Refer to commercial temperature timing parameters for specifications not listed here.
(Notes 5, 14) (-40°C ≤ T_A ≤ 85°C)

DESCRIPTION		-12		-15		-20		-25			
	SYM	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ Cycle											
Output hold from address change	^tOH	2		2		2		2		ns	
Chip Enable to output in Low-Z	^tLZCE	1		1		1		1		ns	7
WRITE Cycle											
Write disable to output in Low-Z	^tLZWE	1		1		1		1		ns	7

AUTOMOTIVE AND EXTENDED TEMPERATURE SPECIFICATIONS (AT AND XT)

The following specifications are to be used for Automotive Temperature (AT) and Extended Temperature (XT) MT5C6408 SRAMs. (-40°C ≤ T_A ≤ 125°C - AT) (-55°C ≤ T_A ≤ 125°C - XT)

			MAX					
DESCRIPTION	**CONDITIONS**	**SYMBOL**	**-12**	**-15**	**-20**	**-25**	**UNITS**	**NOTES**
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	185	175	150	140	mA	3, 13
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	50	45	40	40	mA	13
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	5	5	5	5	mA	13

DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	**CONDITIONS**		**SYMBOL**	**TYP**	**MAX**	**UNITS**	**NOTES**
Data Retention Current	$\overline{CE}$ ≥ (V_{CC} -0.2V) V_{IN} ≥ (V_{CC} -0.2V) or ≤ 0.2V	V_{CC} = 2V	I_{CCDR}	130	300	µA	14
		V_{CC} = 3V	I_{CCDR}	210	550	µA	14

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

Refer to commercial temperature timing parameters for specifications not listed here.
(Notes 5, 14) (-40°C ≤ T_A ≤ 125°C; -55°C ≤ T_A ≤ 125°C; V_{CC} = 5V ±10%)

DESCRIPTION		-12		-15		-20		-25			
	SYM	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ Cycle											
Output hold from address change	^tOH	2		2		2		2		ns	
Chip Enable to output in Low-Z	^tLZCE	1		1		1		1		ns	7
WRITE Cycle											
Write disable to output in Low-Z	^tLZWE	1		1		1		1		ns	7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

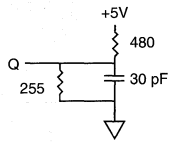


Fig. 1 OUTPUT LOAD EQUIVALENT

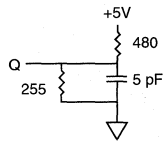


Fig. 2 OUTPUT LOAD EQUIVALENT

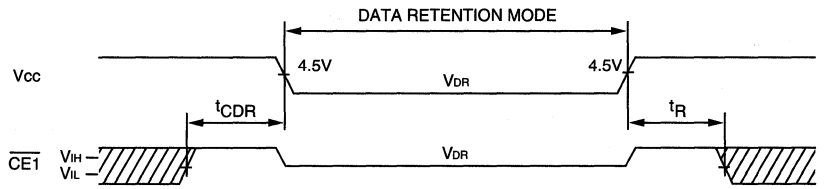
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZWE and ^{t}HZOE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. CE2 timing is the same as $\overline{CE1}$ timing. The wave is inverted.
13. Chip enable and write enable can initiate and terminate a WRITE cycle.
14. Typical values are measured at 5V, 25°C and 15ns cycle time.
15. Typical currents are measured at 25°C.
16. Output enable ($\overline{OE}$) is inactive (HIGH).
17. Output enable ($\overline{OE}$) is active (LOW).

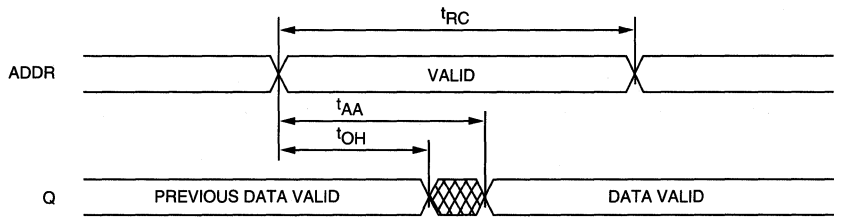
DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2			V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	ICCDR		130	300	µA	15
		Vcc = 3V	ICCDR		210	400	µA	15
Chip Deselect to Data Retention Time			^{t}CDR	0			ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

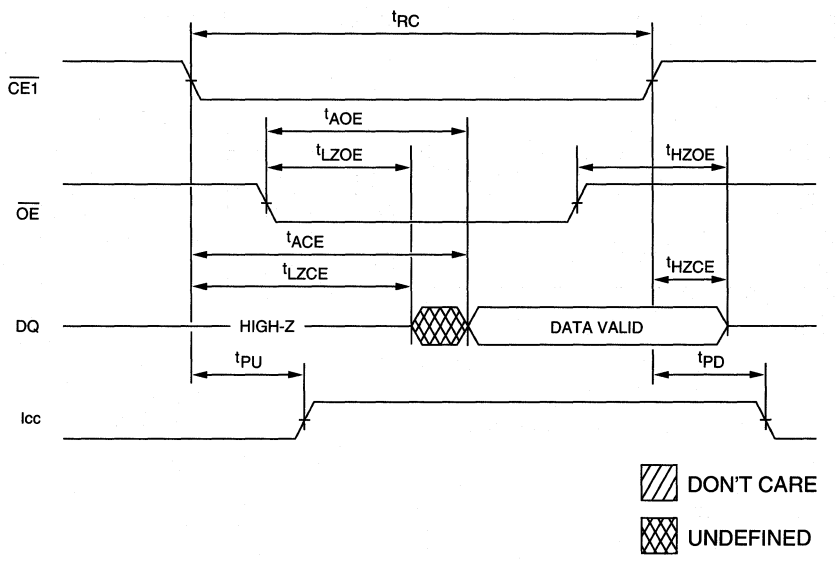
LOW Vcc DATA RETENTION WAVEFORM [12]



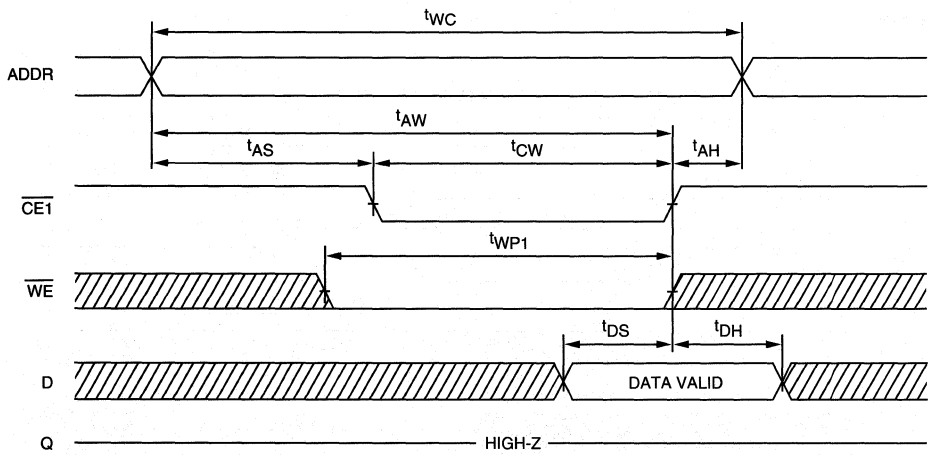
READ CYCLE NO. 1 [8, 9]



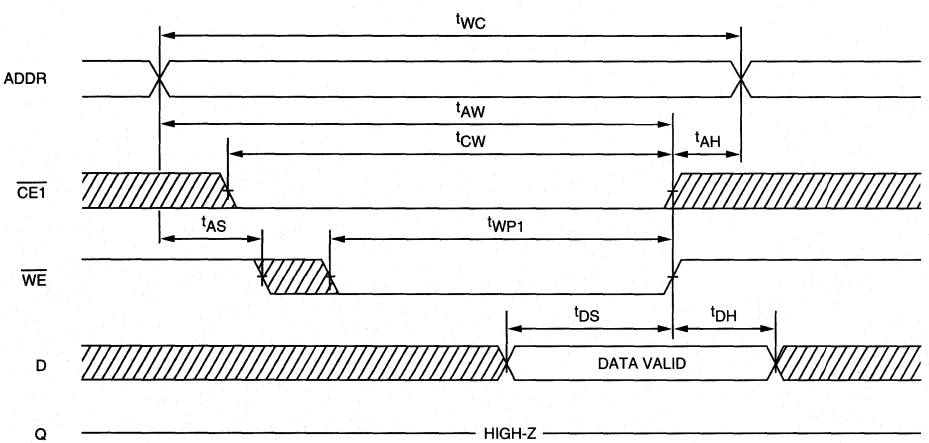
READ CYCLE NO. 2 [7, 8, 10, 12]

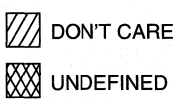


WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)

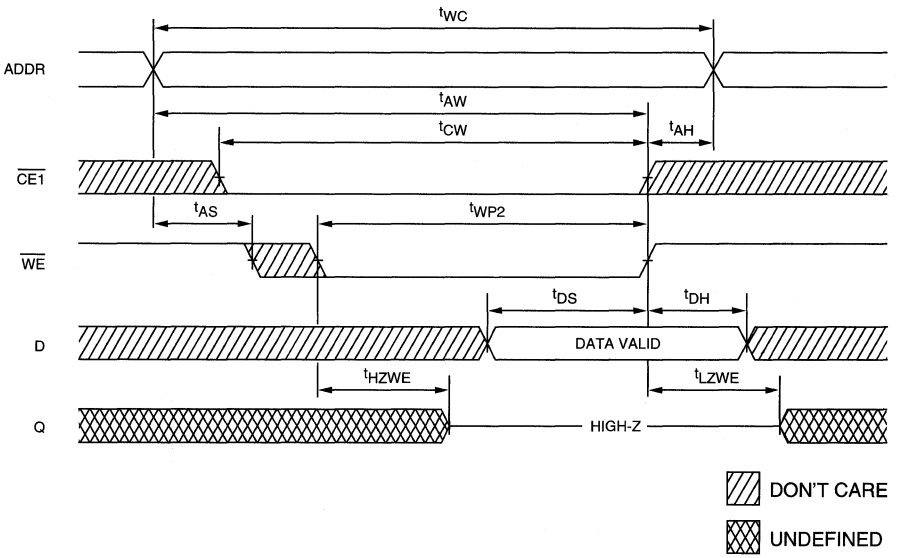


WRITE CYCLE NO. 2 [12, 13, 16]
(Write Enable Controlled)





WRITE CYCLE NO. 3 [7, 12, 13, 17]
(Write Enable Controlled)



SRAM

32K x 8 SRAM

FEATURES

- High speed: 10, 12, 15, 20, 25 and 35ns
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- All inputs and outputs are TTL-compatible

OPTIONS — MARKING

- Timing

10ns access	-10
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
35ns access	-35

- Packages

Plastic DIP (300 mil)	None
Plastic SOJ (300 mil)	DJ

- 2V data retention — L
- Low power — P
- Temperature

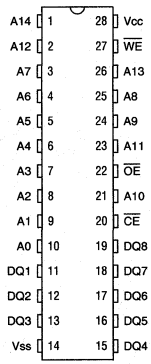
Commercial	(0°C to +70°C)	None
Industrial	(-40°C to +85°C)	IT
Automotive	(-40°C to +125°C)	AT
Extended	(-55°C to +125°C)	XT

- Part Number Example: MT5C2568DJ-20 IT

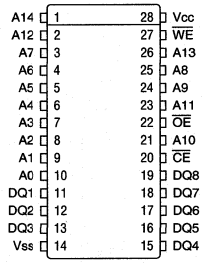
NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

28-Pin DIP (SA-4)



28-Pin SOJ (SD-2)



GENERAL DESCRIPTION

The MT5C2568 is organized as a 32,768 x 8 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

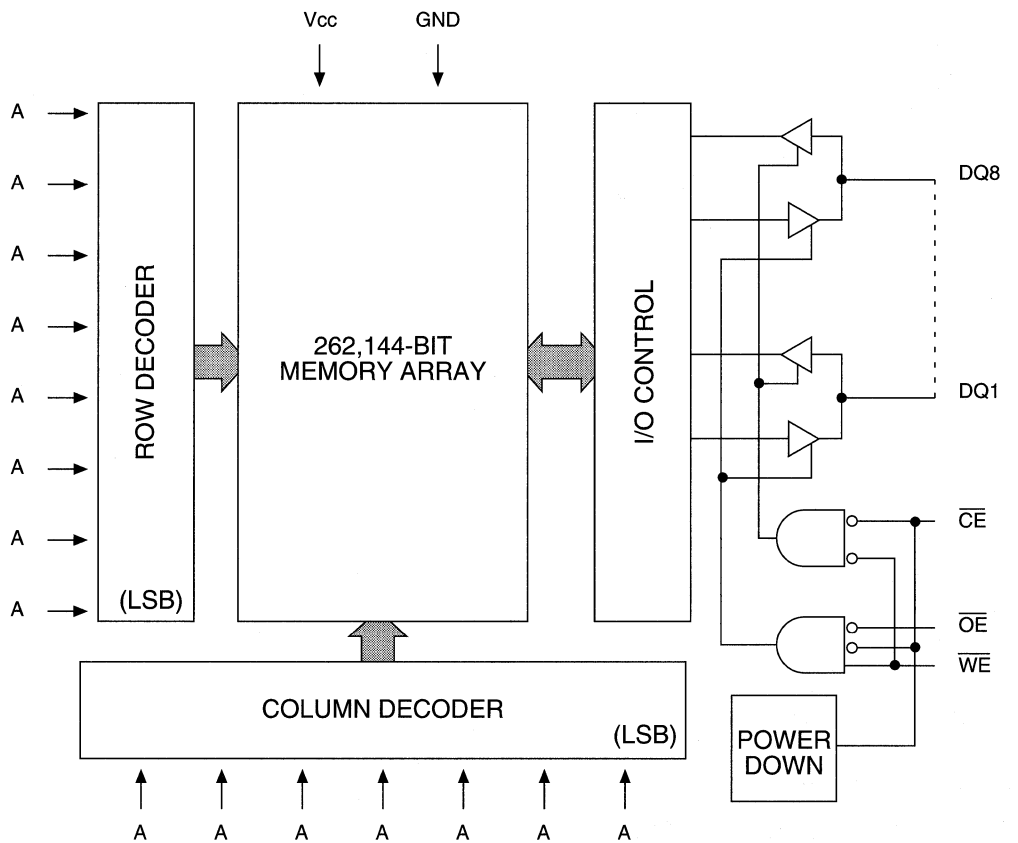
For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) with this organization. These enhancements can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ and $\overline{OE}$ go LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

The "P" version provides a reduction in both operating current (I_{CC}) and TTL standby current (I_{SB1}). The latter is achieved through the use of gated inputs on the $\overline{WE}$, $\overline{OE}$ and address lines, which also facilitates the design of battery backed systems. That is, the gated inputs simplify the design effort and circuitry required to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL-compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA
Voltage on Any Pin Relative to V_{SS} ..... -1V to V_{CC} +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	Vcc+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ Vcc	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) disabled 0V ≤ V_{OUT} ≤ Vcc	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		Vcc	4.5	5.5	V	1

					MAX							
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-10**	-12**	-15**	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; Vcc = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	103	190	170	150	130	125	120	mA	3, 13
	P version	I_{CC}	96	-	-	135	125	120	115	mA	3, 13
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; Vcc = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	24	55	50	45	40	35	35	mA	13
	P version	I_{SB1}	1.4	-	-	4	4	4	4	mA	13
	$\overline{CE}$ ≥ Vcc -0.2V; Vcc = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ Vcc -0.2V; f = 0	I_{SB2}	0.6	5	5	5	5	5	7	mA	13
	P version	I_{SB2}	0.4	-	-	3	3	3	3	mA	13

**P version not available with this speed.

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	6	pF	4
Output Capacitance	Vcc = 5V	C_O	6	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) ($0°C \le T_A \le 70°C$; $V_{CC} = 5V \pm 10\%$)

DESCRIPTION		-10		-12		-15		-20		-25		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle															
READ cycle time	^tRC	10		12		15		20		25		35		ns	
Address access time	^tAA		10		12		15		20		25		35	ns	
Chip Enable access time	^tACE		10		12		15		20		25		35	ns	
Output hold from address change	^tOH	3		3		3		3		3		3		ns	
Chip Enable to output in Low-Z	^tLZCE	3		3		3		3		3		3		ns	7
Chip disable to output in High-Z	^tHZCE		5		6		8		9		9		15	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		0		0		ns	
Chip disable to power-down time	^tPD		10		12		15		20		25		35	ns	
Output Enable access time	^tAOE		5		6		8		8		8		12	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		0		0		ns	
Output disable to out put in High-Z	^tHZOE		5		6		6		7		7		12	ns	6
WRITE Cycle															
WRITE cycle time	^tWC	10		12		15		20		25		35		ns	
Chip Enable to end of write	^tCW	7		8		10		12		15		20		ns	
Address valid to end of write	^tAW	7		8		10		12		15		20		ns	
Address setup time	^tAS	0		0		0		0		0		0		ns	
Address hold from end of write	^tAH	1		1		1		1		1		1		ns	
WRITE pulse width	$^tWP1$	7		8		10		12		15		20		ns	
WRITE pulse width	$^tWP2$	10		12		12		15		15		20		ns	
Data setup time	^tDS	6		7		7		10		10		15		ns	
Data hold time	^tDH	0		0		0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	2		2		2		2		2		2		ns	7
Write Enable to output in High-Z	^tHZWE		5		6		7		8		10		12	ns	6, 7

INDUSTRIAL TEMPERATURE SPECIFICATIONS (IT)

The following specifications are to be used for Industrial Temperature (IT) MT5C2568 SRAMs.
(-40°C ≤ T_A ≤ 85°C)

			MAX							
DESCRIPTION	**CONDITIONS**	**SYM**	**-10**	**-12**	**-15**	**-20**	**-25**	**-35**	**UNITS**	**NOTES**
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	200	180	155	140	135	135	mA	3, 13
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	65	60	50	45	40	40	mA	13
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	6	6	6	6	6	7	mA	13

DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP versions only)

DESCRIPTION	**CONDITIONS**		**SYMBOL**	**MAX**	**UNITS**	**NOTES**
Data Retention Current	$\overline{CE}$ ≥ (V_{CC} -0.2V) V_{IN} ≥ (V_{CC} -0.2V) or ≤ 0.2V	V_{CC} = 2V	I_{CCDR}	400	µA	
		V_{CC} = 3V	I_{CCDR}	600	µA	
Data Retention Current LP version	$\overline{CE}$ ≥ (V_{CC} -0.2V)	V_{CC} = 2V	I_{CCDR}	400	µA	
		V_{CC} = 3V	I_{CCDR}	600	µA	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

Refer to commercial temperature timing parameters for specifications not listed here.
(Notes 5, 13) (-40°C ≤ T_A ≤ 85°C)

DESCRIPTION		-12		-15		-20		-25		-35			
	SYM	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ Cycle													
Output hold from address change	^tOH	2		2		2		2		2		ns	
Chip Enable to output in Low-Z	^tLZCE	2		2		2		2		2		ns	7

AUTOMOTIVE AND EXTENDED TEMPERATURE SPECIFICATIONS (AT AND XT)

The following specifications are to be used for Automotive Temperature (AT) and Extended Temperature (XT) MT5C2568 SRAMs. (-40°C ≤ T_A ≤ 125°C - AT) (-55°C ≤ T_A ≤ 125°C - XT)

			MAX						
DESCRIPTION	**CONDITIONS**	**SYMBOL**	**-12**	**-15**	**-20**	**-25**	**-35**	**UNITS**	**NOTES**
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	180	155	140	135	135	mA	3, 13
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	60	50	45	40	40	mA	13
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	7	7	7	7	7	mA	13

DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP versions only)

DESCRIPTION	**CONDITIONS**		**SYMBOL**	**MAX**	**UNITS**	**NOTES**
Data Retention Current	$\overline{CE}$ ≥ (V_{CC} -0.2V) V_{IN} ≥ (V_{CC} -0.2V) or ≤ 0.2V	V_{CC} = 2V	I_{CCDR}	500	µA	
		V_{CC} = 3V	I_{CCDR}	800	µA	
Data Retention Current LP version	$\overline{CE}$ ≥ (V_{CC} -0.2V)	V_{CC} = 2V	I_{CCDR}	500	µA	
		V_{CC} = 3V	I_{CCDR}	800	µA	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

Refer to commercial temperature timing parameters for specifications not listed here.
(Notes 5, 13) (-40°C ≤ T_A ≤ 125°C; -55°C ≤ T_A ≤ 125°C; V_{CC} = 5V ± 10%)

DESCRIPTION		-12		-15		-20		-25		-35			
	SYM	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ Cycle													
Output hold from address change	^tOH	2		2		2		2		2		ns	
Chip Enable to output in Low-Z	^tLZCE	2		2		2		2		2		ns	7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

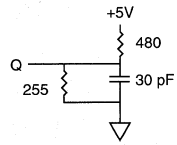


Fig. 1 OUTPUT LOAD EQUIVALENT

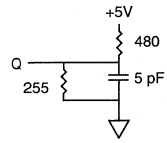


Fig. 2 OUTPUT LOAD EQUIVALENT

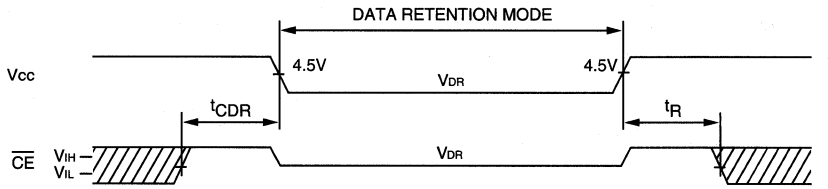
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZOE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE, and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Typical values are measured at 5V, 25°C and 15ns cycle time.
14. Typical currents are measured at 25°C.
15. Output enable ($\overline{OE}$) is inactive (HIGH).
16. Output enable ($\overline{OE}$) is active (LOW).

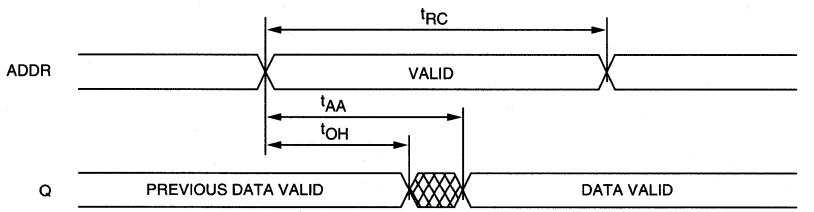
DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP versions only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2			V	
Data Retention Current L version	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	ICCDR		175	300	µA	14
		Vcc = 3V	ICCDR		250	500	µA	14
Data Retention Current LP version	$\overline{CE}$ ≥ (Vcc -0.2V)	Vcc = 2V	ICCDR		175	300	µA	14
		Vcc = 3V	ICCDR		250	500	µA	14
Chip Deselect to Data Retention Time			^{t}CDR	0			ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

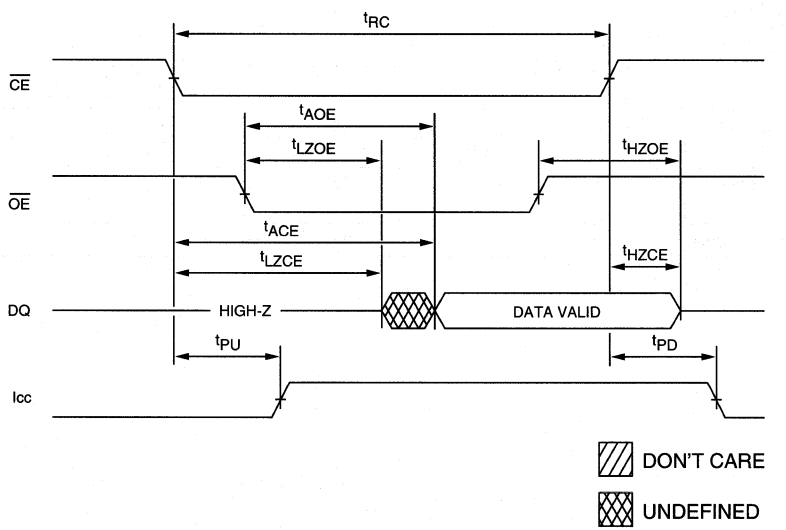
LOW Vcc DATA RETENTION WAVEFORM



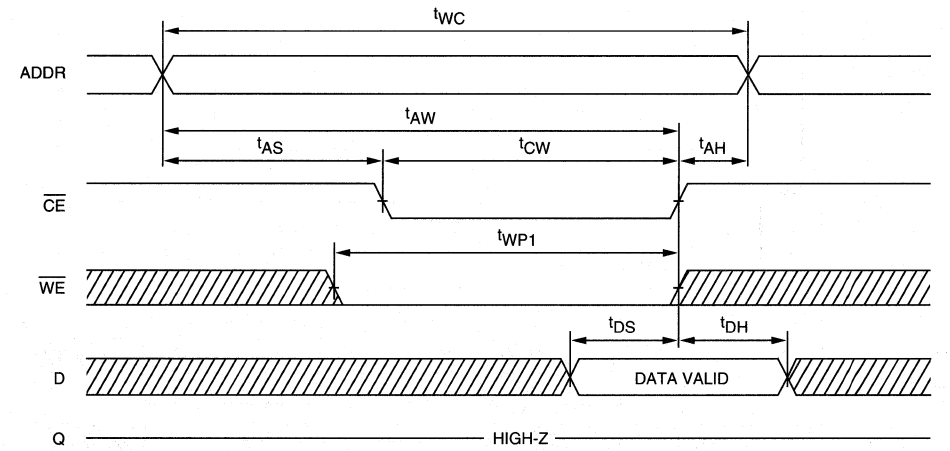
READ CYCLE NO. 1 [8, 9]



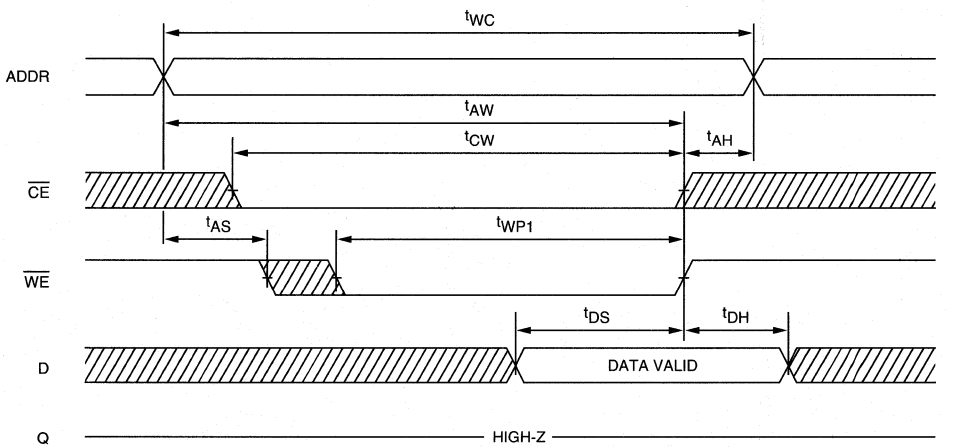
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)



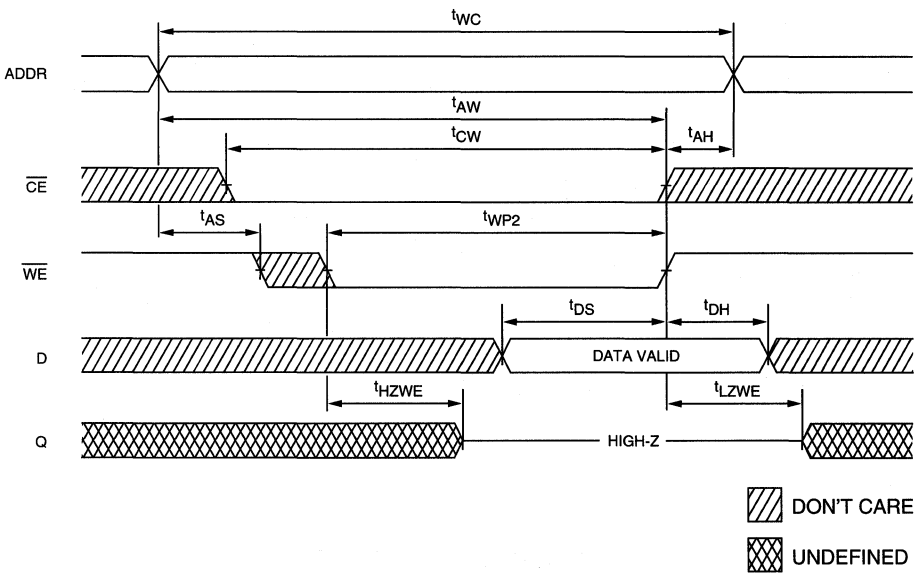
WRITE CYCLE NO. 2 [12, 15]
(Write Enable Controlled)



DON'T CARE

UNDEFINED

WRITE CYCLE NO. 3 [7, 12, 16]
(Write Enable Controlled)



SRAM

128K x 8 SRAM
WITH OUTPUT ENABLE

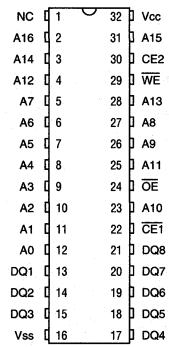
FEATURES
- High speed: 12, 15, 17, 20, 25 and 35ns
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE1}$, CE2 and $\overline{OE}$ options
- All inputs and outputs are TTL-compatible
- Fast $\overline{OE}$ access time: 8ns

OPTIONS — MARKING
- Timing
  - 12ns access — -12
  - 15ns access — -15
  - 17ns access — -17
  - 20ns access — -20
  - 25ns access — -25
  - 35ns access — -35
- Packages
  - Plastic DIP (400 mil) — None
  - Plastic SOJ (400 mil) — DJ
  - Plastic SOJ (300 mil) — SJ
- 2V data retention — L
- 2V data retention, low power — LP
- Temperature
  - Commercial (0°C to +70°C) — None
  - Industrial (-40°C to +85°C) — IT
  - Automotive (-40°C to +125°C) — AT
  - Extended (-55°C to +125°C) — XT
- Part Number Example: MT5C1008DJ-25 LP

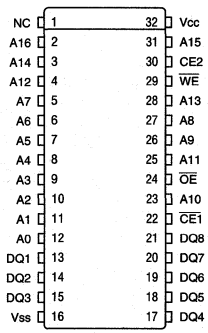
NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

32-Pin DIP (SA-6)



32-Pin SOJ (SD-4, SD-5)



GENERAL DESCRIPTION

The MT5C1008 is organized as a 131,072 x 8 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

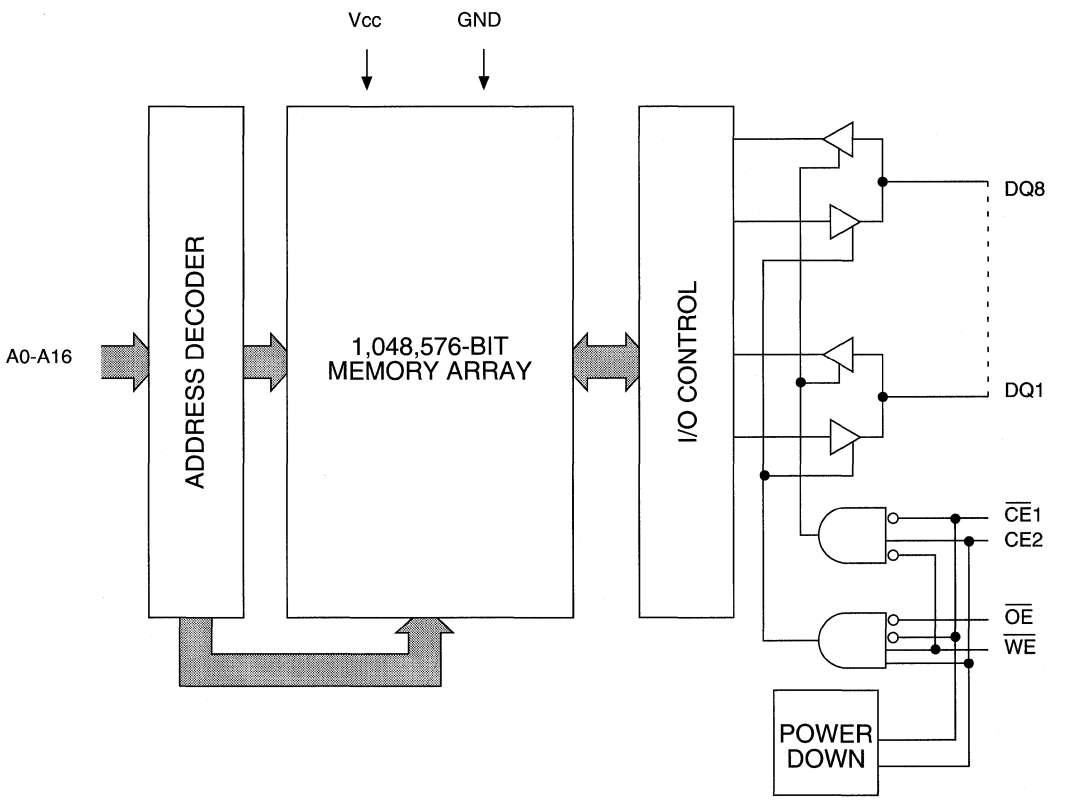
For flexibility in high-speed memory applications, Micron offers dual chip enables ($\overline{CE1}$, CE2) and an output enable ($\overline{OE}$). This enhancement can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE1}$ inputs are both LOW and CE2 is HIGH. Reading is accomplished when $\overline{WE}$ and CE2 remain HIGH and $\overline{CE1}$ and $\overline{OE}$ go LOW. The device offers reduced power standby modes when disabled. This allows system designers to meet low standby power requirements.

The "L" and "LP" versions each provide a 70% reduction in CMOS standby current (I_{SB2}) over the standard version. The "LP" version also provides a 90% reduction in TTL standby current (I_{SB1}). This is achieved by including gated inputs on the $\overline{WE}$, $\overline{OE}$ and address lines. The gated inputs also facilitate the design of battery backed systems where the designer needs to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL-compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE1}$	CE2	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	X	HIGH-Z	STANDBY
STANDBY	X	X	L	X	HIGH-Z	STANDBY
READ	L	L	H	H	Q	ACTIVE
NOT SELECTED	H	L	H	H	HIGH-Z	ACTIVE
WRITE	X	L	H	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA
Voltage on Any Pin Relative to V_{SS} ..... -1V to V_{CC} +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

				MAX							
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-12	-15	-17	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	CE2 ≥ V_{IH}; $\overline{CE1}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	95	190	165	155	140	125	115	mA	3, 13
Power Supply Current: Standby	CE2 ≤ V_{IH} or $\overline{CE1}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	17	45	40	40	35	30	25	mA	13
	LP version only	I_{SB1}	1.3	3	3	3	3	3	3	mA	13
	CE2 ≤ V_{SS} +0.2V; $\overline{CE1}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	0.4	5	5	5	5	5	5	mA	13
	L and LP versions only	I_{SB2}	0.3	1.5	1.5	1.5	1.5	1.5	1.5	mA	13

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	8	pF	4
Output Capacitance	V_{CC} = 5V	C_O	8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION	SYM	-12		-15		-17		-20		-25		-35		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
READ Cycle															
READ cycle time	^tRC	12		15		17		20		25		35		ns	
Address access time	^tAA		12		15		17		20		25		35	ns	
Chip Enable access time	^tACE		12		15		17		20		25		35	ns	
Output hold from address change	^tOH	3		3		3		3		5		5		ns	
Chip Enable to output in Low-Z	^tLZCE	3		5		5		5		5		5		ns	7
Chip disable to output in High-Z	^tHZCE		5		6		7		8		10		15	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		0		0		ns	
Chip disable to power-down time	^tPD		12		15		17		20		25		35	ns	
Output Enable access time	^tAOE		4		5		5		6		8		12	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		0		0		ns	
Output disable to output in High-Z	^tHZOE		4		5		5		6		10		12	ns	6
WRITE Cycle															
WRITE cycle time	^tWC	12		15		17		20		25		35		ns	
Chip Enable to end of write	^tCW	8		10		12		12		15		20		ns	
Address valid to end of write	^tAW	8		10		12		12		15		20		ns	
Address setup time	^tAS	0		0		0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		0		0		ns	
WRITE pulse width	$^tWP1$	8		9		12		12		15		20		ns	
WRITE pulse width	$^tWP2$	10		12		13		15		15		20		ns	
Data setup time	^tDS	6		7		8		8		10		15		ns	
Data hold time	^tDH	0		0		0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	3		3		3		3		3		3		ns	7
Write Enable to output in High-Z	^tHZWE		5		6		7		8		10		15	ns	6, 7

INDUSTRIAL TEMPERATURE SPECIFICATIONS (IT)

The following specifications are to be used for Industrial Temperature (IT) MT5C1008 SRAMs.
(-40°C ≤ T_A ≤ 85°C)

				MAX					
DESCRIPTION	**CONDITIONS**	**SYMBOL**	**TYP**	**-20**	**-25**	**-35**	**-45**	**UNITS**	**NOTES**
Power Supply Current: Operating	CE2 ≥ V_{IH}; $\overline{CE1}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	95	150	135	125	120	mA	3, 13
Power Supply Current: Standby	CE2 ≤ V_{IH} or $\overline{CE1}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	17	35	30	25	25	mA	13
	CE2 ≤ V_{SS} +0.2V; $\overline{CE1}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	0.4	5	5	5	5	mA	13
L version only	CE2 ≤ V_{SS} +0.2V; $\overline{CE1}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	0.3	2	2	2	2	mA	13

DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	**CONDITIONS**		**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**NOTES**
Data Retention Current	$\overline{CE1}$ ≥ (V_{CC} -0.2V) or CE2 ≤ (V_{SS} +0.2V) V_{IN} ≥ (V_{CC} -0.2V) or ≤ 0.2V	V_{CC} = 2V	I_{CCDR}		35	170	µA	14
		V_{CC} = 3V	I_{CCDR}		60	325	µA	14

AUTOMOTIVE AND EXTENDED TEMPERATURE SPECIFICATIONS (AT AND XT)

The following specifications are to be used for Automotive Temperature (AT) and Extended Temperature (XT) MT5C1008 SRAMs. (-40°C ≤ T_A ≤ 125°C - AT) (-55°C ≤ T_A ≤ 125°C - XT)

				MAX					
DESCRIPTION	**CONDITIONS**	**SYMBOL**	**TYP**	**-20**	**-25**	**-35**	**-45**	**UNITS**	**NOTES**
Power Supply Current: Operating	CE2 ≥ V_{IH}; $\overline{CE1}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	95	150	135	125	120	mA	3, 13
Power Supply Current: Standby	CE2 ≤ V_{IH} or $\overline{CE1}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	17	45	40	35	32	mA	13
	CE2 ≤ V_{SS} +0.2V; $\overline{CE1}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	0.4	7	7	7	7	mA	13
L version only	CE2 ≤ V_{SS} +0.2V; $\overline{CE1}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	0.3	5	5	5	5	mA	13

DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	**CONDITIONS**		**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**NOTES**
Data Retention Current	$\overline{CE1}$ ≥ (V_{CC} -0.2V) or CE2 ≤ (V_{SS} +0.2V) V_{IN} ≥ (V_{CC} -0.2V) or ≤ 0.2V	V_{CC} = 2V	I_{CCDR}		35	1,000	µA	14
		V_{CC} = 3V	I_{CCDR}		60	1,500	µA	14

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

Refer to commercial temperature timing parameters for specifications not listed here.
(Notes 5, 14) (-40°C ≤ T_A ≤ 125°C; -55°C ≤ T_A ≤ 125°C; V_{CC} = 5V ±10%)

DESCRIPTION		-20		-25		-35		-45			
	SYM	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ Cycle											
Output hold from address change	^tOH	3		3		3		3		ns	
Chip Enable to output in Low-Z	^tLZCE	3		3		3		3		ns	7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

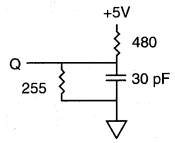


Fig. 1 OUTPUT LOAD EQUIVALENT

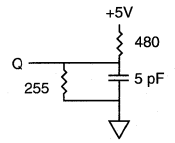


Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

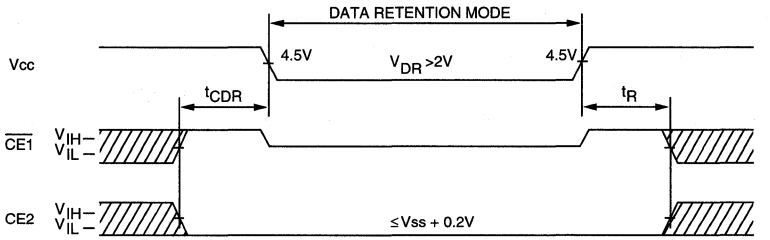
1. All voltages referenced to Vss (GND).
2. -3V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZOE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables and output enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. CE2 timing is the same as $\overline{CE1}$ timing. The waveform is inverted.
13. Chip enable and write enable can initiate and terminate a WRITE cycle.
14. Typical values are measured at 5V, 25°C and 25ns cycle time.
15. Typical currents are measured at 25°C.
16. Output enable ($\overline{OE}$) is inactive (HIGH).
17. Output enable ($\overline{OE}$) is active (LOW).

DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP versions only)

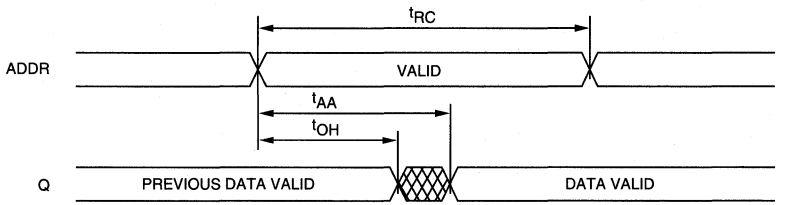
DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2			V	
Data Retention Current L version	$\overline{CE1}$ ≥ (Vcc -0.2V) or CE2 ≤ (Vss +0.2V)	Vcc = 2V	ICCDR		35	150	µA	15
	VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 3V	ICCDR		60	250	µA	15
		Vcc = 3V*	ICCDR		30	100	µA	15
Data Retention Current LP version	$\overline{CE1}$ ≥ (Vcc -0.2V) or CE2 ≤ (Vss +0.2V)	Vcc = 2V	ICCDR		35	150	µA	15
		Vcc = 3V	ICCDR		60	250	µA	15
Chip Deselect to Data Retention Time			^{t}CDR	0			ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

*Advance

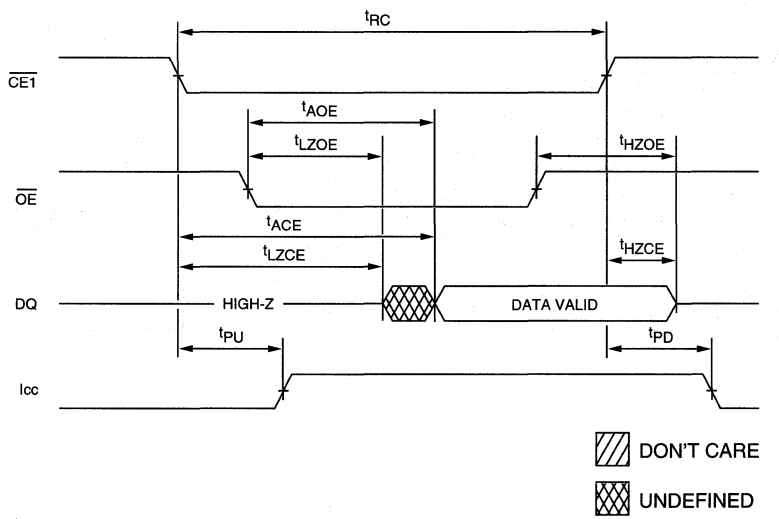
LOW Vcc DATA RETENTION WAVEFORM



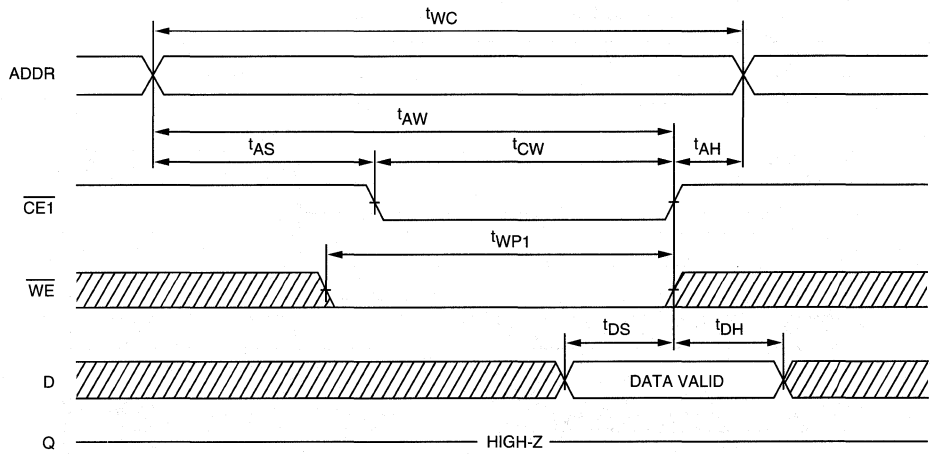
READ CYCLE NO. 1 [8, 9]



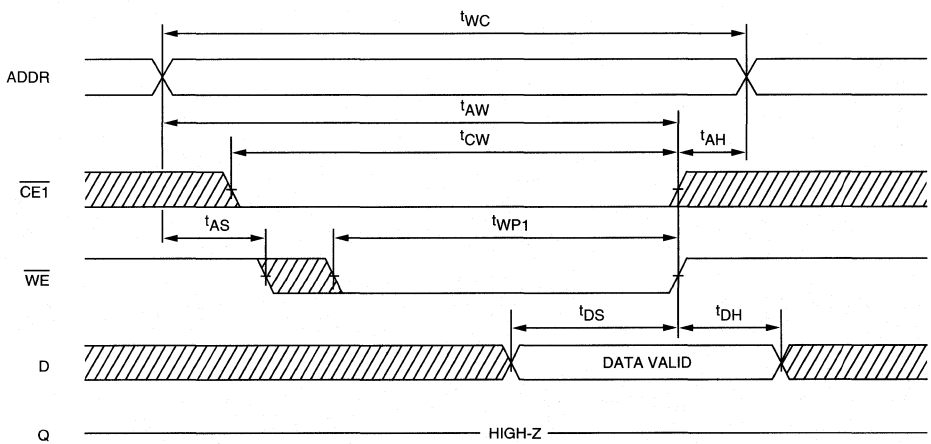
READ CYCLE NO. 2 [7, 8, 10, 12]

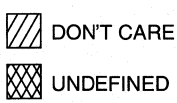


WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)

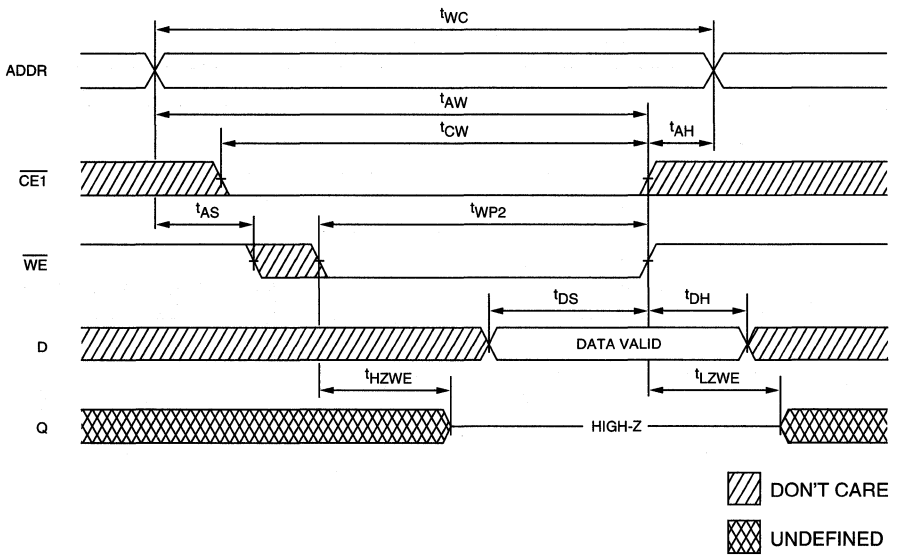


WRITE CYCLE NO. 2 [12, 13, 16]
(Write Enable Controlled)





WRITE CYCLE NO. 3 [7, 12, 13, 17]
(Write Enable Controlled)



MICRON SEMICONDUCTOR, INC.

MT5C128K8A1
REVOLUTIONARY PINOUT 128K x 8 SRAM

SRAM

128K x 8 SRAM

WITH SINGLE CHIP ENABLE,
REVOLUTIONARY PINOUT

FEATURES

- High speed: 12, 15, 20 and 25ns
- Multiple center power and ground pins for greater noise immunity
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- Automatic $\overline{CE}$ power down
- All inputs and outputs are TTL-compatible
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Fast $\overline{OE}$ access times: 6, 8, 10 and 12ns

OPTIONS — MARKING

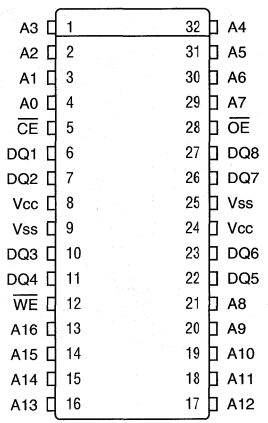
- Timing
  - 12ns access — -12
  - 15ns access — -15
  - 20ns access — -20
  - 25ns access — -25
- 2V data retention — L
- Temperature
  - Commercial (0°C to +70°C) — None
  - Industrial (-40°C to +85°C) — IT*
  - Automotive (-40°C to +125°C) — AT*
  - Extended (-55°C to +125°C) — XT*
- Packages
  - 32-pin SOJ (400 mil) — DJ
- Part Number Example: MT5C128K8A1DJ-25

* Contact factory for specifications and availability.

NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

32-Pin SOJ
(SD-5)



GENERAL DESCRIPTION

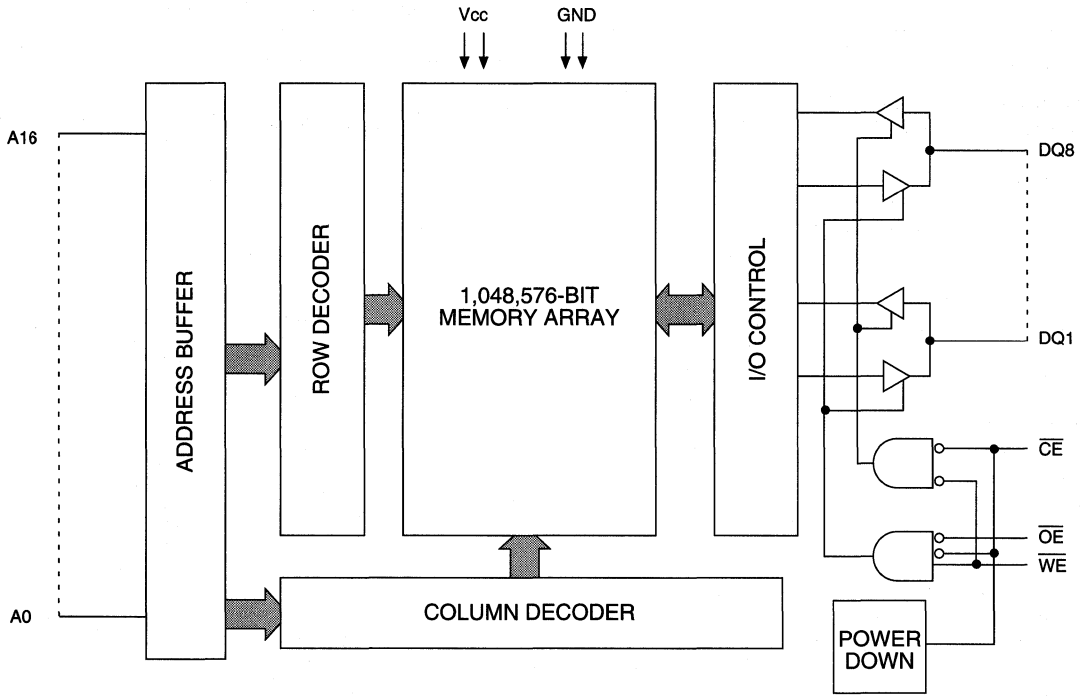
The MT5C128K8A1 is organized as a 131,072 x 8 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

This device offers multiple center power and ground pins for improved performance. For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) with this organization. This enhancement can place the ouputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ and $\overline{OE}$ go LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL-compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

PIN DESCRIPTIONS

SOJ PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
4, 3, 2, 1, 32, 31, 30, 29, 21, 20, 19, 18, 17, 16, 15, 14, 13	A0-A16	Input	Address Inputs: These inputs determine which cell is addressed.
12	$\overline{WE}$	Input	Write Enable: This input determines if the cycle is a READ or WRITE cycle. $\overline{WE}$ is LOW for a WRITE cycle and HIGH for a READ cycle.
5	$\overline{CE}$	Input	Chip Enable: This active LOW input is used to enable the device. When $\overline{CE}$ is HIGH, the chip is disabled and automatically goes into standby power mode.
28	$\overline{OE}$	Input	Output Enable: This active LOW input enables the output drivers.
6, 7, 10, 11, 22, 23, 26, 27	DQ1-DQ8	Input/ Output	SRAM Data I/O: Data inputs and tristate data outputs.
8, 24	Vcc	Supply	Power Supply: 5V ±10%
9, 25	Vss	Supply	Ground: GND

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1.7W
Short Circuit Output Current 50mA
Voltage on Any Pin Relative to V_{SS} ..... -1V to V_{CC} +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

				MAX					
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-12	-15	-20	-25	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	150	300	260	220	200	mA	3
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	25	50	45	40	35	mA	
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	0.5	5	5	5	5	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	6	pF	4
Output Capacitance	V_{CC} = 5V	C_O	6	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 5, 13) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION		-12		-15		-20		-25			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle											
READ cycle time	^tRC	12		15		20		25		ns	
Address access time	^tAA		12		15		20		25	ns	
Chip Enable access time	^tACE		12		15		20		25	ns	
Output hold from address change	^tOH	4		4		5		5		ns	
Chip Enable to output in Low-Z	^tLZCE	4		5		5		5		ns	7
Chip disable to output in High-Z	^tHZCE		6		6		8		8	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		ns	
Chip disable to power-down time	^tPD		12		15		20		25	ns	
Output Enable access time	^tAOE		6		8		10		12	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		ns	
Output disable to output in High-Z	^tHZOE		6		6		8		8	ns	6
WRITE Cycle											
WRITE cycle time	^tWC	12		15		20		25		ns	
Chip Enable to end of write	^tCW	10		12		13		15		ns	
Address valid to end of write	^tAW	8		9		12		14		ns	
Address setup time	^tAS	0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		ns	
WRITE pulse width	$^tWP1$	8		9		10		12		ns	
WRITE pulse width	$^tWP2$	8		9		10		12		ns	
Data setup time	^tDS	6		8		10		10		ns	
Data hold time	^tDH	0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	1		1		1		1		ns	7
Write Enable to output in High-Z	^tHZWE		6		6		8		8	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

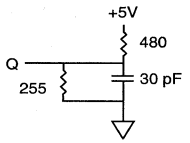


Fig. 1 OUTPUT LOAD EQUIVALENT

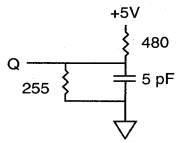


Fig. 2 OUTPUT LOAD EQUIVALENT

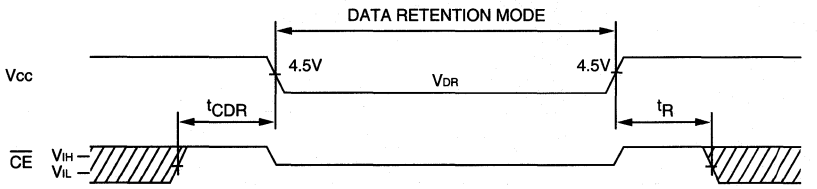
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates. The specified value applies with the outputs unloaded, and $f = \frac{1}{^{t}RC\ (MIN)}$ Hz.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZOE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE, and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. Chip enable and output enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Contact Micron for IT/AT/XT timing and current specifications; they may differ from the commercial temperature range specifications shown in this data sheet.
14. Typical currents are measured at 25°C.
15. Output enable ($\overline{OE}$) is inactive (HIGH).
16. Output enable ($\overline{OE}$) is active (LOW).

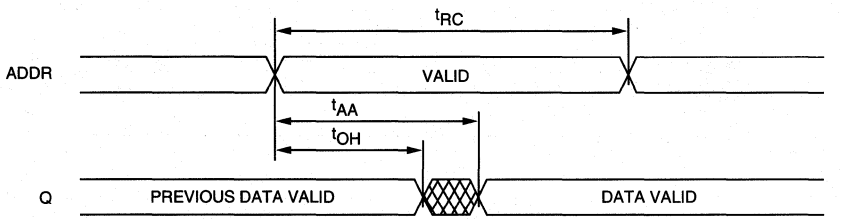
DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2			V	
Data Retention Current L version	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	ICCDR		TBD	TBD	µA	14
		Vcc = 3V	ICCDR		TBD	TBD	µA	14
Chip Deselect to Data Retention Time			^{t}CDR	0			ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

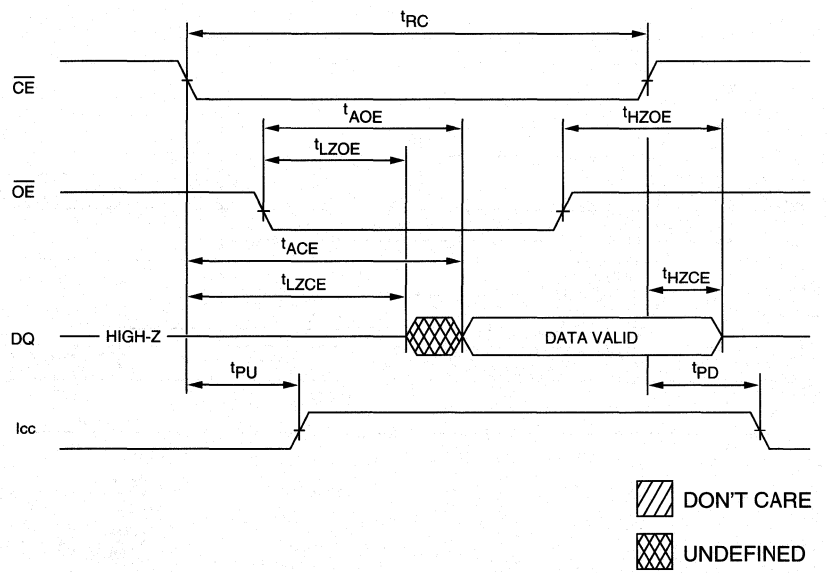
LOW Vcc DATA RETENTION WAVEFORM



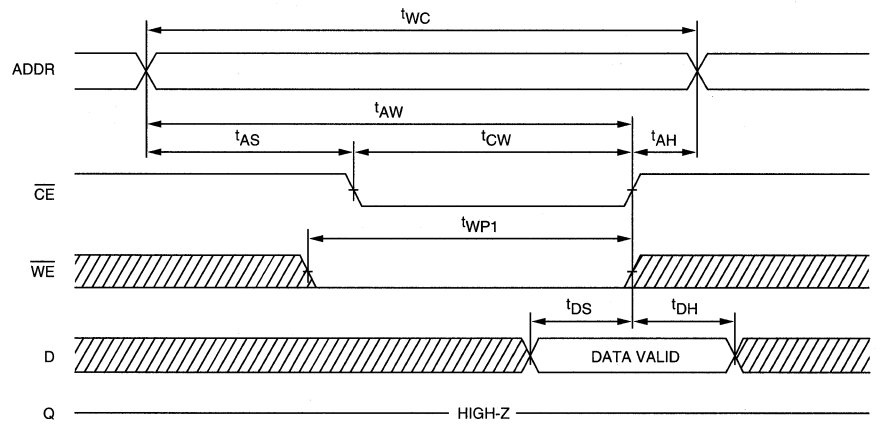
READ CYCLE NO. 1 [8, 9]



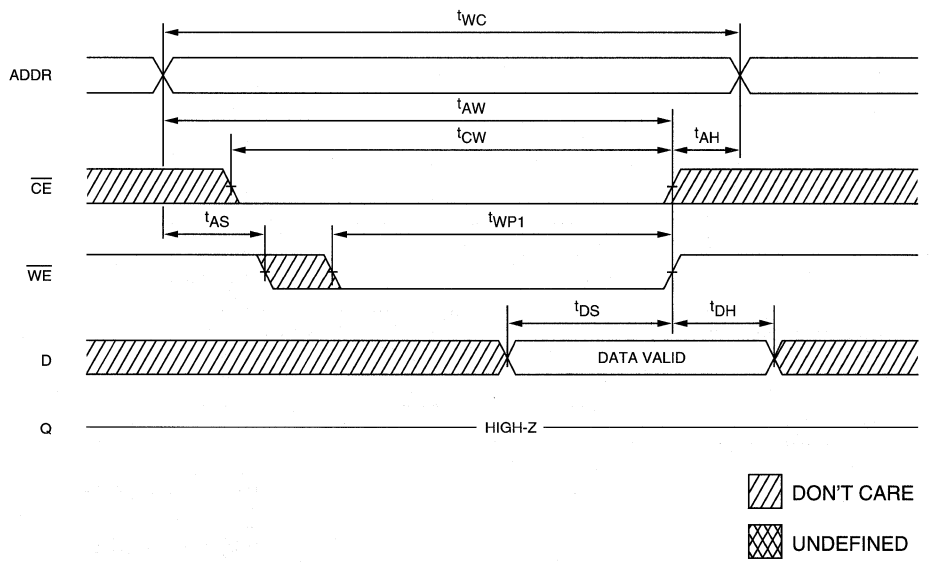
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)

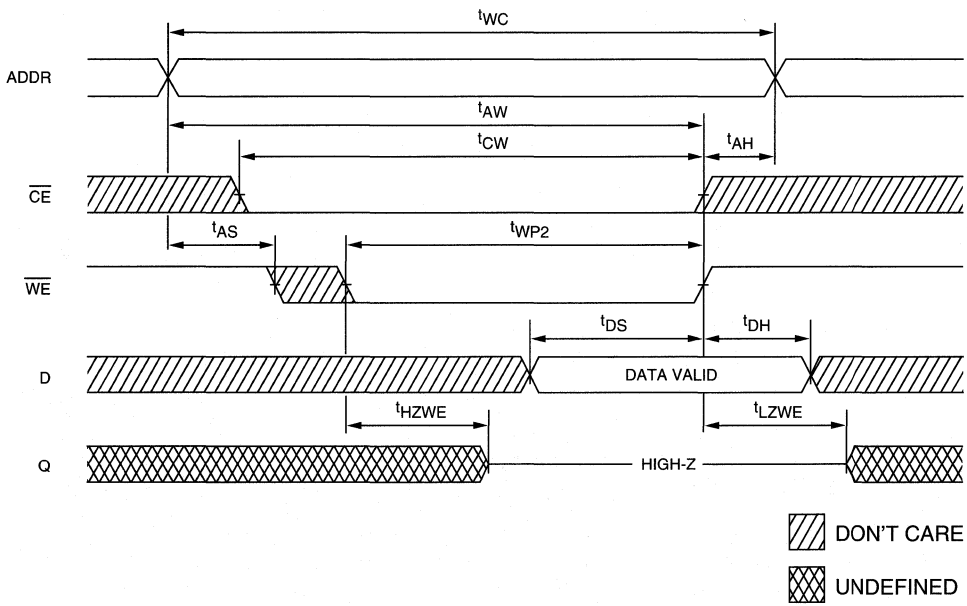


WRITE CYCLE NO. 2 [12, 15]
(Write Enable Controlled)



WRITE CYCLE NO. 3 [7, 12, 16]

(Write Enable Controlled)



MICRON SEMICONDUCTOR, INC.

MT5C128K8A1
REVOLUTIONARY PINOUT 128K x 8 SRAM

SRAM

512K x 8 SRAM

WITH OUTPUT ENABLE

FEATURES

- High speed: 12, 15, 20, 25 and 35ns
- High-performance, low-power, CMOS double-metal process
- Multiple center power and ground pins for improved noise immunity
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- All inputs and outputs are TTL-compatible
- Fast $\overline{OE}$ access time: 6, 8, 10, 12 and 15ns

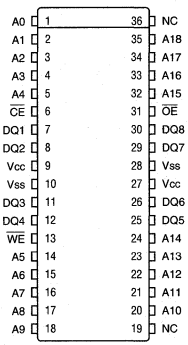
OPTIONS — MARKING

- Timing
  - 12ns access — -12
  - 15ns access — -15
  - 20ns access — -20
  - 25ns access — -25
  - 35ns access — -35
- Packages
  - Plastic SOJ (400 mil) — DJ
  - Plastic TSOP (400 mil) — TG
- 2V data retention — L
- Low power — P
- Temperature
  - Commercial (0°C to +70°C) — None
  - Industrial (-40°C to +85°C) — IT
  - Automotive (-40°C to +125°C) — AT
  - Extended (-55°C to +125°C) — XT
- Part Number Example: MT5C512K8B2DJ-20 L

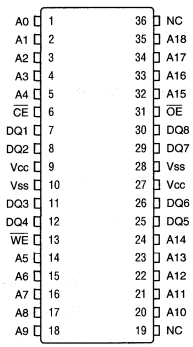
NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

36-Pin SOJ (SD-6)



36-Pin TSOP (SE-2)



GENERAL DESCRIPTION

The MT5C512K8B2 is organized as a 524,288 x 8 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron 4 Meg SRAMs are fabricated using double-layer metal, triple-layer polysilicon technology.

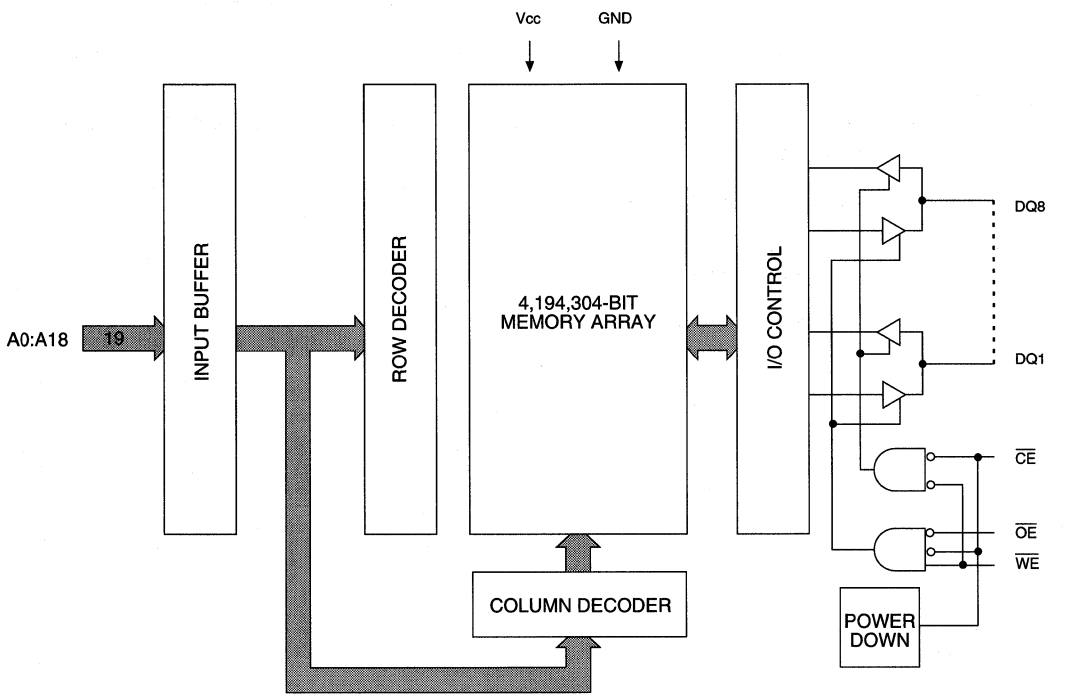
This device offers multiple center power and ground pins for improved performance. For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) and ouput enable ($\overline{OE}$) capabilities. These enhancements can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ and $\overline{OE}$ go LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

The "P" version provides a 90 percent reduction in TTL standby current (I_{SB1}). This is achieved by including gated inputs. The gated inputs also facilitate the design of battery backed systems where the designer needs to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL-compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

THERMAL IMPEDENCE (EST)[16]

PACKAGE	NUMBER OF PINS	θ_{JC}* (°C/W)	θ_{JA}* (°C/W)
SOJ	36	15	55
TSOP	36	5	65

*The thermal impedence numbers assume the device is socketted on a PC board and air flow is zero.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Storage Temperature (plastic) ..... -55°C to +150°C
Short Circuit Output Current 50mA
Voltage on Any Pin Relative to V_{SS} ..... -1V to V_{CC}+1
Junction Temperature** ..... +150°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Maximum junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow. See the Application Information section at the end of this data sheet for more information.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-2	2	µA	
Output Leakage Current	Output(s) disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-2	2	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

			MAX						
DESCRIPTION	CONDITIONS	SYMBOL	-12	-15	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	200	180	175	170	160	mA	3
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	35	30	25	25	20	mA	
	P version only	I_{SB1}	2	2	2	2	2	mA	
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	2	2	2	2	2	mA	
	P version only	I_{SB2}	2	2	2	2	2	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	5	pF	4
Output Capacitance	V_{CC} = 5V	C_O	7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 5, 13) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION		-12		-15		-20		-25		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle													
READ cycle time	^tRC	12		15		20		25		35		ns	
Address access time	^tAA		12		15		20		25		35	ns	
Chip Enable access time	^tACE		12		15		20		25		35	ns	
Output hold from address change	^tOH	3		3		3		3		3		ns	
Chip Enable to output in Low-Z	^tLZCE	3		3		5		5		5		ns	7
Chip disable to output in High-Z	^tHZCE		6		7		8		10		15	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		0		ns	
Chip disable to power-down time	^tPD		12		15		20		25		35	ns	
Output Enable access time	^tAOE		6		8		10		12		15	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		0		ns	
Output disable to output in High-Z	^tHZOE		5		6		7		10		12	ns	6
WRITE Cycle													
WRITE cycle time	^tWC	12		15		20		25		35		ns	
Chip Enable to end of write	^tCW	8		10		12		15		20		ns	
Address valid to end of write	^tAW	8		10		12		15		20		ns	
Address setup time	^tAS	0		0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		0		ns	
WRITE pulse width	$^tWP1$	8		9		10		15		20		ns	
WRITE pulse width	$^tWP2$	9		11		12		17		22		ns	
Data setup time	^tDS	6		7		8		10		15		ns	
Data hold time	^tDH	0		0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	3		3		4		5		5		ns	7
Write Enable to output in High-Z	^tHZWE		5		6		8		10		15	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

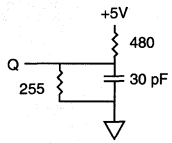


Fig. 1 OUTPUT LOAD EQUIVALENT

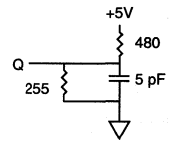


Fig. 2 OUTPUT LOAD EQUIVALENT

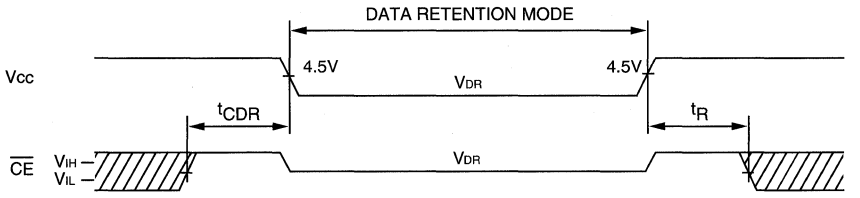
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZOE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE, and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. Chip enables and output enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Contact Micron for IT/AT/XT timing and current specifications; they may differ from the commercial temperature range specifications shown in this data sheet.
14. Output enable ($\overline{OE}$) is inactive (HIGH).
15. Output enable ($\overline{OE}$) is active (LOW).
16. Micron does not warrant functionality nor reliability of any product in which the junction temperature exceeds 150°C. Care should be taken to limit power to acceptable levels.

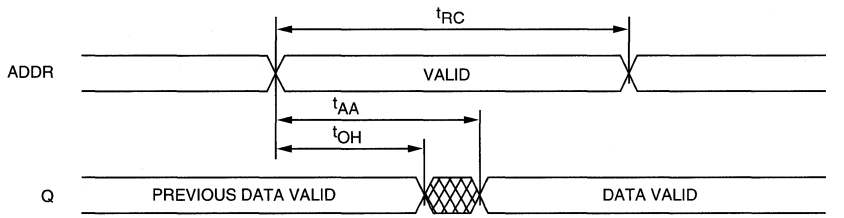
DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP versions only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2		V	
Data Retention Current L version	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	ICCDR		1	mA	
		Vcc = 3V	ICCDR		1.5	mA	
Data Retention Current LP version	$\overline{CE}$ ≥ (Vcc -0.2V)	Vcc = 2V	ICCDR		1	mA	
		Vcc = 3V	ICCDR		1.5	mA	
Chip Deselect to Data Retention Time			^{t}CDR	0		ns	4
Operation Recovery Time			^{t}R	^{t}RC		ns	4, 11

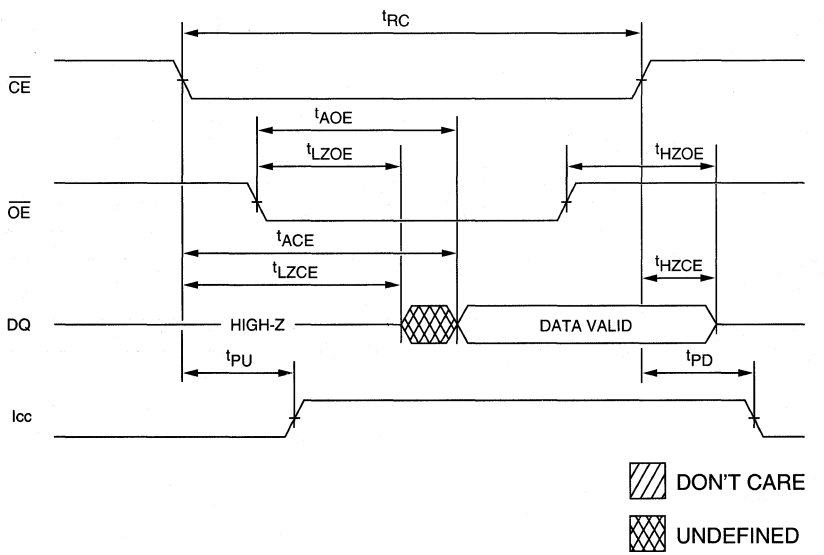
LOW Vcc DATA RETENTION WAVEFORM



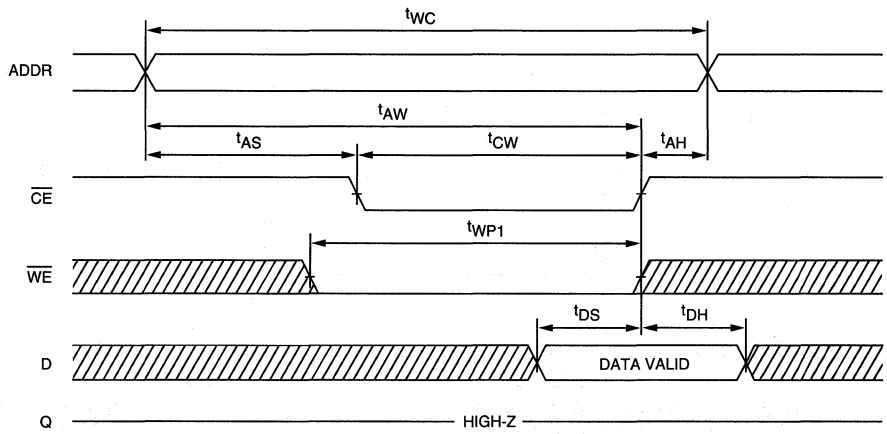
READ CYCLE NO. 1 [8, 9]



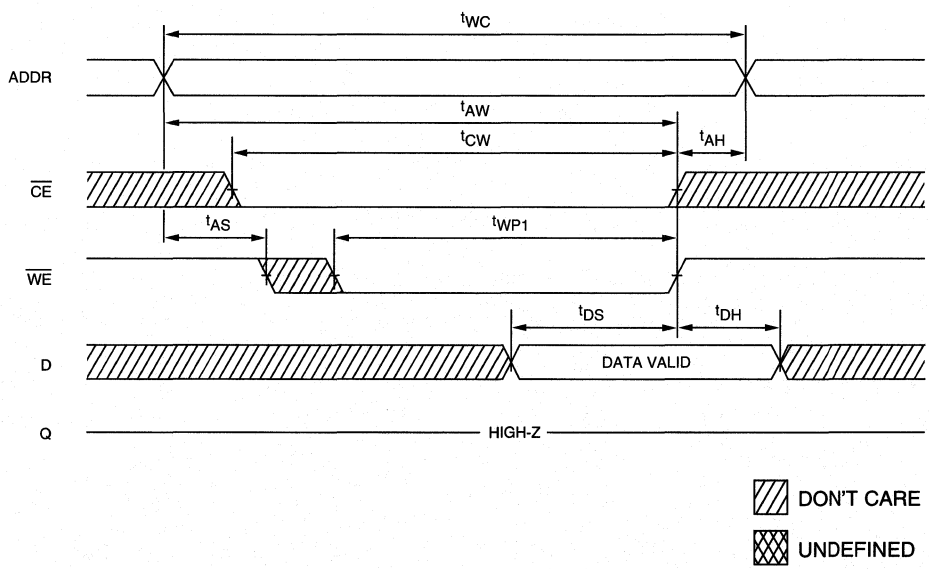
READ CYCLE NO. 2 [7, 8, 10]



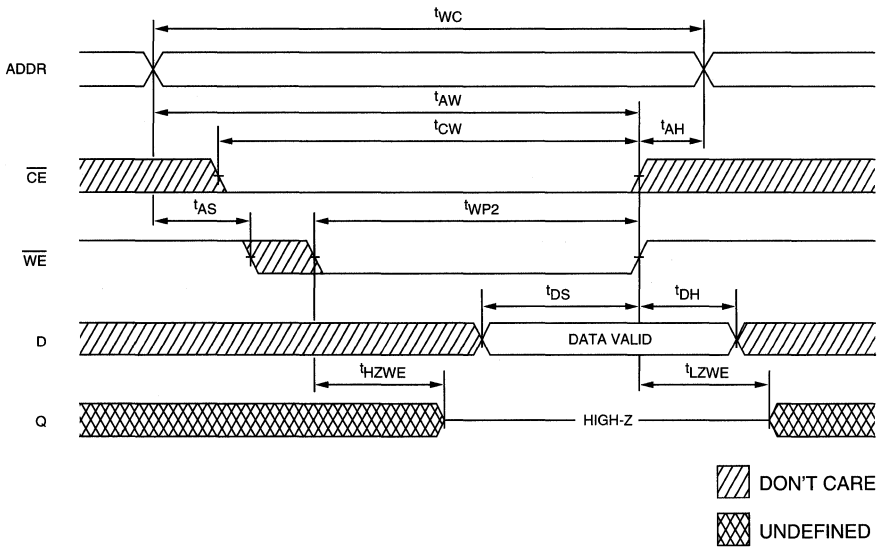
WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)



WRITE CYCLE NO. 2 [12, 14]
(Write Enable Controlled)



WRITE CYCLE NO. 3 [7, 12, 15]
(Write Enable Controlled)



APPLICATION INFORMATION

THERMAL CONSIDERATIONS

This section describes how to determine the junction temperature during operating conditions. It is essential that the maximum junction temperature of the 4 Meg SRAM is not exceeded. If this temperature is exceeded it is necessary to add external cooling such as forced airflow or change the operating conditions. The maximum junction temperature for Micron SRAMs is 150°C. The limiting temperature factor is not the SRAM but the mold compound which prevents reliable operating temperatures significantly about 150°C. However, it is advisable to run the part as cool as possible since reliability (FIT rates) are exponentially dependent upon junction temperature.

The calculation of the actual junction temperature begins with the power calculation and then the junction temperation calculation. Equations 1 and 2 below show how T_j is determined using the ambient temperature, thermal resistance and operating power. If an airflow is introduced into a system then Equation 2 should be used with an airflow thermal multiplier. Specific thermal resistances are given in Micron technical note "SRAM Thermal Design Considerations" and in individual data sheets.

$$T_j = T_A + P * \theta_{JA} \quad (1)$$

$$T_j = T_A + P * \theta_{JA} * \theta_M \quad (2)$$

T_j = Junction temperature of the active portion of the silicon die (°C)
T_A = Ambient air temperature (°C) at which the device is operated
P = Average power dissipation of the device (W)
θ_{JA} = Junction to ambient thermal resistance (°C/W)
θ_M = Airflow multiplier. This value changes for different values of airflow over the part (fpm).

To solve the above equations the average operating power must be calculated. Total power has three separate components (P_1, P_2 and P_3). P_1 is the operating power dissipated by the chip, P_2 is the AC output power due to the capacitive load and P_3 is the DC output power due to TTL DC load current (P_3 is usually negligible). For this example we have chosen P_2 such that outputs are switching from a logic LOW state to a logic HIGH state which gives the worst case output AC current. A complete description of these equations and their derivation is given in Micron technical note "Design Tips: 32K x 36 SRAM."

$$P_1 = Vcc\ Icc$$

$$P_2 = \frac{C_L}{T} (Vcc [V_{OH} - V_{OL}] - 0.5 [V_{OH}^2 - V_{OL}^2]) N_S$$

$$P_3 = (Vcc - V_{OH}) I_O N_H + V_{OL} I_I N_L.$$

Vcc = Supply voltage
Icc = Supply current
C_L = Capacitive output loading
T = Clock period
V_{OH} = Output high voltage
V_{OL} = Output low voltage
I_O = Output current on DQ lines which are high
I_I = Input current on DQ lines which are low
N_H = Number of DQ lines which are high
N_L = Number of DQ lines which are low.

Table 1
EFFECTS OF AIRFLOW ON 4 MEG SRAM SOJ PACKAGES

Package	Air Flow	θ_M Multiplier
PSOJ	200 fpm	0.7 - 0.75
PSOJ	500 fpm	0.55 - 0.65

ADDITIONAL INFORMATION

For more information on thermal considerations see Micron's technical notes, "SRAM Thermal Design Considerations" and "Design Tips: 32K x 36 SRAM." These notes explain how to calculate thermal resistance and how to improve thermal performance in much greater detail. Also available is Micron's *Quality and Reliability Handbook,* which gives an explanation of how thermal impedances are calculated.

SRAM

128K x 9 SRAM

WITH SINGLE CHIP ENABLE

FEATURES

- High speed: 15*, 17, 20, 25 and 35ns
- High-performance, low-power, CMOS double-metal process
- Automatic $\overline{CE}$ power down
- All inputs and outputs are TTL-compatible
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- Fast $\overline{OE}$ access time: 6ns

OPTIONS — MARKING

- Timing

15ns access	-15*
17ns access	-17
20ns access	-20
25ns access	-25
35ns access	-35

- Packages

Plastic SOJ (400 mil)	DJ

- Temperature

Commercial	(0°C to +70°C)	None
Industrial	(-40°C to +85°C)	IT
Automotive	(-40°C to +125°C)	AT
Extended	(-55°C to +125°C)	XT

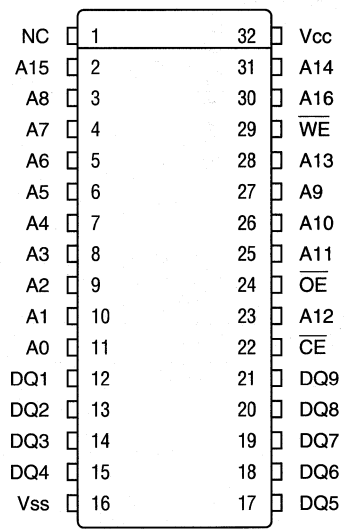
- Part Number Example: MT5C1189DJ-20

*Preliminary

NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

32-Pin SOJ
(SD-5)



GENERAL DESCRIPTION

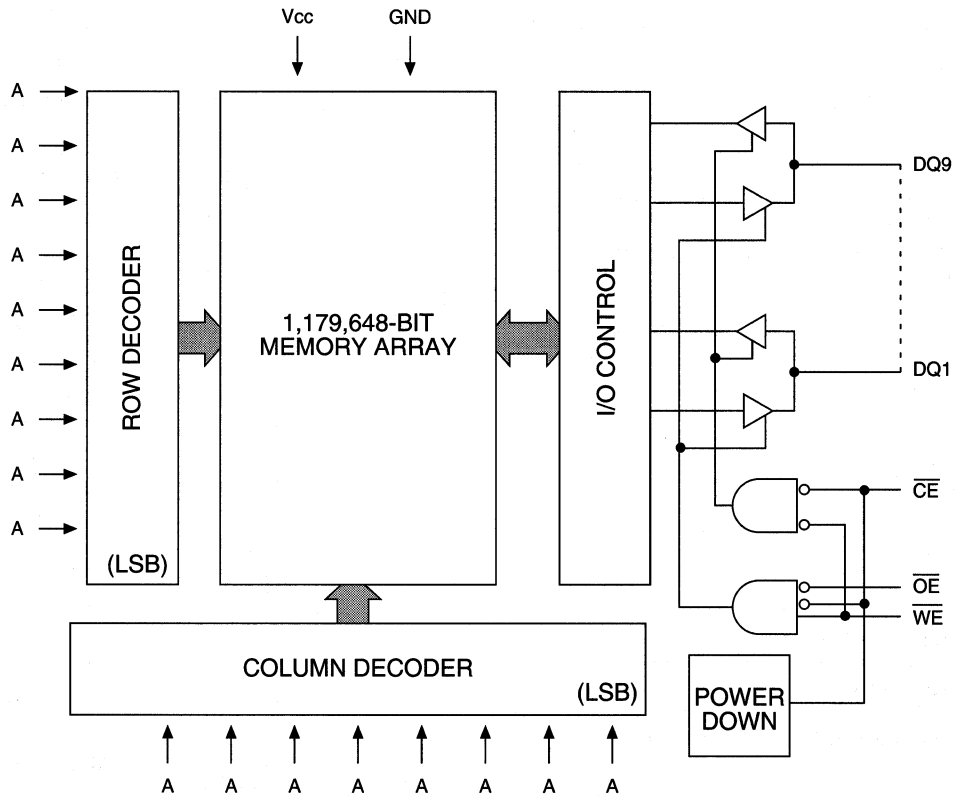
The MT5C1189 is organized as a 131,072 x 9 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) capabilities. This enhancement can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ and $\overline{OE}$ go LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL-compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA
Voltage on Any Pin Relative to V_{SS} ..... -1V to V_{CC}+1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	Vcc+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		Vcc	4.5	5.5	V	1

				MAX						
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-15**	-17	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	95	175	165	150	125	115	mA	3, 13
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	17	40	40	35	30	25	mA	13
	$\overline{CE}$ ≥ (V_{CC} -0.2V); V_{CC} = MAX All other inputs ≤ 0.2V or ≥ (V_{CC} -0.2V); f = 0Hz	I_{SB2}	0.4	5	5	5	5	5	mA	13

**Preliminary

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	6	pF	4
Output Capacitance	V_{CC} = 5V	C_O	8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION		-15*		-17		-20		-25		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle													
READ cycle time	^tRC	15		17		20		25		35		ns	
Address access time	^tAA		15		17		20		25		35	ns	
Chip Enable access time	^tACE		15		17		20		25		35	ns	
Output hold from address change	^tOH	3		5		5		5		5		ns	
Chip Enable to output in Low-Z	^tLZCE	5		5		5		5		5		ns	7
Chip disable to output in High-Z	^tHZCE		6		7		8		10		15	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		0		ns	
Chip disable to power-down time	^tPD		15		17		20		25		35	ns	
Output Enable access time	^tAOE		5		5		6		8		12	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		0		ns	
Output disable to output in High-Z	^tHZOE		5		5		6		10		12	ns	6
WRITE Cycle													
WRITE cycle time	^tWC	15		17		20		25		35		ns	
Chip Enable to end of write	^tCW	11		12		12		15		20		ns	
Address valid to end of write	^tAW	11		12		12		15		20		ns	
Address setup time	^tAS	0		0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		0		ns	
WRITE pulse width	$^tWP1$	11		12		12		15		20		ns	
WRITE pulse width	$^tWP2$	12		15		15		15		20		ns	
Data setup time	^tDS	7		7		8		10		15		ns	
Data hold time	^tDH	0		0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	3		5		5		5		5		ns	7
Write Enable to output in High-Z	^tHZWE		6		7		8		10		15	ns	6, 7

*Preliminary

INDUSTRIAL TEMPERATURE SPECIFICATIONS (IT)

The following specifications are to be used for Industrial Temperature (IT) MT5C1189 SRAMs.
(-40°C ≤ T_A ≤ 85°C)

				MAX					
DESCRIPTION	**CONDITIONS**	**SYMBOL**	**TYP**	**-20**	**-25**	**-35**	**-45**	**UNITS**	**NOTES**
Power Supply Current: Operating	CE2 ≥ V_{IH}; $\overline{CE1}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	95	150	135	125	120	mA	3, 13
Power Supply Current: Standby	CE2 ≤ V_{IH} or $\overline{CE1}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	17	35	30	25	25	mA	13
	CE2 ≤ V_{SS} +0.2V; $\overline{CE1}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	0.4	5	5	5	5	mA	13
L version only	CE2 ≤ V_{SS} +0.2V; $\overline{CE1}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	0.3	2	2	2	2	mA	13

DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	**CONDITIONS**		**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**NOTES**
Data Retention Current	$\overline{CE}$ ≥ (V_{CC} -0.2V) V_{IN} ≥ (V_{CC} -0.2V) or ≤ 0.2	V_{CC} = 2V	I_{CCDR}		35	200	µA	14
		V_{CC} = 3V	I_{CCDR}		70	400	µA	14

AUTOMOTIVE AND EXTENDED TEMPERATURE SPECIFICATIONS (AT AND XT)

The following specifications are to be used for Automotive Temperature (AT) and Extended Temperature (XT) MT5C1189 SRAMs. (-40°C ≤ T_A ≤ 125°C - AT) (-55°C ≤ T_A ≤ 125°C - XT)

				MAX					
DESCRIPTION	**CONDITIONS**	**SYMBOL**	**TYP**	**-20**	**-25**	**-35**	**-45**	**UNITS**	**NOTES**
Power Supply Current: Operating	CE2 ≥ V_{IH}; $\overline{CE1}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	95	165	140	125	120	mA	3, 13
Power Supply Current: Standby	CE2 ≤ V_{IH} or $\overline{CE1}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	17	45	40	35	32	mA	13
	CE2 ≤ V_{SS} +0.2V; $\overline{CE1}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	0.4	7	7	7	7	mA	13
L version only	CE2 ≤ V_{SS} +0.2V; $\overline{CE1}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	0.3	5	5	5	5	mA	13

DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	**CONDITIONS**		**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**NOTES**
Data Retention Current	$\overline{CE}$ ≥ (V_{CC} -0.2V) or V_{IN} ≥ (V_{CC} -0.2V) or ≤ 0.2V	V_{CC} = 2V	I_{CCDR}		35	1,000	µA	14
		V_{CC} = 3V	I_{CCDR}		70	1,500	µA	14

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

Refer to commercial temperature timing parameters for specifications not listed here.
(Notes 5, 14) (-40°C ≤ T_A ≤ 125°C; -55°C ≤ T_A ≤ 125°C; V_{CC} = 5V ±10%)

DESCRIPTION		-20		-25		-35		-45			
	SYM	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ Cycle											
Output hold from address change	^tOH	3		3		3		3		ns	
Chip Enable to output in Low-Z	^tLZCE	3		3		3		3		ns	7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

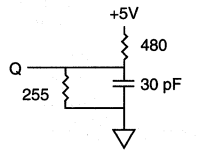


Fig. 1 OUTPUT LOAD EQUIVALENT

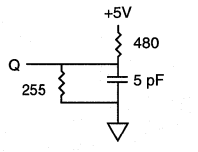
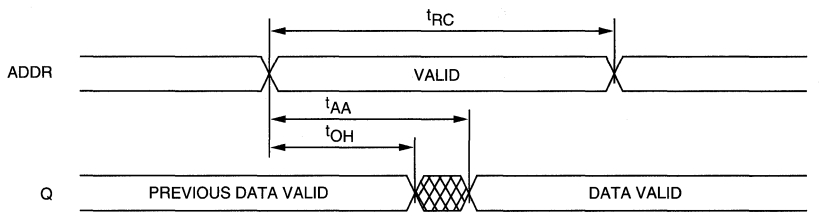


Fig. 2 OUTPUT LOAD EQUIVALENT

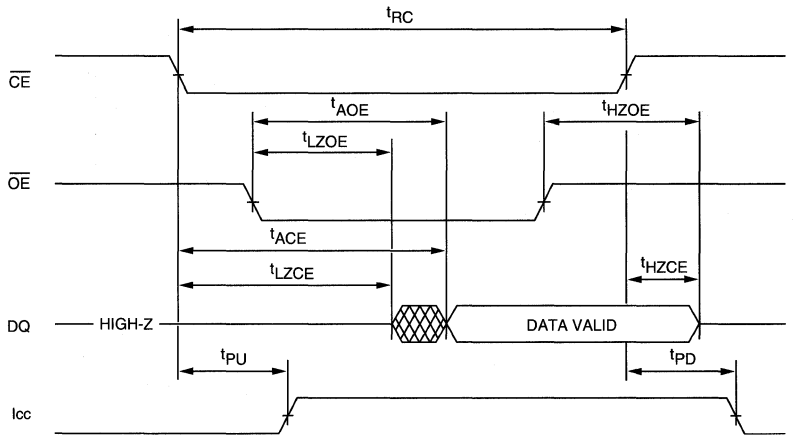
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < $^tRC/2$.
3. Icc is dependent on output loading and cycle rates. The specified value applies with the outputs unloaded, and $f = \frac{1}{^tRC\ (MIN)}$ Hz.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^tHZCE, ^tHZOE and ^tHZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^tHZCE is less than ^tLZCE, and ^tHZWE is less than ^tLZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables and output enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^tRC = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Typical values are measured at 5V, 25°C and 25ns cycle time.
14. Typical currents are measured at 25°C.
15. Output enable ($\overline{OE}$) is inactive (HIGH).
16. Output enable ($\overline{OE}$) is active (LOW).

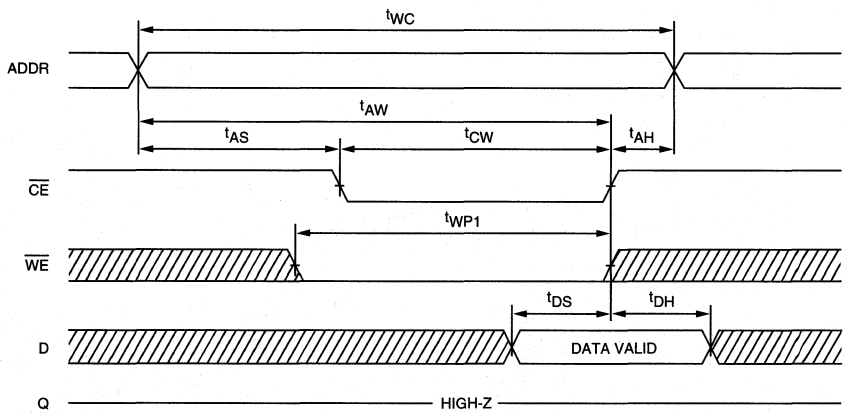
READ CYCLE NO. 1 [8, 9]



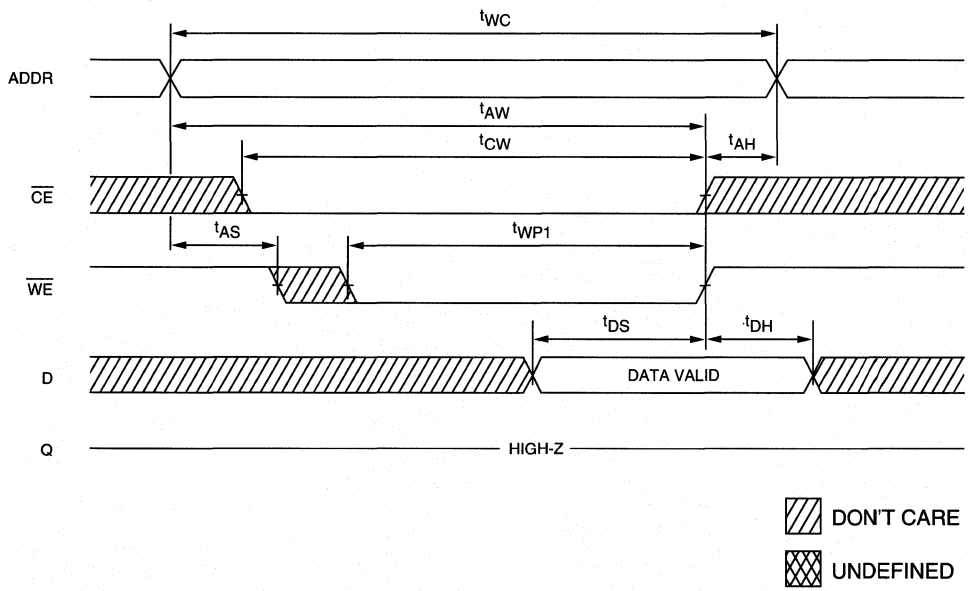
READ CYCLE NO. 2 [7, 8, 10]



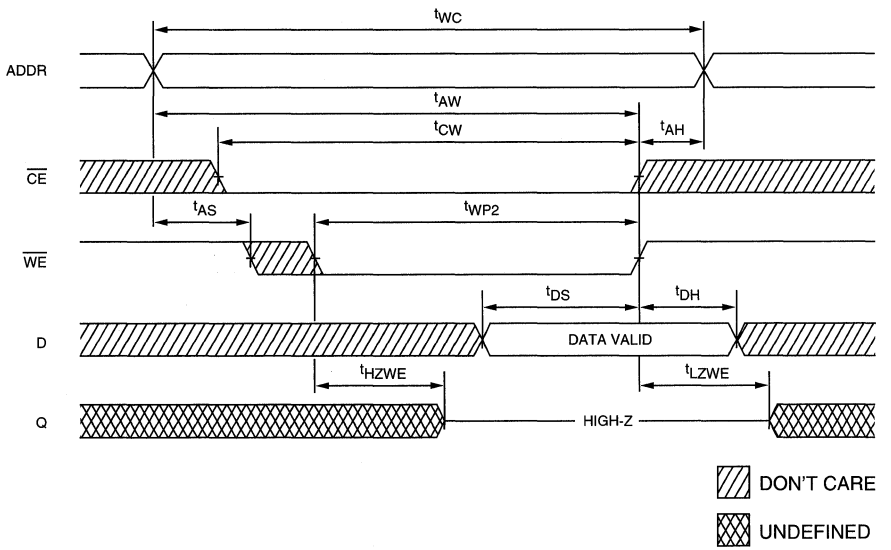
WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)



WRITE CYCLE NO. 2 [12, 15]
(Write Enable Controlled)



WRITE CYCLE NO. 3 [7, 12, 16]
(Write Enable Controlled)



MICRON SEMICONDUCTOR, INC.

MT5C64K16A1
REVOLUTIONARY PINOUT 64K x 16 SRAM

SRAM

64K x 16 SRAM

WITH OUTPUT ENABLE, REVOLUTIONARY PINOUT

FEATURES

- Fast access times: 12, 15, 20 and 25ns
- Fast output enable access time: 6, 8, 10 and 12ns
- Multiple center power and ground pins for improved noise immunity
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Individual byte controls for both READ and WRITE cycles
- All inputs and outputs are TTL-compatible

OPTIONS MARKING

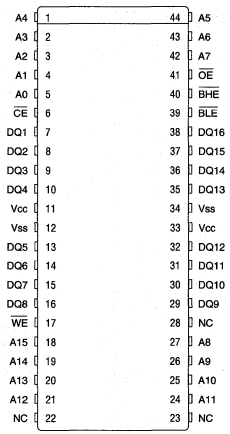
- Timing
  - 12ns access -12
  - 15ns access -15
  - 20ns access -20
  - 25ns access -25
- Packages
  - 44-pin SOJ (400 mil) DJ
  - 44-pin TSOP (400 mil) TG
- 2V data retention L
- Temperature
  - Commercial (0°C to +70°C) None
  - Industrial (-40°C to +85°C) IT*
  - Automotive (-40°C to +125°C) AT*
  - Extended (-55°C to +125°C) XT*
- Part Number Example: MT5C64K16A1DJ-15

* Contact factory for specifications and avilability.

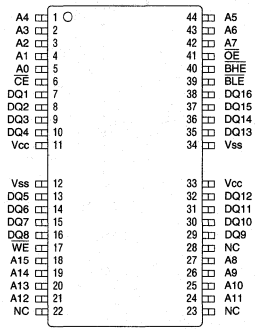
NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

44-Pin SOJ (SD-7)



44-Pin TSOP (SE-3)



GENERAL DESCRIPTION

The MT5C64K16A1 is organized as a 65,536 x 16 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

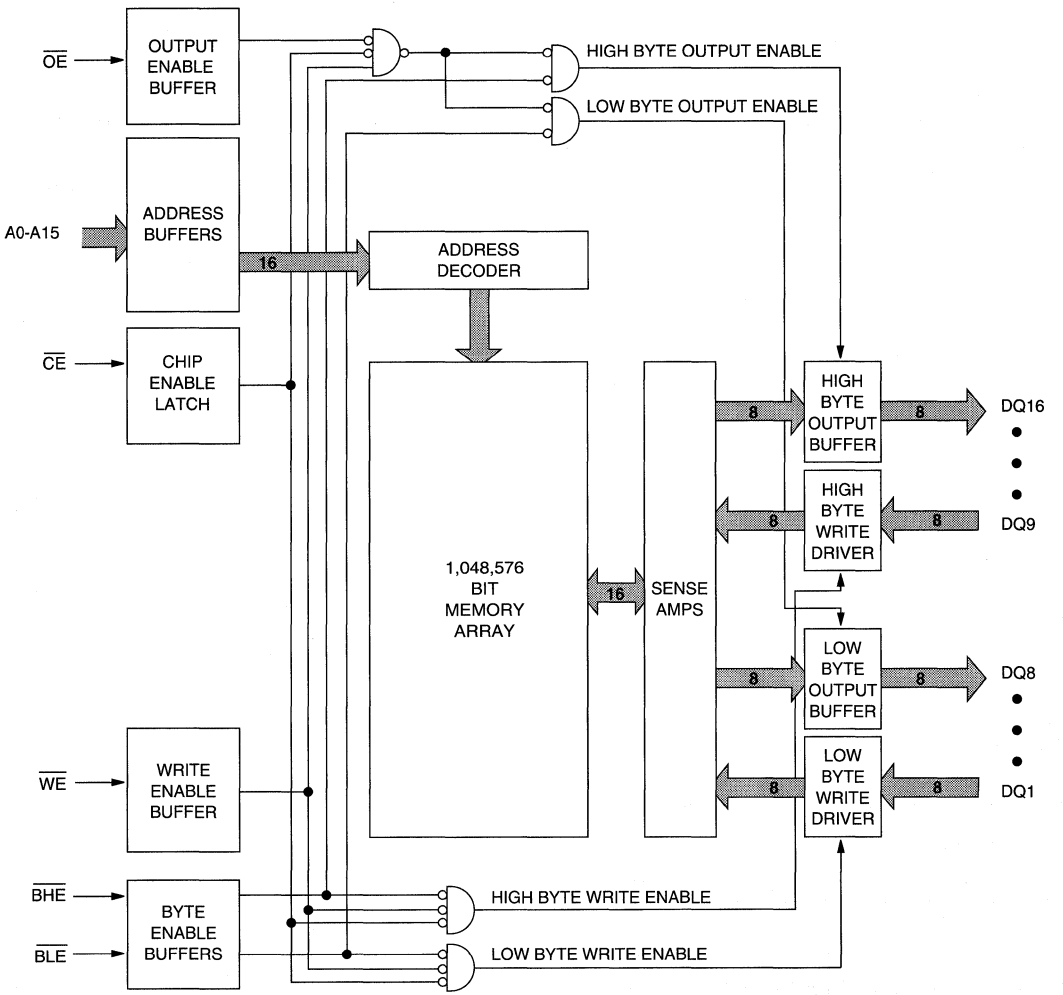
This device offers multiple center power and ground pins for improved performance. For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) capabilities. This enhancement can place the output pin in High-Z for additional flexibility in sytem design.

The MT5C64K16A1 SRAM integrates a 64K x 16 SRAM core with peripheral circuitry consisting of active LOW chip enable, separate upper and lower byte enables and a fast output enable.

Separate byte enable controls ($\overline{BLE}$ and $\overline{BHE}$) allow individual bytes to be written and read. $\overline{BLE}$ controls DQ1-DQ8, the lower bits. $\overline{BHE}$ controls DQ9-DQ16, the upper bits.

The MT5C64K16A1 operates from a single +5V power supply and all inputs and outputs are fully TTL-compatible.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

SOJ and TSOP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
5, 4, 3, 2, 1, 44, 43, 42, 27, 26, 25, 24, 21, 20, 19, 18	A0-A15	Input	Address Inputs: These inputs determine which cell is accessed.
17	$\overline{WE}$	Input	Write Enable: This input determines if the cycle is a READ or WRITE cycle. $\overline{WE}$ is LOW for a WRITE cycle and HIGH for a READ cycle
39, 40	$\overline{BLE}$, $\overline{BHE}$	Input	Byte Enables: These active LOW inputs allow individual bytes to be written or read. When $\overline{BLE}$ is LOW, data is written or read to the lower byte, DQ1-DQ8. When $\overline{BHE}$ is LOW, data is written or read to the upper byte, DQ9-DQ16.
6	$\overline{CE}$	Input	Chip Enable: This signal is used to enable the device. When $\overline{CE}$ is HIGH, the chip automatically goes into standby power mode.
41	$\overline{OE}$	Input	Output Enable: This active LOW input enables the output drivers.
22, 23, 28	NC	-	No Connect: These signals are not internally connected.
7, 8, 9, 10, 13, 14, 15, 16, 29, 30, 31, 32, 35, 36, 37, 38	DQ1-DQ16	Input/ Output	SRAM Data I/O: Lower byte is DQ1-DQ8; Upper byte is DQ9-DQ16.
11, 33	Vcc	Supply	Power Supply: +5V ±10%
12, 34	Vss	Supply	Ground: GND

TRUTH TABLE

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	DQ1-DQ8	DQ9-DQ16	POWER
STANDBY	H	X	X	X	X	HIGH-Z	HIGH-Z	STANDBY
LOW BYTE READ (DQ1-DQ8)	L	L	H	L	H	D	HIGH-Z	ACTIVE
HIGH BYTE READ (DQ9-DQ16)	L	L	H	H	L	HIGH-Z	D	ACTIVE
WORD READ (DQ1-DQ16)	L	L	H	L	L	D	D	ACTIVE
WORD WRITE (DQ1-DQ16)	L	X	L	L	L	Q	Q	ACTIVE
LOW BYTE WRITE (DQ1-DQ8)	L	X	L	L	H	Q	HIGH-Z	ACTIVE
HIGH BYTE WRITE (DQ9-DQ16)	L	X	L	H	L	HIGH-Z	Q	ACTIVE
OUTPUT DISABLE	L	H	H	X	X	HIGH-Z	HIGH-Z	ACTIVE
	L	X	X	H	H	HIGH-Z	HIGH-Z	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1V to 7V
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1.7W
Short Circuit Output Current 50mA
Voltage at Any Pin Relative to V_{SS} ..... -1V to V_{CC}+1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; V_{CC} = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

				MAX					
DESCRIPTION	CONDITIONS	SYMBOL	TYPICAL	-12	-15	-20	-25	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX outputs open f = MAX = 1/ ^tRC	I_{CC}	150	300	260	220	200	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX outputs open f = MAX = 1/ ^tRC	I_{SB1}	25	50	45	40	35	mA	
	$\overline{CE} \ge V_{CC}$ - 0.2V V_{CC} = MAX; $V_{IN} \le V_{SS}$ +0.2V or $V_{IN} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	0.5	5	5	5	5	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1MHz	C_I		6	pF	4
Input/Output Capacitance (D/Q)	V_{CC} = 5V	$C_{I/O}$		6	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 5, 14) ($0°C \le T_A \le 70°C$; $V_{CC} = 5V \pm 10\%$)

DESCRIPTION		-12		-15		-20		-25			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle											
READ cycle time	^tRC	12		15		20		25		ns	
Address access time	^tAA		12		15		20		25	ns	
Chip Enable access time	^tACE		12		15		20		25	ns	
Output hold from address change	^tOH	4		4		5		5		ns	
Chip Enable to output in Low-Z	^tLZCE	4		5		5		5		ns	6, 7
Chip disable to output in High-Z	^tHZCE		6		6		8		8	ns	6, 7
Output Enable access time	^tAOE		6		8		10		12	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		ns	6, 7
Output disable to output in High-Z	^tHZOE		6		6		8		8	ns	6, 7
Byte Enable access time	^tABE		6		8		10		12	ns	
Byte Enable to output in Low-Z	^tLZBE	0		0		0		0		ns	6, 7
Byte disable to output in High-Z	^tHZBE		6		6		8		8	ns	6, 7
WRITE Cycle											
WRITE cycle time	^tWC	12		15		20		25		ns	
Chip Enable to end of write	^tCW	10		12		13		15		ns	
Address valid to end of write	^tAW	8		9		12		14		ns	
Address setup time	^tAS	0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		ns	
Write pulse width	^tWP	8		9		10		12		ns	
Data setup time	^tDS	6		8		10		10		ns	
Data hold time	^tDH	0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	1		1		1		1		ns	6, 7
Write Enable to output in High-Z	^tHZWE		6		6		8		8	ns	6, 7
Byte Enable to end of write	^tBW	8		9		12		14		ns	

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

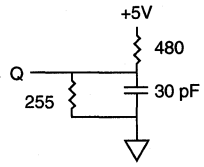


Fig. 1 OUTPUT LOAD EQUIVALENT

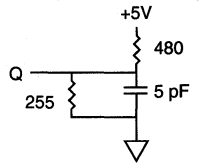


Fig. 2 OUTPUT LOAD EQUIVALENT

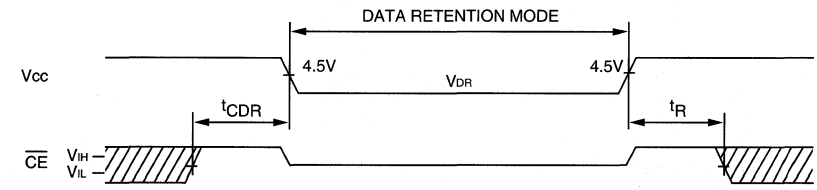
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. Output loading is specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE, ^{t}HZOE is less than ^{t}LZOE, and ^{t}HZBE is less than ^{t}LZBE.
8. Any combination of write enable, chip enable and byte enable can initiate and terminate a WRITE cycle.
9. $\overline{WE}$ is HIGH for READ cycle.
10. Device is continuously selected. Chip enable is held in its active state.
11. Address valid prior to, or coincident with, the latest occurring chip enable.
12. $\overline{BHE}$ and $\overline{BLE}$ are held in their active state (LOW).
13. The output will be in the High-Z state if output enable is HIGH.
14. Contact Micron for IT/AT/XT timing and current specifications; they may differ from the commercial temperature range specifications shown in this data sheet.
15. Typical currents are measured at 25°C.

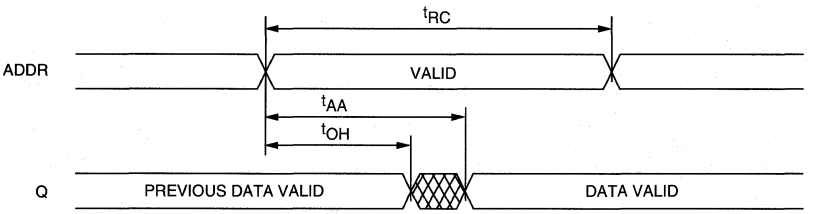
DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			V_{DR}	2			V	
Data Retention Current L version	$\overline{CE}$ ≥ (Vcc -0.2V) V_{IN} ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	I_{CCDR}		TBD	TBD	µA	15
		Vcc = 3V	I_{CCDR}		TBD	TBD	µA	15
Chip Deselect to Data Retention Time			^{t}CDR	0			ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

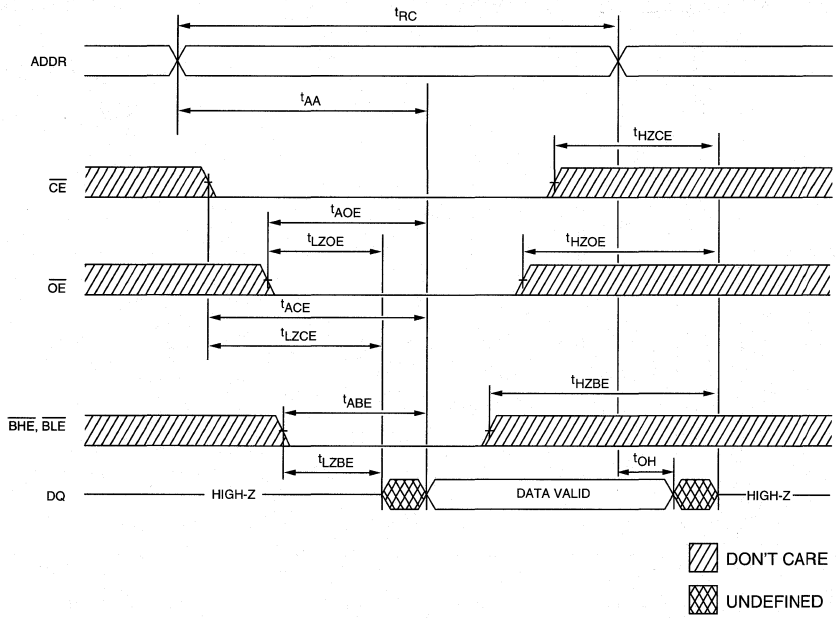
LOW Vcc DATA RETENTION WAVEFORM



READ CYCLE NO. 1 [9, 10, 12]

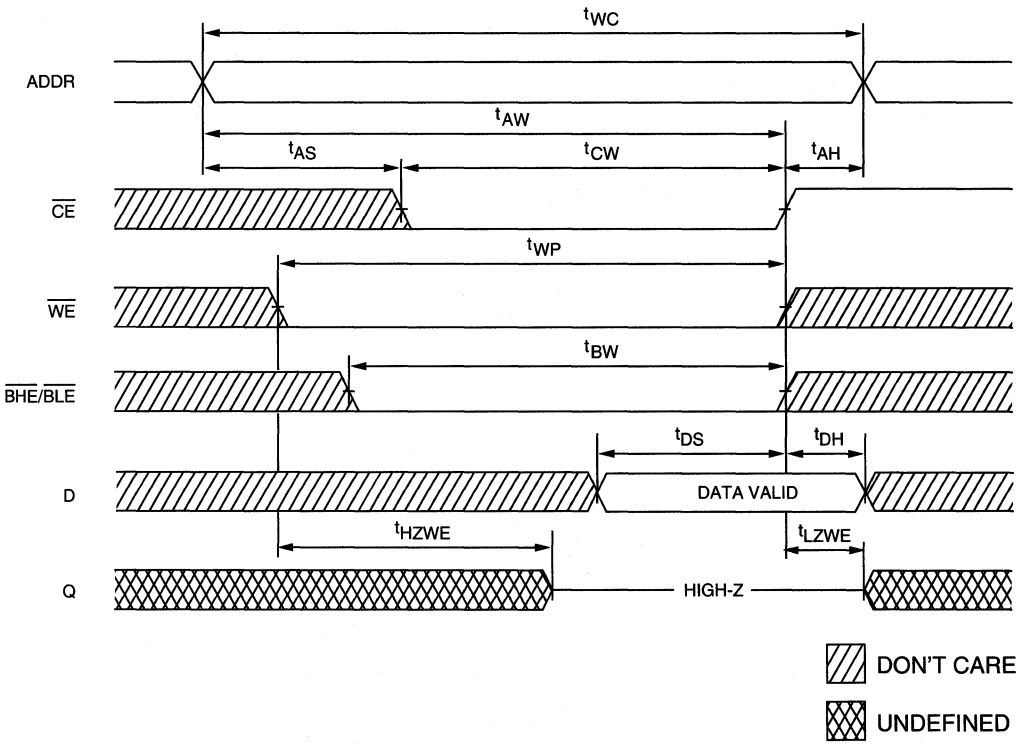


READ CYCLE NO. 2 [7, 9]



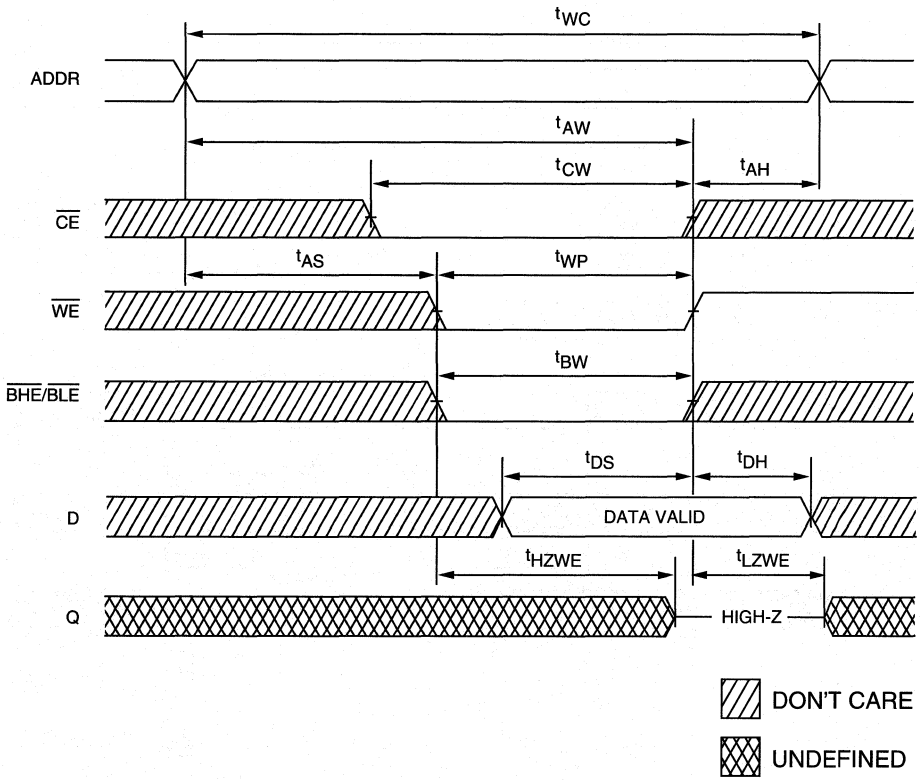
WRITE CYCLE NO. 1 [8, 13]

Chip Enable Controlled



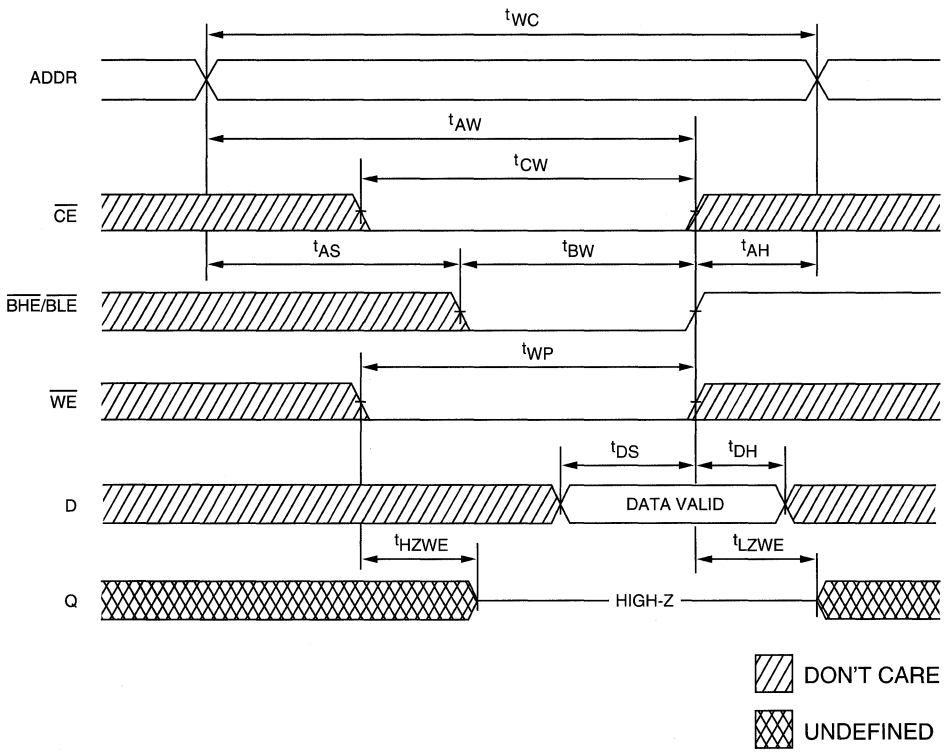
WRITE CYCLE NO. 2 [8, 13]

Write Enable Controlled



WRITE CYCLE NO. 3 [8, 13]

Byte Enable Controlled



SRAM

256K x 16 SRAM

WITH OUTPUT ENABLE

FEATURES

- High speed: 12, 15, 20, 25 and 35ns
- Multiple center power and ground pins for improved noise immunity
- Single +5V ±10% power supply
- Easy memory expansion with chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) options
- All inputs and outputs are TTL-compatible
- Automatic $\overline{CE}$ power-down
- Fast $\overline{OE}$ access time: 6, 8, 10, 12 and 15ns
- High-performance, low-power, CMOS double-metal process

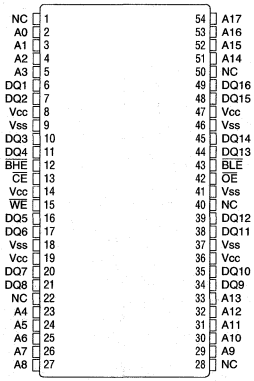
OPTIONS — MARKING

- Timing
  - 12ns access — -12
  - 15ns access — -15
  - 20ns access — -20
  - 25ns access — -25
  - 35ns access — -35
- Packages
  - Plastic SOJ (400 mil) — DJ
  - Plastic TSOP (400 mil) — TG
- 2V data retention — L
- Low power — P
- Temperature
  - Commercial (0°C to +70°C) — None
  - Industrial (-40°C to +85°C) — IT
  - Automotive (-40°C to +125°C) — AT
  - Extended (-55°C to +125°C) — XT
- Part Number Example: MT5C256K16B2DJ-15 L

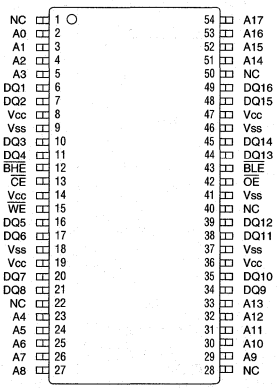
NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

54-Pin SOJ* (SD-8)



54-Pin TSOP* (SE-4)



* JEDEC-proposed pinout (SOJ lead pitch is 0.8mm)

GENERAL DESCRIPTION

The MT5C256K16B2 is organized as a 262,144 x 16 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron 4 Meg SRAMs are fabricated using a double-layer metal, triple-layer polysilicon technology.

This device offers multiple center power and ground pins for improved performance. For flexibility in high-speed memory applications, Micron offers $\overline{CE}$ and $\overline{OE}$ capabilities. These enhancements can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW and the appropriate byte enables ($\overline{BHE}$ and $\overline{BLE}$) are in their proper states.

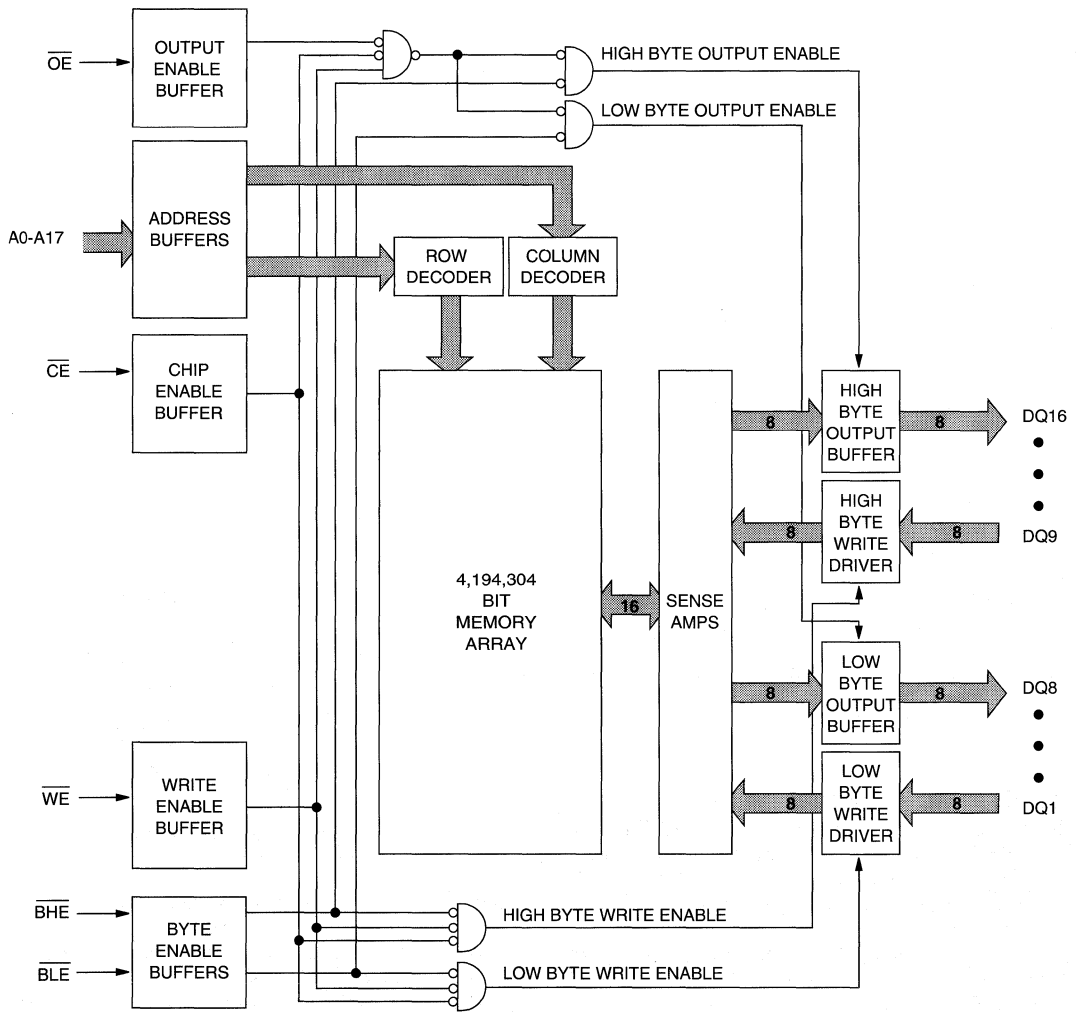
Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ and $\overline{OE}$ go LOW and the appropriate byte enables ($\overline{BHE}$ and $\overline{BLE}$) are in their proper states. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

Separate byte enable controls ($\overline{BLE}$ and $\overline{BHE}$) allow individual bytes to be written and read. $\overline{BLE}$ controls the lower bits (DQ1-DQ8). $\overline{BHE}$ controls the upper bits (DQ9-DQ16).

The "P" version provides a 90 percent reduction in TTL standby current (I_{SB1}). This is achieved by including gated inputs on the design. The gated inputs also facilitate the design of battery-backed systems where the designer needs to protect against inadvertent battery current drain during power-down when inputs may be at undefined levels.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL-compatible.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

SOJ and TSOP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
2-5, 23-27, 29-33 51-54	A0-A17	Input	Address Inputs: These inputs determine which cell is accessed.
15	$\overline{WE}$	Input	Write Enable: This input determines if the cycle is a READ or WRITE cycle. $\overline{WE}$ is LOW for a WRITE cycle and HIGH for a READ cycle
12, 43	$\overline{BHE}$, $\overline{BLE}$	Input	Byte Enables: These active LOW inputs allow individual bytes to be written or read. When $\overline{BLE}$ is LOW, data is written to or read from the lower byte, D1-D8. When $\overline{BHE}$ is LOW, data is written to or read from the upper byte, D9-D16.
13	$\overline{CE}$	Input	Chip Enable: This signal is used to enable the device. When $\overline{CE}$ is HIGH, the chip goes into standby power mode.
42	$\overline{OE}$	Input	Output Enable: This active LOW input enables the output drivers.
1, 22, 28, 40, 50	NC	-	No Connect: These signals are not internally connected.
6, 7, 10, 11, 16, 17, 20, 21, 34, 35, 38, 39, 44, 45, 48, 49	DQ1-DQ16	Input/ Output	SRAM Data I/O: Lower byte is DQ1-DQ8; upper byte is DQ9-DQ16.
8, 14, 19, 36, 47	Vcc	Supply	Power Supply: +5V ±10%
9, 18, 37, 41, 46	Vss	Supply	Ground: GND

TRUTH TABLE

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	DQ1-DQ8	DQ9-DQ16	POWER
STANDBY	H	X	X	X	X	HIGH-Z	HIGH-Z	STANDBY
LOW BYTE READ (DQ1-DQ8)	L	L	H	L	H	D	HIGH-Z	ACTIVE
HIGH BYTE READ (DQ9-DQ16)	L	L	H	H	L	HIGH-Z	D	ACTIVE
WORD READ (DQ1-DQ16)	L	L	H	L	L	D	D	ACTIVE
WORD WRITE (DQ1-DQ16)	L	X	L	L	L	Q	Q	ACTIVE
LOW BYTE WRITE (DQ1-DQ8)	L	X	L	L	H	Q	HIGH-Z	ACTIVE
HIGH BYTE WRITE (DQ9-DQ16)	L	X	L	H	L	HIGH-Z	Q	ACTIVE
OUTPUT DISABLE	L	H	H	X	X	HIGH-Z	HIGH-Z	ACTIVE
	L	X	X	H	H	HIGH -Z	HIGH-Z	ACTIVE

THERMAL IMPEDENCE (EST)[18]

PACKAGE	NUMBER OF PINS	θ_{JC}* (°C/W)	θ_{JA}* (°C/W)
SOJ	54	15	55
TSOP	54	5	65

*The thermal impedence numbers assume the device is socketted on a PC board and air flow is zero.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Storage Temperature (plastic) ..... -55°C to +150°C
Short Circuit Output Current 50mA
Voltage on Any Pin Relative to V_{SS} ..... -1V to V_{CC}+1
Junction Temperature** ..... +150°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Maximum junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow. See the Application Information section at the end of this data sheet for more information.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-2	2	µA	
Output Leakage Current	Output(s) disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-2	2	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

				MAX						
DESCRIPTION	CONDITIONS	SYMBOL	VER	-12	-15	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	ALL	200	180	175	170	160	mA	3
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	STD	35	30	25	25	20	mA	
			P	2	2	2	2	2	mA	
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	STD	2	2	2	2	2	mA	
			P	2	2	2	2	2	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	5	pF	4
Output Capacitance	V_{CC} = 5V	C_O	7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 5, 15) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION		-12		-15		-20		-25		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle													
READ cycle time	^tRC	12		15		20		25		35		ns	
Address access time	^tAA		12		15		20		25		35	ns	
Chip Enable access time	^tACE		12		15		20		25		35	ns	
Output hold from address change	^tOH	3		3		3		3		3		ns	
Chip Enable to output in Low-Z	^tLZCE	3		3		5		5		5		ns	7
Chip disable to output in High-Z	^tHZCE		6		7		8		10		15	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		0		ns	
Chip disable to power-down time	^tPD		12		15		20		25		35	ns	
Output Enable access time	^tAOE		6		8		10		12		15	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		0		ns	
Output disable to output in High-Z	^tHZOE		5		6		7		10		12	ns	6
Byte Enable access time	^tABE		7		8		10		12		15	ns	
Byte Enable to output in Low-Z	^tLZBE	0		0		0		0		0		ns	
Byte Enable to output in High-Z	^tHZBE		7		8		8		8		10	ns	6
WRITE Cycle													
WRITE cycle time	^tWC	12		15		20		25		35		ns	
Chip Enable to end of WRITE	^tCW	8		10		12		15		20		ns	
Address valid to end of WRITE	^tAW	8		10		12		15		20		ns	
Address setup time	^tAS	0		0		0		0		0		ns	
Address hold from end of WRITE	^tAH	0		0		0		0		0		ns	
WRITE pulse width1	$^tWP1$	8		9		10		15		20		ns	
WRITE pulse width2	$^tWP2$	9		11		12		17		22		ns	
Data setup time	^tDS	6		7		8		10		15		ns	
Data hold time	^tDH	0		0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	3		3		4		5		5		ns	7
Write Enable to output in High-Z	^tHZWE		5		6		8		10		15	ns	6, 7
Byte Enable to end of WRITE	^tBW	8		9		12		14		18		ns	

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

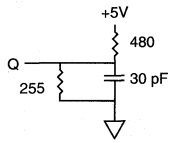


Fig. 1 OUTPUT LOAD EQUIVALENT

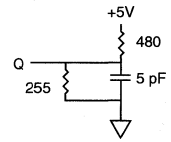


Fig. 2 OUTPUT LOAD EQUIVALENT

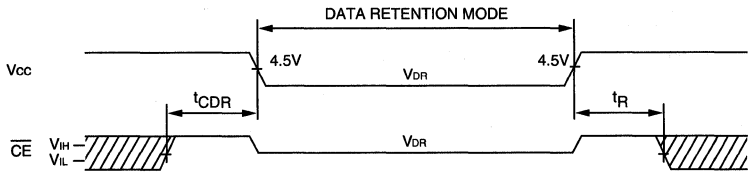
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZOE, ^{t}HZBE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE, and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. Chip enables and output enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC = READ cycle time.
12. Any combination of $\overline{WE}$, $\overline{CE}$ and byte enables can initiate and terminate a WRITE cycle.
13. $\overline{BLE}$ and $\overline{BLH}$ determine what outputs are active during the READ cycle.
14. The output will be in a High-Z state if $\overline{OE}$ is HIGH.
15. Contact Micron for IT/AT/XT timing and current specifications; they may differ from the commercial temperature range specifications shown in this data sheet.
16. Output enable ($\overline{OE}$) is inactive (HIGH).
17. Output enable ($\overline{OE}$) is active (LOW).
18. Micron does not warrant functionality nor reliability of any product in which the junction temperature exceeds 150°C. Care should be taken to limit power to acceptable levels.

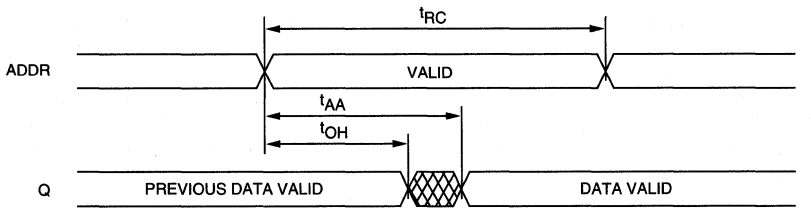
DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP versions only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2		V	
Data Retention Current L version	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	ICCDR		1	mA	
		Vcc = 3V	ICCDR		1.5	mA	
Data Retention Current LP version	$\overline{CE}$ ≥ (Vcc -0.2V)	Vcc = 2V	ICCDR		1	mA	
		Vcc = 3V	ICCDR		1.5	mA	
Chip Deselect to Data Retention Time			^{t}CDR	0		ns	4
Operation Recovery Time			^{t}R	^{t}RC		ns	4, 11

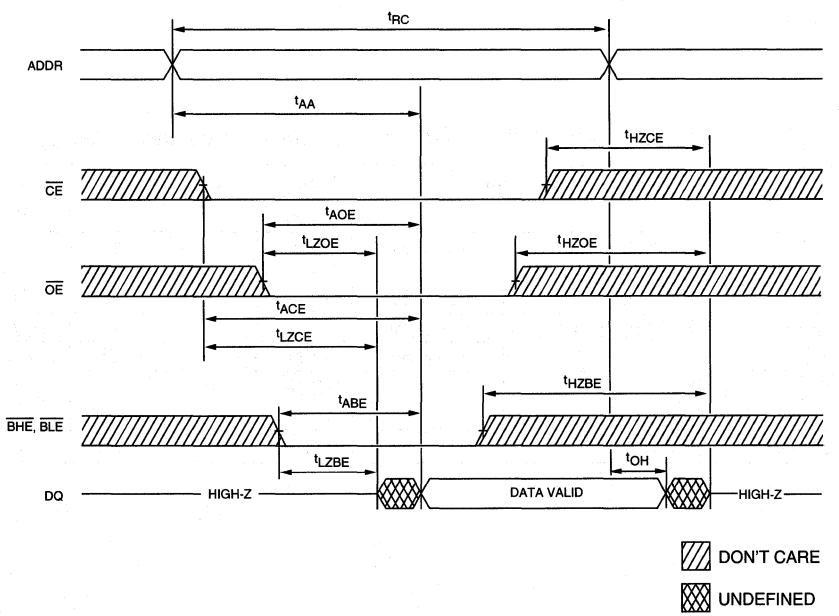
LOW Vcc DATA RETENTION WAVEFORM



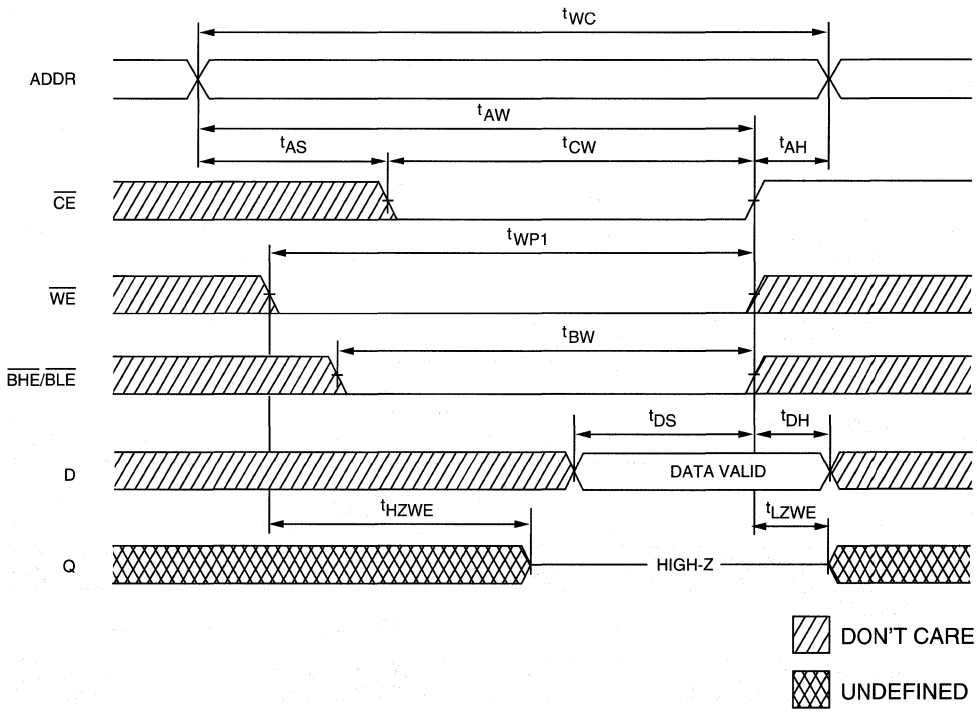
READ CYCLE NO. 1 [8, 9, 13]



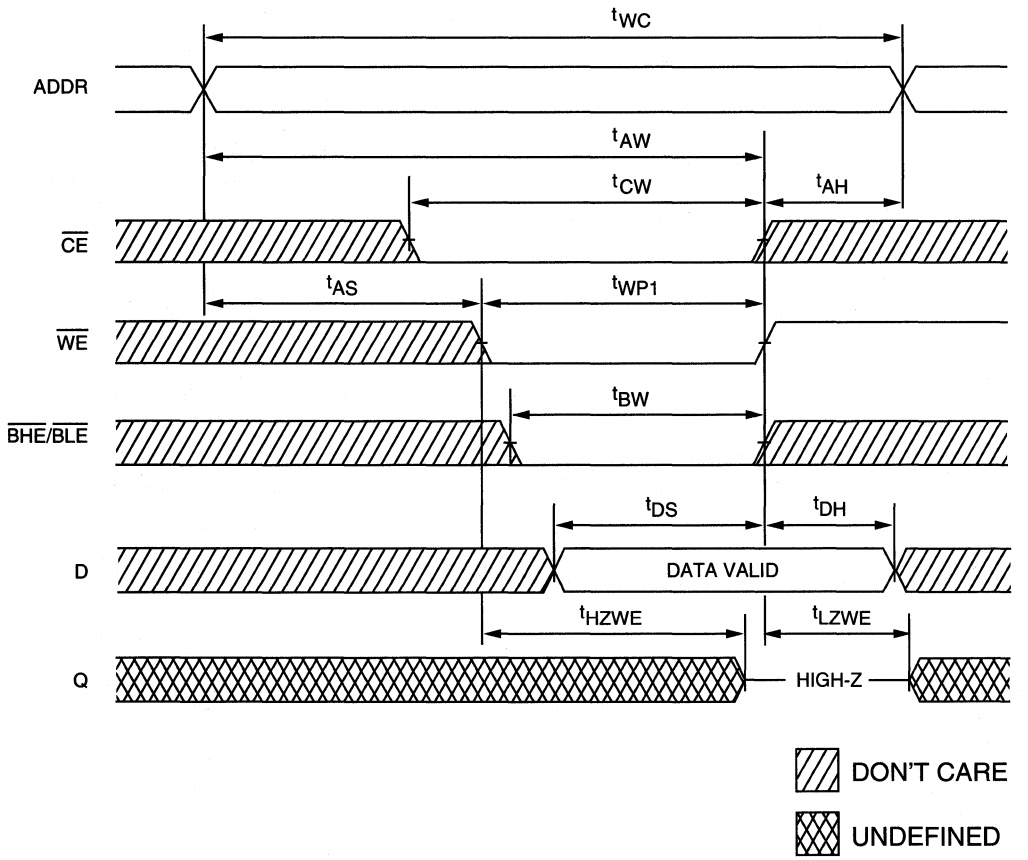
READ CYCLE NO. 2 [7, 8, 10]



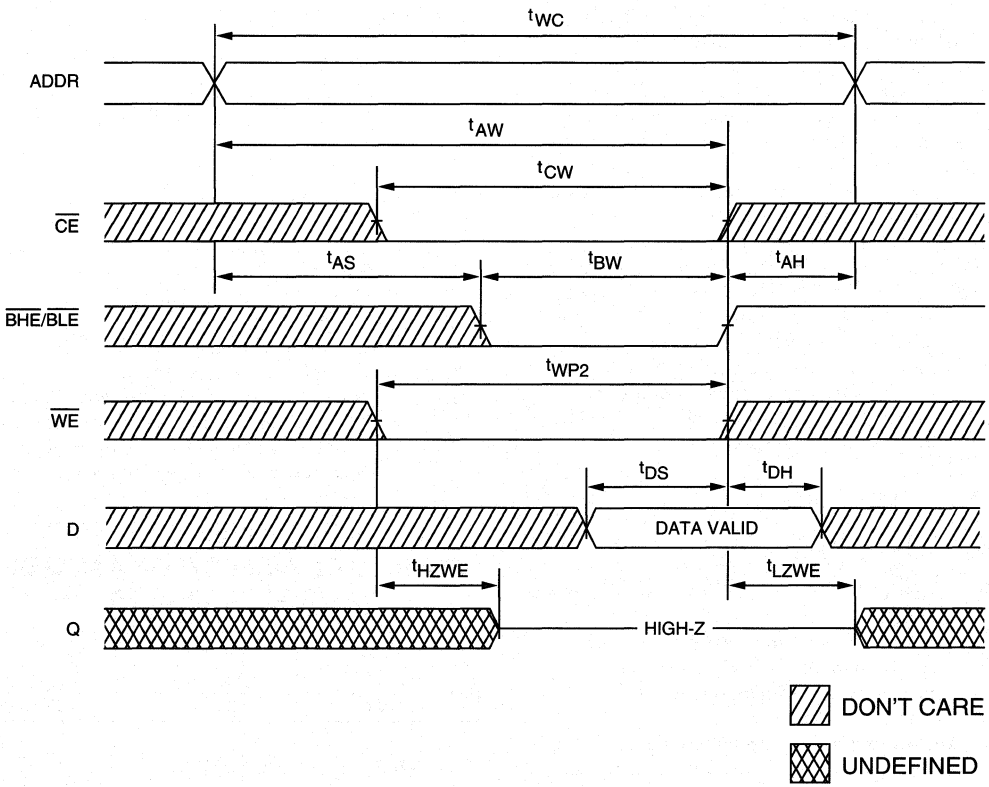
WRITE CYCLE NO. 1 [12, 14]
(Chip Enable Controlled)



WRITE CYCLE NO. 2 [7, 12, 14, 16]
(Write Enable Controlled)



WRITE CYCLE NO. 3 [7, 12, 14, 17]
(Byte Enable Controlled)



APPLICATION INFORMATION

THERMAL CONSIDERATIONS

This section describes how to determine the junction temperature during operating conditions. It is essential that the maximum junction temperature of the 4 Meg SRAM is not exceeded. If this temperature is exceeded it is necessary to add external cooling such as forced airflow or change the operating conditions. The maximum junction temperature for Micron SRAMs is 150°C. The limiting temperature factor is not the SRAM but the mold compound which prevents reliable operating temperatures significantly about 150°C. However, it is advisable to run the part as cool as possible since reliability (FIT rates) are exponentially dependent upon junction temperature.

The calculation of the actual junction temperature begins with the power calculation and then the junction temperation calculation. Equations 1 and 2 below show how T_j is determined using the ambient temperature, thermal resistance and operating power. If an airflow is introduced into a system then Equation 2 should be used with an airflow thermal multiplier. Specific thermal resistances are given in Micron technical note "SRAM Thermal Design Considerations" and in individual data sheets.

$$T_j = T_A + P * \theta_{JA} \quad (1)$$

$$T_j = T_A + P * \theta_{JA} * \theta_M \quad (2)$$

T_j = Junction temperature of the active portion of the silicon die (°C)
T_A = Ambient air temperature (°C) at which the device is operated
P = Average power dissipation of the device (W)
θ_{JA} = Junction to ambient thermal resistance (°C/W)
θ_M = Airflow multiplier. This value changes for different values of airflow over the part (fpm).

To solve the above equations the average operating power must be calculated. Total power has three separate components (P_1, P_2 and P_3). P_1 is the operating power dissipated by the chip, P_2 is the AC output power due to the capacitive load and P_3 is the DC output power due to TTL DC load current (P_3 is usually negligible). For this example we have chosen P_2 such that outputs are switching from a logic LOW state to a logic HIGH state which gives the worst case output AC current. A complete description of these equations and their derivation is given in Micron technical note "Design Tips: 32K x 36 SRAM."

$$P_1 = V_{CC} I_{CC}$$

$$P_2 = \frac{C_L}{T} \left(V_{CC} [V_{OH} - V_{OL}] - 0.5 [V_{OH}^2 - V_{OL}^2] \right) N_S$$

$$P_3 = (V_{CC} - V_{OH}) I_O N_H + V_{OL} I_I N_L.$$

V_{CC} = Supply voltage
I_{CC} = Supply current
C_L = Capacitive output loading
T = Clock period
V_{OH} = Output high voltage
V_{OL} = Output low voltage
I_O = Output current on DQ lines which are high
I_I = Input current on DQ lines which are low
N_H = Number of DQ lines which are high
N_L = Number of DQ lines which are low.

Table 1
EFFECTS OF AIRFLOW ON 4 MEG SRAM SOJ PACKAGES

Package	Air Flow	θ_M Multiplier
PSOJ	200 fpm	0.7 - 0.75
PSOJ	500 fpm	0.55 - 0.65

ADDITIONAL INFORMATION

For more information on thermal considerations see Micron's technical notes, "SRAM Thermal Design Considerations" and "Design Tips: 32K x 36 SRAM." These notes explain how to calculate thermal resistance and how to improve thermal performance in much greater detail. Also available is Micron's *Quality and Reliability Handbook,* which gives an explanation of how thermal impedances are calculated.

MICRON
SEMICONDUCTOR, INC.

3.3V SRAM PRODUCT SELECTION GUIDE

Memory Configuration	Control Functions	Part Number	Access Time (ns)	Package and Number of Pins			Page
				PDIP	SOJ	TSOP	
256K x 1	$\overline{CE}$ only with separate I/O	MT5LC2561	12, 15, 20, 25, 35	24	24	-	2-1
1 Meg x 1	$\overline{CE}$ only with separate I/O	MT5LC1001	15, 17, 20, 25, 35, 45	28	28	-	2-9
64K x 4	$\overline{CE}$ only	MT5LC2564	12, 15, 20, 25, 35	24	24	-	2-17
64K x 4	$\overline{CE}$ and $\overline{OE}$	MT5LC2565	12, 15, 20, 25, 35	28	28	-	2-25
256K x 4	$\overline{CE}$ and $\overline{OE}$	MT5LC1005	15, 17, 20, 25, 35, 45	28	28	-	2-33
256K x 4	$\overline{CE}$ and Revolutionary Pinout	MT5LC256K4D4	15, 20, 25	-	32	32	2-41
1 Meg x 4	$\overline{CE}$, $\overline{OE}$ and Revolutionary Pinout	MT5LC1M4D4	12, 15, 20, 25, 35	-	32	32	2-51
32K x 8	$\overline{CE}$ and $\overline{OE}$	MT5LC2568	12, 15, 20, 25, 35	28	28	-	2-59
128K x 8	$\overline{CE1}$, CE2 and $\overline{OE}$	MT5LC1008	15, 17, 20, 25, 35, 45	32	32	-	2-67
128K x 8	$\overline{CE}$, $\overline{OE}$ and Revolutionary Pinout	MT5LC128K8D4	15, 20, 25	-	32	32	2-75
512K x 8	$\overline{CE}$, $\overline{OE}$ and Revolutionary Pinout	MT5LC512K8D4	12, 15, 20, 25, 35	-	36	36	2-85
64K x 16	$\overline{CE}$, $\overline{OE}$, Byte Enable and Revolutionary Pinout	MT5LC64K16D4	15, 20, 25	-	44	44	2-93
256K x 16	$\overline{CE}$, $\overline{OE}$, Byte Enable	MT5LC256K16D4	12, 15, 20, 25, 35	-	54	54	2-103

NOTE: 1. Many Micron components are available in bare die form. Contact Micron Semiconductor, Inc., for more information.

SRAM

256K x 1 SRAM

LOW VOLTAGE

FEATURES

- All I/O pins are 5V tolerant
- High speed: 12, 15, 20, 25 and 35ns
- High-performance, low-power, CMOS double-metal process
- Single +3.3V ±0.3V power supply
- Easy memory expansion with $\overline{CE}$ option
- All inputs and outputs are TTL-compatible
- Complies to JEDEC LVTTL voltage standards

OPTIONS

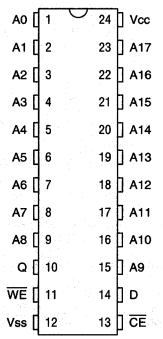
	MARKING
• Timing	
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
35ns access	-35
• Packages	
Plastic DIP (300 mil)	None
Plastic SOJ (300 mil)	DJ
• 2V data retention	L
• Low power	P
• Temperature	
Commercial (0°C to +70°C)	None
Industrial (-40°C to +85°C)	IT
Automotive (-40°C to +125°C)	AT
Extended (-55°C to +125°C)	XT

- Part Number Example: MT5LC2561DJ-20 P

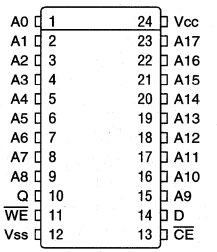
NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

24-Pin DIP
(SA-3)



24-Pin SOJ
(SD-1)



GENERAL DESCRIPTION

The MT5LC2561 is organized as a 262,144 x 1 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

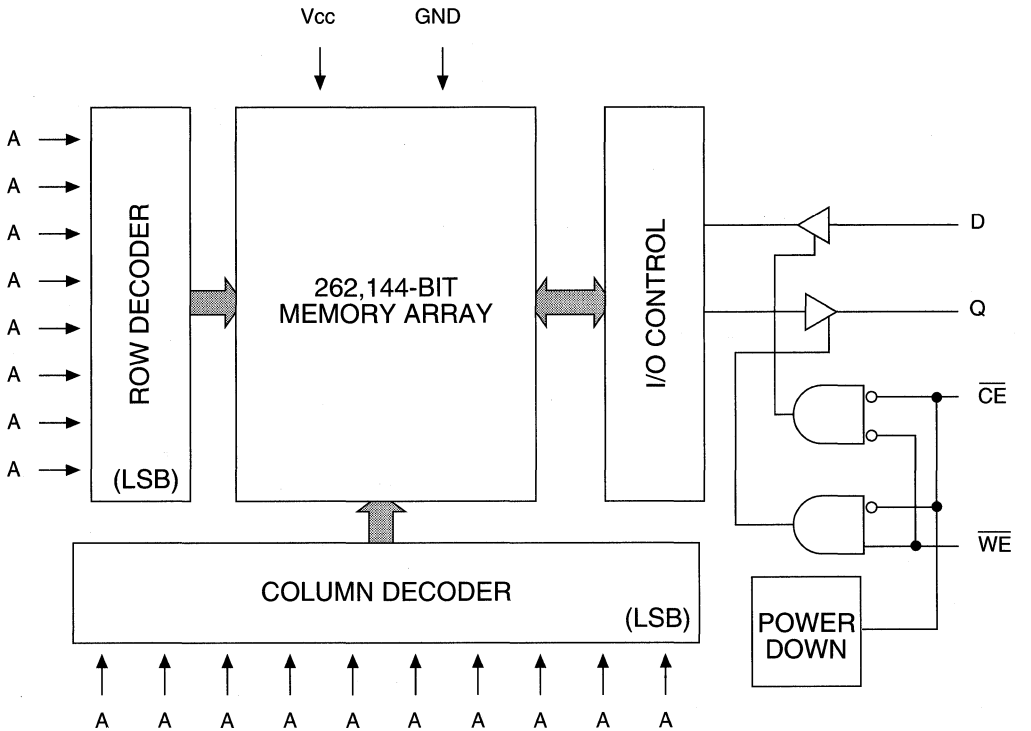
For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) with all organizations. This enhancement can place the outputs in High-Z for additional flexibility in system design. The x1 configuration features separate data input and output.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

The "P" version provides a reduction in both operating current (I_{CC}) and TTL standby current (I_{SB1}). The latter is achieved through the use of gated inputs on the $\overline{WE}$ and address lines, which also facilitates the design of battery backed-systems. That is, the gated inputs simplify the design effort and circuitry required to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

All devices operate from a single +3.3V power supply and all inputs and outputs are fully TTL-compatible and 5V tolerant. These low-voltage parts are ideal for mixed 3.3V and 5V systems.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	INPUT	OUTPUT	POWER
STANDBY	H	X	DON'T CARE	HIGH-Z	STANDBY
READ	L	H	DON'T CARE	Q	ACTIVE
WRITE	L	L	DATA-IN	HIGH-Z	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -0.5V to +4.6V
V_{IN} ..... -0.5V to +6.0V
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; V_{CC} = 3.3V ±0.3V)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.0	5.5	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-1	1	µA	
Output Leakage Current	Output(s) disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	3.0	3.6	V	1

					MAX						
DESCRIPTION	CONDITIONS	SYM	VER	TYP	-12	-15	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX outputs open f = MAX = 1/tRC	I_{CC}	STD	73	125	110	95	90	85	mA	3, 14
			P	39	–	65	55	50	50	mA	
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX outputs open f = MAX = 1/tRC	I_{SB1}	STD	17	35	30	25	25	25	mA	14
			P	8	–	18	15	12	12	mA	14
	$\overline{CE} \ge V_{CC}$ - 0.2V; V_{CC} = MAX $V_{IN} \ge V_{CC}$ - 0.2V or $V_{IN} \le V_{SS}$ + 0.2V	I_{SB2}	STD	1.0	3	3	3	3	5	mA	14
			P	300	–	750	750	750	1,500	µA	14

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	6	pF	4
Output Capacitance	V_{CC} = 3.3V	C_O	6	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) (0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ±0.3V)

DESCRIPTION		-12		-15		-20		-25		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES		
READ Cycle													
READ cycle time	^tRC	12		15		20		25		35		ns	
Address access time	^tAA		12		15		20		25		35	ns	
Chip Enable access time	^tACE		12		15		20		25		35	ns	
Output hold from address change	^tOH	3		3		3		3		3		ns	
Output hold from address change	^tOH	–	–	4		4		4		4		ns	16
Chip Enable to output in Low-Z	^tLZCE	3		3		3		3		3		ns	7
Chip Enable to output in Low-Z	^tLZCE	–	–	4		4		4		4		ns	16
Chip disable to output in High-Z	^tHZCE		6		8		9		9		15	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		0		ns	
Chip disable to power-down time	^tPD		12		15		20		25		35	ns	
WRITE Cycle													
WRITE cycle time	^tWC	12		15		20		25		35		ns	
Chip Enable to end of write	^tCW	8		10		12		15		20		ns	
Address valid to end of write	^tAW	8		10		12		15		20		ns	
Address setup time	^tAS	0		0		0		0		0		ns	
Address hold from end of write	^tAH	1		1		1		1		1		ns	
Address hold from end of write	^tAH	–	–	0		0		0		0		ns	16
WRITE pulse width	^tWP	8		10		12		15		20		ns	
Data setup time	^tDS	7		8		10		10		15		ns	
Data hold time	^tDH	0		0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	3		3		3		3		3		ns	7
Write Enable to output in High-Z	^tHZWE		6		7		8		10		12	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

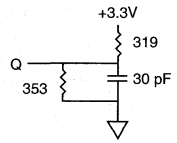


Fig. 1 OUTPUT LOAD EQUIVALENT

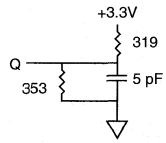


Fig. 2 OUTPUT LOAD EQUIVALENT

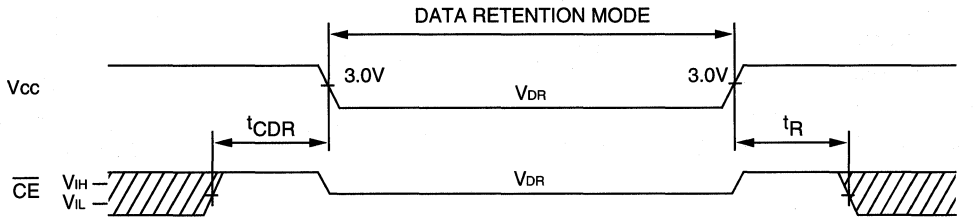
NOTES

1. All voltages referenced to V_{SS} (GND).
2. Overshoot: $V_{IH} \leq +6.0V$ for $t \leq {}^tRC/2$
   Undershoot: $V_{IL} \geq -2.0V$ for $t \leq {}^tRC/2$
   Power-up: $V_{IH} \leq +6.0V$ and $V_{CC} \leq 3.1V$ for $t \leq 200msec$.
3. I_{CC} is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ${}^tHZCE$ and ${}^tHZWE$ are specified with CL = 5pF as in Fig. 2. Transition is measured ±200mV from steady state voltage.
7. At any given temperature and voltage condition, ${}^tHZCE$ is less than ${}^tLZCE$ and ${}^tHZWE$ is less than ${}^tLZWE$.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ${}^tRC$ = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Contact Micron for IT/AT/XT timing and current specifications; they may differ from the commercial temperature range specifications shown in this data sheet.
14. Typical values are measured at 3.3V, 25°C and 15ns cycle time for STD and 20ns for P.
15. Typical currents are measured at 25°C.
16. These timing specifications are only valid for P (low power) parts.

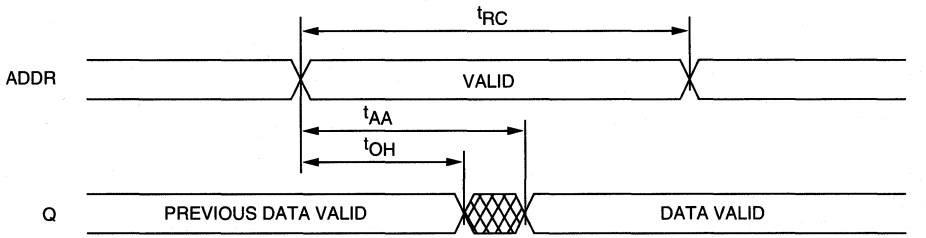
DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP versions only)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V_{CC} for Retention Data		V_{DR}	2			V	
Data Retention Current L version	$\overline{CE} \geq V_{CC}$ -0.2V Other Inputs: $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq V_{SS}$+0.2V V_{CC} = 2V	I_{CCDR}		310	500	µA	15
Data Retention Current LP version	$\overline{CE} \geq V_{CC}$ -0.2V V_{CC} = 2V	I_{CCDR}		195	350	µA	15
Chip Deselect to Data Retention Time		${}^tCDR$	0			ns	4
Operation Recovery Time		${}^tR$	${}^tRC$			ns	4, 11

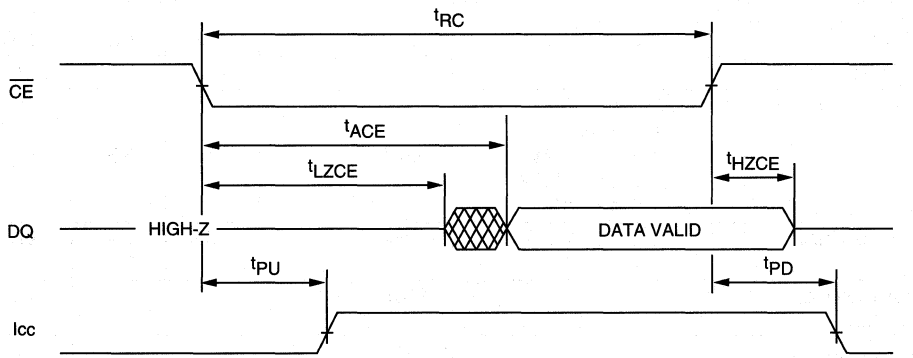
LOW Vcc DATA RETENTION WAVEFORM

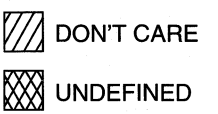


READ CYCLE NO. 1 [8, 9]

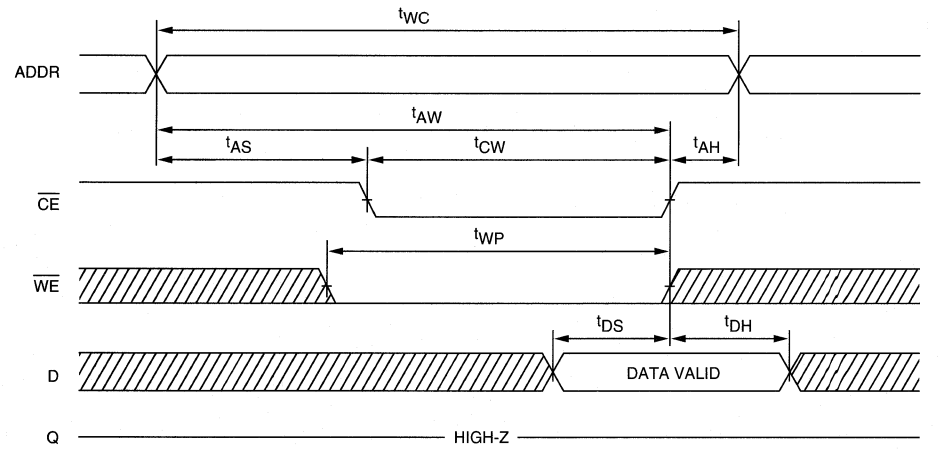


READ CYCLE NO. 2 [7, 8, 10]

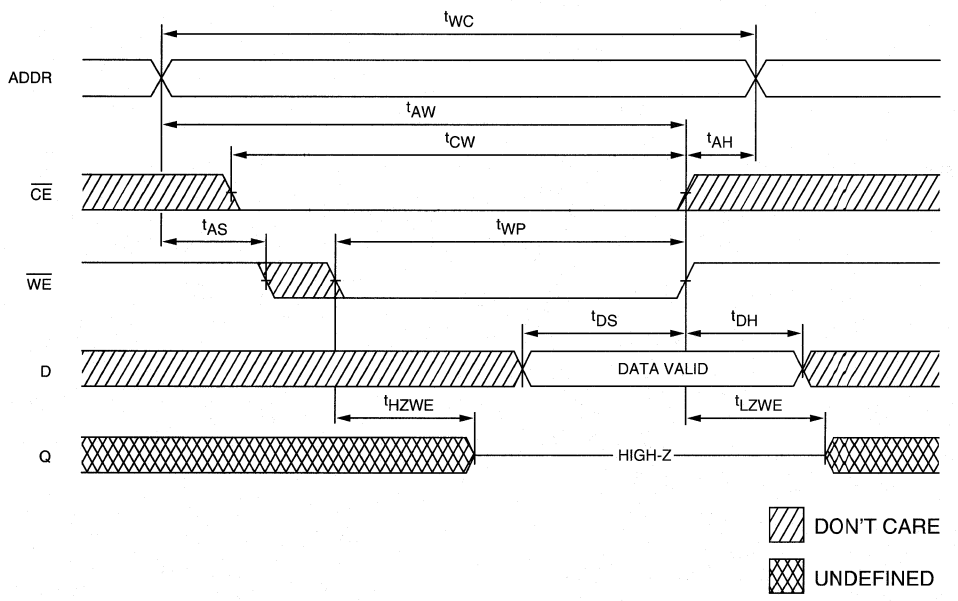




WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)



WRITE CYCLE NO. 2 [7, 12]
(Write Enable Controlled)



SRAM

1 MEG x 1 SRAM

LOW VOLTAGE

FEATURES

- All I/O pins are 5V tolerant
- High speed: 15, 17, 20, 25, 35 and 45ns
- High-performance, low-power, CMOS double-metal process
- Single +3.3V ±0.3 power supply
- Easy memory expansion with $\overline{CE}$ option
- All inputs and outputs are TTL-compatible
- Complies to JEDEC low-voltage TTL standards

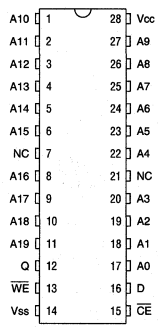
OPTIONS — MARKING

- Timing
  - 15ns access — -15
  - 17ns access — -17
  - 20ns access — -20
  - 25ns access — -25
  - 35ns access — -35
  - 45ns access — -45
- Packages
  - Plastic DIP (400 mil) — None
  - Plastic SOJ (400 mil) — DJ
  - Plastic SOJ (300 mil) — SJ
- 2V data retention — L
- 2V data retention, low power — LP
- Temperature
  - Commercial (0°C to +70°C) — None
  - Industrial (-40°C to +85°C) — IT
  - Automotive (-40°C to +125°C) — AT
  - Extended (-55°C to +125°C) — XT
- Part Number Example: MT5LC1001DJ-25 L

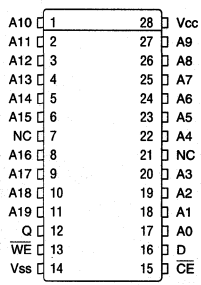
NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

28-Pin DIP (SA-5)



28-Pin SOJ (SD-3) (SD-2)



GENERAL DESCRIPTION

The MT5LC1001 is organized as a 1,048,576 x 1 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

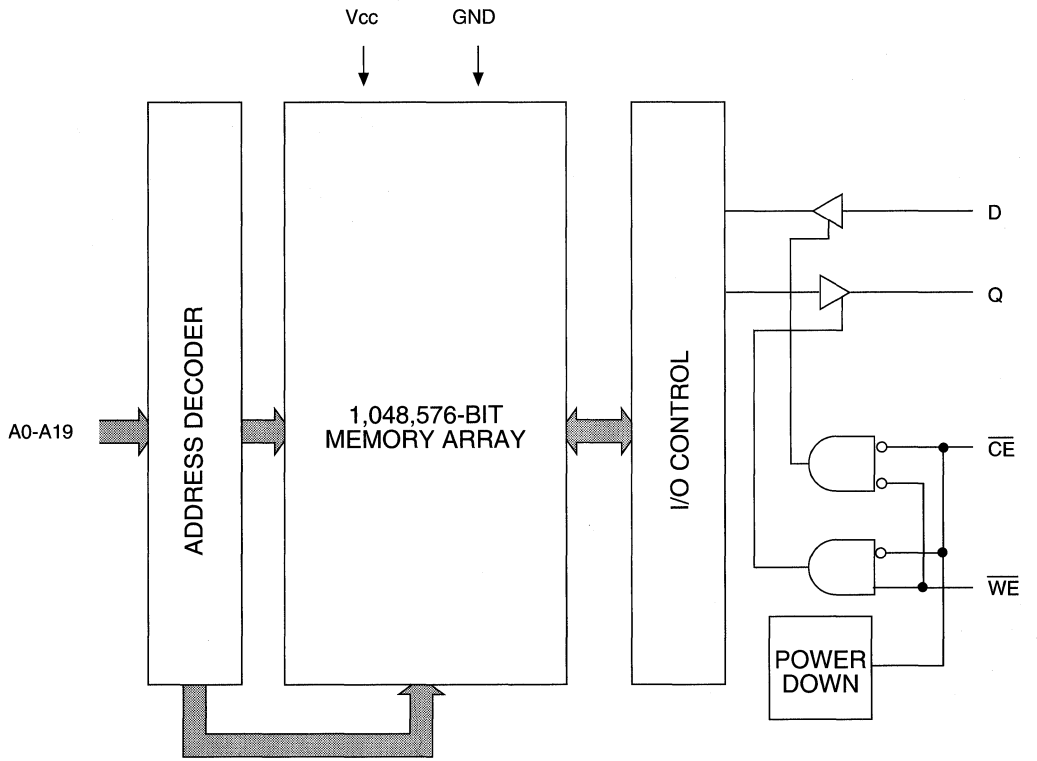
For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) capability. This enhancement can place the outputs in High-Z for additional flexibility in system design.

Writing to this device is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH while $\overline{CE}$ goes LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

The "LP" version provides a reduction in both CMOS standby current (I_{SB2}) and TTL standby current (I_{SB1}) over the standard part. This is achieved through the use of gated inputs on the $\overline{WE}$ and address lines, which also facilitates the design of battery-backed systems. That is, the gated inputs simplify the design effort and circuitry required to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

All devices operate from a single +3.3V power supply and all inputs and outputs are fully TTL-compatible and 5V tolerant. These low-voltage parts are ideal for mixed 3.3V and 5V systems.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	INPUT	OUTPUT	POWER
STANDBY	H	X	DON'T CARE	HIGH-Z	STANDBY
READ	L	H	DON'T CARE	Q	ACTIVE
WRITE	L	L	DATA-IN	HIGH-Z	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -0.5V to +4.6V
V_{IN} ..... -0.5V to +6.0V
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ±0.3V)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.0	5.5	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ Vcc	I_{LI}	-1	1	µA	
Output Leakage Current	Output(s) disabled 0V ≤ V_{OUT} ≤ Vcc	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		Vcc	3.0	3.6	V	1

				MAX							
DESCRIPTION	CONDITIONS	SYMBOL	VER	-15	-17	-20	-25	-35	-45	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; Vcc = MAX outputs open f = MAX = 1/tRC	Icc	ALL	85	75	65	55	45	40	mA	3, 15
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; Vcc = MAX outputs open f = MAX = 1/tRC	I_{SB1}	STD, L	20	18	14	12	8	6	mA	
			LP	500	500	500	500	500	500	µA	
	$\overline{CE}$ ≥ Vcc - 0.2V; Vcc = MAX V_{IN} ≥ Vcc - 0.2V or V_{IN} ≤ V_{SS} + 0.2V	I_{SB2}	STD, L	300	300	300	300	300	300	µA	
			LP	100	100	100	100	100	100	µA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz Vcc = 3.3V	C_I	8	pF	4
Output Capacitance		Co	8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) (0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ±0.3V)

DESCRIPTION		-15		-17		-20		-25		-35		-45			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle															
READ cycle time	^tRC	15		17		20		25		35		45		ns	
Address access time	^tAA		15		17		20		25		35		45	ns	
Chip Enable access time	^tACE		15		17		20		25		35		45	ns	
Output hold from address change	^tOH	3		3		3		5		5		5		ns	
Chip Enable to output in Low-Z	^tLZCE	5		5		3		5		5		5		ns	7
Chip disable to output in High-Z	^tHZCE		6		7		8		10		15		18	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		0		0		ns	
Chip disable to power-down time	^tPD		15		17		20		25		35		45	ns	
WRITE Cycle															
WRITE cycle time	^tWC	15		17		20		25		35		45		ns	
Chip Enable to end of write	^tCW	10		12		12		15		20		25		ns	
Address valid to end of write	^tAW	10		12		12		15		20		25		ns	
Address setup time	^tAS	0		0		0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		0		0		ns	
WRITE pulse width	^tWP	9		12		12		15		20		25		ns	
Data setup time	^tDS	7		8		8		10		15		20		ns	
Data hold time	^tDH	0		0		0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	3		3		3		5		5		5		ns	7
Write Enable to output in High-Z	^tHZWE		6		7		8		10		15		18	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

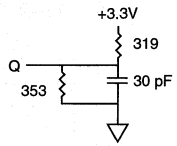


Fig. 1 OUTPUT LOAD EQUIVALENT

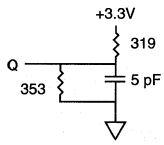


Fig. 2 OUTPUT LOAD EQUIVALENT

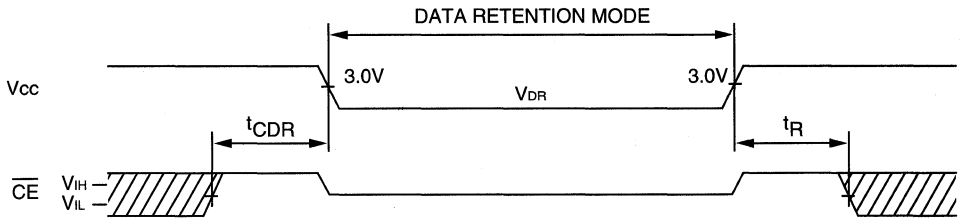
NOTES

1. All voltages referenced to V_{SS} (GND).
2. Overshoot: $V_{IH} \leq +6.0V$ for $t \leq {}^tRC/2$
   Undershoot: $V_{IL} \geq -2.0V$ for $t \leq {}^tRC/2$
   Power-up: $V_{IH} \leq +6.0V$ and $V_{CC} \leq 3.1V$ for $t \leq 200msec$.
3. I_{CC} is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ${}^tHZCE$ and ${}^tHZWE$ are specified with CL = 5pF as in Fig. 2. Transition is measured ±200mV from steady state voltage.
7. At any given temperature and voltage condition, ${}^tHZCE$ is less than ${}^tLZCE$, and ${}^tHZWE$ is less than ${}^tLZWE$.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables and output enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ${}^tRC$ = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Contact Micron for IT/AT/XT timing and current specifications; they may differ from the commercial temperature range specifications shown in this data sheet.
14. Typical values are measured at 3.3V, 25°C and 25ns cycle time.
15. Typical currents are measured at 25°C.

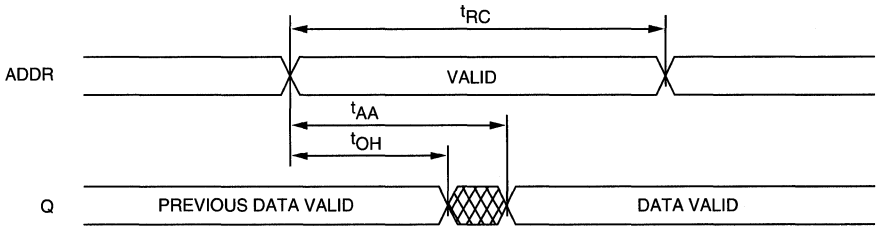
DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP versions only)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V_{CC} for Retention Data		V_{DR}	2			V	
Data Retention Current L version	$\overline{CE} \geq V_{CC}$ -0.2V Other inputs: $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq V_{SS}$+0.2V V_{CC} = 2V		I_{CCDR}	TBD	50	µA	15
Data Retention Current LP version	$\overline{CE} \geq V_{CC}$ -0.2V V_{CC} = 2V		I_{CCDR}	TBD	50	µA	15
Chip Deselect to Data Retention Time		${}^tCDR$	0			ns	4
Operation Recovery Time		${}^tR$	${}^tRC$			ns	4, 11

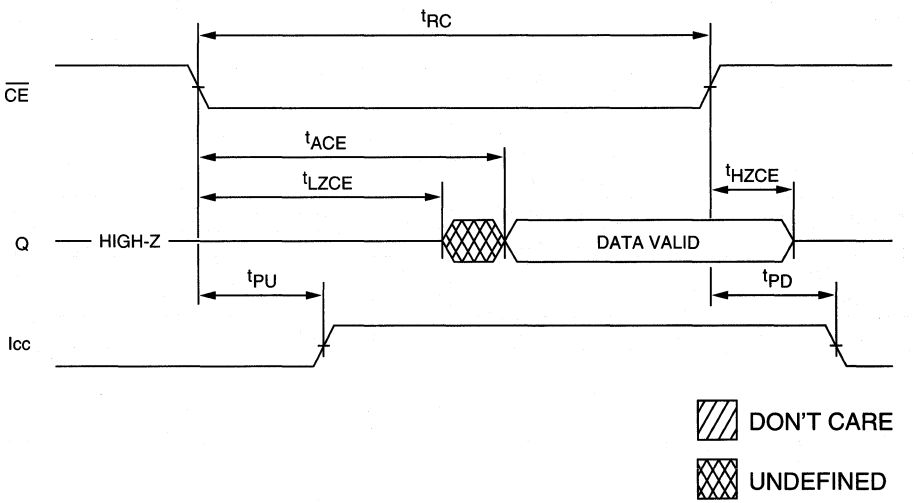
LOW Vcc DATA RETENTION WAVEFORM



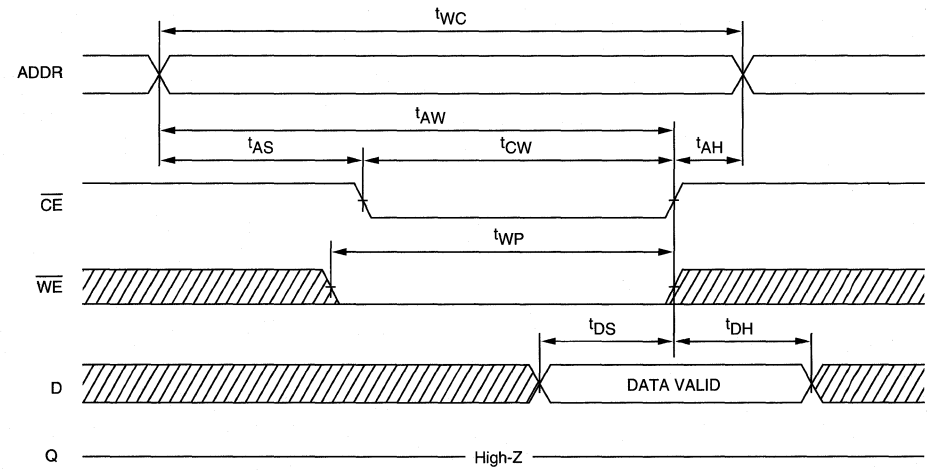
READ CYCLE NO. 1 [8, 9]



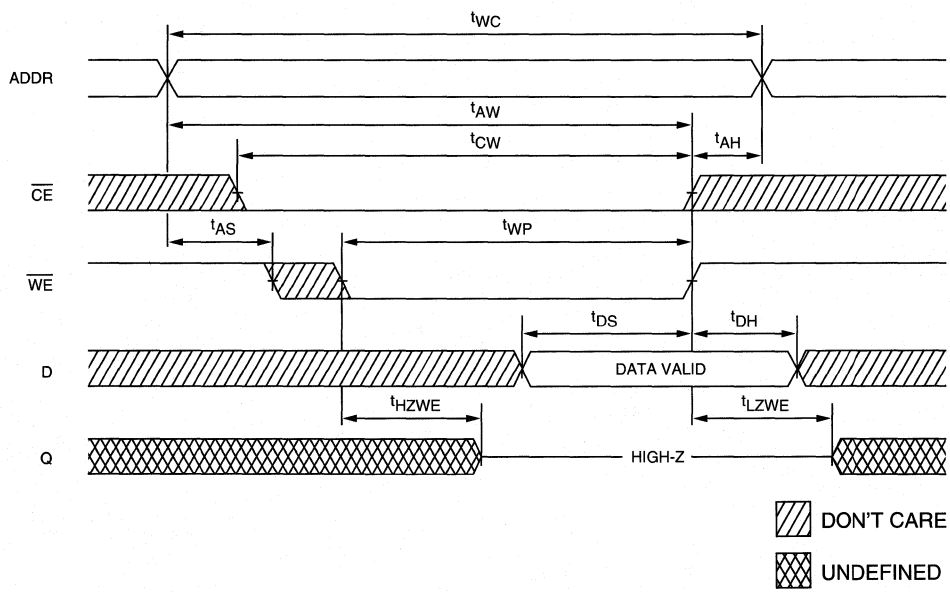
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)



WRITE CYCLE NO. 2 [7, 12]
(Write Enable Controlled)



SRAM

64K x 4 SRAM

LOW VOLTAGE

FEATURES

- All I/O pins are 5V tolerant
- High speed: 12, 15, 20, 25 and 35ns
- High-performance, low-power, CMOS double-metal process
- Single +3.3V ±0.3V power supply
- Easy memory expansion with $\overline{CE}$ option
- All inputs and outputs are TTL-compatible
- Complies to JEDEC low-voltage TTL standards

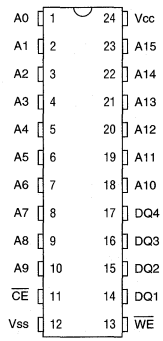
OPTIONS — MARKING

- Timing
  - 12ns access — -12
  - 15ns access — -15
  - 20ns access — -20
  - 25ns access — -25
  - 35ns access — -35
- Packages
  - Plastic DIP (300 mil) — None
  - Plastic SOJ (300 mil) — DJ
- 2V data retention — L
- Low power — P
- Temperature
  - Commercial (0°C to +70°C) — None
  - Industrial (-40°C to +85°C) — IT
  - Automotive (-40°C to +125°C) — AT
  - Extended (-55°C to +125°C) — XT
- Part Number Example: MT5LC2564DJ-25 P

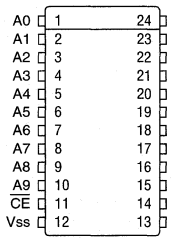
NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

24-Pin DIP (SA-3)



24-Pin SOJ (SD-1)



GENERAL DESCRIPTION

The MT5LC2564 is organized as a 65,536 x 4 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

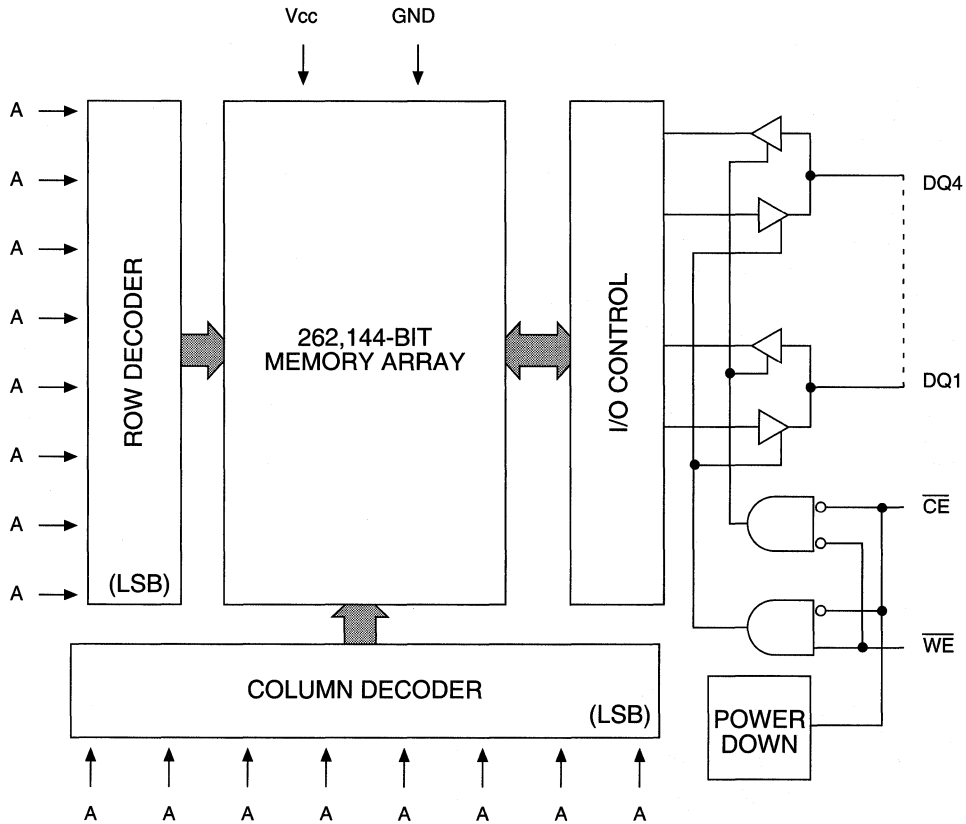
For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) with all organizations. This enhancement can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

The "P" version provides a reduction in both operating current (I_{CC}) and TTL standby current (I_{SB1}). The latter is achieved through the use of gated inputs on the $\overline{WE}$ and address lines, which also facilitates the design of battery-backed systems. That is, the gated inputs simplify the design effort and circuitry required to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

All devices operate from a single +3.3V power supply and all inputs and outputs are fully TTL-compatible and 5V tolerant. These low-voltage parts are ideal for mixed 3.3V and 5V systems.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	H	X	HIGH-Z	STANDBY
READ	L	H	Q	ACTIVE
WRITE	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -0.5V to +4.6V
V_{IN} ..... -0.5V to +6.0V
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; $V_{CC} = 3.3V \pm 0.3V$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.0	5.5	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-1	1	µA	
Output Leakage Current	Output(s) disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	3.0	3.6	V	1

					MAX						
DESCRIPTION	CONDITIONS	SYM	VER	TYP	-12	-15	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX outputs open f = MAX = 1/tRC	I_{CC}	STD	73	125	110	95	90	85	mA	3, 14
			P	39	–	65	55	50	50	mA	
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX outputs open f = MAX = 1/tRC	I_{SB1}	STD	17	35	30	25	25	25	mA	14
			P	8	–	18	15	12	12	mA	14
	$\overline{CE} \ge V_{CC}$ - 0.2V; V_{CC} = MAX $V_{IN} \ge V_{CC}$ - 0.2V or $V_{IN} \le V_{SS}$ + 0.2V	I_{SB2}	STD	1.0	3	3	3	3	5	mA	14
			P	300	–	750	750	750	1,500	µA	14

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	6	pF	4
Output Capacitance	V_{CC} = 3.3V	C_O	6	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) (0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ±0.3V)

DESCRIPTION		-12		-15		-20		-25		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle													
READ cycle time	^tRC	12		15		20		25		35		ns	
Address access time	^tAA		12		15		20		25		35	ns	
Chip Enable access time	^tACE		12		15		20		25		35	ns	
Output hold from address change	^tOH	3		3		3		3		3		ns	
Output hold from address change	^tOH	–	–	4		4		4		4		ns	16
Chip Enable to output in Low-Z	^tLZCE	4		3		3		3		3		ns	7
Chip Enable to output in Low-Z	^tLZCE	–	–	4		4		4		4		ns	16
Chip disable to output in High-Z	^tHZCE		6		8		9		9		15	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		0		ns	
Chip disable to power-down time	^tPD		12		15		20		25		35	ns	
WRITE Cycle													
WRITE cycle time	^tWC	12		15		20		25		35		ns	
Chip Enable to end of write	^tCW	8		10		12		15		20		ns	
Address valid to end of write	^tAW	8		10		12		15		20		ns	
Address setup time	^tAS	0		0		0		0		0		ns	
Address hold from end of write	^tAH	1		1		1		1		1		ns	
Address hold from end of write	^tAH	–	–	0		0		0		0		ns	16
WRITE pulse width	$^tWP1$	8		10		12		15		20		ns	
WRITE pulse width	$^tWP2$	12		12		15		15		20		ns	
Data setup time	^tDS	7		8		10		10		15		ns	
Data hold time	^tDH	0		0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	3		3		3		3		3		ns	7
Write Enable to output in High-Z	^tHZWE		6		7		8		10		12	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

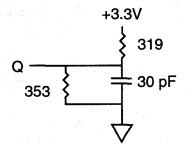


Fig. 1 OUTPUT LOAD EQUIVALENT

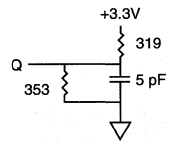


Fig. 2 OUTPUT LOAD EQUIVALENT

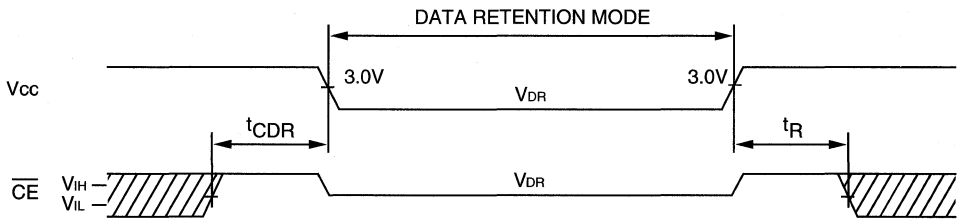
NOTES

1. All voltages referenced to Vss (GND).
2. Overshoot: $V_{IH} \leq +6.0V$ for $t \leq {}^tRC/2$
   Undershoot: $V_{IL} \geq -2.0V$ for $t \leq {}^tRC/2$
   Power-up: $V_{IH} \leq +6.0V$ and $V_{CC} \leq 3.1V$ for $t \leq 200msec$.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ${}^tHZCE$ and ${}^tHZWE$ are specified with CL = 5pF as in Fig. 2. Transition is measured ± 200mV from steady state voltage.
7. At any given temperature and voltage condition, ${}^tHZCE$ is less than ${}^tLZCE$ and ${}^tHZWE$ is less than ${}^tLZWE$.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ${}^tRC$ = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Contact Micron for IT/AT/XT timing and current specifications; they may differ from the commercial temperature range specifications shown in this data sheet.
14. Typical values are measured at 3.3V, 25°C and 20ns cycle time for P, 15ns for STD.
15. Typical currents are measured at 25°C.
16. This timing specification is valid only for P (low power) parts.

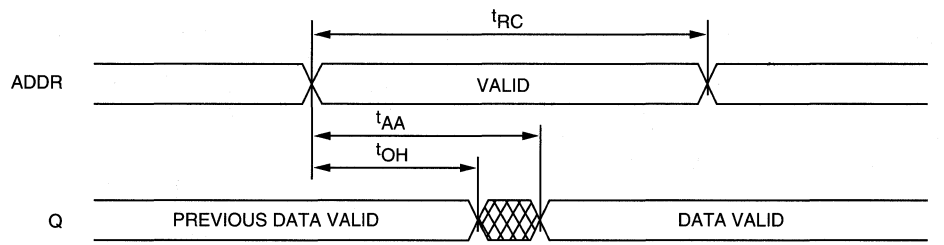
DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP versions only)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data		V_{DR}	2			V	
Data Retention Current L version	$\overline{CE} \geq$ Vcc -0.2V Other inputs: $V_{IN} \geq$ Vcc -0.2V or $V_{IN} \leq$ Vss+0.2V Vcc = 2V	I_{CCDR}		310	500	µA	15
Data Retention Current LP version	$\overline{CE} \geq$ Vcc -0.2V Vcc = 2V	I_{CCDR}		195	350	µA	15
Chip Deselect to Data Retention Time		${}^tCDR$	0			ns	4
Operation Recovery Time		${}^tR$	${}^tRC$			ns	4, 11

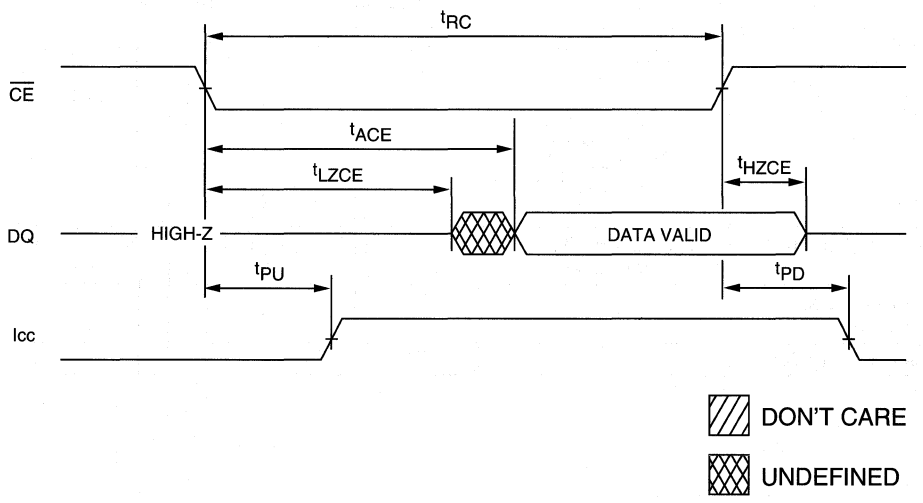
LOW Vcc DATA RETENTION WAVEFORM



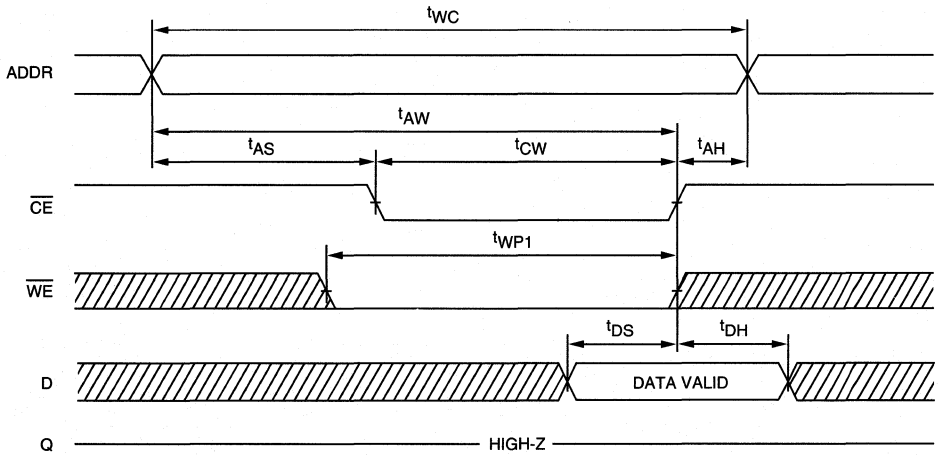
READ CYCLE NO. 1 [8, 9]



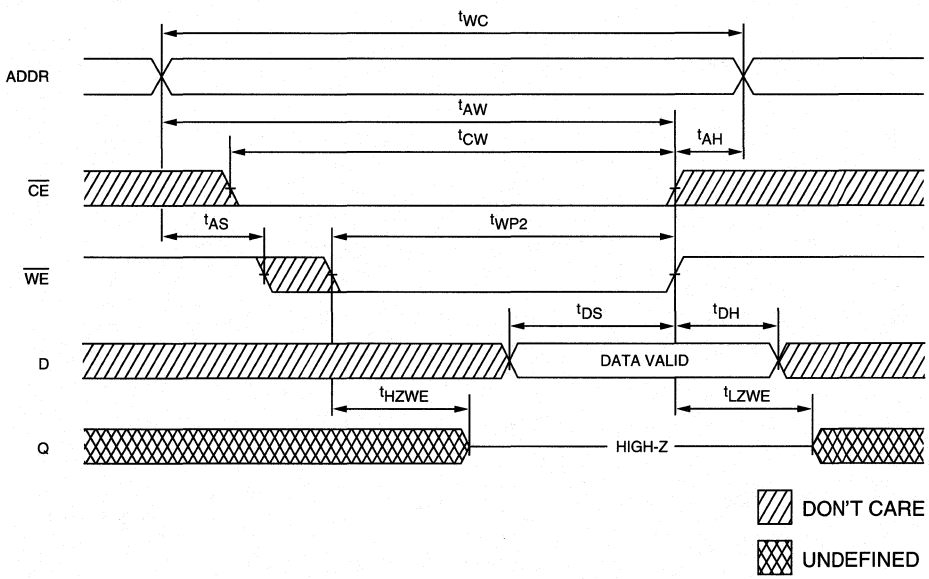
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)



WRITE CYCLE NO. 2 [7, 12]
(Write Enable Controlled)



SRAM

64K x 4 SRAM

LOW VOLTAGE WITH OUTPUT ENABLE

FEATURES

- All I/O pins are 5V tolerant
- High speed: 12, 15, 20, 25 and 35ns
- High-performance, low-power, CMOS double-metal process
- Single +3.3V ±0.3V power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- All inputs and outputs are TTL-compatible
- Complies to JEDEC low-voltage TTL standards

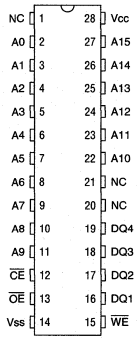
OPTIONS — MARKING

- Timing
  - 12ns access — -12
  - 15ns access — -15
  - 20ns access — -20
  - 25ns access — -25
  - 35ns access — -35
- Packages
  - Plastic DIP (300 mil) — None
  - Plastic SOJ (300 mil) — DJ
- 2V data retention — L
- Low power — P
- Temperature
  - Commercial (0°C to +70°C) — None
  - Industrial (-40°C to +85°C) — IT
  - Automotive (-40°C to +125°C) — AT
  - Extended (-55°C to +125°C) — XT
- Part Number Example: MT5LC2565DJ-25 L

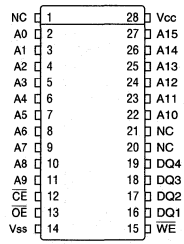
NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

28-Pin DIP (SA-4)



28-Pin SOJ (SD-2)



GENERAL DESCRIPTION

The MT5LC2565 is organized as a 65,536 x 4 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

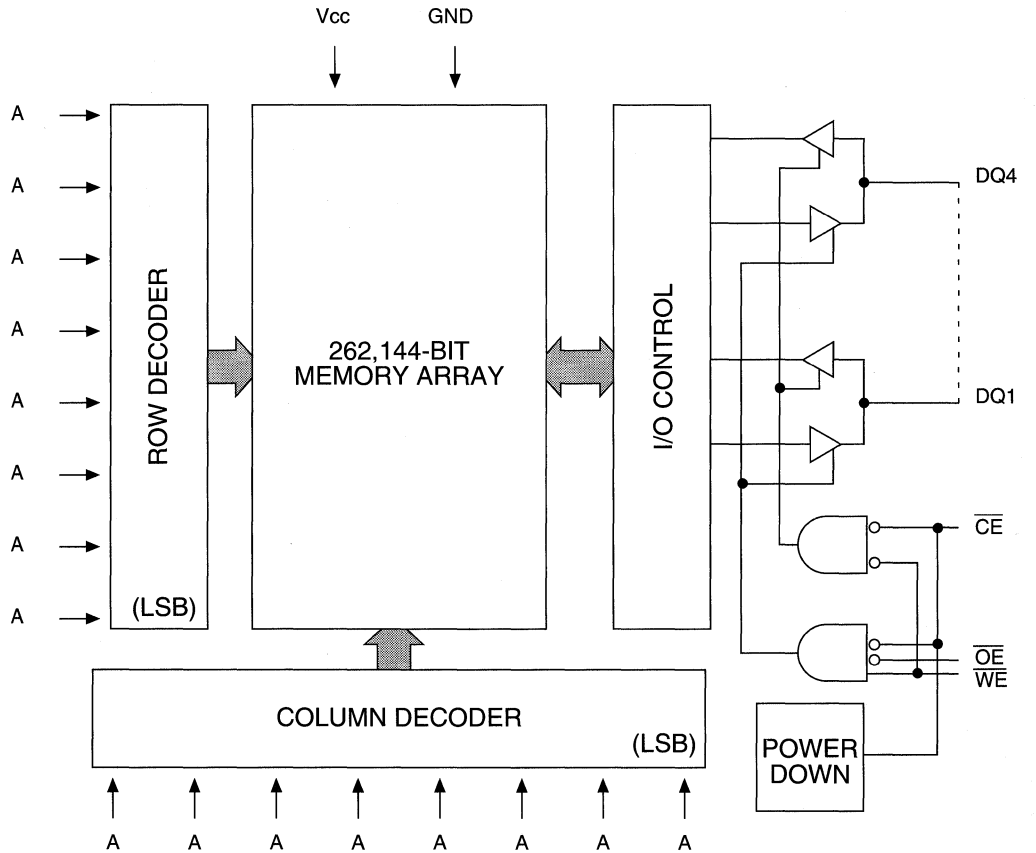
For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) with this organization. These enhancements can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ and $\overline{OE}$ go LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

The "P" version provides a reduction in both operating current (I_{CC}) and TTL standby current (I_{SB1}). The latter is achieved through the use of gated inputs on the $\overline{WE}$, $\overline{OE}$ and address lines, which also facilitates the design of battery-backed systems. That is, the gated inputs simplify the design effort and circuitry required to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

All devices operate from a single +3.3V power supply and all inputs and outputs are fully TTL-compatible and 5V tolerant. These low-voltage parts are ideal for mixed 3.3V and 5V systems.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -0.5V to +4.6V
V_{IN} ..... -0.5V to +6.0V
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ±0.3V)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.0	5.5	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-1	1	µA	
Output Leakage Current	Output(s) disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	3.0	3.6	V	1

					MAX						
DESCRIPTION	CONDITIONS	SYM	VER	TYP	-12	-15	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX outputs open f = MAX = 1/^tRC	I_{CC}	STD	73	125	110	95	90	85	mA	3, 14
			P	39	–	65	55	50	50	mA	
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX outputs open f = MAX = 1/^tRC	I_{SB1}	STD	17	35	30	25	25	25	mA	14
			P	8	–	18	15	12	12	mA	14
	$\overline{CE}$ ≥ V_{CC} - 0.2V; V_{CC} = MAX V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ V_{SS} + 0.2V	I_{SB2}	STD	1.0	3	3	3	3	5	mA	14
			P	300	–	750	750	750	1,500	µA	14

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	6	pF	4
Output Capacitance	V_{CC} = 3.3V	C_O	6	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) (0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ±0.3V)

DESCRIPTION		-12		-15		-20		-25		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle													
READ cycle time	^tRC	12		15		20		25		35		ns	
Address access time	^tAA		12		15		20		25		35	ns	
Chip Enable access time	^tACE		12		15		20		25		35	ns	
Output hold from address change	^tOH	3		3		3		3		3		ns	
Output hold from address change	^tOH	–		4		4		4		4		ns	16
Chip Enable to output in Low-Z	^tLZCE	3		3		3		3		3		ns	7
Chip Enable to output in Low-Z	^tLZCE	–		4		4		4		4		ns	16
Chip disable to output in High-Z	^tHZCE		6		8		9		9		15	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		0		ns	
Chip disable to power-down time	^tPD		12		15		20		25		35	ns	
Output Enable access time	^tAOE		6		7		8		8		12	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		0		ns	
Output disable to output in High-Z	^tHZOE		6		6		7		7		10	ns	6
WRITE Cycle													
WRITE cycle time	^tWC	12		15		20		25		35		ns	
Chip Enable to end of write	^tCW	8		10		12		15		20		ns	
Address valid to end of write	^tAW	8		10		12		15		20		ns	
Address setup time	^tAS	0		0		0		0		0		ns	
Address hold from end of write	^tAH	1		1		1		1		1		ns	
Address hold from end of write	^tAH	–		0		0		0		0		ns	16
WRITE pulse width	$^tWP1$	8		10		12		15		20		ns	
WRITE pulse width	$^tWP2$	12		12		15		15		20		ns	
Data setup time	^tDS	7		8		10		10		15		ns	
Data hold time	^tDH	0		0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	3		3		3		3		3		ns	7
Write Enable to output in High-Z	^tHZWE		6		7		8		10		12	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

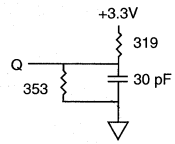


Fig. 1 OUTPUT LOAD EQUIVALENT

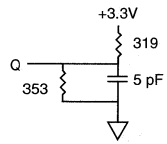


Fig. 2 OUTPUT LOAD EQUIVALENT

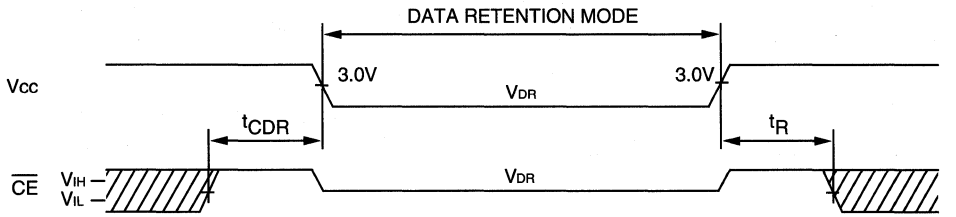
NOTES

1. All voltages referenced to Vss (GND).
2. Overshoot: $V_{IH} \leq +6.0V$ for $t \leq {}^tRC/2$
   Undershoot: $V_{IL} \geq -2.0V$ for $t \leq {}^tRC/2$
   Power-up: $V_{IH} \leq +6.0V$ and $V_{CC} \leq 3.1V$ for $t \leq 200msec$.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ${}^tHZCE$, ${}^tHZOE$ and ${}^tHZWE$ are specified with CL = 5pF as in Fig. 2. Transition is measured ±200mV from steady state voltage.
7. At any given temperature and voltage condition, ${}^tHZCE$ is less than ${}^tLZCE$ and ${}^tHZWE$ is less than ${}^tLZWE$.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ${}^tRC$ = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Contact Micron for IT/AT/XT timing and current specifications; they may differ from the commercial temperature range specifications shown in this data sheet.
14. Typical values are measured at 3.3V, 25°C and 20ns cycle time for P, 15ns for STD.
15. Typical currents are measured at 25°C.
16. This timing specification is only valid for P (low power) parts.

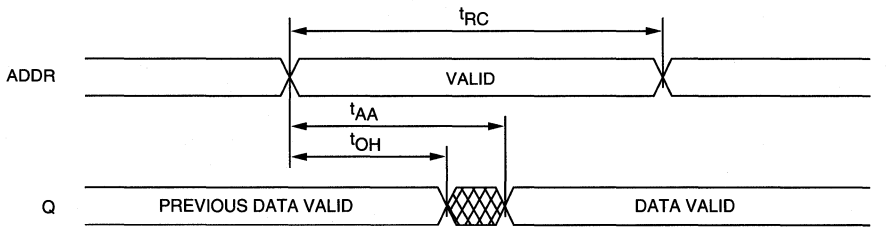
DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP versions only)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data		V_{DR}	2			V	
Data Retention Current L version	$\overline{CE} \geq$ Vcc -0.2V Other inputs: $V_{IN} \geq$ Vcc -0.2V or $V_{IN} \leq$ Vss+0.2V Vcc = 2V	I_{CCDR}		310	500	µA	15
Data Retention Current LP version	$\overline{CE} \geq$ Vcc -0.2V Vcc = 2V	I_{CCDR}		195	350	µA	15
Chip Deselect to Data Retention Time		${}^tCDR$	0			ns	4
Operation Recovery Time		${}^tR$	${}^tRC$			ns	4, 11

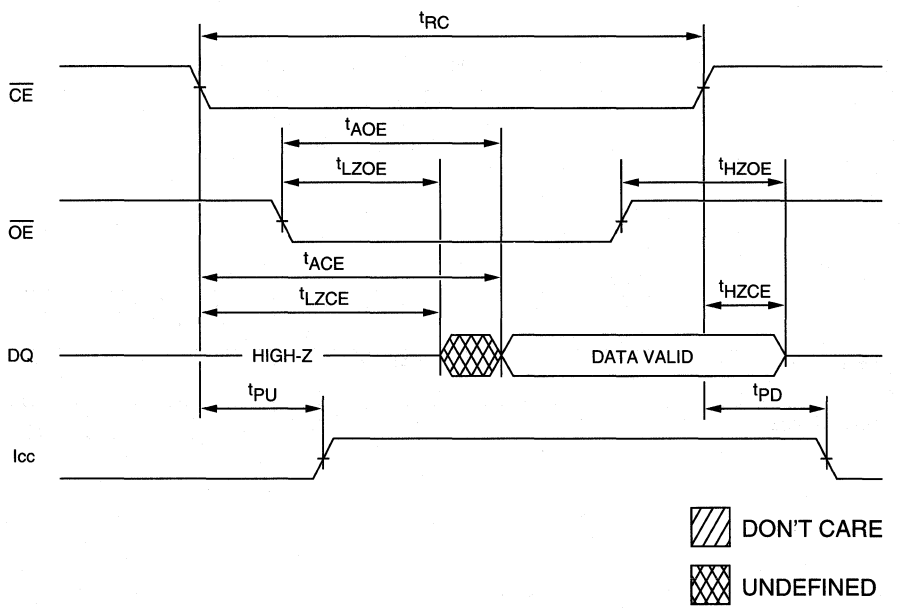
LOW Vcc DATA RETENTION WAVEFORM



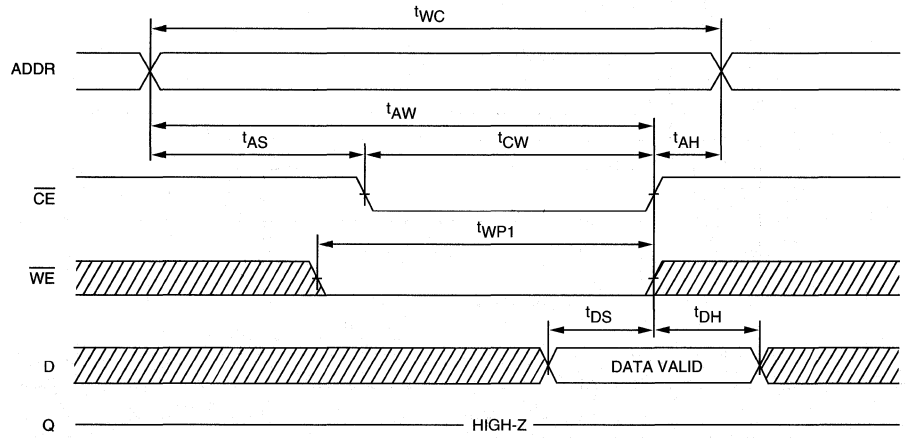
READ CYCLE NO. 1 [8, 9]



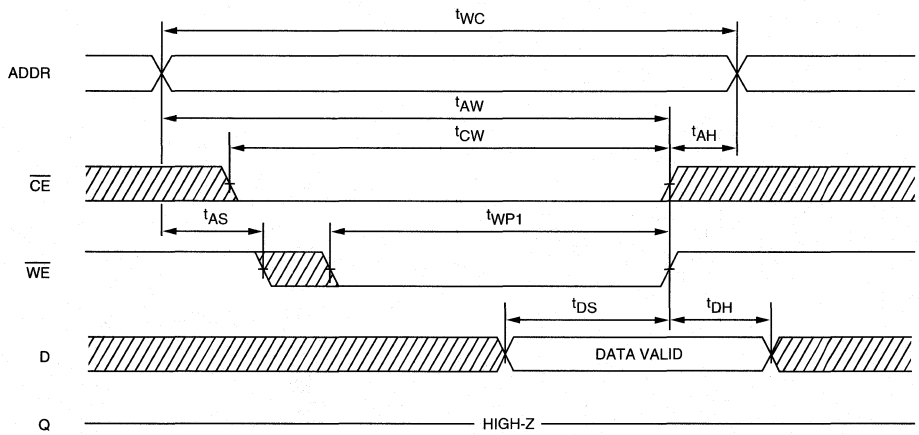
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)

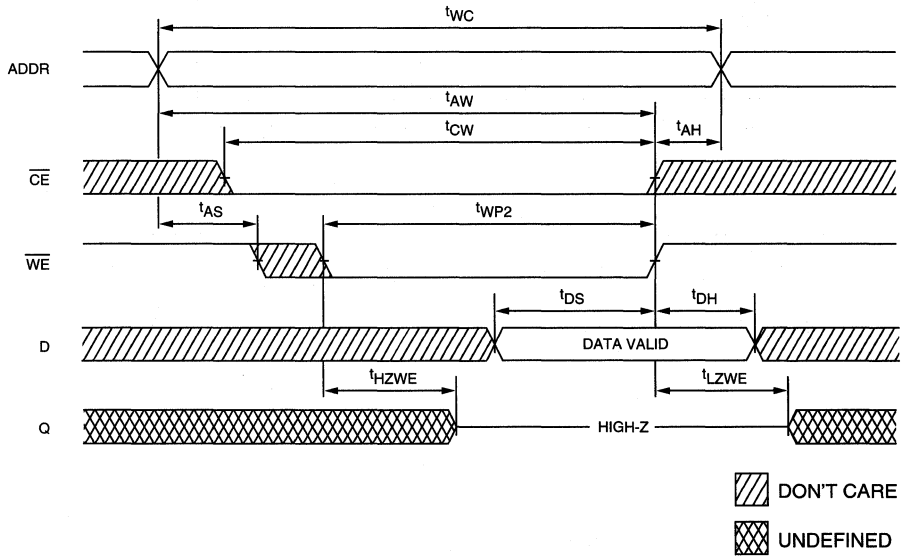


WRITE CYCLE NO. 2 [7, 12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

WRITE CYCLE NO. 3 [7, 12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is active (LOW).

SRAM

256K x 4 SRAM

LOW VOLTAGE WITH OUTPUT ENABLE

FEATURES

- All I/O pins are 5V tolerant
- High speed: 15, 17, 20, 25, 35 and 45ns
- High-performance, low-power, CMOS double-metal process
- Single +3.3V ±0.3V power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- All inputs and outputs are TTL-compatible
- Fast $\overline{OE}$ access time: 8ns
- Complies to JEDEC low-voltage TTL standards

OPTIONS — MARKING

- Timing

15ns access	-15
17ns access	-17
20ns access	-20
25ns access	-25
35ns access	-35
45ns access	-45

- Packages

Plastic DIP (400 mil)	None
Plastic SOJ (400 mil)	DJ
Plastic SOJ (300 mil)	SJ

- 2V data retention — L
- 2V data retention, low power — LP
- Temperature

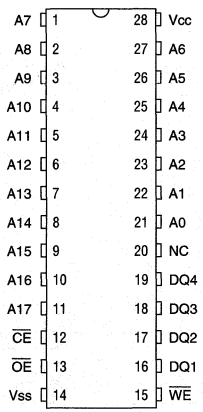
Commercial	(0°C to +70°C)	None
Industrial	(-40°C to +85°C)	IT
Automotive	(-40°C to +125°C)	AT
Extended	(-55°C to +125°C)	XT

- Part Number Example: MT5LC1005DJ-35 LP

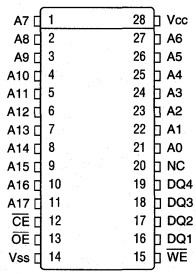
NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

28-Pin DIP (SA-5)



28-Pin SOJ (SD-3) (SD-2)



GENERAL DESCRIPTION

The MT5LC1005 is organized as a 262,144 x 4 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

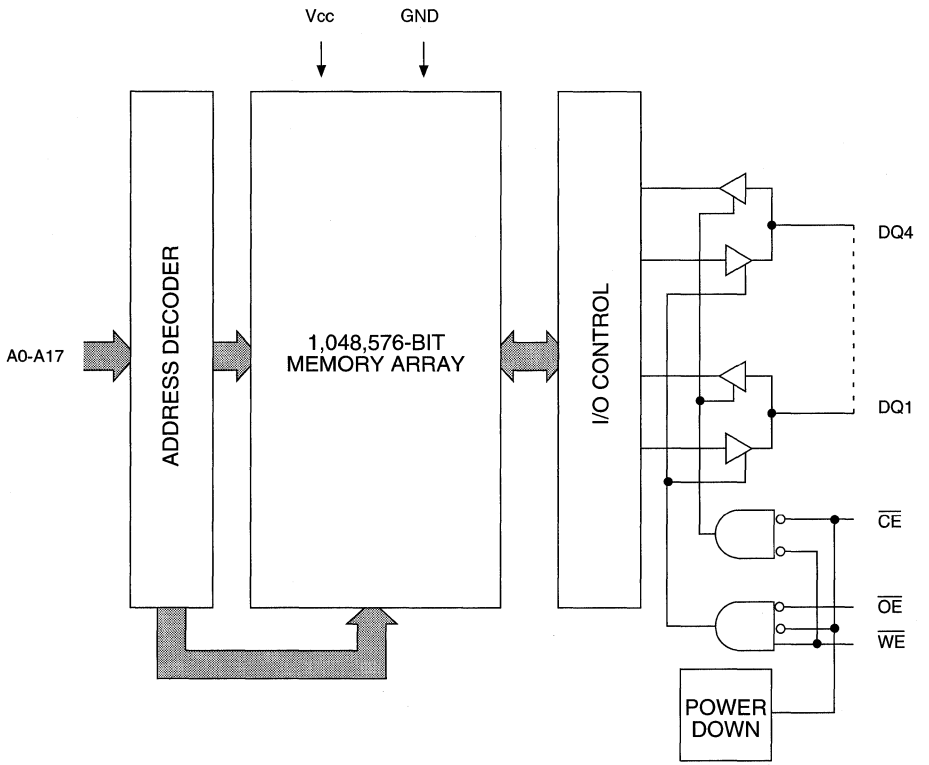
For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) capability. This enhancement can place the outputs in High-Z for additional flexibility in system design.

Writing to this device is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH while output enable ($\overline{OE}$) and $\overline{CE}$ are LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

The "LP" version provides a reduction in both CMOS standby current (I_{SB2}) and TTL standby current (I_{SB1}) over the standard part. This is achieved through the use of gated inputs on the $\overline{WE}$, $\overline{OE}$ and address lines, which also facilitates the design of battery-backed systems. That is, the gated inputs simplify the design effort and circuitry required to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

All devices operate from a single +3.3V power supply and all inputs and outputs are fully TTL-compatible and 5V tolerant. These low-voltage parts are ideal for mixed 3.3V and 5V systems.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -0.5V to +4.6V
V_{IN} ..... -0.5V to +6.0V
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ±0.3V)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.0	5.5	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-1	1	µA	
Output Leakage Current	Output(s) disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	3.0	3.6	V	1

				MAX							
DESCRIPTION	CONDITIONS	SYMBOL	VER	-15	-17	-20	-25	-35	-45	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX outputs open f = MAX = 1/t_{RC}	I_{CC}	ALL	85	75	65	55	45	40	mA	3, 15
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX outputs open f = MAX = 1/t_{RC}	I_{SB1}	STD, L	20	18	14	12	8	6	mA	
			LP	500	500	500	500	500	500	µA	
	$\overline{CE}$ ≥ V_{CC} - 0.2V; V_{CC} = MAX V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ V_{SS} + 0.2V	I_{SB2}	STD, L	300	300	300	300	300	300	µA	
			LP	100	100	100	100	100	100	µA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	8	pF	4
Output Capacitance	V_{CC} = 3.3V	C_O	8	pF	4

3.3 VOLT SRAM

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) (0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ±0.3%)

DESCRIPTION		-15		-17		-20		-25		-35		-45			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle															
READ cycle time	^tRC	15		17		20		25		35		45		ns	
Address access time	^tAA		15		17		20		25		35		45	ns	
Chip Enable access time	^tACE		15		17		20		25		35		45	ns	
Output hold from address change	^tOH	3		3		3		5		5		5		ns	
Chip Enable to output in Low-Z	^tLZCE	5		5		3		5		5		5		ns	7
Chip disable to output in High-Z	^tHZCE		6		7		8		10		15		18	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		0		0		ns	
Chip disable to power-down time	^tPD		15		17		20		25		35		45	ns	
Output Enable access time	^tAOE		5		5		4		8		12		15	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		0		0		ns	
Output disable to output in High-Z	^tHZOE		5		5		4		10		12		15	ns	6
WRITE Cycle															
WRITE cycle time	^tWC	15		17		20		25		35		45		ns	
Chip Enable to end of write	^tCW	10		12		12		15		20		25		ns	
Address valid to end of write	^tAW	10		12		12		15		20		25		ns	
Address setup time	^tAS	0		0		0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		0		0		ns	
WRITE pulse width	$^tWP1$	9		12		12		15		20		25		ns	
WRITE pulse width	$^tWP2$	12		8		15		15		20		25		ns	
Data setup time	^tDS	7		7		8		10		15		20		ns	
Data hold time	^tDH	0		0		0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	3		3		3		5		5		5		ns	7
Write Enable to output in High-Z	^tHZWE		6		7		8		10		15		18	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

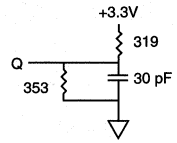


Fig. 1 OUTPUT LOAD EQUIVALENT

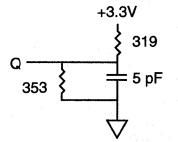


Fig. 2 OUTPUT LOAD EQUIVALENT

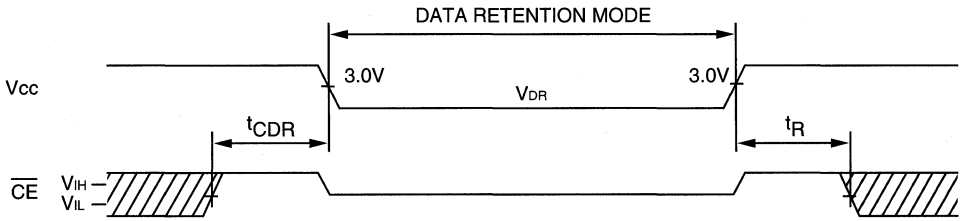
NOTES

1. All voltages referenced to Vss (GND).
2. Overshoot: $V_{IH} \leq +6.0V$ for $t \leq {}^tRC/2$
   Undershoot: $V_{IL} \geq -2.0V$ for $t \leq {}^tRC/2$
   Power-up: $V_{IH} \leq +6.0V$ and $V_{CC} \leq 3.1V$ for $t \leq 200msec$.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ${}^tHZCE$, ${}^tHZOE$ and ${}^tHZWE$ are specified with CL = 5pF as in Fig. 2. Transition is measured ±200mV from steady state voltage.
7. At any given temperature and voltage condition, ${}^tHZCE$ is less than ${}^tLZCE$, and ${}^tHZWE$ is less than ${}^tLZWE$.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables and output enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ${}^tRC$ = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Contact Micron for IT/AT/XT timing and current specifications; they may differ from the commercial temperature range specifications shown in this data sheet.
14. Typical values are measured at 3.3V, 25°C and 25ns cycle time.
15. Typical currents are measured at 25°C.

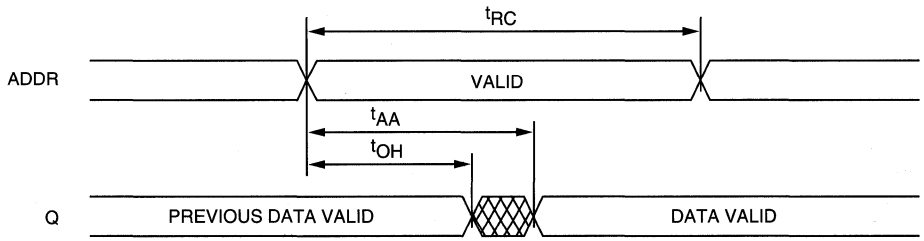
DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP versions only)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data		V_{DR}	2			V	
Data Retention Current L version	$\overline{CE} \geq V_{CC}$ -0.2V Other inputs: $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq V_{SS}$+0.2V V_{CC} = 2V	I_{CCDR}		TBD	50	µA	15
Data Retention Current LP version	$\overline{CE} \geq V_{CC}$ -0.2V V_{CC} = 2V	I_{CCDR}		TBD	50	µA	15
Chip Deselect to Data Retention Time		${}^tCDR$	0			ns	4
Operation Recovery Time		${}^tR$	${}^tRC$			ns	4, 11

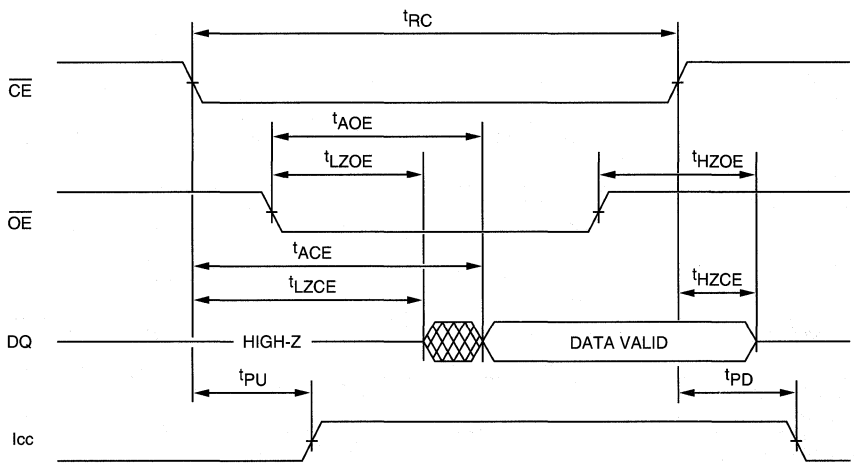
LOW Vcc DATA RETENTION WAVEFORM

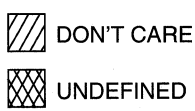


READ CYCLE NO. 1 [8, 9]

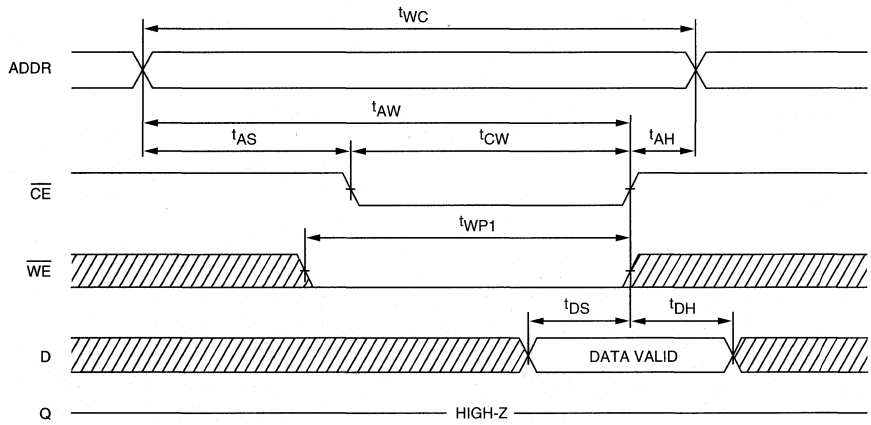


READ CYCLE NO. 2 [7, 8, 10]

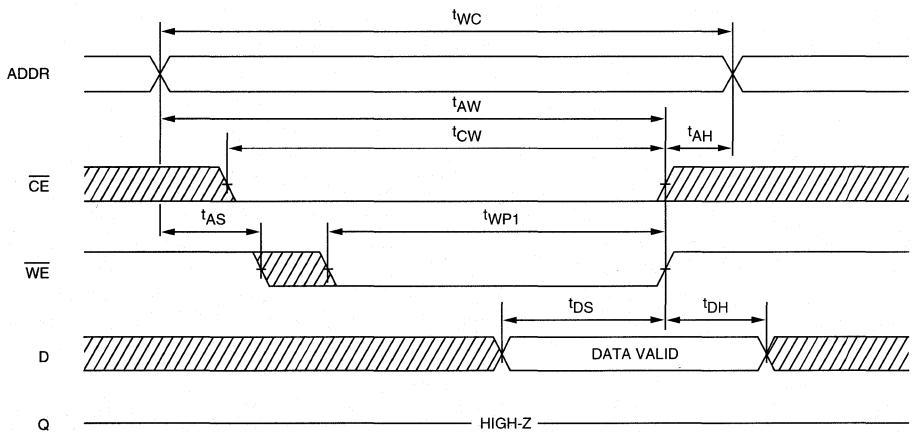




WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)

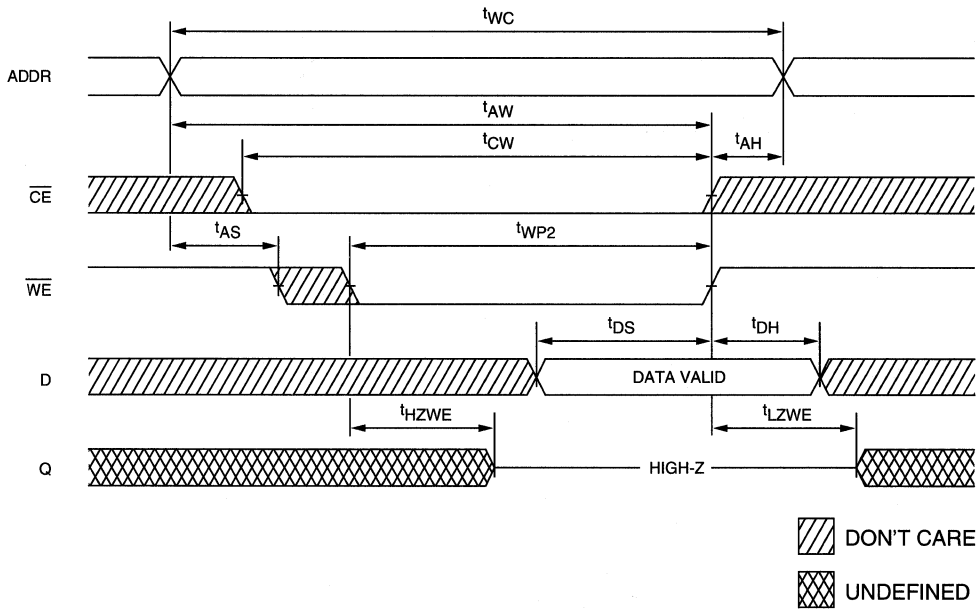


WRITE CYCLE NO. 2 [12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

WRITE CYCLE NO. 3 [7, 12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is active (LOW).

SRAM

256K x 4 SRAM

3.3V OPERATION WITH SINGLE CHIP ENABLE, REVOLUTIONARY PINOUT

FEATURES

- All I/O pins are 5V tolerant
- High speed: 15, 20 and 25ns
- Multiple center power and ground pins for greater noise immunity
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- Automatic $\overline{CE}$ power down
- All inputs and outputs are TTL-compatible
- High-performance, low-power, CMOS double-metal process
- Single +3.3V ±0.3V power supply
- Fast $\overline{OE}$ access times: 10 and 12ns
- Complies to JEDEC low-voltage TTL standards

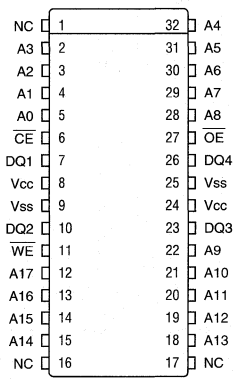
OPTIONS MARKING

- Timing
  - 15ns access -15
  - 20ns access -20
  - 25ns access -25
- Packages
  - 32-pin SOJ (400 mil) DJ
  - 32-pin TSOP (400 mil) TG
- 2V data retention L
- Temperature
  - Commercial (0°C to +70°C) None
  - Industrial (-40°C to +85°C) IT
  - Automotive (-40°C to +125°C) AT
  - Extended (-55°C to +125°C) XT
- Part Number Example: MT5LC256K4D4DJ-20

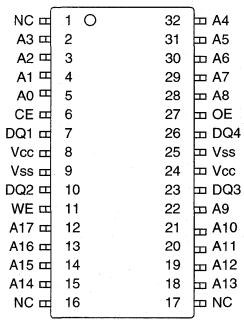
NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

32-Pin SOJ
(SD-5)



32-Pin TSOP
(SE-1)



GENERAL DESCRIPTION

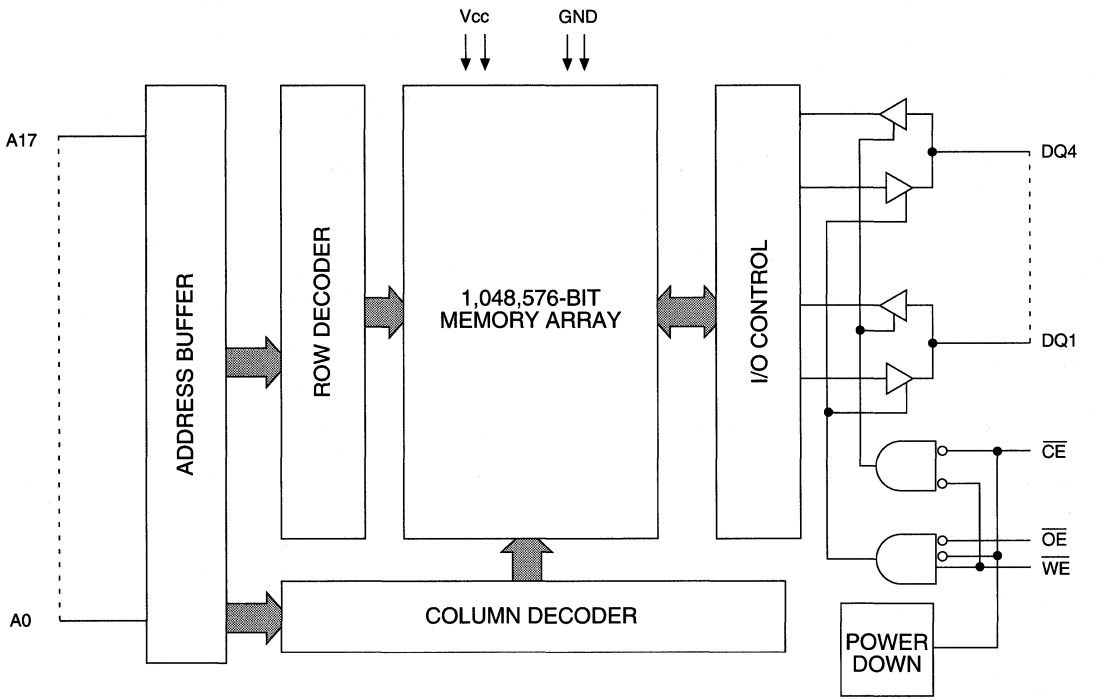
The MT5LC256K4D4 is organized as a 262,144 x 4 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

This device offers multiple center power and ground pins for improved performance. For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) capability. This enhancement can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH while output enable ($\overline{OE}$) and $\overline{CE}$ are LOW. The device offers a reduced power standby mode when disabled. This allows system designers to achieve their low standby power requirements.

All devices operate from a single +3.3V power supply and all inputs and outputs are fully TTL-compatible and 5V tolerant. These low-voltage parts are ideal for mixed 3.3V and 5V systems.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

PIN DESCRIPTIONS

SOJ AND TSOP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
5, 4, 3, 2, 32, 31, 30, 29, 28, 22, 21, 20, 19, 18, 15, 14, 13, 12	A0-A17	Input	Address Inputs: These inputs determine which cell is addressed.
11	$\overline{WE}$	Input	Write Enable: This input determines if the cycle is a READ or WRITE cycle. $\overline{WE}$ is LOW for a WRITE cycle and HIGH for a READ cycle.
6	$\overline{CE}$	Input	Chip Enable: This active LOW input is used to enable the device. When $\overline{CE}$ is HIGH, the chip is disabled and automatically goes into standby power mode.
27	$\overline{OE}$	Input	Output Enable: This active LOW input enables the output drivers.
7, 10, 23, 26	DQ1-DQ4	Input/ Output	SRAM Data I/O: Data inputs and tristate data outputs.
8, 24	Vcc	Supply	Power Supply: 3.3V ±0.3V
9, 25	Vss	Supply	Ground: GND
1, 16, 17	NC	-	No Connect: These signals are not internally connected.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to Vss ..... -0.5V to +4.6V
V_{IN} ..... -0.5V to +6.0V
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ± 0.3V)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.0	5.5	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-1	1	µA	
Output Leakage Current	Output(s) disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	3.0	3.6	V	1

				MAX				
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-15	-20	-25	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	60	100	88	80	mA	3
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	10	20	16	14	mA	
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	0.5	5	5	5	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	6	pF	4
Output Capacitance	V_{CC} =3.3V	C_O	6	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 14) (0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ± 0.3V)

DESCRIPTION		-15		-20		-25			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle									
READ cycle time	^tRC	15		20		25		ns	
Address access time	^tAA		15		20		25	ns	
Chip Enable access time	^tACE		15		20		25	ns	
Output hold from address change	^tOH	4		5		5		ns	
Chip Enable to output in Low-Z	^tLZCE	5		5		5		ns	7
Chip disable to output in High-Z	^tHZCE		6		8		8	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		ns	
Chip disable to power-down time	^tPD		15		20		25	ns	
Output Enable access time	^tAOE		8		10		12	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		ns	
Output disable to output in High-Z	^tHZOE		6		8		8	ns	6
WRITE Cycle									
WRITE cycle time	^tWC	15		20		25		ns	
Chip Enable to end of write	^tCW	12		13		15		ns	
Address valid to end of write	^tAW	9		12		14		ns	
Address setup time	^tAS	0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		ns	
WRITE pulse width	$^tWP1$	9		10		12		ns	
WRITE pulse width	$^tWP2$	9		10		12		ns	
Data setup time	^tDS	8		10		10		ns	
Data hold time	^tDH	0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	1		1		1		ns	7
Write Enable to output in High-Z	^tHZWE		6		8		8	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

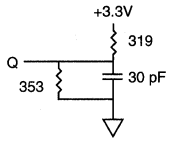


Fig. 1 OUTPUT LOAD EQUIVALENT

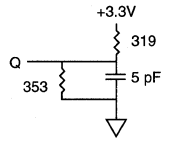


Fig. 2 OUTPUT LOAD EQUIVALENT

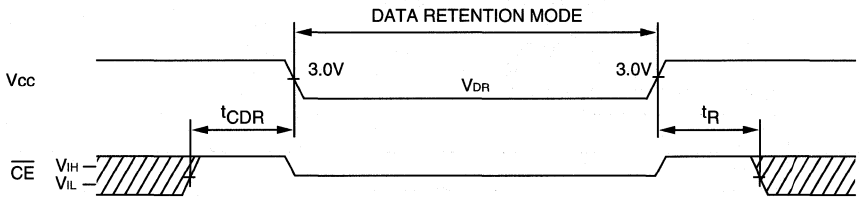
NOTES

1. All voltages referenced to V_{SS} (GND).
2. Overshoot: $V_{IH} \leq +6.0V$ for $t \leq {}^tRC/2$
   Undershoot: $V_{IL} \geq -2.0V$ for $t \leq {}^tRC/2$
   Power-up: $V_{IH} \leq +6.0V$ and $V_{CC} \leq 3.1V$ for $t \leq 200msec$.
3. I_{CC} is dependent on output loading and cycle rates. The specified value applies with the outputs unloaded, and $f = \frac{1}{{}^tRC\ (MIN)}$ Hz.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ${}^tHZCE$, ${}^tHZOE$ and ${}^tHZWE$ are specified with CL = 5pF as in Fig. 2. Transition is measured ±200mV from steady state voltage.
7. At any given temperature and voltage condition, ${}^tHZCE$ is less than ${}^tLZCE$, and ${}^tHZWE$ is less than ${}^tLZWE$.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. Chip enable and output enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ${}^tRC$ = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. The output will be in the High-Z state if output enable is high.
14. Contact Micron for IT/AT/XT timing and current specifications; they may differ from the commercial temperature range specifications shown in this data sheet.
15. Typical currents are measured at 25°C.

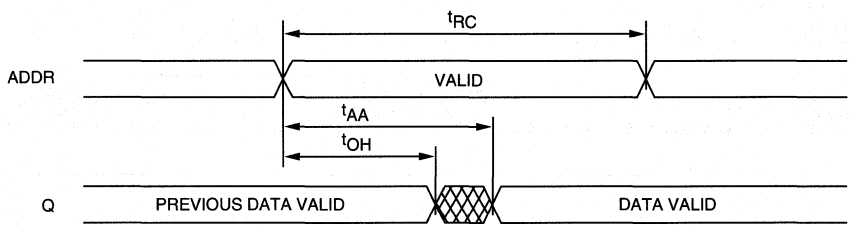
DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP versions only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V_{CC} for Retention Data			V_{DR}	2			V	
Data Retention Current L version LP version	$\overline{CE} \geq (V_{CC} - 0.2V)$ $V_{IN} \geq (V_{CC} - 0.2V)$ or $\leq 0.2V$	V_{CC} = 2V	I_{CCDR}		TBD	TBD	µA	15
Chip Deselect to Data Retention Time			${}^tCDR$	0			ns	4
Operation Recovery Time			${}^tR$	${}^tRC$			ns	4, 11

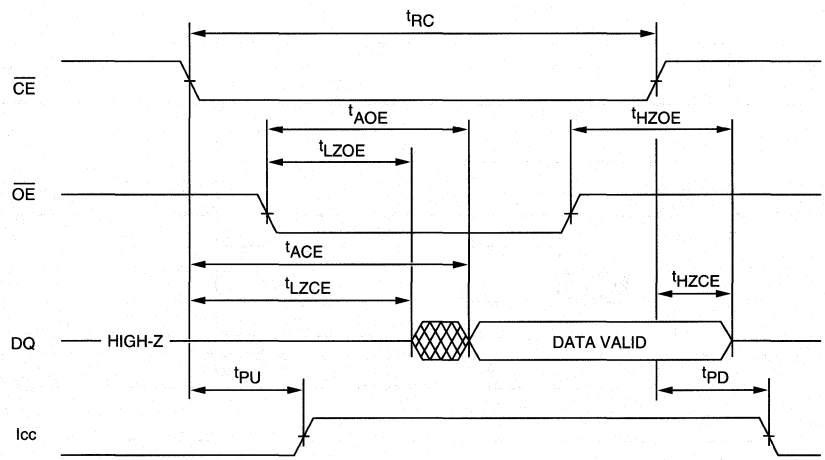
LOW Vcc DATA RETENTION WAVEFORM



READ CYCLE NO. 1 [8, 9]



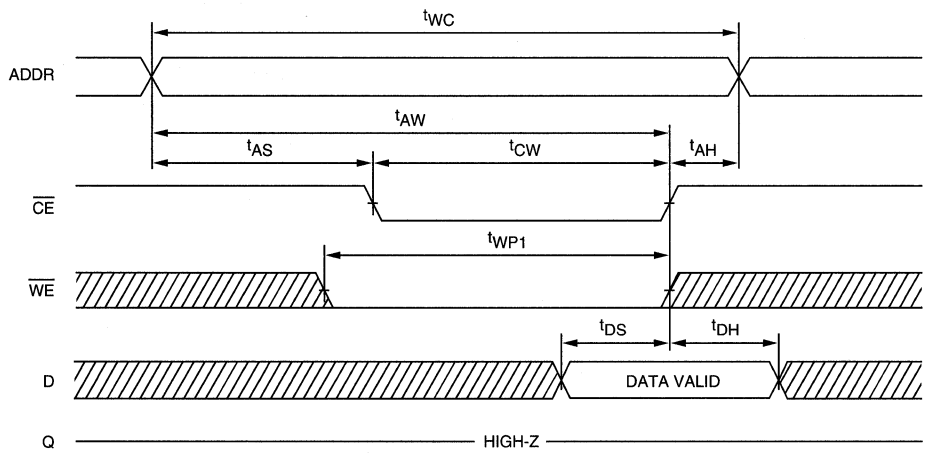
READ CYCLE NO. 2 [7, 8, 10]



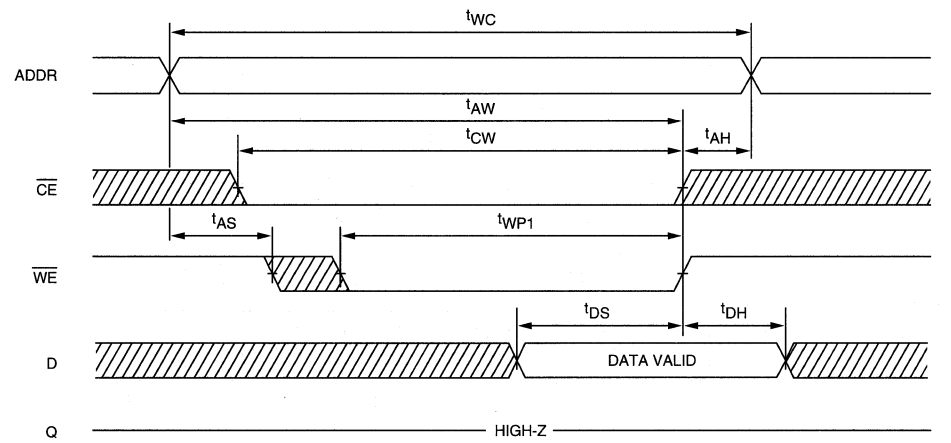
DON'T CARE

UNDEFINED

WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)

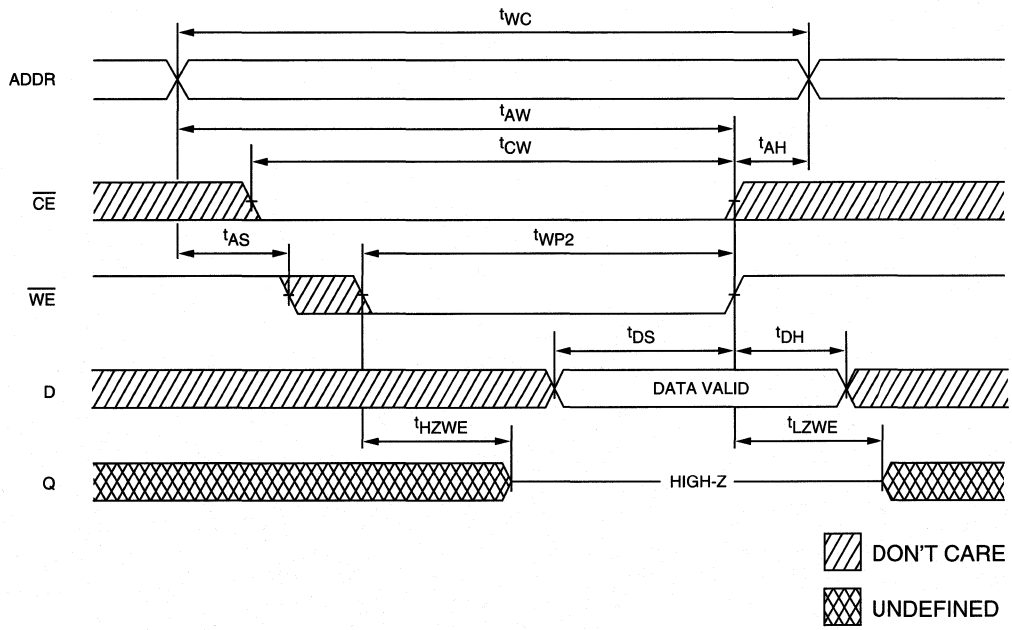


WRITE CYCLE NO. 2 [12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

WRITE CYCLE NO. 3 [7, 12, 13]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is active (LOW).

MICRON SEMICONDUCTOR, INC.

MT5LC256K4D4
REVOLUTIONARY PINOUT 256K x 4 SRAM

SRAM

1 MEG x 4 SRAM

3.3V OPERATION WITH OUTPUT ENABLE, REVOLUTIONARY PINOUT

FEATURES

- All I/O pins are 5V tolerant
- High speed: 12, 15, 20, 25 and 35ns
- High-performance, low-power, CMOS double-metal process
- Multiple center power and ground pins for improved noise immunity
- Single +3.3V ±0.3V power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- All inputs and outputs are TTL-compatible
- Fast $\overline{OE}$ access time: 6, 8, 10, 12 and 15ns
- Complies to JEDEC low-voltage TTL standards

OPTIONS — MARKING

- Timing
  - 12ns access — -12
  - 15ns access — -15
  - 20ns access — -20
  - 25ns access — -25
  - 35ns access — -35
- Packages
  - Plastic SOJ (400 mil) — DJ
  - Plastic TSOP (400 mil) — TG
- 2V data retention — L
- Low power — P
- Temperature
  - Commercial (0°C to +70°C) — None
  - Industrial (-40°C to +85°C) — IT
  - Automotive (-40°C to +125°C) — AT
  - Extended (-55°C to +125°C) — XT
- Part Number Example: MT5LC1M4D4DJ-20

NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

32-Pin SOJ (SD-5)

A0	1	32	A19
A1	2	31	A18
A2	3	30	A17
A3	4	29	A16
A4	5	28	A15
$\overline{CE}$	6	27	$\overline{OE}$
DQ1	7	26	DQ4
Vcc	8	25	Vss
Vss	9	24	Vcc
DQ2	10	23	DQ3
$\overline{WE}$	11	22	A14
A5	12	21	A13
A6	13	20	A12
A7	14	19	A11
A8	15	18	A10
A9	16	17	NC

32-Pin TSOP (SE-1)

A0	1	32	A19
A1	2	31	A18
A2	3	30	A17
A3	4	29	A16
A4	5	28	A15
$\overline{CE}$	6	27	$\overline{OE}$
DQ1	7	26	DQ4
Vcc	8	25	Vss
Vss	9	24	Vcc
DQ2	10	23	DQ3
$\overline{WE}$	11	22	A14
A5	12	21	A13
A6	13	20	A12
A7	14	19	A11
A8	15	18	A10
A9	16	17	NC

GENERAL DESCRIPTION

The MT5LC1M4D4 is organized as a 1,048,576 x 4 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron 4 Meg SRAMs are fabricated using double-layer metal, triple-layer polysilicon technology.

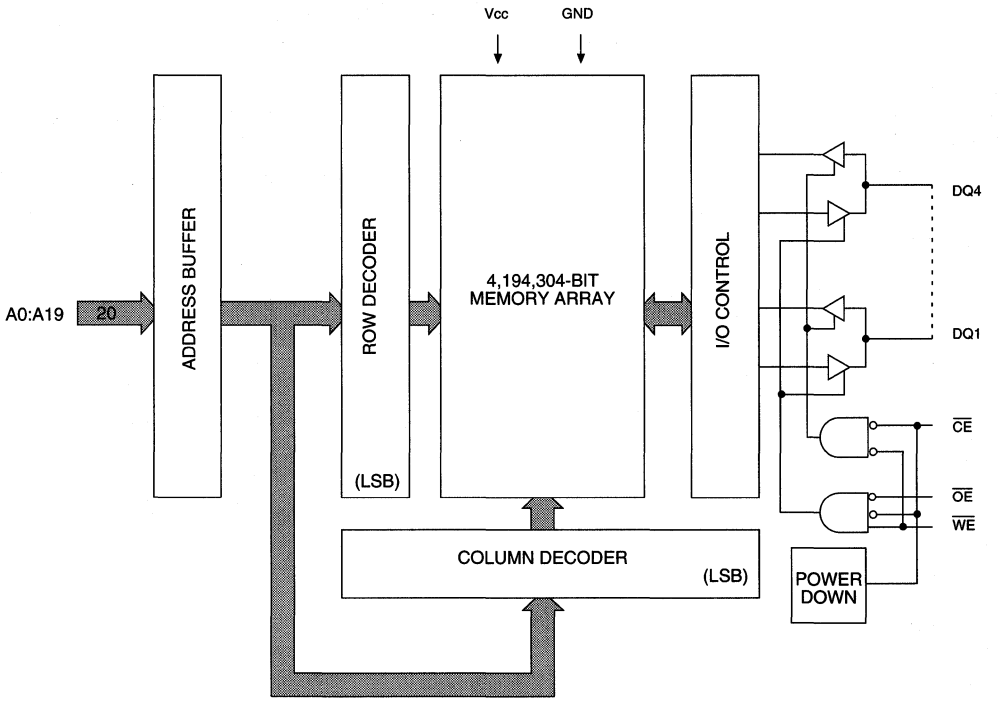
This device offers multiple center power and ground pins for improved performance. For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) capability. These enhancements can place the outputs in High-Z for additional flexibility in system design.

Writing to this device is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH while output enable ($\overline{OE}$) and $\overline{CE}$ go LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

The "P" version also provides a 90 percent reduction in TTL standby current (I_{SB1}) through the use of gated inputs, which also facilitates the design of battery-backed systems. That is, the gated inputs simplify the design effort and circuitry required to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

All devices operate from a single +3.3V power supply and all inputs and outputs are fully TTL-compatible and 5V tolerant. These low-voltage parts are ideal for mixed 3.3V and 5V systems.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

THERMAL IMPEDENCE (EST)[16]

PACKAGE	NUMBER OF PINS	POWER DISSIPATION (watts)	θ_{JC}* (°C/W)	θ_{JA}* (°C/W)
SOJ	32	1.0	15	60
TSOP	32	1.0	5	70

*The thermal impedence numbers assume the device is socketted on a PC board and air flow is zero.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -0.5V to +4.6V
V_{IN} ..... -0.5V to +6.0V
Storage Temperature (plastic) ..... -55°C to +150°C
Short Circuit Output Current 50mA
Junction Temperature** ..... +150°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Maximum junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow. See technical note TN-05-14 for more information.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ±0.3V)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	5.5	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ Vcc	I_{LI}	-1	1	µA	
Output Leakage Current	Output(s) disabled 0V ≤ V_{OUT} ≤ Vcc	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		Vcc	3.0	3.6	V	1

				MAX						
DESCRIPTION	CONDITIONS	SYMBOL	VER	-12	-15	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; Vcc = MAX f = MAX = 1/ ^tRC; outputs open	I_{CC}	ALL	185	165	160	155	145	mA	3
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; Vcc = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	STD	35	30	25	25	20	mA	
			P	1.0	1.0	1.0	1.0	1.0	mA	
	$\overline{CE}$ ≥ Vcc -0.2V; Vcc = MAX; f = 0 VIN ≥ Vcc -0.2V or VIN ≤ VSS +0.2	I_{SB2}	STD	1.0	1.0	1.0	1.0	1.0	mA	
			P	1.0	1.0	1.0	1.0	1.0	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	5	pF	4
Output Capacitance	Vcc = 3.3V	C_O	7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 5, 13) (0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ±0.3V)

DESCRIPTION		-12		-15		-20		-25		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle													
READ cycle time	^tRC	12		15		20		25		35		ns	
Address access time	^tAA		12		15		20		25		35	ns	
Chip Enable access time	^tACE		12		15		20		25		35	ns	
Output hold from address change	^tOH	3		3		3		3		3		ns	
Chip Enable to output in Low-Z	^tLZCE	3		3		5		5		5		ns	7
Chip disable to output in High-Z	^tHZCE		6		7		8		10		15	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		0		ns	
Chip disable to power-down time	^tPD		12		15		20		25		35	ns	
Output Enable access time	^tAOE		6		8		10		12		15	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		0		ns	
Output disable to output in High-Z	^tHZOE		5		6		7		10		12	ns	6
WRITE Cycle													
WRITE cycle time	^tWC	12		15		20		25		35		ns	
Chip Enable to end of write	^tCW	8		10		12		15		20		ns	
Address valid to end of write	^tAW	8		10		12		15		20		ns	
Address setup time	^tAS	0		0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		0		ns	
WRITE pulse width	$^tWP1$	8		9		12		15		20		ns	
WRITE pulse width	$^tWP2$	9		11		14		17		22		ns	
Data setup time	^tDS	6		7		8		10		15		ns	
Data hold time	^tDH	0		0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	3		3		5		5		5		ns	7
Write Enable to output in High-Z	^tHZWE		5		6		8		10		15	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

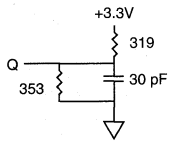


Fig. 1 OUTPUT LOAD EQUIVALENT

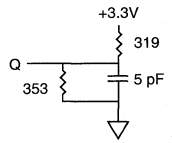


Fig. 2 OUTPUT LOAD EQUIVALENT

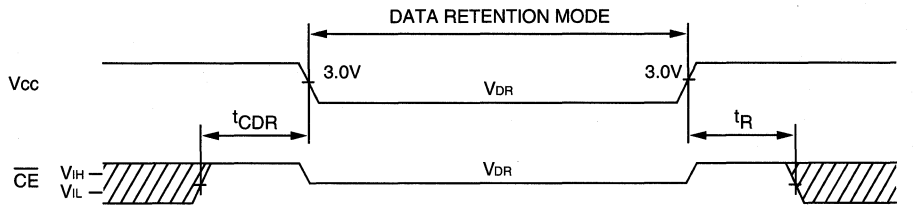
NOTES

1. All voltages referenced to Vss (GND).
2. Overshoot: $V_{IH} \leq +6.0V$ for $t \leq {}^tRC/2$
   Undershoot: $V_{IL} \leq -2.0V$ for $t \leq {}^tRC/2$
   Power-up: $V_{IH} \leq +6.0V$ and $V_{CC} \leq 3.1V$ for $t \leq 200msec$.
3. I_{CC} is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ${}^tHZCE$, ${}^tHZOE$ and ${}^tHZWE$ are specified with CL = 5pF as in Fig. 2. Transition is measured ±200mV from steady state voltage.
7. At any given temperature and voltage condition, ${}^tHZCE$ is less than ${}^tLZCE$, and ${}^tHZWE$ is less than ${}^tLZWE$.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables and output enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ${}^tRC$ = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Contact Micron for IT/AT/XT timing and current specifications; they may differ from the commercial temperature range specifications shown in this data sheet.
14. Output enable ($\overline{OE}$) is inactive (HIGH).
15. Output enable ($\overline{OE}$) is active (LOW).
16. Micron does not warrant functionality nor reliability of any product in which the junction temperature exceeds 150°C. Care should be taken to limit power to acceptable levels.

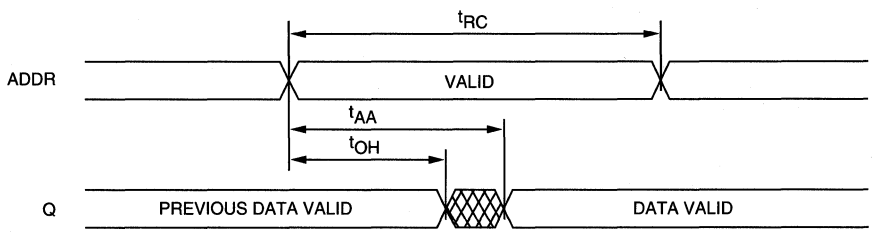
DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP versions only)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Vcc for Retention Data		V_{DR}	2		V	
Data Retention Current L version	$\overline{CE} \geq (Vcc -0.2V)$ $V_{IN} \geq (Vcc -0.2V)$ or $\leq 0.2V$ Vcc = 2.0V	I_{CCDR}		700	µA	
Data Retention Current LP version	$\overline{CE} \geq (Vcc -0.2V)$ Vcc = 2.0V	I_{CCDR}		700	µA	
Chip Deselect to Data Retention Time		${}^tCDR$	0		ns	4
Operation Recovery Time		${}^tR$	${}^tRC$		ns	4, 11

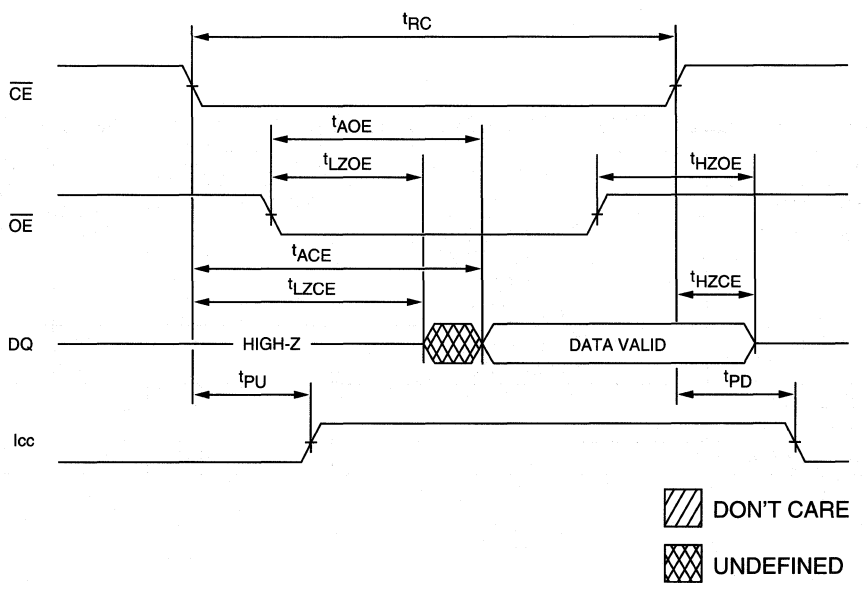
LOW Vcc DATA RETENTION WAVEFORM



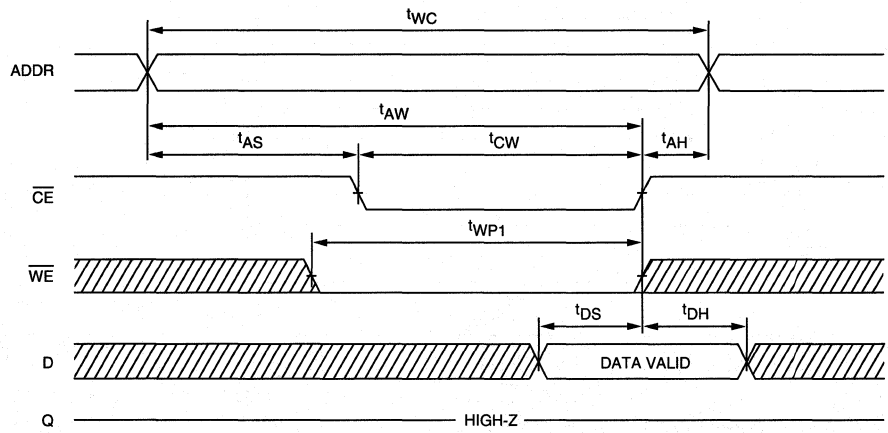
READ CYCLE NO. 1 [8, 9]



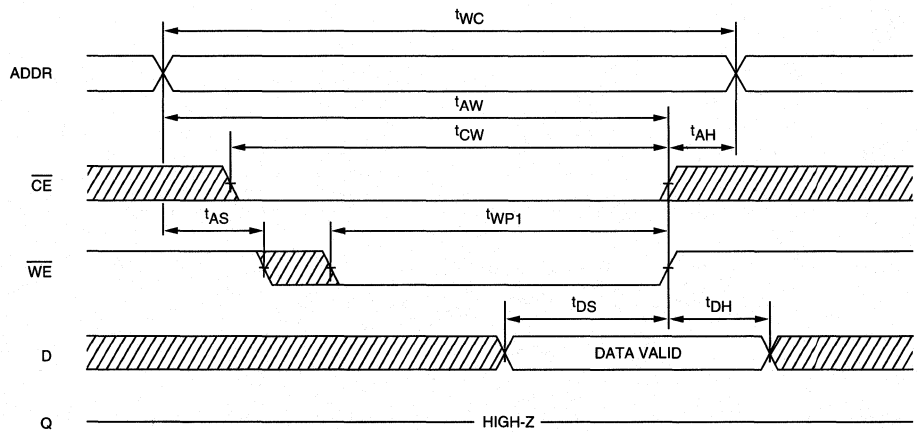
READ CYCLE NO. 2 [7, 8, 10]

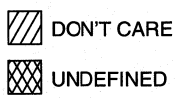


WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)

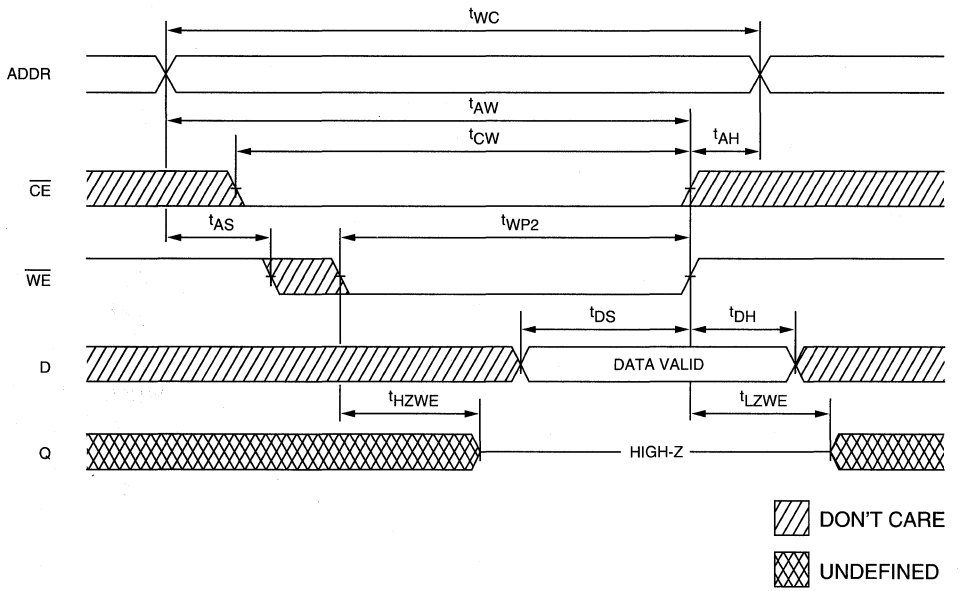


WRITE CYCLE NO. 2 [12, 14]
(Write Enable Controlled)





WRITE CYCLE NO. 3 [7, 12, 15]
(Write Enable Controlled)



SRAM

32K x 8 SRAM

LOW VOLTAGE

FEATURES

- All I/O pins are 5V tolerant
- High speed: 12, 15, 20, 25 and 35ns
- High-performance, low-power, CMOS double-metal process
- Single +3.3V ±0.3V power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- All inputs and outputs are TTL-compatible
- Complies to JEDEC low-voltage TTL standards

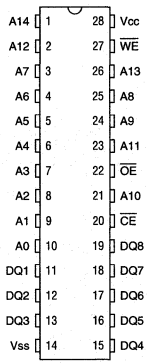
OPTIONS / MARKING

- Timing
  - 12ns access: -12
  - 15ns access: -15
  - 20ns access: -20
  - 25ns access: -25
  - 35ns access: -35
- Packages
  - Plastic DIP (300 mil): None
  - Plastic SOJ (300 mil): DJ
- 2V data retention: L
- Low power: P
- Temperature
  - Commercial (0°C to +70°C): None
  - Industrial (-40°C to +85°C): IT
  - Automotive (-40°C to +125°C): AT
  - Extended (-55°C to +125°C): XT
- Part Number Example: MT5LC2568DJ-25 P

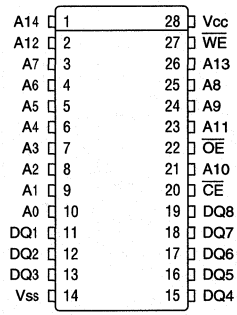
NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

28-Pin DIP (SA-4)



28-Pin SOJ (SD-2)



GENERAL DESCRIPTION

The MT5LC2568 is organized as a 32,768 x 8 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

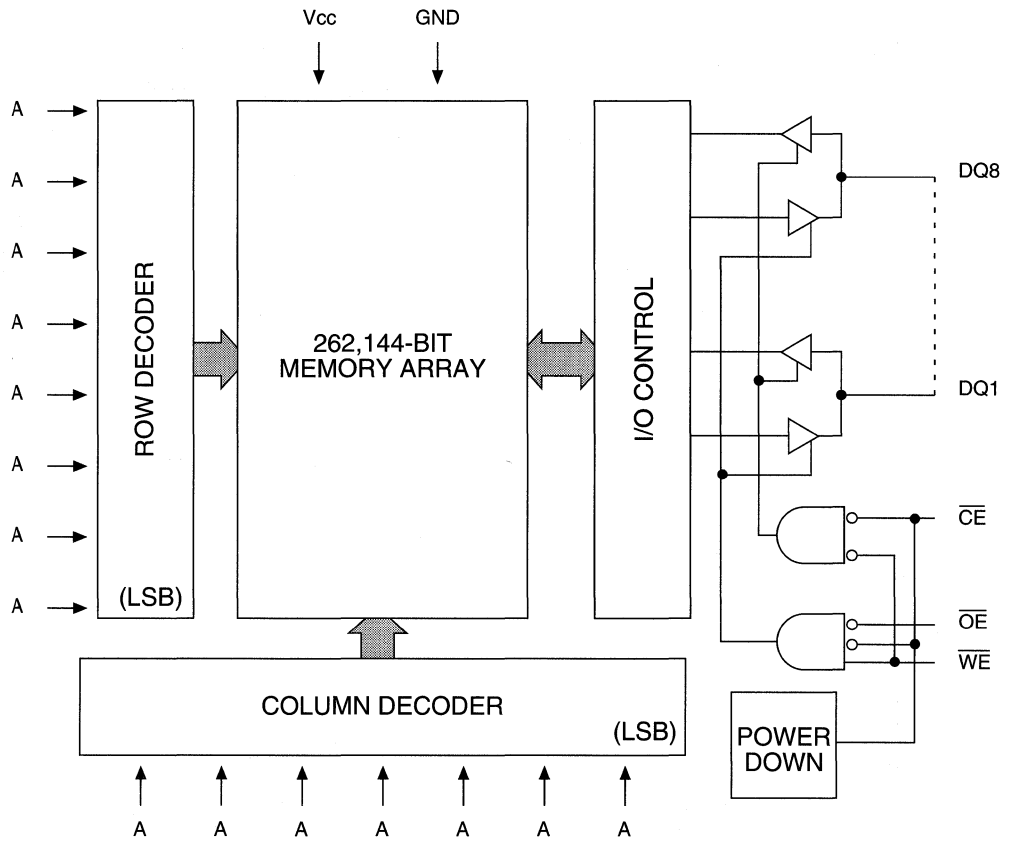
For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) with this organization. These enhancements can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ and $\overline{OE}$ go LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

The "P" version provides a reduction in both operating current (I_{CC}) and TTL standby current (I_{SB1}). The latter is achieved through the use of gated inputs on the $\overline{WE}$, $\overline{OE}$ and address lines, which also facilitates the design of battery-backed systems. That is, the gated inputs simplify the design effort and circuitry required to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

The MT5C2568 operates from a single +3.3V power supply and all inputs and outputs are fully TTL-compatible and 5V tolerant. These low-voltage parts are ideal for mixed 3.3V and 5V systems.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -0.5V to +4.6V
V_{IN} ..... -0.5V to +6.0
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; V_{CC} = 3.3V ±0.3V)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.0	5.5	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-1	1	µA	
Output Leakage Current	Output(s) disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	3.0	3.6	V	1

					MAX						
DESCRIPTION	CONDITIONS	SYM	VER	TYP	-12	-15	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX outputs open f = MAX = $1/t_{RC}$	I_{CC}	STD	73	125	110	95	90	85	mA	3, 14
			P	39	-	65	55	50	50	mA	
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX outputs open f = MAX = $1/t_{RC}$	I_{SB1}	STD	17	35	30	25	25	25	mA	14
			P	8	-	18	15	12	12	mA	14
	$\overline{CE} \ge V_{CC}$ - 0.2V; V_{CC} = MAX $V_{IN} \ge V_{CC}$ - 0.2V or $V_{IN} \le V_{SS}$ + 0.2V	I_{SB2}	STD	1.0	3	3	3	3	5	mA	14
			P	300	-	750	750	750	1,500	µA	14

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	6	pF	4
Output Capacitance	V_{CC} = 3.3V	C_O	6	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) (0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ±0.3V)

DESCRIPTION		-12		-15		-20		-25		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle													
READ cycle time	tRC	12		15		20		25		35		ns	
Address access time	tAA		12		15		20		25		35	ns	
Chip Enable access time	tACE		12		15		20		25		35	ns	
Output hold from address change	tOH	3		3		3		3		3		ns	
Output hold from address change	tOH	–		4		4		4		4		ns	16
Chip Enable to output in Low-Z	tLZCE	3		3		3		3		3		ns	7
Chip Enable to output in Low-Z	tLZCE	–		4		4		4		4		ns	16
Chip disable to output in High-Z	tHZCE		6		8		9		9		15	ns	6, 7
Chip Enable to power-up time	tPU	0		0		0		0		0		ns	
Chip disable to power-down time	tPD		12		15		20		25		35	ns	
Output Enable access time	tAOE		6		7		8		8		12	ns	
Output Enable to output in Low-Z	tLZOE	0		0		0		0		0		ns	
Output disable to output in High-Z	tHZOE		6		6		7		7		10	ns	6
WRITE Cycle													
WRITE cycle time	tWC	12		15		20		25		35		ns	
Chip Enable to end of write	tCW	8		10		12		15		20		ns	
Address valid to end of write	tAW	8		10		12		15		20		ns	
Address setup time	tAS	0		0		0		0		0		ns	
Address hold from end of write	tAH	1		1		1		1		1		ns	
Address hold from end of write	tAH	–		0		0		0		0		ns	16
WRITE pulse width	tWP1	8		10		12		15		20		ns	
WRITE pulse width	tWP2	12		12		15		15		20		ns	
Data setup time	tDS	7		8		10		10		15		ns	
Data hold time	tDH	0		0		0		0		0		ns	
Write disable to output in Low-Z	tLZWE	3		3		3		3		3		ns	7
Write Enable to output in High-Z	tHZWE		6		7		8		10		12	ns	6,7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

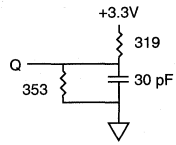


Fig. 1 OUTPUT LOAD EQUIVALENT

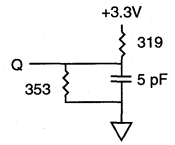


Fig. 2 OUTPUT LOAD EQUIVALENT

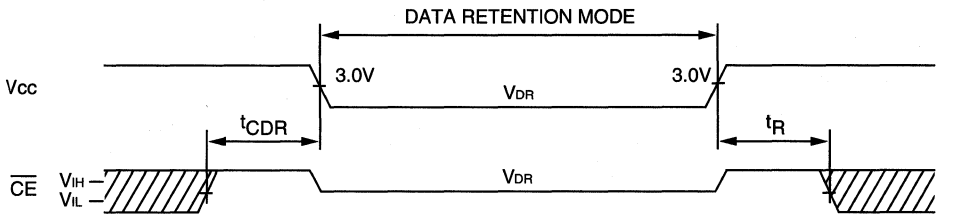
NOTES

1. All voltages referenced to V_{SS} (GND).
2. Overshoot: $V_{IH} \leq +6.0V$ for $t \leq {}^tRC/2$
   Undershoot: $V_{IL} \geq -2.0V$ for $t \leq {}^tRC/2$
   Power-up: $V_{IH} \leq +6.0V$ and $V_{CC} \leq 3.1V$ for $t \leq 200msec$.
3. I_{CC} is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ${}^tHZCE$, ${}^tHZOE$ and ${}^tHZWE$ are specified with CL = 5pF as in Fig. 2. Transition is measured ±200mV from steady state voltage.
7. At any given temperature and voltage condition, ${}^tHZCE$ is less than ${}^tLZCE$ and ${}^tHZWE$ is less than ${}^tLZWE$.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ${}^tRC$ = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Contact Micron for IT/AT/XT timing and current specifications; they may differ from the commercial temperature range specifications shown in this data sheet.
14. Typical values are measured at 3.3V, 25°C and 20ns cycle time for P, 15ns for STD.
15. Typical currents are measured at 25°C.
16. This timing specification is valid only for P (low power) parts.

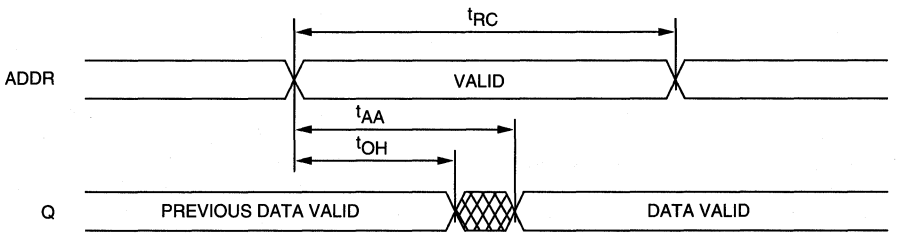
DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP versions only)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V_{CC} for Retention Data		V_{DR}	2			V	
Data Retention Current L version	$\overline{CE} \geq V_{CC}$ -0.2V Other inputs: $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq V_{SS}$+0.2V V_{CC} = 2V	I_{CCDR}		310	500	µA	15
Data Retention Current LP version	$\overline{CE} \geq V_{CC}$ -0.2V V_{CC} = 2V	I_{CCDR}		195	350	µA	15
Chip Deselect to Data Retention Time		${}^tCDR$	0			ns	4
Operation Recovery Time		${}^tR$	${}^tRC$			ns	4, 11

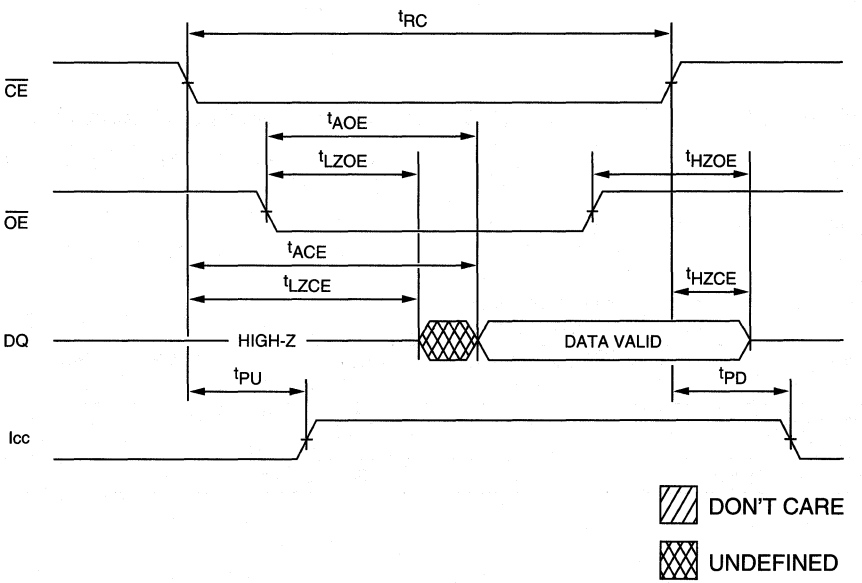
LOW Vcc DATA RETENTION WAVEFORM



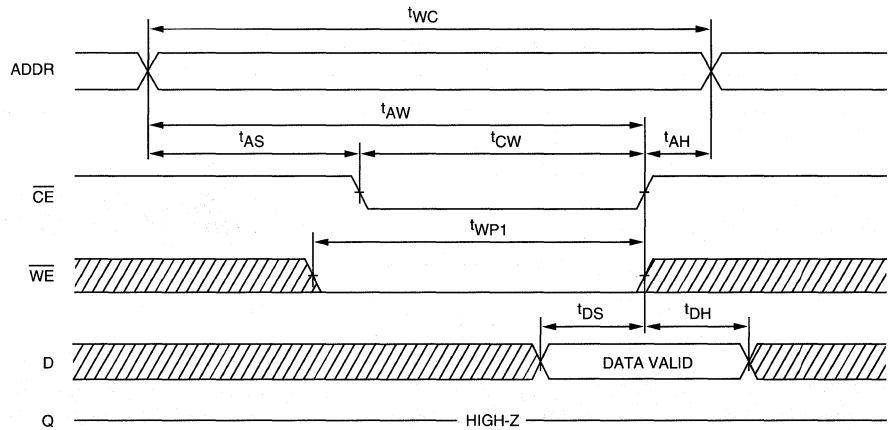
READ CYCLE NO. 1 [8, 9]



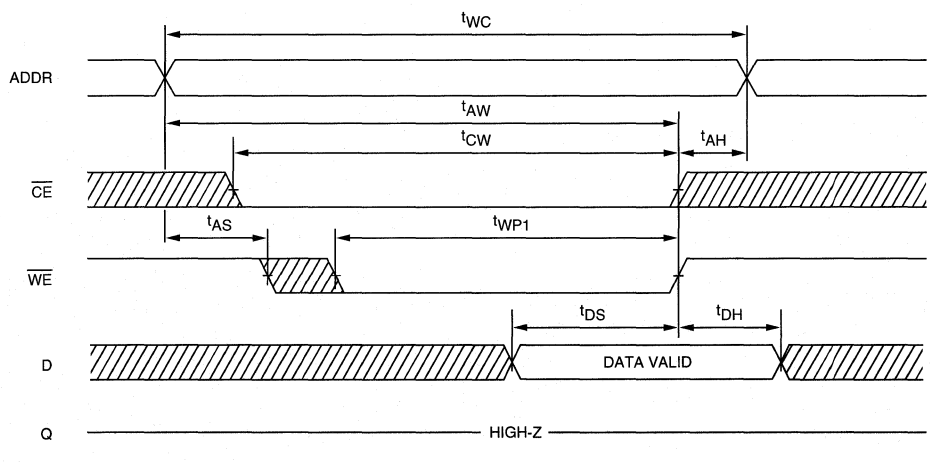
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)

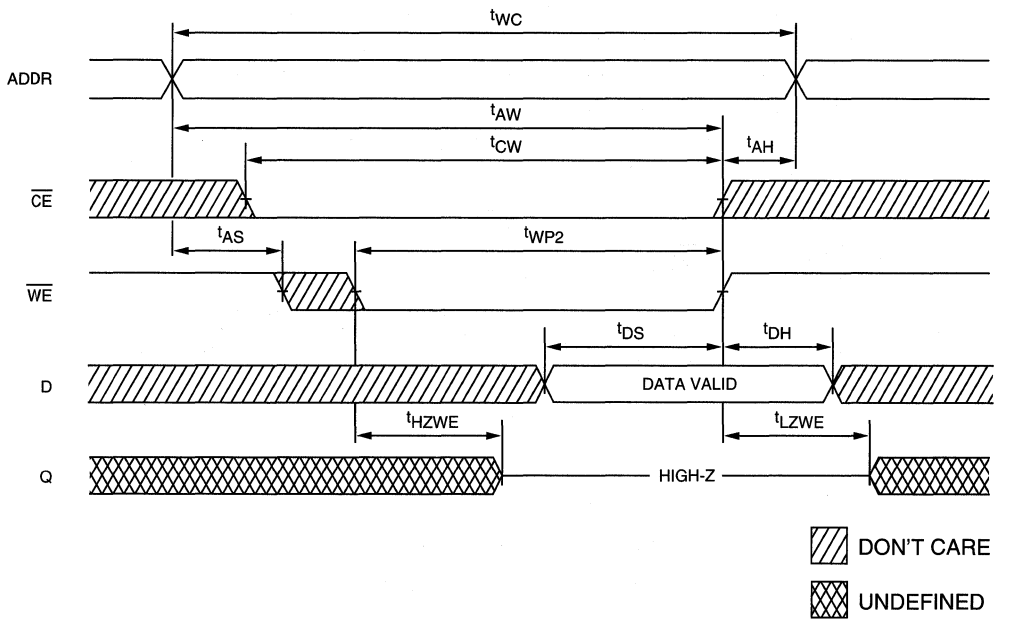


WRITE CYCLE NO. 2 [12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

WRITE CYCLE NO. 3 [7, 12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is active (LOW).

SRAM

128K x 8 SRAM

LOW VOLTAGE WITH OUTPUT ENABLE

FEATURES

- All I/O pins are 5V tolerant
- High speed: 15, 17, 20, 25, 35 and 45ns
- High-performance, low-power, CMOS double-metal process
- Single +3.3V ±0.3V power supply
- Easy memory expansion with $\overline{CE1}$, CE2 and $\overline{OE}$ options
- All inputs and outputs are TTL-compatible
- Fast $\overline{OE}$ access time: 8ns
- Complies to JEDEC low-voltage TTL standards

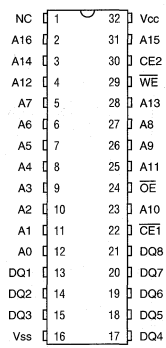
OPTIONS — MARKING

- Timing
  - 15ns access — -15
  - 17ns access — -17
  - 20ns access — -20
  - 25ns access — -25
  - 35ns access — -35
  - 45ns access — -45
- Packages
  - Plastic DIP (400 mil) — None
  - Plastic SOJ (400 mil) — DJ
  - Plastic SOJ (300 mil) — SJ
- 2V data retention — L
- 2V data retention, low power — LP
- Temperature
  - Commercial (0°C to +70°C) — None
  - Industrial (-40°C to +85°C) — IT
  - Automotive (-40°C to +125°C) — AT
  - Extended (-55°C to +125°C) — XT
- Part Number Example: MT5LC1008DJ-35 LP

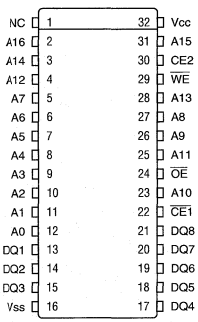
NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

32-Pin DIP
(SA-6)



32-Pin SOJ
(SD-4)
(SD-5)



GENERAL DESCRIPTION

The MT5LC1008 is organized as a 131,072 x 8 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

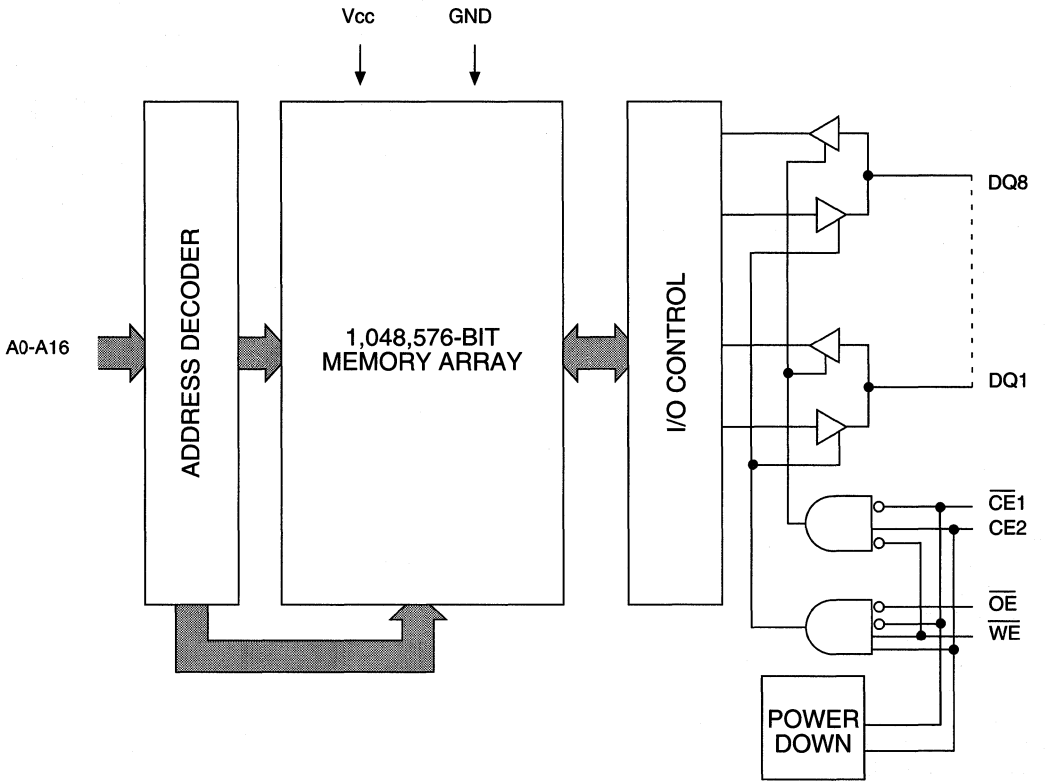
For flexibility in high-speed memory applications, Micron offers dual chip enables ($\overline{CE1}$, CE2). This enhancement can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE1}$ inputs are both LOW and CE2 is HIGH. Reading is accomplished when $\overline{WE}$ and CE2 remain HIGH and $\overline{CE1}$ goes LOW. The device offers reduced power standby modes when disabled. These modes allow system designers to meet low standby power requirements.

The "LP" version provides a reduction in both CMOS standby current (I_{SB2}) and TTL standby current (I_{SB1}) over the standard part. This is achieved through the use of gated inputs on the $\overline{WE}$, $\overline{OE}$ and address lines. The gated inputs also facilitate the design of battery-backed systems where the designer needs to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

All devices operate from a single +3.3V power supply and all inputs and outputs are fully TTL-compatible and 5V tolerant. These low-voltage parts are ideal for mixed 3.3V and 5V systems.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE1}$	CE2	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	X	HIGH-Z	STANDBY
STANDBY	X	X	L	X	HIGH-Z	STANDBY
READ	L	L	H	H	Q	ACTIVE
NOT SELECTED	H	L	H	H	HIGH-Z	ACTIVE
WRITE	X	L	H	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -0.5V to +4.6V
V_{IN} ..... -0.5V to +6.0V
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; V_{CC} = 3.3V ±0.3V)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.0	5.5	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-1	1	µA	
Output Leakage Current	Output(s) disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	3.0	3.6	V	1

				MAX							
DESCRIPTION	CONDITIONS	SYMBOL	VER	-15	-17	-20	-25	-35	-45	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE1} \le V_{IL}$ AND CE2 $\ge V_{IH}$; V_{CC} = MAX; outputs open f = MAX = 1/tRC	I_{CC}	ALL	85	75	65	55	45	40	mA	3, 15
Power Supply Current: Standby	$\overline{CE1} \le V_{IH}$ AND CE2 $\ge V_{IL}$; V_{CC} = MAX; outputs open f = MAX = 1/tRC	I_{SB1}	STD, L	20	18	14	12	8	6	mA	15, 16
			LP	500	500	500	500	500	500	µA	
	$\overline{CE1} \ge V_{CC}$ - 0.2V or CE2 $\le$ Vss + o.2V V_{CC} = MAX $V_{IN} \ge V_{CC}$ - 0.2V or $V_{IN} \le$ Vss + 0.2V	I_{SB2}	STD, L	300	300	300	300	300	300	µA	15, 17
			LP	100	100	100	100	100	100	µA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	8	pF	4
Output Capacitance	V_{CC} = 3.3V	C_O	8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 14) (0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ±0.3V)

DESCRIPTION	SYM	-15		-17		-20		-25		-35		-45		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
READ Cycle															
READ cycle time	^tRC	15		17		20		25		35		45		ns	
Address access time	^tAA		15		17		20		25		35		45	ns	
Chip Enable access time	^tACE		15		17		20		25		35		45	ns	
Output hold from address change	^tOH	3		3		3		5		5		5		ns	
Chip Enable to output in Low-Z	^tLZCE	5		5		3		5		5		5		ns	7
Chip disable to output in High-Z	^tHZCE		6		7		8		10		15		18	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		0		0		ns	
Chip disable to power-down time	^tPD		15		17		20		25		35		45	ns	
Output Enable access time	^tAOE		5		5		4		8		12		15	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		0		0		ns	
Output disable to output in High-Z	^tHZOE		5		5		4		10		12		15	ns	6
WRITE Cycle															
WRITE cycle time	^tWC	15		17		20		25		35		45		ns	
Chip Enable to end of write	^tCW	10		12		12		15		20		25		ns	
Address valid to end of write	^tAW	10		12		12		15		20		25		ns	
Address setup time	^tAS	0		0		0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		0		0		ns	
WRITE pulse width	$^tWP1$	9		12		12		15		20		25		ns	
WRITE pulse width	$^tWP2$	12		13		15		15		20		25		ns	
Data setup time	^tDS	7		8		8		10		15		20		ns	
Data hold time	^tDH	0		0		0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	3		3		3		5		5		5		ns	7
Write Enable to output in High-Z	^tHZWE		6		7		8		10		15		18	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

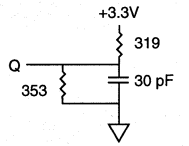


Fig. 1 OUTPUT LOAD EQUIVALENT

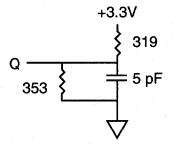


Fig. 2 OUTPUT LOAD EQUIVALENT

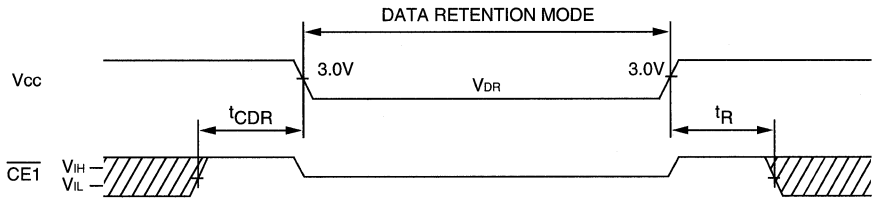
NOTES

1. All voltages referenced to Vss (GND).
2. Overshoot: $V_{IH} \leq +6.0V$ for $t \leq {}^tRC/2$
   Undershoot: $V_{IL} \geq -2.0V$ for $t \leq {}^tRC/2$
   Power-up: $V_{IH} \leq +6.0V$ and $V_{CC} \leq 3.1V$ for $t \leq 200msec$.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ${}^tHZCE$, ${}^tHZOE$ and ${}^tHZWE$ are specified with CL = 5pF as in Fig. 2. Transition is measured ±200mV from steady state voltage.
7. At any given temperature and voltage condition, ${}^tHZCE$ is less than ${}^tLZCE$ and ${}^tHZWE$ is less than ${}^tLZWE$.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables and output enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ${}^tRC$ = Read Cycle Time.
12. CE2 timing is the same as $\overline{CE1}$ timing. The wave form is inverted.
13. Chip enable and write enable can initiate and terminate a WRITE cycle.
14. Contact Micron for IT/AT/XT timing and current specifications; they may differ from the commercial temperature range specifications shown in this data sheet.
15. Typical values are measured at 3.3V, 25°C and 25ns cycle time.
16. One chip enable must be inactive; the other may be $\geq V_{IH}$ or $\leq V_{IL}$.
17. One chip enable must be inactive; the other may be $\leq V_{SS} +0.2$or $\geq V_{CC} -0.2$.
18. Typical currents are measured at 25°C.

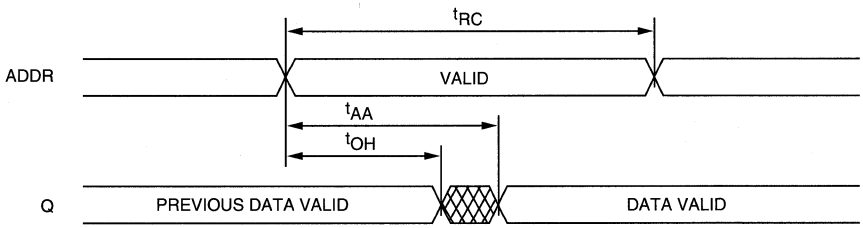
DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP versions only)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data		V_{DR}	2			V	
Data Retention Current L version	$\overline{CE1} \geq V_{CC} -0.2V$ or $CE2 \leq V_{SS} +0.2V$ Other inputs: $V_{IN} \geq V_{CC} -0.2V$ or $V_{IN} \leq V_{SS} +0.2V$ $V_{CC} = 2V$	I_{CCDR}		TBD	50	µA	17, 18
Data Retention Current LP version	$\overline{CE1} \geq V_{CC} -0.2V$ or $CE2 \leq V_{SS} +0.2V$ $V_{CC} = 2V$	I_{CCDR}		TBD	50	µA	17, 18
Chip Deselect to Data Retention Time		${}^tCDR$	0			ns	4
Operation Recovery Time		${}^tR$	${}^tRC$			ns	4, 11

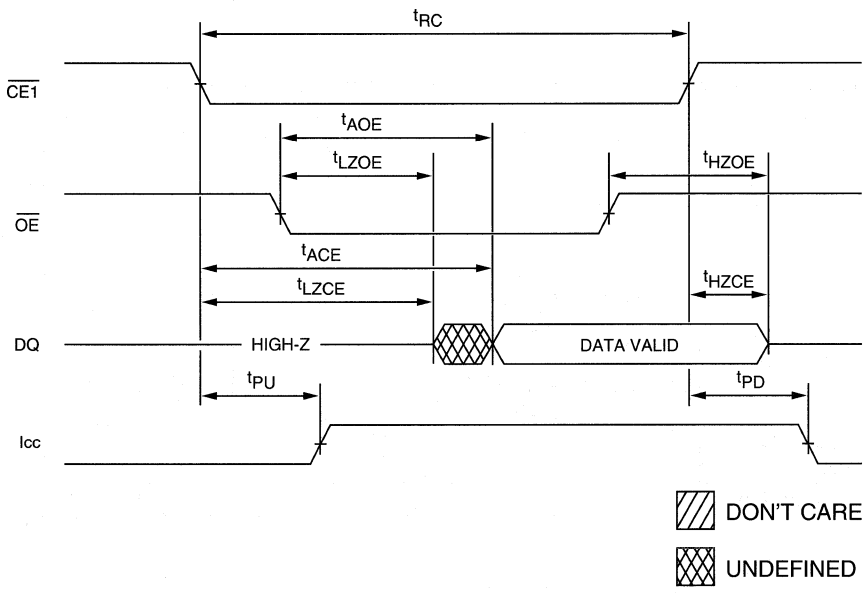
LOW Vcc DATA RETENTION WAVEFORM [12]



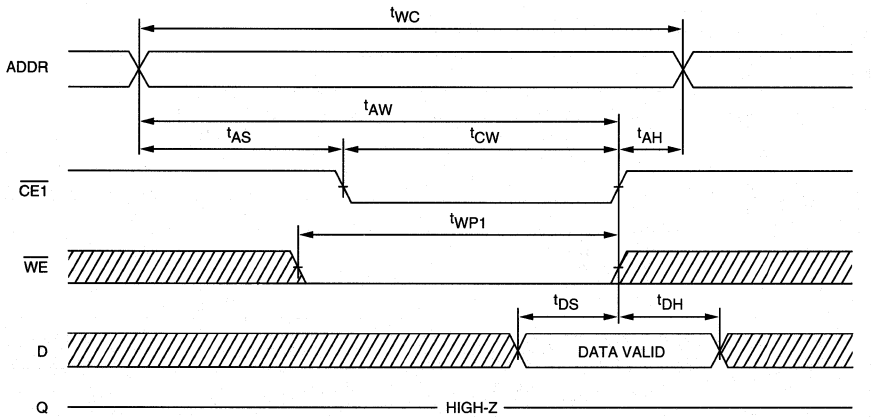
READ CYCLE NO. 1 [8, 9]



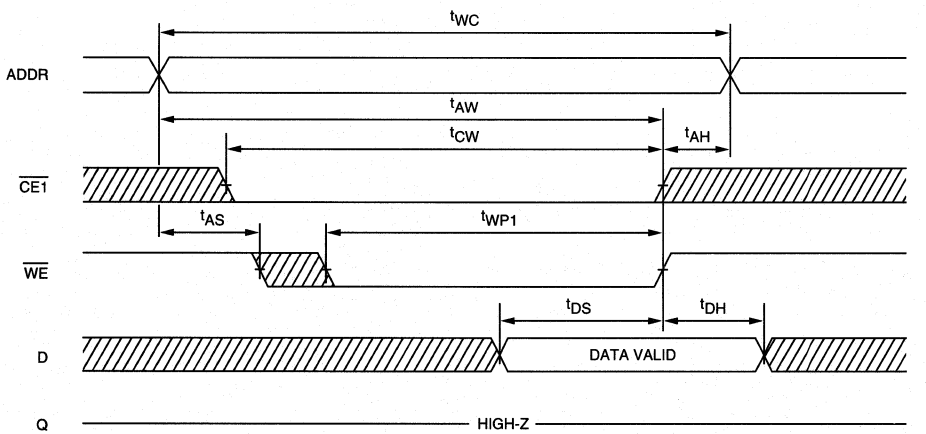
READ CYCLE NO. 2 [7, 8, 10, 12]



WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)

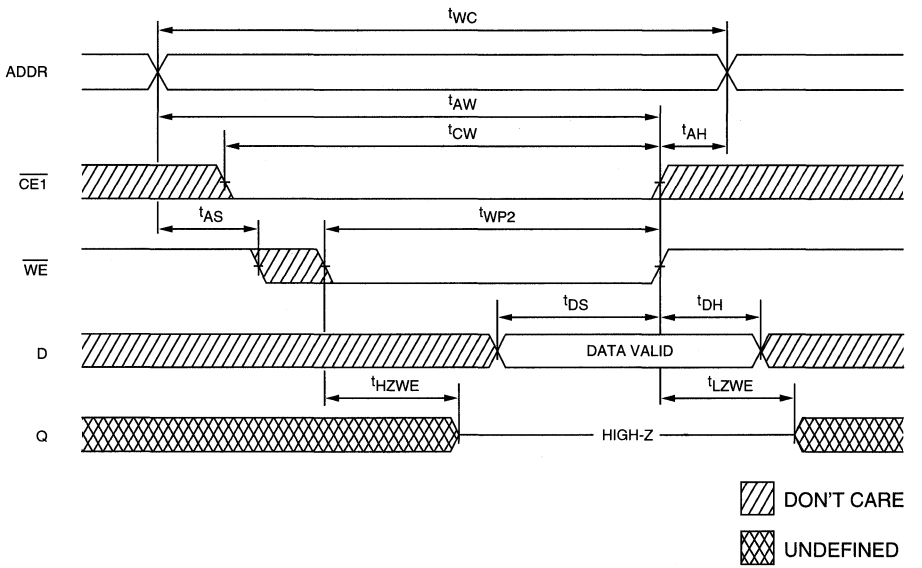


WRITE CYCLE NO. 2 [12, 13]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

WRITE CYCLE NO. 3 [7, 12, 13]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is active (LOW).

SRAM

128K x 8 SRAM

3.3V OPERATION WITH SINGLE CHIP ENABLE, REVOLUTIONARY PINOUT

FEATURES

- All I/O pins are 5V tolerant
- High speed: 15, 20 and 25ns
- Multiple center power and ground pins for greater noise immunity
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- Automatic $\overline{CE}$ power down
- All inputs and outputs are TTL-compatible
- High-performance, low-power, CMOS double-metal process
- Single 3.3V ±0.3V power supply
- Fast $\overline{OE}$ access times: 10 and 12ns
- Complies to JEDEC low-voltage TTL-standards

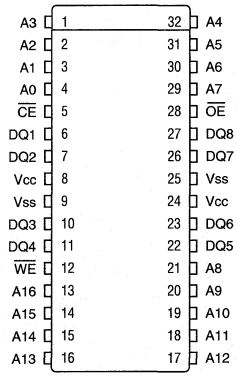
OPTIONS — MARKING

- Timing
  - 15ns access — -15
  - 20ns access — -20
  - 25ns access — -25
- Packages
  - 32-pin SOJ (400 mil) — DJ
  - 32-pin TSOP (400 mil) — TG
- 2V data retention — L
- Temperature
  - Commercial (0°C to +70°C) — None
  - Industrial (-40°C to +85°C) — IT
  - Automotive (-40°C to +125°C) — AT
  - Extended (-55°C to +125°C) — XT
- Part Number Example: MT5LC128K8D4DJ-20

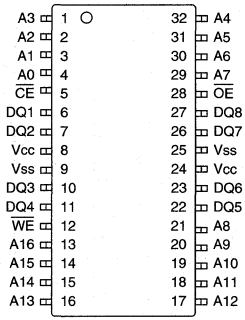
NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

32-Pin SOJ (SD-5)



32-Pin TSOP (SE-1)



GENERAL DESCRIPTION

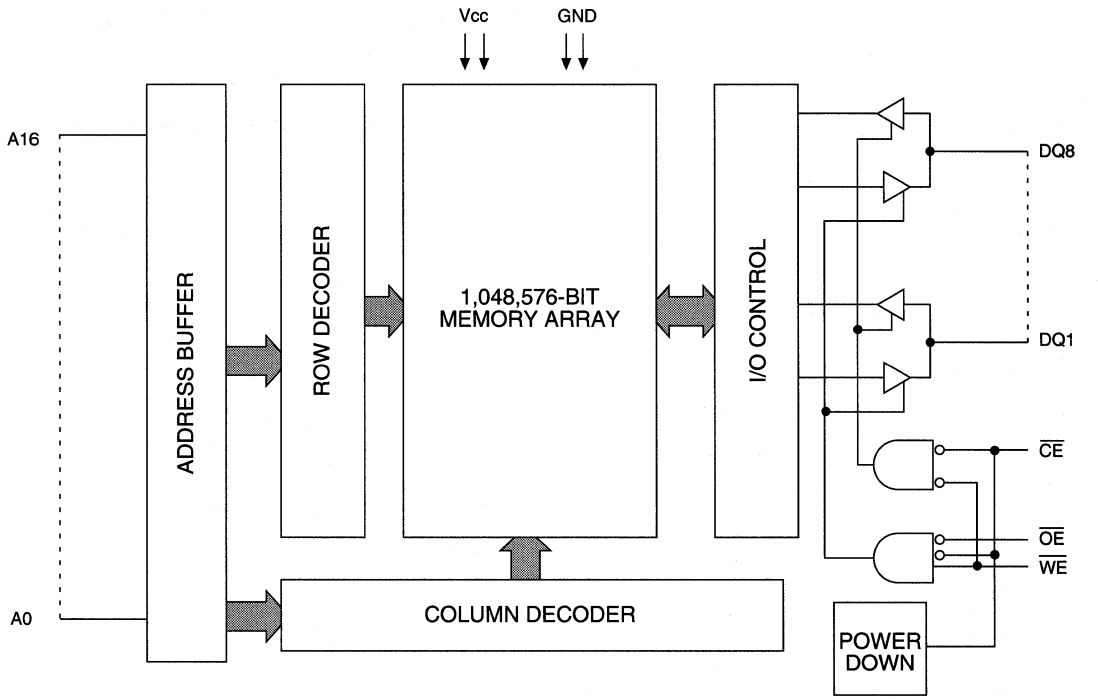
The MT5LC128K8D4 is organized as a 131,072 x 8 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) capability. This enhancement can place the output in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and chip enable inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes LOW. The device offers a reduced power standby mode when disabled. This allows system designers to achieve their low standby power requirements.

All devices operate from a single +3.3V power supply and all inputs and outputs are fully TTL-compatible and 5V tolerant. These low-voltage parts are ideal for mixed 3.3V and 5V systems.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

PIN DESCRIPTIONS

SOJ AND TSOP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
4, 3, 2, 1, 32, 31, 30, 29, 21, 20, 19, 18, 17, 16, 15, 14, 13	A0-A16	Input	Address Inputs: These inputs determine which cell is addressed.
12	$\overline{WE}$	Input	Write Enable: This input determines if the cycle is a READ or WRITE cycle. $\overline{WE}$ is LOW for a WRITE cycle and HIGH for a READ cycle.
5	$\overline{CE}$	Input	Chip Enable: This active LOW input is used to enable the device. When $\overline{CE}$ is HIGH, the chip is disabled and automatically goes into standby power mode.
28	$\overline{OE}$	Input	Output Enable: This active LOW input enables the output drivers.
6, 7, 10, 11, 22, 23, 26, 27	DQ1-DQ8	Input/ Output	SRAM Data I/O: Data inputs and tristate data outputs.
8, 24	V_{CC}	Supply	Power Supply: 3.3V ±0.3V
9, 25	V_{SS}	Supply	Ground: GND

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to Vss ..... -0.5V to +4.6V
V_{IN} ..... -0.5V +6.0V
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc =3.3V ±0.3V)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.0	5.5	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ Vcc	I_{LI}	-1	1	µA	
Output Leakage Current	Output(s) disabled 0V ≤ V_{OUT} ≤ Vcc	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		Vcc	3.0	3.6	V	1

				MAX				
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-15	-20	-25	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; Vcc = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	60	100	88	80	mA	3
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; Vcc = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	10	20	16	14	mA	
	$\overline{CE}$ ≥ Vcc -0.2V; Vcc = MAX V_{IN} ≤ Vss +0.2V V_{IN} ≥ Vcc -0.2V; f = 0	I_{SB2}	0.5	5	5	5	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	6	pF	4
Output Capacitance	Vcc =3.3V	C_O	6	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 14) (0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ± 0.3V)

DESCRIPTION		-15		-20		-25			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle									
READ cycle time	^tRC	15		20		25		ns	
Address access time	^tAA		15		20		25	ns	
Chip Enable access time	^tACE		15		20		25	ns	
Output hold from address change	^tOH	4		5		5		ns	
Chip Enable to output in Low-Z	^tLZCE	5		5		5		ns	7
Chip disable to output in High-Z	^tHZCE		6		8		8	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		ns	
Chip disable to power-down time	^tPD		15		20		25	ns	
Output Enable access time	^tAOE		8		10		12	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		ns	
Output disable to output in High-Z	^tHZOE		6		8		8	ns	6
WRITE Cycle									
WRITE cycle time	^tWC	15		20		25		ns	
Chip Enable to end of write	^tCW	12		13		15		ns	
Address valid to end of write	^tAW	9		12		14		ns	
Address setup time	^tAS	0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		ns	
WRITE pulse width	$^tWP1$	9		10		12		ns	
WRITE pulse width	$^tWP2$	9		10		12		ns	
Data setup time	^tDS	8		10		10		ns	
Data hold time	^tDH	0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	1		1		1		ns	7
Write Enable to output in High-Z	^tHZWE		6		8		8	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

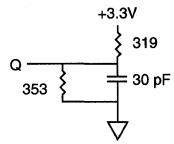


Fig. 1 OUTPUT LOAD EQUIVALENT

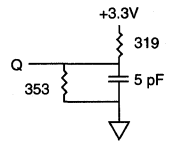


Fig. 2 OUTPUT LOAD EQUIVALENT

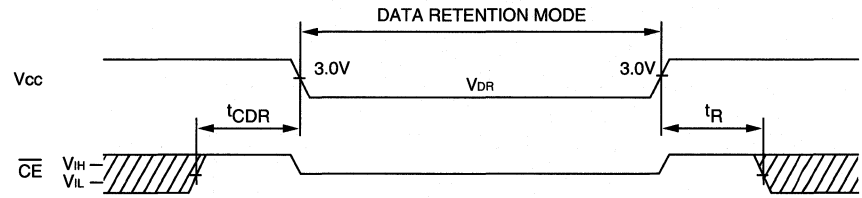
NOTES

1. All voltages referenced to Vss (GND).
2. Overshoot: $V_{IH} \leq +6.0V$ for $t \leq {}^tRC/2$
   Undershoot: $V_{IL} \geq -2.0V$ for $t \leq {}^tRC/2$
   Power-up: $V_{IH} \leq +6.0V$ and $V_{CC} \leq 3.1V$ for $t \leq 200msec$.
3. I_{CC} is dependent on output loading and cycle rates. The specified value applies with the outputs unloaded, and $f = \frac{1}{{}^tRC\ (MIN)}$ Hz.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ${}^tHZCE$, ${}^tHZOE$ and ${}^tHZWE$ are specified with CL = 5pF as in Fig. 2. Transition is measured ±200mV from steady state voltage.
7. At any given temperature and voltage condition, ${}^tHZCE$ is less than ${}^tLZCE$, and ${}^tHZWE$ is less than ${}^tLZWE$.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. Chip enable and output enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ${}^tRC$ = read cycle time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. The output will be in the High-Z state if output enable is high.
14. Contact Micron for IT/AT/XT timing and current specifications; they may differ from the commercial temperature range specifications shown in this data sheet.
15. Typical currents are measured at 25°C.

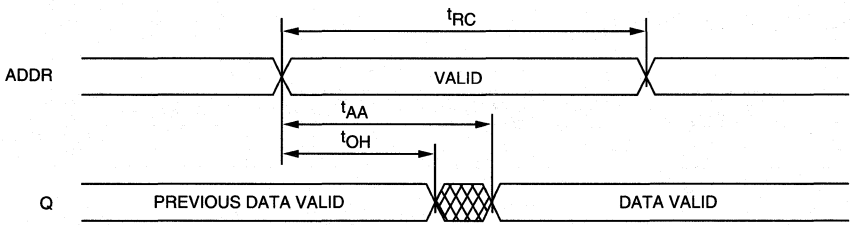
DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP versions only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V_{CC} for Retention Data			V_{DR}	2			V	
Data Retention Current L version LP version	$\overline{CE} \geq (V_{CC} -0.2V)$ $V_{IN} \geq (V_{CC} -0.2V)$ or $\leq 0.2V$	V_{CC} = 2V	I_{CCDR}		TBD	TBD	µA	15
Chip Deselect to Data Retention Time			${}^tCDR$	0			ns	4
Operation Recovery Time			${}^tR$	${}^tRC$			ns	4, 11

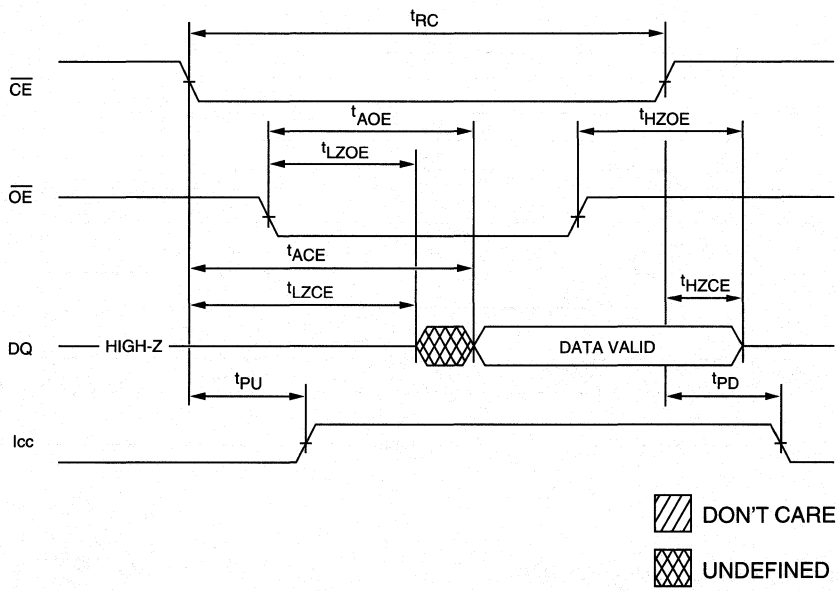
LOW Vcc DATA RETENTION WAVEFORM



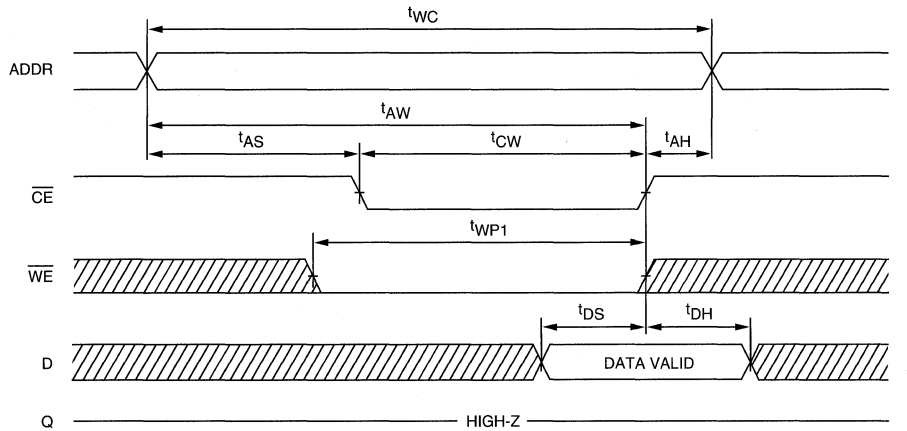
READ CYCLE NO. 1 [8, 9]



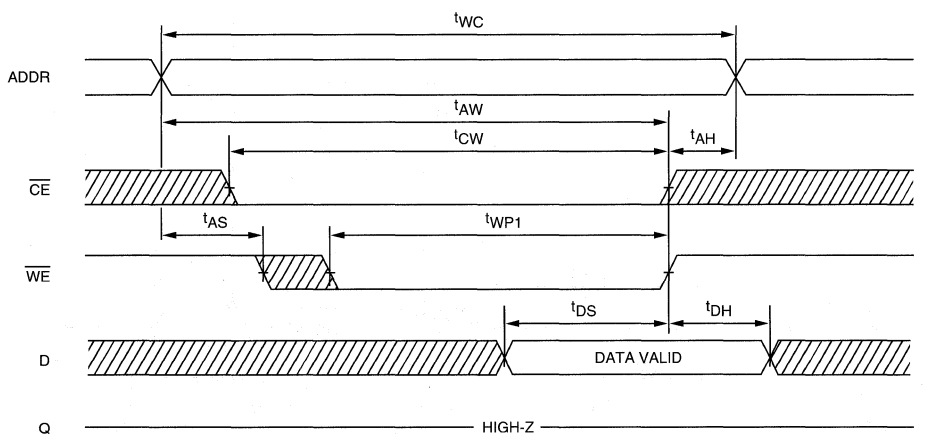
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)



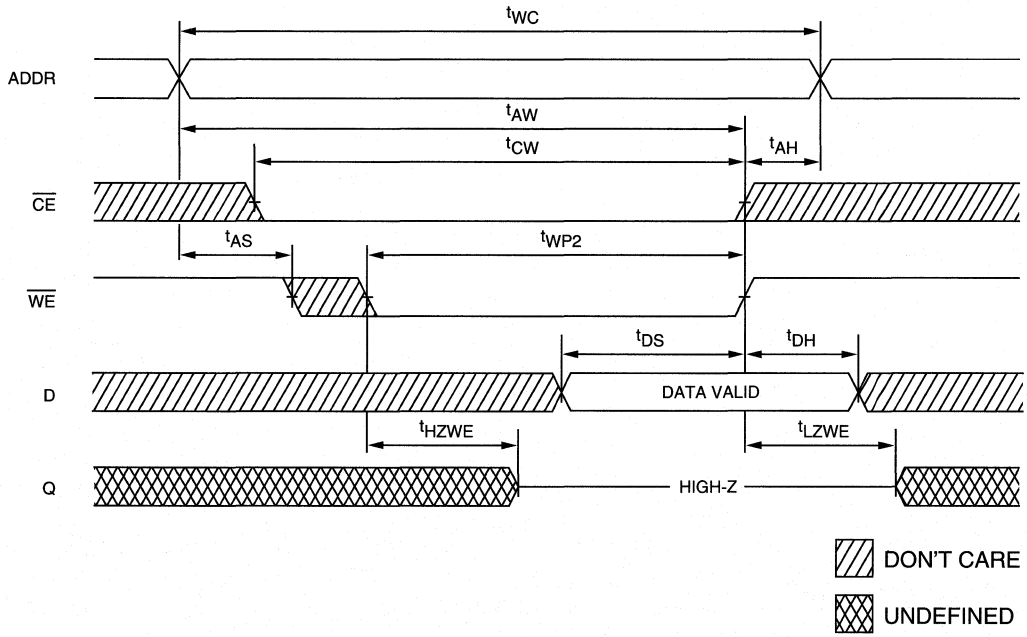
WRITE CYCLE NO. 2 [12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

WRITE CYCLE NO. 3 [7, 12, 13]

(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is active (LOW).

MICRON SEMICONDUCTOR, INC.

MT5LC128K8D4
REVOLUTIONARY PINOUT 128K x 8 SRAM

SRAM

512K x 8 SRAM

3.3V OPERATION WITH OUTPUT ENABLE, REVOLUTIONARY PINOUT

FEATURES

- All I/O pins are 5V tolerant
- High speed: 12, 15, 20, 25 and 35ns
- High-performance, low-power, CMOS double-metal process
- Multiple center power and ground pins for improved noise immunity
- Single +3.3V ±0.3V power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- All inputs and outputs are TTL-compatible
- Fast $\overline{OE}$ access time: 6, 8, 10, 12 and 15ns
- Complies to JEDEC low-voltage TTL standards

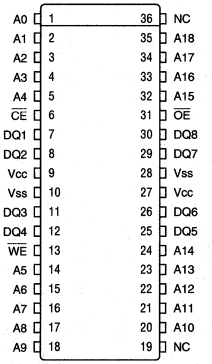
OPTIONS — MARKING

- Timing
  - 12ns access — -12
  - 15ns access — -15
  - 20ns access — -20
  - 25ns access — -25
  - 35ns access — -35
- Packages
  - Plastic SOJ (400 mil) — DJ
  - Plastic TSOP (400 mil) — TG
- 2V data retention — L
- Low power — P
- Temperature
  - Commercial (0°C to +70°C) — None
  - Industrial (-40°C to +85°C) — IT
  - Automotive (-40°C to +125°C) — AT
  - Extended (-55°C to +125°C) — XT
- Part number example: MT5LC512K8D4DJ-20 P

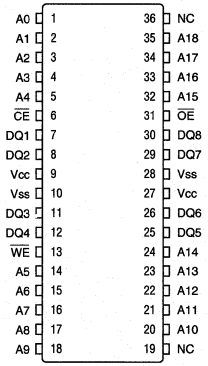
NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

36-Pin SOJ (SD-6)



36-Pin TSOP (SE-2)



GENERAL DESCRIPTION

The MT5LC512K8D4 is organized as a 524,288 x 8 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron 4 Meg SRAMs are fabricated using double-layer metal, triple-layer poly-silicon technology.

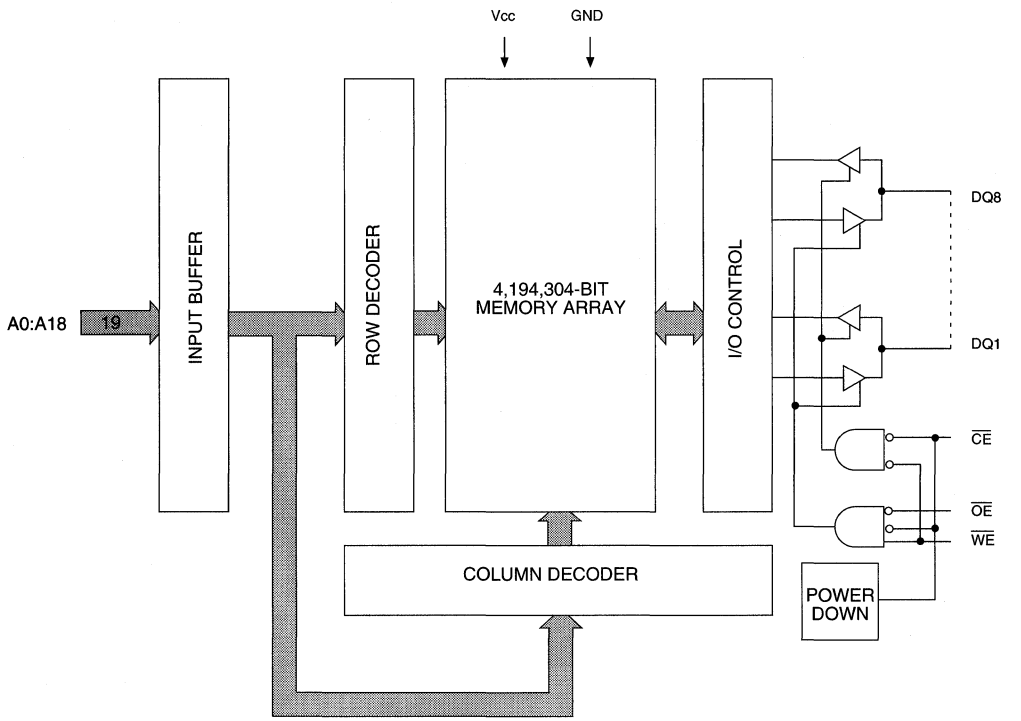
For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) capability. These enhancements can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

The "P" version also provides a 90 percent reduction in TTL standby current (I_{SB1}) through the use of gated inputs, which also facilitate the design of battery-backed systems. That is, the gated inputs simplify the design effort and circuitry required to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

All devices operate from a single +3.3V power supply and all inputs and outputs are fully TTL-compatible and 5V tolerant. These low-voltage parts are ideal for mixed 3.3V and 5V systems.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

THERMAL IMPEDENCE (EST)[16]

PACKAGE	NUMBER OF PINS	POWER DISSIPATION (watts)	θ_{JC}* (°C/W)	θ_{JA}* (°C/W)
SOJ	36	1.0	15	55
TSOP	36	1.0	5	65

*The thermal impedence numbers assume the device is socketted on a PC board and air flow is zero.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -0.5V to +4.6V
V_{IN} ..... -0.5 to +6.0V
Storage Temperature (plastic) ..... -55°C to +150°C
Short Circuit Output Current 50mA
Junction Temperature** ..... +150°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Maximum junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow. See technical note TN-05-14 for more information.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ±0.3V)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	5.5	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ Vcc	I_{LI}	-1	1	µA	
Output Leakage Current	Output(s) disabled 0V ≤ V_{OUT} ≤ Vcc	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		Vcc	3.0	3.6	V	1

				MAX						
DESCRIPTION	CONDITIONS	SYMBOL	VER	-12	-15	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; Vcc = MAX outputs open f = MAX = 1/t_{RC}	Icc		185	165	160	155	145	mA	3
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; Vcc = MAX outputs open f = MAX = 1/t_{RC}	I_{SB1}	STD	35	30	25	25	20	mA	
			P	1.0	1.0	1.0	1.0	1.0	mA	
	$\overline{CE}$ ≥ Vcc - 0.2V; Vcc = MAX V_{IN} ≥ Vcc - 0.2V or V_{IN} ≤ V_{SS} + 0.2V; f = 0	I_{SB2}	STD	1.0	1.0	1.0	1.0	1.0	mA	
			P	1.0	1.0	1.0	1.0	1.0	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	5	pF	4
Output Capacitance	Vcc = 3.3V	C_O	7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 5, 13) (0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ±0.3V)

DESCRIPTION		-12		-15		-20		-25		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle													
READ cycle time	^tRC	12		15		20		25		35		ns	
Address access time	^tAA		12		15		20		25		35	ns	
Chip Enable access time	^tACE		12		15		20		25		35	ns	
Output hold from address change	^tOH	3		3		3		3		3		ns	
Chip Enable to output in Low-Z	^tLZCE	3		3		5		5		5		ns	7
Chip disable to output in High-Z	^tHZCE		6		7		8		10		15	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		0		ns	
Chip disable to power-down time	^tPD		12		15		20		25		35	ns	
Output Enable access time	^tAOE		6		8		10		12		15	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		0		ns	
Output disable to output in High-Z	^tHZOE		5		6		7		10		12	ns	6
WRITE Cycle													
WRITE cycle time	^tWC	12		15		20		25		35		ns	
Chip Enable to end of write	^tCW	8		10		12		15		20		ns	
Address valid to end of write	^tAW	8		10		12		15		20		ns	
Address setup time	^tAS	0		0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		0		ns	
WRITE pulse width	$^tWP1$	8		9		12		15		20		ns	
WRITE pulse width	$^tWP2$	9		11		14		17		22		ns	
Data setup time	^tDS	6		7		8		10		15		ns	
Data hold time	^tDH	0		0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	3		3		5		5		5		ns	7
Write Enable to output in High-Z	^tHZWE		5		6		8		10		15	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

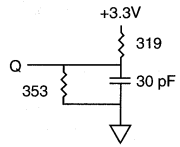


Fig. 1 OUTPUT LOAD EQUIVALENT

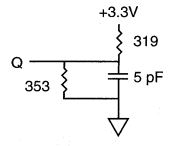


Fig. 2 OUTPUT LOAD EQUIVALENT

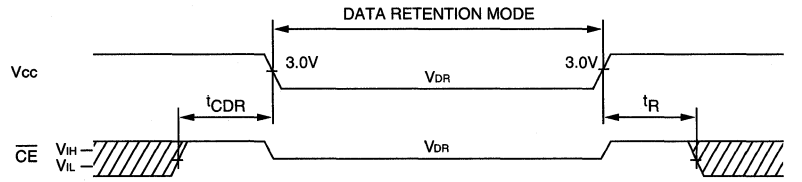
NOTES

1. All voltages referenced to Vss (GND).
2. Overshoot: $V_{IH} \leq +6.0V$ for $t \leq {}^tRC/2$
   Undershoot: $V_{IL} \geq -2.0V$ for $t \leq {}^tRC/2$
   Power-up: $V_{IH} \leq +6.0V$ and $V_{CC} \leq 3.1V$ for $t \leq 200msec$.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ${}^tHZCE$, ${}^tHZOE$ and ${}^tHZWE$ are specified with CL = 5pF as in Fig. 2. Transition is measured ±200mV from steady state voltage.
7. At any given temperature and voltage condition, ${}^tHZCE$ is less than ${}^tLZCE$ and ${}^tHZWE$ is less than ${}^tLZWE$.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables and output enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ${}^tRC$ = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Contact Micron for IT/AT/XT timing and current specifications; they may differ from the commercial temperature range specifications shown in this data sheet.
14. Output enable ($\overline{OE}$) is inactive (HIGH).
15. Output enable ($\overline{OE}$) is active (LOW).
16. Micron does not warrant functionality nor reliability of any product in which the junction temperature exceeds 150°C. Care should be taken to limit power to acceptable levels.

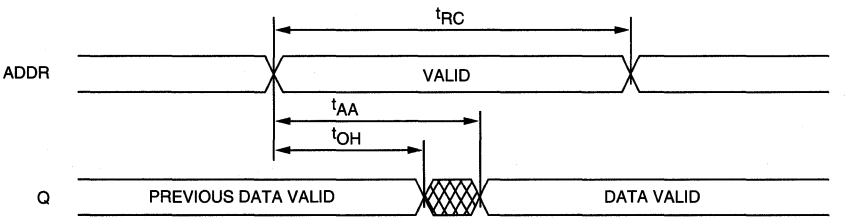
DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP versions only)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Vcc for Retention Data		VDR	2		V	
Data Retention Current L version	$\overline{CE} \geq$ (Vcc -0.2V) $V_{IN} \geq$ (Vcc -0.2V) or ≤ 0.2V Vcc = 2V	ICCDR		700	µA	
Data Retention Current LP version	$\overline{CE} \geq$ (Vcc -0.2V) Vcc = 2V	ICCDR		700	µA	
Chip Deselect to Data Retention Time		${}^tCDR$	0		ns	4
Operation Recovery Time		${}^tR$	${}^tRC$		ns	4, 11

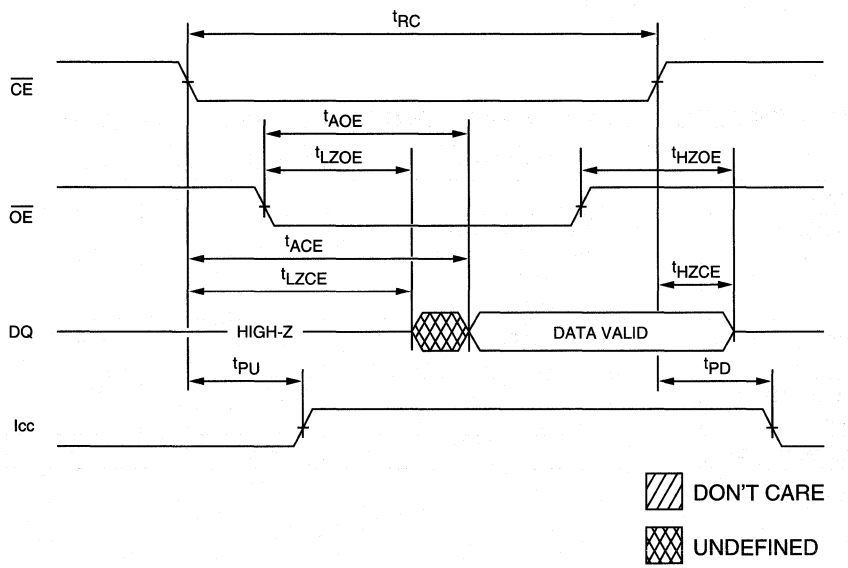
LOW Vcc DATA RETENTION WAVEFORM



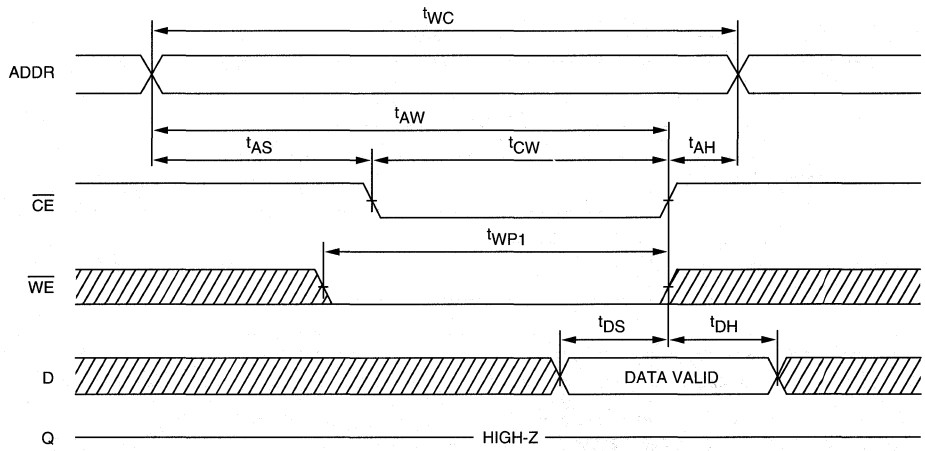
READ CYCLE NO. 1 [8, 9]



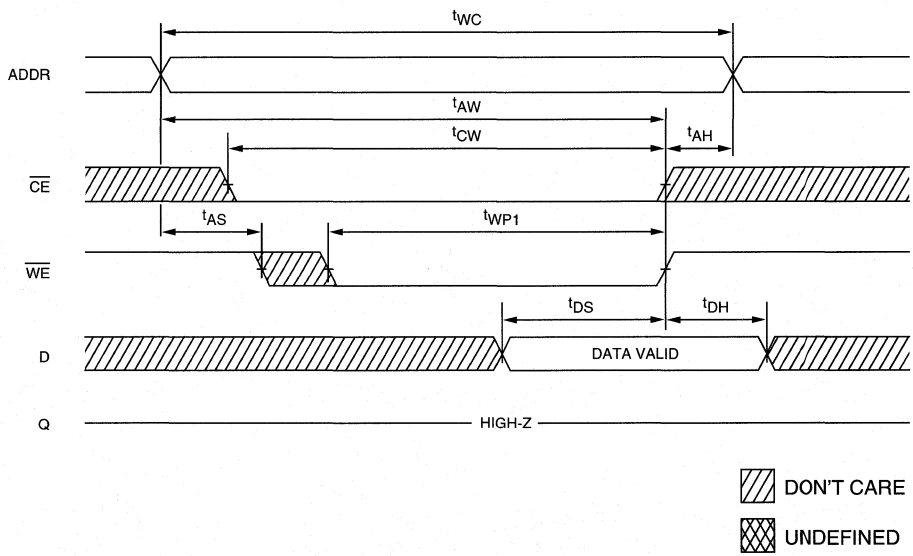
READ CYCLE NO. 2 [7, 8, 10]



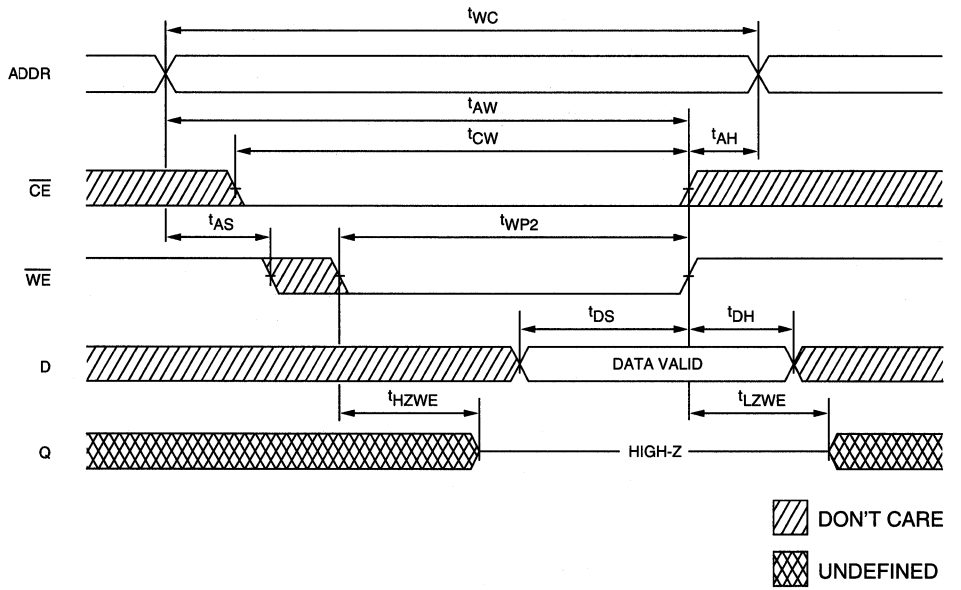
WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)



WRITE CYCLE NO. 2 [12, 14]
(Write Enable Controlled)



WRITE CYCLE NO. 3 [7, 12, 15]
(Write Enable Controlled)



MICRON SEMICONDUCTOR, INC.

MT5LC64K16D4
REVOLUTIONARY PINOUT 64K x 16 SRAM

SRAM

64K x 16 SRAM

3.3V OPERATION WITH OUTPUT ENABLE, REVOLUTIONARY PINOUT

FEATURES

- All I/O pins are 5V tolerant
- Fast access times: 15, 20 and 25ns
- High-performance, low-power, CMOS double-metal process
- Multiple center power and ground pins for improved noise immunity
- Single +3.3V ±0.3Vpower supply
- Individual byte controls for both READ and WRITE cycles
- All inputs and outputs are TTL-compatible
- Fast $\overline{OE}$ access time: 10 and 12ns
- Complies to JEDEC low-voltage TTL standards

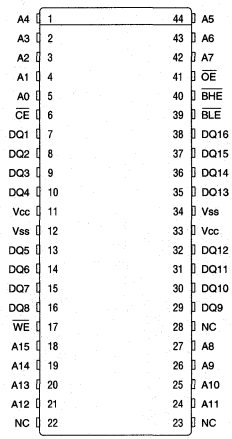
OPTIONS MARKING

- Timing
  - 15ns access -15
  - 20ns access -20
  - 25ns access -25
- Packages
  - 44-pin SOJ (400 mil) DJ
  - 44-pin TSOP (400 mil) TG
- 2V data retention L
- Temperature
  - Commercial (0°C to +70°C) None
  - Industrial (-40°C to +85°C) IT
  - Automotive (-40°C to +125°C) AT
  - Extended (-55°C to +125°C) XT
- Part Number Example: MT5LC64K16D4DJ-20

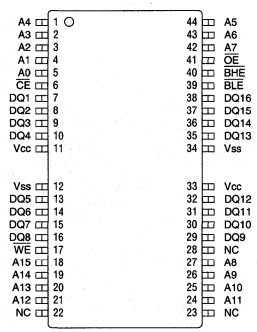
NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

44-Pin SOJ (SD-7)



44-Pin TSOP (SE-3)



GENERAL DESCRIPTION

The MT5LC64K16D4 is organized as a 65,536 x 16 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

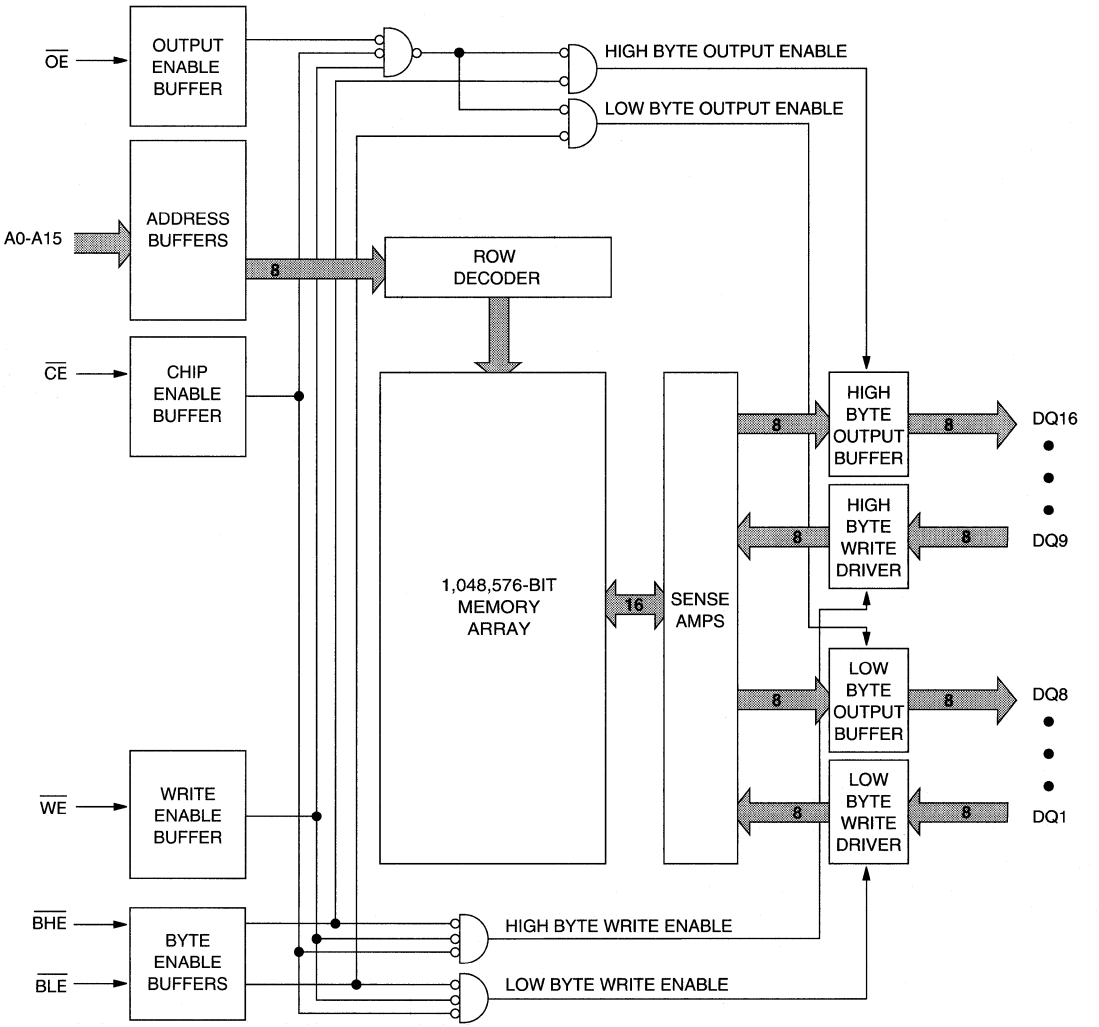
The MT5LC64K16D4 SRAM integrates a 64K x 16 SRAM core with peripheral circuitry consisting of active LOW chip enable, separate upper and lower byte enables and a fast output enable.

Separate byte enable controls ($\overline{BLE}$ and $\overline{BHE}$) allow individual bytes to be written and read. $\overline{BLE}$ controls DQ1-DQ8, the lower bits. $\overline{BHE}$ controls DQ9-DQ16, the upper bits.

The MT5LC64K16D4 operates from a single +3.3V power supply and all inputs and outputs are fully TTL-compatible and 5V tolerant. These low-voltage parts are ideal for mixed 3.3V and 5V systems.

3.3 VOLT SRAM

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

SOJ and TSOP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
5, 4, 3, 2, 1, 44, 43, 42, 27, 26, 25, 24, 21, 20, 19, 18	A0-A15	Input	Address Inputs: These inputs determine which cell is accessed.
17	$\overline{WE}$	Input	Write Enable: This input determines if the cycle is a READ or WRITE cycle. $\overline{WE}$ is LOW for a WRITE cycle and HIGH for a READ cycle
39, 40	$\overline{BLE}$, $\overline{BHE}$	Input	Byte Enables: These active LOW inputs allow individual bytes to be written or read. When $\overline{BLE}$ is LOW, data is written or read to the lower byte, DQ1-DQ8. When $\overline{BHE}$ is LOW, data is written or read to the upper byte, DQ9-DQ16.
6	$\overline{CE}$	Input	Chip Enable: This signal is used to enable the device. When $\overline{CE}$ is HIGH, the chip automatically goes into standby power mode.
41	$\overline{OE}$	Input	Output Enable: This active LOW input enables the output drivers.
22, 23, 28	NC	-	No Connect: These signals are not internally connected.
7, 8, 9, 10, 13, 14, 15, 16, 29, 30, 31, 32, 35, 36, 37, 38	DQ1-DQ16	Input/ Output	SRAM Data I/O: Lower byte is DQ1-DQ8; Upper byte is DQ9-DQ16.
11, 33	Vcc	Supply	Power Supply: +3.3V ±0.3V
12, 34	Vss	Supply	Ground: GND

TRUTH TABLE

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	DQ1-DQ8	DQ9-DQ16	POWER
STANDBY	H	X	X	X	X	HIGH-Z	HIGH-Z	STANDBY
LOW BYTE READ (DQ1-DQ8)	L	L	H	L	H	D	HIGH-Z	ACTIVE
HIGH BYTE READ (DQ9-DQ16)	L	L	H	H	L	HIGH-Z	D	ACTIVE
WORD READ (DQ1-DQ16)	L	L	H	L	L	D	D	ACTIVE
WORD WRITE (DQ1-DQ16)	L	X	L	L	L	Q	Q	ACTIVE
LOW BYTE WRITE (DQ1-DQ8)	L	X	L	L	H	Q	HIGH-Z	ACTIVE
HIGH BYTE WRITE (DQ9-DQ16)	L	X	L	H	L	HIGH-Z	Q	ACTIVE
OUTPUT DISABLE	L	H	H	X	X	HIGH-Z	HIGH-Z	ACTIVE
	L	X	X	H	H	HIGH-Z	HIGH-Z	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -0.5V to 4.6V
V_{IN} ..... -0.5V to +6.0V
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; $V_{CC} = 3.3V \pm 0.3V$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.0	5.5	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-1	1	µA	
Output Leakage Current	Output(s) disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	3.0	3.6	v	

				MAX				
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-15	-20	-25	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	60	100	88	80	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	10	20	16	14	mA	
	$\overline{CE} \ge V_{CC}$ -0.2V; V_{CC} = MAX $V_{IN} \le V_{SS}$ +0.2V or $V_{IN} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	0.5	5	5	5	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1MHz	C_I	6	pF	4
Input/Output Capacitance (D/Q)	V_{CC} = 3.3V	$C_{I/O}$	6	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 14) (0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ± 0.3V)

DESCRIPTION		-15		-20		-25			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle									
READ cycle time	^tRC	15		20		25		ns	
Address access time	^tAA		15		20		25	ns	
Chip Enable access time	^tA		15		20		25	ns	
Output hold from address change	^tOH	4		5		5		ns	
Chip Enable to output in Low-Z	^tLZCE	5		5		5		ns	6, 7
Chip disable to output in High-Z	^tHZCE		6		8		8	ns	6, 7
Output Enable access time	^tAOE		8		10		12	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		ns	6, 7
Output disable to output in High-Z	^tHZOE		6		8		8	ns	6, 7
Byte Enable access time	^tABE		8		10		12	ns	
Byte Enable to output in Low-Z	^tLZBE	0		0		0		ns	6, 7
Byte disable to output in High-Z	^tHZBE		6		8		8	ns	6, 7
WRITE Cycle									
WRITE cycle time	^tWC	15		20		25		ns	
Chip Enable to end of write	^tCW	12		13		15		ns	
Address valid to end of write	^tAW	9		12		14		ns	
Address setup time	^tAS	0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		ns	
Write pulse width	^tWP	9		10		12		ns	
Data setup time	^tDS	8		10		10		ns	
Data hold time	^tDH	0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	1		1		1		ns	6, 7
Write Enable to output in High-Z	^tHZWE		6		8		8	ns	6, 7
Byte Enable to end of write	^tBW	9		12		14		ns	

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

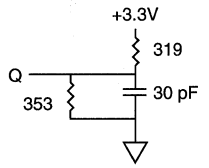


Fig. 1 OUTPUT LOAD EQUIVALENT

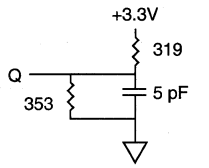


Fig. 2 OUTPUT LOAD EQUIVALENT

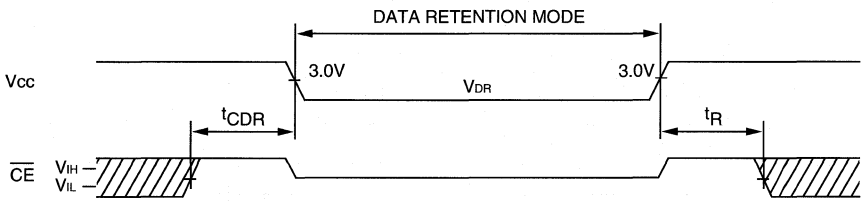
NOTES

1. All voltages referenced to Vss (GND).
2. Overshoot: $V_{IH} \leq +6.0V$ for $t \leq {}^tRC/2$
   Undershoot: $V_{IL} \geq -2.0V$ for $t \leq {}^tRC/2$
   Power-up: $V_{IH} \leq +6.0V$ and $V_{CC} \leq 3.1V$ for $t \leq 200msec$.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. Output loading is specified with CL = 5pF as in Fig. 2. Transition is measured ±200mV from steady state voltage.
7. At any given temperature and voltage condition, ${}^tHZCE$ is less than ${}^tLZCE$, ${}^tHZOE$ is less than ${}^tLZOE$, and ${}^tHZBE$ is less than ${}^tLZBE$.
8. Any combination of write enable, chip enable and byte enable can initiate and terminate a WRITE cycle.
9. $\overline{WE}$ is HIGH for READ cycle.
10. Device is continuously selected. Chip enable is held in its active state.
11. Address valid prior to, or coincident with, the latest occurring chip enable.
12. $\overline{BHE}$ and $\overline{BLE}$ are held in their active state (LOW).
13. The output will be in the High-Z state if output enable is HIGH.
14. Contact Micron for IT/AT/XT timing and current specifications; they may differ from the commercial temperature range specifications shown in this data sheet.
15. Typical currents are measured at 25°C.

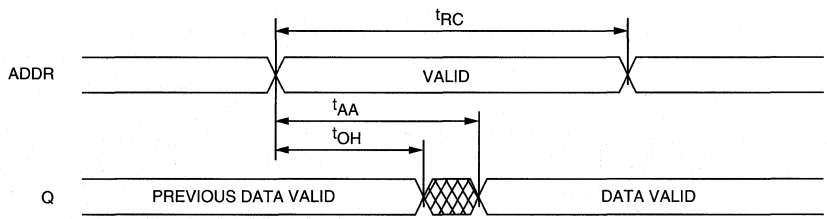
DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP versions only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V_{CC} for Retention Data			V_{DR}	2			V	
Data Retention Current L version LP version	$\overline{CE} \geq (V_{CC} -0.2V)$ $V_{IN} \geq (V_{CC} -0.2V)$ or $\leq 0.2V$	V_{CC} = 2V	I_{CCDR}		TBD	TBD	µA	15
Chip Deselect to Data Retention Time			${}^tCDR$	0			ns	4
Operation Recovery Time			${}^tR$	${}^tRC$			ns	4, 11

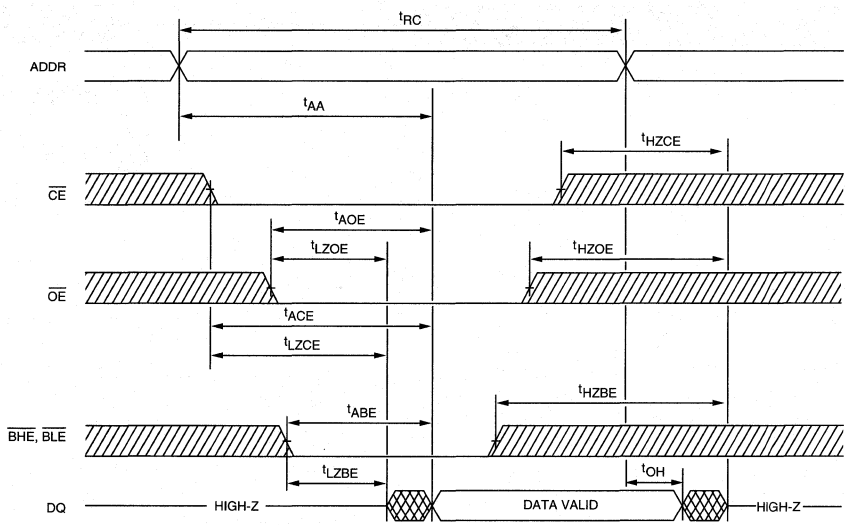
LOW Vcc DATA RETENTION WAVEFORM



READ CYCLE NO. 1 [9, 10, 12]



READ CYCLE NO. 2 [7, 9]

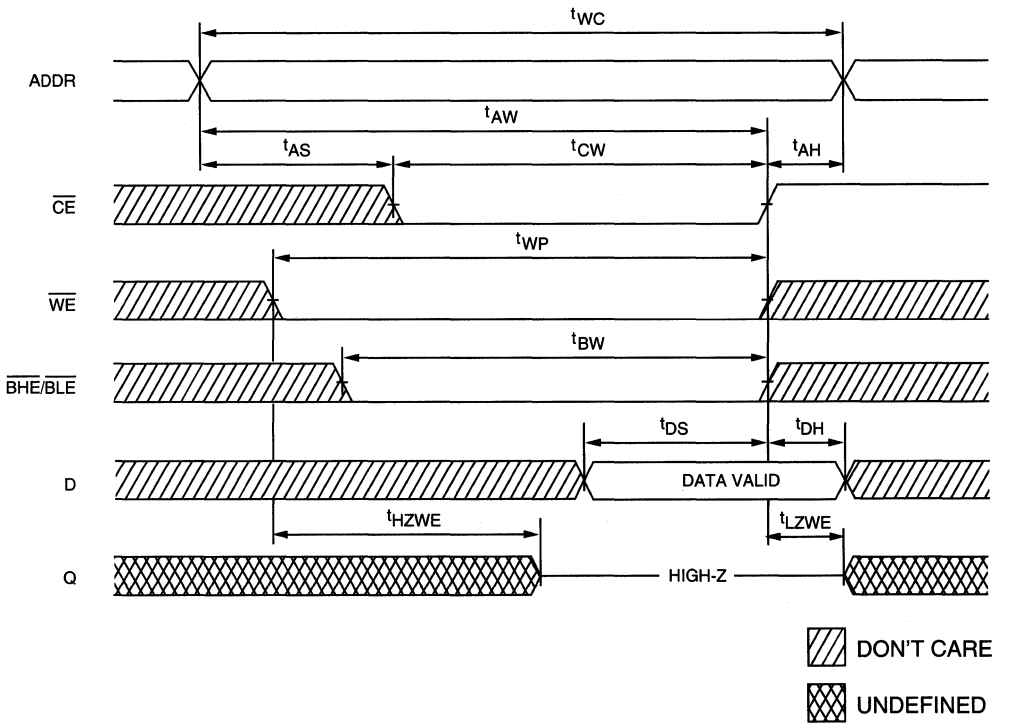


DON'T CARE

UNDEFINED

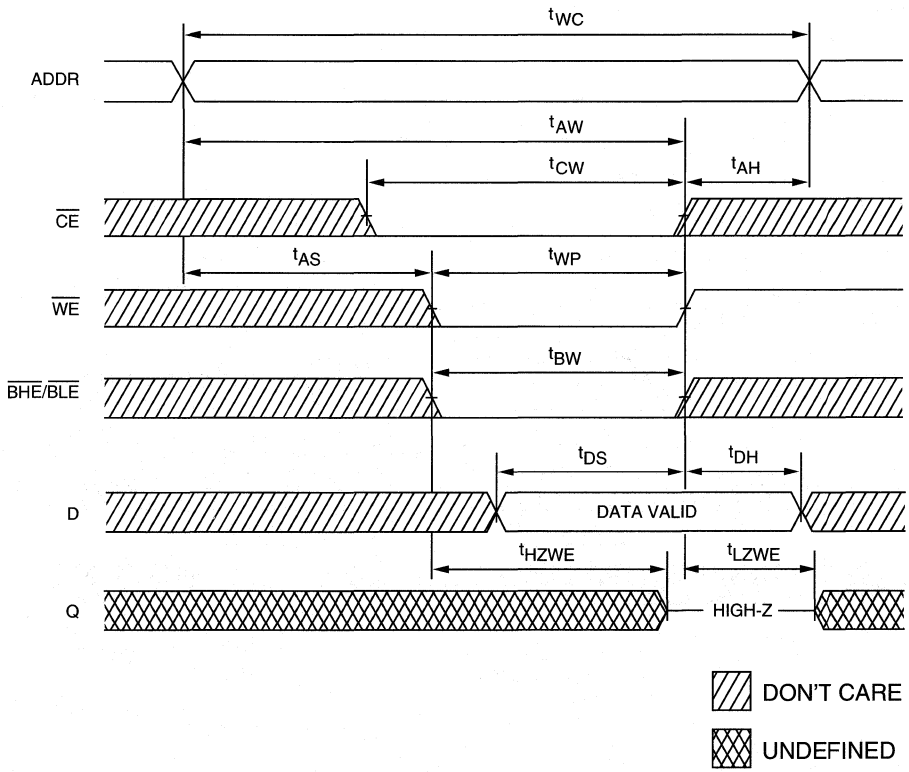
WRITE CYCLE NO. 1 [8, 13]

Chip Enable Controlled



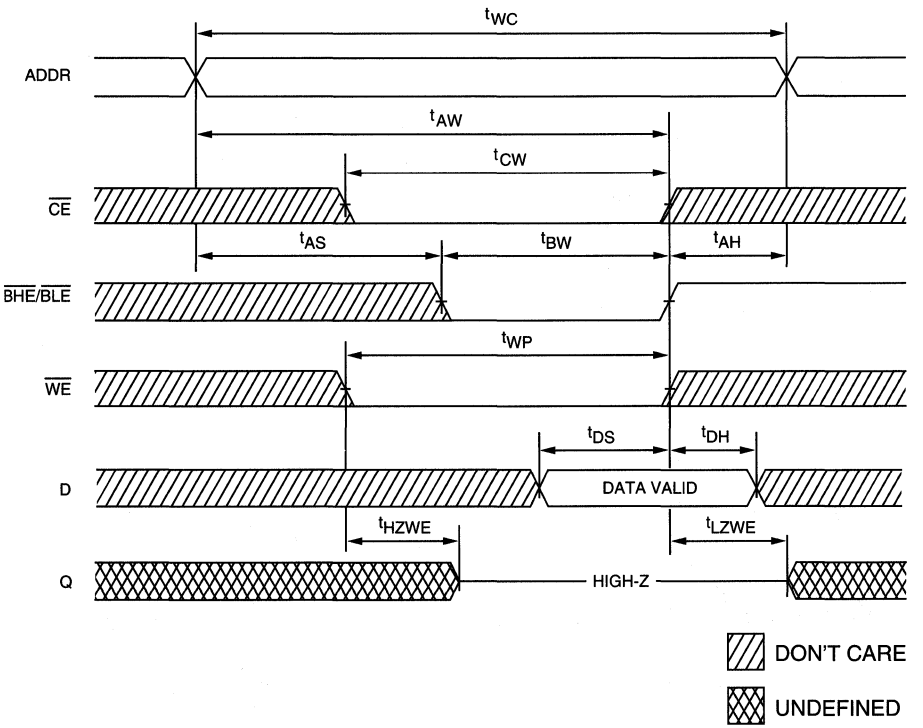
WRITE CYCLE NO. 2 [8, 13]

Write Enable Controlled



WRITE CYCLE NO. 3 [8, 13]

Byte Enable Controlled



SRAM

256K x 16 SRAM

3.3V OPERATION WITH OUTPUT ENABLE

FEATURES

- All I/O pins are 5V tolerant
- High speed: 12, 15, 20, 25 and 35ns
- Multiple center power and ground pins for improved noise immunity
- Single +3.3V ±0.3V power supply
- Easy memory expansion with chip enable($\overline{CE}$) and output enable ($\overline{OE}$) options
- All inputs and outputs are TTL-compatible
- Fast $\overline{OE}$ access time: 6, 8, 10, 12, and 15ns
- High-performance, low-power, CMOS double-metal process
- Complies to JEDEC low-voltage TTL standards

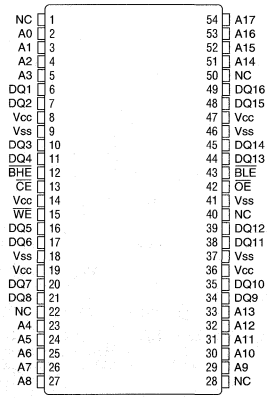
OPTIONS — MARKING

- Timing
  - 12ns access — -12
  - 15ns access — -15
  - 20ns access — -20
  - 25ns access — -25
  - 35ns access — -35
- Packages
  - Plastic SOJ (400 mil) — DJ
  - Plastic TSOP (400 mil) — TG
- 2V data retention — L
- Low power — P
- Temperature
  - Commercial (0°C to +70°C) — None
  - Industrial (-40°C to +85°C) — IT
  - Automotive (-40°C to +125°C) — AT
  - Extended (-55°C to +125°C) — XT
- Part number example: MT5LC256K16D4DJ-20 P

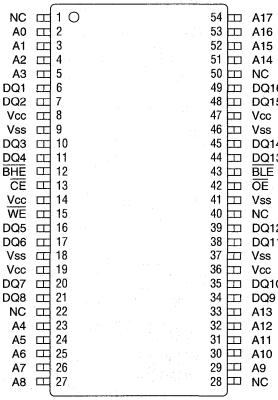
NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

54-Pin SOJ* (SD-8)



54-Pin TSOP* (SE-4)



* JEDEC-proposed pinout (0.8mm pitch)

GENERAL DESCRIPTION

The MT5LC256K16D4 is organized as a 262,144 x 16 using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron 4 Meg SRAMs are fabricated using a double-layer metal, triple-layer polysilicon technology.

This device offers multiple center power and ground pins for improved performance. For flexibility in high-speed memory applications, Micron offers $\overline{CE}$ and $\overline{OE}$ capabilities. These enhancements can place the outputs in High-Z for additional flexibility in system design.

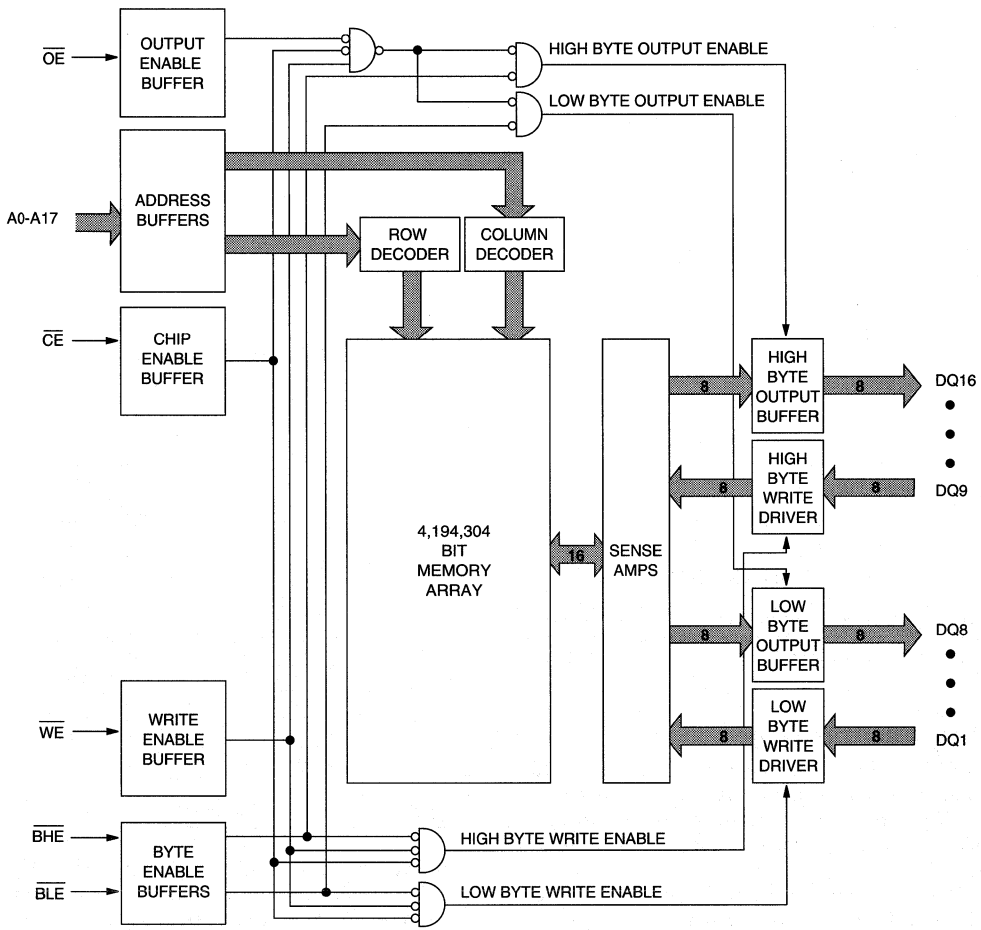
Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW and the appropriate byte enables ($\overline{BHE}$ and $\overline{BLE}$) are in their proper states. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ and $\overline{OE}$ go LOW and the appropriate byte enables ($\overline{BHE}$ and $\overline{BLE}$) are in their proper states. The device offers a reduced-power standby mode when disabled. This allows system designers to meet low standby power requirements.

Separate byte enable controls ($\overline{BLE}$ and $\overline{BHE}$) allow individual bytes to be written and read. $\overline{BLE}$ controls the lower bits (DQ1-DQ8). $\overline{BHE}$ controls the upper bits (DQ9-DQ16).

The LP version also provides a 90 percent reduction in TTL standby current (I_{SB1}). This is achieved by including gated inputs on the design. The gated inputs also facilitate the design of battery-backed systems where the designer needs to protect against inadvertent battery current drain during power-down when inputs may be at undefined levels.

All devices operate from a single +3.3V power supply and all inputs and outputs are fully TTL-compatible and 5V tolerant. These low-voltage parts are ideal for mixed 3.3V and 5V systems.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

SOJ and TSOP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
2-5, 23-27, 29-33 51-54	A0-A17	Input	Address Inputs: These inputs determine which cell is accessed.
15	$\overline{WE}$	Input	Write Enable: This input determines if the cycle is a READ or WRITE cycle. $\overline{WE}$ is LOW for a WRITE cycle and HIGH for a READ cycle
12, 43	$\overline{BHE}$, $\overline{BLE}$	Input	Byte Enables: These active LOW inputs allow individual bytes to be written or read. When $\overline{BLE}$ is LOW, data is written to or read from the lower byte, D1-D8. When $\overline{BHE}$ is LOW, data is written to or read from the upper byte, D9-D16.
13	$\overline{CE}$	Input	Chip Enable: This signal is used to enable the device. When $\overline{CE}$ is HIGH, the chip goes into standby power mode.
42	$\overline{OE}$	Input	Output Enable: This active LOW input enables the output drivers.
1, 22, 28, 40, 50	NC	-	No Connect: These signals are not internally connected.
6, 7, 10, 11, 16, 17, 20, 21, 34, 35, 38, 39, 44, 45, 48, 49	DQ1-DQ16	Input/ Output	SRAM Data I/O: Lower byte is DQ1-DQ8; upper byte is DQ9-DQ16.
8, 14, 19, 36, 47	Vcc	Supply	Power Supply: +3.3V ±0.3V
9, 18, 37, 41, 46	Vss	Supply	Ground: GND

TRUTH TABLE

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	DQ1-DQ8	DQ9-DQ16	POWER
STANDBY	H	X	X	X	X	HIGH-Z	HIGH-Z	STANDBY
LOW BYTE READ (DQ1-DQ8)	L	L	H	L	H	D	HIGH-Z	ACTIVE
HIGH BYTE READ (DQ9-DQ16)	L	L	H	H	L	HIGH-Z	D	ACTIVE
WORD READ (DQ1-DQ16)	L	L	H	L	L	D	D	ACTIVE
WORD WRITE (DQ1-DQ16)	L	X	L	L	L	Q	Q	ACTIVE
LOW BYTE WRITE (DQ1-DQ8)	L	X	L	L	H	Q	HIGH-Z	ACTIVE
HIGH BYTE WRITE (DQ9-DQ16)	L	X	L	H	L	HIGH-Z	Q	ACTIVE
OUTPUT DISABLE	L	H	H	X	X	HIGH-Z	HIGH-Z	ACTIVE
	L	X	X	H	H	HIGH -Z	HIGH-Z	ACTIVE

THERMAL IMPEDENCE (EST)[18]

PACKAGE	NUMBER OF PINS	POWER DISSIPATION (watts)	θ_{JC}* (°C/W)	θ_{JA}* (°C/W)
SOJ	54	1.0	15	55
TSOP	54	1.0	5	65

*The thermal impedence numbers assume the device is socketted on a PC board and air flow is zero.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} .....-0.5V to +4.6V
V_{IN}.....-0.5 to +6.0V
Storage Temperature (plastic) .....-55°C to +150°C
Short Circuit Output Current 50mA
Junction Temperature** .....+150°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Maximum junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow. See the Application Information section at the end of this data sheet for more information.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; V_{CC} = 3.3V ±0.3V)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	5.5	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-1	1	µA	
Output Leakage Current	Output(s) disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	3.0	3.6	V	1

				MAX						
DESCRIPTION	CONDITIONS	SYMBOL	VER	-12	-15	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	ALL	185	165	160	155	145	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	STD	35	30	25	25	20	mA	
			P	1.0	1.0	1.0	1.0	1.0	mA	
	$\overline{CE} \ge V_{CC}$ -0.2V; V_{CC} = MAX $V_{IN} \le V_{SS}$ +0.2V or $V_{IN} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	STD	1.0	1.0	1.0	1.0	1.0	mA	
			P	1.0	1.0	1.0	1.0	1.0	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	5	pF	4
Output Capacitance	V_{CC} = 3.3V	C_O	7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 5, 15) ($0°C \le T_A \le 70°C$; V_{CC} = 3.3V ±0.3V)

DESCRIPTION		-12		-15		-20		-25		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle													
READ cycle time	tRC	12		15		20		25		35		ns	
Address access time	tAA		12		15		20		25		35	ns	
Chip Enable access time	tACE		12		15		20		25		35	ns	
Output hold from address change	tOH	3		3		3		3		3		ns	
Chip Enable to output in Low-Z	tLZCE	3		3		5		5		5		ns	7
Chip disable to output in High-Z	tHZCE		6		7		8		10		15	ns	6, 7
Chip Enable to power-up time	tPU	0		0		0		0		0		ns	
Chip disable to power-down time	tPD		12		15		20		25		35	ns	
Output Enable access time	tAOE		6		8		10		12		15	ns	
Output Enable to output in Low-Z	tLZOE	0		0		0		0		0		ns	
Output disable to output in High-Z	tHZOE		5		6		7		10		12	ns	6
Byte Enable access time	tABE		7		8		10		12		15	ns	
Byte Enable to output in Low-Z	tLZBE	0		0		0		0		0		ns	
Byte Enable to output in High-Z	tHZBE		7		8		8		8		10	ns	
WRITE Cycle													
WRITE cycle time	tWC	12		15		20		25		35		ns	
Chip Enable to end of WRITE	tCW	8		10		12		15		20		ns	
Address valid to end of WRITE	tAW	8		10		12		15		20		ns	
Address setup time	tAS	0		0		0		0		0		ns	
Address hold from end of WRITE	tAH	0		0		0		0		0		ns	
WRITE pulse width	tWP1	8		9		12		15		20		ns	
WRITE pulse width	tWP2	9		11		14		17		22		ns	
Data setup time	tDS	6		7		8		10		15		ns	
Data hold time	tDH	0		0		0		0		0		ns	
Write disable to output in Low-Z	tLZWE	3		3		5		5		5		ns	7
Write Enable to output in High-Z	tHZWE		5		6		8		10		15	ns	6, 7
Byte Enable to end of WRITE	tBW	8		9		12		14		18		ns	

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

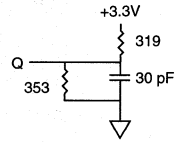


Fig. 1 OUTPUT LOAD EQUIVALENT

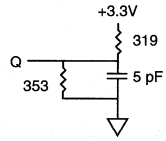


Fig. 2 OUTPUT LOAD EQUIVALENT

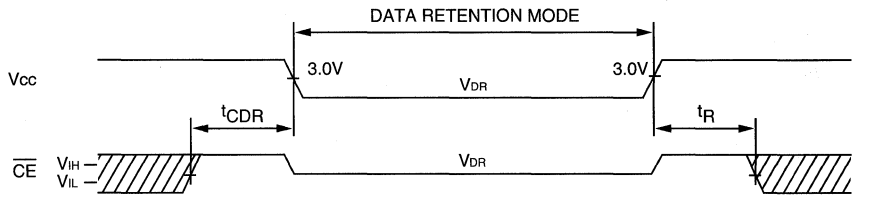
NOTES

1. All voltages referenced to Vss (GND).
2. Overshoot: $V_{IH} \leq +6.0V$ for $t \leq {}^tRC/2$
   Undershoot: $V_{IL} \geq -2.0V$ for $t \leq {}^tRC/2$
   Power-up: $V_{IH} \leq +6.0V$ and $V_{CC} \leq 3.1V$ for $t \leq 200msec$.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ${}^tHZCE$, ${}^tHZOE$, ${}^tHZBE$ and ${}^tHZWE$ are specified with CL = 5pF as in Fig. 2. Transition is measured ±200mV from steady state voltage.
7. At any given temperature and voltage condition, ${}^tHZCE$ is less than ${}^tLZCE$ and ${}^tHZWE$ is less than ${}^tLZWE$.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables and output enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ${}^tRC$ = READ cycle time.
12. Chip enable, write enable and byte enables can initiate and terminate a WRITE cycle.
13. $\overline{BLE}$ and $\overline{BLH}$ determine what outputs are active during the READ cycle.
14. The output will be in a High-Z state if $\overline{OE}$ is HIGH.
15. Contact Micron for IT/AT/XT timing and current specifications; they may differ from the commercial temperature range specifications shown in this data sheet.
16. Output enable ($\overline{OE}$) is inactive (HIGH).
17. Output enable ($\overline{OE}$) is active (LOW).
18. Micron does not warrant functionality nor reliability of any product in which the junction temperature exceeds 150°C. Care should be taken to limit power to acceptable levels.

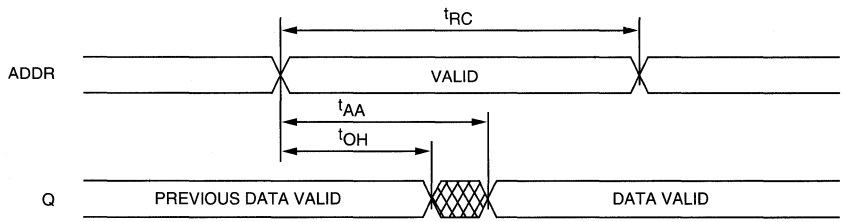
DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Vcc for Retention Data		V_{DR}	2		V	
Data Retention Current L version	$\overline{CE} \geq (Vcc - 0.2V)$ $V_{IN} \geq (Vcc - 0.2V)$ or ≤ 0.2V Vcc = 2V	I_{CCDR}		700	µA	
Data Retention Current LP version	$\overline{CE} \geq (Vcc - 0.2V)$ Vcc = 2V	I_{CCDR}		700	µA	
Chip Deselect to Data Retention Time		${}^tCDR$	0		ns	4
Operation Recovery Time		${}^tR$	${}^tRC$		ns	4, 11

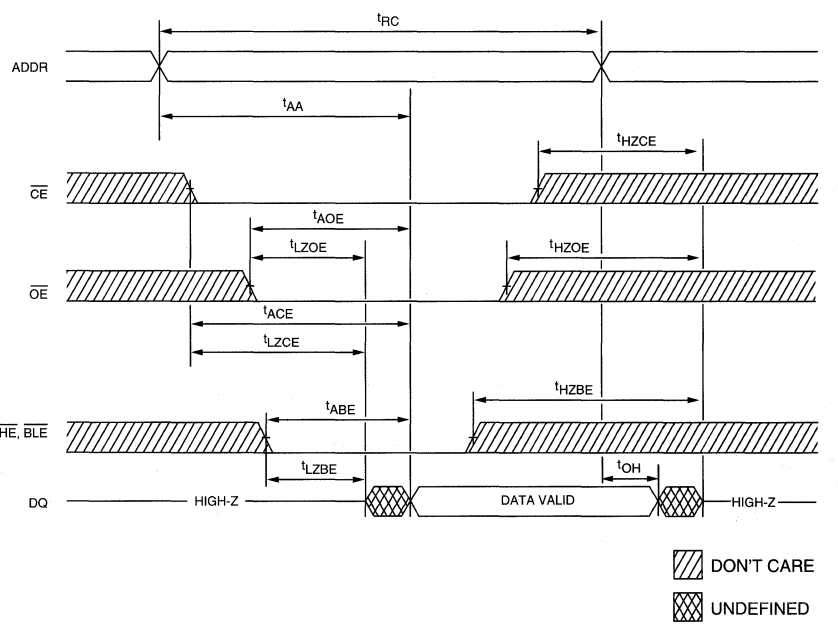
LOW Vcc DATA RETENTION WAVEFORM



READ CYCLE NO. 1 [8, 9, 13]

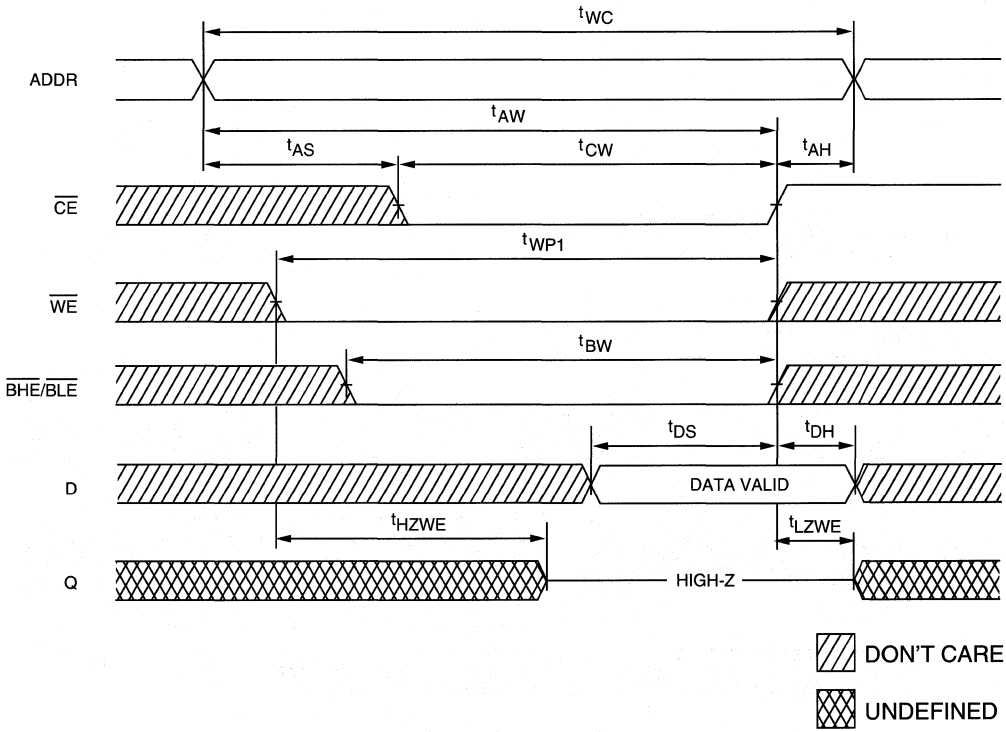


READ CYCLE NO. 2 [7, 8, 10]

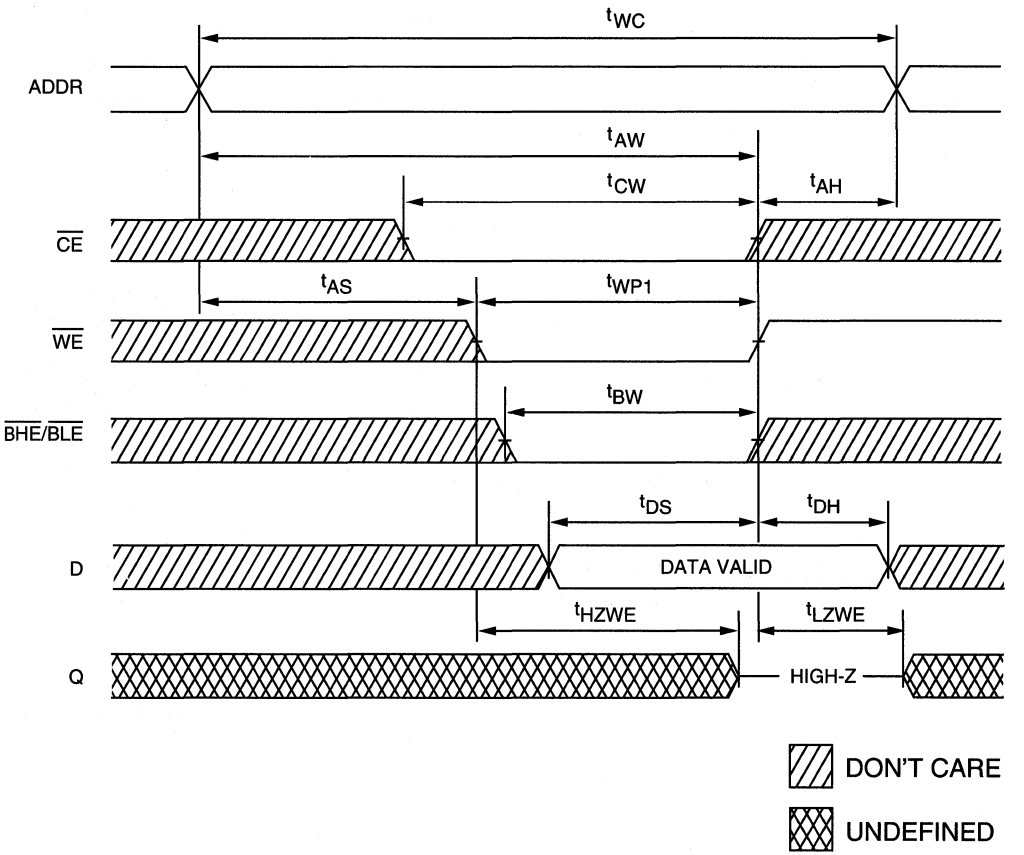


WRITE CYCLE NO. 1 [12,14]

(Chip Enable Controlled)

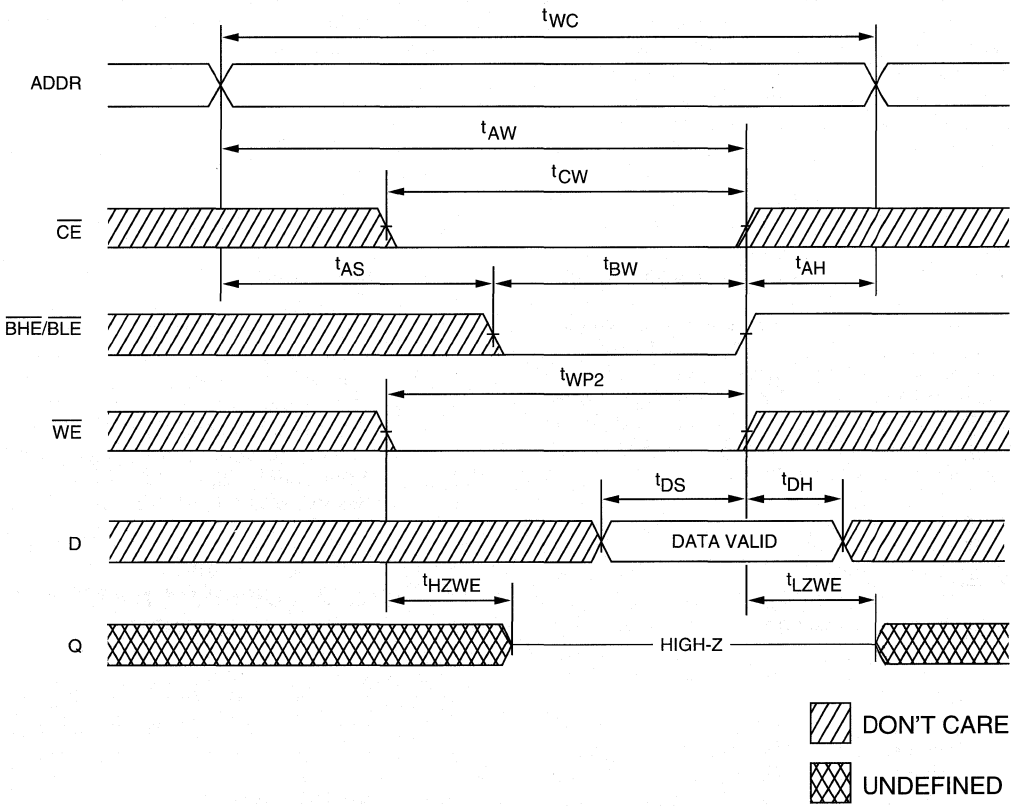


WRITE CYCLE NO. 2 [7, 12, 14, 16]
(Write Enable Controlled)



WRITE CYCLE NO. 3 [7, 12, 14, 17]

(Write Enable Controlled)



APPLICATION INFORMATION

THERMAL CONSIDERATIONS

This section describes how to determine the junction temperature during operating conditions. It is essential that the maximum junction temperature of the 4 Meg SRAM is not exceeded. If this temperature is exceeded it is necessary to add external cooling such as forced airflow or change the operating conditions. The maximum junction temperature for Micron SRAMs is 150°C. The limiting temperature factor is not the SRAM but the mold compound which prevents reliable operating temperatures significantly about 150°C. However, it is advisable to run the part as cool as possible since reliability (FIT rates) are exponentially dependent upon junction temperature.

The calculation of the actual junction temperature begins with the power calculation and then the junction temperation calculation. Equations 1 and 2 below show how T_j is determined using the ambient temperature, thermal resistance and operating power. If an airflow is introduced into a system then Equation 2 should be used with an airflow thermal multiplier. Specific thermal resistances are given in Micron technical note "SRAM Thermal Design Considerations" and in individual data sheets.

$$T_j = T_A + P * \theta_{JA} \quad (1)$$

$$T_j = T_A + P * \theta_{JA} * \theta_M \quad (2)$$

T_j = Junction temperature of the active portion of the silicon die (°C)
T_A = Ambient air temperature (°C) at which the device is operated
P = Average power dissipation of the device (W)
θ_{JA} = Junction to ambient thermal resistance (°C/W)
θ_M = Airflow multiplier. This value changes for different values of airflow over the part (fpm).

To solve the above equations the average operating power must be calculated. Total power has three separate components (P_1, P_2 and P_3). P_1 is the operating power dissipated by the chip, P_2 is the AC output power due to the capacitive load and P_3 is the DC output power due to TTL DC load current (P_3 is usually negligible). For this example we have chosen P_2 such that outputs are switching from a logic LOW state to a logic HIGH state which gives the worst case output AC current. A complete description of these equations and their derivation is given in Micron technical note "Design Tips: 32K x 36 SRAM."

$$P_1 = V_{CC} I_{CC}$$

$$P_2 = \frac{C_L}{T} (V_{CC} [V_{OH} - V_{OL}] - 0.5 [V_{OH}^2 - V_{OL}^2]) N_S$$

$$P_3 = (V_{CC} - V_{OH}) I_O N_H + V_{OL} I_I N_L.$$

V_{CC} = Supply voltage
I_{CC} = Supply current
C_L = Capacitive output loading
T = Clock period
V_{OH} = Output high voltage
V_{OL} = Output low voltage
I_O = Output current on DQ lines which are high
I_I = Input current on DQ lines which are low
N_H = Number of DQ lines which are high
N_L = Number of DQ lines which are low.

Table 1
EFFECTS OF AIRFLOW ON 4 MEG SRAM SOJ PACKAGES

Package	Air Flow	θ_M Multiplier
PSOJ	200 fpm	0.7 - 0.75
PSOJ	500 fpm	0.55 - 0.65

ADDITIONAL INFORMATION

For more information on thermal considerations see Micron's technical notes, "SRAM Thermal Design Considerations" and "Design Tips: 32K x 36 SRAM." These notes explain how to calculate thermal resistance and how to improve thermal performance in much greater detail. Also available is Micron's *Quality and Reliability Handbook*, which gives an explanation of how thermal impedances are calculated.

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5/3.3V SYNCHRONOUS SRAM PRODUCT SELECTION GUIDE

Memory Configuration	Supply Voltage	Control Functions	Part Number	Access Time (ns)	Cycle Time (ns)	Package and Number of Pins				Page
						SOJ	PLCC	TQFP	DIE	
128K x 9	5V	SPARC® architecture	MT58C1289	6,8,10	12*,16.6,20	32	-	-	CD1/CD2	3-1
64K x 18	3.3V	Intel Burst	MT58LC64K18B2	9,10,12,17	15,15,20,25	-	52	100	CD1/CD2	3-11
64K x 18	3.3V	Intel Burst, Pipelined	MT58LC64K18C4	7,10,12,15	15,20,25,30	-	52	100	CD1/CD2	3-23
64K x 18	3.3V	Linear Burst	MT58LC64K18M1	9,10,12,17	15,15,20,25	-	52	100	CD1/CD2	3-37
64K x 18	3.3V	Linear Burst, Pipelined	MT58LC64K18A6	7,10,12,15	15,20,25,30	-	52	100	CD1/CD2	3-49
32K x 36	3.3V	Intel Burst	MT58LC32K36B2	9,10,12,17	15,15,20,25	-	-	100	CD1/CD2	3-61
32K x 36	3.3V	Intel Burst, Pipelined	MT58LC32K36C4	7,10,12,15	15,20,25,30	-	-	100	CD1/CD2	3-75
32K x 36	3.3V	Linear Burst	MT58LC32K36M1	9,10,12,17	15,15,20,25	-	-	100	CD1/CD2	3-89
32K x 36	3.3V	Linear Burst, Pipelined	MT58LC32K36A6	7,10,12,15	15,20,25,30	-	-	100	CD1/CD2	3-103

NOTE: 1. Many Micron components are available in bare die form. Contact Micron Semiconductor, Inc., for more information.
*Preliminary

SYNCHRONOUS SRAM

128K x 9 SRAM

FULLY REGISTERED INPUTS AND OUTPUTS

FEATURES

- Timing specific to SPARC® microprocessor
- Fast cycle times: 12, 16.6 and 20ns
- Fast clock to data valid: 6, 8 and 10ns
- Single +5V ±10% power supply
- READ data and WRITE data registers
- Common, TTL-compatible data inputs and outputs
- All inputs and outputs registered with clock
- Fully synchronous, pipelined architecture

OPTIONS — MARKING

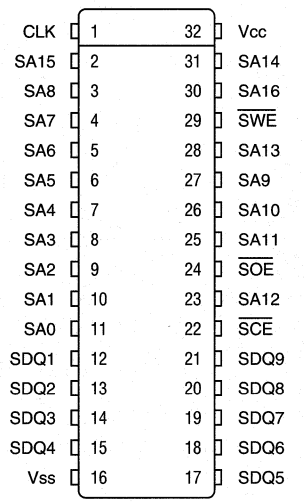
- Timing
  - 6ns access/12ns cycle — -12*
  - 8ns access/16.6ns cycle — -16
  - 10ns access/20ns cycle — -20
- Packages
  - 32-pin SOJ (400mil) — DJ
- Part Number Example: MT58C1289DJ-16

*Preliminary

NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

32-Pin SOJ (SD-5)



GENERAL DESCRIPTION

The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

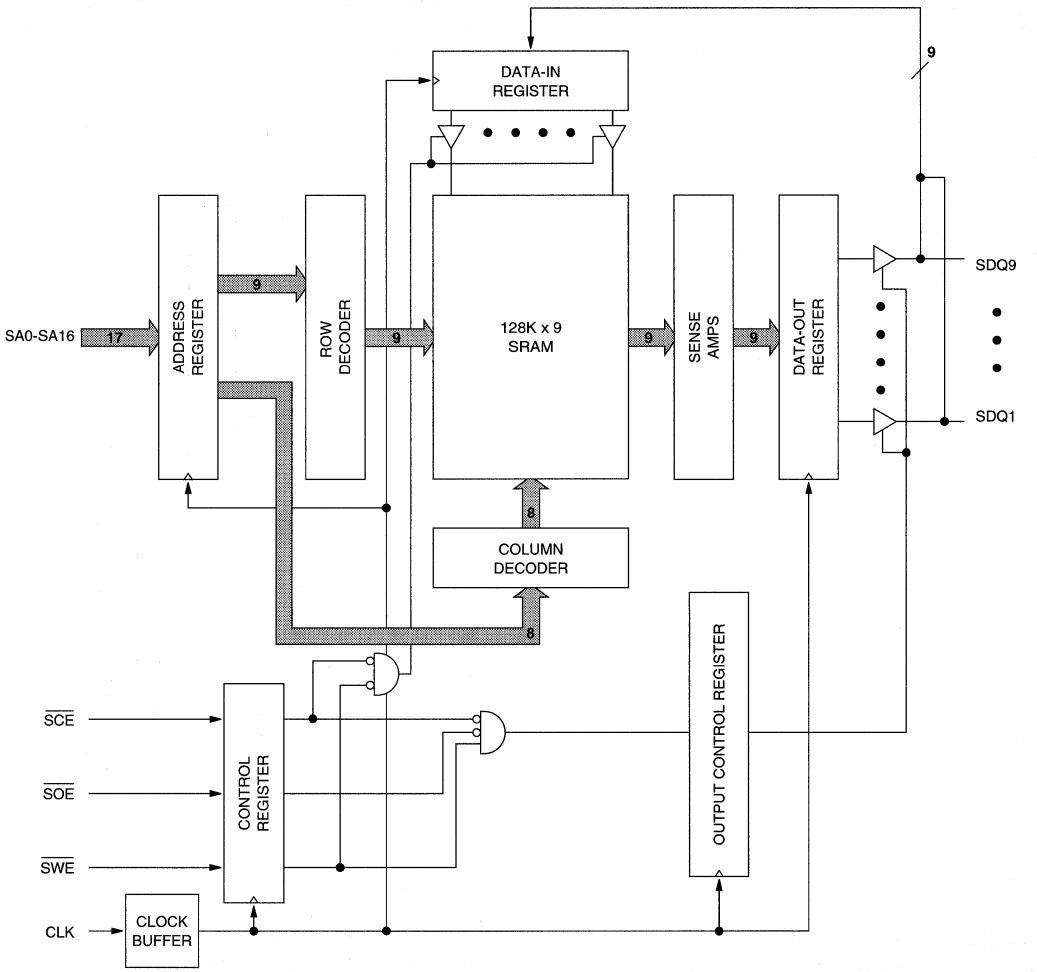
The MT58C1289 is a fully "pipelined" SRAM that integrates registers for address, data-in, data-out and synchronous chip enable ($\overline{SCE}$), output enable ($\overline{SOE}$) and write enable ($\overline{SWE}$). All registers are triggered with the positive edge of the clock signal (CLK).

READ cycles are performed when $\overline{SWE}$ is HIGH and $\overline{SOE}$ and $\overline{SCE}$ are LOW at the positive edge of CLK. Read data is then presented at the next positive edge of CLK.

WRITE cycles occur when $\overline{SWE}$ and $\overline{SCE}$ are LOW at the rising edge CLK. Data present at the data input registers is written to the SRAM address present at the address input registers on that same rising edge of CLK. The WRITE cycle is internally self-timed, eliminating the need for complex write pulse generation external to the SRAM. The WRITE cycle requires three preceding deselect cycles when a WRITE cycle follows a READ cycle. This allows the D/Q lines to be in the High-Z state when write data is applied. The SRAM is deselected if $\overline{SCE}$ is HIGH when a positive edge of CLK occurs.

The MT58C1289 operates from a +5V power supply.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

PLCC AND PQFP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
11, 10, 9, 8, 7, 6, 5, 4, 3, 27, 26, 25, 23, 28, 31, 2, 30	SA0-SA16	Input	Address Inputs: These inputs are synchronous and must meet the setup and hold times around the positive edge of CLK. The address inputs are clocked into the address register on each positive edge of CLK.
29	$\overline{SWE}$	Input	Synchronous Write Enable: This input determines if the cycle is a READ or WRITE cycle. $\overline{SWE}$ is LOW for a WRITE cycle and HIGH for a READ cycle. $\overline{SWE}$ is registered on every positive edge of CLK and must meet the setup and hold times referenced to that edge. WRITE cycles are self-timed internally by the SRAM.
1	CLK	Input	Clock: All timing is controlled by the positive edge of CLK. All synchronous input and output signals are registered on the positive edge of CLK and must meet the setup and hold times referenced to that edge.
22	$\overline{SCE}$	Input	Synchronous Chip Enable: This signal is used to enable the device. This is a synchronous input and must meet the setup and hold times around CLK. When $\overline{SCE}$ is HIGH, the SRAM automatically goes into the standby power mode.
24	$\overline{SOE}$	Input	Synchronous Output Enable: This active LOW input enables the output drivers. This is a synchronous input and must meet the setup and hold times around CLK.
12, 13, 14, 15, 17, 18, 19, 20, 21	SDQ1-SDQ9	Input/ Output	SRAM Data I/O: For a READ, control signals and address are presented at the rising edge of CLK and data is valid ^{t}KQ after the next rising edge of CLK. Data presented for a WRITE cycle must meet the setup and hold times around CLK.
32	Vcc	Supply	Power Supply: +5V ±10%
16	Vss	Supply	Ground: GND

TRUTH TABLE

OPERATION	$\overline{SCE}$	$\overline{SWE}$	CLK	$\overline{SOE}$	D	Q NEXT CLOCK	POWER
Deselected	H	X	↑	X	X	High-Z	Standby
READ	L	H	↑	H	X	High-Z	Active
READ	L	H	↑	L	X	Q1-Q9	Active
WRITE	L	L	↑	X	D1-D9	High-Z	Active

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Voltage on any pin relative to V_{SS} ..... -1V to V_{CC}+1V
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-1	1	µA	
Output Leakage Current	Output(s) disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -1.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 4.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

			MAX				
DESCRIPTION	CONDITIONS	SYMBOL	-12	-16	-20	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX outputs open f = MAX = 1/ ^tRC	I_{CC}	200	160	150	mA	3
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX outputs open f = MAX = 1/ ^tRC	I_{SB1}	90	70	60	mA	
	$\overline{CE}$ ≥ V_{CC} - 0.2V; V_{CC} = MAX; V_{IL} ≤ V_{SS} +0.2V V_{IH} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	5	5	5	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	5	pF	4
Input/Output Capacitance (D/Q)	V_{CC} = 5V	$C_{I/O}$	7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

		-12*		-16		-20			
DESCRIPTION	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Clock									
Clock cycle time	^tKC	12		16.6		20		ns	
Clock HIGH time	^tKH	4		5		5		ns	
Clock LOW time	^tKL	4		5		5		ns	
READ Cycle									
READ cycle time	^tRC	12		16.6		20		ns	9
Address setup time	^tSAS	3		3		3		ns	9
Address hold time	^tSAH	0.5		0.5		1		ns	9
Chip Enable setup time	^tSCES	3		3		3		ns	9
Chip Enable hold time	^tSCEH	0.5		0.5		1		ns	9
Output Enable setup time	^tSOES	3		3		3		ns	9
Output Enable hold time	^tSOEH	0.5		0.5		1		ns	9
Write Enable setup time	^tSWES	3		3		3		ns	9
Write Enable hold time	^tSWEH	0.5		0.5		1		ns	9
Output hold time from clock	^tKOH	1		2		3		ns	
Clock to data valid	^tKQ		6		8		10	ns	
Clock to output High-Z	^tKQHZ		6		8		10	ns	4, 6, 7
Clock to output Low-Z	^tKQLZ	0		0		0		ns	4, 6, 7
WRITE Cycle									
WRITE cycle time	^tWC	12		16.6		20		ns	
Address setup time	^tSAS	3		3		3		ns	9
Address hold time	^tSAH	0.5		0.5		1		ns	9
Chip Enable setup time	^tSCES	3		3		3		ns	9
Chip Enable hold time	^tSCEH	0.5		0.5		1		ns	9
Write Enable setup time	^tSWES	3		3		3		ns	9
Write Enable hold time	^tSWEH	0.5		0.5		1		ns	9
Data setup time	^tSDS	3		3		3		ns	
Data hold time	^tSDH	0.5		0.5		1		ns	

*Preliminary. Consult factory for availability.

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

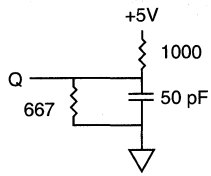


Fig. 1 OUTPUT LOAD EQUIVALENT

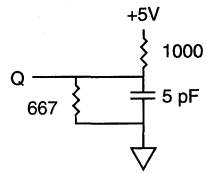
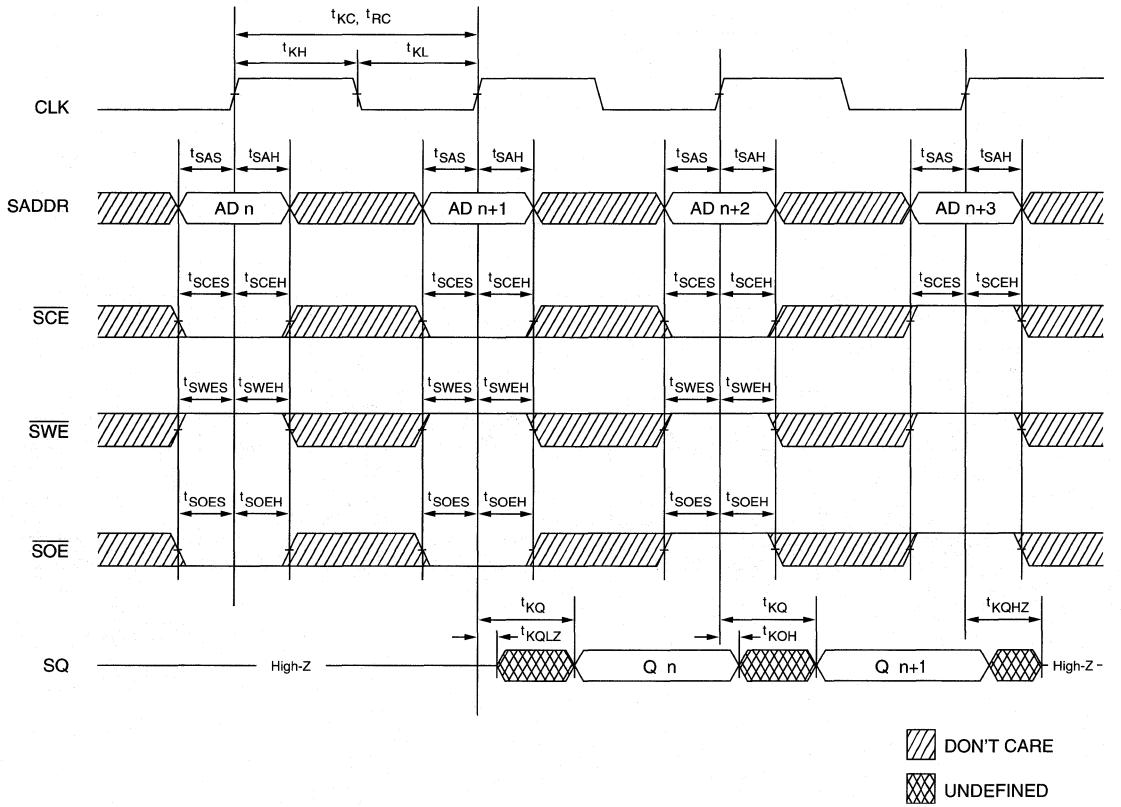


Fig. 2 OUTPUT LOAD EQUIVALENT

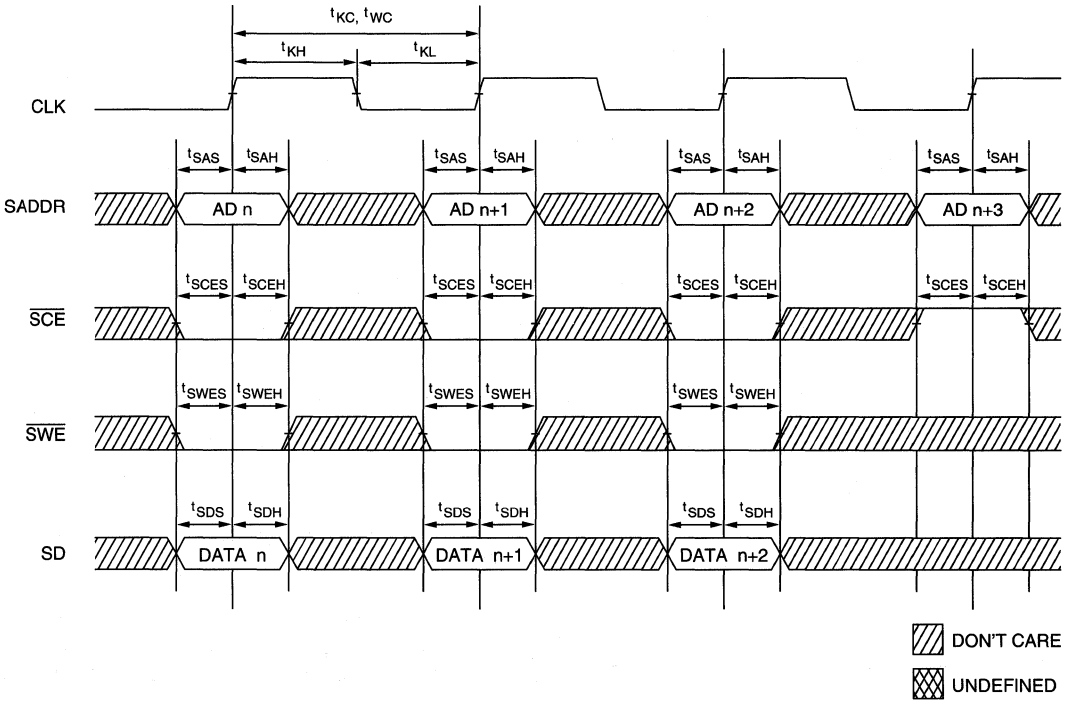
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < $^{t}RC/2$.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. Output loading is specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, $^{t}KQHZ$ is less than $^{t}KQLZ$.
8. $\overline{WE}$ is HIGH for READ cycle.
9. This is a synchronous device. All synchronous inputs must meet the setup and hold times with stable logic levels for all rising edges of CLK.

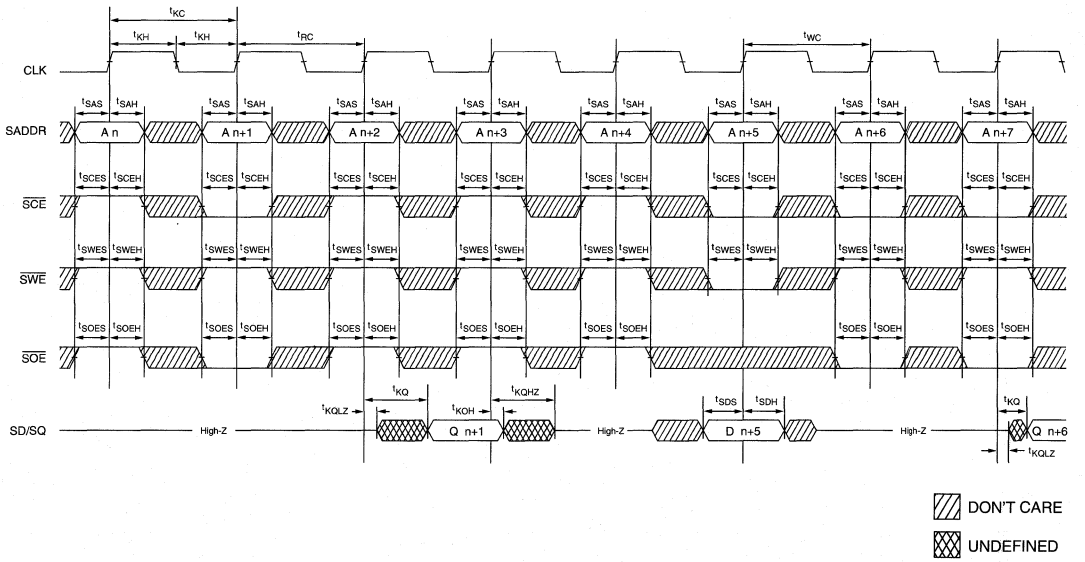
READ TIMING [7, 8, 9]



WRITE TIMING [7, 9]



READ/WRITE TIMING [7, 8, 9]



MICRON SEMICONDUCTOR, INC.

MT58LC64K18B2
64K x 18 SYNCHRONOUS SRAM

SYNCHRONOUS SRAM

64K x 18 SRAM

+3.3V SUPPLY WITH CLOCKED, REGISTERED INPUTS AND BURST COUNTER

NEW

3.3 VOLT SYNCHRONOUS SRAM

FEATURES

- Fast access times: 9, 10, 12 and 17ns
- Fast $\overline{OE}$: 5, 6 and 7ns
- Single +3.3V ±5% power supply
- 5V-tolerant I/O
- Common data inputs and data outputs
- Individual BYTE WRITE control
- Clock controlled, registered, address, data and control
- Internally self-timed WRITE cycle
- Burst control pins (486/Pentium™ burst sequence)
- High density, high speed packages
- Low capacitive bus loading
- High 30pF output drive capability at rated access time

OPTIONS MARKING

- Timing

9ns access/15ns cycle	- 9
10ns access/15ns cycle	-10
12ns access/20ns cycle	-12
17ns access/25ns cycle	-17

- Packages

52-pin PLCC	EJ
100-pin TQFP	LG

- Part Number Example: MT58LC64K18B2EJ-12

NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

GENERAL DESCRIPTION

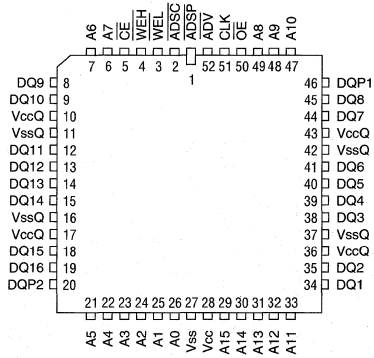
The Micron Synchronous SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

The MT58LC64K18B2 SRAM integrates a 64K x 18 SRAM core with advanced synchronous peripheral circuitry and a 2-bit burst counter. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input (CLK). The synchronous inputs include all addresses, all data inputs, active LOW chip enable ($\overline{CE}$), burst control inputs ($\overline{ADSC}$, $\overline{ADSP}$, $\overline{ADV}$) and byte write enables ($\overline{WEH}$, $\overline{WEL}$).

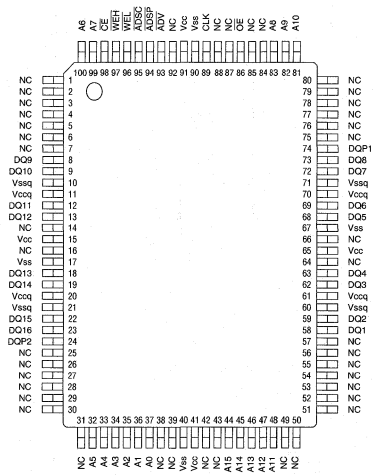
Asynchronous inputs include the output enable ($\overline{OE}$) and the clock (CLK). The data-out (Q), enabled by $\overline{OE}$, is also asynchronous. WRITE cycles can be from one to two bytes wide as controlled by the byte write enables.

PIN ASSIGNMENT (Top View)

52-Pin PLCC
(SB-1)



100-Pin TQFP
(SC-1)



NEW

3.3 VOLT SYNCHRONOUS SRAM

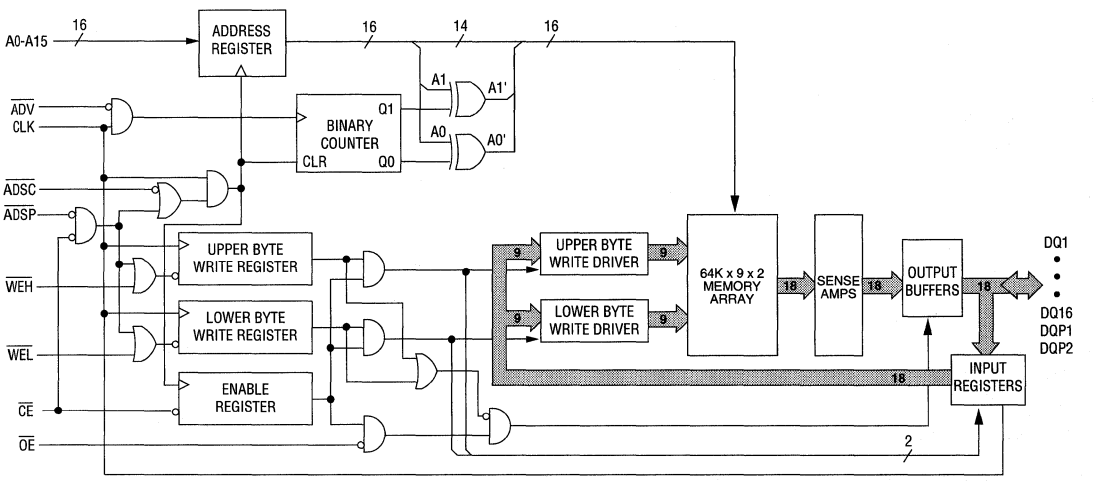
GENERAL DESCRIPTION (continued)

Burst operation can be initiated with either address status processor ($\overline{ADSP}$) or address status controller ($\overline{ADSC}$) input pins. Subsequent burst addresses can be internally generated as controlled by the burst advance pin ($\overline{ADV}$).

Address and write control are registered on-chip to simplify WRITE cycles. This allows self-timed WRITE cycles. Individual byte enables allow individual bytes to be written. $\overline{WEL}$ controls DQ1-DQ8 and DQP1. $\overline{WEH}$ controls DQ9-DQ16 and DQP2.

The MT58LC64K18B2 operates from a +3.3V power supply and all inputs and outputs are TTL-compatible and 5V tolerant. The device is ideally suited for 486 and Pentium (P5) systems and those systems which benefit from a wide synchronous data bus.

FUNCTIONAL BLOCK DIAGRAM



NOTE: The Functional Block Diagram illustrates simplified device operation. See Truth Table, pin descriptions and timing diagrams for detailed information.

BURST SEQUENCE TABLE

	Address Used		
Operation	**A14-A2**	**A1**	**A0**
First access, register external address	A14-A2	A1	A0
Second access (first burst address)	registered A14-A2	registered A1	registered $\overline{A0}$
Third access (second burst address)	registered A14-A2	registered $\overline{A1}$	registered A0
Fourth access (third burst address)	registered A14-A2	registered $\overline{A1}$	registered $\overline{A0}$

NOTE: The burst sequence wraps around to its initial state upon completion.

BURST ADDRESS TABLE

First Address	Second Address	Third Address	Fourth Address
X...X00	X...X01	X...X10	X...X11
X...X01	X...X00	X...X11	X...X10
X...X10	X...X11	X...X00	X...X01
X...X11	X...X10	X...X01	X...X00

NEW 3.3 VOLT SYNCHRONOUS SRAM

PIN DESCRIPTIONS

PLCC PINS	TQFP PINS	SYMBOL	TYPE	DESCRIPTION
26, 25, 24, 23, 22, 21, 7, 6, 49, 48, 47, 33, 32, 31, 30, 29	37, 36, 35, 34, 33, 32, 100, 99, 83, 82, 81, 48, 47, 46, 45, 44	A0-A15	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK.
4, 3	97, 96	$\overline{WEH}$, $\overline{WEL}$	Input	Synchronous Byte Write Enables: These active LOW inputs allow individual bytes to be written and must meet the setup and hold times around the rising edge of CLK. A byte write enable is LOW for a WRITE cycle and HIGH for a READ cycle. $\overline{WEL}$ controls DQ1-DQ8 and DQP1. $\overline{WEH}$ controls DQ9-DQ16 and DQP2. Data I/O are tristated if either of these inputs are LOW.
51	89	CLK	Input	Clock: This signal registers the address, data, chip enable, byte write enables and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
5	98	$\overline{CE}$	Input	Synchronous Chip Enable: This active LOW input is used to enable the device. This input is sampled only when a new external address is loaded.
50	86	$\overline{OE}$	Input	Output Enable: This active LOW asynchronous input enables the data I/O output drivers.
52	93	$\overline{ADV}$	Input	Synchronous Address Advance: This active LOW input is used to advance the internal burst counter, controlling burst access after the external address is loaded. A HIGH on this pin effectively causes wait states to be generated (no address advance). This pin must be HIGH at the rising edge of the first clock after an $\overline{ADSP}$ cycle is initiated if a WRITE cycle is desired (to ensure use of correct address).
1	94	$\overline{ADSP}$	Input	Synchronous Address Status Processor: This active LOW input interrupts any ongoing burst, causing a new external address to be registered. A READ is performed using the new address, independent of the byte write enables and $\overline{ADSC}$ but dependent upon $\overline{CE}$ being LOW.
2	95	$\overline{ADSC}$	Input	Synchronous Address Status Controller: This active LOW input interrupts any ongoing burst, causing a new external address to be registered. A READ or WRITE is performed using the new address if $\overline{CE}$ is LOW. $\overline{ADSC}$ is also used to place the chip into power-down state when $\overline{CE}$ is HIGH.
34, 35, 38, 39, 40, 41, 44, 45, 8, 9, 12, 13, 14, 15, 18, 19	58, 59, 62, 63, 68, 69, 72, 73, 8, 9, 12, 13, 18, 19, 22, 23	DQ1-DQ16	Input/ Output	SRAM Data I/O: Low Byte is DQ1-DQ8. High Byte is DQ9-DQ16. Input data must meet setup and hold times around the rising edge of CLK.
46, 20	74, 24	DQP1, DQP2	Input/ Output	Parity Data I/O: Low Byte Parity is DQP1. High Byte Parity is DQP2.
28	15, 41, 65, 91	Vcc	Supply	Power Supply: +3.3V ±5%
27	17, 40, 67, 90	Vss	Supply	Ground: GND
10, 17, 36, 43	11, 20, 61, 71	VccQ	Supply	Isolated Output Buffer Supply: +3.3V ±5%

PIN DESCRIPTIONS (continued)

PLCC PINS	TQFP PINS	SYMBOL	TYPE	DESCRIPTION
11, 16, 37, 42	10, 21, 60, 71	VssQ	Supply	Isolated Output Buffer Ground: GND
	1, 2, 3, 4, 5, 6, 7, 14, 16, 25, 26, 27, 28, 29, 30, 31, 38, 39, 42, 43, 49, 50, 51, 52, 53, 54, 55, 56, 57, 64, 66, 75, 76, 77, 78, 79, 80, 84, 85, 87, 88, 92	NC	-	No Connect: These signals are not internally connected. These signals may be connected to ground to improve package heat dissipation.

TRUTH TABLE

OPERATION	ADDRESS USED	$\overline{CE}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Deselected Cycle, Power-down	None	H	X	L	X	X	X	L-H	High-Z
READ Cycle, Begin Burst	External	L	L	X	X	X	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	X	X	X	H	L-H	High-Z
WRITE Cycle, Begin Burst	External	L	H	L	X	L	X	L-H	D
READ Cycle, Begin Burst	External	L	H	L	X	H	L	L-H	Q
READ Cycle, Begin Burst	External	L	H	L	X	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	X	H	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	X	H	H	L	H	H	L-H	High-Z
WRITE Cycle, Continue Burst	Next	X	H	H	L	L	X	L-H	D
READ Cycle, Continue Burst	Next	H	X	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	H	X	H	L	H	H	L-H	High-Z
WRITE Cycle, Continue Burst	Next	H	X	H	L	L	X	L-H	D
READ Cycle, Suspend Burst	Current	X	H	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	X	H	H	H	H	H	L-H	High-Z
WRITE Cycle, Suspend Burst	Current	X	H	H	H	L	X	L-H	D
READ Cycle, Suspend Burst	Current	H	X	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	H	X	H	H	H	H	L-H	High-Z
WRITE Cycle, Suspend Burst	Current	H	X	H	H	L	X	L-H	D

NOTE:
1. X means "don't care." H means logic HIGH. L means logic LOW. $\overline{WRITE}$=L means any one or more byte write enable signals ($\overline{WEH}$, $\overline{WEL}$) are LOW. $\overline{WRITE}$=H means all byte write enable signals are HIGH.
2. $\overline{WEL}$ enables writes to DQ1-DQ8 and DQP1. $\overline{WEH}$ enables writes to DQ9-DQ16 and DQP2.
3. All inputs except $\overline{OE}$ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
4. Wait states are inserted by suspending burst.
5. For a write operation following a read operation, $\overline{OE}$ must be HIGH before the input data required setup time and held HIGH throughout the input data hold time.
6. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
7. $\overline{ADSP}$ LOW always initiates an internal READ at the L-H edge of CLK. A WRITE is performed by setting one or more byte write enable signal LOW for the subsequent L-H edge of CLK. Refer to WRITE timing diagram for clarification.

NEW

3.3 VOLT SYNCHRONOUS SRAM

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to Vss .....-0.5V to +4.6V
V_{IN} ..... -0.5V to +6V
Storage Temperature (plastic) ..... -55°C to +150°C
Junction Temperature ..... +150°C
Power Dissipation 1.6W
Short Circuit Output Current 100mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; T_C ≤ 110°C; V_{CC} = 3.3V ±5% unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.0	5.5	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-1	1	µA	
Output Leakage Current	Output(s) disabled, 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	3.1	3.5	V	1

				MAX					
DESCRIPTION	CONDITIONS	SYMBOL	TYPICAL	-9	-10	-12	-17	UNITS	NOTES
Power Supply Current: Operating	Device selected; all inputs ≤ V_{IL} OR ≥ V_{IH}; cycle time ≥ ^tKC min; Vcc = MAX; outputs open	I_{CC}	150	225	225	200	175	mA	3, 12 13
Power Supply Current: Idle	Device selected; $\overline{ADSC}$, $\overline{ADSP}$, $\overline{ADV}$ ≥ V_{IH}; all inputs ≤ V_{IL} OR ≥ V_{IH}; Vcc = MAX; cycle time ≥ ^tKC min; outputs open	I_{SB1}	45	65	65	55	50	mA	12, 13
CMOS Standby	Device deselected; Vcc = MAX; all inputs ≤ Vss +0.2 or ≥ Vcc -0.2; all inputs static; CLK frequency = 0	I_{SB2}	0.2	2	2	2	2	mA	12, 13
TTL Standby	Device deselected; all inputs ≤ V_{IL} OR ≥ V_{IH}; all inputs static; Vcc = MAX; CLK frequency = 0	I_{SB3}	10	18	18	18	18	mA	12, 13
Clock Running	Device deselected; all inputs ≤ V_{IL} OR ≥ V_{IH}; Vcc = MAX; CLK cycle time ≥ ^tKC min	I_{SB4}	20	35	35	30	25	mA	12, 13

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	3	4	pF	4
Input/Output Capacitance (DQ)	V_{CC} = 3.3V	C_O	5	6	pF	4

THERMAL CONSIDERATIONS

DESCRIPTION	CONDITIONS	SYMBOL	PLCC TYP	TQFP TYP	UNITS	NOTES
Thermal resistance - Junction to Ambient	Still Air	θ_{JA}	45	65	°C/W	
Thermal resistance - Junction to Case		θ_{JC}	15	6	°C/W	
Maximum Case Temperature		TC	110	110	°C	11

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) ($0°C \le T_A \le 70°C$; Vcc = 3.3V ±5%)

		-9		-10		-12		-17			
DESCRIPTION	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Clock											
Clock cycle time	^tKC	15		15		20		25		ns	
Clock HIGH time	^tKH	4		5		6		8		ns	
Clock LOW time	^tKL	4		5		6		8		ns	
Output Times											
Clock to output valid	^tKQ		9		10		12		17	ns	
Clock to output invalid	^tKQX	3		3		3		3		ns	
Clock to output in Low-Z	^tKQLZ	5		5		5		5		ns	6, 7
Clock to output in High-Z	^tKQHZ		5		5		6		6	ns	6, 7
$\overline{OE}$ to output valid	^tOEQ		5		5		6		7	ns	9
$\overline{OE}$ to output in Low-Z	^tOELZ	0		0		0		0		ns	6, 7
$\overline{OE}$ to output in High-Z	^tOEHZ		5		5		6		6	ns	6, 7
Setup Times											
Address	^tAS	2.5		3		3		3		ns	8, 10
Address Status ($\overline{ADSC}$, $\overline{ADSP}$)	^tADSS	2.5		3		3		3		ns	8, 10
Address Advance ($\overline{ADV}$)	^tAAS	2.5		3		3		3		ns	8, 10
Byte Write Enables ($\overline{WEH}$, $\overline{WEL}$)	^tWS	2.5		3		3		3		ns	8, 10
Data-in	^tDS	2.5		3		3		3		ns	8, 10
Chip Enable ($\overline{CE}$)	^tCES	2.5		3		3		3		ns	8, 10
Hold Times											
Address	^tAH	0.5		0.5		0.5		0.5		ns	8, 10
Address Status ($\overline{ADSC}$, $\overline{ADSP}$)	^tADSH	0.5		0.5		0.5		0.5		ns	8, 10
Address Advance ($\overline{ADV}$)	^tAAH	0.5		0.5		0.5		0.5		ns	8, 10
Byte Write Enables ($\overline{WEH}$, $\overline{WEL}$)	^tWH	0.5		0.5		0.5		0.5		ns	8, 10
Data-in	^tDH	0.5		0.5		0.5		0.5		ns	8, 10
Chip Enable ($\overline{CE}$)	^tCEH	0.5		0.5		0.5		0.5		ns	8, 10

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	1.5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

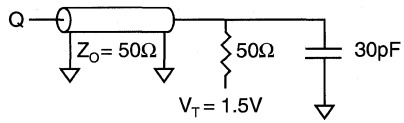


Fig. 1 OUTPUT LOAD EQUIVALENT

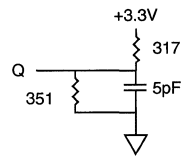
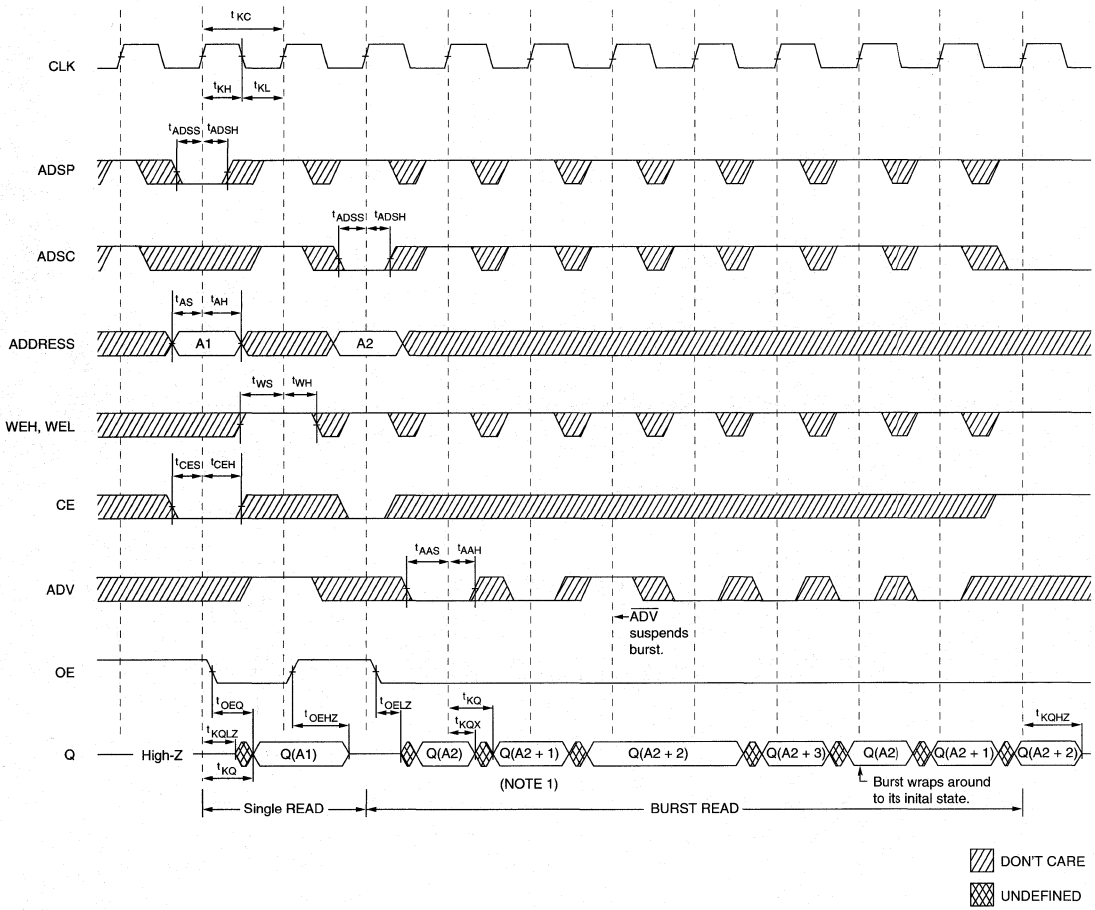


Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

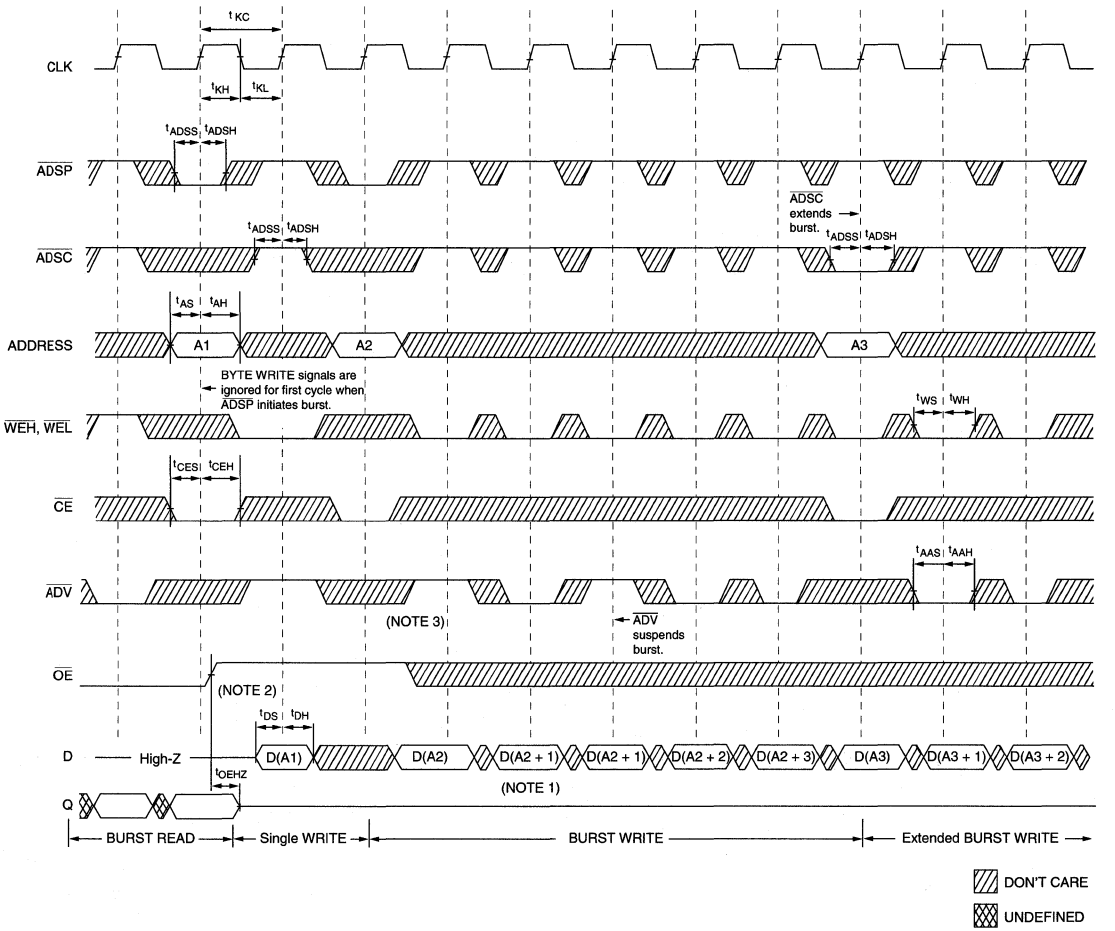
1. All voltages referenced to Vss (GND).
2. Overshoot: $V_{IH} \leq +6.0V$ for $t \leq {}^tKC/2$.
   Undershoot: $V_{IL} \geq -2.0V$ for $t \leq {}^tKC/2$.
   Power-up: $V_{IH} \leq +6.0V$ and $Vcc \leq 3.1V$ for $t \leq 200msec$.
3. Icc is given with no output current. Icc increases with greater output loading and faster cycle times.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. Output loading is specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ${}^tKQHZ$ is less than ${}^tKQLZ$ and ${}^tOEHZ$ is less than ${}^tOELZ$.
8. A READ cycle is defined by byte write enables all HIGH or $\overline{ADSP}$ LOW for the required setup and hold times. A WRITE cycle is defined by at least one byte Write enable LOW and $\overline{ADSP}$ HIGH for the required setup and hold times.
9. $\overline{OE}$ is a "don't care" when a byte write enable is sampled LOW.
10. This is a synchronous device. All addresses must meet the specified setup and hold times for all rising edges of CLK when either $\overline{ADSP}$ or $\overline{ADSC}$ is LOW and chip enabled. All other synchronous inputs must meet the setup and hold times with stable logic levels for all rising edges of clock (CLK) when chip is enabled. Chip enable must be valid at each rising edge of CLK (when either $\overline{ADSP}$ or $\overline{ADSC}$ is LOW) to remain enabled.
11. Micron does not warrant the functionality or reliability of any product in which the case temperature exceeds 110°C. Care should be taken to limit case temperature to acceptable levels.
12. "Device Deselected" means device is in POWER-DOWN mode as defined in the truth table. "Device Selected" means device is active (not in POWER-DOWN mode).
13. Typical values are measured at 3.3V, 25°C and 20ns cycle time.

READ TIMING



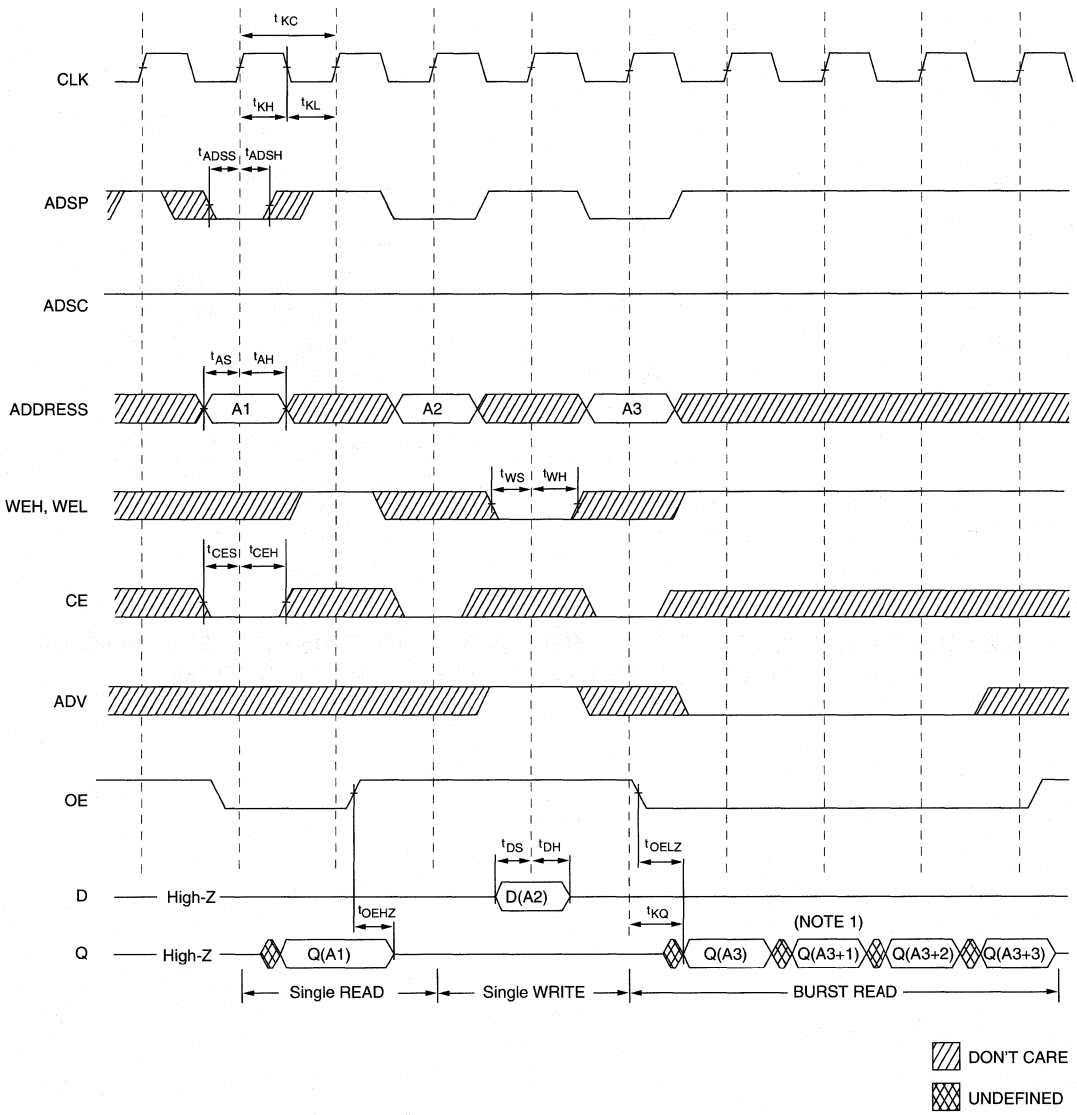
NOTE: 1. Q(A2) refers to output from address A2. Q(A2+1) refers to output from the next internal burst address following A2.

WRITE TIMING



NOTE:
1. D(A2) refers to input to address A2. D(A2+1) refers to input to the next internal burst address following A2.
2. $\overline{OE}$ must be HIGH before the input data setup and held HIGH throughout the the data hold time. This prevents input/output data contention for the time period prior to the byte write enable inputs being sampled.
3. $\overline{ADV}$ must be HIGH to permit a WRITE to the loaded address.

READ/WRITE TIMING



NOTE: 1. Q(A3) refers to output from address A3. Q(A3+1) refers to output from the next internal burst address following A3.

APPLICATION EXAMPLE

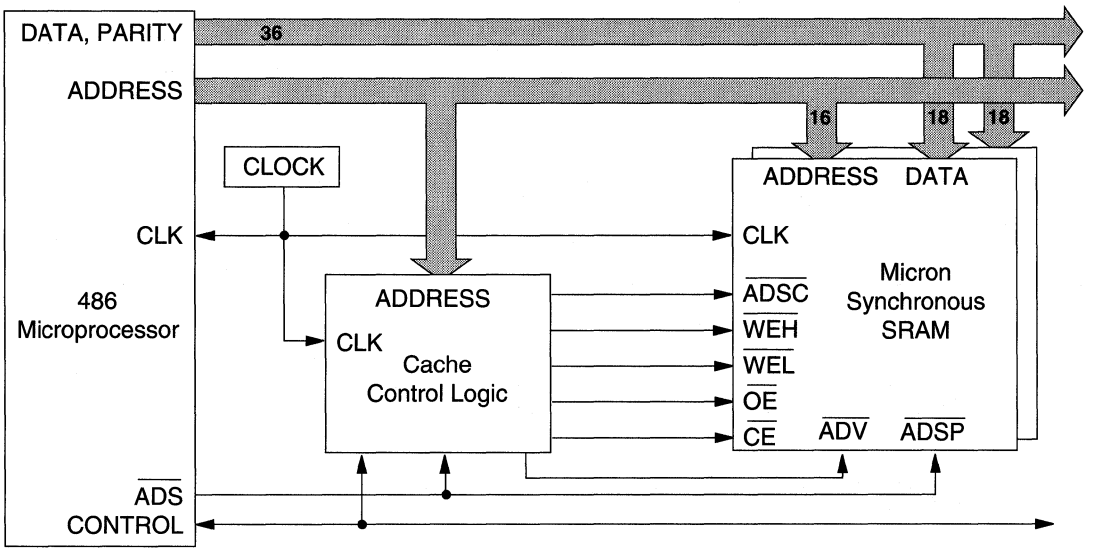


Figure 3
256K BYTE SECONDARY CACHE WITH PARITY AND BURST FOR 50 MHz 80486 USING TWO MT58LC64K18B2EJ-12 SYNCHRONOUS SRAMs

SYNCHRONOUS SRAM

64K x 18 SRAM

+3.3V SUPPLY, FULLY REGISTERED INPUTS AND OUTPUTS AND BURST COUNTER

NEW 3.3 VOLT SYNCHRONOUS SRAM

FEATURES

- Fast access times: 7, 10, 12 and 15ns
- Fast $\overline{OE}$: 5, 6, 7 and 8ns
- Single +3.3V ±5% power supply
- 5V-tolerant I/O
- Common data inputs and data outputs
- Individual BYTE WRITE control
- Clock controlled, registered, address, data I/O and control for fully pipelined applications
- Internally self-timed WRITE cycle
- WRITE pass-through capability
- Burst control pins (486/Pentium™ burst sequence)
- High density, high-speed packages
- Low capacitive bus loading
- High 50pF output drive capability at rated access time

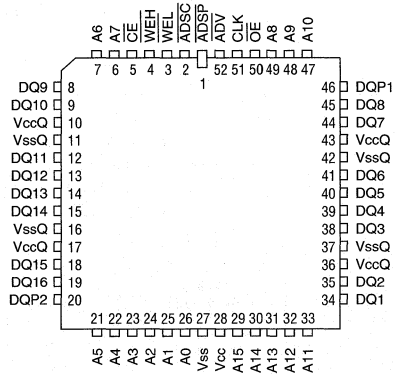
OPTIONS — MARKING

- Timing
  - 7ns access/15ns cycle — -7
  - 10ns access/20ns cycle — -10
  - 12ns access/25ns cycle — -12
  - 15ns access/30ns cycle — -15
- Packages
  - 52-pin PLCC — EJ
  - 100-pin TQFP — LG
- Part Number Example: MT58LC64K18C4EJ-10

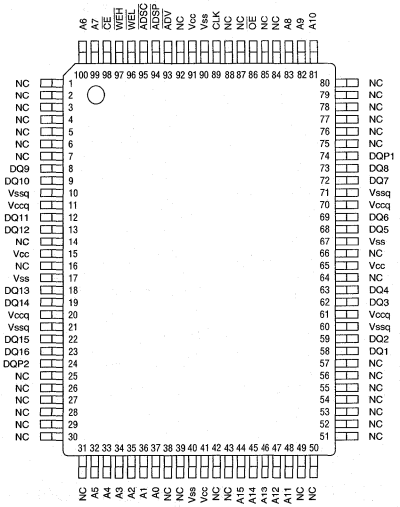
NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

52-Pin PLCC
(SB-1)



100-Pin TQFP
(SC-1)



GENERAL DESCRIPTION

The Micron Synchronous SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

The MT58LC64K18C4 SRAM integrates a 64K x 18 SRAM core with advanced synchronous peripheral circuitry, a 2-bit burst counter and output register. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input (CLK). The synchronous inputs include all addresses, all data inputs, active LOW chip enable ($\overline{CE}$), burst control inputs ($\overline{ADSC}$, $\overline{ADSP}$, $\overline{ADV}$) and the byte write enables ($\overline{WEH}$, $\overline{WEL}$).

Asynchronous inputs include the output enable ($\overline{OE}$) and the clock (CLK). The data-out (Q), enabled by $\overline{OE}$, is also

NEW 3.3 VOLT SYNCHRONOUS SRAM

GENERAL DESCRIPTION (continued)

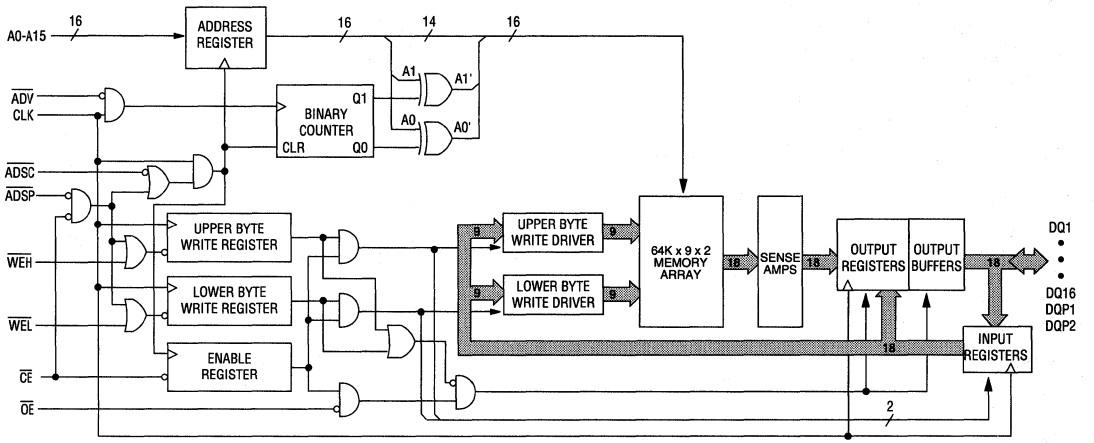
asynchronous. The output register is controlled by the clock. WRITE cycles can be from one to two bytes wide as controlled by the byte write enables.

Burst operation can be initiated with either address status processor ($\overline{ADSP}$) or address status controller ($\overline{ADSC}$) input pins. Subsequent burst addresses can be internally generated as controlled by the burst advance pin ($\overline{ADV}$).

Address and write control are registered on-chip to simplify WRITE cycles. This allows self-timed WRITE cycles. WRITE pass-through makes written data immediately available at the output register during the READ cycle following a WRITE as controlled solely by $\overline{OE}$ to improve cache system response.

The MT58LC64K18C4 operates from a +3.3V power supply and all inputs and outputs are TTL-compatible and 5V tolerant. The device is ideally suited for Pentium (P5) pipelined applications.

FUNCTIONAL BLOCK DIAGRAM



NOTE: The Functional Block Diagram illustrates simplified device operation. See Truth Table, pin descriptions and timing diagrams for detailed information.

BURST SEQUENCE TABLE

	Address Used		
Operation	**A14-A2**	**A1**	**A0**
First access, register external address	A14-A2	A1	A0
Second access (first burst address)	registered A14-A2	registered A1	registered $\overline{A0}$
Third access (second burst address)	registered A14-A2	registered $\overline{A1}$	registered A0
Fourth access (third burst address)	registered A14-A2	registered $\overline{A1}$	registered $\overline{A0}$

NOTE: The burst sequence wraps around to its initial state upon completion.

BURST ADDRESS TABLE

First Address	Second Address	Third Address	Fourth Address
X...X00	X...X01	X...X10	X...X11
X...X01	X...X00	X...X11	X...X10
X...X10	X...X11	X...X00	X...X01
X...X11	X...X10	X...X01	X...X00

PIN DESCRIPTIONS

PLCC PINS	TQFP PINS	SYMBOL	TYPE	DESCRIPTION
26, 25, 24, 23, 22, 21, 7, 6, 49, 48, 47, 33, 32, 31, 30, 29	37, 36, 35, 34, 33, 32, 100, 99, 83, 82, 81, 48, 47, 46, 45, 44	A0-A15	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK.
4, 3	97, 96	$\overline{WEH}$, $\overline{WEL}$	Input	Synchronous Byte Write Enables: These active LOW inputs allow individual bytes to be written and must meet the setup and hold times around the rising edge of CLK. A byte write enable is LOW for a WRITE cycle and HIGH for a READ cycle. $\overline{WEL}$ controls DQ1-DQ8 and DQP1. $\overline{WEH}$ controls DQ9-DQ16 and DQP2. Data I/O are tristated if either of these inputs are LOW.
51	89	CLK	Input	Clock: This signal registers the address, data, chip enable, byte write enables and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
5	98	$\overline{CE}$	Input	Synchronous Chip Enable: This active LOW input is used to enable the device. This input is sampled only when a new external address is loaded.
50	86	$\overline{OE}$	Input	Output Enable: This active LOW asynchronous input enables the data I/O output drivers.
52	93	$\overline{ADV}$	Input	Synchronous Address Advance: This active LOW input is used to advance the internal burst counter, controlling burst access after the external address is loaded. A HIGH on this pin effectively causes wait states to be generated (no address advance). This pin must be HIGH at the rising edge of the first clock after an $\overline{ADSP}$ cycle is initiated if a WRITE cycle is desired (to ensure use of correct address).
1	94	$\overline{ADSP}$	Input	Synchronous Address Status Processor: This active LOW input interrupts any ongoing burst, causing a new external address to be registered. A READ is performed using the new address, independent of the byte write enables and $\overline{ADSC}$ but dependent upon $\overline{CE}$ being LOW.
2	95	$\overline{ADSC}$	Input	Synchronous Address Status Controller: This active LOW input interrupts any ongoing burst, causing a new external address to be registered. A READ or WRITE is performed using the new address if $\overline{CE}$ is LOW. $\overline{ADSC}$ is also used to place the chip into power-down state when $\overline{CE}$ is HIGH.
34, 35, 38, 39, 40, 41, 44, 45, 8, 9, 12, 13, 14, 15, 18, 19	58, 59, 62, 63, 68, 69, 72, 73, 8, 9, 12, 13, 18, 19, 22, 23	DQ1-DQ16	Input/ Output	SRAM Data I/O: Low Byte is DQ1-DQ8. High Byte is DQ9-DQ16. Input data must meet setup and hold times around the rising edge of CLK.
46, 20	74, 24	DQP1, DQP2	Input/ Output	Parity Data I/O: Low Byte Parity is DQP1. High Byte Parity is DQP2.
28	15, 41, 65, 91	Vcc	Supply	Power Supply: +3.3V ±5%
27	17, 40, 67, 90	Vss	Supply	Ground: GND
10, 17, 36, 43	11, 20, 61, 71	VccQ	Supply	Isolated Output Buffer Supply: +3.3V ±5%

PIN DESCRIPTIONS (continued)

PLCC PINS	TQFP PINS	SYMBOL	TYPE	DESCRIPTION
11, 16, 37, 42	10, 21, 60, 71	VssQ	Supply	Isolated Output Buffer Ground: GND
	1, 2, 3, 4, 5, 6, 7, 14, 16, 25, 26, 27, 28, 29, 30, 31, 38, 39, 42, 43, 49, 50, 51, 52, 53, 54, 55, 56, 57, 64, 66, 75, 76, 77, 78, 79, 80, 84, 85, 87, 88, 92	NC	-	No Connect: These signals are not internally connected. These signals may be connected to ground to improve package heat dissipation.

TRUTH TABLE

OPERATION	ADDRESS USED	$\overline{CE}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Deselected Cycle, Power-down	None	H	X	L	X	X	X	L-H	High-Z
READ Cycle, Begin Burst	External	L	L	X	X	X	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	X	X	X	H	L-H	High-Z
WRITE Cycle, Begin Burst	External	L	H	L	X	L	X	L-H	D
READ Cycle, Begin Burst	External	L	H	L	X	H	L	L-H	Q
READ Cycle, Begin Burst	External	L	H	L	X	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	X	H	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	X	H	H	L	H	H	L-H	High-Z
WRITE Cycle, Continue Burst	Next	X	H	H	L	L	X	L-H	D
READ Cycle, Continue Burst	Next	H	X	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	H	X	H	L	H	H	L-H	High-Z
WRITE Cycle, Continue Burst	Next	H	X	H	L	L	X	L-H	
READ Cycle, Suspend Burst	Current	X	H	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	X	H	H	H	H	H	L-H	High-Z
WRITE Cycle, Suspend Burst	Current	X	H	H	H	L	X	L-H	D
READ Cycle, Suspend Burst	Current	H	X	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	H	X	H	H	H	H	L-H	High-Z
WRITE Cycle, Suspend Burst	Current	H	X	H	H	L	X	L-H	D

NOTE:
1. X means "don't care." H means logic HIGH. L means logic LOW. $\overline{WRITE}$=L means any one or more byte write enable signals ($\overline{WEH}$, $\overline{WEL}$) are LOW. $\overline{WRITE}$=H means all byte write enable signals are HIGH.
2. $\overline{WEL}$ enables writes to DQ1-DQ8 and DQP1. $\overline{WEH}$ enables writes to DQ9-DQ16 and DQP2.
3. All inputs except $\overline{OE}$ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
4. Wait states are inserted by suspending burst.
5. For a write operation following a read operation, $\overline{OE}$ must be HIGH before the input data required setup time and held HIGH throughout the input data hold time.
6. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
7. $\overline{ADSP}$ LOW always initiates an internal READ at the L-H edge of CLK. A WRITE is performed by setting one or more byte write enable signal LOW for the subsequent L-H edge of CLK. Refer to WRITE timing diagram for clarification.

PASS-THROUGH TRUTH TABLE

PREVIOUS CYCLE		PRESENT CYCLE				NEXT CYCLE
OPERATION	$\overline{WEs}$	OPERATION	$\overline{CE}$	$\overline{WEs}$	$\overline{OE}$	OPERATION
Initiate WRITE cycle, all bytes Address = A(n-1); data = D(n-1)	All L	Initiate READ cycle Register A(n), Q = D(n-1)	L	H	L	Read D(n)
Initiate WRITE cycle, all bytes Address = A(n-1); data = D(n-1)	All L	No new cycle Q = D(n-1)	H	H	L	No carryover from previous cycle
Initiate WRITE cycle, all bytes Address = A(n-1); data = D(n-1)	All L	No new cycle Q = HIGH-Z	H	H	H	No carryover from previous cycle
Initiate WRITE cycle, one byte Address = A(n-1); data = D(n-1)	One L	No new cycle Q = D(n-1) for one byte	H	H	L	No carryover from previous cycle

NOTE: Previous cycle may be either BURST or NONBURST cycle.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to Vss .....-0.5V to +4.6V
V_{IN} .....-0.5V to +6V
Storage Temperature (plastic) .....-55°C to +150°C
Junction Temperature .....+150°C
Power Dissipation 1.6W
Short Circuit Output Current 100mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; T_C ≤ 110°C; V_{CC} = 3.3V ±5% unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.0	5.5	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-1	1	µA	
Output Leakage Current	Output(s) disabled, 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	3.1	3.5	V	1

				MAX					
DESCRIPTION	CONDITIONS	SYMBOL	TYPICAL	-7	-10	-12	-15	UNITS	NOTES
Power Supply Current: Operating	Device selected; all inputs ≤ V_{IL} OR ≥ V_{IH}; cycle time ≥ ^tKC min; Vcc = MAX; outputs open	I_{CC}	150	225	200	175	160	mA	3, 12, 13
Power Supply Current: Idle	Device selected; $\overline{ADSC}$, $\overline{ADSP}$, $\overline{ADV}$ ≥ V_{IH}; all inputs ≤ V_{IL} OR ≥ V_{IH}; Vcc = MAX; cycle time ≥ ^tKC min	I_{SB1}	45	65	55	50	45	mA	12, 13
CMOS Standby	Device deselected; Vcc = MAX; all inputs ≤ Vss +0.2 or ≥ Vcc -0.2; all inputs static; CLK frequency = 0	I_{SB2}	0.2	2	2	2	2	mA	12, 13
TTL Standby	Device deselected; all inputs ≤ V_{IL} OR ≥ V_{IH}; all inputs static; Vcc = MAX; CLK frequency = 0	I_{SB3}	10	18	18	18	18	mA	12, 13
Clock Running	Device deselected; all inputs ≤ V_{IL} OR ≥ V_{IH}; Vcc = MAX; CLK cycle time ≥ ^tKC min	I_{SB4}	20	35	35	30	25	mA	12, 13

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	3	4	pF	4
Input/Output Capacitance (DQ)	V_{CC} = 3.3V	C_O	5	6	pF	4

THERMAL CONSIDERATIONS

DESCRIPTION	CONDITIONS	SYMBOL	PLCC TYP	TQFP TYP	UNITS	NOTES
Thermal resistance - Junction to Ambient	Still Air	θ_{JA}	45	65	°C/W	
Thermal resistance - Junction to Case		θ_{JC}	15	6	°C/W	
Maximum Case Temperature		TC	110	110	°C	11

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) ($0°C \le T_A \le 70°C$; $V_{CC} = 3.3V \pm 5\%$)

		-7		-10		-12		-15			
DESCRIPTION	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Clock											
Clock cycle time	^tKC	15		20		25		30		ns	
Clock HIGH time	^tKH	5		7		9		11		ns	
Clock LOW time	^tKL	5		7		9		11		ns	
Output Times											
Clock to output valid	^tKQ		7		10		12		15	ns	
Clock to output invalid	^tKQX	3		3		3		3		ns	
Clock to output in Low-Z	^tKQLZ	2		2		2		2		ns	6, 7
Clock to output in High-Z	^tKQHZ		5		6		6		6	ns	6, 7
$\overline{OE}$ to output valid	^tOEQ		5		6		7		8	ns	9
$\overline{OE}$ to output in Low-Z	^tOELZ	0		0		0		0		ns	6, 7
$\overline{OE}$ to output in High-Z	^tOEHZ		5		6		6		6	ns	6, 7
Setup Times											
Address	^tAS	2.5		3		3		3		ns	8, 10
Address Status ($\overline{ADSC}$, $\overline{ADSP}$)	^tADSS	2.5		3		3		3		ns	8, 10
Address Advance ($\overline{ADV}$)	^tAAS	2.5		3		3		3		ns	8, 10
Byte Write Enables ($\overline{WEH}$, $\overline{WEL}$)	^tWS	2.5		3		3		3		ns	8, 10
Data-in	^tDS	2.5		3		3		3		ns	8, 10
Chip Enable ($\overline{CE}$)	^tCES	2.5		3		3		3		ns	8, 10
Hold Times											
Address	^tAH	0.5		0.5		0.5		0.5		ns	8, 10
Address Status ($\overline{ADSC}$, $\overline{ADSP}$)	^tADSH	0.5		0.5		0.5		0.5		ns	8, 10
Address Advance ($\overline{ADV}$)	^tAAH	0.5		0.5		0.5		0.5		ns	8, 10
Byte Write Enables ($\overline{WEH}$, $\overline{WEL}$)	^tWH	0.5		0.5		0.5		0.5		ns	8, 10
Data-in	^tDH	0.5		0.5		0.5		0.5		ns	8, 10
Chip Enable ($\overline{CE}$)	^tCEH	0.5		0.5		0.5		0.5		ns	8, 10

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	1.5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

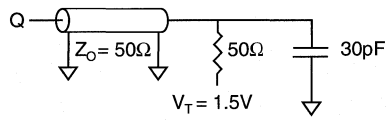


Fig. 1 OUTPUT LOAD EQUIVALENT

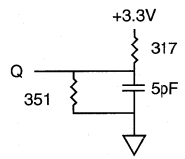
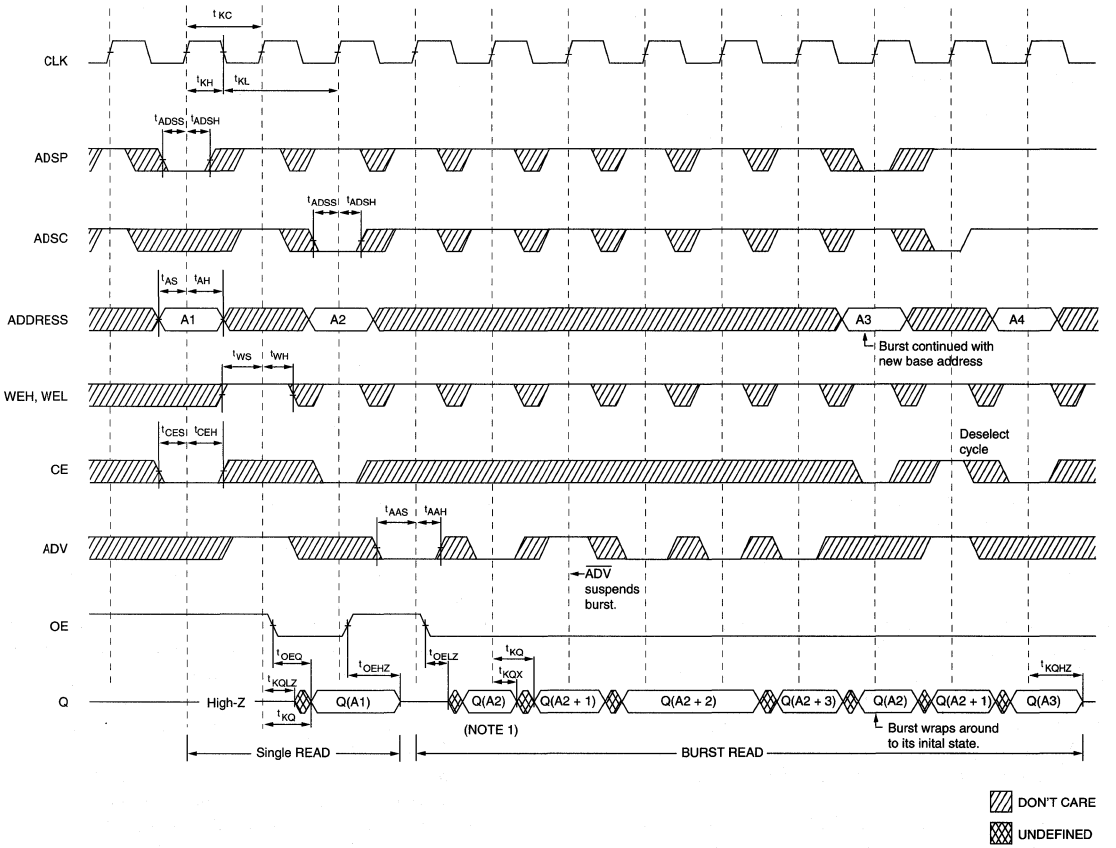


Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

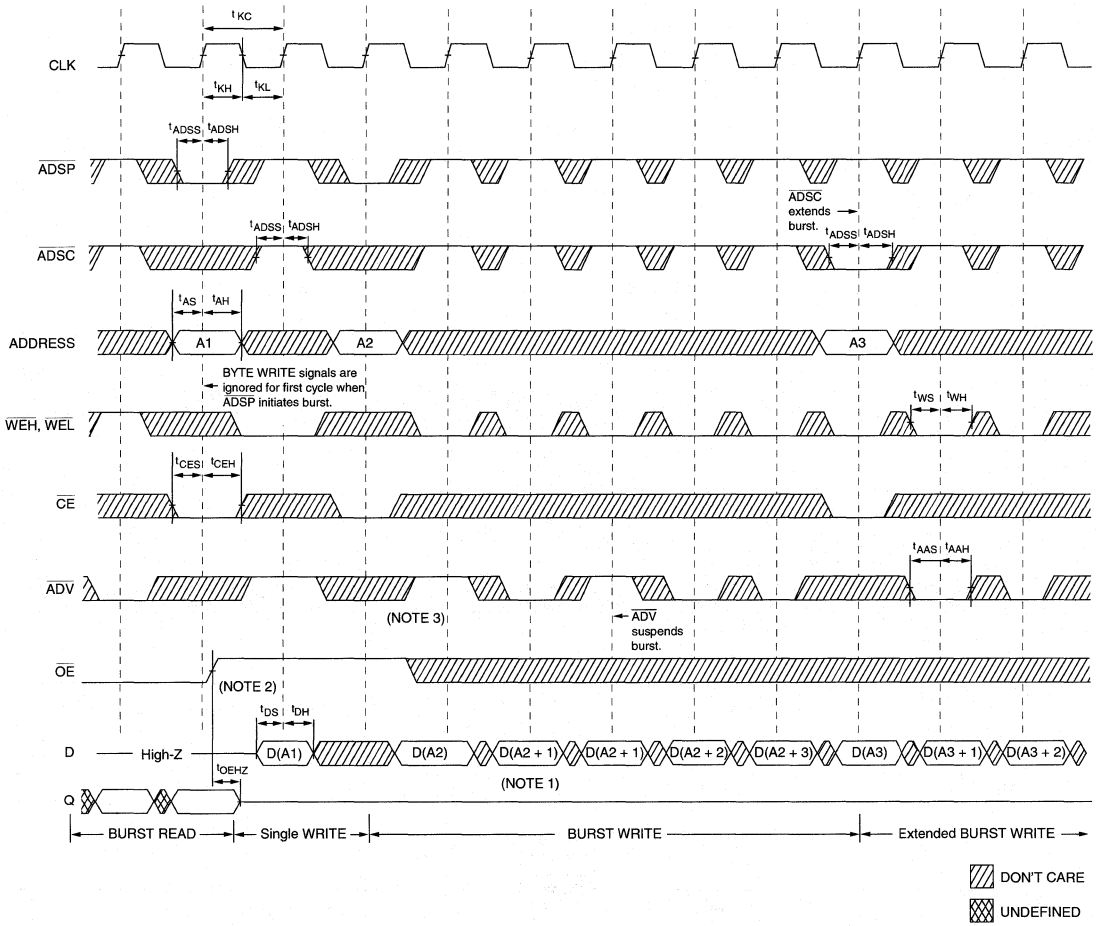
1. All voltages referenced to Vss (GND).
2. Overshoot: $V_{IH} \leq +6.0V$ for $t \leq {}^tKC/2$.
   Undershoot: $V_{IL} \geq -2.0V$ for $t \leq {}^tKC/2$.
   Power-up: $V_{IH} \leq +6.0V$ and $Vcc \leq 3.1V$ for $t \leq 200msec$.
3. Icc is given with no output current. Icc increases with greater output loading and faster cycle times.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. Output loading is specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ${}^tKQHZ$ is less than ${}^tKQLZ$ and ${}^tOEHZ$ is less than ${}^tOELZ$.
8. A READ cycle is defined by byte write enables all HIGH or $\overline{ADSP}$ LOW for the required setup and hold times. A WRITE cycle is defined by at least one byte write enable LOW and $\overline{ADSP}$ HIGH for the required setup and hold times.
9. $\overline{OE}$ is a "don't care" when a byte write enable is sampled LOW.
10. This is a synchronous device. All addresses must meet the specified setup and hold times for all rising edges of CLK when either $\overline{ADSP}$ or $\overline{ADSC}$ is LOW and chip enabled. All other synchronous inputs must meet the setup and hold times with stable logic levels for all rising edges of clock (CLK) when chip is enabled. Chip enable must be valid at each rising edge of CLK (when either $\overline{ADSP}$ or $\overline{ADSC}$ is LOW) to remain enabled.
11. Micron does not warrant the functionality or reliability of any product in which the case temperature exceeds 110°C. Care should be taken to limit case temperature to acceptable levels.
12. "Device Deselected" means device is in POWER-DOWN mode as defined in the truth table. "Device Selected" means device is active (not in POWER-DOWN mode).
13. Typical values are measured at 3.3V, 25°C and 20ns cycle time.

READ TIMING



NOTE: 1. Q(A2) refers to output from address A2. Q(A2+1) refers to output from the next internal burst address following A2.

WRITE TIMING

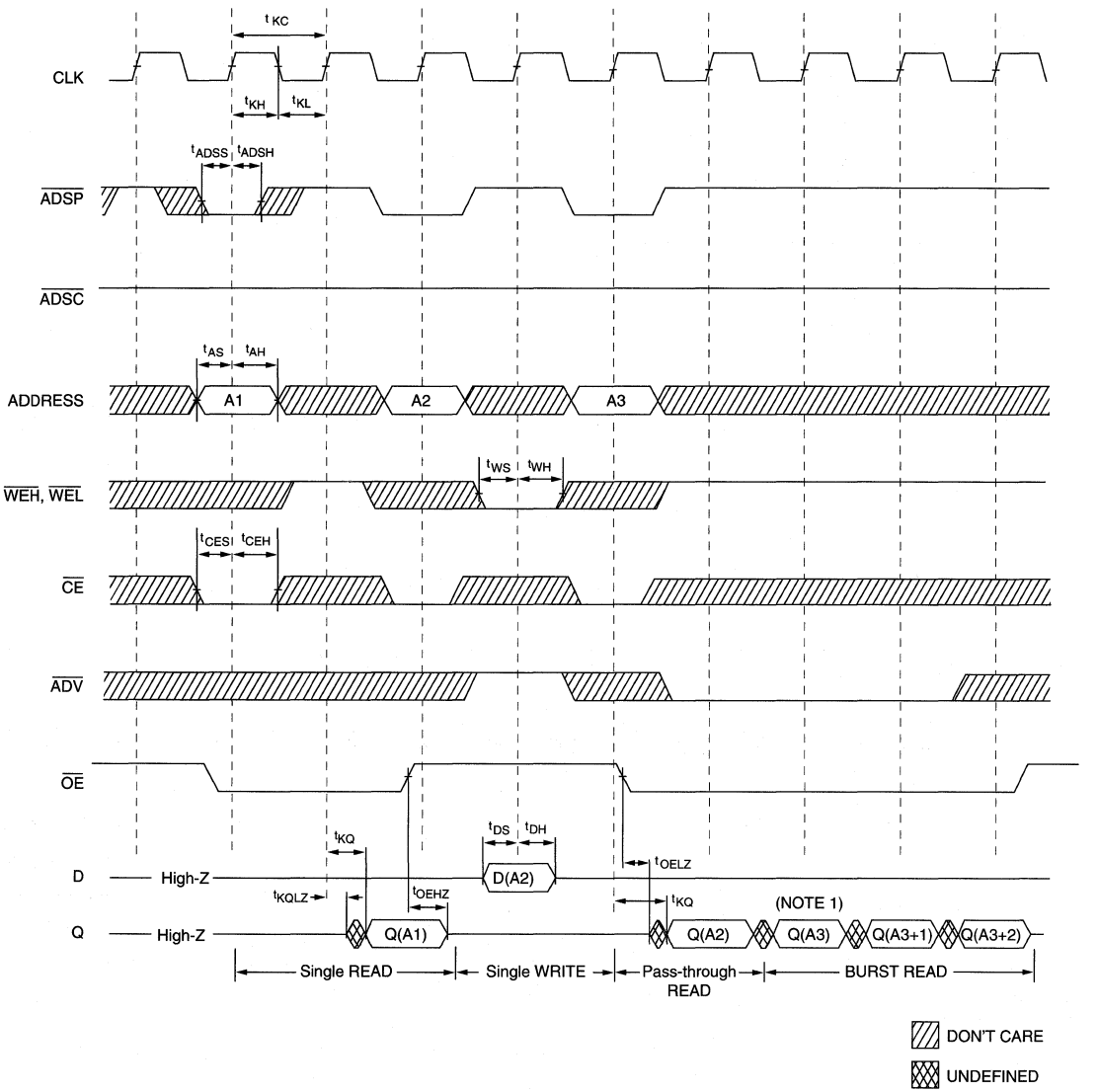


NOTE: 1. D(A2) refers to input to address A2. D(A2+1) refers to input to the next internal burst address following A2.

2. Although a LOW on any one of the byte write inputs will tristate the data outputs, $\overline{OE}$ must be HIGH before the input data setup and held HIGH throughout the the data hold time. This prevents input/output data contention for the time period prior to the byte write enable inputs being latched.

3. $\overline{ADV}$ must be HIGH to permit a WRITE to the loaded address.

READ/WRITE TIMING



NOTE: 1. Q(A2) refers to output from address A2. Q(A2+1) refers to output from the next internal burst address following A2.

APPLICATION EXAMPLE

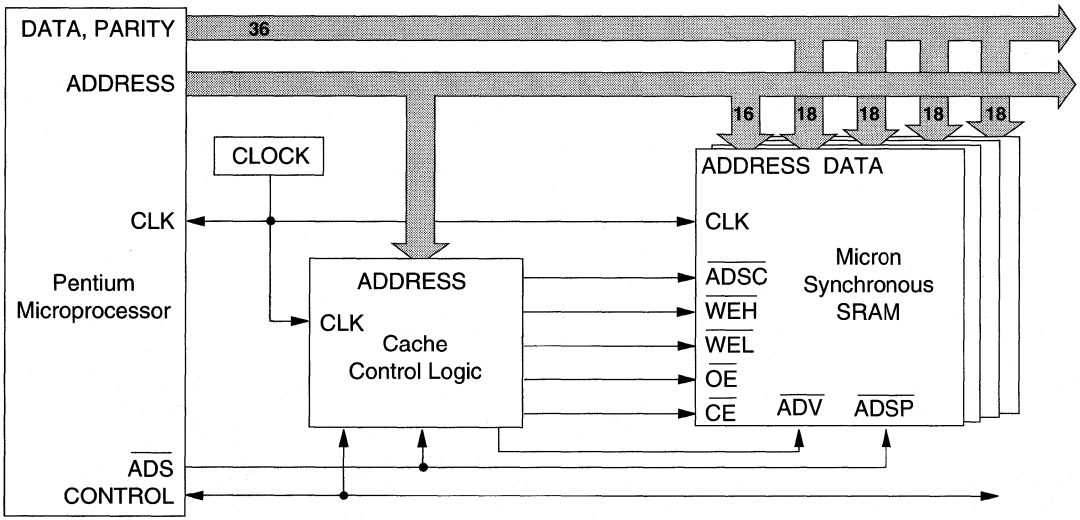


Figure 3
512K BYTE SECONDARY CACHE WITH PARITY AND BURST FOR 50 MHz PENTIUM USING FOUR MT58LC64K18C4EJ-10 SYNCHRONOUS SRAMs

SYNCHRONOUS SRAM

64K x 18 SRAM

+3.3V SUPPLY WITH CLOCKED, REGISTERED INPUTS AND LINEAR BURST COUNTER

NEW 3.3 VOLT SYNCHRONOUS SRAM

FEATURES

- Fast access times: 9, 10, 12 and 17ns
- Fast $\overline{OE}$: 5, 6 and 7ns
- Single +3.3V ±5% power supply
- 5V-tolerant I/O
- Common data inputs and data outputs
- Individual BYTE WRITE control
- Clock controlled, registered, address, data and control
- Internally self-timed WRITE cycle
- Burst control pins (linear burst sequence)
- High density, high-speed packages
- Low capacitive bus loading
- High 30pF output drive capability at rated access time

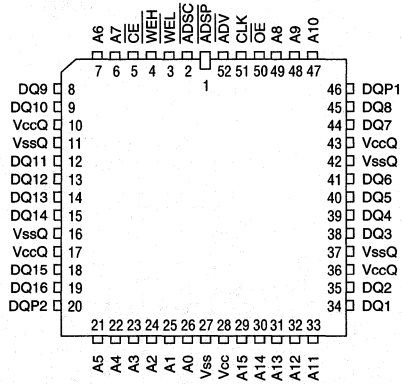
OPTIONS — MARKING

- Timing
  - 9ns access/15ns cycle — -9
  - 10ns access/15ns cycle — -10
  - 12ns access/20ns cycle — -12
  - 17ns access/25ns cycle — -17
- Packages
  - 52-pin PLCC — EJ
  - 100-pin TQFP — LG
- Part Number Example: MT58LC64K18M1EJ-12

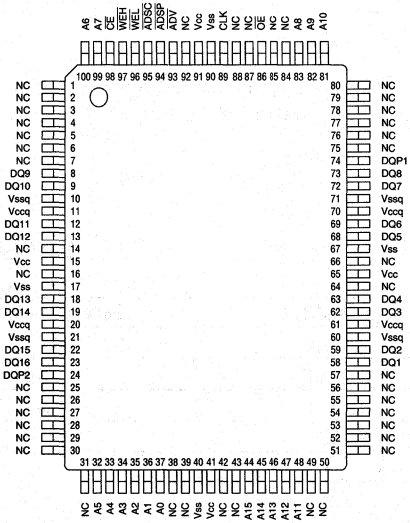
NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

52-Pin PLCC (SB-1)



100-Pin TQFP (SC-1)



GENERAL DESCRIPTION

The Micron Synchronous SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

The MT58LC64K18M1 SRAM integrates a 64K x 18 SRAM core with advanced synchronous peripheral circuitry and a 2-bit burst counter. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input (CLK). The synchronous inputs include all addresses, all data inputs, active LOW chip enable ($\overline{CE}$), burst control inputs ($\overline{ADSC}$, $\overline{ADSP}$, $\overline{ADV}$) and byte write enables ($\overline{WEH}$, $\overline{WEL}$).

Asynchronous inputs include the output enable ($\overline{OE}$) and the clock (CLK). The data-out (Q), enabled by $\overline{OE}$, is also asynchronous. WRITE cycles can be from one to two bytes wide as controlled by the byte write enables.

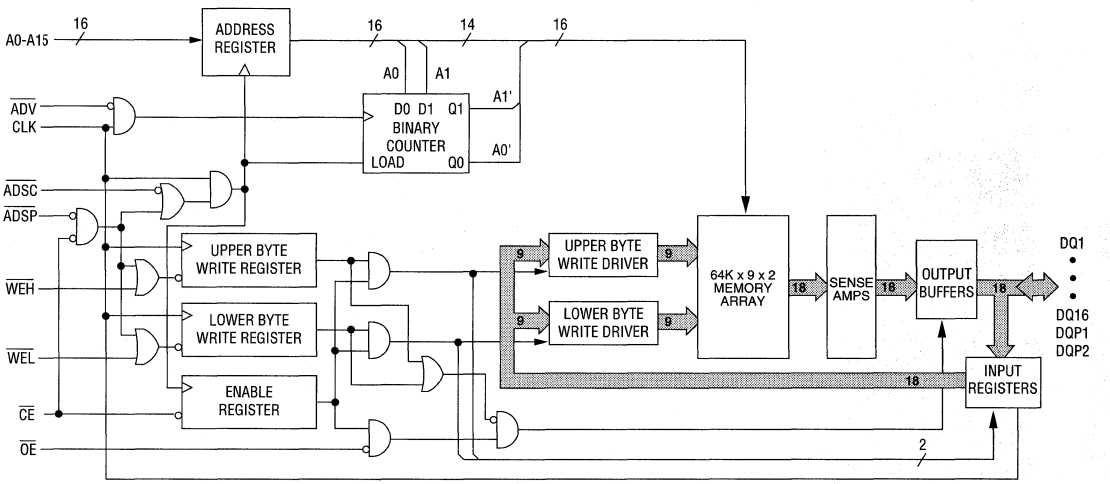
GENERAL DESCRIPTION (continued)

Burst operation can be initiated with either address status processor ($\overline{ADSP}$) or address status controller ($\overline{ADSC}$) input pins. Subsequent burst addresses can be internally generatedas controlled by the burst advance pin ($\overline{ADV}$).

Address and write control are registered on-chip to simplify WRITE cycles. This allows self-timed WRITE cycles. Individual byte enables allow individual bytes to be written. $\overline{WEL}$ controls DQ1-DQ8 and DQP1. $\overline{WEH}$ controls DQ9-DQ16 and DQP2.

The MT58LC64K18M1 operates from a +3.3V power supply and all inputs and outputs are TTL-compatible and 5V tolerant. The device is ideally suited for PowerPC™ and 680X0 systems and those systems which benefit from a wide synchronous data bus.

FUNCTIONAL BLOCK DIAGRAM



NOTE: The Functional Block Diagram illustrates simplified device operation. See Truth Table, pin descriptions and timing diagrams for detailed information.

BURST ADDRESS TABLE

First Address	Second Address	Third Address	Fourth Address
X...X00	X...X01	X...X10	X...X11
X...X01	X...X10	X...X11	X...X00
X...X10	X...X11	X...X00	X...X01
X...X11	X...X00	X...X01	X...X10

PIN DESCRIPTIONS

PLCC PINS	TQFP PINS	SYMBOL	TYPE	DESCRIPTION
26, 25, 24, 23, 22, 21, 7, 6, 49, 48, 47, 33, 32, 31, 30, 29	37, 36, 35, 34, 33, 32, 100, 99, 83, 82, 81, 48, 47, 46, 45, 44	A0-A15	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK.
4, 3	97, 96	$\overline{WEH}$, $\overline{WEL}$	Input	Synchronous Byte Write Enables: These active LOW inputs allow individual bytes to be written and must meet the setup and hold times around the rising edge of CLK. A byte write enable is LOW for a WRITE cycle and HIGH for a READ cycle. $\overline{WEL}$ controls DQ1-DQ8 and DQP1. $\overline{WEH}$ controls DQ9-DQ16 and DQP2. Data I/O are tristated if either of these inputs are LOW.
51	89	CLK	Input	Clock: This signal registers the address, data, chip enable, byte write enables and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
5	98	$\overline{CE}$	Input	Synchronous Chip Enable: This active LOW input is used to enable the device. This input is sampled only when a new external address is loaded.
50	86	$\overline{OE}$	Input	Output Enable: This active LOW asynchronous input enables the data I/O output drivers.
52	93	$\overline{ADV}$	Input	Synchronous Address Advance: This active LOW input is used to advance the internal burst counter, controlling burst access after the external address is loaded. A HIGH on this pin effectively causes wait states to be generated (no address advance). This pin must be HIGH at the rising edge of the first clock after an $\overline{ADSP}$ cycle is initiated if a WRITE cycle is desired (to ensure use of correct address).
1	94	$\overline{ADSP}$	Input	Synchronous Address Status Processor: This active LOW input interrupts any ongoing burst, causing a new external address to be registered. A READ is performed using the new address, independent of the byte write enables and $\overline{ADSC}$ but dependent upon $\overline{CE}$ being LOW.
2	95	$\overline{ADSC}$	Input	Synchronous Address Status Controller: This active LOW input interrupts any ongoing burst, causing a new external address to be registered. A READ or WRITE is performed using the new address if $\overline{CE}$ is LOW. $\overline{ADSC}$ is also used to place the chip into power down state when $\overline{CE}$ is HIGH.
34, 35, 38, 39, 40, 41, 44, 45, 8, 9, 12, 13, 14, 15, 18, 19	58, 59, 62, 63, 68, 69, 72, 73, 8, 9, 12, 13, 18, 19, 22, 23	DQ1-DQ16	Input/ Output	SRAM Data I/O: Low Byte is DQ1-DQ8. High Byte is DQ9-DQ16. Input data must meet setup and hold times around the rising edge of CLK.
46, 20	74, 24	DQP1, DQP2	Input/ Output	Parity Data I/O: Low Byte Parity is DQP1. High Byte Parity is DQP2.
28	15, 41, 65, 91	Vcc	Supply	Power Supply: +3.3V ±5%
27	17, 40, 67, 90	Vss	Supply	Ground: GND
10, 17, 36, 43	11, 20, 61, 71	VccQ	Supply	Isolated Output Buffer Supply: +3.3V ±5%

PIN DESCRIPTIONS (continued)

PLCC PINS	TQFP PINS	SYMBOL	TYPE	DESCRIPTION
11, 16, 37, 42	10, 21, 60, 71	VssQ	Supply	Isolated Output Buffer Ground: GND
	1, 2, 3, 4, 5, 6, 7, 14, 16, 25, 26, 27, 28, 29, 30, 31, 38, 39, 42, 43, 49, 50, 51, 52, 53, 54, 55, 56, 57, 64, 66, 75, 76, 77, 78, 79, 80, 84, 85, 87, 88, 92	NC	-	No Connect: These signals are not internally connected. These signals may be connected to ground to improve package heat dissipation.

TRUTH TABLE

OPERATION	ADDRESS USED	$\overline{CE}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Deselected Cycle, Power-down	None	H	X	L	X	X	X	L-H	High-Z
READ Cycle, Begin Burst	External	L	L	X	X	X	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	X	X	X	H	L-H	High-Z
WRITE Cycle, Begin Burst	External	L	H	L	X	L	X	L-H	D
READ Cycle, Begin Burst	External	L	H	L	X	H	L	L-H	Q
READ Cycle, Begin Burst	External	L	H	L	X	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	X	H	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	X	H	H	L	H	H	L-H	High-Z
WRITE Cycle, Continue Burst	Next	X	H	H	L	L	X	L-H	D
READ Cycle, Continue Burst	Next	H	X	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	H	X	H	L	H	H	L-H	High-Z
WRITE Cycle, Continue Burst	Next	H	X	H	L	L	X	L-H	D
READ Cycle, Suspend Burst	Current	X	H	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	X	H	H	H	H	H	L-H	High-Z
WRITE Cycle, Suspend Burst	Current	X	H	H	H	L	X	L-H	D
READ Cycle, Suspend Burst	Current	H	X	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	H	X	H	H	H	H	L-H	High-Z
WRITE Cycle, Suspend Burst	Current	H	X	H	H	L	X	L-H	D

NOTE:
1. X means "don't care." H means logic HIGH. L means logic LOW. $\overline{WRITE}$=L means any one or more byte write enable signals ($\overline{WEH}$, $\overline{WEL}$) are LOW. $\overline{WRITE}$=H means all byte write enable signals are HIGH.
2. $\overline{WEL}$ enables writes to DQ1-DQ8 and DQP1. $\overline{WEH}$ enables writes to DQ9-DQ16 and DQP2.
3. All inputs except $\overline{OE}$ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
4. Wait states are inserted by suspending burst.
5. For a write operation following a read operation, $\overline{OE}$ must be HIGH before the input data required setup time and held HIGH throughout the input data hold time.
6. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
7. $\overline{ADSP}$ LOW always initiates an internal READ at the L-H edge of CLK. A WRITE is performed by setting one or more byte write enable signal LOW for the subsequent L-H edge of CLK. Refer to WRITE timing diagram for clarification.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to Vss .....-0.5V to +4.6V
V_{IN} .....-0.5V to +6V
Storage Temperature (plastic) .....-55°C to +150°C
Junction Temperature .....+150°C
Power Dissipation 1.6W
Short Circuit Output Current 100mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; T_C ≤ 110°C; V_{CC} = 3.3V ±5% unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.0	5.5	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-1	1	µA	
Output Leakage Current	Output(s) disabled, 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	3.1	3.5	V	1

				MAX					
DESCRIPTION	CONDITIONS	SYMBOL	TYPICAL	-9	-10	-12	-17	UNITS	NOTES
Power Supply Current: Operating	Device selected; all inputs ≤ V_{IL} OR ≥ V_{IH}; cycle time ≥ ^tKC min; Vcc = MAX; outputs open	I_{CC}	150	225	225	200	175	mA	3, 12, 13
Power Supply Current: Idle	Device selected; $\overline{ADSC}$, $\overline{ADSP}$, $\overline{ADV}$ ≥ V_{IH}; all inputs ≤ V_{IL} OR ≥ V_{IH}; Vcc = MAX; cycle time ≥ ^tKC min	I_{SB1}	45	65	65	55	50	mA	12, 13
CMOS Standby	Device deselected; Vcc = MAX; all inputs ≤ Vss +0.2 or ≥ Vcc -0.2; all inputs static; CLK frequency = 0	I_{SB2}	0.2	2	2	2	2	mA	12, 13
TTL Standby	Device deselected; all inputs ≤ V_{IL} OR ≥ V_{IH}; all inputs static; Vcc = MAX; CLK frequency = 0	I_{SB3}	10	18	18	18	18	mA	12, 13
Clock Running	Device deselected; all inputs ≤ V_{IL} OR ≥ V_{IH}; Vcc = MAX; CLK cycle time ≥ ^tKC min	I_{SB4}	20	35	35	30	25	mA	12, 13

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	3	4	pF	4
Input/Output Capacitance (DQ)	V_{CC} = 3.3V	C_O	5	6	pF	4

THERMAL CONSIDERATIONS

DESCRIPTION	CONDITIONS	SYMBOL	PLCC TYP	TQFP TYP	UNITS	NOTES
Thermal resistance - Junction to Ambient	Still Air	θ_{JA}	45	65	°C/W	
Thermal resistance - Junction to Case		θ_{JC}	15	6	°C/W	
Maximum Case Temperature		TC	110	110	°C	11

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) ($0°C \le T_A \le 70°C$; V_{CC} = 3.3V ±5%)

		-9		-10		-12		-17			
DESCRIPTION	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Clock											
Clock cycle time	tKC	15		15		20		25		ns	
Clock HIGH time	tKH	4		5		6		8		ns	
Clock LOW time	tKL	4		5		6		8		ns	
Output Times											
Clock to output valid	tKQ		9		10		12		17	ns	
Clock to output invalid	tKQX	3		3		3		3		ns	
Clock to output in Low-Z	tKQLZ	5		5		5		5		ns	6, 7
Clock to output in High-Z	tKQHZ		5		5		6		6	ns	6, 7
$\overline{OE}$ to output valid	tOEQ		5		5		6		7	ns	9
$\overline{OE}$ to output in Low-Z	tOELZ	0		0		0		0		ns	6, 7
$\overline{OE}$ to output in High-Z	tOEHZ		5		5		6		6	ns	6, 7
Setup Times											
Address	tAS	2.5		3		3		3		ns	8, 10
Address Status ($\overline{ADSC}$, $\overline{ADSP}$)	tADSS	2.5		3		3		3		ns	8, 10
Address Advance ($\overline{ADV}$)	tAAS	2.5		3		3		3		ns	8, 10
Byte Write Enables ($\overline{WEH}$, $\overline{WEL}$)	tWS	2.5		3		3		3		ns	8, 10
Data-in	tDS	2.5		3		3		3		ns	8, 10
Chip Enable ($\overline{CE}$)	tCES	2.5		3		3		3		ns	8, 10
Hold Times											
Address	tAH	0.5		0.5		0.5		0.5		ns	8, 10
Address Status ($\overline{ADSC}$, $\overline{ADSP}$)	tADSH	0.5		0.5		0.5		0.5		ns	8, 10
Address Advance ($\overline{ADV}$)	tAAH	0.5		0.5		0.5		0.5		ns	8, 10
Byte Write Enables ($\overline{WEH}$, $\overline{WEL}$)	tWH	0.5		0.5		0.5		0.5		ns	8, 10
Data-in	tDH	0.5		0.5		0.5		0.5		ns	8, 10
Chip Enable ($\overline{CE}$)	tCEH	0.5		0.5		0.5		0.5		ns	8, 10

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	1.5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

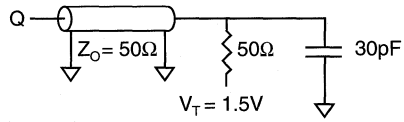


Fig. 1 OUTPUT LOAD EQUIVALENT

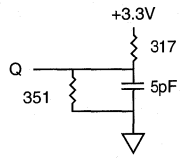


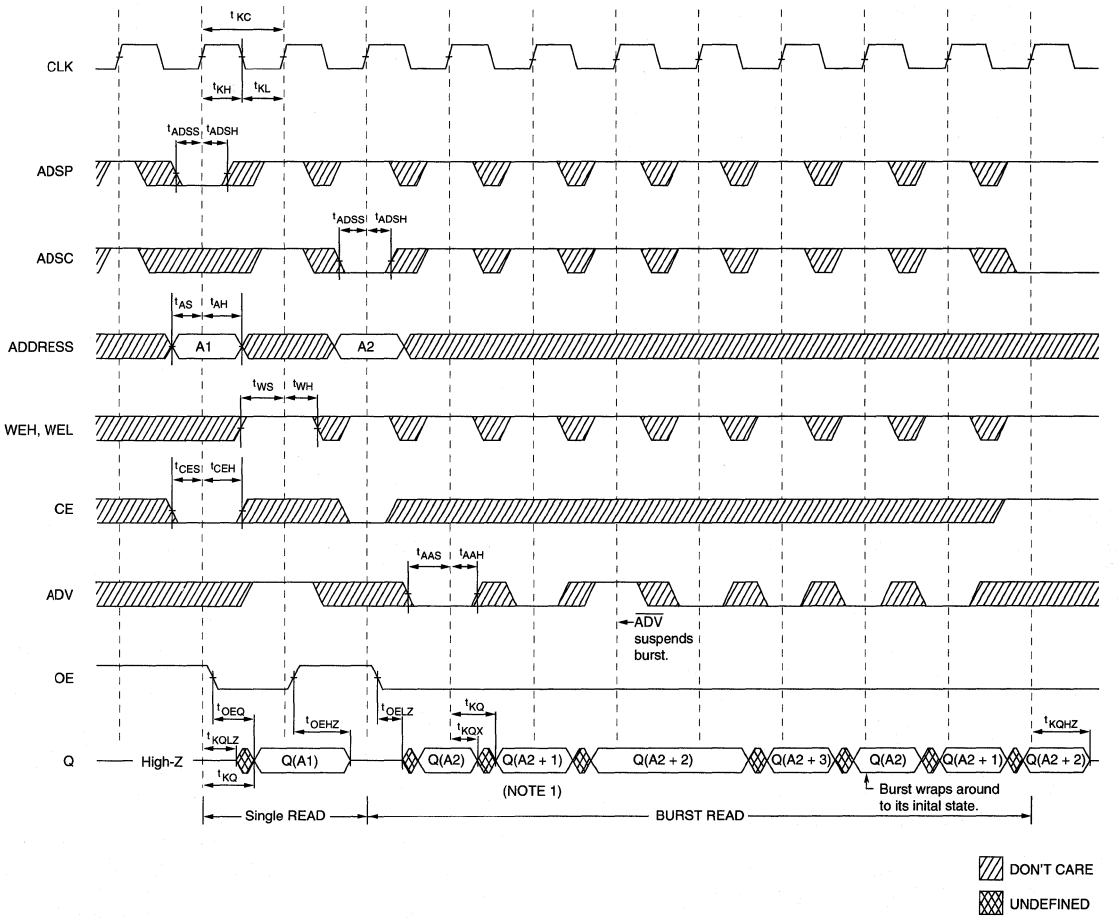
Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

1. All voltages referenced to Vss (GND).
2. Overshoot: $V_{IH} \leq +6.0V$ for $t \leq {}^tKC/2$.
   Undershoot: $V_{IL} \geq -2.0V$ for $t \leq {}^tKC/2$.
   Power-up: $V_{IH} \leq +6.0V$ and $Vcc \leq 3.1V$ for $t \leq 200msec$.
3. Icc is given with no output current. Icc increases with greater output loading and faster cycle times.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. Output loading is specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ${}^tKQHZ$ is less than ${}^tKQLZ$ and ${}^tOEHZ$ is less than ${}^tOELZ$.
8. A READ cycle is defined by byte write enables all HIGH or $\overline{ADSP}$ LOW for the required setup and hold times. A WRITE cycle is defined by at least one byte write enable LOW and $\overline{ADSP}$ HIGH for the required setup and hold times.
9. $\overline{OE}$ is a "don't care" when a byte write enable is sampled LOW.
10. This is a synchronous device. All addresses must meet the specified setup and hold times for all rising edges of CLK when either $\overline{ADSP}$ or $\overline{ADSC}$ is LOW and chip enabled. All other synchronous inputs must meet the setup and hold times with stable logic levels for all rising edges of clock (CLK) when chip is enabled. Chip enable must be valid at each rising edge of CLK (when either $\overline{ADSP}$ or $\overline{ADSC}$ is LOW) to remain enabled.
11. Micron does not warrant the functionality or reliability of any product in which the case temperature exceeds 110°C. Care should be taken to limit case temperature to acceptable levels.
12. "Device Deselected" means device is in POWER-DOWN mode as defined in the truth table. "Device Selected" means device is active (not in POWER-DOWN mode).
13. Typical values are measured at 3.3V, 25°C and 20ns cycle time.

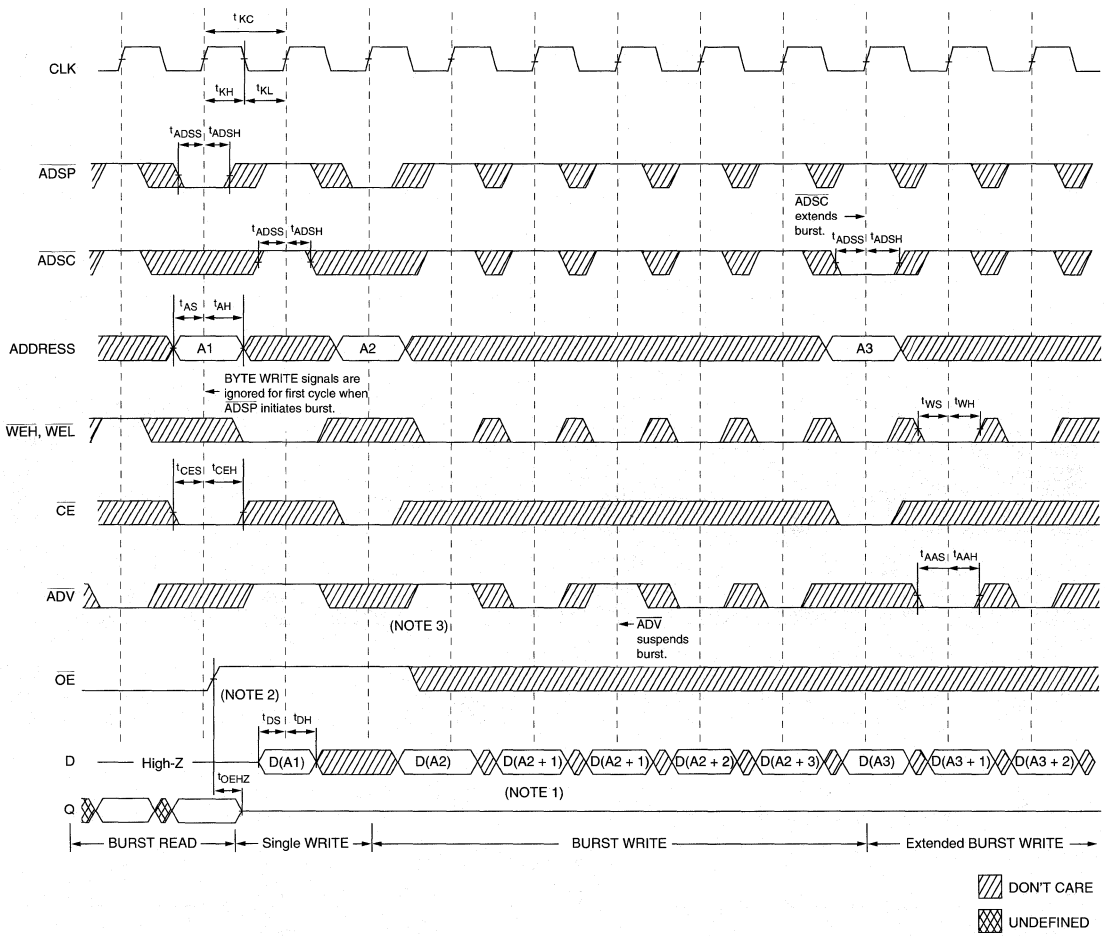
NEW 3.3 VOLT SYNCHRONOUS SRAM

READ TIMING



NOTE: 1. Q(A2) refers to output from address A2. Q(A2+1) refers to output from the next internal burst address following A2.

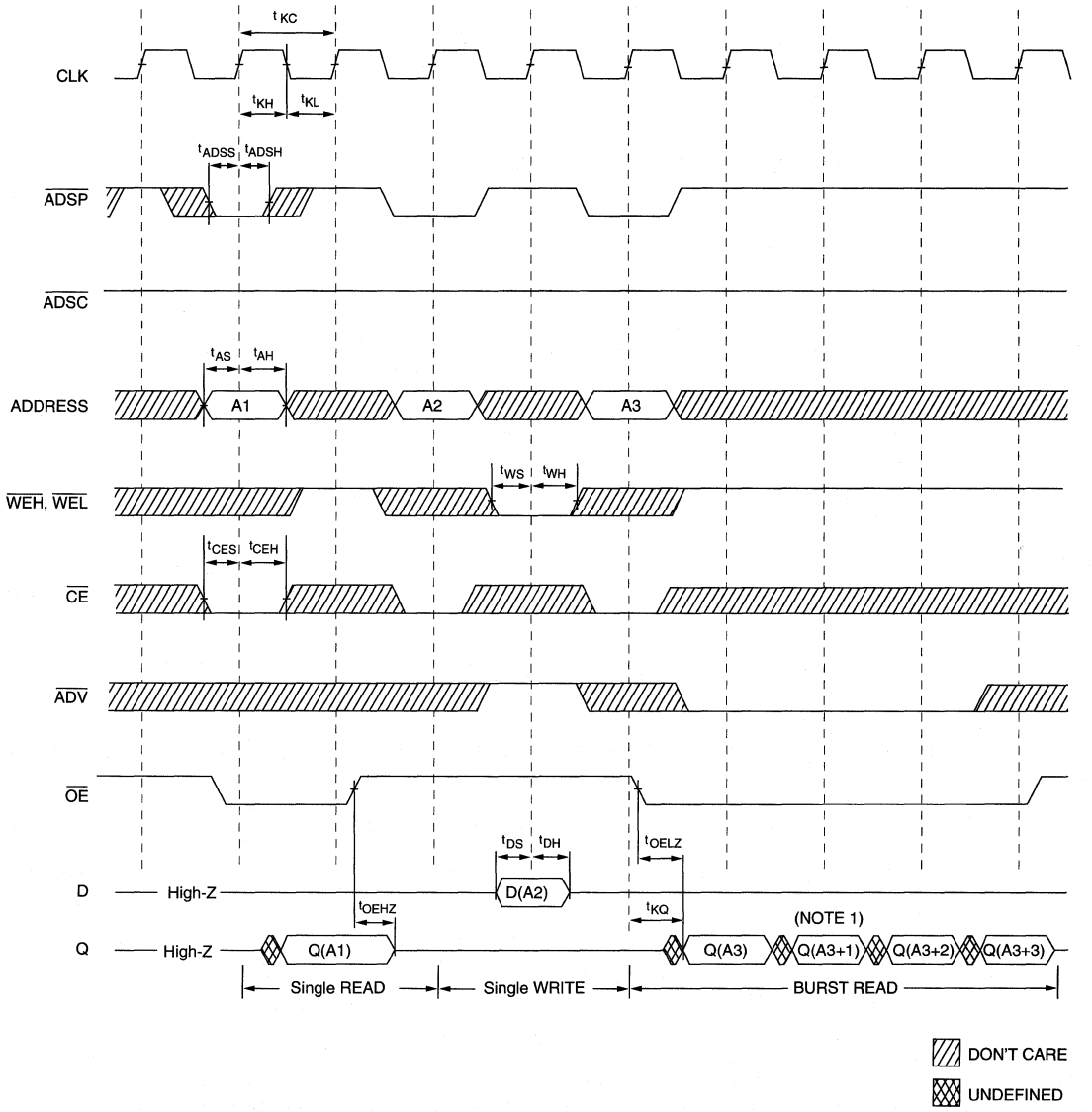
WRITE TIMING



NOTE: 1 D(A2) refers to input to address A2. D(A2+1) refers to input to the next internal burst address following A2.

2. $\overline{OE}$ must be HIGH before the input data setup and held HIGH throughout the the data hold time. This prevents input/output data contention for the time period prior to the byte write enable inputs being sampled.
3. $\overline{ADV}$ must be HIGH to permit a WRITE to the loaded address.

READ/WRITE TIMING



NOTE: 1. Q(A3) refers to output from address A3. Q(A3+1) refers to output from the next internal burst address following A3.

APPLICATION EXAMPLE

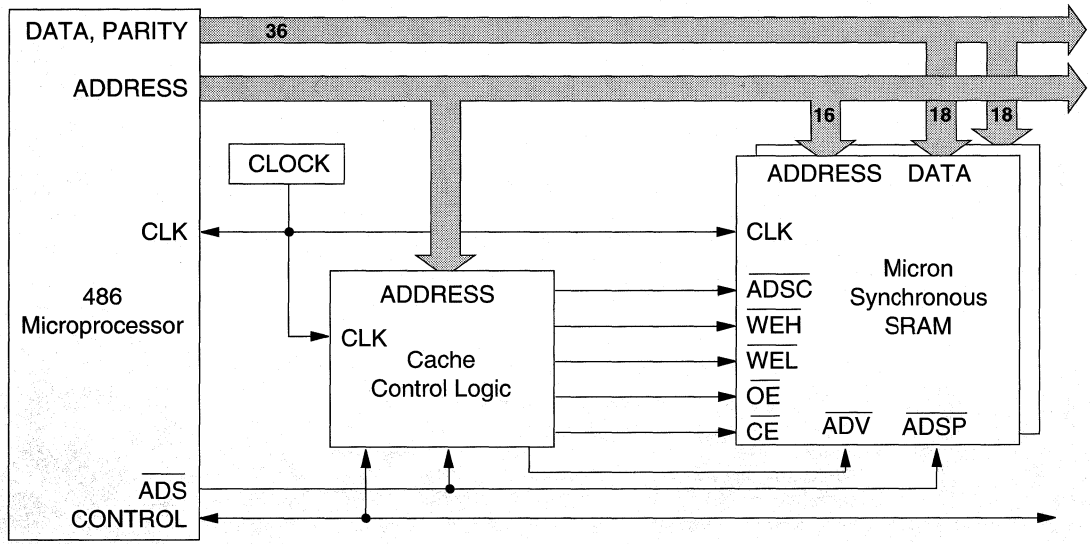


Figure 3
256K BYTE SECONDARY CACHE WITH PARITY AND BURST FOR 50 MHz 80486 OR 680X0 USING TWO MT58LC64K18M1EJ-12 SYNCHRONOUS SRAMs

MICRON SEMICONDUCTOR, INC.

MT58LC64K18M1
64K x 18 SYNCHRONOUS SRAM

MICRON SEMICONDUCTOR, INC.

MT58LC64K18A6
64K x 18 SYNCHRONOUS SRAM

SYNCHRONOUS SRAM

64K x 18 SRAM

+3.3V SUPPLY, FULLY REGISTERED I/O AND LINEAR BURST COUNTER

NEW

3.3 VOLT SYNCHRONOUS SRAM

FEATURES

- Fast access times: 7, 10, 12 and 15ns
- Fast $\overline{OE}$: 5, 6, 7 and 8ns
- Single +3.3V ±5% power supply
- 5V-tolerant I/O
- Common data inputs and data outputs
- Individual BYTE WRITE control
- Clock controlled, registered, address, data I/O and control for fully pipelined applications
- Internally self-timed WRITE cycle
- WRITE pass-through capability
- Burst control pins (linear burst sequence)
- High density, high-speed packages
- Low capacitive bus loading
- High 30pF output drive capability at rated access time

OPTIONS MARKING

- Timing

7ns access/15ns cycle	- 7
10ns access/20ns cycle	-10
12ns access/25ns cycle	-12
15ns access/30ns cycle	-15

- Packages

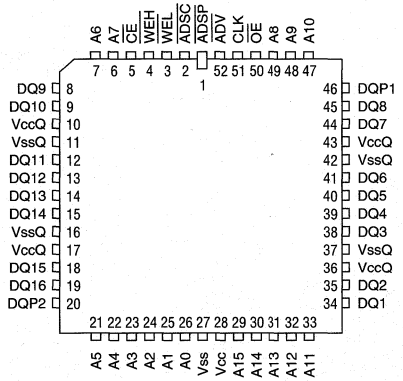
52-pin PLCC	EJ
100-pin TQFP	LG

- Part Number Example: MT58LC64K18A6EJ-10

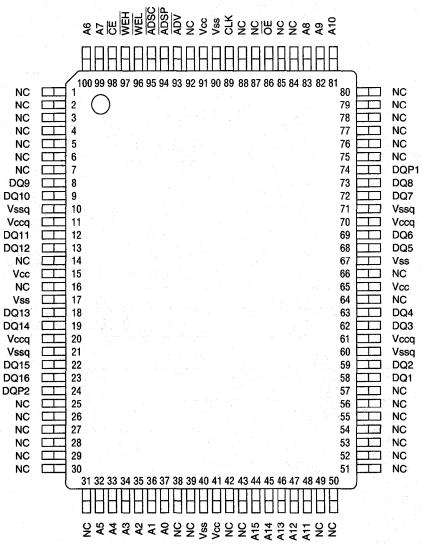
NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

52-Pin PLCC
(SB-1)



100-Pin TQFP
(SC-1)



GENERAL DESCRIPTION

The Micron Synchronous SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

The MT58LC64K18A6 SRAM integrates a 64K x 18 SRAM core with advanced synchronous peripheral circuitry, a 2-bit burst counter and output register. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input (CLK). The synchronous inputs include all addresses, all data inputs, active LOW chip enable ($\overline{CE}$), burst control inputs ($\overline{ADSC}$, $\overline{ADSP}$, $\overline{ADV}$) and the byte write enables ($\overline{WEH}$, $\overline{WEL}$).

GENERAL DESCRIPTION (continued)

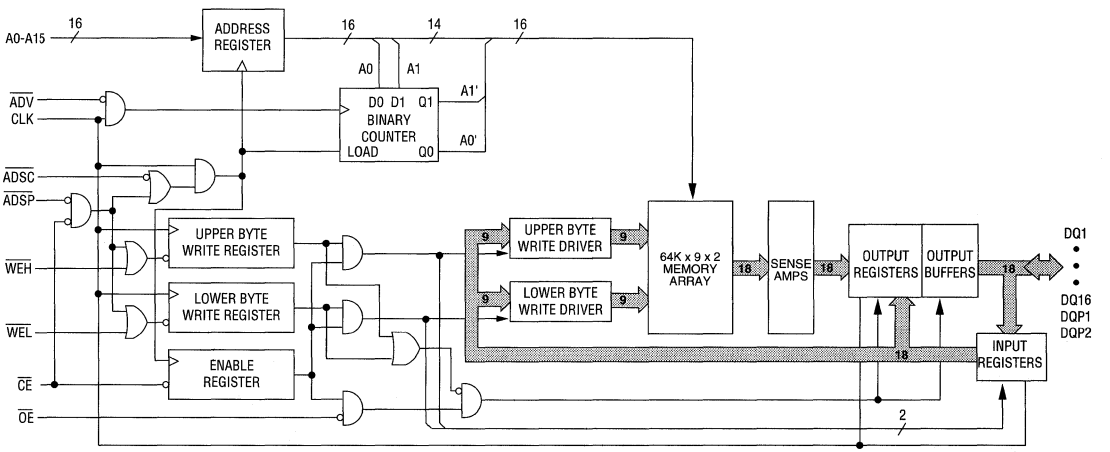
Asynchronous inputs include the output enable ($\overline{OE}$) and the clock (CLK). The data-out (Q), enabled by $\overline{OE}$, is also asynchronous. The output register is controlled by the clock. WRITE cycles can be from one to two bytes wide as controlled by the byte write enables.

Burst operation can be initiated with either address status processor ($\overline{ADSP}$) or address status controller ($\overline{ADSC}$) input pins. Subsequent burst addresses can be internally generated as controlled by the burst advance pin ($\overline{ADV}$).

Address and write control are registered on-chip t simplify WRITE cycles. This allows self-timed WRITE cycles WRITE pass-through makes written data immediatel available at the output register during the READ cycl following a WRITE as controlled solely by $\overline{OE}$ to improv cache system response.

The MT58LC64K18A6 operates from a +3.3V power sup ply and all inputs and outputs are TTL-compatible and 5\ tolerant. The device is ideally suited for PowerPC™ an linear burst pipelined applications.

FUNCTIONAL BLOCK DIAGRAM



NOTE: The Functional Block Diagram illustrates simplified device operation. See Truth Table, pin descriptions and timing diagrams for detailed information.

BURST ADDRESS TABLE

First Address	Second Address	Third Address	Fourth Address
X...X00	X...X01	X...X10	X...X11
X...X01	X...X10	X...X11	X...X00
X...X10	X...X11	X...X00	X...X01
X...X11	X...X00	X...X01	X...X10

PIN DESCRIPTIONS

PLCC PINS	TQFP PINS	SYMBOL	TYPE	DESCRIPTION
26, 25, 24, 23, 22, 21, 7, 6, 49, 48, 47, 33, 32, 31, 30, 29	37, 36, 35, 34, 33, 32, 100, 99, 83, 82, 81, 48, 47, 46, 45, 44	A0-A15	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK.
4, 3	97, 96	$\overline{WEH}$, $\overline{WEL}$	Input	Synchronous Byte Write Enables: These active LOW inputs allow individual bytes to be written and must meet the setup and hold times around the rising edge of CLK. A byte write enable is LOW for a WRITE cycle and HIGH for a READ cycle. $\overline{WEL}$ controls DQ1-DQ8 and DQP1. $\overline{WEH}$ controls DQ9-DQ16 and DQP2. Data I/O are tristated if either of these inputs are LOW.
51	89	CLK	Input	Clock: This signal registers the address, data, chip enable, byte write enables and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
5	98	$\overline{CE}$	Input	Synchronous Chip Enable: This active LOW input is used to enable the device. This input is sampled only when a new external address is loaded.
50	86	$\overline{OE}$	Input	Output Enable: This active LOW asynchronous input enables the Data I/O output drivers.
52	93	$\overline{ADV}$	Input	Synchronous Address Advance: This active LOW input is used to advance the internal burst counter, controlling burst access after the external address is loaded. A HIGH on this pin effectively causes wait states to be generated (no address advance). This pin must be HIGH at the rising edge of the first clock after an $\overline{ADSP}$ cycle is initiated if a WRITE cycle is desired (to ensure use of correct address).
1	94	$\overline{ADSP}$	Input	Synchronous Address Status Processor: This active LOW input interrupts any ongoing burst, causing a new external address to be registered. A READ is performed using the new address, independent of the byte write enables and $\overline{ADSC}$ but dependent upon $\overline{CE}$ being LOW.
2	95	$\overline{ADSC}$	Input	Synchronous Address Status Controller: This active LOW input interrupts any ongoing burst, causing a new external address to be registered. A READ or WRITE is performed using the new address if $\overline{CE}$ is LOW. $\overline{ADSC}$ is also used to place the chip into power-down state when $\overline{CE}$ is HIGH.
34, 35, 38, 39, 40, 41, 44, 45, 8, 9, 12, 13, 14, 15, 18, 19	58, 59, 62, 63, 68, 69, 72, 73, 8, 9, 12, 13, 18, 19, 22, 23	DQ1-DQ16	Input/ Output	SRAM Data I/O: Low Byte is DQ1-DQ8. High Byte is DQ9-DQ16. Input data must meet setup and hold times around the rising edge of CLK.
46, 20	74, 24	DQP1, DQP2	Input/ Output	Parity Data I/O: Low Byte Parity is DQP1. High Byte Parity is DQP2.
28	15, 41, 65, 91	Vcc	Supply	Power Supply: +3.3V ±5%
27	17, 40, 67, 90	Vss	Supply	Ground: GND
10, 17, 36, 43	11, 20, 61, 71	VccQ	Supply	Isolated Output Buffer Supply: +3.3V ±5%

PIN DESCRIPTIONS (continued)

PLCC PINS	TQFP PINS	SYMBOL	TYPE	DESCRIPTION
11, 16, 37, 42	10, 21, 60, 71	VssQ	Supply	Isolated Output Buffer Ground: GND
	1, 2, 3, 4, 5, 6, 7, 14, 16, 25, 26, 27, 28, 29, 30, 31, 38, 39, 42, 43, 49, 50, 51, 52, 53, 54, 55, 56, 57, 64, 66, 75, 76, 77, 78, 79, 80, 84, 85, 87, 88, 92	NC	-	No Connect: These signals are not internally connected. These signals may be connected to ground to improve package heat dissipation.

TRUTH TABLE

OPERATION	ADDRESS USED	$\overline{CE}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Deselected Cycle, Power-down	None	H	X	L	X	X	X	L-H	High-Z
READ Cycle, Begin Burst	External	L	L	X	X	X	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	X	X	X	H	L-H	High-Z
WRITE Cycle, Begin Burst	External	L	H	L	X	L	X	L-H	D
READ Cycle, Begin Burst	External	L	H	L	X	H	L	L-H	Q
READ Cycle, Begin Burst	External	L	H	L	X	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	X	H	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	X	H	H	L	H	H	L-H	High-Z
WRITE Cycle, Continue Burst	Next	X	H	H	L	L	X	L-H	D
READ Cycle, Continue Burst	Next	H	X	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	H	X	H	L	H	H	L-H	High-Z
WRITE Cycle, Continue Burst	Next	H	X	H	L	L	X	L-H	D
READ Cycle, Suspend Burst	Current	X	H	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	X	H	H	H	H	H	L-H	High-Z
WRITE Cycle, Suspend Burst	Current	X	H	H	H	L	X	L-H	D
READ Cycle, Suspend Burst	Current	H	X	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	H	X	H	H	H	H	L-H	High-Z
WRITE Cycle, Suspend Burst	Current	H	X	H	H	L	X	L-H	D

NOTE:
1. X means "don't care." H means logic HIGH. L means logic LOW. $\overline{WRITE}$=L means any one or more byte write enable signals ($\overline{WEH}$, $\overline{WEL}$) are LOW. $\overline{WRITE}$=H means all byte write enable signals are HIGH.
2. $\overline{WEL}$ enables writes to DQ1-DQ8 and DQP1. $\overline{WEH}$ enables writes to DQ9-DQ16 and DQP2.
3. All inputs except $\overline{OE}$ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
4. Wait states are inserted by suspending burst.
5. For a write operation following a read operation, $\overline{OE}$ must be HIGH before the input data required setup time and held HIGH throughout the input data hold time.
6. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
7. $\overline{ADSP}$ LOW always initiates an internal READ at the L-H edge of CLK. A WRITE is performed by setting one or more byte write enable signal LOW for the subsequent L-H edge of CLK. Refer to WRITE timing diagram for clarification.

PASS-THROUGH TRUTH TABLE

PREVIOUS CYCLE		PRESENT CYCLE				NEXT CYCLE
OPERATION	$\overline{WE}$s	OPERATION	$\overline{CE}$	$\overline{WE}$s	$\overline{OE}$	OPERATION
Initiate WRITE cycle, all bytes Address = A(n-1); data = D(n-1)	All L	Initiate READ cycle Register A(n), Q = D(n-1)	L	H	L	Read D(n)
Initiate WRITE cycle, all bytes Address = A(n-1); data = D(n-1)	All L	No new cycle Q = D(n-1)	H	H	L	No carryover from previous cycle
Initiate WRITE cycle, all bytes Address = A(n-1); data = D(n-1)	All L	No new cycle Q = HIGH-Z	H	H	H	No carryover from previous cycle
Initiate WRITE cycle, one byte Address = A(n-1); data = D(n-1)	One L	No new cycle Q = D(n-1) for one byte	H	H	L	No carryover from previous cycle

NOTE: Previous cycle may be either BURST or NONBURST cycle.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to Vss .....-0.5V to +4.6V
V_{IN} .....-0.5V to +6V
Storage Temperature (plastic) .....-55°C to +150°C
Junction Temperature .....+150°C
Power Dissipation 1.6W
Short Circuit Output Current 100mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; T_C ≤ 110°C; V_{CC} = 3.3V ±5% unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.0	5.5	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-1	1	µA	
Output Leakage Current	Output(s) disabled, 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	3.1	3.5	V	1

				MAX					
DESCRIPTION	CONDITIONS	SYMBOL	TYPICAL	-7	-10	-12	-17	UNITS	NOTES
Power Supply Current: Operating	Device selected; all inputs ≤ V_{IL} OR ≥ V_{IH}; cycle time ≥ ^tKC min; Vcc = MAX; outputs open	I_{CC}	150	225	200	175	160	mA	3, 12, 13
Power Supply Current: Idle	Device selected; $\overline{ADSC}$, $\overline{ADSP}$, $\overline{ADV}$ ≥ V_{IH}; all inputs ≤ V_{IL} OR ≥ V_{IH}; Vcc = MAX; cycle time ≥ ^tKC min	I_{SB1}	45	65	55	50	45	mA	12, 13
CMOS Standby	Device deselected; Vcc = MAX; all inputs ≤ Vss +0.2 or ≥ Vcc -0.2; all inputs static; CLK frequency = 0	I_{SB2}	0.2	2	2	2	2	mA	12, 13
TTL Standby	Device deselected; all inputs ≤ V_{IL} OR ≥ V_{IH}; all inputs static; Vcc = MAX; CLK frequency = 0	I_{SB3}	10	18	18	18	18	mA	12, 13
Clock Running	Device deselected; all inputs ≤ V_{IL} OR ≥ V_{IH}; Vcc = MAX; CLK cycle time ≥ ^tKC min	I_{SB4}	20	35	35	30	25	mA	12, 13

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	3	4	pF	4
Input/Output Capacitance (DQ)	V_{CC} = 3.3V	C_O	5	6	pF	4

THERMAL CONSIDERATIONS

DESCRIPTION	CONDITIONS	SYMBOL	PLCC TYP	TQFP TYP	UNITS	NOTES
Thermal resistance - Junction to Ambient	Still Air	θ_{JA}	45	65	°C/W	
Thermal resistance - Junction to Case		θ_{JC}	15	6	°C/W	
Maximum Case Temperature		TC	110	110	°C	11

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) ($0°C \le T_A \le 70°C$; Vcc = 3.3V ±5%)

		-7		-10		-12		-15			
DESCRIPTION	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Clock											
Clock cycle time	tKC	15		20		25		30		ns	
Clock HIGH time	tKH	5		7		9		11		ns	
Clock LOW time	tKL	5		7		9		11		ns	
Output Times											
Clock to output valid	tKQ		7		10		12		15	ns	
Clock to output invalid	tKQX	3		3		3		3		ns	
Clock to output in Low-Z	tKQLZ	2		2		2		2		ns	6, 7
Clock to output in High-Z	tKQHZ		5		6		6		6	ns	6, 7
$\overline{OE}$ to output valid	tOEQ		5		6		7		8	ns	9
$\overline{OE}$ to output in Low-Z	tOELZ	0		0		0		0		ns	6, 7
$\overline{OE}$ to output in High-Z	tOEHZ		5		6		6		6	ns	6, 7
Setup Times											
Address	tAS	2.5		3		3		3		ns	8, 10
Address Status ($\overline{ADSC}$, $\overline{ADSP}$)	tADSS	2.5		3		3		3		ns	8, 10
Address Advance ($\overline{ADV}$)	tAAS	2.5		3		3		3		ns	8, 10
Byte Write Enables ($\overline{WEH}$, $\overline{WEL}$)	tWS	2.5		3		3		3		ns	8, 10
Data-in	tDS	2.5		3		3		3		ns	8, 10
Chip Enable ($\overline{CE}$)	tCES	2.5		3		3		3		ns	8, 10
Hold Times											
Address	tAH	0.5		0.5		0.5		0.5		ns	8, 10
Address Status ($\overline{ADSC}$, $\overline{ADSP}$)	tADSH	0.5		0.5		0.5		0.5		ns	8, 10
Address Advance ($\overline{ADV}$)	tAAH	0.5		0.5		0.5		0.5		ns	8, 10
Byte Write Enables ($\overline{WEH}$, $\overline{WEL}$)	tWH	0.5		0.5		0.5		0.5		ns	8, 10
Data-in	tDH	0.5		0.5		0.5		0.5		ns	8, 10
Chip Enable ($\overline{CE}$)	tCEH	0.5		0.5		0.5		0.5		ns	8, 10

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	1.5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

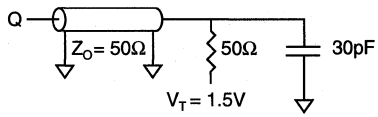


Fig. 1 OUTPUT LOAD EQUIVALENT

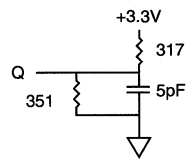
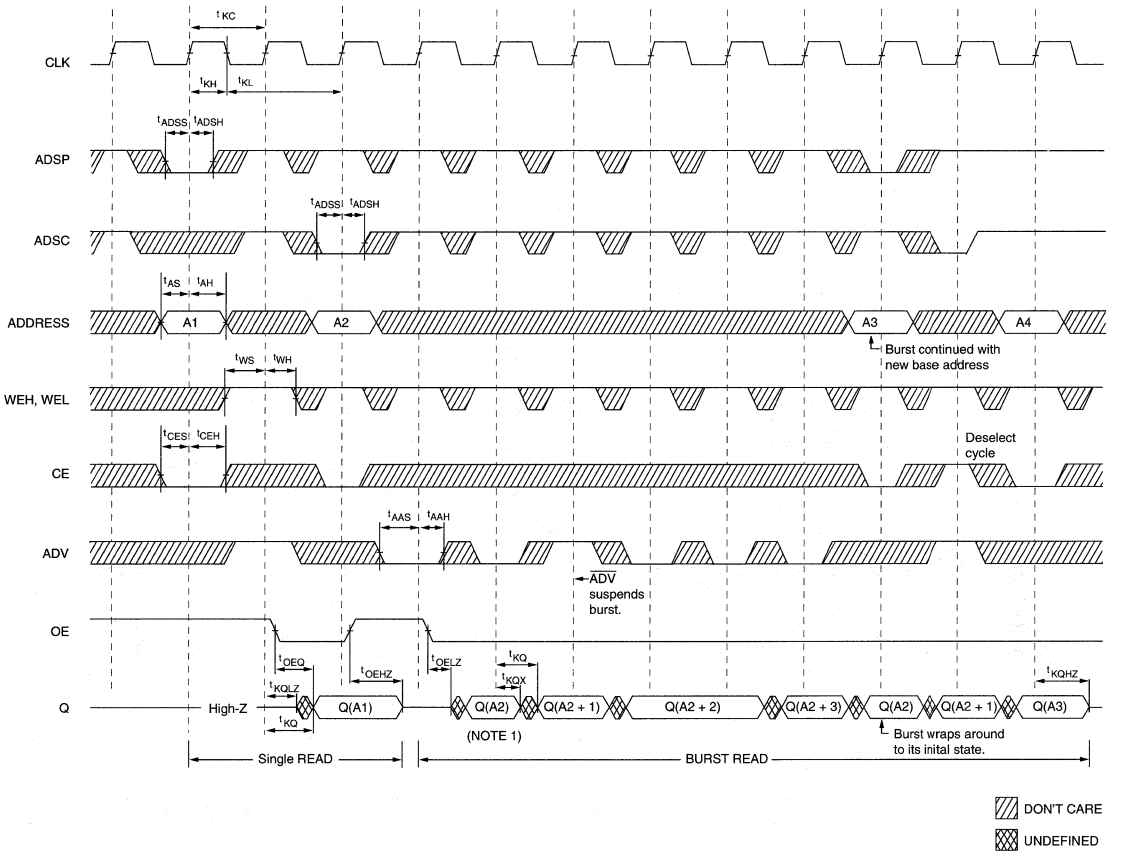


Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

1. All voltages referenced to Vss (GND).
2. Overshoot: $V_{IH} \leq +6.0V$ for $t \leq {}^tKC/2$.
   Undershoot: $V_{IL} \geq -2.0V$ for $t \leq {}^tKC/2$.
   Power-up: $V_{IH} \leq +6.0V$ and $Vcc \leq 3.1V$ for $t \leq 200msec$.
3. Icc is given with no output current. Icc increases with greater output loading and faster cycle times.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. Output loading is specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ${}^tKQHZ$ is less than ${}^tKQLZ$ and ${}^tOEHZ$ is less than ${}^tOELZ$.
8. A READ cycle is defined by byte write enables all HIGH or $\overline{ADSP}$ LOW for the required setup and hold times. A WRITE cycle is defined by at least one byte write enable LOW and $\overline{ADSP}$ HIGH for the required setup and hold times.
9. $\overline{OE}$ is a "don't care" when a byte write enable is sampled LOW.
10. This is a synchronous device. All addresses must meet the specified setup and hold times for all rising edges of CLK when either $\overline{ADSP}$ or $\overline{ADSC}$ is LOW and chip enabled. All other synchronous inputs must meet the setup and hold times with stable logic levels for all rising edges of clock (CLK) when chip is enabled. Chip enable must be valid at each rising edge of CLK (when either $\overline{ADSP}$ or $\overline{ADSC}$ is LOW) to remain enabled.
11. Micron does not warrant the functionality or reliability of any product in which the case temperature exceeds 110°C. Care should be taken to limit case temperature to acceptable levels.
12. "Device Deselected" means device is in POWER-DOWN mode as defined in the truth table. "Device Selected" means device is active (not in POWER-DOWN mode).
13. Typical values are measured at 3.3V, 25°C and 20ns cycle time.

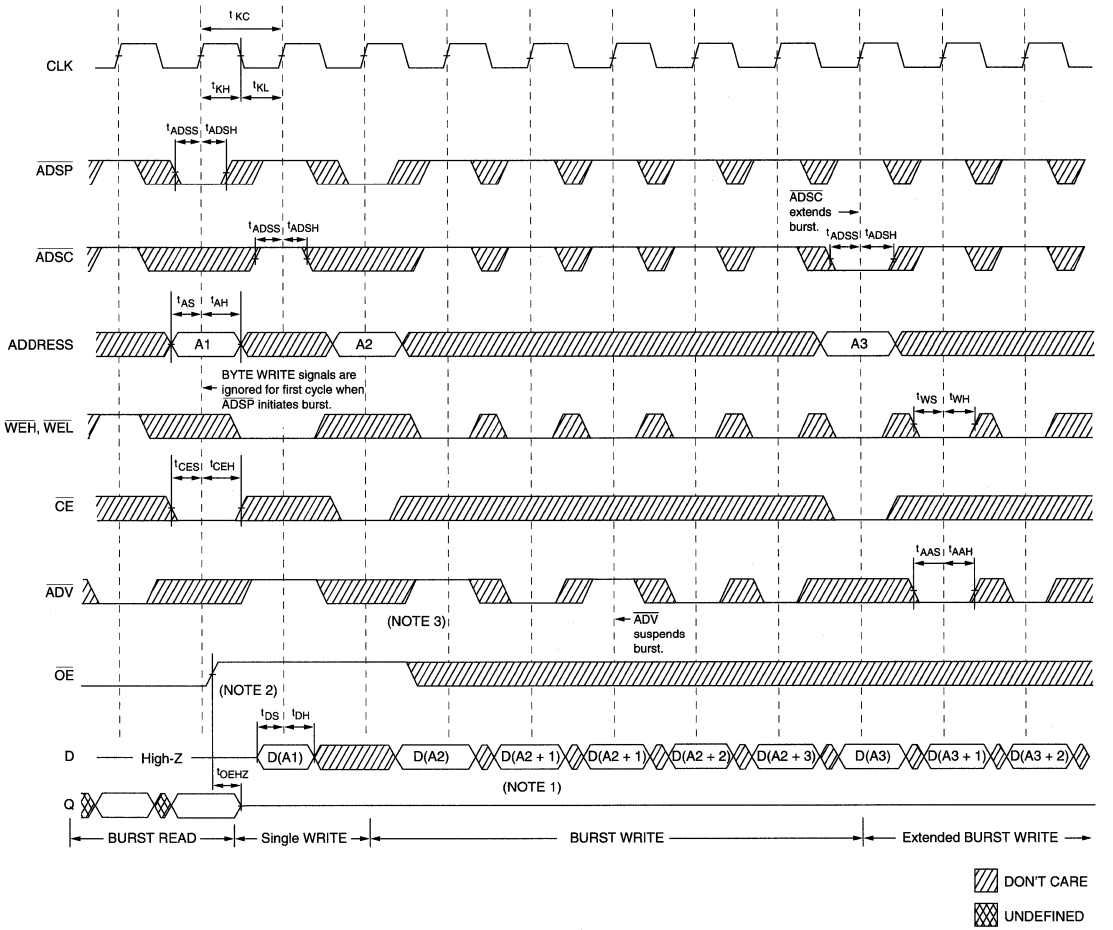
READ TIMING



NOTE: 1. Q(A2) refers to output from address A2. Q(A2+1) refers to output from the next internal burst address following A2.

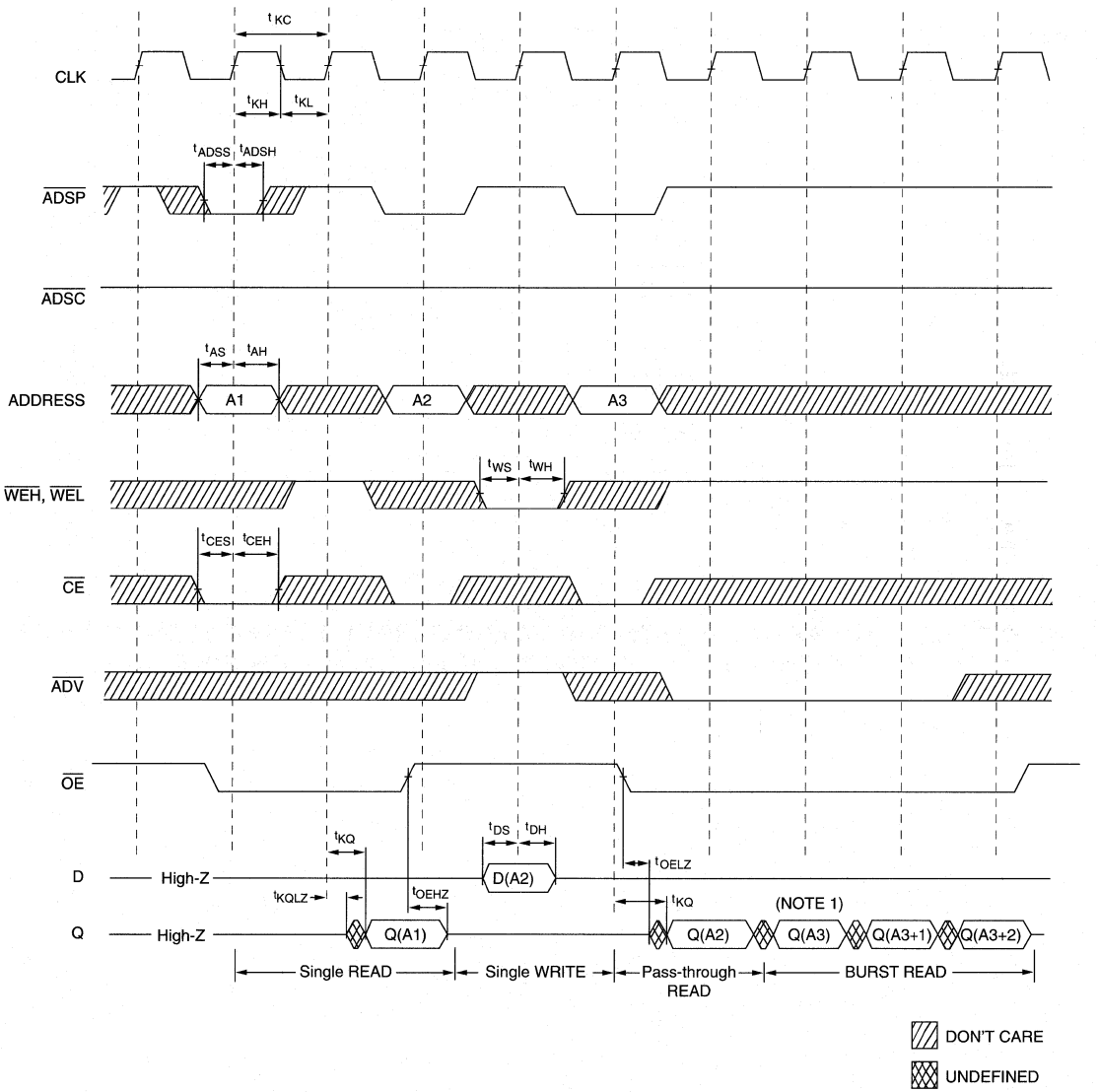
NEW 3.3 VOLT SYNCHRONOUS SRAM

WRITE TIMING



NOTE:
1. D(A2) refers to input to address A2. D(A2+1) refers to input to the next internal burst address following A2.
2. Although a LOW on any one of the byte write inputs will tristate the data outputs, $\overline{OE}$ must be HIGH before the input data setup and held HIGH throughout the the data hold time. This prevents input/output data contention for the time period prior to the byte write enable inputs being latched.
3. $\overline{ADV}$ must be HIGH to permit a WRITE to the loaded address.

READ/WRITE TIMING



NOTE: 1. Q(A2) refers to output from address A2. Q(A2+1) refers to output from the next internal burst address following A2.

APPLICATION EXAMPLE

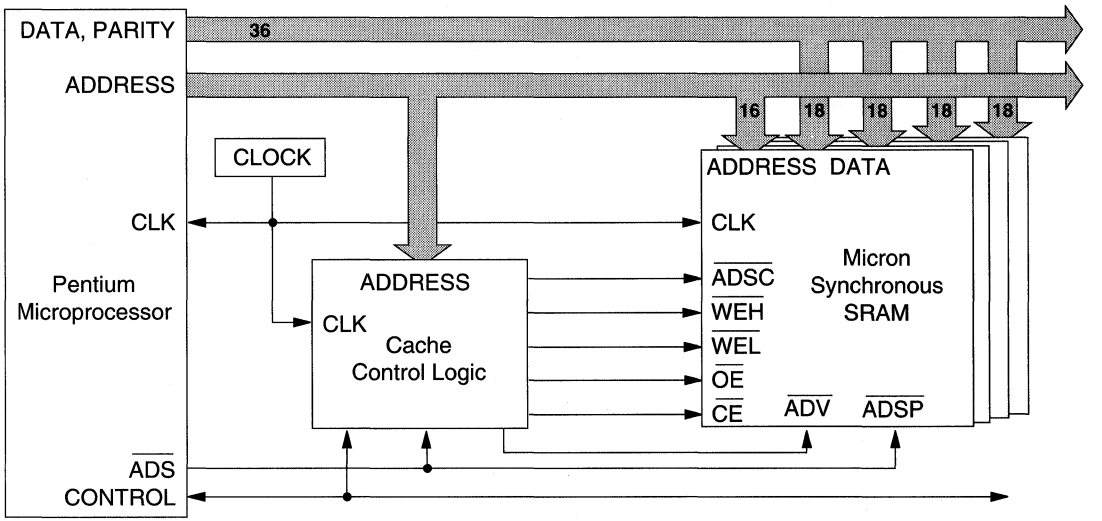


Figure 3
512K BYTE SECONDARY CACHE WITH PARITY AND BURST FOR 50 MHz PENTIUM™ OR POWERPC™ USING FOUR MT58LC64K18A6EJ-10 SYNCHRONOUS SRAMs

SYNCHRONOUS SRAM

32K x 36 SRAM

+3.3V SUPPLY WITH CLOCKED, REGISTERED INPUTS AND BURST COUNTER

FEATURES

- Fast access times: 9, 10, 12 and 17ns
- Fast $\overline{OE}$: 5, 6 and 7ns
- Single +3.3V ±5% power supply
- 5V-tolerant I/O
- Common data inputs and data outputs
- Individual BYTE WRITE control
- Three chip enables for simple depth expansion
- Clock controlled, registered, address, data and control
- Internally self-timed WRITE cycle
- Burst control pins (486/Pentium™ burst sequence)
- 100-lead TQFP package for high density, high speed
- Low capacitive bus loading
- High 30pF output drive capability at rated access time
- Parity Disable function for 32-bit operation

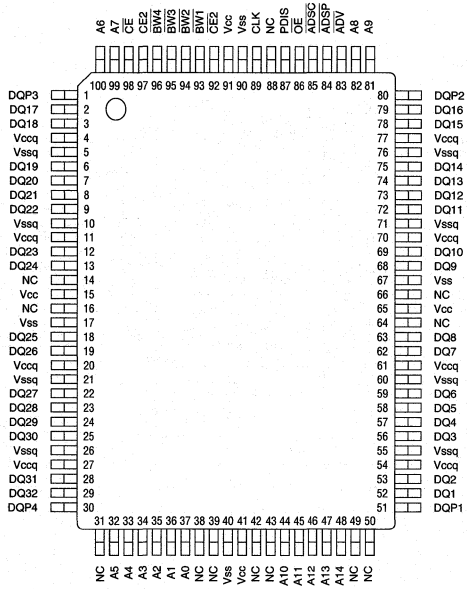
OPTIONS — MARKING

- Timing
  - 9ns access/15ns cycle — -9
  - 10ns access/15ns cycle — -10
  - 12ns access/20ns cycle — -12
  - 17ns access/25ns cycle — -17
- Packages
  - 100-pin TQFP — LG
- Part Number Example: MT58LC32K36B2LG-12

NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

100-Pin TQFP
(SC-1)



GENERAL DESCRIPTION

The Micron Synchronous SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

The MT58LC32K36B2 SRAM integrates a 32K x 36 SRAM core with advanced synchronous peripheral circuitry and a 2-bit burst counter. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input (CLK). The synchronous inputs include all addresses, all data inputs, active LOW chip enable ($\overline{CE}$), two additional chip enables for easy depth expansion (CE2, $\overline{CE2}$), burst control inputs ($\overline{ADSC}$, $\overline{ADSP}$, $\overline{ADV}$) and byte write enables ($\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, $\overline{BW4}$).

Asynchronous inputs include the output enable ($\overline{OE}$) and the clock (CLK). The data-out (Q), enabled by $\overline{OE}$, is also asynchronous. WRITE cycles can be from one to four bytes wide as controlled by the byte write enables.

Burst operation can be initiated with either address status processor ($\overline{ADSP}$) or address status controller ($\overline{ADSC}$) input pins. Subsequent burst addresses can be internally generated as controlled by the burst advance pin ($\overline{ADV}$).

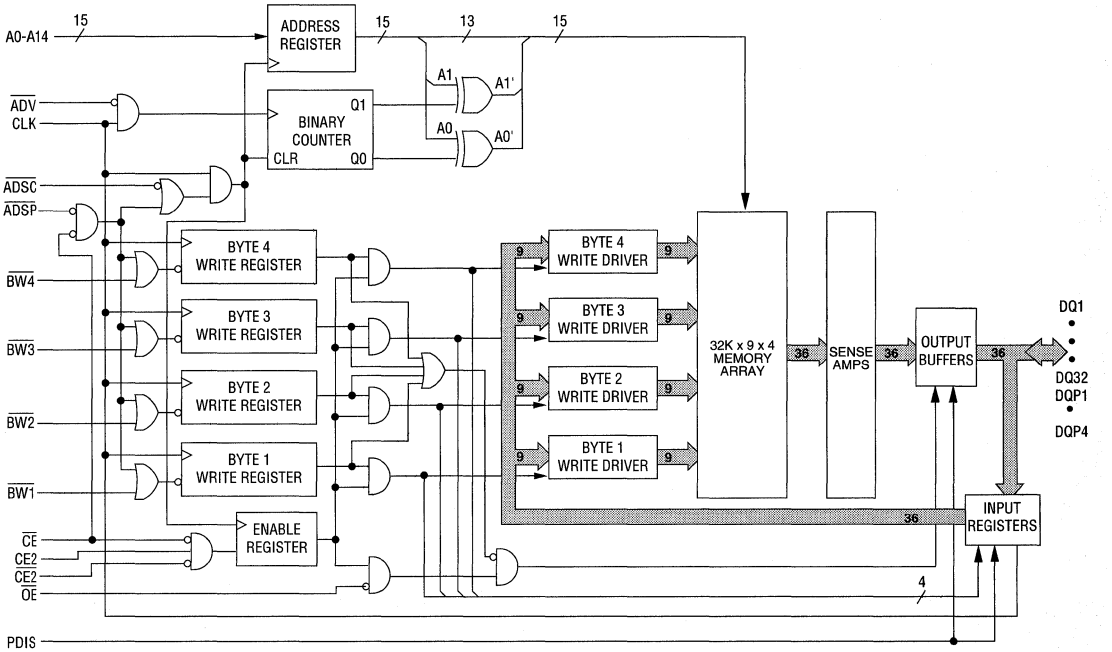
Address and write control are registered on-chip to simplify WRITE cycles. This allows self-timed WRITE cycles. Individual byte enables allow individual bytes to be written. $\overline{BW1}$ controls DQ1-DQ8 and DQP1, $\overline{BW2}$ controls DQ9-DQ16 and DQP2, $\overline{BW3}$ controls DQ17-DQ24 and DQP3, and $\overline{BW4}$ controls DQ25-DQ32 and DQP4.

NEW 3.3 VOLT SYNCHRONOUS SRAM

GENERAL DESCRIPTION (continued)

The MT58LC32K36B2 operates from a +3.3V power supply and all inputs and outputs are TTL-compatible and 5V tolerant. The device is ideally suited for 486 and Pentium (P5) systems and those systems which benefit from a very wide data bus. The device is also ideal in 32-, 64- and 72-bit-wide applications.

FUNCTIONAL BLOCK DIAGRAM



NOTE: 1. The Functional Block Diagram illustrates simplified device operation. See Truth Table, pin descriptions and timing diagrams for detailed information.

PIN DESCRIPTIONS

TQFP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
37, 36, 35, 34, 33, 32, 100, 99, 82, 81, 44, 45, 46, 47, 48	A0-A14	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK.
93, 94, 95, 96	$\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, $\overline{BW4}$	Input	Synchronous Byte Write Enables: These active LOW inputs allow individual bytes to be written and must meet the setup and hold times around the rising edge of CLK. A BYTE WRITE enable is LOW for a WRITE cycle and HIGH for a READ cycle. $\overline{BW1}$ controls DQ1-DQ8 and DQP1. $\overline{BW2}$ controls DQ9-DQ16 and DQP2. $\overline{BW3}$ controls DQ17-DQ24 and DQP3. $\overline{BW4}$ controls DQ25-DQ32 and DQP4. Data I/O are tristated if any of these four inputs are LOW.
89	CLK	Input	Clock: This signal registers the address, data, chip enables, byte write enables and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
98	$\overline{CE}$	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and conditions internal use of $\overline{ADSP}$. This input is sampled only when a new external address is loaded.
92	$\overline{CE2}$	Input	Synchronous Chip Enable: This active LOW input is used to enable the device. This input is sampled only when a new external address is loaded. This input can be used for memory depth expansion.
97	CE2	Input	Synchronous Chip Enable: This active HIGH input is used to enable the device. This input is sampled only when a new external address is loaded. This input can be used for memory depth expansion.
86	$\overline{OE}$	Input	Output Enable: This active LOW asynchronous input enables the data I/O output drivers.
83	$\overline{ADV}$	Input	Synchronous Address Advance: This active LOW input is used to advance the internal burst counter, controlling burst access after the external address is loaded. A HIGH on this pin effectively causes wait states to be generated (no address advance). This pin must be HIGH at the rising edge of the first clock after an $\overline{ADSP}$ cycle is initiated if a WRITE cycle is desired (to ensure use of correct address).
84	$\overline{ADSP}$	Input	Synchronous Address Status Processor: This active LOW input interrupts any ongoing burst, causing a new external address to be registered. A READ is performed using the new address, independent of the byte write enables and $\overline{ADSC}$ but dependent upon CE2 and $\overline{CE2}$. $\overline{ADSP}$ is ignored if $\overline{CE}$ is HIGH. Power down state is entered if CE2 is LOW or $\overline{CE2}$ is HIGH.
85	$\overline{ADSC}$	Input	Synchronous Address Status Controller: This active LOW input interrupts any ongoing burst and causes a new external address to be registered. A READ or WRITE is performed using the new address if all chip enables are active. Power-down state is entered if one or more chip enables are inactive.

PIN DESCRIPTIONS (continued)

TQFP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
14, 16, 31, 38, 39, 42, 43, 49, 50, 64, 66, 88	NC	-	No Connect: These signals are not internally connected.
52, 53, 56, 57, 58, 59, 62, 63, 68, 69, 72, 73, 74, 75, 78, 79, 2, 3, 6, 7, 8, 9, 12, 13, 18, 19, 22, 23, 24, 25, 28, 29	DQ1-DQ32	Input/ Output	SRAM Data I/O: Byte 1 is DQ1-DQ8; Byte 2 is DQ9-DQ16; Byte 3 is DQ17-DQ24; Byte 4 is DQ25-DQ32. Input data must meet setup and hold times around the rising edge of CLK.
51, 80, 1, 30	DQP1-DQP4	Input/ Output	Parity Data I/O: Byte 1 Parity is DQP1; Byte 2 Parity is DQP2; Byte 3 Parity is DQP3; Byte 4 Parity is DQP4.
87	PDIS	Input	Parity Disable: When HIGH, this input disables DQP1 through DQP4 for 32-bit data bus width. A LOW on PDIS enables control of DQP1 through DQP4 in the same manner as DQ1-DQ32 are controlled.
15, 41, 65, 91	Vcc	Supply	Power Supply: +3.3V ±5%
17, 40, 67, 90	Vss	Supply	Ground: GND
4, 11, 20, 27, 54, 61, 70, 77	VccQ	Supply	Isolated Output Buffer Supply: +3.3V ±5%
5, 10, 21, 26, 55, 60, 71, 76	VssQ	Supply	Isolated Output Buffer Ground: GND

BURST SEQUENCE TABLE

	Address Used		
Operation	**A14-A2**	**A1**	**A0**
First access, register external address	A14-A2	A1	A0
Second access (first burst address)	registered A14-A2	registered A1	registered $\overline{A0}$
Third access (second burst address)	registered A14-A2	registered $\overline{A1}$	registered A0
Fourth access (third burst address)	registered A14-A2	registered $\overline{A1}$	registered $\overline{A0}$

NOTE: The burst sequence wraps around to its initial state upon completion.

BURST ADDRESS TABLE

First Address	Second Address	Third Address	Fourth Address
X...X00	X...X01	X...X10	X...X11
X...X01	X...X00	X...X11	X...X10
X...X10	X...X11	X...X00	X...X01
X...X11	X...X10	X...X01	X...X00

TRUTH TABLE

OPERATION	ADDRESS USED	$\overline{CE}$	$\overline{CE2}$	CE2	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Deselected Cycle, Power-down	None	H	X	X	X	L	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	None	L	X	L	L	X	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	None	L	H	X	L	X	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	None	L	X	L	H	L	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	None	L	H	X	H	L	X	X	X	L-H	High-Z
READ Cycle, Begin Burst	External	L	L	H	L	X	X	X	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	L	X	X	X	H	L-H	High-Z
WRITE Cycle, Begin Burst	External	L	L	H	H	L	X	L	X	L-H	D
READ Cycle, Begin Burst	External	L	L	H	H	L	X	H	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	H	L	X	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	X	X	X	H	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	X	X	X	H	H	L	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	H	X	X	X	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	H	X	X	X	H	L	H	H	L-H	High-Z
WRITE Cycle, Continue Burst	Next	X	X	X	H	H	L	L	X	L-H	D
WRITE Cycle, Continue Burst	Next	H	X	X	X	H	L	L	X	L-H	D
READ Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	H	L-H	High-Z
READ Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	H	L-H	High-Z
WRITE Cycle, Suspend Burst	Current	X	X	X	H	H	H	L	X	L-H	D
WRITE Cycle, Suspend Burst	Current	H	X	X	X	H	H	L	X	L-H	D

NOTE:
1. X means "don't care." H means logic HIGH. L means logic LOW. $\overline{WRITE}$=L means any one or more byte write enable signals ($\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$ or $\overline{BW4}$) are LOW. $\overline{WRITE}$=H means all byte write enable signals are HIGH.
2. $\overline{BW1}$ enables writes to Byte 1 (DQ1-DQ8, DQP1). $\overline{BW2}$ enables writes to Byte 2 (DQ9-DQ16, DQP2). $\overline{BW3}$ enables writes to Byte 3 (DQ17-DQ24, DQP3). $\overline{BW4}$ enables writes to Byte 4 (DQ25-DQ32, DQP4).
3. All inputs except $\overline{OE}$ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
4. Wait states are inserted by suspending burst.
5. For a write operation following a read operation, $\overline{OE}$ must be HIGH before the input data required setup time and held HIGH throughout the input data hold time.
6. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
7. PDIS disables the DQP lines when HIGH and enables the DQP lines when LOW.
8. $\overline{ADSP}$ LOW always initiates an internal READ at the L-H edge of CLK. A WRITE is performed by setting one or more byte write enable signals LOW for the subsequent L-H edge of CLK. Refer to WRITE timing diagram for clarification.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to Vss .....-0.5V to +4.6V
V_{IN} .....-0.5V to +6V
Storage Temperature (plastic) .....-55°C to +150°C
Junction Temperature .....+150°C
Power Dissipation 1.6W
Short Circuit Output Current 100mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; T_C ≤ 110°C; V_{CC} = 3.3V ±5% unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.0	5.5	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-1	1	µA	
Output Leakage Current	Output(s) disabled, 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	3.1	3.5	V	1

				MAX					
DESCRIPTION	CONDITIONS	SYMBOL	TYPICAL	-9	-10	-12	-17	UNITS	NOTES
Power Supply Current: Operating	Device selected; all inputs ≤ V_{IL} OR ≥ V_{IH}; cycle time ≥ ^tKC min; V_{CC} = MAX; outputs open	I_{CC}	200	275	275	250	225	mA	3, 12, 13
Power Supply Current: Idle	Device selected; $\overline{ADSC}$, $\overline{ADSP}$, $\overline{ADV}$ ≥ V_{IH}; all inputs ≤ V_{IL} OR ≥ V_{IH}; V_{CC} = MAX; cycle time ≥ ^tKC min	I_{SB1}	55	85	85	70	60	mA	12, 13
CMOS Standby	Device deselected; V_{CC} = MAX; all inputs ≤ V_{SS} +0.2 or ≥ V_{CC} -0.2; all inputs static; CLK frequency = 0	I_{SB2}	0.2	2	2	2	2	mA	12, 13
TTL Standby	Device deselected; all inputs ≤ V_{IL} OR ≥ V_{IH}; all inputs static; V_{CC} = MAX; CLK frequency = 0	I_{SB3}	10	18	18	18	18	mA	12, 13
Clock Running	Device deselected; all inputs ≤ V_{IL} OR ≥ V_{IH}; V_{CC} = MAX; CLK cycle time ≥ ^tKC min	I_{SB4}	20	35	35	30	25	mA	12, 13

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	3	4	pF	4
Input/Output Capacitance (DQ)	V_{CC} = 3.3V	C_O	5	6	pF	4

THERMAL CONSIDERATIONS

DESCRIPTION	CONDITIONS	SYMBOL	TYP	UNITS	NOTES
Thermal resistance - Junction to Ambient	Still Air	θ_{JA}	65	°C/W	
Thermal resistance - Junction to Case		θ_{JC}	6	°C/W	
Maximum Case Temperature		TC	110	°C	11

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ±5%)

		-9		-10		-12		-17			
DESCRIPTION	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Clock											
Clock cycle time	^tKC	15		15		20		25		ns	
Clock HIGH time	^tKH	4		5		6		8		ns	
Clock LOW time	^tKL	4		5		6		8		ns	
Output Times											
Clock to output valid	^tKQ		9		10		12		17	ns	
Clock to output invalid	^tKQX	3		3		3		3		ns	
Clock to output in Low-Z	^tKQLZ	5		5		5		5		ns	6, 7
Clock to output in High-Z	^tKQHZ		5		5		6		6	ns	6, 7
$\overline{OE}$ to output valid	^tOEQ		5		5		6		7	ns	9
$\overline{OE}$ to output in Low-Z	^tOELZ	0		0		0		0		ns	6, 7
$\overline{OE}$ to output in High-Z	^tOEHZ		5		5		6		6	ns	6, 7
Setup Times											
Address	^tAS	2.5		3		3		3		ns	8, 10
Address Status ($\overline{ADSC}$, $\overline{ADSP}$)	^tADSS	2.5		3		3		3		ns	8, 10
Address Advance ($\overline{ADV}$)	^tAAS	2.5		3		3		3		ns	8, 10
Byte Write Enables ($\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, $\overline{BW4}$)	^tWS	2.5		3		3		3		ns	8, 10
Data-in	^tDS	2.5		3		3		3		ns	8, 10
Chip Enables ($\overline{CE}$, $\overline{CE2}$, CE2)	^tCES	2.5		3		3		3		ns	8, 10
Hold Times											
Address	^tAH	0.5		0.5		0.5		0.5		ns	8, 10
Address Status ($\overline{ADSC}$, $\overline{ADSP}$)	^tADSH	0.5		0.5		0.5		0.5		ns	8, 10
Address Advance ($\overline{ADV}$)	^tAAH	0.5		0.5		0.5		0.5		ns	8, 10
Byte Write Enables ($\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, $\overline{BW4}$)	^tWH	0.5		0.5		0.5		0.5		ns	8, 10
Data-in	^tDH	0.5		0.5		0.5		0.5		ns	8, 10
Chip Enables ($\overline{CE}$, $\overline{CE2}$, CE2)	^tCEH	0.5		0.5		0.5		0.5		ns	8, 10

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	1.5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

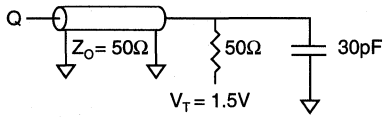


Fig. 1 OUTPUT LOAD EQUIVALENT

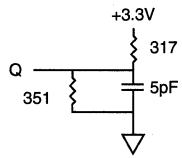
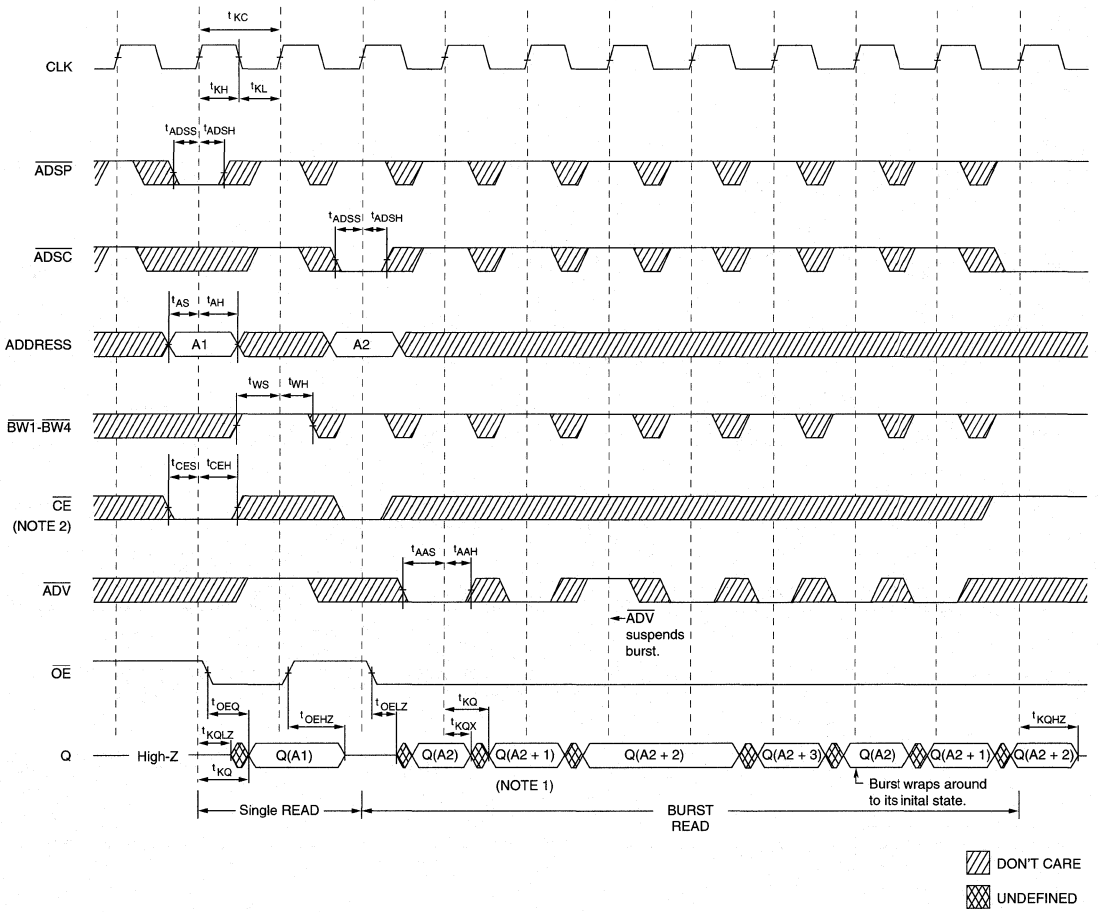


Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

1. All voltages referenced to Vss (GND).
2. Overshoot: $V_{IH} \leq +6.0V$ for $t \leq {}^tKC/2$.
   Undershoot: $V_{IL} \geq -2.0V$ for $t \leq {}^tKC/2$.
   Power-up: $V_{IH} \leq +6.0V$ and $Vcc \leq 3.1V$ for $t \leq 200msec$.
3. Icc is given with no output current. Icc increases with greater output loading and faster cycle times.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. Output loading is specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ${}^tKQHZ$ is less than ${}^tKQLZ$ and ${}^tOEHZ$ is less than ${}^tOELZ$.
8. A READ cycle is defined by byte write enables all HIGH or $\overline{ADSP}$ LOW for the required setup and hold times. A WRITE cycle is defined by at least one byte write enable LOW and $\overline{ADSP}$ HIGH for the required setup and hold times.
9. $\overline{OE}$ is a "don't care" when a byte write enable is sampled LOW.
10. This is a synchronous device. All addresses must meet the specified setup and hold times for all rising edges of CLK when either $\overline{ADSP}$ or $\overline{ADSC}$ is LOW and chip enabled. All other synchronous inputs must meet the setup and hold times with stable logic levels for all rising edges of clock (CLK) when chip is enabled. Chip enable must be valid at each rising edge of CLK (when either $\overline{ADSP}$ or $\overline{ADSC}$ is LOW) to remain enabled.
11. Micron does not warrant the functionality or reliability of any product in which the case temperature exceeds 110°C. Care should be taken to limit case temperature to acceptable levels.
12. "Device Deselected" means device is in POWER-DOWN mode as defined in the truth table. "Device Selected" means device is active (not in POWER-DOWN mode).
13. Typical values are measured at 3.3V, 25°C and 20ns cycle time.

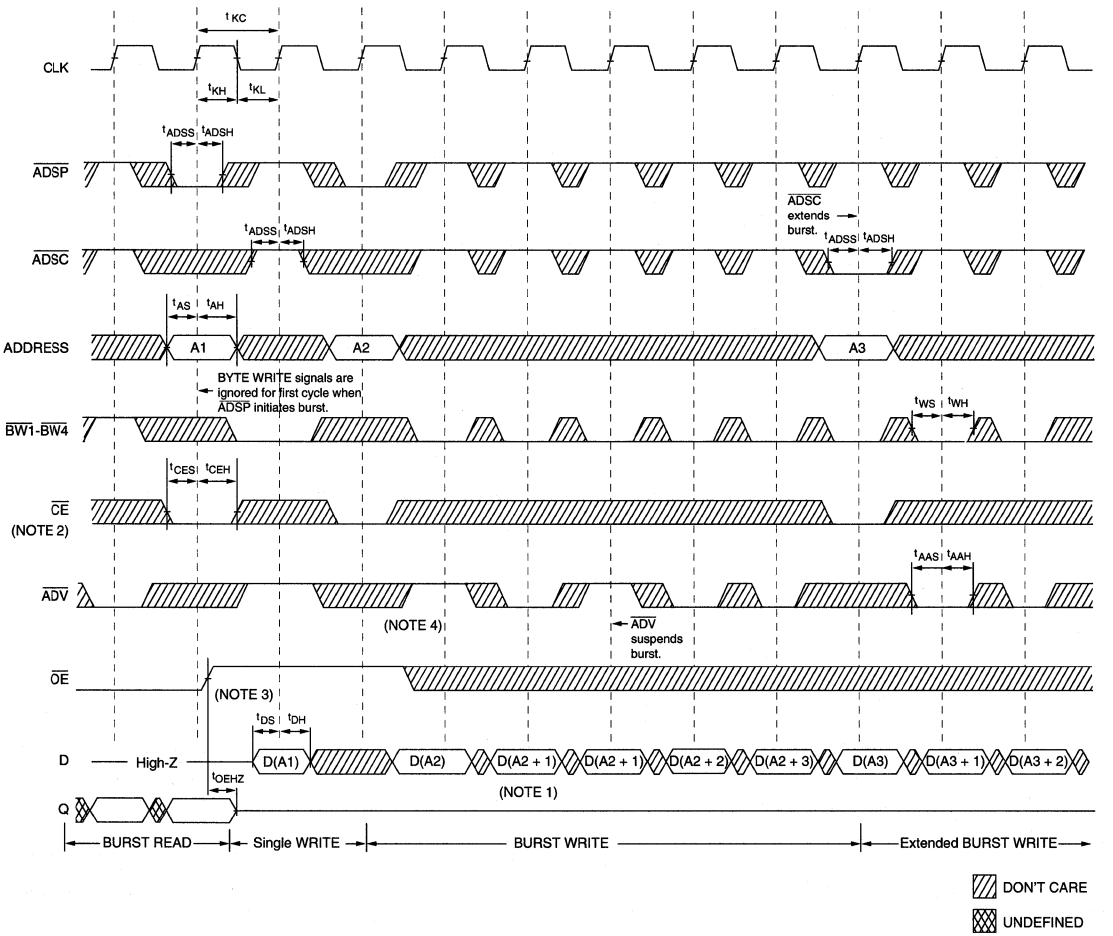
READ TIMING



NOTE:
1. Q(A2) refers to output from address A2. Q(A2+1) refers to output from the next internal burst address following A2.
2. $\overline{CE2}$ and CE2 have timing identical to $\overline{CE}$. On this diagram, when $\overline{CE}$ is LOW, $\overline{CE2}$ is LOW and CE2 is HIGH. When $\overline{CE}$ is HIGH, $\overline{CE2}$ is HIGH and CE2 is LOW.

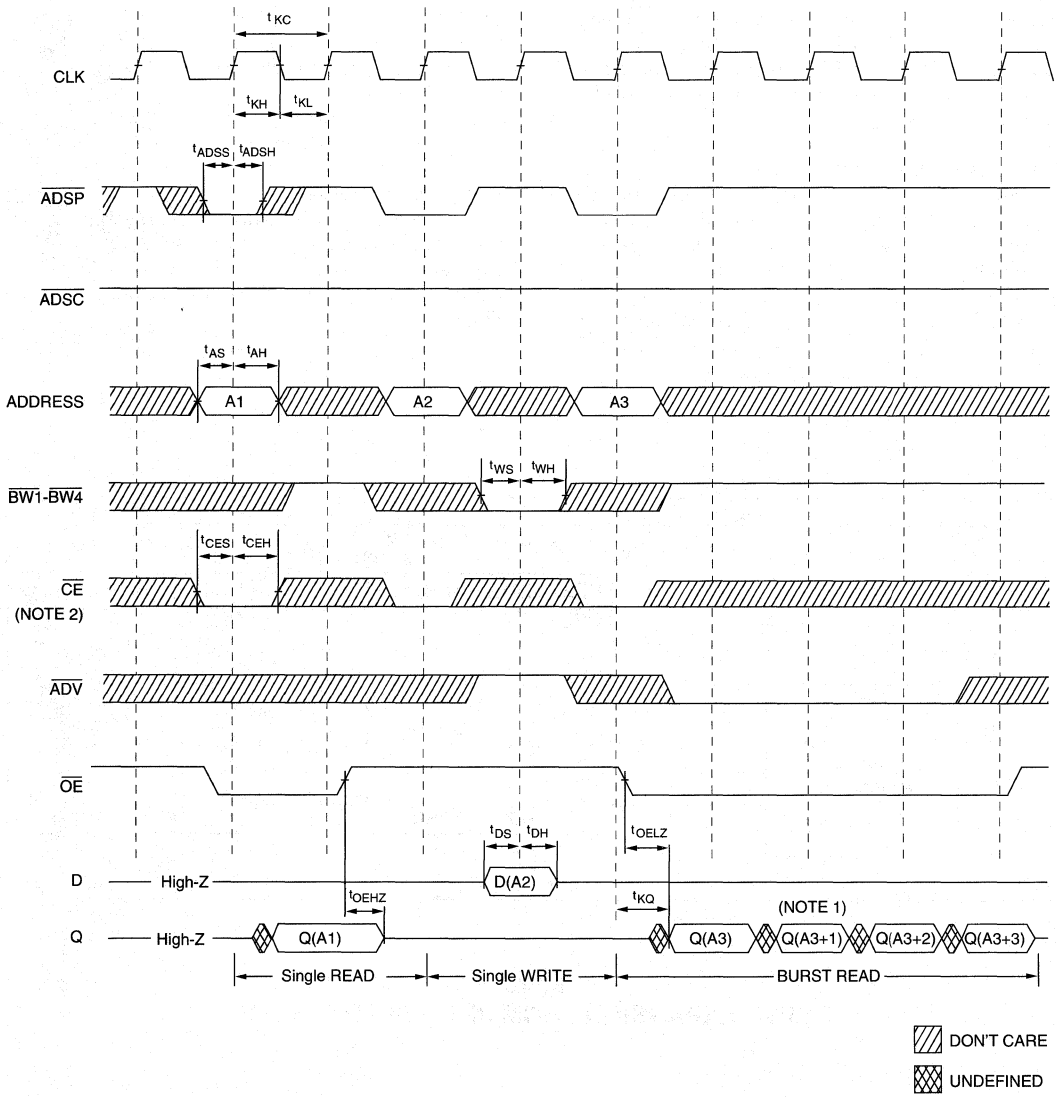
NEW 3.3 VOLT SYNCHRONOUS SRAM

WRITE TIMING



NOTE:
1. Q(A2) refers to output from address A2. Q(A2+1) refers to output from the next internal burst address following A2.
2. $\overline{CE2}$ and CE2 have timing identical to $\overline{CE}$. On this diagram, when $\overline{CE}$ is LOW, $\overline{CE2}$ is LOW and CE2 is HIGH. When $\overline{CE}$ is HIGH, $\overline{CE2}$ is HIGH and CE2 is LOW.
3. $\overline{OE}$ must be HIGH before the input data setup and held HIGH throughout the the data hold time. This prevents input/output data contention for the time period prior to the byte write enable inputs being sampled.
4. $\overline{ADV}$ must be HIGH to permit a WRITE to the loaded address.

READ/WRITE TIMING



NOTE:
1. Q(A3) refers to output from address A3. Q(A3+1) refers to output from the next internal burst address following A3.
2. $\overline{CE2}$ and CE2 have timing identical to $\overline{CE}$. On this diagram, when $\overline{CE}$ is LOW, $\overline{CE2}$ is LOW and CE2 is HIGH. When $\overline{CE}$ is HIGH, $\overline{CE2}$ is HIGH and CE2 is LOW.

NEW 3.3 VOLT SYNCHRONOUS SRAM

APPLICATION INFORMATION

32-BIT-WIDE SYSTEMS

The Micron 32K x 36 Synchronous SRAM may be used in a 32-bit-wide system without the use of any external components by connecting PDIS to Vcc. This disables the output buffer on the data parity input/output lines (DQP1, DQP2, DQP3 and DQP4).

LOAD DERATING CURVES

The Micron 32K x 36 Synchronous SRAM timing is dependent upon the capacitive loading on the outputs. The data sheet is written assuming a load of 30pF. Access time changes with load capacitance as follows:

$\Delta^tKQ = 0.016$ ns/pF x ΔC_L pF. (Note: this is preliminary information subject to change.)

For example, if the SRAM loading is 22pF, ΔC_L is -8pF (8pF less than rated load). The clock to valid output time of the SRAM is reduced by 0.016 x 8 = 0.128ns. If the device is a 12ns part, the worst case ^tKQ becomes 11.87ns (approximately).

Consult the factory for copies of I/O current versus voltage curves and Quad Design models.

DEPTH EXPANSION

The Micron 32K x 36 Synchronous SRAM incorporates two additional chip enables to facilitate simple depth expansion. This permits easy cache upgrades from 32K depth to 64K depth with no extra logic as shown in Figure 3.

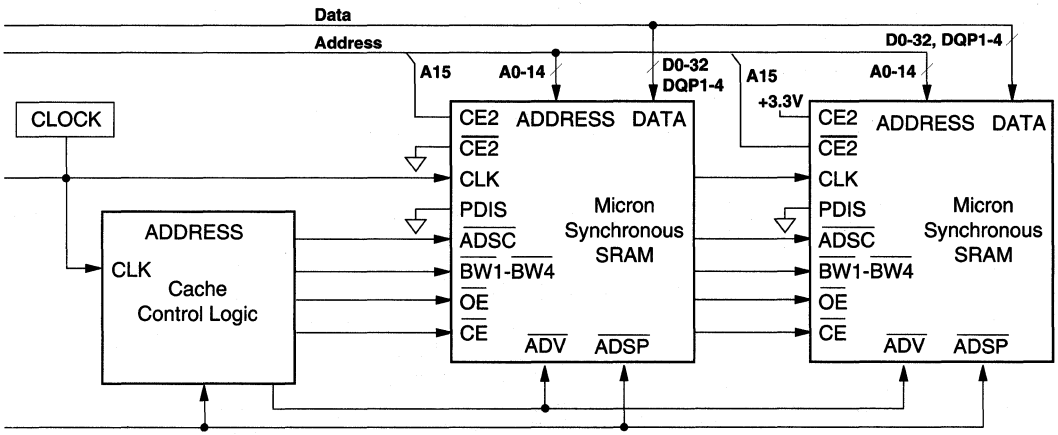


Figure 3
DEPTH EXPANSION FROM 32K x 36 TO 64K x 36

APPLICATION EXAMPLES

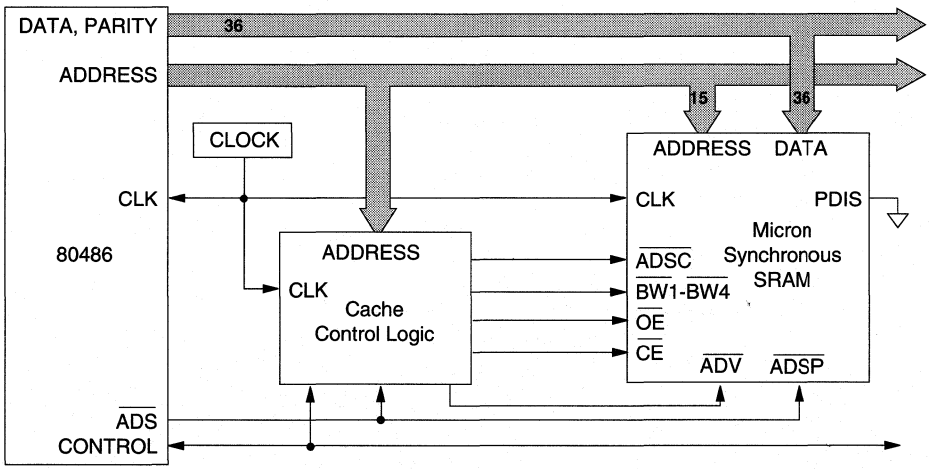


Figure 4
128K BYTE SECONDARY CACHE WITH PARITY AND BURST FOR 50 MHz 80486 USING ONE MT58LC32K36B2LG-12 SYNCHRONOUS SRAM

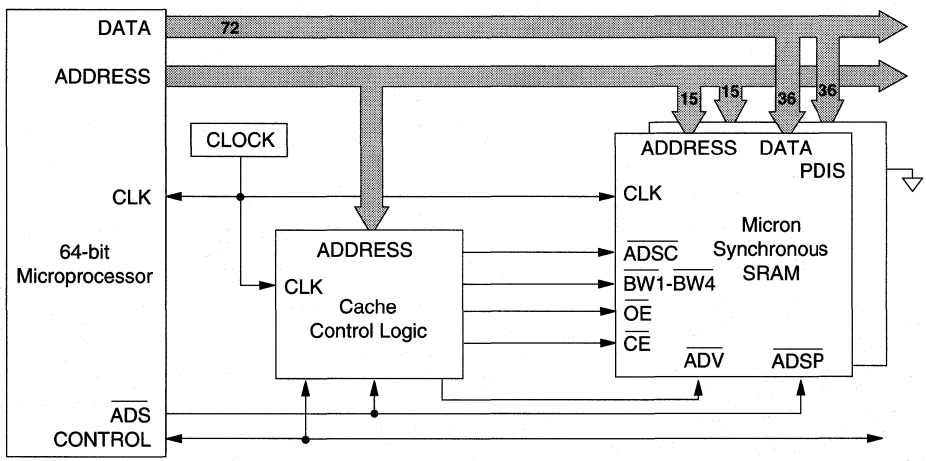


Figure 5
256K BYTE SECONDARY CACHE WITH PARITY AND BURST FOR 66 MHz PENTIUM USING TWO MT58LC32K36B2LG-9 SYNCHRONOUS SRAMs

MICRON SEMICONDUCTOR, INC.

MT58LC32K36B2
32K x 36 SYNCHRONOUS SRAM

MICRON SEMICONDUCTOR, INC.

MT58LC32K36C4
32K x 36 SYNCHRONOUS SRAM

SYNCHRONOUS SRAM

32K x 36 SRAM

+3.3V SUPPLY, FULLY REGISTERED INPUTS AND OUTPUTS AND BURST COUNTER

NEW 3.3 VOLT SYNCHRONOUS SRAM

FEATURES

- Fast access times: 7, 10, 12 and 15ns
- Fast $\overline{OE}$: 5, 6, 7 and 8ns
- Single +3.3V ±5% power supply
- 5V-tolerant I/O
- Common data inputs and data outputs
- Individual BYTE WRITE control
- Three chip enables for simple depth expansion
- Clock controlled, registered, address, data I/O and control for fully pipelined applications
- Internally self-timed WRITE cycle
- WRITE pass-through capability
- Burst control pins (486/Pentium™ burst sequence)
- 100-lead TQFP package for high density, high speed
- Low capacitive bus loading
- High 30pF output drive capability at rated access time
- Parity Disable function for 32-bit operation

OPTIONS

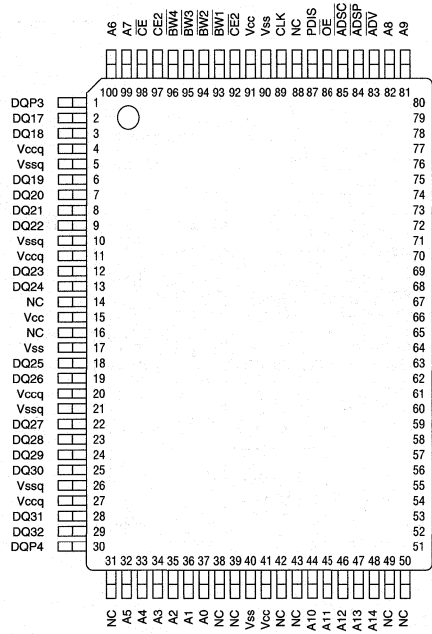
	MARKING
• Timing	
7ns access/15ns cycle	- 7
10ns access/20ns cycle	-10
12ns access/25ns cycle	-12
15ns access/30ns cycle	-15
• Packages	
100-pin TQFP	LG

- Part Number Example: MT58LC32K36C4LG-10

NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

100-Pin TQFP
(SC-1)



GENERAL DESCRIPTION

The Micron Synchronous SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

The MT58LC32K36C4 SRAM integrates a 32K x 36 SRAM core with advanced synchronous peripheral circuitry, a 2-bit burst counter and output register. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input (CLK). The synchronous inputs include all addresses, all data inputs, active LOW chip enable, two additional chip enables for easy depth expansion ($\overline{CE2}$, CE2), burst control inputs ($\overline{ADSC}$, $\overline{ADSP}$, $\overline{ADV}$) and the byte write enables ($\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, $\overline{BW4}$).

Asynchronous inputs include the output enable ($\overline{OE}$) and the clock (CLK). The data-out (Q), enabled by $\overline{OE}$, is also asynchronous. The output register is controlled by the clock. WRITE cycles can be from one to four bytes wide as controlled by the byte write enables.

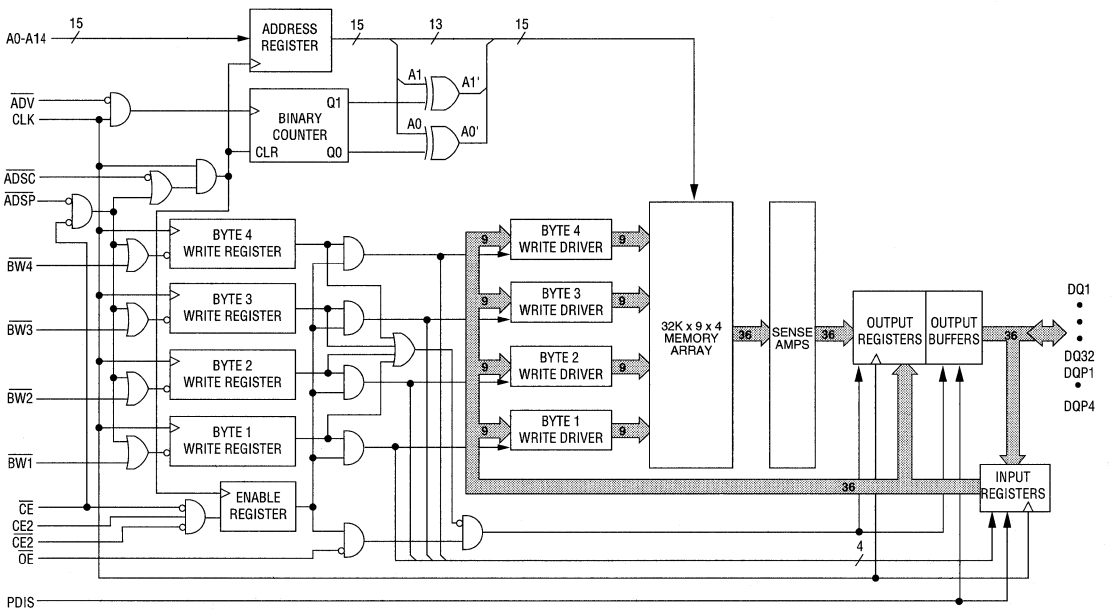
Burst operation can be initiated with either address status processor ($\overline{ADSP}$) or address status controller ($\overline{ADSC}$) input pins. Subsequent burst addresses can be internally generated as controlled by the burst advance pin ($\overline{ADV}$).

GENERAL DESCRIPTION (continued)

Address and write control are registered on-chip to simplify WRITE cycles. This allows self-timed WRITE cycles. Individual byte enables allow individual bytes to be written. WRITE pass-through makes written data immediately available at the output register during the READ cycle following a WRITE as controlled solely by $\overline{OE}$ to improve cache system response.

The MT58LC32K36C4 operates from a +3.3V power supply and all inputs and outputs are TTL compatible and 5V tolerant. The device is ideal for Pentium (P5) pipelined applications and 32-, 64- and 72-bit-wide applications.

FUNCTIONAL BLOCK DIAGRAM



NOTE: 1. The Functional Block Diagram illustrates simplified device operation. See Truth Table, pin descriptions and timing diagrams for detailed information.

PIN DESCRIPTIONS

TQFP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
37, 36, 35, 34, 33, 32, 100, 99, 82, 81, 44, 45, 46, 47, 48	A0-A14	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK.
93, 94, 95, 96	$\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, $\overline{BW4}$	Input	Synchronous Byte Write Enables: These active LOW inputs allow individual bytes to be written and must meet the setup and hold times around the rising edge of CLK. A byte write enable is LOW for a WRITE cycle and HIGH for a READ cycle.$\overline{BW1}$ controls DQ1-DQ8 and DQP1. $\overline{BW2}$ controls DQ9-DQ16 and DQP2. $\overline{BW3}$ controls DQ17-DQ24 and DQP3. $\overline{BW4}$ controls DQ25-DQ32 and DQP4. Data I/O are tristated if any of these four inputs are LOW.
89	CLK	Input	Clock: This signal registers the address, data, chip enables, byte write enables and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
98	$\overline{CE}$	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and conditions internal use of $\overline{ADSP}$. This input is sampled only when a new external address is loaded.
92	$\overline{CE2}$	Input	Synchronous Chip Enable: This active LOW input is used to enable the device. This input is sampled only when a new external address is loaded. This input can be used for memory depth expansion.
97	CE2	Input	Synchronous Chip Enable: This active HIGH input is used to enable the device. This input is sampled only when a new external address is loaded. This input can be used for memory depth expansion.
86	$\overline{OE}$	Input	Output Enable: This active LOW asynchronous input enables the data I/O output drivers.
83	$\overline{ADV}$	Input	Synchronous Address Advance: This active LOW input is used to advance the internal burst counter, controlling burst access after the external address is loaded. A HIGH on this pin effectively causes wait states to be generated (no address advance). This pin must be HIGH at the rising edge of the first clock after an $\overline{ADSP}$ cycle is initiated if a WRITE cycle is desired (to ensure use of correct address).
84	$\overline{ADSP}$	Input	Synchronous Address Status Processor: This active LOW input interrupts any ongoing burst, causing a new external address to be registered. A READ is performed using the new address, independent of the byte write enables and $\overline{ADSC}$ but dependent upon CE2 and $\overline{CE2}$. $\overline{ADSP}$ is ignored if $\overline{CE}$ is HIGH. Power-down state is entered if CE2 is LOW or $\overline{CE2}$ is HIGH.
85	$\overline{ADSC}$	Input	Synchronous Address Status Controller: This active LOW input interrupts any ongoing burst and causes a new external address to be registered. A READ or WRITE is performed using the new address if all chip enables are active. Power-down state is entered if one or more chip enables are inactive.

PIN DESCRIPTIONS (continued)

TQFP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
14, 16, 31, 38, 39, 42, 43, 49, 50, 64, 66, 88	NC	-	No Connect: These signals are not internally connected.
52, 53, 56, 57, 58, 59, 62, 63 68, 69, 72, 73, 74, 75, 78, 79, 2, 3, 6, 7, 8, 9, 12, 13, 18, 19, 22, 23, 24, 25, 28, 29	DQ1-DQ32	Input/ Output	SRAM Data I/O: Byte 1 is DQ1-DQ8; Byte 2 is DQ9-DQ16; Byte 3 is DQ17-DQ24; Byte 4 is DQ25-DQ32. Input data must meet setup and hold times around the rising edge of CLK.
51, 80, 1, 30	DQP1-DQP4	Input/ Output	Parity Data I/O: Byte 1 Parity is DQP1; Byte 2 Parity is DQP2; Byte 3 Parity is DQP3; Byte 4 Parity is DQP4.
87	PDIS	Input	Parity Disable: When HIGH, this input disables DQP1 through DQP4 for 32-bit data bus width. A LOW on PDIS enables control of DQP1 through DQP4 in the same manner as DQ1-DQ32 are controlled.
15, 41, 65, 91	Vcc	Supply	Power Supply: +3.3V ±5%
17, 40, 67, 90	Vss	Supply	Ground: GND
4, 11, 20, 27, 54, 61, 70, 77	VccQ	Supply	Isolated Output Buffer Supply: +3.3V ±5%
5, 10, 21, 26, 55, 60, 71, 76	VssQ	Supply	Isolated Output Buffer Ground: GND

PASS-THROUGH TRUTH TABLE

PREVIOUS CYCLE		PRESENT CYCLE				NEXT CYCLE
OPERATION	$\overline{BWs}$	OPERATION	$\overline{CE}$	$\overline{BWs}$	$\overline{OE}$	OPERATION
Initiate WRITE cycle, all bytes Address = A(n-1), data = D(n-1)	All L	Initiate READ cycle Register A(n), Q = D(n-1)	L	H	L	Read D(n)
Initiate WRITE cycle, all bytes Address = A(n-1), data = D(n-1)	All L	No new cycle Q = D(n-1)	H	H	L	No carryover from previous cycle
Initiate WRITE cycle, all bytes Address = A(n-1), data = D(n-1)	All L	No new cycle Q = HIGH-Z	H	H	H	No carryover from previous cycle
Initiate WRITE cycle, one byte Address = A(n-1), data = D(n-1)	One L	No new cycle Q = D(n-1) for one byte	H	H	L	No carryover from previous cycle

NOTE: Previous cycle may be either BURST or NONBURST cycle.

BURST SEQUENCE TABLE

	Address Used		
Operation	**A14-A2**	**A1**	**A0**
First access, register external address	A14-A2	A1	A0
Second access (first burst address)	registered A14-A2	registered A1	registered $\overline{A0}$
Third access (second burst address)	registered A14-A2	registered $\overline{A1}$	registered A0
Fourth access (third burst address)	registered A14-A2	registered $\overline{A1}$	registered $\overline{A0}$

NOTE: The burst sequence wraps around to its initial state upon completion.

BURST ADDRESS TABLE

First Address	Second Address	Third Address	Fourth Address
X...X00	X...X01	X...X10	X...X11
X...X01	X...X00	X...X11	X...X10
X...X10	X...X11	X...X00	X...X01
X...X11	X...X10	X...X01	X...X00

TRUTH TABLE

OPERATION	ADDRESS USED	$\overline{CE}$	$\overline{CE2}$	CE2	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Deselected Cycle, Power-down	None	H	X	X	X	L	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	None	L	X	L	L	X	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	None	L	H	X	L	X	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	None	L	X	L	H	L	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	None	L	H	X	H	L	X	X	X	L-H	High-Z
READ Cycle, Begin Burst	External	L	L	H	L	X	X	X	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	L	X	X	X	H	L-H	High-Z
WRITE Cycle, Begin Burst	External	L	L	H	H	L	X	L	X	L-H	D
READ Cycle, Begin Burst	External	L	L	H	H	L	X	H	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	H	L	X	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	X	X	X	H	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	X	X	X	H	H	L	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	H	X	X	X	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	H	X	X	X	H	L	H	H	L-H	High-Z
WRITE Cycle, Continue Burst	Next	X	X	X	H	H	L	L	X	L-H	D
WRITE Cycle, Continue Burst	Next	H	X	X	X	H	L	L	X	L-H	D
READ Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	H	L-H	High-Z
READ Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	H	L-H	High-Z
WRITE Cycle, Suspend Burst	Current	X	X	X	H	H	H	L	X	L-H	D
WRITE Cycle, Suspend Burst	Current	H	X	X	X	H	H	L	X	L-H	D

NOTE:

1. X means "don't care." H means logic HIGH. L means logic LOW. $\overline{WRITE}$=L means any one or more byte write enable signals ($\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$ or $\overline{BW4}$) are LOW. $\overline{WRITE}$=H means all byte write enable signals are HIGH.
2. $\overline{BW1}$ enables writes to Byte 1 (DQ1-DQ8, DQP1). $\overline{BW2}$ enables writes to Byte 2 (DQ9-DQ16, DQP2). $\overline{BW3}$ enables writes to Byte 3 (DQ17-DQ24, DQP3). $\overline{BW4}$ enables writes to Byte 4 (DQ25-DQ32, DQP4).
3. All inputs except $\overline{OE}$ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
4. Wait states are inserted by suspending burst.
5. For a write operation following a read operation, $\overline{OE}$ must be HIGH before the input data required setup time and held HIGH throughout the input data hold time.
6. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
7. PDIS disables the DQP lines when HIGH and enables the DQP lines when LOW.
8. $\overline{ADSP}$ LOW always initiates an internal READ at the L-H edge of CLK. A WRITE is performed by setting one or more byte write enable signals LOW for the subsequent L-H edge of CLK. Refer to WRITE timing diagram for clarification.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to Vss .....-0.5V to +4.6V
V_{IN} .....-0.5V to +6V
Storage Temperature (plastic) .....-55°C to +150°C
JunctionTemperature .....+150°C
Power Dissipation 1.6W
Short Circuit Output Current 100mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; T_C ≤ 110°C; V_{CC} = 3.3V ±5% unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.0	5.5	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-1	1	µA	
Output Leakage Current	Output(s) disabled, 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	3.1	3.5	V	1

				MAX					
DESCRIPTION	CONDITIONS	SYMBOL	TYPICAL	-7	-10	-12	-15	UNITS	NOTES
Power Supply Current: Operating	Device selected; all inputs ≤ V_{IL} OR ≥ V_{IH}; cycle time ≥ ^tKC min; Vcc = MAX; outputs open	I_{CC}	200	275	250	225	200	mA	3, 12, 13
Power Supply Current: Idle	Device selected; $\overline{ADSC}$, $\overline{ADSP}$, $\overline{ADV}$ ≥ V_{IH}; all inputs ≤ V_{IL} OR ≥ V_{IH}; Vcc = MAX; cycle time ≥ ^tKC min	I_{SB1}	50	85	70	60	55	mA	12, 13
CMOS Standby	Device deselected; Vcc = MAX; all inputs ≤ Vss +0.2 or ≥ Vcc -0.2; all inputs static; CLK frequency = 0	I_{SB2}	0.2	2	2	2	2	mA	12, 13
TTL Standby	Device deselected; all inputs ≤ V_{IL} OR ≥ V_{IH}; all inputs static; Vcc = MAX; CLK frequency = 0	I_{SB3}	10	18	18	18	18	mA	12, 13
Clock Running	Device deselected; all inputs ≤ V_{IL} OR ≥ V_{IH}; Vcc = MAX; CLK cycle time ≥ ^tKC min	I_{SB4}	20	35	30	25	20	mA	12, 13

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	3	4	pF	4
Input/Output Capacitance (DQ)	Vcc = 3.3V	C_O	5	6	pF	4

THERMAL CONSIDERATIONS

DESCRIPTION	CONDITIONS	SYMBOL	TYP	UNITS	NOTES
Thermal resistance - Junction to Ambient	Still Air	θ_{JA}	65	°C/W	
Thermal resistance - Junction to Case		θ_{JC}	6	°C/W	
Maximum Case Temperature		TC	110	°C	11

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ±5%)

		-7		-10		-12		-15			
DESCRIPTION	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Clock											
Clock cycle time	tKC	15		20		25		30		ns	
Clock HIGH time	tKH	5		7		9		11		ns	
Clock LOW time	tKL	5		7		9		11		ns	
Output Times											
Clock to output valid	tKQ		7		10		12		15	ns	
Clock to output invalid	tKQX	3		3		3		3		ns	
Clock to output in Low-Z	tKQLZ	2		2		2		2		ns	6, 7
Clock to output in High-Z	tKQHZ		5		6		6		6	ns	6, 7
$\overline{OE}$ to output valid	tOEQ		5		6		7		8	ns	9
$\overline{OE}$ to output in Low-Z	tOELZ	0		0		0		0		ns	6, 7
$\overline{OE}$ to output in High-Z	tOEHZ		5		6		6		6	ns	6, 7
Setup Times											
Address	tAS	2.5		3		3		3		ns	8, 10
Address Status ($\overline{ADSC}$, $\overline{ADSP}$)	tADSS	2.5		3		3		3		ns	8, 10
Address Advance ($\overline{ADV}$)	tAAS	2.5		3		3		3		ns	8, 10
Byte Write Enables ($\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, $\overline{BW4}$)	tWS	2.5		3		3		3		ns	8, 10
Data-in	tDS	2.5		3		3		3		ns	8, 10
Chip Enables ($\overline{CE}$, $\overline{CE2}$, CE2)	tCES	2.5		3		3		3		ns	8, 10
Hold Times											
Address	tAH	0.5		0.5		0.5		0.5		ns	8, 10
Address Status ($\overline{ADSC}$, $\overline{ADSP}$)	tADSH	0.5		0.5		0.5		0.5		ns	8, 10
Address Advance ($\overline{ADV}$)	tAAH	0.5		0.5		0.5		0.5		ns	8, 10
Byte Write Enables ($\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, $\overline{BW4}$)	tWH	0.5		0.5		0.5		0.5		ns	8, 10
Data-in	tD	0.5		0.5		0.5		0.5		ns	8, 10
Chip Enables ($\overline{CE}$, $\overline{CE2}$, CE2)	tCEH	0.5		0.5		0.5		0.5		ns	8, 10

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	1.5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

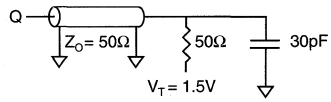


Fig. 1 OUTPUT LOAD EQUIVALENT

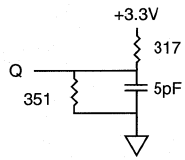
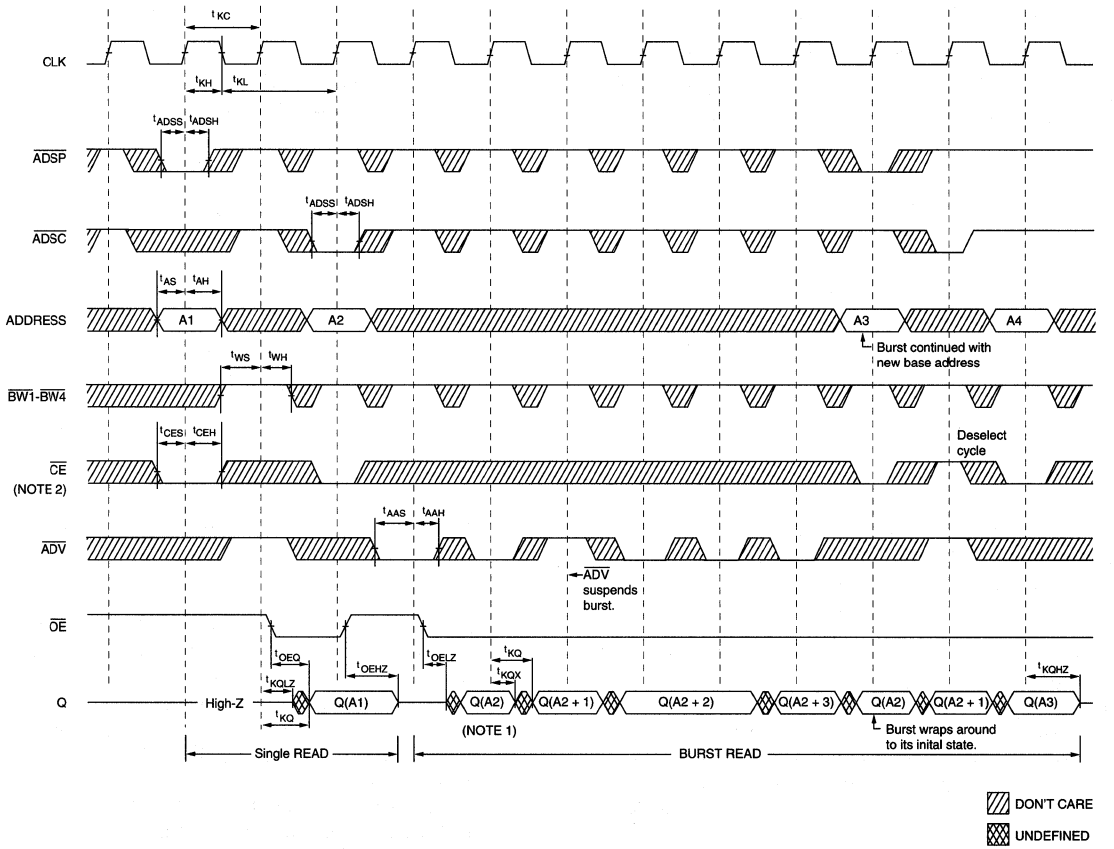


Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

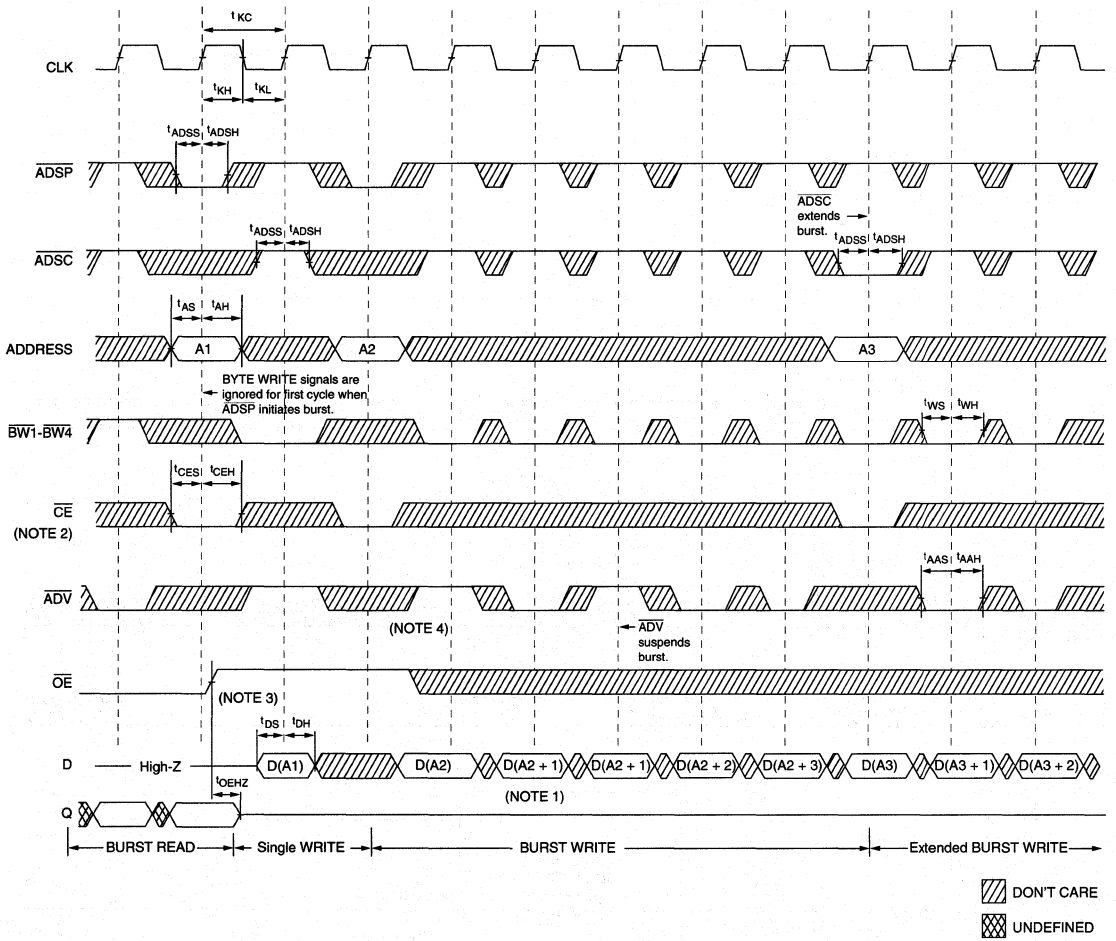
1. All voltages referenced to Vss (GND).
2. Overshoot: $V_{IH} \leq +6.0V$ for $t \leq {}^tKC/2$.
   Undershoot: $V_{IL} \geq -2.0V$ for $t \leq {}^tKC/2$.
   Power-up: $V_{IH} \leq +6.0V$ and $Vcc \leq 3.1V$ for $t \leq 200msec$.
3. Icc is given with no output current. Icc increases with greater output loading and faster cycle times.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. Output loading is specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ${}^tKQHZ$ is less than ${}^tKQLZ$ and ${}^tOEHZ$ is less than ${}^tOELZ$.
8. A READ cycle is defined by byte write enables all HIGH or $\overline{ADSP}$ LOW for the required setup and hold times. A WRITE cycle is defined by at least one byte write enable LOW and $\overline{ADSP}$ HIGH for the required setup and hold times.
9. $\overline{OE}$ is a "don't care" when a byte write enable is sampled LOW.
10. This is a synchronous device. All addresses must meet the specified setup and hold times for all rising edges of CLK when either $\overline{ADSP}$ or $\overline{ADSC}$ is LOW and chip enabled. All other synchronous inputs must meet the setup and hold times with stable logic levels for all rising edges of clock (CLK) when chip is enabled. Chip enable must be valid at each rising edge of CLK (when either $\overline{ADSP}$ or $\overline{ADSC}$ is LOW) to remain enabled.
11. Micron does not warrant the functionality or reliability of any product in which the case temperature exceeds 110°C. Care should be taken to limit case temperature to acceptable levels.
12. "Device Deselected" means device is in POWER-DOWN mode as defined in the truth table. "Device Selected" means device is active (not in POWER-DOWN mode).
13. Typical values are measured at 3.3V, 25°C and 20ns cycle time.

READ TIMING



NOTE:
1. Q(A2) refers to output from address A2. Q(A2+1) refers to output from the next internal burst address following A2.
2. $\overline{CE2}$ and CE2 have timing identical to $\overline{CE}$. On this diagram, when $\overline{CE}$ is LOW, $\overline{CE2}$ is LOW and CE2 is HIGH. When $\overline{CE}$ is HIGH, $\overline{CE2}$ is HIGH and CE2 is LOW.

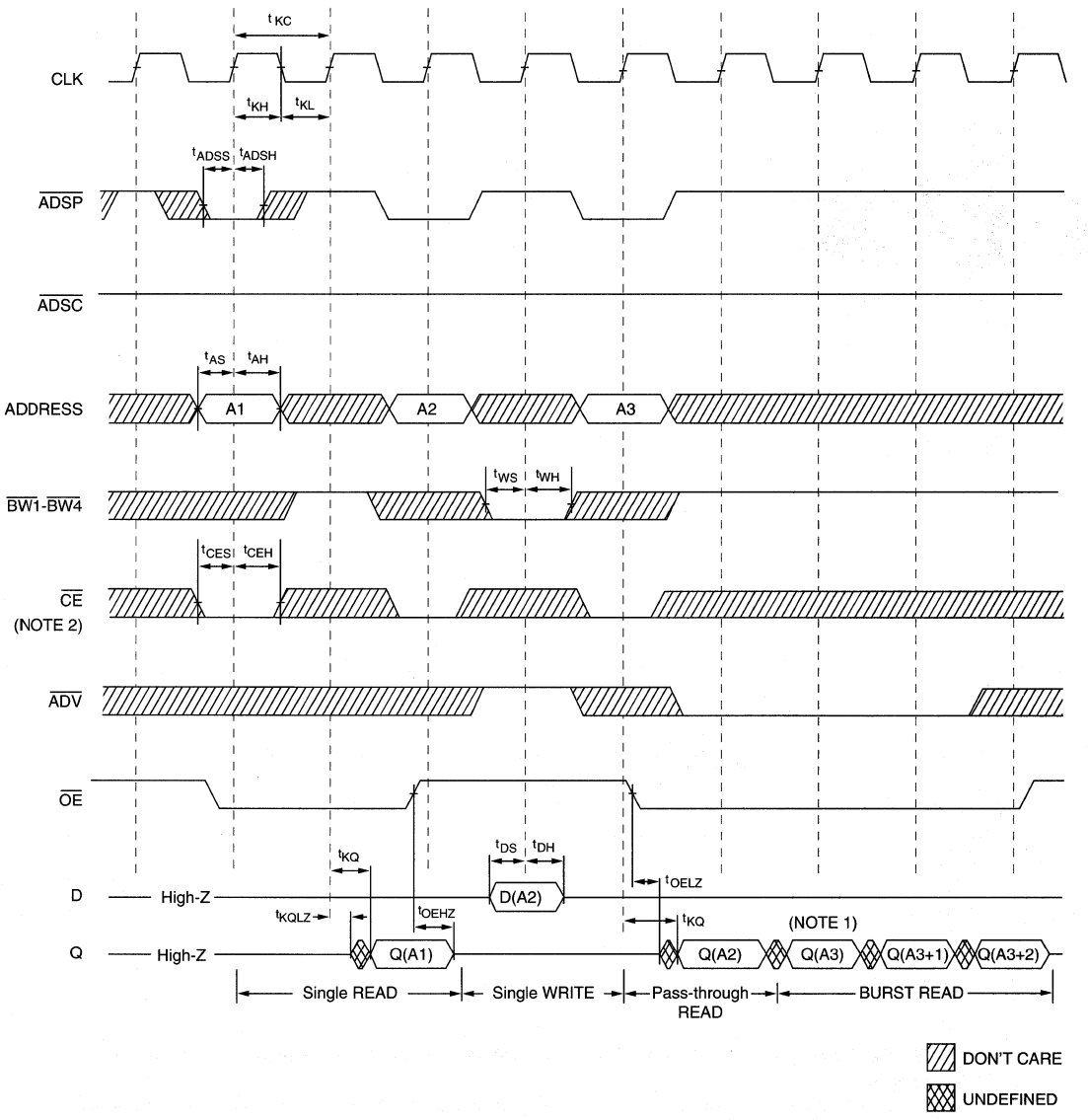
WRITE TIMING



NOTE:

1. Q(A2) refers to output from address A2. Q(A2+1) refers to output from the next internal burst address following A2.
2. $\overline{CE2}$ and CE2 have timing identical to $\overline{CE}$. On this diagram, when $\overline{CE}$ is LOW, $\overline{CE2}$ is LOW and CE2 is HIGH. When $\overline{CE}$ is HIGH, $\overline{CE2}$ is HIGH and CE2 is LOW.
3. $\overline{OE}$ must be HIGH before the input data setup and held HIGH throughout the the data hold time. This prevents input/output data contention for the time period prior to the byte write enable inputs being sampled.
4. $\overline{ADV}$ must be HIGH to permit a WRITE to the loaded address.

READ/WRITE TIMING



NOTE:
1. Q(A3) refers to output from address A3. Q(A3+1) refers to output from the next internal burst address following A3.
2. $\overline{CE2}$ and CE2 have timing identical to $\overline{CE}$. On this diagram, when $\overline{CE}$ is LOW, $\overline{CE2}$ is LOW and CE2 is HIGH. When $\overline{CE}$ is HIGH, $\overline{CE2}$ is HIGH and CE2 is LOW.

APPLICATION INFORMATION

32-BIT-WIDE SYSTEMS

The Micron 32K x 36 Synchronous SRAM may be used in a 32-bit-wide system without the use of any external components by connecting PDIS to Vcc. This disables the output buffer on the data parity input/output lines (DQP1, DQP2, DQP3 and DQP4).

LOAD DERATING CURVES

The Micron 32K x 36 Synchronous SRAM timing is dependent upon the capacitive loading on the outputs. The data sheet is written assuming a load of 30pF. Access time changes with load capacitance as follows:

$\Delta^{t}KC = 0.016$ ns/pF x ΔC_L pF. (Note: this is preliminary information subject to change.)

For example, if the SRAM loading is 22pF, ΔC_L is -8pF (8pF less than rated load). The clock to valid output time of the SRAM is reduced by 0.016 x 8 = 0.128ns. If the device is a 7ns part, the worse case ^{t}KC becomes 6.87ns (approximately).

Consult the factory for copies of I/O current versus voltage curves and Quad Design models.

DEPTH EXPANSION

The Micron 32K x 36 Synchronous SRAM incorporates two additional chip enables to facilitate simple depth expansion. This permits easy cache upgrades from 32K depth to 64K depth with no extra logic as shown in Figure 3.

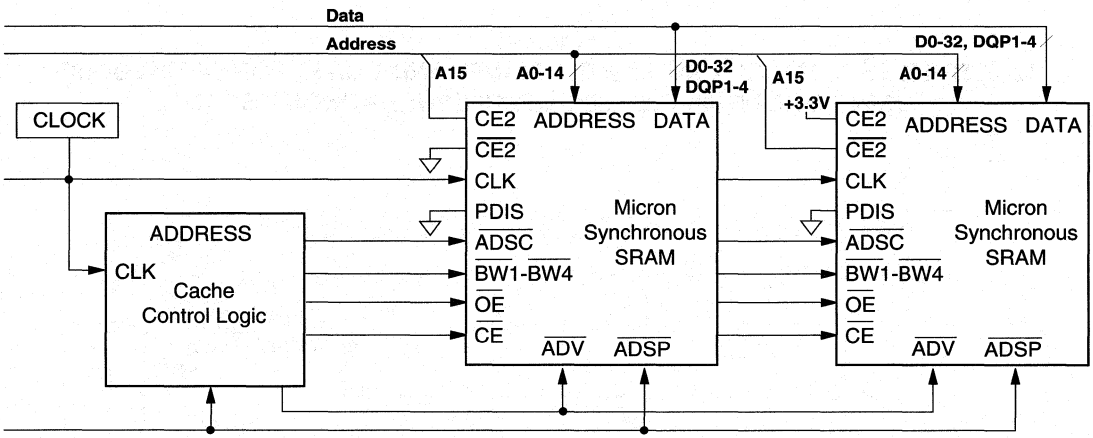


Figure 3
DEPTH EXPANSION FROM 32K x 36 TO 64K x 36

APPLICATION EXAMPLES

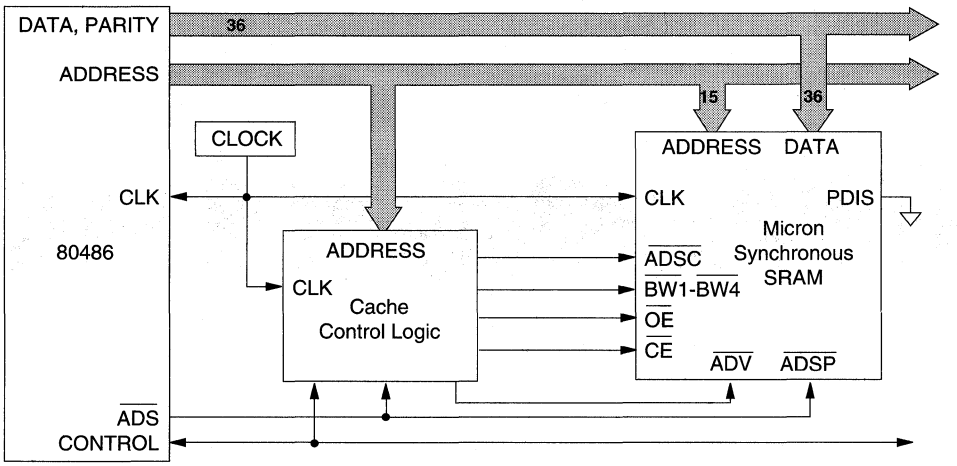


Figure 4
128K BYTE SECONDARY CACHE WITH PARITY AND BURST FOR 50 MHz 80486 USING ONE MT58LC32K36C4LG-10 SYNCHRONOUS SRAM

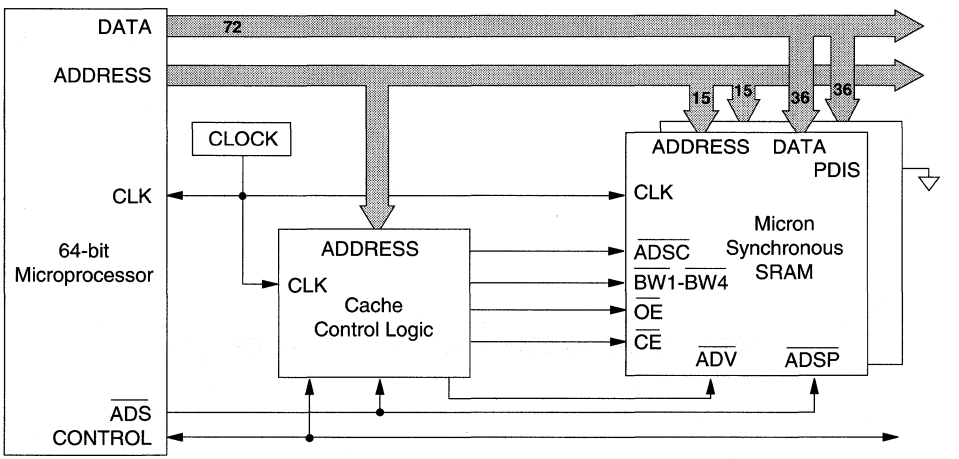


Figure 5
256K BYTE SECONDARY CACHE WITH PARITY AND BURST FOR 66 MHz PENTIUM MICROPROCESSOR USING TWO MT58LC32K36C4LG-7 SYNCHRONOUS SRAMs

MICRON SEMICONDUCTOR, INC.

MT58LC32K36M1
32K x 36 SYNCHRONOUS SRAM

SYNCHRONOUS SRAM

32K x 36 SRAM

+3.3V SUPPLY WITH CLOCKED, REGISTERED INPUTS AND LINEAR BURST COUNTER

NEW ■ 3.3 VOLT SYNCHRONOUS SRAM

FEATURES

- Fast access times: 9, 10, 12 and 17ns
- Fast $\overline{OE}$: 5, 6 and 7ns
- Single +3.3V ±5% power supply
- 5V-tolerant I/O
- Common data inputs and data outputs
- Individual BYTE WRITE control
- Three Chip Enables for simple depth expansion
- Clock controlled, registered, address, data and control
- Internally self-timed WRITE cycle
- Burst control pins (linear burst sequence)
- 100-lead TQFP package for high density, high speed
- Low capacitive bus loading
- High 30pF output drive capability at rated access time
- Parity Disable function for 32-bit operation

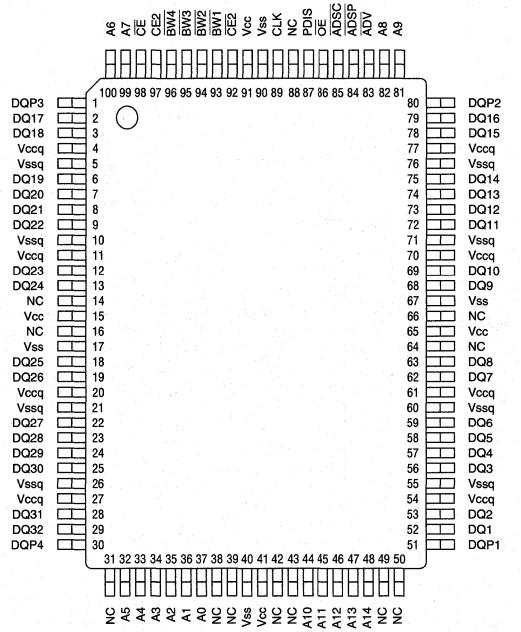
OPTIONS MARKING

- Timing
  - 9ns access/15ns cycle - 9
  - 10ns access/15ns cycle -10
  - 12ns access/20ns cycle -12
  - 17ns access/25ns cycle -17
- Packages
  - 100-pin TQFP LG
- Part Number Example: MT58LC32K36M1LG-12

NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

100-Pin TQFP
(SC-1)



GENERAL DESCRIPTION

The Micron Synchronous SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

The MT58LC32K36M1 SRAM integrates a 32K x 36 SRAM core with advanced synchronous peripheral circuitry and a 2-bit burst counter. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input (CLK). The synchronous inputs include all addresses, all data inputs, active LOW chip enable ($\overline{CE}$), two additional chip enables for easy depth expansion ($\overline{CE2}$, CE2), burst control inputs ($\overline{ADSC}$, $\overline{ADSP}$, $\overline{ADV}$) and the byte write enables ($\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, $\overline{BW4}$).

Asynchronous inputs include the output enable ($\overline{OE}$) and the clock (CLK). The data-out (Q), enabled by $\overline{OE}$, is also asynchronous. WRITE cycles can be from one to four bytes wide as controlled by the byte write enables.

Burst operation can be initiated with either address status processor ($\overline{ADSP}$) or address status controller ($\overline{ADSC}$) input pins. Subsequent burst addresses can be internally generated as controlled by the burst advance pin ($\overline{ADV}$).

Address and write control are registered on-chip to simplify WRITE cycles. This allows self-timed WRITE cycles. Individual byte enables allow individual bytes to be written. $\overline{BW1}$ controls DQ1-DQ8 and DQP1, $\overline{BW2}$ controls DQ9-DQ16 and DQP2, $\overline{BW3}$ controls DQ17-DQ24 and

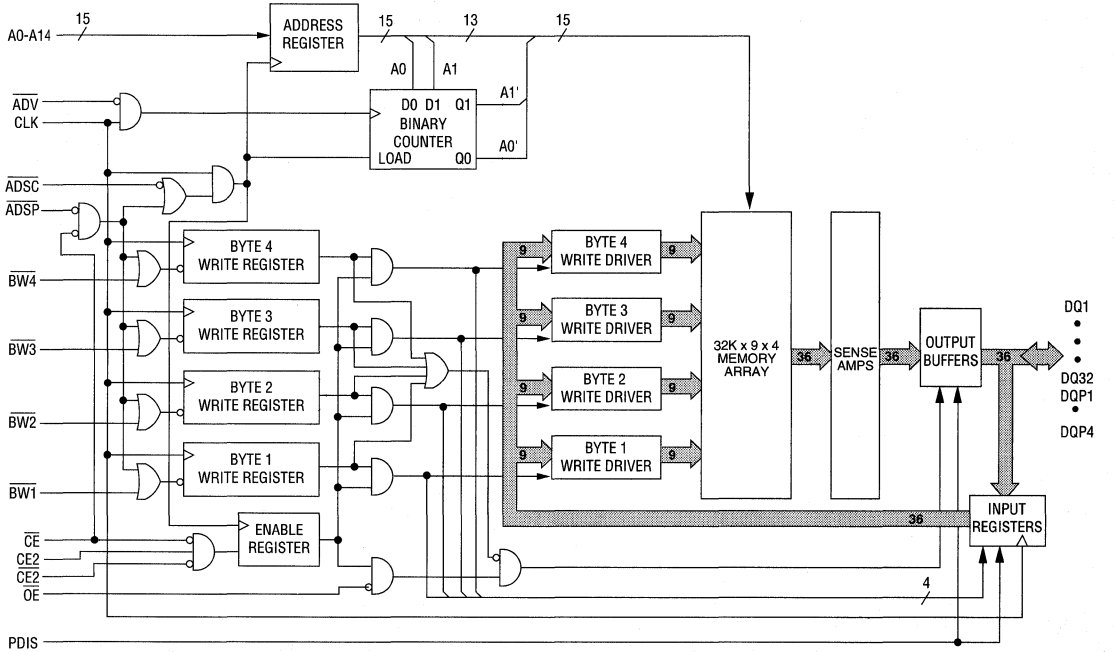
NEW ■ 3.3 VOLT SYNCHRONOUS SRAM

GENERAL DESCRIPTION (continued)

DQP3, and $\overline{BW4}$ controls DQ25-DQ32 and DQP4.

The MT58LC32K36M1 operates from a +3.3V power supply and all inputs and outputs are TTL-compatible and 5V tolerant. The device is ideally suited for PowerPC™, 680X0 and any other system which benefits from a very wide data bus and linear-burst synchronous operation. The device can also be used in 32-, 64- and 72-bit wide applications.

FUNCTIONAL BLOCK DIAGRAM



NOTE: 1. The Functional Block Diagram illustrates simplified device operation. See Truth Table, pin descriptions and timing diagrams for detailed information.

PIN DESCRIPTIONS

TQFP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
37, 36, 35, 34, 33, 32, 100, 99, 82, 81, 44, 45, 46, 47, 48	A0-A14	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK.
93, 94, 95, 96	$\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, $\overline{BW4}$	Input	Synchronous Byte Write Enables: These active LOW inputs allow individual bytes to be written and must meet the setup and hold times around the rising edge of CLK. A byte write enable is LOW for a WRITE cycle and HIGH for a READ cycle. $\overline{BW1}$ controls DQ1-DQ8 and DQP1. $\overline{BW2}$ controls DQ9-DQ16 and DQP2. $\overline{BW3}$ controls DQ17-DQ24 and DQP3. $\overline{BW4}$ controls DQ25-DQ32 and DQP4. Data I/O are tristated if any of these four inputs are LOW.
89	CLK	Input	Clock: This signal registers the address, data, chip enables, byte write enables and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
98	$\overline{CE}$	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and conditions internal use of $\overline{ADSP}$. This input is sampled only when a new external address is loaded.
92	$\overline{CE2}$	Input	Synchronous Chip Enable: This active LOW input is used to enable the device. This input is sampled only when a new external address is loaded. This input can be used for memory depth expansion.
97	CE2	Input	Synchronous Chip Enable: This active HIGH input is used to enable the device. This input is sampled only when a new external address is loaded. This input can be used for memory depth expansion.
86	$\overline{OE}$	Input	Output Enable: This active LOW asynchronous input enables the data I/O output drivers.
83	$\overline{ADV}$	Input	Synchronous Address Advance: This active LOW input is used to advance the internal burst counter, controlling burst access after the external address is loaded. A HIGH on this pin effectively causes wait states to be generated (no address advance). This pin must be HIGH at the rising edge of the first clock after an $\overline{ADSP}$ cycle is initiated if a WRITE cycle is desired (to ensure use of correct address).
84	$\overline{ADSP}$	Input	Synchronous Address Status Processor: This active LOW input interrupts any ongoing burst, causing a new external address to be registered. A READ is performed using the new address, independent of the byte write enables and $\overline{ADSC}$ but dependent upon CE2 and $\overline{CE2}$. $\overline{ADSP}$ is ignored if $\overline{CE}$ is HIGH. Power-down state is entered if CE2 is LOW or $\overline{CE2}$ is HIGH.
85	$\overline{ADSC}$	Input	Synchronous Address Status Controller: This active LOW input interrupts any ongoing burst and causes a new external address to be registered. A READ or WRITE is performed using the new address if all chip enables are active. Power-down state is entered if one or more chip enables are inactive.

PIN DESCRIPTIONS (continued)

TQFP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
14, 16, 31, 38, 39, 42, 43, 49, 50, 64, 66, 88	NC	-	No Connect: These signals are not internally connected.
52, 53, 56, 57, 58, 59, 62, 63, 68, 69, 72, 73, 74, 75, 78, 79, 2, 3, 6, 7, 8, 9, 12, 13, 18, 19, 22, 23, 24, 25, 28, 29	DQ1-DQ32	Input/ Output	SRAM Data I/O: Byte 1 is DQ1-DQ8; Byte 2 is DQ9-DQ16; Byte 3 is DQ17-DQ24; Byte 4 is DQ25-DQ32. Input data must meet setup and hold times around the rising edge of CLK.
51, 80, 1, 30	DQP1-DQP4	Input/ Output	Parity Data I/O: Byte 1 Parity is DQP1; Byte 2 Parity is DQP2; Byte 3 Parity is DQP3; Byte 4 Parity is DQP4.
87	PDIS	Input	Parity Disable: When HIGH, this input disables DQP1 through DQP4 for 32-bit data bus width. A LOW on PDIS enables control of DQP1 through DQP4 in the same manner as DQ1-DQ32 are controlled.
15, 41, 65, 91	Vcc	Supply	Power Supply: +3.3V ±5%
17, 40, 67, 90	Vss	Supply	Ground: GND
4, 11, 20, 27, 54, 61, 70, 77	VccQ	Supply	Isolated Output Buffer Supply: +3.3V ±5%
5, 10, 21, 26, 55, 60, 71, 76	VssQ	Supply	Isolated Output Buffer Ground: GND

BURST ADDRESS TABLE

First Address	Second Address	Third Address	Fourth Address
X...X00	X...X01	X...X10	X...X11
X...X01	X...X10	X...X11	X...X00
X...X10	X...X11	X...X00	X...X01
X...X11	X...X00	X...X01	X...X10

TRUTH TABLE

OPERATION	ADDRESS USED	$\overline{CE}$	$\overline{CE2}$	CE2	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Deselected Cycle, Power-down	None	H	X	X	X	L	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	None	L	X	L	L	X	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	None	L	H	X	L	X	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	None	L	X	L	H	L	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	None	L	H	X	H	L	X	X	X	L-H	High-Z
READ Cycle, Begin Burst	External	L	L	H	L	X	X	X	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	L	X	X	X	H	L-H	High-Z
WRITE Cycle, Begin Burst	External	L	L	H	H	L	X	L	X	L-H	D
READ Cycle, Begin Burst	External	L	L	H	H	L	X	H	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	H	L	X	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	X	X	X	H	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	X	X	X	H	H	L	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	H	X	X	X	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	H	X	X	X	H	L	H	H	L-H	High-Z
WRITE Cycle, Continue Burst	Next	X	X	X	H	H	L	L	X	L-H	D
WRITE Cycle, Continue Burst	Next	H	X	X	X	H	L	L	X	L-H	D
READ Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	H	L-H	High-Z
READ Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	H	L-H	High-Z
WRITE Cycle, Suspend Burst	Current	X	X	X	H	H	H	L	X	L-H	D
WRITE Cycle, Suspend Burst	Current	H	X	X	X	H	H	L	X	L-H	D

NOTE:
1. X means "don't care." H means logic HIGH. L means logic LOW. $\overline{WRITE}$=L means any one or more byte write enable signals ($\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$ or $\overline{BW4}$) are LOW. $\overline{WRITE}$=H means all byte write enable signals are HIGH.
2. $\overline{BW1}$ enables writes to Byte 1 (DQ1-DQ8, DQP1). $\overline{BW2}$ enables writes to Byte 2 (DQ9-DQ16, DQP2). $\overline{BW3}$ enables writes to Byte 3 (DQ17-DQ24, DQP3). $\overline{BW4}$ enables writes to Byte 4 (DQ25-DQ32, DQP4).
3. All inputs except $\overline{OE}$ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
4. Wait states are inserted by suspending burst.
5. For a write operation following a read operation, $\overline{OE}$ must be HIGH before the input data required setup time and held HIGH throughout the input data hold time.
6. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
7. PDIS disables the DQP lines when HIGH and enables the DQP lines when LOW.
8. $\overline{ADSP}$ LOW always initiates an internal READ at the L-H edge of CLK. A WRITE is performed by setting one or more byte write enable signals LOW for the subsequent L-H edge of CLK. Refer to WRITE timing diagram for clarification.

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ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to Vss .....-0.5V to +4.6V
V_{IN} .....-0.5V to +6V
Storage Temperature (plastic) .....-55°C to +150°C
Junction Temperature .....+150°C
Power Dissipation 1.6W
Short Circuit Output Current 100mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; T_C ≤ 110°C; V_{CC} = 3.3V ±5% unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.0	5.5	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-1	1	µA	
Output Leakage Current	Output(s) disabled, 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	3.1	3.5	V	1

				MAX					
DESCRIPTION	CONDITIONS	SYMBOL	TYPICAL	-9	-10	-12	-17	UNITS	NOTES
Power Supply Current: Operating	Device selected; all inputs ≤ V_{IL} OR ≥ V_{IH}; cycle time ≥ ^tKC min; V_{CC} = MAX; outputs open	I_{CC}	200	275	275	250	225	mA	3, 12, 13
Power Supply Current: Idle	Device selected; $\overline{ADSC}$, $\overline{ADSP}$, $\overline{ADV}$ ≥ V_{IH}; all inputs ≤ V_{IL} OR ≥ V_{IH}; V_{CC} = MAX; cycle time ≥ ^tKC min	I_{SB1}	55	85	85	70	60	mA	12, 13
CMOS Standby	Device deselected; V_{CC} = MAX; all inputs ≤ V_{SS} +0.2 or ≥ V_{CC} -0.2; all inputs static; CLK frequency = 0	I_{SB2}	0.2	2	2	2	2	mA	12, 13
TTL Standby	Device deselected; all inputs ≤ V_{IL} OR ≥ V_{IH}; all inputs static; V_{CC} = MAX; CLK frequency = 0	I_{SB3}	10	18	18	18	18	mA	12, 13
Clock Running	Device deselected; all inputs ≤ V_{IL} OR ≥ V_{IH}; V_{CC} = MAX; CLK cycle time ≥ ^tKC min	I_{SB4}	20	35	35	30	25	mA	12, 13

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	3	4	pF	4
Input/Output Capacitance (DQ)	V_{CC} = 3.3V	C_O	5	6	pF	4

THERMAL CONSIDERATIONS

DESCRIPTION	CONDITIONS	SYMBOL	TYP	UNITS	NOTES
Thermal resistance - Junction to Ambient	Still Air	θ_{JA}	65	°C/W	
Thermal resistance - Junction to Case		θ_{JC}	6	°C/W	
Maximum Case Temperature		TC	110	°C	11

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ±5%)

		-9		-10		-12		-17			
DESCRIPTION	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Clock											
Clock cycle time	^tKC	15		20		25		30		ns	
Clock HIGH time	^tKH	4		5		6		8		ns	
Clock LOW time	^tKL	4		5		6		8		ns	
Output Times											
Clock to output valid	^tKQ		9		10		12		17	ns	
Clock to output invalid	^tKQX	3		3		3		3		ns	
Clock to output in Low-Z	^tKQLZ	5		5		5		5		ns	6, 7
Clock to output in High-Z	^tKQHZ		5		5		6		6	ns	6, 7
$\overline{OE}$ to output valid	^tOEQ		5		5		6		7	ns	9
$\overline{OE}$ to output in Low-Z	^tOELZ	0		0		0		0		ns	6, 7
$\overline{OE}$ to output in High-Z	^tOEHZ		5		5		6		6	ns	6, 7
Setup Times											
Address	^tAS	2.5		3		3		3		ns	8, 10
Address Status ($\overline{ADSC}$, $\overline{ADSP}$)	^tADSS	2.5		3		3		3		ns	8, 10
Address Advance ($\overline{ADV}$)	^tAAS	2.5		3		3		3		ns	8, 10
Byte Write Enables ($\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, $\overline{BW4}$)	^tWS	2.5		3		3		3		ns	8, 10
Data-in	^tDS	2.5		3		3		3		ns	8, 10
Chip Enables ($\overline{CE}$, $\overline{CE2}$, CE2)	^tCES	2.5		3		3		3		ns	8, 10
Hold Times											
Address	^tAH	0.5		0.5		0.5		0.5		ns	8, 10
Address Status ($\overline{ADSC}$, $\overline{ADSP}$)	^tADSH	0.5		0.5		0.5		0.5		ns	8, 10
Address Advance ($\overline{ADV}$)	^tAAH	0.5		0.5		0.5		0.5		ns	8, 10
Byte Write Enables ($\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, $\overline{BW4}$)	^tWH	0.5		0.5		0.5		0.5		ns	8, 10
Data-in	^tDH	0.5		0.5		0.5		0.5		ns	8, 10
Chip Enables ($\overline{CE}$, $\overline{CE2}$, CE2)	^tCEH	0.5		0.5		0.5		0.5		ns	8, 10

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	1.5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

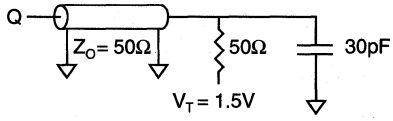


Fig. 1 OUTPUT LOAD EQUIVALENT

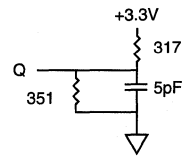
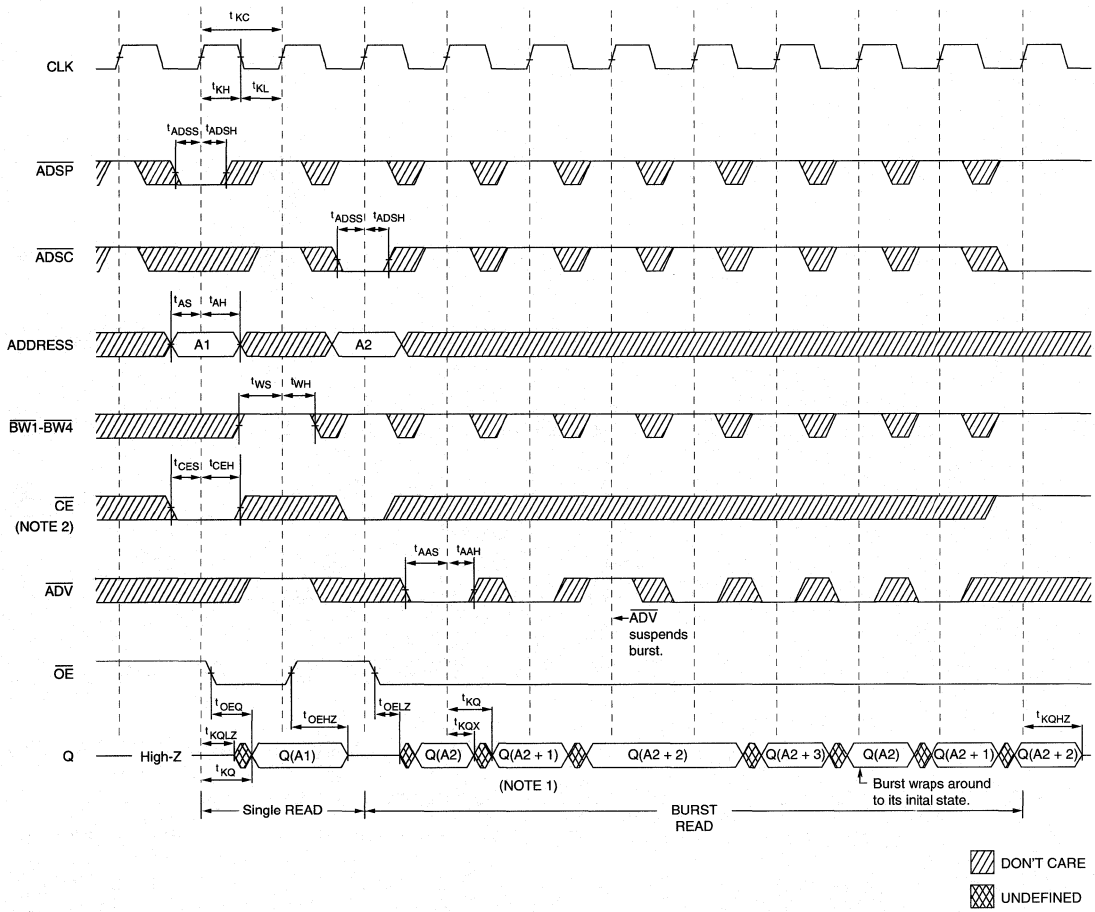


Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

1. All voltages referenced to Vss (GND).
2. Overshoot: $V_{IH} \leq +6.0V$ for $t \leq {}^tKC/2$.
   Undershoot: $V_{IL} \geq -2.0V$ for $t \leq {}^tKC/2$.
   Power-up: $V_{IH} \leq +6.0V$ and $Vcc \leq 3.1V$ for $t \leq 200msec$.
3. Icc is given with no output current. Icc increases with greater output loading and faster cycle times.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. Output loading is specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ${}^tKQHZ$ is less than ${}^tKQLZ$ and ${}^tOEHZ$ is less than ${}^tOELZ$.
8. A READ cycle is defined by byte write enables all HIGH or $\overline{ADSP}$ LOW for the required setup and hold times. A WRITE cycle is defined by at least one byte write enable LOW and $\overline{ADSP}$ HIGH for the required setup and hold times.
9. $\overline{OE}$ is a "don't care" when a byte write enable is sampled LOW.
10. This is a synchronous device. All addresses must meet the specified setup and hold times for all rising edges of CLK when either $\overline{ADSP}$ or $\overline{ADSC}$ is LOW and chip enabled. All other synchronous inputs must meet the setup and hold times with stable logic levels for all rising edges of clock (CLK) when chip is enabled. Chip enable must be valid at each rising edge of CLK (when either $\overline{ADSP}$ or $\overline{ADSC}$ is LOW) to remain enabled.
11. Micron does not warrant the functionality or reliability of any product in which the case temperature exceeds 110°C. Care should be taken to limit case temperature to acceptable levels.
12. "Device Deselected" means device is in POWER-DOWN mode as defined in the truth table. "Device Selected" means device is active (not in POWER-DOWN mode).
13. Typical values are measured at 3.3V, 25°C and 20ns cycle time.

READ TIMING



NOTE: 1. Q(A2) refers to output from address A2. Q(A2+1) refers to output from the next internal burst address following A2.

2. $\overline{CE2}$ and CE2 have timing identical to $\overline{CE}$. On this diagram, when $\overline{CE}$ is LOW, $\overline{CE2}$ is LOW and CE2 is HIGH. When $\overline{CE}$ is HIGH, $\overline{CE2}$ is HIGH and CE2 is LOW.

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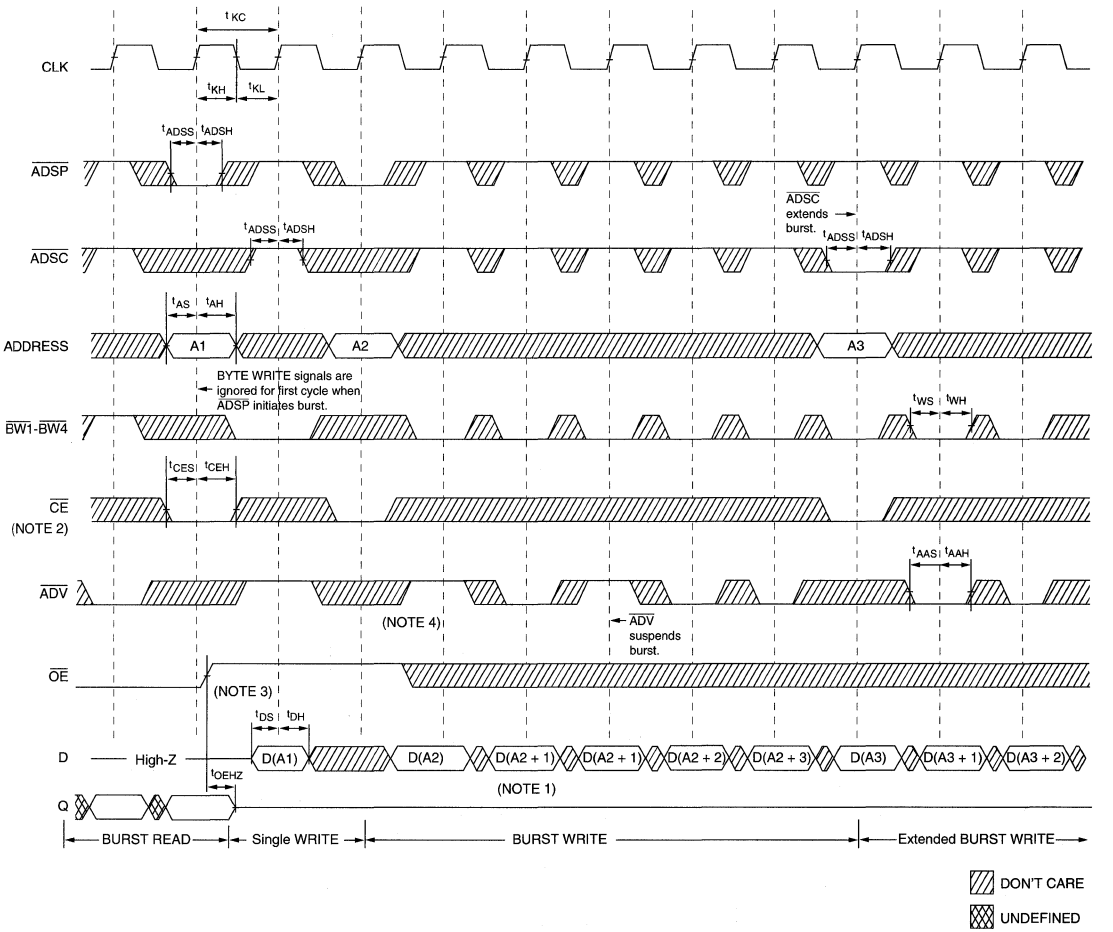
WRITE TIMING

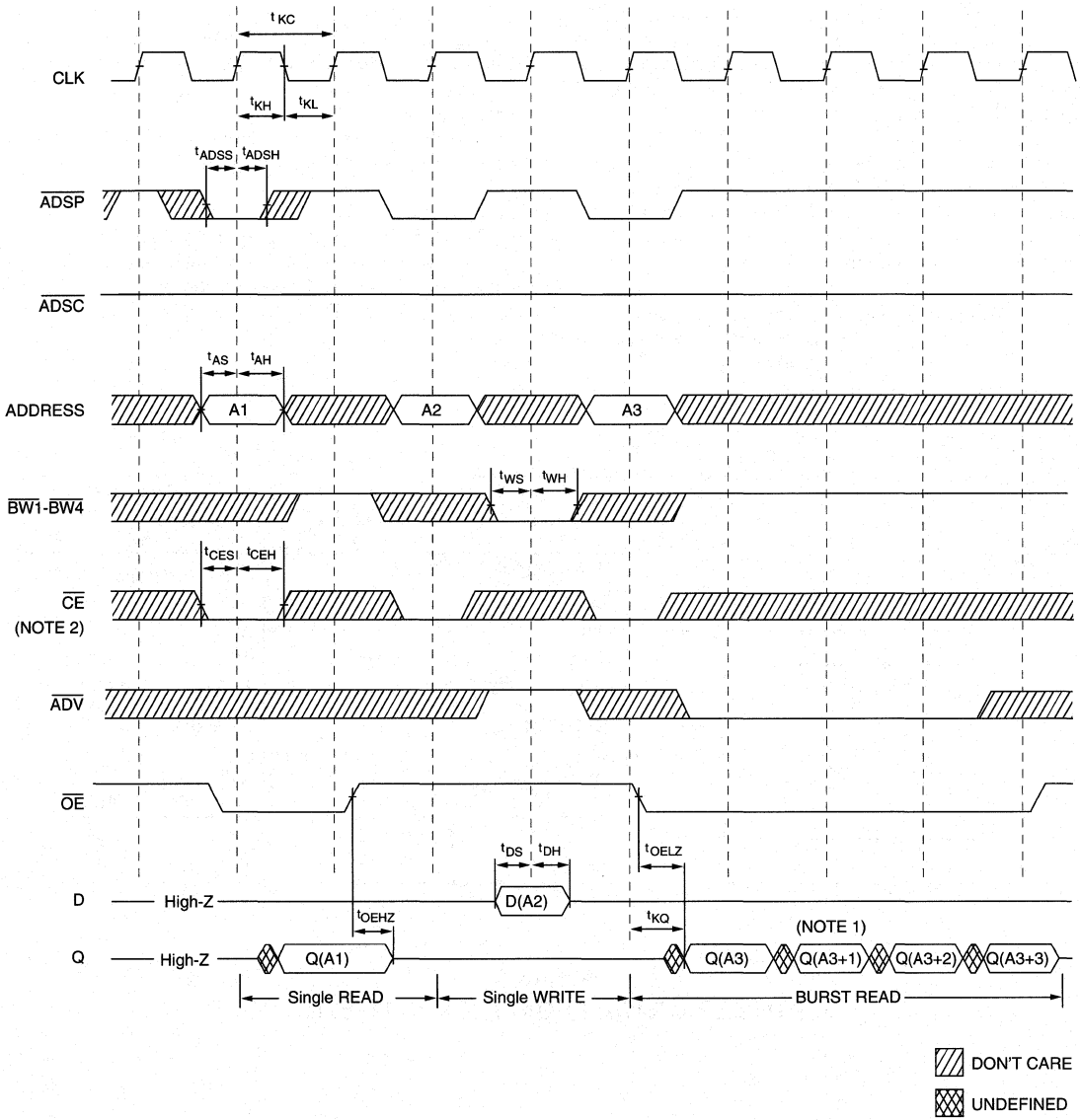


NOTE:

1. Q(A2) refers to output from address A2. Q(A2+1) refers to output from the next internal burst address following A2.
2. $\overline{CE2}$ and CE2 have timing identical to $\overline{CE}$. On this diagram, when $\overline{CE}$ is LOW, $\overline{CE2}$ is LOW and CE2 is HIGH. When $\overline{CE}$ is HIGH, $\overline{CE2}$ is HIGH and CE2 is LOW.
3. $\overline{OE}$ must be HIGH before the input data setup and held HIGH throughout the the data hold time. This prevents input/output data contention for the time period prior to the byte write enable inputs being sampled.
4. $\overline{ADV}$ must be HIGH to permit a WRITE to the loaded address.

NEW 3.3 VOLT SYNCHRONOUS SRAM

READ/WRITE TIMING



NOTE: 1. Q(A3) refers to output from address A3. Q(A3+1) refers to output from the next internal burst address following A3.

2. $\overline{CE2}$ and CE2 have timing identical to $\overline{CE}$. On this diagram, when $\overline{CE}$ is LOW, $\overline{CE2}$ is LOW and CE2 is HIGH. When $\overline{CE}$ is HIGH, $\overline{CE2}$ is HIGH and CE2 is LOW.

NEW 3.3 VOLT SYNCHRONOUS SRAM

APPLICATION INFORMATION

32-BIT-WIDE SYSTEMS

The Micron 32K x 36 Synchronous SRAM may be used in a 32-bit-wide system without the use of any external components by connecting PDIS to Vcc. This disables the output buffer on the data parity input/output lines (DQP1, DQP2, DQP3 and DQP4).

LOAD DERATING CURVES

The Micron 32K x 36 Synchronous SRAM timing is dependent upon the capacitive loading on the outputs. The data sheet is written assuming a load of 30pF. Access time changes with load capacitance as follows:

$\Delta^tKQ = 0.016$ ns/pF x ΔC_L pF. (Note: this is preliminary information subject to change.)

For example, if the SRAM loading is 22pF, ΔC_L is -8pF (8pF less than rated load). The clock to valid output time of the SRAM is reduced by 0.016 x 8 = 0.128ns. If the device is a 12ns part, the worse case ^tKQ becomes 11.87ns (approximately).

Consult the factory for copies of I/O current versus voltage curves and Quad Design models.

DEPTH EXPANSION

The Micron 32K x 36 Synchronous SRAM incorporates two additional chip enables to facilitate simple depth expansion. This permits easy cache upgrades from 32K depth to 64K depth with no extra logic as shown in Figure 3.

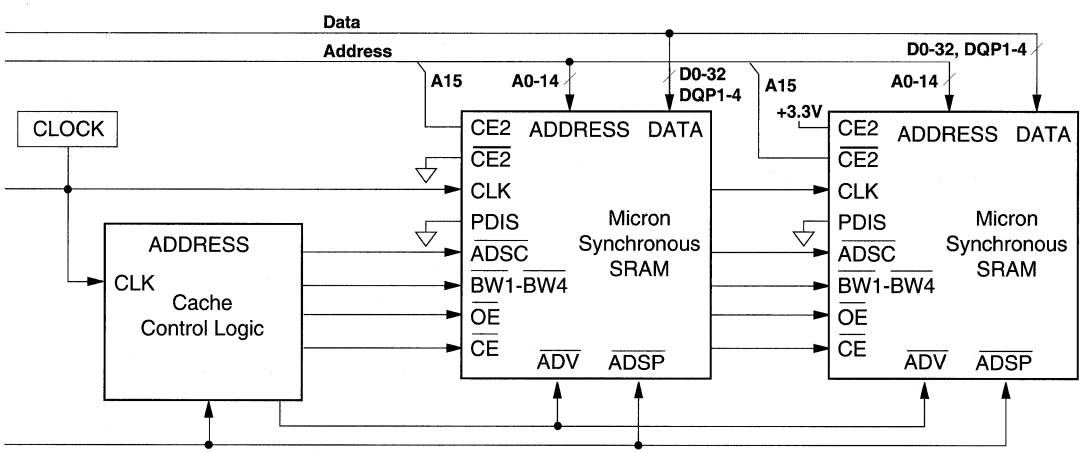


Figure 3
DEPTH EXPANSION FROM 32K x 36 TO 64K x 36

APPLICATION EXAMPLES

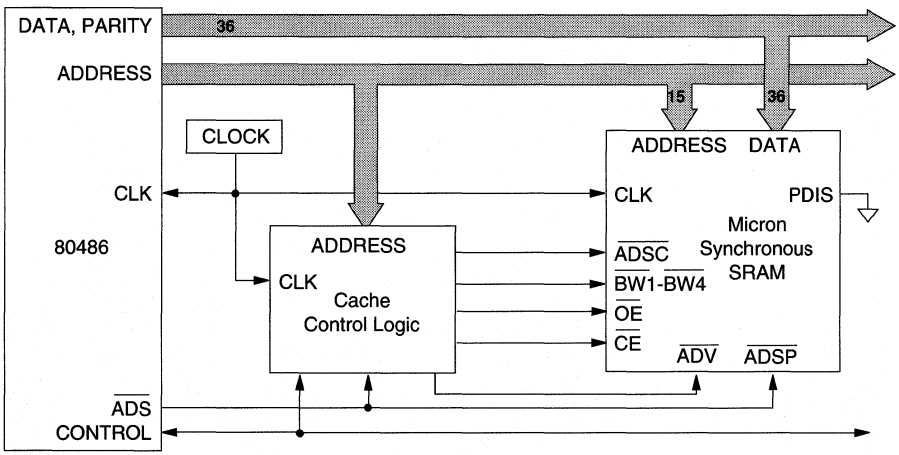


Figure 4
128K BYTE SECONDARY CACHE WITH PARITY AND BURST FOR 50 MHz 80486 OR 680X0 USING ONE MT58LC32K36M1LG-12 SYNCHRONOUS SRAM

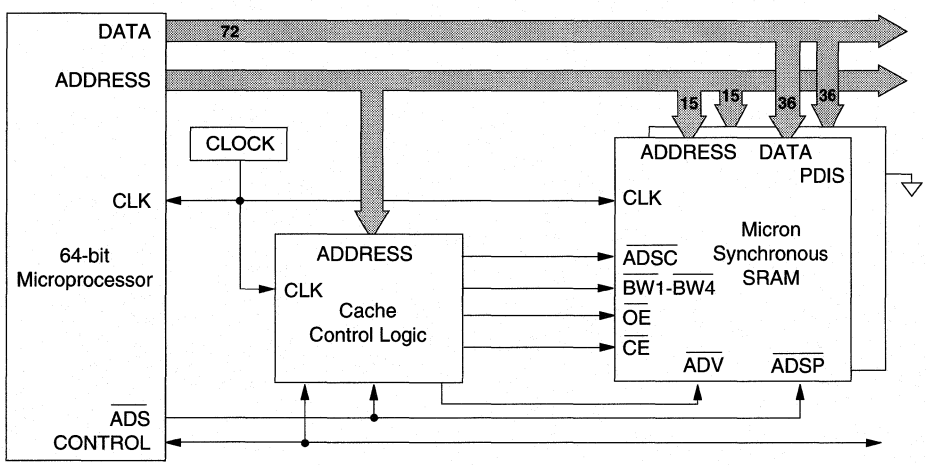


Figure 5
256K BYTE SECONDARY CACHE WITH PARITY AND BURST FOR 66 MHz PROCESSOR USING TWO MT58LC32K36M1LG-9 SYNCHRONOUS SRAMs

MICRON SEMICONDUCTOR, INC.

MT58LC32K36M1
32K x 36 SYNCHRONOUS SRAM

SYNCHRONOUS SRAM

32K x 36 SRAM

+3.3V SUPPLY, FULLY REGISTERED I/O AND LINEAR BURST COUNTER

FEATURES

- Fast access times: 7, 10, 12 and 15ns
- Fast $\overline{OE}$: 5, 6, 7 and 8ns
- Single +3.3V ±5% power supply
- 5V-tolerant I/O
- Common data inputs and data outputs
- Individual BYTE WRITE control
- Three chip enables for simple depth expansion
- Clock controlled, registered, address, data I/O and control for fully pipelined applications
- Internally self-timed WRITE cycle
- WRITE pass-through capability
- Burst control pins (linear burst sequence)
- 100-lead TQFP package for high density, high speed
- Low capacitive bus loading
- High 30pF output drive capability at rated access time
- Parity Disable function for 32-bit operation

OPTIONS

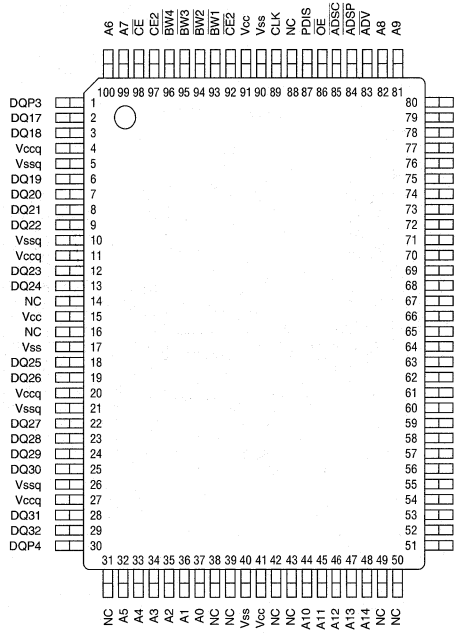
	MARKING
• Timing	
7ns access/15ns cycle	- 7
10ns access/20ns cycle	-10
12ns access/25ns cycle	-12
15ns access/30ns cycle	-15
• Packages	
100-pin TQFP	LG

- Part Number Example: MT58LC32K36A6LG-10

NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

100-Pin TQFP
(SC-1)



GENERAL DESCRIPTION

The Micron Synchronous SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

The MT58LC32K36A6 SRAM integrates a 32K x 36 SRAM core with advanced synchronous peripheral circuitry, a 2-bit burst counter and output register. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input (CLK). The synchronous inputs include all addresses, all data inputs, active LOW chip enable, two additional chip enables for easy depth expansion ($\overline{CE2}$, CE2), burst control inputs ($\overline{ADSC}$, $\overline{ADSP}$, $\overline{ADV}$) and the byte write enables ($\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, $\overline{BW4}$).

Asynchronous inputs include the output enable ($\overline{OE}$), and the clock (CLK). The data-out (Q), enabled by $\overline{OE}$, are also asynchronous. The output register is controlled by the clock. WRITE cycles can be from one to four bytes wide as controlled by the byte write enables.

Burst operation can be initiated with either address status processor ($\overline{ADSP}$) or address status controller ($\overline{ADSC}$) input pins. Subsequent burst addresses can be internally generated as controlled by the burst advance pin ($\overline{ADV}$).

Address and write control are registered on-chip to simplify WRITE cycles. This allows self-timed WRITE cycles. Individual byte enables allow individual bytes to be written. WRITE pass-through makes written data immediately

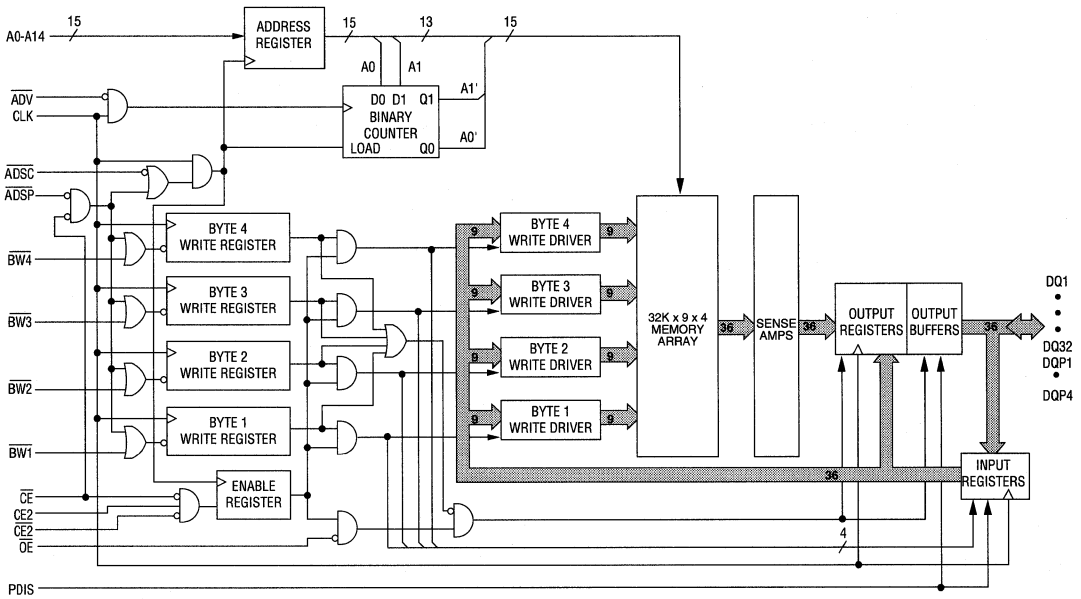
NEW ■ 3.3 VOLT SYNCHRONOUS SRAM

GENERAL DESCRIPTION (continued)

available at the output register during the READ cycle following a WRITE as controlled solely by $\overline{OE}$ to improve cache system response.

The MT58LC32K36A6 operates from a +3.3V power supply and all inputs and outputs are TTL-compatible and 5V tolerant. The device is ideal for PowerPC™ pipelined applications and 32-, 64- and 72-bit-wide applications.

FUNCTIONAL BLOCK DIAGRAM



NOTE: 1. The Functional Block Diagram illustrates simplified device operation. See Truth Table, pin descriptions and timing diagrams for detailed information.

PIN DESCRIPTIONS

TQFP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
37, 36, 35, 34, 33, 32, 100, 99, 82, 81, 44, 45, 46, 47, 48	A0-A14	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK.
93, 94, 95, 96	$\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, $\overline{BW4}$	Input	Synchronous Byte Write Enables: These active LOW inputs allow individual bytes to be written and must meet the setup and hold times around the rising edge of CLK. A byte write enable is LOW for a WRITE cycle and HIGH for a READ cycle. $\overline{BW1}$ controls DQ1-DQ8 and DQP1. $\overline{BW2}$ controls DQ9-DQ16 and DQP2. $\overline{BW3}$ controls DQ17-DQ24 and DQP3. $\overline{BW4}$ controls DQ25-DQ32 and DQP4. Data I/O are tristated if any of these four inputs are LOW.
89	CLK	Input	Clock: This signal registers the address, data, chip enables, byte write enables and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
98	$\overline{CE}$	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and conditions internal use of $\overline{ADSP}$. This input is sampled only when a new external address is loaded.
92	$\overline{CE2}$	Input	Synchronous Chip Enable: This active LOW input is used to enable the device. This input is sampled only when a new external address is loaded. This input can be used for memory depth expansion.
97	CE2	Input	Synchronous Chip Enable: This active HIGH input is used to enable the device. This input is sampled only when a new external address is loaded. This input can be used for memory depth expansion.
86	$\overline{OE}$	Input	Output Enable: This active LOW asynchronous input enables the data I/O output drivers.
83	$\overline{ADV}$	Input	Synchronous Address Advance: This active LOW input is used to advance the internal burst counter, controlling burst access after the external address is loaded. A HIGH on this pin effectively causes wait states to be generated (no address advance). This pin must be HIGH at the rising edge of the first clock after an $\overline{ADSP}$ cycle is initiated if a WRITE cycle is desired (to ensure use of correct address).
84	$\overline{ADSP}$	Input	Synchronous Address Status Processor: This active LOW input interrupts any ongoing burst, causing a new external address to be registered. A READ is performed using the new address, independent of the byte write enables and $\overline{ADSC}$ but dependent upon CE2 and $\overline{CE2}$. $\overline{ADSP}$ is ignored if $\overline{CE}$ is HIGH. Power-down state is entered if CE2 is LOW or $\overline{CE2}$ is HIGH.
85	$\overline{ADSC}$	Input	Synchronous Address Status Controller: This active LOW input interrupts any ongoing burst and causes a new external address to be registered. A READ or WRITE is performed using the new address if all chip enables are active. Power-down state is entered if one or more chip enables are inactive.

PIN DESCRIPTIONS (continued)

TQFP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
14, 16, 31, 38, 39, 42, 43, 49, 50, 64, 66, 88	NC	-	No Connect: These signals are not internally connected.
52, 53, 56, 57, 58, 59, 62, 63 68, 69, 72, 73, 74, 75, 78, 79, 2, 3, 6, 7, 8, 9, 12, 13 18, 19, 22, 23, 24, 25, 28, 29	DQ1-DQ32	Input/ Output	SRAM Data I/O: Byte 1 is DQ1-DQ8; Byte 2 is DQ9-DQ16; Byte 3 is DQ17-DQ24; Byte 4 is DQ25-DQ32. Input data must meet setup and hold times around the rising edge of CLK.
51, 80, 1, 30	DQP1-DQP4	Input/ Output	Parity Data I/O: Byte 1 Parity is DQP1; Byte 2 Parity is DQP2; Byte 3 Parity is DQP3; Byte 4 Parity is DQP4.
87	PDIS	Input	Parity Disable: When HIGH, this input disables DQP1 through DQP4 for 32-bit data bus width. A LOW on PDIS enables control of DQP1 through DQP4 in the same manner as DQ1-DQ32 are controlled.
15, 41, 65, 91	Vcc	Supply	Power Supply: +3.3V ±5%
17, 40, 67, 90	Vss	Supply	Ground: GND
4, 11, 20, 27, 54, 61, 70, 77	VccQ	Supply	Isolated Output Buffer Supply: +3.3V ±5%
5, 10, 21, 26, 55, 60, 71, 76	VssQ	Supply	Isolated Output Buffer Ground: GND

PASS-THROUGH TRUTH TABLE

PREVIOUS CYCLE		PRESENT CYCLE				NEXT CYCLE
OPERATION	$\overline{BWs}$	OPERATION	$\overline{CE}$	$\overline{BWs}$	$\overline{OE}$	OPERATION
Initiate WRITE cycle, all bytes Address = A(n-1); data = D(n-1)	All L	Initiate READ cycle Register A(n), Q = D(n-1)	L	H	L	Read D(n)
Initiate WRITE cycle, all bytes Address = A(n-1); data = D(n-1)	All L	No new cycle Q = D(n-1)	H	H	L	No carryover from previous cycle
Initiate WRITE cycle, all bytes Address = A(n-1); data = D(n-1)	All L	No new cycle Q = HIGH-Z	H	H	H	No carryover from previous cycle
Initiate WRITE cycle, one byte Address = A(n-1); data = D(n-1)	One L	No new cycle Q = D(n-1) for one byte	H	H	L	No carryover from previous cycle

NOTE: Previous cycle may be either BURST or NONBURST cycle.

BURST ADDRESS TABLE

First Address	Second Address	Third Address	Fourth Address
X...X00	X...X01	X...X10	X...X11
X...X01	X...X10	X...X11	X...X00
X...X10	X...X11	X...X00	X...X01
X...X11	X...X00	X...X01	X...X10

NOTE: The burst sequence wraps around to its initial state upon completion.

TRUTH TABLE

OPERATION	ADDRESS USED	$\overline{CE}$	$\overline{CE2}$	CE2	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Deselected Cycle, Power-down	None	H	X	X	X	L	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	None	L	X	L	L	X	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	None	L	H	X	L	X	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	None	L	X	L	H	L	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	None	L	H	X	H	L	X	X	X	L-H	High-Z
READ Cycle, Begin Burst	External	L	L	H	L	X	X	X	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	L	X	X	X	H	L-H	High-Z
WRITE Cycle, Begin Burst	External	L	L	H	H	L	X	L	X	L-H	D
READ Cycle, Begin Burst	External	L	L	H	H	L	X	H	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	H	L	X	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	X	X	X	H	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	X	X	X	H	H	L	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	H	X	X	X	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	H	X	X	X	H	L	H	H	L-H	High-Z
WRITE Cycle, Continue Burst	Next	X	X	X	H	H	L	L	X	L-H	D
WRITE Cycle, Continue Burst	Next	H	X	X	X	H	L	L	X	L-H	D
READ Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	H	L-H	High-Z
READ Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	H	L-H	High-Z
WRITE Cycle, Suspend Burst	Current	X	X	X	H	H	H	L	X	L-H	D
WRITE Cycle, Suspend Burst	Current	H	X	X	X	H	H	L	X	L-H	D

NOTE:
1. X means "don't care." H means logic HIGH. L means logic LOW. $\overline{WRITE}$=L means any one or more byte write enable signals ($\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$ or $\overline{BW4}$) are LOW. $\overline{WRITE}$=H means all byte write enable signals are HIGH.
2. $\overline{BW1}$ enables writes to Byte 1 (DQ1-DQ8, DQP1). $\overline{BW2}$ enables writes to Byte 2 (DQ9-DQ16, DQP2). $\overline{BW3}$ enables writes to Byte 3 (DQ17-DQ24, DQP3). $\overline{BW4}$ enables writes to Byte 4 (DQ25-DQ32, DQP4).
3. All inputs except $\overline{OE}$ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
4. Wait states are inserted by suspending burst.
5. For a write operation following a read operation, $\overline{OE}$ must be HIGH before the input data required setup time and held HIGH throughout the input data hold time.
6. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
7. PDIS disables the DQP lines when HIGH and enables the DQP lines when LOW.
8. $\overline{ADSP}$ LOW always initiates an internal READ at the L-H edge of CLK. A WRITE is performed by setting one or more byte write enable signals LOW for the subsequent L-H edge of CLK. Refer to WRITE timing diagram for clarification.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .....-0.5V to +4.6V
VIN .....-0.5V to +6V
Storage Temperature (plastic) .....-55°C to +150°C
Junction Temperature .....+150°C
Power Dissipation 1.6W
Short Circuit Output Current 100mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; T_C ≤ 110°C; Vcc = 3.3V ±5% unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		VIH	2.0	5.5	V	1, 2
Input Low (Logic 0) Voltage		VIL	-0.3	0.8	V	1, 2
Input Leakage Current	0V ≤ VIN ≤ Vcc	ILI	-1	1	µA	
Output Leakage Current	Output(s) disabled, 0V ≤ VOUT ≤ Vcc	ILO	-1	1	µA	
Output High Voltage	IOH = -4.0mA	VOH	2.4		V	1
Output Low Voltage	IOL = 8.0mA	VOL		0.4	V	1
Supply Voltage		Vcc	3.1	3.5	V	1

				MAX					
DESCRIPTION	CONDITIONS	SYMBOL	TYPICAL	-7	-10	-12	-15	UNITS	NOTES
Power Supply Current: Operating	Device selected; all inputs ≤ VIL OR ≥ VIH; cycle time ≥ tKC min; Vcc = MAX; outputs open	ICC	200	225	250	225	200	mA	3, 12 13
Power Supply Current: Idle	Device selected; $\overline{ADSC}$, $\overline{ADSP}$, $\overline{ADV}$ ≥ VIH; all inputs ≤ VIL OR ≥ VIH; Vcc = MAX; cycle time ≥ tKC min	ISB1	50	85	70	60	55	mA	12, 13
CMOS Standby	Device deselected; Vcc = MAX; all inputs ≤ Vss +0.2 or ≥ Vcc -0.2; all inputs static; CLK frequency = 0	ISB2	0.2	2	2	2	2	mA	12, 13
TTL Standby	Device deselected; all inputs ≤ VIL OR ≥ VIH; all inputs static; Vcc = MAX; CLK frequency = 0	ISB3	10	18	18	18	18	mA	12, 13
Clock Running	Device deselected; all inputs ≤ VIL OR ≥ VIH; Vcc = MAX; CLK cycle time ≥ tKC min	ISB4	20	35	30	25	20	mA	12, 13

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	CI	3	4	pF	4
Input/Output Capacitance (DQ)	Vcc = 3.3V	CO	5	6	pF	4

THERMAL CONSIDERATIONS

DESCRIPTION	CONDITIONS	SYMBOL	TYP	UNITS	NOTES
Thermal resistance - Junction to Ambient	Still Air	θ_{JA}	65	°C/W	
Thermal resistance - Junction to Case		θ_{JC}	6	°C/W	
Maximum Case Temperature		TC	110	°C	11

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ±5%)

		-7		-10		-12		-15			
DESCRIPTION	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Clock											
Clock cycle time	tKC	15		20		25		30		ns	
Clock HIGH time	tKH	5		7		9		11		ns	
Clock LOW time	tKL	5		7		9		11		ns	
Output Times											
Clock to output valid	tKQ		7		10		12		15	ns	
Clock to output invalid	tKQX	3		3		3		3		ns	
Clock to output in Low-Z	tKQLZ	2		2		2		2		ns	6, 7
Clock to output in High-Z	tKQHZ		5		6		6		6	ns	6, 7
$\overline{OE}$ to output valid	tOEQ		5		6		7		8	ns	9
$\overline{OE}$ to output in Low-Z	tOELZ	0		0		0		0		ns	6, 7
$\overline{OE}$ to output in High-Z	tOEHZ		5		6		6		6	ns	6, 7
Setup Times											
Address	tAS	2.5		3		3		3		ns	8, 10
Address Status ($\overline{ADSC}$, $\overline{ADSP}$)	tADSS	2.5		3		3		3		ns	8, 10
Address Advance ($\overline{ADV}$)	tAAS	2.5		3		3		3		ns	8, 10
Byte Write Enables ($\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, $\overline{BW4}$)	tWS	2.5		3		3		3		ns	8, 10
Data-in	tDS	2.5		3		3		3		ns	8, 10
Chip Enables ($\overline{CE}$, $\overline{CE2}$, CE2)	tCES	2.5		3		3		3		ns	8, 10
Hold Times											
Address	tAH	0.5		0.5		0.5		0.5		ns	8, 10
Address Status ($\overline{ADSC}$, $\overline{ADSP}$)	tADSH	0.5		0.5		0.5		0.5		ns	8, 10
Address Advance ($\overline{ADV}$)	tAAH	0.5		0.5		0.5		0.5		ns	8, 10
Byte Write Enables ($\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, $\overline{BW4}$)	tWH	0.5		0.5		0.5		0.5		ns	8, 10
Data-in	tDH	0.5		0.5		0.5		0.5		ns	8, 10
Chip Enables ($\overline{CE}$, $\overline{CE2}$, CE2)	tCEH	0.5		0.5		0.5		0.5		ns	8, 10

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	1.5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

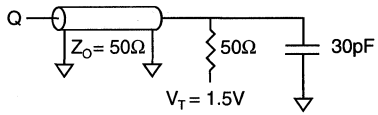


Fig. 1 OUTPUT LOAD EQUIVALENT

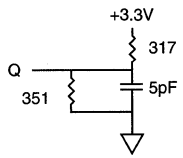
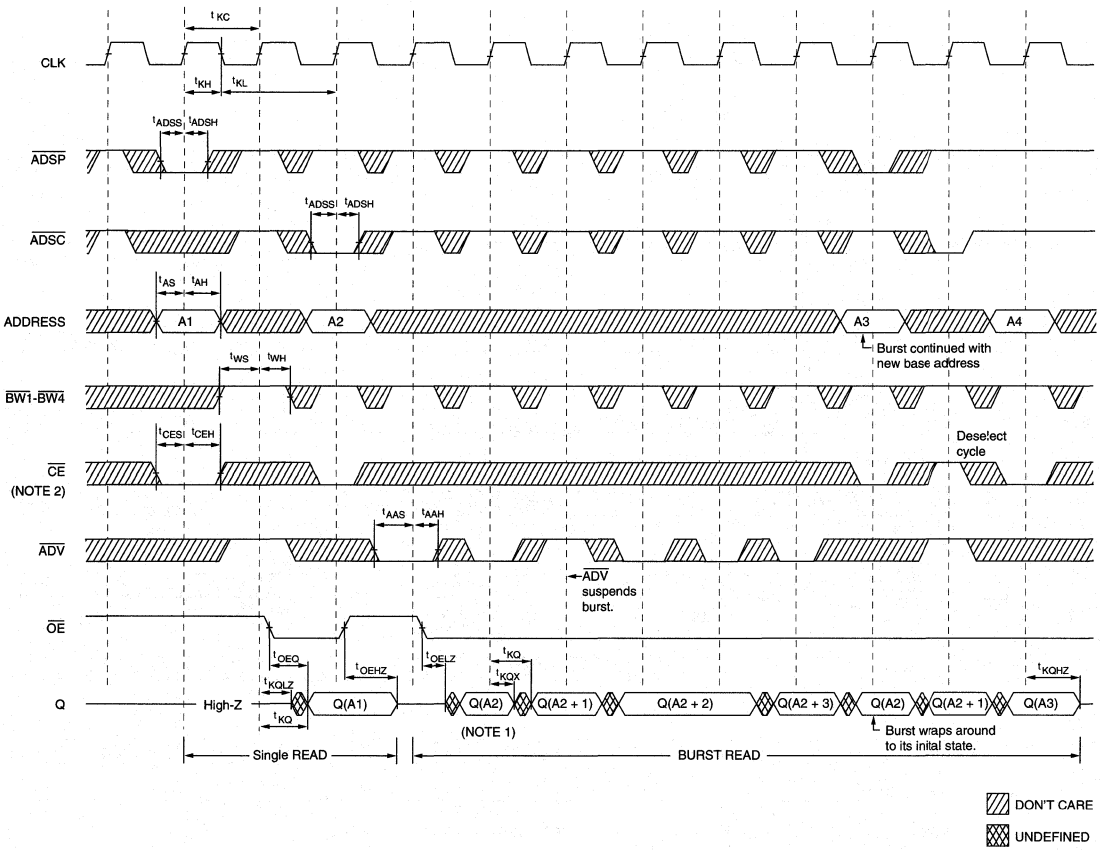


Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

1. All voltages referenced to Vss (GND).
2. Overshoot: $V_{IH} \leq +6.0V$ for $t \leq {}^tKC/2$.
   Undershoot: $V_{IL} \geq -2.0V$ for $t \leq {}^tKC/2$.
   Power-up: $V_{IH} \leq +6.0V$ and $Vcc \leq 3.1V$ for $t \leq 200msec$.
3. Icc is given with no output current. Icc increases with greater output loading and faster cycle times.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. Output loading is specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ${}^tKQHZ$ is less than ${}^tKQLZ$ and ${}^tOEHZ$ is less than ${}^tOELZ$.
8. A READ cycle is defined by byte write enables all HIGH or $\overline{ADSP}$ LOW for the required setup and hold times. A WRITE cycle is defined by at least one byte write enable LOW and $\overline{ADSP}$ HIGH for the required setup and hold times.
9. $\overline{OE}$ is a "don't care" when a byte write enable is sampled LOW.
10. This is a synchronous device. All addresses must meet the specified setup and hold times for all rising edges of CLK when either $\overline{ADSP}$ or $\overline{ADSC}$ is LOW and chip enabled. All other synchronous inputs must meet the setup and hold times with stable logic levels for all rising edges of clock (CLK) when chip is enabled. Chip enable must be valid at each rising edge of CLK (when either $\overline{ADSP}$ or $\overline{ADSC}$ is LOW) to remain enabled.
11. Micron does not warrant the functionality or reliability of any product in which the case temperature exceeds 110°C. Care should be taken to limit case temperature to acceptable levels.
12. "Device Deselected" means device is in POWER-DOWN mode as defined in the truth table. "Device Selected" means device is active (not in POWER-DOWN mode).
13. Typical values are measured at 3.3V, 25°C and 20ns cycle time.

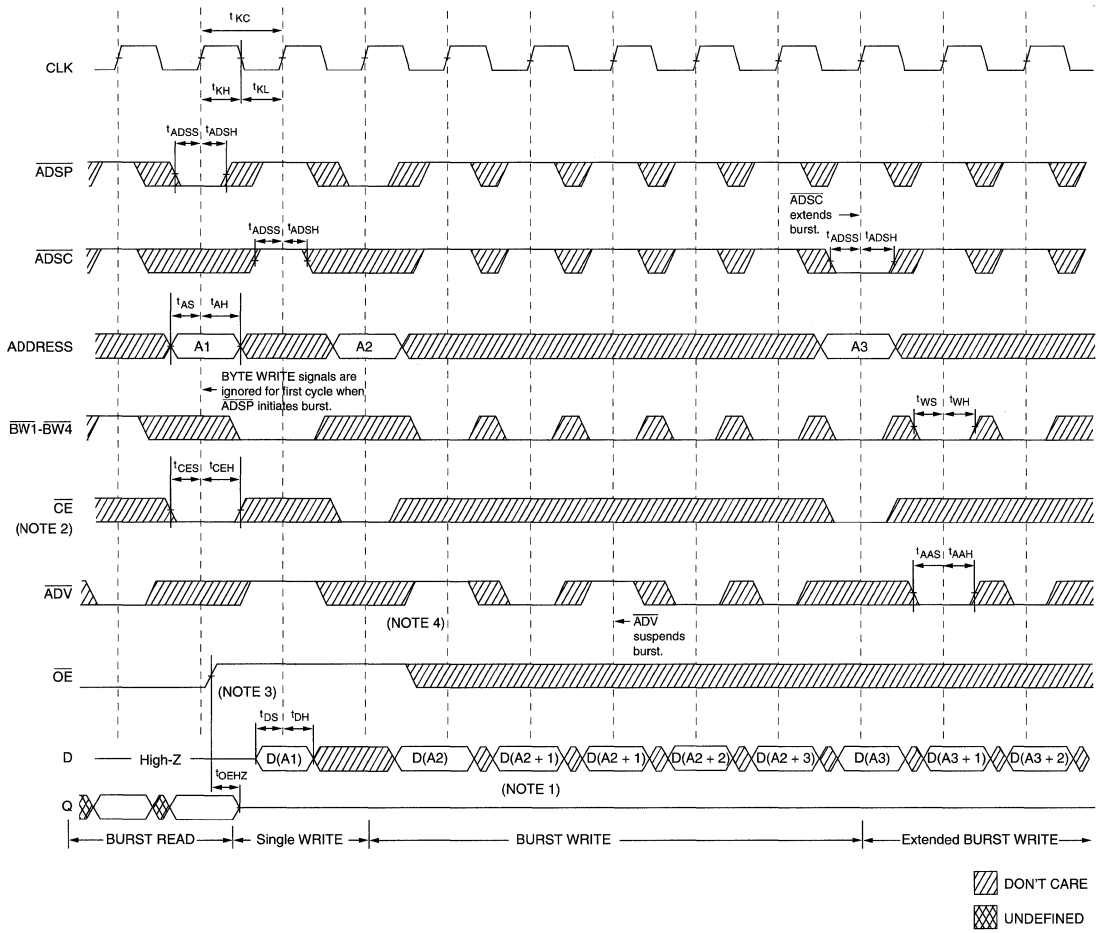
READ TIMING



NOTE:
1. Q(A2) refers to output from address A2. Q(A2+1) refers to output from the next internal burst address following A2.
2. $\overline{CE2}$ and CE2 have timing identical to $\overline{CE}$. On this diagram, when $\overline{CE}$ is LOW, $\overline{CE2}$ is LOW and CE2 is HIGH. When $\overline{CE}$ is HIGH, $\overline{CE2}$ is HIGH and CE2 is LOW.

NEW 3.3 VOLT SYNCHRONOUS SRAM

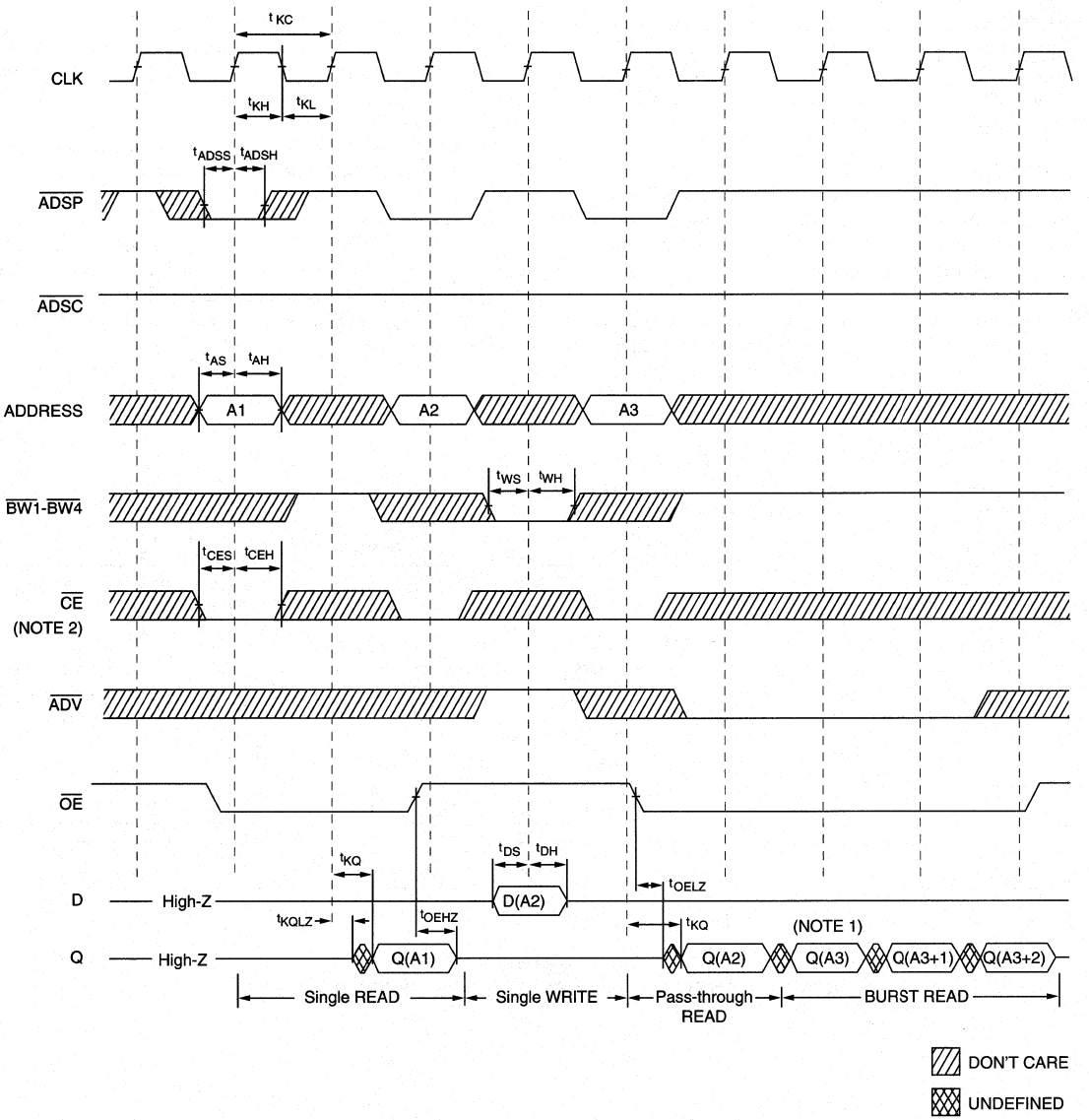
WRITE TIMING



NOTE:

1. Q(A2) refers to output from address A2. Q(A2+1) refers to output from the next internal burst address following A2.
2. $\overline{CE2}$ and CE2 have timing identical to $\overline{CE}$. On this diagram, when $\overline{CE}$ is LOW, $\overline{CE2}$ is LOW and CE2 is HIGH. When $\overline{CE}$ is HIGH, $\overline{CE2}$ is HIGH and CE2 is LOW.
3. $\overline{OE}$ must be HIGH before the input data setup and held HIGH throughout the the data hold time. This prevents input/output data contention for the time period prior to the byte write enable inputs being sampled.
4. $\overline{ADV}$ must be HIGH to permit a WRITE to the loaded address.

READ/WRITE TIMING



NOTE:
1. Q(A3) refers to output from address A3. Q(A3+1) refers to output from the next internal burst address following A3.
2. $\overline{CE2}$ and CE2 have timing identical to $\overline{CE}$. On this diagram, when $\overline{CE}$ is LOW, $\overline{CE2}$ is LOW and CE2 is HIGH. When $\overline{CE}$ is HIGH, $\overline{CE2}$ is HIGH and CE2 is LOW.

APPLICATION INFORMATION

32-BIT-WIDE SYSTEMS

The Micron 32K x 36 Synchronous SRAM may be used in a 32-bit-wide system without the use of any external components by connecting PDIS to Vcc. This disables the output buffer on the data parity input/output lines (DQP1, DQP2, DQP3 and DQP4).

LOAD DERATING CURVES

The Micron 32K x 36 Synchronous SRAM timing is dependent upon the capacitive loading on the outputs. The data sheet is written assuming a load of 30pF. Access time changes with load capacitance as follows:

$\Delta^tKQ = 0.016$ ns/pF x ΔC_L pF. (Note: this is preliminary information subject to change.)

For example, if the SRAM loading is 22pF, ΔC_L is -8p (8pF less than rated load). The clock to valid output time o the SRAM is reduced by 0.016 x 8 = 0.128ns. If the device i a 7ns part, the worse case ^tKQ becomes 6.87n (approximately).

Consult the factory for copies of I/O current versu voltage curves and Quad Design models.

DEPTH EXPANSION

The Micron 32K x 36 Synchronous SRAM incorporate two additional chip enables to facilitate simple deptl expansion. This permits easy cache upgrades from 32I depth to 64K depth with no extra logic as shown i Figure 3.

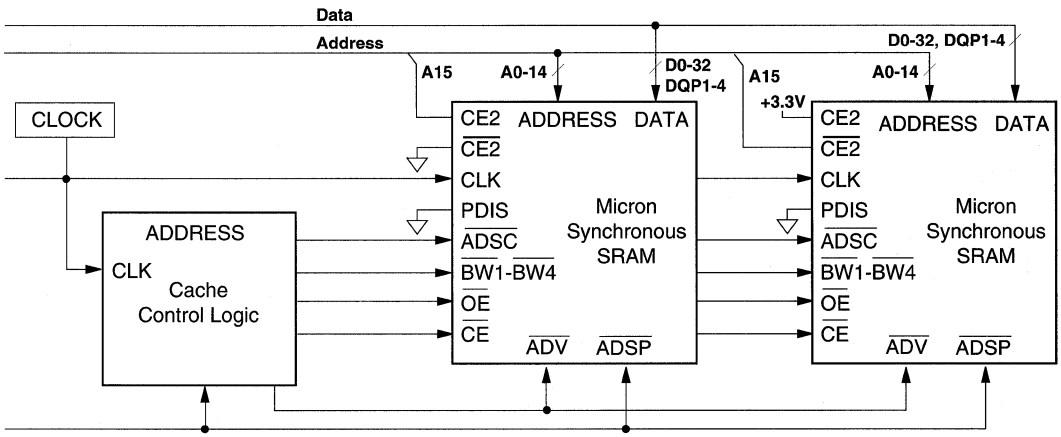


Figure 3
DEPTH EXPANSION FROM 32K x 36 TO 64K x 36

APPLICATION EXAMPLES

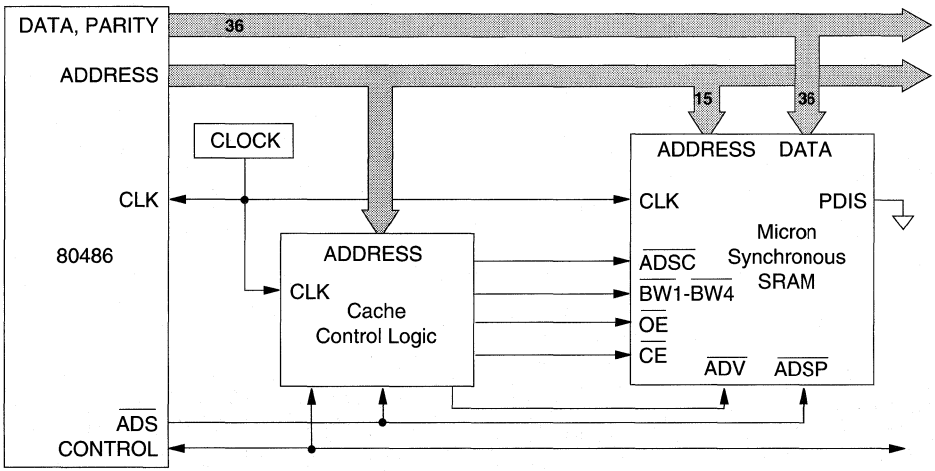


Figure 4
128K BYTE SECONDARY CACHE WITH PARITY AND BURST FOR 50 MHz 80486 OR 680X0 USING ONE MT58LC32K36A6LG-10 SYNCHRONOUS SRAM

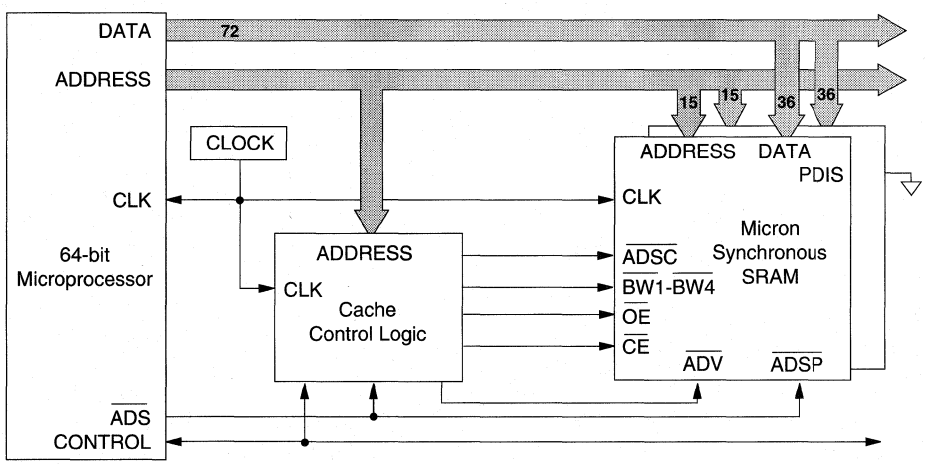


Figure 5
256K BYTE SECONDARY CACHE WITH PARITY AND BURST FOR 66 MHz MICROPROCESSOR USING TWO MT58LC32K36A6LG-7 SYNCHRONOUS SRAMs

MICRON SEMICONDUCTOR, INC.

MT58LC32K36A6
32K x 36 SYNCHRONOUS SRAM

MICRON
SEMICONDUCTOR, INC.

MICRON SEMICONDUCTOR, INC.

SRAM MODULE PRODUCT SELECTION GUIDE

Memory Configuration	Optional Access Cycle	Part Number	Access Time (ns)	Package and No. of Pins		Page
				ZIP	SIMM	
16K x 32	$\overline{CE}$ and $\overline{OE}$	MT8S1632	10*, 12, 15, 20, 25	64	64	4-1
64K x 32	$\overline{CE}$ and $\overline{OE}$	MT8S6432	12*, 15, 20, 25, 30, 35	64	64	4-9
64K x 32	$\overline{CE}$ and $\overline{OE}$	MT8LS6432	17, 20, 25, 35	64	64	4-17
128K x 32	$\overline{CE}$ and $\overline{OE}$	MT4S12832	15*, 20, 25, 35	64	64	4-25
128K x 32	$\overline{CE}$ and $\overline{OE}$	MT4LS12832	17, 20, 25, 35	64	64	4-33
256K x 32	$\overline{CE}$ and $\overline{OE}$	MT8S25632	15*, 20, 25, 35	64	64	4-41
256K x 32	$\overline{CE}$ and $\overline{OE}$	MT8LS25632	17, 20, 25, 35	64	64	4-49

*Preliminary

SRAM MODULE

16K x 32 SRAM

FEATURES

- High speed: 10*, 15, 20, 25 and 35ns
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ functions
- Low profile
- All inputs and outputs are TTL-compatible
- Industry-standard pinout
- Upgradable with 64K x 32, 128K x 32 and 256K x 32 modules

OPTIONS MARKING

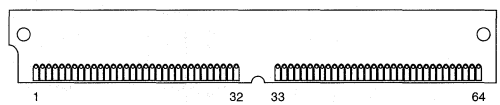
- Timing
  - 10ns access -10*
  - 12ns access -12
  - 15ns access -15
  - 20ns access -20
  - 25ns access -25
- Packages
  - 64-pin SIMM M
  - 64-pin ZIP Z
- 2V data retention L
- Part Number Example: MT8S1632M-10 L

*Consult factory

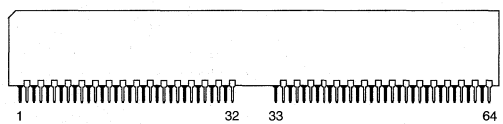
NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

64-Pin SIMM
(SF-1)



64-Pin ZIP
(SG-2)



PIN #	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	Vss	17	A2	33	$\overline{CE4}$	49	A4
2	PD0	18	A9	34	$\overline{CE3}$	50	A11
3	PD1	19	DQ13	35	NC	51	A5
4	DQ1	20	DQ5	36	NC	52	A12
5	DQ9	21	DQ14	37	$\overline{OE}$	53	Vcc
6	DQ2	22	DQ6	38	Vss	54	A13
7	DQ10	23	DQ15	39	DQ25	55	A6
8	DQ3	24	DQ7	40	DQ17	56	DQ21
9	DQ11	25	DQ16	41	DQ26	57	DQ29
10	DQ4	26	DQ8	42	DQ18	58	DQ22
11	DQ12	27	Vss	43	DQ27	59	DQ30
12	Vcc	28	$\overline{WE}$	44	DQ19	60	DQ23
13	A0	29	NC	45	DQ28	61	DQ31
14	A7	30	NC	46	DQ20	62	DQ24
15	A1	31	$\overline{CE2}$	47	A3	63	DQ32
16	A8	32	$\overline{CE1}$	48	A10	64	Vss

GENERAL DESCRIPTION

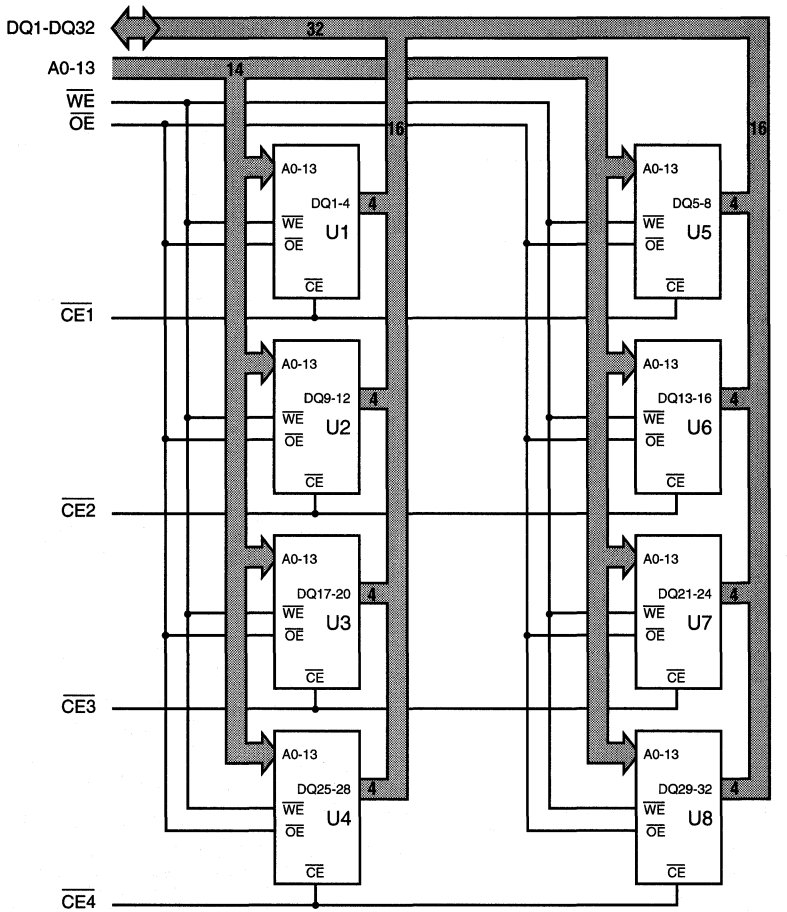
The MT8S1632 is a high-speed SRAM memory module containing 16,384 words organized in a x32-bit configuration. The module consists of eight 16K x 4 fast SRAMs mounted on a 64-pin, double-sided, FR4-printed circuit board.

Data is written into to the SRAM memory when write enable ($\overline{WE}$) and chip enable ($\overline{CE}$) inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ and output enable ($\overline{OE}$) are LOW. $\overline{CE}$ can set the output in High-Z for additional flexibility in system design, and memory expansion is accomplished by use of the $\overline{OE}$ and $\overline{CE}$ functions.

PD0 and PD1 identify the module's density, allowing interchangeable use of alternate density, industry-standard modules. Four chip enable inputs, ($\overline{CE1}$, $\overline{CE2}$, $\overline{CE3}$ and $\overline{CE4}$), are used to enable the module's 4 bytes independently.

The Micron SRAM family uses a high-speed, low-power CMOS design in a four-transistor memory cell featuring double-layer metal, double-layer polysilicon technology. All module components may be powered from a single +5V supply and all inputs and outputs are fully TTL-compatible. The "L" option offers reduced-voltage operation for systems with low standby power requirements.

FUNCTIONAL BLOCK DIAGRAM



PRESENCE DETECT
PD0 = Vss
PD1 = No Connect

U1-U8 = MT5C6405DJ

TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Storage Temperature ..... -55°C to +125°C
Power Dissipation 8W
Short Circuit Output Current 50mA
Voltage on Any Pin Relative to V_{SS} ..... -1V to V_{CC} +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	Vcc+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-40	40	µA	
Output Leakage Current	Output(s) disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

				MAX						
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-10*	-12	-15	-20	-25	UNITS	NOTES
Operating Current: TTL Input Levels	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	520	1,520	1,480	1,460	1,320	1,120	mA	3, 13
Standby Current: TTL Input Levels	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	160	480	400	360	320	280	mA	13
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	3.2	24	24	24	24	24	mA	13

*Consult factory

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A13, $\overline{WE}$, $\overline{OE}$	T_A = 25°C; f = 1 MHz	C_I	60	pF	4
Input Capacitance: $\overline{CE}$1-$\overline{CE}$4	V_{CC} = 5V	C12	15	pF	4
Input/Output Capacitance: DQ1-DQ32		$C_{I/O}$	10	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

		-10*		-12		-15		-20		-25			
DESCRIPTION	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ Cycle													
READ cycle time	tRC	10		12		15		20		25		ns	
Address access time	tAA		10		12		15		20		25	ns	
Chip Enable access time	tACE		9		10		12		15		20	ns	
Output hold from address change	tOH	3		3		3		3		3		ns	
Chip Enable to output in Low-Z	tLZCE†	2		2		2		2		2		ns	7, 14
Chip Enable to output in High-Z	tHZCE		5		6		7		8		8	ns	6, 7
Chip disable to power-up time	tPU	0		0		0		0		0		ns	
Chip Enable to power-down time	tPD		10		12		15		20		25	ns	
Output Enable access time	tAOE		5		6		7		8		8	ns	
Output disable to output in Low-Z	tLZOE	0		0		0		0		0		ns	
Output Enable to output in High-Z	tHZOE		5		6		6		7		8	ns	6
WRITE Cycle													
WRITE cycle time	tWC	10		12		15		20		25		ns	
Chip Enable to end of write	tCW	8		10		12		15		20		ns	
Address valid to end of write	tAW	8		10		12		15		20		ns	
Address setup time	tAS	0		0		0		0		0		ns	
Address hold from end of write	tAH	0		0		0		0		0		ns	
WRITE pulse width	tWP1	7		8		10		12		15		ns	
WRITE pulse width	tWP2	9		10		14		18		20		ns	
Data setup time	tDS	6		7		8		9		10		ns	
Data hold time	tDH	1		1		1		1		1		ns	
Write disable to output in Low-Z	tLZWE	2		2		2		2		2		ns	7
Write Enable to output in High-Z	tHZWE		5		5		6		8		8	ns	6, 7

*Consult factory

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

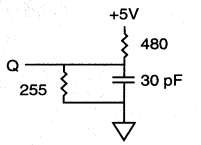


Fig. 1 OUTPUT LOAD EQUIVALENT

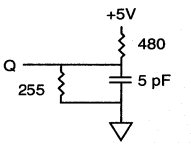


Fig. 2 OUTPUT LOAD EQUIVALENT

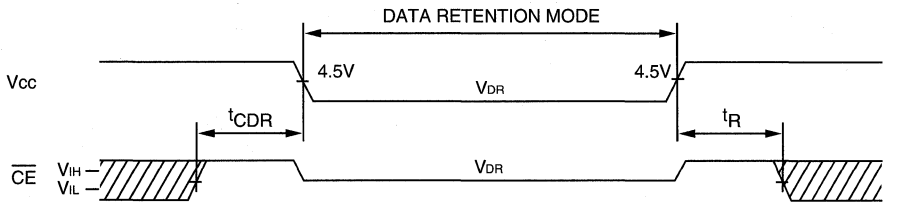
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZOE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE, and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC=Read Cycle Time
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Typical values are measured at 5V, 25°C and 20ns cycle time.
14. Typical currents are measured at 25°C.
15. Output enable ($\overline{OE}$) is inactive (HIGH).
16. Output enable ($\overline{OE}$) is active (LOW).

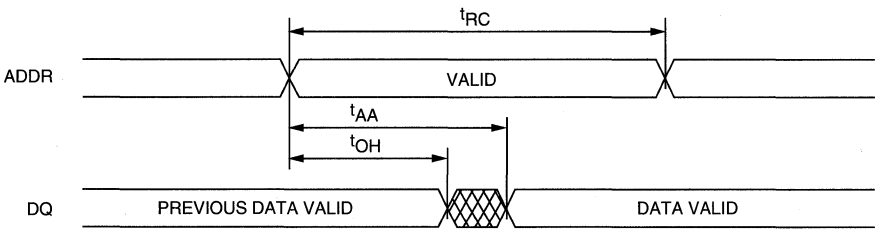
DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2			V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	ICCDR		760	2,400	µA	14
		Vcc = 3V			1,000	4,400	µA	14
Chip Deselect to Data Retention Time			^{t}CDR	0			ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4,11

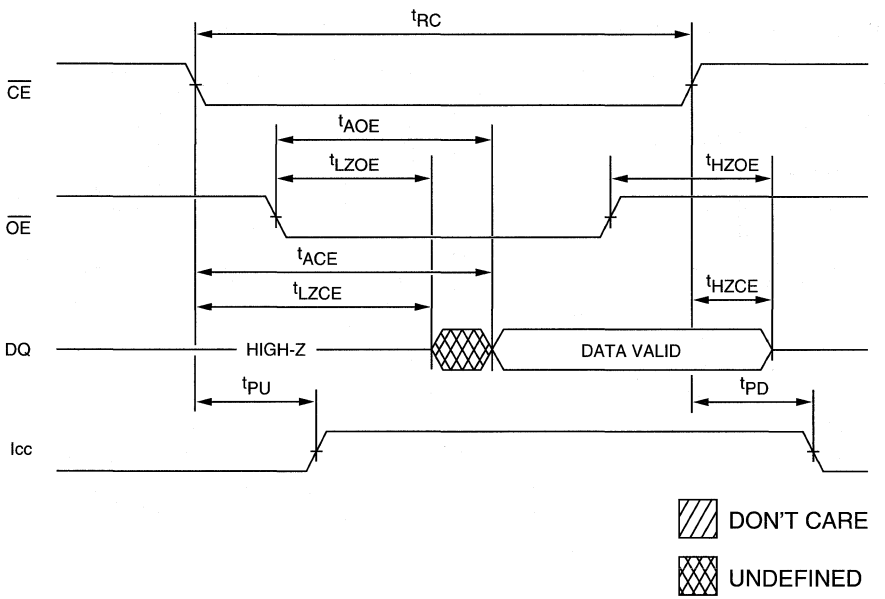
LOW Vcc DATA-RETENTION WAVEFORM



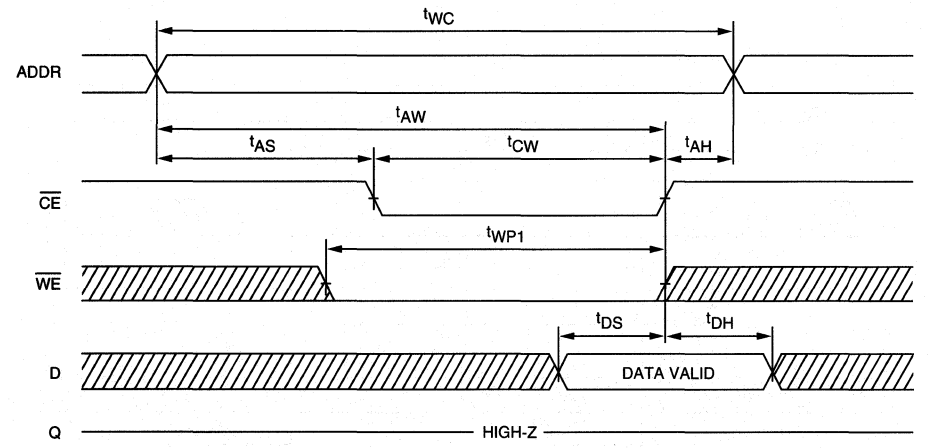
READ CYCLE NO. 1 [8, 9]



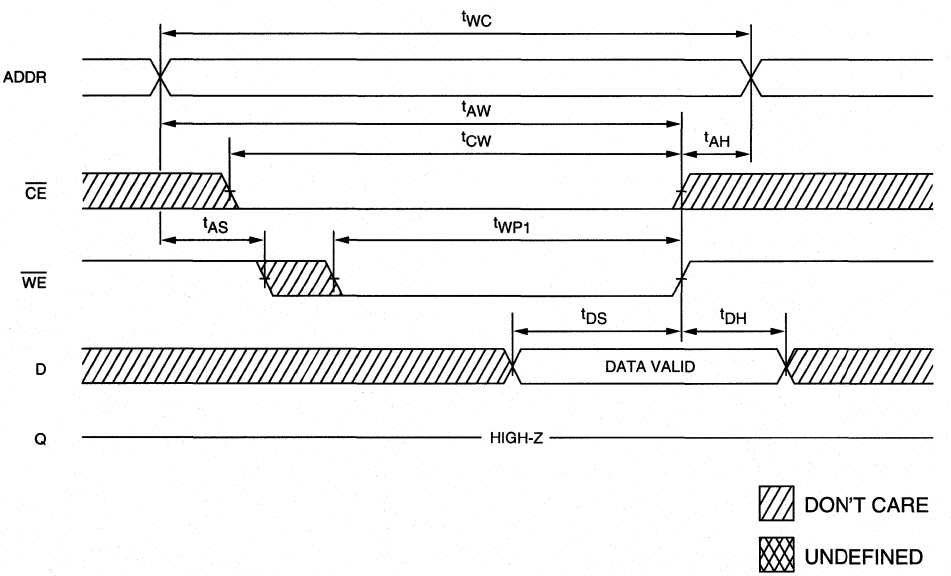
READ CYCLE NO. 2 [7, 8, 10]



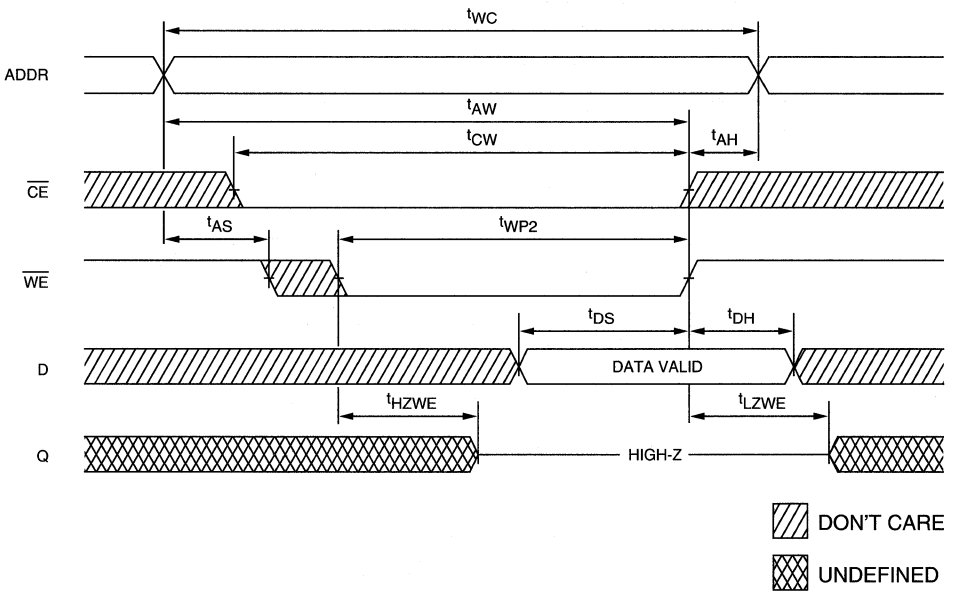
WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)



WRITE CYCLE NO. 2 [7, 12, 15]
(Write Enable Controlled)



WRITE CYCLE NO. 3 [7, 12, 16]
(Write Enable Controlled)



SRAM MODULE

64K x 32 SRAM

FEATURES

- High speed: 15*, 20, 25, 30 and 35ns
- High-performance, low-power CMOS process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ functions
- Low profile
- Industry-standard pinout
- All inputs and outputs are TTL-compatible
- Upgradable with 128K x 32 and 256K x 32 modules

OPTIONS

	MARKING
• Timing	
12ns access	-12*
15ns access	-15
20ns access	-20
25ns access	-25
35ns access	-35
• Packages	
64-pin SIMM	M
64-pin ZIP	Z
• 2V data retention	L
• Low power	P

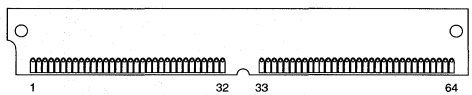
• Part Number Example: MT8S6432Z-15 P

*Consult factory

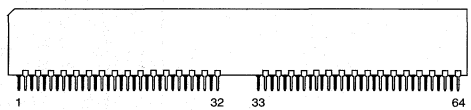
NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

64-Pin SIMM
(SF-2)



64-Pin ZIP
(SG-3)



PIN #	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	Vss	17	A2	33	$\overline{CE4}$	49	A4
2	PD0	18	A9	34	$\overline{CE3}$	50	A11
3	PD1	19	DQ13	35	NC	51	A5
4	DQ1	20	DQ5	36	NC	52	A12
5	DQ9	21	DQ14	37	$\overline{OE}$	53	Vcc
6	DQ2	22	DQ6	38	Vss	54	A13
7	DQ10	23	DQ15	39	DQ25	55	A6
8	DQ3	24	DQ7	40	DQ17	56	DQ21
9	DQ11	25	DQ16	41	DQ26	57	DQ29
10	DQ4	26	DQ8	42	DQ18	58	DQ22
11	DQ12	27	Vss	43	DQ27	59	DQ30
12	Vcc	28	$\overline{WE}$	44	DQ19	60	DQ23
13	A0	29	A15	45	DQ28	61	DQ31
14	A7	30	A14	46	DQ20	62	DQ24
15	A1	31	$\overline{CE2}$	47	A3	63	DQ32
16	A8	32	$\overline{CE1}$	48	A10	64	Vss

GENERAL DESCRIPTION

The MT8S6432 is a high-speed SRAM memory module containing 65,536 words organized in a x32-bit configuration. The module consists of eight 64K x 4 fast SRAMs mounted on a 64-pin, double-sided, FR4 printed circuit board.

Data is written into to the SRAM memory when write enable ($\overline{WE}$) and chip enable ($\overline{CE}$) inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ and output enable ($\overline{OE}$) are LOW. $\overline{CE}$ and/or $\overline{OE}$ can set the output in a High-Z state for additional flexibility in system design and memory expansion.

PD0 and PD1 identify the module's density, allowing interchangeable use of alternate density, industry-standard modules. Four chip enable inputs, ($\overline{CE1}$, $\overline{CE2}$, $\overline{CE3}$ and $\overline{CE4}$) are used to enable the module's 4 bytes independently.

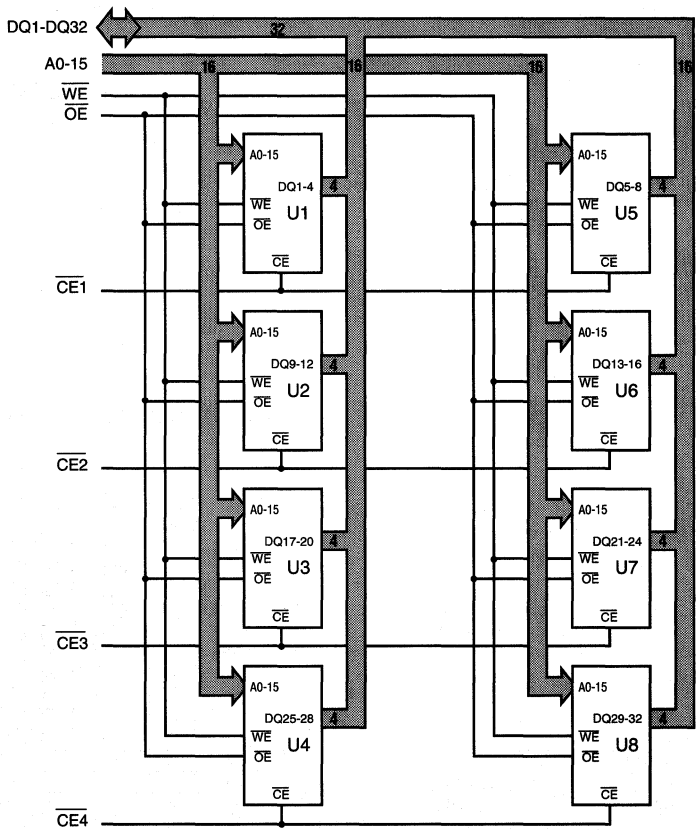
The Micron SRAM family uses a high-speed, low-power CMOS design in a four-transistor memory cell featuring double-layer metal, double-layer polysilicon technology. All module components may be powered from a single +5V DC supply and all inputs and outputs are fully TTL-compatible. The "L" option offers reduced-voltage operation for systems with low standby power requirements.

The "LP" version provides a reduction in both operating current (I_{CC}) and TTL standby current (I_{SB1}). The latter is achieved through the use of gated inputs on the $\overline{WE}$, $\overline{OE}$ and

GENERAL DESCRIPTION (continued)

address lines, which also facilitates the design of battery backed systems. That is, the gated inputs simplify the design effort and circuitry required to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

FUNCTIONAL BLOCK DIAGRAM



PRESENCE DETECT
PD0 = No Connect
PD1 = Vss

U1-U8 = MT5C2565DJ

TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Storage Temperature ..... -55°C to +125°C
Power Dissipation 8W
Short Circuit Output Current 50mA
Voltage on Any Pin Relative to V_{SS} ..... -1V to V_{CC} +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-40	40	µA	
Output Leakage Current	Output(s) disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

					MAX						
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-12	-15†	-20	-25	-35	UNITS	NOTES
Operating Current TTL Input Levels	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	824	1,520	1,360	1,200	1,040	1,000	mA	3, 13
	P Version	I_{CC}	768	-	-	1,080	1,000	920	mA	3, 13
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	192	440	400	360	320	280	mA	13
	P Version	I_{SB1}	11.2	-	-	32	32	32	mA	13
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	4.8	40	40	40	40	56	mA	13
	P Version	I_{SB2}	3.2	-	3	3	3	3	mA	13

† LP version not available with this speed grade.

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A15, $\overline{WE}$, $\overline{OE}$	T_A = 25°C; f = 1 MHz	C_I	70	pF	4
Input Capacitance: $\overline{CE}$1- $\overline{CE}$4	V_{CC} = 5V	C12	15	pF	4
Input/Output Capacitance: DQ1-DQ32		$C_{I/O}$	10	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

		-12*		-15		-20		-25		-35			
DESCRIPTION	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ Cycle													
READ cycle time	^tRC	12		15		20		25		35		ns	
Address access time	^tAA		12		15		20		25		35	ns	
Chip Enable access time	^tACE		12		15		20		25		35	ns	
Output hold from address change	^tOH	3		3		3		3		3		ns	
Chip Enable LOW to output in Low-Z	^tLZCE	3		3		3		3		3		ns	7
Chip Enable to output in High-Z	^tHZCE		6		8		9		9		15	ns	6, 7
Chip Enable LOW to power-up time	^tPU	0		0		0		0		0		ns	
Chip Enable HIGH to power-down time	^tPD		12		15		20		25		35	ns	
Output Enable access time	^tAOE		6		8		8		8		12	ns	
Output Enable LOW to output in Low-Z	^tLZOE	0		0		0		0		0		ns	
Output Enable HIGH to output in High-Z	^tHZOE		6		6		7		7		12	ns	6
WRITE Cycle													
WRITE cycle time	^tWC	12		15		20		20		30		ns	
Chip Enable to end of write	^tCW	8		10		12		15		20		ns	
Address valid to end of write	^tAW	8		10		12		15		20		ns	
Address setup time	^tAS	0		0		0		0		0		ns	
Address hold from end of write	^tAH	1		1		1		1		1		ns	
WRITE pulse width	$^tWP1$	8		10		12		15		20		ns	
WRITE pulse width	$^tWP2$	12		12		15		15		20		ns	
Data setup time	^tDS	7		7		10		10		15		ns	
Data hold time	^tDH	0		0		0		0		0		ns	
Write Enable LOW to output in Low-Z	^tLZWE	2		2		2		2		2		ns	7
Write Enable HIGH to output in High-Z	^tHZWE		6	0	7	0	8	0	10	0	12	ns	6, 7

*Consult factory

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

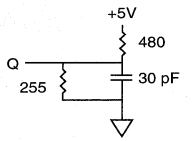


Fig. 1 OUTPUT LOAD EQUIVALENT

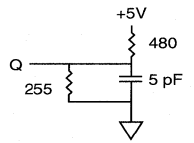


Fig. 2 OUTPUT LOAD EQUIVALENT

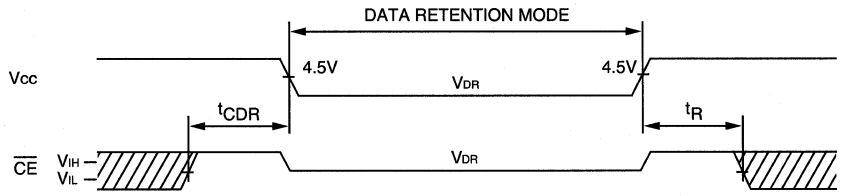
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZOE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC=Read Cycle Time
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Typical values are measured at 5V, 25°C and 20ns cycle time.
14. Typical values are measured at 25°C.
15. Output enable ($\overline{OE}$) is inactive (HIGH).
16. Output enable ($\overline{OE}$) is active (LOW).

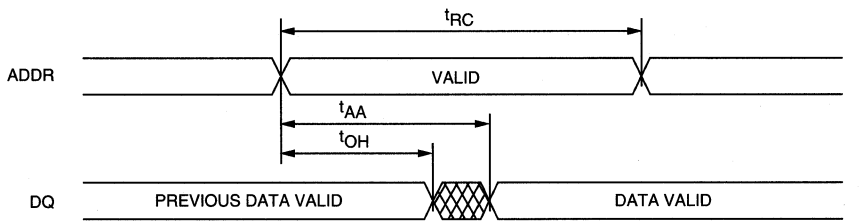
DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2			V	
Data Retention Current L Version	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	ICCDR		280	2,400	µA	14
		Vcc = 3V			720	4,000	µA	14
Data Retention Current LP Version	$\overline{CE}$ ≥ (Vcc -0.2V)	Vcc = 2V	ICCDR		280	2,400	µA	14
		Vcc = 3V	ICCDR		720	4,000	µA	14
Chip Deselect to Data Retention Time			^{t}CDR	0			ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4,11

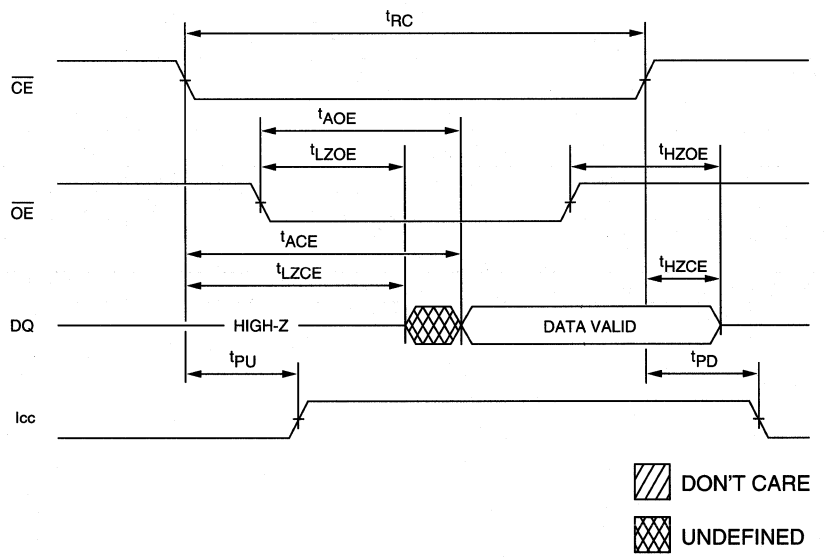
LOW Vcc DATA-RETENTION WAVEFORM



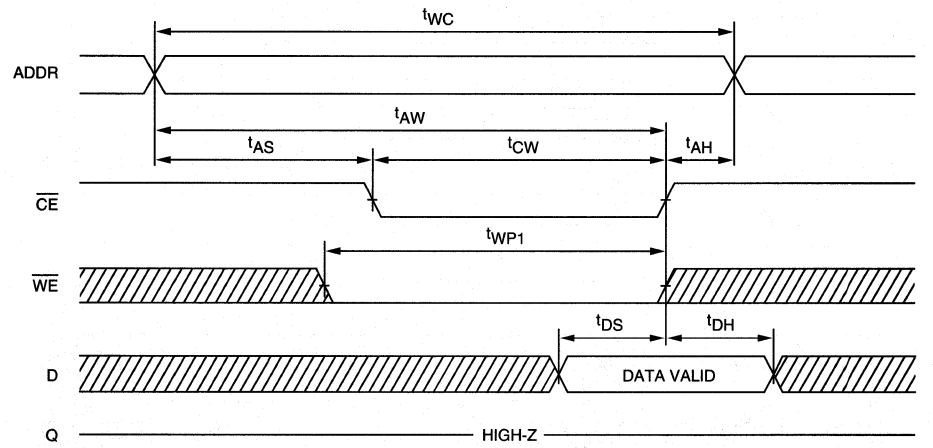
READ CYCLE NO. 1 [8, 9]



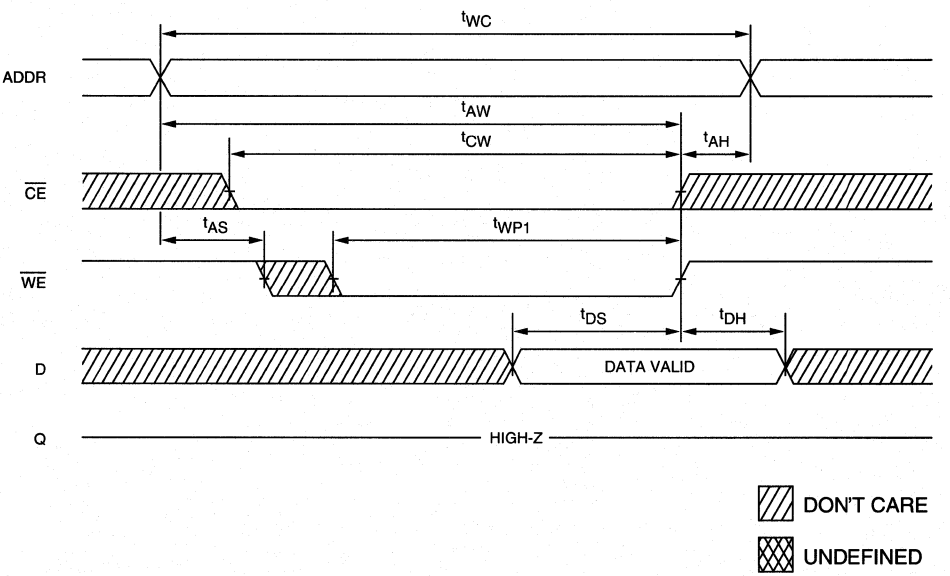
READ CYCLE NO. 2 [7, 8, 10]



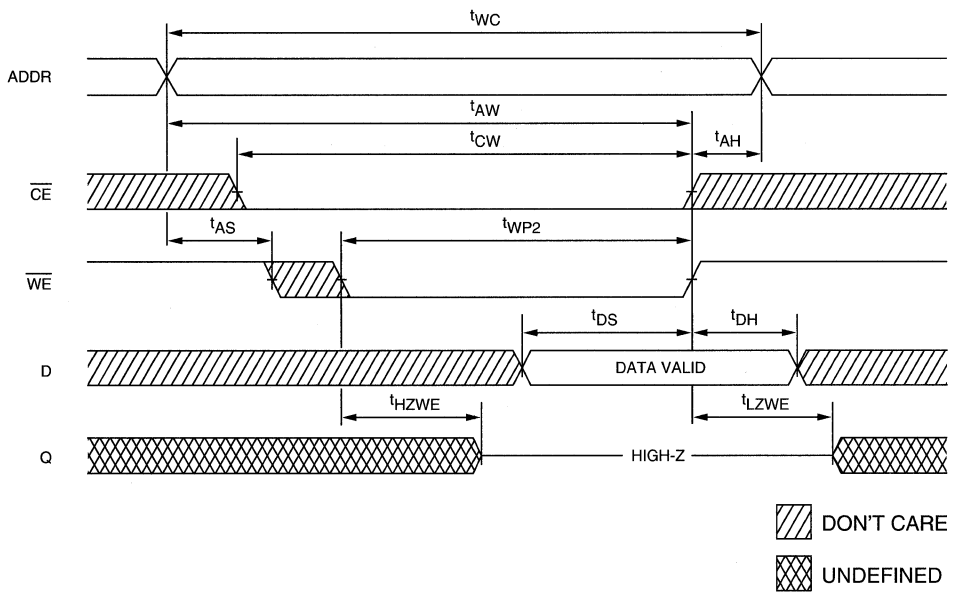
WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)



WRITE CYCLE NO. 2 [7, 12, 15]
(Write Enable Controlled)



WRITE CYCLE NO. 3 [7, 12, 16]
(Write Enable Controlled)



SRAM MODULE

64K x 32 SRAM
LOW VOLTAGE

FEATURES

- High speed: 17, 20, 25, 30 and 35ns
- High-performance, low-power CMOS process
- Single +3.3V ± 0.3V power supply
- 5V-tolerant I/O
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- Low profile
- Industry-standard pinout
- All inputs and outputs are TTL-compatible
- Upgradable with 128K x 32 and 256K x 32 modules

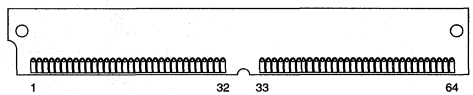
OPTIONS — MARKING

- Timing
  - 17ns access — -17
  - 20ns access — -20
  - 25ns access — -25
  - 35ns access — -35
- Packages
  - 64-pin SIMM — M
  - 64-pin ZIP — Z
- 2V data retention — L
- 2V data retention, low power — LP
- Part Number Example: MT8LS6432Z-20 LP

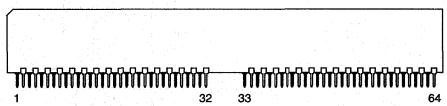
NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

64-Pin SIMM
(SF-2)



64-Pin ZIP
(SG-3)



PIN #	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	Vss	17	A2	33	$\overline{CE4}$	49	A4
2	PD0	18	A9	34	$\overline{CE3}$	50	A11
3	PD1	19	DQ13	35	NC	51	A5
4	DQ1	20	DQ5	36	NC	52	A12
5	DQ9	21	DQ14	37	$\overline{OE}$	53	Vcc
6	DQ2	22	DQ6	38	Vss	54	A13
7	DQ10	23	DQ15	39	DQ25	55	A6
8	DQ3	24	DQ7	40	DQ17	56	DQ21
9	DQ11	25	DQ16	41	DQ26	57	DQ29
10	DQ4	26	DQ8	42	DQ18	58	DQ22
11	DQ12	27	Vss	43	DQ27	59	DQ30
12	Vcc	28	$\overline{WE}$	44	DQ19	60	DQ23
13	A0	29	A15	45	DQ28	61	DQ31
14	A7	30	A14	46	DQ20	62	DQ24
15	A1	31	$\overline{CE2}$	47	A3	63	DQ32
16	A8	32	$\overline{CE1}$	48	A10	64	Vss

GENERAL DESCRIPTION

The MT8LS6432 is a high-speed SRAM memory module containing 65,536 words organized in a x32-bit configuration. The module consists of eight low voltage 64K x 4 fast SRAMs mounted on a 64-pin, double-sided, FR4 printed circuit board.

Data is written into to the SRAM memory when write enable ($\overline{WE}$) and chip enable ($\overline{CE}$) inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ and output enable ($\overline{OE}$) are LOW. $\overline{CE}$ and/or $\overline{OE}$ can set the output in a High-Z state for additional flexibility in system design and memory expansion.

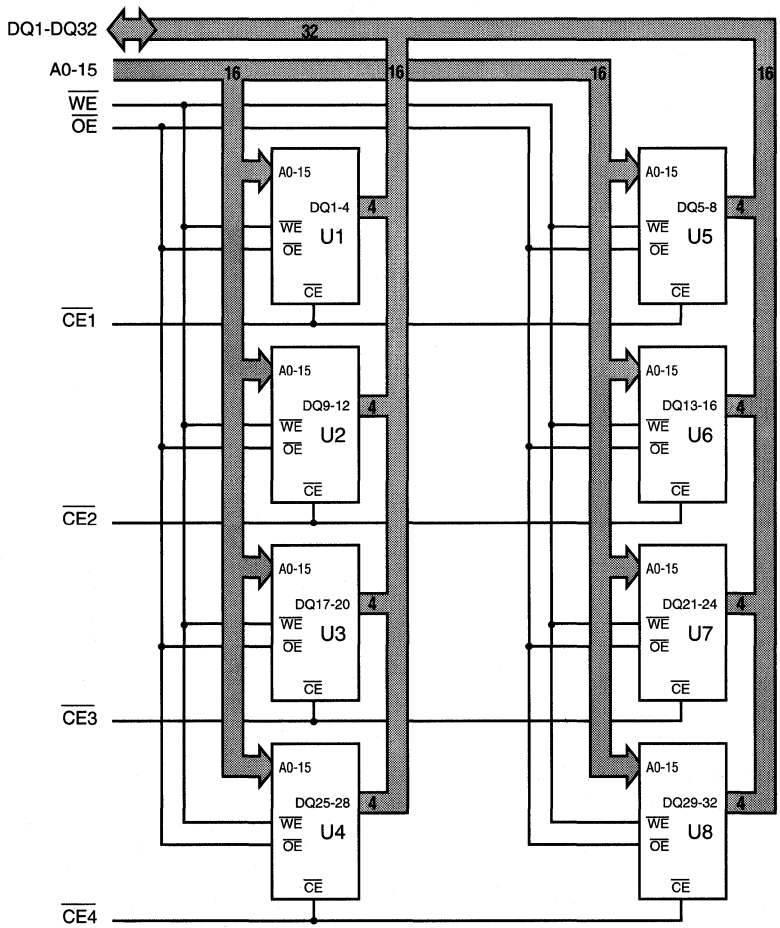
PD0 and PD1 identify the module's density, allowing interchangeable use of alternate density, industry standard modules. Four chip enable inputs, ($\overline{CE1}$, $\overline{CE2}$, $\overline{CE3}$ and $\overline{CE4}$) are used to enable the module's 4 bytes independently.

The Micron SRAM family uses a high-speed, low-power CMOS design in a four-transistor memory cell featuring double-layer metal, double-layer polysilicon technology. All module components may be powered from a single +3.3V DC supply and all inputs and outputs are fully TTL-compatible. The "L" option offers reduced-voltage operation for systems with low standby power requirements.

The "LP" version provides a reduction in both operating current (I_{CC}) and TTL standby current (I_{SB1}). The latter is achieved through the use of gated inputs on the $\overline{WE}$, $\overline{OE}$ and address lines, which also facilitates the design of battery backed systems. That is, the gated inputs simplify the design effort and circuitry required to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

NEW ■ SRAM MODULE

FUNCTIONAL BLOCK DIAGRAM



PRESENCE DETECT
PD0 = No Connect
PD1 = Vss

U1-U8 = MT5LC2565DJ

TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -0.5V to +4.6V
V_{IN} ..... -0.5V to +6.0V
Storage temperature ..... -55°C to +125°C
Power dissipation 8W
Short circuit output current 50mA
Voltage on Any Pin Relative to V_{SS} ..... -1V to V_{CC} +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ±0.3V)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.0	5.5V	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-8	8	µA	
Output Leakage Current	Output(s) disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	3.0	3.6	V	1

					MAX					
DESCRIPTION	CONDITIONS	SYMBOL	VER	TYP	-17	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX outputs open f = MAX = 1/tRC	I_{CC}	STD, L	584	880	860	760	720	mA	3, 13
			LP	312	520	500	440	400	mA	
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX outputs open f = MAX = 1/tRC	I_{SB1}	STD, L	136	240	230	200	200	mA	13
			LP	64	144	140	120	96	mA	13
	$\overline{CE}$ ≥ V_{CC} - 0.2V; V_{CC} = MAX V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ V_{SS} + 0.2V	I_{SB2}	STD, L	8	24	24	24	24	mA	13
			LP	2.4	2.25	2.25	2.25	2.25	mA	13

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A15, $\overline{WE}$, $\overline{OE}$	T_A = 25°C; f = 1 MHz V_{CC} = 3.3V	C_I	55	pF	4
Input Capacitance: $\overline{CE}$1-$\overline{CE}$4		C12	15	pF	4
Input/Output Capacitance: DQ1-DQ32		$C_{I/O}$	7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) (0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ±0.3V)

		-17		-20		-25		-35			
DESCRIPTION	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ Cycle											
READ cycle time	^tRC	17		20		25		35		ns	
Address access time	^tAA		17		20		25		35	ns	
Chip Enable access time	^tACE		17		20		25		35	ns	
Output hold from address change	^tOH	3		3		3		3		ns	
Output hold from address change	^tOH	4		4		4		4		ns	15
Chip Enable to output in Low-Z	^tLZCE	3		3		3		3		ns	
Chip Enable to output in Low-Z	^tLZCE	4		4		4		4		ns	15
Chip disable to output in High-Z	^tHZCE		9		9		10		15	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		ns	
Chip disable to power-down time	^tPD		17		20		25		35	ns	
Output Enable access time	^tAOE		8		8		8		12	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		ns	
Output disable to output in High-Z	^tHZOE		7		7		7		12	ns	6
WRITE Cycle											
WRITE cycle time	^tWC	17		20		25		35		ns	
Chip Enable to end of write	^tCW	12		15		15		20		ns	
Address valid to end of write	^tAW	12		15		15		20		ns	
Address setup time	^tAS	0		0		0		0		ns	
Address hold from end of write	^tAH	1		1		1		1		ns	
Address hold from end of write	^tAH	0		0		0		0		ns	15
WRITE pulse width	$^tWP1$	12		12		15		20		ns	
WRITE pulse width	$^tWP2$	12		15		15		20		ns	
Data setup time	^tDS	10		10		10		15		ns	
Data hold time	^tDH	0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	5		5		5		5		ns	7
Write Enable to output in High-Z	^tHZWE		10		10		10		15	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

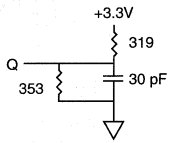


Fig. 1 OUTPUT LOAD EQUIVALENT

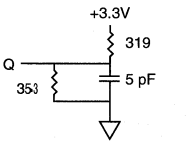


Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

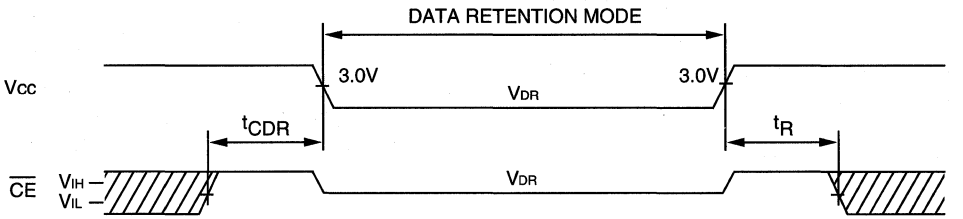
1. All voltages referenced to Vss (GND).
2. Overshoot: $V_{IH} \le +6.0$ for $t \le {}^tKC/2$
   Undershoot: $V_{IL} \ge -2.0$ for $t \le {}^tKC/2$
   Power-up: $V_{IH} \le +6.0$ and $V_{CC} \le 3.1V$ for $t \le 200msec$.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ${}^tHZCE$, ${}^tHZOE$ and ${}^tHZWE$ are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ${}^tHZCE$ is less than ${}^tLZCE$ and ${}^tHZWE$ is less than ${}^tLZWE$.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ${}^tRC$ = READ cycle time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Typical values are measured at 3.3V, 25°C and 25ns cycle time.
14. Typical currents are measured at 25°C. MAX is over operating temperature range.
15. This timing specification is only valid for P (low power) parts.

DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP versions only)

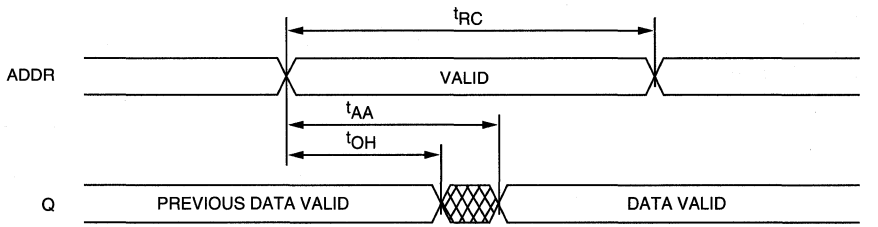
DESCRIPTION	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data		V_{DR}	2			V	
Data Retention Current L Version	$\overline{CE} \ge V_{CC}$ -0.2V Other inputs: $V_{IN} \ge V_{CC}$ -0.2V or $V_{IN} \le V_{SS}$+0.2V V_{CC} = 2V	I_{CCDR}		1,560	2,800	µA	14
Data Retention Current LP Version	$\overline{CE} \ge V_{CC}$ -0.2V V_{CC} = 2V	I_{CCDR}		1,560	2,800		
Chip Deselect to Data Retention Time		${}^tCDR$	0			ns	4
Operation Recovery Time		${}^tR$	${}^tRC$			ns	4, 11

NEW SRAM MODULE

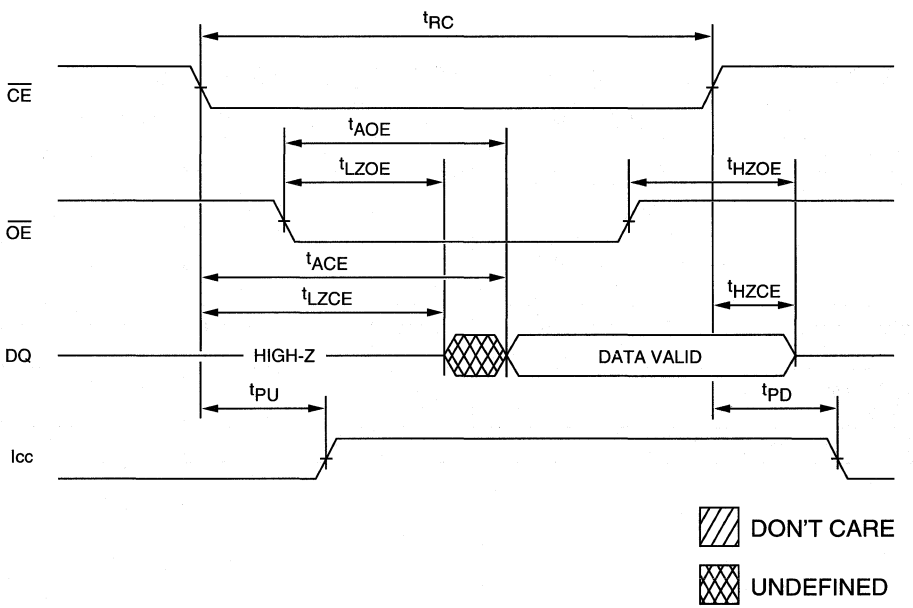
LOW Vcc DATA RETENTION WAVEFORM



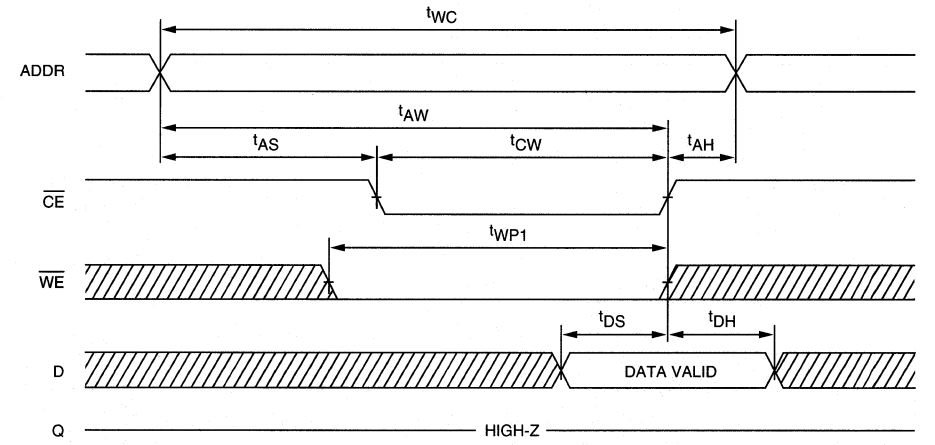
READ CYCLE NO. 1 [8, 9]



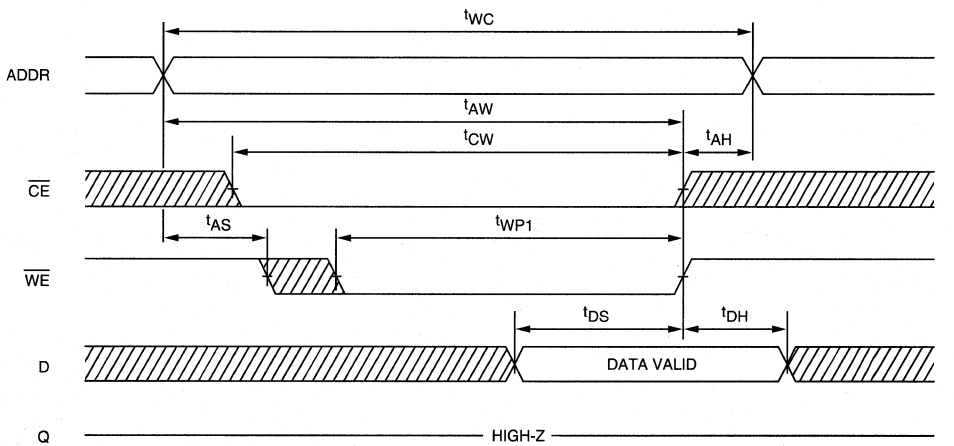
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)



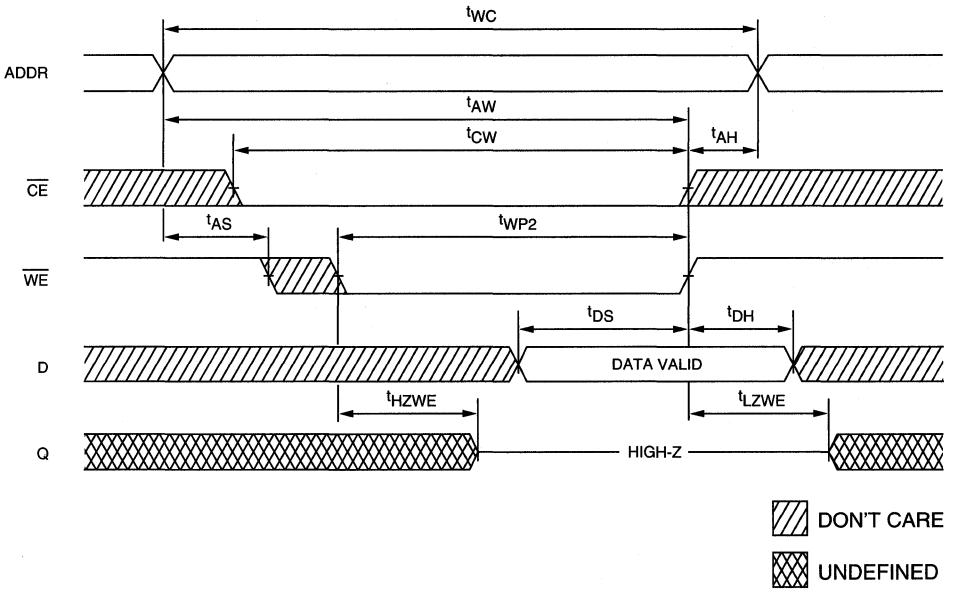
WRITE CYCLE NO. 2 [7, 12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

NEW SRAM MODULE

WRITE CYCLE NO. 3 [7, 12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is active (LOW).

SRAM MODULE

128K x 32 SRAM

FEATURES

- High speed: 15*, 20, 25 and 35ns
- High-density 512KB design
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ functions
- All inputs and outputs are TTL-compatible
- Industry standard pinout
- Low profile
- Upgradable to a 256K x 32 module

OPTIONS — MARKING

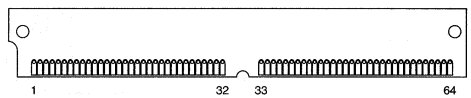
- Timing
  - 15ns access — -15*
  - 20ns access — -20
  - 25ns access — -25
  - 35ns access — -35
- Packages
  - 64-pin SIMM — M
  - 64-pin ZIP — Z
- Optional, 2V data retention — L
- 2V data retention, low power — LP
- Part Number Example: MT4S12832M-15 LP

*Consult factory

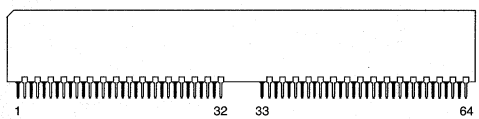
NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

64-Pin SIMM
(SF-3)



64-Pin ZIP
(SG-4)



PIN #	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	Vss	17	A2	33	$\overline{CE4}$	49	A4
2	PD0	18	A9	34	$\overline{CE3}$	50	A11
3	PD1	19	DQ13	35	NC	51	A5
4	DQ1	20	DQ5	36	A16	52	A12
5	DQ9	21	DQ14	37	$\overline{OE}$	53	Vcc
6	DQ2	22	DQ6	38	Vss	54	A13
7	DQ10	23	DQ15	39	DQ25	55	A6
8	DQ3	24	DQ7	40	DQ17	56	DQ21
9	DQ11	25	DQ16	41	DQ26	57	DQ29
10	DQ4	26	DQ8	42	DQ18	58	DQ22
11	DQ12	27	Vss	43	DQ27	59	DQ30
12	Vcc	28	$\overline{WE}$	44	DQ19	60	DQ23
13	A0	29	A15	45	DQ28	61	DQ31
14	A7	30	A14	46	DQ20	62	DQ24
15	A1	31	$\overline{CE2}$	47	A3	63	DQ32
16	A8	32	$\overline{CE1}$	48	A10	64	Vss

GENERAL DESCRIPTION

The MT4S12832 is a high-speed SRAM memory module containing 131,072 words organized in a x32-bit configuration. The module consists of four 128K x 8 fast SRAMs mounted on a 64-pin, single-sided, FR4-printed circuit board.

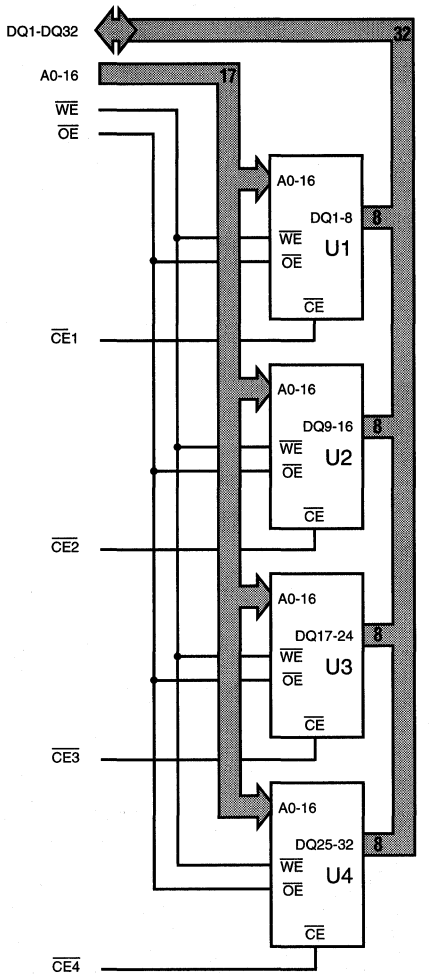
Data is written into the SRAM memory when write enable ($\overline{WE}$) and chip enable ($\overline{CE}$) inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ and output enable ($\overline{OE}$) are LOW. $\overline{CE}$ and/or $\overline{OE}$ can set the output in a High-Z state for additional flexibility in system design and memory expansion.

PD0 and PD1 identify the module's density allowing interchangeable use of alternate density, industry-standard modules. Four chip enable inputs, ($\overline{CE1}$, $\overline{CE2}$, $\overline{CE3}$ and $\overline{CE4}$) are used to enable the module's 4 bytes independently.

The Micron SRAM family uses a high-speed, low- power CMOS design in a four-transistor memory cell featuring double-layer metal, double-layer polysilicon technology. All module components may be powered from a single +5V supply and all inputs and outputs are fully TTL-compatible.

The "L" and "LP" versions each provide a 70 percent reduction in CMOS standby current (I_{SB2}) over the standard version. The "LP" version also provides a 90 percent reduction in TTL standby current (I_{SB1}). This is achieved by including gated inputs on the $\overline{WE}$, $\overline{OE}$ and address lines. The gated inputs also facilitate the design of battery backed systems where the designer needs to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

FUNCTIONAL BLOCK DIAGRAM



U1-U4 = MT5C1008DJ

PRESENCE DETECT
PD0 = No Connect
PD1 = No Connect

TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Storage Temperature ..... -55°C to +125°C
Power Dissipation 4W
Short Circuit Output Current 50mA
Voltage on Any Pin Relative to V_{SS} ..... -1V to V_{CC} +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-20	20	µA	
Output Leakage Current	Output(s) disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

				MAX					
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-15*	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	380	760	620	560	500	mA	3, 13
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	68	180	160	140	120	mA	13
	LP version only	I_{SB1}	5.2	12	12	12	12	mA	13
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IL} ≤ Vss +0.2V V_{IH} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	1.6	20	20	20	20	mA	13
	L and LP versions only	I_{SB2}	1.2	6	6	6	6	mA	13

*Consult factory

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A16, $\overline{WE}$, $\overline{OE}$	T_A = 25°C; f = 1 MHz Vcc = 5V	C_I	35	pF	4
Input Capacitance: $\overline{CE}$1- $\overline{CE}$4		C12	10	pF	4
Input/Output Capacitance: DQ1-DQ32		$C_{I/O}$	10	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) ($0°C \le T_A \le 70°C$; Vcc = 5V ±10%)

		-15*		-20		-25		-35			
DESCRIPTION	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ Cycle											
READ cycle time	^tRC	15		20		25		35		ns	
Address access time	^tAA		15		20		25		35	ns	
Chip Enable access time	^tACE		15		20		25		35	ns	
Output hold from address change	^tOH	3		3		5		5		ns	
Chip Enable to output in Low-Z	^tLZCE	5		5		5		5		ns	7
Chip disable to output in High-Z	^tHZCE		6		8		10		15	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		ns	
Chip disable to power-down time	^tPD		15		20		25		35	ns	
Output Enable access time	^tAOE		5		6		8		12	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		ns	
Output disable to output in High-Z	^tHZOE		5		6		10		12	ns	6
WRITE Cycle											
WRITE cycle time	^tWC	15		20		25		35		ns	
Chip Enable to end of write	^tCW	10		12		15		20		ns	
Address valid to end of write	^tAW	10		12		15		20		ns	
Address setup time	^tAS	0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		ns	
WRITE pulse width	$^tWP1$	9		12		15		20		ns	
WRITE pulse width	$^tWP2$	12		15		15		20		ns	
Data setup time	^tDS	7		8		10		15		ns	
Data hold time	^tDH	0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	3		3		3		3		ns	7
Write Enable to output in High-Z	^tHZWE		6		8		10		15	ns	6, 7

*Consult factory

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

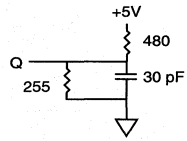


Fig. 1 OUTPUT LOAD EQUIVALENT

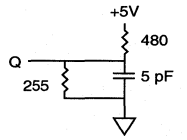


Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

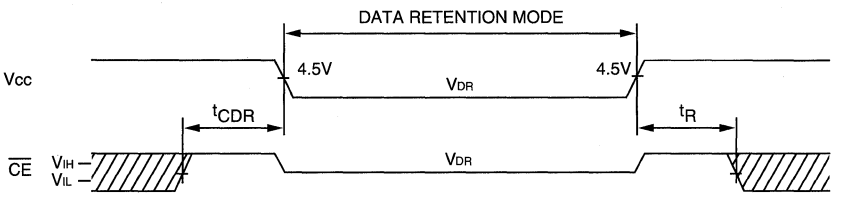
1. All voltages referenced to Vss (GND).
2. -3V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1, unless otherwise noted.
6. ^{t}HZCE, ^{t}HZOE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC=Read Cycle Time
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Typical values are measured at 5V, 25°C and 25ns cycle time.
14. Typical currents are measured at 25°C.
15. Output enable ($\overline{OE}$) is inactive (HIGH).
16. Output enable ($\overline{OE}$) is active (LOW).

DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

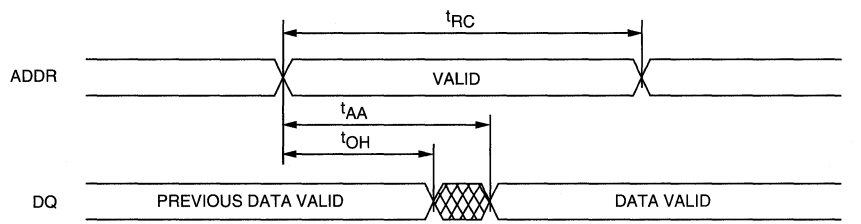
DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2			V	
Data Retention Current L Version	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	ICCDR		140	600	µA	14
		Vcc = 3V	ICCDR		240	1,000	µA	14
		Vcc = 3V*	ICCDR		120	400	µA	14
Data Retention Current LP Version	$\overline{CE}$ ≥ (Vcc -0.2V)	Vcc = 2V	ICCDR		140	600	µA	14
		Vcc = 3V	ICCDR		120	400	µA	14
Chip Deselect to Data Retention Time			^{t}CDR	0			ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4,11

*Consult factory

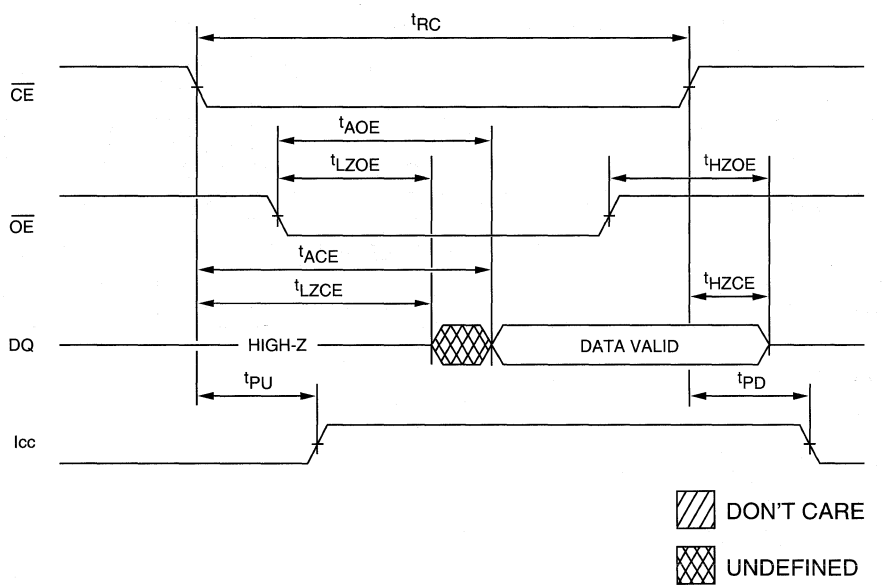
LOW Vcc DATA-RETENTION WAVEFORM



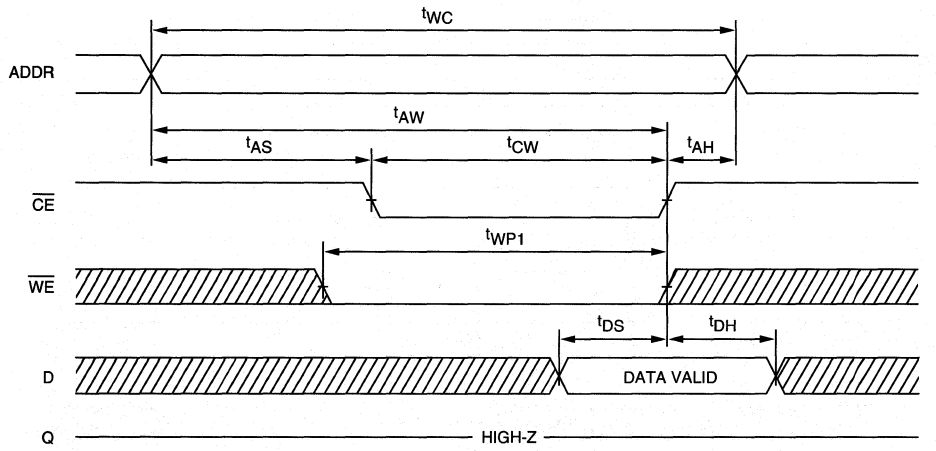
READ CYCLE NO. 1 [8, 9]



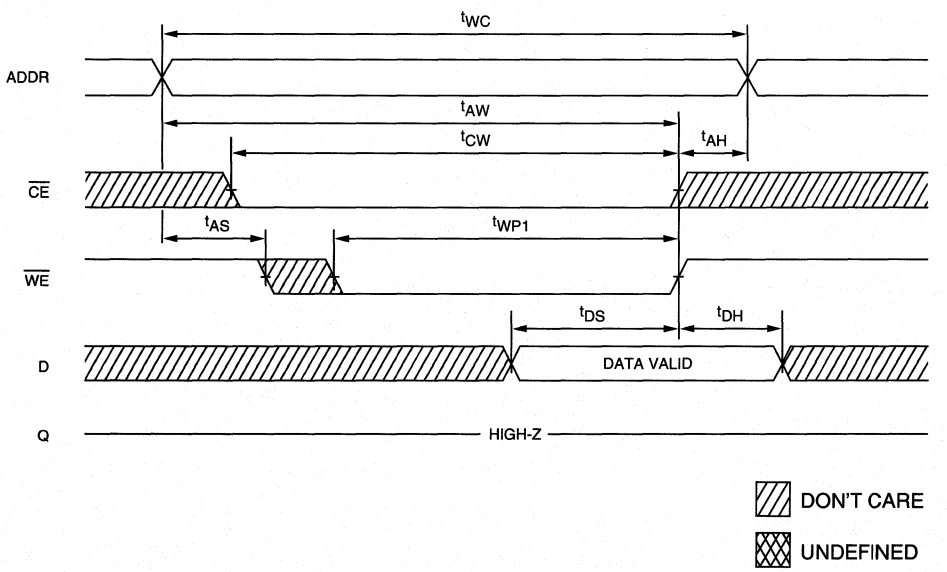
READ CYCLE NO. 2 [7, 8, 10]



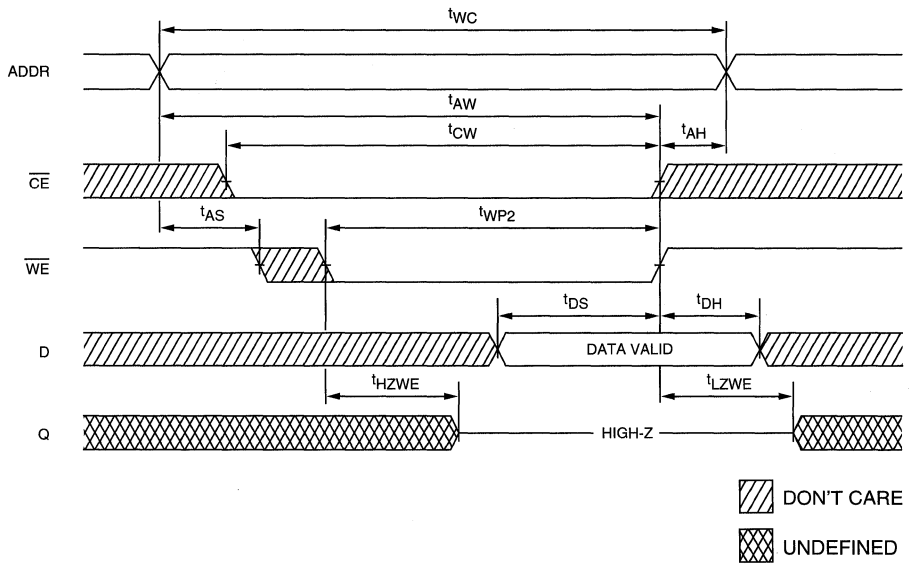
WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)



WRITE CYCLE NO. 2 [12, 13, 15]
(Write Enable Controlled)



WRITE CYCLE NO. 3 [7, 12, 13, 16]
(Write Enable Controlled)



SRAM MODULE

128K x 32 SRAM
LOW VOLTAGE

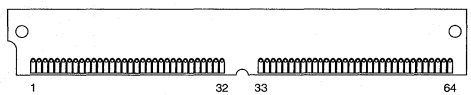
FEATURES
- High speed: 20*, 25 and 35ns
- High-density 512KB design
- High-performance, low-power, CMOS double-metal process
- Single +3.3V ±0.3V power supply
- 5V-tolerant I/O
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ functions
- All inputs and outputs are TTL-compatible
- Industry-standard pinout
- Low profile
- Upgradable to a 256K x 32 module

OPTIONS — MARKING
- Timing
  - 17ns access — -17
  - 20ns access — -20
  - 25ns access — -25
  - 35ns access — -35
- Packages
  - 64-pin SIMM — M
  - 64-pin ZIP — Z
- Optional, 2V data retention — L
- 2V data retention, low power — LP
- Part Number Example: MT4LS12832M-20 LP

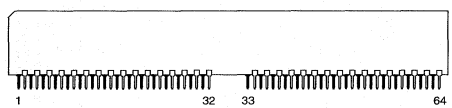
NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

64-Pin SIMM
(SF-3)



64-Pin ZIP
(SG-4)



PIN #	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	Vss	17	A2	33	$\overline{CE4}$	49	A4
2	PD0	18	A9	34	$\overline{CE3}$	50	A11
3	PD1	19	DQ13	35	NC	51	A5
4	DQ1	20	DQ5	36	A16	52	A12
5	DQ9	21	DQ14	37	$\overline{OE}$	53	Vcc
6	DQ2	22	DQ6	38	Vss	54	A13
7	DQ10	23	DQ15	39	DQ25	55	A6
8	DQ3	24	DQ7	40	DQ17	56	DQ21
9	DQ11	25	DQ16	41	DQ26	57	DQ29
10	DQ4	26	DQ8	42	DQ18	58	DQ22
11	DQ12	27	Vss	43	DQ27	59	DQ30
12	Vcc	28	$\overline{WE}$	44	DQ19	60	DQ23
13	A0	29	A15	45	DQ28	61	DQ31
14	A7	30	A14	46	DQ20	62	DQ24
15	A1	31	$\overline{CE2}$	47	A3	63	DQ32
16	A8	32	$\overline{CE1}$	48	A10	64	Vss

GENERAL DESCRIPTION

The MT4LS12832 is a high-speed SRAM memory module containing 131,072 words organized in a x32-bit configuration. The module consists of four low voltage128K x 8 fast SRAMs mounted on a 64-pin, single-sided, FR4-printed circuit board.

Data is written into the SRAM memory when write enable ($\overline{WE}$) and chip enable ($\overline{CE}$) inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ and output enable ($\overline{OE}$) are LOW. $\overline{CE}$ and/or $\overline{OE}$ can set the output in a High-Z state for additional flexibility in system design and memory expansion.

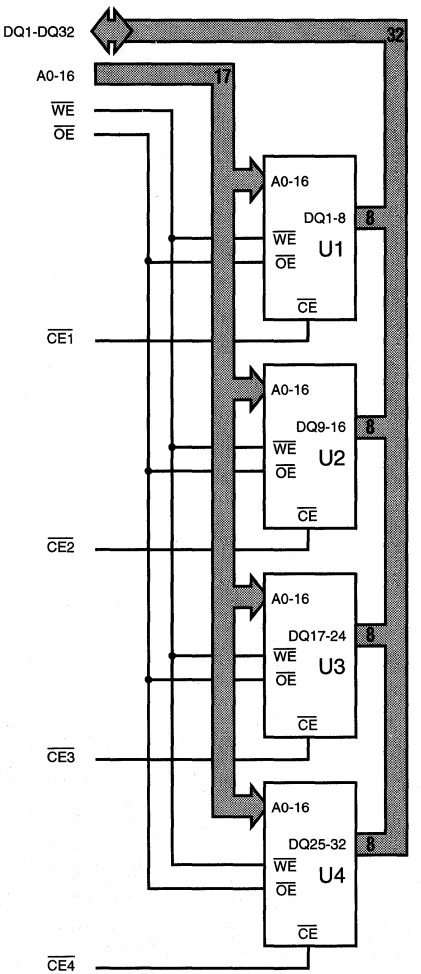
PD0 and PD1 identify the module's density allowing interchangeable use of alternate density, industry-standard modules. Four chip enable inputs, ($\overline{CE1}$, $\overline{CE2}$, $\overline{CE3}$ and $\overline{CE4}$) are used to enable the module's 4 bytes independently.

The Micron SRAM family uses a high-speed, low-power CMOS design in a four-transistor memory cell featuring double-layer metal, double-layer polysilicon technology. All module components may be powered from a single +3.3V DC supply and all inputs and outputs are fully TTL-compatible.

The "L" and "LP" versions each provide a significant reduction in CMOS standby current (I_{SB2}) over the standard version. The "LP" version also provides a significant reduction in TTL standby current (I_{SB1}). This is achieved by including gated inputs on the $\overline{WE}$, $\overline{OE}$ and address lines. The gated inputs also facilitate the design of battery backed systems where the designer needs to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

NEW SRAM MODULE

FUNCTIONAL BLOCK DIAGRAM



U1-U4 = MT5LC1008DJ

PRESENCE DETECT
PD0 = No Connect
PD1 = No Connect

TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -0.5V to +4.6V
V_{IN} ..... -0.5V to +6.0V
Storage temperature ..... -55°C to +125°C
Power dissipation 4W
Short circuit output current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ±0.3V)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.0	5.5V	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ Vcc	I_{LI}	-4	4	µA	
Output Leakage Current	Output(s) disabled 0V ≤ V_{OUT} ≤ Vcc	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		Vcc	3.0	3.6	V	1

				MAX					
DESCRIPTION	CONDITIONS	SYMBOL	VER	-17	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; Vcc = MAX f = MAX = 1/ ^tRC outputs open	Icc	ALL	340	300	260	220	mA	3, 13
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; Vcc = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	STD,L	80	72	56	48	mA	13
			LP	4	4	4	4	mA	13
	$\overline{CE}$ ≥ Vcc -0.2V; Vcc = MAX V_{IN} ≤ Vss +0.2V or V_{IN} ≥ Vcc -0.2V; f = 0	I_{SB2}	STD,L	1.2	1.2	1.2	1.2	mA	13
			LP	400	400	400	400	µA	13

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A17, $\overline{WE}$, $\overline{OE}$	T_A = 25°C; f = 1 MHz Vcc = 3.3V	C_{I1}	30	pF	4
Input Capacitance: $\overline{CE1}$-$\overline{CE4}$		C_{I2}	10	pF	4
Input/Output Capacitance: DQ1-DQ32		$C_{I/O}$	10	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ±0.3V)

		-17		-20		-25		-35			
DESCRIPTION	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ Cycle											
READ cycle time	^tRC	17		20		25		35		ns	
Address access time	^tAA		17		20		25		35	ns	
Chip Enable access time	^tACE		17		20		25		35	ns	
Output hold from address change	^tOH	3		3		5		5		ns	
Chip Enable to output in Low-Z	^tLZCE	5		3		5		5		ns	7
Chip disable to output in High-Z	^tHZCE		7		8		10		15	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		ns	
Chip disable to power-down time	^tPD		17		20		25		35	ns	
Output Enable access time	^tAOE		5		4		8		12	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		ns	
Output disable to output in High-Z	^tHZOE		5		4		10		12	ns	6
WRITE Cycle											
WRITE cycle time	^tWC	17		20		25		35		ns	
Chip Enable to end of write	^tCW	12		12		15		20		ns	
Address valid to end of write	^tAW	12		12		15		20		ns	
Address setup time	^tAS	0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		ns	
WRITE pulse width	$^tWP1$	12		12		15		20		ns	
WRITE pulse width	$^tWP2$	15		15		15		20		ns	
Data setup time	^tDS	8		8		10		15		ns	
Data hold time	^tDH	0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	3		3		5		5		ns	7
Write Enable to output in High-Z	^tHZWE		7		8		10		15	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

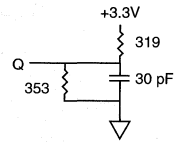


Fig. 1 OUTPUT LOAD EQUIVALENT

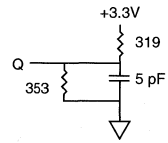


Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

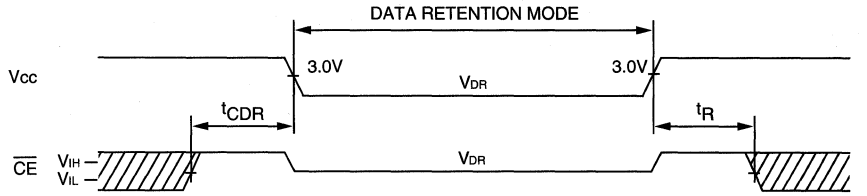
1. All voltages referenced to V_{SS} (GND).
2. Overshoot: $V_{IH} \leq +6.0V$ for $t \leq {}^tKC/2$
   Undershoot: $V_{IL} \geq -2.0V$ for $t \leq {}^tKC/2$
   Power-up: $V_{IH} \geq +6.0V$ and $V_{CC} \leq 3.1V$ for $t \leq 200$ msec.
3. I_{CC} is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1, unless otherwise noted.
6. ${}^tHZCE$, ${}^tHZOE$ and ${}^tHZWE$ are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ${}^tHZCE$ is less than ${}^tLZCE$ and ${}^tHZWE$ is less than ${}^tLZWE$.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ${}^tRC$=READ cycle time
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Typical values are measured at 3.3V, 25°C and 25ns cycle time.
14. Typical currents are measured at 25°C. MAX is over operating temperature range.
15. Output enable ($\overline{OE}$) is inactive (HIGH).
16. Output enable ($\overline{OE}$) is active (LOW).

DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP versions only)

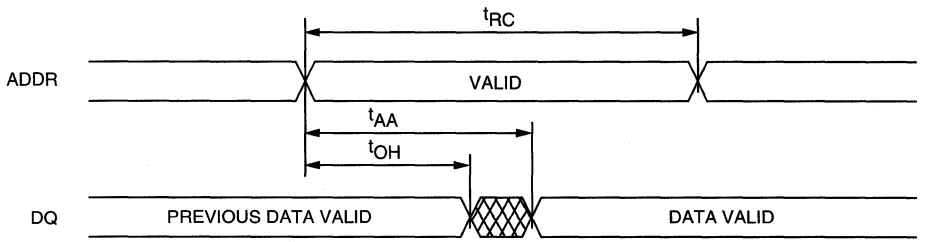
DESCRIPTION	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V_{CC} for Retention Data		V_{DR}	2			V	
Data Retention Current	$\overline{CE} \geq V_{CC}$ -0.2V Other inputs: $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq V_{SS}$+0.2V V_{CC} = 2V	I_{CCDR}		TBD	200	µA	14
Chip Deselect to Data		${}^tCDR$	0			ns	4
Retention Time							
Operation Recovery Time		${}^tR$	${}^tRC$			ns	4, 11

NEW SRAM MODULE

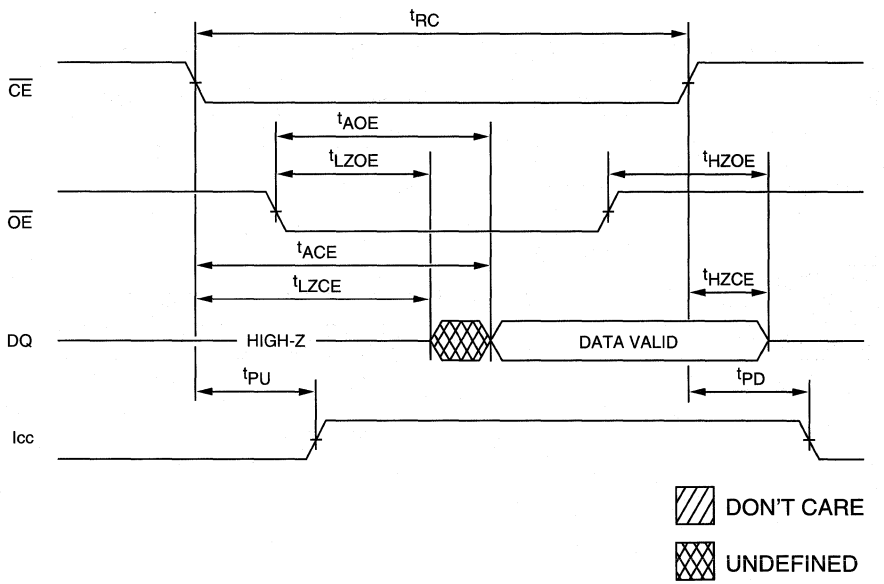
LOW Vcc DATA RETENTION WAVEFORM



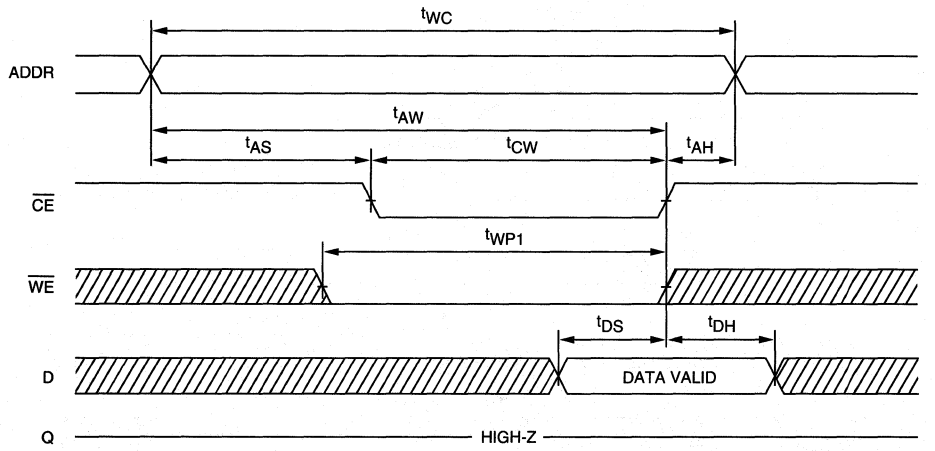
READ CYCLE NO. 1 [8, 9]



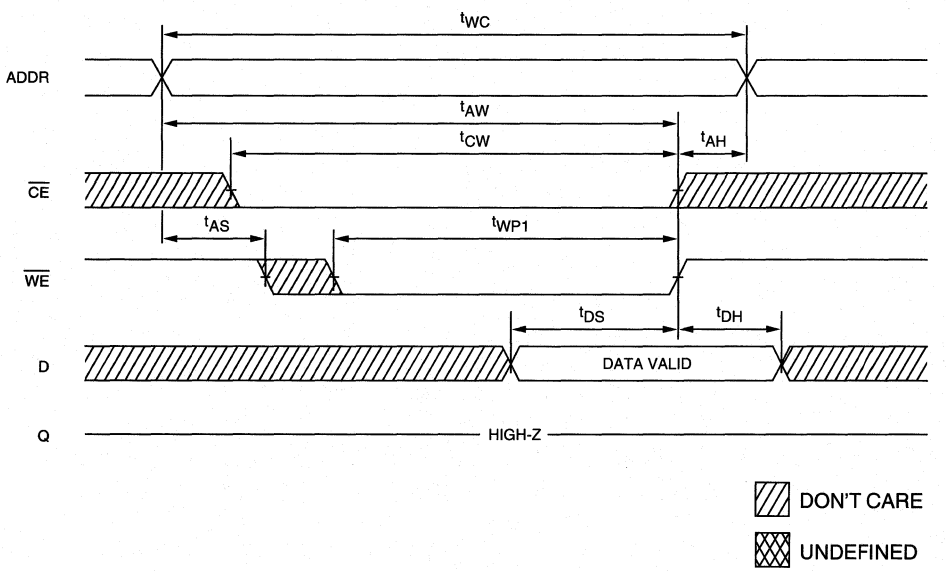
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)

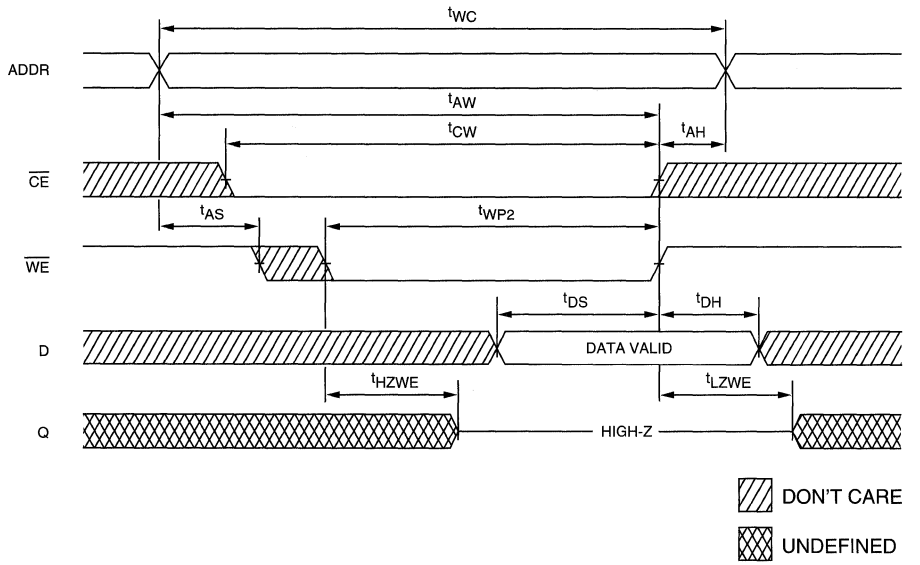


WRITE CYCLE NO. 2 [12, 13, 15]
(Write Enable Controlled)



NEW SRAM MODULE

WRITE CYCLE NO. 3 [7, 12, 13, 16]
(Write Enable Controlled)



SRAM MODULE

256K x 32 SRAM

FEATURES

- High speed: 15*, 20, 25 and 35ns
- High-density 1MB design
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ functions
- Industry-standard pinout
- All inputs and outputs are TTL-compatible
- Low profile

OPTIONS MARKING

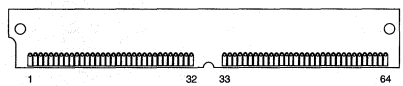
- Timing
  - 15ns access -15*
  - 20ns access -20
  - 25ns access -25
  - 35ns access -35
- Packages
  - 64-pin SIMM M
  - 64-pin ZIP Z
- Optional, 2V data retention L
  - 2V data retention, low power LP
- Part Number Example: MT8S25632Z-15 L

'Consult factory

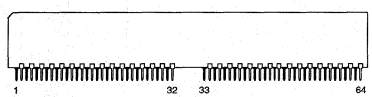
NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

64-Pin SIMM
(SF-4)



64-Pin ZIP
(SG-1)



PIN #	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	Vss	17	A2	33	$\overline{CE4}$	49	A4
2	PD0	18	A9	34	$\overline{CE3}$	50	A11
3	PD1	19	DQ13	35	A17	51	A5
4	DQ1	20	DQ5	36	A16	52	A12
5	DQ9	21	DQ14	37	$\overline{OE}$	53	Vcc
6	DQ2	22	DQ6	38	Vss	54	A13
7	DQ10	23	DQ15	39	DQ25	55	A6
8	DQ3	24	DQ7	40	DQ17	56	DQ21
9	DQ11	25	DQ16	41	DQ26	57	DQ29
10	DQ4	26	DQ8	42	DQ18	58	DQ22
11	DQ12	27	Vss	43	DQ27	59	DQ30
12	Vcc	28	$\overline{WE}$	44	DQ19	60	DQ23
13	A0	29	A15	45	DQ28	61	DQ31
14	A7	30	A14	46	DQ20	62	DQ24
15	A1	31	$\overline{CE2}$	47	A3	63	DQ32
16	A8	32	$\overline{CE1}$	48	A10	64	Vss

GENERAL DESCRIPTION

The MT8S25632 is a high-speed SRAM memory module containing 262,144 words organized in a x32-bit configuration. The module consists of eight 256K x 4 fast SRAMs mounted on a 64-pin, double-sided, FR4-printed circuit board.

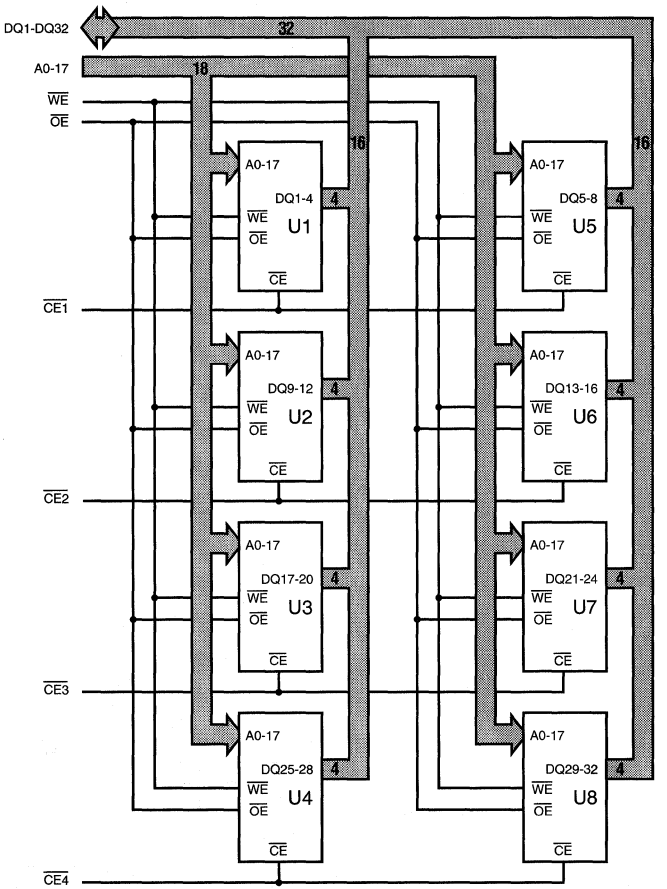
Data is written into the SRAM memory when write enable ($\overline{WE}$) and chip enable ($\overline{CE}$) inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ and output enable ($\overline{OE}$) are LOW. $\overline{CE}$ and/or $\overline{OE}$ can set the output in High-Z for additional flexibility in system design and memory expansion.

PD0 and PD1 identify the module's density allowing interchangeable use of alternate density, industry standard modules. Four chip enable inputs, ($\overline{CE1}$, $\overline{CE2}$, $\overline{CE3}$ and $\overline{CE4}$) are used to enable the module's 4 bytes independently.

The Micron SRAM family uses a high-speed, low-power CMOS design in a four-transistor memory cell featuring double-layer metal, double-layer polysilicon technology. All module components may be powered from a single +5V supply and all inputs and outputs are fully TTL-compatible.

The "L" and "LP" versions each provide a 70 percent reduction in CMOS standby current (I_{SB2}) over the standard version. The "LP" version also provides a 90 percent reduction in TTL standby current (I_{SB1}) through the use of gated inputs on the $\overline{WE}$, $\overline{OE}$ and address lines, which also facilitates the design of battery backed systems. That is, the gated inputs simplify the design effort and circuitry required to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

FUNCTIONAL BLOCK DIAGRAM



PRESENCE DETECT U1-U8 = MT5C1005DJ
PD0 = Vss
PD1 = Vss

TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Storage Temperature ..... -55°C to +125°C
Power Dissipation 8W
Short Circuit Output Current 50mA
Voltage on Any Pin Relative to V_{SS} ..... -1V to V_{CC} +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	Vcc+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ Vcc	I_{LI}	-40	40	µA	
Input/Output Leakage Current	Output(s) disabled DQ1-DQ32 0V ≤ V_{OUT} ≤ Vcc	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		Vcc	4.5	5.5	V	1

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX -15*	MAX -20	MAX -25	MAX -35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; Vcc = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	760	1,520	1,240	1,120	1,000	mA	3, 13
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; Vcc = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	136	360	320	280	200	mA	13
	LP version only	I_{SB1}	10.4	24	24	24	24	mA	13
	$\overline{CE}$ ≥ Vcc -0.2V; Vcc = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ Vcc -0.2V; f = 0	I_{SB2}	3.2	40	40	40	40	mA	13
	L and LP versions only	I_{SB2}	2.4	12	12	12	12	mA	13

Consult factory

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance; A0-A17, $\overline{WE}$, $\overline{OE}$	T_A = 25°C; f = 1 MHz Vcc = 5V	C_{I1}	60	pF	4
Input Capacitance; $\overline{CE1}$-$\overline{CE4}$		C_{I2}	15	pF	4
Input/Output Capacitance: DQ1-DQ32		$C_{I/O}$	10	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

		-15*		-20		-25		-35			
DESCRIPTION	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ Cycle											
READ cycle time	^tRC	15		20		25		35		ns	
Address access time	^tAA		15		20		25		35	ns	
Chip Enable access time	^tACE		15		20		25		35	ns	
Output hold from address change	^tOH	3		3		5		5		ns	
Chip Enable to output in Low-Z	^tLZCE	5		5		5		5		ns	7
Chip disable to output in High-Z	^tHZCE		6		8		10		15	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		ns	
Chip disable to power-down time	^tPD		15		20		25		35	ns	
Output Enable access time	^tAOE		5		6		8		12	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		ns	
Output disable to output in High-Z	^tHZOE		5		6		10		12	ns	6
WRITE Cycle											
WRITE cycle time	^tWC	15		20		25		35		ns	
Chip Enable to end of write	^tCW	10		12		15		20		ns	
Address valid to end of write	^tAW	10		12		15		20		ns	
Address setup time	^tAS	0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		ns	
WRITE pulse width	$^tWP1$	9		12		15		20		ns	
WRITE pulse width	$^tWP2$	12		15		15		20		ns	
Data setup time	^tDS	7		8		10		15		ns	
Data hold time	^tDH	0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	3		3		3		3		ns	7
Write Enable to output in High-Z	^tHZWE		6		8		10		15	ns	6, 7

*Consult factory

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

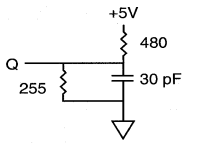


Fig. 1 OUTPUT LOAD EQUIVALENT

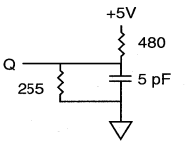


Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

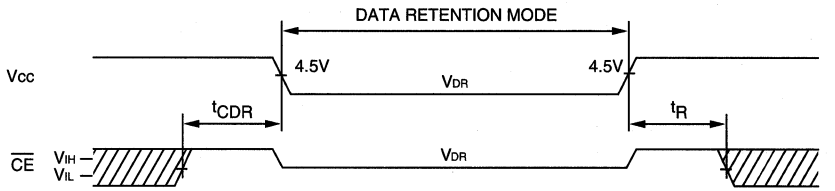
1. All voltages referenced to Vss (GND).
2. -3V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZOE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC=Read Cycle Time
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Typical values are measured at 5V, 25°C and 25ns cycle time.
14. Typical values are measured at 25°C.
15. Output enable ($\overline{OE}$) is inactive (HIGH).
16. Output enable ($\overline{OE}$) is active (LOW).

DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

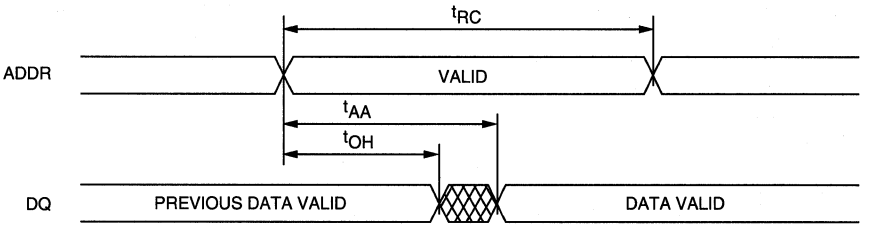
DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2			V	
Data Retention Current L Version	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	ICCDR		280	1,200	µA	14
		Vcc = 3V			480	2,000	µA	14
		Vcc = 3V*			240	800	µA	14
Data Retention Current LP Version	$\overline{CE}$ ≥ (Vcc -0.2V)	Vcc = 2V	ICCDR		280	1,200	µA	14
		Vcc = 3V	ICCDR		240	2,000	µA	14
Chip Deselect to Data Retention Time			^{t}CDR	0			ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4,11

*Consult factory

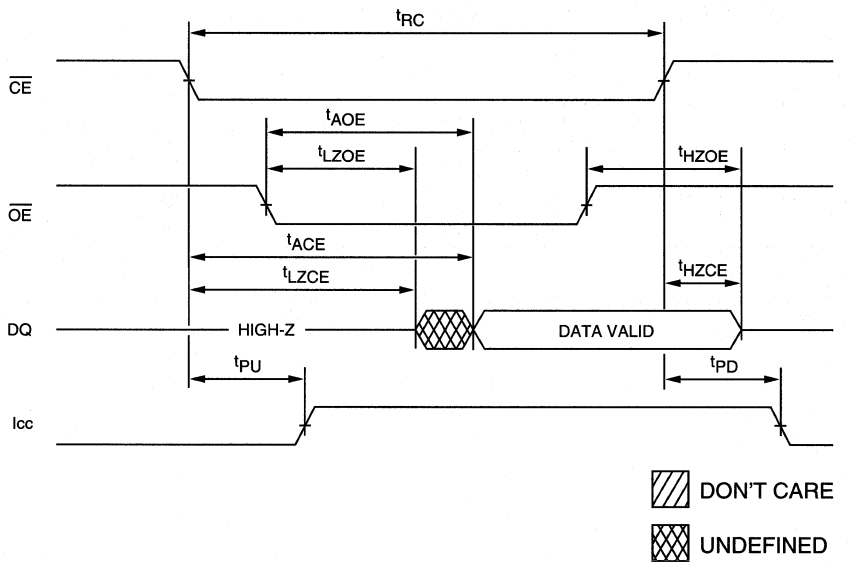
LOW Vcc DATA-RETENTION WAVEFORM



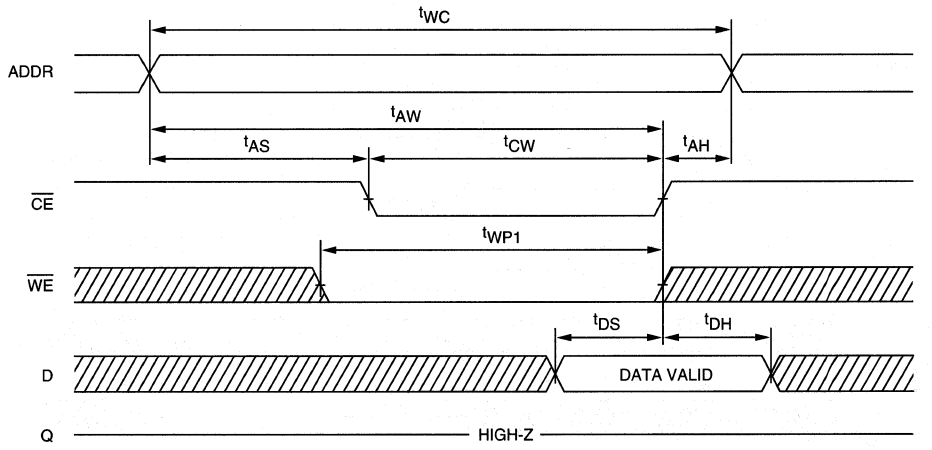
READ CYCLE NO. 1 [8, 9]



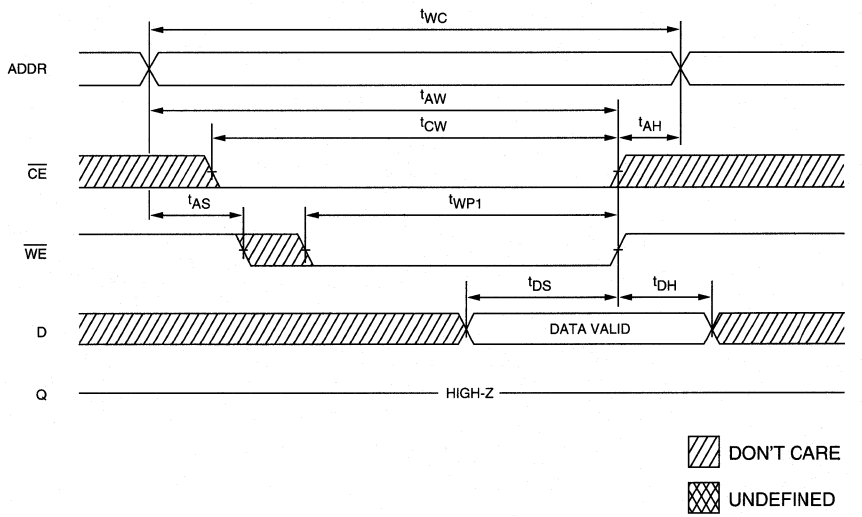
READ CYCLE NO. 2 [7, 8, 10]



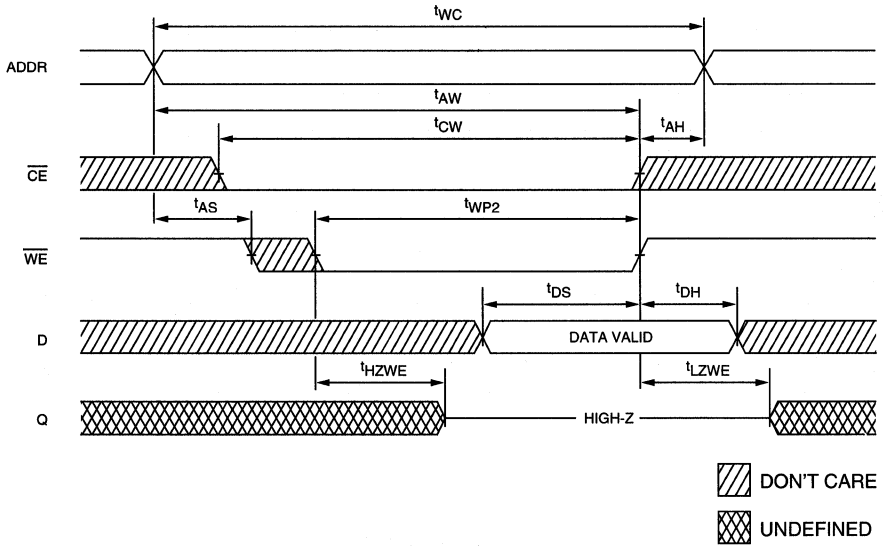
WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)



WRITE CYCLE NO. 2 [12, 15]
(Write Enable Controlled)



WRITE CYCLE NO. 3 [7, 12, 16]
(Write Enable Controlled)



SRAM MODULE

256K x 32 SRAM
LOW VOLTAGE

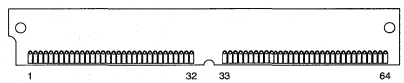
FEATURES
- High speed: 20*, 25 and 35ns
- High-density 1MB design
- High-performance, low-power, CMOS double-metal process
- Single +3.3V ± 0.3V power supply
- 5V-tolerant I/O
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ functions
- Industry-standard pinout
- All inputs and outputs are TTL-compatible
- Low profile

OPTIONS — MARKING
- Timing
  - 17ns access — -17
  - 20ns access — -20
  - 25ns access — -25
  - 35ns access — -35
- Packages
  - 64-pin SIMM — M
  - 64-pin ZIP — Z
- Optional, 2V data retention — L
  - 2V data retention, low power — LP
- Part Number Example: MT8LS25632Z-20 LP

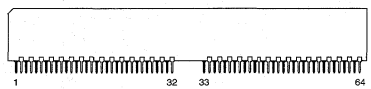
NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

64-Pin SIMM
(SF-4)



64-Pin ZIP
(SG-1)



PIN #	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	Vss	17	A2	33	$\overline{CE4}$	49	A4
2	PD0	18	A9	34	$\overline{CE3}$	50	A11
3	PD1	19	DQ13	35	A17	51	A5
4	DQ1	20	DQ5	36	A16	52	A12
5	DQ9	21	DQ14	37	$\overline{OE}$	53	Vcc
6	DQ2	22	DQ6	38	Vss	54	A13
7	DQ10	23	DQ15	39	DQ25	55	A6
8	DQ3	24	DQ7	40	DQ17	56	DQ21
9	DQ11	25	DQ16	41	DQ26	57	DQ29
10	DQ4	26	DQ8	42	DQ18	58	DQ22
11	DQ12	27	Vss	43	DQ27	59	DQ30
12	Vcc	28	$\overline{WE}$	44	DQ19	60	DQ23
13	A0	29	A15	45	DQ28	61	DQ31
14	A7	30	A14	46	DQ20	62	DQ24
15	A1	31	$\overline{CE2}$	47	A3	63	DQ32
16	A8	32	$\overline{CE1}$	48	A10	64	Vss

GENERAL DESCRIPTION

The MT8LS25632 is a high-speed SRAM memory module containing 262,144 words organized in a x32-bit configuration. The module consists of eight low voltage 256K x 4 fast SRAMs mounted on a 64-pin, double-sided, FR4-printed circuit board.

Data is written into the SRAM memory when write enable ($\overline{WE}$) and chip enable ($\overline{CE}$) inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ and output enable ($\overline{OE}$) are LOW. $\overline{CE}$ and/or $\overline{OE}$ can set the output in High-Z for additional flexibility in system design and memory expansion.

PD0 and PD1 identify the module's density allowing interchangeable use of alternate density, industry standard modules. Four chip enable inputs, ($\overline{CE1}$, $\overline{CE2}$, $\overline{CE3}$ and $\overline{CE4}$) are used to enable the module's 4 bytes independently.

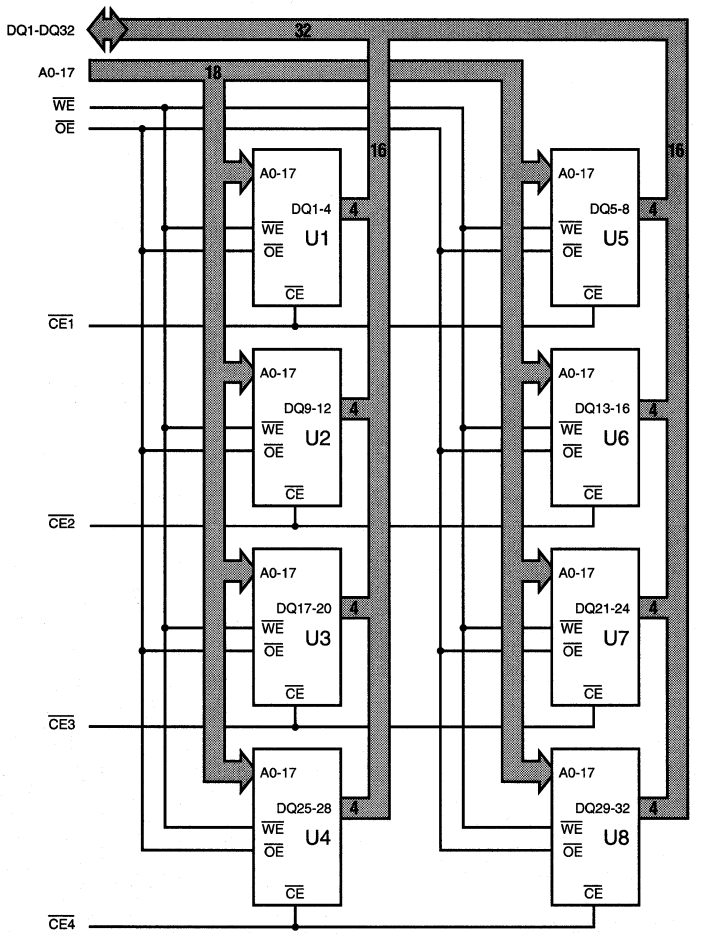
The Micron SRAM family uses a high-speed, low-power CMOS design in a four-transistor memory cell featuring double-layer metal, double-layer polysilicon technology.

All module components may be powered from a single +3.3V DC supply and all inputs and outputs are fully TTL-compatible.

The "L" and "LP" versions each provide a significant reduction in CMOS standby current (I_{SB2}) over the standard version. The "LP" version also provides a significant reduction in TTL standby current (I_{SB1}) through the use of gated inputs on the $\overline{WE}$, $\overline{OE}$ and address lines, which also facilitates the design of battery backed systems. That is, the gated inputs simplify the design effort and circuitry required to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

NEW SRAM MODULE

FUNCTIONAL BLOCK DIAGRAM



PRESENCE DETECT U1-U8 = MT5LC1005DJ
PD0 = Vss
PD1 = Vss

TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -0.5V to +4.6V
V_{IN} ..... -0.5V to +6.0V
Storage temperature ..... -55°C to +125°C
Power dissipation 8W
Short circuit output current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ±0.3V)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage			V_{IH}	2.0	5.5V	V	1, 2
Input Low (Logic 0) Voltage			V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ Vcc		I_{LI}	-8	8	µA	
Input/Output Leakage Current	Output(s) disabled 0V ≤ V_{OUT} ≤ Vcc	DQ1-DQ32	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -4.0mA		V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA		V_{OL}		0.4	V	1
Supply Voltage			Vcc	3.0	3.6	V	1

DESCRIPTION	CONDITIONS	SYMBOL	VER	MAX -17	MAX -20	MAX -25	MAX -35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; Vcc = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	ALL	680	600	520	440	mA	3, 13
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; Vcc = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	STD,L	160	144	112	96	mA	13
			LP	4	4	4	4	mA	13
	$\overline{CE}$ ≥ Vcc -0.2V; Vcc = MAX V_{IN} ≤ Vss +0.2V or V_{IN} ≥ Vcc -0.2V; f = 0	I_{SB2}	STD,L	2.4	2.4	2.4	2.4	mA	13
			LP	0.8	800	800	800	µA	13

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A17, $\overline{WE}$, $\overline{OE}$	T_A = 25°C; f = 1 MHz Vcc = 3.3V	C_{I1}	70	pF	4
Input Capacitance: $\overline{CE1}$-$\overline{CE4}$		C_{I2}	15	pF	4
Input/Output Capacitance: DQ1-DQ32		$C_{I/O}$	10	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) ($0°C \le T_A \le 70°C$; $V_{CC} = 3.3V \pm 0.3V$)

		-17		-20		-25		-35			
DESCRIPTION	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ Cycle											
READ cycle time	^tRC	17		20		25		35		ns	
Address access time	^tAA		17		20		25		35	ns	
Chip Enable access time	^tACE		17		20		25		35	ns	
Output hold from address change	^tOH	3		3		5		5		ns	
Chip Enable to output in Low-Z	^tLZCE	5		3		5		5		ns	7
Chip disable to output in High-Z	^tHZCE		7		8		10		15	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		ns	
Chip disable to power-down time	^tPD		17		20		25		35	ns	
Output Enable access time	^tAOE		5		4		8		12	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		ns	
Output disable to output in High-Z	^tHZOE		5		4		10		12	ns	6
WRITE Cycle											
WRITE cycle time	^tWC	17		20		25		35		ns	
Chip Enable to end of write	^tCW	12		12		15		20		ns	
Address valid to end of write	^tAW	12		12		15		20		ns	
Address setup time	^tAS	0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		ns	
WRITE pulse width	$^tWP1$	12		12		15		20		ns	
WRITE pulse width	$^tWP2$	8		15		15		20		ns	
Data setup time	^tDS	7		8		10		15		ns	
Data hold time	^tDH	0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	3		3		5		5		ns	7
Write Enable to output in High-Z	^tHZWE		7		8		10		15	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 2.8V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

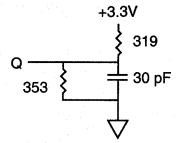


Fig. 1 OUTPUT LOAD EQUIVALENT

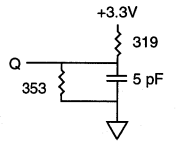


Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

1. All voltages referenced to Vss (GND).
2. Overshoot: $V_{IH} \leq +6.0V$ for $t \leq {}^tKC/2$
   Undershoot: $V_{IL} \geq -2.0V$ for $t \leq {}^tKC/2$
   Power-up: $V_{IH} \geq +6.0V$ and $V_{CC} \leq 3.1V$ for $t \leq 200$ msec.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1, unless otherwise noted.
6. ${}^tHZCE$, ${}^tHZOE$ and ${}^tHZWE$ are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ${}^tHZCE$ is less than ${}^tLZCE$ and ${}^tHZWE$ is less than ${}^tLZWE$.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ${}^tRC$=READ cycle time
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Typical values are measured at 3.3V, 25°C and 25ns cycle time.
14. Typical currents are measured at 25°C. MAX is over operating temperature range.
15. Output enable ($\overline{OE}$) is inactive (HIGH).
16. Output enable ($\overline{OE}$) is active (LOW).

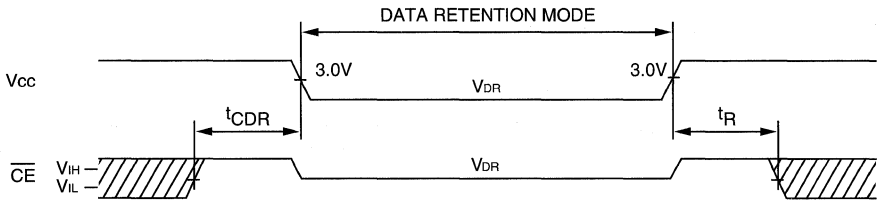
DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP versions only)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data		V_{DR}	2			V	
Data Retention Current L Version	$\overline{CE} \geq$ Vcc -0.2V Other inputs: $V_{IN} \geq$ Vcc -0.2V or $V_{IN} \leq$ Vss+0.2V Vcc = 2V	I_{CCDR}		TBD	400	µA	14
Data Retention Current LP Version	$\overline{CE} \geq$ Vcc -0.2V Vcc = 2V	I_{CCDR}		TBD	400	µA	14
Chip Deselect to Data Retention Time		${}^tCDR$	0			ns	4
Operation Recovery Time		${}^tR$	${}^tRC$			ns	4, 11

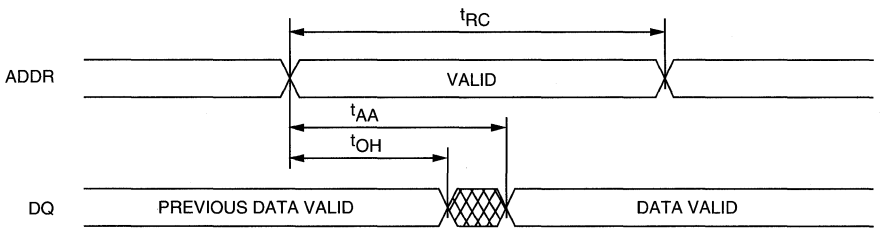
NEW SRAM MODULE

NEW SRAM MODULE

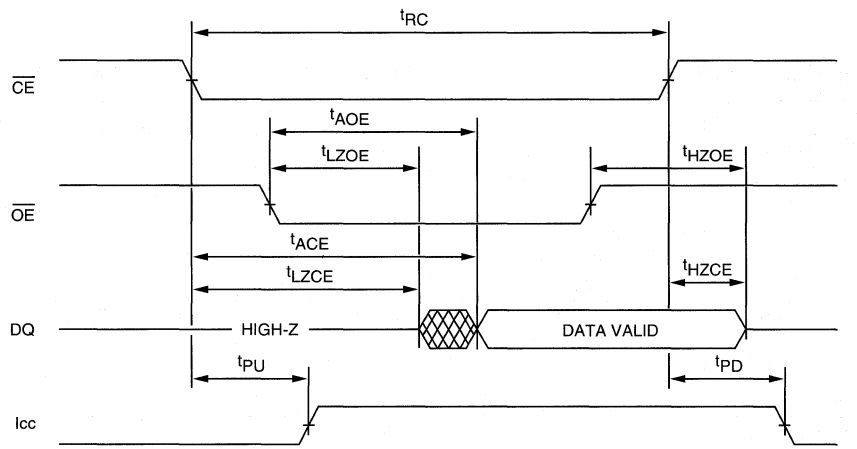
LOW Vcc DATA RETENTION WAVEFORM



READ CYCLE NO. 1 [8, 9]



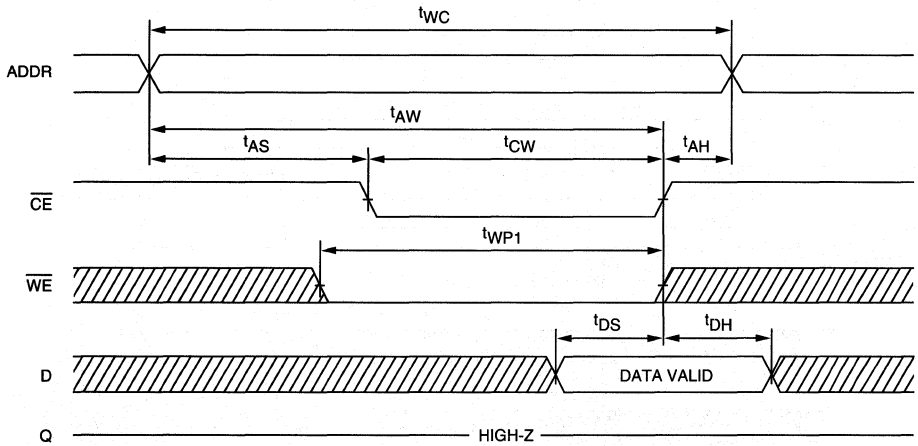
READ CYCLE NO. 2 [7, 8, 10]



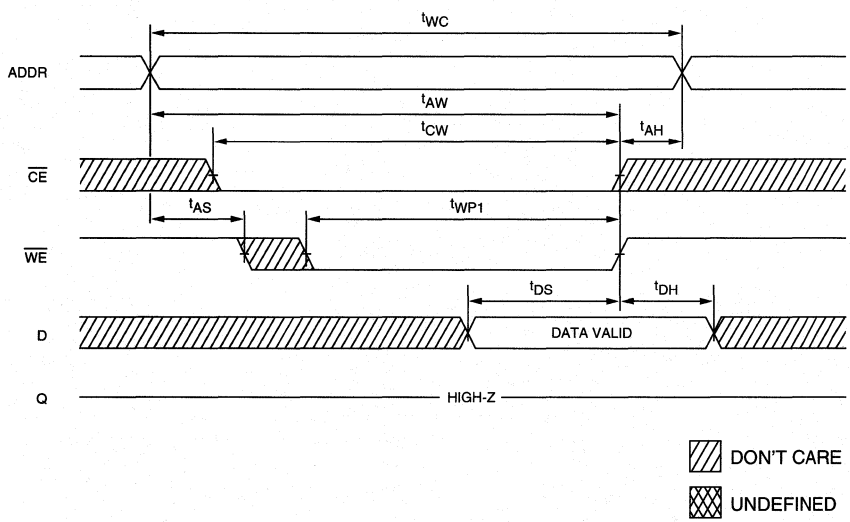
DON'T CARE

UNDEFINED

WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)

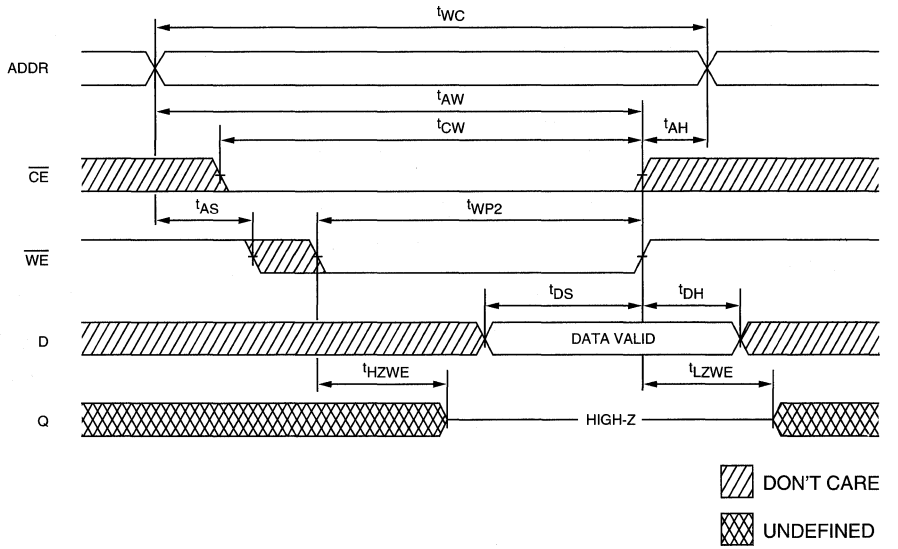


WRITE CYCLE NO. 2 [12, 15]
(Write Enable Controlled)



NEW SRAM MODULE

WRITE CYCLE NO. 3 [7, 12, 16]
(Write Enable Controlled)



MICRON
SEMICONDUCTOR, INC.

TECHNICAL NOTE SELECTION GUIDE

TECHNICAL NOTE

MOISTURE ABSORPTION IN PLASTIC PACKAGES

INTRODUCTION

All plastic integrated-circuit packages have a tendency to absorb moisture. During surface-mount assembly, this moisture can vaporize when subjected to the heat associated with solder reflow operations. Vaporization creates internal stresses that can cause the plastic molding compound to crack. Cracks in the package allow contamination to penetrate to the die and potentially reduce the reliability of the semiconductor device. The cracking process associated with surface-mountable devices is commonly referred to as the "popcorn effect."

Cracks in the plastic pose several reliability concerns. The moisture path to the die is shortened, allowing ion migration or corrosion to occur more readily. Minor cracks which might not be harmful initially could propagate with time, resulting in a longer-term functional failure.

Since plastic packages absorb moisture, care must be taken to prevent exposure for any long period prior to surface-mounting the devices on the printed circuit board. If exposed to excessive moisture, the devices should be baked to remove moisture prior to solder reflow operations.

This technical note describes the shipping procedures that ensure Micron's customers will receive memory devices that do not exhibit the popcorn effect. It also discusses Micron's recommendations for baking the devices if they are exposed to excessive moisture.

ABSORPTION CHARACTERISTICS

Micron's extensive testing empirically characterizes the moisture absorption characteristics of plastic packages. As the plastic takes on moisture, the weight of the device increases. Micron employs a standard procedure for weighing the device before and after it is exposed to moisture. We calculate the percentage of weight gain to determine the relative efficiency of different packaging techniques used for shipping devices.

MICRON PROCEDURES

Micron has eliminated any chance of having popcorn failures with surface-mount packages by shipping all surface-mount devices in sealed bags containing a desiccant. Devices stored in these bags show no measurable weight gain when subjected to a high-humidity environment for long time periods.

DEVICE STORAGE

To prevent device failure due to the popcorn effect, store plastic surface-mount packages carefully before PCB assembly. Micron has run tests on devices that have been exposed to 50 percent humidity outside of their shipping containers for time intervals from six months to one year, and no failures have been recorded.

Any concerns about the moisture absorption can be eliminated by storing the devices in Micron's shipping bags. We designed these containers to prevent the passage of water vapor for long periods of time.

DEVICE BAKING

If devices have been removed from their shipping containers and exposed to high levels of moisture, Micron recommends a device bake-out procedure before surface mounting. This bake-out may be accomplished by placing the parts in a tray and baking them in an oven for 160 hours at 40° C. Any moisture is driven out of the devices during the exposure to the heat.

Moisture may be removed faster by baking at 100° C for 24 hours.

SUMMARY

1. All plastic packages absorb moisture when exposed to high levels of humidity for long time intervals.
2. Micron devices have not exhibited any popcorn effect when exposed to 50 percent humidity for long time periods.
3. Micron ships all surface-mount packages in containers that prevent absorption of moisture.
4. If devices have been removed from their shipping containers and exposed to excessive moisture, they should be baked before being surface-mounted.

REFERENCES

"Moisture Absorption and Mechanical Performance of Surface Mountable Plastic Packages": Bhattacharyya, B. K., et al. : 1988 Proceedings of the 38th Electronics Components Conference.

"Analysis of Package Cracking During Reflow Soldering Process": Kitano, M., et al. : 26th Annual Proceeding, Reliability Physics, 1988.

"Moisture Induced Package Cracking in Plastic Encapsulated Surface Mounted Components During Solder Reflow Process": Lin, R., et al.: 26th Annual Proceeding, Reliability Physics, 1988.

TECHNICAL NOTE

TAPE-AND-REEL PROCEDURES

GENERAL DESCRIPTION

Tape-and-reel is becoming the packaging and shipment method of choice for Micron's surface-mounted memory devices. Tape-and-reel minimizes the handling of components by directly interfacing with automatic pick-and-place machines.

Micron supports the Electronic Industries Association's (EIA) standardization of tape-and-reel specifications number 481A. The intent of this technical note is to describe Micron's status in support of the EIA standard.

Table 1*
MICRON TAPE SIZES AND DEVICES PER REEL

COMPONENT	TAPE WIDTH (W) mm	PITCH (P) mm	DEVICES PER 13-INCH REEL
PLCC			
18 Pin	24	12	1,000
52 Pin	32	16	500
SOJ (300 mil)			
20/26 Pin	24	12	1,000
24 Pin	24	12	1,000
28 Pin	24	12	1,000
SOJ (400 mil)			
28 Pin	32	16	500
32 Pin	44	16	500
40 Pin	44	16	500

*These are examples of tape-and-reel sizes available. Please contact Micron for all available options.

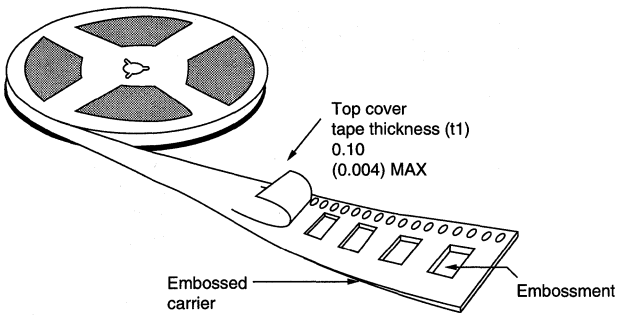


Figure 1
REEL

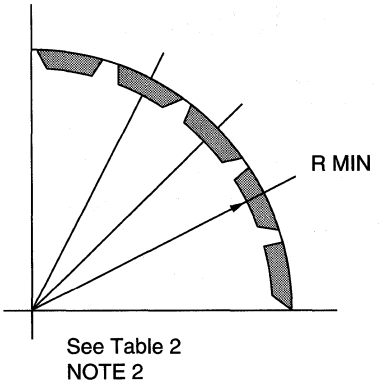
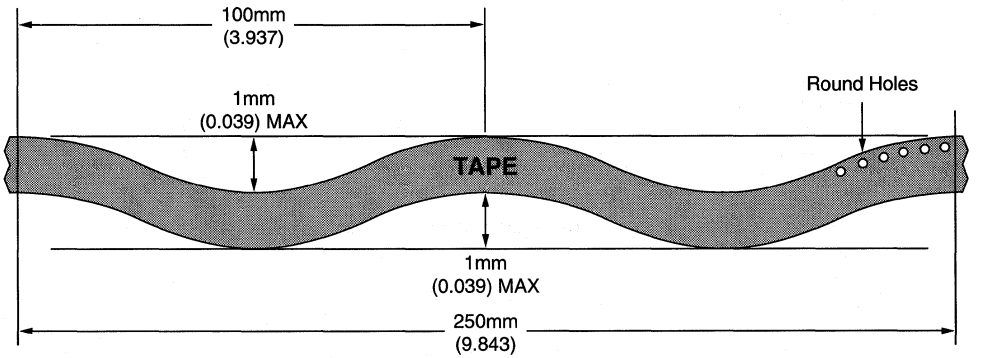


Figure 2
BENDING RADIUS



Allowable camber to be 1mm/100mm nonaccumulative over 250mm.

Figure 3
CAMBER
(top view)

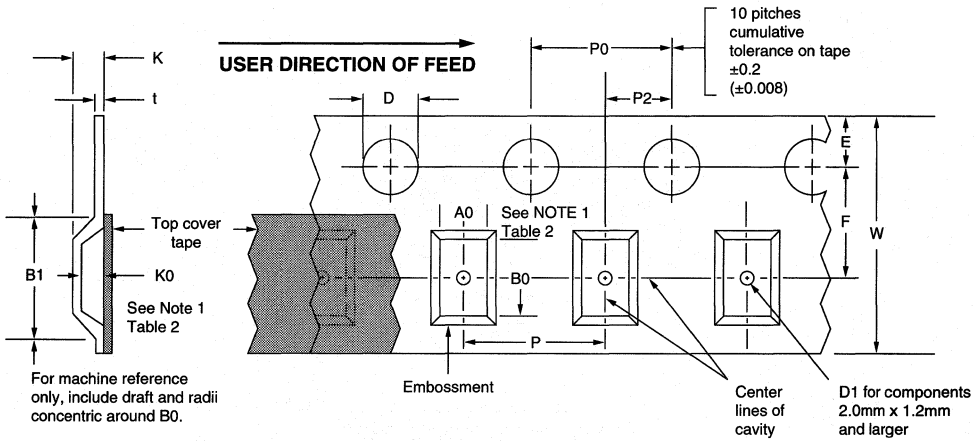


Figure 4
EMBOSSED CARRIER DIMENSIONS
(24mm tape only)

Table 2
24mm EMBOSSED TAPE DIMENSIONS [3]

TAPE SIZE	D	E	P0	t (MAX)	A0, B0, K0
24mm	1.5 $^{+0.10}_{-0.00}$ (0.59) $^{+0.004}_{-0.000}$	1.75 (0.069 ±0.004)	4 (0.157 ±0.004)	0.400 (0.16)	Note 1

TAPE SIZE	B1 (MAX)	D1 (MIN)	F	K (MAX)	P2	R (MIN)	W
24mm	20.1 (0.791)	1.5 (0.059)	11.5 ±0.10 (0.453 ±0.004)	6.5 (0.256)	2 ±0.10 (0.079 ±0.004)	50 (1.969)	24 ±0.30 (0.945 ±0.012)

TAPE SIZE	P					
	4 ±0.10 (0.157 ±0.004)	8 ±0.10 (0.315 ±0.004)	12 ±0.10 (0.472 ±0.004)	16 ±0.10 (0.630 ±0.004)	20 ±0.10 (0.787 ±0.004)	24 ±0.10 (0.945 ±0.004)
24mm			x	x	x	x

NOTE:
1. A0, B0 and K0 are determined by component size. The clearance between the component and the cavity must be within 0.05 (0.002) MIN to 1.00 (0.039) MAX for 24mm tape. The component cannot rotate more than 20° within the determined cavity.
2. Tape and components shall pass around radius "R" without damage.
3. All dimensions in millimeters, (inches).

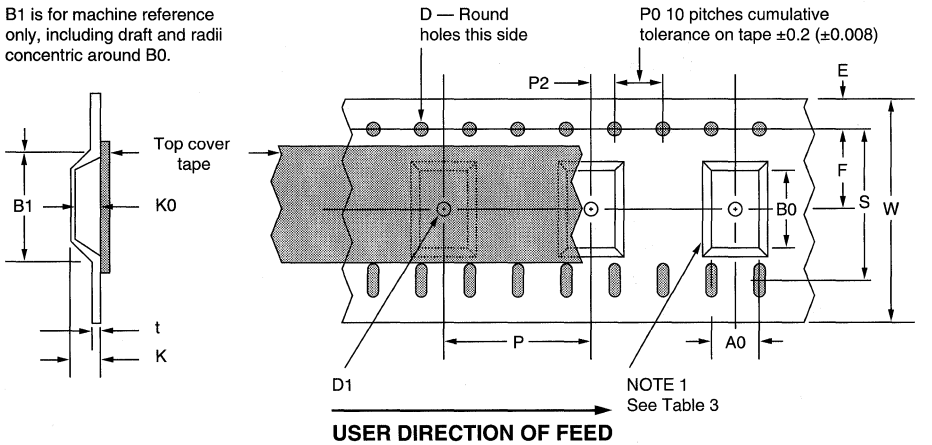


Figure 5
EMBOSSED CARRIER DIMENSIONS
(32 and 44mm tape only)

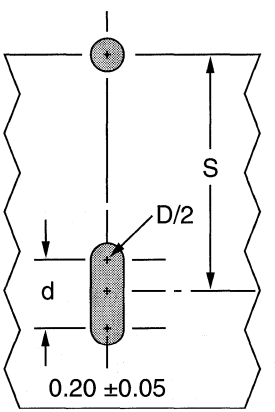


Figure 6
DETAIL ELONGATED HOLE

Table 3
32 AND 44mm EMBOSSED TAPE [3]

TAPE SIZE	D	D1 (MIN)	E	K (MAX)	P0	t (MAX)	A0, B0, K0
32 and 44mm	1.5 $^{+0.10}_{+0.00}$ (0.059) $^{+0.004}_{+0.000}$	2 (0.079)	1.75 ±0.10 (0.069 ±0.004)	10 (0.394)	4 ±0.10 (0.156 ±0.004)	0.500 (0.20)	NOTE 1

TAPE SIZE	B1 (MAX)	F	P2	S	W	R (MIN)
32mm	23 (0.906)	14.2 ±0.10 (0.559 ±0.004)	2 ±0.10 (0.079 ±0.004)	28.4 ±0.10 (1.118 ±0.004)	32 ±0.30 (1.26 ±0.012)	50 (1.973)
44mm	35 (1.378)	20.2 ±0.15 (0.795 ±0.006)	2 ±0.15 (0.079 ±0.006)	40.4 ±0.10 (1.591 ±0.004)	44.8 ±0.30 (1.732 ±0.12)	50 (1.973)

TAPE SIZE	P							
	16 ±0.10 (0.630 ±0.004)	20 ±0.10 (0.787 ±0.004)	24 ±0.10 (0.945 ±0.004)	28 ±0.10 (1.102 ±0.004)	32 ±0.10 (1.26 ±0.004)	36 ±0.10 (1.417 ±0.004)	40 ±0.10 (1.575 ±0.004)	44 ±0.10 (1.732 ±0.004)
32mm	x	x	x	x	x			
44mm			x	x	x	x	x	x

NOTE:
1. A0, B0 and K0 are determined by component size. The clearance between the component and the cavity must be within 0.05 (0.002) MIN to 1.00 (0.039) MAX for 24mm tape. The component cannot rotate more than 20° within the determined cavity.
2. Tape and components shall pass around radius "R" without damage.
3. All dimensions in millimeters (inches).

TECHNICAL NOTE

SRAM BUS CONTENTION DESIGN CONSIDERATIONS

INTRODUCTION

High-speed SRAM memory systems normally share a common data bus with other memory devices, processors and memory management or caching devices. All of these devices are required to control the data bus at one time or another. Turning off a device that is driving the bus before a new device takes control of the bus can be a difficult design problem when these systems are operating at minimum cycle times.

When two or more devices are driving the bus at the same time, a conflict known as "bus contention" occurs. This technical note discusses bus contention design issues and points out design features of Micron's fast SRAMs that help minimize bus contention problems.

BUS CONTENTION EFFECTS

System-design problems caused by bus contention are difficult to analyze. The effects are transient, normally not longer than 5ns. The most visible result of bus contention is observed as noise on power-supply lines and data lines connecting the contending devices. While these conflicts are not destructive, they potentially reduce long-term system reliability. However, in most cases, they do not affect system performance when all the active components are MOS.

MOS devices are inherently self-current limiting. As the current through a MOS transistor increases, the transistor heats up and its gain decreases. Bipolar transistors have the opposite behavior. When a bipolar transistor's temperature

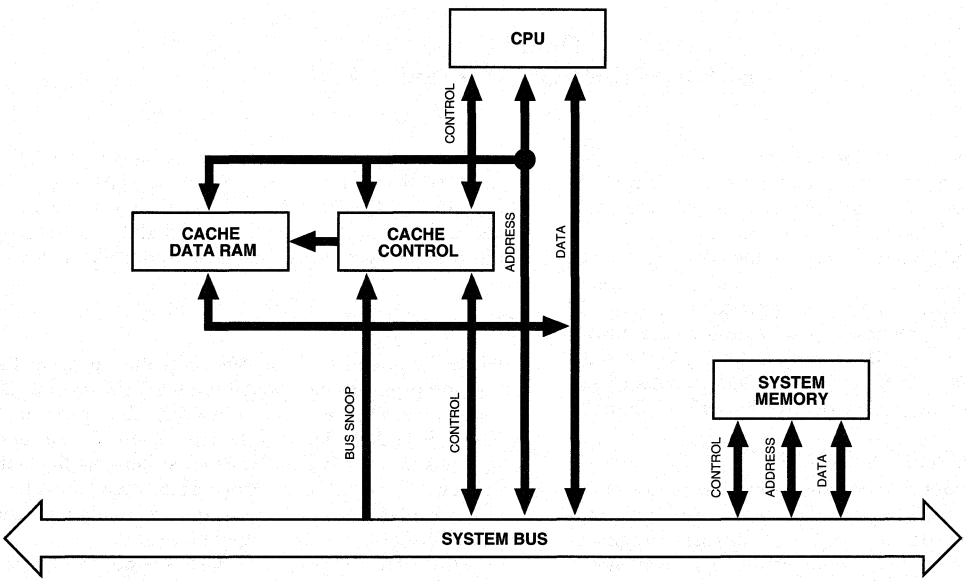


Figure 1
BLOCK DIAGRAM OF A CACHE MEMORY SYSTEM

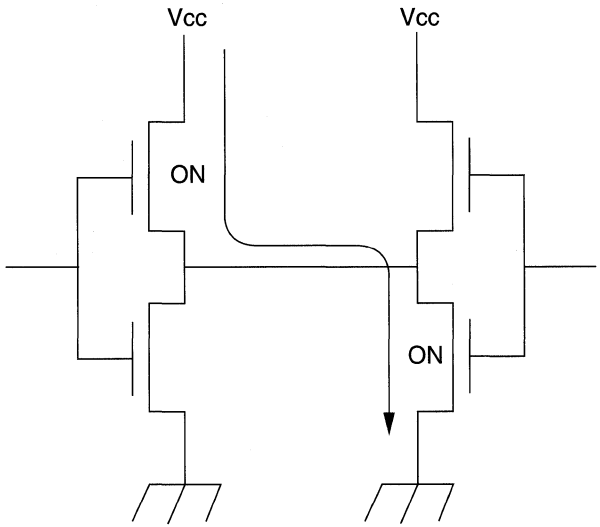


Figure 2
BUS CONTENTION CURRENT PATH

is elevated, the gain of the device increases, making it possible for the current through the transistor to increase to a destructive level. This phenomenon is known as "thermal runaway." If CMOS SRAMs share any data lines with bipolar or BiCMOS output devices, the system should be designed to eliminate any possibility of bus contention.

Figure 2 is a schematic diagram of two contending SRAM output buffers. A high current path has been created by two SRAM output buffers. The current is flowing between the "on" transistor connected to Vcc in the buffer on the left and the transistor connected to ground in the buffer on the right.

SRAM SPECIFICATIONS

The critical parameter for calculating the amount of bus contention for a high-speed SRAM system design is the time it takes for a device to go to low impedance (logic 1 or 0) on its output versus the time required for a contending output to go to high impedance. A typical SRAM has three control signals: chip enable (CE), write enable (WE) and output enable (OE). ^{t}LZCE, ^{t}LZWE and ^{t}LZOE are the times it takes for the outputs to become active or low impedance upon the assertion of CE, WE and OE. ^{t}HZCE, ^{t}HZWE and ^{t}HZOE are the times required for the outputs to become inactive or high impedance after CE, WE and OE are removed. These times are shown in the READ and WRITE cycle timing diagram (Figure 3). A preliminary review of a fast SRAM data sheet would imply that the worst case for bus contention could be calculated from the equation:

$$^{t}C = {}^{t}HZ\ (MAX) - {}^{t}LZ\ (MIN)$$

where ^{t}C is equal to the bus-contention overlap time. For an output enable change in an SRAM rated at 20ns access time, ^{t}HZWE = 7ns and ^{t}LZWE = 2ns; therefore ^{t}C = 5ns. If this calculation is correct, there would be a serious bus contention problem. Thus, for a system running with a 20ns cycle, almost 25 percent of the total cycle would be lost to bus contention and there would be a large increase in power dissipation in the output buffers.

Fortunately, the previous analysis is not valid because ^{t}HZWE is a MAX parameter and ^{t}LZWE is a MIN parameter. ^{t}HZWE maximum occurs under completely different test conditions than ^{t}LZWE minimum. ^{t}HZWE maximum is worst-case at the highest operating temperature and the lowest power-supply voltage. On a commercial data sheet, this would be at 70° C and 4.5V. ^{t}LZWE minimum is

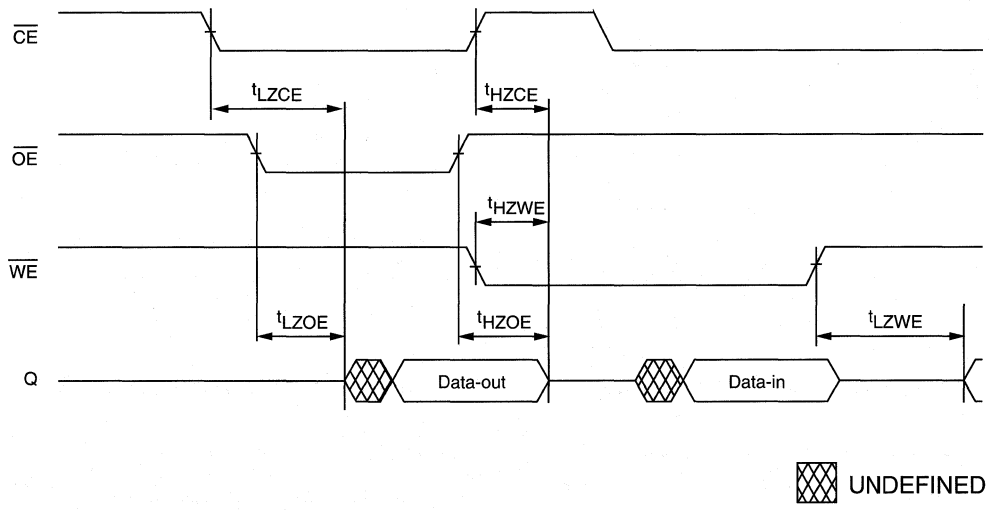


Figure 3
READ AND WRITE CYCLE TIMING

specified at the lowest operating temperature and the highest voltage. Again, on the commercial data sheet, this would be 0° C and 5.5V. It is not possible for two SRAMs on the same board to be at such diverse temperatures and voltages. Micron devices are designed to turn-off faster than they turn-on under the same voltage/temperature conditions.

This means Micron fast SRAMs have been designed so that at any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE and ^{t}HZWE is less than ^{t}LZWE. Since the devices will normally be mounted on the same board, the bus contention associated with the SRAM control signals has been eliminated.

Care must be taken when multiple vendors' SRAMs share the bus. An analysis of the output turn-off time must be done under the same operating and temperature conditions to insure that bus contention between the devices is minimized.

EXAMPLE DATA

As an example, Figures 4 to 9 shows actual ^{t}HZCE and ^{t}LZCE data taken from an 8ns and 10ns 64K SRAM. Note that the SRAM always turns off much faster than it turns on.

Figure 4 - 8ns 64K SRAM (0°C)

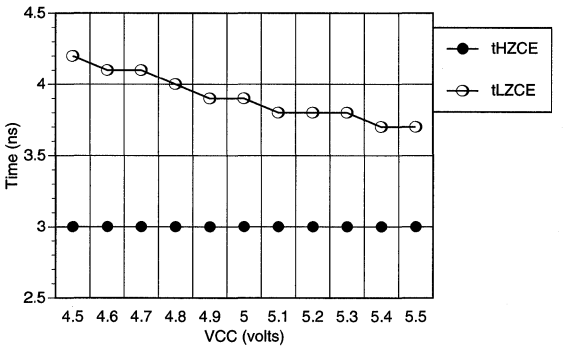


Figure 5 - 8ns 64K SRAM (25°C)

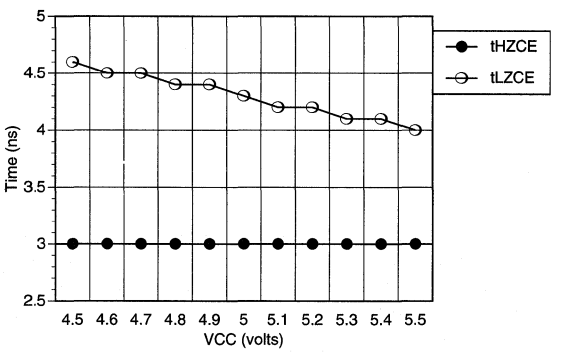


Figure 6 - 8ns 64K SRAM (70°C)

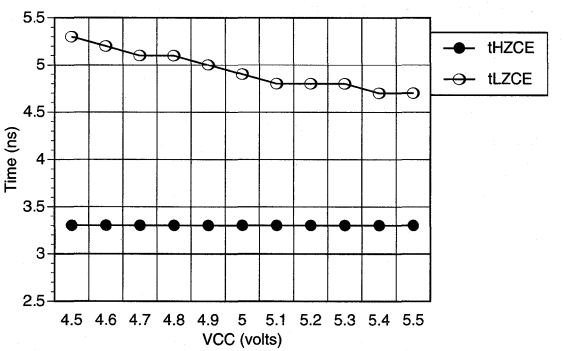


Figure 7 - 10ns 64K SRAM (0°C)

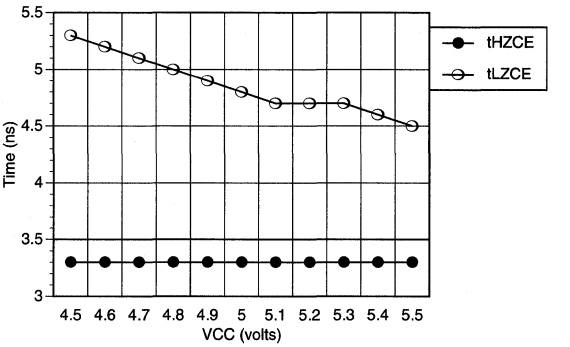


Figure 8 - 10ns 64K SRAM (25°C)

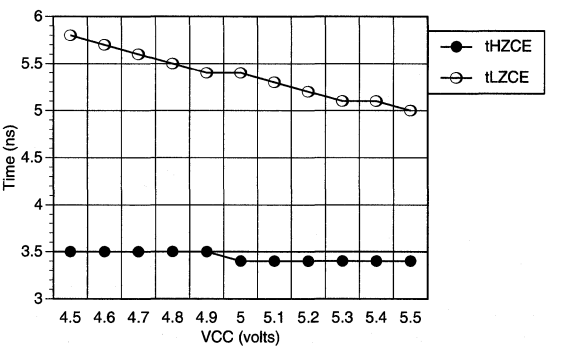
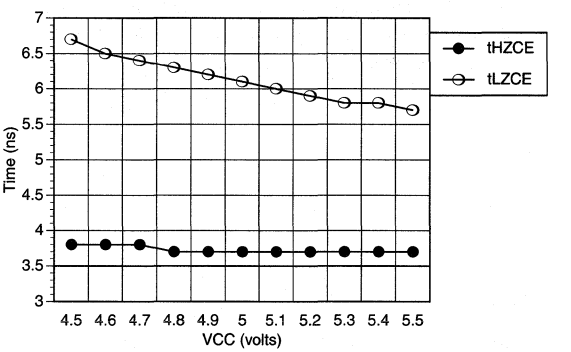


Figure 9 - 10ns 64K SRAM (70°C)



TECHNICAL NOTE

SRAM CAPACITIVE LOADING

INTRODUCTION

Many high-speed 16-bit and 32-bit microprocessor systems require fast SRAMs. SRAMs are used either in main memory or caching subsystems. In either case, the SRAMs are typically required to interface with a system bus that is shared by one or more microprocessors, several I/O devices and other types of memory (ROM, EPROM, etc.).

Even though transceivers and/or buffers interface with the actual bus, SRAMs are typically required to drive loads larger than what is specified in the data sheet timing parameters. Hence, the access time must be derated to reflect the actual performance of the SRAM under these circumstances.

SIMILARITY BETWEEN SRAM FAMILIES

Micron's 16K, 64K, 256K and 1 Meg 5.0V SRAM families all have the same size output transistors and output architecture. Hence, all devices will have the same drive characteristics. The actual data presented in this technical note are derived from the 256K SRAM family.

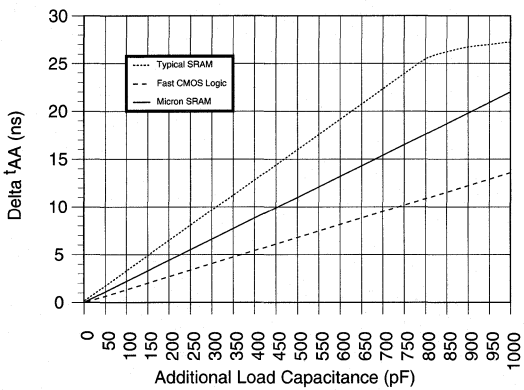


Figure 1
INCREASED ACCESS TIME vs ADDITIONAL OUTPUT LOADING

COMPARISON OF DEVICES

Figure 1 compares the effects of capacitive loading on the Micron SRAM family with SRAMs from a typical memory supplier and discrete CMOS logic, designed to drive heavy loads. The graph illustrates the additional access time required to drive various capacitive loads.

As expected, the Micron SRAM family does not drive heavy loads as well as the discrete CMOS logic, but does drive faster than the typical SRAM from other suppliers.

The graph line representing the Micron SRAM family is based on data gathered on the Micron 256K SRAM. Access time measurements were taken with the SRAM subjected to various capacitive loads. In the range covered, the change in access time was seen to be a linear function of the capacitive load. The following equation may be used to determine the access time required for a specific load.

$$T_{AA}(\text{actual}) = T_{AA}(\text{data sheet}) + T_{AA}(\text{additional})$$

$$T_{AA}(\text{additional})\ (\text{ns}) = .022\ (\text{ns/pF})\ C_a$$

This applies where C_a is the additional capacitive load expressed in picofarads (pF). For example, the access time needed for a 100pF total capacitive load is:

T_{AA}(actual) = 20ns + T_{AA}(additional) =
20ns + .022 * (total load - rated load) =
20ns + .022ns/pF * (100pF - 30pF) =
20ns + 1.5ns = 21.5ns

SUMMARY

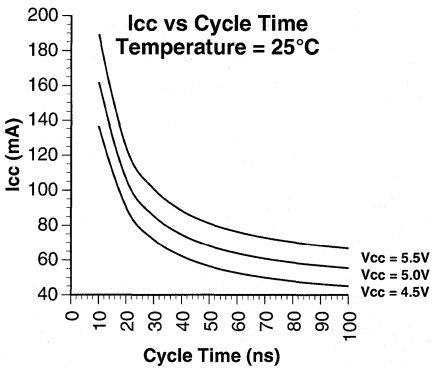
The SRAM timing specifications of all major vendors are based upon an industry standard capacitive load of 30pF. In most applications, the SRAMs are required to drive much larger capacitive loads. In addition, today's designs are implemented around higher frequencies. This requires the system timing to be more precise; hence, loading becomes a more important issue. Understanding how the SRAM will perform under specific loading conditions may result in a more reliable design.

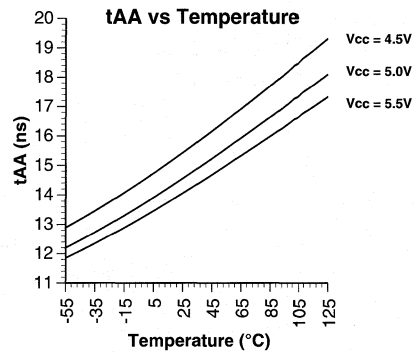
TECHNICAL NOTE

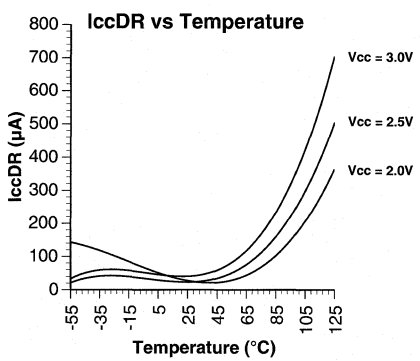
1 MEG FAST SRAM TYPICAL OPERATING CURVES

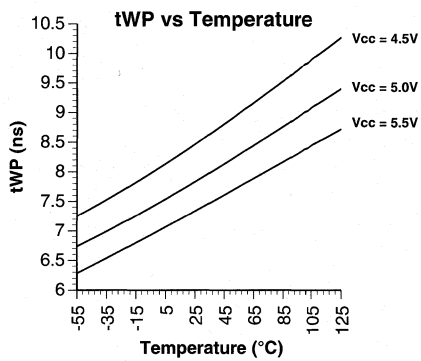
INTRODUCTION

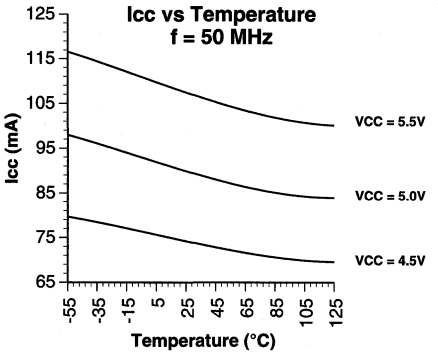
These curves represent the typical operating characteristics of Micron's 1 Meg, 20ns SRAM. They may be used to calculate the typical operating parameters of a memory system. For worst-case design limits, the system designer should refer to the individual data sheets in the SRAM section of this data book.

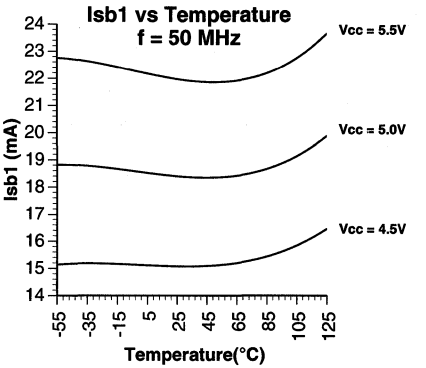


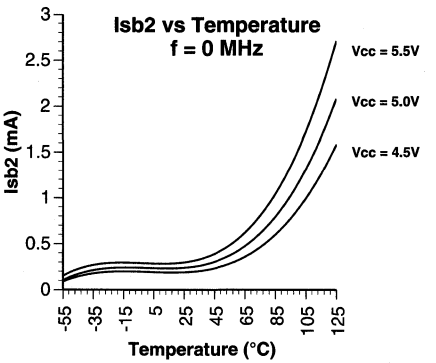












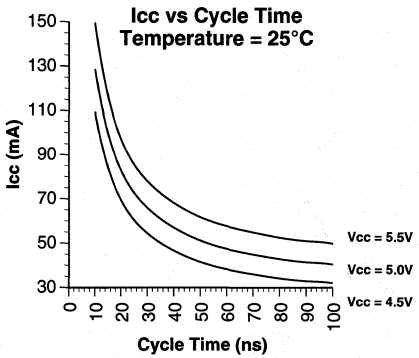
TECHNICAL NOTE

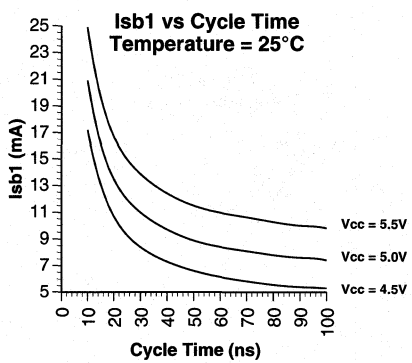
TECHNICAL NOTE

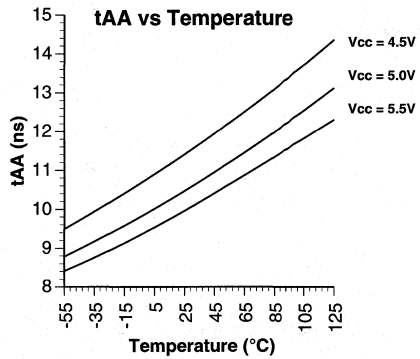
256K FAST SRAM TYPICAL OPERATING CURVES

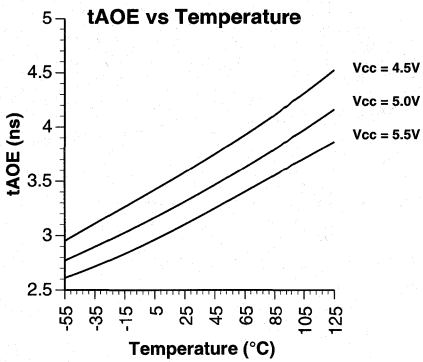
INTRODUCTION

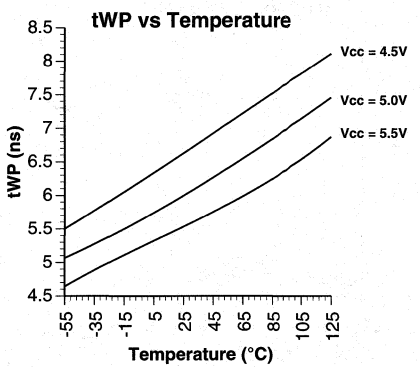
These curves represent the typical operating characteristics of Micron's 256K, 15ns SRAM and 20ns low power (LP) SRAM. They may be used to calculate the typical operating parameters of a memory system. For worst-case design limits, the system designer should refer to the individual data sheets in the SRAM section of this data book.

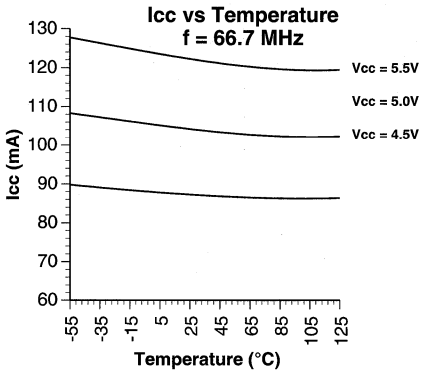


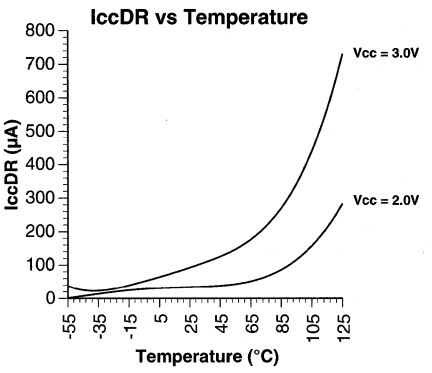


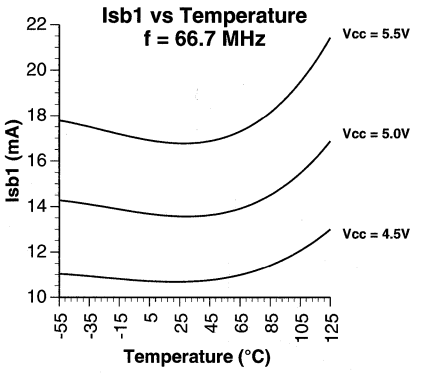


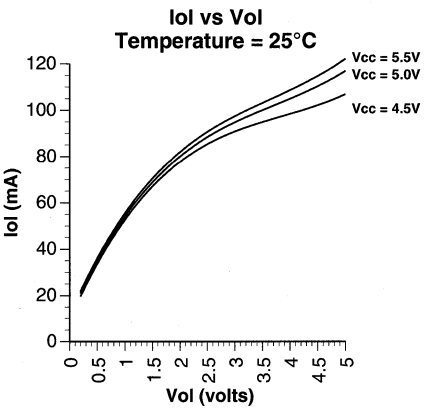


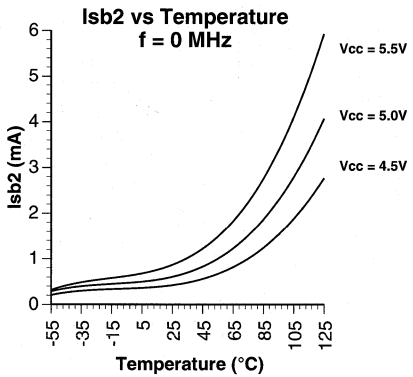


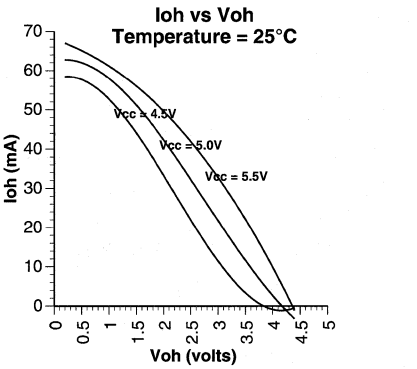


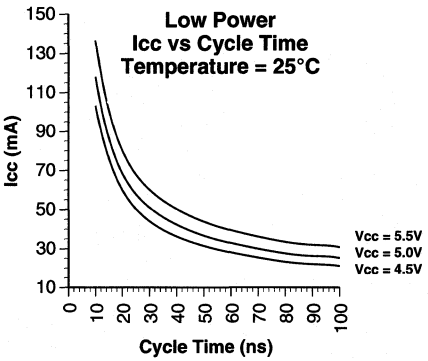


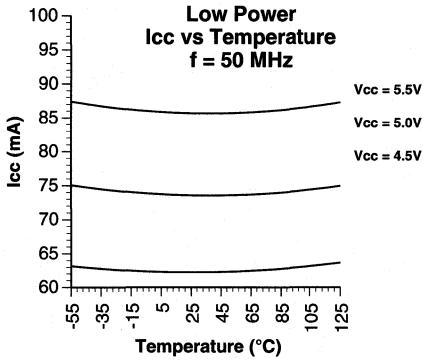


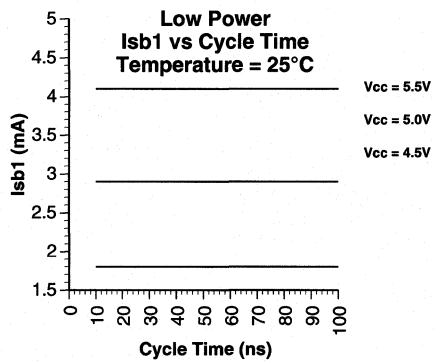


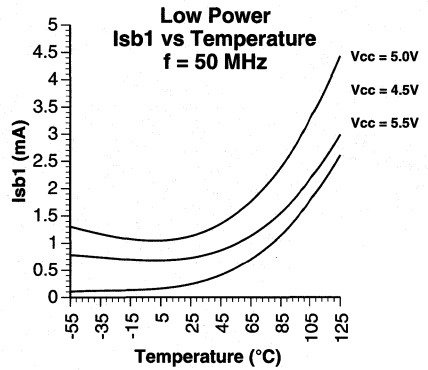












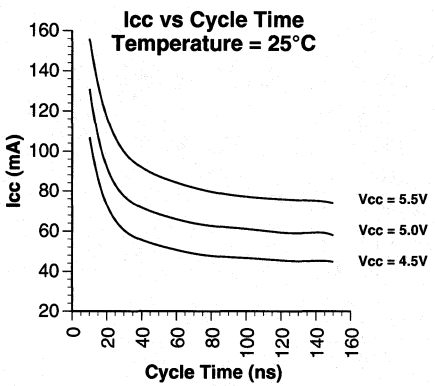
TECHNICAL NOTE

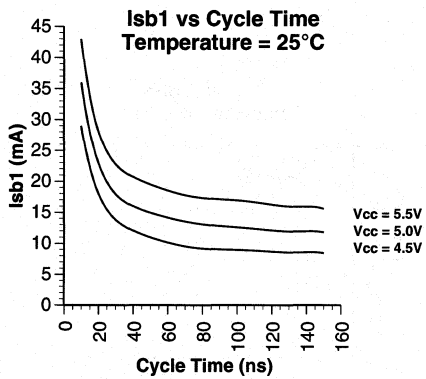
TECHNICAL NOTE

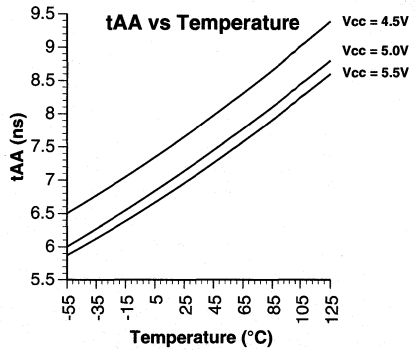
64K FAST SRAM TYPICAL OPERATING CURVES

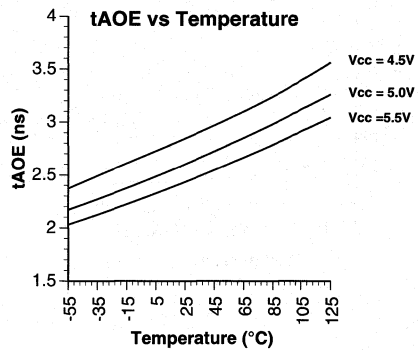
INTRODUCTION

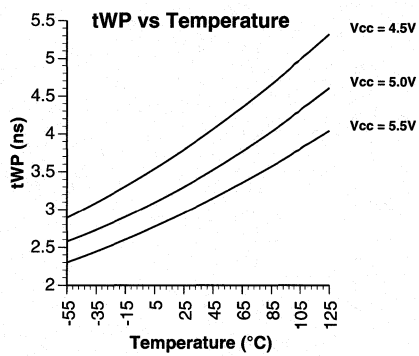
These curves represent the typical operating characteristics of Micron's 64K, 10ns SRAM. They may be used to calculate the typical operating parameters of a memory system. For worst-case design limits, the system designer should refer to the individual data sheets in the SRAM section of this data book.

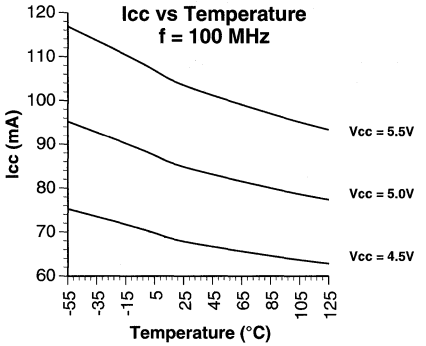


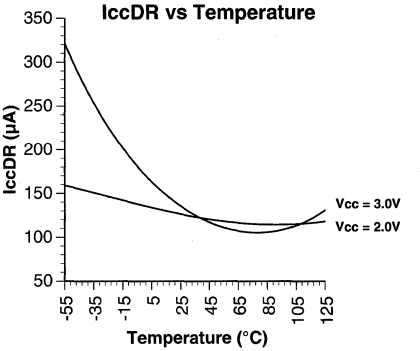


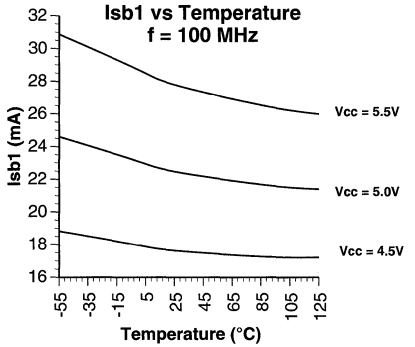


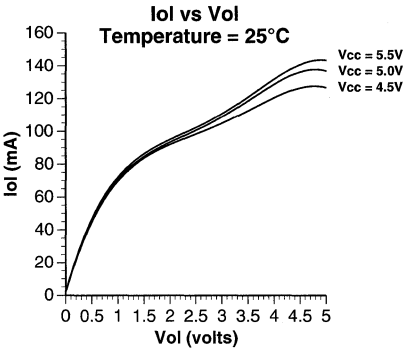


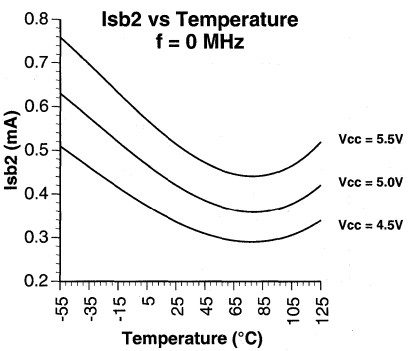


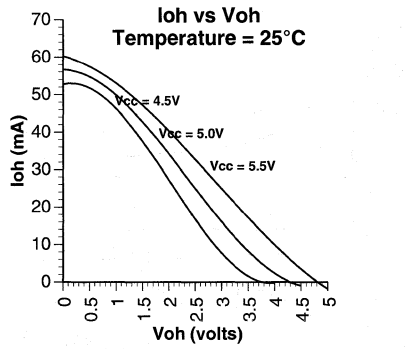












TECHNICAL NOTE

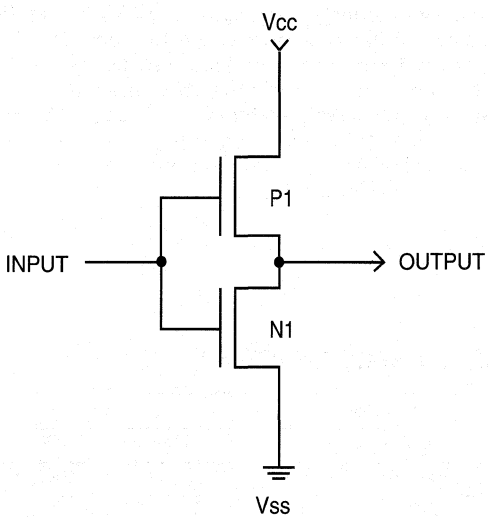
1 MEG LOW-POWER SRAMs

INTRODUCTION

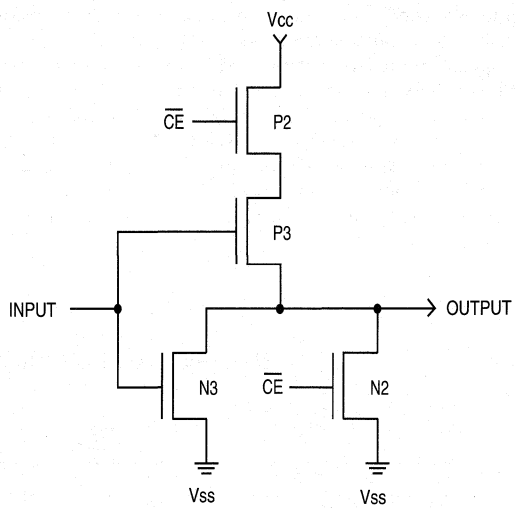
By using the low-power versions of the Micron 1 Meg SRAM family (MT5C100X LP), designers can reduce both operating power consumption and battery back-up power consumption in their systems. This technical note describes the physical differences between the low-power versions and the standard versions of the 1 Meg SRAM and how these differences affect the various current consumption specifications for the devices. The note then discusses the system-level benefits of low-power parts.

LOW-POWER vs STANDARD VERSIONS

The primary difference between the low-power versions and the standard versions of the 1 Meg SRAM is that the low-power versions contain gated inputs on the write enable ($\overline{WE}$), output enable ($\overline{OE}$) and address inputs. The difference between gated and non-gated inputs is shown in Figure 1. In the non-gated input buffer, current will flow from V_{CC} to V_{SS} when both transistors are conducting (i.e. when the input is switching or is sitting at a level between V_{CC} and V_{SS}). Current flow is at a minimum when the input is held at either the V_{CC} or V_{SS} level. In the gated input buffer, $\overline{CE}$ is an internal chip enable signal derived from the chip enable pin(s) of the device. When the chip is selected, $\overline{CE}$ is LOW, P2 is ON and N2 is OFF. Operation in this mode is similar to the non-gated input buffer. When the chip is deselected, $\overline{CE}$ is HIGH, N2 is ON and P2 is OFF. In this case, both the logical operation of the buffer and the flow-through current are independent of the voltage level at the



NON-GATED INPUT BUFFER



GATED INPUT BUFFER

Figure 1
NON-GATED vs GATED INPUT BUFFERS

Table 1
OPERATING AND STANDBY CURRENT DEFINITIONS

PARAMETER	MODE	CHIP ENABLE CONDITIONS	INPUT CONDITIONS
I_{CC}	Chip Selected	$\overline{CE} \le V_{IL}$	switching at MAX frequency
I_{SB1} (Standard)	Chip Deselected	$\overline{CE} \ge V_{IH}$	switching at MAX frequency
I_{SB1} (Low-Power)	Chip Deselected	$\overline{CE} \ge V_{IH}$	static or switching
I_{SB2} (Standard)	Chip Deselected	$\overline{CE} \ge (V_{CC} - 0.2V)$	static
I_{SB2} (Low-Power)	Chip Deselected	$\overline{CE} \ge (V_{CC} - 0.2V)$ Chip enable input	static or switching Write enable

input node. The output of the buffer is LOW because N2 is ON, and virtually no current flows from V_{CC} to V_{SS}, because the gate of P2 is held at the V_{CC} level.

Another difference from the standard versions found in the low-power versions is a process enhancement designed to reduce the current consumed by the memory cells under quiescent conditions. This means that the standby current attributed to the memory array is reduced.

Specifications are summarized in Table 1 to help illustrate the effects of these differences on the various current consumption specifications of the parts. The values for these parameters are shown in Table 2. Note that I_{SB1} and I_{SB2} are substantially reduced in the low-power version while I_{CC} remains the same. The I_{SB1} (MAX) limit is reduced by 90 percent, primarily through the use of gated inputs, and the I_{SB2} (MAX) limit is reduced by 70 percent due to the process enhancements. Icc is not affected by these changes because it is measured when the chip is selected and the memory array is being accessed.

Another way of looking at the effects of these changes on I_{SB1} and I_{SB2} for the low-power version is to note that the specified values for I_{SB1} approach the values for I_{SB2}. The remaining difference between the I_{SB1} and I_{SB2} values represents the amount of current consumed by the chip enable input buffers themselves. By definition, I_{SB1} is measured with the chip enable inputs at V_{IH} (MIN) or V_{IL} (MAX) levels. This causes more current to flow than if the inputs were within 0.2 volts of V_{CC} or V_{SS} levels, as is the case when measuring I_{SB2}.

Table 2
OPERATING AND STANDBY CURRENT SPECIFICATIONS

DEVICE VERSION	I_{CC}*		I_{SB1}		I_{SB2}	
	MAX	TYP	MAX	TYP	MAX	TYP
Standard	125 mA	95 mA	30 mA*	17 mA	5 mA	400 uA
Low-Power	125 mA	95 mA	3 mA	1.3 mA	1.5 mA	300 uA

* Specified at 40 MHz
Typical values are measured at V_{CC} = 5.0V and T_A = 25°C

SYSTEM-LEVEL BENEFITS

The system-level benefits can be seen by examining two different modes of system operation. First, consider a system containing several banks of SRAMs where, in an effort to minimize operating current, only one bank will be selected at any given time during normal operation. While the active bank is being accessed, the address and control signals being switched appear on the inputs of SRAMs in all banks. This causes current consumption by input buffers in standard parts. When using low-power parts, the power consumption in the deselected banks will be reduced to one-tenth of the value for standard parts. This reduces the overall operating power consumption of the system. Next, consider a system with a battery back-up mode requiring data retention in the SRAMs while the devices that interface with the SRAMs are completely powered down. In addition to a 70 percent reduction in battery back-up power consumption, the low-power SRAMs facilitate the system design. When using standard devices, designers must take precautions to ensure that all the address and control inputs are taken to within 0.2 volts of V_{CC} or V_{SS}, while taking care to avoid powering-up other devices in the system. With the low-power devices, only the chip enable inputs need to be taken to these levels—the $\overline{WE}$, $\overline{OE}$ and address inputs may then be driven to, or allowed to assume, any value between V_{CC} and V_{SS}.

SUMMARY

The low-power versions of the Micron 1 Meg SRAMs offer a 90 percent reduction in TTL standby current and a 70 percent reduction in CMOS standby current. These reductions in component standby current lead to reductions in both operating power and battery back-up power consumption at the system level, while at the same time facilitating system design.

TECHNICAL NOTE

SRAM THERMAL DESIGN CONSIDERATIONS

INTRODUCTION

As operating frequencies increase, memory components must dissipate more power to satisfy the needed reduction in permissible access time. SRAM thermal design considerations become increasingly important as power consumption approaches the package power dissipation limit. This technical note separately addresses thermal performance of Micron packaged SRAMs and SRAM die. Contact the factory for thermal information on any package not listed in this note.

DEFINITIONS

T_A = ambient air temperature (°C) at which the device is operated. The ambient temperature range of a device is listed under the "Electrical Characteristics and Recommended DC Operating Conditions" section of each SRAM data sheet. Commercial temperature range is 0°C to 70°C, industrial temperature range is -40°C to 85°C, automotive temperature range is -40°C to 125°C and extended and military temperature range is -55°C to 125°C.

T_C = case temperature of the device (°C). In a packaged part this is the surface temperature at a point on the device package.

T_J = junction temperature of the active portion of the silicon die (°C). The maximum recommended junction temperature of Micron SRAMs is 150°C to achieve good long-term reliability. All Micron SRAMs are tested for high temperature operating life (HTOL) at 125°C ambient and 6V. Under HTOL conditions, the failure rate of a 1 Meg SRAM is 484 FITs compared with 5 FITs at 50°C ambient and 5V. The device will operate with junction temperatures in excess of 150°C but much higher failure rates should be expected. Since the limiting factor in plastic components is the plastic mold compound, 155°C should never be exceeded anywhere in the plastic body.

P = average device power dissipation. Device power is dependent upon the operating conditions. SRAM data sheets indicate maximum I_{CC} values that incorporate significant guardband (margin to guard against process changes, tester skew, etc.). Device power should be calculated to reflect the actual junction temperature, supply voltage, operating frequency and output loading conditions.

θ_{JC} = junction to case thermal resistance (°C/W). In a die-level product, the case is considered to be the surface of the die which is bonded to the hybrid substrate. θ_{JC} is a function of the die thickness, area, and number of bonds. In a packaged component, θ_{JC} is larger due to the extra thermal resistance of the package material thickness.

θ_{CA} = case to ambient thermal resistance (°C/W). In a die-level product, this is comprised of the θ_{CA} of the hybrid substrate plus packaging around the substrate if applicable. In a packaged component, this is a function of the surface area of the component (for convection and radiation) and the amount of heat conduction through the device leads. In applications where a heat sink is attached to the device, θ_{CA} is expressed as $\theta_{CS} + \theta_{SA}$ where θ_{CS} is the case to heat sink thermal resistance and θ_{SA} is the heat sink to ambient thermal resistance. θ_{CS} is normally very small, typically 0.3° C/W. θ_{SA} is mostly dependent upon the surface area of the heat sink. Under most circumstances, Micron SRAMs do not require heat sinks for reliable long-term operation.

θ_{JA} = junction to ambient thermal resistance. This is the sum of $\theta_{JC} + \theta_{CA}$.

Given the above parameters, T_J may be calculated using the following equation:

$$T_J = T_A + P(\theta_{JC} + \theta_{CA})$$
$$= T_A + P\theta_{JA}.$$

DETERMINING THERMAL RESISTANCES

The reliability monitors published for each component family details the procedure used to determine thermal impedances. The procedure is summarized as follows: θ_{JC} is determined by inserting the IC package into a socket assembly with a thermocouple glued to the top side of the package to measure the case temperature. The contact area is minimized so that the thermocouple does not act as a significant additional heat sink. θ_{JA} is measured with the IC package inserted into the same socket assembly but suspended inside a one-cubic-foot closed container that provides a still-air environment. The junction temperature

is measured by characterizing the IC's input pin to substrate diode at various temperatures. θ_{JA} and θ_{JC} are determined using linear regression analysis on the data gathered. Characterization data generally indicates a 99.0% correlation to a linear curve fit.

The above discussion accounts for the determination of packaged component thermal properties. In actual applications, θ_{JA} is lower because printed circuit board traces conduct heat away from the package more efficiently than the test socket. θ_{JC} is essentially a constant, therefore the user may determine the actual θ_{JA} by calculating θ_{CA}. This can be done by measuring the average device power, ambient air temperature and package surface temperature of the SRAM soldered in circuit and calculating as follows:

$$\theta_{CA} = (T_C - T_A)/P.$$

θ_{JA} is simply the sum of the calculated θ_{CA} and the supplied θ_{JC}.

Table 1 summarizes the thermal resistances of Micron plastic package SRAMs rounded to two significant figures.

Table 1
PLASTIC SRAM THERMAL RESISTANCE

Device	Package Pins	Width (mils)	Type	θ_{JC} °C/W	θ_{CA} °C/W	θ_{JA} °C/W
64K x 1	22	300	PDIP	14	64	78
16K x 4	24	300	PDIP	8.4	61	70
8K x 8	28	300	PDIP	7.8	46	54
16K x 4	24	300	PSOJ	10	79	90
8K x 8	28	300	PSOJ	9.4	84	93
256K x 1	24	300	PDIP	18	55	73
64K x 4	24	300	PDIP	18	53	71
32K x 8	28	300	PDIP	10	56	66
256K x 1	24	300	PSOJ	19	71	90
64K x 4	24	300	PSOJ	14	72	86
32K x 8	28	300	PSOJ	11	71	82
64K x 4	24	300	SOIC	3.1	77	80
1 Meg x 1	28	400	PDIP	5.9	50	56
128K x 8	32	400	PDIP	5.3	50	56
128K x 8	32	600	PDIP	4.5	38	43
1 Meg x 1	28	400	PSOJ	4.4	62	66
128K x 8	32	400	PSOJ	3.0	55	58
128K x 9	32	400	PSOJ	3.5	56	59

TRUE SRAM POWER

SRAM power is determined by accounting for three components: power dissipation of internal operations, power dissipation due to transient output current (AC load current) and power dissipation due to steady state output current (DC load current). Data sheets generally contain worst-case numbers which, for I_{CC}, occur at the fastest cycle time, coldest ambient temperature and highest voltage. Device data for specific operating voltages, temperatures and frequencies can be obtained from Micron, generally in the Reliability Monitors.

The following is a derivation from first principles, hopefully putting the issue to rest concerning how to calculate the extra power due to AC output load current:

$$P_L = \frac{1}{T}\int_0^T v\,i\,dt.$$

$$P_L = \frac{1}{T}\int_0^T (Vcc - V_L)\,I_L\,dt \text{ for LOW to HIGH case.}$$

$$P_L = \frac{1}{T}\int_0^T (V_L)\,I_L\,dt \text{ for HIGH to LOW case.}$$

Solving for the LOW to HIGH case (substituting $I_L = C\frac{dV_L}{dt}$):

$$P_L = \frac{1}{T}\int_{VOL}^{VOH} (Vcc - V_L)\,C_L\,dV_L$$

$$= \frac{C_L}{T}\left(Vcc\,V_L - 0.5\,V_L^2\right)\Big|_{VOL}^{VOH}$$

$$= \frac{C_L}{T}\left(Vcc\,[VOH - VOL] - 0.5\,[VOH^2 - VOL^2]\right).$$

Solving for the HIGH to LOW case:

$$P_L = \frac{1}{T}\int_{VOL}^{VOH} V_L\,C_L\,dV_L$$

$$= \frac{C_L}{T}\left(0.5\,V_L^2\right)\Big|_{VOL}^{VOH}$$

$$= \frac{C_L}{T}\left(0.5\,[VOH^2 - VOL^2]\right)$$

where: C_L is the load capacitance.
V_{OH} is the highest load voltage during the cycle.
V_{OL} is the lowest load voltage during the cycle.
I_L is the load current resulting from C_L.
T is the device cycle time.
P_L is the power dissipation in the SRAM due to the output current on one DQ line.

These solutions make one important assumption: the output voltage waveform has no overshoot/undershoot. The presence of either overshoot or undershoot increases the SRAM power dissipation. True SRAM power for Micron synchronous devices is therefore:

$$P = Vcc\ I_{CC} + \Sigma\ P_{L\ (\text{for all output changes})}.$$

The marginal power due to steady-state current flow into or out of the DQ pins (due to I/O leakage of connected devices) is ignored in the above equation because it is insignificant in most new design work. That extra power would be:

$$(Vcc - V_{OH})\ I_O\ N_H + V_{OL}\ I_I\ N_L,$$

where V_{OH} is the logic HIGH output voltage, I_O is output current on those DQ lines and N_H is the number of DQ lines that are HIGH; V_{OL} is the actual logic LOW voltage, I_I is the resulting input current into the DQ line and N_L is the number of DQ lines that are LOW. Almost all CMOS devices have I_I or I_O less than 10uA (often 1 or 2uA), hence this calculation is inconsequential. If devices with high input currents are connected to the DQ lines, do not ignore this additional power component. For example, take the case where eight outputs are connected to loads having 10uA of leakage. The contribution to device power is (given that V_{OH} is 3.8V during the average cycle):

$$(5V - 3.8V)\ 10uA\ (8) = 96uW,$$

which can indeed be ignored. With higher leakage, V_{OH} drops and power increases as a result of both increased current and greater voltage drop in the SRAM output driver.

DESIGN EXAMPLE

Use of thermal resistance information can be seen in the following example: An MT5C1008DJ-20 SRAM operates at an ambient temperature of 70°C with a 5.5V supply, READ and WRITE cycle times of 25ns (40 MHz), continuous operation in still-air and an output loading of 50pF. The following discussion demonstrates how this thermal resistance information is utilized.

In the *1 Meg SRAM Reliability Monitor*, the typical device current at 25ns cycle time, 5V and 25°C is 94mA. This decreases by 4 percent as temperature increases to 70°C, but increases by 17 percent as Vcc increases to 5.5V (also from the *Reliability Monitor*). The net result is an I_{CC} of approximately 105.6mA. The power is calculated as follows (assuming the worst case, all outputs switch from LOW to HIGH):

$$P = I_{CC}\ Vcc + \frac{C_L}{T}\ (Vcc\ [V_{OH} - V_{OL}] - 0.5\ [V_{OH}^2 - V_{OL}^2])\ x\ 8$$

$$= 0.1056(5.5) + \frac{50E\text{-}12}{25E\text{-}9}\ (5.5[4.3\text{-}0.1] - 0.5\ [4.3^2 - 0.1^2])\ 8$$

$$= 0.581 + 0.222$$

$$= 0.803 \text{ watts.}$$

The V_{OH} used (4.3V) is typical for operation at 5.5V. At 5V and full speed operation, V_{OH} is approximately 3.8V. V_{OL} is typically between 0.1 and 0V.

Given the true operating power of 0.803W, the case and junction temperatures can be predicted as follows:

$$T_C = T_A + P\theta_{CA}$$
$$= 70 + 0.803 \times 55$$
$$= 114.2°C.$$
$$T_J = T_A + P\theta_{JA}$$
$$= 70 + 0.803 \times 58$$
$$= 116.6°C.$$

The calculated junction temperature is below the 150°C recommended limit demonstrating that the operating conditions are acceptable. As previously mentioned, the actual θ_{CA} is lower when the SRAM is soldered in circuit. One can therefore expect lower case temperatures than calculated in this example.

To illustrate this point, the MT56C0818LG dual 4K x 18 cache SRAM was characterized in both still air and circuit. In still air, θ_{JA} was determined to be 100°C/W maximum. θ_{JC} was determined to be 45°C/W maximum. In circuit (2" x 3" circuit board with no ground or power planes), θ_{JA} was found to drop to 70°C/W. This implies that θ_{CA} dropped from 55 to 30°C/W (since $\theta_{CA} = \theta_{JA} - \theta_{JC}$) as a result of the additional conduction through the device leads and the circuit board traces.

IMPROVING THERMAL PERFORMANCE

The motivation for achieving the lowest possible junction temperatures is twofold: most AC timing parameters change adversely as junction temperature increases. This can be seen in any of the SRAM reliability monitors where AC timing specifications versus temperature are plotted.

NEW TECHNICAL NOTE

Another consideration is that component life decreases exponentially as temperature increases. Component life shows a strong correlation to the following equation:

$$t_O = t_N \exp([Ea/k][1/T_O - 1/T_N]),$$

where: t_O is the mean time to failure under the stress operating condition.
t_N is the mean time to failure under normal operating conditions.
Ea is the activation energy of failure modes, the most common one being dielectric defects, 0.3eV.
k is Boltzmann's constant, 8.617×10^{-5} eV/K.
T_N is the normal operating temperature (Kelvin).
T_O is the stress operating temperature (Kelvin).

Several considerations can improve thermal performance. Ground and power planes on a PCB can have a significant effect on conduction and therefore on power dissipation and safe operating temperatures. More power and ground leads on the device package produce greater relief. The addition of a thermal pad under the device with appropriate thermal bonding will also help conduct heat away from the device.

Air flow has a significant effect in reducing component temperatures. Table 3 shows test results for industry standard packages, demonstrating the effective reduction in θ_{CA} as airflow increases (these results have *not* been verified by Micron). For example, a 1 Meg SRAM in plastic SOJ having θ_{CA} of 55°C/W in still air would have a θ_{CA} of approximately 55°C/W x 0.75 or 41°C/W at 200fpm of air flow. The new θ_{JA} is approximately 41 + 3.0 = 44°C/W.

DIE THERMAL CONSIDERATIONS

Die level thermal considerations are more complex for the user to handle because more factors are involved than with factory packaged components. Figure 1 illustrates the thermal interfaces involved in a die application with ceramic substrate. Typical thermal resistances which need to be quantified are: die to adhesive, adhesive to substrate, substrate to lid, lid and/or substrate to ambient. The path is highly dependent upon the multichip module (MCM) construction. Heat radiation from die to lid could be an applicable factor. Thermal vias below the die would significantly reduce the total package thermal resistance and should be modeled appropriately.

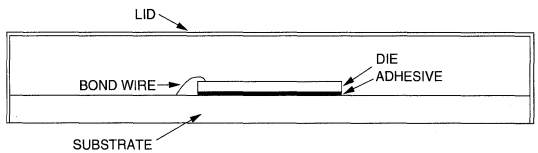


Figure 1
DIE APPLICATION

An application which uses a ceramic substrate can use the θ_{JC} values provided for ceramic SRAMs as a conservative value. This accounts for thermal resistances from die to adhesive (assuming gold eutectic in ceramic packaged parts), adhesive to substrate, and also accounts for the effects of the bond wires. The value is conservative because the thermal resistance through the substrate material of Figure 1 is included, whereas this portion is actually unique to the substrate of each user. Without adjustment, this would be double-counting a portion of the thermal resistance.

Figure 2 illustrates the thermal resistances in a typical die application on silicon substrate. The following discussion uses a silicon substrate die application with four Micron 1 Meg SRAM die mounted on the substrate. The die areas for various Micron SRAM die products are listed in Table 4. Thermal resistance from junction to die backside for the 1 Meg SRAM is calculated as follows:

θ = (0.0185 inch die thickness) / (2.23W/°C/inch)
/ (0.131 sq. inches die area)
= 0.06°C/W.

The remaining thermal resistance values are user-dependent and also dependent upon contact area. Some typical values are: 0.06°C cm^2/W for the die to silicon substrate interface, 0.2°C cm^2/W through the silicon substrate, 0.7°C cm^2/W silicon substrate to module carrier, 0.6°C cm^2/W through the aluminum module carrier, 0.7°C

Table 3
EFFECTS OF AIRFLOW ON θ_{CA}

Package	Air Flow	θ_{CA} Multiplier
PDIP	200 fpm	0.7 - 0.75
PSOJ	200 fpm	0.7 - 0.75
PDIP	500 fpm	0.55 - 0.65
PSOJ	500 fpm	0.55 - 0.65

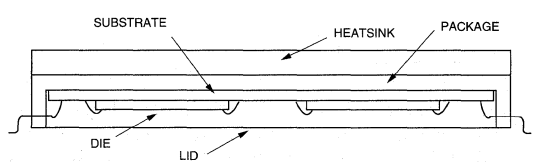


Figure 2
SILICON SUBSTRATE DIE APPLICATION

cm^2/W from module carrier to heat sink and 30°C cm^2/W from heat sink to ambient. For an MCM with 4 SRAMs dissipating the 0.803W of the previous example with 3cm x 3cm dimensions, the calculations would be as follows (assuming 70°C ambient is in still air):

$T_{heat\ sink}$ = 70°C + 30°C cm^2/W / 9cm^2 x 0.803 W x 4
= 80.71°C.

$T_{module\ carrier}$ = 80.71°C + (0.6+0.7°C cm^2/W)/ 9cm^2 x 0.803 W x 4
= 81.17°C.

$T_{silicon\ substrate}$ = 81.17°C + (0.2+0.7°C cm^2/W)/ 9cm^2 x 0.803 W x 4
= 81.49°C.

$T_{junction}$ = 81.49°C + (0.06°C cm^2/W / 0.845cm^2 + 0.06°C/W) x 0.803W
= 81.60°C.

This MCM type, as seen from the example, is very well suited for much higher power dissipation devices than the four SRAMs used in this example. Eliminating the heat sink would alter the analysis (using 170°C cm^2/W for the module carrier package to air thermal resistance):

$T_{module\ carrier}$ = 70°C + (0.6 + 170°C cm^2/W)/ 9cm^2 x 0.803 W x 4
= 130.89°C.

$T_{junction}$ = 130.99°C.

The junction temperature is calculated using the same methodology as before. This indicates that a heat sink would not be necessary using the stated assumptions.

Table 4
MICRON DIE INFORMATION

Configuration	Data Base	Dimensions (mils)	Area cm^2	θ^1 °C/W
8K x 8	SO3	110 x 232	0.165	0.325
32K x 8	SO6	167 x 346	0.373	0.144
128K x 8	SO1	241 x 544	0.846	0.063

Note 1: This is the thermal resistance from junction to die backside (calculated value).

SUMMARY

Thermal analysis and design have become an important consideration in SRAM applications. The benefit to the end user when these considerations are properly accounted for is higher system reliability due to longer component life. For the designer, thermal design techniques result in knowledge of device junction temperatures over the operating temperature range, which directly leads to an understanding of device characteristics under the varying operating conditions. In die applications, thermal considerations are an essential part of the design task. Analysis tools based on finite element and finite difference techniques are frequently used to predict temperatures throughout MCM assemblies. Tables included in this note provide thermal resistance values which are useful in analyzing both die and packaged component applications.

NEW TECHNICAL NOTE

NEW TECHNICAL NOTE

TECHNICAL NOTE

DESIGN TIPS: 32K X 36 SYNCHRONOUS SRAM

INTRODUCTION

New medium- and high-end personal computers all need cache to reach a reasonable point on the price-performance curve. The most desirable cache is one that eliminates the most wait states. In workstation design, cache is compulsory. In personal computer design, cache is becoming essential, even in portable computer designs. The new Micron family of synchronous SRAMs provides the means to achieve the desired price-performance target. This technical note discusses the benefits of these new parts and compares them to alternatives currently available. The discussion will focus primarily on the 32K x 36 synchronous burst family members.

NEW MICRON SYNCHRONOUS SRAMs

The new Micron synchronous SRAMs comprise two configurations, each having five versions. The configurations are 32K x 36 and 64K x 18. The versions are summarized in Table 1. Intel burst sequence parts (B2 and C4 versions) are ideal for 486 and Pentium™ nonpipelined and pipelined applications. Linear burst sequence parts (M1 and A6 versions) are ideal for PowerPC™ and 680X0 nonpipelined and pipelined applications. These four versions all use BYTE WRITE inputs rather than byte enable inputs. This enables them to functionally replace 32K x 9 synchronous burst SRAMs. Hence, any cache controllers or chipsets that can use the 32K x 9 devices will function with these four 32K x 36 devices from Micron. The remaining family member has no burst counter and use byte enables. The P3 version has output registers for pipelined applications.

32K DEEP CACHE SYSTEMS WITH BURST

Zero wait state performance can be achieved in fast systems (bus speeds of 50 MHz and above) only using synchronous burst SRAMs or multiple banks of fast SRAMs with extremely fast control logic. The latter solution will at least double the minimum cache size because a minimum of two banks is required. Also, buffers are generally added in the dual bank solution because bus loading is doubled, hence more timing pressure falls upon the SRAMs and control logic which inevitably makes both more costly.

Synchronous burst SRAMs available at a 32K depth provide the easiest solution to the zero wait state dilemma. If a larger cache size is needed, they provide the option of depth expansion or using the additional parts as a second set of associativity. Studies have shown that many new software applications benefit as much or more from partitioning the cache into the two-way set associative architecture as compared to doubling the direct-mapped cache size. In other words, a 64K x 72 two-way set associative cache will perform as well or better than a 128K x 72 direct-mapped cache. Although the two-way cache is more complex to control, only half the memory is needed for a given performance target. The multiple bank SRAM solution for a two-way set design results in too much bus loading and is therefore not a practical option. In contrast, two 32K x 72 sets of synchronous burst SRAMs with each set comprised of two 32K x 36 devices can be implemented with minimal bus loading and board space.

The available 32K deep synchronous burst SRAM solutions in the industry are (or will be) 32K x 9, 32K x 18 and 32K x 36. Table 2 compares several key considerations. Since no 3.3V x9 and x18 devices have been announced, the 5V versions are used for comparison. The 32K x 36 3.3V SRAM is the clear winner in every category. The power dissipation in a 5V system using 32K x 36 devices includes the power dissipated by the 5V to 3.3V linear regulator which is needed if 3.3V is not available anywhere. The regulator adds less than 0.4 square inches more board area than listed in Table 2. This still results in the least area used. None of the cases include I/O power.

Table 1
MICRON SYNCHRONOUS SRAM VERSIONS

Part Number	Features
MT58LC32K36B2 MT58LC64K18B2	Byte Writes, Intel Burst
MT58LC32K36C4 MT58LC64K18C4	Byte Writes, Intel Burst Output Registers, Write-Through
MT58LC32K36M1 MT58LC64K18M1	Byte Writes, Linear Burst
MT58LC32K36A6 MT58LC64K18A6	Byte Writes, Linear Burst Output Registers, Write-Through
MT58LC32K36P3 MT58LC64K18P3	Byte Enables Output Registers, Write-Through

NEW TECHNICAL NOTE

Table 2
32K x 72 DIRECT-MAPPED CACHE COMPARISON

	32K x 9	32K x 18	32K x 36
Quantity for 32K x 72	8	4	2
SRAM Voltage (V)	5	5	3.3
Board area (sq. in.)	3.86	2.53	1.10
Address loading (pF)	24	16	8
Data loading (pF)	8	6	6
Power in 5V System 66 MHz (W)	7.0	5.3	2.5
Power in 3.3V System 66 MHz (W)	n/a	n/a	1.65
Power in 5V System 50 MHz (W)	5.8 (est)	4.3	2.2
Maximum height (mils)	180	180	63

FUNCTIONAL DIFFERENCES

There are almost no differences in functionality between the various 32K deep devices listed in Table 2. The 32K x 18 and 32K x 36 devices both use BYTE WRITE signals. This means that four 32K x 9 devices may be replaced by two 32K x 18 devices or one 32K x 36 device. Any of these alternatives appear the same to cache control logic. The only functional difference lies within the $\overline{ADSP}$ / $\overline{CE}$ logic within the device. The 32K x 18 and 32K x 36, because they are newer devices, benefit from lessons learned in systems employing 32K x 9 parts. The $\overline{ADSP}$ signal (which is typically fed directly from the microprocessor address/data strobe) is gated by $\overline{CE}$ in the new wider devices. This permits address pipelining to function correctly, whereas in systems built using 32K x 9 devices, this becomes awkward.

For example, assume that the cache controller discovers an L2 cache READ miss. The controller initiates a cache line fill from main memory. $\overline{ADSC}$ is used to latch in the address to the SRAM. While this fill is in progress, there is no reason to tie up the address bus since the main memory controller knows where data is needed from and the SRAM knows where it is going. The cache controller can issue a "next address" command to the microprocessor and begin the tag hit/miss comparison of the new address while the fill is still in progress. This potentially eliminates wait states when the system is ready to proceed with the next bus operation. A problem can arise using 32K x 9 SRAMs whe the next address is requested because the microprocessc will issue a new $\overline{ADSP}$ and address simultaneously. Sinc there is no way to block this command from that SRAM the cache fill in progress would be terminated by the nev $\overline{ADSP}$ command.

The newer SRAMs (32K x 18 and 32K x 36) address thi problem by the extra gate shown in Figure 1. This extra gat intercepts $\overline{ADSP}$ before propagating inside the chip an conditions it with $\overline{CE}$. Figure 1 actually shows the 32K x 3 although the logic is independent of the device width. Als shown in Figure 1 are the additional chip enables in th 32K x 36, which will be addressed later. The cache controlle can simply take $\overline{CE}$ HIGH during the fill, which will bloc $\overline{ADSP}$ from terminating the fill in progress. In systems nc utilizing this extra functionality, the extra gate does n harm and introduces no functional incompatibilities wit existing designs.

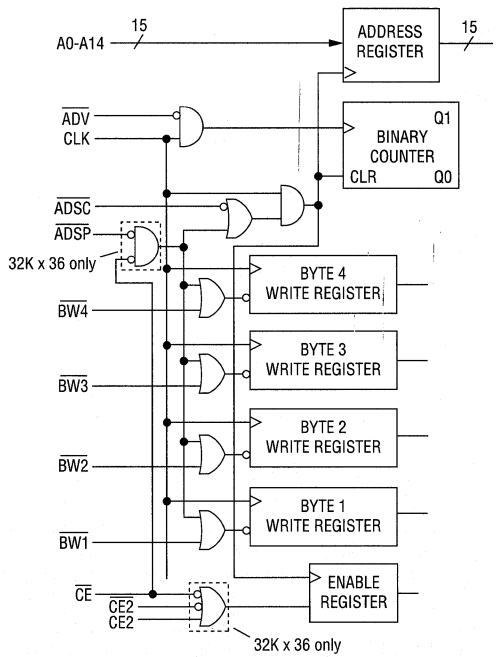


Figure 1
DIFFERENCE BETWEEN 32K x 9 AND 32K x 36

VOLTAGE CONSIDERATIONS

The electronics industry is well into the transition from 5V to 3.3V devices. High-speed (hence, high-power) requirements in microprocessors have made them very difficult to design at 5V. This is the main reason for the new 3.3V microprocessors such as Pentium, Alpha, PowerPC, 680X0, 486, etc. With the steady increase in system speed, there has also been a steady increase in SRAM power dissipation. The transition to 3.3V provides welcome relief—power dissipation is less than half in 3.3V devices compared to 5V devices with identical speed. This enables devices such as the 32K x 36 to be placed into the space-efficient TQFP without requiring expensive thermal management.

The new Micron devices obviously function in systems which are 3.3V only. However, they also function correctly in mixed voltage systems (5V and 3.3V both present). A single 3.3V supply is needed for all V_{CC} and V_{CC} Q pins. All other I/O pins are 5V tolerant. Hence, 5V CMOS logic may drive inputs to the 32K x 36 and 5V devices may reside on the same data bus with these devices. The datasheets guarantee that no special precautions are required during power-up. For example, if the main power supply is 5V and a secondary 3.3V linear regulator operates from the 5V supply to provide 3.3V to the SRAMs and elsewhere, the 5V logic could present signals to the SRAM before 3.3V is present at its supply pins. Since the 32K x 36 will not be damaged in this condition, costly power supply sequencing is not required in mixed voltage systems.

Another consideration is systems that do not have any 3.3V supplies available. Although at first glance it may seem that only 5V SRAMs should be considered, this may be a hasty judgement. Referring back to Table 2, to implement a 32K x 72 cache, two 32K x 36 devices using 1.10 sq. in. of board area are required. If a 3.3V regulator is added, less than 0.4 additional square inches is needed resulting in 1.50 square inches of board area. This is still less board area than four 32K x 18 devices (2.53 sq. in.) and results in less power dissipation than the 32K x 18 devices even with the inherent inefficiency of linear regulation. Since 3.3V regulators are inexpensive, this solution is very cost competitive as well. Once again, the argument about mixed voltage systems apply—the Micron device will accept the 5V I/O levels of the rest of the system. All outputs are 5V TTL compatible; therefore, two-way data transfer occurs with no translation circuitry required.

The Micron parts can be used in 3.6V systems as well. It is best to set the power supply voltage on the low side of 3.6V. With a reasonable tolerance, both microprocessor and SRAM will operate nominally. For example, at 3.5±0.1V both SRAM and microprocessor will operate within design specifications. In fact, the SRAM will operate slightly faster than datasheet specifications (which are listed for the low voltage and high temperature case).

POWER CONSIDERATIONS

There is a great deal of confusion in the industry about how to accurately predict power and we have all fallen victim to misconceptions at one time or another. The SRAM data sheets from any vendor excludes the current needed to switch the load capacitance from one state to another. The I_{CC} given in the datasheet accounts for everything else. The I_{CC} is used in the calculation should be appropriate for the operating conditions; e.g., I_{CC} max is specified for the lowest operating temperature, the highest recommended V_{CC} and has guardband added to it. For actual power, I_{CC} should be looked up from published current versus voltage, temperature and cycle times. See the Micron Technical Note "SRAM Thermal Design Considerations" (TN-05-14) for a derivation of true SRAM power. True SRAM power for Micron synchronous devices is:

$$P = V_{CC}\, I_{CC} + \Sigma\, P_{LAC\ (\text{for all outputs that toggle})} + P_{LDC}.$$

The incremental power due to steady-state current flow into or out of the DQ pins (P_{LDC} due to I/O leakage of connected devices) is generally ignored because it is small in systems employing CMOS devices. That extra power would be:

$$P_{LDC} = (V_{CC} - V_{OH})\, I_O\, N_H + V_{OL}\, I_I\, N_L,$$

where V_{OH} is the actual logic HIGH output voltage, I_O is output current on those DQ lines and N_H is the number of DQ lines that are HIGH; V_{OL} is the actual logic LOW voltage, I_I is the resulting input current into the DQ line and N_L is the number of DQ lines that are LOW. Since almost all CMOS devices have I_I or I_O less than 10uA (often 1 or 2uA), this calculation is inconsequential. For example, take the case where 36 outputs are connected to loads having 10uA of leakage. The contribution to device power is :

$$(3.3V - 3.0V)\ 10uA\ (36) = 108uW.$$

With higher leakage, V_{OH} drops and power increases as a result of both increased current and greater voltage drop in the SRAM output driver.

The AC load component is a different matter. For outputs which swing from logic LOW to logic HIGH, each output contributes the following to device power:

$$P_{LAC} = \frac{C_L}{T}\left(V_{CC}\,[V_{OH} - V_{OL}] - 0.5\,[V_{OH}^2 - V_{OL}^2]\right).$$

Assuming a load capacitance (C_L) of 30pF, V_{CC} = +3.3V, clock period (T) of 20ns, dynamic V_{OH} of 3.0V, dynamic V_{OL} of 0.1V, the incremental power for each output that swings

NEW TECHNICAL NOTE

from LOW to HIGH is 7.6mW. If 36 outputs did this, the output power component of the SRAM would be 274mW. The total power would be:

$$210mA \times 3.3V + 274mW = 0.967W.$$

The HIGH to LOW transition case is less severe:

$$P_{LAC} = \frac{C_L}{T}(0.5\,[V_{OH}^2 - V_{OL}^2]).$$

Using the same load conditions as the logic LOW to logic HIGH example, the resulting AC power for each output that changes from logic HIGH to logic LOW is 6.7mW.

Using the logic LOW to logic HIGH calculated power, the device case temperature is:

$$\begin{aligned} T_C &= T_A + P \times \theta_{CA} \\ &= 70°C + 0.967W \times 59°C/W \\ &= 127°C. \end{aligned}$$

This value exceeds the 110°C specification limit. In practice, θ_{CA} is lower than the specified 59°C/W because that measurement was taken in still air but not soldered in circuit. Extra thermal conduction through the 100 leads of the device lowers the θ_{CA} to approximately 35°C/W (this is dependent upon each circuit board design) in a system with a ground plane. Recalculating the case temperature for the device soldered in circuit gives a value of 104°C which is lower than the 110°C specified limit.

$$\begin{aligned} T_J &= T_A + P \times \theta_{JA} \\ &= 70°C + 0.967W \times 65°C/W \\ &= 133°C \text{ junction temperature} \end{aligned}$$

is less than the 150°C specification limit. In reality, for a device soldered in circuit, θ_{JA} is only 51°C/W which lowers the calculated junction temperature to 119°C.

At 66 MHz, the device power with all outputs switching from LOW to HIGH is 1.19W (0.365W I/O power) resulting in a T_C for a device soldered in circuit of 112°C and a T_J of 131°C, assuming 70°C ambient temperature. The maximum T_C specification is violated in this example by 2 Celsius degrees. This means that either the ambient temperature must be lowered by 2 Celsius degrees or some airflow should be added to abide by the device specifications. Practically speaking, most PC and workstation designs have airflow with the main exception being portable computers. Portables typically do not run at bus frequencies higher than 33 MHz at this time. At 33 MHz the only power dissipation or temperature specification that users need to be concerned about is staying below the 70°C maximum ambient temperature. The remainder will not be exceeded.

DEPTH EXPANSION

Another major advantage of the 32K x 36 synchronous burst SRAMs is the two extra chip enables. The extra active LOW and HIGH chip enables ($\overline{CE2}$, CE2) facilitate expansion from 32K to 64K memory depth without any additional logic. This is illustrated in Figure 2. None of the other 32K deep devices offer this flexibility.

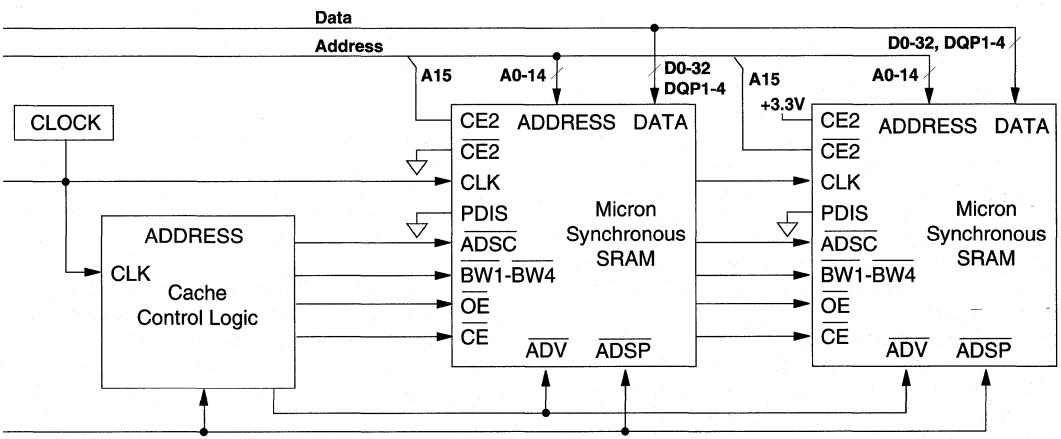


Figure 2
DEPTH EXPANSION FROM 32K x 36 TO 64K x 72

Table 3
64K x 72 DIRECT-MAPPED CACHE COMPARISON

	64K x 18	TQFP Micron 32K x 36	PLCC Micron 64K x 18**
Quantity for 64K x 72	4	4	4
SRAM Voltage (V)	5	3.3	3.3
Board area (sq. in.)	5.06	4.40	5.06
Address loading (pF)	20	16	16
Data loading (pF)	8	12	6
Power in 5V System 66 MHz (W)	7.2	3.4*	4.1*
Power in 3.3V System 66 MHz (W)	n/a	2.2	2.6
Power in 3.3V System 50 MHz (W)	n/a	1.8	2.2
Maximum height (mils)	180	63	180

* Micron device power at 5V includes power dissipated by 3.3V regulator
** Also available in a 100-pin TQFP

This expandability translates into greater flexibility in PC designs. For example, a 72-bit system which requires either a 256KB or a 512KB cache can be laid out for four 32K x 36 devices and then populated with either two or four devices, depending on the desired cache size—with no board changes and no sockets. The only other upgrade which is that simple is the change from 32K x 18 to 64K x 18. This has several disadvantages by comparison: four devices are needed in either case, the total board area needed is greater than the 32K x 36 devices (and greater still if sockets are required), power dissipation is higher and two separate part types must be stocked by the manufacturer instead of just one. Table 2 compares the 32K x 18 solution to the 32K x 36 assuming that sockets are not required. Table 3 compares the 64K x 72 cache configuration using four 32K x 36 devices versus four 64K x 18 devices. The Micron 64K x 18 solution is also shown for completeness. The one advantage that the 64K x 18 solution does offer is lower data bus loading, although the difference is small. In all other criteria, the 32K x 36 is a superior solution. Although it is clear why the 3.3V 32K x 36 results in lower power than the 5V 64K x 18, it may not be clear why the 32K x 36 system has lower power than the 3.3V 64K x 18. The reason is that only two of the four 32K x 36 devices are active at one time. At 66 MHz, the active current is 250mA but the standby current is only 85mA with clock running and all inputs toggling. By contrast, the four 64K x 18 devices from Micron would each require 200mA. The 5V competing parts require 360mA at the higher voltage.

SUMMARY

The new family of Micron Synchronous SRAMs provides the optimal solution for high-performance cache systems. 3.3V operation with 5V-tolerant I/O affords these devices flexibility to operate in any system with either 3.3V or 5V (or function with both types of devices) while dissipating less power than other alternatives. Caches of 32K depth can be created using the 32K x 36 devices and result in the lowest board space, loading and power requirements of any alternative. Systems requiring the flexibility of cache depth doubling can also be satisfied with the 32K x 36 devices using the extra available chip enables incorporated into the device. The resulting 64K deep cache is still more efficient than designs using the 5V 64K x 18 devices.

NEW TECHNICAL NOTE

TECHNICAL NOTE

A DESIGNER'S GUIDE TO 3.3V SRAMs

INTRODUCTION

The challenge of reducing power consumption is critical in laptop, notebook and palmtop computers, and is a growing factor in desktop and workstation applications. A key solution to reducing power is the use of 3.3 volt components in system designs. Although battery life is the dominant issue in most portable designs, other issues such as the migration of high-density microprocessors to 3.3V and technology requirements to produce memory components, especially in DRAMs, are forcing the transition to 3.3V. Even the Environmental Protection Agency (EPA) is getting into the act by mandating power reduction for all computers purchased by the federal government.

This paper discusses the main reasons propelling system designers to use 3.3V logic, how Micron SRAMs are constructed for 3.3V operation, and issues specific to designing mixed 3.3V and 5V systems. Because not all components are currently available at 3.3V, it is especially important for designers to understand how to incorporate these lower voltage parts in robust, reliable system designs.

REASONS FOR 3.3V LOGIC

Several issues are accelerating the use of 3.3V components in computer systems. Although reduction of system power is the primary reason, other considerations form a powerful argument for converting new designs to 3.3V. This section details the main reasons and advantages.

REDUCING SYSTEM POWER AND EXTENDING BATTERY LIFE

Extending battery life and reducing the size and weight of the battery pack are two key design concerns. Many current laptop and notebook designs run out of power in one to two hours, forcing the user to recharge batteries frequently or carry spare battery packs. The long-term goal of portable computers is to provide desktop-equivalent performance, extended battery life (8 to 10 hours or more) and drastically reduced battery weight (perhaps as few as two AA cells).

Current techniques to reduce power rely on enhanced power- management modes implemented in memory controllers, or in the processor itself. Other savings in power have come about through the use of low-power components such as extended refresh or SELF REFRESH DRAMs. These methods have decreased power, but fail to achieve desired performance and battery life levels. These goals can be realized only through the use of lower voltage components.

To show the benefits of 3.3V over 5V components, Table 1 gives a comparison of power for several products avail-

Table 1
A COMPARISON OF 3.3V AND 5V MEMORY POWER DISSIPATION

Manufacturer	Part Type	Power Mode	5V Power (MAX mW)	3.3V Power (MAX mW)	% Savings 3.3V vs. 5V
SRAMs					
Micron	256K, x8, 20ns	Operating	660	252	67
		CMOS Standby	28	3.6	87
IDT	256K, x8, 20ns	Operating	798	342	57
		CMOS Standby	110	1.8	98
DRAMs					
Micron	4 Meg, x4, 80ns	Operating	495	180	44
		BBU*	1.65	.324	80
NEC	4 Meg, x4, 80ns	Operating	495	216	56
		SELF REFRESH	0.72	0.36	50
TI	DSP TMS320C5x	Typical Operating	13.8mW per MIPS	5.4mW per MIPS	61
Motorola	DSP56L002	Operating 40 MHz	500	165	67

* BATTERY BACKUP current. This represents the DRAM operating at a $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ refresh at the slowest possible cycle time.

able at both voltages. Memory components (DRAMs and SRAMs) and DSP microprocessors are shown. As shown, the amount of power saved in converting to 3.3V is significant. Power savings average 67 percent, allowing the system battery life to more than double.

SUPPORTING 3.3V PROCESSORS

A number of 3.3V microprocessors and microcontrollers have appeared in the marketplace and are leading the industry into low- voltage system design. For optimal performance, minimized power and chipcount, and simplified design, these chips require lower voltage support chips and peripherals.

High-speed and high-performance designs are adopting 3.3V products as demonstrated by Digital's Alpha AXP chip, Silicon Graphics' MIPS R4400, and IBM and Motorola's PowerPC. One of the main reasons these products have moved to 3.3V is to reduce the power dissipated by the high-frequency processor chips. At 5V, Intel's Pentium chip draws some 17 watts at 66 MHz. The problems of dissipating this power should force Intel to move quickly to a reduced-voltage part. Even though Digital's 21064 Alpha chip already operates at 3.3V, it still dissipates a whopping 23 watts at 150 MHz. Digital recently announced new versions running up to 200 MHz with plans to move to 300 MHz in the next several years. These processors must move to 3.3V due to high transistor count and high-frequency operation. The lower voltage helps reduce or eliminate external cooling components such as heatsinks or fans.

At the lower end of the scale, portable applications are using 3.3V microprocessors to reduce system power and extend battery life. A number of 3.3V microprocessors have appeared for use in portable applications such as personal digital assistants (PDAs) and notebook computers. Digital signal processors such as TI's TMS320C5x and Motorola's DSP56L002 have appeared with options to run at either 3.3V or 5V. As shown in Table 1, the TMS320C5x runs with a 62 percent reduction in power at 3.3V, while the DSP56L002 saves 67 percent.

EPA ENERGY STAR PROGRAM

According to the EPA, computer systems account for five percent of commercial electricity consumption in the United States. Left unchecked, this could grow to ten percent by the year 2000. A large percentage of this power is consumed by unused computers left on after hours or through the weekend. During these time periods, as many as 30 to 40 percent of all computers are left on and inactive.

The goal of the Energy Star Program is to reverse the trend of increased power usage of computers, thus eliminating the need to build more power plants. The primary strategy is to reduce power requirements of desktop computers that can use as much as 300 watts of power in active mode to below 150W with a standby mode power of less than 30W (not including the monitor). PCs meeting these specifications are commonly referred to as "green machines" or "green PCs."

Another incentive has been given to the computer industry by the federal government through its purchase of computer products. All computers purchased after October, 1993 by the federal government must meet these new Energy Star standards. This motivator has led to development of a number of "green PCs," with an increasing number running at 3.3V.

RELIABILITY

Because 3.3V logic reduces power consumption, devices run cooler than their higher voltage counterparts, and junction temperatures are reduced. Reliability is exponentially related to junction temperature, with a reduction in junction temperature increasing the long-term reliability of the component. Reduced voltage levels mean less stress is placed on the dielectrics. Because Micron's SRAM inputs are tolerant to 5V inputs (+6V MAX), potential problems with damaging input voltage levels in mixed-voltage systems are considerably reduced.

Reliability improvements also extend to the system level since 3.3V components generate less noise due to their reduced power levels. This reduced power leads to a minimization in the number of components for cooling, thus reducing system size.

TECHNOLOGY ISSUES

As DRAM technology moves to 0.55µm and smaller, the voltage level has to be reduced. Current 16 Meg DRAMs are manufactured with 5V periphery logic and I/O using an internally generated 3.3V power supply for the memory array. These parts interface with the external world using industry-standard 5V I/O levels while maintaining the benefits of lower voltage for the internal array. Next generation 16 Meg DRAMs will have versions operating externally at 3.3V, while all 64 Meg DRAMs will operate exclusively at the 3.3V level.

The main motivation for DRAM conversion to 3.3V has been to reduce power in the DRAM device. However, at the transistor level, several technical factors are also making 3.3V a desired standard. As DRAM technology moves toward thinner oxides, and 0.55µm (and finer) design rules are used to shrink transistor dimensions, applying 5V across the transistor degrades both performance and reliability. The move to 3.3V allows reliable transistor performance down to channel lengths of 0.4µm before requiring further voltage reduction.

3.3V SRAM MEMORIES

In the past year, several 3.3V SRAM memory components have been introduced. Initially these 3.3V SRAMs were recharacterized 5V products that usually suffered a significant speed loss and sometimes reduced noise margins when operating at 3.3V. Some estimates have shown that recharacterization slows parts by at least 50 percent. Users are unwilling to pay a performance penalty in order to extend battery life, and desire the same type of performance in a portable machine as in a desktop. This is attainable only if the lower power components can also operate at high-performance levels.

The second generation of 3.3V SRAMs takes advantage of new design techniques that optimize speed at the reduced voltage level. These speed improvements are made possible by the lower voltage, which, due to lower breakdown levels, reduces critical transistor dimensions. As lithographic techniques improve and dimensions get smaller, only lower-voltage parts can take advantage of smaller transistor dimensions. For this reason, they will eventually exceed the speed of 5V parts. The other advantage new 3.3V designs have over screened parts is that they optimize transistor threshold voltages, increasing noise margin on inputs and outputs.

The input protection circuits on Micron's 3.3V SRAMs have been designed to provide excellent immunity to electrostatic discharge (ESD). Micron's new 3.3V 256K SRAM exhibited greater than 2000V of ESD tolerance on all pins with the average pin typically having more than 6000V of tolerance. These tests were performed using the Human Body Model ESD test. Even though Micron SRAMs have excellent tolerance to ESD, it is still recommended that while handling, shipping or storing devices, appropriate ESD measures be used.

Micron 3.3V SRAMs have been designed to work in cache memory applications for high-performance systems ranging from workstations to notebooks. Micron's 3.3V SRAM product line features a wide variety of SRAMs including 256K, 1 Meg (evolutionary and revolutionary pinout) and 4 Meg versions (Table 2). These SRAMs have been designed using Micron's advanced 3.3V process technology and optimized 3.3V circuits.

One of the major advantages of these SRAMs is their ability to work in high-performance systems. Micron's 3.3V 256K SRAMs presently run as fast as 12ns and are excellent choices for cached memory systems in 3.3V desktop green machine or notebook design. While these 3.3V SRAMs provide the power savings that portable applications require, they do not have the speed penalty associated with screened 5V SRAMs.

3.3V JEDEC STANDARDS

In order to ensure conformity of 3.3V interfaces among manufacturers, the computer industry has adopted JEDEC protocol 8-1, "Interface Standard for 3.3V ±0.3V Supply Digital Integrated Circuits." The voltage requirements for this specification are shown in Table 3. All Micron 3.3V SRAMs conform to this standard or exceed it.

Some confusion may exist because a number of ICs operate with a wide voltage supply range of 2.7 to 5.5V. This voltage range has been used in some battery-powered applications where speed is not as important as battery life. These systems pay a significant penalty in speed and will not be used when performance is an issue. Designers refer to these systems as unregulated because the wide voltage range means they can be designed without voltage regulators.

NEW TECHNICAL NOTE

Table 2
MICRON'S 3.3V ASYNCHRONOUS FAMILY

Part Number	Configuration	Access Time	Packages
MT5LC2561	256K x 1	12, 15, 20, 25, 35	DIP, SOJ
MT5LC1001	1 Meg x 1	20, 25, 35, 45	DIP, SOJ
MT5LC2564	64K x 4	12, 15, 20, 25, 35	DIP, SOJ
MT5LC2565	64K x 4 $\overline{OE}$	12, 15, 20, 25, 35	DIP, SOJ
MT5LC1005	256K x 4	20, 25, 35, 45	DIP, SOJ
MT5LC256K4D4	256K x 4	20, 25	SOJ
MT5LC1M4D4	1 Meg x 4	20, 25, 35	SOJ
MT5LC2568	32K x 8	12, 15, 20, 25, 35	DIP, SOJ
MT5LC1008	128K x 8	20, 25, 35, 45	DIP, SOJ
MT5LC128K8D4	128K x 8	20, 25	SOJ
MT5LC512K8D4	512K x 8	20, 25, 35	SOJ
MT5LC64K16D4	64K x 16	20, 25	SOJ
MT5LC256K16D4	256K x 16	20, 25, 35	SOJ

Table 3
JEDEC STANDARD 8-1 FOR 3.3V LOGIC

DC Operating Conditions			
Parameter	**Condition**	**MIN**	**MAX**
V_{CC}	-	3.0V	3.6V
V_{OH}	-2mA	2.4V	-
V_{OL}	2mA	-	0.4V
V_{IH}	-	2.0V	V_{CC} + 0.3V
V_{IL}	-	-0.3V	0.8V
Absolute Maximum Conditions			
V_{CC}	-	0.5V	4.6V
V_{IN}	-	0.5V	V_{CC} + 0.5V (4.6V MAX)

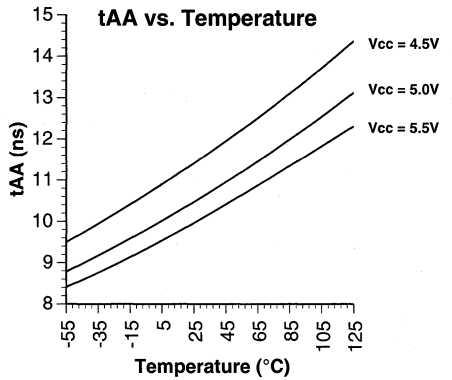


Figure 1
ACCESS TIME VERSUS TEMPERATURE AND VOLTAGE

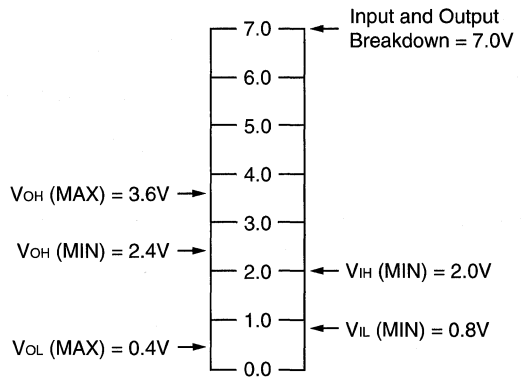


Figure 2
3.3V DEVICES DRIVING 5V LOGIC

High-speed systems use microprocessors running with a much tighter tolerance with Vcc of 5V ±5% or 3.3V ±0.15V to provide higher performance. The voltage supply of the microprocessor is usually shared with the cache memory and hence the SRAM speed can also benefit from the increased timing margins due to only a five percent variance.

Figure 1 shows how access time varies versus temperature and voltages for the 5V 256K SRAM. A 3.3V part will exhibit similar performance characteristics. At 5V, a ten percent tolerance on Vcc means a low Vcc of 4.5V and a five percent tolerance means a low Vcc of 4.75V. For the parts shown here, the increase in low end Vcc increases the speed of the part. This gain becomes even more important as clock speeds approach or exceed 60 MHz.

3.3V SRAMS DRIVING 5V COMPONENTS

Figure 2 shows how 3.3V output logic levels can be used to drive 5V TTL levels. These logic levels guarantee a minimum noise margin to 400mV when driving HIGH or LOW output levels and typical values provide even more margin. 5V device inputs require a minimum V_{IL} of 0.8V and 3.3V devices supply less than 0.4V. Similarly, inputs require a minimum V_{IH} of 2.0V and are supplied with 2.4V or greater.

There has been some concern that 3.3V parts driving 5V inputs will cause a slightly higher power dissipation because the inputs are not driven to a full voltage rail. But because not all 5V TTL memories drive to CMOS rails, they will have similar power dissipation on inputs.

There are no difficulties using 3.3V outputs to drive 5V TTL circuits, but they should not be used to directly drive 5V CMOS level inputs on true CMOS devices. To reach V_{IH} (MIN), 5V CMOS devices with CMOS thresholds require a greater logic-HIGH input voltage than can be supplied by 3.3V devices. Designs requiring 5V CMOS levels need a voltage translation or buffer circuit. This restriction is also present on 5V TTL outputs, but can be more easily alleviated by means of a pullup device.

Some manufacturers specify that logic HIGH on their 3.3V High-Z outputs or bidirectional buses not exceed Vcc+0.5V. This limitation is especially critical when the outputs are connected to a bus with 5V drivers. Even a 3.3V notebook might be connected to a 5V printer or peripheral. Although the 3.3V devices can drive 5V inputs, the 5V bus may overdrive the maximum allowable voltage during High-Z. Devices with restrictive maximum voltages require some type of buffering to prevent damage to the I/O pins. This buffering may be the addition of a current limiting resistor for 3.3V components that would have excessive current through a clamping diode or a register latch buffer for those devices that suffer from latchup problem when overdriven.

An advantage of Micron 3.3V SRAMs is that these extra circuits are not required when connecting to a 5V bus. Micron SRAMs are designed to tolerate 5V signals driven directly into bidirectional or High-Z outputs. This also means our 3.3V circuits can be connected to buses using pull-up resistors to 5V or drivers using 5V TTL or CMOS levels. If a pull-up transistor is required on a bus, we

recommend a pull-up connected to 3.3V instead of 5V. While saving power, this pull-up to 3.3V will still allow a logic HIGH on the bus when driving TTL components. This SRAM tolerance to 5V signals saves space by eliminating buffer circuits, saves power by reducing components, and prevents headaches. Figure 3 shows the various bus options that must be considered by a designer. In the figure, 3.3V circuit A requires a current limiting register to prevent destructive currents when being driven by a 5V output. 3.3V circuit B requires a buffer to prevent latchup, and Micron's 3.3V SRAM, interfaces directly to the bus.

5V COMPONENTS DRIVING 3.3V SRAMS

The JEDEC 8-1 standard specifies that 3.3V input voltages can range from -0.5V to Vcc+0.5V (4.6V [MAX]). This range was reduced by JEDEC from their original 1984 standard, which specified a maximum input voltage of 5.5V, therefore allowing 5V devices to directly drive 3.3V inputs. JEDEC modified the older standard because the transition period to 3.3V is turning out to be much shorter than originally envisioned.

Micron SRAMs are designed to surpass the 8-1 JEDEC standard by allowing an absolute maximum voltage of +6.0V on the inputs, with 5.5V as the recommended maximum DC operating condition. This allows any 5V device with either a TTL or CMOS output to directly drive the 3.3V inputs. These 5V-tolerant inputs supplant buffer logic between components with different supply voltages, thus saving power and board space and reducing complexity.

Designers need to be careful when considering 3.3V components because some do not exceed the JEDEC +4.6V MAX (V_{IN}) specification. Directly driving these 3.3V components with 5V parts will exceed this value and could cause a latchup failure. Mismatched impedances worsen the problem since ringing will occur and drive the voltages higher than their steady-state values. A number of companies including IDT, National Semiconductor, Texas Instruments and Toshiba offer buffering components specifically designed to address the buffering issues encountered in mixed-voltage systems. As 3.3V components proliferate, designers may be forced to use these buffer circuits if the 3.3V component does not offer direct 5V compatibility. Figures 4 and 5 show how to connect circuits and how the voltage levels interact when 5V components drive 3.3V circuits.

Although the minimum JEDEC standard for V_{OH} and V_{OL} specifies a current of +2mA and -2mA, Micron exceeds these standards and offers output currents identical to the 5V TTL standards of +8 and -4mA. These high currents allow Micron SRAMs to attain high-speed operation.

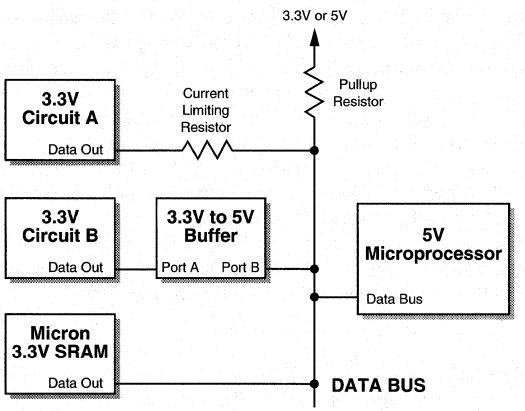


Figure 3
CONNECTING 3.3V OUTPUTS TO 5V CIRCUITS

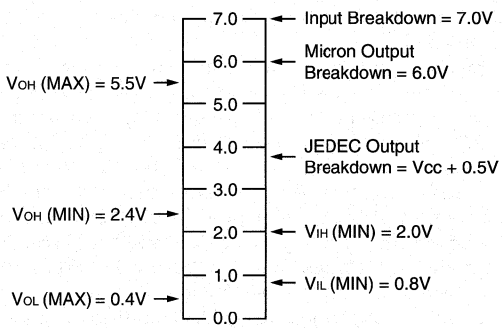


Figure 4
5V DEVICES DRIVING 3.3V LOGIC

NEW TECHNICAL NOTE

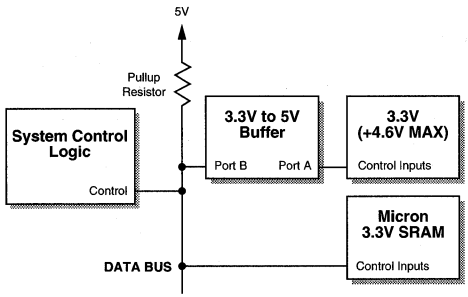


Figure 5
5V DEVICES DRIVING 3V LOGIC

POWER-UP DESIGN CONSIDERATIONS

Mixed-voltage designers need to be especially careful during the power-up and power-down sequence to ensure that 5V parts do not violate the input specifications of 3.3V parts. For instance, even though the 3.3V Alpha microprocessor can tolerate direct 5V inputs, according to the Hardware Reference Manual no input or bidirectional pin can rise above 4V until the 3.3V supply is stable. Failure to meet this rule can cause damage to the Alpha. This is because a 5V part could drive an input to a 3.3V part with a Vcc of 0V, exceeding breakdown voltages and permanently damaging the device.

Three solutions are available to minimize problems during power-up and power-down in mixed voltage systems. The first is to use power supply sequencing to ensure that the 3.3V power supply is stable before any 5V signals are applied. The second is to use tristate outputs to drive 3.3V logic, and ensure that all inputs remain in tristate until the 3.3V supply is stable. Power supply designs that sample the 3.3V power supply and generate a tristate signal based on it offer the safest design approach because the tristate will be removed only when power is stable.

The third solution is to use a 3.3V product without a power-up problem. Micron SRAMs have been constructed to completely eliminate such problems. They are designed so that a 5V signal can be applied to the inputs even if the 3.3V Vcc pin is between 0 and 3V. These SRAMs provide ample time for both power supplies to reach a stable state regardless of which is turned on first. A typical power supply voltage ramp-up time is between 10ms and 20ms. For long term reliability, we recommend that the input voltage does not exceed 3.3V for greater than 200ms while Vcc < 3.0V. To support a wide variety of 3.3V parts, power supplies of mixed-voltage systems should ensure a minimum delay between power-up of the 5V supply and the 3.3V supply.

POWER SUPPLY CONSIDERATIONS

Power supply manufacturers are developing a wide array of products simplifying mixed-voltage designs and power-up considerations. Power supply chips that supply multiple output voltages are now available, such as Maxim's MAX782 supply. These chips can be used to generate the voltage supplies of mixed voltage systems, and support power supply sequencing per the designer's specifications.

Many designers have not considered using a lower voltage part because a 3.3V supply is unavailable. Many expansion slots in computers only have a 5V supply available and 3.3V has to be generated on the card. However a 3.3V supply can easily be generated with a voltage regulator as shown in Figure 6. Regulators are inexpensive and take up minimal area (typically < 0.4 in2). The additional power drawn by the regulator is insignificant given the power savings of the 3.3V components. Micron SRAMs require only a 3.3V supply and no additional buffer circuitry when interfacing to other 5V components.

CONCLUSION

Although the transition to 3.3V was envisioned to take a number of years, 3.3V microprocessors and low-power portable designs may force a majority of systems to transition in the next 18 months. This transition will be marked by a number of mixed-voltage systems until all computer components are available in 3.3V versions. Designers of the mixed-voltage systems must look carefully at manufacturers' specifications to determine if external buffering is required, and how to gain maximum power savings from the devices. Micron 3.3V SRAMs are an excellent choice for 3.3V systems because they have been designed to minimize design headaches and eliminate buffers when interfacing with 5V TTL components. As Micron is continually improving and expanding our 3.3V line, designers should consult the factory for the latest information on new products.

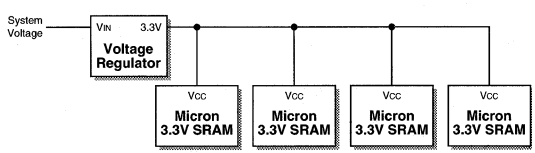


Figure 6
GENERATING 3.3V IN A 5V SYSTEM OR PERIPHERAL

MICRON SEMICONDUCTOR, INC.

OVERVIEW

Product reliability is a product's ability to function over time within given performance limits under specified operational conditions. This section contains a brief overview of some of the issues that affect the reliability of IC devices and briefly describes Micron's reliability program.

For a more in-depth discussion of reliability, please refer to Micron's quality/reliability literature.

RELIABILITY GOALS

When we discuss reliability goals of semiconductor ICs, we typically refer to the traditional reliability curve of component life. The reliability curve, or "bathtub curve," appears below, where h(t) is the hazard rate or the probability of a component failing at t_0+1 in time if it has survived at time t_0.

The reliability curve in Figure 1 is divided into three segments: infant mortality, random failure, and wearout. The term "infant mortality" refers to those ICs that would fail early in their lives due to manufacturing defects. To screen out these failures, Micron evaluates all our products using intelligent burn-in. Our unique AMBYX® intelligent burn-in and test system, is described in the following section.

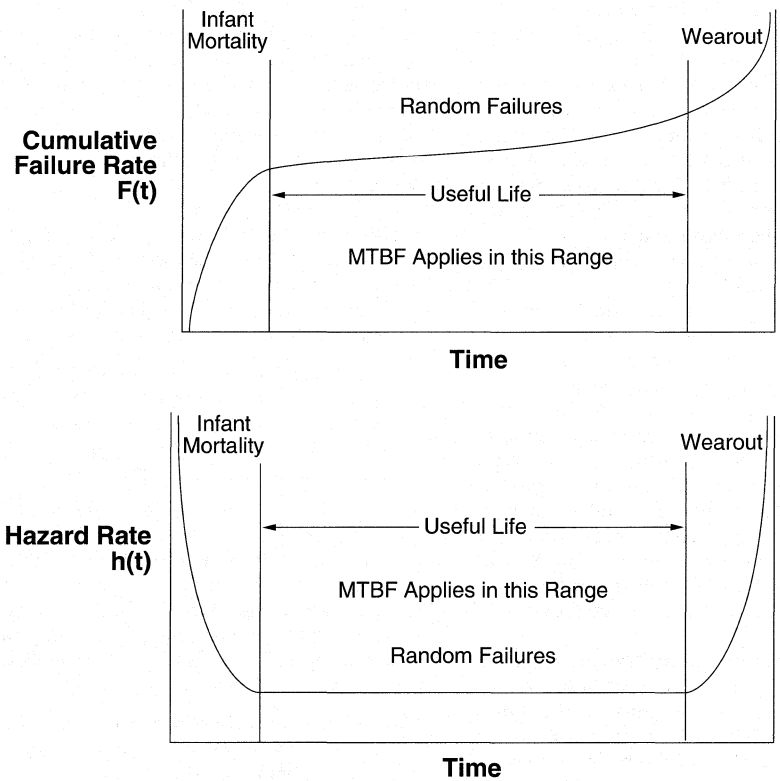


Figure 1
RELIABILITY CURVE

MICRON'S AMBYX INTELLIGENT BURN-IN AND TEST SYSTEM

As the semiconductor industry has evolved, burn-in has become regarded as critical to product reliability. To effectively screen out infant mortalities, Micron believes it is critical to functionally test devices several times during the burn-in cycle without removing them from the burn-in oven. In 1986, we were unable to find a system that met our requirements, so we introduced the concept of "intelligent" burn-in and developed the AMBYX intelligent burn-in and test system. Today, we use it to test every component and system-level product we make.

With AMBYX, we can determine if the failure rate curves of individual product lots reach the random failure region of the bathtub curve by the end of the burn-in cycle. We subject product lots that do not exhibit a stable failure rate to additional burn-in. This burn-in flow also brings the slightest variation in a product's failure rate to our attention.

Since AMBYX allows us to test devices for functionality without removing them from the burn-in oven, we effectively eliminate failures resulting from handling, thereby minimizing "noise" from the test results. During the test phase, output produced by the devices under test is compared to the pattern expected. If a discrepancy occurs, AMBYX records the failure and provides the bit address, device address, board address, temperature, Vcc voltage, test pattern, and time set.

During the burn-in cycle itself, devices are functionally tested in four intervals. The first test begins at room temperature. Then, we ramp up the oven to 125°C. The devices are functionally tested while the temperature ramps up and again when the oven has reached 125°C. This enables us to detect thermal intermittent failures, another unique feature of intelligent burn-in. Any device that does not pass this sequence is eliminated. As the burn-in process continues, the devices are dynamically stressed at high temperature and voltage for a given number of hours. At the end of this period, we functionally test all devices again, followed by another burn-in cycle and further tests. This sequence is repeated four times on every device in every production lot.

These test results allow us to identify individual failures after each burn-in cycle. Figure 2 illustrates how the four burn-in and test cycles flow. This test curve is used for a number of our 5-volt products. The typical test results shown make up the first portion of the bathtub curve of component reliability.

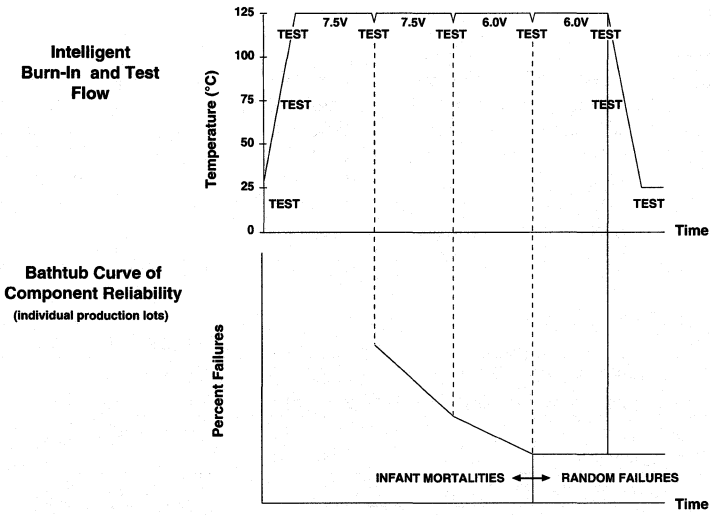
There are two important reasons that Micron conducts the last two burn-in and test periods (or "quarters") at lower Vcc than the first two portions. First, we want the several million device hours that we accumulate weekly on production lots to be conducted at stress conditions identical to the conditions for the extended high-temperature-operating-life (HTOL) test. All semiconductor manufacturers use this test to calculate random field failure rates. Second, we want to be sure we are not introducing new failure modes unrelated to normal wearout (such as Vos) by testing under extremely elevated conditions. In this way, Micron ensures that we've effectively screened our products for infant mortalities.

Control charts, such as the one shown in Figure 3, alert us to trends in the failure rates of some lots. When we detect an upward trend in a failure rate, we pinpoint the lots that need additional burn-in cycles to identify all variables that might influence the failure rates of those lots. Such variables could include fabrication and assembly equipment, manufacturing shifts and time frames when the lots were processed through specific steps.

The overall benefits of intelligent burn-in are wide ranging. Three of the most important benefits are summarized below:

- Using the AMBYX system, we are able to determine the optimal amount of burn-in time required for each product and/or process and thereby eliminate the risk of inadequate burn-in, which could allow inherently weaker devices to go undiscovered.
- Because AMBYX test results for each product and/or process are derived through optimal burn-in time, we are able to correlate the burn-in data with millions of device hours of HOTL testing, used to calculate hard error rates for all Micron products.
- Using AMBYX, we are able to react quickly to reliability related process shifts, correlating lots that need additional burn-in cycles with all variables that might be influencing the failure rates of those lots. Examples of such variables include fabrication and assembly equipment, manufacturing shifts, time frames during which the lots were processed through specific steps and process recipes.

Other benefits include the ability to differentiate between hard and soft errors and to identify variation in these parameters on production lots.



Note: The voltage levels vary depending on the product being tested (for example, standard 5V product vs 3.3V product).

Figure 2
AMBYX BURN-IN/TEST FLOW AND TEST RESULTS

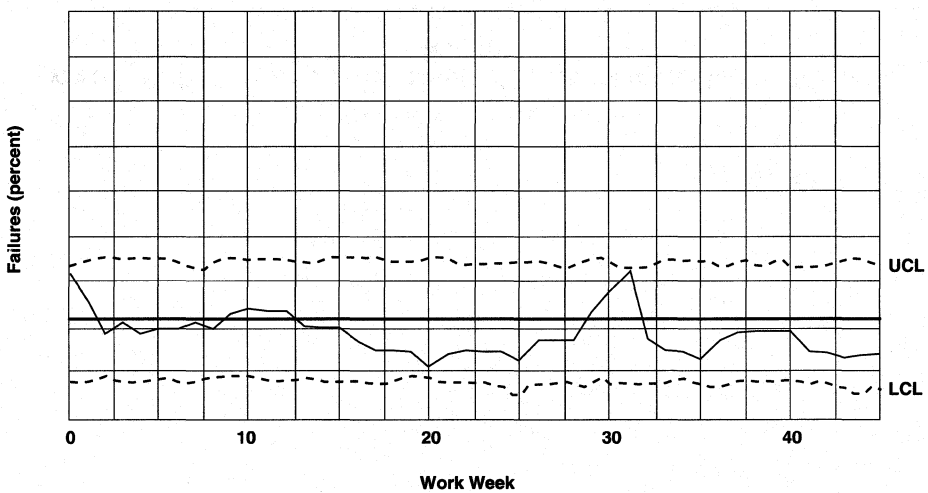


Figure 3
AMBYX FOURTH QUARTER FAILURES

ENVIRONMENTAL PROCESS MONITOR PROGRAM

Micron's environmental process monitor (EPM) program is designed to ensure the reliability of our standard products. Under this program, we subject weekly samples of our various product and package types to a battery of environmental stress tests.

During these tests, we stress the devices for many hours under conditions designed to simulate years of normal field use. We then apply equations derived from intricate engineering models to the data collected from the accelerated tests. From these calculations, we are able to predict failure rates under normal use. Figure 4 shows the conditions for these environmental stress tests. The EPM program described in Figure 4 is for Micron's 1 Meg SRAM.

TEST NAME AND DESCRIPTION	TEST DURATION	BIWEEKLY SAMPLE SIZE
HIGH TEMPERATURE OPERATING LIFE* (125°C, 6V, Checkerboard and Checkerboard Complement Patterns)	1,008 Hours	100 Devices
TEMPERATURE AND HUMIDITY* (85°C, 85% RH, 5.5V, Alternating Bias)	1,008 Hours	50 Devices
AUTOCLAVE (121°C, 100% RH, 15 PSI, No Bias)	96 Hours	25 Devices
LOW TEMPERATURE LIFE* (-25°C, 7V, Checkerboard and Checkerboard Complement Pattern)	1,008 Hours	5 Devices
TEMPERATURE CYCLE (-65°C to +150°C, Air to Air)	1,000 Cycles	50 Devices
THERMAL SHOCK (-55°C to +125°C, Liquid to Liquid)	700 Cycles	10 Devices
HIGH TEMPERATURE STORAGE (150°C, No Bias)	1,008 Hours	50 Devices
ELECTROSTATIC DISCHARGE (+ and -)	MIL-STD-3015	40 Devices
HIGH TEMPERATURE STEADY STATE* (150°C, 6.5V)	1,008 Hours	5 Devices
V_{CC} LATCH-UP (85°C)	–	10 Devices

Figure 4
SAMPLE ENVIRONMENTAL PROCESS MONITOR – 1 MEG SRAM

NOTE: Samples pulled from five different lots at finished goods.
* Voltage levels will vary depending upon the product being tested (for example, standard 5V product vs 3.3V product).

FAILURE RATE CALCULATION

The failure rate during the useful life of a device is expressed as percent failures per thousand device hours or as FITs (failures in time, per billion device hours). To facilitate our explanation of how FIT rates are calculated, Figure 5 contains sample high temperature operating life (HTOL) test results for Micron's 1 Meg SRAM. The failure rate is calculated as follows:

$$\text{Failure Rate} = \frac{Pn}{\text{Device hours} \times \text{AF environment}}$$

AF is relative to the typical operating environment.

where: Pn = Poisson Statistic (at a given confidence level). In our example, for two failures at a 60 percent confidence level, Pn = 3.105.

Device hours = sample size multiplied by test time (in hours). From the table in our example, device hours in an accelerated environment = (2,466 x 168) + (2,365 x 168) + (2,357 x 168) + (2,357 x 168) + (2,357 x 168) + (2,155 x 168) = 2.362×10^6.

AF = acceleration factor between the stress environment and typical operating conditions. For the 1 Meg SRAM, the acceleration factor between 125°C, 6V (HTOL stress conditions) and 50°C, 5V (typical operating conditions) equals 93. (Calculation of this acceleration factor is described in the following section.)

Thus, the failure rate of the Micron 1 Meg SRAM family is computed as follows:

$$\text{Failure Rate} = \frac{3.105}{(2.362 \times 10^6)\,(93)} = 1.414 \times 10^{-8}$$

where: Total device hours at test conditions = 2.362×10^6. Equivalent device hours at typical use conditions (50°C, 5V Vcc) using an acceleration factor of 93 equals: $93\,(2.362 \times 10^6) = 220 \times 10^6$.

To translate the failure rate for the 1 Meg SRAM family into a percentage of failures per thousand device hours, we multiply the failure rate obtained from the equation above by 10^5:

$$\text{Failure Rate} = (1.414 \times 10^{-8}) \times 10^5 = 0.001414\% \text{ or } 0.0014\% \text{ per 1K device hours.}$$

To state the failure rate in FITs, we multiply the failure rate obtained from the equation above by 10^9:

$$\text{Failure Rate} = (1.414 \times 10^{-8}) \times 10^9 = 14.14 \text{ or } 14 \text{ FITs.}$$

RELIABILITY

Package	Configuration	168 Hours	336 Hours	504 Hours	672 Hours	840 Hours	1,008 Hours
SOJ	x4, 28L	0/0400	0/0400	0/0400	0/0400	2/0400	0/0298
	x8, 32L	0/1199	0/1098	0/1098	0/1098	0/1098	0/0998
PDIP	x4, 28L	0/0100	0/0100	0/0100	0/0100	0/0100	0/0100
	x8, 32L	0/0767	0/0767	0/0759	0/0759	0/0759	0/0759
	Total	0/2466	0/2365	0/2357	0/2357	0/2357	0/2155

Figure 5
HIGH TEMPERATURE OPERATING LIFE (HTOL)

Note:
1. Preconditioning: All surface-mount packages are run twice through an infrared (IR) reflow oven, reaching a peak temperature of 240°C.
2. Test conditions: 125°C, 6V Vcc, checkerboards and checkerboard complement pattern for up to 1,008 hours in 168-hour intervals. Devices are tested for functionality after each interval.

ACCELERATION FACTOR CALCULATION

The acceleration factor between high temperature operating life stress conditions (125°C, 6V) and typical operating conditions (50°C, 5.5V) for the 1 Meg SRAM is computed using the following models:

ACCELERATION FACTOR DUE TO TEMPERATURE STRESS

The acceleration factor due to temperature stress is computed using the Arrhenius equation, which is stated as follows:

$$AF_T = e^{\left(\frac{E_a}{k}\left[\frac{1}{T_o} - \frac{1}{T_s}\right]\right)}$$

where: k = Boltzmann's constant, which is equal to 8.617×10^{-5} eV/K

T_o and T_s = typical operating and stress temperatures, respectively, in kelvins

E = activation energy in eV. (For oxide defects, which are the most common failure mechanisms for the 1 Meg SRAM [used in our example], the activation energy is determined to be 0.3eV.)

Using these values, the temperature acceleration factor between 125°C and 50°C is computed to be 7.623.

ACCELERATION FACTOR DUE TO VOLTAGE STRESS

The acceleration factor due to voltage stress is computed using the following model:

$$AF_v = e^{(\beta [v_s - v_o])}$$

where:

v_s and v_o = stress voltage and typical operating voltage, respectively, in volts

β = constant, the value of which was derived from TDDB studies. (For the 1 Meg SRAM used in our example, ß equals 2.5).

Thus, the voltage acceleration factor for the 1 Meg SRAM between 6V (stress condition) and 5V (typical operating condition) is computed to be 12.182.

Finally, the overall acceleration factor due to temperature and voltage stress is calculated as the product of the two respective acceleration factors or:

$$AF_{overall} = AF_{temperature} \times AF_{voltage}$$
$$= 7.623 \times 12.182$$
$$= 93.$$

RELIABILITY

OUTGOING PRODUCT QUALITY

Before being sent to our finished goods area, where products are prepared for shipping, a special unit within the quality assurance department takes a random sample from each production lot. These samples are subjected to visual and electrical testing in order to measure the acceptable quality level (AQL) of all outgoing product.

Visual or mechanical testing consists of an unaided visual inspection of the sample devices for any physical irregularities that could negatively affect their performance. If a sample device is found to have, for example, a bent lead, a package irregularity or excess solder, the entire lot is returned to our test area for a 100 percent visual inspection.

Electrical testing of the sample devices is performed using automatic test equipment (ATE) systems. Should an electrical failure occur, a quality assurance engineer further evaluates the failing device. If after completing this analysis, the quality assurance engineer determines which production monitor or test should have caught the failure, and the entire lot is retested at that point in the test flow. These are important steps to preserve the integrity of our test process.

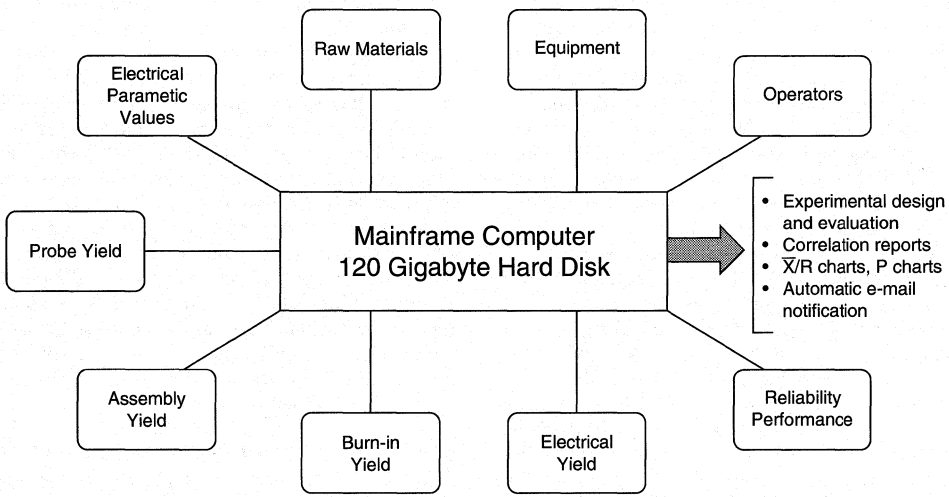


Figure 6
STATISTICAL CORRELATION

AUTOMATED DATA CAPTURE & ANALYSIS

Micron has developed a sophisticated data capture and analysis system with a computer network tailored to the needs of quality IC manufacturing. Figure 6 shows the various functional areas that provide the input to our VAX databases.

DATA CAPTURE

Automated, real-time data capture makes real-time charting ($\overline{X}$ and R charts, etc.) of all critical operations and processes possible and ensures that appropriate personnel know of any unexpected variation on a timely basis. As production lots move through each manufacturing step, detailed information (including step number, lot number, machine number, date/time, and operator number) are entered into the production data base. Automated, highly-programmable measurement systems capture a host of parameters associated with equipment, on-line process material and environmental variables.

DEVICE TRACEABILITY

Each Micron device can be traced to its original fabrication lot through an alphanumeric code inscribed on both the top and bottom of the package. Alphanumeric codes are maintained in our computer network and can be assessed from any computer terminal. The system user can request information relative to a particular scribe or series of scribes. Information provided by the system includes: the lot number associated with each scribe specified, the date and time that the lot was inscribed and the part type associated with the lot. If the scribe number is not readily available, this same information can also be requested by entering a specific lot number or lot number series, or by specifying the date and time that a device or lot of interest was inscribed.

In addition to the package scribe, we are in the process of adding a laser mark to each individual die on the wafer. This new laser mark will provide a level of traceability yet unmatched in the industry by identifying the location of the parent wafer within the fabrication lot as well as the precise location of the die on the wafer. This complete traceability will provide significant advantages in analyzing reliability issues and further enhance our ability to continuously improve product performance.

STATISTICAL TECHNIQUES AND TOOLS

By using highly flexible, on-line data extraction programs, system users can tap this vast data base and design their own correlation and trend analyses. Because we can correlate process variables to product performance, we can make on-line projections of the quality of our finished product for a given lot or process run. In addition, we can estimate the impact of process improvements on quality well in advance and can make the impact of process deviations more visible to our engineers. This approach allows us to model yield and quality parameters based on on-line parameters. We then use this model to predict the final product results through the following means.

GROUP SUMMARIES

Summaries, which provide the means and standard deviations of user-defined parametrics, enable system users to compare the parametric values of production lots as well as special engineering lots.

TREND ANALYSIS

Trend charts are routinely generated for critical parameters. System users can plot the means and ranges of any probe or parametric data captured throughout the manufacturing process.

CORRELATION ANALYSIS

Correlation analysis can be performed on any combination of factors such as equipment, masks or electrical parameters. One report, regularly produced and disseminated to key personnel, takes two groups of lots (one with a high failure rate, the other with a low failure rate) and identifies all the pieces of equipment that are common to one or the other group. The report quickly alerts us to any correlation between a lot with a high failure rate and particular pieces of equipment in the wafer fabrication or assembly areas.

Another regularly produced report analyzes a user-selected set of database parametrics against an index, such as manufacturing yield. Lots are divided into three subgroups (upper yielding, middle yielding and lower yielding). The report then correlates the yields with all electrical parametric values taken on individual lots at wafer sort. It helps us determine which processing step may have caused the yields to vary among the three subgroups.

STATISTICAL PROCESS CONTROL CHARTS

Micron employs SPC control charts throughout the company to monitor and evaluate critical process parameters, such as critical dimensions (CDs), oxide thickness, chemical vapor depositions (CVDs), particle counts, temperature and humidity, and many other critical process and product quality parameters.

OVERLAYS OR WAFER MAPS

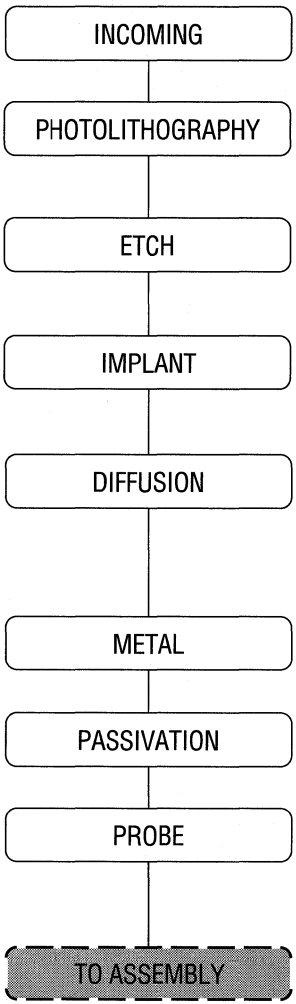
Maps, which are produced for all wafers during probe, show various parameters as a function of position on the wafer and are very useful for problem isolation. Maps may be analyzed individually or in groups. For example, wafers from an entire lot may be analyzed in relation to one particular parameter.

RS/1 DISCOVER/EXPLORE

This analysis software is used for experimental design, and evaluation of results. The statistical approach supported by this software (*t* tests, ANOVA tables, multiregression analysis, etc.) has proven invaluable in reducing time expended for product development and for trouble shooting. It is also used to determine the relationships between process output and probe and parametric data. Using multiregression analysis, for example, we are able to determine the relationship between L effective and CD dimensions to the speed of a device.

The use of automation in data capture, analysis and feedback greatly enhances the flexibility and speed with which we can view all aspects of the manufacturing process. This effective data analysis and feedback system helps to reduce parametric deviations, improve margin to specifications, increase manufacturing yields and provide for more accurate fabrication output planning.

FABRICATION



Incoming

All starting material is verified for cleanliness, uniformity and compliance with Micron's specifications. Each wafer receives an individual laser scribe for total product traceability.

Photolithography

Wafers are coated with a layer of light-sensitive photoresist. Specified sections of the wafer are exposed by projecting ultraviolet light onto the wafer through a mask. The nonexposed photoresist hardens and becomes impervious to etchants.

Etch

The areas of the wafer not protected by the exposed photoresist are removed by either plasma (dry etch) or acid (wet etch). The photoresist is then cleaned ("stripped") off of the wafer, leaving a pattern in the exact design of the mask.

Implant

Wafers are bombarded with positively or negatively charged dopant ions, which are implanted into the silicon. This process changes electrical characteristics in selective areas of the silicon. This is called "doping," and forms conductive regions on the wafer.

Diffusion

Silicon dioxide, nitride and polysilicon layers are formed on the wafer during a number of high-temperature furnace processes. The wafers are exposed to various gases, which either react with the silicon, causing it to oxidize and form an SiO_2 layer, or react with each other, forming polysilicon and nitride deposits. These layers are patterned using photolithography, and form the layers of diodes, transistors and capacitors making up the circuit. High temperature furnaces are also used to introduce and diffuse dopants into the wafers.

Metal

A thin layer of aluminum or other metal is deposited and patterned, forming interconnections between various regions of the die.

Passivation

The fabrication process is completed by forming a final glass layer on the wafer. This layer protects the circuits from contamination or damage through the testing and packaging process flows.

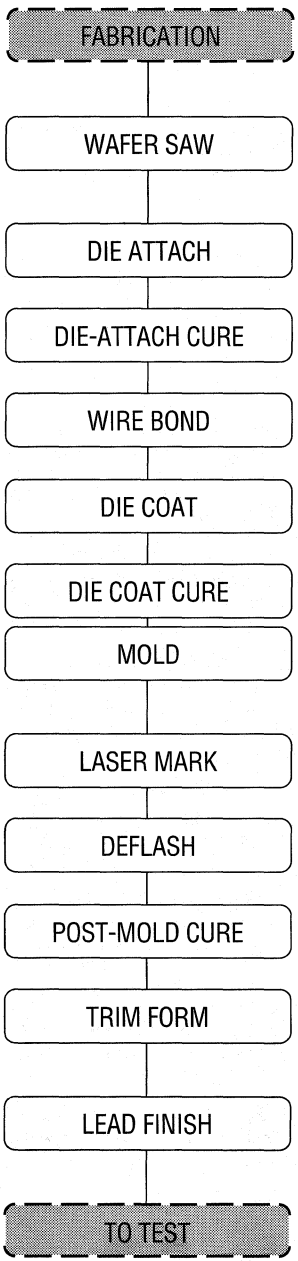
Probe

When the fabrication process is complete, each wafer consists of many "die." Each die on the wafer is taken individually through a series of tests. A computer attached to a probe card tests the die and produces a "wafer map" storing data on each functioning (good) die. All data is collected and stored for each die. Wafer maps are used in assembly to ensure that only good die are packaged.

Assembly

(See next page.)

ASSEMBLY



Fabrication
The fabrication process yields silicon wafers containing many discrete integrated circuits or die. Following fabrication, the wafers undergo assembly processing where the individual die are separated and encapsulated according to package specifications.

Wafer Saw
Wafers that have finished fab processing and probe are automatically mounted on a carrying film. The wafer is then sawed using an automated, high-speed diamond blade and high-pressure water. This separates each individual die from the others on the wafer without disturbing the carrying film.

Die Attach
With automated pick-and-place equipment, the good die as specified by the probe "wafer map" are removed from the carrier film. Each die is attached to a leadframe with a layer of adhesive.

Die-Attach Cure
To fully polymerize the die-attach adhesive, the die-attached leadframes are cured in an oven for two and one-half hours.

Wire Bond
With high-speed automated equipment, interconnections are made with gold wire (the diameter of a human hair). These interconnections are between the aluminum circuit on the die and the lead fingers of the leadframe.

Die Coat
Polyimide die coat is drop dispensed onto the wirebonded die. The die coat protects the surface of the die during the subsequent encapsulation step.

Die Coat Cure
To fully polymerize the die coat, the die coated leadframes are cured for six hours in an oven reaching 265°C.

Mold
A heated mold with a hydraulic press is used to transfer hot thermosetting plastic into mold cavities where the leadframe is placed. This encapsulation protects the die and the interconnections throughout the useful life of the product.

Laser Mark
A laser mark is scribed on the bottom side of the package. This mark is a code used to identify the assembly manufacturing lot.

Deflash
Prior to lead-finish processing, the leadframes are run through chemical baths to remove contaminants. This process is known as deflash.

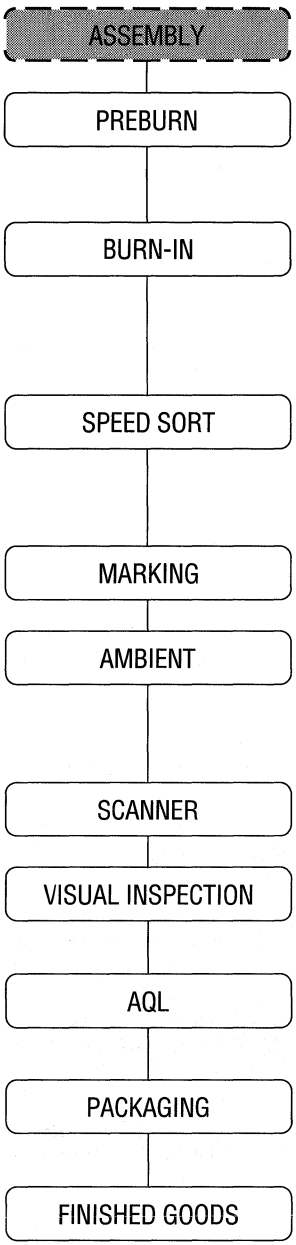
Post-Mold Cure
Molded leadframes are placed in an oven for four and one-half hours at 175°C to complete the polymerization of the epoxy encapsulant.

Trim/Form
A press-and-tool set is used to cut the leadframes, separating the encapsulated die into discrete devices and forming the leads into the appropriate shape for the package specified (ZIP and DIP packages for through-hole applications; SOJ, PLCC, and TSOP packages for surface-mount applications).

Lead Finish
The leads of each device receive a finish of tin/lead solder or tin/lead electroplating to ensure reliable application by the customer. If the leads receive an electroplated rather than solder finish, the lead-finish step is performed prior to the trim and form.

Test
(See next page.)

TEST



Assembly
Fully fabricated silicon wafers reach assembly after each die has been probed to screen out failures. Passing chips are then carried through a number of steps to become individual units in leaded packages.

Preburn
All testing is conducted at 125°C. Parametric tests are performed to detect opens, shorts, and input/output leakage and to determine whether standby/operating currents are within specified limits. Functional tests include low and high Vcc margin and vbump. Patterns performed include march, scan and address complement. Backgrounds used include solids and checkerboard. The specific tests performed depend upon the product being tested.

Burn-In*
Micron uses its exclusive AMBYX intelligent burn-in and test system to screen out infant mortalities. Devices are dynamically burned-in using checkerboard/checkerboard complement patterns in four intervals under the following conditions: 125°C, 7.5V Vcc for the first three intervals and 125°C, 6V Vcc for the final interval. Functional testing is performed at 85°C and back to 25°C AMBYX tests for thermal intermittent opens. Devices are also functionally tested at burn-in conditions (125°C, 7.5V) at the beginning of the burn-in cycle to verify that the devices under test are being properly exercised.

Speed Sort
Parametric and functional testing is conducted at 86°C. Parametric tests are performed to detect opens, shorts, and input/output leakage and to determine whether voltage input/output high and low levels and standby and operating currents are within specificed limits. Functional tests include low/high Vcc margin and vbump and access tests. Patterns performed include march, scan and address complement. Backgrounds used include solids and checkerboard. The specific tests performed depend upon the product being tested.

Marking
Devices are marked with ink with the following information: year, special process designator, part type, package type and speed grade.

Ambient
All testing is conducted at 25°C. Parametric tests are performed to detect opens, shorts, and input/output leakage. These tests also determine whether high and low levels of voltage input and output as well as standby and operating currents are within specified limits. Functional tests include low and high Vcc margin and vbump. Patterns performed include march, scan and address complement. Backgrounds used include solids and checkerboard. The specific tests performed depend upon the product being tested.

Scanner
Devices are optically scanned by an automated scanning machine for bent leads, incorrect splay, coplanarity failures and tweeze failures. Passing and failing parts are then sorted into appropriate bins.

Visual Inspection
All devices, now tested to be functional, are visually inspected for cosmetic defects such as bent leads, poor marks, broken packages and poor solder. Defective products are removed and repaired if possible. Data on the type of defects found is carefully recorded and used for improving the manufacturing processes in both assembly and test.

AQL
A quality assurance monitoring program oversees the electrical and mechanical performance of all production lots. New products that have not met required production volume and parts per million (ppm) levels are held at this stage until it is confirmed that electrical and environmental test results meet Micron requirements.

Packaging
Devices are prepared for shipping. They may remain in tubes or they may be mechanically placed in tape-and-reel packages, ready for application in automatic pick-and-place machines. Products will be either dry packed in vacuum sealed bags with a desiccant, or placed in black antistatic bags.

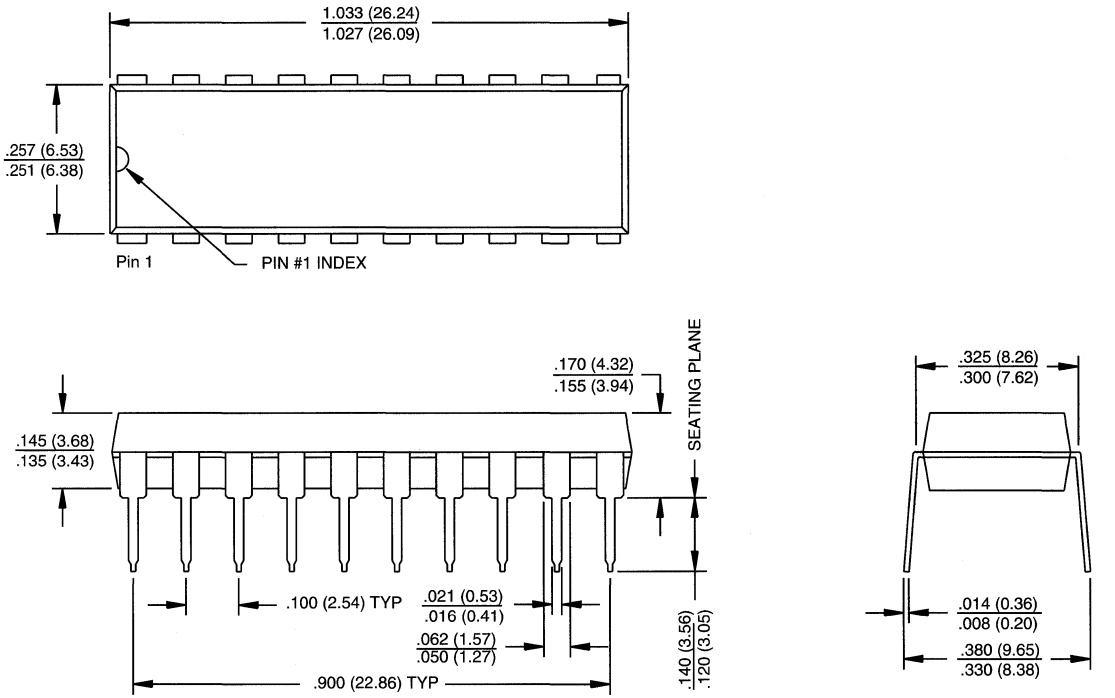
Finished Goods
Devices are shipped through a system that maintains lot identity.

*Voltage levels will vary depending upon the product being tested (for example, standard 5V product vs 3.3V product).

MICRON
SEMICONDUCTOR, INC.

20-PIN PLASTIC DIP

SA-1

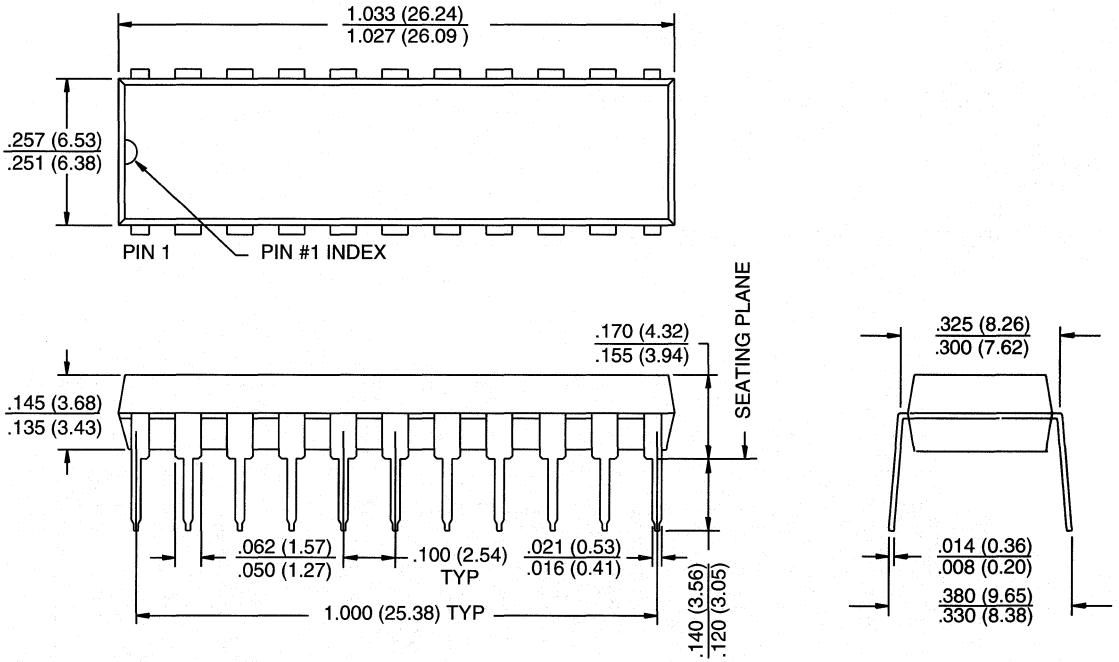


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

22-PIN PLASTIC DIP

SA-2

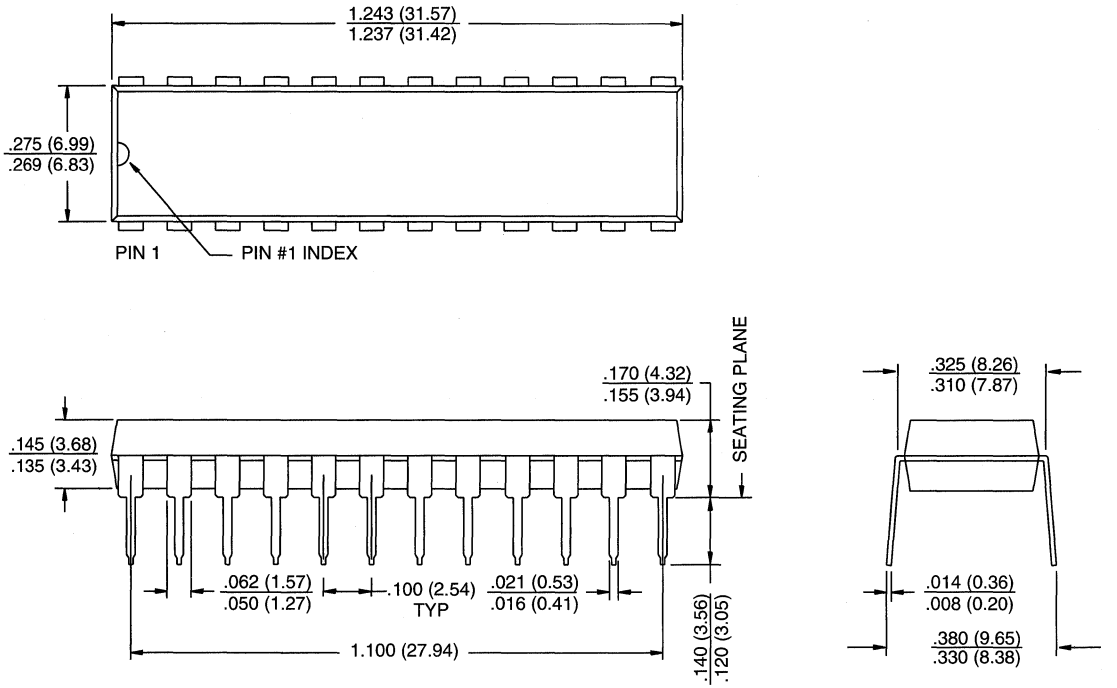


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

24-PIN PLASTIC DIP

SA-3



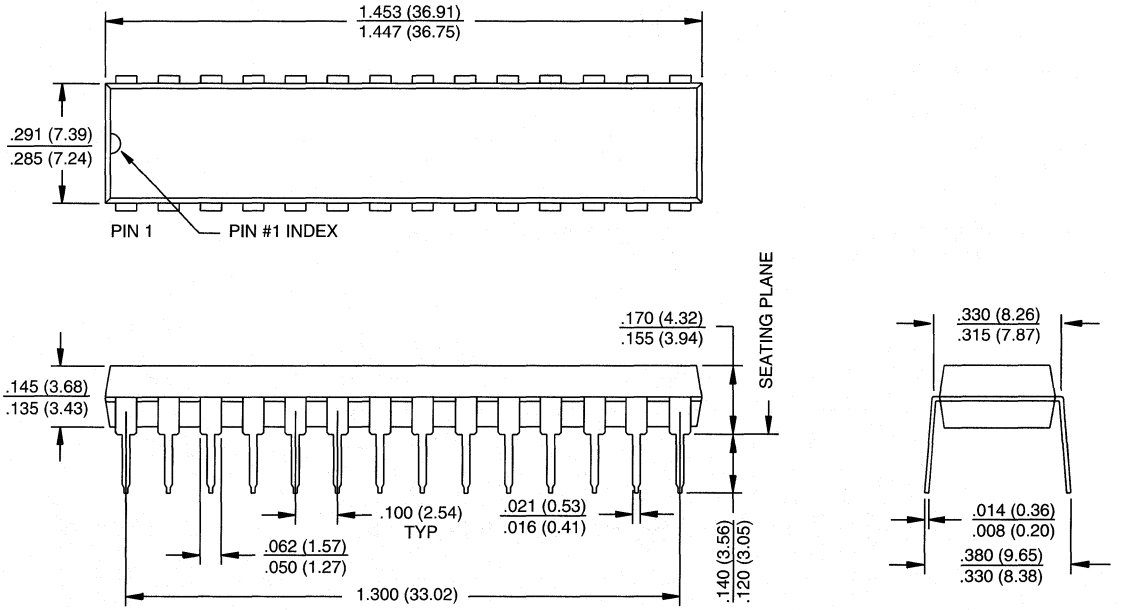
PACKAGE INFORMATION

NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

28-PIN PLASTIC DIP

SA-4

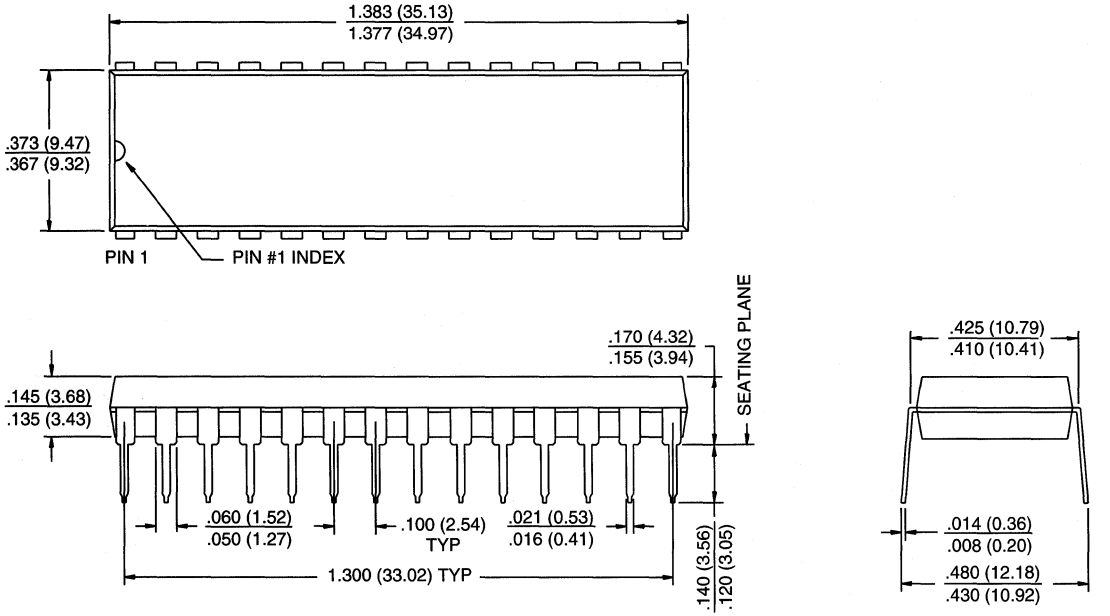


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

28-PIN PLASTIC DIP

SA-5

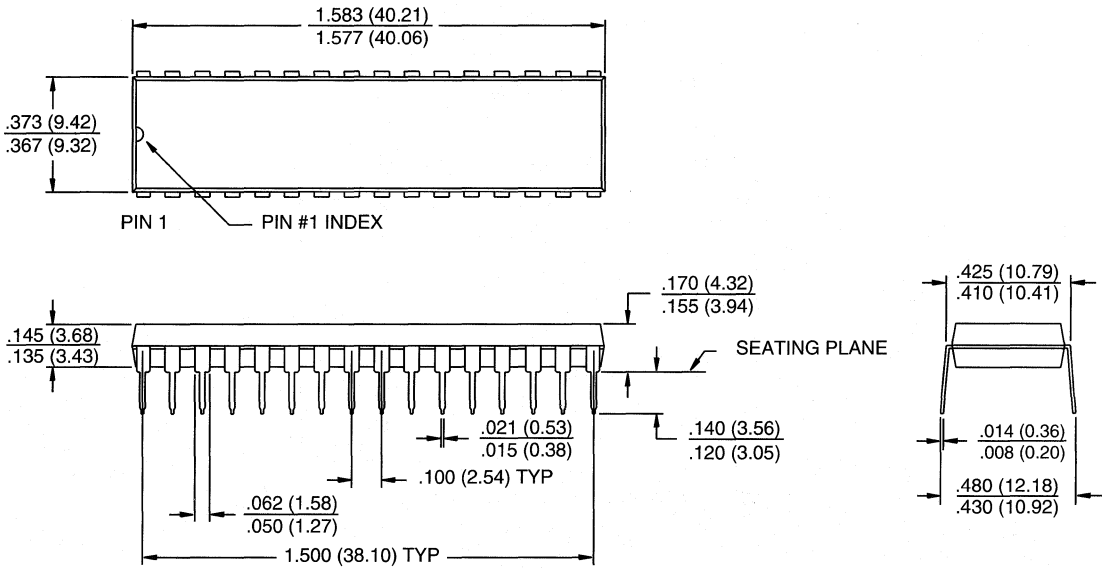


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

32-PIN PLASTIC DIP

SA-6

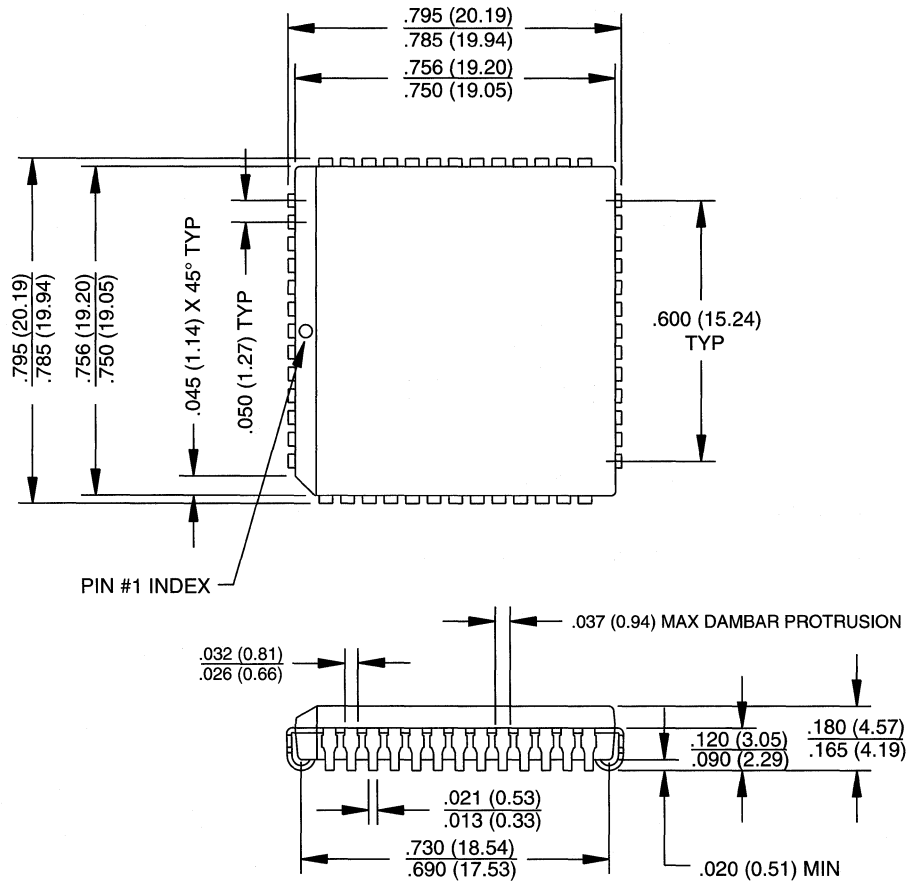


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

52-PIN PLCC

SB-1

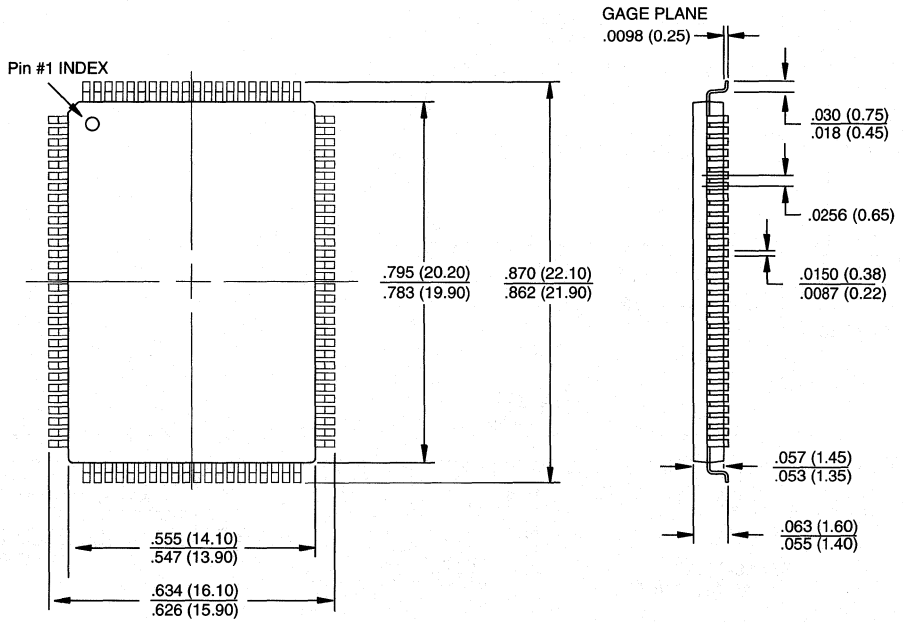


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

100-PIN TQFP

SC-1

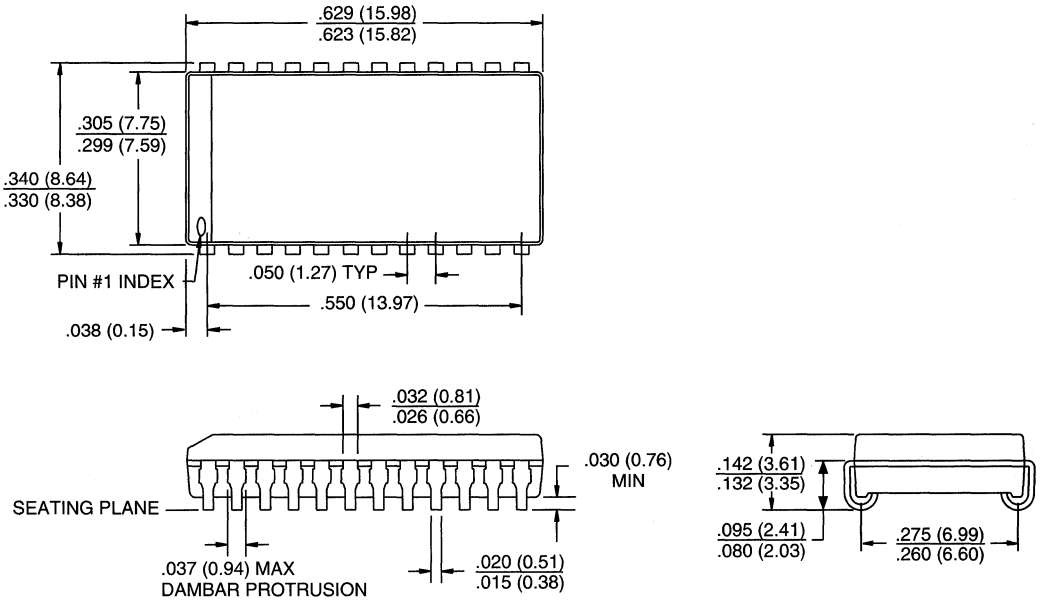


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

24-PIN PLASTIC SOJ

SD-1

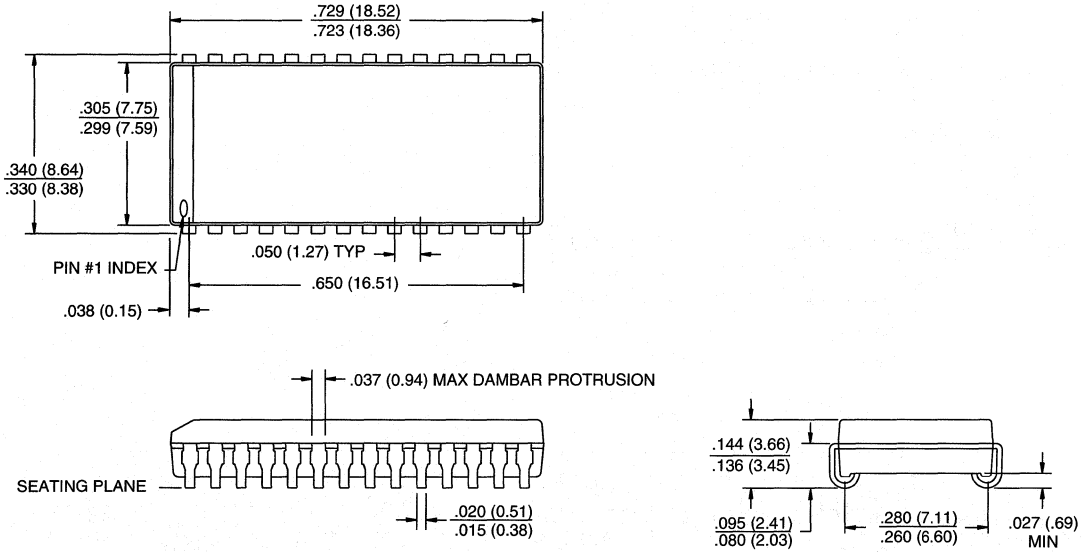


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

28-PIN PLASTIC SOJ

SD-2

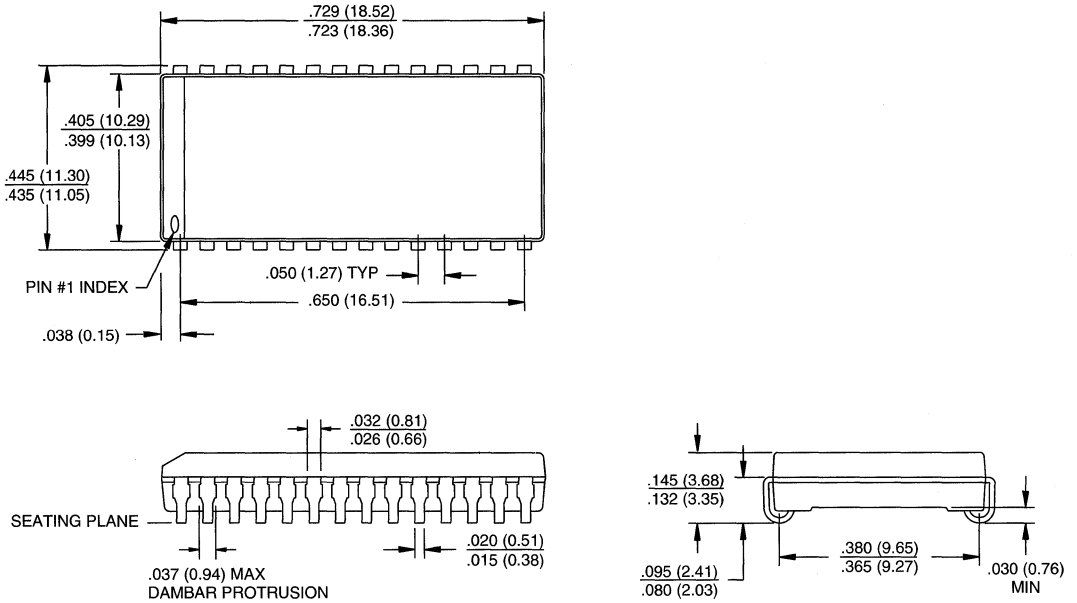


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

28-PIN PLASTIC SOJ

SD-3

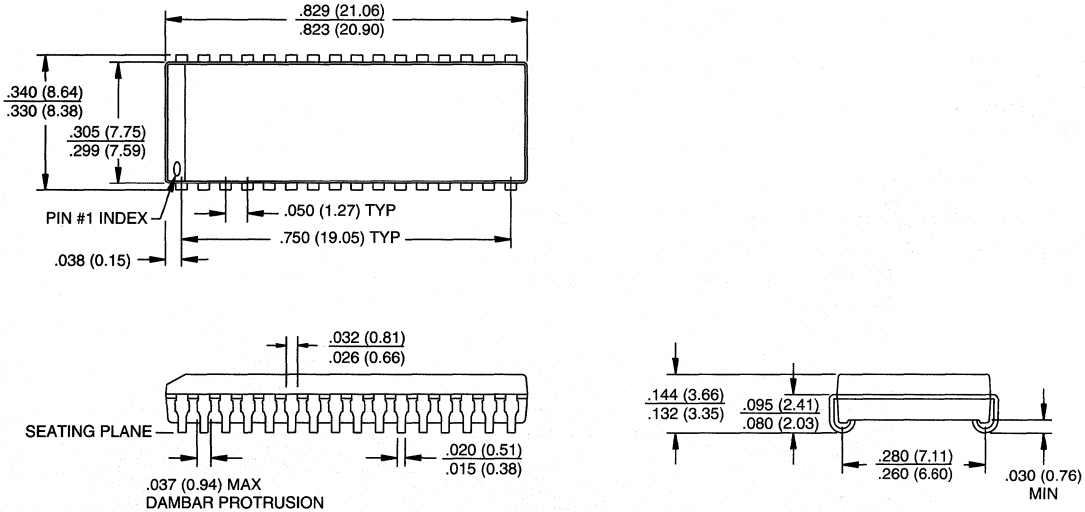


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

32-PIN PLASTIC SOJ

SD-4

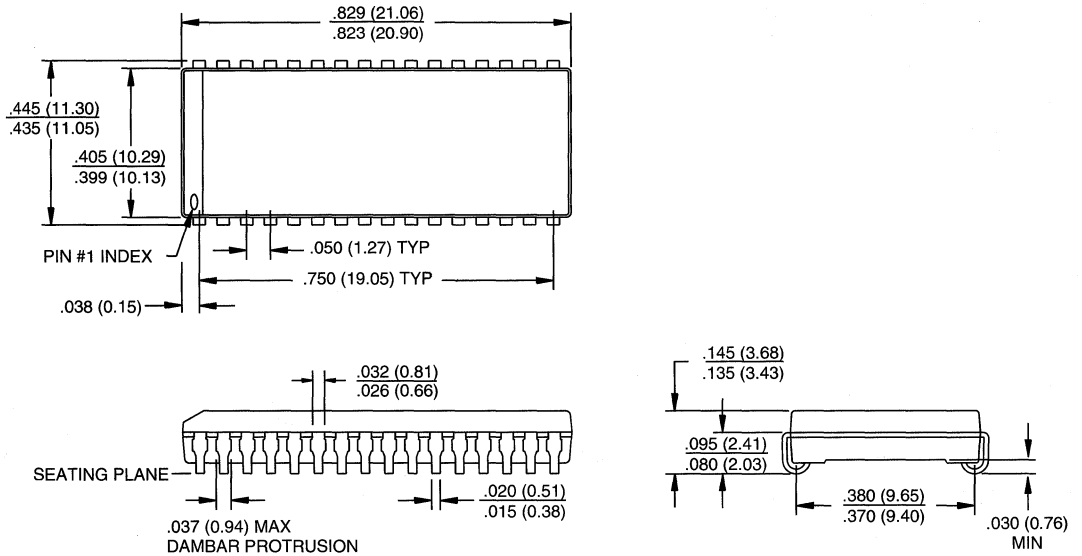


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

32-PIN PLASTIC SOJ

SD-5

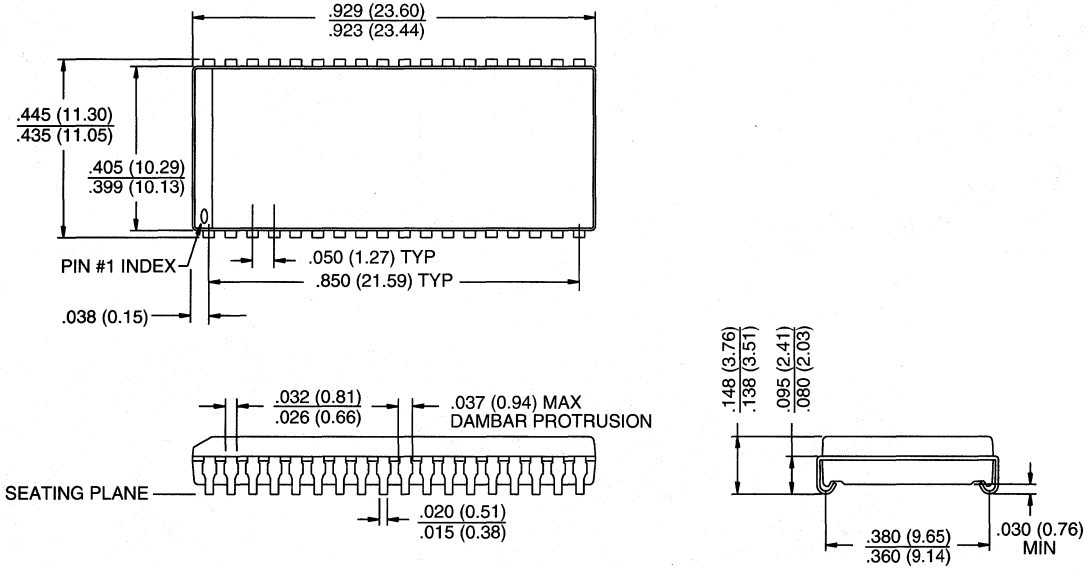


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

36-PIN PLASTIC SOJ

SD-6

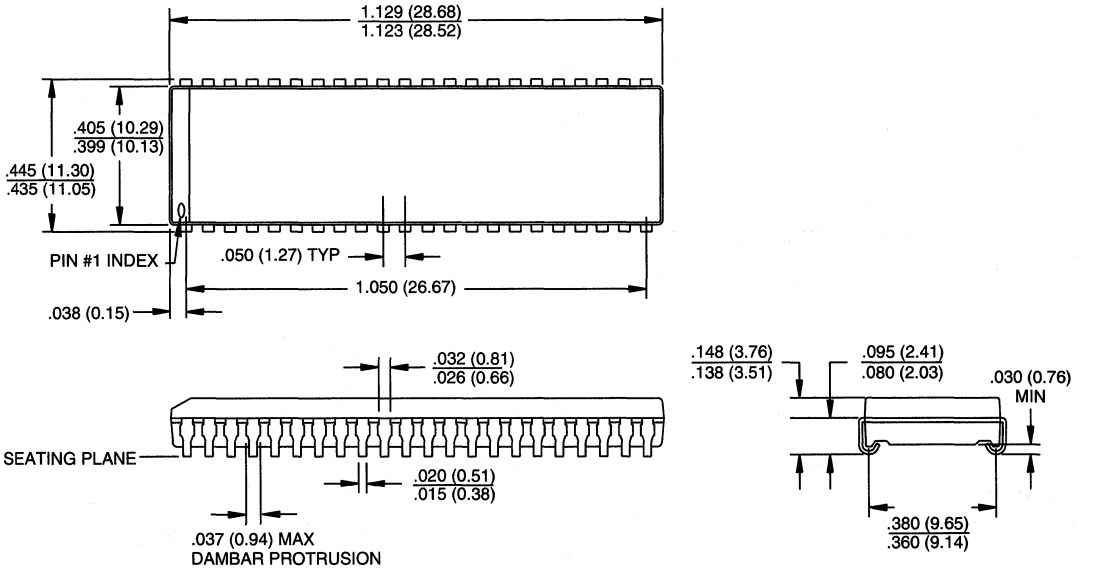


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

44-PIN PLASTIC SOJ

SD-7

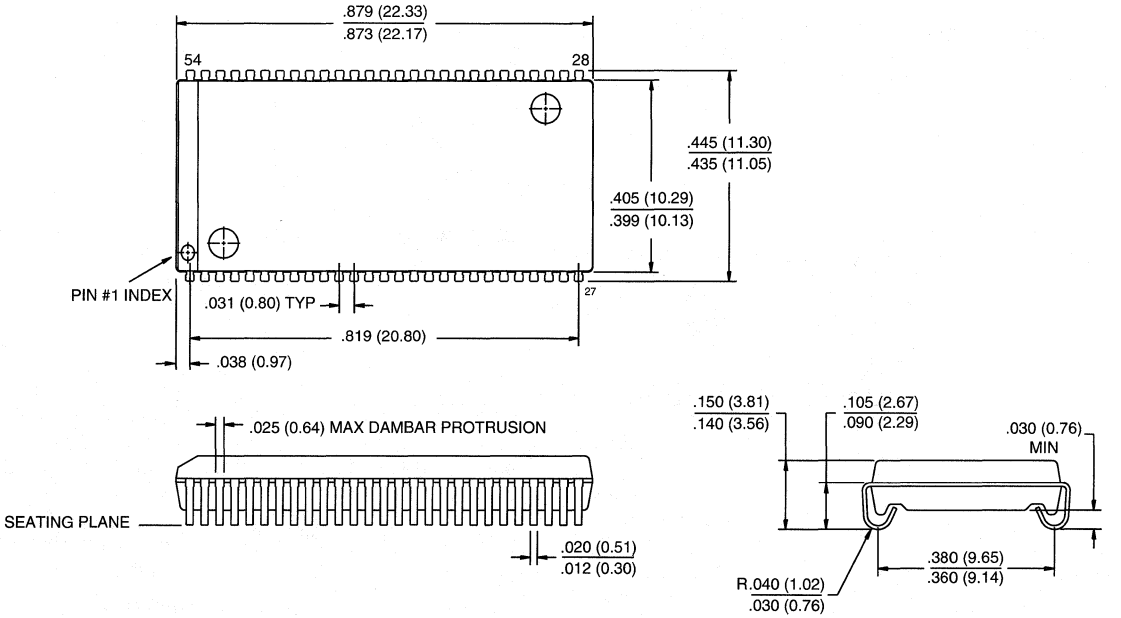


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

54-PIN PLASTIC SOJ

SD-8

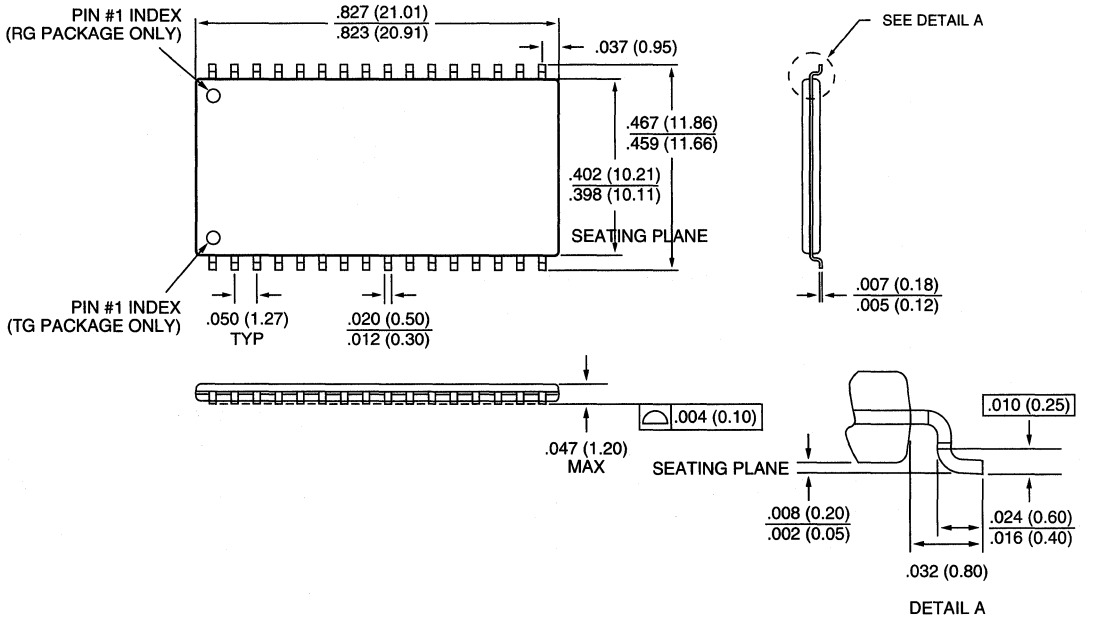


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

32-PIN PLASTIC TSOP

SE-1

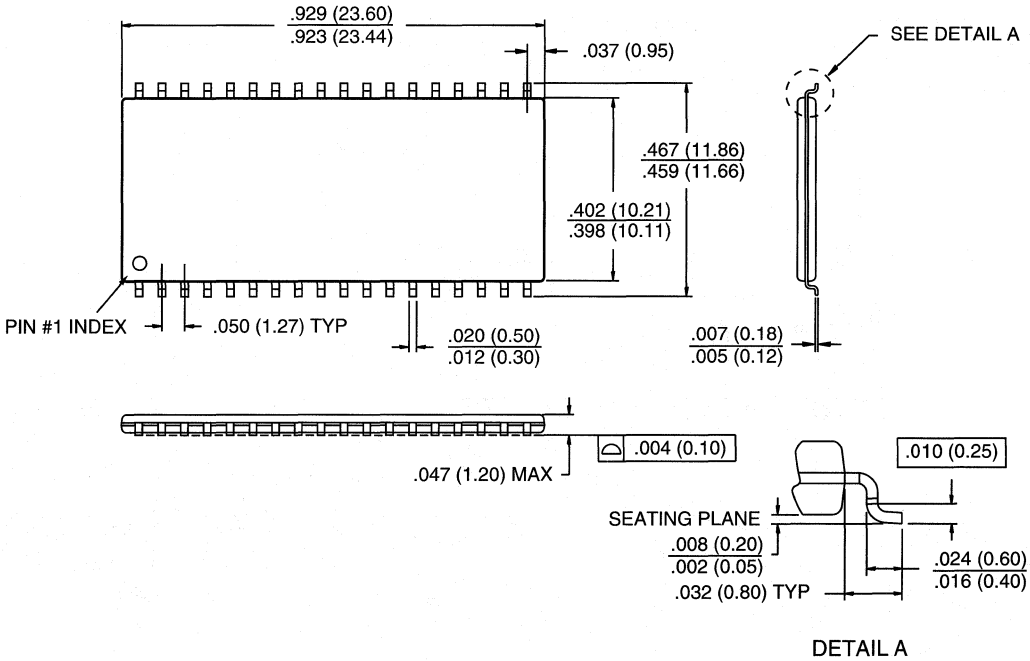


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

36-PIN PLASTIC TSOP

SE-2

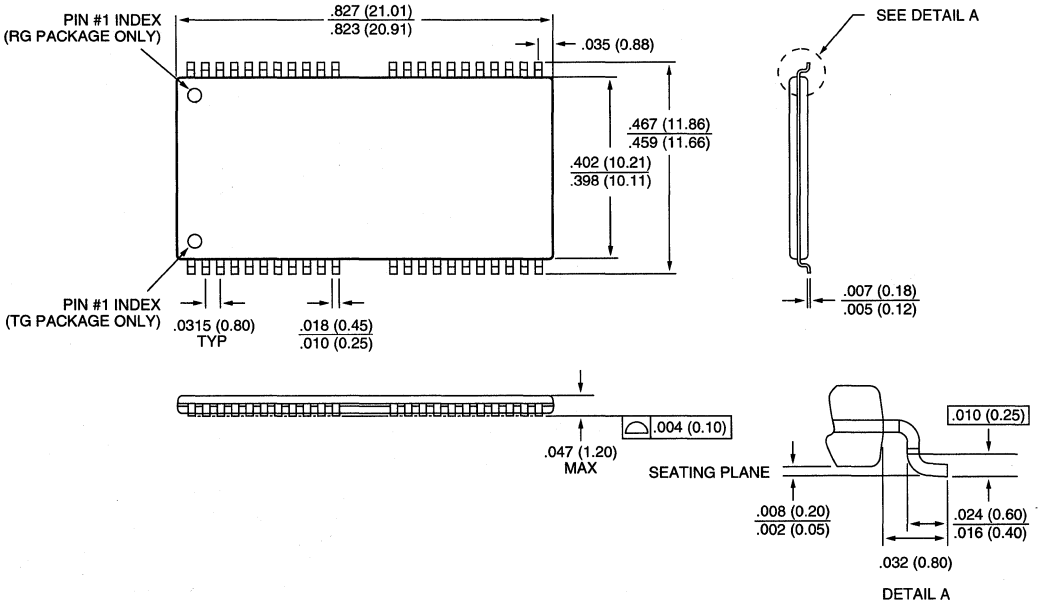


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

44/50-PIN PLASTIC TSOP

SE-3

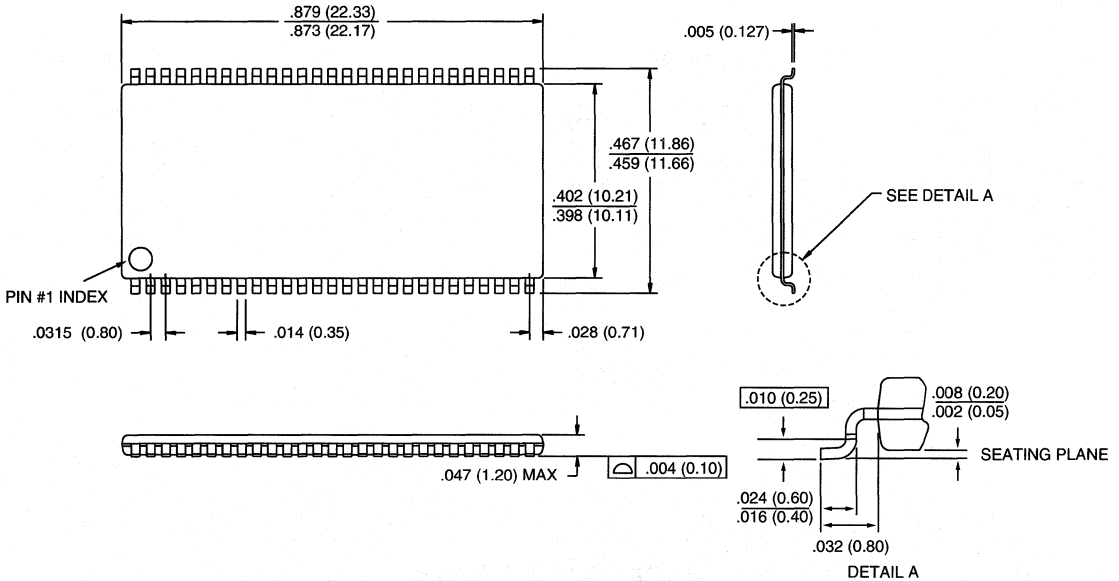


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

54-PIN PLASTIC TSOP

SE-4

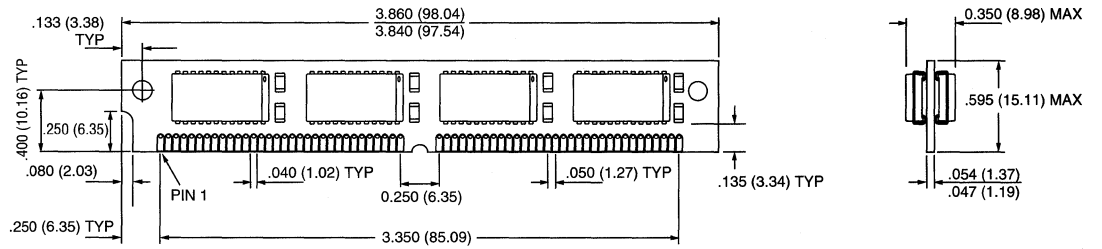


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

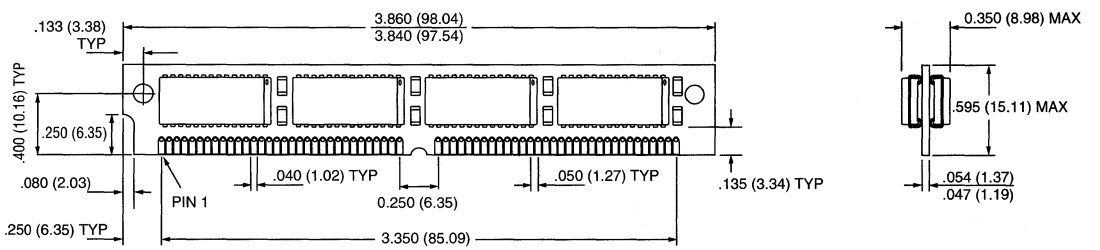
64-PIN MODULE SIMM

SF-1



64-PIN MODULE SIMM

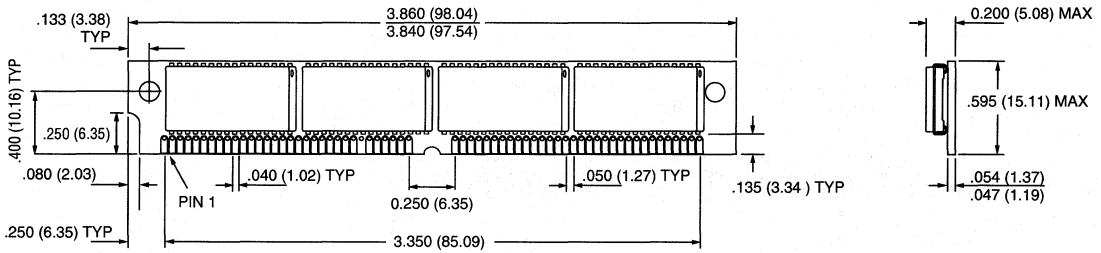
SF-2



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

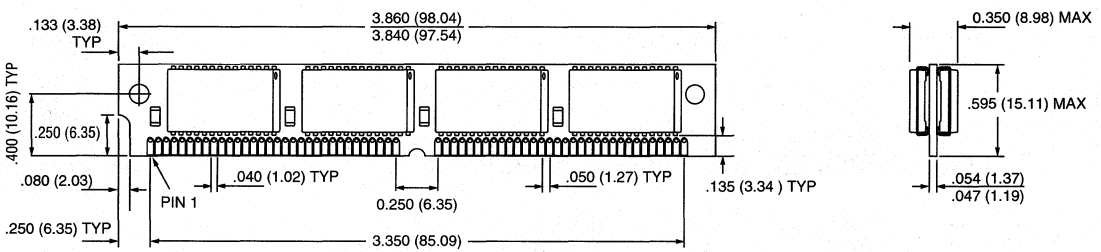
64-PIN MODULE SIMM

SF-3



64-PIN MODULE SIMM

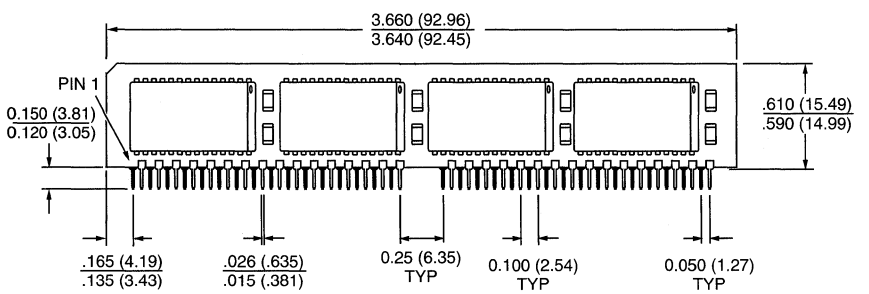
SF-4



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

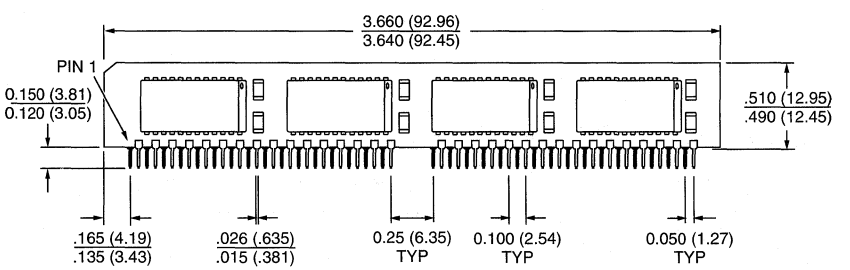
64-PIN MODULE ZIP

SG-1



64-PIN MODULE ZIP

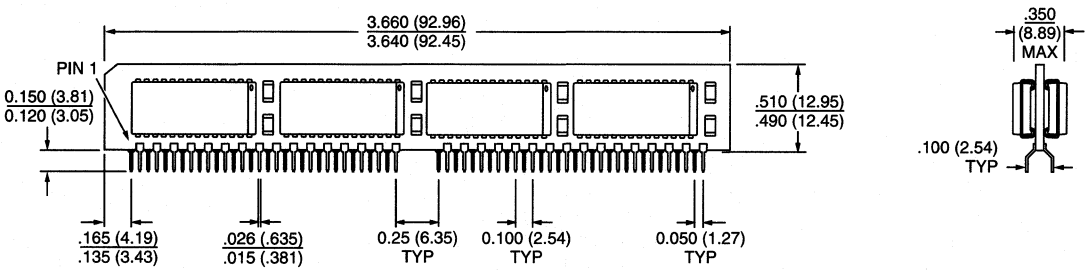
SG-2



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

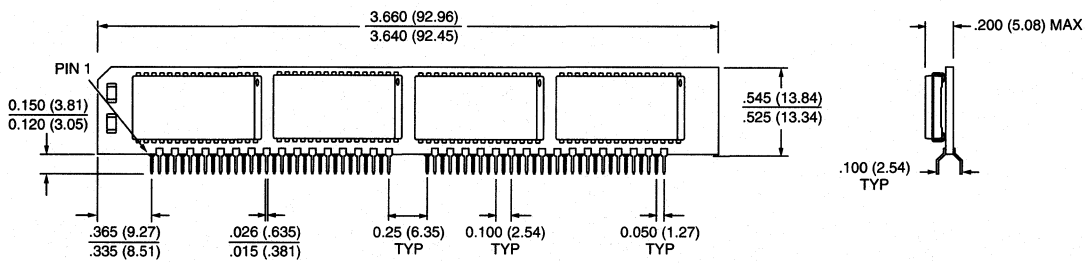
64-PIN MODULE ZIP

SG-3



64-PIN MODULE ZIP

SG-4



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

MICRON
SEMICONDUCTOR, INC.

CUSTOMER SERVICE NOTE

STANDARD SHIPPING BAR CODE LABELS

INTRODUCTION

Effective July 1, 1991, Micron implemented new standard bar coding labels that will accompany all shipments. These labels conform to EIA Standard 556.

Samples and tape-and-reel boxes will have their own individual bar code labels (see CSN-02). The bar code labels will allow customers to scan individual Micron containers for quick order verification. Figure 1 shows an example of the standard bar coding label.

BAR CODE INFORMATION

The information provided on the label is:

(S) — Serial: Individual box serial number

(13Q) — Special: Individual box number and total number of boxes in the shipment (example: 2 of 10)

(Q) — Quantity: Total quantity of parts in the box

(K) — Trans ID: Customer purchase order number

(P) — Customer Product ID: Customer part number

If a customer part number is not designated, the Micron part number will be printed.

ADDITIONAL SALES INFORMATION

Ship-to-Name: Customer's name and ship-to address

Ship-From-Name: Micron name and address

Lot Date Code: Indicates date of oldest lot in the box

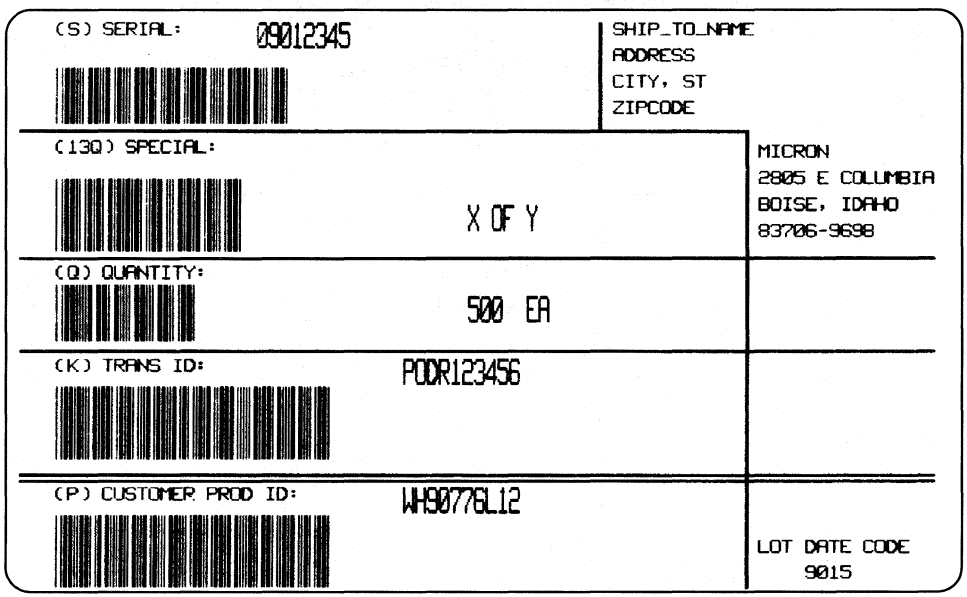


Figure 1
STANDARD BAR CODE LABEL

CUSTOMER SERVICE NOTE

TAPE-AND-REEL/SAMPLE BAR CODE LABELS

INTRODUCTION

Micron provides a standard bar code label on each individual sample and tape-and-reel box. The standard bar code label allows scanning of Micron shipping containers at a receiving dock for quick order verification.

Figure 1 shows an example of the standard bar code label.

BAR CODE INFORMATION

The information provided on the label is:

Label 1: Individual box number (in a multibox shipment)
Actual box number printed
Micron part number/speed/customer code
Part type/rev/quantity/date code of oldest lot*.

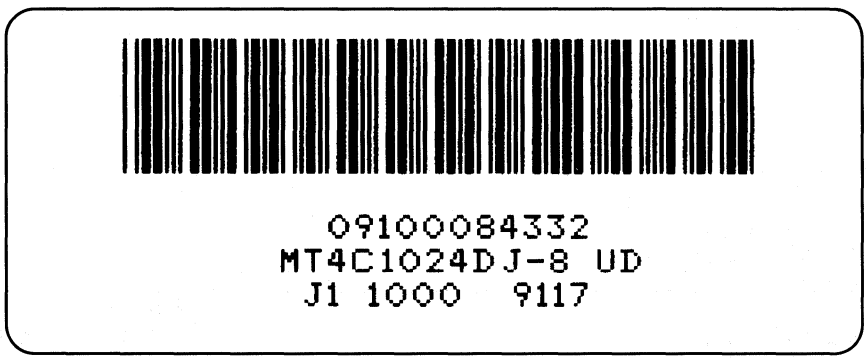


Figure 1
LABEL 1

*Indicates that more than one date code is contained on the reel.

CUSTOMER SERVICE NOTE

SURFACE-MOUNT PRODUCTS' SPC LABELS

INTRODUCTION

On November 15, 1991, Micron began providing a new SPC label on all surface-mount products. The label is attached to the static-proof bag for products packaged in tape-and-reel as well as tubes.

Figure 1 shows an example of the standard SPC label, while Figures 2 and 3 show the difference between the labels for tubed and tape-and-reel packaged products.

DATE INFORMATION

The SPC label includes the date on which the tube or reel was hermetically sealed in drypack. It also lists the ID number of the operator who sealed the product.

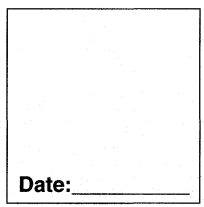


Figure 1
SURFACE-MOUNT PRODUCT SPC LABEL

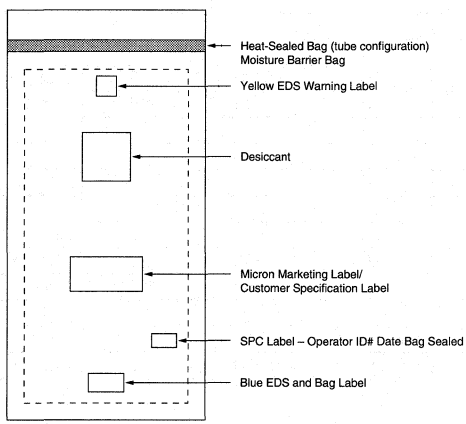


Figure 2
TUBED PRODUCT LABEL

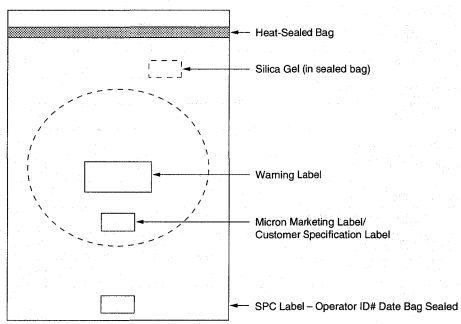


Figure 3
TAPE-AND-REEL PACKAGED PRODUCT LABEL

SALES INFORMATION

CUSTOMER SERVICE NOTE

BOX AND TAPE-AND-REEL QUANTITY AND WEIGHT CHART

INTRODUCTION

Micron encourages customers to place orders in increments of standard box, tray and reel quantities whenever possible. The chart below will help determine order quantities.

ADDITIONAL SALES INFORMATION

Benefits to Micron's customers by ordering in standard quantities:

1. Cost Savings—it is less expensive to send a shipment containing full boxes.
2. Process Control—Micron's production tracking system automatically checks speeds, revs, customer codes and quantities. When standard box quantities are ordered, manual errors are eliminated, thus ensuring error-free shipments.
3. Lot Integrity—lot integrity is kept in tact when box quantities are not broken up.
4. Fewer returns—fewer errors equal fewer complaints and returns.

Part Type	Quantity Per Tray	Quantity Per Box	Lbs Per Box	Quantity Per Tube	Tape-&-Reel Quantity	Lbs Per Reel	Tape Size
SRAM 16K							
MT5C1601-1608		1500	9.9	15			
MT5C1601DJ-1608DJ		4000	12.7	25	1000	4.0	24mm x 12mm
SRAM 64K							
MT5C6401-6407		1500	9.9	15			
MT5C6408		1000	9.9	10			
MT5C6401DJ-6408DJ		4000	12.7	25	1000	4.0	24mm x 12mm
SRAM 256K							
MT5C2561-2564		1500	9.9	15			
MTC2565-2568		1000	9.9	10			
MT5C2561DJ-2568DJ		4000	12.5	25	1000	3.9	24mm x 12mm
MT5C2889DJ		2000	10.5	20	1000	4.5	32mm x 12mm
MT5C2568Z		1300	10.1	13			
SRAM 1 Meg							
MT5C1001, 1005		500	6.5	10			
MT5C1008		500	7.8	10			
MT5C1001DJ-1005DJ		2000	11.5	25	500	3.5	32mm x 16mm
MT5C1008DJ		2000	11.5	20	500	3.5	44mm x 16mm
MT5C1189DJ		2000	11.5	20	500	3.5	44mm x 16mm
SYNCHRONOUS SRAMs							
MT58C1618LG	119	1000	5.0				
MT58C1289DJ		2000	9.9	20	500	3.5	44mm x 16mm

CUSTOMER SERVICE NOTE

ENVIRONMENTAL PROGRAMS

INTRODUCTION

Environmental issues such as the depletion of the ozone layer by chlorofluorocarbons (CFCs) affect everyone. Micron Semiconductor, Inc., takes a proactive approach to eliminating hazardous and polluting chemicals by educating and involving our workforce in their removal. We have eliminated ozone-depleting chemicals (ODCs) from the manufacturing process. Micron is in full compliance with Section 611 of the Clean Air Act and does not have to label any product to the contrary. We believe a proactive approach to environmental responsibility is not only environmentally advantageous, but gives the company a long-term competitive advantage.

COMPLETED TEAM PROJECTS

WET SIDE ECONOMIZER

This system, developed by Micron engineers in 1987, saves the company $150,000 annually. The Wet Side Economizer uses cold air rather than refrigeration to cool the manufacturing complex. This system reduces kwh consumption by 15.1 million, which translates into a 11,174-ton reduction in CO^2 emissions, a 121-ton reduction in SO^2 emissions, and a 53-ton cut in NO_x emissions. The system earned Micron a Certificate of Recognition for Energy Consciousness from the state of Idaho and an award for Energy Innovation from the federal Department of Energy in 1991.

AQUEOUS CLEANING

Micron's Custom Manufacturing Services group researched the possibility of switching from solvent-based CFC cleaners to aqueous (water only) cleaning in early 1990. The group eliminated all CFC-based solvents in October 1991 and discovered that the new aqueous cleaning process proved more effective and cheaper than the solvent-based process.

REFRIGERANTS

Micron's Plant Operations group has installed high-efficiency purge pumps that exceed EPA specifications on refrigeration units in order to eliminate the discharge of refrigerants into the atmosphere. In addition, portable refrigerant reclaim units are used to recover and recycle refrigerants during maintenance or when equipment is retired.

FIRE EXTINGUISHERS

Micron eliminated the use of all halon fire extinguishers in 1993. They were replaced with more environmentally safe units according to their application. The quick elimination of ozone-depleting chemicals such as halon saves the company money because the price of these chemicals goes up as manufacturers discontinue their production.

WATER TREATMENT FACILITY

During the past year, Micron has allocated $10 million for the first phase of a new industrial waste water pretreatment facility. The facility is designed to reclaim process waste waters and reduce ground water usage by 50 percent in the first phase. The final $5 million phase, scheduled for completion in 1997, will reduce ground water use by 80 percent.

RECYCLING

Several Micron teams have developed systems to recycle items for sale to outside customers or reuse within the manufacturing process. These items include sulfuric acid, gold, various solvents and alcohols, scrap metal, wire, aluminum and steel cans, buckets and barrels, pallets, plastic, and cardboard and paper products.

GLYCOL ETHER ELIMINATION

Micron has instituted a program to eliminate glycol ethers, which have been implicated as reproductive toxins.

ONGOING TEAM PROJECTS

VOLATILE ORGANIC COMPOUNDS (VOCS)

The goal of this team project is to reduce VOC emissions by 90 percent within one year.

HAZARDOUS AIR POLLUTANTS

This project focuses on reducing the use of MEK, acetone, toluene and methanol by 90 percent by the spring of 1994.

HAZARDOUS WASTE REDUCTION

This ongoing team focuses on reducing all hazardous wastes. Chemical usage is screened and chemicals containing toxic substances are included on a "hit list." The team works to reduce or eliminate the use of these hit list chemicals. If the chemical cannot be immediately eliminated,

team members work with lab staff, plant operations, and production engineering to find substitutes for the chemicals that contain the toxic substances.

POLLUTION ABATEMENT

Micron is working with a start-up company on a new approach to abating organic compounds. Our chemistry group also continuously reviews existing abatement technologies.

ENVIRONMENTAL BENCHMARKING

The benchmarking team reviews environmental programs that are successful in other semiconductor facilities and develops a shared network of information.

SUPPLIER ASSISTANCE

Micron offers assistance to suppliers to help eliminate toxic substances in chemicals or products they provide. A Micron team is currently working with suppliers to eliminate perfluorinated compounds that contribute to global warming.

COMMUNITY ASSISTANCE

Micron volunteers lab resources and provides consultation to local companies and community organizations, such as the Peregrine Fund, to help resolve industrial hygiene and environmental issues. Micron team members are active in local environmental and safety organizations and in the Community Emergency Planning Committee. They also periodically host training classes (such as Hazardous Gas Bottle Handling and Disposal) for local professional organizations.

CUSTOMER SERVICE NOTE

ELECTRONIC DATA INTERCHANGE

INTRODUCTION

Electronic Data Interchange (EDI) has become an important data transmission element in today's marketplace. Micron is ready to serve your EDI needs and encourages customer participation.

STANDARDS SUPPORTED

X.12

Micron supports versions 002000 through 003020 for all implemented transaction sets. The addition of new versions is an automated process which drives off of the standard diskettes available through Data Interchange Standards Association.

EDIFACT

Micron supports EDIFACT under the 90.1 EDIFICE guidelines for the Purchase Order (PO), PO Acknowledgment, PO Change and PO Change Acknowledgment messages.

TRANSACTION SETS

Inbound	Outbound
850 - PO	855 - PO Acknowledgment
860 - PO Change	865 - PO Change Acknowledgment
840 - Request For Quote (RFQ)	843 - Response to RFQ
830 - Forecast	856 - Advanced Ship Notice
846 - Inventory Inquiry/ Advice	810 - Invoice
867 - Product Transfer & Resale	
844 - Product Transfer Account Adjustment (PTAA)	849 - Response to PTAA
997 - Functional Acknowledgment	

VALUE ADDED NETWORKS

A T & T

A T & T allows our partners to transmit EDI documents via standard protocol or X.400 (e-mail protocol).

Advantis

Advantis is the result of a merger between the Sears and IBM networks.

TRANSMISSION TIMES

Transmission times are 2 a.m., 10 a.m., 1 p.m., 3 p.m. and 8 p.m. MST weekdays and 1 p.m. MST on weekends. Additional transmission times can be added easily as circumstances warrant.

MICRON EDI CONTACTS

EDI Project Leader	EDI Software Development
Becka Shirrod	Tony Holden
208-368-3338	208-368-3855

STEPS TO IMPLEMENTATION

The following are typical steps taken as Micron begins exchanging EDI data with a new trading partner:

- Micron receives an implementation guide from a trading partner
- Micron's EDI team contacts the trading partner's EDI coordinator to set up a trading partnership and coordinate the transmission and receipt of test documents
- Micron receives a test EDI document from the partner's VAN and responds with the necessary acknowledgments
- Once both parties agree everything is working properly, parallel testing with EDI and paper documents begins
- Micron insures an EDI agreement has been signed and returned to the trading partner
- Paper documents are replaced with EDI documents (full production).

CUSTOMER SERVICE NOTE

RETURN MATERIAL AUTHORIZATION (RMA) PROCEDURES

HOW TO RETURN PRODUCT TO MICRON

- Obtain an RMA number (see "How to Obtain an RMA" below).
- Package product taking all antistatic precautions.
- Write RMA number on outside of box for proper routing.
- Ship package prepaid to:
  Micron Semiconductor, Inc.
  Attn.: RMA Area
  2805 East Columbia Road
  Boise, ID 83706
- If RMA is being shipped from outside of the United States, please note that Boise, Idaho, is a customs port city; reference Port City Code 2907.

HOW TO OBTAIN AN RMA

NONFAILURE-RELATED RETURNS:

- If you buy direct, contact your Micron sales rep at 1-208-368-3900.
- If you buy through a Micron rep, contact that rep.
- If you buy through Distribution, contact the distributor.

Provide the Following Information:

- Micron part number, including speed and package
- Reason for return
- One of the following: PO number, invoice number, or sales order number
- One of the following: replacement parts, credit only, or refund

FAILURE-RELATED RETURNS AND/OR APPLICATION PROBLEMS:

- Contact Micron Application Engineering Department at 1-208-368-3900

Provide the Following Information:

- Micron part number, including speed and package
- Type of failure
- Name of engineer who witnessed failure or requested failure analysis report
- One of the following: PO number, invoice number, or sales order number
- One of the following: replacement parts, credit only, or refund

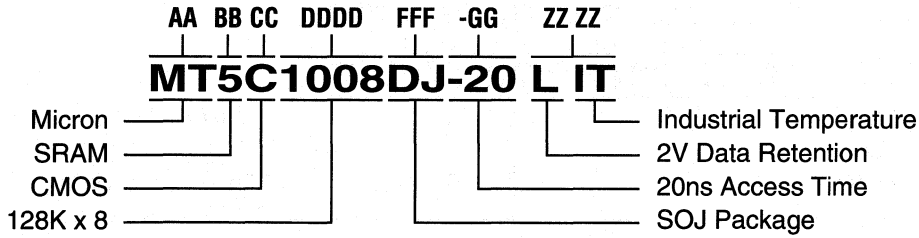
FAILURE ANALYSIS STANDARDS FOR RETURN MATERIAL AUTHORIZATIONS:

- Upon receipt of an RMA for failure analysis, Micron's Quality Assurance Department will provide an initial response within 48 hours.
- Micron's Quality Assurance Department will issue a completed failure analysis report within three weeks of receiving an RMA.

MICRON ACCOUNTING PROCEDURES FOR RETURN MATERIAL AUTHORIZATIONS

- Replacements: Replacement parts are shipped after receipt of the RMA parts. The credit memo will be applied directly to the replacement invoice; no new invoice will be sent as long as the invoice amount is equal to or greater than the credit memo amount. If this is not compatible with your accounts payable procedures, please advise your sales rep upon RMA request.
- Credit: A credit memo is sent out for the amount of the return upon arrival of the RMA parts. This credit memo number should be referenced when sending in payment information if intended to be used.
- Refund: A check request is submitted to Micron Accounts Payable upon receipt of RMA parts. A refund check is sent upon completion of the check request approval process.

CURRENT COMPONENT EXPANDED NUMBERING SYSTEM



AA – PRODUCT LINE IDENTIFIER

Micron Product ..... MT

BB – PRODUCT FAMILY

DRAM 4
DPDRAM (VRAM) 42
TPDRAM 43
SRAM 5
Synchronous SRAM 58

CC – PROCESS TECHNOLOGY

CMOS C
Low Voltage CMOS LC

DDDD – DEVICE NUMBER

(Can be modified to indicate variations)

DRAM ..... Width, Density
DPDRAM (VRAM) ..... Width, Density
TPDRAM ..... Width, Density
SRAM ..... Total Bits, Width
Synchronous SRAM ..... Density, Width

E – DEVICE VERSIONS

(Alphabetic characters only; located between D and F when required.)

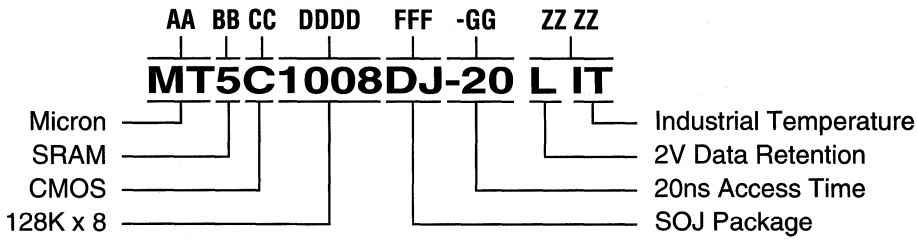
JEDEC Test Mode (4 Meg DRAM) ..... J
Errata on Base Part ..... Q

FFF – PACKAGE CODES

PLASTIC

DIP ..... Blank
DIP (Wide Body) ..... W
ZIP ..... Z
LCC ..... EJ
SOP/SOIC ..... SG
QFP ..... LG
TSOP (Type II) ..... TG
TSOP (Reversed) ..... RG
TSOP (Longer) ..... TL
SOJ ..... DJ
SOJ (Reversed) ..... DR
SOJ (Longer) ..... DL

CURRENT COMPONENT EXPANDED NUMBERING SYSTEM (continued)



GG – ACCESS TIME

-5	5ns or 50ns
-6	6ns or 60ns
-7	7ns or 70ns
-8	8ns or 80ns
-10	10ns or 100ns
-12	12ns or 120ns
-15	15ns or 150ns
-17	17ns
-20	20ns
-25	25ns
-35	35ns
-45	45ns
-50 (SRAM only)	50ns
-53	53ns
-55	55ns
-70 (SRAM only)	70ns

ZZ ZZ – PROCESSING CODES

(Multiple processing codes are separated by a space and are listed in hierarchical order.)

Example:
A DRAM supporting low power, extended refresh (L); low voltage (V) and the industrial temperature range (IT) would be indicated as V L IT.

Interim	I
Low Voltage	V

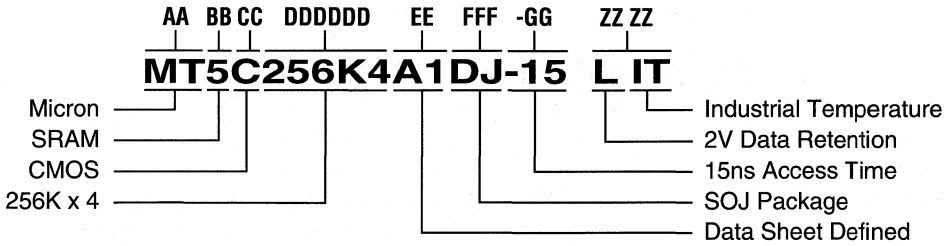
ZZ ZZ – PROCESSING CODES (continued)

DRAMs	
Low Power (Extended Refresh)	L
Low Voltage, Low Power (Extended Refresh)	VL
Low Power (Self Refresh)	S
Low Voltage, Low Power (Self Refresh)	VS
SRAMs	
Low Volt Data Retention	L
Low Power	P
Low Power, Low Volt Data Retention	LP
Low Voltage, Low Power	VP
Low Voltage, Low Volt Data Retention	VL
Low Voltage, Low Volt Data Retention, Low Power	VB
EPI Wafer	E
Commercial Testing	
0°C to +70°C	Blank
-40°C to +85°C	IT
-40°C to +125°C	AT
-55°C to +125°C	XT
Special Processing	
Engineering Sample	ES
Mechanical Sample	MS
Sample Kit*	SK
Tape-and-Reel*	TR
Bar Code*	BC

* Used in device order codes; this code is not marked on device.

SALES INFORMATION

NEW COMPONENT NUMBERING SYSTEM



AA – PRODUCT LINE IDENTIFIER

Micron Product ..... MT

BB – PRODUCT FAMILY

DRAM 4
DPDRAM (VRAM) 42
TPDRAM 43
Synchronous DRAM 48
SRAM 5
Synchronous SRAM 58

CC – PROCESS TECHNOLOGY

CMOS C
Low Voltage CMOS LC
BiCMOS ..... B
Low Voltage BiCMOS ..... LB

DDDDDD – DEVICE NUMBER

Depth, Width

Example:
1M16 = 1 megabit deep by 16 bits wide = 16 megabits of total memory.

No Letter ..... Bits
K ..... Kilobits
M ..... Megabits
G ..... Gigabits

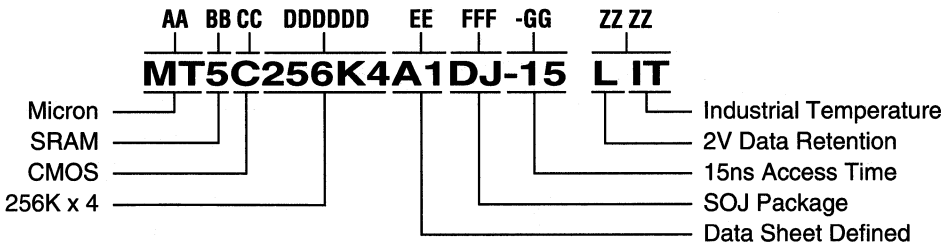
EE – DEVICE VERSIONS

(The first character is an alphabetic character only; the second character is a numeric character only.)
Specified by individual data sheet.

FFF – PACKAGE CODES

Plastic
DIP ..... Blank
DIP (Wide Body) ..... W
ZIP ..... Z
LCC ..... EJ
SOP/SOIC ..... SG
QFP ..... LG
TSOP (Type II) ..... TG
TSOP (Reversed) ..... RG
TSOP (Longer) ..... TL
SOJ ..... DJ
SOJ (Wide) ..... DW
SOJ (Reversed) ..... DR
SOJ (Longer) ..... DL

NEW COMPONENT NUMBERING SYSTEM (continued)



GG – ACCESS TIME

-5	5ns or 50ns
-6	6ns or 60ns
-7	7ns or 70ns
-8	8ns or 80ns
-9	9ns or 90ns
-10	10ns or 100ns
-12	12ns or 120ns
-15	15ns or 150ns
-17	17ns
-20	20ns
-25	25ns
-35	35ns
-45	45ns
-53	53ns
-55	55ns

ZZ ZZ – PROCESSING CODES

(Multiple processing codes are separated by a space and are listed in hierarchical order.)

Example:
A DRAM supporting low power, extended refresh (L); low voltage (V) and the industrial temperature range (IT) would be indicated as V L IT.

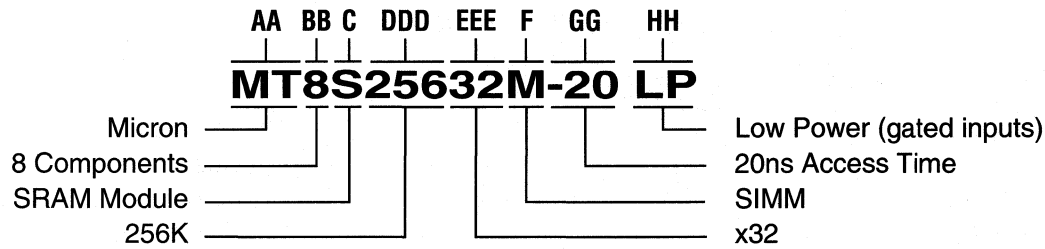
Interim	I
Low Voltage	V

ZZ ZZ – PROCESSING CODES (continued)

DRAMs	
Low Power (Extended Refresh)	L
Low Voltage, Low Power (Extended Refresh)	VL
Low Power (Self Refresh)	S
Low Voltage, Low Power (Self Refresh)	VS
SRAMs	
Low Volt Data Retention	L
Low Power	P
Low Volt Data Retention, Low Power	LP
EPI Wafer	E
Commercial Testing	
0°C to +70°C	Blank
-40°C to +85°C	IT
-40°C to +125°C	AT
-55°C to +125°C	XT
Special Processing	
Engineering Sample	ES
Mechanical Sample	MS
Sample Kit*	SK
Tape-and-Reel*	TR
Bar Code*	BC

* Used in device order codes; this code is not marked on device.

MODULE NUMBERING SYSTEM



AA – PRODUCT LINE IDENTIFIER
- Micron Product ..... MT

BB – NUMBER OF MEMORY COMPONENTS

C – RAM FAMILY
- SRAM ..... S
- DRAM ..... D
- 3.3V SRAM ..... LS
- 3.3V DRAM ..... LD

DDD – DEPTH

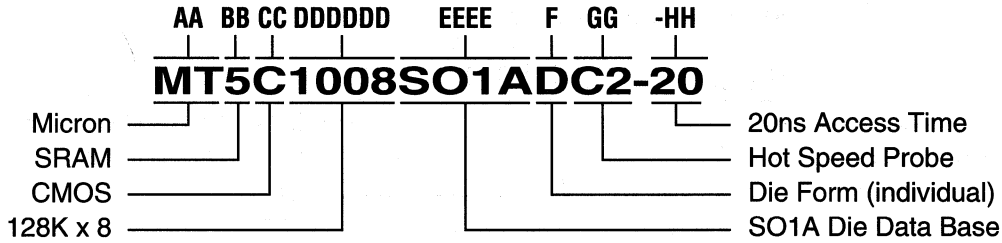
EEE – WIDTH

F – PACKAGE CODE
- DIP ..... D
- ZIP ..... Z
- SIMM ..... M
- SIP ..... N
- Gold SIMM ..... G

GG – ACCESS TIME
- -10 ..... 10ns
- -12 ..... 12ns
- -15 ..... 15ns
- -20 ..... 20ns
- -25 ..... 25ns
- -30 ..... 30ns
- -35 ..... 35ns

HH – SPECIAL DESIGNATOR
- Low Volt, Data Retention L
- Low Power (gated inputs) ..... LP

DIE PRODUCT NUMBERING SYSTEM



AA – PRODUCT LINE IDENTIFIER
Component Product ..... MT

BB – PRODUCT FAMILY
SRAM 5
DRAM 4
Synchronous SRAM 58
DPRAM (VRAM) 42

CC – PROCESS TECHNOLOGY
CMOS C
Low Voltage CMOS LC

DDDDDD – DEVICE NUMBER
When *no* alpha character appears as part of this section, the section is defined as:
DRAM ..... Width, Density
VRAM ..... Width, Density
SRAM ..... Total Bits, Width
Synchronous SRAM ..... Depth, Width

When an alpha character occurs as part of this section, the section is defined as:
Depth, Width

Example:
1M16 = 1 megabit deep by 16 bits wide = 16 megabits of total memory.

No Letter ..... Bits
K ..... Kilobits
M ..... Megabits
G ..... Gigabits

EEEE – DIE DATA BASE REVISION

F – FORM
Die Form ..... D
Wafer Form (6" Wafer) ..... W

GG – TESTING LEVELS
Standard Probe (0° to 70°C) C1
Hot Speed Probe (0° to 70°C) C2
Standard Probe (-55° to 125°C) X1
Hot Speed Probe (-55° to 125°C) X2

HH – ACCESS TIME
(Applicable for C2 and C3 only)
-5 ..... 5ns or 50ns
-6 ..... 6ns or 60ns
-7 ..... 7ns or 70ns
-8 ..... 8ns or 80ns
-9 ..... 9ns or 90ns
-10 ..... 10ns or 100ns
-12 ..... 12ns or 120ns
-15 ..... 15ns or 150ns
-17 ..... 17ns
-20 ..... 20ns
-25 ..... 25ns
-35 ..... 35ns
-45 ..... 45ns
-50 (SRAM only) 50ns

ORDER INFORMATION*

Each Micron component family is manufactured and quality controlled in the U.S.A. at our modern Boise, Idaho, facility employing Micron's low-power, high-performance CMOS silicon-gate process. Micron products are functionally equivalent to other manufacturers' products meeting JEDEC standards. Device functionality is consistently assured over a wider power supply, temperature range and refresh range than specified. Each unit receives continuous system-level testing during many hours of accelerated burn-in prior to final test and shipment. This testing is performed with Micron's exclusive AMBYX intelligent burn-in and test system.

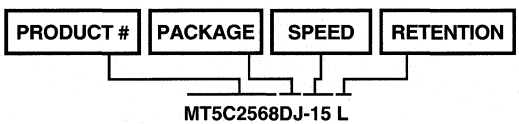
Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributor nearest you. Micron's policy is to offer prompt, accurate and courteous service while assuring reliability and quality.

Telephone: 208-368-3900
Fax: 208-368-4431
Micron DataFax: 208-368-5800
Customer Comment Line:
800-932-4992 (U.S.A.)
01-208-368-3410 (Intl.)

ORDER EXAMPLES

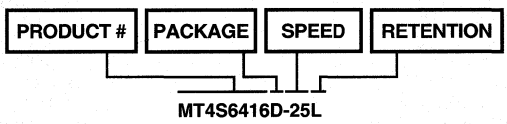
SRAM

32K x 8, 15ns in Plastic SOJ



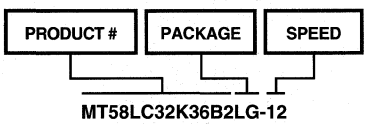
SRAM MODULE

64K x 16, 25ns in DIP Module with 2V Data Retention



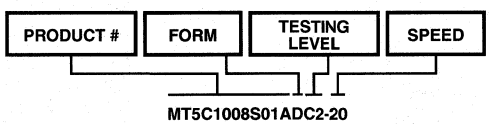
SYNCHRONOUS SRAM

3.3V, 32K x 36, 12ns in TQFP



SRAM DIE

128K x 8, S01A Database, Die Form, Speed Probe, 20ns



SALES INFORMATION

*For more detailed information, refer to the product numbering charts on pages 8-9 through 8-14.

ALABAMA

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Fax - 205-534-2384

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Fax - 205-830-2565

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Fax - 602-437-2124

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1810 N. Greenville Avenue
Richardson, TX 75081
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Bay Area Electronics Sales, Inc.
2001 Gateway Place, Suite 315 W
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Fax - 408-452-8139

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9119 Eden Oak Circle
Loomis, CA 95650
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Fax - 916-652-5678

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5100 Campus Drive, Suite 300
Newport Beach, CA 92660
Phone - 714-724-8080
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Jones & McGeoy Sales, Incorporated
5060 Shoreham Place, Suite 200
San Diego, CA 92122
Phone - 619-458-5856
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20501 Ventura Blvd., Suite 130
Woodland Hills, CA 91364
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Chatsworth, CA 91311
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Fax - 818-775-1302

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1 Old Field Drive
East Irvine, CA 92718-2809
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Fax - 916-624-9750

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9369 Carroll Park Drive
San Diego, CA 92121
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3170 Pullman Street
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Fax - 818-594-8234

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134 Rio Robles
San Jose, CA 95134
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Fax - 408-954-9113

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217 Technology Drive, Suite 110
Irvine, CA 92718
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Fax - 714-753-5074

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3000 Bowers Avenue
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Fax - 408-727-5896

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Rancho Cordova, CA 95742
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Fax - 916-638-1491

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9525 Chesapeake Drive
San Diego, CA 92123
Phone - 619-565-9171
Fax - 619-565-0512

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26010 Mureau Road, Suite 150
Calabasas, CA 91302
Phone - 818-880-9000
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66 Colonnade Road, Suite 205
Nepean, Ontario K2E 7K7
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Clark-Hurman Associates
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Davetek Marketing
107-3738 North Fraser Way
Burnaby, BC V5J 5G1
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8610 Commerce Court
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Fax - 604-420-5376

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151 Superior Blvd., Unit 1-6
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Fax - 514-335-2481

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4860 Ward Road
Wheatridge, CO 80033
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Fax - 303-422-9892

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Fax - 303-790-4532

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12503 E. Euclid Drive, Suite 20
Englewood, CO 80111
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Fax - 303-790-4991

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451 E. 124th Street
Thornton, CO 80241
Phone - 303-457-9953
Fax - 303-457-4831

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Advanced Tech Sales Incorporated
Westview Office Park
Building 2, Suite 1C
850 N. Main Street Extension
Wallingford, CT 06492
Phone - 508-664-0888
Fax - 508-664-5503

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61 Mattatuck Heights
Waterbury, CT 06705
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Fax - 203-596-3232

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Cheshire, CT 06410
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Fax - 203-272-1704

Pioneer Standard
#2 Trap Falls Road
Shelton, CT 06484
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Fax - 203-929-9791

Wyle Laboratories
20 Chapin Road, Bldg. 1013
Pinebrook, NJ 07058
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Phone - 800-862-9953
Fax - 201-882-9109

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Omega Electronic Sales Incorporated
Four Neshaminy Interplex, Suite 101
Trevose, PA 19053
Phone - 215-244-4000
Fax - 215-244-4104

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Pioneer Technologies
500 Enterprise Road
Horsham, PA 19044
Phone - 215-674-4000
Fax - 215-674-3107

Wyle Laboratories
1 Eves Drive, Suite 111
Marlton, NJ 08053-3185
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Fax - 609-985-8757

DISTRICT OF COLUMBIA

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Electronic Engineering & Sales, Inc.
305 Kramer Road
Pasadena, MD 21122
Phone - 410-255-9686
Fax - 410-255-9688

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Anthem Electronics Incorporated
7168 A Columbia Gateway Drive
Columbia, MD 21046-2101
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10240 Old Columbia Road
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Fax - 410-381-2036

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9100 Gaither Road
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9101 Guilford Road, Suite 120
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Fax - 301-490-2190

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Representatives

Photon Sales, Inc.
1600 Sarno Road, Suite 21
Melbourne, FL 32935
Phone - 407-259-8999
Fax - 407-259-1323

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715 Florida Street
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Fax - 407-896-6197

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3475 B. East Bay Drive
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Fax - 813-536-4599

Distributors

Anthem Electronics Incorporated
598 S. Northlake Blvd., Suite 1024
Altamonte Springs, FL 32701
Phone - 407-831-0007
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7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
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Fax - 407-290-0164

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3350 NW 53rd Street, Suite 105-107
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Fax - 305-484-2995

Hamilton Hallmark
10491 72nd Street North
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Fax - 404-416-6433

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Component Sales
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Fax - 208-368-3488
Micron DataFax - 208-368-5800

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Fax - 314-291-7958

Industrial Representatives, Inc. (N. IL)
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Skokie, IL 60077
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Fax - 708-967-5903

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Phone - 800-528-8471
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Phone - 516-351-1000
Fax - 516-351-1606

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