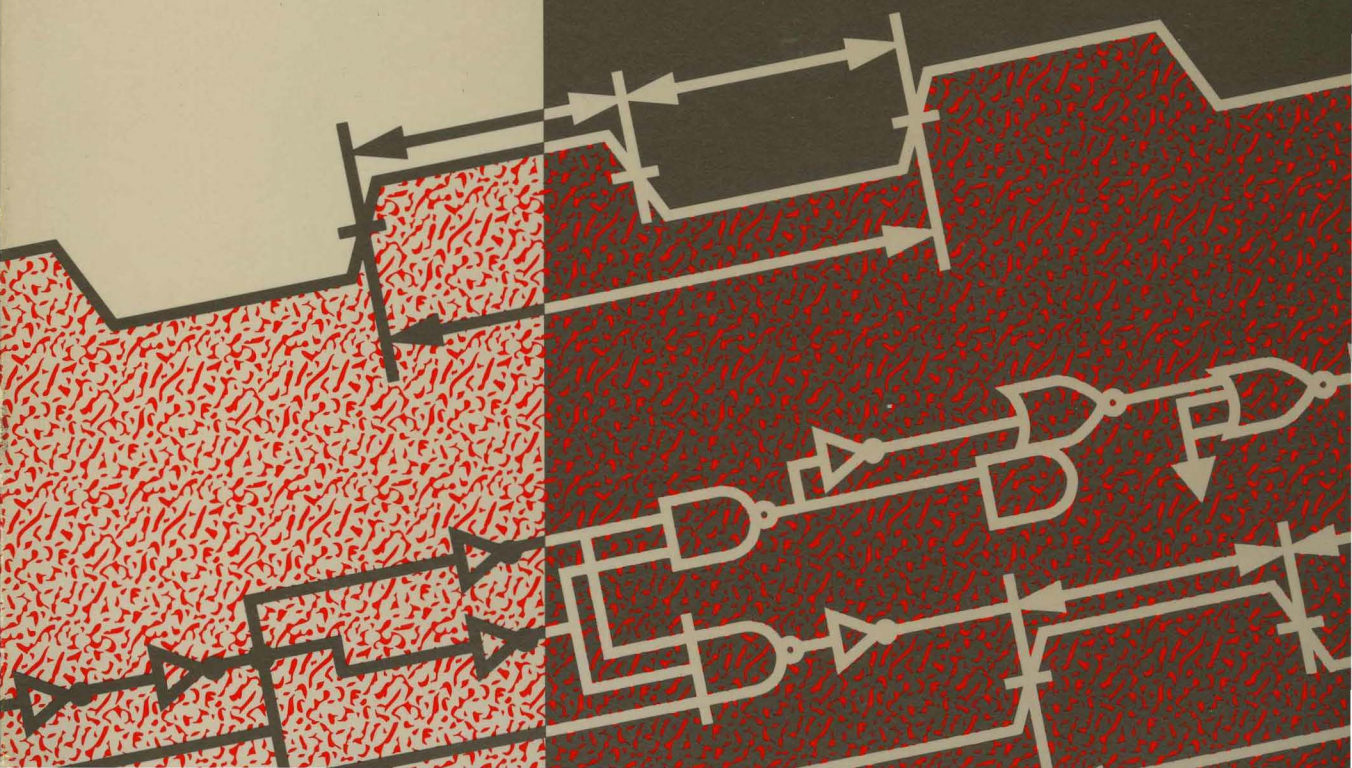
LSI LOGIC

Shortform Catalog
1991



LSI LOGIC

Shortform Catalog

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LSI LOGIC

Products and Services

LSI LOGIC

Products and Services

Introduction

ASICs

LSI Logic is the leading designer, developer and manufacturer of the most advanced ASICs (Application-Specific Integrated Circuits) in the industry. The company's broad ASIC line includes high performance HCMOS and BiCMOS array-based and cell-based ASICs which integrate random logic, microprocessors, memory and analog functions on chips with up to 200,000 equivalent gates. LSI Logic also manufactures and markets SPARC and MIPS microprocessors using RISC (Reduced Instruction Set Computing) technology and other selected standard products.

Military

Radiation-hardened versions of array-based ASICs are available from 10,000 to 50,000 usable gates with a total dose of 200 to 1,000 krads (Si). LSI's mil/aero facility in Fremont, CA is fully self-contained, with assembly, burn-in, test and qualification in one domestic location.

MDE Design Tools

LSI Logic's comprehensive and flexible ASIC design tools support both silicon-specific and system design environments. The MDE® (Modular Design Environment®) Design Tools, CDE® (Co-Designer™ Environment) Design System and interface tools are fully integrated with the company's advanced manufacturing capabilities.

MDE tools offer Design Builder and Silicon Builder, which greatly increase ASIC designers' productivity while making sure that correct-by-construction circuits are designed. Design Builder tools synthesize higher level descriptions of circuits into netlists. These netlists are then synthesized using the Silicon Builder tools to produce efficient physical layout. This combination produces ASICs guaranteed to meet specifications, whether customers use in-house MDE software, or one of LSI Logics's Design Resource Centers.

The MDE toolset, comprised of over 25 modules, is used to design chips with up to 200,000 gates and systems in excess of two million gates. More than 1,000 library elements ranging from simple macrocells to complex megacells are available for both array- and cell-based ASICs.

RISC Microprocessors

The LSI Logic MIPS and SPARC microprocessor product lines provide open-architecture RISC design solutions. A variety of peripheral chips and chip sets, including processors optimized for embedded control, and innovative chip-on-board module packaging technology, enhance the product line. LSI Logic's leading-edge microprocessor products simplify design and shorten the time-to-market for SPARC- and MIPS-based products.

DSP Products

LSI Logic manufactures selected standard products, such as DSP (Digital Signal Processing) products. LSI Logic's DSP family currently includes 32-bit building block processors, special purpose memory devices, Function-Specific DSP, Crossbar Switch, Error Correcting Reed-Solomon Codec and still image and video compression chip sets.

The term "Function-Specific DSP" covers a wide range of devices which are optimized to perform a particular algorithm, or function. Typically the system designer turns to function-specific devices when the performance required far exceeds that which can be delivered by a single chip DSP microprocessor. LSI Logic offers devices capable of processing video data at 20 or even 40 MHz in real time. Application areas where this kind of performance is required include image processing, radar, sonar, C3I, visualization systems and any application where video data rates are required.

Image and video compression products, the newest LSI Logic DSP products, offer the ability to drastically reduce the amount of digital information required to store or transmit images (either still or full motion video). The still image compression chip set is compatible with the JPEG standard, while the video compression chip set is designed to the CCITT H.261 standard.

Introduction
Cont'd

Worldwide Manufacturing
LSI Logic has state-of-the-art manufacturing sites in the US, Japan, West Germany and Canada. Through these facilities, LSI Logic offers high-performance 1.0-micron drawn gate length (0.7-micron effective channel length) processes and more than 400 different advanced package types.

Right-First-Time™ Silicon
Prototype turnaround times average two weeks for gate arrays and six weeks for sell-based ASICs–the fastest in the industry. LSI Logic's proven track record of over 10,000 successful designs assures Right-First-Time™ ASIC solutions.

Design Concept

LSI Logic design tools are focused on reducing the design cycle and "buying you time". This is vital in establishing a market lead in product introduction.

They also leverage the silicon technology providing highly optimized, fast circuits that lead to differentiated products.

Design Resource Centers

LSI Logic offers the industry's most extensive ASIC design support network and a full range of hardware and software design tools. At 39 LSI Logic Design Resource Centers worldwide and 12 authorized distributor Design Centers, experienced application engineers offer training and design assistance giving customers the expertise, hardware platforms and design tools they need to integrate systems into silicon.

Manufacturing

Advanced wafer fabrication, assembly, testing and packaging technology make LSI Logic the leader in prototype and volume ASIC manufacturing. With worldwide production facilities extending from the US to the United Kingdom, Japan, West Germany and Canada, LSI Logic's manufacturing operations are geared to produce dense and fast chips, a wide variety of packages, small-to-large production runs and extensive test patterns. These manufacturing sites offer advanced ASIC processes including 1.0 and 1.5-micron drawn gate lengths (0.7-micron and 0.9-micron effective channel lengths) HCMOS and high-performance BiCMOS.

LSI Logic offers more than 400 different plastic and ceramic package types with up to 524 leads and accommodating die up to 1.5 cm sq. These include pin grid array, leaded and leadless chip carrier, chip on tape, plastic quad flat packs and dual-in-line packages.

Fast Prototypes

LSI Logic offers the fastest ASIC prototype services in the industry. Fully tested and working gate array prototypes are delivered in only two to three weeks – or an eight-day *Hot Lot* services is offered if a customer requires faster turnaround. For cell-based ASICs, tested and working prototypes are delivered in six weeks – or *Hot Lots* in just four weeks.

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ASIC Design Tools

LSI LOGIC

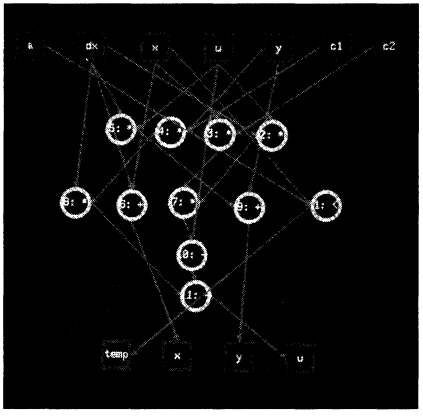
Silicon 1076 VHDL
Preliminary

Overview

Silicon 1076 is an advanced system development environment that reduces the time-to-market for ASIC-based systems. It provides a complete concept-to-silicon design methodology based on the VHDL (VHSIC Hardware Description Language). Because Silicon 1076 is integrated with LSI Logic's MDE® Design Tools and advanced manufacturing capabilities, it is the only environment that provides Right-First-Time™ manufacturing assurance for the most complex systems.

Silicon 1076 eliminates labor-intensive mapping of code from one design level to the next:

- At the **architectural level**, partitioning tools turn abstract code into design alternatives. Area estimation software helps the designer evaluate the alternatives. Synthesizing software generates a register transfer level VHDL description of the selected alternative
- At the **register transfer level** (RTL), synthesis tools generate and optimize gate-level VHDL netlists
- At the **gate level**, the optimized VHDL netlist can be translated to MDE format. After the MDE netlist is validated, the resulting delay information is annotated back into the VHDL netlist



Silicon 1076

Benefits

- Reduces the time-to-market for ASIC-based electronic systems
- Ensures that the complex designs can be built in silicon
- Facilitates the design of complex systems in silicon
- Maximizes designer creativity and productivity by supporting top-down design
- Eases the translation of designs to new or different technologies
- Shortens the learning curve with its integrated, single-language design environment
- Complies fully with MIL-STD 454M requirement 64

Features

- Integrates powerful VHDL design tools with LSI Logic's proven design analysis and signoff tools and worldwide manufacturing capability
- Allows flexible VHDL data entry at the architectural, RTL or gate level
- Provides flexible design optimization: library-independent or based on LSI Logic libraries
- Partitions functions, estimates area and synthesizes RTL code from VHDL architectural descriptions
- Synthesizes memory and logic blocks through calls to LSI Logic distributed experts: Logic Block Synthesizer (LBS) and Memory Compiler (MEMCOMP)
- Annotates delays from MDE back into the gate-level VHDL netlist
- Supports LSI Logic product line libraries
- Assures LSI Logic Right-First-Time silicon

LSI LOGIC

C-MDE Design System
Preliminary

Overview

C-MDE™ (Concurrent Modular Design Environment) Design System is a new state-of-the-art ASIC design environment that enables you to meet and beat your time-to-market deadlines. The C-MDE Design System combines new capability, ease of use and LSI's proven ASIC design methodology with powerful results.

The C-MDE tool set was designed to take schematic capture and simulation through to layout tools into an integrated environment that allows multiple programs to run and interact concurrently.

In the C-MDE environment, concurrency and a unified database means designers can open simultaneously a schematic capture window and a simulation window. Changes made to the schematic are reflected almost immediately in the simulation window. This eliminates having to exit schematic entry, transfer the netlist to a file and import the netlist into simulation before proceeding. This rapid feedback speeds design cycle time.

Features and Benefits

- Concurrency and intertasking among applications dramatically cut the analysis and debug cycle
- Common design database simplifies the flow of data and reduces memory requirements
- Interactive, integrated graphical interface quickly transfers vital design data to the user
- Incremental linking and compilation reduces design cycle time
- Rule-based automation manages design complexity

Modular Design Environment Design Tools

Description

LSI Logic's MDE® (Modular Design Environment®) Design Tools represent the industry's most advanced and proven array- and cell-based design system. MDE software products and third-party offerings (CAE design tools, testers and accelerators) meet any ASIC design requirement and run in virtually any workstation or mainframe environment.

The MDE Integrator Series, Logic Integrator™ and Silicon Integrator™, offers a diverse range of high-performance graphics and non-graphic design-entry tools supported by the most extensive library in the industry. The Integrator Series includes all the elements necessary to quickly and accurately design arrays and cell-based ASICs (Application-Specific Integrated Circuits).

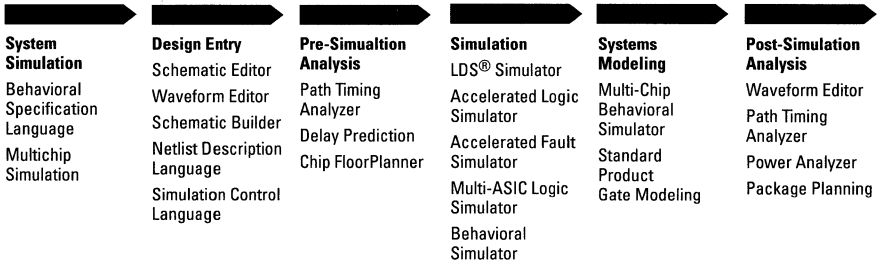
The entry-level Logic Integrator is for designs with complexities up to 12,500 gates. It can be upgraded with Silicon Integrator modules for building ASICs with up to 200,000 usable gates. The Silicon Integrator can also be easily coupled to the System Integrator's multi-chip mixed-mode simulation capabilities.

The Integrator Series operates on a variety of popular workstations.

Highly integrated, yet expandable, MDE configurations can include optional hardware accelerators and behavioral modelling, plus automated schematic and production test-pattern generators. MDE's modular approach allows easy migration into new leading-edge technologies and emerging CAE standards. MDE links the design to LSI Logic technology guaranteeing accuracy with a Right-First-Time™ record of over 10,000 successful designs.

MDE offerings are backed by LSI Logic's software support and technology training classes with complete documentation, system consulting and maintenance. A user hotline is available with trained engineering professionals on hand to assist with urgent customer problems. MDE tools are also available through LSI Logic's 39 global Design Resource Centers.

MDE Integrator Series ASIC Design Flow



The Integrator Series ASIC Design Flow lists the MDE modules available for each design step. The Logic Integrator, Silicon Integrator and System Integrator design packages each include a subset of these modules as standard and optional offerings.

Modular Design Environment Design Tools

LSI LOGIC

MDE Integrator Series Products

CAE Modules	Logic Integrator	Silicon Integrator
LDS Simulation and Verification Tools	■	■
Schematic Editor*	■	■
Waveform Editor*	■	■
Schematic Builder*		■
Path Timing Analyzer†		■
Power Analyzer†		■
Chip FloorPlanner		■
Behavioral Simulator		□
Multi-ASIC Simulator		□
Multi-Chip Behavioral Simulator		
Standard Product Gate Modeling		
Hardware-Accelerated Logic Simulator		□
Hardware-Accelerated Fault Simulator		□
Package Planner		□
Silicon Compilers		□

■ Modules included.
□ Modules available as options.
* Requires graphics platform.
† Supports 1.5-micron drawn gate length technology and under.

MDE Integrator Series Platforms

Workstations

Sun Microsystems
3 series, 4 series — Sun UNIX

Contact your LSI Logic sales representative for specific configurations and availability.
The integrator Series runs in nearly any CAE environment. The Logic Integrator runs on Sun Microsystems 3 and 4 series only. Graphics tools are supported only on Sun Microsystems workstations.

Modular Design Environment Design Tools

LSI LOGIC

Silicon Integrator Overview

The Silicon Integrator is a comprehensive single-chip design system for creating ASICs. Designed to run on high-performance multitasking computers, the Silicon Integrator features interactive event-driven simulation and one of the most extensive ASIC cell library sets in the industry. Graphics and multi-windowing provide a high productivity CAE environment. Non-graphic support on popular mainframes extends the Silicon Integrator availability to most high-powered computer hardware in use today.

A modular system, the Silicon Integrator anticipates a wide variety of user needs with standard features and add-on capabilities such as silicon compilation, chip sizing, hardware acceleration and PLA-to-ASIC cell conversion. The Silicon Integrator includes the following modules: schematic capture, waveform editor, single-chip simulator, test program extraction, path timing analysis, power analysis, chip floorplanning and schematic builder. Customers can select optional library support for specific applications.

Features

- Extensive library support
  - Macrocell Libraries–over 800 fully characterized SSI/MSI logic cells for device families from 700-gate channeled arrays to 100K-gate Compacted Arrays™ as well as cell-based ASICs
  - Megafunction and Megacell Libraries (optional library set) – more than 400 complex LSI/VLSI building blocks, including industry-standard parts and proprietary LSI Logic functions
- Precise gate-level simulation with back-annotated wire lengths guarantees ASIC performance and eliminates breadboarding
- Automatic error checking and reporting catches design problems early, enhancing productivity and manufacturability
- Automatic test program formatting for industry-standard test equipment
- Add-on capabilities
  - Design productivity tools such as Design Builder, Test Builder and Silicon Builder
  - Multi-ASIC gate-level simulators
  - Behavioral simulators
  - Mixed-mode simulators
  - Automatic test pattern generator for scan-based synchronous circuits
  - ChipSizer™

Logic Integrator Overview

The Logic Integrator is a low-cost entry-level system containing design and simulation tools for creating single-chip ASICs on Sun platforms. Optimized for graphic entry and multi-window tasking, the Logic Integrator boosts CAE productivity for 1.5-micron drawn gate length (0.9-micron effective channel length) HCMOS Channel-Free™ designs using LSI Logic's design libraries. These libraries contain hundreds of industry-standard logic elements, supporting designs with up to 12,500 usable gates.

The Logic Integrator provides a low-cost entry point to the MDE Design Tools allowing ASIC designers to upgrade to more powerful tools and emerging technologies later. A modular expansion path offers application and design portability to a variety of hardware platforms as well as upgrades to emerging technologies and mixed-mode behavioral and gate-level multi-chip simulation. The Logic Integrator features near-mainframe performance providing schematic capture, waveform editor, graphic entry and editing of simulation test patterns, interactive (single-chip) simulation, design verification and production test pattern extraction.

Features

- Graphic schematic editing with advanced automated features
- Graphic waveform logic editing for precise interactive simulation of all or part of a design
- Automatic extraction of production test programs, including patterns to evaluate timing sensitivity
- Silicon-specific designs for guaranteed ASIC perfomance-to-simulation specifications
- Upgrade path to Silicon Integrator and System Integrator tools

LSI LOGIC

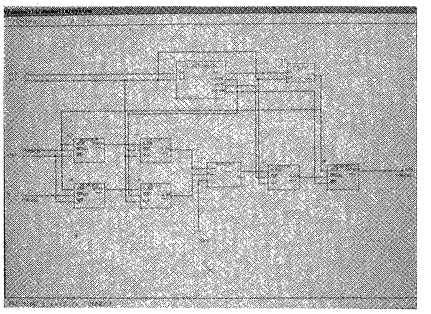
Design Builder Synthesis Software

Description

Design Builder enables the designer to design complex ASICs (Application-Specific Integrated Circuits) on his own workstation or at any of LSI Logic's worldwide Design Resource Center locations. With this sophisticated set of design tools, the designer no longer needs to worry about designing ASICs at gate level. He simply describes what he wants, be it a state machine, logic functions, ASIC memories or a datapath block, such as the adder. Design Builder automatically generates optimized netlists.

While designing various components of a single or multi-ASIC system, Design Builder allows the designer to perform quick feasibility analysis and get reliable answers to "what if" kinds of questions about alternative chip sizes, packages, etc. Design Builder is fully compatible with LSI Logic's MDE® Design Tools and is available on the Sun/UNIX platform. Support for other platforms is available if needed.

Design Builder demonstrates LSI Logic's continued commitment to Right-First-Time™ delivery of working prototypes that are verified and fully tested.



Design Builder provides capabilities to implement RAM/ROM, DataPath logic, control logic, logic blocks, and logic arrays on an ASIC efficiently.

Benefits

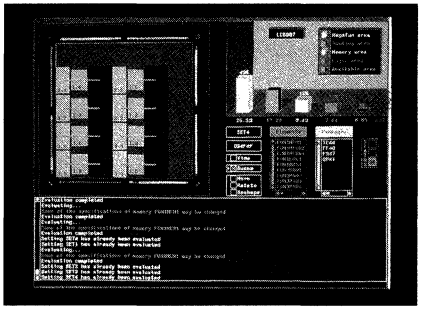
- Design productivity is enhanced and ASIC development costs are reduced
- First-pass working silicon ensures on-time product market entry
- On-site design tools offer efficient project management control and promote a team project approach and the sharing of design system resources
- Expert technical support is available in local Design Resource Centers at worldwide locations
- Full MDE Design Tools support including customer training and a hotline service is available

LSI LOGIC

ChipSizer Synthesis Software

Overview

LSI Logic's ChipSizer™ software offers systems designers an ASIC (Application-Specific Integrated Circuit) planning environment. In this environment, designers can evaluate various alternatives in determining which system functions are ideal for ASIC implementation, the appropriate technology and die size of an ASIC, and the package requirements based on the die size and the pin requirements. ASIC designers can quickly perform this iterative task and document "what if" type of analysis to evaluate various alternatives of system partitioning. The versatility of the software allows expert designers to supplement the rules based on their experience. The ChipSizer tool is fully automatic in effectively illustrating multiple ASIC solutions. The user specifies system components such as logic blocks, memories, I/Os or other elements via a user-friendly graphics interface. Then the ChipSizer tool graphically displays the area allocation diagram and pad locations of various components in a system. It also allows designers to fine tune the floorplan by moving or rotating megacells. The accuracy of die size estimation improves with design details.



ChipSizer enables users to select the best architecture by evaluating different alternatives.

Benefits

- Ensures silicon efficiency to a high level of confidence
- Analyzes design alternatives without having to describe the netlist or physical design
- Describes designs as logic blocks, ASIC memory blocks or other LSI Logic library elements, such as megafunctions
- Describes designs independent of the technology and helps in realizing an optimum system configuration of multiple ASICs
- Bases the floorplan of the chip on place-and-route software algorithms, which can be fine-tuned using graphic commands, such as **move**, **rotate** and **reshape**
- Allows expert designers to specify their own rules to tailor the tool to their particular needs
- Can easily implement alternative technologies or design rule changes
- Documents system concepts and various alternatives
- Offers a user-friendly graphics interface

Features

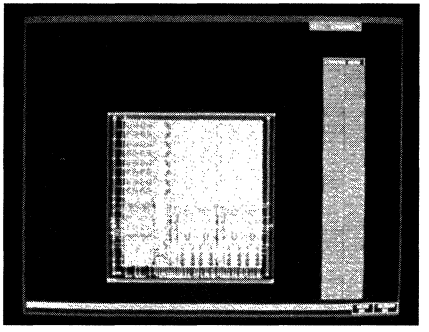
- Specifies buses as global (that is, with connection between blocks) or local to a logic block
- Evaluates multiple ASIC architectures by hierarchical function
- Computes memories with the use of LSI Logic's Design Builder
- Offers a wide range of user-specified options within each class of logic functions
- Describes designs independent of technology
- Can easily evaluate a given design under alternative technologies
- Bases its floorplan estimation on layout design tools
- Automatically calculates power pad requirements
- Ensures that packaging requirements are met and suggests suitable packages
- Has full MDE® Design Tools support available

LSI LOGIC

Memory Compiler
Preliminary

Overview

LSI Logic's Memory Compiler software allows ASIC system designers to automatically compile memories such as multi-port RAMs, ROMs, FiFOs, ROM-Multipliers or Barrel-Shifters. The Memory Compiler generates megacells for cell-based products and Channel-Free™ array-based products using 1.0 and 1.5-micron drawn gate length (0.7 and 0.9-micron effective channel length) HCMOS technology. With Memory Compiler, the user can quickly and efficiently generate memories optimized for both speed and area. Memory Compiler generates all the necessary data files for accurate timing simulation as well as physical layout design. ASICs with on-board mem-ory requirements can now be implemented easily, using advanced 1.0-micron gate length HCMOS technology.



ASIC RAMs and ROMs can be generated in minutes using Memory Compiler.

Benefits

- Megacells can be compiled and implemented on user's own workstation
- Fast megacell turnaround significantly reduces ASIC development cycles
- Automatic test vector generation saves significant design time
- Risks are reduced, since megacells are "right by construction"
- Easy to use, graphics menu interface
- Fully integrated within MDE® Design Tools
- Has full MDE Design Tools support available
- Technical training available from experienced staff

Features

- Memory Compiler supports both array-based and cell-based products
- Memory Compiler supports both 1.0 and 1.5-micron gate length HCMOS process technologies
- RAMs can be compiled with single port, two ports, three ports or six ports
- ROMs can be compiled with maximum block size of up to 64K bits
- Single-port RAMs can be compiled in two types: low power RAMs with up to 4K bits maximum, and 1.0-micron gate length high-density cell-based RAMs with up to 72K bits maximum per block
- High-density, single-port RAM's performance is competitive with commercially available SRAMs, Taa < 7.5uS
- Programmable I/Os allow easy expansion for wide data word widths such as 16, 32 or 64 bits
- Flexible design allows for easy scan test implementation by user

Description

The user specifies the memory parameters such as Words, Bits (wordlength), number and types of Address ports. As shown in figure 1, a 32 x 16 single-port RAM with one read/write Address port and an eight-bit Byte Write capability is specified.

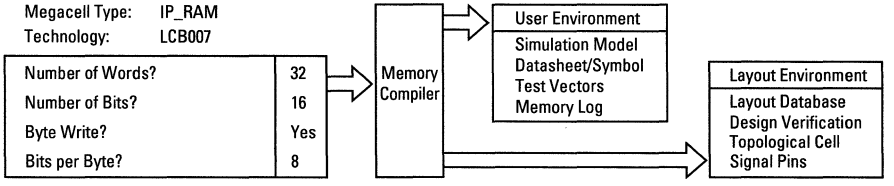


Figure 1. Memory Compiler User Specifications and Output Files

LSI LOGIC

Test Builder
Preliminary

Overview

Test Builder is an advanced scan design environment that reduces time-to-market and improves productivity for ASIC-based systems. It provides high fault coverage and performance based on the full scan design methodology. Because Test Builder is integrated with LSI Logic's MDE® Design Tools and advanced manufacturing capabilities, it is the only scan design environment that provides Right-First-Time™ silicon.

Test Builder is an integrated scan design environment that automates creation of test vectors to achieve high stuck-at-fault coverage for synchronous designs. It consists of Scan Design Expert (LDMC), Scan Design Synthesizer (LSCAN) and Synchronous Automatic Pattern Generator (SATPG).

Benefits

- Time scale for test vector development is substantially reduced
- Ensures that the complex scan designs are fully testable
- Increases reliability of ASICs
- Generates test patterns that typically have 95% or more stuck-at-fault coverage
- Eases ASICs debugging and straightforward timing analysis
- Maximizes designer creativity and productivity by supporting higher level design
- Full software support
- Easy to learn and use
- Technical training available from experienced staff

Features

- Fast and efficient built-in fault simulation and test vector generation
- No additional hardware required
- Full support of LSI Logic scan methodology
- Checks all scan design rules automatically
- Automatically converts non-scan design to scan design
- Produces compact and optimized test vectors
- Provides flexibility in handling special blocks such as RAM/ROM and megafunction
- Enables flexible integration of boundary scan (JTAG) scheme
- Works at net-list level
- Only one test pin is needed for scan compatible designs. Scan in and scan out can be multiplexed with regular I/Os
- Selects best scan chain order to minimize chip area overhead
- Detailed summary reports

Logic Block Synthesizer

Overview

The Logic Block Synthesizer (LBS) is a logic design tool which significantly enhances designer productivity during the logic design phase by automating the design, verification and documentation of common logic functions. Counters, registers and muxes are examples of such functions that are part of almost every digital system design. With the LBS, optimized logic functions which are "right by construction" can be automatically generated from user specifications. As a result, ASIC systems and logic designers greatly enhance their design productivity.

Benefits

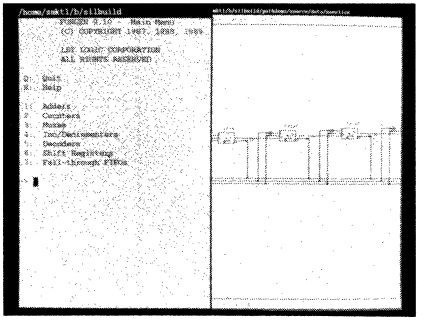
- Increases logic design productivity thus reducing ASIC development costs
- Datapath building blocks such as multipliers and adders are available. As a result of this Datapath, designs can be built efficiently
- 13 logic functions, each with different varieties of modules supported
- Hotline service is available
- Fully integrated within MDE® Design Tools
- Technical training available from experienced staff

Features

- Supports most commonly used logic building blocks
- Generated circuits are optimized for speed or area (gate count)
- Wide range of user specified options within each class of logic functions
- On-line help menu available
- Easy to use, menu driven user interface

Description

LSI Logic's Block Synthesizer generates adders, counters, muxes, incrementer/decrementer, decoders, shift-registers and fallthru FIFOs. The Logic Block Synthesizer generates an NDL netlist and a file with file type or extension of .PINS, which contains the I/O signal names. The netlist can be implemented in Channel-Free™ array-based products or cell-based products using 1.0 or 1.5-micron drawn gate length (0.7 or 0.9-micron effective channel length) HCMOS technology. Schematic of the netlists thus generated is made available by the Schematic Builder software. The simulation of the whole ASIC, of which the complied function is a part, is done within LSI Logic's MDE Design Tools.



Logic Block Synthesizer saves designers time in building logic and Datapath blocks.

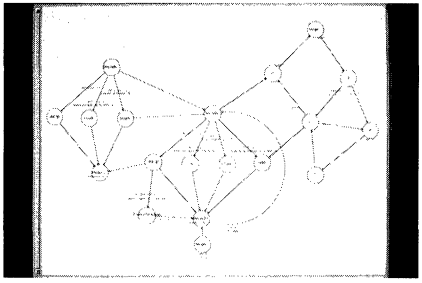
Availability

Technology	Channel-Free Array Products		Cell-Based Products
1.5-micron	LCA10000	LMA9000	LCB15
	✓	✓	✓
1.0-micron	LCA100K	–	LCB007

Logic Expression Synthesizer Design Tool

Description

LSI Logic's Design Builder software includes Logic Expression Synthesizer (LES), a logic synthesis tool, that helps to design high-performance ASICs (Application-Specific Integrated Circuits). LES provides an efficient means of designing finite state machines, sequencers and other control logic, which are essential parts of most digital ASIC circuits. It allows design description using Boolean equations, truth tables or a HDL language similar to C. An associated Register-Transfer Level simulator allows the verification of a circuit at the design-language level without a gate-level translation. As a result, the design can be iterated quickly for evaluating various alternatives. Once the design is functionally complete, LES automatically builds a gate-level NDL netlist for either Channel-Free™ array-based products or cell-based products. It also features an optimizer. With this logic synthesis tool, designers can shorten design time to build finite state machines, datapaths and control logic circuits that are correct by construction.



Logic Expression Synthesizer synthesizes finite state machines, control and Datapath logic efficiently.

Benefits

- Saves weeks in generating gate-level netlists from higher levels of abstraction compared to the schematic capture approach
- Simplifies the tracking of design details
- Efficiently manages complex ASICs because logic is described in higher levels of abstraction
- Optimizes the circuit for area and speed, saving designers a great deal of time
- Is technology-independent
- Minimizes production costs by reducing the overall chip size due to increased silicon efficiency compared with Schematic Capture
- Is fully supported by LSI Logic's MDE® Design Tools

Features

- Offers an easy-to-use, flexible, high-level synthesis language
- Offers multi-tasking capability, nonstandard clocking and compile-time control structures
- Synthesizes gate-level schematics directly from Boolean equations and finite state machines in Mealy or Moore form
- Translates truth table inputs similar to UC Berkeley's format into LES
- Supports both combinational and synchronous circuits
- Offers a logic optimization capability for technology implementation to achieve high performance
- Features a source-level debugger
- Offers a mixed-mode simulator by translating LES models to behavioral simulation language (BSL) models
- Performs static timing analysis using LCAP

LSI LOGIC

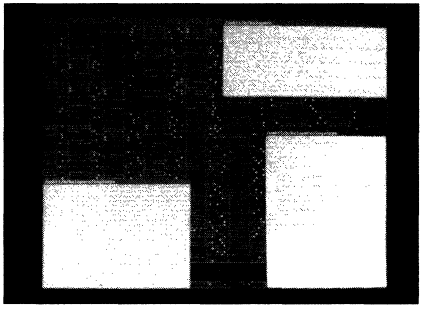
Silicon Builder
Preliminary

Overview

Silicon Builder is a suite of design tools that automatically generates layouts of random and regular structure logic block functions. This productivity-enhancing toolset is comprised of two compilers, Data Path Compiler and Block Compiler with its powerful Graphics Editor, and is yet another MDE® Design Tools package. Silicon Builder enables the designer to manage the design of today's and tomorrow's ASICs (Application-Specific Integrated Circuits) by offering:

- Complete control of the design process because the design tools are available on his own workstation
- Improved predictability of the final die size and length of the design cycle
- Increased accuracy of simulation and ability to avoid costly post-layout design changes

Although Silicon Builder is targeted for ASIC designers with limited layout expertise, these flexible tools allow expert designers to influence layouts. Actual segment length information enables the designer to verify accurate timing behavior of the circuit including setup and hold time checks. As a result, the designer can design ASICs on time with the assurance of first-time success.



With Silicon Builder, high-performance ASICs can be designed quickly and efficiently because the designer has access to actual layout information early in the design cycle for accurate timing verification of the functional logic blocks.

Benefits

- Provides access to a proven layout design system with over 10,000 completed designs
- Guarantees Right-First-Time™ ASICs
- Offers user control of the design cycle, because designers have access to Silicon Builder on their own workstations
- Allows easy sharing of design tool resources among various design projects, which significantly reduces ASIC development costs
- Eliminates the need for post-layout design change and significantly increases design productivity
- Saves silicon area and improves speed performance of ASICs
- Offers customer support, training and a hotline service

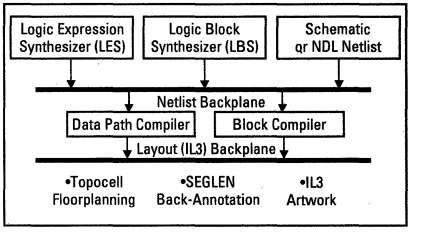


Figure 1. Silicon Builder enables ASIC designers to build block layouts efficiently, regardless of their expertise in layout.

Features

- Provides a segment length file (SEGLEN) that allows the designer to accurately verify the timing of the compiled blocks or datapath circuits
- Produces optimized layouts to minimize overall die size and to improve the performance of the ASIC circuits
- Allows expert designers to influence the layout so that they can meet their design goals
- Features a powerful layout Graphics Editor (GE) with built-in design rule checking
- Features a Graphics Editor with a rich command set that offers great flexibility in the interactive layout process, while ensuring compliance with design rules

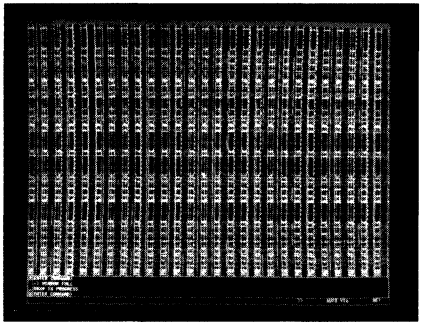
LSI LOGIC

Data Path Compiler
Preliminary

Overview

Data Path Compiler is a specialized Silicon Builder design tool that automatically generates optimized layouts of regular datapath structures for cell-based and array-based ASICs (Application-Specific Integrated Circuits). Its flexibility permits easy handling of designs with regular multibit logic elements connected by buses and non-bit-slice structures. Unlike conventional approaches to datapath compilation, the designer is not restricted to a limited set of cell library elements or a specific design description tool.

Datapaths can be efficiently described using the powerful Schematic Editor (LSED), an MDE® Design Tool. Alternatively, datapaths can be described using a high-level design language. For example, Logic Block Synthesizer (LBS), one of the Design Builder design tools, can be used to automatically generate NDL netlists of datapath elements, such as adders and muxes. Data Path Compiler accepts a netlist of the design, provides quick feedback on size estimate and wiring efficiency, and generates a completed layout along with wire segment information for accurate timing simulation.



Data Path Compiler produces dense layout datapath blocks by taking advantage of the regularity of structures and generates wire segment information for accurate timing verification.

Benefits

- Enhances system performance because optimized layouts are produced
- Minimizes costly post-layout design changes because datapath circuits can be accurately verified at an early stage
- Gives the designer complete control of the design process
- Increases design productivity, thus reducing ASIC development costs
- Provides expert technical support at worldwide Design Resource Center locations
- Offers full MDE design tools support, including customer training and a hotline service

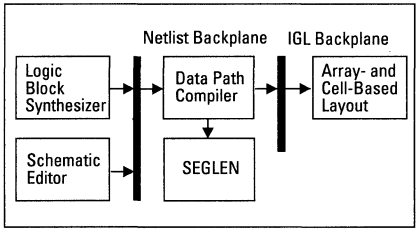


Figure 1. Data Path Compiler generates layout and segment length information for accurate timing verification.

Features

- Provides feedback on area estimation and wiring efficiency
- Compiles datapaths at the cell or chip level
- Allows routing of signal nets over the compiled datapath megacell
- Allows expert designers to use LSI Logic's powerful Graphics Editor (GE) to modify the layout manually
- Supports nonuniform bus widths and inter-bit-slice wiring
- Is compatible with Logic Block Synthesizer (LBS) to allow automatic generation of datapath elements, such as adders, incrementers/decrementers, registers, muxes and decoders
- Supports 1.0 and 1.5-micron drawn gate length (0.7 and 0.9-micron effective channel length) HCMOS Channel-Free™ array-based and cell-based products
- Allows easy use of graphics interface

LSI LOGIC

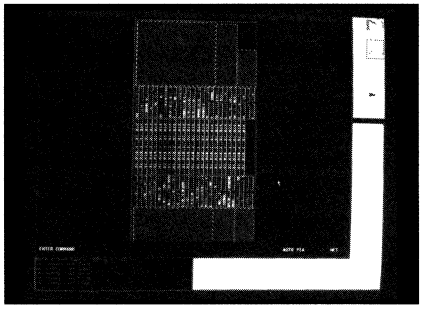
Block Compiler
Preliminary

Overview

Block Compiler is a specialized Silicon Builder design tool that automatically generates optimized layouts of random logic blocks for Channel-Free™ array-based or cell-based ASICs (Application-Specific Integrated Circuits). Block Compiler offers control of the layout process during the ASIC design phase. Block Compiler accepts a flat or a hierarchical netlist of functional blocks. It then places all of the cells and routes signal nets within the block, including clock lines and power buses automatically. ASIC designers with limited layout expertise benefit from the use of Block Compiler because the compiler produces block layouts that are 100% executed.

At the same time this flexible tool allows expert designers to interactively influence the layout and meet performance goals. With Block Compiler, sections of the design, including the physical layout, are fully implemented. Actual wiring information is quickly made available by the compiler to facilitate accurate timing verification of the blocks.

As a result, designers are able to predict both the size of an ASIC and its performance at an early stage rather than at the chip layout completion stage. Any design changes in the post-layout stage have an adverse effect on design schedules. Block Compiler virtually eliminates costly design iterations allowing timely market introduction of products. As a result, design productivity is enhanced.



Block Compiler produces finished layouts of logic blocks and generates wire segment information for accurate timing verification.

Benefits

- Gives ASIC designers complete control of the ASIC design process because it's available on their own workstations
- Produces optimized layouts, which enhance system performance
- Verifies critical sections of the circuit with accuracy at an early stage; therefore, no major surprises are encountered when the chip layout is completed
- Eliminates the need for costly design iterations and greatly enhances design productivity resulting in minimized ASIC development costs
- Offers full MDE® Design Tools support, including customer training and a hotline service

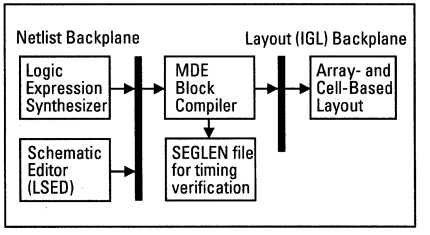


Figure 1. Block Compiler provides an easy and efficient means of bridging the netlist and layout (IGL) backplanes.

MDE
Support Service

Service Description

LSI Logic's MDE Support Service offers a comprehensive software support and maintenance package for MDE users. The service is required for each computer node authorized to run MDE design tools.

Features

The MDE Support Service offers the following benefits to the customer:

- **Hotline Support:**
  A dedicated, toll-free hotline is available for MDE Support Service subscribers (1.800.MDE.4545). Customers designate one primary and one alternate contact who may place direct calls to the Technical Support Center. Knowledgeable design tool engineers are ready to answer software questions and if software problems arise, assist in resolving them. In addition, users may report enhancement requests for the design tools through the Hotline. This service is not intended to replace or augment customer product training.

- **Periodic Software Updates:**
  Customers will receive regular updates to their MDE design tools. These updates include revisions covering enhanced software functionality, support of new hardware operating systems, documentation updates and corrections to software problems. If a critical software problem is encountered, every effort is made to correct the problem and update the user with a software patch.

- **Periodic Library Updates:**
  Technology libraries are updated on a regularly scheduled basis. Changes reflected in these library updates can affect design perfomance and functionality.

- **MDE Design Tools User Conference:**
  An annual conference allowing MDE users from across the country to meet with LSI Logic's management, engineering and CAD engineers to discuss various design issues ranging from future design tool requirements to current customer case studies. The conference is free to all MDE Support Service customers.

Note: The MDE Support Service does not cover hardware or operating system problem support. Installation services and system consulting are available at an additional cost.

CDE/MG Co-Designer Software for Mentor Graphics

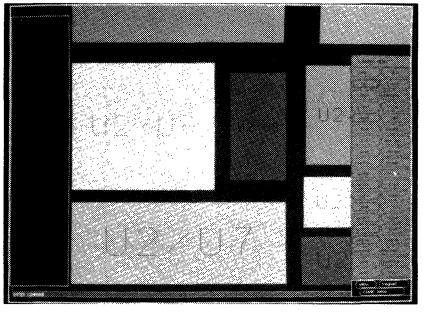
LSI LOGIC

Overview

Co-Designer® Environment for Mentor Graphics (CDE®/MG) software allows the user to design LSI Logic ASICs (Application-Specific Integrated Circuits) accurately in the Mentor Graphics environment, enhancing its capabilities by coupling LSI Logic's design methodology with Mentor Graphic's tools. CDE/MG software is the result of an engineering partnership between LSI Logic and Mentor Graphics, where both parties ensure that their software and libraries work together.

Designing high performance gate arrays and cell-based ASICs requires accurate timing for successful design implementation. The designer also needs to simulate at the system level to ensure the ASIC works correctly with the other components of the system.

CDE/MG software features quality silicon-specific timing within the Mentor Graphics environment. CDE/MG is fully integrated with LSI Logic's advanced manufacturing capabilities. The result is an ASIC that can be manufactured with LSI Logic's Right-First-Time™ assurance.



Floorplanning map of a chip, preparatory to full layout. The blocks have been placed by FloorPlanner™ software, an MDE® Design Tool.

Overview

- Is compatible with LSI Logic's Modular Design Environment software
- Uses Mentor Graphics' SYMED and NETED for schematic capture
- Uses Mentor Graphics' QUICKSIM for simulation
- Translates automatically hierarchical netlist between Mentor Graphics and MDE software databases
- Offers CSM, the Co-Designer Scheduling Monitor, making CDE/MG software easy to use
- Results in MDE software quality design sign-offs
- Back-annotates to QUICKSIM for accurate system-level simulation
- Includes LDS® simulation and verification, FloorPlanner software and bonding diagram programs
- Supports selected LSI Logic technology libraries
- Assures LSI Logic Right-First-Time silicon

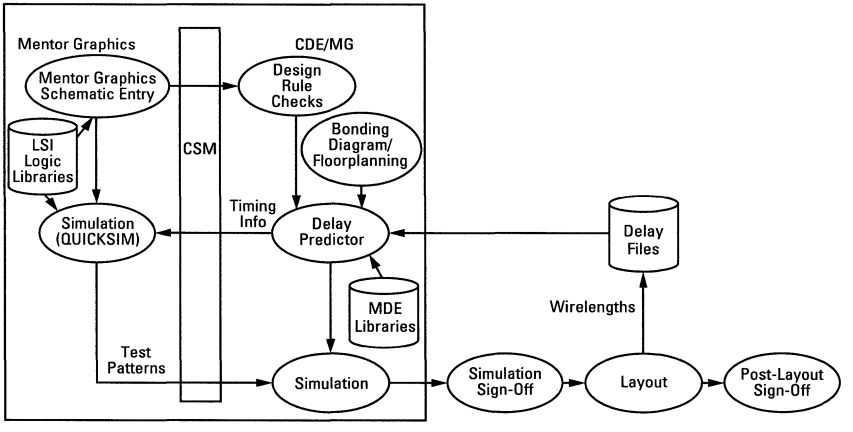


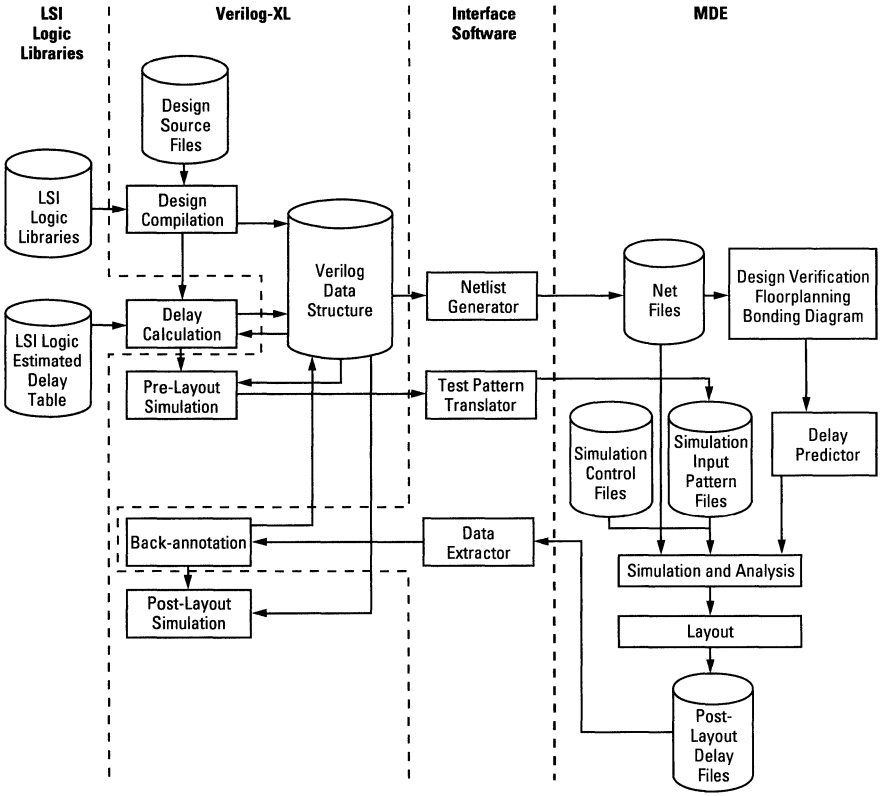
Figure 1. Using CDE/MG software in the Mentor Graphics Environment

VERILOG Design Kit

Introduction

The coupling of general-purpose EDA software along with silicon-specific software in the design of ASICs (Application-Specific Integrated Circuits) is becoming increasingly popular with electronic designers. The Verilog Design Kit from LSI Logic supports the use of Cadence's popular and highly regarded VERILOG-XL simulator in conjunction with LSI Logic's MDE® Design Tools. Now with the Verilog Design Kit, ASIC designers have a way to blend their Verilog simulator with MDE software. This is yet another example of LSI Logic's Open Systems Architecture, whereby general-purpose EDA software is bridged to silicon-specific MDE software. The results are superior, high-performance ASICs that are designed quickly with Right-First-Time™ assurance. Verilog Design Kit was written by LSI Logic's software and model development engineers working with their counterparts at Cadence, the Verilog vendor.

Block Diagram



LSI LOGIC

Synopsys Synthesis Libraries

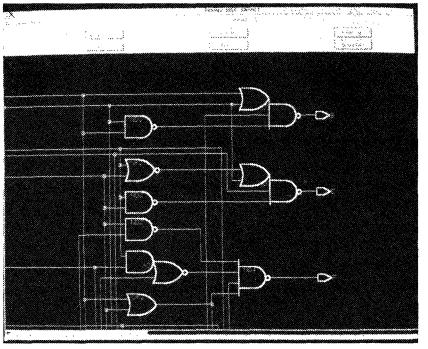
Overview

The LSI Logic/Synopsys libraries offer the user of the Synopsys Design Compiler software a link to LSI Logic's ASIC (Application-Specific Integrated Circuit) technology and manufacturing capability. A synthesis library, written in Synopsys library language format, contains the timing and functional description of LSI Logic macrocells. It also contains the definition of environmental delay conditions and wire loading tables. Each table is associated with a die and a package.

The synthesis libraries are developed in cooperation with Synopsys to effectively exploit the synthesis and optimization capabilities that Design Compiler offers.

LSI Logic/Synopsys libraries are designed to incorporate MDE® Design Tools delay estimation techniques into the process of logic synthesis and optimization with the Synopsys Design Compiler. Complex LSI Logic designs may be synthesized and optimized using process specifications that are offered and maintained by LSI Logic.

The synthesis libraries software includes internal macrocells only. Timing and logic information represents specification of MDE software and its libraries for use with Design Compiler. MDE software simulation and design verification are required for design acceptance at LSI Logic.



Synopsys Design Compiler uses timing models and embedded synthesis strategies in the LSI Logic synthesis library to generate optimized netlists.

Benefits

- Accurate timing and modelling
- Ease of use and compatibility with MDE software, Logic Expression Synthesis, Design Compiler, etc.
- Cost savings at implementation

Features

- Environmental condition scaling factors for delay calculation (i.e., WCCOM, BCCOM, NOM, etc.)
- Wire loading tables specific to each die code
- Default scaling factors
- Macrocell definitions
- Specifications for delay calculations under specific environmental conditions
- Instructions for Design Compiler to adopt alternative algorithms or actions to comply with LSI Logic modelling strategies

LLC
Valid Logic
LCA10000, LMA9000
Libraries

LSI LOGIC

Description

The Logic Library Connection (LLC) design interface supports front end design of LSI Logic's Channel- Free™ array and cell-based ASICs (Application-Specific Integrated Circuits) on Valid Logic workstations.

The LLC interface provides the graphics symbols of the macrocells to support graphics capture. It also provides simulation models that allow the designer to simulate on the Valid Logic workstation.

Once complete, it provides interface software to manage the transition to LSI Logic when the design is ready. It generates a network description language (NDL) file for LSI Logic's MDE® Design Tools. In addition, Valid Logic simulation outputs are converted to simulation control files, test pattern files and simulation listing files suitable for transfer to MDE software, where they will be used to test the chip and to compare and verify with MDE software simulations.

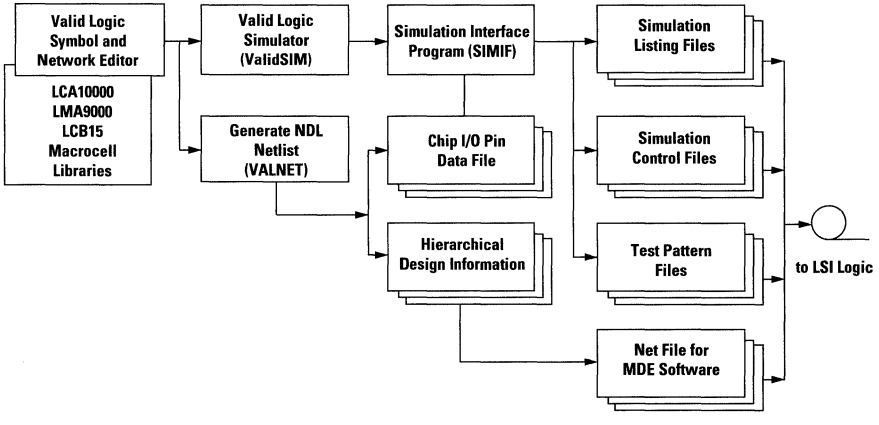
For the LCA10000 and LMA9000 libraries, the gate delays may be modified as functions of fanout, voltage, temperature, processing parameters and estimated wirelengths. For the LCB15 library, the gate delay is fixed, assuming no wirelength contribution and worst-case commercial conditions of 70°C, 4.75 V and +50% worst-case process.

ASIC designers can use the Valid Logic tools to capture and simulate an LSI Logic design prior to transferring to MDE software for final simulation, design rule checks, sign-off and layout. This can either be done on site or at one of LSI Logic's Design Resource Centers.

Features

- Interfaces with Valid Logic's schematic capture, ValidGED
- Interfaces with Valid Logic's ValidSIM simulation environment
- Offers the LCA10000 macrocell library
- Offers the LMA9000 macrocell library
- Includes macrocell elements
- Has high-drive buffers available
- Has configurable buffers available
- Generates NDL file with complete design hierarchy
- Generates simulation source files for functional test, parametric test, 3-state functional test and IDD test
- Generates expected simulation results listing
- Generates logical states for all outputs at the end of each simulation cycle
- Checks pulse width, setup and hold violations under worst-case commercial conditions

Diagram



LSI LOGIC

Other Third-Party Interfaces

Zycad Corporation	■ Support for LE, FE and XP hardware accelerators ■ All technology libraries supported	■ Megafunctions and memories supported ■ Sun4 platform supported
IKOS Systems	■ Support for 800/1900 hardware accelerators and simulation environment ■ LCA100K, LCB007, LCA10000 technology libraries supported	■ No memory or megafunction ■ At present, Sun4 and Sun3 platforms supported
Viewlogic Systems, Inc.	■ Certified LCA10000 and LMA9000 libraries	■ Sold by Viewlogic directly (contact Viewlogic for ordering information)

Note: Customers should contact LSI Logic for more information regarding third-party interface offerings.

LSI LOGIC

Design Services

LSI LOGIC

Design Building Blocks
Design Services

Overview

LSI Logic supports an extensive library of design building blocks. Complexities of the devices in this library range from gate-level macrocells and macrofunctions through function-level megacells and megafuctions, all the way up to system-level megacores. Designers can choose from almost 1,000 cells including flip-flops for special scan configurations, hard-coded functional elements, RAM and ROM configurations and multiplier configurations. In addition there are almost 200 significant Megafunctions, including military microprocessors, AMD, Motorola and Intel compatible devices, all types of data communications and microcontrollers, as well as a plethora of arithmetic functions. For further information, please see LSI Logic's Cell Development datasheet and Design Building Block Catalog.

Basic Building Blocks

LSI Logic has the industry's largest collection of design elements included with every technology library purchased. Design elements include everything from flip-flops, shift registers, I/O and internal buffers, latches, clock drivers, clock-prescalers, oscillators FIFOs, LIFOs, and arithmetic functions, to multiplexers, synchronizers and RAM and ROM configurations. Many basic megafunctions are also provided as an integral part of every technology library along with macrocells, macrofunctions, megacells and metal megacells. LSI has a technology library for every technology supported. Technologies currently include the LMA9000, LCA10000, LDD10000, LCB15, LCA100K, LCB007, LEA100K and LRH10000 and as LSI introduces new technologies, new libraries will be available to support them.

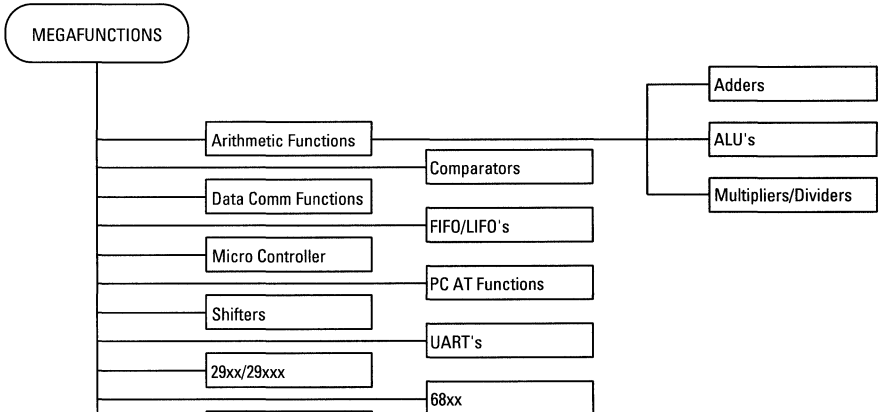
Individually Licensed Building Blocks

Complex megafunctions add significant value to LSI Logic's product offering. These functions are sold individually because of their added value. The megafunction lists in the library catalog are shown independent of technology. Not all megafunctions are actually available at the present time in all technologies. Translation into other technologies or conversions into rad-hard technologies or metal megacells can be done on a case-by-case basis.

Netlists

Netlists are available for most megafunctions. A netlist license agreement is required.

Building Blocks



LSI LOGIC

Cell Development
Design Services

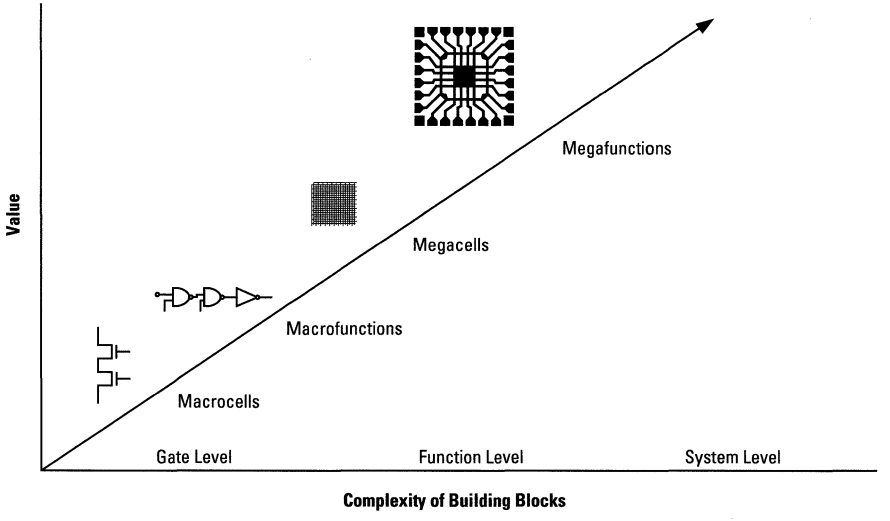
Overview

LSI Logic has the industry's largest collection of library elements for designing array- and cell-based ASICs (Application-Specific Integrated Circuits). LSI Logic Cell Development Design Services are prepared to design customer specific elements ranging from macrocells to megafunctions. Commonly developed cells include flip-flops for special scan configurations, hard-coded functional elements, new RAM and ROM configurations and multiplier configurations.

Benefits

Circuit performance can be dramatically improved by incorporating macrocells that efficiently fit the architecture of unique system designs. Variations in setup and hold time between register element instances caused by layout differences can be reduced by hard-coding the logic surrounding those register elements. Features for register elements such as set-direct, scan control and input data multiplexing can all be handled in this manner.

LSI Logic has a significant number of unique RAM and ROM configurations in the megacell libraries. These memories are constructed in an efficient manner optimizing area and speed. LSI Logic will create the correct size or number of access ports for memories needed by designers.



LSI LOGIC

Full Scan Testing and ATPG
Design Services

Overview

LSI Logic supports Full Scan Testing on designs which meet our published guidelines. The customer may supply his/her own vectors or purchase the scan ATPG (Automatic Test Pattern Generation) design service option. Purchase of the Scan Chain Creator program (LSCAN) and the Design Methodology Checker program (LDMC) provides optimal methodology support.

Benefits

When compared to ad-hoc test generation, scan-based designs reach higher fault coverage in test programs with far fewer engineering hours spent developing test vectors. Reaching 99% stuck-at fault coverage with less than three hours of CPU time is common for scan ATPG. This results in a higher quality product that reaches market faster. Design For Testability (DFT) is becoming increasingly important to the overall success of new systems, and scan-based design is the most mature DFT technique. A device can be tested with scan-based tests while it is resident in the circuit board. Scan-based tests can be implemented for boards and systems by incorporating boundary scan onto the devices.

LSI Logic offers scan ATPG as a service to those customers who don't have ATPG software themselves. Customers can now take advantage of all the benefits of scan-based DFT without having to make the capital expenditures or learn the complexities of the ATPG software. Customers can rely on the LSI Logic expertise of Right-First-Time™ success for scan-based testing.

Features

LSI Logic has developed a comprehensive methodology for designing a fully synchronous scannable device, and has attained a high level of expertise in scan design methodology. LSI Logic has successfully delivered hundreds of scan-based designs.

LSI Logic has invested significant resources in scan design software, layout programs, tester hardware, documentation and other support functions. Customers can leverage this significant investment in their designs by utilizing our tools and services.

Software

The software enhancements to the MDE® (Modular Design Environment®) Design Tools for ATPG include a Design Methodology Checker (LDMC) and a Scan Chain Creator (LSCAN). These software programs allow greater flexibility for the designer to select scan elements and connection order manually, or to allow the software to make the selections. During the layout process the scan chain order can be optimized to reduce routing congestion.

ATPG algorithms, such as the D-Algorithm, are well known for scan-based designs and have attained very high fault coverages (even 100%). LSI Logic uses a modified D-Algorithm (FAN) as well as other heuristics. Full scan design requires all memory elements (flip-flops or registers) to be directly controllable through the scan chain, which causes the circuit to appear completely combinatorial (logic). All buried states in sequential machines are thus controllable and observable, thereby making ATPG practical. Partial scan, where some of the register elements are not part of the scan chain, is not supported in the LSI Logic full scan methodology. An entire test pattern can be automatically generated in a matter of hours, with fault coverage from such ATPG runs consistently above 97%, and often above 99.5%.

LSI LOGIC

Fault Grading
Design Services

Overview

LSI Logic's Fault Grading design service combines state-of-the-art software with hardware acceleration to provide a cost effective quality improvement methodology. Through Fault Grading of the test patterns, the designer can determine the effectiveness in detecting potential manufacturing defects. The results of Fault Grading simulation can be used as a tool to modify the test program and increase the fault coverage. This improves the quality of tested devices. Simulation and design files are sent for fault simulation processing to computer accounts in Milpitas, California, or other design centers where Zycad hardware accelerators are located. Reliable, accurate and convenient fault simulation based on exhaustive or statistical methods is provided, accompanied by comprehensive, easy-to-analyze reports.

Benefits

LSI Logic's Fault Grading design service addresses the complex issue of assessing test vector completeness. By utilizing this fully integrated environment, the designer doesn't need to learn any additional procedures, methodologies or languages. This saves time and reduces potential sources of errors that can occur with complicated translations.

The fault simulations are performed on Zycad hardware accelerators using fault models that are built into LSI Logic macrocell libraries at the primitive level. The Zycad simulator is "socketed" into the MDE® Design Tools.

Studies show that high fault coverage test programs are directly related to higher quality levels and lower defect rates in end products. This saves significant production costs by reducing yield loss, returns and repairs of electronic equipment. Product quality is becoming a product differentiator with ever increasing importance. Reliance on tools such as Fault Grading is becoming more important in managing the increasing complexity of ASIC (Application-Specific Integrated Circuit) design.

Unless a structured design approach (such as scan test) is used, the responsibility of the test program is in the hands of the circuit designer rather than the ASIC manufacturer. Therefore, the quality of the product delivered will depend on how thoroughly a functional test can be produced by the designer. LSI Logic helps the designer by providing industry-leading tools and services to attain the highest level of ASIC design and quality.

Many designers rely on high node toggle coverage to obtain quality test programs. LSI Logic design methodology requires that a designer obtain 100% node toggle coverage, but this does not ensure the highest possible fault coverage (and therefore, quality). In order for the test program to be effective in detecting potential faults, each toggle node must have the toggle data propagate to an output pin of the device. This fault observability is what Fault Grading checks for and why only high fault coverage, not node toggle coverage, can guarantee high quality end product.

LSI LOGIC

SPICE Models
Design Services

Overview

LSI Logic supports SPICE I/O models for licensing to customers. Models are available for most technologies. These models are for I/O cells only, not internal macrocells. The models are designed only for use with META Software HSPICE, not Berkeley SPICE or P-SPICE.

Benefits

The SPICE I/O models simulate the output characteristics and input capacitance of LSI Logic I/O buffers. The designer creates his own circuit board simulation to check the operation of the board level circuit. This can also be used for "what if" calculations. When there is heavy capacitance, long traces or concern about round trip delay and signal integrity (reflections and ringing) in a board design, the designer can use SPICE simulations to analyze circuit operation.

Simulations can be run for worst case (weak N, weak P) and best case (strong N, strong P) conditions of the P and N transistors.

LSI Logic guarantees that silicon passes LDS®, MDE® Design Tools simulator approved tests which specify output buffer delays into a lumped capacitance rather than to SPICE simulations. Test programs for all designs are generated from MDE Design Tools and cannot be modified to reflect SPICE results.

Features

SPICE I/O models are comprised of subcircuit and transistor parameter text files compatible with META Software's HSPICE, version H8701 or higher.

Models for slew rate control versions of output buffers are included in the library. Each I/O buffer is formed by subcircuits. For instance, the BT4 is constructed of a predriver, an inverting buffer and a clamp diode. Each of these subcircuits is constructed of P and N transistor models. Transistor models exist for all process variations:

- Nominal
- Weak
- Strong
- Weak N strong P
- Strong N weak P

Parameters for poly and metal capacitance are also included.

The P and N transistor models include the following parameters:

NRD	NRS	ACM	HDIF	CAPOP
BULK	VTO	TOX	NSUB	LD
XL	WD	XW	UO	UCRIT
UEXP	UTRA	XJ	RSH	NEFF
VMAX	DELTA	CJ	MJ	CJSW
MJSW	OGDO	OGSO	OGBO	

Support

Maintenance service for SPICE I/O models is not required. The models are considered stable and do not require updates. Questions regarding these models should be directed to your local applications engineer.

Any questions regarding use of HSPICE should be directed to META Software in Campbell, California, phone number 800.346.5953 or 408.371.5100.

LSI Logic is unable to support any questions arising from usage of these models in software other than HSPICE.

LSI LOGIC

Layout
Design Services

Overview

LSI Logic offers custom tailoring of every design through the use of proprietary, state-of-the-art layout design tools, optimized for both our array-based and cell-based ASIC (Application-Specific Integrated Circuit) products. Several levels of layout complexity are offered, enabling a choice of cost/performance solutions. The standard layout is included with every NRE for a new design. The merge layout is for small changes to an original LSI netlist. Trial layout has two types. One type of trial layout is for timing performance evaluation and another is for determining die size. Custom layout is for designs pushing the limits of the standard design criteria. These designs will require handcrafting of the layout in order to meet extraordinary design objectives.

Standard Layout

Included in every new design NRE is the standard layout. LSI performs a comprehensive series of procedures to ensure a clean, efficient layout for every design. There are over 30 steps in LSI's layout procedure. Each step must be signed off along the way, ensuring a quality layout is achieved.

Merge Layout

A merge is when a small change is made to a completed layout. That is, the change is merged into the original database. Merges only work for very small changes in the netlist. Even a relatively small change may not work if the change causes a chain-reaction to many more nets that drive it, or are driven by it. The maximum merge amount is 50 macrocells or 100 gates. There is no limit when gates are subtracted. However, any design over 40% utilization is not eligible for a merge layout. This is because in larger designs the chain-reactions increase beyond routibility.

Trial Layout for Speed Evaluation

Wire length estimates for pre-layout simulation generated by LSI's FloorPlanner™ program are generally adequate for simulation of most designs. However, some design architectures are dependent on precise delay path predictions. The designer in these cases must make design tradeoffs based on the precise delay path predictions before handing off the final netlist for layout (ECR). This is much different than creating the fastest possible layout configuration, defined as the optimum total delay sum on all nets in a design, which can be done without going through a trial layout phase. The customer must determine whether or not this kind of trial layout is necessary for the design objectives set.

There are two ways of performing trial layout for speed evaluation:

- Auto route only (leave the drops unconnected)
- Finish all nets (connect the drops as in a full layout)

The cost difference between the two options can be significant since finishing the drops will be time consuming and involves manual intervention. In the case of the auto route only option, any critical net necessary for timing analysis is so noted and completed first. This produces a SEGLEN file with only the completed nets. The unconnected nets must have timing information inserted from the pre-layout estimated file.

When a timing analysis requires all nets to be completed, the full standard layout procedure is completed in its entirety.

A SEGLEN file contains actual wire lengths. This is used by LDEL to calculate the delay times for back-annotation into MDE® Design Tools for precise timing analysis.

LSI LOGIC

Applications Engineering Support
Design Services

Overview

LSI Logic has produced over 10,000 ASIC (Application-Specific Integrated Circuit) designs to date. LSI offers the support of the most experienced field applications engineering organization in the ASIC industry. This resource is available to our customers at different levels of support as stated in the purchase agreements. It is also possible to obtain applications support services for specific objectives.

LSI Facilities

LSI Logic operates 39 design centers worldwide. These facilities include the latest high performance workstations available for customer use. Customers may use this equipment without making the capital budget expenditures, while gaining access to the latest LSI Logic MDE® Design Tools.

Applications engineers are available for consultations whenever the customer is engaged in design activity at the LSI Logic facilities. This is particularly valuable for first time MDE Design Tools users. All LSI Logic MDE Design Tools are available for use by customers at design centers, although the usage fee may vary depending on the type of software desired.

Consulting Support

LSI Logic has extensive system level architectural experience. Major workstation suppliers have designed multiple LSI Logic ASICs into their most advanced workstations. Architectural partitioning at the system and chip level was accomplished with the aid of LSI Logic experience and expertise. LSI Logic is expert in many different system design disciplines, including:

- Architectural partitioning
- Design methodologies
- Testing methodologies
- SPICE analysis of board level interconnects
- Clock distribution architectures
- Technology assessments/tradeoffs
- Design system configurations

The basic design flow for ASICs has not changed much over the last few years. What has changed is the migration in the bulk of the design task to earlier in the design cycle. The proper decisions at the early stages of the design will pay huge dividends later.

On Site Applications Support

LSI Logic applications engineers may be sent to the customer's site to perform any of these support functions. If there will be substantial interaction between customer and vendor engineers, it is more convenient to tackle these situations directly at the customer site where the work is being performed.

Applications engineers may be assigned full time to a customer site for extended periods of time if warranted by the size and scope of the design effort.

LSI LOGIC

Array-Based ASICs

LSI LOGIC

LCA200K Compacted Array Turbo Series
Preliminary

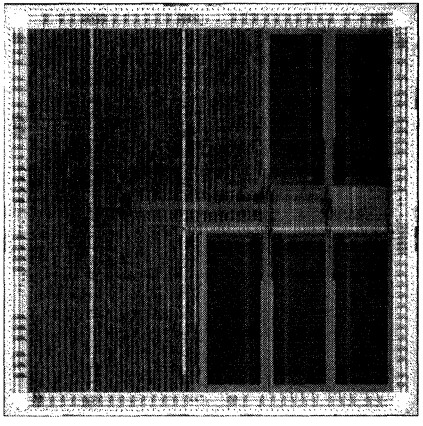
Description

The LCA200K Compacted Array™ Turbo series is a submicron array-based HCMOS product family offering extremely high performance and density. The LCA200K is manufactured using 0.7-micron drawn gate length (0.55-micron effective channel length) silicon gate HCMOS technology. The advanced feature size of the LCA200K translates into high performance with gate delays of 270ps and maximum flip-flop toggle frequency of 300 MHz. LSI Logic proprietary library elements such as the phase locked loop for minimizing system clock skew, and new high-performance I/O, dramatically increase system performance capability.

The LCA200K utilizes LSI Logic's Channel-Free™ architecture, which constitutes an array core filled with potentially active transistors connected through either two layers of metal interconnect in the LCA200K product line or three layers in the LCA210K product line. Integration of cache memories and microcode is possible through customer defined memory capability up to 36K bits of SRAM and 160K bits of ROM. The largest masterslice is capable of integrating 32K bits of SRAM, 16K bits of ROM, and over 100,000 random gates.

LSI offers one of the largest libraries in the industry including SSI/MSI circuitry and complex industry standard Intel, AMD and Motorola functions, as well as SPARC and MIPS microprocessors and peripherals. This robust library yields many distinct architectural solutions to a given system design, allowing the designer to make performance, functionality and cost tradeoffs.

The LCA200K is supported by LSI Logic's proprietary C-MDE™ (Concurrent Modular Design Environment) Design System that allows a design to be captured and simulated prior to fabrication. New enhancements in the delay prediction scheme utilize piecewise linear modeling of cell outputs as well as considering cell input ramp times and thresholds, providing accurate delay modeling and enabling the designer to access the true performance capabilities of the LCA200K. Optimum performance and efficient layout are assured by consideration of the design hierarchy during the simulation phase of the design. Cell compilation, floorplanning and hardware acceleration are available to expedite the design of ASICs (Application-Specific Integrated Circuits) up to 200,000 random gates.



Typical LCA200K Compacted Array Turbo Device

LFT150K FasTest Array Series
Preliminary

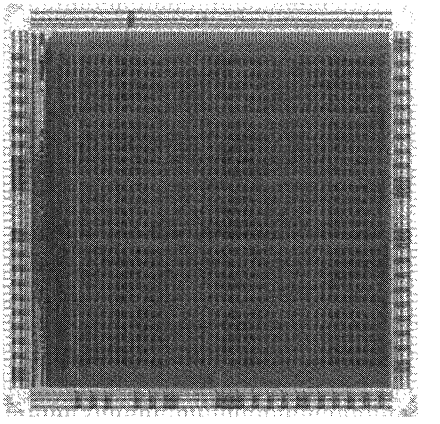
Description

The LFT150K FasTest™ Array series is a unique Array-Based ASIC (Application-Specific Integrated Circuit) product line incorporating the patented CrossCheck technology. This new family of arrays provides the customer a new design for test (DFT) methodology that transparently generates a very high quality test in zero test development time. This enhances designer productivity and reduces the time-to-market.

The FasTest Array series is suited for high performance, complex applications where quality, reliability, fast time-to-market and time-to-production are driving requirements. All design styles are supported from totally asynchronous through to completely synchronous with a single clock. A wide spectrum of applications are enabled by the FasTest Array series to enjoy the benefits of the ASIC technology without compromising test.

The core of the four masterslices consists of an array of proprietary sea-of-gates cells that support the extensive, macrocell library of the Compacted Array™ products offered by LSI Logic. The performance of each cell is not altered by the CrossCheck technology providing the designer with a solution to critical timing problems in complex designs. The MDE® Design Tools achieve extremely high utilizations of the arrays providing support of design complexities from 30,000 to 80,000 used gates. LSI Logic's proven experience at implementing complex designs is enhanced by the CrossCheck technology to provide very high fault coverage with no additional effort.
The periphery of the arrays have proven structures that support all of the I/O functions such as TTL and CMOS compatible inputs, multi-drive and slew-rate controlled outputs, 3.3 V and ECL interface I/Os that are supported in other LSI Logic Compacted Array series.

The hardware implementation of the embedded CrossCheck structures is supported by a suite of software tools that performs fault grading and ATPG to achieve a test tape that verifies the design. The software has been fully integrated into the MDE software which allows designers to work productively due to familiarity with a widely used and interfaced platform.



Typical LFT150K FasTest Array Device

Features

- Quality test transparent to the designer in "ZERO" time
- Observability of "real" manufacturing defects
- Greater than 98% stuck-at fault coverage
- Comprehensive fault modeling capability
- Highest performance structured test solution
- Test vector generation service
- 30K to 80K usable gates and up to 414 I/Os
- Four FasTest Array masterslices (with CrossCheck technology)
- Qualified 1.0-micron CMOS process technology
- Fault simulation and ATPG tools integrated with MDE Design Tools

LCA100K Compacted Array Plus Series

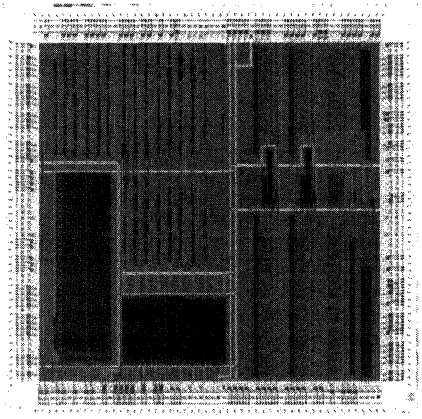
Description

The LCA100K Compacted Array Plus™ series is an HCMOS Array-Based ASIC (Application-Specific Integrated Circuit) product offering extremely high performance. The LCA100K series is manufactured using 1.0-micron drawn gate length (0.7-micron effective channel length) silicon gate HCMOS technology. Twelve masterslice options provide from 6,580 to 234,916 equivalent gates. Two layers of metal interconnect are used to implement circuits of greater than 100,000 gates in complexity. LSI Logic's Channel-Free™ architecture is employed in the array core, which is completely filled with potentially active transistors. A total of 438 pads are available on the largest masterslice for use in most industry standard packages.

The LCA100K is ideally suited for system-to-silicon integration. Sophisticated simulation algorithms incorporated in LSI Logic's proprietary MDE® Design Tools allow very complex circuits to be accurately modeled prior to fabrication. Optimum performance and efficient layout are assured by consideration of the design hierarchy during the simulation phase of design. Cell compilation, floorplanning and hardware acceleration are available to expedite the design of very large ASIC chips of over 100,000 gates complexity.

Applications for highly integrated array products such as the LCA100K Compacted Array Plus series include proprietary CPU designs and artificial intelligence processors. Parallel processor designs can benefit substantially from the high gate density of the LCA100K.

Applications formerly implemented with software, such as image processing and speech recognition/synthesis algorithms, can be performed in real time with the speed and density of the LCA100K. These high speed CMOS arrays allow digital signal processing to supplant all but the most advanced analog processing techniques.



Typical LCA100K Compacted Array Plus Device

Features

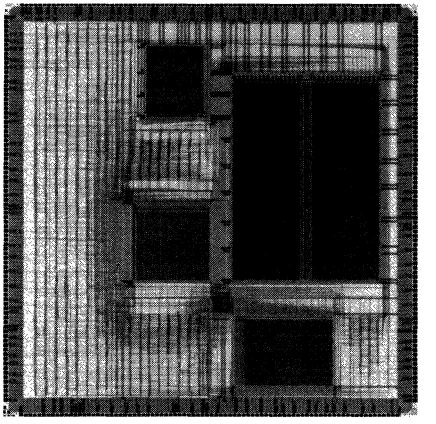
- Greater than 100,000 usable gates
- Silicon gate, 1.0-micron gate length, HCMOS technology
- Channel-Free architecture for maximum layout flexibility
- Fully integrated with LSI Logic's MDE Design Tools
- High speed performance: 350 ps average through high drive NAND (ND2P) gate. 430 ps average through standard drive 2-input NAND gate. Standard load = 2, VDD = 5 V, TA = 25°C
- Twelve array sizes from 6,580 gates to 234,916 available gates
- Up to 418 signal I/O with choice of:
  - Input, output, or bidirectional buffers
  - HCMOS or TTL input levels
  - Schmitt trigger inputs
  - Configurable output drive up to 48 mA with slew rate (dV/dt) control capability
- 3.3 V I/O interface capacity
- Power dissipation 3.0 µW/gate/MHz
- Compilable ASIC memory (up to 32K RAM/128K ROM) plus logic implemented on one chip
- Extensive library of macrocells, macrofunctions, megafunctions and standard memory configurations
  Over 400 macrocell and 300 megafunction types available. Standard and high-drive versions of macrocells and macrofunctions for speed and gate usage optimization.
- Full netlist compatibility with all other LSI Logic ASIC products

LEA100K Embedded Array Series

Description

The LEA100K Embedded Array™ Series is an HCMOS ASIC (Application-Specific Integrated Circuit) product which combines the benefits of cell-based and array-based ASICs. Design-specific, standard cell format embeddable cores offer high density and performance rivaling full custom design methodologies. Memory, microprocessors, megacells and any user-defined semicustom cores may be placed in any location on the user-defined masterslice. The remaining area is filled with potentially active transistors using LSI Logic's Channel-Free™ architecture.

The LEA100K series is manufactured using 1.0-micron drawn gate length (0.7-micron effective channel length) silicon gate HCMOS technology. This technology provides the advantages of ECL speeds with the lower power consumption and the higher noise margin characteristics of CMOS technology. With the added capability to incorporate very high density cell-based memory blocks, LEA100K Embedded Arrays offer an effective, high performance, high density design capability to implement virtually any digital logic design.



LEA100K Embedded Array Series Device

The LEA100K Embedded Array series offers the very high density and high performance of a cell-based ASIC design, with gate array turnaround time.

Features

- Silicon gate 1.0-micron drawn gate length HCMOS technology
- LCA100K Compacted Array Plus™ series proto turnaround time
- Array production leadtimes available through wafer bank program
- LCB007 Series of cell-based ASIC density and performance
- Up to 150,000 equivalent gate capacity
- Up to 422 signal I/O
- High density memory blocks:
  - High speed static RAM up to 144K bits
  - Up to five ports available
  - Contact programmable ROM up to 1M bits
- Megafunctions (soft-coded LSI and MSI building blocks) including:
  - RISC Microprocessors and Floating Point Controllers
  - Motorola, Intel and AMD peripherals
  - Communication controllers
  - Generic adders, multipliers, MACs and CAMs
  - Barrel shifters, FIFOs, LIFOs and ALUs
  - All megafunctions may be converted into megacells (hard-coded large building blocks)
- Extensive macro libraries
- Hierarchical functional placement
- Clock driver distribution methodology
- Full netlist compatibility with all other LSI Logic ASIC products
- Full military capability
- Fully supported by LSI Logic's MDE® Design Tools

LCA10000 Compacted Array Series

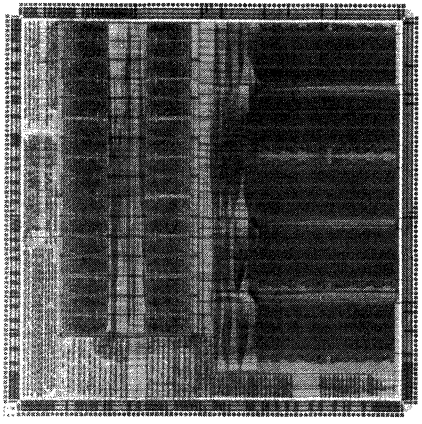
Description

The LCA10000 Compacted Array™ series is an HCMOS semicustom technology offering speed performance equivalent to 10K ECL, combined with very high gate counts. The LCA10000 series is processed using 1.5-micron drawn gate length (0.9-micron effective channel length), 2-layer metal HCMOS technology and is based on a Channel-Free™ array, completely filled with potentially active transistors. Densities from 25,740 to 129,042 equivalent gates are offered. Up to 348 signal I/Os are available from the larger members.

The speed and range of gate counts available in the LCA10000 series make it ideally suited for achieving system-to-silicon integration. Sophisticated algorithms incorporated in LSI Logic's proprietary MDE® Design Tools allow a circuit designer's modular hierarchy to be utilized to its maximum potential. By performing an optimized functional placement of these building blocks, and then collapsing and compacting them to minimum size, substantial benefits are realized in both device speed and silicon area utilization.

Output buffer drive strengths of 1, 2, 4, 6, 8, 12 mA and 24 mA (24 mA available with commercial specifications only) are available and determined by the user during the design phase. A slew rate control circuit is available that allows the dV/dt of each output to be tailored to individual load conditions.

The Compacted Array shown below demonstrates the versatility of Channel-Free architecture in efficiently implementing random logic, wide buses and memory elements.



Typical LCA10000 Compacted Array Device

Features

- Up to 50,000 usable gates
- 1.5-micron silicon-gate length, 2-layer metal HCMOS technology
- Speeds equivalent to 10K ECL, 450 ps through high-drive NAND (ND2P) gate, 550 ps through standard drive, 2-input NAND (ND2) gate (standard load = 2, VDD = 5 V, TA = 25°C)
- Up to 348 signal I/O capability
- Extensive library of over 400 macrocell and 300 megafunction types available, as well as standard memory configurations; standard and high-drive versions available for speed and gate usage optimization
- Six array sizes from 25,740 to 129,042 gates
- Fully integrated with LSI Logic's MDE Design Tools
- Channel-Free architecture for maximum layout flexibility
- Random routing with hierarchical functional placement
- Configurable output drive up to 12 mA (24 mA available with commercial specifications only) with slew rate control capability
- 3.3 V input and output capability
- Compilable Application Specific Integrated Circuit (ASIC) memory (up to 16K RAM and 64K ROM) plus logic implemented on one chip
- TTL/CMOS I/O compatibility
- Inputs and outputs protected from overvoltage and latch-up
- Efficient implementation of large logic blocks
- Clock driver distribution methodology
- Advanced packaging techniques
- ESD protection: 2001 V

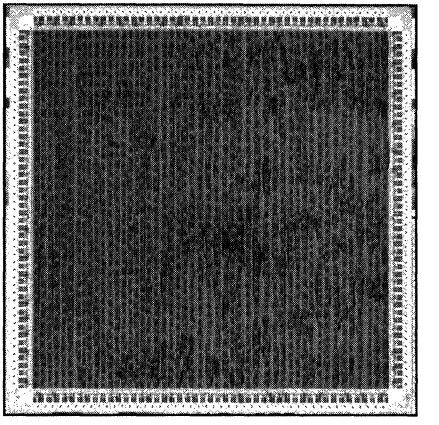
LSI LOGIC

LMA9000
Micro Array Series

Description

The LMA9000 Micro Array series is an HCMOS semicustom technology offering both speed and performance equivalent to 10K ECL and high gate density ASICs. The LMA9000 Micro Array series is processed using 1.5-micron drawn gate length (0.9-micron effective channel length), 2-layer metal HCMOS technology and is based on LSI Logic's Channel-Free™ architecture, in which potentially active transistors fill the array core. Arrays ranging from 1,968 to 34,944 available gates are offered. The largest micro array has up to 174 available signal I/Os. The LMA9000 series uses small device structures which exhibit low power consumption. The series is well suited to be used as a high reliability universal logic design vehicle, able to integrate entire printed circuit boards into a single array.

The larger micro arrays can be used for VLSI implementation of high performance subsystem architectures such as intelligent special purpose processors or multifunction controllers. The smaller members can be used for replacement of high speed Schottky TTL or 10K ECL logic. Midrange micro arrays are ideal for high performance dedicated peripheral controllers, intelligent support functions, etc. A large library of macrocells, macrofunctions, megafunctions, metal-megacells, RAMs and ROMs is available to simplify the conversion of existing logic designs or to easily produce new circuit designs.



Typical Micro Array Die

Features

- 1.5-micron silicon gate length, 2-layer metal HCMOS technology
- Gate speed equivalent to 10K ECL; faster than 74S TTL; 0.57 ns through 2-input NAND gate, standard load = 2, VDD = 5 V, TA = 25°
- Up to 174 signal I/O capability
- Extensive macrocell, macrofunction, megafunction, metal-megacell and memory library
- Ten array sizes from 1,968 to 34,944 gates
- Fully supported by LSI's MDE® Design Tools for verification, simulation and layout
- Channel-Free architecture for maximum layout flexibility
- Random routing with hierarchical function placement
- Configurable output drive up to 12 mA with slew rate control
- Over voltage and latch-up protection for I/Os
- TTL/CMOS I/O compatibility
- Efficient implementation of large logic blocks
- Extensive selection of ceramic and plastic packages
- ESD protection greater than 2001 V
- Functionally compatible with LL7000 and LL9000 macrocell and macrofunction libraries
- Full military capability

BiCMOS LDD10000 Direct Drive Array Series

LSI LOGIC

Description

The LDD10000 Direct Drive™ Array series is a BiCMOS Array-Based ASIC (Application-Specific Integrated Circuit) offering the fast speed, low power dissipation and very high gate count of a CMOS Compacted Array™ device, and the high output load driving performance of LS or AS bipolar TTL.

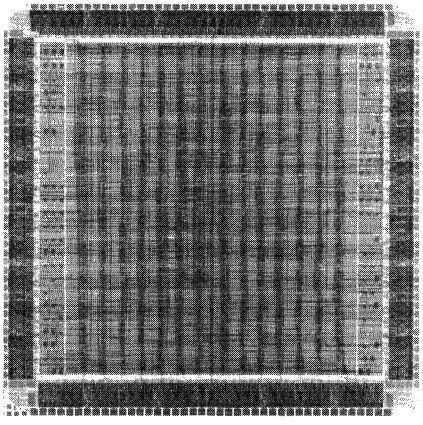
The LDD10000 series is manufactured using a BiCMOS process that has 1.5-micron drawn gate length (0.9-micron effective channel length), 1.5-micron bipolar emitters, and two metal layers. The proprietary 3-region architecture shown in figure 1 consists of (1) high density CMOS Channel-Free™ gates, (2) peripheral BiCMOS blocks for high drive of internal loads and (3) BiCMOS I/O buffers with additional gates to implement basic macrocells.

The major portion of each array consists of Channel-Free CMOS logic gates, making the LDD10000 series functionally compatible with existing Compacted Array logic/memory libraries and design software. Optimization of selected internal speed-critical paths is possible using the BiCMOS blocks to drive high-fanout nets such as clock lines and buses. In addition improved I/O characteristics, I/O modules can be configured as flip-flops, latches and gates to allow easy integration of TTL standard logic devices into the I/O area.

Sophisticated algorithms incorporated in LSI Logic's proprietary MDE® Design Tools allow very complex circuits to be accurately modeled prior to fabrication. Optimum performance and efficient layout are assured by consideration of the design hierarchy during the simulation phase.

Cell compilation, floorplanning and hardware acceleration are available as options to expedite the design process.

Output drive strengths of 6, 12 and 24 mA with selectable TTL or CMOS levels are possible from a single I/O module. Three output buffers can be used in parallel for 72 mA drive capability, allowing direct interface to common bus specifications such as VME and Multibus. Differential TTL and backplane transceivers can be implemented for line drivers and high-speed, high-data integrity bus communication applications. A series termination resistor, selected during the design phase, is provided to tailor output characteristics and minimize bus ringing.



Typical LDD10000 Direct Drive Array chip with 3-region architecture highlighted

Features

- 1.5-micron gate length, micron poly-silicon emitter BiCMOS technology
- BiCMOS output buffer performance equivalent to LS or AS bipolar TTL (4.2ns, conditions: 25 mA TTL output, C_L = 100pF, VDD = 5 V, TJ = 25°C)
- Eight array sizes from 7,198 to 116,778 available gates
- Fully supported by LSI Logic's MDE Design Tools
- 3-region architecture for optimized performance and density
- CMOS Channel-Free gate core is directly compatible with existing logic and memory libraries
- BiCMOS blocks allow speed enhancement of heavily loaded internal nets
- I/O modules can implement logic functions such as basic gates, latches and flip-flops
- Configurable output drive up to 24 mA per I/O module or parallel buffers for 72 mA maximum rating

BiCMOS LAD310 Analog/Digital Array Series
Preliminary

LSI LOGIC

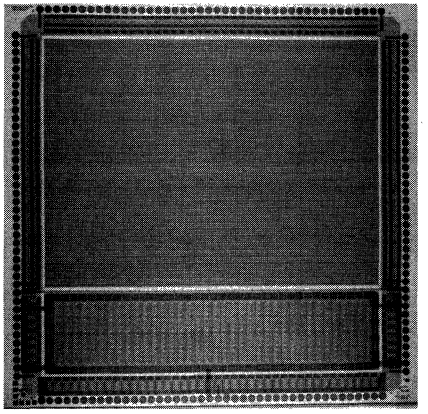
Description

The LAD310 Analog/Digital Array series is a BiCMOS array-based ASIC (Application-Specific Integrated Circuit) offering high performance bipolar and CMOS analog functions combined with the speed, low power dissipation and very high gate density of a digital CMOS Compacted Array™.

The LAD310 series is manufactured using a BiCMOS process that has 1.5-micron drawn gate length (0.9-micron effective channel length) CMOS devices and 1.5-micron bipolar emitters (Ft=6 GHz) and two metal layers. The array architecture is shown in figure 1 and consists of two distinct sections. The upper part of the chip contains a digital CMOS Compacted Array surrounded on three sides by digital I/O buffers. The lower part is an analog tile array with analog I/O buffers also available on three sides of the tiled region.

Equivalent gate densities for the digital section range from 1512 to 114,987 available gates with up to 239 digital I/O pads. The analog section has from 96 to 672 available tiles depending on the array size (approximately 4 tiles are required to construct a basic operational amplifier) and 97 analog I/O pads on the largest member.

The ability to implement high performance analog and digital functions on a single chip makes the LAD310 series ideally suited for total system integration onto silicon. Using a Channel-Free™ architecture throughout the array assures maximum silicon utilization and direct compatibility with existing Compacted Array logic/memory libraries and design software for the digital section. An extensive library of precharacterized analog functions is available to expedite the design process in the analog section. Each function makes selective use of both MOS and bipolar devices to implement accurate, high speed and



Array Architecture

low noise building blocks. The analog designer can choose the specifications of a function to optimize the circuit for a particular application.

Sophisicated algorithms incorporated within LSI Logic's proprietary MDE® Design Tools allow very complex circuits to be accurately modeled prior to fabrication. Optimum performance and efficient layout are assured by consideration of design hierarchy during the simulation and layout phase.

Digital output buffer drive strengths of 1,2,4,6,8 and 12 mA are available in the digital section and determined by the user during the design phase. Also available is a slew rate control circuit that allows the dV/dt of each output to be tailored to individual load conditions. Analog output buffers with emitter follower and push-pull configurations are available with up to 50 mA drive capability. ECL logic can also be integrated within the analog section of the array with pseudo ECL interface.

Features

- 1.5-micron gate length poly-silicon emitter BiCMOS process
- Analog and digital functions on a single chip
- High-performance bipolar analog functions: 800 MHz wide band operational amplifiers, 3 ns high-speed comparators
- High-speed digital CMOS logic: 0.57 ns through 2-input NAND gate, standard load = 2, VDD = 5 V, TA = 25°C
- Seven array sizes: 1512 to 114,987 digital gates, 96 to 672 analog tiles
- Advanced packaging techniques
- Up to 239 digital I/O and 97 analog I/O
- Channel-Free architecture throughout array for maximum layout flexibility and silicon utilization
- Pre-characterized library of analog functions
- Digital section is directly compatible with existing logic and memory libraries
- CMOS, TTL, ECL and analog I/O capability
- ESD protection to 2001 V and latch-up immunity
- Full military specifications supported including MIL883 and CECC90000 (H)

RHASIC LRH10000 Radiation Hardened Series

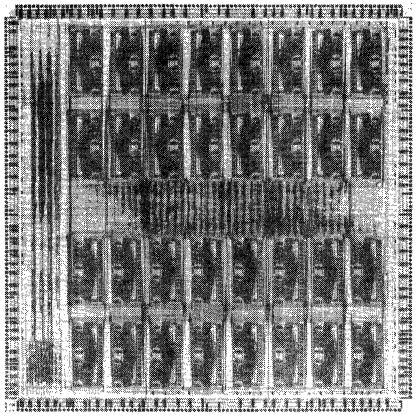
LSI LOGIC

Description

RHASIC is the LSI Logic family of radiation hardened ASICs (Application-Specific Integrated Circuits). The LRH10000 Compacted Array™ series is a radiation hardened HCMOS semicustom technology offering speed performance equivalent to 10K ECL, combined with high gate counts. The LRH10000 series is processed using 1.5-micron drawn gate length (0.9-micron effective channel length), 2-layer metal, epitaxial bulk silicon HCMOS technology. The LRH10000 is a Channel-Free™ array, completely filled with potential active transistors. Densities from 25,740 to 129,042 equivalent gates are offered. Usable gate capacity of 50,000 gates and up to 348 signal I/Os are available.

The speed and range of gate counts available in the LRH10000 series make it ideally suited for achieving system-to-silicon integration. Sophisticated algorithms incorporated in LSI Logic's proprietary MDE® Design Tools development software allow a circuit designer's modular hierarchy to be utilized to its maximum potential. By performing an optimized functional placement of these building blocks, and then collapsing and compacting them to minimum size, substantial benefits are realized in both device speed and silicon area utilization.

Output buffer drive strengths of 0.8, 1.6, 3.2, 4.8, 6.4 and 9.6 mA are available and determined by the user during the design phase. Also available is a slew rate control circuit that allows dV/dt of each output to be tailored to individual load conditions.



LRH10000 Compacted Array Chip

Overview

- Guaranteed total dose specification 1 x 10^6 rad(Si)
- Total dose functional to >1 x 10^7 rad(Si)
- Upset resistant for dose rates up to 1 x 10^9 rad(Si)/sec
- Latch-up resistant to dose rates ≤10^{12} rad(Si)/sec
- SEU <5 x 10^{-9} errors/bit-day measured at room temperature on latch type memory structure without cross-coupled resistors. Actual value will be design and layout dependent.
- No SEU latchup for 240 MeV Br ions
- Silicon-gate 1.5-micron gate length, 2-layer metal HCMOS technology
- Speeds equivalent to 10K ECL— 0.57 ns through 2-input NAND gate, standard load = 2, VDD = 5 V, TA = 25°C
- Up to 348 signal I/O capability
- Extensive macrocell, macrofunction and megafunction library elements (directly compatible with industry standard LCA10000 series)
- Six array sizes from 10,000 to 50,000 usable gates
- All design and manufacturing done in the USA
- Fully supported by MDE Design Tools for verification, simulation and layout
- Channel-Free architecture for maximum layout flexibility
- Random routing with hierarchical functional placement
- Configurable output drive up to 9.6 mA with slew rate control capability
- Inputs and outputs protected from over-voltage and electrical latchup
- TTL/CMOS I/O compatibility
- Efficient implementation of large logic blocks
- Clock driver distribution methodology
- Advanced packaging available
- ESD protection: 2000 V
- Military capability up to MIL-STD-883, Class S

RHASIC LRH9000 Radiation Hardened Series

LSI LOGIC

Description

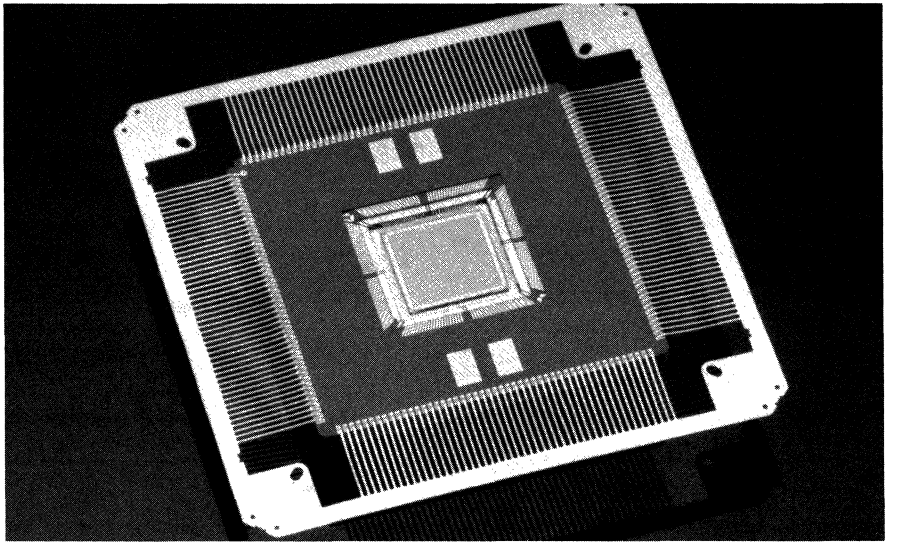
RHASIC is the LSI Logic family of radiation hardened ASIC (Application-Specific Integrated Circuits). The RHASIC LRH9000 series of radiation hardened silicon-gate HCMOS logic arrays exhibits bipolar speeds, while at the same time, offers high radiation resistance, low power consumption, high noise margins and ease of design.

The speed and range of gate counts available in the radiation hardened LRH9000 series make it ideal for LSI/VLSI implementation of a variety of high-performance functions that are required to operate in a radiation environment.

Features

- Total dose specification: 200 krads (Si); fully functional to 500 krads (Si)
- Upset resistant for dose rates $\leq 1 \times 10^9$ rads (Si)/sec
- No latch-up observed up to 10^{12} rads (Si)/sec (limit of source capability)
- SEU $<10^{-8}$ errors/bit-day (Adams 10% worst-case)
- No SEU latch-up
- Speeds higher than 74S TTL – 1.1 ns (1)
- Epitaxial silicon substrates
- Silicon-gate 1.5-micron drawn gate length (1.1-micron effective channel length) HCMOS technology
- Two levels of metal interconnect
- Compatible with the industry standard LL9000 series macrocell and macrofunction libraries
- Optimal structure of two n-channel and two p-channel transistors
- Complexities ranging from 1,443 to 10,013 gates
- Ceramic package pin counts ranging up to 224
- Custom packaging available
- All design, manufacturing including assembly done in USA
- Fully supported by LSI Logic's MDE® Design Tools for pre- and post-radiation conditions
- All non-power pads configurable as inputs, outputs or bidirectional I/O
- TTL/CMOS I/O compatiblity
- Configurable output drive up to 9.6 mA
- Input protection circuitry
- LRH9320Q evaluation device available
- Secure design and manufacturing facilities
- Military capability up to MIL-STD-883, Class S

LRH9000 Device in Leaded Chip Carrier



Notice: The United States Government imposes special requirements for the authorization to export semiconductor products that are designed or manufactured to provide radiation hardening or radiation tolerant qualities

L63500 DATAC ARINC 629 Terminal Device
Preliminary

Introduction

The L63500 data bus terminal controller is specified in ARINC 629. Primarily developed to function as a bus interface terminal in a multiple transmitter data bus, the L63500 simplifies I/O design and allows flexibility in the physical layout of user systems. In addition, it minimizes problems associated with centralized data communication systems – loss of all communication, application complexity, etc. The L63500 is an ideal device for application in aircraft avionic "fly by wire" systems, factory automation systems, and other control systems requiring high reliability and performance. The L63500 is currently available in a 180-pin ceramic pin grid array. A surface mountable leaded chip carrier version is under development. Both package options are available processed to the requirements of Mil-Std-883 with operation guaranteed over the military 125°C/ -55°C temperature range.

During operation, bus access control is distributed among all terminals and decisions concerning transmission go-ahead are determined autonomously. The data bus access protocol is Carrier Sense Multiple Access-Clash Avoidance (CSMA-CA) which enables equal priority access for all terminals even during overload conditions. Under normal operating conditions the terminals transmit at a fixed update rate (periodic). When overload conditions exist the terminal transmits continuously (aperiodic) utilizing 100% of the bus.

Transmitted information (messages) is (are) formatted by the scheduler. Each message consists of a set of wordstrings which are stored in the transmit personality PROM. In addition, the wordstrings contain labels which provide subsystem identification. Once the transmitted information is received by another terminal, the serial data is decoded and tested for proper format. The label of each wordstring is compared to the information stored in the receive personality PROM. If correlation between the personality and transmitted data exists, then the subsystem will initiate the proper I/O activity. If no correlation exists the system will remain idle.

During transmission the receiver acts as a data monitor. Erroneous transmissions are terminated and after seven consecutive errors the transmitter is disabled.

Features

- ARINC 629 compliant
- Boeing certified
- Autonomous bus control
- Manchester II biphase coded serial data
- 2 megabit data rate
- Direct memory access capability
- Periodic and aperiodic protocol modes
- Provides transmit and receive interrupt vectors
- Automatic shutdown on error of transmitted data
- Data validation based on format and parity
- Voltage, current and fiber optic transmission media supported
- CMOS 1.5-micron drawn gate length (0.9-micron effective channel length) technology
- Low power dissipation
- +5 V supply voltage

LSI LOGIC

Cell-Based ASICs

LCB007 Series
Cell-Based ASICs

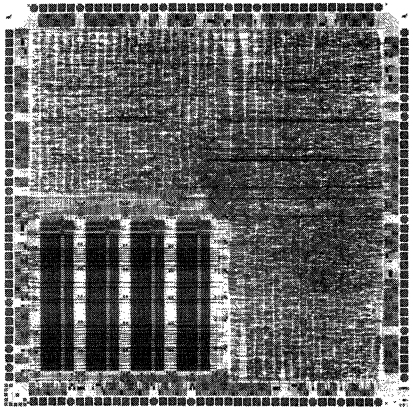
Description

The LCB007 series of Cell-Based ASICs (Application-Specific Integrated Circuits) is a family of standard cell format, semicustom solutions available for implementing a wide variety of complex logic functions for digital applications. Based on a 1.0-micron drawn gate length (0.7-micron effective channel length) HCMOS process technology, it offers very high density and high performance that rivals full-custom design methodologies.

Fully supported by LSI Logic's MDE® Design Tools, the easy-to-use LCB007 design tools produce circuits which are guaranteed to work the first time to predetermined specifications. The LCB007 also features many SSI, MSI, LSI and VLSI building blocks, including high-density memory capacities of up to 1M bit of ROM and 144K bits of RAM.

Features

- 1.0-micron gate length, 2-layer metal, silicon-gate HCMOS technology
- Up to 200,000 equivalent gate capacity
- High-speed performance:
  - 350 ps through high drive NAND (ND2C) gate
  - 450 ps through standard drive, 2-input NAND gate (ND2A) (standard load = 2, VDD = 5 V, TA = 25°C)
- Latch-up immunity over 200 mA
- Electrostatic discharge (ESD) protection of over 2001 V
- Up to 422 signal I/Os with choice of:
  - Input, output or bidirectional buffer
  - HCMOS or TTL input levels
  - Schmitt trigger inputs
  - Configurable output drive up to 24 mA (one slot 24 mA available with commercial specifications only) with slew rate control capability
  - 3.3 V input and output capability
- High-density memory blocks:
  - High-speed static RAM up to 144K bits
  - Up to five ports available
  - Contact programmable ROM up to 1M bit
  - Specialized memories, including FIFOs, LIFOs and CAMs
  - Memory blocks compiled to any user-specified widths and depths
- Extensive macro libraries:
  - Gate-level, SSI, MSI, LSI, VLSI and RISC building blocks
  - Over 200 macrocell and 300 macrofunction types available
  - Each macrocell available in a minimum of four drive strengths
- All megafunctions available as, or can be converted into, megacells
- Built-in scan circuitry for all megacells; user-defined test circuits on all memories; choice of system-level test structures for the balance of logic
- Full netlist compatibility with all other LSI Logic ASIC products
- Full military capability
- Fully supported by LSI Logic's MDE Design Tools
- Library compatible with 1.0-micron gate length LCA100K Compacted Array Plus™ Series and LEA100K Embedded Array™ Series



Typical LCB007 Series Cell-Based ASIC

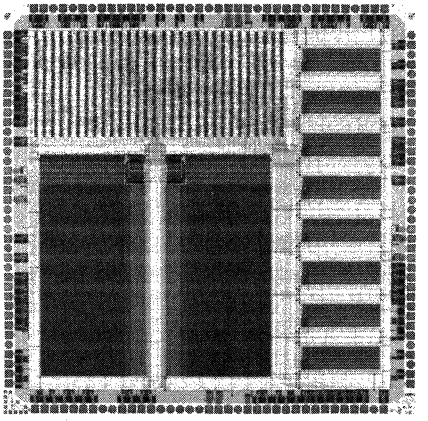
LSI LOGIC

LCB15 Series
Cell-Based ASICs

Description

The LCB15 Series of Cell-Based ASICs (Application-Specific Integrated Circuits) is a family of standard cell format, semicustom solutions available for implementing a wide variety of complex logic functions for digital applications. Based on a 1.5-micron drawn gate length (0.9-micron effective channel length) HCMOS process technology, it offers high density and high performance that rivals full-custom design methodologies.

Fully supported by LSI Logic's MDE® Design Tools, the easy-to-use LCB15 design methodology yields designs which are guaranteed to work the first time to predetermined specifications. The LCB15 also features many SSI, MSI, LSI and VLSI building blocks including high-density memory capacities of up to 2M bits of ROM and 144K bits of RAM.



Typical Cell-Based ASIC Design

Features

- 1.5-micron gate length, 2-layer metal, silicon gate HCMOS technology
- Up to 100,000 equivalent gate complexity capacity
- Typical gate delays of 570 ps (ND2C 2-input NAND gate with 8 standard loads, 5 V VDD, TA = 25°C)
- Electrostatic discharge (ESD) protection of over 2001 V
- Full military capability
- Up to 348 pads (328 signal I/Os, 256 testable) with choice of:
  - Input, output, or bidirectional buffer
  - HCMOS or TTL input levels
  - Schmitt trigger inputs
  - Different output drive capability and slew rate
- High-density memory blocks:
  - High-speed static RAM up to 144K bits
  - Up to five ports available
  - Metal programmable ROM up to 512K bits
  - Diffusion programmable ROM up to 2M bits
  - Specialized memories including FIFOs, LIFOs and CAMs
  - Memory blocks compiled to any user-specified widths and depths
- Extensive macro libraries
  - Gate-level, SSI, MSI, LSI and VLSI building blocks
  - Over 200 macrocell and 300 macrofunction types available
  - Each macrocell available in a minimum of three versions varying in drive strengths
- All megafunctions available as, or can be converted into, megacells
- Built-in scan circuitry on all memories and megacells; choice of system level test structures for the balance of logic
- Full netlist compatibility with all other LSI Logic ASIC products
- Fully supported by LSI Logic's MDE Design Tools

LSI LOGIC

IEEE P1149.1/JTAG Testability Bus

IEEE P1149.1/JTAG Testability Bus
Preliminary

Overview

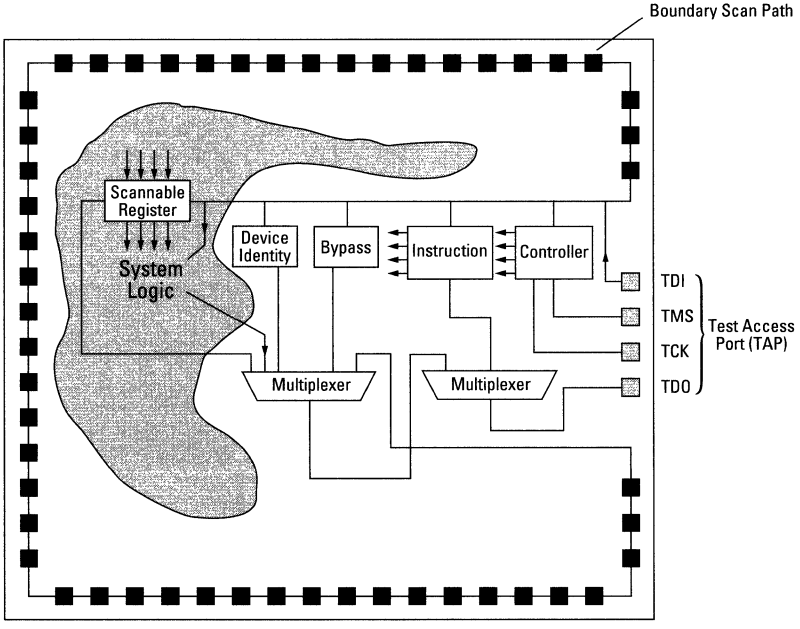
The IEEE P1149.1/JTAG Testability Bus is a proposed standard protocol for board test. LSI Logic supports this testability bus with special cells and design methodology. The IEEE P1149.1/JTAG Testability Bus is a boundary scan scheme controlled by four (optionally five) pins. In addition to boundary scan, a designer can add internal scan path, LSSD, BIST or CrossCheck test capability or other special test modes. LSI Logic supports P1149.1/JTAG in a variety of cell-based and array-based technologies.

The JTAG testability bus offers improved board level testing and diagnostic capabilities for systems where "bed-of-nails" testing is impractical. Board test vectors may be introduced and resulting outputs read out from the board edge connector. Individual IC's, boards, or an entire system may be tested in this fashion.

The JTAG testability bus in and of itself does not improve IC testability per se, but it does provide a standardized gateway for IC structured test schemes such as scan, LSSD, BIST or CrossCheck.

The Joint Test Action Group (JTAG) is an international group of companies who are seeking test solutions for boards and hybrid assemblies. They have involved the IEEE in the effort to develop an industry standard boundary scan test methodology. The result has been a proposed standard known as IEEE P1149.1. While the specification will not be final until voted on by the committee, LSI Logic offers JTAG capability now, based on the preliminary specification "Standard Test Access Port and Boundary-Scan Architecture", Test Technical Committee of the IEEE, June 1989. Any specification changes will be incorporated in future revisions.

Block Diagram



Block Diagram

LSI LOGIC

DSP Standard Products

L64032
32 x 32-Bit Multiplier-Accumulator

Description

The L64032 is a high-speed 32 x 32-bit parallel multiplier-accumulator which provides single precision (32 x 32) and multiple precision (64 x 64) fixed point multiplication and single precision multiplication with accumulation. The device is fabricated with a 1.5-micron drawn gate length (0.9-micron effective channel length) HCMOS process. High speed is obtained through the use of modified Booth encoding, Wallace tree adders and a high-speed carry select adder.

The L64032 is useful in DSP (Digital Signal Processing) applications such as Fourier transforms, digital filtering, power series expansions and correlations. In these applications, the 32-bit word length yields a signal to noise ratio and dynamic range of up to 192 dB. This device is also useful for general computational tasks such as matrix manipulations, graphics processing and arithmetic acceleration.

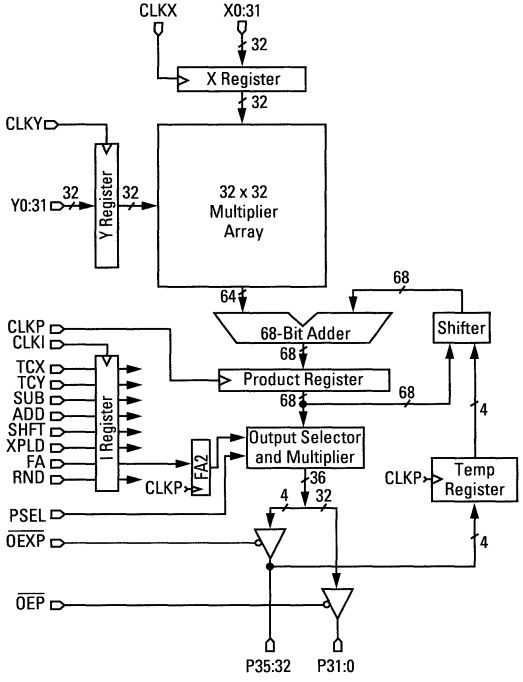
Features

- 32 x 32-bit parallel multiplication and product accumulation
- 64 x 64-bit fixed-point multiplication
- Fast cycle times

Commercial	Military
125 ns	160 ns
100 ns	125 ns
80 ns	100 ns

- Low power consumption–900 mW at 10 MHz
- Supports unsigned integer, two's complement integer, unsigned fractional and two's complement fractional input formats
- Supports unsigned integer, two's complement integer, unsigned fractional, two's complement fractional (shifted) and two's complement fractional (unshifted) output formats
- Positive and negative product accumulation
- TEMP register supports product register preloading
- Full rounding capability
- All registers offer full built-in scan testing capability
- 132-pin CPGA or PPGA (ceramic or plastic pin-grid array) package

Block Diagram



L64134
32-Bit HCMOS IEEE Floating-Point Processor

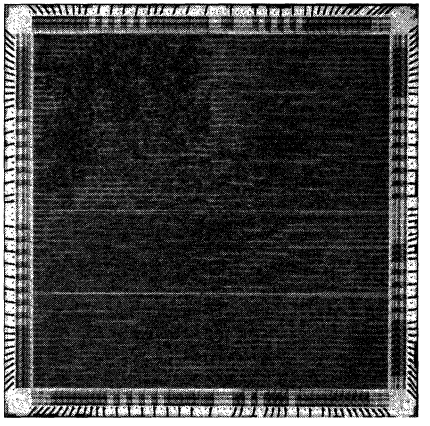
LSI LOGIC

Description

The L64134 is a high-speed processor which contains a full 32-bit floating-point multiplier and a full 32-bit floating-point ALU on a single chip. This three-bus device has a clean architecture with no internal pipelines. It is ideally suited for high-speed graphics and DSP (Digital Signal Processing) applications.

The L64134 supports the ANSI/IEEE Standard P754-1985 (commonly called IEEE) format. The device has been implemented in a 1.0-micron drawn gate length (0.7-micron effective channel length) HCMOS process for high-speed with low power dissipation and is packaged in an industry standard 144-pin ceramic pin grid array.

L64134 is functionally equivalent and pin compatible with the L64133. The L64134 has minor variations from the L64133 in terms of performance, flag generation and exception handling. In all cases, the L64134 behaves in a manner which is more consistent with the accepted interpretation of the IEEE standard.



L64134 Chip

Features

- Provides separate 32-bit floating-point multiplier and floating-point ALU on a single chip
- Fully supports all boundary conditions of the IEEE format except operations with denormalized numbers, which are treated as zero
- Three-bus architecture for high bandwidth
- Six ported internal core for super-scalor performance
- Separate register enable signals
- Fast floating-point operation times

Commercial	Military
50 ns	60 ns
60 ns	80 ns
80 ns	100 ns

- No internal pipelines for low latency
- Architecture optimized for sum of products and product of sums calculations
- All input registers can be selected as edge-triggered flip-flops or level-triggered latches
- All output registers can be selected as edge-triggered flip-flops or transparent buffers
- Single master clock
- Four separate input registers
- Provides conversion from integer to floating-point and from floating-point to integer formats
- Performs (2 minus X) for Newton-Raphson division
- Special graphics operation such as Min and Max
- Full serial scan test mode for all input and output registers eases board and system level testing

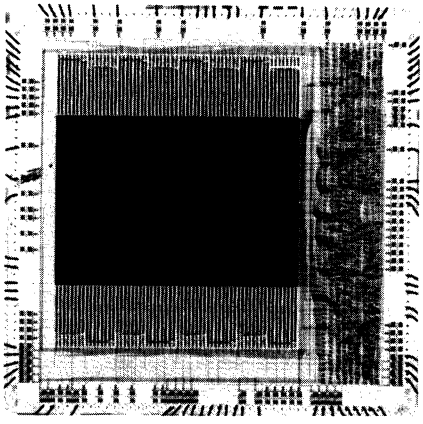
L64210/L64211 Variable-Length Video Shift Registers

Description

The L64210 and L64211 are two high-speed Variable-Length Video Shift Registers. These devices can be used individually or as video line delays for the L64200 series filter processors.

The L64210 provides four individual 8-bit shift registers, each with a length of up to 1032, and is packaged in a 68-pin plastic leaded chip carrier or ceramic pin grid array.

The L64211 provides eight individual 8-bit shift registers, each with a length adjustable to 516 and is packaged in a 120-pin plastic or ceramic pin grid array.



L64210/L64211 Chip

Features

- Variable-length video shift register
- Acts as a variable-length line delay, reformatting serial (raster-scanned video) data into a 2-D video signal for image processing
- Can work individually or with any of the LSI Logic L64200 series filter processors
- L64210 contains four separate 8-bit shift registers whose length can be varied from 24 to 1032
- L64211 contains eight separate 8-bit shift registers whose length can be varied from 12 to 516
- High data rates

Commercial	Military
20 MHz	16 MHz
15 MHz	12 MHz

- Control available to blank (force to zero) data outputs during horizontal video blanking intervals
- Control available to blank (force to zero) data inputs, which could be used to ignore invalid data during vertical video blanking intervals
- Input data can be sent to all eight internal shift registers simultaneously
- L64210 is available in a 68-pin PLCC (plastic leaded chip carrier) or CPGA (ceramic pin grid array) package
- L64211 is available in a 120-pin PPGA (plastic pin grid array) or CPGA (ceramic pin grid array) package

Architecture

The L64211 contains eight individual 8-bit variable-length shift registers which can be used as video line delays. The L64210 has every other shift register output connected to external package pins and effectively has four individual 8-bit shift registers. The length of the shift registers is controlled by the value residing in the level-triggered LENGTH latch register controlled by an active LOW $\overline{WE}$ input. The length of each of the eight shift registers of the L64211 can be varied from 12 to 516 bits by loading the LENGTH register according to:

Number of Shifts = (4 • LENGTH) + 8.

where 0 is an illegal input. Since the L64210 internally cascades two shift registers together, each of the resulting four registers can be varied from 24 to 1032 bits long, and its length is determined by the equation:

Number of Shifts = (8 • LENGTH) + 16.

In a video or image processing system, the length of each shift register is normally set to the number of pixels per video line. When used in this fashion (as a video line delay or as a front end to any of the LSI Logic real-time image-processing chips), the line delay ouputs the pixels vertically adjacent to (in the same column as) the input pixel.

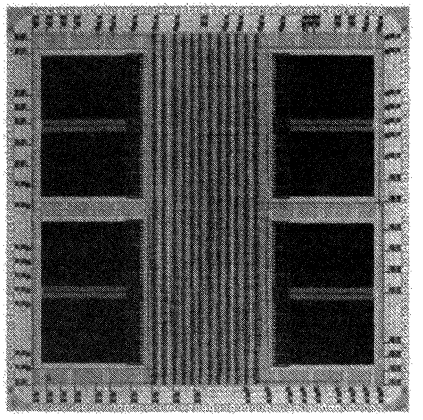
L64212 Variable-Length Video Shift Register (HVSR)

LSI LOGIC

Description

The L64212 is a high-speed Variable-Length Video Shift Register. This device can be used individually or as video line delays for the L64200 family of processors. The delay of the L64212 can be set to any value between 11 and 4140. The L64212 features fully static operation and 40 MHz data rates. The L64212 can be operated in a circular buffer mode, in which the buffer is filled once and then read continuously.

The L64212 has four delay elements each with a maximum delay of 1035. Two data inputs allow operation in 18-bit applications with delays up to 2070 or as two independent 9-bit line delays. The L64212 is packaged in a 95-pin grid array.



L64212 Chip

Features

- Variable-length video shift register
- Acts as a variable-length line delay, reformatting serial (raster-scanned video) data into a 2-D video signal for image processing
- Contains four separate 9-bit shift registers whose length can be varied from 11 to 1035
- Programmable for any delay value between 11 and 4140
- High data rates

Commercial	Military
40 MHz	40 MHz
30 MHz	30 MHz

- Variable-length circular buffer
- 3-State outputs for double-buffered memories
- Available in 95-pin CPGA (ceramic pin grid array) package

Pin Listing and Description

DI0
Nine-bit input data bus. Data inputs are loaded into the first stage of the first shift register at the rising edge of CLK while SHIFT/HOLD is HIGH.

DI1
Nine-bit input data bus. Data inputs are loaded into the first stage of the third shift register at the rising edge of CLK while SHIFT/HOLD is HIGH. Only active when internal control signal 2inp is HIGH.

CLK
System clock (when SELCLK is LOW), active at the rising edge.

WCLK
System clock (when SELCLK is HIGH), active at the rising edge. Used to load circular buffer.

SELCLK
Selects either CLK (when LOW) or WCLK (when HIGH) as system clock.

SRWE
Enables writing of data into the shift registers. Held HIGH for line delay applications and during loading in circular buffer applications. Held LOW during reading in circular buffer applications.

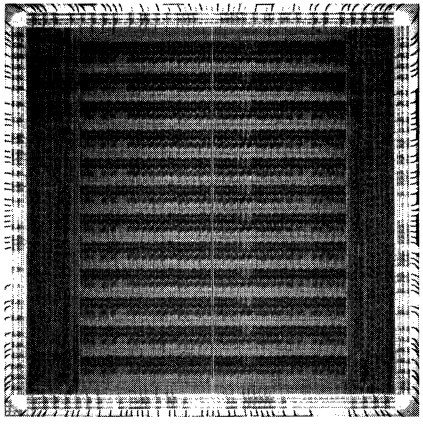
CI.0 to CI.7
Control input bus. This bus is common to all L64200 series devices. On the L64212, the bus is used to load the length of each of the delay elements and other control information.

L64220 Rank-Value Filter (RVF)

Description

The L64220 computes a given rank of the input values in a moving window and outputs the rank value. The operation is similar to a linear transversal filter except that the output is chosen from a sorted list of the input values rather than a weighted sum of the input values. Some examples of useful rank values include the maximum, minimum and median. Median filtering has been shown to be effective in removing noise that has a probability density with long tails (i.e., spikey noise), while preserving monotonic changes in the input data. The maximum and minimum can also be used to suppress certain types of noise in a non-linear manner.

The Rank-Value Filter can be reconfigured for operation as an 8 x 8, 4 x 16, 2 x 32 filter or as a 1 x 64 1-D filter. Values can be masked from the computation, giving the user very general control over the window of the filter. Thus, the size and shape of the window can be varied for many applications.



L64220 Chip

Features

- 64-tap, 12-bit reconfigurable Rank-Value Filter processor (RVF)
- Sorts and selects output data value based upon input rank (000000 = min, 111111 = max)
- Configurable for 8 x 8, 4 x 16, 2 x 32 or 64-tap window size
- Operates on signed or unsigned data
- Eight separate 12-bit input buses
- Configurable window shape and size
- Double-buffered coefficient/control registers
- High-speed real-time operation

Commercial	Military
20 MHz	16 MHz
15 MHz	12 MHz

- Extremely useful as a median filter to remove impulse-like (salt and pepper) noise
- Fully compatible with other LSI Logic L64200 series devices

Architecture

The L64220 Rank-Value Filter (RVF) sorts all the values within a window and outputs the value of interest as determined by the RANK selector. Commonly used rank values are the maximum or minimum value within a set of inputs. The most common application of the device will be as a median filter which has excellent properties for removal of impulse-like noise. The device is a stand-alone filter which can operate on either 1-D or 2-D windows where each data point is up to 12 bits in length. The L64220 is easily reconfigurable to perform RVF operations with a variety of window sizes and shapes.

The Rank-Value Filter operates at very high speeds and is useful in high-end applications such as radar signal processing, image processing, high-speed data communications and other areas where performance and processing power are important.

The device contains eight individual 8-tap shift registers (RVF0–RVF7), each 12 bits wide. By controlling the input source to each 8-tap shift-register section, the Rank-Value Filter can be configured as a 64-tap 1-D Rank-Value Filter or as a 2-D filter with a 2 x 32, 4 x 16 or 8 x 8 window.

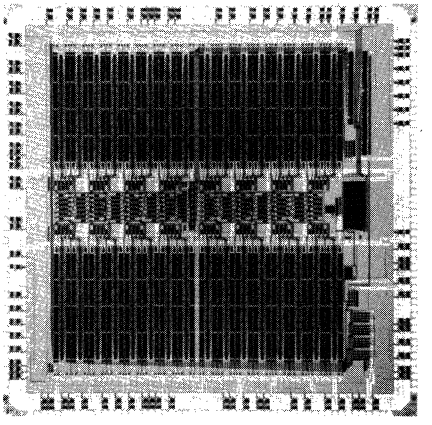
LSI LOGIC

L64230 Binary Filter and Template Matcher (BFIR)

Description

The L64230 is a 1024-tap high-speed binary transversal filter processor and template matcher. The processor can be configured as a 1-D (one-dimensional) filter for radar or other signal processing applications, or as a 2-D (two-dimensional) filter for image processing applications. The processor accepts 2-D data directly from a L64210/L64211 Variable-Length Video Shift Register or other video source. The coefficients can be changed in time to perform adaptive filtering and correlation. The window and/or precision of a 1-D or 2-D filter is expandable using more L64230 processors with minimal external logic.

The processor is ideally suited for real-time image processing applications, like video pattern matching, noise removal and the morphological operations, erosion and dilation. The maximum window size is 32 x 32 for a single chip. Video output formatting circuitry is also available on chip to clip the ouput to a single bit. Data throughput of 20 MHz (WCCOM) makes the processor suitable for radar processing. Implemented in 1.5-micron drawn gate length (0.9-micron effective channel length) low power HCMOS technology, the L64230 is available in a 155-lead ceramic pin grid array package.



L64230 Chip

Features

- Performs FIR filtering, template matching, erosion and dilation
- Compatible with the L64200 family of products
- 1024-tap sections, each operating on 1-bit data and 1 1/2-bit coefficients
- Reconfigurable for 1-D and 2-D correlation/convolution/morphology
- Multiple processors can be used to extend data and/or coefficient precision
- Multiple processors can achieve window sizes of over 64K taps
- 16-bit output precision
- Double buffering of coefficients
- High speed operation

Commercial	Military
20 MHz	16 MHz
15 MHz	12 MHz

- Available in 155-lead CPGA (ceramic pin grid array) package

Architecture

The core of the processor is organized as 32 32-tap filter sections. The outputs of all 32-tap sections are summed and delayed by the variable-length shift register. This delayed output is added to an incoming partial result to form the processor output. The partial result input is used to sum partial results in a multi-processor system and to set the threshold value to clip the output to a single bit. The variable-length shift register is used only in multiprocessor systems to compensate for additional latency acquired in the partial result path.

Each filter tap performs the basic XNOR and AND operations. The Ai, j and Bi, j are stored in double buffered registers. Bi, j controls the XNOR gate ane Ai, j controls the AND gate. The XNOR gate performs inversion (erosion) or magnitude differencing (template matching). The AND gate performs masking (template matching) or 1-bit multiplication (FIR filtering, dilation, erosion). The outputs of all taps are summed to produce the final result. It should be noted that no significant bits of any signal are lost.

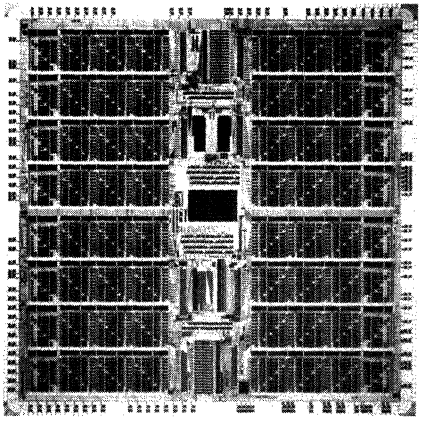
The processor has 32 single-bit inputs (DI0-DI31). For 1-D filtering, the only active input is DI0. When performing 2-D operations over N × M window, N of the inputs are active. Normally, when performing 2-D operations, an L64210/211 Video Shift Register with a raster-scanned signal as its input would provide the N active data inputs. In this case, the output of the processor, DO(n) represents the raster-scanned output.

L64240
Multi-Bit Filter
(MFIR)

Description

The L64240 is a 64-tap high-speed transversal filter processor consisting of two 32-tap sections, with 8-bit wide coefficients and data. The processor can be configured as a 1-D (one-dimensional) filter for radar or other signal processing applications, or as a 2-D (two-dimensional) filter for image processing applications. The processor accepts 2-D data directly from a L64210/L64211 Variable-Length Video Shift Register or other video source. The coefficients can be changed to perform adaptive filtering and correlation. The window and/or precision of a 1-D or 2-D filter is expandable using more L64240 processors with minimal external logic.

The processor is ideally suited for real-time image processing applications such as video pattern matching, noise removal, inverse filtering, edge enhancement, and edge detection. The maximum window size is 8 x 8 for a single chip. Video output formatting circuitry is also available on-chip to alter gain, threshold and other parameters. Worst-case commercial grade data throughput of 20 MHz make the processor suitable for radar processing. Implemented in 1.5-micron drawn gate length (0.9-micron effective channel length) low power HCMOS technology, the L64240 is available in 155-lead ceramic pin grid array package.



L64240 Chip

Features

- Two 32-tap sections, each 8-bit data and coefficients
- One 32-tap section, each 16-bit data or coefficients
- Reconfigurable for 1-D and 2-D correlation/ convolution
- Multiple processors can be used to extend data and/or coefficient precision up to 24 bits
- Multiple processors can achieve window sizes of over 1024 taps
- Two's complement or unsigned 8-bit input data and coefficient
- Output precision up to 40 bits for 1-D processing, up to 24 bits for 2-D processing
- Double buffering of coefficients
- Format adjustment for video display
- On-chip barrel shifter for precision expansion
- Block floating-point format output
- Configurable as an IIR filter
- High speed operation

Commercial	Military
20 MHz	16 MHz
15 MHz	12 MHz

- Ability to perform Sobel edge extraction
- Available in 155-lead CPGA (ceramic pin grid array) package

Architecture

The L64240 Multi-Bit Filter is a stand-alone Finite Impulse Response (FIR) filter which can operate on either 1-D or 2-D data. It is easily reconfigurable to perform FIR filter operations with a variety of window sizes and shapes.

It operates at very high speeds and is useful in high-end applications such as radar signal processing, image processing, high speed data communications and other areas where performance and processing power are important.

The L64240 performs convolution/correlation operations of the type:

$$1\text{-}D: y(n) = \sum_{l=0}^{L-1} h_l\, x(n-l)$$

$$2\text{-}D: y(n,m) = \sum_{l=0}^{L-1} \sum_{k=0}^{K-1} h_{l,k}\, x(n-l, m-k).$$

The device contains eight individual 8th order FIR filters (FIR0–FIR7).

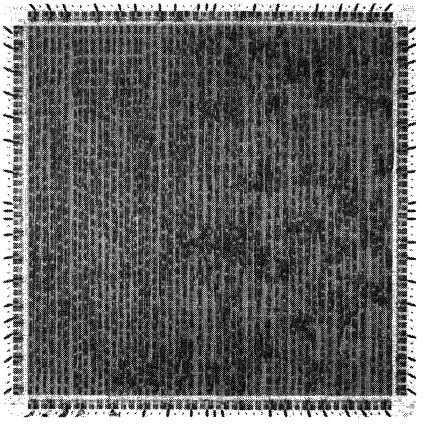
LSI LOGIC

L64243
3 x 3 Multi-Bit Filter (MFIR3)

Description

The L64243 is a 9-tap high speed transversal filter processor consisting of a 9-tap section, with 8-bit wide coefficients and data. The processor can be configured as a 1-D (one-dimensional) filter for radar or other signal processing applications, or as a 2-D (two-dimensional) filter for image processing applications. The processor accepts 2-D data directly from a L64210/L64211 Variable-Length Video Shift Register or other video source. The coefficients can be changed to perform adaptive filtering and correlation.

The processor is ideally suited for real-time image processing applications such as video pattern matching, noise removal, inverse filtering, edge enhancement and edge detection. The maximum window size is 3 x 3 for a chip. Data throughput of 40 MHz makes the processor suitable for radar processing. The L64243 is implemented in a 1.5-micron drawn gate length (0.9-micron effective channel length) low power HCMOS technology.



L64243 Chip

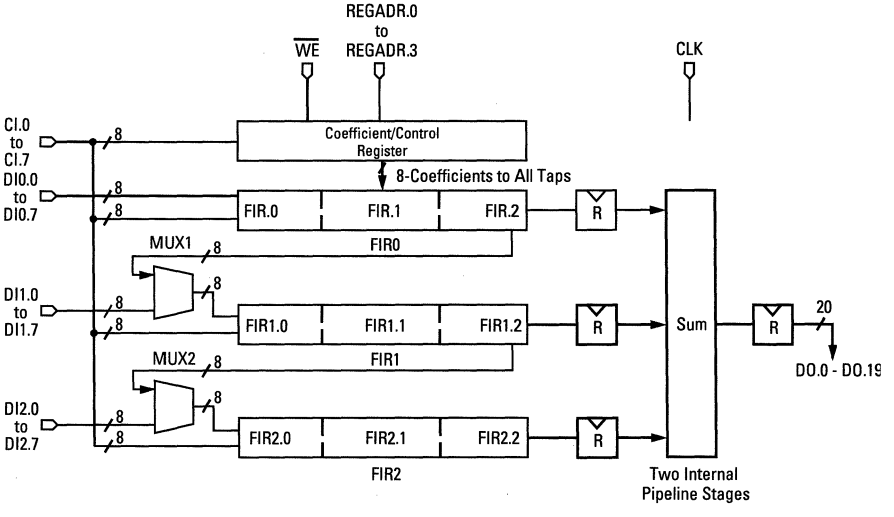
Features

- 9-taps, 8-bit data and coefficients
- Reconfigurable for 1-D and 2-D correlation/convolution
- Two's complement or unsigned 8-bit input data and coefficient
- Output precision up to 20 bits
- Double buffering of coefficients
- High speed operation

	Commercial	Military
L64243-40	40 MHz	40 MHz
L64243-30	30 MHz	30 MHz
L64243-20	20 MHz	20 MHz

- Available in 68-pin CPGA (ceramic pin grid array) or 68-pin PLCC (plastic leaded chip carrier) package

Block Diagram



LSI LOGIC

L64245
FIR Filter Processor
Preliminary

Description

The L64245 is a device for computing FIR Filters on continuous data streams at data rates up to 40 MHz. 1-D (one-dimensional) filters with a range of data sample rates and filter lengths can be implemented.

Input and coefficient data are both 10-bit signed or unsigned values. Both real and complex (I&Q) data types are supported.

The L64245 is capable of implementing a range of filter functions. Decimating filters, interpolators, interleaved and complex filters are all supported. The length of the filter in all cases is determined by the input or output data rate. As this data rate drops below the device's clock rate, the number of taps available increases.

The L64245 consists of 26 processing elements. Each element is a 40 MHz multiplier combined with eight coefficient registers and an eight tap shift register. This makes it possible to implement real filters ranging from 208-taps at 5 MHz to 26-taps at 40 MHz. Coefficients not being used by a multiplier can be updated without effecting the operation of the filter.

Features

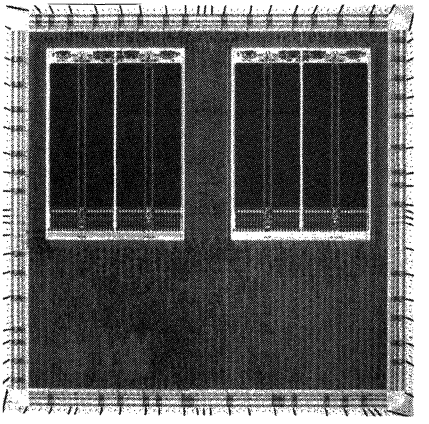
- 26 10*10 multiplier accumulators
- 208 coefficient registers
- Real and complex filters
- Interpolation and decimation
- Up to eight independent interleaved data stream
- Clock/Data Rates
  - L64245-30 30 MHz
  - L64245-40 40 MHz
- 68-pin CPGA (ceramic pin grid array) or PPGA (plastic pin grid array) package

L64250 Histogram/Hough Transform Processor (HHP)

LSI LOGIC

Description

The L64250 computes histograms and modified Hough transforms for data sets up to 2^{24} points or images up to 4096 x 4096 pixels. In addition, pixel location operations may be performed in which the X and Y coordinates of pixels of designated grey values are stored. Data rates up to 20 MHz and data precisions up to nine bits are accommodated.



L64250 Chip

Features

- Histogram and Hough transform calculation performed on images up to 4096 x 4096 pixels
- Four 512 x 9 look-up tables provided to perform user-defined point-wise transformations
- Real-time histogram equalization
- High data rates

Commercial	Military
20 MHz	16 MHz
15 MHz	12 MHz

- Two system clocks provided for different pixel and host controller data rates
- Marker circuit allows users to flag points of interest on the histogram, modified Hough transform or accumulated histogram
- Available in a 68-pin CPGA (ceramic pin grid array) or 68-pin PLCC (plastic leaded chip carrier) package

Architecture

The architecture of the L64250 accommodates the implementation of multiple algorithms with the same memory-based circuitry. The particular operation that is to be performed is defined via a group of mode latches.

The accumulation memory (ACC RAM) holds the histogram, modified Hough transform partial results or the X and Y pixel coordinates. Four 512 x 9 LUT RAMs hold any combination of the histogram-equalized transfer function, user-specified transfer functions, the function needed to perform the modified Hough transform ($X\tan\phi$ or $Y\cot\phi$) or a table indicating which pixel locations should be stored.

The X and Y counters are used when performing modified Hough transforms and pixel location and contain the X and Y coordinates within the image. The LUT, adder and counters compute the Hough transform parameter for each point in the image. The user controls the X and Y counters via the count (CX, CY) and reset (RX, RY) pins.

The I/O controller is used to generate addresses for the RAMs when reading results from the processor or loading the LUTs. The processor output comes from either the ACC RAM, the LUT RAM or the marker memory depending on the type of operation being performed.

Two clocks control the flow of data in the system. CLK1 is the pixel or input data clock. CLK2 is provided to allow the user to read data from or write data into the RAMs at a lower rate than the data input rate. CLK2 can be tied to CLK1 when all operations are performed at the data input rate (e.g. histogram equalization).

L64260/L64261 High-Speed Versatile FIR Filter (VFIR)

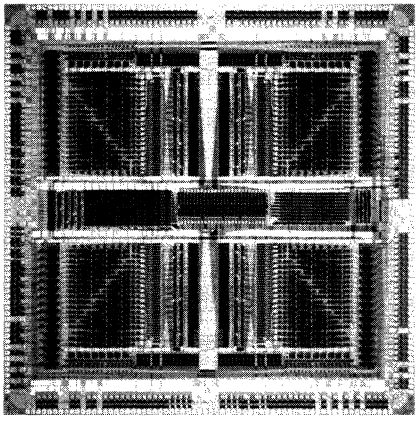
LSI LOGIC

Description

The L64260/61 compute inner products in many different forms. FIR filters to perform decimation, interpolation, adaptive filtering and 2-D (two-dimensional) filtering can be implemented. In addition, matrix-matrix and matrix-vector multiplication can both be performed. Each processor contains four high-speed MACs each with four data and four coeffcient registers. An on-chip sequencer is used to control the chip when repetitive operations are performed.

There are two versions of the processor. The L64260 comes in a 223-pin ceramic pin grid array with eight 16-bit data inputs bonded out.

The L64261 comes in a 144-pin ceramic pin grid array that does not provide the use of all I/O pins. The L64261 has two 16-bit data inputs, three 12-bit data inputs and three 12-bit data inputs that are shared with the buses needed to cascade parts. In applications not requiring both the additional data input buses and the ability to cascade parts, the L64261 can be used. The L64260 is useful in applications in which either very high I/O bandwidth is required (e.g., general inner products) or the extra data precision is needed. The L64261 is aimed primarily at filtering and matrix multiplication applications. In these applications, not all of the data input buses are necessary.



L64260/L64261 Chip

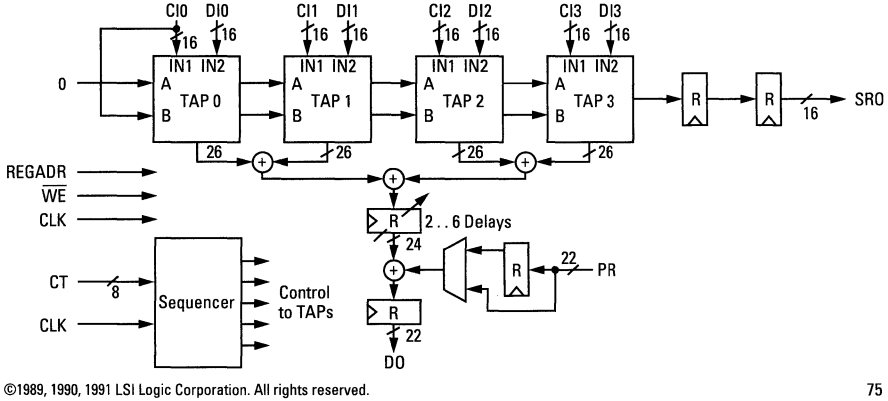
Features

- Four 16-bit MACs
- On-chip control functions reduce system size
- Multiple chips can be used to increase performance
- Flexible architecture with 16 coefficient and data registers
- High I/O bandwidth for:
  - Adaptive filtering
  - Matrix-matrix or matrix-vector multiplication
  - General inner products
- Variable input and output data rates for decimation and interpolation
- Can perform one-chip 4 x 4 convolution
- High data rates

Commercial	Military
40 MHz	30 MHz
30 MHz	25 MHz

- L64260 is available in a 223-pin CPGA (ceramic pin grid array) package
- L64261 is available in a 144-pin CPGA (ceramic pin grid array) package

L64260 Block Diagram



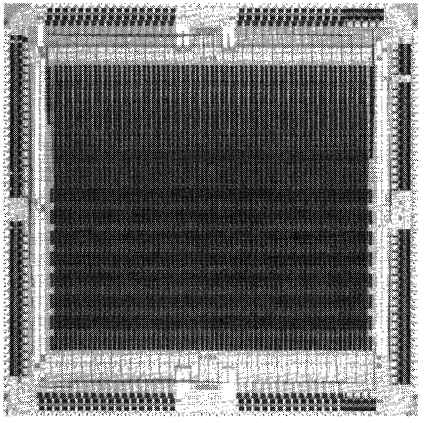
L64270
64 to 64
Crossbar Switch
(XBAR)

LSI LOGIC

Description

The L64270 is a 64 to 64 Crossbar Switch in which any of the 64 outputs can be connected to any of the 64 inputs without any blocking constraints. In addition, any output can be set to a constant value or put in a high impedance state. Each of the 64 switches can be operated in a flow through mode with a delay of 25 ns from input to output or in a pipelined mode with a delay of 15 ns from clock to output.

The device can be put into a bus and/or a bidirectional mode to simplify operation with multi-bit uni-directional or bidirectional buses. The L64270 is implemented in a 1.5-micron drawn gate length (0.9-micron effective channel length) low power HCMOS technology.



L64270 Chip

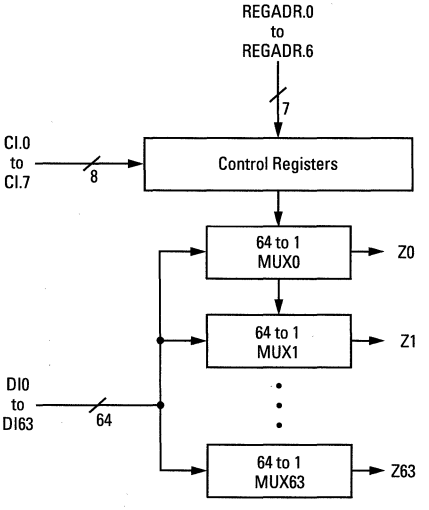
Features

- Non-blocking 64 to 64 crossbar switch
- Pipelined or flow through modes
- Multiple chips can be used to increase switch size
- Outputs can be set to constant values
- Can easily switch buses of different widths
- Can be be configured as 64 bidirectional ports
- Double buffered control signals
- Can perform arithmetic or logical shifting and bit rotation
- High data rates

	Pipelined Mode	Flow Through Mode
L64270JC-40	40 MHz	25 ns
L64270JC-30	30 MHz	35 ns

- 160-pin PQFP (plastic quad flat pack) package

Block Diagram



L64280
Complex FFT Processor (FFTP)
Preliminary

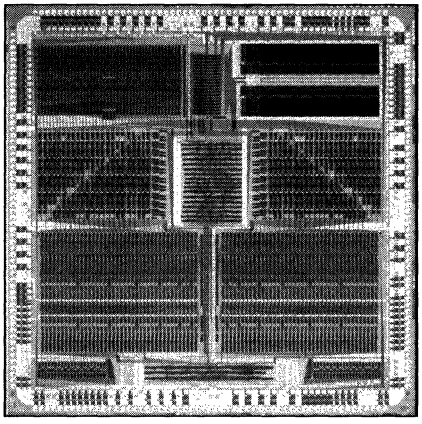
Description

The L64280 FFTP (Fast Fourier Transform Processor) is a floating-point complex FFT processor and is designed for primary use with the L64281 FFTSR (Fast Fourier Transform Video Shift Register) in real-time FFT systems. It can also be used in a single processor configuration in which system cost is reduced along with system performance. The FFTP includes the FFT controller and complex exponential ROM needed to compute transforms of 2048 points or less. For longer transforms, external controllers and coefficient storage devices are required.

The device performs both the forward and inverse transforms and can accept data in either normal order or bit-reversed order.

A variety of operating modes and data formats can be chosen. The input data can be either a floating-point or fixed-point number. Likewise, the output data can be either a floating-point or fixed-point number. For fixed-point outputs, a user supplied scale factor determines which internal bits are output.

In addition to performing FFTs, the device can be operated as a complex MAC, two real MACs or as a MAC with one complex and one real operand. The user can either input a complex or real coefficient or input the phase of a complex exponential or real sinusoid.



L64280 Chip

Features

- Computes FFT butterflies at 20 MHz rate
- Real or complex multiplication-accumulation
- Integer or floating-point data formats
- Internal FFT controller for up to 2K point FFT
- Internal complex exponential, real sinusoid ROM for up to 2K point FFT
- Forty-bit internal accumulation for high precision
- Applications in modulation and demodulation
- Internal controller for single processor systems
- High data rates

Commercial	Military
40 MHz	30 MHz
30 MHz	25 MHz

- Available in a 144-pin CPGA (ceramic pin grid array) package

Pin Listing and Description
(the highest numbered bit is always the most significant)

EDI.0:3
Four-bit input exponent set to constant for fixed-point data input.

RDI.0:19
Twenty-bit real data mantissa input.

IDI.0:19
Twenty-bit imaginary data mantissa input.

EDO.0:3/OVF.0:3
Four-bit output exponent and overflow flags. In floating-point output mode, the output data exponent appears on these pins. In fixed-point output mode, OVF.0 HIGH indicates overflow of the data on RDO, and OVF.1 is the sign of the data on RDO; OVF.2 HIGH indicates overflow of the data on IDO, and OVF.3 is the sign of the data on IDO.

RDO.0:19
Twenty-bit real data mantissa output.

IDO.0:19
Twenty-bit imaginary data mantissa output.

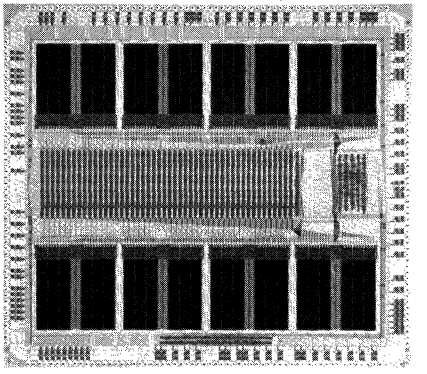
L64281 FFT Video Shift Register(FFTSR)
Preliminary

Description

The L64281 is a high-speed FFT (Fast Fourier Transform) video shift register. It is used to perform data formatting in real-time FFT systems using the L64280 FFTP (Fast Fourier Transform Processor), or as a flexible variable-length video line delay. The FFTSR (Fast Fourier Transform Video Shift Register) features fully static operation and 40 MHz data rates.

When used in an FFT system, the FFTP devices generate all control signals for the FFTSRs, simplifying the system design. A single FFTSR can perform the data formatting required at each stage of the FFT if the length is limited to 2K points and the data word widths are limited to 47 bits. Multiple FFTSRs can be cascaded (and/or paralleled) when longer transform lengths or wider data words are required.

The user has access to all 48 single-bit delay element inputs and outputs, which makes very flexible video line delays and data buffering possible. The device can be operated in 1, 2, 4, 8, 12, 16 and 48-bit modes. The input and output of the device can be independently operated in serial or parallel modes. For example, the input can be serial and the output parallel (video line delay), or the input can be parallel and the output serial. The delay of each internal shift register is 4N + 14, where $0 \leq N \leq 255$. Therefore, a 48-bit signal can be delayed up to 1034 cycles, and a single-bit signal can be delayed up to 49632 cycles.



L64281 Chip

Features

- High-speed FFT data formatting
- Flexible video line buffering
- Serial to parallel data conversion
- Parallel to serial data conversion
- Internally configurable for different data word widths
- Contains 48 independent 1-bit shift registers whose length can be varied from 14 to 1034
- All data outputs available
- High data rates

	Commercial	Military
L64281-40	40 MHz	40 MHz
L64281-30	30 MHz	30 MHz

- Available in a 132-pin CPGA (ceramic pin grid array) package

LSI LOGIC

L64290
Object Contour Tracer

Description

The Object Contour Tracer is used to locate the contours of objects in a binary (1-bit) image. It will return the sequence of X, Y coordinates and discrete curvature values for each contour. In addition, the bounding box, area and perimeter of each contour is returned.

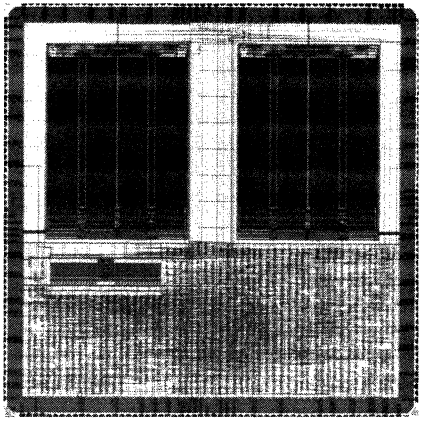
The device can store images internally with sizes up to 128 x 128 pixels. For images of up to 1024 x 1024 pixels, external RAM is used.

Searching for objects can be restricted to a subset of the image to decrease the object detection time. When using the internal RAM, the image is automatically run-length coded which allows the processor to skip runs of eight or more pixels when searching.

The tracer will find all contours including contours within other contours for all of the objects within the search window. The user can force the tracer to ignore those contours which touch an edge of the frame or which are in the interior of an object.

The contour tracer can be used in object/target tracking and identification applications.

The discrete curvature, when normalized, provides insensitivity of the identification process with respect to translation, rotation and scaling of the object. The device can also be used to compress black and white images by coding and transmitting only the contour information.



L64290 Chip

Features

- Finds all object contours
- Internal RAM for 128 x 128 pixel images
- Handles 1K x 1K pixel images with external RAM
- Automatic run-length coding decreases search time
- 20 MHz clock rate
- User selectable search window
- Outputs object contour features
  {X(n), Y(n)}, {CURV(n)}, {SLOPE(n)}
  bounding box, area, perimeter
- Execution Time (image dependent) for N x M image:
  typical: < NM cycles
  worst case (checker board pattern): (4.5)NM cycles
- 68-pin CPGA (ceramic pin grid array) package

Pin Listing and Description

(SIGNAL.0 is always the LSB)

XIO.0-XIO.9
Ten-bit bus for loading operating and searching parameters into the device. Also used to read contour features and the external RAM X coordinate. Data is latched internally when CS is HIGH and RW is LOW. Data is output on this bus when CS and RW are HIGH. The XIO bus floats when CS is LOW.

YIO.0-YIO.9
Similar to the XIO bus, but carries the RAM Y coordinate.

REGADR.0-REGADR.4
Five-bit register address. Selects one of the internal data registers to be output on the XIO and YIO buses when CS and RW are HIGH. If CS is HIGH and RW is LOW, the register with an address of REGADR will be loaded with the data on the XIO and YIO buses.

CS
Chip Select. When HIGH data can be read from or written to the internal data registers. When LOW, the XIO and YIO buses float.

LSI LOGIC

Video and Still Image Compression

LSI LOGIC

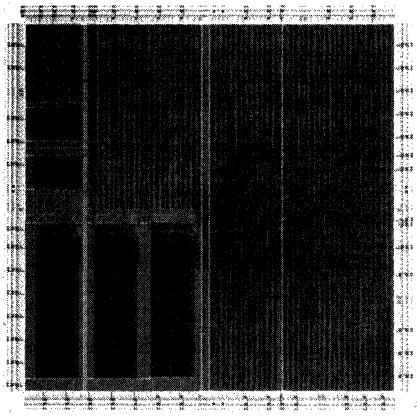
L64710
8-Error Correcting Reed-Solomon Codec

Description

The L64710 contains a RS (Reed-Solomon) encoder and a RS decoder. This pipelined, high-speed, error-correction device implements an RS code with 8 bits (1 byte) per symbol. The encoder appends 16 redundant check bytes to every K message bytes. The message length K is user-programmable between 38 and 239. Each RS codeword consists of N = K + 16 bytes of data. Thus the codeword length N may range between 54 and 255 bytes.

The decoder is capable of correcting up to 8-byte errors per codeword. Sustained throughput data rates up to 40 Mbytes per second (commercial) are supported for both the encoder and decoder

The L64710 is ideally suited for ensuring data integrity in high-performance storage media and communication channels. The device is implemented in a 1.0-micron drawn gate length (0.7-micron effective channel length) HCMOS technology.



L64710 Chip

Features

- Eight bits (1 byte) per code symbol
- Sixteen bytes of redundancy per codeword
- Percentage redundancy as low as 6.79%
- Corrects up to 8 byte errors per codeword
- Corrects single burst up to 57 bits long
- Systematic Reed-Solomon code for easy retrieval of message data
- User-selectable codeword length of between 54 and 255 bytes
- Separate encoder and decoder for full duplex operation
- Pipelined architecture with high data rate

Commercial	Military
40 MHz	40 MHz
30 MHz	30 MHz

- Fully static design with no minimum speed requirement
- Built-in test modes
- Available in a 68-pin CPGA (ceramic pin grid array) package

L64715
Two-Error Correcting BCH Encoder-Decoder

Description

The L64715 implements the forward error correction, bit filling and synchronization scheme specified in CCITT (International Consultative Committee for Telephones and Telegraphs) recommendation H.261. The forward error correcting code is a 2-error correcting BCH code. The device contains both an encoder and a decoder for full duplex operation.

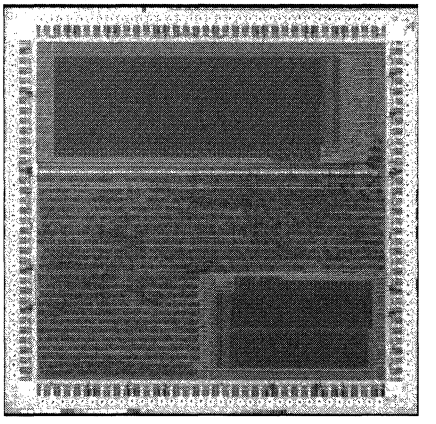
The device processes blocks of 512 bits. Each block consists of a 511-bit BCH codeword and a single internally generated or user supplied frame bit. The encoder appends 18 bits of redundant check bits to every 493 bits of message to form the BCH codeword. The message consists of either 493 bits of data or a fill indicator bit and 492 bits of data or a fill indicator and 492 fill bits.

The BCH decoder can correct up to two errors per codeword. The number of errors that have been corrected is reported for channel characterization.

When internal framing and synchronization is selected, the encoder appends a single framing bit, as specified in CCITT recommendation H.261, to each BCH codeword. The decoder will automatically detect the synchronization pattern to determine the codeword boundary. External synchronization can also be provided, in which the codeword boundary for the decoder is provided externally.

The device can be programmed to operate with or without bit filling. When the fill mode is selected, the first message bit is used to indicate if the rest of the message has been filled or contains data.

Sustained encoded bit rates of up to 30 or 40 Mbits per second are supported for both the encoder and decoder in full duplex mode.



L64715 Chip

Features

- Codeword size of 511 bits
- Corrects up to two bits of errors per codeword
- Separate encoder and decoder for full duplex operation
- Optional synchronization and bit filling
- Compatible with CCITT H.261 requirements
- 40/30 MHz data rate for decoder and encoder
- Internal BCH decoding buffers
- 44-pin PLCC (plastic leaded chip carrier) package

L64720 Video Motion Estimation Processor (MEP)

Description

The MEP (Motion Estimation Processor) detects the relative motion between data blocks in two video frames. This operation makes it possible to transmit or store less information in a video compression system.

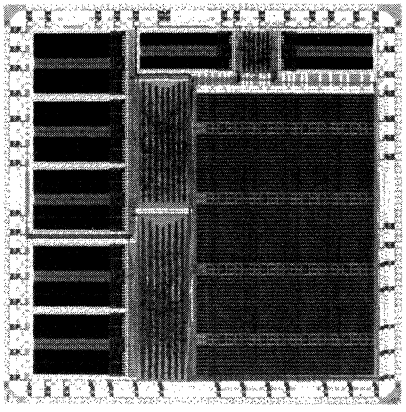
The data block (user selectable for either 16 x 16 or 8 x 8) in the current video frame is offset and compared with the reference image. The position of the best match, the minimum error and the zero offset error are returned by the processor. The error computed is the sum of absolute differences.

For the 16 x 16 data block size, errors are computed for offsets of -8 to +7 in both the X and Y dimensions. For the 8 x 8 data block size, errors are computed for offsets of -4 to +3 in both the X and Y dimensions. In both cases, multiple devices can be used to increase the search window size.

The L64720-30 can process a 352 x 288 image at a 30 MHz frame rate with a 16 x 16 data block size. When operating with an 8 x 8 data block size, the L64720-30 can process broadcast quality images (600 x 480) at a 30 MHz frame rate.

All input and output data is double buffered to minimize the main memory bandwidth requirements. The search window and data blocks are loaded sequentially while the output values are randomly accessed.

The device is available in 68-pin ceramic and plastic PGAs (pin grid arrays).



L64720 Chip

Features

- 16 x 16 or 8 x 8 data block
- 32 x 32 or 16 x 16 search window
- Search window can be increased with multiple devices
- Multiple devices can be used for increased performance
- Compatible with proposed CCITT standard
- 30/40 MHz clock rates
- Double buffered I/O
- Simple control
- 68-pin CPGA (ceramic pin grid array) or PPGA (plastic pin grid array) package

L64730 Discrete Cosine Transform Processor (DCT)
Preliminary

Description

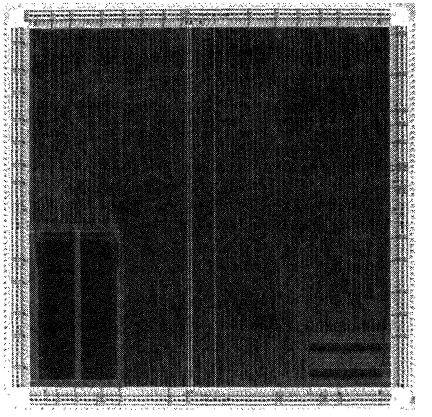
The DCT (Discrete Cosine Transform) Processor computes both the forward and inverse DCT over 8 x 8 data blocks and meets the CCITT (International Consultative Committee for Telephones and Telegraphs) standard. Up to 12-bits of data precision is available for the input and output data. The output can also be rounded to 9 or 12 bits. The device supports data rates up to 40 MHz.

All DCT coefficients and control signals are generated internally; the user only supplies a signal indicating the beginning of the data block, the direction of the transform and the number of bits desired at the output.

The device can also perform the loop filtering specified in the CCITT standard. This operation is performed at the same rate as the DCT and inverse DCT.

The Discrete Cosine Transform is ideal for image or video compression systems as the DCT coefficients can typically be coded with fewer bits of information than the original image. To ensure proper tracking between an encoder and decoder, the proposed CCITT standard has placed strict limits on the statistics of the errors encountered when computing the inverse DCT. This device complies fully with these requirements.

The device is available in 68-pin ceramic and plastic PGAs (pin grid arrays).



L64730 Chip

Features

- 8 x 8 data block
- Handle continuous data streams
- Up to 12-bit input and output precision
- Computes forward and inverse transforms
- Multiple devices can be used for increased performance
- Compatible with proposed CCITT standard
- Performs spacially variant loop filtering
- 30/40 MHz clock rates
- Simple external control
- 68-pin CPGA (ceramic pin grid array) or PPGA (plastic pin grid array) package

L64735
Discrete Cosine Transform Processor
Preliminary

Description

The DCT (Discrete Cosine Transform) Processor computes both the forward and inverse DCT over 8 x 8 data blocks and meets the proposed CCITT (International Consultative Committee for Telephones and Telegraphs) standard (H.261). The device operates with either signed or unsigned pixel data. Eight-bit unsigned pixel data is transformed into 11-bit signed DCT coefficients while 9-bit signed pixel data is transformed into 12-bit signed DCT coefficients. DCT coefficients are accepted and generated in either raster order or zig-zag order. The pixel data I/O is always in raster order. The device supports data rates up to 35 MHz.

The cosine basis functions and control signals are generated internally.

The user only supplies a signal indicating the beginning of the data block, the direction of the transform, the format of the pixel data and the ordering of the DCT coefficients. The Discrete Cosine Transform is ideal for image or video compression systems as the DCT coefficients can typically be coded with fewer bits of information than the original image. To ensure proper tracking between an encoder and decoder, the proposed CCITT standard has placed strict limits on the statistics of the errors encountered when computing the inverse DCT. This device complies fully with these requirements.

The device is available in 68-pin ceramic and plastic PGAs (pin grid arrays) and 100-pin PQFP's (plastic quad flat packs).

Features

- 8 x 8 data block
- Handles continuous data streams
- 9-bit signed or 8-bit unsigned pixel data
- Raster order pixel data
- Zig-zag or raster order DCT coefficients
- Compatible with proposed CCITT standard
- Bypass mode
- 20/27/35 MHz clock rates
- Simple external control
- 68-pin CPGA (ceramic pin grid array) or PPGA (plastic pin grid array) or 100-Pin PQFP (plastic quad flat pack) package

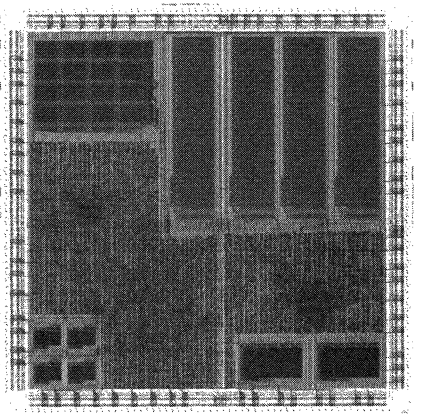
L64740 DCT Quantization Processor (DCTQ)

Description

The L64740 performs many of the functions required after the DCT (Discrete Cosine Transform) and before the IDCT (Inverse Discrete Cosine Transform) of the proposed CCITT (International Consultative Committee for Telephones and Telegraphs) RM8 and H.261 and JPEG (Joint Pictures Expert Group) R5 baseline image compression standards. The device will optionally perform the variable threshold function in CCITT mode and the quantization and the zig-zag run-length coding in both modes. In addition, the inverse run-length coding and inverse quantization can be performed.

The L64740 can accept DCT data directly from the L64730 (DCT processor) and generate data for the L64730. In addition, the device will accept DCT data in raster scanned or transposed formats.

When operating as a CCITT encoder, the DCTQ generates the run and level information to be coded and transmitted to the decoder and the quantized DCT coefficients which are processed by the inverse DCT processor. The DCTQ accepts the run and level information and reconstructs the DCT coefficients which are passed to the inverse DCT processor when operating in a CCITT decoder. Operation in JPEG systems is simpler. In the encoder, the device quantizes the incoming block of coefficients using two internally stored tables. After quantizaton, the coefficients are zig-zag run-length coded. In the decoder, the inverse of the two operations is performed.



L64740 Chip

Features

- 8 x 8 data block
- Handles continuous data streams
- Performs quantization and inverse quantization
- Two quantization tables for JPEG operation
- Zig-zag run-length coding and decoding
- Supports with proposed CCITT and JPEG standards
- 30/40 MHz clock rates
- Simple external control
- 84-pin CPGA (ceramic pin grid array) or PLCC (plastic leaded chip carrier) package

LSI LOGIC

L64745
JPEG Coder
Preliminary

Description

The L64745 is a variable-length encoder-decoder used to implement the quantization, zip-zag run-length coding and the variable-length coding and decoding of events as specified in the proposed baseline JPEG (Joint Pictures Expert Group) standard. The device includes four quantization tables and two AC and DC variable-length coding tables.

When encoding, the processor will accept 11-bit DCT coefficients as generated by the L64735 or similar device. The coefficients are quantized, coded and buffered into 32-bit words. A 32-word output fifo makes it possible to read the data in bursts.

When decoding, the device accepts 32-bit words from the buffer, decodes the events and reconstructs the DCT coefficients which are output in format suitable for processing by the L64735.

The encoding and decoding operations can process one pixel and/or event each cycle. This feature makes is possible to cascade the L64745 with the DCT (DCT processor) for high-speed image compression systems.

The device can also be used to perform the lossless 2-D (two-dimensional) DPCM coding excluding the 2-D prediction and to collect statistics for code table generation.

Features

- Compatible with proposed JPEG standard (8-R8)
- Performs quantization, run coding and variable-length coding
- 32-word coded data FIFO
- Two downloaded AC and DC code tables
- Four downloaded quantization tables
- Can be cascaded with DCT in encoder and decoder modes
- Supports lossless mode
- Mode for collecting statistics for code table generation
- Can be used in non-JPEG systems
- 20/27 MHz data rates
- 84-pin CPGA (ceramic pin grid array) or PPGA (plastic pin grid array) or 100 lead PQFP (plastic quad flat pack) package

LSI LOGIC

L64750/51 CCITT Variable-Length Coder/Decoder
Preliminary

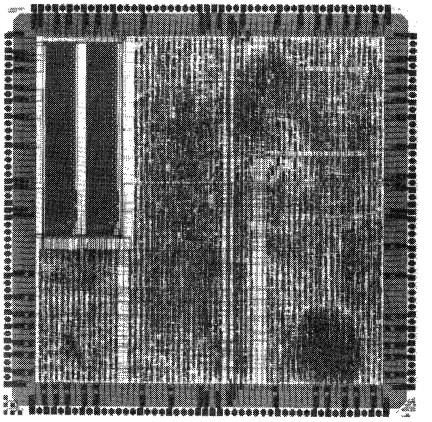
Description

The L64750 and L64751 perform the run-length and variable-length coding and decoding functions of the CCITT (Consultative Committee for International Telephones and Telegraphs) video compression standard, respectively.

The L64750 encoder accepts quantized DCT coefficients from the L64740 DCT Quantization Processor and parameters from the L64760 Interframe Processor and the motion compensator (the parameters include the quantization stepsize, the motion vectors, the loop filter flag and the inter-intra decision flag). The data is multiplexed and coded according to the CCITT H.261 standard. The composite coded data is packed into 24-bit words for transmission or storage. The device encodes each quantized DCT coefficient in a single cycle.

The L64751 decoder accepts 24-bit words of composite coded data. The header information is decoded and system parameters are passed to the appropriate devices. Each quantized DCT coefficient is decoded in a single cycle and hence can be used in high-speed pipelined systems. The L64751 also optionally performs the inverse quantization and zig-zag to raster conversion within each block. When operating in this mode, the L64751 is connected directly to the L64730 IDCT processor without the need for a quantization processor.

Both devices were designed to operate with L64730 (DCT Processor), L64740 (DCT Quantization Processor) and L64760 (Interframe Processor) to form a compact video compression system that can operate at data rates ranging from those required for full CIF CCITT systems to those needed for processing broadcast quality video.



L64750/51

Features

- Compatible with proposed CCITT standard
- Decoder and Encoder
- Packed 24-bit coded I/O
- Simple interface to other L647XX devices
- Up to 20/27 MHz clock rates
- Full or quarter CIF
- L64750 is available in a 68-pin CPGA (ceramic pin grid array) or PPGA (plastic pin grid array) or 80-pin PQFP (plastic quad flat pack)
- L64751 is available in a 68-pin CPGA (ceramic pin grid array) or PPGA (plastic pin grid array) or 100-pin PQFP (plastic quad flat pack)

L64760 Interframe Processor
Preliminary

Description

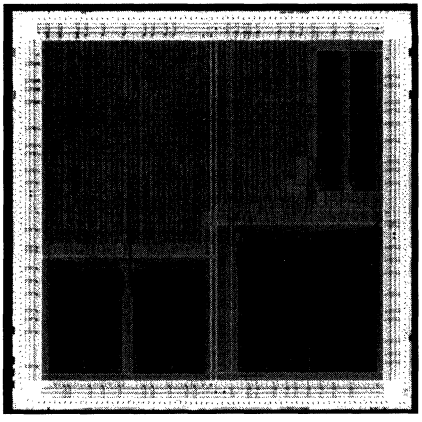
The L64760 performs many of the functions required for the interframe prediction of the CCITT (Consultative Committee for International Telephones and Telegraphs) video compression standard. The current frame data and the motion compensated (optional) previous frame data are supplied as inputs to the device. The loop filtering will be performed if the previous frame data has been motion compensated. The decision is then made to process the data in an intraframe or interframe mode by comparing the energy of the luminance data in the current frame to the energy of the difference between the current and previous frame luminance data. The signal with less energy is sent to the DCT (Discrete Cosine Transform) processor (decision made according to RM8). The reconstructed pixel values are generated by summing the prediction value with the output of the IDCT (Inverse Discrete Cosine Transform).

In decoder mode, the inter-intra decision is transmitted from the variable-length decoder and the internal decision circuit is not used.

All delays associated with internal or external processes are compensated internally and hence are transparent to the user.

The device also generates strobes for the variable-length coder (L64750) and the quantizer (L64740). In addition, the quantization stepsize from the channel data buffer is latched by the L64760 and sent to the quantization processor at the next macroblock boundary.

The internal inter-intra decision can be overridden externally for forced updating.



L64760 Chip

Features

- Compatible with CCITT H.261
- Loop filter
- Internal/external intra-inter decision
- Performs pixel reconstruction
- System delays internally compensated
- Up to 30/40 MHz clock rates
- Simple external control
- 100-pin CPGA (ceramic pin grid array), PQFP (plastic quad flat pack) or PPGA (plastic pin grid array) package

Pin Listing and Description

(SIGNAL.0 is always the LSB)

CFI.0:7
Eight-bit data input bus for current frame pixel data. The data is input one macroblock at a time, with each 8 x 8 pixel block raster scanned. This bus is not used in decoder mode.

PFI.0:7
Eight-bit data input bus for previous frame pixel data which has been motion compensated (if desired). The data is input one macroblock at a time, with each 8 x 8 pixel block raster scanned.

PFO.0:7
Eight-bit data output bus for previous frame pixel data. The data is output one macroblock at a time, with each 8 x 8 pixel block raster scanned. This data updates the previous frame data store.

PPIXO.0:8
Nine-bit predicted pixel output bus for data to be coded by the DCT processor. The data is output one macroblock at a time, with each 8 x 8 pixel block raster scanned. This bus is not used in decoder mode.

LSI LOGIC

MIPS Microprocessors

RISC Products MIPS Architecture Microprocessors and Peripherals

LSI LOGIC

Description

The LR2000 and LR3000 CPUs are high-speed HCMOS implementations of the Industry Standard MIPS RISC (Reduced Instruction Set Computer) microprocessor architecture. The MIPS architecture was initially developed at Stanford University under the auspices of DARPA. Both the LR2000 and LR3000 RISC microprocessors are extensions of the Stanford MIPS architecture developed by MIPS Computer Systems Inc. This architecture makes possible a microprocessor that can execute instructions for high-level language programs at rates approaching one instruction per processor clock.

The LR2000 and LR3000 microprocessors include on-chip memory management and support for up to three external coprocessors including the single-chip LR2010 and LR3010 Floating-Point Accelerators.

Features

- Reduced Instruction Set Computer (RISC) architecture
  - MIPS Instruction set
  - Simple 32-bit instructions
  - Register-to-register load-store operation
  - All instructions (except MPY and DIV) execute in a single cycle
- High performance
  - Fast instruction cycle with five-stage pipeline
  - Efficient handling of pipeline stalls and exceptional events
- Optional devices tightly coupled for high performance
  - LR2010/LR3010 Floating-Point Accelerator (FPA)
  - LR3220 Read/Write Buffer
  - LR2020/LR3020 Write Buffers (WB)
  - MipSET workstation chipset
- 32 general-purpose registers
- On-chip cache control
- On-chip memory management unit (MMU)
  - Fully-associative, 64-entry translation lookaside buffer (TLB)
  - Supports 4 Gbyte virtual address space
- Multi-tasking support
  - User and kernal (supervisor) modes
- Tightly-coupled coprocessor interface
  - Generates all addresses and handles memory interface control
  - Supports up to three external coprocessors
- Strong, integrated software support
  - RISC/OS operating system
  - SVID-Compliant version of UNIX
  - Optimizing compilers

C	Ada (Verdix)
FORTRAN	LPI-COBOL
Pascal	LPI-PL-1

  - Systems Programmer's Package
  - A complete integrated tool kit used to "Bring up" target systems.

LSI LOGIC

Components

Family	Product Code	Description	Clock Rate (MHz)	Packages
LR2000	LR2000	MIPS RISC CPU	12.5, 16.7	144 CPGA
	LR2010	Floating-Point Accelerator	12.5, 16.7	84 CLDCC-J
LR3000	LR3000	MIPS RISC CPU Military Version	16.7, 20, 25 16.7, 20	172 CLDCC 144CPGA
	LR3000A	Enhanced MIPS RISC CPU	25, 33.3	175 CPGA - cavity down 172 CLDCC - cavity down
	LR3010	Floating-Point Accelerator Military Version	16.7, 20, 25 16.7, 20	84 CPGA - cavity down 84 CLDCC - cavity down
	LR3010A	Enhanced FP Accelerator	25, 33.3	84 CPGA - cavity down 84 CLDCC - cavity down
	LR3220	Integrated Read/Write Buffer	25, 33.3	180 CPGA 184 PQFP
MipSET	LR3201	RST/INT Controller	20, 25	64 PQFP
	LR3202	L-Bus Controller	20, 25	208 PQFP
	LR3203	DRAM Controller	20, 25	160 PQFP
	LR32D04	Integrated DRAM Data Buffer	20, 25	100 PQFP
	LR3205	Block Transfer Buffer	20, 25	208 PQFP
MIPS Ngine	RPM3310	LR3000 & LR3010 Module w/ 32K I&D Cache & R/W Buffer	20, 25	Module Board
	RPM3330	LR3000A & LR3010A Module with 64K I&D Cache with Multiprocessor support	33.3	Module Board
Embedded Processor	LR33000	Highly integrated MIPS based Embedded Processor	25, 33.3 25	155 CPGA 160 PQFP

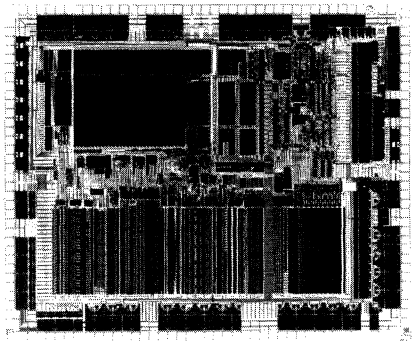
LSI LOGIC

LR2000 MIPS RISC Microprocessor

Description

The LR2000 CPU is a high-speed HCMOS implementation of the MIPS RISC (Reduced Instruction Set Computer) microprocessor architecture. The MIPS architecture was initially developed at Stanford University under the auspices of DARPA. The LR2000 is an extension of the Stanford MIPS architecture developed by MIPS Computer Systems, Inc. This architecture makes possible a microprocessor that can execute instructions for high-level language programs at rates approaching one instruction per processor clock. It supports up to three tightly coupled coprocessors including the single chip LR2010 Floating-Point Accelerator.

The full-custom 32-bit VLSI CMOS Reduced Instruction Set Computer shown in the CPU chip photo includes thirty-two 32-bit registers, on-chip TLB (translation lookaside buffer), memory management unit, and cache control circuitry.



LR2000 CPU Chip

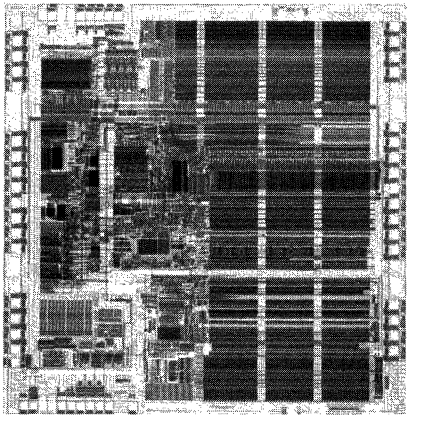
Features

- Reduced Instruction Set Computer (RISC) architecture
  - MIPS instruction set
  - Simple 32-bit instructions, single addressing mode
  - Register-to-register, load-store operation
  - All instructions (except MPY and DIV) execute in a single cycle
- High performance
  - Fast instruction cycle with five-stage pipeline
  - Efficient handling of pipeline stalls and exceptional events
- Two speed versions
  - LR2000GC-12 12.5 MHz 8 VAX mips equivalents
  - LR2000GC-16 16.7 MHz 10 VAX mips equivalents
- Optional devices tightly coupled for high performance
  - LR2010 Floating-Point Accelerator (FPA)
  - LR2020 Write Buffers (WB)
- 32 general-purpose registers
- On-chip cache control
  - Separate external instruction and data cache memories
  - From 4 to 64 Kbytes each
  - Both cache memories accessed during a single CPU cycle
  - Dual cache bandwidth up to133 Mbytes/second
  - Uses standard SRAMs
    LR2000GC-12 35 ns access time
    LR 2000GC-16 25 ns access time
- On-chip memory management unit (MMU)
  - Fully-associative, 64-entry translation lookaside buffer (TLB)
  - Supports 4-Gbyte virtual address space
- Multi-tasking support
  - User and kernel (supervisor) modes
- Seamless coprocessor interface
  - Generates all addresses and handles memory interface control
  - Supports up to three external coprocessors
- Strong, integrated software support
  - RISC /OS operating system
    System V.3,4.3 BSD
  - Optimizing compilers
    C Ada (Verdix)
    FORTRAN COBOL (LPI)
    Pascal PL-1 (LPI)
  - Systems Programmer's Package-
    A complete, integrated tool kit used to bring up target systems
- 144-pin CPGA (ceramic pin grid array) package

LR2010 MIPS Floating-Point Accelerator
Preliminary

Description

The LR2010 Floating-Point Accelerator (FPA) provides high-speed, floating-point capability for systems based on the LR2000 CPU. The organization of FPA architecture is similar to that of the CPU, allowing high-level language compilers to optimize both integer and floating-point performance. The LR2010, with associated system software, fully conforms to the requirements and recommendations of the ANSI/IEEE Standard 754-1985. The LR2010 connects seamlessly to the CPU. Since both units receive instructions in parallel, floating-point instructions can be initialized at the same single-cycle rate as fixed-point instructions.



LR2010 FPA Chip

Features

- Fully compatible to ANSI/IEEE Standard 754-1985 floating-point arithmetic
- Supports single- and double-precision data formats
- High speed throughput, low latency
- Two speed versions
  - LR2010LC-12 12.5 MHz
  - LR2010LC-16 16.7 MHz
- Highly pipelined architecture coupled with optimizing compilers generates high throughput.
- Load/store oriented instruction set initiates floating-point instructions in a single cycle and overlaps execution with additional fixed or floating-point instructions
- Status/control registers implemented to provide access to all IEEE Standard exception handling capability
- Sixteen on-chip 64-bit registers individually accessible for flexible operation
- Complete instruction set
  - Single and double precision multiply, divide, add, subtract, negate, absolute value
  - Conversion to/from all supported formats
  - Comparison instructions derived from predicates named in IEEE Standard
- 84-pin CLDCC (ceramic leaded chip carrier) package
- LR2010 FPA performance floating-point benchmarks
- Linpack
  - Single precision 4.8 MFlops
  - Double precision 2.2 MFlops
- Whetstone
  - Single precision 11.4 MWips
  - Double precision 9.1 MWips
- Livermore loops
  - Single precision 9.6 x VAX 11/780
  - Double precision 12.1 x VAX 11/780
  - Spice 9.7 x VAX 11/780
  - 256-Point FFT 23 x VAX 11/780

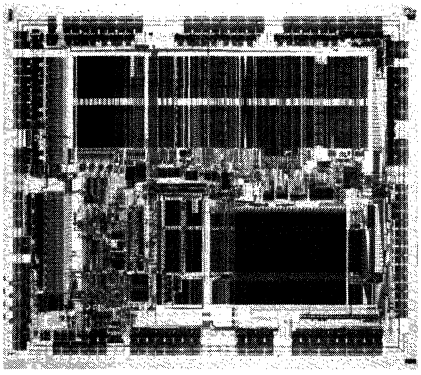
LSI LOGIC

LR3000 MIPS RISC Microprocessor

Introduction

The LSI Logic LR3000 is a 32-bit RISC (Reduced Instruction Set Computer) microprocessor for use in multiprocessing servers to low-cost workstations, and high-performance embedded controllers through various military applications. The LR3000 consists of two tightly coupled processors implemented on a single chip. The first processor is a full 32-bit CPU, which incorporates RISC techniques to achieve a new standard of microprocessor performance. The second processor is a system control coprocessor, referred to as CP0, which contains a Translation Lookaside Buffer (TLB) and control registers to support a virtual memory subsystem with a dual-cache bandwidth of up to 200 Mbytes/second.

The MIPS architecture grew out of earlier RISC hardware and software development efforts at Stanford University. Developing the hardware and software in tandem enabled the system architects to make performance tradeoffs across the hardware/software boundary. They verified that every function or feature that complicated the hardware design measurably enhanced system performance before implementing it.



LR3000 Chip

The resulting instruction set is very well tuned for high-level language use, in contrast to many other machines labeled RISC, which have user-level instructions or instruction mode combinations that are very difficult to reach from compiled languages.

Features

- RISC architecture
- MIPS instruction set
- Load/store architecture supports configurable endian-ness and misaligned data
- All instructions execute in one cycle (except multiply and divide), and the system execution rate approaches one instruction per cycle
- Five-stage pipeline provides precise, efficient handling of pipeline stalls and exceptions
- LR2000-compatible instruction set
- Complete on-chip cache control supports separate, external data and instruction caches of up to 256 Kbytes each
- Both caches are accessible during a single CPU cycle
- On-chip Memory Management Unit (MMU) with fully associative, 64-entry Translation Lookaside Buffer (TLB) provides fast address translation for virtual-to-physical memory mapping of up to 4 Gbytes of virtual address space
- Seamless coprocessor interface generates all addresses and handles memory interface control for up to three tightly coupled external coprocessors, including the LR3010 Floating-Point Accelerator (FPA)
- Strong integrated software support includes the RISC/OS operating system (SVID-compliant version of UNIX) and high-performance optimizing compilers for C, Pascal, Fortran, Ada, Cobol, and PL/1
- Flexible, on-chip multiprocessor support for low-cost duplicate tags or a high-performance secondary cache system
- Development system supports complete, native hardware, software, and applications development environment
- Three speed options, 16.67, 20, and 25 MHz, provide a wide price/performance range
- Multi-source pin compatibility in advanced LSI Logic 172-pin CLDCC (ceramic leaded chip carrier) and 144-pin CPGA (ceramic pin grid array) packages

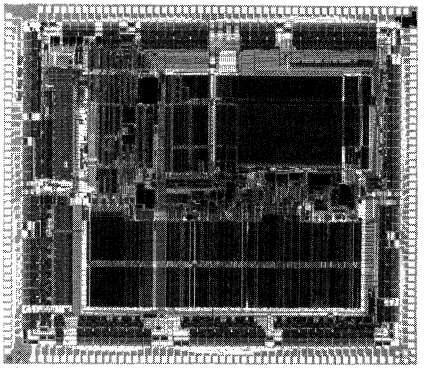
LSI LOGIC

LR3000A MIPS RISC Microprocessor
Preliminary

Introduction

The LSI Logic LR3000A is a 32-bit MIPS Reduced Instruction Set Computer (RISC) microprocessor for use in applications that include multiprocessing servers, low-cost workstations, and high-performance embedded controllers. The LR3000A consists of two tightly coupled processors implemented on a single chip. One processor is a 32-bit CPU, which incorporates RISC techniques to achieve a new standard of microprocessor performance. The other processor is a system control coprocessor that contains a Translation Lookaside Buffer (TLB) and control registers to support a virtual memory subsystem with a dual-cache bandwidth of up to 267 Mbytes/second. The LR3000A maintains compatibility with the LR3000 while providing several enhancements.

The MIPS architecture grew from earlier RISC hardware and software development efforts at Stanford University. Developing the hardware and software in tandem enabled the system architects to make performance tradeoffs across the hardware/software boundary. Any function or feature that complicated the hardware design was implemented only if it measurably enhanced system performance. The resulting instruction set is very well tuned for high-level language use, in contrast to many other machines labeled RISC, which have user-level instructions or instruction mode combinations that are very difficult to reach from compiled languages.



LR3000A Chip

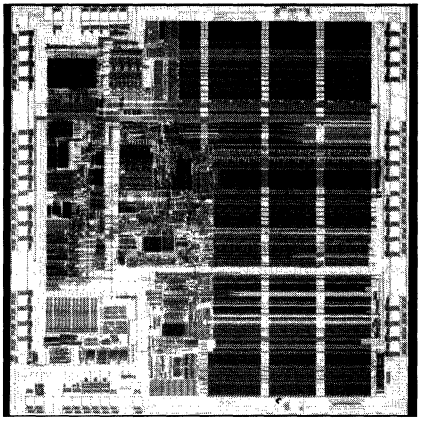
Features

- MIPS I instruction set
- Two speed options, 25 and 33.33 MHz, provide a wide price/performance range
- Load/store architecture supports configurable byte ordering and misaligned data
- All instructions execute in one cycle (except multiply and divide), and the system execution rate approaches one instruction per cycle
- Five-stage pipeline provides precise, efficient handling of pipeline stalls and exceptions
- Complete on-chip cache control supports separate, external data and instruction caches of up to 256 kbytes each
- Both caches are accessible during a single CPU cycle
- On-chip Memory Management Unit (MMU) with fully associative, 64-entry Translation Lookaside Buffer (TLB) provides fast address translation for virtual-to-physical memory mapping of up to 4 Gbytes of virtual address space
- LR3000A enhanced features include parity error detection, ignore parity option, byte-ordering reversal and a high-impedance option for the AdrLo bus during multiprocessor stalls
- Flexible, on-chip multiprocessor support for low-cost duplicate tags or a high-performance secondary cache system
- Seamless coprocessor interface generates all addresses and handles memory interface control for up to three tightly coupled external coprocessors, including the LR3010A Floating-Point Accelerator (FPA)
- Strong integrated software support includes the RISC/OS operating system (SVID-compliant version of UNIX) and high-performance optimizing compilers for C, Pascal, FORTRAN, Ada, COBOL, and PL/1
- Development system supports complete, native hardware, software, and applications development environment
- Multi-source pin compatibility in advanced LSI Logic 172-pin CLDCC (ceramic leaded chip carrier) and 175-pin CPGA (ceramic pin grid array) packages

LR3010 MIPS Floating-Point Accelerator

Description

The LR3010 Floating-Point Accelerator (FPA) provides high-speed, floating-point capability for systems based on the LR3000 CPU. The organization of FPA architecture is similar to that of the CPU, allowing high-level language compilers to optimize both integer and floating-point performance. The LR3010, with associated system software, fully conforms to the requirements and recommendations of the ANSI/IEEE Standard 754-1985. The LR3010 connects seamlessly to the CPU. Since both units receive instructions in parallel, floating-point instructions can be initiated at the same single-cycle rate as fixed-point instructions.



LR3010 FPA Chip

Features

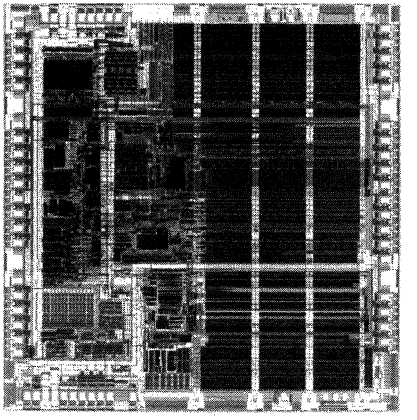
- Fully compatible to ANSI/IEEE Standard 754-1985 floating-point arithmetic
- Supports single- and double-precision data formats
- High-speed throughput, low latency
- Three speed versions: 16.7, 20, 25 MHz
- Highly pipelined architecture coupled with optimizing compilers generates high throughput
- Load/store oriented instruction set initiates floating-point instructions in a single cycle and overlaps execution with additional fixed or floating-point instructions
- Status/control registers implemented to provide access to all IEEE Standard exception handling capability
- Sixteen on-chip 64-bit registers individually accessible for flexible operation
- Complete instruction set
  - Single- and double-precision multiply, divide, add, subtract, negate, absolute value
  - Conversion to/from all supported formats
  - Comparison instructions derived from predicates named in IEEE Standard
- Available in 84-pin CLDCC (ceramic leaded chip carrier) (cavity down) and 84-pin CPGA (ceramic pin grid array) (cavity down) packages
- LR3010 FPA performance floating-point benchmarks
- SPEC floating-point 16.8
- Linpack
  - Single precision 7.1 MFlops
  - Double precision 4.0 MFlops
- Whetstone
  - Single precision 13.6 MWips
  - Double precision 16.4 MWips
- Livermore loops
  - Single precision 14.4 x VAX 11/780
  - Double precision 18.2 x VAX 11/780
  - Spice 16.0 x VAX 11/780
  - 256-Point FFT 29.0 x VAX 11/780

LSI LOGIC

LR3010A MIPS Floating-Point Accelerator

Description

The LR3010A Floating-Point Accelerator (FPA) provides high-speed, floating-point capability for systems based on the LR3000A CPU. The organization of FPA architecture is similar to that of the CPU, allowing high-level language compilers to optimize both integer and floating-point performance. The LR3010A, with associated system software, fully conforms to the requirements and recommendations of the ANSI/IEEE Standard 754-1985. The LR3010A connects seamlessly to the CPU. Since both units receive instructions in parallel, floating-point instructions can be initiated at the same single-cycle rate as fixed-point instructions.



LR3010A FPA Chip

Features

- Fully compatible to ANSI/IEEE Standard 754-1985 floating-point arithmetic
- Supports single- and double-precision data formats
- High-speed throughput, low latency
- Two speed versions: 25 and 33 MHz
- Highly pipelined architecture coupled with optimizing compilers generates high throughput
- Load/store oriented instruction set initiates floating-point instructions in a single cycle and overlaps execution with additional fixed or floating-point instructions
- Status/control registers implemented to provide access to all IEEE Standard exception handling capability
- Sixteen on-chip 64-bit registers individually accessible for flexible operation
- Complete instruction set
  - Single and double precision multiply, divide, add, subtract, negate, absolute value
  - Conversion to/from all supported formats
  - Comparison instructions derived from predicates named in IEEE Standard
- Available in 84-pin CLDCC (ceramic leaded chip carrier) (cavity down) and 84-pin CPGA (ceramic pin grid array) (cavity down) packages
- LR3010A FPA performance floating-point benchmarks
- SPEC floating-point 16.8
- Linpack
  - Single precision 7.1 MFlops
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  - Single precision 13.6 MWips
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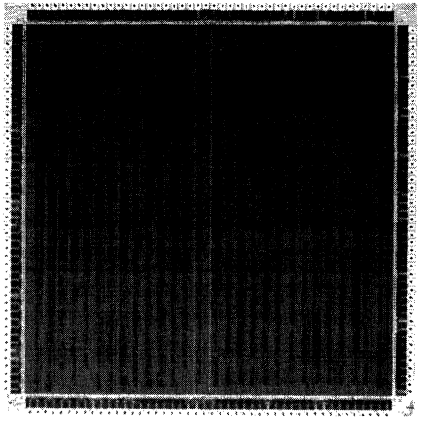
  - Single precision 14.4 x VAX 11/780
  - Double precision 18.2 x VAX 11/780
  - Spice 16.0 x VAX 11/780
  - 256-Point FFT 29.0 x VAX 11/780

LSI LOGIC

LR3220 MIPS Read-Write Buffer
Preliminary

Introduction

The LR3220 Read-Write Buffer enhances the performance of MIPS architecture-based systems by buffering write and read operations. Using the Read-Write Buffer, the system can perform memory write operations at the cycle rate of the processor, instead of stalling the processor to write data to memory. On memory read operations, the system uses the Read-Write Buffer to pass the read address to main memory and latch the read data from memory. The Read-Write Buffer generates parity and then passes the data and parity to the processor. A single LR3220 provides six-deep write buffering and one level of read buffering for 32 bits of address and 32 bits of data. It operates at the system clock rate, and is available at 25 and 33.33 MHz to support the requirements of LR3000-based systems.



LR3220 Chip

Features

- Combines the functionality of four LR3020 Write Buffers
- Minimizes additional loading on the address and data buses with on-chip data and address latches for read operations
- Supports big endian and little endian byte-order addressing
- Uses byte mask outputs to ease system design
- Performs block-mode conflict detection for block sizes of eight words or less
- Offers separate enable signals for all address and data buses
- Supports fast page-mode writes for 1 MBit DRAM-based memory implementations
- Provides six-deep write buffering of data and addresses
- Supports two operating modes:
  1) LR3000 mode
     - Compatible with the LR3000's staggered Address and Tag bus timing - decodes AccTyp [1:0] and AdrLo [1:0] inputs for byte ordering
  2) Harvard mode
     - Uses synchronous address latching on the rising edge of the clock
     - Uses byte mask inputs for byte ordering
- Offered in both 180-pin CPGA (ceramic pin grid array) and compact 184-pin PQFP (plastic quad flat pack) packages

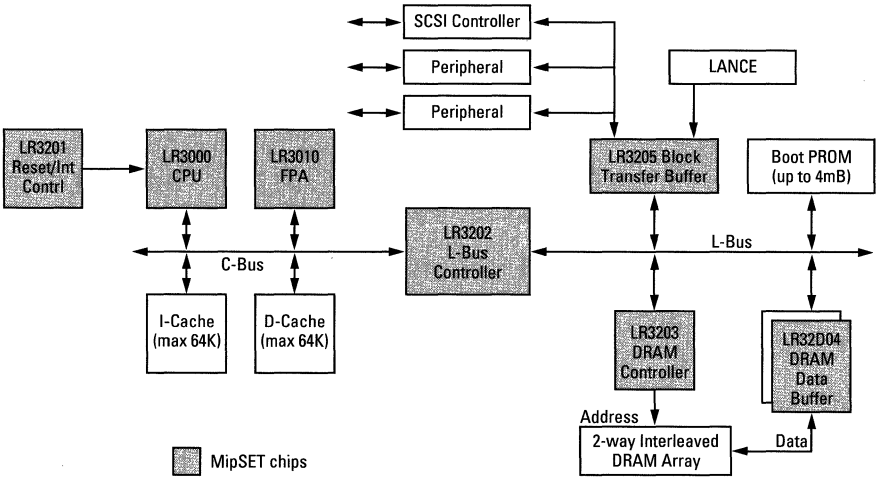
MipSET Chips

Description

The MipSET™ chips are the industry's first complete set in support of the MIPS RISC microprocessor. The MIPS RISC Architecture is regarded as the highest performance microprocessor available today and is already used in a variety of applications including 3-D graphics, workstations, super-minicomputers, On-Line-Transaction-Processors and high-performance desktop systems. Virtually all of these systems have required extensive engineering time and effort to complete. The MipSET chips provide a common solution for the basic functions of a computer, allowing the system vendor to significantly reduce design cost and effort while accelerating time-to-market. All without comprising performance.

LSI Logic's MipSET chips include the LR3201 Reset/Interrupt Controller, the LR3202 L-Bus Controller, the LR3203 DRAM Controller, the LR32D04 DRAM Data Buffer and the LR3205 Block Transfer Buffer along with the LR3000(A) CPU and the LR3010(A) Floating-Point Accelerator. With the MipSET chips, cache, main memory, ROM, SCSI, Ethernet, floppy disk controller, one parallel and four serial ports, a complete workstation can be implemented with as few as 30 ICs.

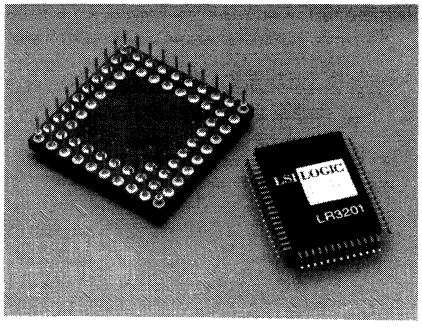
MipSET System Block Diagram



LR3201 MipSET
RST-INT Controller
Preliminary

Description

The LR3201 RST-INT Controller device is designed to control the reset and interrupt inputs for the LR3000 CPU, and the initialization sequence defined by the LR3000 mode select programming of the W, X, Y and Z cycles during reset.

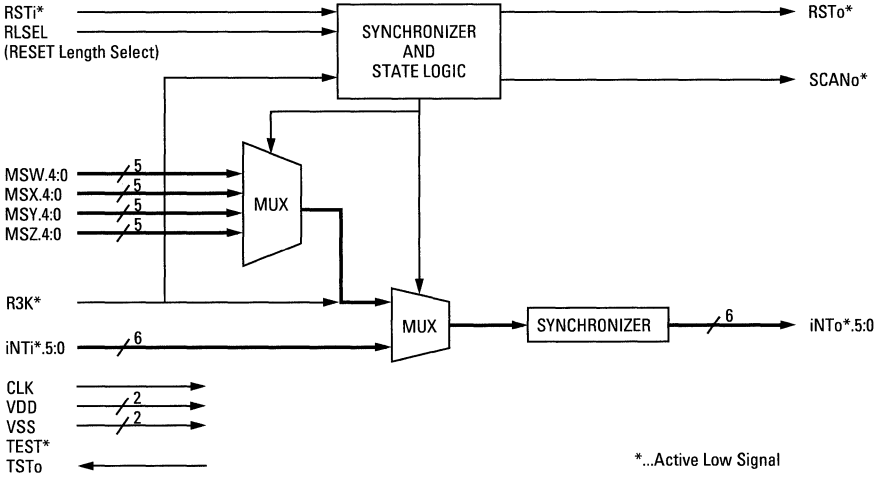


LR3201 Chip

Features

- Up to 25 MHz LR3000 system
- Schmitt trigger type asynchronous RESET input
- A synchronous RESET input, and synchronous RESET output for LR3000 CPU
- Selectable RESET output active time length (132 or 8196 clock cycles)
- W, X, Y and Z cycle support for LR3000 CPU initialization
- Interrupt input synchronization

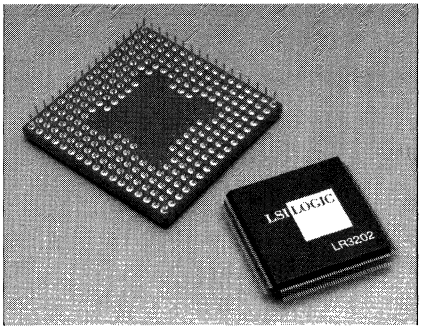
Block Diagram



LR3202 MipSET Bus Controller
Preliminary

Description

The LR3202 Bus Controller is a member of the LR3000 microprocessor peripheral chip family and is designed to provide the functions critical to implement LR3000-based general purpose computer systems. The LR3202 Bus Controller interfaces directly with LR3000 Cache-bus (C-Bus), and the complete control logic necessary for data transfer between cache and memory subsystem are supported. The LR3202 acts as a master device for L-Bus, which is newly defined by LSI Logic and designed to accommodate a chip level interconnect with a variety of memory and I/O controllers.



LR3202 Chip

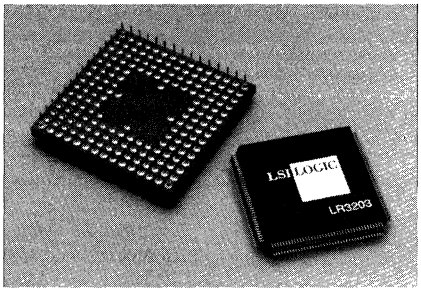
Features

- Up to 25 MHz LR3000 system
- Big endian/little endian mode selection
- LR3000 cache bus interface
  - External read buffers might be required for high clock frequency (25 MHz) system
- Memory and I/O local bus (L-Bus) interface
  - Accommodates general purpose peripheral controllers
- Bus arbitration
  - Arbitration for the access to L-Bus, instruction fetch, data read, data write and DMA request
- Block refill operation for both instruction and data read are supported via L-Bus burst transfer
  - Programmable selection of 4, 8, 16 or 32 words block refill mode
- Eight-level deep write buffer FIFO
- Boot ROM Interface
  - Boot ROM chip select output signal
  - 32-bit or 8-bit boot ROM data bus width selection, data assembly for 8-bit mode
  - Programmable wait-state cycle control
- DRAM main memory interface
  - Interface to LR3203 DRAM Controller
  - Programmable DRAM refresh interval timer
- Three independent I/O area selection outputs with programmable wait-state cycle control
- Vectored interrupt interface (up to 256 type vectored interrupts)
- 224-pin CPGA (ceramic pin grid array) or 208-pin PQFP (plastic quad flat pack) (gull-wing) package

LR3203 MipSET DRAM Controller
Preliminary

Description

The LR3203 DRAM Controller is a member of the LR3000 microprocessor peripheral chip family and is designed to provide interface necessary to build an L-Bus-based main memory subsystem. The LR3203, when used in conjunction with the LR3204 DRAM Data Bus Buffer, allows the system designer to build a highly integrated memory system.



LR3203 Chip

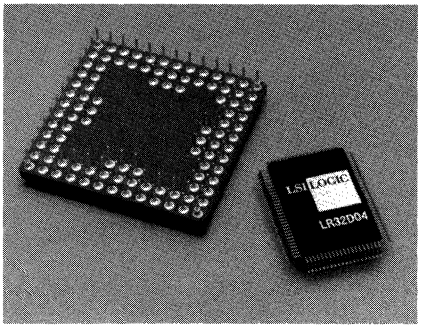
Features

- Up to 25 MHz operation in LR3000 system
- Variety of DRAM components, 1M x 1, 256K x 4, 4M x 1 or 1M x 4
- 2-Way interleaved DRAM implementation allowing block refill or burst transfer (maximum 32 words) over L-Bus (LSI Logic Local Bus) at 100 MBytes/sec = peak transfer rate
- Either 8 MBytes or 16 MBytes memory area supported per LR3203 when used with 1M x 1-bit DRAM's
- Maximum 16 MBytes memory area with 2 MBytes granularity supported per LR3203 when used with 256K x 4 bits DRAMs
- Either 32 MBytes or 64 MBytes memory area supported per LR3203 when used with 4M x 1 bit DRAM's
- Maximum 64 MBytes memory area with 8 MBytes granularity supported per LR3203 when used with 1M x 4 bit DRAM's
- Read modify write mode at partial word write operation for x 4 type DRAM parity bits or ECC redundant bits
- 160-pin PQFP (plastic quad flat pack) package

LR32D04 MipSET DRAM Data Bus Buffer (16-Bit)
Preliminary

Description

The LR32D04 DRAM Bus Buffer is a member of the LR3000 microprocessor peripheral chip family and is designed to function as a data buffer to/from a DRAM array. LR32D04 also works as a data parity generator and checker by generating parity bits when writing a data to DRAM main memory, or checking parity bits when reading a data from DRAM array. The LR32D04 performs its function as a 16-bit (Halfword) device, thus, two (2) LR32D04s are required to build a system based on M-3 chipset. In conjunction with the LR3203 DRAM Controller, the LR32D04 DRAM Data Bus Buffer provides a complete interface solution necessary for a main memory subsystem built around the various types of DRAM components widely available in the market.



LR32D04 Chip

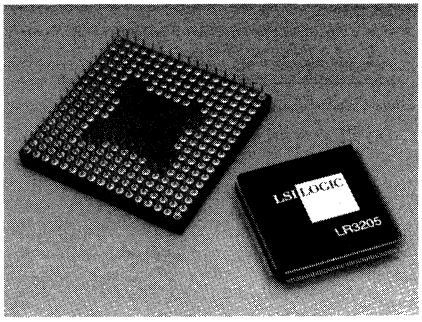
Features

- Up to 25 MHz LR3000 system
- 2 LR32D04's required for 32-bit data bus
- Data separator and/or selector for 2-way interleaved DRAM bank
- Direct drive capability for DRAM Data Bus (12 mA type high speed output buffer)
- Optional Read-Modify-Write function for interfacing with 4-bit wide DRAM components
- 100-pin CPGA (ceramic pin grid array) or 100-pin PQFP (plastic quad flat pack) package

LR3205 MipSET Block Transfer Buffer
Preliminary

Description

The LR3205 Block Transfer Buffer is a member of the LR3000 microprocessor peripheral chip family and is designed to provide the interface between the system bus, the L-Bus and various I/O devices via 8 or 16-bit I/O channels, called the B-Bus channels and the E-channels respectively. The B-Bus provides 3 DMA channels for 8-bit I/O devices and the E-channel is intended to interface with a 16-bit device. Each DMA channel can be programmed independently, and contains the 8-word x 32-bit FIFO memory, which allows burst mode data transfers between the DRAM main memory subsystem and each I/O device. The LR3205 can interface to AMD 7990 LANCE and NCR 53C90 SCSI controller without any glue devices.



LR3205 Chip

Features

- Up to 25 MHz LR3000 system
- Big endian/little endian mode selection
- 4 independent DMA channels (one 16/8-bit channel and three 8-bit channels)
- Byte to word assembly and word to byte disassembly function
- 8-word x 32-bit FIFO memories for each channel
- 4-word burst block transfer to or from main memory
- Direct interface capability to Am7990 LANCE and NCR 53C90 SCSI controller
- Independent polarity control of DMA acknowledge outputs
- Internal or external end of process control for each channel
- Reset control outputs for each channel I/O device
- Cascading capability for more than 4 DMA channels
- 208-pin PQFP (plastic quad flat pack) (gull-wing) package

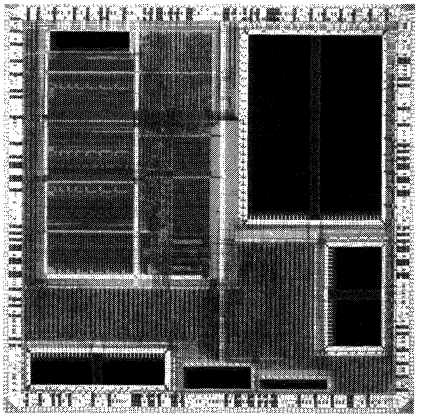
LR33000
MIPS RISC
Embedded Processor

Description

The LR33000 processor is a MIPS-compatible, single-chip controller designed for high performance embedded processor applications. With its on-board caches, write buffer and flexible memory interface, it facilitates low-cost embedded processor designs requiring the high performance of 32-bit RISC.

The LR33000 consists of a MIPS CPU core along with system functions which significantly reduce the overall number of chips required to build a system. This reduction in component count helps to substantially cut the overall system cost and power consumption and improve system reliability. This processor maintains user binary software compatibility with the LR2000 and LR3000/A implementations of the MIPS architecture, allowing direct portability of the growing base of MIPS software and development tools.

The LR33000's bus interface design allows it to interface to the rest of the system in a simple and cost effective manner. The LR33000's system on a chip approach integrates the following units onto a single device: MIPS compatible CPU, 8kbytes of Instruction Cache, 1-kbyte of Data Cache, Write Buffer, Timer/Counters, DRAM Controller, 8 and 32-bit wide boot PROM support, programmable wait-state generators and an improved memory interface.



LR33000 Chip

The LR33000 is specifically tuned for applications that requires high performance yet are sensitive to systems cost and power consumption. This embedded processor fits into applications such as laser beam printers, X Window terminals, LAN controllers, I/O processors, disk controllers, graphics rendering and military/avionics.

Features

- RISC architecure
  - MIPS instruction set
  - Single-cycle instruction execution
  - LR2000/LR3000/LR3000A user software binary compatibility
- High on-chip integration
  - 8 kbyte I-Cache
  - 1 kbyte D-Cache
  - 1 deep write buffer
  - 3 timers/counters
  - Integrated DRAM controller
- Simple I/O interface
  - Direct DRAM interface
  - Glueless 8-bit boot PROM support
  - Direct interface to other memories and peripherals
  - DMA interface support
  - Programmable wait-state generation
- Simple 1X clock input
- Debug features
  - Hardware breakpoint registers
  - Instruction trace capabilities
- Cache coherency support
  - Bus snooping
  - Cache invalidate command
- High performance
  - Five-stage pipeline
  - Efficient handling of pipeline stalls and exceptions
- Reduced power requirements
- Three speed versions
  - 25/33/40 MHz
- Packages
  - 155-pin CPGA (ceramic pin qrid array)
  - 160-pin PQFP (plastic quad flat pack)

RPM3310
MIPS Ngine Module

Description

The RPM3310 Ngine™ Module is a high-performance CPU subsystem based on the MIPS RISC (Reduced Instruction Set Computer) architecture. The Ngine Module combines LSI Logic's LR3000 MIPS Microprocessor and LR3010 Floating-Point Accelerator with 64 Kbytes of instruction and data cache on a compact, self-contained module. By integrating the 4-phase clock generation circuitry and cache memory on the RPM3310, all critical timing paths are confined to the module. In addition, the on-board reset configuration logic greatly simplifies adapting the RPM3310 to operate in a wide range of applications.

The compact size of the module is achieved by utilizing a double-sided printed circuit board with direct die attach assembly. Thermal management and electrical properties are greatly enhanced by utilizing this technology.

LSI Logic's RPM3310 is the first of a line of MIPS pin- and function- compatible modules. This means the ability to upgrade your system's performance by simply plugging in LSI Logic's newest Ngine Module.

Features

- 18 to 20 VAX MIPS performance at 25 MHz
- 14 to 16 VAX MIPS performance at 20 MHz
- Integer and floating-point capabilities
- 32 Kbytes each of instruction and data cache
- 6-word deep write buffer
- On-board 4-phase clock generation and reset configuration logic
- Buffered I/O and control signals
- Programmable block refill sizes for data and instructions
- Instruction streaming
- Even parity generation for read operations
- Low power consumption
- Five registered interrupt inputs
- Compact size: 3.5" x 3.5" x 0.67", packaged on a double-sided PCB
- Direct silicon-on-board technology
- CPU and FPA silicon mounted on integral head spreaders
- 100-pin AMP connector

LSI LOGIC

RPM3330
MIPS Ngine Module

Description

The RPM3330 Ngine™ Module is the second generation of LSI Logic's high-performance CPU subsystem based on the MIPS RISC (Reduced Instruction Set Computer) architecture. The Ngine Module combines LSI Logic's LR3000A MIPS Microprocessor and LR3010A Floating-Point Accelerator with 128 Kbytes of instruction and data cache on a compact, self-contained module. By integrating the 4-phase clock generation circuitry and cache memory on the RPM3330, all critical timing paths are confined to the module. In addition, the on-chip reset configuration logic greatly simplifies adapting the RPM3330 to operate in a wide range of applications.

The compact size of the module is achieved by utilizing a double-sided printed circuit board with direct die attach assembly. Thermal management and electrical properties are greatly enhanced by utilizing this technology.

Features

- 27 VAX MIPS performance at 33 MHz
- Multiprocessing support
- Hardware Cache Invalidation
- Integer and floating-point capabilities
- 64 Kbytes each of instruction and data cache
- 6-word deep write buffer
- On-board 4-phase clock generation and reset configuration logic
- Buffered I/O and control signals
- Programmable block refill sizes for data and instructions
- Instruction streaming
- Even parity generation for read operations
- Low power consumption
- Five registered interrupt inputs
- Compact size: 3.5" x 3.5" x 0.67", packaged on a double-sided PCB
- Direct silicon-on-board technology
- CPU and FPA silicon mounted on integral head spreaders
- 100-pin high-speed AMP connector

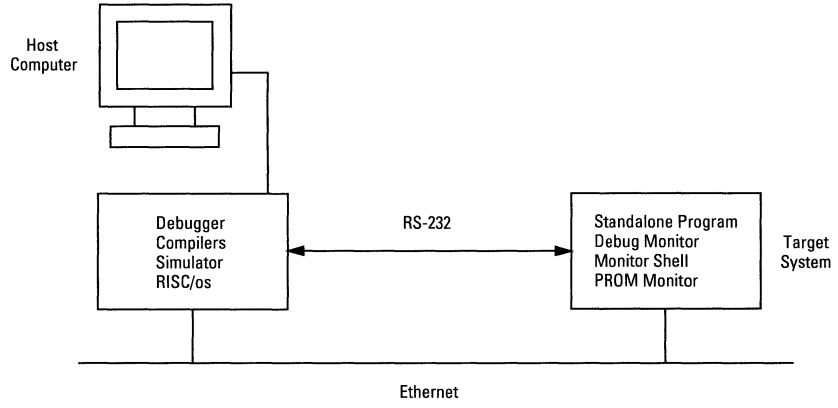
MIPS System Programmer's Package

Overview

The SSP (System Programmer's Package) accelerates the development of systems based on the high-performance MIPS RISC architecture. SSP allows system developers to execute MIPS software on an instruction set simulator, to make cache memory architectural tradeoffs early in the design cycle and to debug software on a target system. SPP includes utilities to help build standalone software and download the software to a target system. SPP is a source code product that can be customized to the user's target environment. SPP helps shorten development time since software development can begin before target hardware is ready.

Benefits

- Start software development early using simulator
  - Simulates the target system, allowing the designer to debug system software before the target hardware is ready
- Meet memory system cost and performance goals
  - Models different memory subsystems, ensuring the target system meets cost and performance objectives
- Develop software easily with a high-level debugger
  - Symbolically debugs code running on the simulator or a remote target at the source level
- Compile and link quickly using the MIPS RISComputer
  - Offers a robust programming environment in which developers can quickly compile optimized software for a target machine



SPP was designed to meet the unique requirements of customers developing MIPS-based embedded systems and UNIX systems. Unlike CISC-based systems, MIPS-based systems often include cache memory to meet cost and performance objectives. SPP includes tools to model memory subsystems. In the past, the use of software simulation was limited by the performance of CISC-based computers. Since SPP is hosted on high-performance MIPS RISComputers, instruction set simulation is a viable alternative for software development before the target hardware is available. SPP includes a target monitor for standalone software development. In addition, SPP includes a standalone I/O library and a high-level debugger for both simulation and target execution. Because SPP is provided with source code, the user can configure SPP to a specific target environment.

LSI LOGIC

MIL-STD-1750A L64500 Microprocessor

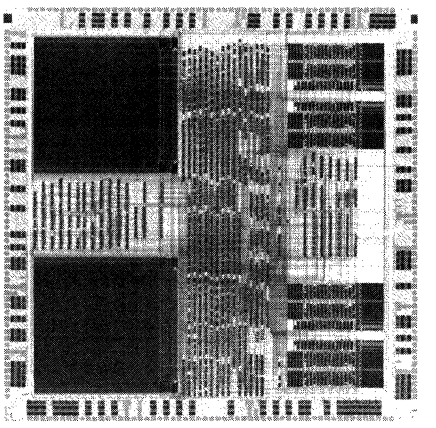
Description

The LSI Logic L64500 is a monolithic 1.5-micron drawn gate length (0.9-micron effective channel length) HCMOS chip which implements the MIL-STD-1750A (Notice 1) Instruction Set Architecture (ISA). The L64500 is a 16-bit Central Processing Unit (CPU) used for real-time processing. The CPU uses a sophisticated ALU architecture which is expandable up to 32 bits depending on the operation and uses separate address and data buses to improve system performance. It also contains independent instruction operand fetch and execution units.

The L64500 can be augmented with the L64550 (MBU) chip to implement optional enhancements of the MIL-STD-1750A. The L64550 includes a Memory Management Unit (MMU) with memory expansion capabilities up to 1 M words of memory, the Block Protect Unit (BPU), Memory Fault Status Register (MFSR), the Bus Arbitron Unit (BAU) with six bus masters, Start-up ROM interface, discrete I/O Port, Trigger-go Counter and other options.

The L64500 CPU and the L64550 MBU chips were designed as a system to optimize the performance.

The L64500 is included in LSI Logic's MDE® Design Tools as an ASIC library library element. This element can be used as a hard macros when combined with gate arrays or standard cells, or can be used in multi-chip system simulations when adding new ASIC chips to the system.



Chip Layout

The L64500 is available in several speed grades from 15 MHz to 30 MHz over the full military temperature range of -55° to 125°C.

Features

- Single-chip high-perfomance microprocessor
- Implements MIL-STD-1750A (Notice 1) Instruction Set Architecture
- 1.5-micron gate length HCMOS 2-layer metal cell-based technology
- 30 MHz operation over full military range
- Power dissipation ≤ 1 W
- TTL compatible interface
- Flexible packaging capability
- Available as ASIC hard macro library element
- Continuous panel mode operation
- Performance optimized architecture
  - Split data and address bus
  - Variable width ALU: up to 32 bits
  - Instruction pre-fetch
  - Multiport register files
- Timers A and B included on-chip
- 64K word address space expandable to 1 M word with optional MBU chip

MIL-STD-1750A
L64550
MBU Peripheral

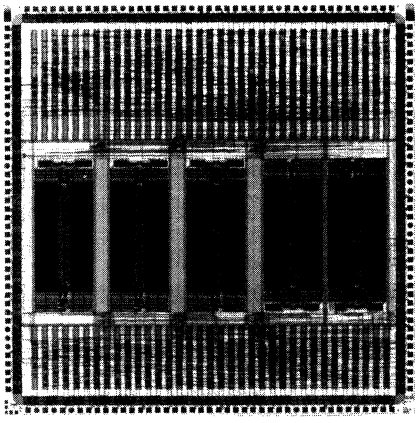
Description

The LSI Logic L64550 Memory Management and Block Protection Unit device is a monolithic 1.5-micron drawn gate length (0.9-micron effective channel length) HCMOS chip designed to support the L64500 CPU (MIL-STD-1750A ISA). The L64550 contains a number of MIL-STD-1750A support options including the Memory Management Unit (MMU) with mapping RAM, Block Protect Unit (BPU) with protection RAM, Memory Fault Status Register (MFSR), watch-dog timer and start-up ROM interface. In addition, the L64550 contains other options such as, a bus arbitrator with up to 6 bus masters, extended addressing capability to 8 M words, a discrete I/O port, sophisticated CPU/MBU handshake to increase performance and bus time-out timer.

The MMU allows addressing of up to 1 M word memory. In applications not requiring adherence to the standard, addressing can be extended to 8 M words. The MMU performs the logical-to-physical address translation and protection of logical space.

The BPU provides write protection in 1K page granularity for up to 1 M word of physical memory for both L64500 CPU and DMA access.

If desired, the MMU and the BPU can be individually disabled.



Chip Layout

The L64550 MBU and L64500 CPU are included in LSI Logic's MDE® Design Tools as ASIC library elements. These elements can be used as Gigacells when combined with gate arrays or standard cells, or they can be used in multichip system simulations when adding new ASIC chips to the system.

The L64550 is available in several speed grades from 15 MHz to 30 MHz over the full military temperature range of -55°C to 125°C.

Features

- 1.5-micron gate length HCMOS technology
- 30 MHz operation over full military range
- Power dissipation <1 W
- Memory Management Unit (MMU) with 512 x 16 cache RAM
- Block Protect Unit (BPU) with 128 x 16 cache RAM
- Hit/miss mechanism
- Discrete I/O ports
- Extended addressing to 8 M words
- Bus arbitration unit with up to 6 bus masters
- Memory Fault Status Register (MFSR)
- Start-up ROM interface
- Bus time-out timer
- Watch-dog timer
- TTL compatible interface
- Flexible packaging capability

MIL-STD-1750A L64501 Radiation-Hardened Microprocessor

LSI LOGIC

Description

The L64501 CPU from LSI Logic is a radiation-hardened, single-chip implementation of the MIL-STD-1750A instruction set. The cell-based L64501 provides separate address and data buses for enhanced performance, and it utilizes the LSI Logic radiation-hardened two-layer metal HCMOS process technology for reliable operation. The L64501 can interface directly with the L64551 Memory Management and Block Protect Unit (MBU), also available from LSI Logic, to provide optional MIL-STD-1750A enhancements and to optimize system performance.

To shorten the design cycle for L64501-based systems, L64501 CPU and L64551 MBU models are available in LSI Logic's MDE® Design Tools. The MDE Design Tools provide extensive design flexibility through its multichip and system simulation capabilities.

The radiation-hardened L64501 operates at 25 MHz over the military temperature range, -55°C to 125°C, and utilizes a single 5V ± 10% power supply.

Features

- Total ionizing dose specification 200 krad (Si)
- No single event upset (SEU) latchup detected (tested to LET = 70 MeV-cm^2/mg)
- SEU cross-section of 3.13e-^{6}cm^2/bit
- 24.7 MeV-cm^2 per milligram (LET) threshold
- Guaranteed post-radiation clock frequency of 25 MHz
- MIL-STD-883C/38510 Class B and Class S screening options
- Silicon-gate epitaxial two-layer metal LRH10000 HCMOS technology
- MIL-STD-1750A (Notice 1) Instruction Set
- SEAFAC certification for L64501 CPU and optional L64551 MBU
- Optional timers A and B implemented on-chip
- Directly interfaces with optional L64551 MBU, which provides memory management and block-protect capabilities and additional MIL-STD-1750A options
- TTL-compatible interface
- Available in 144-pin CPGA (ceramic pin grid array) and CLDCC (ceramic leaded chip carrier) packages

Radiation Test Data

LSI Logic characterized the L64501 for total ionizing dose radiation effect and single event upset (SEU) phenomena. Total dose radiation testing was performed in accordance with MIL-STD-883C, Method 1019.2, and utilized a Cobalt-60 gamma ray source. Following irradiation up to 200 krad (Si), the L64501 devices passed test characterization at 25 MHz.

LSI Logic conducted SEU testing at Brookhaven National Laboratory using the Tandem Van de Graff Facility. SEU testing utilized two ions, Chlorine-35 (202 MeV) and Nickel-58 (240 MeV).

For more information on total dose or SEU radiation testing, please refer to "MIL-STD-1750A Single Event Upset (SEU) Test Methodology", an LSI Logic test procedure report, or contact the Military Microprocessor Group of LSI Logic Corporation.

Technical Information

Refer to the L64500 MIL-STD-1750A Microprocessor Technical Manual, October, 1989.

Ordering Information

L64501 G M 25

- 25 — Screening option: M–Class B, S–Class S
- M — Package option: G–144-Pin CPGA (Ceramic pin Grid Array), L–144-Pin CLDCC (Ceramic Leaded Chip Carrier)
- G — Part number: Radiation-hardened
- L64501

L64551
MIL-STD-1740A
Radiation-Hardened
MBU

LSI LOGIC

Description

The L64551 MBU (Memory Management and Block Protect Unit) from LSI Logic is a radiation-hardened, single-chip memory management unit which supports the L64501 CPU. While the L64501 provides the required 1750A functionality as defined in MIL-STD-1750A, the L64551 focuses on the system implementation aspects and optional features of the standard.

For example, the L64551 includes on-chip control logic and fast mapping RAMs to implement both a memory management unit (MMU) and a block protect unit (BPU). The MMU provides logical-to-physical address translation and logical protection and the BPU provides physical block protection. Other on-chip functions include watch-dog and bus time-out timers, a memory fault status register (MFSR), multimaster bus arbitration and an extended addressing capability for up to 8 M words of physical memory. The L64551 can interface directly with the L64501 CPU, also available from LSI Logic, to provide these optional MIL-STD-1750A enhancements and to optimize system performance.

To shorten the design cycle for L64501-based systems, L64551 MBU and L64501 CPU models are available in LSI Logic's MDE® Design Tools. The MDE Design Tools provide extensive design flexibility through its multichip and system simulation capabilities.

LSI Logic manufactures the L64551 MBU in a two-layer metal HCMOS process. The radiation-hardened L64551 operates at 25 MHz, guaranteed after exposure, over the military temeprature range –55°C to 125°C, and utilizes a single 5V ± 10% power supply.

Features

- Total ionizing dose specification of 200 krad (Si)
- No single event upset (SEU) latchup expected; test results available Q4 89
- SEU cross-section (cm^2/bit) to be determined; test results available Q4 89
- Threshold (MeV-cm^2 per milligram (LET)) to be determined; test results available Q4 89
- Guaranteed post-radiation clock frequency of 25 MHz
- MIL-STD-1750A (Notice 1) Instruction Set
- SEAFAC certification in an L64501-based system
- MMU, BPU, MFSR, timers, multi-master arbitration
- TTL-compatible interface
- MIL-STD-883C/38510 Class B and Class S screening options
- Silicon-gate epitaxial two-layer metal LMA9000 HCMOS technology
- Directly interfaces with L64501 CPU
- Available in 144-pin CPGA (ceramic pin grid array) and CLDCC (ceramic leaded chip carrier) packages

Radiation Test Data

SEU and total dose radiation data expected in Q4 89.

Technical Information

Refer to the L64500/64550 MIL-STD-1750A Microprocessor Technical Manual and datasheet, October, 1989.

Ordering Information

L64551 G M 25

- 25 — Part number: Radiation-hardened
- G — Package option: G–144-Pin CPGA (Ceramic Pin Grid Array); L–144-Pin CLDCC (Ceramic Leaded Chip Carrier)
- M — Screening option: M–Class B; S–Class S

LSI LOGIC

SPARC Microprocessors

RISC Products SPARC Architecture Microprocessors and Peripherals

LSI LOGIC

Description

LSI Logic offers a broad range of SPARC-compatible microprocessors and peripherals designed to form the core logic of today's high-performance workstations and embedded control applications.

The SPARC architecture was developed by Sun Microsystems based on RISC (Reduced Instruction Set Computer) research done at the University of California, Berkeley. SPARC stands for Scalable Processor ARChitecture. Because of its relative simplicity, the SPARC architecture will scale well as advancing semiconductor technology allows SPARC processors to be implemented in smaller geometries. This will allow higher operating speeds and proportionally higher performance.

LSI Logic's SPARC product line includes three microprocessors: the L64801 Integer Unit (IU), the L64811 Enhanced Integer Unit (IU) and the L64901 Embedded Processor. The L64801 executes up to 15 MIPS, and the L64811 executes up to 29 MIPS. The L64901 Embedded Processor has been specially optimized for embedded control applications and executes up to 15 MIPS.

All three processors are complemented by peripherals specially designed to support workstation and embedded control applications. The SparKIT-20 supports the L64801 IU and includes the peripherals required to build a SPARCstation 1-compatible workstation. The SparKIT-25, -33 and -40 support the L64811 and provide the functionality required to build a high-performance workstation based on the SPARC standard. The L64901 Embedded Processor is supported by the L64951 System Controller, which contains the cache control, DRAM control and other peripheral logic required to implement embedded control systems.

Features

- Reduced Instruction Set Computer (RISC) architecture
  - SPARC instruction set
  - Simple 32-bit instruction format
  - Large windowed register file

L64801	120 registers	7 windows
L64811	136 registers	8 windows
L64901	120 registers	7 windows

- High Performance
  - Single-cycle execution for most instructions
  - Efficient four-stage instruction pipeline with hardware interlocks
- Multitasking support with user and supervisor modes
- Multiprocessing support with tightly coupled coprocessor interfaces
- Artificial intelligence support using tagged arithmetic instructions
- SunOS operating system based on UNIX 4.3 BSD
- Optimized high-level language compilers: C, FORTRAN, Ada, Pascal, LISP
- Complete peripheral chipsets
  - SparKIT-20 for SPARCstation 1 implementations
  - SparKIT-25, -33 and 40 for high-performance workstation implementations

Components

Family	Product Code	Description	Clock Rates	Packages
SparKIT-20	L64801	Integer Unit	20	160 PQFP, 179 PPGA, 179 CPGA
	L64804	Floating-Point Unit	20	
	L64821	Memory Management Unit	20	
	L64822	Data Buffer	20	
	L64823	Clock Controller	20	
	L64824	Cache Controller	20	
	L64825	Video Controller	20	
	L64826	DRAM Controller	20	

Components
Continued

Family	Product Code	Description	Clock Rates	Packages
SparKIT-25,-33,-40	L64811	Advanced Integer Unit	25, 33, 40	207 PPGA, 207 CPGA
	L64814	Advanced Floating-Point Unit	25, 33, 40	143 PPGA, 143 CPGA
	L64815	Memory Management, Cache Control, and Cache Tag Unit	25, 33, 40	223 CPGA
	L64850	DRAM Controller	25, 33, 40	223 CPGA
	L64851	Standard I/O Interface	25, 33, 40	208 PQFP
	L64852	MBus to SBus Controller	25, 33, 40	223 CPGA
	L64853	SBus DMA Controller	25,	120 PQFP
L64900 Embedded Control	L64901	SPARC Embedded Processor	20, 25	160 PGFP, 144 PPGA
	L64951	System Control Processor	20, 25	160 PQFP, 144 PPGA

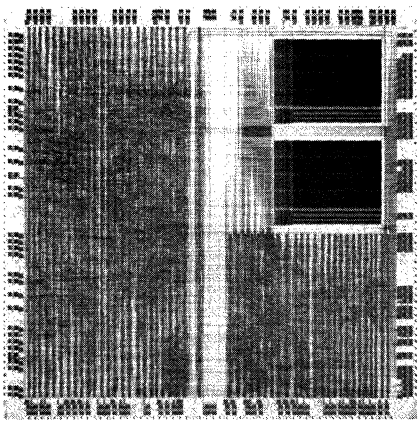
LSI LOGIC

L64801 SPARC Integer Unit (IU)

Description

The L64801 IU (Integer Unit) is a high-performance CMOS implementation of a SPARC (Scalable Processor ARChitecture) 32-bit RISC microprocessor. This integer unit provides the CPU function in Sun's SPARCstation1 and LSI Logic's SparKIT-20 Chipset.

The L64801 features a large register file to optimize procedure calls, variable assignments and context switches. Execution speed improves significantly because this register-to-register architecture minimizes the number of external memory accesses. Most of the L64801 instructions execute in a single cycle due to its 4-stage pipeline that minimizes interlocks, a bus structure that allows single-cycle instruction/data accesses and an optimized branch handler.



L64801 Chip

Features

- High performance operation
  - Commercial
    - L64801C-20 12 VAX MIPS
    - L64801C-25 15 VAX MIPS
  - Military
    - L64801M-15 9 VAX MIPS
    - L64801M-20 12 VAX MIPS
- Open Architecture:
  - Multiple vendor sourced
  - Variety of binary compatible price/performance options
- Optimized for operation under high-level languages such as C, FORTRAN, Pascal, Ada and the UNIX operating system
- External MMU, memory system and floating-point unit assure flexible interface for the largest range of applications and price/performance levels
- 32-bit virtual address bus
  - Supports up to 4 Gbytes of direct address space
  - Allows a variety of memory management and caching schemes
- Simple instruction format with fast instruction cycle with a 4-stage pipeleine
- Single-cycle execution for the majority of instructions
- Large central register file divided into seven overlapping windows of 24 registers each, plus eight global registers
- All pipeline interlocks implemented directly in hardware
- High-performance coprocessor interface for concurrent execution of floating-point or other coprocessor instructions
- Multitasking support with user/supervisor mode and privileged instructions
- Artificial intelligence support through use of tagged instructions
- Option to use as an ASIC core
- 179-pin CPGA or PPGA (ceramic or plastic pin grid array) packages
- 160-pin PQFP (plastic quad flat pack) package

L64804 SPARC Floating-Point Unit (FPU)

Description

The L64804 Floating-Point Unit provides floating-point support for SparKIT-20 systems. The L64804 includes a floating-point datapath and a floating-point controller. The datapath consists of a multiplier, an ALU, a divider/square-root unit and a register file. The register file is a three-port configuration that can be used in either 64-bit-by-16-word or 32-bit-by-32-word configurations. The floating-point controller handles IEEE exceptions and provides an interface between the datapath and both the integer unit and main memory.

Features

- Provides single-chip implementation of floating-point functions
- Includes 64-bit multiplier
- Includes 64-bit ALU
- Includes 64-bit divide/square-root unit
- Includes internal register file
- Interfaces directly to LSI Logic L64801 Integer Unit and Fujitsu's S-20/S-25 Integer Unit
- Interfaces directly to main memory
- Complies with ANSI/IEEE-754 standard for binary floating-point arithmetic

LSI LOGIC

L64821 SPARC Memory Management Unit (MMU)

Description

The L64821 MMU (Memory Management Unit) manages the translation of virtual addresses into physical addresses using a two-level mapping scheme. The mapping scheme supported by the L64821 includes a page map and a segment map. The L64821 also prioritizes interrupt requests generated by external devices and provides a mechanism for software-generated interrupts. The L64821 includes an SBus interface and all signals needed to interface with the other members of the SparKIT-20 chipset.

Features

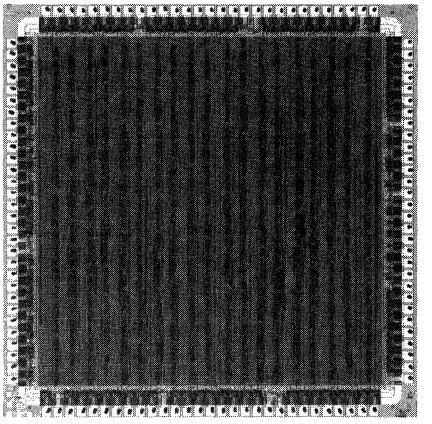
- Manages two-level virtual address translation map
- Provides decoding and timing strobes for all Sun-4 type 1 devices, including:
  - Keyboard
  - Mouse
  - Serial controller chip
  - Time-of-day clock
  - EPROM
  - Floppy disk controller
  - Audio DAC
  - SBus expansion slots
- Prioritizes 15 levels of interrupts
- Replaces all MMU read/write buffers
- Updates MMU statistics bits during bus cycles
- Includes the Sun-4 interrupt register to provide software interrupts and interrupt enabling
- Includes a four-bit context register to support switchable MMU contexts
- Includes two internal counters to generate programmable high-resolution periodic interrupts
- Includes SBus interface signals

LSI LOGIC

L64822 SPARC Data Buffer

Description

The L64822 Data Buffer provides a data interface between the SBus and the main memory in LSI Logic's SparKIT-20 Chipset. The L64822 includes internal read and write buffers. An internal parity checker generator creates parity bits during memory write operations and checks parity during memory read operations. The L64822 generates an SBus error acknowledgment in the case of a parity error. Assembly/disassembly logic interfaces 8-bit I/O devices to the 32-bit IU data bus. The Sun-4 Parity Control Register is located in the L64822.



L64822 Chip

Features

- Generates and checks parity during main memory operations
- Performs buffered write operations in conjunction with L64824 Cache Controller
- Assembles 8-bit I/O data into 32-bit words for IU data bus
- Disassembles 32-bit words into 8-bit data for I/O devices
- Forces NoOp on memory exceptions

LSI LOGIC

L64823 SPARC Clock Controller

Description

The L64823 Clock Controller generates all clocks necessary for a system based on the SparKIT-20 chipset. The L64823 can support either the LSI Logic L64801 Integer Unit or the Fujitsu S-20/S-25 Integer Units. The L64823 also generates various write enable and clock signals.

Features

- Generates all system clocks
- Generates write enables for data/instruction and tag caches
- Generates serial controller clock
- Generates refresh clock and periodic interrupt clock

LSI LOGIC

L64824 SPARC Cache Controller

Description

The L64824 Cache Controller manages the data/instruction and tag caches in a SparKIT-20 system. The data/instruction cache is based on 16-byte lines. The tag cache is based on 20-bit words. The cache size can vary from 4,096 to 16,384 lines deep. The L64824 determines cache hits and misses and initiates cache fill operations as needed. During write operations, the L64824 flushes cache lines as required to ensure system data integrity.

The L64824 also includes an internal SBus controller to manage SBus operations in a SparKIT-20 system. Standard SBus operations including bus requests and grants, bus timeouts, bus arbitration and rerun initiation are controlled by the L64824. The L64824 also performs byte-to-word assembly operations so that byte-wide devices such as EPROMs and peripherals can communicate with the L64801 Integer Unit. Upon receipt of a reset signal from the IU, the L64824 generates an SBus reset signal.

Features

- Implements write-through instruction/data cache with 16-byte line size
- Supports cache size from 64 Kbytes to 256 Kbytes
- Controls all cache operations, including:
  - Fills on cache misses
  - Flushes on cache writes
  - Tag comparison
- Performs SBus controller functions, including:
  - SBus reads and writes
  - Bus master requests and grants
  - Bus monitoring for unacknowledged transfers
- Performs buffered writes with external write buffer
- Assembles data from byte-wide devices into 32-bit words for IU
- Contains set of four Sun-4 error registers for diagnosing bus errors
- Maintains copy of Sun-4 context register
- Contains Sun-4 system enable register
- Generates system reset

LSI LOGIC

L64825 SBus Video Controller

Description

The L64825 Video Controller generates the signals needed to control the video RAM and the external DACs that drive the video display. The L64825 also includes an SBus interface. Key parameters of the video display, including video timing and resolution, are software programmable. The L64825 supports the Sun auto configuration feature.

Features

- Provides a single-chip video subsystem
- Interfaces to SBus
- Software control of video timing and display resolution
- Supports 256-by-4, 128K-by-8 and 64K-by-4 video RAMs
- Supports 1-, 8- and 24-bit-per-pixel frame buffers
- Supports up to four video clocks
- Includes built-in video shifter for 1-bit frame buffers (maximum pixel clock up to 100 MHz)
- Supports Sun Video Monitor sense lines for auto configuration
- Interfaces directly to VRAM and video DACs with no external components

LSI LOGIC

L64826 SBus DRAM Controller

Description

The L64826 DRAM Controller handles all address handling, RAS and CAS decoding and control for a memory system of four or eight SIMM memory modules. The L64826 includes two sets of output buffers, each driving a group of four SIMMs. The L64826 supports 1-Mbit and 4-Mbit SIMMs. Up to four L64826s can be connected in banks to support a maximum memory configuration of 32 SIMMs.

Features

- Supports 1M- and 4M-DRAM SIMMs
- Drives up to eight SIMMs with no external buffers
- Can be combined with other L64826s to drive up to 32 SIMMs for a maximum memory size of 128 Mbytes
- Supports high-speed burst mode with fast-page RAMs
- Contains refresh logic and timer

L64811 SPARC Enhanced Integer Unit (IU)

Description

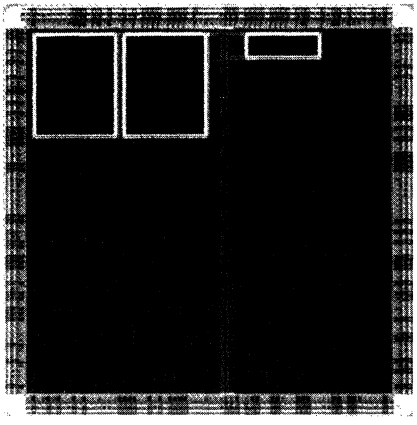
The L64811 Enhanced IU (Integer Unit) is a high-speed CMOS implementation of the SPARC 32-bit RISC (Reduced Instruction Set Computer) architecture processor. This architecture specifies a processor which can execute instructions at a rate approaching one instruction per processor clock and which supports both a tightly coupled floating-point unit and an implementation-definable coprocessor. The L64811 IU provides:

Simple Instruction Format
All instructions are 32 bits wide and aligned on 32-bit boundaries in memory. There are only three basic instruction formats, featuring uniform placement of opcode and address fields.

Register-Intensive Architecture
Most instructions operate on the contents of two registers and place the results in a third register. Only load and store instructions access off-chip memory.

Delayed Control Transfer
The IU always fetches the instruction which follows a control transfer instruction, and either executes it or annuls it depending on the state of a bit in the control transfer instruction. This feature allows compilers to rearrange code and place a useful instruction after a delayed control transfer, for optimal use of the processor pipeline.

Concurrent Floating-Point Operation
Floating-point instructions can execute concurrently with non-floating-point instructions, other floating-point instructions and co-processor instructions.



L64811 Chip

Fast Interrupt Response
The IU samples the interrupt inputs on every clock cycle and can acknowledge them in one to three cycles. The IU can access the first instruction of an interrupt service routine within six to eight cycles of receiving the interrupt request.

The L64811 IU is part of the LSI Logic L64811 Chip Family which implements and supports SPARC-based system development.

Features

- RISC architecture - Simple instruction format, most instructions execute in a single cycle
- Very high performance - Four-stage pipeline has a 25 ns instruction cycle at 40 MHz
- 29 million instructions per second (29 MIPS)
- Large windowed register file - 136 general-purpose 32-bit registers organized as 8 overlapping windows of 24 registers each
- 32-bit address bus and 8-bit address space identifier (ASI) support large virtual address space
- Hardware pipeline interlocks
- Multiprocessing support
- User/supervisor modes
- Artificial intelligence support
- High-performance floating-point and coprocessor interfaces support concurrent execution of floating-point and coprocessor instructions
- 1.0-micron drawn gate length 2-layer metal CMOS technology
- 207-pin CPGA or PPGA (ceramic or plastic pin grid array) packages
- 2.5 watts maximum power dissipation

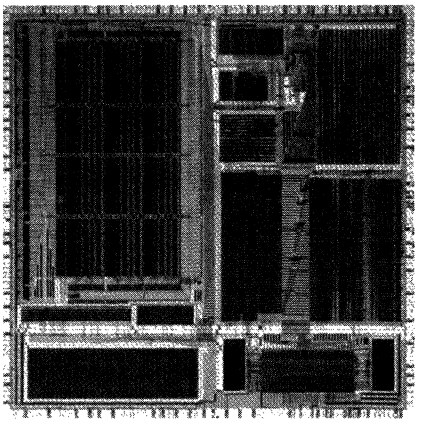
L64814 SPARC Enhanced Floating-Point Unit (FPU)

Description

The L64814 Enhanced FPU (Floating-Point Unit) is a high-performance, CMOS implementation of the SPARC (Scalable Processor ARChitecture) FPU. The FPU combines a floating-point controller with a high-throughput floating-point processor to provide a single-chip floating-point solution for SPARC-based systems.

The FPU implements the IEEE 754-1985 standard for floating-point arithmetic. It operates concurrently with the IU to execute single- and double-precision floating-point operations, as well as register-to-register move instructions, floating-point loads and stores, and floating-point queue and state register instructions. Supported floating-point operations are: add, subtract, multiply, divide, square root, compare, and convert. Each instruction not implemented in the L64814 hardware generates an instruction trap, so that the instruction can be emulated in software. Note that the FPU handles all IEEE exceptions in hardware, except for denormals in the floating-point multiplier unit.

The L64814 FPU is part of the LSI Logic SparKIT Chipset Family which implements and supports SPARC-based system development.



L64814 Chip

Features

- High-performance operation provides double-precision Linpack floating-point operation (assuming 25% degradation due to cache misses) at:

Device	Performance
L64814-25 MHz	3.04 MFlops
L64814-33 MHz	4.00 MFlops
L64814-40 MHz	4.80 MFlops

- Low-cost solution integrates a floating-point controller and floating-point processor on a single chip for cost-efficient system implementation
- Wide range of operating frequencies including 25/33/40 MHz versions
- Implements IEEE exception handling directly in hardware
- 64-bit wide internal datapath for all floating-point operations results in highly efficient double-precision performance
- Connects directly to the L64811 Integer Unit (IU)
- Pin-compatible with the Weitek Abacus 3171 and Texas Instruments TMS390C602 floating-point units
- Advanced, 143-pin cavity-up PPGA or CPGA (plastic or ceramic pin grid array) package

L64815 SPARC Memory Management, Cache Control and Cache Tag Unit

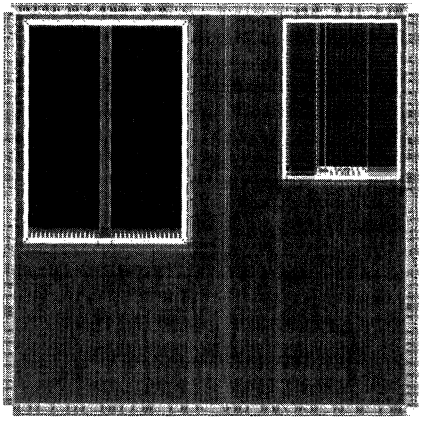
LSI LOGIC

Description

The L64815 MCT (Memory Management, Cache Control, and Cache Tag Unit) provides two essential functions for SPARC (Scalable Processor ARChitecture) CPU Cores - memory management and cache control. The MCT's memory management function implements the SPARC Reference MMU (Memory Management Unit). The Cache Controller manages a direct-mapped, combined instruction and data cache. In addition, the MCT provides an interface between the 32-bit Local Bus and the 64-bit Mbus.

The L64815 MCT is made by LSI Logic using 1.0-micron drawn gate length (0.7-micron effective channel length), silicon gate HCMOS technology.

The MCT is a member of LSI Logic's SparKIT Chipset Family which implements and supports SPARC-based system development.



L64815 Chip

Features

The memory management unit of the L64815:

- Incorporates a 64-entry, fully associative TLB (Translation Lookaside Buffer)
- Uses Least Recently Used (LRU) replacement algorithm for the TLB
- Uses 4096-byte or greater page size
- Supports three-level page mapping
- Supports sparse address spaces
- Supports large linear mappings
- Supports 256 contexts
- Provides page-level protection
- Performs 32-bit virtual to 36-bit physical address translation

The write-through, no-allocate cache controller of the L64815:

- Provides 2048 virtual address cache tags
- Provides 32-byte block size
- Provides hardware-miss processing
- Includes 32-byte Line Buffer
- Supports cache sizes of 32, 64, 128 and 256 Kbytes
- Supports line-by-line cache freezing

In addition, the L64815:

- Supports 25/33/40 MHz operation
- Uses 64-bit Mbus as its main memory interface
- Is available in 223-pin CPGA (ceramic pin grid array) package
- Provides Block Fill capability
- Provides Block Copy capability

The MCT in the SPARC CPU Core

The MCT is part of a high-performance, general-purpose, reprogrammable computer based on Sun Microsystems' SPARC. Such a computer requires three main components: a CPU Core, main memory, and an input/output (I/O) subsystem. A SPARC CPU Core consists of the following elements: a SPARC-compatible IU (Integer Unit), an FPU (Floating-Point Unit), an MMU (Memory Management Unit) and a cache. These elements provide data, integer and floating-point arithmetic processing power and the flexible, fast memory management required to support multiple processes running simultaneously from a large physical memory.

L64850 Mbus DRAM Controller

Introduction

The L64850 DMC (DRAM Controller) is a high-performance CMOS integrated circuit that provides a direct interface between an Mbus and a DRAM array in a SPARC-based system. The L64850 provides single-chip control for high-performance, low-cost memory systems, and supports 4M x 9, 4M x 8, 1M x 9, and 1M x 8 SIMMS and 4M x 1 and 1M x 1 DRAMs.

Features

- Supports up to 4 Gbytes of DRAM address space
- One- to 128-byte burst mode Mbus transactions
- Even or odd parity generation and checking with disable option
- Parity error address register
- Staggered $\overline{CAS}$ before $\overline{RAS}$ refresh for dual-bank memory systems
- Mbus level 1 and 2 operations
- Built-in scan chain to provide 99.97% fault coverage test vector
- Advanced 223-pin CPGA (ceramic pin grid array) package
- Supports 100 ns - 70 ns DRAMs

System Diagram

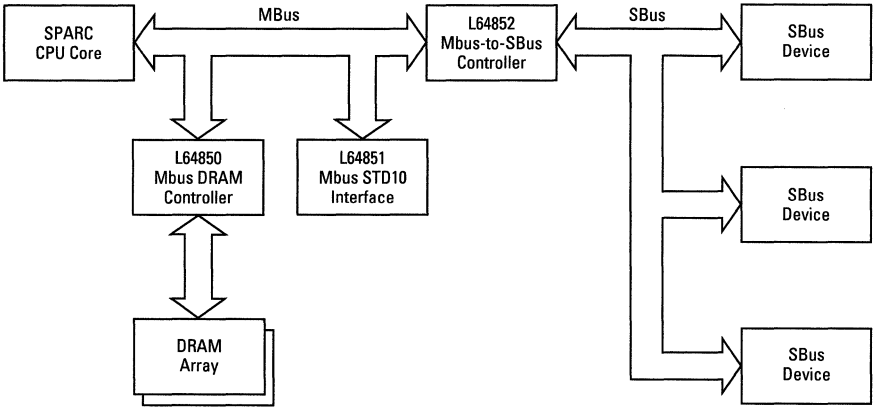
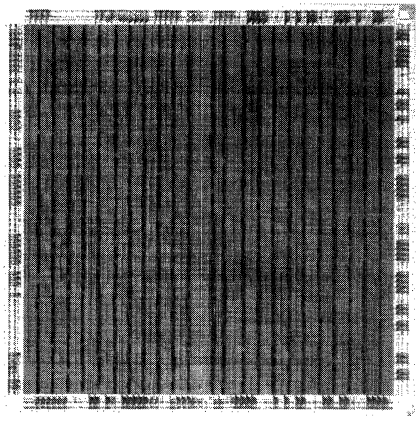


Figure 1. Typical SPARC-based System

L64851
Mbus to Standard I/O Bus Interface

Introduction

The L64851 M2STDIO (Mbus to Standard I/O Bus Interface) is a high-performance CMOS interface chip that interfaces an Mbus and a STDIO (standard, 8-bit I/O) bus . As an Mbus interface to I/O devices, the L64851 M2STDIO accepts requests for I/O service from an Mbus master, converts them to I/O bus protocol and redirects them to a designated device on the I/O bus. In addition to the the Mbus interface, the L64851 provides three other Mbus functional modules: a four-level Mbus arbiter, a watch dog timer that generates Mbus Time Out and an interrupt level encoder that generates the interrupt request levels for the SPARC IU (Integer Unit). These three additional modules allow the L64851 to be used in systems that do not have an M2S chip.



L64851 Chip

Features

- Supports Mbus access to eight I/O devices on a standard, 8-bit bus
- Data packing for full use of Mbus bandwidth
- Accesses 1 Mbyte of I/O address space per device
- Programmable latency delays for I/O devices
- One- to 128-byte Mbus burst transfer capability
- Mbus Arbiter supports up to four Mbus masters
- Mbus watch dog timer times out bus masters 8000 (2^{13}) clock cycles after assertion of $\overline{MBB}$
- 15-level IU Interrupt Level Encoder supports 13 external devices and two internal, programmable timers
- IRL[7:1] can be generated in hardware (external devices), software (interrupt bits 7:1) or both through IU device polling
- Maskable interrupts, except for IRL15
- 25, 33, and 40 MHz system clock speed
- 5 MHz clock for SCC timing
- Advanced, 208-pin, square gull-wing PQFP (plastic quad flat pack) package

System Diagram

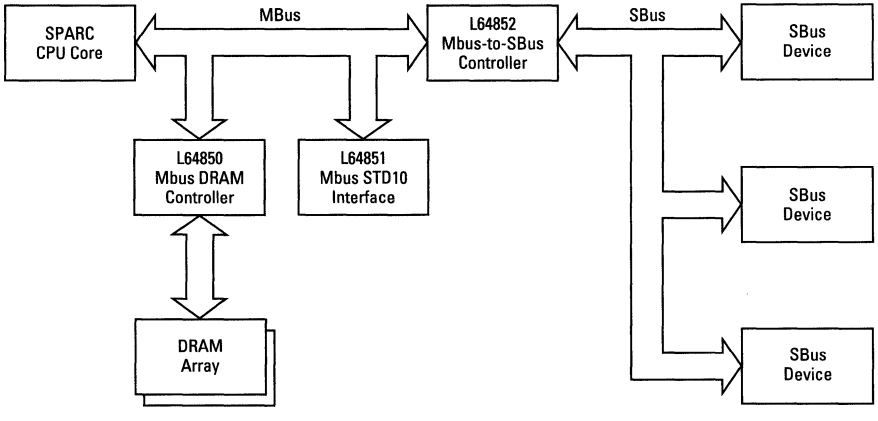


Figure 1. Typical SPARC-based System

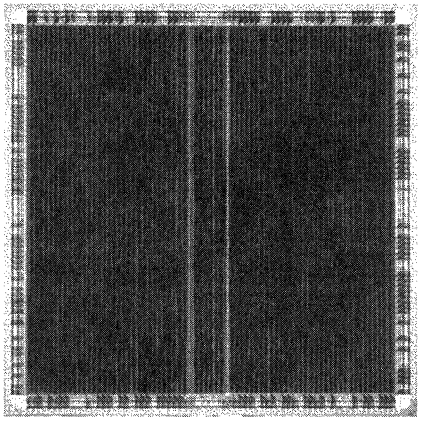
L64852
Mbus-to-SBus Controller

Introduction

The L64852 M2S (Mbus-to-SBus) Controller is a high-performance CMOS integrated circuit that provides all the control, arbitration and memory-management functions needed to interface Mbus and SBus subsystems.

The M2S acts as an intermediary while moving data between Mbus and SBus devices, instead of transferring control of one bus to the other bus. When an Mbus device initiates a read from or write to an SBus device, the M2S chip responds as an Mbus slave and then becomes the SBus master for the data transfer. Conversely, when an SBus device initiates a data access to the Mbus, the M2S chip responds as an SBus slave and becomes the Mbus master.

The M2S contains an Mbus arbiter to control Mbus access and an SBus controller. The SBus controller contains both an SBus arbiter to control SBus access and an I/O MMU (input/output memory-management unit). The I/O MMU, which supports the SBus virtual addressing scheme, includes a 16-entry TLB



L64852 Chip

(Translation Lookaside Buffer) and virtual-to-physical address calculation logic. The M2S also contains low-level protection and diagnostic logic for the two bus subsystems.

Features

- Provides complete Mbus and SBus master/slave logic
- Supports arbitration for up to four Mbus masters, including itself
- Manages SBus transactions and supports arbitration for up to six SBus master/slave devices
- Incorporates a 16-entry fully-associative TLB (Translation Lookaside Buffer) in the I/O MMU
- Uses the LRU (Least-Recently-Used) replacement algorithm in TLB
- Performs 32-bit virtual SBus to 36-bit physical Mbus address translation
- Performs 32-bit virtual SBus to 28-bit physical SBus address translation and SBus slave device selection using table walking logic
- Provides two sets of internal data buffers for data transfer
- Performs bus protocol conversion
- Tracks internal status and generates error and busy signals
- Stores system and bus error information in a readable error register
- Advanced 223-pin CPGA (ceramic pin grid array) package

L64853 SBus DMA Controller

Description

The L64853 SBus DMA (Direct Memory Access) Controller by LSI Logic provides a complete SBus interface for SBus peripheral subsystems. The L64853 is a high-speed, low-power, dual-port device. It provides Master/Slave-type peripherals with a single-chip solution for interfacing to the SBus. The principal components of the L64853 are two functionally distinct DMA channels (an 8-bit and 16-bit channel) and an SBus interface with associated bus arbitration logic.

The L64853 is ideal for both master and slave peripherals as it operates either in master mode or in slave mode. As an SBus master, the L64853 generates, upon request from a device attached to either channel, sequences of SBus data transfers (reads or writes) between the peripheral controller and main memory. In SBus terminology, the L64853 is a DVMA (Direct Virtual Memory Access) Master, that is, it generates virtual addresses on the SBus data lines and employs the SBus controller's MMU (Memory Management Unit) to translate these virtual addresses into physical addresses.

When the L64853 is an SBus slave, software reads and writes the internal registers on the L64853 and also on the two peripheral controllers. The CPU uses the L64853 as a conduit to access the two peripheral controller chips.

The DMA Controller operates at a maximum clock frequency of 25 MHz. The L64853 is implemented in a 1.5-micron CMOS process and is packaged in an inexpensive, 120-pin, plastic quad flat package (PQFP).

Features

- Operation at clock frequencies up to 25 MHz
- Packing/unpacking of SBus words into bytes or halfwords for use by the peripheral controllers
- Support for 8- or 16-bit peripherals
- Supports byte, halfword, or word transfers on the SBus
- Operation in virtual address space with the SPARC MMU providing virtual-to-physical address translations
- Support for rerun acknowledgments
- Inclusion of 24-bit address and data counters
- Packaged in a low-cost, 120-pin PQFP (plastic quad flat pack) package

L64853A SBus Direct Memory Access (DMA) Controller

LSI LOGIC

Description

The L64853A SBus DMA (Direct Memory Access) Controller is a high-speed, low-power, dual-port device that provides a complete SBus interface solution for SBus peripheral subsystems. The principal components of the L64853A are its two functionally distinct DMA channels and its SBus interface with associated bus arbitration logic.

The L64853A supports both 8- and 16-bit peripherals through two independent DMA channels, a 16-bit channel and an 8-bit channel. The L64853A is ideal for both master and slave peripherals as it operates either in master mode or in slave mode.

During SBus DMA transfers, the L64853A packs the data into one of two 32-byte caches for optimum bus performance. The SBus DMA Controller supports concurrent 5 MByte/sec SCSI and 1.25 MByte/sec Ethernet transfers. The L64853A is pin and software compatible with the L64853 SBus DMA Controller. The L64853A provides additional features over the L64853 such as support for 4-word SBus bursts and data block chaining.
The L64853A operates at clock frequencies of up to 25 MHz. The L64853A is implemented in a 1.5-micron CMOS process and is packaged in an inexpensive, 120-pin, plastic quad flat package (PQFP).

Features

- Operation at clock frequencies up to 25 MHz
- Support for 8- or 16-bit peripherals
- Support for byte, halfword or word transfers on the SBus
- Operation in virtual address space with the SPARC MMU providing logical-to-physical address translations
- Support for rerun acknowledgments
- Inclusion of 24-bit address and data counters
- Inclusion of two 32-byte caches for data transfers
- Four-word burst operation
- Data block chaining
- Packaging in a low-cost, 120-pin PQFP (plastic quad flat pack) package
- Pin and software compatible with the L64853 SBus DMA Controller

LSI LOGIC

L64855 SBus Video Frame Buffer

Description

The L64855 Video Controller generates the signals needed to control the video RAM and the external DACs that drive the video display. The L64855 also includes an SBus interface. Key parameters of the video display, including video timing and resolution, are software programmable. The L64855 supports the Sun auto configuration feature.

Features

- Provides a single-chip video subsystem
- Interfaces to SBus
- Software control of video timing and display resolution
- Supports 256-by-4, 128K-by-8 and 64K-by-4 video RAMs
- Supports 1-, 8- and 24-bit-per-pixel frame buffers
- Supports up to four video clocks
- Includes built-in video shifter for 1-bit frame buffers (maximum pixel clock up to 100 MHz)
- Supports Sun Video Monitor sense lines for auto configuration
- Interfaces directly to VRAM and video DACs with no external components

LSI LOGIC

L64901 SPARC Embedded Processor
Preliminary

Description

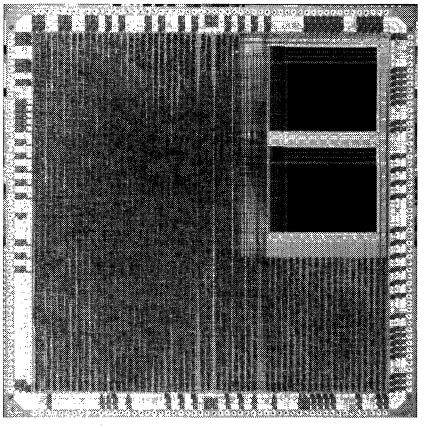
The L64901 SPARC Embedded Processor is a high- speed implementation of the SPARC 32-bit RISC architecture, and it is fabricated by LSI Logic in a 1.5-micron drawn gate length (0.9-micron effective channel length) CMOS process. The L64901 processor provides:

Simple Instruction Format
All instructions are 32 bits wide and aligned on word boundaries in memory. There are only three basic instruction formats, which feature uniform placement of opcode and other fields.

Register Intensive Architecture
Most instructions operate on the contents of two registers and place the results in a third register. Only Load and Store instructions access off-chip memory.

Delayed Control Transfer
The L64901 always fetches the instruction which follows a control transfer instruction, and either executes it or annuls it depending on the state of a bit in the control transfer instruction. This feature allows compilers to rearrange code to place a useful instruction after conditional branches, for optimal use of the processor pipeline.

Fast Interrupt Response
The L64901 processor can access the first instruction of an interrupt service routine within three to six cycles of receiving the interrupt request.



L64901 Chip

ASIC Implementation
The L64901 processor is implemented in LSI Logic's advanced sub-micron HCMOS process, which offers up to 200,000 usable gates on a single integrated circuit. LSI Logic's ASIC methodology facilitates modifications to the processor and provides users the ability to increase system integration or to reduce system cost.

The L64901 is part of LSI Logic's L64900 Embedded Processor Family for SPARC-based systems.

Features

- SPARC RISC (Reduced Instruction Set Computer) Architecture
- Simple instruction format
- Simple 1x clock input
- Most instructions execute in a single cycle
- Low cost
- 4-stage pipeline
- Large windowed register file
- 120 general-purpose 32-bit registers
- 7 overlapping windows of 24 registers each
- Hardware pipeline interlocks
- Separate 32-bit address and data buses
- User/supervisor modes
- Privileged instructions
- Artificial intelligence support
- 1.5-micron gate length, 2-layer metal CMOS technology
- 160-pin PQFP (plastic quad flat pack) and 144-pin PPGA (plastic pin grid array) packages
- 0.8 Watts maximum power dissipation
- Available in 20 or 25 MHz versions

LSI LOGIC

L64951 Integrated System Controller
Preliminary

Description

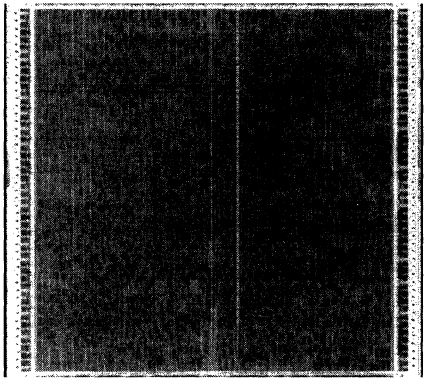
The L64951 Integrated System Controller (ISC) is a member of the L64900 Family of Embedded Solutions. Manufactured in LSI Logic's advanced 1.5-micron drawn gate length HCMOS process, the ISC provides memory control, address decode and other support services for the L64901 SPARC Embedded Processor, a 32-bit implementation of the SPARC RISC architecture. Designers can use the L64901 and the L64951 to build a low-chip-count, high-performance embedded processor core.

The ISC includes a host of features that make the implementation of a processor core straightforward. In addition to a variety of glue logic, the ISC includes the five major features described below.

The ISC includes a **DRAM controller** that can control up to four banks of DRAMs. The address range for each bank is programmable. The DRAM controller also includes refresh logic.

The ISC provides eight **chip selects** to control SRAMs, EPROMs, and I/O devices. The address range and control signal timing for each chip select are programmable.

The ISC includes an **interrupt controller** that prioritizes and encodes eight external interrupt lines and two internal interrupt sources. Interrupts can be individually masked or masked by priority.



L64951 Chip

The ISC provides three **DMA channels**, two for use by I/O devices and one for block transfers by the processor. These DMA channels allow large blocks of data to be transferred between I/O devices and memory with minimal processor involvement. The two I/O DMA channels generate interrupts when a transfer is complete. The interrupt levels are programmable.

The ISC includes **cache control** logic that allows construction of a high-performance cache memory.

The ISC provides eight **protection registers** to permit or prohibit access to blocks of memory. These protection registers can also be used to set breakpoints to ease software debug.

Features

In addition to the major functions described above, the ISC provides many of the glue logic functions that are required to complete a processor core. Those functions are included in this list of features:

- DRAM control with programmable address decoders for up to four banks of DRAMs
- Eight chip selects with programmable address decoders and control signal timing for SRAM, EPROM and I/O control
- Interrupt control for eight external and two internal interrupts
- Three DMA channels with programmable interrupt levels
- Programmable memory protection and debug breakpoints
- Data bus buffer control signals
- Reset logic
- Processor bus request and acknowledge signals for I/O devices
- Low-cost 160-pin PQFP (plastic quad flat pack) package and 144-pin PPGA (plastic pin grid array) package
- 20 MHz operating speed

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LSI Logic Corporation of Canada, Inc. Headquarters
■ Petro-Canada Centre, Ste., 3410
150 6th Avenue SW
Calgary AB T2P 3Y7
Tel: 403.262.9292
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Netherlands
LSI Logic/Arcobel
■ Griekenweg 25
Postbox 344
NL-5340 AH Oss
Tel: 31.4120.30335
TWX: 37489
FAX: 31.4120.30635

Scotland
LSI Logic Limited
■ Lomond House
Beveridge Square
Livingstone EH 54 6QF
Tel: 44.506.416767
FAX: 44.506.414836

Sweden
LSI Logic Export AB
TorShamnsgatan 39
S-16440 Kista
Tel: 46.8.703.4680
FAX: 46.8.7506647

Switzerland
LSI Logic Sulzer AG
■ Erlenstrasse 36
CH-2555 Brugg/Biel
Tel: 41.32.536363
FAX: 41.32.536367

Taiwan
LSI Logic Corporation
■ 3F2, 678 Tun-Hua S. Rd
Taipei, Taiwan R.O.C.
Tel: 886.2.755.3433
FAX: 886.2.755.5176

United Kingdom
LSI Logic Limited
Headquarters
■ 1 Maidstone Road
Sidcup, Kent
DA14 5HU
Tel: 44.81.302.8282
FAX: 44.81.300.0116

■ Grenville Place, The Ring
Bracknell
Berkshire RG12 1BP
Tel: 44.344.426544
Telex: 848679
FAX: 44.344.481039

West Germany
LSI Logic GMBH
Headquarters
■ Arabellastrasse 33
8000 Munich 81
Tel: 49.89.9269030
FAX: 49.89.917096

■ Niederkasseler AM
Seestern, Lohweg 8
4000 Dusseldorf 11
Tel: 49.211.5961066
TWX: 8587248
FAX: 49.211.592130

■ Buechsenstrasse 15
7000 Stuttgart 1
Tel: 49.711.2262151
TWX: 723813
Tel: 49.711.2261124

AE Advanced Electronics
■ Theaterstr. 14
3000 Hannover 1
Tel: 49.511.3681756
FAX: 49.511.3681759

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LSI LOGIC

LSI Logic
Corporation
Milpitas CA
408.433.8000

LSI Logic
Corporation
of Canada, Inc.
Calgary
403.262.9292

Japan
LSI Logic K.K.
Tokyo
81.33.589.2711

United Kingdom
LSI Logic Limited
Sidcup
44.81.302.8282

West Germany
LSI Logic GmbH
Munich
49.89.926903.0

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