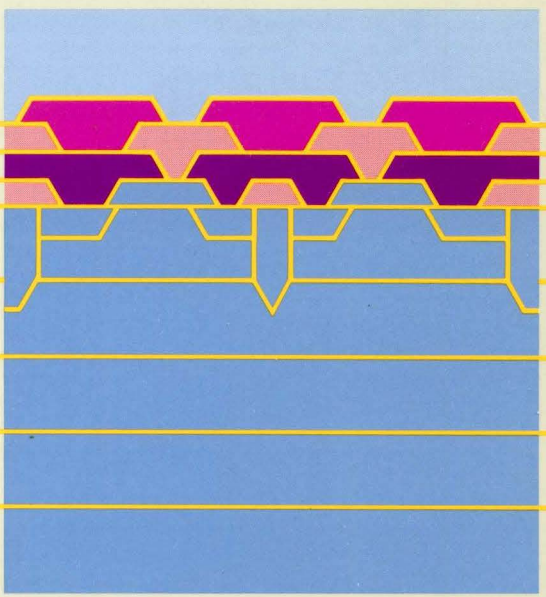
LSI LOGIC CORPORATION

CMOS Macrocell Manual

July 1985



Prepared by the Application Design Engineering Department

LSI LOGIC CORPORATION CMOS Macrocell Manual July 1985

CMOS MACROCELL MANUAL

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Preface

This CMOS Macrocell Manual is written for logic and system designers who wish to use CMOS Logic Arrays from LSI Logic Corporation. It provides circuit, logic, and specifications of available macrocell-macrofunctions.

Second Edition (July 1985)

This edition, AR50-000001-20 D, is the fourth release of this manual. The material supersedes the CMOS Macrocell and Macrofunction Library, Revisions 1 through 5, published in 1982 and 1983.

Publications are stocked at the address given below. Requests should be addressed to:

LSI Logic Corporation
1551 McCarthy Boulevard
Milpitas, CA 95035
Telex 172 153

Figures

Tables

I.1 Using the Guide

This introduction lists all the logic functions available for LSI Logic Corporation CMOS and HCMOS Logic Arrays. Additional, special-purpose functions may be available. Contact your LSI Logic representative for specific requirements.

If a clear direct (CD) or set direct (SD) is used,this is noted. Logic complexity (GATES) is listed: if two numbers are used the first corresponds to single-layer (3000 Series), and the second to two-layer (5000 and 7000 Series) technologies.

For more detail, see specific logic diagrams on the pages noted.

I.2 Macrocells

I.3 Macrofunctions

1.1 Design Process Sequence Overview

This macrocell manual is one of two documents needed to design an LSI Logic gate array. The second document, The LSI Logic LDS Design Manual, is a detailed treatment of the methodology necessary to build a circuit using the LDS software tools. (The Design Manual is provided to designers attending the LSI Logic Design Class.) The macrocell manual is primarily a catalog detailing the libraries of logic functions available for implementation in LSI LOGIC gate arrays. It also serves as a preliminary overview of the complete design process, with emphasis on its initial steps. This manual enables you to complete steps 1, 3, 4, 6, and 8 below. Steps printed in capitals are formal milestones, and require the signatures of both the designer and an LSI Logic applications engineer.

You may want to perform some of the steps in an order different from the one outlined in this manual. You may, for example, need to design your circuit for a particular package. In that case, you would change the order of the steps outlined below. The lessons you learn in an LSI Logic Design Class will enable you to design your circuit with maximum efficiency.

The sequence of initial steps is:

1. Read Background Information to become familiar with LSI LOGIC design concepts.

2. Become familiar with circuit specification forms and formal milestone documents. (These are detailed in Part II, the Design Manual.)

3. Choose an array series.

4. Choose a device, i.e., choose an array size.

5. Optimize the design, if necessary.

6. Select a package.

7. Prepare a bonding diagram.

8. Make power calculations.

9. Be sure you have designed testability and reliability into your circuit.

10. Prepare test patterns.

The remaining steps, which are explained in the LSI LOGIC LDS Design Manual, are as follows:

11. Create a network of interconnects.

12. Execute VERIFY on top-level module to simulate delay values and functional results.

13. Modify network, if necessary.

14. Simulate top-level module.

15. COMPLETE DESIGN ACCEPTANCE CHECKLIST, only if you purchased either the Software Data Book or the Design Verifier Software. For these products the checklist is the first formal milestone document.

16. Perform detectable fault simulation.

17. Execute test patterns extraction program.

18. Complete ac test form.

19. COMPLETE ENGINEERING COMPLETION REPORT. THIS FORM CONSTITUTES THE FIRST FORMAL MILESTONE DOCUMENT.

20. AFTER LAYOUT, COMPLETE PERFORMANCE APPROVAL, THE SECOND FORMAL MILESTONE DOCUMENT.

21. AFTER FABRICATION, COMPLETE PROTOTYPE APPROVAL, THE THIRD AND LAST MILESTONE DOCUMENT.

Formal Milestone Documents -- Steps 15, 19, 20,and 21 above are formal milestones; as such, they require the signatures of both the designer and an LSI LOGIC engineer to establish that both have approved the circuit at that "milestone" stage of its design. Step 15 is not required, unless you purchased either the Software Data Book or the Design Verifier Software.

1.2 System Environment

Table 1.1 illustrates the order in which each task will be performed, depending upon the environment in which you are working.

If you are using LSI's Mainframe LDS System	If you purchased the Software Data Book	If you purchased the Software Data Book and Design Verifier Software
Complete steps 1-10, 20, and 21 at your desk. Complete steps 11-14 and 16-19 on the LDS System. Do not perform step 15.	Complete steps 1-10, 15, 20, and 21 at your desk. Complete steps 11,13, and 14 on the work-station. Complete steps 16-19 on the LDS System. Do not perform step 12.	Complete steps 1-10, 15, 20, and 21 at your desk. Complete steps 11-14 on the workstation. Complete steps 16-19 on the LDS System.

Table 1.1
Design Tasks Related to Working Environment

1.3 Background Information

As a logic designer, you are undoubtedly familiar with traditional electronic circuit-design techniques which make use of standard parts from vendor catalogs. Your knowledge of these techniques will help you in learning to design LSI LOGIC gate arrays.

There are three series of arrays to choose from:

- 3000 Series
- 5000 Series
- 7000 Series

The array series differ in:

- Speed
- Number of gates
- Number of I/O and power pads
- Package requirements

LSI LOGIC software products allow you to design complex circuits by starting with a functional block diagram and continuing through a logical sequence to the final tested product. To help you understand LSI LOGIC's design concept, this section presents background information about:

- CMOS Circuit Structure
- Gate Array Structure
- Traditional Circuit Design vs. Gate Array Design
- Macrocells
- Macrofunctions
- Equivalent Gates
- Macrocell Models

CMOS Circuit Structure -- LSI LOGIC's circuit structure uses Complementary Metal Oxide Semiconductor (CMOS) technology. This technology is made up of N and P channel MOSFET transistors whose switching operation is "complementary"; that is, when the N transistor is on, the P transistor is off, and vice versa.

Figure 1.1 is a cross-sectional view of a two-layer metal array. A P MOSFET transistor is formed directly on the N- substrate. An N MOSFET transistor is formed in the P- well. First layer metal contacts form connections to the N+ and P+ areas. First layer metal contacts also form connections to polysilicon (this connection is not shown in the figure). The second layer metal (2nd metal in the figure) connects to the first layer metal through via contacts.

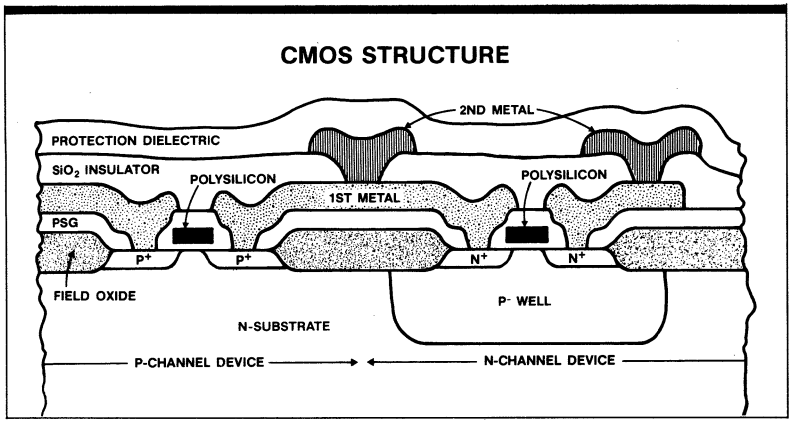


Figure 1.1
A Cross-Sectional View of a Two-Layer Metal Array

Two familiar components, an inverter and a two-input NAND gate, illustrate CMOS circuit operation. An inverter is shown in Figure 1.2.

To construct a CMOS inverter, a P MOSFET is connected between VDD (+5V) and the inverter's output. An N MOSFET is connected between the output and VSS(0V). The gates of both MOSFETs are connected both to the input and to one another, as depicted in Figure 1.2.

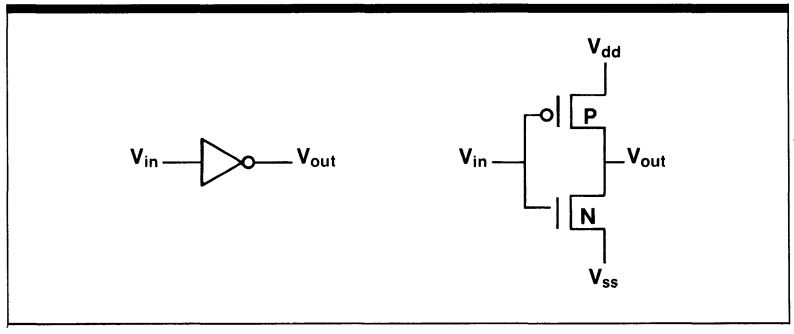


Figure 1.2
A CMOS Inverter

When Vin is low, the P MOSFET is ON, the N MOSFET is OFF, and Vout is pulled close to VDD (Vout=5v). When Vin is high, the P MOSFET is OFF, the N MOSFET is ON, and Vout is pulled close to VSS (Vout=0v). Table 1.2 illustrates these actions.

Vin	P MOSFET	N MOSFET	Vout
0	ON	OFF	1
1	OFF	ON	0

Table 1.2
CMOS Inverter Operation

For a brief time during input voltage transition, both MOSFETs are ON. However, since at least one MOSFET is off when the inverter is in one of its stable states, very little dc current flows through the inverter, and very little power is consumed.

By adding two more transistors to the inverter diagram in Figure 1.2 (indicated by the dotted lines in Figure 1.3) and making minor wire modifications, we can create a two-input NAND gate; one of the basic components used by LSI LOGIC.

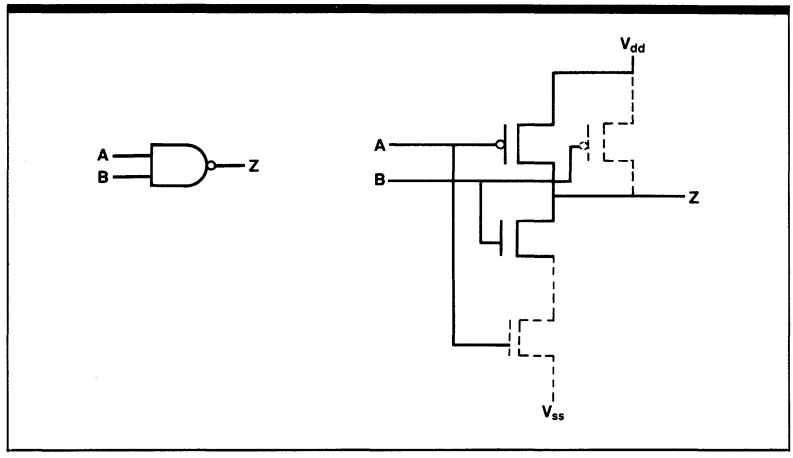


Figure 1.3
A Two-input NAND

In Figure 1.3, when both inputs are high, both N transistors are ON, both P transistors are OFF, and the output is low. If either input is low, then at least one of the P transistors is ON, and at least one of the N transistors is OFF and the output is high. The effect of high and low input states on a two-input NAND gate is shown in Table 1.3.

INPUT	N TRANSISTORS	P TRANSISTORS	OUTPUT
Both 1	Both On	Both Off	0
Either 0	One or More On	One or More Off	1

Table 1.3
Effect of High and Low States
on a Two-Input NAND

Gate Array Structure -- The basic LSI LOGIC circuit structure is an array composed of N and P transistors. It is known as a gate array, a logic array, a ULA, or a masterslice. The term "gate array" is somewhat misleading, since the base array is not an array of gates, but an array of components (N and P transistors) which may be interconnected to form inverters, NAND gates, NOR gates, flip-flops, or other types of circuitry. Because its components are standardized, the array can be produced in high volume at low cost. All that you supply is the configuration of your metal interconnections: these define your logic.

LSI LOGIC's CMOS arrays are structured in columns of gates, known as "diffusion columns." Each gate location, called a "slot," consists of two pairs of N and P transistors. There is enough space to route three horizontal wires across each slot. The slots are stacked to form columns, i.e., the sum of all slots in a given axis is a column.

The diffusion columns are separated by blank silicon columns, which are used for vertical wire routing. In each blank column there are, depending on the array series, 12-26 wiring tracks available for global vertical wire-routing. Figure 1.4 shows an unconnected array.

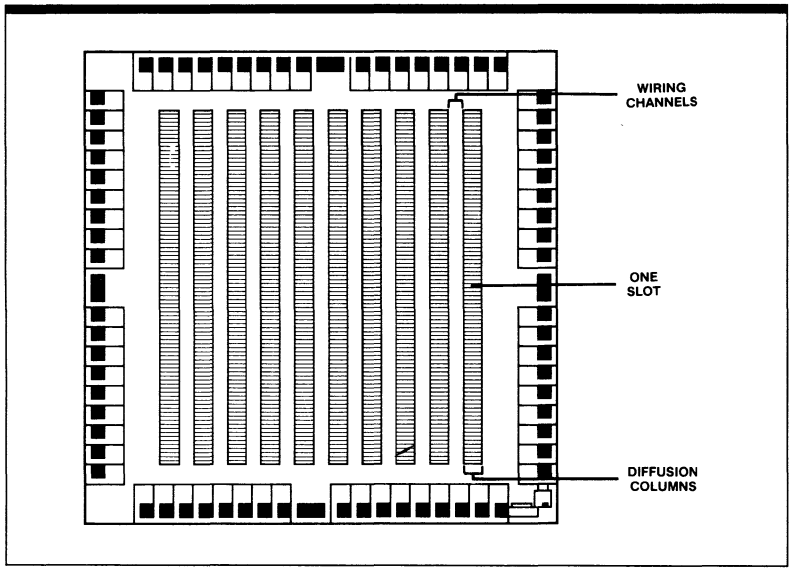


Figure 1.4
An Unconnected CMOS Gate Array

Figure 1.5 shows a portion of a 5000 Series wired array. Most of the wiring connecting the macrocells (the global vertical wiring) is on the first layer metal. The second layer metal is used for the horizontal wiring.

The peripheral cells consist of large-geometry i.e., physically large, transistors plus input protection circuits to implement input- and output-buffers. Each series has certain peripheral cells preassigned to power and ground. The unassigned cells can all be configured either as inputs, as outputs, or as bidirectional pads.

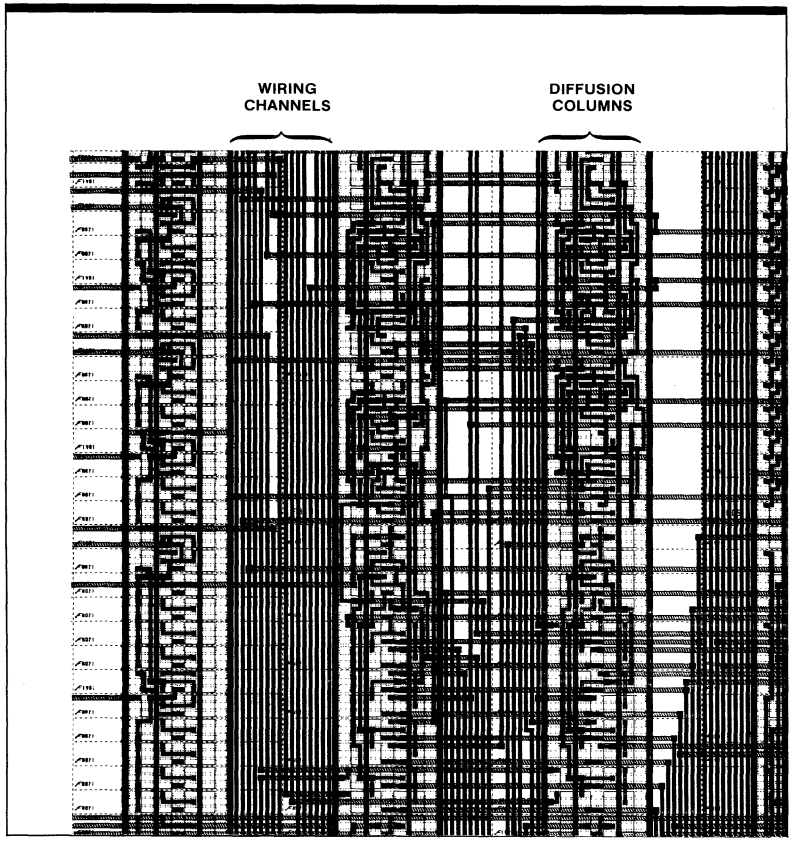


Figure 1.5
A Portion of a 5000 Series Wired Array

Traditional Circuit Design vs. Gate Array Design -- Today's integrated circuits are impossible to design using yesterday's methods. Functions previously designed for large circuit boards are now designed for single silicon chips.

Using the traditional breadboard method, you designed with a functional block diagram and a standard parts catalog. You located parts in the catalog, then purchased them and inserted them into a circuit board. After you wired and soldered the parts into a circuit network, you tested the board to see if it functioned correctly. If a part was faulty, you removed it and replaced it with a new standard part. A given circuit might need to be redesigned and rewired several times before it was finally correct.

In gate array design, computer simulation is used to electronically breadboard and analyze a circuit's performance. Voltage, temperature variation, parasitic capacitances, as well as other factors affecting a circuit's performance, are simulated on the computer before the circuit is fabricated. An analog to the redesign and rewire operation continues to be necessary in gate array design, but computer simulation spares you the necessity of physical rewiring, and also catches and corrects timing errors before your design is fabricated.

Although you may breadboard a circuit before designing the circuit as a gate array, this procedure has limited usefulness. The breadboard will show that the circuit is functionally correct. But the breadboard is an unreliable predictor of: 1) the circuit's behavior when it is implemented as a gate array, and 2) timing problems due to capacitive loading and parasitic effects on the silicon.

In most cases you should not map a finished breadboard directly into a gate array. Rather you should use the design techniques described in Chapter 4 to optimize your design either by improving its speed or by reducing its gate count. There are techniques by means of which to enhance the testability and reliability of your circuit; these can be found in Chapter 8 of this manual and in Chapter 2 of the LSI LOGIC LDS Design Manual.

Macrocells -- A macrocell is the metal pattern which connects a group of N and P transistors in such a way that the end product is a logic element. LSI LOGIC macrocells are predesigned circuits for which there exist the symbol and model files needed for accurate CAD analysis. Macrocells are available in a library similar to a standard parts catalog. Macrocells span a wide range of complexity. The simplest is a simple inverter. Among the more complex are flip-flops and RAM cells.

Macrofunctions -- Macrofunctions are collections of "software coded" macrocells which perform functions more complex than those of macrocells. Macrofunctions are available from libraries, or they may be user-defined. Before fabrication, the LDS System breaks macrofunctions down into macrocells; thus, unused macrocells can be automatically deleted.

The macrocell/macrofunction concept allows you to work in a hierarchical fashion with a large number of logic blocks of several levels of complexity, while at the same time facilitating flexible layout with a small number of standard elements.

Beginning with your circuit specifications and the LSI LOGIC Macrocell Library, you move through a logical design sequence to determine the array size, to select the correct package, and to determine which macrocells will be used as building blocks to comprise the circuit's network.

Equivalent Gates -- The number of gate equivalents required to implement the entire circuit, its "gate count," reflects the complexity of the design. LSI LOGIC array sizes vary from 400 to 10,000 gates.

LSI LOGIC defines one "gate equivalent" as equal to two P and two N transistors, or enough to create either a two-input NAND gate or a two-input NOR gate. The complexity of each macrocell is measured in terms of the number of gate equivalents required to construct it.

Macrocell Models -- Each macrocell model in the Macrocell Library contains the information you will need to create a network and perform preliminary delay calculations and simulation.

2.1 Choose an Array Series

Your paramount design consideration may be cost, or it may be performance, or it may be some other other design criterion, e.g., package size. The series at LSI are designed with overlapping characteristics so you can migrate between one series and another if the need should arise. Designs a little too large for the array size you have initially chosen can move to a larger size; designs a little too slow can move to a faster series.

2.2 Critical Path

To determine speed requirements, you need to identify the critical path or paths. Generally, the critical path is the signal path that travels through the greatest number of gates between one register and another. (A register is either a flip-flop or a latch.) In order to calculate the propagation delay of each macrocell in the path, it is necessary to determine the fanout for each macrocell in the path.

2.3 Fanout

A macrocell's fanout is equal to the number of "input loads" it drives. An "input loading factor" is assigned to the inputs of each macrocell and is used to indicate how large a capacitive load is associated with each input. A standard input loading factor of 1 is defined as the sum of an N and a P MOSFET gate capacitance. Therefore, an inverter has an input loading factor of 1; similarly, each of the inputs on a two-input NAND gate has an input loading factor of 1. The exclusive OR and exclusive NOR gate inputs each have an input loading factor of 2, since each input is connected to 2 N and 2 P MOSFET gate inputs.

The equation for calculating a macrocell's fanout is:

$$FO = IL(MC1) + IL(MC2) + \ldots IL(MCn)$$

where:

FO	= fanout for the driving macrocell
MC1,MC2...MCn	= names of the driven macrocells
IL	= input loading factor of the driven macrocell

Study each macrocell in the critical path and determine how many macrocells it drives (including those not in the critical path). Note the input loading factor for each driven macrocell, taking care to use the factor corresponding to the correct input. Then add the input loading factors of each driven macrocell. The sum equals the fanout of the driving macrocell.

Repeat this process until fanout is calculated for every macrocell in the critical path. Then total the nominal delays for each macrocell from the verifier delay tables in the macrocell section. Select from the technology that is most in keeping with your delay specifications.

2.4 Worst-Case

With a defined nominal delay, there remains the necessity of calculating a worst-case factor in order to find the propagation delay under worst-case operating conditions.

To find the worst-case delay, multiply the nominal propagation delay by the appropriate standard worst-case factor below:

w.c. commercial	(70 degrees C, 4.75V)	1.74
w.c. industry	(85 degrees C, 4.75V)	1.83
w.c. military	(125 degrees C, 4.5V)	2.21

It is possible that the standard worst-case delay factors are not suitable for your application. The following paragraphs show how LSI LOGIC calculated the commercial worst-case factor of 1.74; they also give an equation for calculating your own worst-case delay factors.

The typical propagation delays shown for each series in each macrocell listing are for 25 degrees C, 5v, and typical processing. You will need to extrapolate delays if your fanout are not equivalent to those in the tables.

Process variation could increase delays up to 40%. Thus, a 1.4 multiplier factor (called "Kp") is used to estimate the effect of worst case processing. Junction temperature (called "Kt") and supply voltage variation (called "Kv") also affect the delay. Multipliers for Kt and Kv are shown in Figure 2.1.

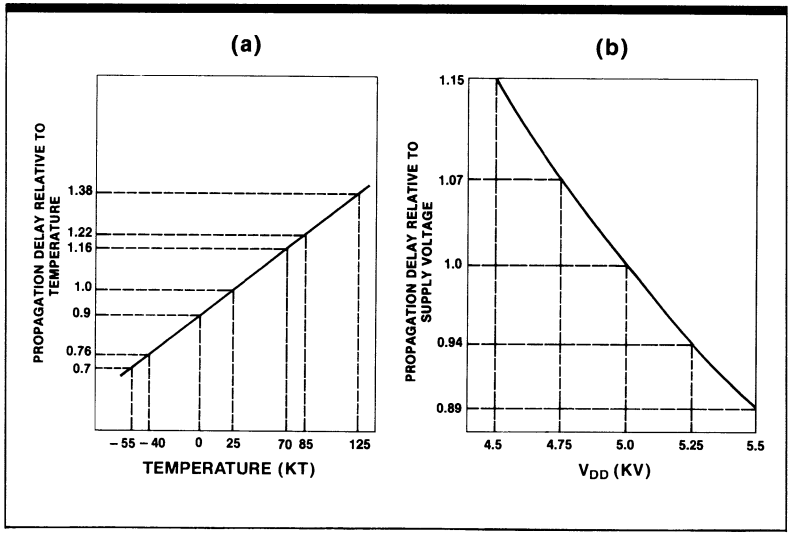


Figure 2.1
Propagation Delay (a) as a Function of Temperature (KT) and (b) as a Function of Supply Voltage (KV)

The temperature and voltage effects on delay are quite insensitive for the single-layer metal 3000 Series because the typical delays for each macrocell include polysilicon interconnect delays, which are relatively insensitive to voltage and temperature effects.

The formula for calculating worst-case propagation delay factors (Twc) is:

$$Twc = Kp \times Kt \times Kv$$

For worst case commercial range (0-70 degrees C, 4.75 to 5.25V) the maximum delay factor is:

$$Twc = 1.4 \times 1.16 \times 1.07$$
$$Twc = 1.74$$

You can calculate worst case factors for conditions other than commercial, industrial, or military uses in a similar manner.

At this point you should be able to decide on an appropriate array series.

3.1 Choose a Device

Choosing a device is sometimes called choosing an "array size." Each device in each array series has a specific number of gates, I/O pads, power (VSS, VDD) pads, and package pins, as shown in Table 3.1. In order to choose the device best serving your needs, you will need to determine the following factors in your circuit:

- Percentage of device used ("array utilization")
- Number of I/O pads used, totaling input pads, output pads, assigned power pads, additional power pads (if necessary), and BlI pads
- Number of package pins

Then review the table below for an appropriate size in your chosen array series.

Device Number	Gate Count	% Max. AUR*	Max. I/O Pads	Assigned VDD Pads	Assigned VSS Pads	Assigned VSS2 Pads	Max. Pads
3000 Series Silicon gate, oxide isolated, 3.5 micron, single layer metal							
LL3020	272	95	32	1	3	0	36
LL3030	342	95	36	1	3	0	40
LL3040	420	90	40	1	3	0	44
LL3060	600	90	48	1	3	0	52
LL3080	812	90	56	1	3	0	60
LL3110	1056	85	64	1	3	0	68
LL3130	1332	85	72	1	3	0	76
LL3170	1722	85	82	1	3	0	86
LL3210	2162	80	92	1	3	0	96
LL3250	2550	80	100	1	3	0	104
5000 Series Silicon gate, oxide isolated, 3.0 micron, double-layer metal							
LL5080	880	90	66	2	4	2	74
LL5140	1404	90	84	2	4	2	92
LL5220	2224	90	106	2	4	2	114
LL5320	3192	85	130	2	4	2	138
LL5420	4202	85	144	4	4	4	156
LL5600	5902	80	168	4	4	4	180
7000 Series (P-Version Standard Pad Pitch) Silicon gate, oxide isolated, 2.0 micron, double-layer metal							
LL7080	880	90	44	2	4	2	52
LL7140	1443	90	58	2	4	2	66
LL7220	2224	85	70	2	4	2	78
LL7320	3192	85	80	4	8	4	96
LL7420	4242	85	98	4	8	4	114
LL7600	6072	80	122	4	8	4	138
LL7840	8370	80	150	4	8	4	166
LL71000	10013	70	158	4	8	4	174
7000 Series (C-Version Tight Pad Pitch) Silicon gate, oxide isolated, 2.0 micron, double-layer metal							
LL7080	880	90	60	2	4	2	68
LL7140	1443	90	78	2	4	2	86
LL7220	2224	85	98	2	4	2	106
LL7320	3192	85	112	4	8	4	128
LL7420	4242	85	134	4	8	4	150
LL7600	6072	80	170	4	8	4	186
LL7840	8370	80	206	4	8	4	222
LL71000	10013	70	216	4	8	4	232

*Maximum Array Usage Recommended

Table 3.1
LSI LOGIC Array Specifications

3.2 Slot Count

To arrive at the slot count for your circuit, determine the number of slots required for each macrocell and then total the number of slots used for all macrocells. In most macrocells the slot count is equal to the gate count shown for each macrocell in Chapter 17 of this manual. However, there are a few exceptions which are listed below:

(5000 and 7000 Series)

Macrocell Name	Gate Count	Slot Count
IVDA	1	2
IVP	1	2
ND2	1	2
NR2	1	2

The cells listed above have an additional space assigned to them to insure routability. Since the cells are stacked in diffusion columns, adequate room must be left for horizontal crossing wires.

When you have added the total slots required for each macrocell in your design, divide them by the gate count in your array size. This percentage is your array usage. Check Table 3.1 to see that your array usage is below the maximum percentage of array usage recommended for your array size.

3.3 I/O Pad Count

Next you must determine the total number of I/O pads used. Refer to the following two tables and total the pad count for all input and output buffers. Note input buffers could require 0 or 1 pads, while output buffers can require 1 to 4 pads.

Buffer Name	Interface TTL	Interface CMOS	# Pads	* DT	Gate Count 3000 Series	Gate Count 5000 Series	Gate Count 7000 Series
IBUF		x	1	0	1	0	0
IBUFI		x	0	0	2	3	3
IBUFD		x	1	0	2	0	0
IBUFU		x	1	0	2	0	0
IBUFN		x	1	0	-	-	0
ICK1		x	2	1	-	-	0
ICK2		x	3	2	-	-	0
SCHMDT1			1	0	3	3	3
SCHMDT2			1	0	4	4	4
TLCHT	x		1	0	0	0	0
TLCHTI	x		0	0	2	3	3
TLCHTN	x		1	0	-	-	0

Table 3.2
LSI LOGIC Input Buffer Specifications

* DT is a measurement of the drive capability of the I/Os, using B1 as a standard drive capability equal to 1.

BUFFER NAME	NO. OF PADS			DT	EQUIV. GATE COUNT			REMARKS
	3K	5K	7K		3K	5K	7K	
B14	-	1	1	.25	-	1	1	
B18	1	1	1	.5	1	1	1	
B1	1	1	1	1	1	2	2	
B1OD	1	1	1	1	1	1	1	Unidirect
B2	2	2	2	2	2	4	4	Standard
B2OD	2	2	2	2	2	2	2	push/pull
OSC2	3	3	3	2	1	0	0	
B3	3	4	4	3	3	2	2	
B3OD	3	3	3	3	3	3	3	
BTS14	-	1	1	.25	-	5	5	
BTS18	-	1	1	.5	-	5	5	
BTS1	1	1	1	1	4	7	7	Uni-tristate
BTS2	2	2	2	2	5	8	8	
BTS3	3	3	3	3	6	11	11	
BTS6	-	2	-	2	-	7	-	
BTS7	1	1	1	1	4	7	7	
BTS7D	-	1	1	1	-	7	-	
BTS7LO	-	1	1	.5	-	4	4	
BTS7OD	1	1	1	1	1	1	1	
BTS7U	1	1	1	1	-	7	7	
BTS78	-	1	1	.5	-	5	5	Bi-direct
BTS8	2	2	2	2	5	8	8	
BTS8U	-	2	2	2	-	8	-	
BTS9	3	3	3	3	6	11	11	
BTS9D	-	3	3	3	-	11	-	
BTS9U	3	3	3	3	6	11	-	
B1I	1	1	1	1	1	2	2	Internal Buffer

Table 3.3
LSI LOGIC Output Buffer Specifications

3.4 Power Pads

After completing the I/O pad count, total the BlI's and add them to your total pad count. Finally, you must determine the number of power pads required and add this number to your previous total to find your total pad requirement for your circuit. This number must not exceed the "MAX. PADS" column in Table 3.1.

The number of power pads is determined primarily by the number and type of output buffers you used in your circuit. The output buffers' "slew rate," or the time it takes for a signal to switch from logical 0 to logical 1, or vice versa, causes a current spike (known as "abrupt transient current"). The output buffer devices in the 3-micron 5000 Series and the 2-micron 7000 Series have the same high slew rates, switching high capacitance loads (50pfd) in a few nanoseconds. This slew interacts with parasitic package inductance to cause current "noise." Several grounds and VDD supply pads are required to minimize the noise.

Power pads are defined as:

VSS - Ground pads for I/O buffers on the perimeter of the circuit.

VSS2 - Ground pads for internal cells of the circuit. (Protect internal macrocells from current spikes generated by the output buffers; this is not required in the 3000 Series).

VDD - Positive power pads (nominal voltage 5V).

Your particular array size (footprint) can be found on the following pages with its preassigned power pads indicated on each footprint. You must use the following information to see which VSS, VSS2, and VDD pads need to be added to the ones required originally. These additional VSS, VSS2, and VDD pads are added to the number of preassigned VSS, VSS2, and VDD pads and the sum comprises your total power pad requirements.

Equations for determining additional power pads are:

3000 Series

VSS = DT/16 - x
VSS2 Not Applicable
VDD = DT/16 - z

5000 Series

VSS = DT/16 - x
VSS2 = C - Y
VDD = DT/16 - z

7000 Series

VSS = DT/16 - x
VSS2 = All Preassigned VSS2
VDD = DT/32 - z

where:

C = the minimum number of VSS2 pads required for the 5000 Series as indicated below. The 3000 Series does not require any VSS2 pads.

Array Size	Minimum No. of VSS2 Pads
LL5080	1
LL5140	2
LL5220	2
LL5320	3
LL5420	3
LL5600	4

16 is the maximum number of B1 (or equivalent) buffers that can be placed around VSS pads (8 on each side)

x = number of preassigned VSS pads

y = number of preassigned VSS2 pads

z = number of preassigned VDD pads

Note 1: Round all results to the next higher integer

Note 2: In the 3000 and 5000 Series, you should use the preassigned VSS, VSS2 (not in 3000 Series), and VDD pads first, whenever possible. If you need to, you can use any of the other pads as a VSS, VSS2 (not in 3000 Series), or VDD. Preassigned VSS, VSS2, and VDD pads cannot be used as a signal pad in the 3000 and 5000 Series.

Note 3: 7000 Series power pads are separated into primary and secondary pads. The primary pads are grouped together in sets of 2 or 4 at the midpoint on each of the four sides. The secondary pads are located individually near the four corners of the chip. All primary pads must be used first. If additional pads are required, then the secondary pads may be used. All secondary pads not used for power may be used for circuit I/O signals.

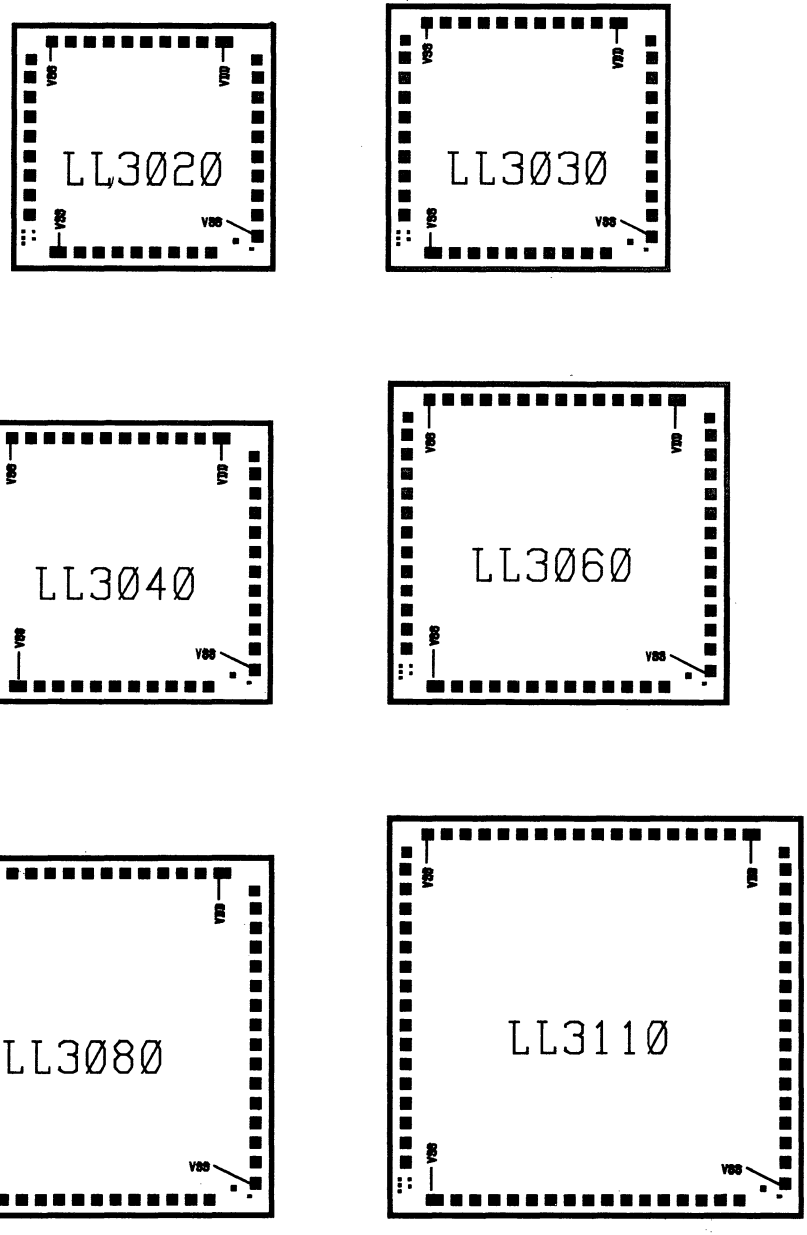


Figure 3.1
3000 Series Footprints
(LL3020 through LL3110)

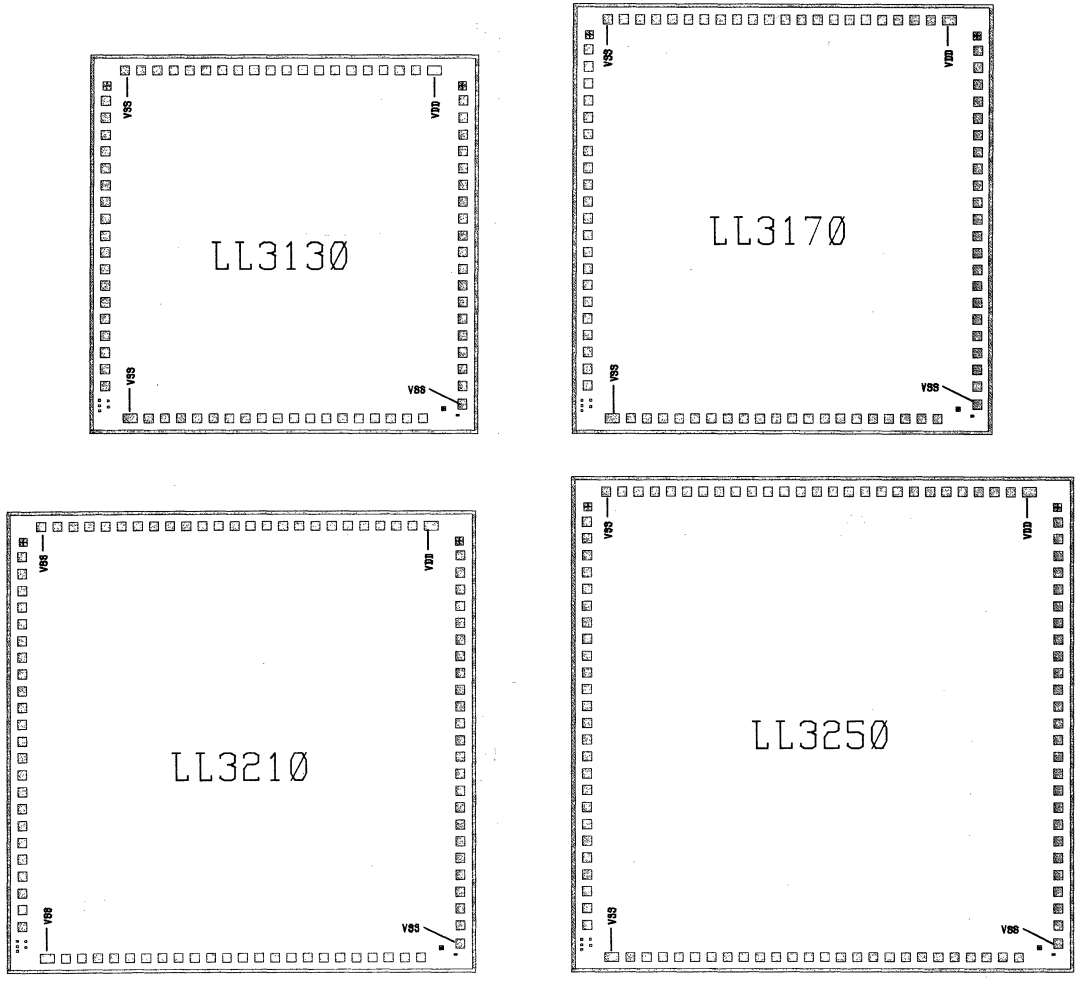
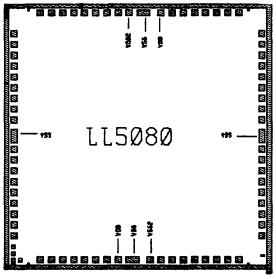
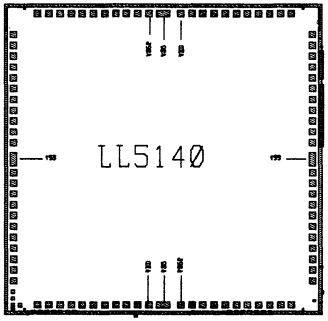
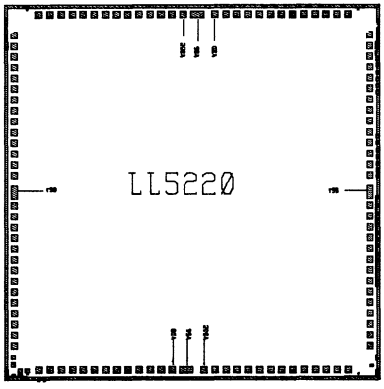


Figure 3.2
3000 Series Footprints
(LL3130 through LL3250)







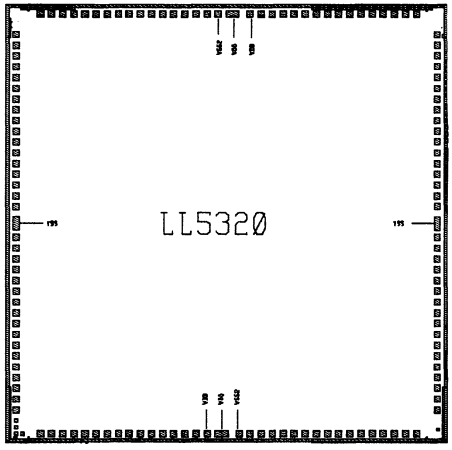
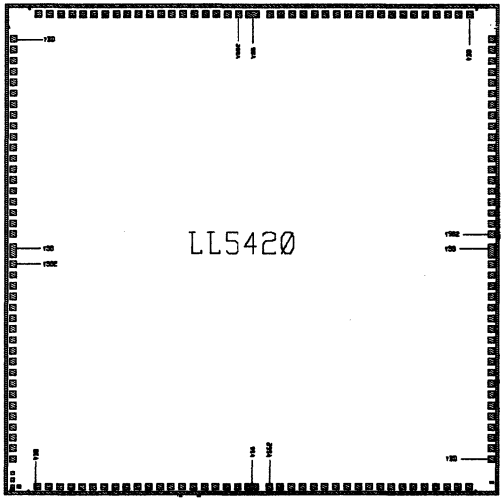


Figure 3.3
5000 Series Footprints
(LL5080 through LL5320)



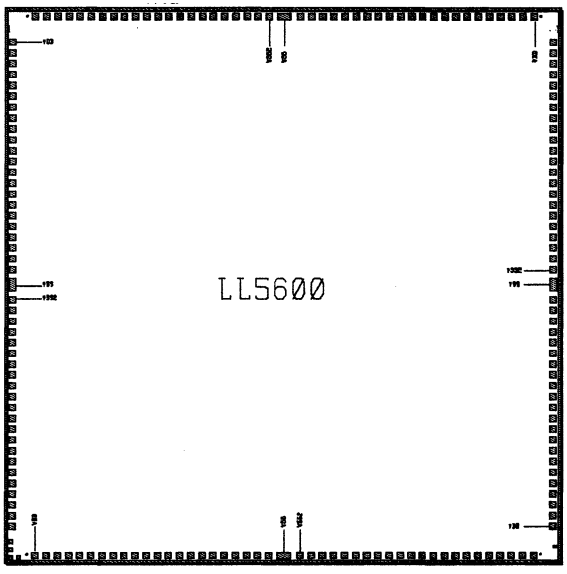


Figure 3.4
5000 Series Footprints
(LL5420 through LL5600)

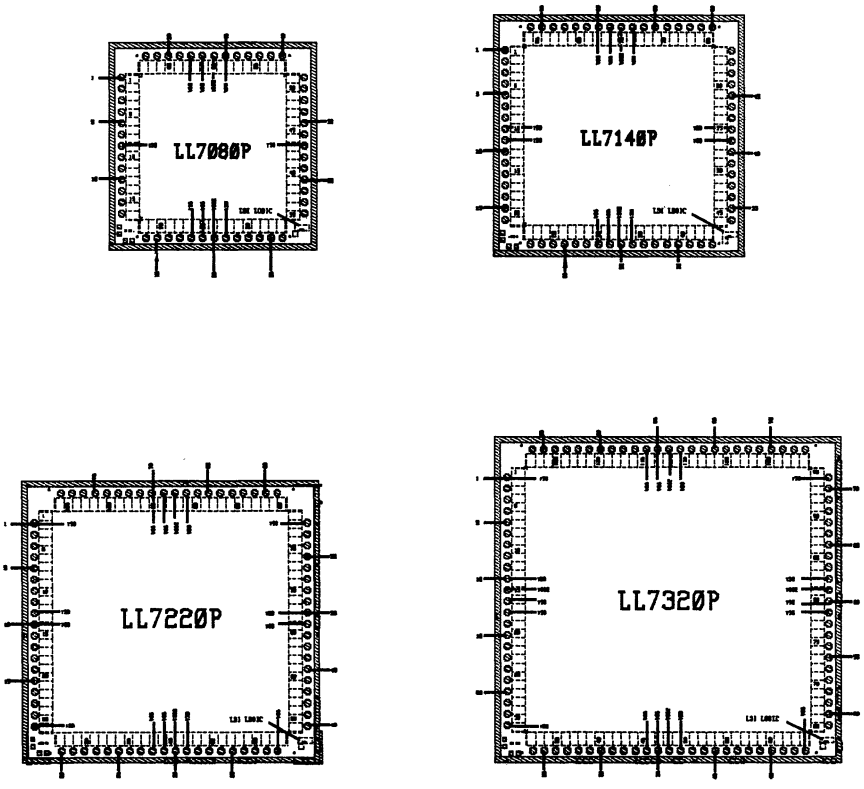
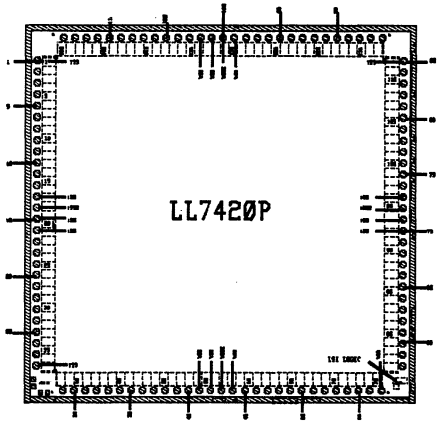


Figure 3.5
7000 Series Footprints
(LL7080P through LL7320P)



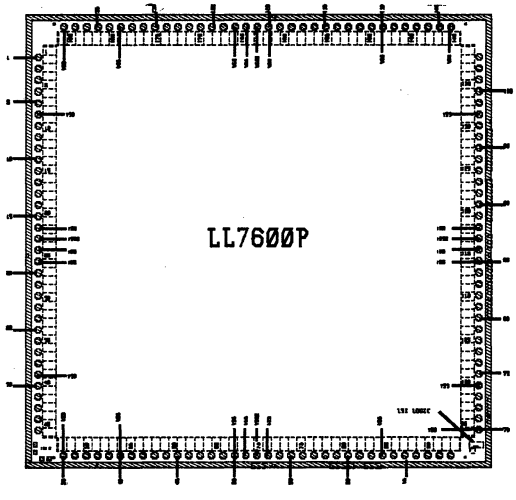


Figure 3.6
7000 Series Footprints
(LL7420P through LL7600P)

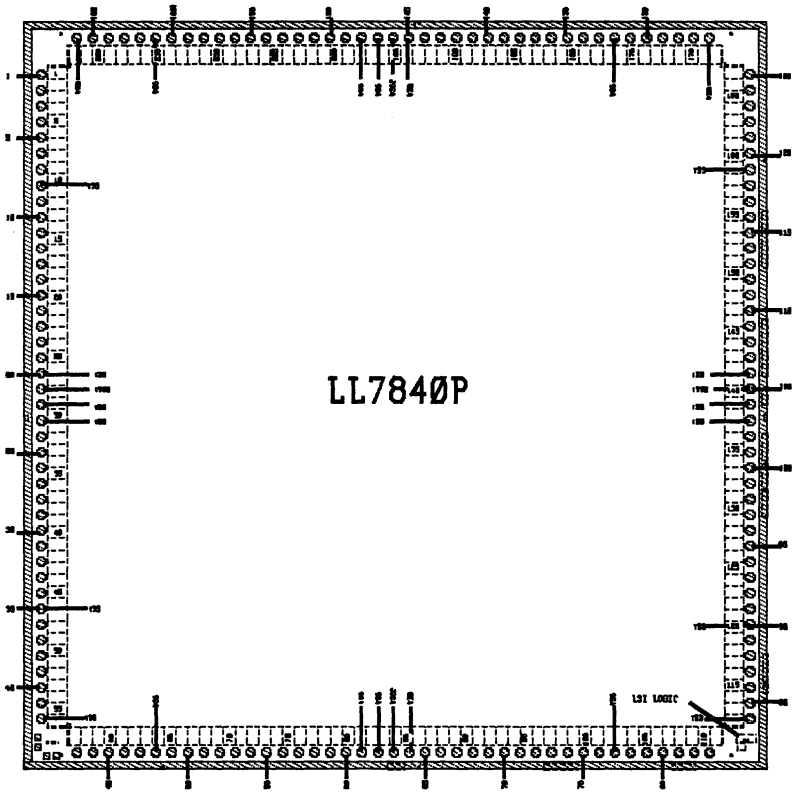


Figure 3.7
7000 Series Footprint
(LL7840P)

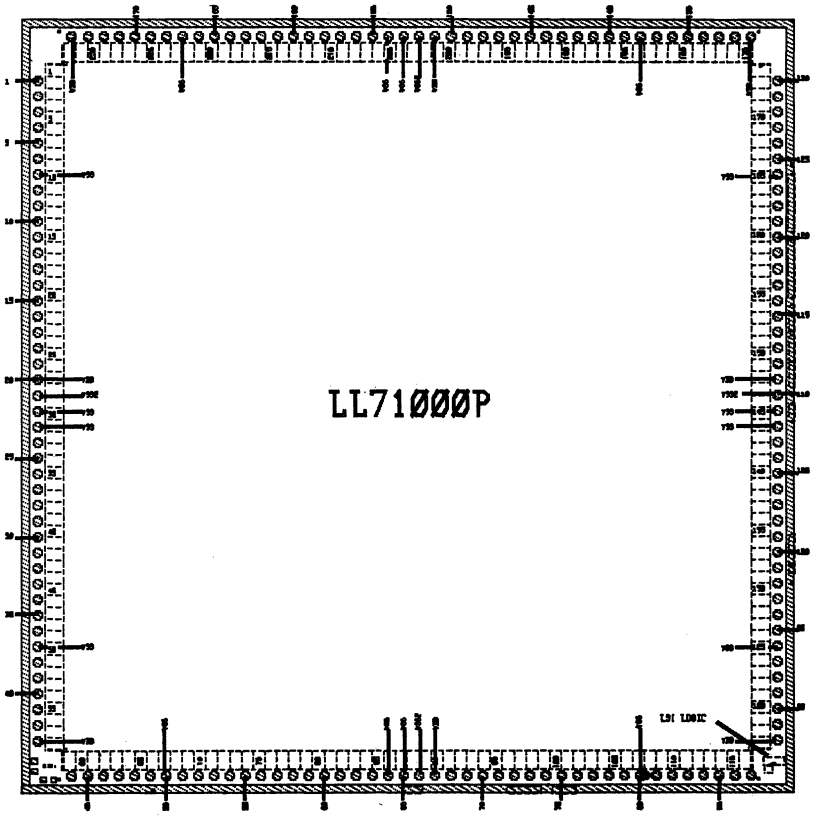
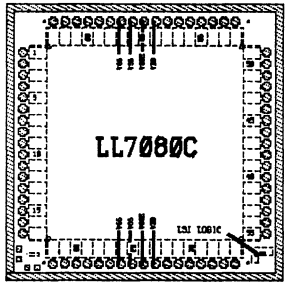
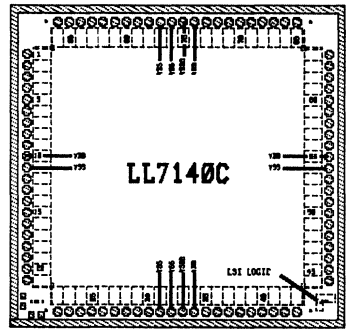
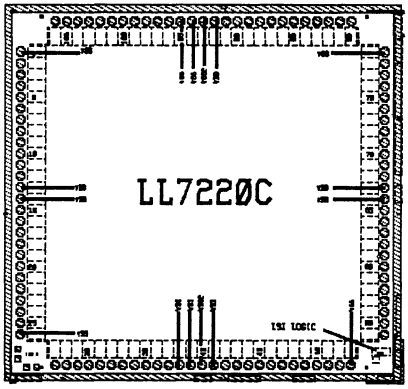


Figure 3.8
7000 Series Footprint
(LL71000P)







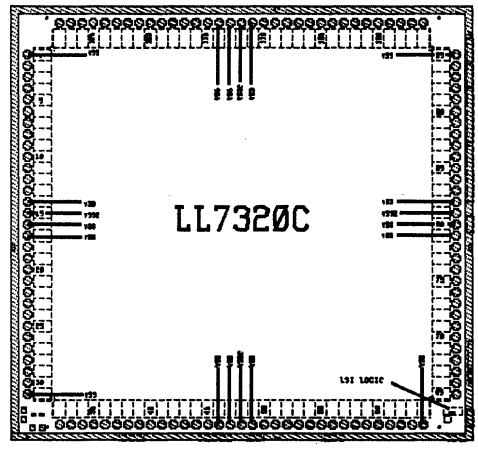
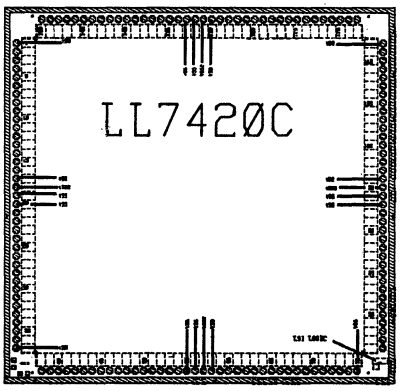


Figure 3.9
7000 Series High Density Pad Pitch Footprints
(LL7080C through LL7320C)



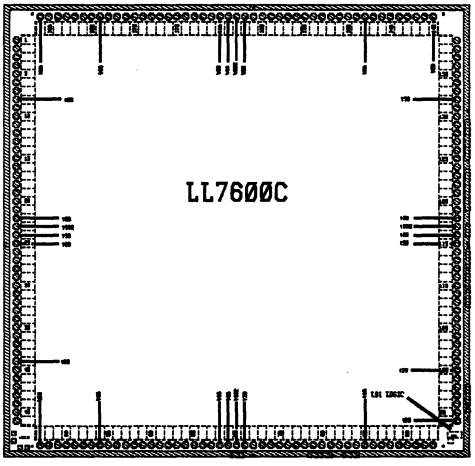


Figure 3.10
7000 Series High Density Pad Pitch Footprints
(LL7420C through LL7600C)

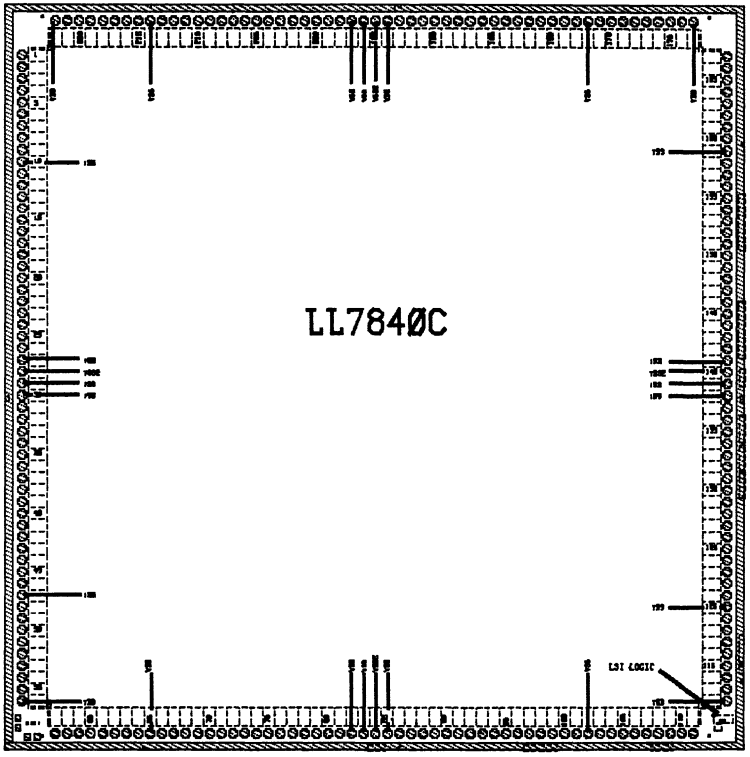


Figure 3.11
7000 Series High Density Pad Pitch Footprint
(LL7840C)

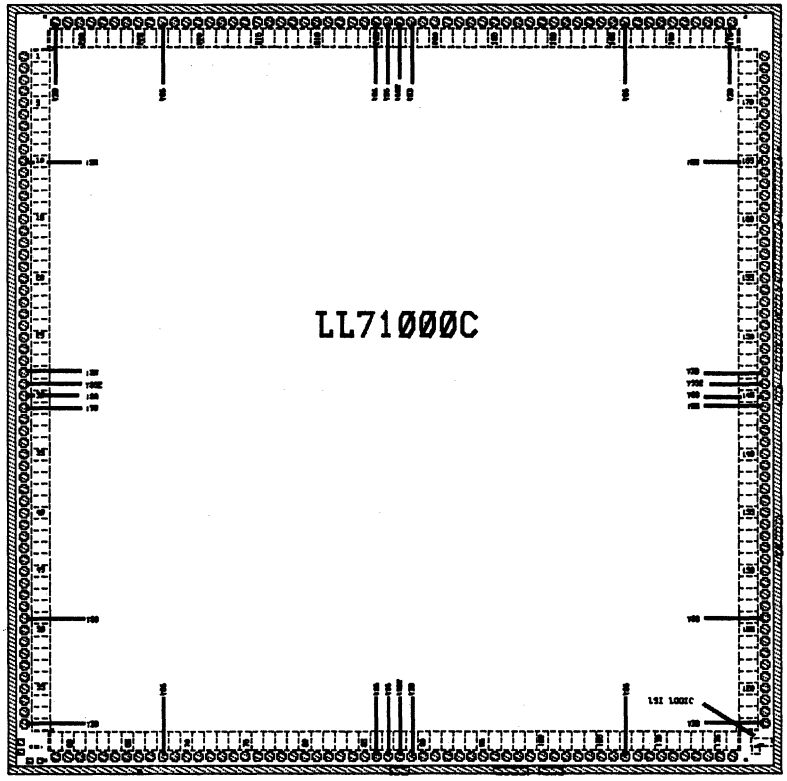


Figure 3.12
7000 Series High Density Pad Pitch Footprint
(LL71000C)

4.1 Optimize Your Design

In optimizing your design, you can improve speed, reduce gate count, and reduce I/O pin count. These improvements are covered in more detail in the LSI LOGIC LDS Design Manual.

4.2 Improve Speed

- When FO is low, use AO (And Or Invert) elements
- Place signals efficiently in multilevel gating structures
- Minimize gate inputs
- Minimize NOR gates
- Use shift counters
- Use independent outputs of flip-flops and latches
- Duplicate logic
- Use carry generate/carry propagate
- Use fast adder techniques
- Avoid high drive buffers with low fanouts
- Design high input AND gates efficiently
- Use on-chip buffers with high fanout

4.3 Reduce Gate Count

The size of a circuit is a function of its gate count and the number of its interconnections (nodes). Use the following techniques to reduce required chip area and thus the gate count and size of your array.

- Make maximum use of large macrocells with many internal interconnections.
- Use shift counters.
- Use ripple counters, propagation delay permitting.
- Minimize the number of signal nodes by routing only one polarity of signal between modules.

- When you need an input multiplexer for a flip-flop or latch, use a scan test flip-flop or latch.

- Minimize the use of inverters by careful logic design and the use of DeMorgan's theorem.

4.4 Reduce I/O Pin Count

An array's cost is influenced by its package. Often, it is cost-effective to add logic to reduce pins, and thus reduce package size. Reducing the number of outputs may also reduce the number of power pins.

You may use several techniques to reduce I/O pin count:

- Bit Slicing - Partitioning a system by bits rather than by function will nearly always reduce its pin count. It will also reduce the number of unique part types.

- Serial Transfer - When propagation delay permits, transmit data in series rather than in parallel.

- Illegal Input Codes for Test - Initialize test nodes by forcing array inputs to respond to input patterns which do not occur in the circuit's normal operating mode.

- Multiplex Test Points - Bring test points off-chip without using an extra pin by multiplexing the normal outputs with a test pin control.

- Single Rail Transfer - Transfer only one polarity of signal between arrays; invert the signal locally on the receiver array.

- Decode Locally - Use a separate signal decoding network on each array.

- Use Local Counters - Rather than transferring counter data between several arrays, duplicate counters in each array and synchronize the counters.

- Use Signal Bussing - Use one line to carry information from a variety of sources. Use local storage to hold signal values.

- Use External MSI - When you require a large number of parallel outputs, use external MSI registers to save array pins.

5.1 Selection Process

Selecting a package requires the following steps:

- Decide the package type you want, using the LSI LOGIC "Logic Array Packaging Application Note A33." (Ask your LSI LOGIC application engineer for a copy of this note.)
- Use the charts in this Section 5.3 to determine package size.
- Use the LSI LOGIC Corporation "Logic Array Package Selector Guide" to select a specific package.

5.2 Determine the Package Type

You may choose from a variety of plastic and ceramic packages for your device, including:

Package Type	LSI LOGIC Package Code
Plastic Dual-in-Line Packages	
16-pin plastic dual-in-line package	LE
22-pin plastic dual-in-line package	LH
24-pin plastic dual-in-line package	LA
28-pin plastic dual-in-line package	LB
40-pin plastic dual-in-line package	LC
48-pin plastic dual-in-line package	LJ
Ceramic Dual-in-Line Packages	
16-pin ceramic dual-in-line package	GE
22-pin ceramic dual-in-line package	GH
24-pin ceramic dual-in-line package	GA
28-pin ceramic dual-in-line package	GB
40-pin ceramic dual-in-line package	GC
48-pin ceramic dual-in-line package	GJ
64-pin ceramic dual-in-line package	GD
Plastic Chip Carriers	
68-pin plastic chip carrier (J-bend leads)	MC
84-pin plastic chip carrier (J-bend leads)	MD

Package Type	LSI LOGIC Package Code
Ceramic Chip Carriers	
20-pin leadless ceramic chip carrier	AG
28-pin leadless ceramic chip carrier	AE
52-pin leadless ceramic chip carrier	AJ
68-pin leadless ceramic chip carrier (ECL type A)	AA
68-pin leadless ceramic chip carrier (MOS type A)	AB
68-pin leadless ceramic chip carrier (MOS type B)	AK
84-pin leadless ceramic chip carrier (MOS type A)	AL
84-pin leadless ceramic chip carrier (MOS type B)	AM
84-pin leadless ceramic chip carrier (MOS type C)	AD
Ceramic Pin-grid Arrays	
64-pin ceramic pin-grid array	FA
68-pin ceramic pin-grid array	FB
84-pin ceramic pin-grid array	FC
100-pin ceramic pin-grid array	FG
120-pin ceramic pin-grid array	FD
144-pin ceramic pin-grid array	FE
180-pin ceramic pin-grid array	FF

Table 5.1
LSI LOGIC Package Types

5.3 Determine Package Size

Use Tables 5.2, 5.3, and 5.4 to determine how large a package you need for the array size you have chosen.

The tables are arranged for each series by device and package type, showing the minimum number of package pins required to implement each device. (Pin counts are in proportion to package cavity size: in general, the larger the pin count, the larger the cavity size.) Using the tables, determine the minimum number of pins required to accomodate your design.

Read the tables in this way:

- The DEVICE column lists the LSI LOGIC part number of each device.

- The CERAMIC DIP, PLASTIC DIP, CERAMIC CHIP CARRIERS, PIN GRID ARRAYS, and PLASTIC CHIP CARRIERS columns refer to package types that are offered by LSI LOGIC. They are to be read in the following way. Suppose you have chosen Device LL3020. Suppose also that you have chosen to use a ceramic dip package. The number 16 signifies the smallest package (16 pin) that will accommodate your design. The plus sign signifies that the device can fit into a package with more than 16 pins. The N/A means there is no package of that type suitable for the array listed in the leftmost column on the same line; no die is allowed to be placed in a package with more leads than are needed to bond all pads. The large lead count packages have large die pad cavities; therefore, the wire bonds will be too long for a small die.

DEVICE	CERAMIC DIP	PLASTIC DIP	CERAMIC CHIP CARRIER	PIN GRID ARRAY	PLASTIC CHIP CARRIER
LL3020	16+	16+	20+	N/A	N/A
LL3030	16+	16+	20+	N/A	N/A
LL3040	16+	16+	20+	N/A	N/A
LL3060	22+	22+	20+	N/A	N/A
LL3080	22+	22+	20+	N/A	N/A
LL3100	22+	22+	28+	64+	68+
LL3130	22+	22+	28+	64+	68+
LL3170	24+	24+	44+	64+	68+
LL3210	24+	24+	44+	64+	68+
LL3250	24+	28+ (1)	52+	64+	68+

Table 5.2
3000 Series Minimum Package Pin Requirements

DEVICE	CERAMIC DIP	PLASTIC DIP	CERAMIC CHIP CARRIER	PIN GRID ARRAY	PLASTIC CHIP CARRIER
LL5080	22+	22+	28+	64+	68+
LL5140	22+	22+	44+	64+	68+
LL5220	24+	28+	44+	64+	68+
LL5320	40+	28+ (1)	68+	64+	68+
LL5420	64+	N/A	68+	64+	68+
LL5600	64+	N/A	84+	68+	68+

Table 5.3
5000 Series Minimum Package Pin Requirements

DEVICE	CERAMIC DIP	PLASTIC DIP	CERAMIC CHIP CARRIER	PIN GRID ARRAY	PLASTIC CHIP CARRIER
LL7090	22+	22+	20+	64+	N/A
LL7140	22+	22+	28+	64+	68+
LL7220	22+	22+	28+	64+	68+
LL7320	24+	24+	44+	64+	68+
LL7430	24+	28+ (1)	52+	64+	68+
LL7600	40+	28+ (1)	68+	64+	68+
LL7840	64+	N/A	84+	68+	68+
LL71000	64+	N/A	84+	68+	68+

Table 5.4
7000 Series Minimum Package Pin Requirements

(1) The device may be placed into an etch frame at additional cost.

5.4 Use the Selector Guide

Once you have decided on a package and have used the charts to determine its size, refer to the LSI LOGIC Corporation "Logic Array Package Selector Guide" for a choice of specific packages. This guide lists the physical dimensions of each package.

5.5 7000 Series Packaging

If final production will make use of a plastic package, the device must nevertheless be designed with the standard pad pitch array footprint. Even though prototypes will be in a ceramic package, there is no difficulty in taking a standard pad patch and building it on a ceramic package. But, no 7000 Series array designed on a dense pad pitch footprint can be put into a plastic package.

6.1 Determine I/O Assignment

After the array selection has been made, and the pinout and I/O established, a bonding diagram may be done. Obtain from an LSI LOGIC applications engineer the right package cavity outline and the correct die footprint. Exercise care in the assignment of input and output signals: position outputs near VSS pads and cluster them together, away from inputs. Make sure that there are sufficient VSS pads to service output switching current. Identify cell types and name I/O signals. After the completion of the bonding diagram, present it to an LSI LOGIC applications engineer for approval.

A completed bonding diagram signifies fixed pinout locations; while LSI LOGIC cannot guarantee layout according to the established pinout, every effort will be made to accommodate the pinout specification. In general, this can be accomplished.

Figure 6.1 shows a sample completed bonding diagram.

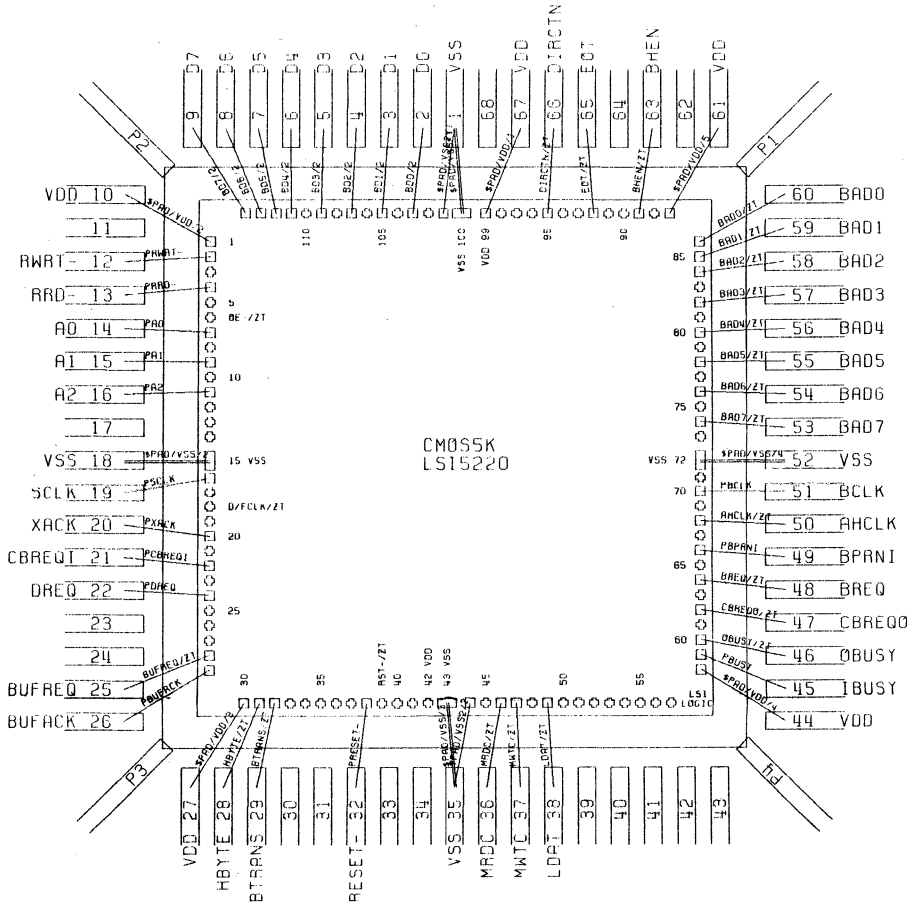


Figure 6.1
A Completed 5220 Bonding Diagram
(68-pin chip carrier)

7.1 Junction Temperature

In calculating propagation delays it is necessary to use the junction temperature (i.e., the temperature of the die inside the package) in order to determine the temperature multiplier: note that a rise in junction temperature increases a circuit's propagation delay.

LSI LOGIC CORPORATION
1601 McCarthy Boulevard, Milpitas, CA 95035

POWER CALCULATIONS FORM

Customer Information

Company Name: _____

Engineer's Name: _____

Circuit Name: _____

Circuit Data

Array Series milliwatts/gate (P): (check one)
P = _____ .025 (3000 Series)
_____ .020 (5000 Series)
_____ .018 (7000 Series)

Operating Frequency (F) (in megahertz)
F = _____ MHz

Ambient Operating Temperature (T_a) (in degrees centigrade)
T_a = _____ C

Number of Gates (G):
G = _____

Number of Outputs (B):
B = _____

Output Load Capacitance (C): (in picofarads)
C = _____ pF

Register Percentage (R): (gate count of registers/total gates)
R = _____

Internal Power Dissipation (P_{int}) (in milliwatts)

$P \times F \times G \times \{[R \times 0.1] + [(1 - R) \times 0.3]\} = P_{int}$
P_{int} = _____ mW

External Power Dissipation (P_{ext}) (in milliwatts)

$.025\ mW \times F \times B \times 20\% \times C = P_{ext}$
P_{ext} = _____ mW

Total Power Dissipation (P_{tot}) (in watts)

$(P_{int} + P_{ext}) \times .001 = P_{tot}$
P_{tot} = _____ W

Junction Temperature (T_j) (in degrees centigrade)

$(P_{tot} \times \theta_{ja}) + T_a = T_j$
T_j = _____ C

Figure 7.1
Power Calculations Form

7.2 Power Calculations Form

The power calculation form shown in Figure 7.1 helps you to calculate the junction temperature.

7.3 Step Completion

Follow these instructions to complete the power calculations form:

Step 1: Complete the Circuit Data Section -- Complete each part of the Circuit Data Section as follows:

- Typical Power Dissipation (P) (millwatts/gate): Put a checkmark in the blank corresponding to the array series you have chosen.
- Operating Frequency (F): Write the circuit's operating frequency (in megahertz) in the blank.
- Ambient Operating Temperature (Ta): Write the circuit's ambient operating temperature (in degrees centigrade) in the blank.
- Number of Gates (G): Write the number of gates required by the circuit in the blank.
- Number of Outputs (B): Write the number of outputs the circuit contains in the blank.
- Output Load Capacitance (C): If you do not know the actual wire lengths between your circuit and interfacing chips on the printed circuit board, you must estimate the output load capacitance by using the input capacitance specifications for the interfacing chips. Write your estimate (in picofarads) in the blank.

Step 2: Calculate the Register Percentage (R) -- Count the number of registers (flip-flops and latches) your circuit contains, and calculate the number of gates used by the registers. Divide the gate count of the registers by the circuit's total gate count, and write the result in the blank.

Step 3: Calculate the Internal Power Dissipation (IP) -- Using the values you noted in the Circuit Data Section, and the Register Percentage you calculated, solve the equation shown, and write the result in the blank.

Step 4: Calculate the External Power Dissipation (EP) -- Using the values you entered in the Circuit Data Section, solve the equation shown; write the result in the blank.

Step 5: Calculate the Total Power Dissipation (TP) -- Add the Internal Power Dissipation to the External Power Dissipation and multiply the sum by .001. The result is the circuit's Total Power Dissipation (in watts). Write the result in the blank.

Step 6: Calculate the Junction Temperature (Tj) -- Multiply the Total Power Dissipation by the thermal impedence (Oja) of the package you have chosen. (Typical package thermal impedences are shown in Table 7.1. When the thermal impedence is given as a range, use the highest value in the range.) Add the result to the Ambient Operating Temperature (Ta) you entered in the Circuit Data Section. Write the sum in the blank.

PACKAGE TYPE	θ_{JC} (°C/WATT)	θ_{JA} STILL AIR (°C/WATT)	θ_{JA} 300 FT/MIN (°C/WATT)
16 LEAD DIP—Ceramic	28	95	
—Plastic		150	
24 LEAD DIP—Ceramic	16	45 - 60	30 - 40
—Plastic	50	110 - 130	
40 LEAD DIP—Ceramic		45 - 50	25 - 30
—Plastic	45	110 - 125	
68 LEAD CHIP CARRIER	5	50	35
with heat sink			10 - 20
68 LEAD CARRIER			
in socket		40	30
with heat sink/socket		25 - 30	10 - 25
PIN GRID (Cavity Up)			
64-100 (10 x 10 grid)		30 - 35	20 - 23

Table 7.1
Typical Thermal Impedences

Chapter 8: Design for Testability and Reliability

This chapter concentrates on ways to design testability and reliability into a circuit. As you complete your design, follow these recommendations for developing logic that lends itself to system simulation, functional simulation, and tester parametric simulation. Details of these techniques can be found in the LSI LOGIC LDS Design Manual, Chapter 2.

- Recommended Techniques for Improving a Circuit's Testability
  - Know the characteristics of combinational logic
  - Add test lines to sequential logic
  - Use reset signals to reset registers
  - Break up long counters
  - Make buried states more accessible and observable
  - Use Level-Sensitive Scan Design (LSSD) to simplify test pattern creation
  - Use Transparent latches
  - Be sure redundant logic is testable
  - Use a test pin to drive all outputs and I/O's to high impedance states

- Recommended Techniques for Improving a Circuit's Reliability
  - Avoid Ring Oscillators
  - Use redundant arrays featuring Monitor-Mode
  - Be aware of glitch circuits
  - Use potential glitch generators safely
  - Avoid Asynchronous Pulse Generators
  - Correct glitches by using non-overlapping signal generators
  - Avoid gated clocks
  - Use Johnson counters or separate flip-flops to decode terminal counts
  - Avoid race conditions
  - Avoid feedback paths between registers
  - Avoid floating nodes on internal tristate buses or external bidirectional buses
  - Use output buffers with pull-up or pull-down resistors for external bidirectional buffers
  - Limit fanout

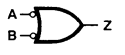
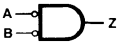
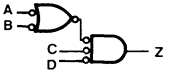
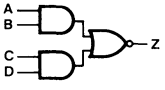
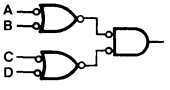
Your device will be tested twice during the manufacturing process: once before and once after the device is packaged. During both testing sequences, the LSI LOGIC automatic tester uses test patterns which you create during tester functional and parametric simulations. The tester verifies the correct operation of each circuit by clocking in your test patterns, and then checking to see whether the output patterns are identical to the ones predicted in simulations.

Final test patterns must conform to the test pattern standards.

The LSI LOGIC LDS Design Manual will detail preparations for test pattern generation. (Additional information can be found in LSI LOGIC Application Note A32A entitled "Testing Logic Arrays.")

CMOS technology is ideal for logic arrays since it allows easy implementation of a variety of logic functions. NANDs, NORs, AND-OR Inverts, and Exclusive ORs are all easily implemented in CMOS. Logic design which takes advantage of CMOS's flexibility makes for smaller, faster circuits.

Available LSI LOGIC Macrocell gates are shown tabulated in Table 10.1. A design can be simplified by considering the operation of the gate with both active level- high and active level-low inputs. Table 10.1 provides two logic symbols for each physical implementation. Manipulation of the alternate logic symbols and use of DeMorgan's theorem can facilitate logic design and minimize gates.(1)

MACRO-CELL	*EQUIV.(1) GATES*	*LOGIC SYMBOL*	*ALTERNATE LOGIC SYMBOL*	*FUNCTION*	*REMARKS*
ND2 ALSO AVAILABLE ND3, ND4, ND6, ND8	ND2 1 ND3 2 ND4 2 ND6 5 ND8 6			A B Z H H L H L H L H H L L H	NAND GATES EXHIBIT LOWER, MORE SYMMETRICAL DELAYS THAN NORS. THEY PROVIDE THE ACTIVE LEVEL HIGH OR FUNCTION FOR COMPLEMENTED (ACTIVE LEVEL LOW) INPUTS.
NR2 ALSO AVAILABLE NR3, NR4, NR6, NR8	NR2 1 NR3 2 NR4 2 NR6 5 NR8 6			A B Z H H L H L L L H L L L H	NOR GATES PROVIDE THE ACTIVE LEVEL HIGH AND FUNCTION FOR COMPLEMENTED (ACTIVE LEVEL LOW) INPUTS.
AO1	2			A B C D Z H H X X L X X H X L X X X H L X L L L H L X L L H	AO1 PROVIDES BOTH AND & OR FUNCTIONS WITH A SINGLE INVERSION.
AO2	2			A B C D Z H H X X L X X H H L L X L X H X L L X H L X X L H X L X L H	THE AO2 PROVIDES AND, OR FUNCTIONS WITH A SINGLE INVERSION.

(1) EQUIVALENT GATES FOR 3K/5K/7K SERIES, LC MAY BE DIFFERENT.

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(1) Winkel and Prosser, The Art of Digital Design, Prentice Hall, 1980

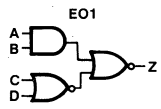
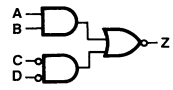
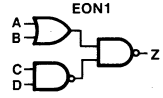
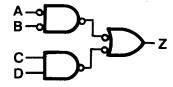
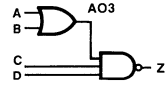
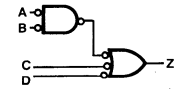
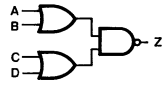
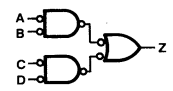
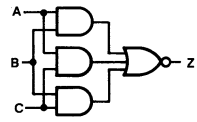
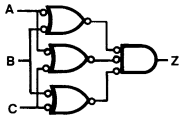
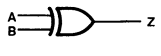
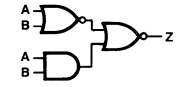
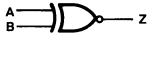
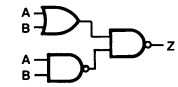
MACRO-CELL	EQUIV.(1) GATES	LOGIC SYMBOL	ALTERNATE LOGIC SYMBOL	FUNCTION	REMARKS
EO1	3			A B C D Z H H X X L X X L L L L X H X H X L H X H L X X H H X L X H H	THE EO1 PROVIDES AN INVERTING DATA SELECTOR WHEN B AND C ARE CONNECTED.
EON1	3			A B C D Z L L X X H X X H H H X H X L L H X X L L X H L X L H X L X L	THE EON1 PROVIDES A NON-INVERTING DATA SELECTOR WHEN B AND C ARE CONNECTED.
AO3	2			A B C D Z H X H H L X H H H L L L X X H X X L X H X X X L H	THE AO3 PROVIDES OR & AND FUNCTIONS WITH A SINGLE INVERSION.
AO4	2			A B C D Z L L X X H X X L L H H X H X L X H H X L H X X H L X H X H L	THE AO4 IS IDEAL FOR THE AND-OR FUNCTION WHEN COMPLEMENTED INPUTS, i.e., INPUTS IN OPPOSITE STATES, ARE AVAILABLE.
AO5	3			A B C Z H H X L H X H L X H H L L L X H L X L H X L L H	THE AO5 PROVIDES THE MAJORITY FUNCTION; WHEN ANY TWO INPUTS ARE HIGH, THE OUTPUT IS LOW, AND VICE-VERSA.
EO	3			A B Z L L L H L H L H H H H L	THE EXCLUSIVE OR FUNCTION ALSO WORKS AS A GATED INVERTER, WHEN B IS LOW, Z = A, WHEN B IS HIGH, Z = $\overline{A}$.
EO3	6			A B C Z L L L L L L H H L H L H L H H L H L L H H L H L H H L L H H H H	3-INPUT EXCLUSIVE OR
EN	3			A B Z L L H H L L L H L H H H	THE EXCLUSIVE NOR PROVIDES THE COMPARE FUNCTION, Z = H WHEN A = B.
EN3	6			A B C Z L L L H L L H L L H L L L H H H H L L L H L H L H H L L H H H L	3-INPUT EXCLUSIVE NOR

Table 10.1
Combinatorial Macrocells

The remainder of this manual consists primarily of the macrocell and macrofunction catalog, with some preliminary information about gate macrocells, on-chip buffers, flip-flops, latches, I/O buffers, and counters.

Refer to the table of contents for:

- alphanumeric listing of macrocells
- alphanumeric listing of macrofunctions

Refer to Appendix I, The Selector Guide for:

- functional listing of macrocells
- functional listing of macrofunctions

Note 1:

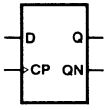
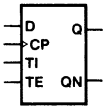
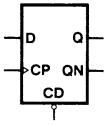
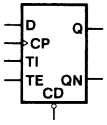
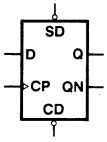
The delay values for macrocells in both the 5000 and 7000 Series arrays have been calculated based on statistical wirelengths for a 2200 gate array. For macrocells in a 3000 Series array, calculations were based on an 1100 gate array. For larger arrays, the delay values increase due to longer wirelengths. For example, a 6000 gate array has approximately 10% slower performance for a macrocell with a fanout of 3.

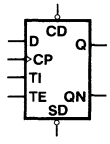
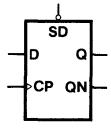
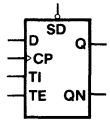
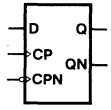
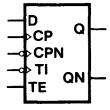
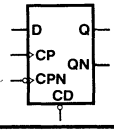
Note 2:

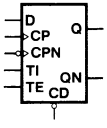
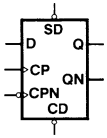
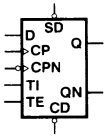
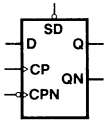
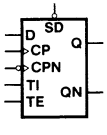
All macrofunctions using transmission gates will be replaced by a MUX21LA.

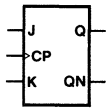
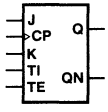
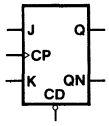
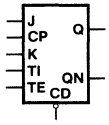
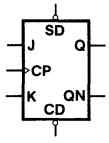
11.1 Flip-Flop Characteristics

The following table lists all of LSI's flip-flops and their major characteristics.

MACRO-CELL	LOGIC SYMBOL	FUNCTION	EQUIV. GATE COUNT	TYPE	REMARKS
FD1		D CP | Q QN 0 ↑ | 0 1 1 ↑ | 1 0	5	D	No async inputs
FD1S		D TI TE CP | Q QN 0 X 0 ↑ | 0 1 1 X 0 ↑ | 1 0 X 0 1 ↑ | 0 1 X 1 1 ↑ | 1 0	8	D	No async inputs with scan test inputs
FD2		D CP CD | Q QN 0 ↑ 1 | 0 1 1 ↑ 1 | 1 0 X X 0 | 0 1	6	D	With clear direct
FD2S		D TI TE CP CD | Q QN 0 X 0 ↑ 1 | 0 1 1 X 0 ↑ 1 | 1 0 X 0 1 ↑ 1 | 0 1 X 1 1 ↑ 1 | 1 0 X X X X 0 | 0 1	9	D	With scan test inputs, clear direct
FD3		D CP CD SD | Q QN 0 ↑ 1 1 | 0 1 1 ↑ 1 1 | 1 0 X X 0 1 | 0 1 X X 1 0 | 1 0 X X 0 0 | 1 1	7	D	With clear direct, set direct

MACRO-CELL	LOGIC SYMBOL	FUNCTION	EQUIV. GATE COUNT	TYPE	REMARKS
FD3S		D TI TE CP CD SD | Q QN 0 X 0 ↑ 1 1 | 0 1 1 X 0 ↑ 1 1 | 1 0 X 0 1 ↑ 1 1 | 0 1 X 1 1 ↑ 1 1 | 1 0 X X X X 0 1 | 0 1 X X X X 1 0 | 1 0 X X X X 0 0 | 1 1	10	D	With scan test inputs, clear direct, set direct
FD4		D CP SD | Q QN 0 ↑ 1 | 0 1 1 ↑ 1 | 1 0 X X 0 | 1 0	6	D	With set direct
FD4S		D TI TE CP SD | Q QN 0 X 0 ↑ 1 | 0 1 1 X 0 ↑ 1 | 1 0 X 0 1 ↑ 1 | 0 1 X 1 1 ↑ 1 | 1 0 X X X X 0 | 1 0	9	D	With scan test inputs, set direct
FD5		D CP CPN | Q QN 0 ↑ ↓ | 0 1 1 ↑ ↓ | 1 0	4	D	Without buffered clocks
FD5S		D TI TE CP CPN | Q QN 0 X 0 ↑ ↓ | 0 1 1 X 0 ↑ ↓ | 1 0 X 0 1 ↑ ↓ | 0 1 X 1 1 ↑ ↓ | 1 0	7	D	Without buffered clocks, with scan test inputs
FD6		D CP CPN CD | Q QN 0 ↑ ↓ 1 | 0 1 1 ↑ ↓ 1 | 1 0 X X X 0 | 0 1	5	D	Without buffered clocks, with clear direct

MACRO-CELL	LOGIC SYMBOL	FUNCTION	EQUIV. GATE COUNT	TYPE	REMARKS
FD6S		D TI TE CP CPN CD | Q QN 0 X 0 ↑ ↓ 1 | 0 1 1 X 0 ↑ ↓ 1 | 1 0 X 0 1 ↑ ↓ 1 | 0 1 X 1 1 ↑ ↓ 1 | 1 0 X X X X X 0 | 0 1	8	D	Without buffered clocks, with scan test inputs clear direct
FD7		D CP CPN CD SD | Q QN 0 ↑ ↓ 1 1 | 0 1 1 ↑ ↓ 1 1 | 1 0 X X X 0 1 | 0 1 X X X 1 0 | 1 0 X X X 0 0 | 1 1	6	D	Without buffered clocks, with clear direct, set direct
FD7S		D TI TE CP CPN CD SD | Q QN 0 X 0 ↑ ↓ 1 1 | 0 1 1 X 0 ↑ ↓ 1 1 | 1 0 X 0 1 ↑ ↓ 1 1 | 0 1 X 1 1 ↑ ↓ 1 1 | 1 0 X X X X X 0 1 | 0 1 X X X X X 1 0 | 1 0 X X X X X 0 0 | 1 1	9	D	Without buffered clocks, with scan test with clear direct , set direct
FD8		D CP CPN SD | Q QN 0 ↑ ↓ 1 | 0 1 1 ↑ ↓ 1 | 1 0 X X X 0 | 1 0	5	D	Without buffered clocks, with set direct
FD8S		D TI TE CP CPN SD | Q QN 0 X 0 ↑ ↓ 1 | 0 1 1 X 0 ↑ ↓ 1 | 1 0 X 0 1 ↑ ↓ 1 | 0 1 X 1 1 ↑ ↓ 1 | 1 0 X X X X X 0 | 1 0	8	D	Without buffered clocks, with scan test inputs set direct

MACRO-CELL	LOGIC SYMBOL	FUNCTION	EQUIV. GATE COUNT	TYPE	REMARKS
FJK1		J K CP | Q QN 0 0 ↑ | Q QN 0 1 ↑ | 0 1 1 0 ↑ | 1 0 1 1 ↑ | QN Q	8	JK	
FJK1S		J K TI TE CP | Q QN 0 0 X 0 ↑ | Q QN 0 1 X 0 ↑ | 0 1 1 0 X 0 ↑ | 1 0 1 1 X 0 ↑ | QN Q X X 0 1 ↑ | 0 1 X X 1 1 ↑ | 1 0	10 3k 11	JK	With scan test inputs
FJK2		J K CP CD | Q QN 0 0 ↑ 1 | Q QN 0 1 ↑ 1 | 0 1 1 0 ↑ 1 | 1 0 1 1 ↑ 1 | QN Q X X X 0 | 0 1	9	JK	With clear direct
FJK2S		J K TI TE CP CD | Q QN 0 0 X 0 ↑ 1 | Q QN 0 1 X 0 ↑ 1 | 0 1 1 0 X 0 ↑ 1 | 1 0 1 1 X 0 ↑ 1 | QN Q X X 0 1 ↑ 1 | 0 1 X X 1 1 ↑ 1 | 1 0 X X X X X 0 | 0 1	11 3K 12	JK	With scan test inputs, clear direct
FJK3		J K CP CD SD | Q QN 0 0 ↑ 1 1 | Q QN 0 1 ↑ 1 1 | 0 1 1 0 ↑ 1 1 | 1 0 1 1 ↑ 1 1 | QN Q X X X 0 1 | 0 1 X X X 1 0 | 1 0 X X X 0 0 | 1 1	10	JK	With clear direct set direct

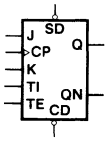
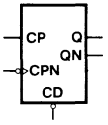
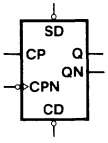
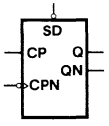
MACRO-CELL	LOGIC SYMBOL	FUNCTION	EQUIV. GATE COUNT	TYPE	REMARKS
FJK3S		J K TI TE CP CD SD | Q QN 0 0 X 0 ↑ 1 1 | Q QN 0 1 X 0 ↑ 1 1 | 0 1 1 0 X 0 ↑ 1 1 | 1 0 1 1 X 0 ↑ 1 1 | QN Q X X 0 1 ↑ 1 1 | 0 1 X X 1 1 ↑ 1 1 | 1 0 X X X X X 0 1 | 0 1 X X X X X 1 0 | 1 0 X X X X X 0 0 | 1 1	12 3K 11	JK	With scan test inputs, clear direct, set direct
FT2		CP CPN CD | Q QN ↑ ↓ 1 | QN Q X X 0 | 0 1	5	T	Without buffered clocks, with clear direct
FT3		CP CPN CD SD | Q QN ↑ ↓ 1 1 | QN Q X X 0 1 | 0 1 X X 1 0 | 1 0 X X 0 0 | 1 1	6	T	Without buffered clocks, with clear direct, set direct
FT4		CP CPN SD | Q QN ↑ ↓ 1 | QN Q X X 0 | 1 0	5	T	Without buffered clocks, with set direct

Table 11.1
Available Flip-Flops

11.2 Types of Flip-Flops

All D flip-flops change outputs on the positive rising clock edge. Their asynchronous inputs are active level-low. Some D flip-flops are available with all combinations of asynchronous inputs, and with scan test input. Parts FD1 through FD4 make useof a single phase clock. FD5 through FD8 require a dual-phase clock. Be sure to keep clock skew between CP and CPN at a safe level. These latter flip-flops (i.e., FD5 through FD8) have somewhat better set-up and delay time specifications than other D-type flip-flops since they do not have internal clock buffers.

All JK type flip-flops use a single-phase clock. They are available with various combinations of asynchronous inputs and scan-testability.

T flip-flops are available only with dual-phase clocks. They are used almost exclusively for ripple counters, as shown in Figure 11.1

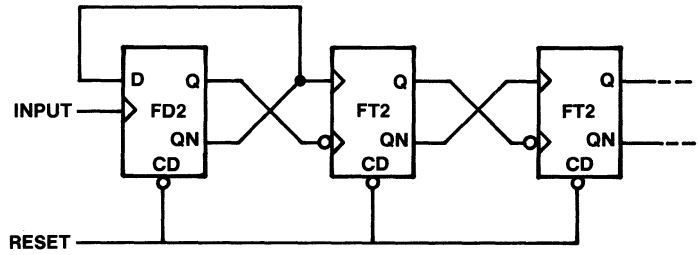


Figure 11.1
Ripple Binary Counter Using FT2 T Flip-Flops

11.3 Usage Limits

Heavy input loading on T flip-flops slows clocks down; this reduction in clock speed is called clock skew. Clock skew may cause unreliable circuit operation. In all but scan test flip-flops, the Q output (called the "independent output") changes first. The QN output (called the "dependent output") is driven by the Q output, and changes later. The skew between Q and QN outputs increases when the dependent output is heavily loaded. Minimize clock skew on ripple counters by not heavily loading QN outputs.

- Avoid Gated Clocks -- To remove gate delay as a clock skew source, avoid gated clocks. In the single-layer 3000 Series, the amount of polysilicon in clock lines is kept to a minimum during physical design to minimize skew. In the double-layer arrays, such as the 5000 and 7000 Series, you may eliminate clock skew altogether by using a large buffer (such as a BlI) to drive all clock inputs simultaneously.

- Use Scan Test Flip-flops to Simplify Layout -- Scan test flip-flops can be useful even if you aren't using scan testing. Because they have built-in input multiplexers, you can use them to store data from one of two sources. Figure 11.2 shows a shift register with a synchronous parallel load implemented with FD2S scan test flip-flops. Although the gate count is the same as it would be if you were using an external multiplexer, the number of nets and macrocells is reduced, thereby simplifying layout.

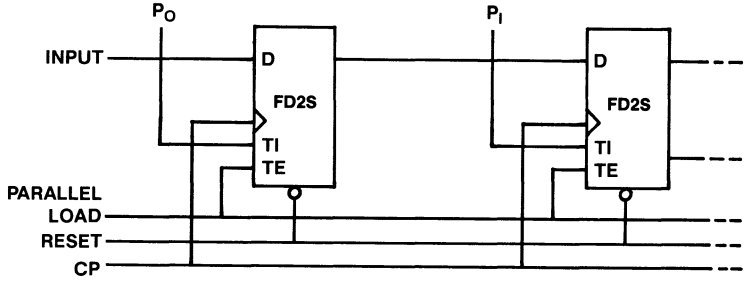


Figure 11.2
Scan Test Flip-Flops Used to Simplify
Design of Shift Register with Parallel Load

11.4 Calculate Setup and Hold Times

A flip-flop's setup time is the minimum time the data pin must be stable before the active edge of the clock pin occurs. The hold time is the minimum time the data pin must be stable after the active edge of the clock. Figure 11.3 illustrates this concept.

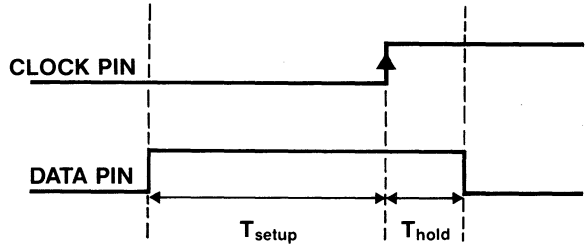


Figure 11.3
Definition of Setup and Hold Times

Both setup and hold times are a function of the internal propagation delays of the master portion of the flip-flop only. As such, they are independent of loading on the Q and QN outputs.

To calculate setup and hold times you must analyze the logical schematic representing the flip-flop. Figure 11.4 shows an FD1 flip-flop with each of its internal elements labeled.

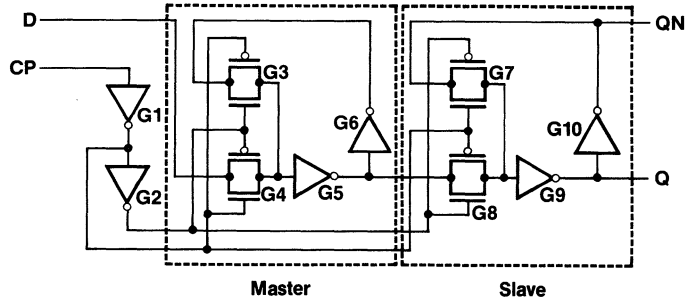


Figure 11.4
FD1 Macrocell

Assume initially that the clock pin is low. Therefore, transmission gate G4 is enabled and G3 is disabled. Any signal changes occurring on the data pin will affect the outputs of G5 and G6. The result is a change in signal state that is set up on input G3, as illustrated in Figure 11.5.

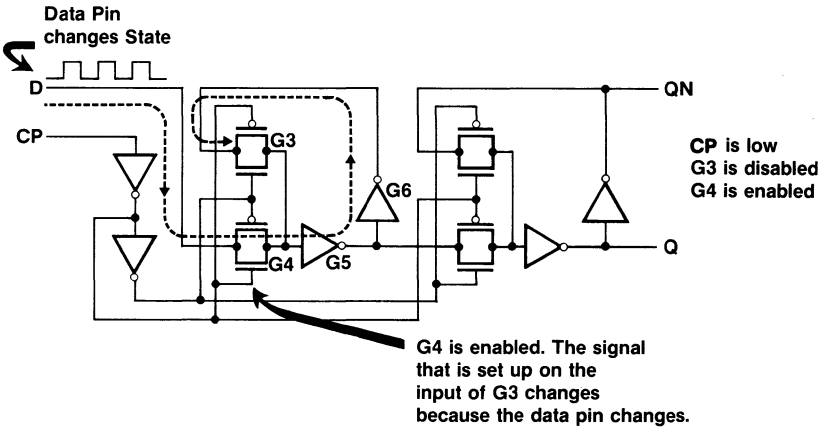


Figure 11.5
FD1 Flip-Flop with Clock Pin Low

When the clock pin goes high, G3 is enabled and G4 is disabled. As a result, the signal set up on G3's input is transmitted through G3 and G5 to the slave portion. Since G4 is disabled, any data changes occurring on the data pin are blocked out, as shown in Figure 11.6.

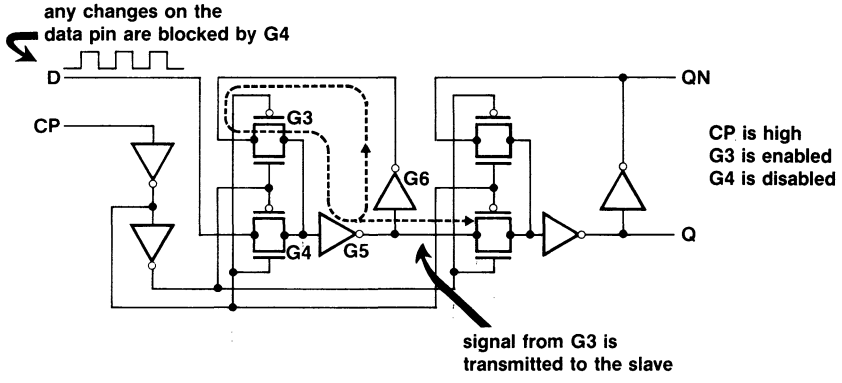


Figure 11.6
FD1 Flip-Flop with Clock Pin High

To meet setup-time requirements, the signal at G3's input must be stable prior to the time that G3 is enabled. Since any changes occurring on the data pin must go through G4, G5, and G6 before reaching G3, the setup time is the sum of the propagation delays through these latter 3 gates. However, the clock signal must go through G1 and G2 before enabling G3. Therefore, the setup time for the FD1 flip-flop is equal to the sum of the G4, G5, and G6 propagation delays minus the sum of the G1 and G2 propagation delays. The equation is:

$$Tsetup = (TpdG4 + TpdG5 + TpdG6) - (TpdG1 + TpdG2)$$

To meet hold-time requirements, the data pin must not change state before G4 is disabled. Since the clock signal must propagate through G1 and G2 before disabling G4, the hold time is equal to the sum of the G1 and G2 propagation delay. The equation is:

$$Thold = (TpdG1 + TpdG2)$$

Table 11.2 shows the setup and hold times for the FD1 flip-flop under various operating conditions.

	Nominal Condition	Worst-case Commercial	Worst-case Industrial	Worst-case Military
Tsetup	2.5	4.4	4.6	5.5
Thold	2.5	4.4	4.6	5.5

Table 11.2
Setup and Hold Times for the FD1 Flip-Flop

Table 11.3 shows the Setup and Hold Time (under nominal conditions) for all of the flip-flop macrocells in the 3000, 5000, and 7000 Series.

Cell	3000 Series Setup	3000 Series Hold	5000 Series Setup	5000 Series Hold	7000 Series Setup	7000 Series Hold
FDA	-	-	3.0ns	2.0ns	1.5ns	1.0ns
FD1	2.6	2.8	2.5ns	2.5ns	1.5ns	1.0ns
FD1S	6.7	1.7	9.1ns	*	4.4ns	*
FD2	2.7	2.5	2.5ns	2.5ns	1.5ns	1.0ns
FD2S	6.7	1.7	9.1ns	*	4.4ns	*
FD2TS	-	-	2.5ns	2.5ns	1.5ns	1.0ns
FD3	2.8	2.6	2.5ns	2.5ns	1.5ns	1.0ns
FD3S	6.7	1.7	9.1ns	*	4.4ns	*
FD4	2.7	2.7	2.5ns	2.5ns	1.5ns	1.0ns
FD4S	6.7	1.7	9.1ns	*	4.4ns	*
FD5	4.6	0	5.0ns	0	2.5ns	0
FD5S	10.7	*	11.1ns	*	5.4ns	*
FD6	5.2	0	5.0ns	0	2.5ns	0
FD6S	10.7	*	11.1ns	*	5.4ns	*
FD7	5.2	0	5.0ns	0	2.5ns	0
FD7S	10.7	*	11.1ns	*	5.4ns	*
FD8	5.0	0	5.0ns	0	2.5ns	0
FD8S	10.7	*	11.1ns	*	5.4ns	*
FJKA	-	-	6.2ns	*	3.7ns	*
FJK1	7.4	0.7	6.2ns	*	3.7ns	*
FJK1S	10.7	*	12.6ns	*	5.9ns	*
FJK2	8.4	0.7	6.2ns	*	3.7ns	*
FJK2S	10.7	*	12.6ns	*	5.9ns	*
FJK3	8.2	0.7	6.2ns	*	3.7ns	*
FJK3S	10.7	*	12.6ns	*	5.9ns	*
FT2	5.4	0	5.0ns	0	2.5ns	0
FT3	5.4	0	5.0ns	0	2.5ns	0
FT4	5.4	0	5.0ns	0	2.5ns	0

* Note: hold time may be negative.

Table 11.3
Setup and Hold Times for All Flip-Flops

11.5 Clock Pulse Width

To ensure proper flip-flop operation, be sure that clock signals meet minimum positive and negative clock pulse-width conditions.

While the clock pin is low (see Figure 11.5) the signal from the data pin propagates through G4, G5, G6, and is set up on the input of G3. The clock signal must remain low during this period so that the master can latch in the correct data. The minimum negative pulse width is:

$$T(pw-) = (TpdG4 + TpdG5 + TpdG6)$$

Since the master drives no external loads, the minimum negative pulse-width is independent of the loading on the Q and QN outputs.

While the clock is high, data is transferred from master to slave. The data signal propagates through G8, G9, and G10 and is set up on the input of G7, as illustrated in Figure 11.7.

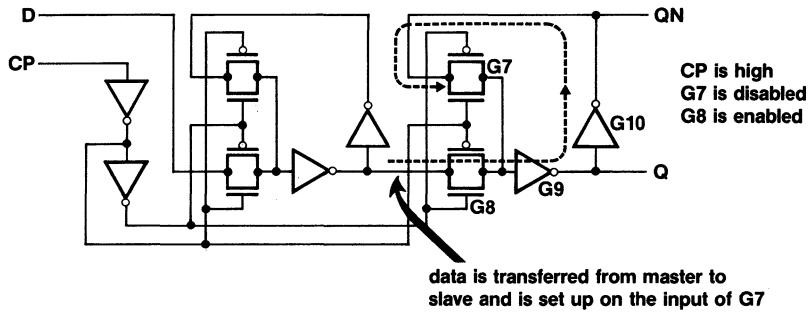


Figure 11.7
FD1 Minimum Positive Clock Pulse Width

The minimum positive clock pulse width is:

$$T(pw+) = (TpdG8 + TpdG9 + TpdG10)$$

The clock signal must remain high during this period, allowing the slave to latch in the correct data.

Unlike the master, the slave drives external loads, i.e., G9 drives the Q output and G10 drives the QN output. If Q drives a high fanout line, then the propagation delay of G9 increases, increasing the minimum positive clock pulse-width. The same argument applies to G10 and the QN output. Table 11.4 shows the minimum clock pulse-width for the FD1 flip-flop with a fanout of zero.

		NOM	WCCOM	WCIND	WCMIL
Tpw+	Data=0	5	8.7	9.2	11.1
	Data=1	5	8.7	9.2	11.1

Table 11.4
Minimum Clock Pulse Width for the FD1 Flip-Flop

The minimum positive clock pulse-width is a function of loading on the Q and QN outputs. In most applications, you must buffer both Q and QN outputs with an IVA and/or an IVP before they can drive a high fanout line, as indicated in Figure 11.8.

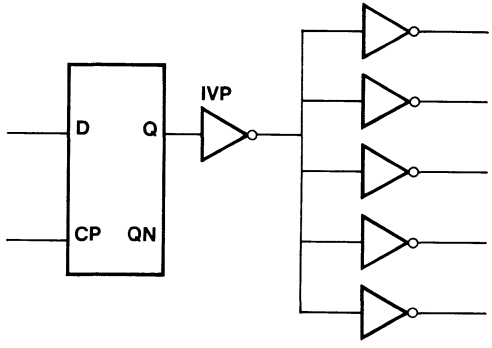


Figure 11.8
Buffer Q or QN Outputs
Before Driving a High Fanout Line

11.6 Latches

Latches provide size- and speed-advantages over flip-flops. Four D-type latches are available:

- LD1, with active level-high control (gate) input
- LD2, with active level-low control (gate) input
- LD3, a gated D latch with active level-high and asynchronous clear.
- LD4, a gated D latch with active level-low and asynchronous clear.

LD1 and LD2 require three gates; LD3 and LD4 require four gates.

Two special purpose scan test latches, the LS1 and the LS2, are available for classic Level Scan Sensitive Design. You may also use the LS1 when you require a two-input multiplexer. Note that only one control (gate) input may be high at a time.

Use the RAM1 macrocell to configure dual port register/memory requiring separate read and write addressing. RAM1 consists of a gated D latch coupled with a separately addressable tristate output.

Table 11.5 lists all of the latches and their major characteristics:

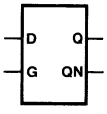
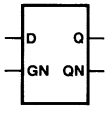
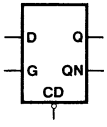
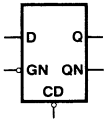
LATCH NAME	LOGIC SYMBOL	FUNCTION	EQUIV. GATE COUNT	TYPE	REMARKS
LD1		D G | Q QN 0 1 | 0 1 1 1 | 1 0 X 0 | Q QN	3	D	Active level high, control gate input
LD2		D GN | Q QN 0 0 | 0 1 1 0 | 1 0 X 1 | Q QN	3	D	Active level low control gate input
LD3		D G CD | Q QN 0 1 1 | 0 1 1 1 1 | 1 0 X 0 1 | Q QN X X 0 | 0 1	4	D	Active level high with clear direct
LD4		D GN CD | Q QN 0 0 1 | 0 1 1 0 1 | 1 0 X X 0 | 0 1 X 1 1 | Q QN	4	D	Active level low with clear direct

Table 11.5
Available Latches

For speed-sensitive paths, a maximum fanout of four standard loads should be bused. For higher fanouts, on-chip buffers will generally provide increased speed.

Figure 12.1 tabluates available on-chip buffers. The input loading is shown in terms of standard loads; one standard load is defined as one N and one P transistor, i.e., the number comprising a simple inverter. Output Drive is also shown in terms of a simple inverter; an output drive of 4 will have one fourth the output impedance of a simple inverter. Note that buffers such as the BlI use an output buffer internally; one I/O pad is sacrificed. The BTS4 is an internal tri-state buffer; if all buffers are off, the node will float and partially turn on, i.e., enable, receiving elements, causing dc power supply current to flow. Each internal bus must be driven by one and only one tristate driver at all times.

TYPE	DESIG-NATION	INPUT LOADING/OUTPUT DRIVE (1) 3000 SERIES	5000 SERIES	7000 SERIES	(2) EQUIV. GATES	REMARKS
Balanced Inverter	IVA	1.5/1.5	1.5/1.5	1.5/1.5	1	One N, Two P Transistors (4)
Power Inverter	IVP	2/2	2/2	2/2	1	Two Parallel Inverters
Power Inverter	B1A	---	3/3	3/3	2	Two N, Four P Transistors (4)
Power Inverter	B2A	---	6/6	6/6	4	Four N, Eight P Transistors (4)
Power Inverter	B5I	3/3	3/3	3/3	2	Three Parallel Inverters
Power Inverter	B4I	4/4	4/4	4/4	2	Four Parallel Inverters
Non-Inverting Buffer	B2I	1/2	1/3	1/3	2	Inverted Output Also Available
Non-Inverting Buffer	B3I	2/2	2/2	2/2	2	Inverted Output Also Available
Non-Inverting Buffer	B1I	3/8	3/12	3/12	2(3)	B1 Output Buffer Used Internally
Non-Inverting Buffer	BTS4	2/1	2/1	2/1	3	Tri-State Internal Bus Driver

Notes:

(1) Input Loading is one N-P pair, i.e. the same as that of a simple inverter.
Output drive is defined in terms of a simple inverter.
(2) Equivalent gates for 5000 Series; others may differ.
(3) Requires output driver and pad
(4) Symmetric rise and fall propagation delay cells

Figure 12.1
On-Chip Buffers

13.1 Input Buffer Components

Signals coming from off-chip go through an input buffer made up of the following:

- an input protection circuit
- an optional voltage translator (TTL or Schmitt trigger)
- an input buffer to drive the signal on-chip
- an optional pull-up or pull-down resistor to increase noise immunity

The input protection circuit consists of a series resistor with diodes returned to VSS and VDD (Figure 13.1). The series resistor introduces a small R-C (resistance-capacitance) delay, typically of 1 ns.

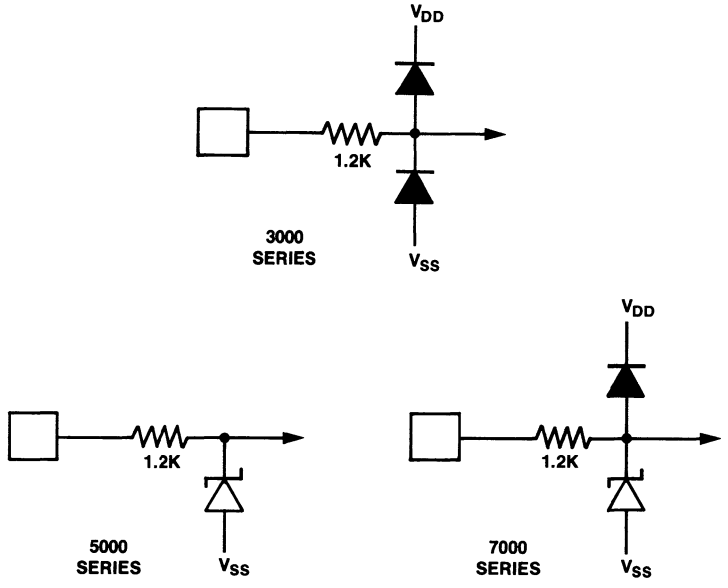


Figure 13.1
Input Protection Circuits (typical resistances shown)

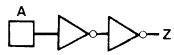
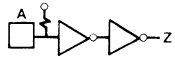
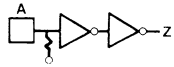
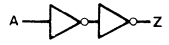
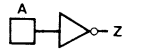
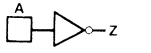
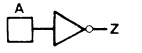
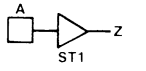
Two voltage translators are available: a Schmitt trigger and a TTL input translator. The Schmitt trigger typically exhibits 1.5 volts of hysterisis. (Hysterisis prevents the element from reacting to noise by the inclusion of two thresholds.) Use the Schmitt trigger for noisy or slowly changing inputs. The TTL input translator accepts standard TTL worst-case inputs of 0.8 VIL MAX and 2.0 VIH MIN (2.25 VIH MIN for industrial and military temperature ranges). Because TTL input translators decrease noise immunity and add propagation delay, you may use external pull-up resistors on TTL signals to eliminate the need for a translator.

If you do not use voltage translators, the circuit will exhibit standard CMOS input specifications of 1.3V VIL MAX and 3.5V VIH MIN.

You may specify pull-up or pull-down resistors to provide noise immunity to an input. The resistors hold an input at logic one or logic zero when the logic is in the steady state. The resistors, whose typical values are 50K ohms in the 3000 and 7000 Series, and one megohm on the 5000 Series, are intended only to reduce noise. Do not use them to pull a node up or down, except nodes that are in steady state. Refer to individual data sheets for more information.

13.2 Characteristics

Table 13.1 details input buffer macrocells. Each input buffer uses one pad location. For high fan-in applications, put an internal buffer after the input buffer to minimize delay.

MACROCELL	NO. I/O CELLS	NO. INTERNAL CELLS			LOGIC SYMBOL	REMARKS
		3K	5K	7K		
IBUF	1	1	0	0		Input pad with buffer for CMOS input
IBUFU	1	2	0	0		Input pad with pull up and buffer for CMOS input
IBUFD	1	2	0	0		Input pad with pull down and buffer for CMOS input
IBUFI	0	2	3	3		Buffer for bidirect CMOS input
IBUFN	1	-	-	0		Inverting pad with buffer for CMOS input
ICK1	2	-	-	0		Inverting clock driver
ICK2	3	-	-	0		Inverting clock driver
SCHMDT1	1	3	3	3		Input pad with Schmitt trigger
SCHMDT2	1	4	4	4		Input pad with inverting Schmitt trigger

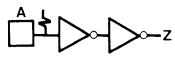
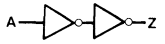
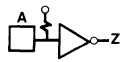
MACROCELL	NO. I/O CELLS	NO. INTERNAL CELLS			LOGIC SYMBOL	REMARKS
		3K	5K	7K		
TLCHT	1	0	0	0		Input pad with buffer for TTL input
TLCHTI	0	2	3	3		Buffer for bidirect TTL input
TLCHN	1	-	-	0		Inverting input pad with buffer for TTL input

Table 13.1
Input Buffer Summary

14.1 Output Buffer Characteristics

You may configure output buffers in standard, tristate, or open drain form. (An open drain is an output that can either float or go low, but can never go high.) You may also configure output drive to match system requirements. High drive buffers may use more than one pad, decreasing available I/O pads, and increasing VDD/VSS requirements. Table 14.1 tabulates available buffers, their worst case sinking currents at 0.4 volts, the number of pads each buffer uses, and the number of internal gates each buffer uses. Internal gates are used to form a predriver; in general, output buffers use both internal gates and one or more pads.

Input/Output (bidirectional) buffers are also listed in Table 14.1. By putting the buffer into the high impedance state, you may use the depicted pin as an input.

		3000 Series					5000 Series					7000 Series				
	Buffer Name	Current Load (ma) IOL	(ma) IOH	#I/O Slots	DT	Gate Count	Current Load (ma) IOL	(ma) IOH	#I/O Slots	DT	Gate Count	Current Load (ma) IOL	(ma) IOH	#I/O Slots	DT	Gate Count
UNIDIRECT	B14	----------Not Available----------					1	-1	1	.25	1	1	-1	1	.25	1
	B18	----------Not Available----------					2	-2	1	.5	1	2	-2	1	.5	1
	B1	1.6	-1.6	1	1	1	4	-4	1	1	2	4	-4	1	1	2
	B1OD	1.6	----	1	1	1	4	----	1	1	1	4	----	1	1	1
	B1I	Internal Buffer		1	1	1	Internal Buffer		1	1	2	Internal Buffer		1	1	2
	B2	3.2	-3.2	2	2	2	8	-8	2	2	4	8	-8	2	2	4
	B2OD	3.2	----	2	2	2	8	----	2	2	2	8	----	2	2	2
	OSC2	Oscillator Cell		3	2	1	Oscillator Cell		3	2	0	Oscillator Cell		3	2	0
	B3	4.8	-4.8	3	3	3	12	-12	4	3	2	12	-12	4	3	2
	B3OD	4.8	----	3	3	3	12	----	3	3	3	12	----	3	3	3
3STATE	BTS14	----------Not Available----------					1	-1	1	.25	5	1	-1	1	.25	3
	BTS18	----------Not Available----------					2	-2	1	.5	5	2	-2	1	.5	3
	BTS1	1.6	-1.6	1	1	4	4	-4	1	1	7	4	-4	1	1	7
	BTS2	3.2	-3.2	2	2	5	8	-8	2	2	8	8	-8	2	2	8
	BTS3	4.8	-4.8	3	3	6	12	-12	3	3	11	12	-12	3	3	11
	BTS6	----------Not Available----------					4	-4	2	1	7	4	-8	2	1	7
BIDIRECT	BTS7	1.6	-1.6	1	1	4	4	-4	1	1	7	4	-4	1	1	7
	BTS7D	----------Not Available----------					4	-4	1	1	7	4	-4	1	1	7
	BTS7LO	----------Not Available----------					4	----	1	1	4	4	----	1	1	4
	BTS7OD	1.6	----	1	1	4	4	----	1	1	1	4	----	1	1	1
	BTS7U	1.6	-1.6	1	1	4	4	-4	1	1	7	4	-4	1	1	7
	BTS78	----------Not Available----------					2	-2	1	.5	5	2	-2	1	.5	3
	BTS8	3.2	-3.2	2	2	5	8	-8	2	2	8	8	-8	2	2	8
	BTS8U	3.2	-3.2	2	2	5	8	-8	2	2	8	8	-8	2	2	8
	BTS9	4.8	-4.8	3	3	6	12	-12	3	3	11	12	-12	3	3	11
	BTS9D	----------Not Available----------					12	-12	3	3	11	12	-12	3	3	11
	BTS9U	4.8	-4.8	3	3	6	12	-12	3	3	11	12	-12	3	3	11

Note: IOL, IOH current ratings are for worst-case commercial conditions.
IOL, IOH for worst-case military is 3.6ma for the 5K and 7K.

Table 14.1
Output Buffer Summary

14.2 Propagation Delays

Consider propagation delay when choosing output buffers. Output-buffer propagation delay is a function of buffer type, capacitive load, and type of element being driven. When driving CMOS chips, buffer delays are normally measured from their inception to the time at which the signal achieves the CMOS threshold of 2.5 volts. When driving TTL or CMOS with TTL input translators, the delays are normally measured to the TTL threshold from their inception to the time at which the signal achieve a CMOS threshold of 1.4 volts. The output buffer delays shown in the macrocell models are measured to a 1.4 volt threshold.

Propagation delays are the sum of a fixed predriver delay and a load-variable output-driver delay. High drive buffers such as B2 and B3 have larger fixed delays, but lower total delays into high capacitive loads. For example, in the 5000 Series, a B1 (4.8 madc) has an average delay of 3.7 ns driving 15 pF, 12.1 ns when driving 100 pF. The hefty B3 (14.4 madc) has an average propagation delay of 4.7 ns driving 15 pF, 7.65 ns driving 100 pF. Clearly, the B1 is faster when driving light loads.

14.3 Buffer Drive

Use the lowest drive buffer that meets your specifications. Buffer drive has an impact on the number of required power pins. In general, you should select the lowest-drive buffer meeting your ac and dc drive specifications for each output pin. This minimizes gates, pads, and power pins, as well as system noise.

15.1 Considerations About Counters

Keep the following considerations in mind when you are designing counters.

- Synchronous Clear -- Use synchronous clear when you want a counter to return to the initial state after detecting a final state. This scheme can be used with counters of fixed or variable modulos. Reference macrofunctions CB4C and SR45 are examples of synchronous clear counters.

- Synchronous Parallel Load -- Use synchronous parallel load when you want a counter to enter a predefined state after decoding the terminal state. Like synchronous clear, this scheme can also be used in counters with fixed or variable modulos. Synchronous load counters use more gates than synchronous clear counters, and thus operate more slowly. Reference macrofunction SR45 is an example of a synchronous parallel load counter.

- Expandable Counters -- Many counters are expandable to increase the number of stages. Ripple carry between stages may increase propagation delay. Reference macrofunctions CUD41, CB41, and M160D are examples of expandable counters.

- Shift Counters -- Shift counters are both fast and compact. Reference macrofunctions CM8SR and C5LSR are examples of shift counters.

- Binary Counters -- Binary counters simplify arithmetic manipulations on counter states. Reference macrofunctions CM8B, CB4C, CB4F, CB41, and CUD41 are examples of binary counters.

- Ripple Binary Counters -- Ripple counters have the lowest gate count per bit, but their asynchronous nature and long ripple delay limit their use to special purpose applications such as pre-scalers, where their limitations are acceptable. Reference macrocell CM8BR is an example of a ripple binary counter. A modulo number is equal to the number of signals a storage element will receive before it recycles; you can create ripple binary counters in any modulo by using CMBR an an example and following the four steps ennumerated below:

  1. String n FT2 flip-flops together, where 2 EXP n > desired modulo.

2. NAND the 1's of the terminal count into an LD2 latched with CP. Note: The NAND must be valid, and the LD2 set up before the next low-high transition of CP.

3. AND the LD2 (QN output) with CP.

4. NOR Step 3 with CD and use to clear all FT2 flip-flops.

- Synchronous Counters -- In synchronous counters, all outputs switch on the same active edge of the clock. They are faster than asynchronous counters. Reference macrofunctions CM8B and CB4C are examples of synchronous counters.

- Gray Counters -- Use gray counters when you want a single bit change on each clock pulse, or to accomodate high clock rates. Gray counter decoded states do not generate glitches. Reference macrofunction C3G is an example gray counter.

- Johnson Counters -- Johnson counters are shift registers with feedback; n flip-flops within a Johnson counter will provide modulo 2n counts. They are fast because there are no gates between flip-flops. Any state may be decoded with a two-input NAND or NOR for glitch-free gate output. Reference macrofunction CM8J is a Johnson counter.

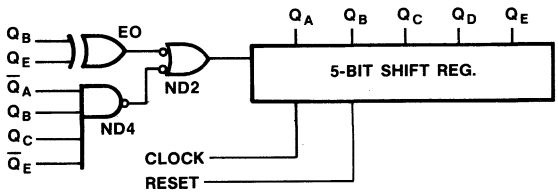
- Linear Feedback Counters -- Sometimes called pseudo-random or polynomial counters, linear feedback counters are shift registers with one or more exclusive OR feedbacks. Linear feedback counters exhibit a modulo of 2^{n-1} for n flip-flops, as opposed to binary counters, which exhibit 2^n states.

Linear feedback counters have a number of advantages. They are fast, with only the delay of exclusive ORs between flip-flops. They have the lowest gate count per state of any synchronous counter. And they have the following additional properties, which are sometimes necessary or desirable:

- Count sequences satisfy many random number criteria.
- They may be used as pseudo random-number generators.
- They may be used to encrypt and decrypt transmission data.
- They may be used to generate check sums or CRC characters.
- They have strong auto-corrolation properties.

The disadvantages of linear-feedback counters are their unfamiliarity relative to other counters, and the difficulty of decoding their random count sequences. Linear feedback shift counters are advantageous for use as high modulo counters where only a few states must be decoded.

C5LSR, a 5-bit modulo 31 linear feedback counter, and its state table are shown in Figure 15.1.



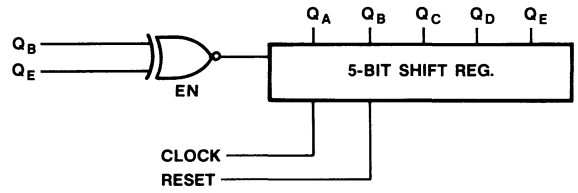
	Q_A	Q_B	Q_C	Q_D	Q_E	OLD STATE	NEW STATE	
	0	0	0	0	0	0	0	
	1	0	0	0	0	1	1	
	1	1	0	0	0	2	2	
	0	1	1	0	0	3	3	
→	0	0	1	1	0	4		
THESE	1	0	0	1	1	5	STATES TO	
STATES	0	1	0	0	1	6	BE DELETED—	
DIFFER IN	1	0	1	0	0	7	BECOME DON'T	
THEIR FIRST	1	1	0	1	0	8	CARE	
BIT ONLY	0	1	1	0	1	9		
→	1	0	1	1	0	10	4	
	1	1	0	1	1	11	5	
	1	1	1	0	1	12	6	
	1	1	1	1	0	13	7	
	0	1	1	1	1	14	8	
	1	0	1	1	1	15	9	
	0	1	0	1	1	16	10	
	1	0	1	0	1	17	11	
	0	1	0	1	0	18	12	
	0	0	1	0	1	19	13	
	0	0	0	1	0	20	14	
	1	0	0	0	1	21	15	
	0	1	0	0	0	22	16	
	0	0	1	0	0	23	17	
	1	0	0	1	0	24	18	
	1	1	0	0	1	25	19	
	1	1	1	0	0	26	20	
	0	1	1	1	0	27	21	
	0	0	1	1	1	28	22	
	0	0	0	1	1	29	23	
	0	0	0	0	1	30	24	
	0	0	0	0	0	0	0	

Figure 15.1
C5LSR Modulo 31 Linear Feedback
Shift Counter Generic Macrofunction

15.2 Truncation

You can "truncate" a Linear Feedback shift counter to any required modulo with a few extra gates. For example, suppose a modulo 25 counter is required. The count sequence of the base modulo 31 counter shows that 6 counts can be truncated by forcing QA to a one when the state $\overline{QA}$ QB QC $\overline{QD}$ $\overline{QE}$ is

attained, thereby bypassing six states, as shown in Figure 15.2. This would normally require a five-input gate, but the state $\overline{QA}$ QB QC $\overline{QD}$ $\overline{QE}$ has been bypassed, and is now in a "don't-care" state. $\overline{QE}$ can be deleted, and the gate becomes an ND4. You can obtain any modulo through sequence truncation by modifying only the first bit of a count state. However, the extra gate introduces a speed penalty.



Q_A	Q_B	Q_C	Q_D	Q_E	STATE
0	0	0	0	0	0
1	0	0	0	0	1
1	1	0	0	0	2
0	1	1	0	0	3
0	0	1	1	0	4
1	0	0	1	1	5
0	1	0	0	1	6
1	0	1	0	0	7
1	1	0	1	0	8
0	1	1	0	1	9
1	0	1	1	0	10
1	1	0	1	1	11
1	1	1	0	1	12
1	1	1	1	0	13
0	1	1	1	1	14
1	0	1	1	1	15
0	1	0	1	1	16
1	0	1	0	1	17
0	1	0	1	0	18
0	0	1	0	1	19
0	0	0	1	0	20
1	0	0	0	1	21
0	1	0	0	0	22
0	0	1	0	0	23
1	0	0	1	0	24
1	1	0	0	1	25
1	1	1	0	0	26
0	1	1	1	0	27
0	0	1	1	1	28
0	0	0	1	1	29
0	0	0	0	1	30
0	0	0	0	0	0

Figure 15.2
Modulo 31 Linear Feedback Shift
Counter Truncated to Modulo 25

A manual technique for truncation is:

- Simulate the untruncated Linear Feedback shift counter and print the states in a column.
- Cut a piece of paper to a length corresponding to the number of states to be deleted minus 1 in the simulation print-out column.
- Move the paper up and down, looking for two states which differ by only the first bit.
- Detect the state prior to the state to be modified, and force the first bit to the appropriate opposite state. The bypassed states become don't-cares; they may simplify the state detection gate.

Both Johnson and Linear Feedback counters have lock-up states from which they will not exit. This is normally not a problem, since all counters must be initialized for testing. Use the chip-initialization capability to power-on reset each time power is brought up, so that the counter is initialized with no danger of entering a lock-up state. If power is brought up without initializing to a known state, you must force the counters out of lock-up states.

The lock-up state of a Linear Feedback shift counter is the all-ones state. You can protect against lock-up by detecting the all-ones state and forcing a flip-flop input low.

ADDER Network Examples

Several carry look-ahead ADDERS have been assembled as macrofunctions for the convenience of designers. CLA1 and CLA2 are 4-bit ADDERS with and without least significant nibble (1/2 a byte), while FA4 is a 4-bit binary full ADDER. Figures 16.1 and 16.2 below show how 4-bit fast ADDERS can be constructed using the FA4 macrofunction.

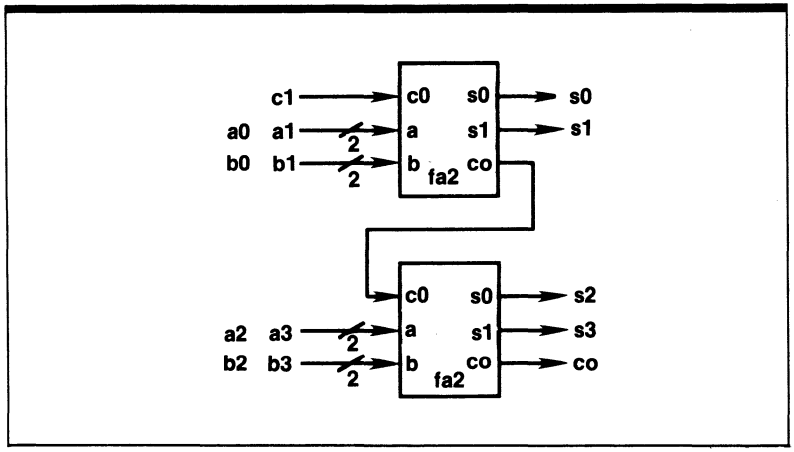


Figure 16.1
Using two FA2 Macrofunctions
to Form a 4-Bit Fast ADDER

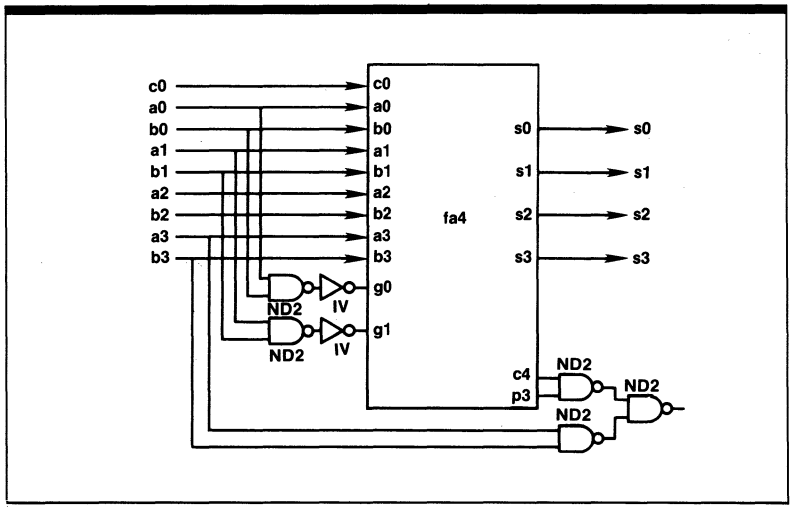


Figure 16.2
Using the FA4 Macrofunction
to Form a 4-Bit Fast ADDER

As shown above in Figure 16.1, if the ADDER is constructed using two FA2 macrofunctions, the number of gates used will be 40. The longest delay path will be up to 29 ns (nominal 5000 Series). If the FA4 macrofunction is used, the longest delay path is reduced to 21 ns, but it will occupy 51 gates.

Figure 16.3 shows the simulation results for both networks. The input and output signals are displayed (until stable) for 8 input patterns using an arbitrary 100 ns clock cycle.

DELAY VALUE GENERATED
FROM TWO FA2 TO BUILD
A 4 BIT ADDER

```
(((((((((( (((((
CABABABAB SSSSC
000112233 01234
)))))))))) )))))
INPUTS    OUTPUTS
```

	TIME		
	0	000000000	XXXXX
1st	5	000000000	0XXX0
PATTERN	9	000000000	0X0X0
	14	000000000	00000
	100	111111111	00000
	103	111111111	10000
2nd	108	111111111	11010
	109	111111111	11011
	117	111111111	11111
	200	000000000	11111
	202	000000000	01111
3rd	205	000000000	01110
	209	000000000	01010
	214	000000000	00000
	300	101010101	00000
	303	101010101	10000
	306	101010101	00000
4th	307	101010101	00110
	319	101010101	00010
	324	101010101	00000
	329	101010101	00001
	400	000000000	00001
	403	000000000	10001
	405	000000000	00000
5th	406	000000000	01110
	409	000000000	01010
	414	000000000	00000
6th	500	001010101	00000
	507	001010101	11110
7th	600	000000000	11110
	605	000000000	00000
	700	110101010	00000
	703	110101010	10000
	706	110101010	00000
8th	707	110101010	00110
	719	110101010	00010
	724	110101010	00000
	729	110101010	00001
	800	111001100	00001
9th	805	111001100	00000
	806	111001100	11110

DELAY VALUE GENERATED
FROM FA4 TO BUILD A
4 BIT ADDER

```
(((((((((( (((((
CABABABAB SSSSC
000112233 01234
)))))))))) )))))
INPUTS    OUTPUTS
```

	TIME		
	0	000000000	XXXXX
	5	000000000	0XXXX
1st	7	000000000	0XXX0
PATTERN	11	000000000	00XX0
	14	000000000	000X0
	23	000000000	00000
	100	111111111	00000
	103	111111111	10000
2nd	104	111111111	10001
	113	111111111	11101
	114	111111111	11111
	200	000000000	11111
	202	000000000	01111
	204	000000000	01110
3rd	211	000000000	00110
	214	000000000	00010
	219	000000000	00000
	300	101010101	00000
	303	101010101	10000
	306	101010101	00000
4th	307	101010101	00110
	308	101010101	01110
	311	101010101	00110
	316	101010101	00010
	319	101010101	00000
	321	101010101	00001
	400	000000000	00001
5th	403	000000000	10001
	405	000000000	00001
	406	000000000	0XX11
	407	000000000	00010
	408	000000000	00000
	500	001010101	00000
6th	507	001010101	10110
	508	001010101	11110
7th	600	000000000	11110
	605	000000000	00000
	700	110101010	00000
8th	703	110101010	10000
	706	110101010	00000
	707	110101010	00110

Figure 16.3
Comparison of Delay Results Between the FA2 and FA4 to Form a 4-Bit ADDER

An 8-bit fast ADDER can be constructed using CLA1 and FA4 as shown below in Figure 16.4.

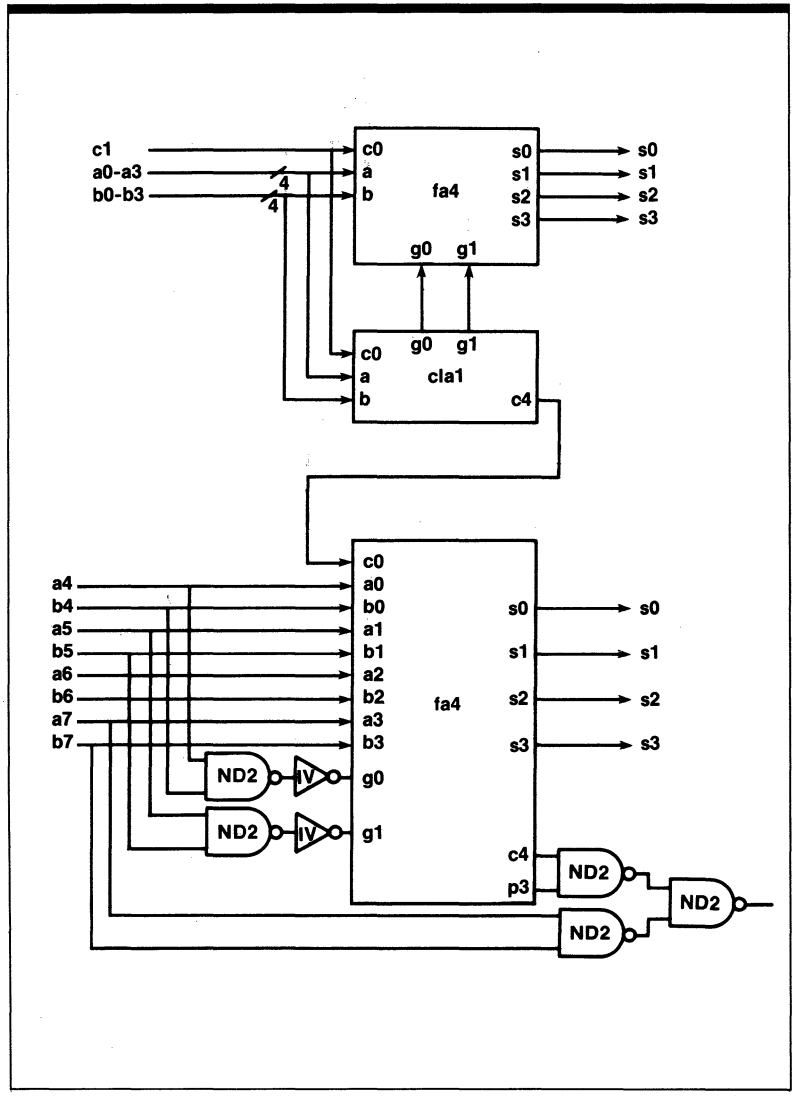


Figure 16.4
Using the CLA1 and FA4 Macrofunctions
to Form an 8-Bit Fast ADDER

This configuration uses 117 gates and the longest delay path is up to 24 ns (nominal 5000 Series) as shown below in Figure 16.5.

```
                    THE LONGEST DELAY PATH IS UP TO 24NS
                    AT NOMINAL SIMULATION

                    (((((((((((((((( (((((((((
                    CAAAAAAAABBBBBBBB SSSSSSSSC
                    0012345670123456 7 012345670
                    ))))))))))))))) )))))))))
                    INPUTS            OUTPUTS

          TIME

             0 0000000000000000 XXXXXXXXX
             5 0000000000000000 0XXXXXXXX
             7 0000000000000000 0XXXXXXX0
            11 0000000000000000 0XXXX0XX0
1st         12 0000000000000000 00XXX0XX0
PATTERN     15 0000000000000000 000XX00X0
            17 0000000000000000 000X000X0
            22 0000000000000000 0000000X0
            23 0000000000000000 000000000

          1000 1111111111111111 000000000
          1003 1111111111111111 100000000
2nd       1004 1111111111111111 100000001
          1013 1111111111111111 100101101
          1014 1111111111111111 111101111
          1017 1111111111111111 111111111

          2000 1000000011111111 111111111
          2004 1000000011111111 111111110
          2006 1000000011111111 010001000
3rd       2007 1000000011111111 000000000
          2008 1000000011111111 000000001
          2015 1000000011111111 000000X01
          2016 1000000011111111 000000001

          3000 0000000000000000 000000001
          3003 0000000000000000 100000001
          3005 0000000000000000 000000001
          3006 0000000000000000 0XXX11111
4th       3007 0000000000000000 000011110
          3010 0000000000000000 000010110
          3015 0000000000000000 000010010
          3016 0000000000000000 000000010
          3017 0000000000000000 000000000

          4000 1111111100000000 000000000
          4003 1111111100000000 100000000
          4006 1111111100000000 000000000
          4007 1111111100000000 001110110
5th       4008 1111111100000000 011111110
          4011 1111111100000000 001111110
          4016 1111111100000000 000101110
          4018 1111111100000000 000001110
          4021 1111111100000000 000000010
          4022 1111111100000000 000000000
          4024 1111111100000000 000000001

          5000 0000000000000000 000000001
          5003 0000000000000000 100000001
          5005 0000000000000000 000000001
6th       5006 0000000000000000 0XXX11111
          5007 0000000000000000 000011110
          5010 0000000000000000 000010110
          5015 0000000000000000 000010010
          5016 0000000000000000 000000010
```

Figure 16.5
Delay Results Using the CLA1 and FA4 Macrofunctions to Form an 8-Bit Fast ADDER

A similar network for a 16-bit ADDER has been coded as a FA16 macrofunction, as shown below in Figure 16.6. CLA1 is used for the lowest four bits only and CLA4 is used for the higher bits and faster propagation.

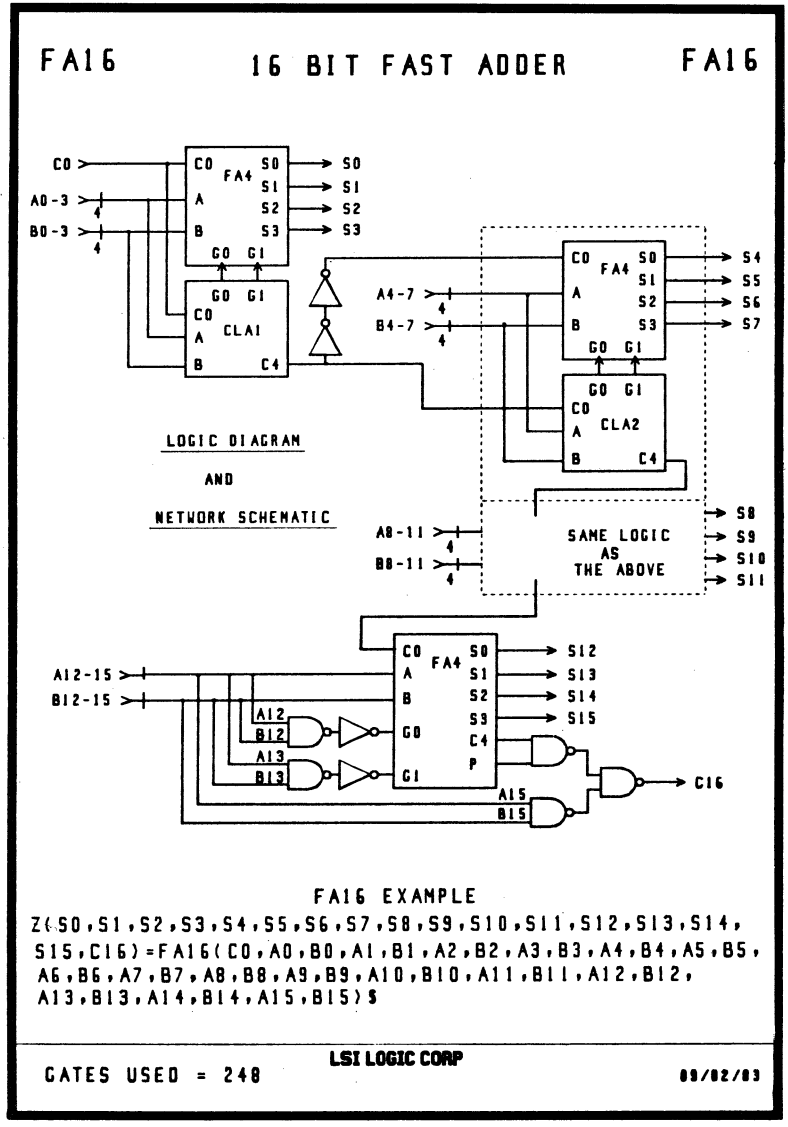


Figure 16.6
Using the FA16 Macrofunction
to Form a 16-Bit Fast ADDER

It uses 248 gates and the longest delay path is 34 ns (nominal 5000 Series), as shown below in Figure 16.7.

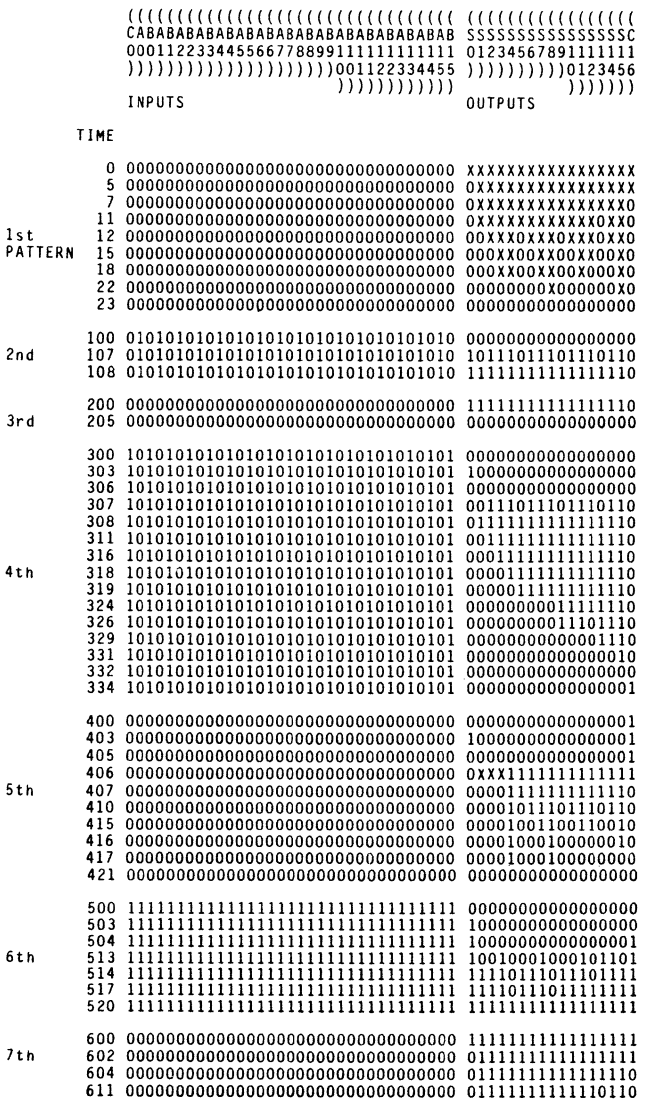


Figure 16.7
Delay Results Using the FA16 Macrofunction to Form a 16-Bit Fast ADDER

This page explains how to read the macrocell model catalog and annotates the AOl macrocell model in Figure 17.1.

1. The macrocell's name appears in the upper-left and upper-right corners.

2. The macrocell's function is provided on the same line as the macrocell's name.

3. The macrocell's logic diagram is shown.

4. The electrical schematic is also shown.

5. A truth table is provided. Not all macrocells will have truth tables.

6. A table of typical propagation delays for various fanouts (or load capacity in buffer outputs) is provided, so that you can estimate the critical path delays. The delay values provided are based on nominal conditions. You may extrapolate larger fanouts and/or capacitances from these values.

7. The number of equivalent gates required to implement the macrocell is given.

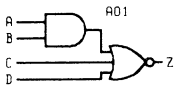
8. Input loading is shown for every input pin to the macrocell. The order of the values follows that in the coding syntax equation shown in item 9. The input loading factor of higher capacitance inputs is greater than one. You should take such extra capacitance into account when you calculate propagation delays.

9. The coding syntax in TDL format is shown. This particular syntax is used by the LDS System logic simulator, not by the workstation simulator.

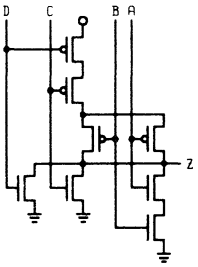
10. Rise and fall delays fixed in the workstation Software Data Book are shown. The values are worst-case commercial (70 degrees C, 4.5 V, 40% process.) The LSI LOGIC Design Verifier on the mainframe or workstation will calculate more precise delays based on fanout, operating conditions, and manufacturing process variations.

AO1 (1) 2AND INTO 3NOR (2) AO1

(3) LOGIC DIAGRAM



(4) ELECTRICAL SCHEMATIC



(5) FUNCTION

A	B	C	D	Z
H	H	X	X	L
X	X	H	X	L
X	X	X	H	L
X	L	L	L	H
L	X	L	L	H

NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

(6) (7)

		FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	GATES
3000 Series	TPLH	13.4ns	16.6	19.8	23.1	36.2	2
	TPHL	4.2	4.9	5.6	6.3	9.2	
5000 Series	TPLH	7.4	9.8	12.2	14.7	24.3	2
	TPHL	1.3	1.8	2.3	2.8	4.8	
7000 Series	TPLH	3.5	4.5	5.5	6.5	10.6	2
	TPHL	1.6	1.8	2.1	2.3	3.4	

INPUT LOADING: 3K (1, 1, 1, 1)
(8) 5K (1, 1, 1, 1)
7K (1, 1, 1, 1)

(9) Z = AO1(A, B, C, D)$

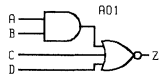
(10)

WORKSTATION WC. DELAY LSI LOGIC CORP 09/25/84
(RISE/FALL) DAISY Ω MENTOR - 17.5 / 5.0 VALID - 12

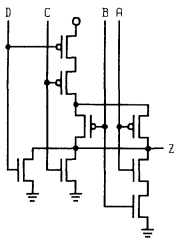
Figure 17.1
Model for Macrocell AO1

AO1 — 2AND INTO 3NOR — AO1

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



FUNCTION

A	B	C	D	Z
H	H	X	X	L
X	X	H	X	L
X	X	X	H	L
X	L	L	L	H
L	X	L	L	H

NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

		F0 = 1	F0 = 2	F0 = 3	F0 = 4	F0 = 8	GATES
3000 Series	TPLH	13.4ns	16.6	19.8	23.1	36.2	2
	TPHL	4.2	4.9	5.6	6.3	9.2	
5000 Series	TPLH	7.4	9.8	12.2	14.7	24.3	2
	TPHL	1.3	1.8	2.3	2.8	4.8	
7000 Series	TPLH	3.5	4.5	5.5	6.5	10.6	2
	TPHL	1.6	1.8	2.1	2.3	3.4	

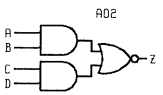
INPUT LOADING: 3K (1, 1, 1, 1)
5K (1, 1, 1, 1)
7K (1, 1, 1, 1)

Z = AO1(A, B, C, D)$

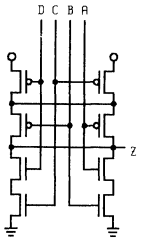
WORKSTATION WC. DELAY — **LSI LOGIC CORP** — 09/25/84
(RISE/FALL) DAISY ∩ MENTOR = 17.5 / 5.0 VALID = 12

AO2 — 2 2ANDS INTO 2NOR — AO2

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



FUNCTION

A	B	C	D	Z
H	H	X	X	L
X	X	H	H	L
L	X	L	X	H
X	L	L	X	H
L	X	X	L	H
X	L	X	L	H

NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

		F0 = 1	F0 = 2	F0 = 3	F0 = 4	F0 = 8	GATES
3000 Series	TPLH	9.2ns	11.3	13.4	15.6	24.4	2
	TPHL	4.2	4.9	5.6	6.3	9.2	
5000 Series	TPLH	5.7	7.3	8.9	10.5	17.0	2
	TPHL	1.7	2.2	2.7	3.2	5.2	
7000 Series	TPLH	2.8	3.5	4.2	4.9	7.6	2
	TPHL	1.2	1.5	1.7	2.0	3.0	

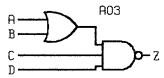
INPUT LOADING: 3K (1, 1, 1, 1)
5K (1, 1, 1, 1)
7K (1, 1, 1, 1)

Z = AO2(A, B, C, D)$

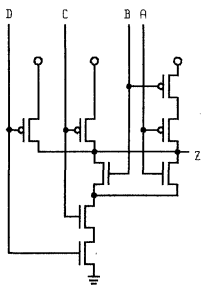
WORKSTATION WC. DELAY — **LSI LOGIC CORP** — 09/25/84
(RISE/FALL) DAISY ∩ MENTOR = 10.3 / 5.0 VALID = 8

AO3 — 2OR INTO 3NAND — AO3

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



FUNCTION

A	B	C	D	Z
H	X	H	H	L
X	H	H	H	L
L	L	X	X	H
X	X	L	X	H
X	X	X	L	H

NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

		FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	GATES
3000 Series	TPLH	9.2ns	11.3	13.4	15.6	24.4	2
	TPHL	4.5	5.4	6.4	7.4	11.3	
5000 Series	TPLH	3.9	5.5	7.2	8.8	15.3	2
	TPHL	2.3	3.0	3.8	4.5	7.4	
7000 Series	TPLH	2.4	3.1	3.7	4.4	7.2	2
	TPHL	1.6	2.0	2.4	2.7	4.2	

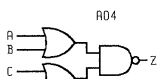
INPUT LOADING: 3K (1, 1, 1, 1)
5K (1, 1, 1, 1)
7K (1, 1, 1, 1)

Z = AO3(A, B, C, D)$

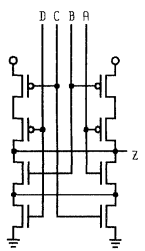
WORKSTATION WC. DELAY **LSI LOGIC CORP** 09/25/84
(RISE/FALL) DAISY ∩ MENTOR = 10.3/ 6.6 VALID = 9

AO4 — 2 2ORS INTO 2NAND — AO4

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



FUNCTION

A	B	C	D	Z
L	L	X	X	H
X	X	L	L	H
H	X	H	X	L
X	H	H	X	L
H	X	X	H	L
X	H	X	H	L

NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

		FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	GATES
3000 Series	TPLH	14.7ns	17.9	21.2	24.6	38.0	2
	TPHL	4.9	5.9	6.8	7.8	11.8	
5000 Series	TPLH	4.1	5.7	7.3	8.9	15.4	2
	TPHL	1.6	2.1	2.6	3.1	5.1	
7000 Series	TPLH	2.3	3.0	3.6	4.3	7.0	2
	TPHL	1.5	1.7	2.0	2.3	3.3	

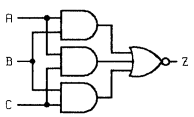
INPUT LOADING: 3K (1, 1, 1, 1)
5K (1, 1, 1, 1)
7K (1, 1, 1, 1)

Z = AO4(A, B, C, D)$

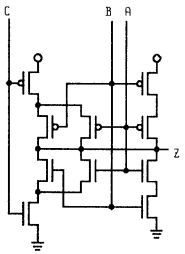
WORKSTATION WC. DELAY **LSI LOGIC CORP** 09/25/84
(RISE/FALL) DAISY ∩ MENTOR = 10.3/ 5.0 VALID = 8

A05 — INVERTING 2 OF 3 MAJORITY — A05

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



FUNCTION

A	B	C	Z
H	H	X	L
H	X	H	L
X	H	H	L
L	L	X	H
L	X	L	H
X	L	L	H

NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

		F0 = 1	F0 = 2	F0 = 3	F0 = 4	F0 = 8	GATES
3000 Series	TPLH	10.7ns	12.2	13.7	15.3	21.6	3
	TPHL	4.5	5.0	5.6	6.2	8.6	
5000 Series	TPLH	6.4	8.0	9.6	11.3	17.7	3
	TPHL	2.0	2.5	3.0	3.5	5.5	
7000 Series	TPLH	3.0	3.7	4.3	5.0	7.7	3
	TPHL	1.6	1.9	2.1	2.4	3.4	

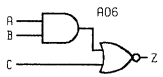
INPUT LOADING: 3K (2, 2, 1)
5K (2, 2, 2)
7K (2, 2, 2)

Z = AO5(A, B, C)$

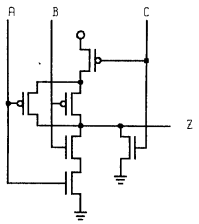
WORKSTATION WC. DELAY **LSI LOGIC CORP** 09/25/84
(RISE/FALL) DAISY Ω MENTOR = 10.8 / 6.6 VALID = 9

A06 — 2AND INTO 2NOR — A06

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

		F0 = 1	F0 = 2	F0 = 3	F0 = 4	F0 = 8	GATES
5000 Series	TPLH	4.9ns	6.5	8.1	9.7	16.2	2
	TPHL	1.3	1.8	2.3	2.8	4.9	
7000 Series	TPLH	2.6	3.2	3.9	4.6	7.3	2
	TPHL	1.2	1.5	1.7	2.0	3.0	

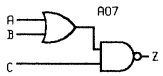
INPUT LOADING: 3K (1, 1, 1)
5K (1, 1, 1)
7K (1, 1, 1)

Z = AO6(A, B, C)$

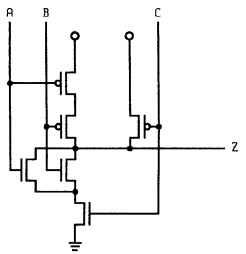
WORKSTATION WC. DELAY **LSI LOGIC CORP** 09/25/84
(RISE/FALL) DAISY Ω MENTOR = 9.6 / 4.8 VALID = 7

A07 — 2OR INTO 2NAND — A07

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

		F0 = 1	F0 = 2	F0 = 3	F0 = 4	F0 = 8	GATES
5000 Series	TPLH	3.8ns	5.5	7.1	8.7	15.2	2
	TPHL	1.7	2.2	2.7	3.1	5.1	
7000 Series	TPLH	2.3	3.0	3.6	4.3	7.0	2
	TPHL	1.4	1.6	1.9	2.2	3.3	

INPUT LOADING: 3K (1, 1, 1)
5K (1, 1, 1)
7K (1, 1, 1)

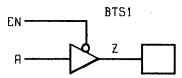
Z = AO7(A, B, C)$

WORKSTATION WC. DELAY — **LSI LOGIC CORP** — 09/25/84
(RISE/FALL) DAISY ∩ MENTOR = 10.4 / 3.9 VALID = 7

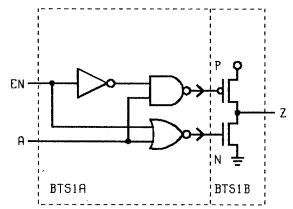
BTS1 — TRISTATE OUTPUT BUFFER — BTS1

PERFORMANCE IS EQUIVALENT TO B1 OUTPUT BUFFER

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

		C = 15PF	C = 50PF	C = 85PF	C = 100PF	WORST CASE COMM. 5V ± 5% @ 0°C-70°C OUTPUT DRIVE	GATES
3000 Series	TPLH	8.9ns	13.7	18.5	20.6	IOH = -1.6ma@2.4v	4
	TPHL	14.3	23.3	32.4	36.3	IOL = 1.6ma@0.4v	
5000 Series	TPLH	5.6	8.8	12.1	13.5	IOH = -4.0ma@2.4v	7
	TPHL	5.4	8.8	12.2	13.6	IOL = 4.0ma@0.4v	
7000 Series	TPLH	4.1	5.5	6.8	7.4	IOH = -4.0ma@2.4v	7
	TPHL	5.2	8.0	10.9	12.1	IOL = 4.0ma@0.4v	

INPUT LOADING: 3K (5, 4) ONE I/O CELL
5K (5, 4)
7K (5, 4)

THE DELAYS FOR OUTPUT ARE MEASURED AT TTL LEVEL.

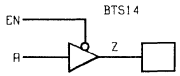
Z = BTS1(A, EN)$

WORKSTATION WC. DELAY — **LSI LOGIC CORP** — 09/25/84
(RISE/FALL) DAISY ∩ MENTOR = 24 / 21.2 VALID = 23

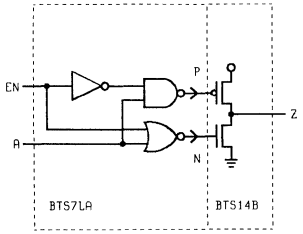
BTS14 TRISTATE OUTPUT BUFFER BTS14

(5K,7K ONLY) (5K,7K ONLY)

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

	C = 15PF	C = 50PF	C = 85PF	C = 100PF	WORST CASE COMM. 5V ± 5% @ 0°C-70°C OUTPUT DRIVE	GATES
5000 TPLH	8.4ns	16.5	24.7	28.1	IOH = -1.0ma@2.4v	5
Series TPHL	10.9	25.7	40.5	46.8	IOL = 1.0ma@0.4v	
7000 TPLH	5.5	10.4	15.3	17.4	IOH = -1.0ma@2.4v	5
Series TPHL	9.0	21.1	33.2	38.4	IOL = 1.0ma@0.4v	

INPUT LOADING: 5K (2, 2) ONE I/O CELL
7K (2, 2)

THE DELAYS FOR OUTPUT ARE MEASURED AT TTL LEVEL.

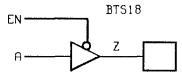
Z = BTS14(A, EN)$

WORKSTATION WC. DELAY **LSI LOGIC CORP** 09/25/84
(RISE/FALL) DAISY ∩ MENTOR = 84.9 / 43.3 VALID = 64

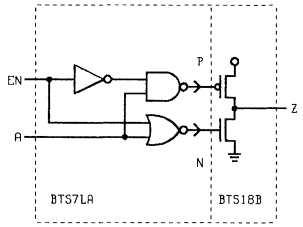
BTS18 TRISTATE OUTPUT BUFFER BTS18

(5K,7K ONLY) (5K,7K ONLY)

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

	C = 15PF	C = 50PF	C = 85PF	C = 100PF	WORST CASE COMM. 5V ± 5% @ 0°C-70°C OUTPUT DRIVE	GATES
5000 TPLH	7.0ns	11.6	16.2	18.2	IOH = -2.0ma@2.4v	5
Series TPHL	8.0	15.4	22.8	25.9	IOL = 2.0ma@0.4v	
7000 TPLH	4.6	6.9	9.3	10.3	IOH = -2.0ma@2.4v	5
Series TPHL	6.4	12.2	17.9	20.4	IOL = 2.0ma@0.4v	

INPUT LOADING: 5K (2, 2) ONE I/O CELL
7K (2, 2)

THE DELAYS FOR OUTPUT ARE MEASURED AT TTL LEVEL.

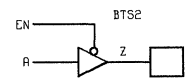
Z = BTS18(A, EN)$

WORKSTATION WC. DELAY **LSI LOGIC CORP** 09/25/84
(RISE/FALL) DAISY ∩ MENTOR = 30.6 / 20.2 VALID = 37

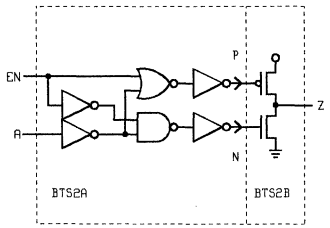
BTS2 — TRISTATE OUTPUT BUFFER — BTS2

PERFORMANCE IS EQUIVALENT TO B2 OUTPUT BUFFER

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

	C = 15PF	C = 50PF	C = 85PF	C = 100PF	WORST CASE COMM. 5V ± 5% @ 0°C-70°C OUTPUT DRIVE	GATES
3000 TPLH Series TPHL	9.7ns 11.2	12.1 15.7	14.6 20.2	15.6 22.1	IOH = -3.2ma@2.4v IOL = 3.2ma@0.4v	5
5000 TPLH Series TPHL	7.3 5.9	9.0 7.7	10.6 9.4	11.3 10.1	IOH = -8.0ma@2.4v IOL = 8.0ma@0.4v	8
7000 TPLH Series TPHL	4.5 4.7	5.2 6.3	5.8 7.9	6.1 8.5	IOH = -8.0ma@2.4v IOL = 8.0ma@0.4v	8

INPUT LOADING: 3K (2, 2.5)
5K (2, 2.5)
7K (2, 2.5)

TWO I/O CELL

THE DELAYS FOR OUTPUT ARE MEASURED AT TTL LEVEL.

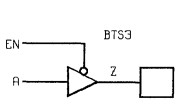
Z = BTS2(A, EN)$

WORKSTATION WC. DELAY **LSI LOGIC CORP** 09/25/84
(RISE/FALL) DAISY ∩ MENTOR = 17.7 / 17.6 VALID = 18

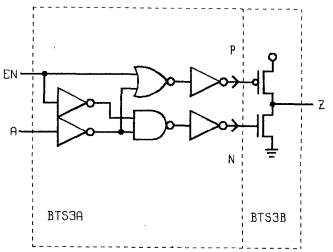
BTS3 — TRISTATE OUTPUT BUFFER — BTS3

PERFORMANCE IS EQUIVALENT TO B3 OUTPUT BUFFER

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

	C = 15PF	C = 50PF	C = 85PF	C = 100PF	WORST CASE COMM. 5V ± 5% @ 0°C-70°C OUTPUT DRIVE	GATES
3000 TPLH Series TPHL	9.5ns 11.9	11.1 14.9	12.7 17.9	13.3 19.2	IOH = -4.8ma@2.4v IOL = 4.8ma@0.4v	6
5000 TPLH Series TPHL	6.1 6.6	7.2 7.9	8.3 9.1	8.7 9.7	IOH = -12.0ma@2.4v IOL = 12.0ma@0.4v	11
7000 TPLH Series TPHL	4.9 5.0	5.3 6.4	5.6 7.7	5.8 8.3	IOH = -12.0ma@2.4v IOL = 12.0ma@0.4v	11

INPUT LOADING: 3K (2, 2.5)
5K (2, 2.5)
7K (2, 2.5)

THREE I/O CELL

THE DELAYS FOR OUTPUT ARE MEASURED AT TTL LEVEL.

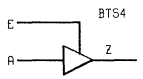
Z = BTS3(A, EN)$

WORKSTATION WC. DELAY **LSI LOGIC CORP** 09/25/84
(RISE/FALL) DAISY ∩ MENTOR = 16 / 15.8 VALID = 16

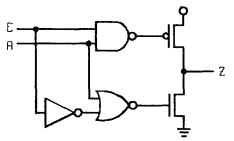
BTS4 BTS4

TRISTATE INTERNAL BUS DRIVER

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

		F0 = 1	F0 = 2	F0 = 3	F0 = 4	F0 = 8	GATES
3000 Series	TPLH	6.6ns	7.4	8.4	9.3	13.0	3
	TPHL	4.7	5.1	5.5	6.0	8.0	
5000 Series	TPLH	2.3	3.2	4.0	4.8	8.1	3
	TPHL	3.1	3.4	3.7	4.0	5.2	
7000 Series	TPLH	1.4	1.8	2.2	2.6	4.2	3
	TPHL	1.8	1.9	2.1	2.3	3.0	

INPUT LOADING: 3K (2, 2)
5K (2, 2)
7K (2, 2)

Y(Z) = BTS4(A, E)$

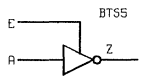
LSI LOGIC CORP

WORKSTATION WC. DELAY 09/25/84
(RISE/FALL) DAISY Ω MENTOR = 5.7 / 4.7 VALID = 5

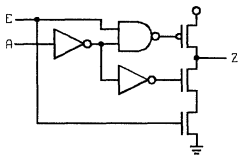
BTS5 BTS5

INVERTING TRISTATE INTERNAL BUS DRIVER

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

		F0 = 1	F0 = 2	F0 = 3	F0 = 4	F0 = 8	GATES
5000 Series	TPLH	2.3ns	3.1	3.9	4.8	8.1	3
	TPHL	1.1	1.6	2.1	2.6	4.6	
7000 Series	TPLH	1.4	1.9	2.3	2.7	4.3	3
	TPHL	0.6	0.8	1.1	1.4	2.4	

INPUT LOADING: 5K (1, 2)
7K (1, 2)

Y(Z) = BTS5(A, E)$

LSI LOGIC CORP

WORKSTATION WC. DELAY 09/25/84
(RISE/FALL) DAISY Ω MENTOR = 9.4 / 6.4 VALID = 8

BTS6

(5K ONLY)

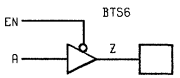
BTS6

(5K ONLY)

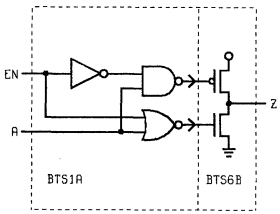
TRISTATE OUTPUT BUFFER

OPTIMIZED FOR EXTERNAL CMOS ENVIRONMENT

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

	C = 15PF	C = 50PF	C = 85PF	C = 100PF	WORST CASE COMM. 5V ± 5% @ 0°C-70°C OUTPUT DRIVE	GATES
5000 TPLH Series TPHL	4.7ns 6.9	6.4 10.3	8.0 13.7	8.7 15.1	IOH = -8.0ma@4.5v IOL = 8.0ma@0.4v	7

INPUT LOADING: 5K (5, 4) TWO I/O CELL

THE DELAYS FOR OUTPUT ARE MEASURED AT TTL LEVEL.

Z = BTS6(A, EN)$

WORKSTATION WC. DELAY **LSI LOGIC CORP** 09/25/84

(RISE/FALL) DAISY ∩ MENTOR = 11.5/ 19.0 VALID = 15

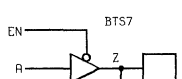
BTS7

BTS7

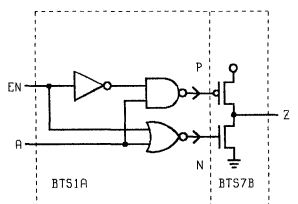
TRISTATE IN/OUTPUT BUFFER

PERFORMANCE IS EQUIVALENT TO B1 OUTPUT BUFFER

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

	C = 15PF	C = 50PF	C = 85PF	C = 100PF	WORST CASE COMM. 5V ± 5% @ 0°C-70°C OUTPUT DRIVE	GATES
3000 TPLH Series TPHL	9.0ns 13.9	13.9 22.9	18.7 32.0	20.8 35.8	IOH = -1.6ma@2.4v IOL = 1.6ma@0.4v	4
5000 TPLH Series TPHL	5.7 5.4	8.9 8.8	12.2 12.1	13.6 13.6	IOH = -4.0ma@2.4v IOL = 4.0ma@0.4v	7
7000 TPLH Series TPHL	4.2 5.1	5.6 7.9	6.9 10.8	7.5 12.0	IOH = -4.0ma@2.4v IOL = 4.0ma@0.4v	7

INPUT LOADING: 3K (5, 4) ONE I/O CELL
5K (5, 4)
7K (5, 4)

THE DELAYS FOR OUTPUT ARE MEASURED AT TTL LEVEL.

Z = BTS7(A, EN)$

WORKSTATION WC. DELAY **LSI LOGIC CORP** 09/25/84

(RISE/FALL) DAISY ∩ MENTOR = 23.7 / 20.9 VALID = 22

BTS7D

(5K ONLY)

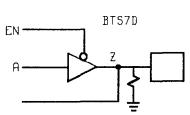
BTS7D

(5K ONLY)

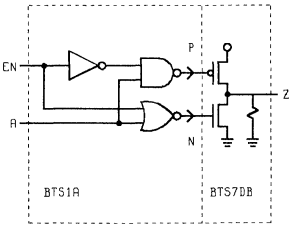
TRISTATE IN/OUTPUT BUFFER

PERFORMANCE IS EQUIVALENT TO B1 OUTPUT BUFFER

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

	C = 15PF	C = 50PF	C = 85PF	C = 100PF	WORST CASE COMM. 5V ± 5% @ 0°C-70°C OUTPUT DRIVE	GATES
5000 TPLH	5.7ns	8.9	12.2	13.6	IOH = -4.0ma@2.4v	7
Series TPHL	5.4	8.8	12.1	13.6	IOL = 4.0ma@0.4v	

INPUT LOADING: 5K (5, 4) ONE I/O CELL

THE DELAYS FOR OUTPUT ARE MEASURED AT TTL LEVEL.

Z = BTS7D(A, EN)$

WORKSTATION WC. DELAY **LSI LOGIC CORP** 09/25/84

(RISE/FALL) DAISY ∩ MENTOR = 15.3/ 16.5 VALID = 16

BTS7L

(5K,7K ONLY)

BTS7L

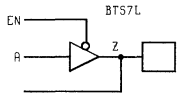
(5K,7K ONLY)

TRISTATE IN/OUTPUT BUFFER

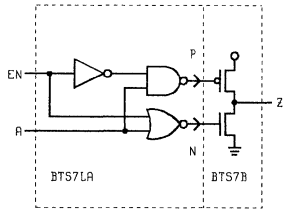
PERFORMANCE IS EQUIVALENT TO B1 OUTPUT BUFFER

PREAMP IS SLOWER

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

	C = 15PF	C = 50PF	C = 85PF	C = 100PF	WORST CASE COMM. 5V ± 5% @ 0°C-70°C OUTPUT DRIVE	GATES
5000 TPLH	6.7ns	9.9	13.2	14.6	IOH = -4.0ma@2.4v	7
Series TPHL	7.1	10.5	13.8	15.3	IOL = 4.0ma@0.4v	
7000 TPLH	4.7	6.1	7.4	8.0	IOH = -4.0ma@2.4v	7
Series TPHL	6.2	9.0	11.9	13.1	IOL = 4.0ma@0.4v	

INPUT LOADING: 5K (2, 2) ONE I/O CELL
7K (2, 2)

THE DELAYS FOR OUTPUT ARE MEASURED AT TTL LEVEL.

Z = BTS7L(A, EN)$

WORKSTATION WC. DELAY **LSI LOGIC CORP** 09/25/84

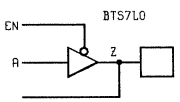
(RISE/FALL) DAISY ∩ MENTOR = 27.0 / 21.6 VALID = 24

BTS7LO (5K,7K ONLY) **BTS7LO** (5K,7K ONLY)

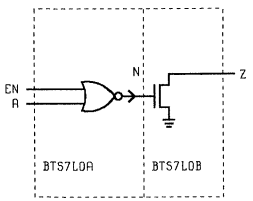
TRISTATE IN/OUTPUT BUFFER WITH OPEN DRAIN

PERFORMANCE IS EQUIVALENT TO B18 OUTPUT BUFFER

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

	C = 15PF	C = 50PF	C = 85PF	C = 100PF	WORST CASE COMM. 5V ± 5% @ 0°C-70°C OUTPUT DRIVE	GATES
5000 TPLH Series TPHL	--.-ns 5.4	--.- 8.7	--.- 12.1	--.- 13.6	IOL = 4.0ma@0.4v	4
7000 TPLH Series TPHL	--.- 4.5	--.- 7.4	--.- 10.2	--.- 11.5	IOL = 4.0ma@0.4v	4

INPUT LOADING: 5K (3, 3) ONE I/O CELL
7K (3, 3)

THE DELAYS FOR OUTPUT ARE MEASURED AT TTL LEVEL.

Z = BTS7LO(A, EN)$

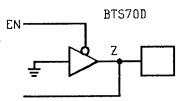
WORKSTATION WC. DELAY **LSI LOGIC CORP** 09/25/84
(RISE/FALL) DAISY ∩ MENTOR = / 24.2 VALID = 24

BTS70D **BTS70D**

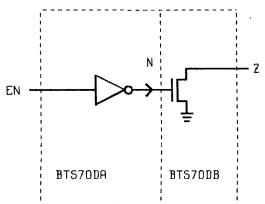
TRISTATE IN/OUTPUT BUFFER WITH OPEN DRAIN

PERFORMANCE IS EQUIVALENT TO B18 OUTPUT BUFFER

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

	C = 15PF	C = 50PF	C = 85PF	C = 100PF	WORST CASE COMM. 5V ± 5% @ 0°C-70°C OUTPUT DRIVE	GATES
3000 TPLH Series TPHL	--.- 8.3	--.- 17.4	--.- 26.4	--.- 30.3	IOL = 1.6ma@0.4v	4
5000 TPLH Series TPHL	--.- 5.1	--.- 8.4	--.- 11.8	--.- 13.3	IOL = 4.0ma@0.4v	4
7000 TPLH Series TPHL	--.- 4.6	--.- 7.5	--.- 10.3	--.- 11.6	IOL = 4.0ma@0.4v	4

INPUT LOADING: 3K (2) ONE I/O CELL
5K (2)
7K (2)

THE DELAYS FOR OUTPUT ARE MEASURED AT TTL LEVEL.

Z = BTS70D(EN)$

WORKSTATION WC. DELAY **LSI LOGIC CORP** 09/25/84
(RISE/FALL) DAISY ∩ MENTOR = / 24.2 VALID = 25

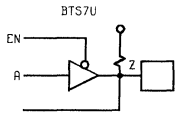
BTS7U

BTS7U

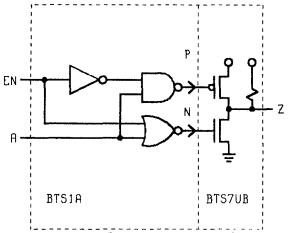
TRISTATE IN/OUTPUT BUFFER WITH PULL UP

PERFORMANCE IS SIMILAR TO B1 OUTPUT BUFFER

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

	C = 15PF	C = 50PF	C = 85PF	C = 100PF	WORST CASE COMM. 5V ± 5% @ 0°C-70°C OUTPUT DRIVE	GATES
3000 TPLH Series TPHL	9.0ns 13.9	13.9 22.9	18.7 32.0	20.8 35.8	IOH = -1.6ma@2.4v IOL = 1.6ma@0.4v	4
5000 TPLH Series TPHL	5.7 5.4	8.9 8.8	12.2 12.1	13.6 13.6	IOH = -4.0ma@2.4v IOL = 4.0ma@0.4v	7
7000 TPLH Series TPHL	4.2 5.1	5.6 7.9	6.9 10.8	7.5 12.0	IOH = -4.0ma@2.4v IOL = 4.0ma@0.4v	7

INPUT LOADING: 3K (5, 4)
5K (5, 4)
7K (5, 4)

ONE I/O CELL

THE DELAYS FOR OUTPUT ARE MEASURED AT TTL LEVEL.

Z = BTS7U(A, EN)$

WORKSTATION WC. DELAY **LSI LOGIC CORP** 09/25/84

(RISE/FALL) DAISY ∩ MENTOR = 23.7 / 20.9 VALID = 22

BTS78

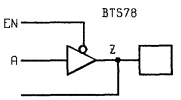
(5K,7K ONLY)

BTS78
(5K,7K ONLY)

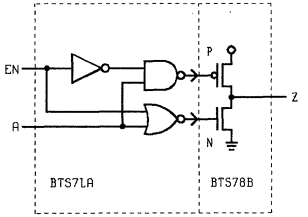
TRISTATE IN/OUTPUT BUFFER

PERFORMANCE IS EQUIVALENT TO B1B OUTPUT BUFFER

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

	C = 15PF	C = 50PF	C = 85PF	C = 100PF	WORST CASE COMM. 5V ± 5% @ 0°C-70°C OUTPUT DRIVE	GATES
5000 TPLH Series TPHL	7.1ns 7.9	11.7 15.3	16.3 22.7	18.3 25.9	IOH = -2.0ma@2.4v IOL = 2.0ma@0.4v	5
7000 TPLH Series TPHL	4.7 6.3	7.1 12.0	9.4 17.7	10.4 20.2	IOH = -2.0ma@2.4v IOL = 2.0ma@0.4v	5

INPUT LOADING: 5K (2, 2)
7K (2, 2)

ONE I/O CELL

THE DELAYS FOR OUTPUT ARE MEASURED AT TTL LEVEL.

Z = BTS78(A, EN)$

WORKSTATION WC. DELAY **LSI LOGIC CORP** 09/25/84

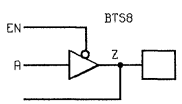
(RISE/FALL) DAISY ∩ MENTOR = 45.2 / 28.2 VALID = 37

BTS8 BTS8

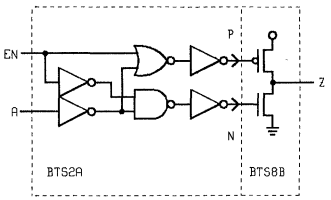
TRISTATE IN/OUTPUT BUFFER

PERFORMANCE IS EQUIVALENT TO B2 OUTPUT BUFFER

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

	C = 15PF	C = 50PF	C = 85PF	C = 100PF	WORST CASE COMM. 5V ± 5% @ 0°C-70°C OUTPUT DRIVE	GATES
3000 TPLH Series TPHL	9.9ns 11.0	12.3 15.5	14.7 20.1	15.8 22.0	IOH = -3.2ma@2.4v IOL = 3.2ma@0.4v	5
5000 TPLH Series TPHL	7.5 5.9	9.1 7.6	10.7 9.3	11.4 10.1	IOH = -8.0ma@2.4v IOL = 8.0ma@0.4v	8
7000 TPLH Series TPHL	4.6 4.6	5.2 6.2	5.9 7.8	6.2 8.4	IOH = -8.0ma@2.4v IOL = 8.0ma@0.4v	8

INPUT LOADING: 3K (2, 2.5) TWO I/O CELLS
5K (2, 2.5)
7K (2, 2.5)

THE DELAYS FOR OUTPUT ARE MEASURED AT TTL LEVEL.

Z = BTS8(A, EN)$

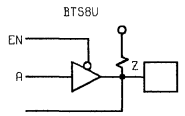
WORKSTATION WC. DELAY **LSI LOGIC CORP** 09/25/84
(RISE/FALL) DAISY ∩ MENTOR = 17.2 / 17.4 VALID = 18

BTS8U (5K ONLY) BTS8U (5K ONLY)

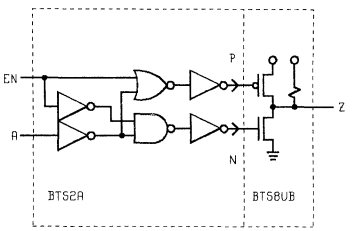
TRISTATE IN/OUTPUT BUFFER WITH PULL UP

PERFORMANCE IS SIMILAR TO B2 OUTPUT BUFFER

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

	C = 15PF	C = 50PF	C = 85PF	C = 100PF	WORST CASE COMM. 5V ± 5% @ 0°C-70°C OUTPUT DRIVE	GATES
5000 TPLH Series TPHL	7.5ns 5.9	9.1 7.6	10.7 9.3	11.4 10.1	IOH = -8.0ma@4.5v IOL = 8.0ma@0.4v	8

INPUT LOADING: 5K (2, 2.5) TWO I/O CELL

THE DELAYS FOR OUTPUT ARE MEASURED AT TTL LEVEL.

Z = BTS8U(A, EN)$

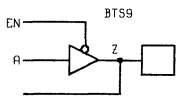
WORKSTATION WC. DELAY **LSI LOGIC CORP** 09/25/84
(RISE/FALL) DAISY ∩ MENTOR = 14.4 / 13.6 VALID = 14

BTS9 BTS9

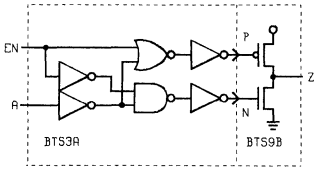
TRISTATE IN/OUTPUT BUFFER

PERFORMANCE IS EQUIVALENT TO B3 OUTPUT BUFFER

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

	C = 15PF	C = 50PF	C = 85PF	C = 100PF	WORST CASE COMM. 5V ± 5% @ 0°C-70°C OUTPUT DRIVE	GATES
3000 TPLH Series TPHL	9.6ns 11.2	11.2 12.9	12.8 14.6	13.5 15.4	IOH = -4.8ma@2.4v IOL = 4.8ma@0.4v	6
5000 TPLH Series TPHL	6.2 6.5	7.3 7.8	8.4 9.1	8.8 9.6	IOH = -12.0ma@2.4v IOL = 12.0ma@0.4v	11
7000 TPLH Series TPHL	5.0 4.9	5.3 6.3	5.7 7.6	5.8 8.2	IOH = -12.0ma@2.4v IOL = 12.0ma@0.4v	11

INPUT LOADING: 3K (2, 2.5) THREE I/O CELLS
5K (2, 2.5)
7K (2, 2.5)

THE DELAYS FOR OUTPUT ARE MEASURED AT TTL LEVEL.

Z = BTS9(A, EN)$

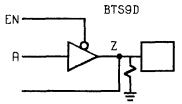
WORKSTATION WC. DELAY **LSI LOGIC CORP** 09/25/84
(RISE/FALL) DAISY ∩ MENTOR = 15.5 / 15.5 VALID = 16

BTS9D (5K ONLY) BTS9D (5K ONLY)

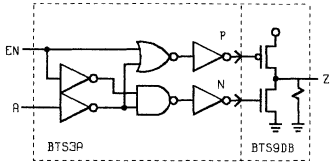
TRISTATE IN/OUTPUT BUFFER WITH PULL DOWN

PERFORMANCE IS EQUIVALENT TO B3 OUTPUT BUFFER

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

	C = 15PF	C = 50PF	C = 85PF	C = 100PF	WORST CASE COMM. 5V ± 5% @ 0°C-70°C OUTPUT DRIVE	GATES
5000 TPLH Series TPHL	6.2 6.5	7.3 7.8	8.4 9.1	8.8 9.6	IOH = -12.0ma@2.4v IOL = 12.0ma@0.4v	11

INPUT LOADING: 5K (2, 2.5) THREE I/O CELLS

THE DELAYS FOR OUTPUT ARE MEASURED AT TTL LEVEL.

Z = BTS9D(A, EN)$

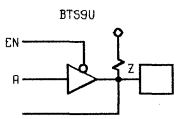
WORKSTATION WC. DELAY **LSI LOGIC CORP** 09/25/84
(RISE/FALL) DAISY ∩ MENTOR = 13.6 / 13.2 VALID = 14

BTS9U BTS9U

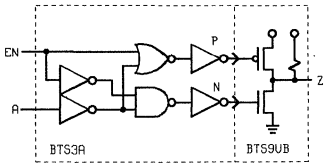
TRISTATE IN/OUTPUT BUFFER WITH PULL UP

PERFORMANCE IS SIMILAR TO B3 OUTPUT BUFFER

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

	C = 15PF	C = 50PF	C = 85PF	C = 100PF	WORST CASE COMM. 5V ± 5% @ 0°C-70°C OUTPUT DRIVE	GATES
3000 TPLH Series TPHL	9.4ns 11.2	11.0 12.9	12.6 14.6	13.3 15.4	IOH = -4.8ma@2.4v IOL = 4.8ma@0.4v	6
5000 TPLH Series TPHL	6.2 6.5	7.3 7.8	8.4 9.1	8.8 9.6	IOH = -12.0ma@2.4v IOL = 12.0ma@0.4v	11

INPUT LOADING: 3K (2, 2.5)
5K (2, 2.5)

THREE I/O CELLS

THE DELAYS FOR OUTPUT ARE MEASURED AT TTL LEVEL.

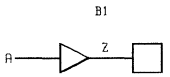
Z = BTS9U(A, EN)$

WORKSTATION WC. DELAY **LSI LOGIC CORP** 09/25/84
(RISE/FALL) DAISY ∩ MENTOR = 13.6/ 13.2 VALID = 14

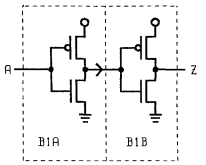
B1 B1

OUTPUT BUFFER

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

	C = 15PF	C = 50PF	C = 85PF	C = 100PF	WORST CASE COMM. 5V ± 5% @ 0°C-70°C OUTPUT DRIVE	GATES
3000 TPLH Series TPHL	6.3ns 9.6	11.1 17.4	15.9 25.3	18.0 28.7	IOH = -1.6ma@2.4v IOL = 1.6ma@0.4v	1
5000 TPLH Series TPHL	4.1 4.5	7.3 7.9	10.6 11.3	12.0 12.7	IOH = -4.0ma@2.4v IOL = 4.0ma@0.4v	2
7000 TPLH Series TPHL	3.0 4.3	4.4 7.1	5.7 10.0	6.3 11.2	IOH = -4.0ma@2.4v IOL = 4.0ma@0.4v	2

INPUT LOADING: 3K (3)
5K (3)
7K (3)

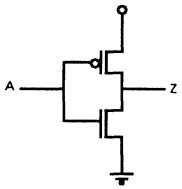
ONE I/O CELL

THE DELAYS FOR OUTPUT ARE MEASURED AT TTL LEVEL.

Z = B1(A)$

WORKSTATION WC. DELAY **LSI LOGIC CORP** 09/25/84
(RISE/FALL) DAISY ∩ MENTOR = 20.7 / 17.7 VALID = 19

B1A — Inverting Power Buffer — B1A



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

		F0 = 4	F0 = 8	F0 = 16	F0 = 32	F0 = 64	GATES
3000 Series	TPLH	4.3ns	6.4	10.6	19.1	36.2	1
	TPHL	2.8	3.9	6.4	11.3	21.2	
5000 Series	TPLH	1.8	2.6	4.3	7.5	14.1	2
	TPHL	1.3	1.9	3.0	5.3	9.9	
7000 Series	TPLH	1.3	1.7	2.4	4.0	7.1	2
	TPHL	1.1	1.4	2.1	3.4	6.1	

INPUT LOADING: 3K (3)
5K (3)
7K (3)

ONE I/O CELL

Z = B1A(A)$

FIXED DELAYS [WORKSTATION SOFTWARE DATABOOK]

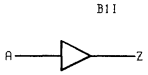
WORST CASE COMMERCIAL DELAYS BASED UPON FO= 8 WITH STATISTICAL WIRE LENGHTS		VALID	DAISY	MENTOR
	TPHL	4	3.0	3.0
	TPLH		4.2	4.2

B1I — B1I

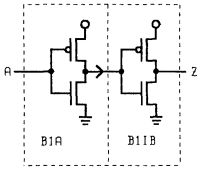
INTERNAL BUFFER

PERFORMANCE IS EQUIVALENT TO B1 OUTPUT BUFFER

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

		F0 = 4	F0 = 8	F0 = 16	F0 = 32	F0 = 64	GATES
*3000 Series	TPLH	7.6ns	8.3	9.9	13.4	20.4	1
	TPHL	8.6	9.1	10.3	12.8	17.9	
5000 Series	TPLH	3.1	3.4	4.0	5.2	7.7	2
	TPHL	3.0	3.1	3.2	3.6	4.4	
7000 Series	TPLH	2.3	2.5	2.8	3.3	4.4	2
	TPHL	2.3	2.4	2.7	3.2	4.2	

INPUT LOADING: 3K (3)
5K (3)
7K (3)

ONE I/O CELL

* THE DELAYS FOR HIGH FANOUT CAN BE REDUCED IF SPECIFIED AS CRITICAL NET.

Z = B1I(A)$

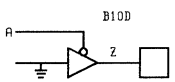
LSI LOGIC CORP

WORKSTATION WC. DELAY 09/25/84
(RISE/FALL) DAISY ⌂ MENTOR = 5.4 / 3.5 VALID = 5

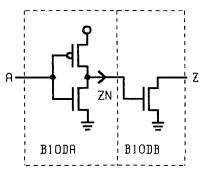
B10D B10D

OUTPUT BUFFER
WITH OPEN DRAIN

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

	C = 15PF	C = 50PF	C = 85PF	C = 100PF	WORST CASE COMM. 5V ± 5% @ 0°C-70°C OUTPUT DRIVE	GATES
3000 TPLH Series TPHL	--.- 7.5	--.- 12.7	--.- 17.9	--.- 20.2	IOL = 1.6ma@0.4v	1
5000 TPLH Series TPHL	--.- 4.7	--.- 8.1	--.- 11.5	--.- 12.9	IOL = 4.0ma@0.4v	1
7000 TPLH Series TPHL	--.- 3.7	--.- 6.6	--.- 9.4	--.- 10.7	IOL = 4.0ma@0.4v	1

INPUT LOADING: 3K (1.5)
5K (1.5)
7K (1.5)

ONE I/O CELL

THE DELAYS FOR OUTPUT ARE MEASURED AT TTL LEVEL.

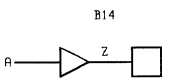
Z = B10D(A)$

WORKSTATION WC. DELAY **LSI LOGIC CORP** 09/25/84
(RISE/FALL) DAISY Ω MENTOR = / 22.3 VALID = 22

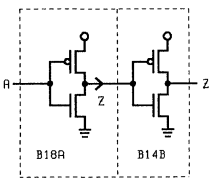
B14 B14

OUTPUT BUFFER

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

	C = 15PF	C = 50PF	C = 85PF	C = 100PF	WORST CASE COMM. 5V ± 5% @ 0°C-70°C OUTPUT DRIVE	GATES
5000 TPLH Series TPHL	5.9ns 9.0	14.0 23.8	22.2 38.6	25.6 44.9	IOH = -1.0ma@2.4v IOL = 1.0ma@0.4v	1
7000 TPLH Series TPHL	4.7 8.3	9.6 20.4	14.5 32.5	16.6 37.7	IOH = -1.0ma@2.4v IOL = 1.0ma@0.4v	1

INPUT LOADING: 5K (1.5)
7K (1.5)

ONE I/O CELL

THE DELAYS FOR OUTPUT ARE MEASURED AT TTL LEVEL.

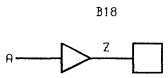
Z = B14(A)$

WORKSTATION WC. DELAY **LSI LOGIC CORP** 09/25/84
(RISE/FALL) DAISY Ω MENTOR = 80.7 / 35.3 VALID = 58

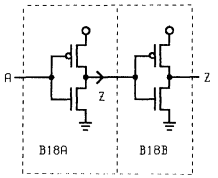
B18 B18

OUTPUT BUFFER

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

	C = 15PF	C = 50PF	C = 85PF	C = 100PF	WORST CASE COMM. 5V ± 5% @ 0°C-70°C OUTPUT DRIVE	GATES
3000 TPLH Series TPHL	5.6ns 12.1	10.4 27.8	15.3 43.6	17.3 50.3	IOH = -0.8ma@2.4v IOL = 0.8ma@0.4v	1
5000 TPLH Series TPHL	4.8 6.4	9.4 13.8	14.0 21.2	16.0 24.3	IOH = -2.0ma@2.4v IOL = 2.0ma@0.4v	1
7000 TPLH Series TPHL	3.8 5.5	6.1 11.3	8.5 17.0	9.5 19.5	IOH = -2.0ma@2.4v IOL = 2.0ma@0.4v	1

INPUT LOADING: 3K (1.5)
5K (1.5)
7K (1.5)

ONE I/O CELL

THE DELAYS FOR OUTPUT ARE MEASURED AT TTL LEVEL.

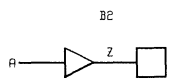
Z = B18(A)$

WORKSTATION WC. DELAY **LSI LOGIC CORP** 09/25/84
(RISE/FALL) DAISY ∩ MENTOR = 42.1 / 22.3 VALID = 32

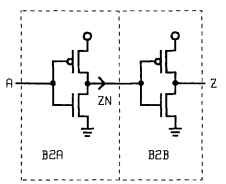
B2 B2

OUTPUT BUFFER

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

	C = 15PF	C = 50PF	C = 85PF	C = 100PF	WORST CASE COMM. 5V ± 5% @ 0°C-70°C OUTPUT DRIVE	GATES
3000 TPLH Series TPHL	6.4ns 9.3	8.8 13.8	11.3 18.3	12.3 20.2	IOH = -3.2ma@2.4v IOL = 3.2ma@0.4v	2
5000 TPLH Series TPHL	3.3 3.6	5.0 5.4	6.6 7.1	7.3 7.8	IOH = -8.0ma@2.4v IOL = 8.0ma@0.4v	4
7000 TPLH Series TPHL	2.6 3.2	3.3 4.8	3.9 6.4	4.2 7.0	IOH = -8.0ma@2.4v IOL = 8.0ma@0.4v	4

INPUT LOADING: 3K (6)
5K (6)
7K (6)

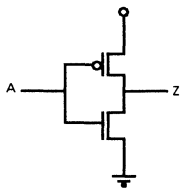
TWO I/O CELLS

THE DELAYS FOR OUTPUT ARE MEASURED AT TTL LEVEL.

Z = B2(A)$

WORKSTATION WC. DELAY **LSI LOGIC CORP** 09/25/84
(RISE/FALL) DAISY ∩ MENTOR = 12.5 / 9.6 VALID = 11

B2A — Inverting Power Buffer — B2A



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

		F0 = 4	F0 = 8	F0 = 16	F0 = 32	F0 = 64	GATES
3000 Series	TPLH	3.4ns	4.6	7.1	12.3	22.6	2
	TPHL	2.3	3.1	4.8	8.1	14.9	
5000 Series	TPLH	1.4	1.8	2.6	4.2	7.5	4
	TPHL	1.0	1.3	1.9	3.1	5.4	
7000 Series	TPLH	1.0	1.2	1.5	2.3	3.9	4
	TPHL	0.9	1.0	1.4	2.1	3.4	

INPUT LOADING: 3K (3)
5K (3)
7K (3)

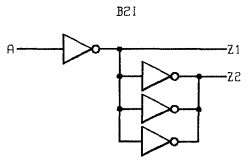
Z = B2A(A)$

WORST CASE COMMERCIAL DELAYS BASED UPON FO= 8 WITH STATISTICAL WIRE LENGHTS		VALID	DAISY	MENTOR
	TPHL	3	2.1	2.1
	TPLH		2.8	2.8

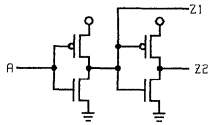
B2I — B2I

INVERTER INTO 3 PARALLEL INVERTERS

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

Z2 OUTPUT Z1 UNLOADED		F0 = 4	F0 = 8	F0 = 16	F0 = 32	F0 = 64	GATES
*3000 Series	TPLH	6.7ns	8.2	11.3	17.5	30.0	2
	TPHL	8.7	9.6	11.5	15.4	23.2	
5000 Series	TPLH	2.8	3.8	6.0	10.3	19.0	2
	TPHL	3.2	3.7	4.5	6.3	9.7	
7000 Series	TPLH	1.9	2.4	3.5	5.7	10.1	2
	TPHL	2.2	2.5	3.1	4.3	6.7	

INPUT LOADING: 3K (1)
5K (1)
7K (1)

* THE DELAYS FOR HIGH FANOUT CAN BE REDUCED IF SPECIFIED AS CRITICAL NET.

X(Z1, Z2) = B2I(A)$

LSI LOGIC CORP

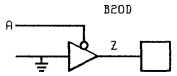
WORKSTATION WC. DELAY
(RISE/FALL) DAISY ⌂ MENTOR = 5.4 / 4.4 VALID = 5

09/25/84

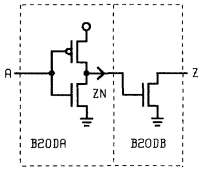
B20D B20D

OUTPUT BUFFER
WITH OPEN DRAIN

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

	C = 15PF	C = 50PF	C = 85PF	C = 100PF	WORST CASE COMM. 5V ± 5% @ 0°C-70°C OUTPUT DRIVE	GATES
3000 TPLH Series TPHL	--.- 8.5	--.- 10.2	--.- 11.9	--.- 12.7	IOL = 1.6ma@0.4v	2
5000 TPLH Series TPHL	--.- 4.6	--.- 6.3	--.- 8.1	--.- 8.8	IOL = 8.0ma@0.4v	2
7000 TPLH Series TPHL	--.- 2.9	--.- 4.5	--.- 6.1	--.- 6.8	IOL = 8.0ma@0.4v	2

INPUT LOADING: 3K (3.5)
5K (3.5)
7K (3.5)

TWO I/O CELLS

THE DELAYS FOR OUTPUT ARE MEASURED AT TTL LEVEL.

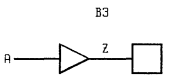
Z = B2OD(A)$

WORKSTATION WC. DELAY **LSI LOGIC CORP** 09/25/84
(RISE/FALL) DAISY ∩ MENTOR = / 8.0 VALID = 8

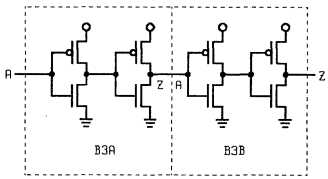
B3 B3

OUTPUT BUFFER

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

	C = 15PF	C = 50PF	C = 85PF	C = 100PF	WORST CASE COMM. 5V ± 5% @ 0°C-70°C OUTPUT DRIVE	GATES
3000 TPLH Series TPHL	11.4ns 11.6	13.0 13.3	14.6 15.0	15.2 15.8	IOH = -4.8ma@2.4v IOL = 4.8ma@0.4v	3
5000 TPLH Series TPHL	5.3 6.5	6.4 7.8	7.5 9.1	8.0 9.6	IOH = -12.0ma@2.4v IOL = 12.0ma@0.4v	2
7000 TPLH Series TPHL	6.5 6.1	6.8 7.4	7.2 8.8	7.3 9.4	IOH = -12.0ma@2.4v IOL = 12.0ma@0.4v	2

INPUT LOADING: 3K (1)
5K (1)
7K (1)

FOUR I/O CELLS

THE DELAYS FOR OUTPUT ARE MEASURED AT TTL LEVEL.

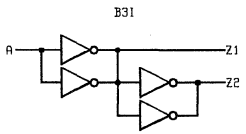
Z = B3(A)$

WORKSTATION WC. DELAY **LSI LOGIC CORP** 09/25/84
(RISE/FALL) DAISY ∩ MENTOR = 12.2 / 12.9 VALID = 13

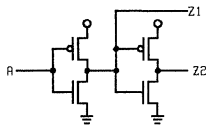
B3I B3I

2 PARALLEL INVERTERS INTO 2 PARALLEL INVERTERS

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

Z2 OUTPUT Z1 UNLOADED		FO = 2	FO = 4	FO = 8	FO = 16	FO = 32	GATES
*3000 Series	TPLH	5.8ns	6.9	8.9	13.2	21.7	2
	TPHL	5.8	6.3	7.5	10.0	14.9	
5000 Series	TPLH	1.9	2.7	4.3	7.6	14.1	2
	TPHL	2.0	2.3	2.9	4.2	6.7	
7000 Series	TPLH	1.4	1.8	2.6	4.2	7.3	2
	TPHL	1.6	1.7	2.1	2.7	4.0	

INPUT LOADING: 3K (2)
5K (2)
7K (2)

* THE DELAYS FOR HIGH FANOUT CAN BE REDUCED IF SPECIFIED AS CRITICAL NET.

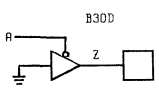
X(Z1, Z2) = B3I(A)$

WORKSTATION WC. DELAY **LSI LOGIC CORP** 09/25/84
(RISE/FALL) DAISY ∩ MENTOR = 5.7 / 4.9 VALID = 5

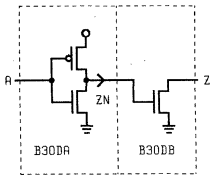
B30D B30D

OUTPUT BUFFER

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

	C = 15PF	C = 50PF	C = 85PF	C = 100PF	WORST CASE COMM. 5V ± 5% @ 0°C-70°C OUTPUT DRIVE	GATES
3000 Series TPLH	--.-	--.-	--.-	--.-		
3000 Series TPHL	9.2	11.0	12.7	13.4	IOL = 1.6ma@0.4v	3
5000 Series TPLH	--.-	--.-	--.-	--.-		
5000 Series TPHL	3.4	4.7	6.0	6.6	IOL = 12.0ma@0.4v	2
7000 Series TPLH	--.-	--.-	--.-	--.-		
7000 Series TPHL	2.8	4.1	5.5	6.1	IOL = 12.0ma@0.4v	2

INPUT LOADING: 3K (4.5)
5K (4.5)
7K (4.5)

FOUR I/O CELLS

THE DELAYS FOR OUTPUT ARE MEASURED AT TTL LEVEL.

Z = B30D(A)$

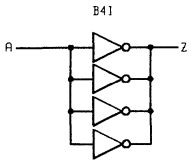
WORKSTATION WC. DELAY **LSI LOGIC CORP** 09/25/84
(RISE/FALL) DAISY ∩ MENTOR = / 13.7 VALID = 16

B4I

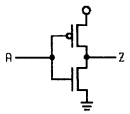
B4I

4 PARALLEL INVERTERS

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

		F0 = 4	F0 = 8	F0 = 16	F0 = 32	F0 = 64	GATES
3000 Series	TPLH	3.0ns	4.2	6.8	12.0	22.3	2
	TPHL	2.1	2.9	4.5	7.9	14.7	
5000 Series	TPLH	1.8	2.6	4.3	7.5	14.1	2
	TPHL	0.9	1.2	1.8	2.9	5.3	
7000 Series	TPLH	1.3	1.7	2.5	4.1	7.4	2
	TPHL	0.7	0.9	1.3	2.1	3.8	

INPUT LOADING: 3K (4)
5K (4)
7K (4)

THE DELAYS FOR HIGH FANOUT CAN BE REDUCED IF SPECIFIED AS CRITICAL NET.

Z = B4I(A)$

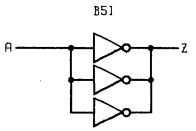
WORKSTATION WC. DELAY **LSI LOGIC CORP** 09/25/84
(RISE/FALL) DAISY ∩ MENTOR = 2.8 / 1.2 VALID = 2

B5I

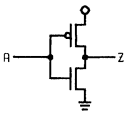
B5I

3 PARALLEL INVERTERS

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

		F0 = 4	F0 = 8	F0 = 16	F0 = 32	F0 = 64	GATES
3000 Series	TPLH	3.5ns	5.0	8.1	14.4	26.9	2
	TPHL	2.3	3.2	5.2	9.0	16.8	
5000 Series	TPLH	2.2	3.3	5.5	9.9	18.8	2
	TPHL	1.0	1.4	2.2	3.8	6.9	
7000 Series	TPLH	1.4	1.9	2.9	5.0	9.1	2
	TPHL	0.8	1.0	1.5	2.5	4.4	

INPUT LOADING: 3K (3)
5K (3)
7K (3)

THE DELAYS FOR HIGH FANOUT CAN BE REDUCED IF SPECIFIED AS CRITICAL NET.

Z = B5I(A)$

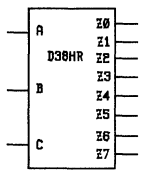
WORKSTATION WC. DELAY **LSI LOGIC CORP** 09/25/84
(RISE/FALL) DAISY ∩ MENTOR = 3.8 / 1.7 VALID = 3

D38HR

D38HR

NON-OVERLAPPING 3 TO 8 DECODER, BUFFERED OUTPUTS, ACTIVE HIGH

LOGIC DIAGRAM



TRUTH TABLE

C	B	A	0	1	2	3	4	5	6	7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

		F0 = 1	F0 = 2	F0 = 3	F0 = 4	F0 = 8	GATES
5000 Series	TPLH	13.4ns	13.6	13.8	14.0	14.8	47
	TPHL	10.1	10.1	10.2	10.3	10.6	

INPUT LOADING: 5K (2, 2, 2)

Z(Z0, Z1, Z2, Z3, Z4, Z5, Z6, Z7) = D38HR(A, B, C)$

LSI LOGIC CORP

GATES USED - 19

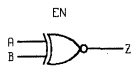
09/07/83

EN

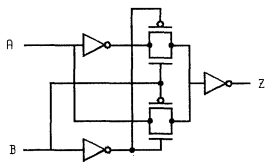
EN

EXCLUSIVE 2NOR

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

		F0 = 1	F0 = 2	F0 = 3	F0 = 4	F0 = 8	GATES
3000 Series	TPLH	3.3ns	3.7	4.1	4.6	6.7	3
	TPHL	5.1	5.9	6.8	7.8	11.7	
5000 Series	TPLH	3.0	3.4	3.8	4.2	5.8	3
	TPHL	4.3	4.5	4.7	4.9	5.6	
7000 Series	TPLH	2.0	2.2	2.4	2.6	3.4	3
	TPHL	2.5	2.6	2.7	2.8	3.3	

INPUT LOADING: 3K (4, 2)
5K (5.3, 2)
7K (5.9, 2)

THE DELAYS FOR HIGH FANOUT CAN BE REDUCED IF SPECIFIED AS CRITICAL NET.

Z = EN(A, B)$

WORKSTATION WC. DELAY (RISE/FALL) DAISY Ω MENTOR = 5.6 / 3.8 VALID = 5

LSI LOGIC CORP

09/25/84

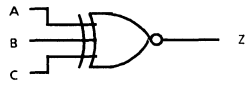
EN3

3 Input Exclusive Nor

EN3

(7k only)

(7k only)



FUNCTION

A	B	C	Z
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

		F0 = 1	F0 = 2	F0 = 4	F0 = 8	F0 = 16	GATES
7000 Series	TPLH	4.1ns	4.3	4.7	5.5	7.2	6
	TPHL	2.6	2.7	2.9	3.3	4.2	

INPUT LOADING: 7K (8.3, 3, 2)

Z = EN3(A, B, C)$

FIXED DELAYS [WORKSTATION SOFTWARE DATABOOK]

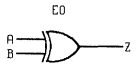
WORST CASE COMMERCIAL DELAYS BASED UPON FO= 2 WITH STATISTICAL WIRE LENGHTS		VALID	DAISY	MENTOR
	TPLH	6	7.0	7.0
	TPHL		5.0	5.0

EO

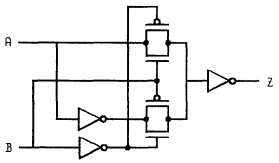
EO

EXCLUSIVE 2OR

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

		F0 = 4	F0 = 8	F0 = 16	F0 = 32	F0 = 64	GATES
3000 Series	TPLH	4.3ns	5.1	6.0	7.0	10.7	3
	TPHL	4.6	5.5	6.4	7.3	11.2	
5000 Series	TPLH	3.4	3.9	4.3	4.7	6.4	3
	TPHL	4.2	4.4	4.6	4.8	5.5	
7000 Series	TPLH	2.0	2.2	2.4	2.6	3.4	3
	TPHL	2.5	2.6	2.7	2.8	3.3	

INPUT LOADING: 3K (4, 2)
5K (5.3, 2)
7K (5.9, 2)

Z = EO(A, B)$

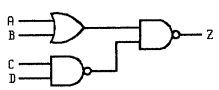
WORKSTATION WC. DELAY **LSI LOGIC CORP** 09/25/84

(RISE/FALL) DAISY Ω MENTOR = 5.9 / 4.4 VALID = 5

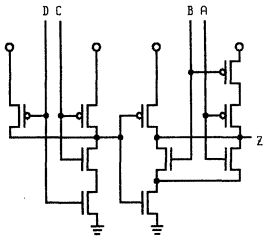
EON1 EON1

2OR, 2NAND INTO 2NAND

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

		FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	GATES
3000 Series	TPLH	9.4ns	11.5	13.6	15.8	24.6	3
	TPHL	4.0	4.6	5.3	6.0	8.9	
5000 Series	TPLH	3.8	5.4	7.1	8.7	15.2	3
	TPHL	3.6	4.1	4.7	5.2	7.2	
7000 Series	TPLH	2.5	3.2	3.9	4.5	7.3	3
	TPHL	2.4	2.6	2.9	3.2	4.3	

INPUT LOADING: 3K (1, 1, 1, 1)
5K (1, 1, 1, 1)
7K (1, 1, 1, 1)

Z = EON1(A, B, C, D)$

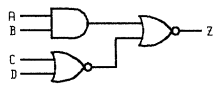
LSI LOGIC CORP

WORKSTATION WC. DELAY 09/25/84
(RISE/FALL) DAISY ∩ MENTOR = 12.2/ 8.0 VALID = 10

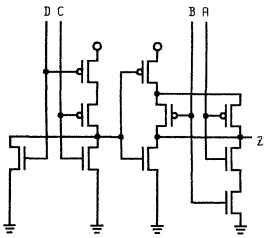
EO1 EO1

2AND, 2NOR INTO 2NOR

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

		FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	GATES
3000 Series	TPLH	7.4	8.9	10.5	12.1	18.6	3
	TPHL	3.1	3.6	4.1	4.7	7.2	
5000 Series	TPLH	5.6	7.2	8.9	10.5	17.0	3
	TPHL	3.7	4.0	4.4	4.7	6.0	
7000 Series	TPLH	2.7	3.4	4.1	4.8	7.5	3
	TPHL	1.4	1.7	1.9	2.2	3.3	

INPUT LOADING: 3K (1, 1, 1, 1)
5K (1, 1, 1, 1)
7K (1, 1, 1, 1)

Z = EO1(A, B, C, D)$

LSI LOGIC CORP

WORKSTATION WC. DELAY 09/25/84
(RISE/FALL) DAISY ∩ MENTOR = 11.8 / 9.4 VALID = 11

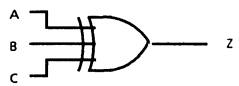
EO3

(7k only)

3 Input Exclusive Or

EO3

(7k only)



FUNCTION

A	B	C	Z
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

		F0 = 1	F0 = 2	F0 = 4	F0 = 8	F0 = 16	GATES
7000 Series	TPLH	2.7ns	2.9	3.3	4.1	5.8	6
	TPHL	4.0	4.1	4.3	4.7	5.6	

INPUT LOADING: 7K (8.3, 3, 2)

Z = EO3(A, B, C)$

FIXED DELAYS [WORKSTATION SOFTWARE DATABOOK]

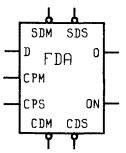
WORST CASE COMMERCIAL DELAYS BASED UPON FO = 2 WITH STATISTICAL WIRE LENGHTS		VALID	DAISY	MENTOR
	TPLH	6	7.0	7.0
	TPHL		5.0	5.0

FDA

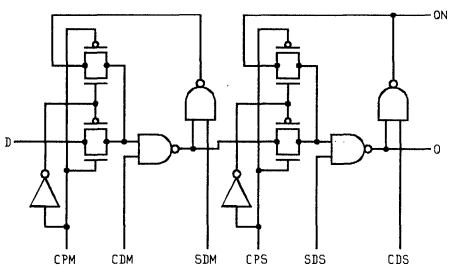
D FLIP FLOP WITH SEPERATE MASTER ⌂ SLAVE CLOCKS, CLEAR DIRECT ⌂ SET DIRECT.

FDA

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

Q OUTPUT		F0 = 1	F0 = 2	F0 = 3	F0 = 4	F0 = 8	GATES
5000 Series	TPLH	4.2ns	5.0	5.8	6.7	10.0	7
	TPHL	3.4	3.9	4.4	4.9	7.0	
7000 Series	TPLH	3.5	3.8	4.2	4.6	6.2	7
	TPHL	3.2	3.5	3.7	4.0	5.1	

INPUT LOADING: 5K (3.7, 2, 2, 1, 1, 1, 1)
7K (3.4, 2, 2, 1, 1, 1, 1)

Z(Q,QN) = FDA(D, CPM, CPS, CDM, CDS, SDM, SDS)$

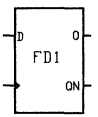
LSI LOGIC CORP

WORKSTATION WC. DELAY 09/25/84

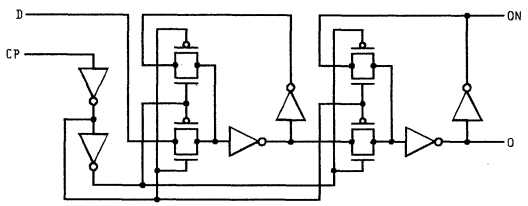
(RISE/FALL) DAISY ⌂ MENTOR = 10.8 / 9.2 VALID = 10

FD1 — DFF — FD1

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

Q OUTPUT		FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	GATES
3000 Series	TPLH	9.3ns	10.2	11.1	12.1	15.8	5
	TPHL	7.0	7.4	7.9	8.4	10.4	
5000 Series	TPLH	5.8	6.6	7.5	8.3	11.7	5
	TPHL	4.4	5.0	5.5	6.0	8.1	
7000 Series	TPLH	3.4	3.9	4.3	4.7	6.3	5
	TPHL	2.8	3.0	3.2	3.3	4.1	

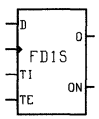
INPUT LOADING: 3K (2.3, 1)
5K (3.8, 1)
7K (3.4, 1)

Z(Q,QN) = FD1(D, CP)$

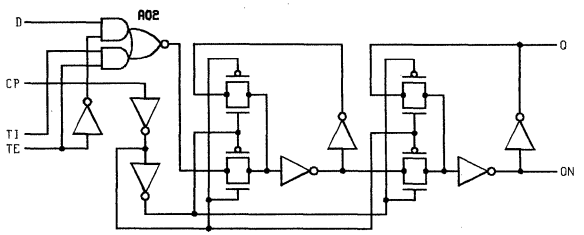
WORKSTATION WC. DELAY **LSI LOGIC CORP** 09/25/84
(RISE/FALL) DAISY ∩ MENTOR = 12.7 / 13.2 VALID = 13

FD1S — DFF WITH SCAN TEST INPUTS — FD1S

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

Q OUTPUT		FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	GATES
3000 Series	TPLH	12.4ns	13.2	14.0	14.9	18.7	8
	TPHL	12.5	12.8	13.2	13.7	15.6	
5000 Series	TPLH	5.9	6.7	7.5	8.3	11.7	8
	TPHL	6.2	6.7	7.2	7.7	9.7	
7000 Series	TPLH	3.7	4.1	4.5	4.9	6.6	8
	TPHL	4.0	4.2	4.5	4.8	5.8	

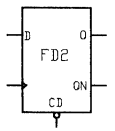
INPUT LOADING: 3K (1, 1, 1, 2)
5K (1, 1, 1, 2)
7K (1, 1, 1, 2)

Z(Q,QN) = FD1S(D, CP, TI, TE)$

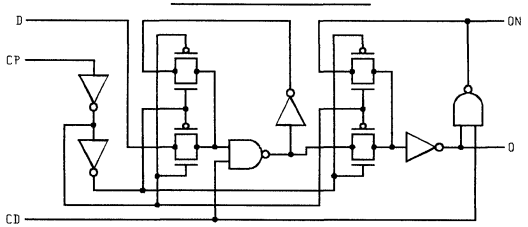
WORKSTATION WC. DELAY **LSI LOGIC CORP** 09/25/84
(RISE/FALL) DAISY ∩ MENTOR = 13.2 / 13.2 VALID = 13

FD2 — DFF WITH CLEAR DIRECT — FD2

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

Q OUTPUT		F0 = 1	F0 = 2	F0 = 3	F0 = 4	F0 = 8	GATES
3000 Series	TPLH	9.7ns	10.6	11.5	12.5	16.2	6
	TPHL	7.0	7.4	7.9	8.4	10.4	
5000 Series	TPLH	5.8	6.6	7.5	8.3	11.7	6
	TPHL	4.4	5.0	5.5	6.0	8.1	
7000 Series	TPLH	3.4	3.9	4.3	4.7	6.3	6
	TPHL	2.8	3.0	3.2	3.3	4.1	

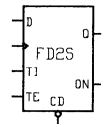
INPUT LOADING: 3K (2.2, 1, 2)
5K (3.7, 1, 2)
7K (3.4, 1, 2)

Z(Q,QN) = FD2(D, CP, CD)$

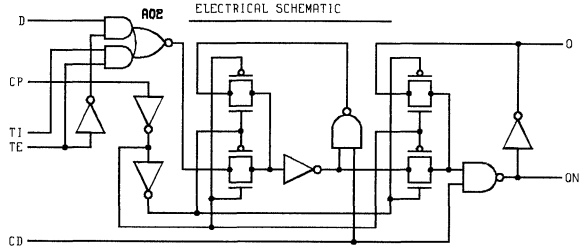
WORKSTATION WC. DELAY — **LSI LOGIC CORP** — 09/25/84
(RISE/FALL) DAISY Ω MENTOR = 13.4 / 9.2 VALID = 12

FD2S — DFF WITH SCAN TEST INPUTS, CLEAR DIRECT — FD2S

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

Q OUTPUT		F0 = 1	F0 = 2	F0 = 3	F0 = 4	F0 = 8	GATES
3000 Series	TPLH	14.0ns	14.8	15.6	16.5	20.3	9
	TPHL	12.5	12.8	13.2	13.7	15.6	
5000 Series	TPLH	5.9	6.7	7.5	8.3	11.7	9
	TPHL	6.2	6.7	7.2	7.7	9.7	
7000 Series	TPLH	3.7	4.1	4.5	4.9	6.6	9
	TPHL	4.0	4.2	4.5	4.8	5.8	

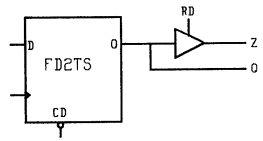
INPUT LOADING: 3K (1, 1, 2, 1, 2)
5K (1, 1, 2, 1, 2)
7K (1, 1, 2, 1, 2)

Z(Q,QN) = FD2S(D, CP, CD, TI, TE)$

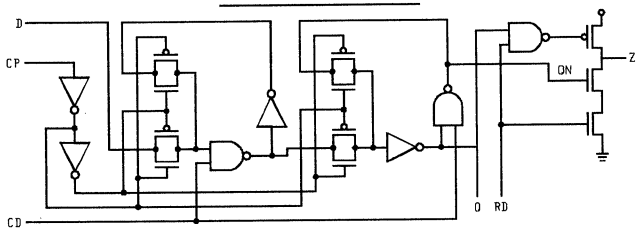
WORKSTATION WC. DELAY — **LSI LOGIC CORP** — 09/25/84
(RISE/FALL) DAISY Ω MENTOR = 14.6 / 13.2 VALID = 14

FD2TS — DFF WITH CLEAR DIRECT AND ADDED TRISTATE OUTPUT — FD2TS

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

RD TO Z OUTPUT		F0 = 1	F0 = 2	F0 = 3	F0 = 4	F0 = 8	GATES
5000 Series	TPLH	2.2ns	2.6	3.1	3.5	5.2	9
	TPHL	0.8	1.1	1.3	1.6	2.6	
7000 Series	TPLH	1.7	1.9	2.1	2.3	3.1	9
	TPHL	0.5	0.6	0.8	0.9	1.5	

INPUT LOADING: 5K (3.7, 1, 2, 2)
7K (3.4, 1, 2, 2)

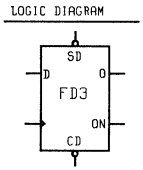
Z(Z, Q) = FD2TS(D, CP, CD, RD)$

LSI LOGIC CORP

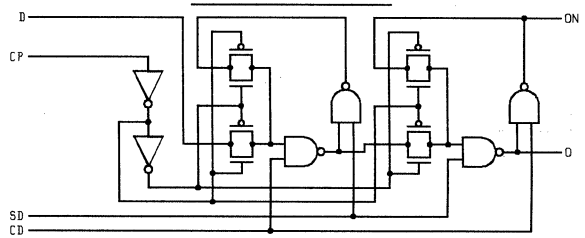
WORKSTATION WC. DELAY 09/25/84
(RISE/FALL) DAISY ∩ MENTOR = 4.7 / 3.2 VALID = 4

FD3 — DFF WITH CLEAR DIRECT, SET DIRECT — FD3

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

Q OUTPUT		F0 = 1	F0 = 2	F0 = 3	F0 = 4	F0 = 8	GATES
3000 Series	TPLH	10.5ns	11.3	12.3	13.2	16.9	7
	TPHL	9.1	9.7	10.4	11.1	14.0	
5000 Series	TPLH	5.8	6.6	7.5	8.3	11.7	7
	TPHL	4.4	5.0	5.5	6.0	8.1	
7000 Series	TPLH	3.4	3.9	4.3	4.7	6.3	7
	TPHL	2.8	3.0	3.2	3.3	4.1	

INPUT LOADING: 3K (2.2, 1, 2, 2)
5K (3.7, 1, 2, 2)
7K (3.4, 1, 2, 2)

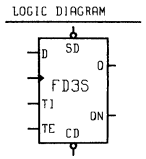
Z(Q,QN) = FD3(D, CP, CD, SD)$

LSI LOGIC CORP

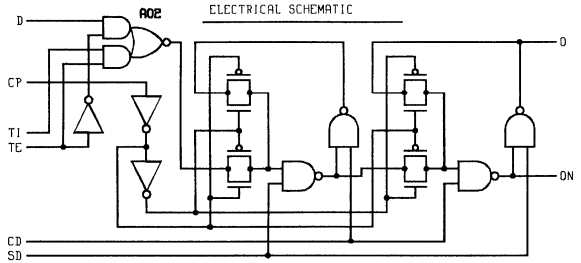
WORKSTATION WC. DELAY 09/25/84
(RISE/FALL) DAISY ∩ MENTOR = 13.1/ 11.1 VALID = 12

FD3S — DFF WITH SCAN TEST INPUTS CLEAR DIRECT, SET DIRECT — FD3S

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

Q OUTPUT		F0 = 1	F0 = 2	F0 = 3	F0 = 4	F0 = 8	GATES
3000 Series	TPLH	13.8ns	14.6	15.4	16.3	20.1	10
	TPHL	14.5	15.1	15.7	16.5	19.5	
5000 Series	TPLH	5.9	6.7	7.5	8.3	11.7	10
	TPHL	6.2	6.7	7.2	7.7	9.7	
7000 Series	TPLH	3.7	4.1	4.5	4.9	6.6	10
	TPHL	4.0	4.2	4.5	4.8	5.8	

INPUT LOADING: 3K (1, 1, 2, 2, 1, 2)
5K (1, 1, 2, 2, 1, 2)
7K (1, 1, 2, 2, 1, 2)

Z(Q,QN) = FD3S(D, CP, CD, SD, TI, TE)$

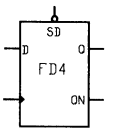
LSI LOGIC CORP

WORKSTATION WC. DELAY
(RISE/FALL) DAISY ∩ MENTOR = 14.3 / 15.3 VALID = 15

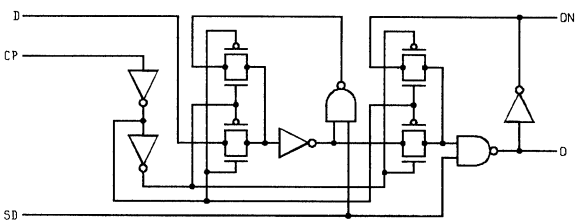
09/25/84

FD4 — DFF WITH SET DIRECT — FD4

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

Q OUTPUT		F0 = 1	F0 = 2	F0 = 3	F0 = 4	F0 = 8	GATES
3000 Series	TPLH	11.5ns	12.3	13.2	14.1	17.8	6
	TPHL	10.4	11.0	11.7	12.5	15.5	
5000 Series	TPLH	5.8	6.6	7.5	8.3	11.7	6
	TPHL	4.4	5.0	5.5	6.0	8.1	
7000 Series	TPLH	3.4	3.9	4.3	4.7	6.3	6
	TPHL	2.8	3.0	3.2	3.3	4.1	

INPUT LOADING: 3K (2.3, 1, 2)
5K (3.8, 1, 2)
7K (3.4, 1, 2)

Z(Q,QN) = FD4(D, CP, SD)$

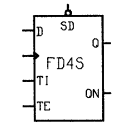
LSI LOGIC CORP

WORKSTATION WC. DELAY
(RISE/FALL) DAISY ∩ MENTOR = 12.2 / 11.1 VALID = 12

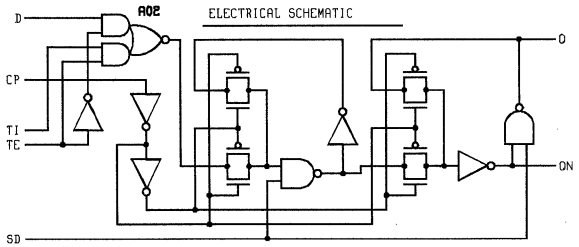
09/25/84

FD4S — DFF WITH SCAN TEST INPUTS, SET DIRECT — FD4S

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

Q OUTPUT		F0 = 1	F0 = 2	F0 = 3	F0 = 4	F0 = 8	GATES
3000 Series	TPLH	12.4ns	13.2	14.0	14.9	18.7	9
	TPHL	14.4	15.0	15.6	16.4	19.4	
5000 Series	TPLH	5.9	6.7	7.5	8.3	11.7	9
	TPHL	6.2	6.7	7.2	7.7	9.7	
7000 Series	TPLH	3.7	4.1	4.5	4.9	6.6	9
	TPHL	4.0	4.2	4.5	4.8	5.8	

INPUT LOADING: 3K (1, 1, 2, 1, 2)
5K (1, 1, 2, 1, 2)
7K (1, 1, 2, 1, 2)

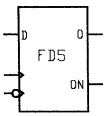
Z(Q,QN) = FD4S(D, CP, SD, TI, TE)$

LSI LOGIC CORP

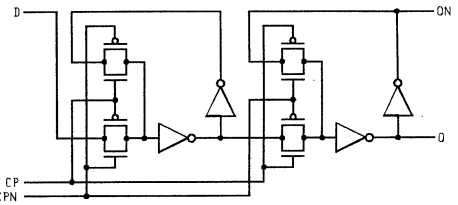
WORKSTATION WC. DELAY 09/25/84
(RISE/FALL) DAISY Ω MENTOR = 13.2 / 15.1 VALID = 14

FD5 — DFF WITHOUT BUFFERED CLOCKS — FD5

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

Q OUTPUT		F0 = 1	F0 = 2	F0 = 3	F0 = 4	F0 = 8	GATES
3000 Series	TPLH	8.5ns	9.3	10.2	11.1	14.8	4
	TPHL	6.2	6.5	6.9	7.4	9.4	
5000 Series	TPLH	4.1	4.9	5.7	6.6	9.9	4
	TPHL	3.3	3.8	4.3	4.8	6.8	
7000 Series	TPLH	2.4	2.8	3.2	3.6	5.1	4
	TPHL	2.4	2.7	2.9	3.2	4.3	

INPUT LOADING: 3K (2.3, 2, 2)
5K (3.8, 2, 2)
7K (3.4, 2, 2)

Z(Q,QN) = FD5(D, CP, CPN)$

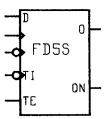
LSI LOGIC CORP

WORKSTATION WC. DELAY 09/25/84
(RISE/FALL) DAISY Ω MENTOR = 8.0 / 6.6 VALID = 8

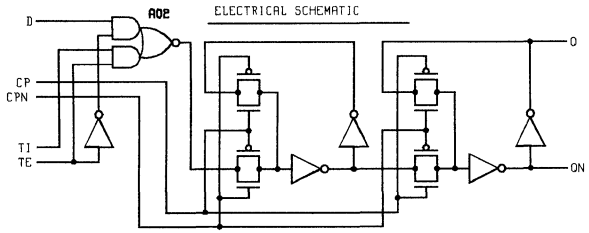
FD5S FD5S

DFF WITHOUT BUFFERED CLOCKS, WITH SCAN TEST INPUTS

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

Q OUTPUT		FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	GATES
3000 Series	TPLH	11.0ns	11.8	12.6	13.5	17.3	7
	TPHL	9.9	10.2	10.6	11.1	13.0	
5000 Series	TPLH	4.8	5.6	6.4	7.3	10.5	7
	TPHL	4.5	5.0	5.5	6.0	8.0	
7000 Series	TPLH	3.3	3.7	4.1	4.4	6.0	7
	TPHL	2.9	3.1	3.4	3.7	4.7	

INPUT LOADING: 3K (1, 2, 2, 1, 2)
5K (1, 2, 2, 1, 2)
7K (1, 2, 2, 1, 2)

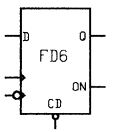
Z(Q,QN) = FD5S(D, CP, CPN, TI, TE)$

WORKSTATION WC. DELAY **LSI LOGIC CORP** 09/25/84
(RISE/FALL) DAISY Ω MENTOR = 10.8 / 8.7 VALID = 10

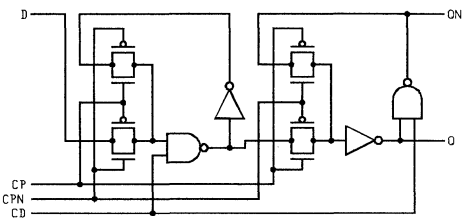
FD6 FD6

DFF WITHOUT BUFFERED CLOCKS, WITH CLEAR DIRECT

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

Q OUTPUT		FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	GATES
3000 Series	TPLH	7.0ns	7.9	8.8	9.8	13.5	5
	TPHL	5.0	5.4	5.9	6.4	8.4	
5000 Series	TPLH	4.1	4.9	5.7	6.6	9.9	5
	TPHL	3.3	3.8	4.3	4.8	6.8	
7000 Series	TPLH	2.4	2.8	3.2	3.6	5.1	5
	TPHL	2.4	2.7	2.9	3.2	4.3	

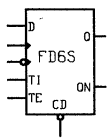
INPUT LOADING: 3K (2.2, 2, 2, 2)
5K (3.7, 2, 2, 2)
7K (3.4, 2, 2, 2)

Z(Q,QN) = FD6(D, CP, CPN, CD)$

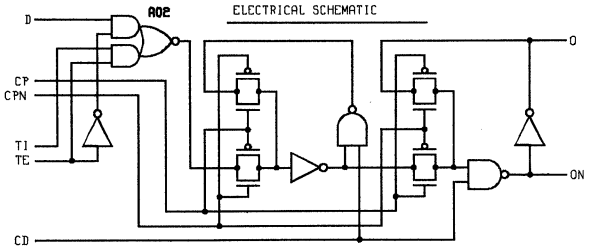
WORKSTATION WC. DELAY **LSI LOGIC CORP** 09/25/84
(RISE/FALL) DAISY Ω MENTOR = 8.7 / 6.6 VALID = 8

FD6S — DFF WITHOUT BUFFERED CLOCKS, WITH SCAN TEST INPUTS, CLEAR DIRECT — FD6S

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

Q OUTPUT		F0 = 1	F0 = 2	F0 = 3	F0 = 4	F0 = 8	GATES
3000 Series	TPLH	12.9ns	13.7	14.5	15.4	19.2	8
	TPHL	8.9	9.2	9.6	10.1	12.0	
5000 Series	TPLH	4.8	5.6	6.4	7.3	10.5	8
	TPHL	4.5	5.0	5.5	6.0	8.0	
7000 Series	TPLH	3.3	3.7	4.1	4.4	6.0	8
	TPHL	2.9	3.1	3.4	3.7	4.7	

INPUT LOADING: 3K (1, 2, 2, 2, 1, 2)
5K (1, 2, 2, 2, 1, 2)
7K (1, 2, 2, 2, 1, 2)

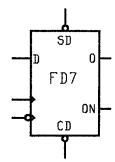
Z(Q,QN) = FD6S(D, CP, CPN, CD, TI, TE)$

LSI LOGIC CORP

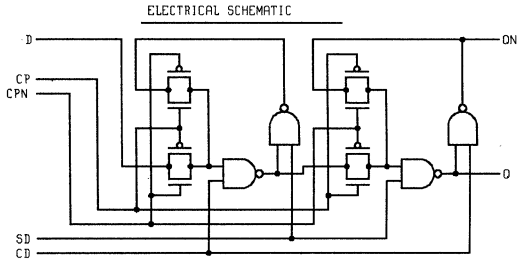
WORKSTATION WC. DELAY 09/25/84
(RISE/FALL) DAISY ∩ MENTOR = 10.8 / 8.9 VALID = 10

FD7 — DFF WITHOUT BUFFERED CLOCKS, WITH CLEAR DIRECT, SET DIRECT — FD7

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

Q OUTPUT		F0 = 1	F0 = 2	F0 = 3	F0 = 4	F0 = 8	GATES
3000 Series	TPLH	7.8ns	8.7	9.6	10.5	14.3	6
	TPHL	7.3	7.9	8.6	9.3	12.2	
5000 Series	TPLH	4.1	4.9	5.7	6.6	9.9	6
	TPHL	3.3	3.8	4.3	4.8	6.8	
7000 Series	TPLH	2.4	2.8	3.2	3.6	5.1	6
	TPHL	2.4	2.7	2.9	3.2	4.3	

INPUT LOADING: 3K (2.2, 2, 2, 2, 2)
5K (3.7, 2, 2, 2, 2)
7K (3.4, 2, 2, 2, 2)

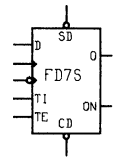
Z(Q,QN) = FD7(D, CP, CPN, CD, SD)$

LSI LOGIC CORP

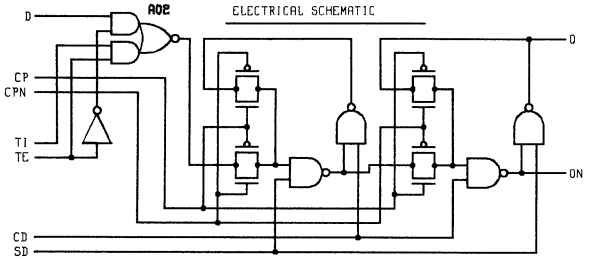
WORKSTATION WC. DELAY 09/25/84
(RISE/FALL) DAISY ∩ MENTOR = 8.4 / 8.7 VALID = 9

FD7S — DFF WITHOUT BUFFERED CLOCKS, WITH SCAN TEST INPUTS, CLEAR DIRECT, SET DIRECT — FD7S

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

Q OUTPUT		F0 = 1	F0 = 2	F0 = 3	F0 = 4	F0 = 8	GATES
3000 Series	TPLH	12.2ns	13.0	13.8	14.7	18.5	9
	TPHL	12.1	12.7	13.3	14.1	17.1	
5000 Series	TPLH	4.8	5.6	6.4	7.3	10.5	9
	TPHL	4.5	5.0	5.5	6.0	8.0	
7000 Series	TPLH	3.3	3.7	4.1	4.4	6.0	9
	TPHL	2.9	3.1	3.4	3.7	4.7	

INPUT LOADING: 3K (1, 2, 2, 2, 2, 1, 2)
5K (1, 2, 2, 2, 2, 1, 2)
7K (1, 2, 2, 2, 2, 1, 2)

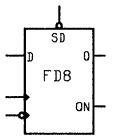
Z(Q,QN) = FD7S(D, CP, CPN, CD, SD, TI, TE)$

LSI LOGIC CORP

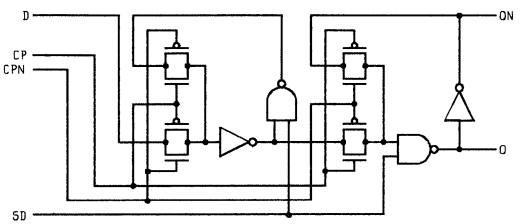
WORKSTATION WC. DELAY 09/25/84
(RISE/FALL) DAISY Ω MENTOR = 11.5/ 11.1 VALID = 12

FD8 — DFF WITHOUT BUFFERED CLOCKS, WITH SET DIRECT — FD8

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

Q OUTPUT		F0 = 1	F0 = 2	F0 = 3	F0 = 4	F0 = 8	GATES
3000 Series	TPLH	7.4ns	8.2	9.2	10.1	13.8	5
	TPHL	7.3	7.9	8.6	9.3	12.2	
5000 Series	TPLH	4.1	4.9	5.7	6.6	9.9	5
	TPHL	3.3	3.8	4.3	4.8	6.8	
7000 Series	TPLH	2.4	2.8	3.2	3.6	5.1	5
	TPHL	2.4	2.7	2.9	3.2	4.3	

INPUT LOADING: 3K (2.3, 2, 2, 2)
5K (3.8, 2, 2, 2)
7K (3.4, 2, 2, 2)

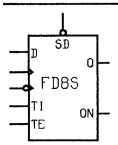
Z(Q,QN) = FD8(D, CP, CPN, SD)$

LSI LOGIC CORP

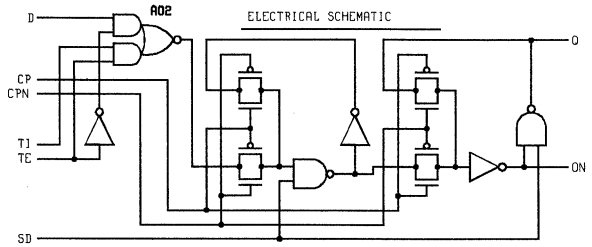
WORKSTATION WC. DELAY 09/25/84
(RISE/FALL) DAISY Ω MENTOR = 8.7 / 8.7 VALID = 9

FD8S — DFF WITHOUT BUFFERED CLOCKS, WITH SCAN TEST INPUTS, SET DIRECT — FD8S

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

Q OUTPUT		F0 = 1	F0 = 2	F0 = 3	F0 = 4	F0 = 8	GATES
3000 Series	TPLH	10.8ns	11.6	12.4	13.3	17.1	8
	TPHL	12.0	12.6	13.2	14.0	17.0	
5000 Series	TPLH	4.8	5.6	6.4	7.3	10.5	8
	TPHL	4.5	5.0	5.5	6.0	8.0	
7000 Series	TPLH	3.3	3.7	4.1	4.4	6.0	8
	TPHL	2.9	3.1	3.4	3.7	4.7	

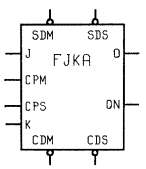
INPUT LOADING: 3K (1, 2, 2, 2, 1, 2)
5K (1, 2, 2, 2, 1, 2)
7K (1, 2, 2, 2, 1, 2)

Z(Q,QN) = FD8S(D, CP, CPN, SD, TI, TE)$

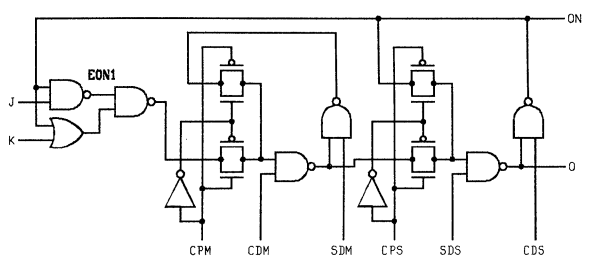
WORKSTATION WC. DELAY — **LSI LOGIC CORP** — 09/25/84
(RISE/FALL) DAISY Ω MENTOR = 10.4 / 11.0 VALID = 11

FJKA — JK FLIP FLOP WITH SEPERATE MASTER Ω SLAVE CLOCKS, CLEAR DIRECT Ω SET DIRECT. — FJKA

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

Q OUTPUT		F0 = 1	F0 = 2	F0 = 3	F0 = 4	F0 = 8	GATES
5000 Series	TPLH	6.7ns	7.5	8.4	9.2	12.5	10
	TPHL	5.2	5.7	6.2	6.8	8.9	
7000 Series	TPLH	3.4	3.8	4.2	4.6	6.2	10
	TPHL	3.2	3.5	3.7	4.0	5.1	

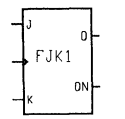
INPUT LOADING: 5K (1, 1, 2, 2, 1, 1, 1, 1)
7K (1, 1, 2, 2, 1, 1, 1, 1)

Z(Q,QN) = FJKA(J, K, CPM, CPS, CDM, CDS, SDM, SDS)$

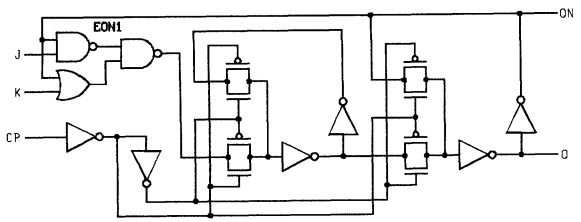
WORKSTATION WC. DELAY — **LSI LOGIC CORP** — 09/25/84
(RISE/FALL) DAISY Ω MENTOR = 13.9 / 10.8 VALID = 13

FJK1 — JKFF — FJK1

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

Q OUTPUT		F0 = 1	F0 = 2	F0 = 3	F0 = 4	F0 = 8	GATES
3000 Series	TPLH	9.2ns	10.1	11.0	12.0	15.7	8
	TPHL	6.9	7.3	7.8	8.3	10.3	
5000 Series	TPLH	6.7	7.5	8.4	9.2	12.5	8
	TPHL	5.2	5.7	6.2	6.8	8.9	
7000 Series	TPLH	3.4	3.9	4.3	4.7	6.3	8
	TPHL	2.8	3.0	3.2	3.3	4.1	

INPUT LOADING: 3K (1, 1, 1)
5K (1, 1, 1)
7K (1, 1, 1)

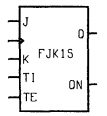
Z(Q,QN) = FJK1(J, K, CP)$

LSI LOGIC CORP

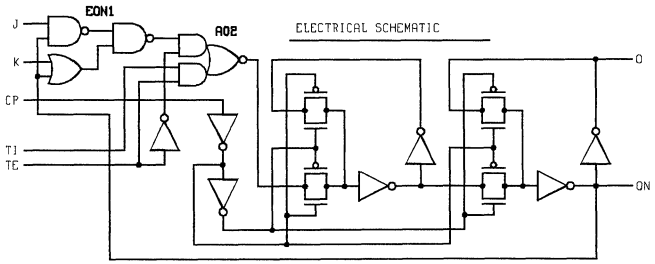
WORKSTATION WC. DELAY 09/25/84
(RISE/FALL) DAISY Ω MENTOR = 12.7/ 9.0 VALID = 11

FJK1S — JKFF WITH SCAN TEST INPUTS — FJK1S

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

Q OUTPUT		F0 = 1	F0 = 2	F0 = 3	F0 = 4	F0 = 8	GATES
3000 Series	TPLH	14.5ns	15.1	16.0	16.8	20.6	11
	TPHL	14.6	14.8	15.2	15.6	17.6	
5000 Series	TPLH	6.6	7.5	8.3	9.1	12.4	10
	TPHL	6.5	7.0	7.5	8.0	10.0	
7000 Series	TPLH	4.0	4.4	4.8	5.2	6.9	10
	TPHL	4.3	4.6	4.8	5.1	6.2	

INPUT LOADING: 3K (1, 1, 1, 1, 2)
5K (1, 1, 1, 1, 2)
7K (1, 1, 1, 1, 2)

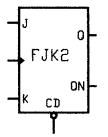
Z(Q,QN) = FJK1S(J, K, CP, TI, TE)$

LSI LOGIC CORP

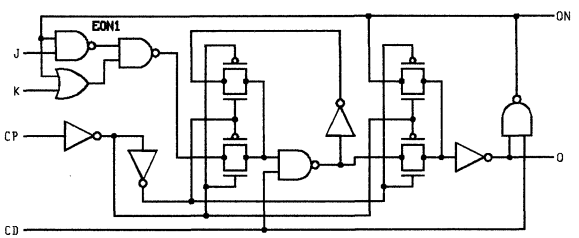
WORKSTATION WC. DELAY 09/25/84
(RISE/FALL) DAISY Ω MENTOR = 14.1 / 13.6 VALID = 14

FJK2 — JKFF WITH CLEAR DIRECT — FJK2

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

Q OUTPUT		F0 = 1	F0 = 2	F0 = 3	F0 = 4	F0 = 8	GATES
3000 Series	TPLH	9.7ns	10.6	11.5	12.5	16.2	9
	TPHL	6.9	7.3	7.8	8.3	10.3	
5000 Series	TPLH	6.7	7.5	8.4	9.2	12.5	9
	TPHL	5.2	5.7	6.2	6.8	8.9	
7000 Series	TPLH	3.4	3.9	4.3	4.7	6.3	9
	TPHL	2.8	3.0	3.2	3.3	4.1	

INPUT LOADING: 3K (1, 1, 1, 2)
5K (1, 1, 1, 2)
7K (1, 1, 1, 2)

Z(Q,QN) = FJK2(J, K, CP, CD)$

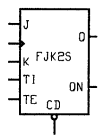
LSI LOGIC CORP

WORKSTATION WC. DELAY
(RISE/FALL) DAISY ∩ MENTOR = 13.4 / 9.0 VALID = 11

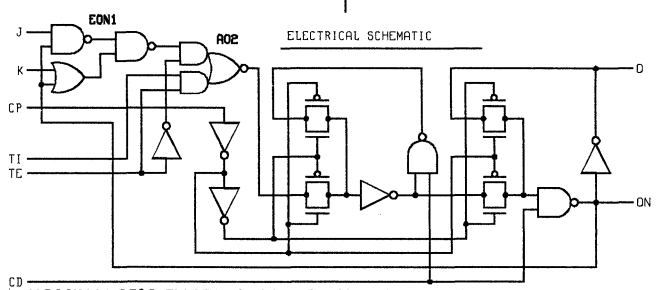
09/25/84

FJK2S — JKFF WITH SCAN TEST INPUTS, CLEAR DIRECT — FJK2S

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

Q OUTPUT		F0 = 1	F0 = 2	F0 = 3	F0 = 4	F0 = 8	GATES
3000 Series	TPLH	15.8ns	16.6	17.4	18.3	22.1	12
	TPHL	15.0	15.3	15.7	16.2	18.1	
5000 Series	TPLH	6.5	7.3	8.2	9.0	12.3	11
	TPHL	6.6	7.1	7.6	8.1	10.1	
7000 Series	TPLH	3.9	4.3	4.7	5.1	6.8	11
	TPHL	4.4	4.6	4.9	5.2	6.2	

INPUT LOADING: 3K (1, 1, 1, 2, 1, 2)
5K (1, 1, 1, 2, 1, 2)
7K (1, 1, 1, 2, 1, 2)

Z(Q,QN) = FJK2S(J, K, CP, CD, TI, TE)$

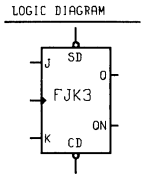
LSI LOGIC CORP

WORKSTATION WC. DELAY
(RISE/FALL) DAISY ∩ MENTOR = 14.6 / 13.4 VALID = 14

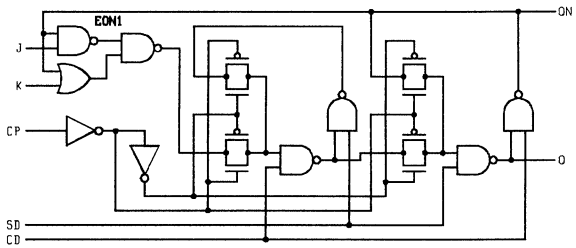
09/25/84

FJK3 — JKFF WITH CLEAR DIRECT, SET DIRECT — FJK3

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

Q OUTPUT		F0 = 1	F0 = 2	F0 = 3	F0 = 4	F0 = 8	GATES
3000 Series	TPLH	10.5ns	11.3	12.3	13.2	16.9	10
	TPHL	9.1	9.7	10.4	11.1	14.0	
5000 Series	TPLH	6.7	7.5	8.4	9.2	12.5	10
	TPHL	5.2	5.7	6.2	6.8	8.9	
7000 Series	TPLH	3.4	3.9	4.3	4.7	6.3	10
	TPHL	2.8	3.0	3.2	3.3	4.1	

INPUT LOADING: 3K (1, 1, 1, 2, 2)
5K (1, 1, 1, 2, 2)
7K (1, 1, 1, 2, 2)

Z(Q,QN) = FJK3(J, K, CP, CD, SD)$

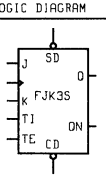
LSI LOGIC CORP

WORKSTATION WC. DELAY
(RISE/FALL) DAISY ∩ MENTOR = 13.1 / 11.1 VALID = 12

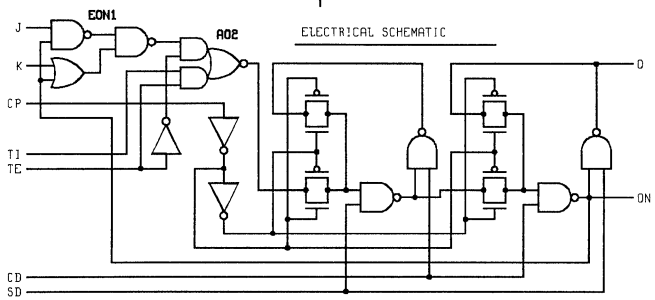
09/25/84

FJK3S — JKFF WITH SCAN TEST INPUTS, CLEAR DIRECT, SET DIRECT — FJK3S

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

Q OUTPUT		F0 = 1	F0 = 2	F0 = 3	F0 = 4	F0 = 8	GATES
3000 Series	TPLH	15.6ns	16.4	17.2	18.1	21.9	13
	TPHL	16.8	17.4	18.0	18.8	21.8	
5000 Series	TPLH	6.5	7.3	8.2	9.0	12.3	12
	TPHL	6.6	7.1	7.6	8.1	10.1	
7000 Series	TPLH	3.9	4.3	4.7	5.1	6.8	12
	TPHL	4.4	4.6	4.9	5.2	6.2	

INPUT LOADING: 3K (1, 1, 1, 2, 2, 1, 2)
5K (1, 1, 1, 2, 2, 1, 2)
7K (1, 1, 1, 2, 2, 1, 2)

Z(Q,QN) = FJK3S(J, K, CP, CD, SD, TI, TE)$

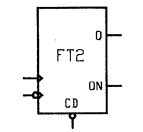
LSI LOGIC CORP

WORKSTATION WC. DELAY
(RISE/FALL) DAISY ∩ MENTOR = 14.3 / 15.1 VALID = 15

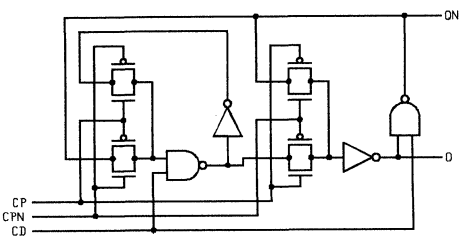
09/25/84

FT2 TOGGLE FF WITHOUT BUFFERED CLOCKS, WITH CLEAR DIRECT FT2

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

Q OUTPUT		F0 = 1	F0 = 2	F0 = 3	F0 = 4	F0 = 8	GATES
3000 Series	TPLH	6.9ns	7.8	8.7	9.7	13.4	5
	TPHL	5.0	5.4	5.9	6.4	8.4	
5000 Series	TPLH	4.1	4.9	5.7	6.6	9.9	5
	TPHL	3.3	3.8	4.3	4.8	6.8	
7000 Series	TPLH	2.4	2.8	3.2	3.6	5.1	5
	TPHL	2.4	2.7	2.9	3.2	4.3	

INPUT LOADING: 3K (2, 2, 2)
5K (2, 2, 2)
7K (2, 2, 2)

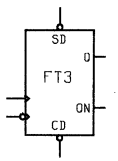
Z(Q,QN) = FT2(CP, CPN, CD)$

LSI LOGIC CORP

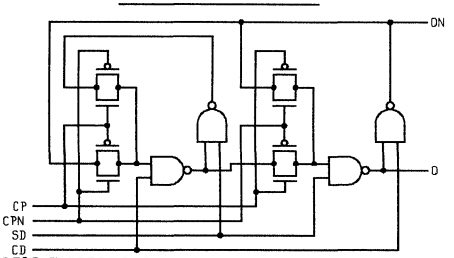
WORKSTATION WC. DELAY 09/25/84
(RISE/FALL) DAISY ∩ MENTOR = 8.7 / 6.6 VALID = 8

FT3 TOGGLE FLIPFLOP WITHOUT BUFFERED CLOCKS, WITH CLEAR DIRECT, SET DIRECT FT3

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

Q OUTPUT		F0 = 1	F0 = 2	F0 = 3	F0 = 4	F0 = 8	GATES
3000 Series	TPLH	7.7ns	8.5	9.5	10.4	14.1	6
	TPHL	7.2	7.8	8.5	9.2	12.1	
5000 Series	TPLH	4.1	4.9	5.7	6.6	9.9	6
	TPHL	3.3	3.8	4.3	4.8	6.8	
7000 Series	TPLH	2.4	2.8	3.2	3.6	5.1	6
	TPHL	2.4	2.7	2.9	3.2	4.3	

INPUT LOADING: 3K (2, 2, 2, 2)
5K (2, 2, 2, 2)
7K (2, 2, 2, 2)

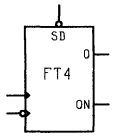
Z(Q,QN) = FT3(CP, CPN, CD, SD)$

LSI LOGIC CORP

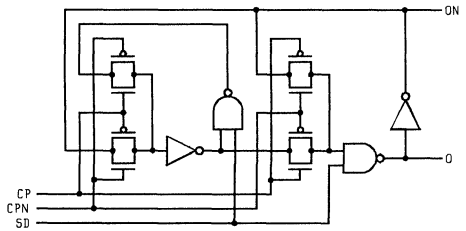
WORKSTATION WC. DELAY 09/25/84
(RISE/FALL) DAISY ∩ MENTOR = 8.4 / 8.2 VALID = 9

FT4 — TOGGLE FLIPFLOP WITHOUT BUFFERED CLOCKS, WITH SET DIRECT — FT4

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

Q OUTPUT		F0 = 1	F0 = 2	F0 = 3	F0 = 4	F0 = 8	GATES
3000 Series	TPLH	7.3ns	8.1	9.1	10.0	13.7	5
	TPHL	7.2	7.8	8.5	9.2	12.1	
5000 Series	TPLH	4.1	4.9	5.7	6.6	9.9	5
	TPHL	3.3	3.8	4.3	4.8	6.8	
7000 Series	TPLH	2.4	2.8	3.2	3.6	5.1	5
	TPHL	2.4	2.7	2.9	3.2	4.3	

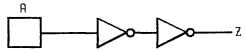
INPUT LOADING: 3K (2, 2, 2)
5K (2, 2, 2)
7K (2, 2, 2)

Z(Q,QN) = FT4(CP, CPN, SD)$

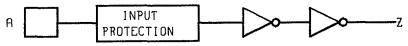
WORKSTATION WC. DELAY — **LSI LOGIC CORP** — 09/25/84
(RISE/FALL) DAISY ∩ MENTOR = 8.7 / 8.2 VALID = 9

IBUF — INPUT PAD WITH BUFFER FOR CMOS INPUT — IBUF

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

		F0 = 1	F0 = 2	F0 = 3	F0 = 4	F0 = 8	GATES
3000 Series	TPLH	5.8ns	6.2	6.7	7.2	9.3	1
	TPHL	4.9	5.1	5.4	5.7	6.8	
5000 Series	TPLH	2.4	2.5	2.7	2.8	3.3	0
	TPHL	2.6	2.7	2.8	2.9	3.2	
7000 Series	TPLH	3.1	3.2	3.3	3.4	3.7	0
	TPHL	2.9	2.9	3.0	3.0	3.2	

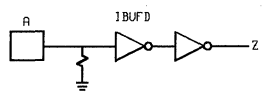
Z = IBUF(A)$

WORKSTATION WC. DELAY — **LSI LOGIC CORP** — 09/25/84
(RISE/FALL) DAISY ∩ MENTOR = 1.9 / 2.1 VALID = 2

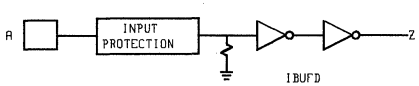
IBUFD IBUFD

INPUT PAD WITH PULL DOWN AND BUFFER FOR CMOS INPUT

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

		F0 = 1	F0 = 2	F0 = 3	F0 = 4	F0 = 8	GATES
3000 Series	TPLH	8.6	9.0	9.5	10.0	12.1	2
	TPHL	8.6	9.0	9.4	9.9	11.9	
5000 Series	TPLH	2.4	2.5	2.7	2.8	3.3	0
	TPHL	2.6	2.7	2.8	2.9	3.2	
7000 Series	TPLH	3.1	3.2	3.3	3.4	3.7	0
	TPHL	4.0	4.0	4.1	4.1	4.3	

Z = IBUFD(A)$

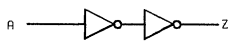
LSI LOGIC CORP

WORKSTATION WC. DELAY 09/25/84
(RISE/FALL) DAISY Ω MENTOR = 2.1 / 1.9 VALID = 2

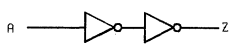
IBUFI IBUFI

BUFFER FOR BIDIRECT CMOS INPUT

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

		F0 = 1	F0 = 2	F0 = 3	F0 = 4	F0 = 8	GATES
3000 Series	TPLH	4.0	4.4	4.9	5.4	7.5	2
	TPHL	3.9	4.3	4.7	5.2	7.2	
5000 Series	TPLH	1.7	1.9	2.1	2.3	3.2	3
	TPHL	2.2	2.3	2.5	2.6	3.2	
7000 Series	TPLH	1.3	1.4	1.5	1.6	2.0	3
	TPHL	1.5	1.6	1.6	1.7	2.1	

INPUT LOADING: 3K (1.5)
5K (1.5)
7K (1.5)

Z = IBUFI(A)$

LSI LOGIC CORP

WORKSTATION WC. DELAY 09/25/84
(RISE/FALL) DAISY Ω MENTOR = 3.6 / 3.4 VALID = 4

IBUFN

(7k only)

Inverting Input Pad With Buffer For Cmos Input

IBUFN

(7k only)

NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

		F0 = 1	F0 = 2	F0 = 4	F0 = 8	F0 = 16	GATES
7000 Series	TPLH	2.1ns	2.3	2.5	3.0	3.9	0
	TPHL	2.0	2.0	2.2	2.5	3.2	

INPUT LOADING: 7K (5)

Z = IBUFN(A)$

FIXED DELAYS [WORKSTATION SOFTWARE DATABOOK]

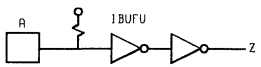
WORST CASE COMMERCIAL DELAYS BASED UPON FO = 2 WITH STATISTICAL WIRE LENGHTS		VALID	DAISY	MENTOR
	TPLH	4	3.5	3.5
	TPHL		3.8	3.8

IBUFU

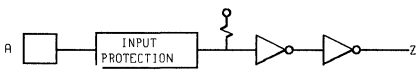
INPUT PAD WITH PULL UP AND BUFFER FOR CMOS INPUT

IBUFU

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

		F0 = 1	F0 = 2	F0 = 3	F0 = 4	F0 = 8	GATES
3000 Series	TPLH	8.6ns	9.0	9.5	10.0	12.1	2
	TPHL	8.6	9.0	9.4	9.9	11.9	
5000 Series	TPLH	2.4	2.5	2.7	2.8	3.3	0
	TPHL	2.6	2.7	2.8	2.9	3.2	
7000 Series	TPLH	3.1	3.2	3.3	3.4	3.7	0
	TPHL	2.9	2.9	3.0	3.0	3.2	

Z = IBUFU(A)$

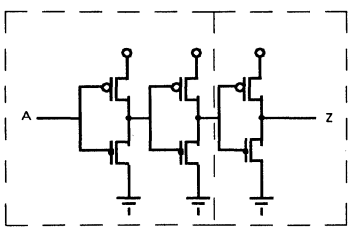
LSI LOGIC CORP

WORKSTATION WC. DELAY 09/25/84

(RISE/FALL) DAISY ∩ MENTOR = 1.9 / 1.9 VALID = 2

ICK1 — Inverting Clock-driver — ICK1

(7k only) (7k only)



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

		F0 = 4	F0 = 8	F0 = 16	F0 = 32	F0 = 64	GATES
7000 Series	TPLH	4.0	4.2	4.5	5.0	6.1	0
	TPHL	4.3	4.4	4.7	5.2	6.2	

TWO I/O CELLS

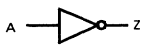
Z = ICK1(A)$

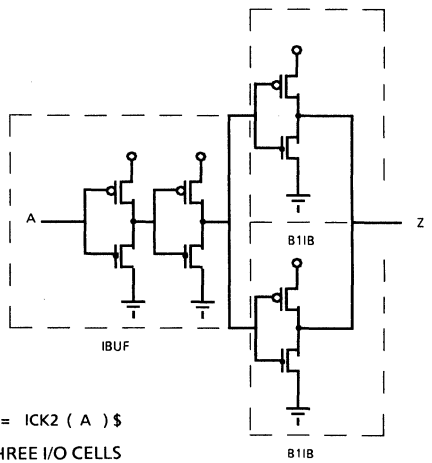
FIXED DELAYS [WORKSTATION SOFTWARE DATABOOK]

WORST CASE COMMERCIAL DELAYS BASED UPON FO = 2 WITH STATISTICAL WIRE LENGHTS		VALID	DAISY	MENTOR
	TPLH	8	8.2	8.2
	TPHL		7.5	7.5

ICK2 — Inverting Clock-driver — ICK2

(7k only) (7k only)





Z = ICK2 (A)$

THREE I/O CELLS

NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

		F0 = 4	F0 = 8	F0 = 16	F0 = 32	F0 = 64	GATES
7000 Series	TPLH	4.4	4.4	4.6	4.9	5.4	0
	TPHL	5.0	5.0	5.2	5.4	5.9	

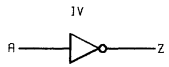
FIXED DELAYS [WORKSTATION SOFTWARE DATABOOK]

WORST CASE COMMERCIAL DELAYS BASED UPON FO = 2 WITH STATISTICAL WIRE LENGHTS		VALID	DAISY	MENTOR
	TPLH	9	8.5	8.5
	TPHL		8.2	8.2

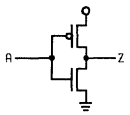
IV IV

SINGLE INVERTER

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

		F0 = 1	F0 = 2	F0 = 3	F0 = 4	F0 = 8	GATES
3000 Series	TPLH	3.7ns	4.6	5.5	6.4	10.2	1
	TPHL	2.3	2.7	3.2	3.7	5.6	
5000 Series	TPLH	2.0	2.8	3.6	4.4	7.7	1
	TPHL	0.8	1.1	1.4	1.7	2.9	
7000 Series	TPLH	1.5	1.9	2.2	2.6	4.2	1
	TPHL	0.8	1.0	1.1	1.3	2.0	

INPUT LOADING: 3K (1)
5K (1)
7K (1)

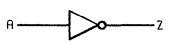
Z = IV(A)$

WORKSTATION WC. DELAY **LSI LOGIC CORP** 09/25/84
(RISE/FALL) DAISY ∩ MENTOR = 5.0 / 2.7 VALID = 4

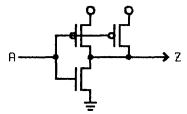
IVA IVA

INVERTER WITH PARALLEL P TRANSISTORS

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

		F0 = 1	F0 = 2	F0 = 3	F0 = 4	F0 = 8	GATES
3000 Series	TPLH	2.9ns	3.3	3.8	4.3	6.4	1
	TPHL	2.9	3.3	3.7	4.2	6.1	
5000 Series	TPLH	1.3	1.7	2.1	2.5	4.2	1
	TPHL	0.9	1.2	1.5	1.8	3.0	
7000 Series	TPLH	1.1	1.3	1.5	1.7	2.5	1
	TPHL	1.1	1.2	1.4	1.6	2.2	

INPUT LOADING: 3K (1.5)
5K (1.5)
7K (1.5)

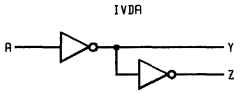
Z = IVA(A)$

WORKSTATION WC. DELAY **LSI LOGIC CORP** 09/25/84
(RISE/FALL) DAISY ∩ MENTOR = 3.3 / 2.7 VALID = 3

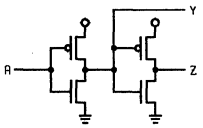
IVDA IVDA

INVERTER INTO INVERTER

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

Z OUTPUT		F0 = 1	F0 = 2	F0 = 3	F0 = 4	F0 = 8	GATES
3000 Series	TPLH	5.9	6.8	7.7	8.6	12.4	1
	TPHL	5.9	6.3	6.8	7.3	9.2	
5000 Series	TPLH	2.8	3.6	4.4	5.2	8.5	1
	TPHL	2.8	3.1	3.4	3.7	4.9	
7000 Series	TPLH	2.3	2.7	3.0	3.4	5.0	1
	TPHL	2.3	2.5	2.6	2.8	3.5	

INPUT LOADING: 3K (1)
5K (1)
7K (1)
WITH Y OUTPUT UNLOADED

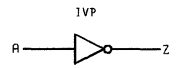
X(Y, Z) = IVDA(A)$

WORKSTATION WC. DELAY **LSI LOGIC CORP** 09/25/84
(RISE/FALL) DAISY Ω MENTOR = 7.3 / 6.7 VALID = 7

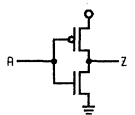
IVP IVP

POWER INVERTER (2 PARALLEL INVERTERS)

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

		F0 = 1	F0 = 2	F0 = 3	F0 = 4	F0 = 8	GATES
3000 Series	TPLH	2.9	3.3	3.8	4.3	6.4	1
	TPHL	2.0	2.2	2.5	2.8	3.9	
5000 Series	TPLH	1.4	1.8	2.2	2.6	4.3	1
	TPHL	0.7	0.9	1.0	1.2	1.8	
7000 Series	TPLH	1.0	1.2	1.4	1.6	2.4	1
	TPHL	0.6	0.7	0.8	0.9	1.3	

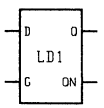
INPUT LOADING: 3K (2)
5K (2)
7K (2)

Z = IVP (A)$

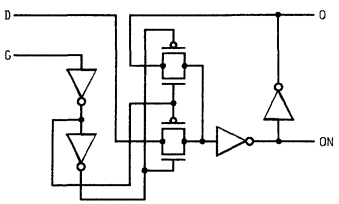
WORKSTATION WC. DELAY **LSI LOGIC CORP** 09/25/84
(RISE/FALL) DAISY Ω MENTOR = 4.3/ 2.6 VALID = 3

LD1 — DLATCH, GATED — LD1

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

Q1 OUTPUT		F0 = 1	F0 = 2	F0 = 3	F0 = 4	F0 = 8	GATES
3000 Series	TPLH	10.4	11.3	12.2	13.2	16.9	3
	TPHL	9.6	10.0	10.5	11.0	13.0	
5000 Series	TPLH	4.8	5.6	6.4	7.3	10.6	3
	TPHL	4.3	4.6	4.9	5.1	6.3	
7000 Series	TPLH	3.0	3.4	3.8	4.2	5.9	3
	TPHL	3.0	3.1	3.3	3.5	4.2	

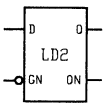
INPUT LOADING: 3K (2.3, 1)
5K (3.8, 1)
7K (3.4, 1)

Z(Q, QN) = LD1 (D, G)$

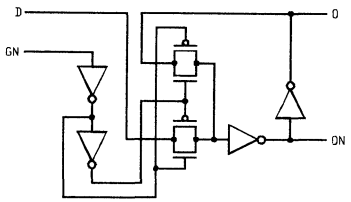
WORKSTATION WC. DELAY — LSI LOGIC CORP — 09/25/84
(RISE/FALL) DAISY Ω MENTOR = 14.6 / 11.4 VALID = 13

LD2 — DLATCH, GATED (GATE ACTIVE LOW) — LD2

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

Q1 OUTPUT		F0 = 1	F0 = 2	F0 = 3	F0 = 4	F0 = 8	GATES
3000 Series	TPLH	11.1	12.0	12.9	13.9	17.6	3
	TPHL	10.0	10.4	10.9	11.4	13.4	
5000 Series	TPLH	5.7	6.5	7.3	8.1	11.4	3
	TPHL	4.6	4.9	5.2	5.5	6.6	
7000 Series	TPLH	3.9	4.3	4.7	5.1	6.6	3
	TPHL	3.3	3.5	3.7	3.8	4.5	

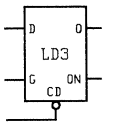
INPUT LOADING: 3K (2.3, 1)
5K (3.8, 1)
7K (3.4, 1)

Z(Q, QN) = LD2 (D, GN)$

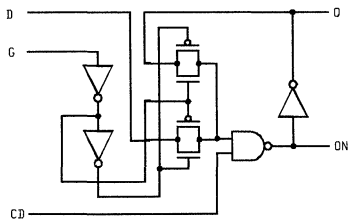
WORKSTATION WC. DELAY — LSI LOGIC CORP — 09/25/84
(RISE/FALL) DAISY Ω MENTOR = 14.6 / 11.4 VALID = 13

LD3 — DLATCH, GATED, CLEAR DIRECT, GATE ACTIVE HIGH — LD3

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

Q1 OUTPUT		F0 = 1	F0 = 2	F0 = 3	F0 = 4	F0 = 8	GATES
5000 Series	TPLH	5.5ns	6.4	7.2	8.0	11.3	4
	TPHL	4.9	5.2	5.5	5.8	6.9	
7000 Series	TPLH	4.5	4.9	5.3	5.7	7.2	4
	TPHL	4.2	4.3	4.5	4.7	5.3	

INPUT LOADING: 5K (3.7, 1, 1)
7K (3.4, 1, 1)

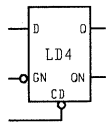
Z(Q, QN) = LD3 (D, G, CD)$

LSI LOGIC CORP

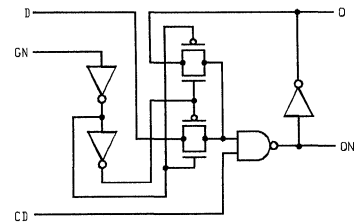
WORKSTATION WC. DELAY 09/25/84
(RISE/FALL) DAISY Ω MENTOR = 14.6/ 11.4 VALID = 13

LD4 (5K ONLY) — DLATCH, GATED, CLEAR DIRECT (GATE ACTIVE LOW) — LD4 (5K ONLY)

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

Q1 OUTPUT		F0 = 1	F0 = 2	F0 = 3	F0 = 4	F0 = 8	GATES
5000 Series	TPLH	6.3ns	7.1	7.9	8.7	12.0	4
	TPHL	5.2	5.5	5.8	6.1	7.3	
7000 Series	TPLH	4.5	4.9	5.3	5.7	7.2	4
	TPHL	4.2	4.3	4.5	4.7	5.3	

INPUT LOADING: 5K (3.7, 1, 1)
7K (3.4, 1, 1)

Z(Q, QN) = LD4 (D, GN, CD)$

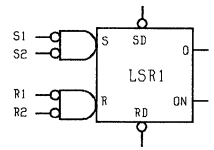
LSI LOGIC CORP

WORKSTATION WC. DELAY 09/25/84
(RISE/FALL) DAISY Ω MENTOR = 14.6/ 11.4 VALID = 13

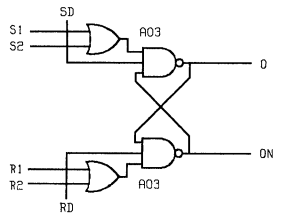
LSR1 — SRLATCH WITH SEPARATE GATED INPUTS, SD, RD

LSR1

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

Q OUTPUT		F0 = 1	F0 = 2	F0 = 3	F0 = 4	F0 = 8	GATES
3000 Series	TPLH	11.3ns	13.4	15.6	17.8	26.6	4
	TPHL	14.6	15.6	16.6	17.5	21.5	
5000 Series	TPLH	4.4	6.0	7.6	9.2	15.6	4
	TPHL	5.8	6.5	7.2	8.0	10.9	
7000 Series	TPLH	3.1	3.7	4.4	5.1	7.8	4
	TPHL	4.4	4.8	5.1	5.5	6.9	

INPUT LOADING: 3K (1, 1, 1, 1, 1, 1)
5K (1, 1, 1, 1, 1, 1)
7K (1, 1, 1, 1, 1, 1)

Z(Q, QN) = LSR1 (S1, S2, SD, R1, R2, RD)$

LSI LOGIC CORP

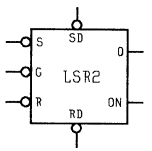
WORKSTATION WC. DELAY
(RISE/FALL) DAISY Ω MENTOR = 12.3/ 7.8 VALID = 10

09/25/84

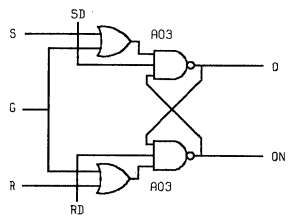
LSR2 — SRLATCH WITH COMMON GATED INPUTS, SD, RD

LSR2

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

Q OUTPUT		F0 = 1	F0 = 2	F0 = 3	F0 = 4	F0 = 8	GATES
3000 Series	TPLH	11.3ns	13.4	15.6	17.8	26.6	4
	TPHL	14.6	15.6	16.6	17.5	21.5	
5000 Series	TPLH	5.5	7.2	8.8	10.4	16.9	4
	TPHL	6.9	7.7	8.4	9.1	12.0	
7000 Series	TPLH	3.1	3.7	4.4	5.1	7.8	4
	TPHL	4.4	4.8	5.1	5.5	6.9	

INPUT LOADING: 3K (1, 1, 2, 1, 1)
5K (1, 1, 2, 1, 1)
7K (1, 1, 2, 1, 1)

Z(Q, QN) = LSR2 (S, R, G, SD, RD)$

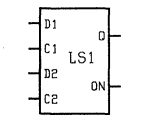
LSI LOGIC CORP

WORKSTATION WC. DELAY
(RISE/FALL) DAISY Ω MENTOR = 6.6 / 10.3 VALID = 10

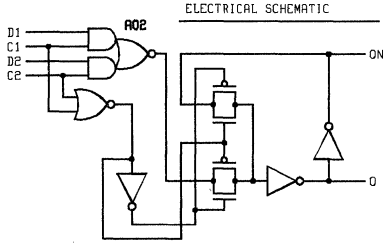
09/25/84

LS1 DLATCH WITH SCAN TEST INPUTS (LSSD) LS1

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

Q1 OUTPUT		F0 = 1	F0 = 2	F0 = 3	F0 = 4	F0 = 8	GATES
3000 Series	TPLH	9.7ns	10.5	11.4	12.3	16.0	6
	TPHL	7.6	7.9	8.3	8.8	10.8	
5000 Series	TPLH	5.5	6.4	7.2	8.0	11.4	6
	TPHL	8.9	9.2	9.6	9.9	11.3	
7000 Series	TPLH	4.2	4.6	5.0	5.4	7.0	6
	TPHL	3.2	3.4	3.5	3.7	4.4	

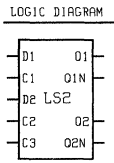
INPUT LOADING: 3K (1, 2, 1, 2)
5K (1, 2, 1, 2)
7K (1, 2, 1, 2)

Z(Q, QN) = LS1 (D1, C1, D2, C2)$

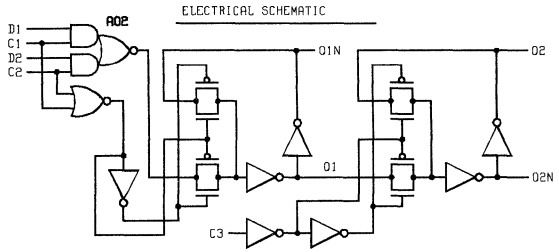
WORKSTATION WC. DELAY **LSI LOGIC CORP** 09/25/84
(RISE/FALL) DAISY ⌂ MENTOR = 11.8 / 9.5 VALID = 11

LS2 DLATCH INTO DLATCH WITH SCAN INPUTS (LSSD) LS2

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

Q1 OUTPUT		F0 = 1	F0 = 2	F0 = 3	F0 = 4	F0 = 8	GATES
3000 Series	TPLH	12.8ns	13.4	14.3	15.1	18.9	9
	TPHL	9.3	9.5	9.9	10.3	12.3	
5000 Series	TPLH	6.7	7.5	8.3	9.1	12.4	9
	TPHL	8.3	8.6	8.9	9.2	10.4	
7000 Series	TPLH	3.7	4.1	4.5	5.0	6.6	9
	TPHL	2.9	3.1	3.2	3.4	4.2	

INPUT LOADING: 3K (1, 2, 1, 2, 1)
5K (1, 2, 1, 2, 1)
7K (1, 2, 1, 2, 1)

Z(Q1, Q1N, Q2, Q2N) = LS2 (D1, C1, D2, C2, C3)$

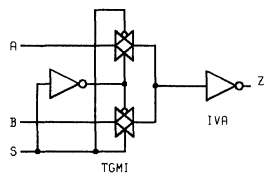
WORKSTATION WC. DELAY **LSI LOGIC CORP** 09/25/84
(RISE/FALL) DAISY ⌂ MENTOR = 14.0 / 10.6 VALID = 12

MUX21L

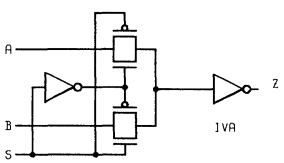
MUX21L

INVERTING GATE MULTIPLEXER

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

		F0 = 1	F0 = 2	F0 = 3	F0 = 4	F0 = 8	GATES
3000 Series	TPLH	4.8ns	5.2	5.7	6.2	8.3	3
	TPHL	4.7	5.1	5.5	6.0	8.0	
5000 Series	TPLH	2.9	3.2	3.5	3.8	4.9	3
	TPHL	2.8	3.0	3.1	3.3	3.9	
7000 Series	TPLH	2.0	2.1	2.3	2.4	2.9	3
	TPHL	1.6	1.7	1.8	1.9	2.3	

INPUT LOADING: 3K (2.9, 2.9, 2)
5K (4.9, 4.9, 2)
7K (4.7, 4.7, 2)

Z = MUX21L (A, B, S)$

LSI LOGIC CORP

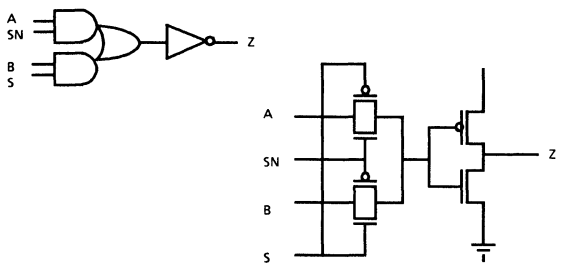
WORKSTATION WC. DELAY
(RISE/FALL) DAISY n MENTOR = 6.7 / 6.2 VALID = 7

09/25/84

MUX21LA

Two to One Transmission Gate Multiplexer, Inverting output

MUX21LA



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

		F0 = 1	F0 = 2	F0 = 3	F0 = 4	F0 = 8	GATES
3000 Series	TPLH	5.5ns	5.9	6.5	7.0	9.0	2
	TPHL	4.7	4.9	5.2	5.4	6.6	
5000 Series	TPLH	2.3	2.7	3.1	3.5	5.2	2
	TPHL	2.3	2.5	2.6	2.8	3.4	
7000 Series	TPLH	1.3	1.5	1.7	1.9	2.7	2
	TPHL	1.5	1.6	1.7	1.7	2.1	

INPUT LOADING: 3K (1, 2.9, 1, 2.9)
5K (1, 4.5, 1, 4.5)
7K (1, 4.3, 1, 4.3)

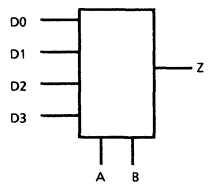
Z = MUX21LA (SN, A, S, B)$

FIXED DELAYS [WORKSTATION SOFTWARE DATABOOK]

WORST CASE COMMERCIAL DELAYS BASED UPON FO = 2 WITH STATISTICAL WIRE LENGHTS		VALID	DAISY	MENTOR
	TPLH	5	4.2	4.2
	TPHL		4.5	4.5

MUX41 — 4 Bit Non-inverting Mux — MUX41

(7k only) (7k only)



FUNCTION

B	A	Z
0	0	D0
0	1	D1
1	0	D2
1	1	D3

NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

		F0 = 1	F0 = 2	F0 = 3	F0 = 4	F0 = 8	GATES
7000 Series	TPLH	2.7ns	2.9	3.3	4.1	5.7	6
	TPHL	3.9	4.0	4.2	4.5	5.3	

INPUT LOADING: 7K (3.4, 3.4, 3.4, 3.4, 3, 2)

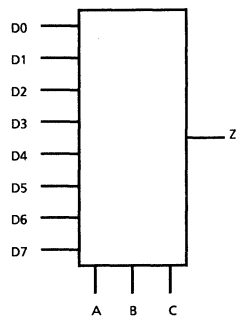
Z = MUX41 (D0, D1, D2, D3, A, B)$

FIXED DELAYS [WORKSTATION SOFTWARE DATABOOK]

WORST CASE COMMERCIAL DELAYS BASED UPON FO = 2 WITH STATISTICAL WIRE LENGHTS		VALID	DAISY	MENTOR
	TPLH	6	7.0	7.0
	TPHL		5.0	5.0

MUX81 — 8 Bit Non-inverting Mux — MUX81

(7k only) (7k only)



FUNCTION

C	B	A	Z
0	0	0	D0
0	0	1	D1
0	1	0	D2
0	1	1	D3
1	0	0	D4
1	0	1	D5
1	1	0	D6
1	1	1	D7

NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

		F0 = 1	F0 = 2	F0 = 3	F0 = 4	F0 = 8	GATES
7000 Series	TPLH	4.2ns	4.4	4.8	5.6	7.2	12
	TPHL	5.6	5.7	5.9	6.3	7.2	

INPUT LOADING: 7K (3.4, 3.4, 3.4, 3.4, 3.4, 3.4, 3.4, 3.4, 1, 3, 2)

Z = MUX81 (D0, D1, D2, D3, D4, D5, D6, D7, A, B, C)$

FIXED DELAYS [WORKSTATION SOFTWARE DATABOOK]

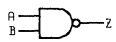
WORST CASE COMMERCIAL DELAYS BASED UPON FO = 2 WITH STATISTICAL WIRE LENGHTS		VALID	DAISY	MENTOR
	TPLH	9	9.7	9.7
	TPHL		7.5	7.5

ND2

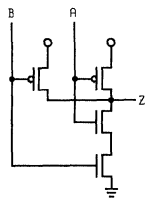
ND2

2NAND

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

		F0 = 1	F0 = 2	F0 = 3	F0 = 4	F0 = 8	GATES
3000 Series	TPLH	4.3ns	5.1	6.0	7.0	10.7	1
	TPHL	3.5	4.2	4.9	5.6	8.5	
5000 Series	TPLH	2.3	3.2	4.0	4.8	8.1	1
	TPHL	1.2	1.7	2.2	2.7	4.7	
7000 Series	TPLH	1.4	1.8	2.2	2.6	4.1	1
	TPHL	1.0	1.3	1.5	1.8	2.9	

INPUT LOADING: 3K (1, 1)
5K (1, 1)
7K (1, 1)

Z = ND2 (A, B)$

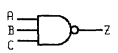
WORKSTATION WC. DELAY **LSI LOGIC CORP** 09/25/84
(RISE/FALL) DAISY ∩ MENTOR = 5.5 / 4.1 VALID = 4.2

ND3

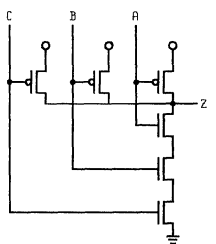
ND3

3NAND

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

		F0 = 1	F0 = 2	F0 = 3	F0 = 4	F0 = 8	GATES
3000 Series	TPLH	4.7ns	5.6	6.5	7.4	11.1	2
	TPHL	5.0	5.9	6.8	7.8	11.7	
5000 Series	TPLH	3.0	3.8	4.7	5.5	8.8	2
	TPHL	2.0	2.7	3.4	4.1	7.0	
7000 Series	TPLH	1.7	2.1	2.4	2.8	4.4	2
	TPHL	1.5	1.9	2.3	2.6	4.2	

INPUT LOADING: 3K (1, 1, 1)
5K (1, 1, 1)
7K (1, 1, 1)

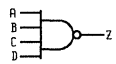
Z = ND3 (A, B, C)$

WORKSTATION WC. DELAY **LSI LOGIC CORP** 09/25/84
(RISE/FALL) DAISY ∩ MENTOR = 8.8 / 12.0 VALID = 11

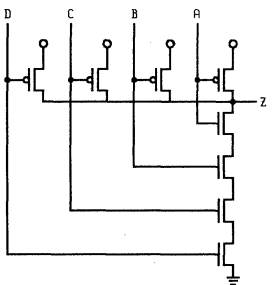
ND4 ND4

4NAND

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

		F0 = 1	F0 = 2	F0 = 3	F0 = 4	F0 = 8	GATES
3000 Series	TPLH	5.2ns	6.0	6.9	7.8	11.5	2
	TPHL	6.8	7.9	9.2	10.4	15.5	
5000 Series	TPLH	3.3	4.1	4.9	5.8	9.1	2
	TPHL	2.7	3.6	4.6	5.5	9.3	
7000 Series	TPLH	1.7	2.1	2.4	2.8	4.4	2
	TPHL	1.6	2.1	2.6	3.0	5.0	

INPUT LOADING: 3K (1, 1, 1, 1)
5K (1, 1, 1, 1)
7K (1, 1, 1, 1)

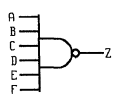
Z = ND4 (A, B, C, D)$

WORKSTATION WC. DELAY **LSI LOGIC CORP** 09/25/84
(RISE/FALL) DAISY ∩ MENTOR = 7.3 / 8.8 VALID = 8

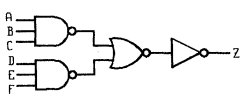
ND6 ND6

2 3NANDS INTO 2NOR INTO INVERTER (6NAND)

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

		F0 = 1	F0 = 2	F0 = 3	F0 = 4	F0 = 8	GATES
3000 Series	TPLH	5.8ns	6.2	6.7	7.2	9.3	5
	TPHL	7.4	7.5	7.8	8.1	9.3	
5000 Series	TPLH	4.4	4.9	5.3	5.7	7.4	5
	TPHL	5.5	5.7	5.9	6.1	6.7	
7000 Series	TPLH	2.8	3.0	3.2	3.4	4.3	5
	TPHL	3.3	3.4	3.5	3.6	4.0	

INPUT LOADING: 3K (1, 1, 1, 1, 1, 1)
5K (1, 1, 1, 1, 1, 1)
7K (1, 1, 1, 1, 1, 1)

Z = ND6 (A, B, C, D, E, F)$

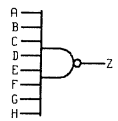
WORKSTATION WC. DELAY **LSI LOGIC CORP** 09/25/84
(RISE/FALL) DAISY ∩ MENTOR = 8.8 / 12.0 VALID = 11

ND8

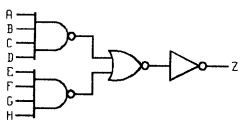
ND8

2 4NANDS INTO 2NOR INTO INVERTER (8NAND)

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

		F0 = 1	F0 = 2	F0 = 3	F0 = 4	F0 = 8	GATES
3000 Series	TPLH	6.2ns	6.6	7.1	7.6	9.6	6
	TPHL	8.5	8.7	9.0	9.3	10.4	
5000 Series	TPLH	4.7	5.2	5.6	6.0	7.7	6
	TPHL	6.4	6.5	6.7	6.9	7.7	
7000 Series	TPLH	3.0	3.2	3.4	3.6	4.5	6
	TPHL	3.7	3.8	3.9	4.0	4.5	

INPUT LOADING: 3K (1, 1, 1, 1, 1, 1, 1, 1)
5K (1, 1, 1, 1, 1, 1, 1, 1)
7K (1, 1, 1, 1, 1, 1, 1, 1)

Z = ND8 (A, B, C, D, E, F, G, H)$

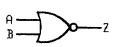
WORKSTATION WC. DELAY **LSI LOGIC CORP** 09/25/84
(RISE/FALL) DAISY ⌂ MENTOR = 9.2 / 12.8 VALID = 11

NR2

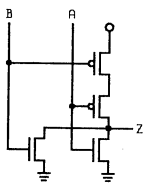
NR2

2NOR

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

		F0 = 1	F0 = 2	F0 = 3	F0 = 4	F0 = 8	GATES
3000 Series	TPLH	7.6ns	9.7	11.9	14.1	22.9	1
	TPHL	2.4	2.8	3.3	3.8	5.8	
5000 Series	TPLH	3.4	5.0	6.6	8.2	14.7	1
	TPHL	1.0	1.3	1.6	1.9	3.1	
7000 Series	TPLH	1.9	2.6	3.3	4.0	6.8	1
	TPHL	1.0	1.2	1.3	1.5	2.2	

INPUT LOADING: 3K (1, 1)
5K (1, 1)
7K (1, 1)

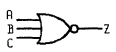
Z = NR2 (A, B)$

WORKSTATION WC. DELAY **LSI LOGIC CORP** 09/25/84
(RISE/FALL) DAISY ⌂ MENTOR = 9.4 / 3.1 VALID = 6

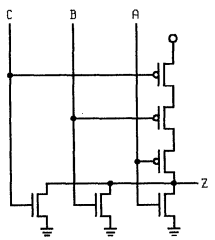
NR3 NR3

3NOR

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

		F0 = 1	F0 = 2	F0 = 3	F0 = 4	F0 = 8	GATES
3000 Series	TPLH	12.0ns	15.2	18.5	21.7	34.9	2
	TPHL	2.5	3.0	3.4	3.9	5.9	
5000 Series	TPLH	5.9	8.3	10.7	13.1	22.8	2
	TPHL	1.0	1.3	1.6	1.9	3.1	
7000 Series	TPLH	3.3	4.3	5.3	6.3	10.4	2
	TPHL	1.2	1.4	1.6	1.7	2.4	

INPUT LOADING: 3K (1, 1, 1)
5K (1, 1, 1)
7K (1, 1, 1)

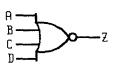
Z = NR3 (A, B, C)$

WORKSTATION WC. DELAY **LSI LOGIC CORP** 09/25/84
(RISE/FALL) DAISY ∩ MENTOR = 16.0 / 3.5 VALID = 10

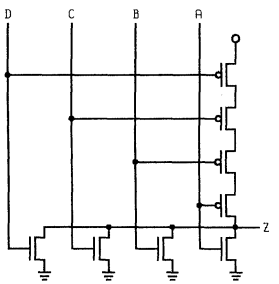
NR4 NR4

4NOR

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

		F0 = 1	F0 = 2	F0 = 3	F0 = 4	F0 = 8	GATES
3000 Series	TPLH	15.1ns	18.2	21.4	24.5	37.3	2
	TPHL	3.7	4.1	4.5	5.0	7.0	
5000 Series	TPLH	8.2	11.4	14.6	17.9	30.8	2
	TPHL	1.0	1.3	1.6	1.9	3.2	
7000 Series	TPLH	4.7	6.1	7.5	8.8	14.3	2
	TPHL	1.3	1.5	1.6	1.8	2.5	

INPUT LOADING: 3K (1, 1, 1, 1)
5K (1, 1, 1, 1)
7K (1, 1, 1, 1)

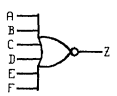
Z = NR4 (A, B, C, D)$

WORKSTATION WC. DELAY **LSI LOGIC CORP** 09/25/84
(RISE/FALL) DAISY ∩ MENTOR = 21.6/ 3.5 VALID = 13

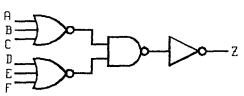
NR6 NR6

2 3NORS INTO 2NAND INTO INVERTER (6NOR)

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

		F0 = 1	F0 = 2	F0 = 3	F0 = 4	F0 = 8	GATES
3000 Series	TPLH	9.8ns	10.2	10.7	11.2	13.2	5
	TPHL	4.6	4.8	5.0	5.3	6.5	
5000 Series	TPLH	7.2	7.6	8.0	8.4	10.1	5
	TPHL	3.5	3.6	3.8	4.0	4.6	
7000 Series	TPLH	4.3	4.5	4.7	4.8	5.6	5
	TPHL	2.2	2.3	2.4	2.5	2.9	

INPUT LOADING: 3K (1, 1, 1, 1, 1, 1)
5K (1, 1, 1, 1, 1, 1)
7K (1, 1, 1, 1, 1, 1)

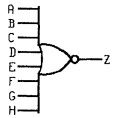
Z = NR6 (A, B, C, D, E, F)$

WORKSTATION WC. DELAY **LSI LOGIC CORP** 09/25/84
(RISE/FALL) DAISY Ω MENTOR = 13.2 / 7.8 VALID = 11

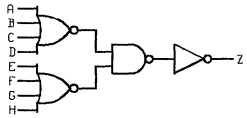
NR8 NR8

2 4NORS INTO 2NAND INTO INVERTER (8NOR)

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

		F0 = 1	F0 = 2	F0 = 3	F0 = 4	F0 = 8	GATES
3000 Series	TPLH	12.8ns	13.2	13.7	14.2	16.3	6
	TPHL	5.5	5.7	6.0	6.3	7.5	
5000 Series	TPLH	9.3	9.7	10.1	10.5	12.2	6
	TPHL	3.4	3.6	3.7	3.9	4.6	
7000 Series	TPLH	4.9	5.1	5.3	5.5	6.3	6
	TPHL	2.2	2.3	2.4	2.5	2.9	

INPUT LOADING: 3K (1, 1, 1, 1, 1, 1, 1, 1)
5K (1, 1, 1, 1, 1, 1, 1, 1)
7K (1, 1, 1, 1, 1, 1, 1, 1)

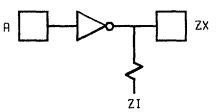
Z = NR8 (A, B, C, D, E, F, G, H)$

WORKSTATION WC. DELAY **LSI LOGIC CORP** 09/25/84
(RISE/FALL) DAISY Ω MENTOR = 16.7/ 7.8 VALID = 12

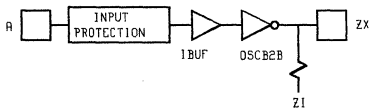
OSC2 OSC2

COMPLETE OSCILLATOR
FOR USE WITH EXTERNAL XTAL

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

		C = 15PF	C = 50PF	C = 85PF	C = 100PF	GATES
3000 Series	TPLH	10.3	12.6	15.0	16.0	1
	TPHL	14.2	18.4	22.5	24.3	
5000 Series	TPLH	5.2	6.9	8.5	9.2	0
	TPHL	5.4	7.1	8.8	9.5	
7000 Series	TPLH	4.8	5.5	6.2	6.5	0
	TPHL	6.0	7.6	9.2	9.9	

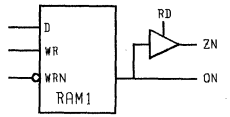
Z(ZX, ZI) = OSC2 (A)$

WORKSTATION WC. DELAY **LSI LOGIC CORP** 07/05/84
(RISE/FALL) DAISY ∩ MENTOR = 7.8 / 10.4 VALID = 13

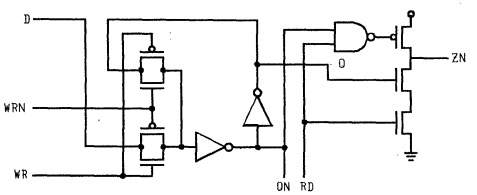
RAM1 RAM1

DLATCH, GATED
WITH ADDED TRISTATE OUTPUT

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

RD TO ZN OUTPUT		F0 = 1	F0 = 2	F0 = 3	F0 = 4	F0 = 8	GATES
3000 Series	TPLH	5.3ns	5.7	6.3	6.8	8.8	4
	TPHL	5.3	6.1	7.0	7.8	11.3	
5000 Series	TPLH	2.7	3.5	4.3	5.2	8.4	4
	TPHL	1.5	2.0	2.4	2.9	4.9	
7000 Series	TPLH	1.8	2.0	2.1	2.3	3.1	4
	TPHL	1.0	1.4	1.7	2.0	2.3	

INPUT LOADING: 3K (2.3, 1, 1, 1)
5K (3.8, 1, 1, 1)
7K (3.4, 1, 1, 1)

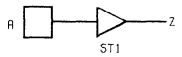
Z(ZN, QN) = RAM1 (D, WR, WRN, RD)$

WORKSTATION WC. DELAY **LSI LOGIC CORP** 09/25/84
(RISE/FALL) DAISY ∩ MENTOR = 5.6 / 4.5 VALID = 5

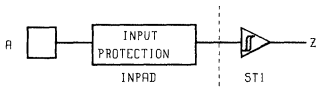
SCHMDT1 SCHMDT1

INPUT PAD WITH SCHMDT TRIGGER

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

		F0 = 1	F0 = 2	F0 = 3	F0 = 4	F0 = 8	GATES
3000 Series	TPLH	11.6ns	12.0	12.5	13.0	15.1	3
	TPHL	17.4	17.6	17.9	18.2	19.3	
5000 Series	TPLH	4.5	4.9	5.3	5.8	7.4	3
	TPHL	7.1	7.3	7.5	7.7	8.3	
7000 Series	TPLH	3.1	3.3	3.5	3.7	4.5	3
	TPHL	4.3	4.4	4.6	4.7	5.1	

Z = SCHMDT1 (A)$

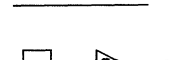
LSI LOGIC CORP

WORKSTATION WC. DELAY 09/25/84
(RISE/FALL) DAISY ∩ MENTOR = 8.5 / 14.1 VALID = 12

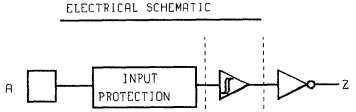
SCHMDT2 SCHMDT2

INPUT PAD WITH INVERTING SCHMDT TRIGGER

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

		F0 = 1	F0 = 2	F0 = 3	F0 = 4	F0 = 8	GATES
3000 Series	TPLH	20.6ns	21.0	21.5	22.0	24.1	4
	TPHL	14.0	14.2	14.5	14.8	15.9	
5000 Series	TPLH	8.6	9.0	9.4	9.8	11.5	4
	TPHL	5.5	5.7	5.8	6.0	6.6	
7000 Series	TPLH	5.4	5.6	5.8	6.0	6.8	4
	TPHL	3.8	3.9	4.0	4.1	4.5	

Z = SCHMDT2 (A)$

LSI LOGIC CORP

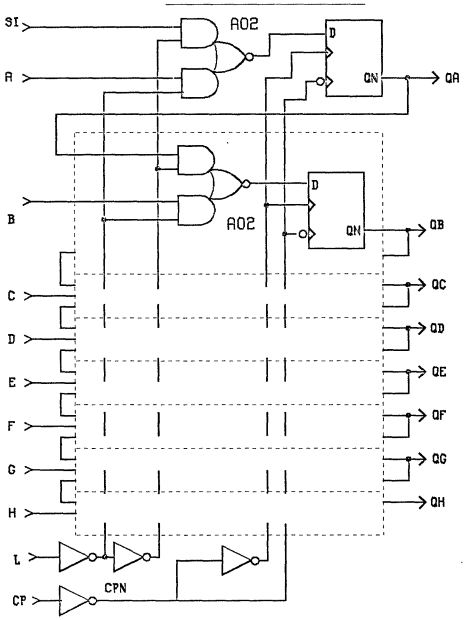
WORKSTATION WC. DELAY 09/25/84
(RISE/FALL) DAISY ∩ MENTOR = 17.2 / 10.4 VALID = 14

SR84
(5K ONLY)

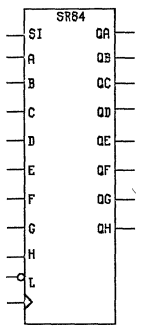
8 BIT SHIFT REGISTER WITH 2 BIT MULTIPLEXED INPUTS

SR84
(5K ONLY)

NETWORK SCHEMATIC



LOGIC DIAGRAM



SR84 EXAMPLE

Z(QA,QB,QC,QD,QE,QF,QG,QH)=SR84(SI,A,B,C,D,E,F,G,H,L,CP)$

LSI LOGIC CORP

GATES USED = 60

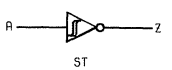
09/02/83

ST

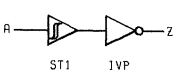
ST

INVERTING SCHMIDT TRIGGER FOR INTRACHIP WAVE SHAPING

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

		FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	GATES
3000 Series	TPLH	9.4ns	11.5	13.6	15.8	24.6	2
	TPHL	4.3	4.9	5.6	6.3	9.2	
5000 Series	TPLH	6.8	7.2	7.6	8.0	9.7	4
	TPHL	4.2	4.4	4.5	4.7	5.3	
7000 Series	TPLH	4.3	4.5	4.7	4.9	5.7	4
	TPHL	3.1	3.2	3.3	3.4	3.8	

INPUT LOADING: 3K (2)
5K (2)
7K (2)

Z = ST (A)$

WORKSTATION WC. DELAY (RISE/FALL) DAISY ⌂ MENTOR = 13.6 / 8.0 VALID = 11

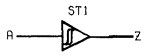
LSI LOGIC CORP

09/25/84

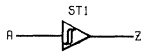
ST1 ST1

NON INVERTING SCHMDT TRIGGER IN FOR INTRACHIP WAVE SHAPING

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

		F0 = 1	F0 = 2	F0 = 3	F0 = 4	F0 = 8	GATES
3000 Series	TPLH	7.7ns	8.1	8.6	9.1	11.2	3
	TPHL	12.8	13.0	13.3	13.6	14.7	
5000 Series	TPLH	3.2	3.6	4.0	4.5	6.1	3
	TPHL	5.3	5.5	5.7	5.9	6.5	
7000 Series	TPLH	2.4	2.6	2.8	3.0	3.8	3
	TPHL	3.2	3.3	3.5	3.6	4.0	

INPUT LOADING: 3K (2)
5K (2)
7K (2)

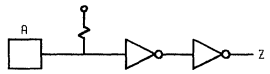
Z = ST1 (A)$

WORKSTATION WC. DELAY **LSI LOGIC CORP** 09/25/84
(RISE/FALL) DAISY ∩ MENTOR = 6.1 / 10.4 VALID = 8

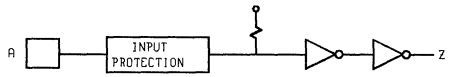
TLCHT TLCHT

INPUT PAD WITH BUFFER FOR TTL INPUT

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

		F0 = 1	F0 = 2	F0 = 3	F0 = 4	F0 = 8	GATES
3000 Series	TPLH	3.8ns	4.1	4.6	5.1	7.2	0
	TPHL	5.2	5.3	5.5	5.7	6.7	
5000 Series	TPLH	2.3	2.5	2.8	3.1	4.1	0
	TPHL	3.9	4.0	4.1	4.2	4.7	
7000 Series	TPLH	3.0	3.1	3.2	3.3	3.7	0
	TPHL	4.3	4.3	4.4	4.5	4.8	

INPUT LOADING: 3K (5)
5K (5)
7K (5)

ONE I/O CELL

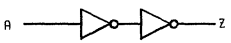
Z = TLCHT(A)$

WORKSTATION WC. DELAY **LSI LOGIC CORP** 09/25/84
(RISE/FALL) DAISY ∩ MENTOR = 3.5 / 7.0 VALID = 5

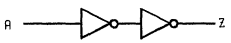
TLCHTI TLCHTI

BUFFER FOR BIDIRECT TTL INPUT

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

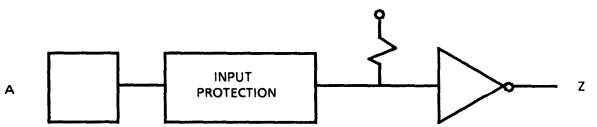
		FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	GATES
3000 Series	TPLH	3.4ns	3.8	4.3	4.8	6.9	2
	TPHL	6.3	6.7	7.1	7.6	9.6	
5000 Series	TPLH	1.6	2.0	2.4	2.9	4.6	3
	TPHL	2.7	3.0	3.3	3.6	4.7	
7000 Series	TPLH	1.3	1.5	1.7	1.9	2.7	3
	TPHL	1.6	1.8	2.0	2.2	2.9	

INPUT LOADING: 3K (3)
5K (3)
7K (3)

Z = TLCHTI(A)$

WORKSTATION WC. DELAY **LSI LOGIC CORP** 09/25/84
(RISE/FALL) DAISY ∩ MENTOR = 3.8 / 8.7 VALID = 6

TLCHN (7k only) **Inverting Input Pad With Buffer For TTL Input** **TLCHN** (7k only)



NOMINAL 25°C, 5V PERFORMANCE WITH STATISTICAL WIRE LENGTHS

		FO = 1	FO = 2	FO = 4	FO = 8	FO = 16	GATES
7000 Series	TPLH	3.0ns	3.2	4.5	5.5	6.1	0
	TPHL	2.4	2.5	2.9	3.3	3.5	

INPUT LOADING: 7K (5)

Z = TLCHN(A)$

FIXED DELAYS [WORKSTATION SOFTWARE DATABOOK]

WORST CASE COMMERCIAL DELAYS BASED UPON FO = 2 WITH STATISTICAL WIRE LENGHTS		VALID	DAISY	MENTOR
	TPLH	5	4.4	4.4
	TPHL		5.6	5.6

This page explains how to read the macrofunction model catalog and annotates the CB4C macrofunction model in Figure 18.1.

1. The macrofunction's name appears in the upper-left and upper-right corners.

2. The macrofunction's function is provided on the same line as the macrocell's name.

3. The macrofunction's network schematic, illustrating interconnected macrocells, is shown.

4. The macrofunction's logic diagram is also shown.

5. The coding syntax in TDL format is shown. This particular syntax is used by the LDS System logic simulator, not by the workstation simulator.

6. The number of gates used by the macrofunction is shown in the lower left corner.

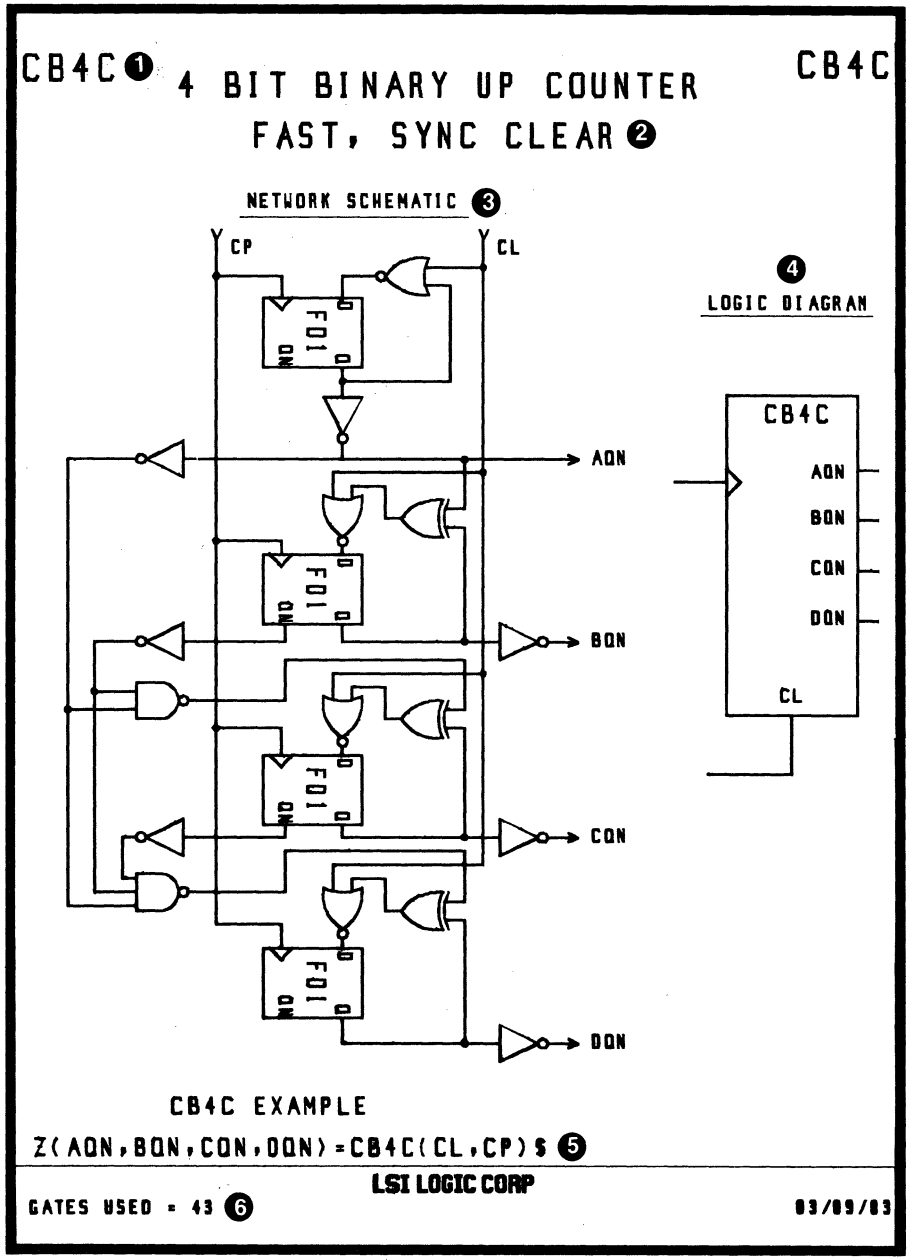


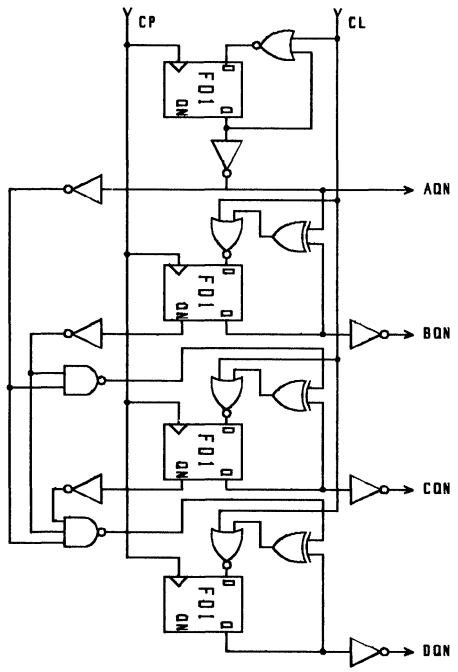
Figure 18.1
Model for CB4C Macrofunction

CB4C

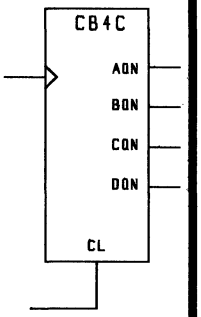
4 BIT BINARY UP COUNTER
FAST, SYNC CLEAR

CB4C

NETWORK SCHEMATIC



LOGIC DIAGRAM



CB4C EXAMPLE

Z(AQN,BQN,CQN,DQN)=CB4C(CL,CP)$

LSI LOGIC CORP

GATES USED = 43

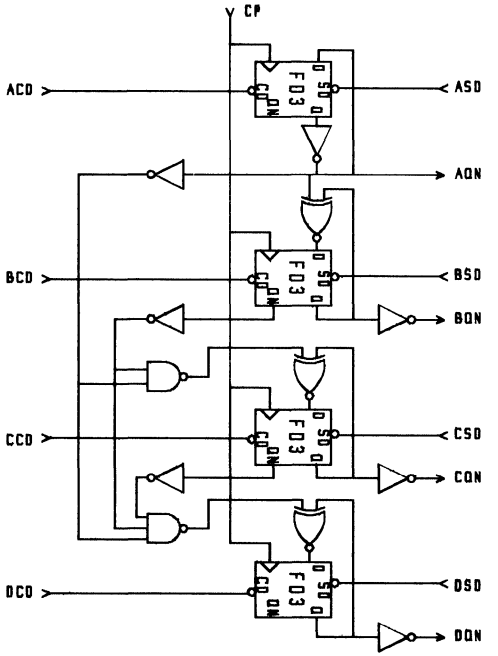
03/09/83

CB4F

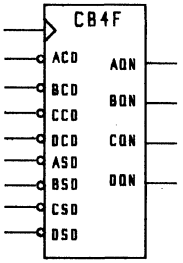
4 BIT BINARY UP COUNTER
FAST, INDIVIDUAL CD SD

CB4F

NETWORK SCHEMATIC



LOGIC DIAGRAM



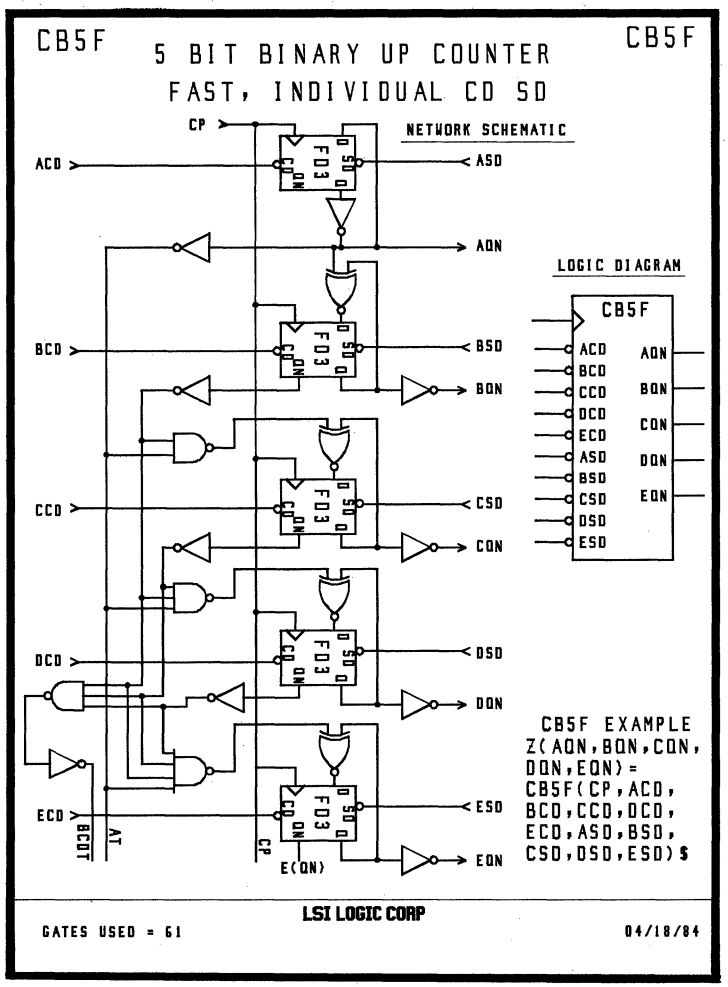
CB4F EXAMPLE

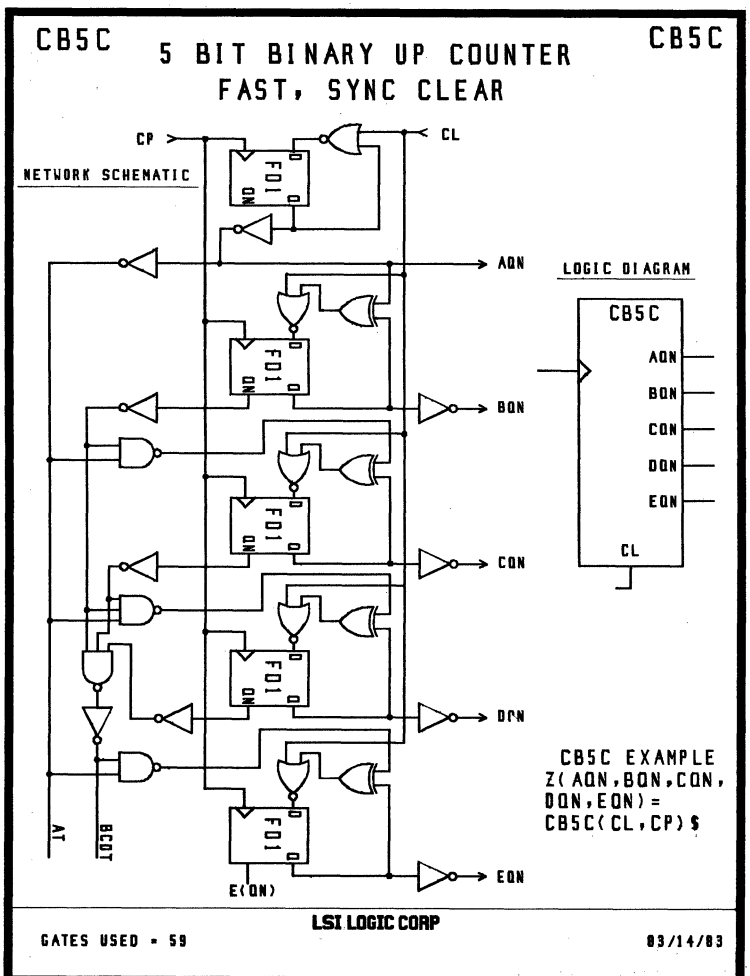
Z(AQN,BQN,CQN,DQN)=CB4F(CP,ACD,BCD,CCD,DCD,
ASD,BSD,CSD,DSD)$

LSI LOGIC CORP

GATES USED = 47

02/20/83


CB5F
5 BIT BINARY UP COUNTER
FAST, INDIVIDUAL CD SD
CB5F
NETWORK SCHEMATIC
CP
ACD
BCD
CCD
DCD
ECD
ASD
BSD
CSD
DSD
ESD
AQN
BQN
CQN
DQN
EQN
FD3
LOGIC DIAGRAM
CB5F
CB5F EXAMPLE
Z(AQN,BQN,CQN,
DQN,EQN)=
CB5F(CP,ACD,
BCD,CCD,DCD,
ECD,ASD,BSD,
CSD,DSD,ESD)$
BCDT
AT
E(QN)
LSI LOGIC CORP
GATES USED = 61
04/18/84

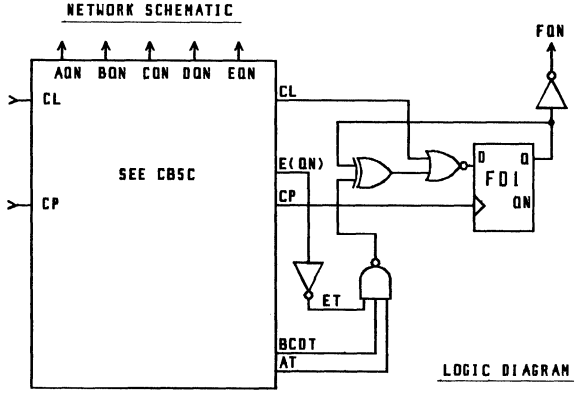

CB5C
5 BIT BINARY UP COUNTER
FAST, SYNC CLEAR
CB5C
NETWORK SCHEMATIC
CP
CL
AQN
BQN
CQN
DQN
EQN
FD1
LOGIC DIAGRAM
CB5C
CB5C EXAMPLE
Z(AQN,BQN,CQN,
DQN,EQN)=
CB5C(CL,CP)$
BCDT
AT
E(QN)
LSI LOGIC CORP
GATES USED = 59
03/14/83

CB6C

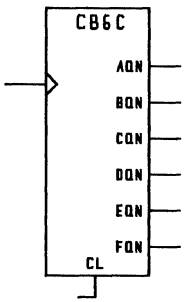
6 BIT BINARY UP COUNTER
FAST, SYNC CLEAR

CB6C

NETWORK SCHEMATIC



LOGIC DIAGRAM



CB6C EXAMPLE

Z(AQN,BQN,CQN,DQN,EQN,FQN)=CB6C(CL,CP)$

LSI LOGIC CORP

GATES USED = 70

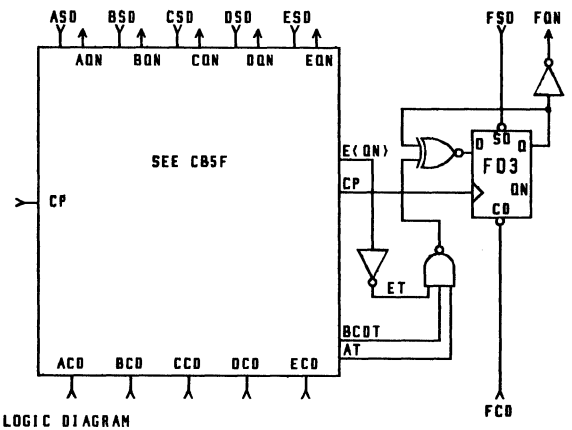
03/14/83

CB6F

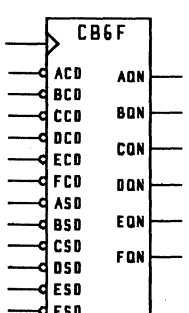
6 BIT BINARY UP COUNTER
FAST, INDIVIDUAL CD SD

CB6F

NETWORK SCHEMATIC



LOGIC DIAGRAM



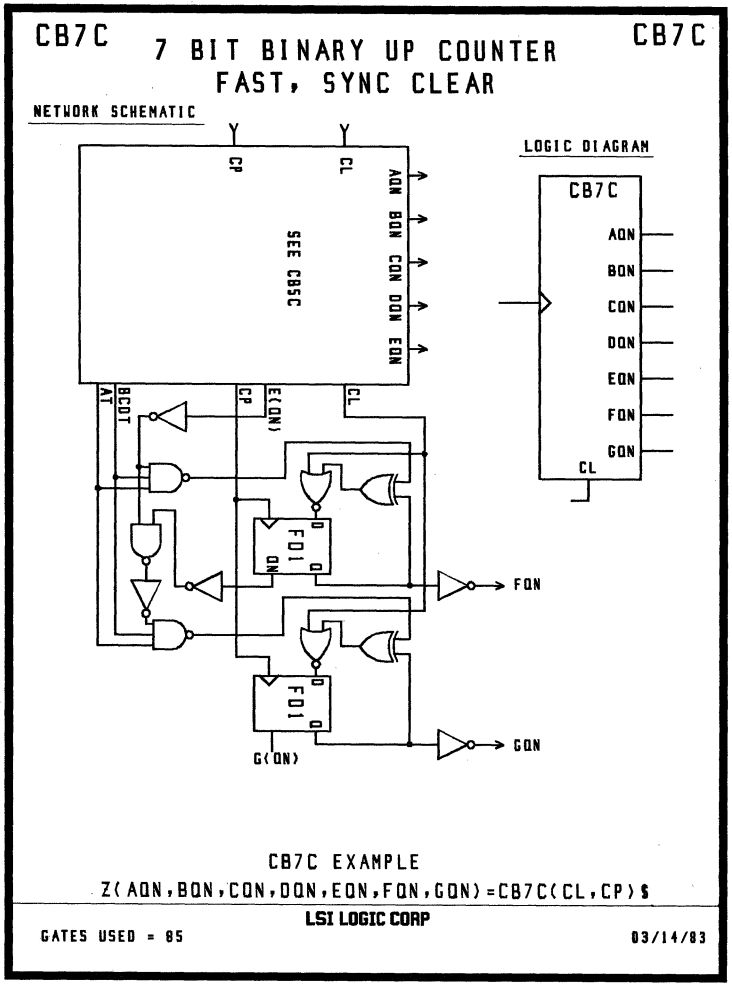
CB6F EXAMPLE

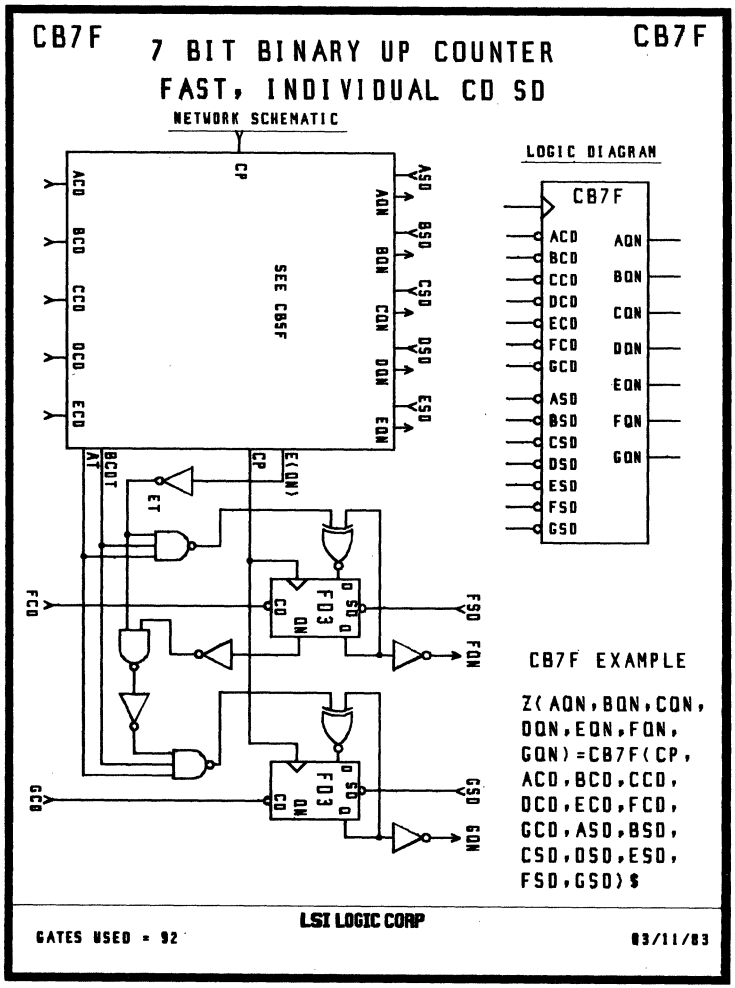
Z(AQN,BQN,CQN,DQN,EQN,FQN)=
CB6F(CP,ACD,BCD,CCD,DCD,ECD,
FCD,ASD,BSD,CSD,DSD,ESD,FSD)$

LSI LOGIC CORP

GATES USED = 76

03/11/83


CB7C
7 BIT BINARY UP COUNTER
FAST, SYNC CLEAR
CB7C
NETWORK SCHEMATIC
LOGIC DIAGRAM
SEE CB5C
CP
CL
AQN
BQN
CQN
DQN
EQN
FQN
GQN
BCOT
AT
E(QN)
FD1
G(QN)
CB7C EXAMPLE
Z(AQN,BQN,CQN,DQN,EQN,FQN,GQN)=CB7C(CL,CP)$
LSI LOGIC CORP
GATES USED = 85
03/14/83

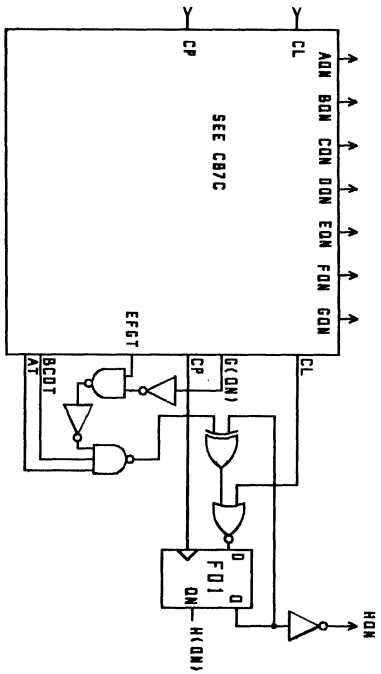

CB7F
7 BIT BINARY UP COUNTER
FAST, INDIVIDUAL CD SD
CB7F
NETWORK SCHEMATIC
LOGIC DIAGRAM
SEE CB5F
ACD
BCD
CCD
DCD
ECD
FCD
GCD
ASD
BSD
CSD
DSD
ESD
FSD
GSD
AQN
BQN
CQN
DQN
EQN
FQN
GQN
FD3
CB7F EXAMPLE
Z(AQN,BQN,CQN,
DQN,EQN,FQN,
GQN)=CB7F(CP,
ACD,BCD,CCD,
DCD,ECD,FCD,
GCD,ASD,BSD,
CSD,DSD,ESD,
FSD,GSD)$
LSI LOGIC CORP
GATES USED = 92
03/11/83

CB8C

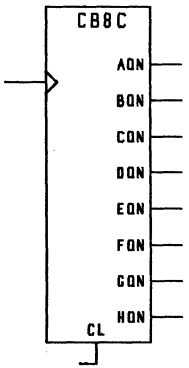
8 BIT BINARY UP COUNTER
FAST, SYNC CLEAR

CB8C

NETWORK SCHEMATIC



LOGIC DIAGRAM



CB8C EXAMPLE

```
Z(AQN,BQN,CQN,DQN,EQN,FQN,GQN,HQN)=CB8C(CL,CP)$
```

LSI LOGIC CORP

GATES USED = 98

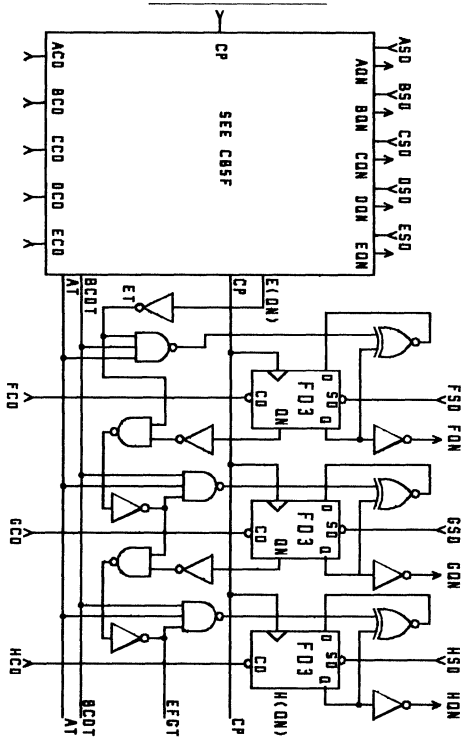
03/14/83

CB8F

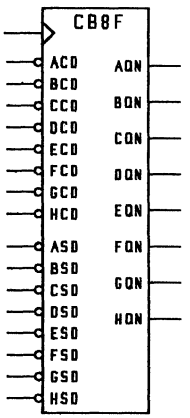
8 BIT BINARY UP COUNTER
FAST, INDIVIDUAL CD SD

CB8F

NETWORK SCHEMATIC



LOGIC DIAGRAM



CB8F EXAMPLE

```
Z(AQN,BQN,CQN,
DQN,EQN,FQN,GQN,
HQN)=CB8F(CP,
ACD,BCD,CCD,DCD,
ECD,FCD,GCD,HCD,
ASD,BSD,CSD,DSD,
ESD,FSD,GSD,HSD)$
```

LSI LOGIC CORP

GATES USED = 187

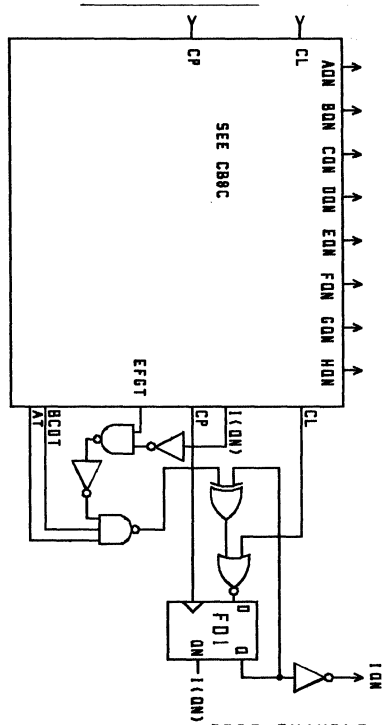
03/11/83

CB9C

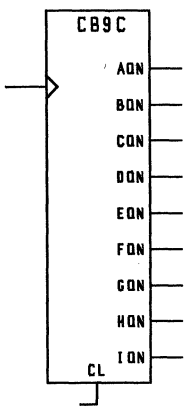
9 BIT BINARY UP COUNTER
FAST, SYNC CLEAR

CB9C

NETWORK SCHEMATIC



LOGIC DIAGRAM



CB9C EXAMPLE

Z(AQN,BQN,CQN,DQN,EQN,FQN,GQN,HQN,IQN)=CB9C(CL,CP)$

LSI LOGIC CORP

GATES USED = 114

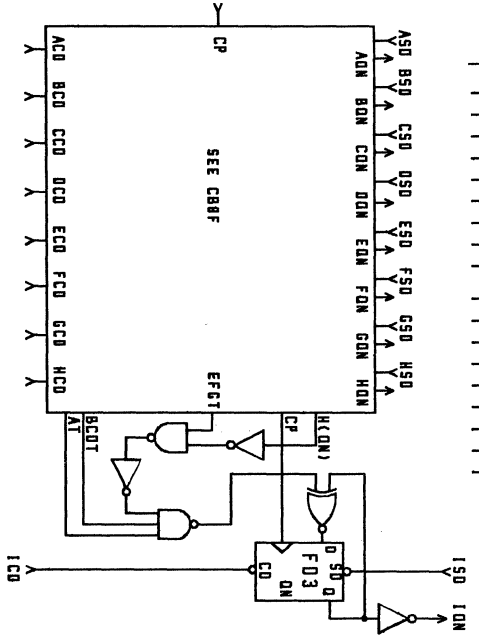
03/14/83

CB9F

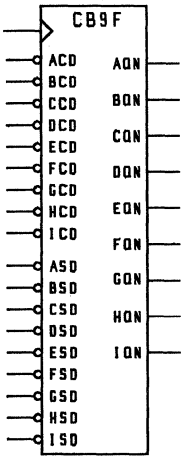
9 BIT BINARY UP COUNTER
FAST, INDIVIDUAL CD SD

CB9F

NETWORK SCHEMATIC



LOGIC DIAGRAM



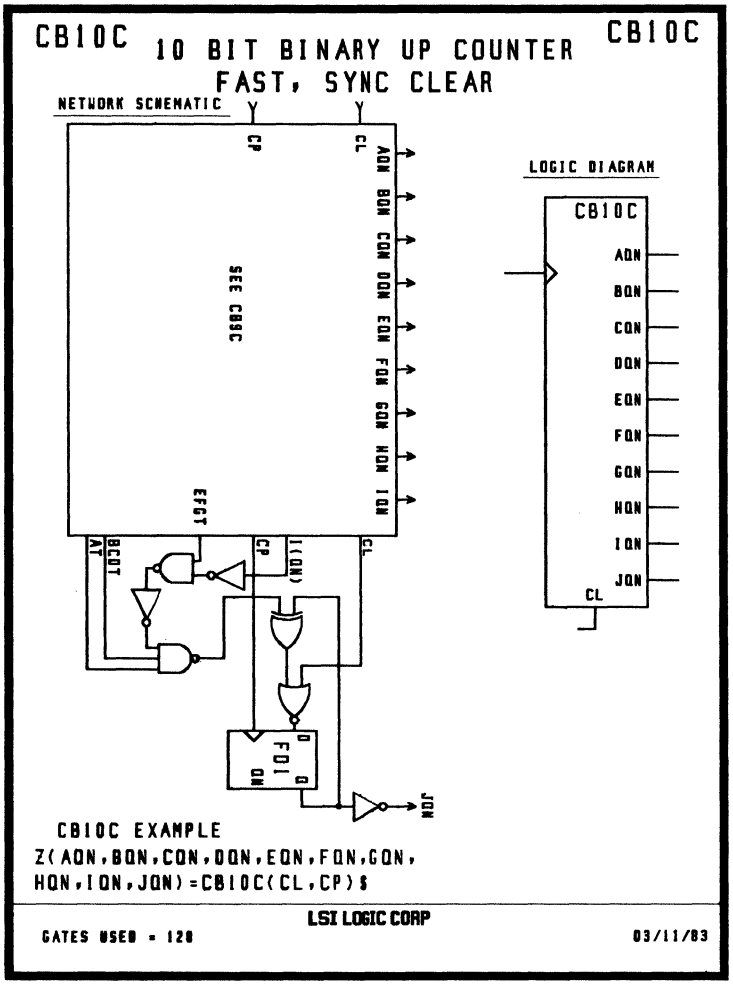
CB9F EXAMPLE

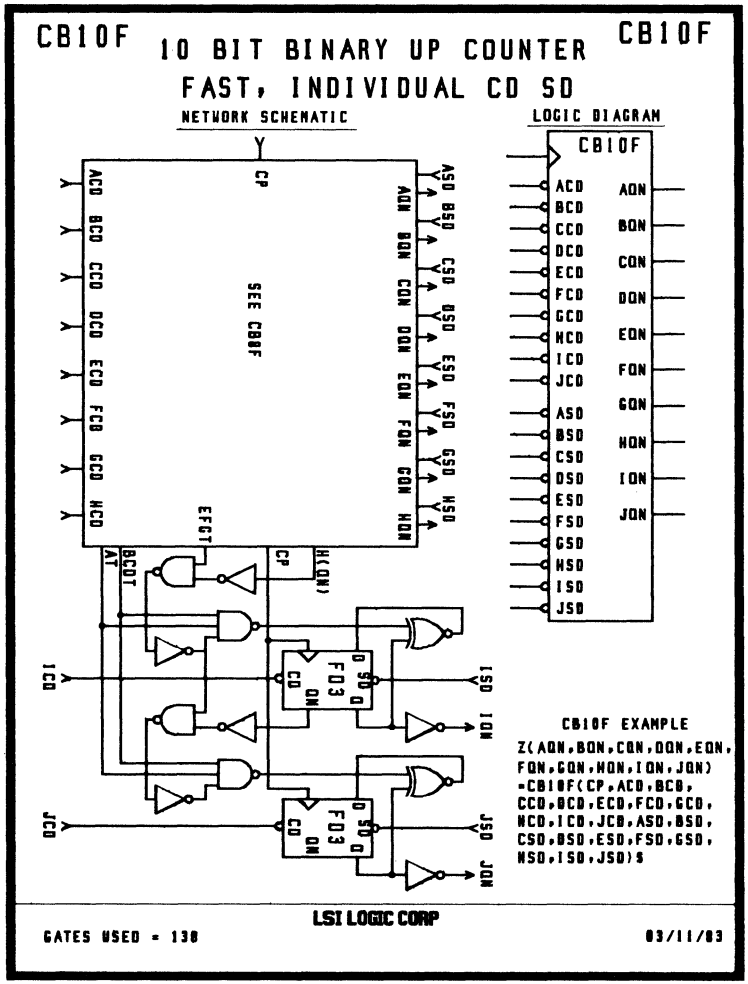
Z(AQN,BQN,CQN,DQN,EQN,FQN,GQN,HQN,IQN)=CB9F(CP,
ACD,BCD,CCD,DCD,ECD,FCD,GCD,HCD,ICD,
ASD,BSD,CSD,DSD,ESD,FSD,GSD,HSD,ISD)$

LSI LOGIC CORP

GATES USED = 123

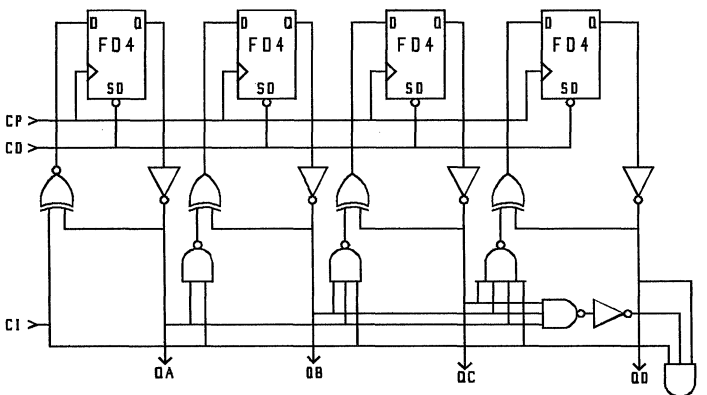
03/11/83


CB10C
10 BIT BINARY UP COUNTER
FAST, SYNC CLEAR
CB10C
NETWORK SCHEMATIC
LOGIC DIAGRAM
CB10C
AQN
BQN
CQN
DQN
EQN
FQN
GQN
HQN
IQN
JQN
CL
CB10C EXAMPLE
Z(AQN,BQN,CQN,DQN,EQN,FQN,GQN,
HQN,IQN,JQN)=CB10C(CL,CP)$
LSI LOGIC CORP
GATES USED = 120
03/11/83

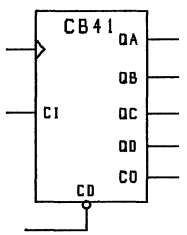

CB10F
10 BIT BINARY UP COUNTER
FAST, INDIVIDUAL CD SD
CB10F
NETWORK SCHEMATIC
LOGIC DIAGRAM
CB10F
ACD
BCD
CCD
DCD
ECD
FCD
GCD
HCD
ICD
JCD
ASD
BSD
CSD
DSD
ESD
FSD
GSD
HSD
ISD
JSD
AQN
BQN
CQN
DQN
EQN
FQN
GQN
HQN
IQN
JQN
CB10F EXAMPLE
Z(AQN,BQN,CQN,DQN,EQN,
FQN,GQN,HQN,IQN,JQN)
=CB10F(CP,ACD,BCD,
CCD,DCD,ECD,FCD,GCD,
HCD,ICD,JCD,ASD,BSD,
CSD,DSD,ESD,FSD,GSD,
HSD,ISD,JSD)$
LSI LOGIC CORP
GATES USED = 130
03/11/83

CB41 4 BIT BINARY UP COUNTER, CB41
EXPANDABLE ENABLE CLEAR DIRECT

NETWORK SCHEMATIC



LOGIC DIAGRAM



	OUTPUT			
	QA	QB	QC	QD
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
10	0	1	0	1
11	1	1	0	1
12	0	0	1	1
13	1	0	1	1
14	0	1	1	1
15	1	1	1	1

CB41 EXAMPLE
Z(QA,QB,QC,QD,CO)=CB41(CP,CI,CD)$

LSI LOGIC CORP

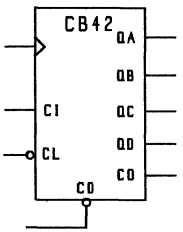
GATES USED = 42

02/01/83

CB42 4 BIT BINARY UP COUNTER, CB42
EXPANDABLE ENABLE SYNC CLEAR,CD

NETWORK SCHEMATIC

LOGIC DIAGRAM



CB42 EXAMPLE
Z(QA,QB,QC,QD,CO)=CB42(CP,CI,CL,CD)$
GATES USED = 46

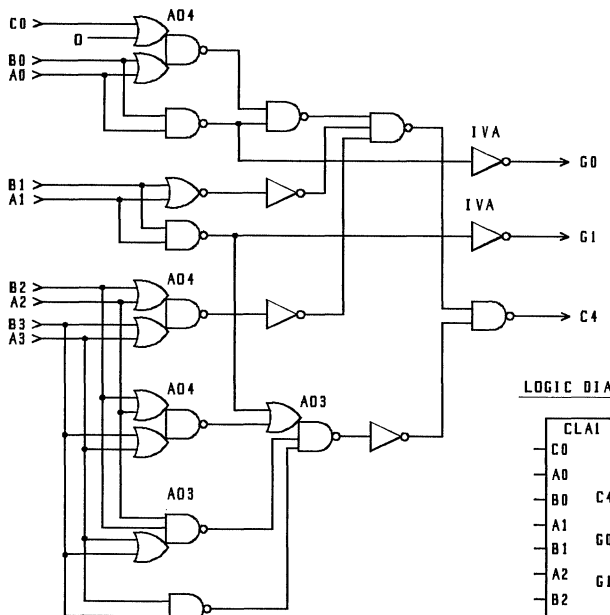
LSI LOGIC CORP

02/01/83

CLA1 CLA1

CARRY LOOK AHEAD FOR 4 BIT ADDER (LEAST SIGNIFICANT NIBBLE)

NETWORK SCHEMATIC



LOGIC DIAGRAM

CLA1 EXAMPLE

Z(C4,G0,G1)=CLA1(C0,A0,B0,A1,B1,A2,B2,A3,B3)$

LSI LOGIC CORP

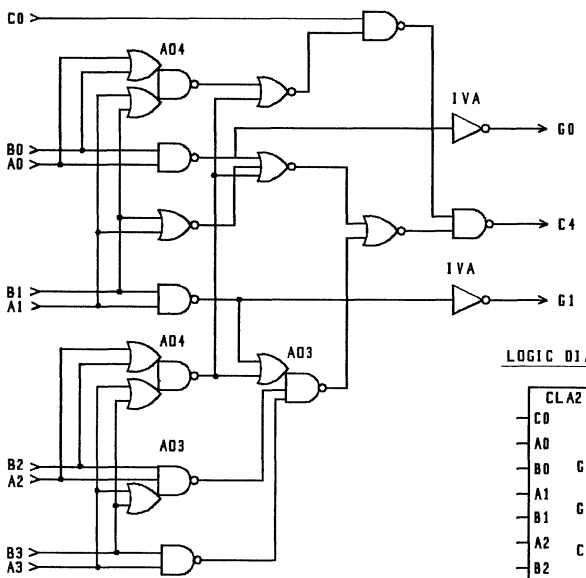
GATES USED = 22

05/20/83

CLA2 CLA2

CARRY LOOK AHEAD FOR 4 BIT ADDER

NETWORK SCHEMATIC



LOGIC DIAGRAM

CLA2 EXAMPLE

Z(G0,G1,C4)=CLA2(C0,A0,B0,A1,B1,A2,B2,A3,B3)$

LSI LOGIC CORP

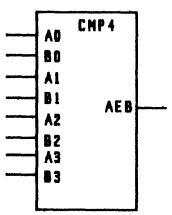
GATES USED = 19

06/21/83

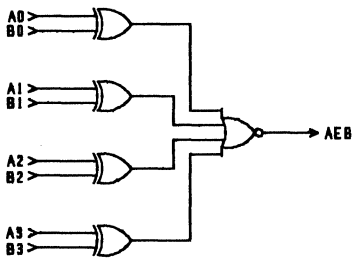
CMP4 CMP4

4 BIT EQUALITY COMPARATOR

LOGIC DIAGRAM



NETWORK SCHEMATIC



TRUTH TABLE

0=0	1=1	2=2	3=3	AEB
1	1	1	1	1
(	ANY	0	)	0

CMP4 EXAMPLE

```
Z(AEB)=CMP4(A0,B0,A1,B1,A2,B2,A3,B3)$
```

LSI LOGIC CORP

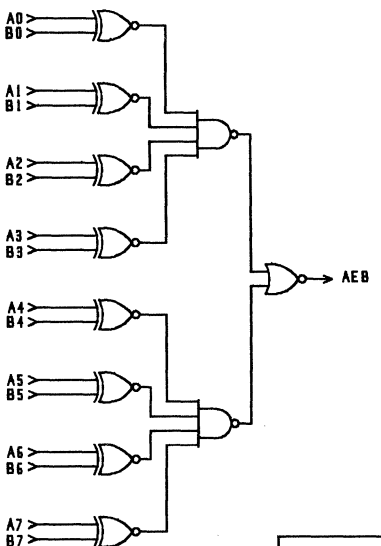
GATES USED = 14

03/11/83

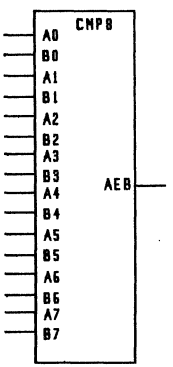
CMP8 CMP8

8 BIT EQUALITY COMPARATOR

NETWORK SCHEMATIC



LOGIC DIAGRAM



TRUTH TABLE

0=0	1=1	2=2	3=3	4=4	5=5	6=6	7=7	AEB
1	1	1	1	1	1	1	1	1
(			ANY		0		)	0

CMP8 EXAMPLE

```
Z(AEB)=CMP8(A0,B0,A1,B1,A2,B2,A3,B3,A4,B4,A5,B5,
A6,B6,A7,B7)$
```

LSI LOGIC CORP

GATES USED = 29

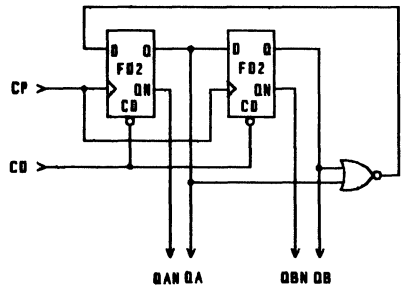
03/11/83

CM3B

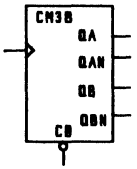
CM3B

MODULO 3 BINARY COUNTER
CLEAR DIRECT

NETWORK SCHEMATIC



LOGIC DIAGRAM



OUTPUT	
QA	QB
0	0
1	0
0	1

CM3B EXAMPLE

Z(QA,QAN,QB,QBN) = CM3B(CP,CD)$

GATES USED = 13

LSI LOGIC CORP

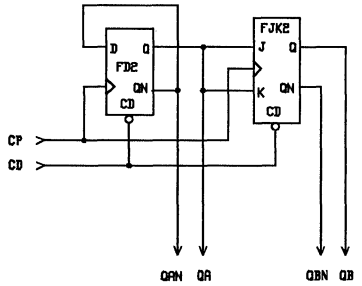
03/10/83

CM4B

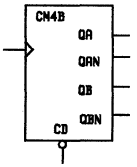
CM4B

MODULO 4 BINARY COUNTER
CLEAR DIRECT

NETWORK SCHEMATIC



LOGIC DIAGRAM



OUTPUT	
QA	QB
0	0
1	0
0	1
1	1

CM4B EXAMPLE

Z(QA,QAN,QB,QBN) = CM4B(CP,CD)$

GATES USED = 16

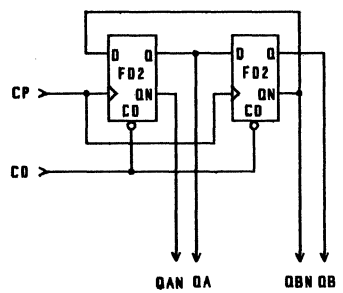
LSI LOGIC CORP

02/25/83

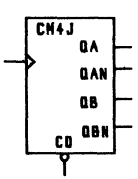
CM4J

MODULO 4 JOHNSON COUNTER
CLEAR DIRECT

NETWORK SCHEMATIC



LOGIC DIAGRAM



OUTPUT	
QA	QB
0	0
1	0
1	1
0	1

CM4J EXAMPLE

Z(QA,QAN,QB,QBN) = CM4J(CP,CD)$

GATES USED = 12

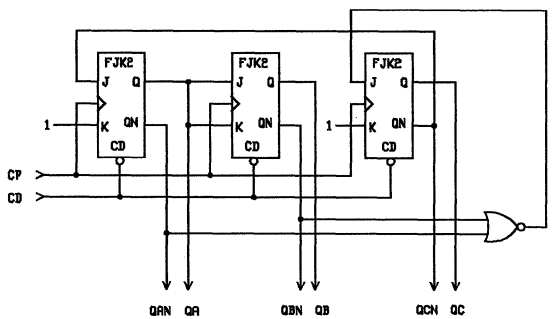
LSI LOGIC CORP

03/11/83

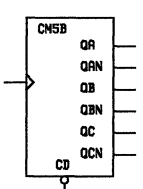
CM5B

MODULO 5 BINARY COUNTER
CLEAR DIRECT

NETWORK SCHEMATIC



LOGIC DIAGRAM



OUTPUT		
QA	QB	QC
0	0	0
1	0	0
0	1	0
1	1	0
0	0	1

CM5B EXAMPLE

Z(QA,QAN,QB,QBN,QC,QCN) = CM5B(CP,CD)$

GATES USED = 30

LSI LOGIC CORP

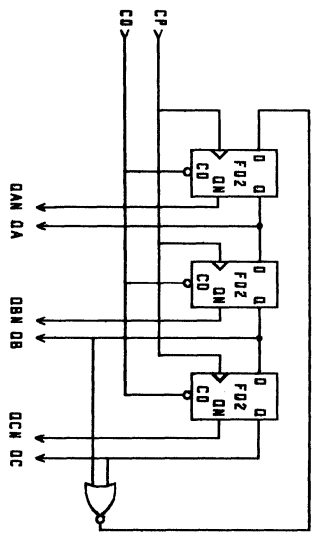
02/25/83

CM5SR

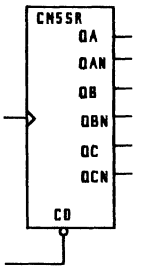
MODULO 5 SHIFT COUNTER, CLEAR DIRECT

CM5SR

NETWOTK SCHEMATIC



LOGIC DIAGRAM



OUTPUT

QA	QB	QC
0	0	0
1	0	0
1	1	0
0	1	1
0	0	1

```
CM5SR EXAMPLE
Z(QA,QAN,QB,QBN,QC,QCN)
=CM5SR(CP,CD)$
```

LSI LOGIC CORP

GATES USED=19

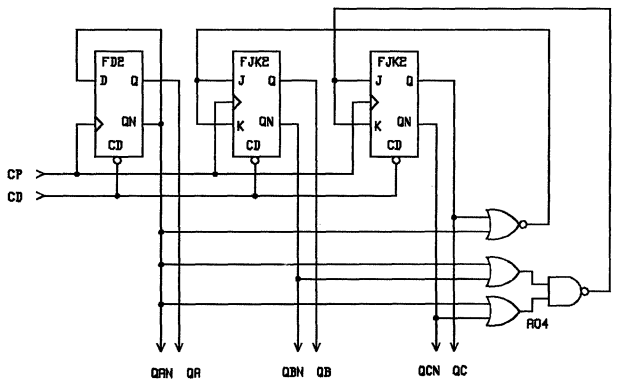
03/08/83

CM6B

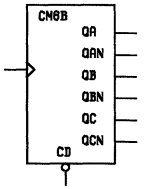
MODULO 6 BINARY COUNTER CLEAR DIRECT

CM6B

NETWORK SCHEMATIC



LOGIC DIAGRAM



OUTPUT		
QA	QB	QC
0	0	0
1	0	0
0	1	0
1	1	0
0	0	1
1	0	1

```
CM6B EXAMPLE
Z(QA,QAN,QB,QBN,QC,QCN) = CM6B(CP,CD)$
```

GATES USED = 31

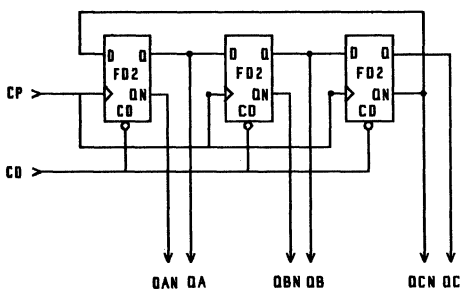
LSI LOGIC CORP

02/25/83

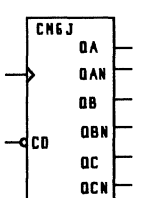
CM6J

MODULO 6 JOHNSON COUNTER
CLEAR DIRECT

NETWORK SCHEMATIC



LOGIC DIAGRAM



OUTPUT		
QA	QB	QC
0	0	0
1	0	0
1	1	0
1	1	1
0	1	1
0	0	1

CM6J EXAMPLE

Z(QA,QAN,QB,QBN,QC,QCN)=CM6J(CP,CD)$

LSI LOGIC CORP

GATES USED = 18

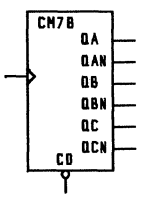
03/11/83

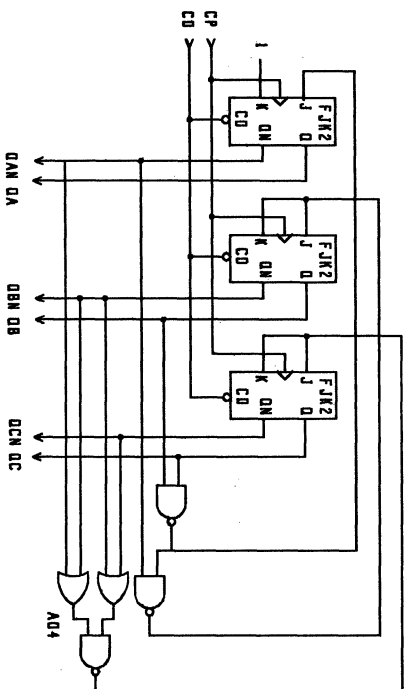
CM7B

MODULO 7 BINARY COUNTER
CLEAR DIRECT

NETWORK SCHEMATIC

LOGIC DIAGRAM





CM7B EXAMPLE

Z(QA,QAN,QB,QBN,QC,QCN) = CM7B(CP,CD)$

LSI LOGIC CORP

02/25/83

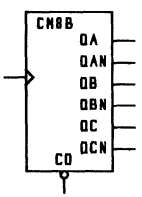
GATES USED = 31

CM8B

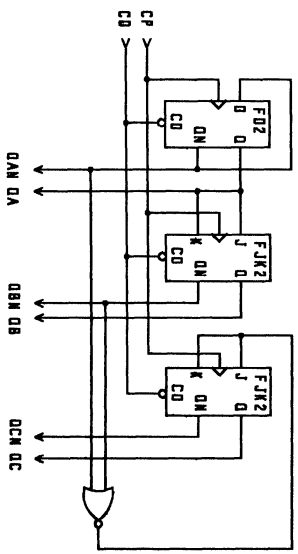
MODULO 8 BINARY COUNTER CLEAR DIRECT

CM8B

LOGIC DIAGRAM



NETWORK SCHEMATIC



CM8B EXAMPLE

Z(QA,QAN,QB,QBN,QC,QCN) = CM8B(CP,CD)$

GATES USED = 25

LSI LOGIC CORP

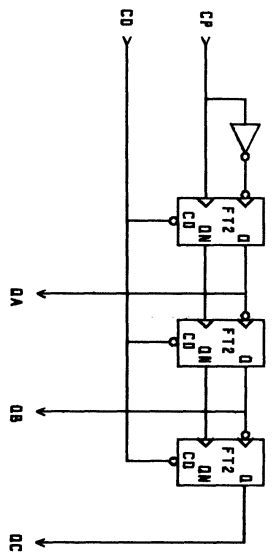
02/25/83

CM8BR

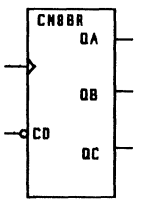
CM8BR

MODULO 8 BINARY RIPPLE COUNTER, CLEAR DIRECT

NETWORK SCHEMATIC



LOGIC DIAGRAM



	OUTPUT		
	QA	QB	QC
0	0	0	0
1	1	0	0
2	0	1	0
3	1	1	0
4	0	0	1
5	1	0	1
6	1	0	1
7	1	1	1

CM8BR EXAMPLE

Z(QA,QB,QC)=CM8BR(CP,CD)$

GATES USED = 16

LSI LOGIC CORP

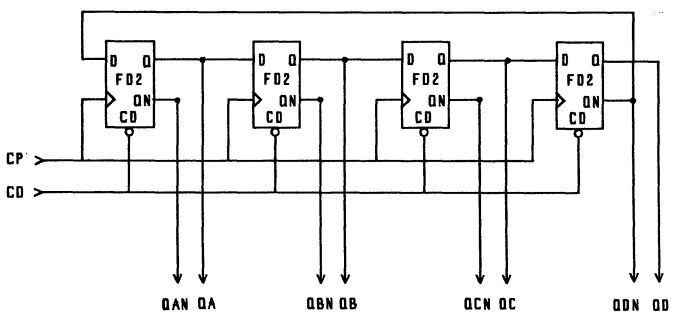
03/08/83

CM8J

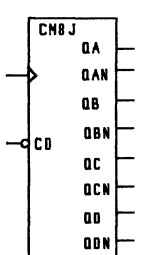
MODULO 8 JOHNSON COUNTER CLEAR DIRECT

CM8J

NETWORK SCHEMATIC



LOGIC DIAGRAM



OUTPUT			
QA	QB	QC	QD
0	0	0	0
1	0	0	0
1	1	0	0
1	1	1	0
1	1	1	1
0	1	1	1
0	0	1	1
0	0	0	1

CM8J EXAMPLE
Z(QA,QAN,QB,QBN,QC,QCN,QD,QDN)=CM8J(CP,CD)$

LSI LOGIC CORP

GATES USED = 24

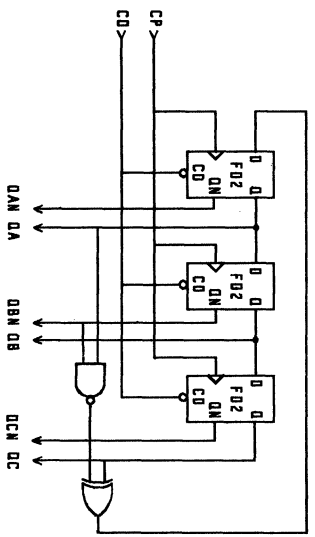
02/21/83

CM8SR

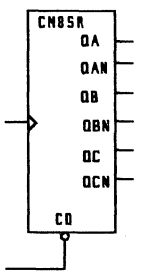
MODULO 8 SHIFT COUNTER, CLEAR DIRECT

CM8SR

NETWOTK SCHEMATIC



LOGIC DIAGRAM



OUTPUT

QA	QB	QC
0	0	0
1	0	0
0	1	0
1	0	1
1	1	0
1	1	1
0	1	1
0	0	1

CM8SR EXAMPLE
Z(QA,QAN,QB,QBN,QC,QCN)
=CM8SR(CP,CD)$

LSI LOGIC CORP

GATES USED=22

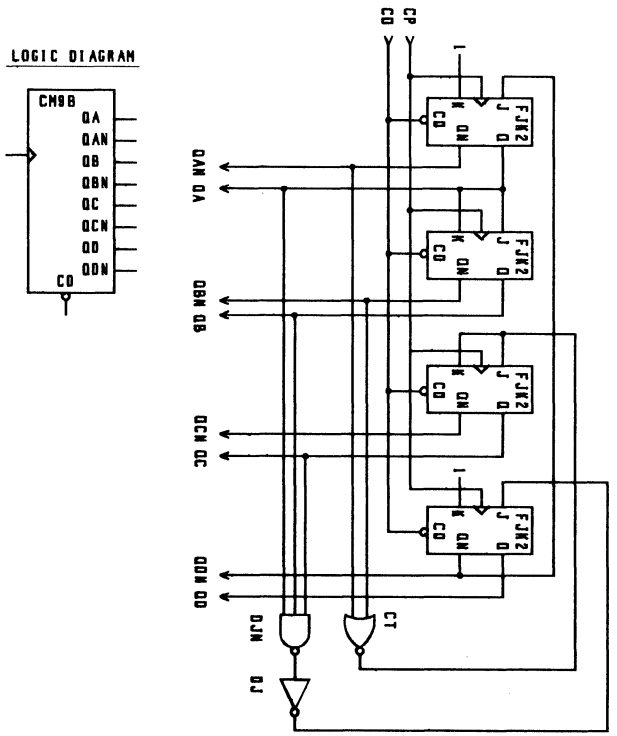
03/08/83

CM9B

CM9B

MODULO 9 BINARY COUNTER CLEAR DIRECT

NETWORK SCHEMATIC



LOGIC DIAGRAM

LSI LOGIC CORP

CM9B EXAMPLE GATES USED = 40 02/25/83

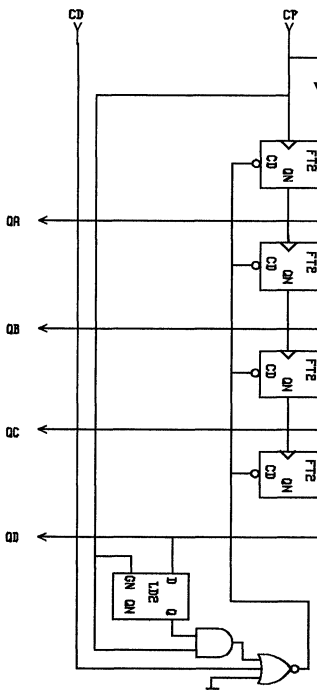
Z(QA,QAN,QB,QBN,QC,QCN,QD,QDN) = CM9B(CP,CD)$

CM9BR

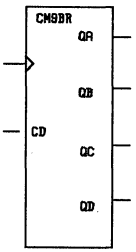
CM9BR

MODULO 9 BINARY RIPPLE COUNTER, CLEAR DIRECT

NETWORK SCHEMATIC



LOGIC DIAGRAM



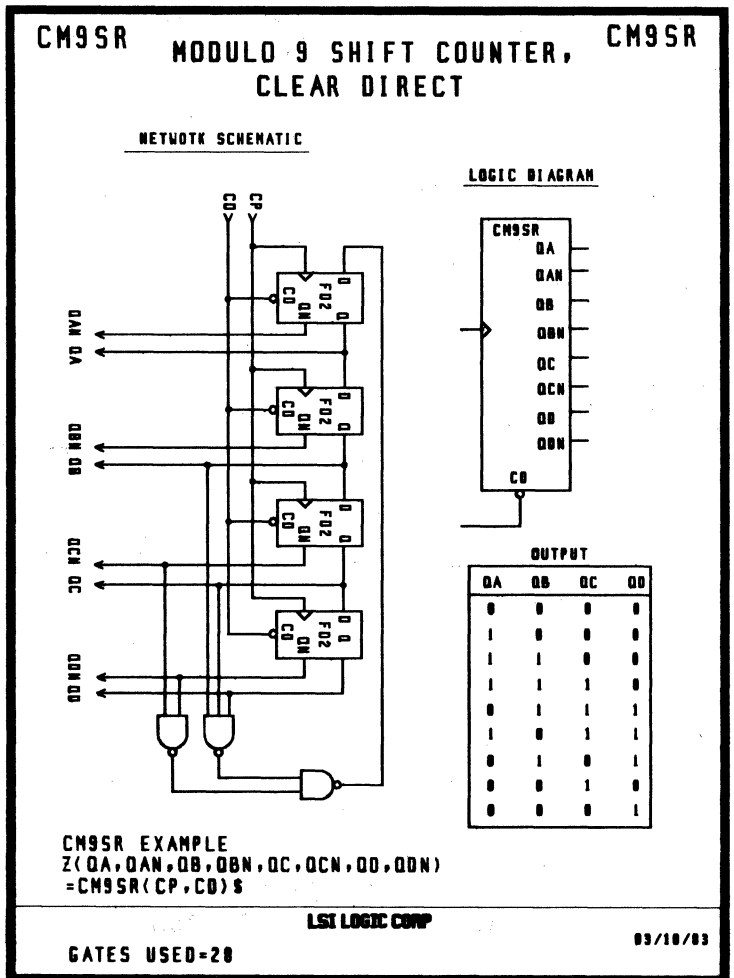
	OUTPUT			
	QA	QB	QC	QD
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1

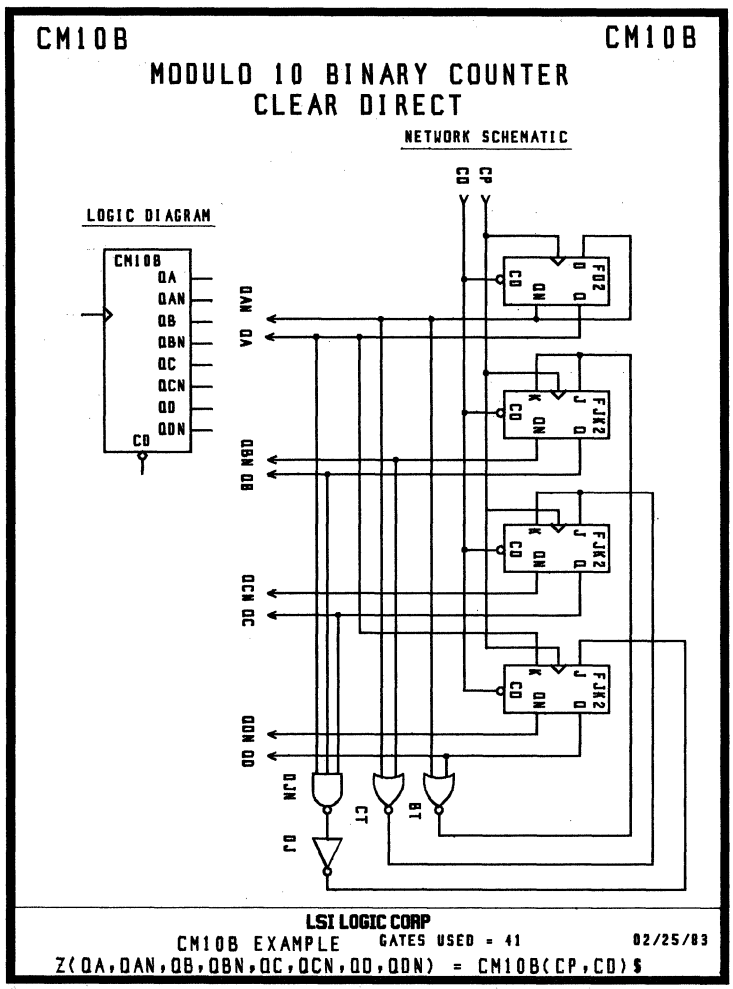
CM9BR EXAMPLE

Z(QA,QB,QC,QD)=CM9BR(CP,CD)$

LSI LOGIC CORP

GATES USED = 26 03/08/83

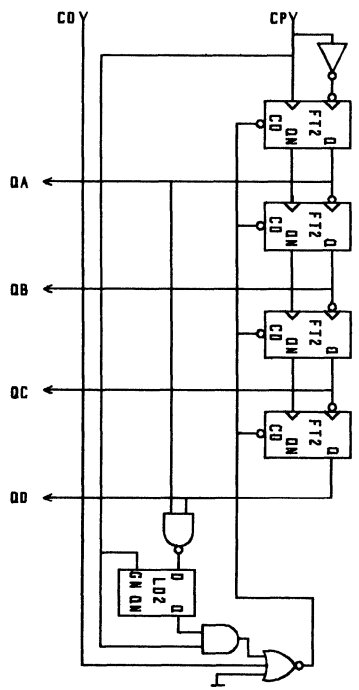

CM9SR
MODULO 9 SHIFT COUNTER,
CLEAR DIRECT
CM9SR
NETWOTK SCHEMATIC
LOGIC DIAGRAM
CM9SR
QA
QAN
QB
QBN
QC
QCN
QD
QDN
CD
OUTPUT
QA QB QC QD
CM9SR EXAMPLE
Z(QA,QAN,QB,QBN,QC,QCN,QD,QDN)
=CM9SR(CP,CD)$
LSI LOGIC CORP
GATES USED=28
03/10/83


CM10B
MODULO 10 BINARY COUNTER
CLEAR DIRECT
CM10B
NETWORK SCHEMATIC
LOGIC DIAGRAM
CM10B
QA
QAN
QB
QBN
QC
QCN
QD
QDN
CD
LSI LOGIC CORP
CM10B EXAMPLE
GATES USED = 41
02/25/83
Z(QA,QAN,QB,QBN,QC,QCN,QD,QDN) = CM10B(CP,CD)$

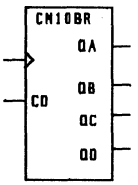
CM10BR

MODULO 10 BINARY RIPPLE COUNTER, CLEAR DIRECT

NETWORK SCHEMATIC



LOGIC DIAGRAM



	OUTPUT			
	QA	QB	QC	QD
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1

CM10BR EXAMPLE

Z(QA,QB,QC,QD)=CM10BR(CP,CD)$

LSI LOGIC CORP

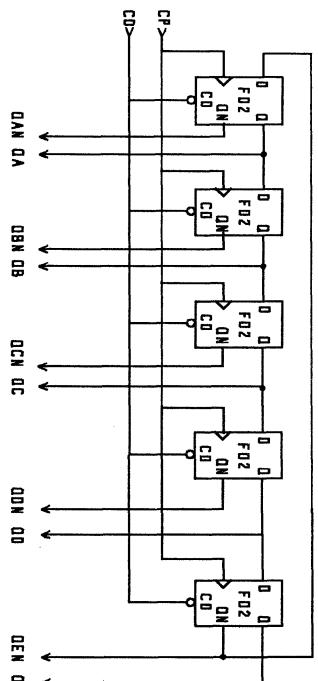
GATES USED = 27

03/08/83

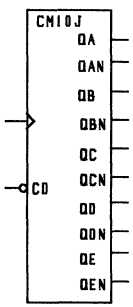
CM10J

MODULO 10 JOHNSON COUNTER CLEAR DIRECT

NETWORK SCHEMATIC



LOGIC DIAGRAM



OUTPUT					
QA	QB	QC	QD	QE	
0	0	0	0	0	
1	0	0	0	0	
1	1	0	0	0	
1	1	1	0	0	
1	1	1	1	0	
1	1	1	1	1	
0	1	1	1	1	
0	0	1	1	1	
0	0	0	1	1	
0	0	0	0	1	

CM10J EXAMPLE

Z(QA,QAN,QB,QBN,QC,QCN,QD,QDN,QE,QEN)=CM10J(CP,CD)$

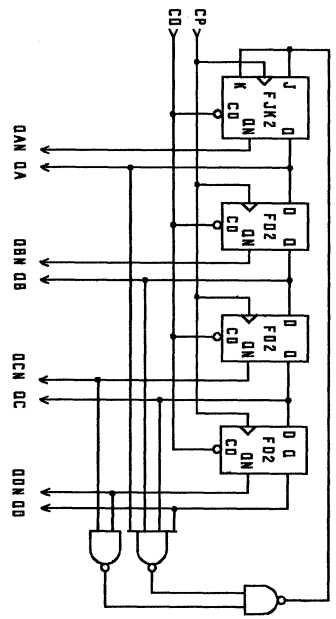
LSI LOGIC CORP

GATES USED = 30

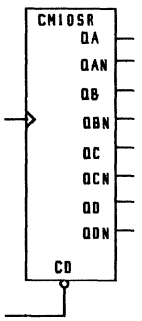
02/21/83

CM10SR MODULO 10 SHIFT COUNTER, CLEAR DIRECT CM10SR

NETWOTK SCHEMATIC



LOGIC DIAGRAM



OUTPUT

QA	QB	QC	QD
0	0	0	0
1	0	0	0
0	1	0	0
1	0	1	0
1	1	0	1
1	1	1	0
1	1	1	1
0	1	1	1
0	0	1	1
0	0	0	1

CM10SR EXAMPLE
Z(QA,QAN,QB,QBN,QC,QCN,QD,QDN)
=CM10SR(CP,CD)$

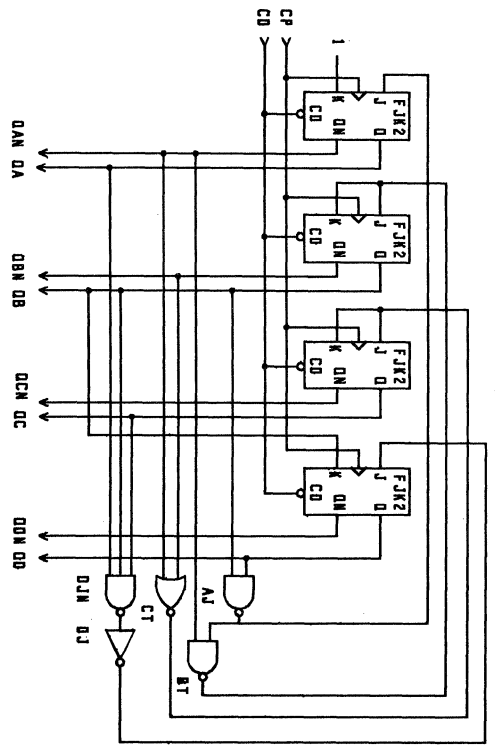
GATES USED = 31

LSI LOGIC CORP

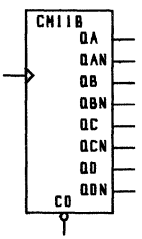
03/11/83

CM11B MODULO 11 BINARY COUNTER CLEAR DIRECT CM11B

NETWORK SCHEMATIC



LOGIC DIAGRAM



LSI LOGIC CORP

CM11B EXAMPLE GATES USED = 41

Z(QA,QAN,QB,QBN,QC,QCN,QD,QDN) = CM11B(CP,CD)$

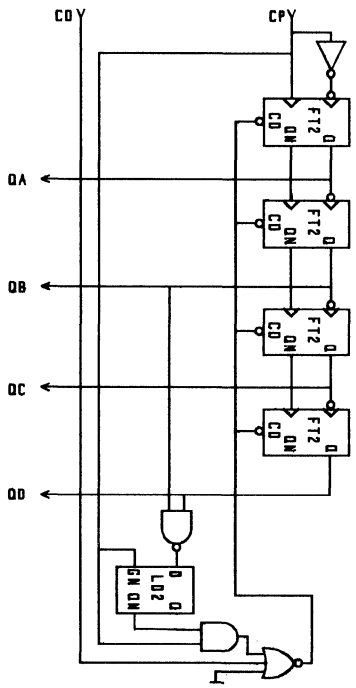
02/25/83

CM11BR

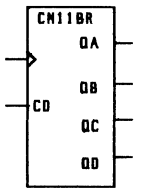
MODULO 11 BINARY RIPPLE COUNTER, CLEAR DIRECT

CM11BR

NETWORK SCHEMATIC



LOGIC DIAGRAM



	OUTPUT			
	QA	QB	QC	QD
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
10	0	1	0	1

CM11BR EXAMPLE

Z(QA,QB,QC,QD)=CM11BR(CP,CD)$

LSI LOGIC CORP

GATES USED = 27

03/08/83

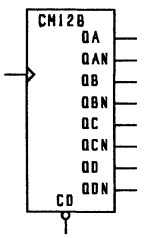
CM12B

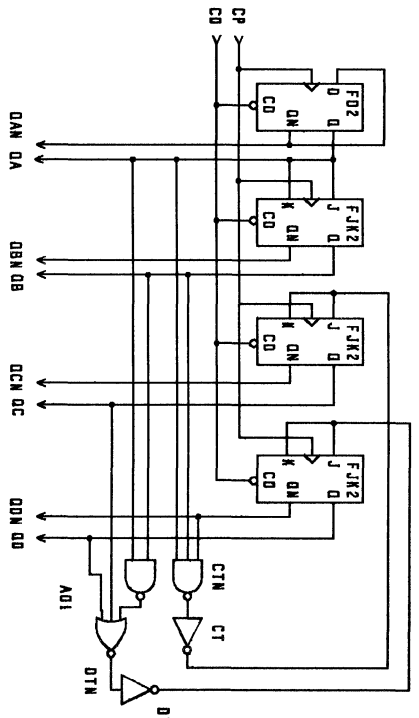
MODULO 12 BINARY COUNTER CLEAR DIRECT

CM12B

NETWORK SCHEMATIC

LOGIC DIAGRAM





LSI LOGIC CORP

CM12B EXAMPLE GATES USED = 42

Z(QA,QAN,QB,QBN,QC,QCN,QD,QDN) = CM12B(CP,CD)$

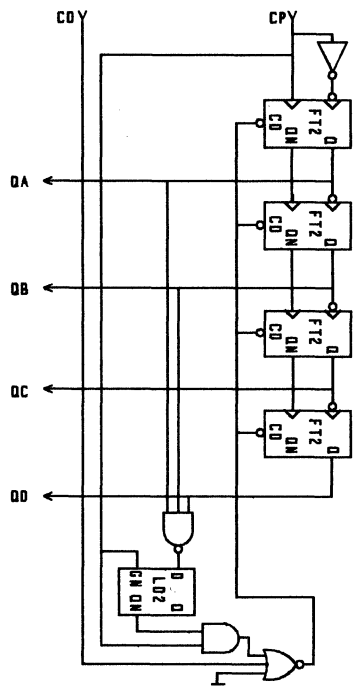
02/25/83

CM12BR

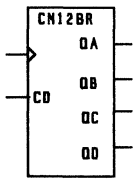
CM12BR

MODULO 12 BINARY RIPPLE COUNTER, CLEAR DIRECT

NETWORK SCHEMATIC



LOGIC DIAGRAM



	OUTPUT			
	QA	QB	QC	QD
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
10	0	1	0	1
11	1	1	0	1

CM12BR EXAMPLE
Z(QA,QB,QC,QD)=CM12BR(CP,CD)$

LSI LOGIC CORP

GATES USED = 27

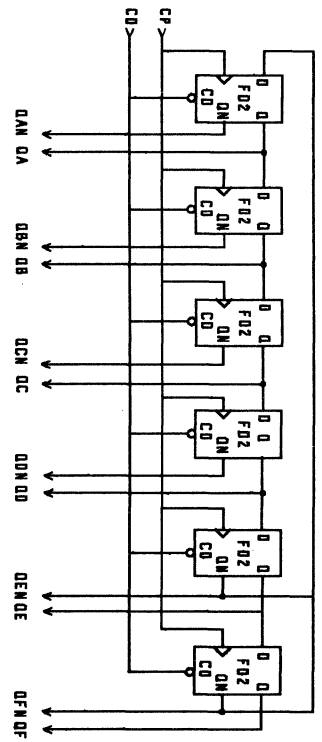
03/08/83

CM12J

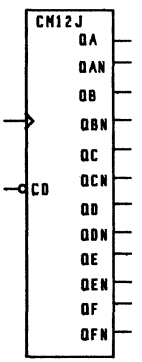
CM12J

MODULO 12 JOHNSON COUNTER CLEAR DIRECT

NETWORK SCHEMATIC



LOGIC DIAGRAM



CM12J EXAMPLE
Z(QA,QAN,QB,QBN,QC,QCN,QD,QDN,QE,QEN,QF,QFN)
=CM12J(CP,CD)$

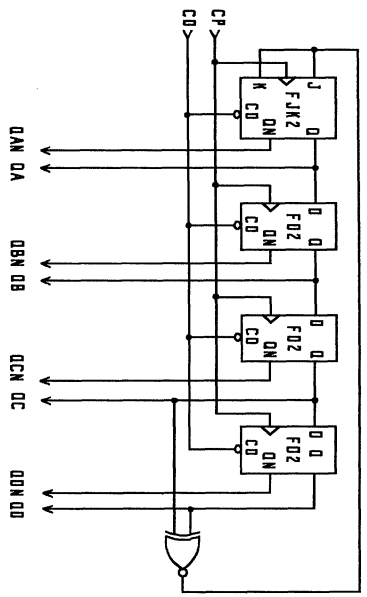
LSI LOGIC CORP

GATES USED=36

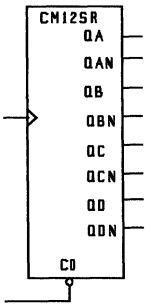
02/21/83

CM12SR MODULO 12 SHIFT COUNTER, CLEAR DIRECT CM12SR

NETWOTK SCHEMATIC



LOGIC DIAGRAN



OUTPUT

QA	QB	QC	QD
0	0	0	0
1	0	0	0
0	1	0	0
1	0	1	0
1	1	0	1
1	1	1	0
1	1	1	1
0	1	1	1
1	0	1	1
0	1	0	1
0	0	1	0
0	0	0	1

CM12SR EXAMPLE
Z(QA,QAN,QB,QBN,QC,QCN,QD,QDN)
=CM12SR(CP,CD)$

GATES USED = 29

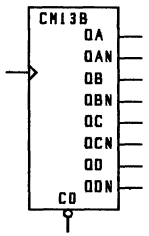
LSI LOGIC CORP

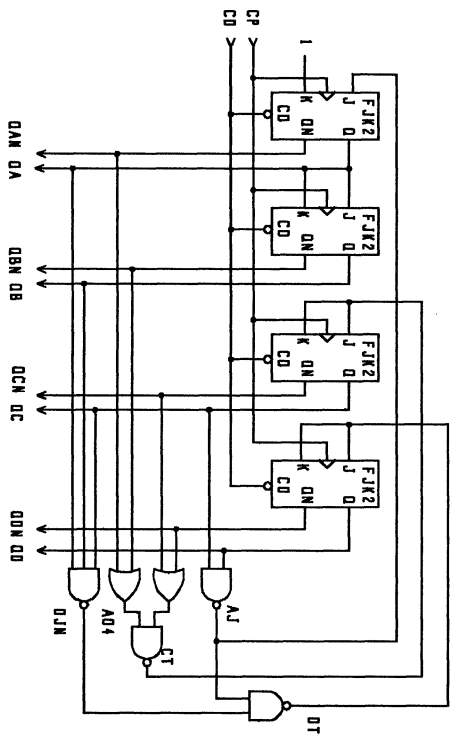
05/11/83

CM13B MODULO 13 BINARY COUNTER CLEAR DIRECT CM13B

NETWORK SCHEMATIC

LOGIC DIAGRAN





LSI LOGIC CORP

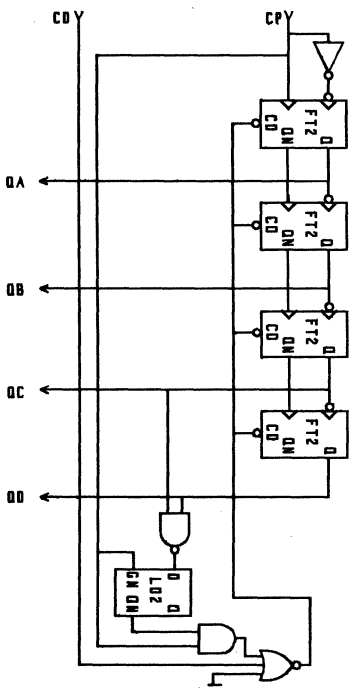
CM13B EXAMPLE GATES USED = 41 03/14/83

Z(QA,QAN,QB,QBN,QC,QCN,QD,QDN) = CM13B(CP,CD)$

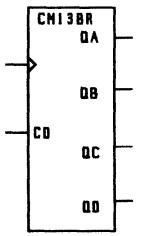
CM13BR CM13BR

MODULO 13 BINARY RIPPLE COUNTER, CLEAR DIRECT

NETWORK SCHEMATIC



LOGIC DIAGRAN



	OUTPUT			
	QA	QB	QC	QD
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
10	0	1	0	1
11	1	1	0	1
12	0	0	1	1

CM13BR EXAMPLE
Z(QA,QB,QC,QD)=CM13BR(CP,CD)$

LSI LOGIC CORP

GATES USED = 27

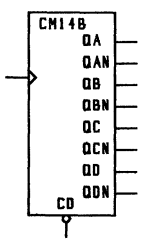
03/08/83

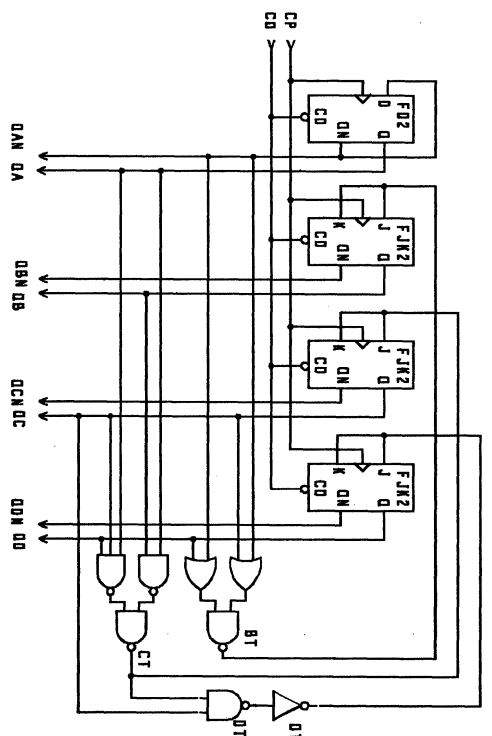
CM14B CM14B

MODULO 14 BINARY COUNTER CLEAR DIRECT

NETWORK SCHEMATIC

LOGIC DIAGRAN





LSI LOGIC CORP

CM14B EXAMPLE GATES USED = 42 06/21/83

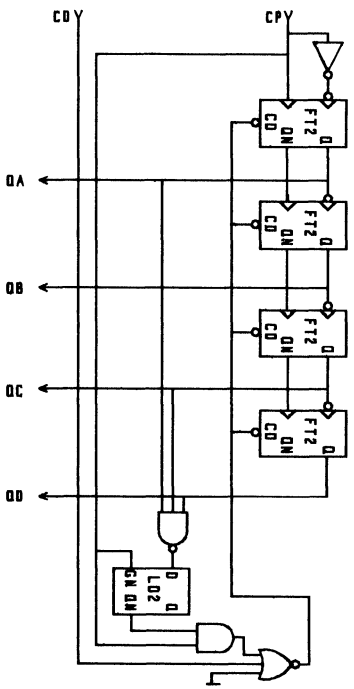
Z(QA,QAN,QB,QBN,QC,QCN,QD,QDN) = CM14B(CP,CD)$

CM14BR

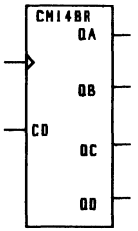
MODULO 14 BINARY RIPPLE COUNTER, CLEAR DIRECT

CM14BR

NETWORK SCHEMATIC



LOGIC DIAGRAM



	OUTPUT			
	QA	QB	QC	QD
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
10	0	1	0	1
11	1	1	0	1
12	0	0	1	1
13	1	0	1	1

CM14BR EXAMPLE
Z(QA,QB,QC,QD)=CM14BR(CP,CD)$

LSI LOGIC CORP

GATES USED = 27

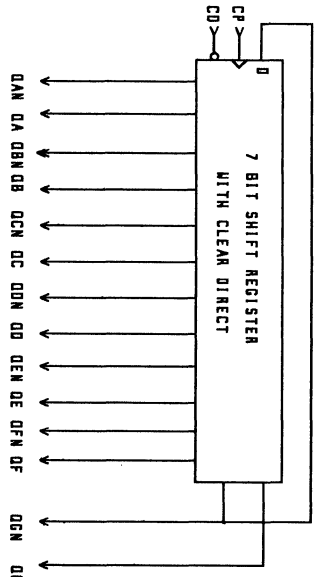
03/08/83

CM14J

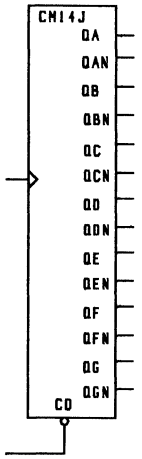
MODULD 14 JOHNSON COUNTER, CLEAR DIRECT

CM14J

NETWOTK SCHEMATIC



LOGIC DIAGRAM

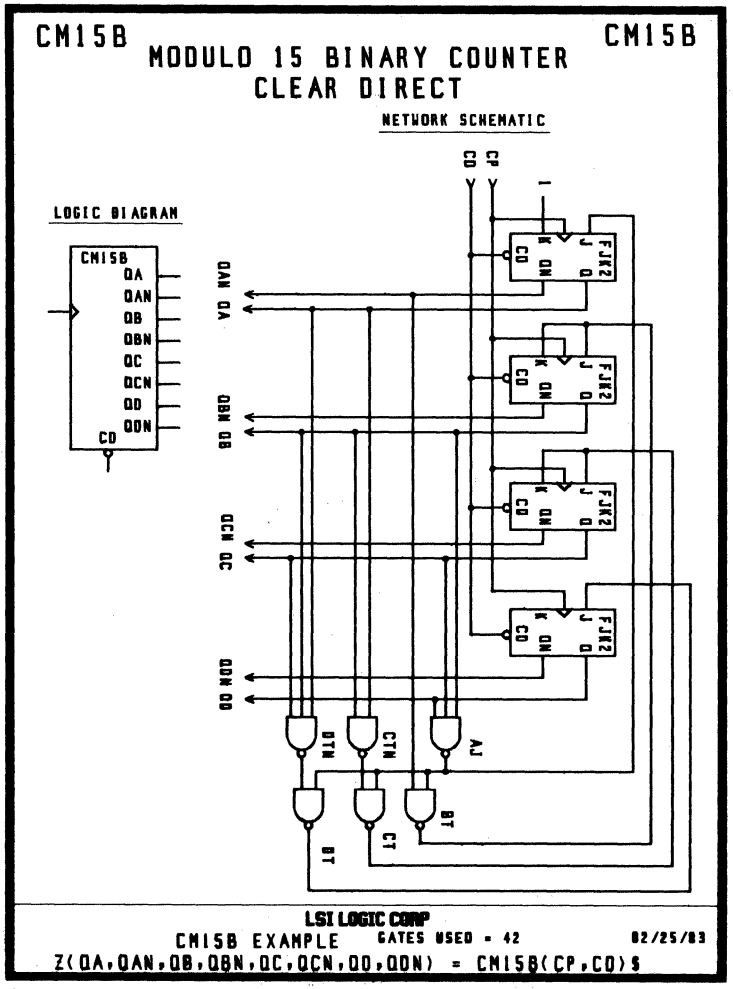


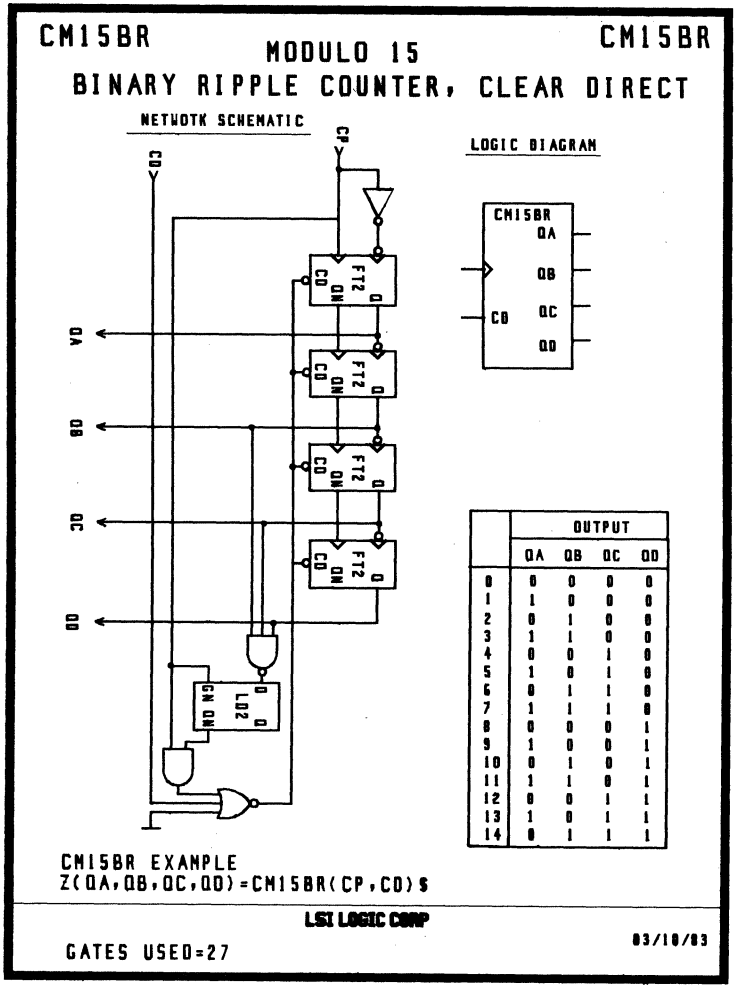
CM14J EXAMPLE
Z(QA,QAN,QB,QBN,QC,QCN,QD,QDN,QE,QEN,QF,QFN,
QG,QGN)=CM14J(CP,CD)$

LSI LOGIC CORP

03/04/83

GATES USED=42


CM15B
MODULO 15 BINARY COUNTER
CLEAR DIRECT
CM15B
NETWORK SCHEMATIC
LOGIC DIAGRAM
CM15B
QA
QAN
QB
QBN
QC
QCN
QD
QDN
CD
CP
CD
1
FJK2
J
K
CD
QN
Q
QA QAN
QB QBN
QC QCN
QD QDN
BTN
CTN
AJ
BT
CT
LSI LOGIC CORP
CM15B EXAMPLE
GATES USED = 42
02/25/83
Z(QA,QAN,QB,QBN,QC,QCN,QD,QDN) = CM15B(CP,CD)$

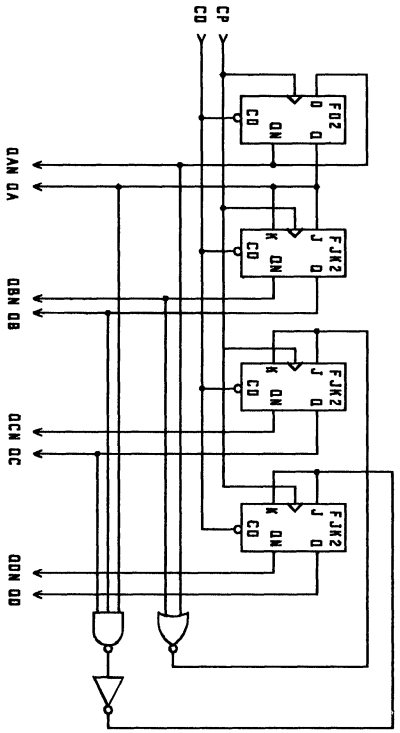

CM15BR
MODULO 15
BINARY RIPPLE COUNTER, CLEAR DIRECT
CM15BR
NETWORK SCHEMATIC
LOGIC DIAGRAM
CM15BR
QA
QB
QC
QD
CD
CP
CD
FT2
D
CD
QN
Q
QA
QB
QC
QD
CEN
LD2
OUTPUT
QA QB QC QD
0 0 0 0 0
1 1 0 0 0
2 0 1 0 0
3 1 1 0 0
4 0 0 1 0
5 1 0 1 0
6 0 1 1 0
7 1 1 1 0
8 0 0 0 1
9 1 0 0 1
10 0 1 0 1
11 1 1 0 1
12 0 0 1 1
13 1 0 1 1
14 0 1 1 1
CM15BR EXAMPLE
Z(QA,QB,QC,QD)=CM15BR(CP,CD)$
LSI LOGIC CORP
GATES USED=27
03/10/83

CM16B

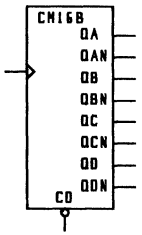
MODULO 16 BINARY COUNTER CLEAR DIRECT

CM16B

NETWORK SCHEMATIC



LOGIC DIAGRAM



LSI LOGIC CORP

CM16B EXAMPLE GATES USED = 35 02/25/83

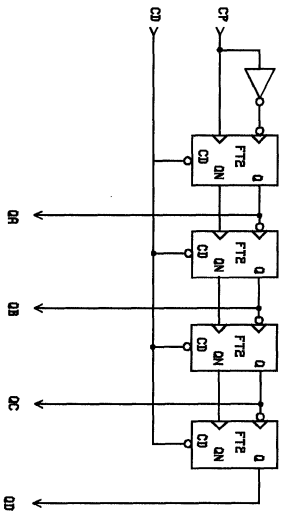
Z(QA,QAN,QB,QBN,QC,QCN,QD,QDN) = CM16B(CP,CD)$

CM16BR

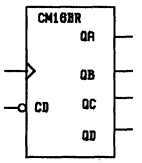
CM16BR

MODULO 16 BINARY RIPPLE COUNTER, CLEAR DIRECT

NETWOTK SCHEMATIC



LOGIC DIAGRAM



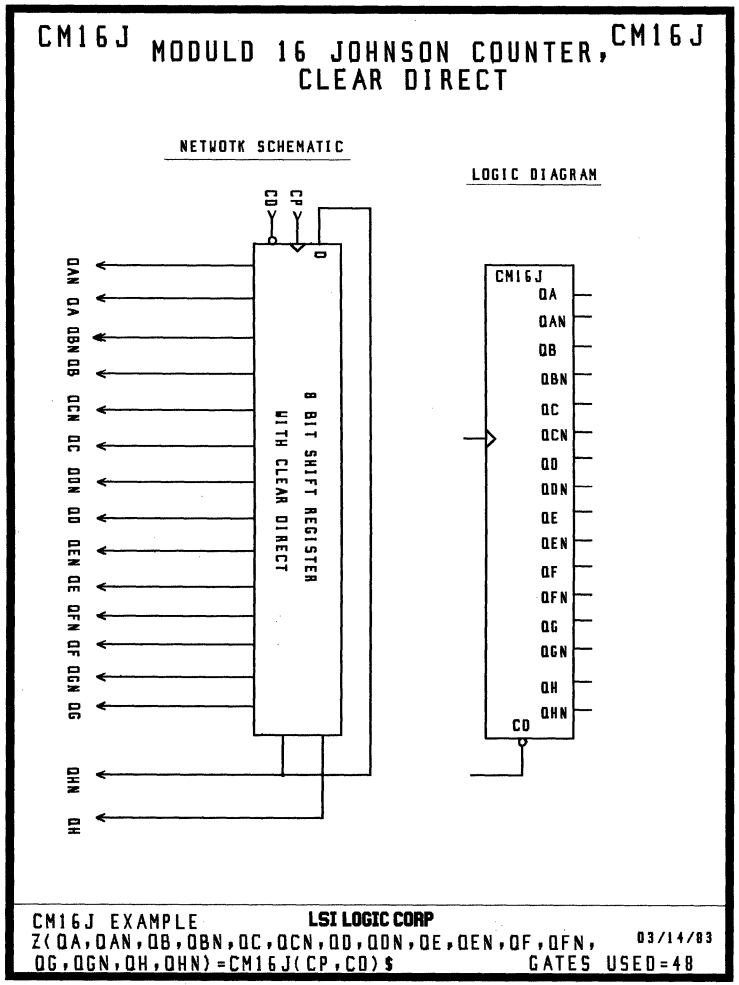
	OUTPUT			
	QA	QB	QC	QD
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
10	0	1	0	1
11	1	1	0	1
12	0	0	1	1
13	1	0	1	1
14	0	1	1	1
15	1	1	1	1

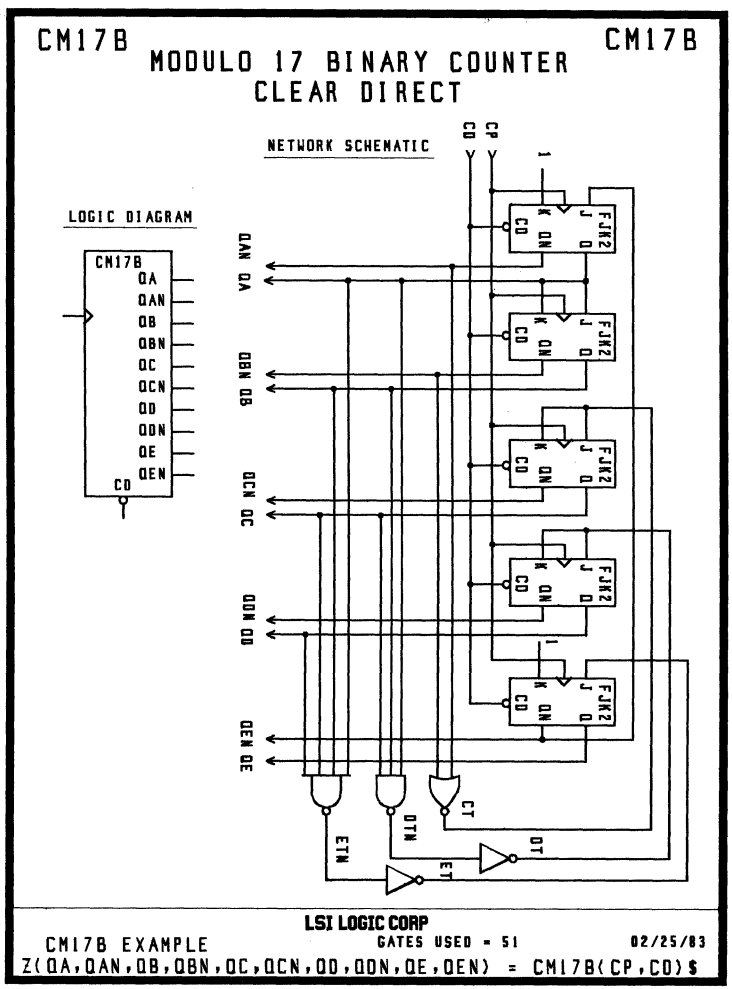
CM16BR EXAMPLE
Z(QA,QB,QC,QD)=CM16BR(CP,CD)$

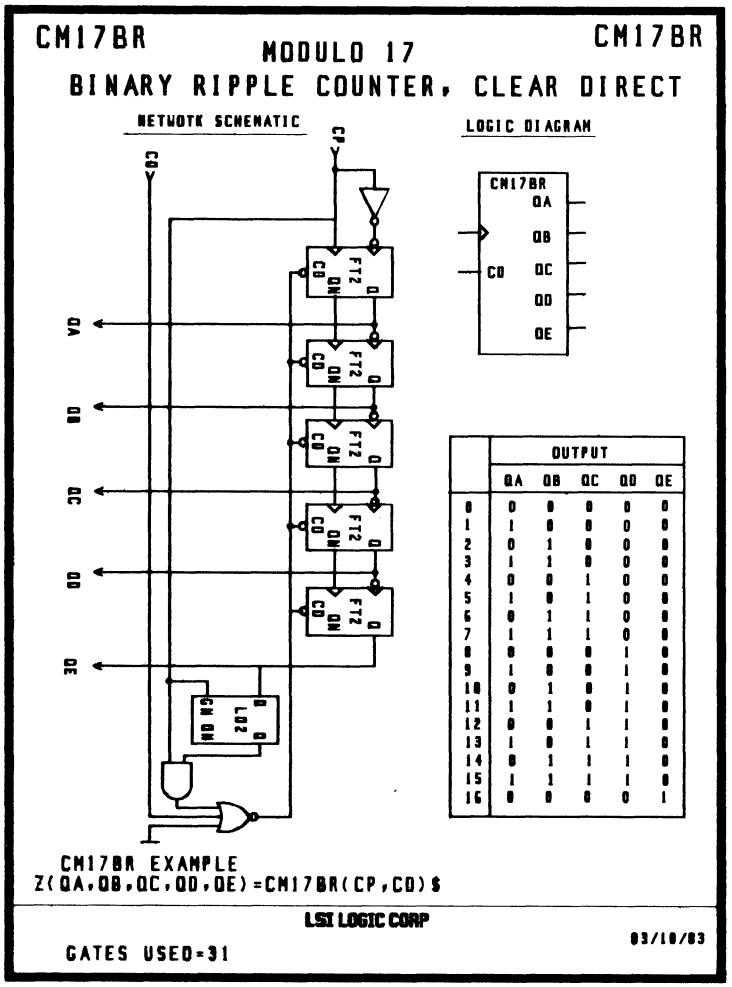
LSI LOGIC CORP

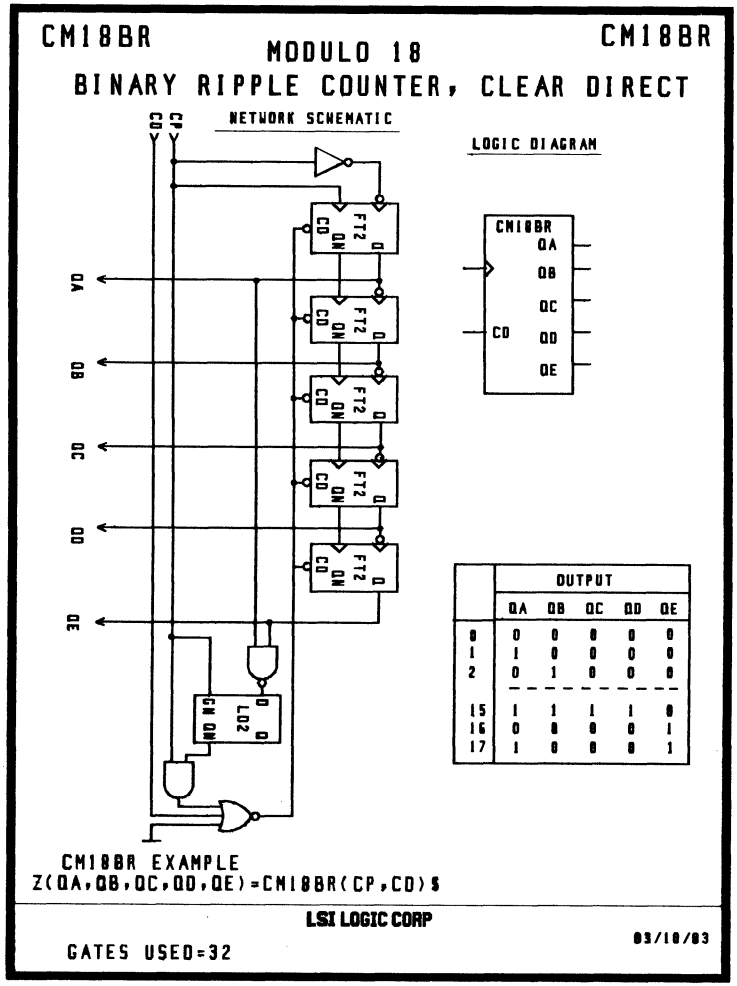
GATES USED=21

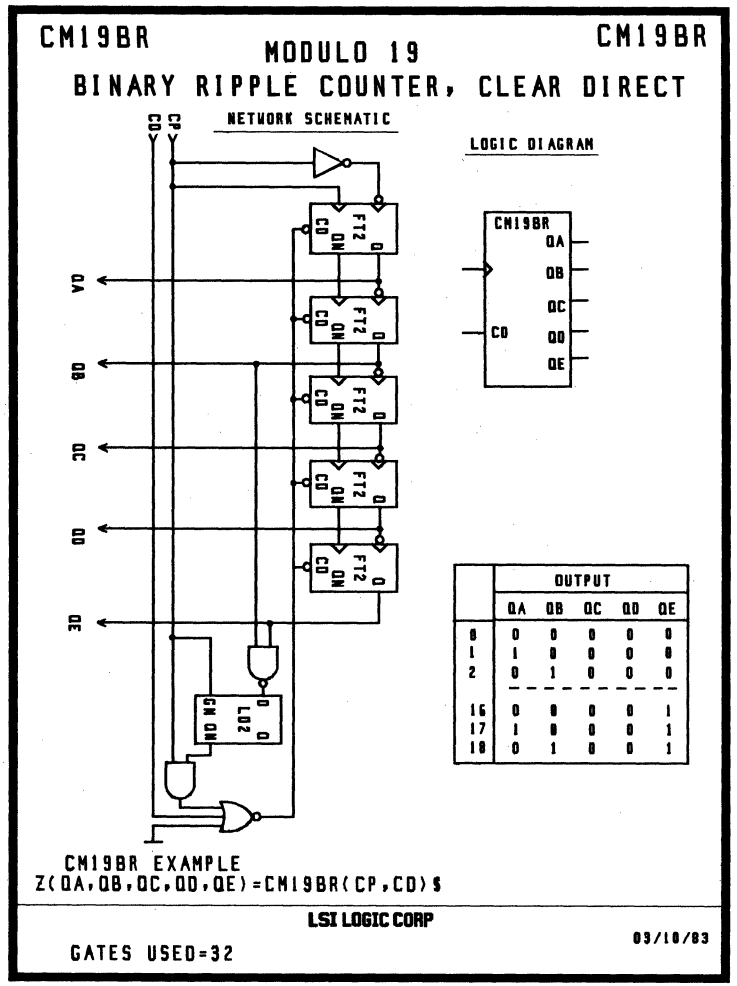
03/10/83

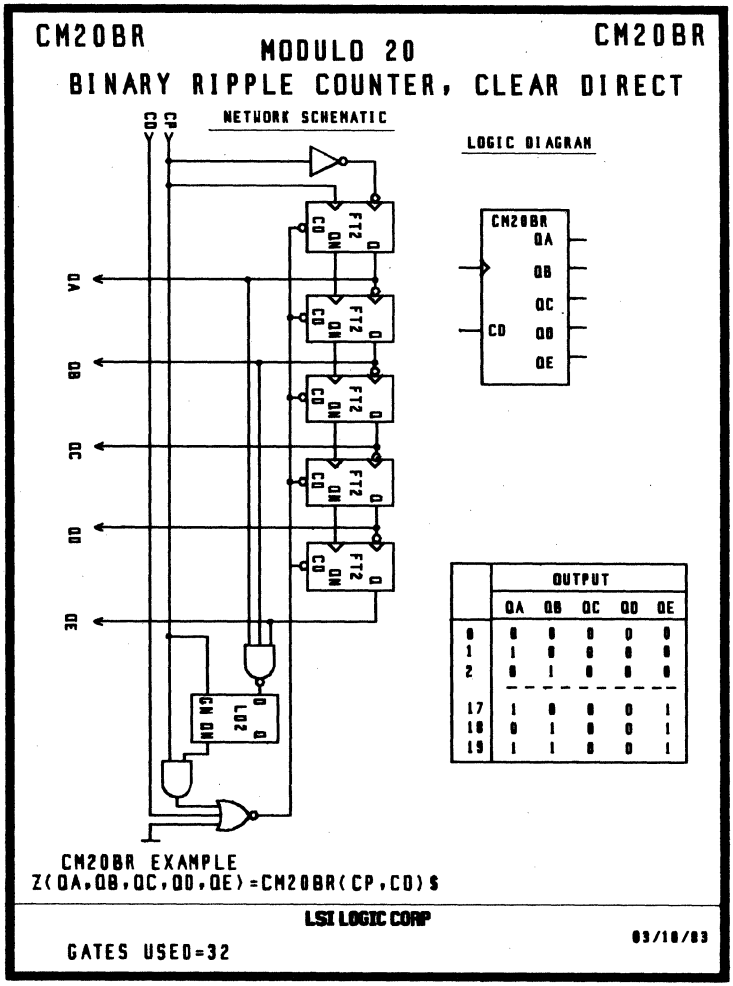

CM16J
MODULD 16 JOHNSON COUNTER,
CLEAR DIRECT
CM16J
NETWOTK SCHEMATIC
LOGIC DIAGRAM
CD
CP
D
8 BIT SHIFT REGISTER
WITH CLEAR DIRECT
QAN QA QBN QB QCN QC QDN QD QEN QE QFN QF QGN QG
QHN QH
CM16J
QA
QAN
QB
QBN
QC
QCN
QD
QDN
QE
QEN
QF
QFN
QG
QGN
QH
QHN
CD
CM16J EXAMPLE
LSI LOGIC CORP
Z(QA,QAN,QB,QBN,QC,QCN,QD,QDN,QE,QEN,QF,QFN,
QG,QGN,QH,QHN)=CM16J(CP,CD)$
03/14/83
GATES USED=48


CM17B
MODULO 17 BINARY COUNTER
CLEAR DIRECT
CM17B
NETWORK SCHEMATIC
LOGIC DIAGRAM
CM17B
QA
QAN
QB
QBN
QC
QCN
QD
QDN
QE
QEN
CD
CP
CD
1
FJK2
QAN QA
QBN QB
QCN QC
QDN QD
QEN QE
CT
QTN
ETN
QT
ET
LSI LOGIC CORP
CM17B EXAMPLE
GATES USED = 51
02/25/83
Z(QA,QAN,QB,QBN,QC,QCN,QD,QDN,QE,QEN) = CM17B(CP,CD)$


CM17BR
MODULO 17
CM17BR
BINARY RIPPLE COUNTER, CLEAR DIRECT
NETWORK SCHEMATIC
LOGIC DIAGRAM
CM17BR
QA
QB
QC
QD
QE
CO
OUTPUT
QA QB QC QD QE
CM17BR EXAMPLE
Z(QA,QB,QC,QD,QE)=CM17BR(CP,CO)$
LSI LOGIC CORP
GATES USED=31
03/10/83

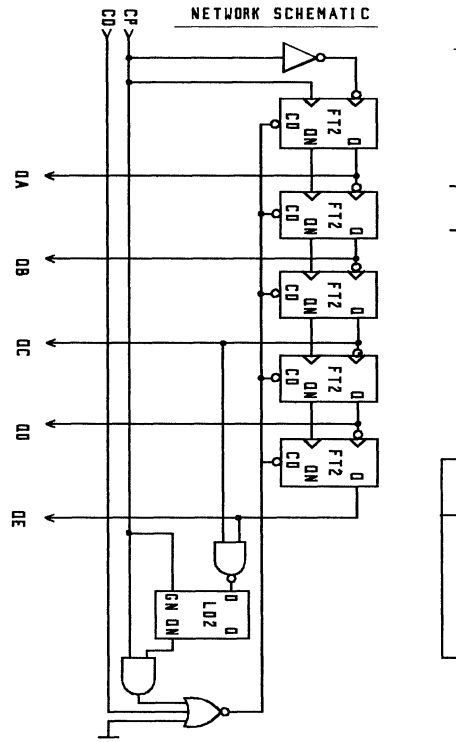

CM18BR
MODULO 18
CM18BR
BINARY RIPPLE COUNTER, CLEAR DIRECT
NETWORK SCHEMATIC
LOGIC DIAGRAM
CM18BR
QA
QB
QC
QD
QE
CO
OUTPUT
QA QB QC QD QE
CM18BR EXAMPLE
Z(QA,QB,QC,QD,QE)=CM18BR(CP,CO)$
LSI LOGIC CORP
GATES USED=32
03/10/83


CM19BR
MODULO 19
CM19BR
BINARY RIPPLE COUNTER, CLEAR DIRECT
NETWORK SCHEMATIC
LOGIC DIAGRAM
CM19BR
QA
QB
QC
QD
QE
CD
OUTPUT
QA QB QC QD QE
0 0 0 0 0 0
1 1 0 0 0 0
2 0 1 0 0 0
16 0 0 0 0 1
17 1 0 0 0 1
18 0 1 0 0 1
CM19BR EXAMPLE
Z(QA,QB,QC,QD,QE)=CM19BR(CP,CD)$
LSI LOGIC CORP
GATES USED=32
03/10/83

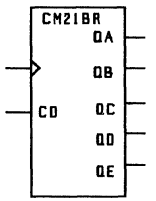

CM20BR
MODULO 20
CM20BR
BINARY RIPPLE COUNTER, CLEAR DIRECT
NETWORK SCHEMATIC
LOGIC DIAGRAM
CM20BR
QA
QB
QC
QD
QE
CD
OUTPUT
QA QB QC QD QE
0 0 0 0 0 0
1 1 0 0 0 0
2 0 1 0 0 0
17 1 0 0 0 1
18 0 1 0 0 1
19 1 1 0 0 1
CM20BR EXAMPLE
Z(QA,QB,QC,QD,QE)=CM20BR(CP,CD)$
LSI LOGIC CORP
GATES USED=32
03/10/83

CM21BR MODULO 21 CM21BR

BINARY RIPPLE COUNTER, CLEAR DIRECT



LOGIC DIAGRAM



	OUTPUT				
	QA	QB	QC	QD	QE
0	0	0	0	0	0
1	1	0	0	0	0
2	0	1	0	0	0
18	0	1	0	0	1
19	1	1	0	0	1
20	0	0	1	0	1

CM21BR EXAMPLE

Z(QA,QB,QC,QD,QE)=CM21BR(CP,CD)$

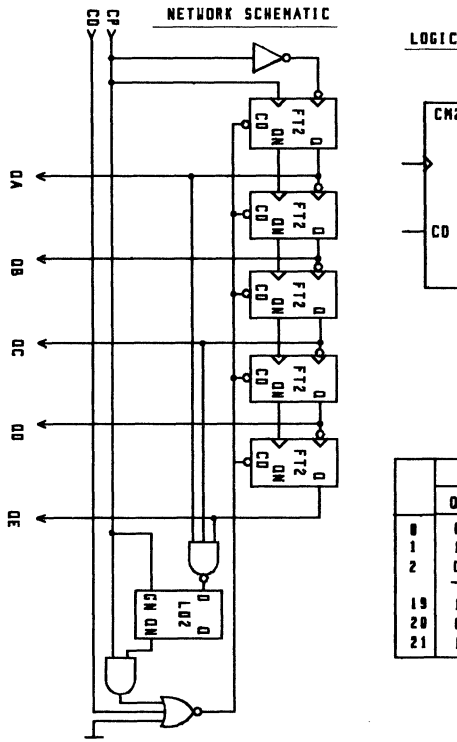
LSI LOGIC CORP

05/10/83

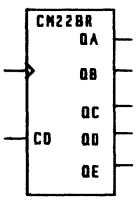
GATES USED=32

CM22BR MODULO 22 CM22BR

BINARY RIPPLE COUNTER, CLEAR DIRECT



LOGIC DIAGRAM



	OUTPUT				
	QA	QB	QC	QD	QE
0	0	0	0	0	0
1	1	0	0	0	0
2	0	1	0	0	0
19	1	1	0	0	1
20	0	0	1	0	1
21	1	0	1	0	1

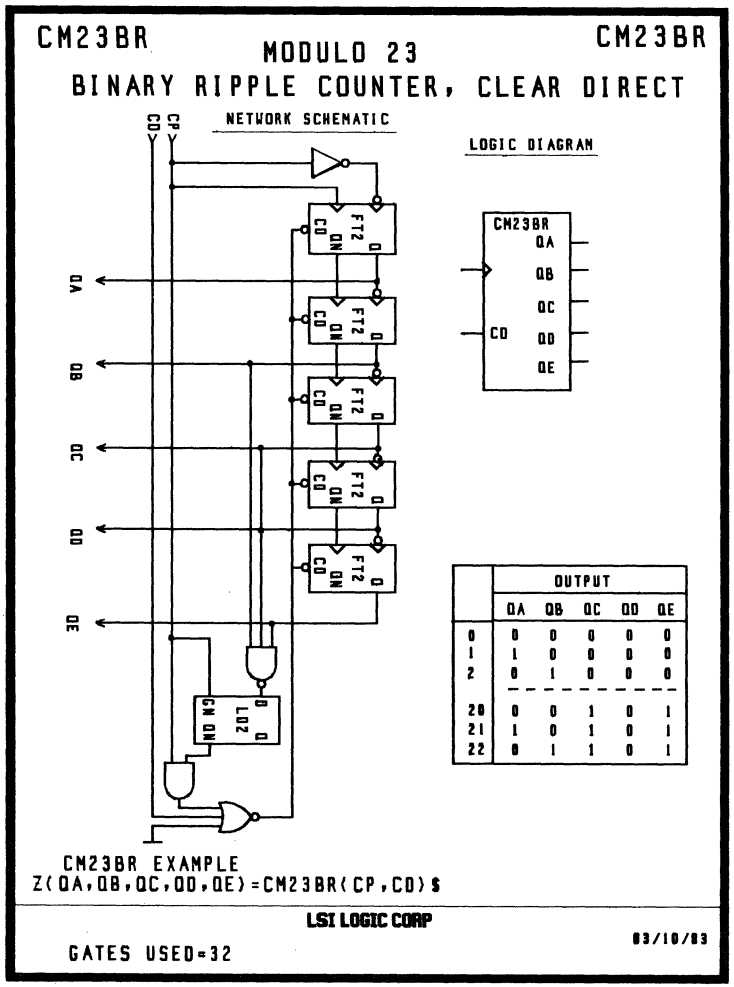
CM22BR EXAMPLE

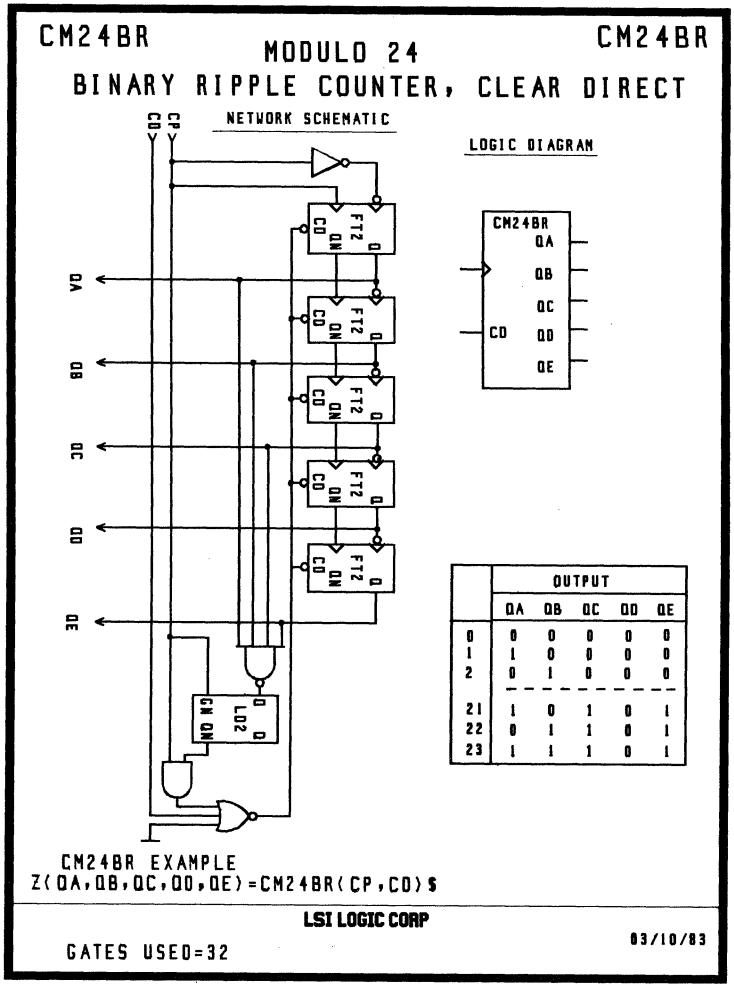
Z(QA,QB,QC,QD,QE)=CM22BR(CP,CD)$

LSI LOGIC CORP

03/10/83

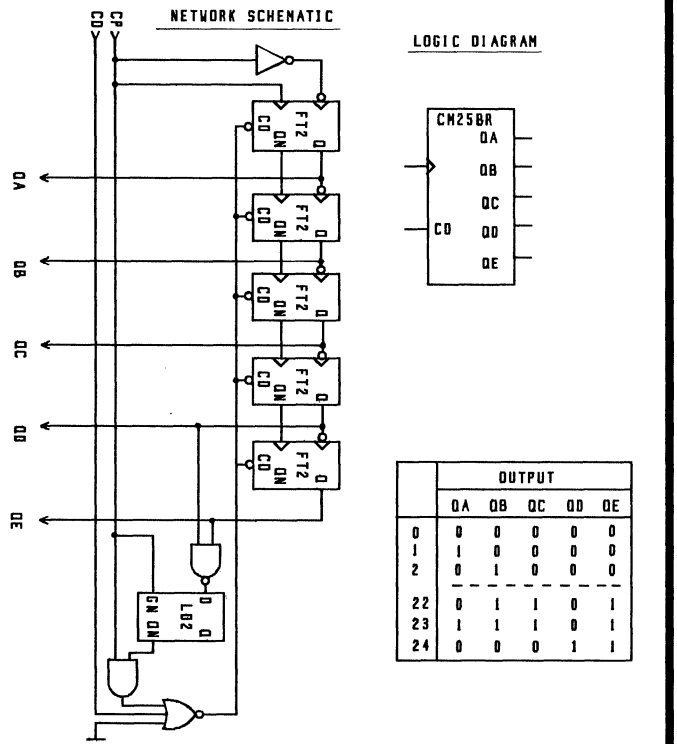
GATES USED=32


CM23BR
MODULO 23
CM23BR
BINARY RIPPLE COUNTER, CLEAR DIRECT
NETWORK SCHEMATIC
LOGIC DIAGRAM
CM23BR
QA
QB
QC
QD
QE
CD
OUTPUT
QA QB QC QD QE
0 0 0 0 0 0
1 1 0 0 0 0
2 0 1 0 0 0
20 0 0 1 0 1
21 1 0 1 0 1
22 0 1 1 0 1
CM23BR EXAMPLE
Z(QA,QB,QC,QD,QE)=CM23BR(CP,CD)$
LSI LOGIC CORP
GATES USED=32
03/10/83


CM24BR
MODULO 24
CM24BR
BINARY RIPPLE COUNTER, CLEAR DIRECT
NETWORK SCHEMATIC
LOGIC DIAGRAM
CM24BR
QA
QB
QC
QD
QE
CD
OUTPUT
QA QB QC QD QE
0 0 0 0 0 0
1 1 0 0 0 0
2 0 1 0 0 0
21 1 0 1 0 1
22 0 1 1 0 1
23 1 1 1 0 1
CM24BR EXAMPLE
Z(QA,QB,QC,QD,QE)=CM24BR(CP,CD)$
LSI LOGIC CORP
GATES USED=32
03/10/83

CM25BR MODULO 25 CM25BR

BINARY RIPPLE COUNTER, CLEAR DIRECT



LOGIC DIAGRAM

	OUTPUT				
	QA	QB	QC	QD	QE
0	0	0	0	0	0
1	1	0	0	0	0
2	0	1	0	0	0
22	0	1	1	0	1
23	1	1	1	0	1
24	0	0	0	1	1

CM25BR EXAMPLE

Z(QA,QB,QC,QD,QE)=CM25BR(CP,CD)$

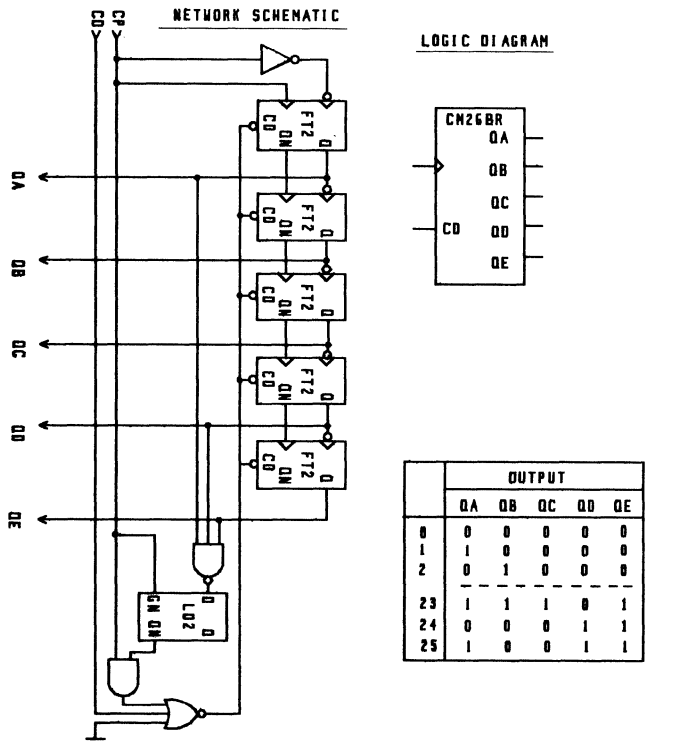
LSI LOGIC CORP

GATES USED=32

03/11/83

CM26BR MODULO 26 CM26BR

BINARY RIPPLE COUNTER, CLEAR DIRECT



LOGIC DIAGRAM

	OUTPUT				
	QA	QB	QC	QD	QE
0	0	0	0	0	0
1	1	0	0	0	0
2	0	1	0	0	0
23	1	1	1	0	1
24	0	0	0	1	1
25	1	0	0	1	1

CM26BR EXAMPLE

Z(QA,QB,QC,QD,QE)=CM26BR(CP,CD)$

LSI LOGIC CORP

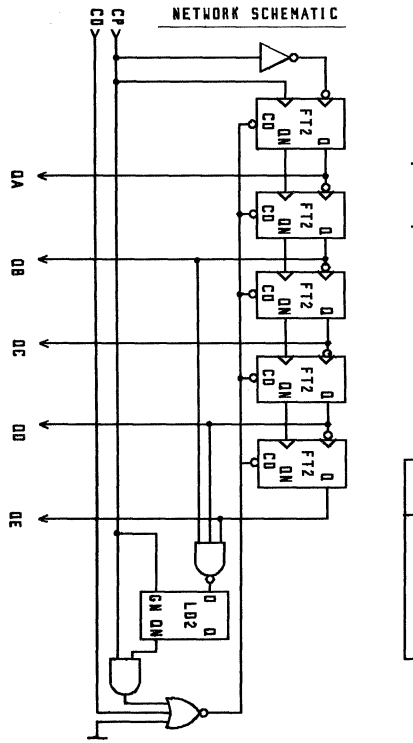
GATES USED=32

03/11/83

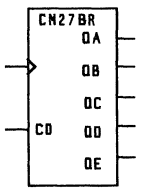
CM27BR MODULO 27 CM27BR

BINARY RIPPLE COUNTER, CLEAR DIRECT

NETWORK SCHEMATIC



LOGIC DIAGRAM



	OUTPUT				
	QA	QB	QC	QD	QE
0	0	0	0	0	0
1	1	0	0	0	0
2	0	1	0	0	0
24	1	1	1	0	1
25	0	0	0	1	1
26	1	0	0	1	1

CM27BR EXAMPLE

Z(QA,QB,QC,QD,QE)=CM27BR(CP,CD)$

LSI LOGIC CORP

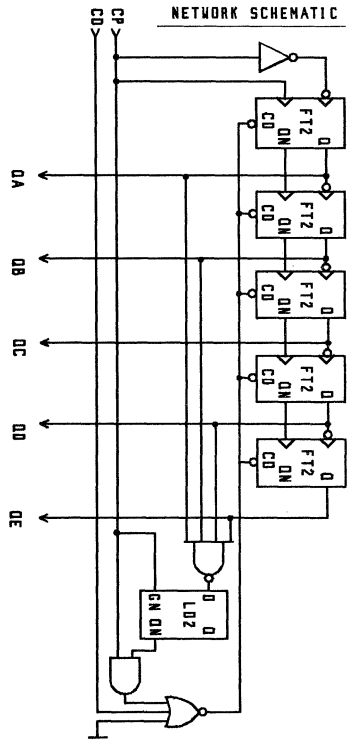
03/11/83

GATES USED=32

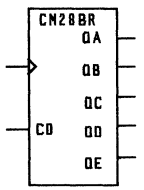
CM28BR MODULO 28 CM28BR

BINARY RIPPLE COUNTER, CLEAR DIRECT

NETWORK SCHEMATIC



LOGIC DIAGRAM



	OUTPUT				
	QA	QB	QC	QD	QE
0	0	0	0	0	0
1	1	0	0	0	0
2	0	1	0	0	0
25	1	0	0	1	1
26	0	1	0	1	1
27	1	1	0	1	1

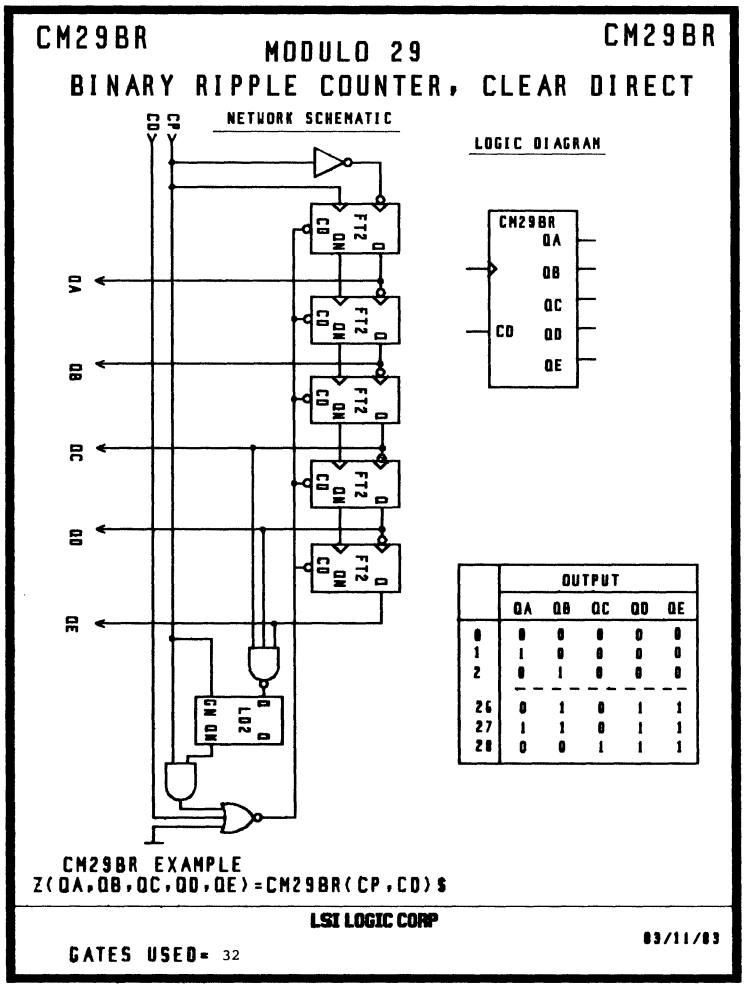
CM28BR EXAMPLE

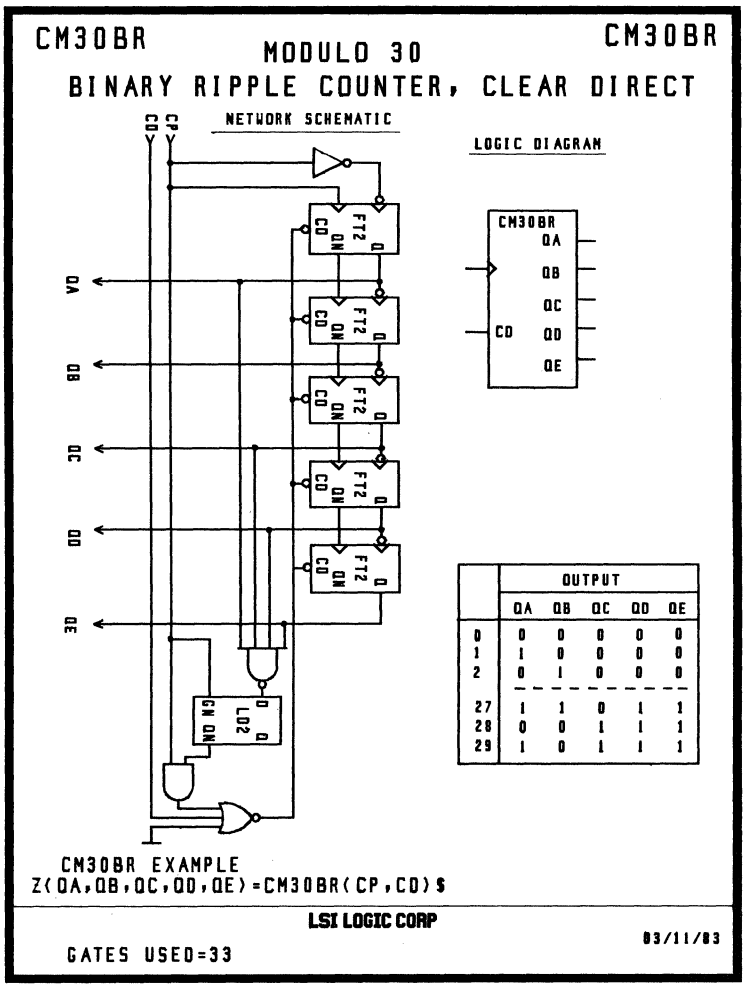
Z(QA,QB,QC,QD,QE)=CM28BR(CP,CD)$

LSI LOGIC CORP

03/11/83

GATES USED=33

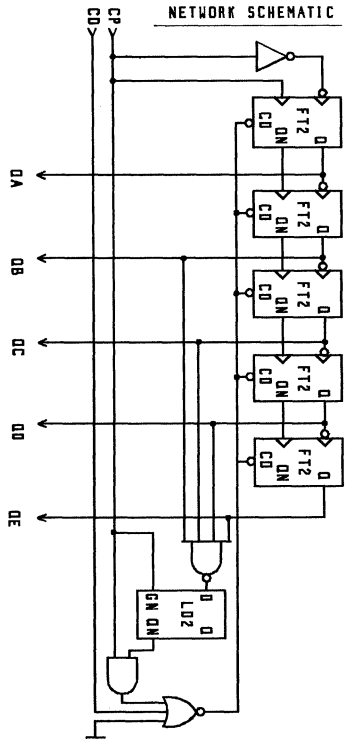

CM29BR
MODULO 29
CM29BR
BINARY RIPPLE COUNTER, CLEAR DIRECT
NETWORK SCHEMATIC
LOGIC DIAGRAM
CM29BR
QA
QB
QC
QD
QE
CD
OUTPUT
QA QB QC QD QE
0 0 0 0 0 0
1 1 0 0 0 0
2 0 1 0 0 0
26 0 1 0 1 1
27 1 1 0 1 1
28 0 0 1 1 1
CM29BR EXAMPLE
Z(QA,QB,QC,QD,QE)=CM29BR(CP,CD)$
LSI LOGIC CORP
03/11/83
GATES USED= 32


CM30BR
MODULO 30
CM30BR
BINARY RIPPLE COUNTER, CLEAR DIRECT
NETWORK SCHEMATIC
LOGIC DIAGRAM
CM30BR
QA
QB
QC
QD
QE
CD
OUTPUT
QA QB QC QD QE
0 0 0 0 0 0
1 1 0 0 0 0
2 0 1 0 0 0
27 1 1 0 1 1
28 0 0 1 1 1
29 1 0 1 1 1
CM30BR EXAMPLE
Z(QA,QB,QC,QD,QE)=CM30BR(CP,CD)$
LSI LOGIC CORP
03/11/83
GATES USED=33

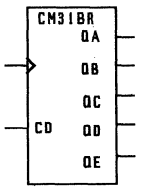
CM31BR MODULO 31 CM31BR

BINARY RIPPLE COUNTER, CLEAR DIRECT

NETWORK SCHEMATIC



LOGIC DIAGRAM



	OUTPUT				
	QA	QB	QC	QD	QE
0	0	0	0	0	0
1	1	0	0	0	0
2	0	1	0	0	0
28	0	0	1	1	1
29	1	0	1	1	1
30	0	1	1	1	1

CM31BR EXAMPLE
Z(QA,QB,QC,QD,QE)=CM31BR(CP,CD)$

LSI LOGIC CORP

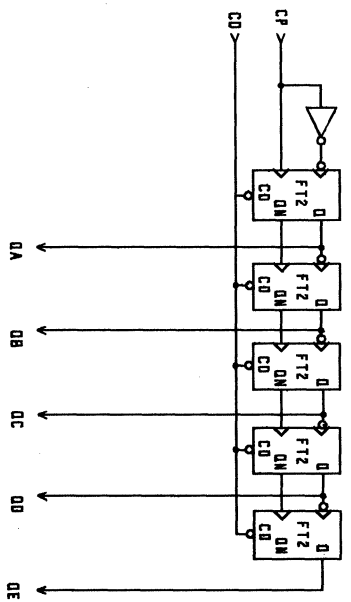
03/11/83

GATES USED=33

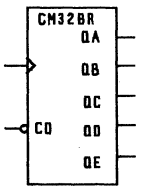
CM32BR MODULO 32 CM32BR

BINARY RIPPLE COUNTER, CLEAR DIRECT

NETWORK SCHEMATIC



LOGIC DIAGRAM



	OUTPUT				
	QA	QB	QC	QD	QE
0	0	0	0	0	0
1	1	0	0	0	0
2	0	1	0	0	0
30	0	1	1	1	1
30	1	1	1	1	1

CM32BR EXAMPLE
Z(QA,QB,QC,QD,QE)=CM32BR(CP,CD)$

LSI LOGIC CORP

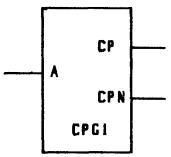
03/11/83

GATES USED=26

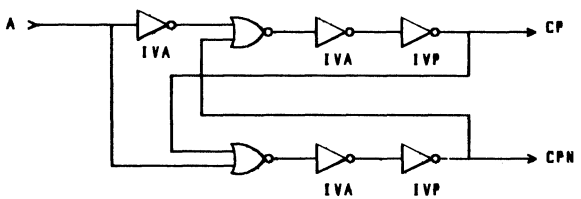
CPG1 CPG1

TWO PHASE CLOCK GENERATOR, UNBUFFERED, HI UNDERLAP LO DRIVE

LOGIC DIAGRAM



NETWORK SCHEMATIC



CPG1 EXAMPLE
Z(CP,CPN)=CPG1(A)$

GATES USED = 7

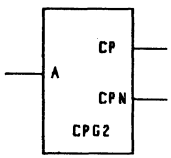
LSI LOGIC CORP

13/01/83

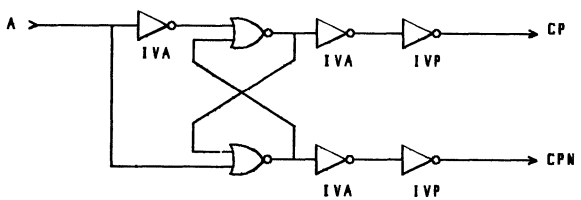
CPG2 CPG2

TWO PHASE CLOCK GENERATOR, UNBUFFERED, LO UNDERLAP LO DRIVE

LOGIC DIAGRAM



NETWORK SCHEMATIC



CPG2 EXAMPLE
Z(CP,CPN)=CPG2(A)$

GATES USED = 7

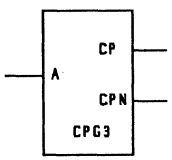
LSI LOGIC CORP

13/11/83

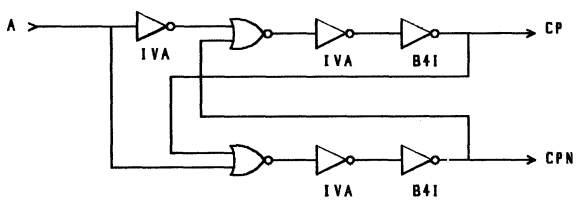
CPG3 CPG3

TWO PHASE CLOCK GENERATOR, UNBUFFERED, HI UNDERLAP HI DRIVE

LOGIC DIAGRAM



NETWORK SCHEMATIC



CPG3 EXAMPLE
Z(CP,CPN)=CPG3(A)$

LSI LOGIC CORP

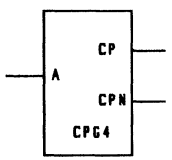
GATES USED = 9

13/11/83

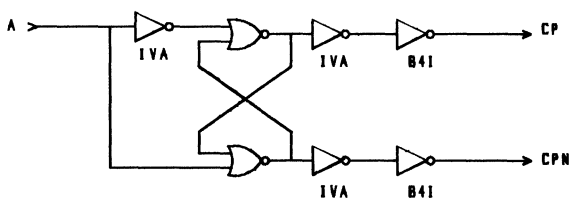
CPG4 CPG4

TWO PHASE CLOCK GENERATOR, UNBUFFERED, LO UNDERLAP HI DRIVE

LOGIC DIAGRAM



NETWORK SCHEMATIC

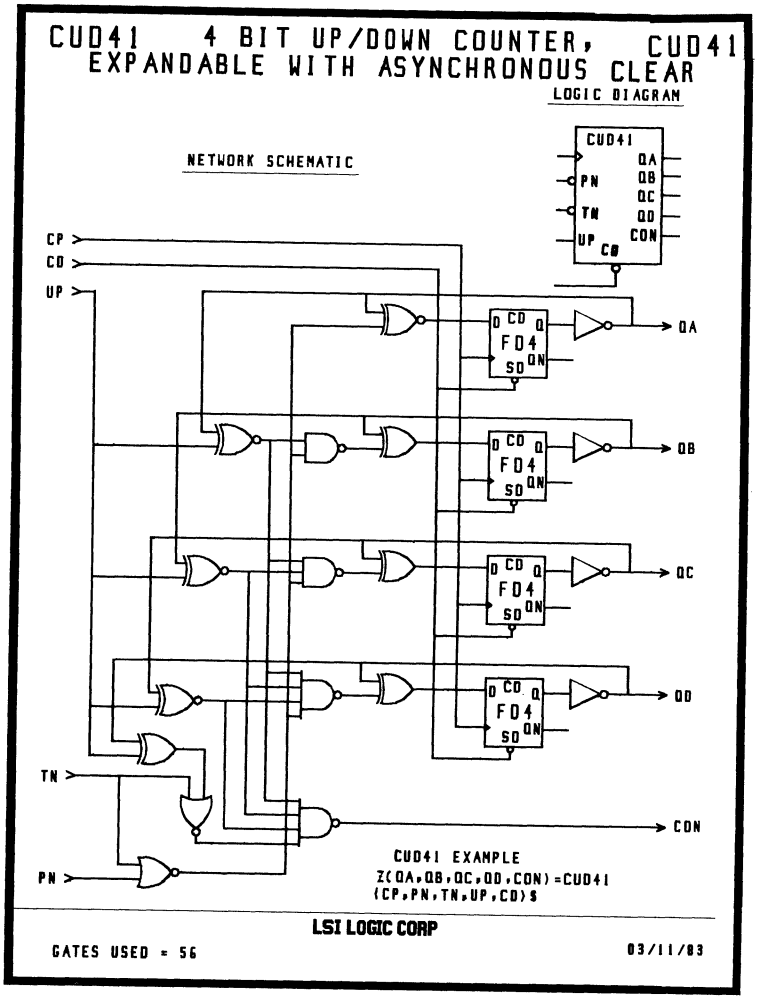


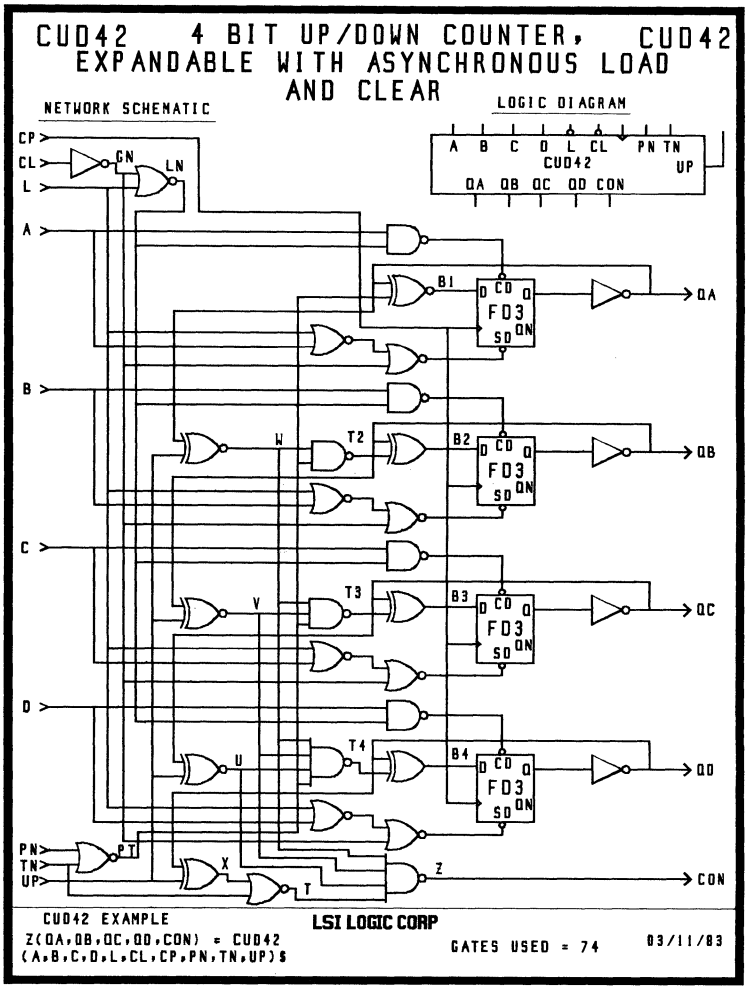
CPG4 EXAMPLE
Z(CP,CPN)=CPG4(A)$

LSI LOGIC CORP

GATES USED = 9

83/11/83

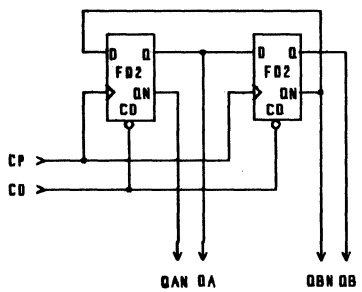

CUD41 4 BIT UP/DOWN COUNTER, CUD41
EXPANDABLE WITH ASYNCHRONOUS CLEAR
LOGIC DIAGRAM
NETWORK SCHEMATIC
CUD41
QA
QB
QC
QD
CON
PN
TN
UP
CD
CP
FD4
QN
SD
CUD41 EXAMPLE
Z(QA,QB,QC,QD,CON)=CUD41
(CP,PN,TN,UP,CD)$
LSI LOGIC CORP
GATES USED = 56
03/11/83


CUD42 4 BIT UP/DOWN COUNTER, CUD42
EXPANDABLE WITH ASYNCHRONOUS LOAD
AND CLEAR
NETWORK SCHEMATIC
LOGIC DIAGRAM
A B C D L CL PN TN
CUD42
UP
QA QB QC QD CON
CP
CL
L
A
B
C
D
PN
TN
UP
GN
LN
PT
B1
B2
B3
B4
T2
T3
T4
W
V
U
X
T
Z
FD3
CD
SD
QN
CUD42 EXAMPLE
Z(QA,QB,QC,QD,CON) = CUD42
(A,B,C,D,L,CL,CP,PN,TN,UP)$
LSI LOGIC CORP
GATES USED = 74
03/11/83

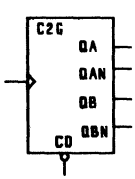
C2G C2G

MODULO 4 GRAY COUNTER
CLEAR DIRECT (SAME AS CM4J)

NETWORK SCHEMATIC



LOGIC DIAGRAM



OUTPUT	
QA	QB
0	0
1	0
1	1
0	1

C2G EXAMPLE

Z(QA,QAN,QB,QBN) = C2G(CP,CD)$

LSI LOGIC CORP

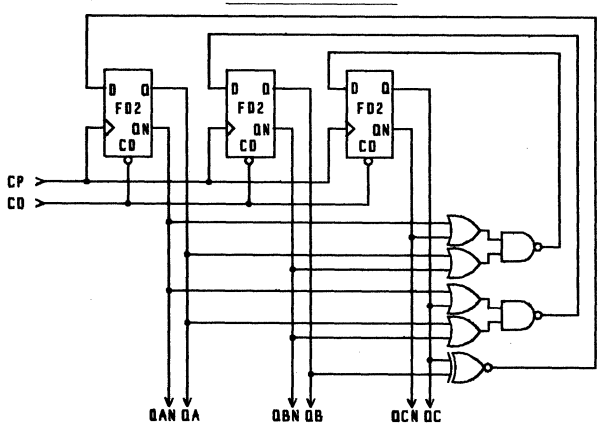
GATES USED = 12

03/06/83

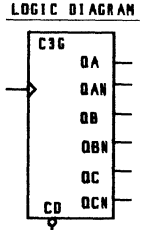
C3G C3G

MODULO 8 GRAY COUNTER
CLEAR DIRECT

NETWORK SCHEMATIC



LOGIC DIAGRAM



OUTPUT		
QA	QB	QC
0	0	0
1	0	0
1	1	0
0	1	0
0	1	1
1	1	1
1	0	1
0	0	1

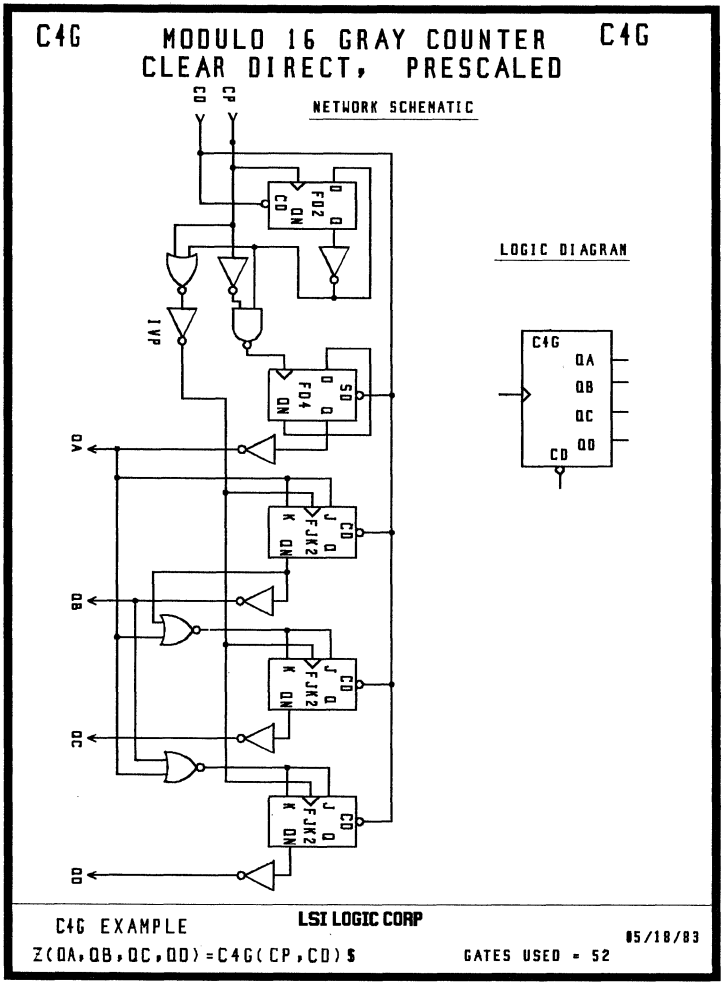
C3G EXAMPLE

Z(QA,QAN,QB,QBN,QC,QCN)=C3G(CP,CD)$

LSI LOGIC CORP

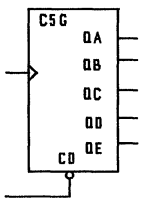
GATES USED = 27

03/06/83

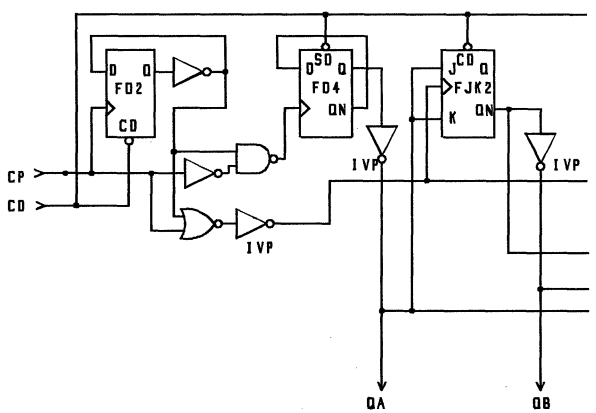

C4G
MODULO 16 GRAY COUNTER
CLEAR DIRECT, PRESCALED
C4G
NETWORK SCHEMATIC
LOGIC DIAGRAM
C4G
QA
QB
QC
QD
CD
C4G EXAMPLE
LSI LOGIC CORP
05/18/83
Z(QA,QB,QC,QD)=C4G(CP,CD)$
GATES USED = 52

C5G MODULO 32 GRAY COUNTER C5G
CLEAR DIRECT, PRESCALED

LOGIC DIAGRAM



NETWORK SCHEMATIC PART I

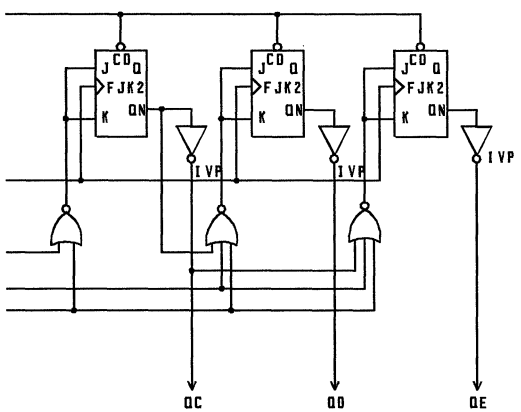


C5G EXAMPLE LSI LOGIC CORP 05/18/83

Z(QA,QB,QC,QD,QE)=C5G(CP,CD)$ GATES USED = 64

C5G MODULO 32 GRAY COUNTER C5G
CLEAR DIRECT, PRESCALED

NETWORK SCHEMATIC PART II

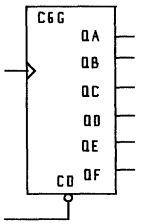


C5G EXAMPLE LSI LOGIC CORP 05/18/83

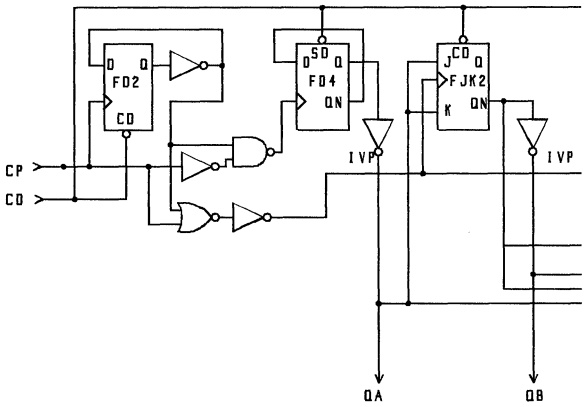
Z(QA,QB,QC,QD,QE)=C5G(CP,CD)$ GATES USED = 64

C6G MODULO 64 GRAY COUNTER C6G
CLEAR DIRECT, PRESCALED

LOGIC DIAGRAM



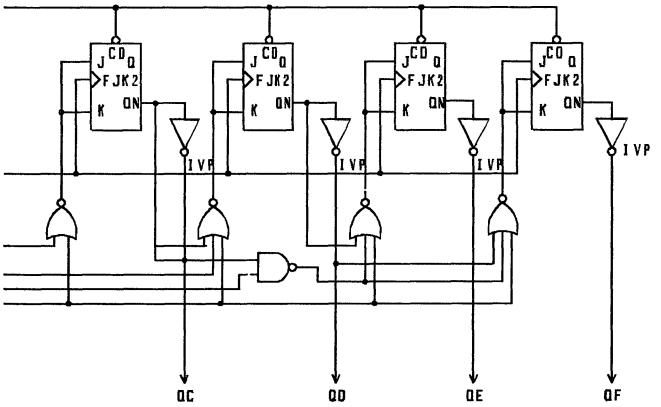
NETWORK SCHEMATIC PART I



C6G EXAMPLE LSI LOGIC CORP 05/18/83
Z(QA,QB,QC,QD,QE,QF)=C6G(CP,CD)$ GATES USED = 88

C6G MODULO 64 GRAY COUNTER C6G
CLEAR DIRECT, PRESCALED

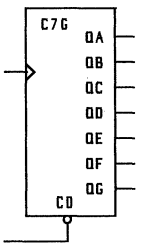
NETWORK SCHEMATIC PART II



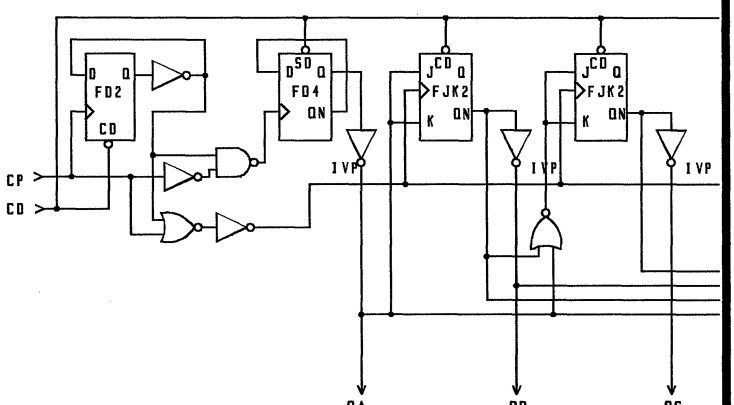
C6G EXAMPLE LSI LOGIC CORP 06/21/83
Z(QA,QB,QC,QD,QE,QF)=C6G(CP,CD)$ GATES USED = 88

C7G MODULO 128 GRAY COUNTER C7G
CLEAR DIRECT, PRESCALED

LOGIC DIAGRAM



NETWORK SCHEMATIC PART I



C7G EXAMPLE

Z(QA,QB,QC,QD,QE,QF,QG)=C7G(CP,CD)$

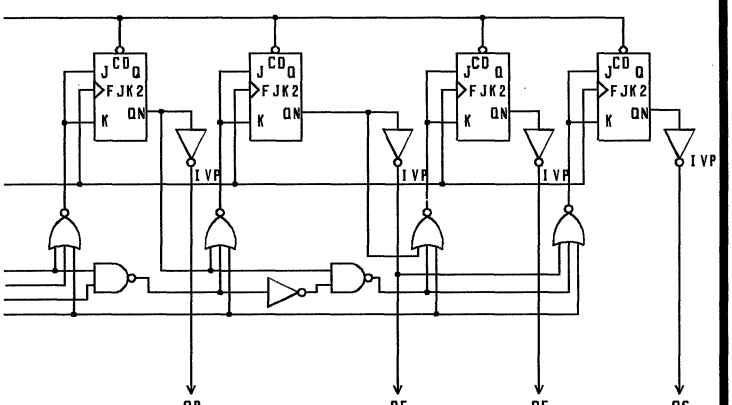
LSI LOGIC CORP

GATES USED = 100

05/18/83

C7G MODULO 128 GRAY COUNTER C7G
CLEAR DIRECT, PRESCALED

NETWORK SCHEMATIC PART II



C7G EXAMPLE

Z(QA,QB,QC,QD,QE,QF,QG)=C7G(CP,CD)$

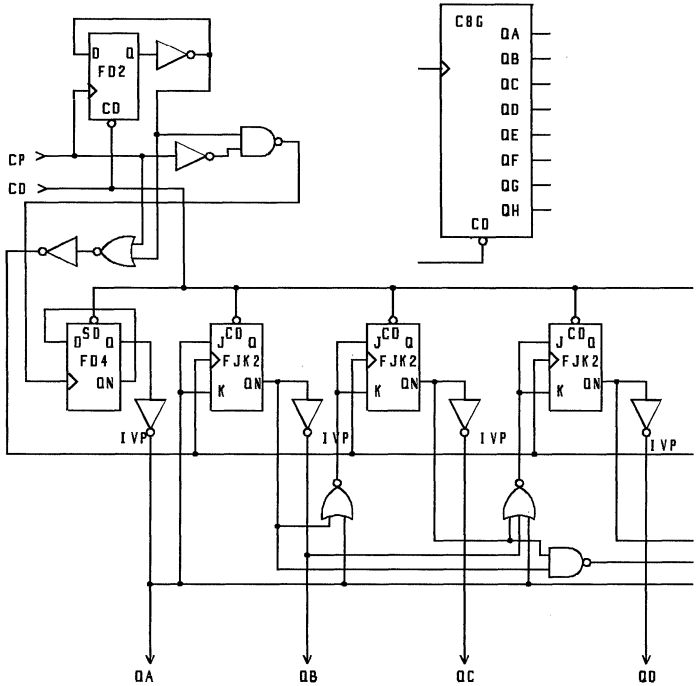
LSI LOGIC CORP

GATES USED = 100

05/18/83

C8G MODULO 256 GRAY COUNTER C8G
CLEAR DIRECT, PRESCALED

NETWORK SCHEMATIC PART I



LOGIC DIAGRAM

C8G EXAMPLE
Z(QA,QB,QC,QD,QE,QF,QG,QH)=C8G(CP,CD)$

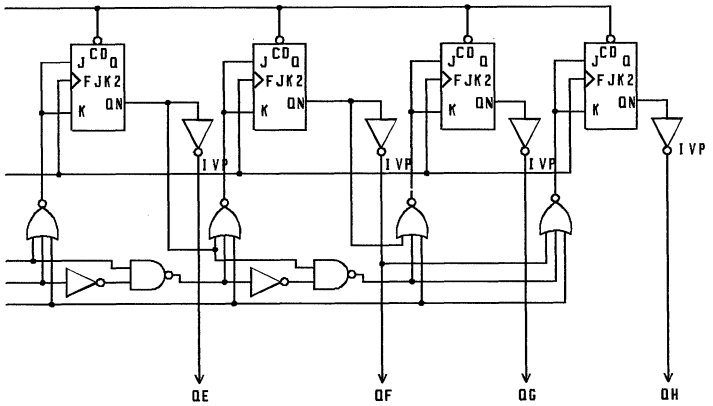
LSI LOGIC CORP

GATES USED = 114

05/18/83

C8G MODULO 256 GRAY COUNTER C8G
CLEAR DIRECT, PRESCALED

NETWORK SCHEMATIC PART II



C8G EXAMPLE
Z(QA,QB,QC,QD,QE,QF,QG,QH)=C8G(CP,CD)$

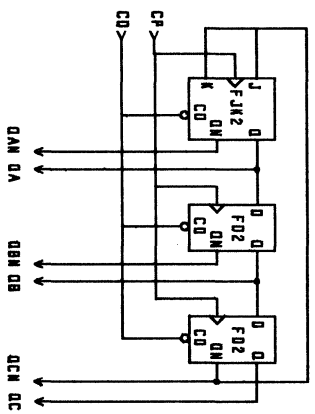
LSI LOGIC CORP

GATES USED = 114

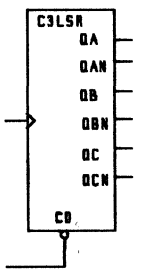
05/18/83

C3LSR 3 BIT, MODULO 7, LINEAR FEEDBACK SHIFT REGISTER C3LSR

NETWORK SCHEMATIC



LOGIC DIAGRAM



OUTPUT

QA	QB	QC
0	0	0
1	0	0
0	1	0
1	0	1
1	1	0
0	1	1
0	0	1

C3LSR EXAMPLE
Z(QA,QAN,QB,QBN,QC,QCN)
=C3LSR(CP,CD)$

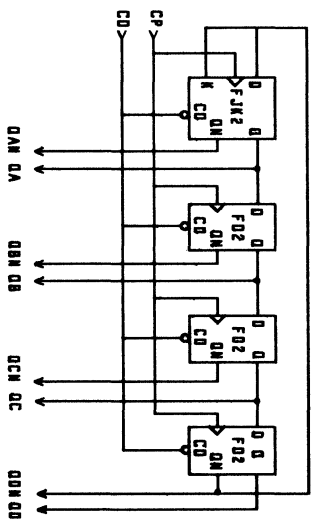
LSI LOGIC CORP

GATES USED=21

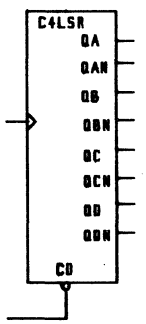
03/05/03

C4LSR 4 BIT, MODULO 15, LINEAR FEEDBACK SHIFT REGISTER C4LSR

NETWORK SCHEMATIC



LOGIC DIAGRAM



C4LSR EXAMPLE
Z(QA,QAN,QB,QBN,QC,QCN,QD,QDN)
=C4LSR(CP,CD)$

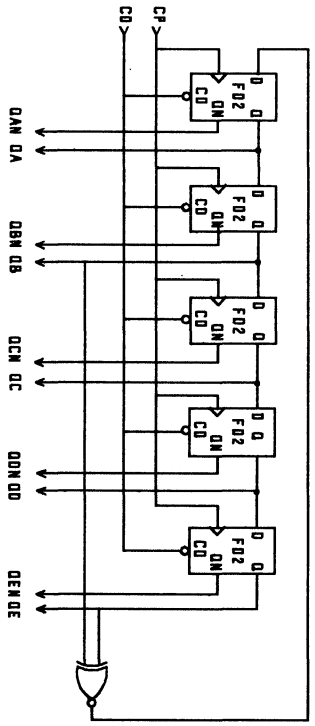
LSI LOGIC CORP

GATES USED=27

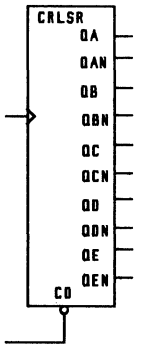
02/21/03

C5LSR 5 BIT, MODULO 31, LINEAR FEEDBACK SHIFT REGISTER C5LSR

NETWOTK SCHEMATIC



LOGIC DIAGRAM



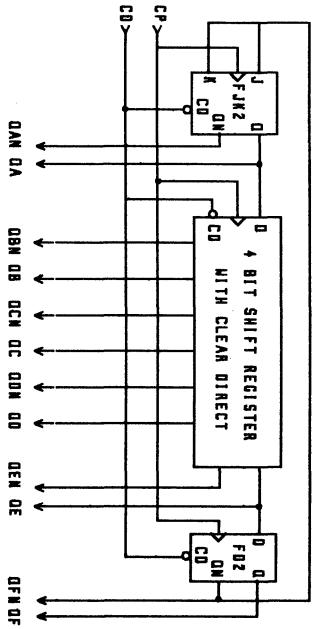
C5LSR
Z(QA,QAN,QB,QBN,QC,QCN,QD,QDN,QE,QEN)
=C5LSR(CP,CD)$

LSI LOGIC CORP
GATES USED=36

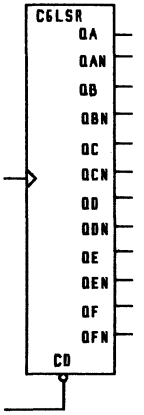
02/21/83

C6LSR 6 BIT, MODULO 63, LINEAR FEEDBACK SHIFT REGISTER C6LSR

NETWOTK SCHEMATIC



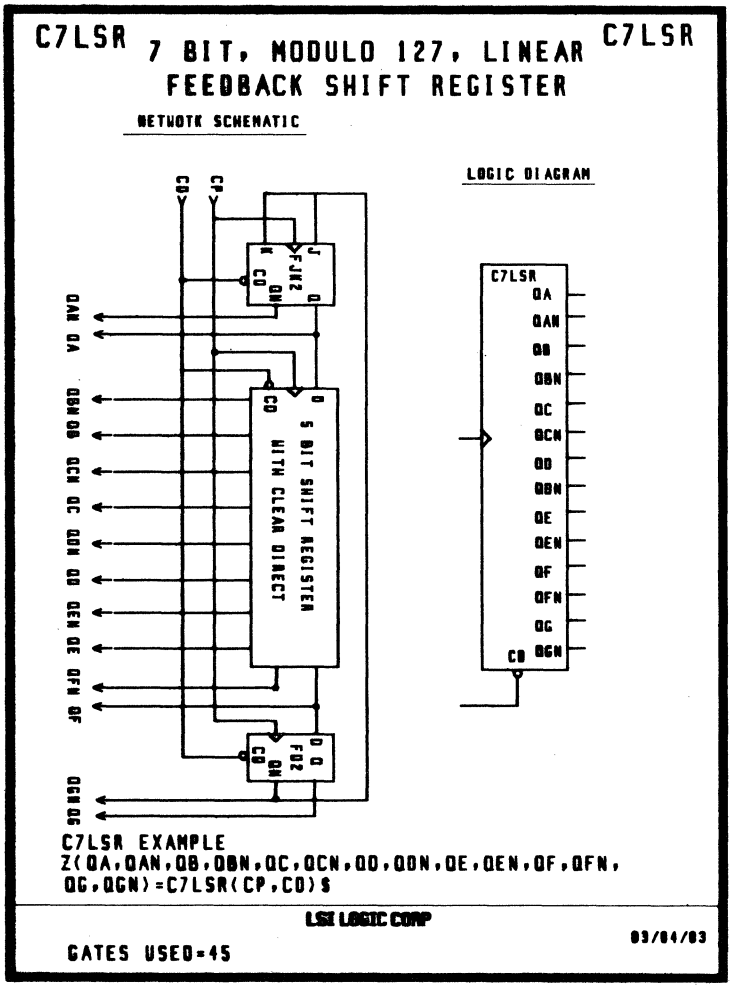
LOGIC DIAGRAM

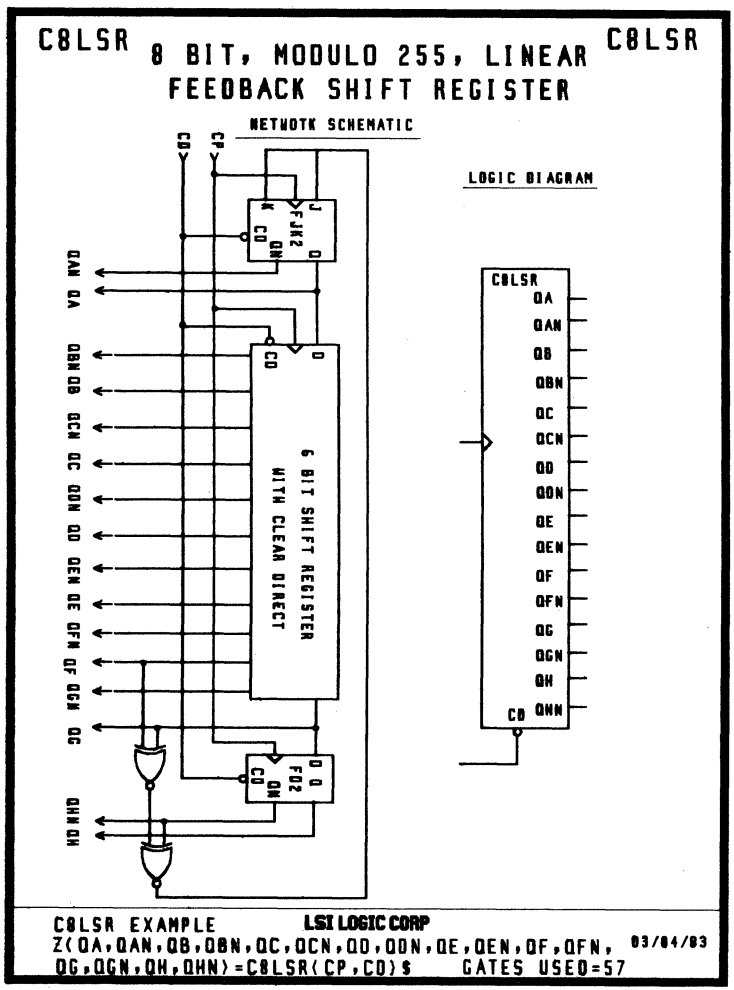


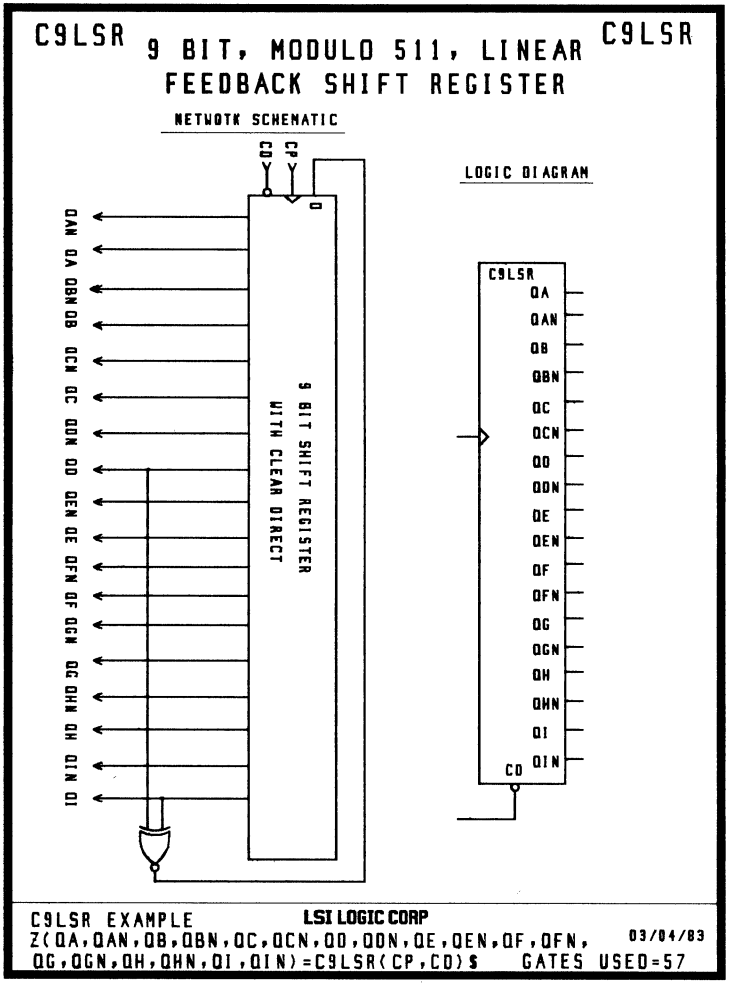
C6LSR EXAMPLE
Z(QA,QAN,QB,QBN,QC,QCN,QD,QDN,QE,QEN,QF,QFN)
=C6LSR(CP,CD)$

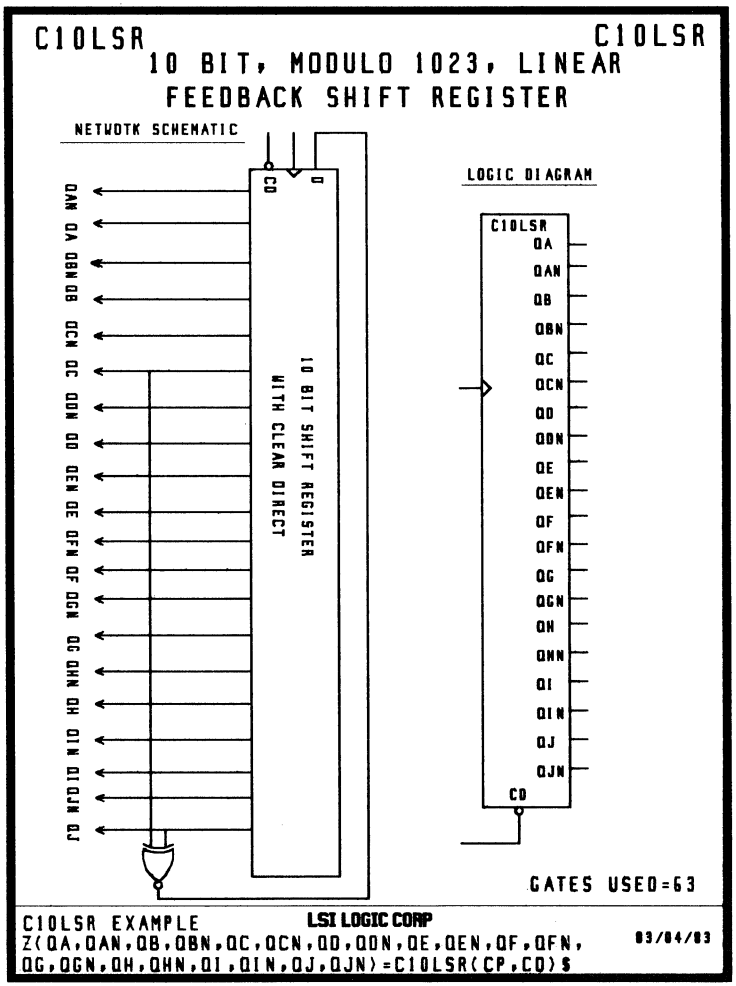
LSI LOGIC CORP
GATES USED=39

03/04/83


C7LSR
7 BIT, MODULO 127, LINEAR
FEEDBACK SHIFT REGISTER
C7LSR
NETWORK SCHEMATIC
LOGIC DIAGRAM
C7LSR
QA
QAN
QB
QBN
QC
QCN
QD
QDN
QE
QEN
QF
QFN
QG
QGN
CD
5 BIT SHIFT REGISTER
WITH CLEAR DIRECT
FJK2
FD2
C7LSR EXAMPLE
Z(QA,QAN,QB,QBN,QC,QCN,QD,QDN,QE,QEN,QF,QFN,
QG,QGN)=C7LSR(CP,CD)$
LSI LOGIC CORP
GATES USED=45
03/04/03

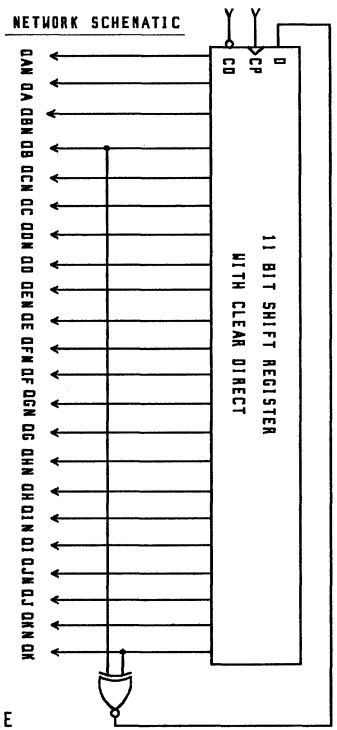

C8LSR
8 BIT, MODULO 255, LINEAR
FEEDBACK SHIFT REGISTER
C8LSR
NETWORK SCHEMATIC
LOGIC DIAGRAM
C8LSR
QA
QAN
QB
QBN
QC
QCN
QD
QDN
QE
QEN
QF
QFN
QG
QGN
QH
QHN
CD
6 BIT SHIFT REGISTER
WITH CLEAR DIRECT
FJK2
FD2
C8LSR EXAMPLE
Z(QA,QAN,QB,QBN,QC,QCN,QD,QDN,QE,QEN,QF,QFN,
QG,QGN,QH,QHN)=C8LSR(CP,CD)$
LSI LOGIC CORP
GATES USED=57
03/04/03


C9LSR
9 BIT, MODULO 511, LINEAR
FEEDBACK SHIFT REGISTER
C9LSR
NETWORK SCHEMATIC
LOGIC DIAGRAM
CD
CP
D
9 BIT SHIFT REGISTER
WITH CLEAR DIRECT
QA QAN QB QBN QC QCN QD QDN QE QEN QF QFN QG QGN QH QHN QI QIN
C9LSR
QA
QAN
QB
QBN
QC
QCN
QD
QDN
QE
QEN
QF
QFN
QG
QGN
QH
QHN
QI
QIN
CD
C9LSR EXAMPLE
LSI LOGIC CORP
Z(QA,QAN,QB,QBN,QC,QCN,QD,QDN,QE,QEN,QF,QFN,
QG,QGN,QH,QHN,QI,QIN)=C9LSR(CP,CD)$
GATES USED=57
03/04/83


C10LSR
10 BIT, MODULO 1023, LINEAR
FEEDBACK SHIFT REGISTER
C10LSR
NETWORK SCHEMATIC
LOGIC DIAGRAM
CD
D
10 BIT SHIFT REGISTER
WITH CLEAR DIRECT
QA QAN QB QBN QC QCN QD QDN QE QEN QF QFN QG QGN QH QHN QI QIN QJ QJN
C10LSR
QA
QAN
QB
QBN
QC
QCN
QD
QDN
QE
QEN
QF
QFN
QG
QGN
QH
QHN
QI
QIN
QJ
QJN
CD
GATES USED=63
C10LSR EXAMPLE
LSI LOGIC CORP
Z(QA,QAN,QB,QBN,QC,QCN,QD,QDN,QE,QEN,QF,QFN,
QG,QGN,QH,QHN,QI,QIN,QJ,QJN)=C10LSR(CP,CD)$
03/04/83

C11LSR C11LSR

11 BIT, MODULO 2047, LINEAR FEEDBACK SHIFT REGISTER



C11LSR EXAMPLE

Z(QA,QAN,QB,QBN,QC,QCN,QD,QDN,QE,QEN,QF,QFN,QG,QGN
QH,QHN,QI,QIN,QJ,QJN,QK,QKN)=C11LSR(CP,CD)$

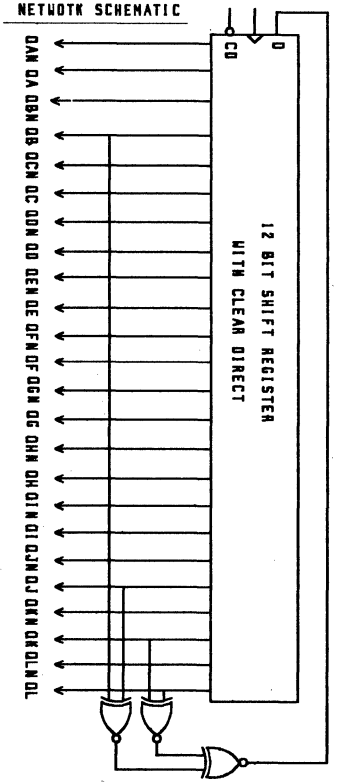
GATES USED=69

LSI LOGIC CORP

03/13/83

C12LSR C12LSR

12 BIT, MODULO 4095, LINEAR FEEDBACK SHIFT REGISTER



GATES USED=81

C12LSR EXAMPLE LSI LOGIC CORP 03/04/83

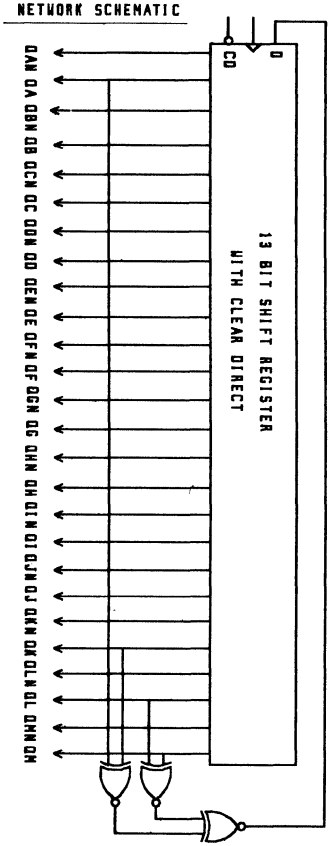
Z(QA,QAN,QB,QBN,QC,QCN,QD,QDN,QE,QEN,QF,QFN,QG,QGN,
QH,QHN,QI,QIN,QJ,QJN,QK,QKN,QL,QLN)=C12LSR(CP,CD)$

C13LSR

C13LSR

13 BIT
MODULO 8191
LINEAR FEEDBACK
SHIFT REGISTER

NETWORK SCHEMATIC



GATES USED=87

C13LSR EXAMPLE
Z(QA,QAN,QB,QBN,QC,QCN,QD,QDN,QE,QEN,QF,QFN,QG,QGN,QH,QHN,QI,QIN,QJ,QJN,QK,QKN,QL,QLN,QM,QMN)=C13LSR(CP,CD)$

LSI LOGIC CORP

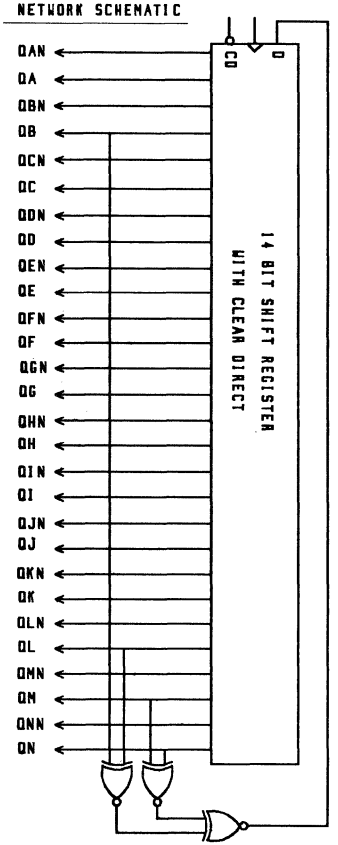
03/08/83

C14LSR

C14LSR

14 BIT
MODULO 16383
LINEAR FEEDBACK
SHIFT REGISTER

NETWORK SCHEMATIC

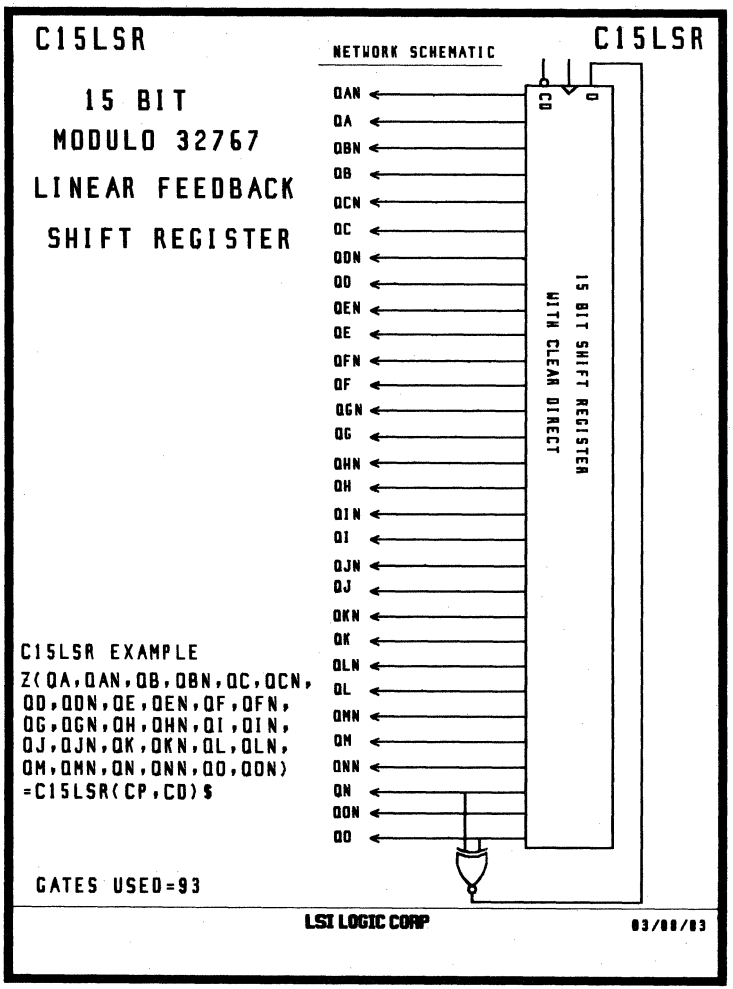


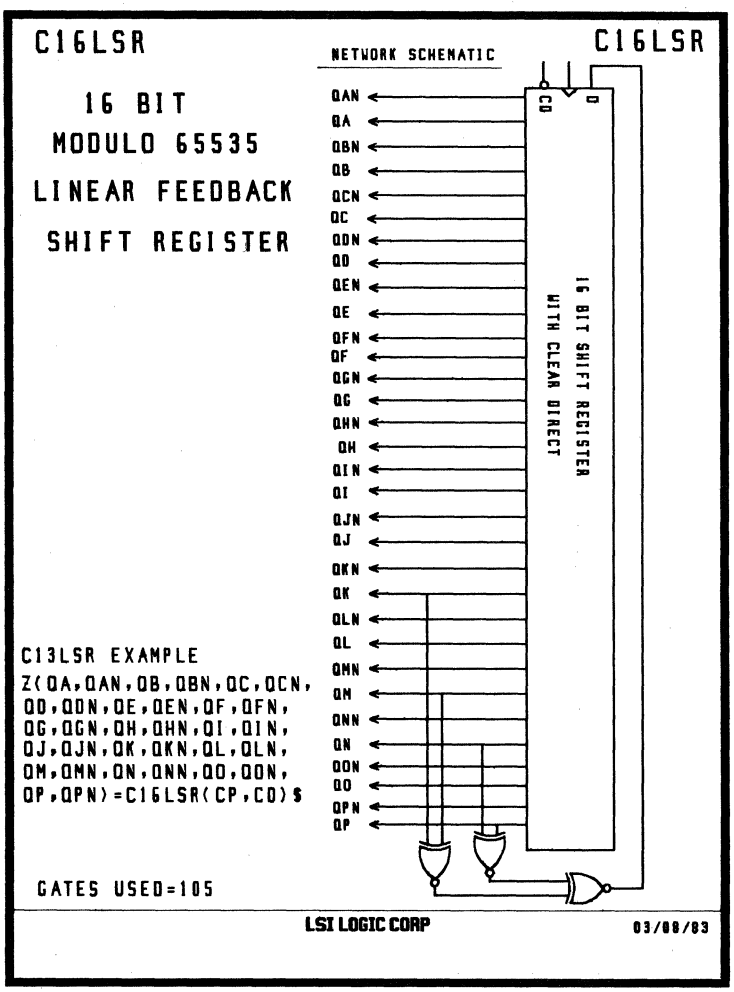
C14LSR EXAMPLE
Z(QA,QAN,QB,QBN,QC,QCN,QD,QDN,QE,QEN,QF,QFN,QG,QGN,QH,QHN,QI,QIN,QJ,QJN,QK,QKN,QL,QLN,QM,QMN,QN,QNN)=C14LSR(CP,CD)$

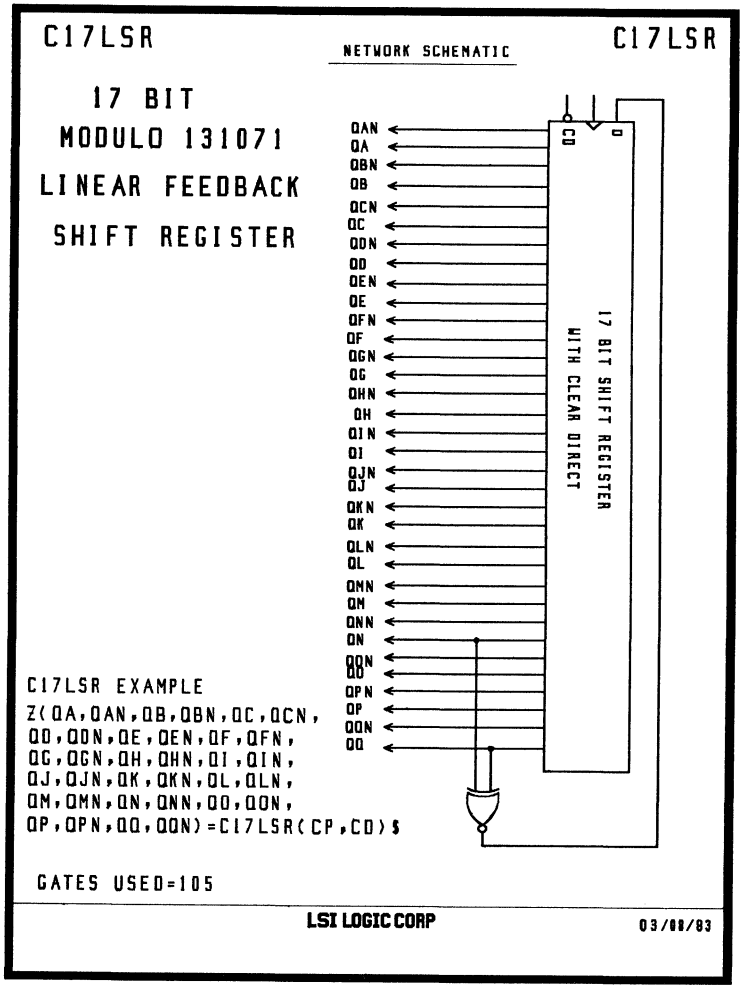
GATES USED=93

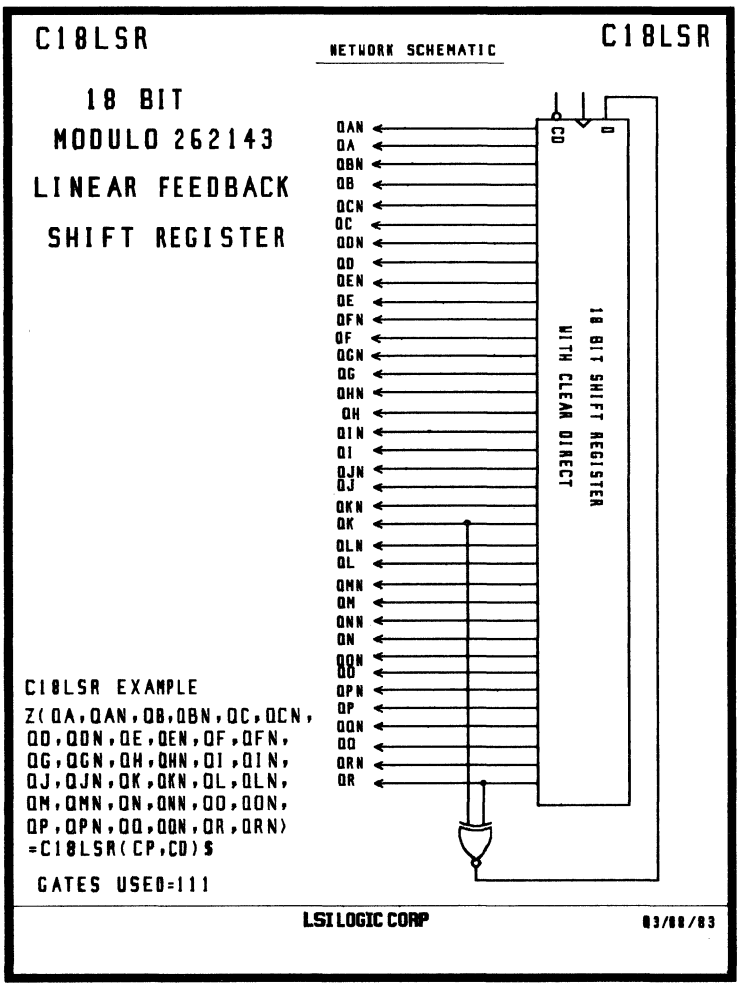
LSI LOGIC CORP

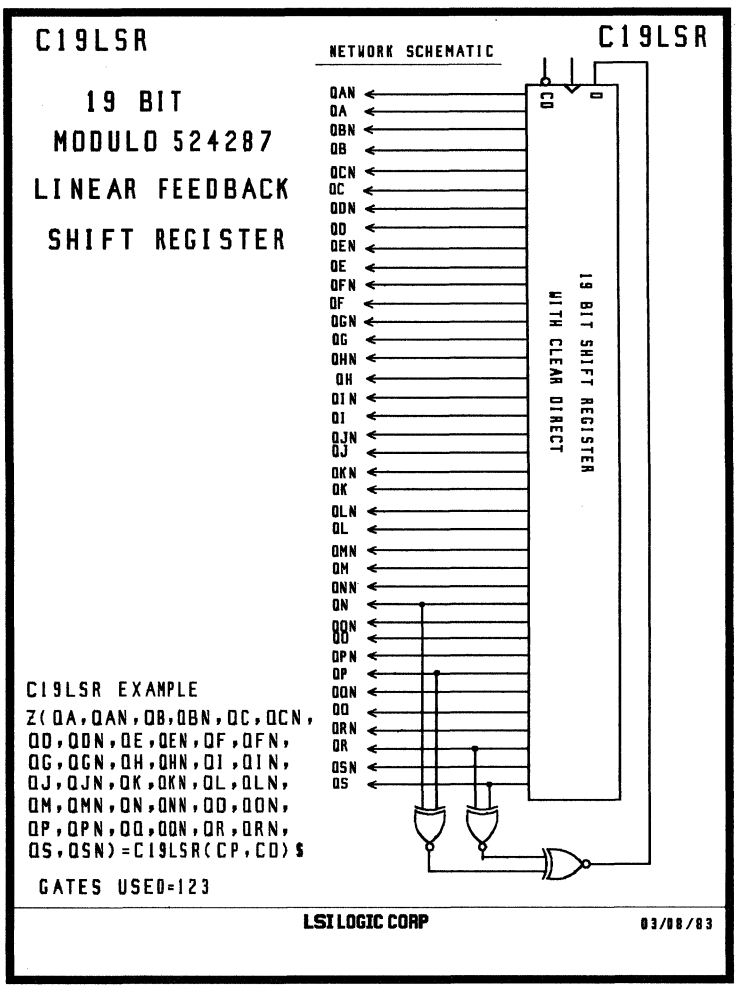
03/08/83

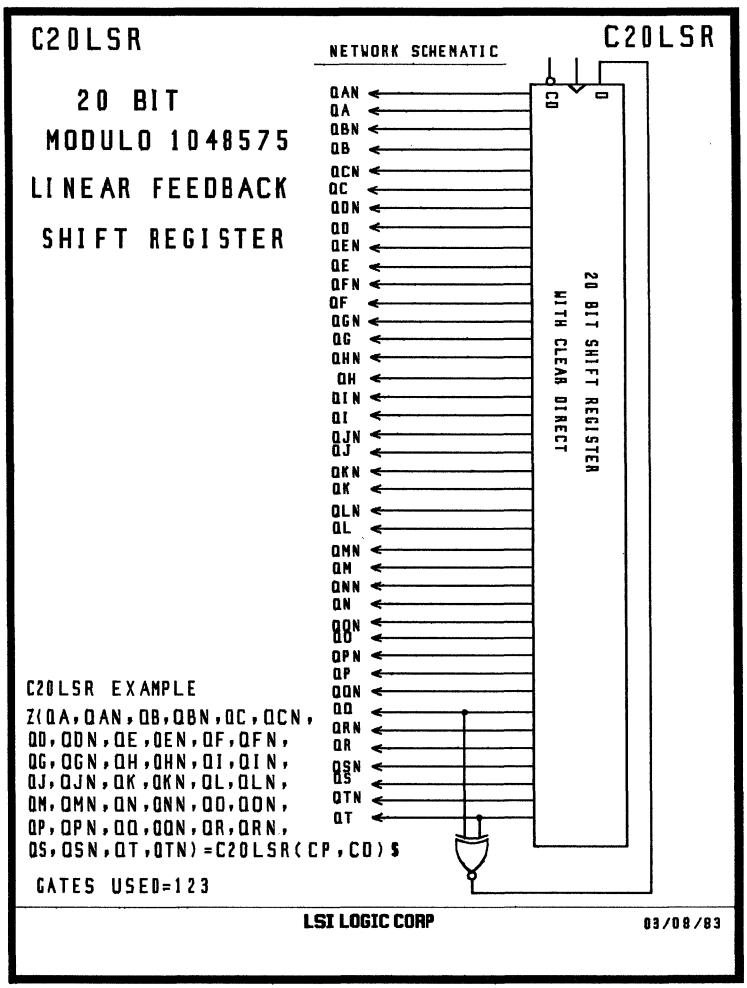

C15LSR
15 BIT
MODULO 32767
LINEAR FEEDBACK
SHIFT REGISTER
NETWORK SCHEMATIC
C15LSR
QAN
QA
QBN
QB
QCN
QC
QDN
QD
QEN
QE
QFN
QF
QGN
QG
QHN
QH
QIN
QI
QJN
QJ
QKN
QK
QLN
QL
QMN
QM
QNN
QN
QON
QO
CD
D
15 BIT SHIFT REGISTER
WITH CLEAR DIRECT
C15LSR EXAMPLE
Z(QA,QAN,QB,QBN,QC,QCN,
QD,QDN,QE,QEN,QF,QFN,
QG,QGN,QH,QHN,QI,QIN,
QJ,QJN,QK,QKN,QL,QLN,
QM,QMN,QN,QNN,QO,QON)
=C15LSR(CP,CD)$
GATES USED=93
LSI LOGIC CORP
03/08/03


C16LSR
16 BIT
MODULO 65535
LINEAR FEEDBACK
SHIFT REGISTER
NETWORK SCHEMATIC
C16LSR
QAN
QA
QBN
QB
QCN
QC
QDN
QD
QEN
QE
QFN
QF
QGN
QG
QHN
QH
QIN
QI
QJN
QJ
QKN
QK
QLN
QL
QMN
QM
QNN
QN
QON
QO
QPN
QP
CD
D
16 BIT SHIFT REGISTER
WITH CLEAR DIRECT
C13LSR EXAMPLE
Z(QA,QAN,QB,QBN,QC,QCN,
QD,QDN,QE,QEN,QF,QFN,
QG,QGN,QH,QHN,QI,QIN,
QJ,QJN,QK,QKN,QL,QLN,
QM,QMN,QN,QNN,QO,QON,
QP,QPN)=C16LSR(CP,CD)$
GATES USED=105
LSI LOGIC CORP
03/08/03


C17LSR
NETWORK SCHEMATIC
C17LSR
17 BIT
MODULO 131071
LINEAR FEEDBACK
SHIFT REGISTER
QAN
QA
QBN
QB
QCN
QC
QDN
QD
QEN
QE
QFN
QF
QGN
QG
QHN
QH
QIN
QI
QJN
QJ
QKN
QK
QLN
QL
QMN
QM
QNN
QN
QQN
QQ
QPN
QP
QQN
QQ
CD
D
17 BIT SHIFT REGISTER
WITH CLEAR DIRECT
C17LSR EXAMPLE
Z(QA,QAN,QB,QBN,QC,QCN,
QD,QDN,QE,QEN,QF,QFN,
QG,QGN,QH,QHN,QI,QIN,
QJ,QJN,QK,QKN,QL,QLN,
QM,QMN,QN,QNN,QQ,QQN,
QP,QPN,QQ,QQN)=C17LSR(CP,CD)$
GATES USED=105
LSI LOGIC CORP
03/08/83

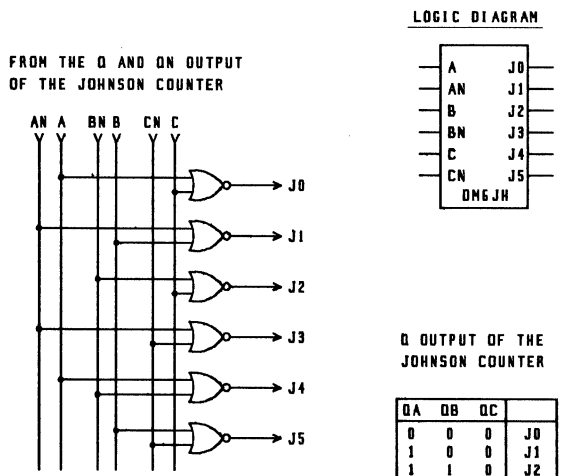

C18LSR
NETWORK SCHEMATIC
C18LSR
18 BIT
MODULO 262143
LINEAR FEEDBACK
SHIFT REGISTER
QAN
QA
QBN
QB
QCN
QC
QDN
QD
QEN
QE
QFN
QF
QGN
QG
QHN
QH
QIN
QI
QJN
QJ
QKN
QK
QLN
QL
QMN
QM
QNN
QN
QQN
QQ
QPN
QP
QQN
QQ
QRN
QR
CD
D
18 BIT SHIFT REGISTER
WITH CLEAR DIRECT
C18LSR EXAMPLE
Z(QA,QAN,QB,QBN,QC,QCN,
QD,QDN,QE,QEN,QF,QFN,
QG,QGN,QH,QHN,QI,QIN,
QJ,QJN,QK,QKN,QL,QLN,
QM,QMN,QN,QNN,QQ,QQN,
QP,QPN,QQ,QQN,QR,QRN)
=C18LSR(CP,CD)$
GATES USED=111
LSI LOGIC CORP
03/08/83


C19LSR
19 BIT
MODULO 524287
LINEAR FEEDBACK
SHIFT REGISTER
NETWORK SCHEMATIC
C19LSR
QAN
QA
QBN
QB
QCN
QC
QDN
QD
QEN
QE
QFN
QF
QGN
QG
QHN
QH
QIN
QI
QJN
QJ
QKN
QK
QLN
QL
QMN
QM
QNN
QN
QQN
QQ
QPN
QP
QQN
QQ
QRN
QR
QSN
QS
CD
D
19 BIT SHIFT REGISTER
WITH CLEAR DIRECT
C19LSR EXAMPLE
Z(QA,QAN,QB,QBN,QC,QCN,
QD,QDN,QE,QEN,QF,QFN,
QG,QGN,QH,QHN,QI,QIN,
QJ,QJN,QK,QKN,QL,QLN,
QM,QMN,QN,QNN,QQ,QQN,
QP,QPN,QQ,QQN,QR,QRN,
QS,QSN)=C19LSR(CP,CD)$
GATES USED=123
LSI LOGIC CORP
03/08/83


C20LSR
20 BIT
MODULO 1048575
LINEAR FEEDBACK
SHIFT REGISTER
NETWORK SCHEMATIC
C20LSR
QAN
QA
QBN
QB
QCN
QC
QDN
QD
QEN
QE
QFN
QF
QGN
QG
QHN
QH
QIN
QI
QJN
QJ
QKN
QK
QLN
QL
QMN
QM
QNN
QN
QQN
QQ
QPN
QP
QQN
QQ
QRN
QR
QSN
QS
QTN
QT
CD
D
20 BIT SHIFT REGISTER
WITH CLEAR DIRECT
C20LSR EXAMPLE
Z(QA,QAN,QB,QBN,QC,QCN,
QD,QDN,QE,QEN,QF,QFN,
QG,QGN,QH,QHN,QI,QIN,
QJ,QJN,QK,QKN,QL,QLN,
QM,QMN,QN,QNN,QQ,QQN,
QP,QPN,QQ,QQN,QR,QRN,
QS,QSN,QT,QTN)=C20LSR(CP,CD)$
GATES USED=123
LSI LOGIC CORP
03/08/83

DM6JH

SPIKE FREE DECODER FOR MOD 6 JOHNSON COUNTER, ACTIVE HI, SEE CM6J



Q OUTPUT OF THE JOHNSON COUNTER

QA	QB	QC	
0	0	0	J0
1	0	0	J1
1	1	0	J2
1	1	1	J3
0	1	1	J4
0	0	1	J5

DM6JH EXAMPLE

```
Z(J0,J1,J2,J3,J4,J5)=DM6JH(A,AN,B,BN,C,CN)$
```

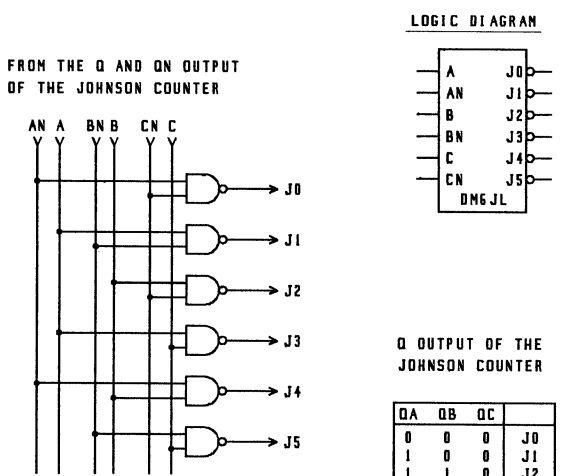
LSI LOGIC CORP

GATES USED = 6

03/14/83

DM6JL

SPIKE FREE DECODER FOR MOD 6 JOHNSON COUNTER, ACTIVE LO, SEE CM6J



Q OUTPUT OF THE JOHNSON COUNTER

QA	QB	QC	
0	0	0	J0
1	0	0	J1
1	1	0	J2
1	1	1	J3
0	1	1	J4
0	0	1	J5

DM6JL EXAMPLE

```
Z(J0,J1,J2,J3,J4,J5)=DM6JL(A,AN,B,BN,C,CN)$
```

LSI LOGIC CORP

GATES USED = 6

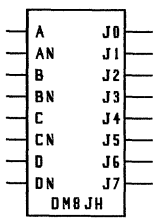
03/14/83

DM8JH

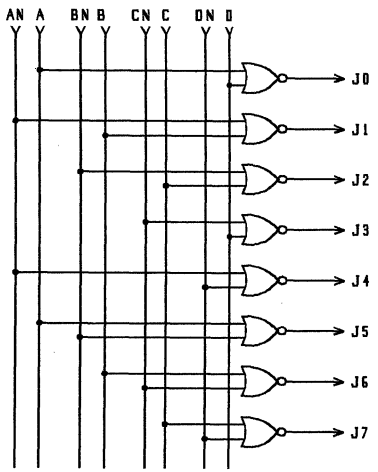
SPIKE FREE DECODER FOR MOD 8 JOHNSON COUNTER, ACTIVE HI, SEE CM8J

DM8JH

LOGIC DIAGRAM



FROM THE Q AND QN OUTPUT OF THE JOHNSON COUNTER



Q OUTPUT OF THE JOHNSON COUNTER

QA	QB	QC	QD	
0	0	0	0	J0
1	0	0	0	J1
1	1	0	0	J2
1	1	1	0	J3
1	1	1	1	J4
0	1	1	1	J5
0	0	1	1	J6
0	0	0	1	J7

DM8JH EXAMPLE

Z(J0,J1,J2,J3,J4,J5,J6,J7)=DM8JH(A,AN,B,BN,C,CN,D,DN)$

LSI LOGIC CORP

GATES USED = 8

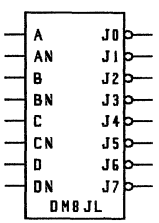
05/11/83

DM8JL

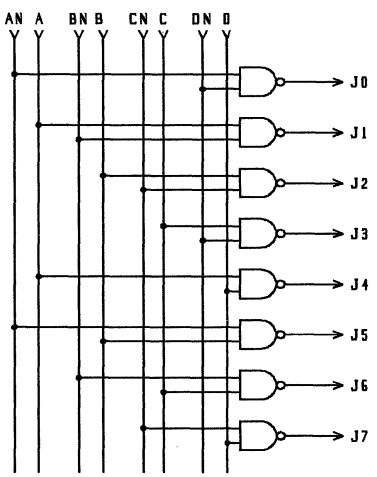
SPIKE FREE DECODER FOR MOD 8 JOHNSON COUNTER, ACTIVE LO, SEE CM8J

DM8JL

LOGIC DIAGRAM



FROM THE Q AND QN OUTPUT OF THE JOHNSON COUNTER



Q OUTPUT OF THE JOHNSON COUNTER

QA	QB	QC	QD	
0	0	0	0	J0
1	0	0	0	J1
1	1	0	0	J2
1	1	1	0	J3
1	1	1	1	J4
0	1	1	1	J5
0	0	1	1	J6
0	0	0	1	J7

DM8JL EXAMPLE

Z(J0,J1,J2,J3,J4,J5,J6,J7)=DM8JL(A,AN,B,BN,C,CN,D,DN)$

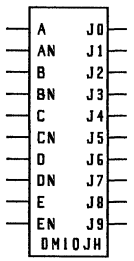
LSI LOGIC CORP

GATES USED = 8

05/11/83

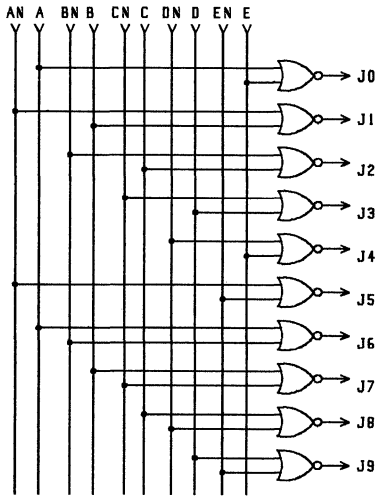
DM10JH SPIKE FREE DECODER DM10JH
FOR MOD 10 JOHNSON COUNTER, ACTIVE HI, SEE CM10J

LOGIC DIAGRAM



NETWORK SCHEMATIC

FROM THE Q AND QN OUTPUT OF THE JOHNSON COUNTER



Q OUTPUT OF THE JOHNSON COUNTER

QA	QB	QC	QD	QE	
0	0	0	0	0	J0
1	0	0	0	0	J1
1	1	0	0	0	J2
1	1	1	0	0	J3
1	1	1	1	0	J4
1	1	1	1	1	J5
0	1	1	1	1	J6
0	0	1	1	1	J7
0	0	0	1	1	J8
0	0	0	0	1	J9

DM10JH EXAMPLE **LSI LOGIC CORP**

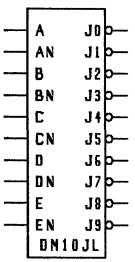
Z(J0,J1,J2,J3,J4,J5,J6,J7,J8,J9)
=DM10JH(A,AN,B,BN,C,CN,D,DN,E,EN)$

03/17/83

GATES USED = 10

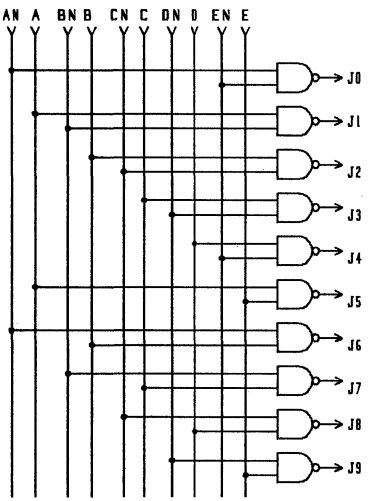
DM10JL SPIKE FREE DECODER DM10JL
FOR MOD 10 JOHNSON COUNTER, ACTIVE LO, SEE CM10J

LOGIC DIAGRAM



NETWORK SCHEMATIC

FROM THE Q AND QN OUTPUT OF THE JOHNSON COUNTER



Q OUTPUT OF THE JOHNSON COUNTER

QA	QB	QC	QD	QE	
0	0	0	0	0	J0
1	0	0	0	0	J1
1	1	0	0	0	J2
1	1	1	0	0	J3
1	1	1	1	0	J4
1	1	1	1	1	J5
0	1	1	1	1	J6
0	0	1	1	1	J7
0	0	0	1	1	J8
0	0	0	0	1	J9

DM10JL EXAMPLE **LSI LOGIC CORP**

Z(J0,J1,J2,J3,J4,J5,J6,J7,J8,J9)
=DM10JL(A,AN,B,BN,C,CN,D,DN,E,EN)$

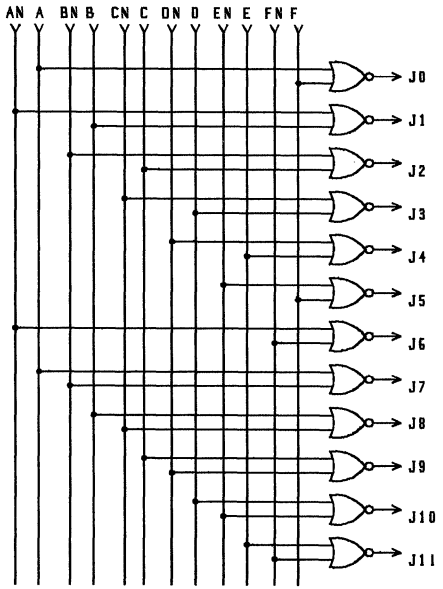
03/17/83

GATES USED = 10

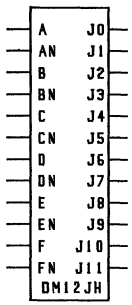
DM12JH SPIKE FREE DECODER DM12JH FOR MOD 12 JOHNSON COUNTER, ACTIVE HI, SEE CM12J

NETWORK SCHEMATIC

FROM THE Q AND QN OUTPUT OF THE JOHNSON COUNTER



LOGIC DIAGRAM



Q OUTPUT OF THE JOHNSON COUNTER

QA	QB	QC	QD	QE	QF	
0	0	0	0	0	0	J0
1	0	0	0	0	0	J1
1	1	0	0	0	0	J2
1	1	1	0	0	0	J3
1	1	1	1	0	0	J4
1	1	1	1	1	0	J5
1	1	1	1	1	1	J6
0	1	1	1	1	1	J7
0	0	1	1	1	1	J8
0	0	0	1	1	1	J9
0	0	0	0	1	1	J10
0	0	0	0	0	1	J11

DM12JH EXAMPLE **LSI LOGIC CORP**

Z(J0,J1,J2,J3,J4,J5,J6,J7,J8,J9,J10,J11)
=DM12JH(A,AN,B,BN,C,CN,D,DN,E,EN,F,FN)$

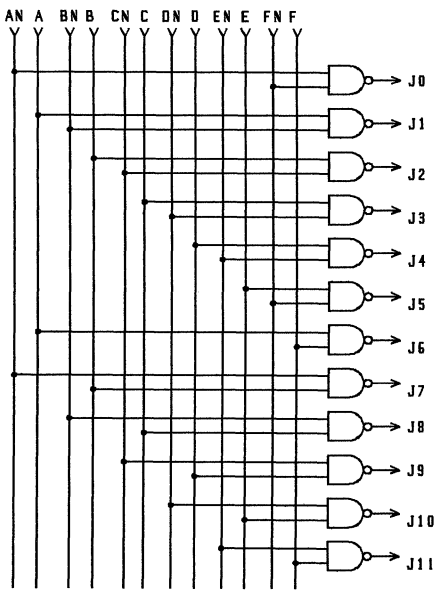
03/17/83

GATES USED = 12

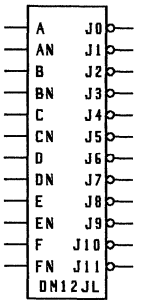
DM12JL SPIKE FREE DECODER DM12JL FOR MOD 12 JOHNSON COUNTER, ACTIVE LO, SEE CM12J

NETWORK SCHEMATIC

FROM THE Q AND QN OUTPUT OF THE JOHNSON COUNTER



LOGIC DIAGRAM



Q OUTPUT OF THE JOHNSON COUNTER

QA	QB	QC	QD	QE	QF	
0	0	0	0	0	0	J0
1	0	0	0	0	0	J1
1	1	0	0	0	0	J2
1	1	1	0	0	0	J3
1	1	1	1	0	0	J4
1	1	1	1	1	0	J5
1	1	1	1	1	1	J6
0	1	1	1	1	1	J7
0	0	1	1	1	1	J8
0	0	0	1	1	1	J9
0	0	0	0	1	1	J10
0	0	0	0	0	1	J11

DM12JL EXAMPLE **LSI LOGIC CORP**

Z(J0,J1,J2,J3,J4,J5,J6,J7,J8,J9,J10,J11)
=DM12JL(A,AN,B,BN,C,CN,D,DN,E,EN,F,FN)$

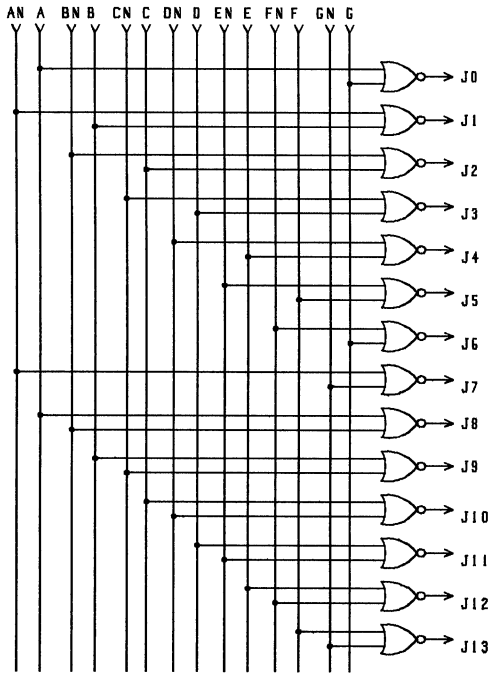
03/17/83

GATES USED = 12

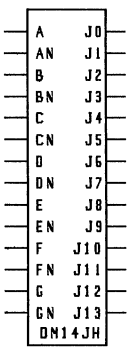
DM14JH SPIKE FREE DECODER DM14JH
FOR MOD 14 JOHNSON COUNTER, ACTIVE HI, SEE CM14J

NETWORK SCHEMATIC

FROM THE Q AND QN OUTPUT OF THE JOHNSON COUNTER



LOGIC DIAGRAM



DM14JH EXAMPLE

LSI LOGIC CORP

Z(J0,J1,J2,J3,J4,J5,J6,J7,J8,J9,J10,J11,J12,J13)
=DM14JH(A,AN,B,BN,C,CN,D,DN,E,EN,F,FN,G,GN)$

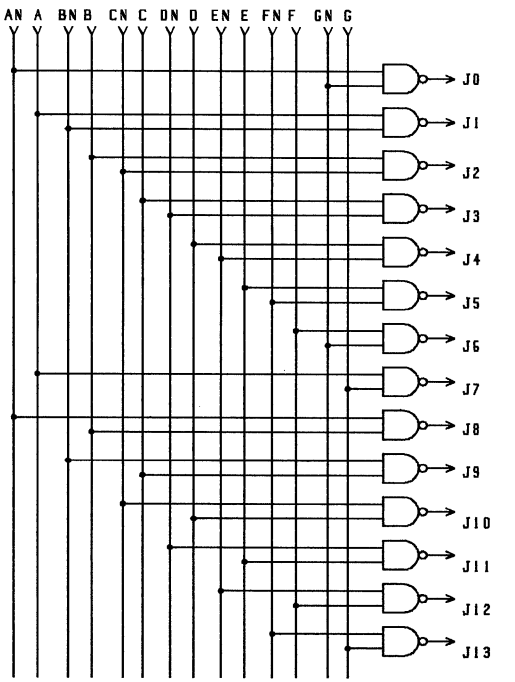
03/17/83

GATES USED = 14

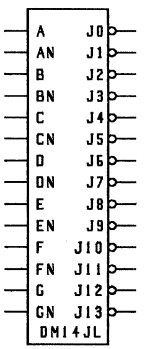
DM14JL SPIKE FREE DECODER DM14JL
FOR MOD 14 JOHNSON COUNTER, ACTIVE LO, SEE CM14J

NETWORK SCHEMATIC

FROM THE Q AND QN OUTPUT OF THE JOHNSON COUNTER



LOGIC DIAGRAM



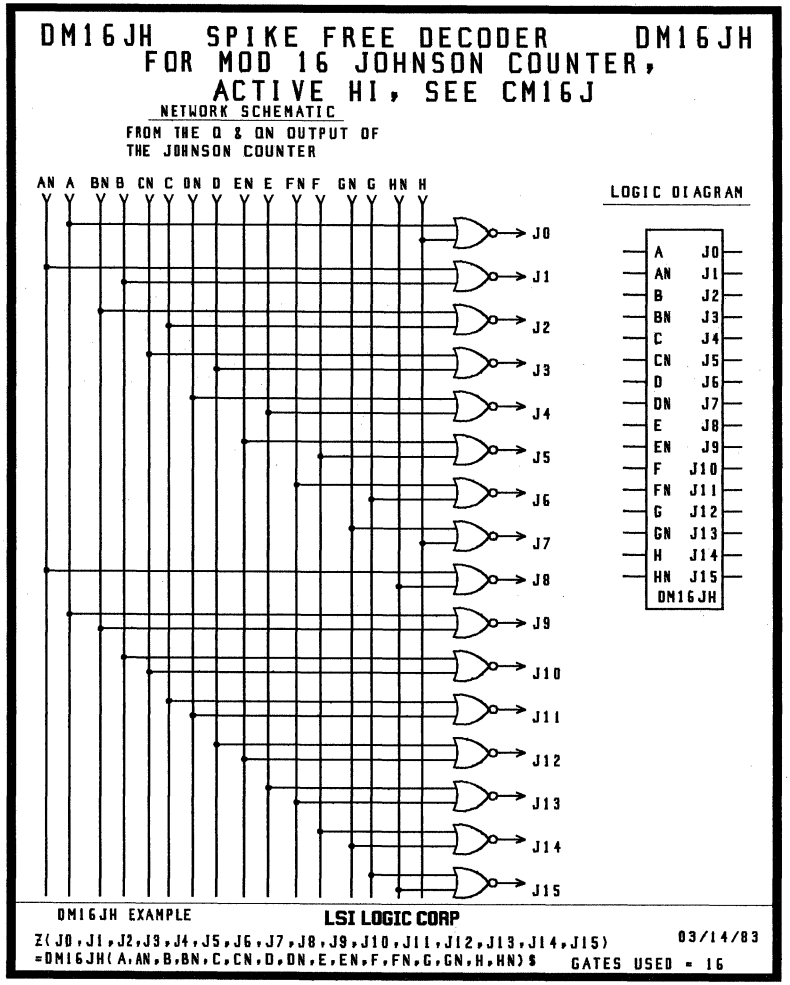
DM14JL EXAMPLE

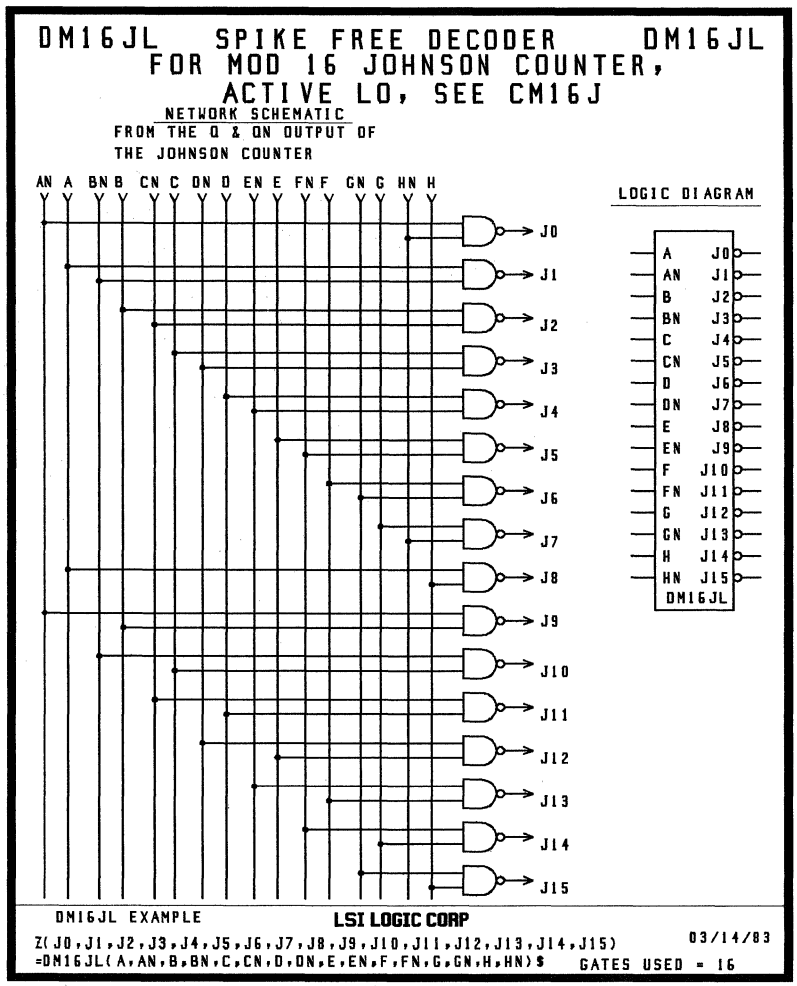
LSI LOGIC CORP

Z(J0,J1,J2,J3,J4,J5,J6,J7,J8,J9,J10,J11,J12,J13)
=DM14JL(A,AN,B,BN,C,CN,D,DN,E,EN,F,FN,G,GN)$

03/14/83

GATES USED = 14

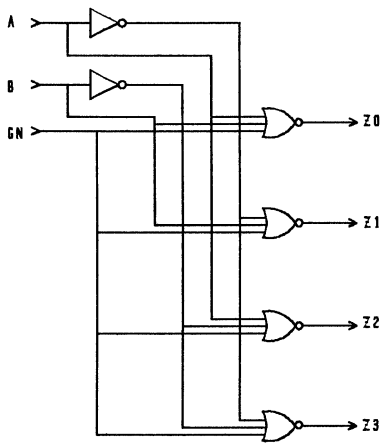

DM16JH SPIKE FREE DECODER DM16JH
FOR MOD 16 JOHNSON COUNTER,
ACTIVE HI, SEE CM16J
NETWORK SCHEMATIC
FROM THE Q & QN OUTPUT OF
THE JOHNSON COUNTER
AN A BN B CN C DN D EN E FN F GN G HN H
J0
J1
J2
J3
J4
J5
J6
J7
J8
J9
J10
J11
J12
J13
J14
J15
LOGIC DIAGRAM
A J0
AN J1
B J2
BN J3
C J4
CN J5
D J6
DN J7
E J8
EN J9
F J10
FN J11
G J12
GN J13
H J14
HN J15
DM16JH
DM16JH EXAMPLE
LSI LOGIC CORP
Z(J0,J1,J2,J3,J4,J5,J6,J7,J8,J9,J10,J11,J12,J13,J14,J15)
=DM16JH(A,AN,B,BN,C,CN,D,DN,E,EN,F,FN,G,GN,H,HN)$
03/14/83
GATES USED = 16


DM16JL SPIKE FREE DECODER DM16JL
FOR MOD 16 JOHNSON COUNTER,
ACTIVE LO, SEE CM16J
NETWORK SCHEMATIC
FROM THE Q & QN OUTPUT OF
THE JOHNSON COUNTER
AN A BN B CN C DN D EN E FN F GN G HN H
J0
J1
J2
J3
J4
J5
J6
J7
J8
J9
J10
J11
J12
J13
J14
J15
LOGIC DIAGRAM
A J0
AN J1
B J2
BN J3
C J4
CN J5
D J6
DN J7
E J8
EN J9
F J10
FN J11
G J12
GN J13
H J14
HN J15
DM16JL
DM16JL EXAMPLE
LSI LOGIC CORP
Z(J0,J1,J2,J3,J4,J5,J6,J7,J8,J9,J10,J11,J12,J13,J14,J15)
=DM16JL(A,AN,B,BN,C,CN,D,DN,E,EN,F,FN,G,GN,H,HN)$
03/14/83
GATES USED = 16

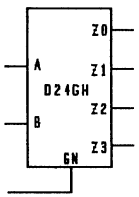
D24GH D24GH

2 TO 4 DECODER,GATED OUTPUTS ACTIVE HI

NETWORK SCHEMATIC



LOGIC DIAGRAM



TRUTH TABLE

A	B	GN	Z0	Z1	Z2	Z3
0	0	0	1	0	0	0
1	0	0	0	1	0	0
0	1	0	0	0	1	0
1	1	0	0	0	0	1
X	X	1	0	0	0	0

D24GH EXAMPLE

Z(Z0,Z1,Z2,Z3) = D24GH(A,B,GN)$

LSI LOGIC CORP

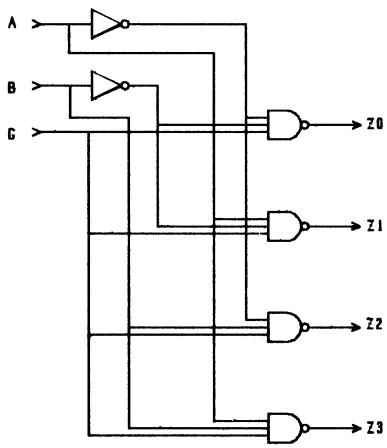
GATES USED = 10

02/04/83

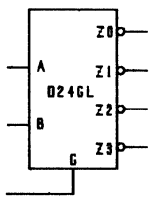
D24GL D24GL

2 TO 4 DECODER,GATES OUTPUTS ACTIVE LO

NETWORK SCHEMATIC



LOGIC DIAGRAM



TRUTH TABLE

A	B	C	Z0	Z1	Z2	Z3
0	0	1	0	1	1	1
1	0	1	1	0	1	1
0	1	1	1	1	0	1
1	1	1	1	1	1	0
X	X	0	1	1	1	1

D24GL EXAMPLE

Z(Z0,Z1,Z2,Z3) = D24GL(A,B,C)$

LSI LOGIC CORP

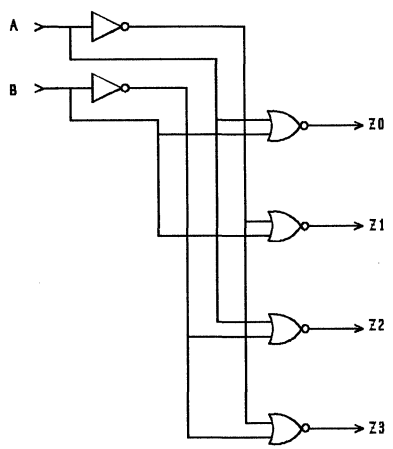
GATES USED = 10

03/11/83

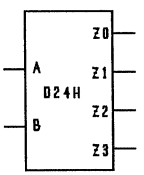
D24H D24H

2 TO 4 DECODER, OUTPUTS ACTIVE HI

NETWORK SCHEMATIC



LOGIC DIAGRAM



TRUTH TABLE

A	B	Z0	Z1	Z2	Z3
0	0	1	0	0	0
1	0	0	1	0	0
0	1	0	0	1	0
1	1	0	0	0	1

D24H EXAMPLE

Z(Z0,Z1,Z2,Z3) = D24H(A,B)$

LSI LOGIC CORP

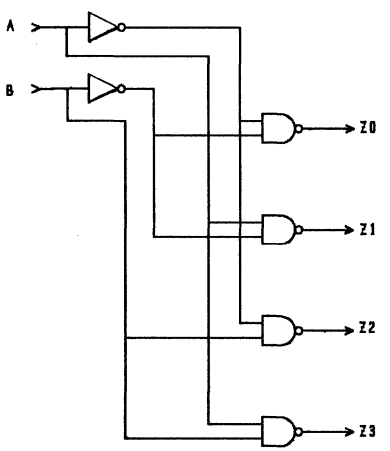
GATES USED = 6

02/04/83

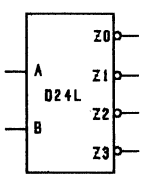
D24L D24L

2 TO 4 DECODER, OUTPUTS ACTIVE LO

NETWORK SCHEMATIC



LOGIC DIAGRAM



TRUTH TABLE

A	B	Z0	Z1	Z2	Z3
0	0	0	1	1	1
1	0	1	0	1	1
0	1	1	1	0	1
1	1	1	1	1	0

D24L EXAMPLE

Z(Z0,Z1,Z2,Z3) = D24L(A,B)$

LSI LOGIC CORP

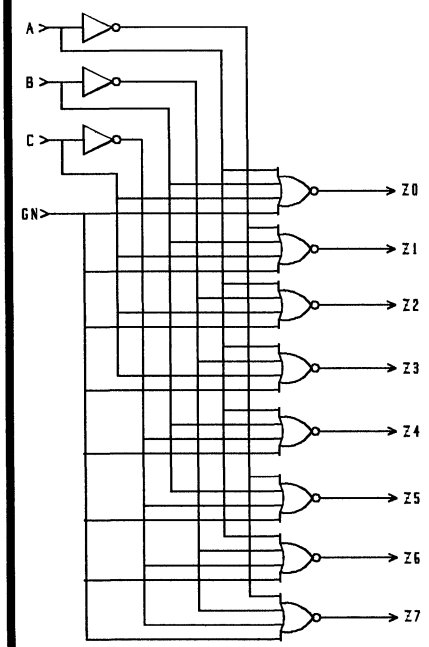
GATES USED = 6

02/04/83

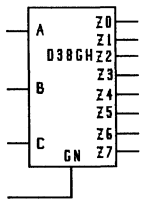
D38GH D38GH

3 TO 8 DECODER,GATED OUTPUTS ACTIVE HI

NETWORK SCHEMATIC



LOGIC DIAGRAM



TRUTH TABLE

A	B	C	GN	0	1	2	3	4	5	6	7
0	0	0	0	1	0	0	0	0	0	0	0
1	0	0	0	0	1	0	0	0	0	0	0
0	1	0	0	0	0	1	0	0	0	0	0
1	1	0	0	0	0	0	1	0	0	0	0
0	0	1	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	0	1	0	0
0	1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	0	1
X	X	X	1	0	0	0	0	0	0	0	0

D38GH EXAMPLE

Z(Z0,Z1,Z2,Z3,Z4,Z5,Z6,Z7) = D38GH(A,B,C,GN)$

LSI LOGIC CORP

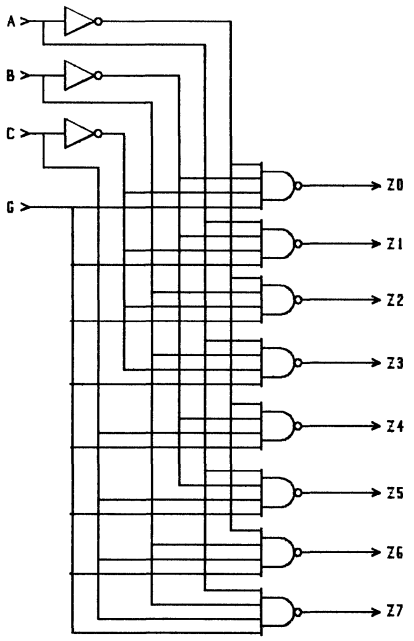
GATES USED = 19

02/04/83

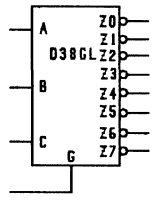
D38GL D38GL

3 TO 8 DECODER,GATED OUTPUTS ACTIVE LO

NETWORK SCHEMATIC



LOGIC DIAGRAM



TRUTH TABLE

A	B	C	G	0	1	2	3	4	5	6	7
0	0	0	1	0	1	1	1	1	1	1	1
1	0	0	1	1	0	1	1	1	1	1	1
0	1	0	1	1	1	0	1	1	1	1	1
1	1	0	1	1	1	1	0	1	1	1	1
0	0	1	1	1	1	1	1	0	1	1	1
1	0	1	1	1	1	1	1	1	0	1	1
0	1	1	1	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	1	1	0
X	X	X	0	1	1	1	1	1	1	1	1

D38GL EXAMPLE

Z(Z0,Z1,Z2,Z3,Z4,Z5,Z6,Z7) = D38GL(A,B,C,G)$

LSI LOGIC CORP

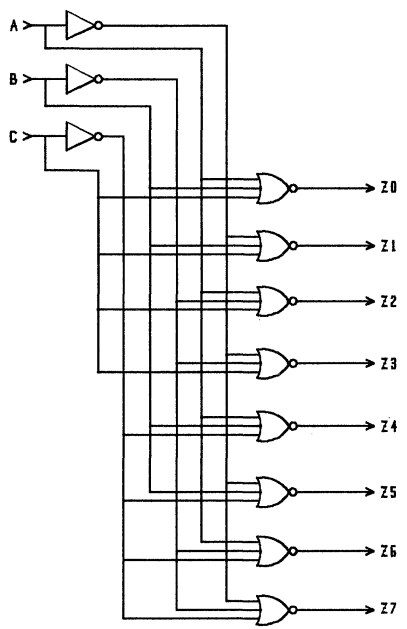
GATES USED = 19

03/11/83

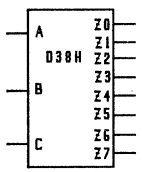
D38H D38H

3 TO 4 DECODER, OUTPUTS ACTIVE HI

NETWORK SCHEMATIC



LOGIC DIAGRAM



TRUTH TABLE

A	B	C	0	1	2	3	4	5	6	7
0	0	0	1	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
1	1	0	0	0	0	1	0	0	0	0
0	0	1	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
0	1	1	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

D38H EXAMPLE

Z(Z0,Z1,Z2,Z3,Z4,Z5,Z6,Z7) = D38H(A,B,C)$

LSI LOGIC CORP

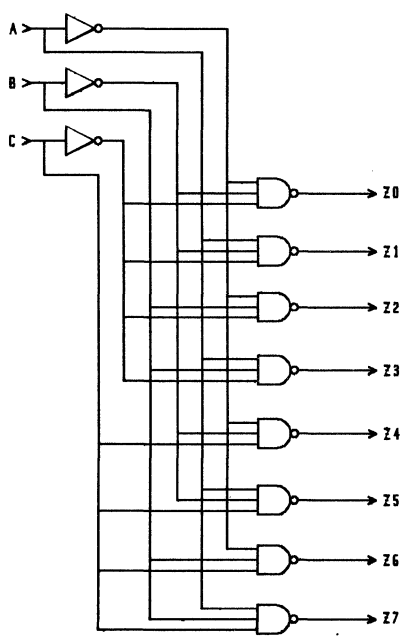
GATES USED = 19

04/18/84

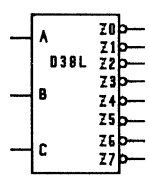
D38L D38L

3 TO 8 DECODER, OUTPUTS ACTIVE LO

NETWORK SCHEMATIC



LOGIC DIAGRAM



TRUTH TABLE

A	B	C	0	1	2	3	4	5	6	7
0	0	0	0	1	1	1	1	1	1	1
1	0	0	1	0	1	1	1	1	1	1
0	1	0	1	1	0	1	1	1	1	1
1	1	0	1	1	1	0	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1
1	0	1	1	1	1	1	1	0	1	1
0	1	1	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	1	0

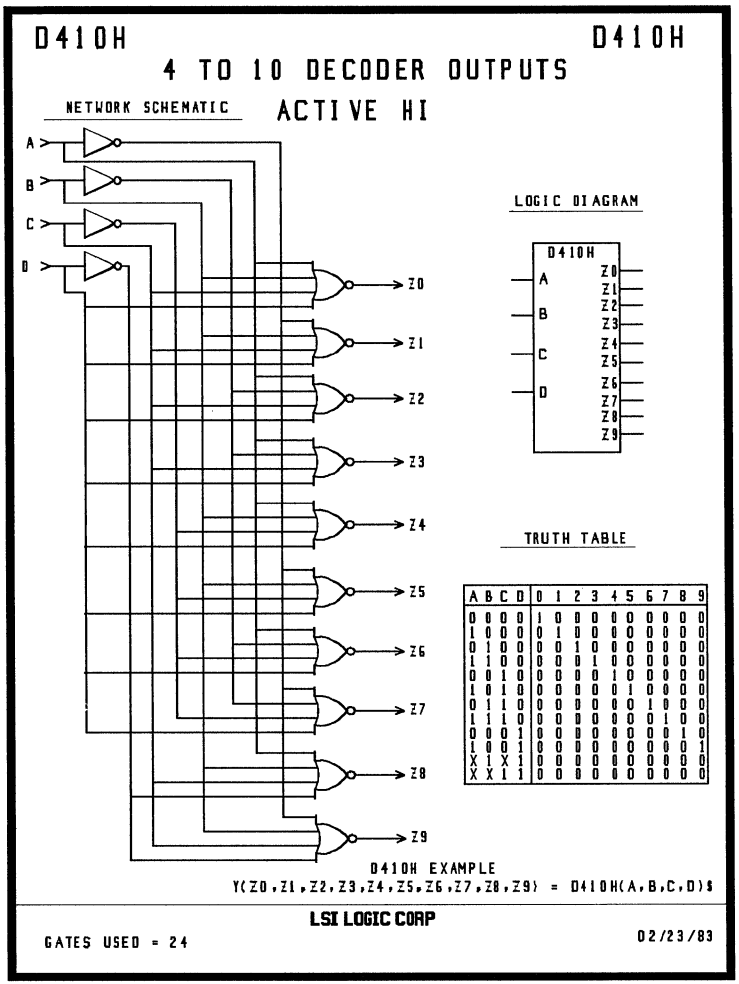
D38L EXAMPLE

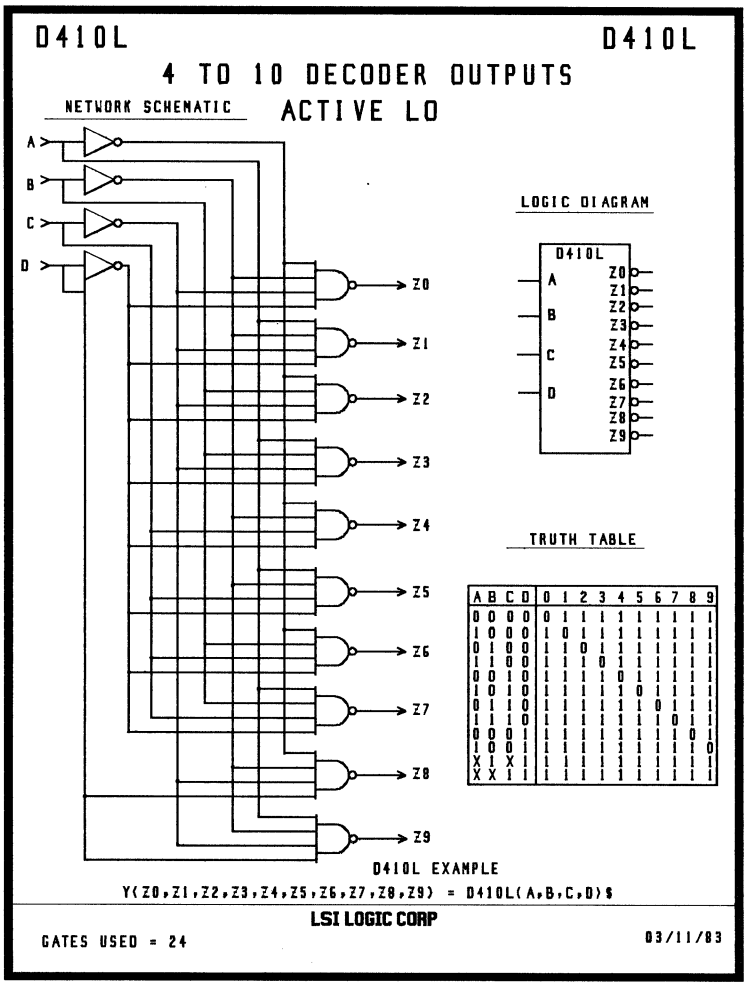
Z(Z0,Z1,Z2,Z3,Z4,Z5,Z6,Z7) = D38L(A,B,C)$

LSI LOGIC CORP

GATES USED = 19

02/04/83


D410H
D410H
4 TO 10 DECODER OUTPUTS
NETWORK SCHEMATIC
ACTIVE HI
A
B
C
D
Z0
Z1
Z2
Z3
Z4
Z5
Z6
Z7
Z8
Z9
LOGIC DIAGRAM
D410H
TRUTH TABLE
A B C D | 0 1 2 3 4 5 6 7 8 9
D410H EXAMPLE
Y(Z0,Z1,Z2,Z3,Z4,Z5,Z6,Z7,Z8,Z9) = D410H(A,B,C,D)$
LSI LOGIC CORP
GATES USED = 24
02/23/83

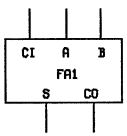

D410L
D410L
4 TO 10 DECODER OUTPUTS
NETWORK SCHEMATIC
ACTIVE LO
A
B
C
D
Z0
Z1
Z2
Z3
Z4
Z5
Z6
Z7
Z8
Z9
LOGIC DIAGRAM
D410L
TRUTH TABLE
A B C D | 0 1 2 3 4 5 6 7 8 9
D410L EXAMPLE
Y(Z0,Z1,Z2,Z3,Z4,Z5,Z6,Z7,Z8,Z9) = D410L(A,B,C,D)$
LSI LOGIC CORP
GATES USED = 24
03/11/83

FA1

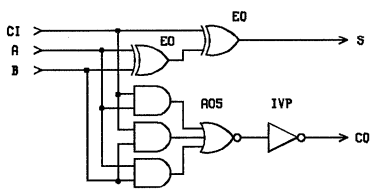
FULL ADDER

FA1

LOGIC DIAGRAM



NETWORK SCHEMATIC



TRUTH TABLE

CI A B	S CO
0 0 0	0 0
1 0 0	1 0
0 1 0	1 0
1 1 0	0 1
0 0 1	1 0
1 0 1	0 1
0 1 1	0 1
1 1 1	1 1

FA1 EXAMPLE

Z(S,CO) = FA1(CI,A,B)$

WORKSTATION WC. DELAY
(RISE/FALL) DAISY ∩ MENTOR = / VALID =

LSI LOGIC CORP

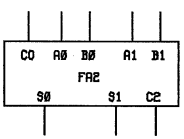
GATES USED = 10
02/02/83

FA2

2 BIT BINARY FULL ADDER
(SAME AS M82C)

FA2

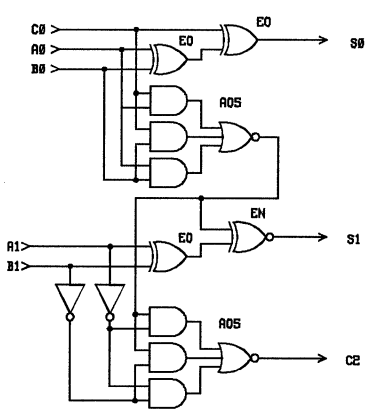
LOGIC DIAGRAM



TRUTH TABLE

C0 A0 B0	A1 B1	S0 S1 C2
0 OF 3	0 OF 2	0 0 0
1 OF 3	0 OF 2	1 0 0
2 OF 3	0 OF 2	0 1 0
3 OF 3	0 OF 2	1 1 0
0 OF 3	1 OF 2	0 1 0
1 OF 3	1 OF 2	1 1 0
2 OF 3	1 OF 2	0 0 1
3 OF 3	1 OF 2	1 0 1
0 OF 3	2 OF 2	0 0 1
1 OF 3	2 OF 2	1 0 1
2 OF 3	2 OF 2	0 1 1
3 OF 3	2 OF 2	1 1 1

NETWORK SCHEMATIC



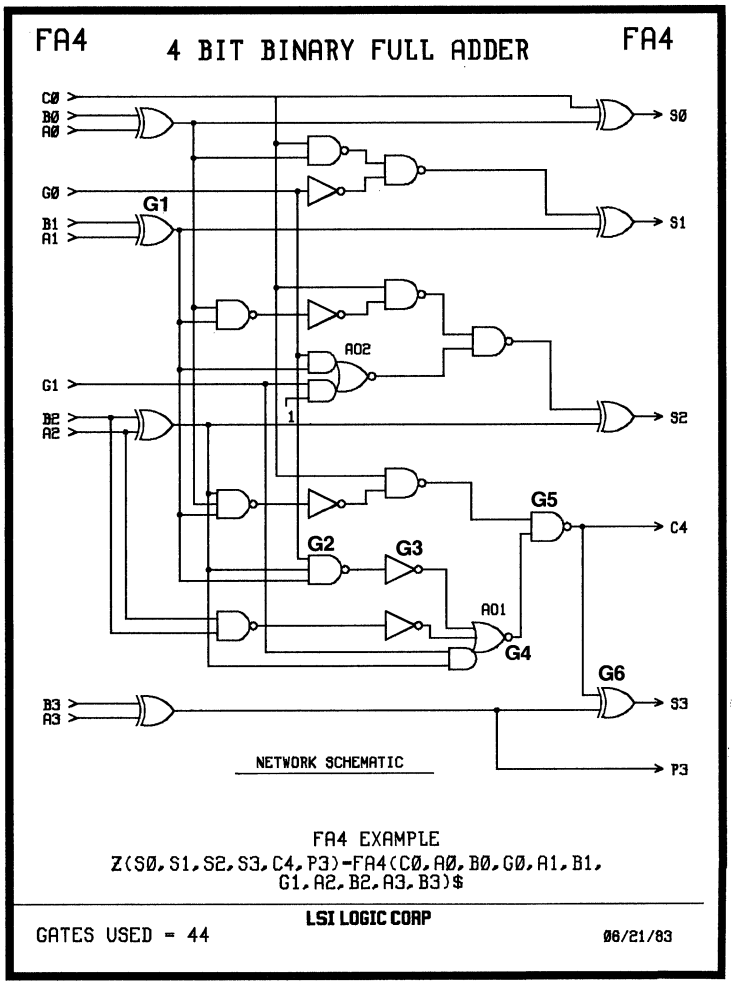
FA2 EXAMPLE

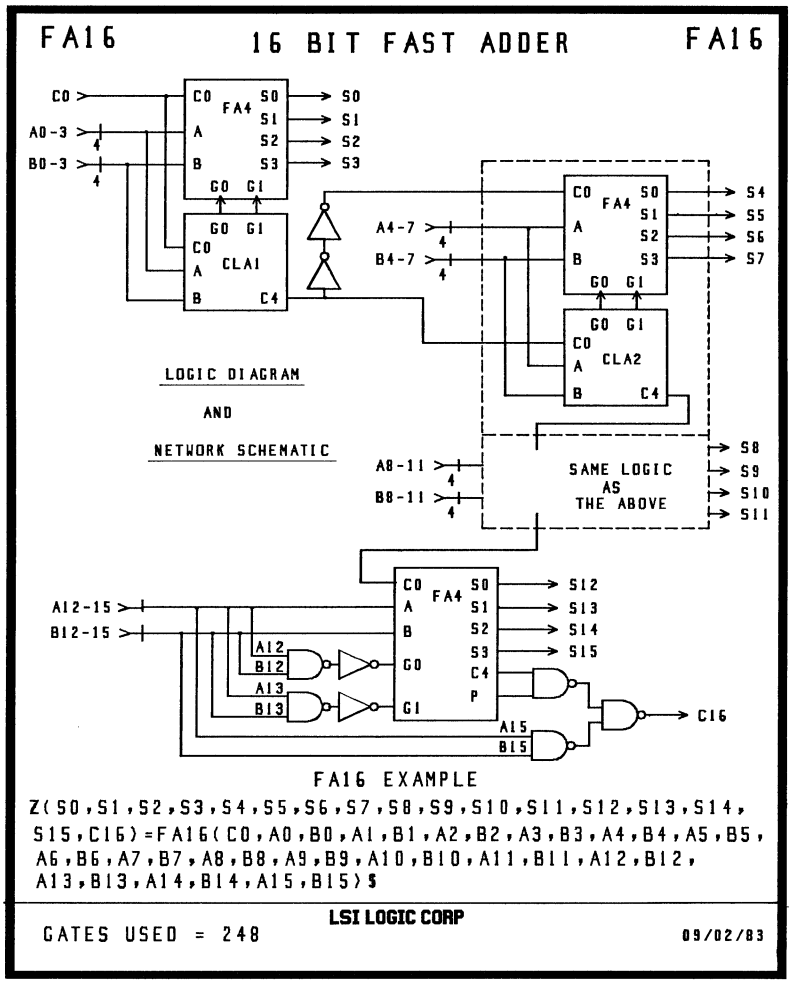
Z(S0,S1,C2) =FA2(C0,A0,B0,A1,B1)

WORKSTATION WC. DELAY
(RISE/FALL) DAISY ∩ MENTOR = / VALID =

LSI LOGIC CORP

GATES USED = 20
03/10/83

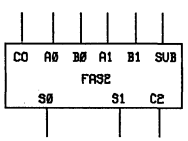

FA4
4 BIT BINARY FULL ADDER
FA4
C0
B0
A0
G0
G1
B1
A1
G1
B2
A2
B3
A3
A02
A01
G2
G3
G4
G5
G6
S0
S1
S2
C4
S3
P3
NETWORK SCHEMATIC
FA4 EXAMPLE
Z(S0,S1,S2,S3,C4,P3)=FA4(C0,A0,B0,G0,A1,B1,
G1,A2,B2,A3,B3)$
LSI LOGIC CORP
GATES USED = 44
06/21/83


FA16
16 BIT FAST ADDER
FA16
C0
A0-3
B0-3
FA4
CLA1
CLA2
LOGIC DIAGRAM
AND
NETWORK SCHEMATIC
A4-7
B4-7
A8-11
B8-11
SAME LOGIC
AS
THE ABOVE
A12-15
B12-15
S0
S1
S2
S3
S4
S5
S6
S7
S8
S9
S10
S11
S12
S13
S14
S15
C16
FA16 EXAMPLE
Z(S0,S1,S2,S3,S4,S5,S6,S7,S8,S9,S10,S11,S12,S13,S14,
S15,C16)=FA16(C0,A0,B0,A1,B1,A2,B2,A3,B3,A4,B4,A5,B5,
A6,B6,A7,B7,A8,B8,A9,B9,A10,B10,A11,B11,A12,B12,
A13,B13,A14,B14,A15,B15)$
LSI LOGIC CORP
GATES USED = 248
09/02/83

FAS2 FAS2

2 BIT BINARY 2'S COMPLEMENT FULL ADDER (A+B)
SUBTRACTOR (A-B). SIMILAR TO FA2 EXCEPT SUB
INVERTS B0 AND B1 AND SUBVERTS THE MEANING
OF CARRY TO NO BORROW.

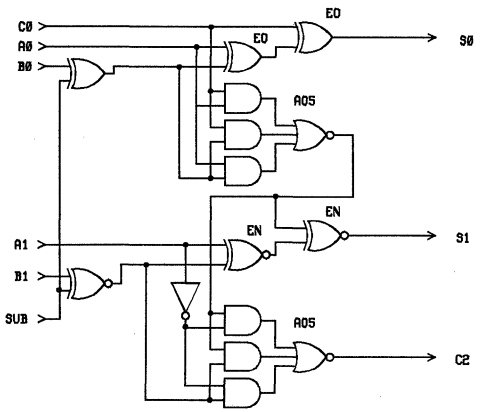
LOGIC DIAGRAM



TRUTH TABLE

C0 A0 B0	A1 B1	SUB	S0 S1 C2
		0	SEE FA2
C0 A0 B0	A1 B1	SUB	S0 S1 C2
		1	SEE FA2

NETWORK SCHEMATIC



FAS2 EXAMPLE

Z(S0,S1,C2) =FAS2(C0,A0,B0,A1,B1,SUB)$

WORKSTATION WC. DELAY (RISE/FALL) DAISY ∩ MENTOR = / VALID =

LSI LOGIC CORP

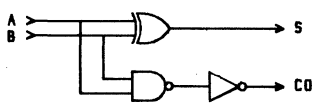
GATES USED = 25

02/16/83

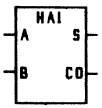
HA1 HA1

HALF ADDER

ELECTRICAL SCHEMATIC



LOGIC DIAGRAM



TRUTH TABLE

A	B	S	CO
0	0	0	0
1	0	1	0
0	1	1	0
1	1	0	1

HA1 EXAMPLE

Z(S,CO)=HA1(A,B)$

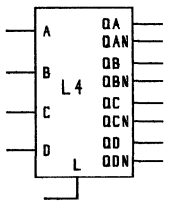
LSI LOGIC CORP

GATES USED = 5

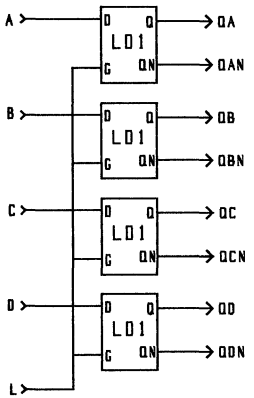
01/17/83

L4 4 BIT DATA LATCH L4

LOGIC DIAGRAM



NETWORK SCHEMATIC



L4 EXAMPLE

Z(QA,QAN,QB,QBN,QC,QCN,QD,QDN)=L4(A,B,C,D,L)$

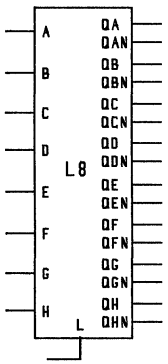
LSI LOGIC CORP

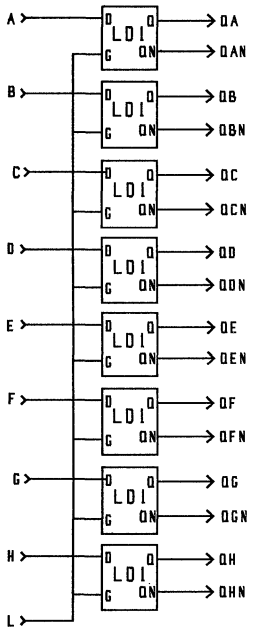
GATES USED = 12 02/01/83

L8 8 BIT DATA LATCH L8

NETWORK SCHEMATIC

LOGIC DIAGRAM



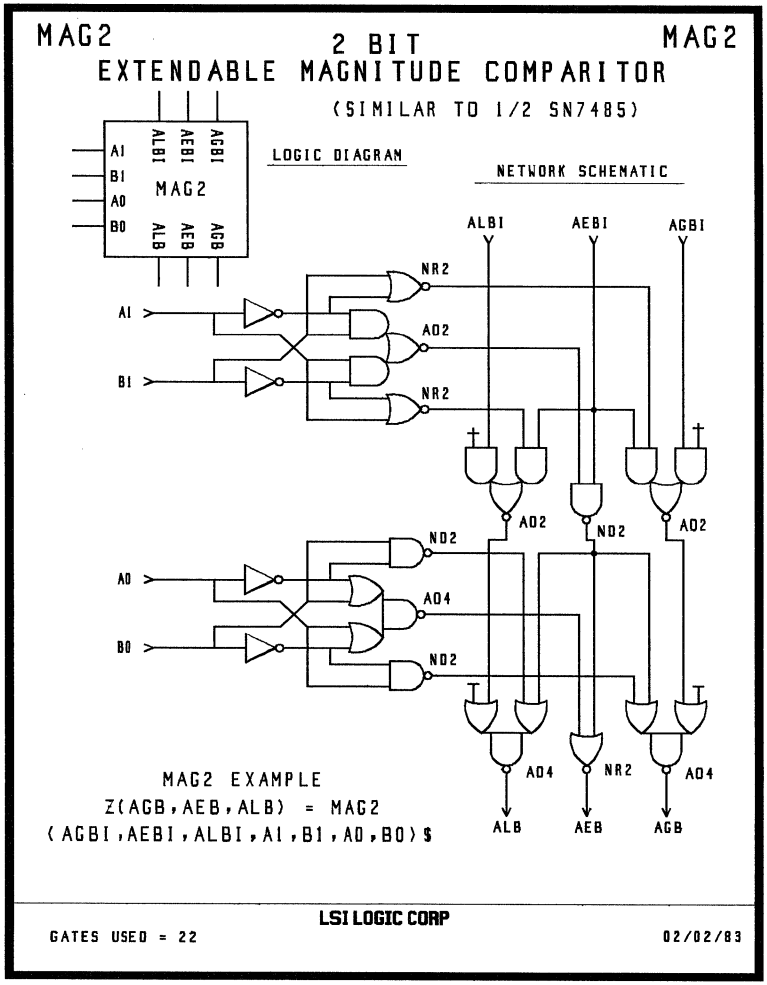


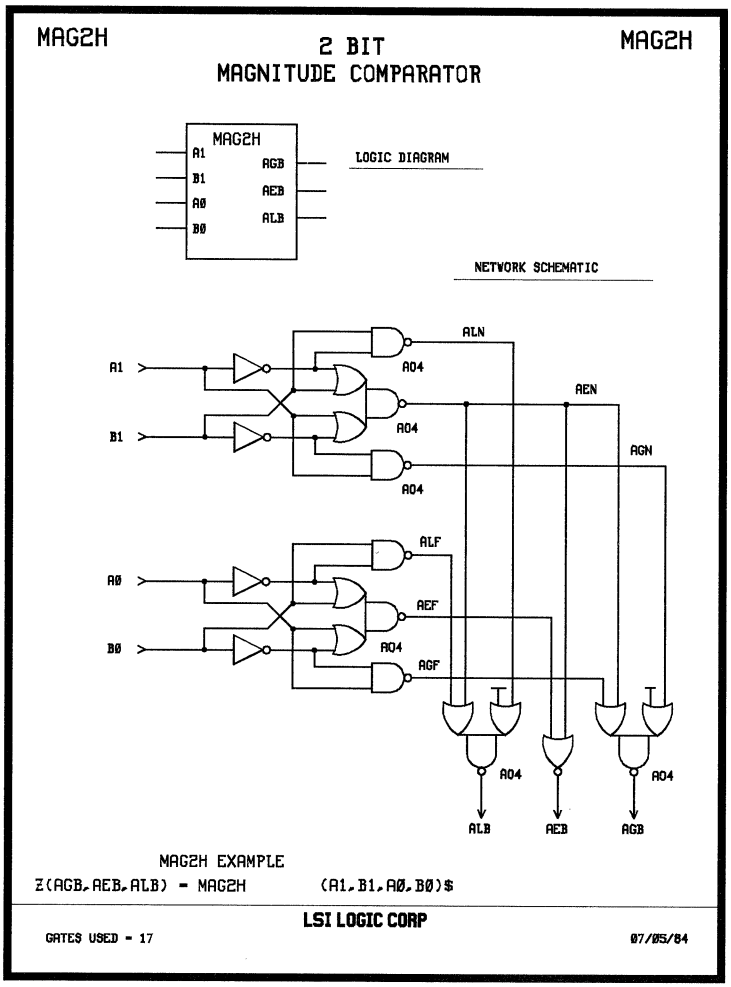
L8 EXAMPLE

Z(QA,QAN,QB,QBN,QC,QCN,QD,QDN,QE,QEN,QF,QFN,QG,QGN,
QH,QHN)=L8(A,B,C,D,E,F,G,H,L)$

LSI LOGIC CORP

GATES USED = 24 02/01/83

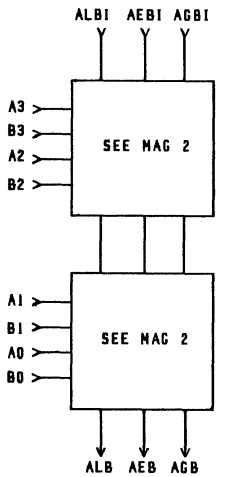

MAG2
2 BIT
EXTENDABLE MAGNITUDE COMPARITOR
MAG2
(SIMILAR TO 1/2 SN7485)
LOGIC DIAGRAN
NETWORK SCHEMATIC
A1
B1
A0
B0
ALBI
AEBI
AGBI
MAG2
ALB
AEB
AGB
NR2
AO2
ND2
AO4
MAG2 EXAMPLE
Z(AGB,AEB,ALB) = MAG2
(AGBI,AEBI,ALBI,A1,B1,A0,B0)$
LSI LOGIC CORP
GATES USED = 22
02/02/83


MAG2H
2 BIT
MAGNITUDE COMPARATOR
MAG2H
LOGIC DIAGRAM
NETWORK SCHEMATIC
A1
B1
AØ
BØ
AGB
AEB
ALB
AIN
AEN
AGN
AIF
AEF
AGF
AO4
MAG2H EXAMPLE
Z(AGB,AEB,ALB) = MAG2H (A1,B1,AØ,BØ)$
LSI LOGIC CORP
GATES USED = 17
07/05/84

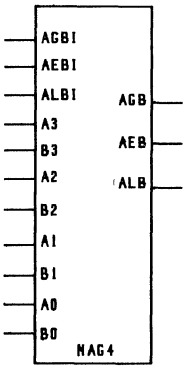
MAG4 MAG4

4 BIT MAGNITUDE COMPARATOR
EXPANDABLE (SAME AS M85C OR SN7485)

NETWORK SCHEMATIC



LOGIC DIAGRAM



MAG4 EXAMPLE

Z(AGB,AEB,ALB,)=MAG4(AGBI,AEBI,ALBI,A3,B3,A2,B2,
A1,B1,A0,B0)$

LSI LOGIC CORP

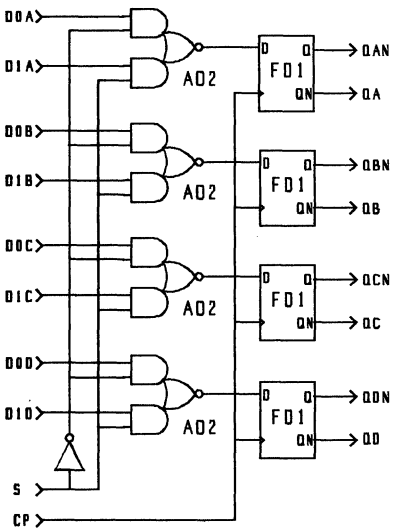
GATES USED = 44

02/21/83

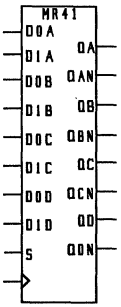
MR41 MR41

4 BIT REGISTER WITH 2 BIT MULTIPLEXED INPUTS

NETWORK SCHEMATIC



LOGIC DIAGRAM



MR41 EXAMPLE

Z(QA,QAN,QB,QBN,QC,QCN,QD,QDN) = MR41
(D0A,D1A,D0B,D1B,D0C,D1C,D0D,D1D,S,CP)$

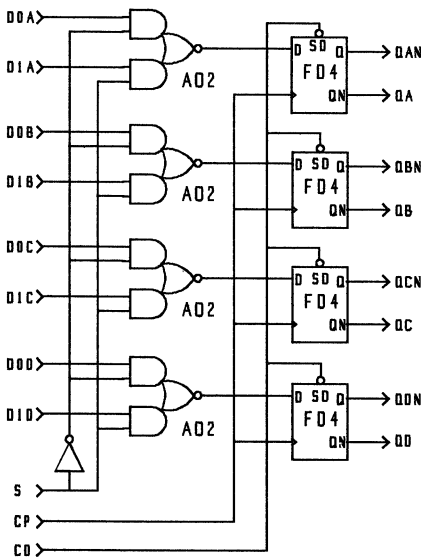
LSI LOGIC CORP

GATES USED = 29

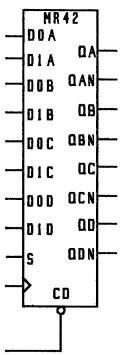
02/02/83

MR42 4 BIT REGISTER WITH 2 BIT MULTIPLEXED INPUTS, CLEAR DIRECT MR42

NETWORK SCHEMATIC



LOGIC DIAGRAN



MR42 EXAMPLE

Z(QA,QAN,QB,QBN,QC,QCN,QD,QDN) = MR42
(D0A,D1A,D0B,D1B,D0C,D1C,D0D,D1D,S,CP,CD)$

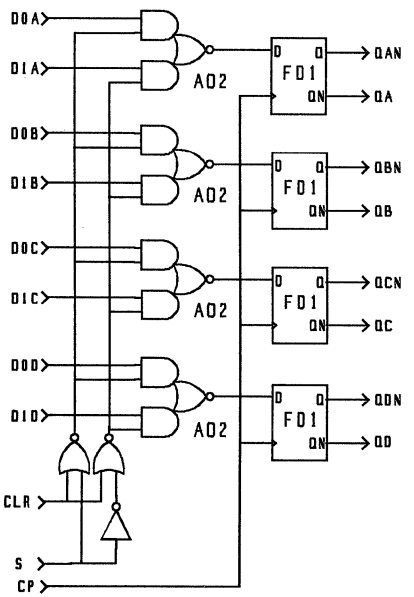
LSI LOGIC CORP

GATES USED = 33

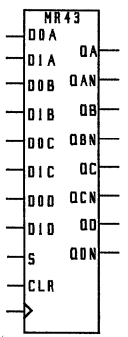
02/02/83

MR43 4 BIT REGISTER WITH 2 BIT MULTIPLEXED INPUTS, SYNC CLEAR MR43

NETWORK SCHEMATIC



LOGIC DIAGRAN



MR43 EXAMPLE

Z(QA,QAN,QB,QBN,QC,QCN,QD,QDN) = MR43
(D0A,D1A,D0B,D1B,D0C,D1C,D0D,D1D,S,CLR,CP)$

LSI LOGIC CORP

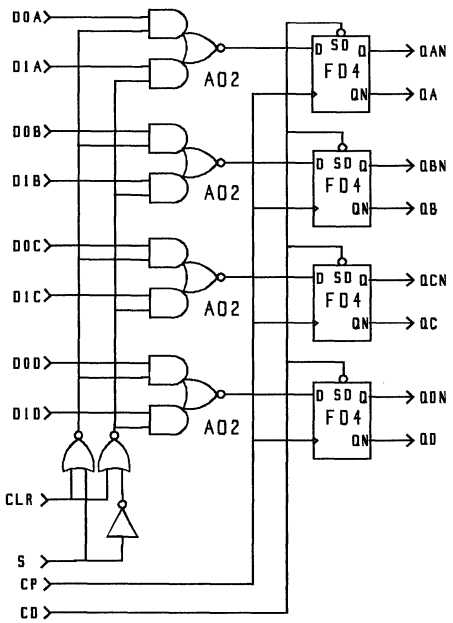
GATES USED = 31

02/02/83

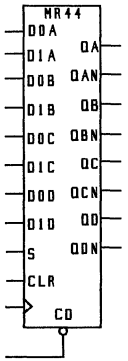
MR44 4 BIT REGISTER WITH 2 BIT MULTIPLEXED INPUTS, SYNC CLEAR CD

MR44

NETWORK SCHEMATIC



LOGIC DIAGRAN



MR44 EXAMPLE

```
Z(QA,QAN,QB,QBN,QC,QCN,QD,QDN) = MR44
(D0A,D1A,D0B,D1B,D0C,D1C,D0D,D1D,S,CLR,CP,CD)$
```

LSI LOGIC CORP

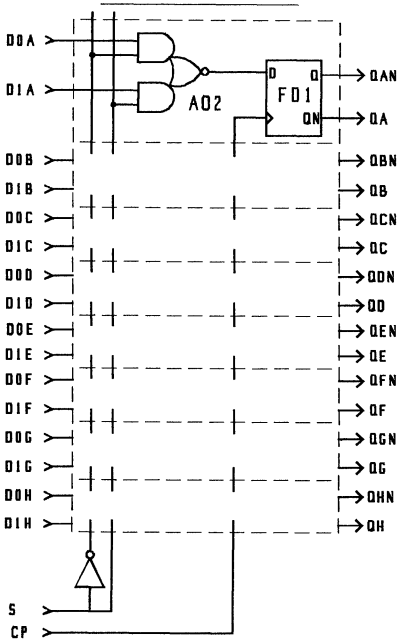
GATES USED = 35

02/02/83

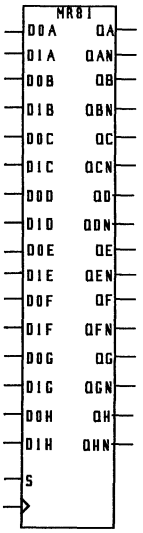
MR81 8 BIT REGISTER WITH 2 BIT MULTIPLEXED INPUTS

MR81

NETWORK SCHEMATIC



LOGIC DIAGRAN



MR81 EXAMPLE

```
Z(QA,QAN,QB,QBN,QC,QCN,QD,QDN,QE,QEN,QF,QFN,QG,QGN,
QH,QHN)=MR81(D0A,D1A,D0B,D1B,D0C,D1C,D0D,D1D,
  D0E,D1E,D0F,D1F,D0G,D1G,D0H,D1H,S,CP)$
```

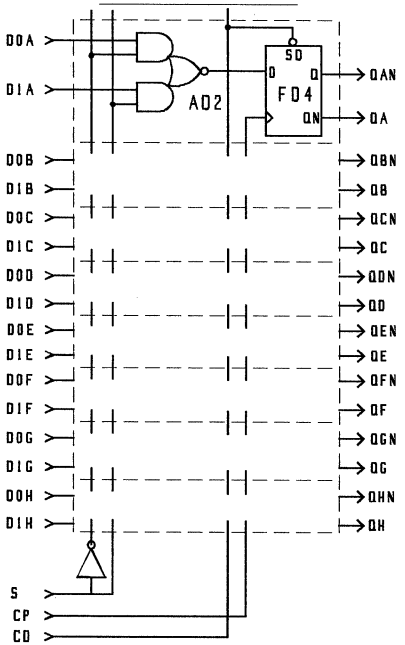
LSI LOGIC CORP

GATES USED = 57

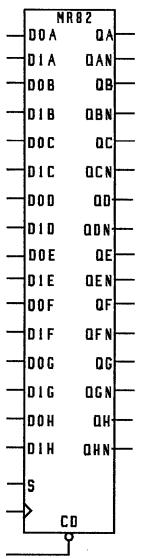
05/12/83

MR82 8 BIT REGISTER WITH 2 BIT MULTIPLEXED UNITS, CLEAR DIRECT MR82

NETWORK SCHEMATIC



LOGIC DIAGRAM



MR82 EXAMPLE

Z(QA,QAN,QB,QBN,QC,QCN,QD,QDN,QE,QEN,QF,QFN,QG,QGN,
QH,QHN)=MR82(D0A,D1A,D0B,D1B,D0C,D1C,D0D,D1D,
D0E,D1E,D0F,D1F,D0G,D1G,D0H,D1H,S,CP,CD)$

LSI LOGIC CORP

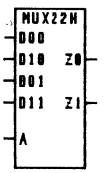
GATES USED = 65

05/12/83

MUX22H MUX22H

DUAL 2 BIT NON INVERTING MUX

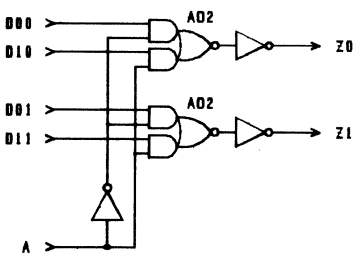
LOGIC DIAGRAM



TRUTH TABLE

A	Z(I)
0	D0(I)
1	D1(I)

ELECTRICAL SCHEMATIC



MUX22H EXAMPLE

Y(Z0,Z1)=MUX22H(D00,D10,D01,D11,A)$

LSI LOGIC CORP

GATES USED = 7

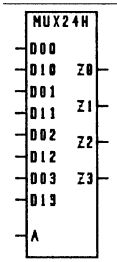
03/14/83

MUX24H

MUX24H

QUAD 2 BIT NON INVERTING MUX

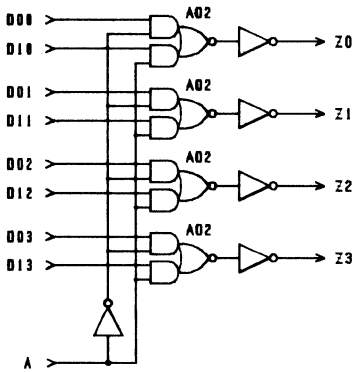
LOGIC DIAGRAM



TRUTH TABLE

A	Z(I)
0	D0(I)
1	D1(I)

ELECTRICAL SCHEMATIC



MUX24H EXAMPLE

```
Y(Z0,Z1,Z2,Z3)=MUX24H(D00,D10,
,D01,D11,D02,D12,D03,D13,A)$
```

LSI LOGIC CORP

GATES USED = 13

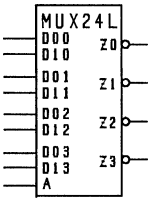
03/14/83

MUX24L

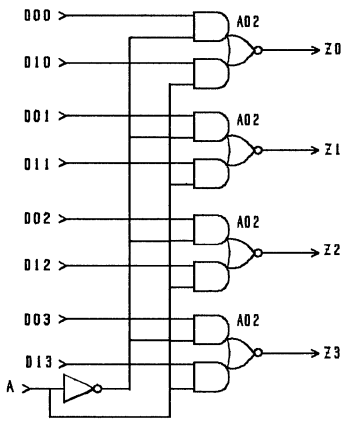
MUX24L

QUAD 2 BIT INVERTING MUX

LOGIC DIAGRAM



NETWORK SCHEMATIC



MUX24L EXAMPLE

```
Z(Z0,Z1,Z2,Z3)=MUX24L(D00,D10,D01,D11,D02,D12,D03,D13,A)$
```

LSI LOGIC CORP

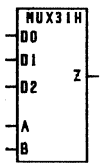
GATES USED = 9

02/04/83

MUX31H MUX31H

3 BIT NON INVERTING MUX

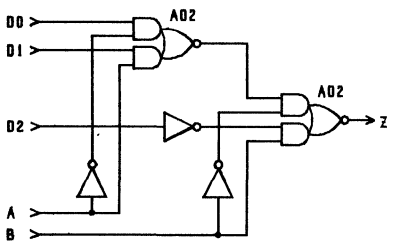
LOGIC DIAGRAM



TRUTH TABLE

A	B	Z
0	0	D0
1	0	D1
0	1	D2
1	1	D2

ELECTRICAL SCHEMATIC



MUX31H EXAMPLE

Z = MUX31H (D0,D1,D2,A,B)$

LSI LOGIC CORP

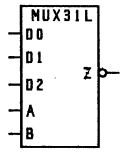
GATES USED = 7

03/04/83

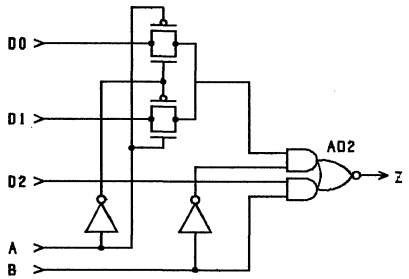
MUX31L MUX31L

3 BIT INVERTING MUX

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



MUX31L EXAMPLE

Z = MUX31L (D0,D1,D2,A,B)$

LSI LOGIC CORP

GATES USED = 6

04/11/83

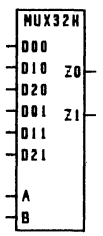
MUX32H MUX32H

DUAL 3 BIT NON INVERTING MUX

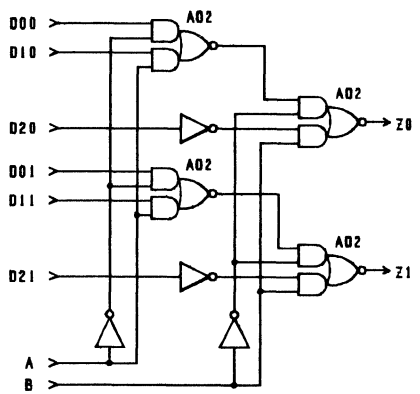
TRUTH TABLE

A	B	Z(I)
0	0	D0(I)
1	0	D1(I)
0	1	D2(I)
1	1	D2(I)

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



MUX32H EXAMPLE

Y(Z0,Z1)=MUX32H(D00,D10,D20,D01,D11,D21,A,B)$

LSI LOGIC CORP

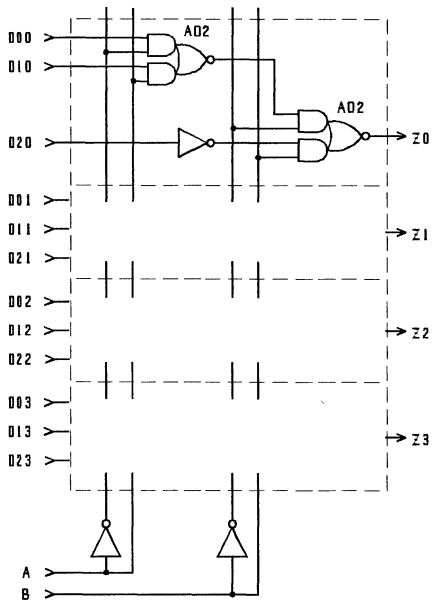
GATES USED = 12

03/14/83

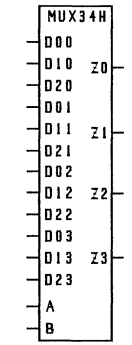
MUX34H MUX34H

QUAD 3 BIT NON INVERTING MUX

ELECTRICAL SCHEMATIC



LOGIC DIAGRAM



TRUTH TABLE

A	B	Z(I)
0	0	D0(I)
1	0	D1(I)
0	1	D2(I)
1	1	D2(I)

MUX34H EXAMPLE

Y(Z0,Z1,Z2,Z3)=MUX34H(D00,D10,D20,D01,D11,D21,
D02,D12,D22,D03,D13,D23,A,B)$

LSI LOGIC CORP

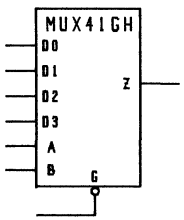
GATES USED = 22

05/11/83

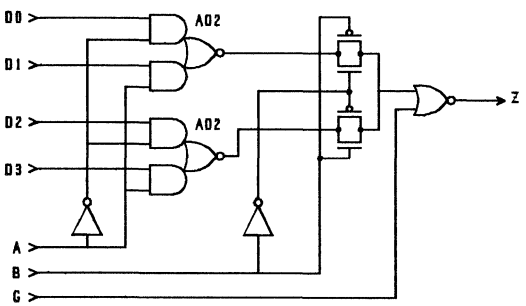
MUX41GH — MUX41GH

4 BIT NON INVERTING MUX, GATED

LOGIC DIAGRAM



NETWORK SCHEMATIC



MUX41GH EXAMPLE

```
Z(Z) = MUX41GH(D0,D1,D2,D3,A,B,G)$
```

LSI LOGIC CORP

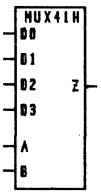
GATES USED = 8

03/11/83

MUX41H — MUX41H

4 BIT NON INVERTING MUX

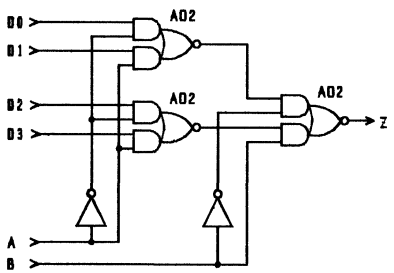
LOGIC DIAGRAM



TRUTH TABLE

A	B	Z
0	0	D0
1	0	D1
0	1	D2
1	1	D3

ELECTRICAL SCHEMATIC



MUX41H EXAMPLE

```
Z = MUX41H (D0,D1,D2,D3,A,B)$
```

LSI LOGIC CORP

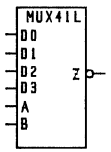
GATES USED = 8

03/04/83

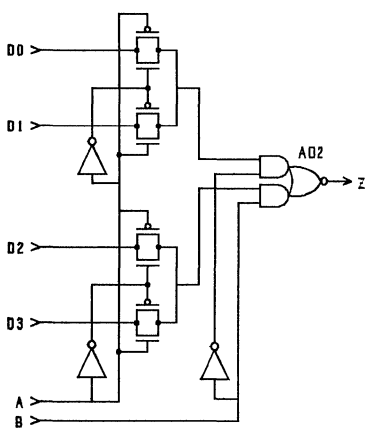
MUX41L

4 BIT INVERTING MUX

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



MUX41L EXAMPLE

```
Z = MUX41L (D0,D1,D2,D3,A,B)$
```

LSI LOGIC CORP

GATES USED = 7

01/17/83

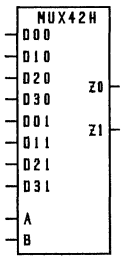
MUX42H

DUAL 4 BIT NON INVERTING MUX

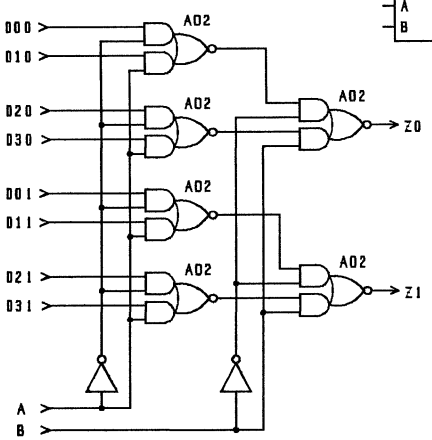
TRUTH TABLE

A	B	Z(I)
0	0	D0(I)
1	0	D1(I)
0	1	D2(I)
1	1	D3(I)

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



MUX42H EXAMPLE

```
Y(Z0,Z1)=MUX42H(D00,D10,D20,D30,D01,D11,D21,D31,A,B)$
```

LSI LOGIC CORP

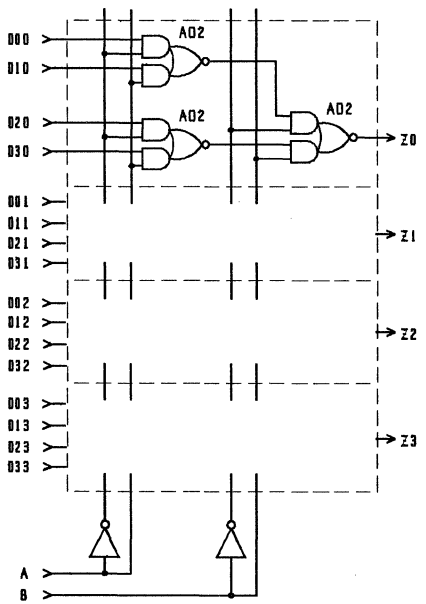
GATES USED = 14

03/14/83

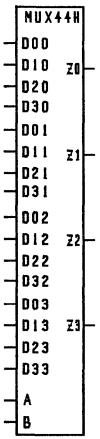
MUX44H MUX44H

QUAD 4 BIT NON INVERTING MUX

ELECTRICAL SCHEMATIC



LOGIC DIAGRAM



TRUTH TABLE

A	B	Z(I)
0	0	D0(I)
1	0	D1(I)
0	1	D2(I)
1	1	D3(I)

MUX44H EXAMPLE

```
Y(Z0,Z1,Z2,Z3)=MUX44H(D00,D10,D20,D30.D01,D11,D21,D31,
    D02,D12,D22,D32,D03,D13,D23,D33,A,B)$
```

LSI LOGIC CORP

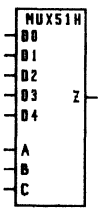
GATES USED = 26

06/21/83

MUX51H MUX51H

5 BIT NON INVERTING MUX

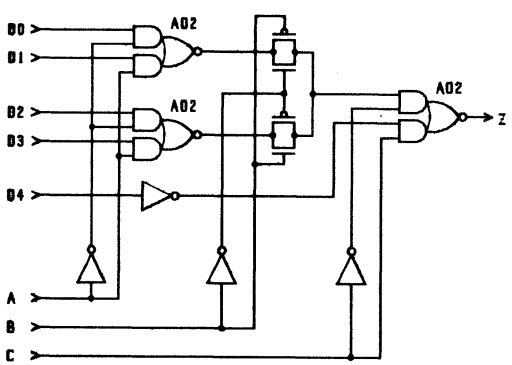
LOGIC DIAGRAM



TRUTH TABLE

A	B	C	Z
0	0	0	D0
1	0	0	D1
0	1	0	D2
1	1	0	D3
0	0	1	D4
1	0	1	D4
0	1	1	D4
1	1	1	D4

ELECTRICAL SCHEMATIC



MUX51H EXAMPLE

```
Z = MUX51H (D0,D1,D2,D3,D4,A,B,C)$
```

LSI LOGIC CORP

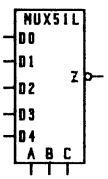
GATES USED = 11

03/04/83

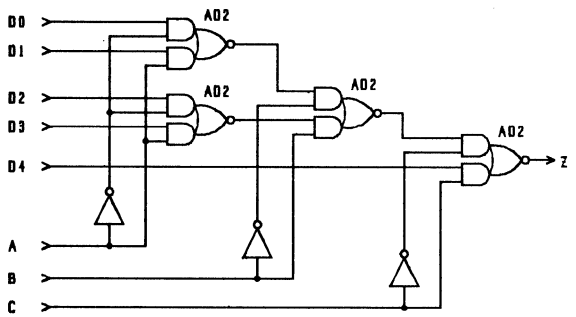
MUX51L MUX51L

5 BIT INVERTING MUX

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



MUX51L EXAMPLE

Z = MUX51L (D0,D1,D2,D3,D4,A,B,C)$

LSI LOGIC CORP

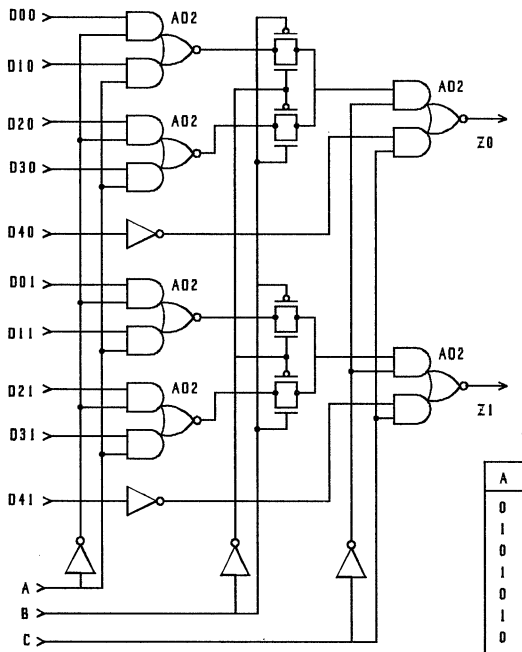
GATES USED = 11

03/10/83

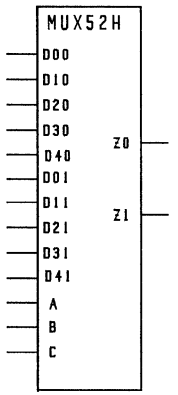
MUX52H MUX52H

DUAL 5 BIT NON INVERTING MUX

NETWORK SCHEMATIC



LOGIC DIAGRAM



TRUTH TABLE

A	B	C	Z(I)
0	0	0	D0(I)
1	0	0	D1(I)
0	1	0	D2(I)
1	1	0	D3(I)
0	0	1	D4(I)
1	0	1	D4(I)
0	1	1	D4(I)
1	1	1	D4(I)

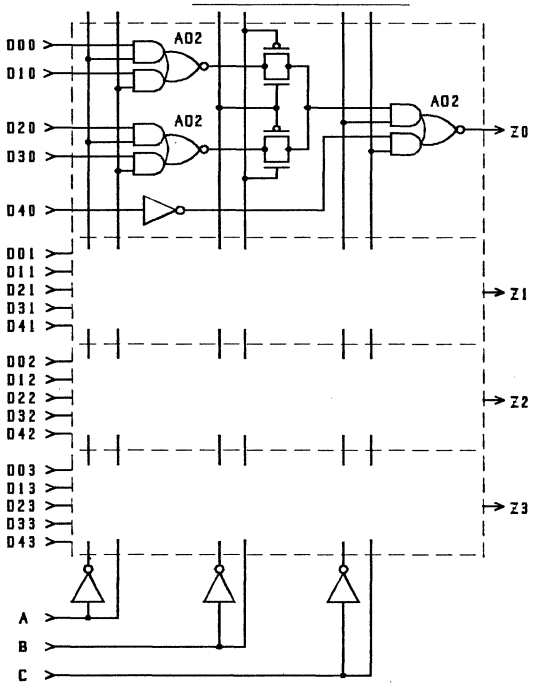
MUX41GH EXAMPLE LSI LOGIC CORP

Y(Z0,Z1)=MUX52H(D00,D10,D20,D30,D40,D01,D11, 05/15/83

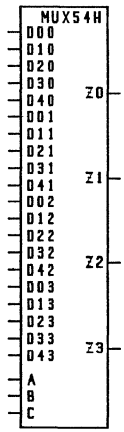
D21,D31,D41,A,B,C)$ GATES USED = 19

MUX54H QUAD 5 BIT NON INVERTING MUX MUX54H

NETWORK SCHEMATIC



LOGIC DIAGRAM



TRUTH TABLE

A	B	C	Z(I)
0	0	0	D0(I)
1	0	0	D1(I)
0	1	0	D2(I)
1	1	0	D3(I)
0	0	1	D4(I)
1	0	1	D4(I)
0	1	1	D4(I)
1	1	1	D4(I)

MUX54H EXAMPLE

```
Y(Z0,Z1,Z2,Z3)=MUX54H(D00,D10,D20,D30,D40,D01,
 D11,D21,D31,D41,D02,D12,D22,D32,D42,D03,D13,
 D23,D33,D43,A,B,C)$
```

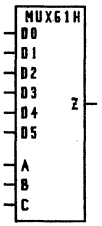
LSI LOGIC CORP

GATES USED = 35

05/12/83

MUX61H 6 BIT NON INVERTING MUX MUX61H

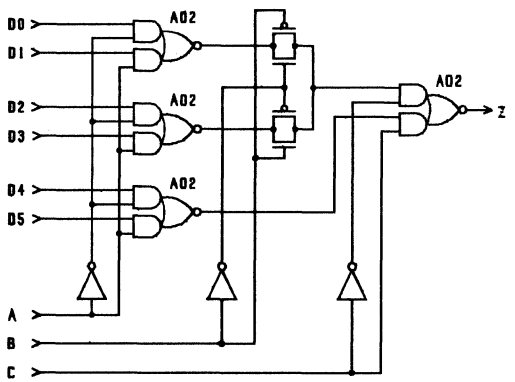
LOGIC DIAGRAM



TRUTH TABLE

A	B	C	Z
0	0	0	D0
1	0	0	D1
0	1	0	D2
1	1	0	D3
0	0	1	D4
1	0	1	D5
0	1	1	D4
1	1	1	D5

ELECTRICAL SCHEMATIC



MUX61H EXAMPLE

```
Z = MUX61H (D0,D1,D2,D3,D4,D5,A,B,C)$
```

LSI LOGIC CORP

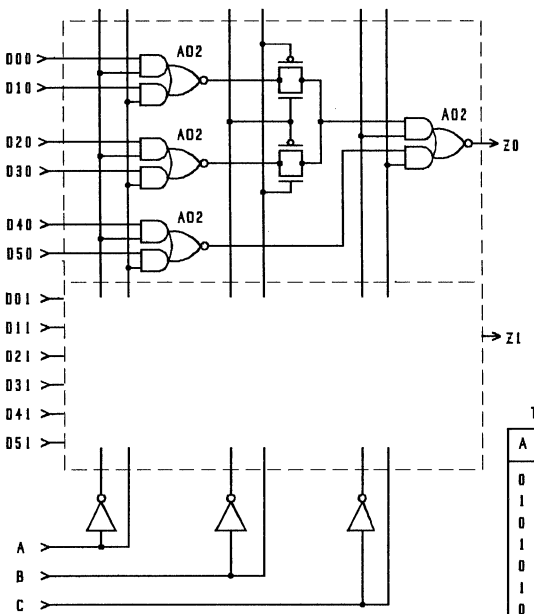
GATES USED = 12

03/04/83

MUX62H DUAL MUX62H

6 BIT NON INVERTING MUX

NETWORK SCHEMATIC



TRUTH TABLE

A	B	C	Z(I)
0	0	0	D0(I)
1	0	0	D1(I)
0	1	0	D2(I)
1	1	0	D3(I)
0	0	1	D4(I)
1	0	1	D5(I)
0	1	1	D4(I)
1	1	1	D5(I)

MUX62H EXAMPLE

```
Y(Z0,Z1)=MUX62H(D00,D10,D20,D30,D40,D50,
 D01,D11,D21,D31,D41,D51,A,B,C)$
```

LSI LOGIC CORP

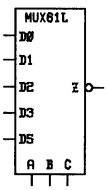
GATES USED = 21

06/21/83

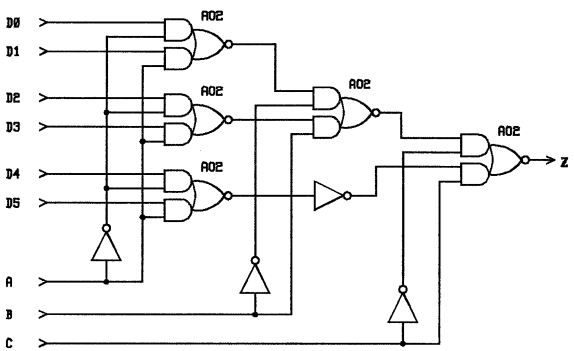
MUX61L MUX61L

6 BIT INVERTING MUX

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



MUX61L EXAMPLE

```
Z = MUX61L (D0,D1,D2,D3,D4,D5,A,B,C)$
```

LSI LOGIC CORP

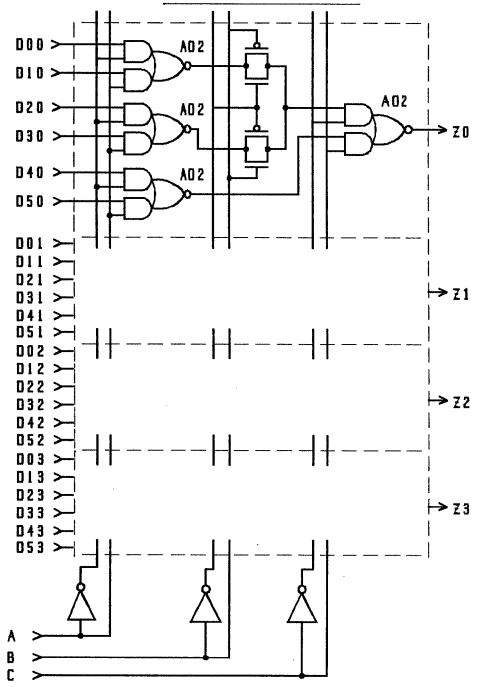
GATES USED = 14

02/21/83

MUX64H QUAD MUX64H

6 BIT NON INVERTING MUX

NETWORK SCHEMATIC



TRUTH TABLE

A	B	C	Z(I)
0	0	0	D0(I)
1	0	0	D1(I)
0	1	0	D2(I)
1	1	0	D3(I)
0	0	1	D4(I)
1	0	1	D5(I)
0	1	1	D4(I)
1	1	1	D5(I)

MUX64H EXAMPLE

```
Y(Z0,Z1,Z2,Z3)=MUX64H(D00,D10,D20,D30,D40,D50,D01,
 D11,D21,D31,D41,D51,D02,D12,D22,D32,D42,D52,D03,
 D13,D23,D33,D43,D53,A,B,C)$
```

LSI LOGIC CORP

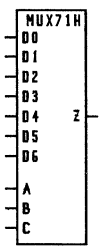
GATES USED = 39

05/15/83

MUX71H MUX71H

7 BIT NON INVERTING MUX

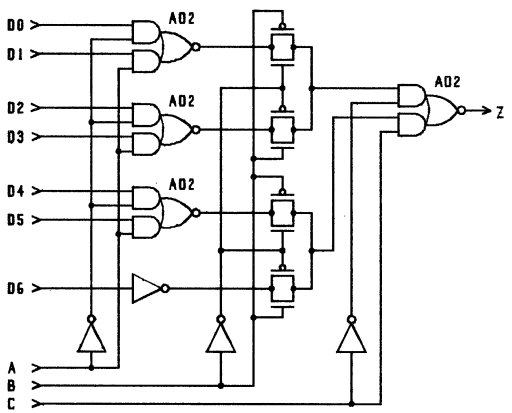
LOGIC DIAGRAM



TRUTH TABLE

A	B	C	Z
0	0	0	D0
1	0	0	D1
0	1	0	D2
1	1	0	D3
0	0	1	D4
1	0	1	D5
0	1	1	D6
1	1	1	D6

ELECTRICAL SCHEMATIC



MUX71H EXAMPLE

```
Z = MUX71H (D0,D1,D2,D3,D4,D5,D6,A,B,C)$
```

LSI LOGIC CORP

GATES USED = 13

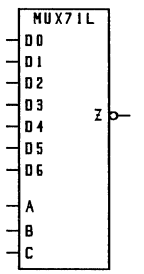
03/08/83

MUX71L

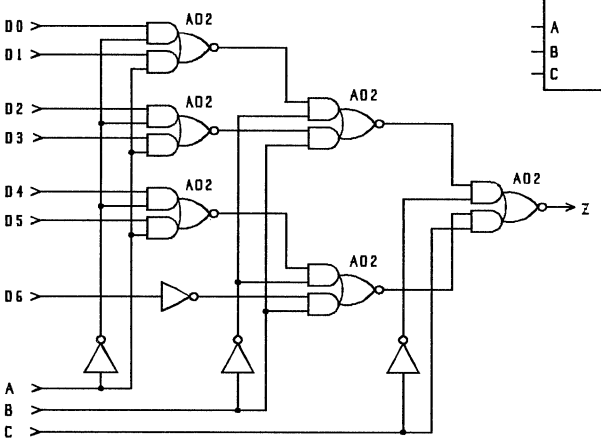
7 BIT INVERTING MUX

MUX71L

LOGIC DIAGRAM



NETWORK SCHEMATIC



MUX71L EXAMPLE

```
Z = MUX71L (D0,D1,D2,D3,D4,D5,D6,A,B,C)$
```

LSI LOGIC CORP

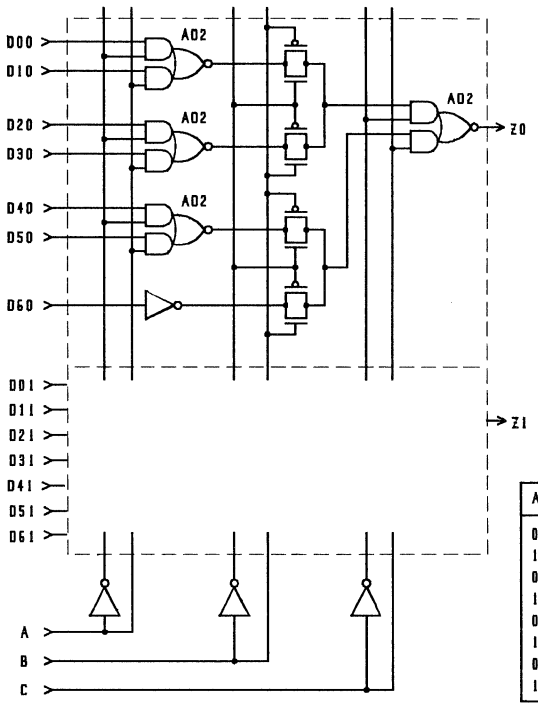
GATES USED = 16

05/11/83

MUX72H

DUAL 7 BIT NON INVERTING MUX

MUX72H



TRUTH TABLE

A	B	C	Z(I)
0	0	0	D0(I)
1	0	0	D1(I)
0	1	0	D2(I)
1	1	0	D3(I)
0	0	1	D4(I)
1	0	1	D5(I)
0	1	1	D6(I)
1	1	1	D6(I)

MUX72H EXAMPLE

```
Y(Z0,Z1)=MUX72H(D00,D10,D20,D30,D40,D50,D60,
 D01,D11,D21,D31,D41,D51,D61,A,B,C)$
```

LSI LOGIC CORP

GATES USED = 23

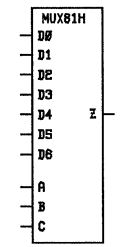
06/21/83

MUX81H

MUX81H

8 BIT NON INVERTING MUX

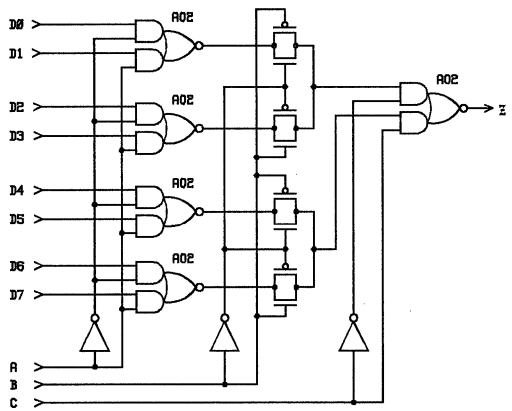
LOGIC DIAGRAM



TRUTH TABLE

A	B	C	Z
0	0	0	D0
1	0	0	D1
0	1	0	D2
1	1	0	D3
0	0	1	D4
1	0	1	D5
0	1	1	D6
1	1	1	D7

ELECTRICAL SCHEMATIC



MUX81H EXAMPLE

Z = MUX81H (D0,D1,D2,D3,D4,D5,D6,D7,A,B,C)$

LSI LOGIC CORP

GATES USED = 14

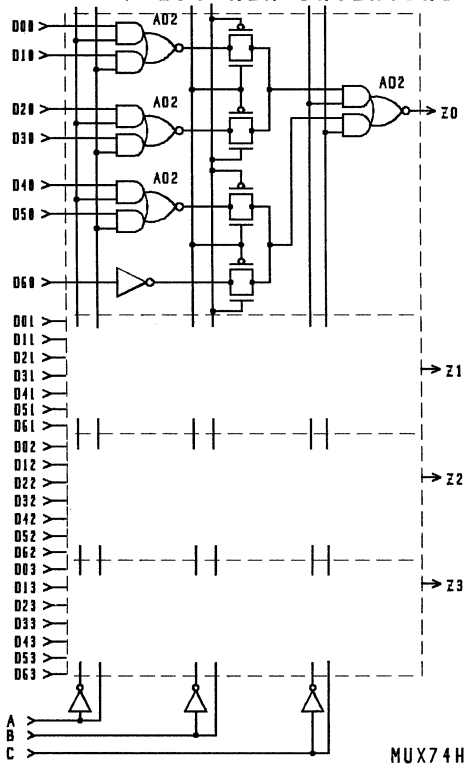
07/05/84

MUX74H

QUAD

MUX74H

7 BIT NON INVERTING MUX



TRUTH TABLE

A	B	C	Z(I)
0	0	0	D0(I)
1	0	0	D1(I)
0	1	0	D2(I)
1	1	0	D3(I)
0	0	1	D4(I)
1	0	1	D5(I)
0	1	1	D6(I)
1	1	1	D6(I)

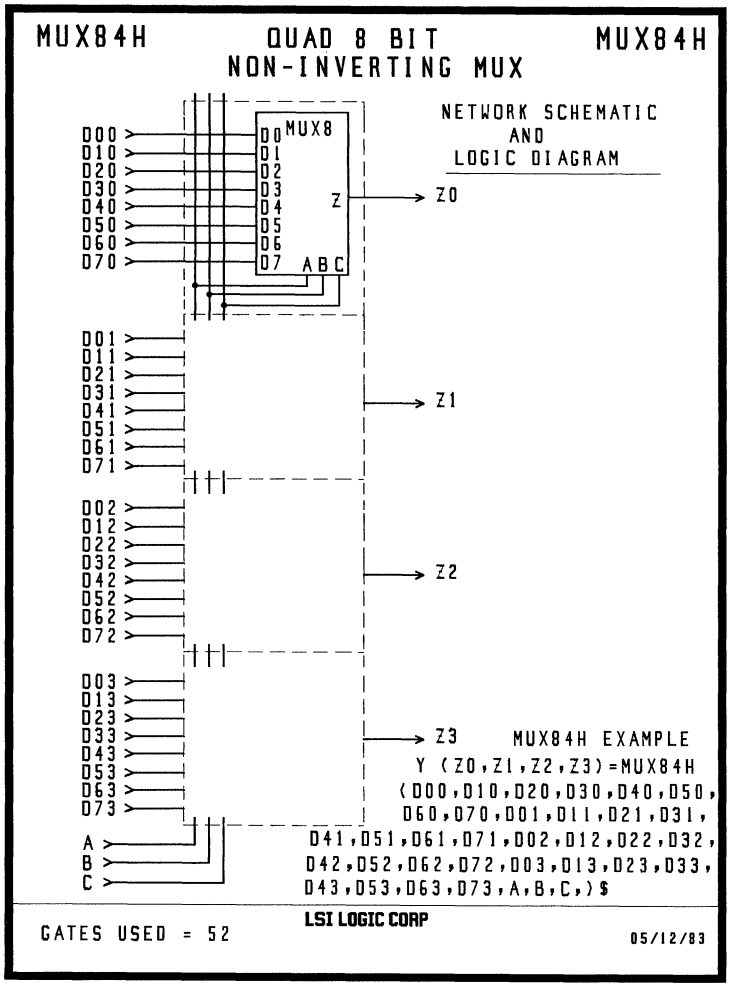
MUX74H EXAMPLE

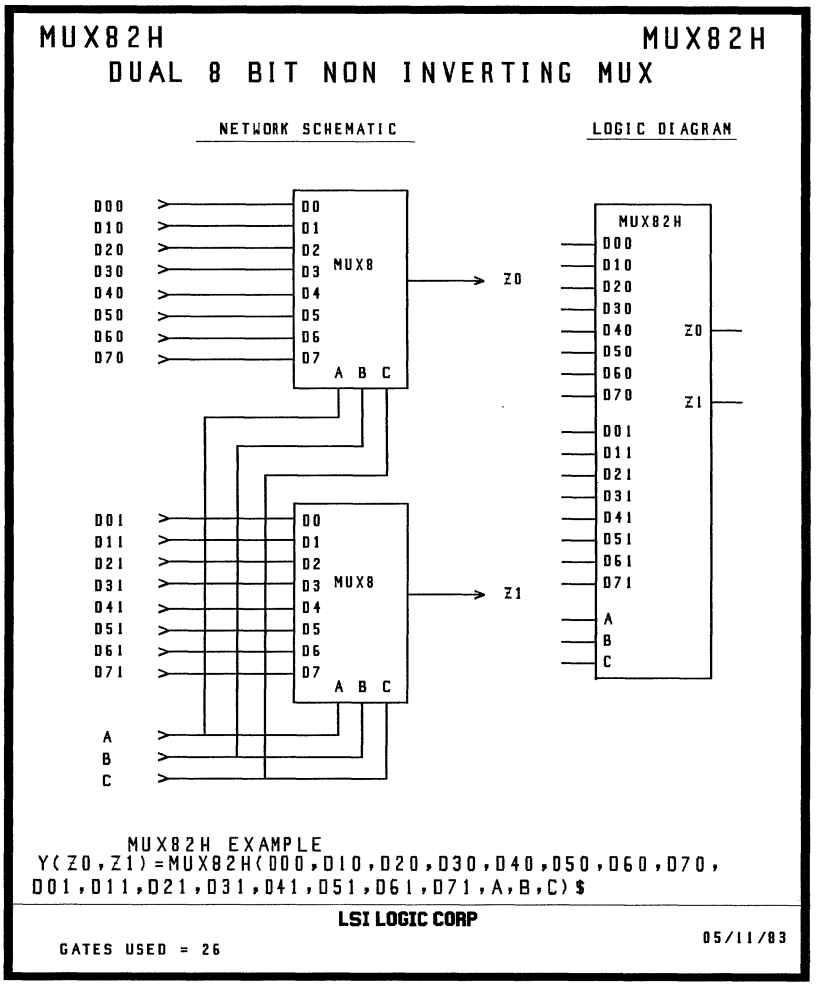
Y(Z0,Z1,Z2,Z3)=MUX74H(D00,D10,D20,D30,D40,D50,D60,
D01,D11,D21,D31,D41,D51,D61,D02,D12,D22,D32,D42,D52,
D62,D03,D13,D23,D33,D43,D53,D63,A,B,C)$

LSI LOGIC CORP

GATES USED = 47

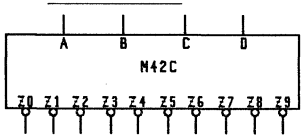
06/21/83


MUX84H
QUAD 8 BIT
NON-INVERTING MUX
MUX84H
NETWORK SCHEMATIC
AND
LOGIC DIAGRAM
MUX8
D00
D10
D20
D30
D40
D50
D60
D70
D0
D1
D2
D3
D4
D5
D6
D7
Z
A B C
Z0
D01
D11
D21
D31
D41
D51
D61
D71
Z1
D02
D12
D22
D32
D42
D52
D62
D72
Z2
D03
D13
D23
D33
D43
D53
D63
D73
Z3
A
B
C
MUX84H EXAMPLE
Y (Z0,Z1,Z2,Z3)=MUX84H
(D00,D10,D20,D30,D40,D50,
D60,D70,D01,D11,D21,D31,
D41,D51,D61,D71,D02,D12,D22,D32,
D42,D52,D62,D72,D03,D13,D23,D33,
D43,D53,D63,D73,A,B,C,)$
LSI LOGIC CORP
GATES USED = 52
05/12/83

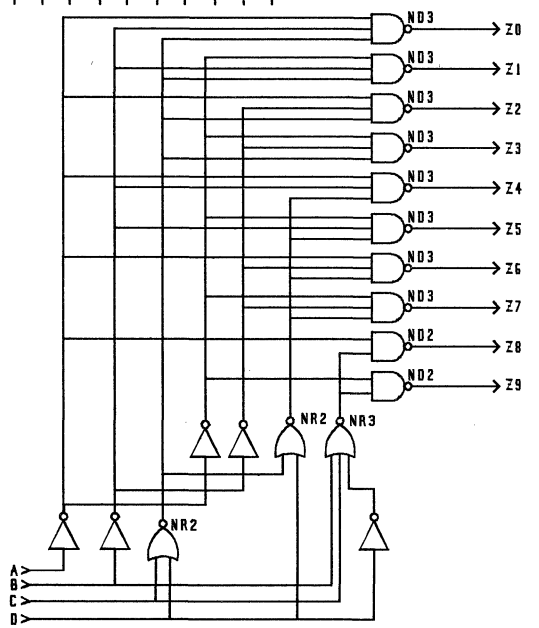

MUX82H
MUX82H
DUAL 8 BIT NON INVERTING MUX
NETWORK SCHEMATIC
LOGIC DIAGRAM
MUX8
D00
D10
D20
D30
D40
D50
D60
D70
D0
D1
D2
D3
D4
D5
D6
D7
A B C
Z0
D01
D11
D21
D31
D41
D51
D61
D71
Z1
A
B
C
MUX82H
MUX82H EXAMPLE
Y(Z0,Z1)=MUX82H(D00,D10,D20,D30,D40,D50,D60,D70,
D01,D11,D21,D31,D41,D51,D61,D71,A,B,C)$
LSI LOGIC CORP
GATES USED = 26
05/11/83

M42C 4 TO 10 DECODER M42C

LOGIC DIAGRAM



NETWORK SCHEMATIC



M42C EXAMPLE

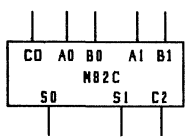
Y(Z0,Z1,Z2,Z3,Z4,Z5,Z6,Z7,Z8,Z9)=M42C(A,B,C,D)$

LSI LOGIC CORP 02/10/83

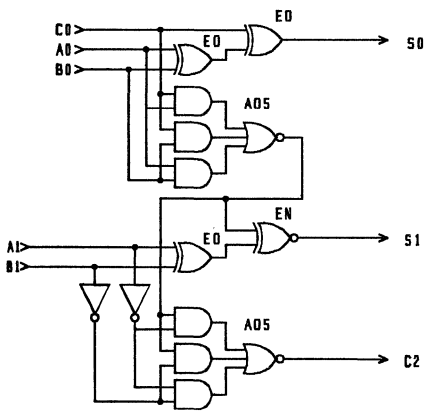
GATES USED = 22

M82C 2 BIT BINARY FULL ADDER (SAME AS FA2) M82C

LOGIC DIAGRAM



NETWORK SCHEMATIC



M82C EXAMPLE

Z(S0,S1,C2) = M82C(C0,A0,B0,A1,B1)$

LSI LOGIC CORP 02/15/83

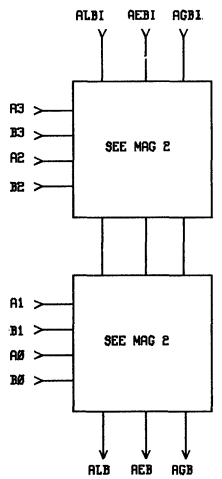
GATES USED = 20

M85C M85C

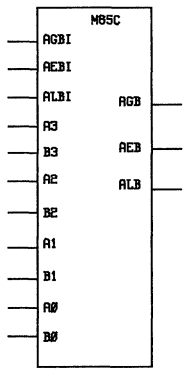
4 BIT MAGNITUDE COMPARITOR

EXPANDABLE (SIMILIAR TO MAG4 OR SN7485)

NETWORK SCHEMATIC



LOGIC DIAGRAM



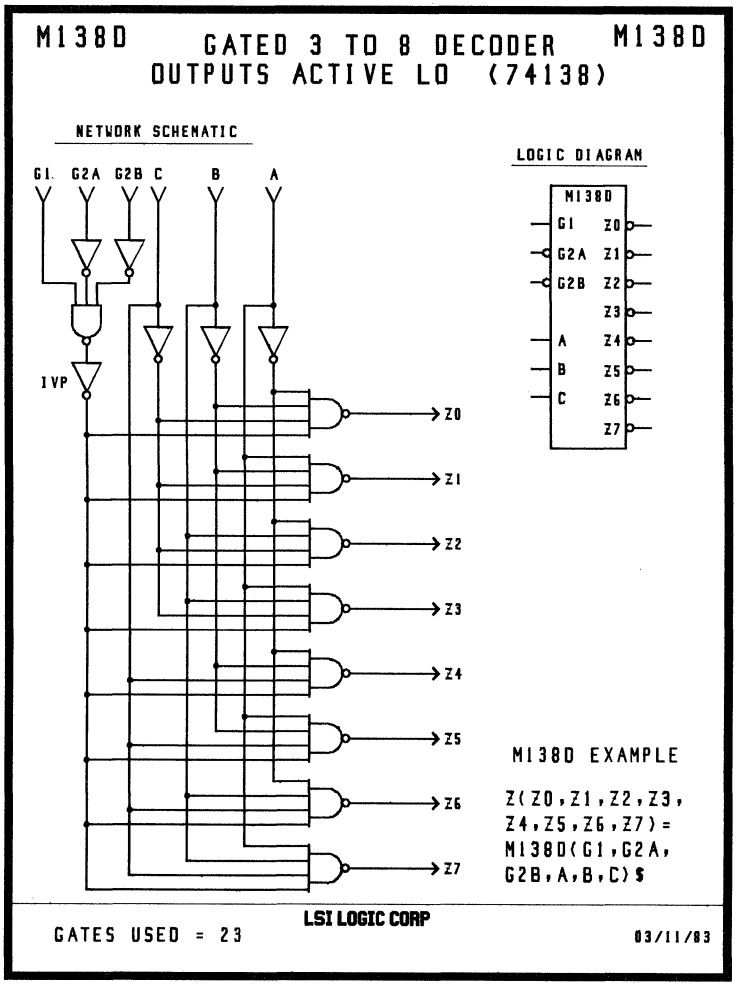
M85C EXAMPLE

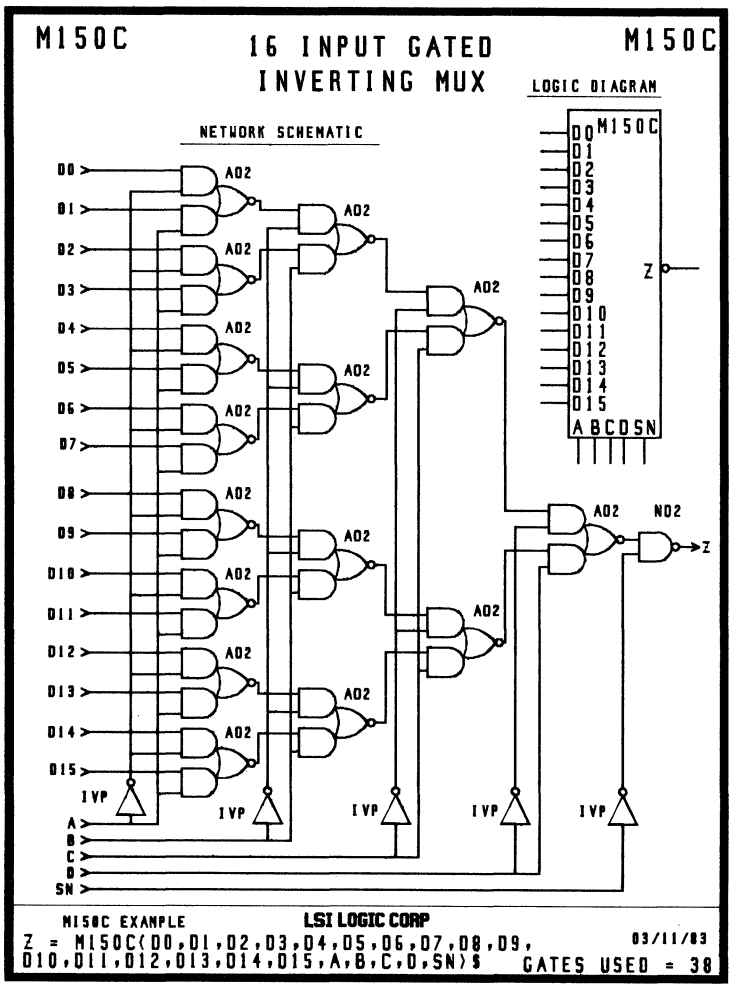
Z(AGB,AEB,ALB,)=M85C(AGBI,AEBI,ALBI,A3,B3,A2,B2,
A1,B1,A0,B0)$

LSI LOGIC CORP

GATES USED = 44

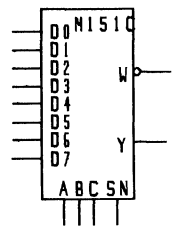
07/05/84


M138D
GATED 3 TO 8 DECODER
OUTPUTS ACTIVE LO (74138)
M138D
NETWORK SCHEMATIC
G1 G2A G2B C B A
IVP
Z0
Z1
Z2
Z3
Z4
Z5
Z6
Z7
LOGIC DIAGRAM
M138D
G1 Z0
G2A Z1
G2B Z2
Z3
A Z4
B Z5
C Z6
Z7
M138D EXAMPLE
Z(Z0,Z1,Z2,Z3,
Z4,Z5,Z6,Z7)=
M138D(G1,G2A,
G2B,A,B,C)$
LSI LOGIC CORP
GATES USED = 23
03/11/83

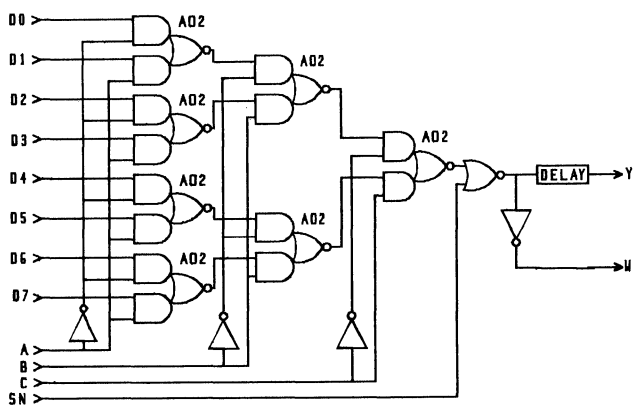

M150C
16 INPUT GATED
INVERTING MUX
M150C
LOGIC DIAGRAM
M150C
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
Z
A B C D SN
NETWORK SCHEMATIC
AO2
NO2
IVP
A
B
C
D
SN
Z
M150C EXAMPLE
Z = M150C(D0,D1,D2,D3,D4,D5,D6,D7,D8,D9,
D10,D11,D12,D13,D14,D15,A,B,C,D,SN)$
LSI LOGIC CORP
03/11/83
GATES USED = 38

M151C 8 INPUT GATED MUX M151C

LOGIC DIAGRAM



NETWORK SCHEMATIC



M151C EXAMPLE

Z(W,Y) = M151C(D0,D1,D2,D3,D4,D5,D6,D7,A,B,C,SN)$

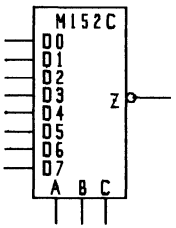
GATES USED = 20

LSI LOGIC CORP

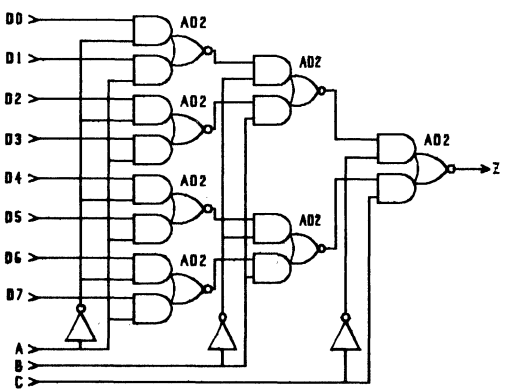
03/11/83

M152C 8 INPUT INVERTING MUX M152C

LOGIC DIAGRAM



NETWORK SCHEMATIC



GATES USED = 18

LSI LOGIC CORP

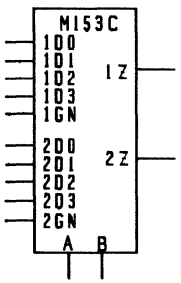
M152C EXAMPLE

Z = M152C(D0,D1,D2,D3,D4,D5,D6,D7,A,B,C)$

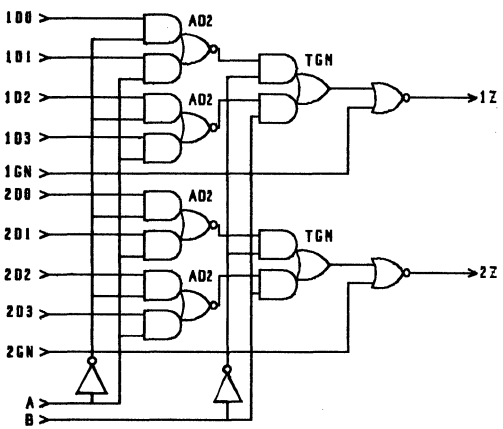
03/11/83

M153C DUAL 4 INPUT MUX M153C

LOGIC DIAGRAM



NETWORK SCHEMATIC

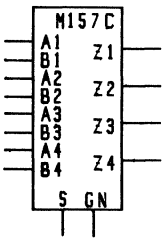


M153C EXAMPLE LSI LOGIC CORP

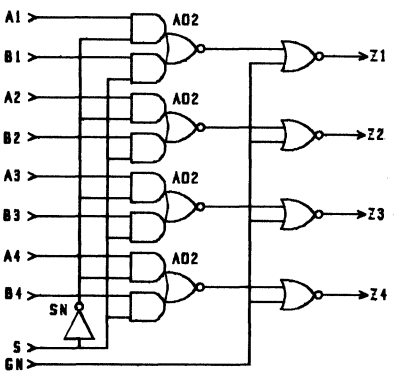
X(1Z,2Z) = M153C(1D0,1D1,1D2,1D3,2D0,2D1, 03/11/83
2D2,2D3,A,B,1GN,2GN)$ GATES USED = 14

M157C QUAD 2 INPUT GATED NON INVERTING MUX M157C

LOGIC DIAGRAM



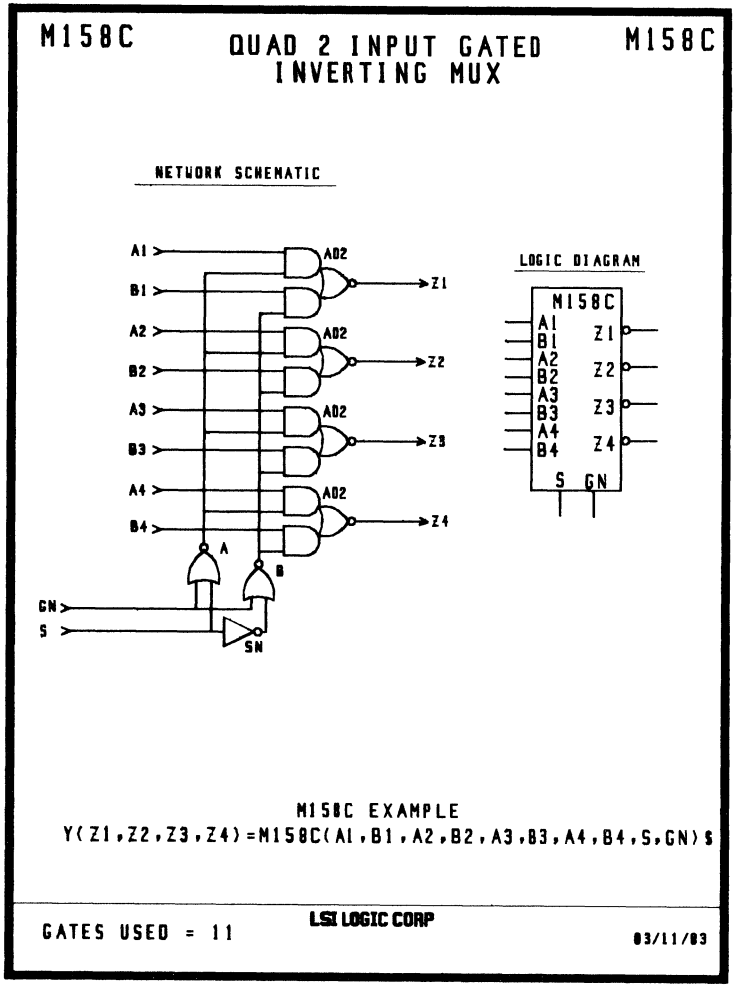
NETWORK SCHEMATIC

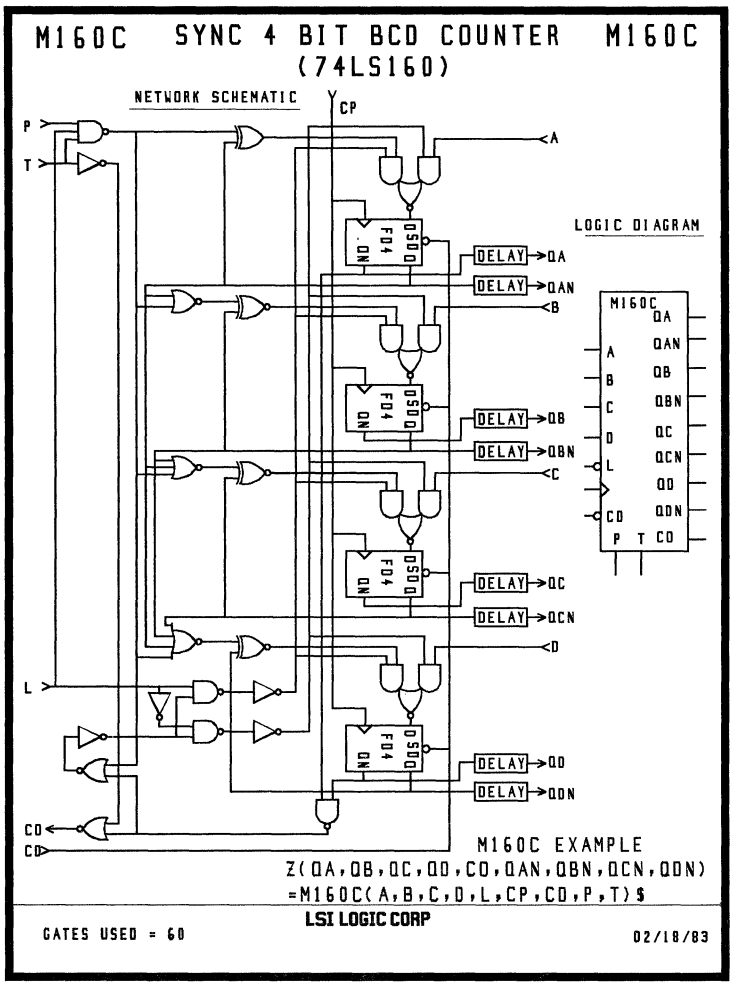


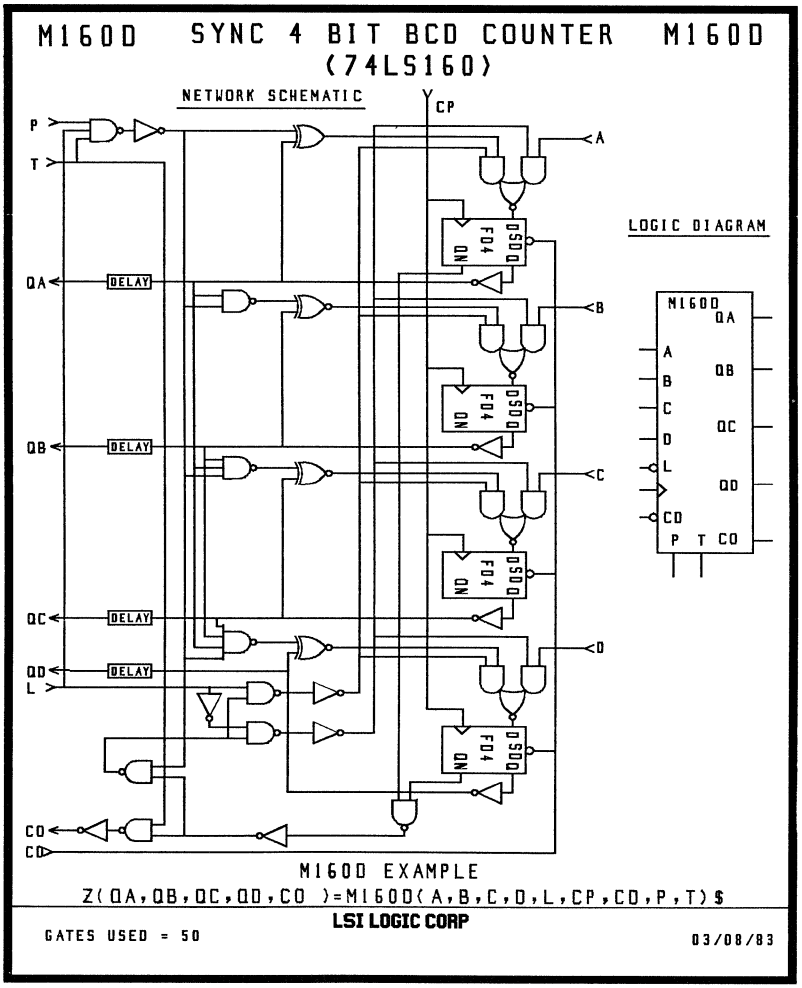
M157C EXAMPLE

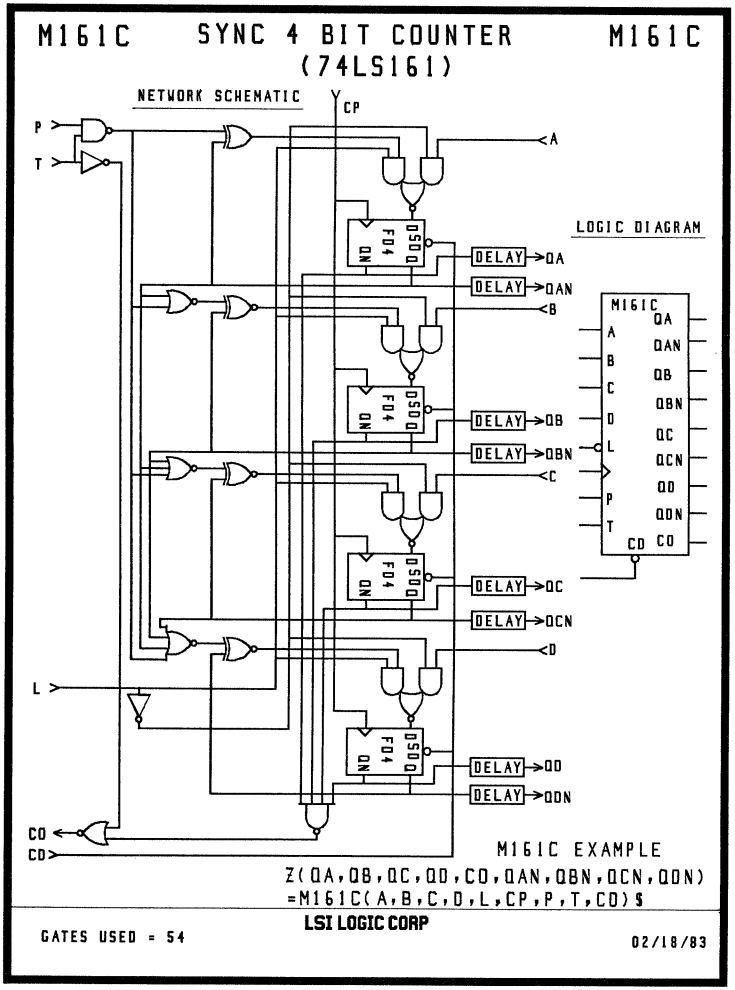
Y(Z1,Z2,Z3,Z4)=M157C(A1,B1,A2,B2,A3,B3,A4,B4,S,GN)$

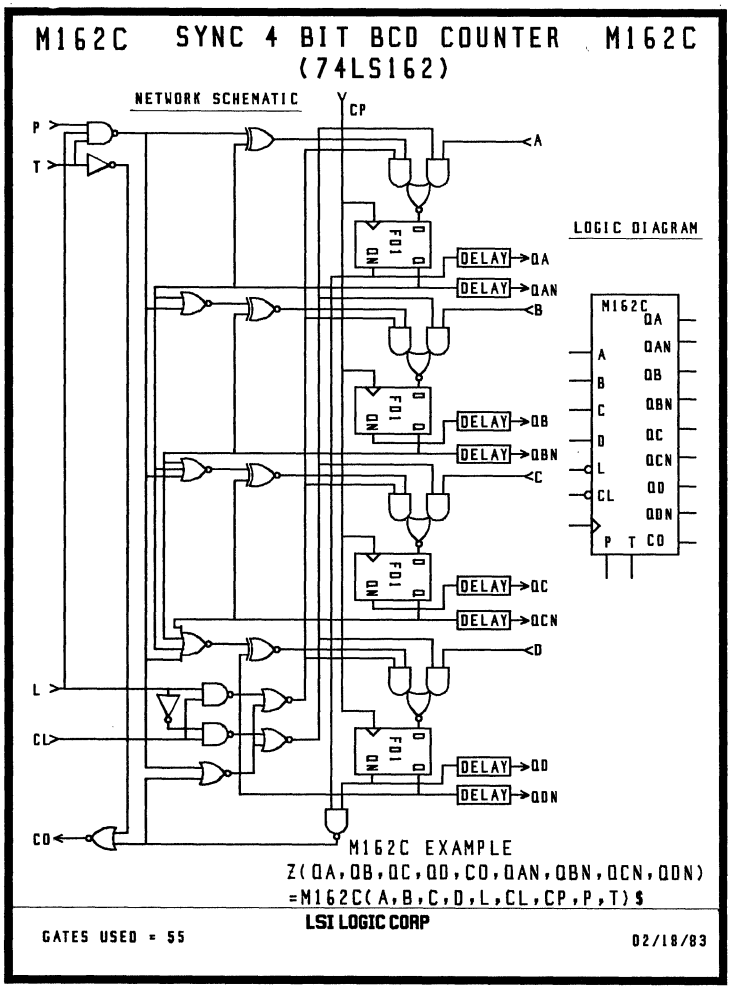
GATES USED = 13 LSI LOGIC CORP 03/11/83

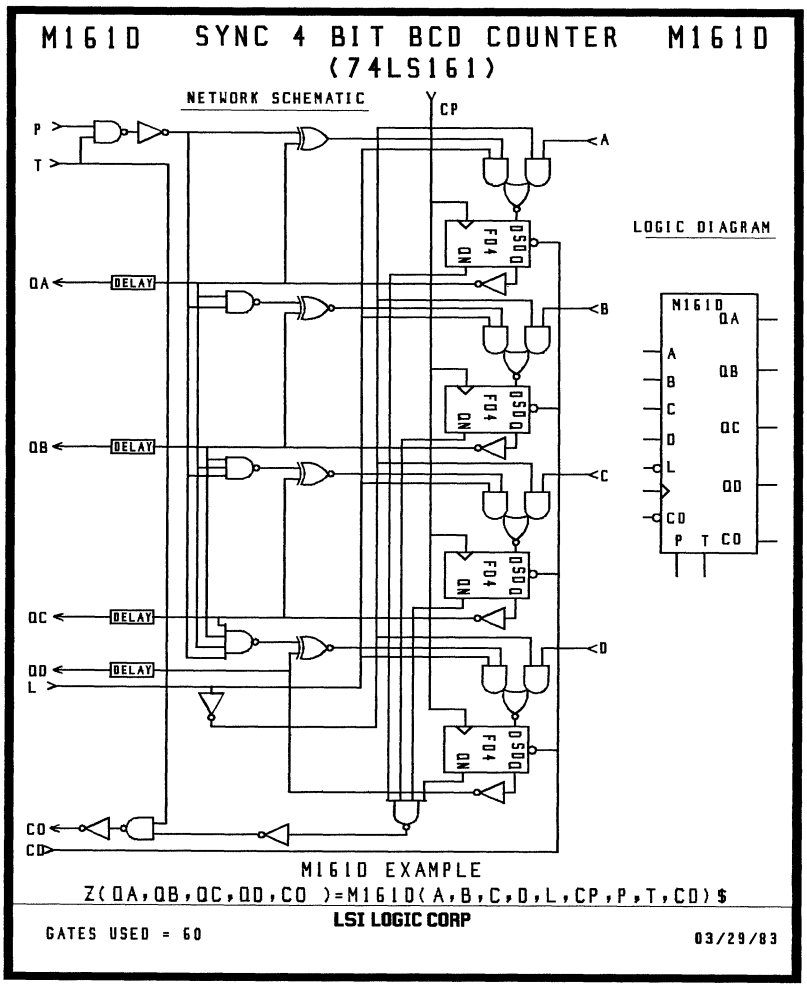

M158C
QUAD 2 INPUT GATED INVERTING MUX
M158C
NETWORK SCHEMATIC
LOGIC DIAGRAM
A1
B1
A2
B2
A3
B3
A4
B4
GN
S
Z1
Z2
Z3
Z4
A
B
SN
M158C EXAMPLE
Y(Z1,Z2,Z3,Z4)=M158C(A1,B1,A2,B2,A3,B3,A4,B4,S,GN)$
GATES USED = 11
LSI LOGIC CORP
03/11/83

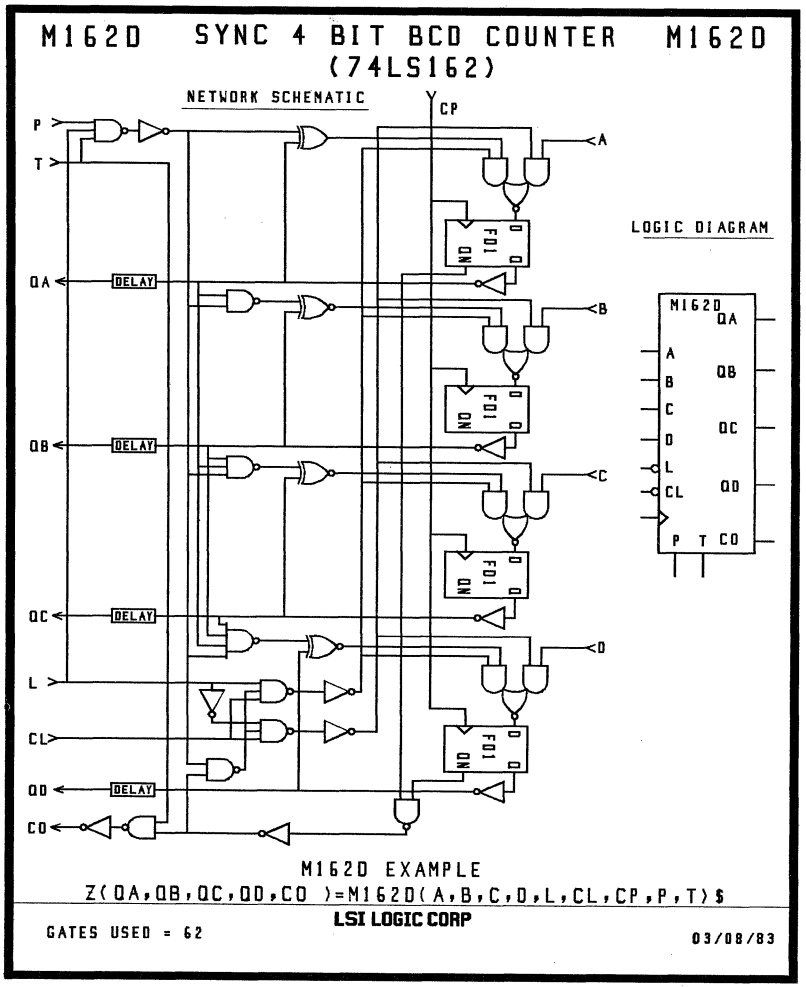

M160C
SYNC 4 BIT BCD COUNTER
(74LS160)
M160C
NETWORK SCHEMATIC
LOGIC DIAGRAM
P
T
CP
L
CD
A
B
C
D
DELAY
QA
QAN
QB
QBN
QC
QCN
QD
QDN
M160C EXAMPLE
Z(QA,QB,QC,QD,CO,QAN,QBN,QCN,QDN)
=M160C(A,B,C,D,L,CP,CD,P,T)$
GATES USED = 60
LSI LOGIC CORP
02/18/83

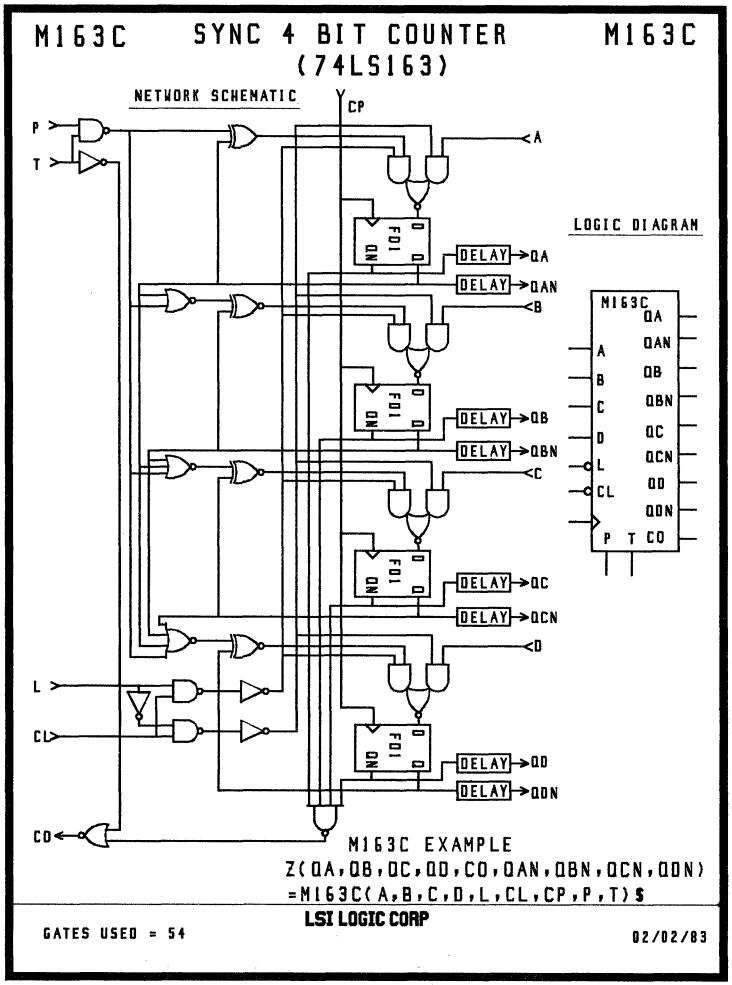

M160D SYNC 4 BIT BCD COUNTER M160D
(74LS160)
NETWORK SCHEMATIC
LOGIC DIAGRAM
M160D EXAMPLE
Z(QA,QB,QC,QD,CO)=M160D(A,B,C,D,L,CP,CD,P,T)$
LSI LOGIC CORP
GATES USED = 50
03/08/83

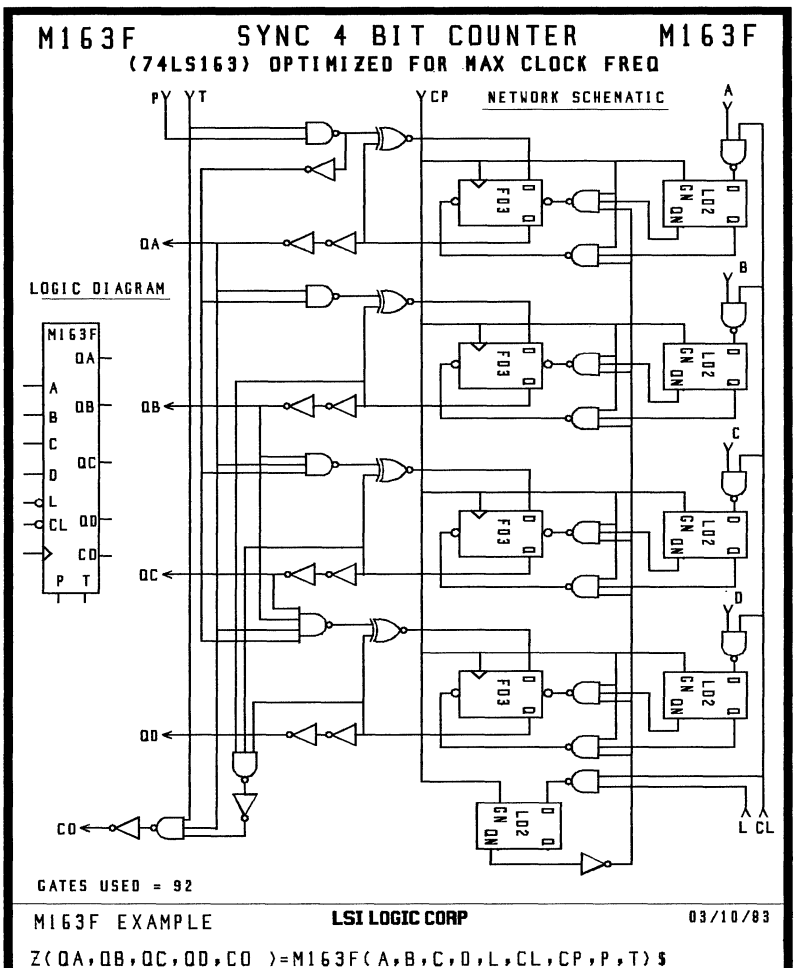

M161C SYNC 4 BIT COUNTER M161C
(74LS161)
NETWORK SCHEMATIC
LOGIC DIAGRAM
M161C EXAMPLE
Z(QA,QB,QC,QD,CO,QAN,QBN,QCN,QDN)
=M161C(A,B,C,D,L,CP,P,T,CD)$
LSI LOGIC CORP
GATES USED = 54
02/18/83

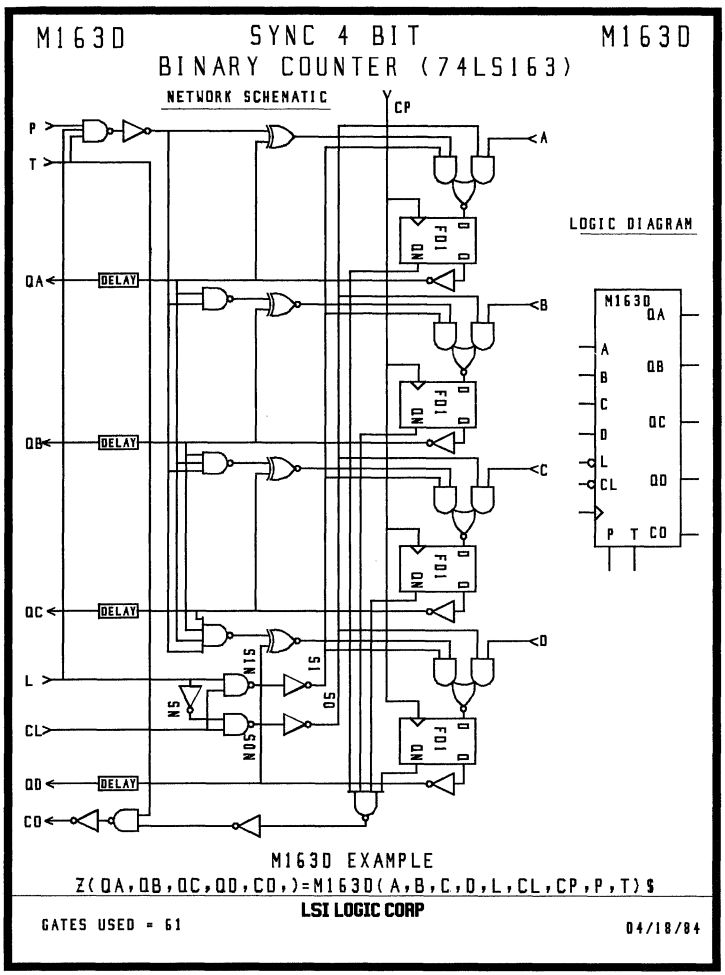

M162C SYNC 4 BIT BCD COUNTER M162C
(74LS162)
NETWORK SCHEMATIC
LOGIC DIAGRAM
M162C EXAMPLE
Z(QA,QB,QC,QD,CO,QAN,QBN,QCN,QDN)
=M162C(A,B,C,D,L,CL,CP,P,T)$
LSI LOGIC CORP
GATES USED = 55
02/18/83


M161D SYNC 4 BIT BCD COUNTER M161D
(74LS161)
NETWORK SCHEMATIC
LOGIC DIAGRAM
M161D EXAMPLE
Z(QA,QB,QC,QD,CO)=M161D(A,B,C,D,L,CP,P,T,CD)$
LSI LOGIC CORP
GATES USED = 60
03/29/83


M162D SYNC 4 BIT BCD COUNTER M162D
(74LS162)
NETWORK SCHEMATIC
LOGIC DIAGRAM
M162D EXAMPLE
Z(QA,QB,QC,QD,CO)=M162D(A,B,C,D,L,CL,CP,P,T)$
GATES USED = 62
LSI LOGIC CORP
03/08/83

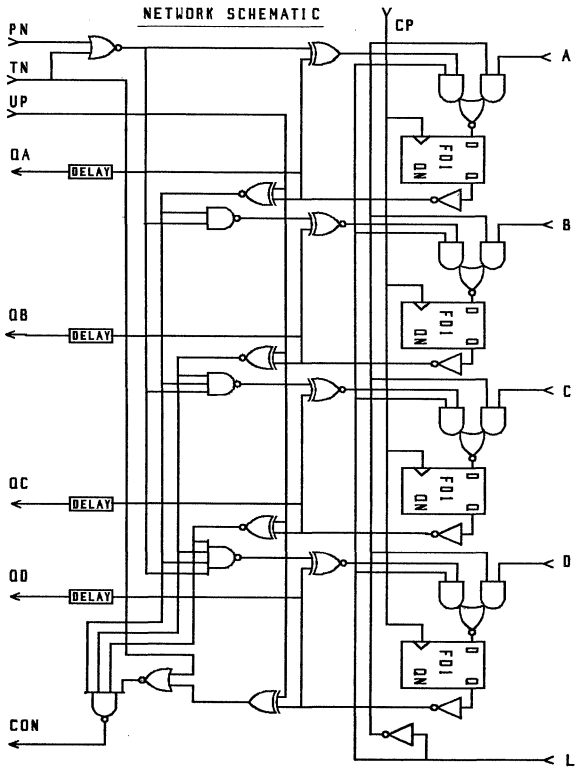

M163C SYNC 4 BIT COUNTER M163C
(74LS163)
NETWORK SCHEMATIC
LOGIC DIAGRAM
M163C EXAMPLE
Z(QA,QB,QC,QD,CO,QAN,QBN,QCN,QDN)
=M163C(A,B,C,D,L,CL,CP,P,T)$
GATES USED = 54
LSI LOGIC CORP
02/02/83


M163F SYNC 4 BIT COUNTER M163F
(74LS163) OPTIMIZED FOR MAX CLOCK FREQ
NETWORK SCHEMATIC
LOGIC DIAGRAM
M163F
GATES USED = 92
M163F EXAMPLE
LSI LOGIC CORP
03/10/83
Z(QA,QB,QC,QD,CO)=M163F(A,B,C,D,L,CL,CP,P,T)$

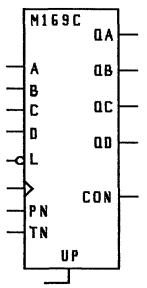

M163D SYNC 4 BIT M163D
BINARY COUNTER (74LS163)
NETWORK SCHEMATIC
LOGIC DIAGRAM
M163D
M163D EXAMPLE
Z(QA,QB,QC,QD,CO,)=M163D(A,B,C,D,L,CL,CP,P,T)$
GATES USED = 61
LSI LOGIC CORP
04/18/84

M169C 4 BIT U/D COUNTER M169C
(74LS169)

NETWORK SCHEMATIC



LOGIC DIAGRAM



M169C EXAMPLE

Z(QA,QB,QC,QD,CON)=M169C(A,B,C,D,L,CP,PN,TN,UP)$

LSI LOGIC CORP

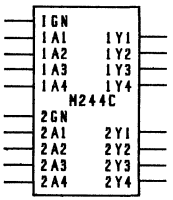
GATES USED = 65

03/10/83

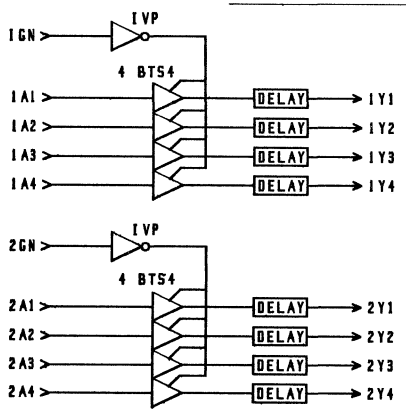
M244C M244C

DUAL 4 BIT TRISTATE BUFFER
ON CHIP

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



M244C EXAMPLE

Z(1Y1,1Y2,1Y3,1Y4,2Y1,2Y2,2Y3,2Y4) = M244C
(1A1,1A2,1A3,1A4,2A1,2A2,2A3,2A4,1GN,2GN)$

LSI LOGIC CORP

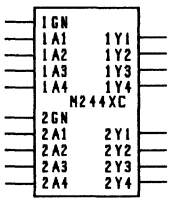
GATES USED = 24

03/11/83

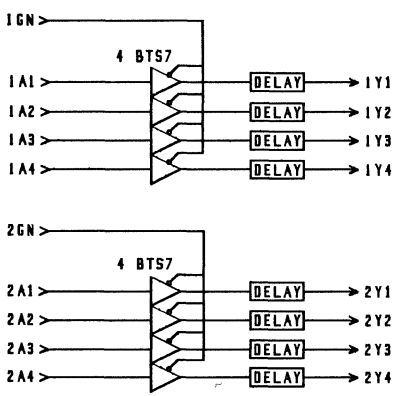
M244XC M244XC

DUAL 4 BIT TRISTATE OUTPUT BUFFER OFF CHIP

LOGIC DIAGRAM



ELECTRICAL SCHEMATIC



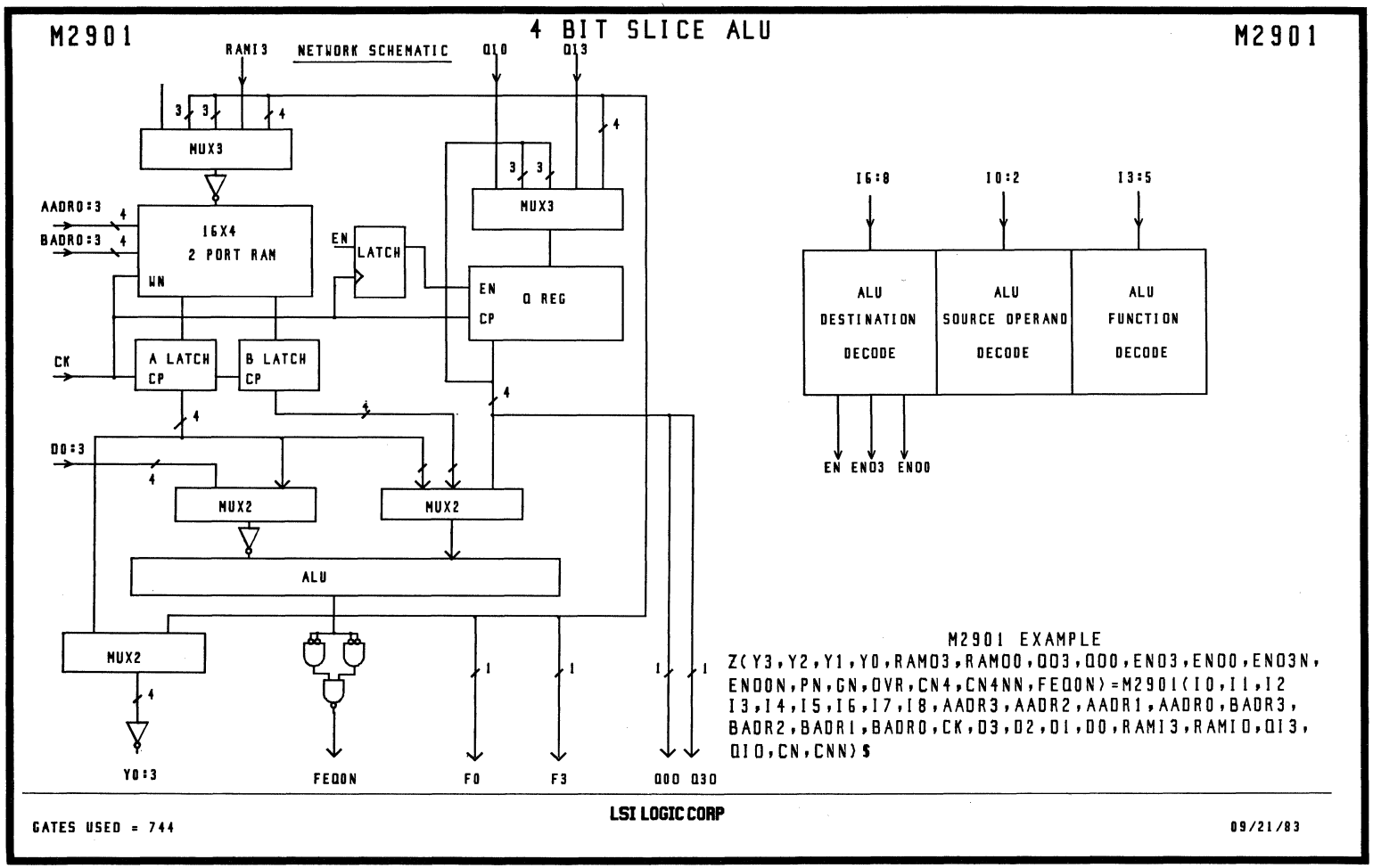
M244XC EXAMPLE

Z(1Y1,1Y2,1Y3,1Y4,2Y1,2Y2,2Y3,2Y4) = M244XC
(1A1,1A2,1A3,1A4,2A1,2A2,2A3,2A4,1GN,2GN)$

LSI LOGIC CORP

GATES USED = 56

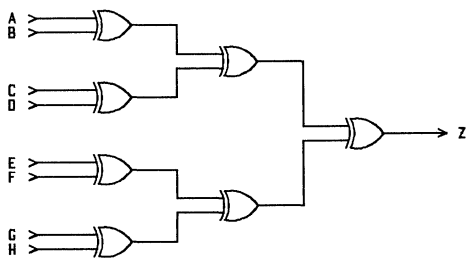
03/11/83


M2901
4 BIT SLICE ALU
M2901
NETWORK SCHEMATIC
RAM3
Q10
Q13
MUX3
MUX3
AADR0:3
BADR0:3
16X4
2 PORT RAM
WN
EN
LATCH
EN
Q REG
CP
CK
A LATCH
CP
B LATCH
CP
D0:3
MUX2
MUX2
ALU
MUX2
Y0:3
FEQ0N
F0
F3
Q00 Q30
I6:8
I0:2
I3:5
ALU
DESTINATION
DECODE
ALU
SOURCE OPERAND
DECODE
ALU
FUNCTION
DECODE
EN EN03 EN00
M2901 EXAMPLE
Z(Y3,Y2,Y1,Y0,RAM03,RAM00,Q03,Q00,EN03,EN00,EN03N,
EN00N,PN,GN,OVR,CN4,CN4NN,FEQ0N)=M2901(I0,I1,I2
I3,I4,I5,I6,I7,I8,AADR3,AADR2,AADR1,AADR0,BADR3,
BADR2,BADR1,BADR0,CK,D3,D2,D1,D0,RAM13,RAM10,Q13,
Q10,CN,CNN)$
LSI LOGIC CORP
GATES USED = 744
09/21/83

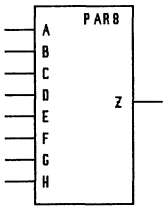
PAR8 PAR8

8 BIT ODD PARITY DETECTOR

NETWORK SCHEMATIC



LOGIC DIAGRAM



IF NUMBER OF TRUE
(1) INPUTS IS ODD,
THEN Z = 1.

PAR8 EXAMPLE
Y(Z) = PAR8(A,B,C,D,E,F,G,H)$

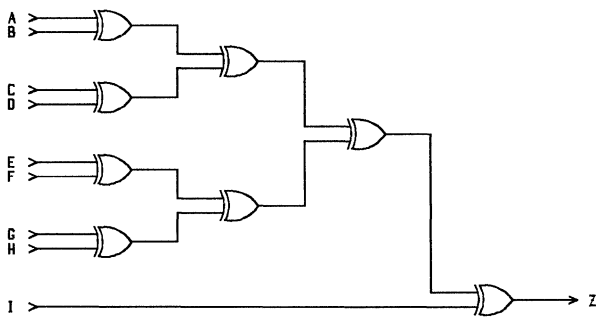
LSI LOGIC CORP

GATES USED = 21 02/21/83

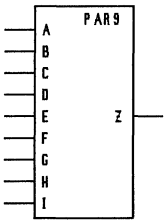
PAR9 PAR9

9 BIT ODD PARITY DETECTOR

NETWORK SCHEMATIC



LOGIC DIAGRAM



IF NUMBER OF TRUE
(1) INPUTS IS ODD,
THEN Z = 1.

PAR9 EXAMPLE
Y(Z) = PAR9(A,B,C,D,E,F,G,H,I)$

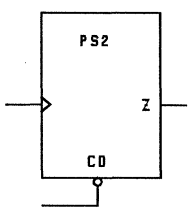
LSI LOGIC CORP

GATES USED = 24 02/21/83

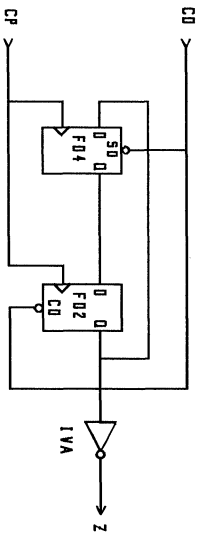
PS2 PS2

DIVIDE BY 2 EXTERNAL CLOCK PRESCALER
WITH NO INPUT PROTECTION

LOGIC DIAGRAM



NETWORK SCHEMATIC



PS2 EXAMPLE
Z = PS2(CP,CO)$

GATES USED = 13

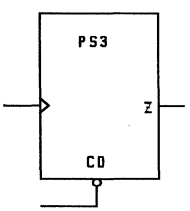
LSI LOGIC CORP

05/11/83

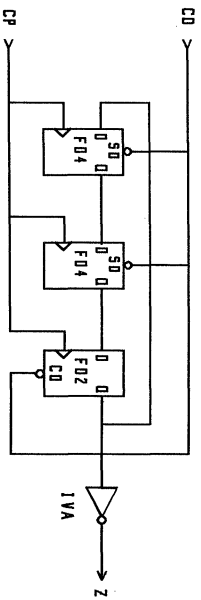
PS3 PS3

DIVIDE BY 3 EXTERNAL CLOCK PRESCALER
WITH NO INPUT PROTECTION

LOGIC DIAGRAM



NETWORK SCHEMATIC



PS3 EXAMPLE
Z = PS2(CP,CO)$

GATES USED = 19

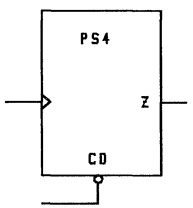
LSI LOGIC CORP

05/11/83

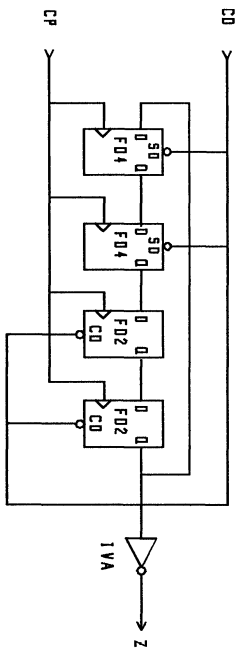
PS4 PS4

DIVIDE BY 4 EXTERNAL CLOCK PRESCALER WITH NO INPUT PROTECTION

LOGIC DIAGRAM



NETWORK SCHEMATIC



PS4 EXAMPLE

Z = PS2(CP,CD)$

GATES USED = 25

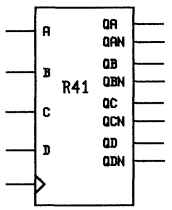
LSI LOGIC CORP

05/11/83

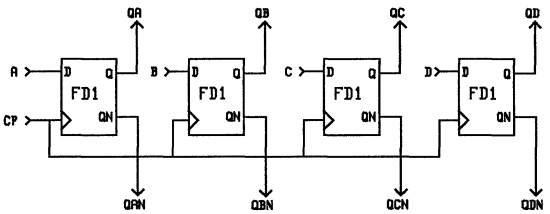
R41 R41

4 BIT DATA REGISTER

LOGIC DIAGRAM



NETWORK SCHEMATIC



R41 EXAMPLE

Z(QA,QAN,QB,QBN,QC,QCN,QD,QDN)=R41(A,B,C,D,CP)$

GATES USED = 20

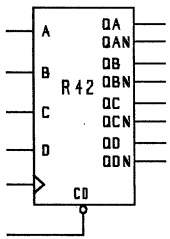
LSI LOGIC CORP

02/01/83

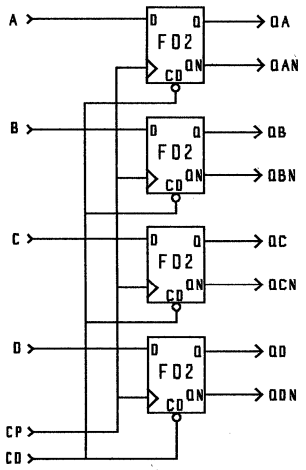
R42 R42

4 BIT DATA REGISTER, CLEAR DIRECT

LOGIC DIAGRAM



NETWORK SCHEMATIC



R42 EXAMPLE

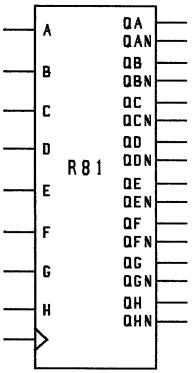
Z(QA,QAN,QB,QBN,QC,QCN,QD,QDN)=R42(A,B,C,D,CP,CD)$

LSI LOGIC CORP

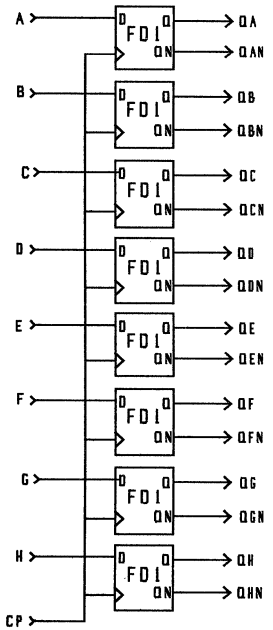
GATES USED = 24 02/01/83

R81 8 BIT DATA REGISTER R81

LOGIC DIAGRAM



NETWORK SCHEMATIC



R81 EXAMPLE

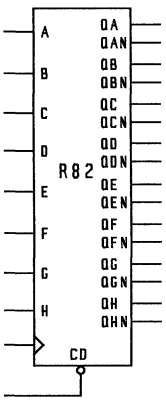
Z(QA,QAN,QB,QBN,QC,QCN,QD,QDN,QE,QEN,QF,QFN,QG,QGN,
QH,QHN)=R81(A,B,C,D,E,F,G,H,CP)$

LSI LOGIC CORP

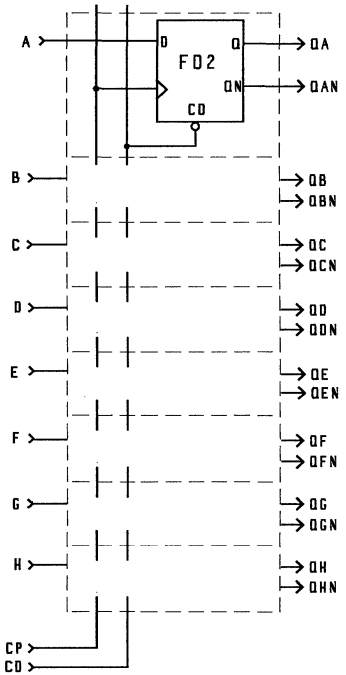
GATES USED = 40 02/01/83

R82 8 BIT DATA REGISTER, CLEAR DIRECT R82

LOGIC DIAGRAM



NETWORK SCHEMATIC



R82 EXAMPLE

Z(QA,QAN,QB,QBN,QC,QCN,QD,QDN,QE,QEN,QF,QFN,QG,QGN, QH,QHN)=R82(A,B,C,D,E,F,G,H,CP,CD)$

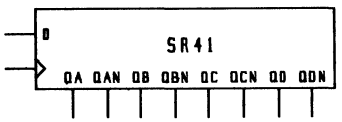
LSI LOGIC CORP

GATES USED = 48

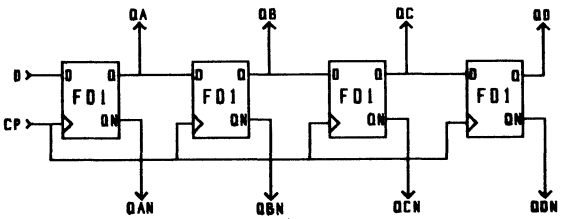
05/11/83

SR41 4 BIT SHIFT REGISTER SR41

LOGIC DIAGRAM



NETWORK SCHEMATIC



SR41 EXAMPLE

Z(QA,QAN,QB,QBN,QC,QCN,QD,QDN)=SR41(D,CP)$

LSI LOGIC CORP

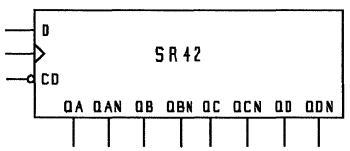
GATES USED = 20

03/11/83

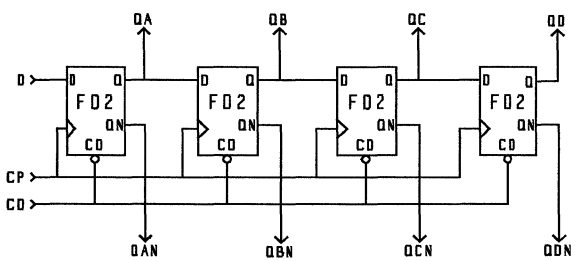
SR42 SR42

4 BIT SHIFT REGISTER, CLEAR DIRECT

LOGIC DIAGRAM



NETWORK SCHEMATIC



SR42 EXAMPLE
Z(QA,QAN,QB,QBN,QC,QCN,QD,QDN)=SR42(D,CP,CD)$

LSI LOGIC CORP

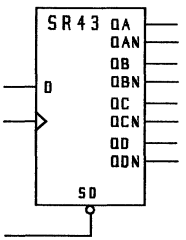
GATES USED = 24

02/01/83

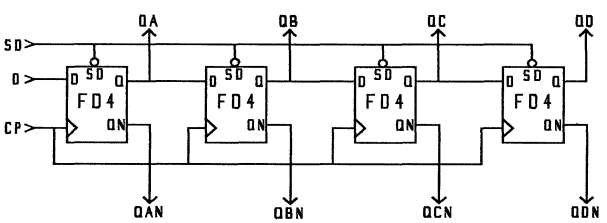
SR43 SR43

4 BIT SHIFT REGISTER, SET DIRECT

LOGIC DIAGRAM



NETWORK SCHEMATIC



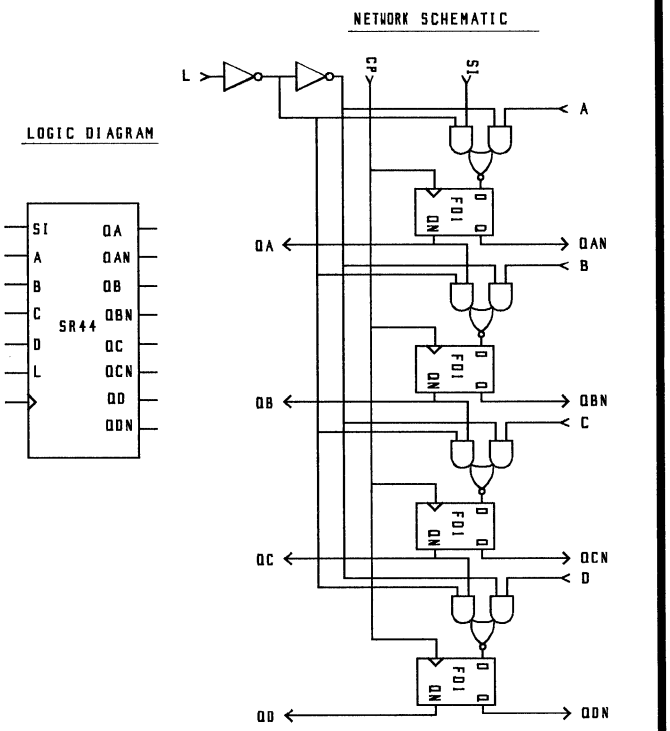
SR43 EXAMPLE
Z(QA,QAN,QB,QBN,QC,QCN,QD,QDN)=SR43(D,CP,SD)$

LSI LOGIC CORP

GATES USED = 24

07/06/83

SR44 4 BIT SHIFT REGISTER, SR44
SYCHRONOUS PARALLEL LOAD



SR44 EXAMPLE

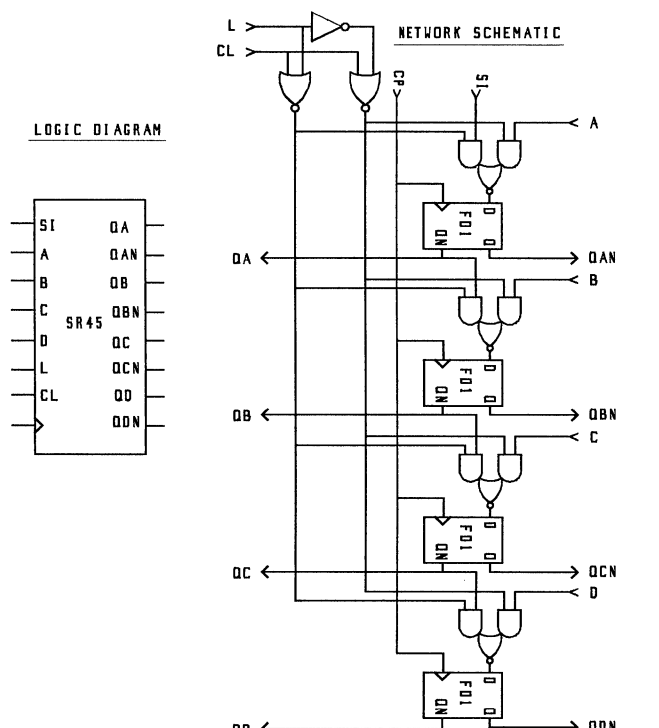
Z(QA,QAN,QB,QBN,QC,QCN,QD,QDN)=SR44(SI,A,B,C,D,L,CP)$

GATES USED = 29

LSI LOGIC CORP

02/01/83

SR45 4 BIT SHIFT REGISTER, SR45
SYCHRONOUS PARALLEL LOAD AND CLEAR



SR45 EXAMPLE

Z(QA,QAN,QB,QBN,QC,QCN,QD,QDN)=SR45
(SI,A,B,C,D,L,CL,CP)$

GATES USED = 31

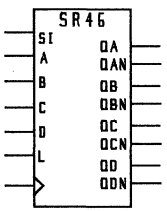
LSI LOGIC CORP

02/02/83

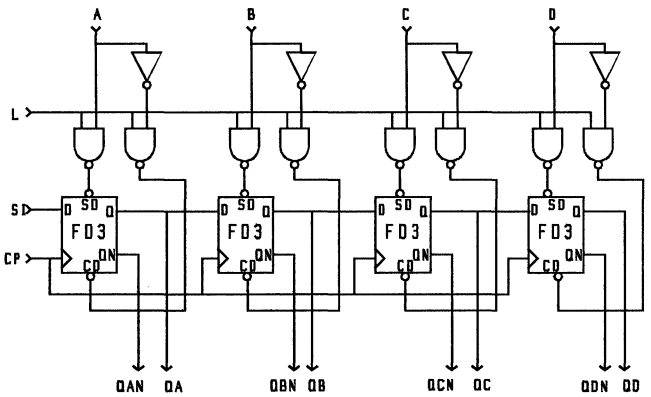
SR46 SR46

4 BIT SHIFT REGISTER
ASYNCHONOUS PARALLEL LOAD

LOGIC DIAGRAM



NETWORK SCHEMATIC



SR46 EXAMPLE

Z(QA,QAN,QB,QBN,QC,QCN,QD,QDN)=SR46(SI,A,B,C,D,L,CP)$

LSI LOGIC CORP

GATES USED = 40

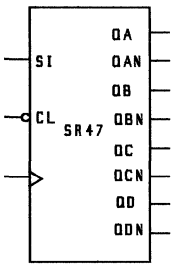
02/01/83

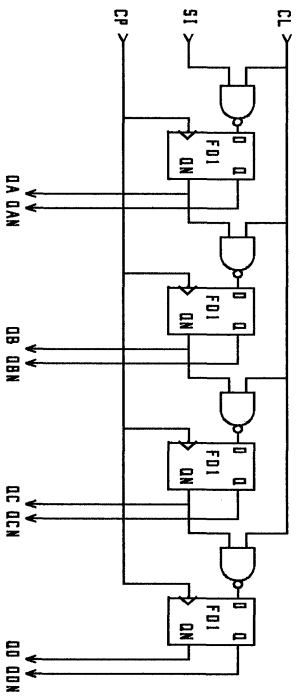
SR47 SR47

4 BIT SHIFT REGISTER, SYNC CLEAR

NETWORK SCHEMATIC

LOGIC DIAGRAM





SR47 EXAMPLE

Z(QA,QAN,QB,QBN,QC,QCN,QD,QDN)=SR47(SI,CL,CP)$

LSI LOGIC CORP

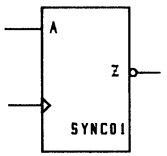
GATES USED = 24

03/17/83

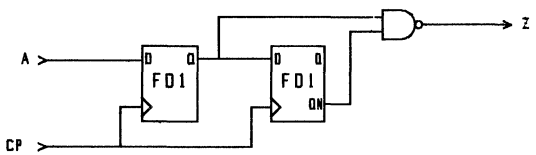
SYNC01 SYNC01

SYNCHRONIZER FOR ASYNCHRONOUS 0 TO 1 EVENT

LOGIC DIAGRAM



NETWORK SCHEMATIC



SYNC01 EXAMPLE
Z=SYNC01(A,CP)$

GATES USED = 11

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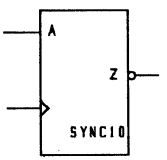
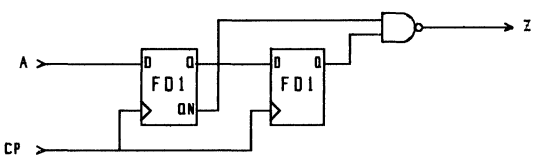
SYNC10 SYNC10

SYNCHRONIZER FOR ASYNCHRONOUS 1 TO 0 EVENT

LOGIC DIAGRAM



NETWORK SCHEMATIC



SYNC10 EXAMPLE
Z=SYNC10(A,CP)$

GATES USED = 11

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