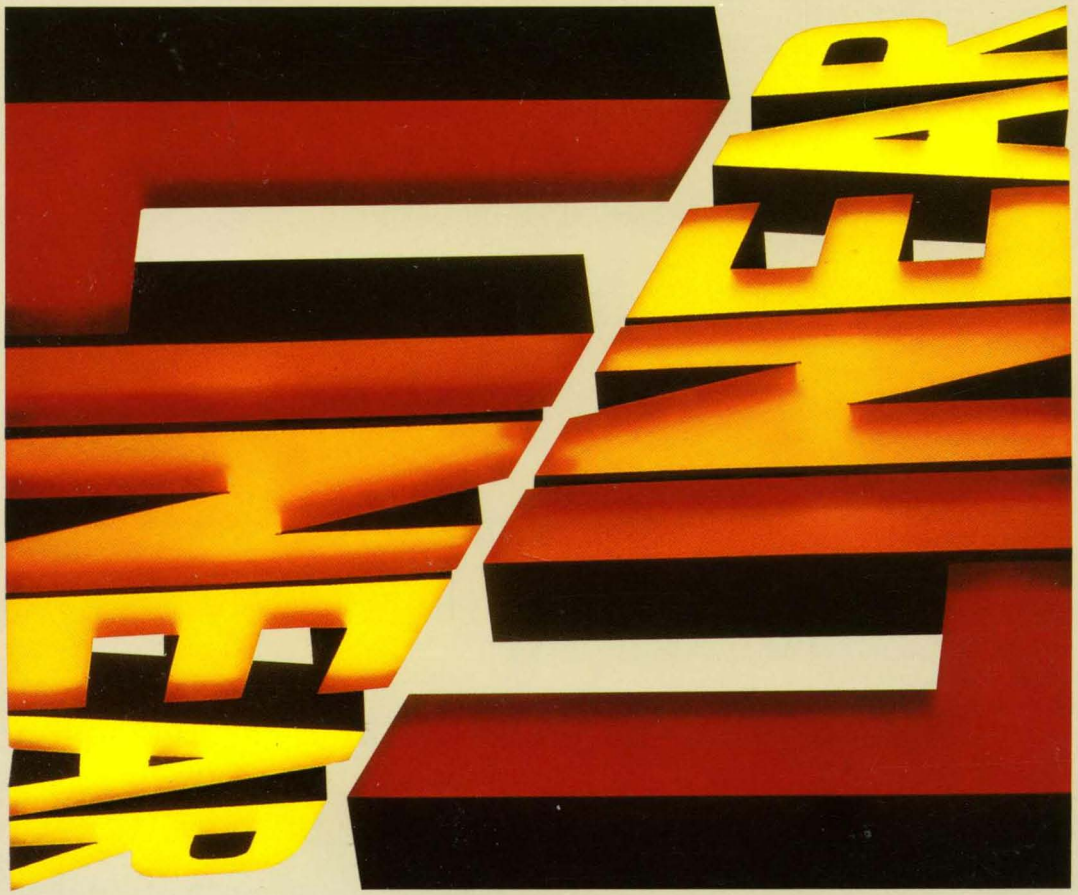
LINEAR TECHNOLOGY

1997
Linear Applications Handbook
Volume III

A Guide to Linear Circuit Design



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1997 Linear Applications Handbook • Volume III

Linear Technology Corporation

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INTRODUCTION

Quality, Efficiency and Style

The title above describes characteristics we seek in our application publications. This fourth* edition of the Linear Applications Handbook includes our latest attempts at instilling these traits into LTC literature. The 1990 edition's introduction described the justification and approach for LTC's application effort in significant detail. It is recommended as a guide to using all LTC application notes, regardless of publication date. As such, its essence is included in this edition. The trio of descriptives forming this section's title heavily abbreviates what has been said, while adding additional perspective.

Quality, in particular good quality, is obviously desirable in any publication. A high quality application note requires attentive circuit design, thorough laboratory technique, and completeness in its description. Text and figures should be thoughtfully organized and presented, visually pleasing, and easy to read. The artwork and printing should maintain this care in the form of clean text appearance and easily readable graphics.

Application notes should also be efficient. An efficiently written note permits the reader to access desired information quickly, and in readily understandable form. There should be enough depth to satisfy intellectual rigor, but the reader should not need an academic bathyscaphe to get to the bottom of things. Above all, the purpose is to communicate useful information clearly and quickly.

Finally, style should always show. Too much technical literature is dull reading. We enjoy our work, and we want to share our enthusiasm. Quite simply, we want our publications to be fun to read. An LTC author's ultimate fantasy features the reader at home in the living room; relaxed, smiling, and reading (while writing down LTC part numbers to buy). Style provides psychological lubrication, helping the mind to run smoothly. Clearly, style must only assist the serious purposes of publication and should not be abused; we do our best to maintain the appropriate balance.

As noted in previous editions a number of people besides authors make this work possible. As always, the final acknowledgement must go to our customers, who define our work, products, and company. We hope they are pleased with our latest efforts.

James M. Williams
January, 1997
Milpitas, California

* Previous editions appeared in 1987, 1990 and 1993. This edition includes only material generated since the 1993 edition. As such, don't throw those other books away!

1990 INTRODUCTION

Why Write Applications?

This is seemingly an odd and unlikely way to begin an applications publication, but it is a valid question. As such, the components of the decision to produce this book are worth reviewing.

Producing linear application material requires an intensive, extended effort. Development costs for worthwhile material are extraordinarily high, absorbing substantial amounts of engineering time and money. Further, these same resources could be directed towards product development, the contribution of which is much more easily measured at the corporate coffers. These are serious issues in any environment, but are particularly critical in a rapidly growing company, where resources must be thoughtfully allocated.

Linear Technology Corporation's commitment to a concerted applications effort was made despite these concerns. Specifically, the nature of linear circuit design is so diverse, the devices so sophisticated, and user requirements so demanding that designers require (or at least welcome) assistance. Ultimately, the procurement and use of linear ICs is tied to the user's ability to solve the problems confronting them. Anything which enhances this ability, in both specific and general cases, obviously benefits user and vendor.

This is a very simple but powerful argument, and is the basis of LTC's commitment to applications. Additional benefits include occasional new product concepts and a way to test products under "real world" conditions, but the basic justification is as described.

Traditionally, application work has involved reviewing considerations for successful use of a specific product. Additionally, basic circuit suggestions or concepts are sometimes offered. Although this approach is useful and necessary, some expansion is possible. LTC's applications are centered on detailed, systems-oriented circuits, (hopefully) similar to the types of designs users are working with. There is a broad tutorial content, reflected in the form of frequent text digressions and liberal use of graphics. Discussions of tradeoffs, options and techniques are emphasized, as opposed to brief descriptions of circuit operation. Many of the application notes contain appended sections which examine related or pertinent topics in detail. Ideally, this treatment provides enough background to allow readers to modify the circuits presented into solutions to their specific problems.

Some comment about the circuit examples is appropriate. They range from relatively simple to quite complex and sophisticated. Emphasis is on high performance, in keeping with the capabilities of LTC's products and the market we serve. The circuit's primary function is to serve as a catalyst—once the reader has started thinking, the material has accomplished its mission.

Substantial effort has been expended in working out and documenting these circuits, but they are not finessed to the highest possible degree. All of the circuits have been breadboarded and bench-tested at the prototype level. Specifications and performance levels quoted in the text represent measured and extrapolated data derived from the breadboard prototype. The volume of material generated prohibits formal worst-case review or tolerances analysis for production. Additionally, despite our best efforts, errors of various sorts do occasionally creep in along the way to publication. Because of these considerations, readers should contact LTC when preparing to use a circuit in a production situation. This allows us to advise on specific areas of the circuit which may require a "second look" before going to production. Updates, suggested modifications and just plain mistakes can also be discussed at this time.

We have received numerous comments and questions since this book's first (1987) edition. The most frequent query concerns topic selection. The topics presented are survivors of a selection process involving a number of disparate considerations. These include reader needs, suitability for magazine publication, LTC's short and long term commercial aspirations, time constraints and author interest in doing the work. Additionally, we seek a 10 year useful lifetime for application notes. This generally precludes narrowly focused effort towards individual ICs. Topics are broad, with a tutorial and design emphasis that (ideally) reflects the reader's long term interests. While the circuits presented unabashedly favor our products, they must be conceptually applicable to succeeding generations of devices (hopefully ours). Similarly, the circuits should represent a relatively complete and interdisciplinary approach to solving the problem at hand. Solving a problem is usually the reader's/customer's overwhelming motivation. The selection and integration of tools and methods towards this end is *the* priority. For this reason the examples and accompanying text are as complete and practical as possible. This may necessitate effort in areas where we have no direct economic stake, e.g., the software presented in AN28 or the magnetics developed for AN25, AN29, and AN35. In some circumstances this policy necessitates use of competitor's products (horrors!) where appropriate. Such gallant objectivity is not without calculation; the goal is to have readers associate LTC with realistic advice, useful products and satisfactory results, regardless of the problem encountered. The long term task is establishing and maintaining credibility and customer loyalty. If unabused, these are powerful sales tools. Maintaining this stance involves a significant amount of negotiation and compromise with issues and individuals, but the results are usually favorable for everyone.

A second common question addresses the time required to produce an individual application note. The work invested varies considerably. AN29 required a year to complete. It involved endless laboratory hours, close coordination with our magnetics supplier and over 300 changes, corrections, band-aids and tweaks before the manuscript was finally released. Conversely, AN31 and AN32 were finished (perhaps therapeutically) within three weeks. In all cases the actual writing time is a miniscule percentage of the total work time. AN29's year of effort was written up in a week. AN31 and AN32 required less than five hours.

Another common question involves our photographic documentation. We have received hundreds of inquiries requesting details on instrumentation, particularly for

multi-trace oscilloscope photography. Almost all photographic work is done with four (Tektronix 547 with a four trace 1A4 plug-in) or eight (Tektronix 556 with two 1A4 plug-ins) trace oscilloscopes. Photographs with more than eight traces utilize multiple exposure or splicing techniques. Tektronix C-12 and C-27 cameras are used on both instruments, with modified graticule illumination on the 556. AN29's Appendix F provides additional discussion.

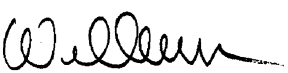
A final recurring question concerns use of this book as text in university level courses. We certainly welcome this, and find it rewarding. However, we cannot develop, or collaborate in the development of, supplementary material for problem sets and laboratory manuals. This simply strays too far from our charter.

Some significant additions since the 1987 edition are the "Design Notes" and the open format used in AN26, AN27 and AN36. "Design Notes" provide a way to cover a specific topic in concise form and get the material to the reader quickly. Most of these notes are stand-alone efforts. In some cases they are excerpted from application note work in progress and fed directly to print. When the application note becomes available, the material appears in unabbreviated form. Another change is the format used for AN26, AN27 and AN36. The segmented approach allows convenient updating and additions at some sacrifice in text flow. Subjects amenable to this treatment avoid the disruptive surgery required to revise a conventional manuscript.

In response to reader requests we have included macromodels of components. The present list includes 28 ICs, all amplifiers. This inventory will grow and diversity into other part types. Significant effort has gone towards making these models realistic and usable. They are intended as powerful adjunct tools in the design process, and should not be abused. More specifically, they are meant to augment actual breadboards, not eliminate them. Bypassing breadboarding is an extraordinarily hazardous process with a high fatality rate, even among veteran designers. Although these macromodels cannot eliminate the cold realities involved in making something work, they ease the task and save time. As such, we encourage readers to use them and invite your comments.

Also new is the inclusion of application notes from other sources. These notes, found in the "Reference Reading" section, have proven particularly useful to readers. The information they contain is pertinent to problem areas that concern our readers. As such, they merit inclusion. If this approach is well received this section will be enlarged in succeeding editions. The cooperation of the contributors is appreciated.

Finally, the appearance of new authors is applauded, particularly by the undersigned. There is plenty of work to do and many pens (and probes) ease the task while broadening perspective.



James M. Williams
November, 1989
Milpitas, California

SECTION 1—APPLICATION NOTES

Note: All publications in **BOLD** are in this Applications Handbook, others appear in LTC's 1990 and 1993 Linear Applications Handbooks ('90HB = LTC's 1990 Linear Applications Handbook and '93HB = LTC's 1993 Linear Applications Handbook).

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SECTION 2—DESIGN NOTES

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SECTION 3—REFERENCE READING

SECTION 3 of 1993 Linear Applications Handbook—REFERENCE READING

SECTION 3 of 1990 Linear Applications Handbook—MACROMODELS

Note: All publications in **BOLD** are in this Applications Handbook, others appear in LTC's 1990 and 1993 Linear Applications Handbooks ('90HB = LTC's 1990 Linear Applications Handbook and '93HB = LTC's 1993 Linear Applications Handbook).

SECTION 4 of 1990 Linear Applications Handbook—REFERENCE READING

Note: All publications in **BOLD** are in this Applications Handbook, others appear in LTC's 1990 and 1993 Linear Applications Handbooks ('90HB = LTC's 1990 Linear Applications Handbook and '93HB = LTC's 1993 Linear Applications Handbook).

1990 EDITION APPLICATION NOTE ABSTRACTS

AN1 **Understanding and Applying the LT1005 Multifunction Regulator**
This application note describes the unique operating characteristics of the LT1005 and describes a number of useful applications which take advantage of the regulator's ability to control the output with a logic control signal.

AN2 **Performance Enhancement Techniques for 3-Terminal Regulators**
This application note describes a number of enhancement circuit techniques used with existing 3-terminal regulators which extend current capability, limit power dissipation, provide high voltage output, operate from 110VAC or 220VAC without the need to switch transformer windings, and many other useful application ideas.

AN3 **Applications for a Switched-Capacitor Instrumentation Building Block**
This application note describes a wide range of useful applications for the LTC1043 dual precision instrumentation switched-capacitor building block. Some of the applications described are ultra high performance instrumentation amplifier, lock-in amplifier, wide range digitally controlled variable gain amplifier, relative humidity sensor signal conditioner, LVDT signal conditioner, charge pump F/V and V/F converters, 12-bit A/D converter and more.

AN4 **Application for a New Power Buffer**
The LT1010 150mA power buffer is described in a number of useful applications such as boosted op amp, a feed-forward, wide-band DC stabilized buffer, a video line driver amplifier, a fast sample-hold with hold step compensation, an overload protected motor speed controller, and a piezoelectric fan servo.

AN5 **Thermal Techniques in Measurement and Control Circuitry**
6 applications utilizing thermally based circuits are detailed. Included are a 50MHz RMS to DC converter, and anemometer, a liquid flowmeter and others. A general discussion of thermodynamic considerations involved in circuitry is also presented.

AN6 **Applications of New Precision Op Amps**
Application considerations and circuits for the LT1001 and LT1002 single and dual precision amplifiers are illustrated in a number of circuits, including strain gauge signal conditioners, linearized platinum RTD circuits, an ultra precision dead zone circuit for motor servos and other examples.

AN7 **Some Techniques for Direct Digitization of Transducer Outputs**
Analog-to-digital conversion circuits which directly digitize low level transducer outputs, without DC preamplification, are presented. Covered are circuits which operate with thermocouples, strain gauges, humidity sensors, level transducers and other sensors.

AN8 **Power Conditioning Techniques for Batteries**
A variety of approaches for power conditioning batteries is given. Switching and linear regulators and converters are shown, with attention to efficiency and low power operation. 14 circuits are presented with performance data.

AN9 **Application Considerations and Circuits for a New Chopper-Stabilized Op Amp**
A discussion of circuit, layout and construction considerations for low level DC circuits includes error analysis of solder, wire and connector junctions. Applications include sub-microvolt instrumentation and isolation amplifiers, stabilized buffers and comparators and precision data converters.

AN10 **Methods for Measuring Op Amp Settling Time**
The AN10 begins with a survey of methods for measuring op amp settling time. This commentary develops into circuits for measuring settling time to 0.0005%. Construction details and results are presented. Appended sections cover oscilloscope overload limitations and amplifier frequency compensation.

AN11 **Designing Linear Circuits for 5V Operation**
This note covers the considerations for designing precision linear circuits which must operate from a single 5V supply. Applications include various transducer signal conditioners, instrumentation amplifiers, controllers and isolated data converters.

AN12 **Circuit Techniques for Clock Sources**
Circuits for clock sources are presented. Special attention is given to crystal-based designs including TXCOs and VXCOs.

AN13 **High Speed Comparator Techniques**
The AN13 is an extensive discussion of the causes and cures of problems in very high speed comparator circuits. A separate applications section presents circuits, including a 0.025% accurate 1Hz to 30MHz V/F converter, a 200ns 0.01% sample-hold and a 10MHz fiber-optic receiver. Five appendices covering related topics complete this note.

AN14 **Designs for High Frequency Voltage-to-Frequency Converters**
A variety of high performance V/F circuits is presented. Included are a 1Hz to 100MHz design, a quartz-stabilized type and a 0.0007% linear unit. Other circuits feature 1.5V operation, sine wave output an nonlinear transfer functions. A separate section examines the trade-offs and advantages of various approaches to V/F conversion.

AN15 **Circuitry for Single Cell Operation**
1.5V powered circuits for complex linear functions are detailed. Designs include a V/F converter, a 10-bit A/D, sample-hold amplifiers, a switching regulator and other circuits. Also included is a section of component considerations for 1.5V powered linear circuits.

AN16 **Unique IC Buffer Enhances Op Amp Designs, Tames Fast Amplifiers**
This note describes some of the unique IC design techniques incorporated into a fast, monolithic power buffer, the LT1010. Also, some application ideas are described such as capacitive load driving, boosting fast op amp output current and power supply circuits.

AN17 **Consideration for Successive Approximation A/D Converters**
A tutorial on SAR type A/D converters, this note contains detailed information on several 12-bit circuits. Comparator, clocking, and preamplifier designs are discussed. A final circuit gives a 12-bit conversion in 1.8μs. Appended sections explain the basic SAR technique and explore D/A considerations.

AN18 **Power Gain Stages for Monolithic Amplifiers**
This note presents output state circuits which provide power gain for monolithic amplifiers. The circuits feature voltage gain, current gain, or both. Eleven designs are shown, and performance is summarized. A generalized method for frequency compensation appears in a separate section.

AN19 **LT1070 Design Manual**
This design manual is an extensive discussion of all standard switching configurations for the LT1070; including buck, boost, flyback, forward, inverting and "Cuk." The manual includes comprehensive information on the LT1070, the external components used with it, and complete formulas for calculating component values.

AN20 **Applications for a DC Accurate Lowpass Switched-Capacitor Filter**
Discusses the principles of operation of the LTC1062 and helpful hints for its application. Various application circuits are explained in detail with focus on how to cascade two LTC1062s and how to obtain notches. Noise and distortion performance are fully illustrated.

AN21 **Composite Amplifiers**
Applications often require an amplifier that has extremely high performance in several areas. For example, high speed and DC precision are often needed. If a single device cannot simultaneously achieve the desired characteristics, a composite amplifier made up of two (or more) devices can be configured to do the job. AN21 shows examples of composite approaches in designs combining speed, precision, low noise and high power.

AN22 **A Monolithic IC for 100MHz RMS/DC Conversion**
AN22 details the theoretical and application aspects of the LT1088 thermal RMS/DC converter. The basic theory behind thermal RMS/DC conversion is discussed and design details of the LT1088 are presented. Circuitry for RMS/DC converters, wide-band input buffers and heater protection is shown.

AN23 **Micropower Circuits for Signal Conditioning**
Low power operation of electronic apparatus has become increasingly desirable. AN23 describes a variety of low power circuits for transducer signal conditioning. Also included are designs for data converters and switching regulators. Three appended sections discuss guidelines for micropower design, strobed power operation and effects of test equipment on micropower circuits.

AN24 **Unique Applications for the LTC1062 Lowpass Filter**
Highlights the LTC1062 as a lowpass filter in a phase lock loop. Describes how the loop's bandwidth can be increased and the VCO output jitter reduced when the LTC1062 is the loop filter. Compares it with a passive RC loop filter.

Also discussed is the use of LTC1062 as simple bandpass and bandstop filter.

AN25 **Switching Regulators for Poets**
Subtitled "A Gentle Guide for the Trepidatious," this is a tutorial on switching regulator design. The text assumes no switching regulator design experience, contains no equations, and requires no inductor construction to build the circuits described.

Designs detailed include flyback, isolated telecom, off-line, and others. Appended sections cover component considerations, measurement techniques and steps involved in developing a working circuit.

AN26 A collection of interface applications between various microprocessors/controllers and the LTC1090 family of data acquisition systems. The note is divided into sections specific to each interface. The following sections are available:

Number	A/D	Microprocessor/ Microcontroller
AN26A	LTC1090	8051
AN26B	LTC1090	68HC05
AN26C	LTC1090	63705
AN26D	LTC1090	COP820
AN26E	LTC1090	TMS7742
AN26F	LTC1090	COP402N
AN26G	LTC1091	8051
AN26H	LTC1091	68HC05
AN26I	LTC1091	COP820
AN26J	LTC1091	TMS7742
AN26K	LTC1091	COP402N
AN26L	LTC1091	HD63705VO
AN26M	LTC1090	TMS320C25
AN26N	LTC1091/92	TMS320C25
AN26O	LTC1090	Z-80
AN26P	LTC1090	HD64180
AN26Q	LTC1091	HD64180
AN26R	LTC1094	TMS320C25

These interface notes demonstrate the ease with which the LTC1090 family can be interfaced to microprocessors/controllers having either parallel or serial ports. A complete hardware and software description of the interface is included.

AN27A **A Simple Method of Designing Multiple Order All Pole Bandpass Filters by Cascading 2nd Order Sections**
Presents two methods of designing high quality switched-capacitor bandpass filters. Both methods are intended to vastly simplify the mathematics involved in filter design by using tabular methods. The text assumed no filter design experience but allows high quality filters to be implemented by techniques not presented before in the literature. The designs are implemented by numerous examples using devices from LTC's Switched-Capacitor filter family: LTC1060, LTC1061, and LATC1064. Butterworth and Chebyshev bandpass filters are discussed.

AN28 **Thermocouple Measurement**
Considerations for thermocouple-based temperature measurement are discussed. A tutorial on temperature sensors summarizes performance of various types, establishing a perspective on thermocouples. Thermocouples are then focused on. Included are sections covering cold-junction compensation, amplifier selection, differential/isolation techniques, protection, and linearization. Complete schematics are given for all circuits. Processor-based linearization is also presented with the necessary software detailed.

AN29 **Some Thoughts on DC/DC Converters**
This note examines a wide range of DC/DC converter applications. Single inductor, transformer, and switched-capacitor converter designs are shown. Special topics like low noise, high efficiency, low quiescent current, high voltage, and wide-input voltage range converters are covered. Appended sections explain some fundamental properties of different types of converters.

AN30 **Switching Regulator Circuit Collection**
Switching regulators are of universal interest. Linear Technology has made a major effort to address this topic. A catalog of circuits has been compiled so that a design engineer can swiftly determine which converter type is best. This catalog serves as a visual index to be browsed through for a specific or general interest.

AN31 **Linear Circuits for Digital Systems**
Subtitled "Some Affable Analogs for Digital Devotees," discusses a number of analog circuits useful in predominantly digital systems. V_{PP} generators for flash memories receive extensive treatment. Other examples include a current loop transmitter, dropout detectors, power management circuits, and clocks.

AN32 **High Efficiency Linear Regulators**
Presents circuit techniques permitting high efficiency to be obtained with linear regulation. Particular attention is given to the problem of maintaining high efficiency with widely varying inputs, outputs and loading. Appendix sections review component characteristics and measurement methods.

AN33 **Converting Light to Digits: LTC1099 Half-Flash 8-Bit A/D Converter Digitizes Photodiode Array**
This application note describes a Linear Technology "Half-Flash" A/D converter, the LTC1099, being connected to a 256 element line scan photodiode array. This technology adapts itself to hand-held (i.e., low power) bar code readers, as well as high resolution automated machine inspection applications.

AN34 **LTC1099 Enables PC-Based Data Acquisition Board to Operate DC-20kHz**
A complete design for a data acquisition card for the IBM PC is detailed in this application note. Additionally, C language code is provided to allow sampling of data at speed of more than 20kHz. The speed limitation is strictly based on the execution speed of the "C" data acquisition loop. A "Turbo" XT can acquire data at speeds greater than 20kHz. Machines with 80286 and 80386 processors can go faster than 20kHz. The computer that was used as a test bed in this application was an XT running at 4.77MHz and therefore all system timing and acquisition time measurements are based on a 4.77MHz clock speed.

AN35 **Step-Down Switching Regulators**
Discusses the LT1074, an easily applied step-down regulator IC. Basic concepts and circuits are described along with more sophisticated applications. Six appended sections cover LT1074 circuitry detail, inductor and discrete component selection, current measuring techniques, efficiency considerations and other topics.

AN36 A collection of interface applications between various microprocessors/controllers and the LTC1290 family of data acquisition systems. The note is divided into sections specific to each interface. The following sections are available:

Number	A/D	Microprocessor/ Microcontroller
AN36A	LTC1290	8051
AN36B	LTC1290	MC68HC05
AN36C	LTC1290/LTC1090	TMS370
AN36D	LTC1290	COP820C
AN36E	LTC1290	TMS7742
AN36F	LTC1290	COP402N
AN36O	LTC1290	Z-80
AN36P	LTC1290	HD64180

These interface notes demonstrate the ease with which the LTC1290 can be interfaced to microprocessors/controllers having either parallel or serial ports. A complete hardware and software description of the interface is included.

AN37 **Fast Charge Circuits for NiCad Batteries**
Safe, fast charging of NiCad batteries is attractive in many applications. This note details simple, thermally-based fast charge circuitry for NiCads. Performance data is summarized and compared to other charging methods.

AN38 **FilterCAD User's Manual, Version 1.00**
This note is the manual for FCAD, a computer-aided design program for designing filters with LTC's switched-capacitor filter family. FCAD helps users design good filters with a minimum amount of effort. The experienced filter designer can use the program to achieve better results by providing the ability to play "what if" with the values and configuration of various components.

AN39 **Parasitic Capacitance Effects in Step-Up Transformer Design**
This note explores the causes of the large resonating current spikes on the leading edge of the switch current waveform. These anomalies are exacerbated in very high voltage designs.

AN40 **Take the Mystery Out of the Switched-Capacitor Filter: The System Designer's Filter Compendium**
This note presents guidelines for circuits utilizing LTC's switched-capacitor filters. The discussion focuses on how to optimize filter performance by optimizing the printed wiring board, the power supply, and the output buffering of the filter. Many additional topics are discussed such as how to select the proper filter response for the application and how to characterize a filter's THD for DSP applications.

1993 EDITION APPLICATION NOTE ABSTRACTS

AN41 **Questions and Answers on the SPICE Macromodel Library**
This note provides answers to some of the more common questions concerning LTC's Macromodel Library. Topics include hardware and software requirements, model characteristics, and limitations and interpretation of results.

AN42 **Voltage Reference Circuit Collection**
A wide variety of voltage reference circuits are detailed in this extensive guidebook of circuits. The detailed schematics cover simple and precision approaches at a variety of power levels. Included are 2 and 3 terminal devices in series and shunt modes for positive and negative polarities. Appended sections cover resistor and capacitor selection and trimming techniques.

AN43 **Bridge Circuits**
Subtitled "Marrying Gain and Balance," this note covers signal conditioning circuits for various types of bridges. Included are transducer bridges, AC bridges, Wien bridge oscillators, Schottky bridges, and others. Special attention is given to amplifier selection criteria. Appended sections cover strain gauge transducers, understanding distortion measurements, and historical perspectives on bridge readout mechanisms and Wein bridge oscillators.

AN44 **LT1074/LT1076 Design Manual**
This note discusses the use of the LT1074 and LT1076 high efficiency switching regulators. These regulators are specifically designed for ease of use. This application note is intended to eliminate the most common errors that customers make when using switching regulators as well as offering insight into the inner workings of switching designs. There is an entirely new treatment of inductor design based upon simple mathematical formulas that yield direct results. There are extensive tutorial sections devoted to the care and feeding of the Positive Step-Down (Buck) Converter, the Tapped Inductor Buck Converter, the Positive-to-Negative Converter and the Negative Boost Converter. Additionally, many troubleshooting hints are included as well as oscilloscope techniques, soft-start architectures, and micropower shutdown and EMI suppression methods.

AN45 **Measurement and Control Circuit Collection**
A variety of measurement and control circuits are included in this application note. Eighteen circuits, including ultra low noise amplifiers, current sources, transducer signal conditioners, oscillators, data converters and power supplies are presented. The circuits emphasize precision specifications with relatively simple configurations.

AN46 **Efficiency Characteristics of Switching Regulator Circuits**
Efficiency varies for different DC/DC converters. This application note compares the efficiency characteristics of some of the more popular types. Step-up, step-down, flyback, negative-to- positive, and positive-to-negative are shown. Appended sections discuss how to select the proper aluminum electrolytic capacitor and explain power switch and output diode loss calculations.

AN47 **High Speed Amplifier Techniques**
This application note, subtitled "A Designer's Companion for Wideband Circuitry," is intended as a reference source for designing with fast amplifiers. Approximately 150 pages and 300 figures cover frequently encountered problems and their possible causes. Circuits include a wide range of amplifiers, filters, oscillators, data converters and signal conditioners. Eleven appended sections discuss related topics including oscilloscopes, probe selection, measurement and equipment considerations, and breadboarding techniques.

AN48 **Using the LTC Op Amp Macromodels**
LTC's op amp macromodels are described in detail, along with the theory behind each model and complete schematics of each topology. Extended modeling topics are discussed, such as phase/frequency response modifications and asymmetric slew rate for JFET op amp models. LTC's macromodels are optimized for accuracy and fast simulation times. Simulation times can be further reduced by using streamlining techniques found throughout AN48.

AN49 **Illumination Circuitry for Liquid Crystal Displays**
Current generation portable computers and instruments utilize backlit liquid crystal displays. The back light requires a highly efficient, high voltage AC source as well as other supply circuitry. AN49 details these circuits and also includes sections on efficiency measurements and instrumentation considerations. A separate section discusses physical and layout considerations for the display.

AN50 **Interfacing to Microprocessor Based 5V Systems**
This application note discusses a variety of approaches for interfacing analog signals to 5V powered systems. Synthesizing a "rail-to-rail" op amp and scaling techniques for A/D converters are covered. A voltage-to-frequency converter, applicable where high resolution is required, is also presented.

AN51 **Power Conditioning for Notebook and Palmtop Systems**
Notebook and palmtop systems need a number of voltages developed from a battery. Competitive solutions require small size, high efficiency and light weight. This publication includes circuits for high efficiency 5V and 3.3V switching and linear regulators, back light display drivers and battery chargers. All the circuits are specifically tailored for the requirements outlined above.

AN52 **Linear Technology Magazine Circuit Collection, Vol 1**
This application note consolidates the circuits from the first few years of Linear Technology Magazine into one publication. Presented in the note are a variety of circuits ranging from a 50W high efficiency (>90%) switching regulator to steep roll-off filter circuits with low distortion to 12-bit differential temperature measurement systems.

AN53 **Micropower High-Side MOSFET Drivers**
This application note describes the operation of high-side N-channel MOSFET switch drivers designed specifically for operation in battery-powered equipment, such as notebook and palmtop computers and portable medical instruments. A selection guide simplifies the proper choice of MOSFET and driver for a particular high-side switch application. Circuits to drive and protect load impedances ranging from large inductors to large capacitors are described and a section on surface mount and copper clad shunts is included.

AN54 **Power Conversion from Milliamps to Amps at Ultra High Efficiency (Up to 95%)**
This application note discusses the use of the LTC1147, LTC1148, and LTC1149 ultra high efficiency switching regulators in a wide variety of applications. These controllers feature a current-mode architecture which includes an automatic low current operating mode called Burst Mode™ operation, making greater than 90% efficiencies possible at output currents as low as 10mA. This feature maximizes battery life while a product is in sleep or standby modes. In addition, the LTC1148 and LTC1149 are synchronous switching regulators which achieve high efficiency conversion from 10mA to 10A.

A GUIDE TO THE INDEX

Linear Technology has made a major effort to address a wide variety of circuit topics. The number of application problems solvable with innovative circuit techniques or new linear integrated circuits continues to grow. This comprehensive index includes Application Notes (AN1–AN68), Design Notes (DN 1–DN134), *Linear Technology* magazine (LTM I:1–LTM V:4) and Data Sheet circuits through December 1995).

The category and subject index is organized so that application circuits and subject tutorials are easily found. The major topics are broken up into specialized categories to help isolate a particular application. Use the Table of Contents (below) to locate major topic areas, then scan the left-hand "Category" column to find the category of interest. The second column gives the titles or descriptions of the specific circuits and/or discussion topics. The third column lists the publications (AN = Application Note, DN = Design Note, DS = Data Sheet, LTM = *Linear Technology* magazine). The remaining columns indicate the page number, figure number (where applicable) and Linear Technology part numbers.

Two other sources of applications information for LTC products recently became available: The LinearView™ CD-ROM and the Linear Technology web site. The LinearView CD-ROM contains a complete selection of Data Sheets, Application Notes, Design Notes and *Linear Technology* magazines through 1995, combined with a powerful search engine. Periodic updates of the CD-ROM are planned. The Linear Technology web site (www.linear-tech.com) also contains the complete library of Linear Technology publications in Adobe PDF format for download or delivery via FAX. The web site is updated regularly.

NOTE: Application Notes 1–40 and Design Notes 1–32 are found in Volume I of the *Applications Handbook*; Application Notes 41–54 and Design Notes 33–69 are found in Volume II; the remaining Application Notes and Design Notes to date are found in the current volume.

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SUBJECT INDEX

A/D (see Converters—Data)

AC Line Monitor

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
AC Line Monitor	AC Line Monitor	LTC1145/46 DS	11	NA	LTC1145, LT1013

Accelerometer (see Signal Conditioning)

Acoustic Thermometer (see Signal Conditioning—Temperature)

Amplifiers

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Absolute Value	Inverting Amplifier with High Input Resistance	LM108 DS	5	NA	LM108
	Precision Absolute Value Circuit	OP05 DS	8	NA	OP-05CH
		LT1001 DS	9	NA	LT1001
		LT1002 DS	13	NA	LT1002
	Wide Bandwidth Absolute Value Circuit	LT1022 DS	6	NA	LT1022
		LT1122 DS	8	NA	LT1122
Additional Feature Circuits	Ammeter with Six Decade Range	LT1012 DS	9	NA	LT1012, LT1004-1.2
		LT1008 DS	11	NA	LT1008, LT1004-1.2
	Constant Gain Amplifier Over Temperature	LT1004 DS	6	NA	LT1004-1.2
	DC and AC Zeroing	LF198 DS	11	NA	LF198
	DC Stabilized FET Probe	LTC1052 DS	15	NA	LTC1052, LT1010
	Five Decade Kelvin-Varley Divider	LT1008 DS	9	NA	LT1008
	Input Amplifier for 4-1/2 Digit Voltmeter	LT1008 DS	1	NA	LT1008
		LT1012 DS	11	NA	LT1012
	Input Bias Current Cancellation	LT1366–69 DS	18	10	LT1366

Amplifiers (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
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	Typical Application—Input Bias Current Cancellation	LT1211/12 DS	1	NA	LT1211
Artifical Ground	Synthetic Ground	AN50	5	6	LT1006, LT1013, LT1014, LT1077, LT1078, LT1079, LT1178, LT1179, others (see schematic)
Audio	1.8kW Shaker-Table Driver/Audio Amplifier	LTM V:4	4	7a–7c	LT1166, LT1360
	350W Power Amplifier	DN126	2	3	LT1166, LT1360, LT1004-2.5
	Balanced, Transformerless Microphone Preamp	LT1115 DS	8	1	LT1115
	Gain-of-Five, Noninverting Line Driver	LTM I:1	12	1	LT1122, LT1010
	High Preformance Transformer Coupled Microphone Preamp	LT1115 DS	11	5	LT1115, LT1010, LT1097
	Low Noise DC Accurate ×10 Buffered Line Amplifier	LT1115 DS	9	2	LT1115, LT1010, LT1097
	Low Noise, Low Distortion Audio Buffer with Gain of 10	LTM III:2	12	8	LT1206, LT1115
	Moving Coil Passive RIAA Phonograph Preamp	LT1115 DS	10	4	LT1115, LT1056
	RIAA Moving Coil "Pre-Preamplifier"	LT1115 DS	9	3	LT1115, LT1097
	RIAA Phonograph Preamplifier (40dB/60dB Gain)	LT1115 DS	1	NA	LT1115, LT1010
	Very Low Distortion Buffered Preamplifier	AN52	15	21	LT1122, LT1010
Auto-Bias	Basic, LT1166 Circuit Configuration	LTM V:4	3	1	LT1166
Boosted Output	±15V Powered, Bipolar Output, Voltage-Gain Stage, (±100V Swing)	AN18	9	15	LT1013, LT319A
	1.5V Voltage Boosted Output Op Amp (0V–10V)	AN15	6	9	LM10
	Basic Boosted Op Amp (150mA)	AN4	1	1	LT1010, LM101A

Amplifiers (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Boosted Output (Continued)	Detailed High Voltage Op Amp	LTM IV:2	20	2	LT1078
	Fast Power Buffer (10MHz)	AN16	20	51	LT1010, LT118A
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	High Output Current Op Amp	LT1022 DS	7	NA	LT1022, LT1010
		LTC1052DS	14	NA	LTC1052
	Increasing Output Current (10mA–20mA)	AN9	18	28	LTC1052
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	LT1010, Paralleling	AN16	17	43	LT1010
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		LT1055 DS	11	NA	LT1055
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	Output Stage (150mA)	AN18	2	1A–1C	LT1022, LT1010, LT1012, LT118A
	Paralleling for High Current	AN21	12	17	LT1010
	Precision Amplifier Drives 300Ω Load to ±10V	OP227 DS	1	NA	OP227
		LT1007 DS	10	NA	LT1007, LT1037
	Precision Amplifier Drives 500Ω Load to ±10V	LT1002 DS	12	NA	LT1002
	Ultrafast Feed Forward Current Booster (1000V/µs, 14MHz, 200mA)	AN18	3	3	LT1012

Amplifiers (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
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		AN50	2	1A	LT1014
Buffer	Fast ±150mA Power Buffer	LT1010 DS	1–20	NA	LT1010
	Fast, Stabilized FET Buffer (FET Probe)	AN9	9	14	LT1010, LTC1052
	Infinite-Input-Impedance, Unity-Gain, High Voltage Buffer	LTM III:3	19	5	LT1300, LT1097
	Input Buffer for the LT1088	AN22	12	23	NA
	Large Signal Voltage Follower	LT1001 DS	9	NA	LT1001
	Low Noise ×10 Buffered Line Driver	AN67	70	106	LT1115, LT1206
	Noise Meter Buffer/Driver Section	AN67	42	54	LT1206
	Rail-to-Rail Potentiometer Buffer	LTM IV:3	14	3	LT1366
	Reference Buffer	LTC1250 DS	8	NA	LTC1250
	Unity-Gain Buffer with Extended Load Capacitance Drive Capability	LT1169 DS	10	NA	LT1169
	High Voltage Buffer	AN59	9	17	LT1300, LT1097
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	DC Stabilized, Full Differential, Parallel Path	AN47	35	74	LT1102, LT1191, LT1193
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	Fast DC Stabilized FET Amplifier (100V/µs, 1MHz Full Power Bandwidth)	AN21	2	2	LT1012, LT318A
	Fast Summing Amplifier	LM108 DS	6	NA	LM108, LM101A

Amplifiers (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
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		AN47	32	66	LT1220
		LT1122 DS	1	NA	LT1122
	Fast Settling 12-Bit DAC Buffer	LT1220 DS	8	NA	LT1220
	No V_{OS} Adjust CMOS DAC Buffer	LTC1052 DS	13	NA	LTC1052, LTC1043
	Simple Preamplifier for Comparator	AN17	4	5	LT318A, LT1016
Dead Zone	Dead Zone Generator	LT1002 DS	13	NA	LT1002, LM301A
		LT1001 DS	10	NA	LT1001, LM301A
Differential	+90V, –3V Common Mode Range Difference Amplifier (A_V = 1)	LT1413 DS	1	NA	LT1413
	Difference Amplifier with Wide Input Common Mode Range	LT1213/14 DS	16	NA	LT1213, LT1004-1.2
	Differential Bridge Amplifier	LTC1250 DS	1	NA	LTC1250
	Differential-Input, Variable-Gain Amplifier	LTM II:3	15	1	LT1228
Discussion	Achieving Picoampere/Microvolt Performance	LT1012 DS	8	NA	NA
		LTC1052 DS	8	NA	NA
		LT1008 DS	6	NA	NA
	Advantages of Matched Dual Op Amps	LT1024 DS	6	NA	NA
		OP227 DS	10	NA	NA
		LT1002 DS	10	NA	NA
	Amplifier Compensation	AN10	8	B1–B3	NA
	Chopper Stabilized Op Amps	AN9	19	B1–B2	NA
	Chopper vs. Bipolar Op Amps	DN42	1	NA	NA

Amplifiers (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Discussion (Continued)	Demo DC009 High Frequency Amplifier	DN50	1	NA	NA
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		LT1008 DS	8	NA	LT1008
	Gain of 1000 Amplifier with 0.001% DC Accuracy	LT1007 DS	10	NA	LT1037
	High Frequency Amplifier Evaluation Board	AN47	127	I2	NA
	High Speed Effects in Cable, Connectors and Termination	AN47	15	NA	NA
	High Speed Operation	LT1055 DS	8	NA	LT1055, LT1056
	Input Guarding	LM108 DS	7	NA	LM108 series
	Input Protection	LM108 DS	7	NA	LM108 series
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	Isolating Large Capacitive Loads	LT118 DS	5	NA	LT318A
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		AN4	7	NA	LT1010
	LT1010 Performance Summary	AN16	7	NA	LT1010
	Offset Voltage Adjustment	OP27 DS	9	NA	OP27
	Operational Amplifier Selection Guide for Optimum Noise Performance	DN3	1	NA	NA
	Perspectives on High Speed Design	AN47	5	NA	NA
	Perspectives on Speed	AN47	5	NA	NA
	Phase Reversal Protection	LT1055 DS	9	NA	LT1055, LT1056
	Typical High Speed Amplifier Problem	AN47	7	NA	NA
Divider	Analog Divider	LT1057 DS	9	NA	LT1057, LTC1043
	Divide by 3	LTC1043 DS	8	NA	LTC1043
	Divide by 4	LTC1043 DS	9	NA	LTC1043
	Divided by 2	LTC1043 DS	8	NA	LTC1043
	Precision Voltage Divide by 2	LTC203 DS	11	NA	LTC203

Amplifiers (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Fast	"Current Mode Feedback" Amplifier (1MHz Full Power Bandwidth)	AN21	7	11	LT1001, LT1010
		AN22	12	24	LT1001, LT1010
		LT1088 DS	9	NA	LT1001, LT1010
	"Current Mode Feedback" Amplifier (3000V/µs, 25MHz Full Power Bandwidth)	LT1088 DS	10	NA	LT1013
		AN22	13	25	LT1013
		AN21	8	12	LT1013
	Fast DC Stabilized FET Amplifier (100V/µs, 1MHz Full Power Bandwidth	AN21	2	2	LT318A, LT1012
	Fast Precision Inverter	LH2108 DS	1	NA	LH2108A, LT118A
		LT1008 DS	11	NA	LT1008, LT318A
	Fast Summing Amplifier	LM108 DS	6	NA	LM101, LM108
	Precision High Speed Op Amp (1000V/µs)	AN6	7	8	LT1001
		LT1001 DS	7	NA	LT1001
	Stabilized FET Buffer (FET Probe)	AN9	9	4	LT1010, LTC1052
High Voltage	High Voltage Op Amp	AN67	58	79	LT1227
	High Speed Suspended Op Amp	AN67	58	80	LT1227
Hydrophone	Low Noise Hydrophone Amplifier with DC Servo	AN67	69	104	LT1113
Instrumentation	±5V Precision Instrumentation Amplifier	AN3	2	2	LT1013, LTC1043
		LT1006 DS	11	NA	LTC1043, LT1006
		LTC1051 DS	1	NA	LTC1051
	2 Op Amp Instrumentation Amplifier	LT1364/65 DS	11	NA	LT1364
		LT1363 DS	11	NA	LT1363
		LT1361/62 DS	11	NA	LT1361
		LT1360 DS	1	NA	LT1360
	20MHz, A_V = 50 Instrumentation Amplifier	LT1225 DS	1	NA	LT1225
		LT1221 DS	7	NA	LT1221

Amplifiers (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Instrumentation (Continued)	3.5MHz Instrumentation Amplifier Rejects $120V_{P-P}$	AN67	77	125	LT1192
	3.5MHz Instrumentation Amplifier	LTM II:3	5	10	LT1192
	5V Powered Precision Instrumentation Amplifier	LT1013 DS	11	NA	LT1014
	5V Powered Ultraprecision Instrumentation Amplifier	LTC1052 DS	12	NA	LTC1052, LTC1043
	5V Single-Supply Dual Instrumentation Amplifier	LT1013 DS	9	NA	LT1013, LTC1043
	Basic Single Op Amp Instrumentation Amplifier	AN67	83	138	LTC1100/LT1101/LT1102
	Buffered Dual Op Amp Instrumentation Amplifier	AN67	83	139	LTC1100/LT1101/LT1102
		LTM I:2	5	1b	NA
	Chopper Stabilized Instrumentation Amplifier	AN3	3	3	LTC1043, LT1056
		LTC1043 DS	10	NA	LTC1043, LT1056
	Differential Input Instrumentation Amplifier	LM108 DS	6	NA	LM108
	Differential Output	LT1102 DS	8	NA	LT1102
		LT1101 DS	12	NA	LT1101
	Gain = 20, 110 or 200 Instrumentation Amplifier	LT1102 DS	8	NA	LT1102
		LT1101 DS	12	NA	LT1101
	High Performance Instrumentation Amplifier	LTC1051 DS	1	NA	LTC1051
	High Speed, Precision, JFET Input Instrumentation Amplifier	LT1102 DS	1–8	NA	LT1102
	High Voltage Instrumentation Amplifier	LTC1151 DS	7	NA	LTC1151
	Instrumentation Amplifer with Shield Driver	LT1124 DS	1	NA	LT1125
		LT1058 DS	11	NA	LT1058
	Instrumentation Amplifier	LT1355/56 DS	11	NA	LT1355
		LT1354 DS	11	NA	LT1354
		LT1357 DS	11	NA	LT1357

Amplifiers (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Instrumentation (Continued)	Instrumentation Amplifier	LT1358/59 DS	11	NA	LT1358
	Instrumentation Amplifier with ±100V Common Mode Range	LT1012 DS	11	NA	LT1012
	Instrumentation Amplifier with 300V Common Mode Range	AN6	2	1	LT1001, LM301A
		LT1001 DS	11	NA	LT1001, LM301A
	Instrumentation Amplifier with Guard/Shield Driver and Input Bias Current Cancellation	LT1213/14 DS	16	NA	LT1214
	Low Noise, Wide Bandwidth Instrumentation Amplifier	LT1028 DS	15	NA	LT1028
	Precision Instrumentation Amplifier	AN11	6	6A	LT1014
	Precision, Chopper Stabilized, Single-Supply Instrumentation Amplifier	LTC1100 DS	1-8	NA	LTC1100
	Precision, Micropower, Single-Supply Instrumentation Amplifier	LT1101 DS	1–12	NA	LT1101
	Rachel's IA Circuit	LTM II:2	13	2b	LTC1047
	Rex's IA Circuit	LTM II:2	13	2a	LTC1047
	Single Amplifier, Precision High Voltage Instrumentation Amp	DN25	1	1	LT1012A
	Single Op Amp Instrumentation Amplifier	LTM I:2	5	1a	NA
	Single- or Dual-Supply, Chopper Stabilized Instrumentation Amplifier	LTC1050 DS	1	NA	LTC1150, LTC1043
	Single-Supply Instrumentation Amplifier	LT1215/16 DS	1	NA	LT1215
	The Final IA Circuit	LTM II:2	13	3	LTC1047, LTC1043
	Three Op Amp Instrumentation Amp with Gain of 100	LTM II:3	12	2	LT1112, LT1114, LT1097
		AN67	79	130	LT1112/LT1114, LT1097/ LT1114
	Three Op Amp Instrumentation Amplifier	LT1002 DS	10	NA	LT1002, LT1037
		OP05 DS	1	NA	OP05, OP37
		LT1024 DS	6	NA	LT1024, LT1037
		LT1169 DS	10	5	LT1169

Amplifiers (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
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	Three Op Amp, Ultralow Noise Instrumentation Amplifier	AN67	80	131	LT1128, LT1037
	Triple Op Amp Instrumentation Amplifier with Bias Current Cancellation	LT1013 DS	16	NA	LT1014
	Two Op Amp Instrumentation Amplifier with CMRR Trim	LT1024 DS	1	NA	LT1024
		LT1002 DS	12	NA	LT1002
	Ultraprecision Instrumentation Amplifier	AN11	6	6B	LTC1043, LTC1052
		AN9	6	11	LTC1043, LTC1052
Integrator	Integrator with Programmable Reset Level	LF198 DS	10	NA	LF398, LT1008
	Low Drift Integrator with Reset	LM108 DS	5	NA	LM108
Inverter	Ultraprecision Voltage Inverter	LTC1043 DS	8	NA	LTC1043
Isolation	Precision Isolation Amplifier (250V Iso.—0.03% Acc.)	AN9	8	12	LTC1052
		LTC1052 DS	19	NA	LM301A, LTC1052
Lock In	Lock In Amplifier	AN3	4	4	LTC1043, LM301A, LT1007, LT1011, LT1012
		AN43	24	27	LTC1043, LT1007, LT1011, LT1057
		LTC1043 DS	11	NA	LTC1043, LM301A, LT1007, LT1011, LT1012
Logarithmic	Logarithmic Amplifier	LT1008 DS	9	NA	LT1008, LM107, LT1004
	Six-Decade Log Amplifier	LTC1051 DS	13	NA	LTC1051
Low Noise	40dB 40MHz Low Noise Amplifier	LTM V:3	28	1	LT1192, LT1206, LT1226
	Accelerometer Circuit with DC Servo	LTM III:3	9	4	LT1113
	Chopped Bipolar Low Noise Amplifier	AN45	2	2	LT1028, LT1097
	Chopper-Stabilized Low Noise, Low Drift FET Amplifier	LTM I:2	17	1	LTC1150, LT1097

Amplifiers (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
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		LT1028 DS	16	14	LT1028, LTC1052
		LTC1150 DS	11	NA	LTC1150, LT1028
	Low Noise Hydrophone Amplifier with DC Servo	LTM III:3	9	3	LT1113
	Low Noise, Chopper Stabilized FET Pair	AN45	3	4	LTC1050, LT1097
	Paralleling Amplifiers to Reduce Voltage Noise	LT1169 DS	11	NA	LT1169
	Paralleling for Low Noise	LT1028 DS	15	NA	LT1028
		LTC1051 DS	12	NA	LTC1053
		AN21	11	16	LT1028
	Ultralow Noise, Low Drift Amplifier	LTC1052 DS	1	NA	LTC1052, LT1007
	Ultralow Noise, Low Drift, Chopped FET Amplifier	AN61	14	18	LTC1150, LT1097
Low Voltage	3V Operation of Linear Technology Op Amps	DN56	1	Table 1	NA
	High Gain Amplifier with ±1.5V Supplies	LTC1152 DS	8	NA	LTC1152
Low V_{OS} Drift	Obtaining Ultralow V_{OS} Drift and Low Noise	LTC1051 DS	11	NA	LTC1051
	Ultralow Noise, Low Drift Chopper Amplifier	LTC203 DS	8	NA	LTC203, LT1028, LT1097
	V_{OS} Nulling Loop	LT1220 DS	10	NA	LT1220, LT1097
Micropower	Meter Amplifier	LM10 DS	13	NA	LM10
	Microphone Amplifier	LM10 DS	14	NA	LM10
	Micropower, Single-Supply Op Amp	LT1178 DS	1–8	NA	LT1178, LT1179
	Precision, Micropower, Single-Supply Instrumentation Amplifier	LT1101 DS	1–12	NA	LT1101
	Transducer Amplifer	LM10 DS	12	NA	LM10
Multiplexer	High Precision, 3-Input MUX	LTC1152 DS	8	NA	LTC1152
	2-Quadrant, 150kHz Bandwidth Analog Multiplier	AN62	3	1	LTC1099, LT1122, LT1019-5

Amplifiers (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
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	AM Modulator with DC Output Nulling Circuit	AN67	57	76	LT1256, LT1077
		LTM IV:2	29	9	LT1256, LT1077
	Analog Multiplier	LTC1099 DS	11	9	LTC1099
	Analog Multiplier with 0.01% Accuracy	AN3	14	19	LTC1043, LT1056
	Analog Multiplier/Divider	LTC1040 DS	11	NA	LTC1040, LTC1043
	Crystal Oscillator, Op Amp Buffer, and Diode-Ring Mixer	LTM V:3	33	1	LT1206
	Four-Quadrant Multiplier Used as a Double-Sideband, Suppressed-Carrier Modulator	LTM IV:2	29	10	LT1256
	Four-Quadrant, 250kHz Bandwidth Analog Multiplier	AN62	4	3	LTC1278, LT1122
	Multiplier—DC to 50MHz	AN47	45	99	LT1193
	Multiply by 2	LTC1043 DS	8	NA	LTC1043
	Precision Multiply by 3	LTC1043 DS	8	NA	LTC1043
	Precision Multiply by 4	LTC1043 DS	8	NA	LTC1043
	Resistor Multiplier	LT1012 DS	11	NA	LT1012
Noise	Noise Calculation in Op Amp Circuits	DN15	1	NA	NA
	Noise Testing	OP27 DS	8	NA	OP27
Oscillation	Frequency Compensation without Tears	AN47	86	NA	NA
Programmable Gain	Programmable Gain Amplifier (Single-Supply)	LT1078 DS	14	NA	LT1079
	Single-Supply, Noninverting AC Amplifier with Digital Gain Control	LTC1251/56 DS	16	NA	LT1251/LT1256, LT1257
Rail-to-Rail	Input Bias Current Cancellation	LT1366-69 DS	18	10	LT1366
	Positive Supply-Rail Current Sense	LT1366-69 DS	1	NA	LT1366
	Rail-to-Rail Buffer	LTC1152 DS	1	NA	LTC1152

Amplifiers (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Rail-to-Rail (Continued)	Rail-to-Rail Potentiometer Buffer	LT1366–69 DS	18	11	LT1366
Rectifier	100kHz Precision Rectifier	LT1011 DS	15	NA	LT1011
	Half Wave Rectifier	LT1077 DS	10	NA	LT1077
	Precision Rectifier	LM101 DS	5	NA	LM101A
RF	RF Leveling Loop	AN22	14	27	LT1010, LT1012, LT1013, LT1088
		LT1088 DS	11	NA	LT1010, LT1012, LT1013, LT1088
		AN47	64	139A	LT1006, LT1088, LT1223
	Simple RF Leveling Loop	AN47	64	139B	LT1006, LT1228
		AN52	13	19	LT1006, LT1223
RF Bias	GaAsFET Bias Generator	AN66	89	170	LTC1044, LTC1153, LT1004-2.5
Sample and Hold	1.5V Fast Sample and Hold (125µs, 0.1%)	AN15	4	7	LM10, LT1018
	1.5V Powered Sample and Hold	AN15	3	6	LM10, LT1018
	5µs Sample and Hold with Zero Hold Step	LT119A DS	6	NA	LT119A
	8-Bit 100ns Sample and Hold	AN47	57	124	LT1220
	Basic Sample and Hold	LF198 DS	1	NA	LF198
	Differential Hold	LF198 DS	12	NA	LF198
	Fast Acquisition, Low Droop Sample and Hold	LF198 DS	11	NA	LF398
	Fast Sample-Hold, 2µs 0.01%, with Hold Step Compensation	AN4	5	9	LT318A, LT1010, LT1056
	Infinite-Hold-Time Sample and Hold	LTC1099 DS	1	NA	LTC1099, LT1022
		AN62	3	2	LTC1099, LT1122
	Low Power, Low Hold Step Sample and Hold	LTC1049 DS	7	NA	LTC1049, LTC201
	Micropower Sample and Hold	AN23	10	14	LT1006
		LT1006 DS	1	NA	LT1006
	Output Holds at Average of Sample Input	LF198 DS	11	NA	LF198

Amplifiers (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Sample and Hold (Continued)	Quad 12-Bit Sample and Hold	DN38	2	3	LTC201A, LT1014
		LTC201A DS	7	NA	LTC201A/LTC202/LTC203, LT1014/LT1079
	Quad Single 5V Supply, Low Hold Step, Sample and Hold	LTC1043 DS	12	NA	LTC1043, LT1014
	Sample and Difference Circuit	LF198 DS	10	NA	LF198
	Sample and Hold	LF198 DS	6	NA	LM108
	Sample and Hold (10ns)	AN13	18	29	LT318A, LT1016
	Sample and Hold (200ns, 0.01%)	AN13	15	23	LT1016
	×1000 Sample and Hold	LM108 DS	10	NA	LF198, LT1008
Settling Time	Circuit for Testing Followers	AN10	3	4	NA
	Improved Settling-Time Test Circuit	LT1055 DS	8	NA	LT1056
		AN10	2	2	NA
	Measuring Amplifier Settling Time	AN47	82	B1	NA
	Sampling Switch for Ultraprecision Settling Time Measurement	AN10	4	5	NA
	Settling Time Test Circuit	AN10	1	1	NA
Single-Supply	Ground Current-Sense Amplifier	LT1213/14 DS	16	NA	LT1213
	Input Bias Current	LT1211/12 DS	1	NA	LT1211
Switchable Gain	Switchable Gain Video Amplifier	LTM III:3	16	7	LT1204
Track and Hold	Fast Track and Hold	AN13	16	26	LT1016
	Track and Hold (5MHz)	AN16	19	47	LT118A, LT1010
Variable Gain	2-Input Video Fader	LT1251/56 DS	1	NA	LT1251/LT1256
	Basic Variable Integrator	LT1251/56 DS	18	NA	LT1256
	Differential Input, Variable Gain Amplifier	AN67	81	132	LT1228

Amplifiers (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Variable Gain (Continued)	Four-Quadrant Multiplier as a Double Sideband, Suppressed-Carrier Modulator	LT1251/56 DS	15	NA	LT1256
	Logarithmic Gain Control	LT1251/56 DS	17	NA	LT1251/LT1256
	Single-Supply, Inverting AC Amplifier	LT1251/56 DS	16	NA	LT1251/LT1256
	Soft Clipper	LT1251/56 DS	17	NA	LT1256
	Variable-Gain Amplifier	AN3	5	6	LTC1043, LT1056
		LTC1043 DS	14	NA	LTC1043, LT1056
Video	"Picture-in-Picture" Test Setup	LTM III:3	21	1	LT1204
	±3dB Variable-Gain Video Amp Optimized for Differential Gain and Phase	AN57	3	1	LT1227, LT1228
	10MHz Bandwidth-Limited Amplifier	LT1189 DS	10	NA	LT1189
	2-Channel Multiplexed Video Cable Driver	AN47	33	68	LT1190
		DN57	1	NA	LT1190
		LT1190 DS	1	NA	LT1190
	2-Input Video Fader	LTM IV:2	28	4	LT1251/LT1256
	250mA Output Line Driver	LTM V:4	21	3	LT1206
	4 × 4 Video Crosspoint	DN81	2	1	LT1205, LT1254
	Bidirectional Video Bus	DN65	1	1	LT1190, LT1193
		LT1187 DS	11	NA	LT1187, LT1195
		LT1195 DS	11	NA	LT1195, LT1187
	Black Clamp Circuit	AN57	4	2	LT1227
	Cable-Sense Amplifier for Loop-Through Connections with DC Adjust	LT1189 DS	1	NA	LT1189
		LT1187 DS	1	NA	LT1187
	DC Stabilized Fast Amplifier (32MHz)	AN21	5	8	LT1008, LT1010
	Differential Cable Sense Amplifier	LT1193 DS	1	NA	LT1193
		AN47	33	70	LT1193

Amplifiers (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Video (Continued)	Differential Input Video Loop-Through Amplifier	DN57	2	NA	LT1194
	Differential Receiver MUX for Power-Down Applications	LTC1189 DS	11	NA	LT1189
	Differential-Input, Variable-Gain Amplifier	AN57	12	A1	LT1228
	Double Terminated Cable Driver	LT1195 DS	8	NA	LT1195
		LT1192 DS	1	NA	LT1192
		LT1193 DS	10	NA	LT1193
		AN47	33	69	LT1192
	Electronically Controlled Gain, Video Loop-Through Amplifier (LT1228)	DN57	2	NA	LT1228
	Fast RGB Multiplexer	LTM IV:1	9	4	LT1203, LT1205, LT1260
	Four-Input Video Multiplexer with Cable Driver	DN79	1	1	LT1204
	Full Differential Line Receiver	AN47	38	82	LT1194
	Gamma Amp	AN57	6	7	LT1227, LT1229
	Low Cost 50MHz Voltage Controlled Amplifier	DN55	1	1	LT1193
	LT1206 Video Distribution Amplifier	AN67	71	107	LT1206
		LTM III:2	11	4	LT1206
	LT1223 Video Cable Driver	LTM I:1	5	2	LT1223
	LT1228 Soft Limiter	AN57	5	4	LT1228
	LT1251 Video Fader	LTM V:1	36	1	LT1251, LT1360
	LT1256 Video Cable Equalizer	DN92	1	1	LT1256, LT1227
	Luma Keyer	LTM IV:3	27	1	LT1203, LT1363, LT1016
		AN67	55	71	LT1203, LT1363, LT1016
	Many-Input Video MUX Cable Driver	LTM II:2	16	2	LT1227
	Picture-in-Picture Test Setup	AN57	18	C1	LT1204
	Programmable Gain Amplifier Accepts Inputs from $62.5mV_{P-P}$ to $8V_{P-P}$	LT1204 DS	17	NA	LT1204

Amplifiers (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Video (Continued)	Single 5V Video Amplifier	LT1195 DS	9	NA	LT1195
	Single-Supply, AC-Coupled, Inverting Amplifier	LT1252 DS	6	NA	LT1252
	Single-Supply, AC-Coupled, Noninverting Amplifier	LT1252 DS	6	NA	LT1252
	Switchable-Gain Amplifier Accepts Inputs from 62.5mV$_{P-P}$ to 18V$_{P-P}$	AN57	8	11	LT1204
	Switchable-Gain Amplifier with Input Z = 75Ω	AN57	9	12	LT1204
	Twisted-Pair Driver/Reciever	AN57	9	13	LT1204, LT1227, LT1193
	Two Input Video Fader	AN67	56	74	LT1251/LT1256
	Video Cable Driver	LT1220 DS	10	NA	LT1220
	Video DC Restore (Clamp) Circuit (LT1228)	DN57	2	NA	LT1228
	Video Distribution Amplifier	AN4	4	7	LT1010
	Video Fader	AN67	53	68	LT1251, LT1360, LT1004-2.5
		DN57	2	NA	LT1228, LT1223
	Video Gain-Control Stage	AN67	72	111	LT1228
	Video Gain-Control Circuit and Test Setup	AN57	15	B1	LT1228
		LTM III:2	17	1	LT1228
	Video Line Driver	LTM V:4	20	1	LT1363
	Video Line Driving Amplifier	AN4	3	6	LT1010
	Video Loop-Through Connection with DC Control	LTM I:2	12	5	LT1193
	Video MUX Cable Driver (LT1227)	DN57	1	NA	LT1227
Wideband (See also Amplifiers, Fast)	DC Stabilized Fast Amplifier, Low Bias Current (100V/µs, 1MHz Full Power Bandwidth)	AN21	6	9	LT1010, LT1012
	Differential Comparator Amplifier—Settable Limiting and Offset	AN47	40	88	LT1016, LT1194
	Fast Differential Comparator Amplifier	AN47	39	86	LT1006, LT1193, LT1019
	Feed Forward, DC Stabilized Buffer	AN4	2	4	LT1008, LT1010

Amplifiers (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Wideband (Continued)	Gain-Trimmable Wideband FET Amplifier	AN21	4	6	LT1010, LT1012
	LT1010 Wideband Amplifier	AN16	17	44	LT1010
	Stabilized, Wideband Cable-Driving Amplifier	AN45	4	6	LTC1150, LT1010
	Transformer Coupled Amplifier	AN47	39	84	LT1191
	Wideband FET Input Stabilized Buffer	AN21	3	4	LT1010, LTC1052
	Wideband, High Input Impedance, Gain = 1000 Amplifier	LT1058 DS	8	NA	LT1058

Amplifiers—Current Feedback

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
AC Coupled	AC Coupled Inverting	LT1227 DS	11	NA	LT1227
		LT1229 DS	11	NA	LT1229
	AC Coupled Noninverting	LT1229 DS	11	NA	LT1229
		LT1227 DS	11	NA	LT1227
Boosted Output	150mA Output Current Video Amp	LT1223 DS	11	NA	LT1223, LT1010
Discussion	Current Feedback	AN47	124	NA	NA
	Current Feedback Amplifier "Dos and Don'ts"	DN46	1–2	NA	LT1223
Driver	Bridge Driver for HDSL	DN132	2	2	LT1207
	CCD Clock Driver	DN132	2	3	LT1207
	Twisted Pair Driver for ADSL	DN132	1	1	LT1210
General	"Current Mode Feedback" (Son of Godzilla Amplifier)	AN21	8	12	LT1013
		AN22	13	25	LT1013
	"Current Mode Feedback" Amplifier (1MHz Full Power Bandwidth)	AN21	7	11	LT1001, LT1010
		LT1088 DS	9	NA	LT1001, LT1010
		AN22	12	24	LT1001, LT1010

Amplifiers—Current Feedback (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Instrumentation	Difference Amplifier	LT1223 DS	10	NA	LT1223
	Video Instrumentation Amplifier	LT1223 DS	10	NA	LT1223
Integrator	Current Feedback Amplifier Integrator	LT1223 DS	9	NA	LT1223
Rectifier	Half-Wave Rectifier	LT1252 DS	6	NA	LT1252
RF	Simple RF Leveling Loop	LTM I:2	16	1	LT1228, LT1006, LT1004-1.2
Single-Supply	Single-Supply AC Coupled Amplifiers	LT1229 DS	11	NA	LT1229
Video	2-Input Video MUX Cable Driver	LT1259/60 DS	1	NA	LT1259
	3.58MHz Phase Shifter	LTC1251/56 DS	19	NA	LT1256, LT1253
	Cable Driver for Composite Video	LT1229 DS	10	NA	LT1229
	Video Cable Driver	LT1223 DS	1	NA	LT1223
	Video Loop-Through Amplifier	LT1229 DS	1	NA	LT1229

Analog Switches

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Driver	±5V Analog Switch Driver	LTC1045 DS	10	NA	LTC1045
Multichannel	Micropower, Low Charge Injection, Quad Analog Switch	LTC201 DS	1–12	NA	LTC201/LTC202/LTC203
Multiplexed	2-Channel Switch	LF198 DS	11	NA	LF398

Anemometer (see Signal Conditioning)

Audio (see Amplifier, Audio)

Backlight (see Regulator—Switching, Backlight)

Ballistocardiograph

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Ballistocardiograph	Heart-Condition Monitoring	AN43	8	11	LT1010, LT1012, LT1018, LTC1043, LTC1150, LT1021

Battery Chargers

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Discussion	Battery Charging Current System Test Circuit	AN68	28	A1	LT1510, LT1006
	Battery Simulator	AN68	35	B1	LT1078, LT1073-12
	Charging up to 8 Cells from a 25V Supply	AN64	7	4	LTC1325
	Construction of Low Resistance Shunts	AN37	4	NA	NA
	Controlled, Constant-Current Load	AN68	36	B2	NA
	Current Comparator for Initiating Float Time	LT1510 DS	10	6	LT1510, LT1011
	Disconnecting the Voltage Divider to Keep V_{BAT} Regulated to the Battery Voltage	LT1510 DS	10	5	LT1510
	LT1510 with Undervoltage Lockout	LT1510 DS	9	3	LT1510
	LTC1325 Charge, Discharge, and Gas Gauge Circuit	AN64	3	2	LTC1325
		LTM IV:3	18	2	LTC1325
	LTC1325 Fast Charger Circuit	LTM IV:3	17	1	LTC1325
	LTC1325 Fault-Detection Circuitry	AN64	4	3	LTC1325
	PWM Current Programming	LT1510 DS	9	4	LT1510
General	50mA Battery Charger and Regulator	LT1020 DS	14	NA	LT1020
	Battery Charger	LT1086 DS	10	NA	LT1086
	Battery Charger with Reversed-Battery Protection	AN64	14	11	LTC1325
	Battery Charger with T_{BAT} and V_{BAT} Failsafes Disabled	AN64	10	8	LTC1325

Battery Chargers (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
General (Continued)	Charging External Battery Through, LTC694/695-3.3 V_{OUT}	LTC694/5-3.3 DS	9	3	LTC694-3.3/LTC695-3.3
	Charging More than 8 Cells from 25V	AN64	8	5	LTC1325, LT1006
	Connecting Portable System Circuits to the LT1510 SENSE Pin	AN68	15	9	LT1510, LT1302/LT1304/LT1307 or Similar
	Constant Current Battery Charger	AN51	8	11	LT1171
	High Efficiency Battery Charger	DN124	1	1	LT1511
	High Efficiency, Dual-Rate Battery Charger	AN51	9	12	LT1171, LT1006
	High Efficiency Power Supply Providing 3.3V/2A with Built-In Charger	LTC1142 DS	18	14	LTC1142
	LT1510 Block Diagram, Showing Basic Charger Circuit	AN68	6	2	LT1510
	LT1510 Charger System, 2-Diode Configuration	AN68	16	10	LT1510, LT1373/LT1439 or Similar
	LT1510 Charger System, Current-Boost Configuration	AN68	17	11	LT1510, LT1006
	LTC1325 Charger Using a Gated, Constant-Current Supply	AN64	11	9	LTC1325
	LTC1325 Typical Application	LTC1325 DS	1	NA	LTC1325
	LTC1325 Typical Application (another one)	LTC1325 DS	23	NA	LTC1325
	Programmable Battery Charger	AN51	10	13	LT1171, LT1006
	SEPIC Charger with 0.5A Output Current	LT1512 DS	1	NA	LT1512
	Wind-Powered Battery Charger	LTC1042 DS	7	NA	LTC1042, LM334, LT1004-1.2
Lead-Acid	Constant Voltage Charger	AN64	12	10	LTC1325
	Fast, Temperature-Compensated SLA Charger	AN68	23, 32	18, A7	LT1510, LT1011
	Lead Acid Battery Charger	AN51	10	16	LT1171, LT1013
		LTC1041 DS	7	NA	LTC1041
	Perfectly Temperature-Compensated Lead-Acid Battery Charger	AN66	74	148	LT1086, LT1012

Battery Chargers (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Lead Acid (Continued)	Temperature-Compensated Lead Acid Batter Charger	LT1038 DS	9	NA	LT1038 LM301A
		LT138 DS	7	NA	LT338A
		LTM IV:1	18	1	LT1086, LT1012
	Temperature-Compensated Standard Sealed-Lead-Acid Battery Charger	AN68	22	16	LT1510
Li-Ion	87% Efficient Lithium Battery Charger	LT1510 DS	1	2	LT1510
	Adding a Protection Resistor for Lithium-Ion Charger	LT1239 DS	11	5	LT1239
	Current Comparator for Initiating Float Time Out	DN111	2	4	LT1510, LT1011
	High Efficiency Li-Ion battery charger	DN111	1	1	LT1510
	Li-Ion Battery Charger	AN66	70	145	LT1510
		AN66	72	146	LTC1147, LT1014, LT1009
		LTM V:2	35	1	
	Li-Ion I_{MIN} + Timer Charger	AN68	24, 34	19, A9	LT1510, LT1011
	Typical LT1510 Based Li-Ion Charger Circuit	AN68	8	3	LT1510
Microprocessor Controlled	12-Bit, Serial Interface, Microprocessor Charge-Current Control	AN68	26	23	LT1510, LTC7543, LT1097
	12-Bit, Parallel Loading, Microprocessor Charge-Current Control	AN68	26	22	LT1510, LTC7541A, LT1097
	Complete LTC1325 Battery Management System	AN64	1	1	LTC1325
	Microprocessor Control of, LT1510 Constant-Voltage Output	AN68	27	24	LT1510, LTC7541A/LTC7543, LT1097
NiCd	4–6 Cell NiCd Battery Charger	DN125	2	6	LT1377
	4-Cell NiCd Battery Charger	AN66	73	147	LT1377
	4-Cell NiCd Regulator/Charger for Notebook Computers	DN54	1	1	LT1018, LTC1155, LT1431
		AN51	14	21	
	4-Cell, 1.3A Battery Charger Using Surface Mount Components	LTM III:3	23	1	LTC1148

Battery Chargers (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
NiCd (continued)	4-Cell, 300mA NiCd Battery Charger	LTM IV:1	17	1	LTC1174
		LTC1265 DS	16	NA	LTC1265
	4-NiCd Cell Battery Charger	DN98	2	6	LTC1265
	5V or 3.3V Input, 4-Cell NiCd Battery Charger	LTM V:2	34	1	LT1377
	90% Efficient NiMH or NiCd Battery Charger	LT1510 DS	1	1	LT1510
	All Surface Mount 4-Cell NiCd Battery Charger	AN66	75	149	LTC1174
	Constant Current Battery Charger	LTM V:4	18	1	LTC1174HV-3.3
	High Efficiency (>90%) NiCd Battery Charger Programmable for Fast Charge or Trickle Charge	AN66	76	150	LTC1148
	LT1510 NiCd Charger with –ΔV Termination	AN68	21, 31	15, A5	LT1510, LT1013, LT1029CZ, LF398
	LT1510 NiCd Charger with dT/dt Termination	AN68	18, 29	13, A3	LT1510, LT1014
	LTC1325 Typical Application	LTC1325 DS	1	NA	LTC1325
	LTC1325 Typical Application (Wide Range Battery Charger)	LTC1325 DS	23	NA	LTC1325
	Microprocessor Controlled NiCd or MiMH Charger	AN68	25	20	LT1510, LTC1096-5, LT1086-5CT
	NiCd or NiMH Battery Charger	AN66	70	144	LT1510
	Switched Mode Thermal NiCd Charger	AN37	4	6	LT311, LT1006
		AN37	3	5	LT1006
	Thermally Controlled NiCd Battery Charger	LT1001 DS	9	NA	LT1001
		AN6	4	3	LT1001
		AN37	2	2	LT1006
NiMH	90% Efficient NiMH or NiCd Battery Charger	LT1510 DS	1	1	LT1510
	Microprocessor Controlled NiCd or NiMH Charger	AN68	25	20	LT1510, LTC1096 LT1086-5CT
	NiCd or NiMH Battery Charger	AN66	70	144	LT1510
	LTC1352 Typical Application	LTC1325 DS	1	NA	LTC1325

Battery Chargers (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Termination	Hardwired Delta TCO Termination	AN64	9	7	LTC1325
	Hardwired TCO Termination	AN64	9	6	LTC1325

Booster (see Amplifier)

Breadboarding Techniques

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Discussion	Breadboarding Techniques	AN47	26	NA	NA
		AN47	98	NA	NA

Bridge Amplifier (see Signal Conditioning)

Buffer (see Amplifier, Buffer)

Bypassing (see Capacitors)

Capacitors

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Discussion	About Bypass Capacitors	AN13	25	A1	NA
		AN47	25	54	NA
	Hold Capacitor	LF198 DS	6	NA	LF198 Series

CCFL—(see Regulator—Switching, Backlight; Regulator—Switching (Micropower), Backlight

CCFL Test Equipment

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Electrical	Fast, Single-Supply Adaptive Trigger	AN61	15	21	LT1192, LT1006, LT1116
	Floating Output Callibrator	AN65	77	C19	LT1172, LT1220, LT1221, LT1222
	High Voltage RMS Calibrator	AN55	71	C13	LT1172, LT1006
	Precision Wideband Differential Probe Amplifier for Floating-Lamp Voltage Measurement	AN65	72	C14	LT1012, LT1193
Photometric	Glometer Lamp-Drive Electronics	AN65	88	D2	LT1006, LT1012, LT1228, LT1021-10, LT1122
	Glometer Photodiode Amplifier	AN65	90	D5	LT1006
	Precision, "Clip-On" Current Probe for CCFL Measurement	DN101	1	1	LT1223

Circuit Breakers

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Circuit Breaker	12V Lamp Driver/Circuit Breaker with Autoreset	LTC1153 DS	12	NA	LTC1153
	24V to 28V Overtemperature Circuit Breaker	LTC1153 DS	11	NA	LTC1153
	24V to 28V Overtemperature Circuit Breaker with Bootstrapped Supply	LTC1153 DS	11	NA	LTC1153
	5V/1A Circuit Breaker with 1ms Trip Delay, 200ms Autoreset Period and 70°C Thermal Shutdown	LTC1153 DS	1	NA	LTC1153
	5V/1A Circuit Breaker with Shutdown	AN66	86	166	LTC1153
	5V/1A Circuit Breaker with Thermal Shutdown	LTM II:2	8	1	LTC1153
	Autoreset Circuit Breaker with Programmable Number of Retries Using Binary Counter	LTC1153 DS	14	NA	LTC1153
	Overtemperature Circuit Breaker	LTC1153 DS	11	NA	LTC1153
	Overvoltage Circuit Breaker	LTC1153 DS	11	NA	LTC1153

Circuit Breakers (Continued)					
Category	**Subject**	**Publication**	**Page Number**	**Figure Number**	**LT Part Number(s)**
	SCSI Termination Power 1A Circuit Breaker with Autoreset and Ramped Turn-On	LTC1153 DS	12	NA	LTC1153

Clock Circuits (see Oscillators)

Comparators

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Additional Feature Circuits	Driving Ground Referred Load	LT1011 DS	10	NA	LT1011
		LT311A DS	6	NA	LT311A
	Driving Load Referenced to Negative Supply	LT1011 DS	9	NA	LT1011
		LT311A DS	6	NA	LT311A
	Driving Load Referenced to Positive Supply	LT311A DS	6	NA	LT311A
		LT1011 DS	9	NA	LT1011
	Noise Immune 60Hz Line Sync	LT119A DS	5	NA	LT319A
		LT1101 DS	11	NA	LT1011
	Using Clamp Diodes to Improve Frequency Response	LT1011 DS	10	NA	LT1011
		LT311A DS	6	NA	LT311A
Current	Fast Current Comparator (12-Bit)	OP15 DS	1	NA	OP16, LT1011, LT1009-2.5
	Fast Current Comparator (16-Bit)	LT1055 DS	10	NA	LT1056, LT1011, LT1009-2.5
DAC	Fast Preamplifier for Comparator	AN17	5	7	LT1016
Discussion	High Speed Comparator Problems	AN13	4	3–4	NA
Hysteresis	Combining Offset Adjust with Hysteresis	LT1011 DS	11	NA	LT1011
	Comparator with Hysteresis	LT685 DS	1	NA	LT685
	Low Power Comparator with <10μV Hysteresis	LT1012 DS	11	NA	LT1012
		LT1097 DS	7	NA	LT1097
Isolated	Fully Isolated Limit Comparator (500V Iso) with Gain of 100	AN11	10	12	LT1018
		LT1017 DS	8	NA	LT1018, LT1004-1.2
Level Shift	Output Level Shifting	AN13	31	E1–E4	LT1016
Microvolt	Dual-Limit Microvolt Comparator	OP227 DS	11	NA	OP227
One Shot	Voltage Controlled High Speed One Shot	LT319A DS	6	NA	LT319A, LM385-1.2
Precision	Dual Limit Microvolt Comparator	LT1002 DS	11	NA	LT1002
	Microvolt Comparator with Hysteresis	LT1007 DS	10	NA	LT1007
	Microvolt Comparator with TTL Output	LT1001 DS	8	NA	LT1001

Comparators (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Precision (Continued)	Offset-Stabilized Comparator	LTC1052 DS	12	NA	LT1011, LTC1052, LTC1043
		AN9	11	16	
Trigger	Trigger (50MHz)	AN13	24	42	LT1016
		AN47	59	130	LT1016, LT1097, LT1222
Ultrafast	High Speed Comparator with Hysteresis	LT685 DS	1	NA	LT685
	Single-Supply, Ground-Sensing Comparator	LT1116 DS	1–8	NA	LT1116
	Ultrafast Summing Comparator	AN47	58	128	LT1016, LT1191
Window	1.5V Powered Refrigerator Alarm	LT1017 DS	1	NA	LT1017
	Multiwindow Comparator and Display	LTC1045 DS	13	NA	LTC1045
	Undervoltage/Overvoltage Detector	DN123	2	2	LTC1442
	Window Comparator	LTC1042 DS	1–8	NA	LTC1042
	Window Comparator with Symmetric Window Limits	LTC1040 DS	1	NA	LTC1040
	Window Detector	LT1011 DS	10	NA	LT1011
		LT311A DS	6	NA	LT311A
Zero Crossing	Fast Zero Crossing Detector	LT1116 DS	6	NA	LT1116

Controllers

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Cooler	Peltier Cooled, Switch-Mode 0°C Reference	AN25	12	18	LT1070, LTC1043, LT1013
Oven	In Crystal Oven Controller	AN1	6	12	LT1005
	Ovenized Oscillator	AN12	3	5	LT1005, LT1001

Converters

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
AC/DC	Fast, Bridge-Switched, Synchronous Rectifier Based AC-DC Converter	AN43	34	50	LT1012, LT1016
	Synchronous Rectifier Based AC/DC Converter ($0V_{RMS}$–$1.5V_{RMS}$ to 0V–1.5V)	AN13	21	36	LT1012, LT1016
AC/F	Bipolar (AC) Input V/F Converter	LTC203 DS	9	NA	LTC203, LT1056, LT1011, LT1102
		LT1058 DS	10	NA	LT1058
	Bipolar Input-to-Frequency Converter	AN45	17	24	LTC201, LT1056, LT1011, LT1102
Capacitance/ Frequency	Humidity-to-Frequency Converter	AN7	11	11	LT1011, LT1056, LTC1043
Capacitance/ Pulse Width	Capacitance-to-Pulse Width Converter	LT1011 DS	13	NA	LT1011
DC/AC	LT1074-Based 400Hz Sine Wave Output (28V to 110VAC)	AN35	15	31	LT1074, LT1013, LT1086-12
DC/AC	Sine Wave Output Converter (115VAC)	AN8	11	24	NA
DC/DC: See Regulators—Switching					
Discussion	Analog Considerations for Interfacing the LTC1090 10-Bit DA System	LTC1090 DS	17–21	6–16	LTC1090
	Analog Considerations for Interfacing the LTC1091	LTC1091 DS	20–25	4–14	LTC1091
	Successive Approximation Techniques	AN17	8	NA	NA
	Thermal RMS/DC Converters	LT1088 DS	1–12	NA	LT1088
		AN22	1	1	NA
	V/F Techniques	AN14	18	B1–B5	NA
F/V	Frequency to Voltage	AN3	11	12	LTC1043
I/V	DAC I-to-V Converter	LT1357 DS	1	NA	LT1357
		LT1358/59 DS	1	NA	LT1358
	Inverting Op Amp Current-to-Voltage Converter	LTM V:2	16	2	LT1311
	LT1220 High Speed I/V Converter	LTM I:1	4	1	LT1220

Converters (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
I/V (Continued)	Photodiode Current-to-Voltage Converter	LTM V:2	16	1	LT1113
Pulse Width/ Voltage	Fast Time-to-Height Converter	AN47	60	132	LT1220
	Pulse Width-to-Voltage Converter	LF198 DS	13	NA	LF398, LT1004
RMS/DC	100MHz Thermally Based RMS/DC Converter	AN61	17	22	LT1088, LT1013, LT1018, LT1097, LT1206
	50MHz Thermal RMS to DC Converter	AN5	4	6	LT1001, LT1002
		LT1013 DS	9	NA	LT1014
		LTC1043 DS	11	NA	LTC1043, LT1013
	Fast Settling RMS/DC Converter	AN22	9	17	LT1088, LT1010, LT1013
		LT1088 DS	7	NA	LT1088, LT1010, LT1013
	Servo-Sensed Heater Protection Circuit	AN22	10	20	LT1018
	Thermal RMS/DC Converter (100MHz)	AN22	5	8	LT1088, LT1013, LT1004-1.2
		LT1088 DS	6	4	
Temperature to Frequency	Isolated Temperature-to-Frequency Converter	LTM III:1	4	4	LTC1146, LTC1049, LT1025
	Isolated, Battery-Powered Temperature-to-Frequency Converter	LTC1145/46 DS	9	NA	LTC1164, LTC201, LT1025, LTC1049, LT1004-1.2
	Quartz-Crystal Based Thermometer	AN61	13	17	LT485
V/F	1.5V Voltage-to-Frequency Converter (0V–1V to 25Hz–10kHz)	AN15	1	1	LT1017
	1.5V Voltage-to-Frequency Converter (1Hz–1kHz, 0V–1V)	AN14	9	12	LT1017
	$1/V_{IN}$ to Frequency Converter (0V–10V to 1kHz–2Hz)	AN14	12	17	LT1011, LT1056
	3.3V-Powered Voltage-to-Frequency Converter	AN61	23	31	LTC1043, LT1017
	90µA Supply Current V–F, 0.05% Linearity (0V–5V to 0kHz–10kHz)	AN45	15	21	LT1017
	Charge Pump $1/V_{IN}$ to Frequency (0V–5V to 10kHz–50Hz)	AN14	13	19	LTC1043, LT319A, LT1010, LT1056

Converters (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
V/F (Continued)	Exponential to Frequency (0V–10V to 20Hz–20kHz)	AN14	15	21	LTC1043, LT318A, LT1056, LT1021-10
	Exponential Voltage-to-Frequency Converter	LT1055 DS	9	NA	LT1055, LM301A
	Fast Response Voltage-to-Frequency (1Hz–2.5MHz, 0V–5V)	AN14	4	5	LT319A, LTC1052, LT1056
	Low Power V/F Converter (0V–1V to 0kHz–1kHz)	LT1018 DS	7	NA	LT1018, LT1034-1.2
	Micropower V/F Converter (0V–5V to 0kHz–10kHz)	AN23	11	16	LT1017
	Micropower V/F Converter (0V–5V to 100Hz–1MHz)	DN38	1	1	LTC201A, LT1178, LT1004-2.5
		LTC201 DS	1	NA	
	Micropower V/F Converter, 0.02% Linearity (0V–5V to 0MHz–1MHz)	AN23	13	20	LTC201, LT1178
		LT1006 DS	10	NA	LT1006, LT1004-1.2, LT1004-2.5
	Offset Stabilizing V/F Converter	AN9	12	18	LTC1052
	Quartz Stabilized Voltage-to-Frequency (0V–10V to 0kHz–10kHz)	AN14	6	8	LTC1043, LT1056, LT1001, LT1011
	Quartz Stabilized, Voltage-to-Frequency (1Hz–30MHz, 0V–10V)	AN13	11	19	LT1002, LT1016
	Single 5V Voltage-to-Frequency Converter	LTC1040 DS	11	NA	LTC1040
	Single-Supply (0V–5V to 0kHz–5kHz)	AN50	7	8	LTC1043, LT1018
	Ultralinear Voltage-to-Frequency Converter (100kHz–1.1MHz)	AN14	7	10	LTC1043, LT1013
	Voltage-to-Frequency (0Hz–30kHz, 0V–3V)	AN3	11	12B	LTC1043, LT1009, LF356
		LTC1043 DS	9	NA	
	Voltage-to-Frequency (1Hz–1.25MHz, 0V–5V)	AN9	13	19	LTC1043, LTC1052
	Voltage-to-Frequency (1Hz–100MHz, 0V–10V: King Kong V/F)	AN14	2	1	LTC1043, LT1013, LTC1052

Converters (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
V/F (Continued)	Voltage-to-Frequency (1Hz–10MHz, 0V–10V)	AN13	9	16	LT318A, LT1011, LT1012, LT1016
		LT1016 DS	14	16	LT318A, LT1011, LT1012, LT1016, LM134, LT1034-1.2, LT1034-2.5
	Voltage-to-Frequency Converter (0Hz–10kHz)	LT1055 DS	1	NA	LT1056
	Voltage-to-Frequency Converter (10Hz–100kHz)	LT1011 DS	14	NA	LT1011, LT1009
	Voltage-to-Frequency Converter (10Hz–1MHz)	LT1022 DS	5	NA	LT1022, LT1011, LT1009
	Voltage-to-Frequency Converter (1Hz–1.25MHz)	LTC1052 DS	13	NA	LTC1052, LTC1043, LT1004-1.2
	Voltage-to-Frequency Converter (1Hz–10MHz)	AN47	54	121	LT1122, LT1016, LT1010, LT1006, LT137
	Voltage-to-Frequency Converter (1Hz–30MHz)	LTC1052 DS	14	NA	LTC1052, LTC1043, LT1004-1.2
	Voltage-to-Frequency Converter (5kHz–2MHz)	LT119A DS	7	NA	LT119A, LT1004-1.2
Voltage/Pulse Width	Voltage-Controlled Pulse-Width Generator	LT1016 DS	15	NA	LT1016, LM385

Converters—Data

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
A/D	4-Digit (10,000 Count) A/D Converter	LT1011 DS	13	NA	LT1011, LF398, LM329
	Extending Resolution	AN50	7	7	LT1014/LT1079/LT1179, LT1004-1.2
A/D 8-Bits	0A-to-2A Battery-Current Monitor Draws Only 70µA	AN62	8	10	LTC1096, LT1178, LT1004-1.2

Converters—Data (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
A/D 8-Bits (Continued)	1kHz Sampling ADC Operates from 3V Lithium Coin Cell	LTM II:1	7	4a	LTC1098
	Two LTC1390 Cascadable, Serially Programmed, 8-Channel Multiplexers Provide 16 Analog Inputs	AN62	15	21	LTC1390, LTC1096
	3V Battery Powered, 10µW, 8-Bit A/D, Samples at 200Hz	LTC1096 DS	1	NA	LTC1096
	Battery-Powered Digital Thermometer Transmits Over RF Link	AN62	13	19	LTC1096, LT1004-1.2, LM134
	Cascading for 9-Bit Resolution	LTC1099 DS	13	NA	LTC1099
	Charge-Pump Powered, Floating A/D Conversion System	AN62	11	16	LTC1096, LT1004-1.2
		LTM II:1	10	8	
	Data-Acquisition Board	AN34	1–12	1–4	LTC1099
	Digitally Controlled Op Amp Offset Voltage Adjustment Circuit	LTM V:3	16	2	LTC1329-50, LT1006
	Digitally Controlled Power Supply Adjustment Circuit	LTM V:3	16	1	LTC1329-50, LT1107
	Floating 8-Bit Data-Acquisition System	LTC1096 DS	23	16	LTC1096
		AN52	4	4	
	Half-Flash 8-Bit A/D Digitizes Photodiodes	AN33	2	2	LTC1099, LT1022, LT1056, LT1019-2.5
	Interfacing a 3V-Powered LTC1196 to a 5V-Powered System	LTC1196/98 DS	18	6	LTC1196
	Interfacing the LTC1196 to the Altera EPM5064 PLD	LTC1196/98 DS	23	13	LTC1196
	Interfacing the LTC1198 to the TMS320C25 DSP	LTC1196 DS	24	15	LTC1198
	LTC1090 to Hitachi HD63705 Microcontroller Hardware Serial Interface	AN62	17	31	LTC1090 (LTC1290)
	LTC1090 to Intel 8051 Microcontroller Hardware Serial Interface	AN62	17	29	LTC1090 (LTC1290)

Converters—Data (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
A/D 8-Bits (Continued)	LTC1090 to Motorola MC68HC05C4 Microcontroller Hardware Serial Interface	AN62	17	30	LTC1090 (LTC1290)
	LTC1196 to Altera EPM5064 PLD Interface	AN62	19	39	LTC1196
	LTC1296 to Microcontroller Hardware Serial Interface	AN62	17	28	LTC1296
	Micropower	DN60	1	2	LTC1098
	Micropower Battery-Voltage Monitor	AN62	8	9	LTC1096
	Single 5V Supply, 1Msps, 8-Bit Sampling ADC	LTC1196/98 DS	1	NA	LTC1196
A/D 10-Bits	0–500°C Furnace Exhaust-Gas Temperature Measurement System with Low Supply Detection	AN62	11	15	LTC1091A, LTC1052, LT1019A-5, LT1025A
	1.5V Powered A/D (10-Bit, 100µs)	AN15	2	3	LT1018, LT1034-1.2
	10-Bit Serial Output A/D Converter	LT119A DS	6	NA	LT119A, LT1004-1.2
	2-Channel, 10-Bit Serial A/D	LTC1091 DS	1	NA	LTC1091
	A Quick Look Circuit for the LTC1090 10-Bit A/D System	LTC1090 DS	22	NA	LTC1090
	Auto Ranging an 8-Channel, 10-Bit A/D Converter	LTC221/222 DS	7	NA	LTC221/LTC222, LTC1090, LT1006, LT1027
	Auto-Zeroing A/D Offset Voltage	DN26	1–2	1–2	LTC1090
	Complete Temperature, Supply Voltage and Supply Current Monitor	LTC1392 DS	1	NA	LTC1392
	Current-Output Silicon Sensor Thermometer Driving 10-Bit A/D Converter	AN62	9	12	LTC1092, LT1019-2.5, LM134
	Data-Acquisition System Uses 4 Wires	DN1	1	1	LTC1090
	Fully Isolated A/D (10-Bit at 175V Iso)	AN11	12	14	LT1018
	Hitachi Synchronous SCI (HD63705) Interface	LTC1090 DS	15	NA	LTC1090
	Intel 8051 Interface	LTC1090 DS	16	NA	LTC1090
		LTC1091 DS	19	NA	LTC1091
	Interfacing LTC1090 to 8051	AN26A	1	1	LTC1090
	Interfacing LTC1090 to COP400	AN26F	1	1	LTC1090

Converters—Data (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
A/D 10-Bits (Continued	Interfacing LTC1090 to COP800	AN26D	1	1	LTC1090
	Interfacing LTC1090 to HD63705V0	AN26C	1	1	LTC1090
	Interfacing LTC1090 to MC68HC05	AN26B	1	1	LTC1090
	Interfacing LTC1090 to TMS7000	AN26E	1	1	LTC1090
	Interfacing LTC1091 to 68HC05	AN26H	1	1	LTC1091
	Interfacing LTC1091 to 8051	AN26G	1	1	LTC1091
	Interfacing LTC1091 to COP800	AN26I	1	1	LTC1091
	Interfacing LTC1091 to HD6305V0	AN26L	1	1	LTC1091
	Interfacing LTC1091 to HD63705V0	AN26L	1	1	LTC1091
	Interfacing LTC1091/92 to TMS320C25	AN26N	1	1	LTC1091
	Isolated 10-Bit Data-Acquisition System	LTC1145/46 DS	10	NA	LTC1145, LTC1090, LT1111, LT1121-5
	LTC1091 to Intel 8051 Microcontroller Hardware Serial Interface	AN62	18	32	LTC1091 (LTC1291)
	LTC1091 to Motorola MC68HC05C4 Microcontroller Hardware Serial Interface	AN62	18	33	LTC1091 (LTC1291)
	LTC1092 10-Bit A/D Converter Receives Power and Transmits Data Over Two Transformer-Isolated Lines	AN62	14	20	LTC1092, LT1021-5
	LTC1094 A/D Converter RS232 Interface with LT1180 Dual Driver/Receiver	AN62	20	41	LTC1094, LT1180A, LT1021-5
	LTC1095 to Intel 8051 Microcontroller Hardware Serial Interface	AN62	18	34	LTC1095
	LTC1095 to Motorola MC68HC05C4 Microcontroller Hardware Serial Interface	AN62	18	35	LTC1095
	LTC1390 Typical Application	LTC1390 DS	1	NA	LTC1390, LTC1096
	LTC1392 Temperature/Voltage Measurement Application	DN106	2	3	LTC1392
	Micropower A/D (10-Bit, 100µs)	AN23	9	11	LT1017
	Micropower, Serial 10-Bit Data-Acquisition with 500V Optoisolated Communication	AN62	12	17	LTC1094, LT1021-5
	Motorola SPI (MC68HC05C4) Interface	LTC1090 DS	15	NA	LTC1090

Converters—Data (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
A/D 10-Bits (Continued)	Motorola SPI (MC68HC05C4, MC68HC11) Interface	LTC1091–94 DS	18	NA	LTC1091
	Multiple LTC1094s Sharing One 3-Wire Serial Interface	AN62	19	38	LTC1094
	Multiple LTC1095s Sharing One 3-Wire Serial Interface	AN62	18	36	LTC1095
	National Microwire™ (COP420) Interface	LTC1090 DS	14	NA	LTC1090
	Simple, Fast A/D (10-Bit)	AN13	20	33	LT1016
	Sneak-A-Bit Circuit for the LTC1090: 11-Bit Resolution from a 10-Bit ADC	AN62	20	40	LTC1090, LT1021-5
	Sneak-A-Bit Code for 10-Bits Plus Sign	LTC1090 DS	22	NA	LTC1090, LT1021-5
	System Monitor for Relative Humidity, Supply Voltage and Ambient Temperature	LTC1392 DS	9	NA	LTC1392, LTC1043, LT1056 LM301A
	System Monitor for Two Supply Voltages and Ambient Temperature	LTC1392 DS	9	NA	LTC1392, LTC1430
	Thermistor-Based Temperature Measurement System	AN62	10	13	LTC1090, LT1006
	Weight Scale	AN62	6	7	LTC1092, LT1013
A/D 12-Bits	0°C–400°C Temperature-Measurement System	LTM II:1	20	1	LTC1292, LT1006, LT1027
	1.8µs, 12-Bit A/D SAR Converter	LT1016 DS	12	15	LT1016
	12-Bit A/D Converter	AN3	12	15	LT319A, LT1056, LTC1043A
		LT1057–58 DS	10	NA	LT1058, LTC1043
	12-Bit A/D Converter Interfaced to MC68HC11	AN67	47	61	LTC1291
	12-Bit Charge Balance A/D Converter	LT1055–56 DS	10	NA	LT1055, LT1001
	12-Bit DAC and LT1220 Op Amp Create Variable Reference Voltages, Enhancing LTC1410 ADC's Input Range	LTM V:4	22	7	LT1220, LTC8043, LTC1410
	12-Bit LTC1296 Data-Acquisition System Strain Gauge with Bridge-Driver Power Shutdown	AN62	16	23	LTC1296, LT1014

Converters—Data (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
A/D 12-Bits (Continued)	12-Bit, 500ksps ADC	LTM IV:1	4	3	LTC1278
	12-Bit, Single 5V Control System with Shutdown	LTC1257 DS	9	NA	LTC1257, LTC1297, LT1025A, LTC1050
	12-Bit, Single 5V Supply ADC Converts AC or DC inputs	LTM I:2	8	2	LTC1272
	12-Bit, Single 5V Temperature Control System with Shutdown	AN67	8	7	LTC1257, LTC1297, LTC1050, LT1025A
		LTM III:3	15	6	LTC1257, LTC1297, LT1025A
	12µW, SO8 Package, 12-Bit ADC Samples at 200Hz and Runs Off a 3V battery	LTC1285/88 DS	1	NA	LTC1285
	2 LTC1390 Multiplexers Expand the Input Capacity of the LTC1286 12-Bit DAC to 16 Channels	DN112	2	3	LTC1390, LTC1286
	2-Channel, Low Power A/D Converter	LT1366–69 DS	15	5	LT1368, LTC1288
	25µW, SO-8 package, 12-Bit ADC Samples at 200Hz and Runs Off a 5V Supply	LTC1286/98 DS	1	NA	LTC1286
	3V Powered, 12-Bit A/D	LTC1289 DS	1	NA	LTC1289, LT1079, LTC1044
	3V Powered, 12µW, 200Hz, 12-Bit ADC	LTC1285/88 DS	1	NA	LTC1285
	8085A and Z80 Interface	LTC1273/5/6 DS	19	19	LTC1273/LTC1275/LTC1276
	8085A and Z80 Interface	LTC1282 DS	20	22	LTC1282
	A "Quick Look" Circuit for the LTC1290	LTC1290 DS	24	NA	LTC1290
	A/D Converter (12-Bits, 7.5µs)	AN17	3	3	LT1021, LT1011A, LT1016
	Autoranging 8-Channel ADC	DN131	2	3	LTC1296, LTC1446
	Autoranging 8-Channel ADC with Shutdown	LTC1257 DS	9	NA	LTC1257, LTC1296
		LTM III:3	4	4	LTC1257, LTC1296
	Bipolar Offset and Full-Scale Adjust Circuit	LTC1279 DS	12	9c	LTC1279
		LTC1282 DS	14	12	LTC1282
	Buffered 2-Channel, Low-Power A/D	DN89	2	3	LTC1288, LT1366

Converters—Data (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
A/D 12-Bits (Continued)	Complete 1.25MHz, 12-Bit Sampling A/D Converter	LTC1410 DS	1	NA	LTC1410
	Complete 100ps-resolution Delta-Time Circuit with "Bow" Correction	AN62	5	5	LTC1282, LM134
	Daisy Chaining Five LTC1390s	LTC1390 DS	7	NA	LTC1390, LTC1286
	Daisy Chaining Five LTC1391s	LTC1391 DS	7	NA	LTC1391, LTC1286
	Daisy Chaining Two LTC1390s for Expansion	LTC1390 DS	6	5	LTC1390, LTC1286
	Daisy Chaining Two LTC1391s for Expansion	LTC1391 DS	6	5	LTC1391, LTC1286
	Delta Time Measurement with the LTC1273	LTC1273/5/6 DS	22	26	LTC1273
	Delta Time Measurement with the LTC1282	LTC1282 DS	21	25	LTC1282
	Differential Temperature-Measurement System	LTM II:1	21	3	LTC1292, LT1027, LM134
	Digitally Linearized Platinum RTD Signal Conditioner	AN62	10	14	LTC1294, LT1101, LT1006, LT1027
	Driving V_{REF} with an LT1006 Op Amp	LTC1282 DS	13	6	LTC1282, LT1006
		LTC1273/5/6 DS	12	6	LTC1275, LT1006
		LTC1279 DS	11	6	LTC1279, LT1006
		LTC1278 DS	11	6	LTC1278, LT1006
		LTC1274/77 DS	13	6	LTC1274, LT1006
	Eight-Channel Data-Acquisition System Without a Buffer Amplifier	DN88	2	4	LTC1278
	Floating, 12-Bit Data-Acquisition System	AN52	3	2	LTC1292, LT1019-5
		LTM II:1	21	2	LTC1292, LT1019-5
	Full-Scale Adjust Circuit	LTC1274/77 DS	16	11a	LTC1274, LTC1277
		LTC1273/5/6 DS	13	10a	LTC1273/5/6
		LTC1279 DS	12	9a	LTC1279
		LTC1278 DS	12	9a	LTC1278

Converters—Data (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
A/D 12-Bits (Continued)	Full-Scale Adjust Circuit	LTC1282 DS	14	10	LTC1282
	Fully Differential 8-Channel, 12-Bit A/D System Using the LTC1390 and LTC1410	AN67	3	1	LTC1390, LTC1410
	High Speed Sampling	DN66	2	2	LTC1273, LTC1275, LTC1276, LTC1282
	Interfacing the LTC1290 to the 8051	AN36A	1	1	LTC1290
	Interfacing the LTC1290 to the COP400	AN36F	1	1	LTC1290
	Interfacing the LTC1290 to the COP800	AN36D	1	1	LTC1290
	Interfacing the LTC1290 to the MC68HC05	AN36B	1	1	LTC1290
	Interfacing the LTC1290 to the MC68HC11	AN36B	1	1	LTC1290
	Interfacing the LTC1290 to the Z-80 MPU	AN36O	1	1	LTC1290
	Interfacing the LTC1290 to TMS7742 MCU	AN36E	1	1	LTC1290
	Interfacing the LTC1390 with the LTC1257 for Demultiplex Operation	LTC1390 DS	8	NA	LTC1390, LTC1257
	Interfacing the LTC1391 with the LTC1257 for Demultiplex Operation	LTC1391 DS	8	NA	LTC1391, LTC1257
	Isolated 4–20mA Current Loop	LTM V:3	31	4	LTC1453, LT1121-3.3, LT1077
	LT574A Bipolar Input Connection	LT574A DS	6	4	LT574A
	LT574A Unipolar Input Connection	LT574A DS	6	3	LT574A
	LTC1272/LTC1273/LTC1275/LTC1276 to 8085A/Z80 Microprocessor Hardware Parallel Interface	AN62	21	43	LTC1272/LTC1273/LTC1275/ LTC1276
	LTC1272/LTC1273/LTC1275/LTC1276 to MC68000 Microprocessor Hardware Parallel Interface	AN62	21	44	LTC1272/LTC1273/LTC1275/ LTC1276
	LTC1272/LTC1273/LTC1275/LTC1276 to TMS32010 DSP Processor Parallel Interface	AN62	22	46	LTC1272LTC1273/LTC1275/ LTC1276
	LTC1273 Offset and Full-Scale Adjust Circuit	LTC1273/5/6 DS	14	10b	LTC1273
	LTC1274 Typical Circuit	LTC1274/77 DS	14	9	LTC1274

Converters—Data (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
A/D 12-Bits (Continued)	LTC1275/76 Offset and Full-Scale Adjust Circuit	LTC1273/75/76 DS	14	10c	LTC1275/LTC1276
	LTC1278 Bipolar Offset and Full-Scale Adjust Circuit	LTC1278 DS	12	9c	LTC1278
	LTC1278 to TMS320C25 DSP Processor Parallel Interface	AN62	22	47	LTC1278
	LTC1278 Unipolar Offset and Full-Scale Adjust Circuit	LTC1278 DS	12	9b	LTC1278
	LTC1282 to TMS320C25 DSP Processor Parallel Interface	AN62	22	45	LTC1282
	LTC1290 to IBM PC Serial Port Interface	AN62	21	42	LTC1290, LT1021-5
		DN35	1	1	LTC1290, LT1021-5
	LTC1297 Data-Acquisition System Micropower Battery-Current Monitor	AN62	9	11	LTC1297, LT1121, LTC1047
	LTC1298 Digitizes Resistive Touchscreen X- and Y-Axis Voltages	DN116	2	3	LTC1298
	LTC1390 Expands the Input Capacity of the 12-Bit LTC1286 DAC to 8-Channels	DN112	1	1	LTC1390, LTC1286
	3V, 8-Channel, 12-Bit A/D Converter	LTC1391 DS	1	NA	LTC1391, LTC1285
	MC68000 Interface	LTC1273/5/6 DS	19	18	LTC1273/5/6
		LTC1282 DS	20	21	LTC1282
	Micropower A/D (12-Bit, 300µs)	AN23	7	9	LT1018, LTC1044
	Micropower Battery Current Monitor Using the LTC1297 12-Bit Data-Acquisition System	AN67	9	8	LTC1297, LTC1047, LT1121
	Micropower Battery-Current Monitor Using the LTC1297	LTM III:1	16	1	LTC1297, LT1121, LT1047
	Micropower Battery-Voltage Monitor	LTC1286/98 DS	23	15	LTC1286
	Multiple LTC1290s Sharing One 3-Wire Serial Interface	AN62	19	37	LTC1290
	Multiplexed, 8-Channel, Data-Acquisition System	LTM IV:1	5	4	LTC1257

Converters—Data (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
A/D 12-Bits (Continued)	MUXing the LTC1275 with the CD4051	LTC1273/5/6 DS	20	21	LTC1275
	MUXing the LTC1282 with the CD4051	LTC1282 DS	21	24	LTC1282
	No-Glue Serial Interface Simplifies Connection to Microcontrollers	DN116	2	2	LTC1286
	Offset and Full-Scale Adjust Circuit	LTC1410 DS	11	10	LTC1410
	Optoisolated Temperature Monitor	AN62	13	18	LTC1292, LTC1050, LT1019-2.5, LT1025A
		LTC1292/97 DS	23	31	LTC1292, LT1019-2.5, LT1025A, LTC1050
	Plugging the LTC1272 into an AD7572 Socket	LTC1272 DS	18–19	22–23	LTC1272
	Power Supply Grounding Practice	LTC1279 DS	13	10	LTC1279
	"Quick Look" Circuit for the LTC1286	LTC1286/98 DS	23	13	LTC1286
	"Quick Look" Circuit for the LTC1297	LTC1292/97 DS	22	28	LTC1297
	SAR Converter (12-Bit, 5µs)	AN13	19	31	LT318A, LT1016
	Several LTC1290s Sharing One 3-Wire Serial Interface	LTC1290 DS	17	5	LTC1290
	Single 3V Supply, 140ksps, 12-Bit Sampling A/D Converter	LTC1282 DS	1	NA	LTC1282
	Single 5V Supply, 10mW, 100kHz, 12-Bit ADC	LTC1274/77 DS	1	NA	LTC1277
	Single 5V Supply, 300ksps, 12-Bit Sampling A/D Converter	LTC1273/5/6 DS	1	NA	LTC1273
	Single 5V Supply, 3µs, 12-Bit Sampling ADC	LTC1272 DS	17	21	LTC1272
	Single 5V Supply, 500kHz, 12-Bit Sampling A/D Converter	LTC1278 DS	1	NA	LTC1278-5
	Single 5V Supply, 600kHz, 12-Bit Sampling A/D Converter	LTC1279 DS	1	NA	LTC1279
	12-Bit, 8-Channel, Sampling Data-Acquisition System	LTC1290 DS	1	NA	LTC1290

Converters—Data (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
A/D 12-Bits (Continued)	Small, 12-Bit, Differential-Input LTC1292 Data-Acquisition System Occupies Only 0.35in^2	AN62	15	22	LTC1292, LT1027
	Smallest Possible 12-Bit ADC Configuration	LTM IV:1	14	4	LTC1286
	Sneak-A-Bit Circuit	LTC1290 DS	25	NA	LTC1290, LT1021-5
	Successive Approximation A/D Converter (12-Bits, 1.8µs)	AN17	6	9	LT1021, LT1016
	Successive Approximation A/D Converter (12-Bits, 10µs)	LT1011 DS	1	NA	LT1021, LT1011A
		AN17	1	1	LT1011A, LM329
	Supplying a 2.5V Reference to the LTC1274	LTC1274/77 DS	13	7	LTC1274, LT1019A-2.5
	Supplying a 2.5V Reference to the LTC1278 with the LT1019A-2.5	LTC1278 DS	11	7	LTC1278, LT1019A-2.5
	Supplying a 2.5V Reference Voltage to the LTC1275 with the LT1019A-2.5	LTC1273/75/ 76 DS	13	7	LTC1275, LT1019-2.5
	Supplying a 2.5V Reference Voltage to the LTC1279 with the LT1019A-2.5	LT1279 DS	11	7	LTC1279, LT1019A-2.5
	Supplying a 2.5V Reference Voltage to the LTC1282 with the LT1019A-2.5	LTC1282 DS	13	7	LTC1282, LT1019A-2.5
	The LTC1278 Undersamples the 455kHz Carrier to Recover the 5kHz Modulating Signal	DN88	2	2	LTC1278
	Tiny LTC1286 12-Bit Differential-Input Data-Acquisition System with LT1019-2.5 Reference	AN62	17	27	LTC1286, LT1019-2.5
	TMS32010 Interface	LTC1273/5/6 DS	20	20	LTC1273/LTC1275/LTC1276
		LTC1282 DS	20	23	LTC1282
	TMS320C25 Interface	LTC1273/5/6 DS	19	17	LTC1273/LTC1275/LTC1276
		LTC1282 DS	19	20	LTC1282
	Two LTC1257 12-Bit Voltage Output DACs Set the Input Span of an LTC1296 12-Bit, 8-Channel ADC	LTM V:3	27	3	LTC1257, LTC1296

Converters—Data (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
A/D 12-Bits (Continued)	2-Channel, 12-Bit, Self-Calibrating Data-Acquisition System	LTC221/222 DS	1	NA	LTC221/222, LT1006, LT1027, LTC1292
	Ultralow Full-Scale Drift LTC1273 3V A/D Converter	AN62	16	26	LTC1273, LT1019A-2.5
	Unipolar Offset and Full-Scale Adjust Circuit	LTC1274/77 DS	16	11b	LTC1274/LTC1277
		LTC1279 DS	12	9b	LTC1279
		LTC1282 DS	14	11	LTC1282
	Using Two LTC1257 12-Bit Voltage Output DACs to Set the Input Span of the 12-Bit, 8-Channel LTC1296	AN67	5	3	LTC1296, LTC1257
	Using the LT1019-2.5 as an External Reference	LTC1410 DS	11	8b	LTC1410, LT1019-2.5
A/D 14-Bits	8-Channel, 14-Bit A/D Converter	LTC221/222 DS	7	NA	LTC221/LTC222, LTC1290, LT1027
A/D 16-Bits	16-Bit Analog to Digital Converter	LTC1052 DS	18	NA	LTC1052, LTC1043, LT1009
	Analog to Digital (16-Bits)	AN9	16	25	LTC1043, LTC1052
Acquisition	12-Bit Data-Acquisition Systems Communicate with Microprocessors Over 4 Wires	DN22	1	1	LTC1290
	12-Bit, Differential Input Data-Acquisition System	LTC1292/97 DS	1	NA	LTC1297, LT1027
	2-Channel, 12-Bit Data-Acquisition System	LTC1291 DS	1	NA	LTC1291
	Closed Loop Control with the LTC1090	DN13	2	2	LTC1092, LT1013
	Data-Acquisition System Showing Sample and Hold Synchronizing Circuitry	DN2	1	1	LTC1090
	Hardware and Software Interface to Intel 8051	LTC1291 DS	12	NA	LTC1291
	Hardware and Software Interface to Motorola MC68HC11	LTC1291 DS	11	NA	LTC1291
	Hardware and Software Interface to Intel 8051 Processor	LTC1292/97 DS	12	5	LTC1292/LTC1297
	Hardware and Software Interface to Motorola MC68HC11	LTC1292/97 DS	11	4	LTC1297

Converters—Data (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Acquisition (Continued)	LTC1283 3V, Single-Supply,10-Bit Data-Acquisition System	LTC1283 DS	1	NA	LTC1283
	Micropower Temperature and Voltage Measurement Sensor	AN67	45	59	LTC1392
	Multiplexed Input Data-Acquisition	LT1102 DS	8	NA	LT1102
	New Data-Acquisition System Communicates with Microprocessors Over 4 Wires	DN1	1	1	LTC1090
	Optoisolated, Multichannel Data-Acquisition System (10-Bit, 500V Iso)	DN10	2	1	LTC1090, LT1021-5
	PC-Based Data-Acquisition	AN34	3	2	LTC1099, LT1019-5
	"Quick Look" Circuit for the LTC1283	LTC1283 DS	22	NA	LTC1283
	"Quick Look" Circuit for the LTC1291	LTC1291 DS	19	NA	LTC1291
	"Quick Look" Circuit for the LTC1292	LTC1292 /97 DS	21	26	LTC1292
	Sneak-A-Bit Circuit	LTC1283 DS	22	NA	LTC1283
	Two-Wire Isolated and Powered 10-Bit Data-Acquisition System	DN19	2	1	LTC1092, LT1021-5
	Autoranging 8-Channel, 12-Bit Data-Acquisition System	AN62	7	8	LTC1257, LTC1296
D/A 8-Bits	LTC1329 Digitally Controls the Output of a Power Supply	AN67	7	5	LTC1329-50, LT1107
	LTC1329 Used to Null Op Amp's Offset Voltage	AN67	7	6	LTC1329-50, LT1006
D/A 12-Bits	12-Bit DAC and LT1220 Op Amp Create Variable Reference Voltages, Enhancing LTC1410 ADC's Input Range	LTM V:4	22	7	LT1220, LTC8043, LTC1410
	12-Bit DACs with Daisy-Chained Outputs	LTC1257 DS	1	NA	LTC1257
	12-Bit, 3V to 5V, Voltage Output DAC	LTC1451–53 DS	10	NA	LTC1451–53
	12-Bit, Single 5V Control System with Shutdown	LTC1257 DS	9	NA	LTC1257, LTC1297, LT1025A, LTC1050
	12-Bit, Single 5V Temperature Control System with Shutdown	AN67	8	7	LTC1257, LTC1297, LTC1050, LT1025A

Converters—Data (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
D/A 12-Bits (Continued)	2-Quadrant Multiplying DAC Has Less Than 0.5LSB (typ) Total Unadjusted Error	LTC7541A DS	1	NA	LTC7541A, LT1097
	2nd Order Active Lowpass Filter Placed Between LTC1390 Multiplexer and LTC1286 12-Bit DAC	DN112	2	4	LT1366, LTC1390, LTC1286
	Autoranging 8-Channel ADC with Shutdown	LTC1257 DS	9	NA	LTC1257, LTC1296
	Bipolar (4-Quadrant Multiplying) DAC	LTC7543/ 8143 DS	7	NA	LTC7543/LTC8143, LT1112
		LTC8043 DS	4	NA	LTC8043, LT1112
	CMOS DAC with Low Drift Full-Scale Trimming	LT1236 DS	9	NA	LT1236-10, LTC7543, LT1007
	Computer Controlled 4–20mA Current Loop	AN67	6	4	LTC1453, LT1121-3.3, LT1077
	DAC I-to-V Converter	LT1358/59 DS	1	NA	LT1358
		LT1357 DS	1	NA	LT1357
	DAC with External Reference	LTC1257 DS	8	NA	LTC1257, LT1021-10
	DACs with Daisy-Chained Control Outputs	LTC1451–53 DS	1	NA	LTC1451
	Digitally Programmable Current Source	LTC1451–53 DS	10	NA	LTC1451, LT1077
	Driving the LTC1257 with Optoisolators	LTC1257 DS	10	NA	LTC1257, LT1021-5
	Easy Stand-Alone Application for the LTC1446 or LTC1446L	DN131	2	2	LTC1446/LTC1446L
	Filtering V_{REF} and V_{OUT}	LTC1257 DS	8	NA	LTC1257
	Isolated 4–20mA Current Loop	LTM V:3	31	4	LTC1453, LT1121-3.3, LT1077
	Isolated 4mA–20mA Process Controller with 3.3V Minimum Loop Voltage	LTC1451–53 DS	9	NA	LTC1453, LT1121-3.3, LT1077
	Low Power Triple DAC	LTC8043 DS	6	NA	LTC1043, LT1179, LT1004-1.2
	LTC1392 Temperature and Voltage Measurement Circuit	LTM V:2	12	5	LTC1392

Converters—Data (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
D/A 12-Bits (Continued)	LTC1453 Operating on a Single 2.7V to 5V Supply	DN96	1	2	LTC1453
	Multiplying DAC with Easy 3-Wire Serial Interface	LTC7543/ 8143 DS	1	NA	LTC7543/LTC8143, LT1097
	Optoisolated, Digitally Controlled, 4mA to 20mA Process Controller with 3.3V Minimum Loop Voltage	DN96	2	3	LTC1453, LT1121-3.3, LT1077
	Single 5V, 12-Bit Temperature Control System with Shutdown	AN62	6	6	LTC1257, LT1025A, LTC1297, LTC1050
	SO-8 Multiplying DAC with Easy 3-Wire Serial Interface	LTC8043 DS	1	NA	LTC8043, LT1097
	Two LTC1257 12-Bit Voltage Output DACs Set the Input Span of an LTC1296 12-Bit, 8-Channel ADC	LTM V:3	27	3	LTC1297, LTC1257
	Unipolar (2-Quadrant Multiplying) DAC	LTC7541A DS	4	NA	LTC7541A, LT1097
		LTC7543/ 8143 DS	6	NA	LTC7543/LTC8143, LT1097
		LTC8043 DS	4	NA	LTC8043, LT1097
	Using 2 LTC1257 12-Bit Voltage Output DACs to Set the Input Span of the 12-Bit, 8-Channel LTC1296	AN67	5	3	LTC1257, LTC1296
	Wide Swing, Bipolar Output, 12-Bit DAC	LTC1451–53 DS	11	NA	LTC1451, LT1077
	Wide-Swing Bipolar DAC with Digitally Controlled Offset	DN131	2	4	LTC1446, LT1077
Discussion	Overvoltage Protection for MUX	LTC1290 DS	23	NA	LTC1290
Infrared Data Communications	IrDA™-SIR 4ppm Data Receiver	LTM V:2	9	2	LT1319
Low Power	3V Powered, 12-Bit Data-Acquisition System	LT1289 DS	1	NA	LTC1289, LTC1097, LTC1044
	LTC1282 3V A/D Converter with Full-Scale Adjust	AN62	16	24	LTC1282, LT1006
	Ultralow Full-Scale Drift LTC1282 3V A/D Converter	AN62	16	25	LTC1282, LT1019A-2.5

Converters—Data (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Micropower	3V Battery Powered, 10µW, 8-Bit A/D, Sample at 200Hz	LTC1096 DS	1	NA	LTC1096
Voltage to Bits	LTC1392 Temperature and Voltage Measurement Circuit	LTM V:2	12	5	LTC1392

Current

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Sensing	18ns Circuit Breaker with Voltage Programmable Trip Point	AN47	66	144	LT1016, LT1193
	5V/1A Electronic Circuit Breaker with 1ms Trip Delay	LTC1153 DS	1	NA	LTC1153
		AN53	15	31	LTC1153
	Circuit Breaker (12ns)	AN13	24	40	LT1016
	Circuit Breaker (700ns)	AN1	3	3	LT1005
	Dual 2A Circuit Breaker with Auto-Reset	LTC1155 DS	9	NA	LTC1155
	Fast High-Side, High Current Limit	AN30	44	89	LT1072CN8, LT317AH
	Ground Current-Sense Amplifier	LT1213/14 DS	16	NA	LT1213
	Hall-Effect Stabilized Current Transformer	AN61	19	24	LT1228
	High-Side Current Sense Amplifier	AN66	78	154	LT1366
	High-Side Power Supply Current Sensing	LTC1152 DS	8	NA	LTC1152, LT1097
	In-Line Current Limiter	LM134 DS	11	NA	LM334
	Positive Supply Rail Current Sense	LT1366–69 DS	1	NA	LT1366
	Precision Current Sensing in Supply Rails	LTC203 DS	11	NA	LTC203
		LTC1043 DS	15	NA	LTC1043
		AN3	13	18	LTC1043

Current (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Sink	1A Voltage-Controlled Current Sink	LT1211/12 DS	16	NA	LT1211
	Precision Current Sink	LT1001 DS	8	NA	LT1001
Source	1A Voltage-Controlled Current Source	LT1211/12 DS	16	NA	LT1211
	2-Terminal Current Regulator	LM10 DS	11	NA	LM10
	2-Terminal Current Source	LT1077 DS	10	NA	LT1007, LT1034-1.2
	20mA Positive Current Source	LM129 DS	1	NA	LM329, LT1001
	Basic 2-Terminal Current Source	LM134 DS	8	NA	LM334
	Bidirection Current Source	AN16	19	48	LT1012, LT1010
	Bilateral Current Source	LM108 DS	6	NA	LM108
	Controlled Gain Voltage-to-Current Converter (Current Source)	LT1251/56 DS	16	NA	LT1256, LT1363
	Current Regulator	LT137 DS	7	NA	LT337A
		LT1033 DS	6	NA	LT1033
	Differential Voltage-to-Current Converter	LTC1051/53 DS	12	NA	LTC1053
	Digitally Programmable Current Source	LTC1451–53 DS	10	NA	LTC1451, LT1077
	Fast, Differential Input Current Source	LT1022 DS	6	NA	LT1022
	Fast, Precise, Voltage Controlled Current Source with Grounded Load	AN47	65	140	LT1190, LT1194
	FET Cascoding for Low Capacitance and/or Ultrahigh Output Impedance	LM134 DS	11	NA	LM334
	Ground-Referenced Current Source	LT1004 DS	5	NA	LT1004, LT1007
	High Power, Wideband, Voltage Controlled Current Source	AN47	65	142	LT1190, LT1194
	High Precision, Low Temperature Coefficient Current Source	LM134 DS	10	NA	LM334, LT1004-1.2
	High-Side Current Source	LT1366–69 DS	17	7	LT1366, LT1004-1.2
	Higher Output Current	LM134 DS	8	NA	LM334

Current (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Source (Continued)	Low Temperature Coefficient, 2-Terminal Current Source	LT1004 DS	6	NA	LT1004-1.2, LM334
	Micropower Bias	LM134 DS	9	NA	LM334
	Precision 10nA Current Source	LM134 DS	10	NA	LM334, LT1008
	Precision Current Source	LT1001 DS	8	NA	LT1001
	Precision Current Source (1μA)	LT1019 DS	7	NA	LT1019-2.5, LT1012
		LT1021 DS	12	NA	LT1021-7, LT1001
	Topside Current Source	LTM IV:3	15	5	LT1366
		AN66	78	153	LT1366
	Voltage Controlled Current Source	AN16	20	49	LT1010
	Voltage Controlled Current Source with Compensating Temperature Coefficient	AN67	82	134	LT1006
	Voltage Controlled Current Source with Ground Referred Input and Output	LT1013 DS	17	NA	LT1013, LTC1043
		AN3	13	17	LT1013, LTC1043
	Voltage Programmable Current Source	LT1102 DS	8	NA	LT1006, LT1102
		AN45	5	8	LT1006, LT1102
	Voltage Programmable Current Source is Simple and Precise	DN40	2	4	LT1006, LT1102
	Voltage Controlled Current Source with a Compensating Temperature Coefficient	LTM II:3	16	3	LT1006
	Zero Temperature Coefficient Current Source	LM134 DS	8	NA	LM334

Current Loop

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Receiver	4mA–20mA Loop Receiver	LT1101 DS	11	NA	LT1101, LT1004-1.2

Current Loop (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Transmitter	2-Wire 0°C to 100°C Temperature Transducer with 4mA–20mA Output	LTC1040 DS	11	NA	LTC1040, LT1019-5, LM134
	4mA–20mA Current Loop Transmitter	AN11	9	10	LT1013, LT1004-1.2
		LT1013 DS	14	NA	LT1013, LT1004-1.2
	4mA–20mA Floating Output for Current Loop Transmitter	AN11	10	11	LT1013
		LT1013 DS	14	NA	LT1013, LT1004-1.2
	Digitally Controlled 4mA–20mA Current Loop Generator	AN31	6	11	LT1072, LT1006
	Fully Floating 4mA–20mA Current Loop Transmitter	AN45	6	10	LT1078, LT1006, LT1004-1.2

Data-Acquisition (see Converters—Data, Acquisition)

DC/DC (see Regulators—Switching)

Detectors (see Signal Conditioning)

Digital Help Circuits

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Additional Feature Circuits	Battery Detectors Sense Removal of Main Battery	AN51	17	24	LT1173
	Battery Discharge Monitor	LTC1150 DS	11	NA	LTC1150
	Logic System DC Isolation	LTC1045 DS	11	NA	LTC1045
	Pushbutton Reset for LTC694-3.3/LTC695-3.3	LTC694/5-3.3 DS	14	13	LTC694-3.3/LTC695-3.3
Battery Backup	Battery Backup Monitor with Optional Test Load	LTC694/5-3.3 DS	12	10	LTC695-3.3
		LTC692/93 DS	12	10	LTC693

Digital Help Circuits (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Battery Backup (Continued)	Capacitor Backup with 74HC4016 Switch	LTC694/5-3.3 DS	14	NA	LTC695-3.3
EEPROM	EEPROM Pulse Generator	LT1013 DS	12	NA	LT1013, LT1004
	EEPROM VPP Pulse Generator	AN31	5	9	LT1072, LT1006, LT1010
EPROM	VPP Generator for EPROMs—No Trim Required	LT1004 DS	7	NA	LT1004, LM301A
Flash Memory	2V Powered Flash-Memory VPP Generator	LT1109A DS	6	NA	LT1109A-12
	3.3V Powered Flash-Memory VPP Generator	LT1109A DS	6	NA	LT1109A-12
	All Surface Mount Flash Memory VPP Generator	AN52	13	18	LT1109-12
		DN58	1	1	LT1109-12
		LT1109 DS	1	NA	LT1109-12
		LT1110 DS	14	NA	LT1110-12
		LT1109A DS	1	NA	LT1109A-12
	Alternative Scheme Allows 12V from VPP1/VPP2 to Provide Power when LT1106 is in Shutdown Mode	LT1106 DS	8	NA	LT1106
	Basic Flash Memory VPP Programming Voltage Supply	AN31	1	1	LT1072
		DN17	1	1	
	Flash Memory VPP Generator Delivers 12V	AN51	19	26	LT1173
	High Power, High Repetition Rate VPP Pulse Generator	AN31	3	7	LT1072, LT1006, LT1004
	High Repetition Rate VPP Programming Supply	AN31	2	4	LT1072, LT1006, LT1010, LT1004
		DN17	2	3	
	LTC1262 Typical Application (Flash-Memory Programming Supply)	LTC1262 DS	1	NA	LTC1262
	Paralleling LTC1262s	LTC1262 DS	6	NA	LTC1262
	VPP Handshake Circuit	AN31	4	8	LT1018, LT1004

Digital Help Circuits (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Notebook Computer	4-Cell NiCd Computer Power Management Systems	LTC1156 DS	1	NA	LTC1156
		AN53	11	23	LTC1156, LT1431
	Bidirectional Battery Switch	AN53	3	7	LTC1154
	Logic-Controlled Battery Switch	LTC1255 DS	11	NA	LTC1255
		LTC1157 DS	7	NA	LTC1157
		LTC1153 DS	12	NA	LTC1153
	LT1521's 12µA Standby Current Eliminates the Need for a Separate Memory Backup Supply	DN121	1	1	LT1521-5, LTC1477
	Slow Turn-On Power Switch	LTC1154 DS	9	3	LTC1154
Supply Monitor	10Ω/0.1µF Combination Eliminates Inductive Overshoot and Prevents Spurious Resets During Battery Replacement	LTC694/5-3.3 DS	10	4	LTC694-3.3/LTC695-3.3
		LTC692/93 DS	10	4	LTC692/LTC693
	5V Power Supply Monitor	LT1017 DS	6	NA	LT1017, LT1034
	6V Battery Level Indicator	LM10 DS	12	NA	LM10
	AC-DC Dropout Detector	AN31	7	14	LT1018, LT1004
	Battery Backup Monitor with Optional Test Load	LTC694/5-3.3 DS	12	10	LTC695-3.3
		LTC692/93 DS	12	10	LTC693
	Battery Voltage Sensing Circuit	LT1005 DS	10	NA	LT1005
		LT1035 DS	10	NA	LT1035
	Capacitor Backup with 74HC4016 Switch	LTC694/5-3.3 DS	14	NA	LTC695-3.3
	Charging an External Battery Through V_{OUT}	LTC692/93 DS	9	3	LTC692/LTC693
		LTC694/5-3.3 DS	9	3	LTC694.3.3/LTC695-3.3
	Delay on Power Up	LT1017 DS	8	NA	LT1017, LT1018
	Lead-Acid Low Battery Detector	LT1004 DS	7	NA	LT1004-1.2

Digital Help Circuits (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Supply Monitor (Continued)	Data-Acquisition System Battery-Current Monitor	AN62	9	11	LTC1297, LT1121, LTC1047, LT1004
	LTC692/93/95 Typical Application	LTC692/93 DS	1	NA	LTC692/LTC693, LT1086-5
		LTC694/5-3.3 DS	1	NA	LTC695-3.3, LT1129-3.3
	Micropower Battery Current Monitor Using the LTC1297 12-Bit Data-Acquisition System	AN67	9	8	LTC1297, LTC1047, LT1121, LT1004
	Microprocessor Supervisory Circuit	LTC1232 DS	1–8	NA	LTC1232
		LTC690 DS	1–16	NA	LTC690/LTC691/LTC694/LTC695
	Monitoring Regulated DC Supply with the Power-Fail Comparator	LTC692/93 DS	11	9	LTC692/LTC693, LT1086-5
		LTC694/5-3.3 DS	11	9	LTC694-3.3/LTC695-3.3, LT1129-3.3
	Monitoring Unregulated DC Supply with the Power-Fail Comparator	LTC692/93 DS	11	8	LTC692/LTC693, LT1086-5
		LTC694/5-3.3 DS	11	8	LTC694-3.3/LTC695-3.3, LT1129-3.3
	Power Supply Monitor	DN20	2	4	LTC1045
		LT1018 DS	7	NA	LT1018, LT1004-1.2
	TTL Power Supply Monitor	LTC1042 DS	6	NA	LTC1042, LT1004-2.5
	Typical Nonvolatile CMOS RAM Application	LTC694/5-3.3 DS	11	6	LTC695-3.3
		LTC692/93 DS	11	6	LTC693
	Using BATT ON to Drive an External PNP Transistor	LTC692/93 DS	9	2	LTC693
		LTC694/5-3.3 DS	9	2	LTC695-3.3
	Write Protect for Additional RAM	LTC694/5-3.3 DS	15	NA	LTC695-3.3

Digital Help Circuits (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Supply Monitor (Continued)	Write Protect for RAM	LTC694/5-3.3 DS	11	7	LTC694-3.3
		LTC692/93 DS	11	7	LTC692
Watchdog Timer	LTC692/93/95 Typical Application	LTC692/93 DS	1	NA	LTC692/LTC693, LT1086-5
		LTC694/5-3.3 DS	1	NA	LTC695-3.3, LT1129-3.3
	Watchdog Timer	AN31	10	22	LT1018

Distortion Measurements

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Discussion	Understanding Distortion Measurements	AN43	44	NA	NA

Drift

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Discussion	Minimizing Thermal EMFs	AN9	2	2–4	NA

Drivers

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Capacitor	Slew Rate Reduction for Large Capacitive Loads	AN53	3	5	LTC1154, LT1121-5

Drivers (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
CCD	CCD Clock Driver	DN132	2	3	LT1207
High-Side	18V–28V High-Side Driver	AN53	4	8	LTC1155
	2-Cell to 3.3V, 5V and 12V High-Side Switch/ Converter with 0.01µA Standby Current	LTC1163/65 DS	7	NA	LTC1163/LTC1165, LT1109, LT1173
	2-Cell, Triple High-Side Switch	LTC1163/65 DS	1	NA	LTC1163/LTC1165
	Dual High-Side 3.3V Switch	AN53	12	26	LTC1157
		LTC1157 DS	1	NA	LTC1157
	High-Side Driver with Reverse Battery Protection	AN53	9	19	LTC1154
	Laptop Computer Power-Bus Switching	LTM I:2	7	2	LTC1155
	LTC1157 Used to Switch Two 3.3V Loads	LTM II:3	13	3	LTC1157
	Mixed-Voltage, High- and Low-Side Switches	LTC1163/65 DS	8	NA	LTC1163/LTC1165
	Ultralow Drop, Triple 3.3V High-Side Switch	LTC1163/65 DS	7	NA	LTC1163/LTC1165
High-Side, Isolated	300V Isolated High-Side Driver	LTC1145/46 DS	9	NA	LTC1145
	Fully Isolated, Quad High-Side Switch	AN66	85	165	LT1161
		LTM IV:1	21	1	LT1161
	Isolated High-Side Driver	LTM IV:1	25	1	LTC1146A
		AN66	79	155	LTC1146A
		LTC1177-5 DS	1	NA	LTC1177-5/LTC1177-12
	Isolated High-Side Switch with Foldback Current Limit	LTC1177-5 DS	6	NA	LTC1177-5/LT1177-12
Lamp	12V Lamp Driver/Circuit Breaker	AN53	8	17	LTC1154
		LTC1154 DS	9	4	LTC1154
	12V Lamp Driver/Circuit Breaker with Auto-Reset	LTC1153 DS	12	NA	LTC1153
	High Current Lamp Driver with Short-Circuit Protection	LT1158 DS	20	18	LT1158

Drivers (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Low-Side	Mixed-Voltage High- and Low-Side Switches	LTC1163/65 DS	8	NA	LTC1163/65
Motor	DC Motor Driver with Stall-Current Circuit Breaker, Thermal-Overload Shutdown and 10µA Standby Current	LTC1153 DS	14	NA	LTC1153
Power MOSFET	200W Class D, 10Hz to 1kHz Amplifier	LT1160 DS	13	6	LT1162, LT1015, LT1016, LT1058
Relay	Relay Driver with Overcurrent Protection	LTC1154 DS	12	NA	LTC1154
		LTC1153 DS	12	NA	LTC1153
	Solid-State Relay	LTC1177 DS	7	NA	LTC1177-5/LTC1177-12
Solenoid	Driving Inductive Loads	LT1188 DS	6	NA	LT1188
		LTC1153 DS	8	2	LTC1153
		LTC1154 DS	8	2	LTC1154
	High-Side Solenoid Driver with Overcurrent Protection	LTC1255 DS	1	NA	LTC1255

Drivers/Receivers (see Interface Circuits)

Fiber Optics (see Signal Conditioning, Photodiode)

Filters—Active RC

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Allpass	3.58MHz Phase Shifter	LT1251 DS	19	NA	LT1256/LT1253
Bandpass	Bandpass Filter with Adjustable Q	LTM V:2	31	1	LT1228
		AN67	28	30	LT1228
	100kHz, 4th Order Butterworth Filter	LT1354 DS	1	NA	LT1354
		LT1355/56 DS	1	NA	LT1355

Filters—Active RC (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Lowpass	100kHz, 4th Order Butterworth Filter (Sallen-Key)	LT1355/56 DS	11	NA	LT1355
		LT1354 DS	1	NA	LT1354
	1kHz, 4th Order Butterworth Filter	AN67	32	37	LT1367
	1kHz, 4th Order Butterworth Lowpass Filter	LTM IV:3	16	7	LT1367
	1MHz, 2nd Order Butterworth Filter	LT1224 DS	7	NA	LT1224
	1MHz, 4th Order Butterworth Filter	LT1360 DS	11	NA	LT1360
		LT1361/62 DS	11	NA	LT1361
	200kHz, 4th Order Butterworth Filter	LT1358/59 DS	11	NA	LT1358
		LT1357 DS	11	NA	LT1357
	2MHz, 4th Order Butterworth Filter	LT1364/65 DS	11	NA	LT1364
		LT1363 DS	11	NA	LT1363
	2nd Order Butterworth Filter (to 100kHz)	LT1200 DS	7	NA	LT1200
	2nd Order Active Lowpass Filter Placed Between LTC1390 Multiplexer and LTC1286 12-Bit A/D	DN112	2	4	LT1366, LTC1390, LTC1286
	3rd Order Sallen and Key Lowpass Filter	LTM V:2	32	1	LT1007
	4th Order Butterworth Filter (to 100kHz)	LT1201 DS	1	NA	LT1201
	4th Order Butterworth Filter (to 1MHz)	LT1208 DS	1	NA	LT1208
	DC Accurate, 18-Bit, 4th Order Antialiasing Bessel (Linear-Phase) 100Hz, Lowpass	LTC1051 DS	15	NA	LTC1051
	DC Accurate, 3rd Order, 100Hz, Butterworth Antialiasing Filter	LTC1051 DS	15	NA	LTC1051
	Precision, Fast Settling, Lowpass Filter	LT1008 DS	10	NA	LT1008, LT311A
	Sallen and Key Lowpass Filter	AN67	22	25	LT1007
	Single-Supply, 3-Pole, 1MHz Butterworth Filter	LT1213/14 DS	1	NA	LT1213
	Single-Supply, 100kHz, 4th Order Butterworth Lowpass Filter	LT1211/12 DS	16	NA	LT1212

Filters—Active RC (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Lowpass (Continued)	Single-Supply, 1kHz, 4th Order Butterworth	DN89	2	2	LT1367
State-Variable	Four-Pole, 1kHz, 3.3V Single-Supply, State-Variable Filter	LT1366–69 DS	17	8	LT1367
	State-Variable Filter with Adjustable Frequency and Q	LT1251/56 DS	20	NA	LT1256, LT1252
	Variable Lowpass, Highpass and Allpass Filter	LT1251/56 DS	18	NA	LT1256, LT1252

Filters

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Discussion	Application Condiserations for an Instrumentation Lowpass Filter	AN20	1–12	(1–27)	LTC1062
	Complex Data-Acquisition System, Few Components	DN24	1	NA	LTC1062, LTC1069, LT1007
	Design of Bandpass Filters	AN27A	NA	NA	NA
	Level Shifting the Input T^2L Clock	LTC1064-1 DS	5	3	LTC1064-1
	Level Shifting the Input T^2L Clock	LTC1064-2 DS	8	4	LTC1064-2
	Protecting the IC from Power Supply Reversal	LTC1064-1 DS	5	3	LTC1064-1
		LTC1064-2 DS	7	2	LTC1064-2
	Square Wave to Sine Wave Converter	AN40	23	NA	LTC1064-1
	Switched Capacitor LPF for Antialiasing Applications	DN16	1	NA	LTC1064-1
	Take the Mystery out of the Switched Capacitor Filter	AN40	NA	NA	NA

Filters (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Discussion (Continued)	Using Schottky Diodes to Protect the IC	LTC1064-1 DS	5	1	LTC1064-1
Resonant Element	Crystal Filter	AN47	48	109	LT1221
	LC Bandpass Filter with Adjustable Q	LTM V:2	31	1	LT1228
		AN67	28	30	
	Piezo-Ceramic Based Filter	AN47	48	106, 108	LT1190

Filters—Switched Capacitor

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Allpass	Allpass Network Configuration Using the LTC1064	AN56	10	B2	LTC1064, LT1056
Bandpass	10Hz–100Hz, 10Hz–1kHz and 400Hz–10kHz Bandpass Filter	DN24	2	2	LTC1064, LTC1062, LT1007
	10kHz–100kHz Bandpass Filter	DN37	2	2	LTC1064, LT1122, LT1064-4
	1kHz Tone Detector with Gain of 10	LTM V:2	25	3	LTC1164-8, LT1013, LTC1040
		AN67	26	29	LTC1164-8, LT1013, LTC1040
	4th Order Butterworth BPF, f_O = 2kHz	AN27A	1–2	1–3	LTC1060/LTC1061/LTC1064
	6th Order Elliptic Bandpass Filter Centered Around 2600Hz	LTC1061 DS	10–11	12–13	LTC1061
	6th Order, Clock-Tunable, 0.5dB Ripple Chebyshev BPF	LTC1061 DS	1	NA	LTC1061
	8th Order Bandpass (to 100kHz)	LTC1264 DS	15	NA	LTC1264
	8th Order Bessel Bandpass (to 250kHz)	LTC1264 DS	15	NA	LTC1264
	8th Order Chebyshev BPF at 10.2kHz	AN27A	15	15	LTC1064
	Bandpass with 2 Notches (–60dB Stopband)	LTC1064 DS	12	NA	LTC1064
	C Message Filter	LTC1064 DS	12	NA	LTC1064

Filters—Switched Capacitor (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Bandpass (Continued)	Cascading Identical Sections 4th Order BPF at 150Hz	AN27A	4	4	LTC1060
	Clock Sweepable Pseudobandpass Filters	AN24	4	5	LTC1062
	Dual 4th Order Bandpass (to 250kHz)	LTC1264 DS	13	NA	LTC1264
	High Frequency, Clock-Tunable Bandpass Filter	LTC1043 DS	13	NA	LTC1043, LT1056
	Linear-Phase, 8th Order Bandpass Filter	LTM III:3	28	1	LTC1264
	Mode 2/4th Order BPF at 150Hz	AN27A	5	6	LTC1060
	Quad Bandpass Filter	LTC1064 DS	11	NA	LTC1064, LT1056
	Single 5V, Gain of 1000 4th Order Bandpass Filter	LTC1060 DS	1	NA	LTC1060
	Single-Supply, 8th Order Bandpass Filter	AN67	37	46	LTC1264
	Single-Supply, Clock-Tunable, 8th Order Bandpass Filter	LTM IV:1	20	1	LTC1264
	Tone Detector and Average Value Circuit	LTC1164-8 DS	9	NA	LTC1164-8, LT1413
	Tone Detector—Detecting a Signal Buried in Wideband Noise	LTC1164-8 DS	10	NA	LTC1164-8, LT1413, LTC1040
	Ultranarrow 1kHz Bandpass Filter	LTC1164-8 DS	1	NA	LTC1164-8, LT1006
	Ultranarrow 1kHz Bandpass Filter with Adjustable Gain	AN67	30	33	LTC1164-8
		LTM IV:3	6	2	LTC1164-8, LT1006
	Wide Range 2nd Order Bandpass/Notch Filter with Q = 10	LTC1059 DS	1	NA	LTC1059
	Wideband (2:1) Bandpass	LTC1064 DS	11	NA	LTC1064
	Wideband, DC-Accurate BPF	DN9	2	2	LTC1062, LTC1050
	Linear-Phase, 8th Order Bandpass Filter	AN67	39	49	LTC1264
Low Power	8th Order Lowpass Butterworth	LTC1164 DS	12	11	LTC1164, LT1056
	8th Order Lowpass Elliptic Filter	LTC1164 DS	14	13	LTC1164, LT1006
	8th Order Lowpass, Single-Supply, Elliptic-Bessel Filter	LTC1164 DS	13	12	LTC1164, LT1006

Filters—Switched Capacitor (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Low Power (Continued)	9th Order Lowpass Elliptic Filter	LTC1164 DS	15	15	LTC1164, LT1006
	Dual 5th Order Linear-Phase Filter with Stopband Notch	LTC1164 DS	1	NA	LTC1164
Lowpass	100Hz, 50Hz, 25Hz 5th Order DC Accurate LP Filter	LTC1062 DS	9	NA	LTC1062
	100kHz 7th Order Butterworth or Bessel Lowpass Filter with Rail-to-Rail Input and Output	LTM V:4	23	1	LTC1063/LTC1065, LT1366
	100kHz Elliptic Lowpass Filter with Input Antialiasing and Output Clock Feedthrough Filters	LTC1066-1 DS	16	NA	LTC1066-1
	10Hz DC Accurate Bessel LPF	DN9	1	1	LTC1062, LTC1050
	16th Order Butterworth Lowpass Filter	LTM II:2	18	1	LTC1164-5
	20Hz 5th Order Butterworth Lowpass Filter	LTC1062 DS	1	NA	LTC1062
	20Hz Bessel Lowpass Filter with 60Hz Notch	LTM V:4	24	5	LTC1065, LT1366
	5th Order Lowpass Filter	LTC1062 DS	10	NA	LTC1062
	5th Order Lowpass Filter with a 60Hz Notch	LTC1062 DS	11	NA	LTC1062, LT1013
	6th Order Butterworth Lowpass Filter Cutoff to 45kHz	LTC1061 DS	7	5	LTC1061
	6th Order Chebyshev Filter Using 3 Different Modes for Speed Optimization	LTC1061 DS	8	8	LTC1061
	7th Order 100Hz Lowpass Filter with Continuous Filtering, Output Buffering	LTC1062 DS	10	NA	LTC1062, LTC1052
	7th Order Lowpass Elliptic Filter	LTC1061 DS	11–12	16, 19	LTC1061, LT1056
	8Hz 5th Order Butterworth LPF	DN7	1	1	LTC1062
	8th Order Bessel to 95kHz	LTC1064-3 DS	1–8	NA	LTC1064-3
	8th Order Bessel with 65:1 f_{CLK}/f_O Ratio	LTC1064 DS	14	NA	LTC1064
	8th Order Butterworth to 140kHz	LTC1064-2 DS	1–8	NA	LTC1064-2
	8th Order Cauer 40kHz LPF	DN16	2	3	LTC1064-1
	8th Order Cauer Cutoff up to 100kHz	LTC1064 DS	1	NA	LTC1064

Filters—Switched Capacitor (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Lowpass (Continued)	8th Order Cauer to 100kHz	LTC1064-4 DS	1–8	NA	LTC1064-4
	8th Order Chebychev, up to 100kHz, Ripple 0.1dB	LTC1064 DS	13	NA	LTC1064
	8th Order, Clock-Sweepable Lowpass Butterworth Filter	LTC1064-2 DS	1	NA	LTC1064-2
	8th Order Elliptic (to 150kHz)	LTC1264 DS	14	NA	LTC1264
	8th Order Elliptic Antialiasing Filter	LTC1064-1 DS	1	NA	LTC1064-1
	8th Order Elliptic Lowpass Filter with 2-Pole Butterworth Input Antialiasing Filter	LTM IV:2	14	7	LTC1066-1
	8th Order Lowpass Butterworth	LTC1164 DS	12	11	LTC1164, LT1056
	8th Order Lowpass Elliptic Filter	LTC1164 DS	14	13	LTC1164, LT1006
	8th Order Lowpass, Single-Supply Elliptic-Bessel Filter	LTC1164 DS	13	12	LTC1164, LT1006
	9th Order Lowpass Elliptic Filter	LTC1164 DS	15	15	LTC1164, LT1006
	Adding a 2-Pole Butterworth Input Antialiasing Filter to 8th Order Elliptic Lowpass Filter	AN67	37	45	LTC1066-1
	Buffering the Filter Output	LTC1064-1 DS	6	4	LTC1064-1
	Cascading Two LTC1062s	AN20	7	12	LTC1062
	Cascading Two LTC1062s Using the First LTC1062s Buffered Output	AN20	7	13	LTC1062
	Clock-Tunable, DC-Accurate, 800Hz to 80kHz Elliptic Lowpass Filter	LTC1066-1 DS	1	NA	LTC1066-1
	DC Accurate, Clock-Tunable 10th Order Butterworth	LTC1063 DS	11	NA	LTC1063
	DC Accurate, Clock-Tunable 5th Order Butterworth	LTC1063 DS	1–12	NA	LTC1063
	DC-Accurate Lowpass Filter with Input Antialiasing	LTC1066-1 DS	14	NA	LTC1066-1

Filters—Switched Capacitor (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Lowpass (Continued)	DC-Accurate, 10Hz to 100kHz, 8th Order Elliptic Lowpass Filter	LTM IV:2	13	4	LTC1066-1
		AN67	35	41	
	DC-Accurate, Clock-Tunable Lowpass Filter with Input Antialiasing	LTM IV:2	25	2	LTC1066-1, LTC1045, LTC202
		AN67	34	40	
		LTC1066-1 DS	15	NA	
	DC-Accurate, Programmable-Cutoff, 5th Order Butterworth Lowpass Filter	LTM II:3	22	1	LTC1063, LT1007
	Dual 4th Order Bessel Lowpass (to 400kHz)	LTC1264 DS	13	NA	LTC1264
	Dual 4th Order Bessel to 140kHz	LTC1064 DS	14	NA	LTC1064
	Dual 5th Order Chebychev, 50/100kHz Cutoff	LTC1064 DS	15	NA	LTC1064
	Dual 5th Order Elliptic/Bessel	LTC1064-1 DS	7	NA	LTC1064-1, LT1056
	Dual-Supply Operation, DC-Accurate, 10Hz–100kHz, Clock-Tunable 8th Order Elliptic Lowpass Filter	LTC1066-1 DS	13	NA	LTC1066-1
	Filtering AC Signals from High DC Voltages	LTC1062 DS	7	NA	LTC1062
	Low Frequency, 5Hz Filter	AN20	11	23	LTC1062
	Low Offset, 12th Order, Maximum Flat Lowpass Filter	AN20	8	15	LTC1062, LTC1051
	Low Power, 16th Order Butterworth Lowpass	AN52	10	12	LTC1164-5
	Low Power, 8th Order Elliptic Lowpass	LTC1164-6 DS	10	NA	LTC1164-6, LT1006
	Lowpass Filter with a 60Hz Notch	AN20	10	21	LTC1062, LT1013
	Output Buffer Eliminates Clock Feedthrough	LTC1064-1 DS	7	NA	LTC1064-1, LT1056
	Programmable Cutoff, Fifth Order Butterworth Lowpass	AN52	11	15	LTC1063, LT1007
	RC to Eliminate Clock Feedthrough and Improve HF Attenuation Floor	AN20	4	6	LTC1062, LTC1050
	Setting the LTC1065 Internal Clock with an External RC	LTM IV:1	11	3	LTC1065

Filters—Switched Capacitor (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Lowpass (Continued)	Simple Cascading Technique—LTC1062	LTC1062 DS	9	NA	LTC1062, LTC1052
	Single 5V, 5mA, 16th Order Butterworth Lowpass	LTC1164-5 DS	11	NA	LTC1164-5
	Single 5V, 5mA, 16th Order Elliptic Lowpass	LTC1164-6 DS	11	NA	LTC1164-6
	Single 5V Operation, DC-Accurate, 10Hz to 36kHz, Clock-Tunable, 8th Order Elliptic Lowpass Filter	LTC1066-1 DS	13	NA	LTC1066-1
	Single-Supply LTC1062	AN20	4	7	LTC1062
	Single-Supply Operation	LTC1064-2 DS	7	3	LTC1064-2
		LTC1064-1 DS	5	2	LTC1064-1
	The LTC1063 Operating as a Clock-Sweepable Lowpass Filter	LTM II:2	17	6a	LTC1063
	Transitional Elliptic/Bessel 10th Order	LTC1064-1 DS	6	NA	LTC1064-1, LT1056
	Typical Configuration for Dynamic Range Measurement	LTM IV:1	12	7	LTC1065, LT1022
	Using a Multiplexer to Obtain Four Different Cutoff Frequencies	AN24	8	14	LTC1062, LT311
	Using an Input Divider to Accommodate High Voltages	AN24	7	12	LTC1062
	Using the LTC1062 with Op Amps Operating from ±15V Power Supply	AN24	7	13	LTC1062, LT1013
Lowpass, Linear-Phase	Low Noise, 8th Order, Group-Delay Equalized Filter (to 100kHz)	LTC1064-7 DS	1–12	NA	LTC1064-7
	3.4kHz Single 5V Supply Bessel Lowpass Filter	LTC1065 DS	1	NA	LTC1065
	80kHz Linear-Phase Lowpass Filter	LTC1064-7 DS	1	NA	LTC1064-7
	Adding an Input Antialiasing RC	LTC1065 DS	11	10	LTC1065
	Adjusting $V_{OS(OUT)}$ for ±7.5V Operation	LTC1065 DS	12	NA	LTC1065, LT1009

Filters—Switched Capacitor (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Lowpass, Linear-Phase (Continued)	Cascading Two LTC1065's for Steeper Roll-Off	LTC1065 DS	11	NA	LTC1065
	Dual 5th Order Linear-Phase Filter with Stopband Notch	LTC1164 DS	1	NA	LTC1164
	Low Noise, 8th Order, Group-Delay Equalized Filter (to 250kHz)	LTC1264-7 DS	1–12	NA	LTC1264-7
	Low Power, 8th Order, Group-Delay Equalized Filter (to 20kHz)	LTC1164-7 DS	1–12	NA	LTC1164-7
	Sharing Clock for Multichannel Applications	LTC1065 DS	11	NA	LTC1065
	Single 5V Supply Operation	LTC1065 DS	12	NA	LTC1065
Noise	Bandpass Filters and Noise	AN40	19	NA	NA
	LTC1060 Wideband RMS Noise	LTC1060 DS	9	Table 2	LTC1060
	Noise in Switched Capacitor Filters	AN40	19	NA	NA
	Wideband RMS Noise	LTC1061 DS	14	Table 3	LTC1061
Notch	5th Order Lowpass Filter with a 60Hz Notch	LTC1062 DS	11	NA	LTC1062, LT1013
	60dB Notch Tunable 30kHz–90kHz	LTC1064 DS	15	NA	LTC1064, LT1056
	6th Order Bandreject Filter with 65dB Notch Depth	LTC1061 DS	11–12	16, 18	LTC1061, LT1056
	6th Order Elliptic Notch Centered at 2600Hz	LTC1061 DS	10–11	12, 13	LTC1061
	8th Order Notch (to 150kHz)	LTC1264 DS	14	NA	LTC1264
	Lowpass Filter with 60Hz Notch	AN20	10	21	LTC1062, LT1013
	Clock-Tunable Notch Filter	AN24	6	10	LTC1062
	Dual 4th Order Notch and Bandpass (to 150kHz)	LTC1264 DS	13	NA	LTC1264
	Using the LTC1062 to Create a Notch	AN20	9	18	LTC1062, LT1056
	Wide Range 2nd Order Bandpass/Notch Filter with Q = 10	LTC1059 DS	1	NA	LTC1059
Output Buffer	Buffering the Filter Output	LTC1064-1 DS	6	4	LTC1064-1, LT1022, LT318, LT1056
		LTC1064-2 DS	7	1	LTC1064-2, LT1006

Filters—Switched Capacitor (Continued)					
Category	**Subject**	**Publication**	**Page Number**	**Figure Number**	**LT Part Number(s)**
Output Buffer (Continued)	Output Buffer Eliminates any Clock Feedthrough	LTC1064-1 DS	7	NA	LTC1064-1
		LTC1064-2 DS	8	5	LTC1064-2, LT1056
Output Offsets	Equivalent Input Offsets of LTC1061	LTC1061 DS	14	23	LTC1061
	LTC1060 Offsets	LTC1060 DS	19	Table 5	LTC1060
	Output DC Offsets, One 2nd Order Section	LTC1064 DS	3	Table 1	LTC1064
	Output Offsets for Modes 1, 1b, 2 and 3	LTC1061 DS	14	Table 4	LTC1061

Flash Memory (see Digital Help Circuits; Memory, Flash)

Flow Measurement (see Signal Conditioning)

Function Generators					
Category	**Subject**	**Publication**	**Page Number**	**Figure Number**	**LT Part Number(s)**
Pulse	1.5V Powered 350ps Rise Time Pulse Generator	AN45	18	27	LT1073
		LT1073 DS	18	NA	
Ramp	Ramp Generator with Variable Reset Level	LF198 DS	10	NA	LF398, LT1004-1.2
	Staircase Generator	LF198 DS	12	NA	LF398, LT1004-1.2
Tri-Wave	Precise Tri-Wave Generator	LT1018 DS	6	NA	LT1018, LT1013, LT1009-2.5

Fuse, Electronic (see Current, Sensing)

Gas Sensor (see Signal Conditioning)

Ground Planes

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Discussion	About Ground Planes	AN13	29	NA	NA
		AN47	24	NA	NA

Hot Swap

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
	"Hot Swap" Circuit Using LTC1477 and LTC699	LTM V:3	32	1	LTC1477, LTC699

Inductance

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
DC/DC	Inductance Selection for Flyback Converters	AN29	38	D1	LT1070
Equivalent	Generating Negative Output Impedance	LM134 DS	11	NA	LM134

Instrumentation Amplifiers (see Amplifiers, Instrumentation)

Interface Circuits

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
ADSL	Twisted-Pair Driver ADSL	DN132	1	1	LT1210
AppleTalk®/ LocalTalk®	AppleTalk Transceiver with ≥25k ESD Protection	LTC1320 DS	7	NA	LTC1320

Interface Circuits (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
AppleTalk/ LocalTalk (Continued)	AppleTalk/LocalTalk Implemented with LTC1323CS-16 and LTC1334 Transceivers	LTC1334 DS	14	19	LTC1334, LTC1323
	IR LocalTalk Infrared Receiver	DN118	2	2	LT1319
	LocalTalk Implemented Using LTC1320 and LTC1335 Transceivers	LTC1321/22/ 35 DS	15	15	LTC1320, LTC1335
	LocalTalk/AppleTalk Interface	LTM IV:1	33	4	LTC1335
	LTC1323 Typical Application (AppleTalk Interface)	LTC1323 DS	1	NA	LTC1323
	PhoneNet® Application	DN85	2	4	LTC1491
		DN85	2	3	LTC1323
	Single 5V Supply AppleTalk Interface	LTC1320 DS	6	NA	LTC1320, LTC1046/LT1054
	Single-Supply LocalTalk Port	DN85	1	1	LTC1323
	Switched Negative Supply AppleTalk Transceiver	LTC1320 DS	7	NA	LTC1320
	Typical Application (DCE)	LTC1318 DS	1	NA	LTC1318
	Typical LocalTalk Connection	LTC1320 DS	1	NA	LTC1320
	Typical LocalTalk Connection for Low EMI	LTC1324 DS	1	NA	LTC1324
Coax	Coax Cable Driver/Receiver	LTC1045 DS	10	NA	LTC1045
DSP (Parallel)	LTC1272/LTC1273/LTC1275/LTC1276 to TMS32010 DSP Processor Parallel Interface	AN62	22	46	LTC1272/LTC1273/LTC1275/ LTC1276
	LTC1278 to TMS320C25 DSP Processor	AN62	22	47	LTC1278
	LTC1282 to TMS320C25 DSP Processor Parallel Interface	AN62	22	45	LTC1282
EIA562 and RS485	EIA562 and RS485 Interfaces with ±5V Supplies	LTC1321/22/ 35 DS	14	13	LTC1321/LTC1322/LTC1335
HDSL	Bridge Driver for HDSL	DN132	2	2	LT1207
	LT1206 Used as a Differential HDSL Transformer Driver	LTM V:1	27	4a	LT1206
	LT1206 Used as a Single-Ended HDSL Transformer Driver	LTM V:1	28	4b	LT1206
	LTC1278 HDSL Circuit with Programmable Gain	LTM V:1	28	5	LTC1287

Interface Circuits (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
High Speed	High Speed Dual Line Receiver	LT1015 DS	1–2	NA	LT1015
	LTC1520 in a Backplane Application	DN129	2	2	LTC1520
Level Translator	ECL to CMOS from Single 5V Supply	LTC1045 DS	14	NA	LTC1045
	ECL to CMOS/TTL Logic	LTC1045 DS	7	NA	LTC1045
	EIA562/RS232 to RS422 Level Translator	LTM IV:1	33	6	LTC1332/LTC1335
	High Voltage CMOS (V_{CC} = 15V) to TTL/CMOS (V_{CC} = 5V)	LTC1045 DS	8	NA	LTC1045
	Logic Ground Isolation	LTC1045 DS	9	NA	LTC1045
	RS232 to RS485 Level Translator with Hysteresis	LTC1485 DS	10	NA	LTC1485
	RS422 to RS562 Converter	LTC1320 DS	6	NA	LTC1320
	TTL/CMOS Logic Levels to ±5V Analog Switch Driver	LTC1045 DS	8	NA	LTC1045
		DN20	1	NA	NA
	Typical EIA562/RS232 to RS422 Level Translator	LTC1321/22/35 DS	18	22	LTC1322/LTC1335
	Typical RS232/EIA526 to RS422 Level Translator	LTC1334 DS	11	17	LTC1334
Light-to-Digital	IrDA-SIR/4PPM Data Receiver	LTM V:2	9	2	LT1319
Microcontroller (Serial)	LTC1090 to Hitachi HD63705 Microcontroller Hardware Serial Interface	AN62	17	31	LTC1090/LTC1290
	LTC1090 to Intel 8051 Microcontroller Hardware Serial Interface	AN62	17	29	LTC1090/LTC1290
	LTC1090 to Motorola MC68HC05C4 Microcontroller Hardware Serial Interface	AN62	17	30	LTC1090/LTC1290
	LTC1091 to Intel 8051 Microcontroller Hardware Serial Interface	AN62	18	32	LTC1091/LTC1291
	LTC1091 to Motorola MC68HC05C4 Microcontroller Hardware Serial Interface	AN62	18	33	LTC1091/LTC1291
	LTC1095 to Intel 8051 Microcontroller Hardware Serial Interface	AN62	18	34	LTC1095

Interface Circuits (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Microprocessor (Parallel)	LTC1095 to Motorola MC68HC05C4 Microcontroller Hardware Serial Interface	AN62	18	35	LTC1095
	LTC1296 to Microcontroller Hardware Serial Interface	AN62	17	28	LTC1296
	No-Glue Serial Interface Simplifies Connection to Microcontrollers	DN116	2	2	LTC1286
	LTC1272/LTC1273/LTC1275/LTC1276 to 8085A/Z80 Microprocessor Hardware Parallel Interface	AN62	21	43	LTC1272/LTC1273/LTC1275/ LTC1276
	LTC1272/LTC1273/LTC1275/LTC1276 to MC68000 Microprocessor Hardware Parallel Interface	AN62	21	44	LTC1272/LTC1273/LTC1275/ LTC1276
Microprocessor (Serial)	12-Bit A/D Converter Interfaced to MC68HC11	AN67	47	61	LTC1291
Mixed Mode	LTC1334 Typical Application	LTC1334 DS	1	NA	LTC1334
	RS232 and RS485 Interfaces with 5V, ±12V Supplies	LTC1321/22/ 35 DS	14	14	LTC1321/LTC1322
	RS232/RS485 Interfaces	LTC1334 DS	11	11	LTC1334
	RS485 and RS232 Interfaces	LTM IV:1	33	2–3	LTC1332, LTC1335
	Typical LTC1322 Application (RS485 and EIA562 Interfaces)	LTC1321/22/ 35 DS	1	NA	LTC1322
Multiprotocol	Multiprotocol Interface	LTC1334 DS	12	12	LTC1334
Ribbon Cable	Flat Ribbon Cable Driver/Receiver	LTC1045 DS	1	NA	LTC1045
RS232/EIA562	2 Drivers/2 Receivers (EIA562) with Shutdown and Driver Disable	LTC1385 DS	1	NA	LTC1385
	2 Drivers/2 Receivers (RS232) with Shutdown	LTC1382 DS	1	NA	LTC1382
	2 Drivers/2 Receivers (RS232) with Shutdown and Receiver Enable	LTC1384 DS	1	NA	LTC1384
	2500V Isolated 5-Driver/5-Receiver RS232 Transceiver	DN27	2	2	LT1130, LT1072
	3 Drivers/5 Receivers (EIA562) with Shutdown	LTC1327 DS	1	NA	LTC1327
	3 Drivers/5 Receivers with Shutdown	LTC1348 DS	1	NA	LTC1348

Interface Circuits (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
RS232/EIA562 (Continued)	3 Drivers/5 Receivers (RS232) with Shutdown	LTC1337 DS	1	NA	LTC1337
	3.3V Powered Flash Memory VPP Supply and RS232 Interface	DN75	2	4	LT1109A-12, LT1332
	3.3V Powered RS232 Driver/Receiver	LT1331 DS	1	NA	LT1331
	5 Drivers/3 Receivers with Shutdown	LTC1338 DS	1	NA	LTC1338
	5V Powered RS232 Driver/Receiver	DN4	2	3	LT1080
	5V Powered RS232 Driver/Receiver with Shutdown	LT1080 DS	1–8	NA	LT1080
	5V Powered RS232 Driver/Receiver with Shutdown and Small Capacitors	LT1180 DS	1–8	NA	LTC1180, LTC1181
	5V RS232 Transceiver with 3V Logic Interface	LT1330 DS	1	NA	LT1330
	Data-Rate Evaluation Circuit	LTC1348 DS	7	5	LTC1348
	Design Considerations for RS232 Interfaces	DN27	1–2	NA	NA
	Extending the Applications of 5V Powered RS232 Transceiver	DN14	1–2	3–4	LT1080
	Fast Turn-On Transceiver with Automatic Shutdown Control	DN30	1	1	LT1180
	Isolated Low Power RS232 Receiver	AN67	19	21	LTC1145/LTC1146
	Isolated RS232 Driver/Receiver	LTC1145/46 DS	8	NA	LTC1145, LT1111, LT1121-5, LT1181A
		LT1381 DS	6	NA	LT1381, LT1111, LT1121-5, LTC1145
	Isolated Low Power RS232 Receiver	LTM III:1	4	3	LTC1145/LTC1146
	Keeping Alive One Receiver While in Shutdown	LT1330 DS	1–8	NA	LT1330
		LT1237 DS	1–8	NA	LT1237
		LT1331 DS	1–8	NA	LT1331
	LT1080 Driving an LT1039	LT1039 DS	5	NA	LT1039, LT1080
	LT1137A ESD Test Circuit	LTM V:3	21	3	LT1137A

Interface Circuits (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
RS232/EIA562 (Continued)	LT1237 Typical Application (RS232 Transceiver)	LT1237 DS	1	NA	LT1237
	LT1332 Powered from an LT1109A Micropower Switching Regulator Configured for Flash Memory	LT1332 DS	1	NA	LT1332, LT1109A-12
	LT1381 Operation Using 5V and 12V Power Supplies	LT1381 DS	7	NA	LT1381
	LT1381 Typical Application (RS232 Transceiver)	LT1381 DS	1	NA	LT1381
	LT1537 Driving Remotely Powered LTC1382	LT1537 DS	6	NA	LT1537, LTC1382
	LT1537 Typical Application	LT1537 DS	1	NA	LT1537
	LTC1094 A/D Converter RS232 Interface with LT1180 Dual Driver/Receiver	AN62	20	41	LTC1094, LT1180A, LT1021-5
	LTC1290 to IBM PC Serial Port	AN62	21	42	LTC1290, LT1021-5
	LTC1383 Typical Application (RS232 Transceiver)	LTC1383 DS	1	NA	LTC1383
	LTC1386 Typical Application (EIA/TIA562 Transceiver)	LTC1386 DS	1	NA	LTC1386
	Multiple LT1332s Powered from a Single Switching Regulator	LT1332 DS	7	1	LT1332, LT1172
	New Developments in RS232 Interfaces	DN4	1–2	NA	NA
	Operating Condition ESD Test Circuit	DN80	2	3	LT1331, LT1180A
	Operation with 5V and 12V Power Supplies	LT1180 DS	7	NA	LT1180
		LT1130 DS	9	NA	LT1130
		LT1341 DS	7	NA	LT1341
		LT1342 DS	7	NA	LT1342
		LTC1337 DS	6	NA	LTC1337
	Paralleling Power Supply Generator with Common Storage Capacitors	LT1130 DS	9	NA	LT1130
		LTC1383 DS	6	NA	LTC1383
		LTC1386 DS	6	NA	LTC1386

Interface Circuits (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
RS232/EIA562 (Continued)	Quad Low Power Line Driver	LT1030 DS	1–4	1	LT1030
		LT1032 DS	1–8	NA	LT1032
	RS232 Driver/Receiver with Shutdown	LT1039 DS	1–8	NA	LT1039
	RS232 Interface Running on Both 3.3V and 5V Supplies	DN71	2	2	LT1330
	RS232 Receiver	LTC1045 DS	11	NA	LTC1045
		DN20	2	3	LTC1045
		LTC488/489 DS	8	NA	LTC488/LTC489
		LTC1485 DS	10	NA	LTC1485
	RS232 Transceiver with Charge Pump Power Supply Generator	LT1130 DS	1–12	NA	LT1130 series
	RS232 Transceivers Withstand 10kV ESD	DN64	1	1	LT1237
	Sharing a Receiver Line	LT1080 DS	6	NA	LT1080
	Sharing a Transmitter Line	LT1080 DS	6	NA	LT1080
		LT1039 DS	6	NA	LT1039
	Sharing Capacitors Between Two LT1381s	LT1381 DS	7	NA	LT1381
	Single-Supply RS232 Interface for Bipolar A/D Converters	DN29	1	1	LTC1094, LT1180, LT1021-5
	Switchable, 9-Pin DTE/DCE Data-Port Circuit	AN67	15	13	LT1137A, LT1138A
		LTM V:1	25	3a	LT1137A, LT1138A
	Transceiver	LT1039 DS	6	NA	LT1039
		LT1080 DS	6	NA	LT1080
	Typical Application Circuit for the LT1237 Under Digital Control	LTM II:3	10	10	LT1237
	Typical Application: 3 Drivers/5 Receivers with Shutdown	LTC1347 DS	1	NA	LTC1347
		LTC1348 DS	1	NA	LTC1348
		LTC1349 DS	1	NA	LTC1349
		LTC1350 DS	1	NA	LTC1350

Interface Circuits (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
RS232/EIA562 (Continued)	Typical Cable Extension for RS232/EIA562 Interface	LTC1321/22/35 DS	18	23	LTC1322/LTC1335
		LTC1334 DS	13	18	LTC1334
	Typical Connection for EIA562 Interface	LTC1321/22/35 DS	16	18	LTC1335
	Typical Connection for EIA562/RS232 Interface	LTC1321/22/35 DS	16	17	LTC1322
		LTC1334 DS	13	13	LTC1334
	Typical LT1341 Application (RS232 Interface)	LT1341 DS	1	NA	LT1341
	Typical LT1342 Application (RS232 interface)	LT1342 DS	1	NA	LT1342
	Typical Mouse Driving Application	LT1237 DS	7	NA	LT1237
		LTC1337 DS	7	NA	LTC1337
		LT1341 DS	6	NA	LT1341
		LT1342 DS	7	NA	LT1342
		LT1537 DS	7	NA	LT1537
RS485/RS422	3.3V RS485 Network	LTC1480 DS	1	NA	LTC1480
	AC Coupled Termination	AN67	21	24	NA
		LTC1485 DS	9	13	LTC1485
	DC Coupled Termination	AN67	21	23	NA
	Differential Bus Transceiver	LTC485 DS	1–12	NA	LTC485
	Differential Driver and Receiver Pair	LTC487 DS	1	NA	LTC487, LTC489
		LTC490 DS	1–8	NA	LTC490
	ESD Protection with TransZorbs®	LTC488/489 DS	8	11	LTC488/LTC489
	Forcing Zero When All Drivers Are Off	LTC488/489 DS	7	10	LTC488/LTC489
		LTC1485 DS	9	14	LTC1485

Interface Circuits (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
RS485/RS422 (Continued)	Typical Application (RS485 Transceiver)	LTC1481 DS	1	NA	LTC1481
		LTC1483 DS	1	NA	LTC1483
	LTC1485 Typical Application	LTC1485 DS	1	NA	LTC1485
	LTC1487 Typical Application	LTC1487 DS	1	NA	LTC1487
	LTC1518 Typical Application	DN129	2	3	LTC1518/LTC1519
	LTC488/LTC489 AC-Coupled Termination	LTC488/489 DS	7	9	LTC488/LTC489
	LTC488/LTC489 Typical Applications	LTC488/489 DS	1	NA	LTC486, LTC487, LTC488, LTC489
	Multiple Transceivers on One Output Bus	DN102	2	3	LTC1481/LTC1483/LTC1487
	Quad, Low Power RS485 Driver	LTC486 DS	1–8	NA	LTC486
	RS422 Cable Repeater	LTM IV:1	33	5	LTC1322/LTC1335
	RS422/RS485 Receiver Interface	LTC1345 DS	10	9	LTC1345, LTC485
	RS485 Repeater	AN67	18	19	LTC485
		LTM IV:1	30	1	LTC485
	Typical Cable Repeater for RS422 Interface	LTC1334 DS	13	16	LTC1334
		LTC1321/22/35 DS	17	21	LTC1322/LTC1335
	Typical Connection for RS422 Interface	LTC1334 DS	13	15	LTC1334
		LTC1321/22/35 DS	17	20	LTC1322/LTC1335
	Typical Connection for RS485 Interface	LTC1334 DS	12	14	LTC1334
		LTC1321/22/35 DS	16	19	LTC1322/LTC1335
	Typical RS485 Network	LTC485 DS	10	NA	NA
		DN39	1	NA	LTC485
SCSI	Active Termination for SCSI-2 Bus	LTC491 DS	1–12	NA	LTC491
		AN52	6	7	LT1117
		DN34	2	3	LT1086

Interface Circuits (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
SCSI (Continued)	Boulay Active Terminator	LTM V:3	5	2	LT1118
	LT1117 SCSI Active Termination	LTM I:1	13	1	LT1117
	LT1118 Typical Application	LTM V:3	6	3	LT1118-2.85
	SCSI Active Terminator	LT1118 DS	4	NA	LT1118-2.85
		LT1117 DS	1	NA	LT1117-2.85
	SCSI Passive Terminator	LTM V:3	5	1	NA
	SCSI Termination Power 1A Circuit Breaker with Autoreset and Ramped Turn-On	LTC1153 DS	12	NA	LTC1153
	SCSI Termination Power Circuitry	LTM II:2	9	4	LTC1153
	SCSI Termination Power Protector	LTC1154 DS	15	NA	LTC1154
		AN53	16	34	LTC1153, LT1117-2.85
	SCSI Termination Power with Short Circuit Protection	AN66	83	161	LTC1155, LT1117-2.85
		LTM I:2	7	3	LTC1155, LT1117-2.85
Termination, Active-Negation	Linear Active-Negation Voltage Source	LTM IV:2	19	3	LT1431
		AN67	16	17	LT1431
	Switching Active-Negation Termination	AN67	17	18	LT1431
		LTM IV:2	19	4	LT1431
Termination, GTL	1.2V, 5A GTL Terminator	LTM III:3	24	1	LT1087
	GTL 1.55V Terminator Provides 10A Max Current	AN67	13	11	LT1158, LT1215, LT1004-1.2
		LTM V:1	33	1	
	GTL Supply	LTM V:4	20	1	LTC1430
	GTL Termination Voltage Circuit	AN67	19	20	LT1087
V.35	Clock and Data Signals for V.35 Interface	LTC1345 DS	1	NA	LTC1345
	Complete, Single 5V V.35 Interface	LTC1345 DS	9	8	LTC1345, LT1134A
		DN94	2	4	
	Typical V.35 Implementation Using the LTC1345 and LTC1346	LTM V:3	23	2	LTC1345, LTC1346, LT1134A
		AN67	11	10	
	Y and Delta Termination Networks	LTC1345 DS	7	6	NA

Laptop Circuits					
Category	**Subject**	**Publication**	**Page Number**	**Figure Number**	**LT Part Number(s)**
Power Management	Lithium-Ion Backup System	LT1239 DS	1	NA	LT1239
	NiCd Backup System with 20mA Charge Current	LT1239 DS	12	NA	LT1239
	NiCd Backup System with 5mA Trickle Charge	LT1239 DS	12	NA	LT1239
Switching Regulator: See Regulators—Switching: Backlight					
VPP Generator	LTC1262 Typical Application	LTC1262 DS	1	NA	LTC1262

LCD Bias Supply (see Regulators—Switching, LCD Bias)

Level Detector (see Signal Conditioning, Level)

Level Shift (see Comparators)

LVDT (see Signal Conditioning, Distance)

Memory

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Discussion	A Primer on Flash Memory	AN31	12	NA	NA
	Preventing Memory Destruction	AN31	14	NA	NA
EEPROM	EEPROM Pulse Generator	LT1013 DS	12	NA	LT1013, LT1004-1.2
	EEPROM VPP Pulse Generator	AN31	5	9	LT1072, LT1006, LT1010, LT1004-1.2
EPROMs	VPP Generator for EPROMs—No Trim Required	LT1004 DS	7	NA	LT1004-1.2, LM301A
Flash	12.7V to 17V In, 120mA VPP Generator for Use with Flyback Converter or Overwindings	DN97	2	NA	LT1121
	12V, 60mA Flash-Memory Programming Supply	LT1309 DS	1	NA	LT1309
		LT1106 DS	1	NA	LT1106
	2V to 12V/120mA Converter	LT1302 DS	14	NA	LT1302
	3.3V or 5V In, 60mA VPP Generator for PCMCIA with Bank Switching for Up to 4 Memory Chips	DN97	1	NA	LT1106
	3.3V Powered Flash-Memory VPP Supply and RS232 Interface	DN75	2	4	LT1109A-12, LT1332
	3.3V/5V In, 120mA/240mA VPP Generator	DN97	2	NA	LT1172
	84%–88% Efficient, 5V/3.3V In 60mA/120mA VPP Generator	DN97	2	NA	LT1301
	All Surface Mount Flash-Memory VPP Generator	LT1109 DS	1	NA	LT1109-12
		LT1109A DS	1	NA	LT1109A
	All Surface Mount, Minimum Component Count, 3.3V/5V In, 60mA/120mA VPP Generator	DN97	1	NA	LT1109-12
	Alternative Scheme Allows 12V from VPP1/VPP2 to Provide Power When LT1106 is in Shutdown	LT1106 DS	8	NA	LT1106
	Basic Flash-Memory VPP Programming Voltage Supply	AN31	1	1	LT1072
	Boost-Mode Switching Regulator for Flash-Memory VPP Programming	LTM II:3	17	1	LT1109A-12

Memory (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Flash (Continued)	Boost Mode Switching Regulator with Low R_{ON} Pass Transistor for Flash-Memory Programming	AN66	65	132	LT1109A-12
	Flash-Memory Programmer	AN61	22	29	LT1109-12
	High Power, High Repetition Rate VPP Pulse Generator	AN31	3	7	LT1072, LT1006, LT1004-1.2
	High Repetition Rate VPP Programming Supply	AN31	2	4	LT1072, LT1006, LT1010, LT1004-1.2
	Inductorless 5V In, 30mA VPP Generator	DN97	1	NA	LTC1262
	Inductorless Flash-Memory VPP Generator	LTM IV:2	18	1	LTC1262
	Inductorless VPP Generator	AN66	64	130	LTC1262
	Inductorless, Charge-Pump 5V In, 60mA VPP Generator	DN97	1	NA	LTC1263
RAM	Typical Nonvolatile CMOS RAM Application	LTC694/5-3.3 DS	11	6	LTC695-3.3
	Write Protect for Additional RAM	LTC694/5-3.3 DS	15	NA	LTC695-3.3
	Write Protect for RAM	LTC694/5-3.3 DS	11	7	LTC694-3.3
Save	Memory Save on Power Down	AN31	8	16	LT1020, LT1086-5

Methane Detector (see Signal Conditioning)

Micropower

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
A/D	Micropower A/D (10-Bit, 100µs)	AN23	9	11	LT1017
	Micropower A/D (12-Bits, 300µs)	AN23	7	9	LTC1043, LT1018
Comparator	Refrigerator Alarm	LT1017 DS	1	NA	LT1017

Micropower (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
DC/DC	Low Quiescent Current Flyback Regulator (150µA, 6V–12V)	AN29	9	12	LT1070, LT1017, LT1004-1.2
		DN11	2	2	LT1070, LT1017, LT1004-1.2
Discussion	Parasitic Effects of Test Equipment on Micropower Circuits	AN23	23	NA	NA
	Sampling Techniques and Components for Micropower Circuits	AN23	21	NA	NA
	Some Guidelines for Micropower Design	AN23	18–20	NA	NA
Instrumentation Amplifier	Micropower, Single-Supply Instrumentation Amplifier	LTC1047 DS	1	NA	LTC1047, LTC1043
	Precision, Micropower, Single-Supply Instrumentation Amplifier	LT1101 DS	1–12	NA	LT1101
Op Amp	Low Power, Chopper Stabilized Op Amp with Internal Capacitors (200µA)	LTC1049 DS	1–8	NA	LTC1049
Sample and Hold	Micropower Sample and Hold	AN23	10	14	LT1006
		LT1006 DS	1	NA	LT1006
Strain Gauge	Sampled Strain-Gauge Bridge Signal Conditioner	AN23	3	3	LT1021, LT1006
	Strobed Power Bridge Signal Conditioner	AN23	4	5	LT1054, LT1013
Temperature Sensor	Freezer Alarm	AN23	7	8	LTC1042
	Micropower Cold Junction Compensation for Thermocouples	LT1004 DS	1	NA	LT1004-1.2
	Micropower, Battery Operated, Remote Temperature Sensor	LT1101 DS	11	NA	LT1101, LM134-3, LT1004-1.2
	Platinum RTD Signal Conditioner with Curvature Correction (2°C–400°C)	AN23	1	1	LT1006/LT1078, LM334
		LT1006 DS	10	1	LT1006, LM334
	Thermistor Based current Loop Signal Conditioner (0°C–100°C)	AN23	5	6	LTC1040, LM134, LT1034-1.2
	Thermocouple Signal Conditioner with Cold Junction Compensation (0°C–60°C)	LT1006 DS	11	NA	LT1006, LT1034
		AN23	2	2	
	Wall-Type Thermostat	AN23	6	7	LTC1041
V/F	90µA Supply Current V/F	AN45	15	21	LT1017, LT1178, LT1004-2.5

Micropower (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
V/F (Continued)	Micropower V/F Converter (0V–5V to 100Hz–1MHz)	DN38	1	1	LTC201A
		LTC201 DS	1	NA	LTC202, LT1178
	Micropower V/F Converter (10kHz)	AN23	11	16	LT1017, LT1004-1.2
	Micropower V/F Converter (1MHz)	AN23	13	20	LT1006, LT1004-1.2, LT1004-2.5
		LT1006 DS	10	NA	
	Ultralow Power 50°F to 100°F Thermostat	LTC1041 DS	1	NA	LTC1041
Voltage Reference	Low Input Voltage Reference Driver	LM134 DS	9	NA	LM334, LT1009
	Low Power V/F Converter	LT1018 DS	7	NA	LT1018, LT1034-1.2
	Micropower 5V Reference	LM134 DS	10	NA	LM334, LT1004-1.2
		LT1004 DS	7	NA	
	Self-Buffered Micropower Reference	LT1178 DS	1	NA	LT1178, LT1004-1.2
		DN23	1	1	LT1178, LT1034-1.2
Voltage Regulator	Buck Switching Regulator (5.8V–10V to 5V)	AN23	15	22	LT1017, LT1004-1.2
	Micropower Preregulated Linear Regulator	AN32	8	15	LT1020
	Micropower Regulator with Comparator and Shutdown	LT1120 DS	1–12	NA	LT1120
	Post Regulated Switching Regulator (6V–10V to 5V)	AN23	16	25	LT1020

Models

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Macromodel	LT1013 Op Amp Spice Macromodel	DN12	1	1	NA
	LT1056 Macromodel	DN43	1–2	1	NA
	Questions and Answers on the Spice Macromodel Library	AN41	1–18	NA	NA

Models (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Macromodel (Continued)	Spice Op Amp Macromodel for the LT1012	DN28	1–2	NA	NA
	Using the LTC Op Amp Macromodels	AN48	1–28	NA	NA

Motor Control

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Driver	10A Locked, Antiphase, Full-Bridge Motor Drive	AN66	91	172a	LT1158
		LTM II:1	5	4a	LT1158
	DC Motor Driver with Overcurrent and Overtemperature Protection	AN66	87	168	LTC1153
		LTM II:2	9	5	LTC1153
	DC Motor Driver with Stall-Current Circuit Breaking	LTC1153 DS	14	NA	LTC1153
	Driving a Supply-Referenced Motor	LT1160 DS	11	3	LT1160
	Full-Bridge Motor Control with the LT1162	LTM V:4	16	6	LT1162
	H-Bridge Motor Driver with Ground-Referenced Current Sensing	LTM III:1	19	1	LT1158
		AN66	90	171	LT1158
	LT1160 Typical Application	LT1160 DS	1	NA	LT1160
	LT1161-Based H-Bridge Motor Driver	LTM V:1	31	1	LT1161
		AN66	96	176	LT1161
Speed	10A Full Bridge Motor Control	LT1158 DS	19	17	LT1158
	A Simple Motor Tachometer Servo Loop	AN25	11	17	LT1070
	High Efficiency, 6-Cell NiCd Protected Motor Drive	LT1158 DS	18	15	LT1158
	High Efficiency Motor-Speed Controller	LT1011 DS	11	NA	LT1011
	Motor-Speed Controller	AN1	7	13	LT1005
		AN4	6	13	LT1010, LM301A
		LTC1041 DS	7	NA	LTC1041, LT1009

Motor Control (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Speed (Continued)	Motor-Speed Controller Needs No Tachometer	LF198 DS	14	NA	LF398, LT3524
	Motor-Speed Controller, No Tachometer Required	LT1013 DS	12	NA	LT1013
		AN11	8	8	LT1013
	Piezoelectric Fan Servo	AN4	7	14	LT1010, LM301A
	Potentiometer-Adjusted Open Loop Motor-Speed Control	LT1158 DS	17	14	LT1158
	Proportional Motor-Speed Controller	LT1035 DS	9	NA	LT1035
		LT1005 DS	9	NA	LT1005
	Tachless Motor-Speed Regulator	AN66	94	175	LT1170, LT1006
		LTM IV:3	29	2	LT1170, LT1006
Stepper Motor Driver	4-Phase Stepper Motor Driver with Overcurrent Protection	LTC1255 DS	15	NA	LTC1255
	4-Phase Stepper Motor Driver with Short Circuit Protection	LTC1156 DS	7	NA	LTC1156
	Power MOSFET Driver, Low Power Consumption, Stepper Motor Driver	LTC1045 DS	15	NA	LTC1045

Multiplexers

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Analog	Daisy Chaining Five LTC1390s	LTC1390 DS	7	NA	LTC1390, LTC1286
	Daisy Chaining Five LTC1391s	LTC1391 DS	7	NA	LTC1391, LTC1286
	Daisy Chaining Two LTC1390s for Expansion	LTC1390 DS	6	5	LTC1390, LTC1286
	Daisy Chaining Two LTC1391s for Expansion	LTC1391 DS	5	5	LTC1391, LTC1286
	Interfacing the LTC1390 with the LT1257 for Demultiplex Operation	LTC1390 DS	8	NA	LTC1390, LTC1257

Multiplexers (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Analog (Continued)	Interfacing the LTC1391 with the LTC1451 for Demultiplex Operation	LTC1391 DS	6	NA	LTC1391, LTC1451
	LTC1390 Typical Application	LTC1390 DS	1	NA	LTC1390, LTC1096
	LTC1391 Typical Application	LTC1391 DS	1	NA	LTC1391, LTC1285
Video	16-to-1 Multiplexer	LT1203/05 DS	11	5	LT1205, LT1252
	4 × 4 Crosspoint	LT1203/05 DS	13	6	LT1205, LT1254
	4-Input Differential Receiver	LT1204 DS	17	NA	LT1204
	4-Input Twisted-Pair Driver/Receiver	LT1204 DS	18	NA	LT1204, LT1227, LT1193
	Fast Differential Multiplexer	AN57	10	16	LT1204
	Fast RGB MUX	AN67	66	97	LT1203, LT1205, LT1260
	High Speed RGB MUX	LT1203/05 DS	1	NA	LT1203, LT1205
	Picture-in-Picture Test Setup	AN67	67	99	LT1204
	RGB MUX	LT1203/05 DS	8	1	LT1203, LT1205, LT1260
	Typical Application—4-Input Video Multiplexer	LT1204 DS	1	NA	LT1204

Noise

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
	See Also Amplifiers, Noise				
Discussion	Minimizing	AN9	3	NA	LTC1052
	Noise Calculation in Op Amps	DN15	1	NA	NA
	Symmetrical White Gaussian Noise	AN67	51	NA	NA
	Voltage Noise vs Current Noise	LT1028 DS	8	NA	LT1028/LT1128

Noise (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Generator	Broadband Random Noise Generator	AN61	24	33	LT1226, LT1228, LT1006, LT1004
		LTM III:2	20	1	LT1226, LT1228, LT1006
		AN67	49	63	LT1226, LT1228, LT1006
	Broadband Random Noise Source with Zener Diode Noise Source	AN61	26	37	LT1226, LT1228, LT1013, LT1004
	Pseudorandom Code Generator	LTM III:2	22	5	LT1190, LT1116, LT1220
		AN67	52	67	LT1190, LT1116, LT1220
		AN56	7	12	LT1190, LT1116, LT1220
	Random Noise Generator with Selectable Bandwidth and RMS Voltage Regulation	DN70	1	1	LT1013, LT1226, LT1228
Meter	Noise Meter Buffer/Driver Section	AN67	42	54	LT1206
	Noise Meter Gain Stage, LT1206 Buffer/ Driver Section, LT1088 RMS Detector Section	LTM V:3	28	1–3	LT1226, LT1192, LT1014, LT1088, LT1206
	RMS Detector Section	AN67	42	55	LT1014, LT1088
	RMS Noise Meter Gain Stage	AN67	41	53	LT1226, LT1192

Op Amps (see Amplifiers)

Oscillators

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Crystal	1.5V Powered Temperature-Compensated Crystal Oscillator	LT1073 DS	19	NA	LT1073, LT1017
	1.5V Temperature-Compensated Crystal Oscillator (3.5MHz)	AN15	6	9	LM10
	10MHz Quartz-Stabilized Sine Wave Oscillator	AN47	49	111	LT1191

Oscillators (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Crystal (Continued)	20MHz Quartz-Stabilized Sine Wave Oscillator with Electronic AGC	AN47	50	112	LT1191, LT1006
	3.58MHz Oscillator	LT1227 DS	11	NA	LT1227
	Crystal Oscillator (10MHz–25MHz)	AN12	3	4	LT1016
		LT1016 DS	1	NA	LT1016
		AN31	11	24B	LT1016
	Crystal Stabilized Relaxation Oscillator	AN12	2	2	LT1011
		LT1011 DS	10	NA	LT1011
	Gate Oscillators	AN12	2	1	NA
	Low Distortion, Crystal Stabilized Oscillator	LT1057 DS	8	NA	LT1057
	Low Frequency Crystal Oscillator Clock	AN31	11	25	LT1018
	Oscillator (1MHz–10MHz)	LT1016 DS	14	NA	LT1016
		AN12	3	4A	LT1016
		AN31	11	24A	LT1016
	Ovenized Oscillator	AN12	3	5	LT1001, LT1005
	Quartz-Stabilized, Low Distortion	AN45	12	18	LT1122, LT1006, LT1010,
	Temperature-Compensated Crystal Oscillator	LT1013 DS	18	NA	LT1013, LT1009
	Temperature-Compensated Crystal Oscillator, TXCO	AN12	4	6	LT1005, LT1055, LT319A
		AN3	15	21	LT1009, LTC1043, LT1056
	Temperature-Compensated, 1.5V Powered	AN45	14	20	LT1073, LT1017
	Voltage-Controlled Crystal Oscillator (VCXO)	AN12	5	8	NA
Discussion	Quartz Crystal	AN12	8	NA	NA
	Wien Bridge	AN43	43	C2	LT1037
Half Sine Wave	A Half Sine Reference Generator	AN35	29	E3	LT1016, LT1086-5
Pulsed	1.5V Temperature-Compensated Crystal Oscillator	AN15	6	9	LM10
	Bridge Oscillator	AN43	27	32	LT1056

Oscillators (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Pulsed (Continued)	Crystal Oscillator (10MHz–25MHz)	LT1016 DS	1	NA	LT1016
		AN12	3	4B	LT1016
	Crystal Stabilized Relaxation Oscillator	AN12	2	2	LT1011
		LT1011 DS	10	NA	LT1011
		LT311A DS	6	NA	LT311A
	Gate Oscillators	AN12	2	1	NA
	Low Frequency Square Wave Generator	LM101 DS	5	NA	LM101A
	Oscillator (1MHz–10MHz)	AN12	3	4A	LT1016
		LT1006 DS	10	NA	LT1016
	Ovenized Oscillator	AN12	3	5	LT1001, LT1005
	Phase Shift Oscillator	LT1032 DS	7	NA	LT1032
	Reset Stabilized Oscillator	AN12	6	13	LT1011, LT1055
	Single-Supply Crystal Oscillator 10MHz–15MHz	LT1116 DS	6	2	LT1116
	Stable RC Oscillator	LT1016 DS	14	NA	LT1016
		AN12	7	15	LT1011
		LT1011 DS	12	NA	LT1011
	Temperature-Compensated Crystal Oscillator	LT1013 DS	18	NA	LT1013, LT1009
	Temperature-Compensated Crystal Oscillator, TXCO	AN12	4	6	LT319A, LT1005, LT1055
		AN3	15	21	LTC1043, LT1009
Sine Wave	10MHz Quartz-Stabilized Sine Wave Oscillator	AN47	49	111	LT1191
	20MHz Quartz-Stabilized Sine Wave Oscillator—Electronic AGC	AN47	50	112	LT1191, LT1006
	Bridge-Based Crystal Oscillator	AN43	27	33	LT1056
	Common Mode Suppression for Quartz Oscillator Lowers Distortion	AN43	28	37	LT1057
	Crystal Oscillator with Lamp Added for Gain Stabilization	AN43	28	35	LT1056
	Low Distortion Sine Wave	AN5	8	12	LT1037

Oscillators (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Sine Wave (Continued)	Low Distortion, Crystal-Stabilized Oscillator	LT1057 DS	8	NA	LT1057
	Multirange Wien Bridge Based Oscillator	AN43	29	40	LT1037
	Quartz-Stabilized Oscillator with 9ppm Distortion	LT1122 DS	8	NA	LT1122, LT1010, LT1004
	Sine Wave Output VCO (1Hz–100kHz)	AN14	10	14	LT1056, LT1011
	Super Low Distortion Variable Sine Wave Oscillator	LT1028 DS	14	NA	LT1028, LT1055, LT1004-2.5
	Ultralow THD Oscillator (5ppm Distortion)	LT1115 DS	12	6	LT1115, LT1006, LT1010, LT1022, LT1004
	Ultrapure Sine Wave Generator	LT1022 DS	7	NA	LT1022
		LT1037 DS	1	NA	LT1037
	Varactor-Tuned 1MHz–10MHz Wien Bridge Oscillator	AN47	51	114	LT1006, LT1191, LT1172
	Voltage-Controlled Sine Wave Oscillator	AN12	5	8	NA
	Voltage-Controlled Sine Wave Oscillator (1Hz–1MHz)	AN13	13	21	LT318A, LT1009, LT1012, LT1016
	Wein Bridge Sine Wave Oscillator	LM101 DS	1	NA	LM107
	Wien Bridge Oscillator with Photocell Stabilization	AN43	32	47	LT1006, LT1009, LT1115, LT1010, LT1022
	Wien Bridge Sine Wave Oscillator	LT1225 DS	7	NA	LT1225
		AN43	29	39	LT1037
	Wien Bridge with 3ppm Distortion	AN43	33	48	LT1006, LT1009, LT1010, LT1022, LT1115
	Wien Bridge with FET Stabilization	AN43	31	45	LT1115, LT1055, LT1004-1.2
		AN43	30	43	LT1115, LT1055, LT1004-1.2
Synchronized	High Noise Immunity Line Synchronization Circuit	AN31	12	26	LT1011
	Synchronized Oscillator	AN12	6	11	LT1055
V/F: See Converters, V/F					

Oscillators (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
VCO	1Hz–1MHz Sine Wave Output	AN47	53	118	LT1016, LT1097, LT1122, LT1150
	Sine Wave Output Voltage to Frequency (1Hz–100kHz)	AN14	10	14	LT1056, LT1011
		LT1055 DS	11	NA	LT1056, LT1011
	Voltage-Controlled Crystal Oscillator	LT319A DS	5	NA	LT319A
	Voltage-Controlled Crystal Oscillator (VCXO)	AN12	5	8	NA
	Voltage-Controlled Sine Wave Oscillator (1Hz–1MHz)	AN13	13	21	LT318A, LT1012, LT1016, LT1056

Oscilloscope

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Discussion	About Oscilloscopes	AN47	20	NA	NA
	Considerations for High Speed Work	AN13	8	NA	NA
	Evaluating Oscilloscope Overload Preformance	AN10	6	NA	NA
	Measuring Equipment Response	AN13	30	NA	NA
	Probes and Oscilloscopes	AN13	27	NA	NA

Ott Process

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Thermal	High Thermal Resistance Die Attach	AN22	4	NA	LT1088

PC Card (Formerly PCMCIA)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Card Slot Power Management	Dual Slot, Protected PCMCIA Power Management System	LTC1472 DS	12	NA	LTC1472, LT1301
	Dual, Protected PCMCIA Power Management System Powered by System 12V Supply	LTC1472 DS	15	NA	LTC1472
	Single Slot, Protected PCMCIA Power Management System Powered from 3.3V or 5V	LTC1472 DS	13	NA	LTC1472, LT1301
	Single, Protected PCMCIA Power Management System Using the LT1121 Powered from Auxiliary Winding	LTC1472 DS	14	NA	LTC1472, LT1121
Driver/ Regulator	Deriving 14V Power from a 3.3V Auxiliary Winding	AN60	7	8	LTC1148-3.3/LTC1142, LT1312
	Deriving 14V Power from a 3.3V Winding	LTM IV:3	4	3	LT1312, LTC1148-3.3, LTC1142
	Deriving 14V Power from a 5V Auxiliary Winding	AN60	5	6	LTC1148-5/LTC1142, LT1312
	Local 12V to 13.75V Boost Regulator for Use with the LT1312	AN60	7	10	LT1111, LT1312
	Local 5V to 13.75V Boost Regulator for Use with the LT1312	AN60	7	9	LT1172, LT1312
	LTC1314 and LT1301 PCMCIA Card Slot Configuration	AN60	9	12	LTC1314, LT1301
	LTC1314 PCMCIA Card Slot Configuration with LT1121 Linear Regulator	AN60	11	15	LT1121, LTC1314
	Typical Dual PCMCIA Socket Application Using the LTC1315 and the LT1301	AN60	11	16	LTC1315, LT1301
	Typical Dual PCMCIA Socket Application with the LTC1471 and LT1313	AN60	8	11	LTC1148-5/LTC1142, LT1313, LTC1471
	Typical Single-Socket PCMCIA Power-Management System	LTM IV:3	3	1	LT1312, LTC1165
V_{CC} and VPP Switching	Dual Slot PCMCIA Controller with SafeSlot™ Current-Limit Protection	LTC1470 DS	7	NA	LTC1470, LT1313
	Dual-Slot PCMCIA Controller	LTC1471 DS	7	NA	LTC1471, LTC1313

PC Card (Formerly PCMCIA) (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
V_{CC} and VPP Switching, Protected	PCMCIA V_{CC} and VPP Switch Matrix with 3.3V/5V Boost Regulator	LTM V:1	22	1	LTC1472, LT1301
	Single-Slot PCMCIA Controller with SafeSlot Current-Limit Protection	LTC1470 DS	10	NA	LTC1470, LT1312
	Typical LTC1472 Application with LT1301 3.3V/5V Boost Regulator	AN60	3	2	LTC1472, LT1301
	Typical LTC1472 PCMCIA V_{CC} and VPP Switch Matrix Application	DN93	1	1	LTC1472, LT1301
	Direct Interface to "365" Type PCMCIA Controller	LTC1472 DS	10	2	LTC1472
	Direct Interface to Industry Standard PCMCIA Controller and LT1301 Step-Up Switching Regulator	LTC1472 DS	9	1	LTC1472, LT1301
	Direct Interface with CL-PD6720 PCMCIA Controller	LTC1470 DS	6	1	LTC1470
	Protected PCMCIA V_{CC} and VPP Card Driver	LTC1472 DS	1	NA	LTC1472
V_{CC} Controller	Direct Interface to "365" Type PCMCIA Controller	LTC1470 DS	7	2	LTC1470
V_{CC} Switch/ Switch Matrix	3.3V PCMCIA Card Power Switching	LTM III:1	22	1	LTC1157, LT1017
	Direct Interface with CL-PD6710 PCMCIA Controller	LTC1471 DS	6	1	LTC1471
	Dual Slot 3.3V/5V PCMCIA Controller with SafeSlot Current Limit	LTC1471 DS	10	NA	LTC1471
	PCMCIA Card 3.3V/5V V_{CC} Switch	LTC1163/65 DS	6	NA	LTC1165
	PCMCIA Card 5V/3.3V Switch	DN76	1	1	LTC1165
	PCMCIA Card Power Switching	AN66	81	158	LTC1157, LT1017
	PCMCIA Dual-Slot 3.3V/5V V_{CC} Switch Matrix	LTC1471 DS	1	NA	LTC1471
	PCMCIA Single-Slot 5V/3.3V V_{CC} Switch	LTC1470 DS	10	NA	LTC1470, LT1312
	Typical LTC1470 Application with the LT1312 VPP Driver/Regulator	AN60	5	5	LTC1470, LT1312

PC Card (Formerly PCMCIA) (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
V_{CC} Switch/ Switch Matrix, Protected	PCMCIA V_{CC} Switching Matrix with LT1312 VPP Drive/Regulator	LTM V:1	23	2	LTC1470, LT1312
VPP Switch/ Regulator	0V, 3.3V, 5V, and 12V Programmable VPP Generator for PCMCIA	LTM IV:1	19	1	LT1107
	12V, 60mA Flash-Memory Programming Supply	LT1106 DS	1	NA	LT1106
	24V-Input PCMCIA VPP Switch/Regulator	LTM IV:2	23	1–2	LT1121A
	All Surface Mount, Programmable 0V, 3.3V, 5V and 12V VPP Generator for PCMCIA	AN66	92	173	LT1107
	Alternative Scheme Allows 12V from VPP1/ VPP2 to Provide Power when LT1106 is in Shutdown	LT1106 DS	8	NA	LT1106
	Current-Limited Linear Regulator VPP Power Management Circuit	DN76	2	3	LT1121
	Deriving 14V Power (for the LT1312) from the Auxiliary Winding on the LTC1142HV Regulator	LT1312 DS	7	1	LT1312, LTC1142HV
	Deriving Auxiliary 14V Power (for the LT1312) from an LTC1142 3.3V Regulator	LT1312 DS	8	3	LT1312, LTC1142
	Direct Interface with "365" Type PCMCIA Controller	LTC1470 DS	7	2	LTC1470
	Dual-Slot PCMCIA Driver/Regulator Powered from Auxiliary Winding on 5V Inductor of LTC1142 regulator	LT1313 DS	10	NA	LT1313, LTC1148
	Dual-Slot PCMCIA Interface to "365 Type" Controller	LT1313 DS	9	NA	LT1313, LTC1157
	Dual-Slot PCMCIA Interface to CL-PD6720	LT1313 DS	8	NA	LT1313, LTC1165
	Local 12V to 15V Boost Regulator for Line-Operated Applications	LT1312 DS	9	5	LT1312, LT1111CS8
	Local 5V to 15V Boost Regulator for Line-Operated Applications	LT1312 DS	9	4	LT1312, LT1172
	PCMCIA Card Socket VPP Switch/Regulator	LTC1163/65 DS	7	NA	LTC1163, LT1109
	PCMCIA Switch Matrix with Boost Regulator	LTM IV:3	5	4	LTC1314, LT1301

PC Card (Formerly PCMCIA) (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
VPP Switch/ Regulator (Continued)	PCMCIA Switch Matrix with Linear Regulator	LTM IV:3	5	5	LTC1314, LT1121
	Single Slot Interface to "365 Type" Controller	LT1312 DS	11	NA	LT1312, LTC1157CS8
	Single Slot Interface to CL-PD6710	LT1312 DS	11	NA	LT1312
	Step-Up Regulator VPP Power Management Circuit	DN76	2	2	LTC1157, LT1107
	Typical PCMCIA Dual-Slot VPP Driver	LT1313 DS	1	NA	LT1313
	Typical PCMCIA Single-Slot VPP Driver	LT1312 DS	1	NA	LT1312

Peak Detectors

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Fast	Closed-Loop Peak Detector	DN61	1	1	LT1190
		LTM II:3	3	3	LT1190
		AN67	75	118	LT1190
	Fast Pulse Detector	DN61	2	5	LT1190
		LT1195 DS	1	NA	LT1195
	Open-Loop, High Speed Peak Detector	DN61	1	3	LT1190
		AN67	76	120	LT1190
		LTM II:3	4	5	LT1190
Negative	Negative Peak Detector	LT1011 DS	12	NA	LT1011, LT1008
		LT311A DS	7	NA	LT311A, LT1008
Positive	Positive Peak Detector	LT1011 DS	12	NA	LT1011, LT1008
		LT311A DS	7	NA	LT311A, LT1008

Phase-Locked Loops

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Discussion	Unique Applications for the LTC1062 Lowpass Filter	AN24	1	1	LTC1062
Filter—Switched Capacitor	DC Accurate Filter Eases PLL Design	DN7	1	1–2	LTC1062

Photodiode (see Signal Conditioning, Photodiode)

Platinum RTD (see Signal Conditioning—Temperature, Platinum RTD)

Power Actuators (see Drivers)

Power Management

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Battery Monitor	0A to 2A Battery-Current Monitor Draws Only 70µA	AN62	8	10	LT1004, LTC1096, LT1178
	LTC1297 Data-Acquisition System Battery-Current Monitor	AN62	10	11	LTC1297, LT1121, LTC1047, LT1004
	Micropower Battery-Voltage Monitor	AN62	8	9	LTC1096
Notebook Computer	Four-Cell NiCd Notebook Power-Management System	LTM II:1	13	1	LTC1156, LT1431
	Laptop Computer Power Bus Switching	AN66	82	160	LTC1155
	Monitoring Regulated Power Supply with the Power Supply Comparator	LTC694/5-3.3 DS	11	8	LTC694-3.3/LTC695-3.3, LT1129-3.3
	Using the LTC695-3.3 BATT ON to Drive External PNP Transistor	LTC694/5-3.3 DS	9	2	LTC695-3.3
Supply Switching	0.85A Protected Switch	LTC1477/78 DS	7	NA	LTC1477
	1.5A Protected Switch	LTC1477/78 DS	6	NA	LTC1477

Power Management (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Supply Switching (Continued)	2-Cell to 3.3V, 5V and 12V High-Side Switch/ Converter with 0.01µA Standby Current	LTC1163/65 DS	7	NA	LTC1163/LTC1165, LT1109, LT1173
	2-Cell, Triple High-Side Switch	LTC1163/65 DS	1	NA	LTC1163/LTC1165
	2A Protected Switch	LTC1477/78 DS	6	NA	LTC1477
	2A Protected Switch Driving a Capacitive Load	LTC1477/78 DS	7	NA	LTC1477
	3.3V/5V Supply Switching Circuit	LTM V:3	25	1	LTC1470, LT1011
	3.3V/5V Switchover Circuit	AN66	84	163	LTC1470, LT1011
	5V to 3.3V Selector Switch with Slope Control and 0.01µA Standby Current	LTC1477/78 DS	7	NA	LTC1478
	Adding Short-Circuit Protection to an LT1301 Step-Up Switching Regulator	LTC1477/78 DS	7	NA	LTC1477, LT1301
	Battery Backup Monitor with Optional Test Load	LTC694/5-3.3 DS	12	10	LTC695-3.3
	Hot Swap Circuit	AN66	88	169	LTC1477, LTC699
	Isolated High-Side Switch	LTC1177 DS	1	NA	LTC1177
	Isolated High-Side Switch with Foldback Current Limit	LTC1177 DS	5	NA	LTC1177
	Logic Controlled Battery Switch with Reverse Battery Protection, Ramped Turn-On and 10µA Standby Current	LTC1153 DS	12	NA	LTC1153
	LTC1157 Used to Switch Two 3.3V Loads	AN66	82	159	LTC1157
	LTC695-3.3 Typical Application	LTC694/5-3.3 DS	1	NA	LTC695-3.3, LT1129-3.3
	Using LTC695-3.3 BATT ON to Drive External PNP Transistor	LTC694/5-3.3 DS	9	2	LTC695-3.3

Power Supplies (see Regulators—Linear; Regulators, Switching)

Power Supply Supervisory Circuits (see Digital Help Circuits)

Preamplifiers (see Amplifiers)

Pressure Measurement (see Signal Conditioning, Pressure)

Probes

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Current	Techniques and Equipment for Current Measurement	AN35	24	NA	NA
Discussion	ABCs of Probes	AN47	69	NA	NA
	Probes and Probing Techniques	AN47	16	NA	NA
Fast	Ultrafast, High Impedance	AN47	96	E1	NA
High Impedance	High Impedance Buffer	AN23	24	C2	LT1010, LT1022
Oscilloscope	About Probes and Oscilloscopes	AN13	27	NA	NA

Programming

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
C Language	A "C" Cruise Through Data Acquisition	AN34	1–9	NA	NA

Pulse Detector

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Fast	Fast Pulse Detector	LTM II:3	4	7	LT1190

Pulse Generator

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Fast Rise	Avalanche Pulse Generator	AN47	93	D1	LT1073
		AN45	18	27	LT1073
General	Triggered 250ps Rise-Time Pulse Generator	AN61	21	26	LT1182
	Current Calibrator for Probe Trimming and Accuracy	DN101	2	3	LT1010, LT1097, LT1122, LT1029

Pulse Width Modulator

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
	PWM with External Clock Synchronization	LT1246/47 DS	10	NA	LT1246/LT1247
	PWM with Soft Start	LT1246/47 DS	10	NA	LT1246/LT1247
	PWM with Adjustable Clamp Level and Soft Start	LT1246/47 DS	10	NA	LT1246/LT1247
	PWM with Slope Compensation at I_{SENSE} Pin	LT1246/47 DS	11	NA	LT1246/LT1247
	PWM with Slope Compensation at the Error Amp	LT1246/47 DS	11	NA	LT1246/LT1247

Radio Station

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
AM	Complete AM Radio Station	AN47	52	116	LT1007, LT1190, LT1194
	AM Modulator with DC Output Nulling Circuit	LT1251/56 DS	15	NA	LT1256, LT1077

Reference—AC

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Half Sine Wave	Half Sine Reference Generator	AN35	29	E3	LT1016, LT1086-5

Reference— Current

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Sink	Precision Current Sink	LT1001 DS	8	NA	LT1001
Source	Precision Current Source	LT1001 DS	8	NA	LT1001
	Precision Current Source (1µA)	LT1019 DS	7	NA	LT1019-2.5, LT1012

Reference—Voltage

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
2-Terminal	1.235V Micropower Reference	LT1004 DS	6	NA	LT1004
		AN42	10	44	LT1004
	1.24V Out Micropower, Current Boosted Reference (100mA)	AN42	11	52	LT1077
	±1.25V Reference	AN42	10	43	LT1009
	1.2V Out Micropower Reference with Wide Input Voltage Range	AN42	11	46	LT1004-1.2, LM334
	10V Buffered Reference Using a Single-Supply	LM129 DS	3	NA	LM329, LT1001
		OP07 DS	1	NA	LM129A, OP07
	2.5V Out Micropower Reference with Wide Input Voltage Range	AN42	11	48	LT1004-2.5
	2.5V Reference	AN42	11	47	LT1004-2.5
	6.9V Reference	LM129 DS	3	NA	LM329

Reference—Voltage (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
2-Terminal (Continued)	Low Noise Reference	LT1004 DS	6	NA	LT1004-1.2
3-Terminal	2.5V Reference, ±5% Trim Range	AN42	5	4	LT1009
		LT1009 DS	1	NA	LT1009
		LM136 DS	1	NA	LM336-2.5
	Low Noise 2.5V Buffered Reference	LT1009 DS	4	NA	LT1009
		LM136 DS	4	NA	LM336-2.5
	Split ±2.5V References	LT1029 DS	4	NA	LT1029, LT1001
	Switchable ±1.25V Bipolar Reference	LM136 DS	4	NA	LM336-2.5
		LT1009 DS	4	NA	LT1009
	Trimming Output to 5.120V	AN42	6	9	LT1029
		LT1029 DS	4	NA	LT1029
	Wide Supply Range	LM136 DS	4	NA	LM334, LM336-2.5
	Wide Supply Range, Adjustable Reference	LT1009 DS	4	NA	LT1009, LM334
		AN42	11	49	LT1009, LM334
Current Boost	1.24V Out, Micropower, Current Boosted Reference (100mA)	AN42	11	52	LT1077, LT1004-1.2
	Boosted Output Current 10V Reference	LT1236 DS	9	NA	LT1236
	Boosted Output Current with No Current Limit	AN42	12	54	LT1031
		LT1021 DS	11	NA	LT1021
		LT1031 DS	8	NA	LT1031
	Handling Higher Load Currents	LT1027 DS	6	2	LT1027
	Output Current Boost with Current Limit	LT1031 DS	8	NA	LT1031
		LT1019 DS	7	NA	LT1019
		LT1021 DS	11	NA	LT1021
	Precision High Current Reference (1.5A)	AN42	12	57	LT317AH, LT1001
Discussion	Application Hints for Ultraprecision Reference	LTZ1000 DS	4	NA	LTZ1000

Reference—Voltage (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Discussion (Continued)	Effects of Air Movement on Low Frequency Noise	LT1021 DS	10	NA	LT1021
	Heat Mode Reduces Temperature Drift to <2ppm/°C	LT1019 DS	1	NA	LT1019
	Output Trimming	LT1019 DS	5	NA	LT1019
	Trimming Output Voltage	LT1021 DS	8	NA	LT1021
Dual Output	Dual-Output Reference Operates on Two AA Cells	LTM II:3	12	3	LT1004, LT1112
General	Battery-Powered LT1004-2.5 2.5V Voltage Reference	AN62	22	49	LT1004-2.5
	LT1034-2.5 2.5V Voltage Reference	AN62	22	48	LT1034-2.5
	LT1431 2.5V Voltage Reference (8-Pin Package)	AN62	23	51	LT1431
	LT1431Z 2.5V Voltage Reference (3-Pin Package)	AN62	23	50	LT1431Z
	LT1431Z 5V Voltage Reference (8-Pin Package)	AN62	23	52	LT1431Z
High Voltage	Ultraprecision Variable Voltage Reference	AN6	6	7	LT1002/ LM301, LM399A
Low Noise	2-Pole Lowpass Filtered Reference	LT1021 DS	14	NA	LT1021, LT1001
		LT1031 DS	10	NA	LT1031, LT1001
	Low Noise Reference	LTZ1000 DS	1	NA	LTZ1000, LT1006
		LT1004 DS	6	NA	LT1004-1.2
Micropower	1.235V Micropower Reference	LT1004 DS	6	NA	LT1004-1.2
		AN42	10	44, 45	LT1004-1.2
	2.5V Micropower Reference	AN42	11	47	LT1004-2.5
		LT1004 DS	6	NA	LT1004-2.5
	Micropower 5V Reference	LM134 DS	10	NA	LM334, LT1004-1.2
	Self-Buffered Micropower Reference	LT1178 DS	1	NA	LT1178, LT1004-1.2
		DN23	1	1	LT1178, LT1034-1.2
		AN42	11	51	LT1178, LT1004-1.2

Reference—Voltage (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Negative	Basic Negative Reference	AN42	9	33	LT1021-5
		LT1021 DS	1	NA	LT1021
		LT1031 DS	8	NA	LT1031
	CMOS DAC with Low Drift Full-Scale Timing	LT1021 DS	14	NA	LT1021-10, LT1007
	Negative 10V Reference for CMOS DAC	LT580 DS	1	NA	LT581, LT1007
		LT1019 DS	7	NA	LT1019-10, LT1007
	Negative Series Reference	LT1021 DS	11	NA	LT1021-10
		LT1019 DS	8	NA	LT1019
		AN42	9	37	LT1019
		LT1236 DS	8	NA	LT1236-10
	Negative Shunt Reference Driven by Current Source	LT1031 DS	11	NA	LT1031, LM334
		AN42	9	35	LT1031
		LT1021 DS	14	NA	LT1021-10, LM334
		LT1236 DS	10	NA	LT1236-10, LM334
	Negative Voltage Reference	LTZ1000 DS	5	NW	LTZ1000, LT1013
		AN42	16	68	LTZ1000, LT1013
	Ultraprecision Voltage Inverter	AN3	14	20	LTC1043, LT1004-1.2
Precision	±10V Reference	LT1236 DS	9	NA	LT1236-10
	10.24V Reference	LT1236 DS	9	NA	LT1236-10
	10V Buffered Reference	LM199 DS	1	NA	LT1012
		AN42	18	73	LM399, LT1012
	10V Reference with Full Trim Range	LT1236 DS	8	NA	LT1236-10
	10V Reference with Restricted Trim Range for Improved Resolution	LT1236 DS	8	NA	LT1236A-10
	2-Pole Lowpass Filtered Reference	LT1236 DS	10	NA	LT1236, LT1001
	6.95V Reference	LM199 DS	4	NA	LM399
		AN42	19	74	LM399
	Buffered Reference for A/D Converters	LT1012 DS	10	NA	LT1012

Reference—Voltage (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Precision (Continued)	CMOS DAC with Low Drift Full-Scale Trimming	LT1236 DS	9	NA	LT1236-10, LTC7543, LT1007C
	Handling Higher Currents	LT1236 DS	9	NA	LT1236-10
	Operating 5V Reference from 5V Supply	LT1021 DS	15	NA	LT1021-5
		LT1236 DS	9	NA	LT1236-5
	Portable Calibrator	LM199 DS	4	NA	LM399, LT1001AC
	Precision ±10V Reference	LT1002 DS	11	NA	LT1002, LM129A
	Precision DAC Reference with System TC Trim	LT1021 DS	15	NA	LT1021-10
		LT1031 DS	11	NA	LT1031
		LT1236 DS	10	NA	LT1236-10
	Restricted Trim Range for Improved Resolution	LT1021 DS	13	NA	LT1021C-10
	Standard Cell Replacement	LM199 DS	4	NA	LM399, LT1001AC
Shunt	2.5V Reference (LT1431)	AN42	6	10	LT1431Z
		LT1431 DS	6	NA	LT1431
	2.5V Reference (LT1431Z)	AN42	6	11	LT1431
		LT1431 DS	6	NA	LT1431Z
	5V Reference	LT1431 DS	6	NA	LT1431
		AN42	6	12	LT1431
	Programmable Reference with Adjustable Current Limit	LT1431 DS	6	NA	LT1431
		AN42	6	14	LT1431
Standard Cell	Saturated Standard Cell Amplifier	LT1012 DS	10	NA	LT1012
		LT1008 DS	9	NA	LT1008
		LT1097 DS	1	NA	LT1097
	Standard Grade Variable Voltage Reference	AN9	5	9	LTC1052
Ultraprecision	7V Positive Reference	AN42	16	67	LTZ1000, LT1013
		LTZ1000 DS	6	NA	LTZ1000, LT1013

Reference—Voltage (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Ultraprecision (Continued)	Adjusting Temperature Coefficient in Unstabilized Applications	LTZ1000 DS	6	NA	LT1006, LTZ1000
	Averaging Reference Voltages for Lower Noise and Better Stability	LTZ1000 DS	5	NA	LTZ1000
	Low Noise Reference	LTZ1000 DS	1	NA	LTZ1000, LT1006
	Ultraprecision Variable Voltage Reference	LT1002 DS	14	NA	LT1002
		LT1001 DS	10	NA	LT1001
		AN6	6	7	LT1002

Regulators—Linear

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Additional Feature Circuits	1A Regulator with Current Limit	LT1020 DS	12	NA	LT1020
	Bypass Circuit for 3.xxV and 5V Microprocessor Swaps Using High-Side Gate Driver	DN82	1	2	LT1085
	Bypass Circuit for 3.xxV and 5V Microprocessor Swaps with Transistor Buffer	DN82	1	1	LT1085, LTC1157
	Current Limited 1A Regulator	LT1020 DS	12	NA	LT1020
	Improved High Frequency Ripple Rejection	LT1185 DS	14	NA	LT1185
	Improving Ripple Rejection	LT138 DS	7	NA	LT338A
		LT1038 DS	8	NA	LT1038
	Low Temperature Coefficient Power Regulator	LT1009 DS	4	NA	LT1009, LT317A
	Pin-Switchable 3.3V/5V Regulator Configuration	AN58	3	2	(see text)
	Pin-Switchable 3.3V/5V Regulator Configuration with LTC1157	AN58	3	3	LT1157 and linear regulator (see text)

Regulators—Linear (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Additional Feature Circuits (Continued)	Regulator with Reference	LT117HV DS	1	NA	LT317
		LT117 DS	1	NA	LT317
	Remote Sensing	LT138 DS	7	NA	LT338A, LM301A
		AN2	8	13	LT350A
	Voltage Regulator Run from 110VAC or 220VAC	AN2	8	14	LT1086, LT1011
Adjustable	0V to 5V Regulator	LM10 DS	10	NA	LM10
	1.2V–25V Adjustable Regulator	LT138 DS	7	NA	LT338A
		LT1038 DS	8	NA	LT1038
		LT117 DS	7	NA	LT317A
	Adjustable 4.75V to 5.25V In, 3.38V/4A Out Regulator Circuit	DN87	2	3	LT1585CT
	Adjustable Regulator 0V–10V at 5A	LT1003 DS	4	NA	LT1003C, LM301A
	Variable Output Supply	LT1004 DS	6	NA	LT338A, LT1004-1.2
Battery Circuits	Battery Backup Regulator	AN23	18	31	LT1020
	High Current Battery Splitter (150mA)	AN16	21	52	LT1010
		AN8	2	5	LT1010
	Low Voltage Regulator	LM10 DS	10	NA	LM10
Control Circuits	Automatic Light Control	LT1038 DS	10	NA	LT1038
		LT138 DS	8	NA	LT338A
	Lamp Flasher	LT138 DS	8	NA	LT1038
		LT1038 DS	10	NA	LT1038
	Optocoupled Output Control	LT1035 DS	9	NA	LT1005
		LT1005 DS	25	NA	LT1035
	Protected High Current Lamp Driver	LT1038 DS	10	NA	LT1038
		LT138 DS	8	NA	LT338A
Current	Adjustable Current Limiter	LT150 DS	7	NA	LT350A

Regulators—Linear (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Digital System Support	21V Programming Supply for UV PROM/ EEPROM	LT117A DS	7	NA	LT317A
	2816 EEPROM Supply Programmer for Read/ Write Control	LT117A DS	7	NA	LT317AH
	5V Power Supply Monitor with ±500mV Window and 50mV Hysteresis	LT1431 DS	9	NA	LT1431
	Battery Backup Regulator	LT1020 DS	11	NA	LT1020
	Delay Power Up	LT1035 DS	9	NA	LT1035
		LT1005 DS	25	NA	LT1005
		LT1036 DS	6	NA	LT1036
	Fast Turn-Off, Delayed Turn-On	AN1	2	2B	LT1005
		LT1005 DS	24	NA	LT1005
		LT1036 DS	6	NA	LT1036
	First-On, First-Off Sequencing	LT1036 DS	7	NA	LT1036
		LT1035 DS	8	NA	LT1035
		LT1005 DS	24	NA	LT1005
	First-On, Last-Off Sequencing	LT1036 DS	7	NA	LT1036
		LT1005 DS	24	NA	LT1005
		LT1035 DS	8	NA	LT1035
	Logic Controlled 3A Low Side Switch with Fault Protection	LT1185 DS	14	NA	LT1185
	Logic Output on Dropout	LT1020 DS	12	NA	LT1020
	Low Input Voltage Monitor Tracks Dropout Characteristic	LT1185 DS	13	NA	LT1185, LT1006
	LT1020 Shutdown	AN23	18	30	LT1020
	Memory Save on Power Down	LT1035 DS	10	NA	LT1035
		LT1005 DS	26	NA	LT1005, LM311
		AN1	4	6	LT1005
		AN31	8	16	LT1020, LT1086-5

Regulators—Linear (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Digital System Support (Continued)	Power Supply Turn-On Sequencing	LT1036 DS	6	NA	LT1036
		LT1005 DS	24	NA	LT1005
		LT1035 DS	8	NA	LT1035
	Push-On, Push-Off	LT1035 DS	9	NA	LT1035
		LT1005 DS	25	NA	LT1005
	Regulator with Logic Output on Dropout	AN23	17	28	LT1020
	Regulator with Output Shutdown on Dropout	LT1020 DS	11	NA	LT1020
		AN23	17	29	LT1020
	Regulator with Output Voltage Monitor	LT1020 DS	9	NA	LT1020
	Time Delayed Start-Up	LT1185 DS	13	NA	LT1185
Discussion	5V to 3.3V Regulator with Multiple Bypassing	AN58	5	4	LT1085-3.3
	Achieving Low Dropout	AN32	10	NA	NA
	Avoiding Ground Loops	LT1003 DS	5	NA	LT1003
	Bypass Capacitors	LT1003 DS	5	NA	LT1003
		LT1038 DS	5	NA	LT1038
	Bypassing the Adjustment Pin	LT1033 DS	5	NA	LT1033
	Linear Power Supplies—Past, Present and Future	AN11	15	NA	NA
	Load Regulation	LT1083 DS	9	NA	LT1083
		LT1038 DS	6	NA	LT1038
	Output Voltage	LT1033 DS	4	NA	LT1033
	Proper Connection of Divider Resistors	LT1033 DS	5	NA	LT1033
	Protection Diodes	LT1038 DS	5	NA	LT1038
	Raw Supply, Transformer, Diode and Capacitor Selection	LT1003 DS	6	NA	LT1003
	Resistor Table	LT1033 DS	7	NA	LT1033
	Ripple Rejection	LT1083 DS	9	NA	LT1083

Regulators—Linear (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Discussion (Continued)	Table of 1/2% and 1% Standard Resistance Values	LT117 DS	6	NA	NA
	Thermal Considerations	LT1083 DS	10	NA	LT1083
Floating	Floating Regulator	LM10 DS	11	NA	LM10
High Current	Regulator with Current and Thermal Protection (8.5V to 5V, 12A)	AN2	2	2	LT1005
	Regulator with Current and Thermal Protection (8.5V to 5V, 10A)	LT1005 DS	11	NA	LT1005
	Variable Regulator (10A)	LT1038 DS	7	NA	LT1038, LM301A, LT1011
High Voltage	High Voltage Regulator	LM10 DS	12	NA	LM10
	High Voltage Regulator (100V)	AN2	6	11	LT317AT
	High Voltage Regulator (2kV)	AN2	7	11A	LT137A
Low Dropout	10A Regulator with 400mV Dropout	AN32	6	11	LT1072, LT1013
	1A Low Dropout Regulator	LT1020 DS	10	NA	LT1020
	2.5V Micropower Supply	LT1580 DS	1	NA	LT1580-2.5
	2.5V/6A Regulator	LT1580 DS	10	NA	LT1580
	3-Cell to 3.3V Ultralow Drop Regulator with Two Ramped Switches	LTC1163/65 DS	8	NA	LTC1163/LTC1165, LT1431
	3-Cell to 3.3V Ultralow Voltage Drop Regulator	LTC1157 DS	8	NA	LTC1157, LT1431
	3.3V to 2.5V Converter with Shutdown Capability	LTM V:3	8	4	LT1580
	3.3V to 2.5V DC/DC Converter with Shutdown Capability	LTM V:2	14	4	LT1580
	3.3V to 2.5V/6A Regulator	LTM V:2	13	1	LT1580
	3.3V, 7A/4.6A/3A Regulator	LT1584/85/ 87 DS	1	NA	LT1584-3.3/LT1585-3.3/ LT1587-3.3
	3.3V/150mA Converter	AN58	6	8	LT1121-3.3
	3.3V/700mA Converter	AN58	6	9	LT1129-3.3
	4-Cell to 5V Extremely Low Voltage Drop Regulator	LTC1154 DS	12	NA	LTC1154
		LTC1156 DS	5	NA	LTC1156, LT1431

Regulators—Linear (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Low Dropout (Continued)	4-Cell to 5V Low Dropout Regulator with Auto-Reset	LTC1153 DS	13	NA	LTC1153, LT1431
	4-Cell to 5V Regulator with 2A Current Limit, Autoreset, Ramped Turn-On and 10µA Standby Current	LTC1153 DS	13	NA	LTC1153, LT1431
	5V Battery-Powered Supply with Shutdown	LT1521 DS	1	NA	LT1521-5
	5V In, 3.3V/700mA Out, Low Dropout Regulator	DN74	1	1	LT1129-3.3
	5V Low Dropout Regulator	LT1123 DS	1	NA	LT1123
		DN44	1	NA	LT1123
	5V Supply with Shutdown	LT1529 DS	1	NA	LT1529-5
	5V to 3.3V/1.5A (or 3.3V/3A) Converter	AN58	7	11	LT1085-3.3/LT1086-3.3
	5V to 3.3V/125mA Converter	AN58	6	7	LT1020/LT1120
	5V to 3.3V/5A (or 3.3V/7.5A) Converter	AN58	7	12	LT1083/LT1084
	5V to 3.3V/800mA Converter	AN58	6	10	LT1117-3.3
	5V Ultralow Dropout Regulator	LTM I:1	14	1	LT1123
	5V, 3A Regulator with 3.5A Current Limit	LT1185 DS	1	NA	LT1185
	5V/3A Extremely Low Drop Regulator	AN66	83	162	LTC1155, LT1431
	5V/3A Extremely Low Voltage-Drop Regulator	LTM I:2	7	4	LTC1155, LT1431
	>4V In, 3.3V/700mA Out Supply with Shutdown	DN91	1	NA	LT1129-3.3
	A Simple Ultralow Dropout Regulator	DN32	1	2	LT1431, LT1006
	Active Output Pulldown During Shutdown	LT1175-5	7	2	LT1175
	Adjustable Low Dropout Regulator with Kelvin Sense Inputs	LT1087 DS	1–8	NA	LT1087
	Auxiliary +12V Low Dropout Regulator for Switching Supply	LT1185 DS	12	NA	LT1185
	Basic Adjustable Regulator	LT1584/85/87 DS	10	3	LT1584
	Battery-Powered 3.3V/150mA Supply	DN91	1	NA	LT1121-3.3

Regulators—Linear (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Low Dropout (Continued)	Connection for Best Load Regulation	LT1584/85/87 DS	10	4-5	LT1584
	Dual Regulators Power Pentium® Processor or Upgrade CPU	LT1580 DS	12	NA	LT1580, LT1587, LT1006
	FET Low Dropout 5V Regulator with Current Limit	LT1431 DS	7	NA	LT1431
	GTL Termination Voltage Circuit	AN67	19	20	LT1087
	Guaranteed LT1584/LT1431 Circuit for Intel 90MHz and 100MHz Pentium Processors	LT1584/85/87 DS	12	NA	LT1584, LT1431S
	High Efficiency Negative Voltage Regulation	DN21	1	1	LT1086
		DN21	1	2	LT1086
	Low Dropout 5V Regulator	LT1013 DS	17	NA	LTC1044, LT1013
		AN8	3	6	LTC1044, LT1013
		LTC1044 DS	11	16	LTC1044, LT1013
	Low Dropout Regulator for 6V Battery	LT1013 DS	18	NA	LT1013, LT1004-1.2
	Low Parts-Count Linear Supply	AN63	4	3	LT1584CT
	LT1118-2.85 Typical Application	LT1118 DS	1	NA	LT1118-2.85
	LT1121 Micropower Low Dropout Regulator	AN51	5	6	LT1121
	LT1123 Low Dropout Voltage	LT1123 DS	5	NA	LT1123
		AN51	4	4	LT1123
	LT1175 –5V/500mA Regulator	LTM V:1	13	1a	LT1175-5
	LT1175 –6V/500mA Regulator	LTM V:1	13	1b	LT1175-ADJ
	LT1521 Adjustable Operation	LT1521 DS	9	NA	LT1521
	LT1521 Kelvin Sense Connection	LT1521 DS	8	1	LT1521
	LT1521's 12µA Standby Current Eliminates the Need for a Separate Memory Backup Supply	DN121	1	1	LT1521-5, LTC1477
	LT1528 Adjustable Operation	LT1528 DS	7	2	LT1528
	LT1528 Kelvin Sense Connection	LT1528 DS	7	1	LT1528

Regulators—Linear (Continued)					
Category	**Subject**	**Publication**	**Page Number**	**Figure Number**	**LT Part Number(s)**
Low Dropout (Continued)	LT1529 Adjustable Operation	LT1529 DS	8	2	LT1529
	LT1529 Kelvin Sense Connection	LT1529 DS	7	1	LT1529-5
	LT1580 3.3V to 2.5/6A Converter	LTM V:3	7	1	LT1580
	LT1580 Conventional Load Sensing	LT1580 DS	7	1	LT1580
	LT1580 Delivers 2.5V from 3.3V at Up to 6A	DN119	2	1	LT1580
	LT1580 Remote Load Sensing	LT1580 DS	7	2	LT1580
	LT1585 Linear Regulator Optimized for Desktop Pentium Applications	DN91	1	NA	LT1585
	Microprocessor Supply with Shutdown	LT1528 DS	1	NA	LT1528
	Minimum Parts Count LT1585 Adjustable Circuit for Intel 90MHz Pentium Processor	LT1584/85/87 DS	11	NA	LT1585CT
	Optional Clamp Diodes Protect Against Input Crowbar Circuits	LT1580 DS	9	6	LT1580
	PNP Low Dropout 5V Regulator	LT1431 DS	7	NA	LT1431
	Power Supply with Battery Backup	LTM II:2	15	6	LT1121-5
	Precision 3.6V/1A Low Dropout Regulator	LT1366–69 DS	16	6	LT1366, LT1004-1.2
		DN89	1	1	LT1366
	Recommended LT1587-3.45 Circuit for Intel 486 DX4 OverDrive® Microprocessor	LT1584/58/87 DS	11	NA	LT1587-3.45
	Remote, Fully Kelvin Sensed Output (4-Wire)	LT1087 DS	6	NA	LT1087
	Remote Load Regulation Compensation (2-Wire)	LT1087 DS	7	NA	LT1087
	Setting Output Voltage for the LT1580	LT1580 DS	8	5	LT1580
	Typical LT1157 Adjustable Connection	LT1175 DS	6	1	LT1175-5
	Typical LT1175 Connection	LT1175 DS	1	NA	LT1175
	Ultralow Dropout 5V Regulator	AN66	66	135	LT1123
Low Noise	Low Noise Voltage Regulator	LT1028 DS	14	NA	LT1028, LT317A, LT1021-10
	Low Noise Wireless Communications Supply (5V/200mA)	AN66	65	134	LT1021-5

Regulators—Linear (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Low Noise (Continued)	Ultralow Noise 5V, 200mA Supply	LTM IV:2	26	1	LT1021-5
Micropower	1.2V Regulator with 1.8V Minimum Input	LM134 DS	9	NA	LM134
	3.3V to 2.5V/6A Converter	AN66	67	137	LT1580
Microprocessor Power	3.3V to 2.5V/6A Converter with Shutdown	AN66	68	140	LT1580
	Linear Regulator Responds to Fast Load Transients	AN66	69	143	LT1585
Multioutput	Dual Output ±5V 150mA Regulator	LT1020 DS	10	NA	LT1020
	Dual Output Regulator	LT1020 DS	10	NA	LT1020
Negative	High Stability Negative Regulator	LT1033 DS	6	NA	LT1033, LM329B
	Negative Regulator	LT137 DS	1	NA	LT137A
		LM10 DS	11	NA	LM10
		LT1017 DS	6	NA	LT1017/LT1018
Paralleling	5V to 3.3V/10A Converter Using Paralleled LT1087s	AN58	7	13	LT1087
	Parallel Regulators for High Current (5V at 8A)	LT138A DS	1	NA	LT338A, LT350A
	Parallel Regulators for High Current (5V at 15A)	AN2	1	1	LT1083
	Paralleling Devices for Higher Current	LT1087 DS	7	NA	LT1087
	Paralleling Regulators	LT1038 DS	6	NA	LT1038-ADJ
Positive	5V Regulator	LT1020 DS	9	NA	LT1020
	Standard Fixed 5V Regulator	LT1003 DS	1	NA	LT1003
Precision	Dual Regulator Supply for Pentium or Upgrade Processor	DN122	1	2	LT1580, LT1587, LT1006
	High Precision Linear Regulator	AN63	4	4	LT1584, LT1431

Regulators—Linear (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Precision (Continued)	High Stability Regulator	LT137 DS	7	NA	LT337, LM329B
		LT1033 DS	6	NA	LT1033, LM329B
		LT1004 DS	5	NA	LT1004-2.5, LT338A
	Precision High Current Reference	LT150A DS	7	NA	LT350A, LT1001, LT1009
	Precision Power Supply with Two Outputs	LT1001 DS	10	NA	LT1001, LM399, LT301A
		LT1002 DS	14	NA	LT1002, LT301A, LM399
Preregulator	Dual Preregulated Supply (90VAC–130VAC to ±12V)	AN30	30	47	LT1086, LT1011, LT1004-2.5
		LT1086 DS	13	NA	LT1086, LT1011, LT1004-2.5
	High Current Low Dissipation Preregulated Linear Regulator (0V–35V, 0A–10A)	AN2	4	7	LT1038
		LT1038 DS	7	NA	LT1083, LT1011
		LT1083 DS	11	NA	LT1083, LT1011
	High Power Linear Regulator with Switching Preregulator	AN29	25	46	LT1011, LT1083, LM301A
		LT1083 DS	13	NA	LT1011, LT1083, LM301A
	Linear Regulator with Switching Preregulator (28V to Adj.)	AN2	3	5	LT350A, LT1018
	Low Dissipation Regulator (10V–20V to 5V)	LT1035 DS	11	NA	LT1035, LT1010
	Low Dissipation Regulator	LT1036 DS	7	NA	LT1010, LT1036, LT1004-2.5
	Micropower Postregulated Switching Regulator (6V–10V to 5V)	AN23	16	25	LT1020
	Micropower Preregulated Linear Regulator (6V–10V to 5V)	AN32	8	15	LT1020
	Preregulated Low Dropout Regulator (7V–20V to 5V, 7.5A)	AN32	4	8A	LT1083-5, LT1018
	SCR Preregulator (90VAC–140VAC to 15V)	AN32	3	5	LT1086, LT1018
	Switching Preregulated Linear Regulator (9V to 5V)	AN8	5	11	LT1013
		LT1013 DS	13	NA	LT1013
	Switching Preregulator for Wide Input Voltage Range (7.5V–30V to 5V)	LT1020 DS	14	NA	LT1020
	Ultralow Dropout Linear Regulator with Preregulator	AN32	7	13	LT1013, LT1018

Regulators—Linear (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Protection Circuits	Crowbar Overvoltage Protection Circuit	AN31	9	18	LT1018
	Crowbar Protection	LT1003 DS	5	NA	LT1003
		LT123 DS	6	NA	LT123A
	Fast Electronic Circuit Breaker	LT1035 DS	10	NA	LT1035
		AN1	3	3	LT1005
		LT1005 DS	26	NA	LT1005
	Foldback Current Limiting	LT1185 DS	12	NA	LT1185
	High Input Voltage Detection	AN1	3	5	LT1005
		LT1005 DS	25	NA	LT1005
		LT1035 DS	9	NA	LT1035
	Latchoff for V_{OUT} <4.7V	LT1035 DS	8	NA	LT1035
		LT1005 DS	24	NA	LT1005
	Latchoff When Output Shorts	LT1036 DS	6	NA	LT1036
		AN1	2	2C	LT1005
		LT1005 DS	9	NA	LT1005
	Line Dropout Detector	AN1	5	8	LT1005
		LT1005 DS	27	NA	LT1005
		LT1036 DS	7	NA	LT1036, LT1011
	Thermal Cutoff at High Ambient Temperatures	LT1035 DS	8	NA	LT1035
		LT1005 DS	24	NA	LT1005
		AN1	6	10	LT1005
Shunt	Shunt Regulator	LM10 DS	11	NA	LM10
Supply Splitter	5V Supply Splitter	LTM V:3	6	4	LT1118-2.5
	LT1118-2.5 Supply Splitter	DN115	1	1b	LT1118-2.5
	Power Supply Splitter	LT1118 DS	4	NA	LT1118-2.5
	Split Supply Application in which Shutdown Pins Can Be Commanded in Parallel Using Positive Logic	DN121	2	2	LT1521-5, LT1175-5

Regulators—Linear (Continued)					
Category	**Subject**	**Publication**	**Page Number**	**Figure Number**	**LT Part Number(s)**
Supply Splitter (Continued)	Split Supply Saves Power and Holds Bias Point DC Resistance to Less than 0.025Ω	DN121	2	4	LT1521-5, LT1118-2.5
Tracking	Dual Tracking 3A Supply	LT1033 DS	6	NA	LT150A, LT1033
		LT137 DS	7	NA	LT317A, LT337A
	Multiple Tracking Regulators	LT137 DS	7	NA	LT317A
		LT1033 DS	6	NA	LT1033

Regulators—Switching

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Adjustable	High Efficiency Adjustable Regulator with 5.5V < V_{OUT} < 13V	LTC1159	12	6	LTC1159
Backlight	"Hot" Cathode Fluorescent Lamps	AN49	7	A1	NA
	20W CCFL Power Supply	AN55	37	H1	LT1170
		LT1371 DS	14	NA	LT1371
	3.6V to 5.5V In, 4mA CCFL Power Supply	AN65	37	40	LT1172
	88% Efficient CCFL Power Supply	AN65	33	35	LT1172
		AN55	4	6	LT1172
	90% Efficient CCFL Supply	LT1373 DS	11	NA	LT1373
		LT1372/77 DS	11	NA	LT1372/LT1377
	90% Efficient Floating CCFL Configuration with Dual Polarity LCD Contrast	LT1182–84 DS	1	NA	LT1182
		LTM IV:3	11	2	LT1182
	90% Efficient Grounded CCFL Configuration with Dual-Polarity LCD Contrast	LTM IV:3	12	3	LT1182
	90% Efficient Grounded CCFL Configuration with Negative Polarity LCD Contrast	LT1182–84 DS	20	NA	LT1183
	91% Efficient CCFL Power Supply for 5mA Loads with Shutdown and Dimming Inputs	AN55	5	8	LT1172
	91% Efficient CCFL Supply for 5mA Loads, with Shutdown and Dimming Inputs	AN65	34	37	LT1372/LT1377
	92% Efficient CCFL Supply for 10mA Loads, with Shutdown and Dimming Inputs	AN55	5	9	LT1172
		AN65	35	38	LT1372/1377
	9V–15V In, 25W CCFL Power Supply	AN65	39	44	LT1170
	A Lot of Cut-Off Ears and No Van Goghs (Some Not-So-Great Ideas)	AN55	39	J1–J8	NA
	An Inherently Synchronous CCFL Power Supply Eliminates Phase Jitter	AN55	20	34	(Generic)
	Backlight CCFL Supply	LT1572 DS	11	NA	LT1572
	Backlight Efficiency Measurements	AN49	10	NA	NA

Regulators—Switching (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Backlight (Continued)	CCFL Power Supply for Floating-Lamp Configuration Operates on 2.7V	DN133	2	2	LT1513
	CCFL Power Supply for Grounded Lamp Configuration Operates on 2.7V	DN133	1	1	LT1513
	Cold Cathode Fluorescent Lamp (CCFL) Power Supply	AN45	21	36	LT1072
		AN49	2	2	LT1172
		DN52	2	3	LT1072
		LTM II:2	3	1	LT1172
	Dual-Transformer CCFL Supply	AN65	112	I2	LT1184
	Floating CCFL with Potentiometer Control of Lamp Current	LT1182–84 DS	21	NA	LT1184F
	Floating-Lamp CCFL Drive Circuit with Low Parts Count, Open Bulb Protection, and Shutdown	AN65	42	49	LT1184F
	Floating-Lamp CCFL Supply with Bipolar Output Contrast Supply	AN65	43	50	LT1182
	Floating-Lamp CCFL Supply with Internal DAC for Microprocessor Control of Lamp Current	AN65	44	51	LT1186
	Floating-Lamp CCFL Supply	DN99	1	1	LT1182
	High Power CCFL Supply for Desktop Computer Applications	AN65	111	I1	LT1184
	High Power, Multilamp Display, Floating-Lamp CCFL Supply	AN65	47	54	LT1269
	LCD Display Contrast Power Supply	DN47	2	4	LT1172
	Low Power CCFL Power Supply	AN49	5	5	LT1173
		AN55	8	11	LT1173
	Low Power CCFL Supply Controls Lamp Current Over a 1μA–1mA Range	AN65	37	41	LT1173
	Low Thermometer CCFL Power Supply Using Micropower, Precision, Topside-Sensing Amplifier	AN55	18	29	LT1172, LT1077

Regulators—Switching (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Backlight (Continued)	Low Thermometer, Floating-Lamp CCFL Power Supply	AN55	17	28	LT1172
	Low Voltage CCFL Power Supply	LT1301 DS	9	NA	LT1301
	Low Voltage Input, 4mA CCFL Power Supply	AN55	8	10	LT1172
	Low Current CCFL Power Supply	LTM II:2	5	4	LT1173
	LT1172 CCFL Supply with Open-Lamp Protection	AN65	94	E2	LT1172
	LT1183 Grounded-Lamp CCFL Supply with Negative-Output LCD Contrast Supply	AN65	117	J6	LT1183
	LT1184 CCFL Supply, Illustrating Open Lamp Protection	AN65	93	E1	LT1184F
	LT1184F Floating CCFL with Potentiometer Control of Lamp Current	LT1182–84 DS	21	NA	LT1184F
	LT1186 Floating CCFL System Using an Intel 80C31 Microcontroller	LTM V:4	7	2	LT1186
	Modification to Limit Output Voltage of CCFL Power Supply	AN55	34	E1	LT1172
	Options for Shutdown and Intensity Control of CCFL Power Supply	AN55	35	F1	LT1172
	Practical Floating-Lamp CCFL Drive Circuit	AN65	41	48	LT1172
	The Thermometer Effect	AN49	15	NA	NA
	Two-Tube CCFL	AN49	4	4	NA
	Up to 90% Efficient Floating CCFL Supply with SPI Control of Lamp Current	LTM V:4	6	1	LT1186
Boost	100kHz Boost Converter (5V to 12V)	LT1170 DS	1	NA	LT1170
	12V Step-Up Regulator with 1A Circuit Breaker, Breaker Status Feedback and Ramped Output	LTC1153 DS	13	NA	LT1070, LTC1153
	12V Step-Up Regulator with Soft Start, Autoreset Circuit Breaker, Status Feedback and 10μA Standby	LTC1153 DS	13	NA	LT1070, LTC1153
	2-Cell to 3.3V/5V Step-Up Converter	LT1300 DS	1	NA	LT1300

Regulators—Switching (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Boost (Continued)	2-Cell to 5V/200mA Step-Up Converter with Automatic Output Disconnect	LT1300 DS	8	NA	LT1300
		LT1301 DS	8	NA	LT1301
	200mA Output Converter (1.5V to 5V)	AN29	15	23	LT1070, LT1018
		AN30	7	6	LT1070, LT1018
	200mA Output, 1.5V-to-5V Converter	LTM III:1	17	1	LT1170, LT1073
	2V to 5V/110mA Converter	LT1109A DS	6	NA	LT1109A-12
	3.3V/5V to 12V Step-Up Converter	LT1301 DS	1	1	LT1301
	5V to 12V Boost Converter	LT1371 DS	1	NA	LT1371
		LT1372/77 DS	1	NA	LT1372/LT1377
		LT1572 DS	1	NA	LT1572
	5V to 12V/110mA Converter with Shutdown to 0V at Output	LT1109A DS	6	NA	LT1109A-12
	5V to 12V/350mA Boost Converter	AN66	25	38	LT1372/LT1377
	5V to 12V/3A Converter	LTM V:2	26	1	LTC1147
	5V to 12V/500mA High Efficiency Boost Regulator	LTC1266 DS	19	12	LTC1266
	5V to 12V Boost Converter	LT1373 DS	1	NA	LT1373
	90V DC/DC Converter	AN45	19	29	LT1072
	Adding Short-Circuit Protection to an LT1301 Step-Up Switching Regulator	LTC1477/78 DS	7	NA	LTC1477, LT1301
	Basic Flash EEPROM VPP Pulse Generator (5V to 12.75V or 12.00V)	AN30	43	87	LT1072
		DN17	1	1	LT1072
	Boost Converter (1.5V to 5V)	LT1018 DS	7	NA	LT1018, LT1004-1.2
		AN15	7	13	LT1018, LT1004-1.2
		AN30	8	9	LT1018, LT1004-1.2
	Boost Converter (15V to 90V)	LT1082 DS	10	NA	LT1082

Regulators—Switching (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Boost (Continued)	Boost Converter (5V to 12V)	AN19	17	18	LT1070
		AN30	5	1	LT1070
		AN46	1	1	LT1070
	Boost Converter (5V to 12V/0.5A)	LT1269/71 DS	4	NA	LT1271
	Boost Converter (5V to 12V/250mA)	LT1072 DS	1	NA	LT1072
	Boost Regulator (5V to 12V/1.5A)	LT1268 DS	4	NA	LT1268CT
	Boost Regulator with 5.3V ±1%/3.75A	LT1268 DS	1	NA	LT1268
	Current Boosted Boost Converter (16V–24V to 28V)	LT1070 DS	9	NA	LT1070
		AN30	5	3	LT1070
		AN19	44	NA	LT1070
	4-Cell to 5V/200mA Converter	LT1301 DS	8	NA	LT1301
	High Repetition Rate VPP Pulse Generator (5V to 12.75V or 12.00V)	AN30	43	88	LT1072, LT1006, LT1010, LT1004-1.2
		DN17	2	3	LT1072, LT1006, LT1010, LT1004-1.2
	Local 12V to 13.75V Regulator for Use with the LT1312	AN60	7	10	LT1111, LT1312
	Local 5V to 13.75V Boost Regulator for Use with the LT1312	AN60	7	9	LT1172, LT1312
	Low Noise Converter (5V to ±15V)	AN30	11	14	LT1054, LT1086, LT337A
		AN29	2	1	LT1054, LT1086, LT337A
	Low Quiescent Current Boost Regulator (150µA, 6V to 12V)	AN29	9	12	LT1070, LT1017
	Low Quiescent Current Flyback Regulator (150µA, 6V to 12V)	DN11	2	2	LT1070, LT1017, LT1004-1.2
		AN30	6	5	LT1070, LT1017, LT1004-1.2
	Low Voltage Circuit Provides Constant Output Voltage as Battery Discharges	DN41	1	1	LT1270
	LT1372 2.7–11V In, 12V Out Boost Converter	LTM IV:3	20	4	LT1372
	LT1372 Dual-Output (±15V) Flyback Converter with Overvoltage Protection	AN66	26	41	LT1372

Regulators—Switching (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Boost (Continued)	LT1372 Positive-to-Negative Converter (2.7V to 16V In, –5V Out) with Direct Feedback	AN66	26	40	LT1372
	LT1377-Based 1MHz 8V–30V In, 5V/1A Out Boost Converter	LTM V:3	24	1	LT1377
	LTC1147-Based 5V to 12V/3A Converter	AN66	24	37	LTC1147
	LT1372 Boost Converter (2.7V to 11V In, 12V/350mA Out)	DN125	1	1	LT1372
	Negative Boost Converter (–5V In, –9V/175mA Out)	LTC1174 DS	13	NA	LTC1174-3.3
	Negative Boost Converter (–5V to –15V to –15V)	LT1074 DS	14	21	LT1074
		AN44	33	21	LT1074
	Negative Boost Regulator	LT1072 DS	11	NA	LT1072
	Negative Boost Regulator (–15V to –28V)	AN19	42	31	LT1070
		LT1070 DS	11	NA	LT1070
		AN30	5	4	LT1070
	Regulated Up Converter (5V to 10V)	LT1018 DS	7	NA	LT1018
		AN30	8	8	LT1018, LT1004-1.2
	Single Cell to 5V Supply	DN123	2	3	LT1300, LTC1444
	Single Cell Up Converter (1.5V to 5V)	AN30	8	11	LM10
		AN8	8	18	LM10
	Single Inductor Dual Output Converter (5V to ±15V)	AN30	13	16	LT1072, LT1054
		AN30	10	13	LT1018
		AN29	6	6	LT1018, LT1004-1.2
	Single-Inductor, Dual-Polarity Regulator (6V to ±15V)	LT1013 DS	17	NA	LT1013, LT1004-1.2
		AN8	10	22	LT1013, LT1004-1.2
		AN30	9	12	LT1013, LT1004-1.2
	Single Li-Ion Cell to 5V Converter	LT1371 DS	13	NA	LT1371
	Single Li-Ion Cell to 5V Converter/Switch with Load Connect Below 2.7V	LTC1477/78 DS	7	NA	LTC1477, LT1304CS8-5

Regulators—Switching (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Boost (Continued)	Typical LTC1472 PCMCIA V_{CC} and VPP Switch Matrix Application	AN60	3	2	LTC1472, LT1301
	Ultralow Noise Sine Wave Drive (5V to ±15V)	AN30	12	15	LT1006, LT1010, LT1013, LT1009-2.5, LT1021
		AN29	4	4	LT1006, LT1010, LT1013
	Up Converter (1.5V to 5V)	AN30	8	10	LM10
	Up Converter (6V to 15V)	AN8	9	20	LT1013, LT1004-1.2
		LT1013 DS	18	NA	
		AN30	7	7	
	Voltage Boosted Boost Converter (15V to 100V)	AN30	8	2	LT1070
		AN19	41	30	
		LT1070 DS	9	NA	
Buck	"Current Boosted" Step-Down Regulator (20V–30V to 5V)	AN44	25	18	LT1074
		AN35	5	12	LT1074
		LT1074 DS	13	NA	LT1074HV
	12V to 5V Buck Converter with Foldback Current Limit	LT1431 DS	8	NA	LT1431, LT1089
	12V–36V to 5V/5A Step-Down Regulator	LTM III:2	25	1	LTC1149-5
	1MHz, 8V–30V to 5V/1A Converter	AN66	10	11	LT1377
	2.5mm High 5V to 3.3V/500mA Converter	LTM V:1	11	8	LTC1265-3.3
		AN66	23	34	
	2.5mm Max Height 5V to 3.3V/500mA Converter	LTC1265 DS	15	NA	LTC1265-3.3
	2.5V/2A Regulator (3.5V to 12V In)	LTC1147 DS	15	11	LTC1147L
	250kHz High Efficiency 12V In, 5V/2A Output Regulator	LTC1149 DS	17	13	LTC1149-5
	25W High Efficiency Regulator (12V to 36V In, 5V/2.5A Out) Using N-Channel MOSFET Switches	LTC1149 DS	19	16	LTC1149-5
	3.3V Regulator with Capacitive Charge Pump for $EXTV_{CC}$	LTC1267 DS	11	5b	LTC1267

Regulators—Switching (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Buck (Continued)	3.3V Regulator with Inductive Boost Circuit for $EXTV_{CC}$	LTC1267 DS	11	5a	LTC1267
	3.3V/1.25A Low Dropout, High Efficiency Regulator (3.5V to 12V In)	LTC1147 DS	14	8	LTC1147-3.3
	3.3V/2A Output, High Efficiency Regulator	LTC1147 DS	15	12	LTC1147-3.3
	4V to 12V In, 3.3V/1A Out, Surface Mount Regulator	DN98	2	4	LTC1265-3.3
	4V to 14V In, 5V/1A Regulator	LTC1148 DS	19	16	LTC1148
	50 Watt, High Efficiency 40V In, 5V Out Switching Regulator	LTM V:4	15	4	LT1160, LT1846
	5:1 Input Range (4V to 20V) High Efficiency 3.3V/2.5A Regulator	LTC1159 DS	16	11	LTC1159
		LTC1159 DS	16	11	LTC1159-3.3
	5V High Current Step-Down (30V–60V to 5.1V/12A)	DN59	1	1	LT1241
	5V In, 3.3V/150mA Out, Surface Mount DC/DC Converter	DN98	1	1	LTC1574-3.3
	5V In, 3.3V/2A Out, 94% Efficiency Synchronous Buck Regulator	DN74	1	2	LT1148-3.3
	5V In, 3.3V/2A Low Dropout, High Efficiency Regulator	LTC1148 DS	17	13	LTC1148L-3.3
	5V to 3.3V/10A Converter	LTC1430 DS	1	NA	LTC1430
		LTC1262 DS	6	NA	LTC1262, LTC1148-3.3
	5V to 3.3V/0.5A Converter	AN58	8	16A	LTC1147-3.3
	5V to 3.3V/10A DC/DC Converter for Pentium-Class Microprocessor	LTM V:2	20	5	LTC1430
	5V to 3.3V/10A Switching Regulator	AN58	1	22A	LT1158, LT1431
	5V to 3.3V/15A High Efficiency Switching Regulator	LTM III:2	23	1	LT1158, LT1431
	5V to 3.3V/175mA Converter	AN58	7	14A	LTC1174-3.3
	5V to 3.3V/1A Buck Converter with Surface Mount Technology	AN58	9	17A	LTC1147-3.3
	5V to 3.3V/1A Converter	LTM III:2	9	2	LTC1147-3.3

Regulators—Switching (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Buck (Continued)	5V to 3.3V/425mA Converter	AN58	8	15A	LTC1174-3.3
	5V to 3.3V/5A Buck Converter	AN58	12	20A	LTC1148-3.3
	5V to 3.3V/7A High Efficiency Switching Regulator	AN58	13	21A	LT1158, LT1431
	5V/10A High Efficiency Step-Down Switching Regulator	LTM II:1	4	2	LT1158, LT3525
	5V/1A High Efficiency Regulator with Extended Input Voltage Range (5.2V to 18V)	LTC1148 DS	16	10	LTC1148HV-5
	6.5V to 18V In, Triple Output (3.3V/2A, 5V/2A, 12V/150mA) High Efficiency Power Supply	DN78	2	2	LTC1142, LT1121
	6V to 24V In, 3.3V/0–3A and 5V/0–3A Out, High Efficiency Surface Mount Supply	DN77	2	3	LTC1149
	6V to 25V In, 5V/1.25A Out Buck Converter	LT1375/76 DS	1	NA	LT1376-5
	8 to 24V In, 5V/0–3A and 3.3V/0–5A Out, High Efficiency Supply	DN72	2	2	LTC1149
	87% Efficient 48V to 5V DC/DC Converter	LTM III:1	12	7	LTC1149-5
	90% Efficiency, 40V to 5V/10A Low Dropout, Voltage Mode Switching Regulator	LT1160 DS	12	4	LT1160, LT3526
	90% Efficiency, Low Dropout Current Mode Switching Regulator	LT1160 DS	12	5	LT1160, LT1846
	90% Efficient Positive Buck with Synchronous Switch (9.5V–14.5V to 5V)	AN30	16	22	LT1072
		AN29	18	32	LT1072
	9V to 5V/175mA Converter	AN66	35	61	LTC1174-5
	9V to 5V/425mA Converter	AN66	35	63	LTC1174-5
	A Practical Step-Down Regulator Using the LT1074 (10V–60V to 5V)	AN35	2	3	LT1074
		AN46	3	5	
		AN44	18	15	
	A Simple Loop Reduces Quiescent Current to 150µA (12V to 5V)	AN35	7	16	LT1074, LT1017

Regulators—Switching (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Buck (Continued)	Adding Synchronous Switching to a Step-Down Switching Regulator	LT1160 DS	11	2	LT1160
	Adjustable 0V–5V/1.5A Power Supply	LTM IV:1	23	1	LT1076, LT1006
	Adjustable Linear Postregulator Maintains Efficiency (35V to 1.2V–28)	AN35	7	15	LT1006, LT1085, LT1074
	Adjustable Voltage Regulator with Precision Adjustable Current Limit	LT1510 DS	16	NA	LT1510
	All N-Channel 3.3V/5A Regulator with Drivers Powered from Separate Power V_{IN} Supply	AN66	6	4a	LTC1266-3.3
	All N-Channel 3.3V/5A Regulator with External Power V_{IN}	LTM V:1	4	3a	LTC1266-3.3
	All N-Channel 4V to 14V In, 3.3V/5A Out Regulator with Drivers Powered from External V_{IN}	DN103	2	2a	LTC1266
	All N-Channel 5V to 3.3V/10A High Efficiency Regulator	LTC1266 DS	19	14	LTC1266-3.3
	All N-Channel 5V to 3.3V/10A Regulator	LTM V:1	5	4a	LTC1266-3.3
	All N-Channel, 5V to 2.5V/5A High Efficiency Regulator	LTC1266 DS	19	15	LTC1266
	All N-Channel, 5V to 3.3V/5A Converter with Drivers Powered from External PWR V_{IN} Supply	LTC1266 DS	18	13	LTC1266-3.3
	All N-Channel, 5V/8A High Efficiency Regulator (Burst Mode™ Suppressed)	LTC1148 DS	20	18	LTC1148HV-5
	All N-Channel, Single Supply 5V to 3.3V/10A Regulator	AN66	6	5a	LTC1266-3.3
	All Surface Mount, 5.2V to 14V In, 3.3V/1A and 5V/2A Out Converter	LTC1143 DS	15	10	LTC1143
	All Surface Mount, 5.2V to 14V In, 3.3V/2A and 5V/2A Out Converter	LTC1143 DS	15	11	LTC1143
	Basic Positive Buck Converter	LT1074 DS	1	NA	LT1074
		LT1176 DS	1	NA	LT1176-5
	Buck Regulator, 1A (8V–30V to 5V)	LT3524 DS	1	NA	LT3524
		AN30	18	25	LT3524

Regulators—Switching (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Buck (Continued)	Capacitive Charge Pump for EXTVcc	LTC1159 DS	11	5b	LTC1159-3.3
	Coupled Inductor Provides Positive and Negative Outputs (28V to 15V, –5V)	AN35	3	8	LT1074, LT1086
	Dual Regulator with 5.2V to 18V In, and 3.6V/2A and 5V/2A Outputs	LTC1142 DS	17	11	LTC1142-ADJ
	Floating Input, Low Saturation Loss Buck Regulator	DN21	2	3	LT1070
	Gate Drive Using 5 and 12V Supplies	LTM V:2	19	2b	LTC1430
	Gate Drive Using 5V Supply	LTM V:2	19	2a	LTC1430
	More Sophisticated Loop Gives Better Regulation while Maintaining 150µA Quiescent Current (12V to 5V)	AN35	8	18	LT1074, LT1017
	High Current, Low Dissipation, Preregulated Linear Regulator (0V–35V, 0A–10A)	LT1083 DS	11	NA	LM301A, LT1011, LT1083, LT1004-1.2
		AN30	33	52	LT1011, LT1083, LT317AH, LT1004-2.5
		AN2	4	7	LT1011, LT1038
	High Current, Positive Buck with Bootstrapped NMOS Gate drive (15V–35V to 5V)	AN30	44	89	LT1072, LT317A
	High Current Supply for Standard 3.3V CPUs	AN63	3	1	LTC1266
	High Current, High Efficiency 15V to 40V In, 5V/10A Output Regulator	LTC1159 DS	16	12	LTC1159-5
	High Efficiency 15V to 40V In, 12V/5A Output Regulator	LTC1159 DS	17	13	LTC1159
	High Efficiency 24V In, 12V/3A Output Regulator	LTC1149 DS	19	17	LTC1149
	High Efficiency 3.3V Regulator with Burst Mode Operation	AN51	3	3	LT1271, LT1269, LT1432
	High Efficiency 48V In, 5V/2A Output Regulator	LTC1149 DS	18	14	LTC1149
	High Efficiency 4V–12V In, 3.3V/425mA Out Regulator	LTC1574 DS	7	NA	LTC1574-5
	High Efficiency 5.2V to 18V In, Dual 3.3V/2A and 5V/2A Out Converter	LTC1142 DS	1	NA	LTC1142

Regulators—Switching (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Buck (Continued)	High Efficiency 5.5V to 25V In, 3.3V/3A and 5V/3A Out Regulator	DN114	2	2	LTC1267
	High Efficiency 50W DC/DC Converter	DN59	2	3	LT3525, LT1158
	High Efficiency 5V Buck Converter	AN66	20	29	LT1271, LT1432
	High Efficiency 5V or 12V In, 3.3V/5A Out Supply for Pentium Processor	DN90	1	1	LTC1148
	High Efficiency 5V Regulator with Burst Mode Operation	LT1269/71 DS	1	NA	LT1271, LT1432
		LT1432 DS	1	1	LT1170/LT1271, LT1432
		AN51	3	2	LT1271/LT1269, LT1432
	High Efficiency 5V to 3.3V/1.5 Converter in 0.6 Square Inches	AN66	13	17	LTC1147-3.3
	High Efficiency 5V to 3.3V/1.5A Converter	LTM IV:1	29	1	LTC1147-3.3
	High Efficiency 5V to 3.3V/1A Converter	LTC1265 DS	13	NA	LTC1265-3.3
		AN66	23	32	LTC1265-3.3
	High Efficiency 5V to 3.3V/1A Converter with Extended Input Voltage Range	LTC1148 DS	16	11	LTC1148HV-3.3
	High Efficiency 5V to 3.3V/5A Step-Down Converter	AN66	7	7	LTC1148-3.3
		LTM III:3	26	1	LTC1148-3.3
	High Efficiency 5V/1A Step-Down Converter	AN66	22	30	LTC1265-5
	High Efficiency 5V/2A Step-Down Regulator	LTC1159 DS	1	1	LTC1159-5
	High Efficiency 8V to 20V In 3.3V/3A Output Regulator	LTC1149 DS	16	11	LTC1149-3.3
	High Efficiency 8V to 20V In, 2.5V/5A Output Regulator	LTC1159 DS	15	10	LTC1159
	High Efficiency 8V to 20V In, 3.3V/1A Output Regulator	LTC1149 DS	16	10	LTC1149-3.3
	High Efficiency Adjustable 3A Regulator	LTC1148 DS	17	13	LTC1148L-3.3
	High Efficiency Buck Converter	AN46	7	14	LT1070, LT1431
		LT1270 DS	1	NA	LT1270, LT1431

Regulators—Switching (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Buck (Continued)	High Efficiency Buck Converter with Active Catch Diode	AN44	15	11	LT1074
	High Efficiency Power Supply Providing 3.3V/2A with Built-In Battery Charger	LTC1142 DS	18	14	LTC1142HV-ADJ
	High Efficiency Regulator 4.5V to 18V In, 3.3V/2A and 2.5V/1.5A Out	LTC1142 DS	17	12	LTC1142HV-ADJ
	High Efficiency Regulator with 5.2V to 8V In, 3.3V/3A and 5V/2A	LTC1142 DS	18	13	LTC1142HV
	High Efficiency Regulator with $5.5V < V_{OUT} < 13V$	LTC1159 DS	12	6	LTC1159
	High Efficiency Step-Down Converter (5.5V–16V In, 5V/175mA Out)	LTC1574 DS	1	NA	LTC1574-5
	High Efficiency Step-Down Converter	LTC1266 DS	1	NA	LTC1266-3.3
	High Efficiency Step-Down Converter (5.2V to 14V In, 5V/2A Out)	LTC1147 DS	1	1	LTC1147-5
	High Efficiency Step-Down Converter (5.2V to 18V In, 5V/2A Out)	LTC1148 DS	1	1	LTC1148HV-5
	High Efficiency Step-Down Regulator	LTC1159 DS	1	1	LTC1159
	High Efficiency Step-Down Regulator (5V/2A Out)	LTC1149 DS	1	1	LTC1149-5
	High Efficiency Step-Down Converter (5.4V to 12V In, 5V/1A Out)	LTC1265 DS	1	NA	LTC1265-5
	High Efficiency, 5V to 3.3V/4.5A Converter	LTC1148 DS	18	15	LTC1148-3.3
	High Efficiency, Dual 5.2V to 14V In, 3.3V/2A and 5V/2A Out Converter	LTC1143 DS	1	1	LTC1143
	High Output Voltage (24V/2A) Buck Regulator	AN66	11	13	LTC1149, LT1211
	High Output Voltage (26–35V In, 24V/2A Out) Buck Regulator	LTM V:2	37	1	LTC1149, LT1211
	High Power Linear Regulator with Switching Preregulator	LT1083 DS	13	NA	LT1011, LT1083
		AN30	30	46	
		AN29	25	46	
	High Precision Microprocessor Supply	AN63	3	2	LTC1266, LT1431

Regulators—Switching (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Buck (Continued)	Inductive Boost Circuit for $EXTV_{CC}$	LTC1159 DS	11	5a	LTC1159-3.3
	Linear Regulator with Switching Preregulator (28V to Adj.)	AN30	31	48	LT1018, LT350A
		AN2	3	5	
	Logic Selectable 5V/1A or 3.3V/1A, High Efficiency Regulator	LTC1148 DS	19	17	LTC1148
	Logic Selectable 5V/2A or 3.3V/2A High-Efficiency Regulator	LTC1149 DS	18	15	LTC1149
	Logic-Selectable 0V/3.3V/5V 700mA Regulator	LTC1265 DS	15	NA	LTC1265
	Low Dissipation Regulator (10V–20V to 5V)	LT1036 DS	7	NA	LT1036, LT1011
		LT1035 DS	11	NA	LT1035, LT1011
		AN30	32	50	LT1035, LT1011
	Low Dropout 3.3V/3A Complementary MOSFET Regulator	AN66	7	6a	LTC1266-3.3
	Low Dropout 3.3V/3A High Efficiency Regulator	LTC1266 DS	17	11	LTC1266-3.3
	Low Dropout 5.5V–12.5V In, 5V/365mA Out Regulator with Low-Battery Detection	LTC1574 DS	7	NA	LTC1574-5
	Low Dropout 5.5V–12V In, 5V/2A Out Converter	AN66	19	27	LTC1147-5
	Low Noise 5V In, 3.3V/425mA Out Regulator	DN98	1	3	LTC1574
	Low Noise 5V to 3.3V/425mA Regulator	LTC1574 DS	5	5	LTC1574
	Low Noise, High Efficiency 4V–12.5V In, 3.3V/450mA Out Regulator	LTC1574 DS	6	NA	LTC1574
	Low Output, 5V/2.5A High Efficiency Regulator	LTC1266 DS	18	12	LTC1266-5
	Low Power Switching Regulator (9V to 5V)	LT1013 DS	13	NA	LT1013
		AN8	4	9	
		AN30	17	23	
	Low Quiescent Current Buck Converter (150µA, 8V–16V to 5V)	AN30	14	18	LT1072, LT1017
		AN29	12	19A	

Regulators—Switching (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Buck (Continued)	Low-Dropout 3.3V/3A Complementary MOSFET Regulator	LTM V:1	5	5a	LTC1266-3.3
	Low-Dropout 5V/2A Regulator	LTM III:1	12	6	LTC1148-5
		LTM III:2	10	6	LTC1147-5
	LT1070 Floating Input Step-Down Switching Regulator	AN46	5	9	LT1070
	LT1070 High Efficiency Buck Switching Regulator	AN46	7	14	LT1070, LT1431
	LT1074 Step-Down Regulator	LTM I:1	8	2	LT1074
	LT1074/LT1076 Adjustable 0V–5V/1.5A Power Supply	AN66	14	19	LT1074/LT1076, LT1006, LT1029
	LT1158 (24V to 5V/10A) Buck Converter	AN52	9	10	LT3525, LT1158
	LT1377-Based Buck Converter	DN125	2	7	LT1377
	LTC1147 High Efficiency 5V to 3.3V/1A Converter	AN66	17	23	LTC1147-3.3
	LTC1148 94% Efficient 5V to 3V Converter	LTM III:1	10	2	LTC1148-3.3
	LTC1149-5 12V–36V to 5V/5A Converter Using N-Channel MOSFETs	AN66	9	9	LTC1149-5
	LTC1266 5V In, 3.38V/7A Supply for Pentium and Other High Speed Microprocessors	DN91	2	NA	LTC1266
	LTC1267 Dual, Adjustable High Efficiency Regulator	AN66	13	16	LTC1267-ADJ
		LTM V:1	8	4	LTC1267
	LTC1267 Dual-Output (3.3V and 5V/2A) High Efficiency Regulator	LTM V:1	8	3	LTC1267-ADJ
	LTC1267 Dual-Output 3.3V/2A and 5V/2A High Efficiency Regulator	AN66	12	15	LTC1267
	LTC1430 5V to 3.3V/10A Regulator	DN113	1	1	LTC1430
	LTC1574 Adjustable Configuration	LTC1574 DS	5	3	LTC1574
	LTC1575 Low-Battery Comparator	LTC1574 DS	5	2	LTC1574
	Micropower Postregulated Switching Regulator (6V–10V to 5V)	AN30	32	51	LT1020
		AN23	16	25	

Regulators—Switching (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Buck (Continued)	Micropower Switching Regulator (5.8V–10V to 5V)	AN30	17	24	LT1017
		AN23	15	22	
	Negative Buck Converter (–20V In, –5.2V/1A Out)	LT1072 DS	11	NA	LT1072
	Negative Buck Converter (–20V to –5.2V/ 4.5A)	AN19	21	19	LT1070
		AN30	16	21	
		LT1070 DS	10	NA	
	Negative Buck Converter (–8V to –30V In, –5.2V/3.5A Out)	LT1269/71 DS	4	NA	LT1271
	No-Design Switching Regulator	DN48	2	1	LT1074
	Pentium P54C 5/10A Power Supply Circuit	LTM V:1	19	1	LTC1266
	Pentium P54C-VR and P54-VRE Power Supply Circuit	LTM V:1	20	2	LTC1266, LT1431
	Positive (3.3V–7.5V) to Negative (–5V) Converter	AN66	24	36	LTC1265-5
	Positive (4V–7.5V) to Negative (–5V/150mA) Converter with Low-Battery Detection	AN66	36	65	LTC1174-5
	Positive Buck Converter	LT1070 DS	10	NA	LT1070
		AN30	15	20	
		AN19	27	21	
	Positive Buck Converter (12V–35V to 5V)	AN29	23	42	LT1072
		AN30	13	17	
	Positive Buck Converter (5V/1A Out)	LT1072 DS	11	NA	LT1072
	Positive Buck Converter (7V–15V to 5V/250mA)	AN30	15	19	LT1072
	Reducing LT1376 Input Voltage	LT1375/76 DS	19	10	LT1376-5
	Self-Bypassing 5V to 3.45V High Efficiency Buck Converter	DN82	2	3	LTC1148

Regulators—Switching (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Buck (Continued)	Step-Down Converter with Doubler Charge Pump	LTC1430 DS	7	4	LTC1430
	Switching Preregulated Linear Regulator (9V to 5V)	LT1013 DS	13	NA	LT1013
		AN30	31	49	
		AN8	5	11	
	Switching Preregulator for Wide Input Voltage Range (7.5V–30V to 5V)	LT1020 DS	14	NA	LT1020
		AN30	33	53	
	Tapped-Inductor Buck Converter	LT1074 DS	13	NA	LT1074
	Triple Output 3.3V/2A, 5V/2A and 12V/150mA Notebook Computer Power Supply	AN66	16	22	LTC1142, LT1121
	Triple Output Regulator with Switched 12V Out	LTC1142 DS	19	16	LTC1142
	Typical 3.3A/3V Converter	LT1432-3.3 DS	1	1	LT1432-3.3, LT1271
	Typical 5V to 3.3V Converter Showing Schematic Layout Considerations	LTC1430 DS	13	11	LTC1430
	Typical 5V to 3.3V/10A LTC1430 Application	AN66	4	1	LTC1430
	Ultrawide Input Range (5.5V to 25V), High Efficiency 5V/2A Regulator	LTC1149 DS	17	12	LTC1149-5
Buck-Boost	"5V to 5V" Step-Up or Step-Down Converter	LT1173 DS	14	NA	LT1173
	3-Cell to 3.3V/300mA Buck-Boost Converter	LTM V:2	36	1	LT1303
	3.3V or 5V In, 3.3V and 5V/150mA Regulator Circuit	DN71	1	1	LT1111, LTC1157
	5V Buck Converter with –5V Overwinding	AN66	27	46	LT1176-5
	5V Buck-Boost Converter	LTC1265 DS	14	NA	LTC1265
	A (Better) Negative Output Step-Down Regulator (–5V Out)	LT1074 DS	13	NA	LT1074
		AN35	5	11	LT1074
	LT1070 High Efficiency Positive to Negative Switching Regulator	AN46	10	22	LT1070, LT1431
	Negative Output Step-Down Regulator (12V to –5V)	AN35	4	9	LT1074, LT1006

Regulators—Switching (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Buck-Boost (Continued)	Negative-to-Positive Buck-Boost Converter (–40V to –60V to 5V)	AN29	21	38	LT1072
		AN25	4	4	LT1070
	No Design Switching Regulator	DN49	2	1	LT1074
	Positive Buck-Boost Converter (15V–35V to 28V/250mA)	AN29	24	44	LT1072
		AN30	18	26	LT1072
	Positive-to-Negative Buck-Boost Converter (10V–30V to –12V/2A)	LT1070 DS	9	NA	LT1070
		AN19	43	NA	
		AN30	19	28	
	Positive-to-Negative Converter (4.5V–40V to –5V)	AN46	9	18	LT1074
		LT1074 DS	13	NA	
		AN44	28	19	
	Transformerless 3.5V–40V to 5V/500mA Converter	AN66	28	47	LT1171
	Transformerless 8V–40V to ±15V/500mA Converter	AN66	30	50	LT1074
	All N-Channel, Single-Supply 5V In, 3.3V/10A Out Regulator	DN103	2	1a	LTC1266
Cuk	Low Ripple 5V to –3V "Cuk" Converter	LT1372/77 DS	11	NA	LT1372/LT1377
		LT1373 DS	11	NA	LT1373
		DN125	2	5	LT1373
Discussion	A Checklist for Switching Regulator Designs	AN25	16–17	NA	NA
	Adding Short-Circuit Limiting, True Shutdown and Regulation When There is a High Input Voltage to the LT1301 in Boost Mode	AN66	39	72	LT1301
	Basic Step-Down Circuit	AN35	1	1–2	NA
	Basic Switching Regulator Topologies	AN19	12–17	NA	NA
	Driving External Transistors	AN19	52–53	40–41	LT1070
	Efficiency and Power Characteristics of Switching Regulator Circuits	AN46	NA	NA	NA

Regulators—Switching (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Discussion (Continued)	Eliminating Start-Up Overshoot	AN44	40	NA	NA
		AN19	49	34	LT1070
	Evolution of a Switching Regulator Design	AN25	20–23	D1–D9	LT1070, LT1071
	External Current Limiting	AN19	50–52	35–39	LT1070
	Frequency Compensation	AN25	14	NA	NA
		AN19	47–49	NA	NA
	General Considerations for Switching Regulator Design	AN35	20–24	NA	NA
	Inductor and Transformer Basics	AN19	60–62	NA	NA
	Inductor Selection	DN8	1	1	LT1070
	Inductor Selection—Alternate Method	AN35	22–23	NA	NA
	Input and Output Capacitors	AN19	59	NA	NA
	Input Filters	AN44	42	NA	NA
	LT1070 Operation	AN19	7	NA	NA
		AN25	13–14	NA	NA
		AN29	37–38	NA	NA
	LT1074 Operation	AN35	17–20	NA	NA
	Magnetics Issues	AN35	30	NA	NA
	Optimizing Switching Regulators for Efficiency	AN35	26–27	NA	NA
	Oscilloscope Techniques	AN44	44	NA	NA
	Output Filters	AN44	41	NA	NA
	Output Rectifying Diode	AN19	53	42	NA
	Regulator Efficiency Discussion	AN32	1	NA	NA
	Sensing Negative Output	AN66	40	74	LT1172
	Some Thoughts on DC/DC Converters	AN29	1–44	NA	NA
	Subharmonic Oscillations	AN19	70	NA	NA

Regulators—Switching (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Flyback	Switched Capacitor Voltage Converters—How They Work	AN29	35–36	BI–B3	LT1054
	Switching Diodes	AN25	18	NA	NA
	Techniques and Equipment for Current Measurement	AN35	24–26	NA	NA
	The 5V to ±15V Converter	AN29	33	A1	NA
	Troubleshooting Hints	AN19	68–70	NA	NA
		AN44	47–48	NA	NA
	1.5V to 5V/200mA Converter	AN61	2	3	LT1170, LT1073
	20V–30V In, 5V/1.5A Out Flyback Converter	LT1072 DS	9	NA	LT1072
	800µA Output Converter (1.5V to 5V)	AN30	26	40	LT1017
		AN29	14	20	LT1017
	Dual-Output Flyback Converter with Overvoltage Protection	LT1372/77 DS	11	NA	LT1372/LT1377
	Dual-Output Flyback Converter (2.7V to 13V In, ±15V Out) with Overvoltage Protection	LT1372/77 DS	11	NA	LT1372/77
	Dual-Output Flyback Converter with Overvoltage Protection	LT1371 DS	13	NA	LT1371
		LT1373 DS	10	NA	LT1373
	Flyback Converter (12V to 5V/1A)	AN29	20	37	LT1070
	Flyback Converter (20V–30V to 5V)	AN30	20	29	LT1070
		AN19	30	22	LT1070
	Fully Isolated Regulator (–40V to –60V to 5V)	AN25	6	6	LT1071, LT1006
		AN30	24	38	
	High Efficiency, Flux-Sensed Isolated Converter (12V to 5V)	AN30	22	33	LT1070
		AN29	19	35	LT1071
	High Voltage Power Supply for Ring-Tone Generator	AN67	60	83	LT1070
	Low I_Q, Isolated (5V to ±15V)	AN30	25	39	LT1070, LT1020, LT1017
		AN29	7	8	LT1070, LT1020, LT1017

Regulators—Switching (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Flyback (Continued)	LT1372 Dual-Output (±15V) Flyback Converter with Overvoltage Protection	AN66	26	41	LT1372
		LTM IV:3	21	7	LT1372
	Multioutput Flyback Converter (12V to 5V, ±12V)	AN30	42	85	LT1071, LT1086-12
		DN18	1	1	
	Negative, Current-Boosted Buck Converter	LT1070 DS	10	NA	LT1070
		AN30	23	35	
		AN19	36	27	
	Negative Input/Negative Output Flyback Converter	LT1070 DS	10	NA	LT1070
		AN19	36	28	
		AN30	23	36	
	Positive. Current-Boosted Buck Converter (28V to 5V)	LT1070 DS	12	NA	LT1070
		AN30	22	34	
		AN19	38	26	
	Positive Input/Negative Output Flyback Converter	LT1070 DS	11	NA	LT1070/LT1071
		AN30	24	37	LT1070/LT1006
		AN19	41	29	LT1070
	Power Supply for Subscriber Line Interface Circuit	DN130	2	2	LT1269, LT1006
		DN130	1	1	LT1171, LT1006
	Totally Isolated Converter (5V to ±15V)	AN30	21	31	LT1070/LT1071
		AN19	34	25	
		LT1070 DS	8	NA	
	Transformer-Coupled, Low Quiescent Current Converter (150µA, 12V to 5V ±15)	DN18	2	3	LT1071, LT1086, LT1017
		AN30	42	86	
		AN29	13	19B	
	Wide-Range, Positive Input, Negative Output Flyback Converter (3.5V–35V to –5V)	AN29	22	40	LT1070
		AN30	21	32	

Regulators—Switching (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Forward	Forward Converter (20V–30V to 5V)	AN19	45	NA	LT1070
		AN30	27	41	
		LT1070 DS	11	NA	
	Push-Pull Forward Converter	LT1846 DS	8	NA	LT1846
High Voltage	Converter with 20,000V Isolation (15V to 10V)	AN30	28	44	LT1020, LT1011
		AN29	28	51	
	High Voltage Power Supply (8V–15V to 330V)	AN39	1	1	LT1070
	Isolated Output Converter (15V to 1kV)	AN29	27	50	LT1072, LT1006
		AN30	28	43	
	Nonisolated Converter (15V to 1kV)	AN30	27	42	LT1072
		AN29	26	49	
	Parasitic Capacitance Effects in Step-Up Transformer Design	AN39	1–4	NA	NA
High Voltage, Variable	LT1074 Permits High Voltage Output (28V to 0V–500V)	AN35	12	26	LT1074, LT1086-12, LT1021-7, LT1010, LTC1050
Inverting	4V–12.5V to 3.3V/450mA Converter	AN66	36	66	LTC1174-3.3
	Regulated Charge Pump Power Supply	AN66	34	59	LTC1044A
Inverting, Negative-to-Positive	Negative-to-Positive Buck-Boost Converter	LT1269/71 DS	4	NA	LT1271
	Negative-to-Positive Buck-Boost Converter (–12V In, 12V/0.5A Out)	LT1072 DS	10	NA	LT1072
Inverting, Offline	300kHz Offline Power Supply	LT1241 DS	11	NA	LT1241
Inverting, Positive-to-Negative	10V–20V to –24V Converter	LTM V:1	29	1	LT1172
	10V–20V to –24V/100mA Converter	AN66	40	74	LT1172
	12V to –12V/1A Converter	AN66	33	57	LTC1159
	3.3V, 5V, and 12V, 18.4W High Efficiency Notebook-Computer Power Supply	LTM IV:1	7	2	LT1142, LT1121
	4V to 9V In, –5V/1A Regulator	LTC1148 DS	18	14	LTC1148

Regulators—Switching (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Inverting, Positive-to-Negative (Continued)	High Efficiency 12V to –12V/1A Converter	LTC1159 DS	18	15	LTC1159
		LTM V:1	35	1	
	LT1372 Positive-to-Negative Converter (2.7V to 16V In, –5V Out) with Direct Feedback	LTM IV:3	21	6	LT1372
		AN66	26	40	LT1372
	Positive (3.5V–7.5V) to Negative (–5V) Converter	AN66	24	36	LTC1265-5
	Positive (4V–12.5V) to –5V Converter	LTC1574-5	7	NA	LTC1574-5
	Positive (4V–7.5V) to Negative (–5V/150mA) Converter with Low-Battery Detection	AN66	36	65	LTC1174-5
	Positive-to-Negative Converter	LTM I:1	9	3	LT1074
	Positive-to-Negative Converter with Op Amp Level Shifting	LTM I:1	9	4	LT1074, LT1006
	Positive-to-Negative (–5V) Converter	LTC1265 DS	13	NA	LTC1265-5
	Positive-to-Negative (2.7V to 16V In, –5V Out) Converter with Direct Feedback	LT1372/77 DS	11	NA	LT1372/77
	Positive-to-Negative (4V to 12V In, –5V Out) Converter	LTC1174 DS	12	NA	LTC1174HV-5
	Positive-to-Negative (4V to 13.5V In, –3.3V/ 210mA Out) Converter	LTC1174 DS	12	NA	LTC1174HV-3.3
	Positive-to-Negative 5V Converter (4V to 12V In, –5V/45mA Out)	LTC1174 DS	9	5	LTC1174HV-5
		LTC1574 DS	5	4	LTC1574-5
	Positive-to-Negative Buck-Boost Converter 10V–30V In, –12V/2A Out)	LT1072 DS	10	NA	LT1072
	Positive-to-Negative Converter (4.5V to 20V In, –5V/0.5A Out)	LT1375/76 DS	23	17	LT1376-5
	Positive-to-Negative Converter (4.5V–20V In, –5V/1A Out)	LT1375/76 DS	23	17	LT1376-5
	Positive-to-Negative Converter with Direct Feedback	LT1371 DS	13	NA	LT1371
		LT1372/77 DS	11	NA	LT1372/LT1377
Isolated	Fully Isolated Regulator	AN25	6	6	LT1071, LT1006
		AN30	24	38	LT1071, LT1006

Regulators—Switching (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Isolated (Continued)	High Efficiency, Flux-Sensed Isolated Converter (12V to 5V)	AN30	22	33	LT1070
		AN29	19	35	LT1071
	Isolated 5V ±15V Flyback Converter	LT1431 DS	8	NA	LT1072, LT1172, LT1431
	Low I_Q, Isolated (5V to ±15V)	AN29	7	8	LT1020, LT1070, LT1017
		AN30	25	39	
	Totally Isolated 5V to ±15V Converter	LT1072 DS	9	NA	LT1072
	Totally Isolated Converter (5V to ±15V)	LT1070 DS	8	NA	LT1070/LT1071
		AN19	34	25	
		AN30	21	31	
Laptop	Cold Cathode Fluorescent Lamp (Backlight)	AN51	8	14	LT1172
	Cold Cathode Fluorescent Lamp Power Supply	DN52	2	3	LT1072
	Cold Cathode Fluorescent Lamp (Backlight)	AN49	2	2	LT1172
		AN45	21	36	LT1072
	Inductor and Switch Capacitor Technique Provide Bipolar Output	DN47	1	1	LT1172
	LCD Display Contrast Power Supply	AN49	6	7, 8	LT1172/ LT1173
		DN47	2	4	LT1172
Laser	Helium Neon Laser Power Supply	AN55	38	H2	LT1170
		AN61	7	11	LT1170
	Laser Driver Power Supply	LTM II:2	4	A1	LT1074, LT1018
	Laser Power Supply	AN49	14	D1	LT1074, LT1018, LT1004-1.2
		LT1371 DS	14	NA	LT1371
		LTM III:1	13	1	LT1170
LCD Bias	DC/DC Converter for LCD Bias (3V to ±12V to ±24V)	AN55	9	13	LT1173
	Dual-Output LCD Bias Voltage Generator	AN55	10	15	LT1107
	LCD Bias Circuit Generates –24V	AN51	13	20	LT1172

Regulators—Switching (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
LCD Bias (Continued)	LCD Bias Currents	AN49	6	7, 8	LT1172
	LCD Contrast Positive Boost Converter	LT1182–84 DS	23	NA	LT1182
	LCD Contrast Positive Boost/Charge Pump Converter	LT1182–84 DS	23	NA	LT1182
	LCD Contrast Supply	LT1301 DS	9	NA	LT1301
		LT1300 DS	8	NA	LT1300
	LT1182 LCD Contrast Positive Boost Converter	AN65	116	J4	LT1182
		LT1182–84 DS	23	NA	LT1182
	LT1182 LCD Contrast Positive Boost/Charge Pump Converter	AN65	117	J5	LT1182
		LT1182–84 DS	23	NA	
	LTC1182 LCD Contrast Positive-to-Negative/ Charge Pump Converter	LT1182–84 DS	24	NA	LT1182
	Transformer-Based LCD Contrast Supply	AN55	10	14	LT1172
	Two-Cell LCD Supply Generates –24V at 10mA	AN51	18	25	LT1173
Local Area Network	Isolated Power Supply for Local Area Networks	DN31	1	1	LT1072
Low Power	200mA Output Converter (1.5V to 5V)	AN29	15	23	LT1070, LT1018
		AN30	7	6	LT1070, LT1018
	800µA Output Converter (1.5V to 5V)	AN30	26	40	LT1017
	A Simple Loop Reduces Quiescent Current to 150µA (12V to 5V)	AN35	7	16	LT1074, LT1017
	Battery Splitter	AN30	38	72	LTC1044
		LTC1044 DS	8	9	
		AN8	2	4	
	Better Regulation while Maintaining 150µA Quiescent Current (12V to 5V)	AN35	8	18	LT1074, LT1017

Regulators—Switching (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Low Power (Continued)	Boost Converter (1.5V to 5V)	AN15	7	13	LT1018
		AN30	8	9	
		LT1018 DS	7	NA	
	Generating CMOS Logic Supply From Two Mercury Batteries (2.4V to 4.8V)	LTC1044 DS	1	NA	LTC1044
		AN30	38	71	
	Low Power Switching Regulator (9V to 5V)	AN30	17	23	LT1013
		AN8	4	9	
		LT1013 DS	13	NA	
	Low Quiescent Current Buck Converter (8V–16V to 5V)	AN30	14	18	LT1072, LT1017
		AN29	12	19A	
	Low Quiescent Current Flyback Regulator (150µA, 6V to 12V/2A)	DN11	2	2	LT1070, LT1017
		AN30	6	5	
		AN29	9	12	
	Micropower Postregulated Switching Regulator (6V–10V to 5V)	AN23	16	25	LT1020
		AN30	32	51	
	Micropower Switching Regulator (5.8V–10V to 5V)	AN30	17	24	LT1017
		AN23	15	22	
	Regulated Up Converter (5V to 10V)	AN30	8	8	LT1018
	Regulated Voltage Up Converter	AN8	7	16	LTC1044, LM10
		AN30	39	76	
		LTC1044 DS	11	16	
	Single-Cell Up Converter (1.5V to 5V)	AN8	8	18	LM10
		AN30	8	11	
	Switching Preregulated Linear Regulator (9V to 5V)	AN8	5	11	LT1013
		AN30	31	49	
		LT1013 DS	13	NA	

Regulators—Switching (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Low Power (Continued)	Transformer-Coupled, Low Quiescent Current Converter (12V to 5V, ±12V)	AN29	13	19B	LT1071, LT1086, LT1017
		DN18	2	3	
		AN30	20	30	
	Up Converter (1.5V to 5V)	AN30	8	10	LM10
		LM10 DS	1	NA	
	Up Converter (6V to 15V)	AN8	9	20	LT1013
		AN30	7	7	
		LT1013 DS	18	NA	
Multioutput	17W Dual Output, High Efficiency 5V and 3V Regulator	LTC1159 DS	17	14	LTC1159
	4V to 12V In, ±12V/55mA Output Converter	LTC1174 DS	14	NA	LTC1174
	4V to 12V In, ±5V/135mA Converter	LTC1174 DS	14	NA	LTC1174-5
	4V–12V In to ±12V Out DC/DC Converter	LTC1265 DS	14	NA	LTC1265
	6V–20V In, ±5V Out Regulator Using Only One Inductor	DN100	1	1	LT1376-5
	9V to ±5V, 4.5W Buck Converter	LTM IV:1	32	1	LT1176-5
	Coupled Inductor Provides Positive and Negative Outputs (28V to 15V, –5V)	AN35	3	8	LT1074, LT1086
	Dual Output Switch Capacitor Voltage Generator	LT1026 DS	5	NA	LT1026
		AN30	39	78	
	Dual Output Voltage Doubler	LT1054 DS	11	NA	LT1054
		AN30	35	60	
	Dual Preregulated Supply (90VAC–130VAC to ±12V)	AN30	30	47	LT1086, LT1011
		LT1086 DS	11	NA	
	Dual Regulator with 3.45V/2.5A and 5V/2A Outputs	LTC1267 DS	15	NA	LTC1267-ADJ5
	Dual Regulator with 3.6V/2.5A and 5V/2A Outputs	LTC1267 DS	15	NA	LTC1267-ADJ

Regulators—Switching (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Multioutput (Continued)	High Current Switched Capacitor Converter (6V to ±5V)	AN30	41	84	LT1020, LT1054
		AN29	29	56	
	High Efficiency, Dual 3.3V/2A and 5V/2A Output Regulator	LTC1267 DS	1	1	LTC1267
	High Voltage (3–15V In, ±110V Out) Power Supply for Ring-Tone Generator	LTM IV:2	22	7	LT1070
	Inductor and Switch Capacitor Techniques Provide Bipolar Output	DN47	1	1	LT1172
	Low I_Q, Isolated (5V to ±15V)	AN29	7	8	LT1020, LT1070, LT1017
		AN30	25	39	
	Low Noise (5V to ±15V)	AN29	2	1	LT1054, LT1086, LT337A
		AN30	11	14	
	Multioutput Flyback Converter (12V to 5V ±12V)	DN18	1	1	LT1071, LT1086
		AN30	42	85	
	Multioutput, Transformer-Coupled, Low Quiescent Current Converter	DN18	2	3	LT1071, LT1086, LT1017
		AN30	42	86	
		AN29	13	19B	
	Single-Inductor Regulated Converter (5V to ±15V)	AN30	10	13	LT1018
		AN29	6	6	
	Single-Inductor, Dual-Output Converter (5V to ±15V)	AN30	13	16	LT1054, LT1072
	Single-Inductor, Dual-Polarity Regulator (6V to ±15V)	AN8	10	22	LT1013
		AN30	9	12	
		LT1013 DS	17	NA	
	Switched Capacitor Based (6V to ±7V)	AN30	40	79	LT1020, LT1026
		AN29	31	59	
	Switched Capacitor Charge Pump Based Voltage Multiplier	AN30	36	62	LT1054
		AN29	31	60	

Regulators—Switching (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Multioutput (Continued)	Switched Capacitor Converter (5V to ±12V)	AN29	30	58	LT1054
		AN30	35	NA	
		LT1054 DS	11	NA	
	Totally Isolated Converter (5V to ±15V)	LT1070 DS	17	NA	LT1070/LT1071
		AN30	21	31	
		AN19	34	25	
	Ultralow Noise Sine Wave Drive Converter (5V to ±15V)	AN29	4	4	LT1006, LT1010, LT1013, LT1021
		AN30	12	15	
	Voltage Multiplier (±5V to ±15V)	LT1032 DS	7	NA	LT1032
		AN30	41	81	
Negative Buck	Negative Buck Converter (–7V to –20V In, –5.2V/0.75A Out)	LT1572	11	NA	LT1572
Offline	100W Offline Switching Regulator (5V at 20A)	AN25	8	9	LT1071, LT1006
		AN30	29	45	
	Fully Isolated Flyback 100kHz, 50W Converter	LT1103/ 1105 DS	1	NA	LT1103
	No-Design Offline Power Supply	DN62	2	1	LT1105
Power-Factor Corrected	25W–300W Power-Factor Corrected Supply	LTM III:2	4	2	LT1248
	300W, 24VDC Output Power-Factor Corrected, Universal Input Supply	LTM V:3	14	3	LT1509, LT1431
		AN66	38	68	
Preregulator	300W, 382V Preregulator	LT1248 DS	11	NA	LT1248
	Adjustable Linear Postregulator Maintains Efficiency (35V to 1.2V–28V)	AN35	7	15	LT1074, LT1085, LT1006
	Dual Preregulated Supply (90VAC–130VAC to ±12V)	LT1086 DS	11	NA	LT1086, LT1011
		AN30	30	47	LT1086, LT1010

Regulators—Switching (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Preregulator (Continued)	High Current, Low Dissipation, Preregulated Linear Regulator (0V–35V, 0A–10A)	AN2	4	7	LM301A, LT1011, LT1038
		AN30	33	52	
		LT1083 DS	11	NA	
	High Power Linear Regulator with Switching Preregulator	LT1083 DS	13	NA	LT1083, LT1011
		AN29	25	46	
		AN30	30	46	
	Linear Postregulator Improves Noise and Transient Response (5V Out)	AN35	6	14	LT1074, LT1084-5
	Linear Regulator with Switching Preregulator (28V to Adj.)	AN2	3	5	LT350A, LT1018
		AN30	31	48	
	Low Dissipation Regulator (10V–20V to 5V)	LT1035 DS	11	NA	LT1035, LT1011
		LT1036 DS	7	NA	LT1036, LT1011
		AN30	32	50	LT1035, LT1011
	Micropower Postregulated Switching Regulator (6V–10V to 5V)	AN23	16	25	LT1020
		AN30	32	51	
	Micropower Preregulated Linear Regulator (6V–10V to 5V)	AN32	8	15	
	Preregulated Low Dropout Regulator (7V–20V to 5V)	AN32	4	8A	LT1083, LT1018
	SCR Preregulator (90VAC–140VAC to 15V)	AN32	3	5	LT1086, LT1006, LT1018
	Switching Preregulated Linear Regulator (9V to 5V)	AN30	31	49	LT1013
		AN8	5	11	
	Switching Preregulator for Wide Input Voltage Range (7.5V–30V to 5V)	LT1020 DS	14	NA	LT1020
		AN30	33	53	
	Ultralow Dropout Linear Regulator with Preregulator	AN32	7	13	LT1018, LT1013

Regulators—Switching (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
SEPIC	2 Li-Ion Cells to 5V SEPIC Converter	LT1372/77 DS	12	NA	LT1372/LT1377
		LT1371 DS	13	NA	LT1371
		LT1373 DS	11	NA	LT1373
	5V, 9W SEPIC Converter	DN125	2	3	LT1371
	Buck-Boost Converter (4V to 12V In, 5V/160mA Out)	LTC1174 DS	15	NA	LTC1174HV-5
	Dual-Output SEPIC Converter (6V to 25V In, ±5V Out)	LT1375/76 DS	26	19	LT1376-5
	Transformerless 3.5V–40V In, 5V Out Voltage Regulator	LTM III:2	15	1	LT1171
	Transformerless 8V–40V In, ±5V Out Switching Regulator	LTM III:1	15	2	LT1074
	Transformerless, 8V–40V In, ±15V Out Switching Regulator	LTM III:1	14	1	LT1074
Step-Down: See Buck					
Step-Up: See Boost, Flyback					
Switched Capacitor	–1.24V Generator for 4mA–20mA to 0V–5V Conversion	LTC1261 DS	14	NA	LTC1261
	–1.7V Regulated Charge Pump	LTM IV:2	26	1	LTC1044A
	–4.1V Generator with $1mV_{P-P}$ Noise	LTC1550/51 DS	1	NA	LTC1551-4.1
	–4.1V Out GaAsFET Bias Generator	LTC1550/51 DS	6	NA	LTC1550-4.1
	–4V Converter with Output Filter to Cut Ripple	LTC1429 DS	9	6	LTC1429-4
	–4V Generator with $\overline{\text{Power Valid}}$	LTC1429 DS	1	NA	LTC1429-4
		LTC1261 DS	1	NA	LTC1264-4
	–5V Supply Generator	LTC1429 DS	11	NA	LTC1429CS
		LTC1261	13	NA	LTC1261
	–V In to +V Out Converter	AN29	29	55	LT1054
		AN30	34	58	

Regulators—Switching (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Switched Capacitor (Continued)	100mA Regulated Negative Doubler	LT1054 DS	10	NA	LT1054
	1mV Ripple, 5V In, –4V Out GaAsFET Bias Generator	LTC1429 DS	12	NA	LTC1429-4
		LTC1261 DS	12	NA	LTC1264-4
	1mV$_{P-P}$ Ripple, –4.1V GaAsFET Bias Generator	LTC1550/51 DS	7	NA	LTC1550-4.1
	3.3V In, 4.5V Out, GaAsFET Bias Generator	LTC1429 DS	11	NA	LTC1429
	3.3V In, –4.5V Out GaAsFET Bias Generator	LTC1261 DS	11	NA	LTC1261
	3.5V to 5.5V In, 5V/50mA Out Converter	LT1054 DS	12	NA	LT1054, LTC1044
	4/5V–15V In Voltage Doubler Using the LTC203	DN38	2	6	LTC203
	5V In, –4V Out, GaAsFET Bias Generator	LTC1429 DS	11	NA	LTC1429-4
		LTC1261 DS	11	NA	LTC1261
	5V In, –0.5V Out GaAsFET Bias Generator	LTC1261 DS	13	NA	LTC1261
	5V to ±12V Converter	LT1054 DS	11	NA	LT1054
	Basic Voltage Inverter	LT1054 DS	10	NA	LT1054
		AN30	34	54	
	Basic Voltage Inverter/Regulator	AN30	34	55	LT1054
		LT1054 DS	10	NA	
	Battery Splitter	LTC1144 DS	7	11	LTC1144
	Battery Splitter (9V to ±4.5V)	AN8	2	4	LTC1044
		AN30	38	72	LTC1046
		LTC1046 DS	7	10	
	Charge Pump Negative Voltage Generator	LT1020 DS	13	NA	LT1020
		AN30	41	82	
	Charge Pump Voltage Doubler	LT1020 DS	13	NA	LT1020
		AN30	41	83	

Regulators—Switching (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Switched Capacitor (Continued)	Digitally Programmable Negative Supply	LT1054 DS	12	NA	LT1054, LT1004-2.5
		AN30	37	65	
	Dual Output Switched Capacitor Voltage Generator	AN30	39	78	LT1026
		LT1026 DS	5	NA	
	Dual Output Voltage Doubler	LT1054 DS	11	NA	LT1054
		AN30	35	60	
	Generating –15V from 15V	LTC1144 DS	1	NA	LTC1144
	High Current Switched Capacitor Converter (6V to ±5V)	AN29	29	56	LT1020, LT1054
		AN30	41	84	
	High Power Switched Capacitor Voltage Converter (12V to 5V)	AN29	32	61	LTC1043, LT1011
		AN8	5	12	
		AN3	16	23	
	Low Output Voltage Generator	LTC1261 DS	13	NA	LTC1261
	LTC1550 Low Noise, Regulated, Switched Capacitor Voltage Inverter for GaAsFET Gate Bias	LTM V:4	19	1	LT1550-4.1
	Micropower, ±4.5V to ±15V, Voltage Inverter Using the LTC203	LTC203 DS	7	NA	LTC203
	Minimum Parts Count –4.1V Generator	LTC1550/51 DS	6	NA	LTC1551-4.1
	Minimum Parts Count –4V Generator	LTC1429 DS	12	NA	LTC1429-4
		LTC1261 DS	13	NA	LTC1261-4
	Negative Doubler with Regulator	AN30	37	67	LT1054
		LT1054 DS	13	NA	
	Negative Voltage Converter	LTC1046 DS	6	7	LTC1046
		LTC1044 DS	7	7	
		AN30	37	68	LTC1044
		LTC1144 DS	7	8	LTC1144
	Negative Voltage Doubler	LT1054 DS	10	NA	LT1054

Regulators—Switching (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Switched Capacitor (Continued)	Paralleling for 100mA Load Current	LTC1046 DS	8	11	LTC1046
	Paralleling for Lower Output Resistance	AN30	38	73	LTC1044
		LTC1044 DS	9	11	
		LTC1144 DS	8	13	LTC1144
	Positive Doubler	AN29	30	57	LT1054
		AN30	34	57	
		LT1054 DS	10	NA	
	Positive Doubler with Regulation	AN30	37	66	LT1054, LT1006
		LT1054 DS	12	NA	
	Regulated –5V Supply	LTC1144 DS	8	12	LTC1144
	Regulated Negative Doubler (100mA)	LT1054 DS	10	NA	LT1054
		AN30	35	59	LT1054
	Regulated Negative Voltage Converter	AN8	2	3	LTC1044, LM10
		AN30	39	77	
	Regulated Voltage Up Converter (3V to 5V)	AN8	7	16	LTC1044, LM10
		AN30	39	76	
	Regulating 12V to –5V/200mA Converter	LT1054 DS	12	NA	LT1054
	Regulating 200mA Converter (12V to –5V)	LT1054 DS	12	NA	LT1054
		AN30	36	64	
	Seven Cells to –1.24V Out GaAsFET Bias Generator	LTC1261 DS	12	NA	LTC1261
	Stacking for Higher Voltage	LTC1044 DS	9	11	LTC1044
		AN30	38	74	
	Switched Capacitor Based Converter (6V to ±7V)	AN29	31	59	LT1020, LT1026
		AN30	40	79	
	Switched Capacitor, Charge-Pump Based Voltage Multiplier (5V to ±12V)	AN30	36	62	LT1054
		AN29	31	60	

Regulators—Switching (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Switched Capacitor (Continued)	Switched Capacitor Converter (5V to ±12V)	LT1054 DS	11	NA	LT1054
		AN30	35	61	
		AN29	30	58	
	Switched Capacitor Regulator (3.5V to 5V)	LT1054 DS	12	NA	LT1054, LTC1044
		AN30	36	63	
	Ultraprecision Voltage Divider	LTC1144 DS	7	10	LTC1144
	Voltage Doubler	AN30	38	70	LTC1044
		AN30	37	69	
		LTC1044 DS	8	NA	
		AN8	6	14	
		LTC1144 DS	7	9	LTC1144
	Voltage Inverter	LTC660 DS	8	NA	LTC660
	Voltage Multiplier (±5V to ±15V)	LT1032 DS	7	NA	LT1032
		AN30	41	81	LT1032
	Voltage Tripler/Quadrupler	AN30	39	75	LTC1044
		LTC1044 DS	9	13	
Synchronized	LT1172 Synchronized by Driving the DC/AC Converter	AN55	19	32	LT1172
	Synchronized, Gated-Oscillator 2- to 3-Cell to 5V Switching Regulator	AN61	1	1	LT1107
	Synchronizing the LT1172 by Lowering the Value of L2	AN55	19	30	LT1172
Synchronous	LTC1148 5V In, 3.38V/3.5A Out Pentium Power Solution	DN91	2	NA	LTC1148
Telecom	Fully Isolated Regulator (–40V to –60V to 5V)	AN30	24	38	LT1071, LT1006
		AN25	6	6	
	Negative to Positive Flyback Converter (–40V to –60V to 5V)	AN29	21	38	LT1072HV
		AN25	4	4	LT1070HV

Regulators—Switching (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Ultrahigh Efficiency	Switching Power Supply for Ring-Tone Generator (60V and –180V)	DN134	1	1	LT1070
	Totally Isolated Converter	LT1082 DS	10	NA	LT1082
	High Current, High Efficiency Synchronous Buck (12V–36V to 5V/5A)	DN68	2	3	LTC1149-5
	High Efficiency Synchronous Buck (5.5V–13V to 5V/2A)	DN68	1	1	LTC1148-5
	LTC1148 (10V–14V to 5V/10A, –5V/0.5A) HIgh Current Buck Converter	AN54	19	17A	LTC1148-5
	LTC1148 (2V–5V to 5V/1A) Buck Converter—Surface Mount	AN54	27	25A	LTC1148, LT1109
	LTC1148 (4V–10V to –5V/1A) Positive-to-Negative Converter	AN54	25	23	LTC1148
	LTC1148 (4V–14V to +5V/0.5A,–5V/0.5A) Split-Supply Converter	AN54	24	22A	LTC1148
	LTC1147 (4V–14V to 3.3V/1A) Buck Converter—Surface Mount	AN54	17	15A	LTC1147-3.3
	LTC1148 (4V–14V to 3.3V/2A) Buck Converter—Surface Mount	AN54	7	5A	LTC1148-3.3
	LTC1148 (4V–14V to 5V/1A) SEPIC Converter	AN54	18	21A	LTC1148
	LTC1148 (5V–14V to 5V/1A) Buck Converter—Surface Mount	AN54	3	1A	LTC1148-5
		AN54	3	14	LTC1147-5
	LTC1148 (5V–14V to 5V/2A) Buck Converter—Surface Mount	AN54	4	2A	LTC1148-5
	LTC1148 (5V–14V to 5V/2A) High Frequency Buck Converter—Surface Mount	AN54	5	3A	LTC1148-5
	LTC1149 (10V–48V to 3.3V/2A) High Voltage Buck Converter	AN54	12	10A	LTC1149-3.3
	LTC1149 (10V–48V to 5V/1A) High Voltage Buck Converter	AN54	10	8A	LTC1149-5
	LTC1149 (10V–48V to 5V/2A) High Voltage Buck Converter with Large P-Channel and N-Channel MOSFETs	AN54	11	9A	LTC1149-5

Regulators—Switching (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Ultrahigh Efficiency (Continued)	LTC1149 (12V–36V to 5V/5A) High Current, High Voltage Buck Converter	AN54	20	18A	LTC1149-5
	LTC1149 (12V–48V to 5V/10A) High Current, High Voltage Buck Converter	AN54	15	13A	LTC1149-5
	LTC1149 (32V–48V to 24V/10A) High Current, High Voltage Buck Converter	AN54	16	14A	LTC1149

Regulators—Switching (Micropower)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Backlight	2–6V In CCFL Power Supply	LTM IV:2	17	1	LT1301
	All Surface Mount EL Panel Driver	LTM V:1	32	1	LT1303
		AN66	61	126	
	Backlight LED Driver	AN59	11	20	LT1300
	CCFL Driver	AN59	10	18	LT1300
	Cold Cathode Fluorescent Lamp Driver	LTM III:3	20	6	LT1300
	Compact EL-Panel Display	AN61	8	12	LT1108
	EL Panel Driver	LT1303 DS	11	NA	LT1303
	High Efficiency EL Panel Driver	AN66	59	124	LT1303
		LTM V:2	29	1	
	Low Power CCFL Supply	AN61	5	9	LT1301
	Low Power CCFL Supply Optimized for Low Voltage Inputs (2V–6V) and Small lamps	AN65	38	43	LT1301
	Low Power, Low Voltage CCFL Power Supply	AN66	60	125	LT1301
	Micropower CCFL Driver Delivers up to 1mA	AN51	20	28	LT1173
Boost	12V, 60mA Flash Memory Programming Supply	LT1309 DS	1	NA	LT1309
	2 AA Cell to 5V/200mA DC/DC Converter	LTM III:3	12	2	LT1300

Regulators—Switching (Micropower) (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Boost (Continued)	2 AA Cell to 5V/50mA DC/DC Converter	LTM III:3	13	8	LT1300
	2 AA NiCd to 6V/550mA Converter	LTM II:2	19	1	LT1110
	2- or 3-Cell to 5V/600mA Converter	AN66	44	79	LT1302
	2- or 3-Cell to 5V/600mA or 3.3V/1A DC/DC Converter	LTM IV:2	7	2	LT1302
	2-Cell to 128V/3mA Converter	AN66	57	123	LT1107
	2-Cell to 12V/120mA Converter	AN66	46	86	LT1302
	2-Cell to 12V/120mA DC/DC Converter	LTM IV:2	9	9	LT1302
	2-Cell to 128V DC/DC Converter with Automatic Shutdown	LTM V:1	34	1	LT1107
	2-Cell to 5V/200mA Boost Converter with Only Four External Parts	DN120	1	1	LT1304-5
	2-Cell to 5V/200mA DC/DC Converter	AN66	51	97	LT1300
	2-Cell to 5V/200mA DC/DC Converter with Low-Battery Detect	LT1303 DS	1	1	LT1303-5
	2-Cell to 5V/200mA Boost Converter	LTM V:3	18	2	LT1304-5
	2-Cell to 5V/50mA DC/DC Converter	AN59	5	8	LT1300
	2-Cell to 5V/600mA Converter	LT1302 DS	1	1	LT1302
	2-Cell to 5V/>200mA DC/DC Converter	AN59	3	2	LT1300
	2-Cells to 5V/200mA Converter	AN66	54	109	LT1304-5
	2-Cells to 5V/50mA Converter	AN66	52	102	LT1300
	2V to 12V/120mA Converter	LT1302 DS	14	NA	LT1302
	2V to 5V/300mA Step-Up Converter with Undervoltage Lockout	LT1173 DS	14	NA	LT1173
	3-Cell to 3.3V Boost/Linear Converter with Output Disconnect	LT1303 DS	10	NA	LT1303
	3.3V or 5V to 12V/120mA Converter	AN59	7	13	LT1301
	3.3V or 5V to 12V DC Converter	LTM III:3	14	13	LT1301
	3.3V or 5V to 12V/120mA Converter	AN66	53	107	LT1301
	3V to 12V Step-Up Converter	LT1073 DS	13	NA	LT1073-12

Regulators—Switching (Micropower) (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Boost (Continued)	3V to 15V Step-Up Converter	LT1073 DS	13	NA	LT1073
	3V to 5V Converter	LT1109 DS	7	NA	LT1109-5
	3V to 5V Step-Up Converter	LT1173 DS	13	NA	LT1173-5
		LT1073 DS	13	NA	LT1073-5
		LT1110 DS	15	NA	LT1110-5
	3V to 5V/100mA Step-Up Converter with Undervoltage Lockout	LT1073 DS	16	NA	LT1073
	3V to 6V at 1A Step-Up Converter	LT1073 DS	18	NA	LT1073
	4- to 5-Cell to 5V/100mA Converter with Output Disconnect	LT1303 DS	10	NA	LT1303-5
	5V Step-Up Converter with Reference Output	LT1303 DS	9	NA	LT1303
	5V to 12V Step-Up Converter	LT1073 DS	14	NA	LT1073-12
	5V to 15V Step-Up Converter	LT1073 DS	14	NA	LT1073
	Boost Converter with Added Short-Circuit Limiting, True Shutdown and Regulation with High Input Voltage	LTM V:2	30	1	LT1301
	LT1106 3.3V to 5V/120mA DC/DC Converter	AN60	14	20	LT1106
	LT1300 3.3V to 5V/250mA DC/DC Converter	AN60	14	22	LT1300
	LTC1329 Digitally Controls the Output of a Power Supply	AN67	7	5	LT1107, LTC1329-50
	LTC1477 Controlled by the LT1304's Low-Battery Detector	DN117	2	4	LTC1304, LTC1477
	Main Logic Converter with Backup Converter	AN51	17	24	LT1173
	Setting Output Voltage on the LT1303	LT1303 DS	9	NA	LT1303
	Short-Circuit Protection and 100% Shutdown for a Micropower Boost Regulator	DN117	2	3	LT1301, LTC1477
	Single-Cell to 3.3V Boost Converter (1V In, 3.3V/75mA Out)	DN128	1	1	LT1307
	Single-Cell to 5V Step-Up Converter	LTM I:1	10	2a	LT1073-5

Regulators—Switching (Micropower) (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Boost (Continued)	Single-Cell to 5V/150mA DC/DC Converter	LT1302 DS	14	NA	LT1302, LT1073
		AN61	4	6	
		LTM IV:2	10	13	
	Single-Cell to 5V/150mA or 3.3V/250mA Converter	AN66	47	90	LT1073, LT1302
	Step-Up Converter (5V to 12V)	LT1173 DS	1	NA	LT1173
	Super Burst™ Mode 2-Cell to 5V/80mA Converter	AN66	55	116	LT1304
	Two AA Cell to 5V Step-Up Converter Delivers 150mA	DN52	1	1	LT1073-5
	Two AA Cells to 5V Deliver 150mA	AN51	16	22	LT1108-5
		LT1108 DS	1	NA	LT1108-5
		LT1107 DS	1	NA	LT1107-5
	Two AA Cells to 6V/550mA	AN52	7	8	LT1110
	Typical LT1106 3.3 or 5V to 12V/60mA Boost Regulator	AN60	12	17	LT1106
Buck	2-Cell to 128V DC/DC Converter with Automatic Shutdown	LTM V:1	34	1	LT1107
	2.5mm High, 5V In, 3.3V/500mA Out Regulator	DN105	2	3	LTC1265
	5.5 to 12V In, 5V/175mA Out Surface Mount Regulator	DN73	1	1	LTC1174-5
	5.5V to 12.5V In, 5V/425mA Out Surface Mount Regulator	DN73	1	3	LTC1174-5
	5V In, 3.3V/425mA Out, High Efficiency Regulator	DN91	1	1	LTC1174-3.3
	5V to 3.3V/450mA Buck Regulator	LTM III:2	8	10	LTC1174-5
	6V to 5V/365mA Step-Down Regulator with Low Battery Detection	LTC1174 DS	11	NA	LTC1174-5
	9V to 5V Pre/Post Regulator	LTC1174 DS	13	NA	LTC1174, LT1121-5
	9V to 5V Reduced Noise Step-Down Converter	LT1073 DS	17	NA	LT1073

Regulators—Switching (Micropower) (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Buck (Continued)	9V to 5V Step-Down Converter	LT1073 DS	15	NA	LT1073
		LT1173 DS	13	NA	LT1173-5
		LT1111 DS	14	NA	LT1111
		LTM I:1	11	2b	LT1073
	9V to 5V/175mA Buck Regulator	LTM III:2	6	1	LTC1174-5
	9V to 5V/425mA Buck Regulator	LTM III:2	6	3	LTC1174-5
	Automatic Current Selection Regulator (6V to 12.5V In, 5V at 0–320mA Out	LTC1174 DS	15	NA	LTC1174-5
	High Efficiency 4V to 12.5V In, 3.3V/425mA Out Regulator	LTC1174 DS	11	NA	LTC1174-3.3
	High Efficiency 4V to 12.5V In, 3V/450mA Out Regulator	LTC1174 DS	12	NA	LTC1174
	High Efficiency 5.4V–12V In, 5V/1A Out, Step-Down Converter	DN105	1	1	LTC1265-5
	High Efficiency 5V to 3.3V/1A Converter	LTM V:1	11	6	LTC1265-3.3
	High Efficiency Step-Down Converter (9V In, 5V/175mA Out)	LTC1174 DS	1	NA	LTC1174-5
	High Efficiency Step-Down Converter (5.4V–12V In, 5V/1A Out)	LTM V:1	10	1	LTC1265-5
	High Power, Low Quiescent Current Step-Down Converter	LT1111 DS	15	NA	LT1111
		LT1173 DS	15	NA	LT1173
	Low Noise 5- to 7-Cell to 5V/120mA DC/DC Converter	LTM IV:3	25	1	LTC1174
	Low Noise, High Efficiency 5- to 7-Cell input 5V/120mA Out Step-Down Regulator for Personal Communication	DN86	1	1	LTC1174
	Low Noise, High Efficiency 5V/120mA Step-Down Regulator for Personal Communications Devices	AN66	43	77	LTC1174
Buck-Boost	3-Cell to 3.3V/200mA Bipolar Buck-Boost Converter	DN109	2	3	LT1303
	3-Cell to 3.3V/200mA MOSFET Buck-Boost Converter	DN109	2	4	LT1303

Regulators—Switching (Micropower) (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Buck-Boost (Continued)	3-Cell to 3.3V/300mA Buck-Boost Converter	AN66	41	75	LT1303
	3-Cell to 3.3V/400mA Converter with Auxiliary 12V/120mA Regulated Output	AN66	48	92	LT1302, LT1121
	4-Cell to 5V/100mA MOSFET Buck-Boost Converter	DN110	2	4	LT1303
	4-Cell to 5V/100mAV SEPIC Converter	DN110	1	1	LT1303-5
	4-Cell to 5V/100mA Bipolar Buck/Boost Converter	DN110	2	3	LT1303-5
	9V to 3V Step-Down Converter	LT1073 DS	15	NA	LT1073
	DC to DC Converter Generates –24V from 3V or 5V	DN52	1	2	LT1173
	Positive to Negative Converter 5V to –5V/75mA	LT1111 DS	15	NA	LT1111
		LT1173 DS	13	NA	LT1173
	Voltage Controlled Positive-to-Negative Converter	LT1173 DS	15	NA	LT1173
		LT1111 DS	15	NA	LT1111, LT1006
Digital System Support	Memory Backup Supply	LT1073 DS	16	NA	LT1073
Dual Output	Single Li-Ion to ±5V Regulator	DN108	2	3	LT1373
Inverting, Positive-to-Negative	Positive (3.5–7.5V) to Negative (–5V) Converter	LTM V:1	12	10	LTC1265-5
	Positive to –5V/150mA Converter with Low-Battery Detection	LTM III:2	8	9	LTC1174-5
	Positive (4V to 7.5V In) to –5V/150mA Converter with Low Battery Detection	DN73	2	7	LTC1174-5
	Positive-to-Negative Converter with Direct Feedback	LT1373 DS	10	NA	LT1373
Isolated	5V Isolated Switching Power Supply	LTM V:2	27	1	LT1111, LTC1145, LT1121-5
	Isolated 5V/100mA Supply	AN66	42	76	LT1111, LTC1145, LT1121
Laser	1.5V Powered Laser Diode Driver	AN52	12	17	LT1110
		LT1110 DS	14	NA	
	LT1110 Single-Cell Laser-Diode Driver	LTM I:1	13	1	LT1110

Regulators—Switching (Micropower) (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
LCD Bias	1.8V–6V In, –4V to –29V Out, LCD Contrast Supply	AN65	114	J1	LT1300/LT1301
	3V In LCD Bias Generator	LTM II:3	17	1	LT1173
	DC/DC Converter Generates LCD Bias from 3V Supply	AN65	115	J2	LT1173
	Dual-Output LCD Bias Generator	AN66	62	128	LT1107
		AN65	115	J3	
		LTM III:3	27	1	
	LCD Bias Generator	LT1111 DS	14	NA	LT1111
		AN51	18	25	LT1173
		LT1173 DS	12	NA	
	LCD Bias Generator (3V to –12 to –24V)	LTM II:2	6	6	LT1173
	LCD Bias Generator (5V to –10 to –30V)	LTM II:2	7	7	LT1172
	LCD Bias Supply	AN66	63	129	LT1173
	LCD Power Supply	LTC1174 DS	13	NA	LTC1174
Multioutput	1.5V to 10V/3mA, 5V/3mA Dual Output Step-Up Converter	LT1110 DS	15	NA	LT1110
	Multioutput Power Supply (5V/400mA, 12V/60mA, –5V/50mA, and 28V/2mA) from 2 AA Cells	LTM III:1	20	1	LT1110
SEPIC	2 Li-Ion Cell to 5.8V/600mA DC/DC Converter	LT1302 DS	15	NA	LT1302
	2.7V–6V In, 3.3V/300mA Out SEPIC Converter	DN109	1	2	LT1372
	3-Cell to 3.3V Buck-Boost Converter with Auxiliary 12V Regulated Output	LT1302 DS	15	NA	LT1302, LT1121
	3-Cell to 3.3V/200mA SEPIC Converter	DN109	1	1	LT1303
	4 AA Cell to 3.3V or 5V/220mA DC/DC Converter	LTM III:3	14	11	LT1300
	4-Cell to 5V or 3.3V/220mA Converter	AN66	53	105	LT1300
	4-Cell to 5V Step-up/Step-Down Converter	LTM V:3	18	7	LT1304-5
	4-Cell to 5V/300mA SEPIC Converter	DN110	1	2	LT1372

Regulators—Switching (Micropower) (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
SEPIC (Continued)	4-Cell to 5V SEPIC Converter	AN66	55	114	LT1304-5
	4-Cell to 3.3V or 5V/220mA Converter	AN59	6	11	LT1300
	4-Cell to 5V/3.3V Up-Down Converter	LT1300 DS	8	NA	LT1300
	Single Li-Ion Cell to 3.3V SEPIC Converter	DN108	1	1	LT1373
	3-Cell to 3.3V Buck-Boost Converter with Auxiliary 12V Regulated Output	LTM IV:2	11	15	LT1302, LT1121
Single Cell	1.5V to 12V Step-Up Converter	LT1073 DS	13	NA	LT1073-12
	1.5V to 3V Step-Up Converter	LT1073 DS	12	NA	LT1073
	1.5V to 5V Bootstrapped Step-Up Converter	LT1073 DS	16	NA	LT1073-5
	1.5V to 5V Low Noise Step-Up Converter	LT1073 DS	17	NA	LT1073
	1.5V to 5V Step-Up Converter with Logic Shutdown	LT1073 DS	14	NA	LT1073
	1.5V to 5V Step-Up Converter with Low-Battery Detector	LT1073 DS	15	NA	LT1073-5
	1.5V to 5V Very Low Noise Step-Up Converter	LT1073 DS	17	NA	LT1073
	1.5V to 9V Step-Up Converter	LT1073 DS	12	NA	LT1073
	Single Cell to 5V Converter	LT1073 DS	1	NA	LT1073-5
"Super Burst"	Super Burst 2-Cell to 5V DC/DC Converter	LTM V:3	19	9	LT1304
Switched Capacitor	Generating –5V from 5V	LTC660 DS	1	NA	LTC660
	Positive Voltage Doubler	LTC660 DS	8	NA	LTC660
	Protected Negative Bias Generator for GaAsFET RF Amplifier	LTM III:2	24	1	LTC1044, LTC1153, LT1004
Synchronized	Clock-Synchronized 2V–4V In, 5V Out Switching Regulator	LTM IV:1	24	1	LT1107
	Clock-Synchronized 2V–4V to 5V Switching Regulator	AN66	50	95	LT1107
Telecom	Telecom Supply	LT1173 DS	13	NA	LT1173

Regulators—Switching (Micropower) (Continued)					
Category	**Subject**	**Publication**	**Page Number**	**Figure Number**	**LT Part Number(s)**
VPP Generator	Boost Mode Switching Regulator with Low R_{ON} Pass Transistor for Flash Memory Programming	AN66	65	132	LT1109A-12
	Inductorless VPP Generator	AN66	64	130	LTC1262
	3.3V or 5V to 12V/120mA Stepup Converter	LTM III:3	14	13	LT1301
	All-Surface Mount Flash-Memory VPP Generator	LTM I:2	16	1	LT1109-12

Relative Humidity (see Signal Conditioning, Humidity)

Sample and Hold (see Amplifiers, Sample and Hold)

Sensors/Transducers (see SIgnal Conditioning)

Settling Time (see Amplifiers, Settling Time)

Signal Conditioning

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Acceleration	Acceleometer Digitizer	AN7	15	16	LT1011, LT1056
	Accelerometer Amplifier with DC Servo	LT1169 DS	12	NA	LT1169
		AN67	70	105	LT1113
	Fast Piezoelectric Accelerometer	LT1022 DS	5	NA	LT1022
Acoustic	Low Noise Hydrophone Amplifier with DC Servo	LT1169 DS	11	NA	LT1169
Audio	Phono Preamplifier	LT1007 DS	11	NA	LT1037
	Tape Head Amplifier	LT1007 DS	11	NA	LT1037
Barometric Pressure	Single-Cell Barometer	AN67	48	62	LT1077, LT1110, LT1004
Bridge	A Practical Instrumentation-Amplifier-Based Bridge Circuit	AN43	5	5	LT1021, LT1010, LT1078
	Amplifier for Bridge Transducer	LM108 DS	6	NA	LM108
		LT1008 DS	9	NA	LT1008
		LT1012 DS	10	NA	LT1012
	Differential Voltage Amplification from a Resistance Bridge	LT1101 DS	11	NA	LT1101
	Floating Input Bridge Instrumentation Amplifier with 200V Common Mode Range	AN43	10	13	LTC1150
	Gain Trimming by Adjustment of Transducer Excitation	DN51	1	2	LT1027, LT1097, LT1010
	High Precision Scale for Human Subjects	AN43	8	11	LT1010, LT1012, LT1018, LT1021, LTC1043, LTC1150
	High Resolution Bridge Amplifier with Common Mode Suppression	AN43	7	10	LT1054, LT1078
	High Resolution Pulsed Excitation Bridge Signal Conditioner	AN43	23	25	LT1007, LT1012, LT1018, LTC1150
	Low Noise Bridge Amplifier with Common Mode Suppression	AN43	6	7	LT1007, LT1028
	Low Noise, Chopper-Stabilized Bridge Amplifier with Common Mode Suppression	AN43	6	8	LT1007, LT1021-5, LT1028, LTC1150

Signal Conditioning (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Bridge (Continued)	Low Power Bridge Driver	AN43	18	19B	LT1078, LT1101
	Marrying Gain and Balance	AN43	NA	NA	NA
	Pulsed Excitation Bridge Signal Conditioner—DC Output	AN43	21	23	LT1077, LT1021, LT1101
	Pulsed Excitation, Sampled Output Bridge Signal Conditioner	AN43	20	21	LT1078, LT1101
	Servo Controlling Bridge Drive Eliminates Common Mode Voltage	AN43	5	6	LTC1150
	Single-Supply Bridge Amplifier with Common Mode Suppression	AN43	7	9	LTC1044, LT1078
	Strobed Power Strain-Gauge Bridge Signal Conditioner	AN43	19	20	LT1054, LT1078
	Time Domain Bridge	AN43	27	31	LT1011
Current-Loop Transmitter	Optoisolated 4mA–20mA Process Controller	LTM V:1	16	4	LTC1453, LT1121-3.3, LT1077
Distance	Linear Variable Differential Transformer (LVDT)	LTC1043 DS	15	NA	LT1004, LT1011, LT1013, LTC1043
		LT1013 DS	16	NA	
		AN3	9	10	LT1011, LT1013, LTC1043
Flow	Air Flow Detector	LT1012 DS	11	NA	LT1012
		LTC1052 DS	13	NA	LTC1052, LT1004
	Hot Wire Anemometer	LT1013 DS	10	NA	LT1014
	Liquid Flowmeter	AN5	6	8	LT1002, LT1011, LT1012
		LT1013 DS	10	NA	LT1014, LT1004
	Thermal Anemometer	AN5	7	11	LT1002, LM107
Gas	Linearized Methane Transducer	AN11	3	2	LT1014, LTC1044
	Methane Concentration Detector with Linearized Output	LT1013 DS	13	NA	LT1014, LTC1044, LT1004
Humidity	Battery Powered Relative Humidity Signal Conditioner	AN45	10	15	LTC1043, LT1006

Signal Conditioning (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Humidity (Continued)	Humidity Sensor	LTM V:2	23	1	LTC1043, LTC1046, LTC1050, LTC1250
	Humidity to Frequency (0%–100% to 0Hz–1000Hz)	AN7	11	11	LTC1043, LT1056, LT1011
	Humidity Sensor Circuit	AN67	46	60	LTC1046, LTC1050, LTC1250, LTC1043
	Relative Humidity	AN3	8	9	LTC1043, LT1056, LM301A, LT1004-1.2
		AN3	7	8	LTC1043, LT1056, LT1009-2.5
		LTC1043 DS	14	NA	LTC1043, LT1056, LM301A, LT1004-1.2
	System Monitor for Relative Humidity, Supply Voltage and Ambient Temperature	LTC1392 DS	9	NA	LTC1392, LTC1043, LT1056, LM301A, LT1004
Infrared	Infrared Detector Preamplifier	LT1007 DS	11	NA	LT1007
	Low Noise Infrared Detector	LT1028 DS	16	NA	LT1028, LTC1043, LM301A, LT1012
Level	Bar Graph Level Gauge	LTC1443–45 DS	1	NA	LTC1443
	Level to Frequency	AN7	13	14	LT319A, LT1056, LTC1043, LM301A
	Level Transducer Digitizer Uses AC Bridge Technique	AN43	26	29B	LT1018, LT1057, LT1102
Light	Discriminator Circuit with Low Battery Detect for 3V Flame Alarm	LTM III:3	18	3	LT1179, LT1004
	Flame Detector	AN59	8	15	LT1300
		LTM III:3	17	1	LT1300
	Light Stick Controller	AN59	11	19	LT1178
		LTM III:3	20	7	LT1178
	Low Noise Light Sensor with DC Servo	LT1169 DS	1	NA	LT1169
Particle Detector	1.5V Powered Particle detector	LT1073 DS	19	NA	LT1073

Signal Conditioning (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Photoconductive Cell	Buffer for Photoconducting Cell	LM134 DS	10	NA	LM334
Photodiode	A Simple Fiber Optic Receiver	AN47	43	95	LT1016, LT1220
	A Simple Photodiode Amplifier	AN47	41	90	LT1122
	A Very Fast Photo Integrator	AN47	42	93	LT1122
	Adaptively Triggered 40MHz Fiber Optic Receiver	AN47	44	97	LT1016, LT1097, LT1220, LT1223
	Amplifier for Photodiode Sensor	LT1008 DS	9	NA	LT1008
		LT1012 DS	10	NA	LT1012
		LTC1150 DS	10	NA	LTC1150
	Fast Fiber Optic Receiver (10MHz)	AN13	23	38	LT1012, LT1016
	IR LocalTalk Infrared Receiver	DN118	2	2	LT1319
	Light Level Sensor	LM10 DS	12	NA	LM10
	Logarithmic Photodiode Amplifier 100dB Range	AN5	3	4	LT1012, LM107, LM301A
		LT1057 DS	11	NA	LT1057, LT1021, LM301A
	Photodiode Amplifier	LT1215/16 DS	16	NA	LT1216
	Photodiode Current-to-Voltage Converter	LTM V:2	16	1	LT1311
	Photodiode Preamp with AC-Coupling Loop	LT1360 DS	11	NA	LT1360, LT1358
	Photodiode, Frequency Output (20Hz–2MHz)	AN7	9	8	LT1011, LT1021-10, LT1056
	PIN Photodiode to Frequency Converter	LT1022 DS	6	NA	LT1022, LT1011, LM329
Piezoelectric	Amplifier for Piezoelectric Transducer	LM108 DS	6	NA	LM108
Pressure	1.5V Powered Barometric Pressure Signal Conditioner	AN61	11	15	LT1110, LT1078, LT1101, LT1004
	1.5V Powered Barometric Pressure Signal Conditioner Eliminates Instrumentation Amp	AN61	12	16	LT1110, LT1077, LT1004
	3.3V Powered, Digital-Output, Barometric Pressure Signal Conditioner	AN61	9	13	LT1172, LT1287, LT1078, LT1101, LTC1043
	Direct Pressure Transducer to Digital Output Signal Conditioner	LT1024 DS	7	NA	LT1024, LT137A

Signal Conditioning (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Pressure (Continued)	Precision Barometer	AN45	11	16	LT1027, LT1078, LT1101
	Single-Cell Barometer	LTM IV:1	22	1	LT1110, LT1077, LT1004
	Single-Supply, Barometric-Pressure Signal Conditioner	AN61	10	14	LT1172, LT1078, LT1101, LT1034
Radiation Detector	Single-Cell Radiation Detector	AN45	11	17	LT1073
Strain Gauge	12-Bit LTC1296 Data-Acquisition System Strain Gauge with Bridge-Driver Power Shutdown	AN62	16	23	LTC1296, LT1014
	9V Battery Powered Strain Gauge Signal Conditioner	LT1013 DS	11	NA	LT1014
	Differential Bridge Amplifier	LTC1250 DS	1	NA	LTC1250
	Differential Voltage Amplification from a Resistance Bridge	LT1101 DS	11	NA	LT1101
	Direct 10-Bit Strain Gauge Digitizer	LTC1052 DS	17	NA	LTC1052, LM301A, LTC1043
	Sampled Strain Gauge Bridge	AN23	3	3	LT1006, LT1021
	Strain Gauge Bridge Signal Conditioner	LT1054 DS	11	NA	LT1054, LT1013
		LT1013 DS	15	NA	LT1013, LT1004-1.2, LTC1044
	Strain Gauge Conditioner for 350Ω Bridge	LT1236 DS	10	NA	LT1236, LM301A, LT1012
		LT1031 DS	9	NA	LT1031-10, LM301A, LT1012C
		LT1021 DS	12	NA	
	Strain Gauge Signal Conditioner	AN11	7	7	LTC1044, LT1013
		LTC1044 DS	10	15	LTC1044, LT1013, LT1004-1.2
	Strain Gauge Signal Conditioner with Bridge Excitation	LT1002 DS	1	NA	LT1001, LT1002, LM329
		LT1001 DS	8	NA	LT1001, LM329
		LT1007 DS	11	NA	LT1007, LT1009

Signal Conditioning (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Strain Gauge (Continued)	Strain Gauge Frequency Output	AN7	6	6	LTC1043, LTC1052
	Strobed Power Strain Bridge	AN23	4	5	LT1013, LT1054
	Ultralinear Strain Gauge	LT1019 DS	1	NA	LT1019-5, LT301A, LT1001
		REF02 DS	1	NA	REF-02, LT307, LT1001
Weight	Weight Scale	AN62	6	7	LTC1092, LT1013

Signal Conditioning—Temperature

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Acoustic	Acoustic Thermometer	AN7	5	4	LT1056, LT1011, LM307
Discussion	Error Sources in Thermocouple Systems	AN28	18	NA	NA
	Linearization Techniques for Thermocouples	AN28	12	NA	NA
	Temperature Sensor Comparison	AN28	2	NA	NA
	Thermal Control Loop Model	AN5	2	1	LT1056
	Thermocouple Measurement	AN28	1	NA	NA
Platinum RTD	0°C–400°C Temperature Measurement System	AN52	2	1	LT1006, LT1027, LTC1292
		LTM II:1	20	1	
	5V Powered, Linearized Platinum RTD Signal Conditioner (0°C–400°C to 0V–4V)	AN11	1	1	LT1014, LT1009
		LT1013 DS	15	NA	
	Digitally Linearized Platinum RTD Signal Conditioner	AN62	10	14	LTC1294, LT1101, LT1006, LT1027
		AN43	13	16	LT1101, LTC1290, LTC1027, LT1006
		DN45	1	1	LT1078, LT1101
	Kelvin Sensed Platinum Temperature Sensor Amplifier	LT1012 DS	10	NA	LT1012
	Linearized Platinum Resistance Thermometer	LT1001 DS	1	NA	LT1001, LM129

Signal Conditioning—Temperature (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Platinum RTD (Continued)	Linearized Platinum RTD Bridge	DN40	2	6	LT1078, LT1101
		AN43	11	14	
	Linearized Platinum RTD Signal Conditioner (2°C–400°C to 0.2V–4V)	LT1006 DS	10	NA	LT1006, LM334
		AN23	1	1	LT1006, LM334
	Linearized Platinum RTD, Precision	LTC1051 DS	14	NA	LTC1051, LTC1043, LT1009-2.5
		LTC1043 DS	12	NA	LT1013, LTC1043, LT1009-2.5
		AN3	6	7	LT1013, LTC1043
	Platinum Resistor Value to Frequency (0kHz–1kHz)	AN14	17	23	LT1056, LT1011, LTC1043
	Switched Capacitor Based RTD Signal Conditioner	AN43	12	15	LT1078, LTC1043
	Ultralinear Platinum Temperature Conditioner	LT1236 DS	11	NA	LT1236-10, LT1001
	Ultralinear Platinum Temperature Sensor	LT1021 DS	13	NA	LT1021-10, LT1001
		LT1031 DS	10	NA	LT1031, LT1001
Quartz Crystal	Quartz Crystal Based Thermometer	AN61	13	17	LTC485
Silicon Sensor	0°C–70°C Thermometer	AN52	5	5	LTC1096, LT1004-1.2
	0°C–70°C Temperature Measurement System	LTM II:1	11	9	LTC1096, LM134, LT1004
	Centigrade Temperature Sensor with 2-Point Trim	LM134 DS	7	4	LM134-3, LT1009
	Delta V_{BE} Based Thermometer	AN45	7	11	LTC1043, LTC1150
	Differential Temperature Measurement System	LTM II:1	21	3	LTC1292, LT1027, LM134
		AN52	3	3	LTC1292, LT1027
	Ground-Referred Fahrenheit Thermometer	LM134 DS	11	NA	LM334, LT1009
	High Noise Rejection Thermometer	AN9	17	27	LTC1052
	Isolated Temperature Sensor	LF198 DS	13	NA	LF398, LM301, LM135
	Low Output Impedance Thermometer	LM134 DS	9	NA	LM334

Signal Conditioning—Temperature (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Silicon Sensor (Continued)	Low Output impedance Thermometer (Kelvin Output)	LM134 DS	8	NA	LM334
	Micropower, Battery Operated, Remote Temperature	LT1101 DS	11	NA	LT1101, LM134-3, LT1004-1.2
	Remote Temperature Sensor with Voltage Output	LM134 DS	1	NA	LM234-3
	Temperature to Frequency Converter	LT1055 DS	10	NA	LT1055, LM134, LM329
	Temperature to Frequency Converter (0°C–100°C to 0kHz–1kHz)	AN7	2	1	LT1056
	Thermometer Using Current Output Silicon Sensors (–55°C–125°C)	DN5	2	3	LTC1092, LT1019-2.5
Thermistor	"Lock-In" Bridge Amplifier for Thermistor	AN43	24	27	LT1007, LT1057, LT1011, LTC1043
	0°C–100°C Linear Output Thermometer	LT1004 DS	5	NA	LT1004-1.2, LT1002
	0°C–500°C Furnace Exhaust Gas Temperature Measurement System with Low Supply Detection	AN62	11	15	LTC1091A, LTC1052, LT1019A, LT1025A
	2-Wire 0°C Temperature Transducer with 4mA to 20mA Output	LTC1040 DS	11	NA	LTC1040, LM134, LT1019-5
	Accurate Thermistor Based Temperature Measurement System (0°C–100°C)	DN5	2	2	LTC1090, LT1006
	Complete Heating/Cooling Automatic Thermostat	LTC1040 DS	9	NA	LTC1040
	Freezer Alarm	AN23	7	8	LTC1042
	Linear Output Thermistor Bridge	AN43	17	18	LT1006, LT1101
	Linear Thermometer, Thermistor	AN3	15	22	LT1004, LT1013, LTC1043
		LT1006 DS	11	NA	LTC1043, LT1004, LT1006
	Precision Temperature Controller	AN5	1	1	LT1012, LT3525A
	Thermistor Based Current Loop Signal Conditioner (0°C–100°C)	AN23	5	6	LTC1040
	Ultralow Power 50°F–100°F Thermostat	LTC1041 DS	1	NA	LTC1041
	Wall-Type Thermostat	AN23	6	7	LTC1041

Signal Conditioning—Temperature (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Thermocouple	±15V Dual Thermocouple Amplifier	LTC1151 DS	1	NA	LTC1151, LT1025
	12-Bit, Single 5V Temperature Control System with Shutdown	LTM III:3	15	6	LTC1257, LTC1297, LT1025, LTC1050
		AN67	8	7	LTC1257, LTC1297, LTC1050, LT1025A
	3-Channel Thermocouple Thermometer	LT1013 DS	1	NA	LT1014, LT1004-1.2
	Breakpoint-Based Linearization for Thermocouples	AN28	14	21	LT1014, LT1025
	Cold Junction Compensation for a Type K Thermocouple	LTK001 DS	1	NA	LT1025, LTKA0x
		AN28	5	10	LT1025
	Cold Junction Compensation for a Type J Thermocouple	AN28	4	9	LT1025, LT1001
	Continuous Function Linearization for Thermocouples	AN28	15	22	LT1025, LT1097
	Differential Thermocouple Amplifiers	LTC1250 DS	8	NA	LTC1250, LT1025
		AN28	6	12A	LTC1043, LT1025
	Direct Thermocouple-to-Frequency Converter	LTC1052 DS	17	NA	LTC1052, LTC1043, LT1004
	Flame Detector	LM10 DS	13	NA	LM10
	Furnace Exhaust Gas Temperature Monitor with Low Supply Detection (0°C–500°C)	DN5	1	1	LTC1091, LT1025, LT1019A-5, LTC1052
	Isolated Temperature-to-Frequency Converter	AN67	20	22	LT1025, LTC1049, LTC1146, LT1004-1.2, LTC201
		LTM III:1	4	4	
	Isolated, Battery Powered, Temperature-to-Frequency Converter	LTC1145/46 DS	9	NA	LTC1146, LTC201, LT1025, LTC1049, LT1004
	Low Noise, Multiplexed Thermocouple Amplifier	OP27 DS	1	NA	OP27
	Micropower Cold Junction Compensation for Thermocouple	LT1004 DS	1	NA	LT1004-1.2
	Micropower Thermocouple Temperature to Frequency Converter	LTC203 DS	10	NA	LTC203, LT1025, LTC1049, LT1004

Signal Conditioning—Temperature (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Thermocouple (Continued)	Multiplexed Differential Thermometer	LTC1053 DS	13	NA	LTC1053, LT1025A
	Offset Based Linearization for Thermocouples	AN28	12	20	LT1025, LTC1052
	Optoisolated Temperature Monitor	LTC1292 DS	19	24	LTC1292, LT1019-2.5, LT1025-A, LTC1050
		AN62	13	18	
	Precision Multiplexed Differential Thermocouple Amplifier	LTC1052 DS	16	NA	LTC1052, LT1004, LTC1043
	Processor-Based Linearization for Thermocouples	AN28	15	23	LT1019A-5, LT1025A, LTC1052, LTC1091A
	Pulse Width Output Thermocouple Isolator	AN28	11	17	LT1006, LT1017, LT1025
	Single +5V Thermocouple Amplifier with Cold Junction Compensation	AN11	5	5	LTC1052, LTC1043, LT1004-1.2
		LTC1052 DS	15	NA	
	Single 5V Thermocouple Overtemperature Alarm	LTC1042 DS	6	NA	LTC1043, LT1034, LTC1052, LTC1042
	Single-Supply Thermocouple Amplifier	LTC1049 DS	1	NA	LTC1049, LT1025A
	Thermocouple Based Temperature-to-Frequency Converter	LTC1049 DS	7	NA	LTC1049, LTC201, LT1025, LT1004
	Thermocouple Cold Junction Compensator	LM185-2.5 DS	1	NA	LM385-2.5, LM334
	Thermocouple Isolation Amplifier (0.01%)	AN28	10	15	LT1013, LT1018, LT1025
	Thermocouple Isolation Amplifier (0.25%)	AN28	8	13	LT398A, LT1013, LT1025
	Thermocouple-Sensed Temperature to Frequency Converter	AN45	8	13	LT1025, LTC1049
	Cold Junction Compensated Thermocouple Signal Conditioner	AN11	5	5	LTC1052, LTC1043
	Thermocouple-to-Frequency Converter (0°C–60°C to 0Hz–600Hz)	AN7	3	2	LTC1052, LTC1043
	Thermocouple Transmitter	LM10 DS	13	NA	LM10, LM134
	Thermocouple with Cold Junction Compensation (0°C–60°C)	LT1006 DS	11	NA	LT1006, LT1034

Signal Processing

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Driver	Oscillator Buffer Drives +17dBm to +27dBm Double Balanced Mixers	AN67	86	143	LT1206
Pulse Detector	Fast Pulse Detector	AN67	76	122	LT1190

Sine Wave Generator (see Oscillators, Sine Wave)

Single Cell

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
A/D	1.5V A/D Converter (10-Bit)	AN15	2	3	LT1018
Amplifier	1.5V Voltage Boosted Output Op Amp (0V–10V)	AN15	6	11	LM10
DC/DC	Boost Regulator (1.5V to 5V)	AN15	7	13	LT1018
Discussion	Components for 1.5V Operation	AN15	8	NA	NA
Oscillator	1.5V Temperature-Compensated Crystal Oscillator	AN15	6	9	LM10
		AN45	14	20	LT1073, LT1017, LM134-3
		LT1073 DS	19	NA	
Sample and Hold	1.5V Fast Sample and Hold (125µs, 0.1%)	AN15	4	7	LM10, LT1018
	1.5V Sample and Hold	AN15	3	6	
Single Cell: V/F	1.5V Voltage to Frequency Converter (0V–1V to 1Hz-1kHz)	AN14	9	12	LT1017
	1.5V Voltage to Frequency Converter (0V–1V to 25Hz–10kHz)	AN15	1	1	LT1018

Single-Supply

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Analog Switch	Low Charge Injection Analog Switch	LTC201 DS	1–12	NA	LTC201, LTC202, LTC203
Current Loop	Digitally Controlled 4mA–20mA Current Loop Generator	AN31	6	11	LT1072, LT1006
Digital Help Circuits	EEPROM Pulse Generator	LT1013 DS	12	NA	LT1013
Discussion	High Performance Single-Supply Analog Amplifiers	AN11	14	NA	NA
Filter—Switched Capacitor	6th Order LP Butterworth	LTC1061 DS	8	5	LTC1061
	Level Shifting TTL Clock for V^+ >6V	LTC1064-1 DS	5	3	LTC1064-1
	Single 5V Supply 5th Order LP Filter	LTC1062 DS	10	NA	LTC1062
	Single 5V, Gain of 1000, 4th Order Bandpass Filter	LTC1060 DS	1	NA	LTC1060
	Single-Supply LTC1062	AN20	4	7	LTC1062
	Single-Supply Operation of LTC1064-1	LTC1064-1 DS	5	2	LTC1064-1
Gas Sensor	Linearized Methane Transducer Signal Conditioner	AN11	3	2	LT1014, LTC1044
Instrumentation Amplifier	Precision Instrumentation Amplifier	AN11	6	6A	LT1014
	Precision, Micropower, Single-Supply Instrumentation Amplifier	LT1101 DS	1–12	NA	LT1101
	Two Op Amp Instrumentation Amplifier	LTC1049 DS	7	NA	LTC1049
	Ultraprecision Instrumentation Amplifier	AN11	6	6B	LTC1043, LTC1052
		LTC1043 DS	10	6B	
Interface	A/D Converter Interface	DN29	1	1	LTC1094, LT1180, LT1021-5
Motor Speed	Motor Speed Controller, No Tachometer Required	LT1013 DS	12	NA	LT1013
Oscillator	Single-Supply Crystal Oscillator 10MHz–15MHz	LT1116 DS	6	2	LT1116
Sample and Hold	Quad Single 5V Supply, Low Hold Step, Sample and Hold	LTC1043 DS	12	NA	LTC1043, LT1014

Single-Supply (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Signal Conditioning	Photodiode Amplifier	LT1215/16 DS	16	NA	LT1216
Strain Gauge	Strain Gauge Bridge Signal Conditioner	LT1054 DS	11	NA	LT1054, LT1013
	Strain Gauge Signal Conditioner	AN11	7	7	LT1013, LTC1044, LT1034
		LTC1044 DS	10	15	LT1013, LTC1044, LT1004
Temperature Sensor	Cold Junction Compensated Thermocouple Signal Conditioner	AN11	5	5	LTC1043, LTC1052
	Linearized Platinum RTD Signal Conditioner (0°C–400°C)	AN11	1	1	LT1014, LT1009
	Single 5V Thermocouple Overtemperature Alarm	LTC1042 DS	6	NA	LTC1042, LTC1043, LTC1052, LTC1034
	Single-Supply Precision Linearized Platinum RTD Signal Conditioner	AN3	6	7	LTC1043, LT1013, LT1009
	Single-Supply Precision Linearized Platinum RTD Signal Conditioner	LTC1043 DS	12	NA	LTC1043, LT1013, LT1009
Transmitter	4mA–20mA Current Loop Transmitter	AN11	9	10	LT1013, LT1004
	4mA–20mA Digitally Controlled Current Loop Transmitter	AN31	6	11	LT1072, LT1006, LT1004
	4mA–20mA Floating Output for Current Loop Transmitter	AN11	10	11	LT1013
Single-Supply: V/F	Ultralinear Voltage to Frequency Converter (100kHz–1.1MHz)	AN14	7	10	LTC1043, LT1013, LT1004
	Ultralinear Voltage to Frequency Converter (100kHz–1.1MHz)	AN23	13	21	LT1006, LM334, LT1004-1.2, LT1004-2.5
	Ultralinear, Micropower V/F (0–5V to 0–10kHz)	AN45	15	21	LT1017, LM334, LT1034
	Voltage to Frequency Converter	LTC1040 DS	11	NA	LTC1040
Voltage Regulator	Low Dropout 5V Regulator	LM10 DS	10	NA	LM10

Strain Gauge (see Signal Conditioning, Strain Gauge)

Switches

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Analog	Low Charge Injection Analog Switch	LTC201 DS	1–12	NA	LTC201, LTC202, LTC203
High-Side	0.85A Protected Switch	LTC1477/78 DS	7	NA	LTC1477
	1.5A Protected Switch	LTC1477/78 DS	6	NA	LTC1477
	2A Protected Switch	LTC1477/78 DS	6	NA	LTC1477
	2A Protected Switch Driving a Capacitive Load	LTC1477/78 DS	7	NA	LTC1477
	5v to 3.3V Selector Switch with Slope Control and 0.01µA Standby Current	LTC1477/78 DS	7	NA	LTC1478
	High-Side Switch (1.5A)	LT1188 DS	1–8	NA	LT1188
	Isolated High-Side Switch	LTC1177 DS	1	NA	LTC1177
	Isolated High-Side Switch with Foldback Current Limit	LTC1177 DS	5	NA	LTC1177
	LTC1477 Controlled by the LTC1304's Low-Battery Detector	DN117	2	4	LTC1477, LT1304
	Short-Circuit Protection and 100% Shutdown for a Micropower Boost Regulator	DN117	2	3	LTC1477, LT1301
	Switched 5V Line with Undervoltage Lockout	DN117	1	2	LTC1477, LTC699

Telecommunications

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
HDSL	LT1206 Used as a Differential HDSL Transformer Driver	LTM V:1	27	4a	LT1206
	LT1206 Used as Single-Ended HDSL Transformer Driver	LTM V:1	28	4b	LT1206
ISDN	Power Supply for Subscriber Line Interface Circuit	DN130	1	1	LT1171, LT1006

Telecommunications (Continued)

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
ISDN (Continued)	Power Supply for Subscriber Line Interface Circuit	DN130	2	2	LT1269, LT1006
Ring-Tone Generator	Complete Ring-Tone Generator Circuit	DN134	2	4	LT1491
	High Voltage Power Supply for Ring-Tone Generator	AN67	60	83	LT1070
	Ring-Tone Generator	AN67	60	82	LT1078, LT1004

Thermal Analysis

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
	SimpleThermal Analysis—a Real Cool Subject for LTC Regulators	AN66	98	NA	See Text

Thermistor (see Signal Conditioning—Temperature, Thermistor)

Thermocouple (see Signal Conditioing—Temperature, Thermocouple)

Thermometer (see Signal Conditioning—Temperature)

Trigger

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Adaptive Threshold	50MHz Trigger with Adaptive Threshold	AN47	59	130	LT1016, LT1097, LT1222

VCO (see Oscillators)

Video (see Amplifiers, Video; Multiplexers, Video)

Voltage

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
Source	5V, ±0.4% Tolerance, ±1A Low Noise Voltage Source	LTM V:4	4	6	LT1166, LT1431
	High Voltage RMS Calibrator	AN65	71	C13	LT1172, LT1006

Voltmeter

Category	Subject	Publication	Page Number	Figure Number	LT Part Number(s)
RMS	Wideband True RMS Voltmeter	AN47	62	137	LT1013, LT1088, LT1223, LT1004
	Single-Supply, AC-Coupled, RMS Calibrated AverageDetector	LT1215/16 DS	16	NA	LT1216

Wein Bridge Oscillator (see Oscillators)

SECTION 1: APPLICATION NOTES

SECTION 1—APPLICATION NOTES

Techniques for 92% Efficient LCD Illumination

Waste Not, Want Not . . .

Jim Williams

INTRODUCTION

In August of 1992 LTC published Application Note 49, "Illumination Circuitry for Liquid Crystal Displays." One notable aspect of this event is that it generated more response *than all previous LTC application notes combined.* This level of interest, along with significant performance advances since AN-49's appearance, justifies further discussion of LCD backlighting circuitry.

This publication includes pertinent information from the previous effort in addition to updated sections and a large body of new material. The partial repetition is a small penalty compared to the benefits of text flow, completeness and time efficient communication. The most noteworthy performance advance is achievement of 92% efficiency for the backlight power supply. Additional new benefits include low voltage operation, synchronizing capability, higher output power for color displays, and extended dimming range.

A practical 92% efficient LCD backlight design is a classic study of compromise in a transduced electronic system. Every aspect of the design is interrelated, and the physical embodiment is an integral part of the electrical circuit. The choice and location of the lamp, wires, display housing and other items has a major effect on electrical characteristics. The greatest care in every detail is required to achieve a practical high efficiency LCD backlight. Getting the lamp to light is just the beginning!

Current generation portable computers and instruments utilize back-lit liquid crystal displays (LCDs). These displays have also appeared in applications ranging from medical equipment to automobiles, gas pumps and retail terminals. Cold Cathode Fluorescent Lamps (CCFLs) provide the highest available efficiency for backlighting the display. These lamps require high voltage AC to operate, mandating an efficient high voltage DC-AC converter. In addition to good efficiency, the converter should deliver the lamp drive in the form of a sine wave. This is desirable to minimize RF emissions. Such emissions can cause interference with other devices, as well as degrading overall operating efficiency. The sine wave excitation also provides optimal current-to-light conversion in the lamp. The circuit should also permit lamp intensity control from zero to full brightness with no hysteresis or "pop-on."

The LCD also requires a bias supply for contrast control. The supply's output should be regulated, and variable over a considerable range.

The small size and battery powered operation associated with LCD equipped apparatus mandate low component count and high efficiency for these circuits. Size constraints place severe limitations on circuit architecture and long battery life is usually a priority. Laptop and hand held portable computers offer an excellent example. The CCFL and its power supply are responsible for almost 50% of the battery drain. Additionally, these components, including PC board and all hardware, usually must fit within the LCD enclosure with a height restriction of 0.25".

Cold Cathode Fluorescent Lamps (CCFLs)

Any discussion of CCFL power supplies must consider lamp characteristics. These lamps are complex transducers, with many variables affecting their ability to convert electrical current to light. Factors influencing conversion efficiency include the lamp's current, temperature, drive waveform characteristics, length, width, gas constituents and the proximity to nearby conductors.

These and other factors are interdependent, resulting in a complex overall response. Figures 1 through 4 show some typical characteristics. A review of these curves hints at the difficulty in predicting lamp behavior as operating conditions vary. The lamp's current and temperature are

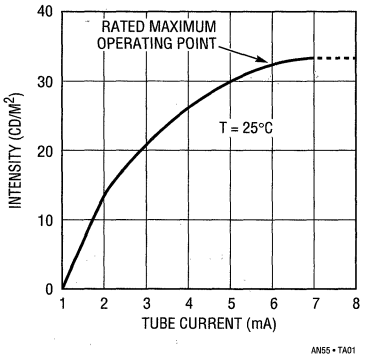


Figure 1. Emissivity for a Typical 6mA Lamp. Curve Flattens Badly Above 6mA

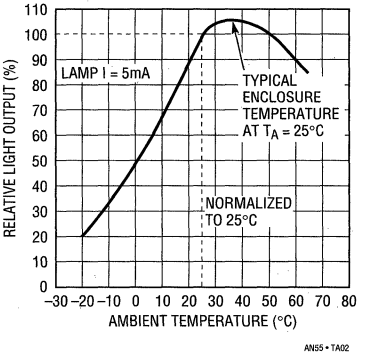


Figure 2. Ambient Temperature Effects on Emissivity of a Typical 5mA Lamp. Lamp and Enclosure Must Come to Thermal Steady State Before Measurements are Made

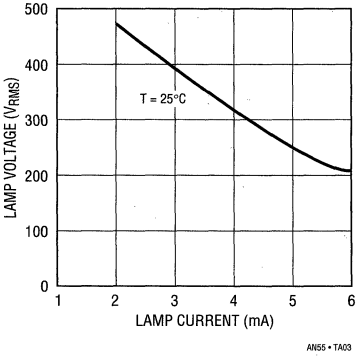


Figure 3. Current vs Voltage for a Lamp in the Operating Region

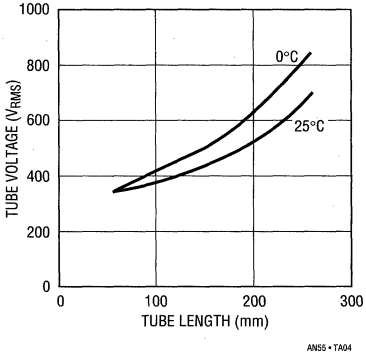
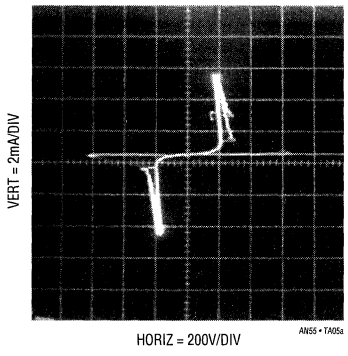


Figure 4. Running Voltage vs Lamp Length at Two Temperatures. Start-Up Voltages are Usually 50% to 200% Higher Over Temperature

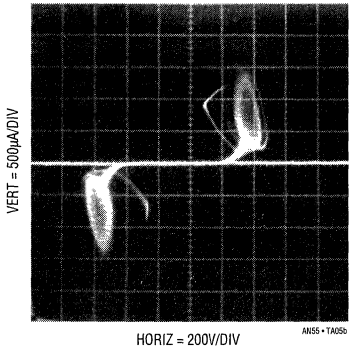
clearly critical to emission, although electrical efficiency may not necessarily correspond to the best optical efficiency point. Because of this, both electrical and photometric evaluation of a circuit is often required. It is possible, for example, to construct a CCFL circuit with 94% electrical efficiency which produces less light output than an approach with 80% electrical efficiency (see Appendix J, "A Lot of Cut-Off Ears and No Van Goghs—Some Not-So-Great Ideas." Similarly, the performance of a very well matched lamp-circuit combination can be severely degraded by a lossy display enclosure or excessive high voltage wire lengths. Display enclosures with too much conducting material near the lamp have huge losses due to capacitive coupling. A poorly designed display enclosure can easily degrade efficiency by 20%. High voltage wire runs typically cause 1% loss per inch of wire.

CCFL Load Characteristics

These lamps are a difficult load to drive, particularly for a switching regulator. They have a "negative resistance" characteristic; the starting voltage is significantly higher than the operating voltage. Typically, the start voltage is about 1000V, although higher and lower voltage lamps are common. Operating voltage is usually 300V to 400V, although other lamps may require different potentials. The lamps will operate from DC, but migration effects within the lamp will quickly damage it. As such, the waveform must be AC. No DC content should be present.



5A



5B

Figure 5. Negative Resistance Characteristic for Two CCFL Lamps. "Snap-Back" is Readily Apparent, Causing Oscillation in 5B. These Characteristics Complicate Power Supply Design

Figure 5A shows an AC driven lamp's characteristics on a curve tracer. The negative resistance induced "snap-back" is apparent. In Figure 5B another lamp, acting against the curve tracer's drive, produces oscillation. These tendencies, combined with the frequency compensation problems associated with switching regulators, can cause severe loop instabilities, particularly on start-up. Once the lamp is in its operating region it assumes a linear load characteristic, easing stability criteria. Lamp operating frequencies are typically 20kHz to 100kHz and a sine-like waveform is preferred. The sine drive's low harmonic content minimizes RF emissions, which could cause interference and efficiency degradation.[1] A further benefit to the continuous sine drive is its low crest factor and controlled rise times, which are easily handled by the CCFL. CCFL's RMS current-to-light output efficiency is degraded by fast rise high crest factor drive waveforms.[2]

CCFL Power Supply Circuits

Figure 6's circuit meets CCFL drive requirements. Efficiency is 88% with an input voltage range of 4.5V to 20V. This efficiency figure can be degraded by about 3% if the LT1172 V_{IN} pin is powered from the same supply as the main circuit V_{IN} terminal. Lamp intensity is continuously and smoothly variable from zero to full intensity. When power is applied the LT1172 switching regulator's feedback pin is below the device's internal 1.2V reference, causing full duty cycle modulation at the V_{SW} pin (Trace A, Figure 7). L2 conducts current (Trace B) which flows from L1's center tap, through the transistors, into L2. L2's current is deposited in switched fashion to ground by the regulator's action.

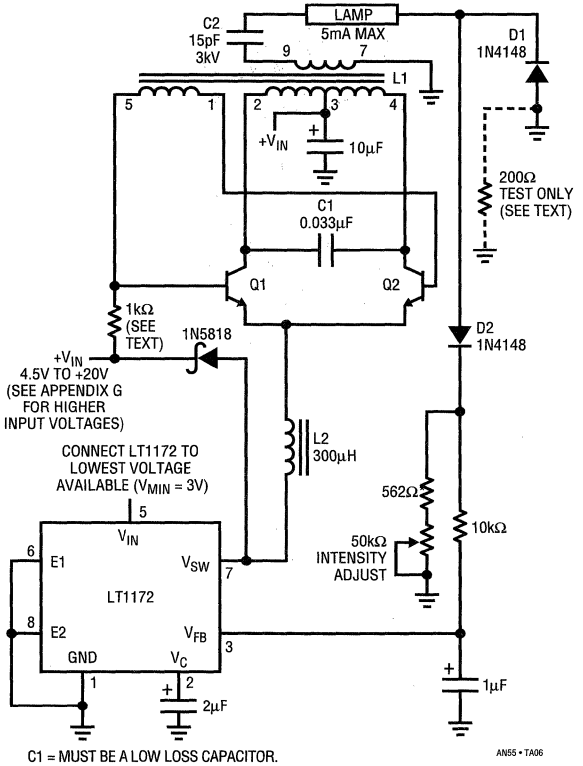
L1 and the transistors comprise a current driven Royer class converter[3] which oscillates at a frequency primarily set by L1's characteristics (including its load) and the 0.033μF capacitor. LT1172 driven L2 sets the magnitude of the Q1-Q2 tail current, hence L1's drive level. The 1N5818 diode maintains L2's current flow when the LT1172 is off. The LT1172's 100kHz clock rate is asynchronous with respect to the push-pull converter's (60kHz) rate, accounting for Trace B's waveform thickening.

The 0.033μF capacitor combines with L1's characteristics to produce sine wave voltage drive at the Q1 and Q2 collectors (Traces C and D respectively). L1 furnishes voltage step-up, and about $1400V_{P-P}$ appears at its secondary (Trace E). Current flows through the 15pF capacitor into the lamp. On negative waveform cycles the lamp's current is steered to ground via D1. Positive waveform cycles are directed, via D2, to the ground referred 562Ω-50k potentiometer chain. The positive half-sine appearing across the resistors (Trace F) represents 1/2 the lamp

Note 1: Many of the characteristics of CCFLs are shared by so-called "Hot" cathode fluorescent lamps. See Appendix A, "Hot" Cathode Fluorescent Lamps.

Note 2: See Appendix J. "A Lot of Cut-Off Ears and No Van Goghs—Some Not-So-Great Ideas."

Note 3: See Appendix I, "Who Was Royer and What Did He Design?" See also reference 2.

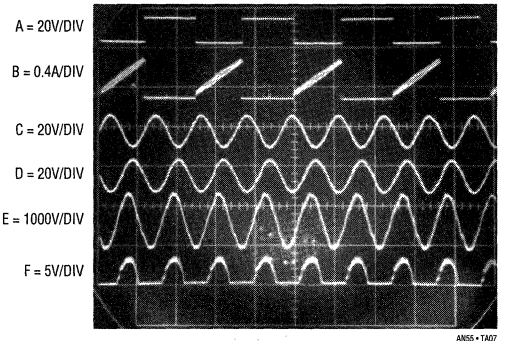


C1 = MUST BE A LOW LOSS CAPACITOR.
METALIZED POLYCARB
WIMA FKP2 OR MKP-20 (GERMAN) RECOMMENDED
L1 = SUMIDA 6345-020 OR COILTRONICS CTX110092-1
PIN NUMBERS SHOWN FOR COILTRONICS UNIT
L2 = COILTRONICS CTX300-4
Q1, Q2 = ZETEX ZTX849 OR ROHM 2SC5001
*= 1% FILM RESISTOR
DO NOT SUBSTITUTE COMPONENTS

COILTRONICS (305) 781-8900, SUMIDA (708) 956-0666

Figure 6. An 88% Efficiency Cold Cathode Fluorescent Lamp (CCFL) Power Supply

current. This signal is filtered by the 10k-1µF pair and presented to the LT1172's feedback pin. This connection closes a control loop which regulates lamp current. The 2µF capacitor at the LT1172's V_C pin provides stable loop compensation. The loop forces the LT1172 to switch-mode modulate L2's average current to whatever value is required to maintain a constant current in the lamp. The constant current's value, and hence lamp intensity, may be varied with the potentiometer. The constant current drive allows full 0%-100% intensity control with no lamp dead zones or "pop-on" at low intensities.[4] Additionally, lamp



A AND B HORIZ = 4µs/DIV
C THRU F HORIZ = 20µs/DIV
TRIGGERS FULLY INDEPENDENT

Figure 7. Waveforms for the Cold Cathode Fluorescent Lamp Power Supply. Note Independent Triggering on Traces A and B, and C through F

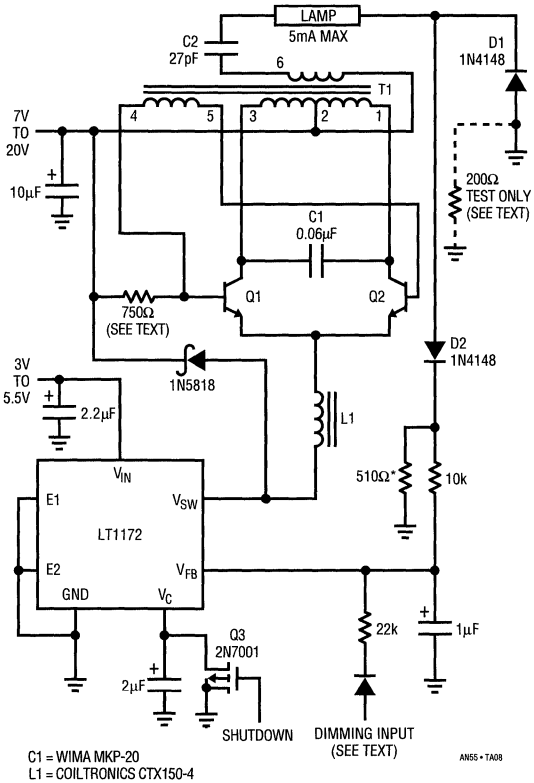
life is enhanced because current cannot increase as the lamp ages.

This circuit's 0.1% line regulation is notably better than some other approaches. This tight regulation prevents lamp intensity variation when abrupt line changes occur. This typically happens when battery powered apparatus is connected to an AC powered charger. The circuit's excellent line regulation derives from the fact that L1's drive waveform never changes shape as input voltage varies. This characteristic permits the simple 10kΩ-1µF RC to produce a consistent response. The RC averaging characteristic has serious error compared to a true RMS conversion, but the error is constant and "disappears" in the 562Ω shunt's value.

This circuit is similar to one previously described[5] but its 88% efficiency is 6% higher. The efficiency improvement is primarily due to the transistor's higher gain and lower saturation voltage. The base drive resistor's value (nominally 1kΩ) should be selected to provide full V_{CE} saturation without inducing base overdrive or beta starvation. A procedure for doing this is described in the following section, "General Measurement and Optimization Considerations."

Note 4: Controlling a nonlinear load's current, instead of its voltage, permits applying this circuit technique to a wide variety of nominally evil loads. See Appendix H, "Related Circuits."

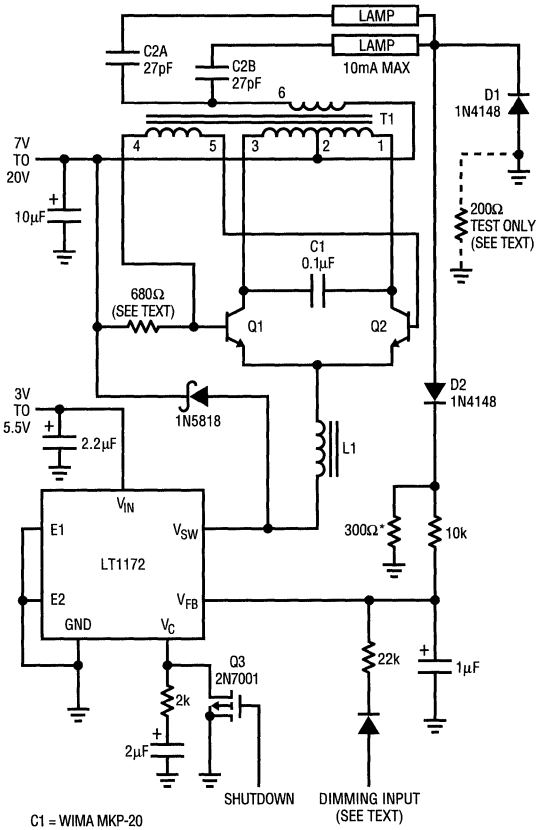
Note 5: See "Illumination Circuitry for Liquid Crystal Displays," Linear Technology Corporation, Application Note 49, August 1992.



C1 = WIMA MKP-20
L1 = COILTRONICS CTX150-4
Q1, Q2 = ZETEX ZTX849 OR ROHM 2SC5001
T1 = COILTRONICS CTX110600-1 OR SUMIDA EPS-207
PIN NUMBERS SHOWN FOR COILTRONICS UNIT
* = 1% FILM RESISTOR
DO NOT SUBSTITUTE COMPONENTS

COILTRONICS (305) 781-8900, SUMIDA (708) 956-0666

Figure 8. A 91% Efficient CCFL Supply for 5mA Loads Features Shutdown and Dimming Inputs



C1 = WIMA MKP-20
L1 = COILTRONICS CTX150-4
Q1, Q2 = ZETEX ZTX849 OR ROHM 2SC5001
T1 = COILTRONICS CTX110600-1 OR SUMIDA EPS-207
PIN NUMBERS SHOWN FOR COILTRONICS UNIT
* = 1% FILM RESISTOR
DO NOT SUBSTITUTE COMPONENTS

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Figure 9. A 92% Efficient CCFL Supply for 10mA Loads Features Shutdown and Dimming Inputs. Two Lamps are Typical of Color Displays

Figure 8's circuit is similar, but uses a transformer with lower copper and core losses to increase efficiency to 91%. The trade-off is slightly larger transformer size. Value shifts in C1, L2 and the base drive resistor reflect different transformer characteristics. This circuit also features shutdown via Q3 and a DC or pulse width controlled dimming input. Appendix F, "Intensity Control and Shutdown Methods," details operation of these features. Figure 9, directly derived from Figure 8, produces 10mA output to drive color LCD's at 92% efficiency. The slight efficiency improvement comes from a reduction in LT1172 "housekeeping" current as a percentage of total current drain. Value changes in components are the result of higher power operation. The most significant change involves driving two lamps. Accommodating two lamps involves separate ballast capacitors but circuit operation is similar. Two lamp designs reflect slightly different loading back through the transformer's primary. C2 usually ends up in the 10pF to 47pF range. Note that C2A and B appear with their lamp loads in parallel across the transformer's secondary. As such, C2's value is often smaller than in a single lamp circuit using the same type lamp. Ideally the

transformer's secondary current splits evenly between the C2-lamp branches, with the total load current being regulated. In practice, differences between C2A and B and differences in lamps and lamp wiring layout preclude a perfect current split. Practically, these differences are small, and the lamps appear to emit equal amounts of light. Layout and lamp matching can influence C2's value. Some techniques for dealing with these issues appear in the text section, "Layout Issues."

General Measurement and Optimization Considerations

Several points should be kept in mind when observing operation of these circuits. L1's high voltage secondary can only be monitored with a wideband, high voltage probe fully specified for this type of measurement. *The vast majority of oscilloscope probes will break down and fail if used for this measurement.*[6] Tektronix probe types P-6007 and P-6009 (acceptable in some cases) or types P6013A and P6015 (preferred) probes must be used to read L1's output.

Another consideration involves observing waveforms. The LT1172's switching frequency is completely asynchronous from the Q1-Q2 Royer converter's switching. As such, most oscilloscopes cannot simultaneously trigger and display all the circuit's waveforms. Figure 7 was obtained using a dual beam oscilloscope (Tektronix 556). LT1172 related Traces A and B are triggered on one beam, while the remaining traces are triggered on the other beam. Single beam instruments with alternate sweep and trigger switching (e.g., Tektronix 547) can also be used, but are less versatile and restricted to four traces.

Obtaining and verifying high efficiency[7] requires some amount of diligence. The optimum efficiency values given for C1 and C2 are typical, and will vary for specific types of lamps. An important realization is that the term "lamp" includes the *total* load seen by the transformer's secondary. This load, reflected back to the primary, sets transformer input impedance. The transformer's input impedance forms an integral part of the LC tank that produces the high voltage drive. Because of this, circuit efficiency must be optimized with the wiring, display housing and physical layout arranged *exactly* the same way they will be built in production. Deviations from this procedure will result in lower efficiency than might otherwise be possible. In practice, a "first cut" efficiency optimization with "best guess" lead lengths and the intended lamp in its display housing usually produces results within 5% of the achievable figure. Final values for C1 and C2 may be established when the physical layout to be used in production has been decided on. C1 sets the circuit's resonance point, which varies to some extent with the lamp's characteristic. C2 ballasts the lamp, effectively buffering its negative resistance characteristic. Small values of C2 provide the most load isolation, but require relatively large transformer output voltage for loop closure. Large C2 values minimize transformer output voltage, but degrade load buffering. Also, C1's "best" value is somewhat dependent on the lamp type used. Both C1 and C2 must be selected for given lamp types. Some interaction occurs, but generalized guidelines are possible. Typical values for C1 are 0.01μF to 0.15μF. C2 usually ends up in the 10pF to 47pF range. C1 *must* be a low loss capacitor and substitution of the recommended devices is not recommended. A poor quality dielectric for C1 can easily degrade efficiency by 10%. Before capacitor selection the Q1-Q2 base drive resistor should be set to a value which insures saturation, e.g., 470Ω. Next, C1 and C2 are selected by trying different values for each and iterating towards best efficiency. During this procedure insure that loop closure is maintained by monitoring the LT1172's feedback pin, which should be at 1.23V. Several trials usually produce the optimum C1 and C2 values. Note that the highest efficiencies are not necessarily associated with the most esthetically pleasing waveshapes, particularly at Q1, Q2 and the output. Finally, the base drive resistor's value should be optimized.

Note 6: Don't say we didn't warn you!

Note 7: The term "efficiency" as used here applies to electrical efficiency. In fact, the ultimate concern centers around the efficient conversion of power supply energy into light. Unfortunately, lamp types show considerable deviation in their current-to-light conversion efficiency. Similarly, the emitted light for a given current varies over the life and history of any particular lamp. As such, this publication treats "efficiency" on an electrical basis; the ratio of power removed from the primary supply to the power delivered to the lamp. When a lamp has been selected the ratio of primary supply power to lamp emitted light energy may be measured with the aid of a photometer. This is covered in Appendix D, "Photometric Measurement." See also Appendix K, "Perspectives on Efficiency."

The base drive resistor's value (nominally 1kΩ) should be selected to provide full V_{CE} saturation without inducing base overdrive or beta starvation. This point may be established for any lamp type by determining the peak collector current at full lamp power.

The base resistor should be set at the largest value that ensures saturation for worst case transistor beta. This condition may be verified by varying the base drive resistor about the ideal value and noting small variations in input supply current. The minimum obtainable current corresponds to the best beta vs saturation trade-off. In practice, supply current rises slightly on either side of this point. This "double value" behavior is due to efficiency degradation being caused by either excessive base drive or saturation losses.

Other issues influencing efficiency include lamp wire length and energy leakage from the lamp. The high voltage side of the lamp should have the smallest practical lead length. Excessive length results in radiative losses which can easily reach 3% for a 3 inch wire. Similarly, no metal should contact or be in close proximity to the lamp. This prevents energy leakage which can exceed 10%.[8]

It is worth noting that a custom designed lamp affords the best possible results. A jointly tailored lamp-circuit combination permits precise optimization of circuit operation, yielding highest efficiency.

These considerations should be made with knowledge of other LCD issues. See Appendix B, "Mechanical Design Considerations for Liquid Crystal Displays." This section was guest written by Charles L. Guthrie of Sharp Electronics Corporation.

Special attention should be given to the layout of the circuit board since high voltage is generated at the output. The output coupling capacitor must be carefully located to minimize leakage paths on the circuit board. A slot in the board will further minimize leakage. Such leakage can permit current flow outside the feedback loop, wasting power. In the worst case, long term contamination build-up can increase leakage inside the loop, resulting in starved lamp drive or destructive arcing. It is good practice for minimization of leakage to break the silk screen line which outlines transformer T1. This prevents leakage from the high voltage secondary to the primary. Another technique for minimizing leakage is to evaluate and specify the silk screen ink for its ability to withstand high voltages.

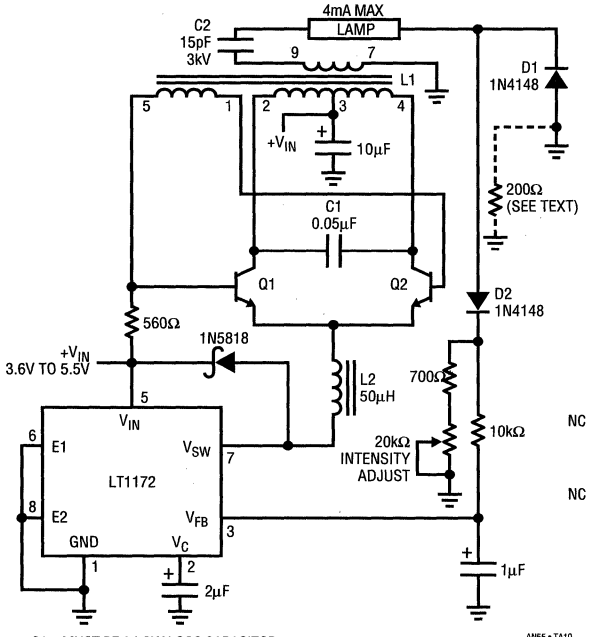
Efficiency Measurement

Once these procedures have been followed efficiency can be measured. Efficiency may be measured by determining lamp current and voltage. Measuring current involves measuring RMS voltage across a temporarily inserted 200Ω, 0.1% resistor in the ground lead of the negative current steering diode. The lamp current is: $I_{LAMP} = E_{RMS}/200\Omega \times 2$. The × 2 factor is necessitated because the diode steering dumps the current to ground on negative cycles. The 200Ω value allows the RMS meter to read with a scale factor numerically identical to the total current. Once this measurement is complete the 200Ω resistor may be deleted and the negative current steering diode again returned directly to ground. Lamp RMS voltage is measured at the lamp with a properly compensated high voltage probe. Multiplying these two results gives power in watts, which may be compared to the DC input supply(s) E×I product(s). In practice, the lamp's current and voltage contain small out of phase components but their error contribution is negligible.

Both the current and voltage measurements require a wideband True RMS voltmeter. The meter must employ a thermal type RMS converter—the more common logarithmic computing type based instruments are inappropriate because their bandwidth is too low.

The previously recommended high voltage probes are designed to see a 1MΩ-10pF-22pF oscilloscope input. The RMS voltmeters have a 10MΩ input. This difference necessitates an impedance matching network between the probe and the voltmeter. Details on this and other efficiency measurement issues appear in Appendix C, "Achieving Meaningful Efficiency Measurements."

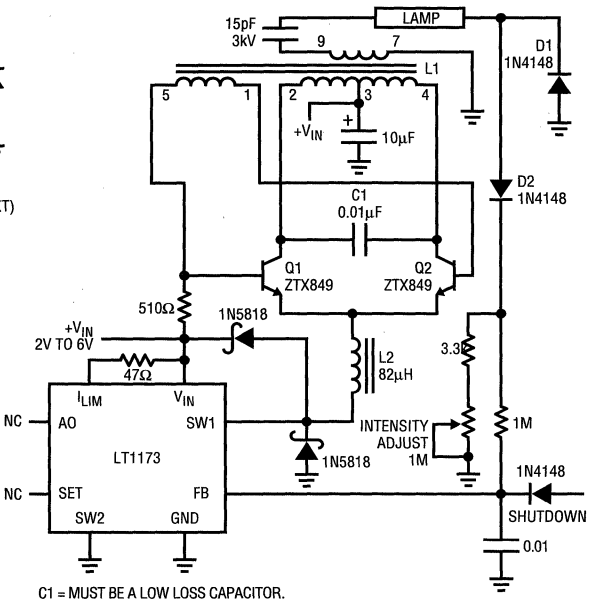
Note 8: A very simple experiment quite nicely demonstrates the effects of energy leakage. Grasping the lamp at its low voltage end (low field intensity) with thumb and forefinger produces almost no change in circuit input current. Sliding the thumb-forefinger combination towards the high voltage (higher field intensity) lamp end produces progressively greater input currents. Don't touch the high voltage lead or you may receive an electrical shock. Repeat: Do not touch the high voltage lead or you may receive an electrical shock.



C1 = MUST BE A LOW LOSS CAPACITOR.
METALIZED POLYCARB
WIMA FKP2 OR MKP-20 (GERMAN) RECOMMENDED
L1 = COILTRONICS CTX110654-1
L2 = COILTRONICS CTX50-4
Q1, Q2 = ZETEX ZTX849 OR ROHM 2SC5001
* = 1% FILM RESISTOR
DO NOT SUBSTITUTE COMPONENTS

COILTRONICS (305) 781-8900, SUMIDA (708) 956-0666

Figure 10. A 4mA Design Intended for Low Voltage Operation. L1's Modified Turns Ratio Allows Operation Down to 3.6V



C1 = MUST BE A LOW LOSS CAPACITOR.
METALIZED POLYCARB
WIMA FKP2 OR MKP-20 (GERMAN) RECOMMENDED
L1 = SUMIDA 6345-020 OR COILTRONICS CTX110092-1
PIN NUMBERS SHOWN FOR COILTRONICS UNIT
L2 = TOKO 262LYF-0091K
(408) 432-8251
DO NOT SUBSTITUTE COMPONENTS

Figure 11. Low Power CCFL Power Supply. Circuit Controls Lamp Current Over a 1µA to 1mA Range

Low Power CCFL Supplies

Many applications require relatively low power CCFL backlighting. Figure 10's variation, optimized for low voltage inputs, produces 4mA output. Circuit operation is similar to the previous examples. The fundamental difference is L1's higher turns ratio, which accommodates the reduced available drive voltage. The circuit values given are typical, although some variation occurs with various lamps and layouts.

Figure 11's design, the so-called "dim backlight," is optimized for single lamp operation at very low currents. The circuit is meant for use at low input voltages, typically 2V to 6V with a 1mA maximum lamp current. This circuit maintains control down to lamp currents of 1µA, a very dim light! It is intended for applications where the longest possible battery life is desired. Primary supply drain ranges from hundreds of microamperes to 100mA with lamp currents of microamps to 1mA. In shutdown the circuit pulls only 100µA. Maintaining high efficiency at low lamp currents requires modifying the basic design.

Achieving high efficiency at low operating current requires lowering quiescent power drain. To do this the LT1172, a pulse width modulator based device, is replaced with an LT1173. The LT1173 is a Burst Mode™ operation regulator. When this device's feedback pin is too low it delivers a burst of output current pulses, putting energy into the transformer and restoring the feedback point. The regulator maintains control by appropriately modulating the burst duty cycle. The ground referred diode at the V_{SW} pin prevents substrate turn-on due to excessive L2 ring-off.

Burst Mode is a trademark of Linear Technology Corporation.

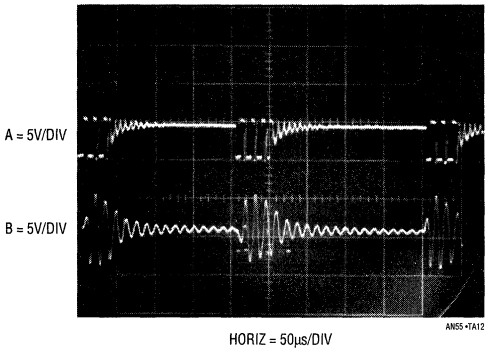


Figure 12. Waveforms for the Low Power CCFL Power Supply. LT1173 Burst Type Regulator (Trace A) Periodically Excites the Resonant High Voltage Converter (Q1 Collector is Trace B)

During the off periods the regulator is essentially shut down. This type of operation limits available output power, but cuts quiescent current losses. In contrast, the other circuit's LT1172 pulse width modulator type regulator maintains "housekeeping" current between cycles. This results in more available output power but higher quiescent currents.

Figure 12 shows operating waveforms. When the regulator comes on (Trace A, Figure 12) it delivers bursts of output current to the L1-Q1-Q2 high voltage converter. The converter responds with bursts of ringing at its resonant frequency.[9] The circuit's loop operation is similar to the previous designs except that L1's drive waveform varies with supply. Because of this, line regulation suffers and the circuit is not recommended for wide ranging inputs.

Some lamps may display non-uniform light emission at very low excitation currents. See the text section, "Extending Illumination Range."

Note 9: The discontinuous energy delivery to the loop causes substantial jitter in the burst repetition rate, although the high voltage section maintains resonance. Unfortunately, circuit operation is in the "chop" mode region of most oscilloscopes, precluding a detailed display. "Alternate" mode operation causes waveform phasing errors, producing an inaccurate display. As such, waveform observation requires special techniques. Figure 12 was taken with a dual beam instrument (Tektronix 556) with both beams slaved to one time base. Single sweep triggering eliminated jitter artifacts. Most oscilloscopes, whether analog or digital, will have trouble reproducing this display.

LCD Bias Supplies

LCDs also require a bias supply for contrast control. The supply's variable output permits adjustment of display contrast. Relatively little power is involved, easing RF radiation and efficiency requirements. The logic sections of display drivers operate from single 5V supplies, but the actual driver outputs swing between +5V and a negative bias potential. Varying this bias causes the display contrast to vary.

An LCD bias generator, developed by Steve Pietkiewicz of LTC, is shown in Figure 13. In this circuit U1 is an LT1173 micropower DC to DC converter. The 3V input is converted to +24V by U1's switch, L2, D1, and C1. The switch pin (SW1) also drives a charge pump composed of C2, C3, D2, and D3 to generate –24V. Line regulation is less than 0.2% from 3.3V to 2V inputs. Load regulation, although suffering somewhat since the –24V output is not directly regulated, measures 2% from a 1mA to 7mA load. The circuit will deliver 7mA from a 2V input at 75% efficiency.

If greater output power is required, Figure 13's circuit can be driven from a +5V source. R1 should be changed to 47Ω and C3 to 47µF. With a 5V input, 40mA is available at 75% efficiency. Shutdown is accomplished by bringing D4's anode to a logic high, forcing the feedback pin of U1 to go above the internal 1.25V reference voltage.

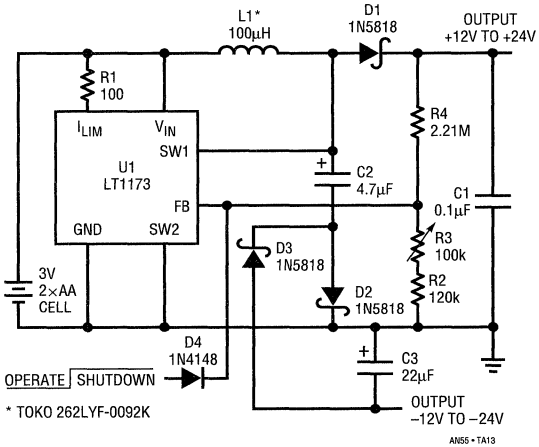


Figure 13. DC to DC Converter Generates LCD Bias

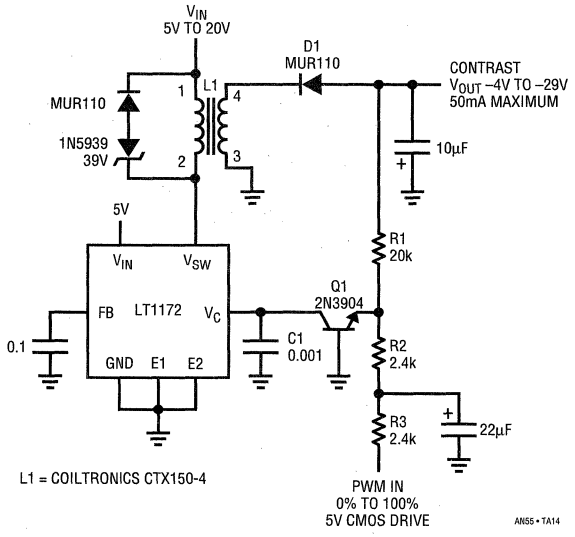


Figure 14. A Transformer Based LCD Contrast Supply. Q1 Level Shifts the Feedback Signal and Functions as a Reference Amplifier

Shutdown current is 110µA from the input source and 36µA from the shutdown signal.

Figure 14 is a transformer based approach to generating LCD bias. The LT1172 drives L1, producing negative flyback events at pin 4. D1 rectifies these events, producing a negative DC output. The R1-R2-R3 string sets feedback at Q1's emitter. Q1, acting as a reference amplifier, biases the LT1172, closing a control loop. C1 provides frequency compensation, stabilizing the loop. In this case, a pulse width modulated signal biases the feedback string, setting operating point and contrast. A 0V to 5V DC signal could also be used. The use of Q1's V_{BE} as a reference introduces a –0.3%/°C temperature coefficient, but this is not deleterious to system operation. Maximum output current is 50mA and efficiency measures about 82%.

Dual Output LCD Bias Voltage Generator

The many different kinds of LCD displays available make programming LCD bias voltage at the time of manufacture attractive. Figure 15's circuit, developed by Jon Dutra of

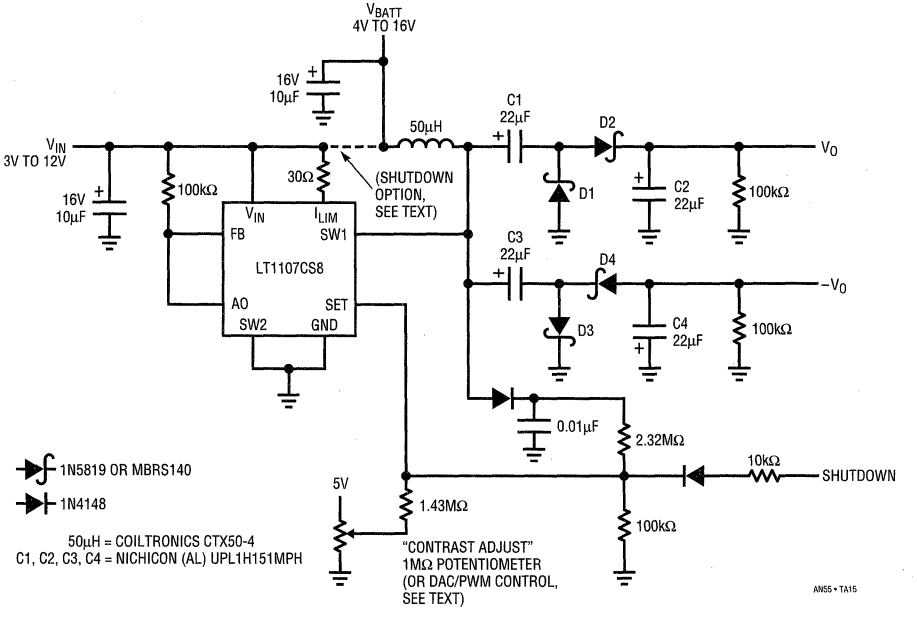


Figure 15. Dual Output LCD Bias Voltage Generator

LTC, is an AC coupled boost topology. The feedback signal is derived separately from the outputs, so loading does not affect loop compensation, although load regulation is somewhat compromised. With 28V out, from 10% to 100% load (4mA to 40mA), the output voltage sags about 0.65V. From 1mA to 40mA load the output voltage drops about 1.4V. This is acceptable for most displays.

Output noise is reduced by using the auxiliary gain block within the LT1107 (see LT1107 data sheet) in the feedback path. This added gain effectively reduces comparator hysteresis and tends to randomize output noise. Output noise is below 30mV over the output load range. Output power increases with V_{BATT}, from about 1.4W with 5V in to about 2W with 8V or more. Efficiency is 80% over a broad output power range. If only a positive or negative output voltage is required, the diodes and capacitors associated with the unused output can be eliminated. The 100kΩ resistor is required on each output to load a parasitic voltage doubler created by D2-D4 shunt capacitance. Without this minimum load, the output voltage can rise to unacceptable levels.

The voltage at the switch pin (SW1) swings from 0V to V_{OUT} plus 2 diode drops. This voltage is AC coupled to the positive output through C1 and D1, and to the negative output through C3 and D3. C1 and C3 have the full RMS output current flowing through them. Most tantalum capacitors are not rated for current flow. Use of a rated tantalum or electrolytic is recommended for reliability. At lower output currents monolithic ceramics are also an option.

The circuit may be shut down in several ways. The easiest is to pull the set pin above 1.25V. This approach consumes 200μA in shutdown. A lower power method is to turn off V_{IN} to the LT1107 by a high side switch or simply disable the input supply (see option in schematic). This drops quiescent current from the V_{BATT} input below 10μA. In both cases V_{OUT} drops to zero volts. In the event $+V_{OUT}$ does not need to drop to zero, C1 and D1 can be eliminated. The output voltage can be adjusted from any voltage above V_{BATT} to 46V. Output voltage can be controlled by the user with DAC, PWM or potentiometer control. Summing currents into the feedback node allows downward adjustment of output voltage.

Layout

The physical layout of the lamp, its leads, the display housing and other high voltage components is an integral part of the circuit. Poor layout can easily degrade efficiency by 25%, and higher layout induced losses have been observed. Producing an optimal layout requires attention to how losses occur. Figure 16 begins our study by examining potential parasitic paths between the transformer's output and the lamp. Parasitic capacitance to AC ground from any point between the transformer output and the lamp creates a path for undesired current flow. Similarly, stray coupling from any point along the lamp's length to AC ground induces parasitic current flow. All parasitic current flow is wasted, causing the circuit to produce more energy to maintain the desired current flow

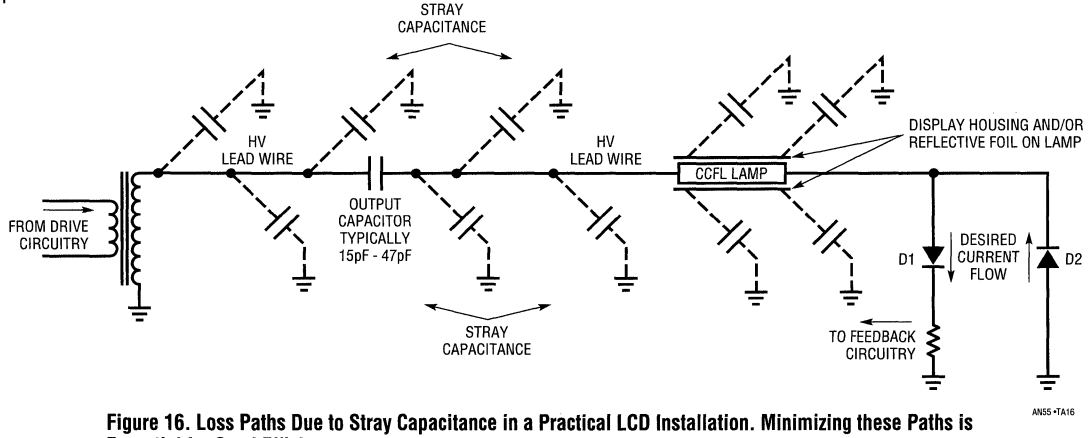


Figure 16. Loss Paths Due to Stray Capacitance in a Practical LCD Installation. Minimizing these Paths is Essential for Good Efficiency

in D1 and D2. The high voltage path from the transformer to the display housing should be as short as possible to minimize losses. A good rule of thumb is to assume 1% efficiency loss per inch of high voltage lead. Any PC board ground or power planes should be relieved by at least 1/4" in the high voltage area. This not only prevents losses, but eliminates arcing paths.

Parasitic losses associated with lamp placement within the display housing require attention. High voltage wire length within the housing must be minimized, particularly for displays using metal construction. Insure that the high voltage is applied to the shortest wire(s) in the display. This may require disassembling the display to verify wire length and layout. Another loss source is the reflective foil commonly used around lamps to direct light into the actual LCD. Some foil materials absorb considerably more field energy than others, creating loss. Finally, displays supplied in metal enclosures tend to be lossy. The metal absorbs significant energy and an AC path to ground is unavoidable. Direct grounding of a metal enclosed display further increases losses. Some display manufacturers have addressed this issue by relieving the metal in the lamp area with other materials.

The highest efficiency "in system" backlights have been produced by careful attention to these issues. In some cases the entire display enclosure was re-engineered for lowest losses.

Layout Considerations for Two Lamp Designs

Systems using two lamps have some unique layout problems. Almost all two lamp displays are color units. The lower light transmission characteristics of color displays necessitates more light. As such, display manufacturers use two lamps to produce more light. The wiring layout of these two lamp color displays affects efficiency and illumination balance in the lamps. Figure 17 shows an "x-ray" view of a typical display. This symmetrical arrangement presents equal parasitic losses. If C1 and C2 and the lamps are matched, the circuit's current output splits evenly and equal illumination occurs.

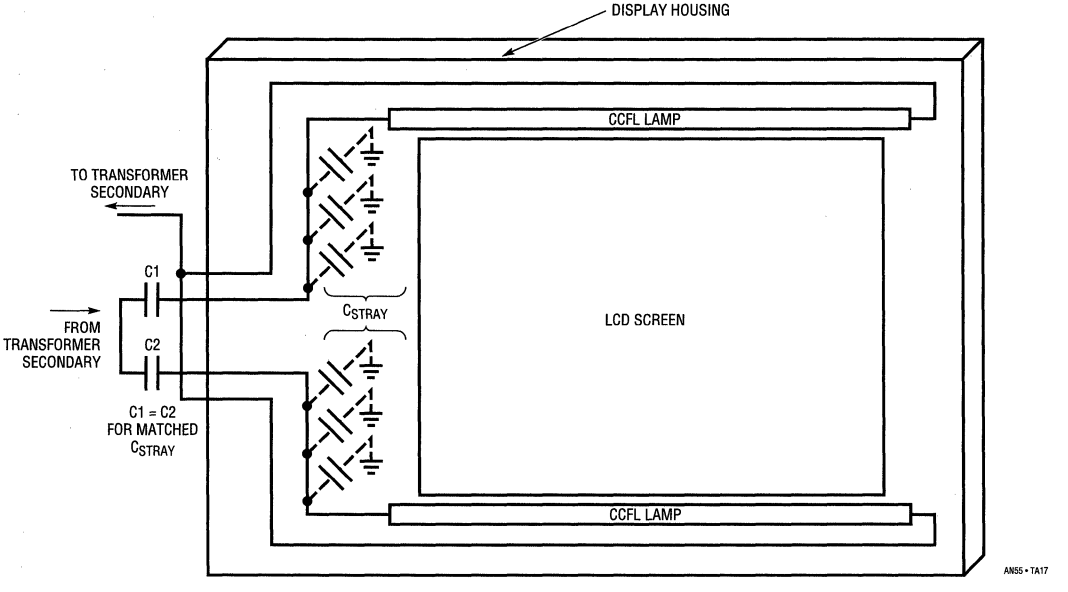


Figure 17. Loss Paths for a "Best Case" Dual Lamp Display. Symmetry Promotes Balanced Illumination

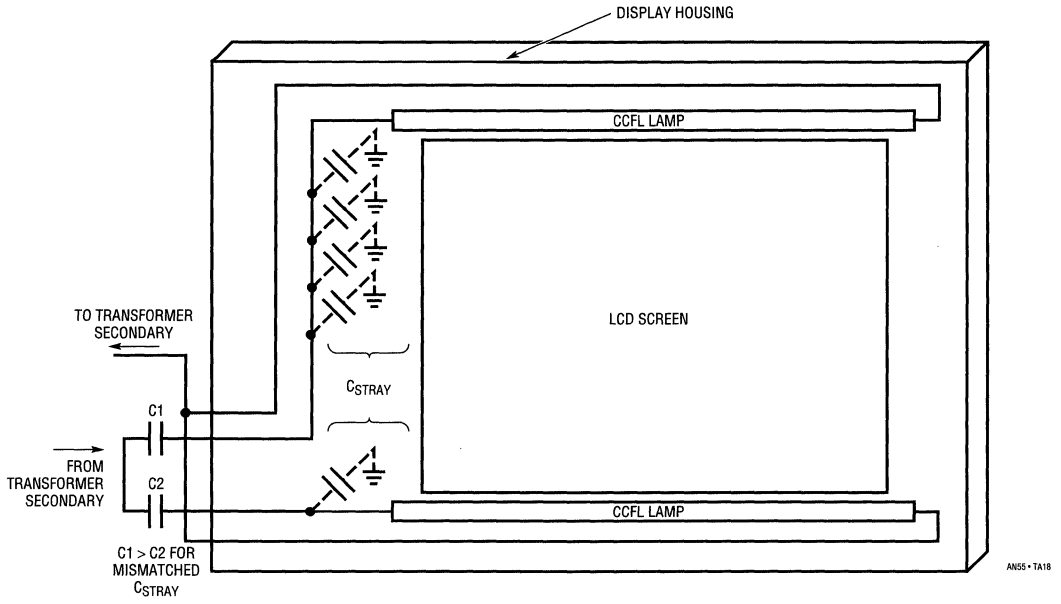


Figure 18. Asymetric Losses in a Dual Lamp Display. Skewing C1 and C2 Values Compensates Imbalanced Loss Paths, but Not Wasted Energy

Figure 18's display arrangement is less friendly. The asymmetrical wiring forces unequal losses, and the lamps receive imbalanced current. Even with identical lamps, illumination may not be balanced. This condition is correctable by skewing C1 and C2's values. C1, because it drives greater parasitic capacitance, should be larger than C2. This tends to equalize the currents, promoting equal lamp drive. It is important to realize that this compensation does nothing to recapture the lost energy—efficiency is still compromised. There is no substitute for minimizing loss paths.

In general, imbalanced illumination causes fewer problems than might be supposed. The effect is very difficult for the eye to detect at high intensity levels. Unequal illumination is much more noticeable at lower levels. In the worst case the dimmer lamp may only partially illuminate. This phenomenon, sometimes called "Thermometering," is discussed in detail in the text section "Extending Illumination Range."

Feedback Loop Stability Issues

The circuits shown to this point rely on closed loop feedback to maintain the operating point. All linear closed loop systems require some form of frequency compensation to achieve dynamic stability. Circuits operating with relatively low power lamps may be frequency compensated by simply overdamping the loop. Text Figures 6, 8 and 10 use this approach. The higher power operation associated with color displays requires more attention to loop response. The transformer produces much higher output voltages, particularly at start-up. Poor loop damping can allow transformer voltage ratings to be exceeded, causing arcing and failure. As such, higher power designs may require optimization of transient response characteristics.

Figure 19 shows the significant contributors to loop transmission in these circuits. The resonant Royer converter delivers information at about 50kHz to the lamp. This

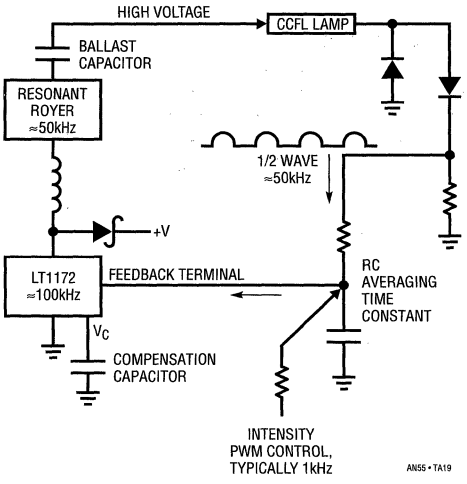


Figure 19. Delay Terms in the Feedback Path. The RC Time Constant Dominates Loop Transmission Delay and must be Compensated for Stable Operation

information is smoothed by the RC averaging time constant and delivered to the LT1172's feedback terminal as DC. The LT1172 controls the Royer converter at a 100kHz rate, closing the control loop. The capacitor at the LT1172 rolls off gain, nominally stabilizing the loop. This compensation capacitor must roll off the gain bandwidth at a low enough value to prevent the various loop delays from causing oscillation.

Which of these delays is the most significant? From a stability viewpoint the LT1172's output repetition rate and the Royer's oscillation frequency are sampled data systems. Their information delivery rate is far above the RC averaging time constants delay and is not significant. The RC time constant is the major contributor to loop delay. This time constant must be large enough to turn the half wave rectified waveform into DC. It also must be large enough to average any intensity control PWM signal to DC. Typically, these PWM intensity control signals come in at a 1kHz rate (see Appendix F, "Intensity Control and Shutdown Methods"). The RC's resultant delay dominates loop transmission. It must be compensated by the capacitor at the LT1172. A large enough value for this capacitor rolls off loop gain at low enough frequency to provide stability. The loop simply does not have enough gain to oscillate at a frequency commensurate with the RC delay.[10]

This form of compensation is simple and effective. It ensures stability over a wide range of operating conditions. It does, however, have poorly damped response at system turn-on. At turn-on the RC lag delays feedback, allowing output excursions well above the normal operating point. When the RC acquires the feedback value the loop stabilizes properly. This turn-on overshoot is not a concern if it is well within transformer breakdown ratings. Color displays, running at higher power, usually require large initial voltages. If loop damping is poor, the overshoot may be dangerously high. Figure 20 shows such a loop responding to turn-on. In this case the RC values are 10k and 4.7µF, with a 2µF compensation capacitor. Turn-on overshoot exceeds 3500V for over 10ms! Ring-off takes over 100ms before settling occurs. Additionally, an inadequate (too small) ballast capacitor and excessively lossy layout force a 2000V output once loop settling occurs. This photo was taken with a transformer rated well below this figure. The resultant arcing caused transformer destruction, resulting in field failures. A typical destroyed transformer appears in Figure 21.

Figure 22 shows the same circuit, with the RC values reduced to 10k and 1µF. The ballast capacitor and layout have also been optimized. Figure 22 shows peak voltage

Note 10: The high priests of feedback refer to this as "Dominant Pole Compensation." The rest of us are reduced to more pedestrian descriptives.

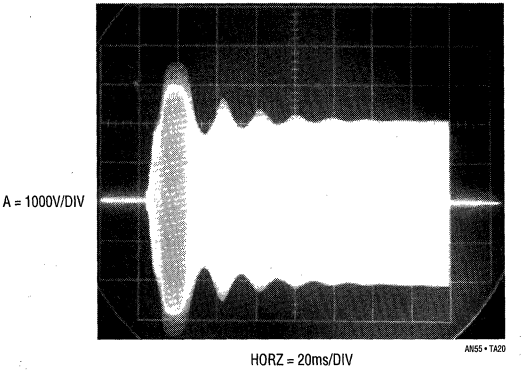


Figure 20. Destructive High Voltage Overshoot and Ring-Off Due to Poor Loop Compensation. Transformer Failure and Field Recall are Nearly Certain. Job Loss may also Occur

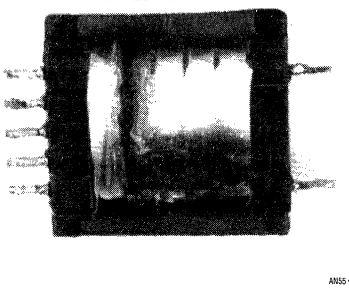


Figure 21. Poor Loop Compensation Caused this Transformer Failure. Arc Occured in High Voltage Secondary (Lower Right). Resultant Shorted Turns Caused Overheating

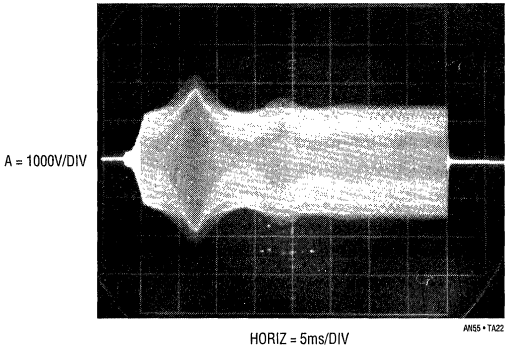


Figure 22. Reducing RC Time Constant Improves Transient Response, although Peaking, Ring-Off and Run Voltage are Still Excessive

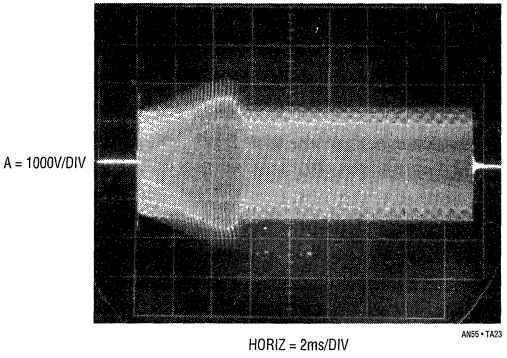


Figure 23. Additional Optimization of RC Time Constant and Compensation Capacitor Reduces Turn-On Transient. Run Voltage is Large, Indicating Possible Lossy Layout and Display

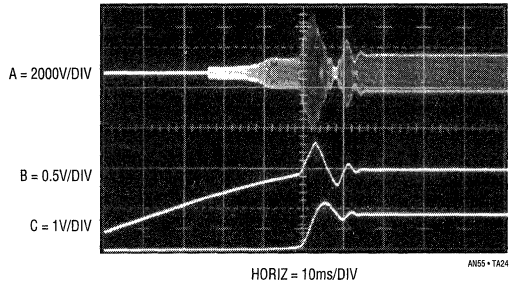


Figure 24. Waveforms for a Lower Loss Layout and Display. High Voltage Overshoot (Trace A) is Reflected at Compensation Node (Trace B) and Feedback Pin (Trace C)

reduced to 2.2kV with duration down to about 2ms (note horizontal scale change). Ring-off is also much quicker, with lower amplitude excursion. Increased ballast capacitor value and wiring layout optimization reduce running voltage to 1300V. Figure 23's results are even better. Changing the compensation capacitor to a 3kΩ-2μF network introduces a leading response into the loop, allowing faster acquisition. Now, turn-on excursion is slightly lower, but greatly reduced in duration (again, note horizontal scale change). The running voltage remains the same.

The photos show that changes in compensation, ballast value and layout result in dramatic reductions in overshoot amplitude and duration. Figure 20's performance almost guarantees field failures, while Figures 22 and 23 do not overstress the transformer. Even with the improvements, more margin is possible if display losses can be controlled. Figures 20-23 were taken with an exceptionally lossy display. The metal enclosure was very close to the metallic foil wrapped lamps, causing large losses with subsequent high turn-on and running voltages. If the display is selected for lower losses, performance can be greatly improved.

Figure 24 shows a low loss display responding to turn-on with a 2μF compensation capacitor and 10k-1μF RC values. Trace A is the transformer's output while Traces B and C are the LT1172's $V_{Compensation}$ and feedback pins, respectively. The output overshoots and rings badly,

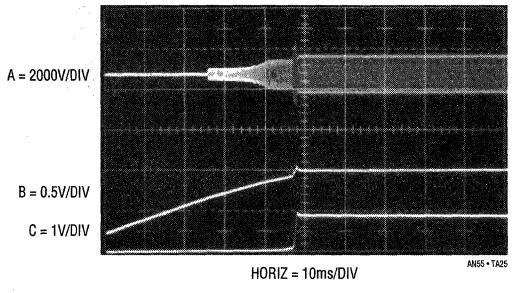


Figure 25. Reducing RC Time Constant Produces Quick, Clean Loop Behavior. Low Loss Layout and Display Result in 650V_{RMS} Running Voltage

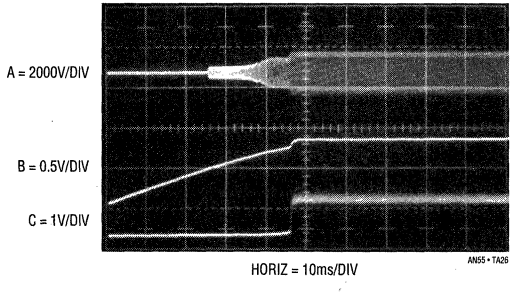


Figure 26. Very Low RC Value Provides Even Faster Response, but Ripple at Feedback Pin (Trace C) is too High. Figure 25 is the Best Compromise

peaking to about 3000V. This activity is reflected by overshoots at the $V_{Compensation}$ pin (the LT1172's error amplifier output) and the feedback pin. In Figure 25 the RC is reduced to 10kΩ-0.1μF. This substantially reduces loop delay. Overshoot goes down to only 800V—a reduction of almost a factor of four. Duration is also much shorter. The $V_{Compensation}$ and feedback pins reflect this tighter control. Damping is much better, with slight overshoot induced at turn-on. Further reduction of the RC to 10k-0.01μF (Figure 26) results in even faster loop capture, but a new problem appears. In Trace A lamp turn on is so fast the overshoot does not register in the photo. The $V_{Compensation}$ (Trace B) and feedback nodes (Trace C) reflect this with exceptionally fast response. Unfortunately, the RC's light filtering causes ripple to appear when the feedback node settles. As such, Figure 25's RC values are probably more realistic for this situation.

The lesson from this exercise is clear. The higher voltages involved in color displays mandate attention to transformer outputs. Under running conditions layout and display losses can cause higher loop compliance voltages, degrading efficiency and stressing the transformer. At turn-on improper compensation causes huge overshoots, resulting in possible transformer destruction. Isn't a day of loop and layout optimization worth a field recall?

Extending Illumination Range

Lamps operating at relatively low currents may display the "thermometer effect," that is, light intensity may be non-uniformly distributed along lamp length. Figure 27 shows that although lamp current density is uniform, the associated field is imbalanced. The field's low intensity, combined with its imbalance, means that there is not enough energy to maintain uniform phosphor glow beyond some point. Lamps displaying the thermometer effect emit most of their light near the positive electrode, with rapid emission fall-off as distance from the electrode increases. Placing a conductor along the lamp's length largely alleviates "thermometering." The trade-off is decreased efficiency due to energy leakage (see footnote 8 and associated text). It is worth noting that various lamp types have different degrees of susceptibility to the thermometer effect.

Some displays require extended illumination range. "Thermometering" usually limits the lowest practical illumination level. One acceptable way to minimize "thermometering" is to eliminate the large field imbalance. Figure 28's circuit does this. This circuit's most significant

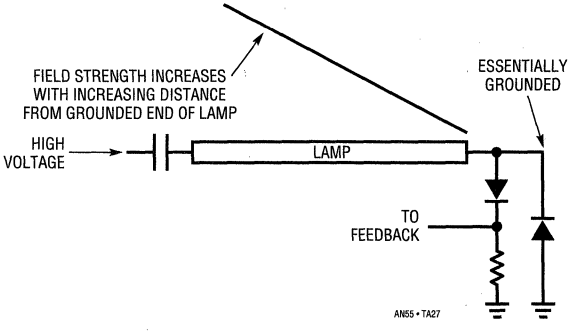


Figure 27. Field Strength vs Distance for a Ground Referred Lamp. Field Imbalance Promotes Uneven Illumination at Low Drive Levels

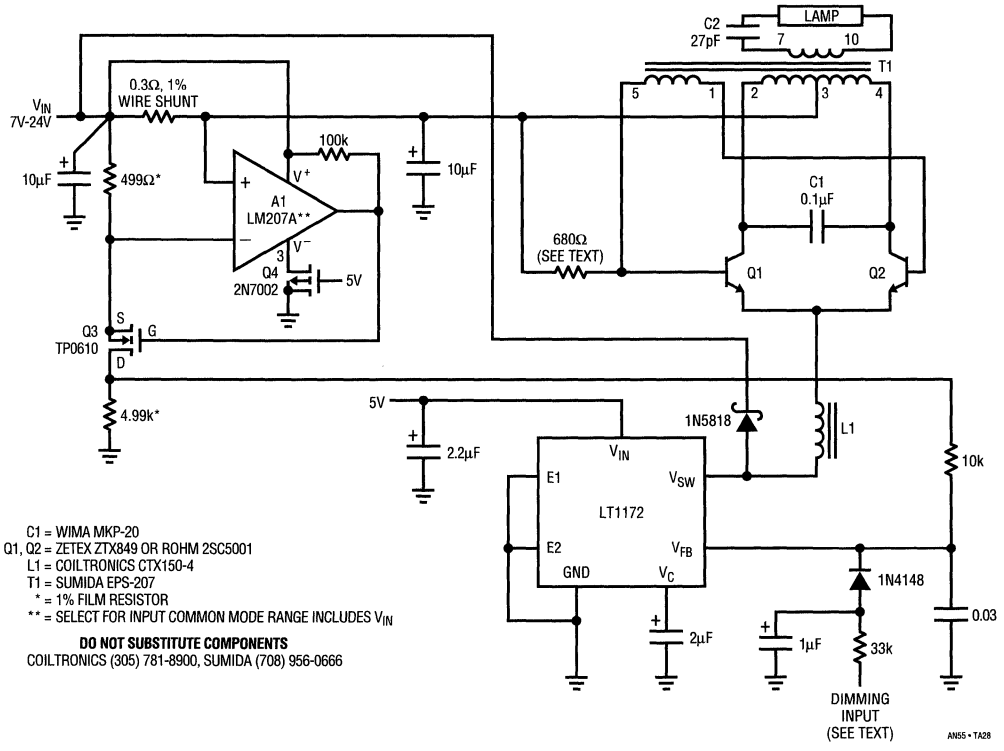


Figure 28. The "Low Thermometer" Configuration. "Topside Sensed" Primary Derived Feedback Balances Lamp Drive, Extending Dimming Range

aspect is that the lamp is fully floating—there is no galvanic connection to ground as in the previous designs. This allows T1 to deliver symmetric, differential drive to the lamp. Such balanced drive eliminates field imbalance, reducing thermometering at low lamp currents. This approach precludes any feedback connection to the now floating output. Maintaining closed loop control necessitates deriving a feedback signal from some other point. In theory, lamp current proportions to T1's or L1's drive level, and some form of sensing this can be used to provide feedback. In practice, parasitics make a practical implementation difficult.[11]

Figure 28 derives the feedback signal by measuring Royer converter current and feeding this information back to the LT1172. The Royer's drive requirement closely proportions to lamp current under all conditions. A1 senses this current across the 0.3Ω shunt and biases Q3, closing a local feedback loop. Q3's drain voltage presents an amplified, single ended version of the shunt voltage to the feedback point, closing the main loop. The lamp current is not as tightly controlled as before, but 0.5% regulation over wide supply ranges is possible. The dimming in this circuit is controlled by a 1kHz PWM signal. Note the heavy filtering (33k-1µF) *outside* the feedback loop. This allows a fast time constant, minimizing turn-on overshoot.[12]

In all other respects operation is similar to the previous circuits. This circuit typically permits the lamp to operate over a 40:1 intensity range without "thermometering." The normal feedback connection is usually limited to a 10:1 range.

Note 11: See Appendix J, "A Lot of Cut-Off Ears and No Van Goghs—Some Not-So-Great Ideas," for details.

Note 12: See text section, "Feedback Loop Stability Issues."

The losses introduced by the current shunt and A1 degrade overall efficiency by about 2%. As such, circuit efficiency is limited to about 90%. Most of the loss can be recovered at moderate cost in complexity. Figure 29's modifications reduce shunt and A1 losses. A1, a precision micropower type, cuts power drain and permits a smaller shunt value without performance degradation. Unfortunately, A1 does not function when its inputs reside at the V^+ rail. Because the circuit's operation requires this, some accommodation must be made.[13]

At circuit start-up A1's input is pulled to its supply pin potential (actually, slightly above it). Under these conditions A1's input stage is shut off. Normally, A1's output state would be indeterminate but, for the amplifier specified, it will always be high. This turns off Q3, permitting the LT1172 to drive the Royer stage. The Royer's operation causes Q1's collector swing to exceed the supply rail. This turns on the 1N4148, the BAT-85 goes off and A1's supply pin rises above the supply rail. This "bootstrapping" action results in A1's inputs being biased within the amplifier's common mode range and normal circuit operation commences.

Note 13: In other words, we need a hack.

The result of all this is a 1.6% efficiency gain, permitting an overall circuit efficiency of just below 92%.

Synchronizing

In some situations it is desirable to synchronize circuit operation to a system clock. In particular, pen based computers may be especially sensitive to asynchronous components. The LT1172 can be synchronized by briefly pulling its V_C pin to ground (see LT1172 data sheet).

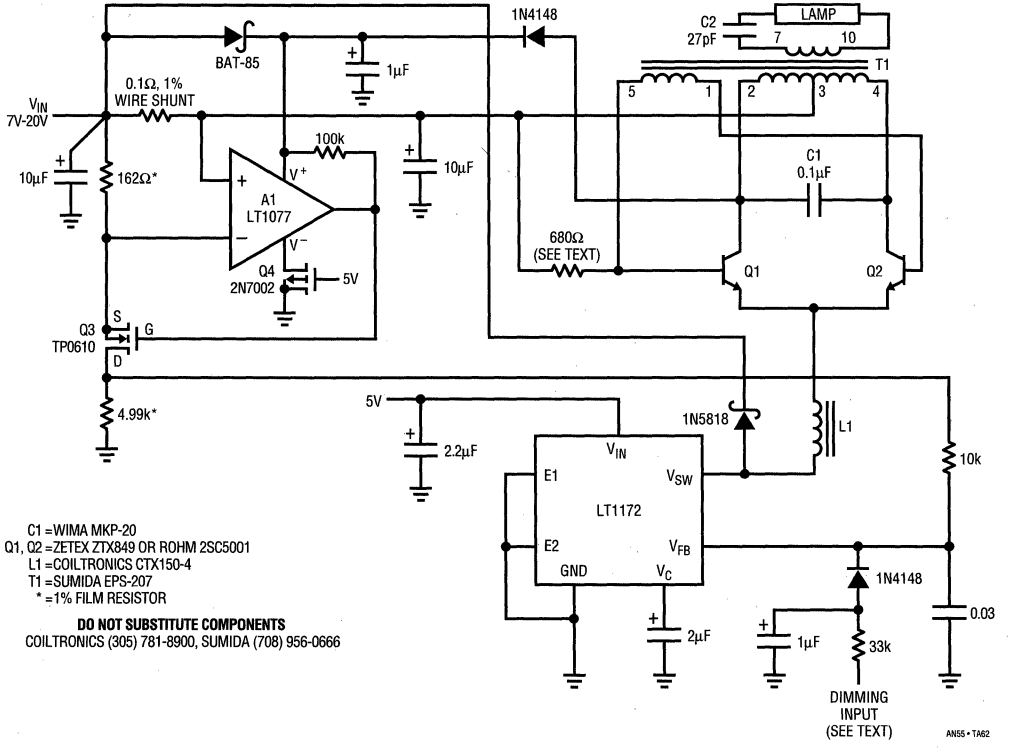


Figure 29. The "Low Thermometer" Circuit using a Micropower, Precision Topside Sensing Amplifier. Supply Bootstrapping Eliminates Input Common Mode Requirement, Permitting a 1.6% Efficiency Gain

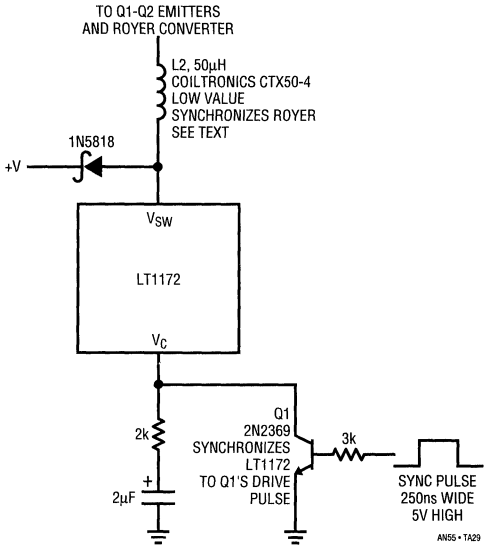


Figure 30. Synchronizing by Lowering L2's Value

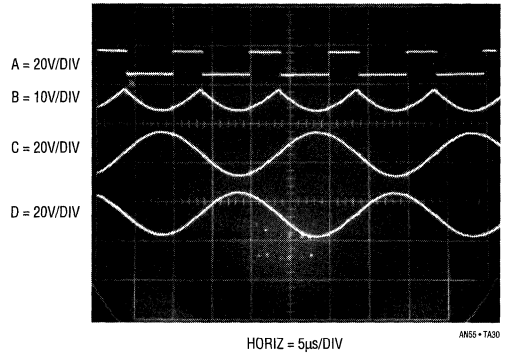


Figure 31. Waveforms for Synchronized Operation

Figure 30 shows a way to do this via Q1 and associated components. If Royer synchronization is also required, reducing L2's value can do this under some conditions. L2's low value introduces greater LT1172 harmonic, causing the Royer to lock at 1/2 the LT1172's switching frequency. This can only occur *if the free running Royer frequency is close to this value.* Pulling the Royer away from its resonant frequency causes some efficiency loss. A further limitation is that, although synchronization is never lost, phase jitter increases over extended dimming and supply ranges. Typically, 2.5:1 ranges of supply and 10:1 dimming range are practical. Efficiency is typically degraded by about 5% at full power. This approach to full synchronization is simple, but interactions are complex and require careful evaluation for any specific application. Figure 31 shows LT1172 V_{SW} pin, Q1-Q2 emitter and Royer collector waveforms (Traces A, B, C and D respectively) for a synchronized circuit.

Figure 32 uses a different approach to achieve fully synchronized operation. Here, Q1 and Q2 are driven from L3. L3's drive, in turn, comes from a flip-flop which is clocked from the LT1172's V_{SW} pin. L3 provides a level shift, allowing drive to the floating Q1-Q2 pair. The flip-flop's differential drive prevents DC biasing of L3. D1 and D2 permit L3's output current to alternately bias Q1 and Q2 without V_{BE} reverse bias occurring. Figure 33 shows operating waveforms. Trace A is the LT1172 V_{SW} pin while traces B and C are the flip-flop outputs. Traces D and E are the Q1-Q2 bases and Traces F and G their collectors. This scheme works reasonably well, although phase jitter and

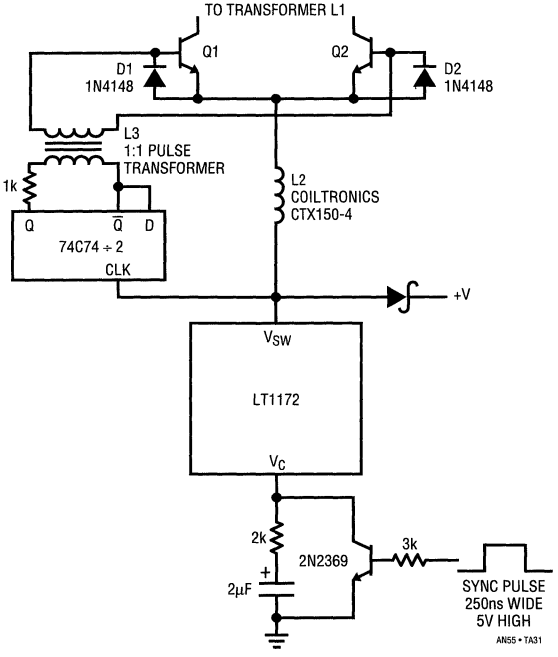


Figure 32. Synchronizing by Driving the DC to AC Converter

efficiency restrictions (similar to those previously described) apply.

Figure 34's approach eliminates phase jitter. This prototype circuit replaces the Royer configuration with a flip-flop driven pair, Q1-Q2. The flip-flop is driven from an external clock. This clock also sets the frequency of the step-down regulator feeding the L1 based high voltage converter. The step-down regulator supplies a DC potential to L2. L2's "output" end sources current to the L1 based converter. C1, C2, L1 and the lamp form a tank circuit which, nominally, resonates at the clock regulated frequency. L1's high voltage output puts current through the lamp. Feedback from the lamp, similar to the previous circuit's, closes a control loop at the step-down regulator. The 0.22µF capacitor stabilizes this loop.

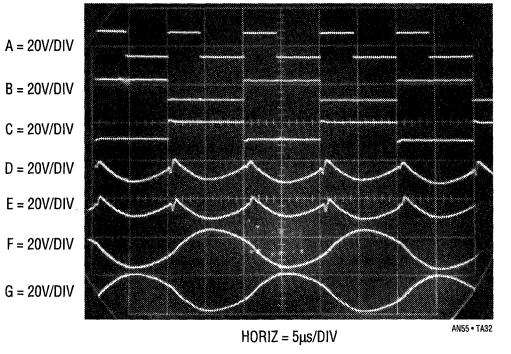


Figure 33. Waveforms for the Driven DC to AC Converter

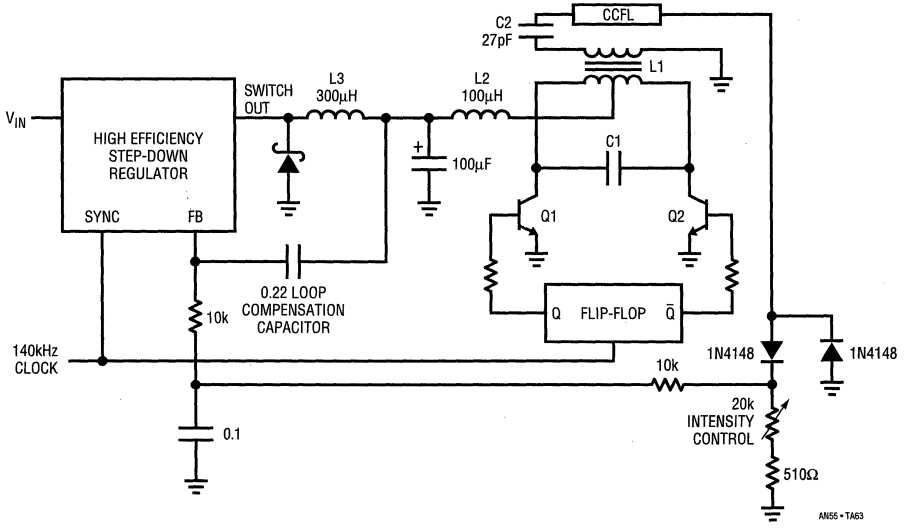


Figure 34. An Inherently Synchronous CCFL Circuit Eliminates Phase Jitter. Trade-Offs Include Increased Complexity and Lower Efficiency over Lamp Operating Range

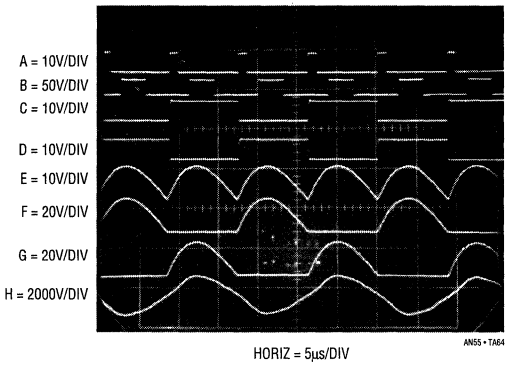


Figure 35. The Fully Synchronized CCFL Circuit's Waveforms, Taken During On-Resonance Operation

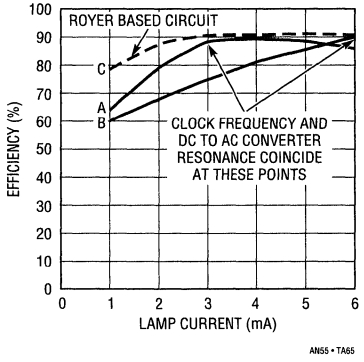


Figure 36. Efficiency vs Lamp Current for the Synchronous Circuit. Off-Resonance Operation Causes Efficiency Fall-Off away from Indicated Lamp Currents

Figure 35 shows circuit waveforms. Trace A is the clock, while Trace B is the step-down regulator's switch output. Traces C and D are flip-flop Q and $\overline{Q}$ outputs, respectively. Trace E is the L2-L1 junction and Traces F and G are the Q1 and Q2 collectors, respectively. Trace H is L1's high voltage output. The waveforms show that the synchronous drive to the resonant high voltage converter produces a clean sine wave output. The driven, fully synchronous operation eliminates phase jitter under all conditions. This circuit has the same excellent power supply rejection and regulation characteristics of the Royer based approach.

A potential drawback to this approach is that the resonant frequency of the high voltage converter changes with lamp operating current. The Royer based circuits inherently change frequency in response to this, maintaining on-resonance operation. This contributes to high efficiency operation over a broad range of lamp currents. This circuit's fixed frequency drive means that on-resonance operation only occurs at one lamp current. In practice, C1 and C2 set the "true" resonant operating point at any desired current. Efficiency falls off at other currents because the high voltage converter is forced to run off-resonance.

Figure 36's plot shows the effects of this on efficiency. Curve A results with the circuit optimized at 3mA lamp current (1/2 power), while Curve B represents optimization at 6mA (full power). In both cases, efficiency suffers at currents away from these points. Curve C shows a Royer based circuit's performance for comparison.

The circuit is also sensitive to C1 and C2 tolerances. A 10% total tolerance deviation can cause 4% efficiency degradation at the nominally optimized current.

Note: *This application note was derived from a manuscript originally prepared for publication in EDN Magazine.*

References

1. Howard, Rowland, "You Never Miss the Water," Petersons Magazine, 1876.
2. Bright, Pittman and Royer, "Transistors as On-Off Switches in Saturable Core Circuits," Electrical Manufacturing, December 1954. Available from Technomic Publishing, Lancaster, PA.
3. Sharp Corporation, "Flat Panel Displays," 1991.
4. C. Kitchen, L. Counts, "RMS-to-DC Conversion Guide," Analog Devices, Inc., 1986.
5. Williams, Jim, "A Monolithic IC for 100MHz RMS-DC Conversion," Linear Technology Corporation, Application Note 22, September 1987.
6. Hewlett-Packard, "1968 Instrumentation. Electronic-Analytical-Medical," AC Voltage Measurement, p. 197-198, 1968.
7. Hewlett-Packard, "Model 3400RMS Voltmeter Operating and Service Manual," 1965.
8. Hewlett-Packard, "Model 3403C True RMS Voltmeter Operating and Service Manual," 1973.
9. Ott, W.E., "A New Technique of Thermal RMS Measurement," IEEE Journal of Solid State Circuits, December 1974.
10. Williams, J.M. and Longman, T.L., "A 25MHz Thermally Based RMS-DC Converter," 1986 IEEE ISSCC Digest of Technical Papers.
11. O'Neill, P.M., "A Monolithic Thermal Converter," H.P. Journal, May 1980.
12. Williams, J., "Thermal Techniques in Measurement and Control Circuitry," "50MHz Thermal RMS-DC Converter," Linear Technology Corporation, Application Note 5, December 1984.
13. Williams, J. and Huffman, B., "Some Thoughts on DC-DC Converters," Appendix A, "The +5 to ±15V Converter—A Special Case." Linear Technology Corporation, Application Note 29. October 1988.
14. Baxendall, P.J., "Transistor Sine-Wave LC Oscillators," British Journal of IEEE, February 1960, Paper No. 2978E.
15. Williams, J., "Temperature Controlling to Microdegrees," Massachusetts Institute of Technology, Education Research Center, 1971 (out of print).
16. Fulton, S.P., "The Thermal Enzyme Probe," Thesis, Massachusetts Institute of Technology, 1975.
17. Williams, J., "Designer's Guide to Temperature Measurement," Part II, EDN, May 20, 1977.
18. Williams, J., "Illumination Circuitry for Liquid Crystal Displays," Linear Technology Corporation, Application Note 49. August 1992.
19. Olsen, J.V., "A High Stability Temperature Controlled Oven," Thesis, Massachusetts Institute of Technology, 1974.
20. "The Ultimate Oven," MIT Reports on Research, March 1972.
21. McDermott, James, "Test System at MIT Controls Temperature to Microdegrees," Electronic Design, January 6, 1972.

APPENDIX A

"HOT" CATHODE FLUORESCENT LAMPS

Many CCFL characteristics are shared by so-called "Hot" Cathode Fluorescent Lamps (HCFLs). The most significant difference is that HCFLs contain filaments at each end of the lamp (see Figure A1). When the filaments are powered they emit electrons, lowering the lamp's ionization potential. This means a significantly lower voltage will start the lamp. Typically the filaments are turned on, a relatively modest voltage impressed across the lamp, and start-up occurs. Once the lamp starts, filament power is removed. Although HCFLs reduce the high voltage requirement they require a filament supply and sequencing circuitry. The CCFL circuits shown in the text will start and run HCFLs without using the filaments. In practice this involves simply driving the filament connections at the HCFL ends as if they were CCFL electrodes.

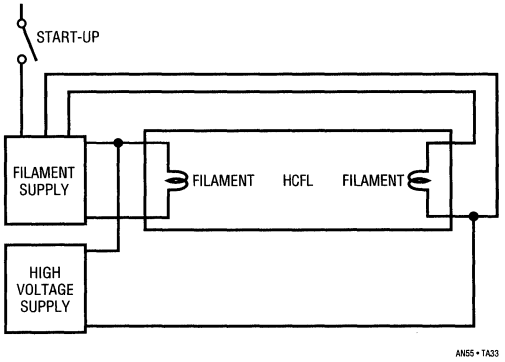


Figure A1. A Conceptual Hot Cathode Fluorescent Lamp Power Supply. Heated Filaments Liberate Electrons, Lowering the Lamp's Start-Up Voltage Requirement. CCFL Supply Discussed in Text Eliminates Filament Supply

APPENDIX B

MECHANICAL DESIGN CONSIDERATIONS FOR LIQUID CRYSTAL DISPLAYS

Charles L. Guthrie, Sharp Electronics Corporation

Introduction

As more companies begin the manufacturing of their next generation of computers, there is a need to reduce the overall size and weight of the units to improve their portability. This has sparked the need for more compact designs where the various components are placed in closer proximity, thus making them more susceptible to interaction from signal noise and heat dissipation. The following is a summary of guidelines for the placement of the display components and suggestions for overcoming difficult design constraints associated with component placement.

In notebook computers the thickness of the display housing is important. The design usually requires the display to be in a pivotal structure so that the display may be folded down over the keyboard for transportation. Also, the outline dimensions must be minimal so that the package will remain as compact as possible. These two constraints drive the display housing design and placement of the display components. This discussion surveys each of the problems facing the designer in detail and offers suggestions for overcoming the difficulties to provide a reliable assembly.

The problems facing the pen based computer designer are similar to those realized in notebook designs. In addition, however, pen based designs require protection for the face of the display. In pen based applications, as the pen is moved across the surface of the display, the pen has the potential for scratching the front polarizer. For this reason the front of the display must be protected. Methods for protecting the display face while minimizing effects on the display image are given.

Additionally, the need to specify the flatness of the bezel is discussed. Suggestions for acceptable construction techniques for sound design are included. Further, display components likely to cause problems due to heat buildup are identified and methods for minimization of the heat's effects are presented.

The ideas expressed here are not the only solutions to the various problems and have not been assessed as to whether they may infringe on any patents issued or applied for.

Flatness and Rigidity of the Bezel

In the notebook computer the bezel has several distinct functions. It houses the display, the inverter for the backlight, and in some instances, the controls for contrast and brightness of the display. The bezel is usually designed to tilt to set the optimum viewing angle for the display.

It is important to understand that the bezel must provide a mechanism to keep the display flat, particularly at the mounting holds. Subtle changes in flatness place uneven stress on the glass which can cause variations in contrast across the display. Slight changes in pressure may cause significant variation in the display contrast. Also, at the extreme, significantly uneven pressures can cause the display glass to fail.

Because the bezel must be functional in maintaining the flatness of the display, consideration must be made for the strength of the bezel. Care must be taken to provide structural members, while minimizing the weight of the unit. This may be executed using a parallel grid, normal to the edges of the bezel, or angled about 45° off of the edges of the bezel. The angled structure may be more desirable in that it provides resistance to torquing the unit while lifting the cover with one hand. Again, the display is sensitive to stresses from uneven pressure on the display housing.

Another structure which will provide excellent rigidity, but adds more weight to the computer, is a "honeycomb" structure. This "honeycomb" structure resists torquing from all directions and tends to provide the best protection for the display.

With each of these structures it is easy to provide mounting assemblies for the display. "Blind nuts" can be molded into the housing. The mounting may be done to either the front or rear of the bezel. Attachment to the rear may provide better rigidity for placement of the mounting hardware.

One last caution is worth noting in the development of a bezel. The bezel should be engineered to absorb most of the shock and vibration experienced in a portable computer. Even though the display has been carefully designed, the notebook computer presents extraordinary shock and abuse problems.

Avoiding Heat Buildup in the Display

Several of the display components are sources for heat problems. Thermal management must be taken into account in the design of the display bezel. A heated display may be adversely affected; a loss of contrast uniformity usually results. The Cold Cathode Fluorescent Tube (CCFT) itself gives off a small amount of heat relative to the amount of power dissipated in its glow discharge. Likewise, even though the inverters are designed to be extremely efficient, there is some heat generated. The buildup of heat in these components will be aggravated by the typically "tight" designs currently being introduced. There is little ventilation designed into most display bezels. To compound the problem, the plastics used are poor thermal conductors, thus causing the heat to build up which may affect the display.

Some current designs suffer from poor placement of the inverter and/or poor thermal management techniques. These designs can be improved, even where redesign of the display housing, with improved thermal management, is impractical.

One of the most common mistakes in current designs is that there has been no consideration for the buildup of heat from the CCFT. Typically, the displays for notebook applications have only one CCFT to minimize display power requirements. The lamp is usually placed along the right edge of the display. Since the lamp is placed very close to the display glass, it can cause a temperature rise in the liquid crystal. It is important to note that variations in temperature of as little as 5°C can cause an apparent nonuniformity in display contrast. Variations caused by slightly higher temperature variations will cause objectionable variations in the contrast and display appearance.

To further aggravate the situation, some designs have the inverter placed in the bottom of the bezel. This has a tendency to cause the same variations in contrast, particularly when the housing does not have any heat sinking for the inverter. This problem manifests itself as a "blooming" of the display, just above the inverter. This "blooming"

looks like a washed out area where, in the worst case, the characters on the display fade completely.

The following section discusses the recommended methods for overcoming these design problems.

Placement of the Display Components

One of the things that can be done is to design the inverter into the base of the computer with the motherboard. In some applications this is impractical because this requires the high voltage leads to be mounted within the hinges connecting the display bezel to the main body. This causes a problem with strain relief of the high voltage leads, and thus with UL certification.

One mistake, made most often, is placing the inverter at the bottom of the bezel next to the lower edge of the display. It is a fact that heat rises, yet this is one of the most overlooked problems in new notebook designs. Even though the inverters are very efficient, some energy is lost in the inverter in the form of heat. Because of the insulating properties of the plastic materials used in the bezel construction, heat builds up and affects the display contrast.

Designs with the inverter at the bottom can be improved in one of three ways. The inverter can be relocated away from the display, heat sinking materials can be placed between the display and the inverter, or ventilation can be provided to remove the heat.

In mature designs, it may be impractical to do what is obvious and move the inverter up to the side of the display towards the top of the housing. In these cases, the inverter may be insulated from the display with a "heat dam." One method of accomplishing this would be to use a piece of mica insulator die cut to fit tightly between the inverter and the display. This heat dam would divert the heat around the end of the display bezel to rise harmlessly to the top of the housing. Mica is recommended in this application because of it's thermal and electrical insulation properties.

The last suggestion for removing heat is to provide some ventilation to the inverter area. This has to be done very carefully to prevent exposing the high voltage. Ventilation may not be a practical solution because resistance to liquids and dust is compromised.

The best solution for the designer of new hardware is to consider the placement of the inverter to the side of the display and at the top of the bezel. In existing designs of this type the effects of heat from the inverter, even in tight housings, has been minimal or non-existent.

One problem which is aggravated by the placement of the inverter at the bezel is heat dissipated by the CCFT. In designs where the inverter is placed up and to the side of the display, fading of the display contrast due to CCFT heat is not a problem. However, when the inverter is placed at the bezel bottom, some designs experience a loss of contrast aggravated by the heat from the CCFT and inverter.

In cases where the inverter must be left at the bottom, and the CCFT is causing a loss of contrast, the problem can be minimized by using an aluminum foil heat sink. This does not remove the heat from the display, but dissipates it over the entire display area, thus normalizing the display contrast. The aluminum foil is easy to install and in some present designs has successfully improved the display contrast.

Remember that the objection to the contrast variation stems more from non-uniformity than from a total loss of contrast.

Protecting the Face of the Display

One of the last considerations in the design of notebook and pen based computers is protection of the display face. The front polarizer is made of a mylar base and thus is susceptible to scratching. The front protection for the display, along with providing scratch protection, may also provide an anti-glare surface.

There are several ways that scratch resistance and anti-glare surfaces can be incorporated. A glass or plastic cover may be placed over the display, thus providing protection. The material should be placed as close to the display as possible to minimize possible parallax problems due to reflections off of the cover material. With anti-glare materials, the further the material is from the front of the display the greater the distortion.

In pen applications, the front anti-scratch material is best placed in contact with the front glass of the display. The cover glass material normally needs to be slightly thicker

to protect the display from distortion when pressure is being exerted on the front.

There are several methods for making the pen input devices. Some use the front surface of the cover glass to provide input data and some use a field effect to a printed wiring board on the back of the display. When the pen input is on the front of the display, the input device is usually on a glass surface.

To limit specular reflection in this application, the front cover glass should be bonded to the display. Care must be taken to insure that the coefficient of thermal expansion is matched for all of the materials used in the system. Because of the difficulties encountered with the bonding of the cover glass, and the potential to destroy the display through improper workmanship, consulting an expert is strongly recommended.

APPENDIX C

ACHIEVING MEANINGFUL EFFICIENCY MEASUREMENTS

Obtaining reliable efficiency data for the CCFL circuits presents a high order difficulty measurement problem. Establishing and maintaining accurate AC measurements is a textbook example of attention to measurement technique. The combination of high frequency, harmonic laden waveforms and high voltage makes meaningful results difficult to obtain. The choice, understanding and use of test instrumentation is crucial. Clear thinking is needed to avoid unpleasant surprises![1]

Probes

The probes employed must faithfully respond over a variety of conditions. Measuring across the resistor in series with the CCFL is the most favorable circumstance. This low voltage, low impedance measurement allows use of a standard 1X probe. The probe's relatively high input capacitance does not introduce significant error. A 10X probe may also be used, but frequency compensation issues (discussion to follow) must be attended to.

The high voltage measurement across the lamp is considerably more demanding on the probe. The waveform fundamental is at 20kHz to 100kHz, with harmonics into the MHz region. This activity occurs at peak voltages in the kilovolt range. The probe must have a high fidelity response under these conditions. Additionally, the probe should have low input capacitance to avoid loading effects which would corrupt the measurement. The design and construction of such a probe requires significant attention. Figure C1 lists some recommended probes along with their characteristics. As stated in the text, almost all standard oscilloscope probes *will fail*[2] if used for this measurement. Attempting to circumvent the probe requirement by resistively dividing the lamp voltage also creates problems. Large value resistors often have significant voltage coefficients and their shunt capacitance is high and uncertain. As such, simple voltage dividing is not recommended. Similarly, common high voltage probes intended for DC measurement will have large errors because of AC effects. The P6013A and P6015 are the favored probes; their 100MΩ input and small capacitance introduces low loading error. The penalty for their 1000X attenuation is reduced output, but the recommended voltmeters (discussion to follow) can accommodate this.

All of the recommended probes are designed to work into an oscilloscope input. Such inputs are almost always 1MΩ paralleled by (typically) 10pF-22pF. The recommended voltmeters, which will be discussed, have significantly different input characteristics. Figure C2's table shows higher input resistances and a range of capacitances. Because of this the probe must be compensated for the voltmeter's input characteristics. Normally, the optimum compensation point is easily determined and adjusted by observing probe output on an oscilloscope. A known amplitude square wave is fed in (usually from the oscilloscope calibrator) and the probe adjusted for correct response. Using the probe with the voltmeter presents an unknown impedance mismatch and raises the problem of determining when compensation is correct.

Note 1: It is worth considering that various constructors of text Figure 6 have reported efficiencies ranging from 8% to 115%.

Note 2: That's twice we've warned you nicely.

TEKTRONIX PROBE TYPE	ATTENUATION FACTOR	ACCURACY	INPUT RESISTANCE	INPUT CAPACITANCE	RISE TIME	BAND-WIDTH	MAXIMUM VOLTAGE	DERATED ABOVE	DERATED TO AT FREQUENCY	COMPENSATION RANGE	ASSUMED TERMINATION RESISTANCE
P6007	100X	3%	10MΩ	2.2pF	14ns	25MHz	1.5kV	200kHz	$700V_{RMS}$ at 10MHz	15-55pF	1M
P6009	100X	3%	10MΩ	2.5pF	2.9ns	120MHz	1.5kV	200kHz	$450V_{RMS}$ at 40MHz	15-47pF	1M
P6013A	1000X	Adjustable	100MΩ	3pF	7ns	50MHz	12kV	100kHz	$800V_{RMS}$ at 20MHz	12-60pF	1M
P6015	1000X	Adjustable	100MΩ	3pF	4.7ns	75MHz	20kV	100kHz	$2000V_{RMS}$ at 20MHz	12-47pF	1M

Figure C1. Characteristics of some Wideband High Voltage Probes. Output Impedances are Designed for Oscilloscope Inputs

MANUFACTURER AND MODEL	FULL SCALE RANGES	ACCURACY AT 1MHz	ACCURACY AT 100kHz	INPUT RESISTANCE AND CAPACITANCE	MAXIMUM BANDWIDTH	CREST FACTOR
Hewlett-Packard 3400 Meter Display	1mV to 300V, 12 Ranges	1%	1%	0.001V to 0.3V Range = 10M and < 50pF, 1V to 300V Range = 10M and < 20pF	10MHz	10:1 At Full Scale, 100:1 At 0.1 Scale
Hewlett-Packard 3403C Digital Display	10mV to 1000V, 6 Ranges	0.5%	0.2%	10mV and 100mV Range = 20M and 20pF ±10%, 1V to 1000V Range = 10M and 24pF ±10%	100MHz	10:1 At Full Scale, 100:1 At 0.1 Scale
Fluke 8920A Digital Display	2mV to 700V, 7 Ranges	0.7%	0.5%	10M and < 30pF	20MHz	7:1 At Full Scale, 70:1 At 0.1 Scale

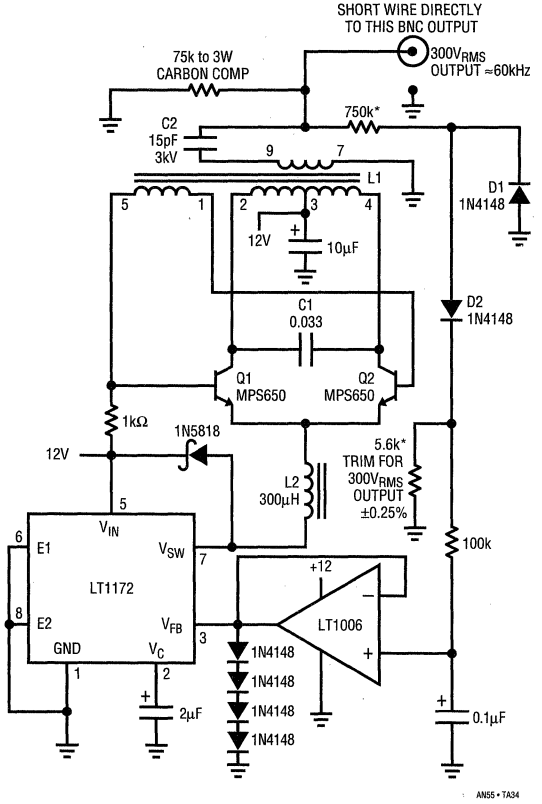
Figure C2. Pertinent Characteristics of some Thermally Based RMS Voltmeters. Input Impedances Necessitate Matching Network and Compensation for High Voltage Probes

The impedance mismatch occurs at low and high frequency. The low frequency term is corrected by placing an appropriate value resistor in shunt with the probe's output. For a 10MΩ voltmeter input a 1.1MΩ resistor is suitable. This resistor should be built into the smallest possible BNC equipped enclosure to maintain a coaxial environment. No cable connections should be employed; the enclosure should be placed *directly* between the probe output and the voltmeter input to minimize stray capacitance. This arrangement compensates the low frequency impedance mismatch. Figure C4 shows the impedance matching box attached to the high voltage probe.

Correcting the high frequency mismatch term is more involved. The wide range of voltmeter input capacitances combined with the added shunt resistor's effects presents problems. How is the experimenter to know where to set the high frequency probe compensation adjustment? One solution is to feed a known value RMS signal to the probe-voltmeter combination and adjust compensation for a proper reading. Figure C3 shows a way to generate a known RMS voltage. This scheme is simply a standard backlight circuit reconfigured for a constant voltage output. The op amp permits low RC loading of the 5.6k feedback termination without introducing bias current error. The 5.6kΩ value may be series or parallel trimmed for a 300V output. Stray parasitic capacitance in the feedback network affects output voltage. Because of this, all feedback associated nodes and components should be rigidly fixed and the entire circuit built into a small metal box. This prevents any significant change in the parasitic terms. The result is a known $300V_{RMS}$ output.

Now, the probe's compensation is adjusted for a 300V voltmeter indication using the shortest possible connection (e.g., BNC-to-probe adapter) to the calibrator box. This procedure, combined with the added resistor, completes the probe-to-voltmeter impedance match. If the probe compensation is altered (e.g., for proper response on an oscilloscope) the voltmeter's reading will be erroneous.[3] It is good practice to verify the calibrator box output before and after every set of efficiency measurements. This is done by *directly* connecting, via BNC adapters, the calibrator box to the RMS voltmeter on the 1000V range.

Note 3: The translation of this statement is to hide the probe when you are not using it. If anyone wants to borrow it, look straight at them, shrug your shoulders and say you don't know where it is. This is decidedly dishonest, but eminently practical. Those finding this morally questionable may wish to re-examine their attitude after producing a day's worth of worthless data with a probe that was unknowingly readjusted.



C1 = MUST BE A LOW LOSS CAPACITOR.
METALIZED POLYCARB
WIMA FKP2 OR MKP-20 (GERMAN) RECOMMENDED
L1 = SUMIDA 6345-020 OR COILTRONICS CTX110092-1
PIN NUMBERS SHOWN FOR COILTRONICS UNIT
L2 = COILTRONICS CTX300-4
Q1, Q2 = AS SHOWN OR BCP 56 (PHILLIPS SO PACKAGE)
* = 1% FILM RESISTOR (TEN 75kΩ RESISTORS IN SERIES)
DO NOT SUBSTITUTE COMPONENTS

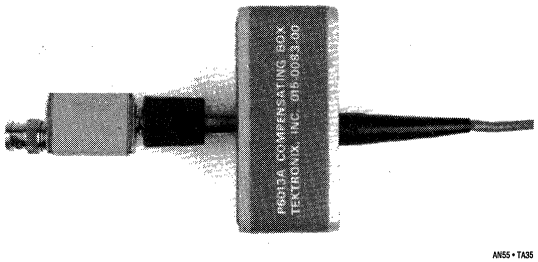
COILTRONICS (305) 781-8900, SUMIDA (708) 956-0666

Figure C3. High Voltage RMS Calibrator is Voltage Output Version of CCFL Circuit

RMS Voltmeters

The efficiency measurements require an RMS responding voltmeter. This instrument must respond accurately at high frequency to irregular and harmonically loaded waveforms. These considerations eliminate almost all AC voltmeters, including DVMs with AC ranges.

There are a number of ways to measure RMS AC voltage. Three of the most common include *average, logarithmic,*



AN55 • TA35

Figure C4. The Impedance Matching Box (Extreme Left) Mated to the High Voltage Probe. Note Direct Connection. No Cable is used

and *thermally* responding. Averaging instruments are calibrated to respond to the average value of the input waveform, which is almost always assumed to be a sine wave. Deviation from an ideal sine wave input produces errors. Logarithmically based voltmeters attempt to overcome this limitation by continuously computing the input's true RMS value. Although these instruments are "real time" analog computers their 1% error bandwidth is well below 300kHz and crest factor capability is limited. Almost all general purpose DVMs use such a logarithmically based approach and, as such, are not suitable for CCFL efficiency measurements. Thermally based RMS voltmeters are direct acting thermo-electronic analog computers. They respond to the input's RMS heating value. This technique is explicit, relying on the very definition of RMS (e.g., the heating power of the waveform). By turning the input into heat, thermally based instruments achieve vastly higher bandwidth than other techniques.[4] Additionally, they are insensitive to waveform shape and easily accommodate large crest factors. These characteristics are necessary for the CCFL efficiency measurements.

Figure C5 shows a conceptual thermal RMS-DC converter. The input waveform warms a heater, resulting in increased output from its associated temperature sensor. A DC amplifier forces a second, identical, heater-sensor pair to the same thermal conditions as the input driven pair. This differentially sensed, feedback enforced loop makes ambient temperature shifts a common mode term, eliminating their effect. Also, although the voltage and thermal interaction is nonlinear, the input-output RMS voltage relationship is linear with unity gain.

Note 4: Those finding these descriptions intolerably brief are commended to References 4, 5 and 6.

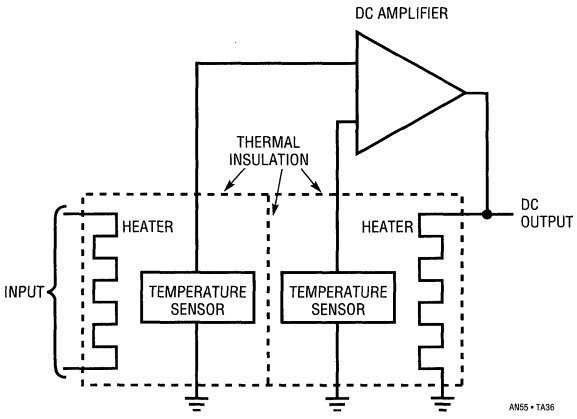


Figure C5. Conceptual Thermal RMS-DC Converter

The ability of this arrangement to reject ambient temperature shifts depends on the heater-sensor pairs being isothermal. This is achievable by thermally insulating them with a time constant well below that of ambient shifts. If the time constants to the heater-sensor pairs are matched, ambient temperature terms will affect the pairs equally in phase and amplitude. The DC amplifier rejects this common mode term. Note that, although the pairs are isothermal, they are insulated from each other. Any thermal interaction between the pairs reduces the system's thermally based gain terms. This would cause unfavorable signal-to-noise performance, limiting dynamic operating range.

Figure C5's output is linear because the matched thermal pair's nonlinear voltage-temperature relationships cancel each other.

The advantages of this approach have made its use popular in thermally based RMS-DC measurements.

The instruments listed in Figure C2, while considerably more expensive than other options, are typical of what is required for meaningful results. The HP3400A and the Fluke 8920A are currently available from their manufacturers. The HP3403C, an exotic and highly desirable instrument, is no longer produced but readily available on the secondary market.

Figure C6 shows equipment in a typical efficiency test set-up. The RMS voltmeters (photo center and left) read output voltage and current via high voltage (left) and standard 1X probes (lower left). Input voltage is read on a DVM (upper right). A low loss clip-on ammeter (lower right) determines input current. The CCFL circuit and LCD display are in the foreground. Efficiency, the ratio of input to output power, is computed with a hand held calculator (lower right).

Calorimetric Correlation of Electrical Efficiency Measurements

Careful measurement technique permits a high degree of confidence in the efficiency measurement's accuracy. It is, however, a good idea to check the method's integrity by measuring in a completely different domain. Figure C7 does this by calorimetric techniques. This arrangement, identical to the thermal RMS voltmeter's operation (Figure C5), determines power delivered by the CCFL circuit by measuring its load temperature rise. As in the thermal RMS voltmeter a differential approach eliminates ambient temperature as an error term. The differential amplifier's output, assuming a high degree of matching in the two thermal enclosures, proportions to load power. The ratio of the two cell's $E \times I$ products yields efficiency information. In a 100% efficient system the amplifier's output energy would equal the power supply's output. Practically it is always less, as the CCFL circuit has losses. This term represents the desired efficiency information.

Figure C8 is similar except that the CCFL circuit board is placed within the calorimeter. This arrangement nominally yields the same information, but is a much more demanding measurement because far less heat is generated. The signal-to-noise (heat rise above ambient) ratio is unfavorable, requiring almost fanatical attention to thermal and instrumentation considerations.[5] It is significant that the *total* uncertainty between electrical and both calorimetric efficiency determinations was 3.3%. The two thermal approaches differed by about 2%. Figure C9 shows the calorimeter and its electronic instrumentation. Descriptions of this instrumentation and thermal measurements can be found in the References section following the main text.

Note 5: Calorimetric measurements are not recommended for readers who are short on time or sanity.

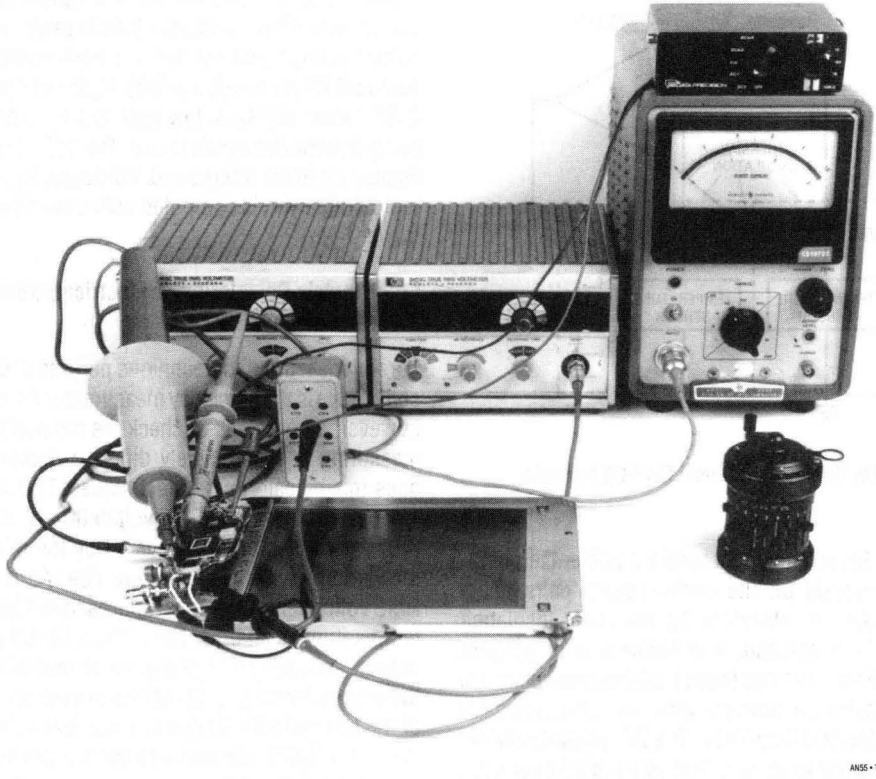


Figure C6. Typical Efficiency Measurement Instrumentation. RMS Voltmeters (Center Left) Measure Output Voltage and Current via Appropriate Probes. Clip-On Ammeter (Right) Gives Low Loss Input Current Readings. DVM (Upper Right) Measures Input Voltage. Hand Calculator (Lower Right) is used to Compute Efficiency

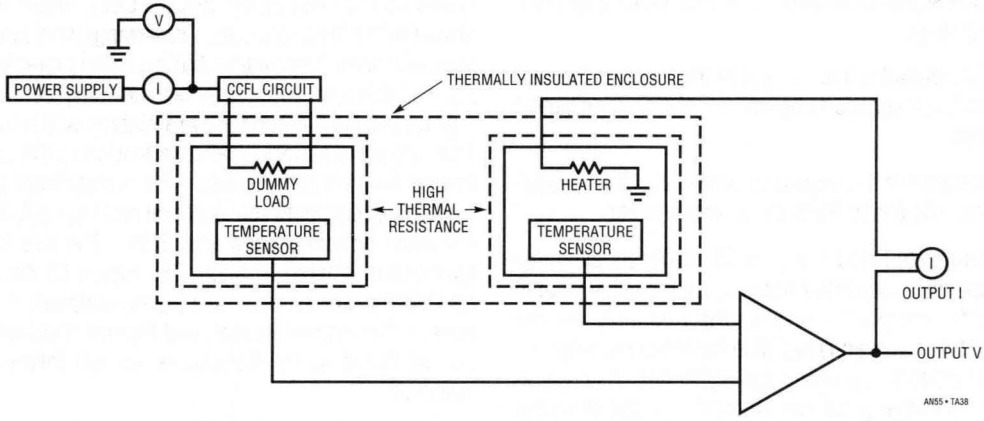


Figure C7. Efficiency Determination via Calorimetric Measurement. Ratio of Power Supply to Output Energy Gives Efficiency Information

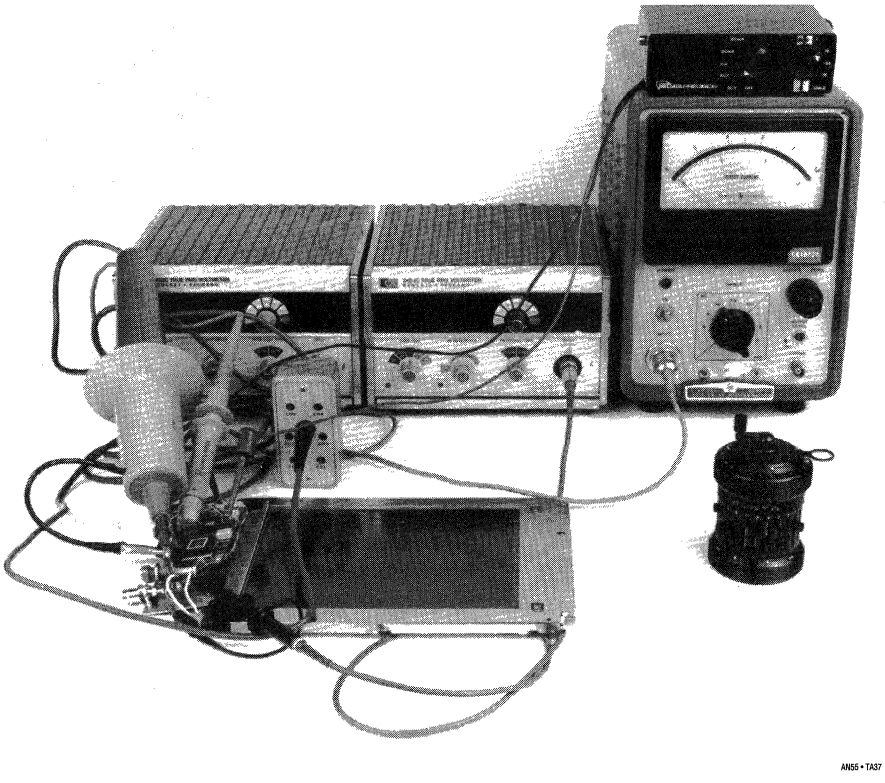


Figure C6. Typical Efficiency Measurement Instrumentation. RMS Voltmeters (Center Left) Measure Output Voltage and Current via Appropriate Probes. Clip-On Ammeter (Right) Gives Low Loss Input Current Readings. DVM (Upper Right) Measures Input Voltage. Hand Calculator (Lower Right) is used to Compute Efficiency

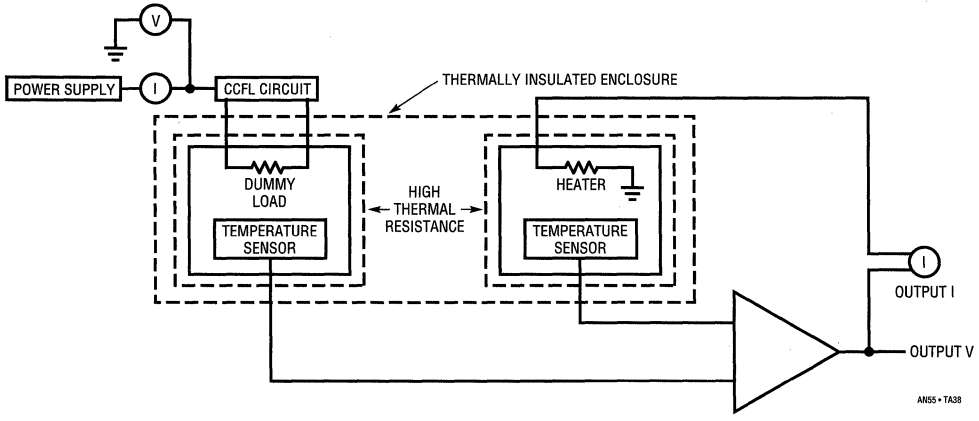


Figure C7. Efficiency Determination via Calorimetric Measurement. Ratio of Power Supply to Output Energy Gives Efficiency Information

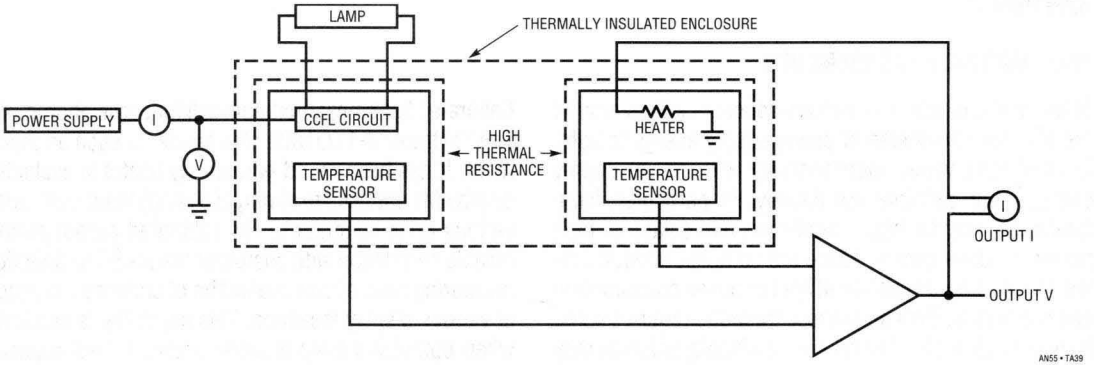


Figure C8. The Calorimeter Measures Efficiency by Determining Circuit Heating Losses

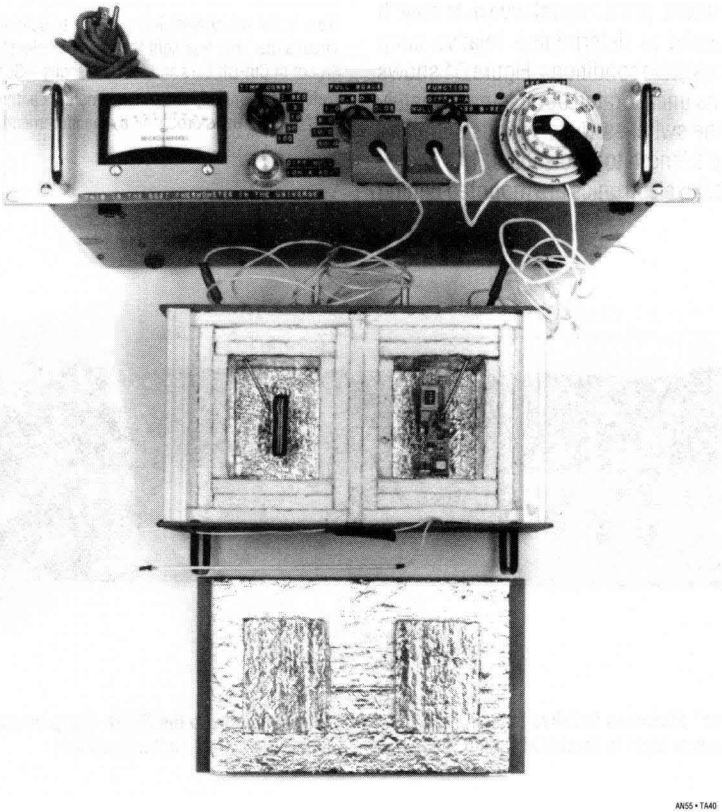


Figure C9. The Calorimeter (Center) and its Instrumentation (Top). Calorimeter's High Degree of Thermal Symmetry Combined with Sensitive Servo Instrumentation Produces Accurate Efficiency Measurements. Lower Portion of Photo is Calorimeter's Top Cover

APPENDIX D

PHOTOMETRIC MEASUREMENTS

In the final analysis, the ultimate concern centers around the efficient conversion of power supply energy to light. Emitted light varies monotonically with power supply energy,[1] but certainly not linearly. In particular, lamp luminosity may be highly nonlinear, particularly at high power, vs drive power. There are complex tradeoffs involving the amount of emitted light vs power consumption and battery life. Evaluating these tradeoffs requires some form of photometer. The relative luminosity of lamps may be evaluated by placing the lamp in a light tight tube and sampling its output with photodiodes. The photodiodes are placed along the lamp's length and their outputs electrically summed. This sampling technique is an uncalibrated measurement, providing relative data only. It is, however, quite useful in determining relative lamp emittance under various drive conditions. Figure D1 shows this "glometer," with its uncalibrated output appropriately scaled in "brights." The switches allow various sampling diodes along the lamp's length to be disabled. The photodiode signal conditioning electronics are mounted behind the switch panel.

Calibrated light measurements call for a true photometer. The Tektronix J-17/J1803 photometer is such an instrument. It has been found particularly useful in evaluating display (as opposed to simply the lamp) luminosity under various drive conditions. The calibrated output permits reliable correlation with customer results.[2] The light tight measuring head allows evaluation of emittance evenness at various display locations. This capability is invaluable when optimizing lamp location and/or ballast capacitor values in dual lamp displays.

Figure D2 shows the photometer in use evaluating a display.

Note 1: But not always! It is possible to build highly electrically efficient circuits that emit less light than "less efficient" designs. See Appendix J, "A Lot of Cut-Off Ears and No Van Goghs—Some Not-So-Great Ideas."

Note 2: It is unlikely customers would be enthusiastic about correlating the "brights" units produced by the aforementioned glometer.

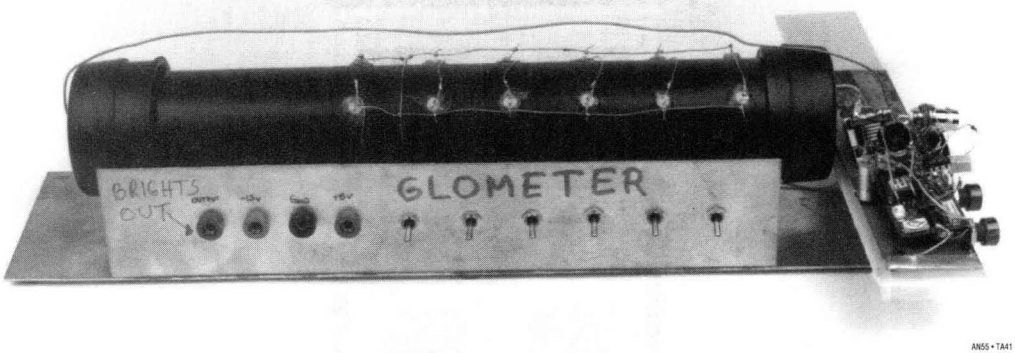


Figure D1. The "Glometer" Measures Relative Lamp Emissivity. CCFL Circuit Mounts to the Right. Lamp is Inside Cylindrical Housing. Photodiodes (Center) Convert Light to Electrical Output (Lower Left) via Amplifiers (Not Visible in Photo)

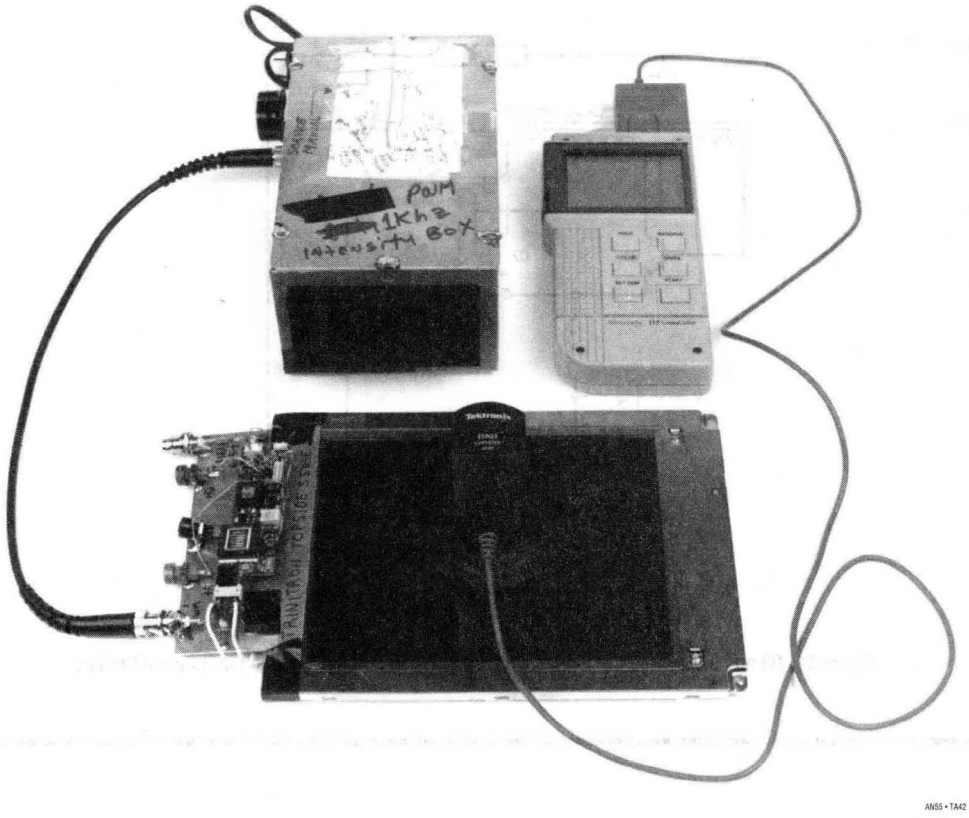


Figure D2. Apparatus for Calibrated Photometric Display Evaluation. Photometer (Upper Right) Indicates Display Luminosity via Sensing Head (Center). CCFL Circuit (Left) Intensity is Controlled by a Calibrated Pulse Width Generator (Upper Left)

APPENDIX E

OPEN LAMP PROTECTION

The CCFL circuit's current source output means that "open" or broken lamps cause full output voltage to appear. If this is objectionable Figure E1's modification may be employed. Q3 and associated components form a simple voltage mode feedback loop that operates if V_Z turns on. If T1 sees no load, there is no feedback and the Q1-Q2 pair receive full drive. Collector voltage rises to abnormal levels, and V_Z biases via Q1's V_{BE} path. Q1's collector current drives the feedback node and the circuit finds a stable operating point. This action controls Royer drive, and hence output voltage. Q3's sensing across the Royer provides power supply rejection. V_Z's value should be somewhat above the worst case Q1-Q2 V_{CE} voltage under running conditions. It is desirable to select V_Z's value so clamping occurs at the lowest output voltage possible while still permitting lamp start-up. This is not as tricky as it sounds because the 10k-1µF RC delays the effects of Q3's turn-on. Usually, selecting V_Z several volts above the worst case Q1-Q2 V_{CE} will suffice.

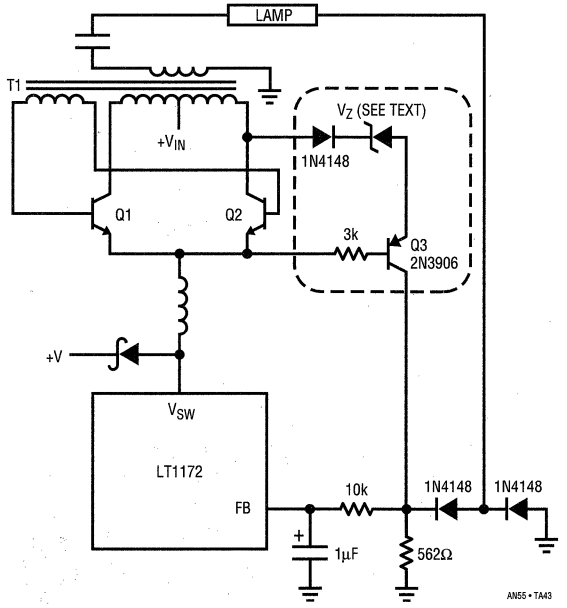


Figure E1. Q3 and Associated Components form a Local Regulating Loop to Limit Output Voltage

APPENDIX F

INTENSITY CONTROL AND SHUTDOWN METHODS

Figure F1 shows a variety of methods for shutting down and controlling intensity of the CCFL circuits. Pulling the LT1172 V_C pin to ground puts the circuit into micropower shutdown. In this mode about 50µA flows into the LT1172 V_{IN} pin with essentially no current drawn from the main (Royer center tap) supply. Turning off V_{IN} power eliminates the LT1172's 50µA drain.

Three basic ways to control intensity appear in the figure. The most common intensity control method is to add a potentiometer in series with the feedback termination. When using this method insure that the minimum value (in this case 562Ω) is a 1% unit. If a wider tolerance resistor is used the lamp current, at maximum intensity setting, will vary appropriately.

Pulse width modulation or variable DC is sometimes used for intensity control. Two interfaces work well. Directly driving the feedback pin via a diode—22k resistor with DC or PWM produces intensity control. The other method shown is similar, but places the 1µf capacitor outside the feedback loop to get best turn-on transient response. This is the best method if output overshoot must be minimized. See the main text section, "Feedback Loop Stability Issues" for pertinent discussion.

Figure F2 shows a simple circuit which generates precision variable pulse widths. This capability is useful when testing PWM based intensity schemes. The circuit is basically a closed loop pulse width modulator. The crystal controlled 1kHz input clocks the C1-Q1 ramp generator via

the differentiator—CMOS inverter network and the LTC201 reset switch. C1's output drives a CMOS inverter to furnish the output. The output is resistively sampled, averaged and presented to A1's negative input. A1 compares this signal with a variable voltage from the potentiometer. A1's output biases the pulse width modulator, closing a loop around it. The CMOS inverter's purely ohmic output structure combines with A1's ratiometric operation (e.g., both of A1's input signals derive from the +5V supply) to hold pulse width constant. Variations in time, temperature and supply have essentially no effect. The potentiometer's setting is the sole determinant of output pulse width. The Schottky diodes protect the output from latch-up due to cable induced ESD or accidental events[1] during testing.

The output width is calibrated by monitoring it with a counter while adjusting the 2kΩ trim pot.

As mentioned, the circuit is insensitive to power supply variation. However, the CCFL circuit averages the PWM output. It cannot distinguish between a duty cycle shift and supply variation. As such, the test box's 5V supply should be trimmed ±0.01V. This simulates a "design centered" logic supply under actual operating conditions. Similarly, paralleling additional logic inverters to get lower output impedance should be avoided. In actual use, the CCFL dimming port will be driven from a single CMOS output, and its impedance characteristics must be accurately mimicked.

Note 1: "Accidental events" is a nice way of referring to the stupid things we all do at the bench. Like shorting a CMOS logic output to a –15V supply (then I installed the diodes).

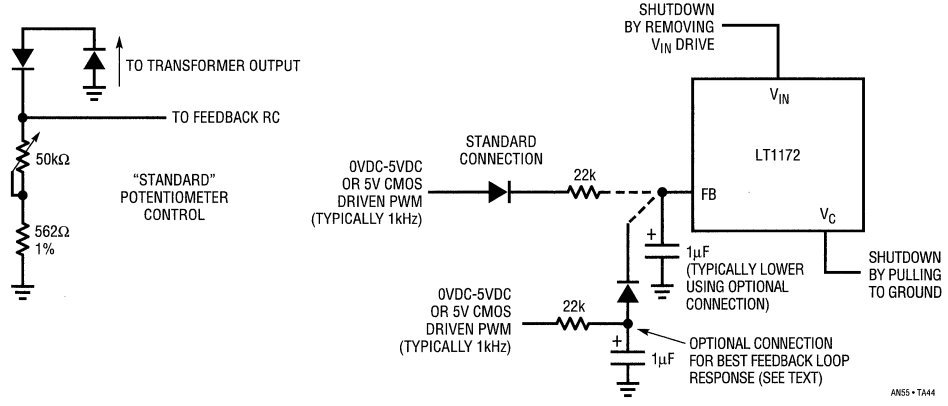


Figure F1. Various Options for Shutdown and Intensity Control

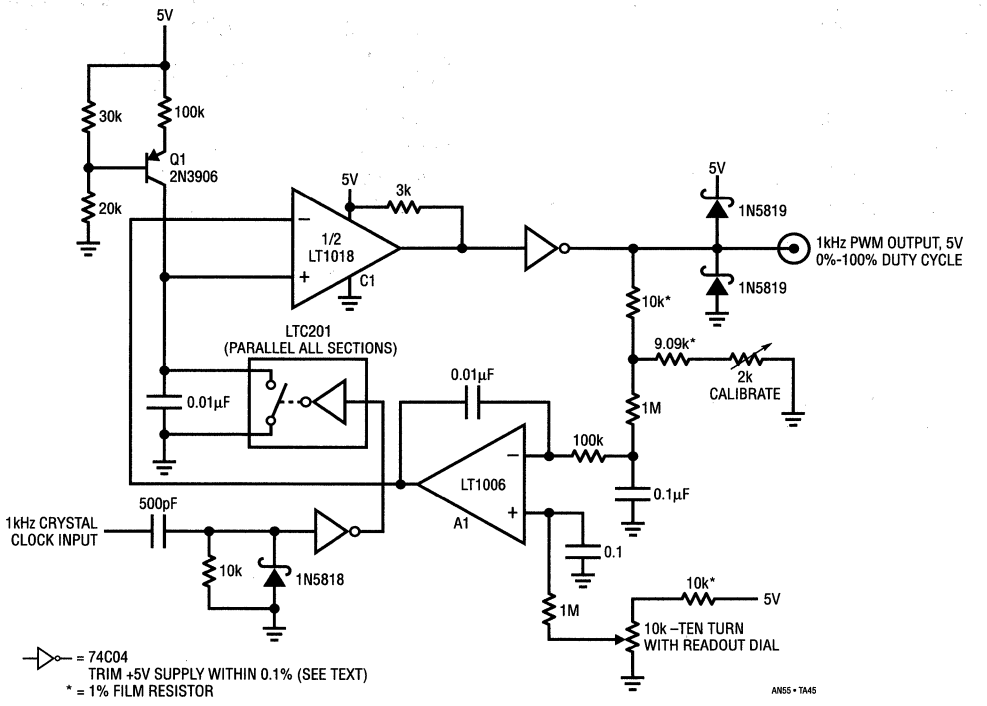


Figure F2. The Calibrated Pulse Width Test Box. A1 Controls C1 Based Pulse Width Modulator, Stabilizing its Operating Point

APPENDIX G

OPERATION FROM HIGH VOLTAGE INPUTS

Some applications require higher input voltages. The 20V maximum input specified in the figures is set by the LT1172 going into its isolated flyback mode (see LT1172 data sheet), not breakdown limits. If the LT1172 V_{IN} pin is driven from a low voltage source (e.g., 5V) the 20V limit may be extended by using Figure G1's network. If the LT1172 is driven from the same supply as L1's center tap, the network is unnecessary, although efficiency will suffer.

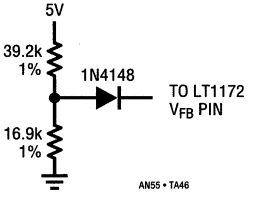


Figure G1. Network allows CCFL Operation beyond 20V Inputs

APPENDIX H

RELATED CIRCUITS

Higher Power Operation

There is no inherent limit on CCFL circuit output power. Figure H1's arrangement is a scaled up version of the text's CCFL circuits. This design, similar to ones employed for automotive use, drives a 25W CCFL. There are virtually no configuration changes, although most component power ratings have increased. The transistors can handle the higher currents, but all other power components are higher capacity. Efficiency is about 80%.

HeNe Laser Power Supply

Helium-neon lasers, used for a variety of tasks, are difficult loads for a power supply. They typically need almost 10kV to start conduction, although they require only about 1500V to maintain conduction at their specified operating currents. Powering a laser usually involves some form of start-up circuitry to generate the initial breakdown voltage and a separate supply for sustaining conduction. Figure H2's circuit considerably simplifies driving the laser. The start-up and sustaining functions have been combined into a single, closed-loop current source with over 10kV of compliance. The circuit is recognizable as a reworked CCFL power supply with a voltage tripled DC output.

When power is applied, the laser does not conduct and the voltage across the 190Ω resistor is zero. The LT1170 switching regulator FB pin sees no feedback voltage, and its switch pin (V_{SW}) provides full duty cycle pulse width modulation to L2. Current flows from L1's center tap through Q1 and Q2 into L2 and the LT1170. This current flow causes Q1 and Q2 to switch, alternately driving L1. The 0.47µF capacitor resonates with L1, providing boosted sine wave drive. L1 provides substantial step-up, causing about 3500V to appear at its secondary. The capacitors and diodes associated with L1's secondary form a voltage tripler, producing over 10kV across the laser. The laser breaks down and current begins to flow through it. The 47kΩ resistor limits current and isolates the laser's load characteristic. The current flow causes a voltage to appear across the 190Ω resistor. A filtered version of this voltage appears at the LT1170 FB pin, closing a control loop. The LT1170 adjusts pulse width drive to L2 to maintain the

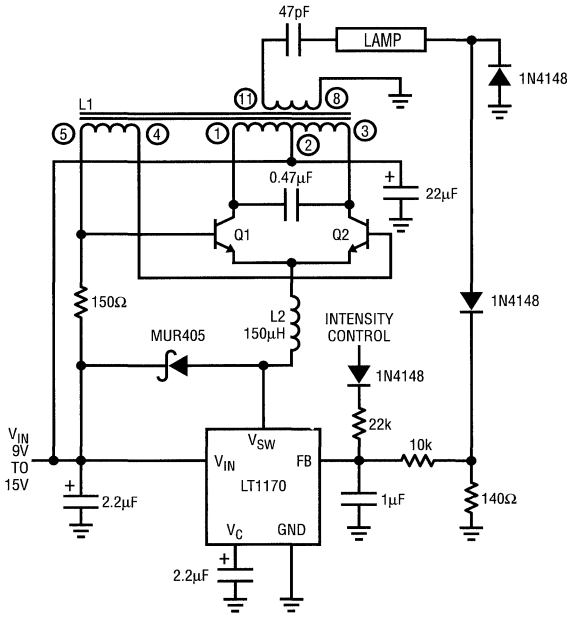


Figure H1. A 20W CCFL Supply

FB pin at 1.23V, regardless of changes in operating conditions. In this fashion, the laser sees constant current drive, in this case 6.5mA. Other currents are obtainable by varying the 190Ω value. The 1N4002 diode string clamps excessive voltages when laser conduction first begins, protecting the LT1170. The 10µF capacitor at the V_C pin frequency compensates the loop and the MUR405 maintains L1's current flow when the LT1170 V_{SW} pin is not conducting. The circuit will start and run the laser over a 9V-35V input range with an electrical efficiency of about 80%.

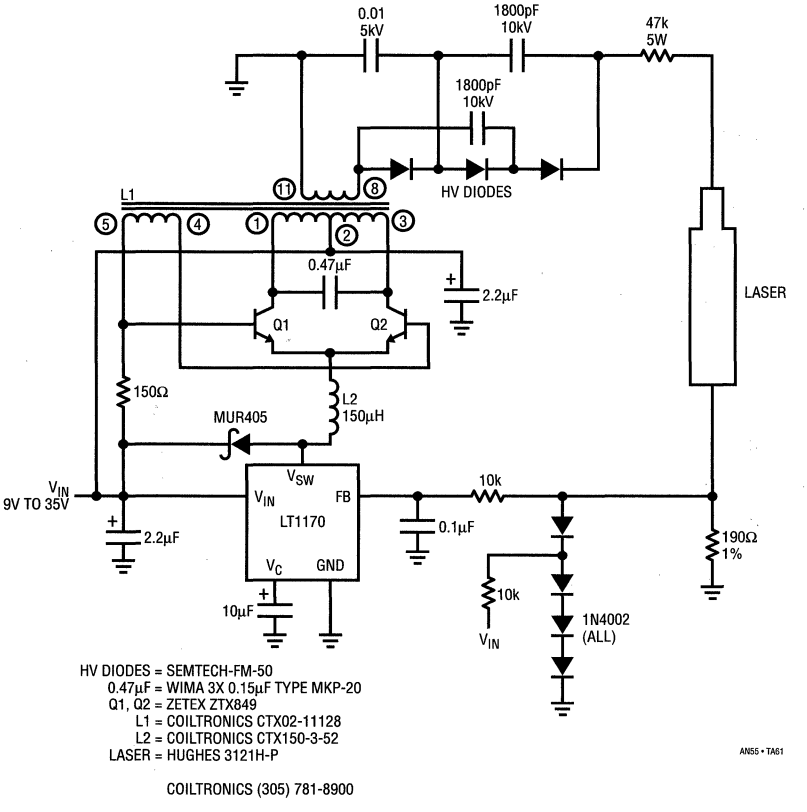


Figure H2. Laser Power Supply, Based on the CCFL Circuit, is Essentially a 10,000V Compliance Current Source

APPENDIX I

WHO WAS ROYER, AND WHAT DID HE DESIGN?

In December 1954 the paper "Transistors as On-Off Switches in Saturable-Core Circuits" appeared in *Electrical Manufacturing*. George H. Royer, one of the authors, described a "d-c to a-c converter" as part of this paper. Using Westinghouse 2N74 transistors, Royer reported 90% efficiency for his circuit. The operation of Royer's circuit is well described in this paper. The Royer converter was widely adopted, and used in designs from watts to kilowatts. It is still the basis for a wide variety of power conversion.

Royer's circuit is not an LC resonant type. The transformer is the sole energy storage element and the output is a square wave. Figure I1 is a conceptual schematic of a typical converter. The input is applied to a self-oscillating configuration composed of transistors, a transformer and a biasing network. The transistors conduct out of phase, switching (Figure I2, Traces A and C are Q1's collector and base, while Traces B and D are Q2's collector and base) each time the transformer saturates. Transformer saturation causes a quickly rising, high current to flow (Trace E).

This current spike, picked up by the base drive winding, switches the transistors. This phase opposed switching causes the transistors to exchange states. Current abruptly drops in the formerly conducting transistor and then slowly rises in the newly conducting transistor until saturation again forces switching. This alternating operation sets transistor duty cycle at 50%.

Photograph I3 is a time and amplitude expansion of I2's Traces B and E. It clearly shows the relationship between transformer current (Trace B, Figure I3) and transistor collector voltage (Trace A, Figure I3).[1]

Note 1: The bottom traces in both photographs are not germane and are not referenced in the discussion.

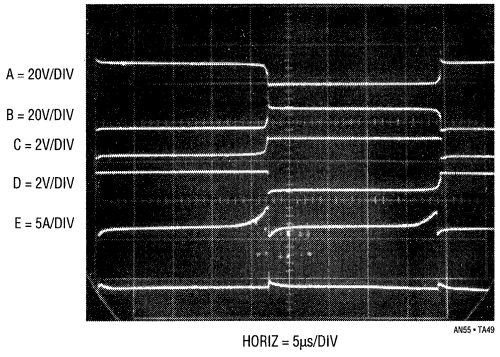


Figure I2. Waveforms for the Classic Royer Circuit

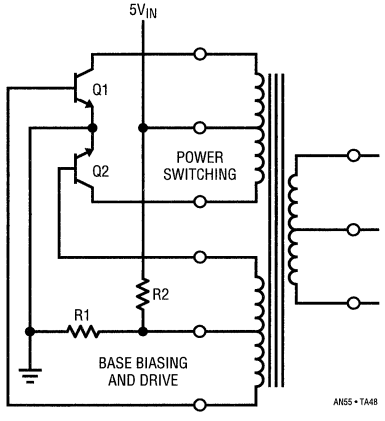


Figure I1. Conceptual Classic Royer Converter. Transformer Approaching Saturation Causes Switching

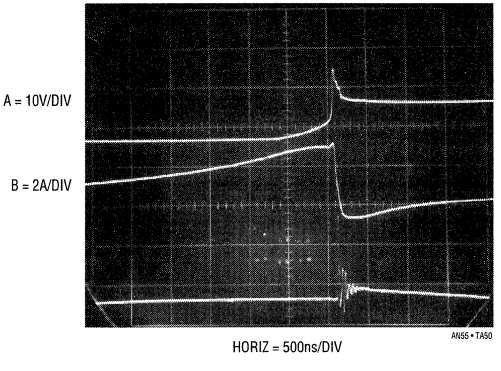


Figure I3. Detail of Transistor Switching. Turn-Off (Trace A) Occurs Just as Transformer Heads into Saturation (Trace B)

APPENDIX J

A LOT OF CUT-OFF EARS AND NO VAN GOGHS

Some Not-So-Great Ideas

The hunt for a practical CCFL power supply covered (and is still covering) a lot of territory. The wide range of conflicting requirements combined with ill-defined lamp characteristics produces plenty of unpleasant surprises. This section presents a selection of ideas that turned into disappointing breadboards. Backlight circuits are one of the deadliest places for theoretically interesting circuits the author has ever encountered.

Not-So-Great Backlight Circuits

Figure J1 seeks to boost efficiency by eliminating the LT1172's saturation loss. Comparator C1 controls a free running loop around the Royer by on-off modulation of transistor base drive. The circuit delivers bursts of high voltage sine drive to the lamp to maintain the feedback node. The scheme worked, but had poor line rejection due to the varying waveform vs supply seen by the RC averaging pair. Also, the "burst" modulation forces the loop to

constantly restart the lamp at the burst rate, wasting energy. Finally, lamp power is delivered by a high crest factor waveform, causing inefficient current-to-light conversion in the lamp.

Figure J2 attempts to deal with some of these issues. It converts the previous circuit to an amplifier controlled current mode regulator. Also, the Royer base drive is controlled by a clocked, high frequency pulse width modulator. This arrangement provides a more regular waveform to the averaging RC, improving line rejection. Unfortunately, the improvement was not adequate. 1% line rejection is required to avoid annoying flicker when the line moves abruptly, such as when a charger is activated. Another difficulty is that, although reduced by the higher frequency PWM, crest factor is still non-optimal. Finally, the lamp is still forced to restart at each PWM cycle, wasting power.

Figure J3 adds a "keep alive" function to prevent the Royer from turning off. This aspect worked well. When the PWM goes low the Royer is kept running, maintaining low level lamp conduction. This eliminates the continuous lamp restarting, saving power. The "supply correction" block feeds a portion of the supply into the RC averager, improving line rejection to acceptable levels.

This circuit, after considerable fiddling, achieved almost 94% efficiency but produced less output light than a "less efficient" version of text Figure 6! The villain is lamp waveform crest factor. The keep alive circuit helps, but the lamp still cannot handle even moderate crest factors.

Figure J4 is a very different approach. This circuit is a driven square wave converter. The resonating capacitor is eliminated. The base drive generator shapes the edges, minimizing harmonics for low noise operation. This circuit works well, but relatively low operating frequencies are required to get good efficiency. This is so because the sloped drive must be a small percentage of the fundamental to maintain low losses. This mandates relatively large magnetics—a crucial disadvantage. Also, square waves

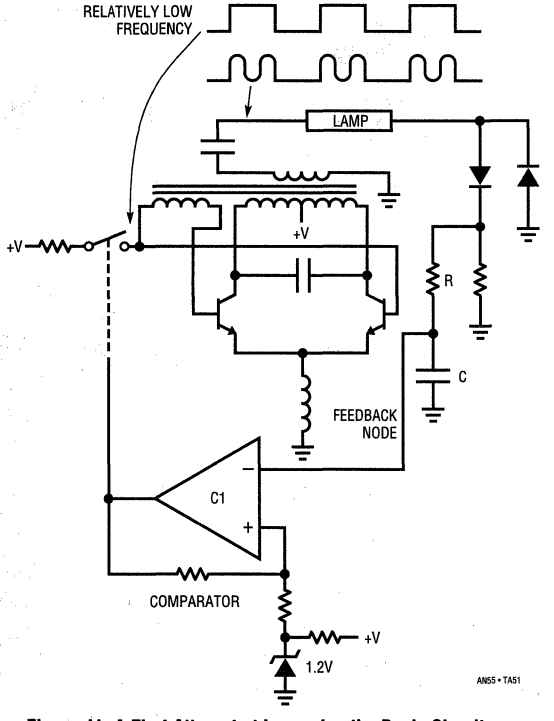


Figure J1. A First Attempt at Improving the Basic Circuit. Irregular Royer Drive Promotes Losses and Poor Regulation

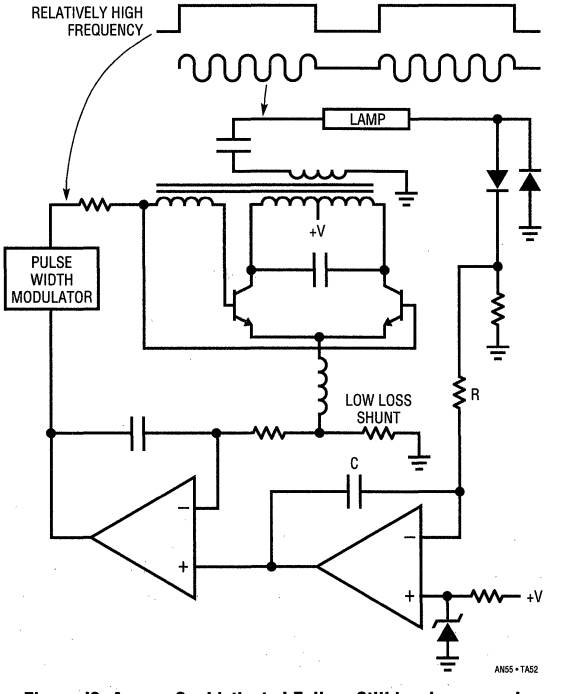


Figure J2. A more Sophisticated Failure Still has Losses and Poor Line Regulation

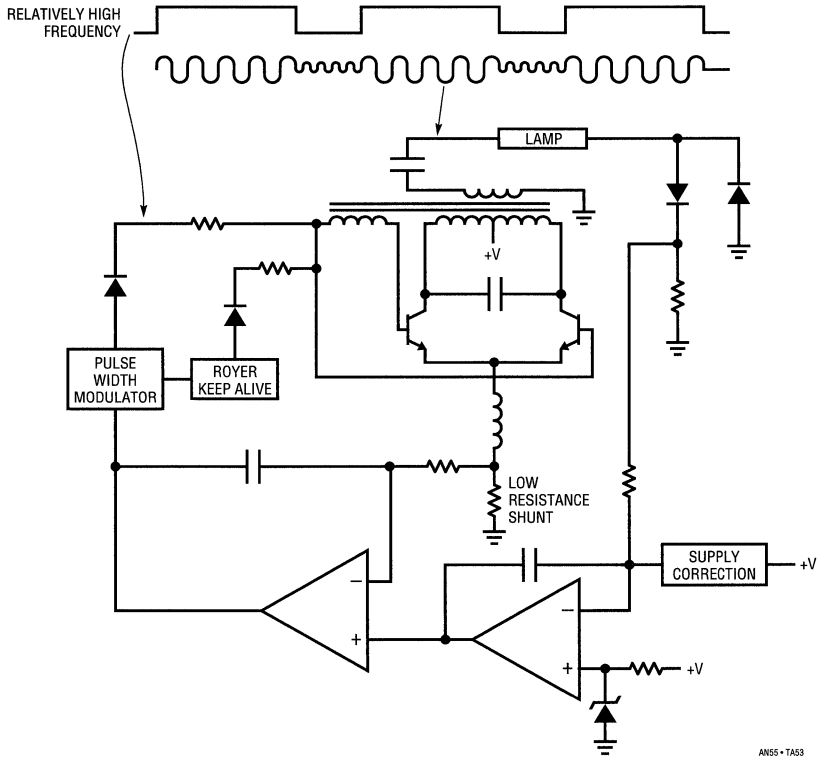


Figure J3. "Keep Alive" Circuit Eliminates Turn-On Losses and has 94% Efficiency. Light Emission is Lower than "Less Efficient" Circuits

have different crest factor and rise time than sines, forcing inefficient lamp transduction.

Not-So-Great Primary Side Sensing Ideas

Text Figures 28 and 29 use primary side current sensing to control lamp intensity. This permits the lamp to fully float, extending its dynamic operating range. A number of primary side sensing approaches were tried before the "top side sense" won the contest.

J5's ground referred current sensing is the most obvious way to detect Royer current. It offers the advantage of simple signal conditioning—there is no common mode voltage. The assumption that essentially all Royer current derives from the LT1172 emitter pin path is true. Also true, however, is that the waveshape of this path's current varies widely with input voltage and lamp operating current. The RMS voltage across the shunt (e.g., the Royer

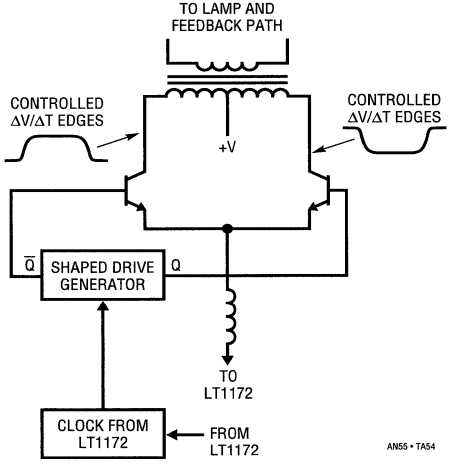


Figure J4. A Non-Resonant Approach. Slew Retarded Edges Minimize Harmonics, but Transformer Size Goes Up. Output Waveform is also Non-Optimal, Causing Lamp Losses

current) is unaffected by this, but the simple RC averager produces different outputs for the various waveforms. This causes this approach to have very poor line rejection, rendering it impractical. J6 senses inductor flux, which should correlate with Royer current. This approach promises attractive simplicity. It gives better line regulation but still has some trouble giving reliable feedback as waveshape changes. Also, in keeping with most flux sampling schemes, it regulates poorly under low current conditions.

Figure J7 senses flux in the transformer. This takes advantage of the transformer's more regular waveform. Line regulation is reasonably good because of this, but low current regulation is still poor. J8 samples Royer collector voltage capacitively, but the feedback signal does not accurately represent start-up, transient and low current conditions.

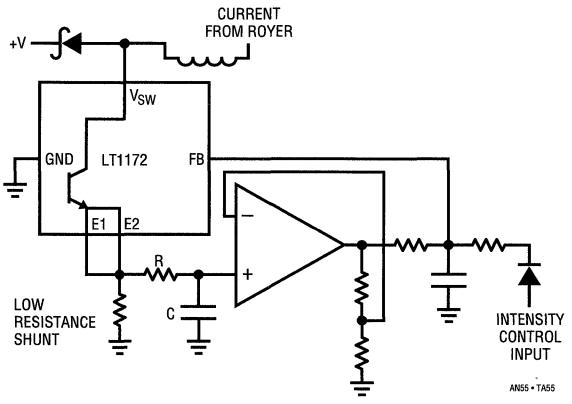


Figure J5. "Bottom Side" Current Sensing has Poor Line Regulation due to RC Averaging Characteristics

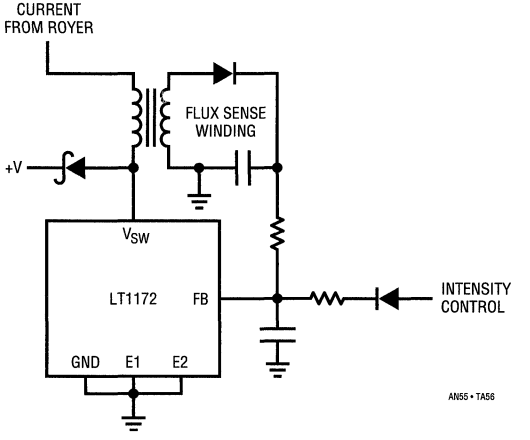


Figure J6. Flux Sensing has Irregular Outputs, Particularly at Low Currents

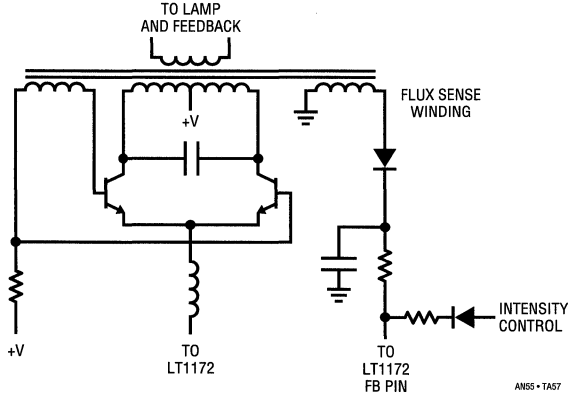


Figure J7. Transformer Flux Sensing Gives More Regular Feedback, but Not at Low Currents

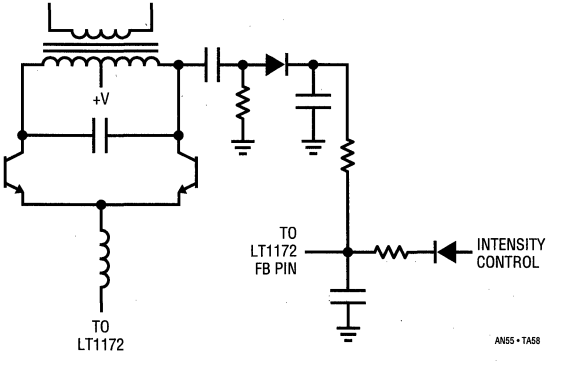


Figure J8. AC Coupled Drive Waveform Feedback is Not Reliable at Low Currents

APPENDIX K

PERSPECTIVES ON EFFICIENCY

The LCD displays currently available require two power sources, a backlight supply and a contrast supply. The display backlight is the single largest power consumer in a typical portable apparatus, accounting for almost 50% of battery drain with the display at maximum intensity. As such, every effort must be expended to maximize backlight efficiency.

The backlight presents a cascaded energy attenuator to the battery (Figure K1). Battery energy is lost in the electrical-to-electrical conversion to high voltage AC to drive the cold cathode fluorescent lamp (CCFL). This section of the energy attenuator is the most efficient; conversion efficiencies exceeding 90% are possible. The CCFL, although the most efficient electrical-to-light converter available today, has losses exceeding 80%. Additionally, the optical transmission efficiency of present displays is under 10% for monochrome, with color types much lower. Clearly, overall backlight efficiency improvements must come from lamp and display improvements.

Higher CCFL circuit efficiency does, however, directly translate into increased operating time. For comparison purposes text Figure 8's circuit was installed in a Toshiba Model 2200 running 5mA lamp current. The result was a 19 minute increase in operating time.

Relatively small reductions in backlight intensity can greatly extend battery life. A 20% reduction in screen intensity results in nearly 30 minutes additional running time. This assumes that efficiency remains reasonably flat as power is reduced. Figure K2 shows that the circuits presented do reasonably well in this regard, as opposed to other approaches.

The contrast supply, operating at greatly reduced power, is not a major source of loss.

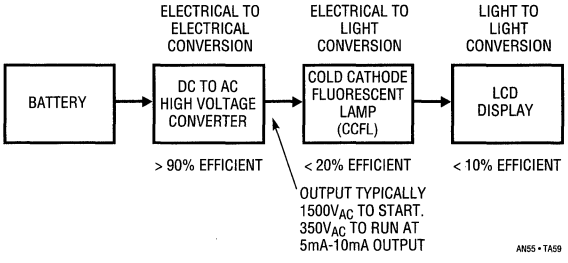


Figure K1. The Backlit LCD Display Presents a Cascaded Energy Attenuator to the Battery. DC to AC Conversion is Significantly more Efficient than Energy Conversions in Lamp and Display

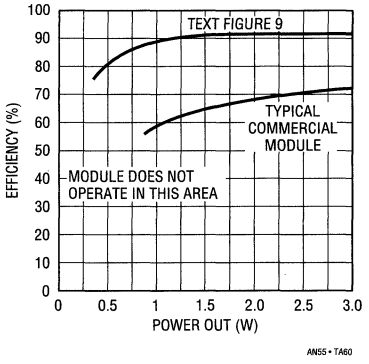


Figure K2. Efficiency Comparison Between Text Figure 9 and a Typical Modular Converter

HELP SUPPORT MY EDUCATION.
CALL MY DAD ABOUT
YOUR BACKLIGHT APPLICATION.

'93

"Better than Bessel" Linear Phase Filters for Data Communications

Richard Markell

INTRODUCTION

The pace of the world of digital communications is increasing at a tremendous rate. Daily, the engineer is requested to compact more data in the same channel bandwidth with closer channel spacing. As an example, multilevel Pulse Amplitude Modulation (PAM) systems can be used to compress data into a bandwidth limited channel. The most typical PAM system is simply ones and zeros, the binary system. By shifting from a two-level system to a four-level system, we double the data bandwidth in a bandwidth limited channel at the expense of requiring a 8dB higher signal-to-noise ratio at the receiver.[1] This signal-to-noise trade-off to cram more bits into the same bandwidth is why filtering is becoming more and more critical in data transmission. This is precisely why the LTC data communications filters were born.

Filters such as the Bessel switched capacitor filter (LTC1064-3), although having excellent transient response, have very poor noise or adjacent channel rejection. DSP is a help if the designer is trying to use telephone bandwidth, but is not fast enough for efficient uses of 100kHz of bandwidth, let alone 200kHz, where data rates approach 400 to 800kbps.

[1] Kamilo Feher, "Digital Communications: Microwave Applications," Prentice-Hall Inc., Englewood Cliffs, NJ, 1981.

[2] Hoopla is an utterance designed to bewilder.

Enter the LTC1264-7 Linear Phase Filter

The LTC1264-7 has group delay which is equal to the Bessel in the passband while it has rejection at the second harmonic of the cutoff frequency of –30dB versus the Bessel's –12dB. Thus, Bessel is banished, replaced by a better linear phase solution for the data transmission problem. Even the most conservative data compaction engineer will agree that the LTC1264-7 is "Better than Bessel." Enough hoopla[2], let's get into the details.

Linear Technology's LTC1X64-7 family of filters incorporates 2 poles of phase compensation (allpass filtering) and 6 poles of lowpass elliptic filtering in a single 14-pin package. No external resistors are required. The LTC1264-7 is the first member of the Dash 7 linear phase filter family. The group includes the LTC1264-7, the LTC1164-7, the low power (4mA) member of the family with cutoff frequency to 20kHz and the LTC1064-7, the originator of the family, which provides cutoff frequencies to 100kHz.

This application note discusses some of the requirements and techniques for using filters in digital communications. The terms "channel bandwidth," "eye diagrams" and "linear phase" filtering are discussed without the need for the "engineering speak" which permeates many textbook explanations of the same subjects.

The eye diagram measures the "quality" of the transmission channel. The eye opening provides subjective indication of bit error rate or the "goodness of the channel." This will be discussed in more detail later in this text.

The eye diagram shown in Figure 1 is illustrative of 100kHz phase performance. Notice the lack of over or undershoot at the transitions. The well-behaved nature of the transitions allows data coding to multiple levels while retaining the required signal-to-noise ratio (SNR). However, the real advantage of the LTC1264-7 is in the stopband rejection. Figure 2 shows an amplitude comparison of the responses of the LTC1264-7, the 8-pole Butterworth, the LTC1064-2, and the 8-pole Bessel filter, the LTC1064-3. The difference is dramatic! The LTC1264-7 attains 28dB attenuation at 2 times cutoff, while the LTC1064-3 attains only 12dB. The phase response of both filters remains linear through their passbands, although the LTC1064-3 extends this response to almost 2 times cutoff. Figures 3a, 3b and 3c, and Figures 4a, 4b, 4c and 4d detail the burst response and the transient response of the LTC1064-1, the LTC1064-2 and the LTC1064-7 as an additional comparison criterion. We shall explore the effect all this has on digital transmission later in this article, but to effect this comparison a short explanation of some principles of digital transmission is first needed.

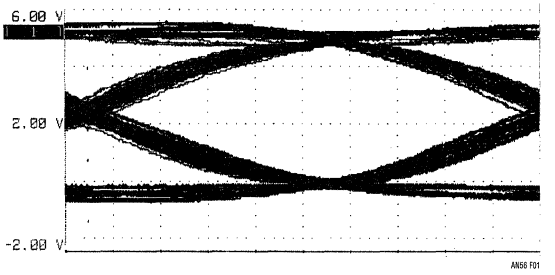


Figure 1. Eye Diagram LTC1264-7, f_{CUTOFF} = 100kHz, Data Rate = 200kbps

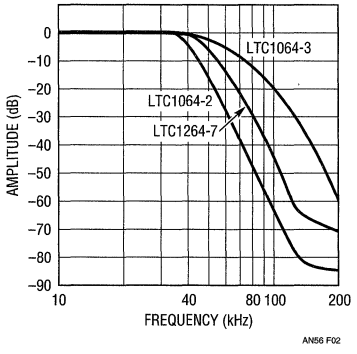


Figure 2. Filter Roll-Off Comparison, f_{CUTOFF} = 40kHz, for Butterworth 8th Order LPF, LTC1064-2, Bessel 8th Order LPF, LTC1064-3 and LTC1264-7 Linear Phase Filter

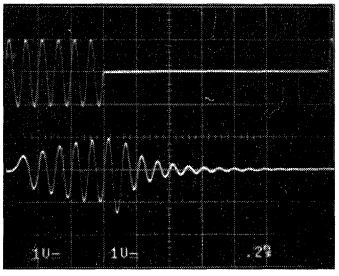


Figure 3a. Burst Reponse LTC1064-1, f_{CLK} = 1MHz, f_C = 10kHz, Burst: 10kHz Sine Wave

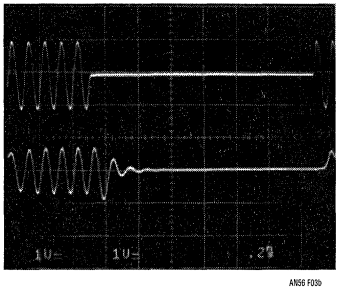


Figure 3b. Burst Response LTC1064-2, f_{CLK} = 1MHz, f_C = 10kHz, Burst: 10kHz Sine Wave

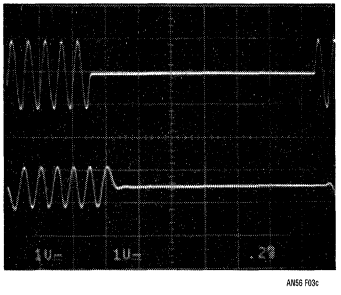


Figure 3c. Burst Response LTC1064-7, f_{CLK} = 750kHz, f_C = 10kHz, Burst: 10kHz Sine Wave

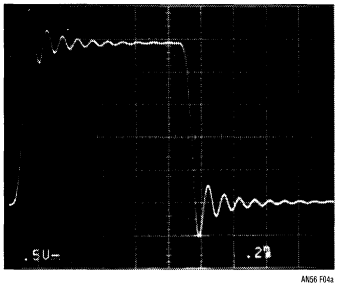


Figure 4a. Transient Response LTC1064-1, f_{CLK} = 1MHz, f_C = 10kHz, f_{IN} = 480Hz

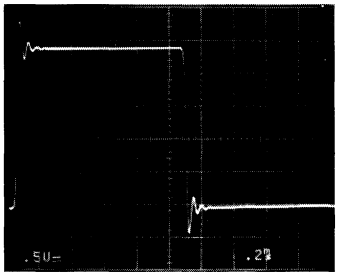


Figure 4b. Transient Response LTC1064-2, f_{CLK} = 1MHz, f_C = 10kHz, f_{IN} = 480Hz

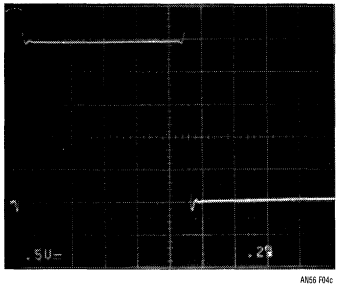


Figure 4c. Transient Response LTC1064-7, f_{CLK} = 1MHz, f_C = 10kHz, f_{IN} = 480Hz

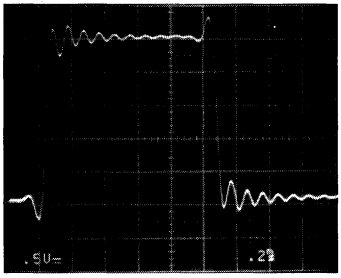


Figure 4d. Transient Response Equalized LTC1064-1, (See Appendix B), f_{CLK} = 1MHz, f_C = 10kHz, f_{IN} = 480Hz

SOME PRINCIPLES OF DATA TRANSMISSION

Transmission of data in a given bandwidth channel is more efficient when as many bits/second can be transmitted through this channel as possible. Shannon theorems show that the theoretical data rate limit is transmission of f_S symbols in a bandwidth (BW = B) of only f_S/2Hz. So, for a binary transmission where one symbol contains one bit, f_B, the number of bits per second is equal to the symbol rate, f_S. Figure 5 shows this situation schematically. For "M ary"[3] systems, such as 4-level Pulse Amplitude Modulation (PAM), each transmitted symbol contains n information bits, where $n = \log_2 M$. In this case the symbol rate is $f_S = f_B/n$.

Consider the example where it is required to transmit a 100kbps source (= f_B). Theoretically this could be accomplished with a channel bandwidth, $B = f_S/2 = f_B/2 = 50kHz$. With the aforementioned 4-level PAM scheme, the channel bandwidth reduces to $25kHz = f_S/2 = f_B/4$. This type of encoding is used by many types of digital communications systems. The trade-offs involve bandwidth versus encoding complexity. If the above mentioned 100kbps source **must** be passed in a bandwidth of $6.25kHz = f_S/2 = f_B/16$, it follows that 256-level PAM or an equivalently dense packing scheme must be used. Multilevel and multiphase signals require the filter be linear phase (to preserve pulse integrity in the time domain) while providing as much roll-off in the stopband as possible. More discussion of these topics is included in the discussion of "eye diagrams."[4]

[3] An M ary system contains M voltage levels. A binary system has 2 levels, whereas an M = 8 system has 8 levels and so on. A 2-level system can detect only 1 and 0, but higher level systems of PAM threshold in more than one place so as to transmit more information in a given bandwidth.

[4] Also see the much more detailed discussions in: Feher, Dr. Kamilo, "Digital Communications--Satellite/Earth Station Engineering," Prentice-Hall Inc., Englewood Cliffs, NJ, 1983.

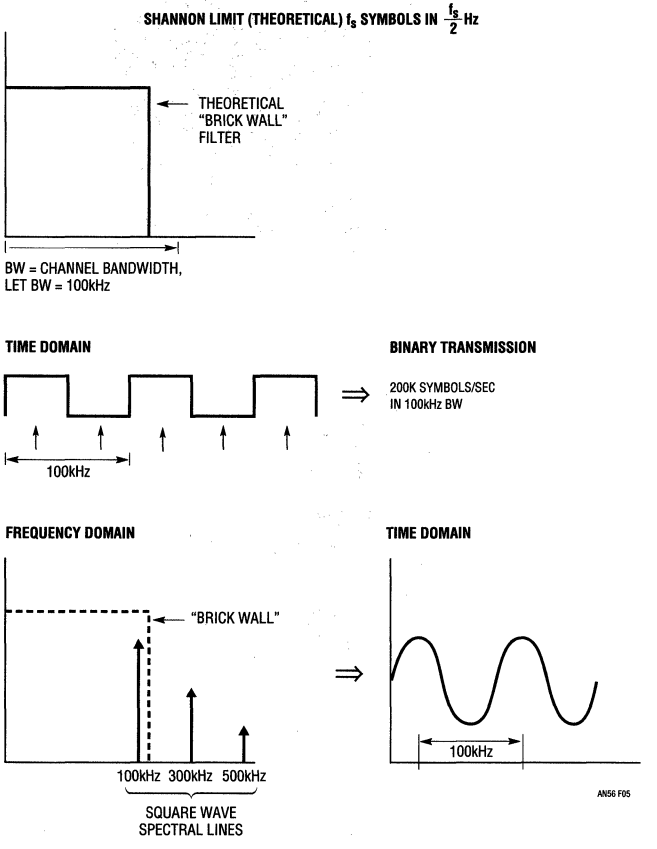


Figure 5. Shannon Data Transmission Shown Schematically

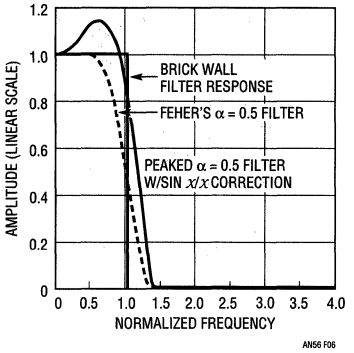


Figure 6. Brick Wall Theoretical Filter and Two Filters Realizable with 8th Order SCF Technology
Note: Linear Amplitude Scale

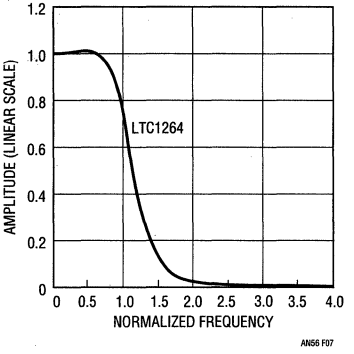


Figure 7. Amplitude Response LTC1264-7
Note: Linear Amplitude Scale

The channel with bandwidth $f_S/2Hz$ is the famous "brick wall"[5] filter. This is the channel all filter designers strive for but no one can build. So we all strive to come as close as possible. If the ideal brick wall filter could be achieved, it would be as shown in Figure 6. Also shown in Figure 6 are two filters which are possible to realize with 8th order switched capacitor filter technology and external resistors. Both filters have theoretically infinite attenuation at 1.5 times the cutoff frequency. The filter with the peaked response can be corrected by a multiplication factor ($\chi/\sin\chi$) so that when the signal is digitally sampled (a procedure common to digital transmission of signals), the result is optimally flat in transmission bandwidth.

Figure 7 shows the amplitude response, normalized, for the LTC Dash 7 series of filters. A comparison with Feher's[6] alpha = 0.5 filter (where alpha is the roll-off factor: alpha = 0 is the brick wall filter, alpha = 1 implies twice the theoretical bandwidth requirement) shows few differences in the amplitude response. The LTC1264-7 will operate to 250kHz, while the LTC1164-7 will operate (using only 4mA of supply current) to 20kHz. The LTC1064-7 will operate to 100kHz. **Best of all, the eye patterns for these filters are superior!! To understand why, read on!**

[5] A brick wall filter has a frequency response which is flat (or 0dB) with no ripple in the passband to the cutoff frequency, f_C, then rolls off to infinite attenuation at the beginning of the stopband, f_S. The brick wall filter is only theoretical, thus $f_C = f_S$.

[6] Feher, ibid.

Why Linear Phase?

An additional criterion that the "close to ideal" data transmission filter must strive to achieve (and they didn't tell you in college) is a linear phase response.

Linear phase means that each frequency which passes through the filtered channel will be delayed in time linearly according to its frequency. Higher frequencies have smaller (in magnitude) delays. The specification of group delay plots this phenomenon, "the delay of the group (of frequencies)," versus frequency. The objective of a group delay plot is to have a flat line representing the situation where all frequencies are delayed the same amount. This is the best case linear phase filter. All other compromises are based on this ideal situation.

Group delay is a most important characteristic in digital data transmission applications because a filter with flat group delay passes a square wave with little distortion. The LTC "Better than Bessel" filters compromise phase linearity outside the passband to achieve more amplitude attenuation in the stopband. Feher, a recognized authority in the field of digital communications, notes that for data transmission, filters should be linear in phase to their –10dB amplitude points in the filter's transition region. The LTC "-7" filters meet this criterion (Figure 8).

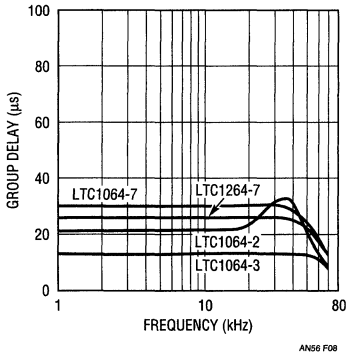


Figure 8. Group Delay vs Frequency for Four Filters: LTC1064-2/LTC1064-3/LTC1064-7/LTC1264-7, f_C(All Filters) = 40kHz, V_S = ±7.5V

FILTERS FOR DATA COMMUNICATIONS: HOW AND WHY TO SELECT THEM

The perfect filter for data communications, if it could be implemented, would be Feher's "brick wall," linear phase, flat group delay, alpha = 0 filter as shown in Figure 9. But, we cannot build this type of filter.

In this section, we describe the LTC1064/LTC1164/LTC1264-7 "Better than Bessel" filter family. These are 6th order lowpass filters with a 2nd order allpass (phase equalizing) section designed for data communications. These filters are contained in a single 14-pin DIP or 16-pin SOL package. They are a complete integrated solution with the resistors required to program the response of the switched capacitor filter sections integrated onto the die of the filter.

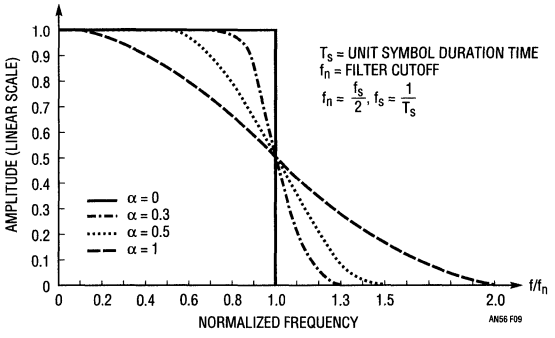


Figure 9. Amplitude Characteristics of the Nyquist Channel for Impulse

LTC1064/LTC1164/LTC1264-7 Filters

The Dash 7 filters were designed by making them "Better than Bessel." That is, the low Q Bessel response was modified to incorporate a notch or zero in the stopband to "pull down" the amplitude response just outside the passband of the filter. This increases the attenuation from the Bessel's –12dB at 2× cutoff to –28dB for the LTC1264-7 (also at 2× cutoff). This is shown in Figure 10. The LTC1064-7 and LTC1164-7 have even better stopband performance at –34dB at 2× cutoff. While this increased

attenuation has little effect on the eye diagram, it increases the attenuation of the carrier signal while not degrading the data that is superimposed on this carrier. This means better (that is lower) bit error rates for the same bandwidth channel.

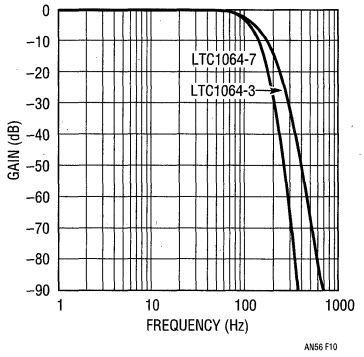


Figure 10. Amplitude Response: LTC1064-3 vs LTC1064-7 (Bessel vs "Better than Bessel"), f_C = 100Hz

MEASUREMENT: THE EYE DIAGRAM, AMPLITUDE AND GROUP DELAY

Since the perfect lowpassed transmission channel does not exist, a means must be found to evaluate channel quality. This means is the so-called "eye" diagram. The eye diagram is generated by the setup shown in Figure 11. Figure 12 shows the pseudorandom code generator circuitry used as the random data source.

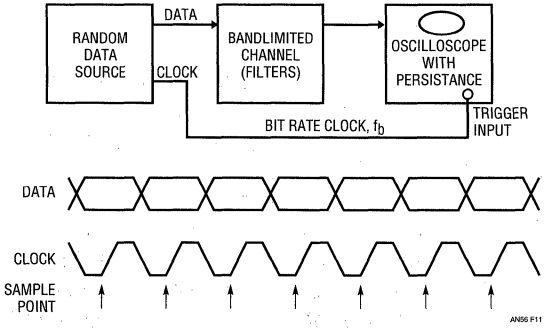


Figure 11. Eye Diagram Generation Circuitry and Data Timing

Symbols transmitted through a theoretical Nyquist channel should have no degradation in amplitude response, and as such, the measured eye diagram opening (of a real channel) shows graphically the "quality" of the transmission channel (which includes the lowpass filter inserted in the transmission path). It can be shown that the degradation in the eye opening is directly related to intersymbol interference (the interference in the detection of one symbol in the presence of another) and therefore is a measure of the systems bit error rate (see Feher)[1].

With this background, some eye opening diagrams exemplify how the LTC1264-7 filter is optimized for applications in data communications. Figures 13 and 14 show the eye diagrams of the LTC1064-2 (8th order Butterworth LPF) and the new LTC1264-7 linear phase filter (6th order elliptic LPF + 2nd order phase correction network). It can be seen that if a digital system thresholds at the midpoint in the eye diagrams, the Bit Error Rate (BER) will be higher for the eye diagram with the smaller "eye opening." The calculation of Intersymbol Interference (ISI) degradation due to "channel" or filter imperfections is a measure of degradation in BER and is calculated:

ISI degradation =
20 log (actual eye opening/100% eye opening)

Thus, it can be seen that the LTC1264-7 is a far superior filter when used to maximize channel efficiency in digital systems. However, we must look at the LTC1064-3 (8th order Bessel LPF) for comparison.

The LTC1064-3 is shown in the eye diagram illustrated as Figure 15. This eye diagram shows ISI degradation similar to the LTC1264-7 with better jitter specifications. Although the Bessel filter appears to be superior from the viewpoint of the eye diagram, the reader should remember that the LTC1264-7 has far superior stopband attenuation, meaning better attenuation of the "carrier" at 27.5kHz in this example. This translates to better bit error rates. The system user must trade off ISI degradation, jitter and the filter attenuation to ensure best "channel performance." In addition, remember that the eye diagrams shown here are for 2-level systems (0V and 5V). For M-level systems, the increased spectrum efficiency means greater signal-to-noise ratios are required necessitating the roll-off characteristics of filters like the LTC1264-7.

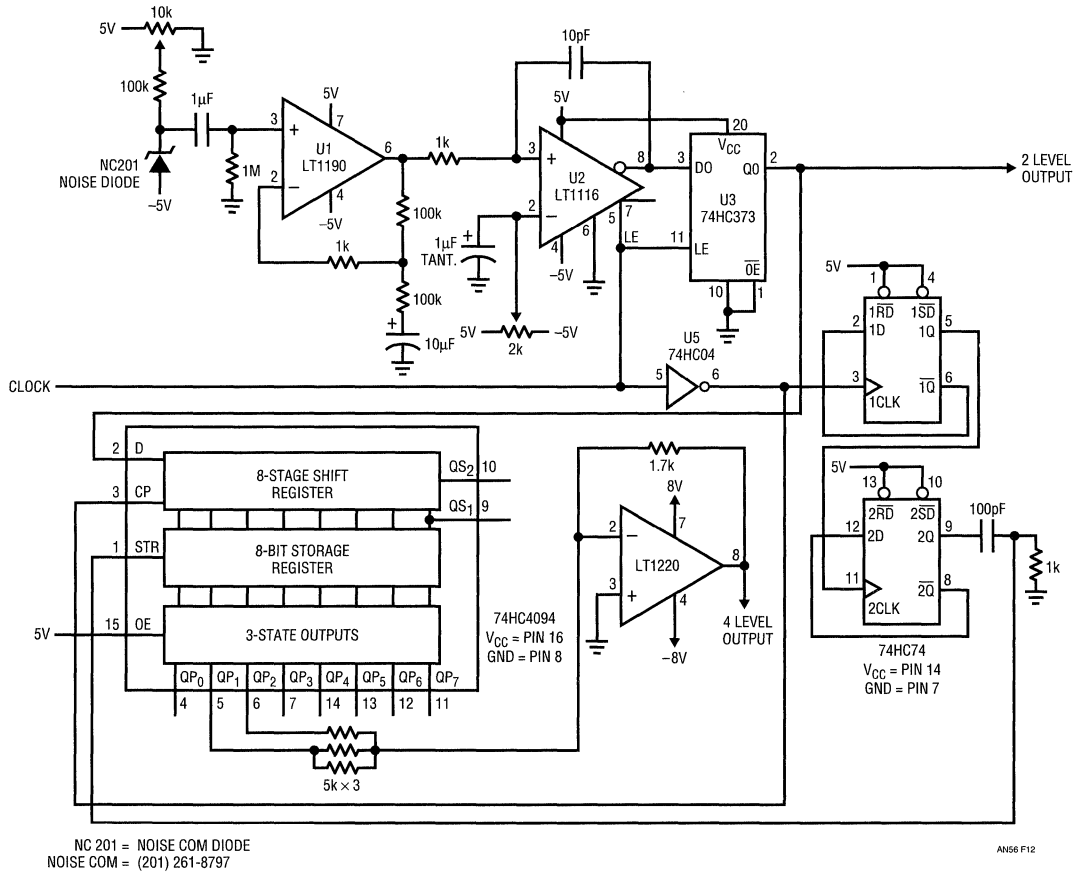


Figure 12. Pseudorandom Code Generator Schematic Diagram

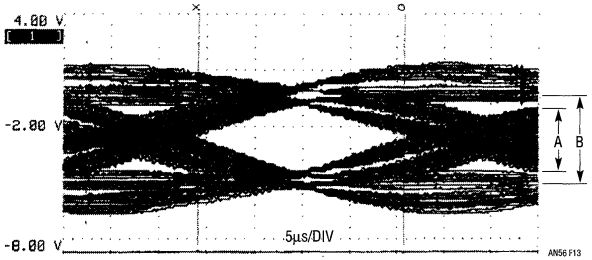


Figure 13. LTC1064-2: f_{CUTOFF} = 13.7kHz, f_S = 27.5kbps, ISI Degradation = 20 Log (0.75) = –2.5dB. A = 75% Opening, B = 100% Opening

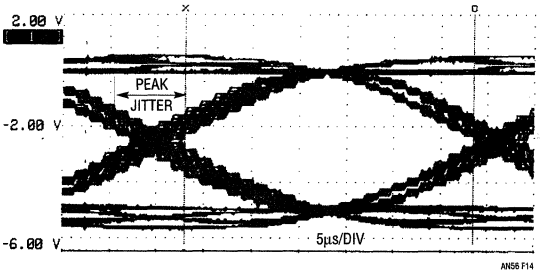


Figure 14. LTC1264-7: f_{CUTOFF} = 13.7kHz, f_S = 27.5kbps, ISI Degradation = −0.46dB, Peak Jitter 5.6µs

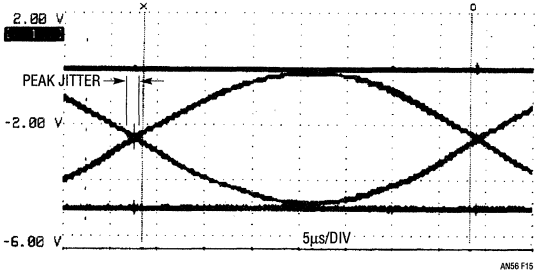


Figure 15. LTC1064-3: f_{CUTOFF} = 13.7kHz, f_S = 27.5kbps, ISI Degradation = −0.94dB, Peak Jitter 1.2µs

To conclude, the LTC1264-7 is a linear phase, better than Bessel, switched capacitor filter optimized for the data communications world. The filter will operate to a cutoff frequency of 200kHz while providing linear phase through its passband. The filter can be used in satellite communications, cellular phones, microwave links, ISDN networks and many other types of digital systems.

References:

1. Kamilo Feher, "Digital Communications: Microwave Applications," Prentice-Hall, Inc., Englewood Cliffs, NJ, 1981

2. Dr. Kamilo Feher and Engineers of Hewlett-Packard Ltd., "Telecommunications, Measurements, Analysis and Instrumentation," Prentice-Hall, Inc., Englewood Cliffs, NJ, 1987

3. Dr. Kamilo Feher, "Digital Communications: Satellite/Earth Station Engineering," Prentice-Hall, Inc., Englewood Cliffs, NJ, 1981

APPENDIX A

Seven Months and No Cigar: The LTC1264-7 Germination Saga

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11902 Parkland Ct., Fairfax, Virginia 22033

The transmission quality of any phase modulated signal depends on the group delay in the passband and the attenuation in the stopband of the (filtered) transmission channel. In synchronous detection the receiver IF center frequency is zero and the IF amplifier becomes a lowpass filter. Since the RF filter operates at a much higher frequency than the IF, it needs all the group delay margin that the total receiver design can give it. The lowpass IF amplifier wants to have a Bessel response characteristic since the Bessel response has the best group delay of any of the classical filters. Unfortunately the Bessel filter has very poor rejection characteristics in the stopband. In a very noisy environment one would prefer to have Butterworth or elliptical roll-off characteristics and Bessel group delay.

About three years ago I set out to design such a filter. It was to have Butterworth roll-off and Bessel group delay. I knew that although I really wanted elliptical characteristics the Butterworth characteristics would be easier to phase equalize (compensate). After returning a number of computer programs which were supposed to optimize group delay characteristics (and didn't), I found one that did. The computer generated filter design looked great on paper

although it contained 29 operational amplifiers. A simple Monte Carlo analysis showed that part tolerances would be a problem. I first built the most complex section and put it on the analyzer. Unfortunately the operational amplifier could not read and thus it did what it knew to do which was to have characteristics which were unlike the simulation. After some looking I found an operational amplifier which would track the simulation very closely if I adjusted the resistors somewhat. Now I not only had 29 operational amplifiers but 30 adjustments. The adjustment was very difficult. Each section of the filter had to be adjusted individually; after that they all had to work together. I wrote some special software which ran on the IEEE bus to compare the actual filter data from the analyzer with the simulation data. The computer would then display the difference between the two in gain and group delay. Adjustment took two days and I got to about twice the differential in group delay that I set as my goal. The circuit had about two times the ambient differential specification I desired when I spray canned the card. This process took about seven months and resulted in a prototype Vector card. I was devastated; seven months and not even close.

One day some time later, I was reading EDN and came across an article about switched capacitor filters by Rich Markell. I had talked to a number of such vendors asking if they knew what group delay was and were they interested in optimizing for group delay. Most said what is group delay? The few who knew said all their filters would have the classical group delay of a nonswitched capacitor filter. Rich said he knew and asked why it was important to me. I poured out my "seven months and no cigar" story. He seemed really interested. A few days later he asked if I would be interested in looking at a switched capacitor filter breadboard which LTC would build. You bet!! The first sample was about where I was with my 29 operational amplifiers but was about two square inches in board space with external resistors. It was also about twice as stable as my design when spray canned. But Rich said that I should not be able to see the changes in group delay. I told him to get to a spectrum analyzer and look. Then a new design with external resistors values arrived in the mail. With this design I could bridge the exact resistor values and build the design. Adjustment of the filter took less time than setting up and calibrating the analyzer. I moved one resistor just a little. I then had Bessel performance in the passband and elliptical performance in the stopband. My dream was to have LTC put the resistors inside: NRE 12k to 15k. As dreams sometimes go, others were interested in my vision for those elliptical skirts and LTC decided to put the resistors inside. Thus, I go from 29 operational amplifiers, 30 adjustments and no cigar to a 14-lead package with no adjustments-- and a box of cigars. Want to adjust the skirt edge a little? Just move the clock. Is this magic or what?!

APPENDIX B

Filter Compromises

The LTC1064-7, LTC 1164-7 and LTC1264-7 are the only "Better than Bessel" filters on the market that include all resistors integrated onto the silicon. The obvious question that many designers will have is: Can I do better? Let's explore this.

Let's try to phase equalize the LTC1064-1 elliptic 8th order LP filter. This filter is a very selective filter and, as such, approximates a brick wall filter. Figure B1 shows the group delay response for the LTC1064-1 at a normalized frequency of 1Hz. Our objective is to flatten the group delay curve as much as possible.

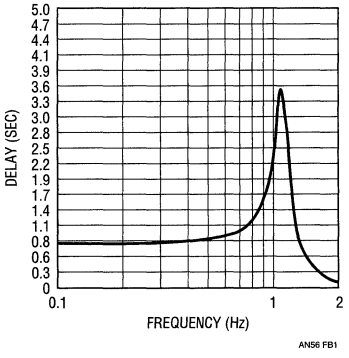


Figure B1. Group Delay Response LTC1064-1, f_{CUTOFF} = 1Hz

Figure B2 shows the architecture used for building allpass filters. For more detailed information see Appendix D. Implementation of the allpass network can be partially done by FilterCAD as shown in Figure B3. Note carefully that to **implement** an allpass network, the f_0, Q and f_n values are entered *only once* into the custom filter design table. See Appendix D if this issue is not clear.

By incorporating the 6th order allpass filter before the LTC1064-1, we have smoothed the variations in the group delay response. Figures B4 and B5 show the group delay response of the system for a 10kHz cutoff frequency. Figures B6 and B7 show the amplitude characteristics.

Note: Each allpass section is very sensitive to the requirement R6/R5 = 1/2 H_{OBP}.

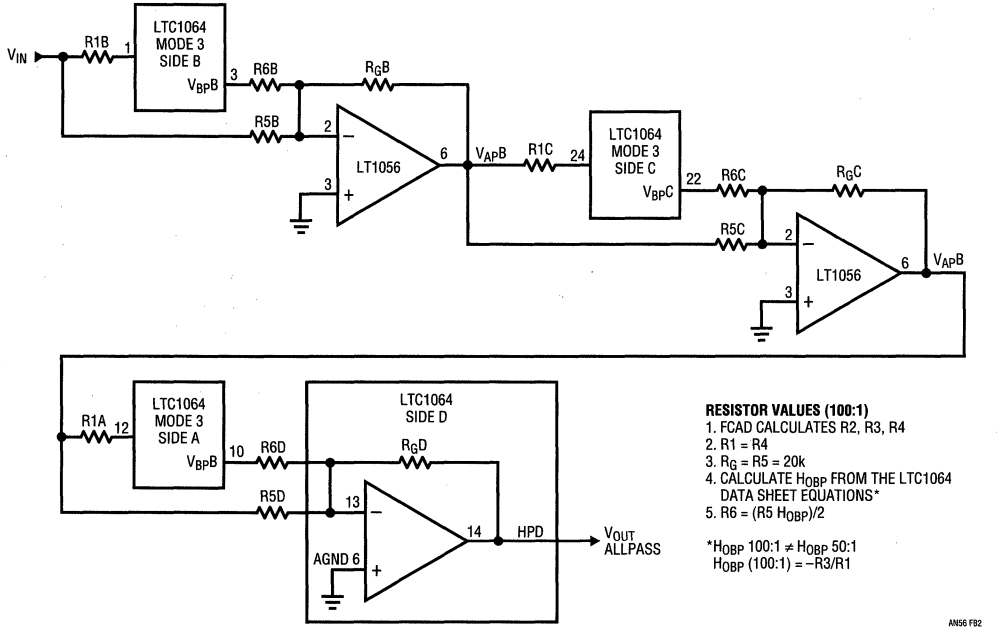


Figure B2. Allpass Network Configuration Using LTC1064

FilterCAD Ver 1.700

FILTER DESCRIPTION: **ALLPASS 6TH ORDER FOR LTC1064-1**

FILTER TYPE:	LOWPASS
FILTER RESPONSE:	CUSTOM
PASSBAND RIPPLE:	0.0000 dB
ATTENUATION:	0.0000 dB
ACTUAL ATTENUATION:	0.0000 dB
FILTER GAIN:	0.0000 dB
ORDER OF FILTER:	6
CORNER/CENTER FREQ:	1.0000 Hz
STOPBAND FREQUENCY:	1.0000 Hz

POLE/ZERO LOCATIONS FOR FILTER

STAGE	Fo	Q	Fn
1	1.0000	0.5470	INFINITE
2	0.7450	0.9430	INFINITE
3	0.5200	0.5470	INFINITE

OPTIMIZE STRATEGY:	NOISE
DEVICE:	LTC1064
CLOCK RATIO:	100:1
CLOCK FREQUENCY:	100.0000 Hz

FILTER STAGE	MODE
1	3
2	3
3	3

RESISTORS (ABSOLUTE VALUES)

STAGE	R1	R2	R3	R4	R5	R6	RG	RH	RL
1		36.56K	20.00K	36.56K	USE GUIDELINES ON ALLPASS				
2		20.00K	25.31K	36.03K	6TH ORDER BLOCK DIAGRAM TO				
3		20.00K	21.03K	73.96K	DETERMINE R1, R5, R6, RG				

RESISTORS (1% VALUES)

STAGE	R1	R2	R3	R4	R5	R6	RG	RH	RL
1	***36.50K***	36.50K	20.00K	36.50K	***20.00K***	***5.40K***	***20.00K***		
2	***35.70K***	20.00K	25.50K	35.70K	***20.00K***	***7.10K***	***20.00K***		
3	***73.20K***	20.00K	21.00K	73.20K	***20.00K***	***2.87K***	***20.00K***		

STAGE	$\lvert H_{OBP}/2 \rvert$	R6/R5
1	0.274	0.270
2	0.357	0.355
3	0.143	0.144

$R6/R5 = 1/2\lvert H_{OBP} \rvert$

H_{OBP} (100:1) = -R3/R1

AN56 FB3

Figure B3. FilterCAD Implementation Screen Used to Calculate Resistors R2, R3 and R4. R1, R5, R6 and R_G Must Be Calculated According to Figure B2's Instructions

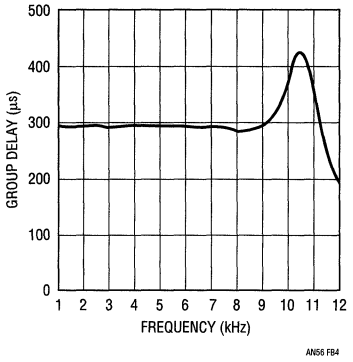


Figure B4. LTC1064 6th Order Allpass Plus LTC1064-1 Group Delay vs Frequency

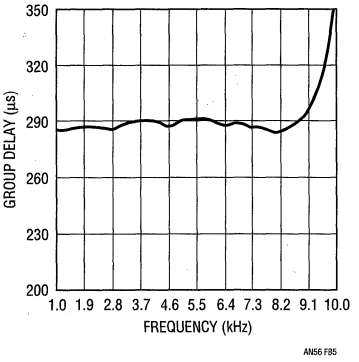


Figure B5. LTC1064 6th Order Allpass Plus LTC1064-1 Detailed Group Delay in Filter Passband

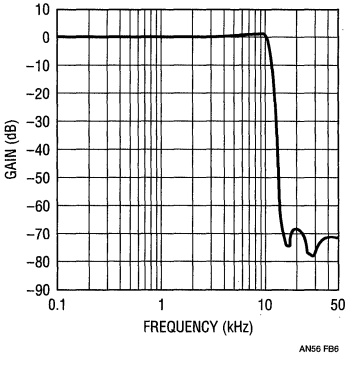


Figure B6. Amplitude Response LTC1064 6th Order Allpass Network Plus LTC1064-1 Elliptic Filter

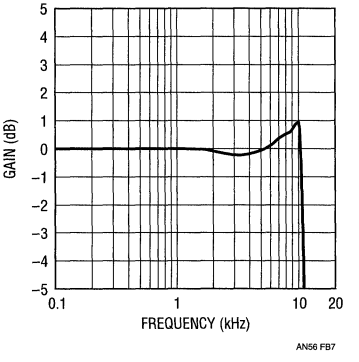


Figure B7. Detailed Amplitude Response LTC1064 6th Order Allpass Network Plus LTC1064-1 Elliptic Filter

APPENDIX C

The LTC1264-7 Filter vs DSP

The LTC1264-7 is the only linear phase "Better than Bessel" filter available in an SO package. Its 250kHz maximum cutoff frequency far exceeds the cutoff frequencies that can be realized with Digital Signal Processing (DSP). A similar DSP Finite Impulse Response (FIR) filter at only 30kHz cutoff frequencies would require approximately 100 filter taps (coefficients) using a multiplier with at least 12-bit precision. Realization of this filter would necessitate 45ns multiplication cycles translating to at least a 22MHz clock frequency. A 250kHz filter would require 5.4ns multiplication cycles and at least a 183MHz clock. These speeds are years, if not a decade, away from realization in silicon.

What about DSP?

The current craze about DSP, while perfectly warranted in many cases, cannot hold a candle to the good old analog switched capacitor approach at frequencies much above 20kHz to 30kHz. Let's see why.

DSP Fundamentals

DSP operates by first digitizing the data via an analog-to-digital converter. Next, the digitized data is digitally filtered by multiplying each digital sample by a "coefficient." Many samples must be multiplied by a coefficient and then "accumulated" in an accumulation register to perform the desired filtering function. The number of coefficients rarely is less than 20 and can sometimes approach 200 in a complex filter.

DSP has advantages and disadvantages like any other technology. DSP filters do not drift over time like op amp RC filters can. They are quite good in approximating the desired filter response characteristics required. Additionally, when the so-called FIR filter is designed, it has linear phase by definition.

DSP is not free, however. Quantization errors in the ADC limit accuracy of the DSP algorithms. Sixteen-bit ADCs, while readily available, generally do not achieve 16-bit accuracy and noise performance even with the best circuit board layout. Quantization errors also creep into the filter coefficients limiting filter performance. Overflow errors in the arithmetic registers can occur without careful software design and have been known to crash the system. Finally, aliasing is a problem with DSP since it is a sampled data system.

DSP and Data Communications

A direct comparison between the switched capacitor approach using the LTC1264-7 and the DSP approach is useful to see how the two approaches compare. Figure C1 shows in block diagram format a DSP filter implemented with discrete registers, multipliers, FIFOs and additional digital circuitry. (The illuminated may exclaim at this point: but what about the TMS320 or the 56001? The illuminated will see why this approach is far too slow.) The circuitry to be of any use at all for speeds useful to data communications must use very fast parts.

Figure C2 shows a DSP filter response calculated using a DSP design program. It is an FIR design and therefore has linear phase. This filter requires a sample rate of 100kHz. As shown, it has a 30kHz cutoff frequency using 12 bits of precision. The DSP program calculates that the filter requires 100 coefficient taps.

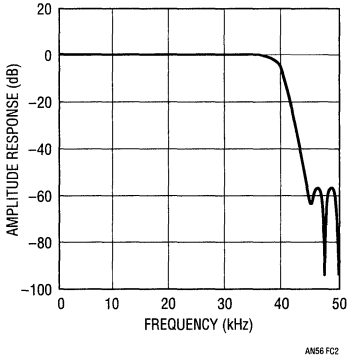


Figure C2. FIR Filter, Kaiser Window, 100ksps, f_{CUTOFF} = 30kHz,12-Bit Precision, 100 Taps

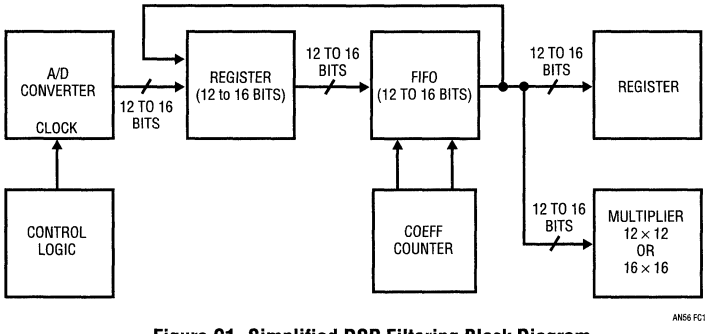


Figure C1. Simplified DSP Filtering Block Diagram

This 30kHz FIR filter would require a 12-bit parallel A/D at its front end. The A/D must convert in less than 45ns. Using a 45ns multiplier/accumulator cycle time, we can calculate:

45ns × 2 cycles (multiply, then accumulate) × 100 taps
= 9µs + 1µs overhead = 10µs

Thus, we need 45ns multipliers to achieve our 30kHz filter which requires a 100kHz sample rate. These multipliers are 1994 state-of-the-art components. They require excellent skills to apply and they are expensive.

The LTC1264-7 Solution Wins

As the above example shows, DSP cannot yet go fast enough to do many of the fundamental filtering requirements for data communications. The 30kHz filter designed in the previous section with DSP can be much more easily implemented by a single switched capacitor filter. The LTC1064-7 linear phase lowpass filter can easily handle the 30kHz requirement. Should the user want to take advantage of the LTC1264-7's 250kHz maximum cutoff frequency, a comparable DSP solution would require blazing fast 5ns multipliers and similarly fast registers and peripheral logic. These type of devices do not exist (as far as I know) today and may not exist until the next century.

APPENDIX D

Designing Allpass Filters (Delay Equalizers) Using FCAD 1.70

Philip Karantzalis

Introduction

While not intended to do so, FilterCAD can be used to design allpass filters for phase equalization and phase shifting applications. FilterCAD, in fact, was used in the design of the LTC1264-7 linear phase filter.

The reader is cautioned that the use of FilterCAD in designing allpass filters is an iterative process which requires patience as well as a thorough knowledge of the required delay characteristics of the filter to be designed. In other words, you must know how much deviation from "flat" group delay your design can tolerate because you can never get absolutely flat group delay.

Using FilterCAD to Design an APF

The FilterCAD software can simulate the delay characteristics of an allpass section when the user enters an equivalent lowpass section into the custom menu twice. This simulates the delay characteristics of an allpass section since a 2nd order allpass section has twice the delay of the equivalent lowpass section.

Since the amplitude response of any allpass section is unity, the amplitude response of the filter should be turned off in FilterCAD so the user can concentrate on optimizing the delay performance.

An Example

Figure D1 shows the normalized custom filter menu for a single 2nd order section lowpass filter with a Q of 2.00. The response plot for this single section LPF is shown in Figure D2. Note that, as described above, the gain response has been turned off, and the graph only shows phase (top) and group delay (bottom).

The next graph, Figure D3, is a composite graph showing the effects of various allpass filters on the lowpass section. Note that each allpass section is simulated by using two entries in the custom table. In this example the f_0 of the allpass section was varied from 0.7 to 1.00 and the Q was varied from 0.52 to 0.55. Note again, that minimization of group delay is a fairly tedious process where the designer is required to do many iterations of the allpass filter section(s). It is recommended that a maximum of two

```
FilterCAD (C) 1988-1990 Linear Technology Corporation

FILTER TYPE:        LOWPASS          Press: ↑ to move cursor UP
FILTER RESPONSE:    CUSTOM                  ↓ to move cursor DOWN
                                            → to move cursor RIGHT
                                            ← to move cursor LEFT
                                            ENTER to ACCEPT data
                                            ESC to RETURN to FILTER MENU
                                            I to enter INFINITY for value
                                            N to change NORMALIZATION value

NORMALIZE TO (Hz):   1.0000
```

	Fo (Hz)	Q	Fn (Hz)		Fo (Hz)	Q	Fn (Hz)
1	1.0000	2.0000	∞	8	0.0000	0.0000	0.0000
2	0.0000	0.0000	0.0000	9	0.0000	0.0000	0.0000
3	0.0000	0.0000	0.0000	10	0.0000	0.0000	0.0000
4	0.0000	0.0000	0.0000	11	0.0000	0.0000	0.0000
5	0.0000	0.0000	0.0000	12	0.0000	0.0000	0.0000
6	0.0000	0.0000	0.0000	13	0.0000	0.0000	0.0000
7	0.0000	0.0000	0.0000	14	0.0000	0.0000	0.0000

AN56 FD1

Figure D1. FilterCAD Menu for 2nd Order Section, Q = 2.00

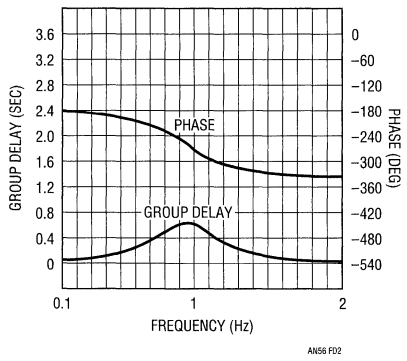


Figure D2. Group Delay and Phase Response of Single 2nd Order Section of Figure D1

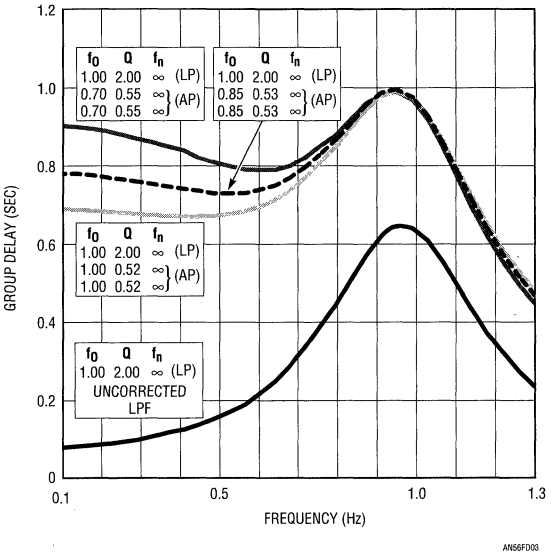


Figure D3. Allpass Group Delay Equalization of a Single 2nd Order LPF

allpass sections be used in an equalized filter design. This will avoid compromising the noise performance of the filter system. However, some elliptic filters may require three or four allpass sections for equalization.

The Hardware—Implementation

Any of LTC's universal filters can be used to implement allpass sections as described in this appendix. Remember that implementation *does not* require each section to be entered twice. See Appendix B.

This example shows how a LTC1064-1 elliptic filter can be equalized up to about 90% of its passband using a 6th order allpass designed by iteration and FCAD graphics. By following this example as a starting point, other filters may be equalized using the same (or similar) design procedure.

FCAD Group Delay Equalization Procedure

1. In lowpass, custom option enter the f_0 and Q values of the filter to be equalized. (Note that f_n values need not be entered.)

2. Below the f_0 and Q values of the lowpass filter enter each allpass f_0 and Q value twice. As explained above, the reason for this is because the delay of an allpass filter is exactly twice that of the equivalent lowpass filter. For this design which uses a 6th order allpass equalizer, three allpass sections must be entered twice.

3. Iterate the values of the f_0 and Q values of the allpass sections only (do not change the values of the lowpass sections) until the desired group delay flatness is obtained. This must be done by alternately viewing the group delay on screen in FCAD and variation of the f_0 and Q values. The procedure is not user friendly or fast, but it can be done and it is certainly faster than the method Bessel used.

The FCAD group delay equalization scheme distorts the gain response plot of the lowpass filter, but this is not a "real" situation since, by definition, the gain response of an allpass filter is unity. This is the reason that we suggest the gain response of the filter under FCAD be toggled off while equalizing. The reason the gain response of the equalized filter is corrupted is because FCAD thinks the allpass sections entered are lowpass filters and calculates their gain as if they were. Thus, the overall equalized response appears as if the lowpass filter we are interested in equalizing has additional lowpass sections added. To reiterate, the correct gain response of the equalized lowpass filter must be calculated in FCAD by using only the lowpass sections of the filter.

The figures show the precise techniques as implemented in FilterCAD for equalizing an LTC1064-1 elliptic filter with a 6th order allpass section. Figure B1 is the non-equalized group delay of the LTC1064-1. This plot was obtained from FCAD by inputting the 4 stages of the LTC1064-1 lowpass filter into the custom lowpass menu and telling FCAD to plot the group delay response.

Figures B4 and B5 illustrate the theoretical group delay response from the fully equalized filter as plotted in FilterCAD.

APPENDIX E

A Reference Table for Rating Lowpass Filters with Constant Group Delay

Bessel and "Better than Bessel" filters are not the only filters with flat group delay. While these filters do have better characteristics than other filters because they have constant group delay to twice f_C and to f_C, respectively, there is another filter that can be used in some situations. This is the trusty Butterworth filter. While the eye diagram of the Butterworth filter may not look pretty, reasonable results may be obtained by using only part of the passband of the filter when more attenuation is needed (in the stopband) than the Dash 7 type of filter achieves. Table E1 summarizes the Group Delay and attenuation specifications for several filters. The table may be used as a simple selection guide.

Table E1. Flat Group Delay Filter Design Table

FILTER	GROUP DELAY	ATTENUATION (dB)		
(Filters are Normalized to $f_C = 1$)		At $f_C = 2$	At $f_C = 3$	At $f_C = 4$
Dash 7 Better than Bessel	Flat to $f_C = 1$	−36	−69	−77
Dash 3 Bessel	Flat to $f_C = 1.912$	−13.3	−32.7	−51.6
Dash 2 Butterworth	Flat to $f_C = 0.376$*	−49	−76	−96
	Flat to $f_C = 0.494$**	−49	−76	−96

* Flat group delay to +5%
** Flat group delay to +10%

Video Circuit Collection

Frank Cox

INTRODUCTION

Even in a time of rapidly advancing digital image processing, analog video signal processing still remains eminently viable. The video A/D converters need a supply of properly amplified, limited, DC restored, clamped, clipped, contoured, multiplexed, faded and filtered analog video before they can accomplish anything. After the digital magic is performed, there is usually more amplifying and filtering to do as an adjunct to the D/A conversion process, not to mention all those pesky cables to drive. The analog way is often the most expedient and efficient, and you don't have to write all that code.

The foregoing is only partly in jest. The experienced engineer will use whatever method will properly get the job done; analog, digital or magic (more realistically, a combination of all three). Presented here is a collection of analog video circuits that have proven themselves useful.

CIRCUIT INDEX

VIDEO AMPLIFIER SELECTION GUIDE

PART	GBW (MHz)	CONFIGURATION	COMMENTS
LT1217	10	S	CFA, I_S = 1mA, Shutdown
LT1200/LT1201/ LT1202	11	S, D, Q	I_S = 1mA per Amp, Good DC Specs
LT1355/LT1356	12	D, Q	400V/µs SR, I_S = 1.25mA per Amp, Good DC Specs
LT1211/LT1212	14	D, Q	Single Supply, Excellent DC Specs
LT1215/LT1216	23	D, Q	Single Supply, Excellent DC Specs
LT1358/LT1359	25	D, Q	600V/µs SR, I_S = 2.5mA per Amp, Good DC Specs
LT1213/LT1214	28	D, Q	Single Supply, Excellent DC Specs
LT1208/LT1209	45	D, Q	400V/µs SR
LT1220	45	S	250V/µs, Good DC Specs, 12-Bit Accurate
LT1224	45	S	400V/µs SR
LT1190	50	S	Low Voltage
LT1360	50	S	800V/µs SR, I_S = 5mA per Amp, Good DC Specs
LT1206	60	S	250mA Output Current CFA, 600V/µs SR, Shutdown
LT1363	70	S	1000V/µs SR, I_S = 7.5mA per Amp, Good DC Specs
LT1204	70	Q	CFA, 4-Input Video MUX Amp, 1000V/µs SR, Superior Isolation
LT1228	80 (g_m = 0.25)	S	Transconductance Amp + CFA, Extremely Versatile
LT1191	90	S	Low Voltage, ±50mA Output
LT1229/LT1230	100	D, Q	CFA, 1000V/µs SR, DG = 0.04%, DP = 0.1°
LT1223	100	S	CFA, 12-Bit Accurate, Shutdown, 1300V/µs SR, Good DC Specs, DG = 0.02%, DP = 0.12°
LT1252	100	S	CFA, DG = 0.01%, DP = 0.09°, Low Cost
LT1253	117	D, Q	CFA, DG = 0.03%, DP = 0.28°, Flat to 30MHz, 0.1dB
LT1259/LT1260	130	D, T	RGB CFA, 0.1dB Flat to 30MHz, DG = 0.016%, DP = 0.075°, Shutdown
LT1227	140	S	CFA, 1100V/µs SR, DG = 0.01%, DP = 0.01°, Shutdown
LT1221	150 (A_V = 4)	S	250V/µs SR, 12-Bit Accurate
LT1193	160 (A_V = 2)	S	Low Voltage, Differential Input, Adjustable Gain, ±50mA Output
LT1203/LT1205	170	D, Q	MUX, 25ns Switching, DG = 0.02%, DP = 0.04°
LT1192	350 (A_V = 5)	S	Low Voltage, ±50mA Output
LT1194	350 (A_V = 10)	S	Differential Input, Low Voltage, Fixed Gain of 10
LT1222	500 (A_V = 10)	S	12-Bit Accurate
LT1226	1000 (A_V = 25)	S	400V/µs SR, Good DC Specs

Key to Abbreviations:

CFA = Current Feedback Amplifier
DG = Differential Gain
DP = Differential Phase
MUX = Multiplexer
SR = Slew Rate

S = Single
D = Dual
Q = Quad
T = Triple

Note:

Differential gain and phase is measured with a 150Ω load, except for the LT1203/LT1205 in which case the load is 1000Ω.

VIDEO PROCESSING CIRCUITS

Variable Gain Amplifier Has ±3dB Range While Maintaining Good Differential Gain and Phase

The circuit in Figure 1 is a variable gain amp suitable for composite video use. Feedback around the transconductance amp (LT1228) acts to reduce the differential input voltage at the amplifier's input, and this reduces the differential gain and phase errors. Table 1 shows the differential phase and gain for three gains. Signal-to-noise ratio is better than 60dB for all gains.

Table 1.

INPUT (V)	I_{SET} (mA)	DIFFERENTIAL GAIN	DIFFERENTIAL PHASE
0.707	4.05	0.4%	0.15°
1.0	1.51	0.4%	0.1°
1.414	0.81	0.7%	0.5°

Black Clamp

Here is a circuit that removes the sync component of the video signal with minimal disturbance to the luminance (picture information) component. It is based on the classic op amp half-wave-rectifier with the addition of a few refinements.

The classic "diode-in-the-feedback-loop" half-wave-rectifier circuit generally does not work well with video frequency signals. As the input signal swings through zero volts, one of the diodes turns on while the other is turned off, hence the op amp must slew through two diode drops. During this time the amplifier is in slew limit and the output signal is distorted. It is not possible to entirely prevent this source of error because there will always be some time when the amp will be open-loop (slewing) as the diodes are switched, but the circuit shown here in Figure 2 minimizes the error by careful design.

The following techniques are critical in the design shown in Figure 2:

1. The use of diodes with a low forward voltage drop reduces the voltage that the amp must slew.

2. Diodes with a low junction capacitance reduce the capacitive load on the op amp. Schottky diodes are a good choice here as they have both low forward voltage and low junction capacitance.

3. A fast slewing op amp with good output drive is essential. An excellent CFA like the LT1227 is mandatory for good results.

4. Take some gain. The error contribution of the diode switch tends to be constant, so a larger signal means a smaller percentage error.

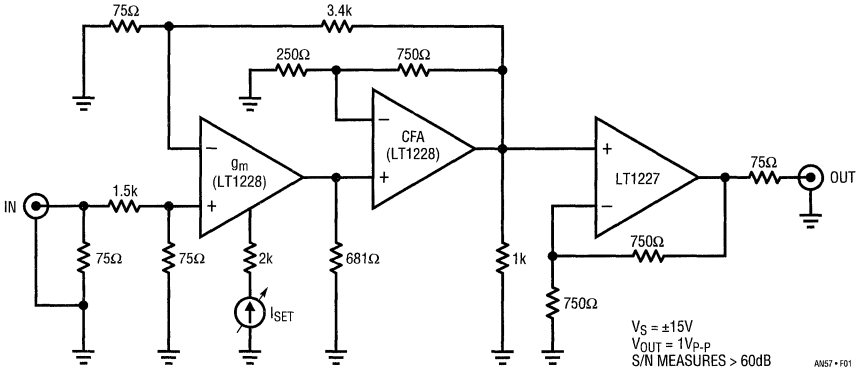


Figure 1. ±3dB Variable Gain Video Amp Optimized for Differential Gain and Phase

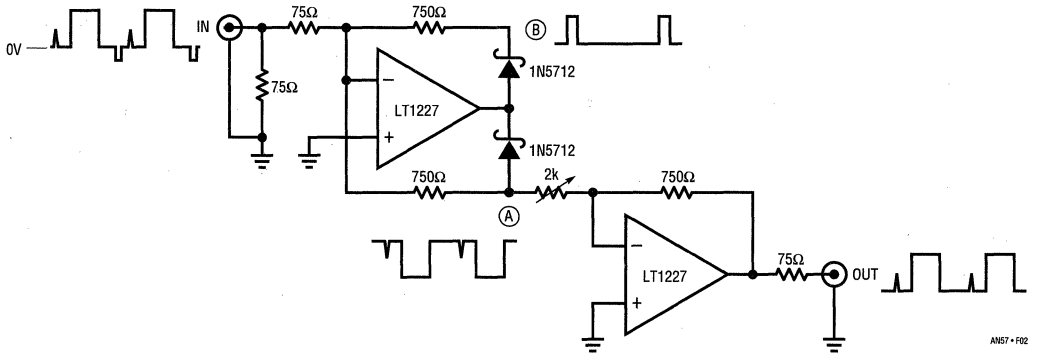


Figure 2. Black Clamp Circuit

Since this circuit discriminates between the sync and video on the basis of polarity, it is necessary to have an input video signal that has been DC restored (the average DC level is automatically adjusted to bring the blanking level to zero volts). Notice that not only is the positive polarity information (luminance: point A in the schematic) available, but that the negative polarity information (sync: point B in the schematic) is also. Circuits that perform this function are called "black clamps." The photograph (Figure 3) shows the circuit's clean response to a 1T[1] pulse (some extra delay is added between the input and output for clarity).

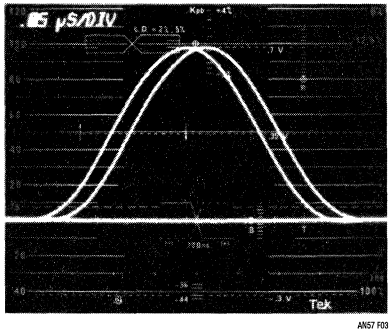


Figure 3. Black Clamp Circuit Response to a "1T" Pulse (±15V Power Supplies)

Video Limiter

Often there is a need to limit the amplitude excursions of the video signal. This is done to avoid exceeding luminance reference levels of the video standard being used, or to avoid exceeding the input range of another processing stage such as an A/D converter. The signal can be hard limited in the positive direction, a process called "white peak clipping," but this destroys any amplitude information and hence any scene detail in this region. A more gradual limiting ("soft limiter") or compression of the peak white excursion is performed by elements called "knee" circuits, after the shape of the amplifier transfer curve.

A soft limiter circuit is shown in Figure 4 which uses the LT1228 transconductance amp. The level at which the limiting action begins is adjusted by varying the set current into pin 5 of the transconductance amplifier. The LT1228 is used here in a slightly unusual, closed-loop configuration. The closed-loop gain is set by the feedback and gain resistors (R_F and R_G) and the open-loop gain by the transconductance of the first stage times the gain of the CFA.

[1] A 1T pulse is a specialized video waveform whose salient characteristic is a carefully controlled bandwidth which is used to quickly quantify gain and phase flatness in video systems. Phase shift and/or gain variations in the video system's passband result in transient distortions which are very noticeable on this waveform (not to mention the picture). [For you video experts out there, the K factor was 0.4% (the TEK TSG120 video signal generator has a K factor of 0.3%)].

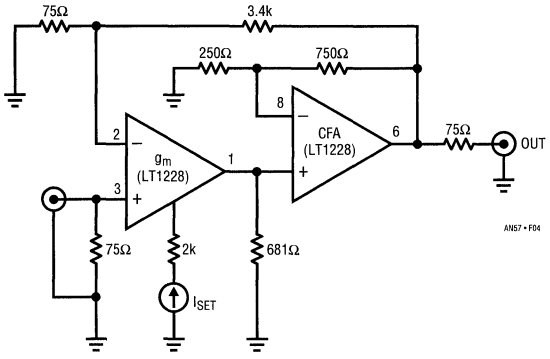


Figure 4. LT1228 Soft Limiter

As the transconductance is reduced (by reducing the set current), the open-loop gain is reduced below that which can support the closed-loop gain and the amp limits. A family of curves which show the response of the limiting amplifier subject to different values of set current with a ramp input is shown in Figure 5. Figure 6 shows the change in limiting level as I_{SET} is varied.

Circuit for Gamma Correction

Video systems use transducers to convert light to an electric signal. This conversion occurs, for example, when a camera scans an image. Video systems also use transducers to convert the video signal back to light when the signal is sent to a display, a CRT monitor for example. Transducers often have a transfer function (the ratio of *signal in to light out*) that is unacceptably nonlinear.

The newer generation of camera transducers (CCDs and the improved versions of vidicon-like tubes) are adequately linear, however, picture monitor CRTs are not. The transfer functions of most CRTs follow a power law. The following equation shows this relation:

$$\text{Light Out} = k \bullet V_{SIG}^{\gamma}$$

where k is a constant of proportionality and gamma (γ) is the exponent of the power law (gamma ranges from 2.0 to 2.4).

This deviation from nonlinearity is usually called just *gamma* and is reported as the exponent of the power law. For instance, "the gamma of this vidicon is 0.43." The correction of this effect is *gamma correction*.

In the equation above, notice that a gamma value of 1 results in a linear transfer function. The typical CRT will have a transfer function with a gamma from about 2.0 to 2.4. Such values of gamma give a nonlinear response which compresses the blacks and stretches the whites. Cameras usually contain a circuit to correct this nonlinearity. Such a circuit is a *gamma corrector* or simply a *gamma circuit*.

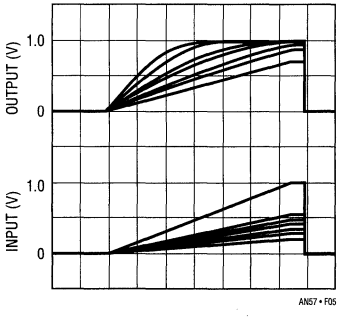


Figure 5. Output of the Limiting Amp (I_{SET} = 0.68mA), with a Ramp Input. As the Input Amplitude Increases from 0.25V to 1V, the Output is Limited to 1V

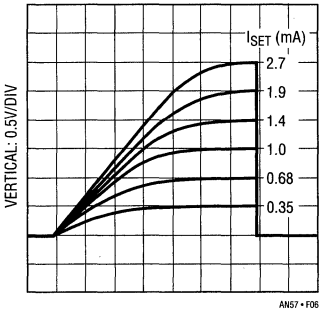


Figure 6. The Output of the Limiting Amp with Various Limiting Levels (I_{SET}). The Input is a Ramp with a Maximum Amplitude of 0.75V

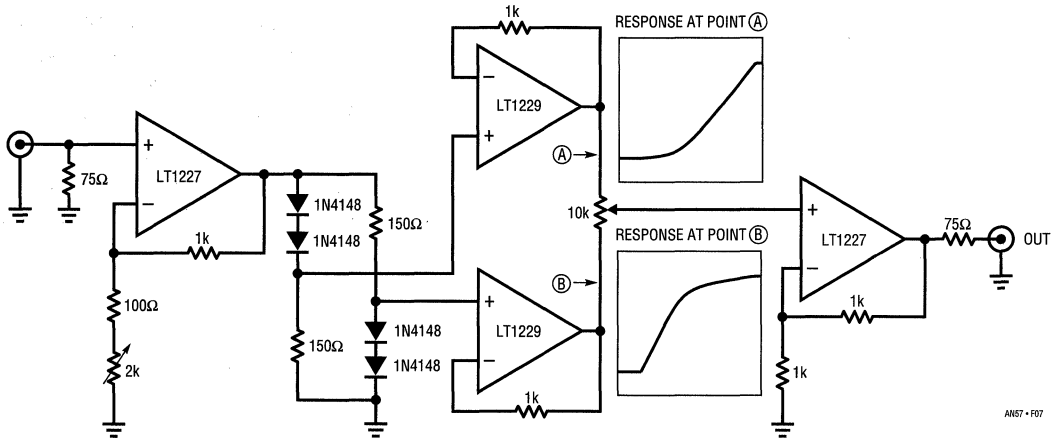


Figure 7. Gamma Amp (Input Video Should Be Clamped)

Figure 7 shows a schematic of a typical circuit which can correct for positive or negative gamma. This is an upgrade of a classic circuit which uses diodes as the nonlinear elements. The temperature variation of the diode junction voltages is compensated to the first order by the balanced arrangement. LT1227s and LT1229s were used in the prototype, but a quad (LT1230) could save some space and work as well.

Figure 8 shows a response curve (transfer function) for an uncorrected CRT. To make such a response linear, the gamma corrector must have a gamma that is the reciprocal of the gamma of the device being linearized. Figure 8, curve A shows a response curve (transfer function) for an uncorrected CRT. The response of a two diode gamma circuit like that in Figure 7 is shown in Figure 8, curve B. Summing these two curves together, as in Figure 8, curve C, demonstrates the action of the gamma corrector. A straight line of appropriate slope, which would be an ideal response, is shown for comparison in Figure 8, curve D. Figure 9 is a triple exposure photograph of the gamma corrector circuit adjusted for gammas of –3, 1 and +3 (approximately). The input is a linear ramp of duration 52µs which is the period of an active horizontal line in NTSC video.

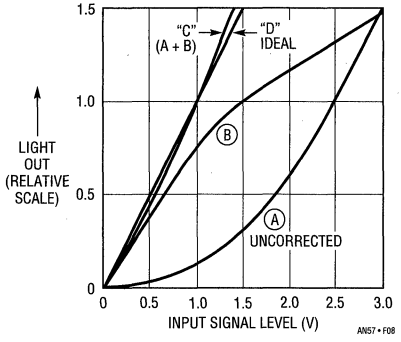


Figure 8. Uncorrected CRT Transfer Function

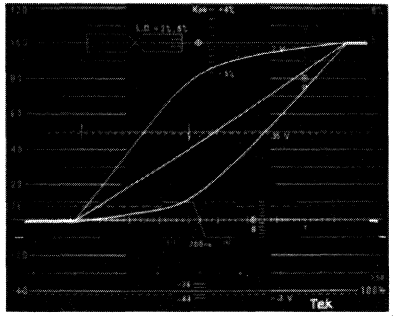


Figure 9. Gamma Corrector Circuit Adjusted for Three Gammas: –3, 1, +3 (Approximately). The Input is a Linear Ramp

LT1228 Sync Summer

The circuit shown in Figure 10a restores the DC level and adds sync to a video waveform. For this example the video source is a high speed DAC with an output which is referenced to –1.2V. The LT1228 circuit (see the LT1228 data sheet for more details) forms a DC restore[2] that maintains a zero volt DC reference for the video. Figure 10b shows the waveform from the DAC, the DC restore pulse, and composite sync. The LT1363 circuit sums the video and composite sync signals. The 74AC04 CMOS inverters are used to buffer the TTL composite sync signal. In addition they drive the shaping network and, as they are mounted on the same ground plane as the analog circuitry, they isolate the ground noise from the digital system used to generate the video timing signals. Since the sync is directly summed to the video, any ground bounce or noise gets added in too. The shaping network is simply a third order Bessel lowpass filter with a bandwidth of 5MHz and an impedance of 300Ω. This circuitry slows the edge rate of the digital composite sync signal and also attenuates the noise. The same network, rescaled to an impedance of 75Ω, is used on the output of the summing amp to attenuate the switching noise from the DAC and to remove some of the high frequency components of the waveform. A more selective filter is not used here as the DAC has low glitch energy to start with and the signal does not have to meet stringent bandwidth requirements. The LT1363 used for the summing amp has excellent transient characteristics with no overshoot or ringing. Figure 10c shows two

[2] This is also referred to as "DC clamp" (or just clamp) but, there is a distinction. Both clamps and DC restore circuits act to maintain the proper DC level in a video signal by forcing the blanking level to be either zero volts or some other appropriate value. This is necessary because the video signal is often AC coupled as in a tape recorder or a transmitter. The DC level of an AC coupled video signal will vary with scene content and therefore the black referenced level must be "restored" in order for the picture to look right. A clamp is differentiated from a DC restore by its speed of response. A clamp is faster, generally correcting the DC error in one horizontal line (63.5µs for NTSC). A DC restore responds slower, more on the order of the frame time (16.7ms for NTSC). If there is any noise on the video signal the DC restore is the preferred method. A clamp can respond to noise pulses that occur during the blanking period and as a result give an erroneous black level for the line. Enough noise causes the picture to have an objectionable distortion called "piano keying." The black reference level and hence the luminance level change from line to line.

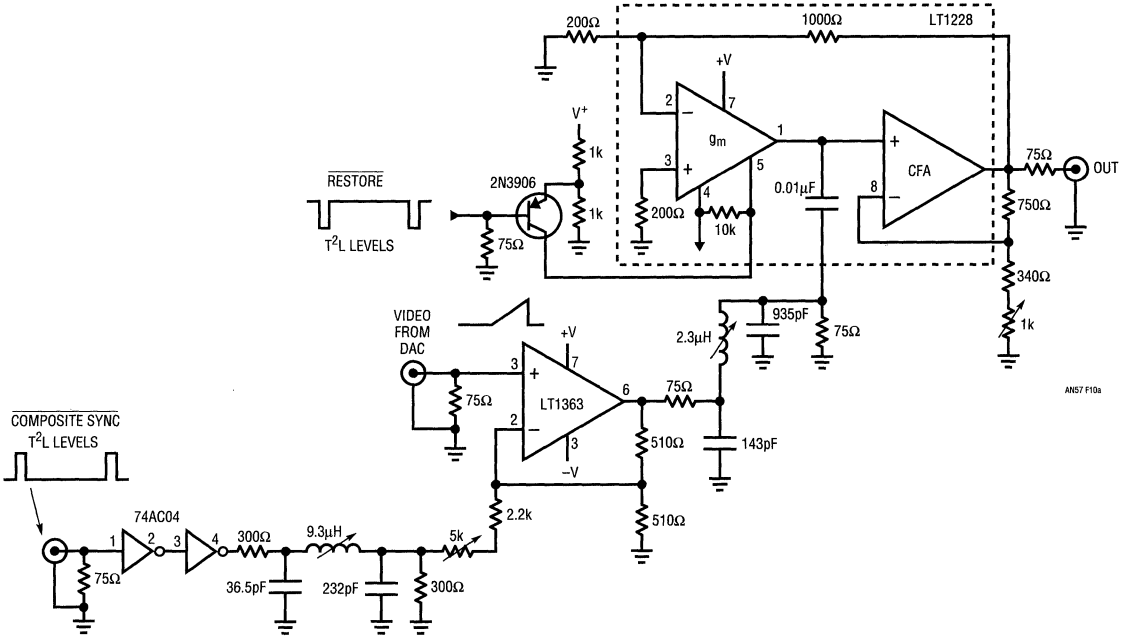
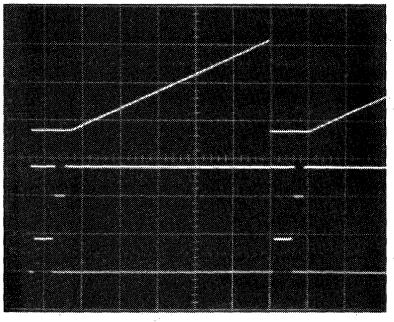
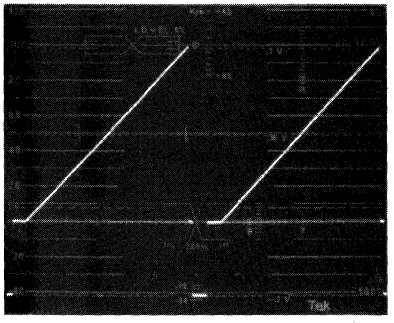


Figure 10a. Simple Sync Summer



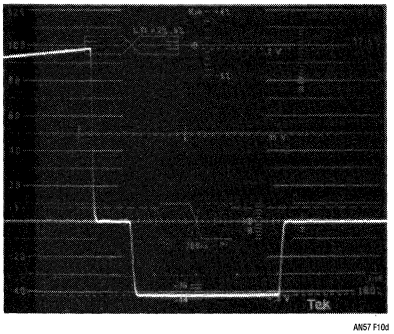
AN57 F10b

Figure 10b. Video Waveform from DAC; Clamp Pulse and Sync Pulse Used as Inputs to Sync Summer



AN57 F10c

Figure 10c. Reconstructed Video Out of Sync Summer



AN57 F10d

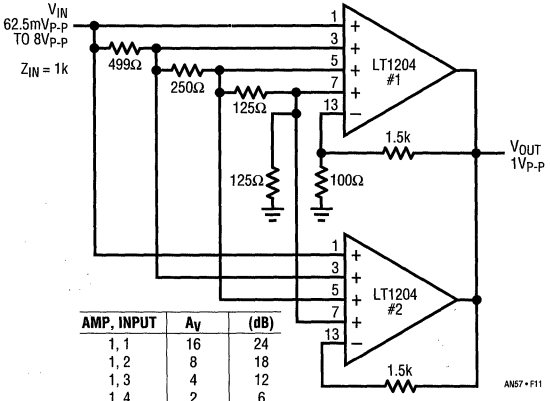
Figure 10d. Close-Up of Figure 10c, Showing Sync Pulse

horizontal lines of the output waveform with the DC restored and the sync added. Figure 10d is an expanded view of the banking interval showing a clean, well formed sync pulse.

LT1204 70MHz MULTIPLEXER CIRCUITS

Stepped Gain Amp Using the LT1204

This is a straightforward approach to a switched-gain amp that features versatility. Figures 11 and 12 show circuits which implement a switched-gain amplifier; Figure 11 features an input Z of 1000Ω, while Figure 12's input Z is 75Ω. In either circuit, when LT1204 amp/MUX #2 is selected the signal is gained by one, or is attenuated by the resistor divider string depending on the input selected. When LT1204 amp/MUX #1 is selected there is an additional gain of sixteen. Consult the table in Figure 11. The gain steps can be either larger or smaller than shown here. The input impedance (the sum of the divider resistors) is also arbitrary. Exercise caution in taking large gains however, because the bandwidth will change as the output is switched from one amp to another. Taking more gain in the amp/MUX #1 will lower its bandwidth even though it is a current feedback amplifier (CFA). This is less true for a CFA than for a voltage feedback amp.



AMP, INPUT	A_V	(dB)
1, 1	16	24
1, 2	8	18
1, 3	4	12
1, 4	2	6
2, 1	1	0
2, 2	0.5	–6
2, 3	0.25	–12
2, 4	0.125	–18

Figure 11. Switchable Gain Amplifier Accepts Inputs from 62.5mVP-P to 8VP-P

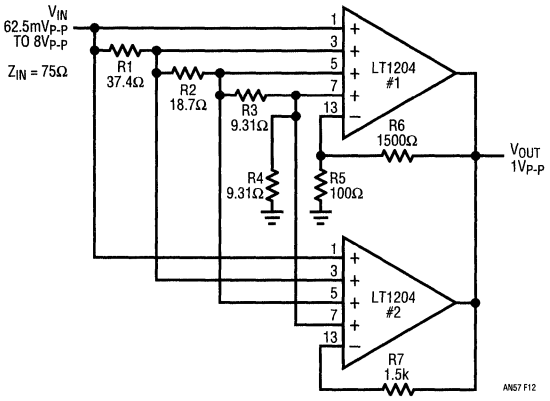


Figure 12. Switchable Gain Amplifier, Z_{IN} = 75Ω Same Gains as Figure 11

LT1204 Amplifier/Multiplexer Sends Video Over Long Twisted Pair

Figure 13 is a circuit which can transmit baseband video over more than 1000 feet of very inexpensive twisted-pair wire and allow the selection of one-of-four inputs. Amp/MUX A1 (LT1204) and A2 (LT1227) form a single differential driver. A3 is a variable gain differential receiver built using the LT1193. The rather elaborate equalization (highlighted on the schematic) is necessary here as the twisted pair goes self-resonant at about 3.8MHz.

Figure 14 shows the video test signal before and after transmission but without equalization. Figure 15 shows before and after with the equalization connected. Differential gain and phase are about 1% and 1°, respectively.

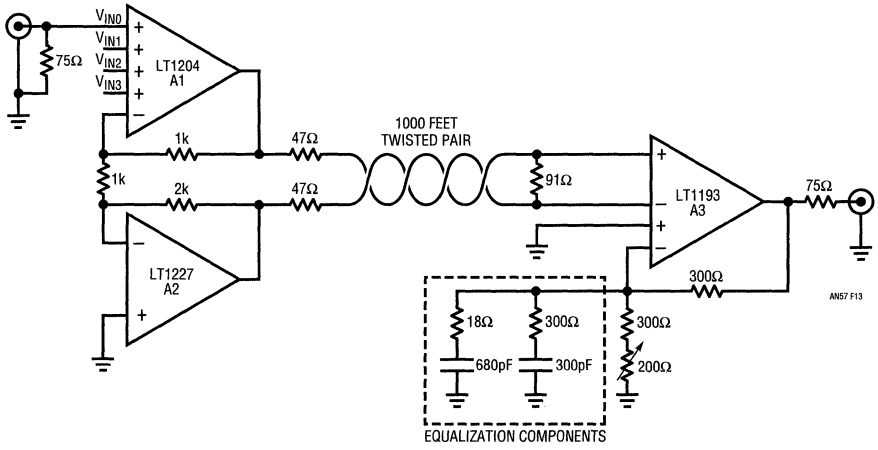


Figure 13. Twisted Pair Driver/Receiver

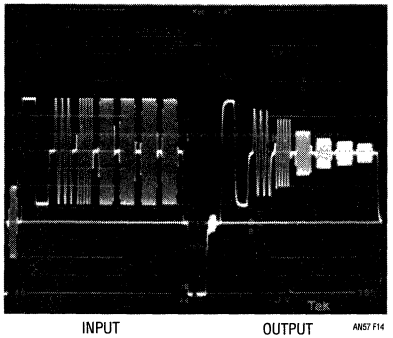


Figure 14. Multiburst Pattern Without Cable Compensation

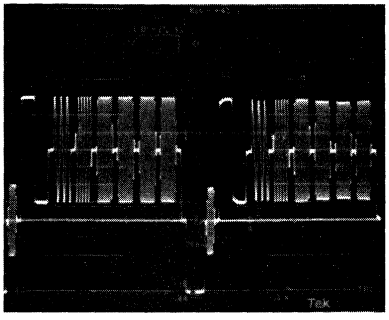


Figure 15. Multiburst Pattern With Cable Compensation

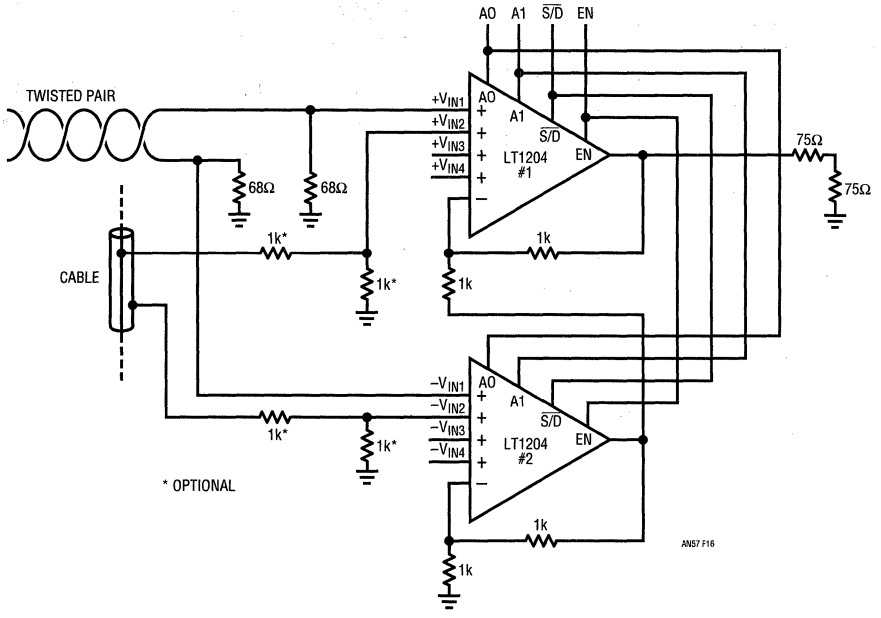


Figure 16. Fast Differential Multiplexer

Fast Differential Multiplexer

This circuit (Figure 16) takes advantage of the gain node on the LT1204 to make a high speed differential MUX for receiving analog signals over twisted pair. Common-mode noise on loop-through connections is reduced because of the unique differential input. Figure 15's circuit also makes a robust differential to single-ended amp/MUX for high speed data acquisition.

Signals passing through LT1204 #1 see a noninverting gain of two. Signals passing through LT1204 #2 also see a noninverting gain of two and then an inverting gain of one (for a resultant gain of minus two) because this amp drives the gain resistor on amp #1. The result is differential amplification of the input signal.

The optional resistors on the second input are for input protection. Figure 17 shows the differential mode response versus frequency. The limit to the response (at low frequency) is the matching of the gain resistors. One percent resistors will match to about 0.1% (60dB) if they are from the same batch.

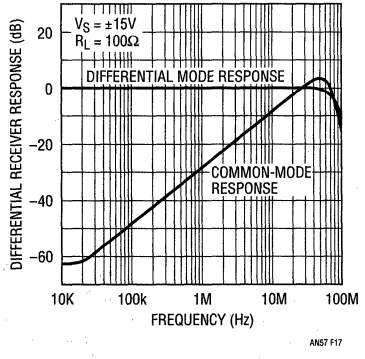


Figure 17. Differential Receiver Response vs Frequency

MISAPPLICATIONS OF CFAs

In general the current feedback amplifier (CFA) is remarkably docile and easy to use. These amplifiers feature "real," usable gain to 100MHz and beyond, low power consumption and an amazingly low price. However, CFAs are still new enough so that there is room for breadboard adventure. Consult the diagrams and the following list for some of the pitfalls that have come to my attention[3].

1. Be sure there is a DC path to ground on the noninverting input pin. There is a transistor in the input that needs some bias current.

2. Don't use pure reactances for a feedback element. This is one sure way to get the CFA to oscillate. Consult the amplifier data sheet for guidance on feedback resistor values. Remember that these values have a direct effect on the bandwidth. If you wish to tailor frequency response with reactive networks, put them in place of R_G, the gain setting resistor.

3. Need a noninverting buffer? Use a feedback resistor!

4. Any resistance between the inverting terminal and the feedback node causes loss of bandwidth.

5. For good dynamic response, avoid parasitic capacitance on the inverting input.

6. Don't use a high Q inductor for power supply decoupling (or even a middling Q inductor for that matter). The inductor and the bypass capacitors form a tank circuit, which can be excited by the AC power supply currents, causing just the opposite of the desired effect. A lossy ferrite choke can be a very effective way to decouple power supply leads without the voltage drop of a series resistor. For more information on ferrites call Fair Rite Products Corp. (914) 895-2055.

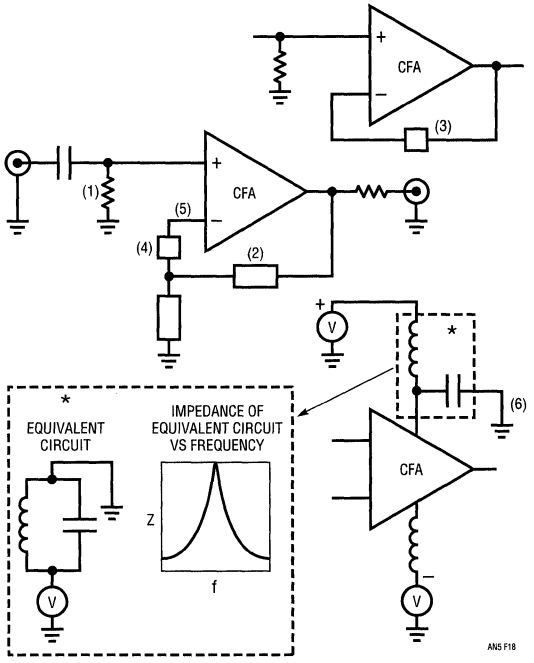


Figure 18. Examples of Misapplications

[3] All the usual rules for any high speed circuit still apply, of course.
A partial list:
a. Use a ground plane.
b. Use good RF bypass techniques. Capacitors used should have short leads, high self-resonant frequency, and be placed close to the pin.
c. Keep values of resistors low to minimize the effects of parasitics. Make sure the amplifier can drive the chosen low impedance.
d. Use transmission lines (coax, twisted pair) to run signals more than a few inches.
e. Terminate the transmission lines (back terminate the lines if you can).
f. Use resistors that are still resistors at 100MHz.
Refer to AN47 for a discussion of these topics.

APPENDICES — VIDEO CIRCUITS FROM LINEAR TECHNOLOGY MAGAZINE

APPENDIX A

A Temperature-Compensated, Voltage-Controlled Gain Amplifier Using the LT1228

It is often convenient to control the gain of a video or intermediate frequency (IF) circuit with a voltage. The LT1228, along with a suitable voltage-to-current converter circuit, forms a versatile gain-control building block ideal for many of these applications.

In addition to gain control over video bandwidths, this circuit can add a differential input and has sufficient output drive for 50Ω systems.

The transconductance of the LT1228 is inversely proportional to absolute temperature at a rate of –0.33%/°C. For circuits using closed-loop gain control (i.e., IF or video automatic gain control) this temperature coefficient does not present a problem. However, open-loop gain-control circuits that require accurate gains may require some compensation. The circuit described here uses a simple thermistor network in the voltage-to-current converter to achieve this compensation. Table A1 summarizes the circuit's performance.

Figure A1 shows the complete schematic of the gain-control amplifier. Please note that these component choices are not the only ones that will work nor are they necessarily the best. This circuit is intended to demonstrate one approach out of many for this very versatile part and, as always, the designer's engineering judgment must be fully engaged. Selection of the values for the input attenuator, gain-set resistor, and current feedback amplifier resistors is relatively straightforward, although some iteration is usually necessary. For the best bandwidth, remember to keep the gain-set resistor R1 as small as possible and the set current as large as possible with due regard for gain compression. See the "Voltage-Controlled Current Source" (I_{SET}) box for details.

Table A1. Characteristics of Example

Input Signal Range	0.5V to 3.0V_{PK}
Desired Output Voltage	1.0V_{PK}
Frequency Range	0Hz to 5MHz
Operating Temperature Range	0°C to 50°C
Supply Voltages	±15V
Output Load	150Ω (75Ω + 75Ω)
Control Voltage vs Gain Relationship	0V to 5V Min to Max Gain
Gain Variation Over Temperature	±3% from Gain at 25°C

Several of these circuits have been built and tested using various gain options and different thermistor values. Test results for one of these circuits are shown in Figure A2. The gain error versus temperature for this circuit is well within the limit of ±3%. Compensation over a much wider

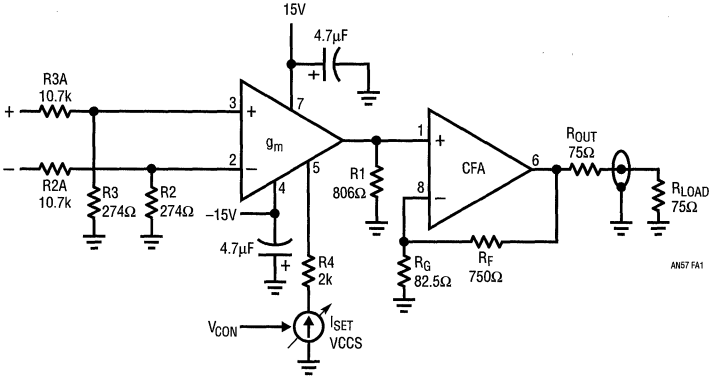


Figure A1. Differential-Input, Variable-Gain Amplifier

range of temperatures or to tighter tolerances is possible, but would generally require more sophisticated methods, such as multiple thermistor networks.

The VCCS is a standard circuit with the exception of the current-set resistor R5, which is made to have a temperature coefficient of –0.33%/°C. R6 sets the overall gain and is made adjustable to trim out the initial tolerance in the LT1228 gain characteristic. A resistor (R_P) in parallel with the thermistor will tend, over a relatively small range, to linearize the change in resistance of the combination with temperature. R_S trims the temperature coefficient of the network to the desired value.

This procedure was performed using a variety of thermistors. BetaTHERM Corporation is one possible source, phone 508-842-0516. Figure A3 shows typical results reported as errors normalized to a resistance with a –0.33%/°C temperature coefficient. As a practical matter, the thermistor need only have about a 10% tolerance for this gain accuracy. The sensitivity of the gain accuracy to the thermistor tolerance is decreased by the linearization network in the same ratio as is the temperature coefficient. The room temperature gain may be trimmed with R6. Of course, particular applications require analysis of aging stability, interchangeability, package style, cost, and the contributions of the tolerances of the other components in the circuit.

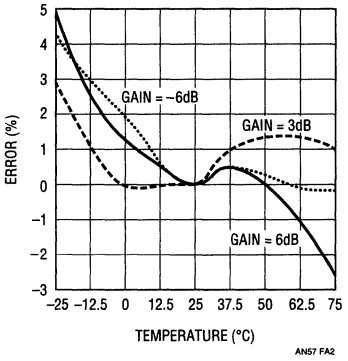


Figure A2. Gain Error for Circuit in Figure 18 Plus Temperature Compensation Circuit Shown in Figure 20 (Normalized to Gain at 25°C)

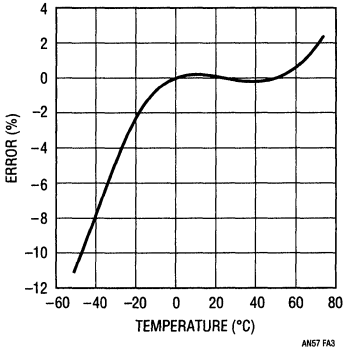


Figure A3. Thermistor Network Resistance Normalized to a Resistor with Exact –0.33%/°C Temperature Coefficient

Voltage-Controlled Current Source (VCCS) with a Compensating Temperature Coefficient

VCCS Design Steps

1. Measure, or obtain from the data sheet, the thermistor resistance at three equally spaced temperatures (in this case 0°C, 25°C, and 50°C). Find R_P from:

$$R_P = \frac{(R0 \times R25 + R25 \times R50 - 2 \times R0 \times R50)}{(R0 + R50 - 2 \times R25)}$$

where R0 = thermistor resistance at 0°C
R25 = thermistor resistance at 25°C
R50 = thermistor resistance at 50°C

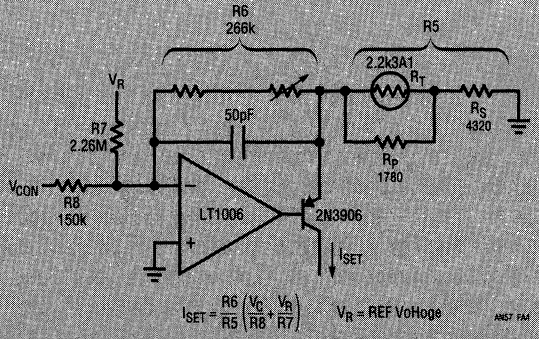


Figure A4. Voltage-Controlled Current Source (VCCS) with a Compensating Temperature Coefficient

2. Resistor R_P is placed in parallel with the thermistor. This network has a temperature dependence that is approximately linear over the range given (0°C to 50°C).

3. The parallel combination of the thermistor and R_P ($R_P||R_T$) has a temperature coefficient (TC) of resistance given by:

$$\text{TC of } R_P \,||\, R_T = \left(\frac{R0\,||\,R_P - R50\,||\,R_P}{R25\,||\,R_P}\right)\left(\frac{100}{T_{HIGH} - T_{LOW}}\right)$$

4. The desired tempco to compensate the LT1228 gain temperature dependence is –0.33%/°C. A series resistance (R_S) is added to the parallel network to trim its tempco to the proper value. R_S is given by:

$$\frac{\left(\text{TC of } R_P \,||\, R_T\right)}{-0.33} \times \left(R_P \,||\, R_{25}\right) - \left(R_P \,||\, R_{25}\right)$$

5. R6 contributes to the resultant TC and so is made large with respect to R5.

6. The other resistors are calculated to give the desired range of I_{SET}.

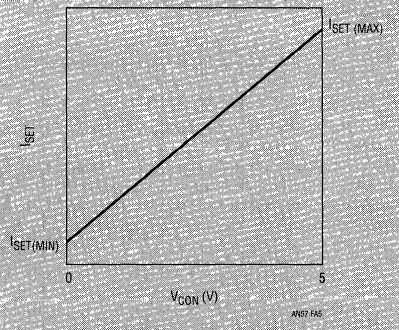


Figure A5. Voltage Control of I_{SET} with Temperature Compensation

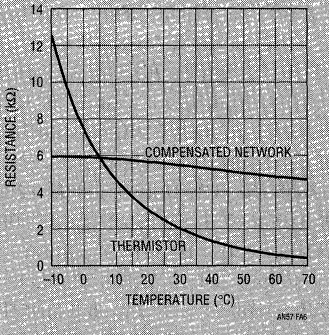


Figure A6. Thermistor and Thermistor Network Resistance vs Temperature

APPENDIX B

Optimizing a Video Gain-Control Stage Using the LT1228

Video automatic-gain-control (AGC) systems require a voltage- or current-controlled gain element. The performance of this gain-control element is often a limiting factor in the overall performance of the AGC loop. The gain element is subject to several, often conflicting restraints. This is especially true of AGC for composite color video systems, such as NTSC, which have exacting phase- and gain-distortion requirements. To preserve the best possible signal-to-noise ratio (S/N),[1] it is desirable for the input signal level to be as large as practical. Obviously, the larger the input signal the less the S/N will be degraded by the noise contribution of the gain-control stage. On the other hand, the gain-control element is subject to dynamic range constraints; exceeding these will result in rising levels of distortion.

Linear Technology makes a high speed transconductance (g_m) amplifier, the LT1228, which can be used as a quality, inexpensive gain-control element in color video and some lower frequency R_F applications. Extracting the optimum performance from video AGC systems takes careful attention to circuit details.

[1] Signal-to-noise ratio, S/N = 20 × log(RMS signal/RMS noise).

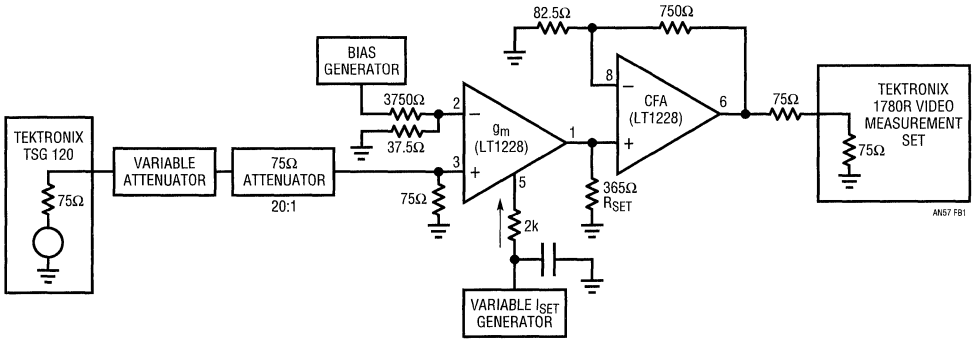


Figure B1. Schematic Diagram

As an example of this optimization, consider the typical gain-control circuit using the LT1228 shown in Figure B1. The input is NTSC composite video, which can cover a 10dB range from 0.56V to 1.8V. The output is to be $1V_{P-P}$ into 75Ω. Amplitudes were measured from peak negative chroma to peak positive chroma on an NTSC modulated ramp test signal. See "Differential Gain and Phase" box.

Notice that the signal is attenuated 20:1 by the 75Ω attenuator at the input of the LT1228, so the voltage on the input (pin 3) ranges from 0.028V to 0.090V. This is done to limit distortion in the transconductance stage. The gain of this circuit is controlled by the current into the I_{SET} terminal, pin 5 of the IC. In a closed-loop AGC system, the loop-control circuitry generates this current by comparing the output of a detector[2] to a reference voltage, integrating the difference and then converting to a suitable current. The measured performance for this circuit is presented in tables B1 and B2. Table B1 has the uncorrected data and Table B2 shows the results of the correction.

All video measurements were taken with a Tektronix 1780R video-measurement set, using test signals generated by a Tektronix TSG 120. The standard criteria for characterizing NTSC video color distortion are the differential gain and the differential phase. For a brief explanation of these tests see the box "Differential Gain and Phase." For this design exercise the distortion limits were set at a somewhat arbitrary 3% for differential gain and 3° for differential phase. Depending on conditions, this should be barely visible on a video monitor.

[2] One way to do this is to sample the colorburst amplitude with a sample-and-hold and peak detector. The nominal peak-to-peak amplitude of the colorburst for NTSC is 40% of the peak luminance.

Table B1. Measured Performance Data (Uncorrected)

INPUT (V)	I_{SET}(mA)	DIFFERENTIAL GAIN	DIFFERENTIAL PHASE	S/N
0.03	1.93	0.5%	2.7°	55dB
0.06	0.90	1.2%	1.2°	56dB
0.09	0.584	10.8%	3.0°	57dB

Table B2. Measured Performance Data (Corrected)

INPUT (V)	BIAS VOLTAGE	I_{SET}(mA)	DIFFERENTIAL GAIN	DIFFERENTIAL PHASE	S/N
0.03	0.03	1.935	0.9%	1.45°	55dB
0.06	0.03	0.889	1.0%	2.25°	56dB
0.09	0.03	0.584	1.4%	2.85°	57dB

Figures B2 and B3 plot the measured differential gain and phase, respectively, against the input signal level (the curves labeled "A" show the uncorrected data from Table B1). The plots show that increasing the input signal level beyond 0.06V results in a rapid increase in the gain distortion, but comparatively little change in the phase distortion. Further attenuating the input signal (and consequently increasing the set current) would improve the differential gain performance but degrade the S/N. What this circuit needs is a good tweak!

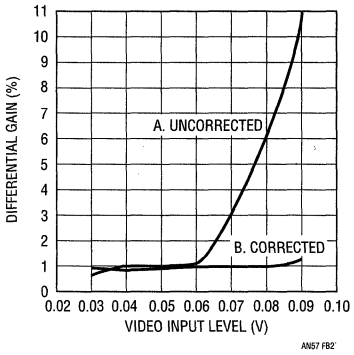


Figure B2. Differential Gain vs Input Level

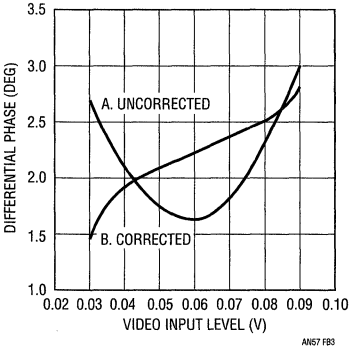


Figure B3. Differential Phase vs Input Level

Optimizing for Differential Gain

Referring to the small signal transconductance versus DC input voltage graph (Figure B4), observe that the transconductance of the amplifier is linear over a region centered around zero volts.[3] The 25°C g_m curve starts to become quite nonlinear above 0.050V. This explains why the differential gain (see Figure B2, curve A) degrades so quickly with signals above this level. Most RF signals do not have DC bias levels, but the composite video signal is mostly unipolar.

[3] Notice also that the linear region expands with higher temperature. Heating the chip has been suggested.

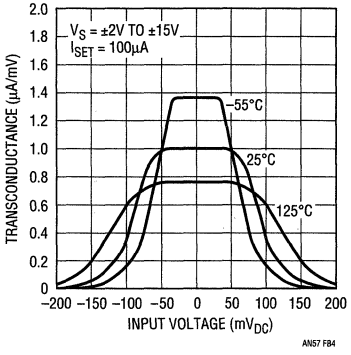


Figure B4. Small-Signal Transconductance vs DC Input Voltage

Video is usually clamped at some DC level to allow easy processing of sync information. The sync tip, the chroma reference burst, and some chroma signal information swing negative, but 80% of the signal that carries the critical color information (chroma) swings positive. Efficient use of the dynamic range of the LT1228 requires that the input signal have little or no offset. Offsetting the video signal so that the critical part of the chroma waveform is centered in the linear region of the transconductance amplifier allows a larger signal to be input before the onset of severe distortion. A simple way to do this is to bias the unused input (in this circuit the inverting input, pin 2) with a DC level.

In a video system it might be convenient to clamp the sync tip at a more negative voltage than usual. Clamping the signal prior to the gain-control stage is good practice because a stable DC reference level must be maintained.

The optimum value of the bias level on pin 2 used for this evaluation was determined experimentally to be about 0.03V. The distortion tests were repeated with this bias voltage added. The results are reported in Table B2 and Figures B2 and B3. The improvement to the differential phase is inconclusive, but the improvement in the differential gain is substantial.

Differential Gain and Phase

Differential gain and phase are sensitive indications of chroma signal distortion. The NTSC system encodes color information on a separate subcarrier at 3.579545MHz. The color subcarrier is directly summed to the black and white video signal. The black and white information is a voltage proportional to image intensity and is called luminance or luma. Each line of video has a burst of 9 to 11 cycles of the subcarrier (so timed that it is not visible) that is used as a phase reference for demodulation of the color information of that line. The color signal is relatively immune to distortions, except for those that cause a phase shift or an amplitude error to the subcarrier during the period of the video line.

Differential gain is a measure of the gain error of a linear amplifier at the frequency of the color subcarrier. This distortion is measured with a test signal called a modulated ramp (shown in Figure B5). The modulated ramp consists of the color subcarrier frequency superimposed on a linear ramp or sometimes on a stair step. The ramp has the duration of the active portion of a horizontal line of video. The amplitude of the ramp varies from zero to the maximum level of the luminance, which, in this case, is 0.714V. The gain error corresponds to compression or expansion by the amplifier (sometimes called "incremental gain") and is expressed as a percentage of the full amplitude range. An appreciable amount of differential gain will cause the luminance to modulate the chroma causing visual chroma distortion. The effect of differential gain errors is to change the saturation of the color being displayed. Saturation is the relative degree of dilution of a pure color with white. A 100% saturated color has 0% white, a 75% saturated color has 25% white, and so on. Pure red is 100% saturated whereas, pink is red with some percentage of white and is therefore less than 100% saturated.

Differential phase is a measure of the phase shift in a linear amplifier at the color subcarrier frequency when the modulated ramp signal is used as an input.

The phase shift is measured relative to the colorburst on the test waveform and is expressed in degrees. The visual effect of the distortion is a change in hue. Hue is

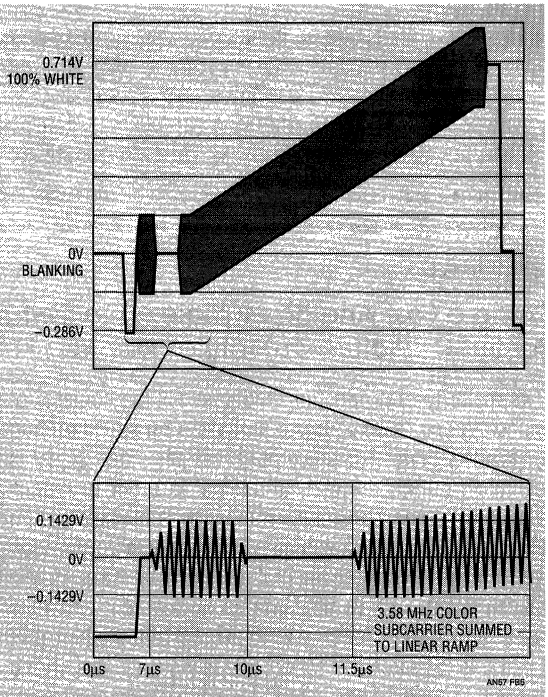


Figure B5. NTSC Test Signal

the quality of perception which differentiates the frequency of the color, red from green, yellow-green from yellow, and so forth.

Three degrees of differential phase is about the lower limit that can unambiguously be detected by observers. This level of differential phase is just detectable on a video monitor as a shift in hue, mostly in the yellow-green region. Saturation errors are somewhat harder to see at these levels of distortion—3% of differential gain is very difficult to detect on a monitor. The test is performed by switching between a reference signal, SMPTE (Society of Motion Picture and Television Engineers) 75% color bars, and a distorted version of the same signal with matched signal levels. An observer is then asked to note any difference.

In professional video systems (studios, for instance) cascades of processing and gain blocks can reach hundreds of units. In order to maintain a quality video

signal, the distortion contribution of each processing block must be a small fraction of the total allowed distortion budget[4] because the errors are cumulative. For this reason, high-quality video amplifiers will have distortion specifications as low as a few thousandths of a degree for differential phase and a few thousandths of a percent for differential gain.

[4] From the preceding discussion, the limits on visibility are about 3° differential phase, 3% differential gain. Please note that these are not hard and fast limits. Tests of perception can be very subjective.

APPENDIX C

Using a Fast Analog Multiplexer to Switch Video Signals for NTSC "Picture-in-Picture" Displays

The majority of production[1] video switching consists of selecting one video source out of many for signal routing or scene editing. For these purposes the video signal is switched during the vertical interval in order to reduce visual switching transients. The image is blanked during this time, so if the horizontal and vertical synchronization and subcarrier lock are maintained, there will be no visible artifacts. Although vertical-interval switching is adequate for most routing functions, there are times when it is desirable to switch two synchronous video signals during the active (visible) portion of the line to obtain picture-in-picture, key, or overlay effects. Picture-in-picture or active video switching requires signal-to-signal transitions that are both clean and fast. A clean transition should have a minimum of pre-shoot, overshoot, ringing, or other aberrations commonly lumped under the term "glitching."

Using the LT1204

A quality, high speed multiplexer amplifier can be used with good results for active video switching. The important specifications for this application are a small, controlled switching glitch, good switching speed, low distortion, good dynamic range, wide bandwidth, low path loss, low channel-to-channel crosstalk, and good channel-to-channel offset matching. The LT1204 specifications match these requirements quite well, especially in the areas of bandwidth, distortion, and channel-to-channel crosstalk which is an outstanding –90dB at 10MHz. The LT1204 was evaluated for use in active video switching with the test setup shown in Figure C1. Figure C2 shows the video waveform of a switch between a 50% white level and a 0% white level about 30% into the active interval and back again at about 60% of the active interval. The switch artifact is brief and well controlled. Figure C3 is an expanded view of the same waveform. When viewed on a monitor, the switch artifact is just visible as a very fine line. The lower trace is a switch between two black level (0V) video signals showing a very slight channel-to-channel offset, which is not visible on the monitor. Switching between two DC levels is a worst-case test as almost any active video will have enough variation to totally obscure this small switch artifact.

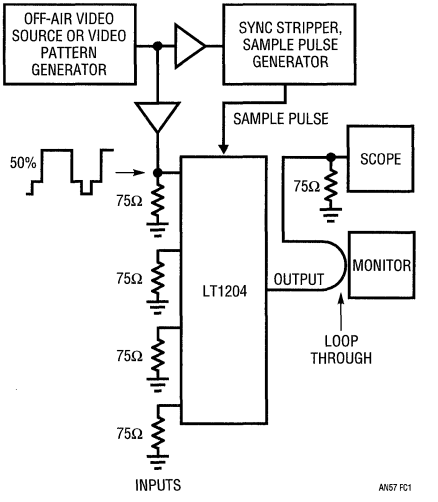
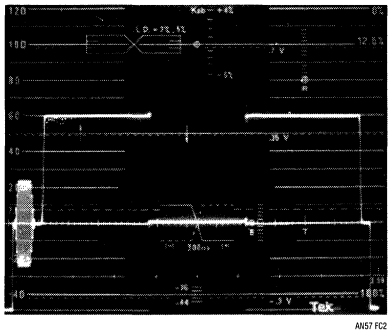


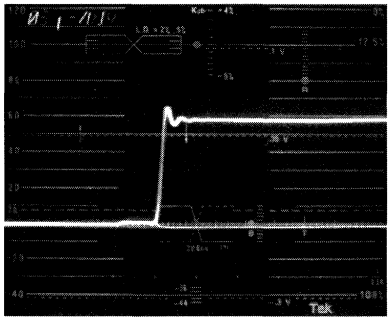
Figure C1. "Picture-in-Picture" Test Setup

[1] Video production, in the most general sense, means any purposeful manipulation of the video signal, whether in a television studio or on a desktop PC.



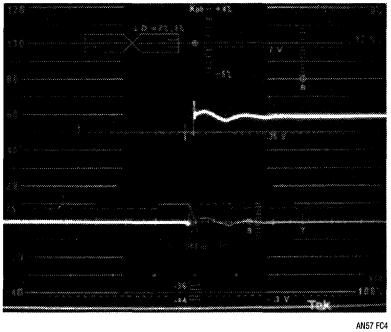
AN57 FC2

Figure C2. Video Waveform Switched from 50% White Level to 0% White Level and Back



AN57 FC3

Figure C3. Expanded View of Rising Edge of LT1204 Switching from 0% to 50% (50ns Horizontal Division)



AN57 FC4

Figure C4. Expanded View of "Brand-X" Switch 0% to 50% Transistion

Video-Switching Caveats

In a video processing system that has a large bandwidth compared to the bandwidth of the video signal, a fast transition from one video level to another with a low-amplitude glitch will cause minimal visual disturbance. This situation is analogous to the proper use of an analog oscilloscope. In order to make accurate measurement of pulse waveforms, the instrument must have much more bandwidth than the signal in question (usually five times the highest frequency). Not only should the glitch be small, it should be otherwise well controlled. A switching glitch that has a long settling "tail" can be more troublesome (that is, more visible) than one that has more amplitude but decays quickly. The LT1204 has a switching glitch that is not only low in amplitude but well controlled and quickly damped. Refer to Figure C4 which shows a video multiplexer that has a long, slow-settling tail. This sort of distortion is highly visible on a video monitor.

Composite video systems, such as NTSC, are inherently band-limited and thus edge-rate limited. In a sharply band-limited system, the introduction of signals that contain significant energy higher in frequency than the filter cutoff will cause distortion of transient waveforms (see Figure C5). Filters used to control the bandwidth of these video systems should be group-delay equalized to minimize this pulse distortion. Additionally, in a band-limited system, the edge rates of switching glitches or level-to-level transitions should be controlled to prevent ringing and other pulse aberrations that could be visible. In practice, this is usually accomplished with pulse-shaping networks. Bessel filters are one example. Pulse-shaping networks and delay-equalized filters add cost and complexity to video systems and are usually found only on expensive equipment. Where cost is a determining factor in system design, the exceptionally low amplitude and brief duration of the LT1204's switching artifact make it an excellent choice for active video switching.

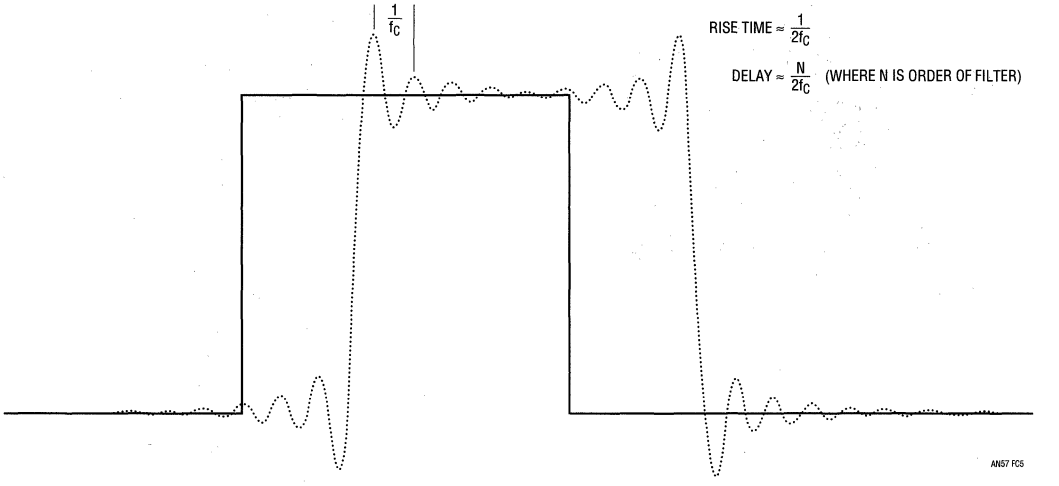


Figure C5. Pulse Response of an Ideal Sharp-Cutoff Filter at Frequency f_C

Conclusion

Active video switching can be accomplished inexpensively and with excellent results when care is taken with both the selection and application of the high speed multiplexer. Both fast switching and small, well-controlled switching glitches are important. When the LT1204 is used for active video switching between two flat-field video signals (a very critical test) the switching artifacts are nearly invisible. When the LT1204 is used to switch between two live video signals, the switching artifacts are invisible.

Some Definitions—

"Picture-in-picture" refers to the production effect in which one video image is inserted within the boundaries of another. The process may be as simple as splitting the screen down the middle or it may involve switching the two images along a complicated geometric boundary. In order to make the composite picture stable and viewable, both video signals must be in horizontal and vertical sync. For composite color signals, the signals must also be in subcarrier lock.

"**Keying**" is the process of switching among two or more video signals triggering on some characteristic of one of the signals. For instance, a chroma keyer will switch on the presence of a particular color. Chroma keyers are used to insert a portion of one scene into another. In a commonly used effect, the TV weather person (the "talent") appears to be standing in front of a computer generated weather map. Actually, the talent is standing in front of a specially colored background; the weather map is a separate video signal, which has been carefully prepared to contain none of that particular color. When the chroma keyer senses the keying color, it switches to the weather map background. Where there is no keying color, the keyer switches to the talent's image.

5V to 3.3V Converters for Microprocessor Systems

Robert Dobkin, Mitchell Lee, Dennis O'Neill and Milt Wilcox

Introduction

The new generation of high performance microprocessors are built on dense, low breakdown voltage processes in order to accommodate increased transistor counts. These new processors require high current power at 3.3V, developed from the 5V input used to power the rest of the system. Special techniques are required to ensure proper operation of the microprocessor and good heat dissipation within the computer system.

The 3.3V supply may be either a linear or switching type. For most applications a linear regulator is preferable since it minimizes components and has acceptable efficiency for a whole computer system. In portable computers where high efficiency is paramount because of battery operation, a switching supply is necessary.

This application note contains a collection of 3.3V regulator circuits, each optimized for a 5V input and surface mount technology. The circuits are split into two categories, linear and switching, and further arranged by current capability.

Most of the circuits, with the possible exception of the high current linear regulators, are surface mountable. Where appropriate, part numbers are given for surface mount coils, capacitors, and diodes. Resistors and small capacitors, unless there are special characteristics, are generic and manufacturer's part numbers are not shown.

Both linear and switching regulators are available for the purpose of converting 5V to 3.3V. In general, the linear regulators are the best choice at lower (≤3A) current levels where their dissipation is minimized, or in line-operated equipment where 66% theoretical efficiency is acceptable. Switchers are favored in higher current and efficiency-conscious applications. Efficiencies in the 90% to 95% range are the norm for switchers described in this application note.

Linear Regulators

Table 1 shows the range of components available for linear regulation of 3.3V with a 5V input. With only 1.7V of headroom, low dropout is essential. Low dropout regulators are available delivering currents from 125mA to 7.5A, allowing almost any microprocessor to be powered with a local 3.3V generation circuit. The first four devices (LT1020, LT1120, LT1121 and LT1129) are PNP micropower low dropout regulators. Since PNP transistors are much larger than monolithic NPNs, higher current regulators use an NPN pass device. The LT1117, LT1086, LT1083 through LT1085, and LT1087 all use NPN pass devices. The NPN structure requires about 1.2V headroom compared to the 400mV to 500mV dropout typical of PNP regulators, and ground current of 5mA or 10mA, independent of output current. Because of this constant quiescent current, the LT1117 and LT1083 family are not suitable for applications requiring micropower standby.

Table 1. 3.3V Linear Regulators

LOAD CURRENT	DEVICE	PASS DEVICE	SHUTDOWN CURRENT	TOLERANCE*
125mA	LT1020	PNP	40μA	2.1% (69mV)
125mA	LT1120	PNP	40μA	2.1% (69mV)
150mA	LT1121-3.3	PNP	16μA	3% (100mV)
700mA	LT1129-3.3	PNP	16μA	3% (100mV)
800mA	LT1117-3.3	NPN	–	2% (65mV)
1.5A	LT1086-3.3	NPN	–	1.6% (53mV)
3A	LT1085-3.3	NPN	–	1.6% (53mV)
5A	LT1084	NPN	–	1.9% (61mV)
7.5A	LT1083	NPN	–	1.9% (61mV)
10A	2 × LT1087	NPN	–	1.9% (61mV)

*Includes line, load, and temperature variations. Adjustable parts also include worst case effect of external 1% resistors.

Controlling Transient Loads

Microprocessors require the input voltage to be maintained within ±5% under worst case transients. The dynamic nodes internal to the processor are sensitive to voltage. Transients drawn by the processor are so fast that no active loop can respond in time. Adequate reserves of charge must be maintained in a group of capacitors to supply this current until the regulator can respond. This is true for both linear and switching regulators.

Modern power saving processors may draw large transient currents unlike older processors. Many include sleep modes which slow down or stop the processor when it is not in use. The transition from normal operation to sleep mode, or sleep mode to normal operation usually causes a large step in power supply current. The supply current can jump several amps in a matter of nanoseconds—far faster than any regulator can respond. Proper printed circuit layout and bypass capacitors are needed to provide these current transients.

Typical printed circuit board layouts include a power plane and a ground plane which are separate from the rest of the system. Connected to the pins of the processor are small 100nF bypass capacitors, as is common practice in processor layout. These capacitors control the voltage for very fast transients in the 10ns to 100ns time period. Further from the processor is a large reservoir capacitor located at the output of the regulator. This capacitor is typically 100µF to 200µF and provides the energy reservoir for 100ns to 2µs until the control loop in the regulator can correct the output. For longer durations, the control loop in the regulator keeps the output voltage constant.

When the load is released the overshoot must be controlled as well, and the capacitors absorb the energy and limit overshoot from the regulator. The capacitors must be low inductance and connected directly to the power plane close to the processor. Several inches of trace going to a capacitor can be sufficient to cause large transient voltages under changing load conditions because of the inductance in the circuit traces. The power cycling associated with the new processors makes this situation far worse than older processors which operated continuously.

An input bypass capacitor is placed close to the regulator to provide a low source impedance. The input to the regulator must also provide an energy reservoir. Typically, here again, is a 10µF to 100µF capacitor that provides the energy at the input of the regulator during a load transient. This capacitor is mandatory since the regulator is usually situated far from the input power supply.

Both the input and output capacitors play a role in the stability of the regulator and help assure adequate transient response. The capacitor values shown in this app note represent the minimum required for stability. Additional capacitance may be necessary to handle load transients. See the design example.

Thermal Design

Heat sinking is an important consideration. For processors drawing 5A, the power dissipated in the regulator can be as high as 8.5W. This amount of power requires adequate heat sinking internal to the computer system.

The general rule for surface mounted components is to maximize the amount of copper connected to the leads of the IC. Flood all open areas, intermediate layers, and the back side of the board with copper. This aids in spreading and radiating the heat. Surface mount components can dissipate up to 2.5W (1.5A output current) using only circuit traces and ground planes totaling 2 or 3 square inches.

For higher output currents a larger heat sink is needed. To compute the thermal resistance of the heat sink it is necessary to know the maximum operating temperature of the regulator, maximum ambient inside the computer enclosure and the air flow over the heat sink. For a power dissipation of 5W (3A output current), maximum junction temperature of 125°C and maximum ambient temperature of 80°C:

$$\theta_{HS} = (T_J - T_A)/P_D - \theta_{JC}$$

$$\theta_{HS} = (125 - 80)/5 - 3$$

$$\theta_{HS} = 6°C/W$$

where:

P_D = Power Dissipation (°C)

T_J = Maximum Junction Temperature (°C)

T_A = Maximum Ambient Temperature (°C)

θ_{JC} = Junction to Case Thermal Resistance of IC (°C/W)

θ_{HS} = Heat Sink Thermal Resistance (°C/W)

The heat sink for this application must have a thermal resistance of 6°C/W or less. Figure 1 shows the effect of air flow over the surface of a 6°C/W heat sink (Thermalloy 7025B-MT). With no air flow the thermal resistance is dominated by convection currents; this is why the graph stops at approximately 100 feet per minute air flow. A much smaller heat sink could be used in this application if some air flow, such as from the computer's cooling fan, could be guaranteed. At higher output currents and dissipations it is almost always necessary to provide some air flow in order to avoid an unreasonably large heat sink.

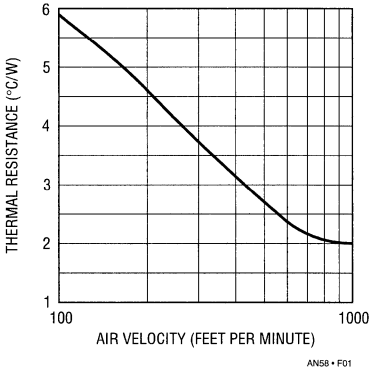


Figure 1. Thermal Resistance vs Air Flow

Selectable 5V and 3.3V

Figure 2 shows a regulator configuration which is pin selectable for 3.3V or 5V output. An external N-channel power MOSFET bypasses the regulator to provide 5V output. When the gate of the MOSFET is grounded by a pin on the microprocessor, the MOSFET turns off and the regulator supplies a 3.3V output. For this type of circuit to operate properly, the regulator must be designed to withstand 5V forced on its output pin without damage. All

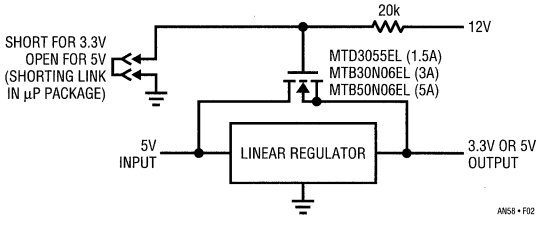


Figure 2. 3.3V Regulator with 5V Bypass Circuit

Linear Technology regulators in the LT1083/4/5/6, LT1117 and LT1121/9 families are designed to withstand over 5V with no problems.

The MOSFET has an on resistance of approximately 30mΩ when the gate is driven to 12V. There is a 12V power supply available in most systems and a high value resistor can be used to tie the gate of the MOSFET high. If 12V is not available, an LTC1157 high-side driver (Figure 3) can be used to drive the gate of the MOSFET.

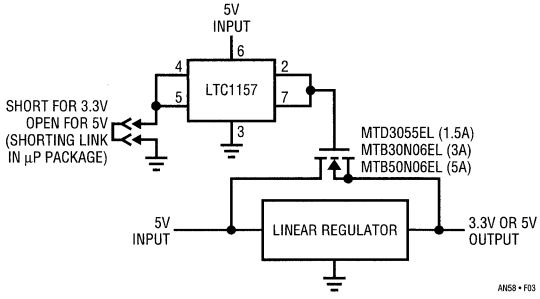


Figure 3. LT1157 Switches Between 5V and 3.3V

Switching Regulators

Properly designed step-down, or buck, switching regulators can provide 5V to 3.3V conversion efficiencies as high as 95%. In a step-down switching regulator, the inductor current flows from the input when the switch is ON and through a diode (or synchronously switching FET) from ground when the switch is OFF. Keys to high efficiency include minimizing quiescent current, using a low resistance power MOSFET switch and in higher current applications, using a synchronous switch to reduce the diode losses. In continuous operation (i.e., the inductor current does not go to zero), the duty cycle for a 5V to 3.3V switching regulator is 66%. This means that the switch is ON for 2/3 of each cycle and OFF for the remaining 1/3.

Table 2 shows four switching regulators suitable for 5V to 3.3V conversion. All of these regulators break the 90% efficiency barrier over a wide range of load currents. High efficiency makes for a compact layout and allows all surface mount solutions at high current since heat sinking is either modest or unnecessary.

Table 2. 3.3V Switching Regulators

LOAD CURRENT	DEVICE	SYNCHRONOUS	SHUTDOWN CURRENT	EFFICIENCY
200mA to 400mA	LTC1174-3.3	No	1µA	90%
0.5mA to 2A	LTC1147-3.3	Yes	10µA	92%
1A to 5A	LTC1148-3.3	Yes	10µA	94%
5A to 20A	LT1158	Yes	2.2mA	91%

The LTC1174, LTC1147 and LTC1148 step-down, high efficiency switching regulators feature Burst Mode™ operation to maintain low quiescent current at light loads (sleep mode) and in the LTC1148, synchronous operation at higher output currents. The LTC1147 and LTC1148 use a constant off-time, current-mode architecture. This results in excellent line and load transient response, constant inductor ripple current and well controlled startup and short-circuit currents.

The LTC1174 and LTC1147 are nonsynchronous converters for applications under 1A. The LTC1148 is fully synchronous for improved efficiency in the 2A to 5A output range. In Figure 17 an LTC1147 is used for 1A output current. This circuit consumes less board space than the LTC1148 circuit of Figure 18, at the cost of 2.5% worse efficiency. The LT1158 is a half-bridge driver designed for 5V to 20A applications. At these current levels multiple paralleled MOSFETs are necessary to maintain high efficiency. The LT1158 is used in Figures 21 and 22.

The compactness of a switching regulator solution is appealing, but not all of the required components shrink as easily as semiconductors and resistors. In particular, coils and high value capacitors present special miniaturization problems. Coil size is limited by practical considerations of core volume, temperature rise, and window area. Very high power densities have been achieved through the use of ferrite cores and materials such as molypermalloy. Unfortunately, the selection of surface mount bobbins for "E" style split cores has lagged behind. This area is the focus of development work but product introductions are slow in coming. A list of surface mount component suppliers can be found in Appendix A of Application Note 54.

Burst Mode™ is a trademark of Linear Technology Corporation

Power Supply Sequencing and Rise Time

New 3.3V microprocessors must interface with 5V logic circuits. As a precaution against damaging logic interfaces, supply turn-on characteristics must be controlled. For example, one specification calls for a maximum difference between the system (5V) supply and the microprocessor (3.3V) supplies of 2.25V. Not all of the circuits shown will meet this specification or have been characterized for input/output differential.

The linear regulators in the LT1083 thru LT1086 family will maintain proper startup and shutdown voltages for mixed supply systems. On turn-on, the output follows the input less the 1.2V dropout voltage until 3.3V is reached on the output. At turn-off, an internal diode insures the 3.3V supply follows the 5V supply down.

Recommended Circuit Design Example

Figure 4 shows a recommended circuit for general purpose 5V to 3.3V conversion in desktop machines. Since the microprocessor draws only a fraction of the total system power, the 66% efficiency of a linear regulator gives acceptable performance. The system requirements are:

V_{IN} = 5V ±0.25V

V_{OUT} = 3.3V ±0.3V

I_{OUT} = 3A

Transients Loads: 200mA to 3A in 100ns and 3A to 100mA in 100ns

Maximum Circuit Height: 1.5"

Bypass Option: 5V out through low resistance switch if 3.3V processor is not installed.

The LT1085 fullfills these requirements with the output bypassing capacitors shown in Figure 4. The 5V bypass switch, detailed in Figures 2 and 3 can be added as an option. A pin on the 3.3V microprocessor serves as the ground shorting switch to disable the bypass circuit.

Thermal design, as previously discussed, would require a 6°C/W heat sink. The Thermalloy 7025B-MT or Aavid 533402 meet this requirement as well as the 1.5" maximum height requirement.

Regulation, including all combinations of line, load, and temperature, is better than 1.6% (53mV) for the LT1085—well inside the 300mV specification. Figure 5 shows the transient response to a 3A load change. The transient response should be checked in the finished circuit to verify the layout and capacitor placement.

Figure 6 shows the output voltage tracking as the system is powered up and down. Note that the 5V supply never out runs the 3.3V supply by more than approximately 1.2V, thereby protecting the processor from damage.

Ground current for the LT1085 is just 5mA, even at 3A output current.

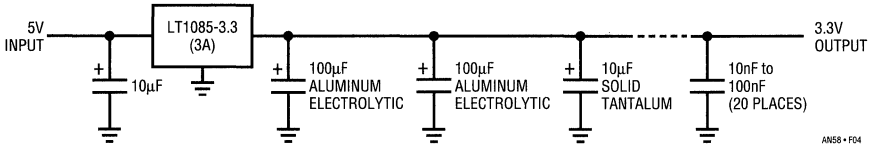


Figure 4. Multiple Bypassing is Necessary in Order to Assure Good Transient Response

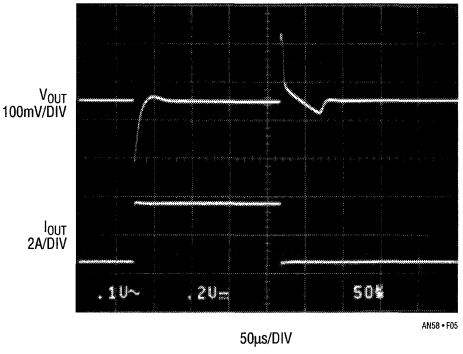
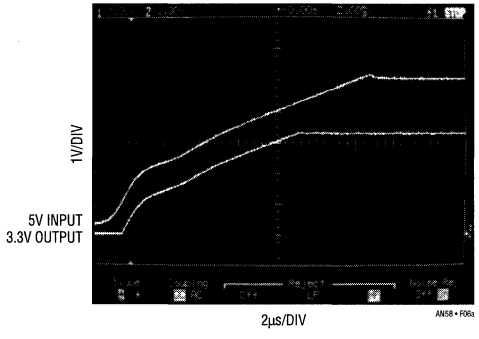
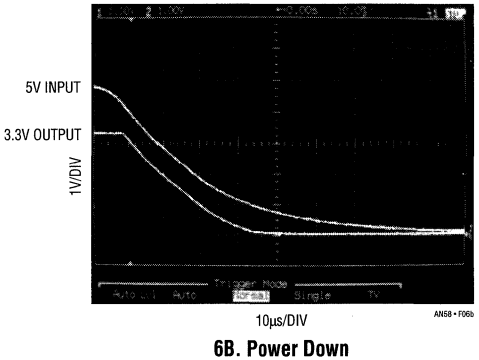


Figure 5. Regulator Transient Response



6A. Power Up



6B. Power Down

Figure 6. 5V/3.3V Tracking at Power Up and Power Down

CIRCUIT INDEX

Linear Regulators

Switching Regulators

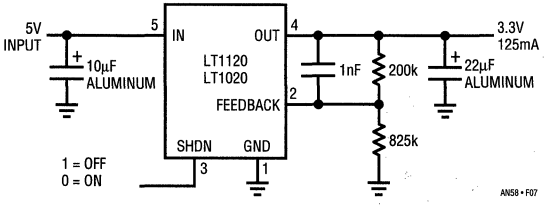


Figure 7. The LT1120 and LT1020 Include On-Chip Comparator Functions. See Their Data Sheets for Details

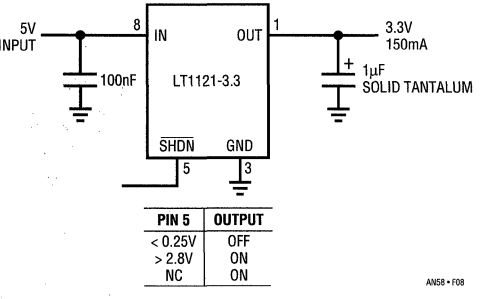


Figure 8. The Output of the LT1121 Can Be Pulled Up to 5V with No III Effects

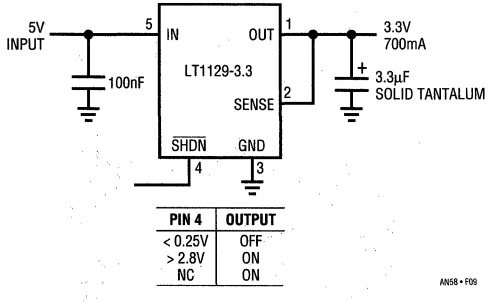


Figure 9. The Output of the LT1129 Can Be Pulled Up to 5V with No III Effects

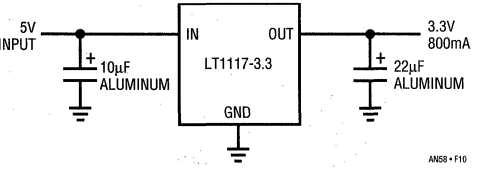


Figure 10. The LT1117 is Available in a Low Cost, SOT-223 Package

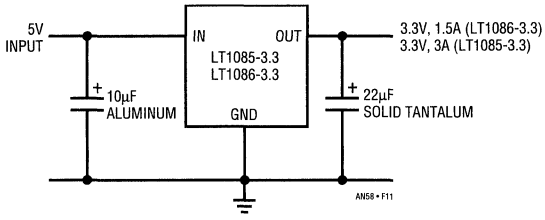


Figure 11. See Figure 4 in the Design Example for Practical Bypassing Values

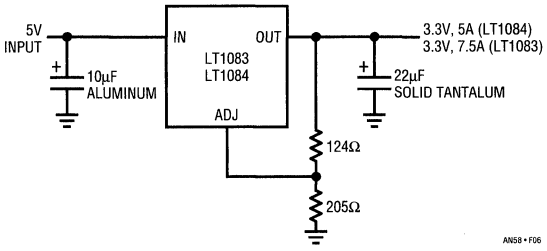
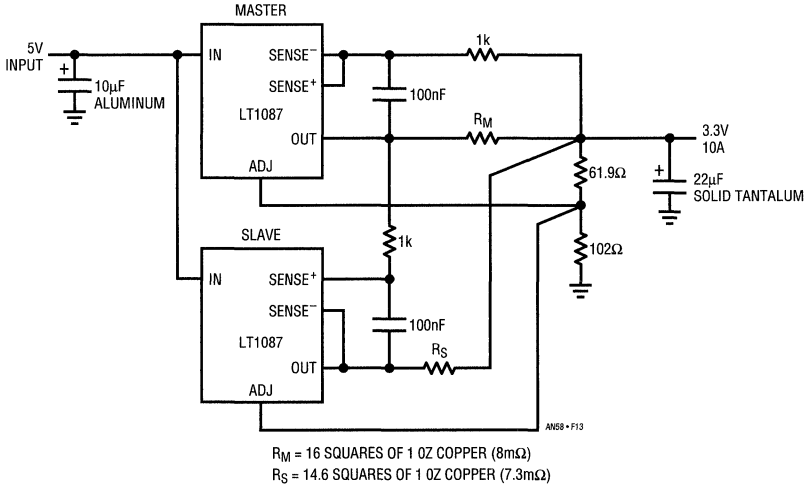
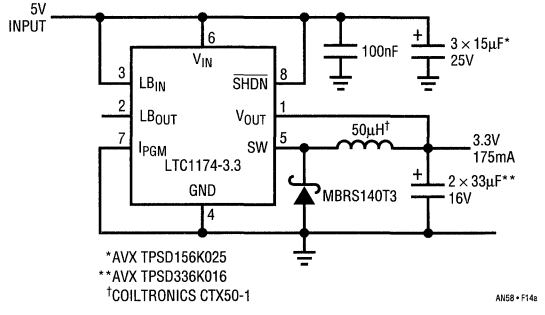


Figure 12. Five Components Deliver Up to 7.5A

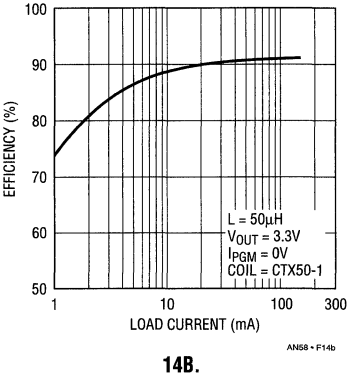


R_M = 16 SQUARES OF 1 0Z COPPER (8mΩ)
R_S = 14.6 SQUARES OF 1 0Z COPPER (7.3mΩ)

Figure 13. Independently, LT1087s Handle 5A. Their Reference Sense Pins Force Current Sharing for Parallel Operation at 10A

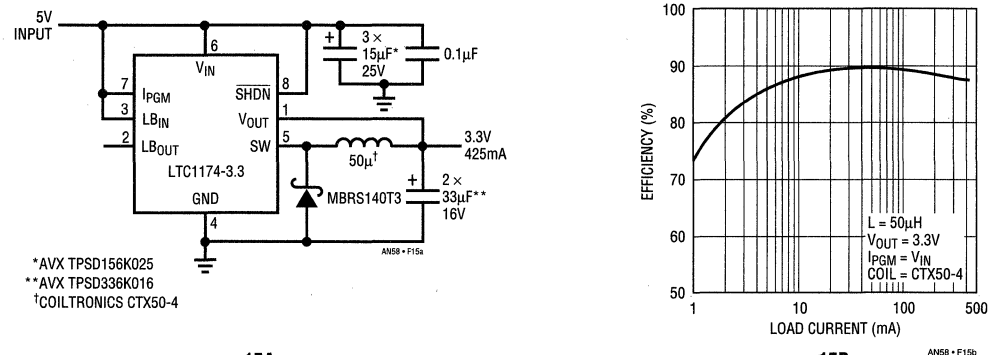


14A.



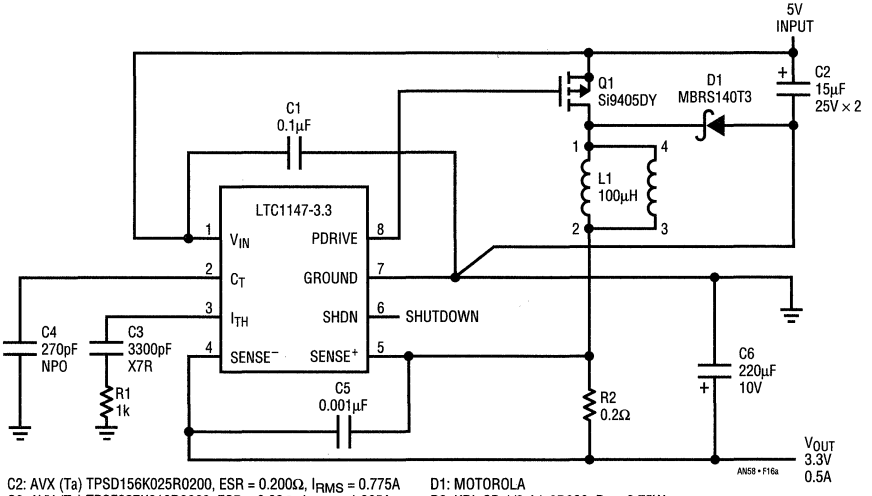
14B.

Figure 14. The LTC1174-3.3 Uses Burst Mode™ Operation Throughout its Entire Current Range. Shutdown Current is Just 1µA



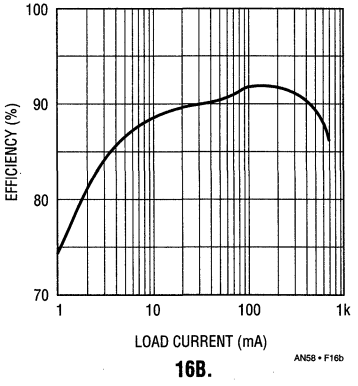
15A. **15B.**

Figure 15. Pulling I_{PGM} (Pin 7) High Increases the Internal Current Threshold and Output Current Capability



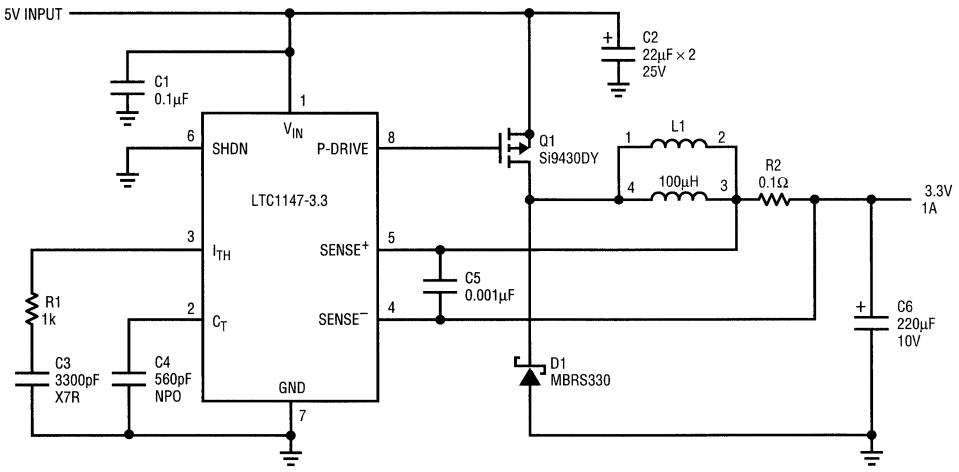
C2: AVX (Ta) TPSD156K025R0200, ESR = 0.200Ω, I_{RMS} = 0.775A
C6: AVX (Ta) TPSE227K010R0080, ESR = 0.80Ω, I_{RMS} = 1.285A
Q1: SILICONIX BV_{DSS} = 20V, DCR_{ON} = 0.14Ω, Q_g = 29nC
D1: MOTOROLA
R2: KRL SP-1/2-A1-0R200, P_D = 0.75W
L1: COILTRONICS CTX100-4, DCR = 0.175Ω, Kool Mµ® Core

16A.



16B.

Figure 16. Slightly Improved Efficiency Over the Circuit of Figure 15, with Continuous Mode Operation at Higher Loads



C2: AVX (Ta) TPSD226K025R0200 ESR = 0.200Ω I_{RMS} = 0.775A
C6: AVX (Ta) TPSE227K010R0080 ESR = 0.080Ω I_{RMS} = 1.285A
Q1: SILICONIX BV_{DSS} = 20V DCR_{ON} = 0.100Ω C_{RSS} = 400pF Q_g = 50nC
D1: MOTOROLA
R2: KRL SP-1/2-A1-0R100 Pd = 0.75W
L1: COILTRONICS CTX100-4 DCR = 0.175Ω KOOL Mµ® CORE

QUIESCENT CURRENT = 170µA
TRANSITION CURRENT (BURST MODE™ OPERATION/CONTINUOUS OPERATION) = 170mA

AN58 F17a

Figure 17A. LTC1147 (5V to 3.3V/1A) Buck Converter with Surface Mount Technology. Shutdown Current is Just 10µA

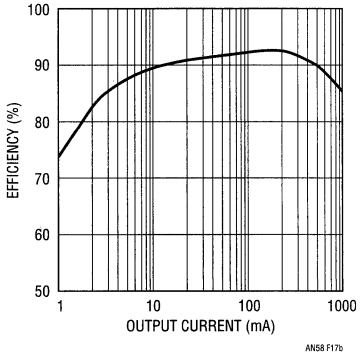
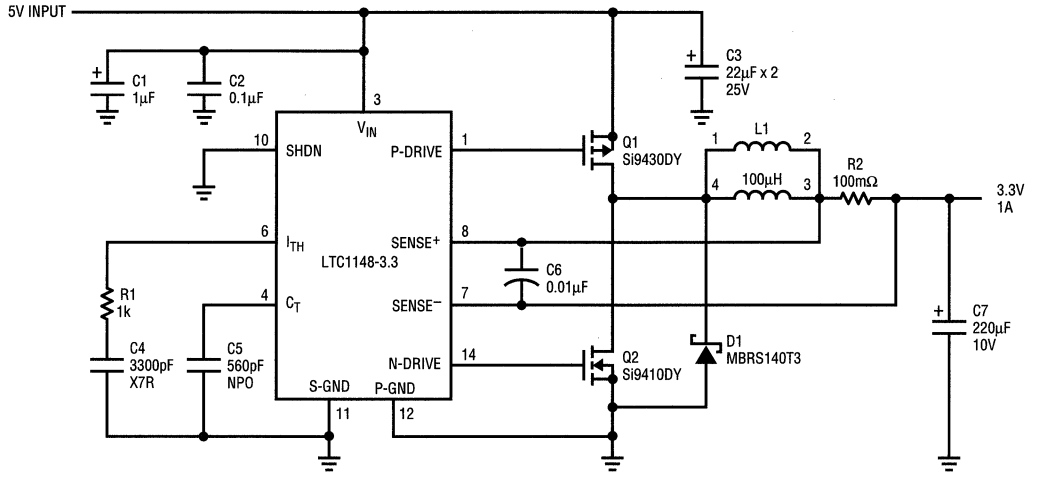


Figure 17B. LTC1147 (5V to 3.3V/1A) Buck Converter Measured Efficiency



C1: (Ta)
C3: AVX (Ta) TPSD226K025R0200 ESR = 0.200Ω I_{RMS} = 0.775A
C7: AVX (Ta) TPSE227K010R0080 ESR = 0.080Ω I_{RMS} = 1.285A
Q1: SILICONIX NMOS BV_{DSS} = 20V RDS_{ON} = 0.100Ω C_{RSS} = 400pF Q_g = 50nC
Q2: SILICONIX NMOS BV_{DSS} = 30V RDS_{ON} = 0.050Ω C_{RSS} = 160pF Q_g = 30nC
D1: MOTOROLA SCHOTTKY VBR = 40V
R2: KRL SP-1/2-A1-0R100J Pd = 0.75W
L1: COILTRONICS CTX100-4 DCR = 0.175Ω KOOL Mµ® CORE

QUIESCENT CURRENT = 180µA
TRANSITION CURRENT (BURST MODE™ OPERATION/CONTINUOUS OPERATION) = 250mA

ALL OTHER CAPACITORS ARE CERAMIC

AN58 F18a

Figure 18A. LTC1148 (5V to 3.3V/1A) Fully Synchronous Buck Converter

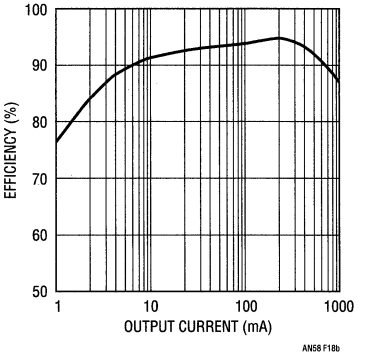
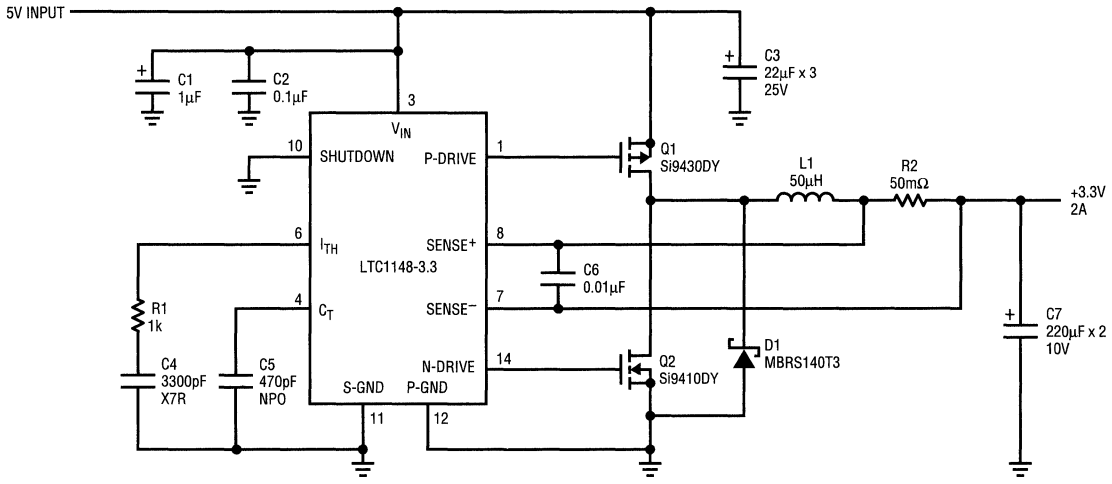


Figure 18B. LTC1148 (5V to 3.3V/1A) Buck Converter Measured Efficiency



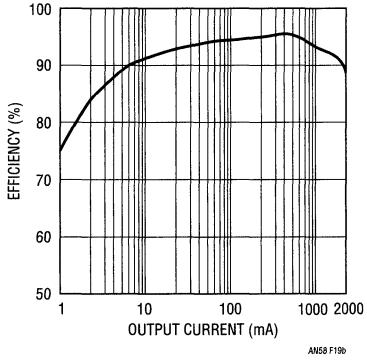
C1: (Ta)
C3: AVX (Ta) TPSD226K025R0200 ESR = 0.200Ω I_{RMS} = 0.775A
C7: AVX (Ta) TPSE227K010R0080 ESR = 0.080Ω I_{RMS} = 1.285A
Q1: SILICONIX PMOS BV_{DSS} = 20V RDS_{ON} = 0.100Ω C_{RSS} = 400pF Q_g = 50nC
Q2: SILICONIX NMOS BV_{DSS} = 30V RDS_{ON} = 0.050Ω C_{RSS} = 160pF Q_g = 30nC
D1: MOTOROLA SCHOTTKY VBR = 40V
R2: KRL SL-1-C1-0R050J Pd = 1W
L1: COILTRONICS CTX50-2-MP DCR = 0.032Ω MPP CORE (THROUGH HOLE)

QUIESCENT CURRENT = 180µA
TRANSITION CURRENT (BURST MODE™ OPERATION/CONTINUOUS OPERATION) = 450mA

ALL OTHER CAPACITORS ARE CERAMIC

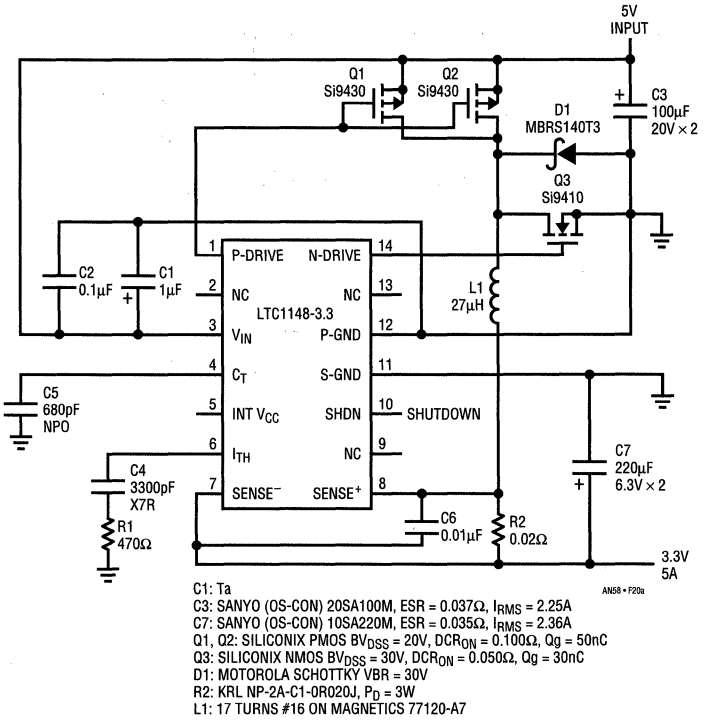
AN58 F19a

Figure 19A. LTC1148 (5V to 3.3V/2A) Buck Converter



AN58 F19b

Figure 19B. LTC1148 (5V to 3.3V/2A) Buck Converter Measured Efficiency



C1: Ta
C3: SANYO (OS-CON) 20SA100M, ESR = 0.037Ω, I_{RMS} = 2.25A
C7: SANYO (OS-CON) 10SA220M, ESR = 0.035Ω, I_{RMS} = 2.36A
Q1, Q2: SILICONIX PMOS BV_{DSS} = 20V, DCR_{ON} = 0.100Ω, Qg = 50nC
Q3: SILICONIX NMOS BV_{DSS} = 30V, DCR_{ON} = 0.050Ω, Qg = 30nC
D1: MOTOROLA SCHOTTKY VBR = 30V
R2: KRL NP-2A-C1-0R020J, P_D = 3W
L1: 17 TURNS #16 ON MAGNETICS 77120-A7

Figure 20A. LTC1148 (5V to 3.3V/5A) Buck Converter. Beyond 5A the LT1158 is a Better Choice

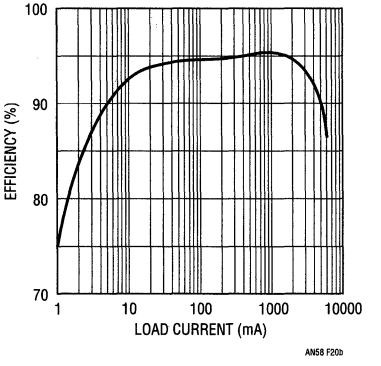


Figure 20B. LTC1148 (5V to 3.3V/5A) Buck Converter Measured Efficiency

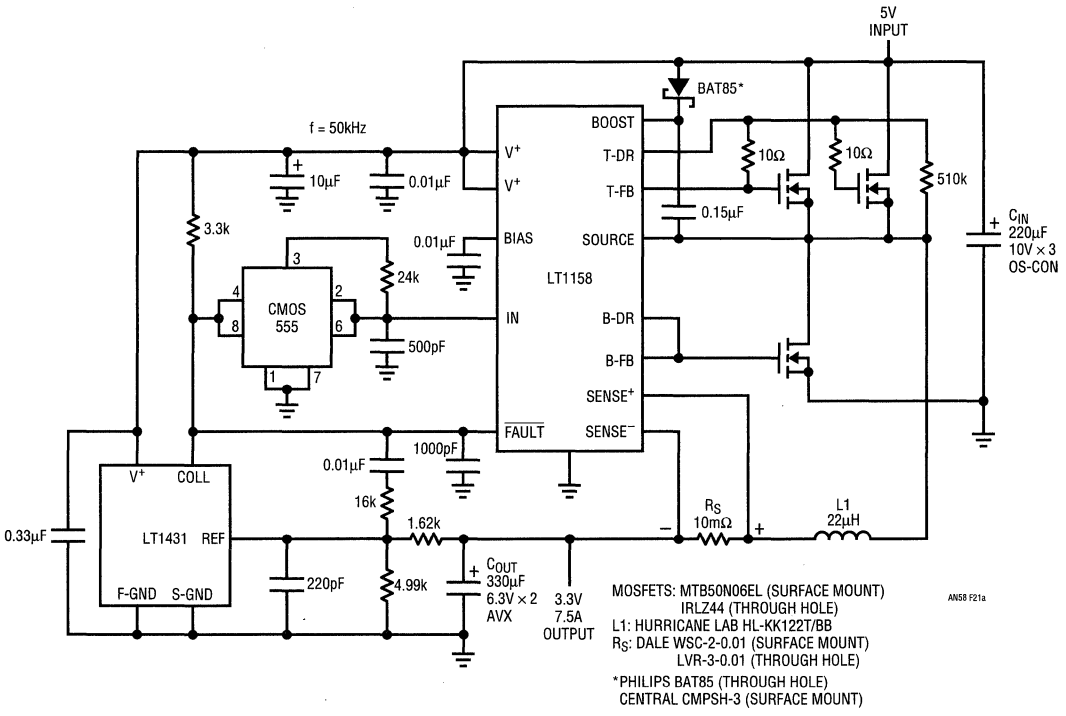


Figure 21A. High Efficiency High Current 5V to 3.3V Switching Regulator Output Current = 7.5A Cont. 10A Peak

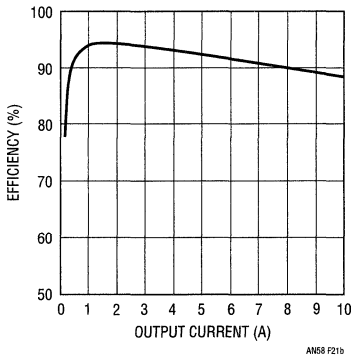


Figure 21B. High Efficiency High Current 5V to 3.3V Switching Regulator

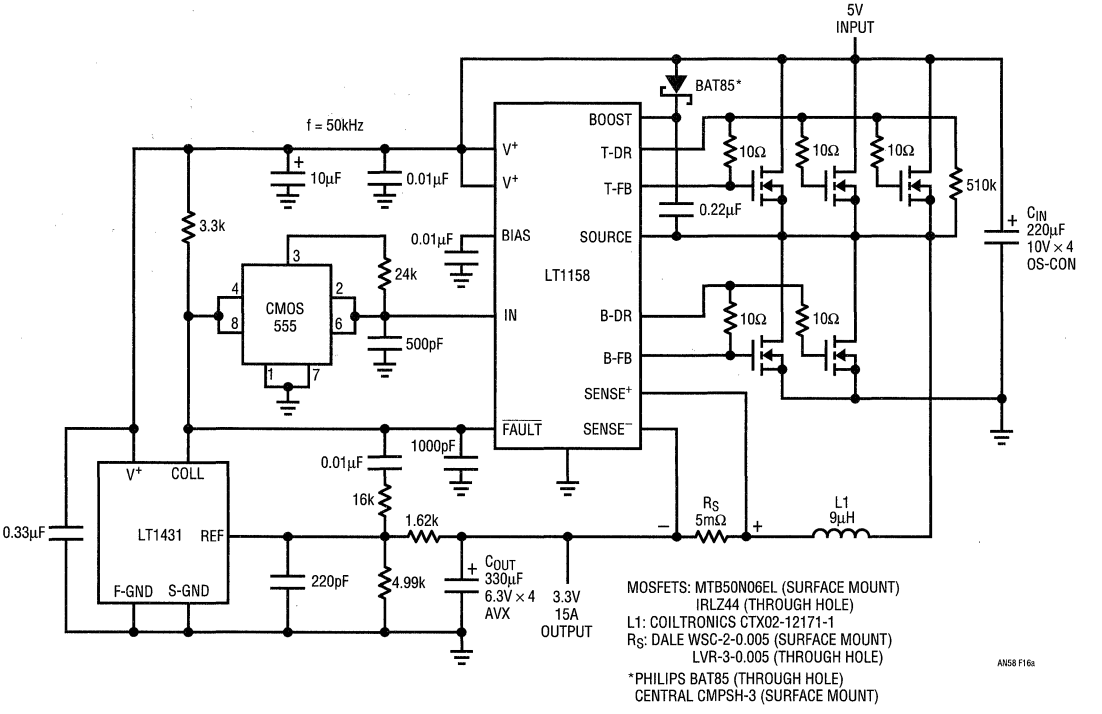


Figure 22A. High Efficiency High Current 5V to 3.3V Switching Regulator Output Current = 15A Cont. 20A Peak

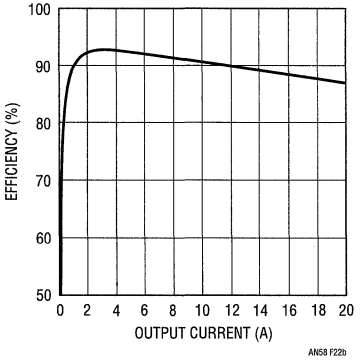


Figure 22B. High Efficiency High Current 5V to 3.3V Switching Regulator

APPENDIX

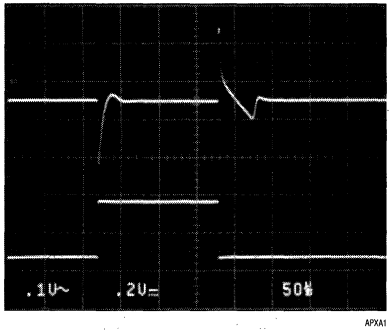
The following photographs illustrate the effect of various types and values of output capacitance on the transient response of the LT1085. The current step for these photographs is equal to the worst case supply current change specified by Intel. This current step occurs when the processor transitions from an idle state to a running state or from a running state to an idle state. The current step illustrated in the photographs is from 100mA to 3A and then from 3A back to 100mA. Both transitions occur in 100ns.

A number of different capacitor types and combinations were used. In each case the capacitors were chosen to limit the output voltage deviation to less than ±5% of 3.3V.

For all photographs:

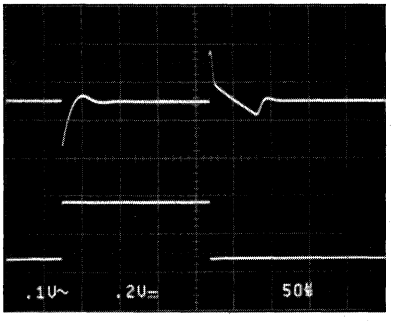
1) The top trace is the output variation and the vertical scale is equal to 100mV per division.
2) The bottom trace is the output current step at 2A per division. The horizontal scale for all photographs is 50μs per division.

C_{OUT} = 100μF/10V AVX Tantalum, Surface Mount



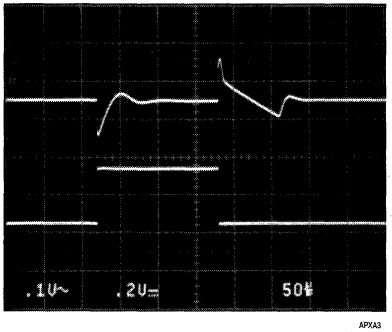
APXA1

C_{OUT} = 100μF/10V AVX Tantalum, Surface Mount in Parallel with 100μF/16V Aluminum Electrolytic



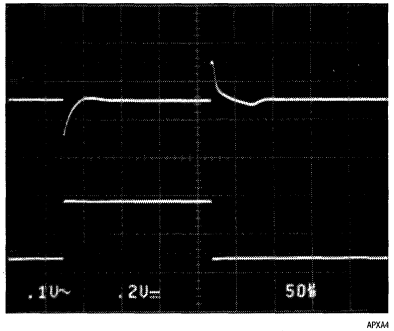
APXA2

C_{OUT} = 2-100μF/10V AVX Tantalum, Surface Mount in Parallel



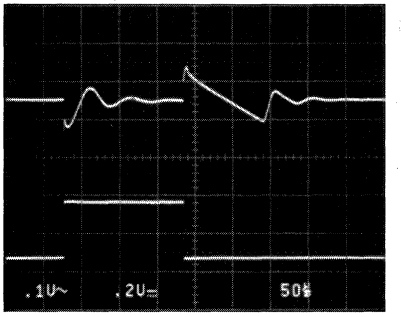
APXA3

C_{OUT} = 100μF/10V AVX Tantalum, Surface Mount in Parallel with 390μF/16V Aluminum Electrolytic



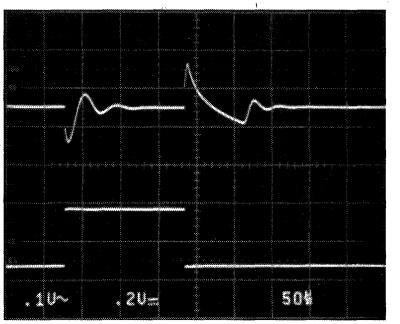
APXA4

C_{OUT} = 220µF/10V OS-CON



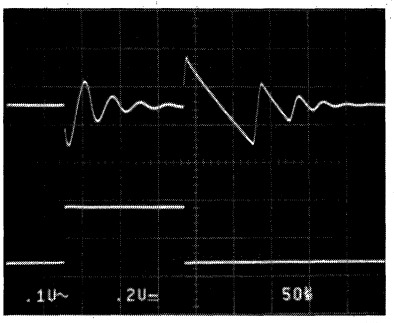
APXA5

C_{OUT} = 100µF/16V OS-CON in Parallel with 220µF/16V Aluminum Electrolytic



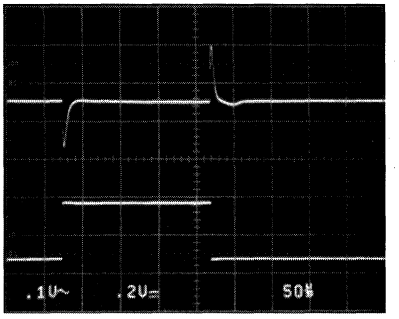
APXA6

C_{OUT} = 100µF/16V OS-CON



APXA7

C_{OUT} = 22µF/20V OS-CON in Parallel with 390µF/16V Aluminum Electrolytic



APXA8

C_{OUT} = 100µF/16V OS-CON in Parallel with 100µF/16V Aluminum Electrolytic

APXA9

Applications of the LT1300 and LT1301 Micropower DC/DC Converters

Dale Eagar and Steve Pietkiewicz

INTRODUCTION

The design of battery-powered equipment can often be quite challenging. Since few ICs can operate directly from the end-of-life voltage from a 2-cell battery (about 1.8V), most systems require a DC/DC converter. The system designer often has a limited area in which to place the DC/DC converter; associated inductors and capacitors must be small. Surface mount components are a must and heat sinks are out of the question! The LT1300 and LT1301 micropower DC/DC converter ICs provide new possibilities for more efficient, compact and cost effective designs. When designing equipment for battery-powered operation, a number of important design constraints should be considered. Some of these are detailed in the check list given here:

- Design for high efficiency. A high efficiency converter increases battery life, eliminates most heat sinks, reduces weight and decreases PC board area. The designer should strive for high efficiency at:
  - Full Load
  - Light Load
- Plan to utilize all the capacity of the battery. Can the circuit run down to the "dead cell" voltage? Is there a micropower shutdown mode?
- Can the DC/DC converter circuitry provide high output power for short time intervals? Often this is a requirement on battery-powered equipment.
- Cost. Is the complete circuit cost competitive?
- Does the design meet packaging constraints?
  - Height
  - PC Board Area
  - Weight

The LT1300 family of DC/DC converters allows a maximum of flexibility in the design of circuits which provide solutions for battery-operated and other equipment needing high efficiency, space efficient, micropower power solutions.

INDEX TO LT1300 CIRCUITS

NEW LT1300 AND LT1301 MICROPOWER DC/DC CONVERTERS

by Steve Pietkiewicz

Introduction

The new LT1300 and LT1301 micropower DC/DC converters provide improvements in both electrical and physical efficiency, two key areas of battery-based power supply design. Housed in 8-lead DIPs or SOIC packages, the devices feature a 1A on-chip switch with a V_{CESAT} of just 170mV. The internal oscillator frequency is set at 155kHz, allowing the use of tiny, 5mm diameter surface mount inductors along with standard D-case size tantalum capacitors. A complete 2-cell to 12V, 5V, or 3.3V converter can fit in less than 0.4 square inches of PC board area.

The devices use Burst Mode™ operation to maintain high efficiency across the full load range. The fully operating quiescent current is only 120µA. It can be further reduced to 10µA by taking the SHUTDOWN pin high, which also disables the device. The output voltage of the LT1300 can be set at either 5V or 3.3V via the logic-controlled SELECT pin, and the LT1301 output can be set at either 5V or 12V using the same pin. The I_{LIM} pin allows the reduction of peak switch current and allows the use of even smaller components. The switch current is nominally set at 1A and can be reduced via the I_{LIM} pin to approximately 400mA, further improving efficiency in systems requiring lower peak powers.

Burst Mode™ is a trademark of Linear Technology Corporation

Theory of Operation

Figure 1 is a block diagram of the LT1300/LT1301. Also refer to Figure 2 for associated component hookup. When A1's negative input, related to the SENSE pin voltage by the appropriate resistor-divider ratio, is higher than the 1.25V reference voltage, A1's output is low. A2, A3 and the oscillator are turned off, drawing no current. Only the reference and A1 consume current, typically 120µA. When the voltage at A1's negative input decreases below 1.25V, overcoming A1's 6mV hysteresis, A1's output goes high, enabling the oscillator, current comparator A2, and driver A3. Quiescent current increases to 2mA as the device prepares for high current switching. Q1 then turns on in a controlled saturation for (nominally) 5.3µs or until current comparator A2 trips, whichever comes first. After a fixed off-time of (nominally) 1.2µs, Q1 turns on again. Refering to Figure 2, the LT1300's switching causes current to alternately build up in L1 and dump into output capacitor C1via D1, increasing the output voltage. When the output is high enough to cause A1's output to go low (Figure 1), switching action ceases. C1 is left to supply current to the

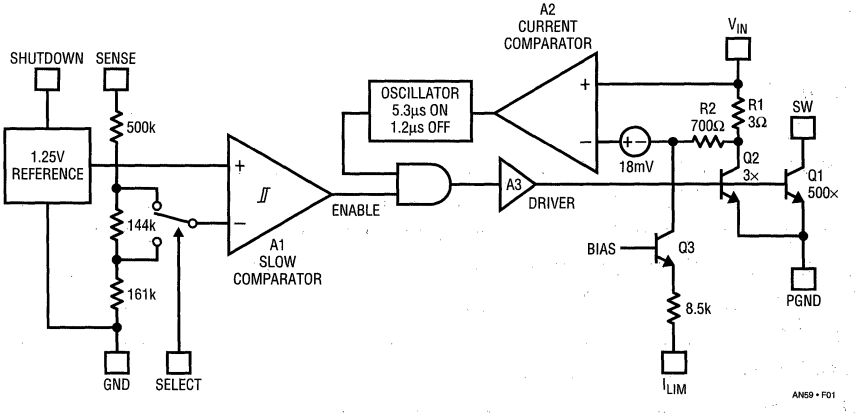


Figure 1. LT1300/LT1301 Block Diagram

load until V_{OUT} decreases enough to force A1's output high, and the entire cycle repeats. If switch current reaches 1A, causing A2 to trip, switch on-time is reduced and off-time increases slightly. This allows continuous mode operation during bursts. Current comparator A2 monitors the voltage across 3Ω resistor R1 which is directly related to inductor L1's current. Q2's collector current is set by the emitter-area ratio to 0.6% of Q1's collector current. When R1's voltage drop exceeds 18mV, corresponding to 1A inductor current, A2's output goes high, truncating the on-time portion of the oscillator cycle and increasing off-time to about 2μs as shown in Figure 3, trace A. This programmed peak current can be reduced by tying the I_{LIM} pin to ground, causing 15μA to flow through R2 into Q3's collector. Q3's current causes a 10.4mV drop in R2, so that only an additional 7.6mV is required across R1 to turn off the switch. This corresponds to a 400mA switch current, as shown in Figure 3, trace B. The reduced peak

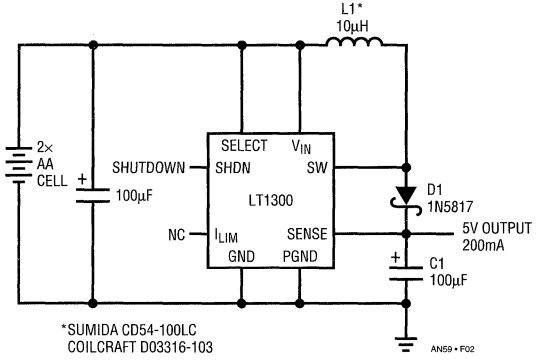


Figure 2. 2-Cell to 5V DC/DC Converter Delivers >200mA with a 2V Input

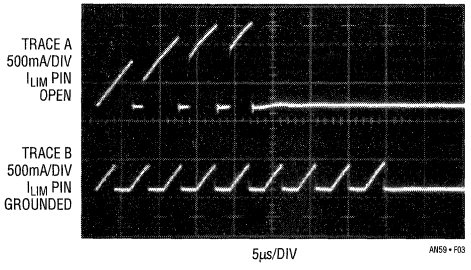


Figure 3. Switch Pin Current with I_{LIM} Floating or Grounded

Burst Mode™ Operation

Burst Mode operation, a technique used by many LTC switching regulator products, extends high efficiency over widely varying loads.

At light load, switching regulators employing traditional PWM regulation techniques suffer from low efficiency. This is primarily due to relatively high quiescent (or housekeeping) supply current and AC switching iosses resulting from constant frequency operation.

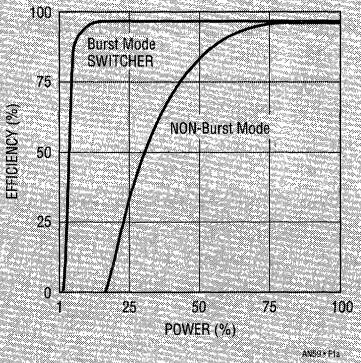


Figure 1a. Characteristics of Burst and Non-Burst Switchers

As seen in Figure 1a, the switching regulator not using Burst Mode operation does not reach peak efficiency until load power approaches 100%. Relatively high fixed power drain inside the regulator accounts for the efficiency fall-off as load is decreased. The regulator utilizing Burst Mode operation, on the other hand, maintains its high efficiency at light loads. It does this by delivering energy to the output in discrete peak efficiency packets. The energy packets result in a small amount of ripple voltage (typically 50mV) on the output. When not delivering these packets of energy to the output, the regulator puts itself in a "sleep" mode with only a voltage reference and a comparator powered up. These two functions can be accomplished with very low power drain. As the load is decreased to zero, even the small amount of power consumed in sleep mode becomes significant compared to the load, resulting ultimately in decreasing efficiency.

switch current reduces I^2R losses in Q1, L1, C1, and D1. You can increase efficiency by doing this provided that the accompaning reduction in full load output current is acceptable. Lower peak currents also extend alkaline battery life due to the alkaline cells' high internal impedance.

5V from 2 Cells

Figure 2's circuit provides 5V from a 2-cell input. Shutdown is effected by taking the SHUTDOWN pin high. V_{IN} current drops to 10µA in this condition. This simple boost topology does not provide output isolation and in shutdown the load is still connected to the battery via L1 and D1. Figure 4 shows the efficiency of the circuit with a range of input voltages, including a fresh battery (3V) and an "almost dead" battery (2V). At load currents below a few milliamperes, the 120µA quiescent current of the device becomes significant, causing the fall-off in efficiency detailed in Figure 4. At load currents in the 20mA to 200mA range, efficiency flattens out in the 80% to 88% range, depending on the input. Figure 5 details circuit operation. V_{OUT} is shown in trace A. The burst repetition pattern is clearly shown as V_{OUT} decays, then steps back up due to switching action. Trace B shows the voltage at the switch node. The damped, high frequency waveform at the end of each burst is due to the inductor "ringing off," forming an LC tank with the switch and diode capacitance. It is not harmful and contains far less energy than the high speed edge which occurs when the switch turns off. Switch current is shown in trace C. The current comparator inside the LT1300 controls peak switch current, turning off the switch when the current reaches approximately 1A.

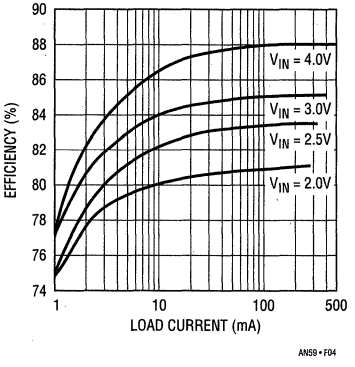


Figure 4. Efficiency of Figure 2's Circuit

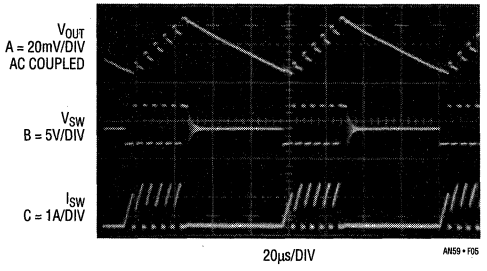


Figure 5. Burst Mode Operation in Action

Although efficiency curves present useful information, a more important measure of battery-powered DC/DC converter performance is operating life. Figures 6 and 7 detail battery life tests with Figure 2's circuit at load currents of 100mA and 200mA respectively. Operating life curves are shown using both Eveready E91 alkaline cells and new L91 "Hi-Energy" lithium cells. These lithium cells, new to the market, are specifically designed for high drain applications. The performance advantage of lithium is about 2:1 at 100mA load current (Figure 6), increasing to 2.5:1 at 200mA load (Figure 7). Alkaline cells perform poorly at high drain rates because their internal impedance ranges

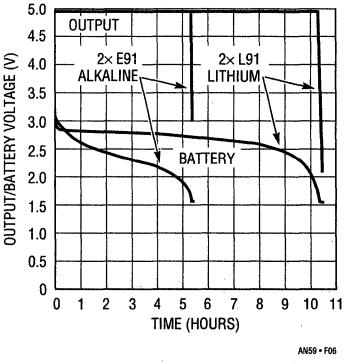


Figure 6. Two Eveready L91 Lithium AA Cells Provide Approximately Twice the Life of E91 AA Alkaline Cells at a 100mA Load Current

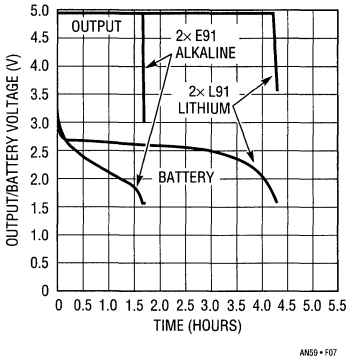


Figure 7. Doubling Load Current to 200mA Causes E91 Alkaline Battery Life to Drop by 2/3; L91 Lithium Battery Shows 2.5:1 Difference in Operating Life

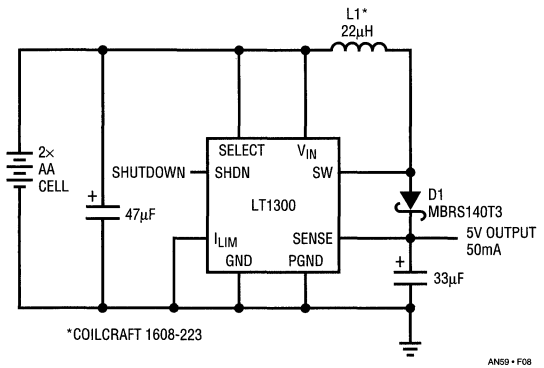


Figure 8. Lower Power Applications Can Use Smaller Components. L1 is Tallest Component at 3.1mm

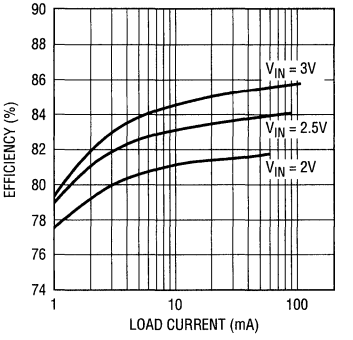


Figure 9. Efficiency of Figure 8's Circuit

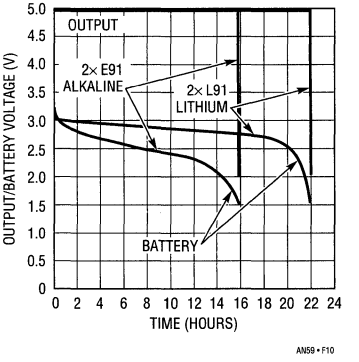


Figure 10. 50mA Load and Reduced Switch Current Are Kind to E91 AA Alkaline Battery; the Advantages of L91 Lithium Are Not as Evident

from 0.20Ω to 0.50Ω, causing a large voltage drop within the cell. The alkaline cells feel quite warm at 200mA load current, the result of I^2R losses inside the cells.

The reduced power circuit shown in Figure 8 can generate 5V at currents up to 50mA. Here the I_{LIM} pin is grounded, reducing peak switch current to 400mA. Lower profile components can be used in this circuit. The capacitors are C-case size solid tantalum and inductor L1 is the tallest component at 3.2mm. The reduced peak current also extends battery life since the I^2R loss due to internal battery impedance is reduced. Figure 9 details efficiency versus load current for several input voltages and Figure 10 shows battery life at a 50mA load. Note that the L91 lithium battery lasts only about 40% longer than the alkaline. The higher cost of the lithium cells makes the alkaline cells more cost effective in this application. A pair of Eveready AAA alkaline cells (type E92) lasts 96.6 hours with 5mA load, very close to the rated capacity of the battery.

A 4-Cell Application

A 4-cell pack is a convenient, popular battery size. Alkaline cells are sold in 4-packs at retail stores and four cells usually provide sufficient energy to keep battery replacement frequency reasonable. Generating 5V from four cells, however, is a bit tricky. A fresh 4-cell pack has a terminal voltage of 6.4V but at the end of its life, the pack's terminal voltage is around 3.2V; hence, the DC/DC converter must step the voltage either up or down, depending on the state of the batteries.

A flyback topology with a costly, custom designed transformer could be employed, but Figure 11's circuit gets around these problems by using a flying capacitor scheme along with a second inductor. The circuit also isolates the input from the output, allowing the output to go to 0V during shutdown. The circuit can be divided conceptually into boost and buck sections. L1 and the LT1300 switch comprise the boost or step-up section, and L2, D1, and C3 comprise the buck or step-down section. C2 is charged to V_{IN} and acts as a level shift between the two sections. The switch node toggles between ground and $V_{IN} + V_{OUT}$, and the L2-C2 diode node toggles between $-V_{IN}$ and $V_{OUT} + V_D$. Figure 12 shows efficiency versus load current for the circuit. All four energy storage elements must handle power, which accounts for the lower efficiency of this circuit compared to the simpler boost circuit in Figure 2.

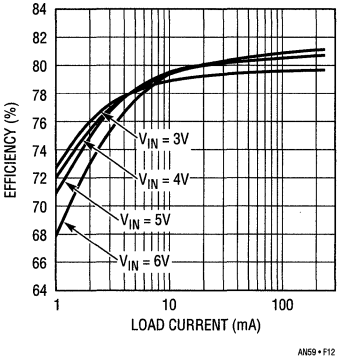


Figure 12. Efficiency of Up-Down Converter in Figure 11

Efficiency is directly related to the ESR and DCR of the capacitors and inductors used. Better capacitors cost more money. Better inductors do not necessarily cost more, but they do take up more space. Worst case RMS current through C2 occurs at minimum input voltage and measures 0.4A at full load with a 3V input. C2's specified maximum RMS current must be greater than this worst case current. The Sanyo capacitors noted specify a maximum ESR of 0.045Ω with a maximum ripple current rating of 2.1A. The Gowanda inductors specify a maximum DCR of 0.058Ω.

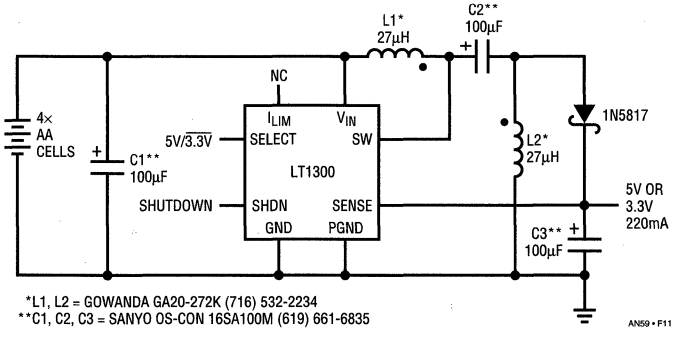


Figure 11. 4-Cell to 3.3V or 5V Converter Output Goes to Zero When in Shutdown. Inductors May Have, But Do Not Require Coupling; a Transformer or Two Separate Units Can Be Used

LT1301 Outputs 5V or 12V

The LT1301 is identical to the LT1300 in every way except output voltage. The LT1301 can be set to a 5V or 12V output via its SELECT pin. Figure 13 shows a simple 3.3V or 5V to 12V step-up converter. It can generate 120mA at 12V from either 3.3V or 5V inputs, enabling the circuit to provide VPP on a PCMCIA card socket. Figure 14 shows the circuit's efficiency. Switch voltage drop is a smaller percentage of input voltage at 5V than 3.3V, resulting in a high efficiency at 5V input.

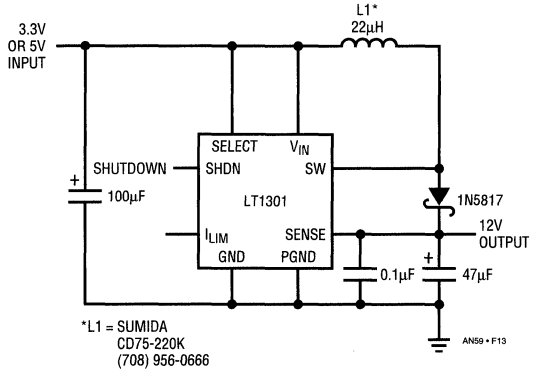


Figure 13. LT1301 Delivers 12V from 3.3V or 5V Input

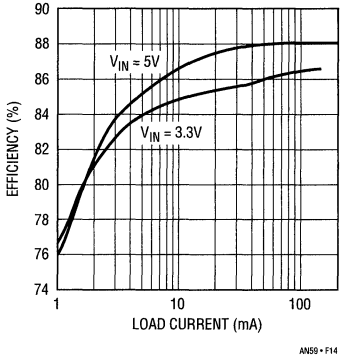


Figure 14. Efficiency of Figure 13's Circuit

THE LT1300: TWO CELLS TO REAL WORLD INTERFACE

By Dale Eagar

Introduction

The LT1300 micropower, high speed, step-up DC/DC converter opens up many new applications to the user, such as those requiring high efficiency in battery-operated equipment. The LT1300 can be used to produce high voltages for many specialized tasks with high efficiency. Here are three such applications. In the first application, a flame detector, the LT1300 is used to produce $325V_{DC}$ while drawing a mere 200µA from two C-size cells.

Flame Sensor

An interesting characteristic of flame is that it emits short wavelength ultraviolet light (<260nm). This short wavelength light falls into a window of the light spectrum that is relatively empty. Tungsten light, fluorescent light and sunlight below the atmosphere are almost totally devoid of spectral energy in this window. The circuit shown in Figure 15 uses a photoelectric sensor with a sufficiently high cathode work function to make it blind to anything with a wavelength longer than 260nm (such as normal UV, visible light or infrared). Cathode work function is a measure of how hard it is to free an electron from an atom; when related to light illuminating a cathode, it specifies the minimum energy of a photon that can liberate an electron. UV photons have higher energy than visible light.

Theory of Operation (see Figure 15)

The LT1300 and transformer T1 form a flyback converter to step up the voltage from 3V to 325V. The secondary winding of T1 connects through D1 (a MUR1100) to C1, a holding capacitor for the 325VDC, which in turn is applied to the anode of the photoelectric sensor tube V1. The LT1300 SENSE pin senses the voltage on C1, as scaled by the turns ratio, through T1. The voltage on the primary winding is programmed to be 10.6V, translating to 325V on C1. When C1 has charged to 325V the feedback loop comprised of D3, R2 and Q1 kicks in and charges C4 through D4. When the voltage at C4 exceeds 3.3V the LT1300 goes into its wait mode. In wait mode the LT1300

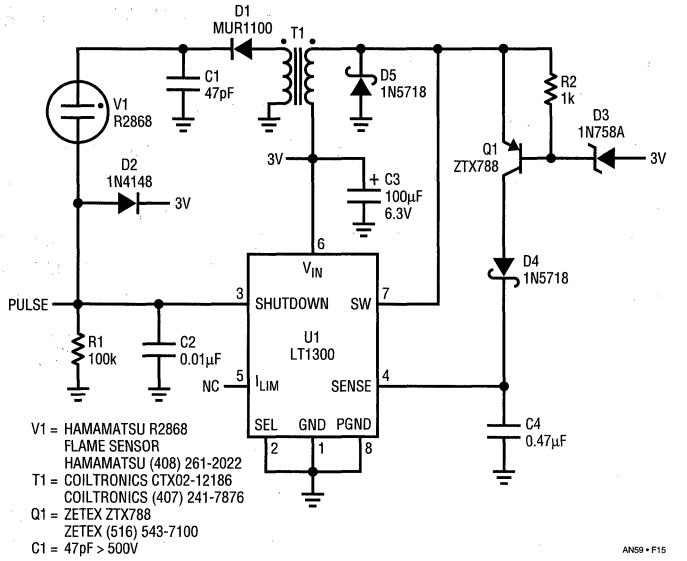


Figure 15. Flame Detector

consumes only 120µA of current. The LT1300 stays in wait mode until the voltage on C4 falls below 3.3V at which time the LT1300 turns on to burst recharge both C1 and C4. Burst Mode operation ensures 30Hz oscillation in this system. This rate is determined by the value of C4, the internal sense resistance to ground in the LT1300 (approximately 1MΩ), and the amount of overcharge C4 gets when charging. D5 is a Schottky catch diode to keep reverse current out of U1.

When illuminated with a photon of sufficient energy the photoelectric tube's cathode liberates an electron. The tube V1 has 325V across its terminals to get sufficient energy into a liberated photo-electron to ionize the gas that fills the tube. Once the gas in the tube ionizes there are more electrons available; they cause a chain reaction in the tube that causes the tube to avalanche. When the tube avalanches most of the charge on C1 is transferred to C2 and the voltage across C1 drops to a fraction of its original 325V. When C2 has charged to 3.6V all the excess charge residing in C1 gets bypassed through D2 back into the battery. The voltage across C2 is the output signal called PULSE. PULSE asserts the shutdown pin of the LT1300, allowing the plasma in the photoelectric tube to quench.

For you analog purists, page 8 of the October 1993 issue of *Linear Technology* magazine shows a discriminator circuit with low-battery detect for a complete 3V flame alarm. The discriminator is needed because the photo detector occasionally detects a cosmic ray or some rare room light photon.

Infinite Input Impedance Voltage Buffer

In the flame detector circuit (Figure 15), it is difficult to measure the voltage across C1 because almost any load invalidates the meter reading. This next application for the LT1300 is a voltage buffer that overcomes this measurement problem. This is a four-terminal, unity-gain buffer as shown functionally in Figure 16. The input impedance is

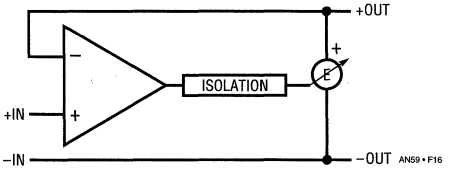


Figure 16. Voltage Buffer Block Diagram

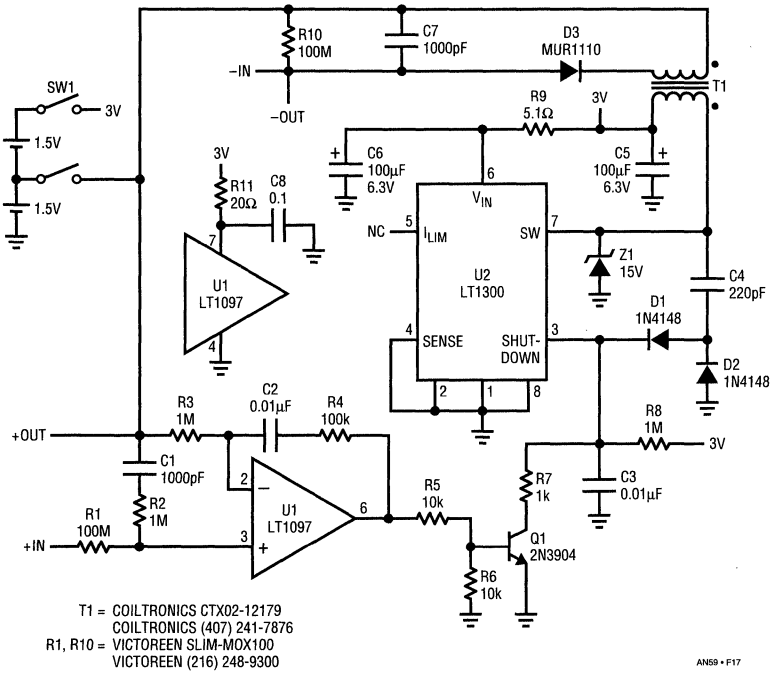


Figure 17. Voltage Buffer Schematic

essentially infinite, the input bias current is negligible and the input offset voltage is less than 0.05V. The output voltage tracks the input voltage from 0V to 520V. For safety (and to isolate the input capacitance) a 100M resistor is placed in series with the input, but with the ±570pA of input bias current (over temperature) for the LT1097, this translates into only ±57mV of additional offset. The input impedance of this buffer measures four trillion ohms when measured with a 100V to 400V input. The detailed circuit is shown in Figure 17.

Theory of Operation

U1 monitors the voltage difference between the circuit's noninverting input and output and attempts to make it zero. If the voltage on the noninverting input is less than the voltage on the noninverting output, U1's output goes positive, turning Q1 on slightly. Q1 acts as a current sink discharging C3. When the voltage on C3 falls below approximately 0.6V, U2 is enabled. When it is enabled U2 turns its switch on (U2's pin 7 pulls low, to near 0V). This causes approximately 3V to be imposed across the primary winding of T1. The magnetizing inductance of the primary winding of T1, across which a voltage is applied, requires a steadily increasing current. At the same time, C4 is charged through D2. When the current flowing through the switch of the LT1300 reaches 1A, the LT1300 switches off. The magnetizing inductance of the primary winding of T1, seeing that the LT1300 is attempting to discontinue current flow, takes over by swinging positive in voltage until it finds something that will take the 1A of magnetizing current. While the primary winding is finding somewhere to put the magnetizing current, the secondary winding takes it upon itself to do the same, but due to its turns ratio with the primary winding, it moves 100 times faster and 100 times as far as the primary winding. T1's secondary dumps a significant portion of the magnetizing energy into C7 via D3, thus forming a flyback inverter.

Z1 dissipates the energy stored in T1's leakage inductance. During the flyback time, C4 charges C3 through D1. This causes the voltage across C3 to exceed 0.6V, shutting down U2. U2 stays shut down until Q1 discharges C3 to restart the sequence.

When the +output voltage is more positive than the + input voltage the output of U1 goes low, Q1 stays off, R8 keeps C3 charged to more than 0.6V, and U2 stays shut down. The parallel combination of R10 and the load resistance (e.g., 10M in a handheld voltmeter) discharges C7 and the +output and the +input voltages are again equal. The current output of this circuit is limited to a safe value (1mA at 50V, 0.1mA at 500V) even when the + input is attached to 500V. We do not recommend increasing the value of C7 because at higher voltages it may become a shock hazard. Battery life is 40 hours for a pair of AA alkaline batteries driving 10MΩ at 500V.

Cold Cathode Florescent Lamp Driver

CCFLs seem to be the latest craze; they offer high brightness, long life, small size and produce white light. Figure 18 shows a CCFL driver circuit.

Theory of Operation

This is a forward/flyback inverter optimized for minimum parts count. When enabled, U1 charges the primary winding of T1 to 1A, and lets go. T1 then flies back exciting many hundreds of volts across its secondary winding, which in turn ionizes the CCFL. Because the initial current through the CCFL is only in one direction, C2 takes on a DC potential. As the circuit runs, the voltage across C2 stabilizes at about 100VDC. Additionally, C2 removes the DC current component from the tube, extending tube life. The nonlinear V/I characteristic of the CCFL, in conjunction with C2, forces the converter to run in both forward and flyback modes simultaneously. The light intensity can be pulse-width modulated by modulating the shutdown pin. When the shutdown pin is pulled high the LT1300 goes into its shutdown mode where it draws only 10μA of input current.

Electronic Light Stick

Camping in November with my kids has its own unique problems, even if we aren't camping in six feet of snow. Although we had the usual light sources something was missing, namely a light that simulates the natural sunset at bedtime to wind the kids down for the night. The circuit in Figures 18 and 19 (see explantation below) details a high efficiency fluorescent lantern with a built-in sunset feature.

The function of the circuit is as follows:

- To turn on: switch SW1 into the ON position.
- To turn off fast: switch SW1 into the OFF position.
- To simulate sunset:
  1. Turn light ON.
  2. Switch SW1 into the SUNSET position.

This application uses the circuitry of both Figure 18 and Figure 19. The pulse-width output of Figure 19 drives the pulse-width input of Figure 18.

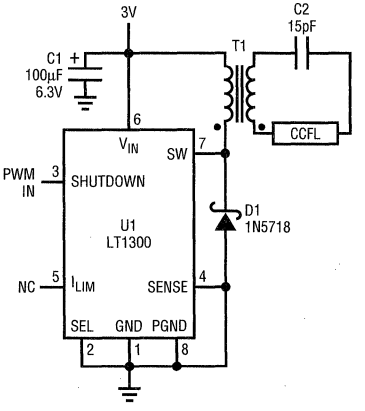


Figure 18. CCFL Driver

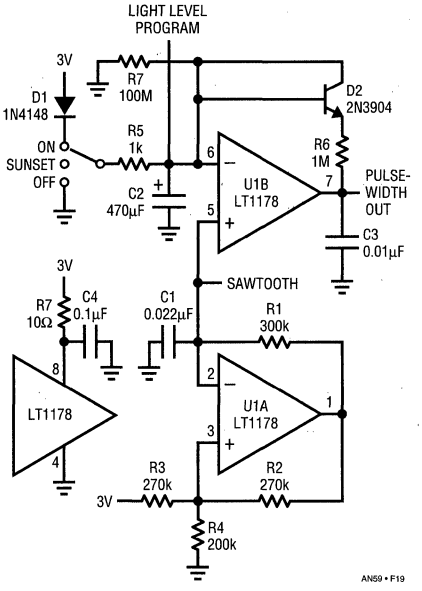


Figure 19. Electronic Light Stick Controller for the CCFL Driver Circuit Shown in Figure 18. This Controller, When Controlling the CCFL, Causes the Light Output Level to Fade from Full Brightness to Off, Thus Simulating a Natural Sunset.

U1A, R1 to R4 and C1 form a sawtooth oscillator for pulse-width modulating the light (implementing light levels less than 100%). U1B acts as a comparator, comparing the sawtooth output of the oscillator with the programmed light level (as seen on the +terminal of C2). C2 is the holding capacitor that programs the light level; when it is charged to 2.5V the light is on 100% of the time. As the voltage on C2 drops below 2.5V, the overall light level decreases because the light is being pulse-width modulated. When the voltage on C2 is at or below 1V the light is off. D1 and R5 charge and hold C2 when SW1 is in the ON position. R5 and SW1 discharge and hold C2 when SW1 is in the OFF position. The combination of D2, R6 and U1B discharge C2 when SW1 is in the SUNSET position. The discharging of C2 when in the SUNSET mode is doubly exponential causing the tail end of the simulated sunset to go very slowly (a good idea because kids have a logarithmic response to light). The first exponential aspect of the SUNSET decay is implemented by R6 and C2 which form an exponential RC time constant. The second exponential aspect of the SUNSET decay is implemented because R6 is driven by U1B pin 7, whose duty factor is changing, causing the off-time to decrease exponentially as the light level fades. The output of U1B is a pulse-width modulated level gating the light driver on and off. The lamp is illuminated when U1B's output is low. C3 is a trash compactor and R7 and C4 form a trash compactor to decouple U1 from the high frequency ripple generated by the switcher.

Constant Current Source

The LT1300 can be configured as a constant current source, a current source that not only possesses good power conversion efficiency, but can be shut down to a state of practically no current draw. These benefits coupled with the LT1300's ability to operate over a wide input voltage range, make the LT1300 an ideal candidate for many current operated devices. Popular uses include solenoid drivers, relay drivers, small motor drives and LED drivers.

Here is an example of a high efficiency LED driver. The LED light source (shown in Figure 20) is used in applications

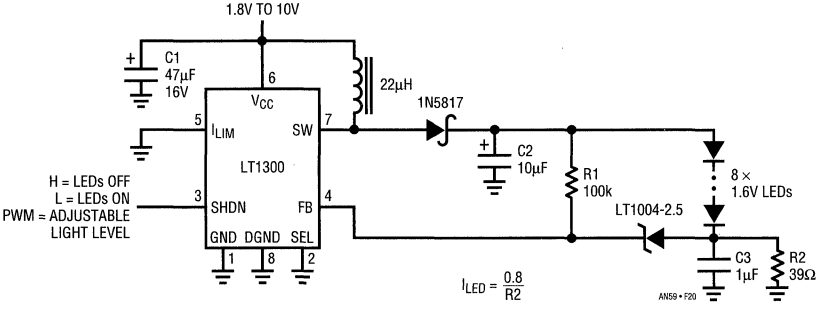


Figure 20. Backlight LED Driver

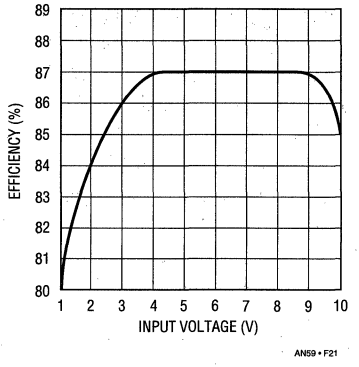


Figure 21. Efficiency of LED Driver

ranging from LCD backlights to special flashlights that preserve full night vision. This circuit sports an impressive list of features:

- Logic Input to Strobe LED's On/Off
- Low Current Draw When Off (10μA)
- Constant LED Drive Current When On (20mA)
- LED Current Unaffected by Temperature
- LED Current Constant with Input Voltage Range (1.8V to 10V)
- High Overall Efficiency (87%)
- Small Size

Theory of Operation

When enabled the LT1300 runs in Burst Mode operation, regulating the voltage on the FB pin to 3.3V. Subtracting 2.5V (corresponding to the knee voltage of the LT1004-2.5) from the 3.3V voltage at the FB pin yields 0.8V, which is seen across R2. This 0.8V and the value of R2 sets the output current level through the LEDs. For proper functionality the voltage across the LED stack should be:

1. Greater than the maximum input voltage less one Schottky drop.
2. Less than 14V.

The LT1300 is optimized for battery operation and lends itself to these and many more applications.

PCMCIA Card and Card Socket Power Management

Doug La Porte

INTRODUCTION

Most portable computers have built-in sockets to accept small PC cards for use as extended memories, fax modems, network interfaces, wireless communicators and a wide assortment of other functions. The Personal Computer Memory Card International Association (PCMCIA) has released specifications that outline the general power requirements for these cards.

The specification calls for an unusual amount of voltage switching. Both supplies are switchable to different voltages to accommodate a wide range of card types. The V_{CC} supply must provide either 3.3V or 5V. The VPP supply must source 12V, 3.3V, 5V, 0V and realize a high impedance state. These diverse, specific requirements call for specialized solutions.

PC card designers may want to design their cards to require the V_{CC} supply only. Flash memory card designers who need to ensure a clean VPP supply may generate their own 12V on the card. Type I PC cards, at an outside thickness of 3.3mm, require ultra-thin highly efficient circuitry. The DC/DC converter IC, inductor, capacitors and diodes are critical components that require unique design to meet the stringent height requirements.

PCMCIA SOCKET POWER MANAGEMENT

PCMCIA Specification Voltage Switching Requirements

Host power delivery to the PC card socket flows through two paths: the main V_{CC} supply pins and the VPP programming pins. Figure 1 shows a typical system's connections. The V_{CC} supply must be capable of providing up to 1A at either 3.3V or 5V. The latest specification has provisions for a future voltage referred to as X.XV (X.X to be less than 3.3V). The actual voltage value will be determined at a later date. The VPP supply must source 12V at up to 120mA, the V_{CC} voltage at lesser currents, 0V and realize a high impedance state.

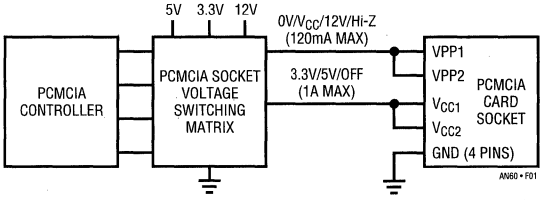


Figure 1. Typical Single Socket Power Management

The PCMCIA specification requires the V_{CC} voltage to be selectable from 3.3V, 5V or an off state. The X.X voltage of the future will not be addressed until the voltage has been defined. The specification does not outline any current draw requirements. The industry standard maximum current that the socket will support is 1A. This number is derived from the maximum connector rating of 500mA per pin and assumes both pins in good condition with current being shared equally. In practice this amount of current draw is exceptional and should not be encouraged for continuous use. One of the most stringent actual requirements is a Type III hard disk drive card. Present hard drives require 5V at 600mA to 820mA for a short duration during spin-up with current draw dropping to 300mA to 420mA during read and write operations.

The PCMCIA specification requires the VPP voltage to be selectable from 0V, V_{CC}, 12V or a high impedance state. Again, the specification does not outline any current draw requirements. The VPP voltage's primary use is for programming flash memory with the current requirements derived from the flash memory needs. A single byte wide flash memory device will require 12V at 30mA for write or erase operations. The PC card bus is 16-bits wide necessitating two flash devices being written to at the same instant. A standard flash memory card will require at least 60mA of current during write or erase operations. Many flash cards designed as solid state disc drives, often referred to as ATA

flash drives, will have two 16-bit wide banks of memory to facilitate simultaneous writing and erasing. This speeds card operation but will double the current requirement. These cards will draw 120mA while writing/erasing.

Additional Practical Considerations

While the PCMCIA specification provides the basis for the voltage switching requirements, there are many real world requirements that must also be considered. These issues include switch resistance, inrush current during voltage switching, voltage ringing during switching, short-circuit protection and cost effectiveness as a system, not just the function.

The MOSFET switch on-resistance $R_{DS(ON)}$, should be low enough to maintain the correct voltage tolerance at the card input. The most critical case is when the V_{CC} is 5V. The specification requires the voltage to be 5V ±5% (±0.25V). The most stringent requirement would be during hard disk drive spin-up where the card can pull up to 820mA. Many systems will have a main supply with a tolerance of ±2%. When the main power supply is at its minimum value of 4.90V, this leaves only 0.150V maximum voltage drop across the switch. To ensure that the hard drive will spin-up without dropping the voltage below 4.75V the switch on-resistance must be less than 0.183Ω. To ensure operation at the 1A limit the switch on-resistance must be less than 0.150Ω. It is common practice to raise the nominal voltage slightly above 5V to relax the voltage tolerance. For example, raising the nominal voltage to 5.10V will allow the tolerance to increase to ±4%.

The nature of PC cards and portable systems requires the card being powered on and off as needed to conserve power. With many PC cards drawing up 2W, this power up/down sequencing can put demanding transient requirements on your system power supply. More important than the static current requirement of the card is the dynamic requirement due to input capacitance. Cards will have up to 150µF of input capacitance. This large capacitor coupled with a fast switch will pull many amperes of current from the system supply. With a simple switch the only factors limiting the inrush current are the switch's rise time, the switch's $R_{DS(ON)}$, the card input capacitor value and the input capacitor's equivalent series resistance (ESR). Many large input capacitors will be for on-card switching power supplies and will likely have an ESR in the 0.1Ω range. As noted above, the switch's $R_{DS(ON)}$ would be 0.183Ω or lower. These low resistance values will do little to limit the inrush current. In a simple switch, this leaves rise time as the only parameter that can keep inrush current to manageable levels. More sophisticated switches will also employ current limiting. Many simple switches, without current limiting, have rise times as fast as 100µs. This gives a peak current of over 7A! With the rise time slowed to 500µs, the peak current is down to a reasonable 1.5A. Current limiting will protect the system against even larger input capacitors. To make the transient response of the system supply manageable, the PCMCIA switch should have a controlled, slowed rise time and current limiting. Slowed rise time and current limiting eliminate inadvertent system resets triggered by a momentary pull on the main supply.

The VPP lines also require slowed switch rise times. The VPP pins are for flash memory programming and will not have excessive input capacitance. As such, inrush current is not a major issue. The switch times must be slowed to avoid voltage ringing and overshoot at the flash memory device. The flash memory device has a 14V absolute maximum input voltage specification. Voltages beyond this limit, for as little as 20ns, can permanently damage the device. If the switch has a fast rise time there will be ringing due to the trace and connector inductance. It will take only a couple of inches of trace to form enough inductance to cause excessive ringing. For this reason the VPP switch must have a controlled, slowed rise time.

The PCMCIA socket will usually have a small door to protect it from unwanted objects entering. Other than this door, the socket pins are exposed to the outside world. The exposed socket pins are vulnerable to being shorted by foreign objects such as paper clips. The card installer is generally not trained and may have little or no technical knowledge. Some users may attempt to install damaged, possibly short-circuited cards. In short, once the product is in the hands of the consumer, the designer and manufacturer have little control over its use and abuse. To ensure a robust system and satisfied customer, PCMCIA switch protection features such as current limiting and thermal shutdown are

a necessity. These features will protect the card, socket and main system power supply.

System design issues also deserve consideration. The switch matrix's digital interface should connect directly to industry standard controllers. This may seem a trivial issue but additional glue logic will add unnecessary cost and consume real estate. The other system issue is the availability of a 12V supply. Some systems have a general purpose 12V supply in the system design from the start and there are only minor issues to consider. The flash memory devices have a strict 12V ±0.6V specification for guaranteed programming. When the main 12V supply tolerance is added to the switch resistance, the main supply tolerance must be very tight. The voltage should also be free of excessive noise spikes that may exceed the flash device maximum voltage limit. In addition, some switch matrix devices need a constant 12V supply to operate while those incorporating on-chip charge pumps require 12V only during flash memory programming. Deriving the clean 12V supply in a simple, cost effective manner is a significant part of the design that must not be overlooked.

LTC1472: Fully Protected Switch Matrix

The LTC®1472 is a complete V_{CC} and VPP switch matrix that addresses all the PCMCIA socket switching needs. The part is fully integrated with no need for external switching FETs. V_{CC} switch $R_{DS(ON)}$ is below 0.120Ω to support the current requirement of up to 1A. The V_{CC} output is switched between 3.3V, 5V and high impedance. VPP 12V switch $R_{DS(ON)}$ is below 0.5Ω to support its current requirement. The VPP output pin is switched between 0V,V_{CC}, 12V and high impedance. The V_{CC} logic inputs are exclusively OR'd to allow direct interfacing with both logic high and logic low industry standard controllers without any external glue logic. The LTC1472 is available in the space saving narrow 16-pin SOIC package.

The LTC1472 features SafeSlot™ protection. Built-in SafeSlot current limiting and thermal shutdown features are vital to ensuring a robust and reliable system. The V_{CC} current limit is above the 1A socket limit to maintain compatibility with all existing cards yet provide protection against inadvertent short circuiting. The VPP current limit is above 200mA to also maintain compatibility and provide protection. All switches are break-before-make type with controlled rise and fall times for minimal system supply impact. The LTC1472's slowed rise time combined with the current limiting minimizes inrush current to manageable levels. Slowed rise time on the VPP switch ensures smooth voltage transitions without damaging ringing and overshoot.

Figure 2 shows a typical LTC1472 application used in conjunction with the LT®1301 to supply the 12V input. The LT1301 is optional. If your system already has a suitable 12V supply it can be directly connected to the VPP_{IN} pin. You should be cautious when using a general purpose 12V supply. Make certain that it does not have spikes or transients exceeding the flash memory 14V maximum voltage rating and that the regulation is within the 5% flash memory tolerance.

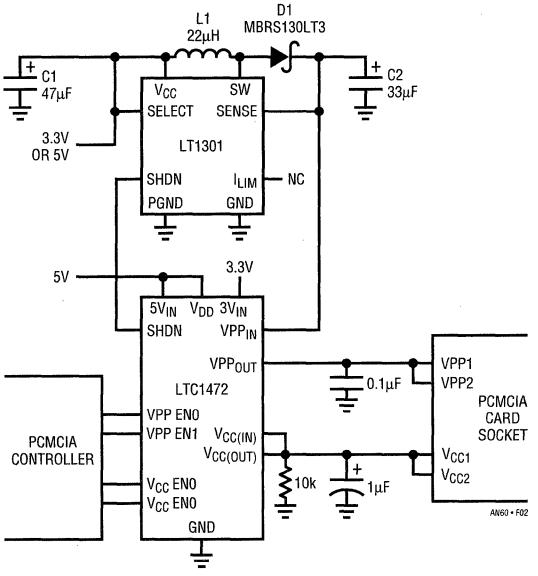


Figure 2. Typical LTC1472 Application with the LT1301 3.3V/5V Boost Regulator

SafeSlot is a trademark of Linear Technology Corporation

The LTC1472 does not require a continuous 12V supply. The device has on-chip charge pumps, running from the 5V supply for driving the switches. For this reason the LT1301 is in shutdown mode, consuming only 10μA, most of the time. The LT1301 becomes operational only when the controller programs the LTC1472 to deliver 12V to the VPP pin. The LTC1472 also conserves power by going to a low 1μA standby mode when both V_{CC} and VPP outputs are switched off. The schematic in Figure 2 includes a 10k pull-down resistor on the $V_{CC(OUT)}$ pin. This resistor will ensure that when switching the V_{CC} voltage from 5V to the off state, the voltage will not float at 5V. The current PCMCIA specification requires the voltage be pulled down to 0.8V within 300ms when turned off. This pull-down resistor is adequate to ensure proper operation.

LTC1470 V_{CC} Protected Switch Matrix with the LT1312 VPP Linear Regulator

Another approach is to use a linear regulator for VPP voltages with a protected V_{CC} switch. The LTC1470 is a complete V_{CC} switch matrix. The part is fully integrated with no need for external switching FETs. Performance specifications are the same as the V_{CC} section of the LTC1472 described above. The LTC1470 is available in the space saving 8-pin SOIC package with a dual version, the LTC1471 in a 16-pin narrow SOIC. The LT1312 is a programmable output voltage linear regulator designed specifically for PCMCIA VPP drive applications. The LT1312 takes a raw, unregulated 13V to 20V input supply and produces a clean, regulated, selectable output voltage in conformance with the PCMCIA standard. It comes in an 8-pin SOIC with a dual version, the LT1313 in a 16-pin narrow SOIC.

The LT1312's VPP pins are programmable to provide either 0V, 3.3V, 5V, 12V or a high impedance state. Figure 3 shows the basic block diagram of the LT1312. Two enable inputs (EN0 and EN1) and the V_{CC} Sense inputs select these five states. The logic inputs interface directly with logic high and logic low industry standard controllers. When a V_{CC} voltage is selected, a comparator in the LT1312 automatically switches the VPP_{OUT} pin to 5V or 3.3V depending on the voltage present at the Sense pin. The LT1312 has a 200mA nominal output current capability with a 250mA short-circuit current limit and thermal shutdown. These protection features can be very important when considering the overall reliability and robustness of the main system. As shown in Figure 4, the rise time of the LT1312 is sufficiently slow to avoid ringing and overshoot. An additional feature of the LT1312 is its low 25μA quiescent current in 0V or high impedance modes.

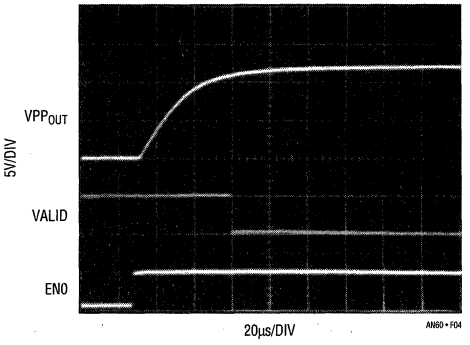


Figure 4. LT1312 VPP Switching Waveform

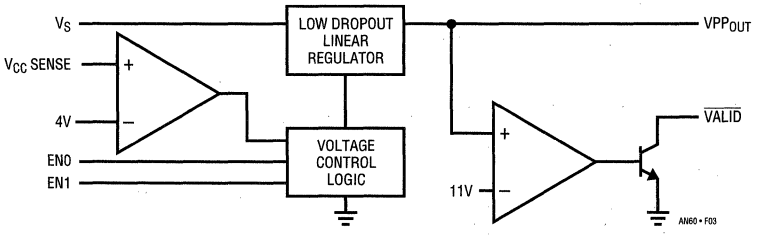


Figure 3. LT1312 Block Diagram

Like the LTC1472, the LTC1470 also features SafeSlot protection. The switches are break-before-make type with controlled rise and fall times for minimal system power supply impact. The built-in SafeSlot current limiting and thermal shutdown features are vital to ensuring a robust and reliable system. The LTC1470 also does not require a continuous 12V supply. The device has on-chip charge pumps running from the 5V supply for driving the switches.

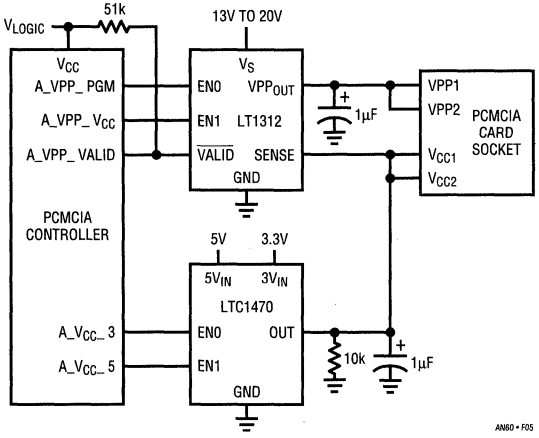


Figure 5. Typical LTC1470 Application with the LT1312 VPP Driver/Regulator

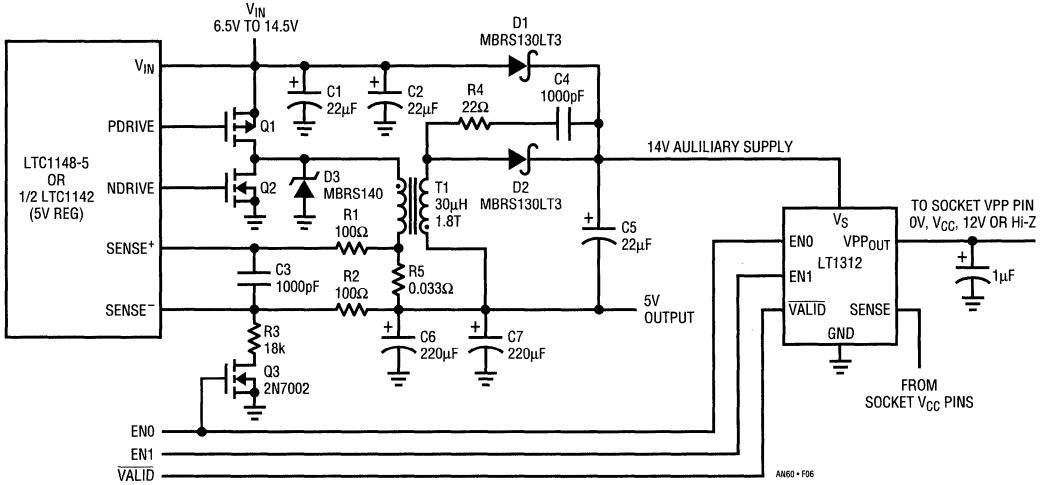
Figure 5 shows a typical LTC1470 application with the LT1312 used to control the VPP section. If your application does not require VPP switching, the LT1312 is eliminated. The LTC1470 conserves power by going to a low 1µA standby mode when the output is switched off. The schematic in Figure 5 includes a 10k pull-down resistor on the $V_{CC(OUT)}$ pin to guarantee that the V_{CC} voltage will not float when turned off.

Auxiliary Winding Power Supplies for Use with the LT1312

Because the LT1312 provides excellent output regulation, the input voltage may come from a loosely regulated source. One convenient and economic source of power is an auxiliary winding on the main 3.3V or 5V switching regulator inductor of the system power supply.

LTC1142 or LTC1148-5 Auxiliary Winding Power Supply

An auxiliary winding to the 5V inductor of an LTC1142 or LTC1148-5 based 5V power supply creates a loosely regulated 14V power supply as shown in Figure 6. Diode D2 rectifies the 9V output from this additional winding adding it to the main 5V output. (Note the phasing of the auxiliary winding shown in Figure 6.)



C1, C2: AVX TPSD226M025R0200
C5: AVX TPSD226M025R0200
C6, C7: AVX TPSE227M010R0100

Q1: SILICONIX Si9430DY
Q2: SILICONIX Si9410DY
T1: DALE LPE-6582-A026 (605) 665-9301

Figure 6. Deriving 14V Power from a 5V Auxiliary Winding

Referencing the auxiliary winding to the main 5V output provides DC current feedback from the auxiliary supply to the main 5V section. Returning the lead of C5 to the 5V output as shown improves the AC transient response.

A TTL logic high on the enable line (ENO) activates the 12V output. This will force the 5V section of the LTC1142 (or LTC1148-5) into the continuous mode of operation. A resistor divider, composed of R2, R3 and switch Q3 forces an offset to counteract the internal offset at the – Sense input of the part. Burst Mode™ operation ceases when this external offset cancels the device's built-in 25mV offset forcing the switching regulator into continuous mode operation. (See the LTC1142 and LTC1148 data sheets for further detail.) In this mode, the LT1312's output can be loaded without regard to the 5V output load.

Only when the LT1312 delivers 12V is the continuous operation mode invoked. The LT1312's input power comes directly from the main power source (battery pack) through diode D1 when delivering 0V, 3.3V or 5V. Again, the LT1312 output can be loaded without regard to loading on the 5V output of the regulator. For cases of fixed V_{CC} voltage (i.e., V_{CC} = 5V only), grounding the Sense pin of the LT1312 automatically selects 5V in the V_{CC} mode.

Figure 7 is a graph of the output voltage versus output current for the auxiliary 14V supply shown in Figure 6. Note that the auxiliary supply voltage is higher when the 5V output loading is heavier. This is due to the increased energy flowing through the main 5V inductor.

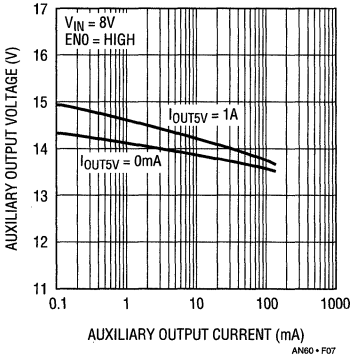


Figure 7. Auxiliary Winding Output Voltage vs Current

LTC1142 or LTC1148-3.3 Auxiliary Power for Low Input Voltage Applications

For low-battery count applications (<6.5V) it is necessary to modify the circuit of Figure 6. As the input voltage falls, the 5V duty cycle increases to the point where there is simply not enough time to transfer energy from the 5V primary winding to the auxiliary secondary winding. For applications where heavy 12V load currents exist in conjunction with these low input voltages, the auxiliary winding can be derived from the LTC1142's 3.3V section or from an LTC1148-3.3 part. The 3.3V duty cycle is more than adequate to support 12V currents. Figure 8 shows this circuit. In this case a transformer with a turns ratio of 1:3.6 replaces the 3.3V section inductor. In the previous circuit, power is drawn directly from the batteries through D1, when the switching regulator (LTC1142 or LTC1148-5) is in Burst Mode operation and the VPP pins require 3.3V or 5V. For these lower input voltages this technique is invalid as the input will fall below the LT1312 linear regulator's dropout voltage. To correct for this situation, the switch Q3 forces the switching regulator into continuous mode operation whenever 3.3V, 5V or 12V is selected.

Equipment with Existing 5V or 12V Supplies

The previous circuits were solutions for portable equipment that require multiple supplies from battery power. For line-powered equipment or products that already have 5V available, the designer need only to generate a rough supply to utilize the LT1312. Figure 9 shows how to use the LT1172 as a boost regulator to convert the 5V input to 13.75V for use by the LT1312.

Some equipment such as PCs will have an existing 12V supply. More often than not this supply is noisy and not well regulated to the 12V±5% flash memory specification. Figure 10 shows a solution utilizing the LT1111 boost regulator to deliver a 13.75V for input to the LT1312.

Burst Mode is a trademark of Linear Technology Corporation

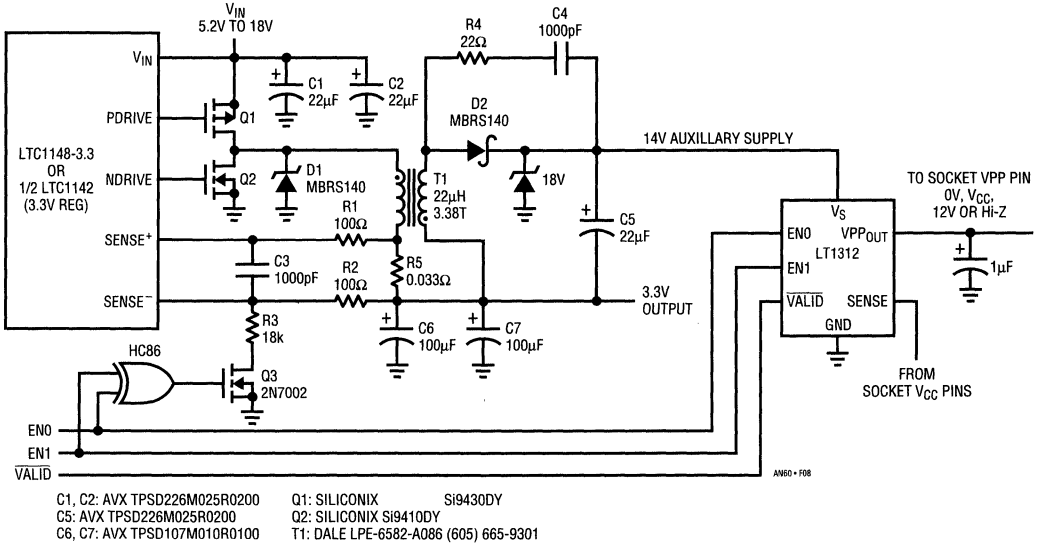


Figure 8. Deriving 14V Power from a 3.3V Auxiliary Winding

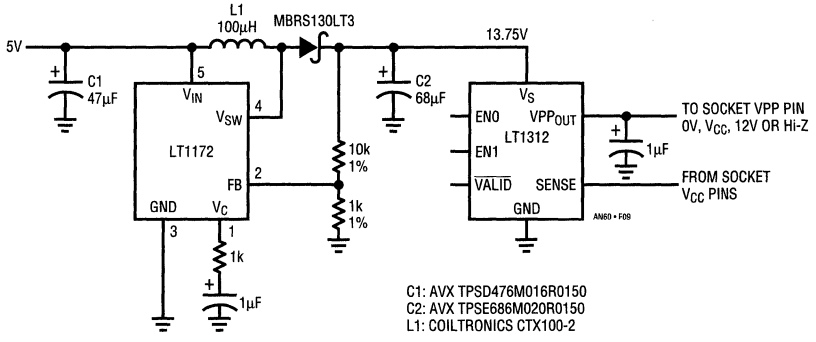


Figure 9. Local 5V to 13.75V Boost Regulator for Use with the LT1312

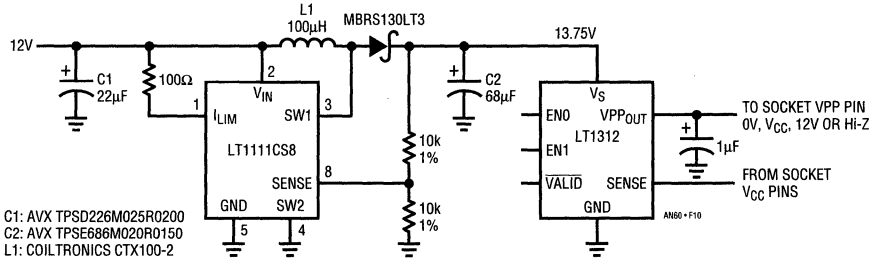


Figure 10. Local 12V to 13.75V Boost Regulator for Use with the LT1312

Dual Socket Design with the LTC1471 and LT1313

For applications requiring two PC card sockets the designer can use the dual versions of the LTC1470 and the LT1312. The LTC1471 dual V_{CC} switch matrix has the same performance characteristics as the LTC1470 and comes in the narrow body 16-pin SOIC. The LT1313 dual VPP regulator driver shares the same performance characteristics as the single version, the LT1312, and is also packaged in the narrow body 16-pin SOIC. Figure 11 shows a typical two-socket application using the LTC1471 for V_{CC} switching and the LT1313 regulating an overwinding to derive the VPP voltages. Performance is the same as if the single version were used but with some board space and cost savings realized.

LTC1314: V_{CC} Switch Driver and VPP Switch Matrix

Figure 12 shows another approach that is very space and power efficient. Here the LTC1314 PCMCIA switch matrix, used in conjunction with the LT1301 DC/DC converter, provides complete power management for a PCMCIA card socket. The LTC1314 and LT1301 combination provide a highly efficient, minimal parts count solution. This circuit is especially good for designers who are adding a PCMCIA socket to existing systems that currently have only 5V or 3.3V available. Table 1 shows the truth table for the LTC1314. The LTC1314's logic interface allows direct connection to active high V_{CC} or active low V_{CC} type controllers eliminating the need for additional glue logic.

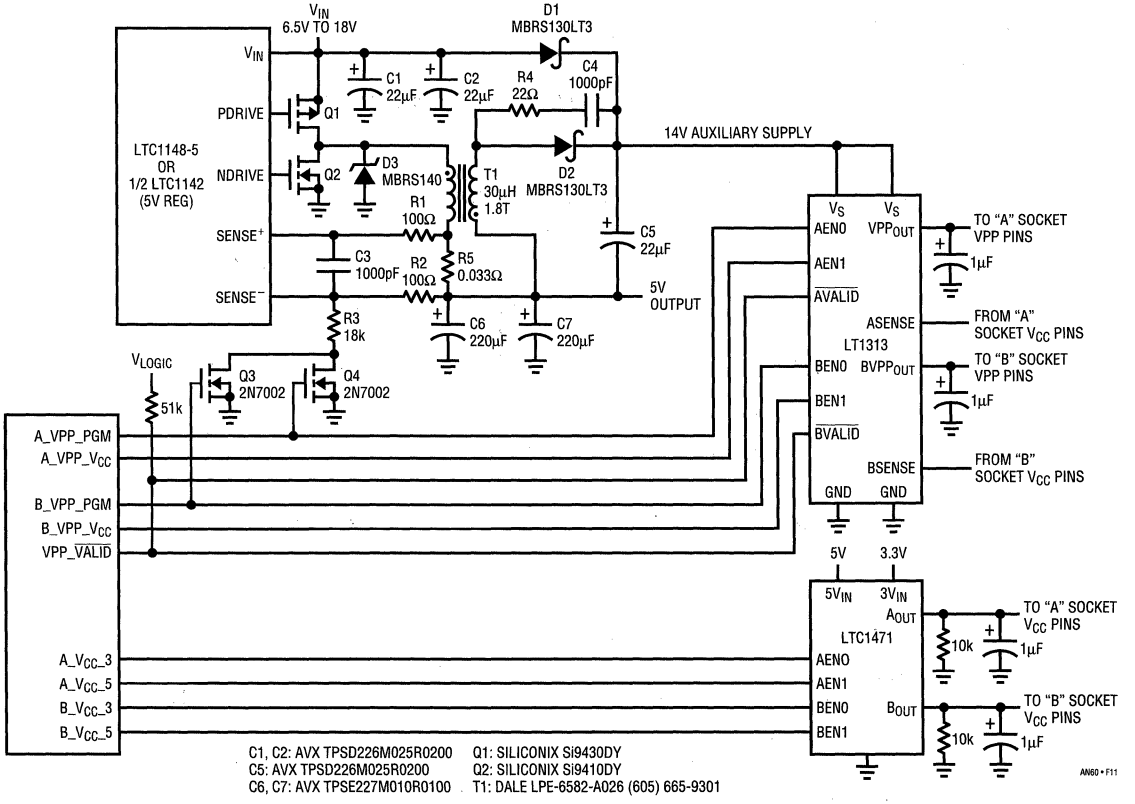


Figure 11. Typical Two-Socket Application with the LTC1471 and LT1313

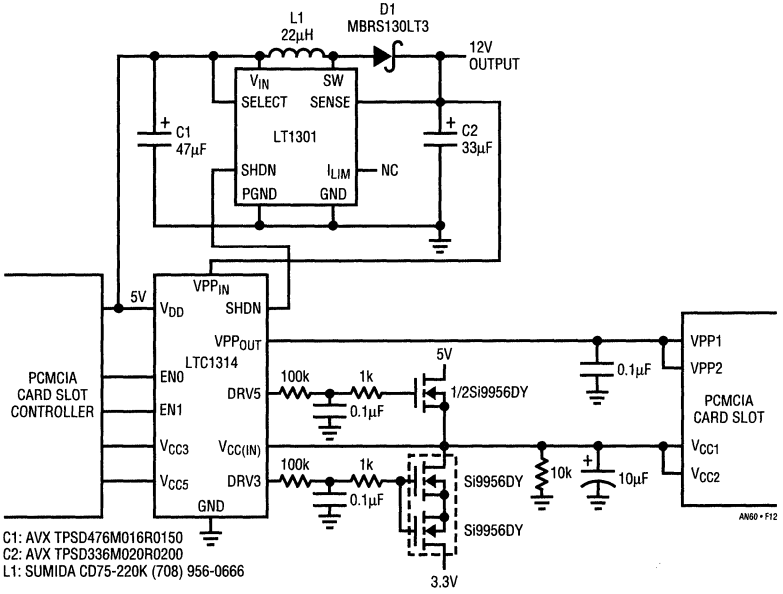


Figure 12. LTC1314 and LT1301 Configuration

Table 1. LTC1314 Truth Table

EN0	EN1	V_{CC3}	V_{CC5}	VPP_{OUT}	DRV3	DRV5
0	0	X	X	GND	X	X
0	1	X	X	$V_{CC(IN)}$	X	X
1	0	X	X	VPP_{IN}	X	X
1	1	X	X	Hi-Z	X	X
X	X	1	0	X	1	0
X	X	0	1	X	0	1
X	X	0	0	X	0	0
X	X	1	1	X	0	0

X = Don't care.

The LTC1314 drives three N-channel MOSFETs that provide V_{CC} pin power switching. On-chip charge pumps provide the necessary voltage to fully enhance the switches. With the charge pumps on-chip the MOSFET drive is available without the need for a 12V supply. This method of V_{CC} switching allows the use of fully enhanced N-channel MOSFETs for low on resistance and low cost. The LTC1314 provides a natural break-before-make action and smooth transitions due to the asymmetrical turn-on and turn-off of the MOSFETs.

The 3.3V V_{CC} switch must use two MOSFETs due to the parasitic body diode of the MOSFET. The on resistance of the 3.3V channel is still below 0.18Ω, adequate for any realistic current level. Different MOSFETs can be used for lower resistance. To limit the inrush current when charging capacitive loads, an RC network is inserted between the LTC1314 and the MOSFET's gate. This will slow the rise time down to a couple of milliseconds. Inrush current is limited only by slowing down the rise time. With a 150µF input capacitor and the 2ms rise time, the inrush current is limited to just 275mA.

The VPP switching is accomplished by a combination of the LTC1314 and LT1301 DC/DC converter. The LT1301 DC/DC converter is in shutdown mode, consuming only 10µA, to conserve power until the VPP pins require 12V. When VPP pins require 12V, the LT1301 is activated and the LTC1314's internal switches will route the VPP_{IN} pin to the VPP_{OUT} pin. The LT1301 is capable of delivering 12V at 120mA maintaining high efficiency as shown in Figure 13. As shown in Figure 14, the LTC1314's break-before-make and slope-controlled switching will ensure that the

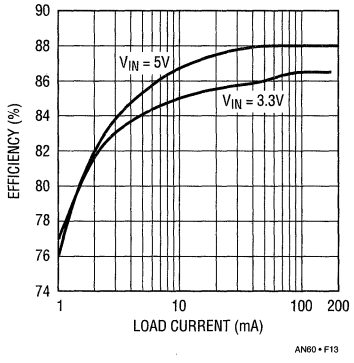


Figure 13. 12V Efficiency of LT1301

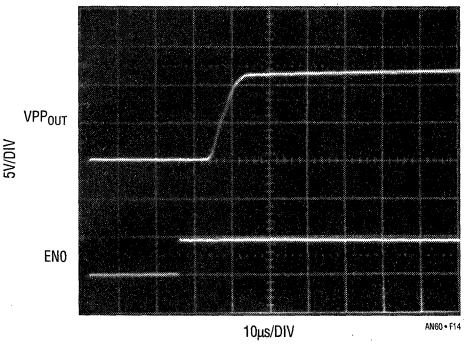


Figure 14. LTC1314/LT1301 VPP Switching Waveform

output voltage transition will be smooth, of moderate slope, and without overshoot. This is critical for flash memory products to prevent damaging parts from overshoot and ringing exceeding the 14V part limit.

The LTC1314's VPP_{IN} pin may be connected directly to a stable 12V supply. However, this should be done with caution. The 12V supply available with most computer systems has an excessive voltage tolerance and is accompanied by significant digital switching noise. The specification for flash memory requires 12V ±5%. Voltages greater than 14V will result in damaged memory devices. When using a general purpose 12V supply, make certain that you meet these criteria to ensure a safe, robust system.

The major characteristics of the previous designs that are missing are current limiting and thermal shutdown. The low cost approach does not have these features and is susceptible to short-circuit connections at the pins and excessive inrush current if extremely large capacitive loads are experienced. This may be acceptable in some systems if the main supply is carefully current limited to maintain operation or if some other form of protection is added. Care should be exercised when allowing exposed external pin connections to go without short-circuit protection.

The LTC1314 with Higher Voltage Supplies Available

Often systems have an available supply voltage greater than 12V. The LTC1314 can be used in conjunction with the LT1121 linear regulator to supply the PC card socket with all necessary voltages. Figure 15 shows this circuit. The LTC1314 will enable the LT1121 linear regulator only when 12V is required at the VPP pin. In all other modes the LT1121 is in shutdown mode and consumes only 16µA. This LT1121 also provides thermal and current limiting features to increase the robustness of the socket. This configuration can be used in conjunction with the LTC1142 auxiliary winding techniques shown earlier to provide a current limited, protected solution.

LTC1315 Dual Switch Driver and VPP Switch Matrix

For applications requiring two PC card sockets the LTC1315 provides a single package switch matrix solution. The LTC1315 is a dual version of the LTC1314 with two complete "A" and "B" sections and operates in a similar fashion. Figure 16 shows a typical circuit utilizing the LT1301 to derive 12V from the 5V line. For maximum efficiency, the ASHDN and BSHDN signals are diode OR'd to enable the LT1301 only when 12V VPP is required.

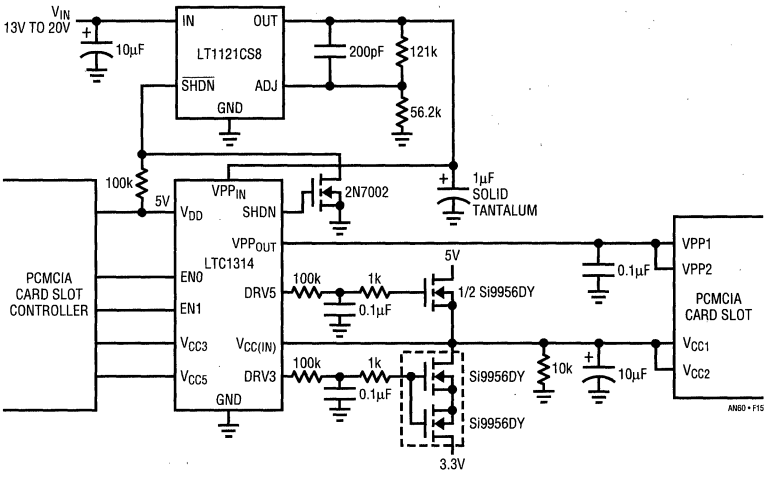


Figure 15. LTC1314 with the LT1121 Linear Regulator

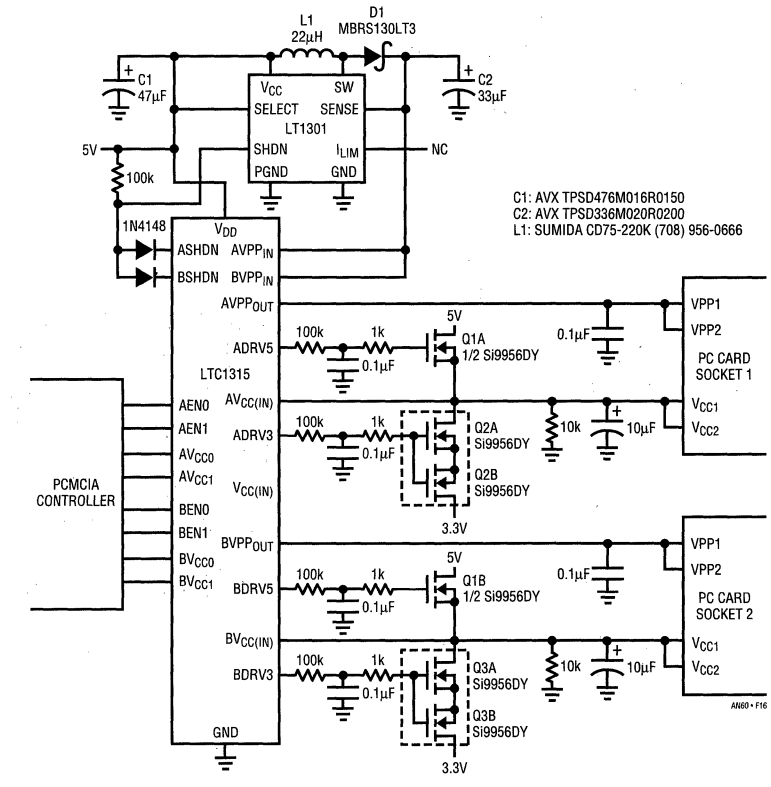


Figure 16. Typical Two-Socket Application Using the LT1315 and the LT1301

THE OTHER SIDE OF THE FENCE: PC CARD ON-CARD POWER MANAGEMENT

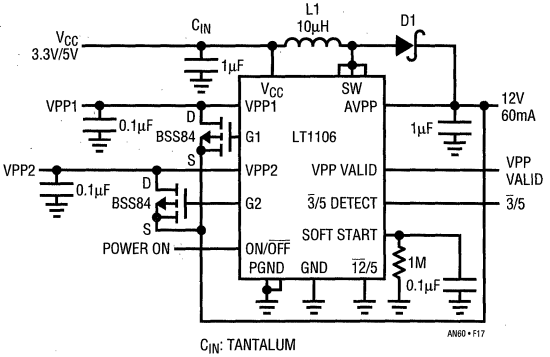
Designers of PC cards may want to have greater control of the power management and not be at the mercy of the socket's provisions. Many sockets do not support all of the voltages that the PCMCIA standard outlines or may not be able to meet the card's current demands. In addition, not all PCMCIA sockets will incorporate smooth voltage transitions thus damaging PC cards. To assure maximum reliability and broad compatibility, the PC card designer can design the card for V_{CC} only operation. With the release of the new PCMCIA low voltage card specifications, cards requiring only 3.3V will become popular. This will often necessitate on-card 3.3V to 5V conversion and VPP generation.

The size constraints of PC cards make on-card power management design extremely challenging. Board "Real Estate" problems are further compounded by severe height requirements. There are few components available compatible with the Type I card's 1.19mm height requirement. Type II cards are only marginally easier at 1.752mm height for center mounted cards and 2.31mm for offset mounted cards. These dimensions are for typical applications and vary depending on board thickness and card frame.

LT1106: PC Card 3.3V/5V to 12V Converter for Flash Memory

Flash memory cards are a typical Type I and Type II PC card application. The PC card socket should provide the necessary VPP 12V programming voltage. Card designers often prefer to have this critical voltage under their own control. The LT1106 is a switching regulator in the ultra-thin 20 pin TSSOP package designed specifically for use in PC cards. Figure 17 shows a typical application of the LT1106 as a boost regulator from 3.3V or 5V to 12V at 60mA.

The LT1106 combines an efficient switching regulator with many special PCMCIA interface features. On-chip comparators sense the socket VPP pins. If 12V is present, internal drivers enhance the P-channel MOSFET switches, Q1 and Q2, and the LT1106 goes into a low power mode (350µA). The LT1106 also produces a VPP valid signal when the voltage at the AVPP pin is greater than 11.5V to indicate that a valid programming voltage is available. An additional comparator output indicates whether the V_{CC} supply is 3.3V or 5V. The LT1106 is also selectable to produce 5V or 12V and has a shutdown pin to reduce supply current to only 10µA. The Soft Start pin controls the rise time of the output by a single resistor and capacitor.



C_{IN}: TANTALUM

FOR TYPE I CARDS (1.19mm MAX HEIGHT)
L1: COILTRONICS CTX02-11238 (407) 241-7876
OR DALE ILS-2538-10 (605) 665-9301
D1: PHILIPS BAT54C (4 IN PARALLEL)

FOR TYPE II CARDS (2.2mm MAX HEIGHT)
L1: MURATA ERIE LQH3C100K04M00
D1: PHILIPS PRLL5818 OR MOTOROLA MBR0530

Figure 17. Typical LT1106 Application

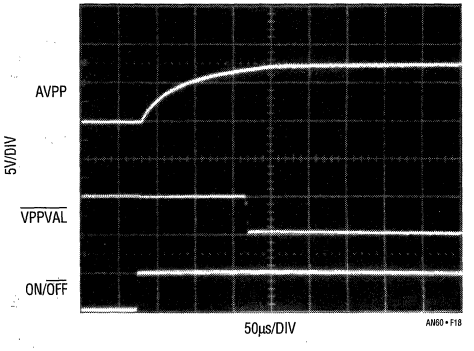


Figure 18. LT1106 VPP Switching Waveform

In Figure 18 the output voltage transition is smooth with no overshoot and ringing. This type of response assures the reliability of flash memory products.

Important performance features, in addition to the thin TSSOP package of the LT1106, make the part ideal for PC card applications. The 500kHz switching frequency allows the use of a small value, small size inductor. Small inductors in an ultra-thin form factor, critical for Type I and Type II PC card applications are achievable. The LT1106 has been designed to require only 1µF input and output capacitance. The LT1106 also features Burst Mode operation with efficiency as high as 85% to minimize battery drain and any on-card thermal issues.

Inductor, diode, and capacitor selection are critical to achieving good regulation and high efficiency at the output currents desired. The LT1106 circuit (Figure 17) requires a 10µH inductor. This inductor must not saturate at the LT1106's rated current, must have low DC resistance, and its inductance as a function of frequency must be relatively constant up to the 500kHz oscillator frequency. The combination of characteristics makes the inductor design formidable. There are several acceptable inductors listed in Figure 17.

The diode selection criteria are also difficult to meet. The diode must switch quickly, have low leakage and have a low forward voltage drop. The switching speed requirement is due primarily to the LT1106's 500kHz oscillator and the low forward voltage drop of the part is necessary to achieve good efficiency. At the time of this writing there is no diode that will satisfy this requirement in a package less than 1.19mm in height necessary for Type I cards. There are several SOT-23 packaged, fast switching diodes that can be paralleled to share the current requirements and therefore run at a lower forward voltage drop. The BAT54C Schottky diode from Philips is a dual diode in the SOT-23 package that is a solution to this problem. The circuit in Figure 17 uses four of these packages (eight diodes) in parallel to get the forward voltage drop down to 530mV at 600mA.

Capacitor selection is also critical. The capacitors must be sufficient in value with an ESR below 0.5Ω to assure good efficiency and output ripple values. The small 1µF output capacitor value allows the use of ceramic capacitors. Thin surface mount ceramic capacitors are readily available. Paralleling ten 0.1µF capacitors, often used to decouple ICs, yields a cost effective solution.

Figure 19 shows the efficiency of the LT1106 when producing 12V at various current levels. You can see how the selection of the passive components affects the efficiency of the regulator. The dashed lines represent the 12V converter made with the ultra-thin Type I card components and shows good efficiency above 80% for most current ranges. The larger Type II components allow the same circuit topology to produce 2% to 3% better efficiency.

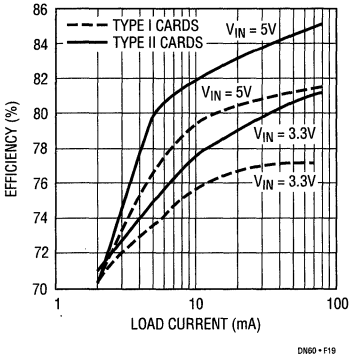
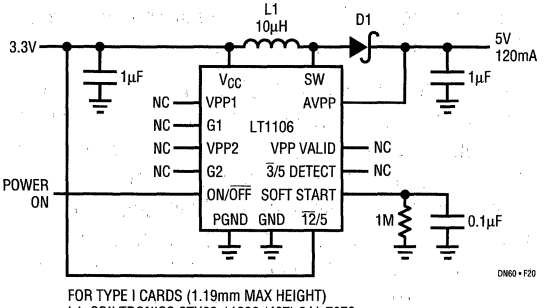


Figure 19. 12V Output Efficiency

LT1106 3.3V to 5V DC/DC Converter for Type I Cards

The LT1106 has an output voltage select pin for 12V output or 5V output. Connecting this pin to the 3.3V input will program the LT1106 for 5V output. Utilizing the same components as the 12V output design, this circuit will provide 5V at up to 120mA output current. For maximum efficiency, the ON/OFF control allows the device to be activated only when required. Figure 20 shows a typical

application. The LT1106's higher frequency operation allows for smaller components making it an ideal part for on-card DC/DC regulation. The typical efficiency is plotted in Figure 21.



FOR TYPE I CARDS (1.19mm MAX HEIGHT)
L1: COILTRONICS CTX02-11238 (407) 241-7876
OR DALE ILS-2538-10 (605) 665-9310
D1: PHILIPS 4 BAT54s IN PARALLEL

Figure 20. LT1106 3.3V to 5V DC/DC Converter

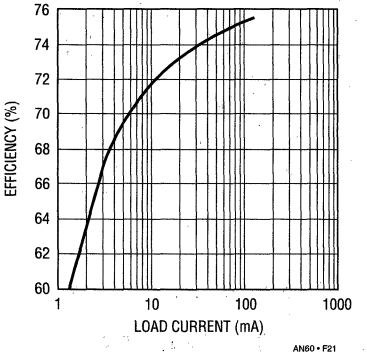
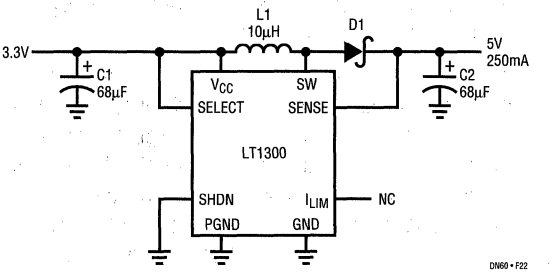


Figure 21. LT1106 3.3V to 5V Efficiency

LT1300 3.3V to 5V DC/DC Converter for Type II Cards

For PC cards requiring 3.3V to 5V conversion at more than 120mA, a design utilizing the LT1300 can provide a solution for Type II and Type III cards. While the LT1300 can deliver more current than the LT1106, it was not designed specifically for high frequency, small component operation. For this reason the inductor and capacitor values will not be as small as the LT1106 design. The LT1300's SOIC package and the use of a larger inductor with tantalum capacitors limit this design to Type II or Type III cards. Figure 22 shows a typical circuit utilizing the LT1300 to deliver 5V at 250mA from a 3.3V input. While the passive devices are not as thin as those used with the LT1106, the parts specified are much thinner than those used in conventional designs with a more standard height requirement. Figure 23 shows the typical efficiency of this design.



C1, C2: SPRAGUE 592D686X0010R2T, 68µF, 10V, (1.5mm MAX HEIGHT)
D1: MOTOROLA MBR0530 (1.35mm MAX HEIGHT)
L1: MURATA ERIE LQH3C220K04, 22µH, 2 IN PARALLEL (2.2mm MAX HEIGHT) OR SUMIDA CLS62-100L, 10µH, (2.5mm MAX HEIGHT)

Figure 22. LT1300 3.3V to 5V Converter for Type II or Type III Cards

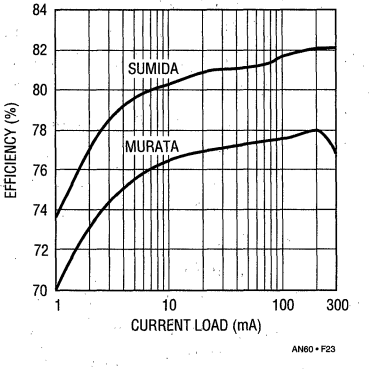


Figure 23. LT1300 3.3V to 5V Efficiency

CONCLUSION

PCMCIA expansion sockets are becoming more popular with portable equipment. The expansion sockets are also being used in desktop systems and other systems that require easy expandability. The PCMCIA specification gives a set of guidelines that form a good starting point for the design of any portable system. There are a host of other practical design issues to consider for a robust system. The main issues are switch on-resistance, inrush current, short-circuit protection and switch output ringing during switching. The main features to look for in the switch matrix are easy interface to standard controllers, low enough on-resistance, slowed switch rise times, and current limiting and thermal shutdown. By designing with these features the PCMCIA socket will meet the voltage requirements of all cards and will ensure a reliable system with a satisfied customer.

On-card power management can take many forms. Conversion from 3.3V or 5V to other voltages, both positive negative, can be achieved through careful design and component selection. The specific voltage requirements will be as varied as the wide diversity of PC card products themselves. For solutions to your specific needs, call Linear Technology for applications assistance.

Notes

Application Note 61
August 1994

Practical Circuitry for Measurement and Control Problems

Circuits Designed for a Cruel and Unyielding World

Jim Williams

INTRODUCTION

This collection of circuits was worked out between June 1991 and July of 1994. Most were designed at customer request or are derivatives of such efforts. All represent substantial effort and, as such, are disseminated here for wider study and (hopefully) use.[1] The examples are roughly arranged in categories including power conversion, transducer signal conditioning, amplifiers and signal generators. As always, reader comment and questions concerning variants of the circuits shown may be addressed directly to the author.

Clock Synchronized Switching Regulator

Gated oscillator type switching regulators permit high efficiency over extended ranges of output current. These regulators achieve this desirable characteristic by using a gated oscillator architecture instead of a clocked pulse width modulator. This eliminates the "housekeeping" currents associated with the continuous operation of fixed frequency designs. Gated oscillator regulators simply self-clock at whatever frequency is required to maintain the output voltage. Typically, loop oscillation frequency ranges from a few hertz into the kilohertz region, depending upon the load.

In most cases this asynchronous, variable frequency operation does not create problems. Some systems, however, are sensitive to this characteristic. Figure 1 slightly modifies a gated oscillator type switching regulator by synchronizing its loop oscillation frequency to the systems clock. In this fashion the oscillation frequency and its attendant switching noise, albeit variable, become coherent with system operation.

Note 1: "Study" is certainly a noble pursuit but we never fail to emphasize use.

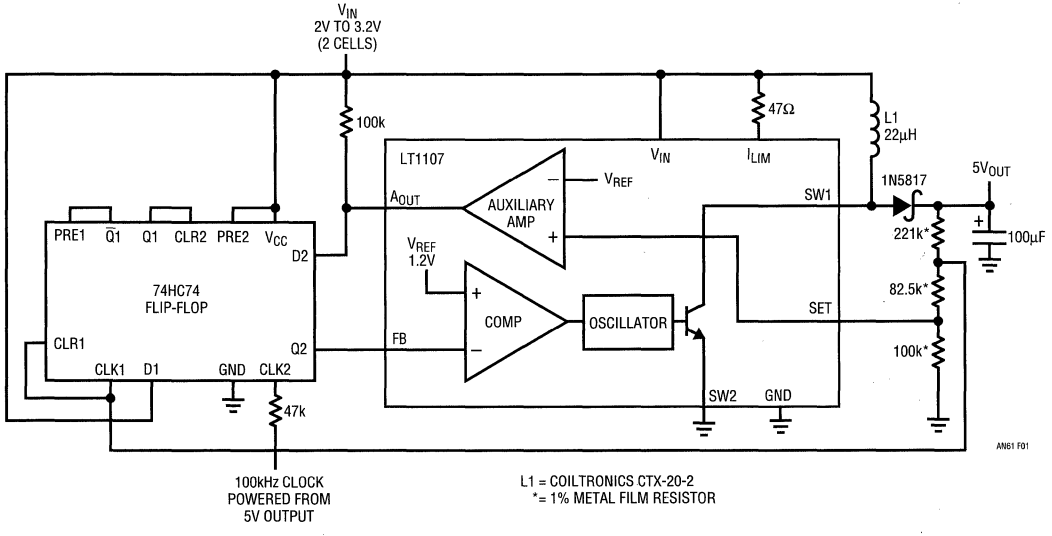


Figure 1. A Synchronizing Flip-Flop Forces Switching Regulator Noise to Be Coherent with the Clock

Circuit operation is best understood by temporarily ignoring the flip-flop and assuming the LT1107 regulator's A_{OUT} and FB pins are connected. When the output voltage decays the set pin drops below V_{REF}, causing A_{OUT} to fall. This causes the internal comparator to switch high, biasing the oscillator and output transistor into conduction. L1 receives pulsed drive, and its flyback events are deposited into the 100µF capacitor via the diode, restoring output voltage. This overdrives the set pin, causing the IC to switch off until another cycle is required. The frequency of this oscillatory cycle is load dependent and variable. If, as shown, a flip-flop is interposed in the A_{OUT}-FB pin path, synchronization to a system clock results. When the output decays far enough (trace A, Figure 2) the A_{OUT} pin (trace B) goes low. At the next clock pulse (trace C) the flip-flop Q2 output (trace D) sets low, biasing the comparator-oscillator. This turns on the power switch (V_{SW} pin is trace E), which pulses L1. L1 responds in flyback fashion, depositing its energy into the output capacitor to maintain output voltage. This operation is similar to the previously described case, except that the sequence is forced to synchronize with the system clock by the flip-flops action. Although the resulting loops oscillation frequency is variable it, and all attendant switching noise, is synchronous and coherent with the system clock.

A start-up sequence is required because this circuit's clock is powered from its output. The start-up circuitry was developed by Sean Gold and Steve Pietkiewicz of LTC. The flip-flop's remaining section is connected as a buffer.

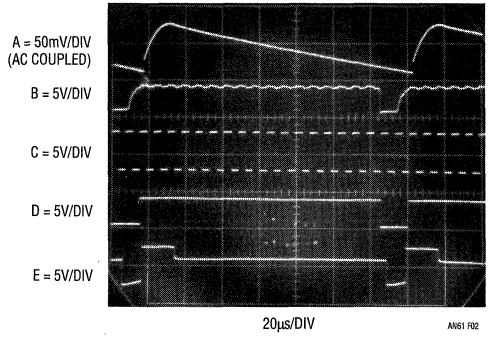


Figure 2. Waveforms for the Clock Synchronized Switching Regulator. Regulator Only Switches (Trace E) on Clock Transitions (Trace C), Resulting in Clock Coherent Output Noise (Trace A)

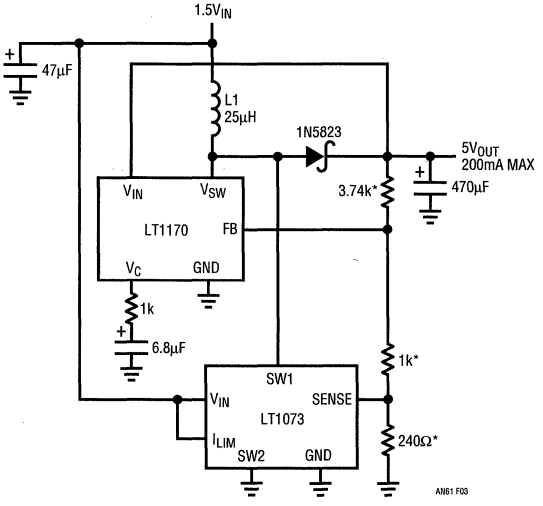
The CLR1-CLK1 line monitors output voltage via the resistor string. When power is applied Q1 sets CLR2 low. This permits the LT1107 to switch, raising output voltage. When the output goes high enough Q1 sets CLR2 high and normal loop operation commences.

The circuit shown is a step-up type, although any switching regulator configuration can utilize this synchronous technique.

High Power 1.5V to 5V Converter

Some 1.5V powered systems (survival 2-way radios, remote, transducer-fed data acquisition systems, etc.) require much more power than stand-alone IC regulators can provide. Figure 3's design supplies a 5V output with 200mA capacity.

The circuit is essentially a flyback regulator. The LT1170 switching regulator's low saturation losses and ease of use permit high power operation and design simplicity. Unfortunately this device has a 3V minimum supply requirement. Bootstrapping its supply pin from the 5V output is possible, but requires some form of start-up



L1 = PULSE ENGINEERING #PE-92100
* = 1% METAL FILM RESISTOR

Figure 3. 200mA Output 1.5V to 5V Converter. Lower Voltage LT1073 Provides Bootstrap Start-Up for LT1170 High Power Switching Regulator

mechanism. The 1.5V powered LT1073 switching regulator forms a start-up loop. When power is applied the LT1073 runs, causing its V_{SW} pin to periodically pull current through L1. L1 responds with high voltage flyback events. These events are rectified and stored in the 470µF capacitor, producing the circuits DC output. The output divider string is set up so the LT1073 turns off when circuit output crosses about 4.5V. Under these conditions the LT1073 obviously can no longer drive L1, but the LT1170 can. When the start-up circuit goes off, the LT1170 V_{IN} pin has adequate supply voltage and can operate. There is some overlap between start-up loop turn-off and LT1170 turn-on, but it has no detrimental effect.

The start-up loop must function over a wide range of loads and battery voltages. Start-up currents approach 1A, necessitating attention to the LT1073's saturation and drive characteristics. The worst case is a nearly depleted battery and heavy output loading.

Figure 4 plots input-output characteristics for the circuit. Note that the circuit will start into all loads with V_{BAT} = 1.2V. Start-up is possible down to 1.0V at reduced loads. Once the circuit has started, the plot shows it will drive full 200mA loads down to V_{BAT} = 1.0V. Reduced drive is possible down to V_{BAT} = 0.6V (a very dead battery)! Figure 5 graphs efficiency at two supply voltages over a range of output currents. Performance is attractive, although at lower currents circuit quiescent power degrades efficiency. Fixed junction saturation losses are responsible for lower overall efficiency at the lower supply voltage.

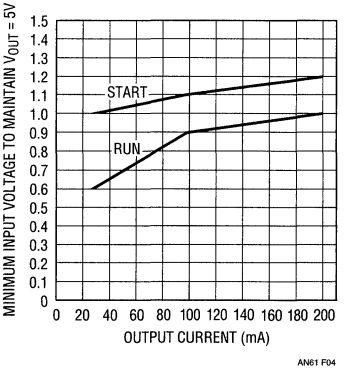


Figure 4. Input-Output Data for the 1.5V to 5V Converter Shows Extremely Wide Start-Up and Running Range into Full Load

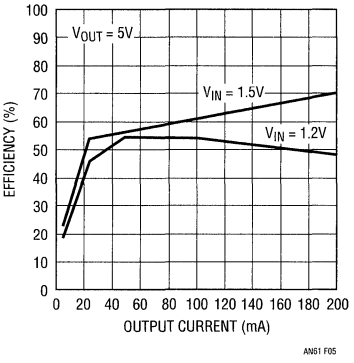


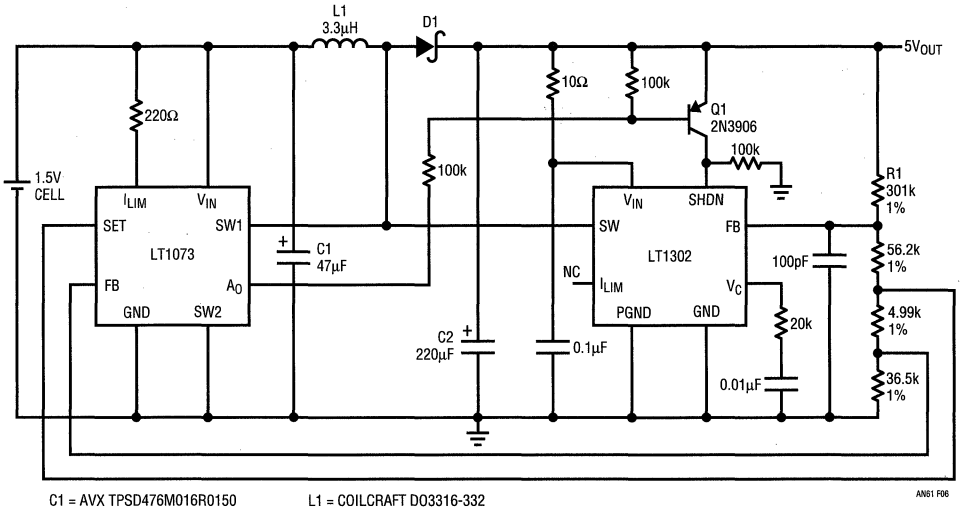
Figure 5. Efficiency vs Operating Point for the 1.5V to 5V Converter. Efficiency Suffers at Low Power Because of Relatively High Quiescent Currents

Low Power 1.5V to 5V Converter

Figure 6, essentially the same approach as the preceding circuit, was developed by Steve Pietkiewicz of LTC. It is limited to about 150mA output with commensurate restrictions on start-up current. It's advantage, good efficiency at relatively low output currents, derives from its low quiescent power consumption.

The LT1073 provides circuit start-up. When output voltage, sensed by the LT1073's "set" input via the resistor divider, rises high enough Q1 turns on, enabling the LT1302. This device sees adequate operating voltage and responds by driving the output to 5V, satisfying its feedback node. The 5V output also causes enough overdrive at the LT1073 feedback pin to shut the device down.

Figure 7 shows maximum permissible load currents for start-up and running conditions. Performance is quite good, although the circuit clearly cannot compete with the previous design. The fundamental difference between the two circuits is the LT1170's (Figure 3) much larger power switch, which is responsible for the higher available power. Figure 8, however, reveals another difference. The curves show that Figure 6 is significantly more efficient than the LT1170 based approach at output currents below 100mA. This highly desirable characteristic is due to the LT1302's much lower quiescent operating currents.



C1 = AVX TPSD476M016R0150
C2 = AVX TPSE227M010R0100

L1 = COILCRAFT DO3316-332
D1 = MOTOROLA MBR3130LT3

Figure 6. Single-Cell to 5V Converter Delivers 150mA with Good Efficiency at Lower Currents

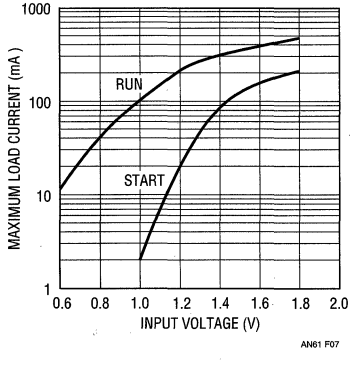


Figure 7. Maximum Permissible Loads for Start-Up and Running Conditions. Allowable Load Current During Start-Up Is Substantially Less Than Maximum Running Current.

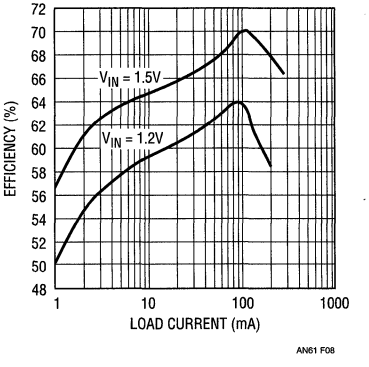


Figure 8. Efficiency Plot for Figure 6. Performance Is Better Than the Previous Circuit at Lower Currents, Although Poorer at High Power

Low Power, Low Voltage Cold Cathode Fluorescent Lamp Power Supply

Most Cold Cathode Fluorescent Lamp (CCFL) circuits require an input supply of 5V to 30V and are optimized for bulb currents of 5mA or more. This precludes lower power operation from 2- or 3-cell batteries often used in palmtop computers and portable apparatus. A CCFL power supply that operates from 2V to 6V is detailed in Figure 9. This circuit, contributed by Steve Pietkiewicz of LTC, can drive a small CCFL over a 100µA to 2mA range.

The circuit uses an LT1301 micropower DC/DC converter IC in conjunction with a current driven Royer class converter comprised of T1, Q1 and Q2. When power and intensity adjust voltage are applied the LT1301's I_{LIM} pin is driven slightly positive, causing maximum switching current through the IC's internal switch pin (SW). Current flows from T1's center tap, through the transistors, into L1. L1's current is deposited in switched fashion to ground by the regulator's action.

The Royer converter oscillates at a frequency primarily set by T1's characteristics (including its load) and the 0.068µF capacitor. LT1301 driven L1 sets the magnitude of the Q1-Q2 tail current, hence T1's drive level. The 1N5817 diode maintains L1's current flow when the LT1301's switch is off. The 0.068µF capacitor combines with T1's characteristics to produce sine wave voltage drive at the Q1 and Q2 collectors. T1 furnishes voltage step-up and about 1400Vp-p appears at its secondary. Alternating current flows through the 22pF capacitor into the lamp. On positive half-cycles the lamp's current is steered to ground via D1. On negative half-cycles the lamp's current flows through Q3's collector and is filtered by C1. The LT1301's I_{LIM} pin acts as a 0V summing point with about 25µA bias current flowing out of the pin into C1. The LT1301 regulates L1's current to equalize Q3's average collector current, representing 1/2 the lamp current, and R1's current, represented by V_A/R1. C1 smooths all current flow to DC. When V_A is set to zero, the I_{LIM} pin's bias current forces about 100µA bulb current.

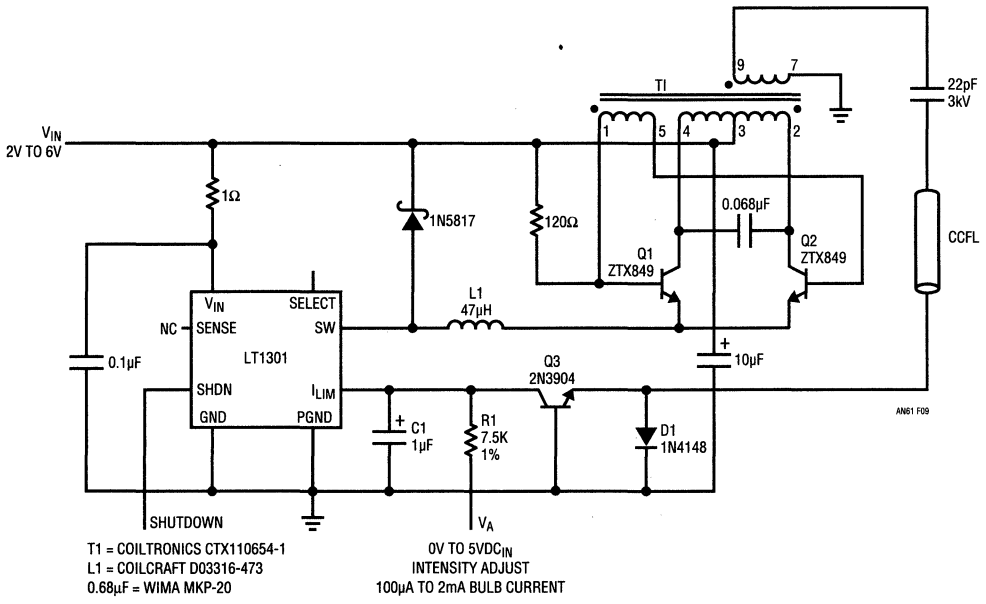


Figure 9. Low Power Cold Cathode Fluorescent Lamp Supply Is Optimized for Low Voltage Inputs and Small Lamps

Circuit efficiency ranges from 80% to 88% at full load, depending on line voltage. Current mode operation combined with the Royer's consistent waveshape vs input results in excellent line rejection. The circuit has none of the line rejection problems attributable to the hysteretic voltage control loops typically found in low voltage micropower DC/DC converters. This is an especially desirable characteristic for CCFL control, where lamp intensity must remain constant with shifts in line voltage. Interaction between the Royer converter, the lamp and the regulation loop is far more complex than might be supposed, and subject to a variety of considerations. For detailed discussion see Reference 3.

Low Voltage Powered LCD Contrast Supply

Figure 10, a companion to the CCFL power supply previously described, is a contrast supply for LCD panels. It was designed by Steve Pietkiewicz of LTC. The circuit is noteworthy because it operates from a 1.8V to 6V input, significantly lower than most designs. In operation the LT1300/LT1301 switching regulator drives T1 in flyback fashion, causing negative biased step-up at T1's secondary. D1 provides rectification, and C1 smooths the output to DC. The resistively divided output is compared to a command input, which may be DC or PWM, by the IC's "I_{LIM}" pin. The IC, forcing the loop to maintain 0V at the I_{LIM} pin, regulates circuit output in proportion to the command input.

Efficiency ranges from 77% to 83% as supply voltage varies from 1.8V to 3V. At the same supply limits, available output current increases from 12mA to 25mA.

HeNe Laser Power Supply

Helium-Neon lasers, used for a variety of tasks, are difficult loads for a power supply. They typically need almost 10kV to start conduction, although they require only about 1500V to maintain conduction at their specified operating currents. Powering a laser usually involves some form of start-up circuitry to generate the initial breakdown voltage and a separate supply for sustaining conduction. Figure 11's circuit considerably simplifies driving the laser. The

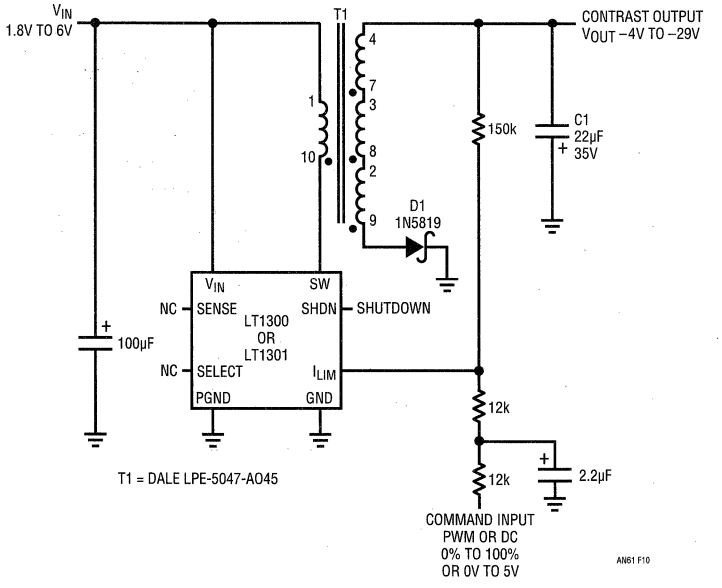
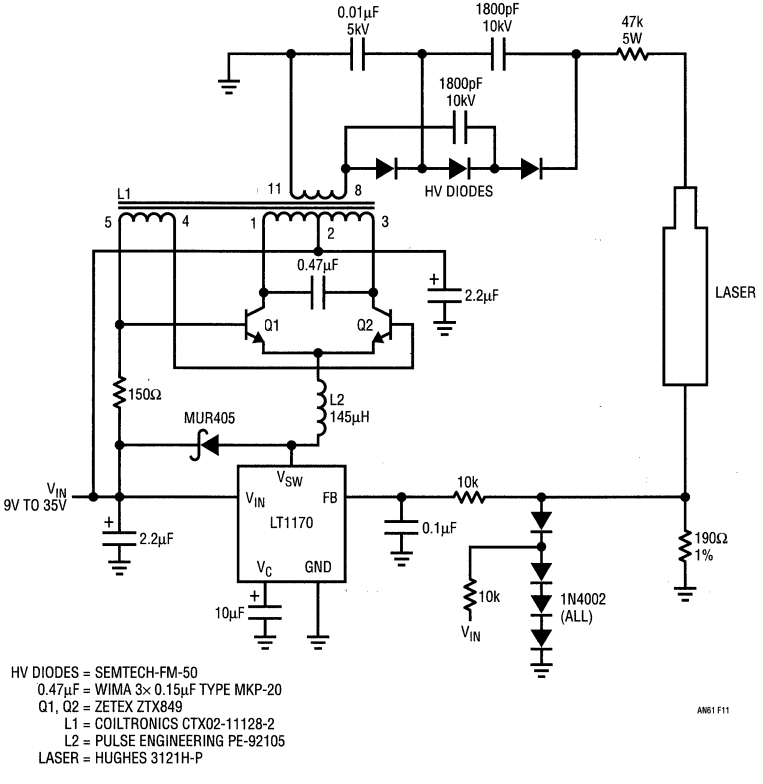


Figure 10. Liquid Crystal Display Contrast Supply Operates from 1.8V to 6V with –4V to –29V Output Range

start-up and sustaining functions have been combined into a single, closed-loop current source with over 10kV of compliance. The circuit is recognizable as a reworked CCFL power supply with a voltage tripled DC output.[2]

When power is applied, the laser does not conduct and the voltage across the 190Ω resistor is zero. The LT1170 switching regulator FB pin sees no feedback voltage, and its switch pin (V_{SW}) provides full duty cycle pulse width modulation to L2. Current flows from L1's center tap through Q1 and Q2 into L2 and the LT1170. This current flow causes Q1 and Q2 to switch, alternately driving L1. The 0.47µF capacitor resonates with L1, providing boosted sine wave drive. L1 provides substantial step-up, causing about 3500V to appear at its secondary. The capacitors and diodes associated with L1's secondary form a voltage tripler, producing over 10kV across the laser. The laser breaks down and current begins to flow through it. The 47k resistor limits current and isolates the laser's load characteristic. The current flow causes a voltage to appear across the 190Ω resistor. A filtered version of this voltage appears at the LT1170 FB pin, closing a control loop. The LT1170 adjusts pulse width drive to L2 to maintain the FB pin at 1.23V, regardless of changes in operating conditions. In this fashion, the laser sees constant current drive,

Note 2: See References 2 and 3 and this text's Figure 9.



HV DIODES = SEMTECH-FM-50
0.47µF = WIMA 3× 0.15µF TYPE MKP-20
Q1, Q2 = ZETEX ZTX849
L1 = COILTRONICS CTX02-11128-2
L2 = PULSE ENGINEERING PE-92105
LASER = HUGHES 3121H-P

Figure 11. LASER Power Supply Is Essentially A 10,000V Compliance Current Source

in this case 6.5mA. Other currents are obtainable by varying the 190Ω value. The 1N4002 diode string clamps excessive voltages when laser conduction first begins, protecting the LT1170. The 10µF capacitor at the V_C pin frequency compensates the loop and the MUR405 maintains L1's current flow when the LT1170 V_{SW} pin is not conducting. The circuit will start and run the laser over a 9V to 35V input range with an electrical efficiency of about 80%.

Compact Electroluminescent Panel Power Supply

Electroluminescent (EL) panel LCD backlighting presents an attractive alternative to fluorescent tube (CCFL) backlighting in some portable systems. EL panels are thin, lightweight, lower power, require no diffuser and work at lower voltage than CCFLs. Unfortunately, most EL DC/AC inverters use a large transformer to generate the 400Hz 95V square wave required to drive the panel. Figure 12's circuit, developed by Steve Pietkiewicz of LTC, eliminates the transformer by employing an LT1108 micropower DC/DC converter IC. The device generates a 95VDC potential via L1 and the diode-capacitor doubler network. The transistors switch the EL panel between 95V and ground. C1 blocks DC and R1 allows intensity adjustment. The 400Hz square wave drive signal can be supplied by the microprocessor or a simple multivibrator. When compared to conventional EL panel supplies, this circuit is noteworthy because it can be built in a square inch with a 0.5 inch height restriction. Additionally, all components are surface mount types, and the usual large and heavy 400Hz transformer is eliminated.

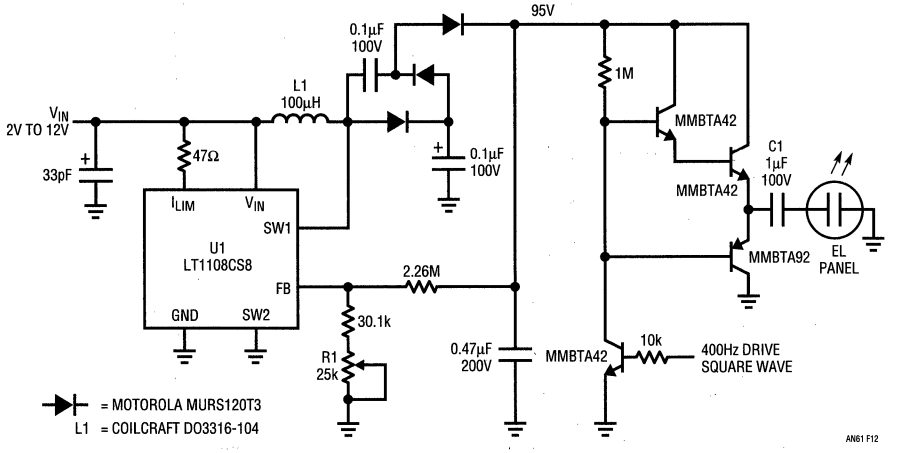


Figure 12. Switch Mode EL Panel Driver Eliminates Large 400Hz Transformer

3.3V Powered Barometric Pressure Signal Conditioner

The move to 3.3V digital supply voltage creates problems for analog signal conditioning. In particular, transducer based circuits often require higher voltage for proper transducer excitation. DC/DC converters in standard configurations can address this issue but increase power consumption. Figure 13's circuit shows a way to provide proper transducer excitation for a barometric pressure sensor while minimizing power requirements.

The 6kΩ transducer T1 requires precisely 1.5mA of excitation, necessitating a relatively high voltage drive. A1 senses T1's current by monitoring the voltage drop across the resistor string in T1's return path.

A1's output biases the LT1172 switching regulator's operating point, producing a stepped up DC voltage which appears as T1's drive and A2's supply voltage. T1's return current out of pin 6 closes a loop back at A1 which is slaved to the 1.2V reference. This arrangement provides the required high voltage drive (≈10V) while minimizing power consumption. This is so because the switching regulator produces only enough voltage to satisfy T1's current requirements. Instrumentation amplifier A2 and A3 provide gain and LTC1287 A/D converter gives a 12-bit digital output. A2 is bootstrapped off the transducer supply, enabling it to accept T1's common-mode voltage. Circuit current consumption is about 14mA. If the shutdown pin is driven high the switching regulator turns off, reducing

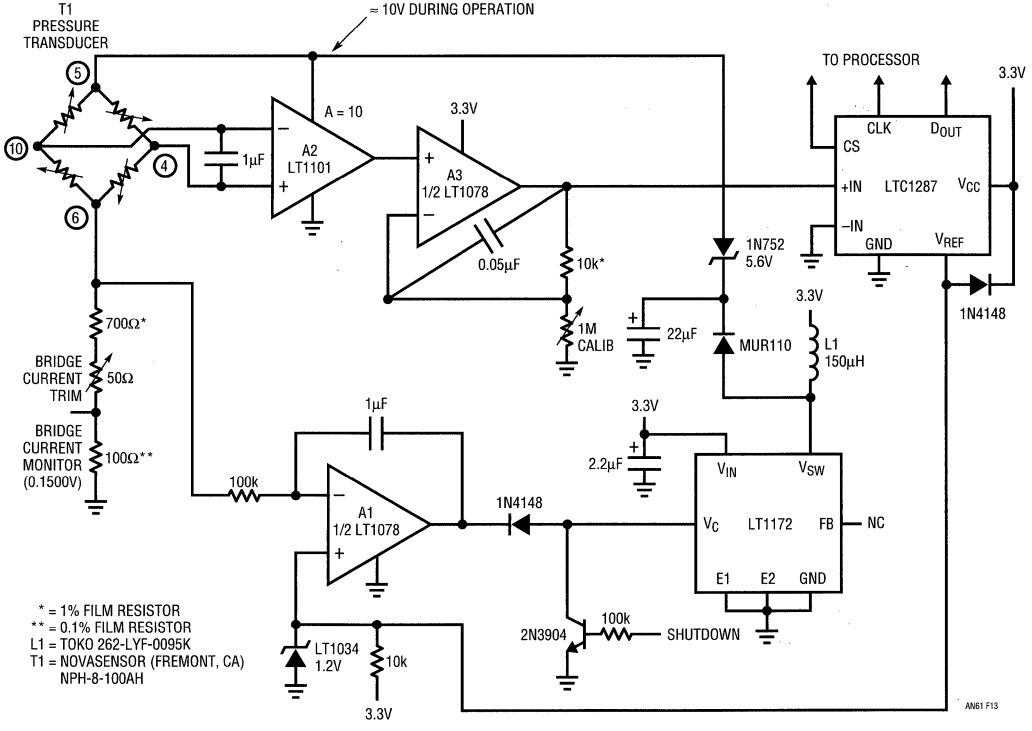


Figure 13. 3.3V Powered, Digital Output, Barometric Pressure Signal Conditioner

total power consumption to about 1mA. In shutdown the 3.3V powered A/D's output data remains valid. In practice, the circuit provides a 12-bit representation of ambient barometric pressure after calibration. To calibrate, adjust the "bridge current trim" for exactly 0.1500V at the indicated point. This sets T1's current to the manufacturers specified point. Next, adjust A3's trim so that the digital output corresponds to the known ambient barometric pressure. If a pressure standard is not available the transducer is supplied with individual calibration data, permitting circuit calibration.

Some applications may require operation over a wider supply range and/or a calibrated analog output. Figure 14's circuit is quite similar, except that the A/D converter is eliminated and a 2.7V to 7V supply is acceptable. The calibration procedure is identical, except that A3's analog output is monitored.

Single Cell Barometers

It is possible to power these circuits from a single cell without sacrificing performance. Figure 15, a direct extension of the above approaches, simply substitutes a switching regulator that will run from a single 1.5V battery. In other respects loop action is nearly identical.

Figure 16, also a 1.5V powered design, is related but eliminates the instrumentation amplifier. As before, the 6kΩ transducer T1 requires precisely 1.5mA of excitation, necessitating a relatively high voltage drive. A1's positive input senses T1's current by monitoring the voltage drop across the resistor string in T1's return path. A1's negative input is fixed by the 1.2V LT1004 reference. A1's output biases the 1.5V powered LT1110 switching regulator. The LT1110's switching produces two outputs from L1. Pin 4's rectified and filtered output powers A1 and T1. A1's

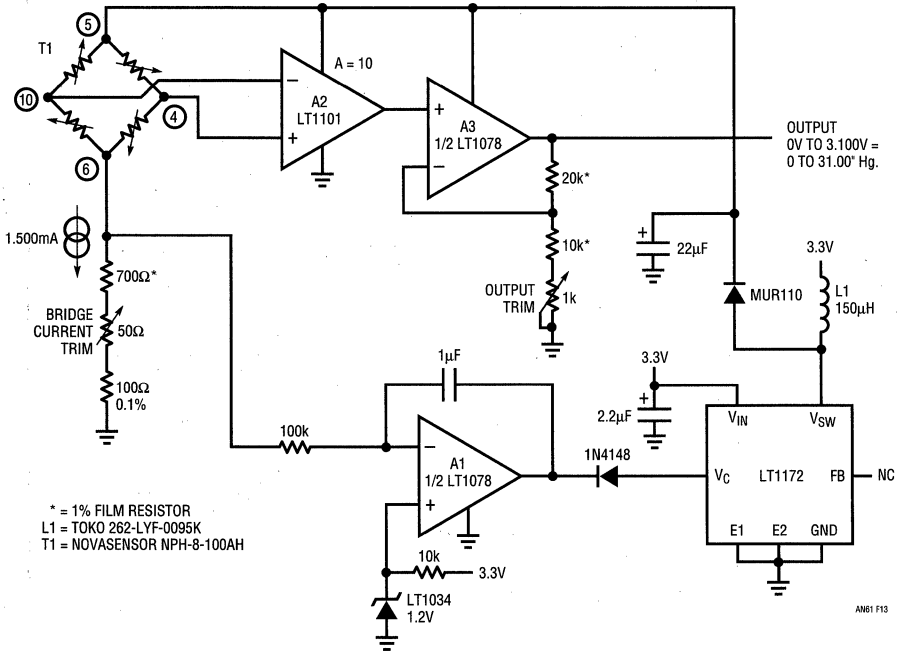


Figure 14. Single Supply Barometric Pressure Signal Conditioner Operates Over a 2.7V to 7V Range

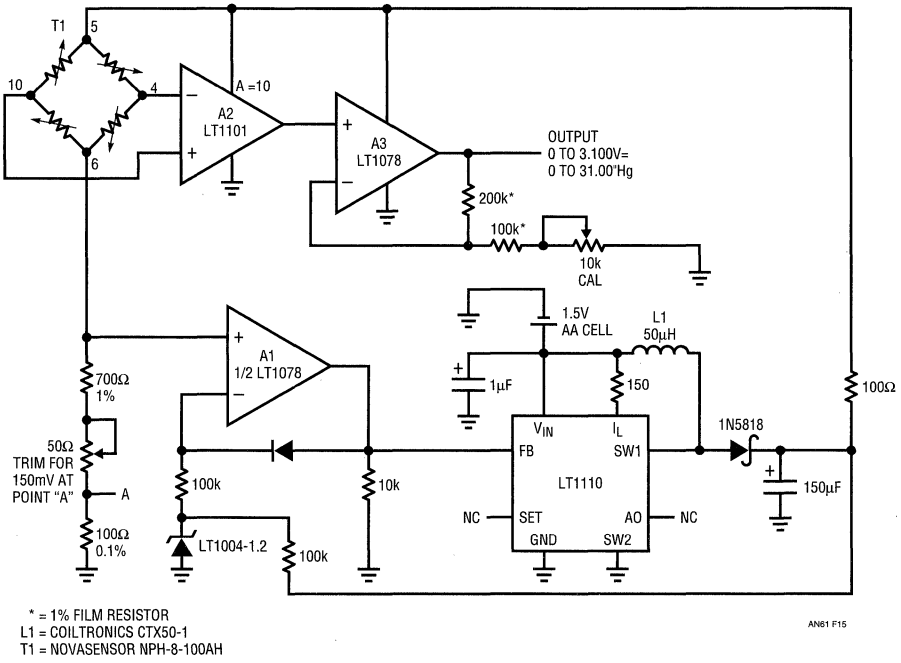


Figure 15. 1.5V Powered Barometric Pressure Signal Conditioner Uses Instrumentation Amplifier and Voltage Boosted Current Loop

output, in turn, closes a feedback loop at the regulator. This loop generates whatever voltage step-up is required to force precisely 1.5mA through T1. This arrangement provides the required high voltage drive while minimizing power consumption. This occurs because the switching regulator produces only enough voltage to satisfy T1's current requirements.

L1 pins 1 and 2 source a boosted, fully floating voltage, which is rectified and filtered. This potential powers A2. Because A2 floats with respect to T1, it can look differentially across T1's outputs, pins 10 and 4. In practice, pin 10 becomes "ground" and A2 measures pin 4's output with respect to this point. A2's gain-scaled output is the circuit's output, conveniently scaled at 3.000V = 30.00"Hg. A2's floating drive eliminates the requirement for an instrumentation amplifier, saving cost, power, space and error contribution.

To calibrate the circuit, adjust R1 for 150mV across the 100Ω resistor in T1's return path. This sets T1's current to the manufacturer's specified calibration point. Next, adjust R2 at a scale factor of 3.000V = 30.00"Hg. If R2 cannot capture the calibration, reselect the 200k resistor in series with it. If a pressure standard is not available, the transducer is supplied with individual calibration data, permitting circuit calibration.

This circuit, compared to a high-order pressure standard, maintained 0.01"Hg accuracy over months with widely varying ambient pressure shifts. Changes in pressure, particularly rapid ones, correlated quite nicely to changing weather conditions. Additionally, because 0.01"Hg corresponds to about 10 feet of altitude at sea level, driving over hills and freeway overpasses becomes quite interesting.

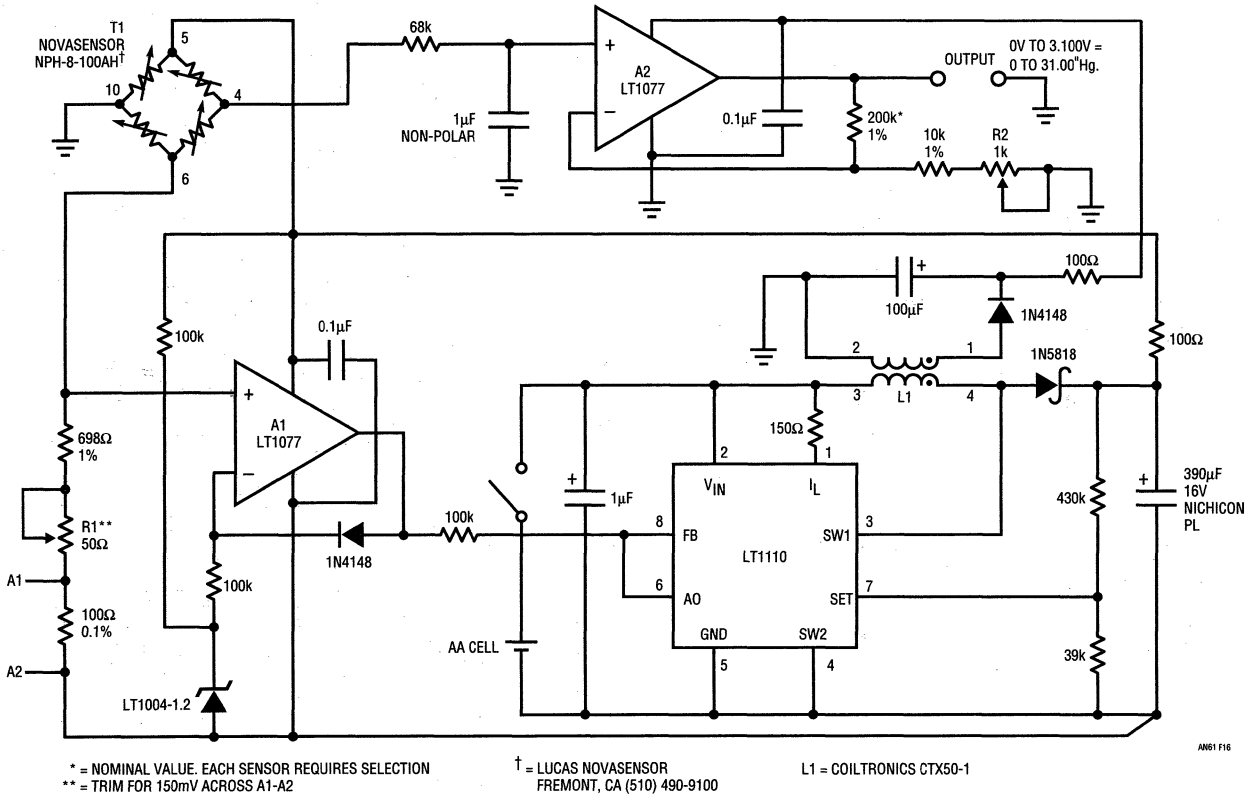


Figure 16. 1.5V Powered Barometric Pressure Signal Conditioner Floats Bridge Drive to Eliminate Instrumentation Amplifier. Voltage Boosted Current Loop Drives Transducer

Until recently, this type of accuracy and stability has only been attainable with bonded strain gauge and capacitively-based transducers, which are quite expensive. As such, semiconductor pressure transducer manufacturers whose products perform at the levels reported are to be applauded. Although high quality semiconductor transducers are still not comparable to more mature technologies, their cost is low and they are vastly improved over earlier devices.

The circuit pulls 14mA from the battery, allowing about 250 hours operation from one D cell.

Quartz Crystal-Based Thermometer

Although quartz crystals have been utilized as temperature sensors (see Reference 5), there has been almost no widespread adaptation of this technology. This is primarily due to the lack of standard product quartz-based temperature sensors. The advantages of quartz-based sensors include simple signal conditioning, good stability and a direct, noise immune digital output almost ideally suited to remote sensing.

Figure 17 utilizes an economical, commercially available (see Reference 6) quartz-based temperature sensor in a thermometer scheme suited to remote data collection.

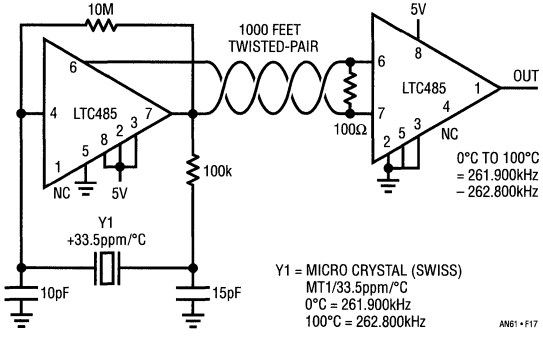


Figure 17. Quartz Crystal Based Circuit Provides Temperature-to-Frequency Conversion. RS485 Transceivers Allow Remote Sensing

The LTC485 RS485 transceiver is set up in the transmit mode. The crystal and discrete components combine with the IC's inverting gain to form a Pierce type oscillator. The LTC485's differential line driving outputs provide frequency coded temperature data to a 1000-foot cable run. A second RS485 transceiver differentially receives the data and presents a single-ended output. Accuracy depends on the grade of quartz sensor specified, with 1°C over 0°C to 100°C achievable.

Ultra-Low Noise and Low Drift Chopped-FET Amplifier

Figure 18's circuit combines the extremely low drift of a chopper-stabilized amplifier with a pair of low noise FETs. The result is an amplifier with 0.05μV/°C drift, offset within 5μV, 100pA bias current and 50nV noise in a 0.1Hz to 10Hz bandwidth. The noise performance is especially noteworthy; it is almost 35 times better than monolithic chopper-stabilized amplifiers and equals the best bipolar types.

FETs Q1 and Q2 differentially feed A2 to form a simple low noise op amp. Feedback, provided by R1 and R2, sets closed-loop gain (in this case 10,000) in the usual fashion. Although Q1 and Q2 have extraordinarily low noise characteristics, their offset and drift are uncontrolled. A1, a chopper-stabilized amplifier, corrects these deficiencies. It does this by measuring the difference between the amplifier's inputs and adjusting Q1's channel current via Q3 to minimize the difference. Q1's skewed drain values ensure that A1 will be able to capture the offset. A1 and Q3 supply whatever current is required into Q1's channel to force offset within 5μV. Additionally, A1's low bias current does not appreciably add to the overall 100pA amplifier bias current. As shown, the amplifier is set up for a noninverting gain of 10,000 although other gains and inverting operation are possible. Figure 19 is a plot of the measured noise performance.

The FETs' V_{GS} can vary over a 4:1 range. Because of this, they must be selected for 10% V_{GS} matching. This matching allows A1 to capture the offset without introducing any significant noise.

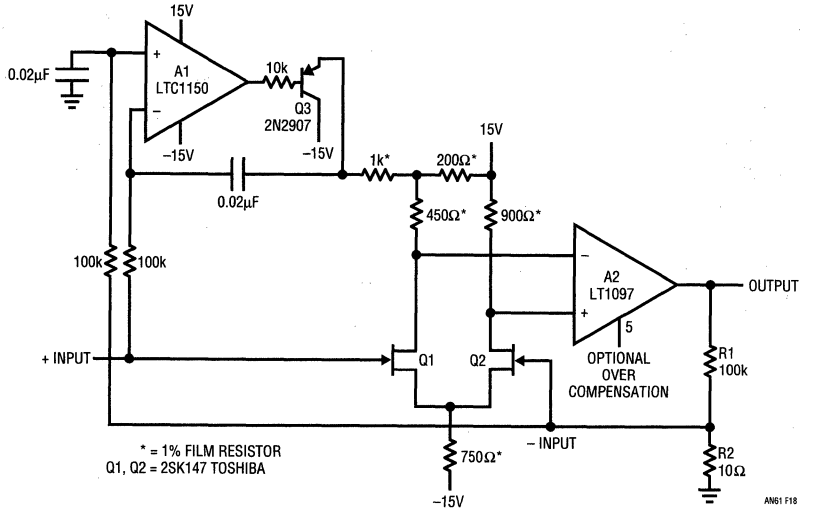


Figure 18. Chopper-Stabilized FET Pair Combines Low Bias, Offset and Drift with 45nV Noise

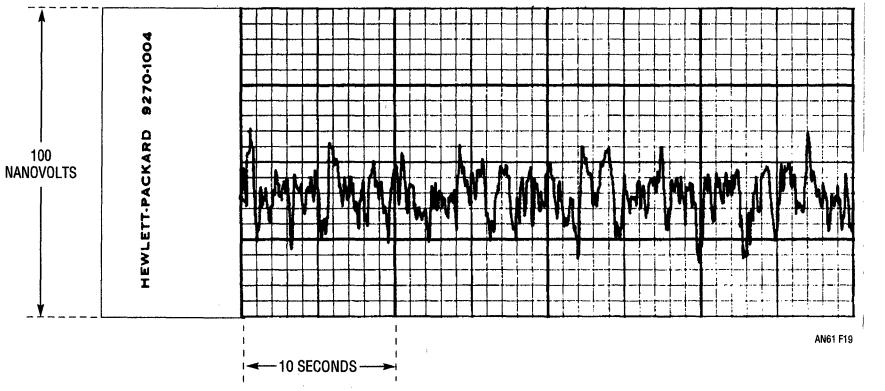


Figure 19. Figure 18's 45nV Noise Performance in a 0.1Hz to 10Hz Bandwidth. A1's Low Offset and Drift Are Retained, But Noise Is Almost 35 Times Better

Figure 20 shows the response (trace B) to a 1mV input step (trace A). The output is clean, with no overshoots or uncontrolled components. If A2 is replaced with a faster device (e.g., LT1055) speed increases by an order of magnitude with similar damping. A2's optional overcompensation can be used (capacitor to ground) to optimize response for low closed-loop gains.

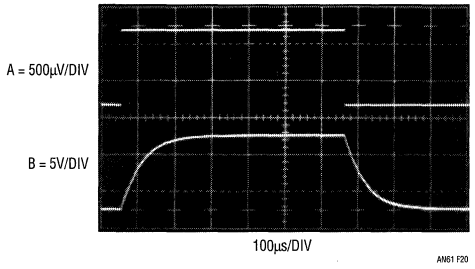


Figure 20. Step Response for the Low Noise × 10,000 Amplifier. A 10× Speed Increase Is Obtainable by Replacing A2 with a Faster Device

High Speed Adaptive Trigger Circuit

Line receivers often require an adaptive trigger to compensate for variations in signal amplitude and DC offsets. The circuit in Figure 21 triggers on 2mV to 100mV signals from 100Hz to 10MHz while operating from a single 5V rail. A1, operating at a gain of 20, provides wideband AC gain. The output of this stage biases a 2-way peak detector (Q1-Q4). The maximum peak is stored in Q2's emitter capacitor, while the minimum excursion is retained in Q4's emitter capacitor. The DC value of A1's output signal's midpoint appears at the junction of the 500pF capacitor and the 10MΩ units. This point always sits midway between the signal's excursions, regardless of absolute amplitude. This signal-adaptive voltage is buffered by A2 to set the trigger voltage at the LT1116's positive input. The LT1116's negative input is biased directly from A1's output. The LT1116's output, the circuit's output, is unaffected by 50:1 signal amplitude variations. Bandwidth limiting in A1 does not affect triggering because the adaptive trigger threshold varies ratiometrically to maintain circuit output.

Split supply versions of this circuit can achieve bandwidths to 50MHz with wider input operating range (See Reference 7).

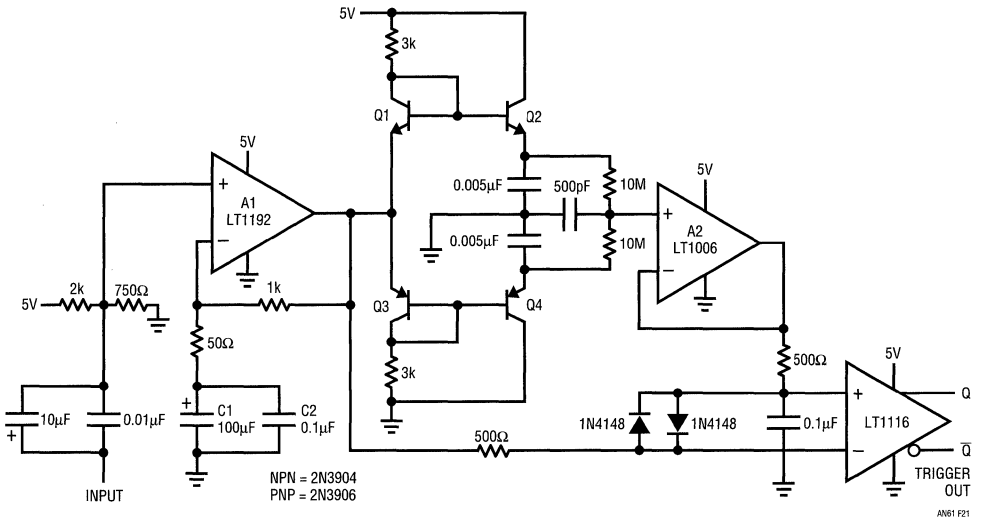


Figure 21. Fast Single Supply Adaptive Trigger. Output Comparator's Trip Level Varies Ratiometrically with Input Amplitude, Maintaining Data Integrity Over 50:1 Input Amplitude Range

Wideband, Thermally-Based RMS/DC Converter

Applications such as wideband RMS voltmeters, RF leveling loops, wideband AGC, high crest factor measurements, SCR power monitoring and high frequency noise measurements require wideband, true RMS/DC conversion. The thermal conversion method achieves vastly higher bandwidth than any other approach. Thermal RMS/DC converters are direct acting, thermoelectronic analog computers. The thermal technique is explicit, relying on "first principles," e.g,. a waveforms RMS value is defined as its heating value in a load.

Figure 22 is a wideband, thermally-based RMS/DC converter.[3] It provides a true RMS/DC conversion from DC to 10MHz with less than 1% error, regardless of input signal waveshape. It also features high input impedance and overload protection.

The circuit consists of three blocks; a wideband FET input amplifier, the RMS/DC converter and overload protection. The amplifier provides high input impedance, gain and drives the RMS/DC converters input heater. Input resistance is defined by the 1M resistor with input capacitance about 3pF. Q1 and Q2 constitute a simple, high speed FET input buffer. Q1 functions as a source follower, with the Q2 current source load setting the drain-source channel current. The LT1206 provides a flat 10MHz bandwidth gain of ten. Normally, this open-loop configuration would be quite drifty because there is no DC feedback. The LT1097 contributes this function to stabilize the circuit. It does this by comparing the filtered circuit output to a similarly filtered version of the input signal. The amplified difference between these signals is used to set Q2's bias, and hence Q1's channel current. This forces Q1's V_{GS} to whatever voltage is required to match the circuit's input and output potentials. The capacitor at A1 provides stable loop compensation. The RC network in A1's output prevents it from seeing high speed edges coupled through Q2's collector-base junction. Q4, Q5 and Q6 form a low leakage clamp which precludes A1 loop latch-up during start-up or overdrive conditions. This can occur if Q1 ever forward biases. The 5K-50pF network gives A2 a slight peaking characteristic at the highest frequencies, allowing 1% flatness to 10MHz. A2's output drives the RMS/DC converter.

The LT1088 based RMS/DC converter is made up of matched pairs of heaters and diodes and a control amplifier. The LT1206 drives R1, producing heat which lowers D1's voltage. Differentially connected A3 responds by driving R2, via Q3, to heat D2, closing a loop around the amplifier. Because the diodes and heater resistors are matched, A3's DC output is related to the RMS value of the input, regardless of input frequency or waveshape. In practice, residual LT1088 mismatches necessitate a gain trim, which is implemented at A4. A4's output is the circuit output. The LT1004 and associated components frequency compensate the loop and provide good settling time over wide ranges of operating conditions (see Footnote 3).

Start-up or input overdrive can cause A2 to deliver excessive current to the LT1088 with resultant damage. C1 and C2 prevent this. Overdrive forces D1's voltage to an abnormally low potential. C1 triggers low under these conditions, pulling C2's input low. This causes C2's output to go high, putting A2 into shutdown and terminating the overload. After a time determined by the RC at C2's input, A2 will be enabled. If the overload condition still exists the loop will almost immediately shut A2 down again. This oscillatory action will continue, protecting the LT1088 until the overload condition is removed.

Note 3: Thermally based RMS/DC conversion is detailed in Reference 9.

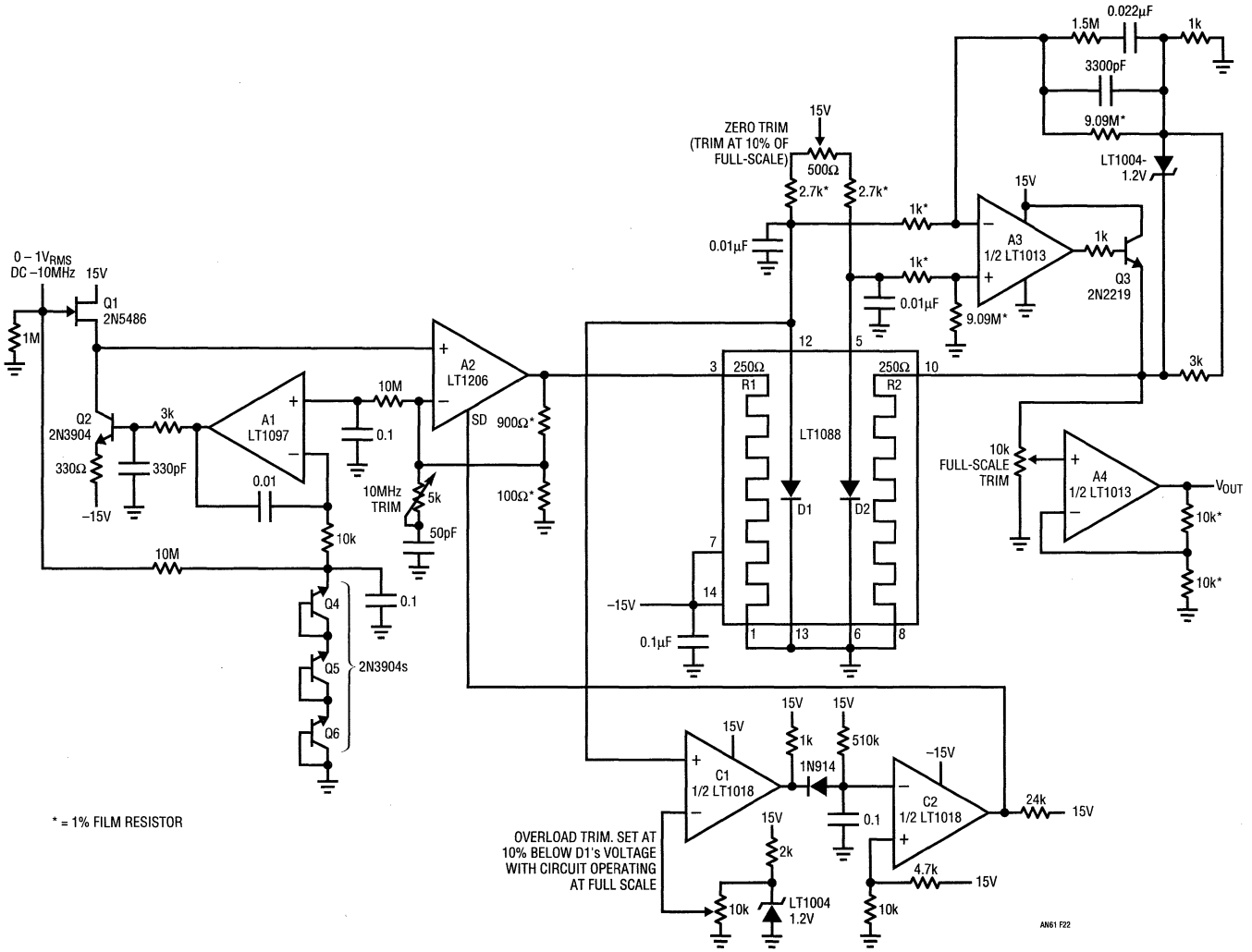


Figure 22. Complete 10MHz Thermally-Based RMS/DC Converter Has 1% Accuracy, High Input Impedance and Overload Protection

Performance for the circuit is quite impressive. Figure 23 plots error from DC to 11MHz. The graph shows 1% error bandwidth of 11MHz. The slight peaking out to 5MHz is due to the gain boost network at A2's negative input. The peaking is minimal compared to the total error envelope, and a small price to pay to get the 1% accuracy to 10MHz.

To trim this circuit put the 5kΩ potentiometer at its maximum resistance position and apply a 100 mV, 5MHz signal. Trim the 500Ω adjustment for exactly $1V_{OUT}$. Next, apply a 5MHz 1V input and trim the 10k potentiometer for $10.00V_{OUT}$. Finally, put in 1V at 10MHz and adjust the 5kΩ trimmer for $10.00V_{OUT}$. Repeat this sequence until circuit output is within 1% accuracy for DC-10MHz inputs. Two passes should be sufficient.

It is worth considering that this circuit performs the same function as instruments costing thousands of dollars.[4]

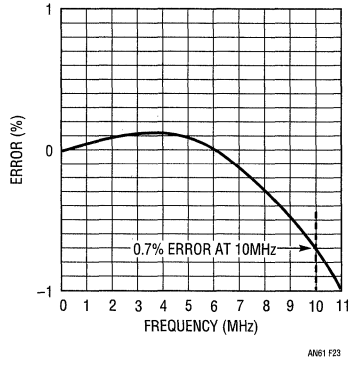


Figure 23. Error Plot for the RMS/DC Converter. Frequency Dependent Gain Boost at A2 Preserves 1% Accuracy, But Causes Slight Peaking Before Roll-Off

Hall Effect Stabilized Current Transformer

Current transformers are common and convenient. They permit wideband current measurement independent of common-mode voltage considerations. The most convenient current transformers are the "clip-on" type, commercially sold as "current probes." A problem with all simple current transformers is that they cannot sense DC and low frequency information. This problem was addressed in the mid-1960's with the advent of the Hall effect stabilized current probe. This approach uses a Hall effect device within the transformer core to sense DC and low frequency signals. This information is combined with the current transformers output to form a composite DC-to-high frequency output. Careful roll-off and gain matching of the two channels preserves amplitude accuracy at all frequencies.[5] Additionally, the low frequency channel is operated as a "force-balance," meaning that the low frequency amplifier's output is fed back to magnetically bias the transformer flux to zero. Thus, the Hall effect device does not have to respond linearly over wide ranges of current and the transformer core never sees DC bias, both advantageous conditions. The amount of DC and low frequency information is obtained at the amplifier's output, which corresponds to the bias needed to offset the measured current.

Figure 24 shows a practical circuit. The Hall effect transducer lies within the core of the clip-on current transformer specified. A very simplistic way to model the Hall generator is as a bridge, excited by the two 619Ω resistors. The Hall generator's outputs (the midpoints of the "bridge") feed differential input transconductance amplifier A1, which takes gain, with roll-off set by the 50Ω, 0.02μF RC at its output. Further gain is provided by A2, in the same package as A1. A current buffer provides power gain to drive the current transformers secondary. This connection closes a flux nulling loop in the transducer core. The offset adjustments should be set for 0V output with no current flowing in the clip-on transducer. Similarly, the loop gain and bandwidth trims should be set so that the composite output (the combined high and low frequency output across the grounded 50Ω resistor) has clean step response and correct amplitude from DC to high frequency.

Note 4: Viewed from a historical perspective it is remarkable that so much precision wideband performance is available from such a relatively simple configuration. For perspective, see Appendix A, "Precision Wideband Circuitry . . . Then and Now."

Note 5: Details of this scheme are nicely presented in Reference 15. Additional relevant commentary on parallel path schemes appears in Reference 7.

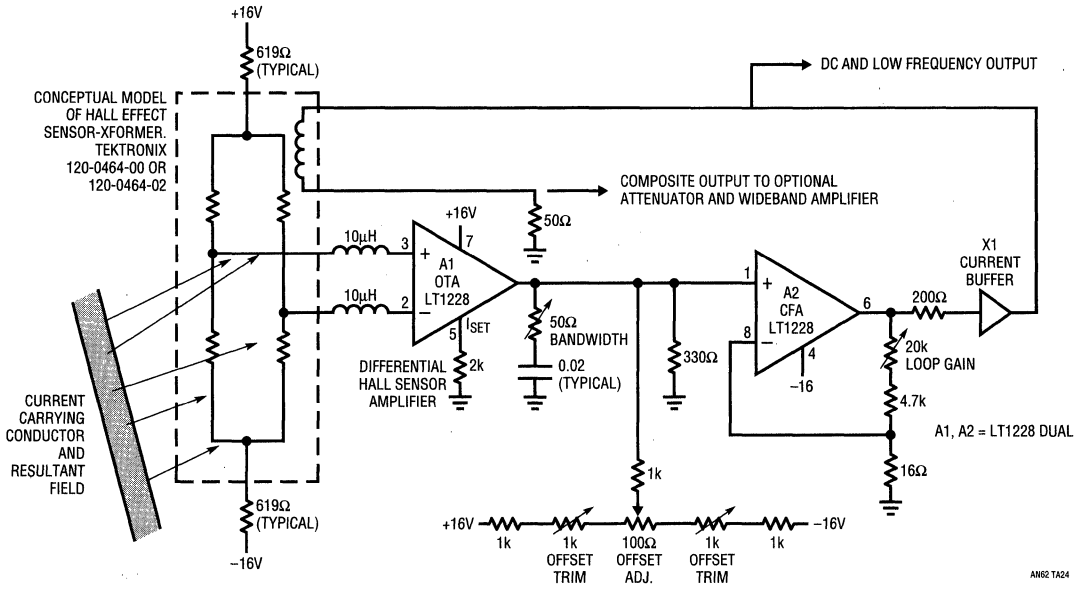


Figure 24. Hall Effect Stabilized Current Transformer (DC → High Frequency Current Probe)

Figure 25 shows a practical way to conveniently evaluate this circuits performance. This partial schematic of the Tektronix P-6042 current probe shows a similar signal conditioning scheme for the transducer specified in Figure 24. In this case Q22, Q24 and Q29 combine with differential stage M-18 to form the Hall amplifier. To evaluate Figure 24's circuit remove M-18, Q22, Q24 and Q29. Next, connect LT1228 pins 3 and 2 to the former M-18 pins 2 and 10 points, respectively. The ±16V supplies are available from the P-6042's power bus. Also, connect the right end of Figure 24's 200Ω resistor to what was Q29's collector node. Finally, perform the offset, loop gain and bandwidth trims as previously described.

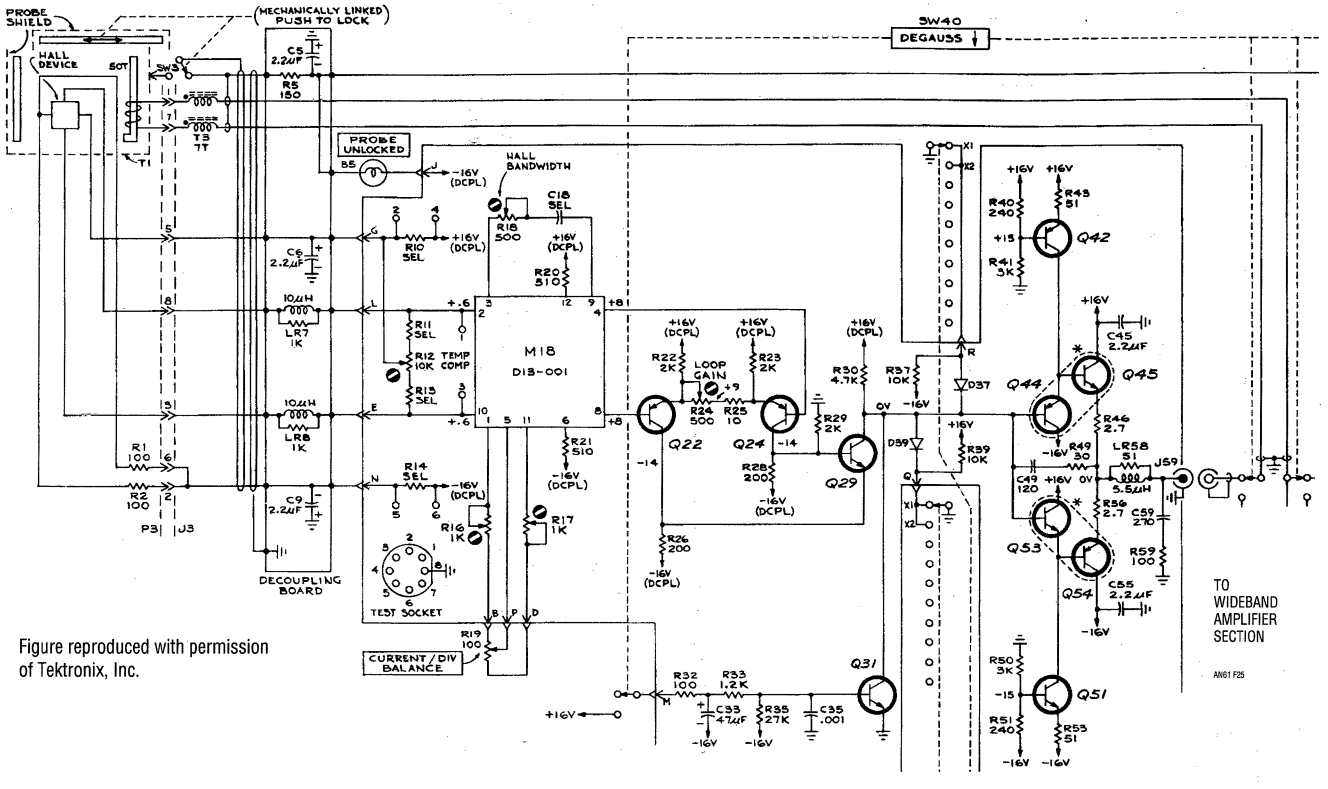


Figure reproduced with permission of Tektronix, Inc.

Figure 25. Tektronix P-6042 Hall Effect Based Current Probe Servo Loop.
Figure 24 Replaces M18 Amplifier and Q22, Q24 and Q29

Triggered 250 Picosecond Rise Time Pulse Generator

Verifying the rise time limit of wideband test equipment setups is a difficult task. In particular, the "end-to-end" rise time of oscilloscope-probe combinations is often required to assure measurement integrity. Conceptually, a pulse generator with rise times substantially faster than the oscilloscope-probe combination can provide this information. Figure 26's circuit does this, providing an 800ps pulse with rise and fall times inside 250ps. Pulse amplitude is 10V with a 50Ω source impedance. This circuit has similarities to a previously published design (see Reference 7) except that it is triggered instead of free running. This feature permits synchronization to a clock or other event. The output phase with respect to the trigger is variable from 200ps to 5ns.

The pulse generator requires high voltage bias for operation. The LT1082 switching regulator to forms a high voltage switched mode control loop. The LT1082 pulse width modulates at its 40kHz clock rate. L1's inductive events are rectified and stored in the 2µF output capacitor. The adjustable resistor divider provides feedback to the LT1082. The 10k-1µF RC provides noise filtering.

The high voltage is applied to Q1, a 40V breakdown device, via the R3-C1 combination. The high voltage "bias adjust" control should be set at the point where free running pulses across R4 *just* disappear. This puts Q1 slightly below its avalanche point. When an input trigger pulse is applied Q1 avalanches. The result is a quickly rising, very fast pulse across R4. C1 discharges, Q1's collector voltage falls and breakdown ceases. C1 then recharges to just below the avalanche point. At the next trigger pulse this action repeats.[6]

Figure 27 shows waveforms. A 3.9GHz sampling oscilloscope (Tektronix 661 with 4S2 sampling pug-in) measures the pulse (trace B) at 10V high with an 800ps base. Rise time is 250ps, with fall time indicating 200ps. The times are probably slightly faster, as the oscilloscope's 90ps rise time influences the measurement.[7] The input trigger pulse is trace A. Its amplitude provides a convenient way to vary the delay time between the trigger and output pulses. A 1V to 5V amplitude setting produces a continuous 5ns to 200ps delay range.

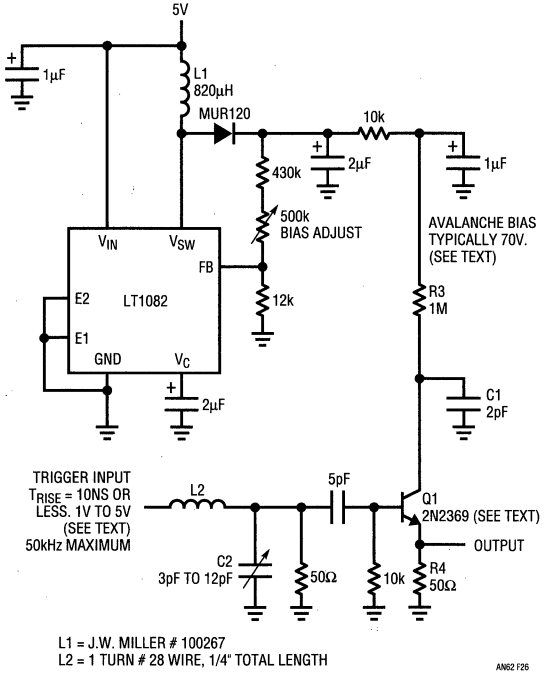


Figure 26. Triggered 250ps Rise Time Pulse Generator. Trigger Pulse Amplitude Controls Output Phase

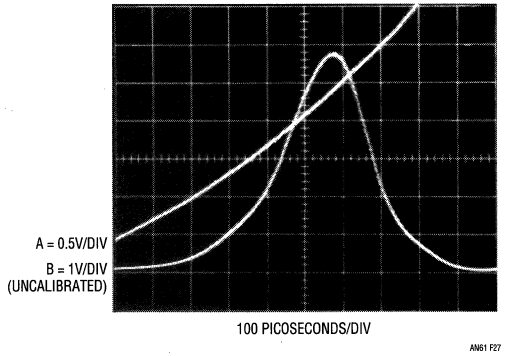


Figure 27. Input Pulse Edge (Trace A) Triggers the Avalanche Pulse Output (Trace B). Display Granularity Is Characteristic of Sampling Oscilloscope Operation

Note 6: This circuit is based on the operation of the Tektronix Type 111 Pulse Generator. See Reference 16.

Note 7: I'm sorry, but 3.9GHz is the fastest 'scope in my house (as of September, 1993).

Some special considerations are required to optimize circuit performance. L2's very small inductance combines with C2 to slightly retard the trigger pulse's rise time. This prevents significant trigger pulse artifacts from appearing at the circuit's output. C2 should be adjusted for the best compromise between output pulse rise time and purity. Figure 28 shows partial pulse rise with C2 properly adjusted. There are no discernible discontinuities related to the trigger event.

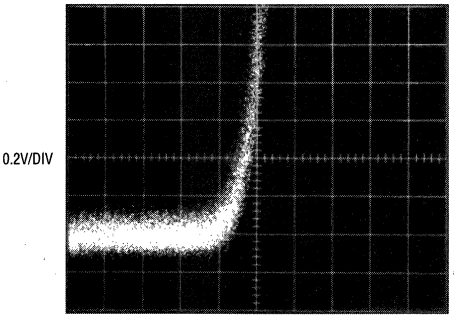


Figure 28. Expanded Scale View of Leading Edge Is Clean with No Trigger Pulse Artifacts. Display Granularity Derives from Sampling Oscilloscope Operation

Q1 may require selection to get avalanche behavior. Such behavior, while characteristic of the device specified, is not guaranteed by the manufacturer. A sample of 50 Motorola 2N2369s, spread over a 12 year date code span, yielded 82%. All "good" devices switched in less than 600ps. C1 is selected for a 10V amplitude output. Value spread is typically 2pF to 4pF. Ground plane type construction with high speed layout, connection and termination techniques are essential for a good results from this circuit.

Flash Memory Programmer

Although "Flash" type memory is increasingly popular, it does require some special programming features. The 5V powered memories need a carefully controlled 12V "VPP" programming pulse. The pulse's amplitude must be within 5% to assure proper operation. Additionally, the pulse must not overshoot, as memory destruction may occur for VPP outputs above 14V.[8] These requirements usually mandate a separate 12V supply and pulse forming circuitry. Figure 29's circuit provides the complete flash memory programming function with a single IC and some discrete components. All components are surface mount types, so little board space is required. The entire function runs off a single 5V supply.

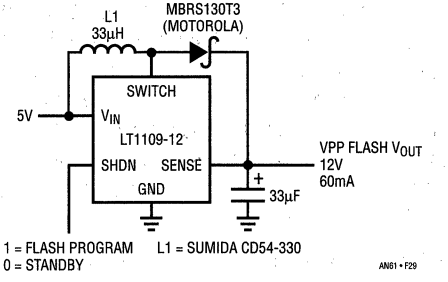


Figure 29. Switching Regulator Provides Complete Flash Memory Programmer

The LT1109-12 switching regulator functions by repetitively pulsing L1. L1 responds with high voltage flyback events, which are rectified by the diode and stored in the 10µF capacitor. The "sense" pin provides feedback, and the output voltage stabilizes at 12V within a few percent. The regulator's "shutdown" pin provides a way to control the VPP programming voltage output. With a logical zero applied to the pin the regulator shuts down, and no VPP programming voltage appears at the output. When the pin goes high (trace A, Figure 30) the regulator is activated, producing a cleanly rising, controlled pulse at the output (trace B). When the pin is returned to logical zero, the output smoothly decays off. The switched mode delivery of power combined with the output capacitor's filtering prevents overshoot while providing the required pulse amplitude accuracy. Trace C, a time and amplitude expanded version of trace B, shows this. The output steps up in amplitude each time L1 dumps energy into the output capacitor. When the regulation point is reached the amplitude cleanly flattens out, with only about 75mV of regulator ripple.

Note 8: See Reference 17 for detailed discussion.

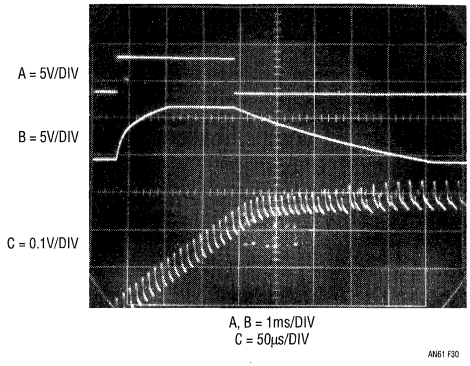


Figure 30. Flash Memory Programmer Waveforms Show Controlled Edges. Trace C Details Rise Time Settling

3.3V Powered V/F Converter

Figure 31 is a "charge pump" type V/F converter specifically designed to run from a 3.3V rail.[9] A 0V to 2V input produces a corresponding 0kHz to 3kHz output with linearity inside 0.05%. To understand how the circuit works assume that A1's negative input is just below 0V. The amplifier output is positive. Under these conditions, LTC1043's pins 12 and 13 are shorted as are pins 11 and 7, allowing the 0.01µF capacitor (C1) to charge to the 1.2V LT1034 reference. When the input-voltage-derived current ramps A1's summing point (negative input-trace A, Figure 32) positive, its output (trace B) goes low. This reverses the LTC1043's switch states, connecting pins 12 and 14, and 11 and 8. This effectively connects C1's positively charged end to ground on pin 8, forcing current to flow from A1's summing junction into C1 via LTC1043 pin 14 (pin 14's current is trace C). This action resets A1's summing point to a small negative potential (again, trace A). The 120pF-50k-10k time constant at A1's positive input ensures A1 remains low long enough for C1 to completely discharge (A1's positive input is trace D). The Schottky diode prevents excessive negative excursions due to the 120pF capacitors differentiated response.

When the 120pF positive feedback path decays, A1's output returns positive and the entire cycle repeats. The oscillation frequency of this action is directly related to the input voltage.

This is an AC coupled feedback loop. Because of this, start-up or overdrive conditions could force A1 to go low and

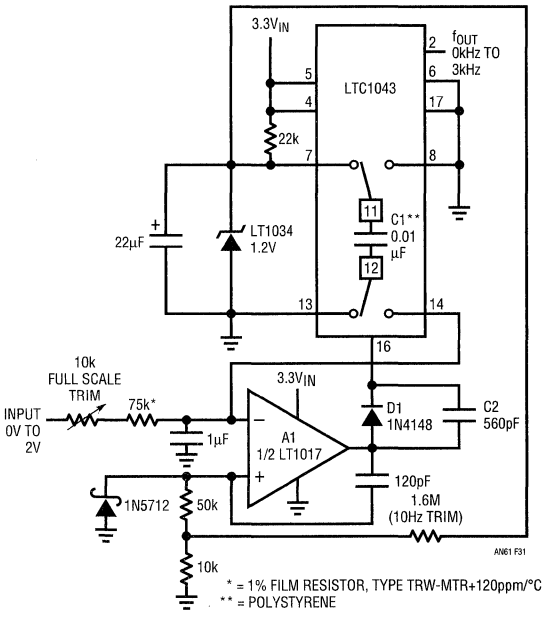


Figure 31. 3.3V Powered Voltage-to-Frequency Converter. Charge Pump Based Feedback Maintains High Linearity and Stability

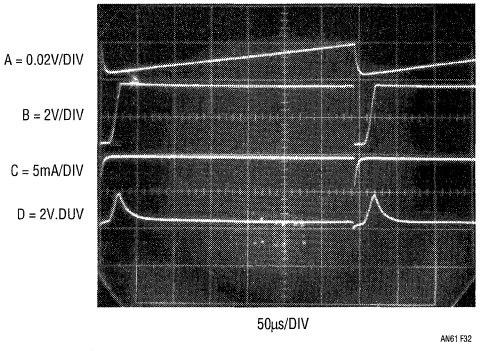


Figure 32. Waveform for the 3.3V Powered V/F. Charge Pump Action (Trace C) Maintains Summing Point (Trace A), Enforcing High Linearity and Accuracy

Note 9: See Reference 20 for a survey of V/F techniques. The circuit shown here is derived from Figure 8 in LTC Application Note 50, "Interfacing to Microprocessor Based 5V Systems" by Thomas Mosteller.

stay there. When A1's output is low the LTC1043's internal oscillator sees C2 and will begin oscillation if A1 remains low long enough. This oscillation causes charge pumping action via the LTC1043-C1-A1 summing junction path until normal operation commences. During normal operation A1 is never low long enough for oscillation to occur, and controls the LTC1043 switch states via D1.

To calibrate this circuit apply 7mV and select the 1.6M (nominal) value for 10Hz out. Then apply 2.000V and set the 10k trim for exactly 3kHz output. Pertinent specifications include linearity of 0.05%, power supply rejection of 0.04%/V, temperature coefficient of 75ppm/°C of scale and supply current of about 200µA. The power supply may vary from 2.6V to 4.0V with no degradation of these specifications. If degraded temperature coefficients are acceptable, the film resistor specified may be replaced by a standard 1% film resistor. The type called out has a temperature characteristic that opposes C1's –120ppm/°C drift, resulting in the low overall circuit drift noted.

Broadband Random Noise Generator

Filter, audio, and RF-communications testing often require a random noise source.[10] Figure 33's circuit provides an RMS-amplitude regulated noise source with selectable bandwidth. RMS output is 300mV with a 1kHz to 5MHz bandwidth, selectable in decade ranges.

Noise source D1 is AC coupled to A2, which provides a broadband gain of 100. A2's output feeds a gain control stage via a simple, selectable lowpass filter. The filter's output is applied to A3, an LT1228 operational transcon-

Note 10: See Appendix B, "Symmetrical White Gaussian Noise," guest written by Ben Hessen-Schmidt of Noise Com, Inc. for tutorial on noise.

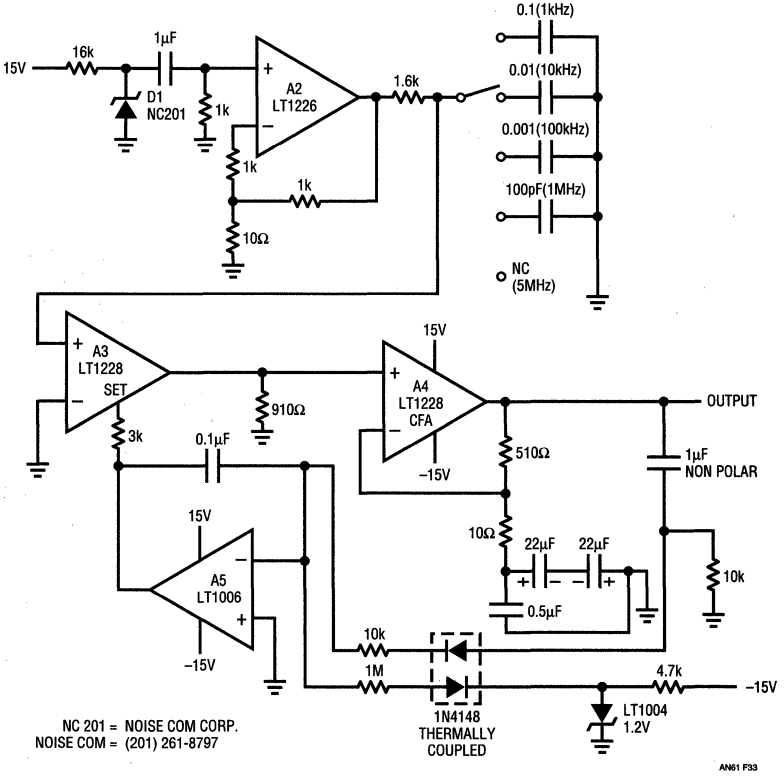


Figure 33. Broadband Random Noise Generator Uses Gain Control Loop to Enhance Noise Spectrum Amplitude Uniformity

ductance amplifier. A3's output feeds LT1228 A4, a current feedback amplifier. A4's output, also the circuit's output, is sampled by the A5-based gain control configuration. This closes a gain control loop to A3. A3's set current controls gain, allowing overall output level control.

Figure 34 shows noise at 1MHz bandpass, with Figure 35 showing RMS noise versus frequency in the same bandpass. Figure 36 plots similar information at full bandwidth (5MHz). RMS output is essentially flat to 1.5MHz with about ±2dB control to 5MHz before sagging badly.

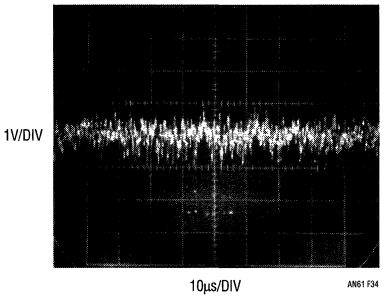


Figure 34. Figure 33's Output in the 1MHz Filter Position

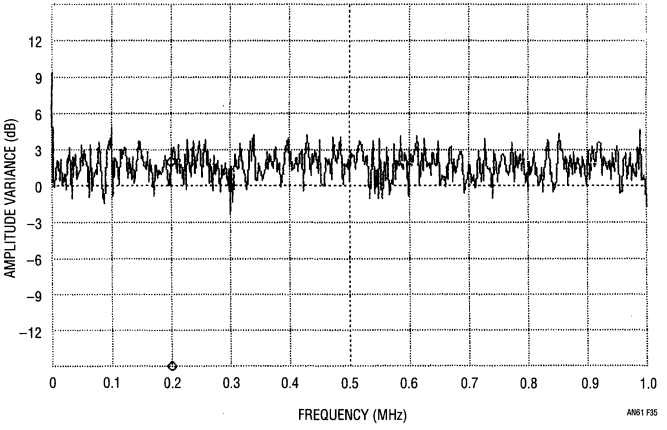


Figure 35. Amplitude vs Frequency for the Random Noise Generator Is Essentially Flat to 1MHz

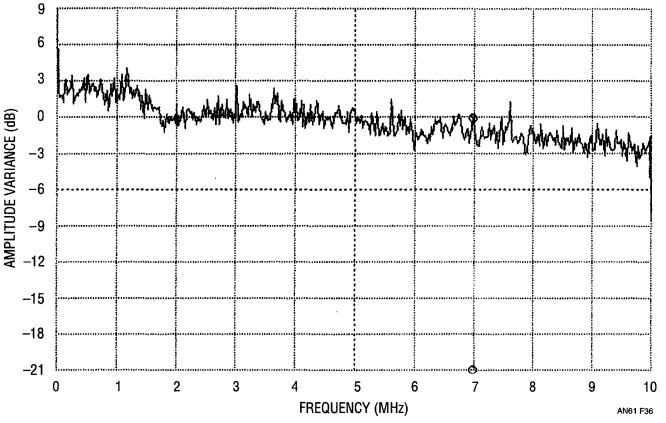


Figure 36. RMS Noise vs Frequency at 5MHz Bandpass Shows Slight Fall-Off Beyond 1MHz

Figure 37's similar circuit substitutes a standard zener for the noise source but is more complex and requires a trim. A1, biased from the LT1004 reference, provides optimum drive for D1, the noise source. AC coupled A2 takes a broadband gain of 100. A2's output feeds a gain-control stage via a simple selectable lowpass filter. The filter's output is applied to LT1228 A3, an operational transconductance amplifier. A3's output feeds LT1228 A4, a current feedbacks amplifier. A4's output, the circuit's output, is sampled by the A5-based gain control configuration. This closes a gain control loop back at A3. A3's set input current controls its gain, allowing overall output level control.

To adjust this circuit, place the filter in the 1kHz position and trim the 5k potentiometer for maximum negative bias at A3, pin 5.

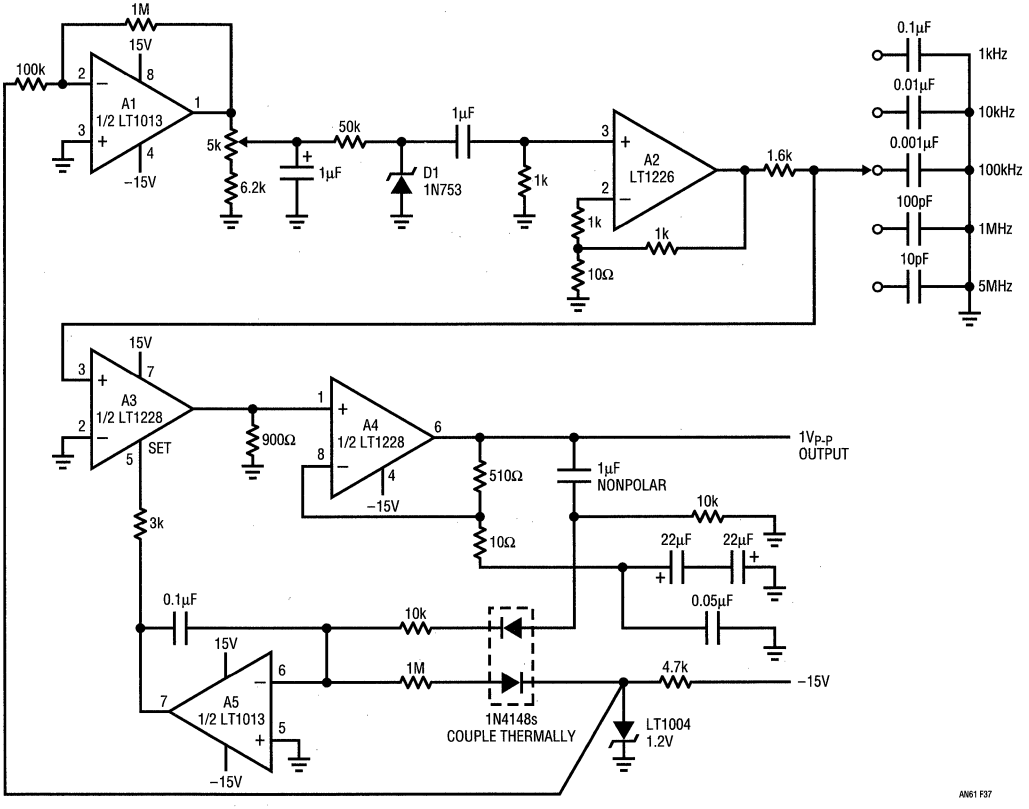


Figure 37. A Similar Circuit Uses a Standard Zener Diode, But Is More Complex and Requires Trimming

Switchable Output Crystal Oscillator

Figure 38's simple crystal oscillator circuit permits crystals to be electronically switched by logic commands. The circuit is best understood by initially ignoring all crystals. Further, assume all diodes are shorts and their associated 1k resistors open. The resistors at the LT1116's positive input set a DC bias point. The 2k-25pF path sets up phase shifted feedback and the circuit looks like a wideband unity gain follower at DC. When "Xtal A" is inserted (remember, D1 is temporarily shorted) positive feedback occurs and oscillation commences at the crystals resonant frequency. If D1 and its associated 1k value are realized, oscillation can only continue if logic input A is biased high. Similarly, additional crystal-diode-1k branches permit logic selection of crystal frequency.

For AT cut crystals about a millisecond is required for the circuit output to stabilize due to the high Q factors involved. Crystal frequencies can be as high as 16MHz before comparator delays preclude reliable operation.

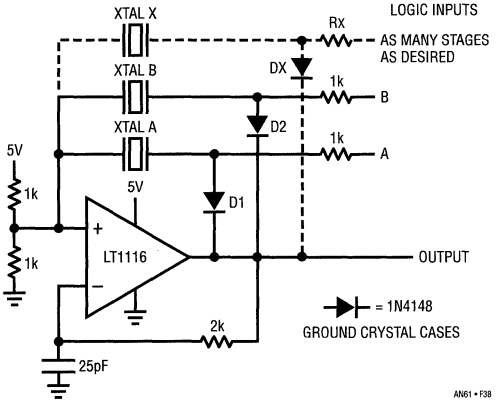


Figure 38. Switchable Output Crystal Oscillator. Biasing A or B High Places the Associated Crystal in the Feedback Path. Additional Crystal Branches Are Permissible

REFERENCES

1. Williams, Jim and Huffman, Brian. "Some Thoughts on DC-DC Converters," pages 13-17, "1.5V to 5V Converters." Linear Technology Corporation, *Application Note 29*, October 1988.
2. Williams, J., "Illumination Circuitry for Liquid Crystal Displays," Linear Technology Corporation, *Application Note 49*, August 1992.
3. Williams, J., "Techniques for 92% Efficient LCD Illumination," Linear Technology Corporation, *Application Note 55*, August 1993.
4. Williams, J., "Measurement and Control Circuit Collection," Linear Technology Corporation, *Application Note 45*, June 1991.
5. Benjaminson, Albert, "The Linear Quartz Thermometer—a New Tool for Measuring Absolute and Difference Temperatures," *Hewlett-Packard Journal*, March 1965.
6. Micro Crystal-ETA Fabriques d'Ebauches., "Miniature Quartz Resonators - MT Series" Data Sheet. 2540 Grenchen, Switzerland.

7. Williams, J., "High Speed Amplifier Techniques," Linear Technology Corporation, *Application Note 47*, August 1991.
8. Williams, Jim, "High Speed Comparator Techniques," Linear Technology Corporation, *Application Note 13*, April 1985.
9. Williams, Jim, "A Monolithic IC for 100MHz RMS-DC Conversion," Linear Technology Corporation, *Application Note 22*, September 1987.
10. Ott, W.E., "A New Technique of Thermal RMS Measurement," *IEEE Journal of Solid State Circuits*, December 1974.
11. Williams, J.M. and Longman, T.L., "A 25MHz Thermally Based RMS-DC Converter," *1986 IEEE ISSCC Digest of Technical Papers.*
12. O'Neill, P.M., "A Monolithic Thermal Converter," *H.P. Journal*, May 1980.
13. C. Kitchen, L. Counts, "*RMS-to-DC Conversion Guide*," Analog Devices, Inc. 1986.
14. Tektronix, Inc. "*P6042 Current Probe Operating and Service Manual*," 1967.
15. Weber, Joe, "Oscilloscope Probe Circuits," Tektronix, Inc., Concept Series. 1969.
16. Tektronix, Inc., *Type 111 Pretrigger Pulse Generator Operating and Service Manual*, Tektronix, Inc. 1960.
17. Williams, J., "Linear Circuits for Digital Systems," Linear Technology Corporation, *Application Note 31*, February 1989.
18. Williams, J., "Applications for a Switched-Capacitor Instrumentation Building Block," Linear Technology Corporation, *Application Note 3*, July 1985.
19. Williams, J., "Circuit Techniques for Clock Sources," Linear Technology Corporation, *Application Note 12*, October 1985.
20. Williams, J. "Designs for High Performance Voltage-to-Frequency Converters," Linear Technology Corporation, *Application Note 14*, March 1986.

APPENDIX A

Precision Wideband Circuitry . . . Then and Now

Text Figure 22's relatively straightforward design provides a sensitive, thermally-based RMS/DC conversion to 10MHz with less than 1% error. Viewed from a historical perspective it is remarkable that so much precision wideband performance is so easily achieved.

Thirty years ago these specifications presented an extremely difficult engineering challenge, requiring deep-seated knowledge of fundamentals, extraordinary levels of finesse and an interdisciplinary outlook to achieve success.

The Hewlett-Packard model HP3400A (1965 price $525 . . . about 1/3 the yearly tuition at M.I.T.) thermally-based RMS voltmeter included all of Figure 22's elements, but considerably more effort was required in its execution.[1] Our comparative study begins by considering H-P's version of Figure 22's FET buffer and precision wideband amplifier. The text is taken directly from the *HP3400A Operating and Service Manual*.[2]

Note 1: We are all constantly harangued about the advances made in computers since the days of the IBM360. This section gives analog aficionados a stage for their own bragging rights. Of course, an HP3400A was much more interesting than an IBM360 in 1965. Similarly, Figure 22's capabilities are more impressive than any contemporary computer I'm aware of.

Note 2: All Hewlett-Packard text and figures used here are copyright 1965 Hewlett-Packard Company. Reproduced with permission.,

4-15. IMPEDANCE CONVERTER ASSEMBLY A2.

4-17. The ac signal input to the impedance converter is RC coupled to the grid of cathode follower V201[3] through C201 and R203. The output signal is developed by Q201 which acts as a variable resistance in the cathode circuit of V201. The bootstrap feedback from the cathode of V201 to R203 increases the effective resistance of R203 to the input signal. This prevents R203 from loading the input signal and preserves the high input impedance of the Model 3400A. The gain compensating feedback from the plate of V201 to the base of Q201 compensates for any varying gain in V201 due to age or replacement.

4-18. Breakdown diode CR201 controls the grid bias voltage on V201 thereby establishing the operating point of this stage. CR202 and R211 across the base-emitter junction of Q201 protects Q201 in the event of a failure in the +75 volt power supply. Regulated dc is supplied to V201 filaments to avoid inducing ac hum in the signal path. This also prevents the gain of V201 changing with line voltage variations.

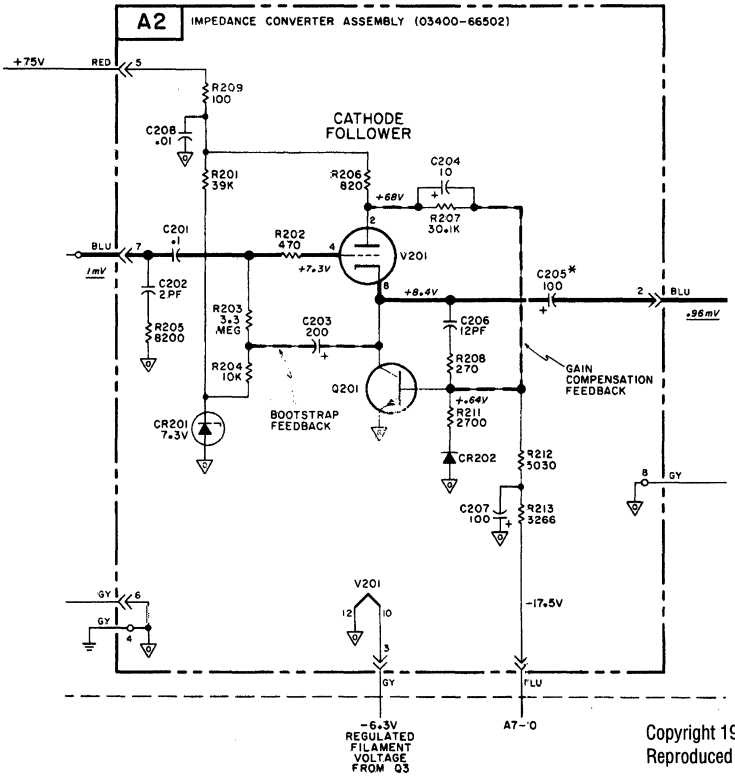


Figure A1. The "Impedance Converter Assembly," H-P's Equivalent of Figure 22's Wideband FET Buffer

Note 3: Although JFETs were available in 1965 their performance was inadequate for this design's requirements. The only available option was the Nuvistor triode described.

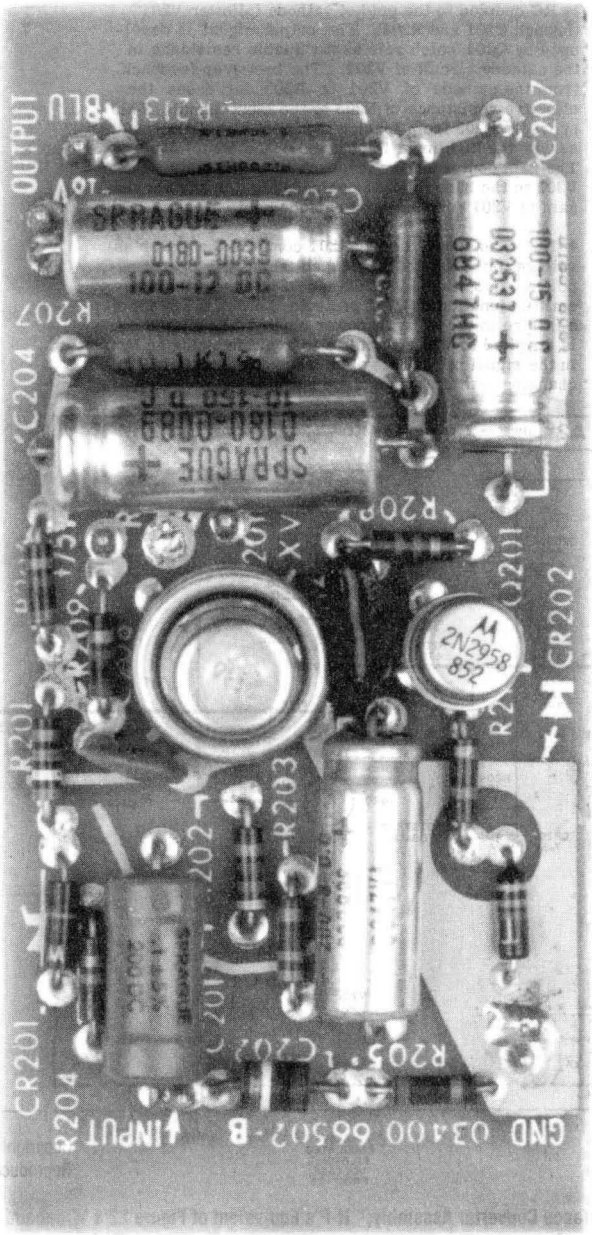


Figure A2. The Hewlett-Packard 3400A's Wideband Input Buffer. Nuvistor Triode (Upper Center) Provided Speed, Low Noise, and High Impedance. Circuit Required 75V, –17.5V and –6.3V Supplies. Regulated Filament Supply Stabilized Follower Gain While Minimizing Noise

4-22. VIDEO AMPLIFIER ASSEMBLY A4.

4-23. The video amplifier functions to provide constant gain to the ac signal being measured over the entire frequency range of Model 3400A. See video amplifier assembly schematic diagram illustrated on Figure 6-2.

4-24. The ac input signal from the second attenuator is coupled through C402 to the base of input amplifier Q401. Q401, a class A amplifier, amplifies and inverts the signal which is then direct coupled to the base of bootstrap amplifier Q402. The output, taken from Q402 emitter is applied to the base of Q403 and fed back to the top of R406 as a bootstrap feedback. This positive ac feedback increases the effective ac resistance of R406 allowing a greater portion of the signal to be felt at the base of Q402. In this manner, the effective ac gain of Q401 is increased for the midband frequencies without disturbing the static operating voltages of Q401.

4-25. Driver amplifier Q403 further amplifies the ac signal and the output at Q403 collector is fed to the base circuit emitter follower Q404. The feedback path from the collector of Q403 to the base of Q402 through C405 (10 MHz ADJ) prevents spurious oscillations at high input frequencies. A dc feedback loop exists from the emitter circuit of Q403, to the base of Q401 through R425. This feedback stabilizes the Q401 bias voltage. Emitter follower Q404 acts as a driver for the output amplifier consisting of Q405 and Q406; a complimentary pair operating as a push-pull amplifier. The video amplifier output is taken from the collectors of the output amplifiers and applied to thermocouples TC401. A gain stabilizing feedback is developed in the emitter circuits of the output amplifiers. This negative feedback is applied to the emitter of input amplifier Q401 and establishes the overall gain of the video amplifier.

4-26. Trimmer capacitor C405 is adjusted at 10 MHz for frequency response of the video amplifier. Diodes CR402 and CR406 are protection diodes which prevent voltage surges from damaging transistors in the video amplifier. CR401, CR407, and CR408 are temperature compensating diodes to maintain the zero signal balance condition in the output amplifier over the operating temperature range. CR403, a breakdown diode, establishes the operating potentials for the output amplifier.

If that's not enough to make you propose marriage to modern high speed monolithic amplifiers, consider the design heroics spent on the thermal converter.

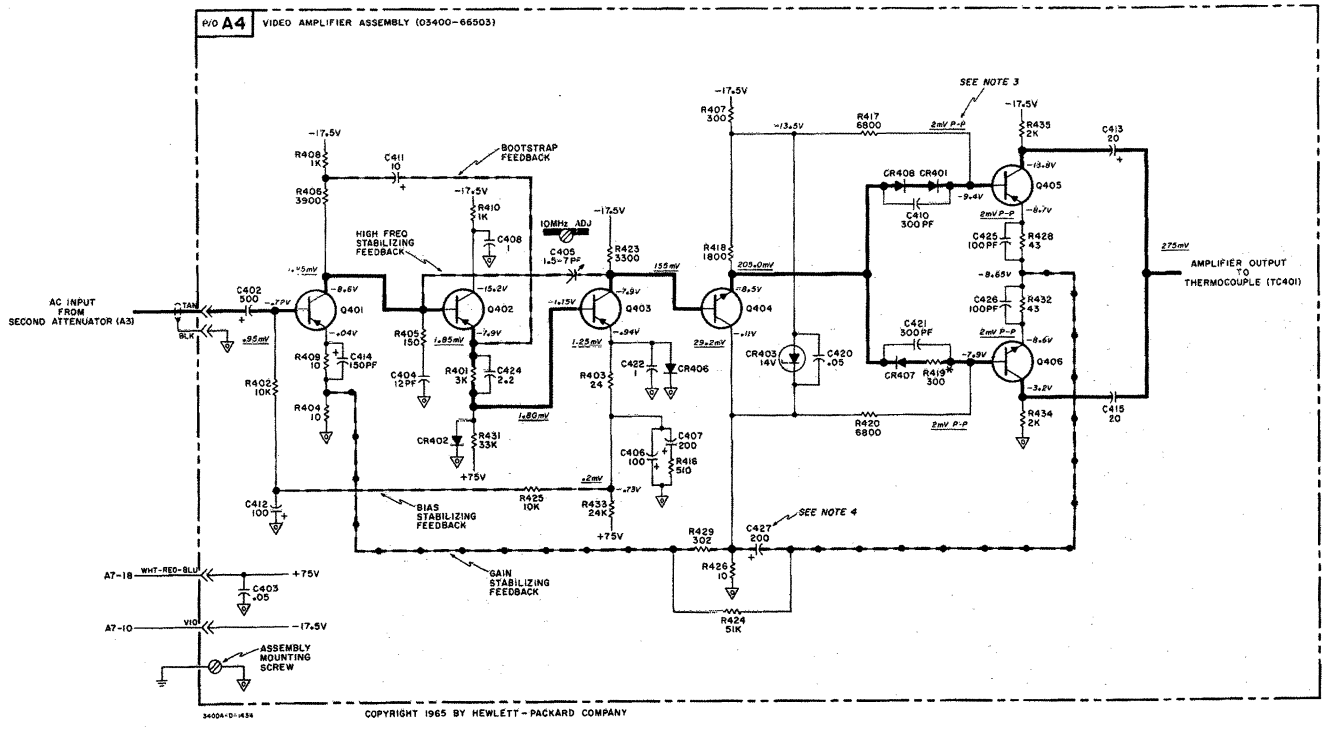


Figure A3. H-P's Wideband Amplifier, the "Video Amplifier Assembly" Contained DC and AC Feedback Loops, Peaking Networks, Bootstrap Feedback and Other Subtleties to Equal Figure 22's Performance

Figure A4. The Voltmeters "Video Amplifier" Received Input at Board's Left Side. Amplifier Output Drove Shrouded Thermal Converter at Lower Right. Note High Frequency Response Trimmer Capacitor at Left Center

4-27. PHOTOCHOPPER ASSEMBLY A5, CHOPPER AMPLIFIER ASSEMBLY A6, AND THERMOCOUPLE PAIR (PART OF A4).

4-28. The modulator/demodulator, chopper amplifier, and thermocouple pair form a servo loop which functions to position the direct reading meter M1 to the rms value of the ac input signal.[4] See modulator/demodulator, chopper amplifier, and thermocouple pair schematic diagram illustrated in Figure 6-3.

4-29. The video amplifier output signal is applied to the heater of thermocouple TC401. This ac voltage causes a dc voltage to be generated in the resistive portion of TC401 which is proportional to the heating effect (rms value) of the ac input. The dc voltage is applied to photocell V501.

4-30. Photocells V501 and V502 in conjunction with neon lamps DS501 and DS502 form a modulator circuit.[5] The neon lamps are lighted alternately between 90 and 100 Hz. Each lamp illuminates one of the photocells. DS501 illuminates V501;DS502 illuminates V502. When a photocell is illuminated it has a low resistance compared to its resistance when dark. Therefore, when V501 is illuminated, the output of thermocouple TC401 is applied to the input of the chopper amplifier through V501. When V502 is illuminated, a ground signal is applied to the chopper amplifier. The alternate illumination of V501 and V502 modulates the dc input at a frequency between 90 and 100 Hz. The modulator output is a square wave whose amplitude is proportional to the dc input level.

4-31. The chopper amplifier, consisting of Q601 through Q603, is a high gain amplifier which amplifies the square wave developed by the modulator. Power supply voltage variations are reduced by diodes CR601 thru CR603. The amplified output is taken from the collector of Q603 and applied to the demodulator through emitter follower Q604.

4-32. The demodulator comprises two photocells, V503 and V504, which operate in conjunction with DS501 and DS502; the same neon lamps used to illuminate the photocells in the modulator. Photocells V503 and V504 are illuminated by DS501 and DS502, respectively.

4-33. The demodulation process is the reverse of the modulation process discussed in Paragraph 4-30. The output of the demodulator is a dc level which is proportional to the demodulator input. The magnitude and phase of the input square wave determines the magnitude and polarity of the dc output level. This dc output level is applied to two emitter follower output stages.

4-34. The emitter follower is needed to match the high output impedance of the demodulator to the low input impedance of the meter and thermocouple circuits. The voltage drop across CR604 in the collector circuit of Q605 is the operating bias for Q604. This fixed bias prevents Q605 failure when the base voltage is zero with respect to ground.

(Text continues on page 38)

Note 4: In 1965 almost all thermal converters utilized matched pairs of discrete heater resistors and thermocouples. The thermocouples' low level output necessitated chopper amplifier signal conditioning, the only technology then available which could provide the necessary DC stability.

Note 5: The low level chopping technology of the day was mechanical choppers, a form of relay. H-P's use of neon lamps and photocells as microvolt choppers was more reliable and an innovation. Hewlett-Packard has a long and successful history of using lamps for unintended purposes.

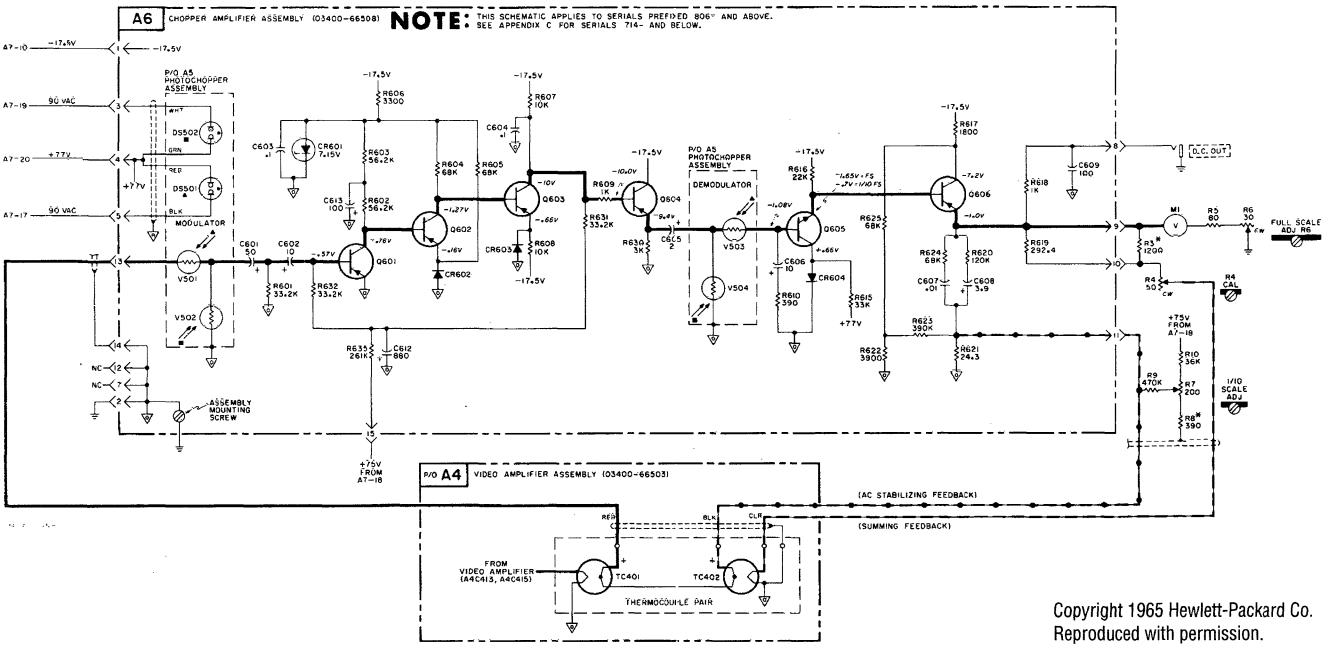


Figure A5. H-P's Thermal Converter ("A4") and Control Amplifier ("A6") Perform Similarly to Text Figure 22's Dual Op Amp and LT1088. Circuit Realization Required Far More Attention to Details

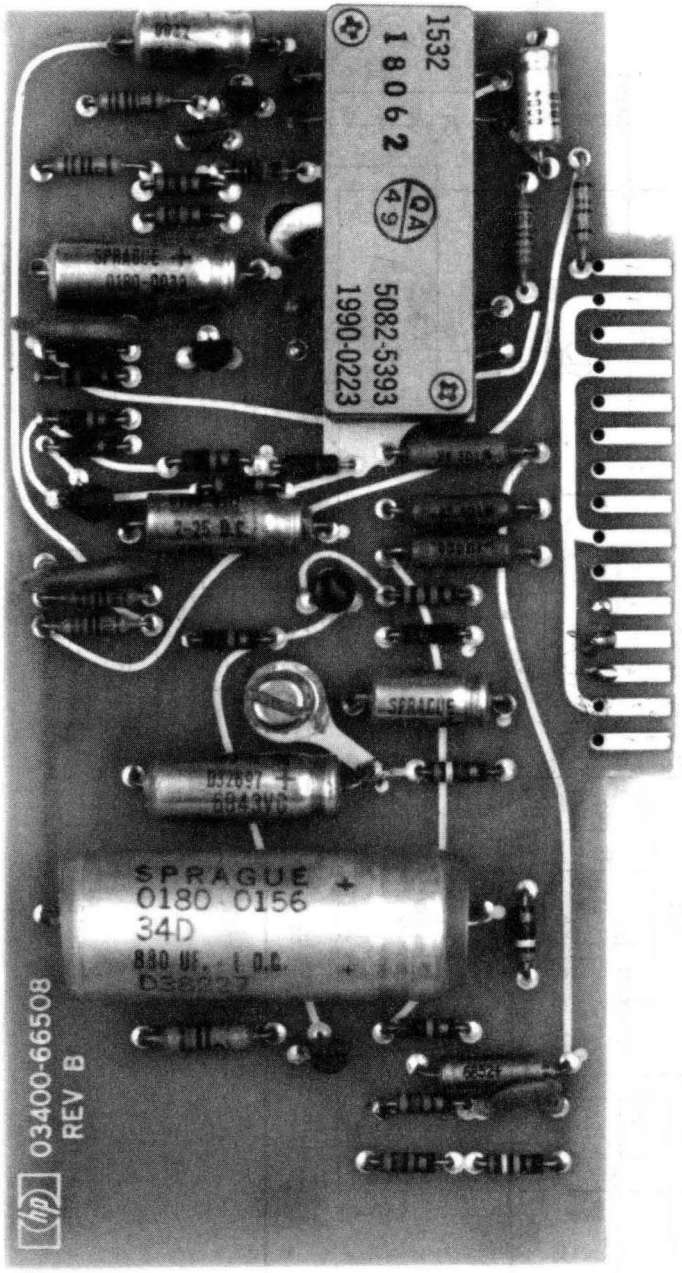


Figure A6. Chopper Amplifier Board Feedback Controlled the Thermal Converter. Over Fifty Components Were Required, Including Neon Lamps, Photocells and Six Transistors. Photo-Chopper Assembly Is at Board's Lower Right

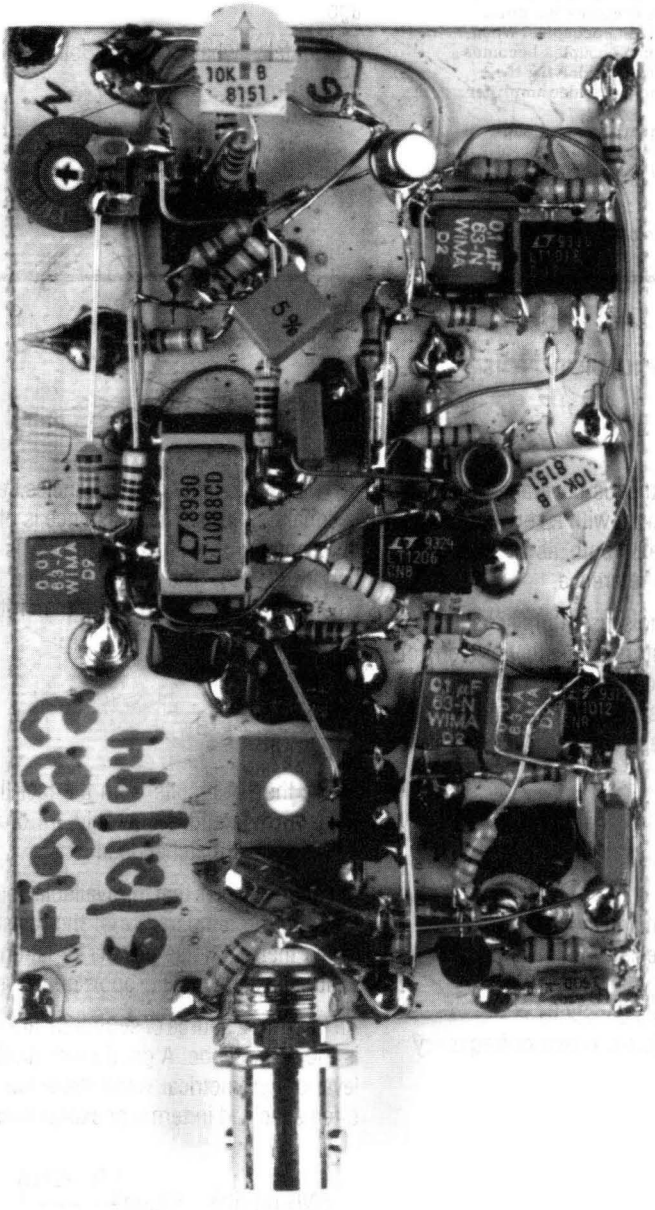


Figure A7. Figure 22's Circuit Puts Entire HP3400 Electronics on One Small Board. FET Buffer-LT1206 Amplifier Appear Left Center Behind BNC Shield. LT1088 IC (Upper Center) Replaces Thermal Converter. LT1013 (Upper Right) Based Circuitry Replaces Photo-Chopper Board. LT1018 and Components (Lower Right) Provide Overload Protection. Ain't Modern ICs Wonderful?

4-35. The dc level output, taken from the emitter of Q606, is applied to meter M1 and to the heating element of thermocouple TC402. The dc voltage developed in the resistive portion of TC402 is effectively subtracted from the voltage developed by TC401. The input signal to the modulator then becomes the difference in the dc outputs of the two thermocouples. When the difference between the two thermocouples becomes zero the dc from the emitter followers (driving the meter) will be equal to the ac from the video amplifier.

4-36. Noise on the modulated square wave is suppressed by feedback from emitter of Q606 through C607 and C608 to the resistive element of TC402.

When casually constructing a wideband amplifier with a few mini-DIPs, the reader will do well to recall the pain and skill expended by the HP3400A's designers some 30 years ago.

Incidentally, what were *you* doing in 1965?

APPENDIX B

Symmetrical White Gaussian Noise

by Ben Hessen-Schmidt,
NOISE COM, INC.

White noise provides instantaneous coverage of all frequencies within a band of interest with a very flat output spectrum. This makes it useful both as a broadband stimulus and as a power-level reference.

Symmetrical white Gaussian noise is naturally generated in resistors. The noise in resistors is due to vibrations of the conducting electrons and holes, as described by Johnson and Nyquist.[1] The distribution of the noise voltage is symmetrically Gaussian, and the average noise voltage is:

$$\overline{V}_n = 2\sqrt{kT\int R(f)\, p(f)\, df} \qquad (1)$$

Where:

k = 1.38E–23 J/K (Boltzmann's constant)
T = temperature of the resistor in Kelvin
f = frequency in Hz
h = 6.62E–34 Js (Planck's constant)
R(f) = resistance in ohms as a function of frequency

$$p(f) = \frac{hf}{kT\left[\exp(hf/kT) - 1\right]} \qquad (2)$$

Note 1: See "Additional Reading" at end of this section.

p(f) is close to unity for frequencies below 40GHz when T is equal to 290°K. The resistance is often assumed to be independent of frequency, and ∫df is equal to the noise bandwidth (B). The available noise power is obtained when the load is a conjugate match to the resistor, and it is:

$$N = \frac{\overline{V}_n^{\,2}}{4R} = kTB \qquad (3)$$

where the "4" results from the fact that only half of the noise voltage and hence only 1/4 of the noise power is delivered to a matched load.

Equation 3 shows that the available noise power is proportional to the temperature of the resistor; thus it is often called thermal noise power, Equation 3 also shows that white noise power is proportional to the bandwidth.

An important source of symmetrical white Gaussian noise is the noise diode. A good noise diode generates a high level of symmetrical white Gaussian noise. The level is often specified in terms of excess noise ratio (ENR).

$$ENR\,(\text{in dB}) = 10\text{Log}\frac{(Te - 290)}{290} \qquad (4)$$

Te is the physical temperature that a load (with the same impedance as the noise diode) must be at to generate the same amount of noise.

The ENR expresses how many times the effective noise power delivered to a non-emitting, nonreflecting load exceeds the noise power available from a load held at the reference temperature of 290°K (16.8°C or 62.3°F).

The importance of high ENR becomes obvious when the noise is amplified, because the noise contributions of the amplifier may be disregarded when the ENR is 17dB larger than the noise figure of the amplifier (the difference in total noise power is then less than 0.1dB). The ENR can easily be converted to noise spectral density in dBm/Hz or $\mu V/\sqrt{Hz}$ by use of the white noise conversion formulas in Table 1.

Table 1. Useful White Noise conversion

dBm	=	dBm/Hz + 10log (BW)
dBm	=	20log ($\overline{V}$n) – 10log(R) + 30dB
dBm	=	20log($\overline{V}$n) + 13dB for R = 50Ω
dBm/Hz	=	20log($\mu\overline{V}n\sqrt{Hz}$) – 10log(R) – 90dB
dBm/Hz	=	–174dBm/Hz + ENR for ENR > 17dB

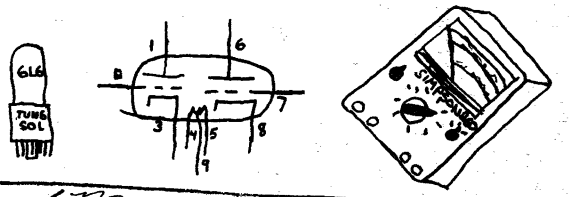
When amplifying noise it is important to remember that the noise voltage has a Gaussian distribution. The peak voltages of noise are therefore much larger than the average or RMS voltage. The ratio of peak voltage to RMS voltage is called crest factor, and a good crest factor for Gaussian noise is between 5:1 and 10:1 (14 to 20dB). An amplifier's 1dB gain-compression point should therefore be typically 20dB larger than the desired average noise-output power to avoid clipping of the noise.

For more information about noise diodes, please contact NOISE COM, INC. at (201) 261-8797.

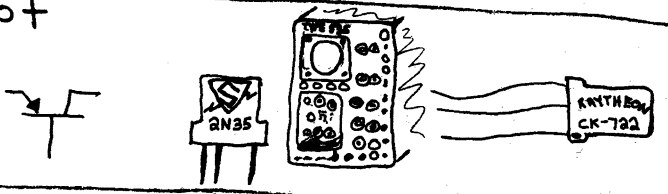
Additional Reading

1. Johnson, J.B, "Thermal Agitation of Electricity in Conductors," *Physical Review*, July 1928, pp. 97-109.
2. Nyquist, H. "Thermal Agitation of Electric Charge in Conductors," *Physical Review*, July 1928, pp. 110-113.

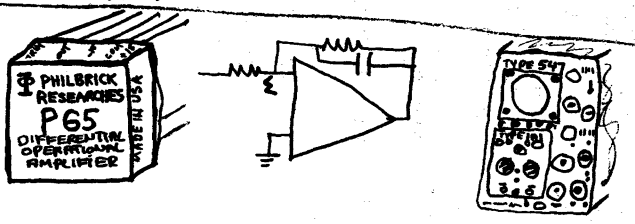
When I WAS 6 years old
All I WANTed to do WAS MAKE
CIRCUITS with 12AX7's & 6L6's.



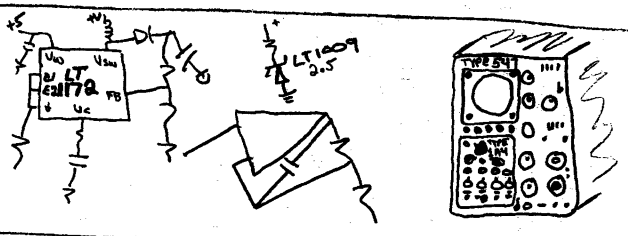
When I WAS 10 I got
2N35's & CK-722's.
No Filaments. WOW!



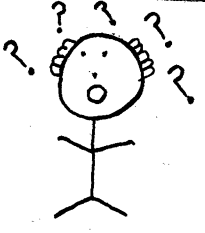
When I WAS 17 I used
PhiLbrick P-65's. You
COULD DO anything.



NOW, I'M 46 & I CAN HACK
ALL the op-amps and switching
Regulators I WANT. EVERY Day!



Is The Mid-LiFe Crisis When They
RUN Out of 10K Resistors?



'94

Data Acquisition Circuit Collection

Kevin R. Hoskins

INTRODUCTION

This application note features 8-, 10-, and 12-bit data acquisition components in various circuit configurations. The circuits include battery monitoring, temperature sensing, isolated serial interfaces, and microprocessor and microcontroller serial and parallel interfaces. Also included are voltage reference circuits (Application Note 42 contains more voltage reference circuits).

Additional circuit information is located in the information references listed in the Circuit Index. Each information reference refers to either an application note (example: AN42 = Application Note 42), a data sheet (example: LTC®1292 DS = LTC1292 Data Sheet), or a design note (example: DN66 = Design Note 66).

CIRCUIT INDEX

GENERAL ANALOG-TO-DIGITAL APPLICATION CIRCUITS

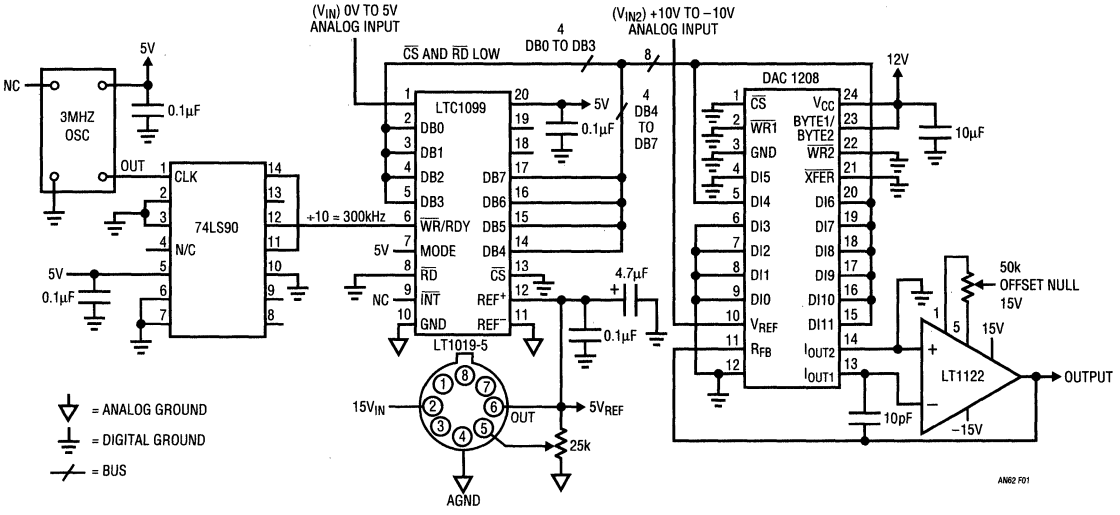


Figure 1. Two-Quadrant 150kHz Bandwidth Analog Multiplier

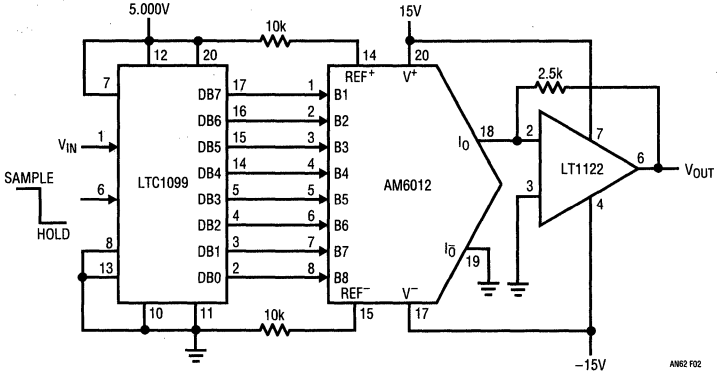


Figure 2. Infinite Hold Time Sample-and-Hold (t_{ACQ} = 240ns)

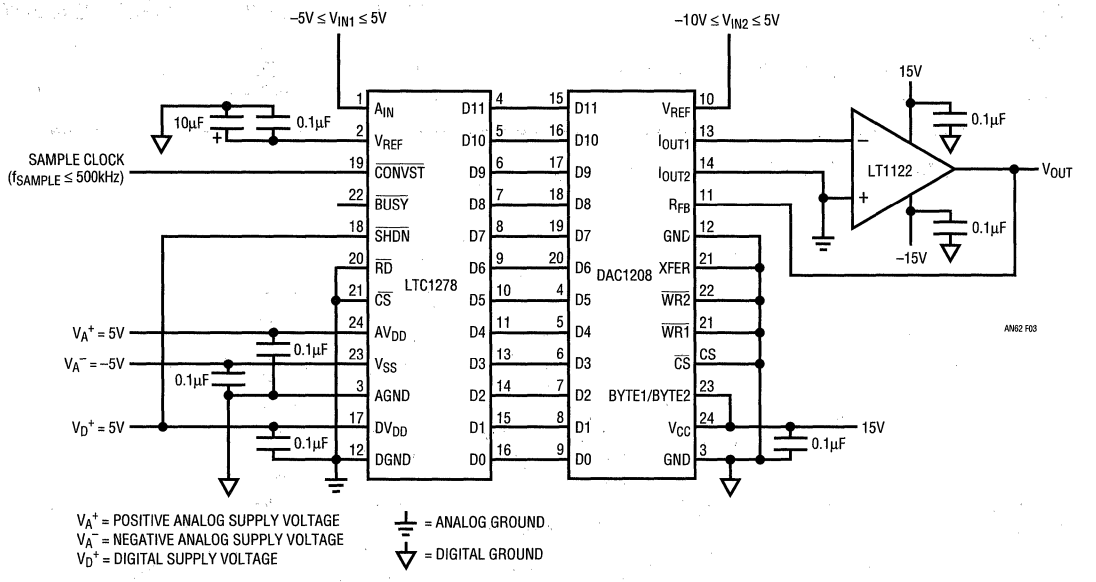


Figure 3. Four-Quadrant 250kHz Bandwidth Analog Multiplier

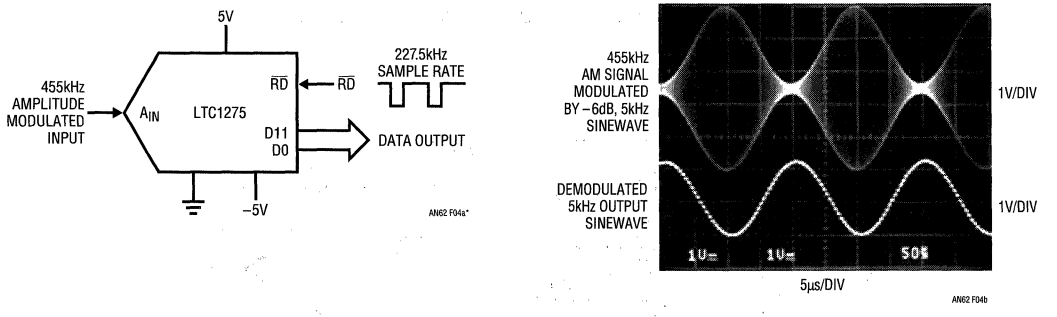
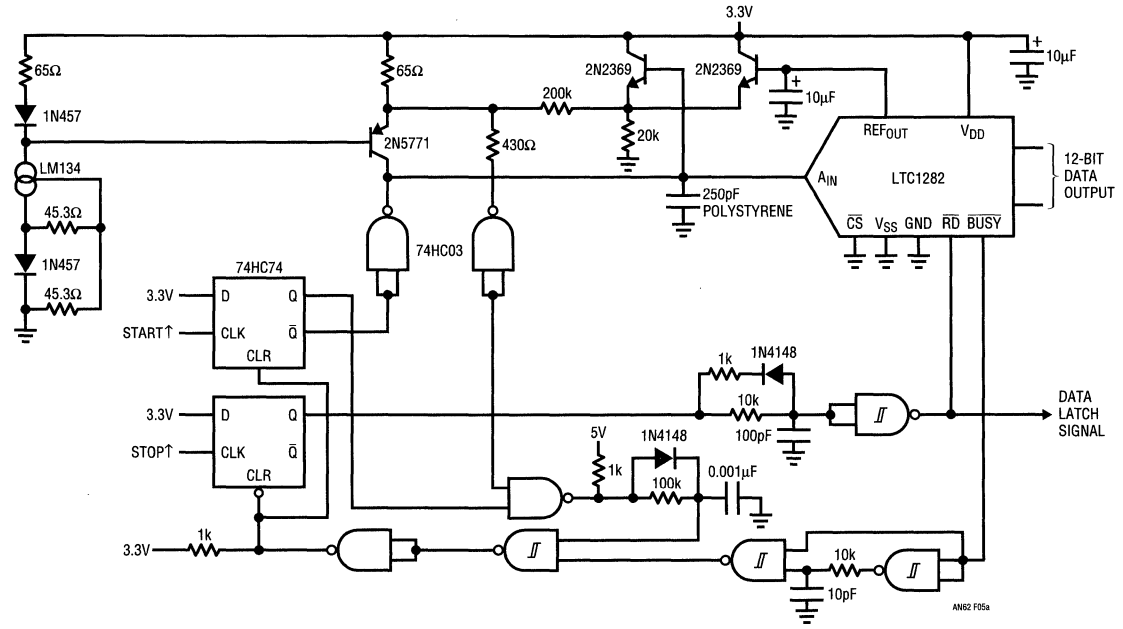
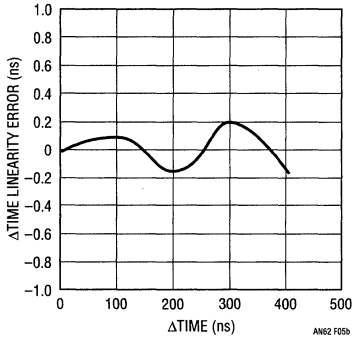
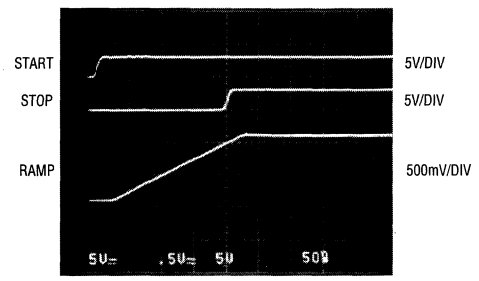


Figure 4. Demodulating a Signal Using Undersampling







THE PHOTO SHOWS THE START, STOP AND RAMP WAVEFORMS FOR A HALF SCALE, 200ns INPUT. THE RAMP REACHES 2.5V IN 400ns FOR A FULL-SCALE ADC INPUT. THE 4096 CODES SPREAD OVER 400ns EQUATE TO 100ps PER LSB.

Figure 5. Complete 100ps Resolution ΔTime Circuit with "Bow" Correction

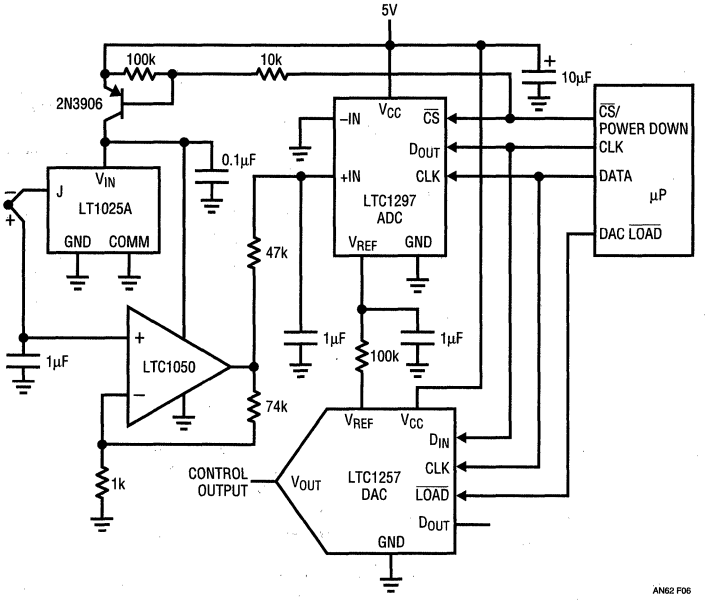


Figure 6. Single 5V 12-Bit Temperature Control System with Shutdown

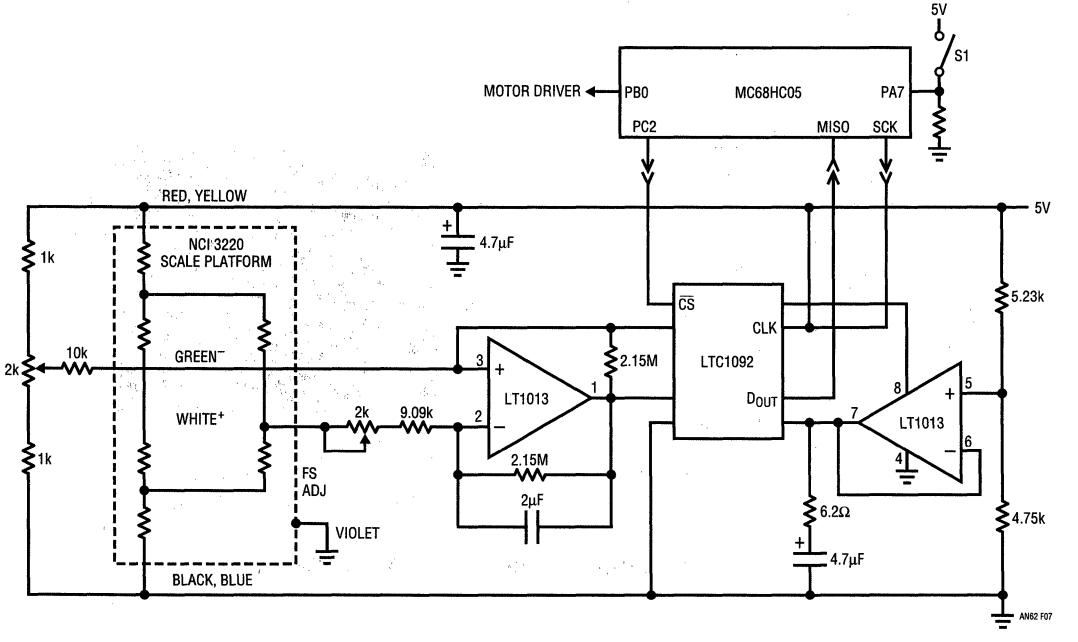
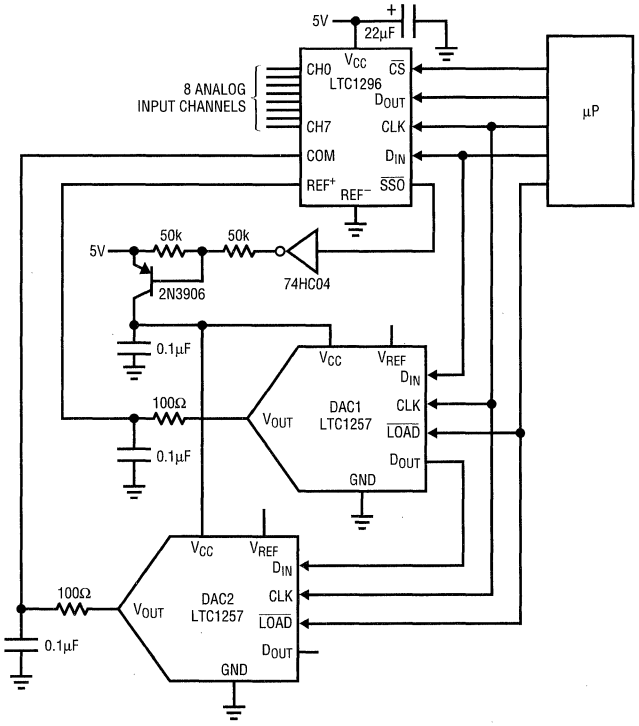


Figure 7. Weight Scale



NOTE: THE µP SETS THE LTC1296's FULL-SCALE AND ZERO-SCALE MAGNITUDES WITH THE CODE APPLIED TO DAC1 AND DAC2, RESPECTIVELY.

AN62 F08

Figure 8. Auto-Ranging 8-Channel 12-Bit Data Acquisition System with Shutdown

ANALOG-TO-DIGITAL BATTERY MONITORING APPLICATION CIRCUITS

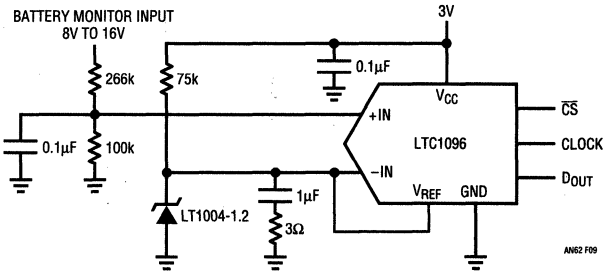


Figure 9. Micropower Battery Voltage Monitor

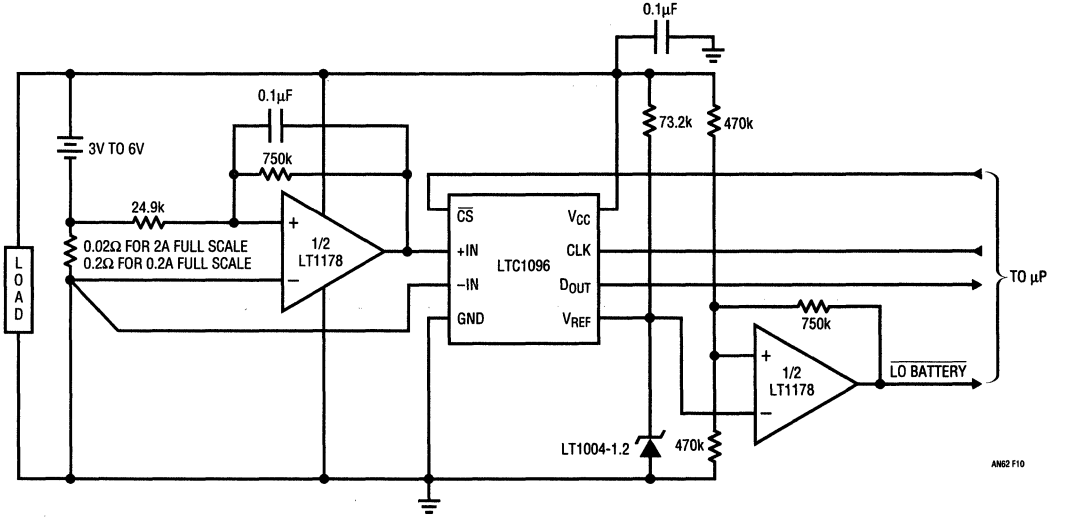


Figure 10. 0A to 2A Battery Current Monitor Draws Only 70µA

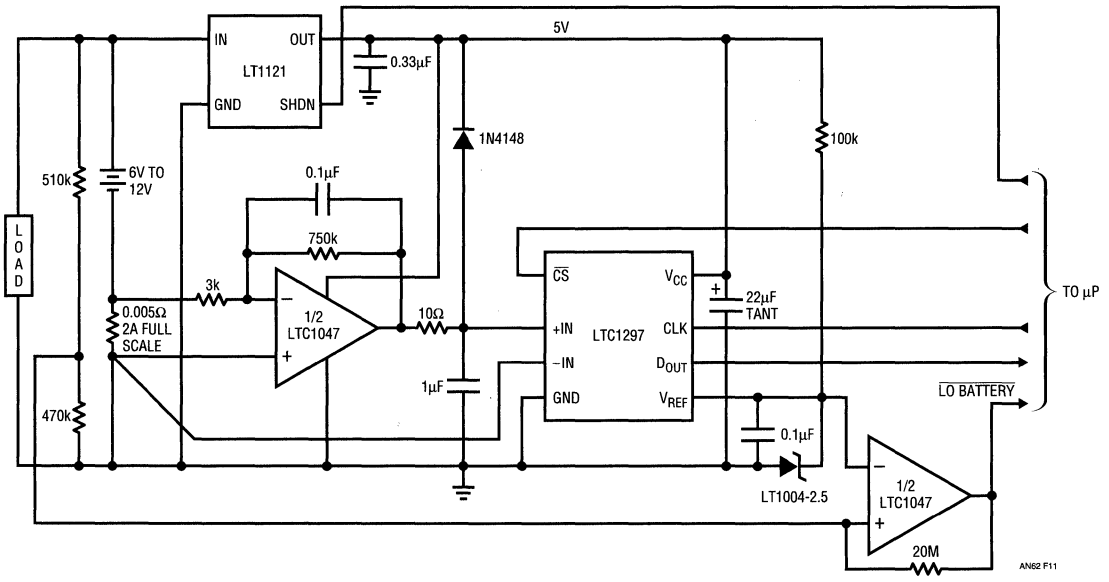


Figure 11. LTC1297 Data Acquisition System Micropower Battery Current Monitor

TEMPERATURE SENSING AND CONVERSION

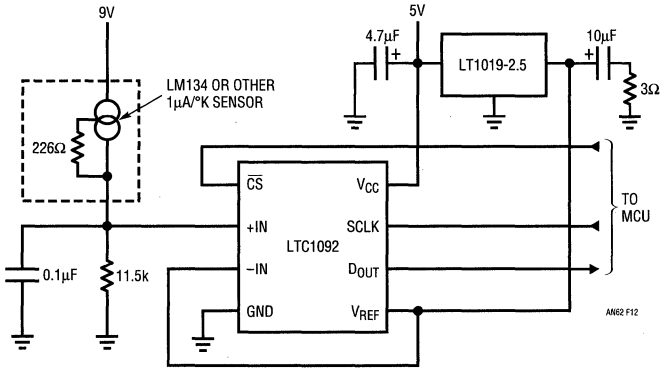


Figure 12. Current Output Silicon Sensor Thermometer Driving 10-Bit Analog-to-Digital Converter Covers –55°C to 125°C with 0.2°C Resolution

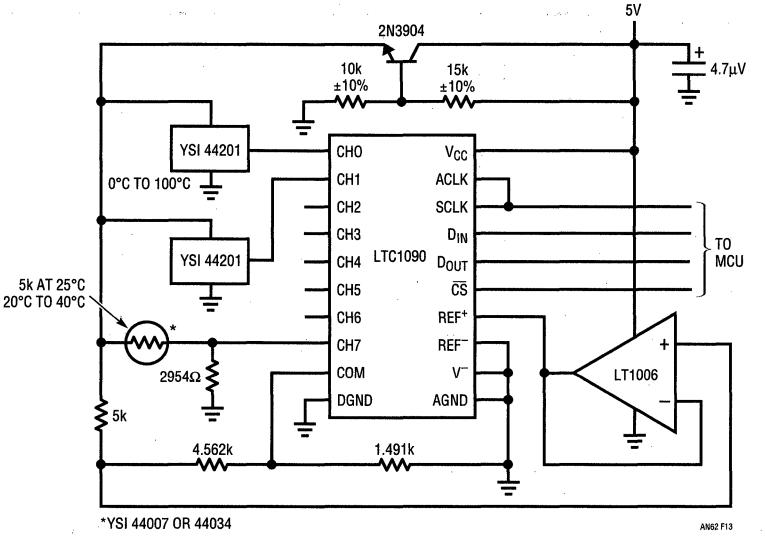


Figure 13. Thermistor-Based Temperature Measurement System Covers 20°C to 40°C and 0°C to 100°C with 0.25°C Accuracy

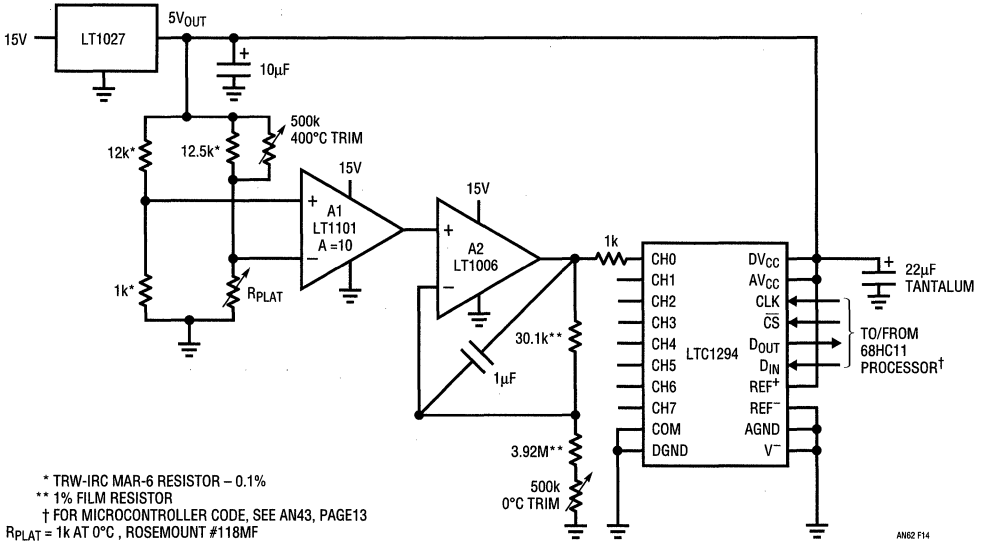


Figure 14. Digitally Linearized Platinum RTD Signal Conditioner

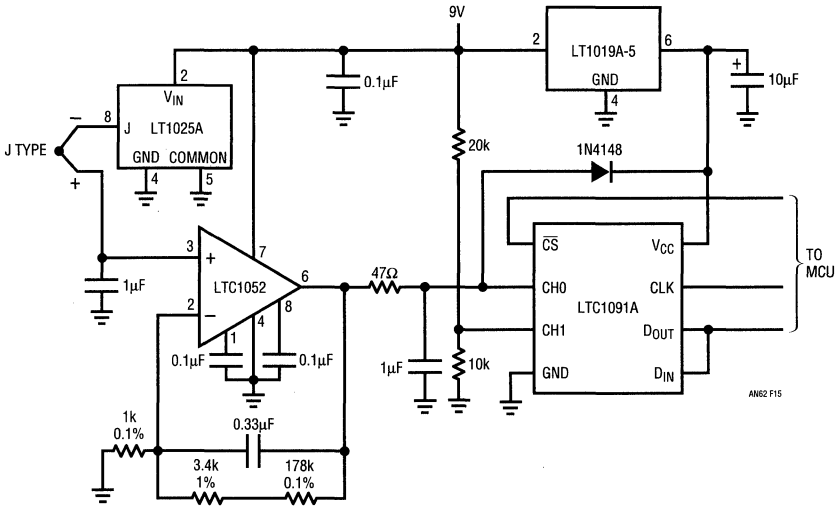


Figure 15. Furnace Exhaust Gas Temperature Monitor Covers 0°C to 500°C and Has Low Supply Detection

ISOLATED INTERFACES

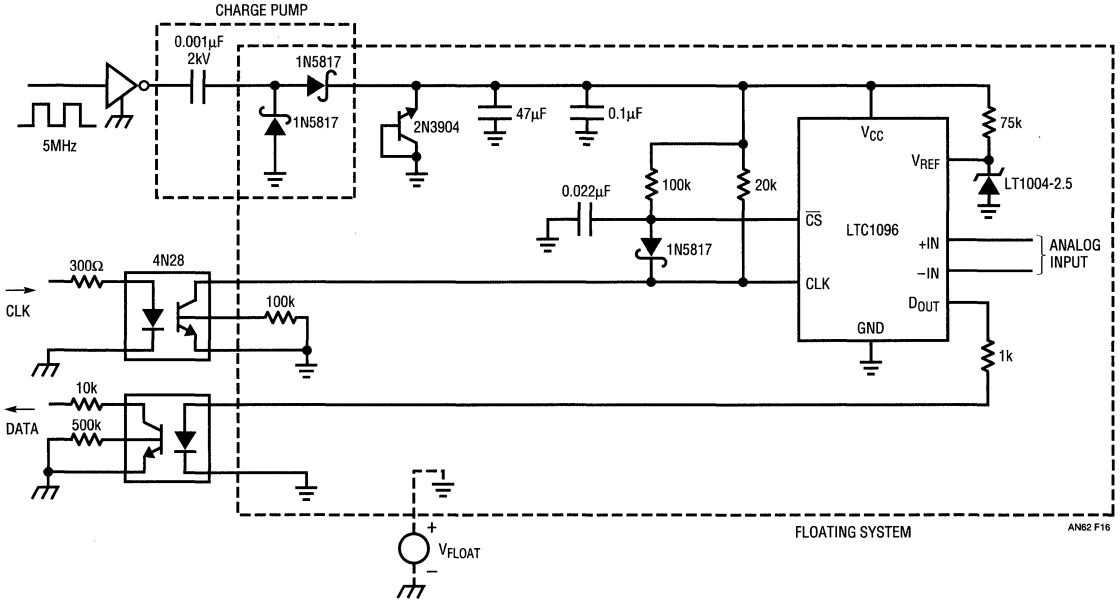


Figure 16. Floating Analog-to-Digital Conversion System Powered by Capacitor Charge Pump

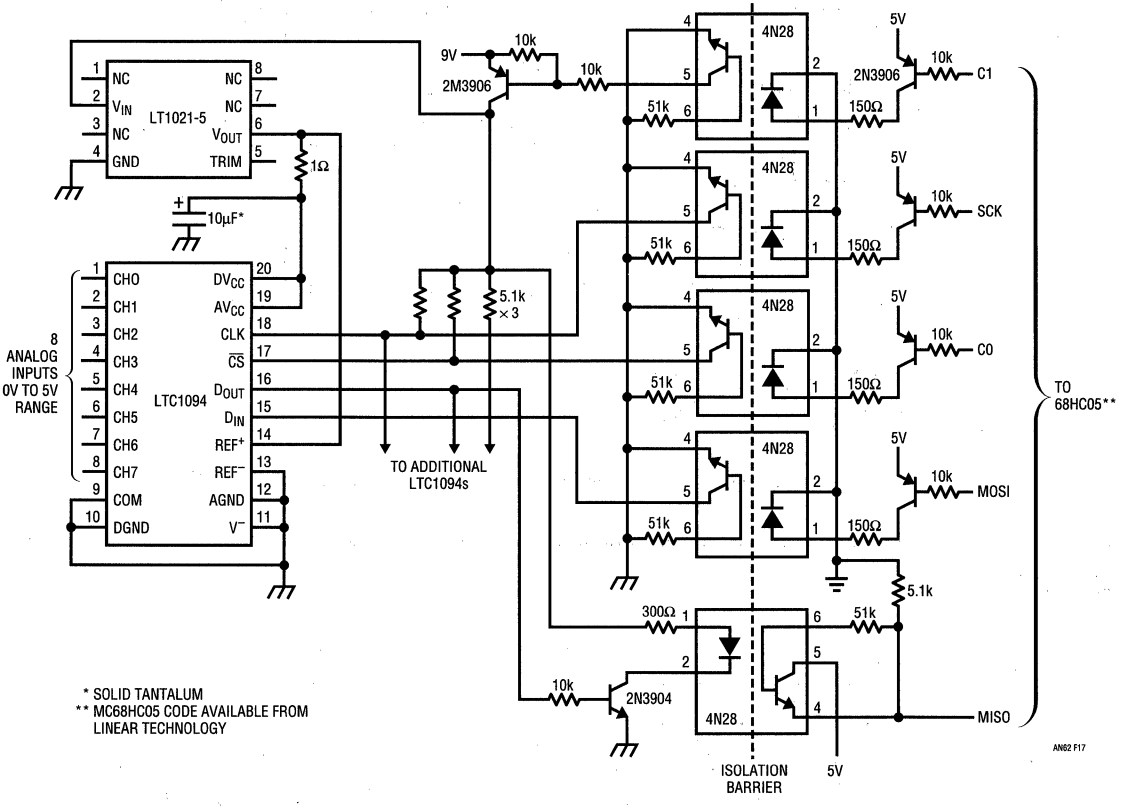


Figure 17. Micropower Serial 10-Bit Data Acquisition System with 500V Opto-Isolated Communication

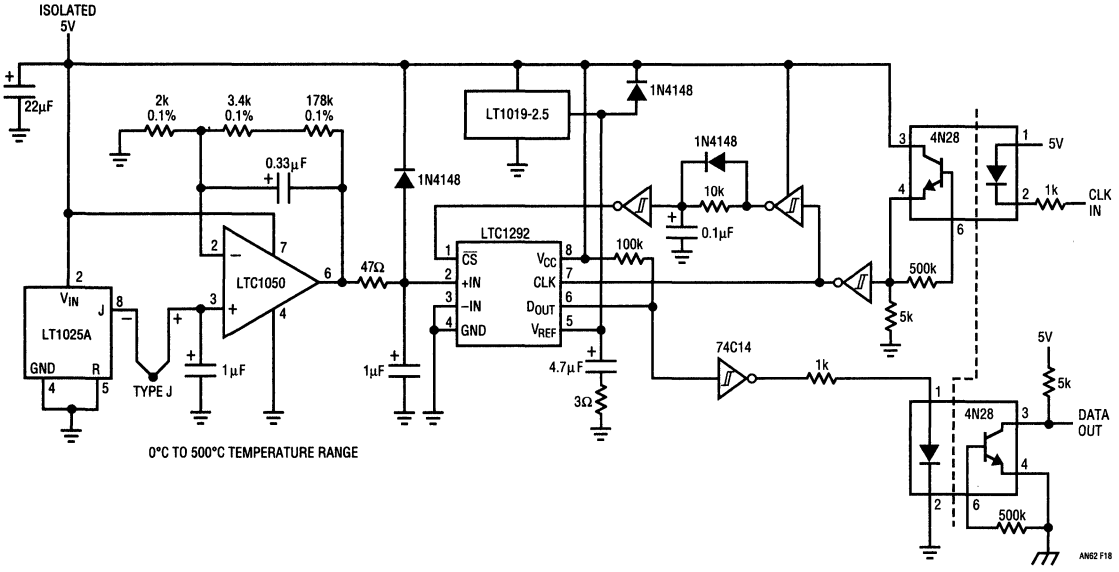


Figure 18. Opto-Isolated Temperature Monitor

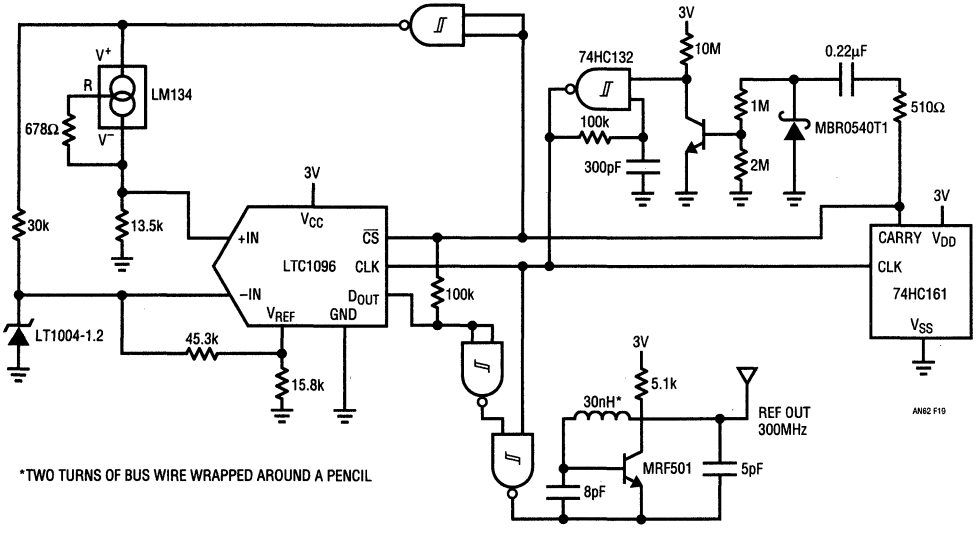
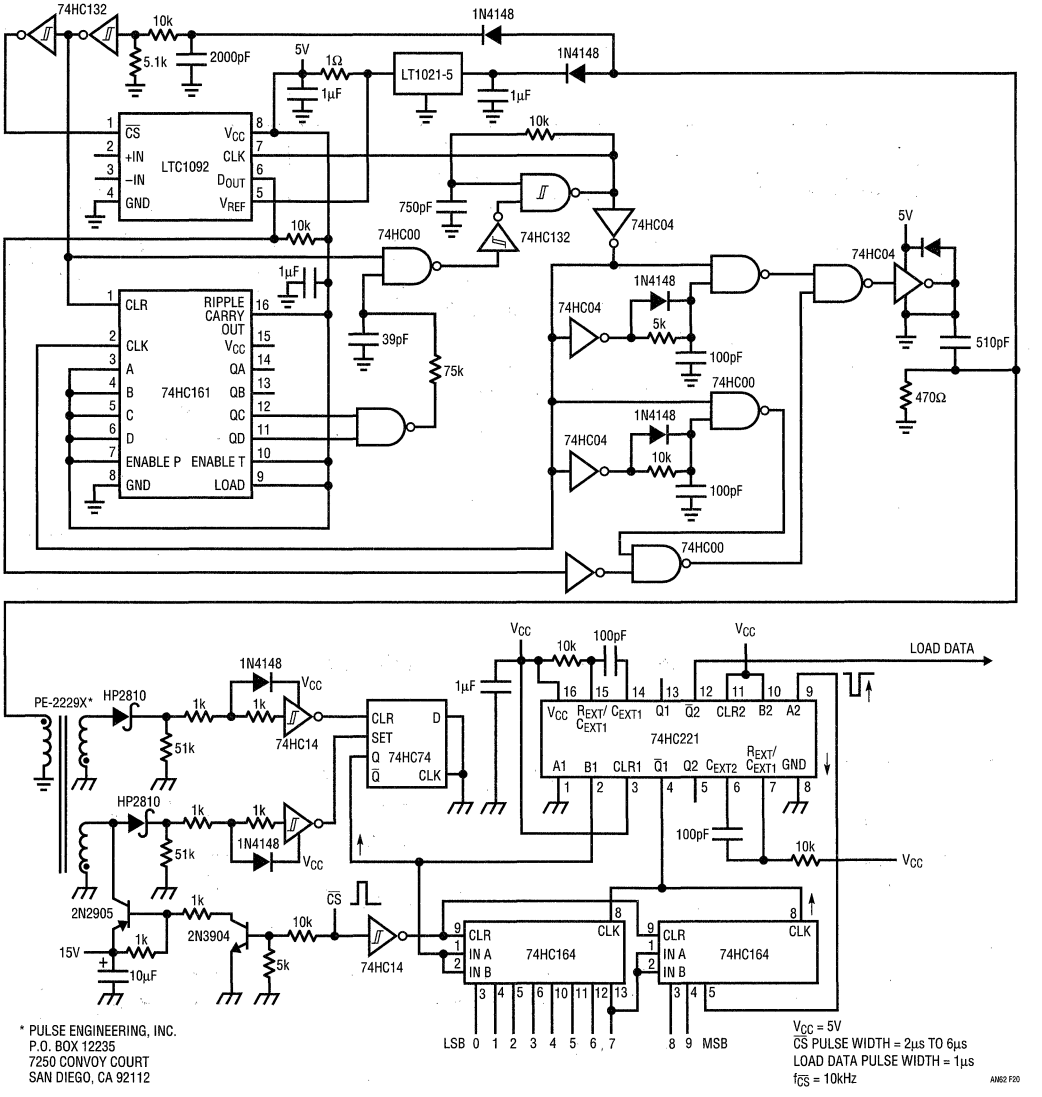


Figure 19. Battery-Powered Digital Thermometer Transmits Over RF-Link



TIMING DIAGRAM SHOWING PULSE-WIDTH CODING TECHNIQUE

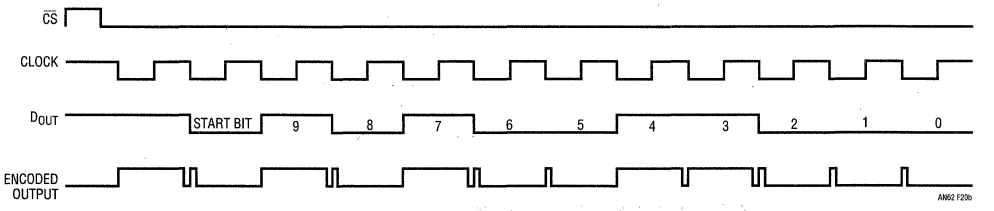


Figure 20. LTC1092 10-Bit Analog-to-Digital Converter Receives Power and Transmits Data Over Two Transformer-Isolated Lines

MISCELLANEOUS CIRCUITS

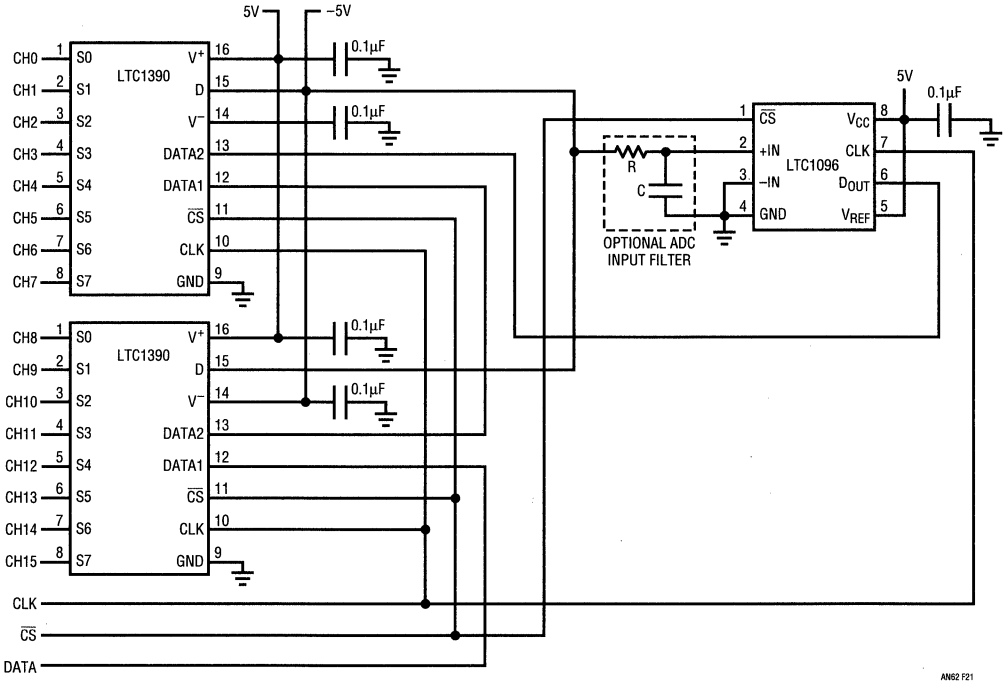


Figure 21. Two LTC1390 Cascadable Serially Programmed 8-Channel Multiplexers Provide the Single Channel LTC1096 with 16 Analog Inputs

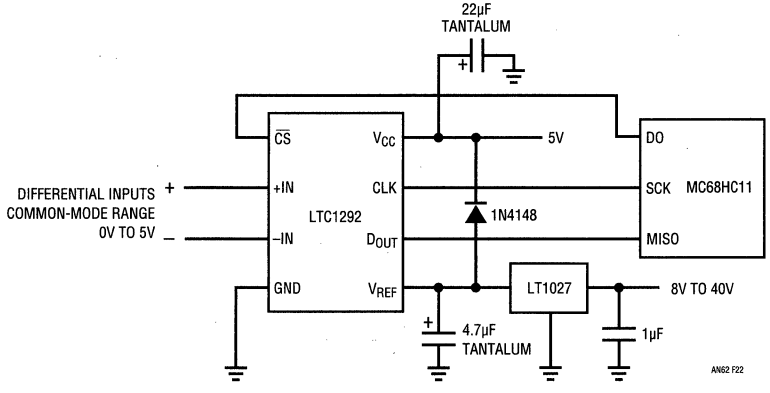


Figure 22. Small 12-Bit Differential-Input LTC1292 Data Acquisition System Occupies Only 0.35IN^2 Including Reference and Power Supply Bypass Components

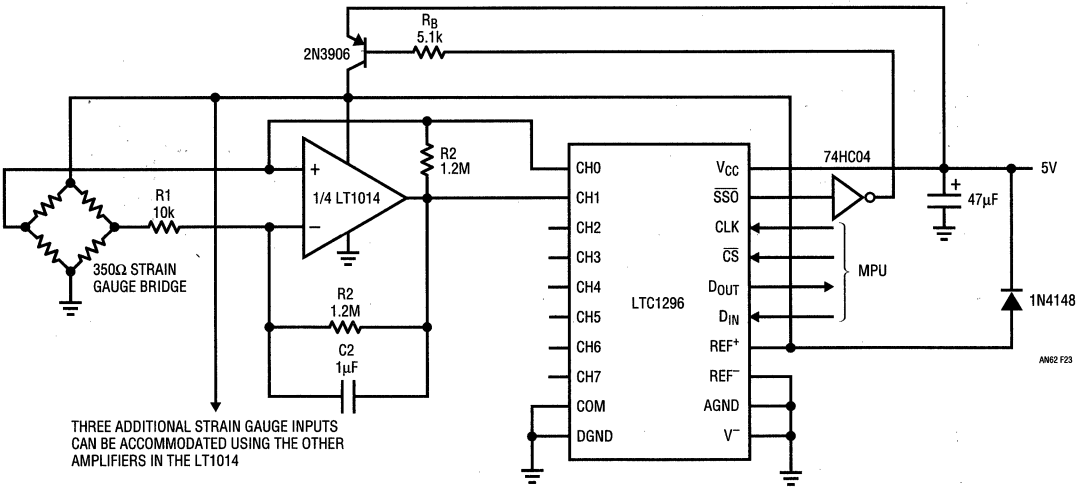


Figure 23. 12-Bit LTC1296 Data Acquisition System Strain Gauge with Bridge-Driver-Power Shutdown

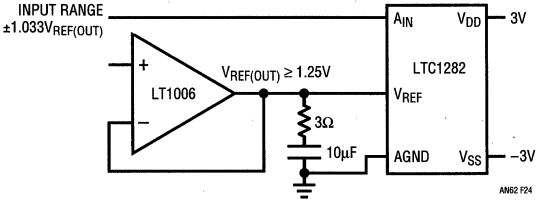


Figure 24. LTC1282 3V Analog-to-Digital Converter with Full-Scale Adjust

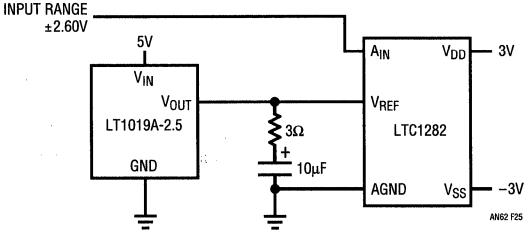


Figure 25. Ultra-Low Full-Scale Drift LTC1282 3V Analog-to-Digital Converter

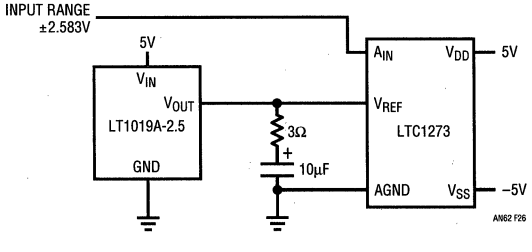


Figure 26. Ultra-Low Full-Scale Drift LTC1273 3V Analog-to-Digital Converter

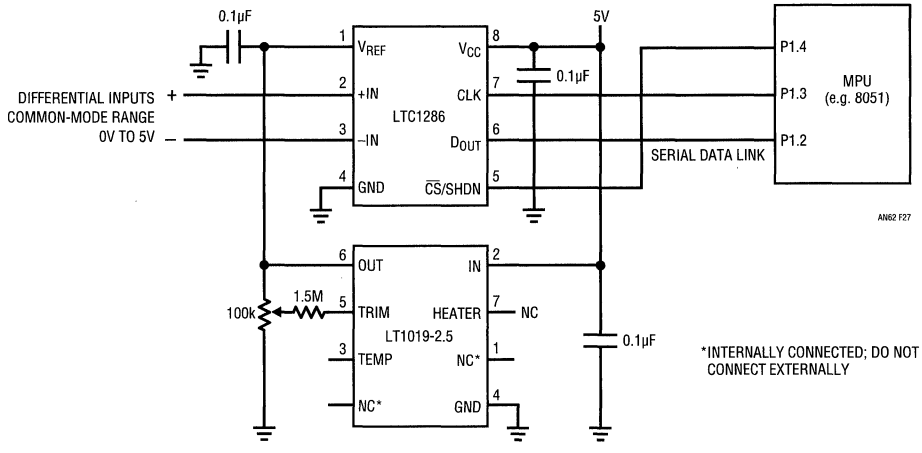


Figure 27. "Tiny" LTC1286 12-Bit Differential-Input Data Acquisition System (In SO Package) and "Tiny" LT1019-2.5 Reference Occupies Only 0.47IN^2 Including Reference and Power Supply Bypass Components

HARDWARE MICROCONTROLLER INTERFACES

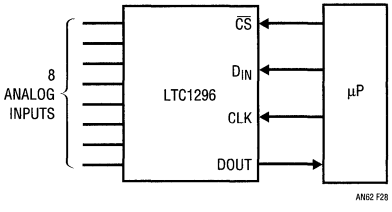


Figure 28. LTC1296 to Microcontroller Hardware Serial Interface

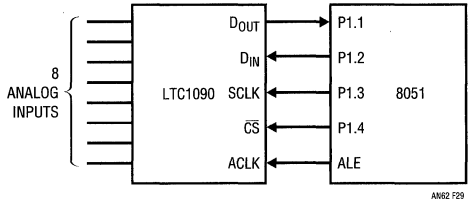


Figure 29. LTC1090* to Intel 8051 Microcontroller Hardware Serial Interface

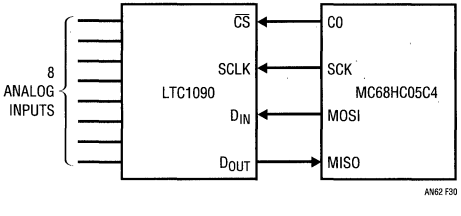


Figure 30. LTC1090* to Motorola MC68HC05C4 Microcontroller Hardware Serial Interface

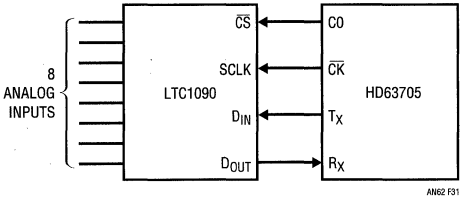


Figure 31. LTC1090* to Hitachi HD63705 Microcontroller Hardware Serial Interface

*Increase resolution from 10 bits to 12 bits with the pin compatible LTC1290.

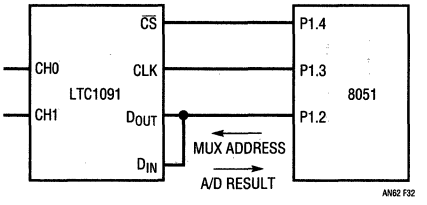


Figure 32. LTC1091* to Intel 8051 Microcontroller Hardware Serial Interface

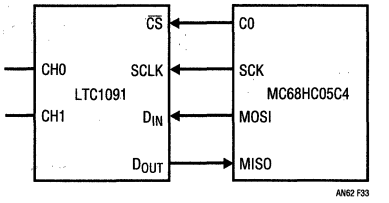


Figure 33. LTC1091* to Motorola MC68HC05C4 Microcontroller Hardware Serial Interface

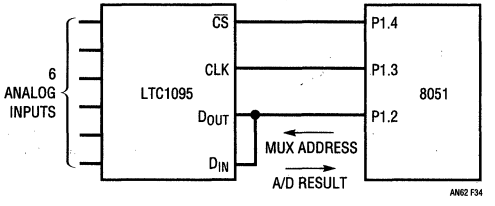


Figure 34. LTC1095 to Intel 8051 Microcontroller Hardware Serial Interface

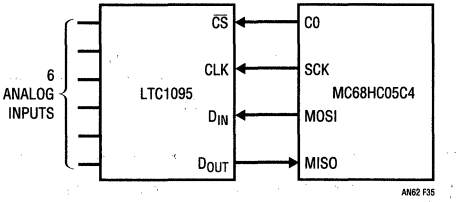


Figure 35. LTC1095 to Motorola MC68HC05C4 Microcontroller Hardware Serial Interface

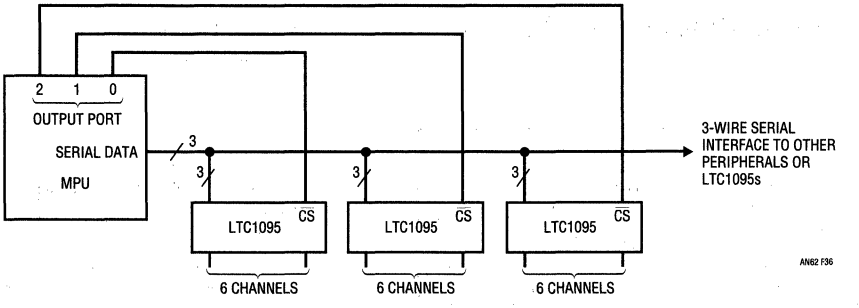


Figure 36. Multiple LTC1095s Sharing One Three-Wire Serial Interface

*Increase resolution from 10 bits to 12 bits with the pin compatible LTC1291.

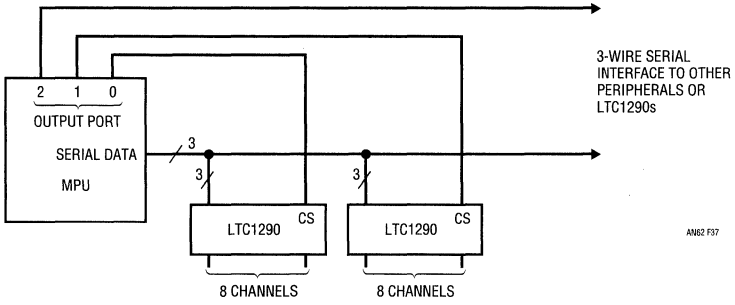


Figure 37. Multiple LTC1290s Sharing One Three-Wire Serial Interface

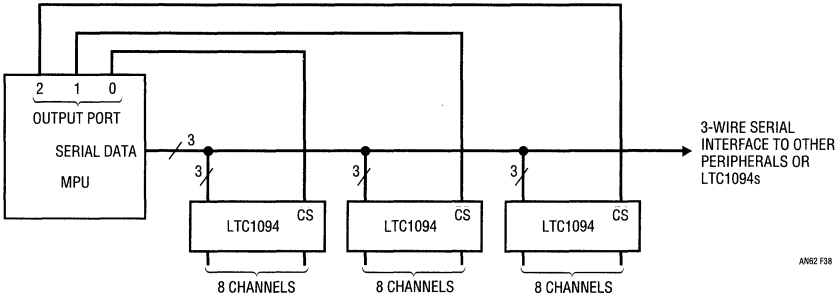


Figure 38. Multiple LTC1094s* Sharing One Three-Wire Serial Interface

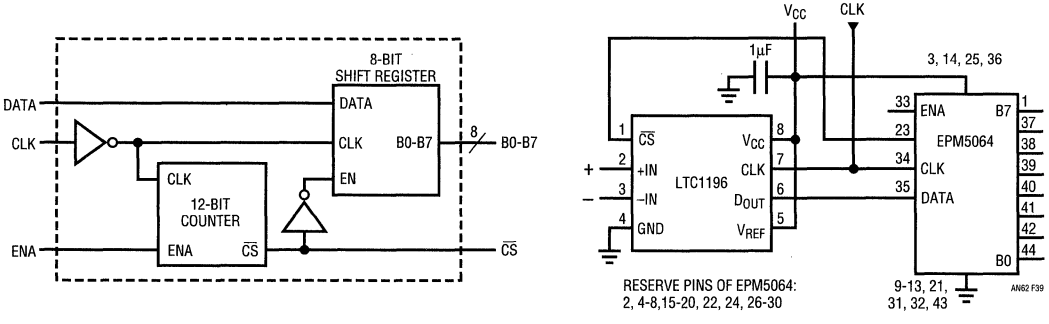


Figure 39. Interfacing the LTC1196 to the Altera EPM5064 PLD

*Increase resolution from 10 bits to 12 bits with the pin compatible LTC1294.

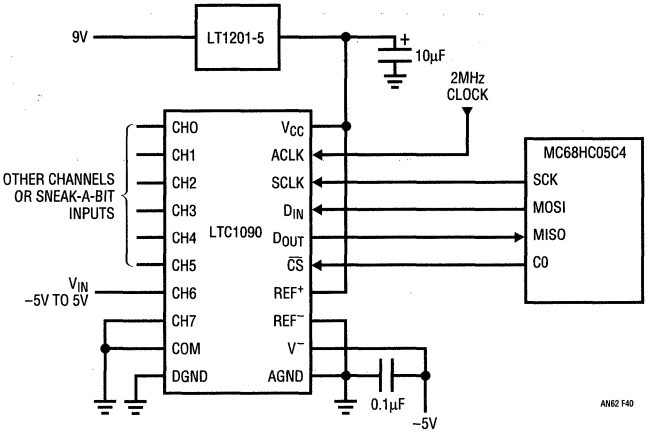


Figure 40. SNEAK-A-BIT Circuit for the LTC1090: 11-Bit Resolution from a 10-Bit ADC

PC SERIAL INTERFACE CIRCUITS

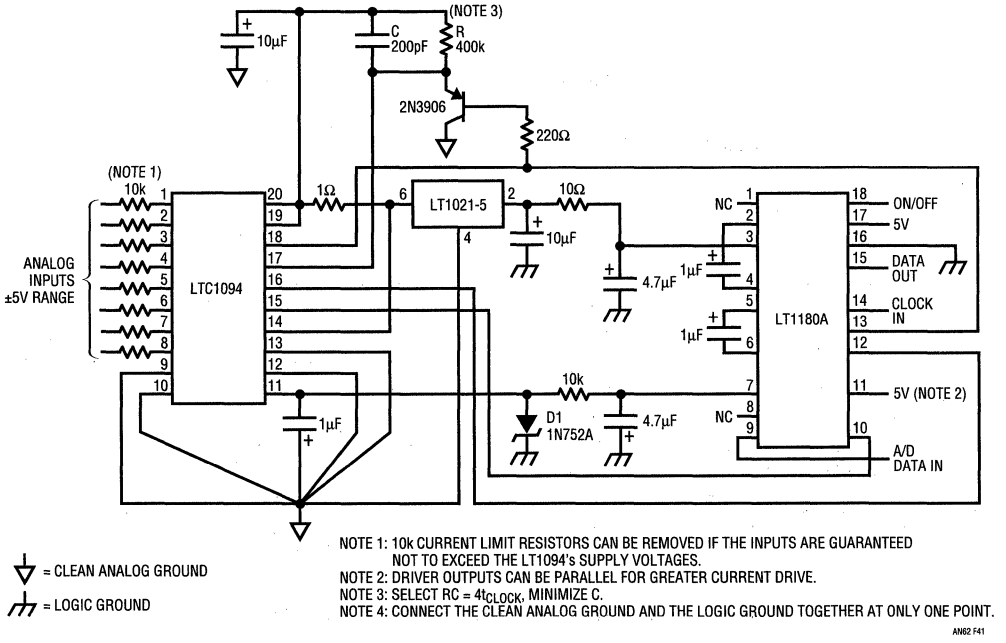


Figure 41. LTC1094 Analog-to-Digital Converter RS232 Serial Interface Using the LT1180A Dual Driver/Receiver

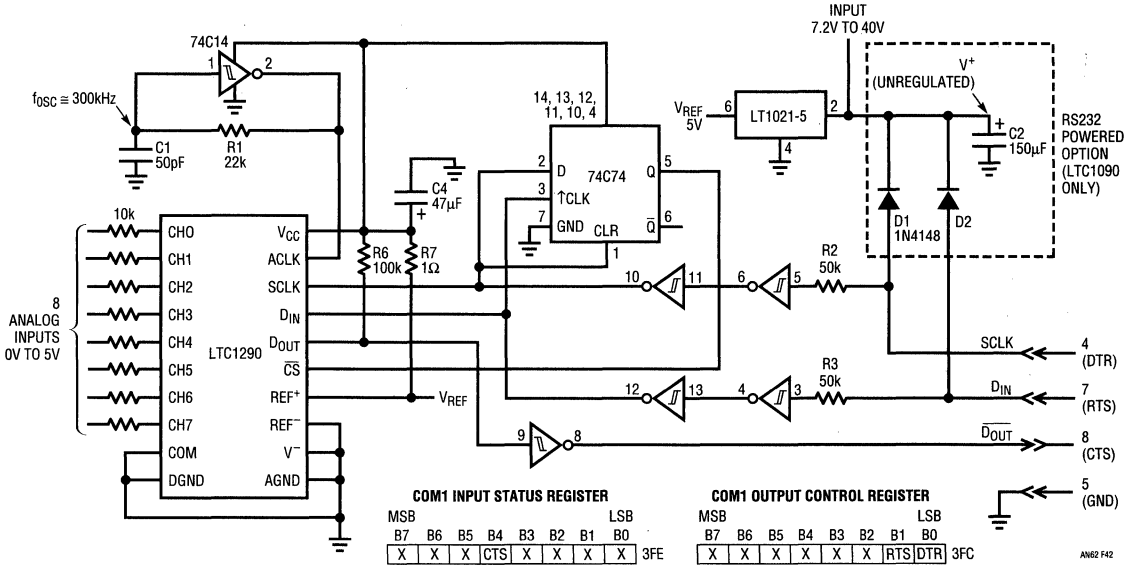


Figure 42. LTC1290 to IBM PC Serial Port

PARALLEL INTERFACE CIRCUITS

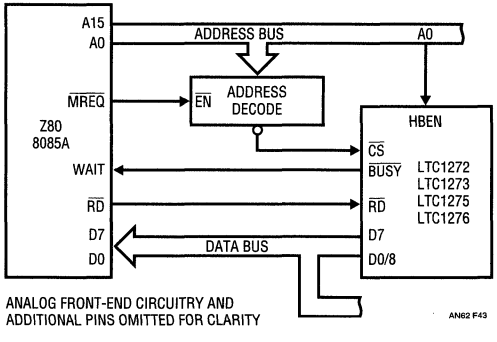


Figure 43. LTC1272/LTC1273/LTC1275/LTC1276 to 8085A/Z80 Microprocessor Hardware Parallel Interface

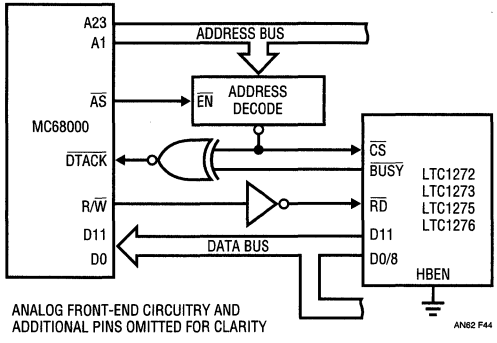


Figure 44. LTC1272/LTC1273/LTC1275/LTC1276 to MC68000 Microproessor Hardware Parallel Interface

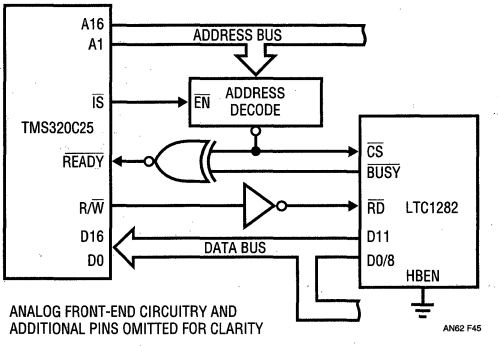


Figure 45. LTC1282 to TMS320C25 DSP Processor Parallel Interface

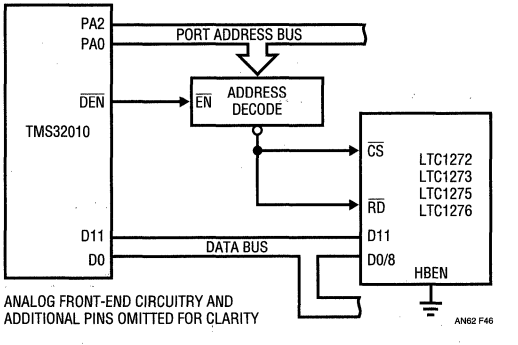


Figure 46. LTC1272/LTC1273/LTC1275/LTC1276 to TMS32010 DSP Processor Parallel Interface

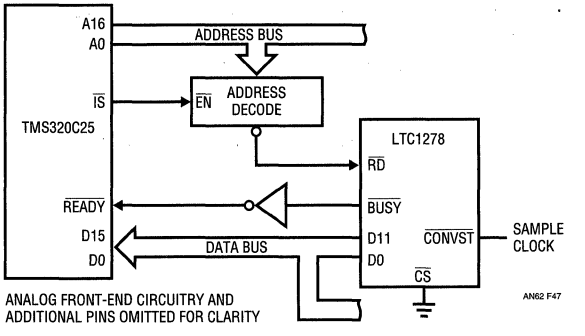


Figure 47. LTC1278 to TMS320C25 DSP Processor Parallel Interface

REFERENCE CIRCUITS

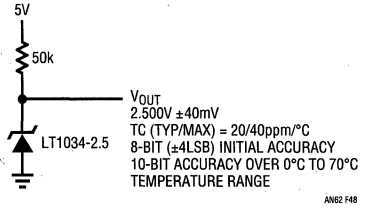


Figure 48. LT1034-2.5 2.5V Voltage Reference

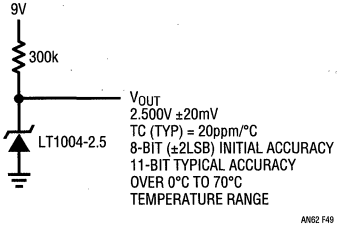


Figure 49. Battery-Powered LT1004-2.5 2.5V Voltage Reference

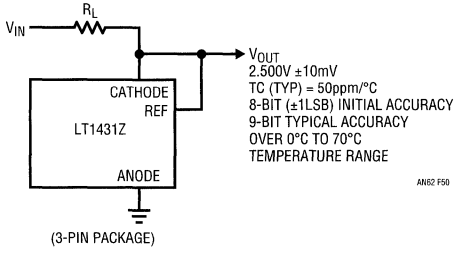


Figure 50. LT1431Z 2.5V Voltage Reference (3-Pin Package)

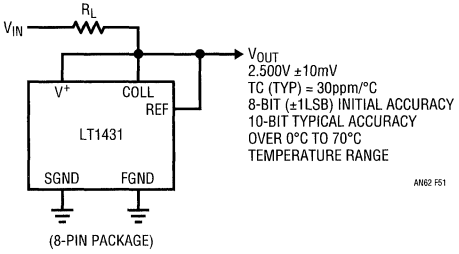


Figure 51. LT1431 2.5V Voltage Reference (8-Pin Package)

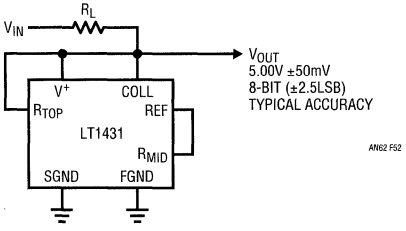


Figure 52. LT1431Z 5V Voltage Reference (8-Pin Package)

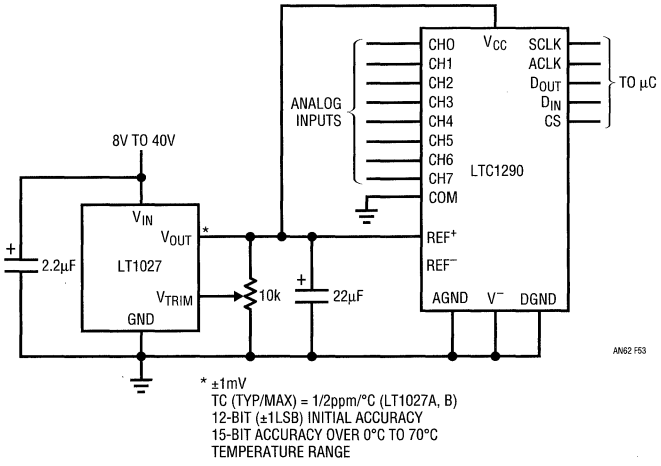


Figure 53. LT1027 12-Bit Accurate 5V Voltage Reference Supplying Input Voltages to the LTC1290's V_{REF} and V_{CC} Pins

ADJUSTABLE REFERENCES

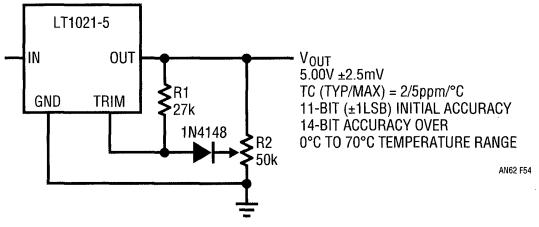


Figure 54. LT1021-5 Adjustable 5V Voltage Reference

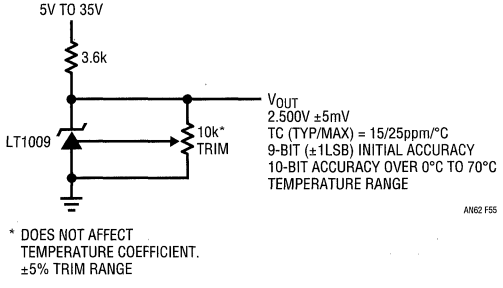
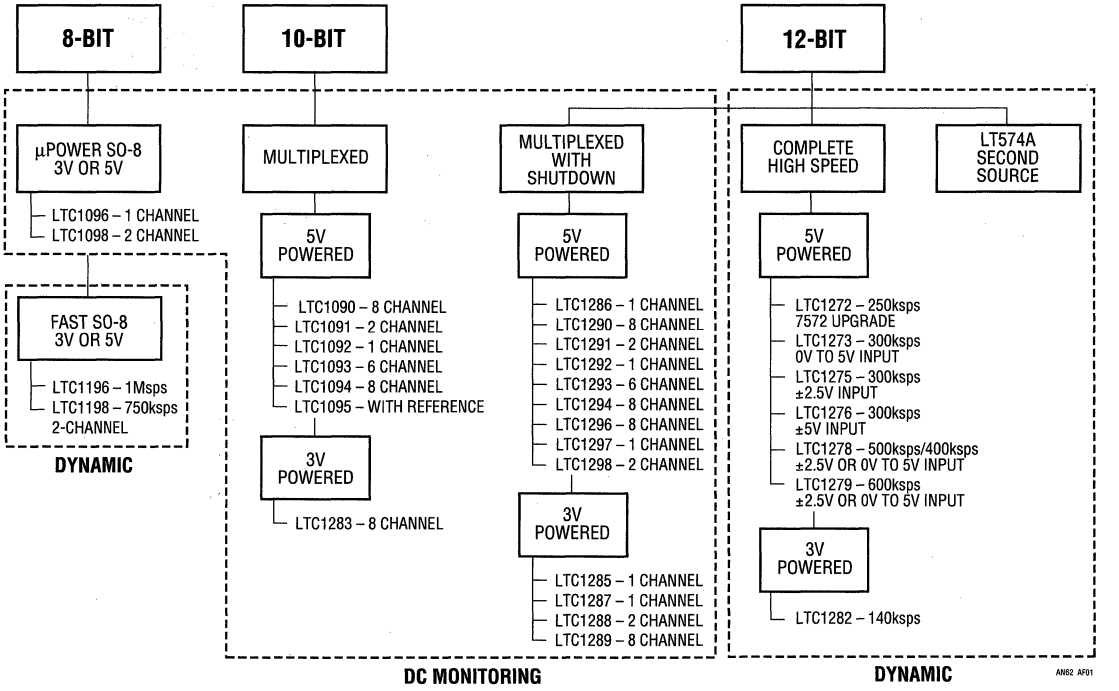


Figure 55. LT1009 2.5V Voltage Reference with ±5% Trim Range

APPENDIX A



Analog-to-Digital Converter Selection Guide

PART NUMBER	DESCRIPTION	RESOLUTION	TOTAL UNADJUSTED ERROR	SAMPLE RATE	VOLTAGE SUPPLY	MAXIMUM SUPPLY CURRENT	PKGS AVAIL	IMPORTANT FEATURES
LTC1090C,M	10-Bit, Serial I/O, A/D Converter with 8-Channel Multiplexer. Full Duplex Serial Interface.	10 Bits	±0.5LSB (LTC1090A) Over Full Temperature Range	35ksps	5V, 10V, or ±5V	2.5mA	J, N, S	10-Bit ADC with Built-In 8-Channel Analog MUX and Sample-and-Hold. Compatible with All Microprocessors' Serial Ports. Software Configuable Bipolar or Unipolar Operation. Full Duplex Serial I/O.
LTC1091C,M	10-Bit, 8-Pin Serial I/O, A/D Converter with 2-Channel Analog Multiplexer.	10 Bits	±0.5LSB (LTC1091A) Over Full Temperature Range	31ksps	5V or 10V	3.5mA	J8, N8	10-Bit ADC with Built-In 2-Channel Analog MUX and Sample-and-Hold. Compatible with All Microprocessors' Serial Ports. Unipolar Operation.
LTC1092C,M	10-Bit, 8-Pin, A/D Converter with Serial Output.	10 Bits	±0.5LSB (LTC1092A) Over Full Temperature Range	38ksps	5V or 10V	2.5mA	J8, N8	Separate Reference Pin Allows Reduced Span (Down to 220mV) Operation. Unipolar ADCs Are Performed on a Differential Input Pair. Compatible with All Microprocessors' Serial Ports.
LTC1093C,M	10-Bit, Serial I/O, A/D Converter with 6-Channel Multiplexer.	10 Bits	±0.5LSB (LTC1093A) Over Full Temperature Range	26ksps	5V, 10V, or ±5V	2.5mA	J, N, S	1-Bit ADC with Built-In 6-Channel Analog MUX and Sample-and-Hold. Compatible with All Microprocessors' Serial Ports. Software Configurable Bipolar or Unipolar Operation. Half Duplex Serial I/O.

PART NUMBER	DESCRIPTION	RESOLUTION	TOTAL UNADJUSTED ERROR	SAMPLE RATE	VOLTAGE SUPPLY	MAXIMUM SUPPLY CURRENT	PKGS. AVAIL.	IMPORTANT FEATURES
LTC1094C,M	10-Bit, Serial I/O. A/D Converter System with 8-Channel Multiplexer.	10 Bits	±0.5LSB (LTC1094A) Over Full Temperature Range	26ksps	5V, 10V, or ±5V	2.5mA	J, N	10-Bit ADC with Built-In 8-Channel Analog MUX and Sample-and-Hold. Compatible with All Microprocessors' Serial Ports. Software Configurable Bipolar or Unipolar Operation. Half Duplex Serial I/O.
LTC1095C,M	10-Bit, Serial I/O, A/D Converter with 6-Channel Multiplexer and 5V Buried Zener Reference.	10 Bits	±0.15% FSR	26ksps	7.2V to 10V	3.7mA	J	10-Bit ADC with Built-In 6-Channel Analog MUX, Sample-and-Hold, and 5V Buried Zener Reference. Compatible with All Microprocessors' Serial Ports. Software Configurable Bipolar or Unipolar Operation. Half Duplex Serial I/O.
LTC1096C	8-Bit, 16µs, Micropower, Sampling A/D Converter with Serial I/O and Differential Input.	8 Bits	±0.5LSB (LTC1096A) Over Full Temperature Range	33ksps	3V to 9V	180µA, 3µA During Shutdown	N8, S8	Single Differential Input, Sample-and-Hold with Single-Ended Inputs. Ultra-Low Power, Automatic Power-Down Mode.
LTC1098C	8-Bit, 16µs, Micropower, Sampling A/D Converter with Serial I/O and 2-Channel MUX.	8 Bits	±0.5LSB (LTC1098A) Over Full Temperature Range	33ksps	3V to 9V	230µA, 3µA During Shutdown	N8, S8	2-Channel Multiplexer, Sampling ADC. Ultra-Low Power, Automatic Power-Down Mode.
LTC1099C,M	8-Bit, 2µs A/D Converter with Built-in Sample-and-Hold. Parallel Output.	8 Bits	±1LSB Over Full Temperature Range	256ksps	5V	15mA	J, N, S	Built-in Sample-and-Hold Allows Direct Conversion of $5V_{P-P}$ Signals up to 156kHz. Pin Compatible with ADC0820 and AD7820.
LTC1196C	8-Bit, 8-Pin, Serial I/O, 600ns, 1MHz, Sampling A/D Converter with Automatic Power-Down.	8 Bits	±0.5LSB Over Full Temperature Range	1Msps	3V to 6V	10mA	N, S	8-Bit ADC with Built-In Sample-and-Hold. Compatible with All Microprocessors' Serial Ports. Full Duplex Serial I/O.
LTC1198C	8-Bit, 8-Pin, Serial I/O, 600ns, 750kHz, Sampling A/D Converter with 2-Channel Analog MUX and Automatic Power-Down.	8 Bits	±0.5LSB Over Full Temperature Range	750ksps	3V to 6V	10mA, 3µA During Shutdown	N, S	8-Bit ADC with Built-In Sample-and-Hold. Compatible with All Microprocessors' Serial Ports. Full Duplex Serial I/O. 2-Channel Analog MUX and Automatic Power-Down.
LTC1272C,M	12-Bit, 3µs, 250ksps Sampling A/D Converter with Parallel Output. Single 5V Supply. Input Range: $0V \le V_{IN} \le 5V$.	12 Bits	±0.5LSB Linearity, ±1LSB Differential Nonlinearity, and ±4LSB Offset Error Over Full Temperature Range. ±10LSB Full-Scale Error. 72dB SINAD and –82dB THD at f_{IN} = 10kHz.	250ksps (111ksps also available)	5V	30mA	J, N, S	Single Supply 12-Bit ADC with Built-In Sample-and-Hold and 250ksps Conversion Rate. Built-In 2.42V Reference. Plug-In Upgrade for AD7572. Operates with or without –15V Supply Required by AD7572.
LTC1273C,M	12-Bit, 2.7µs, 300ksps Sampling A/D Converter with Parallel Output. Single 5V Supply. Input Range: $0V \le V_{IN} \le 5V$.	12 Bits	±0.5LSB Linearity, ±0.75LSB Differential Nonlinearity, and ±4LSB Offset Error Over Full Temperature Range. ±10LSB Full-Scale Error. 70dB SINAD and –74dB THD at f_{IN} = 150kHz.	300ksps	5V	25mA	J, N, S	Single Supply 12-Bit ADC with Built-In Sample-and-Hold, Internal Clock, and 300ksps Conversion Rate. Built-In 2.42V Reference.
LTC1275C	12-Bit, 2.7µs, 300ksps, Sampling A/D Converter with Parallel Output. Split ±5V Supply. Input Range: $-2.5V \le V_{IN} \le 2.5V$.	12 Bits	±0.5LSB Linearity, ±0.75LSB Differential Nonlinearity, and ±4LSB Offset Error Over Full Temperature Range. 70dB SINAD and –74dB THD at f_{IN} = 150kHz. ±10LSB Full-Scale Error.	300ksps	±5V	25mA	N, S	Split Supply 12-Bit ADC with Built-In Sample-and-Hold, Internal Clock, and 300ksps Conversion Rate. Built-In 2.42V Reference.

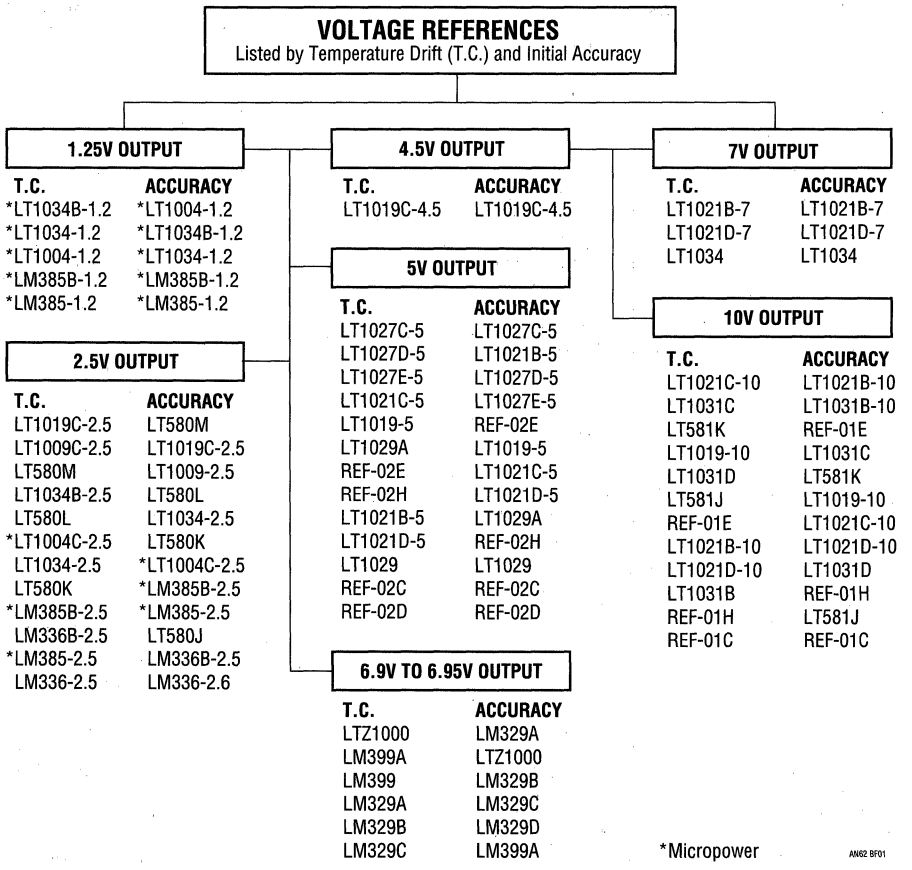
PART NUMBER	DESCRIPTION	RESOLUTION	TOTAL UNADJUSTED ERROR	SAMPLE RATE	VOLTAGE SUPPLY	MAXIMUM SUPPLY CURRENT	PKGS. AVAIL.	IMPORTANT FEATURES
LTC1276C	12-Bit, 2.7µs, 300ksps Sampling A/D Converter with Parallel Output. Split ±5V Supply. Input Range: $-5V \le V_{IN} \le 5V$.	12 Bits	±0.5LSB Linearity, ±0.75LSB Differential Nonlinearity, and ±4LSB Offset Error Over Full Temperature Range. 70dB SINAD and –74dB THD at f_{IN} = 150kHz. ±10LSB Full-Scale Error.	300ksps	±5V	25mA	N, S	Split Supply 12-Bit ADC with Built-In Sample-and-Hold, Internal Clock, and 300ksps Conversion Rate. Built-In 2.42V Reference.
LTC1278C,I	12-Bit, 1.6µs, 500ksps Sampling A/D Converter with Parallel Output. Input Range with Split ±5V Supply: $-2.5V \le V_{IN} \le 2.5V$; with 5V Supply: $0V \le V_{IN} \le 5V$.	12 Bits	±1LSB Linearity, ±1LSB Differential Nonlinearity, and ±6LSB Offset Error Over Full Temperature Range. 70dB SINAD and –74dB THD at f_{IN} = 250kHz. ±15LSB Gain Error.	500ksps (400ksps also available)	5V or ±5V	30mA, 3mA During Shutdown	N, S	Single or Split Supply 12-Bit ADC with Built-In Sample-and-Hold, Internal Clock, and 500ksps Conversion Rate. Built-In 2.42V Reference. Guaranteed 70dB SINAD and –78 THD at 100kHz Input Frequency Over Temperature.
LTC1279C,I	12-Bit, 1.4µs, 600ksps Sampling A/D Converter with Parallel Output. Input Range with 5V Supply: $0V \le V_{IN} \le 5V$; with Split ±5V Supply: $-2.5V \le V_{IN} \le 2.5V$.	12 Bits	±1LSB Linearity, ±1LSB Differential Nonlinearity, and ±6LSB Offset Error Over Full Temperature Range. 70dB SINAD and –74dB THD at f_{IN} = 300kHz. ±15LSB Gain Error.	600ksps	5V or ±5V	20mA, 3mA During Shutdown	N, S	Single or Split Supply 12-Bit ADC with Built-In Sample-and-Hold, Internal Clock, and 600ksps Conversion Rate. Built-In 2.42V Reference. Guaranteed 70dB SINAD and –78dB THD at 100kHz Input Frequency Over Temperature.
LTC1282C	12-Bit, 6µs, 140ksps Sampling A/D Converter with Parallel Output. Input Range with Single 3V Supply: $0V \le V_{IN} \le 2.5V$; with Split ±3V Supply: $-1.25V \le V_{IN} \le 1.25V$.	12 Bits	±0.5LSB Linearity, ±0.75LSB Differential Nonlinearity, and ±4LSB Offset Error Over Full Temperature Range. 69dB SINAD and –77dB THD at f_{IN} = 70kHz. ±10LSB Full-Scale Error.	140ksps	3V or ±3V	8mA	N, S	Single or Split Supply 12-Bit ADC with a 2.7V Guaranteed Minimum Supply Voltage. Complete with Sample-and-Hold, Internal Clock and a 25ppm/°C 1.2V Reference.
LTC1283C	10-Bit, 44µs, 3.3V or ±3.3V Sampling A/D Converter with Serial Output. Input Range with Split ±3.3V Supply: $-2.5V \le V_{IN} \le 2.5V$; with 3.3V Supply: $0V \le V_{IN} \le 2.5V$.	10 Bits	±0.5LSB Linearity and ±0.5LSB Offset Error Over Full Temperature Range.	15ksps	3.3V or ±3.3V	350µA	N, S	3.3V or ±3.3V Supply 10-Bit ADC with Built-In Sample-and-Hold. 10-Bit Unipolar or 9-Bit + Sign Bipolar Serial Output. Compatible with All Microprocessors' Serial Ports. Full Duplex Serial I/O.
LTC1285C	12-Bit, 8-Pin Serial I/O, 160µA (Typ) 3V Sampling A/D Converter with Automatic Power-Down and Differential Analog Input.	12 Bits	±2LSB Linearity, ±0.75LSB Differential Nonlinearity, ±3LSB Offset, and ±8LSB Full-Scale Error Over Full Temperature Range.	7.5ksps	3V	320µA, 3µA During Shutdown	N, S	12-Bit ADC with Built-In Sample-and-Hold. Operates on 3V Supply Voltage. Compatible with All Microprocessors' Serial Ports. Automatic Power-Down.
LTC1286C,I	12-Bit, 8-Pin Serial I/O, 250µA (Typ) Sampling A/D Converter with Automatic Power-Down.	12 Bits	±2LSB Linearity, ±0.75LSB Differential Nonlinearity, ±3LSB Offset, and ±8LSB Full-Scale Error Over Full Temperature Range.	12.5ksps	5V to 9V	500µA, 3µA During Shutdown	N, S	12-Bit ADC with Built-In Sample-and-Hold. Compatible with All Microprocessors' Serial Ports. Automatic Power Down.
LTC1287C,I	12-Bit, 33µs, 3.3V Sampling A/D Converter with Serial Output. Input Range with 3.3V Supply: $0V \le V_{IN} \le 3.3V$.	12 Bits	±0.5LSB Linearity, ±3LSB Offset, and ±0.5LSB Full-Scale Error Over Full Temperature Range.	30ksps	2.7V to 3.3V	5mA	J, N,	12-Bit ADC with Built-In Sample-and-Hold. Guaranteed Operation on a 2.7V Supply. Compatible with All Microprocessors' Serial Ports.

PART NUMBER	DESCRIPTION	RESOLUTION	TOTAL UNADJUSTED ERROR	SAMPLE RATE	VOLTAGE SUPPLY	MAXIMUM SUPPLY CURRENT	PKGS. AVAIL.	IMPORTANT FEATURES
LLTC1288C	12-Bit, 8-Pin, Serial I/O, 210µA (Typ) 3V Sampling A/D Converter with Automatic Power-Down, Differential Analog Input and 2-Channel Multiplexer.	12 Bits	±2LSB Linearity, ±0.75 Differential Nonlinearity, ±3LSB Offset, and ±8LSB Full-Scale Error Over Full Temperature Range.	6.6ksps	3V	390µA, 3µA During Shutdown	N, S	12-Bit ADC with Built-In Sample-and-Hold. Operates on 3V Supply Voltage. Compatible with All Microprocessors' Serial Ports. Automatic Power-Down. 2-Channel Multiplexer.
LTC1289C,I	12-Bit, 40µs, 3.3V or ±3.3V, Sampling A/D Converter with 8-Channel MUX and Serial Output. Input Range with Split ±3.3V Supply: $-3.3V \le V_{IN} \le 3.3V$; with 3.3V Supply: $0V \le V_{IN} \le 3.3V$.	12 Bits	±0.5LSB Linearity, ±1.5LSB Offset, and ±0.5LSB Full-Scale Error Over Full Temperature Range.	25ksps	2.7V to 3.3V or ±2.7V to ±3.3V	5mA, 10µA During Shutdown	J, N, S	12-Bit ADC with Built-In Sample-and-Hold and 8-Channel MUX. Guaranteed Operation on a 2.7V Supply. Compatible with All Microprocessors' Serial Ports. Automatic Power-Down.
LTC1290C,I,M	12-Bit, 8-Pin Serial I/O, A/D Converter with 8-Channel Multiplexer. Full Duplex Serial Interface.	12 Bits	±0.5LSB Linearity, ±1.5LSB Offset, and ±0.5LSB Full-Scale Error Over Full Temperature Range.	50ksps	5V or ±5V	12mA	J, N, S	12-Bit ADC with Built-In 8-Channel Analog MUX and Sample-and-Hold. Compatible with All Microprocessors' Serial Ports. Software Configurable Bipolar or Unipolar Operation. Full Duplex Serial I/O.
LTC1291C,I,M	12-Bit, 12µs, 5V, Sampling A/D Converter with Serial Output. Input Range: $0V \le V_{IN} \le 5V$.	12 Bits	±0.5LSB Linearity, ±3LSB Offset, and ±1LSB Full-Scale Error Over Full Temperature Range.	54ksps	2.7V to 3.3V or ±3.3V	12mA, 10µA During Shutdown	J, N	12-Bit ADC with Built-In Sample-and-Hold. Compatible with All Microprocessors' Serial Ports. Automatic Power-Down.
LTC1292C,I,M	12-Bit, 8-Pin A/D Converter Serial Output.	12 Bits	±0.5LSB Linearity, ±3LSB Offset, and ±0.5LSB Full-Scale Error Over Full Temperature Range.	60ksps	5V	12mA	J, N	12-Bit ADC, Unipolar Conversion of Single Differential Input. Separate Reference Pin Allows Reduced Span. Compatible with All Microprocessors' Serial Ports.
LTC1293C,I,M	12-Bit, Serial I/O, A/D Converter System with 6-Channel Multiplexer.	12 Bits	±0.5LSB Linearity, ±3LSB Offset, and ±0.5LSB Full-Scale Error Over Full Temperature Range.	46ksps	5V or ±5V	12mA	J, N	12-Bit ADC with Built-In 6-Channel MUX and Sample-and-Hold. Compatible with All Microprocessors' Serial Ports. Software Configurable Bipolar or Unipolar Operation. Full Duplex Serial I/O.
LTC1294C,I,M	12-Bit, Serial I/O, A/D Converter System with 8-Channel Multiplexer.	12 Bits	±0.5LSB Linearity, ±3LSB Offset, and ±0.5LSB Full-Scale Error Over Full Temperature Range.	46ksps	5V or ±5V	12mA	J, N	12-Bit ADC with Built-In 8-Channel MUX and Sample-and-Hold. Compatible with All Microprocessors' Serial Ports. Software Configurable Bipolar or Unipolar Operation. Half Duplex Serial I/O.
LTC1296C,I,M	12-Bit, Serial I/O, A/D Converter System with 8-Channel Multiplexer.	12 Bits	±0.5LSB Linearity, ±3LSB Offset, and ±0.5LSB Full-Scale Error Over Full Temperature Range.	46ksps	5V or ±5V	12mA, 10µA During Shutdown	J, N	12-Bit ADC with Built-In 8-Channel MUX and Sample-and-Hold. Compatible with All Microprocessors' Serial Ports. Software Configurable Bipolar or Unipolar Operation. Programmable Power-Down Includes a System Shutdown Output.
LTC1297C,I,M	12-Bit, 20µs, 5V, Sampling A/D Converter with Differential Input and Serial Output. Input Range with 5V Supply: $0V \le V_{IN} \le 5V$.	12 Bits	±0.5LSB Linearity, ±3LSB Offset, and ±1LSB Full-Scale Error Over Full Temperature Range.	20ksps	5V	12mA, 10µA During Shutdown	J, N	12-Bit ADC with Built-In Sample-and-Hold. Compatible with All Microprocessors Serial Ports. Automatic Power-Down.
LTC1298C,I	12-Bit, 8-Pin, Serial I/O, 340µA (Typ) Sampling A/D Converter with Automatic Power-Down.	12 Bits	±2LSB Linearity, ±0.75LSB Differential Nonlinearity, ±3LSB Offset, and ±8LSB Full-Scale Error Over Full Temperature Range.	11.1ksps	5V to 9V	640µA, 3µA During Shutdown	N, S	12-Bit ADC with Built-In Sample-and-Hold and 2-Channel MUX. Compatible with All Microprocessors Serial Ports. Automatic Power-Down.

Digital-to-Analog Converter Selection Guide

PART NUMBER	DESCRIPTION	RESOLUTION	TOTAL UNADJUSTED ERROR	SETTLING TIME	VOLTAGE SUPPLY	MAXIMUM SUPPLY CURRENT	PKGS. AVAIL.	IMPORTANT FEATURES
LTC1257C,I	12-Bit, Serial I/O, 8-Pin D/A Converter. Cascadable Serial I/O. Internal 2.048V Reference. Voltage Output.	12 Bits	±0.5LSB DNL, ±3.5LSB INL	6µs (±1/2LSB)	5V to 15.5V	600µA at V_{CC} = 5V	N, S	12-Bit DAC with Cascadable Serial I/O, Built-In Reference, and Voltage Output. Wide Supply Range of 5V to 15.5V. Space Saving SO-8 Package.

APPENDIX B



Power for Pentium® Processors; Meeting VRE Requirements

Craig Varga

Introduction

Providing power for the Pentium® microprocessor family is not a trivial task by any means. In an effort to simplify this task we have developed a new switching regulator control circuit and a new linear regulator to address the needs of these processors. Considerable time has been spent developing an optimized decoupling network. Here are several circuits using the new LTC®1266 synchronous buck regulator control chip and the LT®1584 linear regulator to provide power for Pentium processors and Pentium VRE processors. The Pentium processor has a supply requirement of 3.3V ±5%. The Pentium VRE processor requires 3.500V ±100mV.

The circuits shown here are designed to supply worst-case specification voltages to the Pentium VRE processor over line, load, transient and temperature. At first glance it may seem that simpler circuits, such as 3-terminal regulators, can provide this function. Worst-case analysis shows the margin to be too small (or negative) to ensure adequate operation over a wide production range. The combination of tight tolerance, tight transient response and large production volumes requires designs with adequate margin to ensure proper operation over the product's life. Failure of this circuit to provide proper power supply voltages can result in intermittent machine lock-up, freezes or erratic operation. There are no self-test software routines which can exercise the power supply over the entire expected combination of load, line and temperature conditions.

LTC1266 Drives N-Channel MOSFETs

The LTC1266 controller offers several advantages over its predecessors. It will drive all N-channel MOSFETs instead of requiring P-FETs for the high side switches. This lowers cost and improves efficiency. It also has a higher gain error amplifier which results in improved load regulation when compared to the LTC1148 family. There is also an undedicated comparator which may be used for a power good monitor, an overvoltage detector or an undervoltage lockout in these applications. There is a shutdown pin and a new burst inhibit function. Burst Mode™ operation is inhibited on all the designs shown here, however for the Pentium processor supplies (non VRE parts) Burst Mode operation may be enabled if desired. This is done by tying Pin 4 low. The reference tolerance available on the LTC1266 (or any other PWM controller for that matter) is not accurate enough to meet the Pentium VRE processor specification. The LT1431 however, does have a sufficiently accurate reference for these applications and permits very effective remote sensing capability (see Figure 2). Do not enable Burst Mode operation on Pentium VRE processor supplies as the circuits shown will not operate correctly at no load.

Handling the Load Transients

The Pentium processor has several habits which require careful attention if the circuit is to be reliable. The main problem is the load transients which the processor generates. The load can go from a low power (200mA) state to nearly 4A in two clock cycles or 20ns. While this is going on, the supply voltage must be held within the specification limits. The Pentium VRE processor specification is ±2.9% tolerance. This specification includes line, load, temperature regulation and initial set point tolerances as well as transient response. As may be imagined, meeting these requirements is not easy. With only 2.9% total deviation from the ideal voltage allowed, the static specifications (line, load, temperature and initial set point) must be held to approximately ±1% if any amount of transient response is to be permitted at all. Realistically, approximately 60mV peak transient response is obtainable. To achieve this, a large amount of low ESR tantalum capacitor must be installed as close to the processor as possible. The microprocessor socket cavity is the best place. As an absolute

minimum, use four pieces of a 100µF, 10V AVX type TPS tantalum. If more height is available, such as with a ZIF socket, it is preferred to use four each, 220µF, 10V parts instead. With the 100µF parts there is very little margin in the design. Also, do not reduce the quantity of the capacitors if going to a larger value. The ESR specifications are the same for the 100µF, 220µF and 330µF capacitors. The reason for paralleling four capacitors is to reduce the ESR as well as providing bulk capacitance. In the case of standard Pentium processor (non VRE) applications, if the above capacitor recommendations are followed, the circuits without the LT1431 (Figures 1 and 3) may be used successfully. In all cases there should be a minimum of 24 pieces of a 1µF ceramic capacitor to decouple the high frequency components of the transient. (Intel recommends 24 each, 1µF X7R ceramic capacitors for high frequency bypass.)

Circuit Board Layout Considerations

All the capacitors in the decoupling network should be installed on power and ground plane areas on the topside of the board. An absolute minimum of one feedthrough per end for each capacitor into the internal power and ground plane should be used. It is preferred to use two feedthroughs per capacitor end (112 total). Any more than 64 proves to be of no benefit for transient improvement, but will still help attenuate very high frequency noise. At 30 feedthroughs total, expect about a 2mV increase in transient droop. This is about a 5% degradation in performance. Decoupling capacitors should be connected with planes rather than traces. The traces will be far too inductive. The total network ESR must be less than 0.0065Ω and ESL less than 0.07nH for the Pentium VRE processor.

Input Capacitance

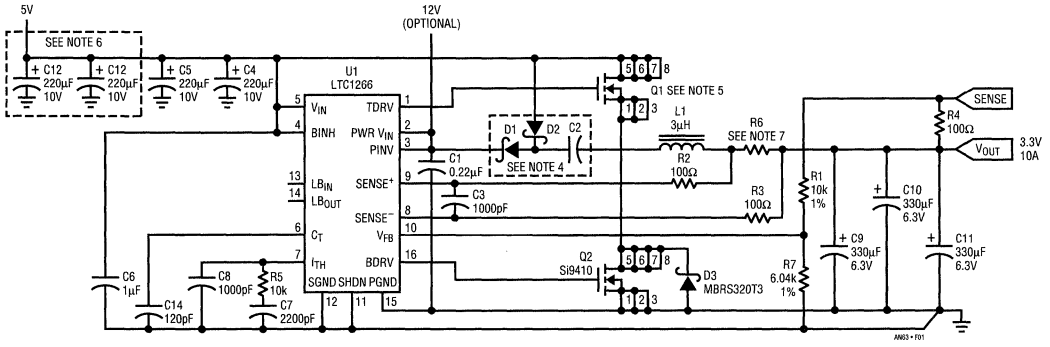
Another important consideration is the amount of capacitance on the power supply input. For switchers, the ripple current rating must be high enough to handle the regulator input ripple. In addition, this capacitance will decouple the load transients from the 5V supply. If insufficient capacitance is used, the disturbance on the 5V supply will exceed the ±5% specification for the TTL logic powered by this voltage. Since the magnitude of this disturbance is quite dependent upon the nature of the 5V power supply, and the performance of these supplies varies widely, it is difficult to say just how much capacitance is needed. In general however, if enough capacitance is present to handle the ripple current, the disturbance on the 5V supply will be acceptable. Good transient response on the 5V supply translates to a need for less input capacitance. If sufficient bulk capacitance is present on the motherboard for the 5V supply, less additional capacitance will be required on the processor supply input. As a minimum there should be at least one low ESR capacitor within an inch of the regulator. Be careful to look at the level of disturbance on the 5V supply to make sure the 5V remains within specifications.

Powering the Pentium Processor

The same basic circuit is used for both the 5A and 10A switcher designs. The necessary substitutions are shown on the schematic, Figure 1. If 12V is available to power the LTC1266, the bootstrap capacitor and diodes may be eliminated. The 12V solution is preferred as it is simpler and somewhat more efficient. If no 12V is available, use the bootstrap circuit. Note also that different MOSFETs are specified for the 5A and 10A circuits. The Si4410 offers less than 1/2 the ON resistance of the Si9410 shown for the 5A circuit.

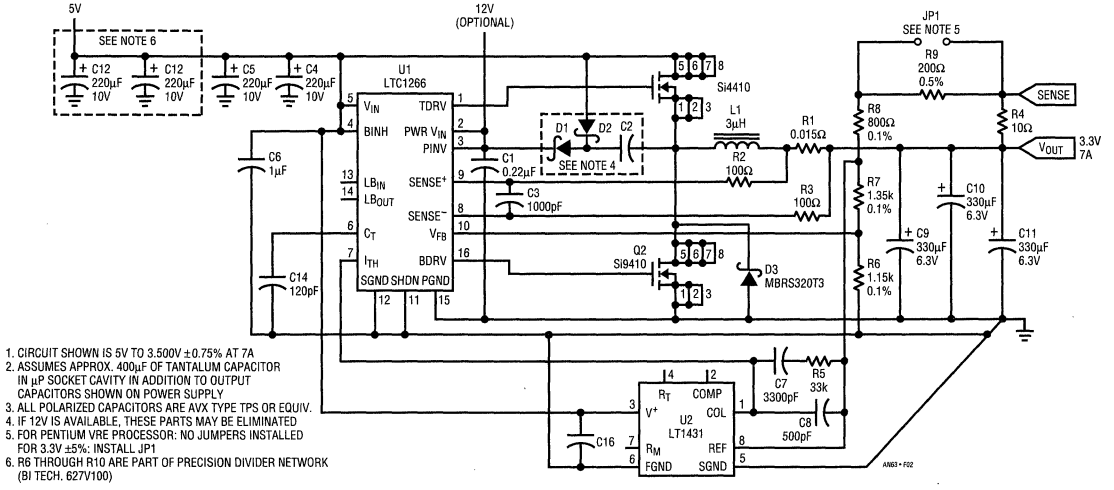
High Accuracy Switcher Solution—Basics of Operation

The solution for the Pentium VRE processor relies on the accuracy of the LT1431 (see Figure 2). The internal reference is specified at 2.5V ±0.4% worst-case at 25°C. The bulk of the parts produced is closer to ±0.2%. This device consists of a precision reference and a wide bandwidth amplifier with an open-collector output. The feedback divider is set to place the Reference Input pin at 2.5V with the desired output present. The 2.5V is further divided to 1.15V to drive the LTC1266 V_{FB} pin. This pin will normally want to sit at 1.25V. As such, the LTC1266 sees the output as being too low and tries to force its internal error amplifier to the positive rail, which is 2.0V. This output shows up as a current out of the I_{TH} pin. The open-collector of the LT1431 pulls enough current from this pin to set the output of the supply at the desired voltage. Since this constitutes a high gain servo loop, the output is regulated very accurately. Loop compensation is accomplished by R5, C7 and C8. The internal error amplifier of the LTC1266 will function as an overvoltage protection loop should the LT1431 ever fail.



1. CIRCUIT SHOWN IS 5V TO 3.3V ±5% AT 5A TO 10A
2. ASSUMES APPROX. 400µF OF TANTALUM CAPACITOR IN µP SOCKET CAVITY IN ADDITION TO OUTPUT CAPACITORS SHOWN ON POWER SUPPLY
3. ALL POLARIZED CAPACITORS ARE AVX TYPE TPS OR EQUIVALENT
4. IF 12V IS AVAILABLE, THESE PARTS MAY BE ELIMINATED D1, D2: MBR120T3 C2: 1µF
5. FOR 5A OUTPUT USE Si9410, FOR 10A USE Si4410
6. PARTS MAY BE ELIMINATED IN 5A DESIGN
7. VALUE FOR 5A IS 0.02Ω, FOR 10A USE 0.01Ω

Figure 1. High Current Supply for Standard 3.3V CPUs



1. CIRCUIT SHOWN IS 5V TO 3.500V ±0.75% AT 7A
2. ASSUMES APPROX. 400µF OF TANTALUM CAPACITOR IN µP SOCKET CAVITY IN ADDITION TO OUTPUT CAPACITORS SHOWN ON POWER SUPPLY
3. ALL POLARIZED CAPACITORS ARE AVX TYPE TPS OR EQUIV.
4. IF 12V IS AVAILABLE, THESE PARTS MAY BE ELIMINATED
5. FOR PENTIUM VRE PROCESSOR: NO JUMPERS INSTALLED FOR 3.3V ±5%: INSTALL JP1
6. R6 THROUGH R10 ARE PART OF PRECISION DIVIDER NETWORK (BI TECH. 627V100)

Figure 2. High Precision Microprocessor Supply

Linear Regulators Provide Simple, Low Cost Solution

For the standard Pentium processor, the LT1584 linear regulator will provide very good performance for 5V to 3.3V regulation. The transient response of this regulator is extremely fast as compared to previous 3-terminal regulators and allows the bulk decoupling capacitance for the processor to be minimized.

The circuit in Figure 3 will provide up to 7A at 3.3V. For 5% tolerance systems, use standard 1% resistors for the feedback divider. If however the application is for a Pentium VRE processor-based system, the DC accuracy of the regulator is not guaranteed to meet the specification requirements under all combinations of line, load and temperature. If typical specifications are used, the regulator will meet requirements, but worst-case calculations reveal larger tolerances than needed to ensure 100% specification compliance. To address this issue, the circuit shown in Figure 4 can be used. With the addition of the LT1431, the reference tolerance is less than half that specified for the LT1584. Temperature effects are nearly eliminated since the LT1431 stays at box ambient rather than the elevated

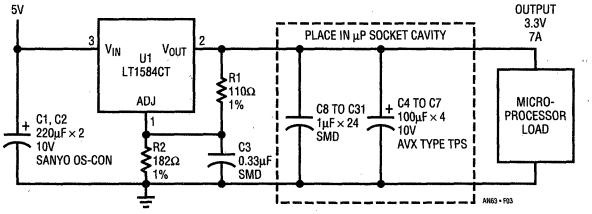


Figure 3. Low Parts Count Linear Supply

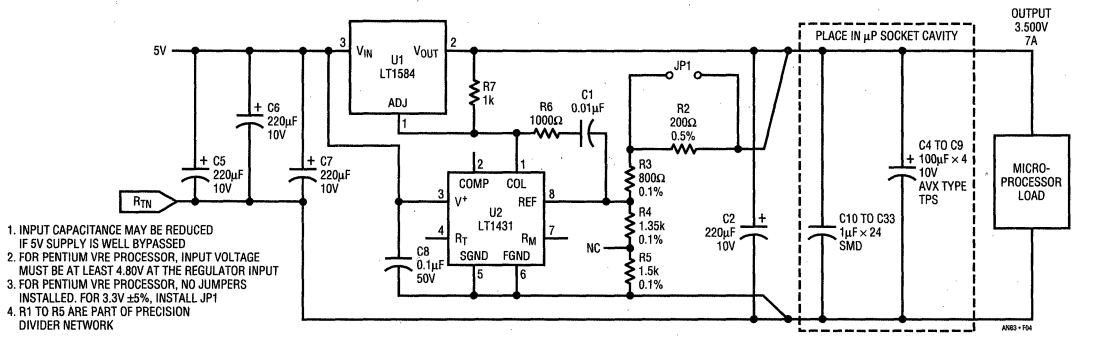


Figure 4. High Precision Linear Regulator

temperature experienced by the internal reference of the LT1584. Also, remote sense is now possible, so any static distribution losses are corrected. This also eliminates problems which may be caused by connector pin contact resistance increasing with time. This circuit also exhibits improved transient response compared to the LT1584 by itself. As a caveat, the minimum input voltage required to meet the Pentium VRE processor output specifications from 25°C and up is 4.80V measured at the regulator input.

The circuit operates by forcing the LT1584 ADJ pin voltage to whatever voltage is required to obtain the desired output voltage. Since R7 is across the 1.25V ADJ to V_{OUT} reference of the LT1584, it acts like a current source. Pin 1 of the LT1431 has an open-collector output which can sink this current to ground and therefore control the ADJ pin to ground voltage. A feedback divider from output to the LT1431 REF pin sets this pin at 2.500V. The internal amplifier in the LT1431 has a very high gain in this configuration, hence static errors are nearly nonexistent. Moreover, since this amplifier is also quite fast, the ADJ pin can be moved further than the actual disturbance caused by a load transient. Thus, a significant response time improvement may be realized with this scheme over an LT1584 by itself.

Conclusion

The Pentium microprocessor offers some interesting challenges to the power system designer. In an attempt to run at higher clock speeds the power supply voltage specifications have gotten tighter and stop clock power saving modes have introduced severe load transients not present in previous generations of processors. However, with careful attention to detail, both in component selection and mechanical layout, the performance required may be obtained. Also, with properly designed switchers, the need for high efficiency can be met while providing the required dynamic performance.

Using the LTC1325 Battery Management IC

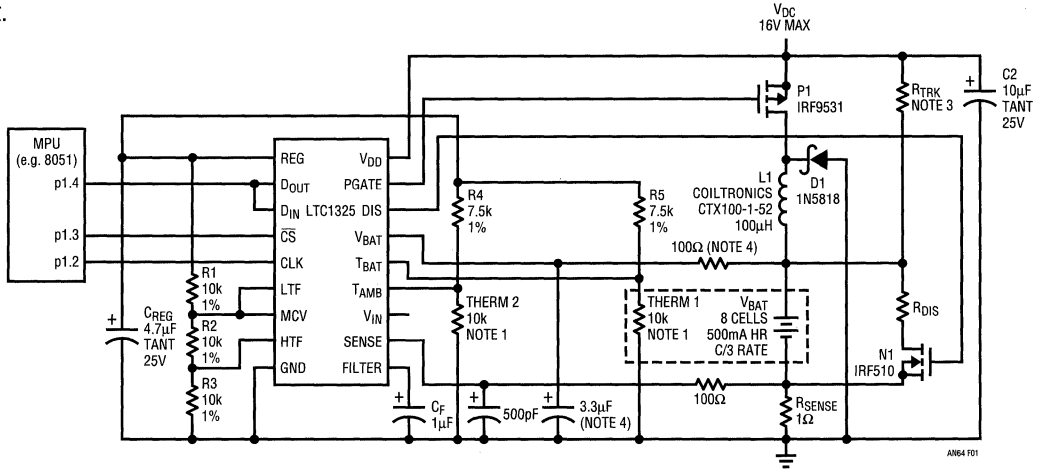
Anthony Ng, Peter Schwartz, Robert Reay,
Richard Markell

INTRODUCTION

For a variety of reasons, it is desirable to charge batteries as rapidly as possible. At the same time, overcharging must be limited to prolong battery life. Such limitation of overcharging depends on factors such as the choice of charge termination technique and the use of multi-rate/ multi-stage charging schemes. The majority of battery charger ICs available today lock the user into one fixed charging regimen, with at best a limited number of customization options to suit a variety of application needs or battery types. The LTC®1325 addresses these shortcomings by providing the user with all the functional blocks needed to implement a simple but highly flexible battery charger (see Figure 1) which not only addresses the issue of charging batteries but also those of battery conditioning and capacity monitoring. A microprocessor interacts with the LTC1325 through a serial interface to control the operation of its functional blocks, allowing software to expand the scope and flexibility of the charger circuit.

This Application Note was written with the following objectives in mind :

- Provide users with an insight into the architecture and operation of the LTC1325.
- Outline basic techniques for charging various battery types.
- Present a variety of useful, tried and tested charging circuits.
- Give an overview of the most common battery types and their characteristics.
- Clarify specialized and application-specific terminology. Definitions are provided in the text, as well as in Appendix C.



NOTE 1: THERMISTORS 1 AND 2 ARE PANASONIC ERT-D2FHL103S NTC THERMISTORS OR EQUIVALENT.
NOTE 2: V_{REF} = 160mV, R_{SENSE} = 1 FOR C/3 CHARGE RATE (160mA).
NOTE 3: CHOOSE FOR C/20 TRICKLE CHARGE RATE.
NOTE 4: 2.0k AND 47µF FOR COMPATIBILITY WITH LITHIUM-ION AND LEAD-ACID

Figure 1. Complete LTC1325 Battery Management System

LTC1325 PRIMER

The main features of the LTC1325 may be summarized as follows:

- It has all the functional blocks needed to build a charger: a 10-bit Analog-to-Digital Converter (ADC), fault detection circuitry, a switching regulator controller with a MOSFET driver, a programmable timer, a precision 3.072V regulator for powering external temperature sensors, and a programmable battery voltage divider.
- The functional blocks are placed under the control of an external microprocessor for ready adaptability to different charging algorithms, battery chemistries, or charge rates.
- Communication with the microprocessor is via a simple serial interface, configurable for 3-wire or 4-wire operation.
- It has autonomous fault detection circuitry to protect the battery against temperature or voltage extremes.
- In addition to charging, the part can discharge batteries for battery conditioning purposes.
- It includes on-chip circuitry for an accurate battery capacity monitor (Gas Gauge).
- It charges batteries using a switching buck regulator for highest efficiency and lowest power dissipation.
- The wide supply voltage range (V_{DD}) of 4.5V to 16V allows the battery charger to be powered from the charging supply while charging batteries of up to 8 cells in series.
- It can charge batteries which require charging voltages greater than V_{DD}.
- It can charge batteries from charging supplies greater than V_{DD}.
- A shutdown mode drops the supply current to 30µA.

Charging Circuit

Unlike most other charger ICs which employ a linear regulator, the LTC1325 charges batteries using a switching buck regulator. This approach simultaneously maximizes efficiency and minimizes power dissipation. The only external power components needed are an inductor, a P-channel MOSFET switch, a sense resistor and a catch diode (see Figure 1). An internal, programmable battery voltage divider which accommodates 1 to 16 cells removes the need for an external resistive divider (for batteries with voltages below the maximum V_{DD} of 16V). All the circuits needed for controlling the loop are integrated on-chip and no external ICs are required. The LTC1325 operates from 4.5V to 16V so that it can be powered directly from the charging supply. The wide supply range makes it possible to charge up to 8 cells without the need for an external regulator to drop the charging supply down to the supply range of the LTC1325. These features make the LTC1325 easy to use. When charging is completed and the charging supply is removed, the chip does not load down other system supplies. If the LTC1325 is powered from a system supply, the microprocessor can program it into shutdown mode in which the quiescent current drops to 30µA. In shutdown mode the digital inputs stay alive to await the wake-up signal from the microprocessor.

The buck regulator control circuit maintains the average voltage across the sense resistor (R_{SENSE}) at V_{DAC} (see Figure 2). In addition, a programmable duty cycle can modulate the P-channel MOSFET driver output (PGATE) to reduce average charging current. The average charging current is given by:

$$I_{CHRG} = V_{DAC}(\text{duty cycle})/Rsense$$

The microprocessor can set V_{DAC} to one of four values, and the duty cycle to one of five values, giving 20 possible I_{CHRG} values with a single R_{SENSE} resistor.

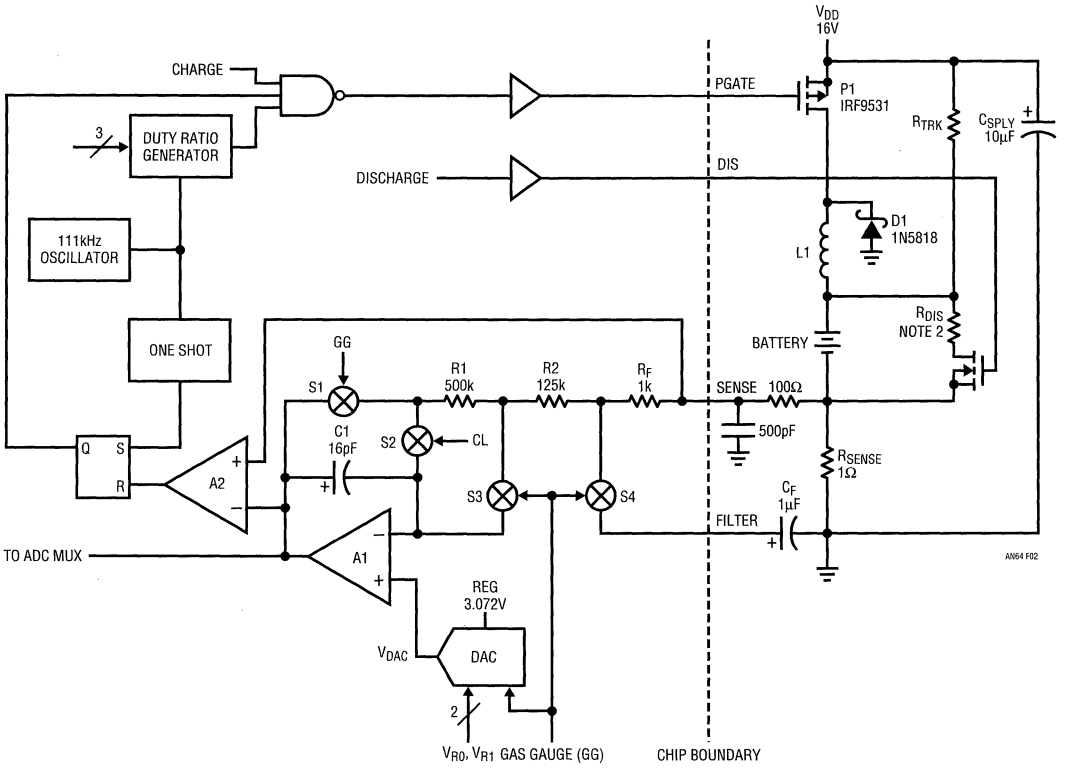


Figure 2. LTC1325 Charge, Discharge and Gas Gauge Circuit

Charge Termination

Virtually any known charge termination technique can be implemented with the LTC1325. The most common of these are based on battery temperature (T_{BAT}), cell voltage (V_{CELL}), time (t), ambient temperature (T_{AMB}), or a combination of these parameters. Unlike other fast charging ICs, the LTC1325 does not lock the user into a particular termination technique and any shortcomings of that technique. Instead, it provides the microprocessor a means to measure T_{BAT}, T_{AMB} and V_{CELL}. By keeping track of elapsed time, the microprocessor has the means to calculate all existing termination techniques (including dT_{BAT}/dt and d^2V_{BAT}/dt^2), and perform averaging to reduce the probability of false termination. This flexibility also means that a single circuit can charge Nickel-Cadmium, Nickel-Metal Hydride, Sealed Lead-Acid, and Lithium-Ion batteries. The LTC1325 has an on-chip 10-bit successive approximation ADC with a 5-channel input multiplexer. Three channels are dedicated to T_{BAT}, V_{CELL} and the Gas Gauge (see section on Capacity Monitoring); the other two channels can be used for other purposes such as sensing T_{AMB} or another external sensor. The LTC1325 can be programmed into Idle mode in which the charge loop is turned off. This permits measurements to be made without the switching noise that is present across the battery during charging.

Fault Protection

The LTC1325 monitors battery temperature, cell voltage and elapsed time for faults and prevents the initiation or the continuation of charging should a fault arise. The fault detection circuit (see Figure 3) consists of comparators which monitor T_{BAT} and V_{CELL} to detect low temperature faults (LTF), high temperature faults (HTF), low cell voltages (BATR, EDV) and high cell voltages (MCV). The LTF, HTF and MCV thresholds are set by an external resistor divider (R1 to R4) to maximize flexibility. The LTC1325 also includes a timer that permits the microprocessor to set charging time before a timer fault occurs to one of eight values: 5, 10, 20, 40, 80, 160, 320 minutes or no time-out. Selecting "no time-out" disables timer faults (the time-out period is in effect set to infinity).

Battery Conditioning

Under some operating or storage conditions, certain battery types (most notably NiCd) lose their full capacity. It is often necessary to subject such batteries to deep discharge and charge cycles to restore the lost capacity. The LTC1325 can be programmed into Discharge mode in which it automatically discharges each cell to 0.9V. This voltage is defined as the End-of-Discharge Voltage (EDV). Fault protection remains active in Discharge mode to protect the battery against temperature extremes (LTF, HTF) and to detect the EDV discharge termination point.

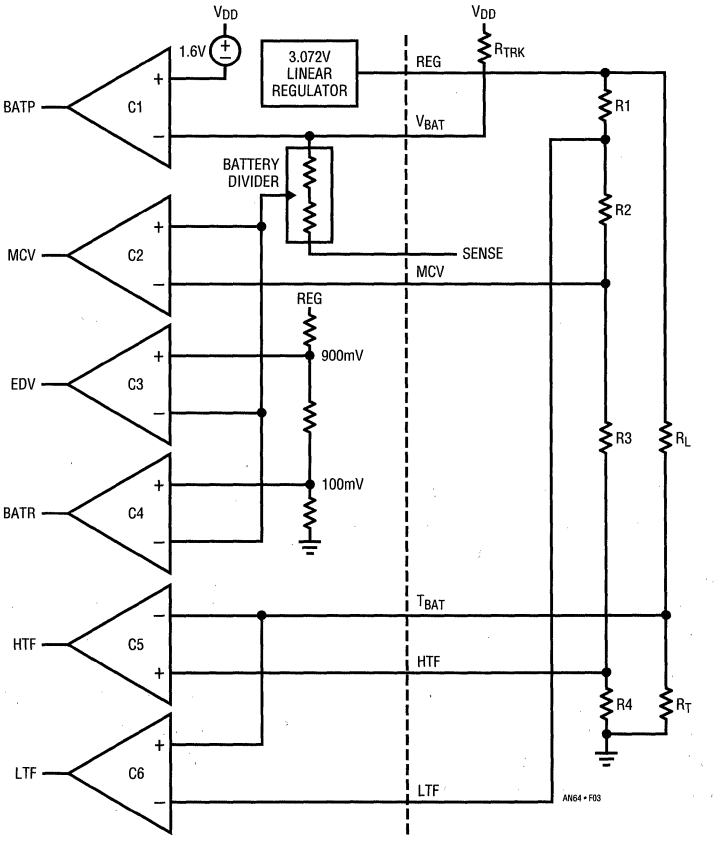


Figure 3. LTC1325 Fault Detection Circuitry

Capacity Monitoring

The LTC1325 may be programmed into Gas Gauge mode (GG = 1 in Figure 2). In this mode, the sense resistor is used to sense the battery load current. The battery load is connected between V_{BAT} and ground so that the load current passes through the sense resistor, producing a negative voltage at the Sense pin. The Sense pin voltage is filtered by a $1k\Omega \times C_F$ lowpass filter and multiplied by a gain of –4 via amplifier A1. The output of A1 is converted by the ADC whenever the gas gauge channel is selected by the microprocessor. By accumulating gas gauge measurements over time, the microprocessor can determine how much charge has left the battery and what capacity remains.

APPLICATIONS CIRCUITS

Charging Nickel Cadmium and Nickel Metal Hydride Batteries

It is desirable to charge batteries as fully and rapidly as possible. At the same time it is necessary to limit overcharging, which can adversely affect battery life. To meet these requirements, multi-stage charging algorithms are recommended for NiCd and NiMH batteries. Multi-stage charging algorithms consist of 2 or 3 stages:

2-Stage: Fast Charge
Trickle Charge

3-Stage: Fast Charge
Top-Off Charge
Trickle Charge

During Fast Charge, the battery is charged at the maximum permitted rate to near full capacity. In Top-Off the battery is charged at a lower rate to bring it to full capacity thus minimizing overcharge. Finally, during Trickle Charge, the battery is charged at a rate that just compensates for self-discharge to maintain it at full capacity. Recommendations of the battery manufacturer determine which algorithm to use. In general, the best way to limit overcharge is to use a primary charge termination technique and several secondary techniques for redundancy. Regardless of the algorithm, the basic circuit to charge up to 8 NiCd or NiMH cells is shown in Figure 1.

Examples of Charging Algorithms

2-Stage NiCd

Fast Charge	C/1 rate, –ΔV (15mV) primary termination Time-out secondary termination (80 minutes)
Trickle Charge	C/10 rate, no termination needed

2-Stage NiCd

Fast Charge	C/1 rate, TCO (45°C) primary termination Time-out secondary termination (80 minutes)
Trickle Charge	C/10 rate, no termination needed.

3-Stage NiMH

Fast Charge	C/1 rate, ΔTCO (10°C) primary termination
Top-Off Charge	C/10 until secondary termination at 180 minutes (160 min + 20 min)
Trickle Charge	C/40 rate, no termination

3-Stage NiMH

Quick Charge	C/3 rate, 120 minute (80 min + 40 min) to 160 minute time-out TCO (40°C) secondary termination
Top-Off Charge	C/10 rate until V_{CELL} = 1.5V
Trickle Charge	C/40 rate, no termination

All these algorithms may be realized with the circuit in Figure 1. Only the software and perhaps some component values change.

Conditioning Batteries

When overcharged for extended periods of time, some NiCd batteries exhibit what is commonly called the "memory effect," The voltage per cell drops 150mV which may lead the user to conclude that the battery is at the end of its discharge curve. This condition may be reversed by deeply discharging and recharging the battery. The LTC1325 can be programmed to discharge a battery until its per cell voltage falls below 0.9V (EDV). As shown in Figure 1, the external N-channel MOSFET N1 is turned on to discharge the battery. R_{DIS} is selected such that the discharge current, V_{BAT}/R_{DIS}, is within the allowable limits set by the battery manufacturer. Discharge currents can be large with high capacity batteries. The power rating of R_{DIS} should be greater than $I_{DIS}^2 \times R_{DIS}$. The source of N1 may be terminated to the top of R_{SENSE} (as in Figure 1) or to ground. The former is preferred since the V_{BAT} pin monitors the battery voltage for EDV and not the battery voltage plus the drop across R_{SENSE}. If desired it is possible to adjust the EDV voltage via the internal battery divider setting as outlined in the next section.

Using the End-of-Discharge Voltage Fail-Safe

The LTC1325, when commanded to do so, will discharge a battery until its cell voltage goes below 900mV nominal, at which point an EDV fail-safe occurs and the DIS pin is taken low to stop discharge. This function of the IC is most commonly used for the protection and conditioning of NiCd and NiMH batteries, but may also be used to condition a Lead-Acid battery or to reset the Gas Guage to a known point (remaining battery capacity equals zero) for any battery type. Immediately following discharge, the voltage per cell for NiCd and NiMH batteries will typically "rebound" by 100mV to 200mV. The controlling software will need to take this rebound into account to prevent a possible oscillation in which the ADC would be read, the EDV and fail-safe bits reset, and the battery discharged for a few more seconds before again indicating EDV and stopping the discharge.

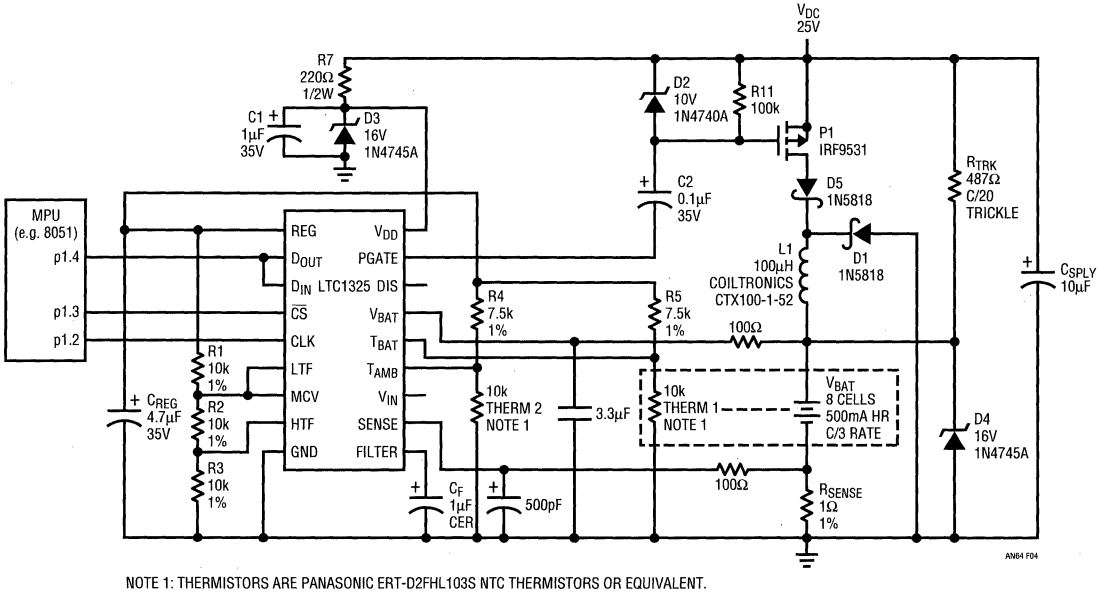
If desired, the battery divider can be programmed to divide by a factor that is less than the number of cells in the battery. For example, if the divider is programmed to divide-by-5 when the number of cells in the battery is six, the EDV fault occurs at $(5 \times 0.9)/6$ or 0.75V. Similarly, programming the divider to divide-by-6 with a three-cell Lead-Acid battery would give an EDV of $(6 \times 0.9)/3 = 1.8V$ per cell at termination of discharge.

Operating from Charging Power Supplies of Above 16V

The LTC1325 has a maximum V_{DD} range of 16V. To operate from a higher supply voltage, it is necessary to do two things: add a regulator to drop the higher supply (V_{DC}) down to the supply range of the LTC1325 and add a level shifter between the PGATE pin and the gate of the external P-channel MOSFET. The level shifter ensures that the P-channel MOSFET can be switched off completely. Figure 4 shows a low cost circuit that will charge up to 8 cells from a 25V supply at 160mA. For 2A charge current, L1 and R_{SENSE} should be changed to 15µH and 0.08Ω respectively. V_{DAC} is set to 160mV in both cases for best accuracy. The number of cells that can be charged is affected by any series resistance in the charge path. At high charging currents low resistance inter-cell connections such as solder tabs are recommended.

The zener diode D3 is used to drop the 25V V_{DC} down to 16V to serve as V_{DD} supply to the LTC1325. R7 should not be greater than 220Ω. Alternatively, a 3-terminal regulator (such as the LT®1086-12 or LT1085-12) may replace D3, C1 and R7. The regulator output voltage (V_{DD}) fixes the number of cells that can be charged with the circuit to about V_{DD}/V_{EC} where V_{EC} is the maximum cell voltage expected.

When the battery is removed, R_{TRK} pulls the V_{BAT} pin towards V_{DC}. D4 acts as a clamp to prevent V_{BAT} from rising above the V_{DD} supply voltage. D2, C2 and R11 form a simple level shifter. During charging, D2 clamps the voltage at the gate of P1 between $V_{DC} - V_Z$ and $V_{DC} + 0.7V$, where V_Z is the reverse breakdown voltage of D2. V_Z is selected to limit the V_{GS} of P1 to within its maximum rating. For logic-level P-channel MOSFETs with a maximum V_{GS} of ±8V, D2 may be a 3.9V zener such as the 1N4730A. For standard MOSFETs (±20V V_{GS} rating), a 1N4740A 10V zener may be used. When power (V_{DC}) is first applied, V_{DD} takes a finite time to charge up to 16V so that the voltage on the PGATE pin is initially 0 and P1 is turned on. D2 breaks down, charging C2 quickly to one zener drop below V_{DC}. Then as PGATE rises, D2 forward



NOTE 1: THERMISTORS ARE PANASONIC ERT-D2FHL103S NTC THERMISTORS OR EQUIVALENT.

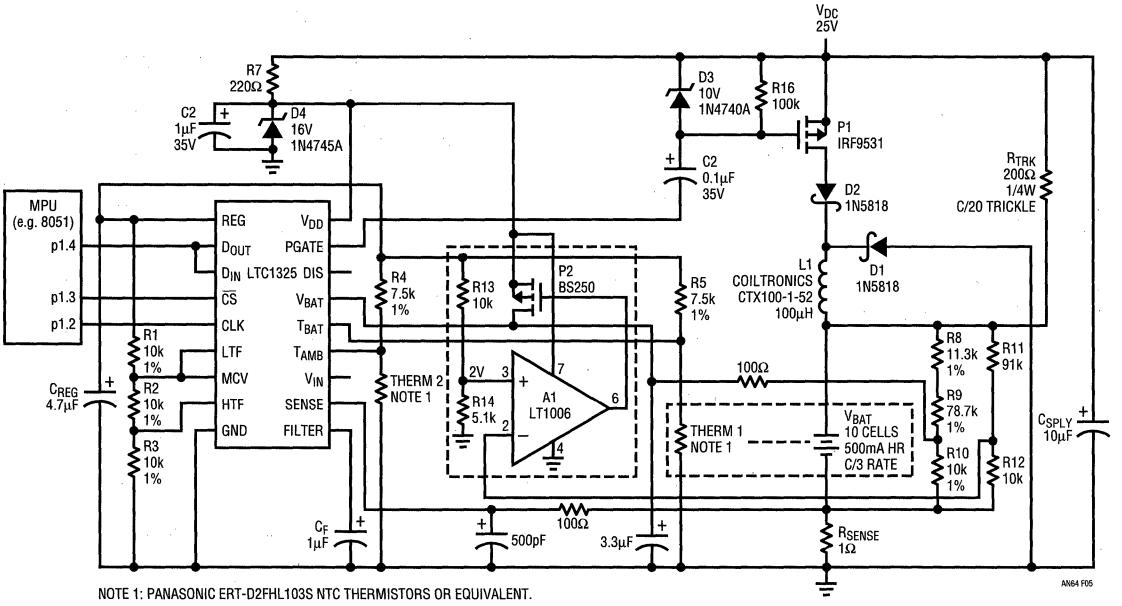
Figure 4. Charging from a 25V Supply

biases and the gate of P1 rises to one diode drop above V_{DC} and P1 shuts off. R11 serves to hold P1 off if the V_{DD} supply should go away for some reason. In this situation, it takes several milliseconds for R11 to shut P1 off completely which means that P1, L1 and R_{SENSE} must be able to withstand a brief current pulse of $(V_{DC}-V_{BAT})/R$, where R is the total of the $R_{DS(ON)}$ of P1, R_{SENSE} and inductor winding resistance. Diode D5 prevents battery discharge if the V_{DC} supply is removed.

Charging "Tall" Batteries (> 8 cells)

To charge more than 8 cells, the charging supply (V_{DC}) must be greater than 16V (assuming 2V per cell at the end of charge). Since V_{DC} is above 16V, a regulator and level shifter are required, as explained in the previous application. Figure 5 shows a circuit that will charge batteries with more than 8 cells in series. In addition, an external battery divider is added to limit the voltage seen at the V_{BAT} pin to below V_{DD}. The values of R8, R9 and R10 are selected such that R10/(R8 + R9 + R10) is the number of cells in the battery. The battery divider in the LTC1325 is programmed to divide by one. V_{DAC} is programmed for 160mV so that the charging current is 160mV/R_{SENSE} or 160mA. This charges the 10 cell 500mA Hr stack at a C/3 rate. R_{TRK} is selected to trickle charge the battery at C/20. The same circuit will charge batteries at 2A if L1 and R_{SENSE} are changed to 15µH and 0.08Ω respectively.

Without R11 to R14, P2 and A1 in Figure 5, the BATP status flag will always be high regardless of whether the battery is present or not. It is therefore possible to start the charge loop when the battery is not present. The current through the charge loop will be low (typically in the milliampere range). If this is undesirable, R11 to R14, P2 and A1 may be added to ensure proper operation of the BATP flag. R11 and R12 are selected such that R12/(R11+R12) is the number of cells in the battery. Op amp A1 compares the cell voltage against a threshold set by R13 and R14. When the battery is absent, A1 trips to turn on P2 which then pulls V_{BAT} up to V_{DD}. This causes the BATP flag to go low to indicate the absence of the battery.



NOTE 1: PANASONIC ERT-D2FHL103S NTC THERMISTORS OR EQUIVALENT.

Figure 5. Charging More Than 8 Cells

Hardwired Charge Termination Using Thermistors

Termination Using Positive Temperature Coefficient (PTC) Thermistors: The resistance of a PTC thermistor increases sharply when its temperature rises above a specified setpoint (T_S). This rapid change may be exploited to implement hardwired TCO charge termination. In Figure 6, fixed resistor R4 is connected from REG to the T_{BAT} input, and the PTC thermistor R5 is connected between the T_{BAT} input and Sense. Hence R5 is the controlling element of a temperature-dependent voltage divider. The PTC is mounted on the battery to sense its temperature. R4 is selected such that when the battery temperature is below T_S, the divider output voltage is between the voltages at the LTF and HTF pins. When the battery temperature rises above T_S, the rapid increase in the resistance of the PTC device causes the divider output (i.e. the voltage at the T_{BAT} pin) to rise above the voltage set by R1, R2 and R3 at the LTF pin. The LTC1325 detects a temperature fail-safe (LTF = 1, FS = 1) and stops charging by taking the PGATE pin to V_{DD}. A typical value for TCO is 45°C. T_S and R_{THERM1} have typical tolerances of ±5°C and ±40% respectively. The PTC shown in Figure 6 has a T_S of 50°C ±5°C, so charging will terminate when the battery temperature reaches a value between 45°C and 55°C. The series resistance of PTC thermistor and R4 should be in the kΩ range to minimize loading on the REG pin of the LTC1325.

In principle, it is possible to implement hardwired ΔTCO termination by replacing R4 with another PTC with a resistance vs temperature characteristic that matches that of R5 as shown in Figure 7. If both PTCs match closely, the divider output will now respond to the difference between

battery and ambient temperature. In practice, matched PTCs are not generally available as standard items from thermistor manufacturers and are therefore not recommended for such use. If hardware ΔTCO termination is desired, standard NTCs such as those matched over a specified temperature range may be used. With NTCs, the divider output will drop as the battery heats up and when the voltage drops below the voltage at the HTF pin, the LTC1325 will detect a temperature fail-safe (HTF = 1, FS = 1) and terminate charging.

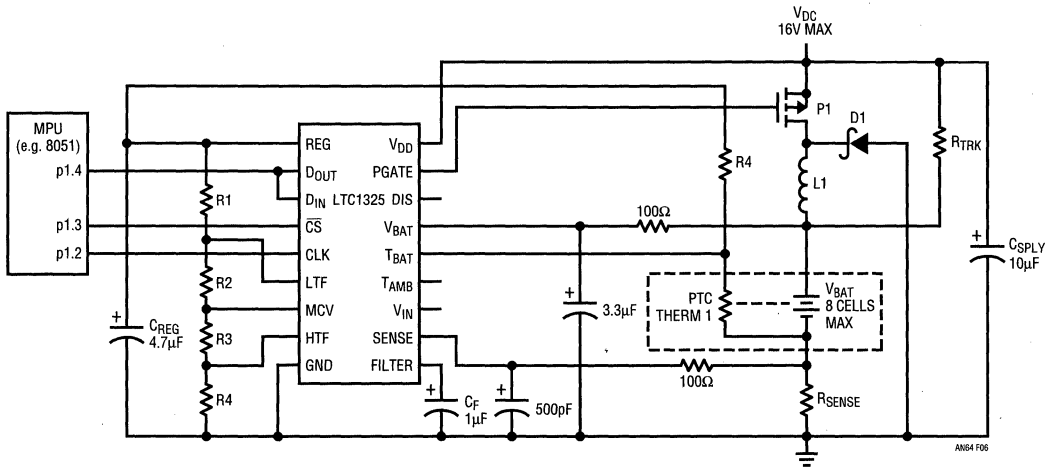


Figure 6. Hardwired TCO Termination

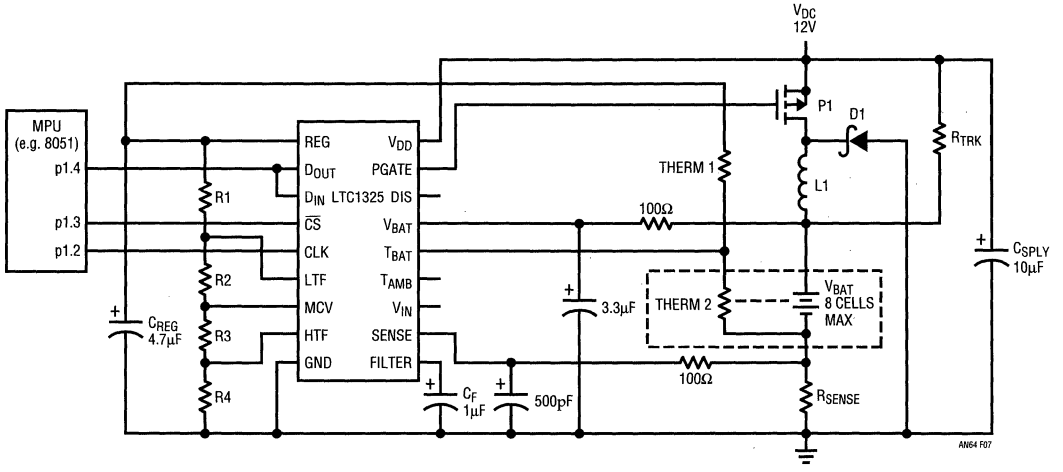


Figure 7. Hardwired ΔTCO Termination

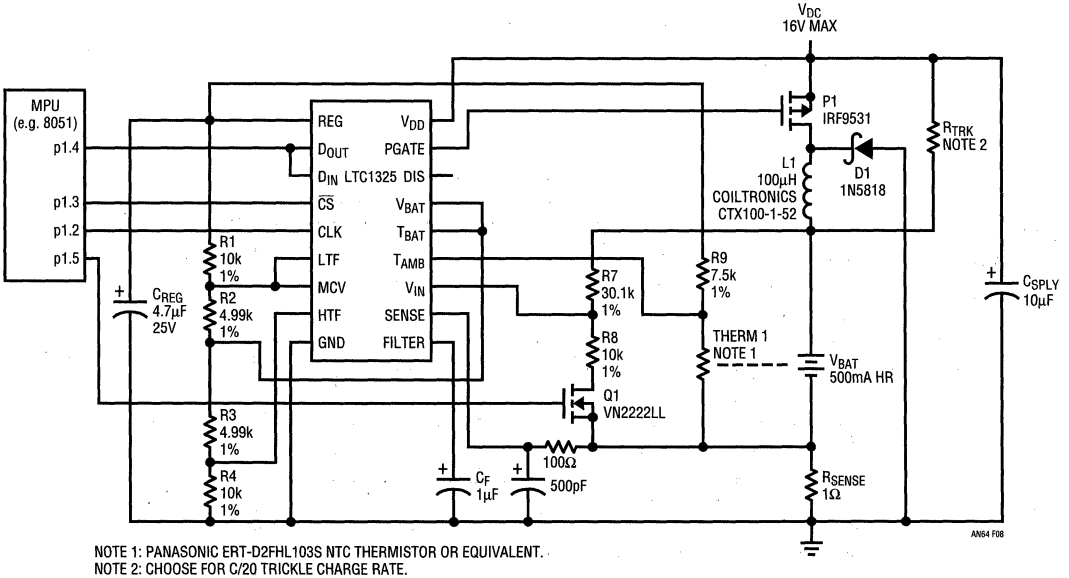
Termination Using Negative Temperature Coefficient (NTC) Thermistor: It is common for the thermistor in the battery pack to be terminated at the negative terminal of the battery. During charging, the Sense pin will exhibit a switching waveform with peaks of 200mV to 300mV when V_{DAC} is programmed for 160mV. This waveform appears on the T_{BAT} pin when the thermistor is terminated at the negative terminal of the battery. The thermistor slope is typically –30mV/°C, so the switching noise can cause premature fail-safes when the battery temperature is within 10°C of the LTF or HTF trip points. An RC filter (with time constant much greater than the clock period of 10µs) can be inserted between the T_{BAT} pin and the output of the battery thermistor circuit to prevent false fail-safes.

Disabling Fail-Safes

The LTC1325's built-in battery voltage and temperature fail-safes can be easily disabled as shown in Figure 8. To disable temperature fail-safes, the T_{BAT} pin is tied to the top of resistor R3. The LTC1325 is made to think that the battery temperature is constant and within the limits set by the LTF and HTF pins. Similarly, V_{BAT} may be tied to the same point to disable all the battery voltage fail-safes (MCV, EDV, BATR). The LTC1325 battery divider is programmed to divide-by-1. Battery temperature and cell voltage can still be measured using the T_{AMB} and V_{IN} channels of the ADC. An external divider (R7, R8) replaces the internal divider connected to the V_{BAT} channel.

Gated P-Channel MOSFET Controller

When an external current-limited voltage source is available, and charging currents are low enough that efficiency and heat dissipation are not major concerns, the LTC1325 can be used to turn on a P-channel MOSFET to gate the current into the battery. This circuit makes an inexpensive and effective combination. The battery's current limit during charging is set by the current limit of the charging power supply V_{DC}. The maximum available current should therefore not exceed the permissible charge rate of the battery. With the LTC1325 V_{DAC} programmed to the 160mV setting, and the voltage at the Sense pin below this value, the LTC1325 will hold MOSFET P1 on until charge



NOTE 1: PANASONIC ERT-D2FHL103S NTC THERMISTOR OR EQUIVALENT.
NOTE 2: CHOOSE FOR C/20 TRICKLE CHARGE RATE.

Figure 8. Charger with T_{BAT} and V_{BAT} Fail-Safes Disabled

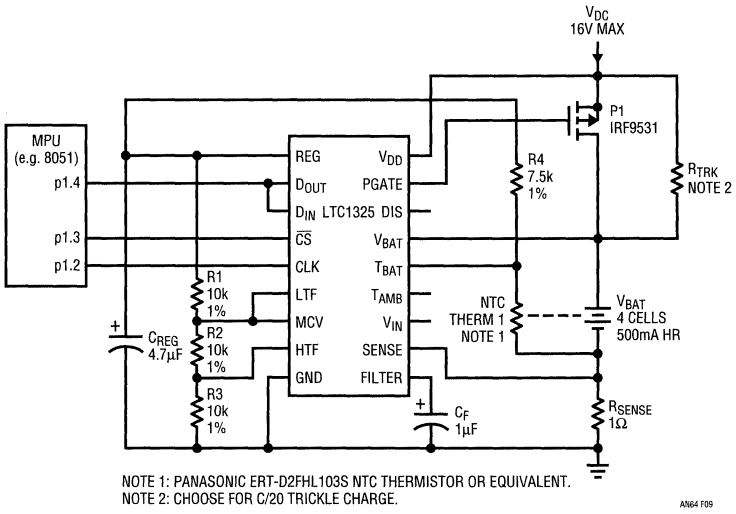


Figure 9. LTC1325 Charger Using an External Constant-Current Supply

is terminated by the microprocessor, or a fail-safe occurs. As shown in Figure 9, the inductor and catch diode that are normally connected to the positive terminal of the battery are not required, as no PWM switching action occurs at the drain of MOSFET P1.

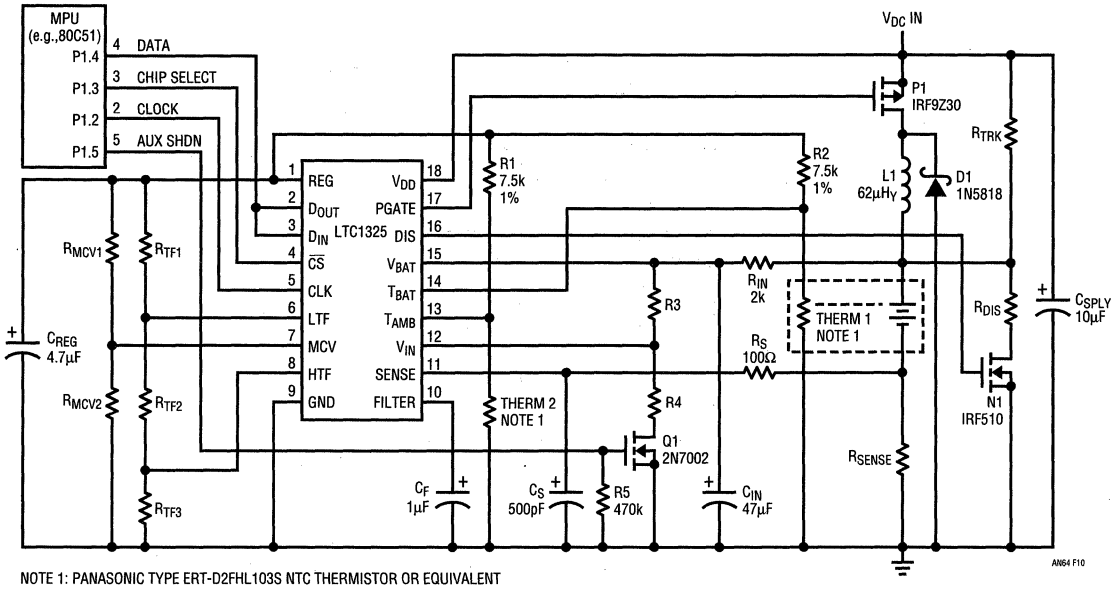
With the wall adapter connected, the current into the battery will always be ($I_{ADAPTER} - I_{EQUIPMENT}$). The use of one additional operational amplifier, such as the LT1077, allows monitoring this charging current by integrating the voltage across R_{SENSE} during the charging interval. The result of this integration can then be measured using the LTC1325's auxiliary ADC input V_{IN}. Combined with the built-in gas gauge function during the discharge interval (via the Sense input), the state of charge of the battery may be reliably determined at any time.

If the battery pack is heavily depleted or is damaged, the wall adapter can still be used to operate the equipment by putting the LTC1325 into Idle mode. Under these conditions the battery will receive no charging current (except through the trickle charging resistor, if one is provided). If the gas gauge is not needed, R_{SENSE} can be removed and the Sense pin should be returned to ground.

Constant-Potential Charging (Lead-Acid and Lithium-Ion)

Constant-current charging, which is the technique of choice for NiCd and NiMH batteries, is not recommended for most Lead-Acid or Lithium-Ion applications. Instead, a constant-voltage charging regimen is required, usually with a means of limiting the initial charging current. Such a charging technique is generally referred to as a "Constant-Potential" (CP) regimen.

The LTC1325 is at first glance a constant-current part. Such a view of its capabilities, however, is too limited. Its power control section is more completely described as a constant-average-current PWM with both hardware and software feedback. The hardware loop used for current sensing is the Sense input; the software loop, which can be used to control the effective output voltage of an LTC1325 charger circuit, is the microprocessor control routine in conjunction with the ADC and the DAC. Given a suitable output filter (the output inductor and the battery itself), current from the PWM section can be made to produce a current-limited constant voltage at the battery's terminals. A circuit intended for such CP operation is shown in Figure 10.



NOTE 1: PANASONIC TYPE ERT-D2FHL103S NTC THERMISTOR OR EQUIVALENT

Figure 10. Constant Potential Battery Management System

Batteries that require a CP charging algorithm generally need a rather accurate charging voltage, especially in fast-charge applications. For this reason the LTC1325's internal battery divider often cannot be used to control the charging voltage, due to its tolerance of ±2% at division ratios other than 1:1. It does, however, remain useful for MCV and/or FEDV detection. For measuring battery voltage an external resistive divider feeding V_{IN} is recommended. The external divider resistors should be chosen such that the voltage at the V_{IN} pin will come as close as possible to the ADC'c full-scale input voltage without exceeding that value; 3.000V maximum is a good choice. Using a near-full-scale input to the ADC improves measurement accuracy. To further improve charging voltage accuracy, it's a good idea to use ±0.1% or ±0.25% tolerance resistors in the battery voltage divider. Under such conditions, the voltage loop error is ideally only the reference error (±0.8%), plus that of the ADC (4 bits out of 1024, or ±0.4%) and of the battery divider (±0.1% or ±0.25%), for a total ±1.3% or ±1.5% error.

"Auxiliary Shutdown" is a static line from the microprocessor to a small-signal MOSFET, which prevents the battery from discharging through the voltage divider string when it is not charging. With the external divider in place, the BATP flag will always be high except when Auxiliary Shutdown is at a logic low and the battery is not installed in the circuit (see "Charging 'Tall' Batteries" above). Battery voltage fail-safes will remain operational (assuming that they use the V_{BAT} input) although it may not be possible to make simultaneous use of the MCV and EDV fail-safes with all CP battery types. R_{TRK}, if needed, maintains the battery in a fully charged condition.

A suitable software algorithm to implement a quasi-CP charger is this:

1. Establish a regular repetition interval for the voltage servo loop. t_{LOOP} values of 10ms to 20ms give good results.
2. Set V_{DAC} to 160mV at the highest charge rates for best resolution. Using a 95% maximum PWM duty cycle $[t_{ON}/(t_{ON} + t_{OFF})]$, R_{SENSE} chosen as $160mV/(0.95 \times I_{MAX})$, where I_{MAX} is the nominal maximum current to be allowed through the battery. A suitable minimum duty cycle is 10%; beyond such a low duty cycle it is

usually better to reduce the peak current through the battery (by programming V_{DAC}) than to reduce the duty cycle further.

3. Perform each of the following tasks once each servo loop interval (t_{LOOP}):
   a) Enter Idle mode of operation.
   b) Read V_{CELL}.
   c) Adjust the value entered into a timer register (or a software timer) up or down according to actual V_{CELL} vs target V_{CELL}. If V_{CELL} is too low, the timer value is increased. If V_{CELL} is too high, the timer value is decreased.
   d) The maximum Charge time of the LTC1325 has been set at 95% of t_{LOOP}; the minimum at 10%. Within that range, the duty cycle at which the loop will operate is set by the timer of 3(c). If the timer's interval is increased (V_{CELL} too low), the portion of each t_{LOOP} during which the LTC1325 is put into Charge mode is increased. If the timer's interval is decreased (V_{CELL} is too high), the LTC1325 is commanded into Idle mode for a greater portion of each t_{LOOP}.
   e) If $t_{ON} < (0.1 \times t_{LOOP})$, switch V_{DAC} to the next lower value (note that the V_{DAC} value of 34mV is not used).
   f) Repeat (a) through (e) until the average current into the battery, or the net duty cycle, drops below a chosen limit. A timer-based secondary cutoff is often recommended for CP chargers.
   g) Terminate the software loop with MOSFET P1 in the "off" state, using R_{TRK} (if required) to maintain the battery's charge.

A flow chart showing the principals of this voltage servo loop is given in Appendix B, Figures B3a and B3b. Figure B3a shows the "ramp-up" from the point where the charger is first turned on to the maximum charging current required and Figure B3b shows the "taper-down" which simulates the necessary CP charging algorithm. (This algorithm is undergoing refinement at press time. For the latest information on its implementation and optimization, please contact LTC.)

R_{IN} and C_{IN} have greater values in Figure 10 than in most of the circuits in this Application Note. This is because batteries requiring a CP charge tend to have a significant positive ΔV during the interval in which charging current is flowing through them. The time constant of $(R_{IN} \times C_{IN})$ filters the resulting 10ms to 20ms ripple before it is presented to the V_{BAT} and V_{IN} pins. If only V_{IN} input will be used, R_{IN} may be omitted, C_{IN} may be placed from V_{IN} to ground, and its value can be decreased.

The circuit of Figure 10 has deliberately been generalized to provide flexibility across all common battery types. For applications requiring the support of only specific battery types, or which do not need extensive thermal or other protection mechanisms, various components can be modified or removed to minimize cost and board space.

Overcurrent Protection

Three common scenarios in which battery current can exceed acceptable levels are: accidental shorting of the battery terminals, excessive loads and inserting the battery into the charger in reverse. Battery or charger damage in all three cases can be prevented through the use of a thermal or overcurrent device to limit fault currents. Usually, it is desirable that this device reset itself when the fault goes away. Possible choices are bimetallic (thermostatic) switches and polymer PTC thermistors. The high series resistance of traditional ceramic PTC thermistors, even in the unexcited state, make them unsuitable for this application.

Bimetallic switches operate by sensing battery temperature. By the nature of their operation, these switches cycle on and off as long as the fault remains, causing the battery and all associated components (mechanical as well as electrical) to heat up and cool down repeatedly. Polymer based PTC thermistors such as the Raychem PolySwitch® also offer very low series resistance until "tripped," and have the advantages of a faster response and freedom from thermal cycling.

Polymer PTCs should be chosen such that under normal operation, the average charging current (V_{DAC}/R_{SENSE}) is less than the Hold Current rating of the PTC to keep it in the low resistance state. Under fault conditions, the Fuse Current should exceed the Trip Current rating of the fuse. This will cause the fuse's resistance to increase dramatically and reduce the fault current to about $V_{BAT}/R_{FUSE}(Trip)$.

PolySwitch is a registered trademark of Raychem Corporation.

The PolySwitch should ideally be placed between cells in the battery, in close physical contact with one of the cells. In this way the trip point of the device will be reduced as the battery's temperature increases. Such a configuration provides substantial protection for the battery against shorts across its terminals and from excessive load currents. It will also protect the battery if it is accidentally inserted into the charger in reverse.

Figure 11 shows the fault current path when a battery is inserted into a charger in reverse. Potentially damaging currents may flow through this path since the Sense resistor is usually in the region of 1Ω or less. A PolySwitch inside the battery pack (as described above), or in series with the Schottky diode, limits fault currents to safe levels. The following points should be noted in choosing the diode and R_{SENSE}.

- Normal charging currents should be equal to or less than the holding current rating of the PolySwitch.
- Temperature affects PolySwitch performance. The manufacturer's data should be consulted for derating factors.
- Initial fault currents will be approximately V_{BAT}/R_{SENSE} if the battery is inserted in reverse. This should exceed the trip current rating of the PolySwitch.
- The wattage of R_{SENSE} should be high enough to withstand the initial fault currents of V_{BAT}/R_{SENSE}.
- The surge current rating of D1 should exceed the initial fault current of V_{BAT}/R_{SENSE}. It may be necessary to confirm the selected diode's applicability with the manufacturer of the part.

In addition to the above scenarios, the battery current may exceed acceptable levels when a battery is inserted into a charger which has the charging supply (V_{DC}) turned off. If the V_{DC} supply exhibits a low impedance path to ground when it is turned off, the diode that is intrinsic to the P-channel MOSFET may turn on to form a battery discharge path which flows from the battery's positive terminal through the inductor, the MOSFET internal diode, the ground lead and the sense resistor before returning to the negative terminal of the battery. This can be prevented by connecting a Schottky diode between V_{DC} (diode anode) and the source of the P-channel. See the section on "Current Sinking V_{DC} Sources" for more details.

Current-Sinking V_{DC} Sources

In some applications, it may be necessary to add a Schottky rectifier between the V_{DC} supply and the source of MOSFET P1. This rectifier prevents the battery from discharging backwards through MOSFET P1, which could damage P1, L1, or R_{SENSE}. It is required if the following conditions are met:

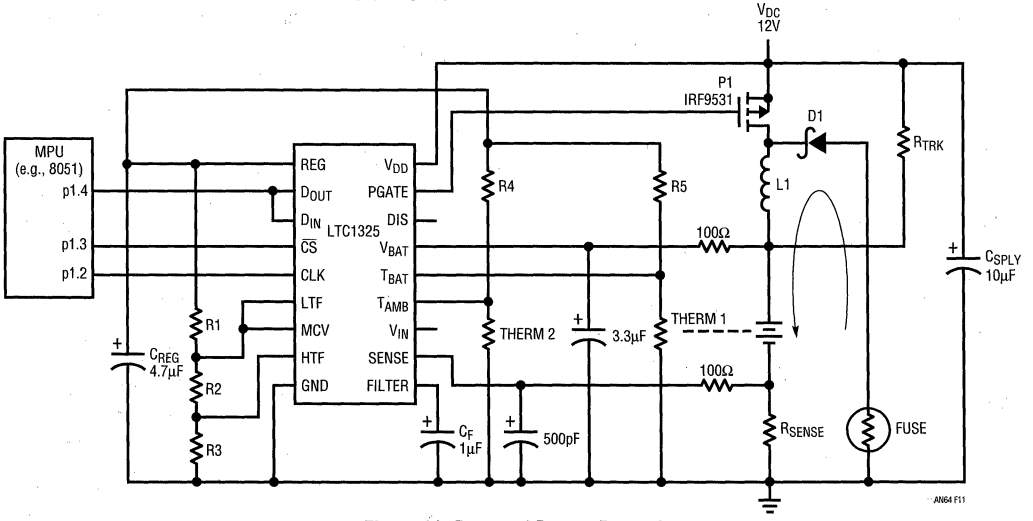


Figure 11. Reversed Battery Protection

- The voltage of the battery being charged can exceed that of the supply.
- The V_{DC} supply can sink current when it is at a lower voltage than the battery being charged.

Most switching power supplies, such as those used for AC adapter and battery charger supplies in portable computers, have a very small reverse leakage current—several milliamperes at most. These would not generally need the additional Schottky rectifier. Two examples of situations where the rectifier *is* necessary are:

- Charging a 7.2V or greater battery from a 12V car battery using the cigarette lighter socket. Under cold-cranking conditions the 12V nominal battery drops to 6V to 7V and an automobile's wiring will allow the starter motor to pull current back out of the lighter socket.
- Bench-top testing. Many power supplies have internal protection circuitry which will sink current from the load rather than allow a sourcing load, such as a charged battery, to force current indiscriminately into the supply's output. Also, any supply with a crowbar represents a possible current-sinking power supply.

Figure 12 depicts a basic charger circuit and shows the proper placement of the Schottky rectifier D_{IN}.

CONCLUSION

Through its ability to accept commands from almost any microprocessor, the LTC1325 takes advantage of the power and flexibility of software to avoid locking the user into any given battery type. This almost endless configurability enables the battery system designer to choose the required charge regimen, charge rate and charge termination technique(s) for virtually any task. Possibilities range from a robust but basic battery charging technique to sophisticated multiple-stage charging algorithms, or even several different algorithms entirely, all executed with the same hardware. In this way a wide range of battery types or end application needs can be accommodated with the same circuit. The on-board fault detection circuitry provides additional confidence in the final design by acting as a "watchdog" on the microprocessor and the battery pack. The design of the overall charging circuit is made as simple as possible by incorporating all the functional blocks needed and minimizing the discrete component count. In addition to charging batteries, the LTC1325 has provisions to condition batteries and to measure battery capacity. As with the LTC1325's charging-related functions, these capabilities are afforded a maximum of versatility and value by being placed almost completely under software control.

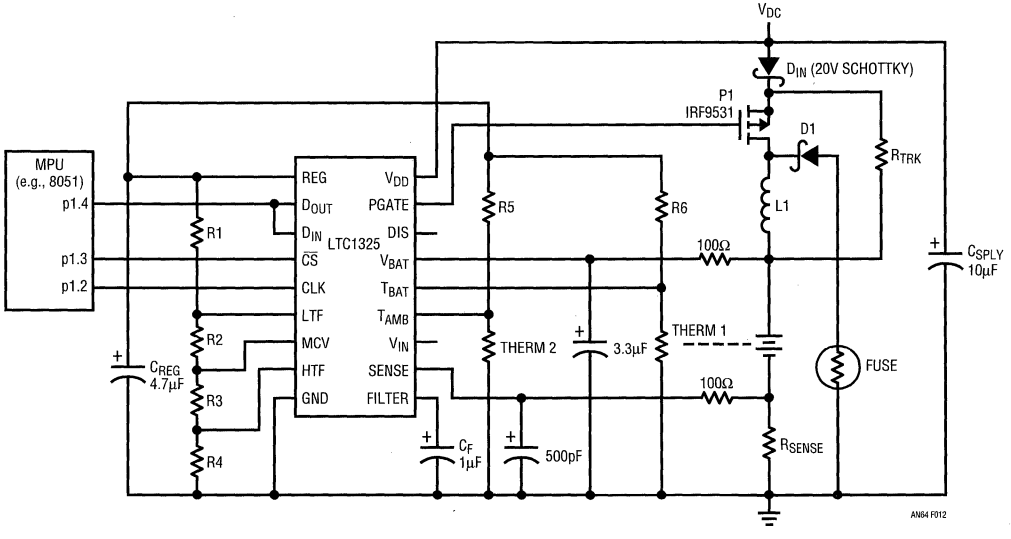


Figure 12. Protection Against Discharging Through V_{DC}

APPENDIX A

An Overview of Battery Types, Terminology, and Techniques

The world is increasingly relying upon portable electronic equipment, and the rechargeable battery systems (battery, battery charger and ancillary functional blocks) which power that equipment. These battery systems are among the defining elements of end product capability, endurance and life. In spite of this, they are commonly considered a necessary evil; their design and testing, a black art. The truth is that commercially viable battery management systems are comprised of well understood electronic and electrochemical components, with well defined performance characteristics. While this Appendix is not intended as a comprehensive treatment of battery technology, it will provide the equipment engineer with practical information for the choice of battery types and battery management techniques.

There are three rechargeable battery types commonly used in portable devices. These are Nickel-Cadmium (NiCd), Nickel-Metal Hydride (NiMH) and Sealed Lead-Acid (SLA). Lithium-Ion (Li-Ion) is also beginning to receive significant attention, primarily due to its very high energy density (as measured in terms of volume and of weight). Table A1 gives a quick overview of the characteristics of these battery types:

Table A1. Battery Type Characteristics

BATTERY CHARACTERISTICS	SEALED LEAD-ACID	NiCd	NiMH	LITHIUM-ION
Energy Density W-h/kg	30	40	60	90
Energy Density W-h/liter	60	100	140	210
Cell Voltage (V)	2.0	1.2	1.2	4.20 Max 3.60 Avg 2.50 Min
Charging Method	Constant Potential	Constant Current	Constant Current	Constant Potential
Dicharge Profile	Mildly Sloping	Flat	Flat	Sloping
#Charge/Discharge Cycles*	300	>500	>500	500 to 1000
Self-Discharge	3%/MO	15%/MO	20%/MO	6%/MO
Internal Resistance	Low	Lowest	Moderate	Highest
Discharge Rate**	> 4**C**	> 10**C**	3**C**	< 2**C**

* Until 80% of rated capacity is available upon discharge.

** **C** is the capacity rating of the battery in Ampere-Hours.

A useful first-approximation view of a rechargeable battery is that it is a container into which energy may be poured as desired, to be subsequently consumed as needed. This analogy generally conjures up an image of a jar of water, which would impose few restrictions upon rates of filling or emptying the vessel. In fact, a battery is more akin to a bottle of thick syrup, with the bottle having a narrow mouth and a wide base. With such a bottle, the syrup must be delivered into the bottle at a controlled rate and pressure (to prevent possible damage to the delivery system or to the neck of the bottle), and may be drawn at a maximum rate determined by the amount of syrup in the bottle and the bottle's shape. To carry this analogy just a little further, it is true of batteries, as it is with the hypothetical syrup bottle, that it is possible to get almost all of the contents out of the container — but it may take a long time to get the last few percent out. The flow rate will vary with the amount remaining, meaning that in situations where a high rate of discharge is required of a battery, not all the "contents of the bottle" — not all the available energy — will be instantaneously available to the discharging circuit.

Battery recharge times generally break down into several groups. The most common of these are the "standard-charge," suitable for overnight applications (typically requiring 16 hours) and the "fast-charge" (typically two hours or less). Between the two is the "quick-charge," which is in many respects akin to a standard-charge but requires a useably shorter interval (about five hours). Examples of standard-charge applications are cordless telephones and UPS systems for small computers. Quick-charge batteries are commonly found in devices which will see brief but significant power drain several times daily, such as cellular phones. Laptop computers and cordless tools are excellent locations for fast-charge systems. In these and other fast-charge uses there is a high average drain on the battery, and the product's value is determined in large part by the availability of battery power upon demand. The LTC1325 forms a comprehensive core for battery management systems operating at any of these charge rates; all that need be changed are a few external components and the microprocessor algorithm used to control the charge cycle. **Only batteries designed and rated for fast-charge should be subjected to a fast-**

charge regimen. Similarly, only batteries rated for quick-charge should be subjected to quick-charging conditions.

As might be expected, there are important differences between the charging regimens used for the four different battery types. There are also more similarities than might be expected. Each of the following sections is intended to stand alone, but it is suggested that the battery system designer read all four sections in order to get a feel for where the similarities and differences between battery families lie. Terms which are specific to the battery user community, or which have special meanings in this Appendix, are defined in the Glossary in Appendix C.

Using Nickel-Cadmium Batteries

Nickel-Cadmium batteries, in various forms, have been in use for over 50 years. During that time they have evolved from expensive, special purpose devices to the battery of choice for most portable equipment. The availability of inexpensive sealed cells, with ongoing improvements in energy density and cycle life, have been the driving forces for this acceptance. The LTC1325 adds to this the ability to easily implement fast-charge routines, gas gauge algorithms and/or switch mode constant current sources, all using very little system overhead and printed circuit board space.

A quick run-down of the pros and cons of Nickel-Cadmium batteries:

The "pros":

- Good energy density, both by weight and by volume, relative to competing technologies.
- Acceptable charging rates range from 0.1**C** to 2**C** and beyond.
- Most NiCd cells can accept a continuous overcharge current of 0.1**C**.
- A very flat discharge profile.
- The lowest cell impedance of the major battery technologies.
- Well understood and documented electrical behavior and electrochemistry.
- Cells and batteries are available in a variety of sizes from a number of vendors.
- Special purpose batteries are available with extended operating temperature ranges.

The "cons":

- Cadmium is commonly considered an environmentally hazardous material. Nickel is also coming under environmental scrutiny.
- NiCd cells have a significant self-discharge rate (0.5%/day at room temperature).

Nickel-Cadmium Standard-Charge

For applications which can allow a recharge period of about 16 hours — an "overnight" charge — the standard-charge regimen is the method of choice. The reasons for this include:

- Simplest charging algorithm.
- Least expensive charge termination techniques.
- Small power supply required to provide the charging current.
- Small charging circuit power components.
- Low overall charging system power dissipation.

A standard-charge is relatively straightforward to implement. In "cookbook" form, such a charge requires:

- Charging Current: 0.1**C**.
- Required Charging Voltage: 1.60V/cell or greater, plus charger overhead.
- Charging Temperature Range: 0°C to 45°C.
- Charging Time: 16 hours.
- Charge Termination Method: None required.
- Secondary Charge Termination Methods: None required.
- Special issues which may require further consideration are: wide temperature range charging, wide temperature range discharging and accurate gas gauging at temperature extremes.

A charging current of 0.1**C**, fed to the battery for 16 hours, will deliver (16 hours × 0.1**C**) = 160% of standard capacity to the battery. At temperatures between 0°C and 25°C, the resulting 60% overcharge is adequate to ensure that the battery is returned to 100% of its standard capacity. Once

the cells in the battery reach their actual capacity for the operating temperature, mild gassing will occur, but not enough to cause venting or other cell damage. Since most NiCd batteries will accept a continuous 0.1**C** charge at any case temperature between 0°C and 50°C, charge termination per se is usually not required. For specialized applications, extended temperature range batteries are available which can be charged at 70°C. Charging at temperatures below 0°C is also possible if the charge current is "throttled back" as the battery temperature decreases. The charging current under such conditions should linearly decrease from 0.1**C** at 0°C to zero current at –15°C to –25°C. In wide temperature range applications, the use of a battery (or ambient) temperature sensor in conjunction with the LTC1325 is an excellent way to provide positive control of battery charging current versus temperature, thereby extending battery life.

The charge acceptance of NiCd batteries is reduced significantly at temperatures above 40°C. This effect is only marginally mitigated by longer charge times, and should be taken into account if gas gauging is to be done over extended temperature ranges. By way of example, a battery that can be fully recharged at 25°C in 16 hours will reach only about 75% of standard capacity at 45°C after 48 hours. Again, no damage will be done to the battery, but its available capacity during subsequent discharge will be less than one would otherwise expect. If correction parameters for the gas gauging function of the LTC1325 will be employed, it is recommended that the manufacturer of the specific battery in question be consulted.

In the same way that charge acceptance is reduced for temperatures above 25°C, actual capacity is reduced when discharging a cell at temperatures much removed from 25°C. The battery temperatures at which actual capacity is 85% of standard capacity are approximately 0°C and 50°C. Again, for more specific data, the manufacturer of the battery to be used should be contacted.

Specially rated NiCd cells can support a higher rate of relatively uncontrolled overcharge than the ubiquitous 0.1**C**. This allows the quick-charge regimen, which is typically 0.33**C** for 5 hours. Charging current and interval aside, most other details for performing a quick-charge are the same as for a standard-charge. It is often desirable in quick-charge regimens to use a timed charge, reducing the charger's output current to a 0.05**C** trickle-charge after the five-hour recharge interval. Checking the cell manufacturer's data will provide further information on this, as well as the specified charge rate, permissible continuous overcharge rate, and information on the allowable temperature range.

Under some conditions, it may be desirable to use a lower charging rate than 0.1**C** (for instance, to reduce charger power requirements). This is feasible only within a narrow range: NiCd cells have a reduced charge acceptance at lower charge rates, lengthening the required charge time. This, and their self-discharge characteristic (approximately 0.5%/day at 23°C), combine to make anything under 0.05**C** a very slow and potentially unreliable charge rate for most cell types.

Nickel-Cadmium Fast-Charge

In recent years a class of applications has arisen for which 5 hours to 16 hours may constitute an excessive recharge time. Portable computer equipment is an excellent example of this — even if the battery pack in a laptop can be "swapped out" for external recharge, it is often needed again within several hours, fully charged and ready for use. In this case, the fast-charge techniques which the LTC1325 makes practical are the way to go. A fast-charge regimen implies:

- 90% recharge within one hour; 100% recharge within two to three hours.
- A method for determining the optimum charge termination point(s).
- Backup charge termination method(s) to ensure best battery life.
- Highly efficient use of available charging energy.
- Increased product value through better battery utilization and greater customer satisfaction.

Unlike the standard-charge and quick-charge regimens, there is no one best way to fast-charge a Nickel-Cadmium battery. Variables introduced by the allowable cost and size of the end application, the continuing evolution of Ni-Cd cells to accomodate faster charge rates, and the specific battery vendor(s) chosen will all influence the final choice of charging technique. There are several areas of

industry consensus, however, regarding the suitable fast-charging of NiCd batteries:

- Charging Current: 1.0**C** to 2.0**C**.
- Required Charging Voltage: 1.80V/cell or greater, plus charger overhead.
- Charging Temperature Range: 10°C to 40°C.
- Charging Time: Three hours (90% of charge is typically returned within the first hour).
- Suitable Charge Termination Methods: See Table A2.
- Suitable Secondary Charge Termination Methods: See Table A2.
- Special issues which may require further consideration are: accurate gas gauging at temperatures over 25° C, and appropriate mechanical integration of the battery pack into the end equipment.

The objective of fast-charging a NiCd battery is, crudely stated, to cram as much energy as it takes to bring the battery back to a fully charged state into that battery in as short a time as possible. Since current is proportional to energy divided by time, the charging current should be as high as the battery system will reasonably allow. Generally, NiCd batteries rated for fast-charge use are designed around a 1**C** to 2**C** maximum charging rate. At the 1**C** rate, more than 90% of the usable discharge capacity of the battery is typically returned within the first hour. Higher rate cells (up to 5**C**) do exist, but they are more oriented to special applications and will not be discussed here, except to note that the LTC1325 is capable of handling the charging routines required for such cells, should that be required.

Fast-charging has compelling benefits, but places certain demands upon the battery system. A properly performed fast-charge can yield a cell life of as many as 500 charge/discharge cycles. The high charging rates involved, however, do engender correspondingly more rapid electrochemical reactions within the cell. Once the cell goes into overcharge, these reactions cause a rapid increase in internal cell pressure, and in the cell's temperature. Figure A1 shows the Voltage, Pressure and Temperature characteristics of a Nickel-Cadmium cell being charged at the 1**C** rate. It can be seen that, as the cell approaches 100% of

Table A2. Fast-Charge Termination Techniques for Nickel-Cadmium Batteries

Voltage Cutoff (VCO)	Uses absolute cell voltage to determine the cell's state of charge. Not generally recommended for use in NiCd charging regimens.
Negative ΔV (–ΔV)	Looks for the relatively pronounced downward slope in cell voltage which a NiCd exhibits (≈30mV to 50mV) upon entering overcharge. Very common in NiCd applications due to its simplicity and reliability.
Zero ΔV	Waits for the time when the voltage of cell under charge stops rising, and is "at the top of the curve" prior to the downslope seen in overcharge. Sometimes preferred over –ΔV, as it causes less overcharging.
Voltage Slope (dV/dt)	Looks for an increasing slope in cell voltage (positive dV/dt) which occurs somewhat before the cell reaches 100% returned charge (prior to the Zero ΔV point). No longer widely used.
Inflection Point Cutoff (d^2V/dt^2, IPCO)	As a NiCd cell approaches full charge, the rate of its voltage rise begins to level off. This method looks for a zero or, more commonly, slightly negative value of the second derivative of cell voltage with respect to time.
Absolute Temperature Cutoff (TCO)	Uses the cell's case temperature (which will undergo a rapid rise as the cell enters high-rate overcharge) to determine when to terminate high-rate charging. A good backup method, but too susceptible to variations in ambient temperature conditions to make a good primary cutoff technique.
Incremental Temperature Cutoff (ΔTCO)	Uses a specified increase of a NiCd cell's case temperature, relative to the ambient temperature, to determine when to terminate high-rate charging. A popular, relatively inexpensive and reliable cutoff method.
Delta Temperature/Delta Time (ΔT/Δt)	Uses the rate of increase of a NiCd cell's case temperature to determine the point at which to terminate the high-rate charge. This technique is inexpensive and relatively reliable as long as the cell and its housing have been properly characterized.

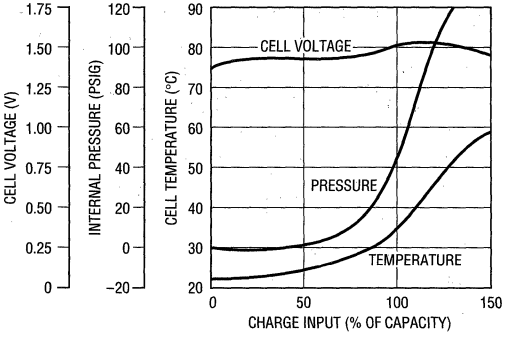


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Figure A1. NiCd Voltage, Pressure, and Temperature Characteristics During Charge at 1C (23°C Ambient)

capacity, the charging current must be reduced or terminated. Left unchecked, overcharge at the **C** rate will ultimately cause the cell's safety vent to open. This results in a loss of gaseous electrolyte to the ambient, and a permanent diminution of cell capacity. Similarly, allowing the temperature of the cell to rise excessively will cause a degradation of the internal materials, again reducing cell life. The science of fast-charging is largely that of determining when the battery has achieved between 90% and 100% of its dischargeable capacity. At that point the charging circuit must switch from the fast-charge current level to a level appropriate to finish the charging of, and/or maintain the charge on, the battery. Some of the common methods for doing this are outlined in Table A2.

As Table A2 shows, there are a number of techniques which have been been successfully employed for the purpose of determining when to terminate the high-rate interval of a fast-charge regimen. Individual application requirements, and manufacturer's recommendations, must of course be considered carefully before making a final design decision. Nonetheless, two techniques for detecting the point at which to make the transition from high-rate charging to top-charging have become especially popular over the years, and are used here as examples. These are the $-\Delta V$ and the ΔTCO methods. The $-\Delta V$ approach looks for a point at which the cell or battery voltage reaches its peak during charging, and holds this maximum value. The high-rate charge is then terminated when the voltage per cell has declined by a value of 15mV to 30mV. ΔTCO sensing uses two thermistors to measure the case temperature of the cell, or of one of the cells in a battery, while also measuring the ambient temperature. A 10°C differential between cell and ambient is the typical high-rate termination criterion. (A single-thermistor variant on the "classic" ΔTCO approach is made possible through the combined power of the LTC1325 and a microprocessor: cell temperature is measured just before commencing charge, and assumed to be the ambient temperature. This baseline value then becomes the reference against which all further temperature measurements are compared.)

For illustration of the fast-charging of NiCd batteries, this document will use a 1**C** charge rate, in a three-stage algorithm. The three stages are:

- Fast-Charge at the 1**C** rate, until it is determined by the charging system that the high-rate portion of the charge regimen must be terminated. At this point, a 1**C** charge will typically have returned between 90% and 95% of the battery's actual capacity.
- Top-Charge at 0.1**C** for two hours, to add an additional 0.2**C** to the battery. This will bring the battery back to 100% of usable capacity.
- Trickle-Charge at between 0.02**C** and 0.1**C** to counter the NiCd's self-discharge value of about 0.5%/day.

Unless the battery is being used in an unusual application, there is little advantage in using a trickle-charge rate different from the 0.1**C** top-charge rate, which most NiCd cells can tolerate indefinitely. If the trickle-charge is the same as the top-charge rate, the charge regimen illustrated effectively has only two stages. This is not uncommon for NiCd batteries.

It cannot be overstated that the high-rate portion of a fast-charge regimen must be terminated once the battery being charged has reached the appropriate cutoff point. Murphy has taught us to prepare for the unexpected. So for each method consider: "How can this method fail?" To give just one example of each case: contact resistance in the charging path could mask the downslope of the battery's terminal voltage, causing the microprocessor to miss the $-\Delta V$ termination point. For ΔTCO termination, the ambient temperature might not be indicative of the battery's temperature at the start of charge (e.g., recharging of a battery just removed from a cooler environment to a warmer one),

which would keep a significant battery-to-ambient temperature differential from appearing. Failure of the charger system to recognize the cutoff point, for whatever reason, can quickly and irretrievably damage the battery. To avoid such damage, inexpensive redundancy is the solution. With the capabilities of the LTC1325 already at hand, the best plan is to simply employ both methods. It is then reasonable to expect that one of the two techniques will result in a successful high-rate charge termination. In this example regimen a good choice for the primary high-rate charge termination for NiCd batteries would be $-\Delta V$ sensing, with ΔTCO serving as a backup. To give Murphy's gremlins a harder time of it, there are maximum and minimum operating temperatures and cell voltages which the LTC1325 can be set to recognize. The LTC1325 also has a timer feature which will turn off the charge current to the battery unless the timer is reset within a certain interval. These preset limits serve to protect the battery from severe overcharge even if the system's microprocessor should fail altogether.

As mentioned above, fast-charge current levels can cause rapid gas evolution within a NiCd cell. Since gas recombination inside the cell is slower at reduced temperatures, the pressure inside the cell will rise as the cell temperature decreases. This places a lower limit on the permissible fast-charge temperature range. Similarly, the cell's charge acceptance decreases at elevated temperatures. Hence, although gas recombination occurs much more rapidly, there is the danger of more gas being generated than the cell mechanisms can handle. This places an upper boundary on the fast-charge temperature range. Putting numbers to these limits, 10°C to 15°C are common minimum figures with the high end at 40°C to 45°C. Using the LTC1325 in conjunction with the microprocessor to ensure that the indicated operations occur within the manufacturer's rated temperature limits will significantly extend the life of the cell or battery.

For the most accurate gas gauging it may be desirable to take into account the battery's actual temperature during charge and its temperature during discharge. Both of these have an effect upon the ratio of actual capacity to standard capacity. This effect may be especially pronounced if the battery is charged at an ambient temperature above 25°C and/or discharged at 0°C or below. For specific data with which to calibrate the gas gauge function against charge and discharge temperatures, the manufacturer of the cells or batteries being used should be contacted.

During fast-charge the battery will get warm and may vent in the unlikely case of overstress or failure. It is prudent engineering to allow for these contingencies in the mechanical design stage of the equipment in which the battery will reside. Again, the manufacturer of the cells or battery to be used should be consulted for specific guidance.

Using Nickel-Metal Hydride Batteries

The Nickel-Hydrogen couple has been known for at least 20 years, but until recently it has been too costly for all but the most specialized of applications. Recent developments in the manufacture of the NiMH cell, specifically of the hydrogen-bearing negative electrode, has brought NiMH technology into the realm of commercial viability. At present NiMH batteries remain somewhat more expensive than either Nickel-Cadmium or SLA units. However, for applications requiring the energy densities which NiMH provides, it can readily justify its higher price. It should also be noted that NiMH is a mature enough technology to be useful and reliable, yet young enough that prices should continue to decline and performance to improve. The LTC1325's features and flexibility make it an excellent choice for Nickel-Metal Hydride applications, providing the ability to easily implement and modify fast-charge routines, gas gauge algorithms and/or switch-mode constant current sources, all using very little system overhead and printed circuit board space.

A quick rundown of the pros and cons of Nickel-Metal Hydride batteries:

The "pros":

- Excellent energy density, both by weight and by volume, relative to competing technologies.
- Acceptable charging rates range from 0.1**C** to 1**C** and beyond (fast-charge capability is virtually a given for NiMH).
- A flat discharge profile.
- Well understood and documented electrical behavior and electrochemistry.

- Cells and batteries are available in a variety of sizes from a number of vendors.
- It is anticipated that new cell formulations will eliminate all cadmium from the NiMH product.

The "cons":

- Nickel is coming under scrutiny as a potential ecological hazard.
- NiMH cells have a significant self-discharge rate (0.5%/day to 1%/day at room temperature).
- Careful attention to overcharge of NiMH cells is required, even at standard-charge rates.
- NiMH cells command a price premium relative to NiCd cells at the present time.
- MiMH cells do not presently cover the same temperature ranges as either NiCd or SLA units.

Nickel-Metal Hydride Standard-Charge

For applications which can allow a recharge period of about 16 hours — an "overnight" charge — the standard-charge regimen is the method of choice. The reasons for this include:

- Simplest charging algorithm.
- Least expensive charge termination techniques.
- Small power supply required to provide the charging current.
- Small charging circuit power components.
- Low overall charging system power dissipation.

A standard-charge is relatively straightforward to implement. In "cookbook" form, such a charge requires:

- Charging Current: 0.1**C**, switching to 0.025**C** trickle-charge.
- Required Charging Voltage: 1.60V/cell or greater, plus charger overhead.
- Charging Temperature Range: 0°C to 50°C.
- Charging Time: 16 hours.
- Charge Termination Method: Timer.
- Secondary Charge Termination Methods: None required.
- Special issues which may require further consideration are: wide temperature range discharging and accurate gas gauging at temperature extremes.

A charging current of 0.1**C**, fed to the battery for 16 hours, will deliver (16 hours × 0.1**C**) = 160% of standard capacity to the battery. At temperatures between 0°C and 25°C, the resulting 60% overcharge is adequate to ensure that the battery is returned to 100% of its standard capacity. Once this has occurred the charging rate must be reduced sufficiently that cell venting does not occur. At the same time the 1%/day self-discharge of the NiMH cell needs to be countered with a suitable trickle-charge rate. The resulting two-level constant-current charger usually switches in a 0.025**C** rate after the 0.1**C** main charge. A NiMH battery will show a modest temperature increase (typically 8°C to 9°C) after 16 hours of standard-rate charging. However, this value is not tightly defined and the rate of temperature rise is quite gradual at the end of the charging cycle. This rules out thermal charge termination for the standard-charge regimen. A better approach is a timed-charge technique which applies the standard-rate charging current for 16 hours and then drops back to a 0.025**C** trickle-charge. A refinement to this is to break the main charging interval into numerous shorter intervals under the control of the timer internal to the LTC1325. In this way, even if the microprocessor controlling the battery system should "lock up," permanent damage to the battery will be prevented. Charging at temperatures below 0°C or above 45°C is not recommended. In addition, NiMH batteries should not be discharged beyond the range of –20°C to 50°C. If a wide temperature excursion of the ambient is anticipated, the use of a thermal sensor in conjunction with the LTC1325 is an excellent way to ensure that battery operations occur only within their permissible temperature boundaries, which will significantly extend battery life.

The charge acceptance of NiMH batteries is reduced significantly at temperatures above 40°C. This effect should be taken into account if gas gauging is to be done over extended temperature ranges. In this regard, the performance of NiMH and Nickel-Cadmium batteries is quite similar. A NiMH battery that will recover 100% of standard capacity after 16 hours at 25°C will attain only about 85% of standard capacity at 45°C. Hence the battery's available capacity during subsequent discharge will be less than

one would otherwise expect. If correction parameters for the gas gauging function of the LTC1325 will be employed, it is recommended that the manufacturer of the specific battery in question be consulted.

In the same way that charge acceptance is reduced for temperatures above 25°C, actual capacity is reduced when discharging a cell at temperatures much below 25°C. Typical figures for actual capacity are 85% of standard capacity at 0°C, and 50% at –20°C. Again, for more specific data the manufacturer of the battery to be used should be contacted.

Generally speaking, it's not a good idea to use a lower charging rate than 0.1**C**. This is due in part to the fact that NiMH cells have a reduced charge acceptance at lower charge rates, lengthening the required charge time, and in part to the fact that their self-discharge rate of approximately 1%/day at 23°C increases quickly with temperature.

Nickel-Metal Hydride Fast-Charge

In recent years a class of applications has arisen for which 5 hours to 16 hours may constitute an excessive recharge time. NiMH batteries, with their relatively high energy densities, were perfected largely for the mobile portion of this market. Portable computer equipment is an excellent example of a NiMH fast-charge application — even if the battery pack in a laptop can be "swapped out" for external recharge, it is often needed again within several hours, fully charged and ready for use. In this case the techniques which the LTC1325 makes practical are the way to go. Such a fast-charge implies:

- 90% recharge within one hour; 100% recharge within two to four hours.
- A method for determining the optimum charge termination point(s).
- Backup charge termination method(s) to ensure best battery life.
- Highly efficient use of available charging energy.
- Increased product value through better battery utilization and greater customer satisfaction.

A fast-charge battery system involves:

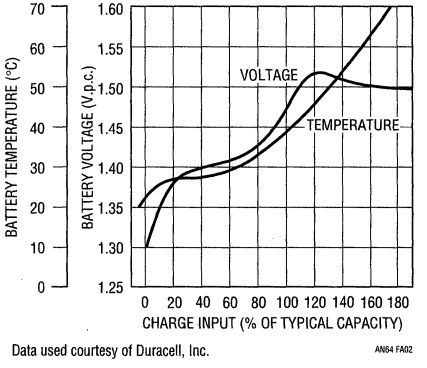
- Charging Current: 1.0**C**.
- Charging Time: Three hours (90% of charge is typically returned within the first hour).
- Required Charging Voltage: 1.80V/cell or greater, plus charger overhead.
- Charging Temperature Range: 15°C to 30°C optimal (consult manufacturer for permissible range).
- Charge Termination Method: See Table A3.
- Secondary Charge Termination Methods: See Table A3.
- Special issues which may require further consideration are: accurate gas gauging at temperatures other than 25°C and appropriate mechanical integration of the battery pack into the end equipment.

The objective of fast-charging a NiMH battery is, crudely stated, to cram as much energy as it takes to bring the battery back to a fully charged state into that battery in as short a time as possible. Since current is proportional to energy divided by time, the charging current should be as high as the battery system will reasonably allow. Generally, NiMH batteries are rated for a 1**C** maximum charging rate. At that rate, more than 90% of the useable discharge capacity of the battery is typically returned within the first hour. Of course, the LTC1325 will also support the charging of higher rate cells as they become available.

Fast-charging has compelling benefits, but places certain demands upon the battery system. A properly performed fast-charge can yield a cell life of as many as 500 charge/discharge cycles. The high charging rates involved, however, do engender correspondingly more rapid electrochemical reactions within the cell. Once the cell goes into overcharge, these reactions cause a rapid increase in internal cell pressure and in the cell's temperature. Figure A2 shows the Voltage and Temperature characteristics of a Nickel-Metal Hydride cell being charged at the 1**C** rate. It can be seen that, as the cell approaches 100% of capacity, the charging current must be reduced or terminated. Left unchecked, overcharge at the **C** rate will ultimately cause the cell's safety vent to open. This results in a loss of gaseous electrolyte to the ambient and a permanent diminution of cell capacity. Similarly, allowing the temperature of the cell to rise excessively will cause a degradation of the internal materials, again reducing cell life. The science of fast-charging is largely that of determining when the battery has achieved between 90% and 100% of its

Table A3. Fast-Charge Termination Techniques for Nickel-Metal Hydride Batteries

Voltage Cutoff (VCO)	Uses absolute cell voltage to determine the cell's state of charge. Not generally recommended for use in NiMH charging regimens.
Negative ΔV (–ΔV)	Looks for the downward slope in cell voltage which a NiMH exhibits (≈ 5mV to 15mV) upon entering overcharge. Common in NiMH applications due to its simplicity and reliability.
Zero ΔV	Waits for the time when the voltage of cell under charge stops rising, and is "at the top of the curve" prior to the downslope seen in overcharge. Sometimes preferred over –ΔV, as it causes less overcharging, and may be easier to detect reliably (due to the small –ΔV of a NiMH cell). Common in NiMH applications.
Voltage Slope (dV/dt)	Looks for an increasing slope in cell voltage (positive dV/dt) which occurs somewhat before the cell reaches 100% returned charge (prior to the Zero ΔV point). Not widely used.
Inflection Point Cutoff (d^2V/dt^2, IPCO)	As a NiMH cell approaches full charge, the rate of its voltage rise begins to level off. This method looks for a zero or, more commonly, slightly negative value of the second derivative of cell voltage with respect to time.
Absolute Temperature Cutoff (TCO)	Uses the cell's case temperature (which will undergo a rapid rise as the cell enters high-rate overcharge) to determine when to terminate high-rate charging. A good backup method, but too susceptible to variations in ambient temperature conditions to make a good primary cutoff technique.
Incremental Temperature Cutoff (ΔTCO)	Uses a specified increase of a NiMH cell's case temperature, relative to the ambient temperature, to determine when to terminate high-rate charging. A popular, relatively inexpensive and reliable cutoff method.
Delta Temperature/Delta Time (ΔT/Δt)	Uses the rate of increase of a NiMH cell's case temperature to determine the point at which to terminate the high-rate charge. This technique is inexpensive and relatively reliable as long as the cell and its housing have been properly characterized.



Data used courtesy of Duracell, Inc.

Figure A2. NiMH Voltage and Temperature Characteristics During Charge at 1C (20°C Ambient)

dischargeable capacity. At that point the charging circuit must switch from the fast-charge current level to a level appropriate to finish the charging of, and/or maintain the charge on the battery. Some of the common methods for doing this are outlined in Table A3.

As Table A3 shows there are a number of techniques which have been been successfully employed for the purpose of determining when to terminate the high-rate interval of a fast-charge regimen. Individual application requirements, and manufacturer's recommendations, must of course be considered carefully before making a final design decision. Several techniques for detecting the point at which to make the transition from high-rate charging to top-charging have gained especially wide acceptance in the NiMH community. Among these are the ΔT/Δt, the ΔTCO, the –ΔV, and the the d^2V/dt^2 methods. ΔT/Δt sensing measures the rate of change of the case temperature of the cell, or of a cell in the battery with respect to time. When this rate of rise reaches 1°C/minute, almost all of the dischargeable capacity has been returned to the cell and the high-rate charge should be terminated. ΔTCO sensing measures the difference between the case temperature of the cell, or of one of the cells in a battery, while also measuring the ambient temperature. A 15°C differential between cell and ambient is the typical high-rate termination criterion. The –ΔV approach looks for a point at which

the cell or battery voltage peaks during charging, and holds this maximum value. The high-rate charge is then terminated when the voltage per cell has declined by a value of 5mV to 10mV. The d^2V/dt^2 technique looks for a slowing rate of rise in the the battery's terminal voltage. This trend, properly filtered and processed by the system's software, will yield a negative second derivative of battery voltage when the battery approaches a complete recharge. **It is important to note that under certain conditions, particularly following intervals of storage, a NiMH battery may give an erroneous voltage peak as charging commences. For this reason, a reliable fast-charge cycle should deliberately disable any voltage-based sensing technique for the first five minutes of the charging interval.**

For illustration of the fast-charging of NiMH batteries, this document will use the regimen recommended by Duracell, Inc. The three stages of this regimen are:

- Fast-charge at the 1**C** rate, until it is determined by the charging system that the high-rate portion of the charging cycle must be terminated. At this point, a 1**C** charge will typically have returned between 90% and 95% of the battery's actual capacity.
- Top-charge at 0.1**C** for one hour to add an additional 0.1**C** to the battery. This will bring the battery back to 100% of usable capacity.
- Trickle-charge at 0.0033**C** to counter the self-discharge characteristic of Nickel-Metal Hydride, while not exposing the battery to excessive overcharge.

Nickel-Metal Hydride batteries suffer quickly and severely from protracted overcharge. To prevent damage to the battery all manufacturer's algorithms recommend a low trickle-charge value. As shown, Duracell recommends 0.0033**C** while many other vendors specify 0.025**C**. The exact value of this trickle-charge, as well as the specific overall charging regimen, is application and vendor dependent, so the literature of the selected battery supplier should be consulted.

It cannot be overstated that the high-rate portion of a fast-charge regimen must be terminated once the battery being charged has reached the appropriate cutoff point. Murphy has taught us to prepare for the unexpected. So for each method consider: "How can the this method fail?" To illustrate by example: contact resistance in the charging path could mask the downslope of the battery's terminal voltage, causing the microprocessor to miss the $-\Delta V$ termination point. For the case of $\Delta T/\Delta t$ termination, the ambient temperature might artificially prevent a rapid enough change in temperature from occuring (e.g., recharging of a battery while it sits in the airstream of an air conditioner). Failure of the charger system to recognize the cutoff point, for whatever reason, can quickly and irretrievably damage the battery. To avoid such damage, inexpensive redundancy is the solution. With the capabilities of the LTC1325 already at hand, the best plan is to simply employ two or more methods. It is then reasonable to expect that one of the techniques will result in a successful high-rate charge termination. In Duracell's suggested regimen the primary technique for terminating the high-rate charge is $\Delta T/\Delta t$ sensing, with $-\Delta V$ serving as a backup. To give Murphy's gremlins a harder time of it, there are maximum and minimum operating temperatures and cell voltages which the LTC1325 can be set to recognize. For example, Duracell recommends using a third, TCO-based "safety" to shut the high-rate charge down if the battery temperature ever exceeds 60°C absolute. The LTC1325 also has a timer feature which will turn off the charge current to the battery unless the timer is reset within a certain interval. Not only does this provide an extra margin of safety, it can simplify charging as well: Duracell's regimen calls for one hour of timer-controlled 0.1**C** overcharge. The LTC1325 can offload this timing job from the system processor. Hence, the battery charging task is simplified and the battery is protected from severe overcharge even if the system's microprocessor should fail altogether.

As mentioned above, fast-charge current levels can cause rapid gas evolution within a NiMH cell. Since gas recombination inside the cell is slower at reduced temperatures, the pressure inside the cell will rise as the cell temperature decreases. This places a lower limit on the permissible fast-charge temperature range. Similarly, the cell's charge acceptance decreases at elevated temperatures. Hence, although gas recombination occurs much more rapidly, there is the danger of more gas being generated than the cell mechanisms can handle. This places an upper boundary on the fast-charge temperature range. Putting numbers to these limits, 10°C to 15°C are common minimum

figures with the high end at 40°C to 45°C. This temperature span constitutes the limit for fast-charging of NiMH batteries; they will give longer life and better performance if charged between 15°C and 30°C. Using the LTC1325's measurement capabilities to ensure that the indicated operations occur within the manufacturer's rated temperature limits will significantly extend the life of the cell or battery.

For the most accurate gas gauging, it may be desirable to take into account the battery's actual temperature during charge and its temperature during discharge. Both of these have an effect upon the ratio of actual capacity to standard capacity. This effect may be especially pronounced if the battery is charged at an ambient temperature above 25°C and/or discharged at 0°C or below. For specific data with which to calibrate the gas gauge function against charge and discharge temperatures, the manufacturer of the cells or batteries being used should be contacted.

During fast-charge the battery will get warm and may vent in the unlikely case of overstress or failure. It is prudent engineering to allow for these contingencies in the mechanical design stage of the equipment in which the battery will reside. Again, the manufacturer of the cells or battery to be used should be consulted for specific guidance.

Using Sealed Lead-Acid Batteries

Lead-Acid batteries are the "venerable elders" among rechargeable power sources. They have been known in various forms for substantially over a century. But age does not imply weakness—many of the most significant developments in Lead-Acid cells, including those which have made the portable Sealed Lead-Acid (SLA) construction practical, have taken place in the last 30 years or less. Concerns about the safety and stability of the sulfuric-acid electrolyte system have been addressed, first by the well-known "Gel Cell," and thereafter by modern "starved-electrolyte" technologies. Improvements in the purity of materials, and the optimization of the internal cell structure for portable battery applications (as opposed to the traditional automotive market which imposes its own unique demands) have made the SLA battery a serious contender for many applications. In the smaller ratings SLA batteries compare favorably in cost per Watt-Hour with NiCd batteries and are superior to NiMH devices; in higher Watt-Hour ratings SLA technology is usually the clear choice. With a minimum of board space and system overhead, the LTC1325 provides a programmable switch-mode charging controller. It also carries on-chip all necessary battery monitoring and safeguard circuitry, and the means to readily implement gas gauge algorithms.

A quick rundown of the pros and cons of Sealed Lead-Acid batteries:

The "pros":

- The electrochemistry and electrical behavior of SLA batteries are very well understood and documented for moderate charge rates and for a broad range of discharge rates.
- SLA technology lends itself to prismatic batteries as well as cylindrical cells.
- SLA batteries are available with wider operating temperature ranges than either NiCd or NiMH batteries.
- Excellent cost/Watt-Hour, especially in larger size cells and batteries.
- Very low self-discharge rates: ≈ 0.2%/day at 25°C
- Low cell impedance with a good capability to handle high pulse currents.
- SLA cells are available in a variety of sizes from a number of vendors.

The "cons":

- The SLA cell has the lowest energy density, by weight and by volume, of all three technologies.
- SLA batteries deliver their best performance under a constant voltage (or pseudo-constant voltage) charge regime.
- Lead is commonly considered to be an environmentally hazardous material.
- SLA cells are susceptible to damage from overcharge, repeated deep discharge, and/or cell reversal.
- The discharge profile of a SLA cell is not as flat as that of a NiCd cell, nor as that of an NiMH cell in most applications.

Sealed Lead-Acid Standard-Charge

For applications which can allow a recharge period of 24 hours or more—any period from an extended "overnight" charge to a "float charge"— the standard-charge is the regimen of choice. The reasons for this include:

- No charge termination required.
- Frequently requires no temperature compensation.
- Small power supply required to provide the charging current.
- Small charging circuit power components.
- Low overall charging system power dissipation.
- Excellent battery life due to low charging stress.

An SLA standard-charge is relatively straightforward to implement. In "cookbook" form, such a charge requires:

- Charging Current: Limited to 0.25**C** or less.
- Charging Voltage: 2.25V/cell to 2.30V/cell, plus charger overhead.
- Charging Temperature Range: 0°C to 40°C.
- Charging Time: 24 hours or longer.
- Charge Termination Method: None required.
- Secondary Charge Termination Methods: None required.
- Special issues which may require further consideration are: wide temperature range charging, wide temperature range discharging, and accurate gas gauging under varying conditions of use.

Sealed Lead-Acid (SLA) batteries are generally charged using a constant voltage source with a deliberately imposed current limit (essentially a current-limited voltage regulator), or a charger which will, in terms of the electrochemical effects seen by the battery, act as if it were such a source. The charging regimen which this gives rise to is known as "Constant Voltage," or more commonly, "Constant Potential." For the purposes of this document the term "Constant Potential" (CP) will be used.

The reasons for using a CP charge regimen are various, but the three principal ones are these:

- Charge acceptance (the efficiency of conversion of previously removed electrical energy back into chemical potential) is reduced as the charging current through an SLA cell is increased.
- Once full charge is achieved, continued charging current through an SLA cell will have an irreversible oxidizing effect upon the positive plate of the battery, ultimately reducing battery capacity.
- Most importantly from the standpoint of designing a practical charger, there is no reliable way to know an SLA cell's state of charge based upon its terminal voltage or its temperature.

A significantly discharged cell undergoing CP charging will initially attempt to draw very high currents, as SLA cells are low impedance devices. The function of the current-limiting in the CP regimen is to keep the peak current flowing into the cell within the cell's (and the charger's) ratings. Following the current-limited phase of the charging profile, the CP charging technique in combination with the characteristics of SLA devices cause the cell under charge to in essence regulate its own charging current. If the cell vendor's recommendation as to charging voltage (typically 2.25V/cell to 2.30V/cell at 20°C) are followed, the cell's charging current will naturally taper off with time as the cell goes slightly into overcharge. Under these conditions a fully discharged cell will essentially cease charging once it has achieved a 110% returned charge which results in a 100% dischargeable capacity. The remaining 10% is lost to heating and other parasitic reactions. This simple charging concept, sometimes combined with compensation for ambient temperature (–2mV/°C to –3mV/°C, depending upon the manufacturer), will provide highly satisfactory results over a good temperature range. A range of 0°C to 40°C is typical, with some vendors specifying their products for operation at temperatures of 50°C or more. Figure A3 shows the way in which SLA charge current tapers off and the returned capacity rises under such a CP charging regimen. Figure A4, a reproduction of Figure 10 from the body of this Application Note, shows how the LTC1325 can be used to provide all the necessary functions for SLA battery management. As in the body of this Application Note, Figures B3a and B3b in Appendix B are also relevant here.

The charge acceptance of SLA batteries is reduced at temperatures below about 0°C, and actual capacity is reduced when discharging a cell at temperatures much

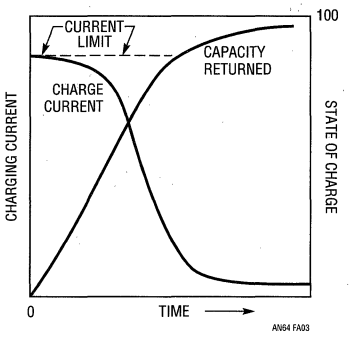


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Figure A3. Typical Charging Current and Capacity Returned vs Charge Time for CP Charging

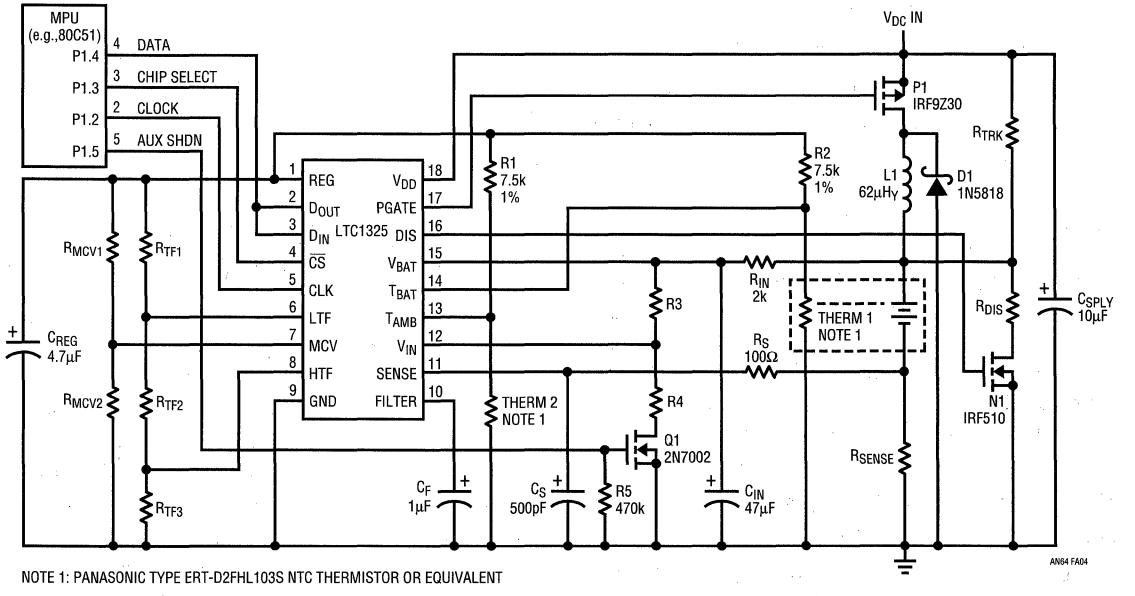
lower than 25°C. The battery temperature at which actual capacity is 85% of standard capacity is approximately 0°C. Similarly, adjustment to the indicated capacity may be desired if the continuous discharge current will be at a rate significantly greater than 0.1**C**. It may be desirable to take these effects into account if gas gauging is to be done over extended temperature ranges. If correction parameters for the gas gauging function of the LTC1325 will be employed, it is recommended that the manufacturer of the specific battery in question be consulted.

Under some conditions, it may be desirable to use a lower charging rate than 0.1**C** (for instance, to reduce charger power requirements). This is quite feasible with SLA batteries due to their low self-discharge rates. SLA batteries have excellent charge acceptance characteristics at lower charge rates. Ultimately, the limiting issue is usually the maximum practical time allowable for a recharge.

During charging, the battery may get warm and/or vent. It is prudent engineering to allow for these contingencies in the mechanical design stage of the equipment in which the battery will reside. The manufacturer of the SLA battery to be used should be consulted for specific guidance.

Sealed Lead-Acid Fast-Charge

In many cases, 24 hours or more will constitute an excessive recharge time. Portable instrumentation is an excellent example—even if the battery pack in an instrument can be "swapped out" for external recharge, it is often needed again before the day is out, fully charged and



NOTE 1: PANASONIC TYPE ERT-D2FHL103S NTC THERMISTOR OR EQUIVALENT

Figure A4. LTC1325 Constant Potential Battery Management System

ready for use. In this case the sophisticated fast-charge techniques which the LTC1325 makes practical are the way to go. A fast-charge regimen implies:

- Significant recharge within one hour; 100% recharge within three hours.
- Suitable means to determine charge termination point.
- A backup charge termination method to ensure best battery life.
- Highly efficient use of available charging energy.
- Increased product value through better battery utilization and greater customer satisfaction.

An SLA fast-charge is very similar to an SLA standard-charge. It is recommended that the section on standard-charging of Sealed Lead-Acid batteries be read before reading this section. There are only three significant differences between the two sections:

a) The charging voltage is increased (to increase the charging current).

b) Temperature compensation is definitely required at a rate of $\approx -5mV/°C$, preferably from a sensor mounted near or on the battery case.

c) Fast-charge termination is required.

- Charging Current: Vendor-dependent. The vendor used as a reference suggests 1.5**C**.
- Charging Voltage: 2.45V/cell to 2.50V/cell, plus charger overhead.
- Charging Temperature Range: 0°C to 30°C.
- Charge Termination Method: Current Cutoff.
- Charging Time: Three hours; 60% of charge is typically returned within the first hour.
- Secondary Charge Termination Methods: Timer.
- Special issues which may require further consideration are: wide temperature range charging, wide temperature range discharging, and accurate gas gauging under varying conditions of use.

The primary termination method, "Current Cutoff" (CCO), looks at the absolute value of the average charging current flowing into the battery. When that current drops below 0.01**C** the battery is charged and needs only a trickle current of about 0.002**C**. The backup method should be a 180-minute time-out, according to the recommendations of the vendor suggesting 1.5**C** as a high-rate current.

During fast-charge the battery will get warm and some venting may occur. It is prudent engineering to allow for these contingencies in the mechanical design stage of the equipment in which the battery will reside. The manufacturer of the SLA battery to be used should be consulted for specific guidance.

In all other regards, the techniques for the fast-charging of SLA cells and batteries are the same as those used for standard-charging these devices. A simple circuit, coupled with a straightforward software servo loop, provides a high performance SLA battery charger and gas gauge as well as significant built-in fault detection and protection mechanisms.

Using Lithium-Ion Batteries

Of the four battery types discussed in this Appendix, Lithium-Ion (Li-Ion) is the newest. Li-Ion cells offer excellent service life, are considered environmentally sound, are easily manufactured in true prismatic (rectangular) format, and most importantly, they have the highest energy density, both in terms of Watt-Hours/kg and Watt-Hours/Liter, of any of the cells discussed.

By merely telling the associated microcontroller whether a NiMH or a Li-Ion battery is present in the system, the LTC1325 using the same hardware can accommodate either type of cell technology.

Li-Ion batteries are charged using a constant voltage source with a deliberately imposed current limit (essentially a current-limited voltage regulator), or a charger which will, in terms of the electrochemical effects seen by the battery, act as if it were such a source. The charging regimen which this gives rise to is known as "Constant Voltage," or more commonly, "Constant Potential." For the purpose of this document, the term "Constant Potential" (CP) will be used.

A quick run-down of the pros and cons of Lithium-Ion batteries:

The "pros":

- Superb energy densities, both by Watt-Hours/Liter and Watt-Hours/kg, relative to competing technologies.

- High average cell voltage during discharge (3.6V).
- Excellent cycle life characteristics.
- Very low self-discharge rates (≈ 0.3%/day at 25°C).
- Environmentally sound (not a heavy-metal technology).
- Li-Ion cells are available in prismatic (rectangular) form factors.

The "cons":

- Susceptible to irreversible damage if taken into deep discharge.
- Susceptible to loss of capacity or catastrophic failure if overcharged.
- Efficient use of cell capacity requires extremely tight control of charging voltage.

Lithium-Ion Fast-Charging

An Li-Ion fast-charge is conceptually quite simple:

- Charging Current: 1**C**.
- Charging Voltage: 4.20V ±0.05V (some cells require slightly different voltages)
- Charging Temperature Range: 0°C to 40°C.
- Charging Time: 2.5 Hours to 5 Hours.
- Charge Termination Method: A timer is typical (consult cell manufacturer).
- Secondary Charge Termination Methods: None required.
- Special issues which require further consideration are: wide temperature range charging, wide temperature range discharging, and accurate gas gauging under varying conditions of use.

A significantly discharged cell undergoing CP charging will initially attempt to draw very high currents, as Li-Ion cells are relatively low impedance devices. The function of the current-limiting in the CP regimen is to keep the peak current flowing into the cell within the cell's (and the charger's) ratings. Following the current-limited phase of the charging profile, the CP charging technique in combination with the characteristics of the Li-Ion cell cause the cell under charge to in essence regulate its own charging current. If the cell vendor's recommendation as to charging voltage (usually 4.20V ±50mV at 23°C) are followed, the cell's charging current will naturally taper off with time. Figure A3 illustrates such charging behavior. This straightforward charging regimen is, to our best knowledge, all that is required to charge one cell. Multicell Li-Ion battery packs (e.g., two or more cells in series) incorporate a custom circuit for monitoring the state of charge of each individual cell within the battery. This circuit also provides extensive overcharge and other major fault protection.

The LTC1325 can readily charge either a single cell, or a manufacturer's finished battery pack. The LTC1325 is, at first glance, a constant-current part. Such a view of its capabilities, however, is too limited. Its power control section is more completely described as a constant-average-current PWM, with the capability for "software" feedback. Given a suitable output filter (probably only the output inductor and the battery itself), the current from the PWM section can be turned into a suitably constant voltage at the battery's terminals and this voltage used to charge Li-Ion cells or batteries.

The software feedback loop mentioned previously allows the controlling processor to handle all aspects of charging, rather than demanding that important variables be hardwired. The necessary CP servo loop is created as follows:

- Establish a regular repetition interval for the voltage servo loop. 10ms to 20ms gives good results for sealed lead-acid and Li-Ion cells and batteries.
- Set V_{DAC} to 150mV for best resolution. R_{SENSE} is then chosen as 150mV/(0.9 • I_{MAX}), where I_{MAX} is the maximum current to be allowed through the battery.
- Perform each of the following tasks once each servo loop interval:
  a) Enter Idle mode of operation.
  b) Each V_{CELL}.
  c) Adjust the value entered into a timer register (or a software timer) up or down according to actual V_{CELL} vs target V_{CELL}. If V_{CELL} is too high the timer value is increased. If V_{CELL} is too low the timer value is decreased.

d) Assume that the maximum t_{ON} of the charger will be 90% of each servo loop interval.

e) Enter Charge mode of operation, for a period of between 90% and 20% of the servo loop interval [as determined by (d)]. In essence, the timer's period is being subtracted from the charging time available during each servo loop interval, to perform a duty cycle modulation via the processor.

f) If t_{ON} < 2ms, switch V_{DAC} to the next lower value.

g) Repeat (a) through (f) until the current into the battery drops below 0.002**C**, or until three hours of charging have elapsed.

h) Terminate the software loop with the MOSFET P1 (Figure A4) in the "off" state. No trick-charging resistor is used.

Lithium-Ion System Issues

Lithium-Ion cells and batteries require tight control over the voltages to which they are exposed. This makes it virtually mandatory that precision external resistive divider be used to scale the battery voltage and present it to the auxiliary ADC input V_{IN} . The highest input voltage possible consistent with not overloading the LTC1325's ADC should be used; 3.000V full-scale is a good choice. This gives the best ADC resolution and helps preserve the accuracy of the part when measuring battery voltage. If the LTC1325's internal battery divider is used, account must be taken of its tolerance (±2%), as well as the reference tolerance (±0.8%) and the ADC tolerances (4 bits/1024 bits = 0.4%). The system tolerance then is ±3.2%. Adding in a ±1% resistor division ratio would bring this tolerance to ±4.2%.

Using a ±0.1% external divider feeding into the V_{IN} pin, the resulting tolerance is the ±0.8% of the reference, plus the ±0.5% represented by the ADC and the divider resistors. The design center charging voltage is 4.19V. Overcharging (an effective voltage at the battery's terminals of greater than 4.250V absolute maximum) is strongly discouraged by Li-Ion cell manufacturers. Any overcharging will shorten the cell's life and may result in catastrophic failure. With the undivided battery voltage connected to the LTC1325's V_{BAT} input, the on-chip battery divider can be used to check for V_{CELL} reaching the FEDV (Fault: End of Discharge Voltage) point.

There is also a need to ensure that the cell voltage rarely, if ever, dips below 2.5V to 2.7V (contact the specific cell manufacturer for details), and that it *never* goes below 1.0V. This is a spot where the fail-safe capabilities of the LTC1325 can serve the Li-Ion user well.

APPENDIX B

Flow Charts

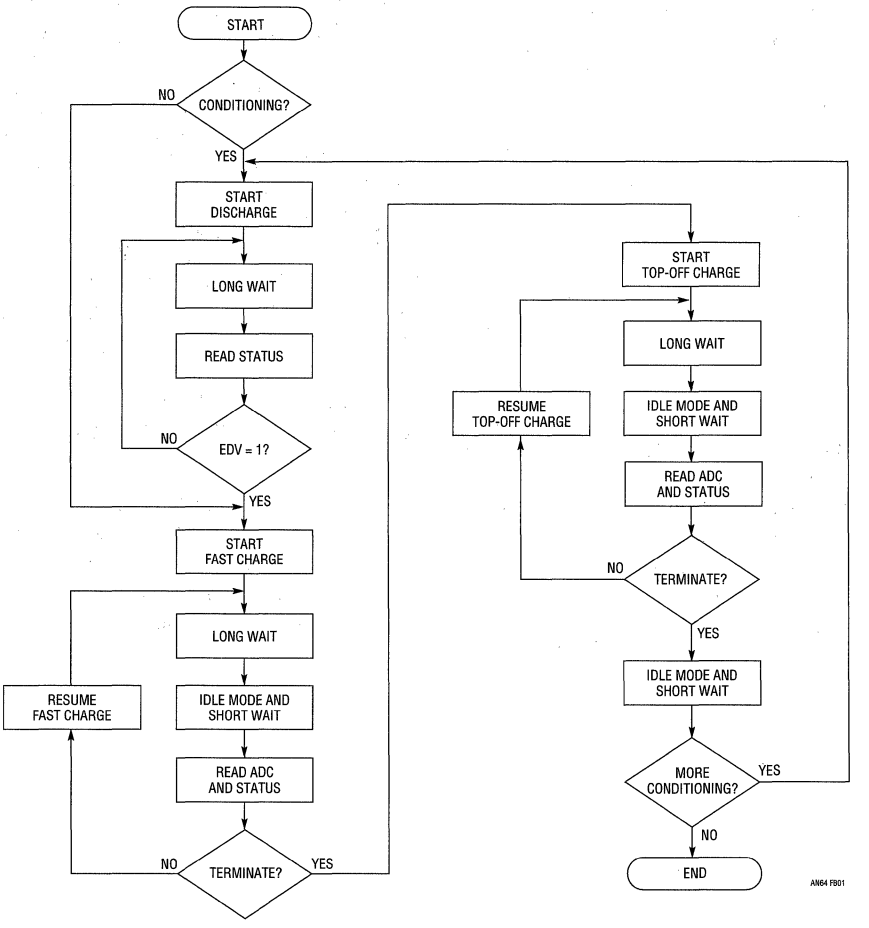


Figure B1. Simplified Battery Management Flow Chart

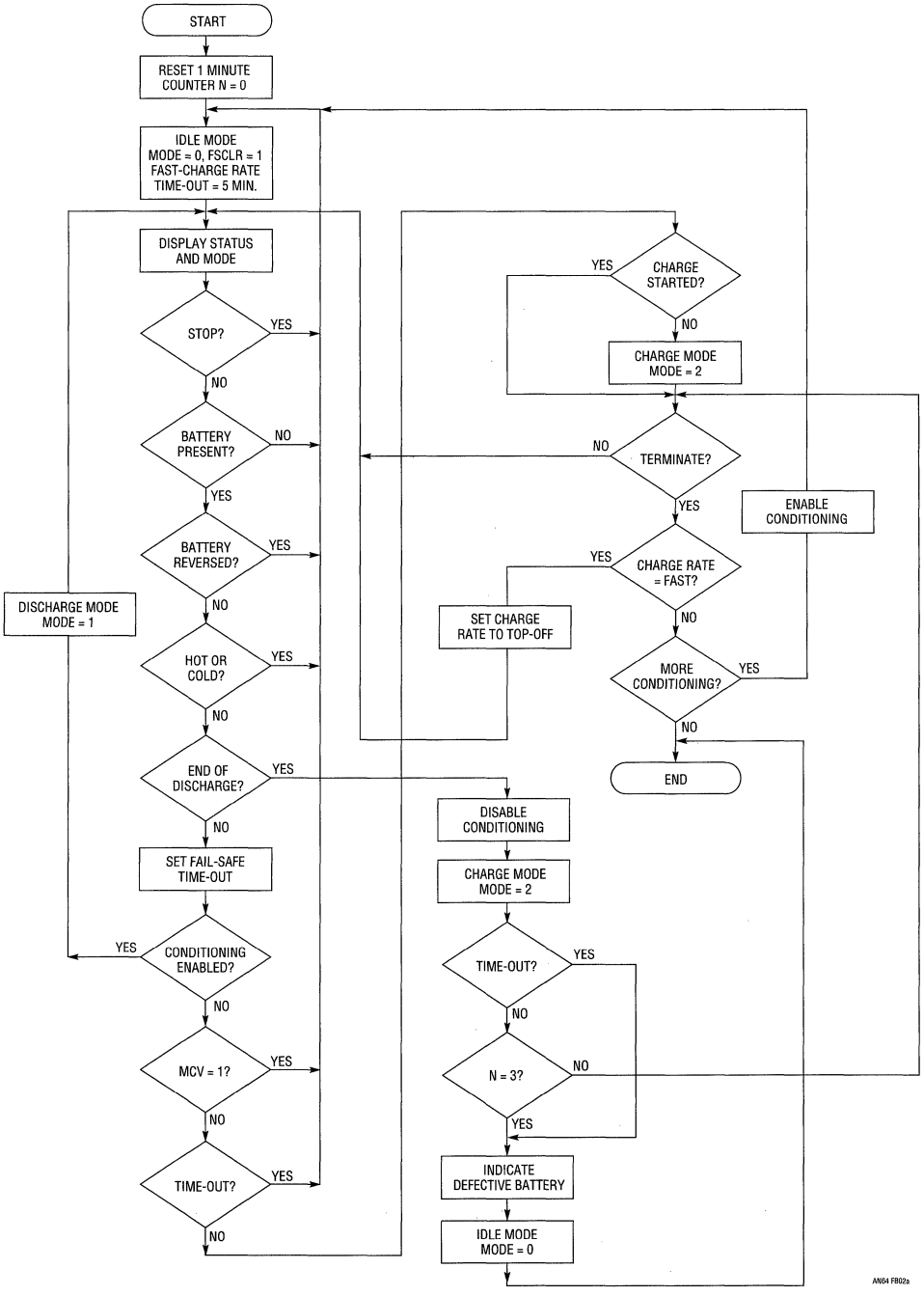


Figure B2a. Comprehensive Battery Management Flow Chart

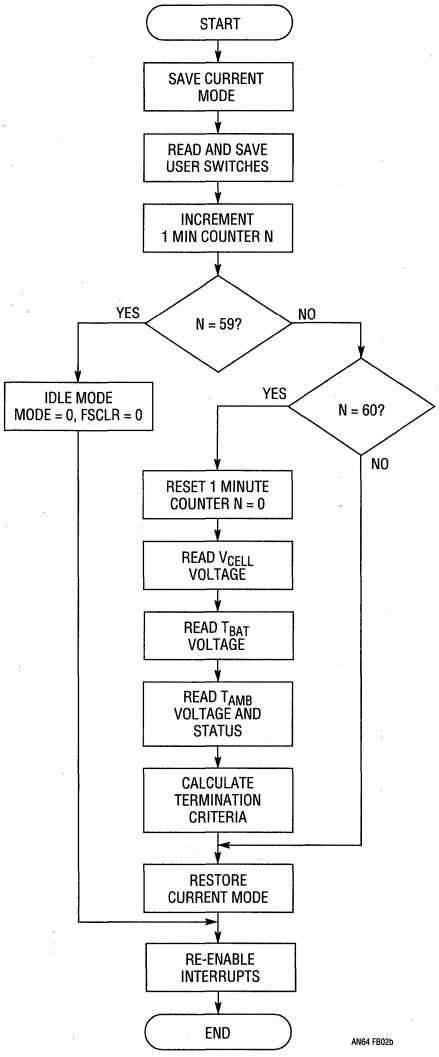


Figure B2b. Timer Interrupt Service Routine for Comprehensive Battery Management

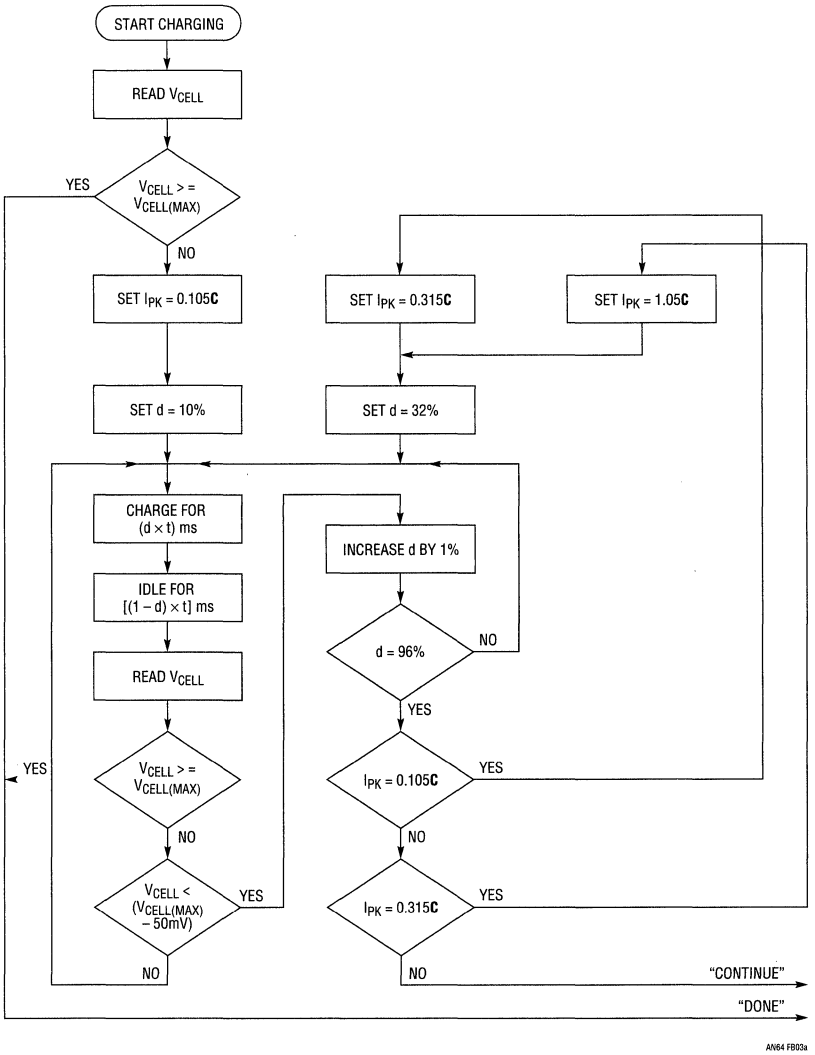


Figure B3a. Constant-Potential Charging Algorithm for Lead-Acid and Li-Ion (1 of 2)

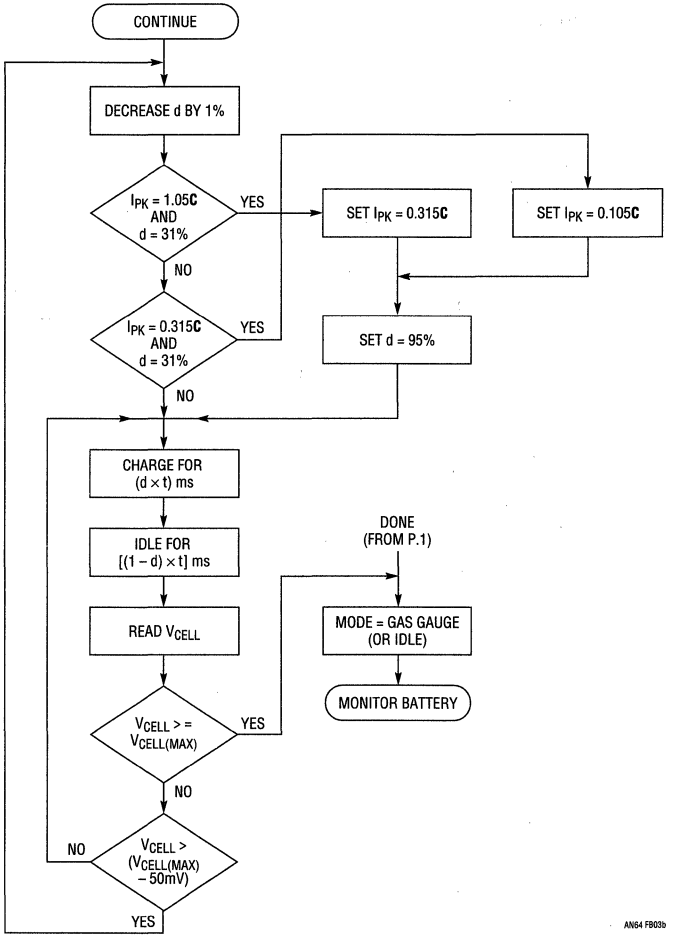


Figure B3b. Constant-Potential Charging Algorithm for Lead-Acid and Li-Ion (2 of 2)

APPENDIX C

A Brief Glossary

As with any other field, rechargeable battery technique has its own terminology. Here are a few definitions which are useful to know. Also included are terms used to describe the LTC1325, its operation and the application circuits.

Actual Capacity: The capacity for electrical energy storage of a cell which is in good condition, under test circumstances which differ from those established for the measurement of the cell's standard capacity.

Battery: A grouping of cells, to increase the voltage (series), the Ampere-Hour capability (parallel), or both (series-parallel). In this document, "battery" may be used interchangeably with "cell." Where the two differ, the battery is assumed to be a series assembly of cells unless otherwise specified.

Battery Divider: A programmable voltage divider (divide by 1,2,..,16) connected between the V_{BAT} and Sense pins of the LTC1325. For battery types with per cell voltages of greater than 2.9V, it is necessary to program the divider to keep the divider output within the 2.9V minimum range of the LTC1325 10-bit ADC (Analog-to-Digital Converter).

BATP: Battery Present Status Bit. One of the status bits that the LTC1325 provides. This bit is set when the V_{BAT} pin is pulled below V_{DD} by at least 1.8V.

BATR: Battery Reversed or Battery Shorted Status Bit. One of the status bits that the LTC1325 provides. When the cell voltage, V_{CELL} is less than 100mV, the BATR bit is set and discharging or charging is terminated.

C: Current expressed in terms of the **C** rate of a battery, e.g., 1.2**C**, 0.1**C**, 2**C**, etc.

C Rate: A normalization concept widely used in the battery community. A **C** rate of unity is equal to the capacity of a cell in ampere-hours, divided by one hour. Hence a 2.4 Ampere-Hour cell has a **C** rate of (2.4 Ampere-Hours)/ (1 Hour) = 2.4 Amperes. By extension, the 0.1**C** rate for the same cell equates to (0.1) (2.4 Ampere-Hours)/ (1 Hour) = 0.24 Amperes, and the 2**C** rate is 4.8 Amperes. The value of this term lies in the fact that, for a given cell type, the behavior of cells of varying actual capacity will nonetheless be very similar at the same **C** rates.

Cell: A single electrochemical energy storage element. Cells come in various technologies (e.g., Nickel-Cadmium and Nickel-Metal Hydride) and in various Ampere-Hour ratings.

Cell Reversal: A situation involving the lowest capacity cell in a battery stack, which can manifest itself as the battery stack approaches a deeply discharged state. If a given cell reaches the condition of zero charge before the current draw from the battery stack as a whole is terminated, then current from other cells in the battery stack will force a net reverse charge onto the cell in question. This reverse charge, if allowed to continue for a significant length of time, can cause irreversible deterioration of the cell undergoing reversal.

Charge Acceptance: The ability of a battery to transform charging energy (in the form of electrical current) into available energy (in the form of useful chemical reactions). Essentially, a measure of the efficiency of the battery as a storage device for electrical energy. This efficiency varies with battery temperature, state of charge, charging rate, age and electrochemistry.

Charge Mode: The LTC1325 can be programmed into this functional mode to charge batteries. Charging will not commence or is terminated if the battery is absent (see BATP) or the battery temperature is outside permissible limits (see LTF and HTF) or the battery is reversed or shorted (see BATR) or if a time-out condition exists.

Charge Termination Method: The means employed by a given charging algorithm to determine the appropriate point in the charging cycle at which to terminate (a phase of) that charging cycle.

Current Cutoff (CCO): A charge termination technique which monitors the current level flowing into a cell or battery, and indicates to the charging circuit that the charging current should be reduced or cut off when the level falls below a given limit.

Cycle Life: The number of charge/discharge cycles which a battery can sustain before its capacity declines to a specified percentage of its standard capacity, or its initial actual capacity in a given application. The permissible percentage of loss of battery capacity is not a fixed term

within the battery industry, as most applications have their own unique criteria.

dT_{BAT}/dt: See Delta Temperature/Delta Time.

Delta Temperature/Delta Time ($\Delta T/\Delta t$ or dT_{BAT}/dt): A Charge Termination Method (or Secondary Charge Termination Method) used to terminate the high-rate portion of a NiCd or NiMH fast-charge regimen. This technique makes use of the fact that the case temperature of a cell undergoing high-rate charge will experience a relatively rapid temperature rise as it goes into high-rate overcharge. When this rate of rise reaches a predetermined value (typically about 1°C/minute), almost all of the dischargeable capacity has been returned to the cell, and the high-rate charge should be terminated.

d^2V_{BAT}/dt^2: See Inflection Point Cutoff.

Discharge Mode: The LTC1325 can be programmed into this functional mode to discharge batteries through an external limiting resistor R_{DIS} and N-channel MOSFET. The gate of the N-channel MOSFET is driven by the DIS pin.

Discharge Profile: The voltage-vs-remaining charge characteristic of a cell or battery; the degree of voltage change shown by the battery as its goes from being fully charged to being fully discharged.

Duty Cycle: The LTC1325 can be programmed to modulate the "on" time of the charge loop with duty cycles of 1/16, 1/8, 1/4, 1/2 and 1. The period of this modulation is 42s.

EDV: End of Discharge Voltage. Refers either to the EDV status bit or to the internal end of discharge voltage of 0.9V. Discharge is automatically terminated by the LTC1325 when the cell voltage (V_{CELL}) falls below 0.9V.

Energy Density (W-H/kg): A "figure-of-merit" term for comparing differing battery technologies in terms of energy storage capacity vs mass (Watt-Hours/kg).

Energy Density (W-H/L): A "figure-of-merit" term for comparing differing battery technologies in terms of energy storage capacity vs. volume (Watt-Hours/Liter).

Fail-Safes: Various protective measures (voltage, temperature and time limits) built into the LTC1325 to protect the battery against potentially damaging voltage and temperature conditions when in charge or discharge modes. Also referred to as "Fault Protection."

Fast-Charge: Generally, any of several charging regimens which is capable of completely recharging a battery within three hours or less. More importantly, such regimens can typically return at least 90% of the battery's useable capacity within one hour or less. Only batteries specifically designed and rated for the requirements imposed by fast-charge applications should be employed in such applications.

Gas Gauging: Computation of the amount of energy remaining in a battery. This is typically done by coulometric means, that is, the net current with which the battery is charged is metered and integrated. Any currents drawn out of the battery are then metered and subtracted from the integrated total. More sophisticated versions of this same concept use look-up tables and/or algorithmic means to allow for the effects of such variables as charging rate, discharge rate, and temperature during charge and discharge phases of battery use. These corrections compensate for measurement discrepancies which the battery's variable charge acceptance and actual capacity might otherwise cause.

Gas Gauge: To perform the gas gauging function. Also, a device or display used somewhere within the system employing the gas gauging function, to indicate the status of the battery to the user and/or to system software routines.

Gas Gauge Mode: The LTC1325 can be programmed into this functional mode to measure load currents sensed by R_{SENSE}. The voltage across R_{SENSE} is multipled by –4, RC filtered before being converted by the ADC. The RC filter consists of an internal 1k resistor and an external non-polarised capacitor C_{FILTER} connected at the Filter pin of the LTC1325.

Gassing: The generation of gas(ses) within a cell as it approaches and enters the overcharge regime. Gassing is an anticipated part of the cell's operation, and is not harmful unless the rate of gassing exceeds the rate at which the cell can recombine the gas(ses) generated. Under such circumstances, the excess gas(ses) will escape to the outside of the cell through a pressure relief valve, causing the permanent loss to the cell of some of the electrolyte from which the gas(ses) were evolved.

High-Rate Charge: The first stage of the two or more stage fast-charge regimen, during which current is flowing

through the battery under charge at a greater rate than the battery can allow on a continuous basis. This portion of the fast-charge requires specific external termination.

HTF: High Temperature Fault. Refers either to the HTF status bit or to the highest battery temperature at which charging or discharging is permitted by the LTC1325. Charging is automatically terminated by the LTC1325 when the voltage at the T_{BAT} pin is less than the voltage at the HTF pin.

I_{CHG}: Average Charging Current. This should be within recommended limits for the battery.

I_{DIS}: Average Discharge Current. This should be within recommended limits for the battery.

Idle Mode: The LTC1325 can be programmed into this mode when none of the other modes are needed or to make ADC measurements without the presence of switching noise.

Inflection Point Cutoff (d^2V_{BAT}/dt^2): A charge termination technique used with Nickel-Cadmium and Nickel Metal Hydride batteries. During charge at a constant rate (e.g., the high-current portion of a fast-charge regimen), the terminal voltage of such batteries increases until the battery is slightly into overcharge. The rate of this increase, however, is not linear with respect to time. Shortly before the battery reaches full charge, the rate of change of terminal voltage becomes constant; at the time the battery becomes fully charged this rate of change becomes either zero or negative. The second derivative of the battery's voltage with respect to time can therefore be used to indicate that point at which the battery is near full charge, by looking for either a zero, or more commonly a negative, value of d^2V_{BAT}/dt.

Incremental Temperature Cutoff (ΔTCO): A Charge Termination Method (or Secondary Charge Termination Method) frequently used to terminate the high-rate portion of a fast-charge regimen. TCO makes use of the fact that the case of a fully charged cell will experience a relatively rapid temperature rise as it goes into high-rate overcharge (typically 0.5°C/minute to 1°C/minute).

LTF: Low Temperature Fault. Refers either to the LTF status bit or to the lowest battery temperature at which charging or discharging is permitted by the LTC1325. Charging is automatically terminated when the voltage at the T_{BAT} pin of the LTC1325 is greater than the voltage at the LTF pin.

MCV: Maximum Cell Voltage. Refers either to the MCV status bit or the highest permissible V_{CELL}. Charging is automatically terminated by the LTC1325 when the cell voltage (V_{CELL}) is greater than the voltage at the MCV pin.

Negative Δ Voltage ($-\Delta V$): A Charge Termination Method (or Secondary Charge Termination Method) frequently used to terminate the high rate portion of a fast-charge regimen. This method makes use of the fact that the voltage across a Nickel-Cadmium cell, and to a lesser degree, a Nickel-Metal Hydride cell, will experience a maximum voltage and a subsequent voltage decrease (the "$-\Delta V$") once it goes into high-rate overcharge (typically between –20mV and –50mV for a Nickel-Cadmium cell). This technique is most commonly employed with NiCd batteries.

NiCd: Nickel-Cadmium

NiMH: Nickel-Metal Hydride

NTC: Negative Temperature Coefficient. Also used in this Application Note to refer to thermistors with negative temperature coefficients.

Overcharge: The situation which arises when a cell has been returned to its state of full charge, but the charging current to the cell is not removed. Of necessity, cells are designed to handle a certain amount of overcharge, hence, this is not necessarily either a harmful or an undesirable condition. During overcharge, the excess electrical energy applied to the cell which does not go towards preventing self-discharge is dissipated as heat, through the formation and recombination of gas(ses) within the cell.

PTC: Positive Temperature Coefficient. Also used in this Application Note to refer to thermistors with positive temperature coefficients.

Quick-Charge: A charging regimen for Nickel-Cadmium and Nickel-Metal Hydride batteries which can return 100% of usable capacity to the battery in five hours. Batteries to be charged in this manner must be rated for such charging. The charging current for this regimen is usually stipulated by the manufacturer to be 0.33**C**.

R_{DIS}: External resistor in LTC1325-based circuits to limit battery discharge currents to within recommended limits for the battery.

$R_{DS(ON)}$: Drain to source on-resistance of a MOSFET.

Required Charging Voltage: The minimum voltage which should be available with which to charge a given type of battery, in a given charge regimen. Essentially, the compliance voltage capability of the charger, as dictated by the voltage which the battery can be expected to achieve during the charging cycle.

R_{SENSE}: Sense Resistor. An external resistor in LTC1325-based circuits which is connected between the Sense pin and ground. This resistor is used to sense battery current in charge and gas gauge modes.

R_{TRK}: Trickle Resistor. An external resistor in LTC1325-based circuits. This resistor has three purposes: 1) it keeps the battery in a fully charged condition after charging is completed, 2) it trickle-charges a deeply discharged battery to raise its cell voltage above 100mV so that charging may commence, and 3) it pulls the V_{BAT} pin high whenever the battery is removed. This tells the LTC1325 that the battery has been removed.

Secondary Charge Termination Methods: Certain charging algorithms, especially fast-charge algorithms, have the potential to damage the batteries which they are charging if charge termination does not occur properly. For this reason, such algorithms generally employ more than one termination method. Secondary Charge Termination Methods are those which provide redundancy for the chosen Charge Termination Method.

Self-Discharge: The characteristic of electrochemical storage cells to bring themselves to the discharged state, even when their terminals are open-circuited.

Self-Discharge Rate: The rate at which an electrochemical storage cell brings itself towards the discharged state, with its terminals open-circuited. This rate is, for example, approximately 0.5%/day to 1%/day for Nickel-Cadmium and Nickel-Metal Hydride cells at room temperature.

Shutdown Mode: The LTC1325 is programmed into this functional mode to reduce current drain on V_{DD} supply to 30mA typical.

Standard Capacity: The capacity for electrical energy storage of a cell which is in good condition. The necessary tests to ascertain this capacity is carried out under the cell manufacturer's specified standard conditions, which are generally those at which the cell can be expected to deliver its best performance.

Standard-Charge: An "overnight" charge method. This regimen typically involves charging at the 0.1**C** rate, requiring 14 to 16 hours to perform a complete charge on a battery.

T_{AMB}: Refers to ambient temperature or to the T_{AMB} pin of the LTC1325. This pin is connected to an undedicated channel of the 10-bit ADC and may be used to monitor ambient temperature.

T_{BAT}: Refers to either battery temperature or the voltage at the T_{BAT} pin of the LTC1325.

Temperature Cutoff (TCO): A technique for determining at what point to terminate the charging of a cell or battery. The absolute temperature of the cell (or one cell of a battery) is monitored by a temperature-sensitive element which, upon detecting a preset temperature, will either reduce or terminate the charging current to the cell or battery. TCO is frequently used as a backup termination method in fast-charge systems.

Time-Out: A time limit on charge and discharge time. May be one of eight values: 5, 10, 20, 40, 80, 160, 320 minutes or no time-out.

Top-Off Charge: The second portion of the three-stage fast-charge regimen, during which the rate of current flow through the battery under charge is cut back significantly from the high-rate value. This portion of the charge serves to put the battery barely into overcharge.

Trickle-Charge: The third stage of the three-stage fast-charge regimen, during which the rate of current flow through the battery under charge is kept at a sufficient level to prevent the battery from self-discharging, but which contributes little to the charging of the battery per se. The current level required for trickle-charge may or may not be lower than that used for the topoff-charge.

V_{CELL}: Cell Voltage. The battery voltage divided by the programmed setting of the LTC1325 battery divider.

V_{DAC}: A programmable reference voltage in the LTC1325 which determines the average voltage at the Sense pin when the LTC1325 is programmed into charge mode. V_{DAC} may be set to one of four values.

V_{DC}: Positive charging supply in the LTC1325 circuits described in this Application Note.

V_{DD}: Positive supply pin of the LTC1325. Same as V_{DC} for voltages between 4.5V to 16V.

V_{EC}: End of Charge Voltage. The maximum voltage across each cell of the battery when fully charged. The voltage at the MCV pin should be set above V_{EC} to prevent false fail-safes from occurring.

Venting: The loss of gas(ses) from the inside of a nominally "sealed" cell to the ambient, through the cell's pressure relief valve. Venting is indicative of a harmful level of overcharge, and will cause eventual irreparable damage to the cell.

V_{BAT}: Battery Voltage

V_{IN}: Refers to the V_{IN} pin of the LTC1325 or its voltage. This pin is connected to an undedicated channel of the 10-bit ADC and may be used to monitor any desired voltage within the 3V range of the ADC.

Zero Voltage (Zero V): A Charge Termination Method (or Secondary Charge Termination Method) frequently used to terminate the high-rate portion of a fast-charge regimen. This method makes use of the fact that the voltage across a Nickel-Metal Hydride or Nickel-Cadmium cell will experience a voltage maximum, and subsequent voltage decrease or plateau once it goes into high-rate overcharge. The point at which voltage stops increasing during charging is the point of Zero V. This technique is most commonly employed with NiMH batteries.

APPENDIX D

External Component Sources List

Batteries

Duracell USA (HQ)
Berkshire Corporate Park
Bethel, CT 06801
(203) 796-4000
(800) 243-9540
FAX: (203) 730-8958

Energizer Power Systems
Div. of Eveready Battery Co., Inc.
Highway 441 North
P.O. Box 147114
Gainesville, FL 32614-7114
(904) 462-3911
FAX: (904) 462-6210

GP Batteries (U.S.A.) Inc,
2772 Loker Avenue West
Carlsbad, CA 92008
(619) 438-2202
FAX: (619) 438-0694

GS Battery (USA) Inc.
17253 Chestnut Street
City of Industry, CA 91748
(818) 964-8348
FAX: (818) 810-9438

Hawker Energy Products, Inc.
617 N. Ridgeview Drive
Warrensburg, MO 64093-9301
(816) 429-2165
FAX: (816) 429-2253

Panasonic Industrial Company
Headquarters:
P. O. Box 1511
Secaucus, NJ 07096
(201) 348-5272
FAX: (201) 392-4728

SAFT America, Inc.
Otay Commerce Center
2155 Paseo de las Americas, #31
San Diego, CA 92173
(619) 661-7992
FAX: (619) 661-5096

SANYO Energy (U.S.A.) Corporation
2001 Sanyo Avenue
San Diego, CA 92173
(619) 661-6620
FAX: (619) 661-6743

Tadiran Electronic Industries, Inc.
2 Seaview Boulevard
Port Washington, NY 11050
(800) 786-9887
(516) 621-4980
FAX: (516) 621-4517

Varta Batteries Inc. (USA)
300 Executive Boulevard
Elmsford, NY 10523-1202
(914) 592-2500
FAX: (914) 592-2667

Inductors

Coiltronics, Inc.
6000 Park of Commerce Boulevard
Boca Raton, FL 33487
(407) 241-7876
FAX: (407) 241-9339

Dale Electronics, Inc.
East Highway 50
P.O. Box 180
Yankton, SD 57078-0180
(605) 665-9301
FAX: (605) 665-1627

Hurricane Electronics Lab
P.O. Box 1280
331 North 2260 West
Hurricane, UT 84737
(801) 635-2003
FAX: (801) 635-2495

Sumida Electric (USA) Corp., Ltd.
5999 New Wilkie Road
Suite 110
Rolling Meadows, IL 60008
(847) 956-0666
FAX: (847) 956-0702

Thermistors

Alpha Thermistor and Assembly Inc.
7181 Construction Court
San Diego, CA 92121
(619) 549-4660
FAX: (619) 549-4791

Fenwal Electronics Inc.
450 Fortune Boulevard
Milford, MA 01757
(508) 478-6000
FAX: (508) 473-6035

Panasonic Industrial Company
Two Panasonic Way, 7H-3
Secaucus, NJ 07094
(201) 348-5232
FAX: (201) 392-4441

Phillips Components
Discrete Products Division
2001 W. Blue Heron Blvd.
P.O. Box 10330
Riviera Beach, FL 33404
(407) 881-3200

Thermometrics Inc.
808 U.S. Highway 1
Edison, NJ 08817
(908) 287-2870
FAX: (908) 287-8847

MOSFETs

International Rectifier
U.S. World Headquarters
233 Kansas Street
El Segundo, CA 90245
(310) 322-3331
FAX: (310) 322-3332

Motorola Semiconductor, Inc.
3102 North 56th Street
MS56-126
Phoenix, AZ 85018
(800) 521-6274

Siliconix Inc.
2201 Laurelwood Road
P.O. Box 54951
Santa Clara, CA 95056
(408) 988-8000
FAX: (408) 970-3950

Schottky Diodes

General Instrument
Power Semiconductor Division
10 Melville Park Road
Melville, NY 11747
(516) 847-3000

International Rectifier
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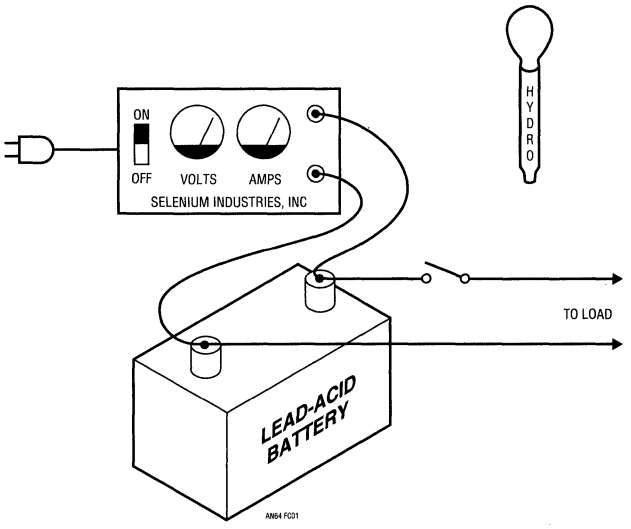
Polymer PTCs

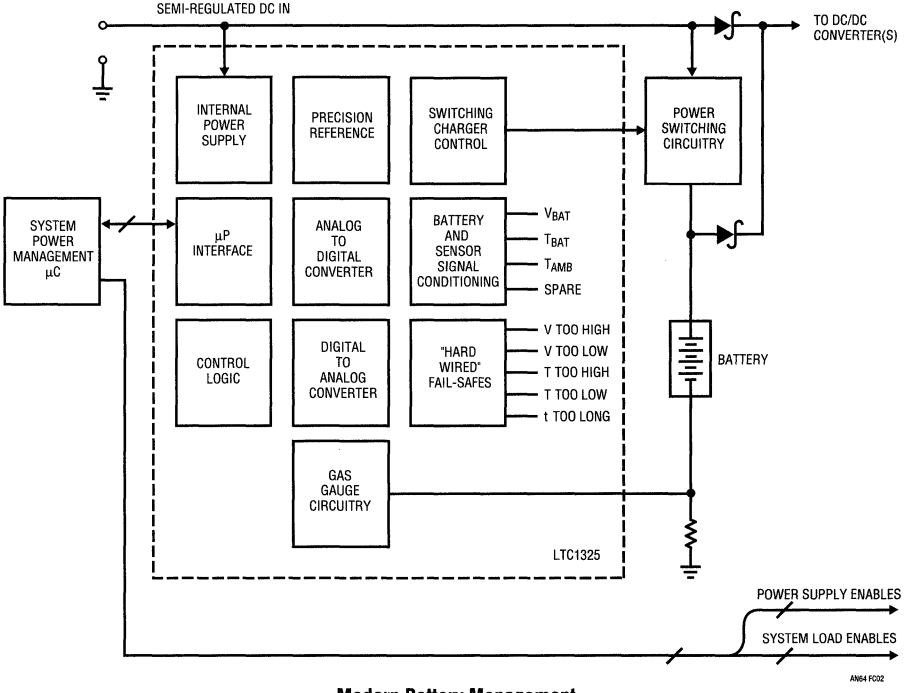
Raychem Corporation
PolySwitch Division
300 Constitution Drive
Menlo Park, CA 94025-1164
(800) 272-9243, x6900
FAX: (800) 227-4866

Bimetallic Thermostats

Phillips Technologies
Airpax Protector Group
550 Highland Avenue
Frederick, MD 21701
(301) 663-5141
FAX: (301) 698-0624



Early Battery Management



Modern Battery Management

Notes

LINEAR TECHNOLOGY

Application Note 65
November 1995

A Fourth Generation of LCD Backlight Technology

Component and Measurement Improvements Refine Performance

Jim Williams

PREFACE

Current generation portable computers and instruments utilize backlit LCDs (Liquid Crystal Displays). These displays have also appeared in applications ranging from medical equipment to automobiles, gas pumps and retail terminals. Cold Cathode Fluorescent Lamps (CCFLs) provide the highest available efficiency for backlighting the display. These lamps require high voltage AC to operate, mandating an efficient high voltage DC/AC converter. In addition to good efficiency, the converter should deliver the lamp drive in sine wave form. This is desirable to minimize RF emissions. Such emissions can cause interference with other devices, as well as degrading overall operating efficiency. The sine wave excitation also provides optimal current-to-light conversion in the lamp. The circuit should permit lamp control from zero to full brightness with no hysteresis or "pop-on," and must also regulate lamp intensity vs power supply variations.

The small size and battery-powered operation associated with LCD equipped apparatus mandate low component count and high efficiency for these circuits. Size constraints place severe limitations on circuit architecture and long battery life is usually a priority. Laptop and handheld portable computers offer an excellent example. The CCFL and its power supply are responsible for almost 50% of the battery drain. Additionally, these components, including PC board and all hardware, usually must fit within the LCD enclosure with a height restriction of 0.25 inches.

A practical, efficient LCD backlight design is a classic study of compromise in a transduced electronic system. Every aspect of the design is interrelated, and the physical embodiment is an integral part of the electrical circuit. The choice and location of the lamp, wires, display housing and other items have a major effect on electrical characteristics. The greatest care in every detail is required to achieve a practical high efficiency LCD backlight. Getting the lamp to light is just the beginning!

First generation backlights were crude, with poor performance in almost all areas. LTC (Linear Technology Corporation) has introduced feedback stabilization and optimized lamp driving configurations in three successive generations of technology. The effort has culminated in dedicated ICs for backlight driving.

This fourth publication reviews our recent work in components and measurement techniques applicable to LCD backlighting. Theoretical considerations are presented with practical suggestions, remedies and circuits. As always, we welcome reader comments, questions and requests for consultation.

CCFL backlight application circuits contained in this Application Note are covered by U.S. patent number 5408162 and other patents pending.

TABLE OF CONTENTS

INTRODUCTION

This scribing marks the fourth LTC publication in as many years concerning LCD illumination.[1] The extraordinary user response to previous efforts has resulted in a continuing LCD backlight development effort by our company. This level of interest, along with significant performance advances since the last publication, justifies further discussion of LCD backlighting.

Development of attractive solutions for LCD illumination has necessitated the longest sustained LTC application engineering effort to date. A single circuit in a 1991 publication (*Measurement and Control Circuit Collection*, LTC Application Note 45, June 1991) has resulted in four years of continuous investigation, summarized in three successive, dedicated publications.

The impetus for all this bustle has been an overwhelming and continuously ascending reader response. Practical, high performance LCD backlighting solutions are needed in a wide range of applications. The optical, transductive and electronic aspects combine (conspire?) to present an extraordinarily challenging problem. The LCD backlight problem's interdisciplinary nature, along with highly interactive effects, provides an exquisitely subtle engineering exercise. Backlights present the most complex set of interdependencies the author has ever encountered. Our academic interest in this challenge is, of course, well patinaed with capitalistic intent. Substantial comfort arrives with the certainty that the audience is similarly acculturated.

This publication includes pertinent information from previous efforts in addition to updated sections and a large body of new material. The partial repetition is a small penalty compared to the benefits of text flow, completeness and time efficient communication. Older material has been altered, abridged or augmented as appropriate, while simultaneously introducing new findings. Previous work has emphasized obtaining and verifying high efficiency. This characteristic is still quite desirable, but other backlight requirements have become evident. These include low voltage operation, improved system interface, minimization of display-induced losses, circuitry compaction and better measurement/optimization techniques. These advances have been enabled by development of new ICs and instrumentation.

Finally, this preamble must appreciate the text's arrangement and review by various LTC personnel and customers. They transmuted a psychotic uproar of a manuscript into this finessed presentation. Hopefully, readers will join the author in applause.

Note 1. Previous publications are annotated in References 1, 18 and 25.

PERSPECTIVES ON DISPLAY EFFICIENCY

The LCD displays currently available require two power sources, a backlight supply and a contrast supply. The display backlight is the single largest power consumer in a typical portable apparatus, accounting for almost 50% of battery drain with the display at maximum intensity. As such, every effort must be expended to maximize backlight efficiency.

Study of LCD energy management should consider the problem from an interdisciplinary viewpoint. The backlight presents a cascaded energy attenuator to the battery (Figure 1). Battery energy is lost in the electrical-to-electrical conversion to high voltage AC to drive the CCFL. This section of the energy attenuator is the most efficient; conversion efficiencies exceeding 90% are possible. The CCFL, although the most efficient electrical-to-light converter available today, has losses exceeding 80%. Additionally, the optical transmission efficiency of present displays is under 10% for monochrome with color types much lower.

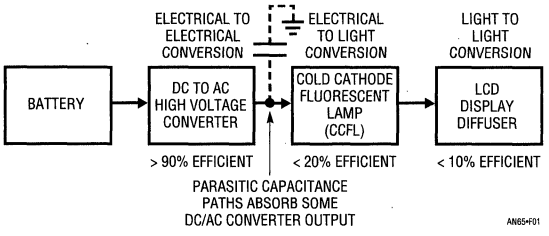


Figure 1. Backlit LCD Display Presents a Cascaded Energy Attenuator to the Battery. DC/AC Conversion is Significantly More Efficient Than Energy Conversions in Lamp and Display

The very high DC/AC conversion efficiency highlights some significant issues. Anything that improves energy transfer in the other "attenuator" areas will have greater impact than further electrical efficiency improvements. Additional improvements in electrical efficiency, while certainly desirable, are reaching the point of diminishing returns. Clearly, overall backlight efficiency gains must come from lamp and display improvements.

There is very little electrical workers can do to improve lamp and display efficiency besides call attention to the problems (see the following sections on lamps and displays).[2] Improvements are, however, possible in related areas. In particular, the *form* of drive applied to the lamp is quite critical. The waveshape supplied to the lamp influences its current-to-light conversion efficiency. Thus, dissimilar waveforms containing equivalent power can produce different amounts of lamp light output. This implies that a more *electrically* efficient inverter with a nonoptimal output waveshape could produce less light than a "less efficient" inverter with a more appropriate waveform. Experiment reveals this to be true. As such, distinction between electrical and photometric efficiency is necessary and requires attention.

Another practical area where improvement is possible is transmission of inverter drive to the lamp. The high frequency AC waveform is subject to losses due to parasitic capacitances in the wiring and display. Controlling the parasitic capacitances and the manner in which lamp drive is applied can yield significant efficiency improvement.

Practical methods addressing both aforementioned areas are contained in subsequent sections of this publication.

Cold Cathode Fluorescent Lamps (CCFLs)

Any discussion of CCFL power supplies must consider lamp characteristics. These lamps are complex transducers, with many variables affecting their ability to convert electrical current to light. Factors influencing conversion efficiency include the lamp's current, temperature, drive waveform characteristics, length, width, gas constituents and the proximity to nearby conductors.

These and other factors are interdependent, resulting in a complex overall response. Figures 2 through 8 show some typical characteristics. A review of these curves hints at the difficulty in predicting lamp behavior as operating conditions vary. The lamp's current, temperature and warm-up time are clearly critical to emission, although electrical efficiency may not necessarily correspond to the best optical efficiency point. Because of this, both electrical and photometric evaluation of a circuit is often required. It is possible, for example, to construct a CCFL circuit with 94% electrical efficiency which produces less

Note 2. "Call attention to the problems" constitutes a pleasant euphemism for complaining. This publication's section on displays presents such complaints in visual form along with suggested remedies.

light output than an approach with 80% electrical efficiency. (See Appendix L, "A Lot of Cut Off Ears and No Van Goghs—Some Not-So-Good Ideas.") Similarly, the performance of a very well matched lamp/circuit combination can be severely degraded by a lossy display enclosure or excessive high voltage wire lengths. Display enclosures with too much conducting material near the lamp have huge losses due to capacitive coupling. A poorly designed display enclosure can easily degrade efficiency by 20%. High voltage wire runs typically cause 1% loss per inch of wire.

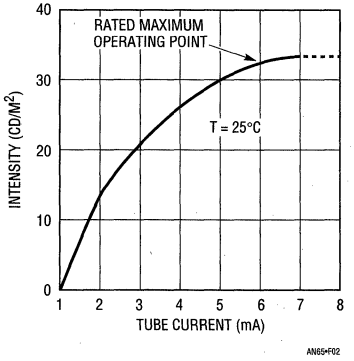


Figure 2. Emissivity for a Typical 5mA Lamp. Curve Flattens Badly Above 6mA

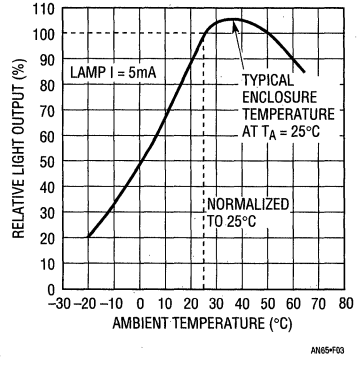


Figure 3. Ambient Temperature Effects on Emissivity of a Typical 5mA Lamp. Lamp and Enclosure Must Come to Thermal Steady State Before Measurements Are Made

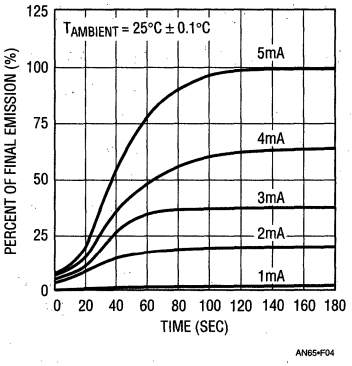


Figure 4. Emissivity vs On-Time for a Typical Lamp in Free Air. Lamp Must Arrive at Temperature Before Emission Stabilizes

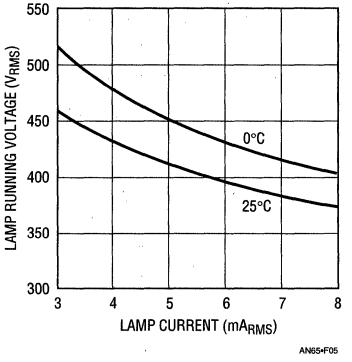


Figure 5. Lamp Current vs Voltage in the Operating Region. Note Large Temperature Coefficient

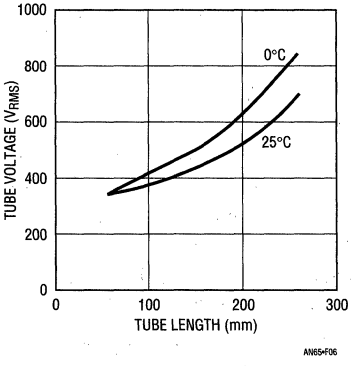


Figure 6. Running Voltage vs Lamp Length at Two Temperatures. Start-Up Voltages Are Usually 50% to 200% Higher Over Temperature

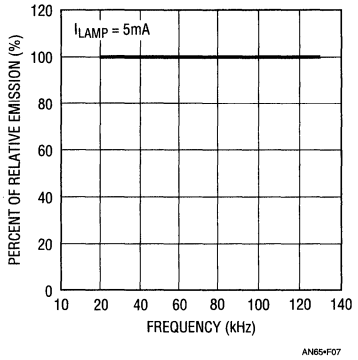


Figure 7. Lamp Emission vs Drive Frequency with Lamp in Free Space. No Change Is Measurable from 20kHz to 130kHz, Indicating Lamp Insensitivity to Frequency

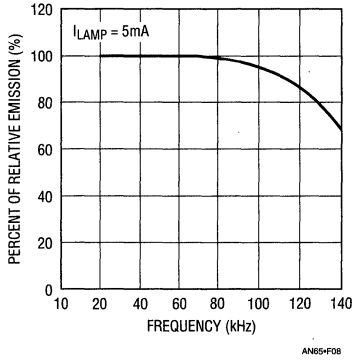


Figure 8. Figure 7's Lamp Shows Significant Emission vs Drive Frequency Degradation When Mounted in a Display. Cause Is Frequency-Dependent Loss Due to Display's Parasitic Capacitance Paths

The optimum drive frequency is determined by display and wiring losses, not lamp characteristics. Figure 7 shows lamp emissivity is essentially flat over a wide frequency range. Figure 8 shows results with the same lamp mounted in a typical display.

The apparent emissivity fall-off at high frequencies is caused by reduced lamp current due to parasitic capacitance-induced losses. As frequency increases, the display's parasitic capacitance diverts progressively more energy, lowering lamp current and emission. This effect is sometimes misinterpreted, leading to the mistaken conclusion that lamp emissivity degrades with increasing frequency.

CCFL Load Characteristics

These lamps are a difficult load to drive, particularly for a switching regulator. They have a "negative resistance" characteristic; the starting voltage is significantly higher than the operating voltage. Typically, the start voltage is about 1000V, although higher and lower voltage lamps are common. Operating voltage is usually 300V to 500V, although other lamps may require different potentials. The lamps will operate from DC, but migration effects within the lamp will quickly damage it. As such, the waveform must be AC. No DC content should be present.

Figure 9a shows an AC driven lamp's characteristics on a curve tracer. The negative resistance-induced "snap-back" is apparent. In Figure 9b another lamp, acting against the curve tracer's drive, produces oscillation. These tenden-

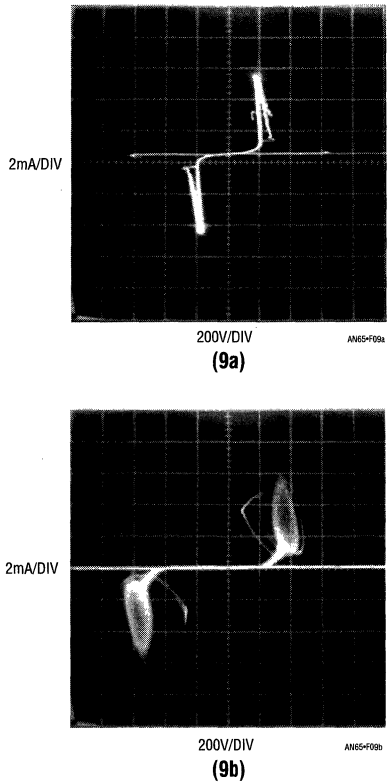


Figure 9. Negative Resistance Characteristic for Two CCFL Lamps. "Snap-Back" Is Readily Apparent, Causing Oscillation in 9b. These Characteristics Complicate Power Supply Design

cies, combined with the frequency compensation problems associated with switching regulators, can cause severe loop instabilities, particularly on start-up. Once the lamp is in its operating region it assumes a linear load characteristic, easing stability criteria. Lamp operating frequencies are typically 20kHz to 100kHz and a sine-like waveform is preferred. The sine drive's low harmonic content minimizes RF emissions, which could cause interference and efficiency degradation.[3] A further benefit to the continuous sine drive is its low crest factor and controlled rise times, which are easily handled by the CCFL. CCFL's RMS current-to-light output efficiency and lifetime degrades with fast rise, high crest factor drive waveforms.[4]

Display and Layout Losses

The physical layout of the lamp, its leads, the display housing and other high voltage components are integral parts of the circuit. Placing the lamp into a display introduces pronounced electrical loading effects which must be considered. Poor layout can easily degrade efficiency by 25% and higher layout-induced losses have been observed. Producing an optimal layout requires attention to how losses occur. Figure 10 begins our study by examining potential parasitic paths between the transformer's output and the lamp. Parasitic capacitance to AC ground from any point between the power supply output and the lamp creates a path for undesired current flow. Similarly, stray coupling from any point along the lamp's length to AC ground induces parasitic current flow. All parasitic current flow is wasted, causing the circuit to produce more energy to maintain desired current flow in the lamp. The high voltage path from the transformer to the display housing should be as short as possible to minimize losses. A good rule of thumb is to assume 1% efficiency loss per inch of high voltage lead. Any PC board traces, ground or power planes should be relieved by at least 1/4" in the high voltage area. This not only prevents losses but eliminates arcing paths.

Parasitic losses associated with lamp placement within the display housing require attention. High voltage wire length within the housing must be minimized, particularly for displays using metal construction. Ensure that the high voltage is applied to the shortest wire(s) in the display. This may require disassembling the display to verify wire length and layout. Another loss source is the reflective foil commonly used around lamps to direct light into the actual LCD. Some foil materials absorb considerably more field energy than others, creating loss. Finally, displays supplied in metal enclosures tend to be lossy. The metal absorbs significant energy and an AC path to ground is unavoidable. Direct grounding of metal enclosed displays further increases losses. Some display manufacturers have addressed this issue by relieving the metal in the lamp area with other materials. Losses introduced by the

Note 3. Many of the characteristics of CCFLs are shared by so-called "Hot" cathode fluorescent lamps. See Appendix A, "Hot" Cathode Fluorescent Lamps.

Note 4. See Appendix L, "A Lot of Cut Off Ears and No Van Goghs—Some Not-So-Great Ideas."

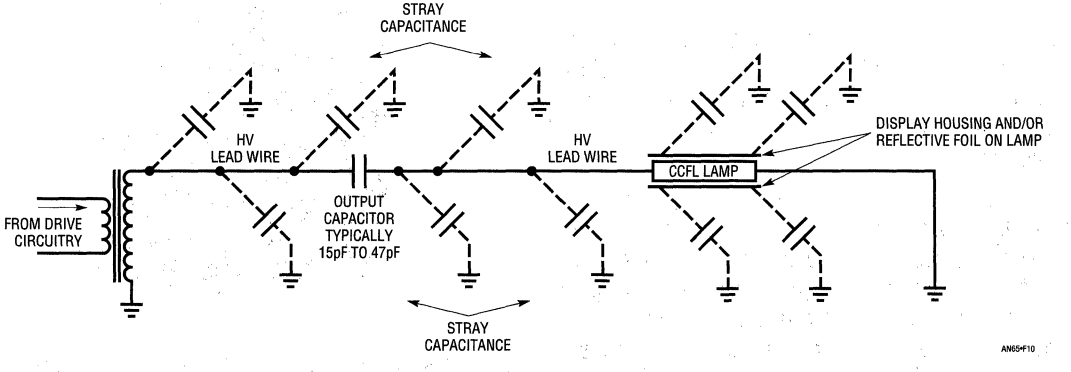


Figure 10. Loss Paths Due to Stray Capacitance in a Practical LCD Installation. Minimizing These Paths Is Essential for Good Efficiency

display are substantial and vary widely with different displays. These losses not only degrade overall efficiency, but complicate meaningful determination of the lamp current. Figure 11 shows effects of distributed parasitic capacitance loss paths on lamp current. The display housing and reflective foil-induced loss paths provide a continuous conduit for loss current flow. This results in a continuously varying value of "lamp current" along the lamp's length. In cases where one end of the lamp is at or near ground, the current fall-off is greatest in the lamp's high voltage regions. Although parasitic capacitance is usually uniformly distributed, its effect becomes far greater as voltage scales up.

These effects illustrate why designing around lamp specifications is such a frustrating exercise. Display vendors typically call out lamp operating parameters based on information received from the lamp manufacturer. Lamp vendors often determine operating characteristics in a completely different enclosure, or none at all. This set of uncertainties complicates design effort. The only viable solution is to determine lamp performance with the display of interest. This is the only practical way to maximize performance and ensure against overdriving the lamp, which wastes power and shortens lamp life.

In general, the display introduces parasitics which degrade performance. Latter portions of this text discuss some compensatory techniques, but the deleterious effects of display parasitics dominate practical backlight design.

There are some benefits to lossy displays. One advantage of display parasitics is that they effectively lower lamp breakdown voltage. The parasitic shunt capacitance along the tube's length forms a distributed electrode, effectively shortening the breakdown path, lowering the lamp's turn-on voltage. This accounts for the fact that many display mounted lamps start at lower voltages than the "naked" lamp breakdown voltage specification suggests. This effect aids low temperature start-up (see Figures 5 and 6).

A second potential advantage of distributed parasitic lamp capacitance is enhancement of low current operation. In some cases extended dimming range is possible because the parasitics provide a more evenly distributed field along the lamp's length. This tends to maintain illumination along the lamp's entire length at low operating currents, allowing low luminosity operation.

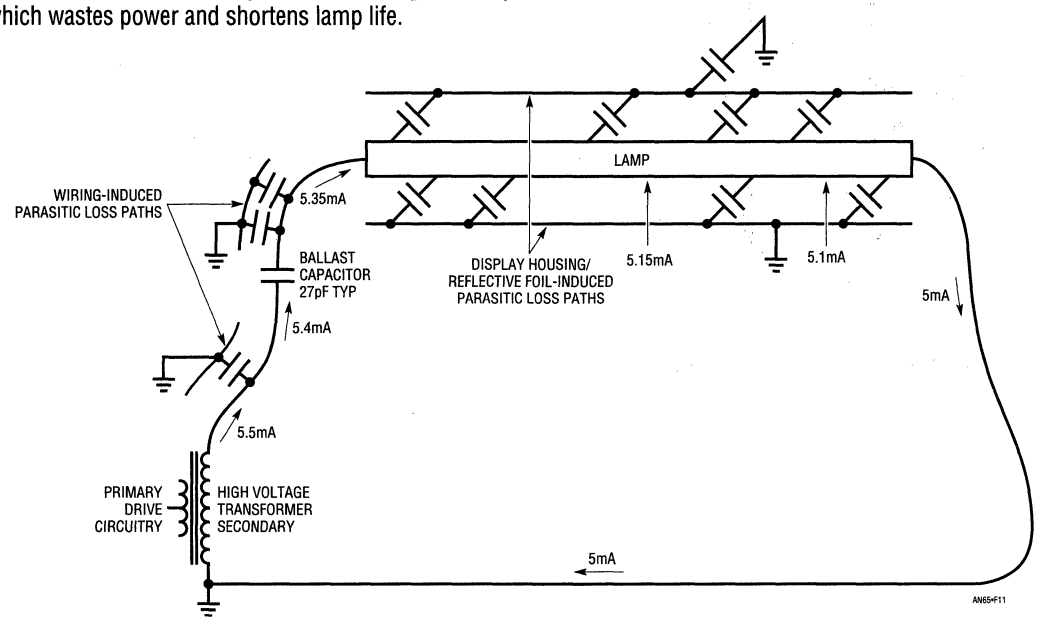


Figure 11. Distributed Parasitic Capacitances in a Practical Situation Cause Continuous Downward Shift in Measured "Lamp Current." In This Case 0.5mA Is Lost to Parasitic Paths. Most Loss Occurs in High Voltage Regions

The lessons here are clear. A thorough characterization of lamp/display losses is crucial to understanding trade-offs and obtaining the best possible performance. The highest efficiency "in system" backlights have been produced by careful attention to these issues. In some cases the entire display enclosure was re-engineered for lower losses.

The display loss issue, central to backlight design, merits detailed attention. The following briefly commented photographs (Figures 12 through 32) illustrate a variety of display situations. Hopefully, this visual tour will alert display users and manufacturers to the problems involved, promoting appropriate action by both.

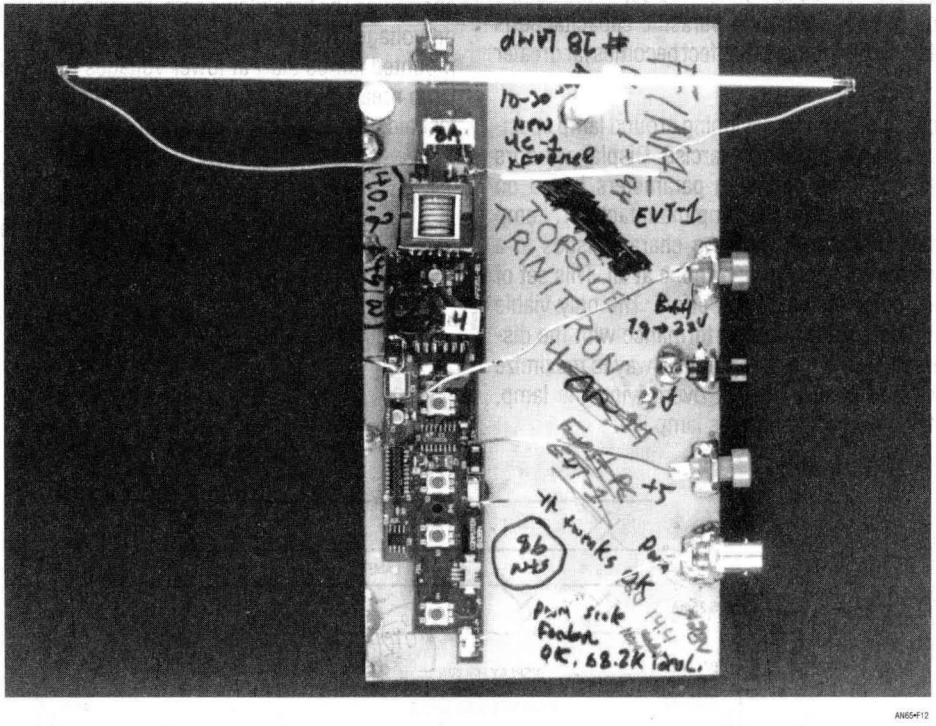
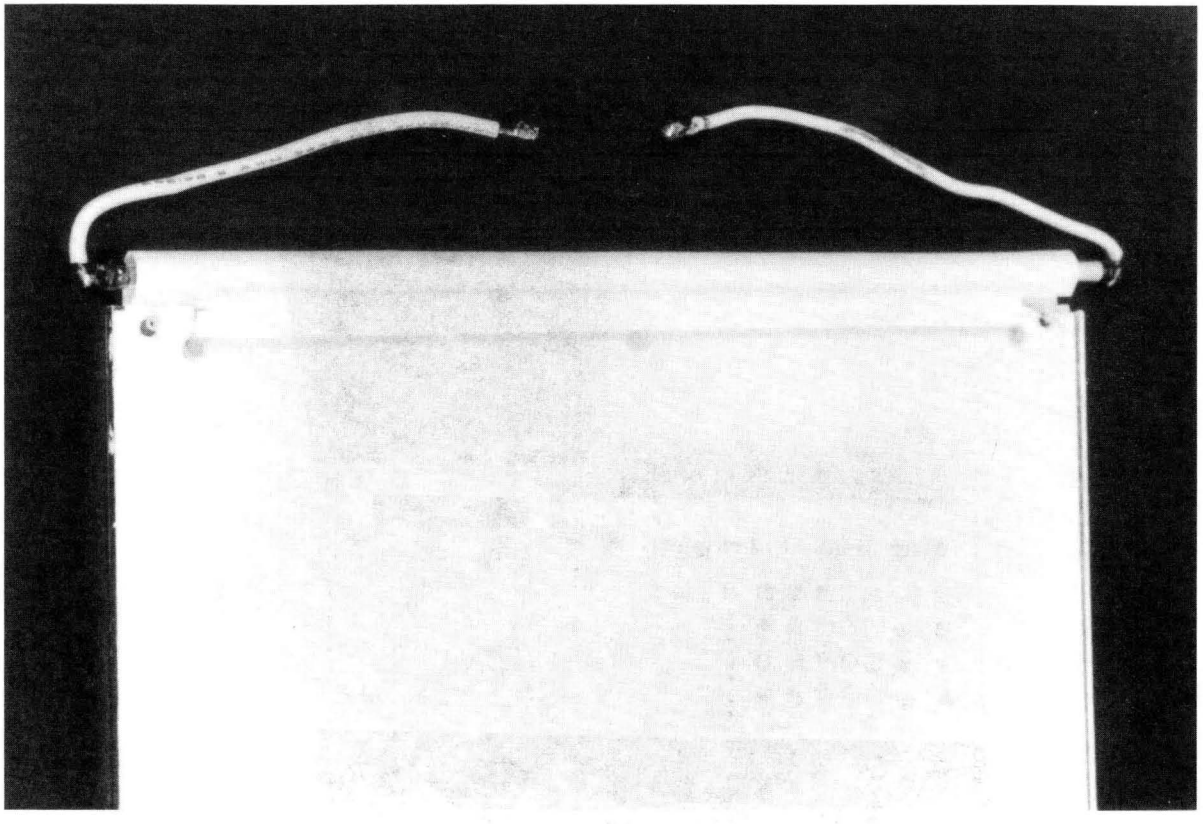


Figure 12. The Ideal Display Is No Display. Drive Electronics Connected to a "Naked" Lamp Simulates a Zero Loss Display. Note Nylon Stand-Offs. Results Obtained Have No Relationship to Practical Display Driving

Figure 13. Measuring Lamp Wire to Display Frame Capacitance. Technique Gives Lead Wire-to-Frame Loss Information but Not Lamp-to-Foil-or-Frame Loss Data. Lamp Must Be Energized Before Its Parasitics Are Measurable



AN65-F14

Figure 14. Low Loss Display Has No Metal in Lamp Region. Reflective Foil Floats from Ground and Has Low Absorption. Display Loss About 1.5%

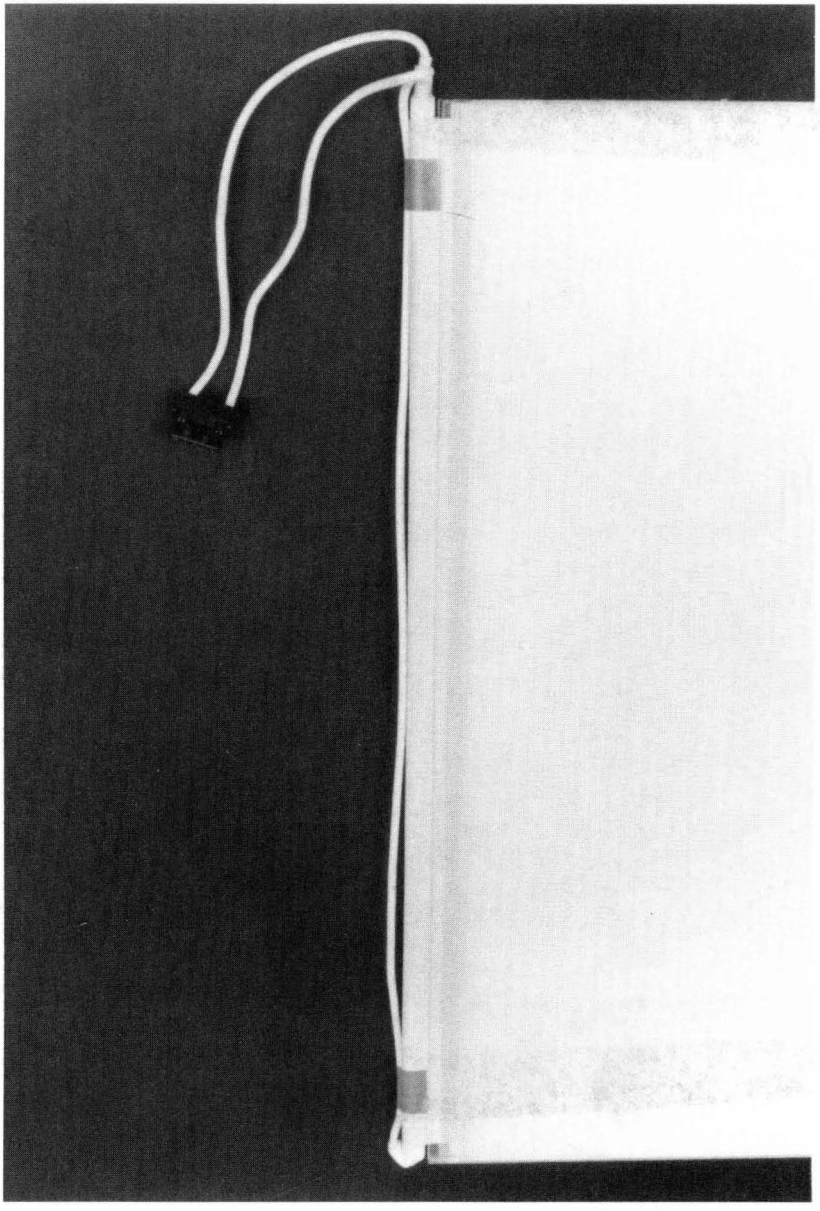
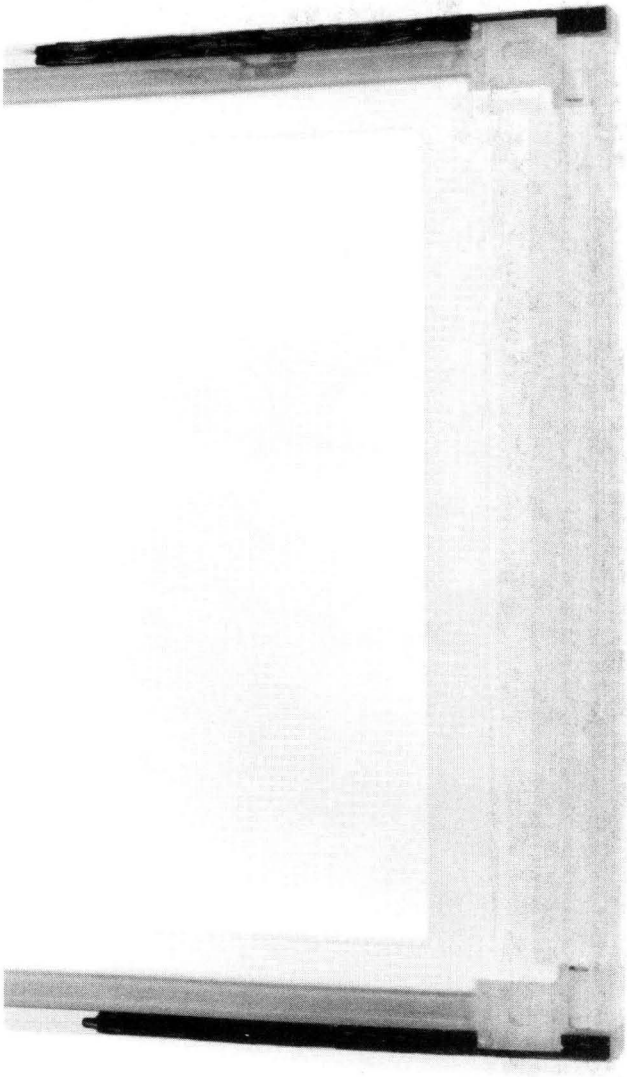


Figure 15. Another Low Loss Display Has Similar Characteristics to Figure 14. Running Long Wire Return Across Lamp Length Increases Loss to about 4%. Spacing Wire Away from Lamp Would Cut Loss by Half



AN65-F16

Figure 16. A Custom Designed, Extremely Low Loss Display. All Metal Is Eliminated in Lamp Area (Lower Portion of Photo). A Good Compromise Between Mechanical Strength and Loss Control

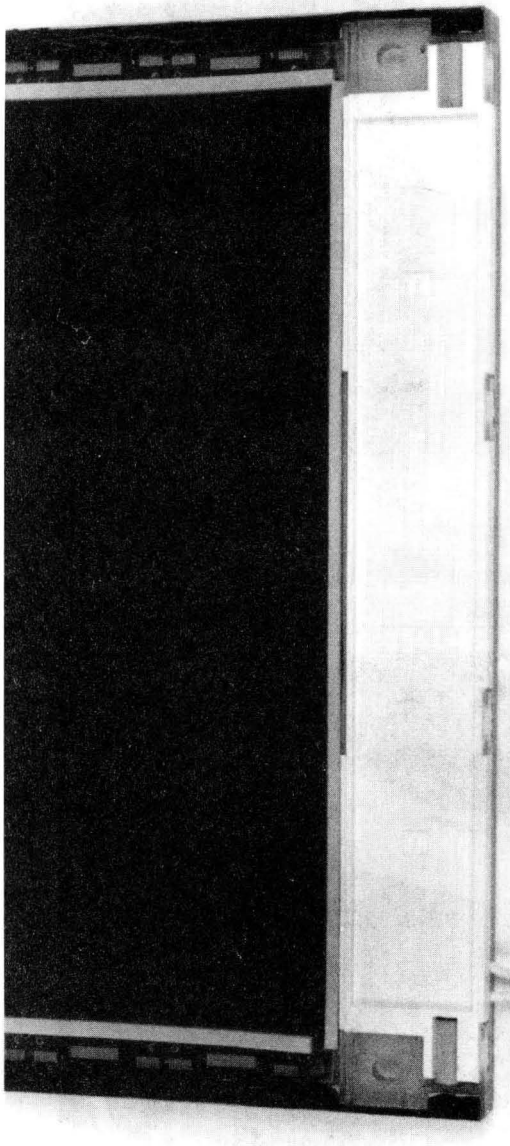


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Figure 17. Figure 16's Reverse Side. All Metal Is Relieved in Lamp Area, Maintaining Low Losses. An Excellent, Practical Display

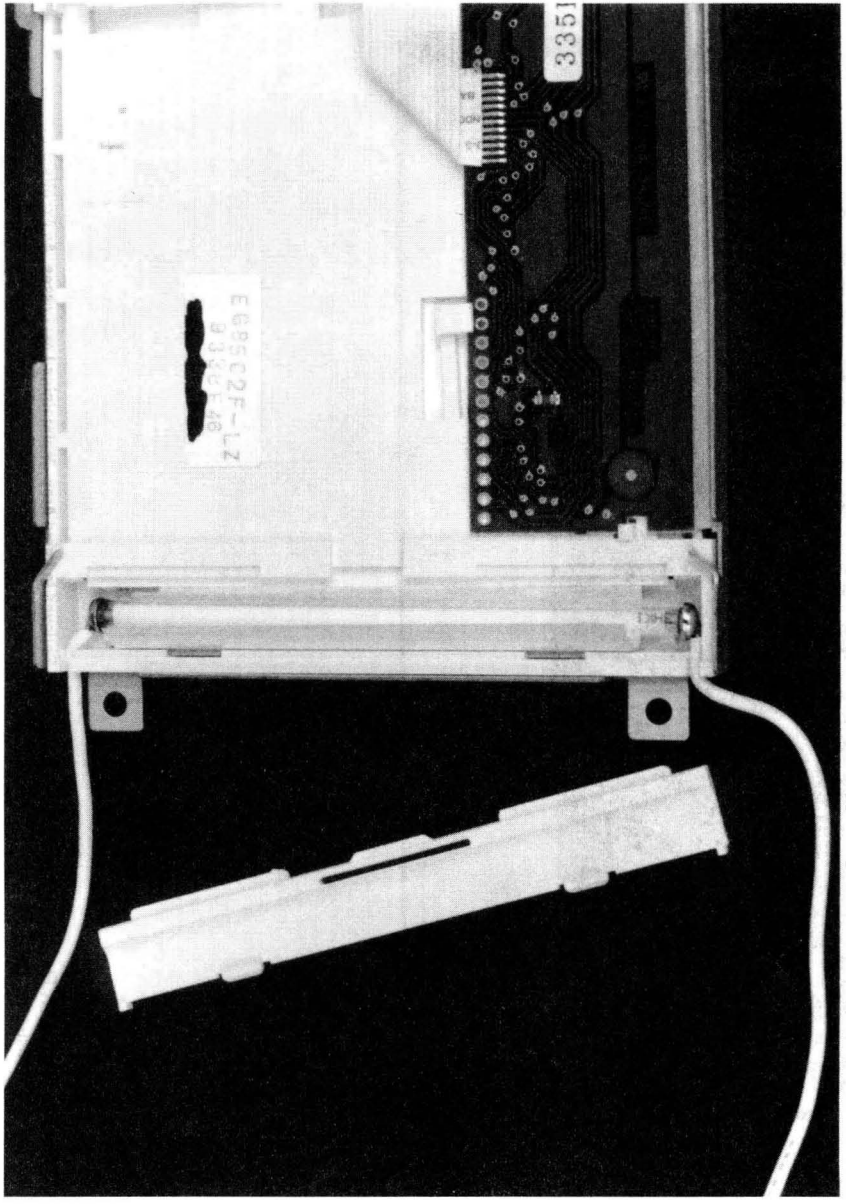
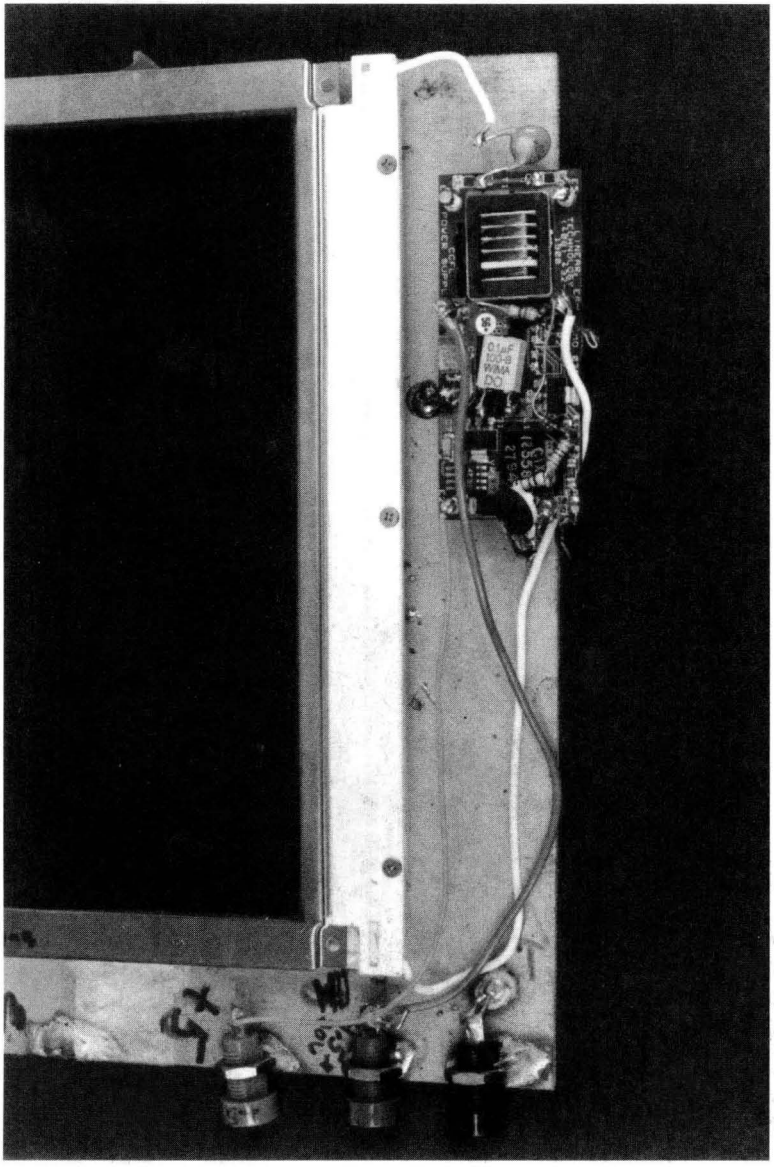
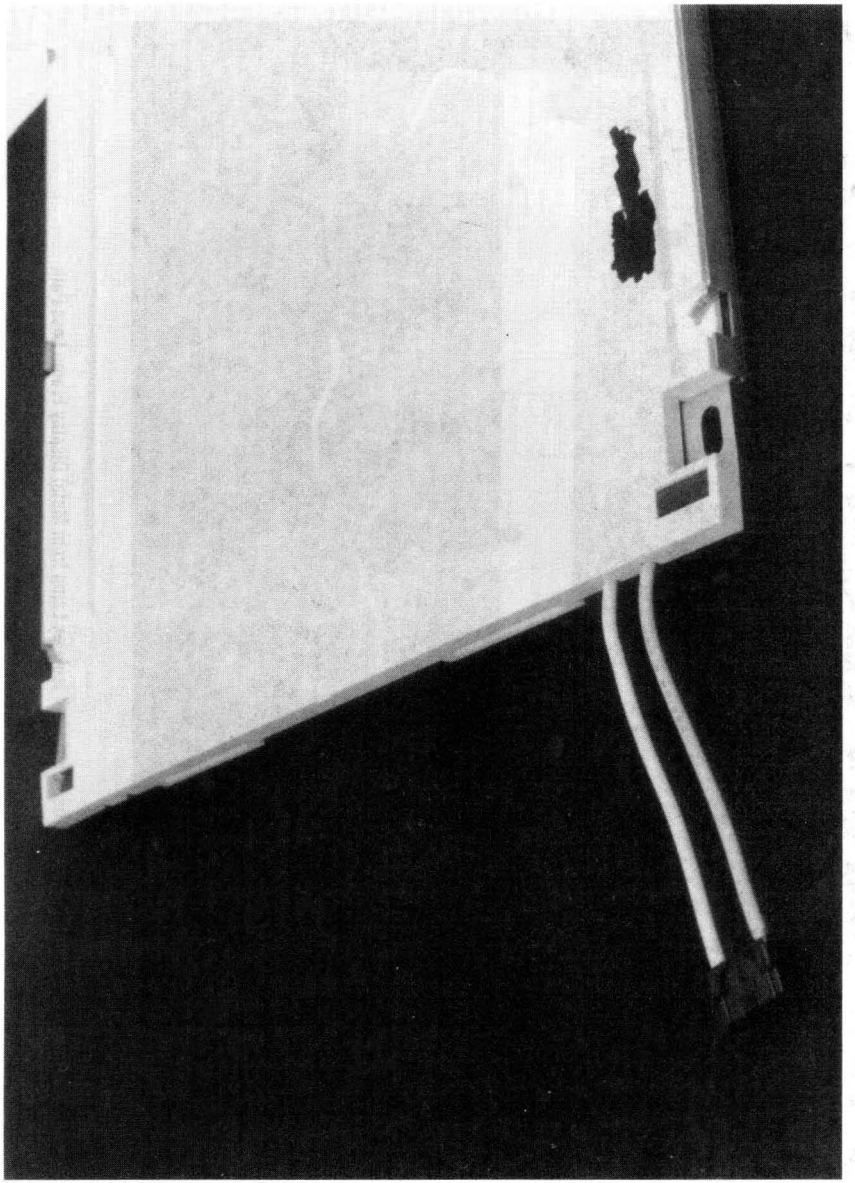


Figure 18. Plastic "Cocoon" Cuts Losses. Metallic Foil Is Absorptive but Floats from Grounded Display Frame. A Good Compromise with about 4% Loss



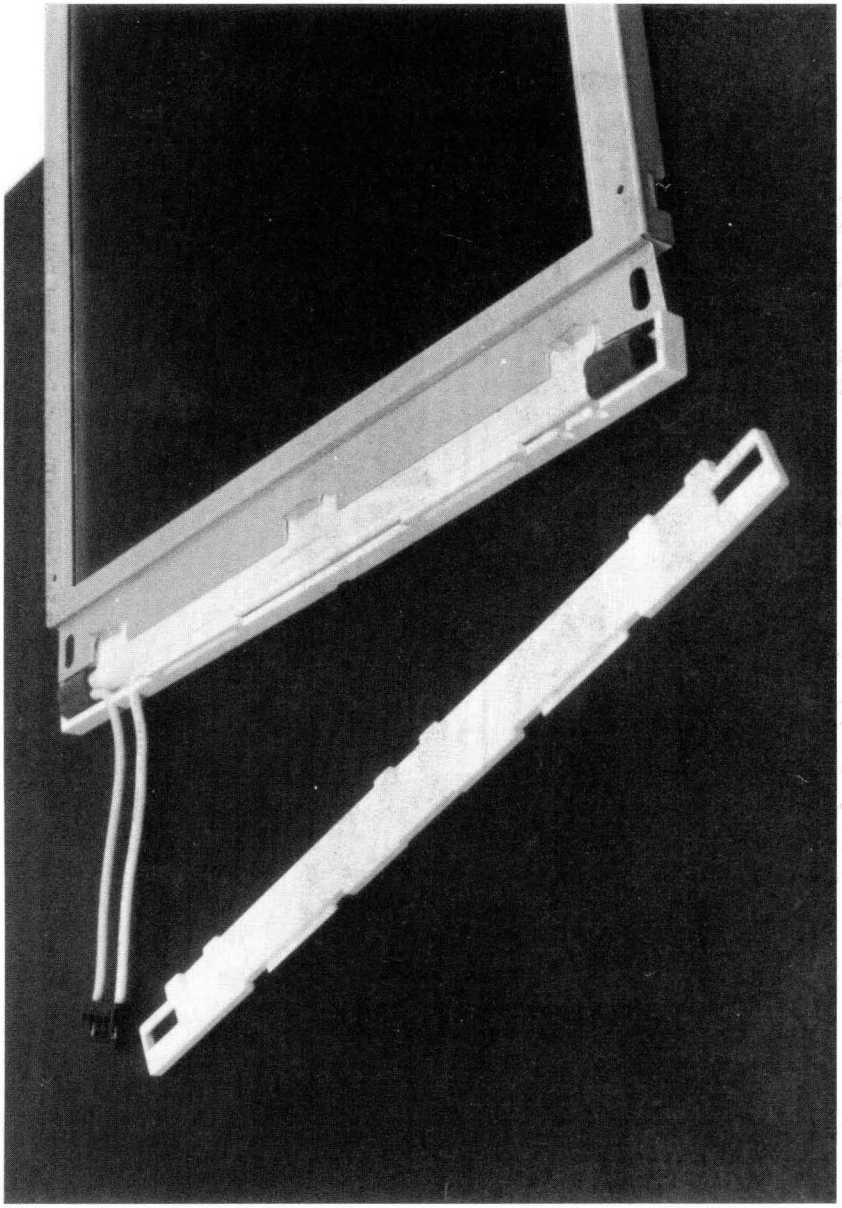
AN65-F19

Figure 19. Plastic "Outrigger" Isolates Lamp from Metal Display Frame Loss Path



AN65#20

Figure 20. Plastic Isolates Lamp from Metal Frame in This Display's Rear View

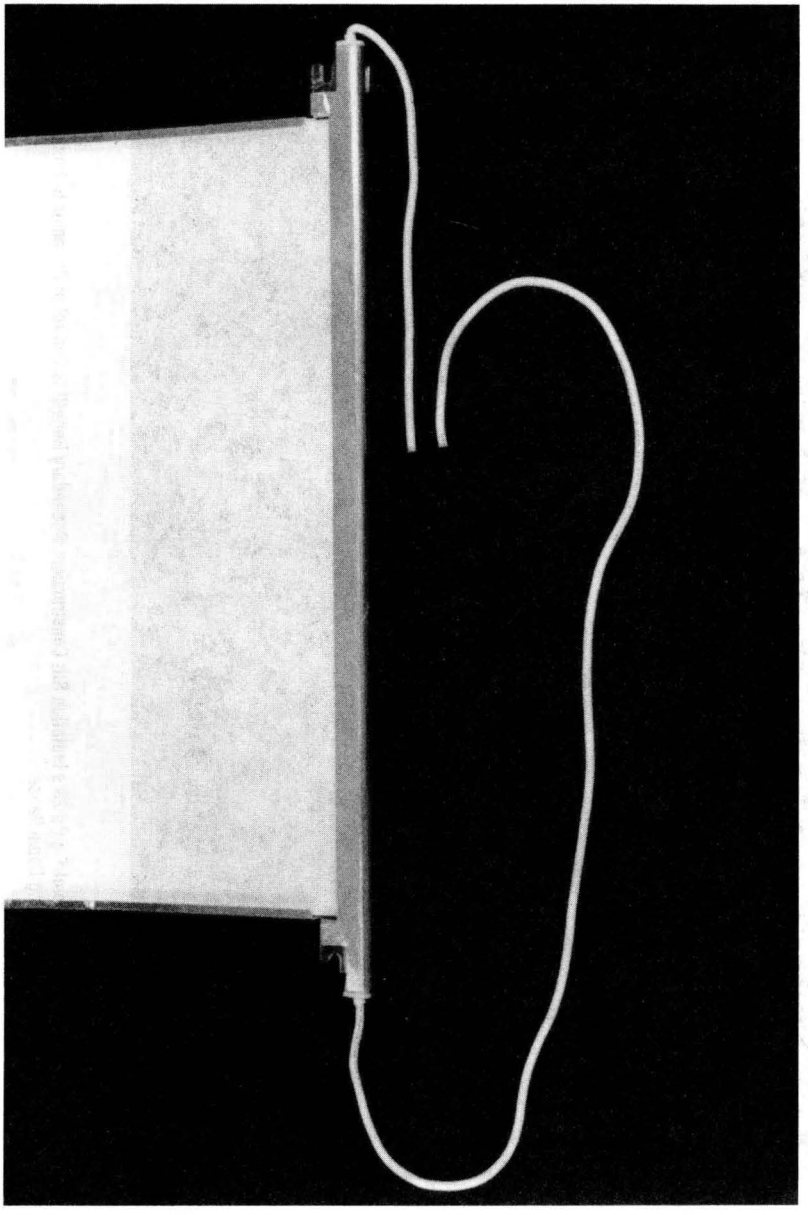


AN65#21

Figure 21. Figure 20's Display Front View Continues Plastic Isolation Treatment but Reflective Foil (over Lamp) Contacts Metal Frame. Massive Losses via This Path Cause Overall 12% Loss. Trimming Foil from Metal Cuts Loss to 4%

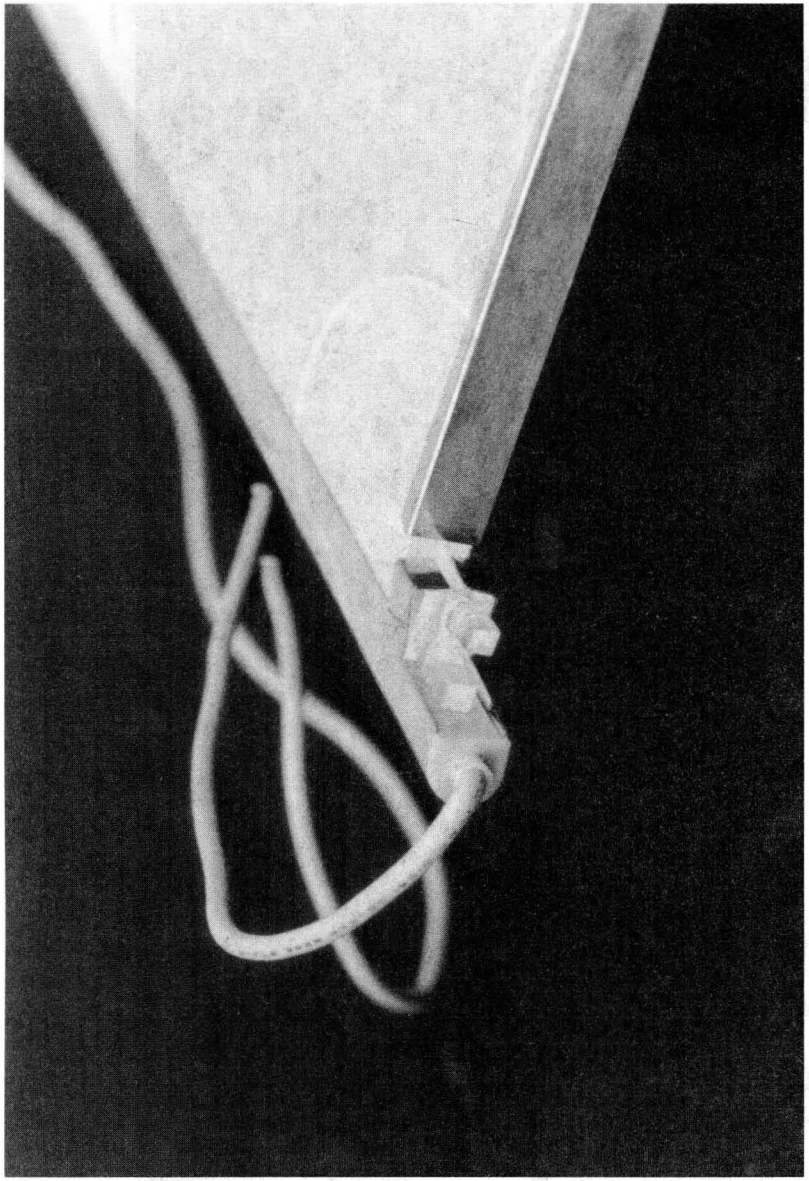
AN65•F22

Figure 22. Another "Outrigged" Plastic Enclosure Suffers Foil Contacting Display's Frame Metal. Relieving Foil from Metal Cuts Losses from 13% to 6%. Poor Wire Routing (Lower Right) Causes 3% Loss



AN65-F23

Figure 23. Isolation Slits (Center Right and Left) in Metal Reflector Prevent Losses to Grounded Metal Frame (Upper Right and Left). Overall Losses About 6%



AN65F24

Figure 24. Close-Up of Figure 23's Isolation Slit Construction. Secondary Benefit Is Control of Reflector-to-Lamp Distance, Minimizing Capacitance

Figure 25. Metal Cover over Lamp Causes 15% Loss. Replacing Cover Securing Screws with Nylon Types Floats Cover from Ground, Dropping Loss to 8%. Replacing Cover with Plastic Improves Loss to Only 3% . . . a 5X Improvement!

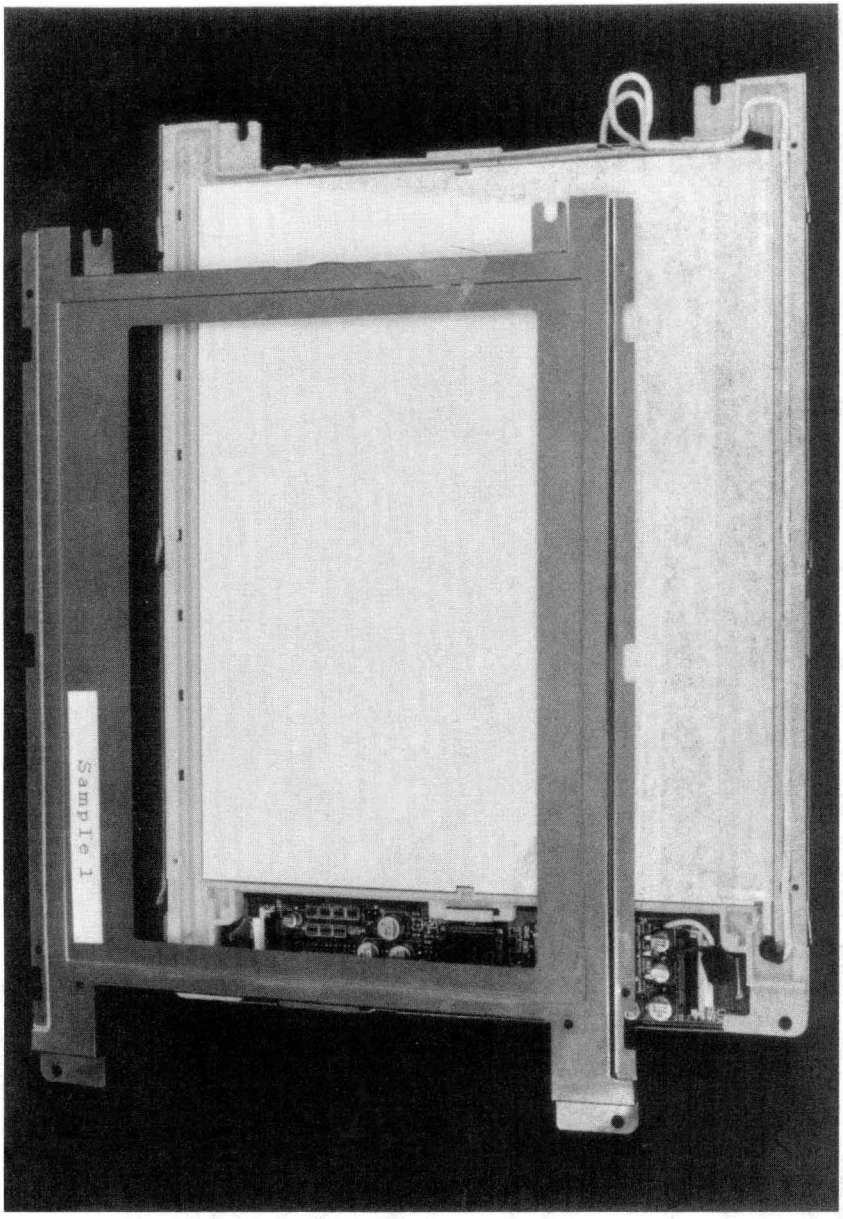
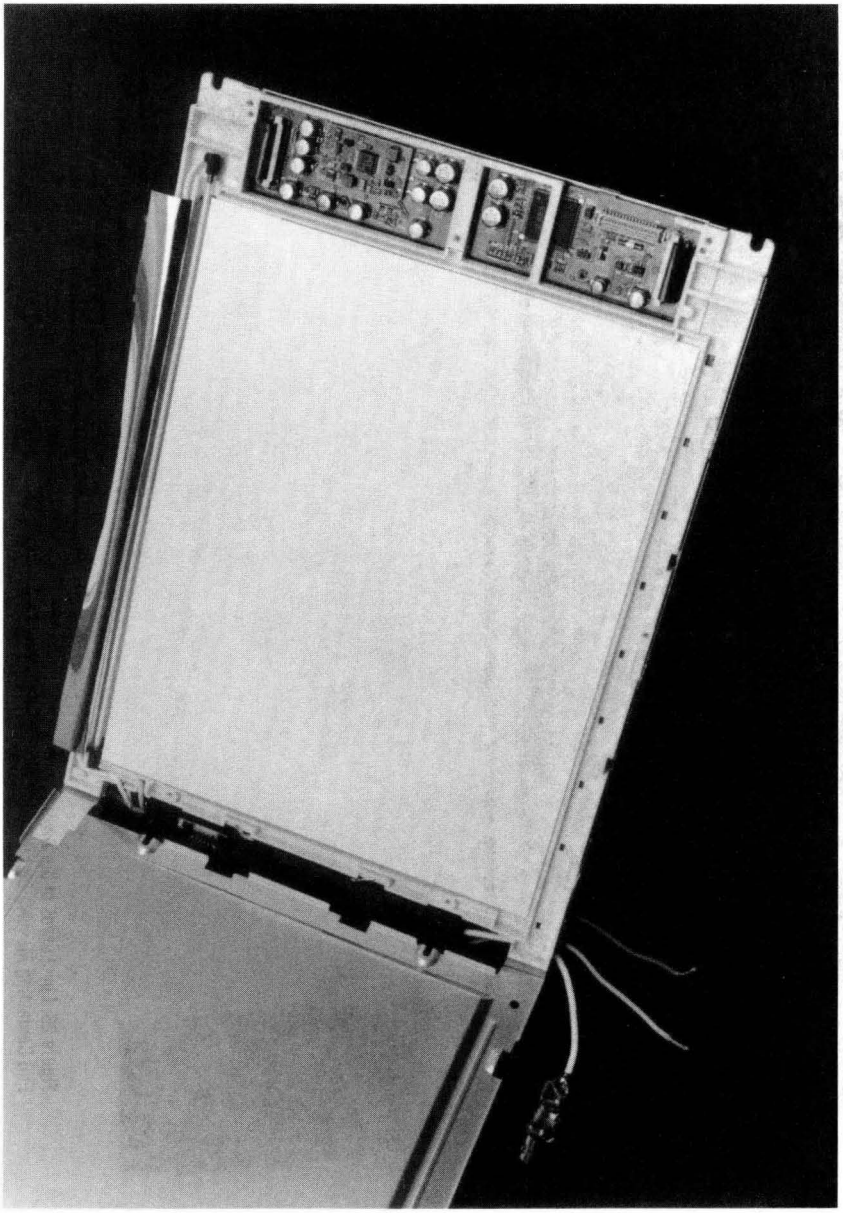
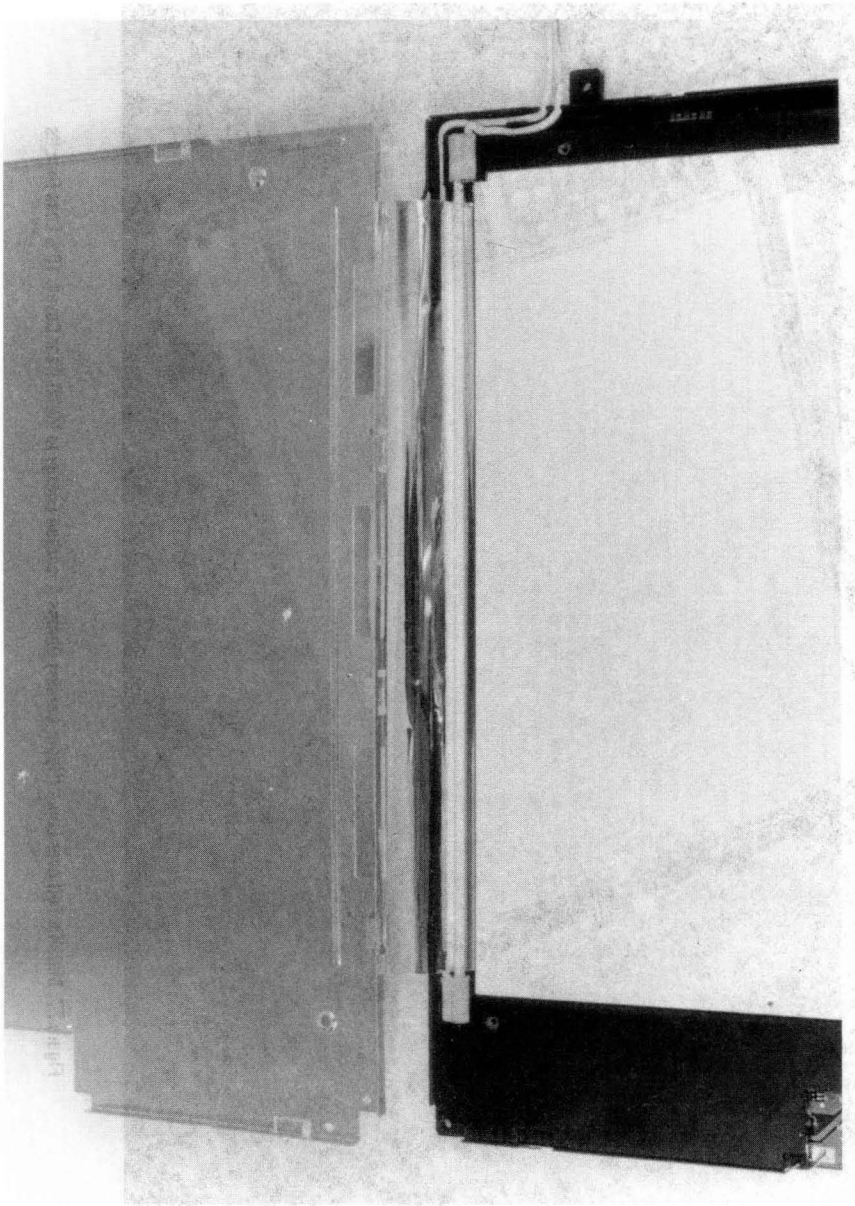


Figure 26. Huge Metal Area over Lamp Causes 14% Loss. Replacing Metal in Lamp Area with Plastic Cuts Loss to 6%



AN65-F27

Figure 27. Metallic Foil over Lamp (Upper Center) Dumps Absorbed Energy to Metal Rear Cover. 16% Loss Results



AN65-F28

Figure 28. Low Losses of the Display's Nonconductive Frame (Black Plastic) Are Thrown Away by Lossy Reflective Foil Contacting Massive Metal Rear Cover. 15% Loss Results

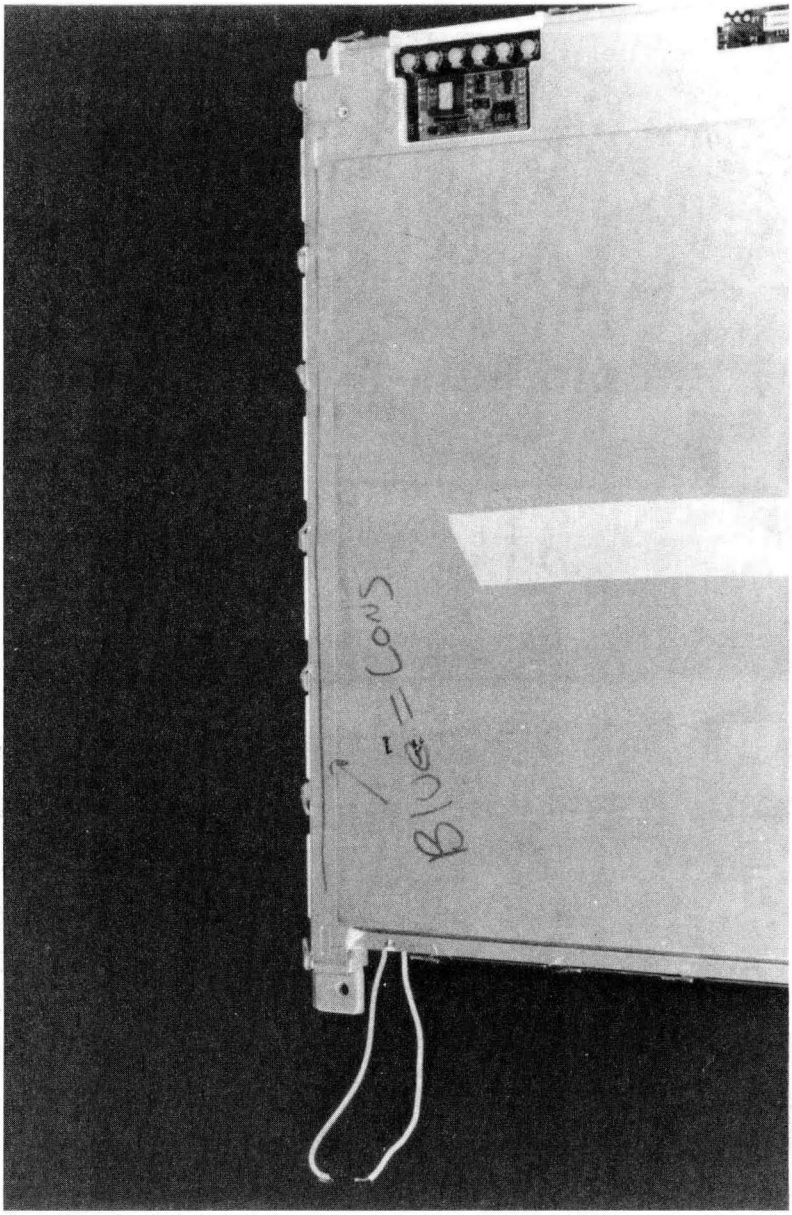


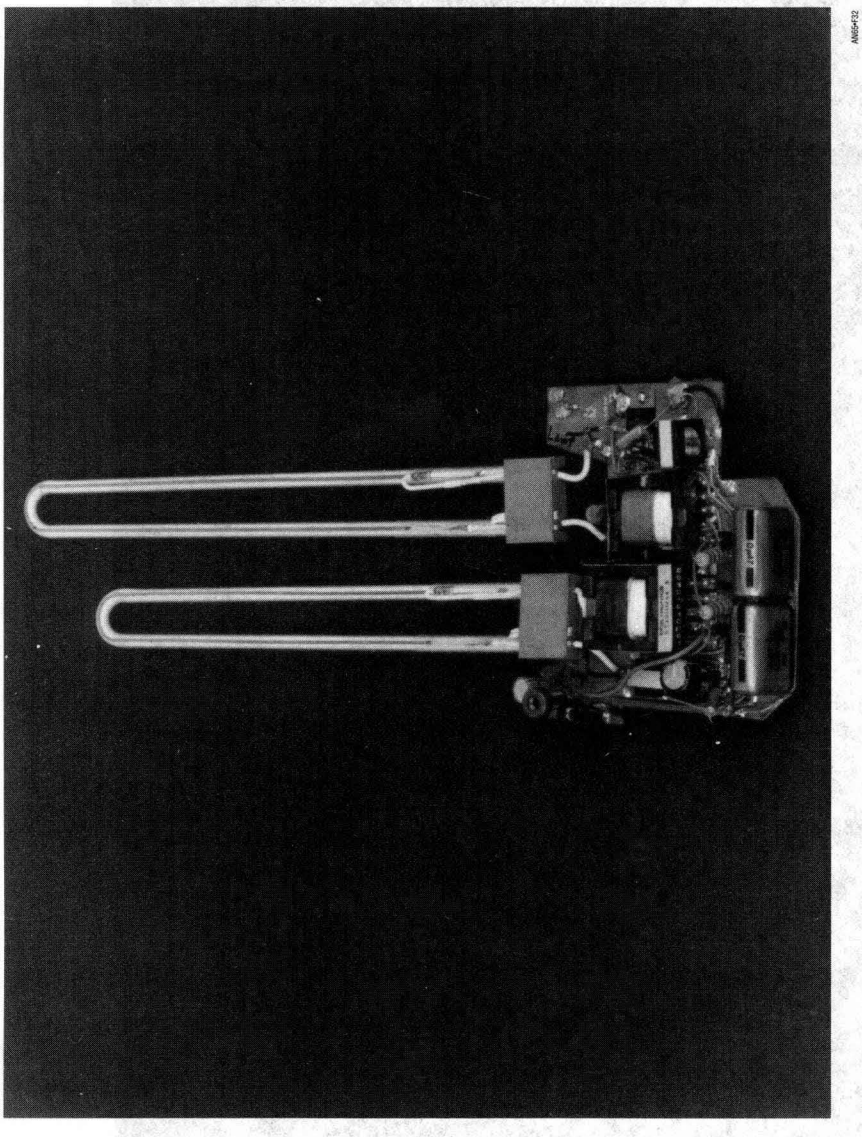
Figure 29. A Similar Situation to Figure 28. Large Metal Rear Cover Contacts Lossy Foil (Not Visible), Causing Huge Losses

AN65-F30

Figure 30. Grounded Metallic Optical Reflector in Automotive Lamp Introduces 18% Loss. Optical Gain over Nonmetallic Reflector May Justify Large Electrical Loss

AN65-F31

Figure 31. Metallic Heater on Lamp in this Automotive Application Eases Low Temperature Starting but Causes 31% Loss



AN65-32

Figure 32. Similar to Figure 31. Metallic Cold Start Heaters in Automotive Application Induce 23% Loss

Considerations for Multilamp Designs

Multiple-lamp designs are not recommended if lamp intensity matching is important. Maintaining emission matching over time, temperature and production variations is quite difficult. In some restricted cases multilamp displays may be a viable option, but a single lamp with good diffuser optics is almost always the better approach. Information on dual-lamp displays is presented here for reference purposes only.[5]

Systems using two lamps have some unique layout problems. Almost all dual-lamp displays are color units. The lower light transmission characteristics of color displays necessitates more light. As such, display manufacturers sometimes use two lamps to produce more light. The wiring layout of these dual-lamp color displays affects efficiency and illumination balance in the lamps. Figure 33 shows an "x-ray" view of a typical display. This symmetrical arrangement presents equal parasitic losses. If C1 and C2 and the lamps are well-matched, the circuit's current output splits evenly and equal illumination occurs.

Figure 34's display arrangement is less friendly. The asymmetrical wiring forces unequal losses and the lamps receive imbalanced current. Even with identical lamps, illumination may not be balanced. This condition is partially correctable by skewing values of C1 and C2 . C1, because it drives greater parasitic capacitance, should be larger than C2. This tends to equalize the currents, promoting equal lamp drive. It is important to realize that this compensation does nothing to recapture the lost energy—efficiency is still compromised. There is no substitute for minimizing loss paths. Similarly, any change in lamp characteristics (e.g., aging) can cause imbalanced illumination to recur.

In general, imbalanced illumination causes fewer problems than might be supposed at high intensity levels. Unequal illumination is much more noticeable at lower levels. In the worst case the dimmer lamp may only partially illuminate. This phenomenon, sometimes called "Thermometering," is discussed in detail in the text section, "Floating Drive Circuits."

Note 5. The text's tone is intended to convey our distaste for multilamp displays. They are the very soul of heartache.

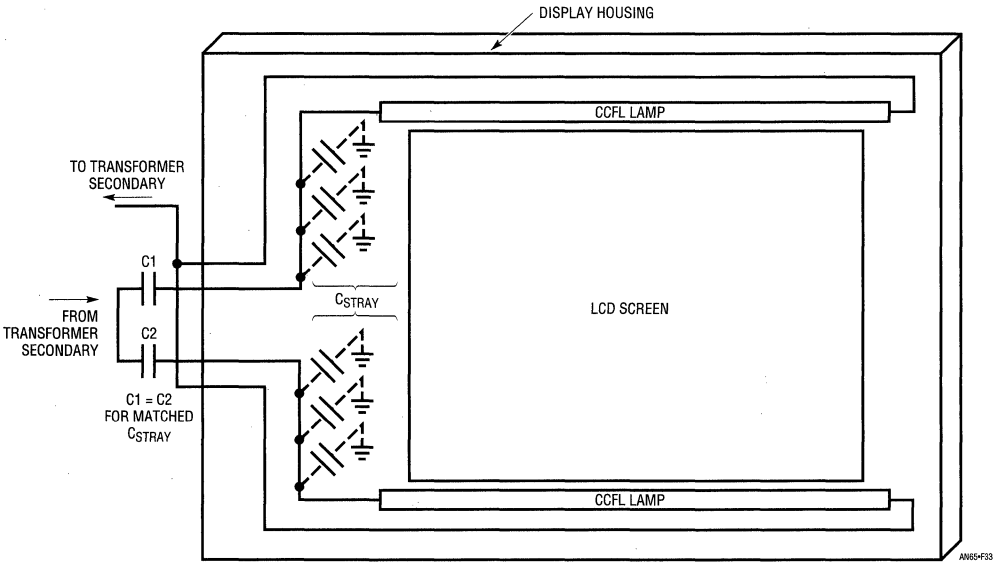


Figure 33. Loss Paths for "Best Case" Dual-Lamp Display. Symmetry Promotes Balanced Illumination, but Lamp Limitations Dominate Achievable Results

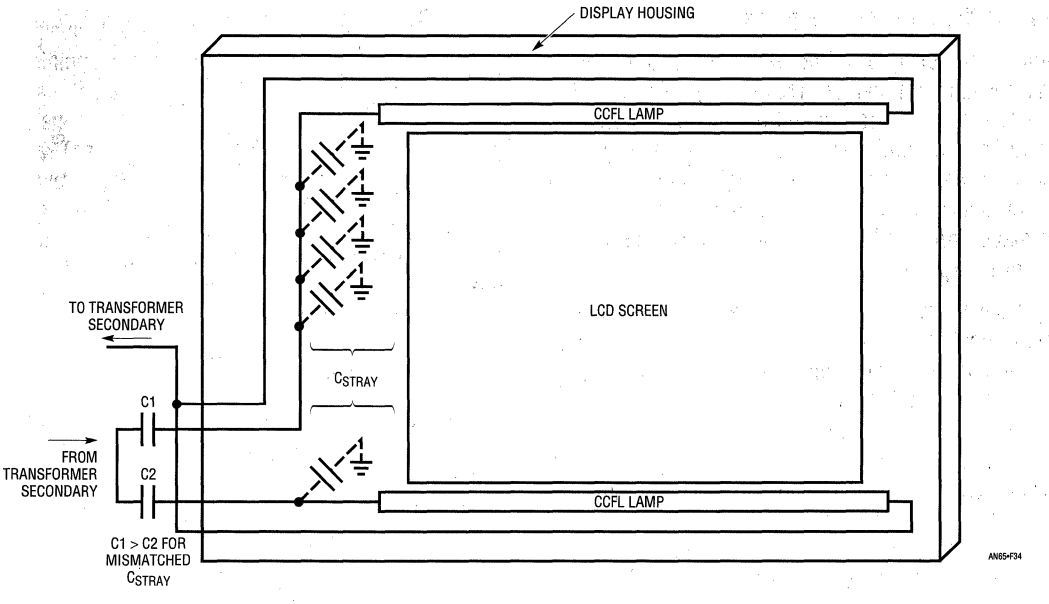


Figure 34. Asymmetric Losses in a Dual-Lamp Display. Skewing C1 and C2 Values Compensates Imbalanced Loss Paths but Not Wasted Energy

CCFL Power Supply Circuits

Choosing an approach for a general purpose CCFL power supply is difficult. A variety of disparate considerations make determining the "best" approach a thoughtful exercise. Above all, the architecture must be extraordinarily *flexible*. The sheer number and diversity of applications demands this. The considerations take many degrees of freedom. Power supply voltages range from 2V to 30V with output power from minuscule to 50W. The load is highly nonlinear and varies over operating conditions. The backlight is often located some distance from the primary power source, meaning the supply must tolerate substantial supply bus impedances. Similarly, it must not corrupt the supply bus with noise, or introduce appreciable RFI into the system or environment. Component count should be low and the supply must be physically quite small as space is usually extremely limited. Additionally, the circuit must be relatively layout-insensitive because of varying board shape requirements. Interface for shutdown and dimming control should accommodate either digital or analog inputs, including voltage, current, resistive, PWM or serial bit-stream addressing. Finally, lamp current should be predictable and stable with changes in time, temperature and supply voltage.

A current-fed, feedback-controlled resonant Royer converter meets these requirements.[6] This approach, because of its extreme flexibility, is a favorable compromise. It operates over wide supply ranges and scales well over a broad output power range. Current is taken from the supply bus almost continuously, making the circuit tolerate supply bus impedance. This characteristic also means that circuit operation does not corrupt power supply lines. There is no RFI problem and component count is low. It is small, relatively insensitive to layout and easy to interface to. Lastly, lamp current is stable and predictable over operating conditions.

Note 6. See Appendices K and L for detailed discussion on architecture selection and the Royer configuration.

Figure 35 is a practical CCFL power supply circuit based on the above discussion. Efficiency is 88% with an input voltage range of 6.5V to 20V. This efficiency figure can be degraded by about 3% if the LT®1172 V_{IN} pin is powered from the same supply as the main circuit V_{IN} terminal. Lamp intensity is continuously and smoothly variable from zero to full intensity. When power is applied the LT1172 switching regulator's Feedback pin is below the device's internal 1.2V reference, causing full duty cycle modulation at the V_{SW} pin (Trace A, Figure 36). V_{SW} conducts current (Trace B) which flows from L1's center tap,

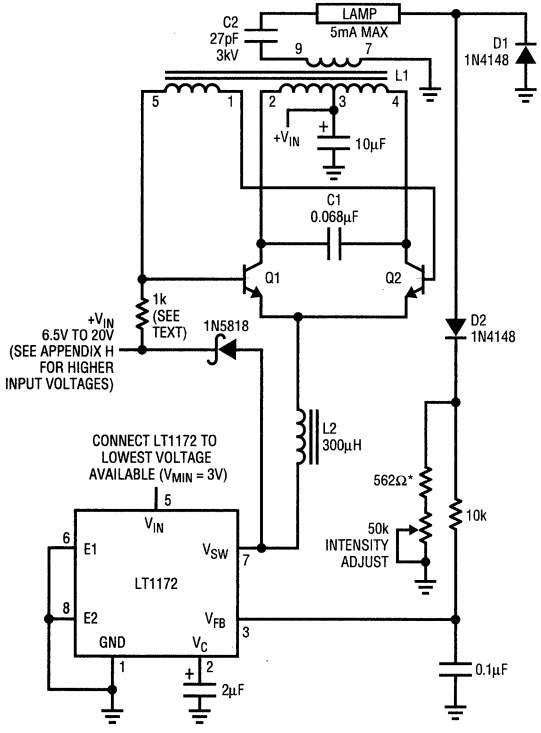


Figure 35. An 88% Efficiency Cold Cathode Fluorescent Lamp Power Supply

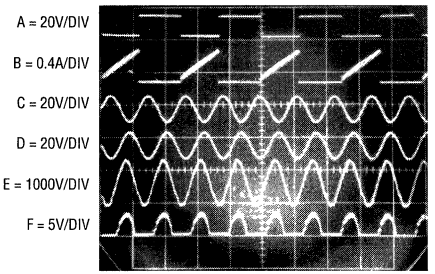


Figure 36. Waveforms for the Cold Cathode Fluorescent Lamp Power Supply. Note Independent Triggering on Traces A and B, and C through F

through the transistors, into L2. L2's current is deposited in switched fashion to ground by the regulator's action.

L1 and the transistors comprise a current driven Royer class converter[7] which oscillates at a frequency primarily set by L1's characteristics (including its load) and the 0.068µF capacitor. LT1172 driven L2 sets the magnitude of the Q1/Q2 tail current, hence L1's drive level. The 1N5818 diode maintains L2's current flow when the LT1172 is off. The LT1172's 100kHz clock rate is asynchronous with respect to the push/pull converter's (60kHz) rate, accounting for Trace B's waveform thickening.

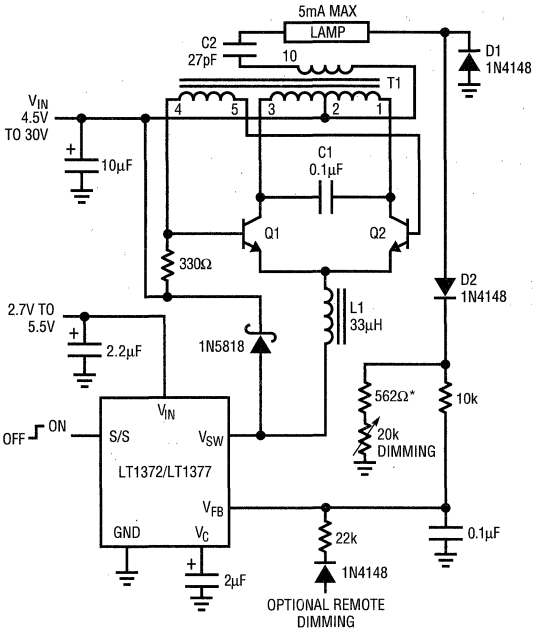
The 0.068µF capacitor combines with L1's characteristics to produce sine wave voltage drive at the Q1 and Q2 collectors (Traces C and D respectively). L1 furnishes voltage step-up and about $1400V_{P-P}$ appears at its secondary (Trace E). Current flows through the 27pF capacitor into the lamp. On negative waveform cycles, the lamp's current is steered to ground via D1. Positive waveform cycles are directed via D2 to the ground referred 562Ω/50k potentiometer chain. The positive half-sine appearing across the resistors (Trace F) represents 1/2 the lamp current. This signal is filtered by the 10k/0.1µF pair and presented to the LT1172's Feedback pin. This connection closes a control loop which regulates lamp current. The 2µF capacitor at the LT1172's V_C pin provides stable loop compensation. The loop forces the LT1172 to switch

Note 7. See Appendix K, "Who Was Royer and What Did He Design?" See also Reference 2.

mode modulate L2's average current to whatever value is required to maintain constant current in the lamp. The constant current's value, and hence lamp intensity, may be varied with the potentiometer. The constant current drive allows full 0% to 100% intensity control with no lamp dead zones or "pop-on" at low intensities.[8] Additionally, lamp life is enhanced because current cannot increase as the lamp ages.

The circuit's 0.1% line regulation is notably better than some other approaches. This tight regulation prevents lamp intensity variation when abrupt line changes occur. This typically happens when battery-powered apparatus is connected to an AC-powered charger. The circuit's excellent line regulation derives from the fact that L1's drive waveform never changes shape as input voltage varies. This characteristic permits the simple 10kΩ/0.1μF RC to produce a consistent response. The RC averaging characteristic has serious error compared to a true RMS conversion, but the error is constant and "disappears" in the 562Ω shunt's value.

This circuit is similar to one previously described[9] but its 88% efficiency is 6% higher. The efficiency improvement is primarily due to the transistor's higher gain and lower saturation voltage. The base drive resistor's value (nominally 1k) should be selected to provide full V_{CE} saturation without inducing base overdrive or beta starvation. A procedure for doing this is described in a following section, "General Optimization and Measurement Considerations."



C1 = WIMA MKP-20, PANASONIC ECH-U
L1 = COILCRAFT DT3316-333
Q1, Q2 = ZETEX ZTX849, ZDT1048
OR ROHM 2SC5001
T1 = COILTRONICS CTX 02-12614-1 OR
CTX110600-1 (SEE TEXT)
* = 1% FILM RESISTOR

DO NOT SUBSTITUTE COMPONENTS
COILTRONICS (407) 241-7876
COILCRAFT (708) 639-6400

AN65•F37

Figure 37. A 91% Efficient CCFL Supply for 5mA Loads Features Shutdown and Dimming Inputs. Higher Frequency Switching Regulator Reduces L1's Size While Requiring Less V_{IN} Current

Figure 37's circuit is similar, but uses a transformer with lower copper and core losses to increase efficiency to 91%. The trade-off is slightly larger transformer size. Additionally, a higher frequency switching regulator offers slightly lower V_{IN} current, aiding efficiency. L1's smaller value, a result of the higher frequency operation, permits slightly reduced copper loss. The transformer options listed allow efficiency optimization over the supply range of interest. Value shifts in C1, L2 and the base drive resistor reflect different transformer characteristics. This circuit also features shutdown and a DC or pulse width controlled dimming input. Appendix F, "Intensity Control and Shutdown Methods," details operation of these features. Figure 38, directly derived from Figure 37, produces 10mA output to drive color LCDs at 92% efficiency. The slight efficiency improvement comes from a reduction in regulator "housekeeping" current as a percentage of total current drain. Value changes in components are the result of higher power operation. The most significant change involves driving two lamps. Accommodating two lamps involves separate ballast capacitors but circuit operation is similar. Dual-lamp designs reflect slightly different loading back through the transformer's primary. C2 usu-

Note 8. Controlling a nonlinear load's current, instead of its voltage, permits applying this circuit technique to a wide variety of nominally evil loads. See Appendix I, "Additional Circuits."

Note 9. See "Illumination Circuitry for Liquid Crystal Displays," Linear Technology Corporation, Application Note 49, August 1992 and "Techniques for 92% Efficient LCD Illumination," Linear Technology Corporation, Application Note 55, August 1993.

ally ends up in the 10pF to 47pF range. Note that C2A and B appear with their lamp loads in parallel across the transformer's secondary. As such, C2's value is often smaller than in a single-lamp circuit using the same type lamp. Ideally, the transformer's secondary current splits evenly between the C2-lamp branches, with the total load current being regulated. In practice, differences between C2A and B, and differences in lamps and lamp wiring layout preclude a perfect current split. Practically, these differences are small and the lamps appear to emit an equal amount of light at high intensity. Layout and lamp matching can influence C2's value. Some techniques for dealing with these issues appear in the text section, "Considerations for Multilamp Designs." As previously stated, dual-lamp designs are distinctly not recommended, particularly if balanced illumination over wide dimming ranges is required.

Figure 39 uses a dedicated CCFL IC, the LT1183, to enhance circuit performance. The Royer-based high voltage converter portion is recognizable from previous circuits, with the 200kHz LT1183 performing the switching regulator/feedback function. This IC also features open lamp protection circuitry, simplified frequency compensation, a separate regulator providing LCD contrast and other features.[10] The contrast supply is driven by the LT1183 with L3 and associated discrete components completing the function. The CCFL and contrast outputs may be adjusted with DC, PWM or potentiometers.

Note 10. Open lamp protection is often desirable and may be added to the previous circuits at the cost of some discrete components. See Appendix E, "Open Lamp/Overload Protection." Frequency compensation issues are covered in the text section "Feedback Loop Stability Issues." See Appendix J for discussion of LCD contrast supplies.

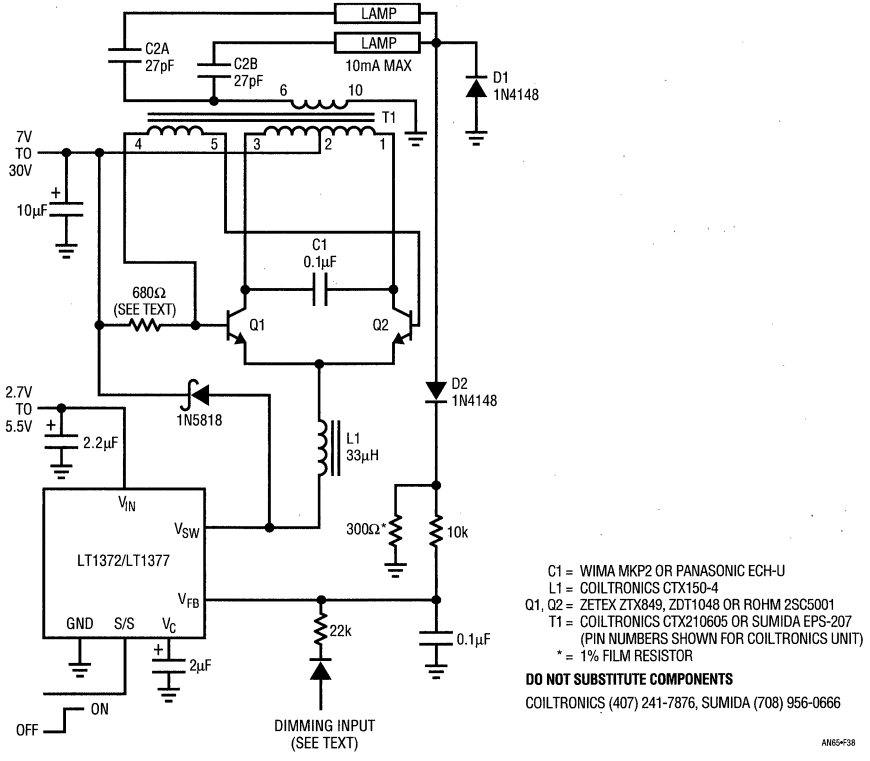


Figure 38. A 92% Efficient CCFL Supply for 10mA Loads Features Shutdown and Dimming Inputs. Dual-Lamp Designs, Typical of Early Color Displays, Are Not Recommended

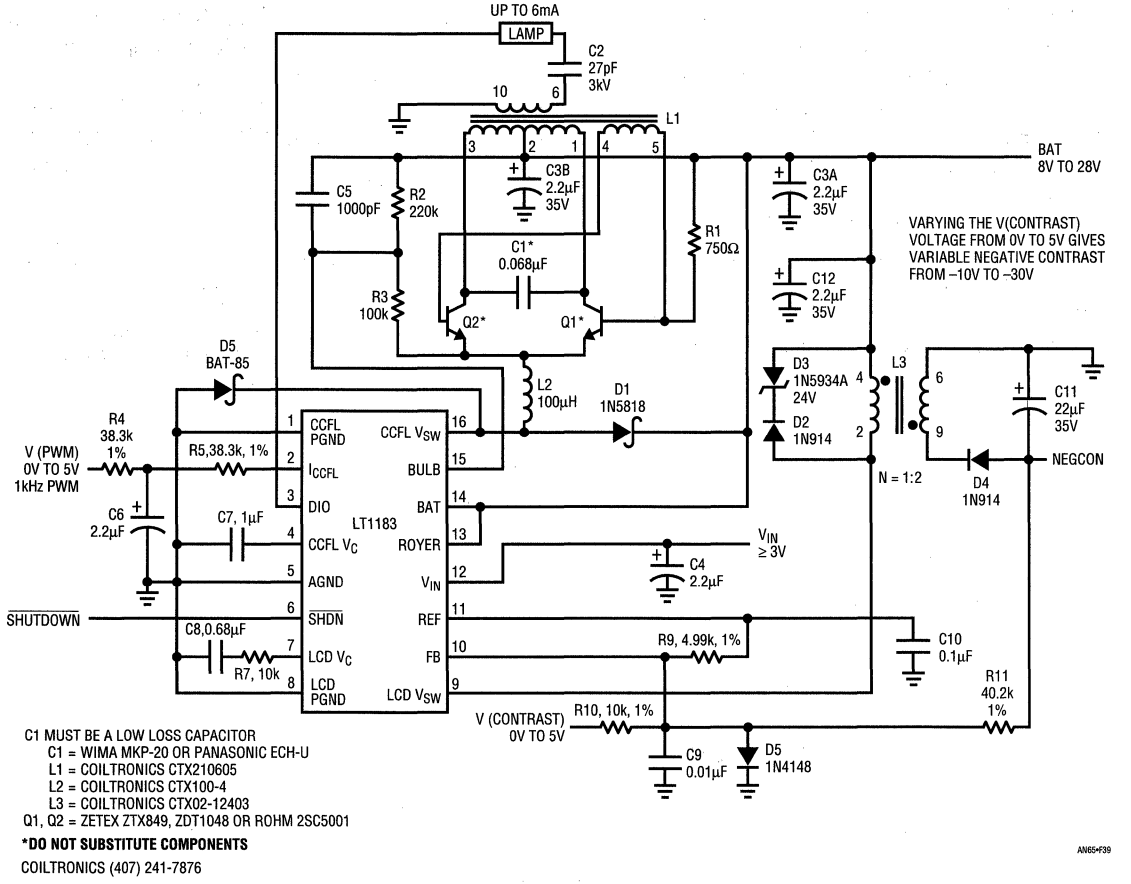


Figure 39. Dedicated Backlight IC Includes Switching Regulator, Open Lamp Protection and LCD Contrast Supply. 200kHz Operation Minimizes L2 Size. Shutdown and Control Inputs Are Simplified

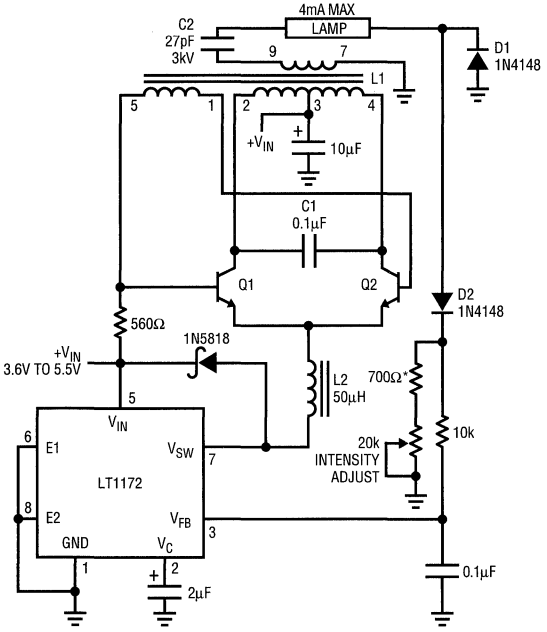
Low Power CCFL Power Supplies

Many applications require relatively low power CCFL backlighting. Figure 40's variation, optimized for low voltage inputs, produces 4mA output. Circuit operation is similar to the previous examples. The fundamental difference is L1's higher turns ratio, which accommodates the reduced available drive voltage. The circuit values given are typical, although some variation occurs with various lamps and layouts.

Figure 41's design, the so-called "dim backlight," is optimized for very low current lamp operation. The circuit is meant for use at low input voltages, typically 2V to 6V with a 1mA maximum lamp current. This circuit maintains control down to lamp currents of 1µA, a very dim light! It is intended for applications where the longest possible battery life is desired. Primary supply drain ranges from hundreds of microamperes to 100mA with lamp currents of microamps to 1mA. In shutdown the circuit pulls only 100µA. Maintaining high efficiency at low lamp currents requires modifying the basic design.

Achieving high efficiency at low operating current requires lowering quiescent power drain. To do this the previously employed pulse width modulator-based devices are replaced with an LT1173. The LT1173 is a Burst Mode™ operation regulator. When this device's Feedback pin is too low it delivers a burst of output current pulses, putting energy into the transformer and restoring the feedback point. The regulator maintains control by appropriately modulating the burst duty cycle. The ground referred diode at the V_{SW} pin prevents substrate turn-on due to excessive L2 ring-off.

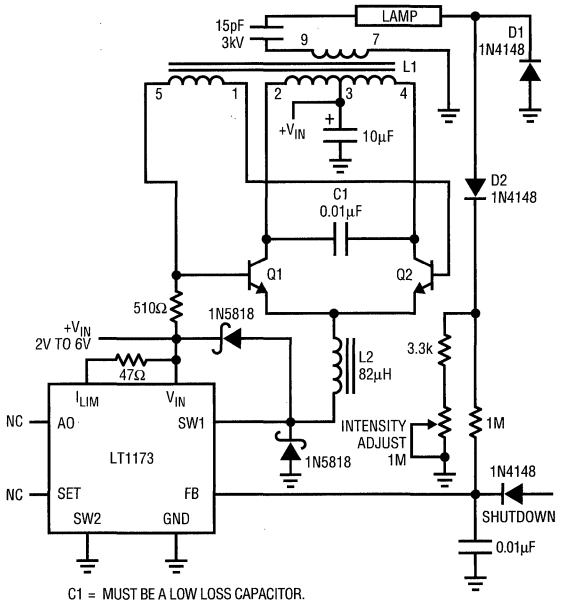
Burst Mode is a trademark of Linear Technology Corporation.



C1 = MUST BE A LOW LOSS CAPACITOR.
METALIZED POLYCARB
WIMA MKP-20 (GERMAN) OR PANASONIC ECH-U RECOMMENDED
L1 = COILTRONICS CTX110654-1
L2 = COILTRONICS CTX50-4
Q1, Q2 = ZETEX ZTX849, ZDT1048 OR ROHM 2SC5001
* = 1% FILM RESISTOR
DO NOT SUBSTITUTE COMPONENTS
COILTRONICS (407) 241-7876, SUMIDA (708) 956-0666

AN65•F40

Figure 40. A 4mA Design Intended for Low Voltage Operation. L1's Modified Turns Ratio Allows Operation Down to 3.6V



C1 = MUST BE A LOW LOSS CAPACITOR.
METALIZED POLYCARB
WIMA FKP2, MKP-20 (GERMAN) OR PANASONIC ECH-U RECOMMENDED
L1 = SUMIDA 6345-020 OR COILTRONICS CTX110092-1
PIN NUMBERS SHOWN FOR COILTRONICS UNIT
L2 = TOKO 262LYF-0091K (408) 432-8251
Q1, Q2 = ZETEX ZTX849, ZDT1048 OR ROHM 2SC5001
DO NOT SUBSTITUTE COMPONENTS

AN65•F41

Figure 41. Low Power CCFL Power Supply. Circuit Controls Lamp Current over a 1µA to 1mA Range

During the off periods the regulator is essentially shut down. This type of operation limits available output power, but cuts quiescent current losses. In contrast, the other circuit's pulse width modulator type regulators maintain "housekeeping" current between cycles. This results in more available output power but higher quiescent currents.

Figure 42 shows operating waveforms. When the regulator comes on (Trace A, Figure 42) it delivers bursts of output current to the L1/Q1/Q2 high voltage converter. The converter responds with bursts of ringing at its resonant frequency.[11] The circuit's loop operation is similar to the previous designs except that T1's drive waveform varies with supply. Because of this, line regulation suffers and the circuit is not recommended for wide ranging inputs.

Some lamps may display nonuniform light emission at very low excitation currents. See the text section, "Floating Lamp Circuits."

A CCFL power supply that addresses the previous circuit's line regulation problems and operates from 2V to 6V is detailed in Figure 43. This circuit, contributed by Steve Pietkiewicz of LTC, can drive a small CCFL over a 100µA to 2mA range.

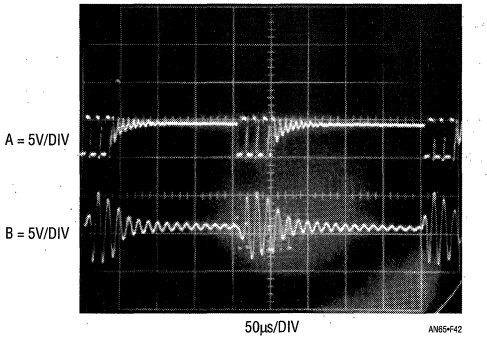


Figure 42. Waveforms for the Low Power CCFL Power Supply. LT1173 Burst Type Regulator (Trace A) Periodically Excites the Resonant High Voltage Converter (Q1 Collector Is Trace B)

Note 11. The discontinous energy delivery to the loop causes substantial jitter in the burst repetition rate, although the high voltage section maintains resonance. Unfortunately, circuit operation is in the "chop" mode region of most oscilloscopes, precluding a detailed display. "Alternate" mode operation causes waveform phasing errors, producing an inaccurate display. As such, waveform observation requires special techniques. Figure 42 was taken with a dual-beam instrument (Tektronix 556) with both beams slaved to one time base. Single sweep triggering eliminated jitter artifacts. Most oscilloscopes, whether analog or digital, will have trouble reproducing this display.

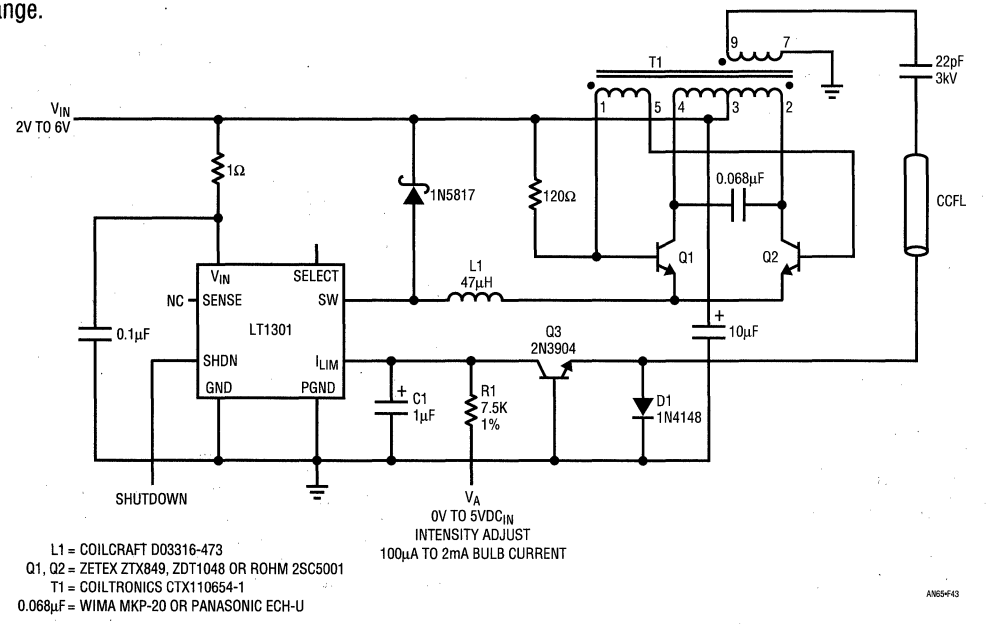


Figure 43. Low Power Cold Cathode Fluorescent Lamp Supply Is Optimized for Low Voltage Inputs and Small Lamps

The circuit uses an LT1301 micropower DC/DC converter IC in conjunction with a current driven Royer class converter comprised of T1, Q1 and Q2. When power and intensity adjust voltage are applied, the LT1301's I_{LIM} pin is driven slightly positive, causing maximum switching current through the IC's internal Switch pin (SW). Current flows from T1's center tap, through the transistors, into L1. L1's current is deposited in switched fashion to ground by the regulator's action.

Circuit efficiency ranges from 80% to 88% at full load, depending on line voltage. Current mode operation combined with the Royer's consistent waveshape vs input results in excellent line rejection. The circuit has none of the line rejection problems attributable to the hysteretic voltage control loops typically found in low voltage micropower DC/DC converters. This is an especially desirable characteristic for CCFL control, where lamp intensity must remain constant with shifts in line voltage.

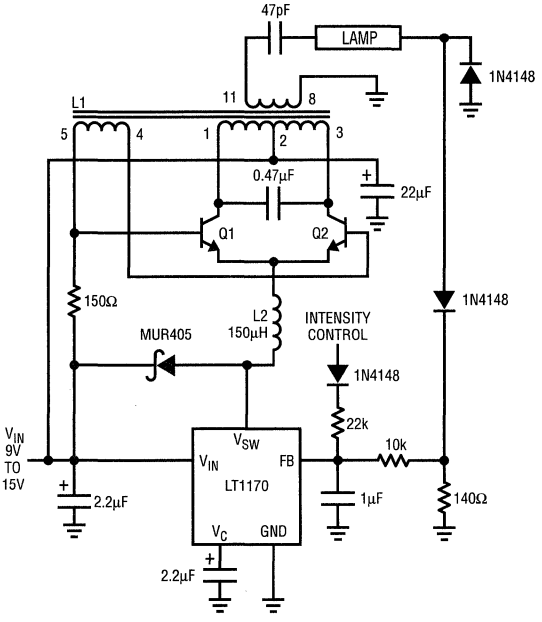
The Royer converter oscillates at a frequency primarily set by T1's characteristics (including its load) and the 0.068µF capacitor. LT1301 driven L1 sets the magnitude of the Q1/Q2 tail current, hence T1's drive level. The 1N5817 diode maintains L1's current flow when the LT1301's switch is off. The 0.068µF capacitor combines with T1's characteristics to produce sine wave voltage drive at the Q1 and Q2 collectors. T1 furnishes voltage step-up and about $1400V_{P-P}$ appears at its secondary. Alternating current flows through the 22pF capacitor into the lamp. On positive half-cycles the lamp's current is steered to ground via D1. On negative half-cycles the lamp's current flows through Q3's collector and is filtered by C1. The LT1301's I_{LIM} pin acts as a 0V summing point with about 25µA bias current flowing out of the pin into C1. The LT1301 regulates L1's current to equalize Q3's average collector current, representing 1/2 the lamp current, and R1's current, represented by V_A/R1. C1 smooths all current flow to DC. When V_A is set to zero, the I_{LIM} pin's bias current forces about 100µA bulb current.

High Power CCFL Power Supply

As mentioned, the CCFL circuit approach presented here scales quite nicely over a wide range of output power. Most circuits are in the 0.5W to 3W region due to the application's small size and battery-driven nature. Automotive, aircraft, desktop computer and other displays often require much higher power.

Figure 44's arrangement is a scaled-up version of the text's CCFL circuits. This design, similar to ones employed for automotive use, drives a 25W CCFL. There are virtually no configuration changes, although most component power ratings have increased. The transistors can handle the higher currents, but all other power components are higher capacity. Efficiency is about 80%.

Additional high power circuits appear in Appendix I, "Additional Circuits."



L1 = COILTRONICS CTX02-11128
L2 = COILTRONICS CTX150-3-52
Q1, Q2 = ZETEX ZTX849, ZDT1048 OR ROHM 2SC5001
0.47µF = WIMA 3X 0.15µF TYPE MKP-20
COILTRONICS (407) 241-7876

AN65-F44

Figure 44. A 25W CCFL Supply Is a Scaled Version of Lower Power Circuits

"Floating" Lamp Circuits

All circuits presented to this point drive the lamp in single-ended fashion. Similarly, Figure 45 shows one lamp electrode receiving drive with the other terminal essentially at ground. This causes significant loss via parasitic paths associated with the lamp's driven end. This is so because of the large voltage swing in this region. The parasitic paths near the lamp's grounded end undergo relatively little swing, contributing small energy loss. Unfortunately, the lost energy is heavily voltage-dependent ($E = 1/2\ CV^2$) and net energy loss is excessive if driven end parasitics are large. Figure 46 minimizes the losses by altering the drive scheme. In this case the lamp is driven from both ends instead of grounding one end. This "floating" lamp arrangement requires only half the voltage swing at each lamp end instead of full swing at one end. This introduces more loss in the parasitic paths previously associated with the grounded end. In most cases these increased losses are favorably offset by the reduced swing because of the V^2 loss term associated with voltage amplitude.

The advantage gained varies considerably with display type, although a 10% to 20% reduction in lost energy is common. In some displays loss reduction is not as good, and occasionally improvement is negligible. Heavily asymmetric wiring to or within the display can sometimes make floating drive more lossy than grounded drive. In such cases testing in both modes is necessary to determine which type drive is most efficient.

A second advantage of floating operation is extended illumination range. "Grounded" lamps operating at relatively low currents may display the "thermometer effect," that is, light intensity may be nonuniformly distributed along lamp length.

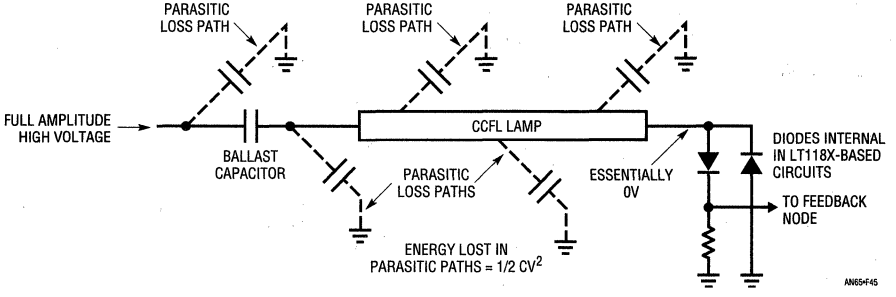


Figure 45. Ground Referred Lamp Drive Has Large Energy Loss in High Voltage Regions Due to Full Amplitude Swing

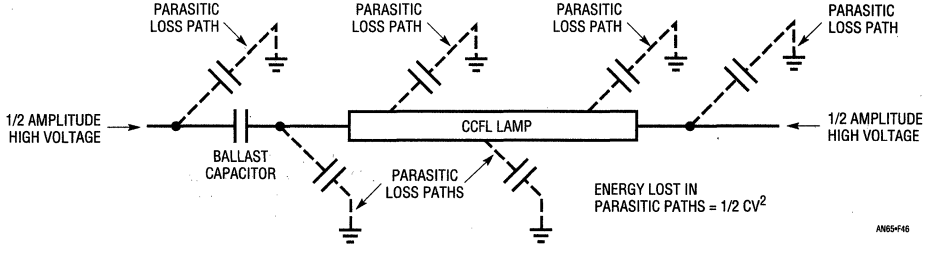


Figure 46. "Floating" Lamp Allows Reduced, Bipolar Drive, Cutting Losses Due to Parasitic Capacitance Paths. Formerly Grounded Lamp End's Paths Absorb More Energy Than Before, but Overall Loss Is Lower Due to Equation's V^2 Term

Figure 47 shows that although lamp current density is uniform, the associated field is imbalanced. The field's low intensity, combined with its imbalance, means that there is not enough energy to maintain uniform phosphor glow beyond some point. Lamps displaying the thermometer effect emit most of their light near the driven electrode, with rapid emission fall-off as distance from the electrode increases. Placing a conductor along the lamp's length largely alleviates "thermometering." The trade-off is decreased efficiency due to energy leakage.[12] It is worth noting that various lamp types have different degrees of susceptibility to the thermometer effect.

Some displays require extended illumination range. "Thermometering" usually limits the lowest practical illumination level. One acceptable way to minimize "thermometering" is to eliminate the large field imbalance. The floating drive used to reduce energy loss also provides a way to minimize "thermometering." Figure 48 reviews a

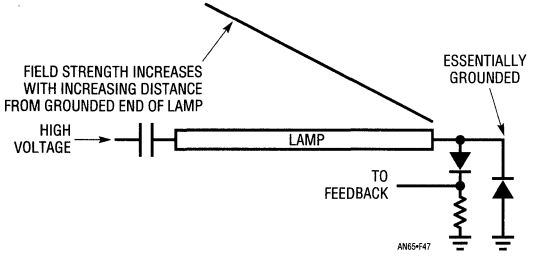


Figure 47. Field Strength vs Distance for a Ground Referred Lamp. Field Imbalance Promotes Uneven Illumination at Low Drive Levels

Note 12. A very simple experiment quite nicely demonstrates the effects of energy leakage. Grasping the lamp at its low voltage end (low field intensity) with thumb and forefinger produces almost no change in circuit input current. Sliding the thumb/forefinger combination towards the high voltage (higher field intensity) lamp end produces progressively greater input currents. Don't touch the high voltage lead or you may receive an electrical shock. Repeat: Do not touch the high voltage lead or you may receive an electrical shock.

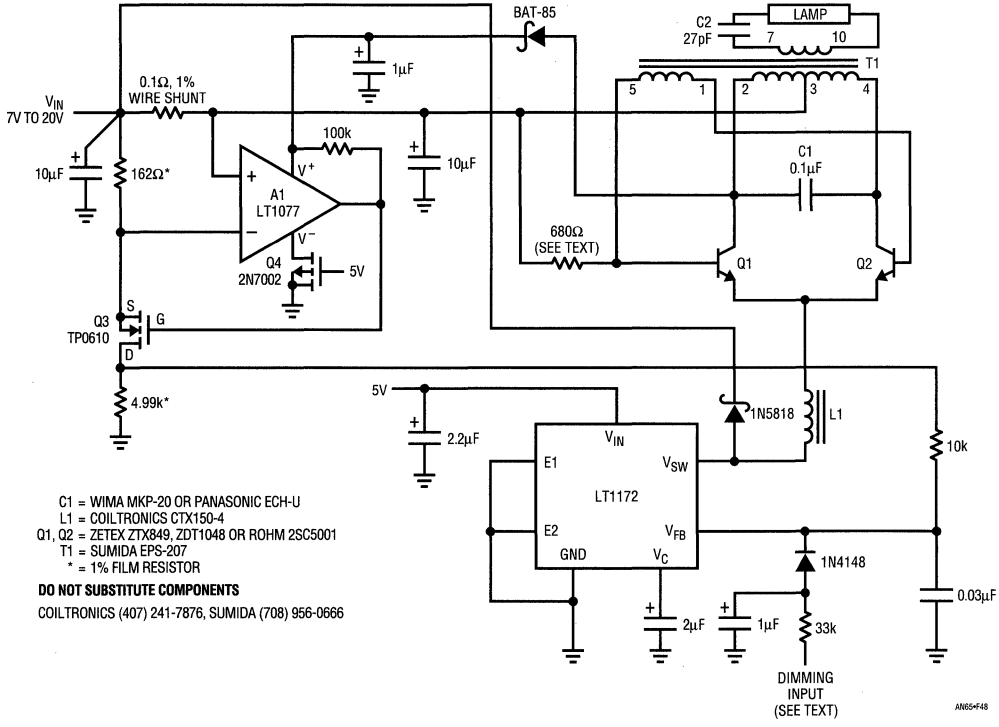


Figure 48. Practical "Floating" Lamp Drive Circuit. A1 Senses Royer Input Current with Q3 Providing Resultant Feedback Information to Switching Regulator. Circuit Reduces Lost Energy Due to Parasitics by 10% to 20%

circuit originally introduced in a previous publication.[13] The circuit's most significant aspect is that the lamp is fully floating—there is no galvanic connection to ground as in the previous designs. This allows T1 to deliver symmetric, differential drive to the lamp. Such balanced drive eliminates field imbalance, reducing thermometering at low lamp currents. This approach precludes any feedback connection to the now floating output. Maintaining closed-loop control necessitates deriving a feedback signal from some other point. In theory, lamp current proportions to T1's or L1's drive level and some form of sensing this can be used to provide feedback. In practice, parasitics make a practical implementation difficult.[14]

Figure 48 derives the feedback signal by measuring Royer converter current and feeding this information back to the LT1172. The Royer's drive requirement closely proportions to lamp current under all conditions. A1 senses this current across the 0.1Ω shunt and biases Q3, closing a local feedback loop. Q3's drain voltage presents an amplified, single-ended version of the shunt voltage to the feedback point, closing the main loop. A1's power supply pin is bootstrapped to T1's boosted swing via the BAT-85 diode, permitting it to sense across the supply-fed shunt resistor. Internal A1 characteristics ensure start-up and substitution of this device is not recommended.[15]

The lamp current is not as tightly controlled as before but 0.5% regulation over wide supply ranges is possible. The dimming in this circuit is controlled by a 1kHz PWM signal. Note the heavy filtering (33k/1µF) *outside* the feedback loop. This allows a fast time constant, minimizing turn-on overshoot.[16]

Note 13. See Reference 1.
Note 14. See Appendix L, "A Lot of Cut Off Ears and No Van Goghs—Some Not-So-Great Ideas," for details.
Note 15. See Reference 1, then don't say we didn't warn you.
Note 16. See text section, "Feedback Loop Stability Issues."

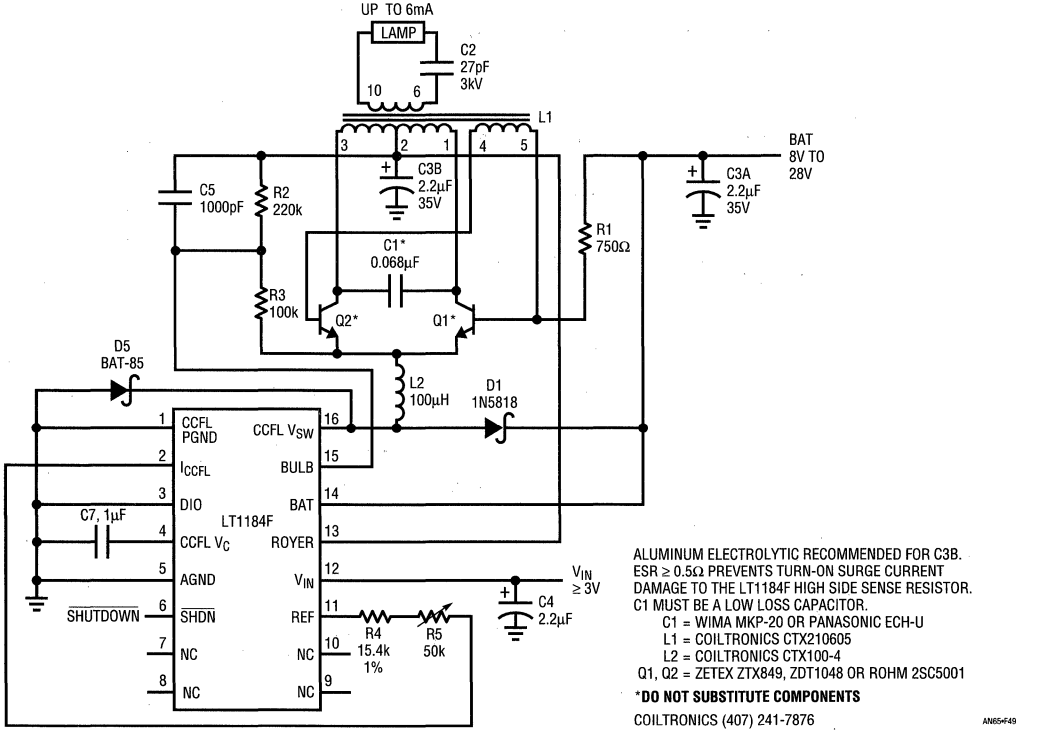


Figure 49. LT1184F IC Version of Figure 48's Floating Lamp Circuit Offers Similar Performance with Fewer Components. Open Bulb Protection and Shutdown Are Included

In all other respects operation is similar to the previous circuits. This circuit typically permits the lamp to operate with less energy loss and over a 40:1 intensity range without "thermometering." The normal feedback connection is usually limited to a 10:1 range.

IC-Based Floating Drive Circuits

Figure 49 compacts Figure 48 into a low component count, floating drive circuit. The LT1184F IC contains all functions except the Royer-based high voltage converter. The circuit also has "open lamp" protection and a 1.23V reference for biasing the dimming potentiometer.

Figure 50 adds a bipolar LCD contrast supply output to Figure 49. The LT1182 allows setting contrast supply polarity by simply grounding the appropriate output terminal. The CCFL portion is similar to the previous circuit, although intensity is controlled with a varying PWM or 0V to 5V input.

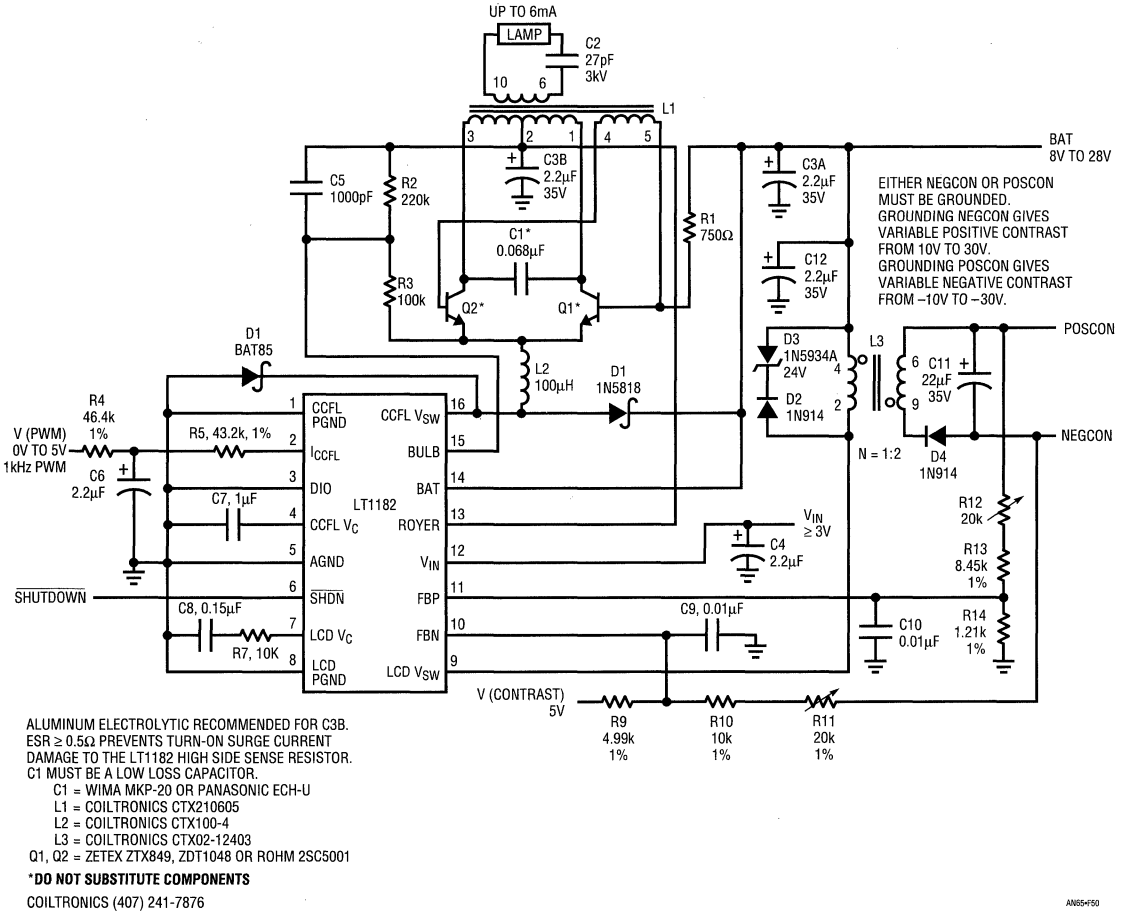


Figure 50. LT1182 Has Bipolar Output Contrast Supply in Addition to Floating Lamp Drive

Figure 51's circuit is similar, although no contrast supply is included. The LT1186 implements a floating lamp drive similar to Figure 49. This IC contains an internal D/A converter which may be addressed by accumulating a bit stream or serial protocol. Figure 52 shows a typical arrangement using an 80C31 type microcontroller. Figure 53 gives the complete software listing which was written by Tommy Wu of LTC.

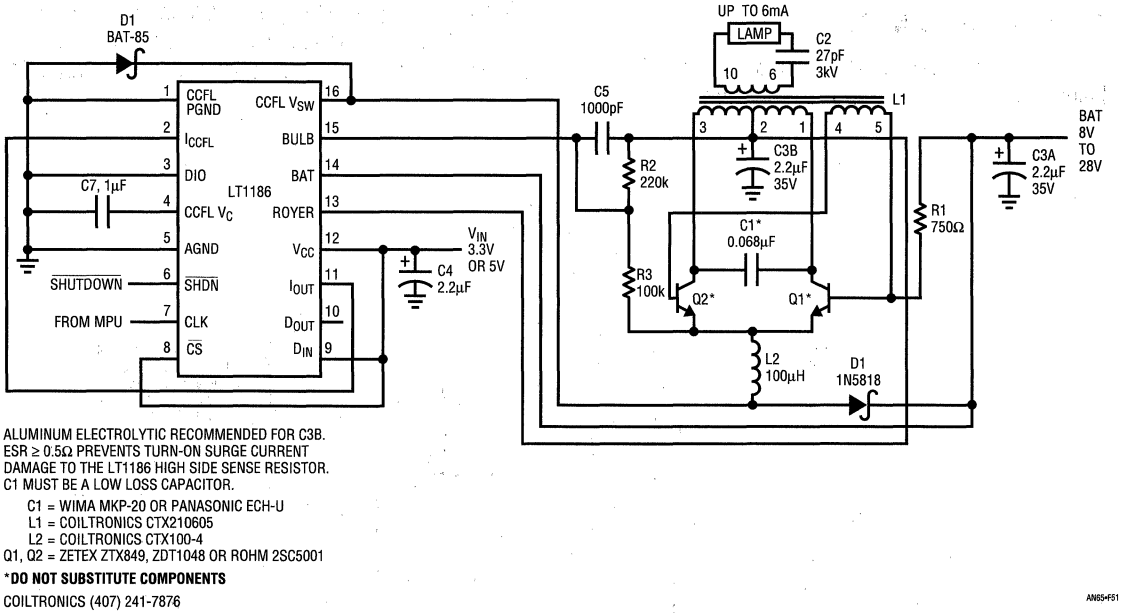


Figure 51. LT1186 Permits Serial or Bit Stream Data Addressing to Set Floating Lamp Current

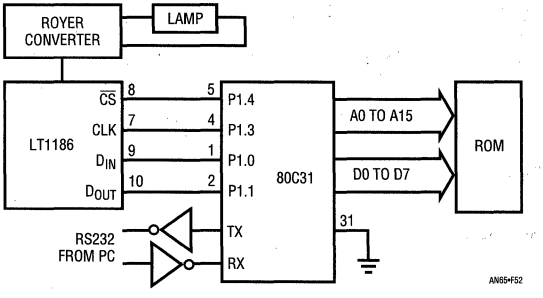


Figure 52. Typical Processor Interface for Figure 51

The LT1186 DAC algorithm is written in assembly code in a file named LT1186A.ASM as a function call from the MAIN fuction below.
Note: A user inputs an integer from 0 to 255 on a keyboard and the LT1186 adjusts the IOUT programming current to control the operating lamp current and the brightness of the LCD display.

```
#include <stdio.h>
#include <reg51.h>
#include <absacc.h>

extern char lt1186(char);  /* external assembly function in lt1186a.asm*/
sbit Clock = 0x93;

main()
{
   int number = 0;
   int LstCode;

   Clock = 0;

   TMOD = 0x20;   /* Establish serial communication 1200 baud */
   TH1 = 0xE8;
   SCON = 0x52;
   TCON = 0x69;

   while(1)    /*  Endless loop  */
   {
      printf("\nEnter any code from 0 - 255:");
      scanf("%d",&number);
      if((0>number)|(number>255))
         {
            number = 0;
            printf("The number exceeds its range. Try again!");
         }
            else
            {
               LstCode = lt1186(number);
               printf("Previous # %u",(LstCode&0xFF)); /* AND the previous number with 0xFF to turn off sign
                  extension */
            }
   number = 0;
   }
}

; The following assembly program named LT1186A.ASM receives the Din word from the main C program,
; lt1186 lt1186(). Assembly to C interface headers, declarations and memory allocations are listed before the
; actual assembly code.
;
; Port p1.4 = CS
; Port p1.3 = CLK
; Port p1.1 = Dout
; Port p1.0 = Din
;
```

Figure 53. Complete Software Listing for Figure 52's Processor Interface

```
NAME  LT1186_ CCFL
PUBLIC lt1186, ?lt1186?BYTE

?PR?ADC_INTERFACE?LT1186_CCFL SEGMENT CODE
?DT?ADC_INTERFACE?LT1186_CCFL SEGMENT  DATA

            RSEG  ?DT?ADC_INTERFACE?LT1186_CCFL
?lt1186?BYTE:  DS  2

            RSEG  ?PR?ADC_INTERFACE?LT1186_CCFL

CS      EQU   p1.4
CLK     EQU   p1.3
DOUT    EQU   p1.1
DIN     EQU   P1.0

lt1186: setb  CS              ;set CS high to initialize the LT1186
        mov   r7,?lt1186?BYTE ;move input number(Din) from keyboard to R7
        mov   p1, #01h        ;setup port p1.0 becomes input
        clr   CS              ;CS goes low, enable the DAC
        mov   a, r7           ;move the Din to accumulator
        mov   r4, #08h        ;load counter 8 counts
        clr   c               ;clear carry before rotating
        rlc   a               ;rotate left Din bit(MSB) into carry
loop:   mov   DIN, c          ;move carry bit to Din port
        setb  CLK             ;Clk goes high for LT1186 to latch Din bit
        mov   c, DOUT         ;read Dout bit into carry
        rlc   a               ;rotate left Dout bit into accumulator
        clr   CLK             ;clear clock to shift the next Dout bit
        djnz  r4, loop        ;next data bit loop
        mov   r7, a           ;move previous code to R7 as character return
        setb  CS              ;bring CS high to disable DAC
        ret
        END
```

Note: When CS goes low, the MSB of the previous code appears at Dout.

Figure 53 (continued). Complete Software Listing for Figure 52's Processor Interface

High Power Floating Lamp Circuit

High power floating lamp circuits require more current than the LT118X series can deliver. In such cases the function can be built from discrete components and ICs. Figure 54 shows a 30W CCFL circuit used in an automotive application. This 4-lamp circuit uses an LT1269 current-fed Royer converter to provide high power. Lamp current is sensed in current transformer T2. A1 and associated components form a synchronous rectifier for T2's low level output. A2 provides gain and closes a loop back at the LT1269's feedback terminal. T2's isolated sensing permits the advantages of floating operation with the LT1269 providing high power capability. This circuit has about 83% efficiency at 30W output, a wide dimming range and 0.1% line regulation.

Selection Criteria for CCFL Circuits

Selecting which CCFL circuit to use for a specific application involves numerous trade-offs. A variety of issues determine which circuit is the "best" approach. At a

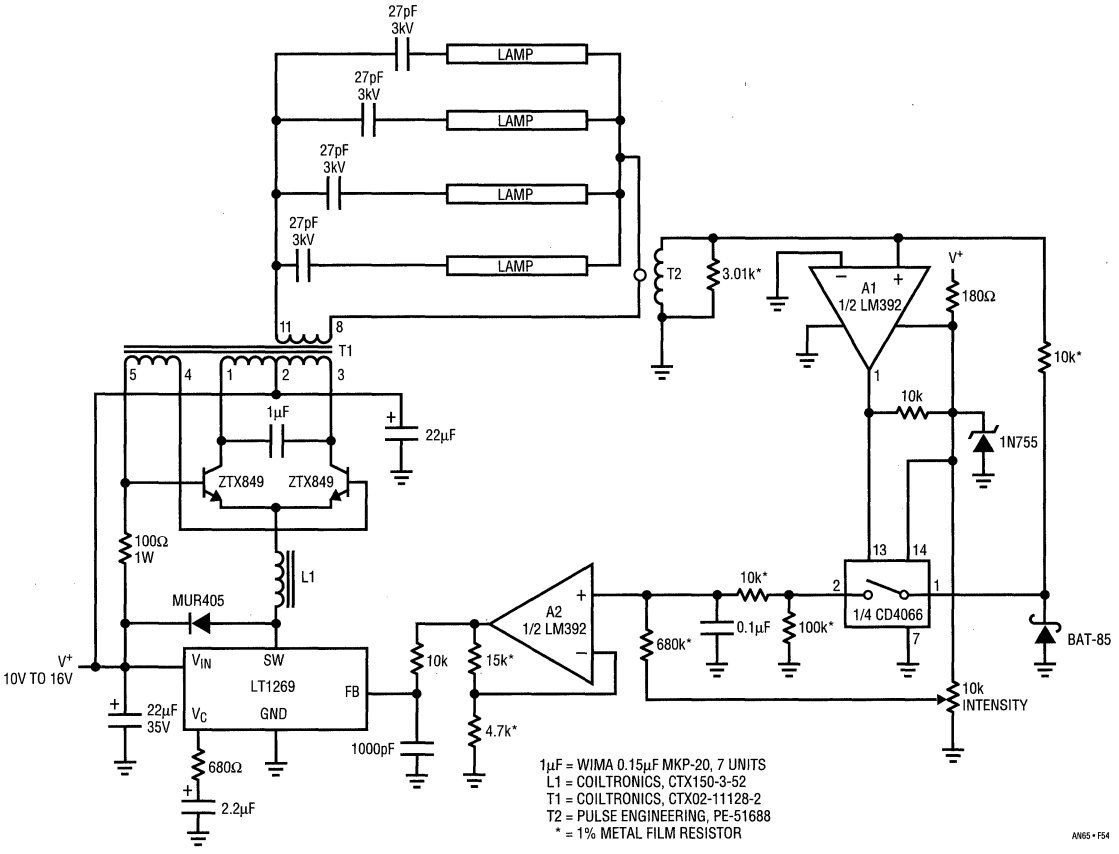


Figure 54. A High Power, Multilamp Display Using the Floating Drive Approach. Power Requirement Necessitates LT1269 Regulator and Discrete Component Approach. Floating Feedback Path Is Via Current Transformer

minimum, the user should consider the following guidelines before committing to any approach. Related discussion to all of the following topics is covered in appropriate text sections.

Display Characteristics

The display characteristics (including wiring losses) should be well-understood. Typically, display manufacturers list *lamp* requirements. These specifications are often obtained from the lamp vendor, who usually tests in free air, with no significant parasitic loss paths. This means that actual required power, start and running voltages may significantly differ from data sheet specifications. The only way to be certain of display characteristics is to measure them. The measured display energy loss can determine if a floating or grounded circuit is applicable. Low loss displays (relatively rare) usually provide better overall efficiency with grounded drive. As losses become worse (unfortunately, relatively common) floating drive becomes a better choice. Efficiency measurements may be required in both modes to determine the best choice. (See "General Optimization and Measurement Considerations.")

Operating Voltage Range

The operating voltage range includes the minimum to maximum voltages the circuit must operate from. In

battery-driven apparatus supply range can easily be 3:1, and sometimes greater. Best backlight performance is usually obtained in the 8V to 28V range. In general, potentials below 7V require some efficiency trade-offs at moderate (1.5W to 3W) power levels. Some systems reduce backlight power when running from the battery, and this can have a pronounced effect on the design. Even seemingly small (e.g., 20%) reductions in power may make painful trade-offs unnecessary. In particular, high turns ratio transformers are required to support low voltage operation at full lamp output. They work well but somewhat less efficiently than lower ratio types due to the higher peak currents characteristic of their operation. Current trends in battery technology encourage system operation at low voltages, necessitating extreme care in transformer selection and Royer circuit design.

Auxiliary Operating Voltages

Auxiliary, logic supply voltages should be used (if available) to run CCFL "housekeeping" currents, such as IC "V_{IN}" pins. This saves power. Always run switching regulators from the lowest potential available, usually 3.3V or 5V. Many systems provide these voltages in switched form, making separate shutdown lines unnecessary. Simply turning off the switching regulator's supply shuts the entire backlight circuit down.

Line Regulation

Grounded lamp circuits, by virtue of their true global feedback, provide the best line regulation. For abrupt changes, a user may notice anything beyond 1% regulation. A grounded circuit easily meets this requirement; a floating circuit usually will. Slowly changing line inputs causing excursions outside 1% are not normally a problem because they are not detectable. Rapid line changes, such as plugging in a systems AC line adapter, require good regulation to avoid annoying display flicker.

Power Requirements

The CCFL's power requirement, *including display and wiring losses*, should be well-defined over all conditions, including temperature and lamp specification variations. Usually, IC versions of floating lamp circuits are restricted to 3W to 4W output power while grounded circuit power is easily scaled.

Supply Current Profile

The backlight is often physically located far "forward" in the system. Impedances in cables, switches, traces and connectors can build up to significant levels. This means that a CCFL circuit should draw operating power continuously, rather than requiring discrete, high current "chunks" from a lossy supply line. Royer-based architectures are nearly ideal in this regard, pulling current smoothly over time and requiring no special bypassing, supply impedance or layout treatment. Similarly, Royer type circuits do not cause significant disturbances to the supply line, preventing noise injection back into the supply.

Lamp Current Certainty

The ability to predict lamp current at full intensity is important to maintain lamp life. Excessive overcurrent greatly shortens lamp life, while yielding little luminosity benefit (see Figure 2). Grounded circuits are excellent in this category with 1% usually achieved. Floating circuits are typically in the 2% to 5% range. Tight current tolerances do not benefit unit/unit display luminosity because lamp emission and display attenuation variations approach ±20% and vary over life.

Efficiency

CCFL backlight efficiency should be considered from two perspectives. The electrical efficiency is the ability of the circuit to convert DC power to high voltage AC and deliver it to the load (lamp and parasitics) with minimum loss. The optical efficiency is perhaps more meaningful to the user. It is simply the ratio of display luminosity to DC power into the CCFL circuit. The electrical and optical losses are lumped together in this measurement to produce a luminosity vs power specification. It is quite significant that *the electrical and optical peak efficiency operating points do not necessarily coincide.* This is primarily due to the lamp's emissivity dependence on waveshape. The optimum waveshape for emissivity may or may not coincide with the circuit's electrical operating peak. In fact, it is quite possible for "inefficient" circuits to produce more light than "more efficient" versions. The only way to ensure peak efficiency in a given situation is to optimize the circuit to the display.

Shutdown

System shutdown almost always requires turning off the backlight. In many cases the low voltage supply is already available in switched form. If this is so, the CCFL circuits shown go off, absorbing very little power. If switched low voltage power is not available the shutdown inputs may be used, requiring an extra control line.

Transient Response

The CCFL circuit should turn on the lamp without attendant overshoot or poor control loop settling characteristics. This can cause objectionable display flicker, and in the worst case result in transformer overstress and failure. Properly prepared floating and grounded CCFL circuits have good transient response, with LT118X-based types inherently easier to optimize.

Dimming Control

The method of dimming should be considered early in the design. All of the circuits shown can be controlled by potentiometers, DC voltages and currents, pulse width modulation or serial data protocol. A dimming scheme with high accuracy at maximum current prevents excessive lamp drive and should be employed.

Open Lamp Protection

The CCFL circuits deliver a current source output. If the lamp is broken or disconnected, compliance voltage is limited by transformer turns ratio and DC input voltage. Excessive voltages can cause arcing and resultant damage. Typically, the transformers withstand this condition but open lamp protection ensures against failures. This feature is built into the LT118X series; it must be added to other circuits.

Size

Backlight circuits usually have severe size and component count limitations. The board must fit within tightly defined dimensions. LT118X series-based circuits offer lowest component count, although board space is usually dominated by the Royer transformer. In extremely tight spaces it may be necessary to physically segment the circuit but this should be considered as a last resort.[17]

Contrast Supply Capability

Some LT118X parts provide contrast supply outputs. The other circuits do not. The LT118X's onboard contrast supply is usually an advantage but space is sometimes so restricted that it cannot be used. In such cases the contrast supply must be remotely located.

Emissions

Backlight circuits rarely cause emission problems and shielding is usually not required. Higher power versions (e.g., >5W) may require attention to meet emission requirements. The fast rise switching regulator output sometimes causes more RFI than the high voltage AC waveform. If shielding is used, its parasitic effects are part of the inverter load and optimization must be carried out with the shield in place.

Summary of Circuits

The interdependence of backlight parameters makes summarizing or rating various approaches a hazardous exercise. There is simply no intellectually responsible way to streamline the selection and design process if optimum results are desired. A meaningful choice *must* be the outcome of laboratory-based experimentation. There are just too many interdependent variables and surprises for a systematic, theoretically based selection. Pure analytics are pretty; working circuits come from the bench. Some generalizations having limited usefulness are, however, possible. Figures 55 and 56 attempt to summarize salient characteristics vs part type and may (however cautiously) be considered a beginning point.[18]

Figure 55 summarizes characteristics of all the circuits. Figure 56 focuses on the features of the LT118X series parts.

Note 17. See Appendix G, "Layout, Component and Emissions Considerations."

Note 18. Readers detecting author ambivalence about inclusion of Figures 55 and 56 are not hallucinating.

ISSUES	LT118X SERIES	LT117X SERIES	LT137X SERIES
Optical Efficiency	Grounded output versions display dependent. Floating versions usually 5% to 20% better.	Display dependent	Display dependent
Electrical Efficiency	Grounded output versions—75% to 90%, depending on supply voltage and display. Floating output versions slightly lower.	75% to 90%, depending on supply voltage and display	75% to 92%, depending on supply voltage and display
Lamp Current Certainty	1% to 2% for grounded versions, 1% to 4% for floating output types	2% maximum	2% maximum
Line Regulation	0.1% to 0.3% for grounded types, 0.5% to 6% for floating versions	0.1% to 0.3%	0.1% to 3%
Operating Voltage Range	5.3V to 30V, depending on output power, temperature range, display, etc.	4.0V to 30V, depending on output power, temperature range, display etc.	4.0V to 30V, depending on output power, temperature range, display, etc.
Power Range	0.75W to 6W typical	0.75W to 20W typical	0.5W to 6W typical
Supply Current Profile	Continuous—no high current peaks	Continuous—no high current peaks	Continuous—no high current peaks
Shutdown Control	Yes—logic compatible	Requires small FET or bipolar transistor	Yes—logic compatible
Transient Response—Overshoot	Excellent—no optimization required	Excellent—requires optimization in some cases	Excellent—requires optimization in some cases
Dimming Control	Pot., PWM, variable DC voltage or current. LT1186 has serial digital input with data storage.	Pot., PWM, variable DC voltage or current	Pot., PWM, variable DC voltage or current
Emissions	Low	Low	Low, although high power versions may require attention to layout and shielding
Open Lamp Protection	Internal to IC	Requires external small-signal transistor and some discretes at high supply voltages	Requires external small-signal transistor and some discretes at high supply voltages
Size	Low component count, small overall board footprint. 200kHz magnetics.	Small—100kHz magnetics	Small—1MHz magnetics for fastest versions
Contrast Supply Capability	Various contrast supply options available, including bipolar output	No	No

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Figure 55. Design Issues vs Typical Part Choice. Chart Makes Simplistic Assumptions and Is Intended As a Guide Only

LT1269/LT1270	LT1301	LT1173
Display dependent	Display dependent	Display dependent
75% to 90%, depending on supply voltage and display	70% to 88%, depending on supply voltage and display	65% to 75%, depending on supply voltage and display
2% maximum	2% typical	5%
0.1% to 0.3%	0.1% to 0.3%	8% to 10%
4.5V to 30V, depending on output power, temperature range, display, etc.	2V to 10V practical	2V to 6V practical
5W to 35W typical	0.02W to 1W practical	Essentially 0W to about 0.6W
Continuous—no high current peaks	Continuous—no high current peaks	Irregular—relatively high current peaking requires attention to supply rail impedance
Requires small FET or bipolar transistor	Yes—logic compatible	Logic compatible shutdown practical
Excellent—requires optimization in some cases	Excellent—no optimization required	Excellent—no optimization required
Pot., PWM, variable DC voltage or current	Pot., PWM, variable DC voltage or current	Pot., PWM, variable DC voltage or current
High power mandates attention to layout and shielding	Real low	Itsy-bitsy
Requires external small-signal transistor and some discretes at high supply voltages	Requires external small-signal tansistor and some discretes, but low supply voltages usually eliminate this consideration	None, but low supply, low power operation usually eliminates this issue
Relatively large due to high power 100kHz magnetics	Very small—low power magnetics cut size	Small—low power magnetics cut size
No	No	No

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	LT1182	LT1183	LT1184	LT1184F	LT1186
Floating Lamp Operation	Yes	Yes	No	Yes	Yes
Grounded Lamp Operation	Yes	Yes	Yes	Yes	Yes
Contrast Supply	Bipolar Contrast Outputs	Unipolar Contrast Outputs	No	No	No
Voltage Reference Available	No	Yes	Yes	Yes	No
Internal Control DAC	No	No	No	No	Yes

Figure 56. Features of Various LT118X IC Backlight Controllers

General Optimization and Measurement Considerations

Once a display/lamp combination has been picked, the appropriate circuit can be selected and optimized. "Optimization" implies maximizing performance in those areas most important in a particular application. This may involve trading off characteristics in one area to gain advantage in another. The circuit types described impose mild penalty in this regard because they are quite flexible.

A desirable characteristic is something often loosely referred to as "efficiency." There are really two types of efficiency in a backlight circuit. The *optical* efficiency measures the circuit/display combination as a transducer. It is the ratio of light output to electrical power input. This ratio lumps the converter's electrical loss with lamp and display losses. A backlight's *electrical* efficiency measures the converter's electrical input vs output power without regard to optical performance. Obviously, high electrical efficiency is required and a reliable way to measure it is desirable. More subtly, the ability to measure and manipulate purely electrical terms offers a way to influence optical efficiency. This is so because the lamp is sensitive to the drive waveform's shape. Best emissivity and lifetime are usually obtained with low crest factor, sinusoidal waveforms. The Royer circuit's transformer and capacitors can be selected to provide this characteristic for any given display/lamp combination. Doing this optimizes lamp drive but also effects the converter's electrical efficiency. This interaction between the optimum electrical and optical operating points must be accounted for to obtain best optical efficiency. The relationship is quite complex with a number of variables determining just where peak optical efficiency occurs.

Typically, optical output peaking occurs with a fairly clean, low harmonic waveform at the Royer collectors (Figure 57). This is usually the result of a relatively large resonating capacitor and a small ballast capacitor. Conversely, the converter's peak electrical efficiency point usually comes just as appreciable second harmonic appears in the Royer collector waveform (Figure 58). The peak electrical and optical efficiency points almost never coincide and optical efficiency often occurs 5% or more off the electrical efficiency peak. Happily, this very messy situation can be resolved by a relatively simple functional trim. The trimming procedure assumes transformer turns ratio and ballast capacitor values commensurate with the lowest

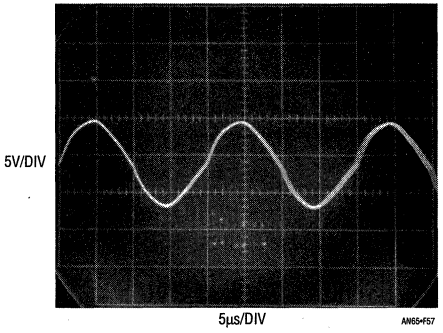

Figure 57. Typical Royer Collector Waveform at the Peak Optical Output Point. Relatively Large Resonating Capacitor May Degrade Electrical Efficiency

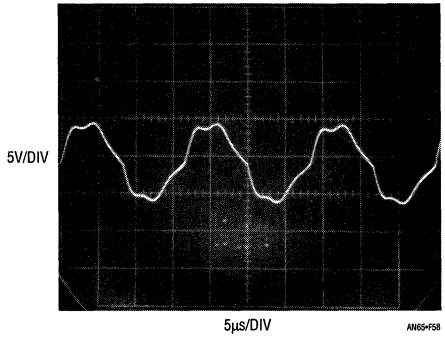

Figure 58. Typical Royer Collector Waveform at the Peak Electrical Efficiency Point. Relatively High Harmonic Content May Degrade Optical Efficiency

required circuit operating voltage have been chosen. If this factor is not considered, the optical efficiency peak will be realized but the design may not regulate at low supply voltages. Low supply voltage operation mandates high turns ratio and larger ballast capacitor values for a given display loss. If display loss is high, ballast capacitor value generally must rise to offset voltage dividing effects between it and the display's parasitic loss paths. Establish the lowest values of turns ratio and ballast capacitor that maintain regulation at minimum supply voltage before performing the trim.

Achieving peak optical efficiency involves comparing display luminosity to input power for different resonating capacitor values. For a given lamp/transformer/ ballast capacitor combination different resonating capacitors produce varying amounts of light. Large values tend to smooth harmonics, peaking optical output but increasing converter circulating losses. Smaller values promote lower circulating currents but less light output. Figure 59 shows typical results for five capacitor values at a forced 10V main supply and 5mA lamp current. Large values produce more light but require more supply current. The raw data is expressed as the ratio of light output-per-watt of input power in the right-most column. This Nits-per-Watt ratio peaks at 0.1µF, indicating the best optical efficiency.[19]

This test must be performed in a stable thermal environment because of the lamp's emission sensitivity to temperature (see Figure 3). Additionally, some arrangement for rapidly switching the capacitor values is desirable. This avoids power interruptions and the resultant long display warm-up times.

CAPACITOR (µF)	10V MAIN SUPPLY CURRENT	5V SUPPLY CURRENT	TOTAL SUPPLY WATTS	INTENSITY (NITS)	NITS/WATT
0.15	0.304	0.014	3.11	118	37.9
0.1	0.269	0.013	2.75	112	40.7
0.068	0.259	0.013	2.65	101	38.1
0.047	0.251	0.013	2.57	95	37.3
0.033	0.240	0.013	2.46	88	35.7

Note: Maintain I_{MAIN} Supply = 10.0V and I_{LAMP} = 5mA$_{RMS}$ under all conditions.

Figure 59. Typical Data Taken for Optical Efficiency Optimization. Note Emissivity Peak (Nits/Watt) for 0.1µF Resonating Value, Indicating Best Trade-Off Point for Electrical vs Optical Efficiency. Data Should Be Retaken for Several Ballast Capacitor Values to Ensure Maximum Optical Efficiency

Electrical Efficiency Optimization and Measurement

Several points should be kept in mind when observing operation of these circuits. The high voltage secondary can only be monitored with a wideband, high voltage probe fully specified for this type of measurement. *The vast majority of oscilloscope probes will break down and fail if used for this measurement.*[20] Tektronix probe types P-6007 and P-6009 (acceptable in some cases) or types P6013A and P6015 (preferred) probes must be used to read L1's output.

Another consideration involves observing waveforms. The switching regulator frequency is completely asynchronous from the Royer converter's switching. As such, most oscilloscopes cannot simultaneously trigger and display all the circuit's waveforms. Figure 36 was obtained using a dual beam oscilloscope (Tektronix 556). Traces A and B are triggered on one beam while the remaining traces are triggered on the other beam. Single beam instruments with alternate sweep and trigger switching (e.g., Tektronix 547) can also be used but are less versatile and restricted to four traces.

Obtaining and verifying high electrical efficiency[21] requires some amount of diligence. The optimum efficiency values given for C1 and C2 (C1 is the resonating capacitor and C2 is the ballast capacitor) are typical and will vary for specific types of lamps. An important realization is that the term "lamp" includes the *total* load seen by the transformer's secondary. This load, reflected back to the primary, sets transformer input impedance. The transformer's input impedance forms an integral part of the LC tank that produces the high voltage drive. Because of this, circuit efficiency must be optimized with the

Note 19. Optical measurement units are beyond arcane; a monument to obscuration. Candela/Meter^2 is a basic unit, and 1 Nit = 1 Candela/Meter^2. "Nit" is a contracted form of the Latin word "Nitere," meaning "to emit light . . . to sparkle."

Note 20. Don't say we didn't warn you!

Note 21. The term "efficiency" as used here applies to electrical efficiency. In fact, the ultimate concern centers around the efficient conversion of power supply energy into light. Unfortunately, lamp types show considerable deviation in their current-to-light conversion efficiency. Similarly, the emitted light for a given current varies over the life and history of any particular lamp. As such, this text portion treats "efficiency" on an electrical basis; the ratio of power removed from the primary supply to the power delivered to the lamp. When a lamp/display combination has been selected, the ratio of primary supply power to lamp emitted light energy may be measured with the aid of a photometer. This is covered in the immediately preceding text and Appendix D.

wiring, display housing and physical layout arranged *exactly* the same way they will be built in production. Deviations from this procedure will result in lower efficiency than might otherwise be possible. In practice, a "first cut" efficiency optimization with "best guess" lead lengths and the intended lamp in its display housing usually produces results within 5% of the achievable figure. Final values for C1 and C2 may be established when the physical layout to be used in production has been decided on. C1 sets the circuit's resonance point, which varies to some extent with the lamp's characteristic. C2 ballasts the lamp, effectively buffering its negative resistance characteristic. Small C2 values provide the most load isolation but require relatively large transformer output voltage for loop closure. Large C2 values minimize transformer output voltage but degrade load buffering. C2 values also affect waveform distortion, influencing lamp emissivity and optical efficiency (see previous text discussion). Also, C1's "best" value is somewhat dependent on the lamp type used. Both C1 and C2 must be selected for given lamp types. Some interaction occurs, but generalized guidelines are possible. Typical values for C1 are 0.01μF to 0.15μF. C2 usually ends up in the 10pF to 47pF range. C1 *must* be a low loss capacitor and substitution of the recommended devices is not recommended. A poor quality dielectric for C1 can easily degrade efficiency by 10%. Before capacitor selection the Q1/Q2 base drive resistor should be set to a value which ensures saturation, e.g., 470Ω. Next, C1 and C2 are selected by trying different values for each and iterating towards best efficiency. During this procedure ensure that loop closure is maintained. Several trials usually produce the optimum C1 and C2 values. Note that the highest efficiencies are not necessarily associated with the most esthetically pleasing waveshapes, particularly at Q1, Q2 and output. Finally, the base drive resistor's value should be optimized.

The base drive resistor's value (nominally 1k) should be selected to provide full V_{CE} saturation without inducing base overdrive or beta starvation. This point may be established for any lamp type by determining the peak collector current at full lamp power.

The base resistor should be set at the largest value that ensures saturation for worst-case transistor beta. This condition may be verified by varying the base drive resistor about the ideal value and noting small variations in input supply current. The minimum obtainable current corresponds to the best beta vs saturation trade-off. In practice, supply current rises slightly on either side of this point. This "double value" behavior is due to efficiency degradation caused by either excessive base drive or saturation losses.

Other issues influencing efficiency include lamp wire length and energy leakage from the lamp. The high voltage side(s) of the lamp should have the smallest practical lead length. Excessive length results in radiative losses which can easily reach 3% for a 3-inch wire. Similarly, no metal should contact or be in close proximity to the lamp. This prevents energy leakage which can exceed 10%.[22]

It is worth noting that a custom designed lamp affords the best possible results. A jointly tailored lamp/circuit combination permits precise optimization of circuit operation, yielding highest efficiency.

These considerations should be made with knowledge of other LCD issues. See Appendix B, "Mechanical Design Considerations for Liquid Crystal Displays." This section was guest-written by Charles L. Guthrie of Sharp Electronics Corporation.

Special attention should be given to the circuit board layout since high voltage is generated at the output. The output coupling capacitor must be carefully located to minimize leakage paths on the circuit board. A slot in the board will further minimize leakage. Such leakage can permit current flow outside the feedback loop, wasting power. In the worst case, long term contamination buildup can increase leakage inside the loop, resulting in starved lamp drive or destructive arcing. It is good practice for minimization of leakage to break the silk screen line which outlines the transformer. This prevents leakage from the

Note 22. This footnote annotates similar issues raised in Footnote 12 and associated text. The repetition is based on the necessity for emphasis. A very simple experiment quite nicely demonstrates the effects of energy leakage. Grasping the lamp at its low voltage end (low field intensity) with thumb and forefinger produces almost no change in circuit input current. Sliding the thumb/forefinger combination towards the high voltage (higher field intensity) lamp end produces progressively greater input currents. Don't touch the high voltage lead or your may receive an electrical shock. Repeat: Do not touch the high voltage lead or you may receive an electrical shock.

high voltage secondary to the primary. Another technique for minimizing leakage is to evaluate and specify the silk screen ink for its ability to withstand high voltages. Appendix G, "Layout, Component and Emissions Considerations," details high voltage layout practice.

Electrical Efficiency Measurement

Once these procedures have been followed efficiency can be measured. Efficiency may be measured by determining lamp current and voltage. Measuring current involves utilization of a wideband, high accuracy clip-on current probe having a true (thermally based) RMS readout. No commercially manufactured current probe will meet the accuracy and bandwidth requirements and the probe must be constructed.[23]

Lamp RMS voltage is measured at the lamp with a wideband, properly compensated high voltage probe.[24] Multiplying these two results gives power in watts, which may be compared to the DC input supply (E)(I) product. In practice, the lamp's current and voltage contain small out-of-phase components but their error contribution is negligible.

Both the current and voltage measurements require a wideband true RMS voltmeter. The meter must employ a thermal type RMS converter—the more common logarithmic computing type-based instruments are inappropriate because their bandwidth is too low.

The previously recommended high voltage probes are designed to see a 1MΩ/10pF-22pF oscilloscope input. The RMS voltmeters have a 10MΩ input. This difference necessitates an impedance matching network between the probe and the voltmeter. Floating lamp circuits require this matching and differential measurement, severely complicating instrumentation design. See Footnote 24.

Feedback Loop Stability Issues

The circuits shown to this point rely on closed-loop feedback to maintain the operating point. All linear closed-loop systems require some form of frequency compensation to achieve dynamic stability. Circuits operating with relatively low power lamps may be frequency compensated by simply overdamping the loop. Text Figures 35, 37 and 38 use this approach. The higher power operation associated with color displays requires more attention to loop response. The transformer produces much higher output voltages, particularly at start-up. Poor loop damping can allow transformer voltage ratings to be exceeded, causing arcing and failure. As such, higher power designs may require optimization of transient response characteristics. LT118X series parts almost never require optimization because their error amplifier's gain/phase characteristics are specially tailored to CCFL load characteristics. The LT1172, LT1372 and other general purpose switching regulators require more attention to ensure proper behavior. The following discussion, applicable to general purpose LTC switching regulators in CCFL applications, uses the LT1172 as an example.

Figure 60 shows the significant contributors to loop transmission in these circuits. The resonant Royer converter delivers information at about 50kHz to the lamp. This information is smoothed by the RC averaging time constant and delivered to the LT1172's feedback terminal as

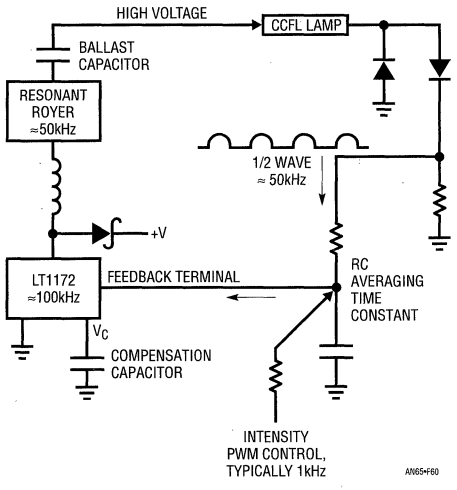

Figure 60. Delay Terms in the Feedback Path. The RC Time Constant Dominates Loop Transmission Delay and Must Be Compensated for Stable Operation

Note 23. Justification for this requirement and construction details appear in Appendix C, "Achieving Meaningful Electrical Measurements."
Note 24. Measuring floating lamp circuit voltages is a particularly demanding exercise requiring a wideband differential high voltage probe. Probe construction details appear in Appendix C.

DC. The LT1172 controls the Royer converter at a 100kHz rate, closing the control loop. The capacitor at the LT1172 rolls off gain, nominally stabilizing the loop. This compensation capacitor must roll off the gain-bandwidth at a low enough value to prevent the various loop delays from causing oscillation.

Which of these delays is the most significant? From a stability viewpoint the LT1172's output repetition rate and the Royer's oscillation frequency are sampled data systems. Their information delivery rate is far above the RC averaging time constants delay and is not significant. The RC time constant is the major contributor to loop delay. This time constant must be large enough to turn the half wave rectified waveform into DC. It also must be large enough to average any intensity control PWM signal to DC. Typically, these PWM intensity control signals come in at a 1kHz rate (see Appendix F, "Intensity Control and Shutdown Methods"). The RC's resultant delay dominates loop transmission. It must be compensated by the capacitor at the LT1172. A large enough value for this capacitor rolls off loop gain at low enough frequency to provide stability. The loop simply does not have enough gain to oscillate at a frequency commensurate with the RC delay.[25]

This form of compensation is simple and effective. It ensures stability over a wide range of operating conditions. It does, however, have poorly damped response at system turn-on. At turn-on the RC lag delays feedback, allowing output excursions well above the normal operating point. When the RC acquires the feedback value the loop stabilizes properly. This turn-on overshoot is not a concern if it is well within transformer breakdown ratings. Color displays, running at higher power, usually require large initial voltages. If loop damping is poor, the overshoot may be dangerously high. Figure 61 shows such a loop responding to turn-on. In this case the RC values are 10k and 4.7µF, with a 2µF compensation capacitor. Turn-on overshoot exceeds 3500V for over 10ms! Ring-off takes over 100ms before settling occurs. Additionally, an inadequate (too small) ballast capacitor and excessively lossy layout force a 2000V output once loop settling occurs. This photo was taken with a transformer rated well below this figure. The resultant arcing caused transformer destruction, resulting in field failures. A typical destroyed transfomer appears in Figure 62.

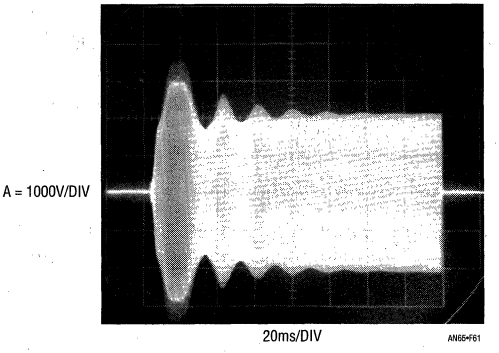

Figure 61. Destructive High Voltage Overshoot and Ring-Off Due to Poor Loop Compensation. Transformer Failure and Field Recall Are Nearly Certain. Job Loss May also Occur

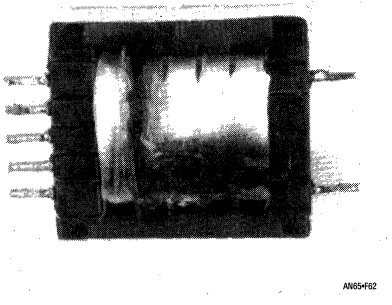

Figure 62. Poor Loop Compensation Caused This Transformer Failure. Arc Occured in High Voltage Secondary (Lower Right). Resultant Shorted Turns Caused Overheating

Figure 63 shows the same circuit with the RC values reduced to 10k and 1µF. The ballast capacitor and layout have also been optimized. Figure 63 shows peak voltage reduced to 2.2kV with duration down to about 2ms (note horizontal scale change). Ring-off is also much quicker with lower amplitude excursion. Increased ballast capacitor value and wiring layout optimization reduce running voltage to 1300V. Figure 64's results are even better. Changing the compensation capacitor to a 3kΩ/2µF network introduces a leading response into the loop, allowing faster acquisition. Now, turn-on excursion is slightly lower, but greatly reduced in duration (again, note horizontal scale change). The running voltage remains the same.

Note 25. The high priests of feedback refer to this as "Dominant Pole Compensation." The rest of us are reduced to more pedestrian descriptives.

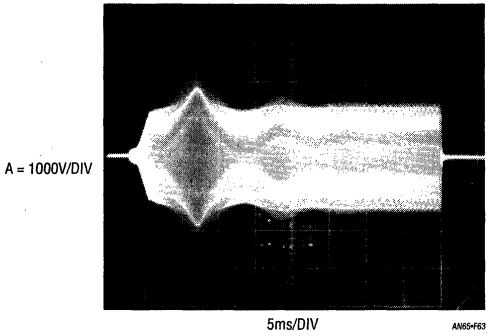

Figure 63. Reducing RC Time Constant Improves Transient Response, Although Peaking, Ring-Off and Run Voltage Are Still Excessive

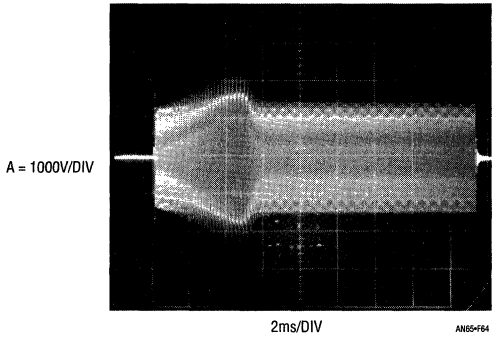

Figure 64. Additional Optimization of RC Time Constant and Compensation Capacitor Reduces Turn-On Transient. Run Voltage Is Large, Indicating Possible Lossy Layout and Display

The photos show that changes in compensation, ballast value and layout result in dramatic reductions in overshoot amplitude and duration. Figure 62's performance almost guarantees field failures while Figures 63 and 64 do not overstress the transformer. Even with the improvements, more margin is possible if display losses can be controlled. Figures 62, 63 and 64 were taken with an exceptionally lossy display. The metal enclosure was very close to the metallic foil wrapped lamp, causing large losses with subsequent high turn-on and running voltages. If the display is selected for lower losses, performance can be greatly improved.

Figure 65 shows a low loss display responding to turn-on with a 2µF compensation capacitor and 10k/1µF RC values. Trace A is the transformer's output while Traces B and C are the LT1172's $V_{COMPENSATION}$ and Feedback pins, respectively. The output overshoots and rings badly, peaking to about 3000V. This activity is reflected by overshoots at the $V_{COMPENSATION}$ pin (the LT1172's error amplifier output) and the Feedback pin. In Figure 66 the RC is reduced to 10kΩ/0.1µF. This substantially reduces loop delay. Overshoot goes down to only 800V—a reduction of almost a factor of four. Duration is also much shorter.

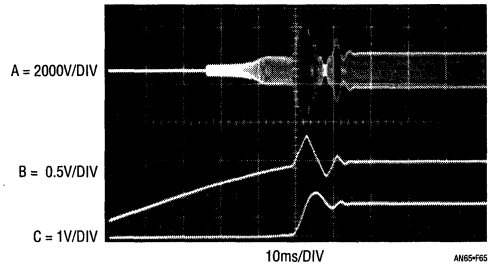

Figure 65. Waveform for a Lower Loss Layout and Display. High Voltage Overshoot (Trace A) Is Reflected at Compensation Node (Trace B) and Feedback Pin (Trace C)

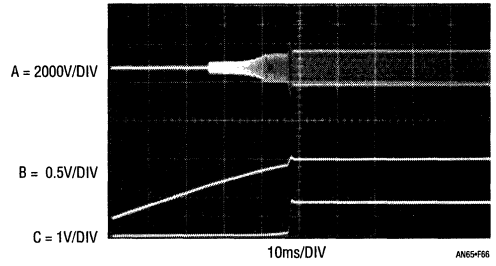

Figure 66. Reducing RC Time Constant Produces Quick, Clean Loop Behavior. Low Loss Layout and Display Result in 650V_{RMS} Running Voltage

The $V_{COMPENSATION}$ and Feedback pins reflect this tighter control. Damping is much better, with slight overshoot induced at turn-on. Further reduction of the RC to 10kΩ/0.01μF (Figure 67) results in even faster loop capture but a new problem appears. In Trace A lamp turn-on is so fast the overshoot does not register in the photo. The $V_{COMPENSATION}$ (Trace B) and feedback nodes (Trace C) reflect this with exceptionally fast response. Unfortunately, the RC's light filtering causes ripple to appear when the feedback node settles. As such, Figure 66's RC values are probably more realistic for this situation.

The lesson from this exercise is clear. The higher voltages involved in color displays mandate attention to transformer outputs. Under running conditions layout and display losses can cause higher loop compliance voltages, degrading efficiency and stressing the transformer. At turn-on improper compensation causes huge overshoots, resulting in possible transformer destruction. Isn't a day of loop and layout optimization worth a field recall?

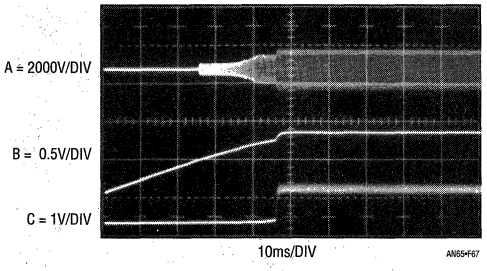

Figure 67. Very Low RC Value Provides Even Faster Response, but Ripple at Feedback Pin (Trace C) Is Too High. Figure 66 Is the Best Compromise

REFERENCES

1. Williams, J., "Techniques for 92% Efficient LCD Illumination," Linear Technology Corporation, Application Note 55, August 1993.
2. Bright, Pittman and Royer, "Transistors As On-Off Switches in Saturable Core Circuits," Electrical Manufacturing, December 1954. Available from Technomic Publishing, Lancaster, PA.
3. Sharp Corporation, "Flat Panel Displays," 1991.
4. C. Kitchen, L. Counts, "RMS-to-DC Conversion Guide," Analog Devices, Inc., 1986.
5. Williams, Jim, "A Monolithic IC for 100MHz RMS-DC Conversion," Linear Technology Corporation, Application Note 22, September 1987.
6. Hewlett-Packard, "1968 Instrumentation. Electronic-Analytical-Medical," AC Voltage Measurement, p. 197-198, 1968.
7. Hewlett-Packard, "Model 3400RMS Voltmeter Operating and Service Manual," 1965.
8. Hewlett-Packard, "Model 3403C True RMS Voltmeter Operating and Service Manual," 1973.
9. Ott, W.E., "A New Technique of Thermal RMS Measurement," IEEE Journal of Solid State Circuits, December 1974.
10. Williams, J.M. and Longman, T.L., "A 25MHz Thermally Based RMS-DC Converter," 1986 IEEE ISSCC Digest of Technical Papers.
11. O'Neill, P.M., "A Monolithic Thermal Converter," H.P. Journal, May 1980.
12. Williams, J., "Thermal Techniques in Measurement and Control Circuitry," "50MHz Thermal RMS-DC Converter," Linear Technology Corporation, Application Note 5, December 1984.
13. Williams, J. and Huffman, B., "Some Thoughts on DC-DC Converters," Appendix A, "The +5 to ±15V Converter—A Special Case," Linear Technology Corporation, Application Note 29, October 1988.
14. Baxendall, P.J., "Transistor Sine-Wave LC Oscillators," British Journal of IEEE, February 1960, Paper No. 2978E.
15. Williams, J., "Temperature Controlling to Microdegrees," Massachusetts Institute of Technology, Education Research Center, 1971 (out of print).
16. Fulton, S.P., "The Thermal Enzyme Probe," Thesis, Massachusetts Institute of Technology, 1975.
17. Williams, J., "Designer's Guide to Temperature Measurement," Part II, EDN, May 20, 1977.
18. Williams, J., "Illumination Circuitry for Liquid Crystal Displays," Linear Technology Corporation, Application Note 49, August 1992.
19. Olsen, J.V., "A High Stability Temperature Controlled Oven," Thesis, Massachusetts Institute of Technology, 1974.
20. "The Ultimate Oven," MIT Reports on Research, March 1972.
21. McDermott, James, "Test System at MIT Controls Temperature to Microdegrees," Electronic Design, January 6, 1972.
22. McAbel, Walter, "Probe Measurements," Tektronix, Inc. Concept Series, 1969.
23. Weber, Joe, "Oscilloscope Probe Circuits," Tektronix, Inc. Concept Series, 1969.
24. Tektronix, Inc., "P6015 High Voltage Probe Operating Manual."
25. Williams, Jim, "Measurement and Control Circuit Collection," Linear Technology Corporation, Application Note 45, June 1991.
26. Williams, J., "High Speed Amplifier Techniques," Linear Technology Corporation, Applicaton Note 47, August 1991.
27. Williams, J., "Practical Circuitry for Measurement and Control Problems," Linear Technology Corporation, Application Note 61, August 1994.
28. Chadderton, Neil, "Transistor Considerations for LCD Backlighting," Zetex plc. Application Note 14, February 1995.

APPENDIX A

"HOT" CATHODE FLUORESCENT LAMPS

Many CCFL characteristics are shared by so-called "Hot" Cathode Fluorescent Lamps (HCFLs). The most significant difference is that HCFLs contain filaments at each end of the lamp (see Figure A1). When the filaments are powered they emit electrons, lowering the lamp's ionization potential. This means a significantly lower voltage will start the lamp. Typically, the filaments are turned on, a relatively modest voltage impressed across the lamp and start-up occurs. Once the lamp starts, filament power is removed. Although HCFLs reduce the high voltage requirement they require a filament supply and sequencing circuitry. The CCFL circuits shown in the text will start and run HCFLs without using the filaments. In practice, this involves simply driving the filament connections at the HCFL ends as if they were CCFL electrodes.

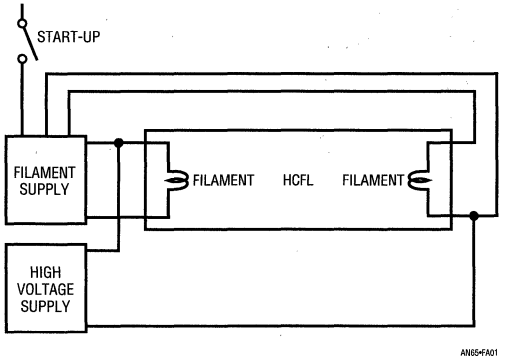

Figure A1. A Conceptual Hot Cathode Fluorescent Lamp Power Supply. Heated Filaments Liberate Electrons, Lowering the Lamp's Start-Up Voltage Requirement. CCFL Supply Discussed in Text Eliminates Filament Supply

APPENDIX B

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MECHANICAL DESIGN CONSIDERATIONS FOR LIQUID CRYSTAL DISPLAYS

Charles L. Guthrie, Sharp Electronics Corporation

Introduction

As more companies begin the manufacturing of their next generation of computers, there is a need to reduce the overall size and weight of the units to improve their portability. This has sparked the need for more compact designs where the various components are placed in closer proximity, thus making them more susceptible to interaction from signal noise and heat dissipation. The following is a summary of guidelines for the placement of the display components and suggestions for overcoming difficult design constraints associated with component placement.

In notebook computers the thickness of the display housing is important. The design usually requires the display to be in a pivotal structure so that the display may be folded down over the keyboard for transportation. Also, the outline dimensions must be minimal so that the package will remain as compact as possible. These two constraints drive the display housing design and placement of the display components. This discussion surveys each of the problems facing the designer in detail and offers suggestions for overcoming the difficulties to provide a reliable assembly.

The problems facing the pen-based computer designer are similar to those realized in notebook designs. In addition, however, pen-based designs require protection for the face of the display. In pen-based applications, as the pen is moved across the surface of the display, the pen has the potential for scratching the front polarizer. For this reason the front of the display must be protected. Methods for protecting the display face while minimizing effects on the display image are given.

Additionally, the need to specify the flatness of the bezel is discussed. Suggestions for acceptable construction techniques for sound design are included. Further, display components likely to cause problems due to heat buildup are identified and methods for minimization of the heat's effects are presented.

The ideas expressed here are not the only solutions to the various problems and have not been assessed as to whether they may infringe on any patents issued or applied for.

Flatness and Rigidity of the Bezel

In the notebook computer the bezel has several distinct functions. It houses the display, the inverter for the backlight, and in some instances, the controls for contrast and brightness of the display. The bezel is usually designed to tilt to set the optimum viewing angle for the display.

It is important to understand that the bezel must provide a mechanism to keep the display flat, particularly at the mounting holds. Subtle changes in flatness place uneven stress on the glass which can cause variations in contrast across the display. Slight changes in pressure may cause significant variation in the display contrast. Also, at the extreme, significantly uneven pressures can cause the display glass to fail.

Because the bezel must be functional in maintaining the flatness of the display, consideration must be made for the strength of the bezel. Care must be taken to provide structural members while minimizing the weight of the unit. This may be executed using a parallel grid, normal to the edges of the bezel, or angled about 45° off of the edges of the bezel. The angled structure may be more desirable in that it provides resistance to torquing the unit while lifting the cover with one hand. Again, the display is sensitive to stresses from uneven pressure on the display housing.

Another structure which will provide excellent rigidity, but adds more weight to the computer, is a "honeycomb" structure. This "honeycomb" structure resists torquing from all directions and tends to provide the best protection for the display.

With each of these structures it is easy to provide mounting assemblies for the display. "Blind nuts" can be molded into the housing. The mounting may be done to either the front or rear of the bezel. Attachment to the rear may provide better rigidity for placement of the mounting hardware.

One last caution is worth noting in the development of a bezel. The bezel should be engineered to absorb most of the shock and vibration experienced in a portable computer. Even though the display has been carefully designed, the notebook computer presents extraordinary shock and abuse problems.

Avoiding Heat Buildup in the Display

Several of the display components are sources for heat problems. Thermal management must be taken into account in the design of the display bezel. A heated display may be adversely affected; a loss of contrast uniformity usually results. The Cold Cathode Fluorescent Tube (CCFT) itself gives off a small amount of heat relative to the amount of power dissipated in its glow discharge. Likewise, even though the inverters are designed to be extremely efficient, there is some heat generated. The buildup of heat in these components will be aggravated by the typically "tight" designs currently being introduced. There is little ventilation designed into most display bezels. To compound the problem, the plastics used are poor thermal conductors, thus causing the heat to build up which may affect the display.

Some current designs suffer from poor placement of the inverter and/or poor thermal management techniques. These designs can be improved even where redesign of the display housing with improved thermal management is impractical.

One of the most common mistakes in current designs is that there has been no consideration for the buildup of heat from the CCFT. Typically, the displays for notebook applications have only one CCFT to minimize display power requirements. The lamp is usually placed along the right edge of the display. Since the lamp is placed very close to the display glass, it can cause a temperature rise in the liquid crystal. It is important to note that variations in temperature of as little as 5°C can cause an apparent nonuniformity in display contrast. Variations caused by slightly higher temperature variations will cause objectionable variations in the contrast and display appearance.

To further aggravate the situation, some designs have the inverter placed in the bottom of the bezel. This has a tendency to cause the same variations in contrast, particularly when the housing does not have any heat sinking for the inverter. This problem manifests itself as a "blooming" of the display, just above the inverter. This "blooming"

looks like a washed out area where, in the worst case, the characters on the display fade completely.

The following section discusses the recommended methods for overcoming these design problems.

Placement of the Display Components

One of the things that can be done is to design the inverter into the base of the computer with the motherboard. In some applications this is impractical because this requires the high voltage leads to be mounted within the hinges connecting the display bezel to the main body. This causes a problem with strain relief of the high voltage leads and thus with UL certification.

One mistake made most often is placing the inverter at the bottom of the bezel next to the lower edge of the display. It is a fact that heat rises, yet this is one of the most overlooked problems in new notebook designs. Even though the inverters are very efficient, some energy is lost in the inverter in the form of heat. Because of the insulating properties of the plastic materials used in the bezel construction, heat builds up and affects the display contrast.

Designs with the inverter at the bottom can be improved in one of three ways. The inverter can be relocated away from the display, heat sinking materials can be placed between the display and the inverter, or ventilation can be provided to remove the heat.

In mature designs it may be impractical to do what is obvious and move the inverter up to the side of the display towards the top of the housing. In these cases the inverter may be insulated from the display with a "heat dam." One method of accomplishing this would be to use a piece of mica insulator die cut to fit tightly between the inverter and the display. This heat dam would divert the heat around the end of the display bezel to rise harmlessly to the top of the housing. Mica is recommended in this application because of its thermal and electrical insulation properties.

The last suggestion for removing heat is to provide some ventilation to the inverter area. This has to be done very carefully to prevent exposing the high voltage. Ventilation may not be a practical solution because resistance to liquids and dust is compromised.

The best solution for the designer of new hardware is to consider the placement of the inverter to the side of the display and at the top of the bezel. In existing designs of this type the effects of heat from the inverter, even in tight housings, has been minimal or nonexistent.

One problem which is aggravated by the placement of the inverter at the bezel is heat dissipated by the CCFT. In designs where the inverter is placed up and to the side of the display, fading of the display contrast due to CCFT heat is not a problem. However, when the inverter is placed at the bezel bottom, some designs experience a loss of contrast aggravated by the heat from the CCFT and inverter.

In cases where the inverter must be left at the bottom, and the CCFT is causing a loss of contrast, the problem can be minimized by using an aluminum foil heat sink. This does not remove the heat from the display but dissipates it over the entire display area, thus normalizing the display contrast. The aluminum foil is easy to install and in some present designs has successfully improved the display contrast.

Remember that the objection to the contrast variation stems more from nonuniformity than from a total loss of contrast.

Protecting the Face of the Display

One of the last considerations in the design of notebook and pen-based computers is protection of the display face. The front polarizer is made of a mylar base and thus is susceptible to scratching. The front protection for the display, along with providing scratch protection, may also provide an antiglare surface.

There are several ways that scratch resistance and antiglare surfaces can be incorporated. A glass or plastic cover may be placed over the display, thus providing protection. The material should be placed as close to the display as possible to minimize possible parallax problems due to reflections off of the cover material. With antiglare materials the further the material is from the front of the display the greater the distortion.

In pen applications, the front antiscratch material is best placed in contact with the front glass of the display. The cover glass material normally needs to be slightly thicker

to protect the display from distortion when pressure is being exerted on the front.

There are several methods for making the pen input devices. Some use the front surface of the cover glass to provide input data and some use a field effect to a printed wiring board on the back of the display. When the pen input is on the front of the display, the input device is usually on a glass surface.

To limit specular reflection in this application, the front cover glass should be bonded to the display. Care must be taken to ensure that the coefficient of thermal expansion is matched for all of the materials used in the system. Because of the difficulties encountered with the bonding of the cover glass, and the potential to destroy the display through improper workmanship, consulting an expert is strongly recommended.

APPENDIX C

ACHIEVING MEANINGFUL ELECTRICAL MEASUREMENTS

Obtaining reliable efficiency data for the CCFL circuits presents a high order difficulty measurement problem. The accuracy required in the high frequency AC measurements is uncomfortably close to the state-of-the-art. Establishing and maintaining accurate wideband AC measurements is a textbook example of attention to measurement technique. The combination of high frequency, harmonic laden waveforms and high voltage makes meaningful results difficult to obtain. The choice, understanding and use of test instrumentation is crucial. Clear thinking is needed to avoid unpleasant surprises![1]

The lamp's current and voltage waveforms contain energy content over a wide frequency range. Most of this energy is concentrated at the inverter's fundamental frequency and immediate harmonics. However, if 1% measurement uncertainty is desirable, then energy content out to 10MHz must be accurately captured. Figure C1, a spectrum analysis of lamp current, shows significant energy out to 500kHz. Diminished, but still significant, content shows

Note 1: It is worth considering that various constructors of text Figure 35 have reported efficiencies ranging from 8% to 115%.

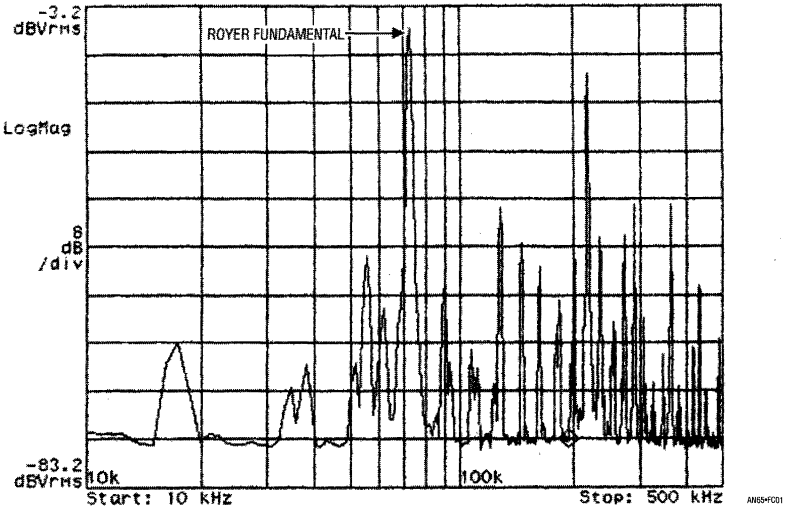

Figure C1. Hewlett-Packard HP89410A Spectral Plot of Lamp Current Shows Significant Energy Out to 500kHz

up in Figure C2's 6MHz wide plot. This data suggests that monitoring instrumentation must maintain high accuracy over wide bandwidth.

Accurate determination of RMS operating current is important for electrical and emissivity efficiency computations and to ensure long lamp life. Additionally, it is desirable to be able to perform current measurements in the presence of high common mode voltage (>1000V_{RMS}). This capability allows investigation and quantification of display and wiring-induced losses, regardless of their origins in the lamp drive circuitry.

Current Probe Circuitry

Figure C3's circuitry meets the discussed requirements. It signal-conditions a commercially available "clip-on" current probe with a precision amplifier to provide 1% measurement accuracy to 10MHz. The "clip-on" probe provides convenience, even in the presence of the high common voltages noted. The current probe biases A1, operating at a gain of about 3.75. No impedance matching is required due to the probe's low output impedance termination. Additional amplifiers provide distributed gain, maintaining wide bandwidth with an overall gain of about

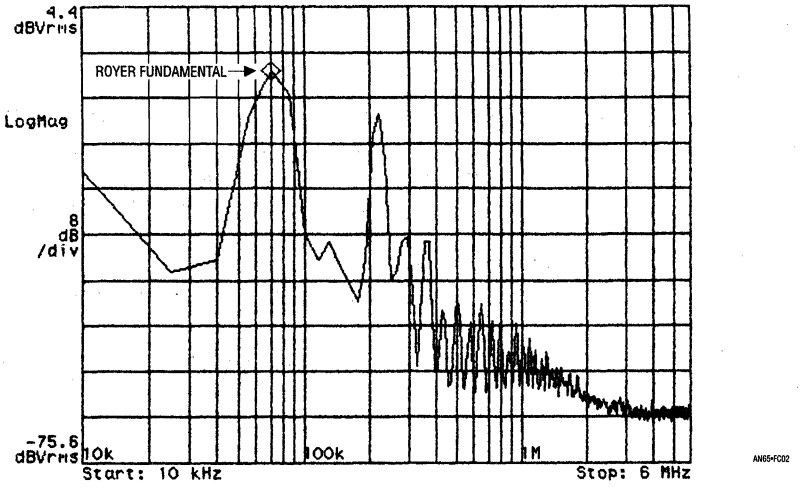

Figure C2. Extended HP89410A Spectral Plot Shows Lamp Current Has Measurable Energy Well into MHz Range. Data Indicates that Lamp Voltage and Current Instrumentation Must Have Precision, Wideband Response

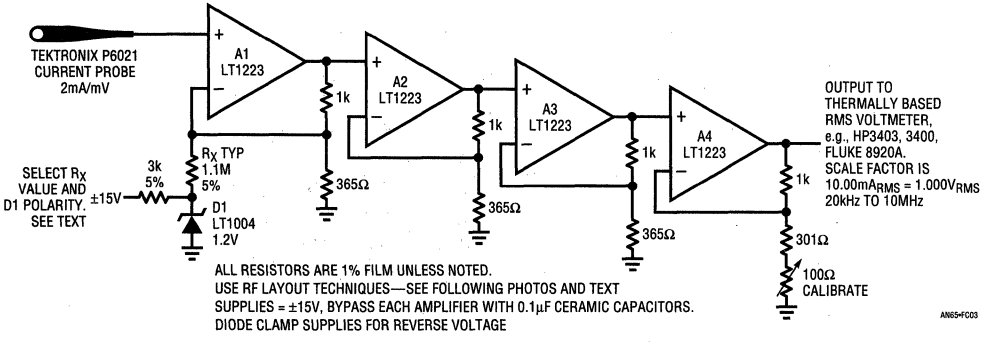

Figure C3. Precision "Clip-On" Current Probe for CCFL Measurements Maintains 1% Accuracy over 20kHz to 10MHz Bandwidth

200. The individual amplifiers avoid any possible crosstalk-based error that could be introduced by a monolithic quad amplifier. D1 and R_X are selected for polarity and value to trim overall amplifier offset. The 100Ω trimmer sets gain, fixing the scale factor. The output drives a thermally based, wideband RMS voltmeter. In practice, the circuit is built into a 2.25" × 1" × 1" enclosure which is *directly* connected via BNC hardware to the voltmeter. No cable is used. Figure C4 shows the probe/amplifier combination. Figure C5 details RF layout techniques used in the amplifier's

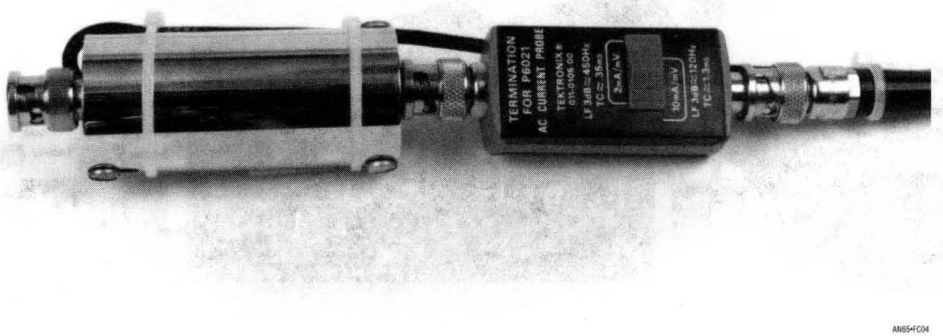

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Figure C4. Current Probe Amplifier Mated to the Current Probe Termination Box

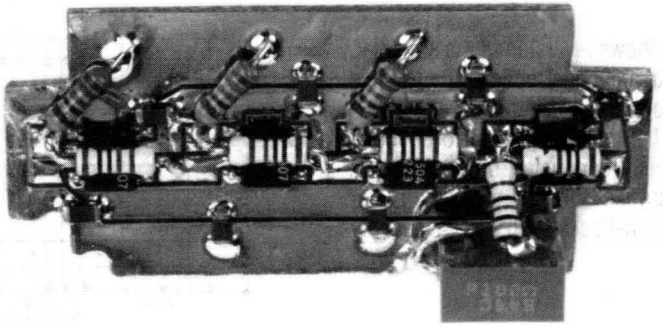

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Figure C5. RF Layout Technique for the Current Probe Amplifier Is Required for Performance Levels Quoted in Text

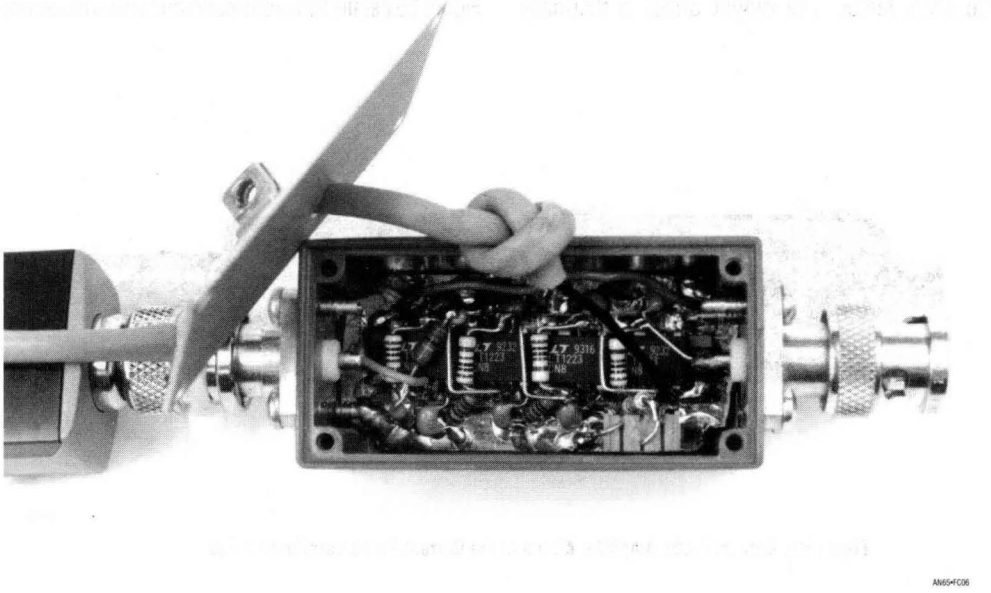

Figure C6. A Version of the Current Probe Amplifier in Its Housing. Current Probe Terminator Is at Left

construction. Figure C6 shows a version of the amplifier, detailing enclosure layout and construction. The result is a "clip-on" current probe with 1% accuracy over a 20kHz to 10MHz bandwidth. This tool has proven to be indispensable to any rigorously conducted backlight work. Figure C7 shows response for the probe/amplifier as measured on a Hewlett-Packard HP4195A network analyzer.

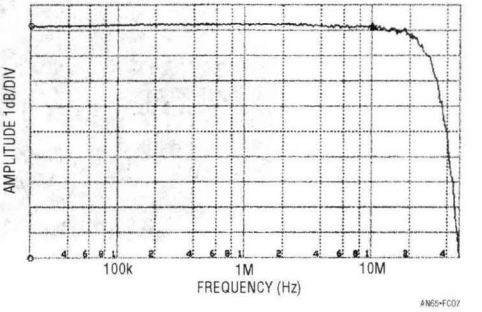

Figure C7. Amplitude vs Frequency Output of HP4195A Network Analyzer. Current Probe/Amplifier Maintains 1% (0.1dB) Error Bandwidth from 20kHz to 10MHz. Small Aberrations Between 10MHz and 20MHz Are Test Fixture Related

Current Calibrator

Figure C8's circuit, a current calibrator, permits calibration of the probe/amplifier and can be used to periodically check probe accuracy. A1 and A2 form a Wein bridge oscillator. Oscillator output is rectified by A4 and A5 and compared to a DC reference at A3. A3's output controls Q1, closing an amplitude stabilization loop. The stabilized amplitude is terminated into a 100Ω, 0.1% resistor to provide a precise 10.00mA, 60kHz current through the series current loop. Trimming is performed by altering the nominal 15k resistor for exactly 1.000V_{RMS} across the 100Ω unit.

In use, this current probe has shown 0.2% baseline stability with 1% absolute accuracy over one year's time. The sole maintenance requirement for preserving accuracy is to keep the current probe jaws clean and avoid rough or abrupt handling of the probe.[2] Figure C9a shows the probe/calibrator used with an RMS voltmeter. Figure C9b shows the current probe in use, in this case determining display frame parasitic loss.

Note 2: Private communication, Tektronix, Inc.

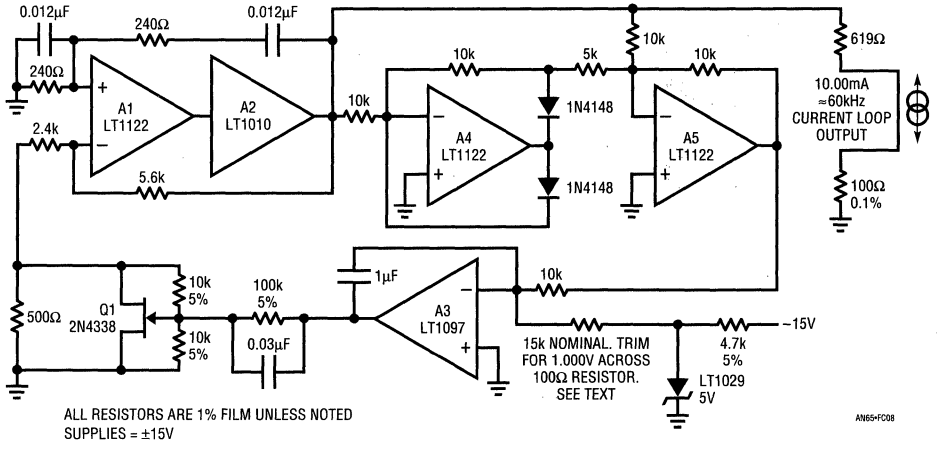

Figure C8. Current Calibrator for Probe Trimming and Accuracy Checks. Stabilized Oscillator Forces 10.00mA Through Output Current Loop at 60kHz

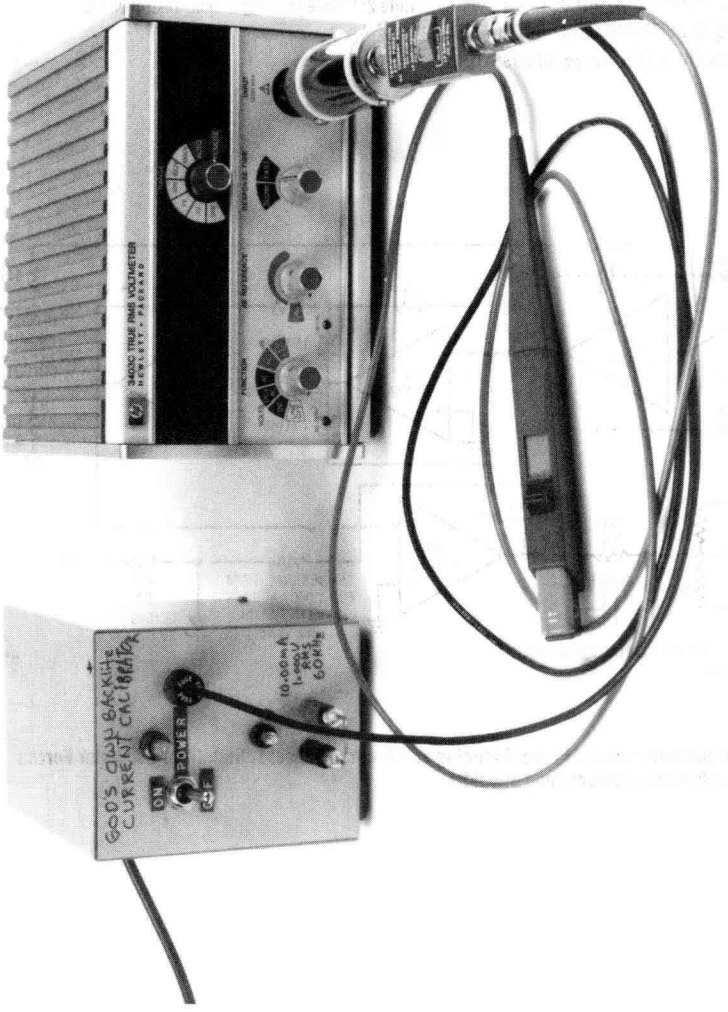

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Figure C9a. Complete Current Probe Test Set Includes Probe, Amplifier, Calibrator and Thermally Based RMS Voltmeter. Accuracy Is 1% to 10MHz

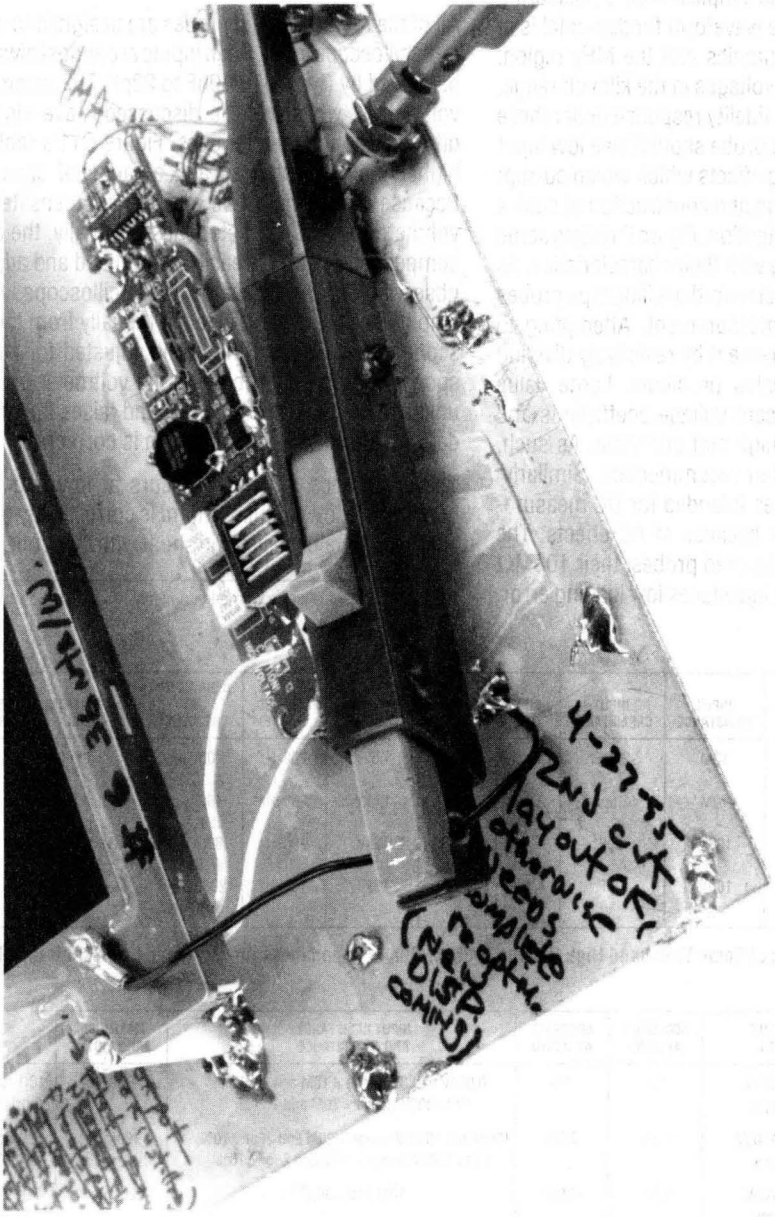


Figure C9b. Current Probe Measuring Display Frame Parasitic Current. "Clip-On" Capability Allows Measurement at Any Point in Lamp Circuit

Voltage Probes for Grounded Lamp Circuits

The high voltage measurement across the lamp is quite demanding on the probe. The simplest case is measuring grounded lamp circuits. The waveform fundamental is at 20kHz to 100kHz, with harmonics into the MHz region. This activity occurs at peak voltages in the kilovolt range. The probe must have a high fidelity response under these conditions. Additionally, the probe should have low input capacitance to avoid loading effects which would corrupt the measurement. The design and construction of such a probe requires significant attention. Figure C10 lists some recommended probes along with their characteristics. As stated in the text, almost all standard oscilloscope probes *will fail* [3] if used for this measurement. Attempting to circumvent the probe requirement by resistively dividing the lamp voltage also creates problems. Large value resistors often have significant voltage coefficients and their shunt capacitance is high and uncertain. As such, simple voltage dividing is not recommended. Similarly, common high voltage probes intended for DC measurement will have large errors because of AC effects. The P6013A and P6015 are the favored probes; their 100MΩ input and small capacitance introduces low loading error. The penalty for their 1000X attenuation is reduced output, but the recommended voltmeters (discussion to follow) can accommodate this.

All of the recommended probes are designed to work into an oscilloscope input. Such inputs are almost always 1MΩ paralleled by (typically) 10pF to 22pF. The recommended voltmeters, which will be discussed, have significantly different input characteristics. Figure C11's table shows higher input resistances and a range of capacitances. Because of this the probe must be compensated for the voltmeter's input characteristics. Normally, the optimum compensation point is easily determined and adjusted by observing probe output on an oscilloscope. A known amplitude square wave is fed in (usually from the oscilloscope calibrator) and the probe adjusted for correct response. Using the probe with the voltmeter presents an unknown impedance mismatch and raises the problem of determining when compensation is correct.

The impedance mismatch occurs at low and high frequency. The low frequency term is corrected by placing an appropriate value resistor in shunt with the probe's output.

Note 3: That's twice we've warned you nicely.

TEKTRONIX PROBE TYPE	ATTENUATION FACTOR	ACCURACY	INPUT RESISTANCE	INPUT CAPACITANCE	RISE TIME	BAND-WIDTH	MAXIMUM VOLTAGE	DERATED ABOVE	DERATED TO AT FREQUENCY	COMPENSATION RANGE	ASSUMED TERMINATION RESISTANCE
P6007	100X	3%	10M	2.2pF	14ns	25MHz	1.5kV	200kHz	$700V_{RMS}$ at 10MHz	15pF to 55pF	1M
P6009	100X	3%	10M	2.5pF	2.9ns	120MHz	1.5kV	200kHz	$450V_{RMS}$ at 40MHz	15pF to 47pF	1M
P6013A	1000X	Adjustable	100M	3pF	7ns	50MHz	12kV	100kHz	$800V_{RMS}$ at 20MHz	12pF to 60pF	1M
P6015	1000X	Adjustable	100M	3pF	4.7ns	75MHz	20kV	100kHz	$2000V_{RMS}$ at 20MHz	12pF to 47pF	1M

Figure C10. Characteristics of Some Wideband High Voltage Probes. Output Impedances Are Designed for Oscilloscope Inputs

MANUFACTURER AND MODEL	FULL SCALE RANGES	ACCURACY AT 1MHz	ACCURACY AT 100kHz	INPUT RESISTANCE AND CAPACITANCE	MAXIMUM BANDWIDTH	CREST FACTOR
Hewlett-Packard 3400 Meter Display	1mV to 300V, 12 Ranges	1%	1%	0.001V to 0.3V Range = 10M and < 50pF, 1V to 300V Range = 10M and < 20pF	10MHz	10:1 At Full Scale, 100:1 At 0.1 Scale
Hewlett-Packard 3403C Digital Display	10mV to 1000V, 6 Ranges	0.5%	0.2%	10mV and 100mV Range = 20M and 20pF ±10%, 1V to 1000V Range = 10M and 24pF ±10%	100MHz	10:1 At Full Scale, 100:1 At 0.1 Scale
Fluke 8920A Digital Display	2mV to 700V, 7 Ranges	0.7%	0.5%	10M and < 30pF	20MHz	7:1 At Full Scale, 70:1 At 0.1 Scale

Figure C11. Pertinent Characteristics of Some Thermally Based RMS Voltmeters. Input Impedances Necessitate Matching Network and Compensation for High Voltage Probes

For a 10MΩ voltmeter input a 1.1M resistor is suitable. This resistor should be built into the smallest possible BNC equipped enclosure to maintain a coaxial environment. No cable connections should be employed; the enclosure should be placed *directly* between the probe output and the voltmeter input to minimize stray capacitance. This arrangement compensates the low frequency impedance mismatch. Figure C12 shows the impedance matching box attached to the high voltage probe.

Correcting the high frequency mismatch term is more involved. The wide range of voltmeter input capacitances combined with the added shunt resistor's effects presents problems. How is the experimenter to know where to set the high frequency probe compensation adjustment? One solution is to feed a known value RMS signal to the probe/voltmeter combination and adjust compensation for a proper reading. Figure C13 shows a way to generate a known RMS voltage. This scheme is simply a standard backlight circuit reconfigured for a constant voltage output. The op amp permits low RC loading of the 5.6kΩ feedback termination without introducing bias current error. The 5.6kΩ value may be series or parallel trimmed for a 300V output. Stray parasitic capacitance in the feedback network affects output voltage. Because of this, all feedback associated nodes and components should be rigidly fixed and the entire circuit built into a small metal box. This prevents any significant change in the parasitic terms. The result is a known $300V_{RMS}$ output.

Now, the probe's compensation is adjusted for a 300V voltmeter indication using the shortest possible connection (e.g., BNC-to-probe adapter) to the calibrator box. This procedure, combined with the added resistor, completes the probe-to-voltmeter impedance match. If the probe compensation is altered (e.g., for proper response on an oscilloscope) the voltmeter's reading will be erroneous.[4] It is good practice to verify the calibrator box output before and after every set of efficiency measurements. This is done by *directly* connecting, via BNC adapters, the calibrator box to the RMS voltmeter on the 1000V range.

Note 4: The translation of this statement is to hide the probe when you are not using it. If anyone wants to borrow it, look straight at them, shrug your shoulders and say you don't know where it is. This is decidedly dishonest, but eminently practical. Those finding this morally questionable may wish to re-examine their attitude after producing a day's worth of worthless data with a probe that was unknowingly readjusted.

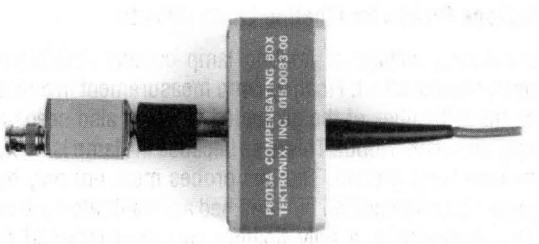
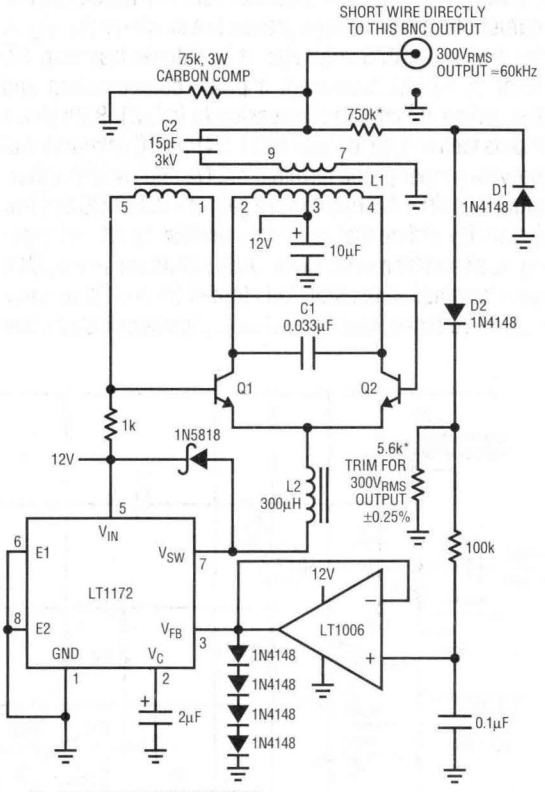


Figure C12. The Impedance Matching Box (Extreme Left) Mated to the High Voltage Probe. Note Direct Connection. No Cable Is Used



C1 = MUST BE A LOW LOSS CAPACITOR.
METALIZED POLYCARB
WIMA FKP2, MKP-20 (GERMAN) OR PANASONIC ECH-U RECOMMENDED
L1 = SUMIDA 6345-020 OR COILTRONICS CTX110092-1
PIN NUMBERS SHOWN FOR COILTRONICS UNIT
L2 = COILTRONICS CTX300-4
Q1, Q2 = ZETEX ZTX849 OR ZDT1048
* = 1% FILM RESISTOR (TEN 75k RESISTORS IN SERIES)

DO NOT SUBSTITUTE COMPONENTS

COILTRONICS (407) 241-7876, SUMIDA (708) 956-0666

AN65•FC13

Figure C13. High Voltage RMS Calibrator Is Voltage Output Version of CCFL Circuit

Voltage Probes for Floating Lamp Circuits

Measuring voltage of floating lamp circuits requires a nearly heroic effort. Floating lamp measurement involves all the difficulties of the grounded case but also needs a fully differential input. This is so because the lamp is freely floating from ground. The two probes must not only be properly compensated but matched and calibrated within 1%. Additionally, a fully floating source is required to check calibration instead of Figure C13's simple single-ended approach.

Figure C14's differential amplifier converts the differential output of the high voltage probes to a single-ended signal for driving an RMS voltmeter. It introduces less than 1% error in 10MHz bandwidth if probe compensation and calibration are correct (discussion to follow). Both probe inputs feed source followers (Q1-Q4) via RC networks that provide proper probe termination. Q2 and Q4 bias differential amplifier A2, running at a gain of ≈2. FET DC and low frequency differential drift is controlled by A1. A1 measures a band limited version of A2's inputs and biases Q4's gate termination resistor. This forces Q4 and Q2 to equal source voltages. This control loop eliminates DC and low frequency error due to FET mismatches.[5] Q1 and Q3 also follow the probe output and feed a small, frequency-dependent, summed signal to A2's auxiliary input. This term is used to correct high frequency common mode rejection limitations of A2's main inputs. A2's output drives the RMS voltmeter via a 20:1 divider. The divider combines with A2's gain-bandwidth characteristics to give 1% accuracy out to 10MHz at the voltmeter input.

To calibrate the amplifier, tie both inputs together and select R_X (shown at Q4) so A1's output is near 0V. It may be necessary to place R_X at Q2 to make this trim. Next, drive the shorted inputs with a 1V, 10MHz sine wave. Adjust the "10MHz CMRR trim" for a minimum RMS voltmeter reading, which should be below 1mV. Finally, lift the "+" input from ground, apply $1V_{RMS}$ at 60kHz and set A2's gain trim for a 100mV voltmeter reading. As a check, grounding the "+" input and driving the "–" input with the 60kHz signal should produce an identical meter reading.

Note 5: A more obvious and less complex way to control FET mismatch-induced offset would utilize a matched dual monolithic FET. Readers are invited to speculate on why this approach has unacceptable high frequency error.

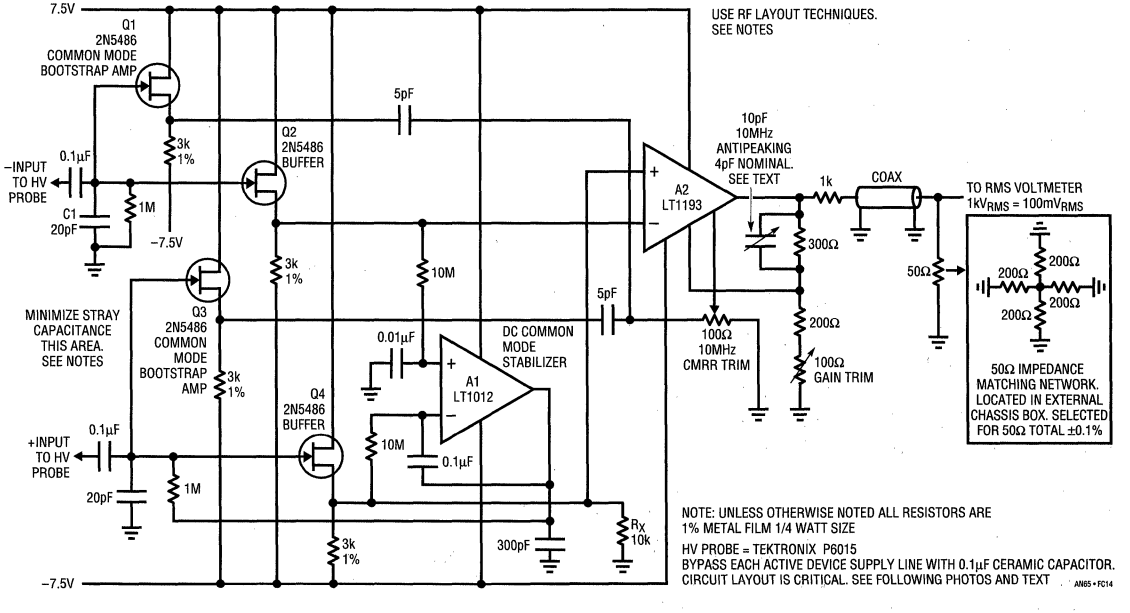


Figure C14. Precison Wideband Differential Probe Amplifier Permits Floating Lamp Voltage Measurement. Source Followers Combine with Impedance Matching Networks to Unload Probes. A2 Provides Differential-to-Single-Ended Transition

Further, known differential inputs at any frequency from 10kHz to 10MHz should produce corresponding calibrated and stable RMS voltmeter readings within 1%. Errors outside this figure at the highest frequencies are correctable by adjusting the "10MHz antipeaking" trim. This completes amplifier calibration.

The high voltage probes must be properly frequency-compensated to give calibrated results with the amplifier. The RC values at the amplifier inputs approximate the termination impedance the probe is designed for. Individual probes must, however, be precisely frequency-compensated to achieve required accuracy. This is quite a demanding exercise because of probe characteristics.

Figure C15 is an approximate schematic of the Tektronix P6015 high voltage probe. A physically large, 100M resistor occupies the probe head. Although the resistor has repeatable wideband characteristics, it suffers distributed parasitic capacitances. These distributed capacitances combine with similar cable losses, presenting a distorted version of the probed waveform to the terminator box. The terminator box impedance-frequency characteristic, when properly adjusted, corrects the distorted information, presenting the proper waveform at the output. The probe's 1000X attenuation factor, combined with its high impedance, provides a safe, minimally invasive measure of the input waveform.

The large number of parasitic terms associated with the probe head and cable result in a complex, multitime-constant response characteristic. Faithful wideband response requires the terminator box components to separately compensate each of these time constants. As such, no less than seven user adjustments are required to compensate the probe to any individual instrument input. These trims are interactive, requiring a repetitive sequence before the probe is fully compensated. The probe manual describes the trimming sequence, using the intended oscilloscope display as the output. In the present case the ultimate output is an RMS voltmeter via the differential amplifier just described. This complicates determining the probe's proper compensation point but can be accommodated.

To compensate the probes, connect them *directly* to the calibrated differential amplifier (see Figures C16, C17, C18) and ground the probe associated with the "–" input. Drive the "+" input probe with a 100V, 100kHz square wave that has a clean 10ns edge with minimal aberrations following the transition.[6] The absolute amplitude of the waveform is unimportant. Monitor this waveform[7] on an oscilloscope. Additionally, monitor A2's output in the

Note 6: Suitable instruments include the Hewlett-Packard 214A and the Tektronix type 106 pulse generators.
Note 7: Use a properly compensated probe, please!

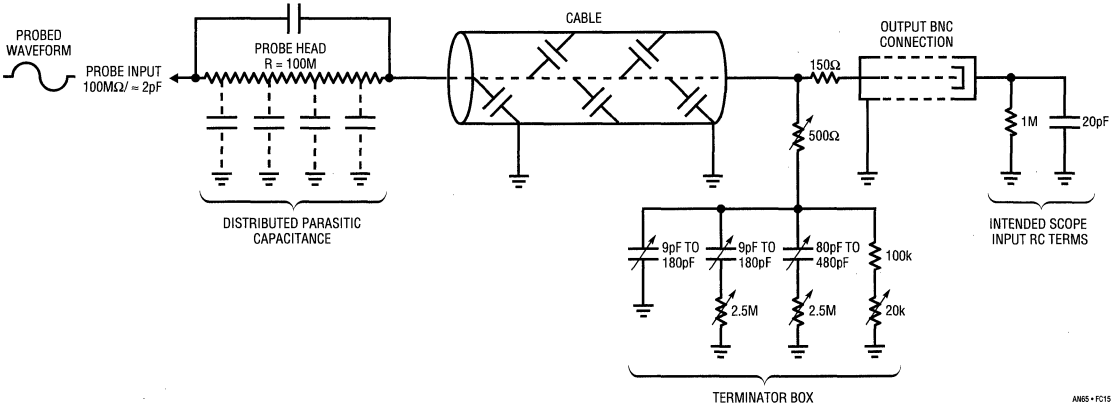


Figure C15. Approximate Schematic of Tektronix P6015 High Voltage Probe. Distributed Parasitic Capacitances Necessitate Numerous Interactive Trims, Complicating Probe Matching to Voltmeter

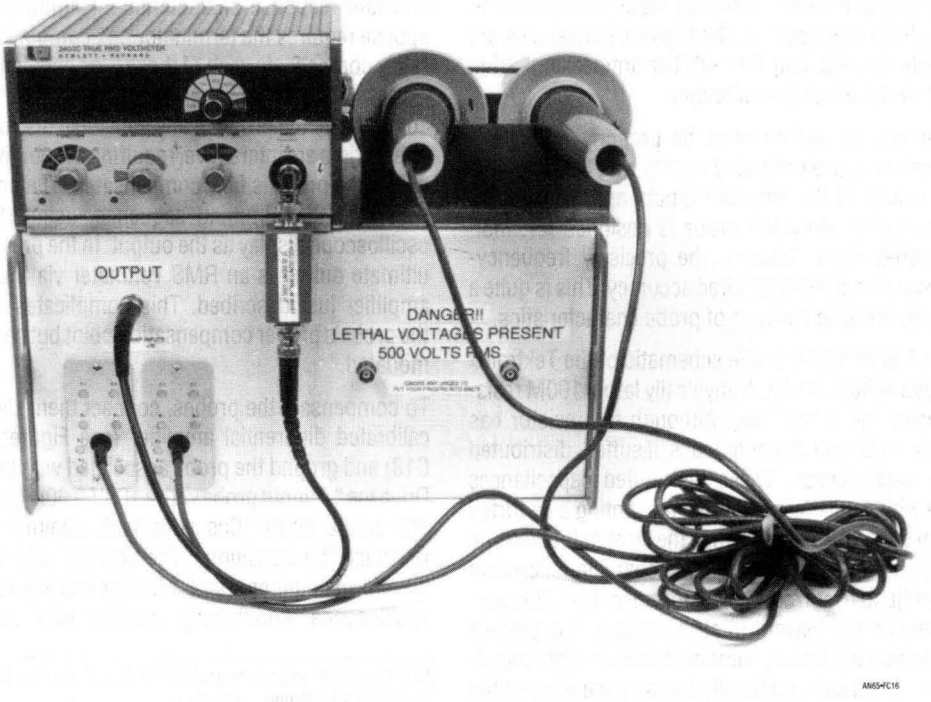


Figure C16. Complete Differential Probe and Calibrator. BNC Outputs Provide Precision, Floating 500V_{RMS} Calibration Source to Check Probe/Amplifier Section

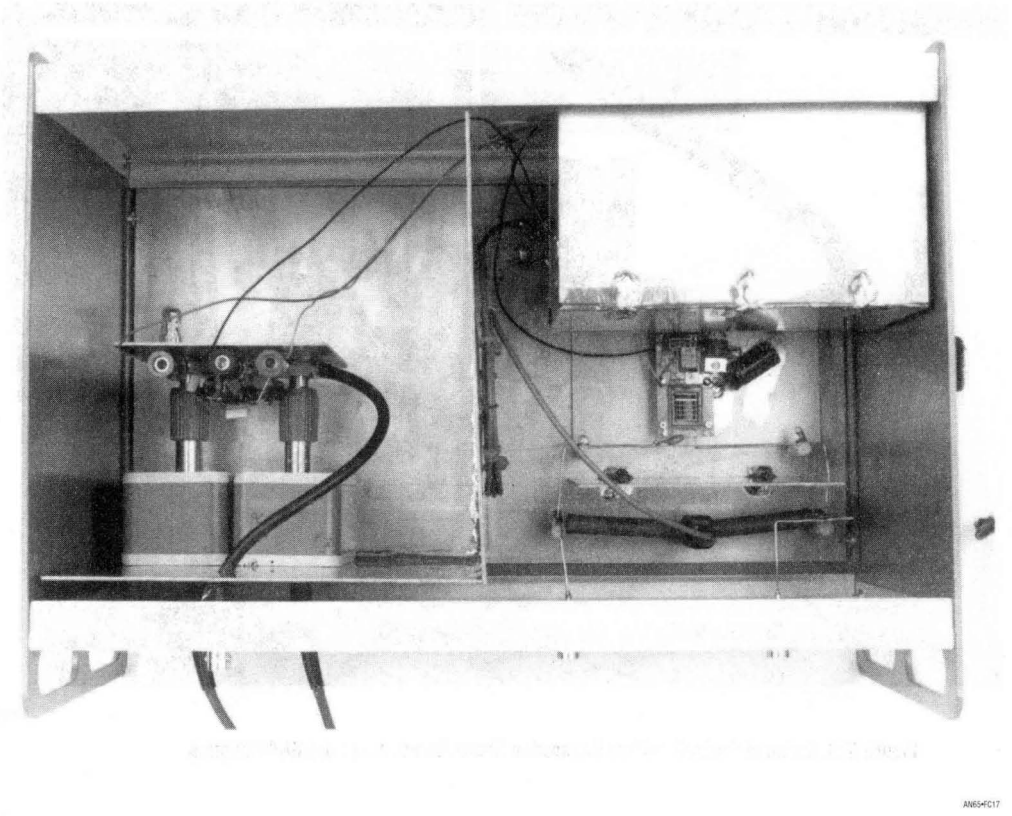
differential amplifier (see Figure C14) with the oscilloscope.[8] Perform the compensation procedure described in the Tektronix P6015 manual until both waveforms displayed on the oscilloscope have identical shapes. When this state is reached, repeat this procedure with the "–" input probe driven and the "+" input probe grounded. This sequence brings the probe's interactive adjustments reasonably close to the optimum points.

To complete the calibration, connect the 50Ω precision termination (see Figures C14 and C16) and the RMS voltmeter to the differential amplifier's output (see Figure C16). Ground the "–" input probe and drive the "+" probe with a known amplitude high voltage waveform of about 60kHz.[9]

Perform *very slight* readjustments of this probe's compensation trims to get the voltmeter's reading to agree with the calibrated input (account for scaling differences––e.g., ignore the voltmeter's range and decimal point indications). The trim(s) having the greatest influence should be utilized for this adjustment—only a slight adjustment should be required. Upon completing this step repeat the procedure using the 100V, 100kHz square wave, verifying input/output waveform edge fidelity. If waveform fidelity has been lost retrim and try again. Several iterations may be necessary until both conditions are met.

Repeat the above procedure for the "–" probe adjustment with the "+" probe grounded.

Note 8: See Footnote 7.
Note 9: Figure C13's calibrator is appropriate.



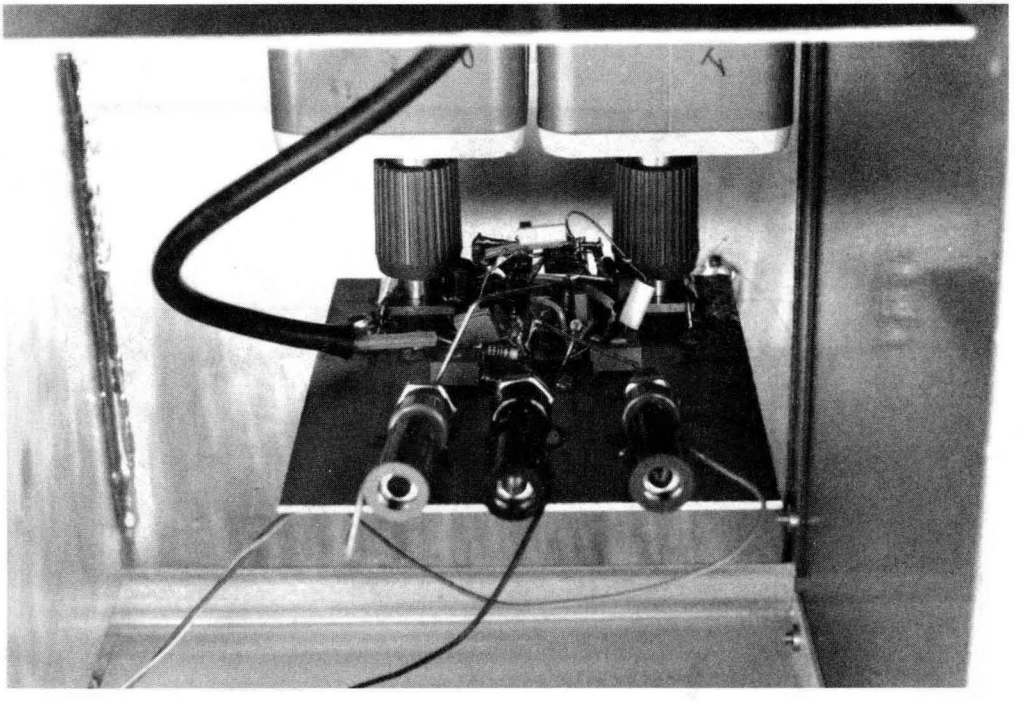
AN65•FC17

Figure C17. Top View of Differential Probe/Calibrator. Probes Are Directly Mated to Differential Amplifier (Left). Calibrator Is to Right. Current Transformer Is Located Between Load Resistors

Short both probes together and drive them with the 100V, 100kHz square wave. The RMS voltmeter should read (ideally) zero. Typically, it should indicate well below 1% of input. The differential amplifier's "10MHz CMRR trim" (Figure C14) can be adjusted to minimize the voltmeter reading.

Next, with the probes still shorted, apply a swept 20kHz to 10MHz sine wave with the highest amplitude available. Monitor A2's output with an RMS voltmeter, ensuring that it never rises above 1% of input amplitude. Finally,[10] apply the highest available known amplitude, swept 20kHz to 10MHz signal to each probe with the other probe grounded. Verify that the RMS voltmeter indicates correct and flat gain over the entire swept frequency range for each case. If any condition described in this paragraph is not met, the entire calibration sequence must be repeated. This completes the calibration.

Note 10: "Finally" is more than an appropriate descriptive. Achieving a wideband, matched probe response involving 14 interactive adjustments takes time, patience and utter determination. Allow at least six hours for the entire session. You'll need it.



AN65•FC18

Figure C18. Detail of Probe/Amplifier Connection Shows Direct, Low Loss BNC Coupling

Differential Probe Calibrator

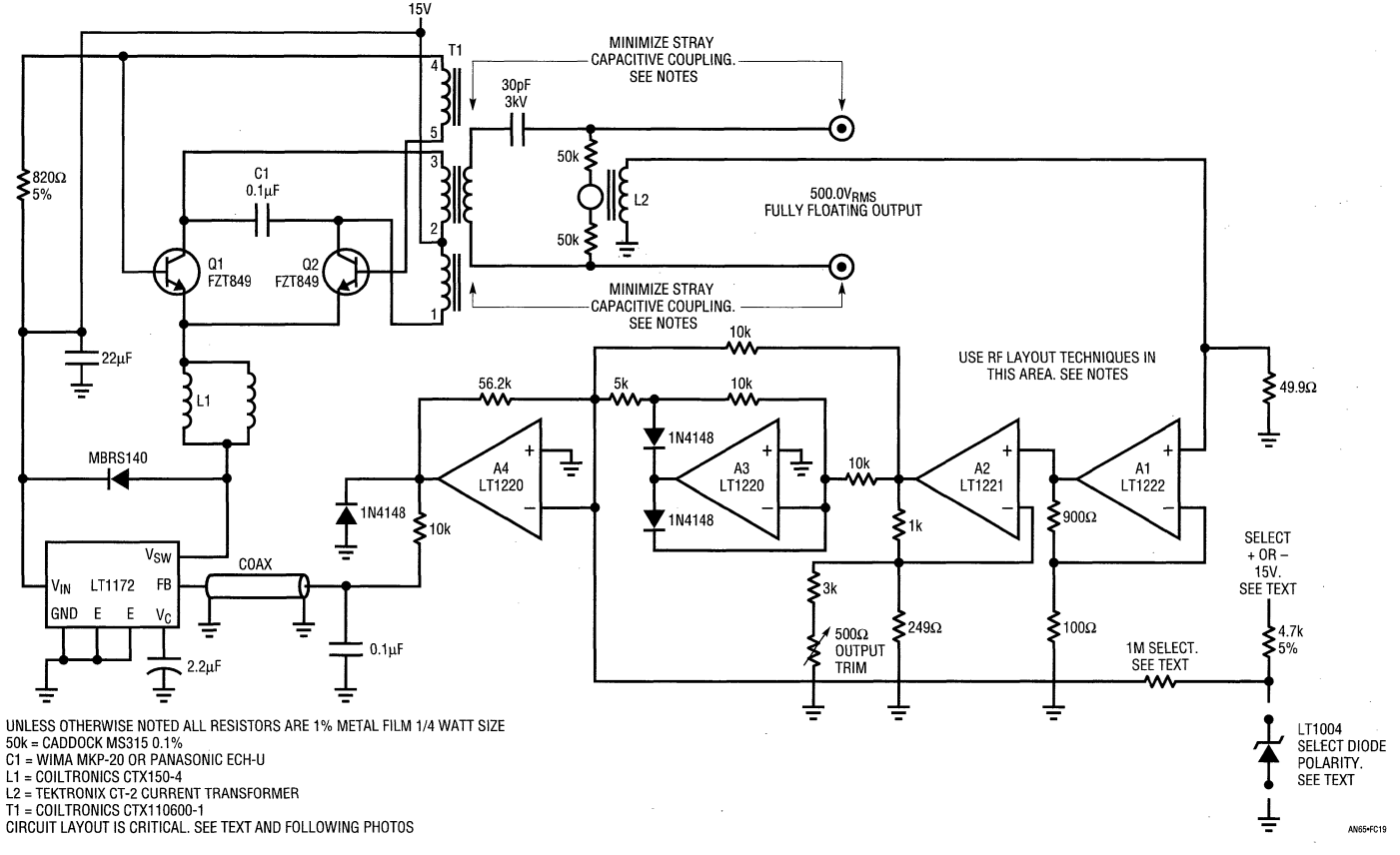
A calibrator with a fully floating, differential output allows periodic operational checking of the differential probe's accuracy. This calibrator is built into the same enclosure as the differential probe (Figure C16). Figure C19 is a schematic of the calibrator.

The circuit is a highly modified form of the basic backlight power supply. Here, T1's output drives two precision resistors which are well-specified for high frequency, high voltage operation. The resistor's current is monitored by L2, a wideband current transformer. L2's placement between the resistors combines with T1's floating drive to minimize the effects of L2's parasitic capacitance. Although L2 has parasitic capacitance, it is bootstrapped to essentially 0V, negating its effect.

L2's secondary output is amplified by A1 and A2, with A3 and A4 serving as a precision rectifier. A4's output is smoothed by the 10kΩ/0.1μF filter, closing a loop at the LT1172's Feedback pin. Similar to previously described CCFL circuits, the LT1172 controls Royer drive, setting T1's output.

To calibrate this circuit, ground the LT1172's V_C pin, open T1's secondary and select the LT1004's polarity and associated resistor value for 0V at A4's output. Next, put a 5.00mA, 60kHz current through L2.[11] Measure A4's smoothed output (the LT1172's Feedback pin) and adjust the "output trim" for 1.23V. Next, reconnect T2's secondary, remove the current calibrator connection and unground

Note 11: Figure C8's output, rescaled for 5.00mA, is a source of calibrated current.



UNLESS OTHERWISE NOTED ALL RESISTORS ARE 1% METAL FILM 1/4 WATT SIZE
50k = CADDOCK MS315 0.1%
C1 = WIMA MKP-20 OR PANASONIC ECH-U
L1 = COILTRONICS CTX150-4
L2 = TEKTRONIX CT-2 CURRENT TRANSFORMER
T1 = COILTRONICS CTX110600-1
CIRCUIT LAYOUT IS CRITICAL. SEE TEXT AND FOLLOWING PHOTOS

Figure C19. The Floating Output Calibrator. Current Transformer Permits Floating Output while Maintaining Tight Loop Control. Amplifiers Provide Gain to Inverter Circuit's Feedback Node

the LT1172 V_C pin. The result is 500V_{RMS} at the calibrator's differential output. This may be checked with the differential probe. Reversing the probe connections should have no effect, with readings well within 1%.[12]

The differential probe and floating output calibrator require almost fanatical attention to layout to achieve the performance levels noted. The wideband amplifier sections utilize RF layout techniques which are reasonably well-documented.[13] Practical construction considerations for parasitic capacitance related issues are photographically detailed in Figures C17 through C23.

Note 12: Those who construct and trim the differential probe and calibrator will experience the unmitigated joy that breaks loose when they agree within 1%.

Note 13: See Reference 26.

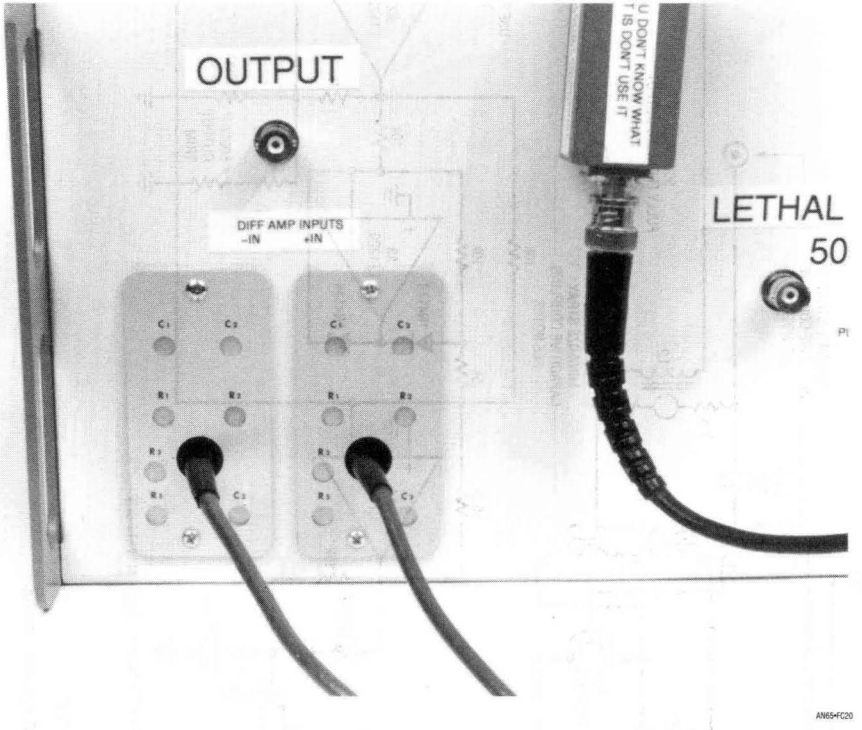


Figure C20. Differential Probes Are Mechanically Secured to Chassis, Discouraging Unauthorized Removal. All Compensation Access Holes Are Sealed, Preventing Unwanted Adjustment

Figure C21. Calibrator Section Detail. Inverter in Center with Load Resistors and Current Transformer in Foreground. Note Shield Between Inverter and Load Resistors, and Low Capacitance Layout

Figure C22. Calibrator Output Detail. Current Transformer Is Bootstrapped to Load Resistor's 0V Midpoint. Shield (Center) Prevents Interaction Between Transformer Field and Load Resistors or Current Transformer. Bus Wire and Nylon Stand-Offs Minimize Stray Capacitance

Figure C23. Calibrator Section Showing Bus Wire/Nylon Post Construction Used to Minimize Stray Capacitance (Left). Inverter in Center; Control Electronics Located at Lower Right. Power Supply Is Enclosed in Shielded Box at Upper Right

RMS Voltmeters

The efficiency measurements require an RMS responding voltmeter. This instrument must respond accurately at high frequency to irregular and harmonically loaded waveforms. These considerations eliminate almost all AC voltmeters, including DVMs with AC ranges.

There are a number of ways to measure RMS AC voltage. Three of the most common include *average, logarithmic* and *thermally* responding. Averaging instruments are calibrated to respond to the average value of the input waveform, which is almost always assumed to be a sine wave. Deviation from an ideal sine wave input produces errors. Logarithmically based voltmeters attempt to overcome this limitation by continuously computing the input's true RMS value. Although these instruments are "real time" analog computers, their 1% error bandwidth is well below 300kHz and crest factor capability is limited. Almost all general purpose DVMs use such a logarithmically based approach and, as such, are not suitable for CCFL efficiency measurements. Thermally based RMS voltmeters are direct acting thermoelectronic analog computers. They respond to the input's RMS heating value. This technique is explicit, relying on the very definition of RMS (e.g., the heating power of the waveform). By turning the input into heat, thermally based instruments achieve vastly higher bandwidth than other techniques.[14] Additionally, they are insensitive to waveform shape and easily accommodate large crest factors. These characteristics are necessary for the CCFL efficiency measurements.

Figure C24 shows a conceptual thermal RMS/DC converter. The input waveform warms a heater, resulting in increased output from its associated temperature sensor. A DC amplifier forces a second, identical, heater/sensor pair to the same thermal conditions as the input driven pair. This differentially sensed, feedback enforced loop makes ambient temperature shifts a common mode term, eliminating their effect. Also, although the voltage and thermal interaction is nonlinear, the input/output RMS voltage relationship is linear with unity gain.

The ability of this arrangement to reject ambient temperature shifts depends on the heater/sensor pairs being isothermal. This is achievable by thermally insulating them with a time constant well below that of ambient shifts. If the time constants to the heater/sensor pairs are

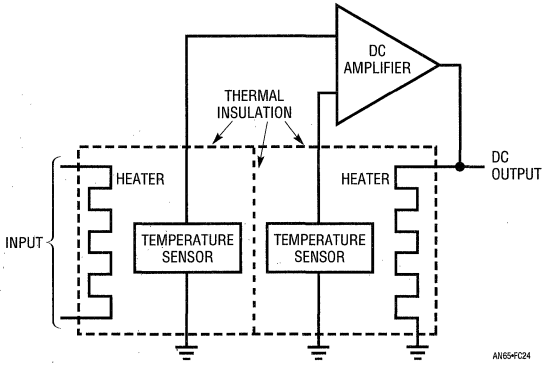


Figure C24. Conceptual Thermal RMS/DC Converter

matched, ambient temperature terms will affect the pairs equally in phase and amplitude. The DC amplifier rejects this common mode term. Note that although the pairs are isothermal, they are insulated from each other. Any thermal interaction between the pairs reduces the system's thermally based gain terms. This would cause unfavorable signal-to-noise performance, limiting dynamic operating range.

Figure C24's output is linear because the matched thermal pair's nonlinear voltage/temperature relationships cancel each other.

The advantages of this approach have made its use popular in thermally based RMS/DC measurements.

The instruments listed in Figure C11, while considerably more expensive than other options, are typical of what is required for meaningful results. The HP3400A and the Fluke 8920A are currently available from their manufacturers. The HP3403C, an exotic and highly desirable instrument, is no longer produced but readily available on the secondary market.

Figure C25 shows an RMS voltmeter which can be constructed instead of purchased.[15] Its small size permits it to be built into bench and production test equipment. As shown, it is designed to be used with Figure C14's differential probe, although the configuration is adaptable to any CCFL-related measurement. It provides a true

Note 14: Those finding these descriptions intolerably brief are commended to References 4, 5, 6, 9, 10, 11 and 12.
Note 15: This circuit derives from Reference 27.

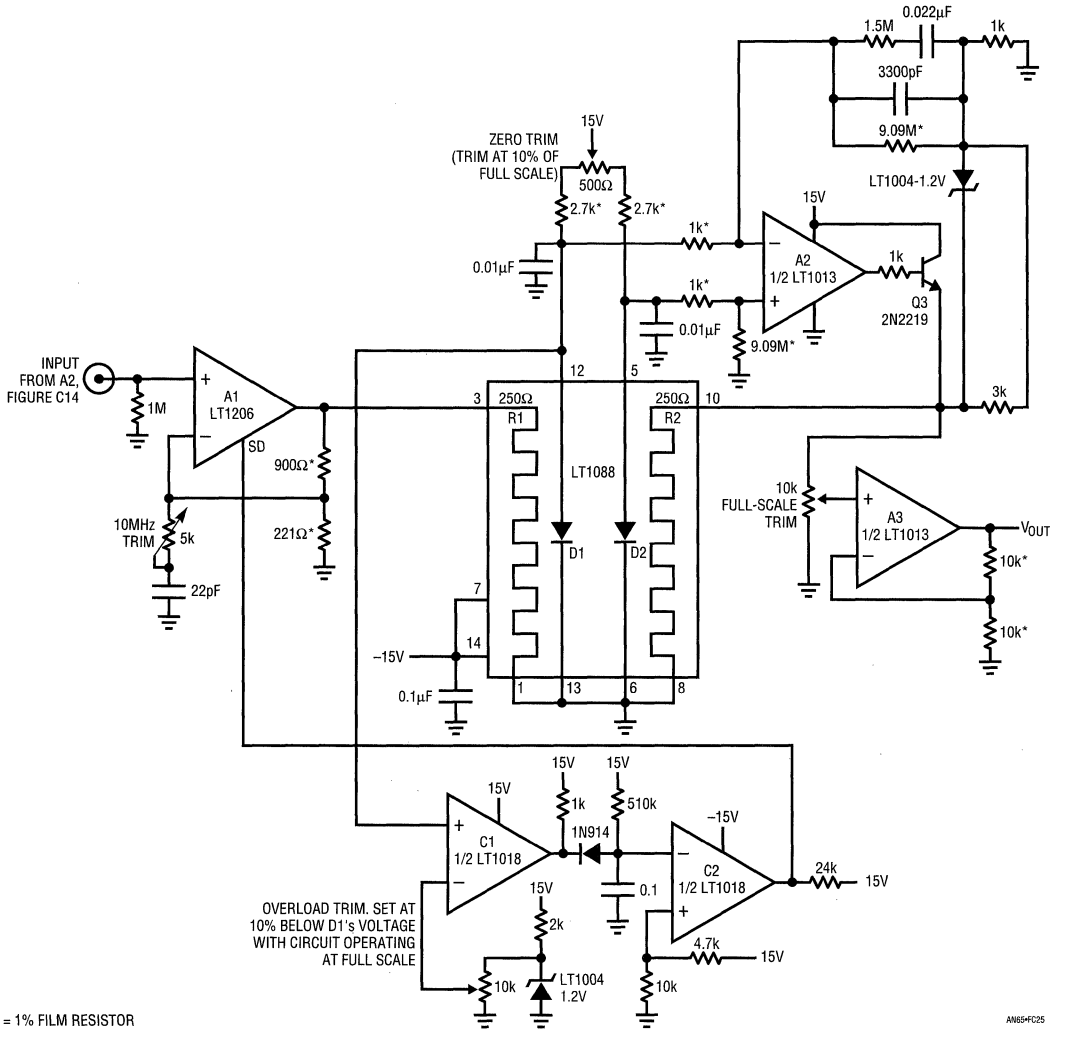


Figure C25. Wideband RMS/DC Converter for Use with Differential Probe/Amplifier. Circuit Is also Usable with Current Probe/Amplifier with Appropriate Gain Adjustments

RMS/DC conversion from DC to 10MHz with less than 1% error, regardless of input signal waveshape. It also features high input impedance and overload protection.

The circuit consists of three blocks; a wideband amplifier, the RMS/DC converter and overload protection. The amplifier provides high input impedance and gain, and drives the RMS/DC converter's input heater. Input resistance is defined by the 1M resistor with input capacitance about 10pF. The LT1206 provides a flat 10MHz bandwidth gain of 5. The 5kΩ/22pF network gives A1 a slight peaking characteristic at the highest frequencies, allowing 1% flatness to 10MHz. A1's output drives the RMS/DC converter.

The LT1088-based RMS/DC converter is made up of matched pairs of heaters and diodes and a control amplifier. The LT1206 drives R1, producing heat which lowers

D1's voltage. Differentially connected A2 responds by driving R2 via Q3 to heat D2, closing a loop around the amplifier. Because the diodes and heater resistors are matched, A2's DC output is related to the RMS value of the input, regardless of input frequency or waveshape. In practice, residual LT1088 mismatches necessitate a gain trim, which is implemented at A3. A3's output is the circuit output. The LT1004 and associated components provide loop compensation and good settling time over wide ranges of operating conditions (see Footnote 14).

Start-up or input overdrive can cause A1 to deliver excessive current to the LT1088 with resultant damage. C1 and C2 prevent this. Overdrive forces D1's voltage to an abnormally low potential. C1 triggers low under these conditions, pulling C2's input low. This causes C2's output to go high, putting A1 into shutdown and terminating the overload. After a time determined by the RC at C2's input, A1 will be enabled. If the overload condition still exists the loop will almost immediately shut A1 down again. This oscillatory action will continue, protecting the LT1088 until the overload condition is removed.

Performance for the circuit is quite impressive. Figure C26 plots error from DC to 11MHz. The graph shows 1% error bandwidth of 11MHz. The slight peaking out to 5MHz is due to the gain boost network at A1's negative input. The peaking is minimal compared to the total error envelope, and a small price to pay to get the 1% accuracy to 10MHz.

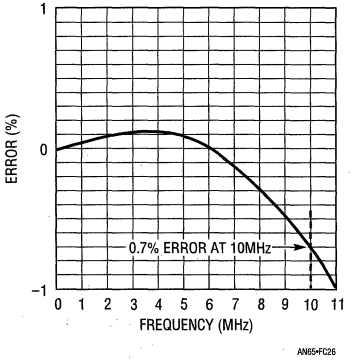


Figure C26. Error Plot for the RMS/DC Converter. Frequency-Dependent Gain Boost at A1 Preserves 1% Accuracy but Causes Slight Peaking Before Rolloff

To trim this circuit put the 5kΩ potentiometer at its maximum resistance position and apply a 100mV, 5MHz signal. Trim the 500Ω adjustment for exactly $1V_{OUT}$. Next, apply a 5MHz, 1V input and trim the 10kΩ potentiometer for $10.00V_{OUT}$. Finally, put in 1V at 10MHz and adjust the 5kΩ trimmer for $10.00V_{OUT}$. Repeat this sequence until circuit output is within 1% accuracy for DC-10MHz inputs. Two passes should be sufficient.

Calorimetric Correlation of Electrical Efficiency Measurements

Careful measurement technique permits a high degree of confidence in the efficiency measurement's accuracy. It is, however, a good idea to check the method's integrity by measuring in a completely different domain. Figure C27 does this by calorimetric techniques. This arrangement, identical to the thermal RMS voltmeter's operation (Figure C24), determines power delivered by the CCFL circuit by measuring its load temperature rise. As in the thermal RMS voltmeter, a differential approach eliminates ambient temperature as an error term. The differential amplifier's output, assuming a high degree of matching in the two thermal enclosures, proportions to load power. The ratio of the enclosure's E • I products yields efficiency information. In a 100% efficient system the amplifier's output energy would equal the power supply's output. Practically it is always less as the CCFL circuit has losses. This term represents the desired efficiency information.

Figure C28 is similar except that the CCFL circuit board is placed within the calorimeter. This arrangement nominally yields the same information, but is a much more demanding measurement because far less heat is generated. The signal-to-noise (heat rise above ambient) ratio is unfavorable, requiring almost fanatical attention to thermal and instrumentation considerations.[16] It is significant that the *total* uncertainty between electrical and both calorimetric efficiency determinations was 3.3%. The two thermal approaches differed by about 2%. Figure C29 shows the calorimeter and its electronic instrumentation. Descriptions of this instrumentation and thermal measurements can be found in the References section following the main text.

Note 16: Calorimetric measurements are not recommended for readers who are short on time or sanity.

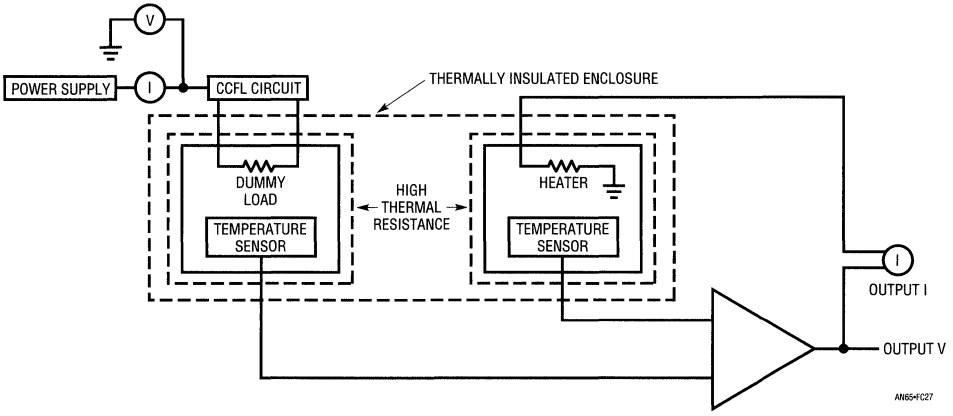


Figure C27. Efficiency Determination via Calorimetric Measurement. Ratio of Power Supply to Output Energy Gives Efficiency Information

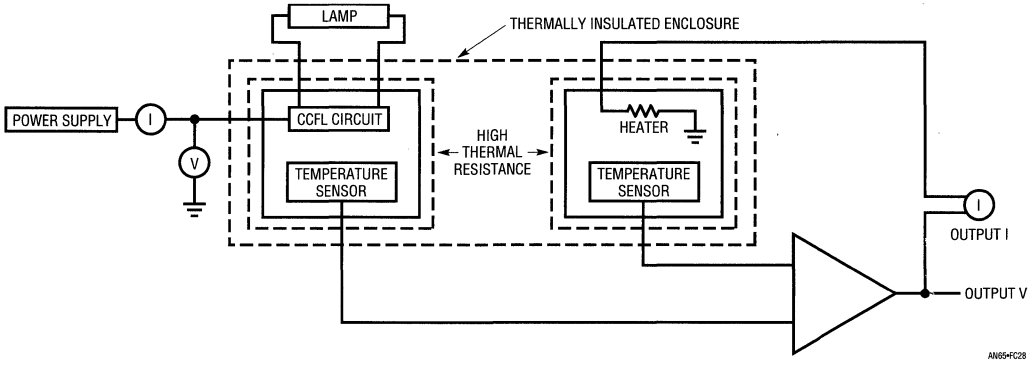


Figure C28. The Calorimeter Measures Efficiency by Determining Circuit Heating Losses

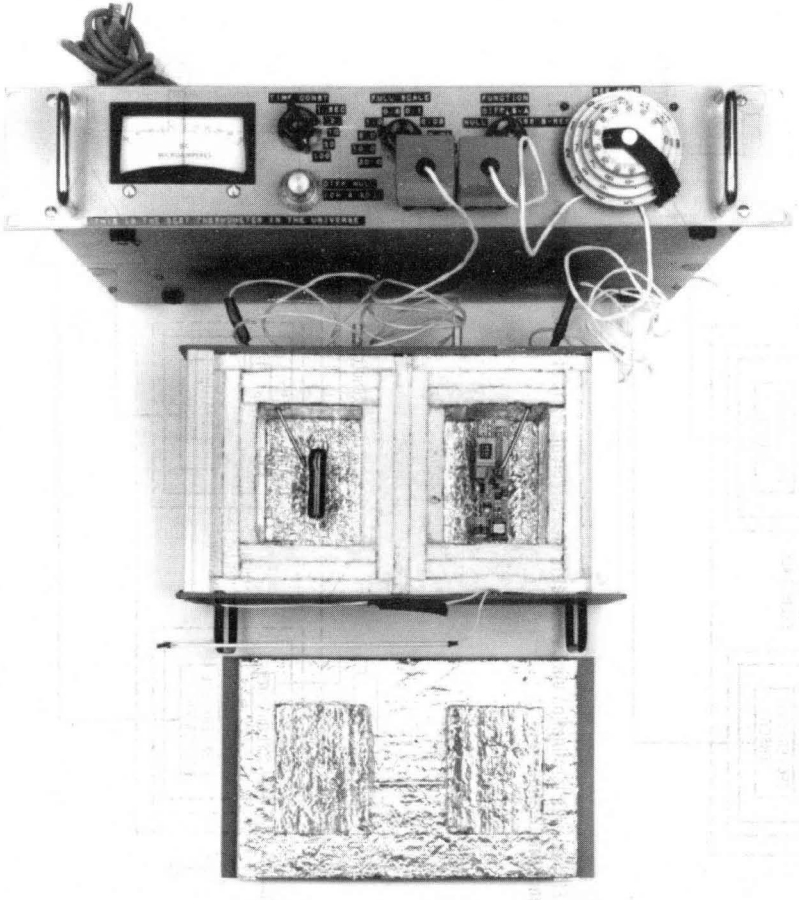


Figure C29. The Calorimeter (Center) and Its Instrumentation (Top). Calorimeter's High Degree of Thermal Symmetry Combined with Sensitive Servo Instrumentation Produces Accurate Efficiency Measurements. Lower Portion of Photo Is Calorimeter's Top Cover

APPENDIX D

PHOTOMETRIC MEASUREMENTS

In the final analysis, the ultimate concern centers around the efficient conversion of power supply energy to light. Emitted light varies monotonically with power supply energy,[1] but certainly not linearly. In particular, lamp luminosity may be highly nonlinear, particularly at high power vs drive power. There are complex trade-offs involving the amount of emitted light vs power consumption, drive waveform shape and battery life. Evaluating these trade-offs requires some form of photometer. The relative luminosity of lamps may be evaluated by placing the lamp in a light tight tube and sampling its output with photodiodes. The photodiodes are placed along the lamp's length and their outputs electrically summed. This sampling technique is an uncalibrated measurement, providing relative data only. It is, however, quite useful in determining relative lamp emittance under various drive conditions. Additionally, because the enclosure has essentially no parasitic capacitance, lamp performance may be evaluated under "zero loss" conditions. Figure D1 shows this "glometer," with its uncalibrated output appropriately scaled in "brights." The switches allow various sampling diodes along the lamp's length to be disabled. The photodiode signal-conditioning electronics are mounted behind the switch panel with the drive electronics located to the left.

Figure D2 details the drive electronics. A1 and A2 form a stabilized output Wein bridge sine wave oscillator. A1 is the oscillator and A2 provides gain stabilization in concert with Q1. The stabilizing loop's operating point is derived from the LT1021 voltage reference. A3 and A4 constitute a voltage-controlled amplifier which feeds power stage A5. A5 drives T1, a high ratio step-up transformer. T1's output sources current to the lamp. Lamp current is rectified and its positive portion terminated into the 1k resistor. The voltage appearing across this resistor, indicative of lamp current, biases A6. Band-limited A6 compares the lamp current-derived signal against the LT1021 reference and closes a loop back to A3. This loop's operating point, and hence lamp current, is set by the "current amplitude" adjustment over a 0mA to 6mA range. A1's "Frequency Adjust" control permits a 20kHz to 130kHz frequency operating range. The switch located at A1's output permits external sources of various waveforms and frequencies to drive the amplifier.

Note 1: But not always! It is possible to build highly electrically efficient circuits that emit less light than "less efficient" designs. See previous text and Appendix L, "A Lot of Cut Off Ears and No Van Goghs—Some Not-So-Great Ideas."

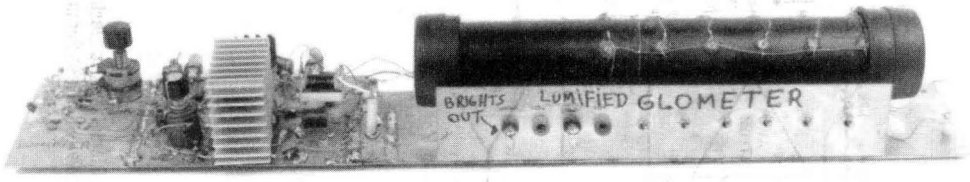


Figure D1. "Glometer" Measures Relative Lamp Emissivity under Various Drive Conditions. Test Lamp Is Inside Cylindrical Housing. Photodiodes on Housing Convert Light to Electrical Output (Center) Via Amplifiers (Not Visible in Photo). Electronics (Left) Permit Varying Drive Waveforms and Frequency

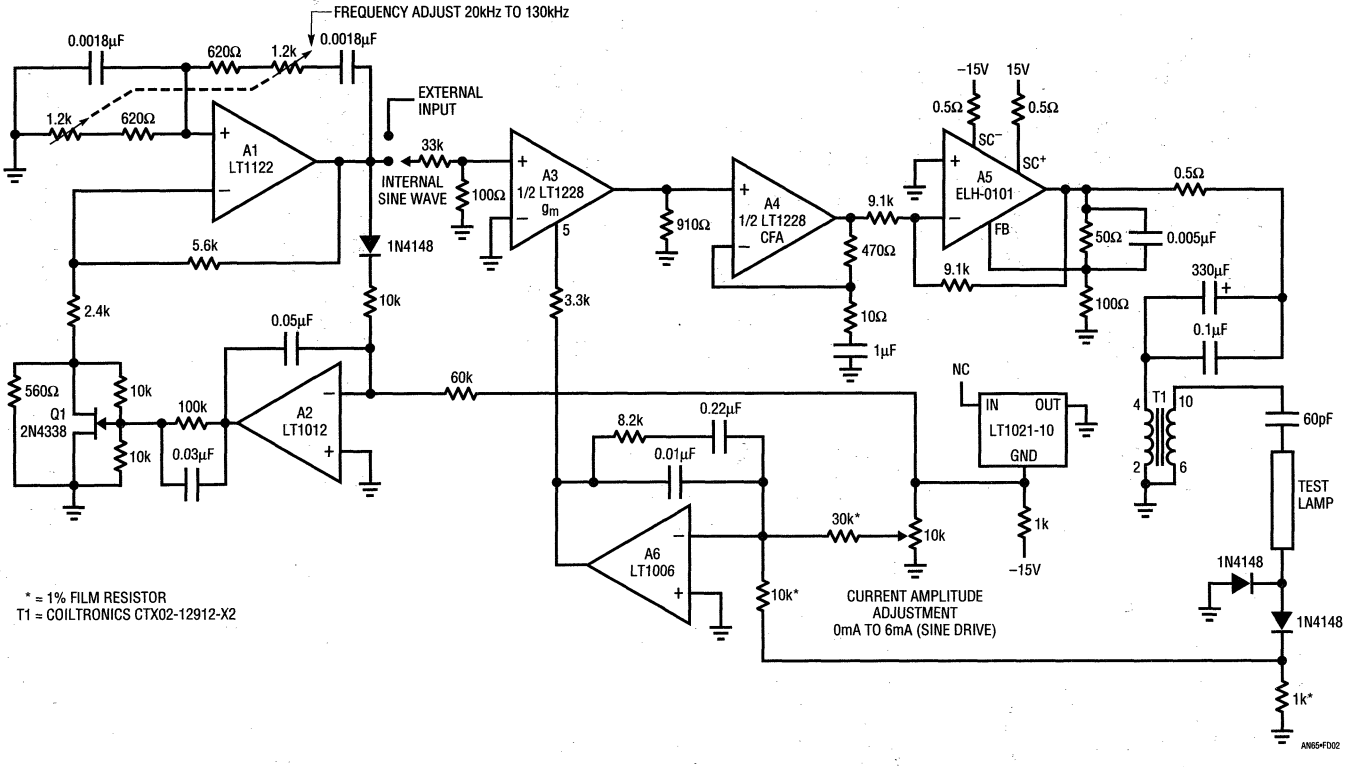


Figure D2. Glometer Drive Electronics Permits Varying Frequency and Waveshape Applied to Test Lamp. Resultant Data Shows Lamp Sensitivity to These Parameters

The drive scheme and wideband transformer provide extremely faithful response. Figure D3 shows waveform fidelity at 100kHz with a 5mA lamp load. Trace A is T1's primary drive and Trace B is the high voltage output. Figure D4, a horizontal and vertical expansion of D3, indicates well-controlled phase shift. Residual effects cause slight primary impedance variations (note primary drive nonlinearity at the sixth vertical division), although the output remains singularly clean.

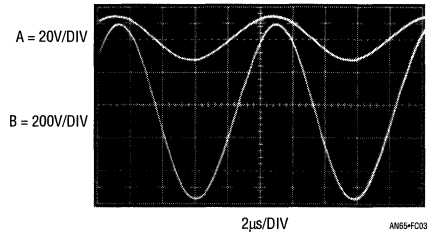


Figure D3. Wideband Transformers Input (Trace A) and Output (Trace B) Waveforms Indicate Clean Response at 100kHz

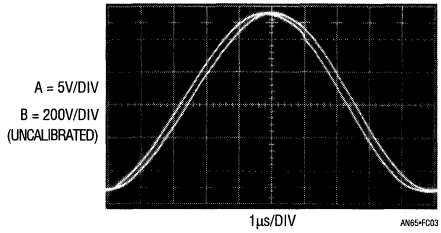


Figure D4. Magnified Versions of Figure D3's waveforms. Output (Trace B) Is Undistorted Despite Slight Drive (Trace A) Deformity at Sixth Vertical Divison. Transfomer Rolloff Dictates This Desirable Behavior

Figure D5 shows the photodiode signal conditioning. Groups of various photodiodes bias amplifiers A1 through A6. Each amplifier's output is fed via a switch to summing amplifier A7. The switches permit establishment of "dead zones" along the test lamp's length, enhancing ability to study emissivity vs location. A7's output represents the summation of all sensed lamp emission.

The glometer's ability to measure relative lamp emission under controlled settings of frequency, waveshape and drive current in a "lossless" environment is invaluable for evaluating lamp performance. Evaluating display performance and correlating results with customers requires absolute light intensity measurements.

Calibrated light measurements call for a true photometer. The Tektronix J-17/J1803 photometer is such an instrument. It has been found particularly useful in evaluating display (as opposed to simply the lamp) luminosity under various drive conditions. The calibrated output permits reliable correlation with customer results.[2] The light tight measuring head allows evaluation of emittance evenness at various display locations.

Figure D6 shows the photometer in use evaluating a display. Figure D7 is a complete display evaluation setup. It includes lamp and DC input voltage and current instrumentation, the photometer described and a computer (lower right) for calculating optical and electrical efficiency.

Note 2: It is unlikely customers would be enthusiastic about correlating the "brights" units produced by the aforementioned glometer.

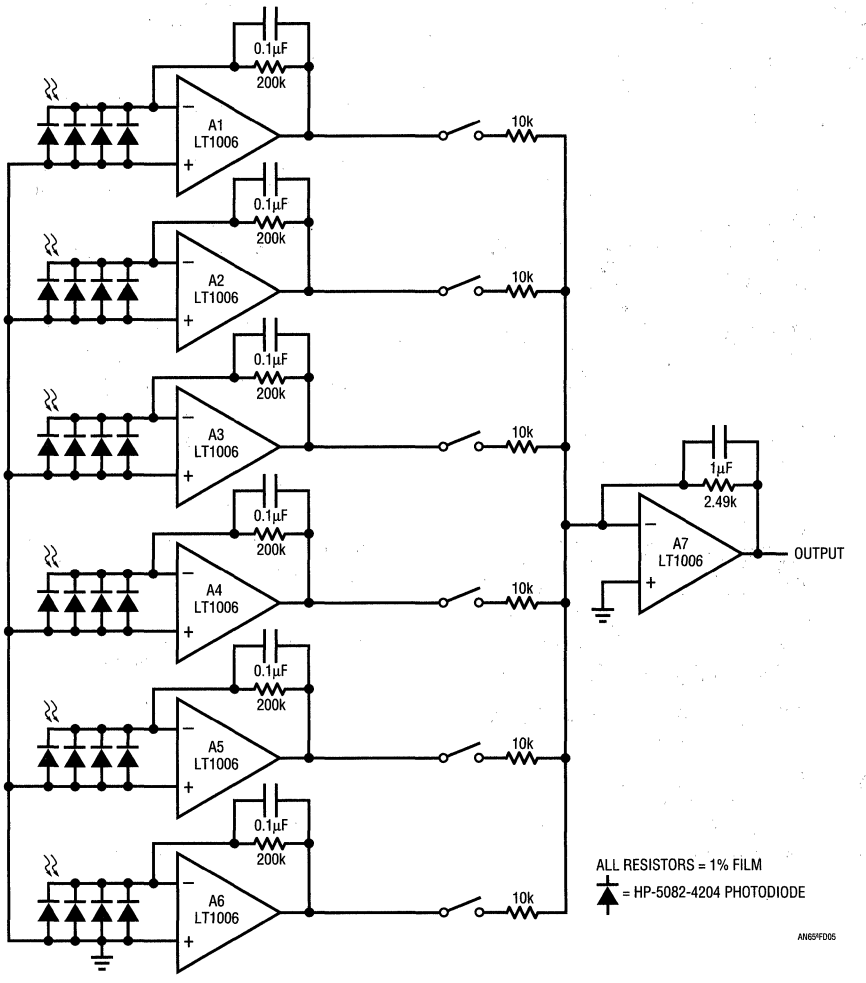


Figure D5. Glometer Photodiode/Amplifier Converts Lamp Light to Relative, Uncalibrated Electrical Output. Switches Permit Investigation of Individual Portions of Lamp Output

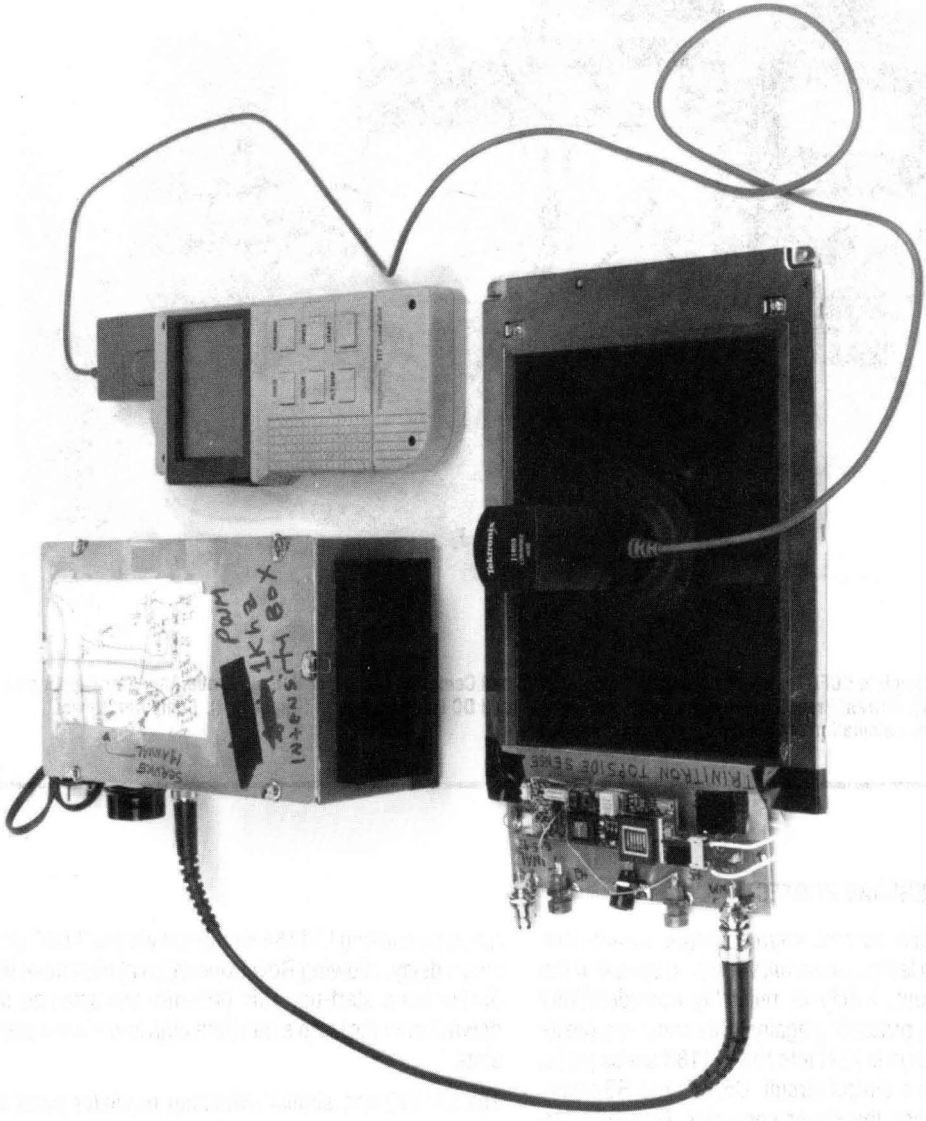


Figure D6. Apparatus for Calibrated Photometric Display Evaluation. Photometer (Upper Right) Indicates Display Luminosity Via Sensing Head (Center). CCFL Circuit (Left) Intensity Is Controlled by Figure F6's Calibrated Pulse Width Generator (Upper Left)

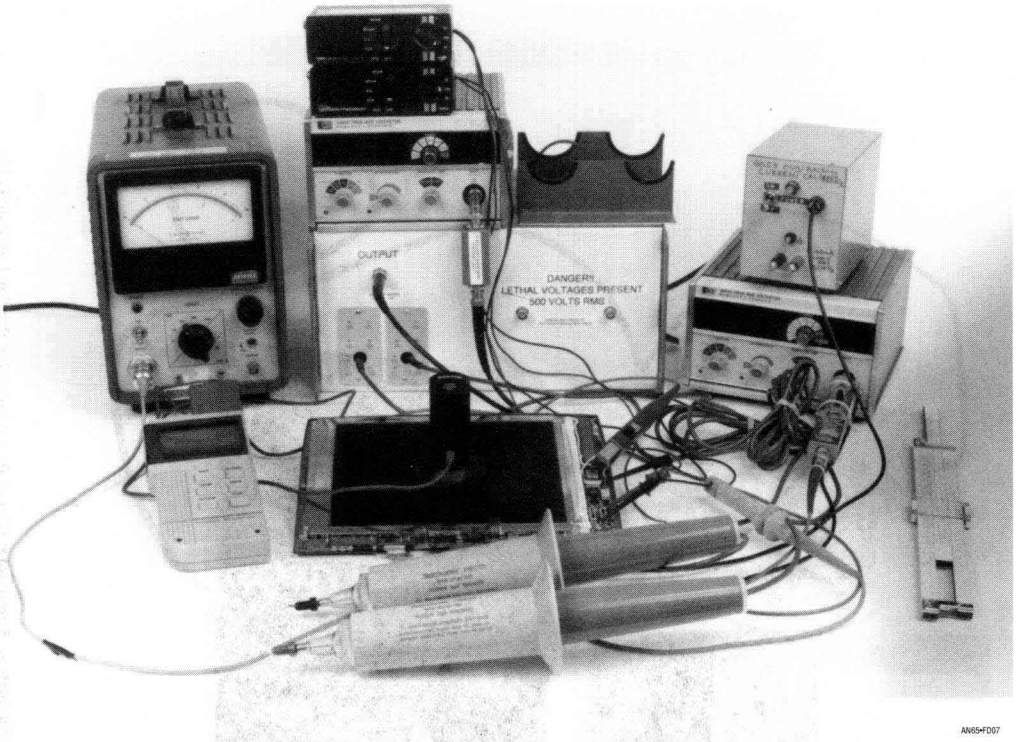


Figure D7. Complete CCFL Test Set Includes Photometer (Left and Center), Differential Voltage Probe/Amplifier (Upper and Lower Center), Current Probe Electronics (Right) and Input V and I DC Instrumentation (Upper Left). Computer (Lower Right) Permits Calculation of Electrical and Optical Efficiency

APPENDIX E

OPEN LAMP/OVERLOAD PROTECTION

The CCFL circuit's current source output means that "open" or broken lamps cause full voltage to appear at the transformer output. Safety or reliability considerations sometimes make protecting against this condition desirable. This protection is built into the LT118X series parts. Figure E1 shows a typical circuit. C5, R2 and R3 sense differentially across the Royer converter. Normally, the voltage across the Royer is controlled to relatively small values. An open lamp will cause full duty cycle modulation at the V_{SW} pin, resulting in large current drive through L2. This forces excessive Royer voltage at the C5/R2/R3 network, causing LT1184 shutdown via the "bulb" pin. C5 sets a delay, allowing Royer operation at high drive levels during lamp start-up. This prevents unwarranted shutdown during the lamp's transient high impedance start-up state.

The LT1172 and similar switching regulator parts need additional circuitry for open lamp protection. Figure E2 details the modifications. Q3 and associated components form a simple voltage mode feedback loop that operates if V_Z turns on. If T1 sees no load, there is no feedback and the Q1/Q2 pair receives full drive. Collector voltage rises to

abnormal levels, and V_Z biases via Q1's V_{BE} path. Q1's collector current drives the feedback node and the circuit finds a stable operating point. This action controls Royer drive and hence output voltage. Q3's sensing across the Royer provides power supply rejection. V_Z's value should be somewhat above the worst-case Q1/Q2 V_{CE} voltage under running conditions. It is desirable to select V_Z's value so clamping occurs at the lowest output voltage possible while still permitting lamp start-up. This is not as tricky as it sounds because the 10k/1µF RC delays the effects of Q3's turn-on. Usually, selecting V_Z several volts above the worst-case Q1/Q2 V_{CE} will suffice.

Additional protection for all CCFL circuits is possible by fusing the main supply line, typically at a value twice the largest expected DC current. Also, a thermally activated fuse is sometimes mated to Q1 and Q2. Excessive Royer current causes heating in the transistors, activating the fuse.

Overload Protection

In certain cases it is desirable to limit output current if either lamp wire shorts to ground. Figure E3 modifies a switching regulator-based circuit to do this. The current sensing network, normally series connected with the lamp, is moved to the transformer. Any overload current must originate from the transformer. Feedback sensing in this path provides the desired protection. This connection measures *total* delivered current, including parasitic terms, instead of lamp return current. Slight line regulation and current accuracy degradation occurs, but not to an objectable extent.

Floating lamp circuits, because of their isolation, are inherently immune to ground referred shorts. Shorted lamp wires are also tolerated because of the primary side current sensing.

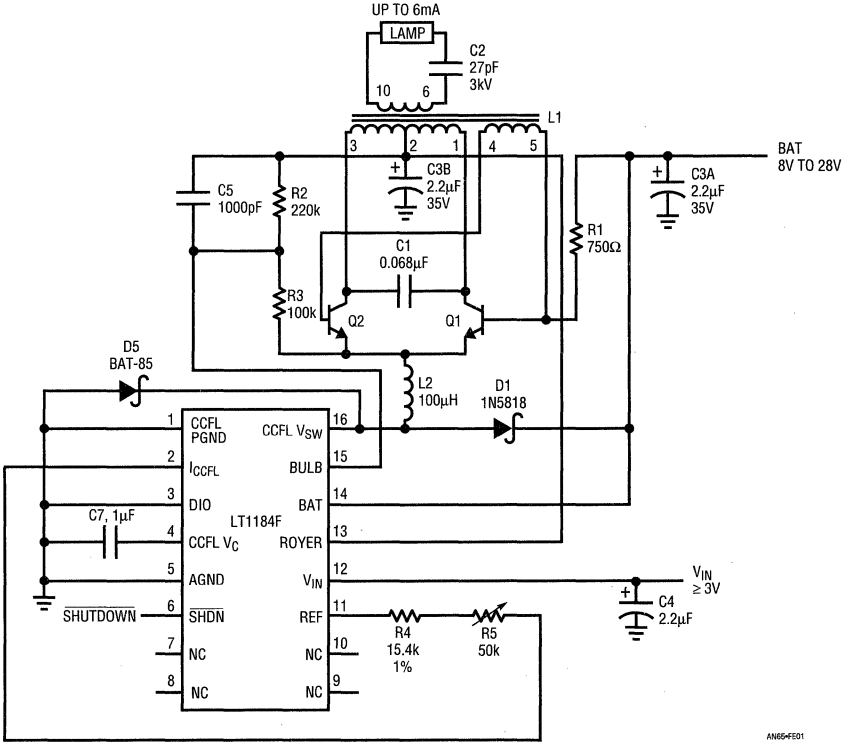


Figure E1. C5, R2 and R3 Provide Delayed Sensing Across Royer Converter, Protecting Against Open Lamp Conditions in LT118X Series ICs

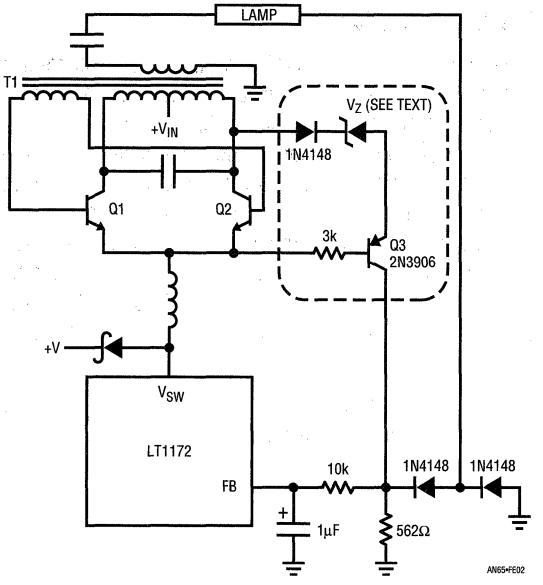


Figure E2. Q3 and Associated Components Form a Local Regulating Loop to Limit Output Voltage

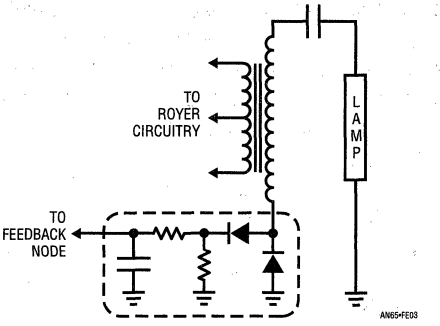


Figure E3. Relocating Feedback Network (Circled Components) to Transformer Secondary Maintains Current Control When Output Is Shorted. Trade-Off Is Slight Degradation in Line Regulation and Current Accuracy

APPENDIX F

INTENSITY CONTROL AND SHUTDOWN METHODS

The CCFL circuits usually require shutdown capability and some form of intensity (dimming) control. Figure F1 lists various options for the LT118X parts. Control sources include pulse width modulation (PWM), potentiometers and DACs or other voltage sources. The LT1186 (not shown) uses a digital serial-bit stream data input and is discussed in text associated with Figure 51.

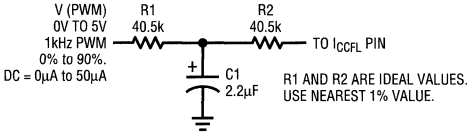
In all cases shown the average current into the I_{CCFL} pin sets lamp current. As such, the amplitude and duty cycle must be controlled in cases A and B. The remaining examples use the LT118X's reference to eliminate amplitude uncertainty-induced errors.

Figure F2 shows shutdown options for LT118X parts. The parts have a high impedance Shutdown pin, or power may simply be removed from V_{IN}. Switching V_{IN} power requires a higher current control source but shutdown current is somewhat lower.

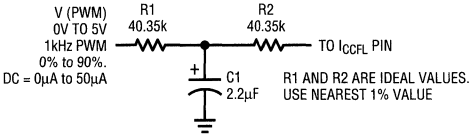
Figure F3 shows options for dimming control in LT1172 and similar regulator-based CCFL circuits. Three basic ways to control intensity appear in the figure. The most common intensity control method is to add a potentiometer in series with the feedback termination. When using this method ensure that the minimum value (in this case 562Ω) is a 1% unit. If a wide tolerance resistor is used the lamp current, at maximum intensity setting, will vary appropriately.

Pulse width modulation or variable DC is sometimes used for intensity control. Two interfaces work well. Directly driving the Feedback pin via a diode—22k resistor with DC or PWM produces intensity control. The other method shown is similar, but places the 1µF capacitor outside the feedback loop to get best turn-on transient response. This is the best method if output overshoot must be minimized. Note that in all cases the PWM source amplitude at 0%

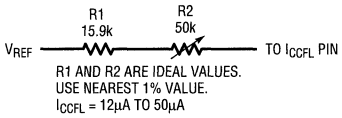
(F1a) LT1182/LT1183 I_{CCFL} PWM Programming



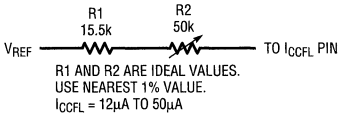
(F1b) LT1184/LT1184F I_{CCFL} PWM Programming



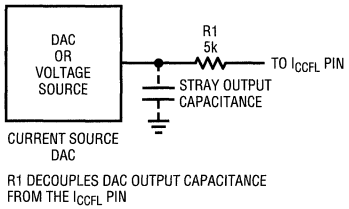
(F1c) LT1183 I_{CCFL} Programming with Potentiometer Control



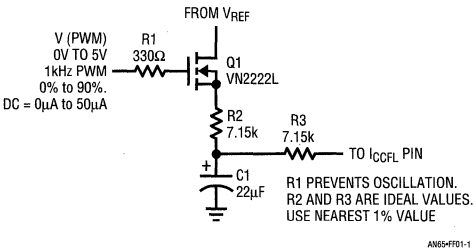
(F1d) LT1184/LT1184F I_{CCFL} Programming with Potentiometer Control



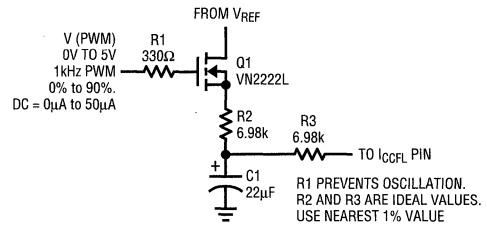
(F1e) LT1182/LT1183/LT1184/LT1184F I_{CCFL} Programming with DAC or Voltage Source Control



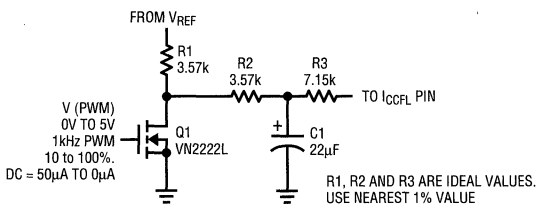
(F1f) LT1183 I_{CCFL} PWM Programming with V_{REF}



(F1g) LT1184/LT1184F I_{CCFL} PWM Programming with V_{REF}



(F1h) LT1183 I_{CCFL} PWM Programming with V_{REF}



(F1i) LT1184/LT1184F I_{CCFL} PWM Programming with V_{REF}

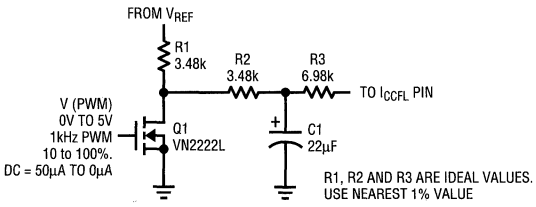


Figure F1. Various Dimming Options for LT118X Series Parts. LT1186 (Not Shown) Has Serial-Bit Stream Digital Dimming Input

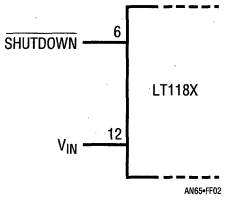


Figure F2. Shutdown Options for LT118X Series Parts Include Shutdown Pin or Simply Removing V_{IN}

duty cycle does not, by definition, effect full-scale lamp current certainty. See the main text section, "Feedback Loop Stability Issues" for pertinent discussion.

Figure F4 shows methods for shutting down switching regulator-based CCFL circuits. In LT1172 circuits pulling the V_C pin to ground puts the circuit into micropower shutdown. In this mode about 50µA flows into the LT1172 V_{IN} pin with essentially no current drawn from the main (Royer center tap) supply. Turning off V_{IN} power eliminates the LT1172's 50µA drain. Other regulators, such as the LT1372, have a separate Shutdown pin.

About Potentiometers

Potentiometers, frequently used in CCFL dimming, require thought to avoid problems. In particular, resistance, ratio tolerances and other issues can upset an ill-prepared design. Keep in mind that ratio tolerances (see Figure F5) are usually better than absolute resistance specifications. Because of this, it is sometimes advantageous to use the device as a voltage divider instead of a rheostat. The key issue in potentiometer-based dimming is usually ensuring that lamp overdrive cannot occur. This is why arranging dimming schemes for maximum intensity at "shorted" potentiometer positions is preferable. The "end resistance" tolerance, which should be checked, is often less significant and more repeatable than that for maximum resistance or even ratio setting. Other issues include wiper current capability, taper characteristic and circuit sensitivity to "opens." Always review circuit behavior for maximum wiper current demands. CCFL dimming schemes almost never require significant wiper current, but ensure that the particular scheme used doesn't have this problem.

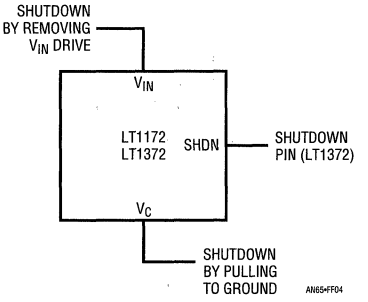


Figure F4. Various Shutdown Options in LT1172/ LT1372 Type CCFL Circuits

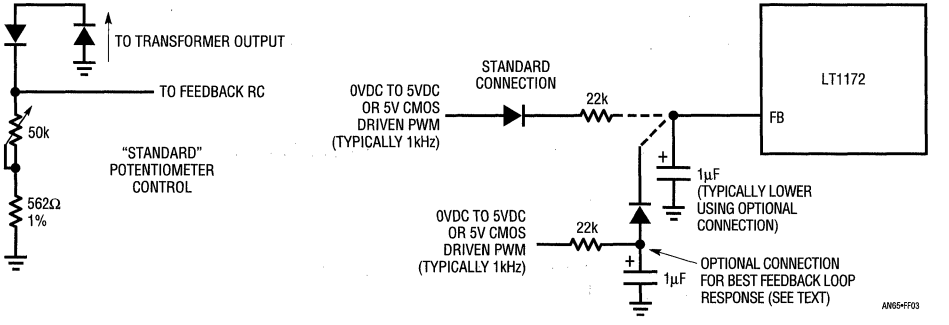


Figure F3. Various Options for Intensity Control in LT1172 and Similar Switching Regulator-Based CCFL Circuits

The potentiometers taper, which may be linear or logarithmic, should be matched to the lamp's current-vs-light output characteristic to provide easy user settability. A poorly chosen unit can cause most of the useful dimming range to occur in a small section of potentiometer travel. Finally, always evaluate how the circuit will react if any terminal develops an open condition, which sometimes happens. It is imperative that the circuit have some relatively benign failure mode instead of forcing excessive lamp current or some other regrettable behavior.

Electronic equivalents of potentiometers are monolithic resistor chains tapped by MOS switches. Some devices feature nonvolatile onboard memory. These units have voltage rating restrictions which must be adhered to as with any integrated circuit. Additionally, they have all the limitations discussed in the section on mechanical potentiometers. Their most serious potential difficulty in backlight dimming applications is extremely high end resistance. In the "shorted" position the FET switch's on-resistance is typically 200Ω—much higher than a mechanical unit. Because of this, electronic potentiometers must almost always be set up as 3-terminal voltage dividers. This can usually be accommodated but may eliminate these devices in some applications.

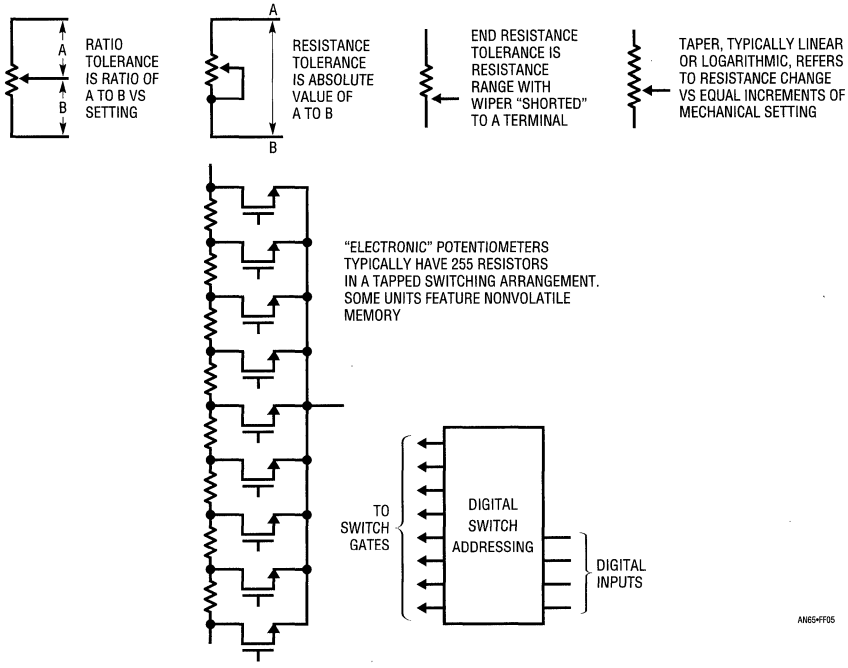


Figure F5. Relevant Characteristics of Mechanical and Electronic Potentiometers in CCFL Dimming Applications

Precision PWM Generator

Figure F6 shows a simple circuit which generates precision variable pulse widths. This capability is useful when testing PWM-based intensity schemes. The circuit is basically a closed-loop pulse width modulator. The crystal controlled 1kHz input clocks the C1/Q1 ramp generator via the differentiator/CMOS inverter network and the LTC201 reset switch. C1's output drives a CMOS inverter, the output of which is resistively sampled, averaged and presented to A1's negative input. A1 compares this signal with a variable voltage from the potentiometer. A1's output biases the pulse width modulator, closing a loop around it. The CMOS inverter's purely ohmic output structure combines with A1's ratiometric operation (e.g., both of A1's input signals derive from the 5V supply) to hold pulse width constant. Variations in time, temperature and supply have essentially no effect. The potentiometer's setting is the sole determinant of output pulse width. Additional inverters provide buffering and furnish the output. The Schottky diodes protect the output from latchup due to cable-induced ESD or accidental events[1] during testing.

The output width is calibrated by monitoring it with a counter while adjusting the 2kΩ trim pot.

As mentioned, the circuit is insensitive to power supply variation. However, the CCFL circuit averages the PWM output. It cannot distinguish between a duty cycle shift and supply variation. As such, the test box's 5V supply should be trimmed ±0.01V. This simulates a "design centered" logic supply under actual operating conditions. Similarly, paralleling additional logic inverters to get lower output impedance should be avoided. In actual use, the CCFL dimming port will be driven from a single CMOS output, and its impedance characteristics must be accurately mimicked.

Note 1: "Accidental events" is a nice way of referring to the stupid things we all do at the bench. Like shorting a CMOS logic output to a –15V supply (then I installed the diodes).

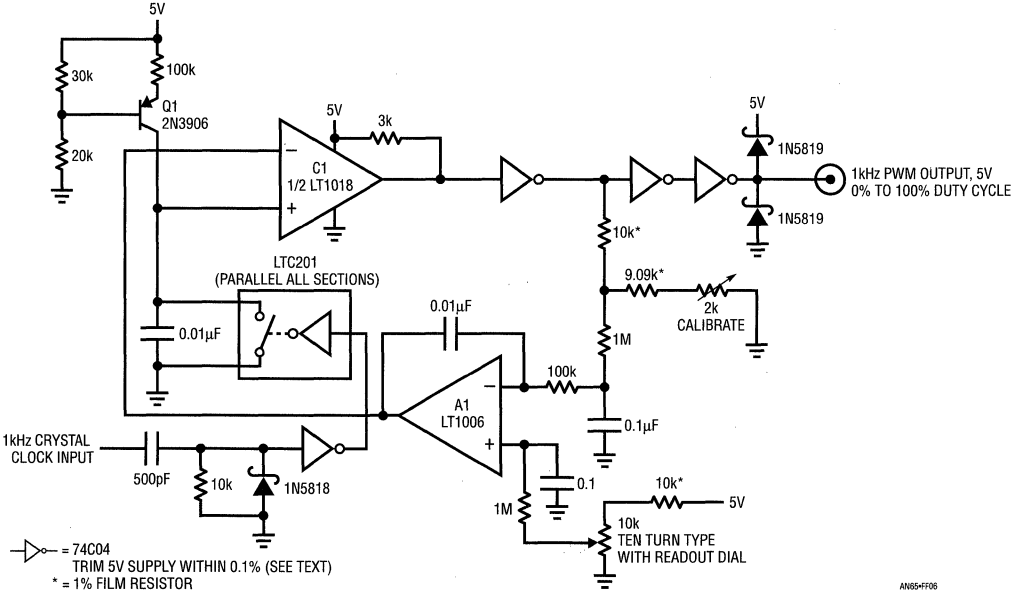


Figure F6. The Calibrated Pulse Width Test Box. A1 Controls C1-Based Pulse Width Modulator, Stabilizing Its Operating Point

APPENDIX G

LAYOUT, COMPONENT AND EMISSIONS CONSIDERATIONS

The CCFL circuits described in the text are remarkably tolerant of layout and impedance in supply lines. This is due to the Royer's relatively continuous current drain over time. Some review of current flow is, however, worthwhile. Figure G1 shows the more critical paths in thick lines for switching regulator-based CCFL circuits. In actual layout, these traces should be reasonably short and thick. The most critical consideration is that C1, T1's center tap and the diode should be connected *directly* together with minimum trace area between them. Similarly, C2 should be near the V_{IN} pin, although this placement is not nearly as critical as C1's.

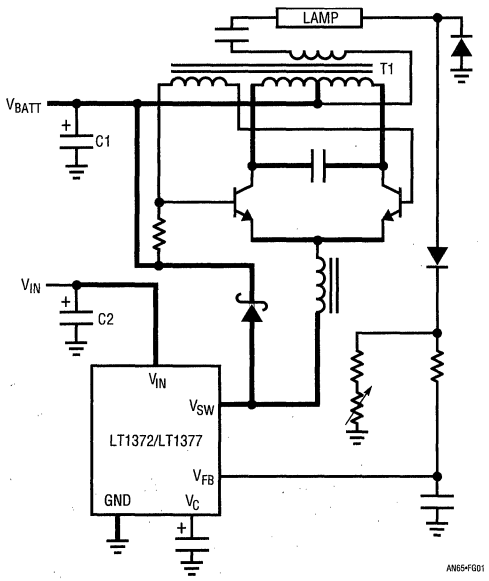


Figure G1. Thick Lines Denote PC Traces Requiring Low Impedance Layout in LT1172/LT1372 Type CCFL Circuits. Bypass Capacitors Associated with These Paths Should Be Mounted Near Load Point

Figure G2 indicates similar layout treatment for LT118X-based circuits. As before, the Royer and V_{IN} bypass capacitors should be near their respective load points, with the diode in close proximity to the Royer center tap.

Circuit Segmenting

In cases where space is extremely limited it may be desirable to physically segment the circuit. Some designs have placed a section of the circuit near the display with another portion remotely located. The best place for segmenting is the junction of the Royer transistor emitters and the inductor (Figure G3). Introducing a long, relatively lossy connection at this point imposes no penalty because signal flow into the inductor closely resembles a constant current source.

There are no wideband components due to the inductor's filtering effect. Figure G4 shows emitter voltage (Trace A) and current (Trace B) waveforms. There is no wideband component or other significant high speed energy movement. The inductor current waveform trace thickening due to Royer and switching regulator frequency mixing is not deleterious.

A very special case of segmentation involves replacing the transformer with two smaller units. Aside from space (particularly height) savings, electrical advantages are also realized. See Appendix I for details.

High Voltage Layout

Special attention is required for the board's high voltage sections. Board leakage, which can increase dramatically over life due to condensation cycling and particulate matter trapping, must be minimized. If precautions are not taken leakage will cause degraded operation, failures or destructive arcing. The only sure way to eliminate these possibilities is to *completely isolate the high voltage points from the circuit.* Ideally, no high voltage point should be within 0.25" of any conductor. Additionally, moisture trapping due to condensation cycling or improper board washing can be eliminated by routing the

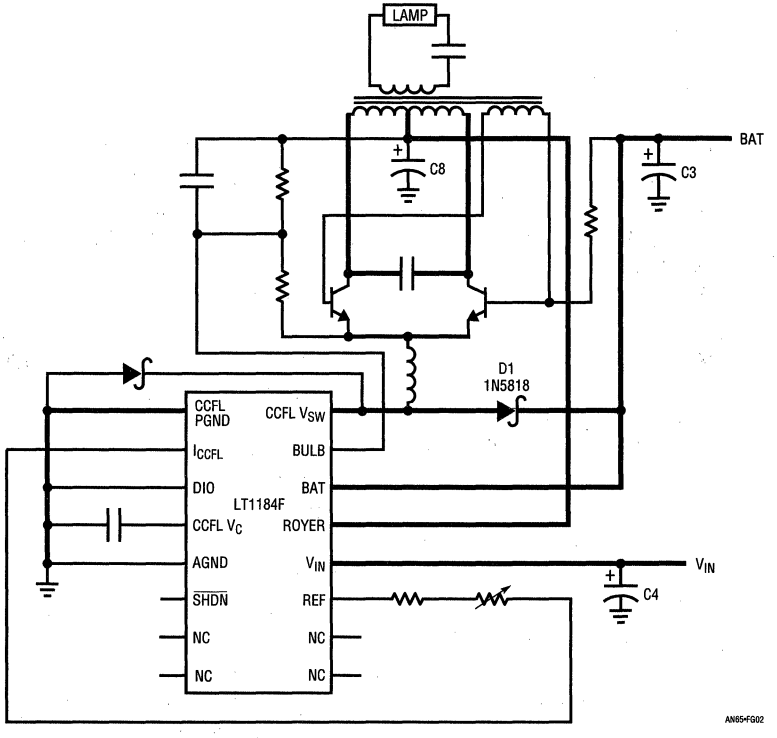


Figure G2. Critical Current Paths for LT118X Type Circuits. Thick Lines Denote PC Traces Requiring Low Impedance. Bypass Capacitors Associated with These Paths Should Be Near Load Points

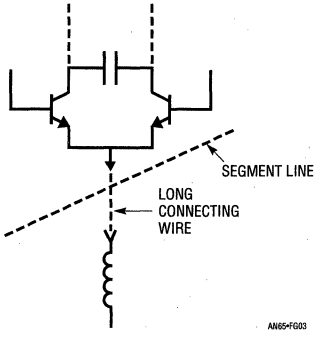


Figure G3. CCFL Circuit May Be Segmented in Limited Space Applications. Breaking at Emitter/Inductor Junction Imposes No Penalty

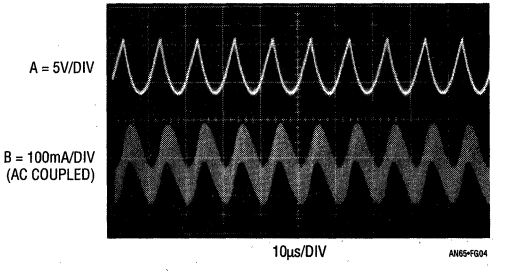


Figure G4. Royer Emitter/Inductor Junction Is Ideal Point for Segmenting CCFL Circuit. Voltage (Trace A) and Current (Trace B) Waveforms Contain Little High Frequency Content. Trace Thickening of Current Waveform Is Due to Frequency Mixing in Inductor

area under the transformer. This treatment, standard technique in high voltage layout, is strongly recommended. In general, carefully evaluate all high voltage areas for possible leakage or arcing problems due to layout, board manufacturing or environmental factors. Clear thinking is needed to avoid unpleasant surprises. The following commented photographs, visually summarizing the above discussion, are examples of high voltage layout.

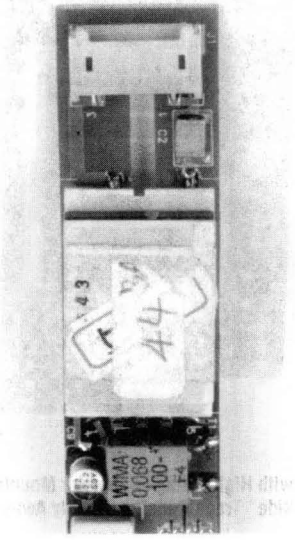


Figure G5. Transformer Output Terminals, Ballast Capacitor and Connector Are Isolated at End of Board. Slit Prevents Leakage

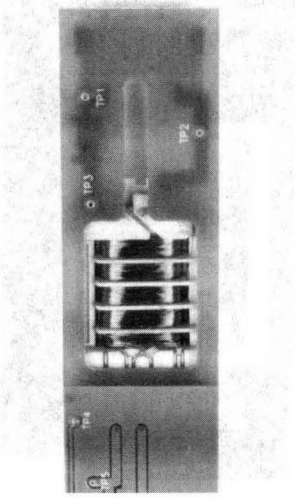


Figure G6. Reverse Side of G5. Note Routed Area under Transformer, Eliminating Possibility of Moisture or Contaminant Trappings

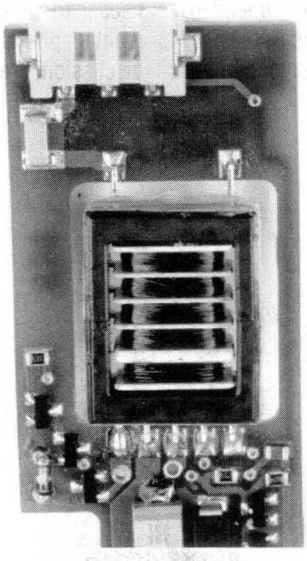


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Figure G7. A Fully Routed Transformer, with High Voltage Capacitor Mounted Well Away from Transformer Ground Terminal (Right). Note Connector "Low Side" Trace Running Directly Away from High Voltage Points

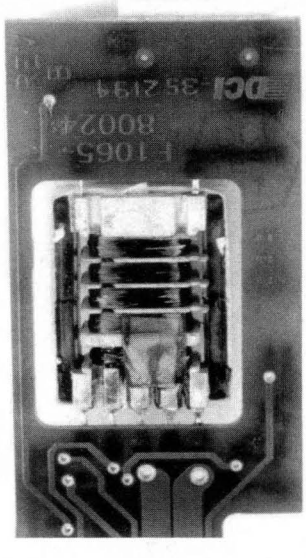

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Figure G8. Routing Detail of Figure G7's Reverse Side. Transformer Header Sits Inside Routed Area, Saving Height Space. Board Markings Are Allowable Because HV Contacts Do Not Plate Through and Board Dielectric Strength Is Known

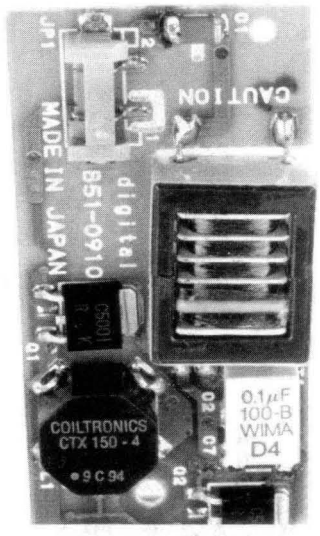


Figure G9. Very Thorough Routing Treatment Breaks Up Leakage. Routing Under Ballast Capacitor and Around Connector "Low Side" Pin Allows Tight Layout

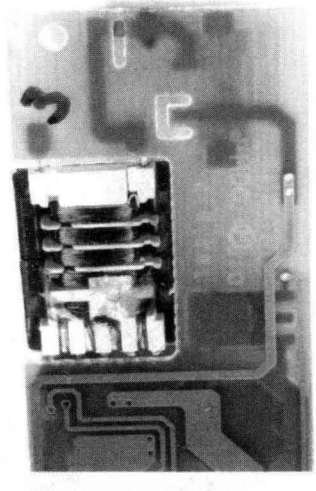


Figure G10. Reverse Side of G9 Shows Offset Transformer Placement Necessitated by Packaging Restrictions. Transformer Header Sits in Routed Area, Minimizing Overall Board Height

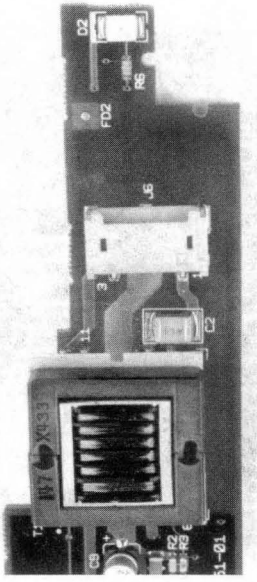


Figure G11. Topside of Board Shows Isolation Slit Running to the HV Connector

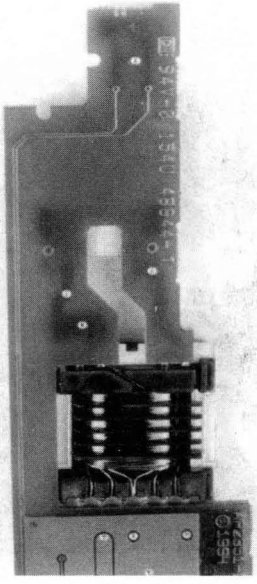


Figure G12. Bottom of G11 Shows Routed Area. Traces at Board Extreme Left Are Undesirable but Acceptable. Isolation Slit Between Traces and HV Points Would Be Preferable

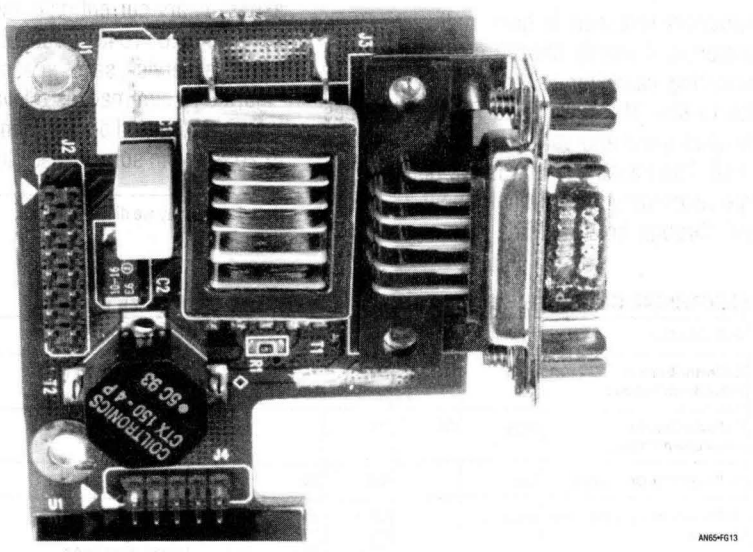


Figure G13. A Disaster. Cross-Hatched Ground Plane Surrounds Output Connector and High Voltage Transformer Pins (Upper Center) in This Computer "Aided" Layout. Board Failed Spectacularly at Turn-On

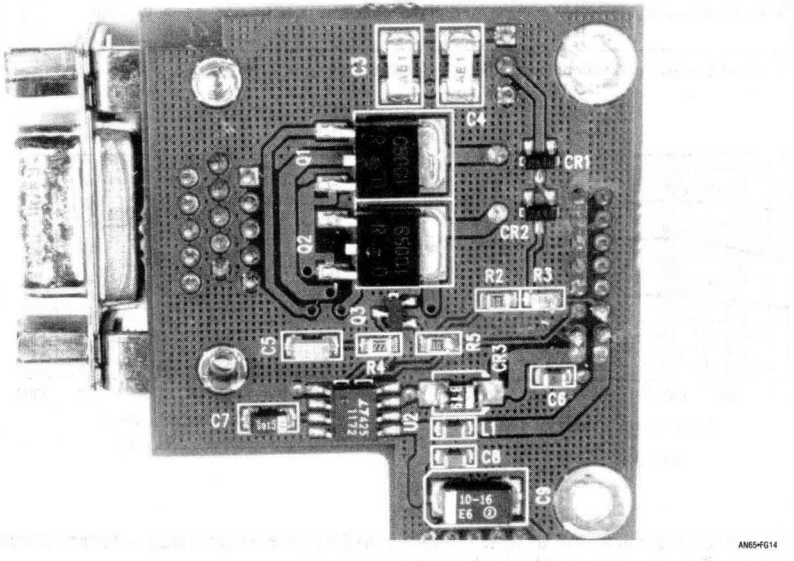


Figure G14. Bottom Side of G13. Ground Plane in Region of Paralleled Ballast Capacitors (Upper Center) Caused Massive Arcing at Turn-On. Board Needs Complete Re-Layout. Computer Layout Software Package Needs E and M Course

Discrete Component Selection

Discrete component selection is quite critical to CCFL circuit performance. A poorly chosen dielectric for the collector resonating capacitor can easily degrade efficiency by 5% to 8%. The WIMA and Panasonic types specified are quite good and very few other capacitors perform as well. The Panasonic unit is the only surface mounting type recommended although about 1% more lossy than the "through-hole" WIMA.

The transistors specified are quite special. They feature extraordinary current gain and V_{CE} saturation specifications. The ZDT1048, a dual unit designed specifically for backlight service, saves space and is the preferred device. Figure G15 summarizes relevant characteristics. Substitution of standard devices can degrade efficiency by 10% to 20% and in some cases cause catastrophic failures.[1]

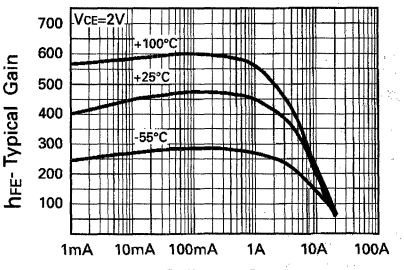
Note 1: Don't say we didn't warn you.

ELECTRICAL CHARACTERISTICS (at T_{amb} = 25°C unless otherwise stated).

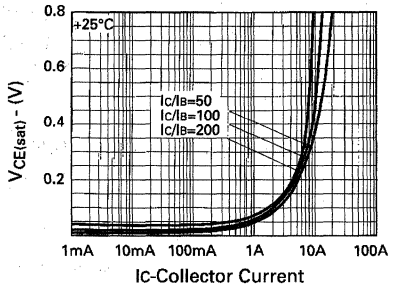
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS.
Collector-Emitter Breakdown Voltage	V_{CES}	50	85		V	I_C=100µA
Collector-Emitter Breakdown Voltage	V_{CEV}	50	85		V	I_C=100µA, V_{EB}=1V
Collector Cut-Off Current	I_{CBO}		0.3	10	nA	V_{CB}=35V
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$		27 55 120 200 250	45 75 160 240 350	mV mV mV mV mV	I_C=0.5A, I_B=10mA* I_C=1A, I_B=10mA* I_C=2A, I_B=10mA* I_C=5A, I_B=100mA* I_C=5A, I_B=20mA*
Static Forward Current Transfer Ratio	h_{FE}	280 300 300 250 50	440 450 450 300 80	1200		I_C=10mA, V_{CE}=2V* I_C=0.5A, V_{CE}=2V* I_C=1A, V_{CE}=2V* I_C=5A, V_{CE}=2V* I_C=20A, V_{CE}=2V*
Transition Frequency	f_T		150		MHz	I_C=50mA, V_{CE}=10V f=50MHz

*Measured under pulsed conditions. Pulse width=300µs. Duty cycle ≤ 2%

ZETEX
U.K. FAX: 0161627-5467
U.S. FAX: 5168647630
HONG KONG FAX: 987 9595



hFE v Ic



VCE(sat) v Ic

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Figure G15. Short Form Specifications for Zetex ZDT1048 Dual Transistor. Extraordinary Beta and Saturation Characteristics Are Ideal for Royer Converter Section of Backlight Circuits

The following section, excerpted with permission from Zetex Application Note 14 (see Reference 28), reviews Royer circuit operation with emphasis on transistor operating conditions and requirements.

Excerpted from "Transistor Considerations for LCD Backlighting," Neil Chadderton, Zetex plc.

Basic Operation Of Converter

The drive requirements dictated by the CCFL tube's behaviour and preferred operating conditions can be achieved by the resonant push-pull converter shown in FigureG16.This is also referred to as the Royer Converter, after G.H. Royer who proposed the topology in 1954 as a power converter. (Note: Strictly speaking the backlighting converter uses a modified version of the Royer converter – the original used a saturating transformer to fix the operating frequency, and therefore produced a squarewave drive waveform). The circuit looks simple but this is very deceptive: many components interact, and while the circuit is capable of operation with widely varying component values, (useful during development) optimisation is required for each design to achieve the highest possible efficiencies.

Transistors Q1 and Q2 are alternatively saturated by the base drive provided by the feedback winding W4. The base current is defined by resistors R1 and R2. Supply inductor L1 and primary capacitance C1 force the circuit to run sinusoidally thereby minimising harmonic generation and RFI, and providing the preferred drive waveform to the load. Voltage step-up is achieved by the W1:(W2+W3) turns ratio. C2 is the secondary winding ballast capacitor, and effectively sets the tube current.

Prior to the tube striking, or when no tube is connected, the operating frequency is set by the resonant parallel circuit comprising the primary capacitance C1, and the transformer's primary winding W2+W3. Once the tube has struck, the ballast capacitor C2 plus distributed tube and parasitic capacitances are reflected back through the transformer, and the operating frequency is lowered.

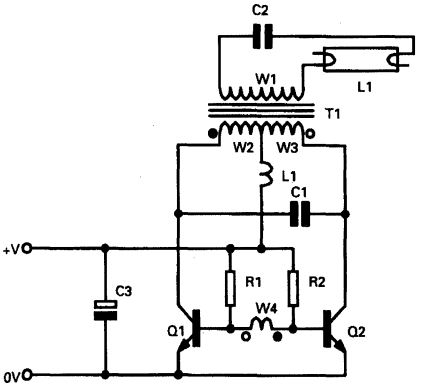


Figure G16. Generalised Royer Converter.

The secondary load can become dominant in circuits with a high transformer turns ratio, Eg. those designed to operate from very low DC input voltages.

Each transistor's collector is subject to a voltage= 2 x $\pi/2$ x V_S, (or just π x V_S) where V_S is the DC input voltage to the converter. (The $\pi/2$ factor being due to the relationship between average and peak values for a sinewave, and the x2 multiplier being due to the 2:1 autotransformer action of the transformer's centre-tapped primary). This primary voltage is stepped up by the transformer turns ratio Ns:Np, to a high enough level to reliably strike the tube under all conditions:- starting voltage is dependent on display housing, location of ground planes, tube age, and ambient temperature.

The basic converter shown in Figure G16 is a valid and useful circuit that has been utilised for many systems and indeed offered as a sub-system by several manufacturers.

Requisite Transistor Characteristics

The relatively low operating frequency as required by the backlighting Royer Converter (to minimise HV parasitic capacitance losses), and the ease of transformer drive, makes this circuit particularly suitable for bipolar transistor implementation. This isn't to exclude MOSFET based designs (some IC vendors have specified MOS as this suits their technology) but in terms of equivalent on-resistance and silicon efficiency, the low voltage bipolar device has no equal. For example, the ZETEX ZTX849 E-LINE (TO-92 compatible) transistor exhibits a $R_{CE(sat)}$ of 36mΩ. This can only be matched by a much larger (and expensive) MOSFET die, only available in TO-220, D-PAK, and similar larger packages.

The most important transistor characteristics are voltage rating, $V_{CE(sat)}$, and h_{FE}, and are considered in some detail below.

The voltage rating required deserves some thought with respect to the standard transistor breakdown parameters, as it is possible to over-specify a device on grounds of voltage rating, and thereby incur a reduction in efficiency due to unnecessary on-resistance losses. The primary breakdown voltage BV_{CBO}, of a planar bipolar transistor depends on the epitaxial layer - specifically it's thickness and resistivity. The breakdown voltage of most interest to the designer is usually that attained across the Collector-Emitter (C-E) terminals. This value can vary between the primary breakdown BV_{CBO} and a much lower voltage dependent on the state of the base terminal bias.

[The breakdown mechanism is caused by the avalanche multiplication effect, whereby free electrons can be imparted with sufficient energy by the reverse bias electric field such that any collisions can lead to ionisation of the lattice atoms. The free electrons thus generated are then accelerated by the field and produce further ionisation. This multiplication of free carriers increases the reverse current dramatically, and so the junction effectively clamps the applied voltage. The base terminal can obviously influence the junction current – thereby modulating the voltage required for a breakdown condition.]

Figure G17 shows how the breakdown characteristic is seen to vary for different circuit conditions. The BV_{CEO} rating (or when the base is open circuit) allows the Collector-Base (C-B) leakage current I_{CBO} to be effectively amplified by the transistor's β thus significantly increasing the leakage component to I_{CEO}. Shorting the base to the Emitter (BV_{CES}) provides a parallel path for the C-B leakage, and so the voltage required for breakdown is higher than the open base condition. BV_{CER} denotes the case between the open and shorted base options:- R indicating an external base-emitter resistance, the value of which is typically 100 to 10kΩ. BV_{CEV} or BV_{CEX} is a special case where the base-emitter is reverse biased; this can provide a better path for the C-B leakage, and so this rating yields a voltage close to, or coincident with the BV_{CBO} value. Figure G18 shows a curve tracer view of the relevant breakdown modes of the ZTX849 transistor, including a curve showing the device in the "on" state. Curves 1 and 2 are virtually coincident and show BV_{CBO} and BV_{CES} respectively. Curve 3 shows the BV_{CEV} case with an applied base bias (V_{EB}) of -1V. Curve 4 shows BV_{CEO} at approximately 36V. Curve 5 is a BV_{CE} curve, showing how the breakdown condition is affected by a positive base bias of 0.5V.

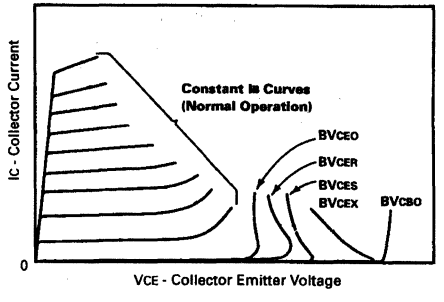


Figure G17. Voltage Breakdown Modes of Bipolar

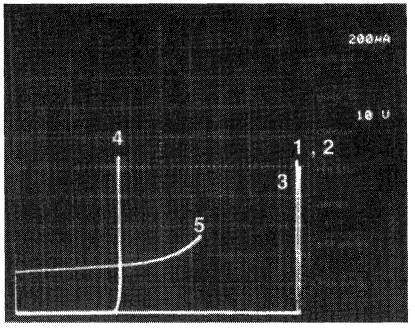


Figure G18. Breakdown Modes of ZTX849.

The BV_{CEV} rating has particular relevance to the Royer Converter, as can be surmised from Figure 19. Examination of this will show that the transistor only experiences the high C-E voltage when the base voltage has been taken negative by the feedback winding, these events of course being in perfect synchronism. An expanded view of the C-E and B-E waveforms is shown in Figure G20.

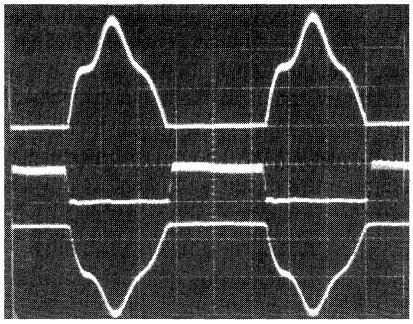


Figure G19. Royer Converter Operating Waveforms: V_{CE} 10V/div; I_E 0.5A/div; V_{BE} 2V/div respectively, 2µs/div horizontal

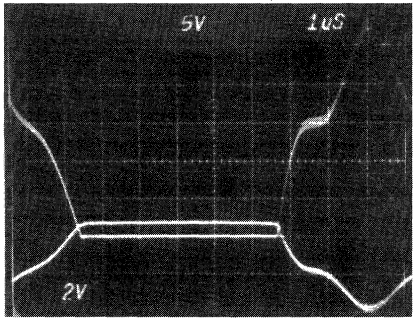


Figure G20. Royer Converter: V_{CE} and V_{BE} Waveforms; 5V/div and 2V/div respectively.

[Note: The voltage applied by the feedback winding must not exceed the BV_{EBO} of the transistor. This is specified at 5V usually, against an actual of 7.5 to 8.5V].

The $V_{CE(sat)}$ and h_{FE} parameters have a direct bearing on the circuit's electrical conversion efficiency. This is especially true of low voltage battery powered systems, due to the high current levels involved. Selection of standard LF amplifier transistors provides far from ideal results; these parts are for general purpose linear and non-critical switching use only. The high $V_{CE(sat)}$ inherent to these parts, and low current gain could reduce circuit efficiency to less than 50%. For example, the stated $V_{CE(sat)}$ maximum measured at 500mA, for the FZT849 SOT223 transistor, and a LF device sometimes quoted as a suitable Royer Converter transistor are 50mV and 0.5V respectively. Eg.

	$V_{CE(sat)}$	@Ic	Ib
FZT849	50mV	0.5A	20mA
BCP56	0.5V	0.5A	50mA

To address the $V_{CE(sat)}$ issue, large power transistors are occasionally specified. Unfortunately their capacitance, and characteristic low base transport factor (a feature of Epitaxial Base devices) can lead to problems with cross-conduction losses due to long storage and switching times. The current gain is also important, as the losses in the base bias can be significant to the overall figure; judicious selection of the bias resistor to ensure a minimum $V_{CE(sat)}$ while preventing base overdrive needs to consider supply variation, maximum lamp current, and transistor h_{FE} minimum value and range.

For the above reasons, transistors designed and optimised for high current switching applications offer the most cost-effective and efficient solutions. Figure G21 shows the $V_{CE(sat)}$ exhibited by the ZTX1048A for a range of forced gain values. This device is one of the ZTX1050 series of transistors that employ a scaled up variant of the highly efficient Matrix geometry, developed for the ZETEX "Super-SOT" series. This enables a $V_{CE(sat)}$ performance similar to the ZTX850 series at the low to moderate currents relevant to this application, though utilising a smaller die, and therefore providing a cost and possibly a space saving advantage.

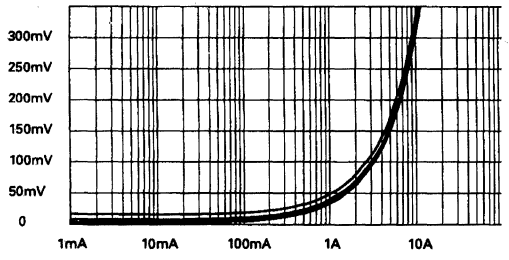


Figure G21. $V_{CE(sat)}$ v I_C for the ZTX1048A Forced gains of 10,20,50,100.

Additional Discrete Component Considerations

The magnetics specified have also been carefully selected and substitution can lead to problems ranging from poor efficiency to bad line regulation.

Bypass capacitors can be any type specified for switching regulator service, although tantalum types should be avoided for Royer bypassing if the supply is capable of delivering high current. As of this writing no tantalum supplier can guarantee reliability in the face of high current turn-on. If tantalums must be used, an X2 voltage derating factor *must* be enforced.[2]

The 2.2µF Royer bypass value used in LT118X-based circuits has been selected to ensure against any possible long-term damage to the IC's internal current shunt. Turn-on current surges can be large and this value limits them to safe excursions.

The high speed catch diode associated with the V_{SW} pin should be capable of handling the fast current spikes encountered. Schottky types offer lower loss than regular high speed units.[3]

Emissions

There are rarely emission problems with the CCFL circuits. The Royer circuit's resonant operation minimizes radiated energy at frequencies of interest. There is often more RF energy associated with the switching regulators V_{SW} node and minimizing exposed trace area eliminates problems. Incidental radiation from magnetics is reasonably low. Some (relatively rare) cases require consideration of magnetics placement to prevent interaction with other circuitry. If shielding is required its effects should be evaluated early in the design. Shielding in the vicinity of the Royer transformer can cause effects ranging from changing the inverter resonance to secondary arcing.

Note 2: See Footnote 1. Read it twice.
Note 3: Discussing utilization of 60Hz rectifier diodes (e.g., 1N4002) in this application qualifies as obscene literature. See also Footnote 1.

APPENDIX H

LT1172 OPERATION FROM HIGH VOLTAGE INPUTS

Some applications require higher input voltages. The 20V maximum input specified in the figures is set by the LT1172 going into its isolated flyback mode (see LT1172 data sheet), not breakdown limits. If the LT1172 V_{IN} pin is driven from a low voltage source (e.g., 5V) the 20V limit may be extended by using Figure H1's network. If the LT1172 is driven from the same supply as L1's center tap, the network is unnecessary, although efficiency will suffer. No other switching regulator discussed in the text is subject to this issue. Their operating voltage is set solely by voltage breakdown limits.

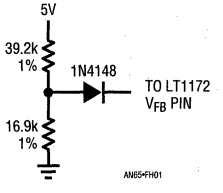


Figure H1. Network Allows LT1172 Operation Beyond 20V Inputs

APPENDIX I

ADDITIONAL CIRCUITS

Desktop Computer CCFL Power Supply

Desktop computers, being line operated, can support higher power displays. High power operation permits high luminosity, enlarged display area or both. Typically, desktop displays absorb 4W to 6W and run from a relatively high voltage, regulated supply. Figure I1 shows such a display. This "grounded lamp" LT1184-based configuration, similar to previously described versions, requires little comment. The transformer is a high power type, and scaling of the "I_{CCFL}" current programming resistors allows 9mA lamp current. In this case programming is via clamped PWM (see Appendix F), although all other methods described are feasible.

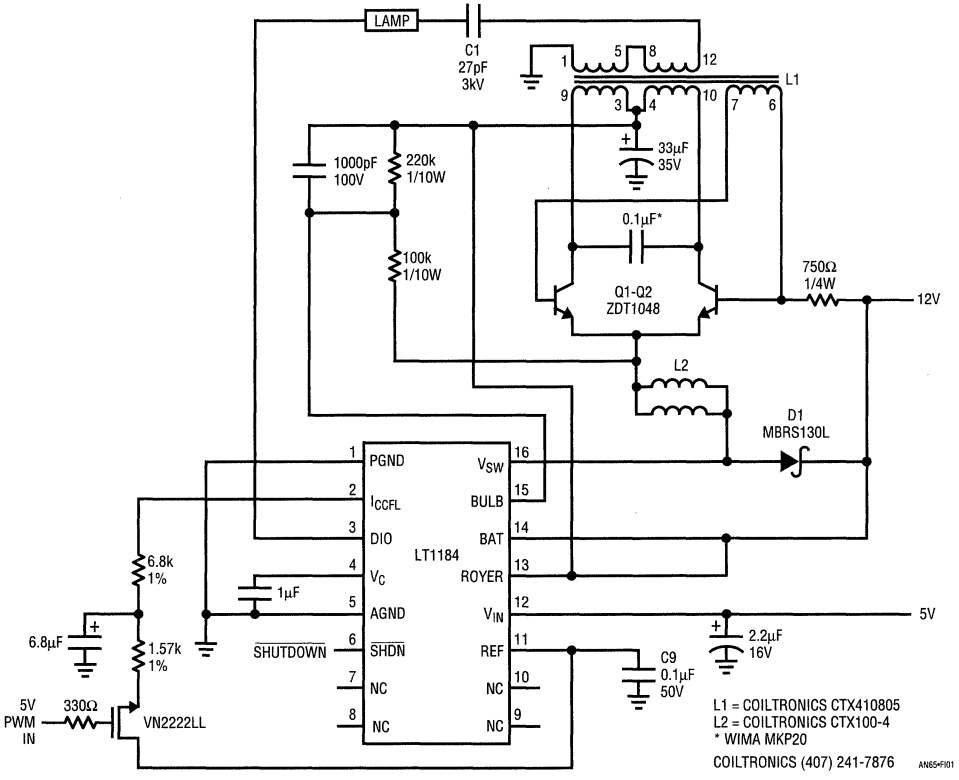


Figure I1. High Power Transformer and Scaled I_{CCFL} Values Permit Desktop Computer LCD Operation

Dual Transformer CCFL Power Supply

Space constraints may dictate utilization of two small transformers instead of a single, larger unit. Although this approach is somewhat more expensive, it can solve space problems and offers other attractive advantages. Figure I2's approach is essentially a "grounded lamp" LT1184-based circuit. The transistors drive two transformer primaries in parallel. The transformer secondaries, stacked in series, provide the output. The relatively small transformers, each supplying half the load power, may be located directly at the lamp terminals. Aside from the obvious space advantage (particularly height), this arrangement minimizes parasitic wiring losses by eliminating high voltage lead length. Additionally, although the lamp receives differential drive, with its attendant low parasitic losses, the feedback signal is ground referred. Thus, the stacked secondaries afford floating lamp operation efficiency with grounded mode current certainty and line regulation.

L1 is directly driven, with winding 4-5 furnishing feedback in the normal fashion. L3, "slaved" to L1, produces phase-opposed output at its secondary. L1's and L3's interconnects must be laid out for low inductance to maintain waveform purity. The traces should be as wide as possible (e.g., 1/8") and overlaid to cancel inductive effects.

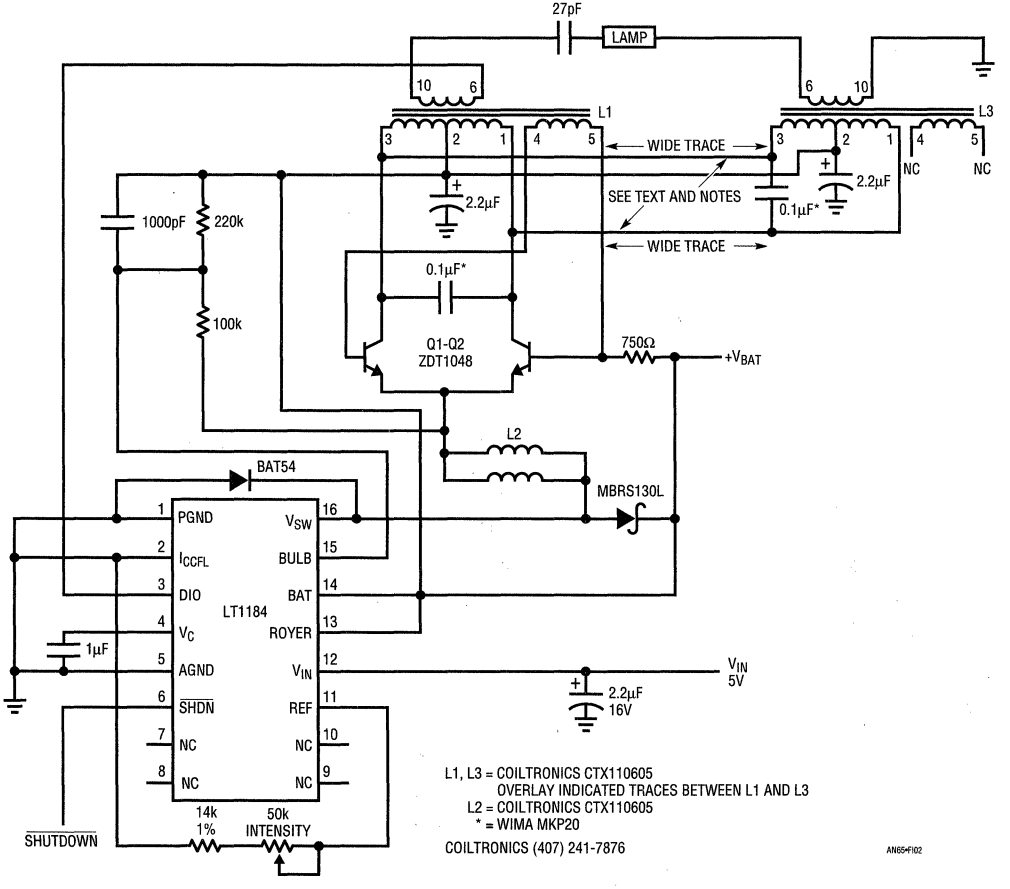


Figure I2. Dual Transformers Save Space and Minimize Parasitic Losses While Maintaining Current Accuracy and Line Regulation. Trade-Off Is Increased Cost

HeNe Laser Power Supply

Helium-neon lasers, used for a variety of tasks, are difficult loads for a power supply. They typically need almost 10kV to start conduction, although they require only about 1500V to maintain conduction at their specified operating currents. Powering a laser usually involves some form of start-up circuitry to generate the initial breakdown voltage and a separate supply for sustaining conduction. Figure 13's circuit considerably simplifies driving the laser. The start-up and sustaining functions have been combined into a single closed-loop current source with over 10kV of compliance. The circuit is recognizable as a reworked CCFL power supply with a voltage tripled DC output.

When power is applied, the laser does not conduct and the voltage across the 190Ω resistor is zero. The LT1170 switching regulator FB pin sees no feedback voltage, and its Switch pin (V_{SW}) provides full duty cycle pulse width modulation to L2. Current flows from L1's center tap through Q1 and Q2 into L2 and the LT1170. This current flow causes Q1 and Q2 to switch, alternately driving L1. The 0.47µF capacitor resonates with L1, providing boosted sine wave drive. L1 provides substantial step-up, causing about 3500V to appear at its secondary. The capacitors and diodes associated with L1's secondary form a voltage tripler, producing over 10kV across the laser. The laser breaks down and current begins to flow through it. The 47k

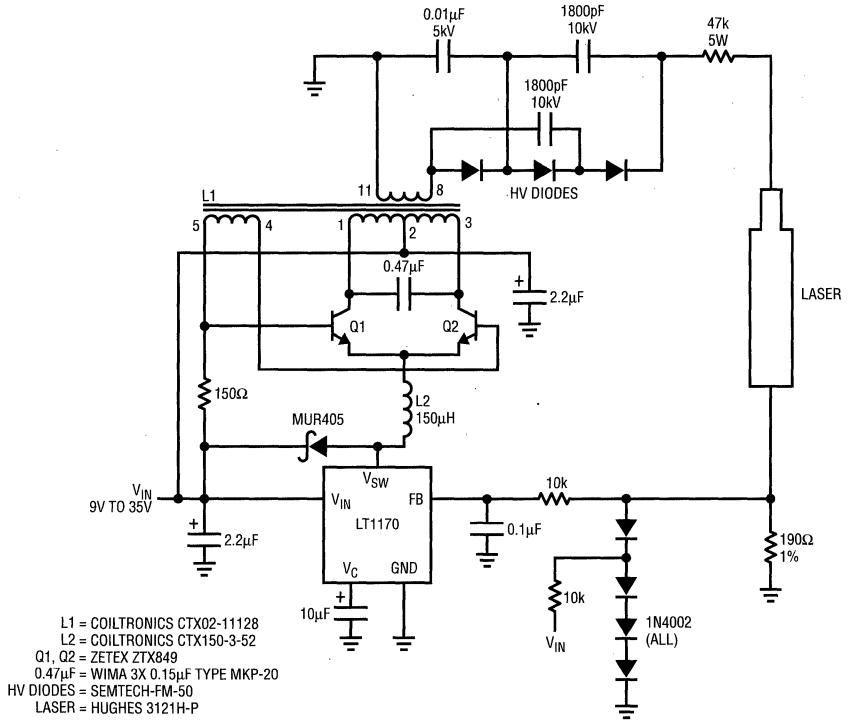


Figure 13. Laser Power Supply, Based on the CCFL Circuit, Is Essentially a 10,000V Compliance Current Source

resistor limits current and isolates the laser's load characteristic. The current flow causes a voltage to appear across the 190Ω resistor. A filtered version of this voltage appears at the LT1170 FB pin, closing a control loop. The LT1170 adjusts pulse width drive to L2 to maintain the FB pin at 1.23V, regardless of changes in operating conditions. In this fashion, the laser sees constant current drive, in this case 6.5mA. Other currents are obtainable by varying the 190Ω value. The 1N4002 diode string clamps excessive voltages when laser conduction first begins, protecting the LT1170. The 10µF capacitor at the V_C pin frequency compensates the loop and the MUR405 maintains L1's current flow when the LT1170 V_{SW} pin is not conducting. The circuit will start and run the laser over a 9V to 35V input range with an electrical efficiency of about 80%.

APPENDIX J

LCD CONTRAST CIRCUITS

LCD panels require variable output contrast control circuits. Contrast power supplies of various capabilities are presented here.

Figure J1 is a contrast supply for LCD panels. It was designed by Steve Pietkiewicz of LTC. The circuit is noteworthy because it operates from a 1.8V to 6V input, significantly lower than most designs. In operation the LT1300/LT1301 switching regulator drives T1 in flyback fashion, causing negative biased step-up at T1's secondary. D1 provides rectification, and C1 smooths the output to DC. The resistively divided output is compared to a command input, which may be DC or PWM, by the IC's I_{LIM} pin. The IC, forcing the loop to maintain 0V at the I_{LIM} pin, regulates circuit output in proportion to the command input.

Efficiency ranges from 77% to 83% as supply voltage varies from 1.8V to 3V. At the same supply limits, available output current increases from 12mA to 25mA.

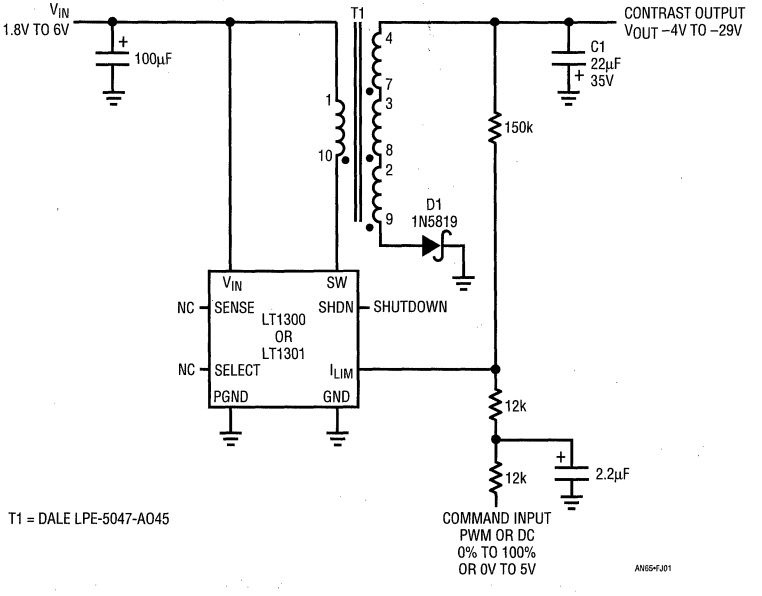


Figure J1. Liquid Crystal Display Contrast Supply Operates from 1.8V to 6V with –4V to –29V Output Range

Another LCD bias generator, also developed by Steve Pietkiewicz of LTC, is shown in Figure J2. In this circuit U1 is an LT1173 micropower DC/DC converter. The 3V input is converted to 24V by U1's switch, L2, D1 and C1. The Switch pin SW1 also drives a charge pump composed of C2, C3, D2 and D3 to generate –24V. Line regulation is less than 0.2% from 3.3V to 2V inputs. Load regulation, although suffering somewhat since the –24V output is not directly regulated, measures 2% from a 1mA to 7mA load. The circuit will deliver 7mA from a 2V input at 75% efficiency.

If greater output power is required, Figure J2's circuit can be driven from a 5V source. R1 should be changed to 47Ω and C3 to 47µF. With a 5V input, 40mA is available at 75% efficiency. Shutdown is accomplished by bringing D4's anode to a logic high, forcing the feedback pin of U1 to go above the internal 1.25V reference voltage. Shutdown current is 110µA from the input source and 36µA from the shutdown signal.

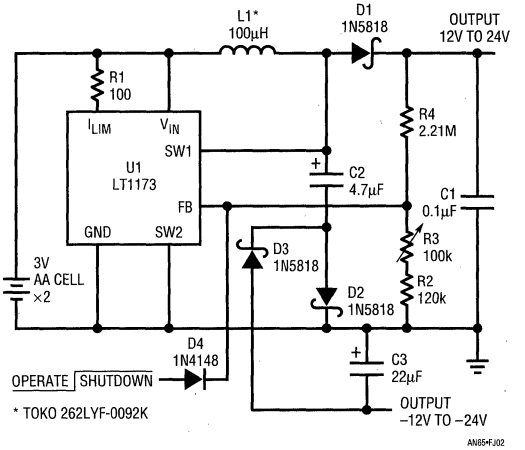


Figure J2. DC/DC Converter Generates LCD Bias from 3V Supply

Dual Output LCD Bias Voltage Generator

The many different kinds of LCDs available make programming LCD bias voltage at the time of manufacture attractive. Figure J3's circuit, developed by Jon Dutra of LTC, is an AC-coupled boost topology. The feedback signal is derived separately from the outputs, so loading does not affect loop compensation, although load regulation is somewhat compromised. With 28V out, from 10% to 100% load (4mA to 40mA), the output voltage sags about

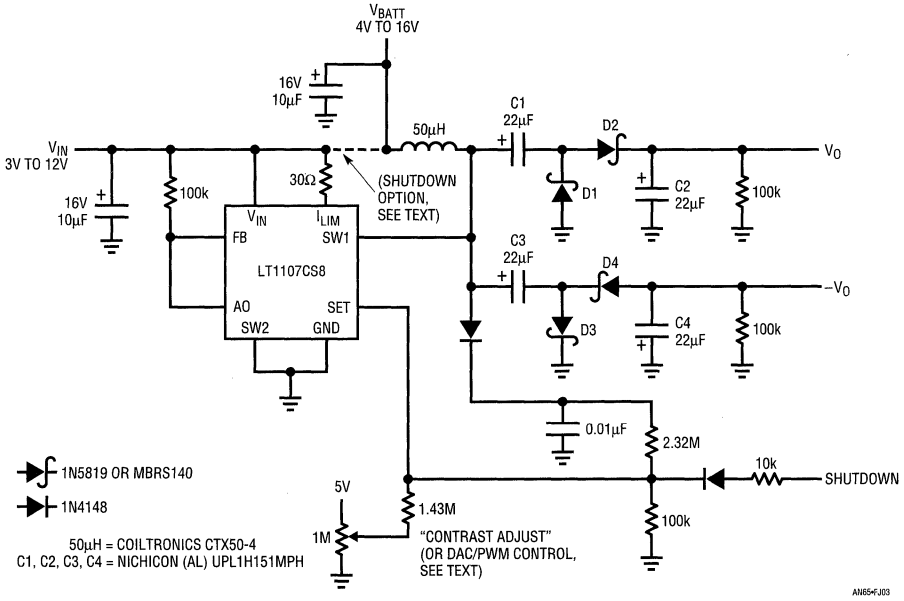


Figure J3. Dual Output LCD Bias Voltage Generator

0.65V. From 1mA to 40mA load the output voltage drops about 1.4V. This is acceptable for most displays.

Output noise is reduced by using the auxiliary gain block within the LT1107 (see LT1107 data sheet) in the feedback path. This added gain effectively reduces comparator hysteresis and tends to randomize output noise. Output noise is below 30mV over the output load range. Output power increases with V_{BATT}, from about 1.4W with $5V_{IN}$ to about 2W with 8V or more. Efficiency is 80% over a broad output power range. If only a positive or negative output voltage is required, the diodes and capacitors associated with the unused output can be eliminated. The 100k resistor is required on each output to load a parasitic voltage doubler created by D2/D4 shunt capacitance. Without this minimum load, the output voltage can rise to unacceptable levels.

The voltage at the Switch pin SW1 swings from 0V to V_{OUT} plus 2 diode drops. This voltage is AC-coupled to the positive output through C1 and D1, and to the negative output through C3 and D3. C1 and C3 have the full RMS output current flowing through them. Most tantalum capacitors are not rated for current flow. Use of a rated tantalum or electrolytic is recommended for reliability. At lower output currents monolithic ceramics are also an option.

The circuit may be shut down in several ways. The easiest is to pull the Set pin above 1.25V. This approach consumes 200µA in shutdown. A lower power method is to turn off V_{IN} to the LT1107 by a high side switch or simply disable the input supply (see option in schematic). This drops quiescent current from the V_{BATT} input below 10µA. In both cases V_{OUT} drops to 0V. In the event $+V_{OUT}$ does not need to drop to zero, C1 and D1 can be eliminated. The output voltage can be adjusted from any voltage above V_{BATT} to 46V. Output voltage can be controlled by the user with DAC, PWM or potentiometer control. Summing currents into the feedback node allows downward adjustment of output voltage.

LT118X Series Contrast Supplies

Some LT118X series parts include a contrast supply based on a boost regulator. Figure J4 shows a basic positive output circuit. The V_{SW}-driven inductor provides voltage step-up with D5 and C11 rectifying and filtering the output to DC. The R12/R14 divider chain sets feedback ratio and hence output voltage. The connection to the LT1182 Feedback pin closes a control loop with R7 and C8 providing frequency compensation.

Figure J5 is similar, except that it uses charge pump techniques to reduce shutdown current. D4 and C12 are placed in L3's discharge path, AC coupling it to the output. In shutdown, no DC current can flow through L3, reducing battery drain over J4's DC-coupled approach.

Figure J6's transformer-fed output provides negative output voltages with the LT1183's "FBN" pin directly accepting the resultant negatively biased feedback signal. No level shift is required. In this case output voltage is set by a voltage control input, although potentiometer or PWM inputs could be accommodated (see Appendix F). D3 and D2 damp L3 flyback amplitude to safe levels and the

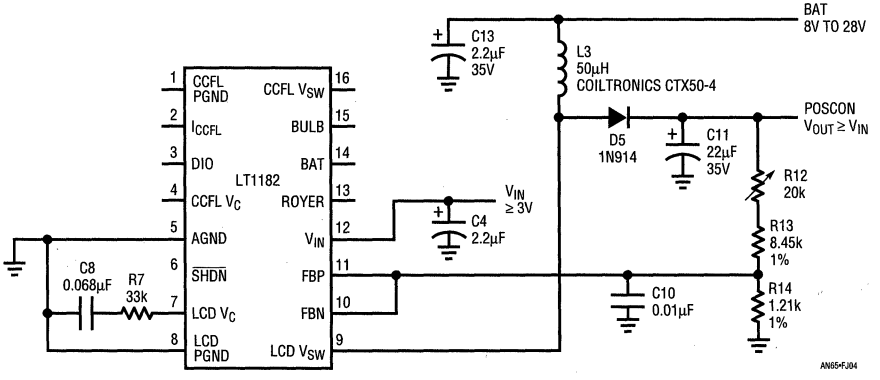


Figure J4. LT1182 LCD Contrast Positive Boost Converter. CCFL Circuitry Is Omitted for Clarity

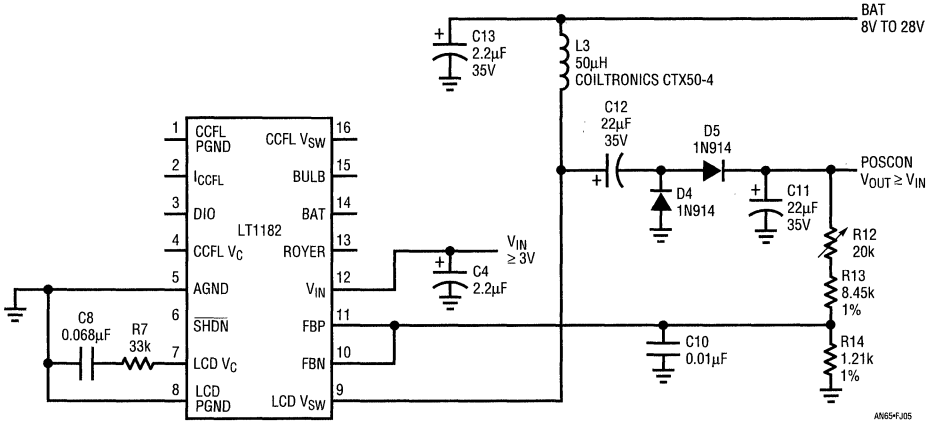


Figure J5. LT1182 LCD Contrast Positive Boost/Charge Pump Converter Reduces Battery Current in Shutdown

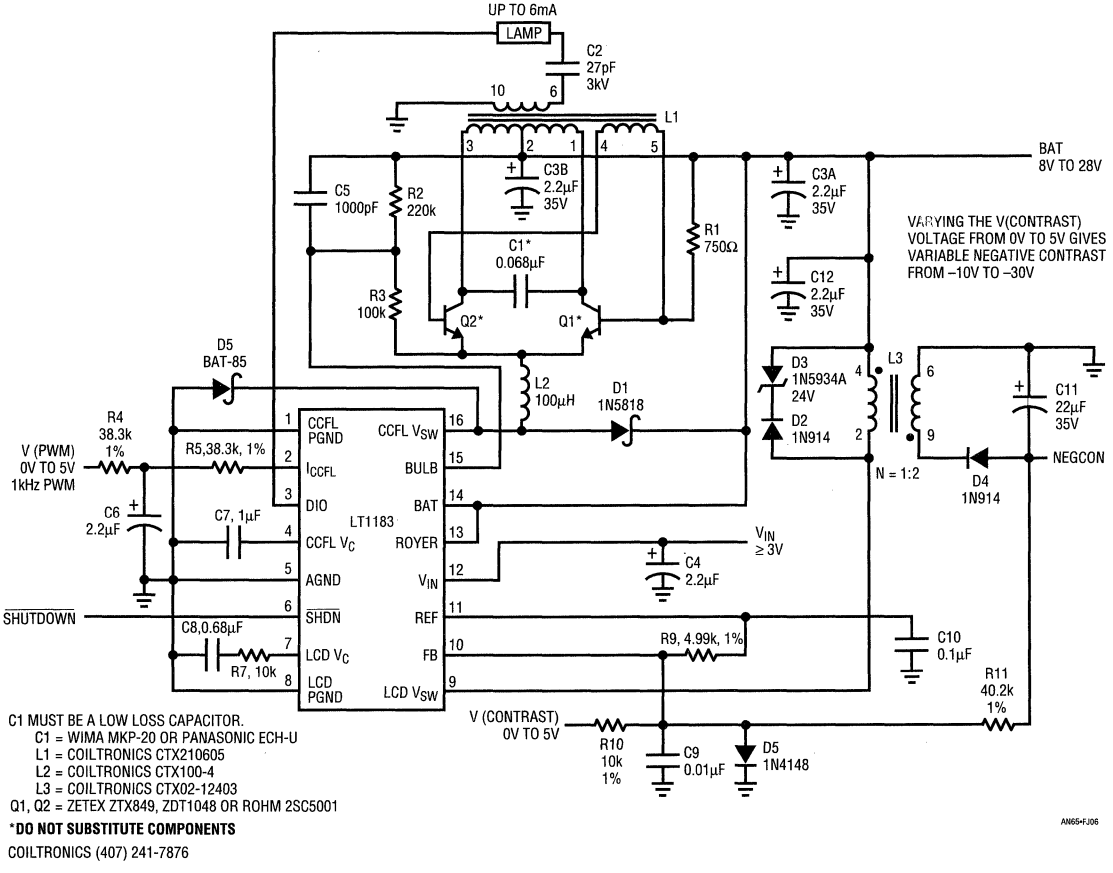


Figure J6. LT1183 Grounded Lamp CCFL Circuit with Negative Output LCD Contrast Supply

isolated secondary permits low shutdown current compared to a simple inductor-based circuit.

Figure J7 takes advantage of the LT1182's bipolar feedback inputs to provide selectable output polarity. This scheme permits the same circuit to be used with LCD's requiring either positive or negative bias. This can be a significant advantage in volume production involving different LCD panels. In operation the circuit is similar to Figure J6, except that L3's secondary winding feeds two separate feedback paths. Output polarity is selected by simply grounding the appropriate L3 secondary terminal.

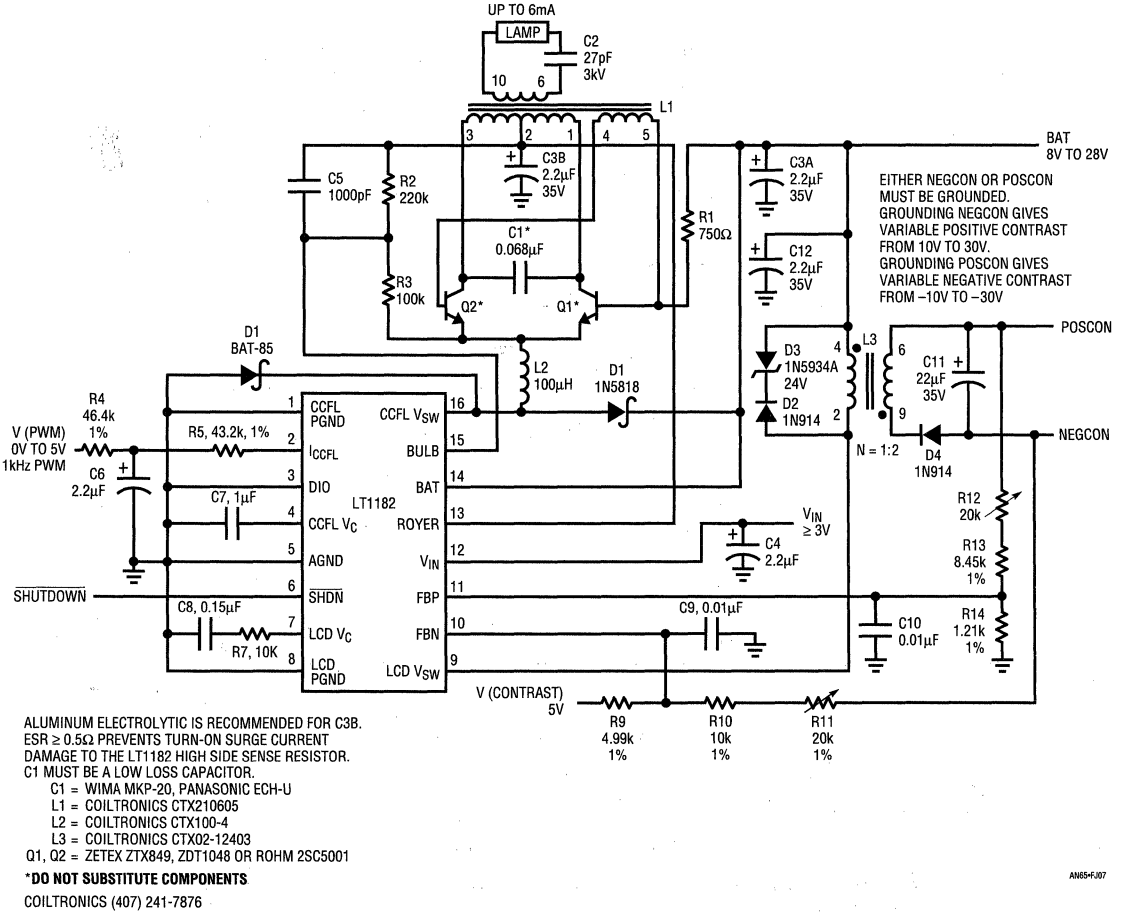


Figure J7. LT1182 Floating Lamp CCFL Circuit with Positive or Negative LCD Contrast Supply

APPENDIX K

WHO WAS ROYER AND WHAT DID HE DESIGN?

In December 1954 the paper "Transistors as On-Off Switches in Saturable-Core Circuits" appeared in *Electrical Manufacturing*. George H. Royer, one of the authors, described a "d-c to a-c converter" as part of this paper. Using Westinghouse 2N74 transistors, Royer reported 90% efficiency for his circuit. The operation of Royer's circuit is well-described in this paper. The Royer converter was widely adopted and used in designs from watts to kilowatts. It is still the basis for a wide variety of power conversion.

Royer's circuit is not an LC resonant type. The transformer is the sole energy storage element and the output is a square wave. Figure K1 is a conceptual schematic of a typical converter. The input is applied to a self-oscillating configuration composed of transistors, a transformer and a biasing network. The transistors conduct out of phase, switching (Figure K2, Traces A and C are Q1's collector and base, while Traces B and D are Q2's collector and base) each time the transformer saturates. Transformer saturation causes a quickly rising, high current to flow (Trace E).

This current spike, picked up by the base drive winding, switches the transistors. This phase opposed switching causes the transistors to exchange states. Current abruptly drops in the formerly conducting transistor and then slowly rises in the newly conducting transistor until saturation again forces switching. This alternating operation sets transistor duty cycle at 50%.

Figure K3 is a time and amplitude expansion of K2's Traces B and E. It clearly shows the relationship between transformer current (Trace B, Figure K3) and transistor collector voltage (Trace A, Figure K3).[1]

Note 1: The bottom traces in both photographs are not germane and are not referenced in the discussion.

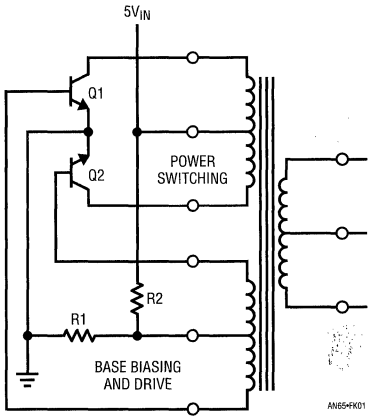


Figure K1. Conceptual Classic Royer Converter. Transformer Approaching Saturation Causes Switching

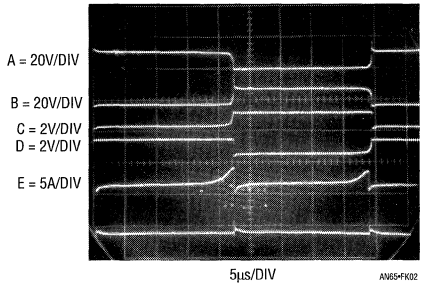


Figure K2. Waveforms for the Classic Royer Circuit

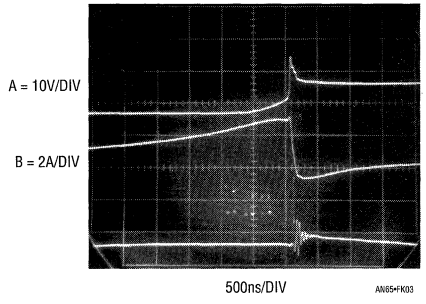


Figure K3. Detail of Transistor Switching. Turn-Off (Trace A) Occurs Just as Transformer Heads into Saturation (Trace B)

APPENDIX L

A LOT OF CUT OFF EARS AND NO VAN GOGHS

Some Not-So-Great Ideas

The hunt for a practical, broadly applicable and easily utilized CCFL power supply covered (and is still covering) a lot of territory. The wide range of conflicting requirements combined with ill-defined lamp characteristics produces plenty of unpleasant surprises. This section presents a selection of ideas that turned into disappointing breadboards. Backlight circuits are one of the deadliest places the author has ever encountered for theoretically interesting circuits.

Not-So-Great Backlight Circuits

Figure L1 seeks to boost efficiency by eliminating the LT1172's saturation loss. Comparator C1 controls a free running loop around the Royer by on-off modulation of transistor base drive. The circuit delivers bursts of high voltage sine drive to the lamp to maintain the feedback node. The scheme worked, but had poor line rejection due to the varying waveform vs supply seen by the RC averaging pair. Also, the "burst" modulation forces the loop to constantly restart the lamp at the burst rate, wasting energy. Finally, lamp power is delivered by a high crest factor waveform, causing inefficient current-to-light conversion in the lamp and shortening its life.

Figure L2 attempts to deal with some of these issues. It converts the previous circuit to an amplifier-controlled current mode regulator. Also, the Royer base drive is controlled by a clocked, high frequency pulse width modulator. This arrangement provides a more regular waveform to the averaging RC, improving line rejection. Unfortunately, the improvement was not adequate. To

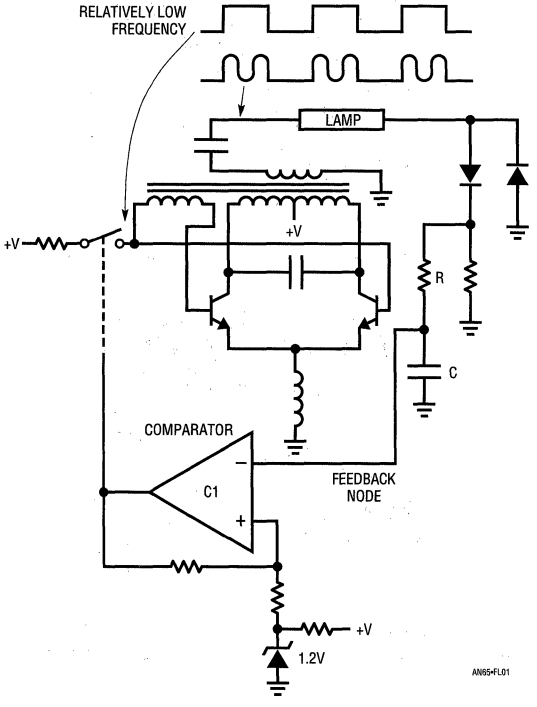


Figure L1. A First Attempt at Improving the Basic Circuit. Irregular Royer Drive Promotes Losses and Poor Regulation

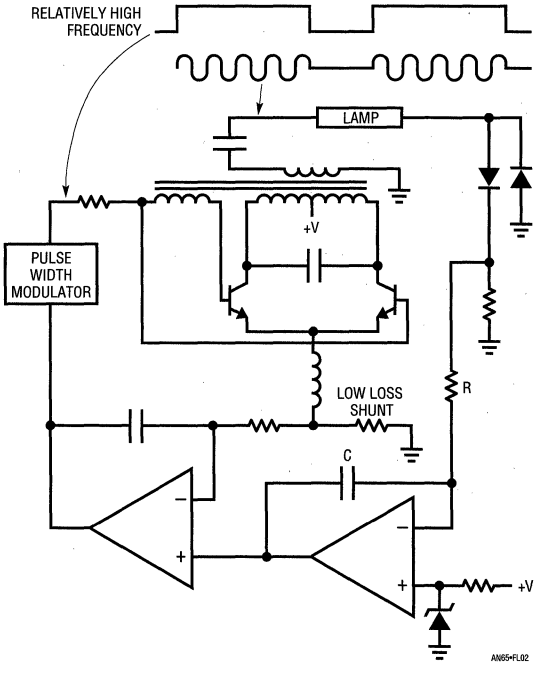


Figure L2. A More Sophisticated Failure Still Has Losses and Poor Line Regulation

avoid annoying flicker, 1% line rejection is required when the line moves abruptly, such as when a charger is activated. Another difficulty is that, although reduced by the higher frequency PWM, crest factor is still nonoptimal with respect to lamp emissivity and life. Finally, the lamp is still forced to restart at each PWM cycle, wasting power.

Figure L3 adds a "keep alive" function to prevent the Royer from turning off. This aspect worked well. When the PWM goes low the Royer is kept running, maintaining low level lamp conduction. This eliminates the continuous lamp restarting, saving power. The "supply correction" block feeds a portion of the supply into the RC averager, improving line rejection to acceptable levels.

This circuit, after considerable fiddling, achieved almost 94% efficiency but produced less output light than a "less efficient" version of text Figure 35! The villain is lamp waveform crest factor. The keep alive circuit helps, but the lamp still cannot handle even moderate crest factors and lamp lifetime is still questionable.

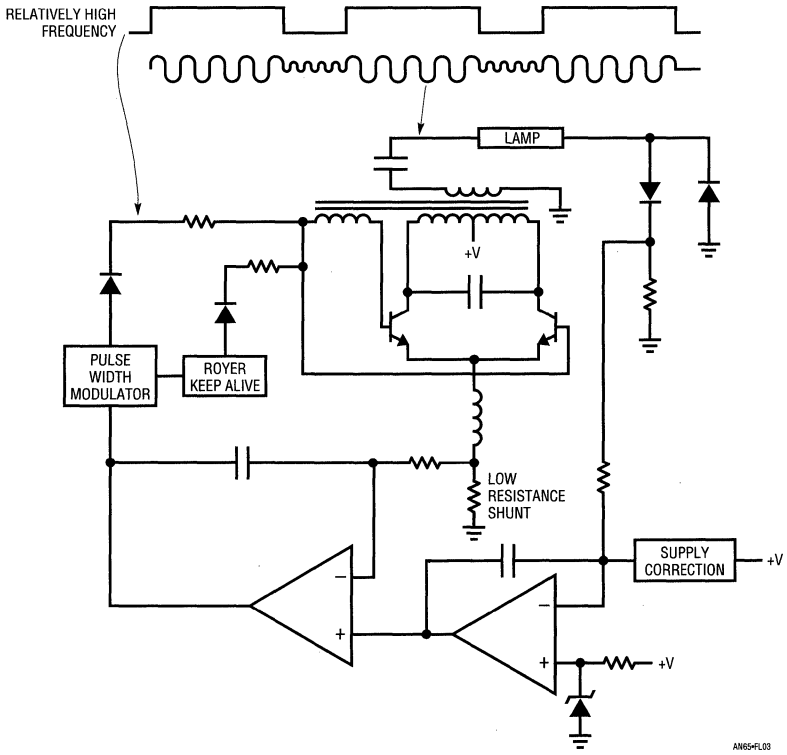


Figure L3. "Keep Alive" Circuit Eliminates Turn-On Losses and Has 94% Efficiency. Light Emission Is Lower Than "Less Efficient" Circuits

Figure L4 is a very different approach. This circuit is a driven square wave converter. The resonating capacitor is eliminated. The base drive generator shapes the edges, minimizing harmonics for low noise operation. This circuit works well, but relatively low operating frequencies are required to get good efficiency. This is so because the sloped drive must be a small percentage of the fundamental to maintain low losses. This mandates relatively large magnetics—a crucial disadvantage. Also, square waves have a different crest factor and rise time than sines, forcing inefficient lamp transduction.

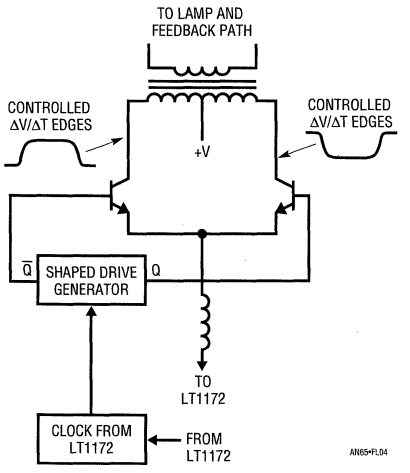


Figure L4. A Nonresonant Approach. Slew Retarded Edges Minimize Harmonics, but Transformer Size Goes Up. Output Waveform Is also Nonoptimal, Causing Lamp Losses

Not-So-Great Primary Side Sensing Ideas

Various text figures use primary side current sensing to control lamp intensity. This permits the lamp to fully float, extending its dynamic operating range. A number of primary side sensing approaches were tried before the "top side sense" won the contest.

L5's ground-referred current sensing is the most obvious way to detect Royer current. It offers the advantage of simple signal conditioning—there is no common mode voltage. The assumption that essentially all Royer current derives from the LT1172 emitter pin path is true. Also true, however, is that the waveshape of this path's current varies widely with input voltage and lamp operating current. The RMS voltage across the shunt (e.g., the Royer current) is unaffected by this, but the simple RC averager produces different outputs for the various waveforms. This causes this approach to have very poor line rejection, rendering it impractical. L6 senses inductor flux, which should correlate with Royer current. This approach promises attractive simplicity. It gives better line regulation but still has some trouble giving reliable feedback as waveshape changes. Also, in keeping with most flux sampling schemes, it regulates poorly under low current conditions.

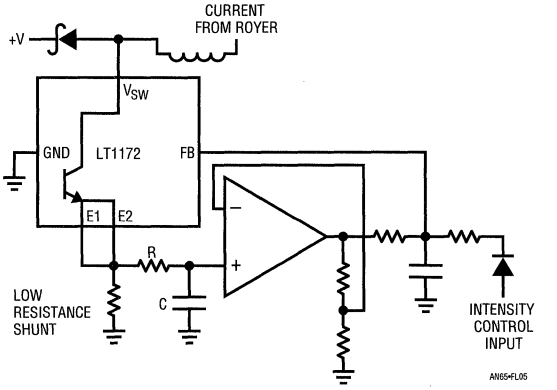


Figure L5. "Bottom Side" Current Sensing Has Poor Line Regulation Due to RC Averaging Characteristics

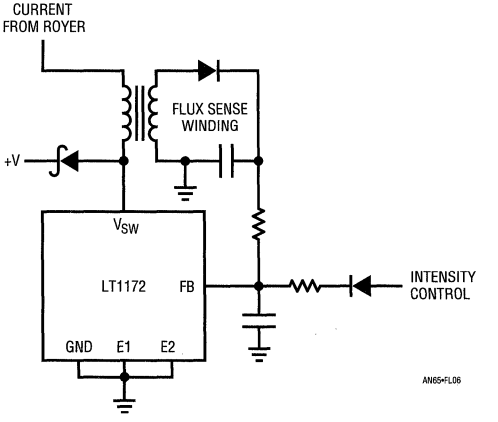


Figure L6. Inductor Flux Sensing Has Irregular Outputs, Particularly at Low Currents

Figure L7 senses flux in the transformer. This takes advantage of the transformer's more regular waveform. Line regulation is reasonably good because of this, but low current regulation is still poor. Figure L8 samples Royer collector voltage capacitively, but the feedback signal does not accurately represent start-up, transient and low current conditions.

Figure L9 is a true, photometrically sensed feedback loop. In theory, it gets around all of the above difficulties by directly sensing lamp emission and feeding back a representative electrical signal. In practice, it introduces severe drawbacks.

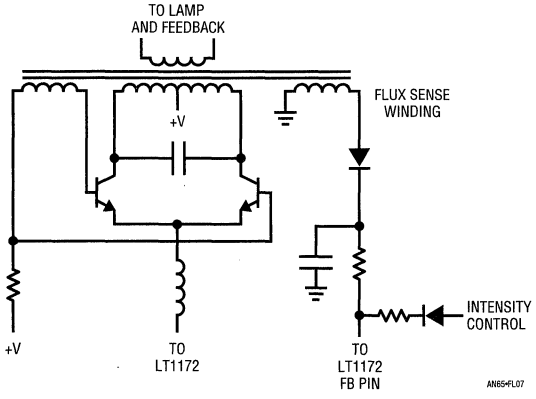


Figure L7. Transformer Flux Sensing Gives More Regular Feedback, but Not at Low Currents

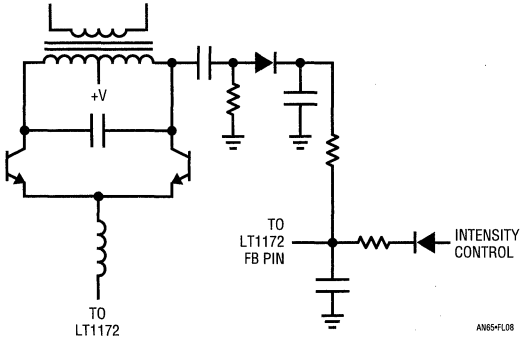


Figure L8. AC-Coupled Drive Waveform Feedback Is Not Reliable at Low Currents

The loop servo controls current to whatever value is required to force lamp emission to the photodiode determined point. This eliminates the gradually increasing lamp output (see text Figure 4) at turn-on. Unfortunately, it also forces huge turn-on currents through the lamp for 10 to 20 seconds, greatly shortening lamp life. Typically, the display immediately settles to the final emission point, but turn-on current peaks at four to six times lamp rating. It is possible to clamp or limit this behavior, but a more insidious problem remains.

As the lamp ages its emissivity drops. Typically, a properly driven lamp will drop to 70% of its original emission level after 10,000 hours. In a photometrically sensed loop, the inverter will continually raise lamp current to counteract decreasing emissivity. Although lamp emission remains constant, life is greatly shortened by the continually increasing overdrive required to maintain output. This positive feedback enforced degenerative spiral assures rapid, systematic lamp destruction. A five to eight times lamp lifetime reduction in this type of loop has been observed. As before, some form of limiting or 2-loop control scheme can mitigate the undesired characteristics, but advantages would be obviated. Finally, an economical photosensor with well-specified response is elusive.

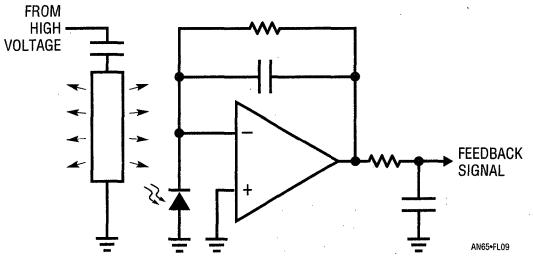


Figure L9. True Optical Sensing Eliminates Feedback Irregularities, but Introduces Systematic Lamp Degradation

Hey Jim, You've been working on Backlights for four years — what have you learned?
Well, I've built Wideband, High Voltage Differential probes, current probes and calibrators. I've played with Resonant Royer Converters, tweaked loop response, made photometers, investigated Lamp Emissivity, and wondered about Reducing display parasitics.
That all sounds real interesting, but what have you Learned?
Uhh, Edison got it right the First time.
'95

Linear Technology Magazine Circuit Collection, Volume II

Power Products

Richard Markell, Editor

INTRODUCTION

Application Note 66 is a compendium of "power circuits" from the first five years of *Linear Technology*. The objective is to collect the useful circuits from the magazine into several applications notes (another, AN67, will collect signal processing circuits into one Application Note) so that valuable "gems" will not be lost. This Application Note contains circuits that can power most any system you can imagine, from desktop computer systems to micropower systems for portable and handheld equipment. Also included here are circuits that provide 300W or more of power factor corrected DC from a universal input. Battery chargers are included, some that charge several battery types, some that are optimized to charge a single type. MOSFET drivers, high side switches and H-bridge driver circuits are also included, as is an article on simple thermal analysis. With these introductory remarks, I'll stand aside and let the authors describe their circuits.

ARTICLE INDEX

Regulators—Switching (Buck)

High Power (>4A)

BIG POWER FOR BIG PROCESSORS: THE LTC1430 SYNCHRONOUS REGULATOR

by Dave Dwelley

The LTC1430 is a new switching regulator controller designed to be configured as a synchronous buck converter with a minimum of external components. It runs at a fixed switching frequency (nominally 200kHz) and provides all timing and control functions, adjustable current limit and soft start, and level shifted output drivers designed to drive an all N-channel synchronous buck converter architecture. The switch driver outputs are capable of driving multiple paralleled power MOSFETs with submicrosecond slew rates, providing high efficiency at very high current levels while eliminating the need for a heat sink in most designs. The LTC1430 is usable in converter designs providing from a few amps to over 50A of output current, allowing it to supply 3.3V power to the most current-hungry arrays of microprocessors.

A Typical 5V to 3.3V Application

The typical application for the LTC1430 is a 5V to 3.xV converter on a PC motherboard. The output is used to power a Pentium® processor, Pentium® Pro processor or similar class processor and the input is taken from the system 5V ±5% supply. The LTC1430 provides the precisely regulated output voltage required by the processor without the need for an external precision reference or trimming. Figure 1 shows a typical application with a 3.30V ±1% output voltage and a 12A output current limit. The power MOSFETs are sized so as not to require a heat sink under ambient temperature conditions up to 50°C. Typical efficiency is above 91% from 1A to 10A output current and peaks at 95% at 5A (Figure 2).

Pentium is a registered trademark of Intel Corporation.

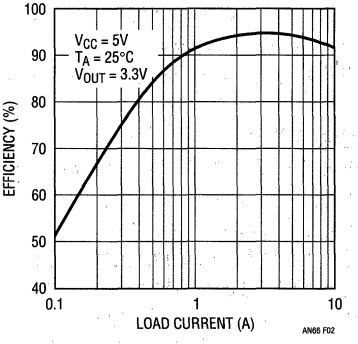


Figure 2. Efficiency Plot for Figure 1's Circuit. Note That Efficiency Peaks at a Respectable 95%

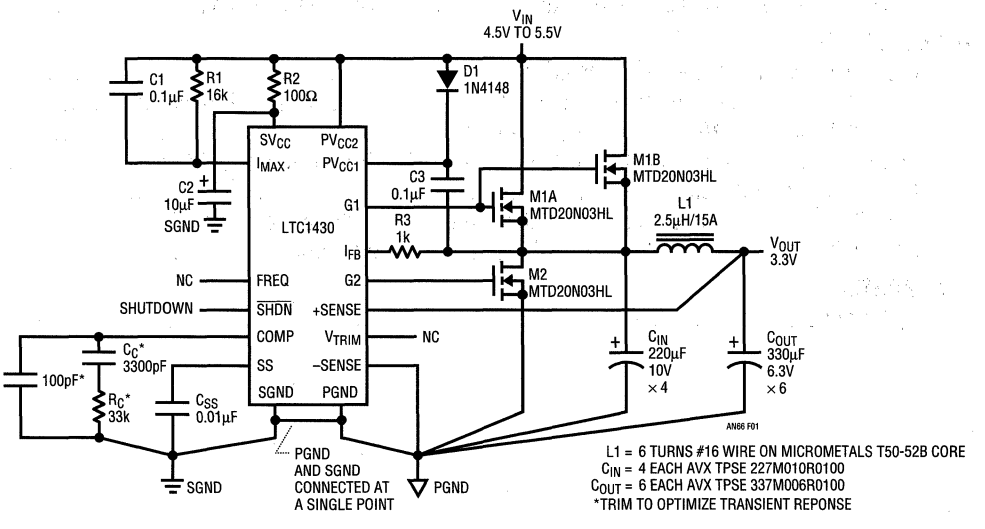


Figure 1. Typical 5V to 3.3V, 10A LTC1430 Application

The 12A current limit is set by the 16k resistor R1 from PV_{CC} to I_{MAX} and the 0.035Ω ON resistance of the MTD20N03HL MOSFETs (M1A, M1B).

The 0.1µF capacitor in parallel with R1 improves power supply rejection at I_{MAX}, providing consistent current limit performance when voltage spikes are present at PV_{CC}. Soft start time is set by C_{SS}; the 0.01µF value shown reacts with an internal 10µA pull-up to provide a 3ms start-up time. The 2.5µH, 15A inductor is sized to allow the peak current to rise to the full current limit value without saturating. This allows the circuit to withstand extended output short circuits without saturating the inductor core. The inductor value is chosen as a compromise between peak ripple current and output current slew rate, which affects large-signal transient response. If the output load is expected to generate large output current transients (as large microprocessors tend to do), the inductor value will need to be quite low, in the 1µH to 10µH range.

Loop compensation is critical for obtaining optimum transient response with a voltage feedback system like the LTC1430; the compensation components shown here give good response when used with the output capacitor values and brands shown (Figure 3). The ESR of the output capacitor has a significant effect on the transient response of the system. For best results use the largest value, lowest ESR capacitors that will fit the design budget and space requirements. Several smaller capacitors wired in parallel can help reduce total output capacitor ESR to acceptable levels. Input bypass capacitor ESR is also important to keep input supply variations to a minimum with $10A_{P-P}$ square wave current pulses flowing into M1. AVX TPS series surface mount tantalum capacitors and Sanyo OS-CON organic electrolytic capacitors are recommended for both input and output bypass duty. Low cost "computer grade" aluminum electrolytics typically have much higher series resistance and will significantly degrade performance. Don't count on that parallel 0.1µF ceramic cap to lower the ESR of a cheap electrolytic cap to acceptable levels.

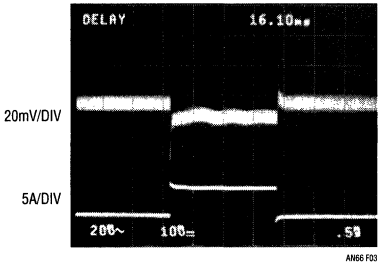


Figure 3. Transient Response: 0A to 5A Load Step Imposed on Figure 1's Output

APPLICATIONS FOR THE LTC1266 SWITCHING REGULATOR

by Greg Dittmer

Figures 4, 5 and 6 show the three basic circuit configurations for the LTC1266. The all N-channel circuit shown in Figure 4 is a 3.3V/5A surface mount converter with the internal MOSFET drivers powered from a separate supply, PWR V_{IN}. The $V_{GS(ON)}$ of the Si9410 N-channel MOSFETs is 4.5V; thus the minimum allowable voltage for PWR V_{IN} is $V_{IN(MAX)}$ + 4.5V. At the other end, PWR V_{IN} should be kept under the maximum safe level of 18V, limiting V_{IN} to 18V – 4.5V = 13.5V. The current sense resistor value is chosen to set the maximum current to 5A according to the formula $I_{OUT} = 100mV/R_{SENSE}$. With V_{IN} = 5V, the 5µH inductor and 130pF timing capacitor provide an operating frequency of 175kHz and a ripple current of 1.25A.

Figure 5 shows an LTC1266 in the charge pump configuration designed to provide a 3.3V/10A output from a single supply. The Si4410s are new logic level, surface mount, N-channel MOSFETs from Siliconix that provide a mere 0.02Ω of on-resistance at V_{GS} = 4.5V and thus provide a 10A solution with minimal components. The efficiency plot shows that the converter is still close to 90% efficient at 10A. Because the charge pump configuration is used, the maximum allowable V_{IN} is 18V/2 = 9V. Due to the high AC currents in this circuit we recommend low ESR OS-CON or AVX input/output capacitors to maintain efficiency and stability.

Figure 6 shows the conventional P-channel topside switch circuit configuration for implementing a 3.3V/3A regulator. The P-channel configuration allows the widest possible supply range of the three basic circuit configurations,

3.5V to 18V, and provides extremely low dropout, exceeding that of most linear regulators. The low dropout results from the LTC1266's ability to achieve a 100% duty cycle when in P-channel mode. In N-channel mode the duty cycle is limited to less than 100% to ensure proper start-up and thus the dropout voltage for the all N-channel converters is slightly higher.

The three application circuits demonstrate the fixed 3.3V version of the LTC1266. The LTC1266 is also available in fixed 5V and adjustable versions. All three versions are available in 16-pin SO packages.

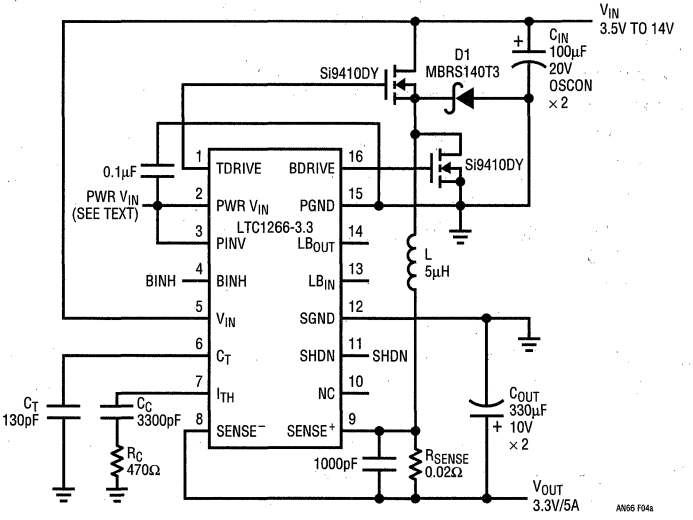


Figure 4a. All N-Channel 3.3V/5A Regulator with Drivers Powered from Seperate Power V_{IN} ($PWR V_{IN}$) Supply

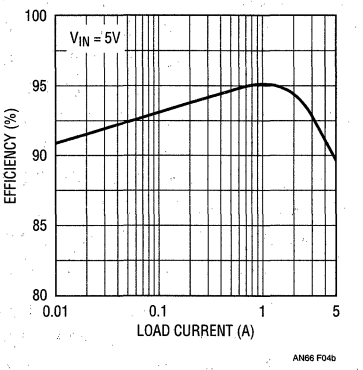


Figure 4b. Efficiency for Figure 4a's Circuit

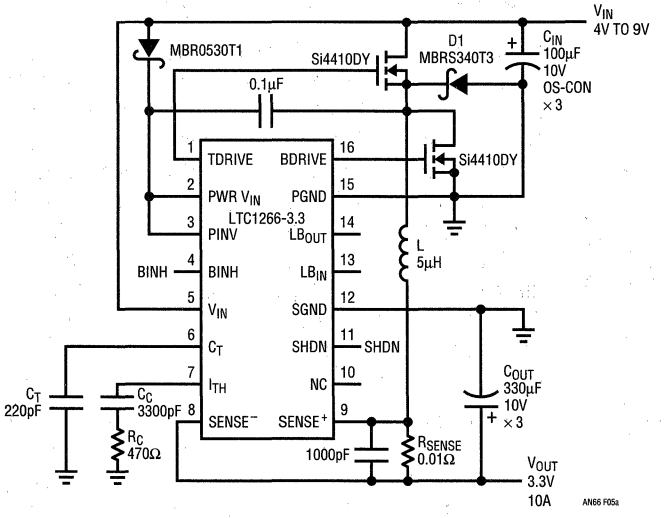


Figure 5a. All N-Channel Single Supply 5V to 3.3V/10A Regulator

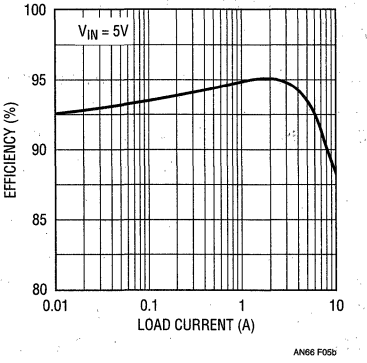


Figure 5b. Efficiency for Figure 5a's Circuit

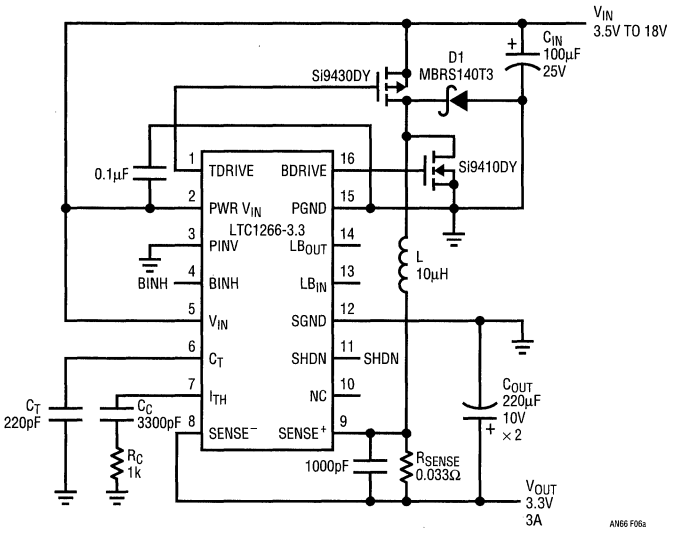


Figure 6a. Low Dropout 3.3V/3A Complementary MOSFET Regulator

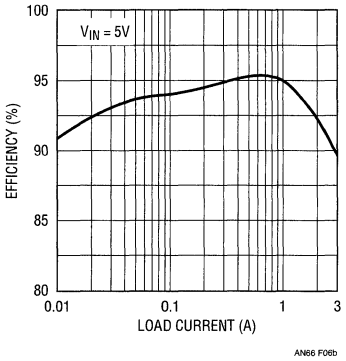


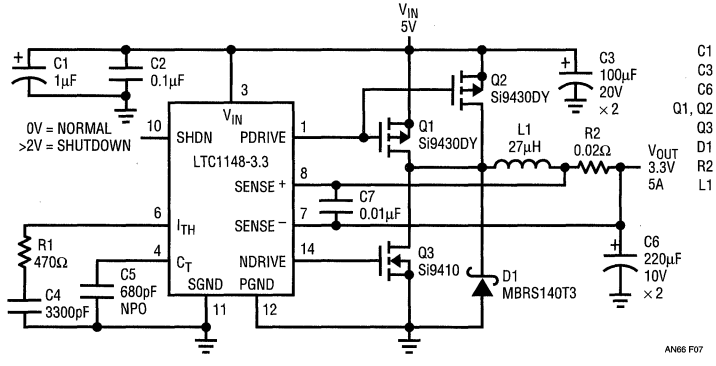
Figure 6b. Efficiency for Figure 6a's Circuit

A HIGH EFFICIENCY 5V TO 3.3V/5A CONVERTER

by Randy G. Flatness

The next generation of notebook and desktop computers is incorporating more 3.3V ICs alongside 5V devices. As the number of devices increases, the current requirements also increase. Typically, a high current 5V supply is already available. Thus, the problem is reduced to deriving 3.3V from 5V efficiently in a small amount of board space. High efficiency is mandatory in these applications, since converting 5V to 3.3V at 5A using a linear regulator would require dissipating over 8W. This wastes power and board space for heat sinking.

The LTC1148 synchronous switching regulator controller accomplishes the 5V to 3.3V conversion with high efficiencies over a wide load current range. The circuit shown in Figure 7 provides 3.3V at efficiencies greater than 90%



C1 = TANTALUM
C3 = SANYO (OS-CON) 20SA100M ESR = 0.037Ω I_{RMS} = 2.25A
C6 = AVX (TA) TPSE227K01R0080 ESR = 0.080Ω I_{RMS} = 1.285A
Q1, Q2 = SILICONIX PMOS BV_{DSS} = 20V DCR_{ON} = 0.100Ω Q_g = 50nC
Q3 = SILICONIX NMOS BV_{DSS} = 30V DCR_{ON} = 0.050Ω Q_g = 30nC
D1 = MOTOROLA SCHOTTKY VBR = 30V
R2 = KRL NP-2A-C1-0R020J Pd = 3W
L1 = KOOL Mµ® CORE, 16 GAUGE
COILTRONICS (408)241-7876
KRL BANTRY (603) 668-3210
SILICONIX (800) 554-5565
KOOL Mµ IS A REGISTERED TRADEMARK OF MAGNETICS, INC.

Figure 7. LTC1148-3.3 High Efficiency 5V to 3.3V/5A Step-Down Converter

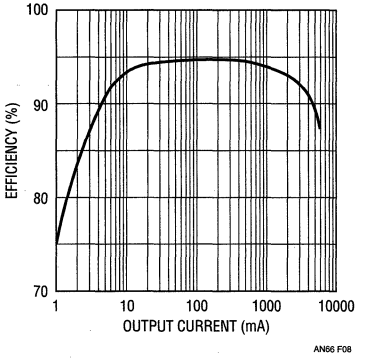


Figure 8. Efficiency for 5V to 3.3V Synchronous Switcher

from 5mA to 5A (over three decades of load current). The efficiency of the circuit in Figure 7 is plotted in Figure 8.

At an output current of 5A the efficiency is 90%; this means only 1.8W are lost. This lost power is distributed among R_{SENSE}, L1 and the power MOSFETs; thus heat sinking is not required.

The LTC1148 series of controllers use constant off-time current mode architecture to provide clean start-up, accurate current limit and excellent line and load regulation. To maximize the operating efficiency at low output currents, Burst Mode™ operation is used to reduce switching losses. Synchronous switching, combined with Burst Mode operation, yields very efficient energy conversion over a wide range of load currents.

The top P-channel MOSFETs in Figure 7 will be on 2/3 of the time with an input of 5V. Hence, these devices should be carefully examined to obtain the best performance. Two MOSFETs are needed to handle the peak currents safely and enhance high current efficiency. The LTC1148 can drive both MOSFETs adequately without a problem. A single N-channel MOSFET is used as the bottom synchronous switch, which shunts the Schottky diode. Finally, adaptive anti-shoot-though circuitry automatically prevents cross conduction between the complementary MOSFETs which can kill efficiency.

The circuit in Figure 7 has a no-load current of only 160µA. In shutdown mode, with Pin 10 held high (above 2V), the quiescent current decreases to less than 20µA with all MOSFETs held off DC. Although the circuit in Figure 7 is specified at a 5V input voltage, the circuit will function from 4V to 15V without requiring any component substitutions.

Burst Mode is a trademark of Linear Technology Corporation.

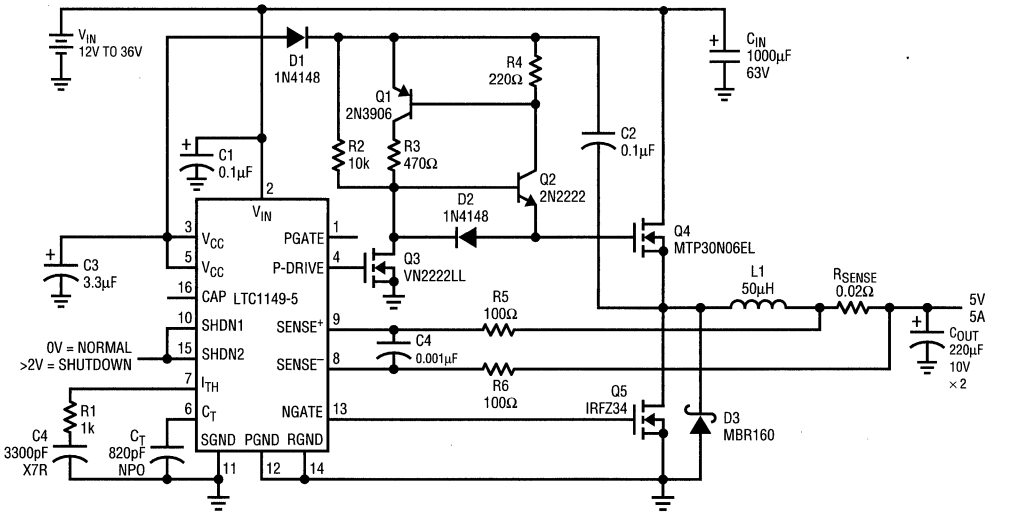
HIGH CURRENT, SYNCHRONOUS STEP-DOWN SWITCHING REGULATOR

by Brian Huffman

The LTC1149 is a half-bridge driver designed for synchronous buck regulator applications. Normally a P- and N-channel output stage is employed, but the P-channel device ON resistance becomes a limiting factor at output currents above 2A. N-channel MOSFETs are better suited for use in high current applications, since they have a substantially lower ON resistance than comparably priced P-channels. The circuit shown in Figure 9 adapts the LTC1149 to drive a half-bridge consisting of two N-channel MOSFETs, providing efficiency in excess of 90% at an output current of 5A.

The circuit's operation is as follows: the LTC1149 provides a P-drive output (Pin 4) that swings between ground and 10V, turning Q3 on and off. While Q3 is on, the N-channel MOSFET (Q4) is off because its gate is pulled low by Q3 through D2. During this interval, the Ngate output (Pin 13) turns the synchronous switch (Q5) on creating a low resistance path for the inductor current.

Q4 turns on when its gate is driven above the input voltage. This is accomplished by bootstrapping capacitor C2 off the drain of Q4. The LTC1149 V_{CC} output (Pin 3) supplies a regulated 10V output that is used to charge C2 through D1 while Q4 is off. With Q4 off, C2 charges to 5V during the first cycle in Burst Mode operation and to 10V thereafter.



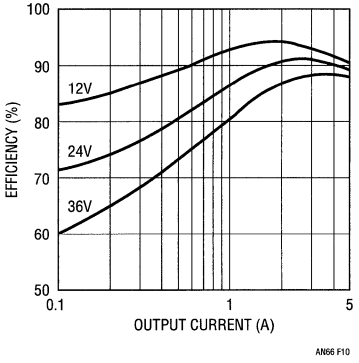
C3 (TA) LOW ESR
C_{IN} NICHICON (AL) UPL1J102MRH, ESR = 0.027Ω, I_{RMS} = 2.370A
C_{OUT} SANYO (OS-CON) 10SA220M, ESR = 0.035Ω, I_{RMS} = 2.360A
Q1 PNP, BVCEO = 30V
Q2 NPN, BVCEO = 40V
Q3 SILICONIX NMOS, BVDSS = 60V, RDS_{ON} = 5Ω
Q4, Q5 NMOS, BVDSS = 60V, RDS_{ON} = 0.05Ω
D1, D2 SILICON, VBR = 75V
D3 MOTOROLA SCHOTTKY, VBR = 60V
R_{SENSE} = KRL NP-2A-C1-0R020J, P_D = 3W
L1 = COILTRONICS CTX50-5-52, DCR = 0.21Ω, IRON POWDER CORE
ALL OTHER CAPACITORS ARE CERAMIC

AN66 F09

Figure 9. LTC1149-5 (12V-36V to 5V/5A) Using N-Channel MOSFETs

When Q3 turns off, the N-channel MOSFET is turned on by the SCR-connected NPN/PNP network (Q1 and Q2). Resistor R2 supplies Q2 with enough base drive to trigger the SCR. Q2 then forces Q1 to turn on, supplying more base drive to Q2. This regenerative process continues until both transistors are fully saturated. During this period, the source of Q4 is pulled to the input voltage. While Q4 is on, its gate source voltage is approximately 10V, fully enhancing the N-channel MOSFET.

Efficiency performance for this circuit is quite impressive. Figure 10 shows that for a 12V input the efficiency never drops below 90% over the 0.6A to 5A range. At higher input voltages efficiency is reduced due to transition losses in the power MOSFETs. For low output currents efficiency rolls off because of quiescent current losses.



AN66 F10

Figure 10. LTC1149-5 (12V-36V to 5V/5A) High Current Buck

Regulators—Switching (Buck)

Medium Power (1A to 4A)

1MHz STEP-DOWN CONVERTER ENDS 455kHz IF WOES

by Mitchell Lee

There can be no doubt that switching power supplies and radio IFs don't mix. One-chip converters typically operate in the range of 20kHz to 100kHz, placing troublesome harmonics right in the middle of the 455kHz band. This contributes to adverse effects such as "desensing" and outright blocking of the intended signals. A new class of switching converter makes it possible to mix high efficiency power supply techniques and 455kHz radio IFs without fear of interference.

The circuit shown in Figure 11 uses an LT1377 boost converter operating at 1MHz to implement a high efficiency buck topology switching regulator. The switch is internally grounded, calling for the floating supply arrangement shown (D1 and C1). The circuit converts inputs of 8V through 30V to a 5V/1A output.

The chip's internal oscillator operates at 1MHz for load currents of greater than 50mA with a guaranteed tolerance of 12% over temperature. Even wideband 455kHz IFs are unaffected, as the converter's operating frequency is well over one octave distant.

Figure 12 shows the efficiency of Figure 11's circuit. You can expect 80% to 90% efficiency over an 8V to 16V input range with loads of 200mA or more. This makes the circuit suitable for 12V battery inputs (that's how I'm using it), but no special considerations are necessary with adapter inputs of up to 30V.

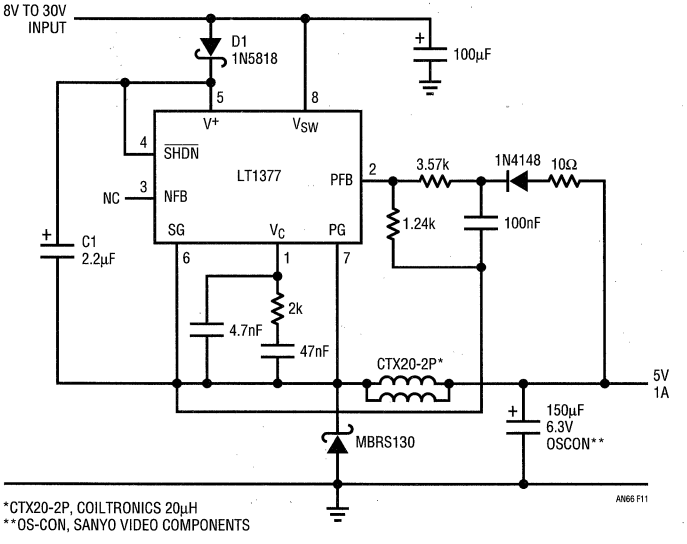


Figure 11. Schematic Diagram: 1MHz LT1377-Based Boost Converter

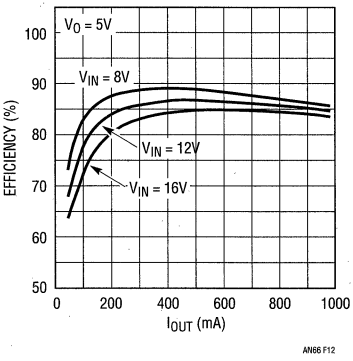


Figure 12. Efficiency Graph of the Circuit Shown in Figure 3

HIGH OUTPUT VOLTAGE BUCK REGULATOR

by Dimitry Goder

High efficiency step-down conversion is easy to implement using the LTC1149 as a buck switching regulator controller. The LTC1149 features constant off-time, current mode architecture and fully synchronous rectification. Current mode operation was selected for its well-known advantages of clean start-up, accurate current limit and excellent transient response.

Inductor current sensing is usually implemented by placing a resistor in series with the coil, but the common mode voltage at the LTC1149's Sense pins is limited to 13V. If a higher output voltage is required, the current sense resistor can be placed in the circuit's ground return to avoid common mode problems. The circuit in Figure 13 can be used in applications that do not lend themselves to this approach.

Figure 13 shows a special level shifting circuit (Q1 and U2) added to a typical LTC1149 application. The LT1211, a high speed, precision amplifier, forces the voltage across R5 to equal the voltage across current sense resistor R8. Q1's drain current flows to the source, creating a voltage across R6 proportional to the inductor current, which is now referenced to ground. This voltage can be directly applied to the current sense inputs of U1, the LTC1149. C12 and C4 are added to improve high frequency noise immunity. Maximum input voltage is now limited by the LT1211; it can be increased if a Zener diode is placed in parallel with C12.

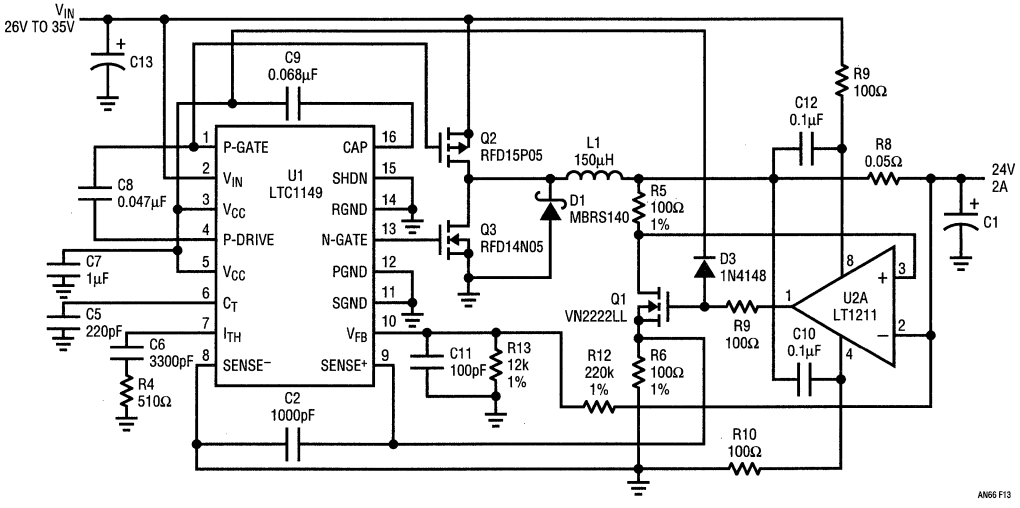


Figure 13. High Output Voltage Buck Regulator Schematic Using LTC1149

THE LTC1267 DUAL SWITCHING REGULATOR CONTROLLER OPERATES FROM HIGH INPUT VOLTAGES

by Randy G. Flatness

Fixed Output 3.3V and 5V Converter

A fixed LTC1267 application circuit creating 3.3V/2A and 5V/2A is shown in Figure 15. The operating efficiency shown in Figure 14 exceeds 90% for both the 3.3V and 5V sections. The 3.3V section of the circuit in Figure 15 comprises the main switch Q1, synchronous switch Q2, inductor L1 and current shunt R_{SENSE3}.

The 5V section is similar and comprises Q3, Q4, L2 and R_{SENSE5}. Each current sense resistor (R_{SENSE}) monitors the inductor current and is used to set the output current according to the formula $I_{OUT} = 100mV/R_{SENSE}$. Advantages of current control include excellent line and load transient rejection, inherent short-circuit protection and controlled start-up currents. Peak inductor currents for L1 and L2 are limited to $150mV/R_{SENSE}$ or 3.0A. The EXT V_{CC} pin is connected to the 5V output increasing efficiency at high input voltages. The maximum input voltage is limited by the MOSFETs and should not exceed 28V.

Adjustable Output 3.6V and 5V Converter

The adjustable output LTC1267-ADJ shown in Figure 16 is configured as a 3.6V/2.5A and 5V/2A converter. The resistor divider composed of R1 and R2 sets the output voltage according to the formula $V_{OUT} = 1.25V\ (1 + R2/R1)$. The input voltage range for this application is 5.5V to 28V.

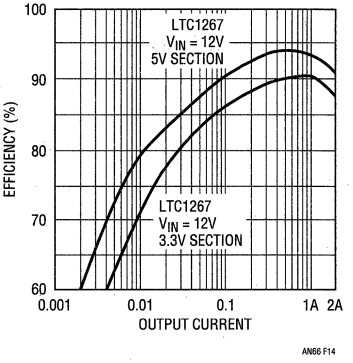


Figure 14. LTC1267 Efficiency vs Output Current of Figure 15 Circuit

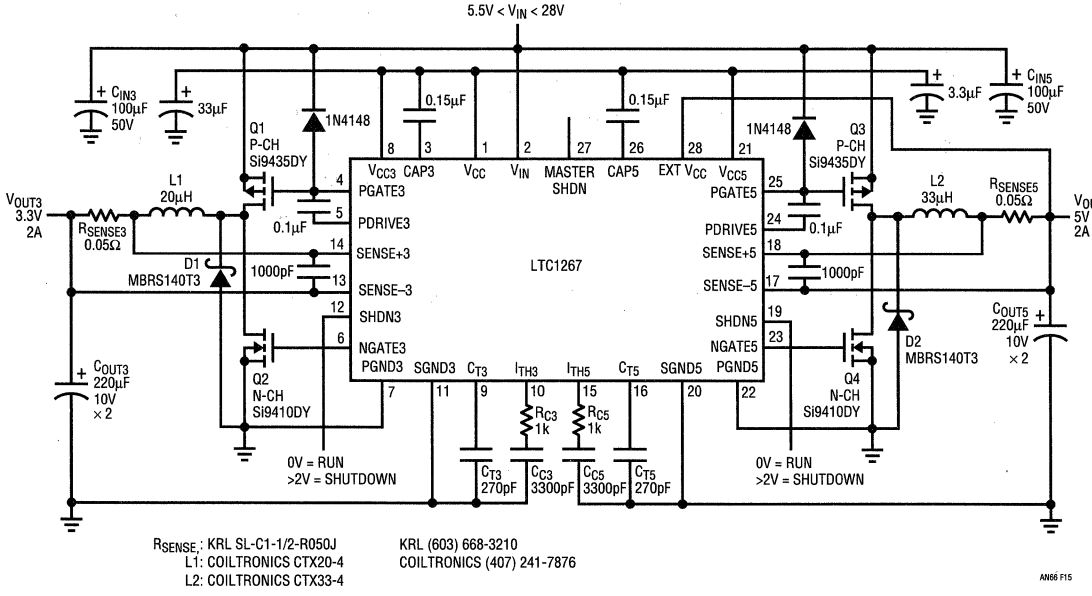


Figure 15. LTC1267 Dual Output 3.3V and 5V High Efficiency Regulator

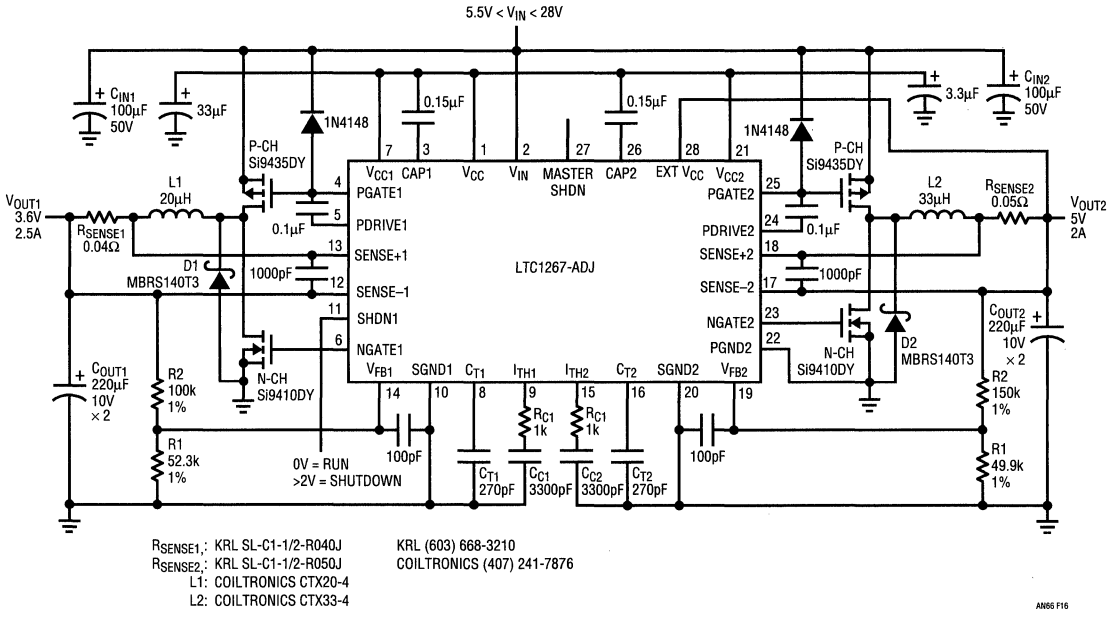


Figure 16. LTC1267 Dual Adjustable High Efficiency Regulator Circuit. Output Voltages Set at 3.6V and 5V

HIGH EFFICIENCY 5V TO 3.3V/1.25A CONVERTER IN 0.6 SQUARE INCHES

by Randy G. Flatness

The next generation of notebook and desktop computers will incorporate a growing number of 3.3V ICs along with 5V devices. As the number of 3.3V devices increases, the current requirements increase. Typically, a high current 5V supply is already available. Thus, the problem is reduced to deriving 3.3V from 5V at high efficiency in a small amount of board space.

High efficiency is mandatory in these applications since converting 5V to 3.3V at 1.25A using a linear regulator would require dissipating over 2W. This is an unnecessary waste of power and board space for heat sinking.

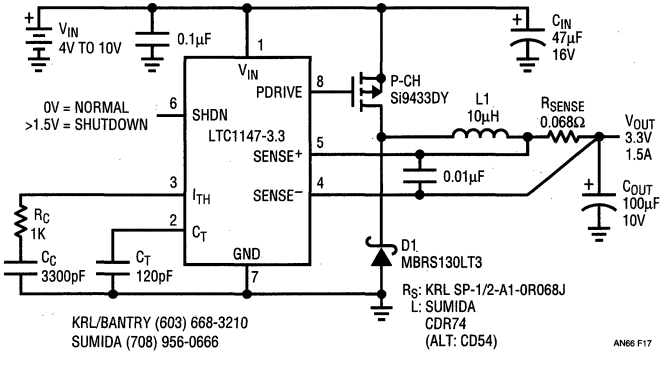


Figure 17. High Efficiency Controller Converts 5V to 3.3V in Minimum Board Area

The LTC1147 SO-8 switching regulator controller accomplishes the 5V to 3.3V conversion with high efficiencies over a wide load current range. The circuit shown in Figure 17 provides 3.3V at efficiencies greater than 90% from 50mA to 1.25A. Using all surface mount components and a low value of inductance (10µH) for L1, the circuit of Figure 17 occupies only 0.6 square inches of PC board area. The efficiency of the circuit in Figure 17 is plotted in Figure 18.

At an output current of 1.25A the efficiency is 90.4%; this means only 0.4W are lost. This lost power is distributed among R_{SENSE}, L1 and the power MOSFETs; thus heat sinking is not required.

The LTC1147 series of controllers use constant off-time current mode architecture to provide clean start-up, accurate current limit and excellent line and load regulation. To maximize the operating efficiency at low output currents, Burst Mode operation is used to reduce switching losses.

The P-channel MOSFET in the circuit of Figure 17 will be on 2/3 of the time with an input voltage of 5V. Hence, this device should be carefully selected to obtain the best performance. This design uses an Si9433DY for optimum efficiency; for lower cost an Si9340DY can be used at a slight reduction in performance.

The circuit in Figure 17 has a no load current of only 160µA. In shutdown, with Pin 6 held high (above 2V), the quiescent current is reduced to less than 20µA with the MOSFET held off. Although the circuit in Figure 17 is specified at a 5V input voltage the circuit will function from 4V to 10V.

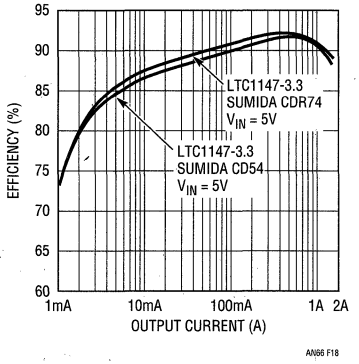


Figure 18. 5V to 3.3V Conversion Efficiency

LT1074/LT1076 ADJUSTABLE 0V TO 5V POWER SUPPLY

by Kevin Vasconcelos

Linear regulator ICs are commonly used in variable power supplies. Common types such as the 317 can be adjusted as low as 1.25V in single-supply applications. At low output voltages power losses in these regulators can be a problem. For example, if an output current of 1.5A is required at 1.25V from an input of 8V, the regulator dissipates more than 10W. Figure 19 shows a DC/DC converter that functionally replaces a linear regulator in this application. The converter not only eliminates power

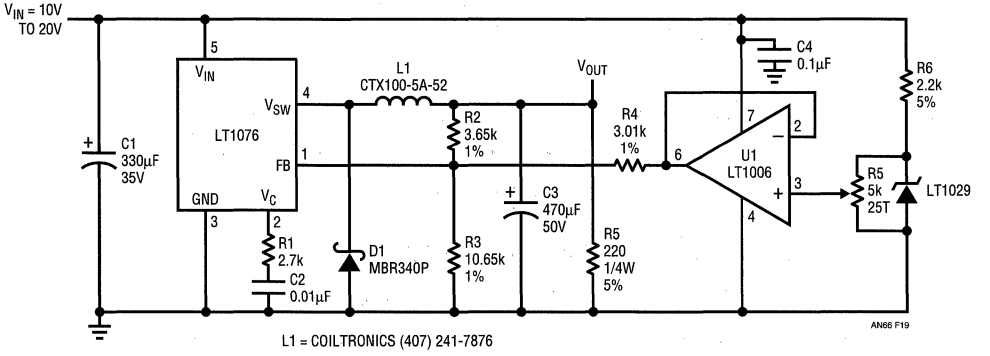


Figure 19. Adjustable LT1074/LT1076 0V to 5V Power Supply

loss as a concern, but can be adjusted for output voltages as low as 25mV while still delivering an output current of 1.5A.

The circuit of Figure 19 employs a basic positive buck topology with one exception: a control voltage is applied through R4 to the feedback summing node at Pin 1 of the LT1076 switching regulator IC, allowing the output to be adjusted from 0V to approximately 6V. This encompasses the 3.3V and 5V logic supply ranges as well as battery pack combinations of one to four D cells.

As R4 is driven from 0V to 5V by the buffer (U1) more or less current is required from R2 to satisfy the loop's desire to hold the feedback summing point at 2.21V. This forces the converter's output to swing over the range of 0V to 6V.

Figure 20 shows a comparison of power losses for a linear regulator and the circuit of Figure 19. The load current is 1.5A in both cases although the LT1076 is capable of 1.75A guaranteed output current in this application and 2A typical. If more current is required the LT1074 can be substituted for the LT1076. This change accommodates outputs up to 5A but at the expense of a heftier diode and coil (D1, L1). An MBR735 and Coiltronics CTX50-2-52 are recommended for 5A service.

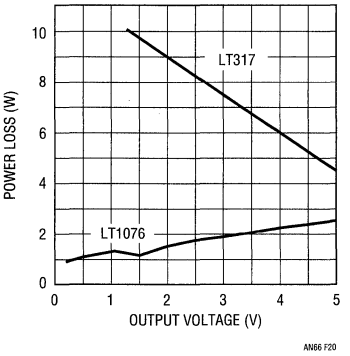


Figure 20. Power Loss Comparison: Linear Regulator vs Figure 19's Power Supply

TRIPLE OUTPUT 3.3V, 5V AND 12V HIGH EFFICIENCY NOTEBOOK POWER SUPPLY

by Randy G. Flatness

LTC1142 Circuit Operation

The application circuit in Figure 22 is configured to provide output voltages of 3.3V, 5V and 12V. The current capability of both the 3.3V and 5V outputs is 2A (2.5A peak). The logic-controlled 12V output can provide 150mA (200mA peak), which is ideal for flash memory applications. The operating efficiency shown in Figure 21 exceeds 90% for both the 3.3V and 5V sections.

The 3.3V section of the circuit in Figure 22 comprises the main switch Q4, synchronous switch Q5, inductor L1 and current shunt R_{SENSE3}. The current sense resistor R_{SENSE} monitors the inductor current and is used to set the output current according to the formula $I_{OUT} = 100mV/R_{SENSE}$. Advantages of current control include excellent line and load transient rejection, inherent short-circuit protection and controlled start-up currents. Peak inductor currents for L1 and T1 of the circuit in Figure 22 are limited to $150mV/R_{SENSE}$ or 3.0A and 3.75A respectively.

When the output current for either regulator section drops below approximately $15mV/R_{SENSE}$, that section automatically enters Burst Mode operation to reduce switching losses. In this mode the LTC1142 holds both MOSFETs off and "sleeps" at 160µA supply current while the output capacitor supports the load. When the output capacitor falls 50mV below its specified voltage (3.3V or 5V) the LTC1142 briefly turns this section back on, or "bursts," to recharge the output capacitor. The timing capacitor pins,

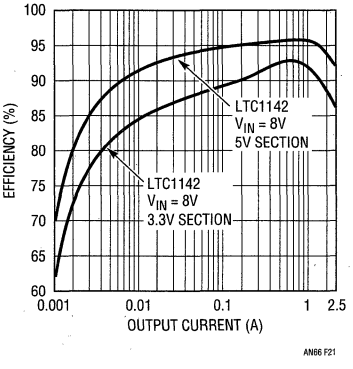


Figure 21. LTC1142 Efficiency

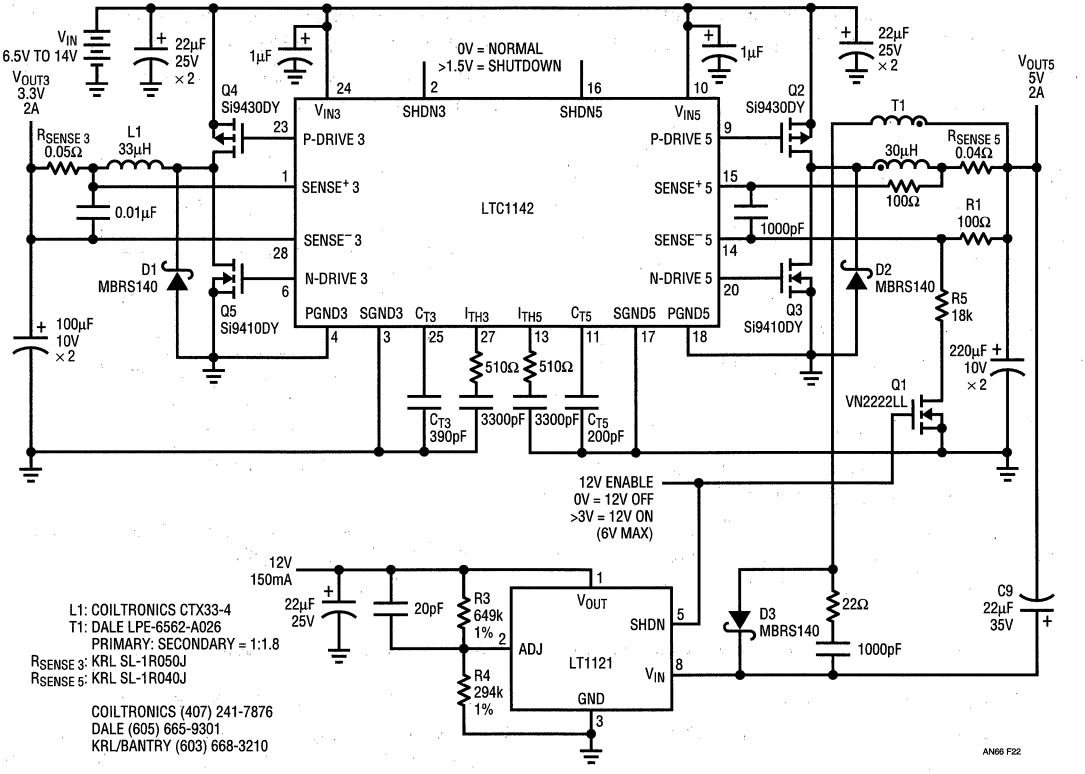


Figure 22. LTC1142 High Efficiency Power Supply Schematic Diagram

which go to 0V during the sleep interval, can be monitored with an oscilloscope to observe burst action. As the load current is decreased the circuit will burst less and less frequently.

The timing capacitors C_{T3} and C_{T5} set the off-time according to the formula $t_{OFF} = 1.3\,(10^4)(C_T)$. The constant off-time architecture maintains a constant ripple current while the operating frequency varies only with input voltage. The 3.3V section has an off-time of approximately 5µs, resulting in a operating frequency of 120kHz with an 8V input. The 5V section has an off-time of 2.6µs and a switching frequency of 140kHz with an 8V input.

Auxiliary 12V Output

The operation of the 5V section is identical to the 3.3V section with inductor L1 replaced by transformer T1. The 12V output is derived from an auxiliary winding on the 5V inductor. The output from this additional winding is rectified by diode D3 and applied to the input of an LT1121 regulator. The output voltage is set by resistors R3 and R4. A turns ratio of 1:1.8 is used for T1 to ensure that the input voltage to the LT1121 is high enough to keep the regulator out of dropout mode while maximizing efficiency.

The LTC1142 synchronous switch removes the normal limitation that power must be drawn from the primary 5V inductor winding in order to extract power from the auxiliary winding. With synchronous switching, the auxiliary 12V output may be loaded without regard to the 5V primary output load, provided that the loop remains in continuous mode operation.

When the 12V output is activated by a TTL high (6V maximum) on the 12V enable line, the 5V section of the LTC1142 is forced into continuous mode. A resistor

divider composed of R1, R5 and switch Q1 forces an offset, subtracting from the internal offset at Pin 14. When this external offset cancels the built-in 25mV offset, Burst Mode operation is inhibited.

Auxiliary 12V Output Options

The circuit of Figure 22 can be modified for operation in low-battery count (6-cell) applications. For applications where heavy 12V load currents exist in conjunction with low input voltages (<6.5V), the auxiliary winding should be derived from the 3.3V instead of the 5V section. As the input voltage falls, the 5V duty cycle increases to the point when there is simply not enough time to transfer energy from the 5V primary winding to the 12V secondary winding. For operation from the 3.3V section, a transformer with a turns ratio of 1:3.25 should be used in place of the 33µH inductor L1. Likewise, a 30µH inductor would replace T1 in the 5V section. With these component changes, the duty cycle of the 3.3V section is more than adequate for full 12V load currents. The minimum input voltage in this case will be determined only by the dropout voltage of the 5V output. The 100% duty cycle inherent in the LTC1142 provides low dropout operation limited only by the load current multiplied by the sum of the resistances of the 5V inductor, Q2 $R_{DS(ON)}$ and current sense resistor R_{SENSE5}.

Extending the Maximum Input Voltage

The circuit in Figure 22 is designed for a 14V maximum input voltage. The operation of the circuit can be extended to over 18V if a few key components are changed. The parts that determine the maximum input voltage of the circuit are the power MOSFETs, the LTC1142 and the input capacitors. With the LTC1142 replaced by an LTC1142HV, an 18V typical (20V maximum) input voltage is allowable. Since the gate drive voltages supplied by the LTC1142 and LTC1142HV are from ground to V_{IN}, the input voltage must not exceed the maximum V_{GS} of the MOSFETs. The MOSFETs specified in Figure 22 have an absolute maximum of 20V, matching that of the LTC1142HV.[1] Finally, the input capacitor's voltage rating will also have to be increased above 12V.

[1]For improved efficiency, CT5 should be charged to 270pF.

THE NEW SO-8 LTC1147 SWITCHING REGULATOR CONTROLLER OFFERS HIGH EFFICIENCY IN A SMALL FOOTPRINT

by Randy Flatness

Introduction

The LTC1147 switching regulator controller is a high efficiency step-down DC/DC converter. It uses the same current mode architecture and Burst Mode operation as the LTC1148/LTC1149 but without the synchronous switch. Ideal for applications requiring up to 1A, the LTC1147 shows 90% efficiencies over two decades of output current.

High Efficiency 5V to 3.3V in a Small Area

The LTC1147 5V to 3.3V converter shown in Figure 23 has 85% efficiency at 1A output with efficiencies greater than 90% for load currents up to 500mA. Using the LTC1147 reduces the power dissipation to less than 500mW. The efficiency plotted as a function of output current is shown in Figure 24.

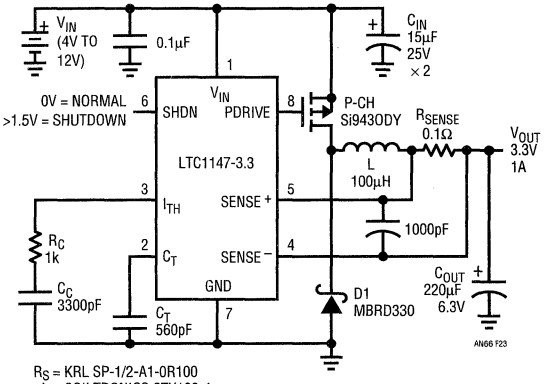


Figure 23. This LTC1147 5V to 3.3V Converter Achieves 92% Efficiency at 300mA Load Current

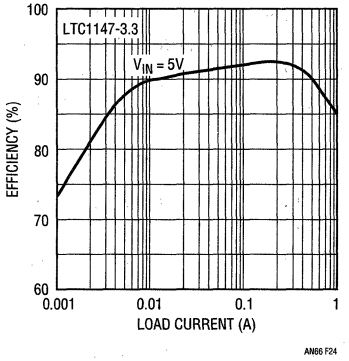


Figure 24. The LTC1147 5V to 3.3V Converter Provides Better Than 90% Efficiency from 20mA to 500mA of Output Current

Giving Up the Synchronous Switch?

The decision whether to use a nonsynchronous LTC1147 design or a fully synchronous LTC1148 design requires a careful analysis of where losses occur. The LTC1147 switching regulator controller uses the same loss reducing techniques as the other members of the LTC1148/LTC1149 family. The nonsynchronous design saves the N-channel MOSFET gate drive current at the expense of increased loss due to the Schottky diode.

Figure 25 shows how the losses in a typical LTC1147 application are apportioned. The gate-charge loss (P-channel MOSFET) is responsible for the majority of the efficiency lost in the midcurrent region. If Burst Mode operation was not employed, the gate charge loss alone would cause the efficiency to drop to unacceptable levels at low output currents. With Burst Mode operation, the DC supply current represents the only loss component that increases almost linearly as output current is reduced. As expected, the I^2R loss and Schottky diode loss dominate at high load currents.

In addition to board space, output current and input voltage are the two primary variables to consider when deciding whether to use the LTC1147. At low input-to-output voltage ratios, the top P-channel switch is on most of the time, leaving the Schottky diode conducting only a small percentage of the total period. Hence, the power lost in the Schottky diode is small at low output currents. This is the ideal application for the LTC1147. As the output current increases the diode loss increases. At high input-to-output voltage ratios, the Schottky diode conducts most of the time. In this situation, any loss in the diode will have a more significant effect on efficiency and an LTC1148 might therefore be chosen.

Figure 26 compares the efficiencies of LTC1147-5 and LTC1148-5 circuits with the same inductor, timing capacitor and P-channel MOSFET. At low input voltages and 1A output current the efficiency of the LTC1147 differs from that of the LTC1148 by less than two percent. At lower

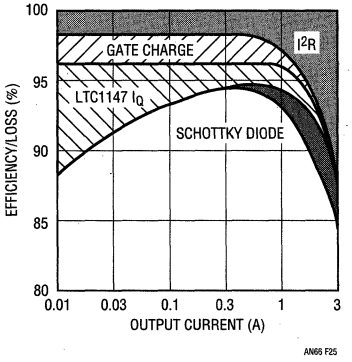


Figure 25. Low Current Efficiency is Enhanced by Burst Mode Operation. Schottky Diode Loss Dominates at High Output Currents

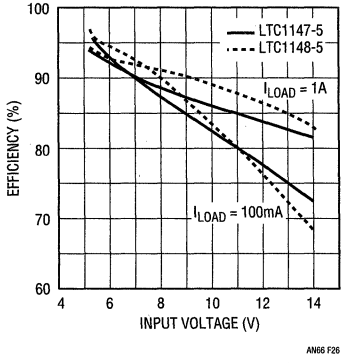


Figure 26. At High Input Voltages Combined with Low Output Currents, the Efficiency of the LTC1147 Exceeds That of the LTC1148

output currents and high input voltages the LTC1147's efficiency can actually exceed that of the LTC1148.

Low Dropout 5V Output Applications

Because the LTC1147 is so well-suited for low input-to-output voltage ratio applications it is an ideal choice for low dropout designs. All members of the LTC1148/LTC1149 family (including the LTC1147) have outstandingly low dropout performance. As the input voltage on the LTC1147 drops, the feedback loop extends the on-time for the P-channel switch (off-time is constant) thereby keeping the inductor ripple current constant. Eventually the on-time extends so far that the P-channel MOSFET is on at DC or at a 100% duty cycle.

With the switch turned on at a 100% duty cycle, the dropout is limited by the load current multiplied by the sum of the resistances of the MOSFET, the current shunt and the inductor. For example, the low dropout 5V regulator shown in Figure 27 has a total resistance of less than 0.2Ω. This gives it a dropout voltage of 200mV at 1A output current. At input voltages below dropout the output voltage follows the input. This is the circuit whose efficiency is plotted in Figure 28.

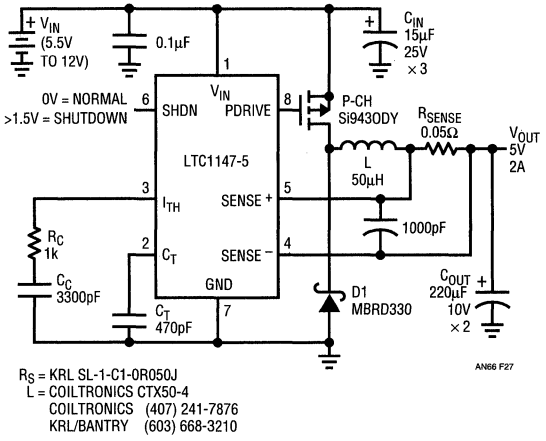


Figure 27. The LTC1147 Architecture Provides Inherent Low Dropout Operation. This LTC1147-5 Circuit Supports a 1A Load with the Input Voltage Only 200mV Above the Output

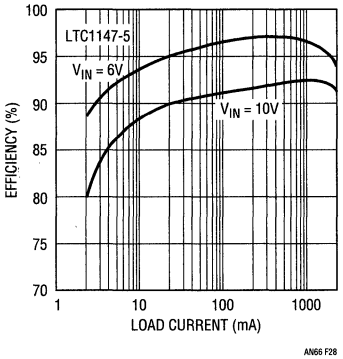


Figure 28. Greater Than 90% Efficiency is Obtained for Load Currents of 20mA to 2A (V_{IN} = 10V)

THE LT1432: 5V REGULATOR ACHIEVES 90% EFFICIENCY

by Carl Nelson

Power supply efficiency has become a highly visible issue in many portable battery-powered applications. Higher efficiency translates directly to longer useful operating time—a potent selling point for products such as notebook computers, cellular phones, data acquisition units, sales terminals and word processors. The "holy grail" of efficiency for 5V outputs is 90%.

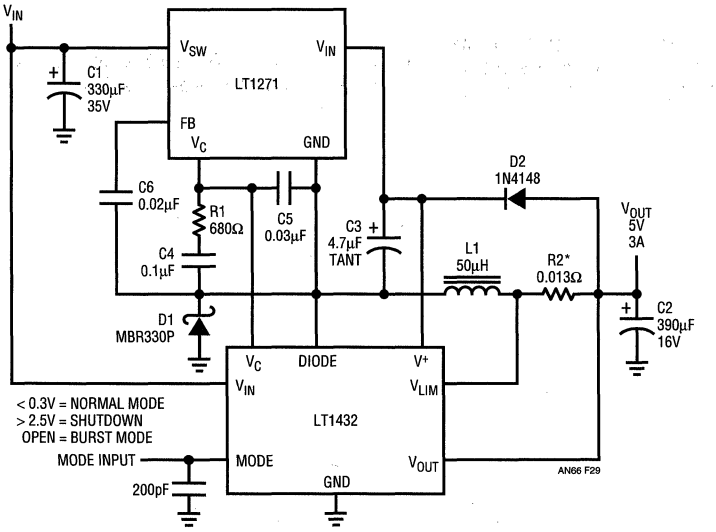
For a number of reasons, older designs were limited to efficiencies of 80 to 85%. High quiescent current in the control circuitry limited efficiency at lower output currents. Losses in the power switch, inductor and catch diode all added up to limit efficiency at moderate-to-high output currents. Each of these areas must be addressed in a design that is to have high efficiency over a wide output current range.

Some portable equipment has the additional requirement of high efficiency at extremely light loads (1mA to 5mA). These applications have a sleep mode in which RAM is kept alive to retain information. The instrument may spend days or even weeks in this mode, so battery drain is critical. Ordinary 5V switchers draw quiescent currents of 5mA to 15mA for these light loads. The efficiency of a 12V to 5V converter with 10mA supply current and 1mA load is only 4%. Clearly, some method must be provided to eliminate the quiescent current of the switching regulator control section.

An additional requirement for some systems is full shutdown of the regulator. It would be ideal if a simple logic signal could cause the converter to turn off and draw only a few microamperes of current.

The combination of battery form factors, their discrete voltage steps and the use of higher voltage wall adapters requires a switching regulator that operates with inputs from 6V to 30V. Both of these voltages present problems for a MOS design because of minimum and maximum gate voltage requirements of power MOS switches.

The LT1432 was designed to address all the requirements described above. It is a bipolar control chip that interfaces directly to the LT1070 family of switching regulators and is capable of operating with 6V to 30V inputs. These ICs have a very efficient, quasisaturating NPN switch that mimics the resistive nature of MOS transistors with much smaller die areas. The NPN is a high frequency device with



*R2 IS MADE FROM PC BOARD COPPER TRACES
L1 = COILTRONICS CTX 50-3-MP (3A) (407) 241-7876

Figure 29. High Efficiency 5V Buck Converter

an equivalent voltage and current overlap time of only 10ns. Drive to the switch is automatically scaled with switch current, so drive losses are also low. Switch and driver losses using an LT1271 with a 12V input and a 5V, 500mA load are only about 2%.

To reduce quiescent current losses, the LT1271 is powered from the 5V output rather than from the input voltage. This is done by pumping the supply capacitor C3 from the output via D2. Quick minded designers will observe that this arrangement does not self-start; accordingly, a parallel path was included inside the LT1432 to provide power to the IC switcher directly from the input during start-up. Equivalent quiescent supply current is reduced to about 3.5mA with this technique.

Catch diode losses cannot be reduced with IC "tricks" unless the diode is replaced with a synchronously driven MOS switch. This is more expensive and still requires the diode to avoid voltage spikes during switch nonoverlap times. The question is, is it worth it?

The following formula was developed to calculate the improvement in efficiency when adding a synchronous switch.

$$\text{Efficiency change} = \frac{(V_{IN} - V_{OUT})(V_f - R_{FET} \bullet I_{OUT})(E)^2}{(V_{IN})(V_{OUT})}$$

With V_{IN} = 10V, V_{OUT} = 5V, V_f (diode forward voltage) = 0.45V, R_{FET} = 0.1Ω and I_{OUT} = 1A the improvement in efficiency is only 2.8%. This does not take into account the losses associated with MOS gate drive, so real improvement would probably be closer to 2%. The availability of low forward voltage Schottky diodes such as the MBR330P makes synchronous switches less attractive than they used to be.

To achieve higher efficiency during sleep, the LT1432 has Burst Mode operation. In this mode the LT1271 is either driven full on, or completely shut down to its micropower state. The LT1432 acts as a comparator with hysteresis instead of a linear amplifier. This mode reduces equivalent input supply current to 1.3mA with a 12V battery. Battery life with NiCd AA cells is over 300 hours with a 1mA 5V load. Burst Mode operation increases output ripple, especially with higher output currents, so maximum load in this mode is 100mA.

The LT1271 normally draws about 50μA to100μA in its shutdown state. A shutdown command to the LT1432 opens all connections to the LT1271 V_{IN} pin so its current drain is eliminated. This leaves only the shutdown current of the LT1432 and the switch leakage of the LT1271, which typically add up to less than 20μA—less than the self-discharge rate of NiCd batteries. For many applications the on/off function is under keystroke control. Digital chips which draw only a few microamps are available for keystroke recognition and power control.

There is no way to design around inductor losses. These losses are minimized by using low loss cores such as molypermalloy or ferrite, and by sizing the core to use wire with sufficient diameter to keep resistive losses low. The 50μH inductor shown has a core loss of 200mW with type-52 powdered iron material and 28mW with molypermalloy. For a 1A load this represents efficiency losses of 4% and 0.56% respectively—a major difference. Ferrite cores would have even lower losses than molypermalloy, but the "moly" has such low losses that ferrites should be chosen for other reasons, such as height, cost, mounting and the like. DC resistance of the inductor shown is 0.02Ω. This represents an efficiency loss of 0.4% at 1A load and 0.8% at 2A. Significant reduction in these resistance losses would require a somewhat larger inductor. The choice is yours.

The LT1432 has a high efficiency current limit with a sense voltage of only 60mV. This has a side benefit in that printed circuit board trace material can be used for the sense resistor. A 3A limit requires a 0.02Ω sense resistor and this is easily made from a small section of serpentine trace. The 60mV sense voltage has a positive temperature coefficient that tracks that of copper so that the current limit is flat with temperature. Foldback current limiting can be easily implemented.

The LT1432 represents a significant improvement in high efficiency 5V supplies that must operate over a wide range of load currents and input voltages. Its efficiency has a very broad peak that exceeds 90%, requiring a new definition of the "holy grail." Logic controlled shutdown, millipower Burst Mode operation and efficient, accurate, current limiting make this regulator extremely attractive for battery-powered applications.

Regulators—Switching (Buck)

Low Power (<1A)

APPLICATIONS FOR THE LTC1265 HIGH EFFICIENCY MONOLITHIC BUCK CONVERTER

by San-Hwa Chee

Efficiency

Figure 30 shows a typical LTC1265-5 application circuit. The efficiency curves for two different input voltages are shown in Figure 31. Note that the efficiency for a 6V input exceeds 90% over a load range from less than 10mA to 850mA. This makes the LTC1265 attractive for all battery operated products and efficiency sensitive applications.

5V to 3.3V Converter

Figure 32 shows the LTC1265 configured for 3.3V output with 1A output current capability. This circuit operates at a frequency of 100kHz. Figure 33 is the efficiency plot of the circuit. At a load current of 100mA the efficiency is at 92%; the efficiency falls to 82% at a 1A output.

2.5mm Typical-Height 5V to 3.3V Regulator

Figure 34 shows the schematic for a very thin 5V to 3.3V converter. For the LTC1265 to be able to source 500mA output current and yet meet the height requirement, a small value inductor must be used. The circuit operates at a high frequency (500kHz typically) increasing the gate charge losses. Figure 35 is the efficiency curve for this application.

Positive-to-Negative Converter

Besides converting from a positive input to positive output, the LTC1265 can be configured to perform a positive-to-negative conversion. Figure 36 shows the schematic for this application.

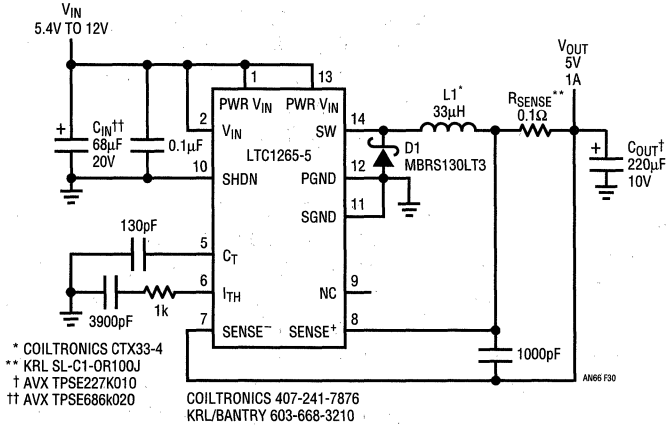


Figure 30. High Efficiency Step-Down Converter

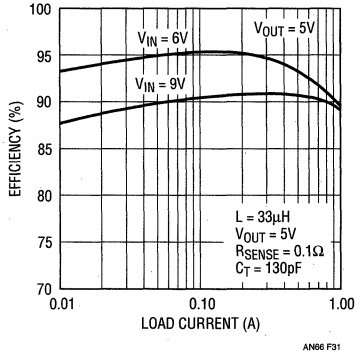


Figure 31. Efficiency vs Load Current

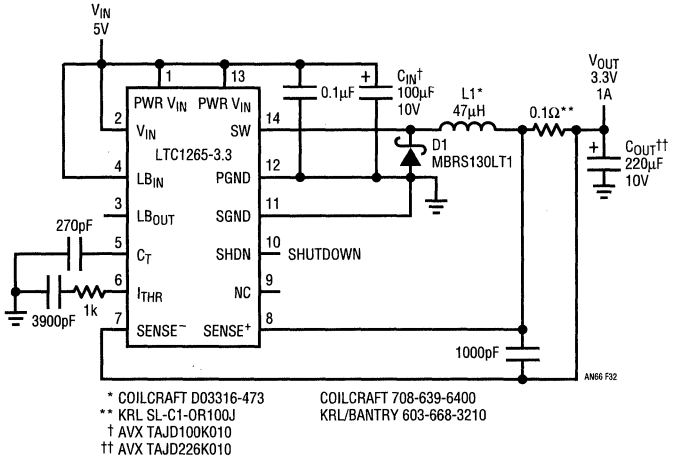


Figure 32. High Efficiency 5V to 3.3V Converter

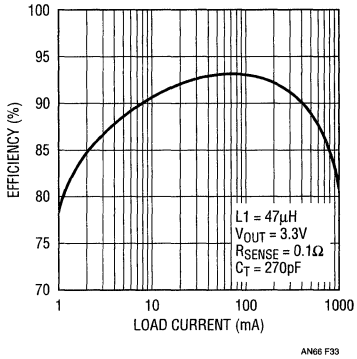


Figure 33. Efficiency vs Load Current

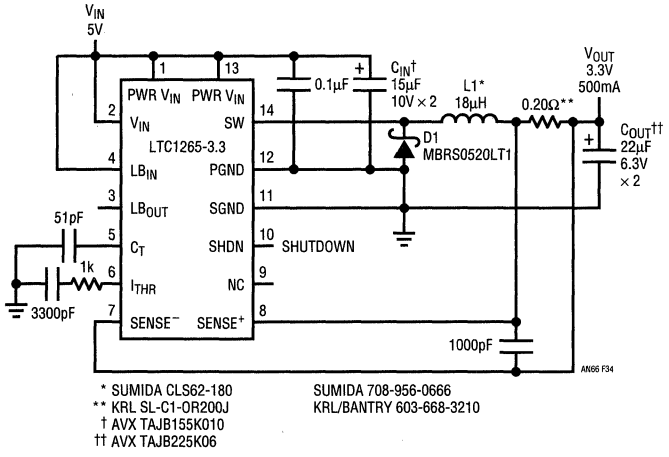


Figure 34. 2.5mm High 5V to 3.3V Converter (500mA Output Current)

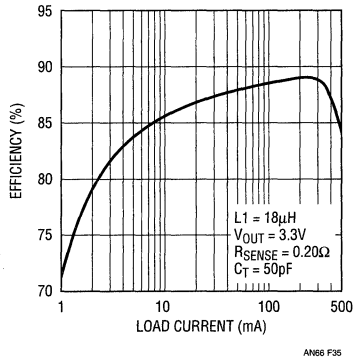
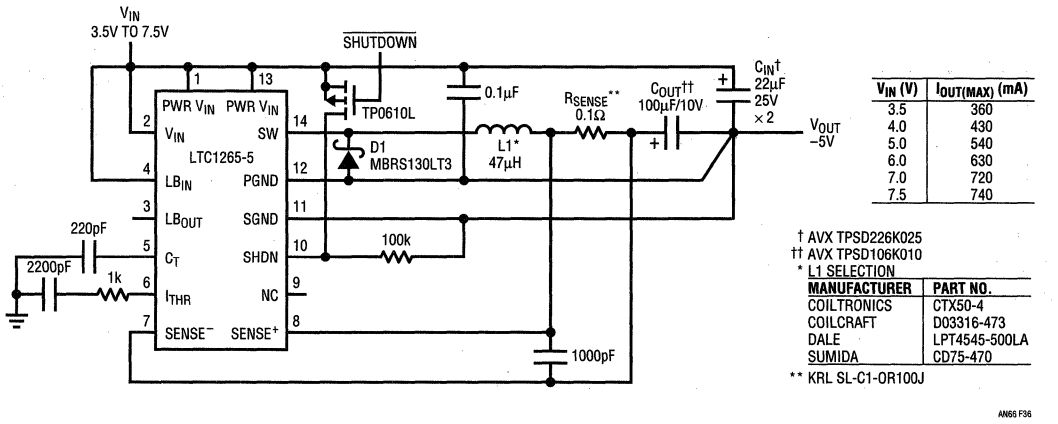


Figure 35. Efficiency vs Load Current



VIN (V)	IOUT(MAX) (mA)
3.5	360
4.0	430
5.0	540
6.0	630
7.0	720
7.5	740

Figure 36. Positive (3.5 to 7.5V) to Negative (–5V) Converter

Regulators—Switching (Boost)

Medium Power (1A to 4A)

HIGH OUTPUT CURRENT BOOST REGULATOR

by Dimitry Goder

Low voltage switching regulators are often implemented with self-contained power integrated circuits featuring a PWM controller and an onboard power switch. Maximum switch currents of up to 10A are available, providing a convenient means for power conversion over wide input and output voltage ranges. If higher switch currents are required, a controller with an external power MOSFET is a better choice.

Figure 37 shows an LTC1147-based 5V to 12V converter with 3.5A peak output current capability. The LTC1147 is a micropower controller that uses a constant off-time

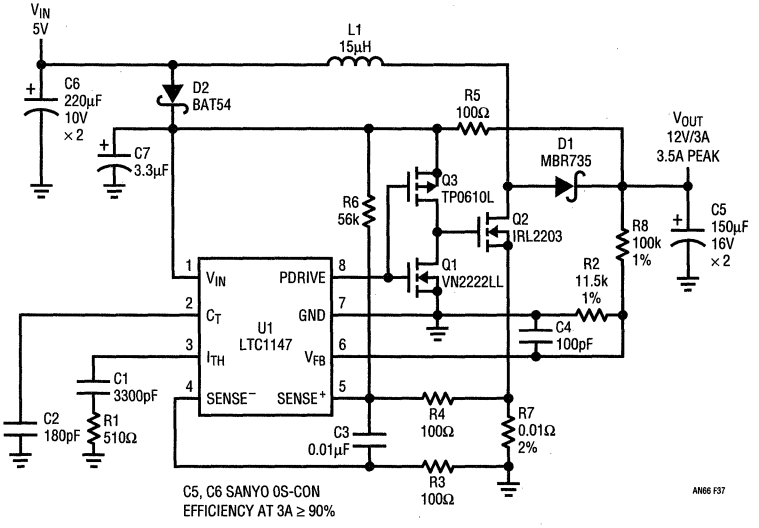


Figure 37. LTC1147-Based 5V to 12V Converter

architecture, eliminating the need for external slope compensation. Current mode control allows fast transient response and cycle-by-cycle current limiting. A maximum voltage of only 150mV across the current-sense resistor R7 optimizes performance for low input voltages.

When Q2 turns on, current starts building up in inductor L1. This provides a ramping voltage across R7. When this voltage reaches a threshold value set internally in the LTC1147, Q2 turns off and the energy stored in L1 is transferred to the output capacitor C5. Timing capacitor C2 sets the operating frequency. The controller is powered from the output through R5 providing 10V of gate drive for Q2. This reduces the MOSFET's ON resistance and allows efficiency to exceed 90% even at full load. The feedback network comprising R2 and R8 sets the output voltage. Current sense resistor R7 sets the maximum output current; it can be changed to meet different circuit requirements.

Regulators—Switching (Boost)

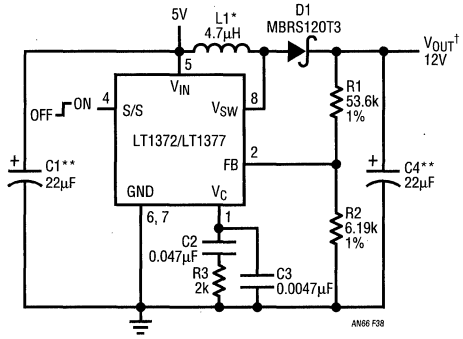
Low Power (<1A)

APPLICATIONS FOR THE LT1372 500kHz SWITCHING REGULATOR

by Bob Essaff

Boost Converter

The boost converter in Figure 38 shows a typical LT1372 application. This circuit converts an input voltage, which can vary from 2.7V to 11V, into a regulated 12V output. Using all surface mount components, the entire boost converter consumes only 0.5 square inches of board space. Figure 39 shows the circuit's efficiency, which can reach 89% on a 5V input.



*COILCRAFT DO1608-472 (4.7µH) OR
COILCRAFT DT3316-103 (10µH) OR
SUMIDA CD43-4R7 (4.7µH) OR
SUMIDA CD73-100KC (10µH) OR
**AVX TPSD226M025R0200

†MAX I_{OUT}

L1	I_{OUT}
4.7µH	0.25A
10µH	0.35A

Figure 38. 5V to 12V Boost Converter

The reference voltage on the FB pin is trimmed to 1.25V and the output voltage is set by the R1/R2 resistor divider ratio ($V_{OUT} = V_{REF} \bullet (R1/R2 + 1)$. R3 and C2 frequency compensate the circuit.

Positive-to-Negative Flyback with Direct Feedback

A unique feature of the LT1372 is its ability to directly regulate negative output voltages. As shown in the positive-to-negative flyback converter in Figure 40, only two resistors are required to set the output voltage. The reference voltage on the NFB pin is $-2V_{REF}$, making $V_{OUT} = -2V_{REF} \bullet (R2/R3 + 1)$. Efficiency for this circuit reaches 72% on a 5V input.

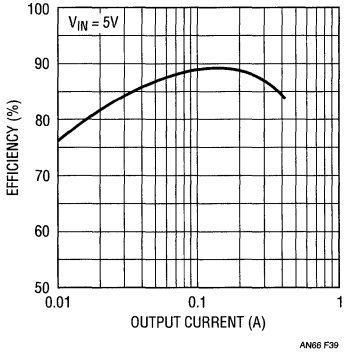


Figure 39. 12V Output Efficiency

Dual Output Flyback with Overvoltage Protection

Multiple-output flyback converters offer an economical means of producing multiple output voltages, but the power supply designer must be aware of cross regulation issues, which can cause electrical overstress on the supply and loads. Figure 41 is a dual-output flyback converter with overvoltage protection. Typically, in multiple-output flyback designs only one output is voltage sensed and regulated. The remaining outputs are "quasi-regulated" by the turns ratios of the transformer secondary. Cross regulation is a function of the transformer used and is a measure of how well the quasi-regulated outputs maintain regulation under varying load conditions. For evenly loaded outputs, as shown in Figure 42, cross regulation can be quite good, but when the loads differ greatly, as in the case of a load disconnect, there may be trouble. Figure 43 shows that when only the 15V output is voltage sensed, the –15V quasi-regulated output exceeds –25V when unloaded. This can cause electrical overstress on the output capacitor, output diode and the load when reconnected. Adding output voltage clamps is one way to fix the problem but the circuit in Figure 41 eliminates this requirement. This circuit senses both the 15V and –15V outputs and prevents either from going beyond its regulating value. Figure 44 shows the unloaded –15V output being held constant. The circuit's efficiency, which can reach 79% on a 5V input, is shown in Figure 45.

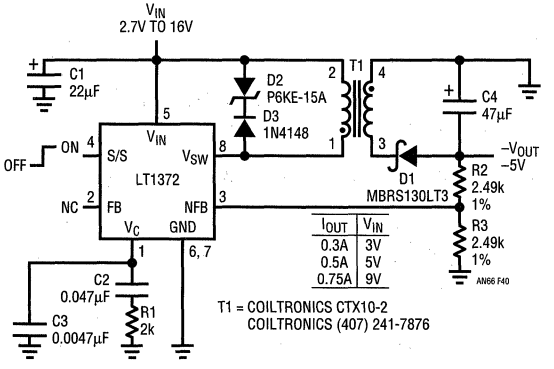


Figure 40. LT1372's Positive-to-Negative Converter with Direct Feedback

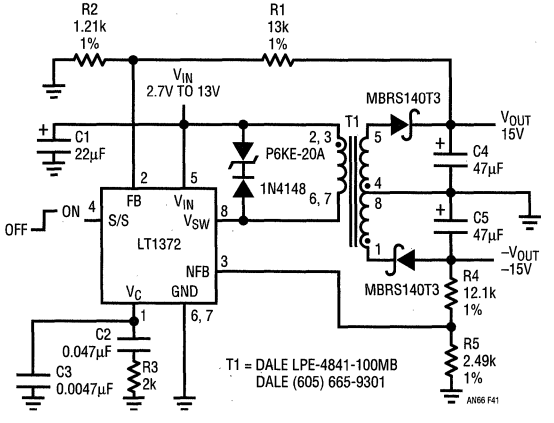


Figure 41. LT1372 Dual Output Flyback Converter with Overvoltage Protection

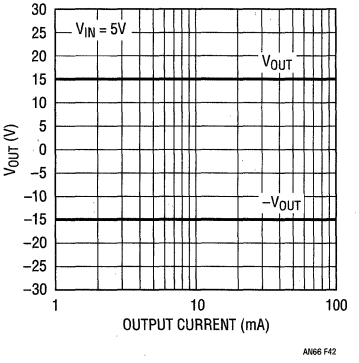


Figure 42. Cross Regulation of Figure 41's Circuit. V_{OUT} and $-V_{OUT}$ Evenly Loaded

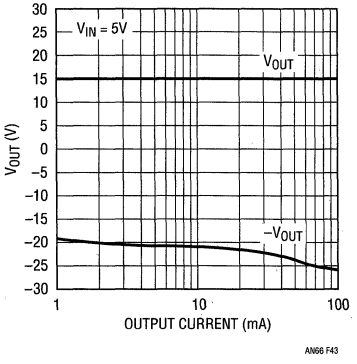


Figure 43. Cross Regulation of Figure 41's Circuit. $-V_{OUT}$ Unloaded; Only V_{OUT} Voltage Sensed

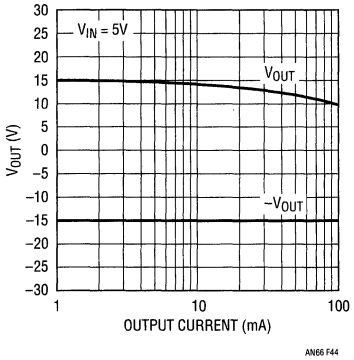


Figure 44. Cross Regulation of Figure 41's Circuit. $-V_{OUT}$ Unloaded; Both $-V_{OUT}$ and V_{OUT} Sensed

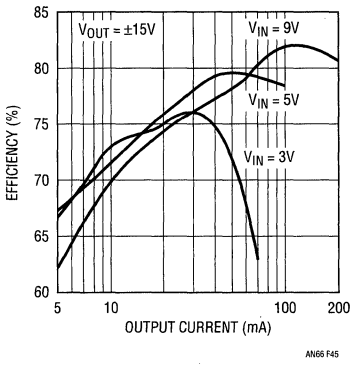


Figure 45. Efficiency of Dual Output Flyback Converter in Figure 41

Regulators—Switching (Buck/Boost)

±5V CONVERTER USES OFF-THE-SHELF SURFACE MOUNT COIL

By Mitchell Lee and Kevin Vasconcelos

Single-output switching regulator circuits can often be adapted to multiple output configurations with a minimum of changes, but these transformations usually call for custom wound inductors. A new series of standard inductors,[1] featuring quadrifilar windings, allows power supply designers to take advantage of these modified circuits but without the risks of a custom magnetics development program.

The circuit shown in Figure 46 fulfills a recent customer requirement for a 9V to 12V input, 5V/800mA and –5V/100mA output converter. It employs a 1:1 overwinding on what is ostensibly a buck converter to provide a –5V output. The optimum solution would be a bifilar wound coil with heavy gauge wire for the main 5V output and smaller wire for the overwinding. To avoid a custom coil design, an off-the-shelf JUMBO-PAC™ quadrifilar wound coil is used. This family of coils is wound with

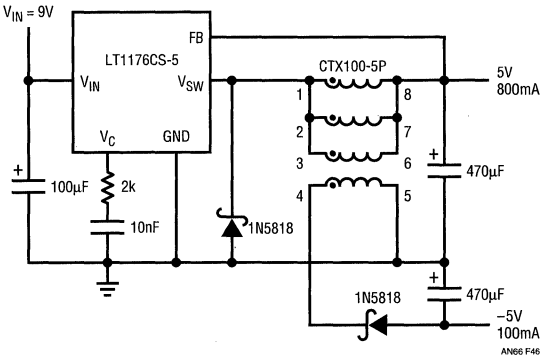


Figure 46. 5V Buck Converter with –5V Overwinding

1:1:1:1 sections. In the application of Figure 46, three sections are paralleled for the main 5V winding and the remaining section is used for the –5V output. This concentrates the copper where it is needed most—on the high current output.

Efficiency with the outputs loaded at 500mA and –50mA is over 80%. Minimum recommended load on the –5V output is 1mA to 2mA, and the –5V load current must always be less than the 5V load current.

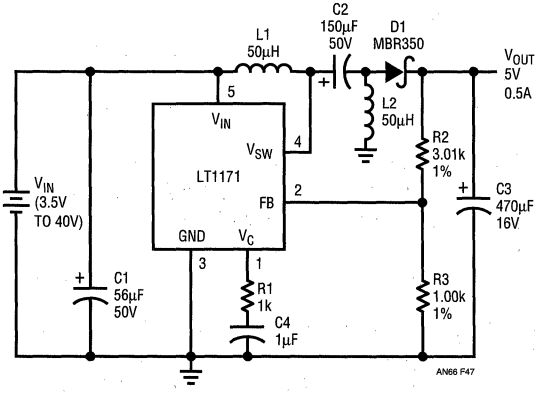
[1] JUMBO-PAC is a trademark of Coiltronics Inc. (407) 241-7876.

SWITCHING REGULATOR PROVIDES CONSTANT 5V OUTPUT FROM 3.5V TO 40V INPUT WITHOUT A TRANSFORMER

by Brian Huffman

A common switching regulator requirement is to produce a constant output voltage from an input voltage that varies above or below the output voltage. This is particularly important for extending battery life in battery-powered applications. Figure 47 shows how an LT1171 switching regulator IC, two inductors and a "flying" capacitor can generate a constant output voltage that is independent of input voltage variations. This is accomplished without the use of a transformer. Inductors are preferred over transformers because they are readily available and more economical.

The circuit in Figure 47 uses the LT1171 to control the output voltage. A fully self-contained switching regulator IC, the LT1171 contains a power switch as well as the control circuitry (pulse-width modulator, oscillator, reference voltage, error amplifier and protection circuitry). The power switch is an NPN transistor in a common-emitter configuration; when the switch turns on, the LT1171's V_{SW} pin is connected to ground. This power switch can handle peak switch currents of up to 2.5A.



C1 = NICHICON (AL) UPL1H560MEH, ESR = 0.250Ω, I_{RMS} = 360mA
C2 = NICHICON (AL) UPL1H151MPH, ESR = 0.100Ω, I_{RMS} = 820mA
C3 = NICHICON (AL) UPL1C471MPH, ESR = 0.090Ω, I_{RMS} = 770mA
L1, L2 = COILTRONICS CTX50-4, DCR = 0.090Ω,
COILTRONICS (407) 241-7876

EQUATION 1: $V_{OUT} = 1.25V (1 + R2/R3)$

Figure 47. LT1171 Provides Constant 5V Output from 3.5V to 40V Input. No Transformer Is Required

Figure 48 shows the operating waveforms for the circuit. In this architecture the capacitor C2 serves as the single energy transfer device between the input voltage and output voltage of the circuit. While the LT1171 power switch is off, diode D1 is forward biased, providing a path for the currents from inductors L1 and L2. Trace A shows inductor L1's current waveform and trace B is L2's current waveform. Observe that the inductor current waveforms occur on top of a DC level. The waveforms are virtually identical because the inductors have identical inductance values and the same voltages are applied across them. The current flowing through inductor L1 is not only delivered to the load but is also used to charge C2. C2 is charged to a potential equal to the input voltage.

When the LT1171 power switch turns on, the V_{SW} pin is pulled to ground and the input voltage is applied across the inductor L1. At the same time, capacitor C2 is connected across inductor L2. Current flows from the input voltage source through inductor L1 and into the LT1171. Trace C shows the voltage at the V_{SW} pin and Trace D is the current flowing through the power switch. The catch diode (D1) is reverse biased and capacitor C2's current also flows through the switch, through ground and into inductor L2. During this interval C2 transfers its stored energy into inductor L2. After the switch turns off the cycle is repeated.

Another advantage of this circuit is that it draws its input current in a triangular waveshape (see Trace A in Figure 48). The current waveshape of the input capacitor is identical to the current waveshape of inductor L1 except that the capacitor's current has no DC component. This type of ripple injects only a modest amount of noise into the input lines because the ripple does not contain any sharp edges.

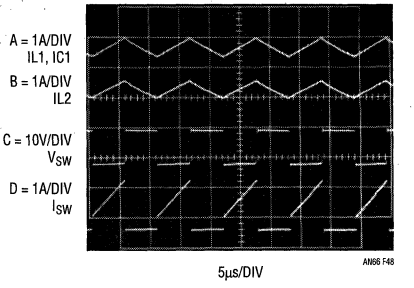


Figure 48. LT1171 Switching Waveforms

Figure 49 shows the efficiency of this circuit for a 0.5A load and maximum output current for various input voltages. The two main loss elements are the output diode (D1) and the LT1171 power switch. A Schottky diode is chosen for its low forward voltage drop; it introduces a 10% loss, which is relatively constant with input voltage variations. At low input voltages the efficiency drops because the LT1171 power switch's saturation voltage becomes a higher percentage of the available input supply.

This circuit can deliver an output current of 0.5A at a 3.5V input voltage. This rises to 1A as input voltage is increased. Above 20V, higher output currents can be achieved by increasing the values of inductors L1 and L2. Larger inductances store more energy, providing additional current to the load. If 0.5A of output current is insufficient, use a higher current part, such as the LT1170.

The output voltage is controlled by the LT1171 internal error amplifier. This error amplifier compares a fraction of the output voltage, via the R1 to R2 divider network shown in Figure 47, with an internal 1.25V reference voltage, and varies the duty cycle until the two values are equal. (The duty cycle is determined by multiplying the switch ON time by the switching frequency.) The RC network (R1 and C4 in Figure 47) connected to the V_C pin provides sufficient compensation to stabilize this control loop. Equation 1 (see Figure 47) can be used to determine the output voltage.

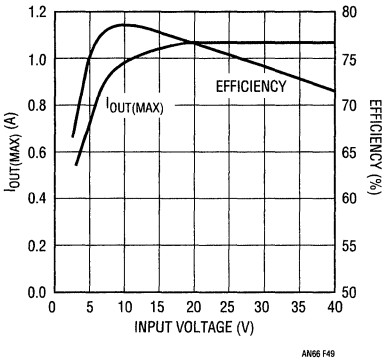


Figure 49. Efficiency and Load Characteristics for Various Input Voltages

SWITCHING REGULATOR PROVIDES ±15V OUTPUT FROM AN 8V TO 40V INPUT WITHOUT A TRANSFORMER

by Brian Huffman

Many systems derive ±15V supplies for analog circuitry from an input voltage that may be above or below the 15V output. The split supply requirement is usually fulfilled by a switcher with a multiple-secondary transformer or by multiple switchers. An alternative approach, shown in Figure 50, uses an LT1074 switching regulator IC, two inductors and a "flying" capacitor to generate a dual-output supply that accepts a wide range of input voltages. This solution is particularly noteworthy because it uses only one switching regulator IC and does not require a transformer. Inductors are preferred over transformers because they are readily available and more economical.

The operating waveforms for the circuit are shown in Figure 51. During the switching cycle, the LT1074's V_{SW} pin swings between the input voltage (V_{IN}) and the negative output voltage ($-V_{OUT}$). (The ability of the LT1074's V_{SW} pin to swing below ground is unusual—most other 5-pin buck switching regulator ICs cannot do this.) Trace A shows the waveform of the V_{SW} pin voltage and Trace B is the current flowing through the power switch.

While the LT1074 power switch is on, current flows from the input voltage source through the switch, through capacitor C2 and inductor L1 (Trace C), and into the load. A portion of the switch current also flows into inductor L2 (Trace D). This current is used to recharge C2 and C4 during the switch OFF time to a potential equal to the positive output voltage (V_{OUT}). The current waveforms for both inductors occur on top of a DC level.

The waveforms are virtually identical because the inductors have identical values and because the same voltage potentials are applied across them during the switching cycles.

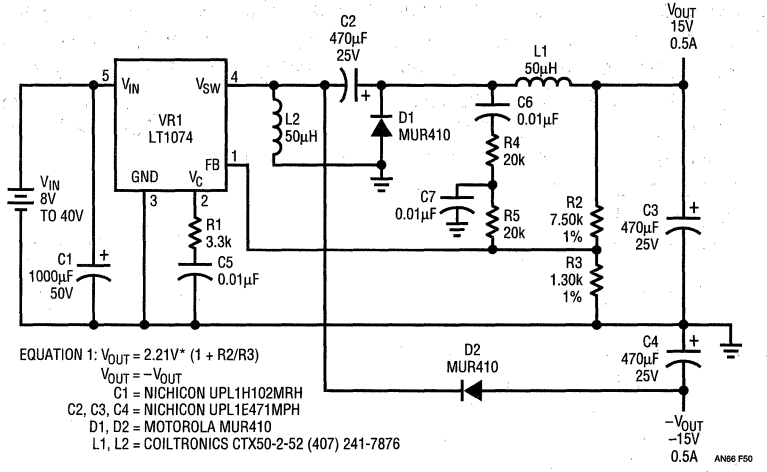


Figure 50. Schematic Diagram for ±15V Version

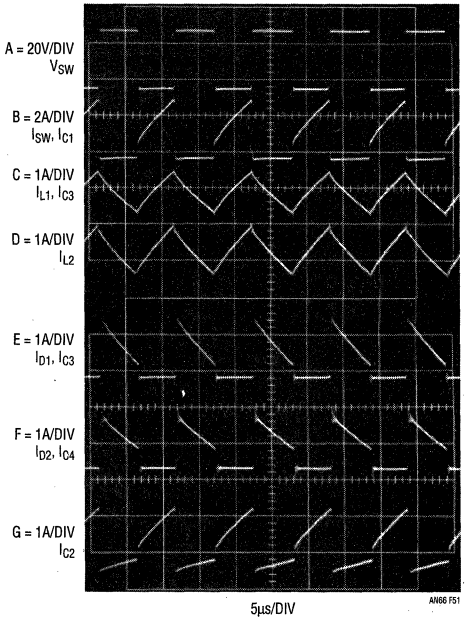


Figure 51. LT1074 Switching Waveforms

When the switch turns off, the current in L1 and L2 begins to ramp downward, causing the voltages across them to reverse polarity and forcing the voltage at the V_{SW} pin below ground. The V_{SW} pin voltage falls until diodes D1 (Trace E) and D2 (Trace F) are forward biased. During this interval the voltage on the V_{SW} pin is equal to a diode drop below the negative output voltage ($-V_{OUT}$). L2's current then circulates between both D1 and D2, charging C2 and C4. The energy stored in L1 is used to replace the energy lost by C2 and C4 during the switch ON time. Trace G is capacitor C2's current waveform. Capacitor C4's current waveform (Trace F) is the same as diode D2's current less the DC component. Assuming that the forward voltage drops of diodes D1 and D2 are equal, the negative output voltage ($-V_{OUT}$) will be equal to the positive output voltage (V_{OUT}). After the switch turns on again the cycle is repeated.

Figure 52 shows the excellent regulation of the negative output voltage for various output currents. The negative

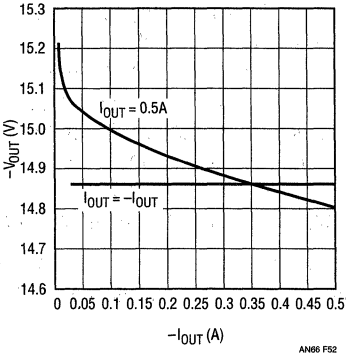


Figure 52. –15V Output Regulation Characteristics

output voltage tracks the positive supply (V_{OUT}) within 200mV for load variations from 50mA to 500mA. Negative output load current should not exceed the positive output load by more than a factor of 4; the imbalance causes loop instabilities. For common load conditions the two output voltages track each other perfectly.

Another advantage of this circuit is that inductor L1 acts as both an energy storage element and as a smoothing filter for the positive output (V_{OUT}). The output ripple voltage has a triangular waveshape whose amplitude is determined by the inductor ripple current (see trace C of Figure 51) and the ESR (effective series resistance) of the output capacitor (C3). This type of ripple is usually small so a post filter is not necessary.

Figure 53 shows the efficiency for a 0.5A common load at various input voltages. The two main loss elements are the output diodes (D1 and D2) and the LT1074 power switch. At low input voltages, the efficiency drops because the switch's saturation voltage becomes a higher percentage of the available input supply.

The output voltage is controlled by the LT1074 internal error amplifier. This error amplifier compares a fraction of the output voltage, via the R2 to R3 divider network shown in Figure 50, with an internal 2.21V reference voltage and then varies the duty cycle until the two values are equal. The RC network (R1 and C5 in Figure 50) connected to the V_C pin along with the R4/R5 and C6/C7 network provides sufficient compensation to stabilize the control loop. Equation 1 can be used to determine the output voltage.

Figure 54 shows the circuit's –5V load regulation characteristics and Figure 55 shows its efficiency.

Refer to the schematic diagram in Figure 56 for modified component values to provide ±5V at 1A.

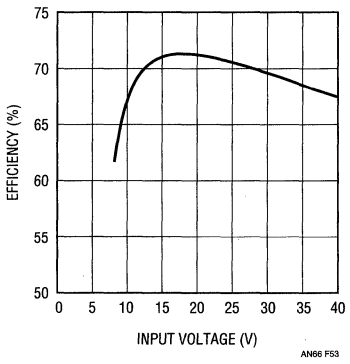


Figure 53. ±15V Efficiency Characteristics with 0.5A Common Load

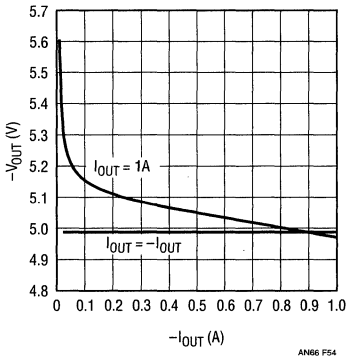


Figure 54. –5V Output Regulation Characteristics

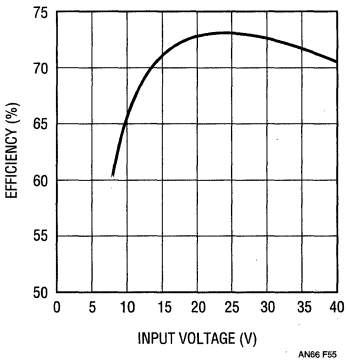


Figure 55. ±5V Efficiency Characteristics with 1A Common Load

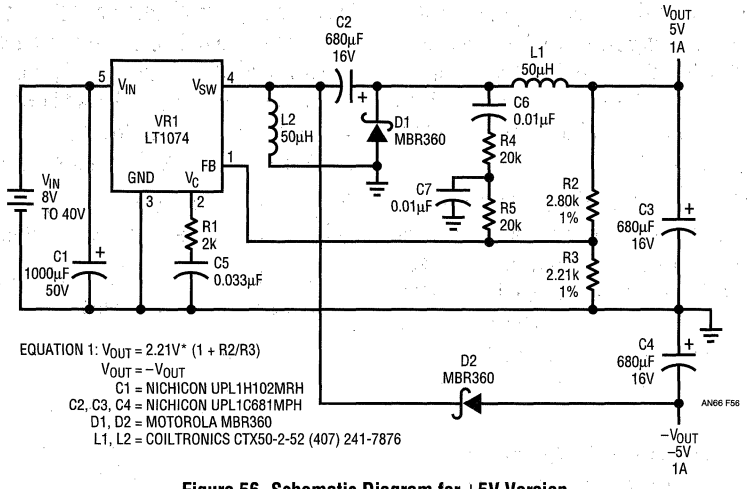


Figure 56. Schematic Diagram for ±5V Version

Regulators—Switching (Inverting)

HIGH EFFICIENCY 12V TO –12V CONVERTER

by Milton Wilcox and Christophe Franklin

It is difficult to obtain high efficiencies from inverting switching regulators because the peak switch and inductor currents must be roughly twice the output current. Furthermore, the switch node must swing twice the input voltage (24V for a 12V inverting converter). The adjustable version of the LTC1159 synchronous stepdown controller is ideally suited for this application, producing a combination of better than 80% efficiency, low quiescent current and 20µA shutdown current.

The 1A circuit shown in Figure 57 exploits the high input-voltage capability of the LTC1159 by connecting the controller ground pins to the –12V output. This allows the simple feedback divider between ground and the output (comprising R1 and R2) to set the regulated voltage, since the internal 1.25V reference rides on the negative output. The inductor connects to ground via the 0.05Ω current-sense resistor.

A unique EXT V_{CC} pin on the LTC1159 allows the MOSFET drivers and control circuitry to be powered from the output of the regulator. In Figure 57 this is accomplished by grounding EXT V_{CC}, placing the entire 12V output voltage across the driver and control circuits (remember the ground pins are at –12V). This is permissible with the LTC1159, which allows a maximum of 13V between the Sense and Ground pins. During start-up or short-circuit conditions, operating power is supplied by an internal 4.5V low dropout linear regulator. This start-up regulator automatically turns off when the output falls below –4.5V.

A cycle of operation begins when Q1 turns on, placing the 12V input across the inductor. This causes the inductor current to ramp to a level set by the error amplifier in the LTC1159. Q1 then turns off and Q2 turns on, causing the current stored in the inductor to flow to the –12V output. At the end of the 5µs off-time (set by capacitor C_T), Q2 turns off and Q1 resumes conduction. With a 12V input the duty cycle is 50%, resulting in a 100kHz operating frequency.

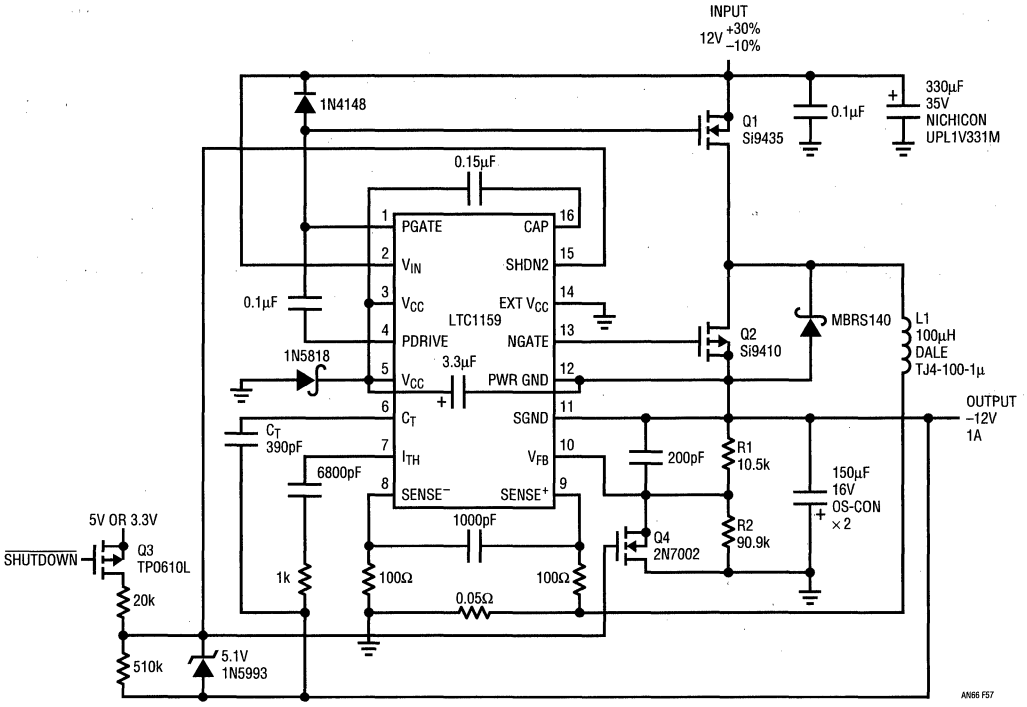


Figure 57. LTC1159 Converts 12V to –12V at 1A

The LTC1159, like other members of the LTC1148 family, automatically switches to Burst Mode operation at low output currents. Figure 57's circuit enters Burst Mode operation below approximately 200mA of load current. This maintains operating efficiencies exceeding 65% over two decades of load current range, as shown in Figure 58. Quiescent current (measured with no load) is 1.8mA.

Complete shutdown is achieved by pulling the gate of Q3 low. Q3, which can be interfaced to either 3.3V or 5V logic, creates a 5V shutdown signal referenced to the negative output voltage to activate the LTC1159 Shutdown 2 pin. Additionally, Q4 offsets the V_{FB} pin to ensure that Q1 and Q2 remain off during the entire shutdown sequence. In shutdown conditions, 40µA flows in Q3 and only 20µA is taken from the 12V input.

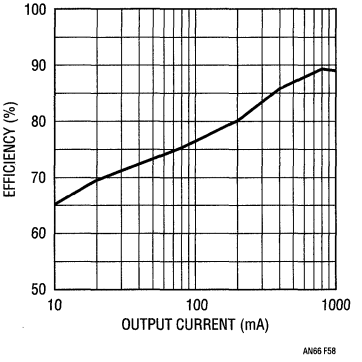


Figure 58. Efficiency Plot of Figure 57's Circuit

REGULATED CHARGE PUMP POWER SUPPLY

by Tommy Wu

The circuit shown in Figure 59 uses an LTC1044A charge pump inverter to convert a 5V input to a –1.7V potential as required for a certain LCD panel. Output regulation is provided by a novel feedback scheme, which uses components Q1, R1 and R2. Without feedback the charge pump would simply develop approximately –5V at its output. With feedback applied, V_{OUT} charges in the negative direction until the emitter of Q1 is biased by the divider comprising R1 and R2. Current flowing in the collector tends to slow the LTC1044A's internal oscillator, reducing the available output current. The output is thereby maintained at a constant voltage.

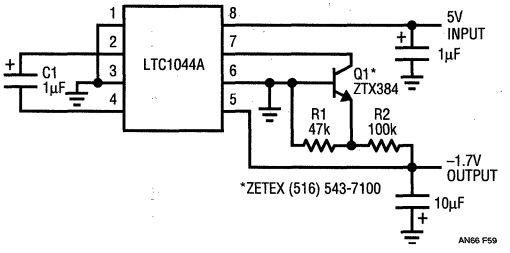


Figure 59. Regulated Charge Pump

In this application less than 5mA output current is required. As a result, charge pump capacitor C1 is reduced to 1µF from the usual 10µF. Curves of output voltage with and without feedback are shown in Figure 60. The equivalent output impedance of the charge pump is reduced from approximately 100Ω to 5Ω.

A variety of output voltages within the limits of the curve in Figure 60 can be set by simply adjusting the V_{BE} multiplier action of Q1, R1 and R2. Tighter regulation or a higher tolerance could be obtained by adding a reference or additional gain, at the expense of increased complexity and cost.

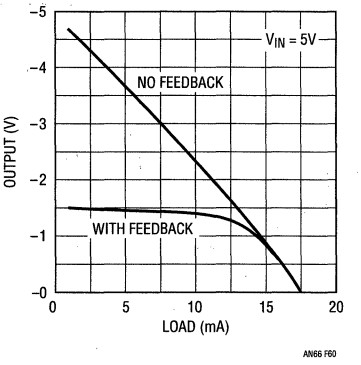


Figure 60. Effect of Feedback on Output Voltage

LTC1174: A HIGH EFFICIENCY BUCK CONVERTER

by San-Hwa Chee and Randy Flatness

The LTC1174 is an 8-pin SO "user-friendly" step-down converter. (A PDIP package is also available.) Only four external components are needed to construct a complete high efficiency converter. With no load it requires only 130µA of quiescent current; this decreases to a mere 1µA upon shutdown. The LTC1174 is protected against output shorts by an internal current limit, which is pin selectable to either 340mA or 600mA. This current limit also sets the inductor's peak current. This allows the user to optimize the converter's efficiency depending upon the output current requirement.

In dropout conditions, the internal 0.9Ω (at a supply voltage of 9V) power P-channel MOSFET switch is turned on continuously (DC), thereby maximizing the life of the battery source. (Who says a switcher has to switch?) In addition to the features already mentioned, the LTC1174 boasts a low-battery detector. All versions function down to an input voltage of 4V and work up to an absolute maximum of 13.5V. For extended input voltage, high voltage parts are also available that can operate up to an absolute maximum of 18.5V.

5V Output Applications

Figure 61 shows a practical LTC1174-5 circuit with a minimum of components. Efficiency curves for this circuit at two different input voltages are shown in Figure 62. Note that the efficiency is 94% at a supply voltage of 6V and load current of 175mA. This makes the LTC1174 attractive to all power sensitive applications and shows clearly why switching regulators are gaining dominance over linear regulators in battery-powered devices.

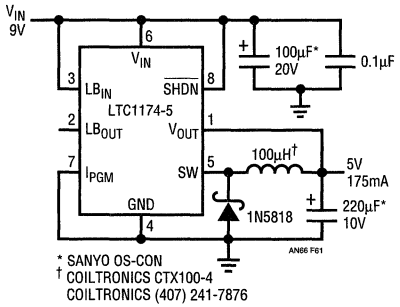


Figure 61. Typical Application for Low Output Currents

If higher output currents are desired Pin 7 (I_{PGM}) can be connected to V_{IN}. Under this condition the maximum load current is increased to 450mA. The resulting circuit and efficiency curves are shown in Figures 63 and 64 respectively.

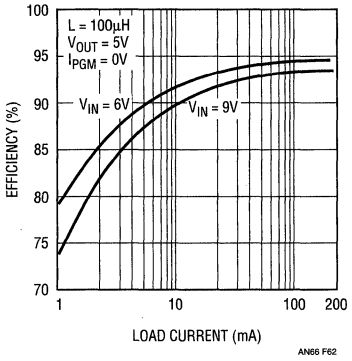


Figure 62. Efficiency vs Load Current

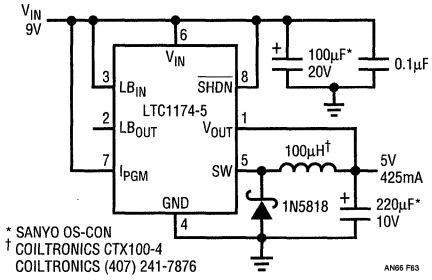


Figure 63. Typical Application for Higher Output Currents

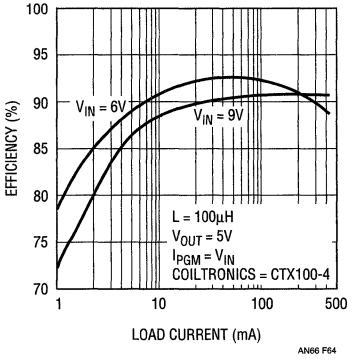


Figure 64. Efficiency vs Load Current

More Applications

Positive-to-Negative Converter

The LTC1174 can easily be set up for a negative output voltage. The LTC1174-5 is ideal for –5V outputs as this configuration requires the fewest components. Figure 65 shows the schematic for this application with low-battery detection capability. The LED will turn on at input voltages below 4.9V. The efficiency of this circuit is 81% at an input voltage of 5V and output current of 150mA.

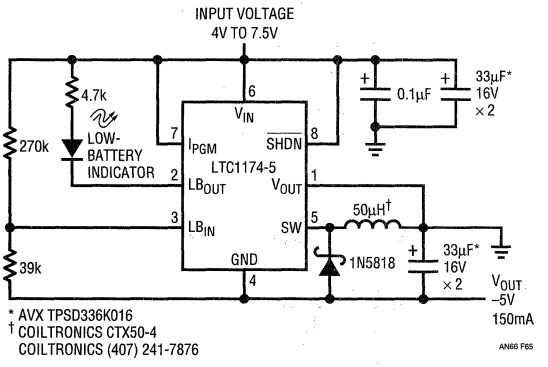


Figure 65. Positive to –5V Converter with Low-Battery Detection

A 5V to 3.3V Converter

The LTC1174-3.3 is ideal for applications that require 3.3V at less than 450mA. A minimum board area surface mount 3.3V regulator is shown in Figure 66. Figure 67 shows that this circuit can achieve efficiency greater than 85% for load currents between 5mA and 450mA.

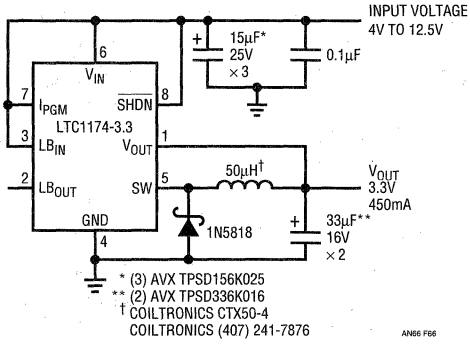


Figure 66. 5V to 3.3V Output Application

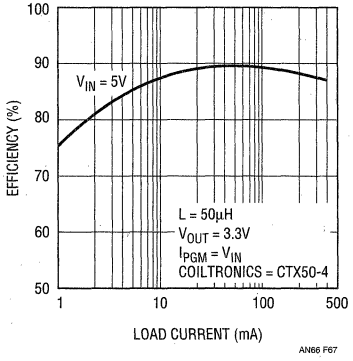


Figure 67. Efficiency vs Load Current

Regulators—Switching (Power Factor Corrected)

THE NEW LT1508/LT1509 COMBINES POWER FACTOR CORRECTION AND A PWM IN A SINGLE PACKAGE

by Kurk Mathews

Typical Application

Figure 68 shows a 24VDC, 300W, power-factor corrected, universal input supply. The continuous, current mode boost PFC preregulator minimizes the differential mode input filter size required to meet European low frequency conducted emission standards while providing a high power factor. The 2-transistor forward converter offers many benefits, including low peak currents, a nondissipative snubber, 500VDC switches and automatic core reset guaranteed by the LT1509's 50% maximum duty-cycle limitation. An LT1431 and inexpensive optoisolation are used to close the loop conservatively at 3kHz with excess phase margin (see Figure 69). Figure 70 shows the output voltage's response to a 2A to almost 10A current step. Regulation is maintained to within 0.5V. Efficiency curves for output powers of 30W, 150W and 300W are shown in Figure 71. The PFC preregulator alone has efficiency numbers of between about 87% and 97% over line and load.

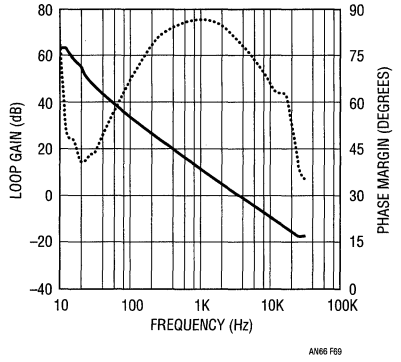


Figure 69. Bode Plot ot the Circuit Shown in Figure 68

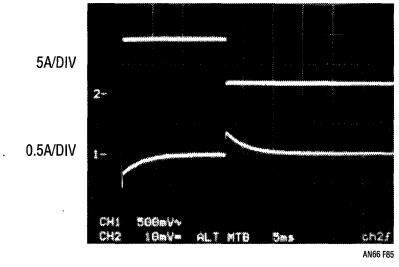


Figure 70. Figure 68's Response to a 2A to ≈10A Load Step

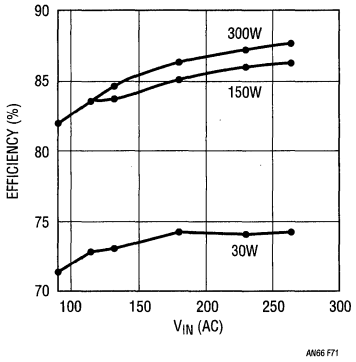


Figure 71. Efficiency Curves for Figure 68's Circuit

Start-up of the circuit begins with the LT1509's V_{CC} bypass capacitors trickle charging through 91kΩ to 16VDC, overcoming the chip's 0.25mA typical start-up current ($V_{CC} \leq$ lockout voltage). PFC soft start is then released, bringing up the 382VDC bus with minimal overshoot. As the bus voltage reaches its final value, the forward converter comes up powering the LT1431 and closing the feedback loop. A 3-turn secondary added to the 70-turn primary of T1 bootstraps V_{CC} to about 15VDC, supplying the chip's 13mA requirement as well as about 39mA to cover the gate current of the three FETs and high side transformer losses. A 0.15Ω sense resistor senses input current and compares it to a reference current (I_M) created by the outer voltage loop and multiplier. Thus, the input current follows the input line voltage and changes, as necessary, in order to maintain a constant bank voltage. The forward converter sees a voltage input of 382VDC unless the line voltage drops out, in which case the 470µF main capacitor discharges to 250VDC before the PWM stage is shut down. Compared to a typical off-line converter, the effective input voltage range of the forward converter is smaller, simplifying the design. Additionally, the higher bus voltage provides greater hold-up times for a given capacitor size. The high side transformer effectively delays the turn-on spike to the end of the built-in blanking time, necessitating the external blanking transistor.

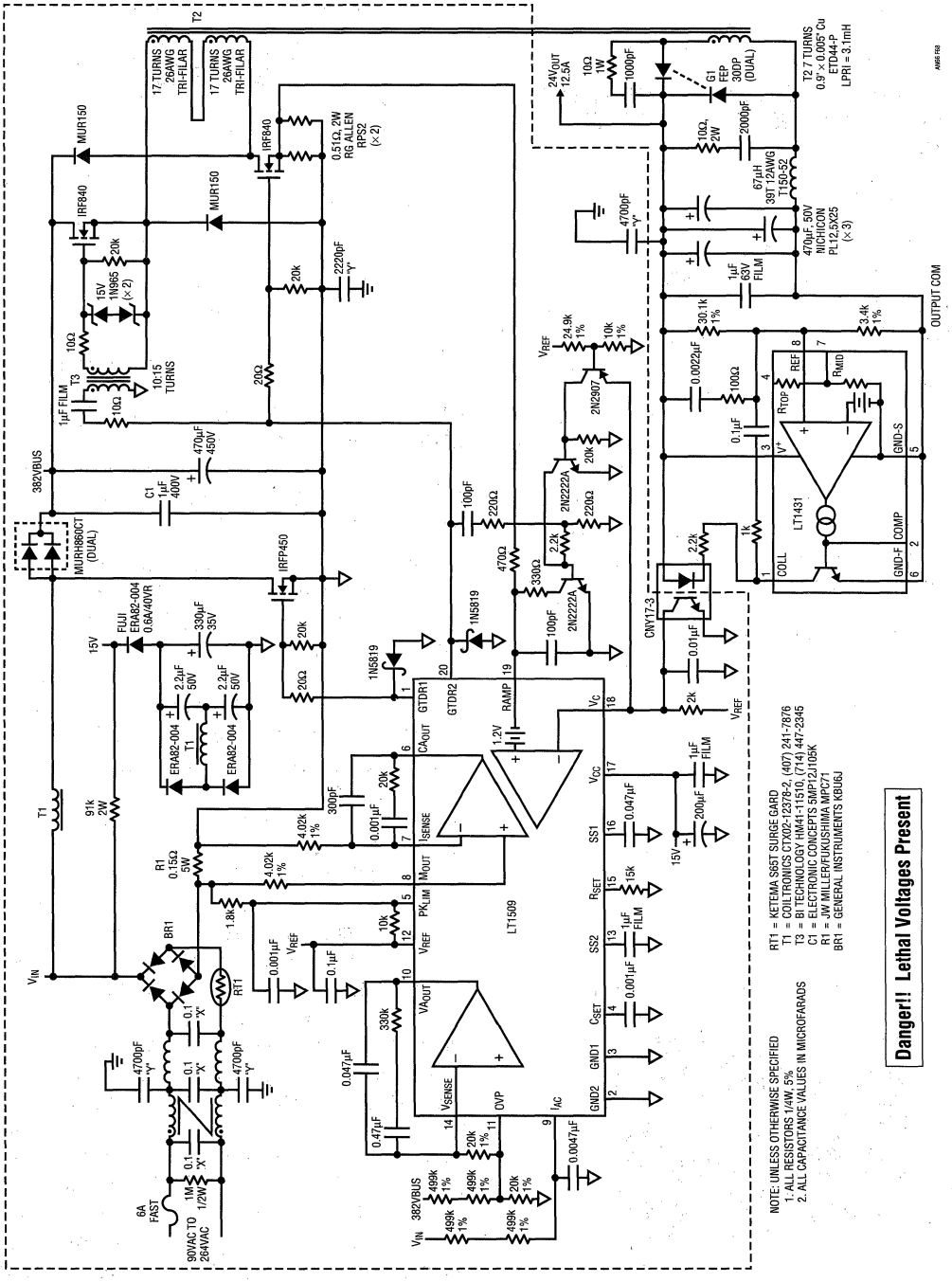


Figure 68. Schematic Diagram of 300W 24VDC Output Power Factor Corrected Universal Input Supply

Regulators—Switching (Discussion)

ADDING FEATURES TO THE BOOST TOPOLOGY

by Dimitry Goder

A boost-topology switching regulator is the simplest solution for converting a 2- or 3-cell input to a 5V output. Unfortunately, boost regulators have some inherent disadvantages, including no short-circuit protection and no shutdown capability. In some battery-operated products, external chargers or adapters can raise the battery voltage to a potential higher than the 5V output. Under this condition a boost converter cannot maintain regulation—the high input voltage feeds through the diode to the output.

The circuit shown in Figure 72 overcomes these problems. An LT1301 is used as a conventional boost converter, preserving simplicity and high efficiency in the boost mode. Transistor Q1 adds short-circuit limiting, true shutdown and regulation when there is a high input voltage.

When the input voltage is lower than 4V and the regulator is enabled, Q1's emitter is driven above its base, saturating the transistor. As a result, the voltages on C1 and C2 are roughly the same and the circuit operates as a conventional boost regulator.

If the input voltage increases above 4V, the internal error amplifier, acting to keep the output at 5V, boosts the voltage on C1 to a level greater than 1V above the input. This voltage controls Q1 to provide the desired output with the transistor operating as a linear pass element. The output does not change abruptly during the switch-over between step-up and step-down modes because it is monitored in both modes by the same error amplifier.

Figure 73 shows efficiency versus input voltage for 5V/100mA output. The break point at 4.25V is evidence of Q1 beginning to operate in a linear mode with an attendant roll-off of efficiency. Below 4.25V the circuit operates as a boost regulator and maintains high efficiency across a broad range of input voltages.

The circuit can be shut down by pulling the LT1301's Shutdown pin high. The LT1301 ceases switching and Q1 automatically turns off, fully disconnecting the output. This stays true over the entire input voltage range.

Q1 also provides overload protection. When the output is shorted the LT1301 operates in a cycle-by-cycle current limit. The short-circuit current depends on the maximum switch current of the LT1301 and on the Q1's gain, typically reaching 200mA. The transistor can withstand overload for several seconds before heating up. For sustained faults the thermal effects on Q1 should be carefully considered.

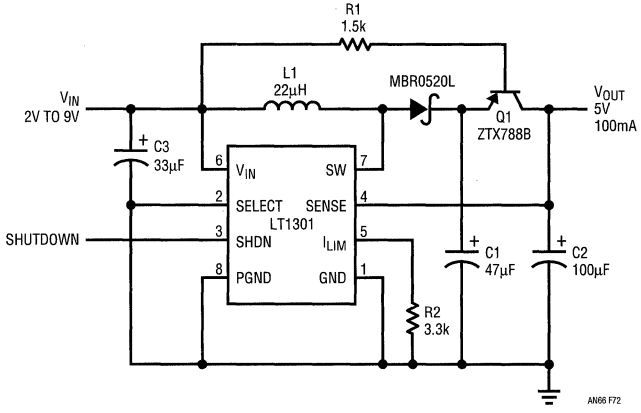


Figure 72. Q1 Adds Short-Circuit Limiting, True Shutdown and Regulation When There Is a High Input Voltage to the LT1301 in Boost Mode

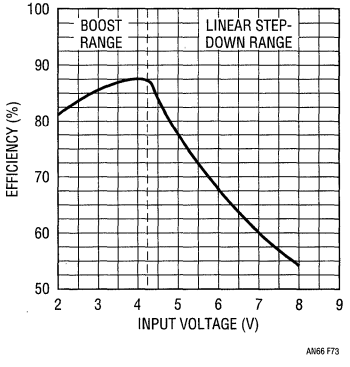


Figure 73. Efficiency vs Input Voltage for 5V/100mA Output

SENSING NEGATIVE OUTPUTS

by Dimitry Goder

Various switching regulator circuits exist to provide positive-to-negative conversion. Unfortunately, most controllers cannot sense the negative output directly; they require a positive feedback signal derived from the negative output. This creates a problem. The circuit presented in Figure 74 provides an easy solution.

The LT1172 is a versatile switching regulator that contains an onboard 100kHz PWM controller and a power switching transistor. Figure 74 shows the LTC1172 configured to provide a negative output using a popular charge pump technique. When the switch turns on, current builds up in the inductor. At the same time the charge on C3 is transferred to output capacitor C4. During the switch off-time, energy stored in the inductor charges capacitor C3. A special DC level-shifting feedback circuit consisting of Q1, Q2, and R1 to R4 senses the negative output.

Under normal conditions Q1's base is biased at a level about 0.6V above ground and the current through resistor R3 is set by the output voltage. If we assume that the base current is negligible, then R3's current also flows through R2, biasing Q2's collector at a positive voltage proportional to the negative output.

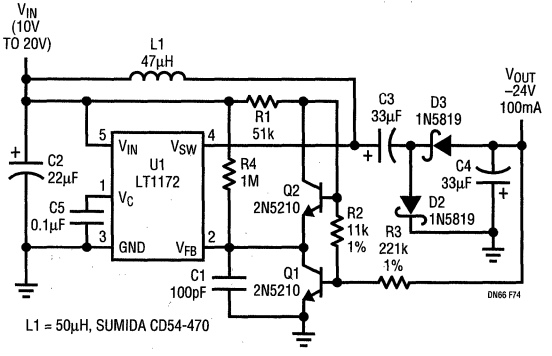


Figure 74. 10V/20V to –24 Converter

Q2 is connected as a diode and is used to compensate for Q1's base-emitter voltage change with temperature and collector current. Both transistors see the same collector current and their base-emitter voltages track quite well. Because the base-emitter voltages cancel, the voltage across R2 also appears on the LT1172's Feedback pin.

The resulting output voltage is given by the following formula:

$$V_{OUT} = V_{FB}\frac{R3}{R2} - V_{BE}$$

where V_{FB} is the LT1172 internal 1.244V reference and V_{BE} is Q1's base/emitter voltage ($\approx$ 0.6V). The V_{BE} term in the equation denotes a minor output voltage dependency on input voltage and temperature. However, the variation due to this factor is usually well below 1%.

Essentially, Q1 holds its collector voltage constant by changing its collector current and will function properly as long as some collector current exists. This puts the following limitation on R1: at minimum input voltage the current through R1 must exceed the current through R2. This is reflected by the following inequality:

$$R1 < R2\,\frac{V_{IN(MIN)} - V_{FB} - V_{BE}}{V_{FB}}$$

If the input voltage drops below the specified limit (e.g., under a slow start-up condition) and Q1 turns off, R4 provides the LT1172 Feedback pin with a positive bias and the output voltage decreases. Without R4 the Feedback pin would not get an adequate positive signal, forcing the LT1172 to provide excessive output voltage and resulting in possible circuit damage.

The feedback configuration described above is simple yet very versatile. Only resistor value changes are required for the circuit to accommodate a variety of input and output voltages. Exactly the same feedback technique can be used with flyback, "Cuk" or inverting topologies, or whenever it is necessary to sense a negative output.

Regulators—Switching (Micropower)

3-CELL TO 3.3V BUCK/BOOST CONVERTER

by Dimitry Goder

Obtaining 3.3V from three 1.2V (nominal) cells is not a straightforward task. Since battery voltage can be either below or above the output, common step-up or step-down converters are inadequate. Alternatives include using more complex switching topologies, such as SEPIC, or a switching boost regulator plus a series linear pass element. Figure 75 presents an elegant implementation of the latter approach.

The LT1303 is a Burst Mode switching regulator that contains control circuitry, an onboard power transistor and a gain block. When the input voltage is below the output, U1 starts switching and boosts the voltage across C2 and C3 to 3.3V. The gain block turns on Q1 because the feedback network R3 to R5 biases the low-battery comparator input (LBI) 20mV below the reference. In this mode the circuit operates as a conventional boost converter, sensing output voltage at the FB pin.

When the input voltage increases, it eventually reaches a point where the regulator ceases switching and the input voltage is passed unchanged to capacitor C2. The output voltage rises until the LBI input reaches the reference voltage of 1.25V, at which point Q1 starts operating as a series pass element. In these conditions the circuit functions as a linear regulator with the attending efficiency rolloff at higher input voltages.

For input voltages derived from three NiCd or NiMH cells, the circuit described provides excellent efficiency and the longest battery life. At 3.6V, where the battery spends most of its life, efficiency exceeds 91%, leaving all alternative topologies far behind.

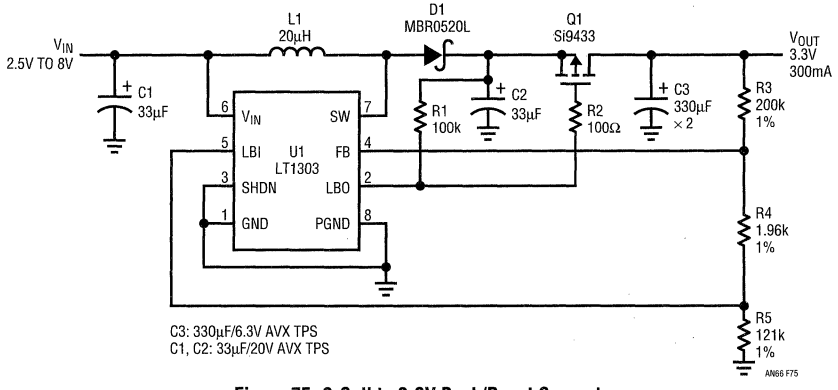


Figure 75. 3-Cell to 3.3V Buck/Boost Converter

LT1111 ISOLATED 5V SWITCHING POWER SUPPLY

by Kevin R. Hoskins

Circuit Description

Many applications require isolated power supplies. Examples include remote sensing, measurement of signals riding on high voltages, remote battery-powered equipment, elimination of ground loops and data acquisition systems where noise elimination is vital. In each situation the isolated circuitry needs a floating power source. In some cases batteries or an AC line transformer can be used for power. Alternately, the DC/DC converter shown here creates an accurately regulated, isolated output from a 5V source. Moreover, it eliminates the optoisolator feedback arrangements normally associated with fully isolated converters.

Figure 76 shows a switching power supply that generates an isolated and accurately regulated 5V at 100mA output. The circuit consists of an LT1111, configured as a flyback converter, followed by an LT1121 low dropout, micropower

linear regulator. An LTC1145 (winner of EDN's IC Innovation of the Year Award) provides micropower isolated feedback.

The LT1111 is a micropower device that operates on only 400µA (max). This micropower operation is important for energy-conscious applications. It works well with surface mount inductors such as the Coiltronics OCTA-PAC shown in the schematic. Although the LT1111's internal power switch handles up to 1A, a 100Ω resistor (R1) limits the peak switch current to approximately 650mA. This maximizes converter efficiency. One side benefit of limiting the peak switch current is that the circuit becomes insensitive to inductance. The circuit operates satisfactorily with an inductance in the range of 20µH to 50µH.

It is important that capacitor C2 have low effective series resistance (ESR) and inductance (ESL) to minimize output ripple voltage. Although aluminum capacitors are abundant and inexpensive, they will perform poorly in this switcher application because of their relatively high ESR and ESL. Two good choices that meet C2's low ESR and ESL requirements are the AVX TPS and Sanyo OS-CON™ capacitor series.

Circuit Operation

The LT1111 is configured to operate as a flyback converter. The voltage on the transformer's secondary is rectified by D2, filtered by C2 and applied to the LT1121's input. As the LT1121's input voltage continues to rise, its output will regulate at 5V. The LT1121's input voltage continues increasing until the differential between input and output equals approximately 600mV. At this point Q1 begins conducting, turning on the LTC1145 isolator. The output of the LTC1145 goes high, turning off the converter. The feedback from the LTC1145 gates the LT1111's oscillator, controlling the energy transmitted to the transformer's secondary and the LT1121's input voltage. The oscillator is gated on for longer periods as the LT1121's load current increases. Q1's gain and the feedback through the LTC1145 force the converter loop to maintain the LT1121 just above dropout, resulting in the best efficiency. The LT1121 provides current limiting as well as a tightly regulated low noise output.

OS-CON is a trademark of SANYO Electric Co., LTD.

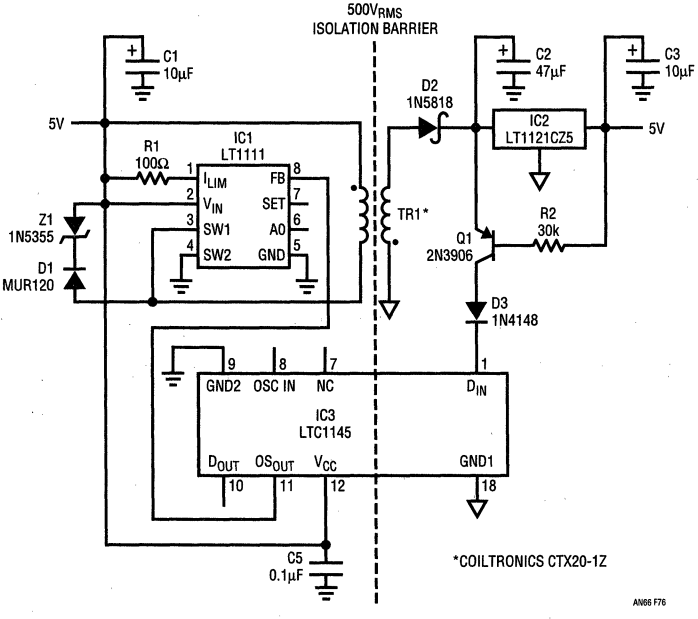


Figure 76. Circuit Generates Isolated, Regulated 5V at 100mA

LOW NOISE PORTABLE COMMUNICATIONS DC/DC CONVERTER

by Mitchell Lee

Portable communications products pack plenty of parts into close proximity. Digital clock noise must be eliminated not only from the audio sections but also from the antenna, which, by the very nature of the product, is located only inches from active circuitry. If a switching regulator is used in the power supply, it becomes another potential source of noise. The LTC1174 stepdown converter is designed specifically to eliminate noise at audio frequencies while maintaining high efficiency at low output currents.

Figure 77 shows an all surface mount solution for a 5V, 120mA output derived from five to seven NiCd or NiMH cells. Small input and output capacitors are used to conserve space without sacrificing reliability. In applications where it is desired, a shutdown feature is available; otherwise, short this pin to V_{IN}.

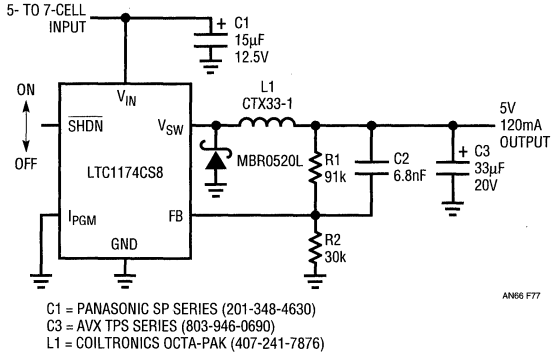


Figure 77. Low Noise, High Efficiency Step-Down Regulator for Personal Communications Devices

The LTC1174's internal switch, which is connected between V_{IN} and V_{SW}, is current controlled at a peak threshold of approximately 340mA. This low peak threshold is one of the key features that allows the LTC1174 to minimize system noise compared to other chips that carry significantly higher peak currents, easing shielding and filtering requirements and decreasing component stress.

To conserve power and maintain high efficiency at light loads, the LTC1174 uses Burst Mode operation. Unfortunately, this control scheme can also generate audio frequency noise at both light and heavy loads. In addition to electrical noise, acoustical noise can emanate from capacitors and coils under these conditions. A feedforward capacitor (C2) shifts the noise spectrum up out of the audio band, eliminating these problems. C2 also reduces peak-to-peak output ripple, which measures approximately 30mV over the entire load range.

The interactions of load current, efficiency and operating frequency are shown in Figure 78. High efficiency is maintained at even low current levels, dropping below 70% at around 800µA. No-load supply current is less than 200µA, dropping to approximately 1µA in shutdown mode. The operating frequency rises above the telephony bandwidth of 3kHz at a load of 1.2mA. Most products draw such low load currents only in standby mode with the audio circuits squelched, when noise is not an issue.

The frequency curve depicted in Figure 78 was measured with a spectrum analyzer, not a counter. This ensures that the lowest frequency noise peak is observed, rather than a faster switching frequency component. Any tendency to generate subharmonic noise is quickly exposed using this measurement method.

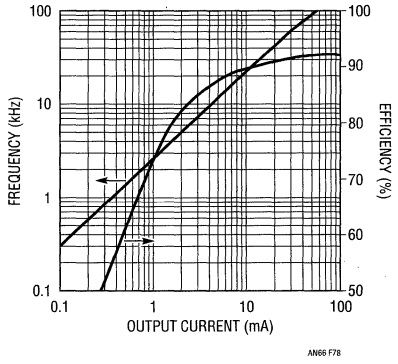


Figure 78. Parameter Interaction Chart for Figure 77's Circuit

APPLICATIONS FOR THE LT1302 MICROPOWER DC/DC CONVERTER

by Steve Pietkiewicz

2- or 3-Cell to 5V Converter

Figure 79 shows a 2- or 3-cell to 5V DC/DC converter that can deliver up to 600mA from a 2-cell input (2V minimum) or up to 900mA from a 3-cell input (2.7V minimum). R1 and R2 set the output voltage at 5V. The 200pF capacitor from FB to ground aids stability; without it the FB pin can act as an antenna and pick up dV/dt from the switch node, causing some instability in switch current levels at heavy loads. L1's inductance value is not critical; a minimum of 10µH is suggested in 2-cell applications (although this guideline is ignored in the 2-cell to 12V circuit shown later). Lower values typically have less DC resistance and can handle higher current. Transient response is better with low inductance but more output current can be had with higher values. Peak current in Burst Mode operation increases as inductance decreases, due to the finite response time of the current sensing comparator in the LT1302. The Coilcraft DO3316 series inductors have been found to be excellent in terms of performance, size and cost but their open construction results in some magnetic flux spray; try Coiltronics' OCTA-PAC series if EMI is a problem. Transient response with a load step of 25mA to 525mA is detailed in Figure 80. There is no overshoot upon load removal because switching stops entirely when output voltage rises above the comparator threshold. Undershoot at load step is less than 5%. The circuit's efficiency at various input voltages is shown in Figure 81.

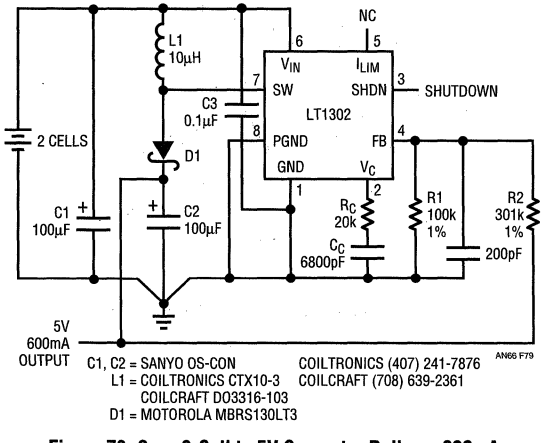


Figure 79. 2- or 3-Cell to 5V Converter Delivers 600mA, 1A From 3.3V Supply

Although efficiency graphs present useful information, a more "real world" measure of converter performance comes from battery lifetime chart recordings. Many systems require high power for a short time, for example to spin up a hard disk or transmit a packet of data. Figures 83, 84 and 85 present battery life data with a load profile of 50mA for 9 seconds and 550mA for 1 second, as detailed in Figure 82. At the chart speeds used, individual 10 second events are not discernable and the battery voltage appears as a very thick line. Figure 83 shows operating life using a 2-cell alkaline (Eveready E91) battery. Battery voltage (pen B) drops 400mV as the output load changes

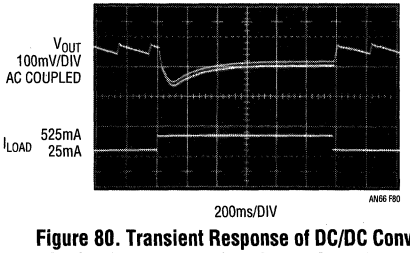


Figure 80. Transient Response of DC/DC Converter with 2.5V Input. Load Step is 25mA to 525mA

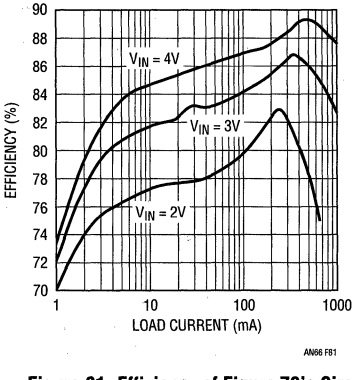


Figure 81. Efficiency of Figure 79's Circuit

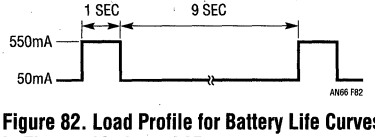


Figure 82. Load Profile for Battery Life Curves in Figures 83, 84 and 85

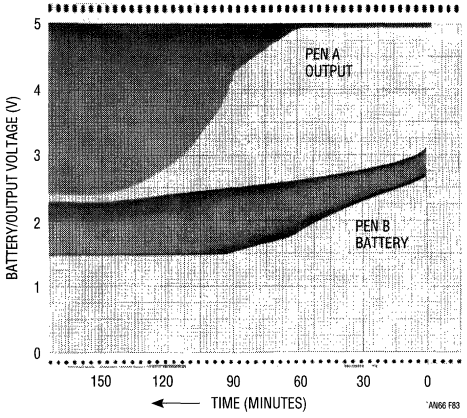


Figure 83. 2-Cell Alkaline Battery to 5V Converter with Load Profile of Figure 82 Gives 63 Minutes Operating Life. Battery Life Decreases When 550mA Load is Applied; Impedance is 330mΩ When Fresh. Output Voltage Drops at 550mA Load After 63 Minutes But Converter Can Still Deliver 50mA

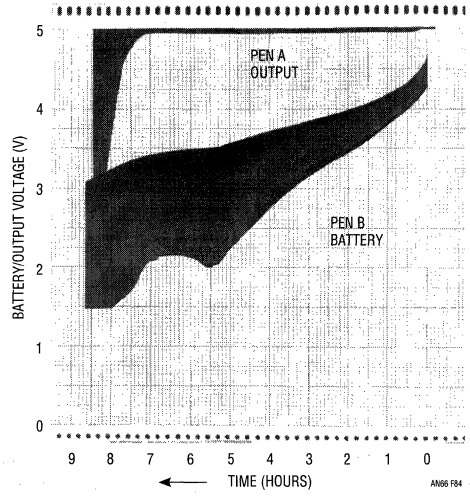


Figure 84. 3-Cell Alkaline Battery to 5V Converter with Pulsed Load Has 7.3 Hours Operating Life

from 50mA to 550mA. Battery impedance (330mΩ when fresh) can be derived from this data. After 63 minutes the battery voltage drops substantially below 2V when the output load is 550mA, causing the output voltage (pen A) to drop. The output returns to 5V when the load drops to 50mA. The LT1302's undervoltage lockout prevents the battery voltage from falling below 1.5V until the battery is completely discharged (not shown on the chart).

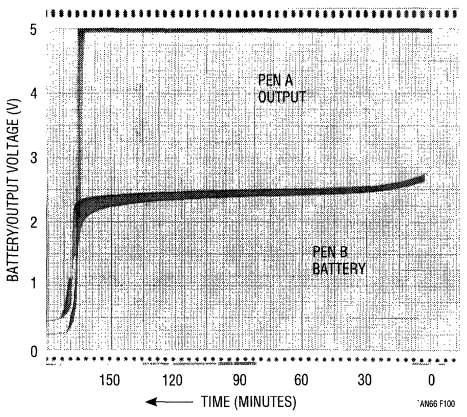


Figure 85. 2-Cell NiCd Battery to 5V Converter Shows Dramatically Lower ESR of NiCds Compared to Alkalines. Battery Impedance Is 80mΩ. Although the 600mA Hour NiCd Has 1/4 the Energy of 2.4A/Hr Alkalines with 50mA/550mA Loads NiCds Outlast Alkalines by a Factor of 2.8. Low Cell Impedance is Maintained Until the Battery Is Completely Discharged

A 3-cell alkaline battery has a significantly longer life, as shown in Figure 84. Note that the time scale here is one hour per inch. Usable life is about 7.3 hours, a sevenfold improvement over the 2-cell battery. Again, battery impedance causes the battery voltage (pen B) to drop as the load changes from 50mA to 550mA. The increasing change between the loaded and unloaded battery voltage over time is due to both increased current demand on the battery as its voltage decreases and increasing battery impedance as it is discharged.

Replacing the 2-cell alkaline with a 2-cell NiCd (AA Gates Millennium) battery results in a surprise shown in Figure 85. Although these AA NiCd cells have one-fourth the energy of AA alkaline cells, operating life is 2.8 times greater with the 50mA/550mA load profile. Dramatically lower battery impedance (80mΩ for the NiCd versus 330mΩ for the alkaline) is the cause. Battery voltage (pen B) drops just 100mV as the output load changes from 50mA to 550mA, compared to 400mV for alkalines. Additionally, impedance stays relatively constant over the life of the battery. This comparison clearly illustrates the limitations of alkaline cells in high power applications.

2-Cell to 12V Converter

Portable systems with PCMCIA interfaces often require 12V at currents of up to 120mA. Figure 86's circuit can

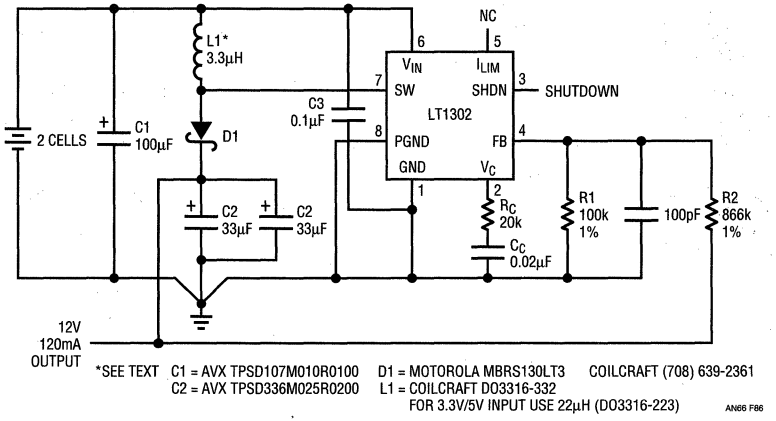


Figure 86. 2-Cell to 12V DC/DC Converter Delivers 120mA. Changing L1's Value Allows Operation from 3.3V/5V Supply

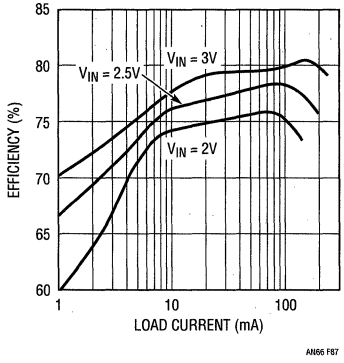


Figure 87. 2-Cell to 12V Converter Efficiency

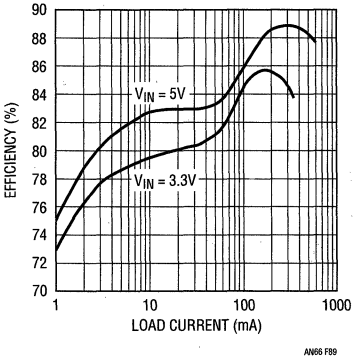


Figure 89. 3.3V/5V to 12V Converter Efficiency

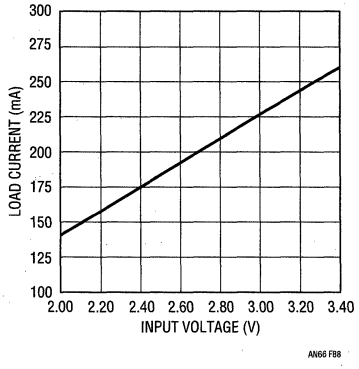


Figure 88. Maximum Load Current of 2-Cell to 12V Converter vs Input

generate 12V at over 120mA from a 2-cell battery. Operating the converter in continuous mode requires a higher duty cycle than the LT1302 provides, so a very low inductance (3.3µH) must be used in order to provide enough output current in discontinuous mode. Efficiency for this circuit is in the 70% to 80% range, as Figure 87's graph shows. Battery life at this power level would be short with a continuous load but the most common application for this voltage/current level, flash memory programming, has a rather low duty factor. Maximum output current versus input voltage is shown in Figure 88. To operate this circuit from a 3-cell battery change L1's value to 6.8µH. This will result in lower peak currents, improving efficiency substantially.

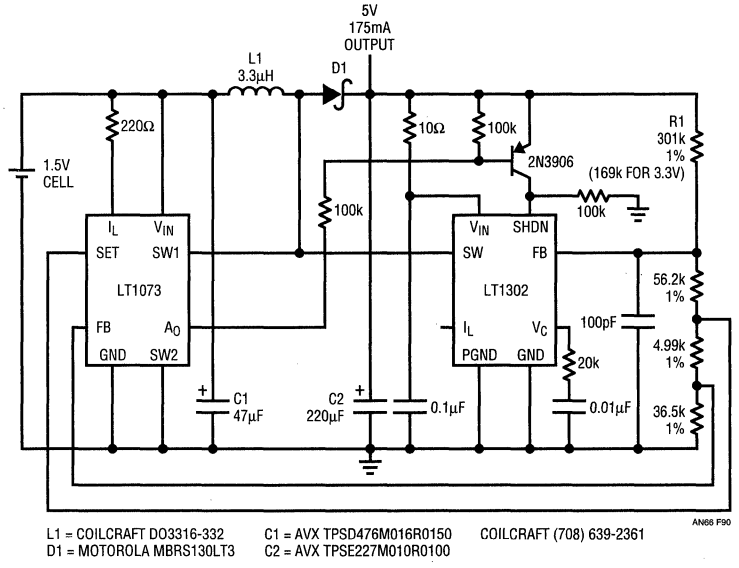


Figure 90. Single Cell to 5V Converter Delivers 150mA. Changing R1 to 169k Provides 3.3V at 250mA

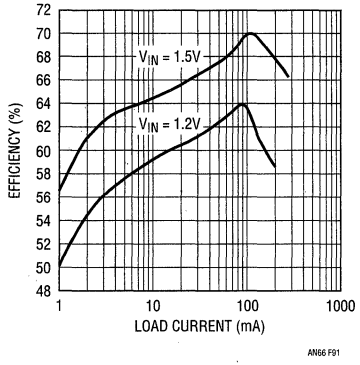


Figure 91. Single Cell to 5V Converter Efficiency

Changing L1's value to 22µH allows the circuit to operate from a 3.3V or 5V supply. Up to 350mA can be generated from 3.3V; 600mA can be delivered from a 5V input. Efficiency, pictured in Figure 89, exceeds 80% over much of the load range and peaks at 89% with a 5V input.

Single Cell to 5V/150mA Converter

Stand alone single-cell converters can typically provide no more than 40mA to 50mA at 5V from a single cell. When more power is required, the LT1302 can be used in conjunction with a single-cell device.[1] Figure 90's circuit operates from a single cell and delivers 5V at 150mA output. Although the LT1302 requires a minimum V_{IN} of 2V, single-cell operation can be achieved by powering the LT1302 from the 5V output. At start-up V_{OUT} is equal to the cell voltage minus a diode drop. The LT1073 initially puts the LT1302 in its shutdown state. The LT1073 switches L1, causing L1's current to alternately build up and dump into C2. When V_{OUT} reaches approximately 2V the LT1073's Set pin goes above 212mV causing A_0 to go low. This pulls the LT1302's SHDN pin low, enabling it. The output, now booted by the much higher power LT1302, quickly reaches 2.4V. When the LT1073's FB pin reaches 212mV its switching action stops. The brief period when the LT1073 and LT1302 are switching simultaneously has no detrimental effect. When the output reaches 5V the LT1073 has ceased switching. Circuit efficiency is in the 60 to 70% range as shown in Figure 91.

3-Cell to 3.3V/12V Buck/Boost Converter

Obtaining 3.3V from three cells is not a straightforward task; a fresh battery measures over 4.5V and a fully depleted one 2.7V. Since battery voltage can be both

[1] Williams, Jim. "200mA Output, 1.5 to 5V Converter." *Linear Technology* III:1 (February, 1993) p. 17.

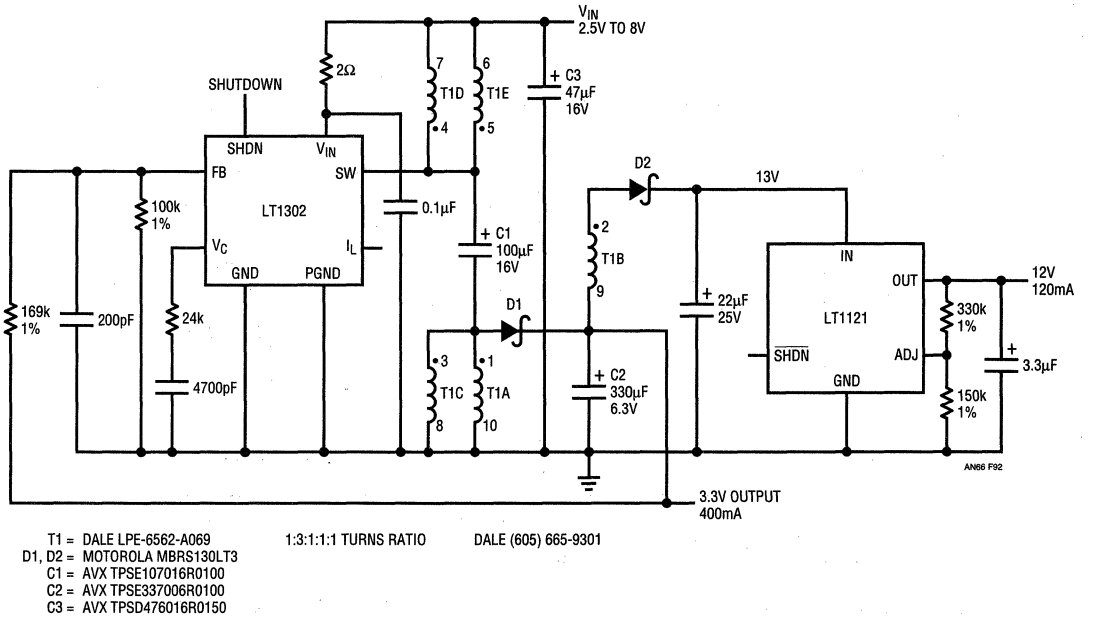


Figure 92. 3-Cell to 3.3V Buck/Boost Converter with Auxiliary 12V Regulated Output

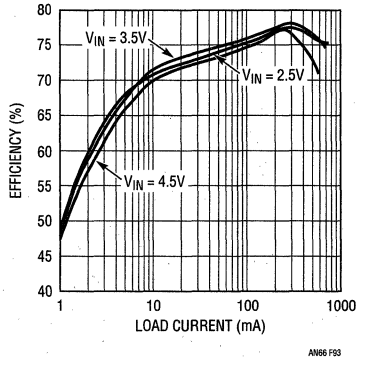


Figure 93. 3.3V Buck/Boost Converter Efficiency

above and below the output, common step-up (boost) or step-down (buck) converters are inadequate. Figure 92's circuit provides an efficient solution to the problem using just one magnetics component and also provides an auxiliary 12V output. When the LT1302's switch is on its SW pin goes low, causing current buildup in T1D and T1E (windings are paralleled to achieve lower DC resistance). D1's anode goes to $-V_{IN}$ because of the phasing of T1C/T1A relative to T1D/T1E. C1 is charged to V_{IN}. When the switch opens, SW flies high to a voltage of $V_{IN} + V_{OUT} + V_{DIODE}$. Energy is transferred to the output by magnetic coupling from T1D/T1E to T1C/T1A and by current flowing through C1. During this flyback phase, T1A/T1C has 3.3V plus a diode drop across the windings. T1B, which has a 3:1 turns ratio, has approximately 10V to 11V impressed upon it. T1B "stands" on the 3.3V output, resulting in about 13V to14V at the input of the LT1121 linear regulator, which then precisely regulates the 12V output. Since this output is not directly regulated by the LT1302, it cannot be loaded without having at least a small load on the directly regulated 3.3V output. The LT1121 can be turned off by pulling its SHDN pin low, isolating the load from the output. Figure 93 shows the circuit's efficiency for various input voltages.

Construction Hints

The high speed, high current switching associated with the LT1302 mandates careful attention to layout. Follow the suggested component placement in Figure 94 for proper operation. High current functions are separated by the package from sensitive control functions. Feedback

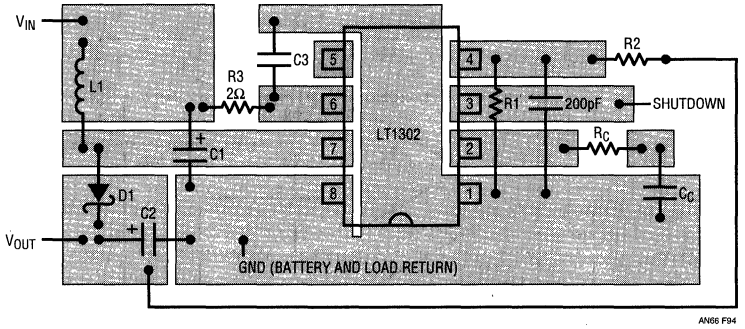


Figure 94. Suggested Component Placement for LT1302

resistors R1 and R2 should be close to the Feedback pin (Pin 4). Noise can easily be coupled into this pin if care is not taken. If the LT1302 is operated off a 3-cell or higher input, R3 (2Ω) in series with V_{IN} is recommended. This isolates the device from noise spikes on the input voltage. Do not install R3 if the device must operate from a 2V input, as input current will cause the LT1302's input voltage to go below 2V. The 0.1µF ceramic bypass capacitor C3 (use X7R not Z5U) should be mounted as close as possible to the package. Grounding should be segregated as illustrated. C3's ground trace should not carry switch current. Run a separate ground trace up under the package as shown. The battery and load return should go to the power side of the ground copper. Adherence to these rules will result in working converters with optimum performance.

CLOCK-SYNCHRONIZED SWITCHING REGULATOR HAS COHERENT NOISE

by Jim Williams, Sean Gold and Steve Pietkiewicz

Gated oscillator type switching regulators permit high efficiency over extended ranges of output current. These regulators achieve this desirable characteristic by using a gated oscillator architecture instead of a clocked pulse-width modulator. This eliminates the "housekeeping" currents associated with the continuous operation of fixed-frequency designs. Gated oscillator regulators simply self-clock at whatever frequency is required to maintain the output voltage. Typically, loop oscillation frequency ranges from a few Hertz into the kiloHertz region depending upon the load.

This asynchronous variable frequency operation seldom creates problems; some systems, however, are sensitive to this characteristic. The circuit in Figure 95 slightly modifies a gated-oscillator-type switching regulator by synchronizing its loop oscillation frequency to the system's clock. In this fashion the oscillation frequency and its attendant switching noise, although variable, are made coherent with system operation.

Circuit operation is best understood by temporarily ignoring the flip-flop and assuming that the LT1107 regulator's A_{OUT} and FB pins are connected. When the output voltage decays, the Set pin drops below V_{REF}, causing A_{OUT} to fall. This causes the internal comparator to switch high, biasing the oscillator and output transistor into conduction. L1 receives pulsed drive and its flyback events are deposited into the 100µF capacitor via the diode, restoring output voltage. This overdrives the Set pin, causing the IC to switch OFF until another cycle is required.

The frequency of this oscillatory cycle is load dependent and variable. If a flip-flop is interposed in the A_{OUT}/FB pin path as shown, the frequency is synchronized to the system clock. When the output decays far enough (trace A, Figure 96) the A_{OUT} pin (trace B) goes low. At the next clock pulse (trace C) the flip-flop Q2 output (trace D) sets low, biasing the comparator-oscillator. This turns on the power switch (V_{SW} pin is trace E), which pulses L1. L1

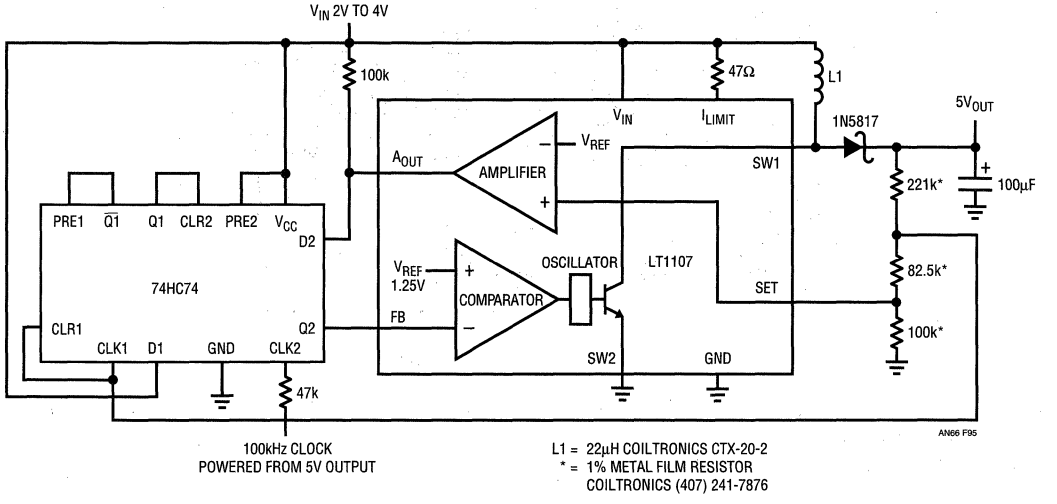


Figure 95. A Synchronizing Flip-Flop Forces Switching Regulator Noise To Be Coherent with the Clock

responds in flyback fashion, depositing its energy into the output capacitor to maintain output voltage. This operation is similar to the previously described case except that the sequence is forced to synchronize with the system clock by the flip-flop's action. Although the resulting loop's oscillation frequency is variable, it and all its attendant switching noise are synchronous and coherent with the system clock.

Because of its sampled nature, this clocked loop may not start. To ensure start-up, the flip-flop's remaining section is connected as a buffer. The CLR1/CLK1 line monitors output voltage via the resistor string. If the circuit does not start, Q1 goes high, CLR2 sets and loop operation commences. Although the circuit shown is a step-up type, any switching regulator configuration can use this technique.

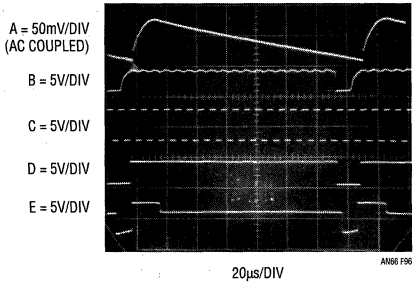


Figure 96. Waveforms for the Clock Synchronized Switching Regulator. The Regulator Switches (Trace E) Only on Clock Transitions (Trace C) Resulting in Clock Coherent Output Noise (Trace A)

BATTERY-POWERED CIRCUITS USING THE LT1300 AND LT1301

by Steve Pietkiewicz

5V from 2 Cells

Figure 97's circuit provides 5V from a 2-cell input. Shutdown is effected by taking the Shutdown pin high. V_{IN} current drops to 10µA in this condition. This simple boost topology does not provide output isolation, and in shutdown the load is still connected to the battery via L1 and D1. Figure 98 shows the efficiency of the circuit with a range of input voltages, including a fresh battery (3V) and an "almost-dead" battery (2V). At load currents below a few milliamperes, the 120µA quiescent current of the device becomes significant, causing the fall off in efficiency detailed in the figure. At load currents in the 20mA to 200mA range, efficiency flattens out in the 80% to 88% range, depending on the input. Figure 99 details circuit operation. V_{OUT} is shown in trace A. The burst repetition

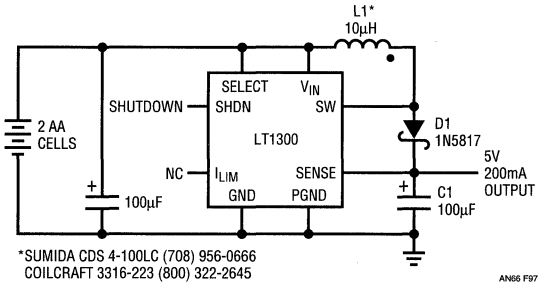


Figure 97. 2-Cell to 5V DC/DC Converter Delivers >200mA with a 2V Input

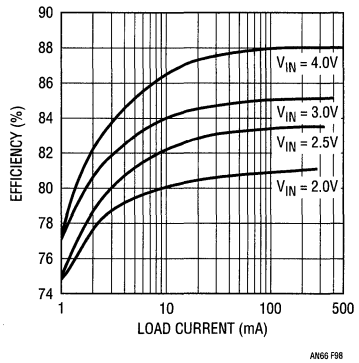


Figure 98. Efficiency of Figure 112's Circuit

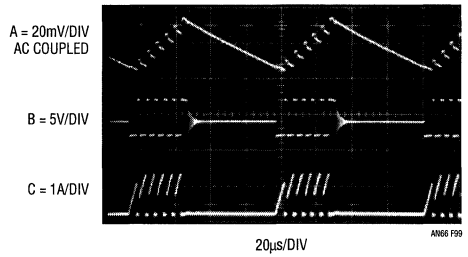


Figure 99. Burst Mode Operation In Action

pattern is clearly shown as V_{OUT} decays, then steps back up due to switching action. Trace B shows the voltage at the switch node. The damped high frequency waveform at the end of each burst is due to the inductor "ringing off," forming an LC tank with the switch and diode capacitance. It is not harmful and contains far less energy than the high speed edge that occurs when the switch turns off. Switch current is shown in trace C. The current comparator inside the LT1300 controls peak switch current, turning off the switch when the current reaches approximately 1A.

Although efficiency curves present useful information, a more important measure of battery-powered DC/DC converter performance is operating life. Figures 100 and 101 detail battery life tests with Figure 97's circuit at load currents of 100mA and 200mA, respectively. Operating-life curves are shown using both Eveready E91 alkaline cells and new L91 "Hi-Energy" lithium cells. These lithium cells, new to the market, are specifically designed for high drain applications. The performance advantage of lithium is about 2:1 at 100mA load current (Figure 100), increasing to 2.5:1 at 200mA load (Figure 101). Alkaline cells perform poorly at high drain rates because their internal impedance ranges from 0.2Ω to 0.5Ω, causing a large voltage drop within the cell. The alkaline cells feel quite warm at 200mA load current, the result of I^2R losses inside the cells.

The reduced power circuit shown in Figure 102 can generate 5V at currents up to 50mA. Here the I_{LIM} pin is grounded, reducing peak switch current to 400mA. Lower profile components can be used in this circuit. The capacitors are C-case size solid tantalum and inductor L1 is the tallest component at 3.2mm. The reduced peak current also extends battery life, since the I^2R loss due to internal battery impedance is reduced. Figure 103 details efficiency versus load current for several input voltages and

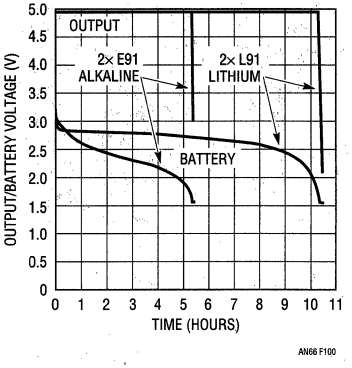


Figure 100. Two Eveready L91 Lithium AA Cells Provide Approximately Twice the Life of E91 Alkaline Cells at a 100mA Load Current

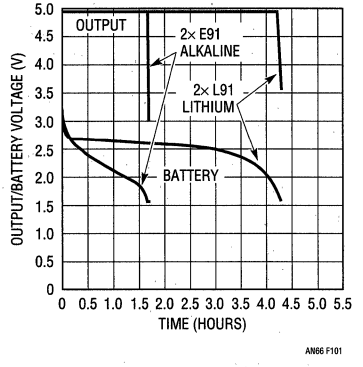


Figure 101. Doubling Load Current to 200mA Causes E91 Alkaline Battery Life to Drop by 2/3; L91 Lithium Battery Shows 2.5:1 Difference in Operating Life

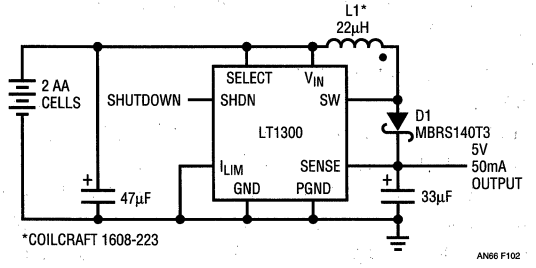


Figure 102. Lower Power Applications Can Use Smaller Components. L1 Is Tallest Component at 3.1mm

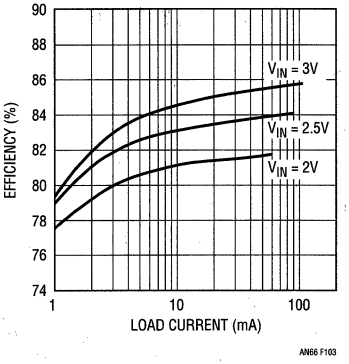


Figure 103. Efficiency of Figure 102's Circuit

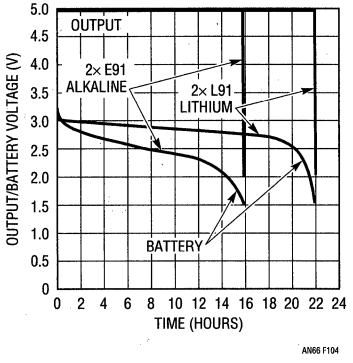


Figure 104. 50mA Load and Reduced Switch Current Are Kind to E91 AA Alkaline Battery; the Advantages of L91 Lithium Are Not as Evident

Figure 104 shows battery life at a 50mA load. Note that the L91 lithium battery lasts only about 40% longer than the alkaline. The higher cost of the lithium cells makes the alkaline cells more cost effective in this application. A pair of Eveready AAA alkaline cells (type E92) lasts 96.6 hours with 5mA load, very close to the rated capacity of the battery.

A 4-Cell Application

A 4-cell pack is a convenient, popular battery size. Alkaline cells are sold in 4-packs at retail stores and 4 cells usually provide sufficient energy to keep battery replacement frequency reasonable. Generating 5V from 4 cells, however, is a bit tricky. A fresh 4-cell pack has a terminal voltage of 6.4V, but at the end of its life the pack's terminal voltage is around 3.2V; hence, the DC/DC converter must

step the voltage either up or down depending on the state of the batteries. A flyback topology with a costly custom designed transformer could be employed but Figure 105's circuit gets around these problems by using a flying capacitor scheme along with a second inductor. The circuit also isolates the input from the output, allowing the output to go to 0V during shutdown. The circuit can be divided conceptually into boost and buck sections. L1 and the LT1300 switch comprise the boost or step-up section and L2, D1 and C3 comprise the buck or step-down section. C2 is charged to V_{IN} and acts as a level shift between the two sections. The switch node toggles between ground and $V_{IN} + V_{OUT}$, and the L2/C2 diode node toggles between $-V_{IN}$ and $V_{OUT} + V_D$. Figure 106 shows efficiency versus load current for the circuit. All four energy storage elements must handle power, which accounts for the lower efficiency of this circuit compared to the simpler boost circuit in Figure 97. Efficiency is directly related to the ESR and DCR of the capacitors and inductors used. Better capacitors cost more money. Better inductors do not necessarily cost more but they do take up more space. Worst-case RMS current through C2 occurs at minimum input voltage and measures 0.4A at full load with a 3V input. C2's specified maximum RMS current must be greater than this worst-case current. The Sanyo capacitors noted specify a maximum ESR of 0.045Ω with a maximum ripple current rating of 2.1A. The Gowanda inductors specify a maximum DCR of 0.058Ω.

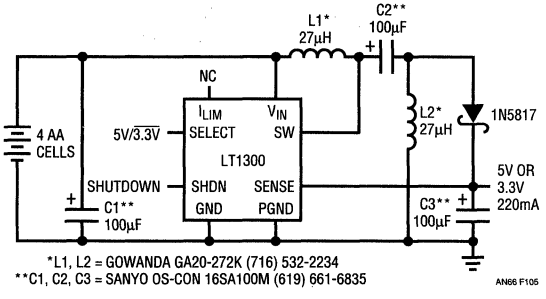


Figure 105. 4-Cell to 3.3V or 5V Converter Output Goes to Zero When in Shutdown. Inductors May Have, but Do Not Require Coupling; a Transformer or Two Separate Units Can Be Used

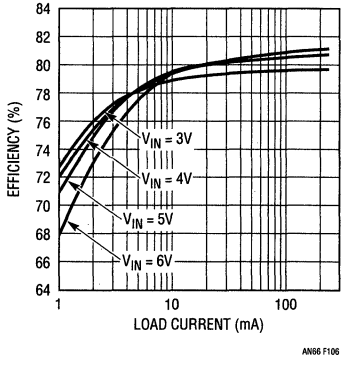


Figure 106. Efficiency of Up/Down Converter in Figure 105

LT1301 Outputs: 5V or 12V

The LT1301 is identical to the LT1300 in every way except output voltage. The LT1301 can be set to a 5V or 12V output via its Select pin. Figure 107 shows a simple 3.3V or 5V to 12V step-up converter. It can generate 120mA at 12V from either 3.3V or 5V inputs, enabling the circuit to provide VPP on a PCMCIA card socket. Figure 108 shows the circuit's efficiency. Switch voltage drop is a smaller percentage of input voltage at 5V than at 3.3V, resulting in the higher efficiency at 5V input.

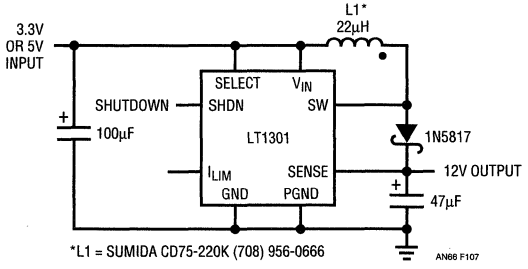


Figure 107. LT1301 Delivers 12V from 3.3V or 5V Input

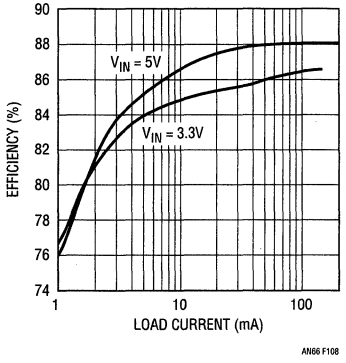


Figure 108. Efficiency of Figure 122's Circuit

BATTERY-POWERED CIRCUITS USING THE LT1304 MICROPOWER DC/DC CONVERTER WITH LOW-BATTERY DETECTOR

by Steve Pietkiewicz

A 2-Cell to 5V Converter

A compact 2-cell to 5V converter can be constructed using the circuit in Figure 109. Using the LT1304-5 fixed output device eliminates the need for external voltage setting resistors, lowering component count. As the battery voltage drops, the circuit continues to function until the LT1304's undervoltage lockout disables the part at approximately V_{IN} = 1.5V. 200mA is available at a battery voltage of 2.0V. As the battery voltage decreases below 2V, cell impedance starts to quickly increase. End-of-life is usually assumed to be around 1.8V, or 0.9V per cell.

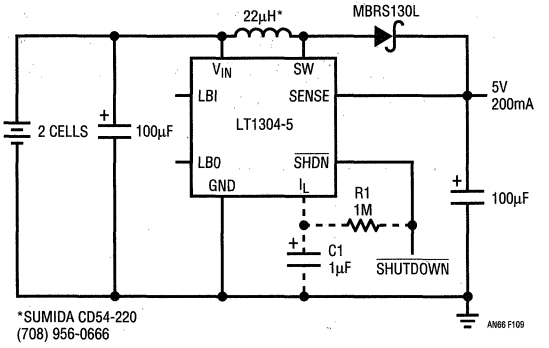


Figure 109. 2-Cell to 5V/200mA Boost Converter Takes Four External Parts. Components with Dashed Lines Are for Soft Start (Optional)

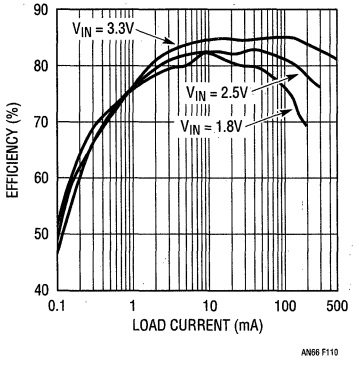


Figure 110. 2-Cell to 5V Converter Efficiency

Efficiency is detailed in Figure 110. Micropower Burst Mode operation keeps efficiency above 70%, even for load current below 1mA. Efficiency reaches 85% for a 3.3V input. Load transient response is illustrated in Figure 111. Since the LT1304 uses a hysteretic comparator in place of the traditional linear feedback loop, the circuit responds immediately to changes in load current. Figure 112 details start-up behavior without soft start circuitry (R1 and C1 in Figure 109). Input current rises to 1A as the device is turned on, which can cause the input supply voltage to sag, possibly tripping the low-battery detector. Output voltage reaches 5V in approximately 1ms. The addition of R1 and C1 to Figure 109's circuit limits inrush current at start-up, providing for a smoother turn-on as indicated in Figure 113.

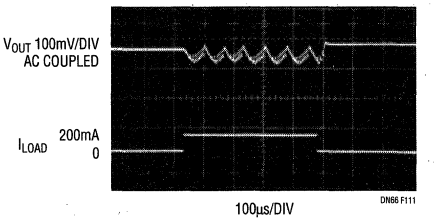


Figure 111. Boost Converter Load Transient Response with V_{IN} = 2.2V

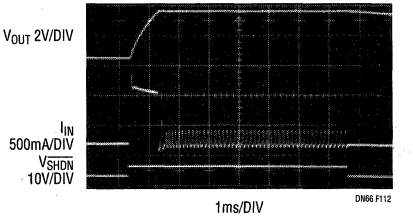


Figure 112. Start-Up Response. Input Current Rises Quickly to 1A. V_{OUT} Reaches 5V in Approximately 1ms. Output Drives 20mA Load

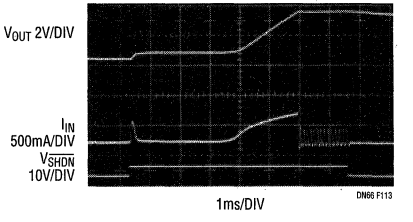


Figure 113. Start-Up Response with 1µF/1MΩ Components in Figure 109 added. Input Current Is More Controlled. V_{OUT} Reaches 5V in 6ms. Output Drives 20mA Load

A 4-Cell to 5V Converter

A 4-cell to 5V converter is more complex than a simple boost converter because the input voltage can be either above or below the output voltage. The single-ended primary inductance converter (SEPIC) shown in Figure 114 accomplishes this task with the additional benefit of output isolation. In shutdown conditions, the converter's output will go to zero, unlike the simple boost converter, where a DC path from input to output through the inductor and diode remains. In this circuit, peak current is limited to approximately 500mA by the addition of 22k resistor R1. This allows very small low profile components to be used. The 100µF capacitors are D-case size with a height of 2.9mm and the inductors are 3.2mm high. The circuit can deliver 5V at up to 100mA. Efficiency is relatively flat across the 1mA to 100mA load range.

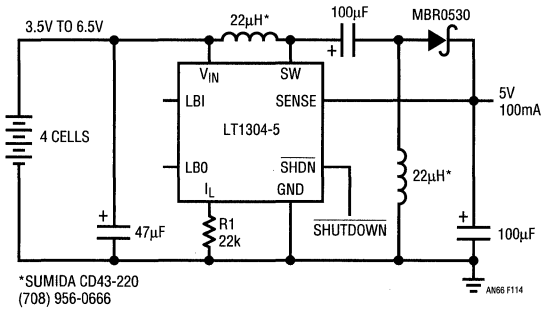


Figure 114. 4-Cell to 5V Step-Up/Step-Down Converter, Also Known as SEPIC (Single-Ended Primary Inductance Converter). Low Profile Components Are Used Throughout

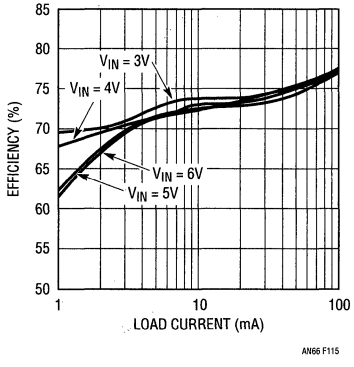


Figure 115. Efficiency Plot of SEPIC Converter Shown in Figure 114

Super Burst™ Mode Operation: 5V/100mA DC/DC with 15µA Quiescent Current

The LT1304's low-battery detector can be used to control the DC/DC converter. The result is a reduction in quiescent current by almost an order of magnitude. Figure 116 details this Super Burst circuit. V_{OUT} is monitored by the LT1304's LBI pin via resistor divider R1/R2. When LBI is above 1.2V LBO is high, forcing the LT1304 into shutdown mode and reducing current drain from the battery to 10µA. When V_{OUT} decreases enough to overcome the low-battery detector's hysteresis (about 35mV) LBO goes low. Q1 turns on, pulling $\overline{SHDN}$ high and turning on the rest of the IC. R3 limits peak current to 500mA; it can be removed for higher output power. Efficiency is illustrated in Figure

Super Burst is a trademark of Linear Technology Corporation.

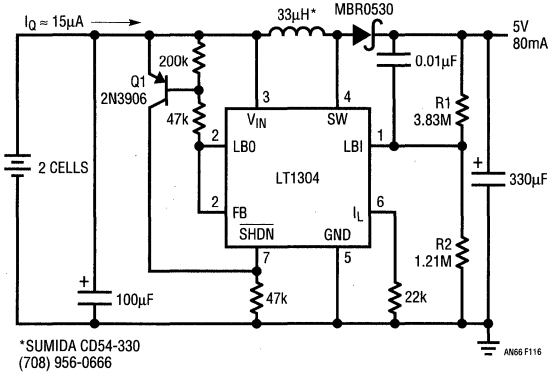


Figure 116. Super Burst Mode Operation 2-Cell to 5V DC/DC Converter Draws Only 15µA Unloaded. 2 AA Alkaline Cells Will Last for Years

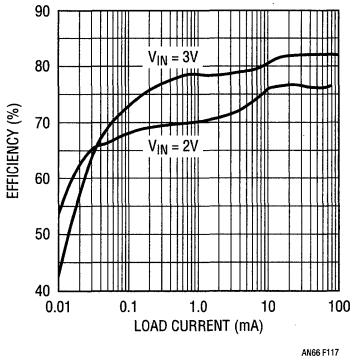


Figure 117. Super Burst Mode Operation DC/DC Converter Efficiency

117. The converter is approximately 70% efficient at a 100µA load, 20 points higher than the circuit of Figure 109. Even at a 10µA load, efficiency is in the 40% to 50% range, equivalent to 100µW to 120µW total power drain from the battery. In contrast, Figure 109's circuit consumes approximately 300µW to 400µW unloaded.

An output capacitor charging cycle or "burst" is shown in Figure 118, with the circuit driving a 50mA load. The slow response of the low-battery detector results in the high number of individual switch cycles or "hits" within the burst.

Figure 119 depicts output voltage at the modest load of 100µA. The burst repetition rate is around 4Hz. With the load removed, the repetition rate drops to approximately 0.2Hz or one burst every 5 seconds. Systems that spend a high percentage of operating time in sleep mode can benefit from the greatly reduced quiescent power drain of Figure 116's circuit.

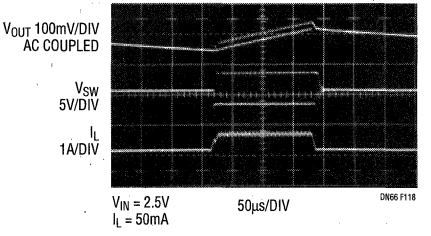


Figure 118. Super Burst Mode Operation in Action

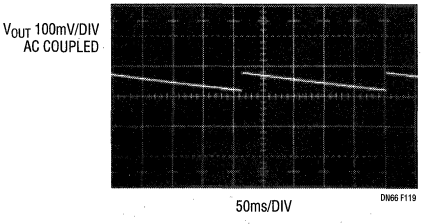


Figure 119. Super Burst Mode Operation Circuit with 100µA Load, Burst Occurs Approximately Once Every 240ms

Layout

The LT1304 switch turns on and off very quickly. For best performance we suggest the component placement in Figure 120. Improper layouts will result in poor load regulation, especially at heavy loads. Parasitic lead inductance must be kept low for proper operation. Switch turn-off is detailed in Figure 121[1]. A close look at the rise time (5ns) will confirm the need for good PC board layout. The 200MHz ringing of the switch voltage is attributable to lead inductance, switch and diode capacitance, and diode turn-on time. Switch turn-on is shown in Figure 122. Transition time is similar to that of Figure 121. Adherence to the layout suggestions will result in working DC/DC converters with a minimum of trouble.

[1]Instrumentation for oscillographs of Figures 121 and 122 include Tektronix P6032 active probe, Type 1S1 sampling unit and type 547 mainframe.

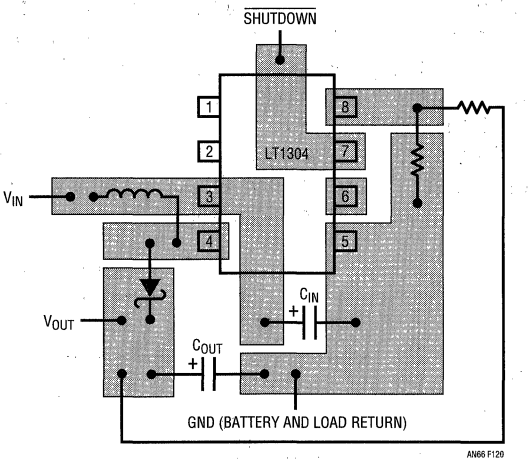


Figure 120. Suggested Layout for Best Performance. Input Capacitor Placement as Shown Is Highly Recommended. Switch Trace (Pin 4) Copper Area is Minimized

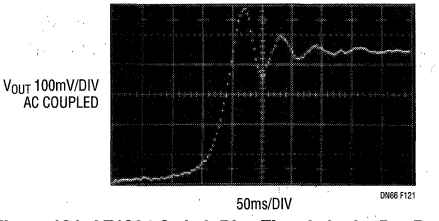


Figure 121. LT1304 Switch Rise Time Is in the 5ns Range. These Types of Edges Emphasize the Need for Proper PC Board Layout

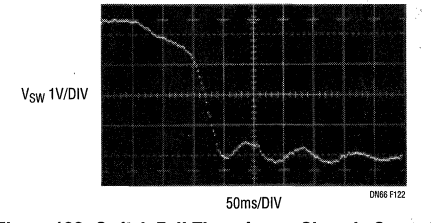


Figure 122. Switch Fall Time. Lower Slope in Second and Third Graticules Shows Effect of Lead and Bond Wire Inductance

AUTOMATIC LOAD SENSING SAVES POWER IN HIGH VOLTAGE CONVERTER

by Mitchell Lee

There are a surprising number of high output voltage applications for LTC's micropower DC/DC converter family. These applications include electroluminescent panels, specialized sensing tubes and xenon strobes. One of the key features of the micropower converters is low quiescent current. Since the quiescent current is far less than the self-discharge rate of common alkaline cells, the traditional ON/OFF switch can be eliminated in cases where the load is intermittent or where the load is shut down under digital control.

The maximum switch voltage for many micropower devices is 50V. For higher outputs the circuit shown in Figure 123 is often recommended. It combines a boost regulator and a charge pump tripler to produce an output voltage of up to 150V. The output is sensed through a divider network, which consumes a constant current of about 12μA. This doesn't seem like much, but reflected back to the 3V battery it amounts to over 3mA. Together with the LT1107's 320μA quiescent current the battery current is 3.5mA under no load. In standby applications this is unacceptably high, even for two D cells.

A circuit consisting of transistors Q1 and Q2 was added to reduce the standby current to an acceptable level. When a load of more than 50μA is present, Q1 turns on, Q2 turns off and the 9.1M resistor (R4) serves as a feedback path. R2, R3 and R4 regulate the output at 128V.

If the load current drops below 50μA, Q1 turns off and Q2 turns on, shorting out R4. With R4 out of the way, R2 and R3 regulate the output to approximately 15V. The measured input current under this condition is only 350μA, just slightly higher than the chip's no-load quiescent current. When the load returns, Q1 senses the excess current and the output automatically rises to its nominal value of 128V.

This automatic feedback switching scheme improves the battery current by a factor of ten and eliminates the need for a mechanical ON/OFF switch in applications where the load is under digital control.

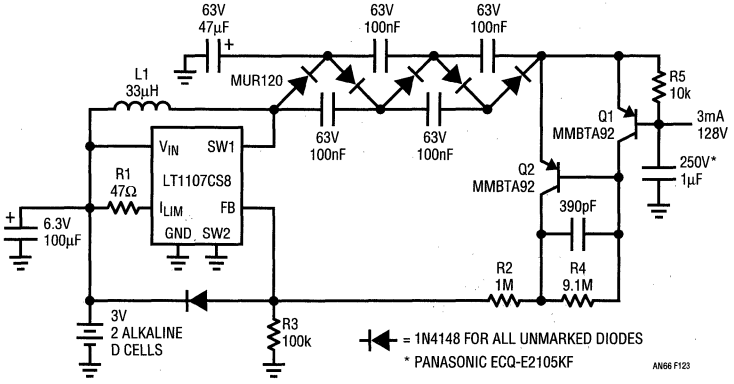


Figure 123. Automatic Shutdown Reduces Battery Current to 350μA

Regulators—Switching (Micropower)

Backlight

HIGH EFFICIENCY EL DRIVER CIRCUIT

by Dave Bell

Electroluminescent (EL) lamps are gaining popularity as sources of LCD backlight illumination, especially in small, handheld products. Compared with other backlighting technologies, EL is attractive because the lamp is thin, lightweight, rugged and can be illuminated with little power.

EL lamps are capacitive in nature, typically exhibiting around 3000pF/in^2, and require a low frequency (50Hz to 1kHz) 120V_{RMS} AC drive voltage. Heretofore, this has usually been generated by a low frequency blocking oscillator using a large transformer.

Figure 124 depicts a high efficiency EL driver that can drive a relatively large (12 in^2) EL lamp using a small high frequency transformer. The circuit is self-oscillating and delivers a regulated triangle wave to the attached lamp. Very high conversion efficiency may be obtained using this circuit, even matching state-of-the-art CCFL backlights at modest brightness levels (10 to 20 foot-lamberts).

Since an EL lamp is basically a lossy capacitor, the majority of the energy delivered to the lamp during the charge half-cycle is stored as electrostatic energy ($1/2CV^2$). Overall conversion efficiency can be improved by almost 2:1 if this stored energy is returned to the battery during the discharge half-cycle. The circuit of Figure 124 operates as a flyback converter during the charge half-cycle, taking energy from the battery and charging the EL capacitance. During the discharge half-cycle the flyback converter operates in the reverse direction, taking energy back out of the EL lamp and returning it to the battery. Nearly 50% of the energy taken during the charge half-cycle is returned during the discharge half-cycle; hence the 2:1 efficiency improvement.

During the charge half-cycle, the LT1303 operates as a flyback converter at approximately 150kHz, ramping the current in T1's 10µH primary inductance to approximately 1A on each switching pulse. When the LT1303's internal power switch turns off, the flyback energy stored in T1 is delivered to the EL lamp through D3 and C5. Successive high frequency flyback cycles progressively charge the EL capacitance until 300V is reached on the "+" side of C5. At this point the feedback voltage present at the LT1303's LBI input reaches 1.25V, causing the internal comparator to change state.

When the LT1303's internal comparator changes state, the open-collector driver at the LBO output is released. This places the circuit into discharge mode and reverses the operation of the flyback energy transfer. Q3 turns on and removes the gate drive from Q2A, thereby disabling switching action on the primary of T1. Flip-flop U2A is also clocked, resulting in a high level on the $\overline{Q}$ output; this positive feedback action keeps LBI above 1.25V. Even though Q2A is turned off the LT1303's SW pin still switches into pull-up resistor R4. The resulting pulses at the SW pin are used to clock U2B and to drive a "poor man's" current mode flyback converter on the secondary of T1.

Every clock pulse to flip-flop U2B turns on Q2B and draws current from the EL lamp through C5, T1, D2 and Q4. (Q4 must be a 600V rated MOSFET to withstand the high peak voltages present on its drain during normal operation.) Current ramps up through T1's 2.25mH secondary inductance until the voltage across current sense resistor R12 reaches approximately 0.6V. At this point Q5 turns on, providing a direct clear to U2B and thereby terminating the pulse. Energy taken from the EL lamp and stored in T1's inductance is then transferred back to the battery through D1 and T1's primary winding. This cycle repeats at approximately 150kHz until the voltage on C5 ratchets down to approximately 0V. Once C5 is fully discharged, the preset input on U2A will be pulled low, forcing the voltage on the LT1303's LBI input to ground and initiating another charge half-cycle.

This circuit produces a triangle voltage waveform with a constant peak-to-peak voltage of 300V, but the frequency of the triangle wave depends on the capacitance of the attached EL lamp. A 12 in^2 lamp has approximately 36nF of capacitance, which results in a triangle wave frequency of approximately 400Hz. This produces approximately 17FL of light output from a state-of-the-art EL lamp. Because of the "constant power" nature of the charging

flyback converter, light output remains relatively constant with changes in the battery voltage. In addition, since EL lamp capacitance decreases with age, the circuit tends to minimize brightness reduction with lamp aging. C5, R9, and R10 maintain a zero average voltage across the EL lamp terminals—an essential factor for reliable lamp operation.

Two options exist for EL lamps with different characteristics. Larger lamps can be supported by specifying an LT1305 instead of the LT1303 shown in Figure 124. The LT1305 will terminate switch cycles at 2A instead of 1A, thereby delivering four times as much energy (energy stored in T1 is defined by $1/2LI^2$). The value of R12 must also be reduced to 7.5Ω to increase the discharge flyback current by the same ratio. For smaller lamps or for brightness adjustment, the circuit may be "throttled" by connecting the LT1303/LT1305's FB pin to a small current-sense resistor in the lower leg of the EL lamp.

Not only does the depicted circuit operate very efficiently, it takes output fault conditions in stride. The circuit, with C5 rated at 300V, tolerates indefinite short-circuit and open-circuit conditions across its EL lamp output pins.

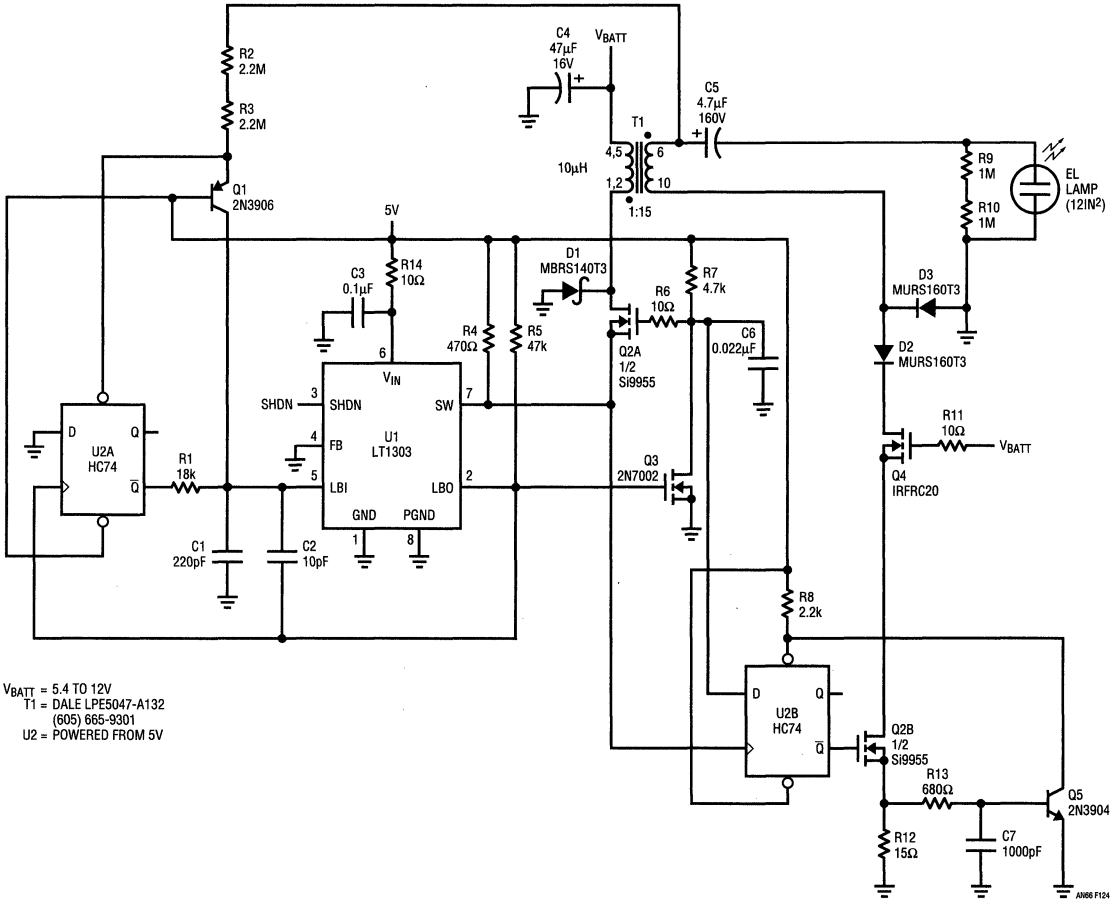


Figure 124. High Efficiency EL Driver Circuit

A LOW POWER, LOW VOLTAGE CCFL POWER SUPPLY

by Steve Pietkiewicz

Most recently published CCFL driver circuits require an input supply of 7V to 20V and are optimized for bulb currents of 5mA or more. This precludes lower power operation from 2- or 3-cell batteries often used in PDAs, palmtop computers and the like. A CCFL power supply that operates from 2V to 6V is shown in Figure 125. This circuit can drive a small (75mm) CCFL over a 100µA to 2mA range.

The circuit uses an LT1301 micropower DC/DC converter IC in conjunction with a current driven Royer class converter comprising T1, Q1 and Q2. When power is applied along with intensity adjust voltage V_A, the LT1301's I_{LIM} pin is driven slightly positive, causing maximum switching current to flow through the IC's internal Switch pin (SW). L1 conducts current, which flows from T1's center tap, through the transistors, into L1. L1's current is deposited in switched fashion to ground by the regulator's action.

The Royer converter oscillates at a frequency set primarily by T1's characteristics (including its load) and the 0.068µF capacitor. L1 sets the magnitude of the Q1-to-Q2 tail current, and hence, T1's drive level. The 1N5817 diode maintains L1's current flow when the LT1301's switch is off. The 0.068µF capacitor combines with L1's characteristics to produce sine wave voltage drive at the Q1 and Q2 collectors. T1 furnishes voltage step-up and about 1400V_{P-P} appears at its secondary. Alternating current flows through the 22pF capacitor into the lamp. On positive half cycles the lamp's current is steered to ground via D1. On negative half cycles the lamp's current flows through Q3's collector and is filtered by C1. The LT1301's I_{LIM} pin acts as a zero summing point with about 25µA bias current flowing out of the pin into C1. The LT1301 regulates L1's current to maintain equality of Q3's average collector current, representing one-half the lamp current, and R1's current, represented by V_A/R1. When V_A is set to zero the I_{LIM} pin's bias current forces about 100µA bulb current.

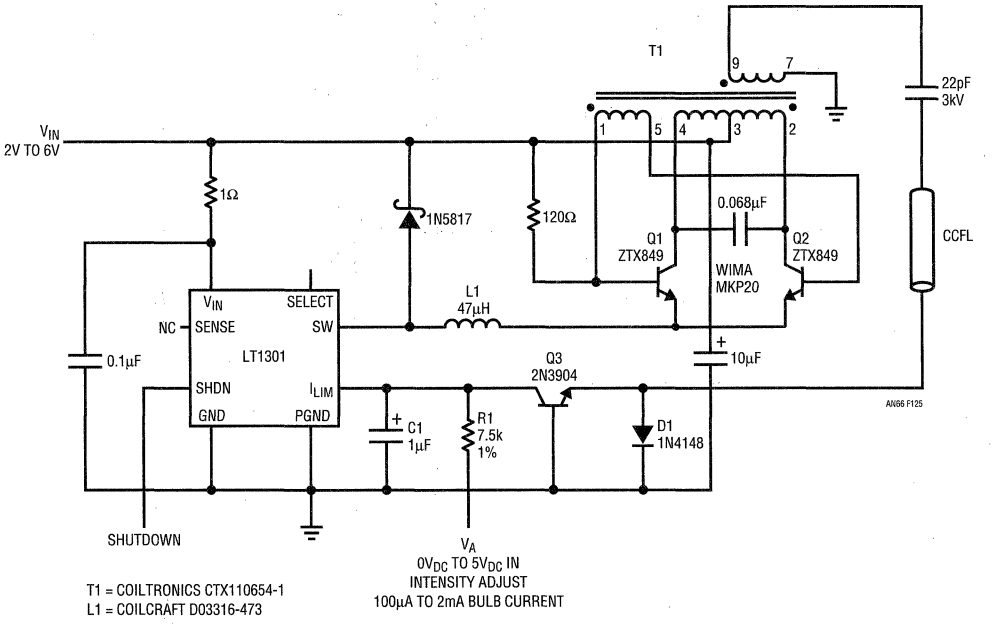


Figure 125. CCFL Power Supply

ALL SURFACE MOUNT EL PANEL DRIVER OPERATES FROM 1.8V TO 8V INPUT

by Steve Pietkiewicz

Electroluminescent (EL) panels offer a viable alternative to LED, incandescent or CCFL backlighting systems in many portable devices. EL panels are thin, rugged, lightweight and consume little power. They require no diffuser and emit an aesthetically pleasing blue-green light. EL panels, being capacitive in nature, typically exhibit about 3000pF per square inch of panel area and require low frequency (50Hz to 1kHz) 120V_{RMS} AC drive. This has traditionally been generated using a low frequency blocking oscillator with a transformer. Although this technique is efficient, transformer size renders the circuit unusable in many applications due to space constraints. Moreover, low frequency transformers are not readily available in surface mount form, complicating assembly.

Figure 126's circuit solves these problems by using an LT1303 micropower switching regulator IC along with a small surface mount transformer in a flyback topology. The 400Hz drive signal is supplied externally. When the drive signal is low, T1 charges the panel until the voltage at point A reaches 240VDC. C1 removes the DC component from the panel drive, resulting in 120VDC at the panel. When the input drive signal goes high the LT1303's FB pin is also pulled high, idling the IC and turning on Q1. Q1's collector pulls point A to ground and the panel to –120VDC. C2 can be added to limit voltage if the panel is disconnected or open. R3 provides intensity control by varying output voltage. Intensity can also be modulated by varying the drive signal's frequency.

Flyback transformer T1 (Dale LPE5047-A132) has a 10µH primary inductance and a 1:15 turns ratio. It measures 12mm by 13.3mm and is 6.3mm high. The 1:15 turns ratio generates high voltage at the output without exceeding the allowable voltage on the LT1303's Switch pin. Schottky diode D1 is required to prevent ringing at the SW pin from forward biasing the IC's substrate diode. Because of T1's low leakage inductance the flyback spike does not exceed 22V. No snubber network is required since the LT1303 SW pin can safely tolerate 25V. R1 and C3 provide decoupling for the IC's V_{IN} pin. Feedback resistor R2 is made from three 3.3M units in series instead of a single 10M resistor. This lessens the possibility of output voltage reduction due to PC board leakage shunting the resistor. Shutdown is accomplished by bringing the IC's SHDN pin high. For minimum current drain in shutdown the 400Hz drive signal should be low.

Figure 127 details relevant circuit waveforms with a 22nF load (about 7 inches of panel) and a 5V input. Trace A is the panel voltage. Trace B shows Switch pin action. The circuit's input current is pictured in trace C and trace D is the 400Hz input signal. The circuit's efficiency measures about 77%. With a 5V input the circuit can deliver 100V_{RMS} at 400Hz into a 44nF load. More voltage can be obtained at lower drive frequencies.

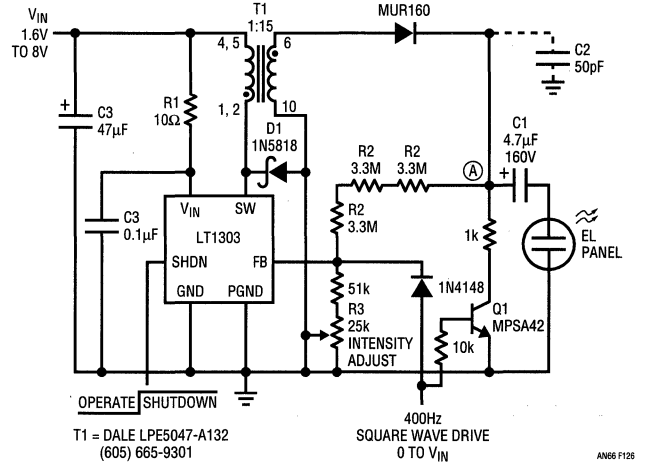
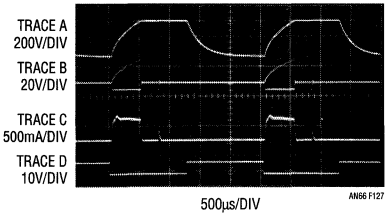


Figure 126. LT1303 Circuit Drives EL Panel



A) HIGH VOLTAGE OUTPUT
B) SWITCH PIN
C) INPUT CURRENT
D) 400Hz DRIVE

Figure 127. Oscillograph of Relevant Circuit Waveforms

A DUAL OUTPUT LCD BIAS VOLTAGE GENERATOR

by Jon A. Dutra

With the many different kinds of LCD displays available, systems manufacturers often want the option of deciding the polarity of the LCD bias voltage at the time of manufacturing.

The circuit in Figure 128 uses the LT1107 micropower DC/DC converter with a single inductor. The LT1107 features an I_{LIM} pin that enables direct control of maximum inductor current. This allows the use of a smaller inductor without the risk of saturation. The LT1111 could also be used with a resulting reduction in output power.

Circuit Operation

The circuit is basically an AC-coupled boost topology. The feedback signal is derived separately from the outputs, so loading of the outputs does not affect loop compensation. Since there is no direct feedback from the outputs, load regulation performance is reduced. With 28V out, from 10% to 100% load (4mA to 40mA), the output voltage sags by about 0.65V. From 1mA to 40mA load, the output voltage sags by about 1.4V. This is acceptable for most displays.

Output noise is reduced by using the auxiliary gain block (AGB) in the feedback path. This added gain effectively reduces the hysteresis of the comparator and tends to randomize output noise. With low ESR capacitors for C2 and C4, output noise is below 30mV over the output load range. Output power increases with $V_{BATTERY}$, from about 1.4W out with 5V in to about 2W out with 8V or more. Efficiency is 80% over a broad output power range.

If only a positive or negative output voltage is required, the two diodes and two capacitors associated with the unused output can be eliminated. The 100kΩ load is required on each output to load a parasitic voltage doubler created by the capacitance of diodes D2 and D4. Without this minimum load, the output voltage can go up to almost 50% above the nominal value.

Component Selection

The voltage at the Switch pin SW1 swings from 0V to V_{OUT} plus two diode drops. This voltage is AC coupled to the positive output through C1 and D1 and to the negative output through C3 and D3. The full output current flows through C1 and C3. Most tantalum capacitors are not rated for current flow and their use can result in field failures.

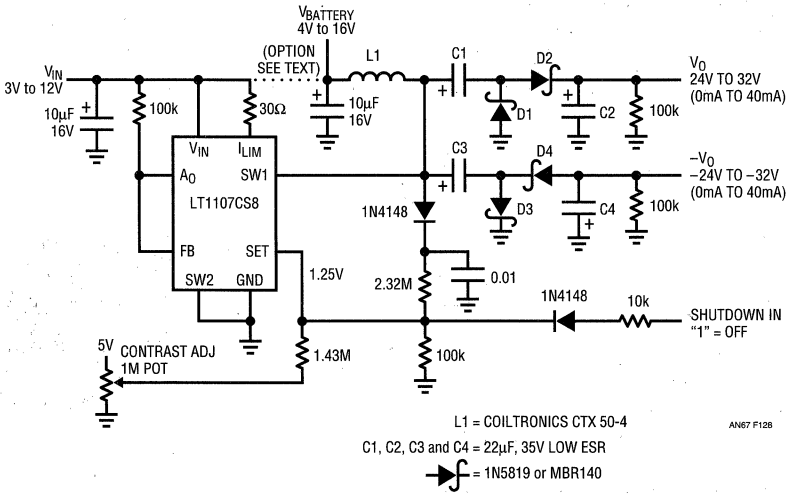


Figure 128. LT1107 Dual Output LCD Bias Generator Schematic Diagram

Use a rated tantalum or a rated electrolytic for longer system life. At lower output currents or higher frequencies, using monolithic ceramics is also feasible.

One could replace the 1N5819 Schottky diodes with 1N4148 types for lower cost, with a reduction in efficiency and load regulation characteristics.

Shutdown

The circuit can be shut down in several ways. The easiest is to pull the Set pin above 1.25V; however, this consumes 300µA in shutdown conditions. A lower power method is to turn off V_{IN} to the LT1107 by means of a high side switch or by simply disabling a logic supply. This drops quiescent current from the $V_{BATTERY}$ input below 10µA. In both cases V_{OUT} drops to 0V. In the event that $+V_{OUT}$ does not need to drop to zero, C1 and D1 can be eliminated.

Output Voltage Adjustment

The output voltage can be adjusted from any voltage above $V_{BATTERY}$ up to 46V with proper passive components. Output voltage can be controlled by the user with DAC, PWM or potentiometer control. By summing currents into the feedback node, the output voltage can be adjusted downward.

LCD BIAS SUPPLY

by Steve Pietkiewicz

An LCD requires a bias supply for contrast control. The supply's variable negative output permits adjustment of display contrast. Relatively little power is involved, easing RF radiation and efficiency requirements. An LCD bias generator is shown in Figure 129. In this circuit, U1 is an LT1173 micropower DC/DC converter. The 3V input is converted to 24V by U1's switch, L2, D1 and C1. The Switch pin (SW1) also drives a charge pump composed of C2, C3, D2 and D3 to generate –24V. Line regulation is less than 0.2% from 3.3V to 2V inputs. Although load regulation suffers somewhat because the –24V output is not directly regulated, it measures 2% for loads from 1mA to 7mA. The circuit will deliver 7mA from a 2V input at 75% efficiency.

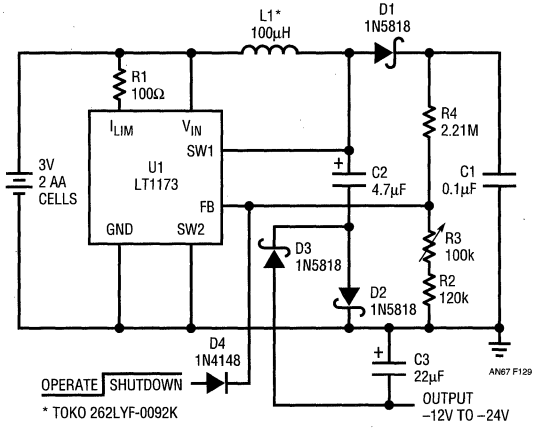


Figure 129. DC/DC Converter Generates LCD Bias

Regulators—Switching (Micropower)

VPP Generator

LTC1262 GENERATES 12V FOR PROGRAMMING FLASH MEMORIES WITHOUT INDUCTORS

by Anthony Ng and Robert Reay

Flash memories require a 5V V_{CC} supply and an additional 12V supply for write or erase cycles. The 12V supply can be a system supply or be generated from the 5V supply using a DC/DC converter circuit. Single supply flash memories (i.e., those with the 12V converter built-in) are available, but these memories have lower capacities and slower write/erase performance and therefore are not as popular as memories without a built-in 12V supply. Flash memories require that the 12V supply be regulated to within 5% and not exceed the permitted maximum voltage (14V for Intel ETOX™ memories). The LTC1262 offers a simple and cost effective 12V programming supply to meet these requirements.

Figure 130 shows a typical application circuit. The only external components needed are four surface mount capacitors. The LTC1262 uses a triple charge pump technique to convert 5V to 12V. It operates from 4.75V to 5.5V and delivers 30mA while regulating the 12V output to within 5%. The TTL-compatible SHDN pin can be driven directly by a microprocessor. When the SHDN pin is taken high (or floated) the LTC1262 enters shutdown mode. In this state the supply current of the LTC1262 is reduced to 0.5µA typical and the 12V output drops to V_{CC}. When SHDN is taken low, the LTC1262 leaves shutdown mode and the output rises to 12V without any potentially harmful overshoot (see Figure 131).

The LTC1262 is available in both 8-pin PDIP and narrow SO packages. With small surface mount capacitors, the complete 12V supply takes up very little space on a printed circuit board. In power sensitive applications, such as PCMCIA flash cards for portable PCs, the LTC1262 shutdown current is low enough to preclude the need for external switching devices when the system is inactive.

ETOX is a trademark of Intel Corporation.

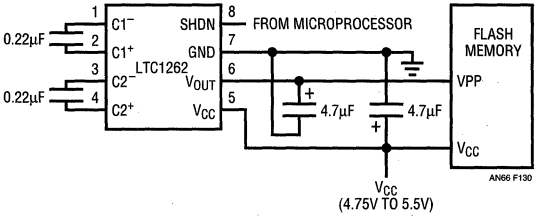


Figure 130. Typical LTC1262 Application Circuit

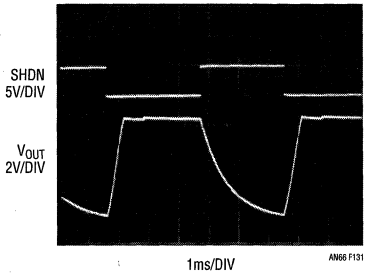


Figure 131. LTC1262 Taken In and Out of Shutdown

FLASH MEMORY VPP GENERATOR SHUTS DOWN WITH 0V OUTPUT

by Sean Gold

Nonvolatile "flash" memories require a well controlled 12V bias (VPP) for programming. The tolerance on VPP is ±5% for 12V memories. Excursions in VPP above 14V or below –0.3V are destructive. VPP is often generated with a boost regulator whose output follows the input supply when shut down. It is sometimes desirable to force VPP to 0V when the memory is not in use or is in read-only mode. The circuit in Figure 132 generates a smoothly rising 12V, 60mA supply that drops to 0V under logic control. Figure 133 illustrates the programming cycle. Shortly after driving the SHDN pin high, the LT1109-12 switching regulator drives L1, producing high voltage pulses at the device's Switch pin. The 1N5818 Schottky diode rectifies these pulses and charges a reservoir capacitor C2. Q1 functions as a low on-resistance pass element. The 1N4148 diode clamps Q1 for reverse voltage protection. The circuit does not overshoot or display unruly dynamics because the

regulator gets its DC feedback directly from the output at Q1's collector. Minor slew aberrations are due to Q1's switching characteristics.

Even with the additional losses introduced by Q1, efficiency is 83% with a 60mA load. Line and load regulation are both less than 1%. Output ripple is about 100mV under light loads. Quiescent current drops to 400µA when shut down. All components shown in Figure 132 are available in surface mount packages, making the circuit well suited for flash memory cards and other applications where minimizing PC board space is critical.

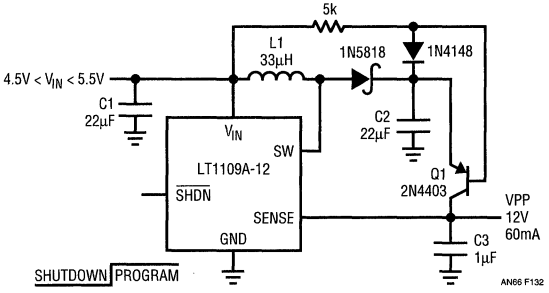


Figure 132. Boost Mode Switching Regulator with Low R_{ON} Pass Transistor for Flash Memory Programming

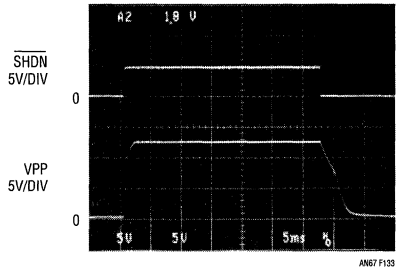


Figure 133. Input and Output Waveforms for the Flash Memory Programming Circuit

Regulators—Linear

LOW NOISE WIRELESS COMMUNICATIONS POWER SUPPLY

by Mitchell Lee and Kevin Vasconcelos

Shown in Figure 134 is a 5V power supply we designed for a synthesizer oscillator. The original design used a 3-terminal regulator but the regulator's voltage noise contributed to excessive phase noise in the oscillator, leading us to this solution. Of prime importance is noise over the 10Hz to 10kHz band. Careful measurements show a 40dB improvement over standard 3-terminal regulators.

The regulator is built around a 5V buried-Zener reference. It is the buried Zener's inherently low noise that makes the finished supply so quiet. Measured over a 10Hz to 10kHz band the 5V output contains just $7\mu V_{RMS}$ noise at full load. The 10Hz to 10kHz noise can be further reduced to $2.5\mu V_{RMS}$ by adding a 100µH, 1000µF output filter. The noise characteristics of the reference are tested and guaranteed to a maximum of 11µV over the band of interest.

An external boost transistor, the ZBD949, provides gain to meet a 200mA output current requirement. Current limiting is achieved by ballasting the pass transistor and clamping base drive. Although our application only requires 200mA, it is possible to extend the output current to at least 1A by selecting an appropriate ballast resistor and addressing attendant thermal considerations in the pass transistor.

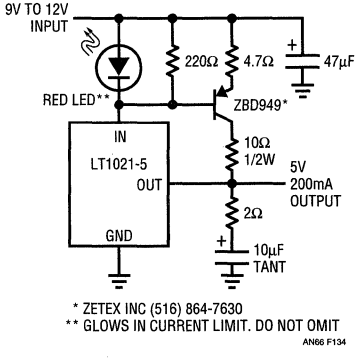


Figure 134. Ultralow Noise 5V, 200mA Supply. Output Noise Is $7\mu V_{RMS}$ Over a 10Hz to 10kHz Bandwidth. Reference Noise Is Guaranteed Less Than $11\mu V_{RMS}$. Standard 3-Terminal Regulators Have 100 Times the Noise and No Guarantees

AN LT1123 ULTRALOW DROPOUT 5V REGULATOR

by Jim Williams and Dennis O'Neill

Switching regulator post regulation, battery-powered apparatus and other applications often require low V_{IN}/V_{OUT} or low dropout linear regulators. For post regulators this is needed for high efficiency. In battery circuits lifetime is significantly affected by regulator dropout. The LT1123, a new low cost reference/control IC, is designed specifically for cost effective duty in such applications. Used in conjunction with a discrete PNP power transistor, the 3-lead TO-92 unit allows very high performance positive regulator designs. The IC contains a 5V bandgap reference, error amplifier, NPN Darlington driver and circuitry for current and thermal limiting.

A low dropout example is the simple 5V circuit of Figure 135 using the LT1123 and an MJE1123 PNP transistor. In operation, the LT1123 sinks Q1 base current through the Drive pin to servo control the FB (feedback) pin to 5V. R1 provides pull-up current to turn Q1 off and R2 is a drive limiter. The 10µF output capacitor (C_{OUT}) provides frequency compensation. The LT1123 is designed to tolerate a wide range of capacitor ESR so that low cost aluminum electrolytics can be be used for C_{OUT}. If the circuit is located more than six inches from the input source, the optional 10µF input capacitor (C_{IN}) should be added.

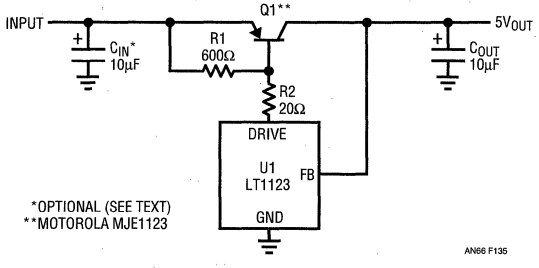


Figure 135. The LT1123 5V Regulator Features Ultralow Dropout

Normally, such configurations require external protection circuitry. Here, the MJE1123 has been cooperatively designed by Motorola and LTC for use with the LT1123. The device is specified for saturation voltage for currents up to 4A with base drive equal to the minimum LT1123 drive current specification. In addition, the MJE1123 is specified for min/max beta at high current. Because of this factor and the defined LT1123 drive, simple current limiting is practical. Excessive output current causes the LT1123 to drive Q1 hard until the LT1123 current limits. Maximum circuit output current is then a product of the LT1123 current and the beta of Q1. The foldback characteristic of the LT1123's drive current combined with the MJE1123 beta and safe area characteristics provide reliable short-circuit limiting. Thermal limiting can also be accomplished by mounting the active devices with good thermal coupling.

Performance of the circuit is notable as it has lower dropout than any monolithic regulator. Line and load regulation are typically within 5mV and initial accuracy is typically inside 1%. Additionally, the regulator is fully short-circuit protected with a no load quiescent current of 1.3mA.

Figure 136 shows typical circuit dropout characteristics in comparison with other IC regulators. Even at 5A the LT1123/MJE1123 circuit dropout is less than 0.5V, decreasing to only 50mV at 1A. Totally monolithic regulators cannot approach these figures, primarily because their power transistors do not offer the MJE1123 combination of high beta and excellent saturation. For example, dropout is ten times lower than in 138 types and significantly better than all the other IC types. Because of Q1's high beta, base drive loss is only 1% to 2% of output current, even at high output currents. This maintains high efficiency under the low V_{IN}/V_{OUT} conditions the circuit will typically see. As an exercise, the MJE1123 was replaced with a 2N4276 germanium device. This provided even lower dropout performance but limiting couldn't be production guaranteed without screening.

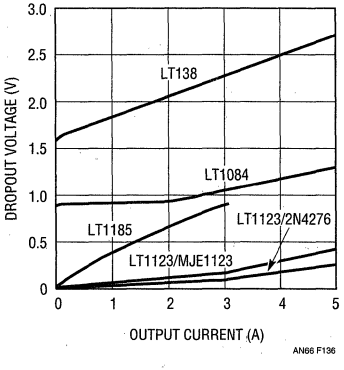


Figure 136. LT1123 Regulator Dropout Voltage vs Output Current

Regulators—Linear (Microprocessor Power)

LT1580 LOW DROPOUT REGULATOR USES NEW APPROACH TO ACHIEVE HIGH PERFORMANCE

by Craig Varga

Enter the LT1580

The LT1580 NPN regulator is designed to make use of the higher supply voltages already present in most systems. The higher voltage source is used to provide power for the control circuitry and supply the drive current to the NPN output transistor. This allows the NPN to be driven into saturation, thereby reducing the dropout voltage by a V_{BE} compared to a conventional design.

The LT1580 is capable of 7A maximum with approximately 0.8V input-to-output differential. The current requirement for the control voltage source is approximately 1/100 of the output load current or about 70mA for a 7A load.

Circuit Examples

Figure 137 shows a circuit designed to deliver 2.5V from a 3.3V source with 5V available for the control voltage. Figure 138 shows the response to a load step of 200mA to 4.0A. The circuit is configured with a 0.33µF Adjust pin bypass capacitor. The performance without this capacitor is shown in Figure 139. This difference in performance is the reason for providing the Adjust pin on the fixed voltage devices. A substantial savings in expensive output decoupling capacitance may be realized by adding a small "1206-case" ceramic capacitor at this pin.

Figure 140 shows an example of a circuit with shutdown capability. By switching the control voltage rather than the main supply, the transistor providing the switch function needs only a small fraction of the current handling ability that it would need if it was switching the main supply. Also, in most applications it is not necessary to hold the voltage drop across the controlling switch to a very low level to maintain low dropout performance.

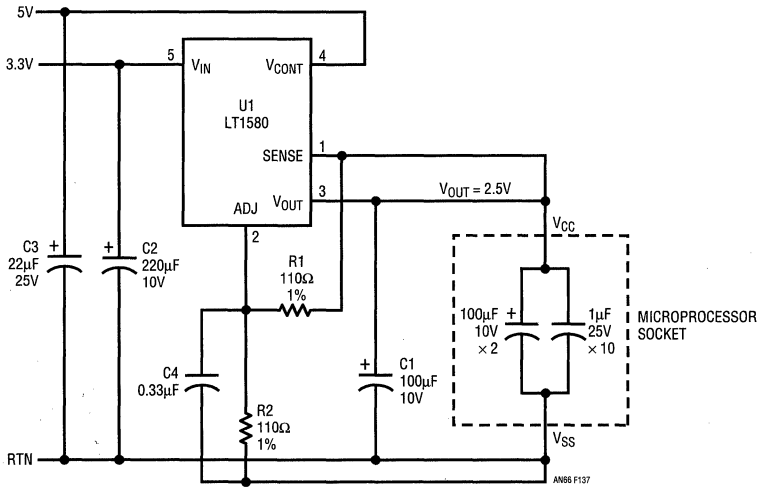


Figure 137. LT1580 Delivers 2.5V from 3.3V at up to 6A

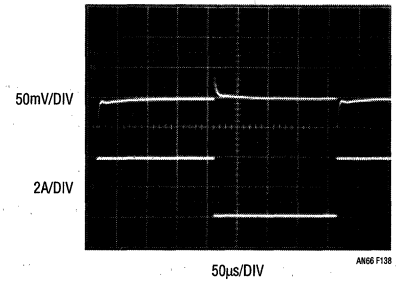


Figure 138. Transient Response of Figure 137's Circuit with Adjust Pin Bypass Capacitor. Load Step Is from 200mA to 4A

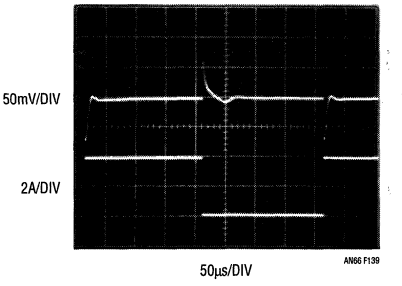


Figure 139. Transient Response Without Adjust Pin Bypass Capacitor. Otherwise, Conditions Are the Same as in Figure 138

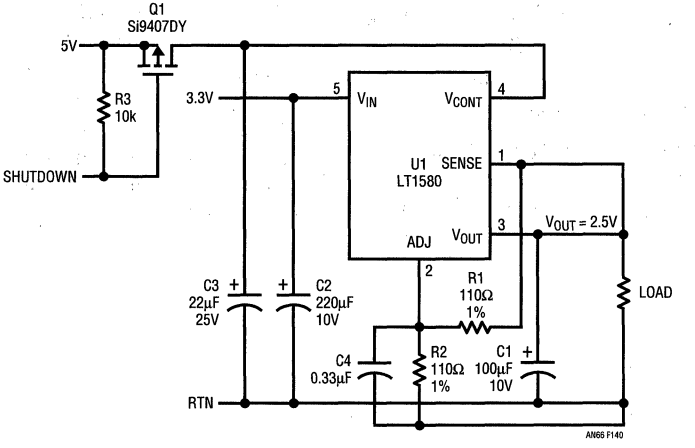


Figure 140. Small FET Adds Shutdown Capability to LT1580 Circuit

LT1585: NEW LINEAR REGULATOR SOLVES LOAD TRANSIENTS

by Craig Varga

The latest hot new microprocessors have added a significant complication to the design of the power supplies that feed them. These devices have the ability to switch from consuming very little power to requiring several amps in tens of nanoseconds. To add a further complication, they are extremely intolerant of supply voltage variations. Gone are the days of the popcorn 3-terminal regulator and the 0.1µF decoupling capacitor. The LT1585 is the first low dropout regulator specifically designed for tight output voltage tolerance (optimized for the latest generation processors) and fast transient response.

Figure 141 shows the kind of response that can and must be achieved if these microprocessors are to operate reliably. Figure 142 details the first several microseconds of

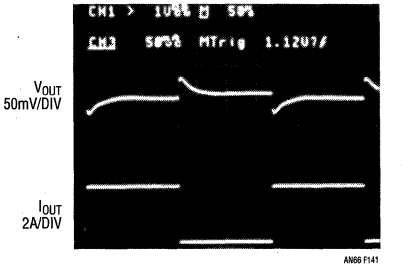


Figure 141. Transient Response of 200mA to 4A Load Step

the transient in Figure 141. The load change in this case is 3.8A in about 20ns. Two parasitic elements dominate the transient performance of the system. Both are controlled by the type, quantity and location of the decoupling capacitors in the system.

Anatomy of a Load Transient

The instantaneous droop at the leading edge of the transient is the result of the sum of the effects of the equivalent series resistance (ESR) and the equivalent series inductance (ESL) from the output capacitor(s) terminal(s) to the load connection. Note that these contributions also include the lead trace parasitics from the capacitor(s) to the load.

The resistive component is simply $\Delta I \bullet ESR$. The droop to point A, 23.6mV, is the ESR contribution. Calculating ESR:

$$23.6mV/3.8A = 0.0062\Omega$$

The effects of inductance are predicted by the formula $V = L dI/dt$. The voltage from point A to the bottom of the trough is the inductive contribution (13.4mV). ESL is calculated to be 0.07nH. After the load current stops rising the inductive effects end, bringing the voltage to point B. At this point the curve settles into a gentle droop. The droop rate is $dV/dt = I/C$. There is about 1300µF of useful capacitance on the board in this case (see Figure 143). As the regulator output current starts to approach the new load current, the droop rate lessens until the regulator supplies the full load current. This is the inflection point in the curve. Since the regulator now measures the output voltage as being too low, it overshoots the load current and recharges the output capacitors to the correct voltage.

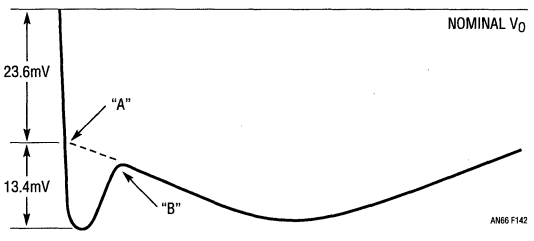


Figure 142. Detailed Sketch of First Few Microseconds of Transients

Faster Regulator Means Fewer Capacitors, Less Board Space

The regulator has one major effect on the system's transient behavior. The faster the regulator, the less bulk capacitance is needed to keep the droop from becoming excessive. It is here that the advantage of the LT1585 shows up. The response time of the LT1585 is about one-half that of the last generation 3-terminal regulators.

The response in the first several hundred nanoseconds is controlled by the careful placement of bypass capacitors. Figure 143 is a schematic diagram of the circuit but the layout is critical so consult the LTC factory for circuit and layout information.

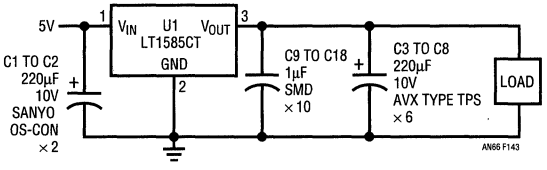


Figure 143. Schematic Diagram: LT1585 Responding to Fast Transients

Battery Chargers

CHARGING NiMH/NiCd OR Li-Ion WITH THE LT1510

by Chia Wei Liao

Charging NiMH or NiCd Batteries

The circuit in Figure 144 will charge battery cells with voltages up to 20V at a full charge current of 1A (when Q1 is ON) and a trickle charge current of 100mA (when Q1 is OFF). If the third charging level is needed, simply add a resistor and a switch. The basic formula for charging current is:

$$\frac{2.465}{R1 \| R2} (2000) \text{ (when Q1 ON)}$$

$$\frac{2.465}{R1} (2000) \text{ (when Q1 OFF)}$$

For NiMH batteries, a pulsed trickle charge can be easily implemented with a switch in series with R1; switch Q1 at the desired rate and duty cycle. If a microcontroller is used to control the charging, connect the DAC current-sink output to the PROG pin.

Charging Li-Ion Batteries

The circuit in Figure 145 will charge lithium-ion batteries at a constant current of 1.5A until battery voltage reaches 8.4V, set by R3 and R4. It then goes into constant voltage charging and the current slowly tapers off to zero. Q3 can be added to disconnect R3 and R4 so they will not drain the battery when the wall adapter is unplugged.

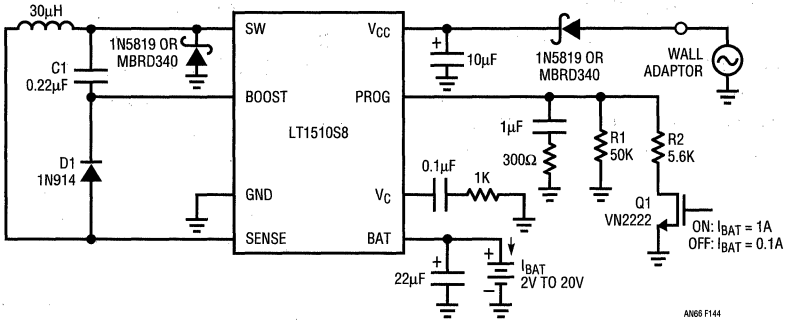


Figure 144. Charging NiCd or NiMH Batteries

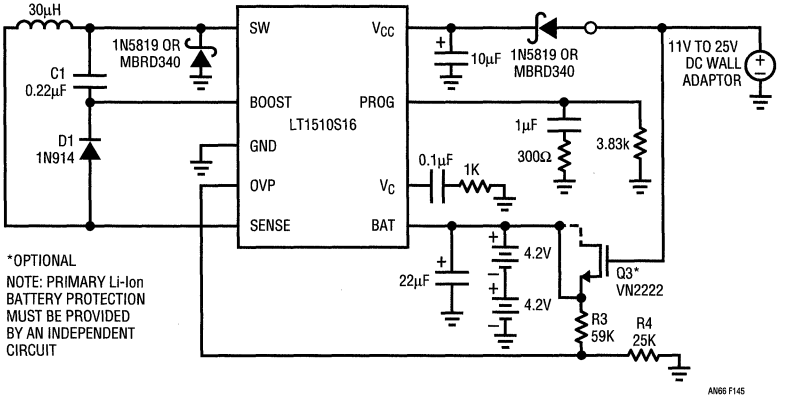


Figure 145. Charging Li-Ion Batteries

Typical Charging Algorithms

The following algorithms are representative of current techniques:

Lithium-Ion — charge at constant voltage with current limiting set to protect components and to avoid overloading the charging source. When the battery voltage reaches the programmed voltage limit, current will automatically decay to float levels. The accuracy of the float voltage is critical for long battery life. Be aware that lithium-ion batteries in series suffer from "walk away" because of the required constant float voltage charging technique. "Walk away" is a condition where the batteries in the series string wind up in different states of the charge/discharge cycle. They may need to be balanced by redistributing charge from one battery to another. This phenomenon is minimized by carefully matching the batteries within a pack.

Nickel-Cadmium — charge at a constant current determined by the power available or by a maximum specified by the manufacturer. Monitor battery charge state using voltage change with time (dV/dt), second derivative of voltage (d^2V/dt), battery pressure or some combination of these parameters. When the battery approaches full charge, reduce the charging current to a value (top-off) that can be maintained for a long time without harming the battery. After the top-off period, usually set by a simple time out, reduce the current further to a trickle level that can be maintained indefinitely, typically 1/10 to 1/20 of the battery capacity.

Nickel-Metal-Hydride — same as NiCd except that some NiMH batteries cannot tolerate a *continuous* low level trickle charge. Instead they require a pulsed current of moderate value with a low duty cycle so that the average current represents a trickle level. A typical scenario would be one second ON and thirty seconds OFF with the current set to thirty times desired trickle level.

LITHIUM-ION BATTERY CHARGER

by Dimitry Goder

Lithium-ion (Li-Ion) rechargeable batteries are quickly gaining popularity in a variety of applications. The main reasons for the success of Li-Ion cells are higher power density and higher terminal voltage compared to other currently available battery technologies. The basic charging principle for a Li-Ion battery is quite simple: apply a constant voltage source with a built-in current limit. A depleted battery is charged with a constant current until it reaches a specific voltage (usually 4.2V per cell), then it floats at this voltage for an indefinite period. The main difficulty with charging Li-Ion cells is that the floating voltage accuracy needs to be around 1%, with 5% current-limit accuracy. These two targets are fairly difficult to achieve. Figure 146 shows the schematic of a full solution for a Li-Ion charger.

The battery charger is built around the LTC1147, a high efficiency step-down regulator controller. The IC's constant off-time architecture and current mode control ensure circuit simplicity and fast transient response. At the beginning of the ON cycle, P-channel MOSFET Q1 turns on and the current ramps up in the inductor. An internal current comparator senses the voltage proportional to the inductor current across sense resistor R13. When this voltage reaches a preset value, the LTC1147 turns Q1 off for a fixed period of time set by C1. After the off-time the cycle repeats.

To provide an accurate current limit, U3A and Q2 are used to sense the charging current separately from the LTC1147. U3A forces the voltage across R11 to match the average drop across the current sense resistor R13. This voltage sets Q2's drain current, which flows unchanged to the source. As a result the same voltage appears across R9, which is now referenced to ground. Since C5 provides high frequency filtering, U3A shifts the average value of the output current. N-channel MOSFET Q2 ensures correct circuit operation even under short-circuit conditions by allowing current sensing at potentials close to ground.

U3B monitors voltage across R9 and acts to keep it constant by comparing it to the reference voltage. Diode D3 is connected in series with U3B's output, allowing the circuit to operate as a current limiter. The current feedback circuit is not active if the output current limit has not been reached.

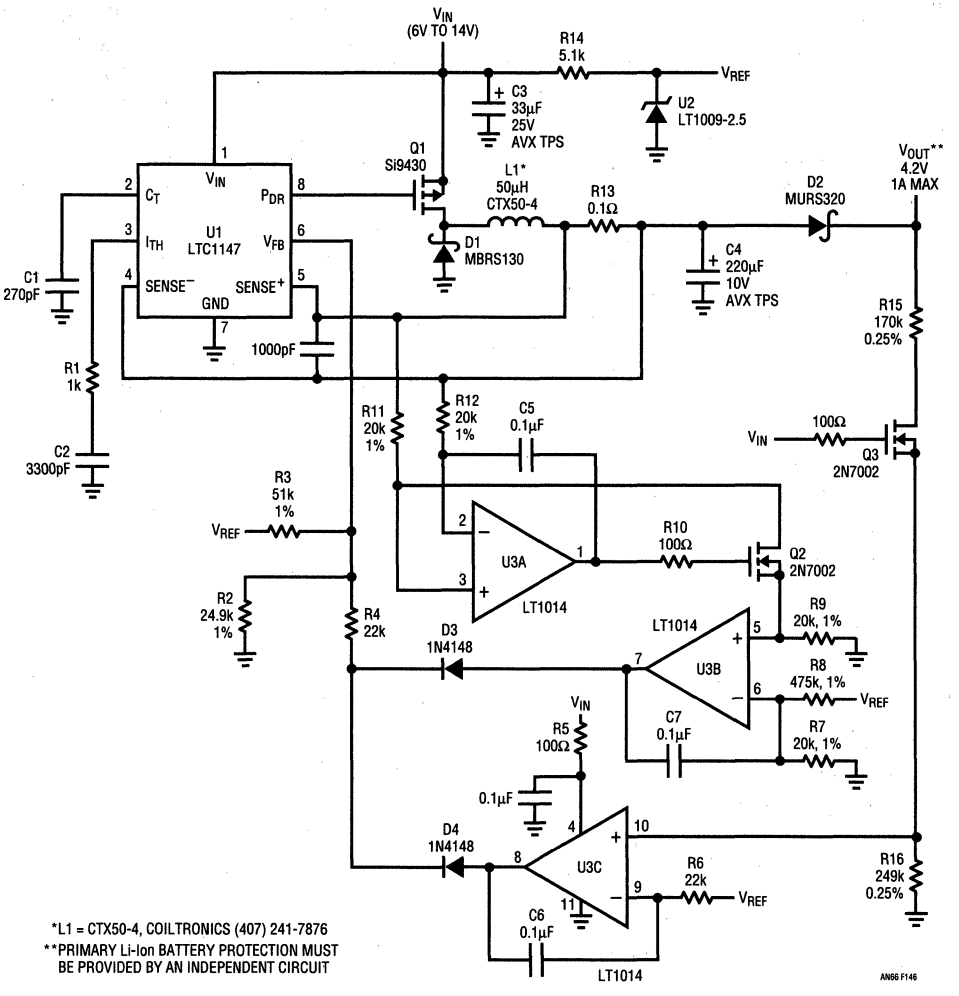


Figure 146. Li-Ion Battery Charger Schematic

U3C provides the voltage feedback by comparing the output voltage to the reference. The feedback resistor ratio [R16/(R15 + R16)] sets the output at exactly 4.2V. U3C has a diode (D4) connected in series with its output. This diode ensures that the voltage and current feedback circuits do not operate at the same time. The reference voltage is supplied by the LT1009, with a guaranteed initial tolerance of 0.2%. Together with the 0.25% feedback resistors, the circuit provides less than 1% output voltage error over temperature.

When the input voltage is not present Q3 is automatically turned off and the feedback resistors do not discharge the battery. Diode D2 is connected in series with the output, preventing the battery from supplying reverse current to the charger.

SIMPLE BATTERY CHARGER RUNS AT 1MHz

by Mitchell Lee

Fast switching regulators have reduced coil sizes to the point that they are no longer the largest components on the board. A case in point is the LT1377, which can operate at 1MHz with inductances under 10µH.

The circuit shown in Figure 147 was designed for a customer who wanted to charge a 4-cell NiCd pack from a 5V logic supply. (This circuit will work equally well with a 3.3V input.) Clearly the circuit needs an output voltage greater than 5V, which is handled easily by the LT1377 boost regulator. The output current is limited to approximately 50mA by a V_{BE} current sensor (Q1/R1) controlling the Feedback pin (2) of the LT1377. This current is perfect for slow charging or trickle charging AA NiCd batteries.

Battery chargers are commonly subject to a number of fault conditions, which must be addressed in the design phase. First, what happens when the battery is disconnected? In a boost regulator the output voltage will increase without bound and blow up either the output capacitor or switch. Some voltage limiting is necessary, and D2 serves this purpose. If the voltage on C3 rises to 11.25V, D2 takes over the control loop at the Feedback pin.

Another potential calamity is an output short circuit; a related fault results from connecting a battery pack containing one or more shorted cells, such that the terminal voltage is less than about 4V. Under either of these circumstances, unlimited current flows from the 5V input supply, through D1 and Q1's base-emitter junction, frying at least Q1.

Q2 has been added to allow full current control even when the output voltage is less than the input voltage. In normal operation, where the output is boosted higher than 5V, Q2 is fully on. Its gate is held at 1.25V (Pin 2 feedback voltage) and its source is greater than 5V; hence it has no choice but to be fully enhanced. Q2 becomes more functional when the output voltage drops to around 4V. First of all, at 4V input the switching regulator stops switching because more than 50mA current flows and the feedback pin is pulled up above 1.25V—Q1 makes sure of that. But as Q1's collector continues to rise, Q2 is gradually cut off, at least to the extent necessary to starve the drain current back to about 50mA. This action works right down to $V_{OUT} = 0$. In a short circuit Q2 dissipates about 200mW, not too much for a surface mount MOSFET.

This circuit is useful for four to six cells and the output current can be modified somewhat by changing sense resistor R1. A reasonable range is from very low currents (1mA or less) up to 100mA. The current will diminish as Q1's V_{BE} drops about 0.3%/°C with temperature.

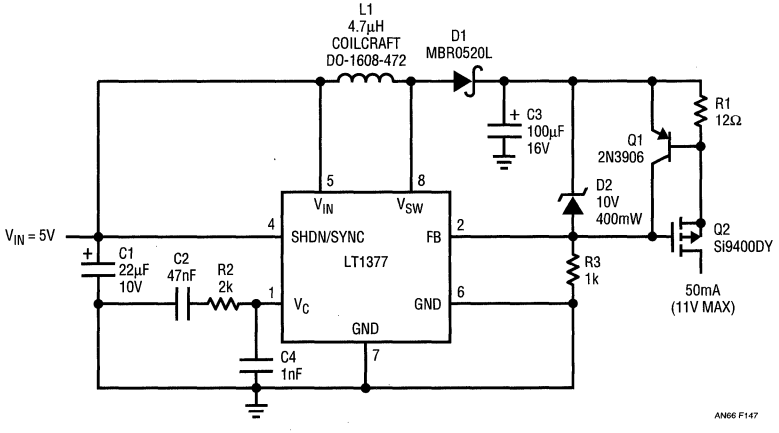


Figure 147. Battery Charger Schematic Diagram

A PERFECTLY TEMPERATURE-COMPENSATED BATTERY CHARGER

by Mitchell Lee and Kevin Vasconcelos

Battery charging circuits are usually greeted with a yawn, but this lead-acid charger offers a combination of features that sets it apart from all others. It incorporates a low dropout regulator, temperature compensation, dual-rate charging, true negative ground and consumes zero standby current.

The LT1083 family of linear regulators exhibits dropout characteristics of less than 1.5V as compared to 2.5V in standard regulators. A smaller regulator drop allows for lower input voltages and less power dissipation in the regulator. In this application the regulator is used to control charging voltage and limit maximum charging current.

The temperature compensation employed in this circuit, unlike diode-based straight-line approximations, follows the true curvature of a lead-acid cell. This prevents over or undercharging of the battery during periods of extended low or high ambient temperatures. Temperature compensation is conveniently provided by a Tempsistor® as shown in Figure 148. The Tempsistor is used to generate a temperature-dependent current, which, in turn, adjusts the charger's output voltage to match that of the battery. The match is within 100mV for a 12V battery over a range of –10°C to 60°C. The best place for the Tempsistor is directly under the battery with the battery resting on a pad of styrofoam.

Q1 provides a low voltage disconnect function that reduces the charger standby current to zero. When the input voltage (from a rectified transformer) is available, Q1 is biased ON and Q2 is turned ON. Q2 connects the various current paths on the output of the regulator to ground, activating the charging circuitry. If the input voltage is removed, Q1 and Q2 turn off, and all current paths from the battery to ground (except for the load, of course) are interrupted. This prevents unnecessary battery drain when the charging source is not available.

A dual-rate charging characteristic is achieved by means of a current-sense resistor (R_S) and a sense comparator (LT1012). If the battery charge current exceeds the float-current threshold of $10mV/R_S$, the comparator pulls the gate of Q3 low, increasing the output voltage by 600mV. This sets the charging voltage to 14.4V at 25°C. After the battery reaches full charge the current will fall below the $10mV/R_S$ threshold and the LT1012 will short out R7, reducing the output by 600mV to a float level of 13.8V.

Tempsistor is a registered trademark of Thermodisc Inc.

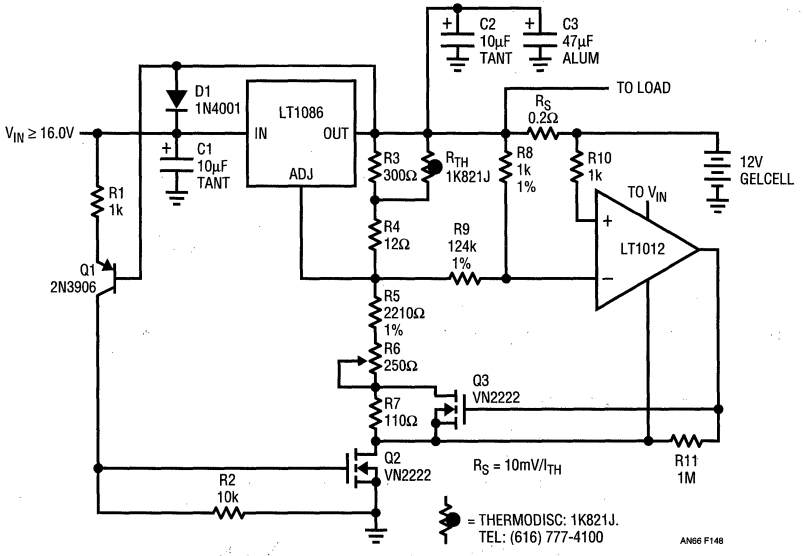


Figure 148. Battery Charger Follows Temperature Coefficient of a Lead-Acid Cell Very Accurately

Both the float and charging voltages can be trimmed by R6; R7 sets the 600mV difference between them.

With the charging source connected, the sense resistor R_S measures only battery current. This eliminates the tendency found in some schemes for the charger to trip on load current.

Table 1 simplifies the selection of an appropriate regulator for batteries of up to 48 Ampere-hours (Ah). The selection is based on providing a minimum available charge current of at least C/4, where C represents the battery's Ampere-hour capacity. The next larger regulator may be required in applications where sustained load currents of greater than C/10 are expected.

If you want to set the trip current to an exact figure, the current shunt R_S can be calculated as $R_S = 10mV/I_{TH}$. For a threshold of C/100 this reduces to $R_S = 1/C$.

Table 1. The Regulator Should Be Chosen to Provide at Least C/4 Charging Current

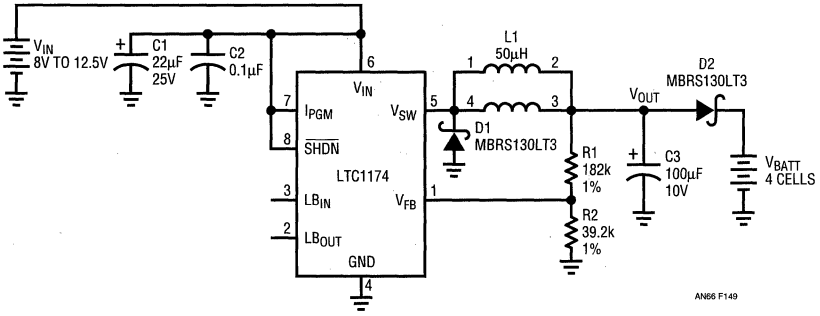
BATTERY CAPACITY	DEVICE	MAXIMUM CHARGING CURRENT	FLOAT CURRENT THRESHOLD	SENSE RESISTOR (SHUNT)
≤3Ah	LT1117	0.8A	20mA	0.5Ω
3Ah to 6Ah	LT1086	1.5A	50mA	0.2Ω
6Ah to 12Ah	LT1085	3.2A	100mA	0.1Ω
12Ah to 24Ah	LT1084	5.5A	200mA	0.05Ω
24Ah to 48Ah	LT1083	8.0A	400mA	0.025Ω

A SIMPLE 300mA NiCd BATTERY CHARGER

by Randy G. Flatness

Low current battery charger circuits are required in handheld products such as palmtop, pen-based and fingertip computers. The charging circuitry for these applications must use surface mount components and consume minimal board space. The circuit shown in Figure 149 meets both of these requirements.

The circuit shown in Figure 149 uses an LTC1174 to control the charging circuit. A fully self-contained switching regulator IC, the LTC1174 contains both a power switch and the control circuitry (constant off-time controller, reference voltage, error amplifier and protection circuitry). The internal power switch is a P-channel MOSFET transistor in a common-source configuration; consequently when the switch turns on, the LTC1174's V_{SW} pin is



C1 = AVX (TA) TPSD226M025R0200 ESR = 0.200 I_{RMS} = 0.775A
C3 = AVX (TA) TPSD107M010R0100 ESR = 0.100 I_{RMS} = 1.095A
D1, D2 = MOTOROLA SCHOTTKY VBR = 30V
L1 = COILTRONICS CTX50-2P DCR = 0.212 IDC = 0.729A TYPE 52 CORE
COILTRONICS (407) 241-7876

$V_{OUT} = 1.25V \bullet (1 + R1/R2) = 7.0V$

$$\text{FAST CHARGE} \approx 0.6A - \frac{(V_{BATT} + 0.6V) \bullet 4\mu s}{2 \bullet L} \quad \text{(EQ.1)}$$

Figure 149. 4-Cell, 300mA LTC1174 Battery Charger Implemented with All Surface Mount Components

connected to the input voltage. This power switch handles peak currents of 600mA. The LTC1174's architecture allows it to achieve 100% duty cycle, forcing the internal P-channel MOSFET on 100% of the time.

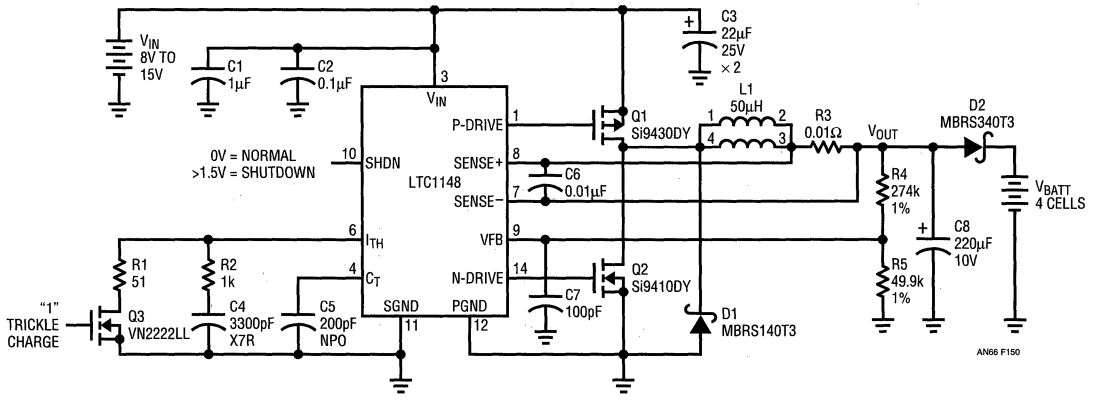
When the batteries are being charged, the resistor divider network (R1 and R2) forces the LTC1174's Feedback pin (V_{FB}) below 1.25V, causing the LTC1174 to operate at the maximum output current. An internal 0.1Ω resistor senses this current and sets it at approximately 300mA, according to equation 1 (shown on the schematic). When the batteries are disconnected, the error amplifier drives the Feedback pin to 1.25V, limiting the output voltage to 7.0V. Diode D2 prevents the batteries from discharging through the divider network when the charger is shut down. In shutdown mode less than 10µA of supply current is drawn from the input supply.

HIGH EFFICIENCY (>90%) NiCd BATTERY CHARGER CIRCUIT PROGRAMMABLE FOR 1.3A FAST CHARGE OR 100mA TRICKLE CHARGE

by Brian Huffman

Battery charger circuits are of universal interest to laptop, notebook and palmtop computer manufacturers. High efficiency is desirable in these applications to minimize the power dissipated in the surface mount components. The circuit shown in Figure 150 is designed to charge four NiCd cells at a 1.3A fast charge or a 100mA trickle charge with efficiency exceeding 90%. This circuit can be modified easily to handle up to eight NiCd cells.

The circuit uses an LTC1148 in a step-down configuration to control the charge rate. The LTC1148 is a synchronous switching regulator controller that drives external, complementary power MOSFETs using a constant off-time current mode architecture. When the LTC1148's P-drive output pulls the gate of Q1 low, the P-channel MOSFET turns on and connects one side of the inductor to the input voltage. During this period, current flows from the input through Q1,



C1 = (TA)
C3 = AVX (TA) TPSD226K025R0200 ESR = 0.200 IRMS = 0.775A
C8 = AVX (TA) TPSE227M010R0100 ESR = 0.100 IRMS = 1.149A
Q1 = SILICONIX PMOS BVDSS = 20V RDS_{ON} = 0.125 C_{RSS} = 400pF Q_G = 25nC θJA = 50°C/W
Q2 = SILICONIX NMOS BVDSS = 30V RDS_{ON} = 0.050 C_{RSS} = 160pF Q_G = 50nC θJA = 50°C/W
D1, D2 = MOTOROLA SCHOTTKY VBR =40V
R3 = KRL SP-1/2-A1-0R100J Pd = 0.75V
L1 = COILTRONICS CTX50-4 DCR = 0.175 IDC = 1.350A KOOL Mµ CORE

ALL OTHER CAPACITORS ARE CERAMIC

COILTRONICS (407) 241-7876
KRL (809) 668-3210

V_{OUT} = 1.25V • (1 + R4/R5) = 8.1V

FAST CHARGE = 130mV/R3 = 1.3A (EQ. 1)
TRICKLE CHARGE = 100mA (SEE FIGURE 2)

Figure 150. 4-Cell, 1.3A Battery Charger Implemented in Surface Mount Technology

through the inductor and into the battery. When the LTC1148 P-drive pin goes high, Q1 is turned off and the voltage on the drain of Q1 drops until the clamp diode is forward biased. The diode conducts for a very short period of time, until the LTC1148 internal circuitry senses that the P-channel is fully off, preventing the simultaneous conduction of Q1 and Q2. Then the N-drive output goes high, turning on Q2, which shorts out D1. Now the inductor current flows through the N-channel MOSFET instead of through the diode, increasing efficiency. This type of switching architecture is known as synchronous rectification.

During the fast-charge interval, the resistor divider network (R4 and R5) forces the LTC1148's Feedback pin (V_{FB}) below 1.25V, causing the LTC1148 to operate at the maximum output current. R3, a 0.1Ω resistor, senses the current and sets it at approximately 1.3A according to equation 1 in Figure 150. When the batteries are disconnected, the error amplifier forces the Feedback pin to 1.25V, limiting the output voltage to 8.1V. Diode D2 prevents the batteries from discharging through the divider network when the charger is shut down. In shutdown mode the circuit draws less than 20μA from the input supply.

The dual rate charging is controlled by Q3, which can be toggled between fast charge and trickle charge. The trickle charge rate is set by resistor R1. Figure 151 is a graph showing the value of R1 for a given trickle charge output current. The trickle charge current can also be varied by using an op amp to force the Threshold pin voltage within its 0V to 2V range. Figure 152 shows the output current as a function of Threshold pin voltage.

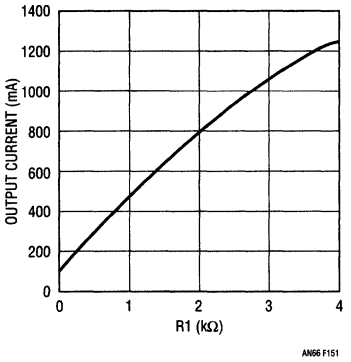


Figure 151. LTC1148 Output Current Voice Trickle Charge Set Resistance (R1)

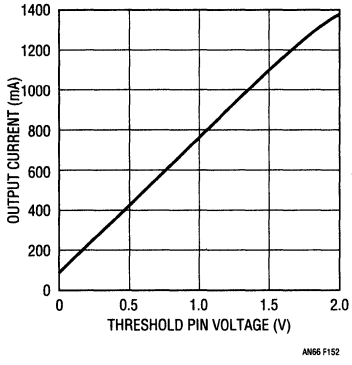


Figure 152. LTC1148 Output Current vs Forced Threshold Pin Voltage

Power Management

LT1366 RAIL-TO-RAIL AMPLIFIER CONTROLS TOPSIDE CURRENT

by William Jett and Sean Gold

Topside Current Source

The circuit shown in Figure 153 takes advantage of the LT1366's rail-to-rail input range to form a wide-compliance current source. The LT1366 adjusts Q1's gate voltage to force the voltage across the sense resistor (R_{SENSE}) to equal the voltage from the supply to the potentiometer's wiper. A rail-to-rail op amp is needed because the voltage across the sense resistor must drop to zero when the divided reference voltage is set to zero. Q2 acts as a constant current sink to minimize error in the reference voltage when the supply voltage varies.

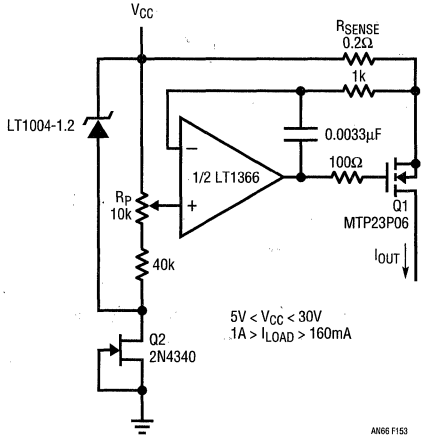


Figure 153. Topside Current Source

The circuit can operate over a wide supply range (5V < V_{CC} < 30V). At low input voltage, circuit operation is limited by the MOSFET's gate-drive requirements. At high input voltage, circuit operation is limited by the LT1366's absolute maximum ratings and the output power requirements.

In this example the circuit delivers 1A at 200mV of sense voltage. With a 5V input supply the power dissipation is 5W. For operation at 70°C ambient temperature, the MOSFET's heat sink must have a thermal resistance of:

$$\theta_{HS} = \theta_{JA\ SYSTEM} - \theta_{JC\ FET} = 55°C/5W - 1.25°C/W$$
$$= 9.75°C/W$$

This is easily achievable with a small heat sink. When input voltages are greater than 5V the use of a larger heat sink or derating of the output current is necessary.

The circuit's supply regulation is about 0.03%/V. The output impedance is equal to the MOSFET's output impedance multiplied by the op amp's open-loop gain. Degradations in current source compliance occur when the voltage across the MOSFET's on-resistance and the sense resistor drops below the voltage required to maintain the desired output current. This condition occurs when $V_{CC} - V_{OUT} < I_{LOAD}\ (R_{SENSE} + R_{ON})$.

High Side Current Sense Amplifier

In power control it is sometimes necessary to sense load current at low loss near the input supply. The current sense amplifier shown in Figure 154 amplifies the voltage across a small value sense resistor by the ratio of the current source resistors (R2/R1). The LT1366 forces the low power MOSFET's gate voltage such that the sense voltage appears across a current source resistor R1. The resulting current in Q1's drain is converted to a ground referred voltage at R2. ($V_O = I_{IN}\ R_S\ [R2/R1]$)

The circuit takes advantage of the LT1366's ability to sense signals up to the supply rail, which permits the use of small value, low loss sense resistors. The LT1366 and the gain setting resistors are also biased at low current to reduce losses in the current sense.

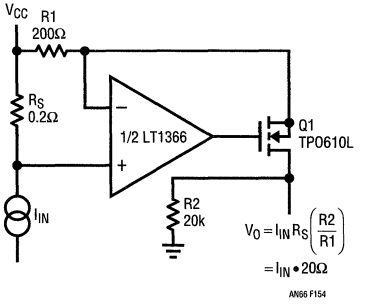


Figure 154. High Side Current Sense Amplifier

AN ISOLATED HIGH SIDE DRIVER

by James Herr

Introduction

The LTC1146 low power digital isolator draws only 70µA of supply current with V_{IN} = 5V. Its low supply current feature is well suited for battery-powered systems that require isolation, such as an isolated high side driver. The LTC1146A is rated at 2500V_{RMS} and is UL approved. The LTC1146 is intended for less stringent applications and is rated at 500VDC.

Theory of Operation

Optoisolators available today require supply currents in the milliampere range even for low speed operation (less than 20kHz). This high supply current is another drain on the battery. Figure 155 shows the alternative of using an LTC1146A to drive an external power MOSFET (IRF840) at speeds to 20kHz with V^+ = 300V.

The Input pin of LTC1146A must be driven with a signal that swings at least 3V (referred to GND1, which is a floating ground). The O_S pin outputs a square wave corresponding to the input signal but with a time delay. The amplitude of the output square wave is equal to the potential at the V_{CC} pin. The TL4426 is a high speed MOSFET driver used here to supply gate drive current to the power MOSFET. The power supply to the LTC1146A and the TL4426 is bootstrapped from a 13V supply referred to system ground. C1 supplies the current to both the LTC1146A and the TL4426 when the power MOSFET is being turned on. Its value should be increased when the input signal's ON time increases. D3 prevents the output from swinging negative due to stray inductance. If the output goes below ground, the gate-to-source voltage of the IRF840 rises. This high potential could damage the power MOSFET. The output slew rate should be limited to 1000V/µs to prevent glitches on the O_S output of the LTC1146A.

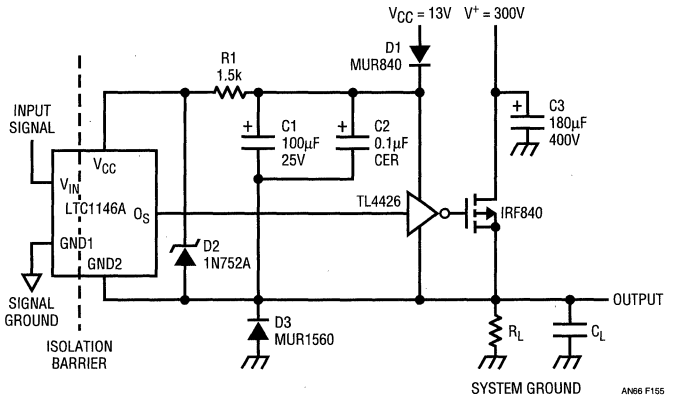


Figure 155. Isolated High Side Driver Schematic Diagram

LTC1163: 2-CELL POWER MANAGEMENT

by Tim Skovmand

The LTC1163 1.8V to 6V high side MOSFET driver allows inexpensive N-channel switches to be used to efficiently manage power in 2-cell systems such as palmtop computers, portable medical equipment, cellular telephones and personal organizers.

Any supply voltage above 3V, such as 3.3V, 5V or 12V, can be generated by step-up converters powered from a 2-cell supply. Step-up regulators are typically configured as shown in Figure 156. An inductor is connected directly to the 2-cell battery pack and switched by a large (1A) switch. The inductor current is then passed through a low drop Schottky rectifier to charge the output capacitor to a voltage higher than the input voltage. Unfortunately, when the regulator is shut down, the inductor and diode remain connected and the load may leak significant current in standby.

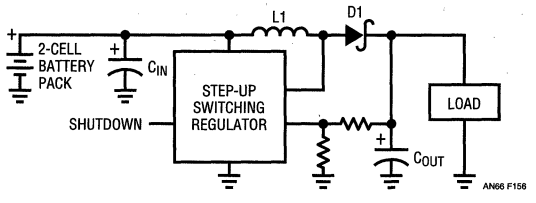


Figure 156. Typical Step-Up Converter Topology

One possible solution to this problem is to add a low $R_{DS(ON)}$ MOSFET switch between the battery pack and the input of the regulator to completely disconnect it and the load from the battery pack. MOSFET switches, however, cannot operate directly from 2-cell battery supplies because the gate voltage is limited to 3V with fresh cells and 1.8V when the cells are fully discharged.

The LTC1163 solves this problem by generating gate drive voltages that fully enhance high side N-channel switches when powered from a 2-cell battery pack, as shown in Figure 157. The standby current with all three drivers switched off is typically 0.01µA. The quiescent current rises to 85µA per channel with the input turned on and the charge pump producing 10V (above ground) from a 3V supply. The surface mount MOSFET switches shown are guaranteed to be less than 0.1Ω with V_{GS} = 5V and less than 0.12Ω with V_{GS} = 4V and therefore have extremely low voltage drops.

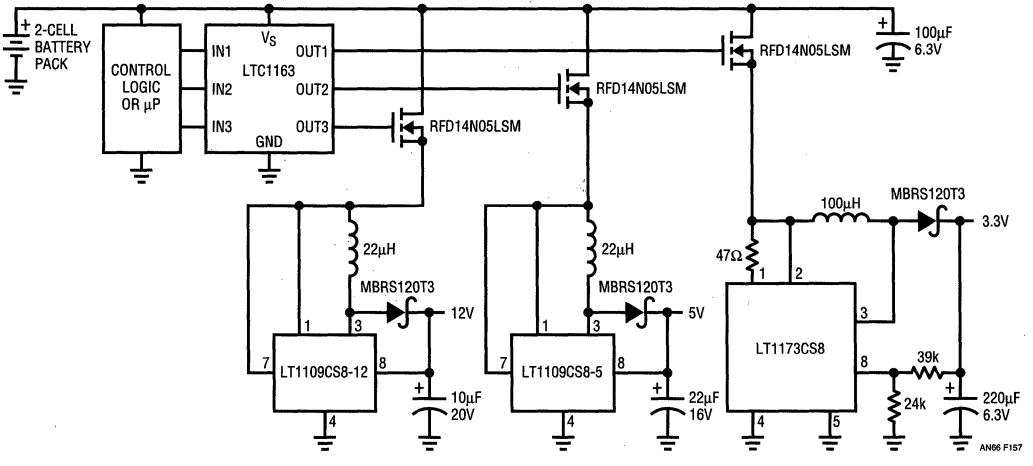


Figure 157. Complete 2-Cell to 3.3V, 5V and 12V Power Management System

LTC1157 SWITCH FOR 3.3V PC CARD POWER

by Tim Skovmand

Computers designed to accept PC cards—plug-in modules specified by the Personal Computer Memory Card International Association (PCMCIA)—have special hardware features to accommodate these pocket-sized cards. PCMCIA-compliant cards require power management electronics that conform to the height restrictions of the three standard configurations: 3.3mm, 5mm and 10.5mm. These height limitations dramatically reduce the available options for power management on the card itself. For example, high efficiency switching regulators to convert the incoming 5V down to 3.3V for the on-card 3.3V logic require relatively large magnetics and filter capacitors, which are not always available in packaging thin enough to meet the tight height requirements.

One possible approach to the problem of supplying power to a 3.3V PC card is to switch the input supply voltage from 5V to 3.3V after the card has been inserted and the attribute ROM has informed the computer of the card's voltage and current requirements. The switching regulator, housed in the computer, switches the power supplied to the connector from 5V to 3.3V.

A window comparator and ultralow drop switch on the PC card, Q1 in Figure 158, closes after the supply voltage drops from 5V to 3.3V, ensuring that the sensitive 3.3V logic on the card is never powered by more than 3.6V or less than 2.4V. A second switch, Q2, is provided on the card to interrupt power to 3.3V loads that can be idled when not in use.

The built-in charge pumps in the LTC1157 drive the gates of the low $R_{DS(ON)}$ N-channel MOSFETs to 8.7V when powered from a 3.3V supply. The LT1017 and the LTC1157 are both micropower and are supplied by a filter (R5 and C2) that holds the supply pins high long enough to ensure that the MOSFET gates are fully discharged immediately after the card is disconnected from the power supply. A large value bleed resistor, R6, further ensures that the high impedance gate of Q1 is not inadvertently charged up when the card is removed or when it is stored.

All of the components shown in Figure 158 are available in thin, surface mount packaging and occupy a very small amount of surface area. Further, the power dissipation is extremely low because the LTC1157 and LT1017 are micropower and the MOSFET switches are very low $R_{DS(ON)}$.

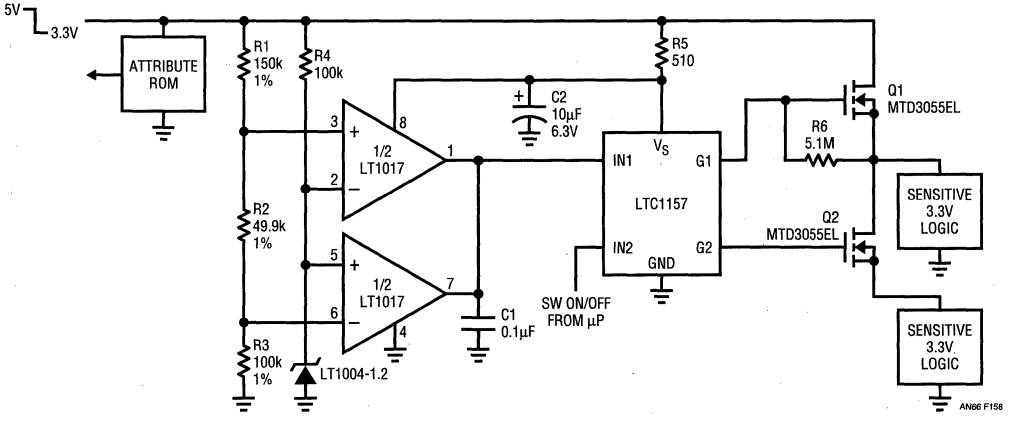


Figure 158. 3.3V PCMCIA Card Power Switching

THE LTC1157 DUAL 3.3V MICROPOWER MOSFET DRIVER

by Tim Skovmand

The LTC1157 dual micropower MOSFET driver makes it possible to switch either supply- or ground-referenced loads through a low $R_{DS(ON)}$ N-channel switch. The LTC1157's internal charge pump boosts the gate drive voltage 5.4V above the positive rail (8.7V above ground), fully enhancing a logic level, N-channel MOSFET for 3.3V high side switching applications.

LTC1157 Switches Two 3.3V Loads

Figure 159 illustrates how two surface mount MOSFETs and the LTC1157 (also available in SO-8 packaging) can be used to switch two 3.3V loads. The gate rise and fall times are typically in the tens of microseconds, but can be slowed by adding two resistors and a capacitor as shown on the second channel. Slower rise and fall times are sometimes required to reduce the start-up current demands of large supply capacitors which might otherwise glitch the main supply.

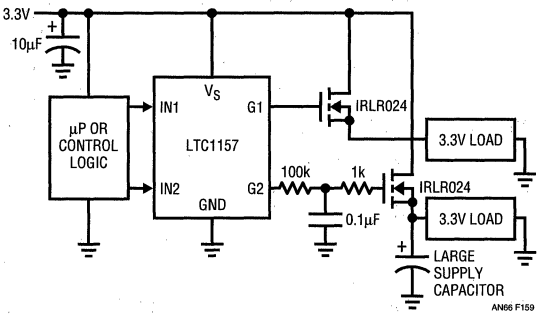


Figure 159. LTC1157 Used to Switch Two 3.3V Loads

THE LTC1155 DOES LAPTOP COMPUTER POWER BUS SWITCHING, SCSI TERMINATION POWER OR 5V/3A EXTREMELY LOW DROPOUT REGULATOR

by Tim Skovmand

The LTC1155 is a new micropower MOSFET driver specifically designed for low voltage, high efficiency switching applications such as those found in laptop or notebook computers. Three applications for this versatile part are detailed here.

Figure 160 is a schematic diagram that demonstrates the use of the LTC1155 for switching the power buses in a laptop computer system. The disk drive, display, printer and the microprocessor system itself are selectively engaged via high side switching with minimum loss and are shut down completely when not in use.

The quiescent current of the LTC1155 is designed to be extremely low in both the OFF and ON states, so that efficiency is preserved even when driving loads that require very little current to operate in standby, but require much larger peak currents when in operation. This combination of a low $R_{DS(ON)}$ MOSFET and an efficient driver delivers the maximum energy to the load.

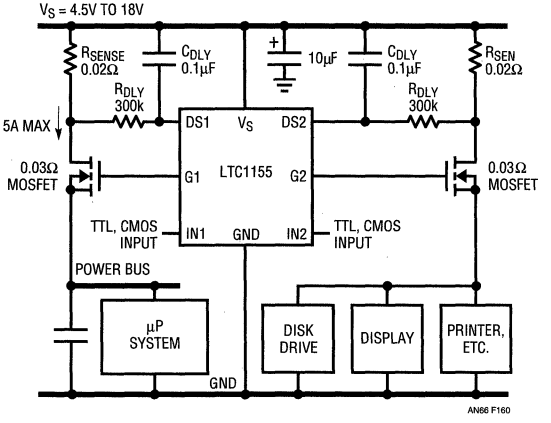


Figure 160. Laptop Computer Power Bus Switching

Protected SCSI Termination Power

The circuit shown in Figure 161 demonstrates how the LTC1155 provides protected power to SCSI terminators. The LTC1155 is initially triggered by the free-running 1Hz oscillator (it could also be triggered by a pulse from the microprocessor) and latches ON via the positive feedback

provided by R_{FB}. The power MOSFET gate is driven to 12V and the MOSFET is fully enhanced.

The delay afforded by the two delay components, R_{DLY} and C_{DLY}, ensures that the protection circuit is not triggered by a high inrush-current load. If, however, the source of the MOSFET is shorted to ground or if the output of LT1117 is shorted, the delay will be exceeded and the MOSFET will be held OFF until the pulse from the free-running oscillator resets the input again. The drain sense resistor, R_{SENSE}, is selected to trip the LTC1155 protection circuitry when the MOSFET current exceeds 1A. This current limit protects both the LT1117 and any peripheral system powered by the SCSI termination power line.

The delay time afforded by R_{DLY} and C_{DLY} is chosen to be considerably smaller than the reset time period (>100:1), so that very little power is dissipated while the short-circuit condition persists, i.e., the LTC1155 will deliver small pulses of current during every reset time period until the short-circuit condition is removed.

The LTC1155 and the LT1117, as well as the power MOSFET shown, are available in surface mount packaging and therefore consume very little board space.

Extremely Low Voltage Drop Regulator

An extremely low voltage drop regulator can be built around the LTC1155 and a low resistance power MOSFET as shown in Figure 162. The LTC1155 charge pump boosts the gate voltage above the supply rail and continuously charges a 0.1µF reservoir capacitor. The LT1431 works against this capacitor and the 100k series resistor to control the MOSFET gate voltage and maintain a constant 5V at the output.

The regulator is switched ON and OFF by the control logic or the microprocessor to conserve power in the standby mode. The LTC1155 standby current drops to about 10µA when the input is switched OFF. The total ON current, including the LT1431 is less than 1mA.

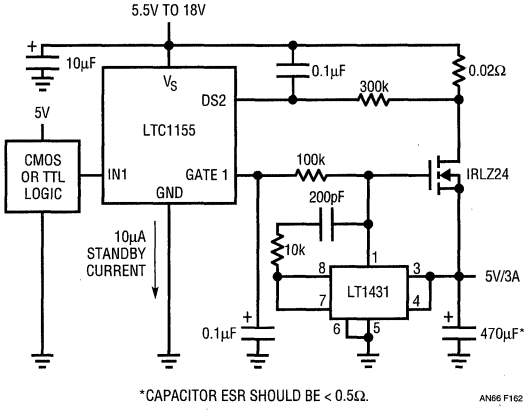


Figure 162. 5V/3A Extremely Low Voltage Drop Regulator

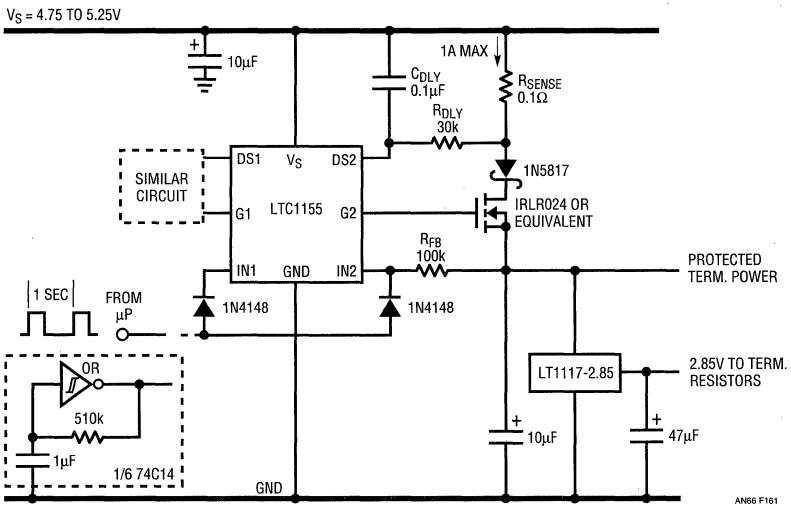


Figure 161. SCSI Termination Power with Short-Circuit Protection

A CIRCUIT THAT SMOOTHLY SWITCHES BETWEEN 3.3V AND 5V

by Doug La Porte

Many subsystems require supply switching between 3.3V and 5V to support both low power and high speed modes. This back-and-forth voltage switching can cause havoc to the main 3.3V and 5V supply buses. If done improperly, switching the subsystem from 5V to 3.3V can cause a momentary jump on the 3.3V bus, damaging other 3.3V devices. When switching the subsystem from 3.3V to 5V, the 5V supply bus can be pulled down while charging the subsystem's capacitors and may inadvertently cause a reset.

The circuit shown in Figure 163 allows smooth voltage switching between 3.3V and 5V with added protection features to ensure safe operation. IC1 is an LTC1470 switch-matrix device. This part has on-chip charge pumps running from the 5V supply to fully enhance the internal N-channel MOSFETs. The LTC1472 also has guaranteed break-before-make switching to prevent cross conduction between buses. It also features current limiting and thermal shutdown.

When switching the subsystem from 5V to 3.3V, the holding capacitor and the load capacitance are initially charged up to 5V. Connecting these capacitors directly to the main 3.3V bus causes a momentary step to 5V. This transient is so fast that the power supply cannot react in time. Switching power supplies have a particularly difficult time coping with this jump. Switching supplies source current to raise the supply voltage and require the load to sink current to lower the voltage. A switching supply will be unable to react to counter the large positive voltage step. This jump will cause damage to many low voltage devices.

The circuit in Figure 163 employs a comparator (IC2) and utilizes the high impedance state of the LTC1470 to allow switching with minimal effect on the supply. When the 3.3V output is selected, IC1's output will go into a high impedance state until its output falls below the 3.3V bus. The output capacitors will slowly discharge to 3.3V, with the rate of discharge depending on the current being pulled by the subsystem and the size of the holding capacitor. The example shown in Figure 163 is for a 250mA subsystem. The discharge time constant should be about 4ms. Once the subsystem supply has dropped below the 3.3V supply, the comparator will trip, turning on the 3.3V switch. The comparator has some hysteresis to avoid instabilities. The subsystem supply will reach a low point of about 3V before the 3.3V switch is fully enhanced.

When switching from 3.3V to 5V, IC1's current limiting prevents the main 5V bus from being dragged down while charging the holding capacitor and the subsystem's capacitance. Without current limiting, the inrush current to charge these capacitors could cause a droop in the main 5V supply.

If done improperly, supply voltage switching leads to disastrous system consequences. The voltage switch should monitor the output voltage and have current limiting to prevent main supply transient problems. A correctly designed supply voltage switch avoids the pitfalls and results in a safe, reliable system.

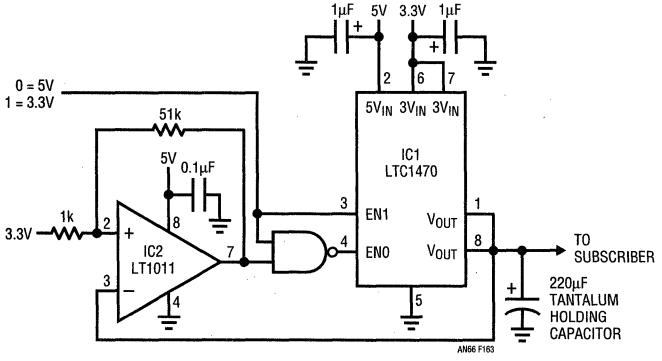


Figure 163. Schematic Diagram of 3.3V and 5V Switchover Circuit

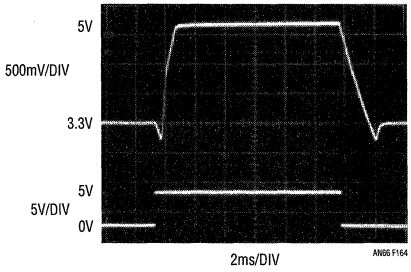


Figure 164. Oscillograph of the Switchover Waveform Showing Smooth Transitions

A FULLY ISOLATED QUAD 4A HIGH SIDE SWITCH

by Milton Wilcox

High side switching in hostile environments often requires isolation to protect the controlling logic from transients on the "dirty" power ground. The circuit shown in Figure 165 drives and protects four low $R_{DS(ON)}$ power MOSFET switches over a wide operating supply range. The LT1161 drivers are protected from transients of up to 60V on the supply pins and 75V on the gate pins. Fault indication is provided by an inexpensive logic gate.

Each of the four LT1161 switch channels has a completely self-contained charge pump, which drives the gate of the N-channel MOSFET switch 12V above the supply rail when the corresponding Input pin is taken high. The specified MOSFET device types have a maximum $R_{DS(ON)}$ of 0.028Ω, resulting in a total switch drop (including sense resistor) of only 0.15V at 4A output current.

The LT1161 independently protects and restarts each MOSFET. It senses drain current via the voltage drop across a current shunt R_S. When the current in one switch exceeds approximately 6A (62mV/0.01Ω) the switch is turned off without affecting the other switches. The switch remains off for 50ms (set by external timing capacitor C_T), after which the LT1161 automatically attempts to restart it. If the fault is still present this cycle repeats until the fault is removed, thus protecting the MOSFET. Current shunts are readily available in both through-hole and surface mount case styles. AN53 has additional information on shunts. Connect the LT1161 V^+ pins directly to the top of the current shunts (see LT1161 data sheet).

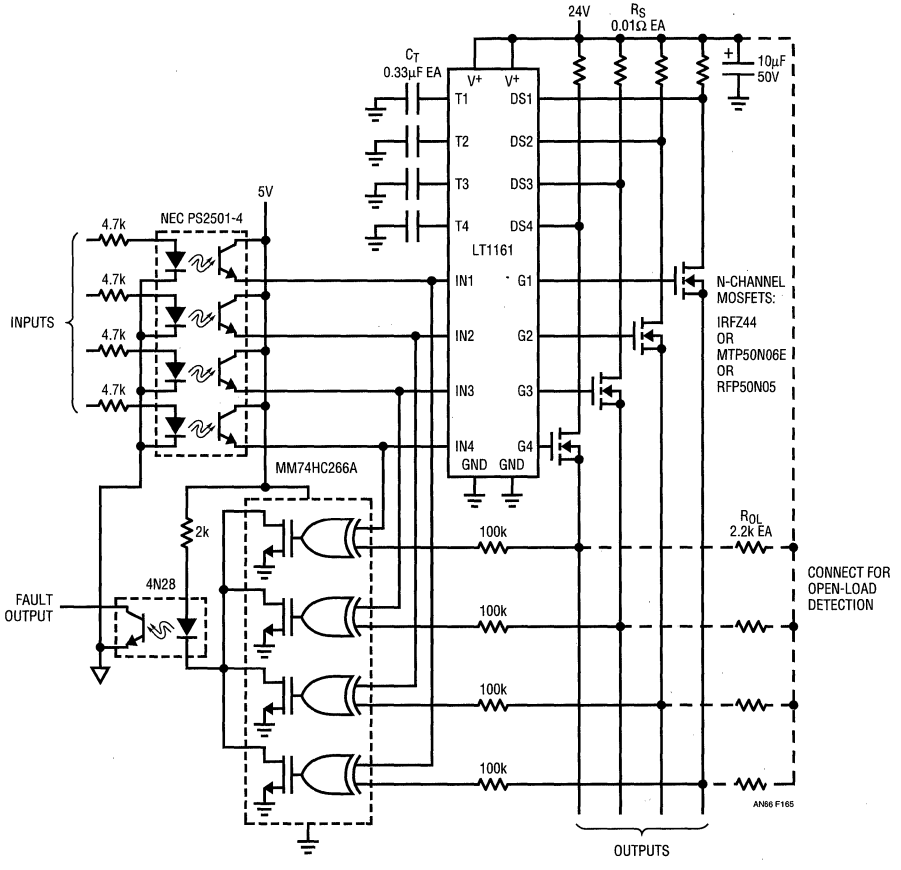


Figure 165. Protected Quad High Side Switch Has Isolated Inputs and Fault Output

The highest MOSFET dissipation occurs with a "soft short" (one in which the current is above the normal operating level but still below the current limit threshold). This can cause dissipation in Figure 165's circuit to rise, in the worst-case to 2W, requiring modest heatsinking. When an output is directly shorted to ground the average dissipation is very low because the MOSFET conducts only during brief restart attempts.

Fault indication is provided by a low cost exclusive NOR gate. In normal operation a low on the LT1161 input forces a low on the output and a high forces a high. If an input is high and the corresponding output is low (i.e., short circuited), the output of the exclusive NOR gate activates the isolated fault output. Similarly, by adding resistor R_{OL} the low input/high output state can be used to diagnose an open load condition. Adjusting the value of R_{OL} sets the output current at which the load is considered to be open. For example, in Figure 165 with V_{SUPPLY} = 24V, a fault would be indicated if the load could not sink 10mA.

Figure 165's circuit is ideal for driving resistive or inductive loads such as solenoids. However, the circuit can be tailored for capacitive or high inrush loads as well. Consult the LT1161 data sheet for information on programming current limit, delay time and automatic restart period to handle other loads. The LT1161 is available in both PDIP and surface mount packaging.

THE LTC1153 ELECTRONIC CIRCUIT BREAKER

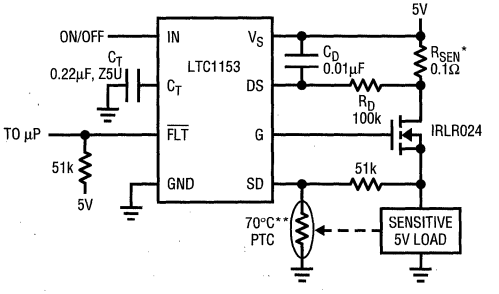
by Tim Skovmand

The LTC1153 electronic circuit breaker is designed to work with a low cost, N-channel power MOSFET to interrupt power to a sensitive electronic load in the event of an overcurrent condition. The breaker is tripped by an overcurrent condition and remains tripped for a period of time programmed by an external timing capacitor, C_T. The switch is then automatically reset and the load momentarily retried. If the load current is still too high, the switch is shut down again. This cycle continues until the overcurrent condition is removed, thereby protecting the sensitive load and the power MOSFET.

5V/1A Circuit Breaker with Thermal Shutdown

The trip current, trip-delay time and autoreset period are programmable over a wide range to accommodate a variety of load impedances. Figure 166 demonstrates how the LTC1153 is used in a typical circuit breaker application. The DC trip current is set by a small valued resistor, R_{SEN}, in series with the drain lead, which drops 100mV when the current limit is reached. In the circuit of Figure 166, the DC trip current is set at 1A (R_{SEN} = 0.1Ω).

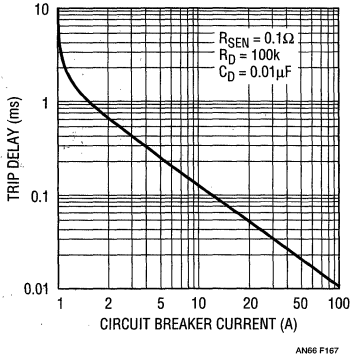
The trip-delay time is set by the two delay components, R_D and C_D, which establish an RC time constant in series with the drain sense resistor, producing a trip delay that is shorter for increasing breaker current (similar to that of a mechanical circuit breaker). Figure 167 is a graph of the trip-delay time versus the circuit breaker current for a 1ms



* ALL COMPONENTS SHOWN ARE SURFACE MOUNT.
** IMS026 INTERNATIONAL MANUFACTURING SERVICE, INC. (401) 683-9700
RL2006-100-70-30-PT1 KEYSTONE CARBON COMPANY (814) 781-1591

AN67 F166

Figure 166. LTC1153 5V/1A Circuit Breaker with Thermal Shutdown



AN66 F167

Figure 167. Trip Delay Time vs Circuit Breaker Current (1ms RC Time Constant for the Circuit of Figure 166)

RC time constant. Note that the trip time is 0.63ms at 2A, but falls to 55µs at 20A. This characteristic ensures that the load and the MOSFET switch are protected against a wide range of overload conditions.

The autoreset time is typically set in the range of 10s of milliseconds to a few seconds by selecting the timing capacitor, C_T. The autoreset period for the circuit in Figure 190 is 200ms, i.e., the circuit breaker is automatically reset (retried) every 200ms until the overload condition is removed.

An open-drain fault output is provided to warn the host microprocessor whenever the circuit breaker has been tripped. The microprocessor can either wait for the autoreset function to reset the load, or shut the switch OFF after a fixed number of retries.

The shutdown input interfaces directly with a PTC thermistor to sense overtemperature conditions and trip the circuit breaker whenever the load temperature or the MOSFET switch temperature exceeds a safe level. The thermistor shown in Figure 166 trips the circuit breaker when the load temperature exceeds approximately 70°C.

LTC1153: DC Motor Protector

A 5V DC motor can be powered and protected using the circuit shown in Figure 168. The DC current delivered to the motor is limited to 5A and a rather long trip delay is used to ensure that the motor starts properly. The motor temperature is also continuously monitored and the breaker is tripped if the motor temperature exceeds 70°C. The fault output of the LTC1153 informs the host microprocessor whenever the breaker is tripped. The microprocessor can disable the motor if a set number of faults occur or it can initiate a retry after a much longer period of time has elapsed. A rectifier diode across the motor returns the motor current to ground and restricts the output of the switch to less than 1V below ground.

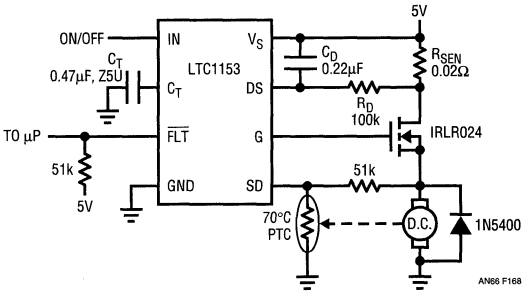


Figure 168. DC Motor Driver with Overcurrent and Overtemperature Protection

LTC1477: 0.07Ω PROTECTED HIGH SIDE SWITCH ELIMINATES "HOT SWAP" GLITCHING

by Tim Skovmand

When a printed circuit board is "hot swapped" into a live 5V socket, a number of bad things can happen.

First, the instantaneous connection of a large, discharged supply bypass capacitor may cause a glitch to appear on the power bus. The current flowing into the capacitor is limited only by the socket resistance, the card trace resistance, and the equivalent series resistance (ESR) of the supply bypass capacitor. This supply glitch can create real havoc if the other boards in the system have power-on RESET circuitry with thresholds set at 4.65V.

Second, the card itself may be damaged due to the large inrush of current into the card. This current is sometimes inadvertently diverted to sensitive (and expensive) integrated circuits that cannot tolerate either overvoltage or overcurrent conditions even for short periods of time.

Third, if the card is removed and then reinserted in a few milliseconds, the glitching of the supply may "confuse" the microprocessor or peripheral ICs on the card, generating erroneous data in memory or forcing the card into an inappropriate state.

Fourth, a card may be shorted, and insertion may either grossly glitch the 5V supply or cause severe physical damage to the card.

Figure 169 is a schematic diagram showing how an LTC1477 protected high side switch and an LTC699 power-on RESET circuit reduce the chance of glitching or damaging the socket or card during "hot swapping."

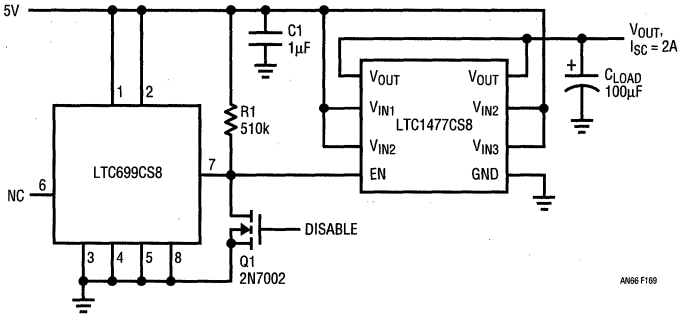


Figure 169. "Hot Swap" Circuit Featuring LTC1477 and LTC699

The LTC1477 protected high side switch provides extremely low $R_{DS(ON)}$ switching (typically 0.07Ω) with built-in 2A current limiting and thermal shutdown, all in an 8-pin SO package.

As the card is inserted, the LTC699 power-on RESET circuit holds the Enable pin of the LTC1477 low for approximately 200ms. When the Enable pin is asserted high, the output is ramped on in approximately 1ms. Even if a very large supply bypass capacitor (for example, over 100µF) is used, the LTC1477 will limit the inrush current to 2A and ramp the capacitor at an even slower rate. Further, the board is protected against short-circuit conditions by limiting the switch current to 2A.

The 5V card supply can be disabled via Q1. The only current flowing is the standby quiescent current of the LTC1477, which drops below 1µA, the 600µA quiescent current of the LTC699 and the 10µA consumed by R1.

Miscellaneous

PROTECTED BIAS FOR GaAs POWER AMPLIFERS

by Mitchell Lee

Portable communications devices such as cellular telephones and answer-back pagers rely on small GaAsFET-based 0.1W to 1.0W RF amplifiers as the transmitter output stage. The main power device requires a negative gate bias supply, which is not readily available in a battery-operated product. The circuit shown in Figure 170 not only develops a regulated negative gate bias, it also switches the positive supply, protects against the loss of gate bias, limits power dissipation in the amplifier under high standing-wave ratio (SWR) conditions and protects against amplifier failures that might otherwise short circuit the battery pack.

Negative bias is supplied by an LTC1044 charge pump inverter and the amplifier's positive supply is switched by an LTC1153 electronic circuit breaker. An open-collector switch can be used to turn the LTC1044 inverter off by grounding the OSC pin (Pin 7). When off the LTC1044 draws only 2µA.

The negative output from the LTC1044 is sensed by a 2.5V reference diode (IC2) and Q2. With no negative bias available, Q2 is off and Q3 turns on, pulling the LTC1153's control input low. This shuts off the GaAs amplifier. Total standby power, including the LTC1044, is approximately 25µA.

If the LTC1044's OSC pin (Pin 7) is released, a negative output nearly equal in magnitude to the battery input voltage appears at V_{OUT} (Pin 5). The negative bias is regulated by R1, IC2 and Q2's base-emitter junction. Q2 saturates, shutting Q3 off and thereby turning the LTC1153 on.

The LTC1153 charges the N-channel MOSFET (Q4) gate to 10V above the battery potential, switching Q4 fully on. Power is thus applied to the GaAs amplifier.

The nominal negative bias is –3.2V, comfortably assuring the –2.5V minimum specified for the amplifier. Total

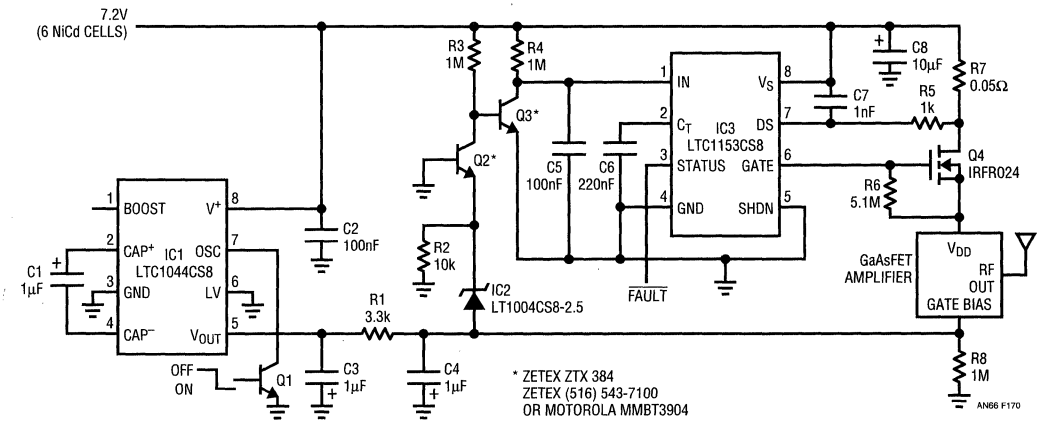


Figure 170. Schematic Diagram

quiescent current, exclusive of the GaAs amplifier drain supply, is approximately 1.5mA in the ON state.

Short circuits or overcurrent conditions in the GaAs amplifier can damage the circuit board, the batteries or both. The LTC1153 senses the amplifier's supply current and turns Q4 off if it is over 2A. After a timeout period set by C6 (200ms) the LTC1153 tries again, turning Q4 on. If the amplifier's supply current is still too high the LTC1153 trips off again. This cycle continues until the fault condition is cleared. Under fault conditions the LTC1153's Status pin (Pin 3) is low. As soon as the fault is cleared the LTC1153 resets and normal operation is restored.

LT1158 H-BRIDGE USES GROUND REFERENCED CURRENT SENSING FOR SYSTEM PROTECTION

by Peter Schwartz

The LT1158 half-bridge motor driver incorporates a number of powerful protection features. Some of these, such as its adaptive gate drive, are dedicated in function. Others are open to a variety of uses depending upon application requirements. The circuit shown in Figure 171 takes advantage of the wide common mode input range of the LT1158's fault comparator to perform ground referenced current sensing in an H-bridge motor driver. By using ground referenced sensing, protection can easily be provided against overloaded, stalled or shorted motors. For overloads and stalls the circuit becomes a constant current chopper, regulating the motor's armature current to a preset maximum value. For shorted loads the circuit protects itself by operating at a very low duty cycle until the short is cleared.

Setting Up for Ground Referenced Sensing

The circuit of Figure 171 is essentially a straightforward LT1158 H-bridge of the "sign/magnitude" type. (See the LT1158 data sheet for a description of component functions.) In many LT1158 applications, a current sense resistor is placed in each upper MOSFET source lead. This circuit, however, senses the IR drop across one resistor (R1) common to the sources of both lower MOSFETs. In Figure 171, U1's $\overline{\text{FAULT}}$ output activates the constant current protection mode (for overloads and stalls) and U2's $\overline{\text{FAULT}}$ output indicates a shorted load. Hence, given a maximum continuous motor current of 15A, R1's value is easily determined: V_{SENSE+} of U1 must exceed V_{SENSE-} by the LT1158's internal threshold of 110mV in order for $\overline{\text{FAULT}}$ to go low. 15A • R1 = 0.110V, so R1 = (0.110V/15A) at 0.0075Ω. The $\overline{\text{FAULT}}$ pin of U2 should go low when I_{R1} is 24A, so a 1.6:1 voltage divider is added at U2's Sense+ input. R2, R3, C1 and C2 filter any switching spikes that appear across R1.

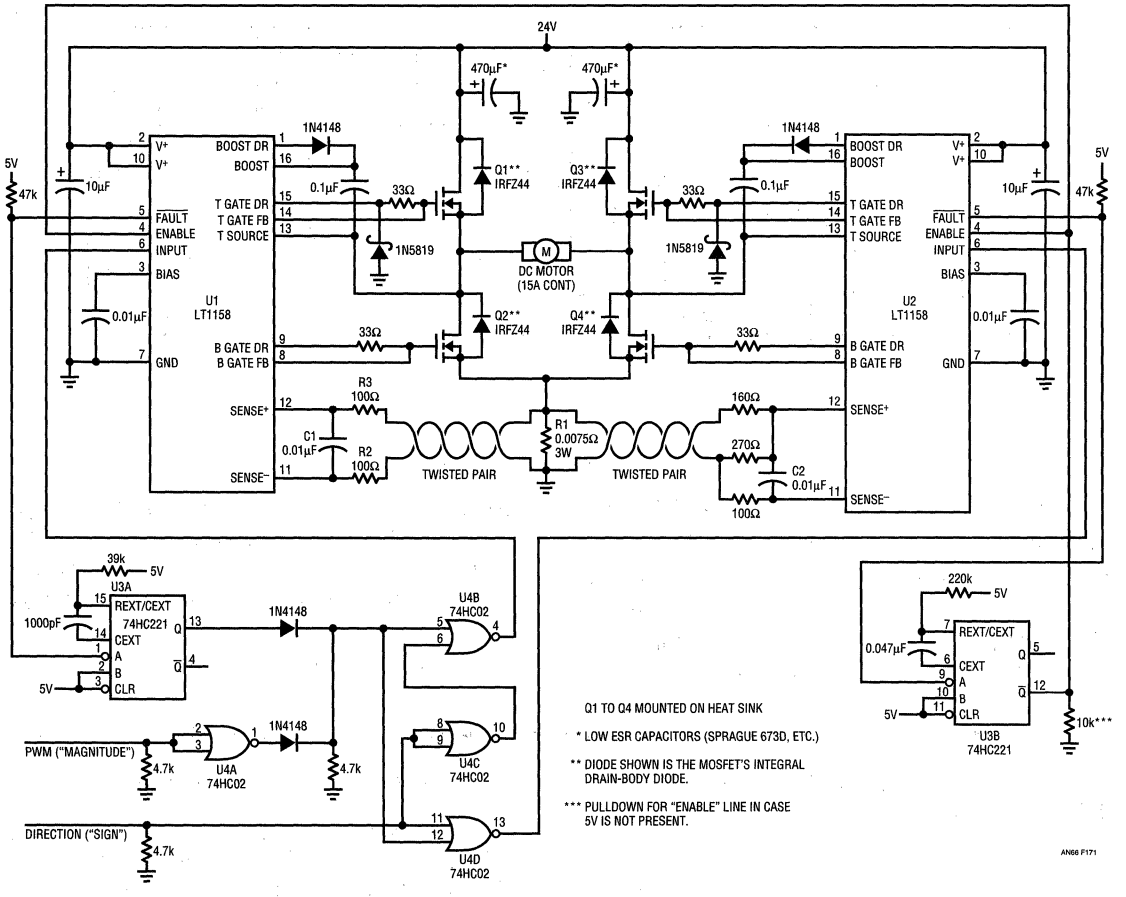


Figure 171. H-Bridge Motor Driver with Ground Referenced Current Sensing

Closing the Loop on Overloads

If the motor is overloaded or stalled, its back EMF will drop, causing the armature current to increase at a rate determined primarily by the motor's inductance. Without protection this current could rise to a value limited only by supply voltage and circuit resistance. The necessary protection is provided via the feedback loop formed by U1's $\overline{\text{FAULT}}$ output, U3A, U4B and U4D. When I_{R1} exceeds 15A, the $\overline{\text{FAULT}}$ pin of U1 conducts, triggering the 40µs monostable U3A. The Q output of U3A in turn forces the outputs of U4B and U4D to a logic low state, turning off Q1 or Q3, and turning on both Q2 and Q4. For the time during which U3A's Q output is high, the motor current decays through the path formed by the motor's resistance, plus the on-resistance of Q2 and Q4 in series. In this application, turning both lower MOSFETs on is preferable to forcing all four MOSFETs off, as it provides a low resistance recirculation path for the motor current. This reduces motor and supply ripple currents, as well as MOSFET dissipation. At the end of U3A's 40ms timeout the H-bridge turns on again. If the overload still exists, the current quickly builds up to the U1 $\overline{\text{FAULT}}$ trip point again and the 40ms timeout repeats. This feedback loop holds the motor current approximately constant at 15A for any combination of supply voltage and duty cycle that would otherwise cause an excess current condition. When the motor's current draw falls below 15A, the circuit resumes normal operation.

Opening the Loop on Shorts

In the event of a short across the motor terminals the current through the H-bridge rises faster than the U1/U3A loop can regulate it. This could easily exceed the safe operating area limits of the MOSFETs. The solution is simple: when the fault comparator of U2 detects that $I_{R1} \geq$ 24A, monostable U3B is triggered. The $\overline{Q}$ output of U3B will then hold the enable line of the two LT1158s low for 10ms, resulting in a rapid shutdown and a very low duty cycle. After the 10ms shutdown interval, U3B's $\overline{Q}$ output will return high and the bridge will be reenabled. If the motor remains shorted, U3B is triggered again, causing another 10ms shutdown. When the short is cleared, circuit operation returns to that described above.

A Final Note

As a class, sign/magnitude H-bridge systems are susceptible to MOSFET and/or motor damage if the motor velocity is accelerated rapidly, or the state of the DIRECTION line is switched while the motor is rotating. This is especially true if the motor/load system has high inertia. The circuit of Figure 171 is designed to provide protection under these conditions: the motor may be commanded to accelerate and to change direction with no precautions. For the case of deceleration, however, it's generally best to use a controlled velocity profile. If a specific application requires the ability to operate with no restrictions upon the rate of change of duty cycle, there are straightforward modifications to Figure 171 that allow this. Please contact the factory for more information.

LT1158 ALLOWS EASY 10A LOCKED ANTIPHASE MOTOR CONTROL

by Milton Wilcox

Allowing synchronous control of two N-channel power MOSFETs operating from 5V to 30V, the LT1158 half-bridge driver effectively deals with the many problems and pitfalls encountered in the design of high efficiency motor control and switching regulator circuits.

Figures 172a and 172b illustrate a locked antiphase motor drive in which the motor stops if either side is shorted to ground (since a 50% input duty cycle is used to stop the motor in locked antiphase operation, the motor would

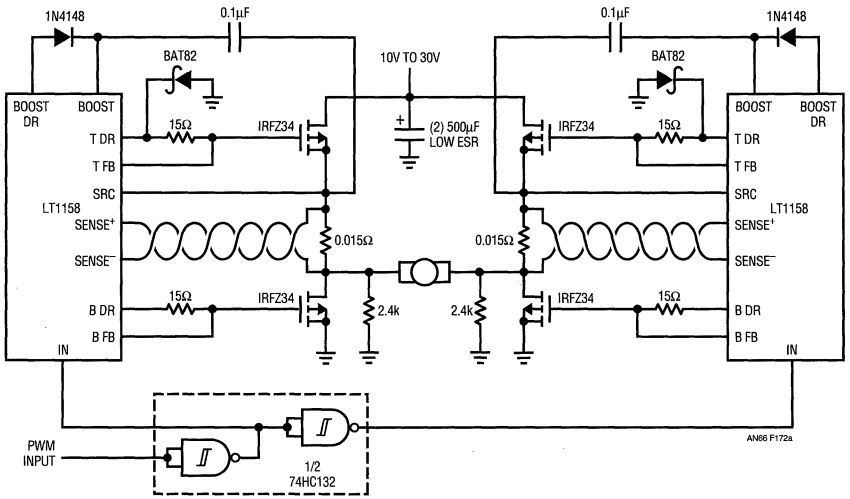


Figure 172a. 10A Locked Antiphase Full-Bridge Circuit Operates Over Wide Supply Range

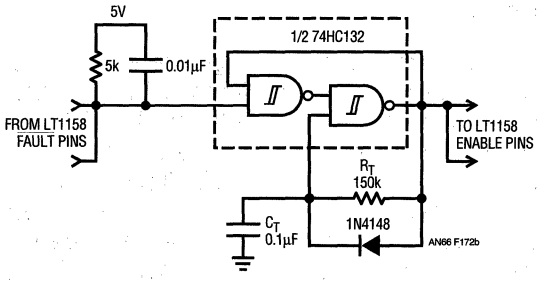


Figure 172b. Protection Logic Stops Motor if Either Side Is Shorted to Ground

normally accelerate to half speed with one side shorted). When a fault is detected by either LT1158, the Figure 172b latch is set, disabling both LT1158s. The circuit periodically tries restarting the motor at a time interval determined by R_T and C_T. If the short still exists, the disabled state is resumed within 20µs, far too short a time to move the motor.

The LT1158 can be used with virtually any N-channel power MOSFET, including 5-lead current sensing MOSFETs. This configuration offers the benefit of no-loss current sensing, since a current shunt is no longer needed in the source. In addition, R_{SENSE} increases by a factor of 1000 or more: from milliohms to ohms. The LT1158 can also be used with logic level MOSFETs for operation as low as 4.5V if a Schottky boost diode is used and connected directly to the supply.

The LT1158 N-channel power MOSFET driver anticipates all of the major pitfalls associated with the design of high efficiency bridge circuits. The designed-in ruggedness and numerous protection features make the LT1158 the best solution for 5V to 30V medium-to-high current synchronous switching applications.

ALL SURFACE MOUNT PROGRAMMABLE 0V, 3.3V, 5V AND 12V VPP GENERATOR FOR PCMCIA

by Jon A. Dutra

Generating the VPP voltage for a PCMCIA port in laptop computers has become more complicated with PCMCIA standard 2.0. The VPP line must come up to 5V initially until the card "tuple" tells the card its type and VPP voltage. For example, a 3.3V SRAM card must have VPP adjusted to 3.3V. If it is a flash memory card, 12V must be supplied during programming. During card insertion, 0V is desirable to unconditionally prevent latch-up. Shutdown supply current must be as low as possible and the supply must not overshoot. This design idea presents a circuit (Figure 173) that meets these specifications. The same topology could be useful for generating other programmable supplies.

The circuit uses the LT1107 micropower DC/DC converter with a single surface mount transformer. The LT1107 features an I_{LIM} pin that enables direct control of maximum inductor current. This allows use of a smaller transformer without risk of saturation. The LT1111 could also be used with a reduction in output power.

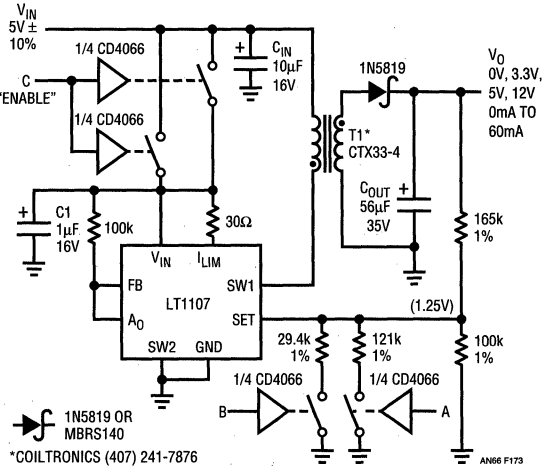


Figure 173. Schematic Diagram for VPP Generator

Circuit Operation

The circuit is basically a gated-oscillator flyback topology. The SET pin of the LT1107 is held at 1.25V by negative feedback. Summing currents into the SET pin to zero for the three different output states yields three equations with three unknown resistor values. The resistor values are easily solved for using Mathametica, MathCad or classical techniques. Table 1 shows the output voltage truth table.

Table 1

INPUTS			OUTPUTS	
A	B	ENABLE	V_O	NOTE
X	X	0	0V	Off
1	1	1	12V	12V
1	0	1	5V	5V
0	1	1	10.3V	Not Used
0	0	1	3.3V	3.3V

Output noise is reduced by using the auxiliary gain block (AGB) in the feedback path. This added gain effectively reduces the hysteresis of the comparator and tends to randomize output noise. With a low ESR capacitor for C1, output noise is below 30mV over the output load range.

Output power increases with $V_{BATTERY}$ from about 1.4W out with 5V in to about 2W out with 8V or more. Efficiency is 62% to 76% over a broad output power range. No minimum load is required.

Component Selection

Substantial current flows through C_{IN} and C_{OUT}. Most tantalum capacitors are not rated for current flow and can result in field failures. Using a rated tantalum or rated electrolytic will result in longer system life.

Shutdown

The circuit is shut down by using two sections of the CD4066 in parallel as a high side switch. Alternatively, simply disabling the logic supply to the V_{IN} and I_{LIM} nodes of the LT1107 will shut it down. This drops quiescent current from the $V_{BATTERY}$ input below 2μA. When the device is shut down V_{OUT} drops to 0V.

A TACHLESS MOTOR SPEED REGULATOR

by Mitchell Lee

A common requirement in many motor applications is a means of maintaining constant speed with variable loading or variable supply voltage. Speed control is easily implemented using tachometer feedback, but the cost of a tach may be prohibitive in many situations and adds mechanical complications to the product. A lower cost solution with no moving parts is presented here.

Motor speed changes under conditions of varying loads because of the effects of series loss terms in the motor. The effects of the predominant contributors to loss, copper and brush/commutator resistance (collectively known as R_M), are best understood by considering the circuit model for a motor (see Figure 174). A motor's back EMF (V_M) is proportional to speed (n) and the motor current (I_M) is proportional to the load torque (T). The following equation predicts the speed of the motor for any given condition of loading:

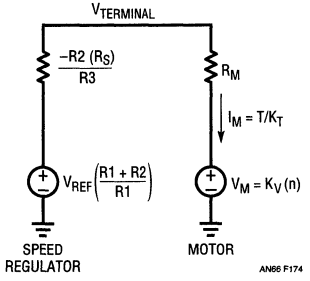


Figure 174. On the Right is Shown an Equivalent Circuit for a Motor. On the Left is the Model for a Circuit Which Will Stablize the Motor's Speed Against Changes in Supply Voltage and Loading

$$n = \frac{V_{TERMINAL}}{K_V} - T\left(\frac{R_M}{(K_T)(K_V)}\right) \quad (1)$$

where K_V and K_T are constants of proportionality for rotational velocity and torque. For a fixed terminal voltage, the speed of the motor must decrease as increasing load

torque is applied to the shaft. For a fixed load, the speed of the motor will also change if the supply (terminal) voltage is changed.

A voltage regulator fixes the problem of a varying terminal voltage, but the only way to eliminate torque from Equation (1) is by reducing R_M to zero. Physically this is impractical, but an electrical solution exists.

If a motor is driven from a regulated source whose output impedance is opposite in sign and equal in magnitude to R_M (see Figure 174), the result is a motor that runs at a constant speed—regardless of loading and power source variations. Figure 175 shows a circuit that does it all. The LT1170 is configured as a buck/boost converter, which can take a wide ranging 3V to 20V input source and produce a regulated output of, say, 6V. The circuit shown can deliver 1A at 6V with a 5V input, adequate for many small permanent-magnet DC motors.

To cancel the effects of the motor resistance, a negative output impedance is introduced with an op amp and a current sense resistor (R_S). As the motor current increases, the LT1006 responds by increasing the motor terminal voltage by an amount equal to $(I_M)(R_M)$. Depending on the value of R3, the speed can be made to increase, decrease or stay the same under load. If R3 is just right, the motor speed will remain constant until the LT1170 reaches full power and the circuit runs out of steam.

Many small motors in the 1W to 10W class are not well characterized. In order to choose proper component values for a given motor, figures for R_M and V_M are necessary. Fortunately, these are easily measured using a DVM and a motor characterization test stand. If you don't have a motor characterization test stand, it is also possible to use a lathe or drill press to do the job.

Chuck up the candidate motor's shaft in a variable speed drill press or lathe, which is set to run at the same speed you're intending to operate the motor. Clamp down the motor frame so it won't spin. Turn on the big machine, and measure the open-circuit motor terminals with a DVM. This is the motor voltage, V_M, as shown in Figure 174. Switch the meter to measure the motor's short circuit current, I_{SC}. Motor resistance $R_M = V_M/I_{SC}$. With these figures the other component values can be calculated:

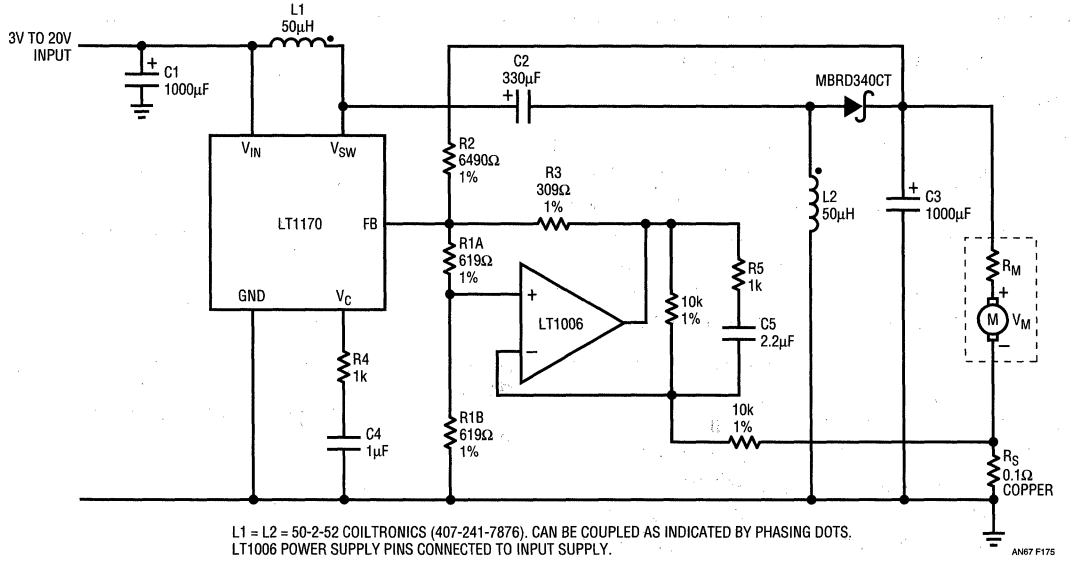


Figure 175. Tachless Motor Speed Regulator

I_{MAX} = motor current at full load

V_{REF} = 1.244V

R1 = series combination of 619Ω + 619Ω = 1238Ω

$R_S \leq 1/I_{MAX}$ (drops less than 1V at maximum load)

$$R2 = (V_M \bullet R1/V_{REF}) - R1 \quad (2)$$

$$R3 = (R2 \bullet R_S)/(R_M + R_S) \quad (3)$$

The component values shown in Figure 175 are for a small motor with the following characteristics measured at 360RPM: V_M = 7.8V, I_{SC} = 3.7A, R_M = 2.1Ω, $I_{MAX} \approx$ 1A.

R_S, a copper resistor, is either located close to or wound around the motor to assist in tracking changes in armature resistance with temperature. Copper has a strong, 3930ppm/°C temperature coefficient, matching the TC of the motor winding.

Setup Procedure

Initial tests should be performed with a potentiometer in place of, and twice the value of, R3. R5 and C5 should be disconnected; remove all loading from the motor. Check the motor's unloaded speed, and adjust R2 if necessary to set it precisely.

With the motor driving a nominal load, decrease R3 until the motor commences "hunting." R3 will be near the nominal calculated value. This threshold is very close to optimum motor resistance cancellation. R5 and C5 offer a convenient means of compensating for frictional and inertial effects in the mechanical system, eliminating instabilities. System stability should be evaluated under a variety of loading conditions. The effect of R5 is to reduce the negative output impedance of the circuit at high frequencies. Systems with a net positive impedance are inherently stable.

When the system stability is satisfactory, a final adjustment of R3 can be made to achieve the desired speed regulation under conditions of varying loads. These final values can be used in production. Note that R2 defines the regulated speed value and may be production trimmed in precision applications.

LT1161: ... AND BACK AND STOP AND FORWARD AND REST —ALL WITH NO WORRIES AT ALL

by Peter Schwartz and Milt Wilcox

Many applications of DC motors require not only the ability to turn the motor on and off, but also to control its direction of rotation. When directional control is involved, the need for rapid deceleration (electronic braking) can also be assumed. A microcontroller interface (logic-level control) is a necessity in modern systems, as is protection of both the motor controller and the motor itself. With the advent of high power, logic-level N-channel MOSFETs, it is a straightforward matter to build the lower half of an H-bridge suitable for the versatile control of DC motor loads. Equivalent performance P-channel MOSFETs, however, are still expensive devices of limited availability, even without logic-level capability. Therefore, motor control circuits commonly use N-channel devices for the upper half of the H-bridge as well. The trick is to do this without requiring an additional power supply to provide bias for the upper MOSFET gates, while ensuring the necessary system protections.

A Complete, Six-Part Plan

The circuit shown in Figure 176 is a complete H-bridge motor driver, with six distinct modes of operation:

- Motor Forward Rotation—In this mode, Q1 and Q4 are on, and Q2 and Q3 are off.
- Motor Reverse Rotation—In this mode, Q2 and Q3 are on, and Q1 and Q4 are off.
- Motor Stop—Here, a rapid stop is performed by using "plugging braking," wherein the motor acts as a generator to dissipate mechanical energy as heat in the braking circuit's resistance.
- Motor Idle—All four MOSFETs are turned off. The motor is, in effect, disconnected from the H-bridge driver.
- Load Protect—If the motor is overloaded or stalled for an excessive period, the on-chip fault detection and protection circuitry of the LT1161 will shut the motor off for programmed interval, then turn it back on.

❑ Short-Circuit Protect—If a source-to-ground short is detected on either Q1 or Q2, the on-chip fault detection and protection circuitry of the LT1161 will shut off the MOSFET at risk for the programmed interval and then attempt to turn the circuit back on.

Figure 176 shows a straightforward H-bridge using four N-channel MOSFETs (Q1 to Q4). The lower MOSFETs (Q3 and Q4) are logic-level devices to allow direct drive from 5V logic. The upper MOSFETs (Q1 and Q2) are driven via level translation circuitry integral to the LT1161. Input 1 of the LT1161 controls a charge pump in the IC, whose output is developed on Gate 1. Similarly, Input 2 controls a charge pump whose output is available on Gate 2. The Gate outputs have voltage swings from 0V to (V_{CC} + 12V), which is more than sufficient to enhance a standard threshold N-channel MOSFET, such as the IRFZ34. D3 is added to Q1 as a gate-source protection diode to prevent excessive voltage from appearing across the gate-source terminals of Q1. This could otherwise happen under certain conditions of "motor-idle" operation. D4 serves the same function for Q2.

The Logic Behind It All

The logic of the circuit is straightforward and could be replaced by a microcontroller in many applications. CMOS inverters U1 and U2 drive the lower MOSFETs directly from a 5V supply, with the RCD networks on their inputs providing the necessary timing to prevent shoot-through currents in the MOSFET switches. Inverter U3 and NOR gate U5 work together to turn Gate 1 and hence Q1 on when point A is at a logical high. This also ensures that C3 is charged to a logical high to take U2's output low and turn Q3 off. Under these conditions, with point B low (or left floating), U1 will turn Q4 on and U6 will hold Gate 2 and hence Q2 off. If point A is now immediately taken low (or left floating), and point B is taken high, the symmetry of the

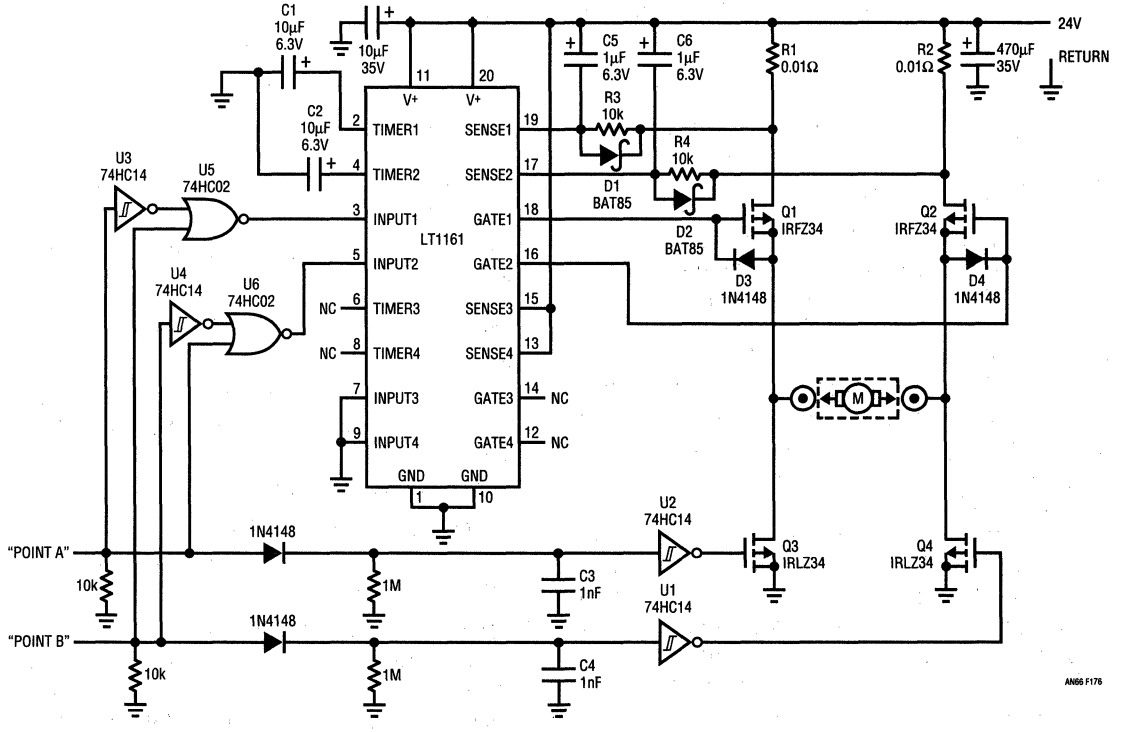


Figure 176. LT1161-Based H-Bridge Motor Driver Schematic Diagram

logic will reverse these conditions—but only after C3 has discharged to the point where the output of U2 can go high to turn Q3 on. This is the shoot-through prevention mentioned previously.

There are two exceptions to the symmetry of the logic: if both point A and point B are low, both upper MOSFETs are turned off while both lower MOSFETs are turned on. Under these conditions, the kinetic energy stored in the motor and its load is used to drive the motor as a generator. This produces a current through the motor winding, Q3 and Q4. In this "plugging braking" mode, the motor's energy is largely dissipated as I^2R losses and a rapid stop occurs. If point A and point B are both high, all four MOSFETs will be turned off and the motor is essentially disconnected from the electrical circuit. Although primarily included as a cross-conduction interlock in the event that both inputs should ever be high at the same time (things do happen on the test bench), this can also be useful in situations where it is desirable that the motor coast down from a higher velocity to a lower one.

Just a Few Grams... But Lots of Protection

In addition to its level translation and charge pump features, the LT1161 also provides comprehensive protection features via its Sense 1 and Sense 2 pins. Each Sense pin is the (–) input to an on-chip comparator, with the (+) input to that driver's comparator fixed at a level 65mV (nominal, 50mV minimum) below the LT1161's V^+ input. If a Sense pin goes more than 65mV below V^+, several things happen: the corresponding Gate output is rapidly pulled to ground, the capacitor on the Timer pin is dumped to ground and the charge pump is shut off. The charge pump will remain shut off, and the Gate pin will remain clamped to ground until the Timer capacitor has charged back up to 3V from an on-chip 14μA current source. When the capacitor reaches this 3V threshold, the internal charge pump starts up again and the clamp from the Gate pin to ground is removed. The net effect of this is that, if one of the Sense pins is pulled 65mV below V^+, the MOSFET turns off for a period that is set by the value of the capacitor connected to the Timer pin. At the end of this programmed interval the circuit will automatically restart. If the fault has been cleared, the protection circuitry then becomes transparent to the system. This shutdown/retry cycle will repeat until the fault is cleared.

The fault scenarios for which protection is required are, as mentioned above, an overloaded or stalled motor or a source-to-ground short on Q1 or Q2. In each case such a fault will cause excessive current to flow through the affected upper MOSFET; this current is readily transformed into a voltage by a current shunt resistor. Allowing for a 5A motor current under load, this yields a resistor value of [5A/50mV (min)] = 0.01Ω for R1 and R2. To allow for inrush current when the motor starts up or changes direction, delay networks (R3/C5 and R4/C6) have been added to each half of the H-bridge. At a 20A startup current, the values shown give a 3ms delay. The value of the capacitor can be changed to affect longer or shorter delays as needed (the resistor value should not be raised above 10k). A short-to-ground fault, however, requires a shutdown in microseconds, not milliseconds. This is accomplished by adding two BAT85 signal level Schottky diodes (D1 and D2) in parallel with the 10k delay resistors. At a fault current of approximately 45A, which is easily attained in the short-circuit case, V_{SHUNT} = 0.45V. At this voltage the appropriate diode conducts to temporarily bypass the delay resistor, allowing the LT1161 to turn off the imperiled MOSFET within 20μs (typical). In each case, the retry interval is programmed by C1 and C2; the 10μF shown gives a time-out of about 1.8 seconds.

The LT1161 is a quad driver IC, capable of providing drive and protection for two additional MOSFETs beyond those shown in Figure 176.

SIMPLE THERMAL ANALYSIS — A REAL COOL SUBJECT FOR LTC REGULATORS

by Alan Rich

As the temperatures go up... so go the problems with voltage regulators.

Introduction

Linear Technology Corporation applications engineers get lots of calls saying, "that $X%#@& voltage regulator is so hot I can't touch it!" The purpose of the article is to show you, the design engineer, how to perform simple thermal calculations to determine regulator temperature and select the proper package style and/or heat sink. In addition, it will show an alternate method of specifying thermal parameters on LTC voltage regulators.

Definition of Terms

Power dissipation is the parameter that causes a regulator to heat up; the unit for power is watts. Power is the product of the voltage across a linear regulator times the load current (see Figure 177).

Thermal resistance is a measure of the flow of heat from one surface to another surface; the unit of thermal resistance is °C/watt. Common terms for thermal resistance that show up on most LTC data sheets are:

θ_{JC}—thermal resistance from the junction of the die to the case of the package

θ_{JA}—thermal resistance from the junction of the die to the ambient temperature

Some typical LTC regulators and their thermal characteristics are shown in Table 1.

Table 1. θ_{JC} and θ_{JA} for Three LTC Regulators

DEVICE	θ_{JC} (°C/W)	θ_{JA} (°C/W)
LT1005CT	5.0	—
LT1083MK	1.6	—
LT1129CT	5.0	50

There are several other common thermal resistance terms:

θ_{CS} — thermal resistance from the case of the package to the heat sink

θ_{SA} — thermal resistance from a heat sink surface to the ambient temperature

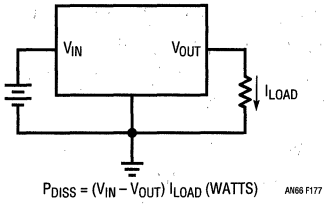


Figure 177. Typical Linear Regulator Circuit

The last two terms are determined by how a regulator is mounted to the heat sink and by the properties of the heat sink. Heat sinks are used to decrease the thermal resistance and therefore lower the temperature rise of the regulator.

Temperature is a term with which we are all very familiar. All thermal calculations will use the Centigrade scale or °C.

T_J — temperature of the junction of the regulator die
T_C — temperature of the case of the regulator
T_A — ambient temperature

The maximum operating junction temperature, $T_{J\,MAX}$ for LTC regulators is shown on the device data sheet.

What is Thermal Analysis?

The goal of any thermal analysis is to determine the regulator junction temperature, T_J, to ensure that this temperature is less than either the regulator rating or a design specification. In the simplest case, temperature rise is calculated by multiplying the power times the total of all thermal resistance:

$$T_R = P(\theta_{TOTAL})$$

θ_{TOTAL} includes the thermal resistance junction-to-case (θ_{JC}), thermal resistance case-to-heat sink (θ_{CS}), and thermal resistance heat sink-to-ambient (θ_{SA}).

T_R represents the temperature rise above the ambient temperature; therefore, to determine the actual junction temperature of the regulator, the ambient temperature must be added to T_R:

Regulator junction temperature =
Ambient Temperature + T_R

For example, consider a circuit using an LT1129CT operating in a 50°C enclosure with an input voltage of 8VDC, an output voltage of 5VDC and a load current of 1A[1].

[1]The LT1129CT is guaranteed for 700mA, but could be selected to output 1A.

The power dissipated by the LT1129CT is:

$P = (V_{IN} - V_{OUT})(I_{LOAD}) = (8V - 5V)(1a) = 3W$

The first question is, does this circuit need a heat sink?

Since we have assumed no heat sink on the LT1129CT for the purpose of this calculation, we must use thermal resistance from junction to ambient, $\theta_{JA} = 50°C/W$.

$T_J = P(\theta_{JA}) + T_A = 3W(50°C/W) + 50°C$

$= 150°C + 50°C = 200°C$

The junction temperature, T_J, that we just calculated is greater than the LT1129CT's maximum junction temperature specification of 125°C; therefore this circuit must use a heat sink.

Now the task at hand is to calculate the correct heat sink to use. The selected heat sink must hold the junction temperature at less than 125°C for the LT1129CT.

$T_J = P(\theta_{TOTAL}) + T_A$
$125°C = 3W(\theta_{TOTAL}) + 50°C$
$\theta_{TOTAL} = 25°C/W$ and
$\theta_{TOTAL} = \theta_{JC} + \theta_{CS} + \theta_{SA}$

For this configuration:

$\theta_{JC} = 5°C/W$ (LT1129CT data sheet)
$\theta_{CS} = 0.2°C/W$ (typical for heat sink mounting)
θ_{SA} = heat sink specification

Plugging in these numbers:

$25°C/W = 5°C/W + 0.2°C/W + \theta_{SA}$
$\theta_{SA} = 19.8°C/W$

Therefore, the heat sink selected must have a thermal resistance of less than 19.8°C/W to hold the LT1129CT junction temperature at less than 125°C. Obviously, the lower the heat sink thermal resistance, the lower the LT1129CT junction temperature. A lower junction temperature will increase reliability.

Now, let's consider a circuit using an LT1129CT operating in a 50°C enclosure with an input voltage of only 6VDC, an output voltage of 5VDC, and a load current of 1A.

The power dissipated by the LT1129CT is:

$P = (V_{IN} - V_{OUT})(I_{LOAD}) = (6V - 5V)1A = 1W$

Does this circuit need a heat sink? Again, for the purposes of the calculation, we must use thermal resistance from junction to ambient, $\theta_{JA} = 50°C/W$ for the LT1129CT.

$T_J = P(\theta_{JA}) + T_A = 1W(50°C/W) + 50°C$

$= 50°C + 50°C = 100°C$

The junction temperature T_J that we just calculated is now less than the LT1129CT's maximum junction temperature specification of 125°C. Therefore this circuit does not need a heat sink. This illustrates the advantage of a low dropout regulator like the LT1129CT.

An Alternative Method for Specifying Thermal Parameters

Linear Technology Corp. has introduced an alternative method to specify and calculate thermal parameters of voltage regulators. Previous regulators, with a single thermal resistance junction-to-case (θ_{JC}), used an average of temperature rise of the control and power sections. This could easily allow excessive junction temperature under certain conditions of ambient temperature and heat sink thermal resistance.

Several LTC voltage regulators include thermal resistance and maximum junction temperature specifications for both the control and power sections, as shown in Table 2.

Table 2. Two Examples Showing Thermal Resistance of Control and Power Sections of LTC Regulators

	CONTROL		POWER	
DEVICE	θ_{JC}	T_{JMAX}	θ_{JC}	T_{JMAX}
LT1083MK	0.6°C/W	150°C	1.6°C/W	200°C
LT1085CT	0.7°C/W	125°C	3.0°C/W	150°C

As an example, let's calculate the junction temperature for the same application shown before, using an LT1085CT instead of the LT1129CT. Once again, we are operating in a 50°C enclosure; the input voltage is 8VDC, the output voltage is 5VDC and the load current is 1A.

The power dissipated by the LT1085CT is the same as before, 3W. We will assume we have selected a heat sink with a thermal resistance, θ_{SA} of 10°C/W. First calculate the control section of the LT1085CT:

θ_{JC} = 0.7°C/W (LT1085CT data sheet)
θ_{CA} = 0.2°C/W (typical)
θ_{SA} = 10°C/W

$\theta_{TOTAL} = \theta_{JC} + \theta_{CA} + \theta_{SA}$ = 0.7°C/W + 0.2°C/W + 10°C/W = 10.9°C/W

To determine the control section junction temperature:

$T_J = P(\theta_{TOTAL}) + T_A$ = 3W(10.9°C/W) + 50°C = 82.7°C ($T_{J\,MAX}$ = 125°C)

To calculate the power section of the LT1085CT:

θ_{JC} = 3°C/W (LT1085CT data sheet)
$\theta_{TOTAL} = \theta_{JC} + \theta_{CA} + \theta_{SA}$ = 3°C/W + 0.2°C/W + 10°C/W = 13.2°C/W

To determine the power section junction temperature:

$T_J = P(\theta_{TOTAL}) + T_A$ = 3W(13.2°C/W) + 50°C = 89.6°C ($T_{J\,MAX}$ = 150°C)

In both cases, the junction temperature is below the maximum rating for the respective section; this ensures reliable operation.

Conclusion

This article is an introduction to thermal analysis for voltage regulators; however, the techniques also apply to other devices, including operational amplifiers, voltage references, resistors, and the like. For the more advanced student of thermal analysis, it can be shown that there is a direct analogy between electronic circuit analysis and thermal analysis, as shown in Table 3.

Table 3. analogy Between Thermal Analysis and Electronic Circuit Analysis

THERMAL WORLD	ELECTRICAL WORLD
Power	Current
Temperature Differences	Voltage
Thermal Resistance	Resistance

All standard electronic network analysis techniques (Kirchhoff's laws, Ohm's law) and computer circuit analysis programs (SPICE) can be applied to complex thermal systems.

ALPHABETICAL INDEX (BY MAJOR CATEGORIES)

Notes

LINEAR TECHNOLOGY

Application Note 67

September 1996

Linear Technology Magazine Circuit Collection, Volume III

Data Conversion, Interface and Signal Processing

Richard Markell, Editor

INTRODUCTION

Application Note 67 is a collection of circuits from the first five years of *Linear Technology*, targeting data conversion, interface and signal processing applications. This Application Note includes circuits such as fast video multiplexers for high speed video, an ultraselective bandpass filter circuit with adjustable gain and a fully differential, 8-channel, 12-bit A/D system. The categories included herein are data conversion, interface, filters, instrumentation, video/op amps and miscellaneous circuits. Application Note 66, which covers power products and circuits from *Linear Technology*'s first five years, is also available from LTC.

ARTICLE INDEX

Data Conversion

FULLY DIFFERENTIAL, 8-CHANNEL, 12-BIT A/D SYSTEM USING THE LTC1390 AND LTC1410

by Kevin R. Hoskins

The LTC1410's fast 1.25Msps conversion rate and differential ±2.5V input range make it ideal for applications that require multichannel acquisition of fast, wide bandwidth signals. These applications include multitransducer vibration analysis, race vehicle telemetry data acquisition and multichannel telecommunications. The LTC1410 can be combined with the LTC1390 8-channel serial interfaced analog multiplexer to create a differential ADC system with conversion throughput rates up to 625ksps. This rate applies to situations where the selected channel changes with each conversion. The conversion rate increases to 1.25Msps if the same channel is used for consecutive conversions.

Figure 1 shows the complete differential, 8-channel A/D circuit. Two LTC1390s, U1 and U2, are used as noninvert-

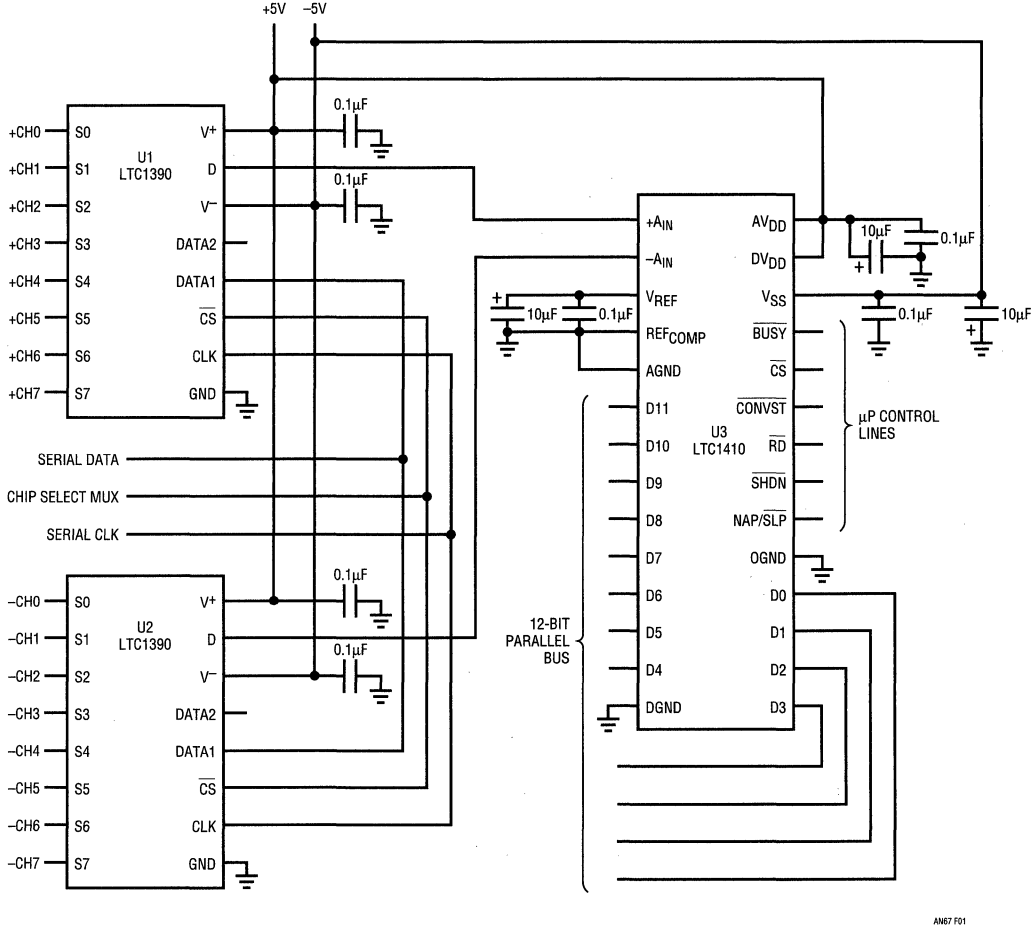


Figure 1. Fully Differential 8-Channel Data Acquisition System Achieves 625ksps Throughput

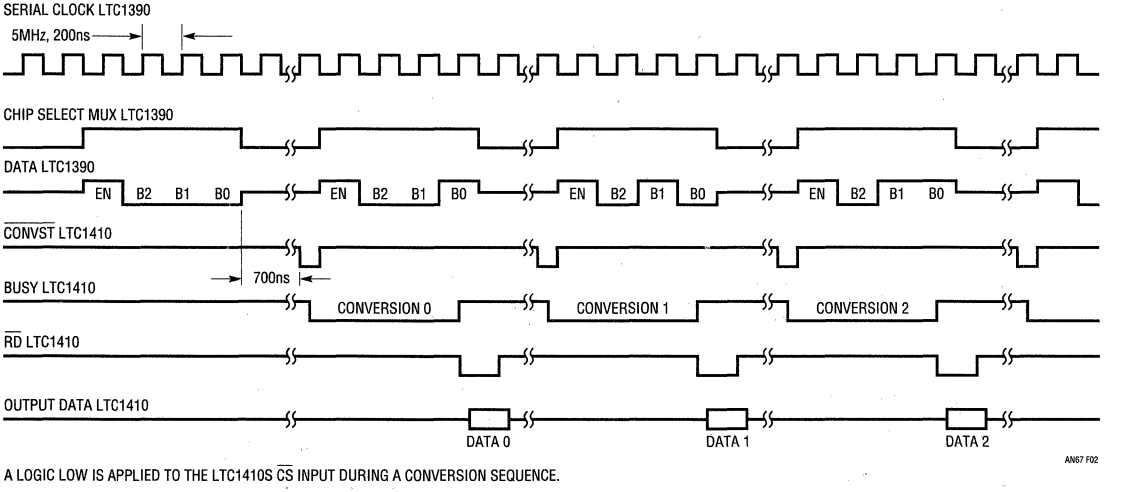
ing and inverting input multiplexers. The outputs of the noninverting and inverting multiplexers are applied to the LTC1410's $+A_{IN}$ and $-A_{IN}$ inputs, respectively. The LTC1390 share the Chip Select MUX, Serial Data and Serial Clock control signals. This arrangement simultaneously selects the same channel on each multiplexer: S0 for both +CH0 and –CH0, S1 for both +CH1 and –CH1, and so on.

As shown in the timing diagram (Figure 2), MUX channel selection and A/D conversion are pipelined to maximize the converter's throughput. The conversion process begins with selecting the desired multiplexer channel pair. With a logic high applied to the LTC1390's $\overline{CS}$ input, the channel pair data is clocked into each Data 1 input on the rising edge of the 5MHz clock signal. Chip Select MUX is then pulled low, latching the channel pair selection data. The signals on the selected MUX inputs are then applied to the LTC1410's differential inputs. Chip Select MUX is pulled low 700ns before the LTC1410's conversion start input, $\overline{CONVST}$, is pulled low. This corresponds to the maximum time needed by the LTC1390's MUX switches to fully turn on. This ensures that the input signals are fully settled before the LTC1410's S/H captures its sample.

The LTC1410's S/H acquires the input signal and begins conversion on $\overline{CONVST}$'s falling edge. During the conversion, the LTC1390's $\overline{CS}$ input is pulled high and the data for the next channel pair is clocked into Data 1. This pipelined operation continues until a conversion sequence is completed. When a new channel pair is selected for each conversion, the sampling rate of each channel is 78ksps, allowing an input signal bandwidth of 39kHz for each channel of the LTC1390/LTC1410 system.

To maximize the throughput rate, the LTC1410's $\overline{CS}$ input is pulled low at the beginning of a series of conversions. The LTC1410's data output drivers are controlled by the signal applied to $\overline{RD}$. The conversion's results are available 20ns before the rising edge of Busy. The rising edge of the Busy output signal can be used to notify a processor that a conversion has ended and data is ready to read.

This circuit takes advantage of the LTC1410's very high 1.25Msps conversion rate and differential inputs and the LTC1390's ease of programming to create an A/D system that maintains wide input signal bandwidth while sampling multiple input signals.



A LOGIC LOW IS APPLIED TO THE LTC1410S $\overline{CS}$ INPUT DURING A CONVERSION SEQUENCE.

Figure 2. The Figure 1 Circuit Timing Diagram

12-BIT DAC APPLICATIONS

by Kevin R. Hoskins

System Autoranging

System autoranging, adjusting an ADC's full-scale range, is an application area for which the LTC1257 is appropriate. Autoranging is especially useful when using an ADC with multiplexed inputs. Without autoranging only two reference values are used: one to set the full-scale magnitude and another to set the zero scale magnitude. Since it is common to have input signals with different zero scale and full-scale magnitude requirements, fixed reference voltages present a problem. Although the ranges selected for some of the inputs may take advantage of the full range of ADC output codes, inputs that do not span the same range will not generate all codes, reducing the ADC's effective resolution. One possible solution is to match the reference voltage span to each multiplexer input.

The circuit shown in Figure 3 uses two LTC1257s to set the full-scale and zero operating points of the LTC1296

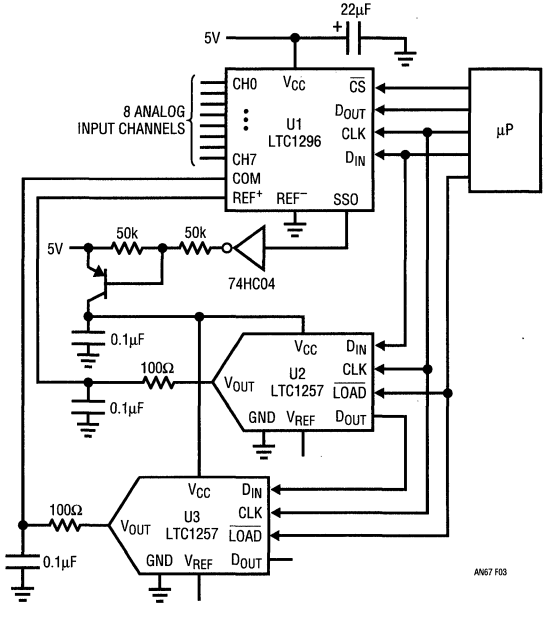


Figure 3. Using Two LTC1257 12-Bit Voltage Output DACs to Set the Input Span of the 12-Bit 8-Channel LTC1296

12-bit, 8-channel ADC. The ADC shares its serial interface with the DACs. To further simplify bus connections, the DACs' data is daisy-chained. Two chip selects are used, one to select the LTC1296 when programming its multiplexer and the other to select the DACs when setting their output voltages.

During the conversion process, U2 and U3 receive the full and zero scale codes, respectively, that correspond to a selected multiplexer channel. For example, let channel 2's span begin at 2V and end at 4.5V. When a host processor wants a conversion of channel 2's input signal, it first sends code that sets the output of U2 to 2V and U3 to 4.5V, fixing the span to 2.5V. The processor then sends data to the LTC1296 selecting channel 2. The processor next clocks the LTC1296 and reads the data generated during the conversion of the $3.5V_{P-P}$ signal applied to channel 2. As other multiplexer channels are selected the DAC outputs are changed to match their spans.

Computer-Controlled 4 – 20mA Current Loop

A common and useful circuit is the 4 – 20mA current loop. It is used to transmit information over long distances using varying current levels. The advantage of using current over voltage is the absence of IR losses and the transmission errors and signal losses they can create.

The circuit in Figure 4 is a computer-controlled 4 – 20mA current loop. It is designed to operate on a single supply over a range of 3.3V to 30V. The circuit's zero output reference signal, 4mA, is set by R1 and calibrated using R2, and its full-scale output current is set by R3 and calibrated using R4. The zero and full-scale output currents are set as follows: with a zero input code applied to the LTC1453, the output current, I_{OUT}, is set to 4mA by adjusting R2; next, with a full-scale code applied to the DAC the full-scale output current is set to 20mA by adjusting R4.

The circuit is self-regulating, forcing the output current to remain stable for a fixed DAC output voltage. This self-regulation works as follows: starting at t = 0, the LTC1453's fixed output (in this example, 2.5V) is applied to the left side of R3; instantaneously, the voltage applied to the LT1077's input is 1.25V; this turns on Q1 and the voltage across R_S starts increasing beginning from 1.25V; as the

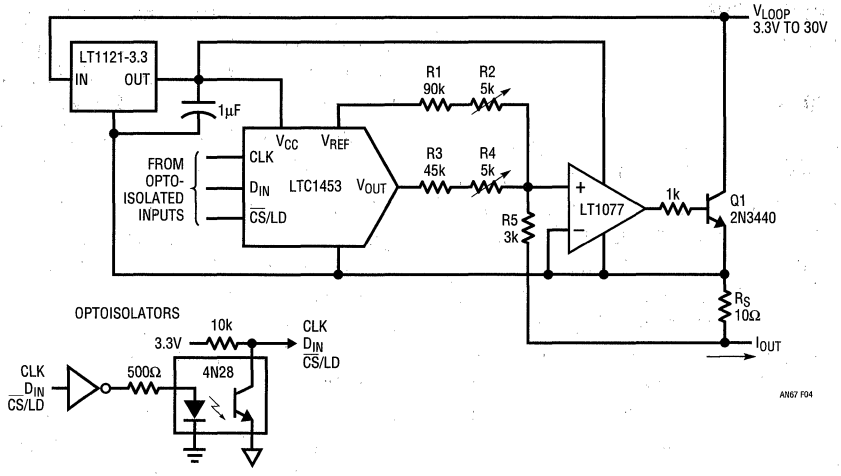


Figure 4. The LTC1453 Forms the Heart of This Isolated 4 – 20mA Current Loop

voltage across R_S increases it lifts the LTC1453's GND pin above 0V; the voltage across R_S continues to increase until it equals the DAC's output voltage.

Once the circuit reaches this stable condition, the constant DAC output voltage sets a constant current through R3 + R4 and R5. This constant current fixes a constant voltage across R5 that is also applied to the LT1077's noninverting input. Feedback from the top of R_S is applied to the inverting input. As the op amp forces its inputs to the same voltage, it will fix the voltage at the top of R_S. This in turn fixes the output current to a constant value.

Optoisolated Serial Interface

The serial interface of the LTC1451 family and the LTC1257 make optoisolated interfaces very easy and cost effective. Only three optoisolators are needed for serial data communications. Since the inputs of the LTC1451, LTC1452 and LTC1453 have generous hysteresis, the switching speed of the optoisolators is not critical. Further, because each of these DACs can be daisy-chained to others, only three optoisolators are required.

LTC1329 MICROPOWER, 8-BIT, CURRENT OUTPUT DAC USED FOR POWER SUPPLY ADJUSTMENT, TRIMMER POT REPLACEMENT

by K.S. Yap

Power Supply Voltage Adjustment

Figure 5 is a schematic of a digitally controlled power supply voltage adjustment circuit using a 2-wire interface. The LT1107 is configured as a step-up DC/DC converter, with the output voltage (V_{OUT}) determined by the values of the feedback resistors. The LTC1329's DAC current output is connected to the feedback node of these resistors, and an 8051 microprocessor is used to interface to the LTC1329. By simply clocking the LTC1329, the DAC current output is decreased or increased (decreased if D_{IN} = 0, increased if D_{IN} = 1), causing V_{OUT} to change accordingly.

Trimmer Pot Replacement

Figure 6 is a schematic of a digitally controlled offset voltage adjustment circuit using a 1-wire interface. By clocking the LTC1329, the DAC current output is increased, causing V_{R2} to increase accordingly. When the DAC current output reaches full scale it will roll over to zero, causing V_{R2} to change from the maximum offset trim voltage to the minimum offset trim voltage.

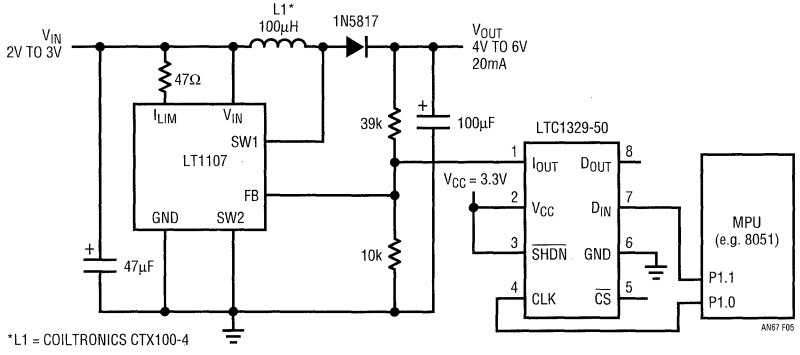


Figure 5. LTC1329 Digitally Controls the Output Voltage of a Power Supply

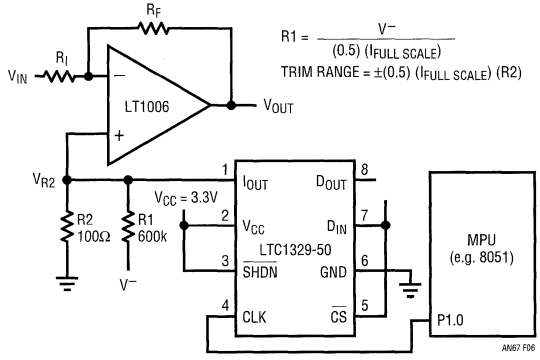


Figure 6. LTC1329 Used to Null Op Amp's Offset Voltage

12-BIT COLD JUNCTION COMPENSATED, TEMPERATURE CONTROL SYSTEM WITH SHUTDOWN

by Robert Reay

The circuit in Figure 7 is a 12-bit, single 5V supply temperature control system with shutdown. An external temperature is monitored by a J-type thermocouple. The LT1025A provides the cold junction compensation for the thermocouple and the LTC1050 chopper op amp provides signal gain. The 47kΩ, 1µF RC network filters the chopping noise before the signal is sent to the A/D converter. The LTC1297 A/D converter uses the reference of the LTC1257 after it has been filtered to set full scale. After the A/D measurement is taken $\overline{CS}$ is pulled high and everything except the LTC1257 is powered down, reducing the system supply current to about 350µA. A word can then be written to the LTC1257 and its output can be used as a temperature control signal for the system being monitored.

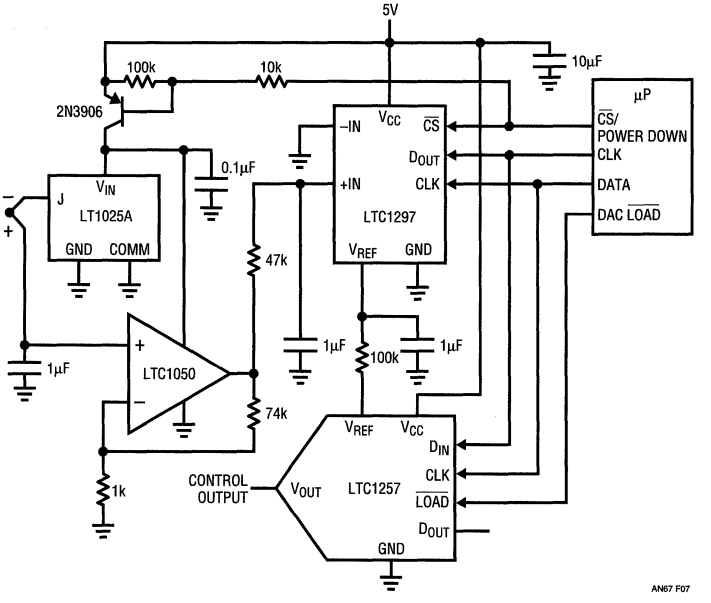


Figure 7. 12-Bit Single 5V Control System with Shutdown

A 12-BIT MICROPOWER BATTERY CURRENT MONITOR

by Sammy Lum

Introduction

The LTC1297 forms the core of the micropower battery current monitor shown in Figure 8. This 12-bit data acquisition system features an automatic power shutdown that is activated after each conversion. In shutdown the supply current is reduced to 6µA, typically. As shown in Figure 9, the average power supply current of the LTC1297 varies from milliamperes to a few microamperes as the sampling frequency is reduced. This circuit draws only 190µA from a 6V to 12V battery when the sampling frequency is less than 10 samples per second. Wake-up time is limited by that required by the LTC1297 (5.5µs). For long periods of inactivity, the circuit's supply current can be further reduced to 20µA by using the shutdown feature on the LT1121. More wake-up time is required when using this mode of shutdown. It is usually determined by the amount of capacitance in the circuit and the available charging current from the regulator.

The Battery Current Monitor

The battery voltage of 6V to 12V is regulated down to 5V by the LT1121 micropower regulator. A sense resistor of 0.05Ω is placed in series with the battery to convert the battery current to a voltage. Full scale is designed for 2A, giving a resolution of 0.5mA with the 12-bit ADC. The LTC1047 amplifies the voltage across the sense resistor

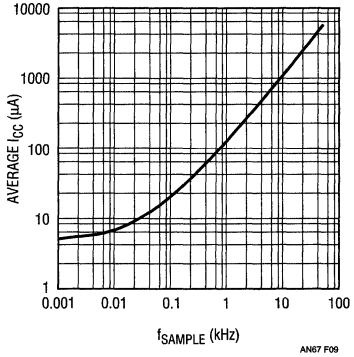


Figure 9. Power Supply Current vs Sampling Frequency for the LTC1297

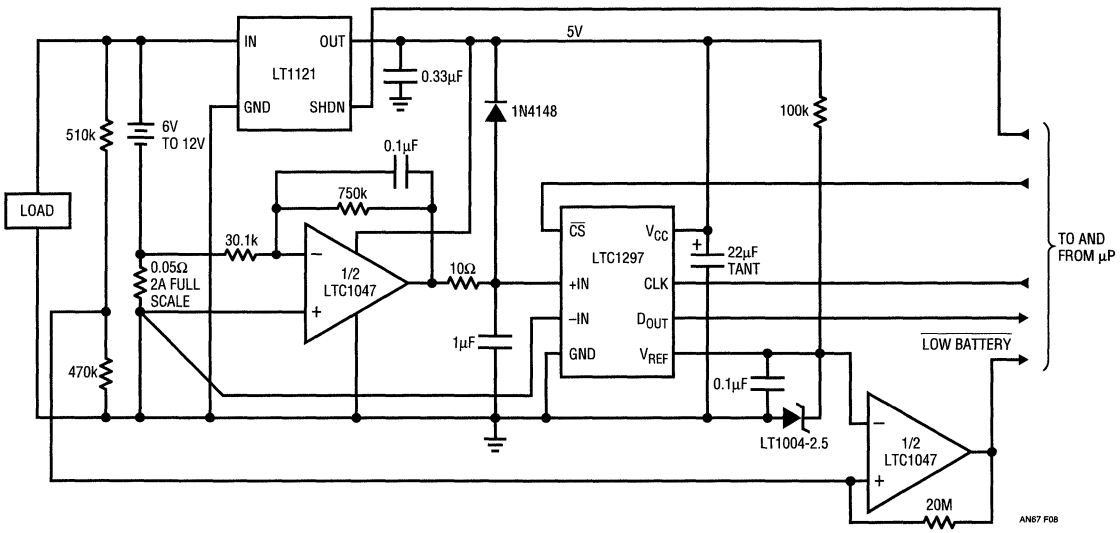


Figure 8. A Micropower Battery Current Monitor Using the LTC1297 12-Bit Data Acquisition System

by 25 V/V. This goes through an RC lowpass filter before being fed into the input of the LTC1297. The RC filter serves two functions. First it helps band limit the input noise to the ADC. Second the capacitor helps the LTC1047 recover from transients due to the switching input capacitor of the LTC1297. The LT1004 provides the full-scale reference for the ADC. A low-battery detection circuit has been created by using the other half of the LTC1047 as a comparator. Its trip point has been set to 5V plus the dropout voltage of the LT1121. Because data is transmitted serially to and from the microprocessor or microcontroller, this current monitor circuit can be located close to the battery.

Interface

V.35 TRANSCEIVERS ALLOW 3-CHIP V.35 PORT SOLUTION

by Y.K. Sim

Two new LTC interface devices, the LTC1345 and the LTC1346, provide the differential drivers and receivers needed to implement a V.35 interface. When used in conjunction with an RS232 transceiver like the LT1134A, they allow a complete V.35 interface to be implemented with just two transceiver chips and one resistor termination chip. The LTC1345 and LTC1346 provide the three differential drivers and receivers necessary to implement the high speed path and the LT1134A provides the four RS232 drivers and receivers required for the handshaking interface. Both the LTC1345 and the LT1134A provide onboard charge pump power supplies allowing a complete V.35 interface to be powered from a single 5V supply. For systems where ±5V supplies are present the LTC1346 is offered without charge pumps, representing a 30% power savings.

The differential transceivers are capable of operating at data rates above 10MBd in nonreturn-to-zero (NRZ) format.

The RS232 handshaking lines can be implemented with standard RS232 transceivers. The LT1134A provides four RS232 drivers and four receivers, enough to implement the extended 8-line handshaking protocol specified in V.35. The LT1134A also includes an onboard charge pump to generate the higher voltages required by RS232 from a single 5V supply, making it an ideal companion to the LTC1345. These two chips, together with the BI Technologies termination resistor network chip provide a complete surface mountable 5V-only V.35 data port. Systems that have multiple power supply voltages available and use only the simpler 5-signal V.35 handshaking protocol can use the LTC1346 with the LT1135A or LT1039 RS232 transceivers; this combination provides a complete port while saving board space and complexity. Figure 10 shows a typical LTC1345/LT1134A V.35 implementation with five differential signals and five basic handshaking signals with an option for three additional handshaking signals.

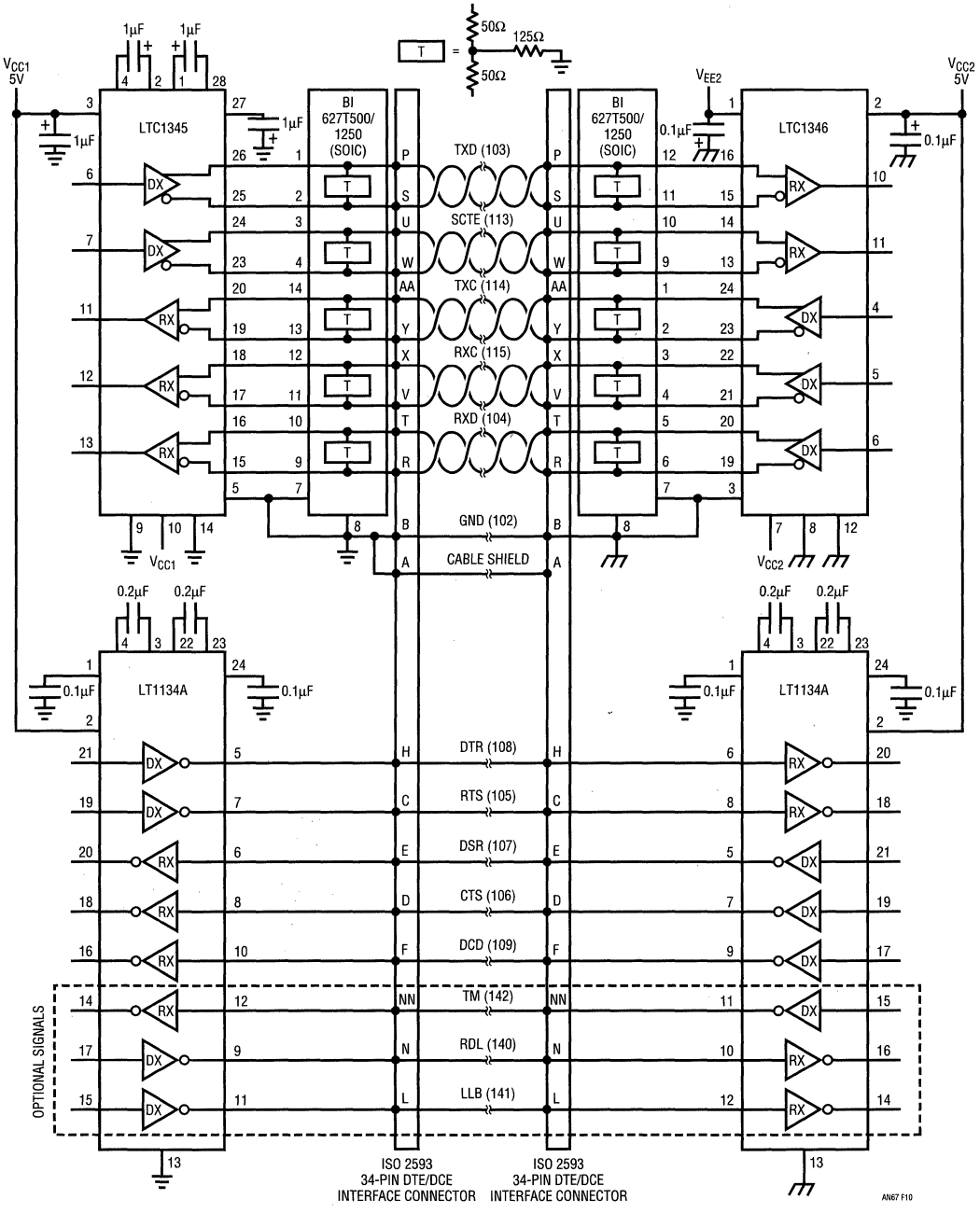


Figure 10. Typical V.35 Implementation Using LTC1345 and LTC1346

SWITCHING, ACTIVE GTL TERMINATOR

by Dale Eagar

Introduction

New high speed microprocessors, especially those used in multiprocessor workstations and video graphics terminals, require high speed backplanes that support peak data rates of up to 1Gbps. The backplane is a passive component, whereas all drivers and receivers are implemented in low voltage swing CMOS (also referred to as GTL logic). These applications require bidirectional terminators, terminators that will either source or sink current (in this case, at 1.55V). The current requirements of the terminator depended on the number of terminations on the backplane. Present applications may require up to 10A. This specification may, of course, be reduced if required.

Circuit Operation

The complete schematic of the terminator is shown in Figure 11. The circuit is based on the LT1158 half-bridge, N-channel, power MOSFET driver. The LT1158 is configured to provide bidirectional synchronous switching to MOSFETs Q1 through Q6. VR1, an LT1004-1.2, R1 and C1 generate a 1.25V reference voltage that programs the terminator's output voltage. U1A, an LT1215, is a moderate speed (23MHz GBW) precision operational amplifier that subtracts the error voltage at its inverting input from the 1.25V reference. U1A is also used to amplify this error signal. Components R3 and C2 tailor the phase and gain of this section and are selected when evaluating the system's load step response.

U1B and part of U2 provide the gain and the phase inversion necessary to form an oscillator. C3 and C4 provide positive feedback at high frequencies, which is necessary for the system to oscillate in a controlled manner while keeping the voltage excursions within the common mode range of U1B. R8, U2 and C6 provide phase inversion and negative feedback at the middle frequencies, causing U1B to oscillate at a frequency much higher than the feedback loop's response. The DC path for the oscillator is closed through the power MOSFETs Q1 to Q6, the output choke L1, the output capacitor C11 and through the feedback path with the error amplifier. R4 and R7 set the center of the common mode voltage of U1B and are selected to limit the maximum duty factor the oscillator can achieve.

R9, R10, R12 and C9 provide output current sense to U2, allowing it to shut down the oscillator via the Fault pin (Pin 5) to prevent catastrophic or even cataclysmic events from occurring. D2, C8 and the circuitry behind the Boost pin (Pin 16) of U2 work together to provide more than sufficient gate drive for the N-channel FETs Q1-3. D3, R11 and C7 allow the oscillator to start up regardless of the state of the oscillator on powerup.

Performance

The circuit provides excellent transient response, efficiencies in the source mode of better than 80% and efficiencies in the sink mode of better than 90%. Figure 12 shows the step response of the terminator.

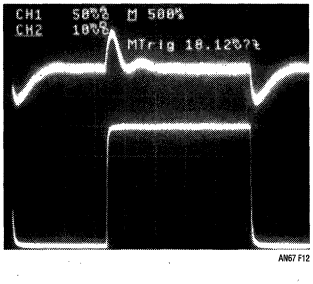
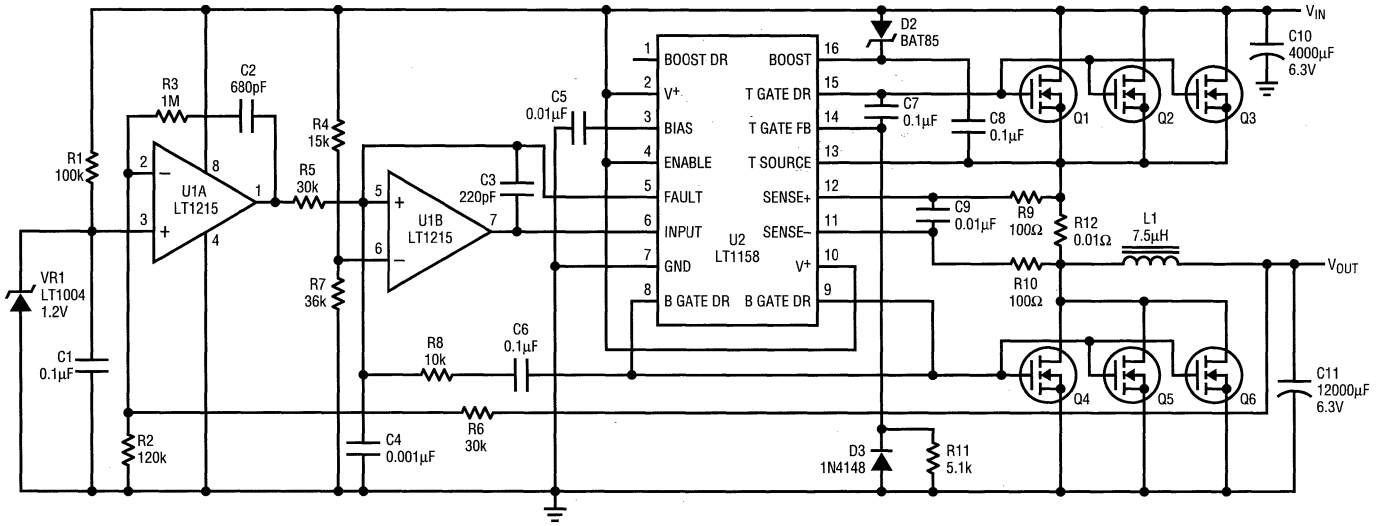


Figure 12. Step Response of LT1158-Based Terminator



Q1 TO Q6: SILICONIX Si9410.
L1: Kool Mµ® CORE #77 548-A7 10 TURNS OF #14AWG.
C10 AND C11: NICHICON HFQ 6.3V.
R12: LR2512-R010. (MFG. IRC)

$$V_{OUT} = 1.25\left(1+\frac{R6}{R2}\right)$$

AN67 F11

Kool Mµ is a registered trademark of Magnetics, Inc.

Figure 11. GTL 1.55V Terminator Provides 10A Max Current

RS232 TRANSCEIVERS FOR DTE/DCE SWITCHING

by Gary Maulding

Switched DTE/DCE Port

There are situations where a data port is required to act alternately as either a DTE or a DCE. Examples include test equipment and data multiplexers. Figure 13 shows a circuit that can switch from a 9-pin DTE to a 9-pin DCE configuration while maintaining full compliance with the RS232 standards.

The circuit uses an LT1137A DTE transceiver and an LT1138A DCE transceiver. A DTE/DCE select logic signal alternately activates or shuts down one of the two transceivers. In addition to drawing no power, the OFF transceiver's drivers achieve a high impedance state, removing themselves from the data line. The receiver inputs will continue to load the line, but this presents no operational problem and does not violate the RS232 standard. The drivers on the activated transceiver can easily drive the extra load of the companion transceiver's inputs along with the termination at the opposite end of the cable. The scope photograph (Figure 14) shows the signal outputs of the DTE/DCE switched circuit driving 3k || 1000pF at 120kBd.

To the transceiver at the opposite end of the data line the data port always appears to be a normal fixed port. All signals into the port are properly terminated in 5k.

The schematic in Figure 13 shows the essential features needed to implement DTE/DCE switching but other features can be easily included. Shutdown of both transceivers could be implemented by adding an additional logic control signal. Multiplexing of the logic level signals is also possible since receiver outputs remain in a high impedance state when the transceivers are shut down. Two capacitors can be saved by sharing the V^+ and V^- filter capacitors between the two transceivers, but the charge pump capacitors must not be shared.

The circuits used in the demonstration circuit are bipolar, but Linear Technology's CMOS transceivers, such as the LTC1327 and 1328 could be substituted where the absolute minimum power dissipation is required.

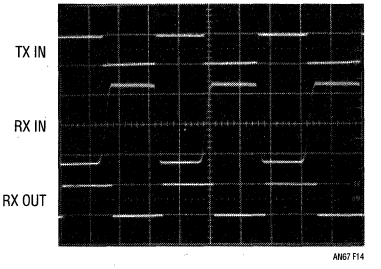


Figure 14. Oscillograph Showing Signal Outputs of the DTE/DCE Circuit of Figure 13 Driving 3k || 1000pF at 120kBd

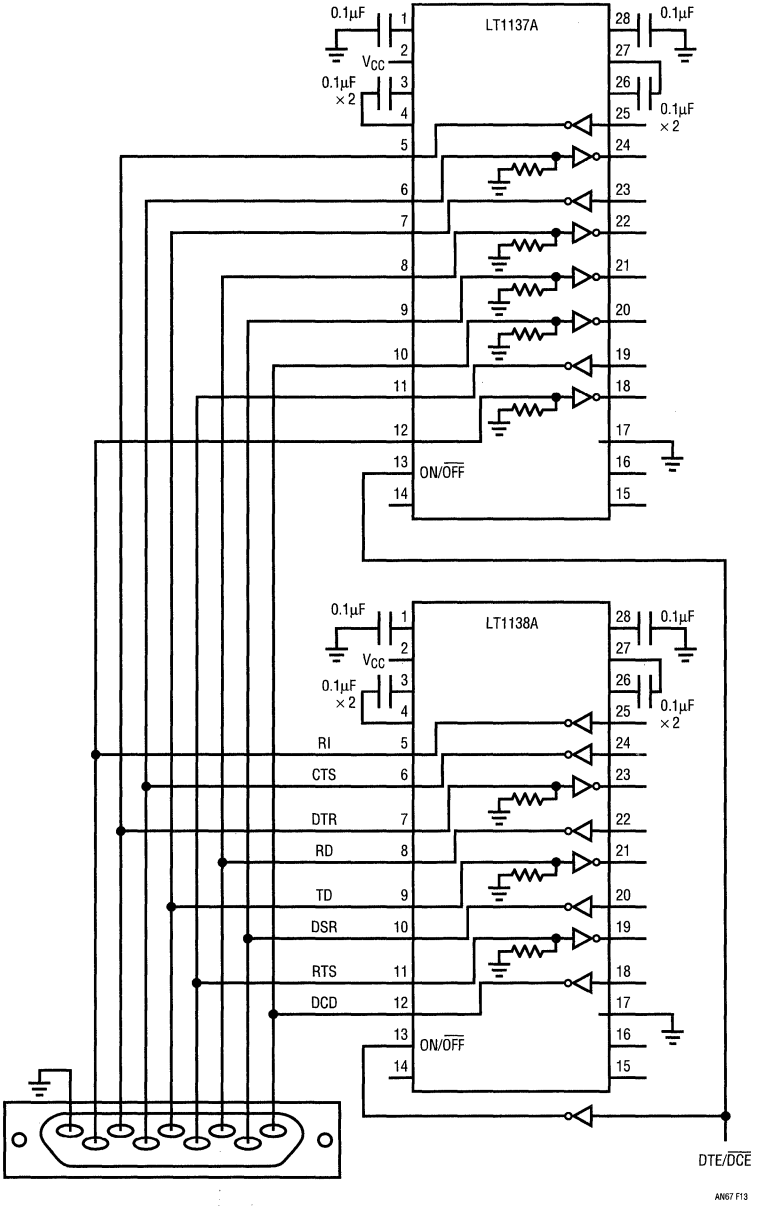


Figure 13. Switchable, 9-Pin DTE/DCE Data Port Circuitry

ACTIVE NEGATION BUS TERMINATORS

by Dale Eagar

High speed data buses require transmission line techniques, including termination, to preserve signal integrity. Lost data on a bus can be attributed to reflections of the signals from the discontinuities of the bus. The solution to this problem is proper termination of the bus.

Early designs of bus terminators were passive (see Figure 15). Passive termination works great but wastes lots of precious power, especially when the bus is not being used.

The ideal solution is a voltage source capable of both sourcing and sinking current. Such a voltage source, with termination resistors, is shown in Figure 16. This is called active negation. Active negation uses minimal quiescent current, essentially providing only the power needed to properly terminate the bus.

Active Negation Bus Terminator Using Linear Voltage Regulation

The active negation circuit shown in Figure 17 provides the power to the output at an efficiency of about 50%; the rest of the power is dissipated in either Q1 or U1 depending on the polarity of the output current.

The circuit will source or sink current. Current is sourced from the 5V supply through Q1, an NPN Darlington, to the output. The sink current flows through CR1 into the collector (Pin 1) of the LT1431, and to ground. The LT1431 regulates a scaled version of the output voltage against the

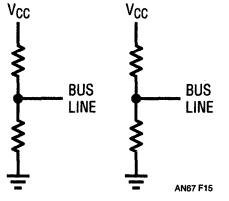


Figure 15. Passive Termination Technique

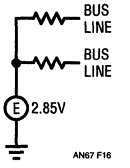


Figure 16. Active Negation Termination Technique

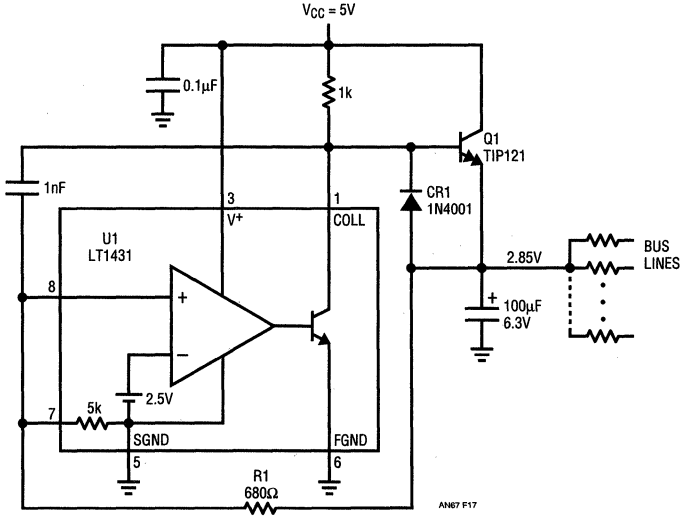


Figure 17. Linear Active Negation Voltage Source

internal 2.5V bandgap reference, driving the base of Q1 or drawing current through CR1 to regulate the output voltage. R1 and the internal 5k resistor of the LT1431 scale the output voltage.

Switching Power Supply, Active Negation Network

The switching active negation terminator shown in Figure 18 is a synchronous switcher. This solution further reduces dissipation and therefore achieves higher efficiency. This type of switcher can both source and sink current.

The switching power supply operates as follows. The 74AC04 hex inverters (U1 and U2) form a 1MHz variable duty factor oscillator. The duty factor is controlled by the output of the regulator, U3, and is maintained at the ratio of 2.85V/V_{IN}. V_{IN} is the 5V supply that powers U1, U2 and U3. The output voltage is the average voltage of the square wave (V_{IN})(duty factor) from the outputs of U1B–U1F and U2A–U2F. L1 and C2 filter the AC component of the 0V to 5V signal yielding a DC output voltage of 2.85V.

CR1 is added to prevent latchup of U1 and U2 during adverse conditions.

A logic gate could easily be added to the oscillator to add a disable function to this terminator, further lowering the quiescent power when termination is not needed.

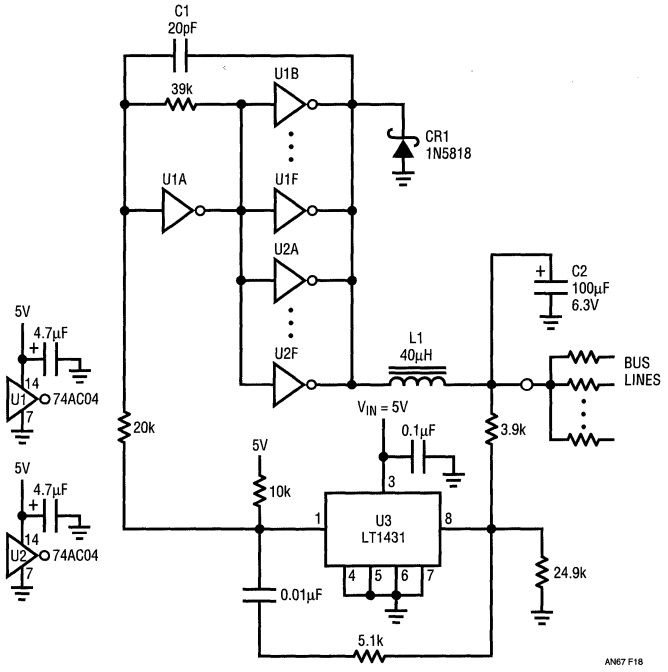


Figure 18. Switching Active Negation Termination

RS485 REPEATER EXTENDS SYSTEM CAPABILITY

by Mitchell Lee

RS485 data communications are specified for distances of up to 4000 feet. This limit is the consequence of losses in the twisted pair used to carry the data signals. Beyond 4000 feet, skin effect and dielectric losses take their toll, attenuating the signal beyond use.

If greater distances must be covered some means of repeating the data is necessary. One method is to terminate a long run of cable with a microprocessor-based node capable of relaying data to yet another length of cable.

A more simple solution* is shown in Figure 19. Two RS485 transceivers are connected back-to-back so as to relay incoming data from either side to the other. A pair of cross coupled one-shots furnish a means of "flow control" so that one and only one transmitter is turned on at any given time. Incoming data is sensed by detecting a 1-0 transition at the output of either idling receiver. The first receiver to spot such a transition triggers its associated one-shot, which, in turn, activates the opposite transmitter and ensures smooth data flow from one side to the other. At the same time the one-shot locks out the other receiver/transmitter/one-shot combination so that only one data path is open.

The one-shot is retriggered by successive 1-0 transitions and start bits, holding the data path in this configuration. The one-shot time constant is set slightly greater than the interval between any two start bits. When the received data stops, the line idles high, producing a 1 at the receiver's output. The one-shot resets, returning the opposite transceiver to the receive mode—ready for any subsequent data flow.

In order to allow adequate time for the one-shot to reset, the software protocol must wait one word length after the end of any data transmission before responding to a call or initiating a new conversation. As shown, the repeater is set up for 100kBd data rates and an 8-bit word length (plus start and stop bits).

*Honeywell Inc. patent 4, 670, 886 may apply.

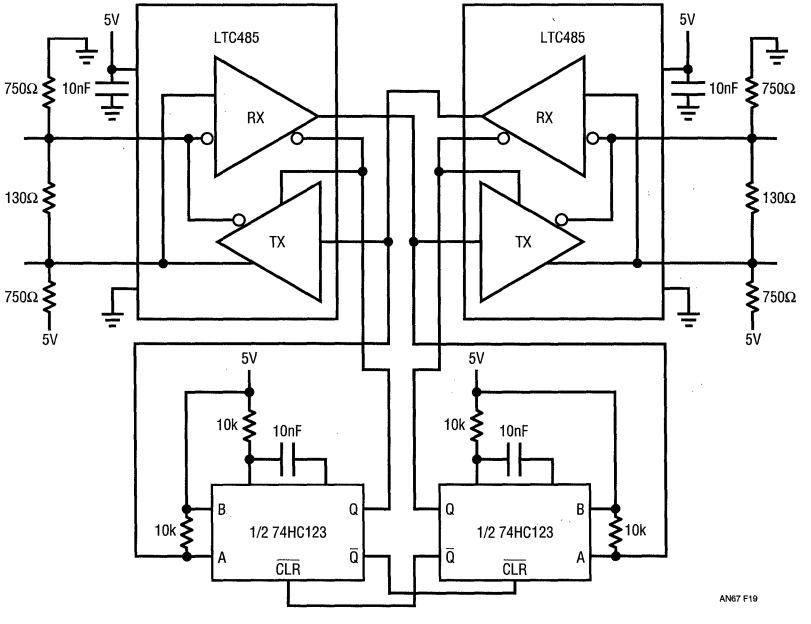


Figure 19. RS485 Repeater Schematic Diagram

AN LT1087-BASED 1.2V GTL TERMINATOR

by Mitchell Lee

A recent development in high speed digital design has resulted in a new family of logic chips called Gunning Transition Logic (GTL). Because of the speeds involved, careful attention must be paid to the transmission line characteristics of the interconnections between these chips; active termination is required.

The termination voltage is 1.20V and currents of several amperes are common in a complete system. One method of generating 1.2V is to use a linear regulator operating from 3.3V or 5V. Unfortunately, this method suffers from two major drawbacks. First, the minimum adjust voltage, without the aid of a negative supply, is 1.25V for most adjustable linear regulators. Second, most low voltage linear regulators do not feature low dropout characteristics, rendering them unusable on a 3.3V input. The LT1087 solves both of these problems with an output that can be adjusted to less than the reference voltage and a low dropout architecture.

Figure 20 shows the complete circuit. The LT1087 features feedback sense, which, in its original application, was used for remote Kelvin sensing. In the GTL terminator circuit the Sense pins are used to adjust the internal 1.25V reference downward. The result is a 1.20V, 5A regulator with 2% output tolerance over all conditions of line, load and temperature. To minimize power dissipation a 3.3V input source is recommended.

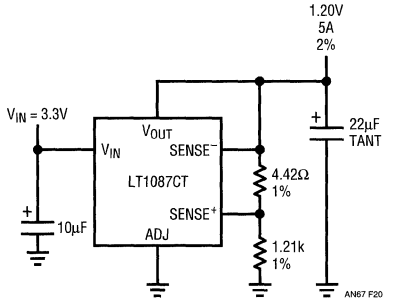


Figure 20. 1.2V GTL Termination Voltage Schematic Diagram

LTC1145/LTC1146 ACHIEVE LOW PROFILE ISOLATION WITH CAPACITIVE LEAD FRAME

by James Herr

The LTC1145 and LTC1146 are a new generation of signal isolators. Previously, signal isolation was accomplished by means of optoisolators. Light from an LED was detected across a physical isolation barrier by either a photo diode or transistor and converted to an electrical signal. Isolation levels up to thousands of volts were easily achieved.

Attempts have been made to provide signal isolation on a single silicon die. Problems arose due to reliability constraints of damage from ESD or overvoltage. A new technique, using a capacitive lead frame, overcomes the problems associated with single package signal isolation. Further, this technique is suitable for use in thin surface mount packages—a solution not available with optoisolators. The data rates are 200kbps for the LTC1145 and 20kbps for the LTC1146. Both parts can sustain over 1000V across their isolation barriers.

Applications

The LTC1145/LTC1146 can be used in a wide range of applications where voltage transients, differential ground potentials or high noise may be encountered, such as isolated serial data interfaces, isolated analog-to-digital converters for process control, isolated FET drivers and low power optoisolator replacement. One possible application is an isolated RS232 receiver. The D_{IN} pin of the LTC1145 is driven by an RS232 signal through a 5.1k resistor (Figure 21). The D_{OUT} pin of the LTC1145 presents

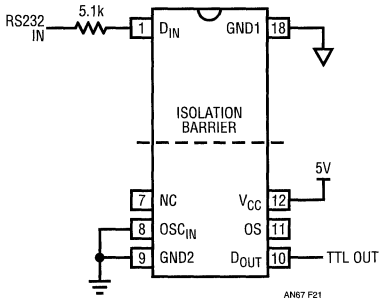


Figure 21. Isolated Low Power RS232 Receiver

isolated TTL-compatible output signals. The GND2 pin of the LTC1145 is connected to the same ground potential as the receiving end of the link. The isolator can accommodate differences of up to 1kV between GND1 and GND2.

Another application is an isolated, thermocouple-sensed temperature-to-frequency converter (see Figure 22). The output of I_3 produces a 0kHz to1kHz pulse train in response to a 0°C to 100°C temperature excursion (see LTC Application Note 45 for the details). The pulses from I_3 drive the D_{IN} pin of LTC1146. The GND1 pin is connected to the same ground potential as I_3. The D_{OUT} pin of LTC1146 presents isolated, TTL-compatible output signals. The circuit consumes only 460µA maximum, allowing it to operate from a 9V battery.

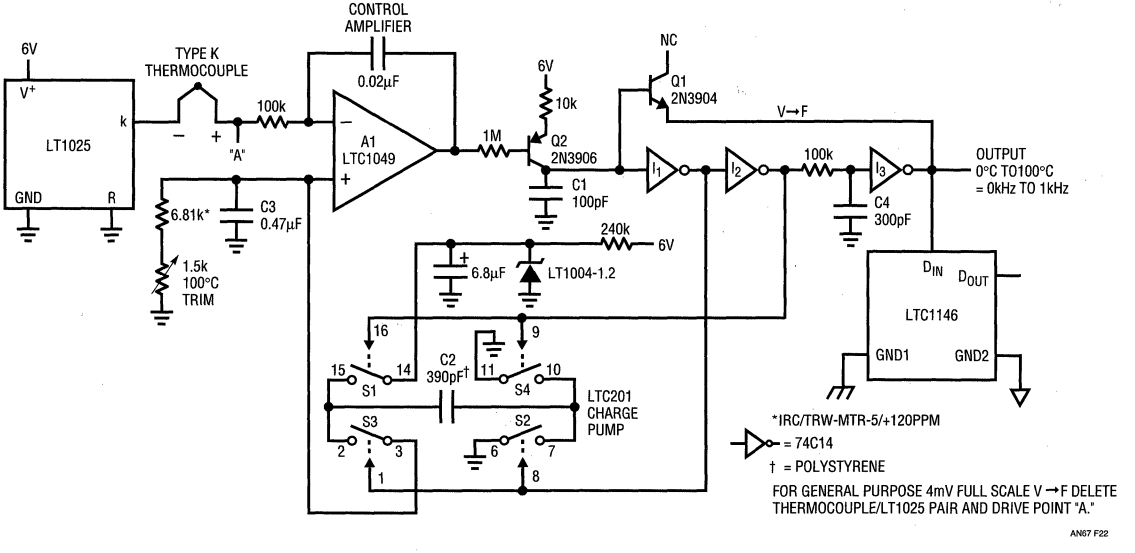


Figure 22. Isolated Temperature-to-Frequency Converter

LTC485 LINE TERMINATION

by Bob Reay

The termination of the data line connecting LTC485 transceivers is very important because an improperly terminated line can cause data errors. The data line is usually a 120Ω shielded twisted pair of wires that is terminated at each end with a 120Ω resistor (Figure 23). For some applications a problem occurs when the output of the drivers is forced into a high impedance state because the termination resistors short the inputs to the receivers. Since the receivers are differential comparators with built-in hysteresis, their output will remain in the last logic state.

For the applications that must force the outputs of the receivers to a known state, but still maintain low power consumption, the cable can be terminated as in Figure 24. A capacitor (typically 0.1µF) has been connected in series with the 120Ω termination resistor R2 and two bias resistors (R1 and R3) have been added. When data is being transmitted the capacitor looks basically like a short circuit and a differential signal is developed across the termination resistor. When the drivers are forced into a high impedance state, the bias resistors force the receiver into a logic 1 state. The receiver inputs can be reversed when the output must be a logic 0.

Because the capacitor is in series with the bias string, no DC current flows when data is not being transmitted. Care must be taken to transmit data at a high enough rate to prevent the bias resistors from charging the capacitor to the wrong state before the next data bit arrives. Also note that differences in the V^+ supplies or grounds will cause DC current to flow in the cable, but this can be kept to a minimum by using high value bias resistors.

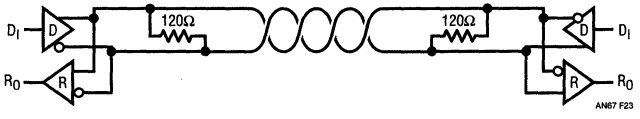


Figure 23. DC Coupled Termination

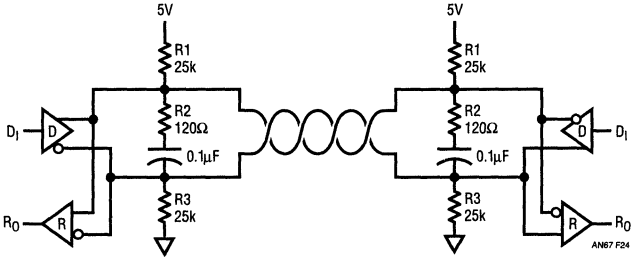


Figure 24. AC Coupled Termination

Filters

SALLEN AND KEY FILTERS USE 5% VALUES

by Dale Eagar

Lowpass filters designed after Sallen and Key usually take the form shown in Figure 25. In the classic Sallen and Key circuit, resistors R1, R2 and R3 are set to the same value to simplify the design equations.

When the three resistors are the same value, the pole placement, and thus the filter characteristics, are set by the capacitor values (C1, C2 and C3). This procedure, although great for the mathematician, can lead to problems. The problem is that, in the real world, the resistors, not the capacitors, are available in a large selection of values.

Taking advantage of the wider range of resistor values is not altogether trivial; the mathematics can be quite cumbersome and time consuming.

This Design Idea includes tables of resistor and capacitor values for third-order Sallen and Key lowpass filters. The resistor values are selected from the standard 5% value pool, and the capacitor values are selected from the standard 10% value pool. Frequencies are selected from the standard 5% value pool used for resistors. Frequencies are in Hertz, capacitance in Farads and resistance in Ohms.

Figure 26 details the PSpice™ simulation of a 1.6kHz Butterworth filter designed from these tables.

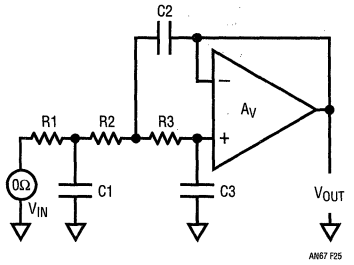


Figure 25. Sallen and Key Lowpass Filter

How to Design a Filter from the Tables:

Pick a cutoff frequency in Hertz as if it were a standard 5% resistor value in Ohms. (that is, if you want a cutoff frequency of 1.7kHz you must choose between 1.6k and 1.8k)

Select the component values from Table 1 or Table 2 as listed for the frequency (think of the first two color bands on a resistor).

Select a scale factor for the resistors and capacitors from Table 3 by the following method:

1. Select a diagonal that represents the frequency multiplier (think of the third color band on a 5% resistor).
2. Choose a particular diagonal box by either choosing a capacitor multiplier from the rows of the table that give you a desired capacitor value or by choosing a resistor multiplier from the columns of the table that gives you a desired resistance value.

Multiply the resistors and capacitors by the scale factors for the rows and columns that intersect at the chosen frequency multiplier box. (for example, 0.68 • 1µF = 0.68µF, 0.47 • 1kΩ = 470Ω).

PSpice is a trademark of MicroSim Corporation.

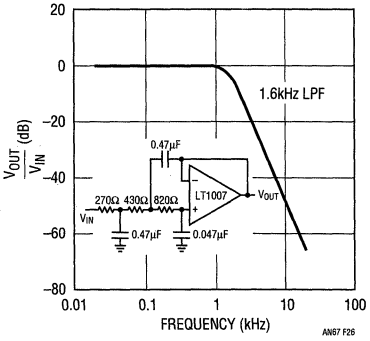


Figure 26. PSpice Simulation of 1.6kHz Butterworth Filter

Table 1. Bessel Lowpass Filter

FREQ	R1	R2	R3	C1	C2	C3
1.0	0.39	0.43	8.20	0.47	0.22	0.01
1.1	0.36	0.39	7.50	0.47	0.22	0.01
1.2	0.33	0.36	6.80	0.47	0.22	0.01
1.3	0.36	2.40	0.033	0.22	2.20	0.047
1.5	0.33	4.70	0.012	0.22	4.70	0.022
1.6	0.30	0.10	0.240	0.47	2.20	0.047
1.8	0.30	3.30	5.10	0.22	0.022	0.010
2.0	0.27	0.51	0.027	0.22	2.20	0.100
2.2	0.24	2.70	0.43	0.22	0.10	0.022
2.4	0.22	2.70	3.60	0.22	0.022	0.010
2.7	0.27	0.43	1.30	0.22	0.10	0.022
3.0	0.18	0.82	0.16	0.22	0.22	0.047
3.3	0.15	0.056	1.00	0.47	1.00	0.010
3.6	0.18	0.16	0.022	0.22	2.20	0.100
3.9	0.15	1.50	2.20	0.22	0.022	0.010
4.3	0.13	0.22	0.013	0.22	2.20	0.100
4.7	0.20	0.12	1.20	0.22	0.22	0.010
5.1	0.18	0.068	0.039	0.22	2.20	0.047
5.6	0.20	1.10	0.036	0.10	0.47	0.022
6.2	0.15	0.091	0.91	0.22	0.22	0.010
6.8	0.16	0.91	0.03	0.10	0.47	0.022
7.5	0.15	1.80	0.27	0.10	0.047	0.010
8.2	0.10	0.12	1.00	0.22	0.10	0.010
9.1	0.13	0.56	0.12	0.10	0.10	0.022

Table 2. Butterworth Lowpass Filter

FREQ	R1	R2	R3	C1	C2	C3
1.0	0.36	3.3	3.3	0.47	0.10	0.022
1.1	0.47	0.47	6.2	0.47	0.47	0.010
1.2	0.36	0.62	1.0	0.47	0.47	0.047
1.3	0.27	2.00	0.33	0.47	0.47	0.047
1.5	0.24	1.60	0.3	0.47	0.47	0.047
1.6	0.27	0.43	0.82	0.47	0.47	0.047
1.8	0.43	1.20	0.13	0.22	1.00	0.047
2.0	0.36	7.50	0.18	0.22	0.47	0.010
2.2	0.24	0.24	3.00	0.47	0.47	0.010
2.4	0.33	0.91	0.043	0.22	2.20	0.047
2.7	0.27	5.60	0.062	0.22	1.00	0.010
3.0	0.24	5.10	0.056	0.22	1.00	0.010
3.3	0.22	1.60	0.30	0.22	0.22	0.022
3.6	0.22	0.56	0.068	0.22	1.00	0.047
3.9	0.24	0.39	0.68	0.22	0.22	0.022
4.3	0.18	0.51	0.024	0.22	2.20	0.047
4.7	0.16	1.30	0.039	0.22	1.00	0.022
5.1	0.16	0.36	0.051	0.22	1.00	0.047
5.6	0.13	1.10	0.033	0.22	1.00	0.022
6.2	0.13	0.36	0.016	0.22	2.20	0.047
6.8	0.24	1.60	0.33	0.10	0.10	0.010
7.5	0.12	0.30	1.20	0.22	0.10	0.010
8.2	0.12	0.11	0.024	0.22	2.20	0.047
9.1	0.18	1.50	0.091	0.10	0.22	0.010

Table 3. Frequency Multipliers

	0.1Ω	1Ω	10Ω	100Ω	1k	10k	100k	1M	10M	100M
1F	10	1	0.1	0.001	—	—	—	—	—	—
0.1F	100	10	1	0.1	0.01	0.001	—	—	—	—
10,000μF	1k	100	10	1	0.1	0.01	0.001	—	—	—
1,000μF	10k	1k	100	10	1	0.1	0.01	0.001	—	—
100μF	100k	10k	1k	100	10	1	0.1	0.01	0.001	—
10μF	1M	100k	10k	1k	100	10	1	0.1	0.01	0.001
1μF	10M	1M	100k	10k	1k	100	10	1	0.1	0.01
0.1μF	100M	10M	1M	100k	10k	1k	100	10	1	0.1
0.01μF	1G	100M	10M	1M	100k	10k	1k	100	10	1
1,000pF	—	1G	100M	10M	1M	100k	10k	1k	100	10
100pF	—	—	1G	100M	10M	1M	100k	10k	1k	100

LOW POWER SIGNAL DETECTION IN A NOISY ENVIRONMENT

by Philip Karantzalis and Jimmylee Lawson

Introduction

In signal detection applications where a small narrowband signal is to be detected in the presence of wideband noise, one can design an asynchronous (nonphase sensitive) tone detector using an ultraselective bandpass filter, such as the LTC1164-8. The ultranarrow passband of the LTC1164-8 filter band limits any random noise and increases the detector's signal sensitivity.

The LTC1164-8 is an eighth-order, elliptic bandpass filter with the following features: the filter's f_{CENTER} (the center frequency of the filter's passband) is clock tunable and is equal to the clock frequency divided by 100; the filter's passband is from $0.995f_{CENTER}$ to $1.005f_{CENTER}$ (±0.5% from f_{CENTER}). Figure 27 shows a typical LTC1164-8 passband response and the area of passband gain variation. Outside the filter's passband, signal attenuation increases to more than 50dB for frequencies between $0.96f_{CENTER}$ and $1.04f_{CENTER}$. Quiescent current is typically 2.3mA with a single 5V power supply.

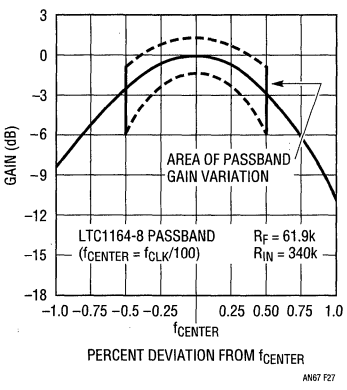


Figure 27. Detail of LTC1164-8 Passband

An Ultraselective Bandpass Filter and a Dual Comparator Build a High Performance Tone Detector

The LTC1164-8 has excellent selectivity, which limits the noise that passes from the input to the output of the filter. As a result, one can build a tone detector that can extract small signals from the "mud." Figure 28 shows the block diagram of such a tone detector. The detector's input is an LTC1164-8 bandpass filter whose output is AC coupled to a dual comparator circuit. The first comparator converts the filter's output to a variable pulsewidth signal. The pulsewidth varies depending on the signal amplitude. The average DC value of the pulse signal is extracted by a lowpass RC filter and applied to the second comparator. The identification of a tone is indicated by a logic high at the output of the second comparator.

One of the key benefits of using a high selectivity bandpass filter for tone detection is that when wideband noise (white noise) appears at the input of the filter, only a small amount of input noise will reach the filter's output. This results in a dramatically improved signal-to-noise ratio at the output of the filter compared to the signal-to-noise at the input of the filter. If the output noise of the LTC1164-8 is neglected, the signal-to-noise ratio at the output of the filter divided by the signal-to-noise ratio at the input of the filter is:

$$\frac{(S/N)_{OUT}}{(S/N)_{IN}} = 20 \text{ Log } \sqrt{\frac{(BW)_{IN}}{(BW)_f}}$$

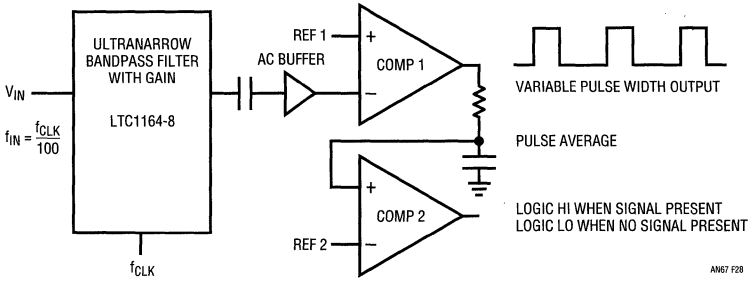


Figure 28. Tone Detector Block Diagram

where: $(BW)_{IN}$ = the noise bandwidth at the input of the filter and $(BW)_f = (0.01)(f_{CENTER})$ is the filter's noise equivalent bandwidth.

For example, a small 1kHz signal is sent through a cable that is also conducting random noise with a 3.4kHz bandwidth. An LTC1164-8 is used to detect the 1kHz signal. The signal-to-noise ratio at the output of the filter is 25.3db larger than the signal-to-noise ratio at the input of the filter:

$$\sqrt{\frac{(BW)_{IN}}{(BW)_f}} = 20\ \text{Log}\ \sqrt{\frac{3.4\text{kHz}}{(0.01)(1\text{kHz})}} = 25.3\text{dB}$$

Figure 29 shows the complete circuit for a 1kHz tone detector operating with a single 5V supply. An LTC1164-8 with a clock input set at 100kHz sets the tone detector's frequency at 1kHz ($f_{CENTER} = f_{CLK}/100$). A low frequency op amp (LT1013) and resistors R_{IN} and R_F set the filter's gain. In order to minimize the filter's output noise and maintain optimum dynamic range, the output feedback resistor R_F should be 61.9k. Capacitor C_F across resistor R_F is added to reduce the clock feedthrough at the filter's output.

To set the gain for the LTC1164-8, R_{IN} should be calculated by the equation:

$$R_{IN} = 340\text{k/Gain}$$

In Figure 29, the filter's gain is 10 (R_{IN} = 34k). Capacitor C1 and a unity-gain op amp (LT1013) AC couple the signal at the filter's output to an LTC1040 dual low power comparator. AC coupling is required to eliminate any DC offset caused by the LTC1164-8.

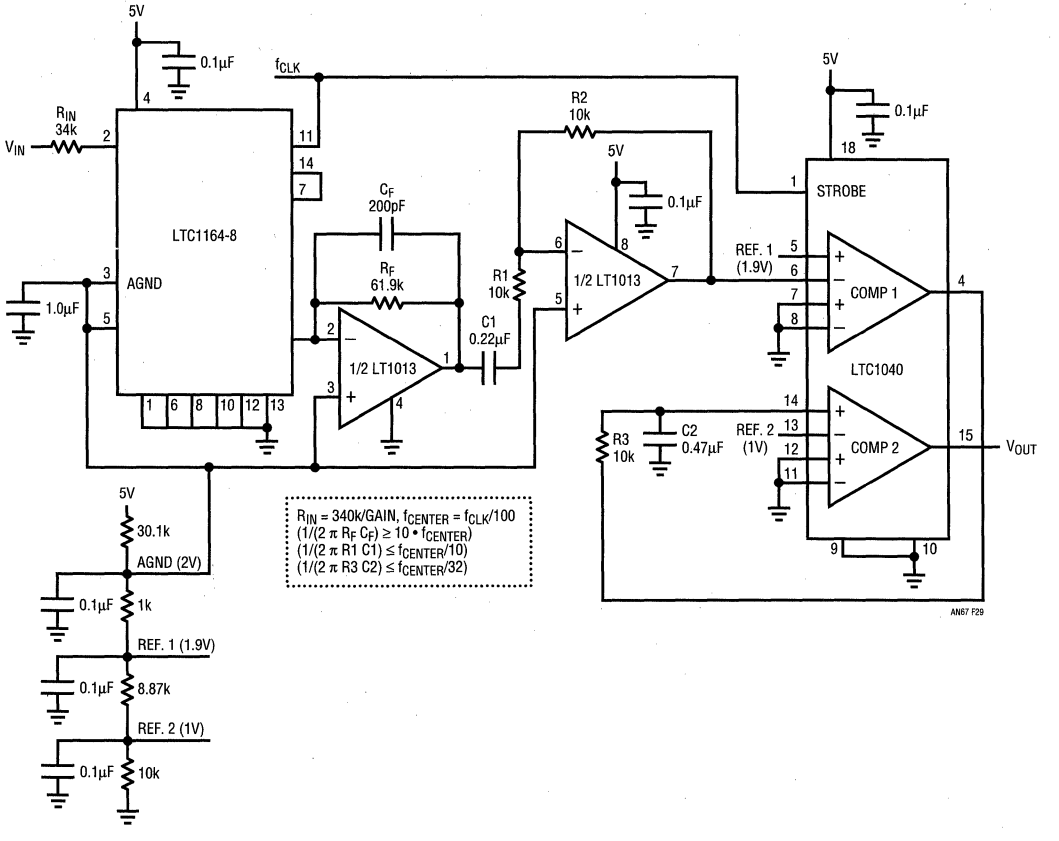


Figure 29. 1kHz Tone Detector with Gain of 10

A resistive divider generates a 2V bias for the LTC1164-8 "ground" (Pins 3 and 5) and the positive input of the LT1013 dual op amps. For single 5V operation the output swing of the LTC1164-8 is from 0.5V to 3.5V, centered at 2V. The divider also provides the reference voltages for the LTC1040 dual comparators (Ref. 1 = 1.9V and Ref. 2 = 1V). Power supply variations do not affect the performance of this circuit because all DC reference voltages are derived from the same resistor divider and will track any changes in the 5V power supply.

Theory of Operation

The tone detector works by looking at the negative peaks at the output of the filter. Signals below 1.9V at the output of the filter trip the first comparator. The second comparator has a 1V reference and detects the average value of the output of the first comparator. The R3/C2 time constant is set to allow detection only if the duty cycle of the first comparator's output exceeds 25%. Waveforms with duty cycles below 25% are arbitrarily assumed to carry false information.

The circuitry is designed so that two or more negative signal peaks of 160mV at the filter's output produce a 25% duty cycle pulse waveform at the output of the first detector (the 1.9V and 1V references for comparators 1 and 2 respectively, set the $160mV_{PEAK}$ and the 25% duty cycle). The 25% duty cycle requirement establishes an operating point or "minimum detectable signal" for the detector circuit. Thus, the circuitry outputs a "tone present" condition only when the duty cycle is greater than or equal to 25%. The 25% duty cycle requirement sets two conditions for optimum tone detection at the detector's input.

The first input condition is the maximum input noise spectral density that will not trigger the detector's output to indicate the presence of a tone. When only noise is present at the filter's input, the maximum input noise spectral density is conservatively defined as the amount required to produce noise peaks at the filter's output of 160mV or lower amplitude. The 160mV maximum noise peak specification at the filter's output can be converted to output noise in mV_{RMS} by using a crest factor of 5 (the crest factor of a signal is the ratio of its peak value to its RMS value—a theoretical crest factor of 5 predicts 99.3% of the maximum peaks of wideband noise with uniform spectral density). Therefore, the maximum allowable noise at the filter's output is $32mV_{RMS}$ ($160mV_{PEAK}/5$). The noise at the filter's output depends on the filter's gain and noise equivalent bandwidth and the spectral density of the noise at the filter's input. Therefore, the maximum input noise spectral density for Figure 3's circuit is:

$$e_{IN} \leq 32mV_{RMS}/(Gain \bullet \sqrt{(BW)_f}) \frac{V_{RMS}}{\sqrt{Hz}}$$

where: Gain is the filter's gain at its center frequency and $(BW)_f$ is the filter's noise equivalent bandwidth.

Note: Compared to $32mV_{RMS}$ the $270mV_{RMS}$ output noise of the LTC1164-8 is negligible. The output noise of the LTC1164-8 is independent of the chosen filter signal gain.

The second input condition is the minimum input signal required so that a tone can be detected when it is buried by the maximum noise, as defined by the first input condition. When a tone plus noise is present at the filter's input, the output of the filter will be a tone whose amplitude is modulated by the bandlimited noise at the filter's output. If a maximum noise peak of 160mV modulates the tone's amplitude, a 320mV tone peak at the filter's output can be detected because the product of the noise and the tone crosses the (negative) $160mV_{PEAK}$ detection threshold and the 25% duty cycle requirement is exceeded. Therefore, a conservative value for the minimum signal at the filter's output can be set to $320mV_{PEAK}$ or $226mV_{RMS}$, but a value of $200mV_{RMS}$ was established experimentally. Therefore, the minimum input signal for reliable tone detection in the presence of the maximum input noise spectral density is:

$$V_{IN(MIN)} = 200mV_{RMS}/Gain$$

For optimum tone detection, the signal's frequency should be in the filter's passband, within ±0.1% of f_{CENTER}.

Conclusion

A very selective bandpass filter, the LTC1164-8, can be configured as a nonphase-sensitive tone detector. This allows signals to be detected in the presence of comparatively large amounts of noise or signal-to-noise ratios that are less than unity.

BANDPASS FILTER HAS ADJUSTABLE Q

by Frank Cox

The bandpass filter circuit shown in Figure 30 features an electronically controlled Q. Q for a bandpass filter is defined as the ratio of the 3dB pass bandwidth to the stop bandwidth at some specified attenuation. The center frequency of the bandpass filter in this example is 3MHz, but this can be adjusted with appropriate LC tank components. The upper limit of the usable frequency range is about 10MHz. The width of the passband is adjusted by the current into Pin 5 (set current or I_{SET}) of the transconductance amplifier segment of IC1, an LT1228. Figure 31 is a network analyzer plot of frequency response versus set current. This plot shows the variation in Q while the center frequency and the passband gain remain relatively constant.

The circuit's operation is best understood by analyzing the closed-loop transfer function. This can be written in the form of the classic negative feedback equation:

$$H(s) = \frac{A(s)}{1 + A(s)\,B(s)}$$

where A(s) is the forward gain and B(s) is the reverse gain. The forward gain is the product of the transconductance stage gain (g_m) and the gain of the CFA (A_{CFA}). For this circuit, g_m is ten times the product of I_{SET} and the impedance of the tank circuit as a function of frequency. This gives the complete expression for the forward gain as a function of frequency:

$$A(s) = 10\, I_{SET}\, A_{CFA}\left(\frac{sL}{1 + s^2\, LC}\right)$$

The reverse gain is simply:

$$B(s) = \frac{R7}{R6 + R7}$$

$$\text{and } A_{CFA} = \frac{R4 + R5}{R4}$$

$$\text{Setting } B(s) = \frac{1}{A_{CFA}}\, R_{RATIO}$$

and substituting these expressions into the first equation gives:

$$H(s) = \frac{1}{R_{RATIO}} \cdot \frac{10\, I_{SET}\left(\frac{sL}{1 + s^2\, LC}\right)}{1 + 10\, I_{SET}\left(\frac{sL}{1 + s^2\, LC}\right)}$$

The last equation can be rewritten as:

$$H(s) = \frac{1}{R_{RATIO}} \cdot \frac{S\left[\frac{1}{\sqrt{LC}}\left(\frac{10\, I_{SET}\sqrt{LC}}{C}\right)\right]}{S^2 + S\left[\frac{1}{\sqrt{LC}}\left(\frac{10\, I_{SET}\sqrt{LC}}{C}\right)\right] + \frac{1}{LC}}$$

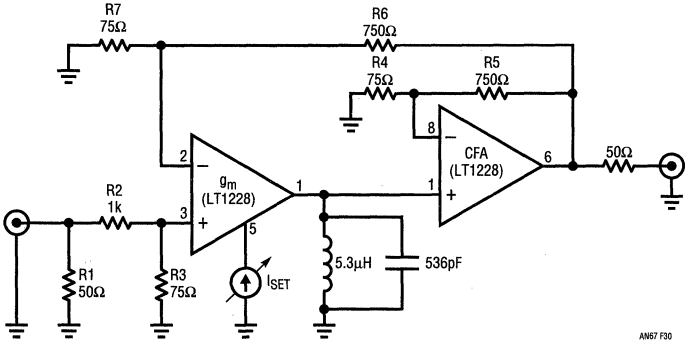


Figure 30. LT1228 Bandpass Filter Circuit Diagram

The transfer function of a second order bandpass filter can be expressed in the form[1]:

$$H(s) = H_{BP} \frac{S(\omega_O/Q)}{S^2 + S(\omega_O/Q) + \omega_O^2}$$

Comparing the last two equations note that

$$\omega_O = \frac{1}{\sqrt{LC}} \text{ and } \frac{1}{Q} = \frac{10\, I_{SET}\sqrt{LC}}{C}$$

$$\text{And therefore } Q = \frac{C}{10\, I_{SET}\sqrt{LC}}$$

It can be seen from the last equation that the Q is inversely proportional to the set current.

Many variations of the circuit are possible. The center frequency of the filter can be tuned over a small range by the addition of a varactor diode. To increase the maximum realizable Q, add a series LC network tuned to the same frequency as the LC tank on Pin 1 of IC1. To lower the minimum obtainable Q, add a resistor in parallel with the tank circuit. To create a variable Q notch filter, connect the inductor and capacitor at Pin 1 in series rather than in parallel.

A variable Q bandpass filter can be used to make a variable bandwidth IF or RF stage. Another application for this circuit is as a variable-loop filter in a phase locked loop phase demodulator. The variable Q bandpass filter is set for a wide bandwidth while the loop acquires the signal and is then adjusted to a narrow bandwidth for best noise performance after lock is achieved.

[1]Thanks to Doug La Porte for this equation hack.

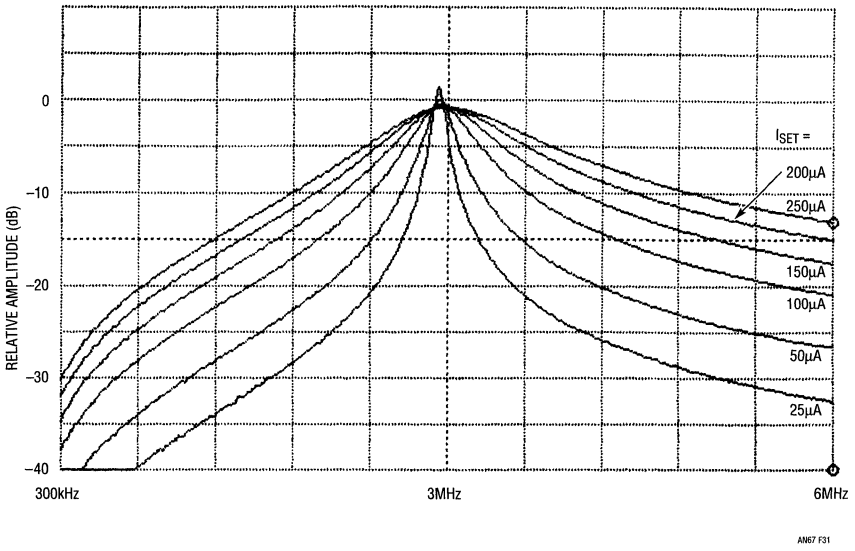


Figure 31. Network Analyzer Plot of Frequency Response vs "Set" Current

AN ULTRASELECTIVE BANDPASS FILTER WITH ADJUSTABLE GAIN

by Philip Karantzalis

Introduction

The LTC1164-8 is a monolithic, ultraselective, eighth order elliptic bandpass filter. The passband of the LTC1164-8 is tuned with an external clock; the clock-to-center-frequency ratio is 100:1. The stopband attenuation of the LTC1164-8 is greater than 50dB for input frequencies outside a narrow band defined as ±4% of the center frequency of the filter (see Figure 32).

One Op Amp and Two Resistors Build an Ultraselective Filter

The LTC1164-8 requires an external op amp and two external resistors. The filter's gain at its center frequency is equal to $3.4R_F/R_{IN}$. For optimum dynamic range with a gain equal to one, the external resistor R_F should be 90.9k and the external resistor R_{IN} should be 340k. For gains other than 1, R_{IN} = 340k/gain. Gains of up to 1000 are possible. The complete configuration is shown in Figure 33. Note that programming the filter's gain with input resistor R_{IN} is equivalent to providing the LTC1164-8 with noiseless preamplification, since the filter's internal noise is not amplified. The wideband noise of the LTC1164-8 measures $400\mu V_{RMS}$ at ±5V and is independent of the filter's gain and center frequency. A capacitor, C_F, across resistor R_F reduces clock feedthrough and provides a smooth sine wave output.

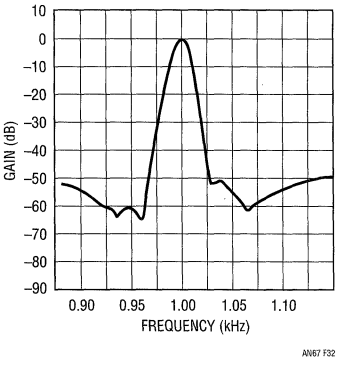


Figure 32. LTC1164-8 Gain vs Frequency Response

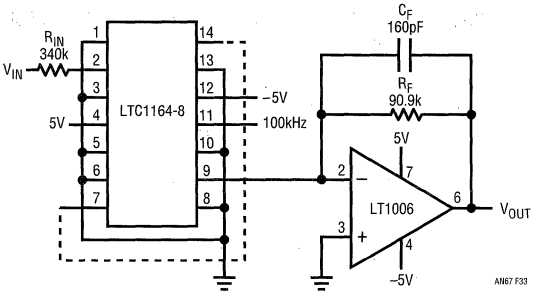


Figure 33. LTC1164-8 Ultranarrow, 1kHz Bandpass Filter with Gain (Gain = 340k/R_{IN}, $1/2\pi R_F C_F$ = 10 f_{CENTER})

Signal Detection in a Hostile Environment

An outstanding feature of the LTC1164-8 is its ultraselectivity. A bandpass filter with ultraselectivity is ideal for signal detection applications. One signal detection application occurs when two signals are very closely spaced in the frequency spectrum and only one of the signals has useful information. The LTC1164-8 can extract the signal of interest and suppress its unwanted neighbor. For example, a small 1kHz, $10mV_{RMS}$ signal is combined with an unwanted 950Hz, $40mV_{RMS}$ signal. The two signals differ in frequency by only 5% and the 950Hz signal is four times larger than the 1kHz signal. To detect the 1kHz signal, the LTC1164-8 is set to a gain of 100 and the clock frequency is set to 100kHz. At the filtered output of the LTC1164-8 the following signals will be present: an extracted 1kHz, $1V_{RMS}$ signal and a rejected 950Hz, $2.7mV_{RMS}$ signal, as shown in Figure 34. In a narrowband signal separation and extraction application, as described previously, the LTC1164-8 provides a simple and reliable detection circuit solution.

A second signal detection application occurs when a small signal is to be detected in the presence of noise. For example, a 1kHz, $10mV_{RMS}$ signal is mixed with a wideband noise signal that measures $5mV_{RMS}$ in a 400Hz frequency band. The signal-to-noise ratio is just 6dB. With the LTC1164-8 set for a center frequency of 1kHz (f_{CLK} is equal to 100kHz) and a gain of 100, the 1kHz, $10mV_{RMS}$ signal will be detected and amplified. The wideband noise will be band limited by the very narrow band gain response of the LTC1164-8. At the output of a LTC1164-8, the 1kHz signal will be $1V_{RMS}$ as shown in Figure 35. The total band limited

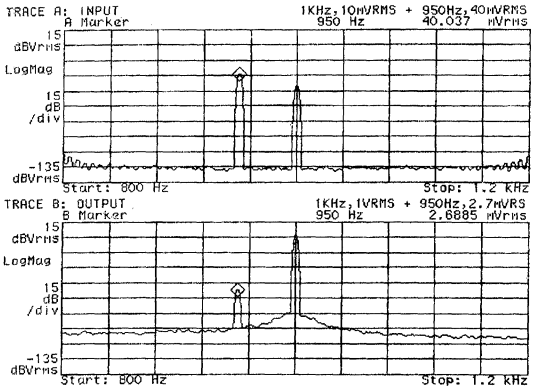


Figure 34. Narrow Band Signal Extraction Showing Input to and Output from the LTC1164-8 Filter. Filter f_{CENTER} set to 1kHz with Gain = 100

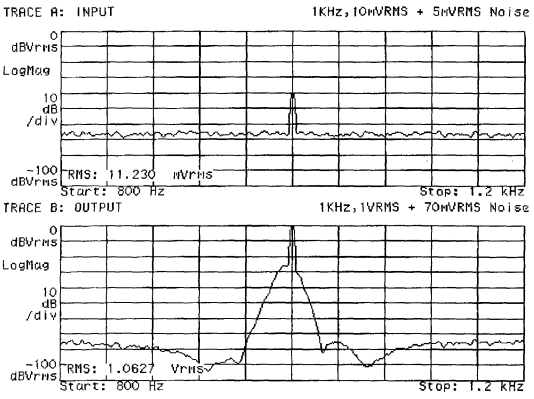


Figure 35. Signal Detection in the Presence of Noise Example Showing Input to and Output from the LTC1164-8 Filter. Filter f_{CENTER} set to 1kHz with Gain = 100

noise will be 70mV$_{RMS}$ with a signal-to-noise ratio of more than 20dB, as shown in Figure 36. In applications of signal detection in the presence of noise, the LTC1164-8 provides asynchronous detection. Signal detection circuits such as synchronous demodulators and lock-in amplifiers require the presence of a reference or carrier signal to provide phase and frequency information of the signal to be detected. With an LTC1164-8, signal detection is accomplished by selecting a very narrow signal detection band around the frequency of the desired signal, which is defined as f_{CLK} divided by 100 (f_{CLK} is the clock frequency of the LTC1164-8), and by selecting the filter gain by choosing the value of a resistor.

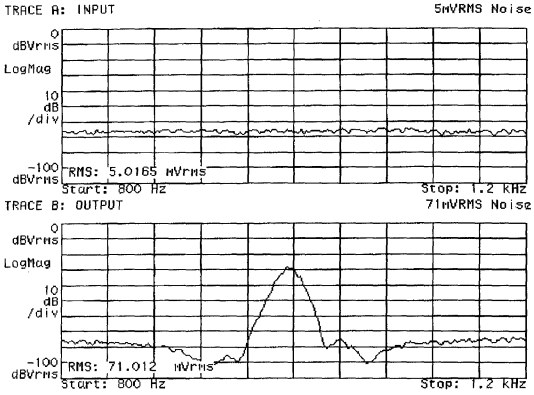


Figure 36. Wideband Noise Input to LTC1164-8 Filter. Plots Show Input to and Output from the Filter. Filter f_{CENTER} set to 1kHz with Gain = 100

LT1367 BUILDS RAIL-TO-RAIL BUTTERWORTH FILTER

by William Jett and Sean Gold

Single Supply 1kHz, 4th Order Butterworth Filter

The circuit shown in Figure 37 takes advantage of all four op amps in the LT1367 to form a 4th order Butterworth filter. The filter is a simplified state-variable architecture consisting of two cascaded second order sections. Each section uses the 360 degree phase shift around the two op amp loop to create a negative summing junction at A1's positive input.[1] The circuit has two-thirds the power dissipation and component count as the classic three op amp biquad,[2] yet it has the same low component sensitivities for center frequency, ω_0 and Q.

For cutoff frequencies other than the 1kHz example shown, use the following formula for each section:

$\omega_0^2 = 1/(R1\ C1\ R2\ C2)$,

where $R1 = 1/(\omega_0\ Q\ C1)$ and $R2 = Q/(\omega_0 C2)$

The DC bias applied to A2 and A4 for single supply operation is not needed when split supplies are available. The circuit's output can swing rail-to-rail and displays the maximally flat amplitude response with a 1kHz cutoff frequency with 80dB/decade rolloff (Figure 38).

[1] Hahn, James. 1982. State Variable Filter Trims Predecessor's Component Count. *Electronics*, April 21, 1982.

[2] Thomas, L.C. 1971. The Biquad: Part I—Some Practical Design Considerations. *IEEE Transactions on Circuit Theory*, 3:350-357, May 1971.

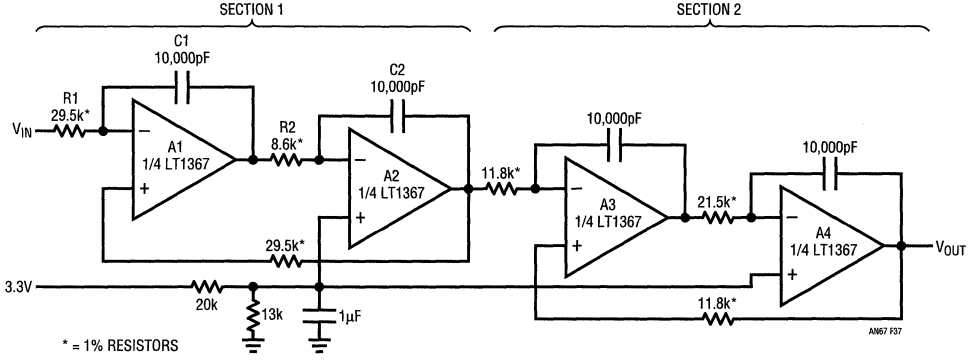


Figure 37. 1kHz 4th Order Butterworth Filter

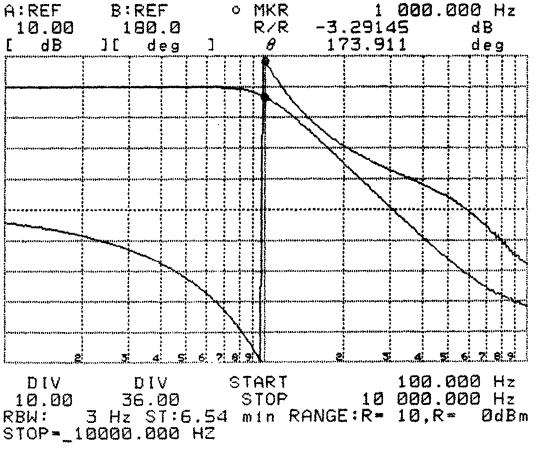


Figure 38. Frequency Response of 4th Order Butterworth Filter

DC ACCURATE, CLOCK TUNABLE LOWPASS FILTER WITH INPUT ANTIALIASING FILTER

by Philip Karantzalis

In a sampled data system, the sampling theorem says that if an input signal has any frequency components greater than one half the sampling frequency, aliasing errors will appear at the output. In practice aliasing is not always a serious problem. High order switched capacitor lowpass filters are band limited and significant aliasing occurs only for input signals centered around the clock frequency and its multiples.

Figure 39 shows the LTC1066-1 aliasing response when operated with a clock-to-f_C ratio of 50:1. With a 50:1 ratio, the LTC1066-1 samples its input twice during one clock period and the effective sampling frequency is twice the clock frequency. Figure 39 shows that the maximum aliased output is generated for inputs in the range of $2(f_{CLK} \pm f_C)$. (f_C is the cutoff frequency of the LTC1066-1.) For instance, if the LTC1066-1 is programmed to produce a cutoff frequency of 20kHz with a 1MHz clock, maximum aliasing will occur only for input signals in the narrow range of 2MHz ±20kHz and its multiples.

The simplest antialiasing filter is a passive 1st order lowpass RC filter. The –3dB frequency of the RC filter should be chosen so that the passband of the RC filter does not influence the passband of the LTC1066-1. When the LTC1066-1 clock frequency is 500kHz, an RC filter with the –3dB frequency set at 50kHz attenuates by 26dB any

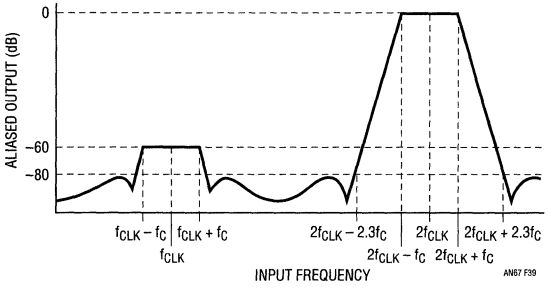


Figure 39. Aliasing vs Frequency f_{CLK}/f_C = 50:1 (Pin 8 to V⁺); Clock is a 50% Duty Cycle Square Wave

possible aliasing inputs in the range 1MHz ±10kHz. The passband shape of the 50kHz RC filter does not degrade the flat passband of the LTC1066-1 at 10kHz (the passband attenuation of the 50kHz RC filter for frequencies less than 10kHz is less than 0.2dB). If the LTC1066-1 is clock tuned to a cutoff frequency of 5kHz (with a clock frequency of 250kHz), the 50kHz RC filter will provide 20dB attenuation for aliasing inputs in the range of 500kHz ±5kHz. Therefore, a 1st order lowpass RC filter will attenuate all aliasing signals to the LTC1066-1 by a minimum of 20dB for a clock tunable range of one octave.

For added antialiasing bandwidth, a 1st order lowpass RC filter can be tuned by the clock signal of LTC1066-1 to follow the cutoff frequency of the higher order filter. The circuit is shown in Figure 40. The circuit operation is as follows. The six comparators inside the LTC1045 detect the clock frequency. The clock signal of the LTC1066-1 is converted to a pulse output whose duty cycle changes with clock frequency. The average voltage of the pulse signal is delivered to a 4-window comparator whose outputs drive the four analog switches of the LTC202. When the LTC1066-1 clock frequency increases or decreases by more than one octave (2x or x/2), a capacitor is switched in or out of the 1st order lowpass filter formed by resistor R1 (1k) and capacitor C1. The –3dB frequency of the lowpass RC filter is therefore doubled or halved if the cutoff frequency of the LTC1066-1 is doubled or halved. Resistor R1 and capacitors C1 through C5 allow the lowpass RC filter to be tuned over a range of five octaves, providing at least 20dB attenuation to any LTC1066-1 input signals in the range $2(f_{CLK} \pm f_C)$ (the RC filter also attenuates all aliasing signals near any multiples of the clock frequency).

The circuit in Figure 40 can be used for any clock tunable, 5-octave range for cutoff frequencies from 10Hz to 80kHz (with ±5V supplies for LTC1066-1) or for cutoff frequencies as high as 100kHz (with ±8V supplies for the LTC1066-1). For cutoff frequencies greater than 50kHz, a 15pF capacitor in series with a 30k resistor should be connected between Pins 11 and 13 of the LTC1066-1 to minimize passband gain peaking.

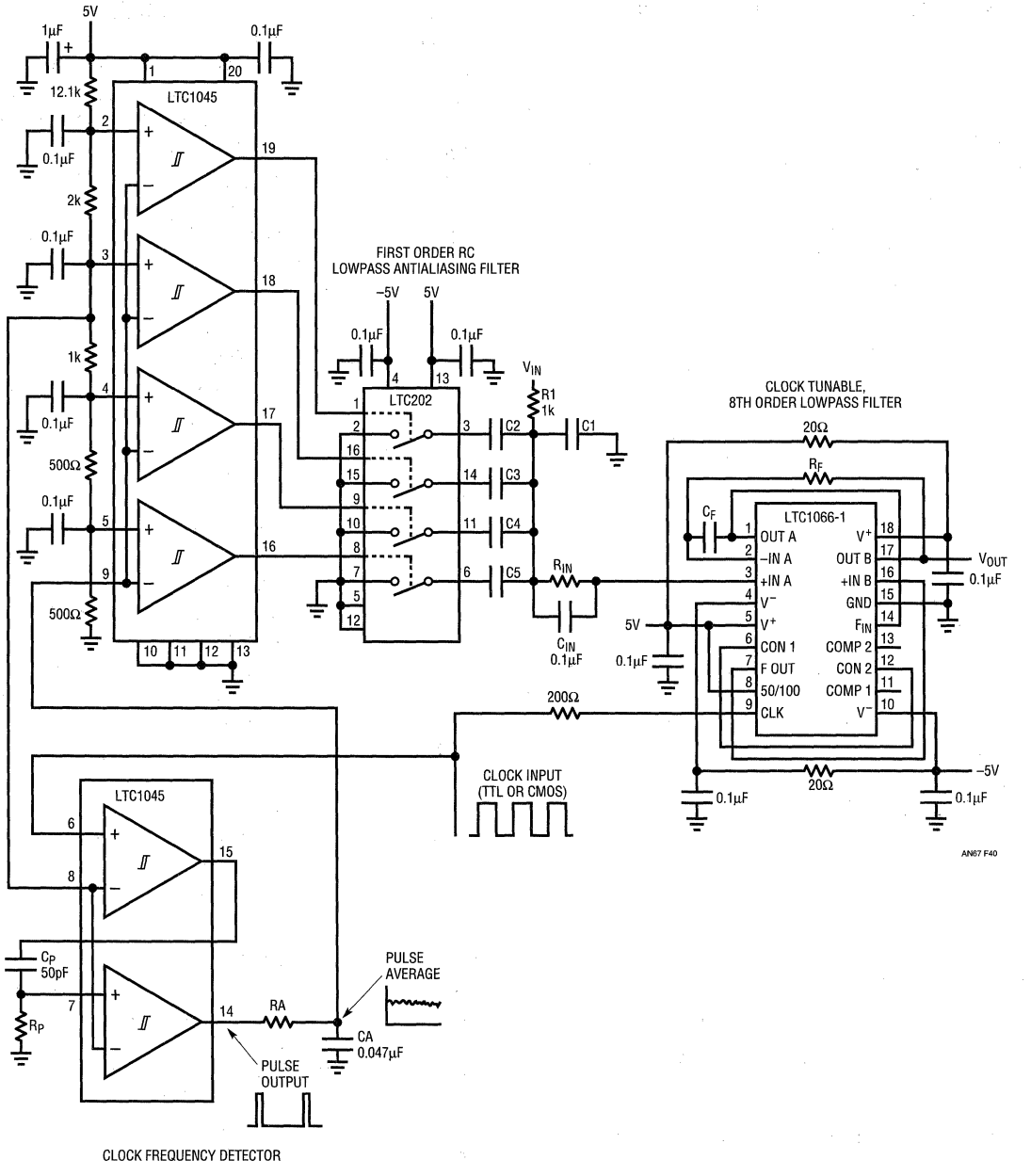


Figure 40. DC-Accurate, Clock-Tunable Lowpass Filter with Input Antialiasing

Use the following design guide for choosing the component values of R_A, R_P, R_F, R_{IN}, C_F, C1 through C5, C_P and C_A.

Definitions

1. The cutoff frequency of the LTC1066-1 is abbreviated as f_C.
2. $f_{C(LOW)}$ is the lowest cutoff frequency of interest
3. A range of five octaves is from $f_{C(LOW)}$ to $32 \bullet f_{C(LOW)}$

Component Calculations

$$\frac{1}{2\pi R_F C_F} = \frac{f_{C(LOW)}}{250}$$ $R_{IN} = R_F$ (If R_F can be chosen as 20k, R_{IN} and C_{IN} are not needed)

$$C1 = \frac{1}{f_{C(LOW)}}$$ ($f_{C(LOW)}$ in Hz); R1 = 1k

C2 = C1 ±5%, C3 = 2(C1) ±5%, C4 = 4(C1) ±5%, C5 = 8(C1) ±5%

$$C_P = 50pF,\ R_P = \frac{10^5}{50\ f_{C(LOW)}}\ k$$

$$C_A = 0.047\mu F,\ R_A = \frac{5(10^5)}{50\ f_{C(LOW)}}\ k$$

Example

For a five octave range from 1kHz to 32kHz:

$f_{C(LOW)}$ = 1kHz

Let C_F = 1µF ±20%, then R_F = 40.2k ±1%. $R_{IN} = R_F$ = 40.2k ±1%, C_{IN} = 0.1µF

C1 = 0.001µF ±5%, C2 = 0.001µF ±5%, C3 = 0.0022µF ±5%

C4 = 0.0039µF ±55, C5 = 0.0082µF ±5%

C_P = 50pF, R_P = 2k, C_A = 0.047µF, R_A = 10k

THE LTC1066-1 DC ACCURATE ELLIPTIC LOWPASS FILTER

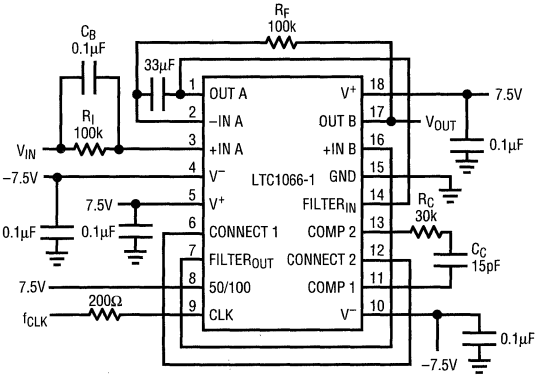
by Nello Sevastopoulos

Figure 41 shows an application allowing clock tunability from 10Hz to 100kHz. The R_CC_C frequency compensating components (needed only for cutoff frequencies above 60kHz) maintain a flat passband for cutoff frequencies between 50kHz and 100kHz. The input resistor, R_I, reduces the output DC offset caused by the op amp bias current through the 100k feedback resistor, R_F. The measured DC offset and the gain nonlinearity are 4mV and ±0.0063% (84dB), respectively. The 0.1µF bypass capacitor, C_B, helps keep the total harmonic distortion of the filter from being degraded by the 100k input resistor.

Clock Tunability

An external clock tunes the cutoff frequency of the internal switched capacitor network. The device has been optimized for a clock-to-cutoff-frequency ratio of 50:1. The internal double sampling greatly reduces the risk of aliasing.

The maximum obtainable cutoff frequency, $f_{CUTOFF(MAX)}$, depends on power supply, clock duty cycle and temperature; $f_{CUTOFF(MAX)}$ does not depend on the value of the external resistor/capacitor combination R_FC_F. The R_CC_C compensation is shown in Figure 41. The data detailed in



MAXIMUM OUTPUT VOLTAGE OFFSET = 4mV, DC LINEARITY = ±0.0063%, T_A = 25°C.
THE PIN 6 TO 12 CONNECTION SHOULD BE UNDER THE IC AND SHIELDED BY AN ANALOG SYSTEM GROUND PLANE.
RC COMPENSATION BETWEEN PINS 11 AND 13 REQUIRED ONLY FOR f_{CUTOFF} > 50kHz.
THE 33µF CAPACITOR IS A NONPOLARIZED, ALUMINUM ELECTROLYTIC, ±20%, 16V (NICHICON UUPIC 330MCRIGS OR NIC NACEN 33M16V 6.3 × 5.5 OR EQUIVALENT).

AN67 F41

Figure 41. DC Accurate, 10MHz to 100kHz 8th Order Elliptic Lowpass Filter, f_{CLK}/f_C = 50:1

Figure 42 reveals the important fact that for a cutoff frequency of 100kHz, the stopband attenuation still remains greater than 70dB for input frequencies up to 1MHz.

The minimum obtainable cutoff frequency depends on the R_FC_F time constant of the servo loop. For a given R_FC_F time constant, the minimum obtainable cutoff frequency of the LTC1066-1 is:

$$f_{CUTOFF(MIN)} = 250(1/2\pi R_FC_F).$$

$$f_{CUTOFF(MAX)} = 100kHz$$

For instance, if $R_F = 20k$, $C_F = 1\mu F$, $f_{CUTOFF(MIN)} = 2kHz$, and $f_{CLOCK(MIN)} = 100kHz$.

Under these conditions, a clock frequency below 100kHz will "warp" the passband gain by more than 0.1dB. Please see the LTC1066-1 data sheet for more details.

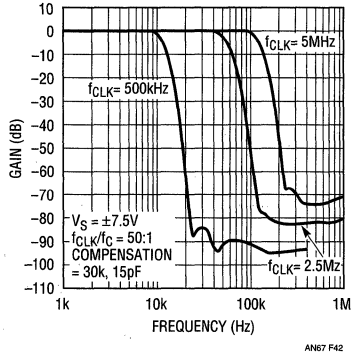


Figure 42. LTC1066-1 Amplitude vs Frequency

Dynamic Range

The LTC1066-1 wideband noise is $100\mu V_{RMS}$. Figure 43 shows the noise plus distortion versus RMS input voltage at 1kHz. With a ±5V supply, the filter can swing ±2.5V (5V full scale) with better than 0.01% distortion plus noise. The maximum signal-to-noise ratio, in excess of 90dB, is achieved with ±7.5V supplies. Unlike previous monolithic filters the data shown in Figure 43 is taken without using any input or output op amp buffers. The output buffer of the LTC1066-1 can drive a 200Ω load without dynamic range degradation.

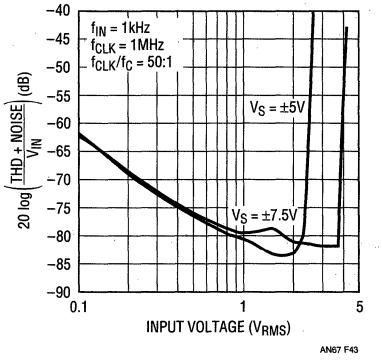


Figure 43. LTC1066-1 Dynamic Range

Aliasing and Antialiasing

All sampled data systems will alias if their input signals exceed half the sampling rate, but aliasing for high order, band limited, switched capacitor filters need not be a serious problem. The LTC1066-1, when operating with a 50:1 clock-to-cutoff-frequency ratio, will have significant aliasing only for input signals centered around twice the clock frequency and its even multiples. Figure 44 shows the input frequencies that will generate aliasing at the filter output. For instance, if the filter is tuned to a 50kHz cutoff frequency using a 2.5MHz clock, significant aliasing will occur only for input frequencies of 5MHz ±50kHz. The filter user should be aware of the spectrum at the input to the filter. Next, an assessment should be made as to whether a simple, continuous-time antialiasing filter in front of the LTC1066-1 is required. The antialiasing filter should do precisely what it is meant to do, that is, provide

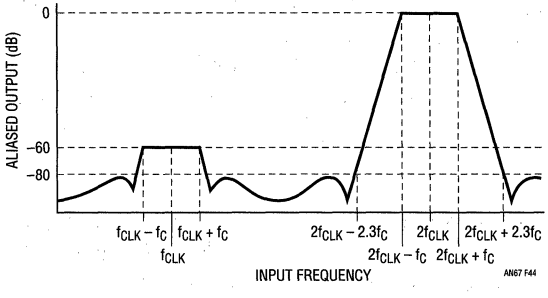


Figure 44. Aliasing vs Frequency f_{CLK}/f_C = 50:1 (Pin 8 to V+). Clock is a 50% Duty Cycle Square Wave

band limiting. The antialiasing filter should not degrade the DC or AC performance of the LTC1066-1.

For fixed cutoff frequency applications, the antialiasing function is quite trivial. Figure 45 shows the internal precision input op amp configuration used to perform both the DC accurate function of the LTC1066-1 and the input antialiasing configuration. The cutoff frequency of the RC antialiasing filter is set three times higher than the cutoff frequency of the LTC1066-1. For the example shown in Figure 45 the input antialiasing filter provides a 62dB attenuation at twice the clock frequency of the switched capacitor filter.

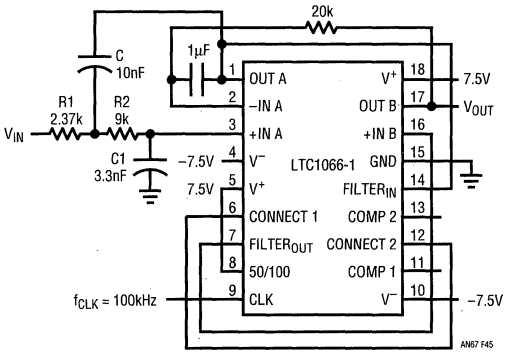
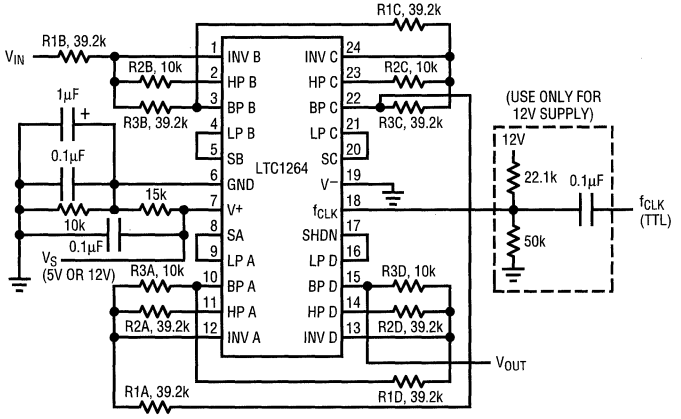


Figure 45. Adding a 2-Pole Butterworth Input Antialiasing Filter. Set C1 = 0.33C, R2 = 3.8(R1); f–3dB (Input Antialiasing) = 0.8993/(2πR1C)

CLOCK TUNABLE BANDPASS FILTER OPERATES TO 160kHz IN SINGLE SUPPLY SYSTEMS

by Philip Karantzalis

When the only available power supply in a system is 5V or 12V and a precision bandpass filter is needed at cutoff frequencies greater than 20kHz, the LTC1264 switched capacitor active filter building block can be configured to realize an 8th order bandpass filter accurate to ±1% or better over temperature (–40°C to 85°C). Figure 46 is a schematic diagram of an 8th order bandpass filter tunable with a TTL clock signal to any center frequency up to 70kHz with a 5V supply or to 100kHz with a 12V supply. The clock frequency-to-center frequency ratio is 20:1. The gain response for a 50kHz bandpass filter is shown in Figure 47 and the input dynamic range with a 5V supply is shown in Figure 48.



V_S	f_{CENTER}	R1 (EACH SECTION)
5V	80kHz	42.2k
5V	90kHz	47.5k
12V	120kHz	40.2k
12V	140kHz	42.2k
12V	160kHz	47.5k

Figure 46. Single Supply Bandpass Filter

The passband frequency range (the frequency range where the filter's attenuation is 3dB or less) is equal to the center frequency divided by ten. The stopband attenuation reaches 60dB at twice the center frequency and at one-half the center frequency. The typical gain variation at the center frequency is ±0.5dB at 25°C and ±1.5dB over temperature. (Note that an additional ±0.4dB should be added to account for the gain variation due to the 1% resistors). If the operating temperature range is 25°C (±20°C) and the power supply voltage can be controlled to ±2%, the center frequency can be extended to 90kHz for a 5V supply or 160kHz for a 12V supply. Note that the gain error for center frequencies greater than 70kHz with a 5V supply and greater than 100kHz with a 12V supply increases from 1dB to 7dB. Therefore, the value of resistor R1 for each LTC1264 section should be increased to reduce the error to ±1dB (see the table in Figure 46).

If the power supply for this filter is a switching regulator, the regulator's output noise can appear at the filter's output if the center frequency of the filter is tuned to the noise frequency of the regulator. This is due to the filter's low power supply rejection near its center frequency. The LTC1264 is not a low power device. The typical quiescent current is 11mA with a 5V supply or 18mA with a 12V supply.

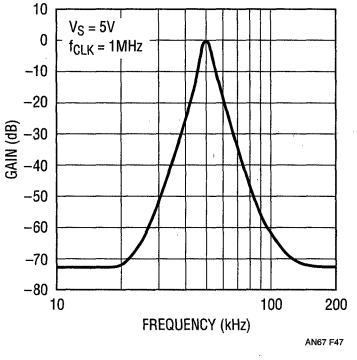


Figure 47. LTC1264 Single 5V Supply, 50kHz Bandpass Response

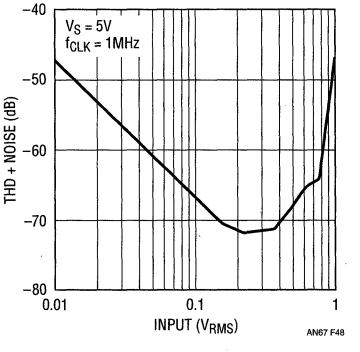


Figure 48. Dynamic Range vs Input Signal. LTC1264 Single 5V Supply, 50kHz Bandpass Filter

A LINEAR-PHASE BANDPASS FILTER FOR DIGITAL COMMUNICATIONS

By Philip Karantzalis

Bandpass filters with linear passband phase are useful for a variety of data-communications tasks, the most noteworthy of which may be in modulation-demodulation (modem) circuitry. Modems generate signals that must be processed without phase distortion to allow error free transmission and reception of information (or the closest approach to that ideal we can achieve).

Figure 49 shows a linear-phase bandpass filter using the LTC1264 high frequency, universal switched capacitor filter building block. This filter is an 8th order narrow bandpass filter, centered at 50kHz for a 1MHz clock input, with flat group delay in its passband. The f_{CLK}-to-f_{CENTER} frequency ratio is 20:1. Figure 50 shows the filter's narrowband gain response and Figure 51 shows the passband group delay.

An interesting feature of linear-phase bandpass filters is that their response to a step input produces a short transient sine wave burst with a symmetrical envelope. Figure 52 shows a comparison of the transient responses to a step input for the linear-phase bandpass filter of

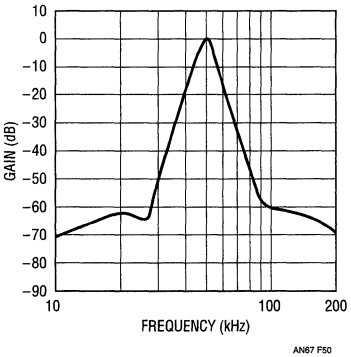


Figure 50. Filter Gain vs Frequency

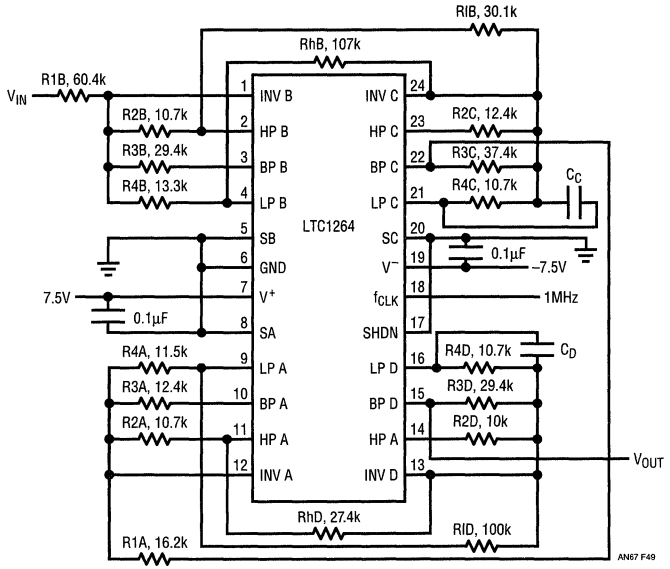


Figure 49. LTC1264 Linear Phase, 8th Order Bandpass Filter

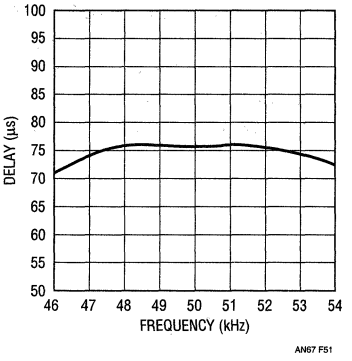


Figure 51. Filter Group Delay vs Frequency

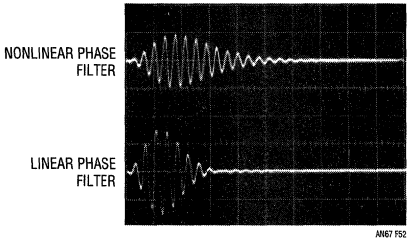


Figure 52. Step Response

Figure 49 and a bandpass filter with a similar passband and nonlinear phase response. The response of a bandpass filter to a step input is a simple qualitative test for determining the linearity of its phase response, although in data transmission systems the measurements are usually made with eye diagrams and constellation displays.

The maximum clock frequency for the filter is 2MHz with ±7.5V supplies. This allows bandpass filters with center frequencies up to 100kHz to be realized without significant phase distortion in the passband.

Capacitor C, across R4 in sections C and D, minimizes gain and phase variations when the filter is used with clock frequencies greater than 1.4MHz. For ±5V supplies the maximum clock frequency is 1.6MHz. Use the Table 1 as a guide for the selection of capacitor C.

Table 1. Capacitor Selection Guide

V_S	f_{CLK}	$C_C = C_D$
±7.5V	1.8MHz	3pF
	2.0MHz	5pF
±5V	1.6MHz	5pF
	1.4MHz	3pF

Instrumentation

WIDEBAND RMS NOISE METER

by Mitchell Lee

Recently, I needed to measure and optimize the wideband RMS noise of a power supply over about a 40MHz bandwidth. A quick calculation showed that the 12nV to 15nV/$\sqrt{Hz}$ noise floor of my spectrum analyzer would come up short—my circuit was predicted to exhibit a spot noise of perhaps 8nV to 10nV/$\sqrt{Hz}$. In fact, I didn't have a single instrument in my lab that would measure 50μV_{RMS} to 60μV_{RMS}.

For the 40MHz bandwidth, the HP3403C RMS voltmeter is a good choice but its most sensitive range is 100mV, about 66dB shy of my requirement. This obsolete instrument today carries a hefty price on the used market. The fact that here in the Silicon Valley HP3403Cs are a common sight at flea markets is of little consolation to most customers wishing to reproduce my measurements. We have several of these meters in the LTC design lab but they are in constant use and closely guarded by "The Keepers of the Secret RMS Knowledge." I resolved to build my own meter using an LT1088 thermal RMS converter.

Full scale on the LT1088 is 4.25V_{RMS}. To measure 50μV full scale, I'd need an amplifier with a gain of 100,000. At 40MHz bandwidth, this didn't sound like it would have a good chance of working first time—built by hand and without benefit of a custom casting.

Rather than build a circuit with 40MHz bandwidth and a gain of 100dB, I decided to use just enough gain to put my desired noise performance around twice minimum scale. Aside from gain, this amplifier would also need less than 5nV/$\sqrt{Hz}$ input noise, and the output stage would have to drive the 50Ω load presented by the LT1088.

It wasn't hard to find an appropriate output stage. The LT1206 (see Figure 53) can easily drive the required 120mA peak current into the LT1088 converter and there's plenty left over for handling noise spikes. To preserve 40MHz bandwidth, the LT1206 was set to run at a gain of 2.

The front end was harder to solve. I needed a low noise, high speed amplifier that could give me plenty of gain. Here I selected the LT1226. This is a 1GHz GBW op amp with only 2.6nV/$\sqrt{Hz}$ input noise. It has a minimum stable gain of 25 but in this circuit high gain is an advantage.

Cascading two LT1226s on the front end gives a gain of 625, a little shy of the 5,000 to 10,000 required. Another gain of 5, plus the gain of 2 in the LT1206 adds up to a gain of 6,250—just about right.

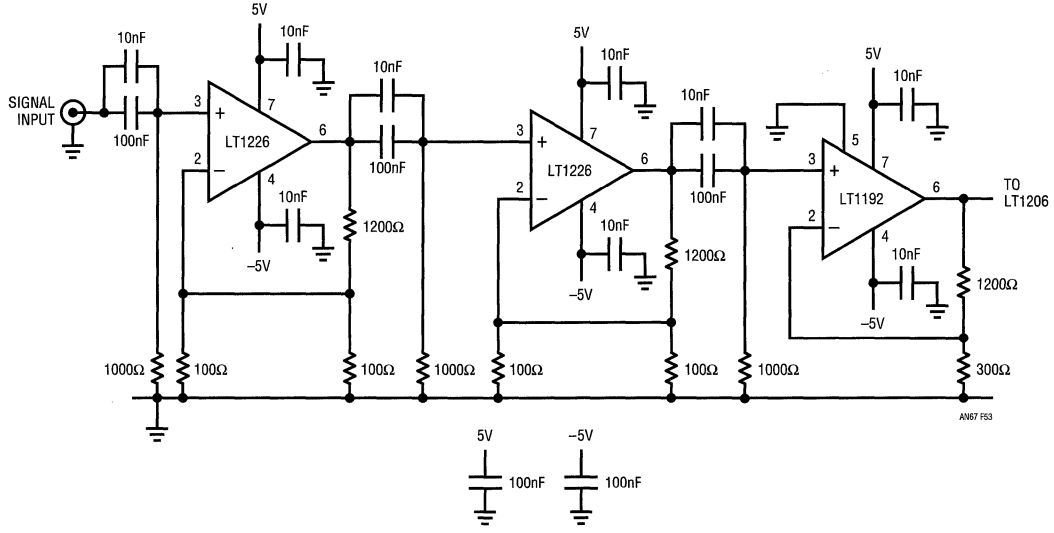


Figure 53 Noise Meter Gain Stage

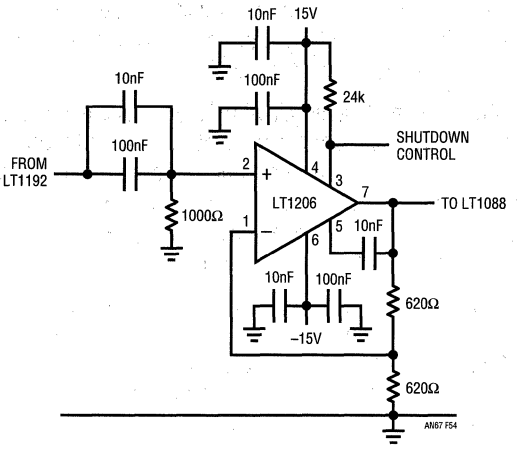


Figure 54. LT1206 Buffer/Driver Section

There are several ways to get 40MHz bandwidth at a gain of 5, including the LT1223 and LT1227 current feedback amplifiers, but I settled on the LT1192 voltage amplifier because it is the lowest cost solution. This brings the gain up to 6250, for a minimum scale sensitivity of 34μV_{RMS} and a full-scale sensitivity of 680μV_{RMS}.

My advice-filled coworkers assured me that there was no way I could build a wideband amplifier with a gain of 6250 and make it stable. Nevertheless, I built my amplifier on a 1.5" × 6" copperclad board, taking care to maintain a linear layout. The finished circuit was stable provided that a coaxial connection was made to the input. The amplifier was flat with 3dB points at 4kHz and 43MHz and some peaking at high frequencies.

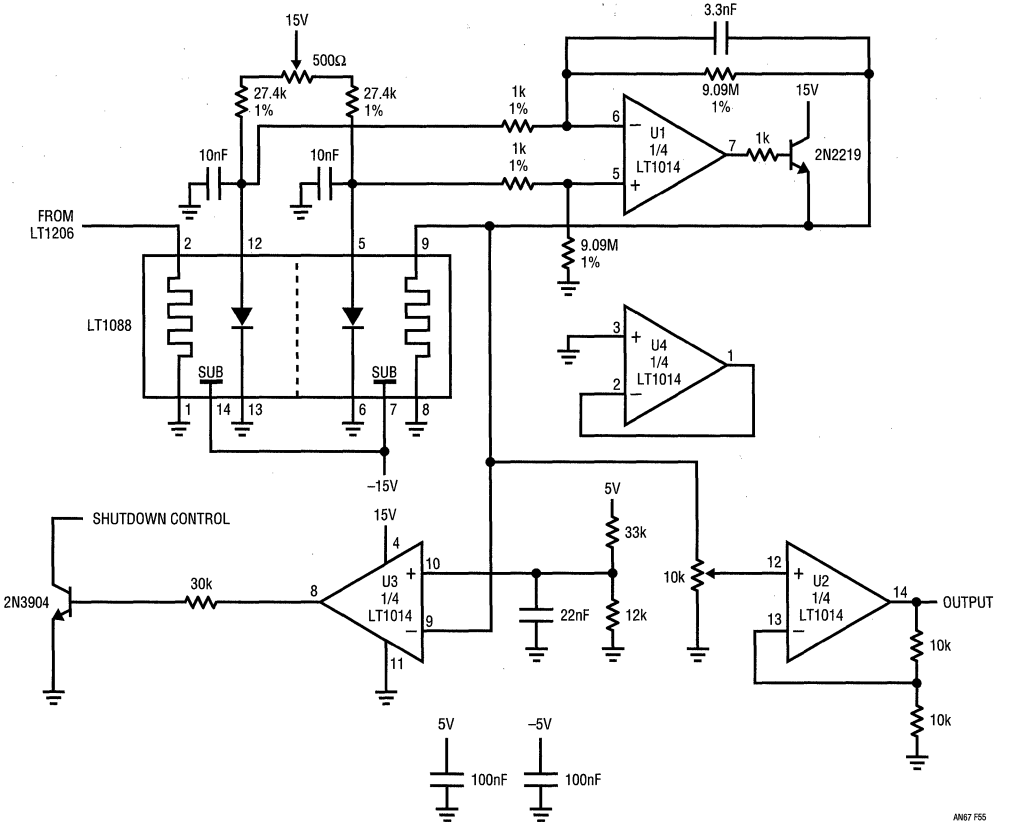


Figure 55. LT1088 RMS Detector Section

Coaxial Measurements

When measuring low level signals it is difficult to get a clean, accurate result. Scope probes have two problems. 10× probes attenuate the already small signal, and both 1× and 10× probes suffer from circuitous grounds. Coaxial adapters are a partial solution but these are expensive. They make for a lot of wear and tear on the probes and, without a little forethought, they can be a bear to attach to the circuit under test. My favorite way to get clean measurements of small signals is to directly attach a short length of coaxial cable as shown in Figure 56.

I use the good part of a damaged BNC cable, cutting away the shorter portion to leave at least 18" of RG-58/U and one good connector. At the cut, or as I call it, "real world" end of the cable, I unbraid, twist and tin a very small amount of outer conductor to form a stub 1/4" to 3/8" long. Next, I cut away the dielectric, exposing a similar length of center conductor, which I also tin. Now the probe is ready for use. It can be soldered directly to a circuit or breadboard, eliminating any lead length that might otherwise pick up stray noise, or worse, act as an antenna in a sensitive high gain circuit.

Small signals aren't the only beneficiaries of this technique. This works great for looking at ripple on the outputs of switching supplies. Ripple measurements are simplified because the large voltage swings associated with the switch node are completely isolated and no loop is formed where di/dt could inject magnetically coupled noise.

In some instances, I've found it important to retain the 50Ω termination impedance on the cable, but it is rarely possible to place a terminator at the "BNC" end of the cable, since this creates a DC path directly across the circuit under test. There is, however, another way as shown in Figure 57. Here, a technique known as back termination is used. No termination is used at the far end of the cable, but a 51Ω resistor is connected in series with the measurement end. Signals sent down the cable reach the BNC connector without attenuation, and fast edges that bounce off the unterminated end are absorbed back into the 51Ω source resistor. I've found this especially useful for measuring fast switch signals, or when measuring the RMS value of small signals, for ensuring that the amplifier input sees a properly terminated source. The resistor trick does not work if the node under test is high impedance; a FET probe is a better choice for high impedance measurements.

While I'm at it, I might as well give away my only other secret. We've all encountered ground loop problems, giving rise to 60Hz (50Hz for my friends overseas) injection into sensitive circuits. Every lab is replete with isolation transformers and "controlled substance" line cords with missing ground prongs for battling ground loops. There are similar problems at high frequencies, but the victim is wave fidelity, not AC pick up. To determine whether or not high frequency grounding, ground loops or common mode rejection is a problem for your oscilloscope, simply clamp a small ferrite E core around the probe lead while observing any effects on the waveform (see Figure 58). Sometimes the news is bad; the waveform really is messed up and there is some work to be done on the circuit. But occasionally the circuit is exonerated, the unexplainable aberrations disappear, proving that high frequency gremlins are at work. If necessary, several passes of the probe cable can be made through the E-Core and it can be taped together for as long as needed.

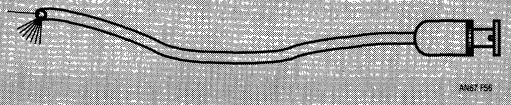


Figure 56. BNC Cable Used as a "Probe"

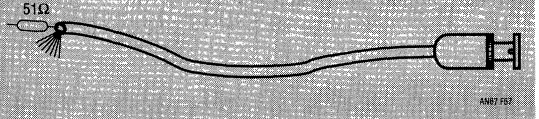


Figure 57. BNC Cable Probe Back Terminated

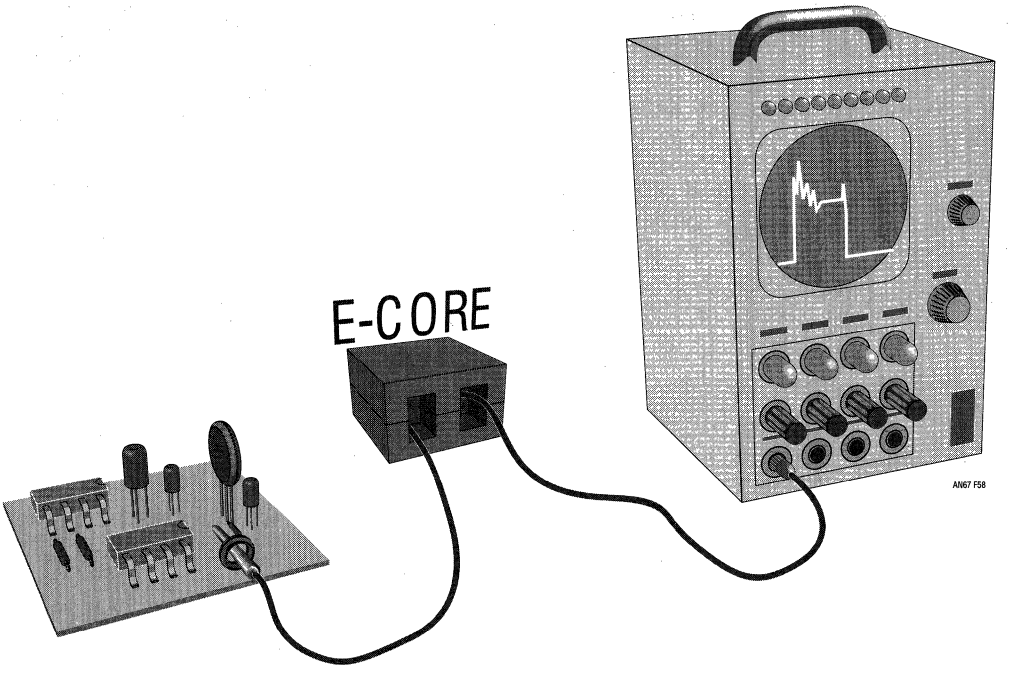


Figure 58. An E-Core Serves to Attenuate High Frequency Common Mode Currents from a Scope Probe

The performance of the amplifier and thermal converter can be optimized by adjusting the value of the feedback and gain setting resistors around the LT1206. Slightly more bandwidth can be achieved at the expense of higher peaking by reducing the resistor values 10%. Reducing the resistor values will decrease peaking effects at the expense of bandwidth. A good compromise value is 680Ω.

I've shown the LT1226 amplifiers operating from ±5 supplies, which puts their bandwidth on the edge at 40MHz. Their bandwidth can be improved by operating at ±15V.

Because the LT1206 operates on 15V rails, it is possible to overdrive the LT1088 and possibly cause permanent damage. One section of the LT1014 (U3) is used to sense an overdrive condition on the LT1088 and shut down the LT1206. Sensing the feedback heater instead of the input heater allows the LT1088 to accommodate high crest factor waveforms, shutting down only when the average input exceeds maximum ratings.

By the way, my power supply noise measured 200μV; filtering brought it down to less than 60μV.

LTC1392 MICROPOWER TEMPERATURE AND VOLTAGE MEASUREMENT SENSOR

by Ricky Chow and Dave Dwelley

The LTC1392 is a micropower data acquisition system designed to measure temperature, on-chip supply voltage and differential rail-to-rail common mode voltage. The device incorporates a temperature sensor, a 10-bit A/D converter, a high accuracy bandgap reference and a 3-wire half-duplex serial interface.

Figure 59 shows a typical LTC1392 application. A single point "star" ground is used along with a ground plane to minimize errors in the voltage measurements. The power supply is bypassed directly to the ground plane with a 1µF tantalum capacitor in parallel with an 0.1µF ceramic capacitor.

The conversion time is set by the frequency of the signal applied to the CLK pin. The conversion starts when the $\overline{CS}$ pin goes low. The falling edge of $\overline{CS}$ signals the LTC1392 to wake up from micropower shutdown mode. After the LTC1392 recognizes the wake-up signal, it requires an additional 80µs delay for a temperature measurement, or a 10µs delay for a voltage measurement, followed by a 4-bit configuration word shifted into D_{IN} pin. This word configures the LTC1392 for the selected measurement and initiates the A/D conversion cycle. The D_{IN} pin is then disabled and the D_{OUT} pin switches from three-state mode to an active output. A null bit is then shifted out of the D_{OUT} pin on the falling edge of the CLK, followed by the result of the selected conversion. The output data can be formatted as an MSB-first sequence or as an MSB-first followed by an LSB-first sequence, providing easy interface to either LSB-first or MSB-first serial ports. The minimum conversion time for the LTC1392 is 142µs in temperature mode or 72µs in the voltage conversion modes, both at the maximum clock frequency of 250kHz.

Conclusion

The LTC1392 provides a versatile data acquisition and environmental monitoring system with an easy-to-use interface. Its low supply current, coupled with space saving SO-8 or PDIP packaging, makes the LTC1392 ideal for systems that require temperature, voltage and current measurement while minimizing space, power consumption and external component count. The combination of temperature and voltage measurement capability on one chip makes the LTC1392 unique in the market, providing the smallest, lowest power multifunction data acquisition system available.

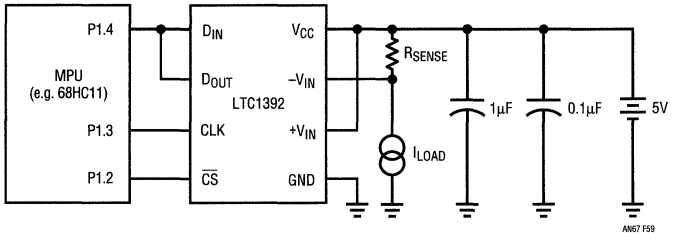


Figure 59. Typical LTC1392 Application

HUMIDITY SENSOR TO DATA ACQUISITION SYSTEM INTERFACE

by Richard Markell

Introduction

It can be difficult to interface humidity sensors to data acquisition systems because of the sensors' drive requirements and their wide dynamic range. By carefully selecting the devices that comprise the analog front end, users can customize the circuit to meet their humidity sensing requirements and achieve reasonable accuracy throughout the chosen range. This article details the analog front end interface between a Phys-Chem Scientific Corp.[1] model EMD-2000 humidity sensor and a user selected (probably microprocessor-based) data acquisition system.

Design Considerations

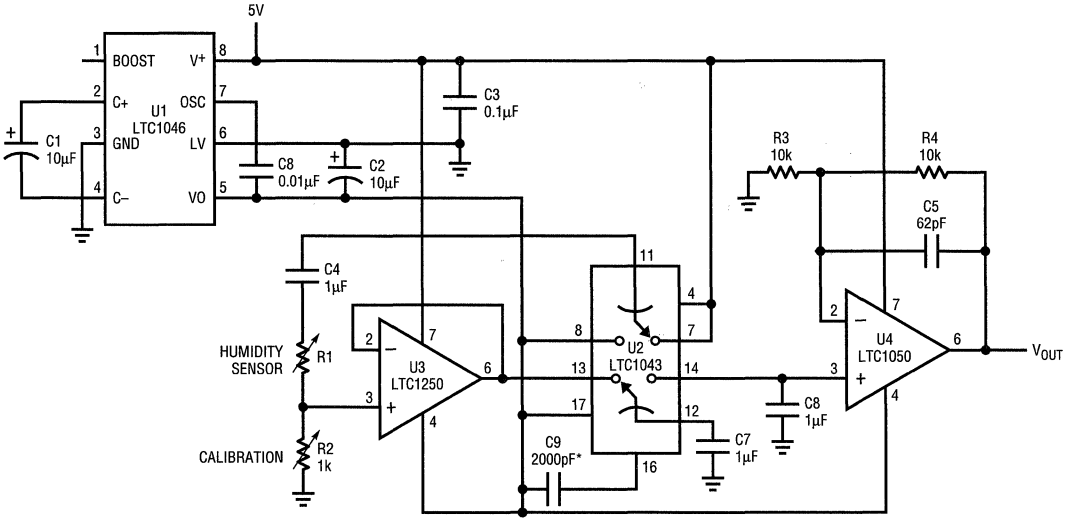
The Phys-Chem humidity sensor is a small, low cost, accurate resistance-type relative humidity (RH) sensor. This sensor has a well-defined stable response curve and can be replaced in circuit without system recalibration.

The design criteria call for a low cost, high precision analog front end that requires few calibration "tweaks" and operates on a single 5V supply. The sensor requires a square wave or sine wave excitation with no DC component. The sensor reactance varies over an extremely wide range (approximately 700Ω to 20MΩ). The wide dynamic range (approximately 90dB) required to obtain the full RH range of the sensor results in some challenges for the designer.

The circuit shown in the schematic features zero drift operational amplifiers (LTC1250 and LTC1050) and a precision instrumentation switched capacitor block (LTC1043). This design will maintain excellent DC accuracy down to microvolt levels. This method was chosen over the use of a true RMS-to-DC or log converter because of the expense and temperature sensitivity of these parts.

Circuit Description

Figure 60 is a schematic diagram of the circuit. Only a single 5V power supply is required. Integrated circuit U1, an LTC1046, converts the 5V supply to –5V to supply power to U2, U3 and U4. U2A, part of an LTC1043 switched capacitor building block, provides the excitation for the sensor, switching between 5V and –5V at a rate of approximately 2.2kHz. This rate can be varied, but we recommended that it be kept below approximately 2.4kHz, which is one-half the auto zero rate of U3. We believe the



NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTANCES ARE IN OHMS, 1/4 W 5%
*C9 ADJUSTS OSC. FREQUENCY 2000pF YIELDS ~ 2.2kHz

AN67 F60

Figure 60. Schematic Diagram of Humidity Sensor Circuit

deviation from the Phys-Chem response curves taken at 5kHz is insignificant.

Variable resistor R2 sets the full-scale output. Since the sensor resistance is 700Ω at approximately 90% humidity, setting R2 at 700Ω will provide a 2:1 voltage divider that, when combined with the gain of U4 (×2), results in an overall gain of one. U3 must be included in order for the circuit to function properly; otherwise C4 and C7 form a voltage divider that is dependent on the resistance of the RH sensor. U3 is a precision auto zero operational amplifier with an auto zero frequency of approximately 4.75kHz. U2B (the "lower" switch) samples the output of U3 and provides this sample to the input of U4. U4 is set to provide a gain of 2.

It is easy to digitize the output of U4. Figure 61 is the schematic of a 12-bit converter that can be used for this purpose. The range of humidity that can be sensed depends on the resolution of the converter. The full-scale output (which is equivalent to approximately 90% humidity) is essentially independent of the number of bits in the A/D converter, but the dry (low RH) end of the scale is dependent on the A/D resolution. As an example, the above referenced 12-bit converter will process humidity signals that translate to approximately 20% RH, since the voltage output at this humidity is approximately 2.3mV, while 0.5LSB is 1.2mV. Digitization down to 10% RH requires the conversion of 350μV signals or a 16-bit converter. From a cost standpoint this seems unwieldy. It is much more economical to use a 2-channel 12-bit converter that changes ranges somewhere in the humidity range.

All of the above solutions measure output voltage from a voltage divider consisting of the RH sensor and a fixed "calibration" resistor. The resistance of the sensor at a fixed output voltage can be calculated from the formula

$$R\ (\Omega) = \frac{R2\ V_{FULL\ SCALE}}{V_{OUT}/2} - R2$$

In this case, if R2 is set to 700Ω and $V_{FULL\ SCALE}$ = 5.00V, then

$$R\ (\Omega) = \frac{3500}{V_{OUT}/2} - 700$$

Once R is calculated (probably by the microprocessor), the humidity can be calculated from the quadratic approximation in the Phys-Chem literature:

$$RH = \frac{LnR - 13.95 - \sqrt{(13.95 - LnR)^2 + 24.288}}{-0.184}$$

If a suitable humidity chamber is not available, the sensor can be removed and fixed resistors substituted. The circuit should then be calibrated from the EMD-2000 "typical response curve." This should provide approximately 2% accuracy.

[1]Phys-Chem Scientific Corporation, 26 West 20th Street, New York, NY 10011. (212) 924-2070 Phone, (212) 243-7352 FAX

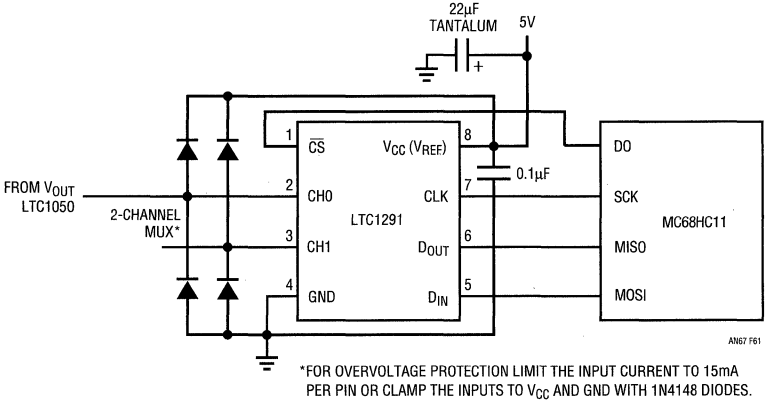


Figure 61. LTC1291 12-Bit A/D Converter Interfaced to MC68HC11

A SINGLE CELL BAROMETER

by Jim Williams and Steve Pietkiewicz

Figure 62, a complete barometric pressure signal conditioner, operates from a single 1.5V battery. Until recently, high accuracy and stability have been obtainable only with bonded strain gauge and capacitively-based transducers, which are quite expensive. This design, using a recently introduced semiconductor transducer, achieves 0.01"Hg (inches of mercury) uncertainty over time and temperature. The 1.5V powered operation permits portable application.

The 6kΩ transducer (T1) requires precisely 1.5mA of excitation, necessitating a relatively high voltage drive. A1's positive input senses T1's current by monitoring the voltage drop across the resistor string in T1's return path. A1's negative input is fixed by the 1.2V LT1004 reference. A1's output biases the 1.5V powered LT1110 switching regulator. The LT1110's switching produces two outputs from L1. Pin 4's rectified and filtered output powers A1 and T1. A1's output, in turn, closes a feedback loop at the regulator. This loop generates whatever voltage step-up is required to force precisely 1.5mA through T1. This arrangement provides the required high voltage drive while minimizing power consumption. This occurs because the switching regulator produces only enough voltage to satisfy T1's current requirements.

L1 Pins 1 and 2 source a boosted, fully floating voltage, which is rectified and filtered. This potential powers A2. Because A2 floats with respect to T1, it can look differentially across T1's outputs, Pins 10 and 4. In practice, Pin 10 becomes "ground" and A2 measures Pin 4's output with respect to this point. A2's gain scaled output is the circuit's output, conveniently scaled at 3.000V = 30.00"Hg.

To calibrate the circuit, adjust R1 for 150mV across the 100Ω resistor in T1's return path. This sets T1's current to the manufacturer's specified calibration point. Next, adjust R2 at a scale factor of 3.000V = 30.00"Hg. If R2 cannot capture the calibration, reselect the 200k resistor in series with it. If a pressure standard is not available, the transducer is supplied with individual calibration data permitting circuit calibration.

This circuit, compared to a high order pressure standard, maintained 0.01"Hg accuracy over months with widely varying ambient pressure shifts. Changes in pressure, particularly rapid ones, correlated quite nicely to changing weather conditions. Additionally, because 0.01"Hg corresponds to about 10 feet of altitude at sea level, driving over hills and freeway overpasses becomes quite interesting. The circuit pulls 14mA from the battery, allowing about 250 hours operation from one D cell.

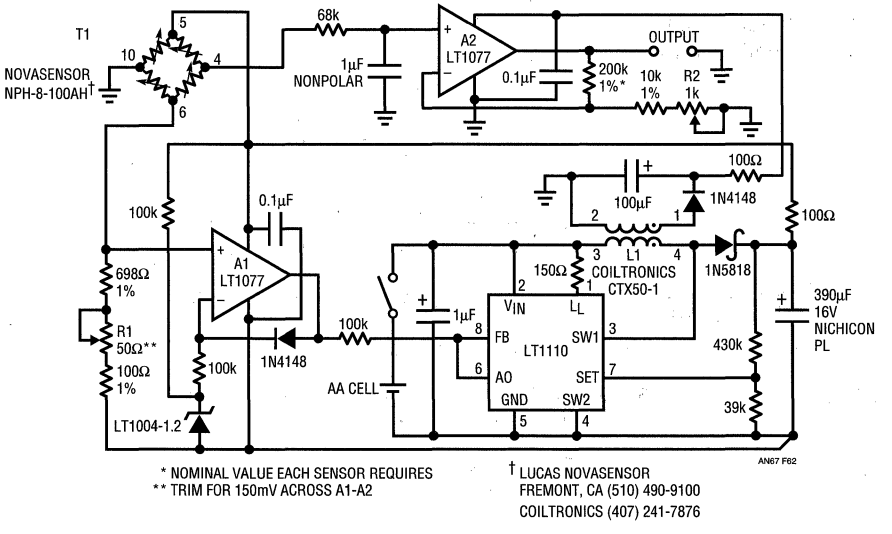


Figure 62. Single Cell Barometer Schematic Diagram

NOISE GENERATORS FOR MULTIPLE USES

A Broadband Random Noise Generator

by Jim Williams

Filter, audio and RF communications testing often require a random noise source. Figure 63's circuit provides an RMS amplitude regulated noise source with selectable bandwidth. RMS output is 300mV with a 1kHz to 5MHz bandwidth, selectable in decade ranges.

Noise source D1 is AC coupled to A2, which provides a broadband gain of 100. A2's output feeds a gain control stage via a simple, selectable lowpass filter. The filter's output is applied to A3, an LT1228 operational transconductance amplifier. A1's output feeds LT1228 A4, a current feedback amplifier. A4's output, which is also the circuit's output, is sampled by the A5-based gain control configuration. This closes a gain control loop to A3. A3's I_{SET} current controls gain, allowing overall output level control.

Figure 64 plots noise at a 1MHz bandpass, whereas Figure 65 shows RMS noise versus frequency in the same bandpass. Figure 66 plots similar information at full bandwidth (5MHz). RMS output is essentially flat to 1.5MHz, with about ±2dB control to 5MHz before sagging badly.

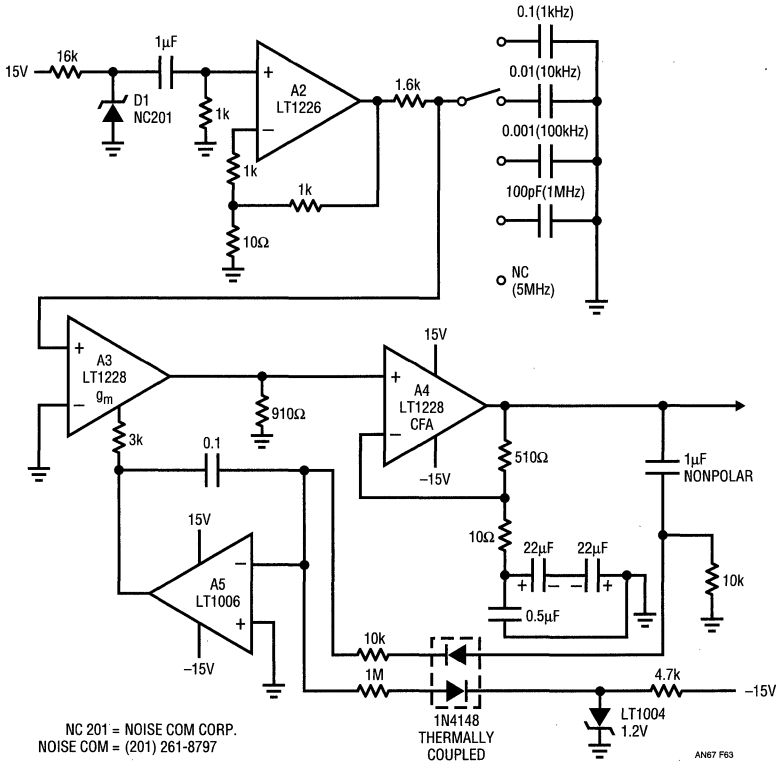


Figure 63. Broadband Random Noise Generator Schematic

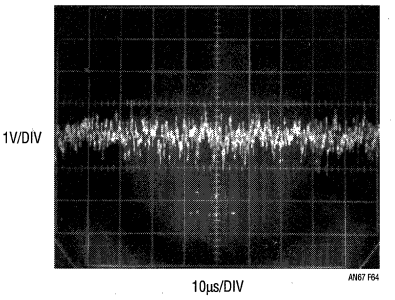


Figure 64. Figure 63's Output In the 1MHz Filter Position

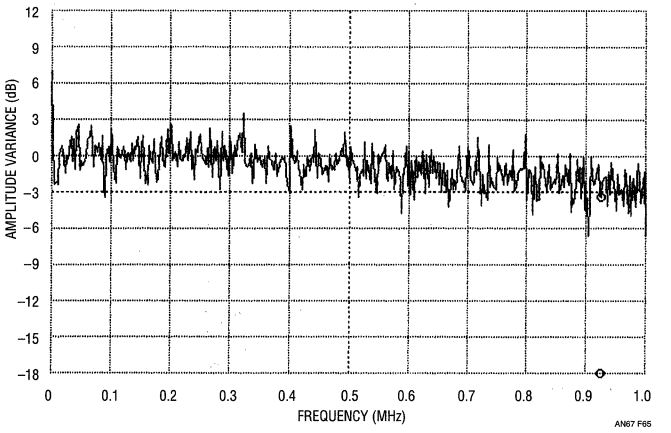


Figure 65. RMS Noise vs Frequency at 1MHz Bandpass

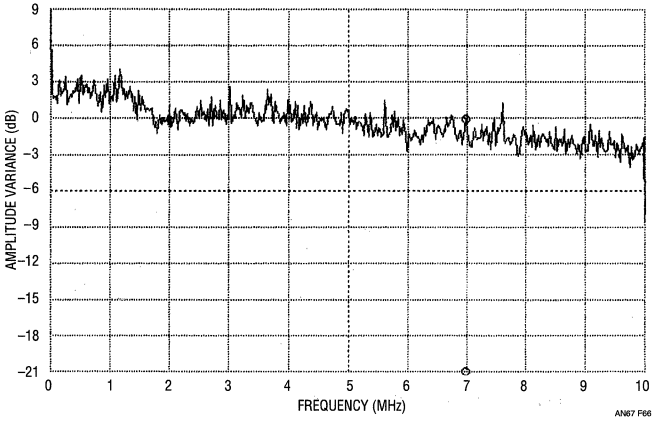


Figure 66. RMS Noise vs Frequency at 5MHz Bandpass

SYMMETRICAL WHITE GAUSSIAN NOISE

by Bent Hessen-Schmidt, NOISE COM, INC.

White noise provides instantaneous coverage of all frequencies within a band of interest with a very flat output spectrum. This makes it useful both as a broadband stimulus and as a power level reference.

Symmetrical white Gaussian noise is naturally generated in resistors. The noise in resistors is due to vibrations of the conducting electrons and holes as described by Johnson and Nyquist.[1, 2] The distribution of the noise voltage is symmetrically Gaussian, and the average noise voltage is:

$$\overline{V}_n = 2\sqrt{kTf\ R(f)\ p(f)\ df} \qquad (1)$$

where:

k = 1.38E-23 J/K (Boltzmann's constant)

T = temperature of the resistor in Kelvin

f = frequency in Hz

h = 6.62E-34 Js (Planck's constant)

R(f) = resistance in ohms as a function of frequency

$$p(f) = \frac{hf}{kT[\exp(hf/kT) - 1]} \qquad (2)$$

p(f) is close to unity for frequencies below 40GHz when T is equal to 290°K. The resistance is often assumed to be independent of frequency, and $f$df is equal to the noise bandwidth (B). The available noise power is obtained when the load is a conjugate match to the resistor, and it is:

$$N = \frac{\overline{V}_n^2}{4R} = kTB \qquad (3)$$

where the "4" results from the fact that only half of the noise voltage and hence only 1/4 of the noise power is delivered to a matched load.

Equation 3 shows that the available noise power is proportional to the temperature of the resistor; thus it is often called thermal noise power. Equation 3 also shows that white noise power is proportional to the bandwidth.

An important source of symmetrical white Gaussian noise is the noise diode. A good noise diode generates a high level of symmetrical white Gaussian noise. The level is often specified in terms of excess noise ratio (ENR).

$$\text{ENR (in dB)} = 10\text{Log}\frac{(Te - 290)}{290} \qquad (4)$$

Te is the physical temperature that a load (with the same impedance as the noise diode) must be at to generate the same amount of noise.

The ENR expresses how many times the effective noise power delivered to a nonemitting, nonreflecting load exceeds the noise power available from a load held at the reference temperature of 290°K (16.8°C or 62.3°F).

The importance of a high ENR becomes obvious when the noise is amplified, because the noise contributions of the amplifier may be disregarded when the ENR is 17dB larger than the noise figure of the amplifier (the difference in total noise power is then less than 0.1dB). The ENR can easily be converted to noise spectral density in dBm/Hz or $\mu V/\sqrt{Hz}$ by use of the white noise conversion formulas in Table 1.

Table 1. Useful White Noise Conversion

dBm = dBm/Hz + 10log(BW)
dBm = 20log($\overline{V}$n) – 10log(R) + 30dB
dBm = 20log($\overline{V}$n) + 13dB, for R = 50Ω
dBm/Hz = 20log($\mu V\sqrt{Hz}$) – 10log(R) – 90dB
dBm/Hz = –174dBm/Hz + ENR, for ENR > 17dB

When amplifying noise it is important to remember that the noise voltage has a Gaussian distribution. The peak voltages of noise are therefore much larger than the average or RMS voltage. The ratio of peak voltage to RMS voltage is called crest factor, and a good crest factor for Gaussian noise is between 5:1 and 10:1 (14dB to 20dB). An amplifier's 1dB gain compression point should therefore be typically 20dB larger than the desired average noise output power to avoid clipping of the noise.

For more information about noise diodes, please contact NOISE COM, INC. at (201) 261-8797.

[1] Johnson, J.B. "Thermal Agitation of Electricity in Conductors," *Physical Review*, July 1928, pp. 97-109.

[2] Nyquist, H. "Thermal Agitation of Electric Charge in Conductors," *Physical Review*, July 1928, pp. 110-113.

NOISE GENERATORS FOR MULITPLE USES

A Diode Noise Generator for "Eye Diagram" Testing

by Richard Markell

The circuit that Jim Williams describes evolved from my desire to build a circuit for testing communications channels by means of "eye diagrams." (See *Linear Technology*, Volume I, Number 2 for a short explanation of the eye diagram.) I wanted to replace my pseudorandom code generator circuit, which used a PROM, with a more "analog" design—one that more people could build without specialized components. What evolved was a noise source sampled by a very fast comparator (see Figure 67). The comparator outputs a random pattern of 1's and 0's.

The noise diode (an NC201) is filtered and amplified by the LT1190 high speed operational amplifier (U1). The output feeds the LT1116 (U2), a 12ns single supply, ground-sensing comparator. The 2kΩ pot at the inverting input of the LT1116 sets the threshold to the comparator so that a quasiequal number of 1's and 0's are output. U3 latches the output from U2 so that the output from the comparator remains latched throughout one clock period. The two-level output is taken from U3's Q0 output.

The additional circuitry shown in the schematic diagram allows the circuit to output four-level data for PAM (pulse amplitude modulation) testing. The random data from the two-level output is input to a shift register, which is reset on every fourth clock pulse. The output from the shift register is weighted by the three 5k resistors and summed into the LT1220 operational amplifier from which the output is taken. The filter network between the 74HC74 output and the 74HC4094 strobe input is necessary to ensure that the output data is correct.

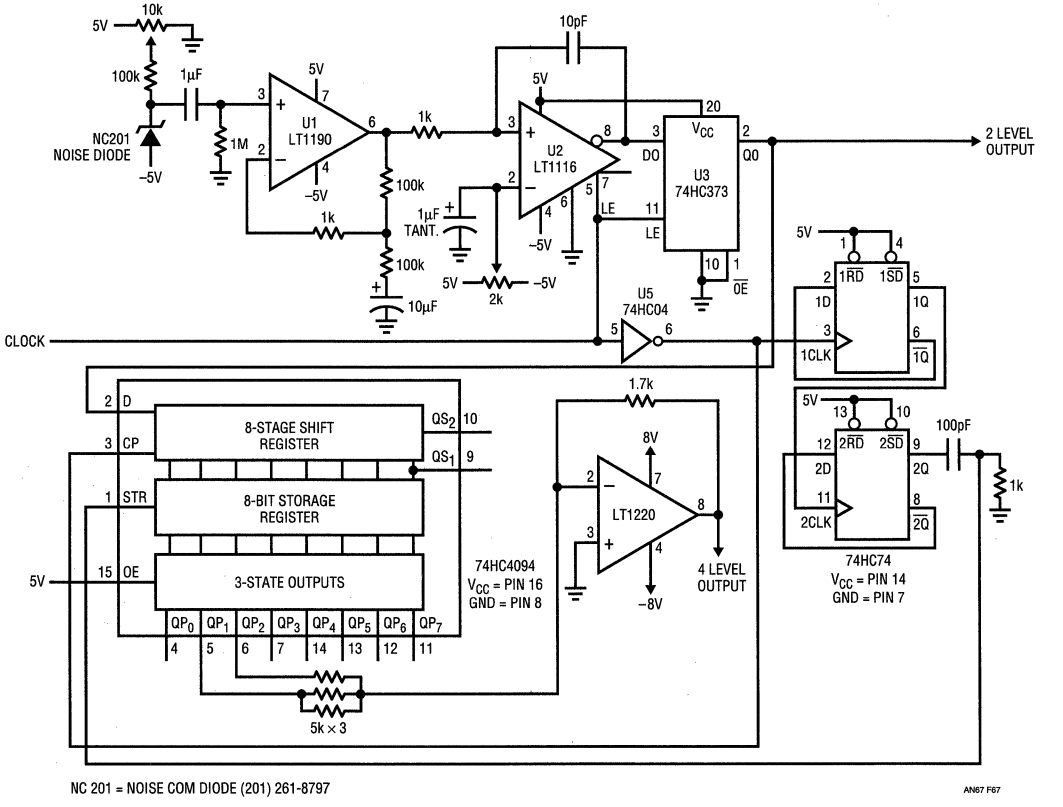


Figure 67. Pseudorandom Code Generator Schematic Diagram

Video/Op Amps

LT1251 CIRCUIT SMOOTHLY FADES VIDEO TO BLACK

by Frank Cox

When a video signal is attenuated, there is a point were the sync amplitude is too small for a monitor to process properly. Instead of making a smooth transition to black, the picture rolls and tears. One solution to this problem is to run a separate sync signal into the monitor. This may not be a viable solution in a system where cost and complexity are the prime concerns. What is needed is a simple video "volume control."

The circuit in Figure 68 can perform a smooth fade to black, while maintaining good video fidelity. U1, an LT1360 op amp, and its associated components form an elementary sync separator. C1, R1 and D1 clamp the composite video. D2 biases the input of U1 to compensate for the drop across D1. When D1 conducts, the most negative portion of the waveform containing the sync information is amplified by U1. The clamp circuit in the feedback network of U1 (D4 to D8) prevents the amplifier from saturating. D3 and the CMOS inverter U4 complete the shaping of the sync waveform. This sync separator works with most video signals but, because of its simplicity, will not work with very noisy or distorted video. The remainder of the circuit is an LT1251 video fader (U2) configured to fade between the original video and the sync stripped from that video. Thus, the video fades to black.

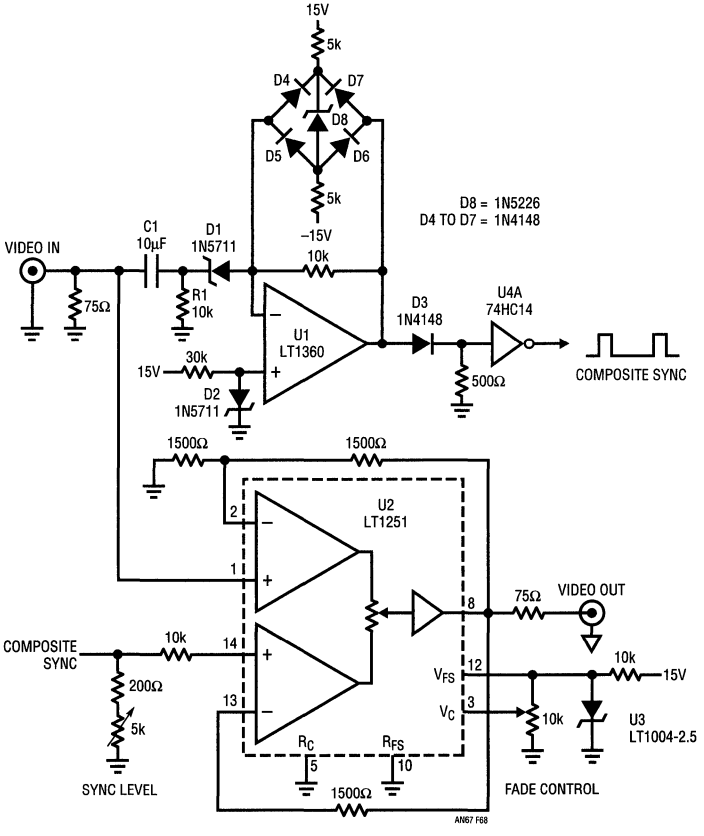


Figure 68. LT1251 Video Fader Schematic Diagram

The control voltage for the fader is generated by a voltage reference and a 10k variable resistor. If this control potentiometer is mounted an appreciable distance from the circuit or if the control generates any noise when adjusted, this node should be bypassed.

Figure 69 is a multiple exposure waveform photograph that shows the action of this circuit. Two linear ramp video test signals are shown in this photograph. The video is faded from full amplitude to zero amplitude in six steps. The sync waveform (lower center) remains unchanged. In Figure 70, a single video line modulated with color subcarrier is faded from full video amplitude to zero video amplitude. The monitor will eventually lose color lock and shut the color off as the amplitude of the color subcarrier is reduced. This is not a problem in this application because the color decoding circuits in the monitor are designed to work with a variety of signals from tape or broadcast, and so have a large dynamic range. Color portions of the picture will remain after the luminance portion is completely black.

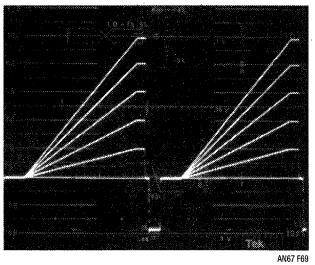


Figure 69. Multiple Exposure Photo Showing Circuit Operation

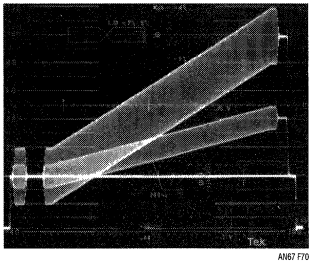


Figure 70. Photo Detailing a Single Video Line with Color Subcarrier Faded to Zero Amplitude

LUMA KEYING WITH THE LT1203 VIDEO MULTIPLEXER

by Frank Cox

In video systems, the action of switching between two or more active video sources is referred to as a "wipe" or a "key." When the decision to switch video sources is based on an attribute of the active video itself, the action is called keying. A wipe is controlled by a nonvideo signal such as a ramp. The circuit presented in Figure 71 is referred to as a "luma key" because it switches between two sources when the luminance ("luma") of a monochrome key signal reaches a set level. It is also possible to key on the color of the video source and this, not surprisingly, is called "chroma keying."

Figure 71's operation is very straightforward. A monochrome video source is used to generate the key signal. The LT1363 is used as a buffer and may not be needed in all applications. If the key signal is to be used as one of the switched signals, it is convenient to "loop through" the input of this buffer. The LT1016 comparator switches when the video level exceeds the DC reference on its inverting input, which is controlled by the "key sensitivity" control. The TTL key signal controls an LT1203 video multiplexer. Any two video sources may be connected to the inputs of the LT1203, as long as they are gen locked and within the common mode range (on ±5V supplies this is ±3V over 0°C to 70°C) of the multiplexer. The LT1203's fast switching speed, low offset and clean switching make it a natural for an active video switching application like this one. Composite color signals can be used, but the best results will be obtained if the key signal's horizontal sync is phase coherent with the color reference of the sources. The key source video should be monochrome to prevent the key comparator from switching on the color subcarrier.

Nonstandard video signals can be used for the inputs to the LT1203. For instance, it is possible to select between two DC input levels to construct a two-level image. Figure 72 is an example of an image constructed this way. A monochrome video signal is sliced and used to key between black (0V) and gray (approximately 0.5V) to

generate this image of a famous linear IC designer. An image formed in this way is not a standard video output until the blanking and sync intervals are reconstructed. The second LT1203 blanks the video and an LT1363 circuit sums composite sync to the video and drives a cable. For more information on this part of the circuit, see AN 57, page 7. A clamp is not used since the DC levels are arbitrarily set by the inputs, but one could be used, as in the figure on page 7 of AN57, if the sources were video. As another option, Figure 73 shows the same key signal used as one of the inputs to the multiplexer.

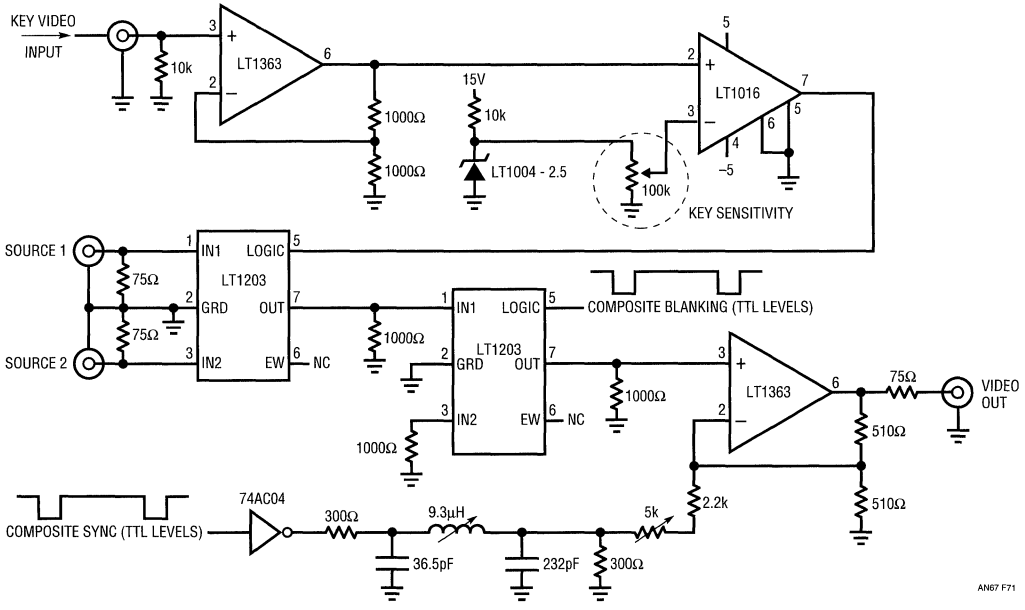


Figure 71. Luma Keyer Schematic Diagram

Figure 72. Two Level Image of IC Designer

Figure 73. Key Signal Used as Input to the MUX

LT1251/LT1256 VIDEO FADER AND DC GAIN CONTROLLED AMPLIFIER

by William H. Gross

The Video Fader

Figure 74 shows the LT1251/LT1256 configured as a fader with unity gain. A full-scale voltage of 2.5V is applied to Pin 12 and the control input drives Pin 3.

Figure 75 shows the true response of the control path. The control path is fast enough for quick switching between signals, as when keying on a color or luminance level. The control path introduces only a small (50mV), short (50ns) glitch when switched quickly.

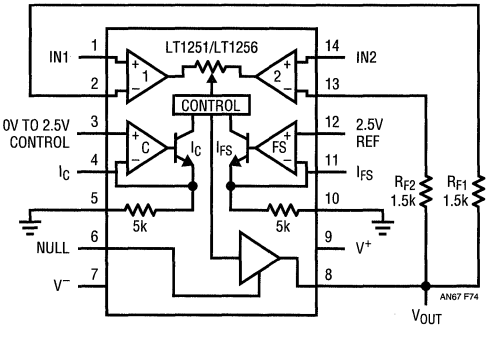


Figure 74. Two Input Video Fader

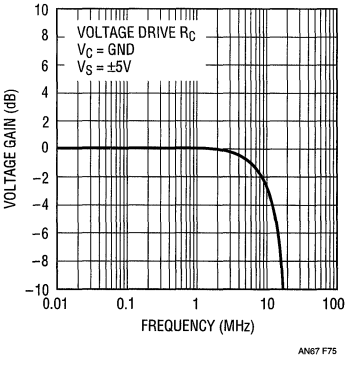


Figure 75. LT1251/56 Control Path Bandwidth

A summary of the LT1251/LT1256 performance operating on ±5V supplies in the configuration shown in Figure 74 is given in Table 1.

Table 1. LT1251/LT1256 Performance Summary

Slew Rate (at ±2V, R_L = 150Ω)	300V/µs
Full-Power Bandwidth ($1V_{RMS}$)	30MHz
Small-Signal Bandwidth	30MHz
Differential Gain (NTSC, R_L = 150Ω)	0.1%
Differential Phase (NTSC, R_L = 150Ω)	0.1°
Total Harmonic Distortion (1kHz, K = 1)	0.001%
(1kHz, K = 0.5)	0.01%
(1kHz, K = 0.1)	0.4%
Rise Time, Fall Time	11ns
Overshoot	3%
Propagation Delay	10ns
Settling Time (0.1%, V_O = 2V)	65ns
Quiescent Supply Current	13.5mA

Applications

Grounding IN2 of the LT1256 in Figure 74 results in a 2-quadrant multiplier. Figure 76 shows the 2-quadrant multiplier being used as an AM modulator. The output will deliver 10dBm into 50Ω. The LT1077 op amp senses the LT1256 output DC and drives the Null pin, eliminating any DC at the output. The Null pin voltage is nominally 100mV above the negative supply and therefore the op amp output must be able to swing within a few millivolts of the negative supply. Without the LT1077, the worst-case DC output voltage is 50mV.

By operating one input stage in an inverting configuration and the other in a noninverting configuration and driving both inputs, the LT1256 becomes a 4-quadrant multiplier. Figure 77 shows the 4-quadrant multiplier being used as a double-sideband, suppressed-carrier modulator. The LT1077 DC output nulling circuit could be added if necessary.

The LT1251/LT1256 can be used to implement numerous other functions, including voltage controlled filters, phase shifters and oscillators. Squaring and limiting circuits can be designed by feeding the output or input into the Control pins. Gamma correction and other compression circuits are created in a similar manner. The applications are limited only by the designer's imagination.

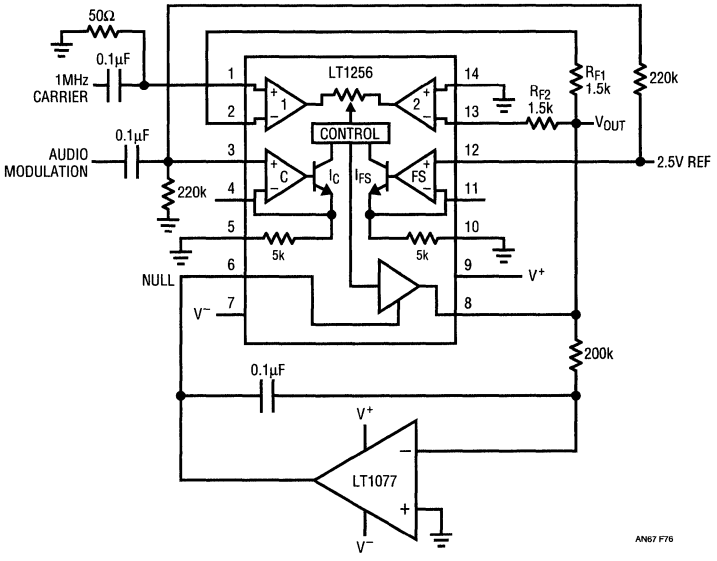


Figure 76. AM Modulator with DC Output Nulling Circuit

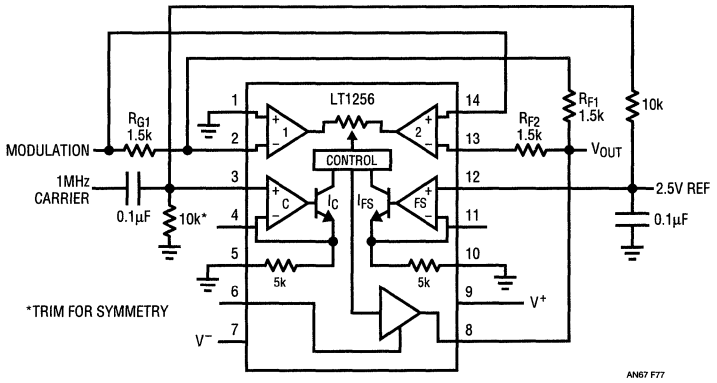


Figure 77. Four Quadrant Multiplier Uses as a Double Sideband, Suppressed Carrier Modulator

EXTENDING OP AMP SUPPLIES TO GET MORE OUTPUT VOLTAGE

by Dale Eagar

We often hear of applications that require high output voltage, low output impedance amplifiers. Here is a topology that allows you to extend an op amp's output voltage swing while still maintaining its short-circuit protection. The trick is to suspend the op amp between two MOSFET source followers so that the supply voltages track the op amp's output voltage (see Figure 78). The circuit shown in Figure 78 will perform very nicely with any run-of-the-mill ideal op amp. The problem is in the lead times of ideal op amps—they just keep getting pushed out to later dates.

Nonideal op amps have realistic lead times and can be made to work in the extended supply mode. They have bandwidth limitations in both CMRR and PSRR. The circuit shown in Figure 79 implements the extended supply as shown in Figure 78 and has several additional components: C1 is added to decouple the supply, improving high frequency PSRR; R3 and R5 decouple the gates of Q1 and Q2 from AC ground, preventing Q1 and Q2 from running off together to redirect local air traffic; R1, R2 and C4 form a snubber to de-Q the 2-pole system formed by the Miller capacitance of Q1 and Q2 and the high frequency CMRR of IC1; additionally, R4, R6, C2, C3, Z1 and Z2 form the two 15V voltage sources (E1 and E2 in Figure 78); CR1 and CR2 are protection diodes that allow the output to be instantaneously shorted to ground when the output is at any output voltage.

The values of R1, R2 and C4 vary with the MOSFETs' Miller capacitance and with the high frequency CMRR of the op amp used. They are selected to minimize the overshoot in the step response of the amplifier.

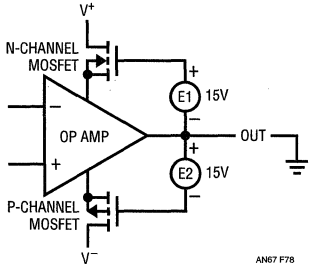


Figure 78. Block Diagram of Suspended Supply Op Amp

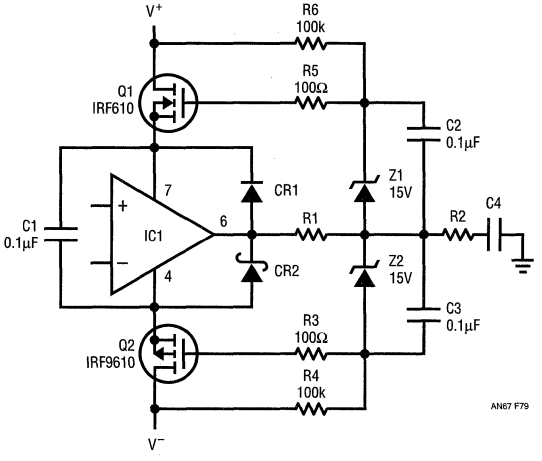


Figure 79. Detailed High Voltage Op Amp

High Voltage, High Frequency Amplifier

Using the LT1227 current feedback amplifier (CFA) in the extended supply mode as shown in Figure 79, it is relatively easy to get a 1MHz power bandwidth at $100V_{P-P}$ (see Figure 80 for component values). This circuit has short-circuit protection and is stable into all capacitive loads.

If One Is Good, Are Two Better?

Dual and quad op amps can also be configured with extended supplies, although the design gets just a wee bit tricky. When extending supplies of multiple stages and/or complete circuits, some design rules need to change. Op amp circuits generally require a ground against which to reference all signals. The problem encountered when

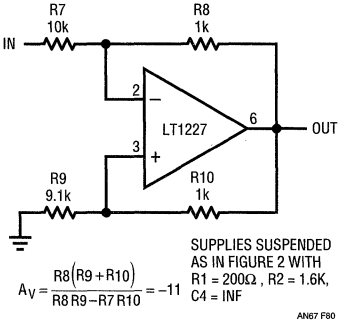


Figure 80. High Speed Suspended Op Amp

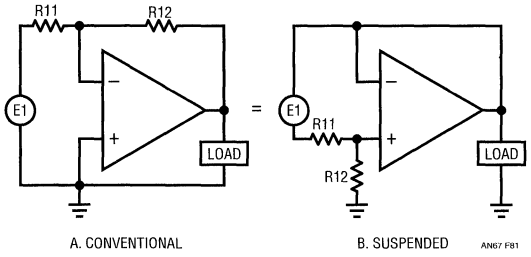


Figure 81. Inverting Amplifiers (A. Conventional, B. Suspended)

using extended supply mode is that "ground" is swinging through the common mode range of the op amp and beyond. This raises the following question: "If I cannot reference the signals to ground, to what can I reference them?" The answer? "Use the output as the signal reference." This works for all stages except the last stage, where using the output as the reference would simply discard the signal. In the last stage, ground is effectively the output and the feedback resistor is R12. This is shown in Figures 81a and 81b. Figure 81a shows a conventional inverting amplifier where the input and output signals are referred to ground. Figure 81b shows the equivalent circuit implemented in the extended supply mode.

Here are two rules for design in the extended supply mode, which will be demonstrated in the next application:

Rule 1: When designing multiple stages in the extended supply mode, reference the signals of all stages except the last to the output of the last stage.

Rule 2: Invert the signal using the circuit in Figure 81b at the last stage.

Ring-Tone Generator

Ring-tone generators are sine wave output, high voltage inverters for the specific purpose of ringing telephone bells. In decades past, the phone company generated their ring tones with motor generator sets with the capacity to ring numerous phones simultaneously. Often, ring tones are 20Hz at 90V with less than 10mA per bell output current capability. Since the power supplied is low one would think that the task is minimal. This is not always so. "It's simple—no problem," is often heard in response to queries about ring tone generators. "Just hook a couple of logic level FETs to two spare output bits of the microprocessor and hook their drains to the primary side of a transformer, with the center tap hooked to 5V or 12V or whatever." At this point everyone is happy until the transformer comes in. After a few phone calls to make sure that the transformer maker shipped the right one, the engineer (face covered with egg) asks if anyone needs a rather large paperweight. The engineer (still wiping egg from his face) then decides to use switching power supply technology to solve this "simple" problem.

Here is a simple ring-tone generator that can be turned on and off with a logic signal. It has a fully isolated output, is short-circuit protected and can be powered by any input voltage from 3V to 24V.

How It Works

Suspended along with the dual op amp in Figure 82 are two voltage references and an oscillator. Keep in mind when referring to Figure 82 that the node labeled "A" is the output; this is the reference common for the references, the oscillator and the first lowpass filter (U1a). The two references, VR1 and VR2, produce ±2.5V. The oscillator U2, running on the ±2.5V references, produces a 20Hz square wave rail-to-rail. U1a is a 2nd order, Sallen and Key lowpass filter that knocks off the sharp edges, presenting the somewhat smoothed signal at point "B."

Next comes the tricky stuff. U1b is a 2nd order, multiple-feedback (MFB) lowpass filter/amplifier that performs four functions: first, it subtracts the voltage at point "A" (its own output voltage) from the voltage at point "B" (the incoming signal), forming a difference that is the signal; second, it filters the difference signal with a 2-pole lowpass filter, smoothing out the last wrinkles in the signal; third, it amplifies the filtered difference signal with a gain of 34; and fourth, it references the amplified signal to ground, forming the output.

Note that R99 shown in Figure 82 is there to protect the input of U1b in the event that the output is shorted when the output voltage is very high. This measure is necessary because the bottom end of C99 is connected to ground, and C99 could have up to 100V across it. When the output is shorted to ground from a high voltage, R99 limits the current into the input of U1b to an acceptable level.

This circuit, when coupled with the switching power supply shown in Figure 83, implements a fully isolated sine wave ring tone generator.

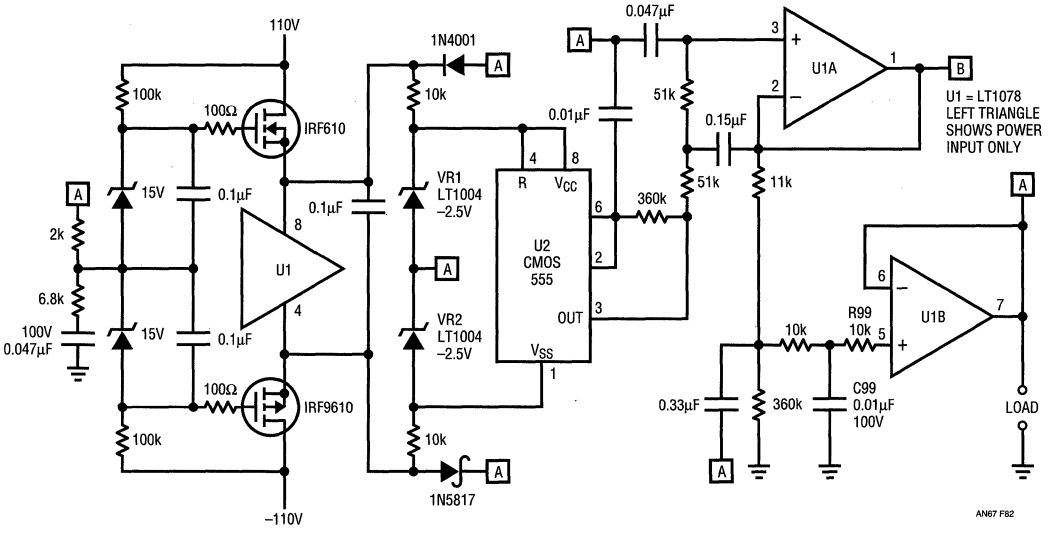


Figure 82. Ring Tone Generator: Oscillator, Filter and Driver

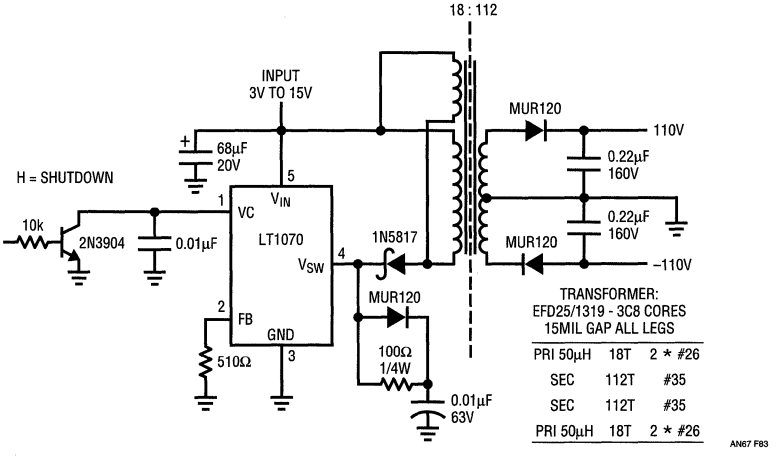


Figure 83. High Voltage Power Supply for Ring Tone Generator

The input current and power versus input voltage for the combination ring-tone generator (Figures 82 and 83) are shown in Figure 84. The output waveform (loaded with one bell) is shown in Figure 85 and the harmonic distortion is shown in Figure 86.

Although somewhat tricky at first, extended supply mode is a valuable tool to get out of many tight places. There is also a great deal of satisfaction to be gathered when making it work, for those of you who love a technical challenge.

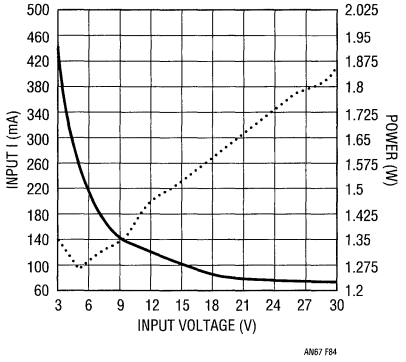


Figure 84. Input Current and Input Power vs Input Voltage While Ringing One Bell for Figure 82 Circuit

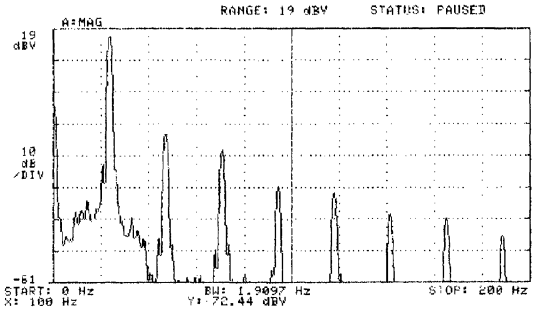


Figure 85. Ring-Tone Generator Frequency Spectrum Plot

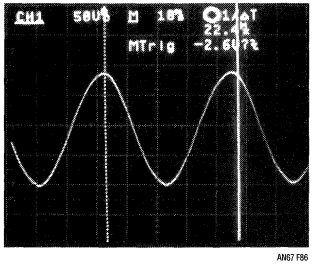


Figure 86. Sine Wave Output from Ring-Tone Generator

USING SUPER OP AMPS TO PUSH TECHNOLOGICAL FRONTIERS: AN ULTRAPURE OSCILLATOR

by Dale Eagar

The advent of high speed op amps allows the implementation of circuits that were impossible just a few years ago. This article describes a new topology that makes use of these new high speed circuits and makes astounding improvements in its performance. An oscillator using such op amps has distortion limits beyond our ability to measure.

An Ultralow Distortion, 10kHz Sine Wave Source for Calibration of 16-Bit or Higher A/D Converters

The path to low distortion in an amplifier or an oscillator begins with amplifiers with the lowest possible open-loop distortion and lots of excess open-loop gain in the frequency band of interest. The next step is closing the loop, thereby reducing open-loop distortion by an amount approximately equal to the loop gain. This is not easy, as certain stability criteria must be met by an amplifier that isn't an oscillator or by an oscillator that oscillates at a specified frequency.

The trick used in this circuit is to build an amplifier that has excessive gain where it is needed but no excess gain or phase shift where it isn't. In many applications the band from DC to 100kHz requires the above mentioned high gain; the gain should fall off when the open-loop gain falls through unity (around 5MHz). How this is done in the flesh (silicon) is shown here.

Circuit Operation and Circuit Evolution

A standard inverting amplifier topology, as shown in Figure 87, has a finite open-loop gain in the frequency band of interest (see Figure 88), with some open-loop harmonic distortion (about –60dB) and an open-loop output impedance of about 70Ω.

The amplifier shown in Figure 87 can achieve low distortion, but since the circuit has a limited loop gain, the curative effects of feedback can only be taken so far. The designer must also be careful to ensure that R_L is many times higher than the open-loop output impedance of U1.

Figure 89's circuit makes several improvements over the circuit of Figure 87. First, the open-loop gain of U1 is multiplied by $A_V(f)$, the gain of the composite amplifier stage A1. Second, the input impedance of A1 can be made very high, further improving both open-loop gain of U1 and the open-loop harmonic distortion of U1. Third, the output voltage swing of U1 is decreased, keeping its output circuitry in its lowest distortion area.

The composite circuit, A1, consists of three sections. The first section, as seen in Figure 90, has the gain/phase plot shown in Figure 92. Note the high gain at 10kHz (60dB) and the gain of 6dB at 5MHz, with only 17 degrees of phase contribution. In fact, this looks so nice that you might ask, "why not use two?" and thus reduce your distortion by an additional 60dB?

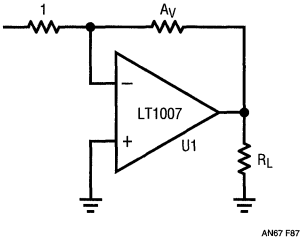


Figure 87. Conventional Inverting Op Amp Topology

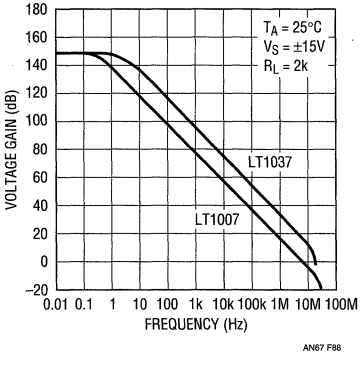


Figure 88. Voltage Gain vs Frequency

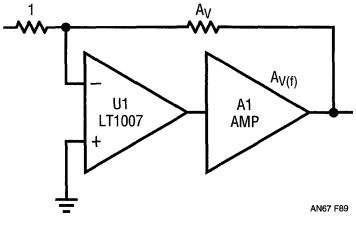


Figure 89. LT1007 Followed by Composite Amplifier A1

The second section, shown in Figure 91, has the gain/phase plot shown in Figure 93. Note that here the gain doesn't change significantly, but the phase is positive just where we want it (1MHz to 5MHz) to allow a very stable system to be built.

The third section, as you might guess, is the same as the first. In sum, the gain/phase plot of the composite amplifier A1 is shown in Figure 94. Note the gain, which is in

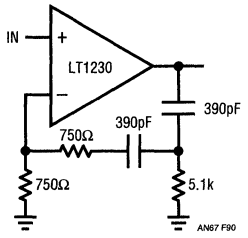


Figure 90. First Section of Composite Amplifier A1

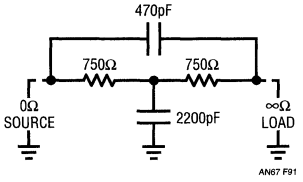


Figure 91. Second Section of Composite Amplifier A1

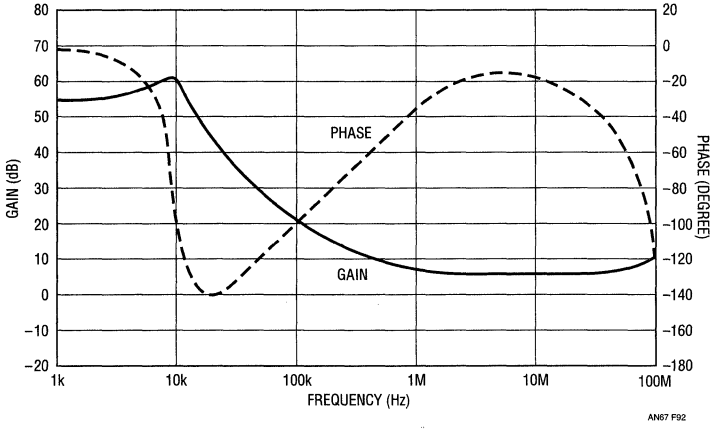


Figure 92. Gain/Phase Response of Circuit Shown in Figure 90

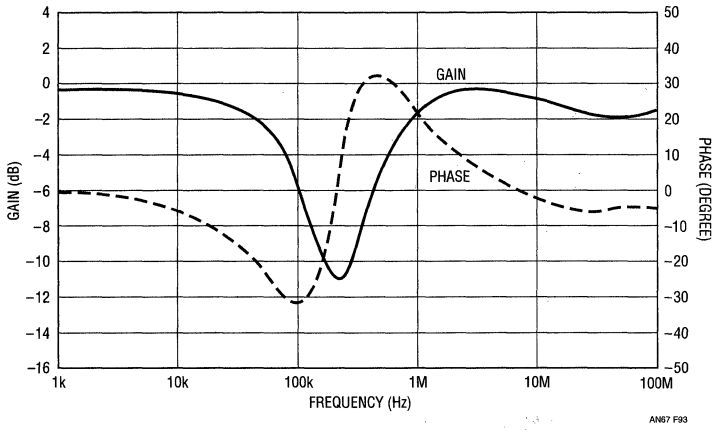


Figure 93. Gain/Phase Response of Circuit Shown in Figure 91

excess of 120db at 10kHz and the total phase contribution of about –20 degrees at 5MHz. The complete gain block is shown in Figure 95.

Super Gain Block Oscillator Circuitry

When A1, as described above is connected with U1, as shown in Figure 89, the resulting circuit is not only unity-gain stable but has open-loop gain of 180dB at 10kHz (yes, 1 billion). This means that the closed-loop harmonic distortion can easily be kept in the region of "parts per billion."

A Wien bridge oscillator with harmonic distortion in the parts per billion is shown in Figure 96. The super op amps S1 and S2 are the previously described composite amplifiers as shown in Figure 95. Note that the output is taken between the two outputs of S1 and S2. This topology gives the best signal-to-noise ratio, in addition to balancing the

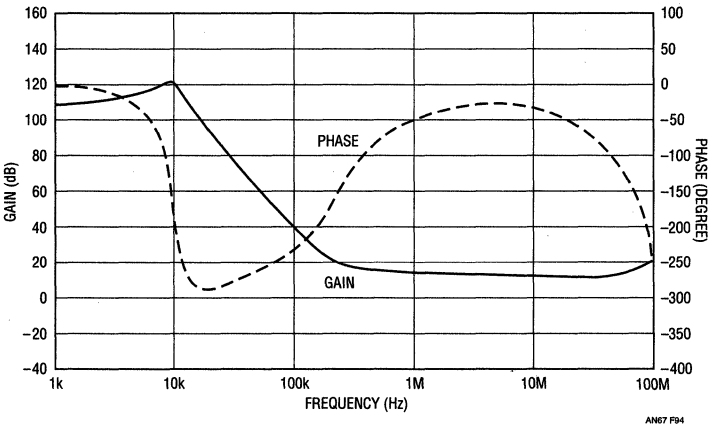


Figure 94. Gain/Phase Response of Composite Amplifier A1 (Shown in Figure 89)

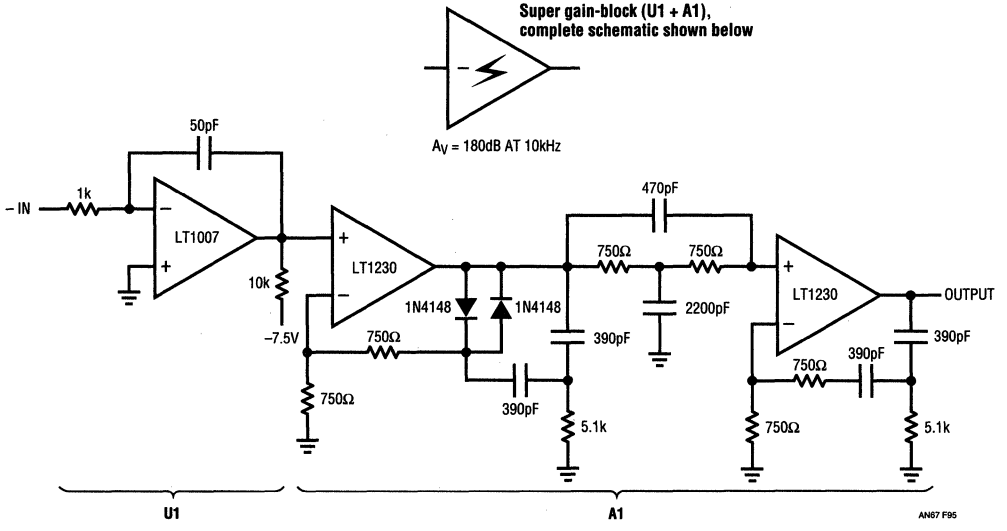


Figure 95. Super Gain Block S1 and S2 Schematic Diagram

power supply currents and their harmonics. Taking the output from one amplifier's output to ground is also valid.

To align the circuit, first center the output amplitude adjustment potentiometer. Next, adjust the gain trim for oscillation while also adjusting the output amplitude for $5V_{P-P}$ output (single ended). Next, adjust the gain trim to $1V_{P-P}$ at the output of the LT1228. Finally, connect a spectrum analyzer to the output of the LT1228 and adjust the second harmonic trim potentiometer for a null in the second harmonic of the oscillator frequency. The measurement of the harmonic distortion of this oscillator defies all of our resources, but appears to be well into the parts-per-billion range.

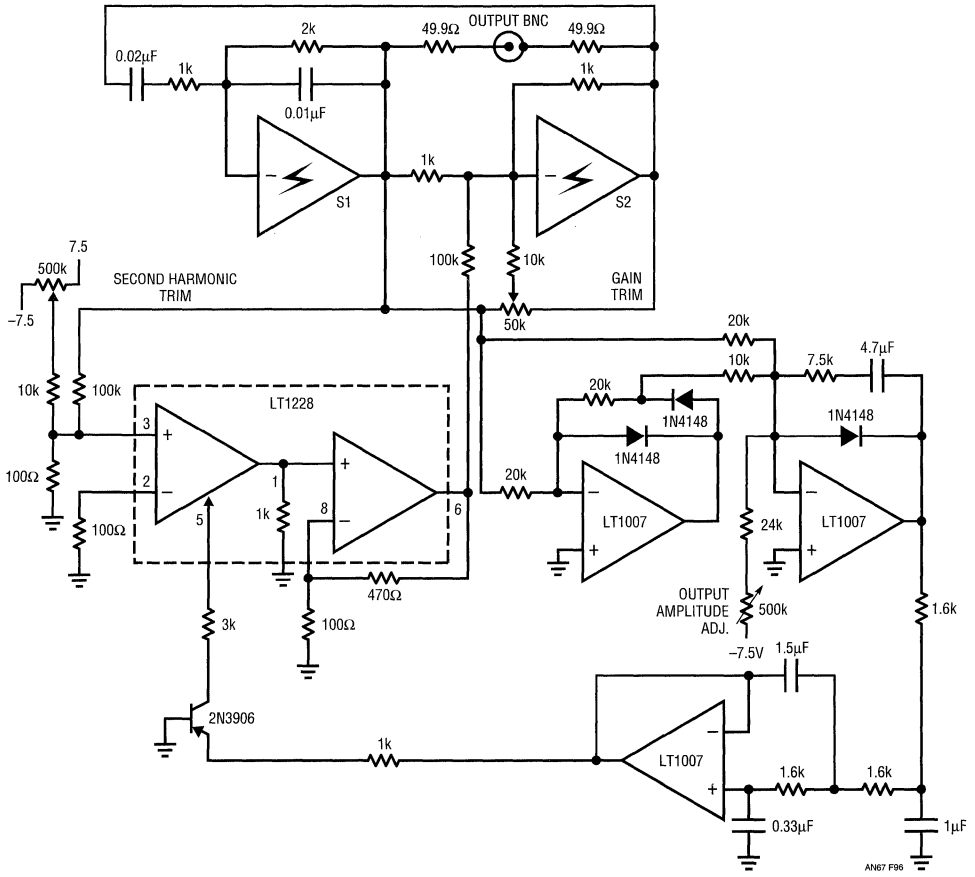


Figure 96. Schematic Diagram: Wien Bridge Oscillator with Distortion in the Parts-per-Billion Range

FAST VIDEO MUX USES LT1203/LT1205

by Frank Cox

To demonstrate the switching speed of the LT1203/LT1205, the RGB MUX of Figure 97 is used to switch the inputs of an RGB workstation with a 22ns pixel width. Figure 98a is a photo showing the workstation output and RGB MUX output. The slight rise time degradation at the RGB MUX output is due to the bandwidth of the LT1260 current feedback amplifier used to drive the 75Ω cable. In Figure 98b the LT1203 switches at the end of the first pixel to an input at zero and removes the following pixels.

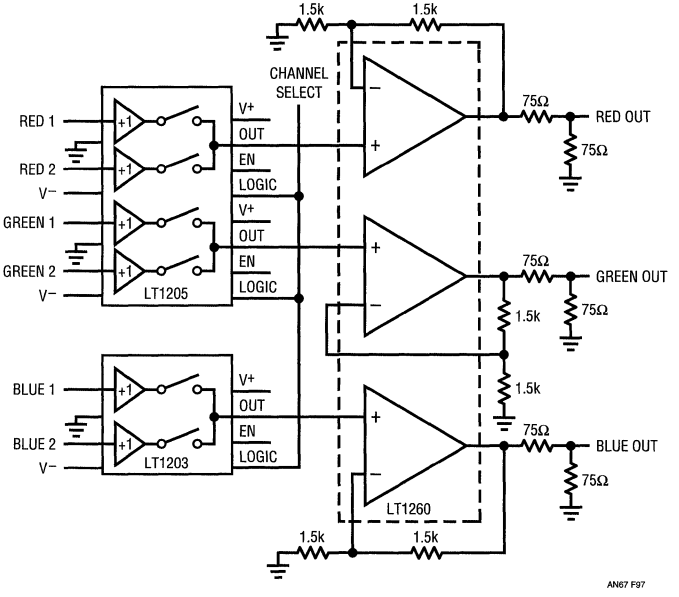


Figure 97. Fast RGB MUX

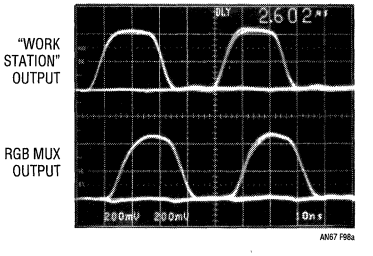


Figure 98a. Workstation and RGB MUX Output

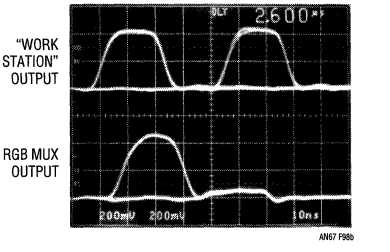


Figure 98b. RGB MUX Output Switched to Ground After One Pixel

USING A FAST ANALOG MULTIPLEXER TO SWITCH VIDEO SIGNALS FOR NTSC "PICTURE-IN-PICTURE" DISPLAYS

by Frank Cox

Introduction

The majority of production[1] video switching consists of selecting one video source out of many for signal routing or scene editing. For these purposes, the video signal is switched during the vertical interval in order to reduce visual switching transients. The image is blanked during this time, so if the horizontal and vertical synchronization and subcarrier lock are maintained, there will be no visible artifacts. Although vertical interval switching is adequate for most routing functions, there are times when it is desirable to switch two synchronous video signals during the active (visible) portion of the line to obtain picture-in-picture, key or overlay effects. Picture-in-picture or active video switching requires signal-to-signal transitions that are both clean and fast. A clean transition should have a minimum of preshoot, overshoot, ringing or other aberrations commonly lumped under the term "glitching."

Using the LT1204

A quality high speed multiplexer amplifier can be used with good results for active video switching. The important specifications for this application are small, controlled switching glitch, good switching speed, low distortion, good dynamic range, wide bandwidth, low path loss, low channel-to-channel crosstalk and good channel-to-channel offset matching. The LT1204 specifications match these requirements quite well, especially in the areas of bandwidth, distortion and channel-to-channel crosstalk (which is an outstanding 90dB at 10MHz). The LT1204 was evaluated for use in active video switching with the test setup shown in Figure 99. Figure 100 shows the video waveform of a switch between a 50% white level and a 0% white level about 30% into the active interval and back again at about 60% of the active interval. The switch artifact is brief and well controlled. Figure 101 is an expanded view of the same waveform. When viewed on a monitor, the switch artifact is just visible as a very fine

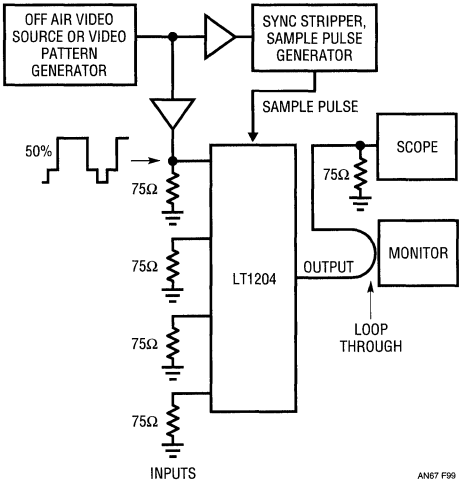


Figure 99. "Picture-in-Picture" Test Setup

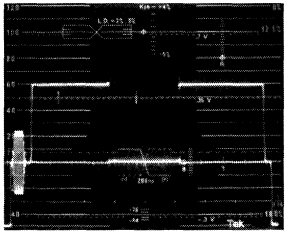


Figure 100. Video Waveform Switched from 50% White Level to 0% White Level and Back

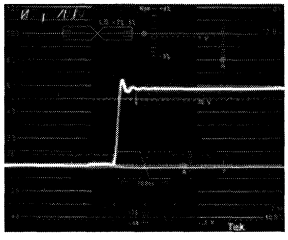
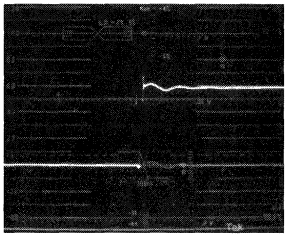


Figure 101. Expanded View of Rising Edge of LT1204 Switching from 0% to 50% (50ns Horizontal Division)



AN67 F102

Figure 102. Expanded View of "Brand-X" Switch 0% to 50% Transition

line. The lower trace is a switch between two black level (0V) video signals showing a very slight channel-to-channel offset, which is not visible on the monitor. Switching between two DC levels is a worst-case test, as almost any active video will have enough variation to totally obscure this small switch artifact.

Video Switching Caveats

In a video processing system that has a large bandwidth compared to the bandwidth of the video signal, a fast transition from one video level to another (with a low amplitude glitch) will cause minimal visual disturbance. This situation is analogous to the proper use of an analog oscilloscope. In order to make accurate measurement of pulse waveforms, the instrument must have much more bandwidth than the signal in question (usually five times the highest frequency). Not only should the glitch be small, it should be otherwise well controlled. A switching glitch that has a long settling "tail" can be more troublesome (that is, more visible) than one that has more amplitude but decays quickly. The LT1204 has a switching glitch that is not only low in amplitude but well controlled and quickly damped. Refer to Figure 102, which shows a video multiplexer that has a long, slow-settling tail. This sort of distortion is highly visible on a video monitor.

Composite video systems, such as NTSC, are inherently band limited and thus edge-rate limited. In a sharply band limited system, the introduction of signals that contain significant energy higher in frequency than the filter cutoff will cause distortion of transient waveforms (see Figure 103). Filters used to control the bandwidth of these video systems should be group-delay equalized to minimize this pulse distortion. Additionally, in a band limited system, the edge rates of switching glitches or level-to-level transitions should be controlled to prevent ringing and other pulse aberrations that could be visible. In practice, this is usually accomplished with pulse-shaping networks (Bessel filters are one example). Pulse-shaping networks and delay equalized filters add cost and complexity to video systems and are usually found only on expensive equipment. Where cost is a determining factor in system design, the exceptionally low amplitude and brief duration of the LT1204's switching artifact make it an excellent choice for active video switching.

Some Definitions—

"Picture in picture" refers to the production effect in which one video image is inserted within the boundaries of another. The process may be as simple as splitting the screen down the middle or it may involve switching the two images along a complicated geometric boundary. In order to make the composite picture stable and viewable, both video signals must be in horizontal and vertical sync. For composite color signals the signals must also be in subcarrier lock.

"Keying" is the process of switching among two or more video signals, triggering on some characteristic of one of the signals. For instance, a chroma keyer will switch on the presence of a particular color. Chroma keyers are used to insert a portion of one scene into another. In a commonly used effect, the TV weather person (the "talent") appears to be standing in front of a computer generated weather map. Actually, the talent is standing in front of a specially colored background; the weather map is a separate video signal which has been carefully prepared to contain none of that particular color. When the chroma keyer senses the keying color, it switches to the weather map background. Where there is no keying color, the keyer switches to the talent's image.

[1] Video production, in the most general sense, means any purposeful manipulation of the video signal, whether in a television studio or on a desktop PC.

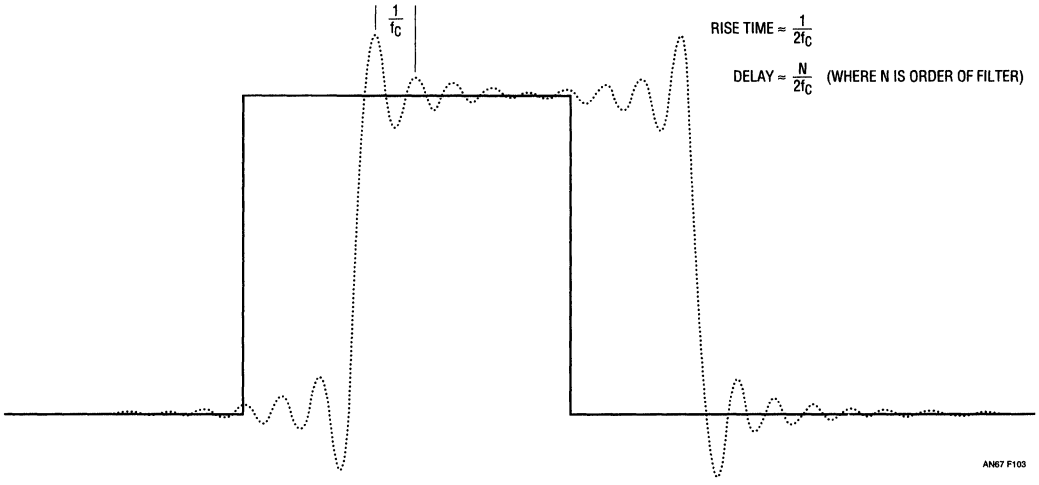


Figure 103. Pulse Response of an Ideal Sharp Cutoff Filter at Frequency f_C

APPLICATIONS FOR THE LT1113 DUAL JFET OP AMP

by Alexander Strong

Figure 104 shows a low noise hydrophone amplifier with a DC servo. Here one half (A) of the LT1113 is configured in the noninverting mode to amplify a voltage signal from the hydrophone, and the other half (B) of the LT1113 nulls errors due to voltage and current offsets of amplifier A and to null out DC errors of the hydrophone. The value of C1 depends on the capacitance of the hydrophone, which can range from 200pF to 8000pF. The time constant of the servo should be larger than the time constant of the hydrophone capacitance and the 100M source resistance. This will prevent the servo from canceling the low frequency signals from the hydrophone.

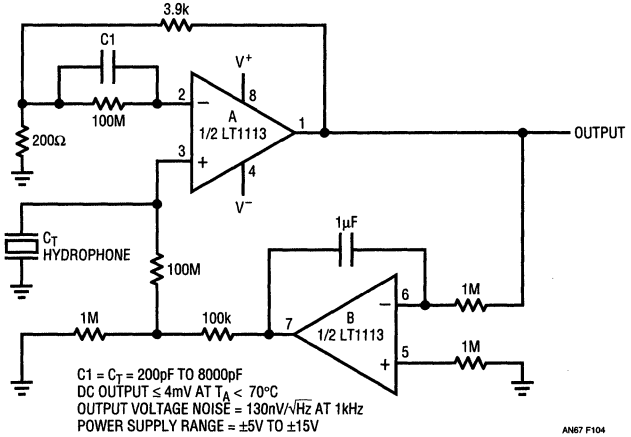


Figure 104. Low Noise Hydrophone Amplifier with DC Servo

Another popular charge-output transducer is the accelerometer. Since precision accelerometers are charge-output devices, the inverting mode is used to convert the transducer charge to an output voltage. Figure 105 is an example of an accelerometer with a DC servo. The charge from the transducer is converted to a voltage by C1, which should equal the transducer capacitance plus the input capacitance of the op amp. The noise gain will be 1 + C1/C_T. The low frequency bandwidth of the amplifier will depend on the value of R1 • C1 (or R1 (1 + R2/R3) for a Tee network). As with the hydrophone example, the time constant of the servo (1/R5C5) should be larger than the time constant of the amplifier (1/R1C1).

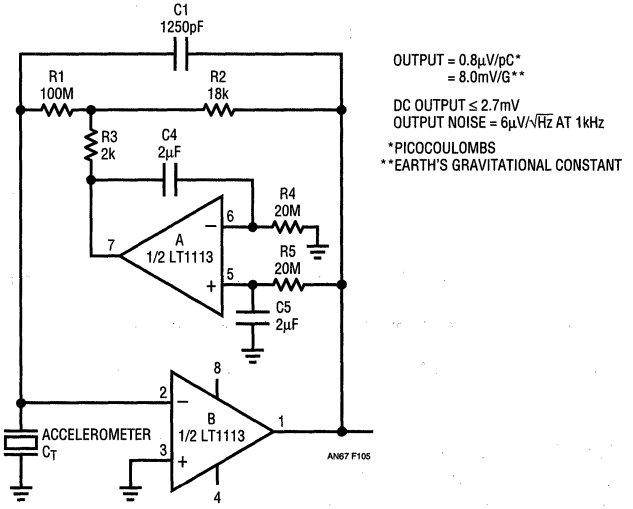


Figure 105. Accelerometer Amplifier with DC Servo

LT1206 AND LT1115 MAKE LOW NOISE AUDIO LINE DRIVER

by William Jett

Although the wide bandwidth and high output drive capabilities of the LT1206 make it a natural for video circuits, these characteristics are also useful for audio applications. Figure 106 shows the LT1206 combined with the LT1115 low noise amplifier to form a very low noise, low distortion audio buffer with a gain of 10. With a 32Ω load and a $5V_{RMS}$ output level (780mW), the THD + noise for the circuit is 0.0009% at 1kHz, rising to 0.004% at 20kHz. The frequency response is flat to 0.1dB from DC to 600kHz, with a –3dB bandwidth of 4MHz. The circuit is stable with capacitive loads of 250pF or less.

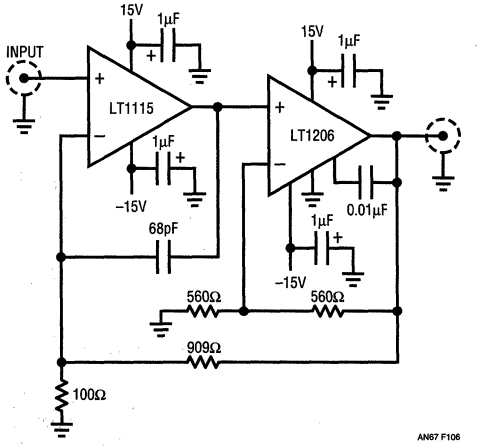


Figure 106. Low Noise × 10 Buffered Line Driver

DRIVING MULITPLE VIDEO CABLES WITH THE LT1206

by William Jett

The combination of a 60MHz bandwidth, 250mA output current capability and low output impedance makes the LT1206 ideal for driving multiple video cables. One concern when driving multiple transmission lines is the effect of an unterminated (open) line on the other outputs. Since the unterminated line creates a reflected wave that is incident on the output of the driver, a nonzero amplifier output impedance will result in crosstalk to the other lines.

Figure 107 shows the LT1206 connected as a distribution amplifier. Each line is separately terminated to minimize the effect of reflections. For systems using composite video, the differential gain and phase performance are also important and have been considered in the internal design of the device. The differential phase and differential gain performance versus supply is shown in Figures 108 and 109 for 1, 3, 5 and 10 cables. Figure 110 shows the output impedance versus frequency. Note that at 5MHz the output impedance is only 0.6Ω.

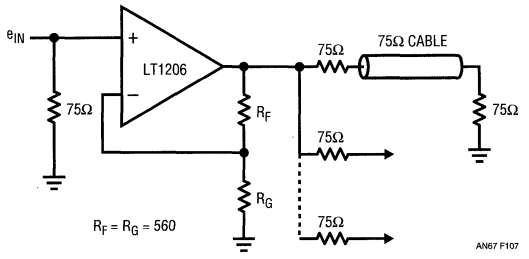


Figure 107. LT1206 Distribution Amplifier

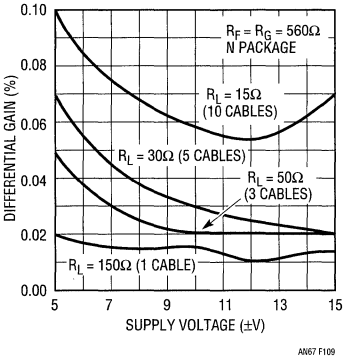


Figure 109. Differential Gain vs Supply Voltage

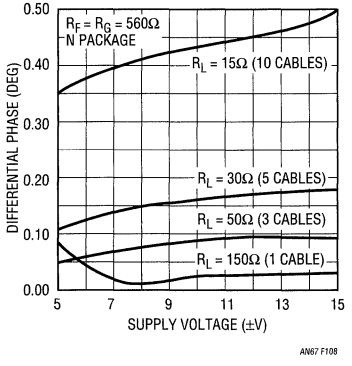


Figure 108. Differential Phase vs Supply Voltage

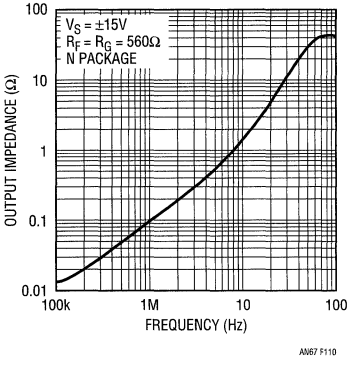


Figure 110. Output Impedance vs Frequency

OPTIMIZING A VIDEO GAIN CONTROL STAGE USING THE LT1228

by Frank Cox

Video automatic gain control (AGC) systems require a voltage- or current-controlled gain element. The performance of this gain-control element is often a limiting factor in the overall performance of the AGC loop. The gain element is subject to several, often conflicting, restraints. This is especially true of AGC for composite color video systems such as NTSC, which have exacting phase and gain distortion requirements. To preserve the best possible signal-to-noise ratio (S/N),[1] it is desirable for the input signal level to be as large as practical. Obviously, the larger the input signal the less the S/N will be degraded by the noise contribution of the gain control stage. On the other hand, the gain control element is subject to dynamic range constraints and exceeding these will result in rising levels of distortion.

Linear Technology makes a high speed transconductance (g_m) amplifier, the LT1228, which can be used as a quality, inexpensive gain control element in color video and some lower frequency RF applications. Extracting the optimum performance from video AGC systems takes careful attention to circuit details.

As an example of this optimization, consider the typical gain control circuit using the LT1228 shown in Figure 111. The input is NTSC composite video, which can cover a 10dB range, from 0.56V to 1.8V. The output is to be 1V peak-to-peak into 75Ω. Amplitudes were measured from peak negative chroma to peak positive chroma on an NTSC modulated ramp test signal (see page 74).

Notice that the signal is attenuated 20:1 by the 75Ω attenuator at the input of the LT1228, so the voltage on the input (Pin 3) ranges from 0.028V to 0.090V. This is done to limit distortion in the transconductance stage. The gain of this circuit is controlled by the current into the I_{SET} terminal, Pin 5 of the IC. In a closed-loop AGC system the loop control circuitry generates this current by comparing the output of a detector[2] to a reference voltage, integrating the difference and then converting to a suitable current. The measured performance for this circuit is presented in Table 1.

Table 1. Measured Performance Data (Uncorrected)

INPUT (V)	I_{SET} (mA)	DIFFERENTIAL GAIN	DIFFERENTIAL PHASE	S/N
0.03	1.93	0.5%	2.7°	55dB
0.06	0.90	1.2%	1.2°	56dB
0.09	0.584	10.8%	3.0°	57dB

All video measurements were taken with a Tektronix 1780R video measurement set, using test signals generated by a Tektronix TSG 120. The standard criteria for characterizing NTSC video color distortion are the differential gain and the differential phase. For a brief explanation of these tests see "Differential Gain and Phase" page 74. For this design exercise the distortion limits were set at a somewhat arbitrary 3% for differential gain and 3° for differential phase. Depending on conditions, this should be barely visible on a video monitor.

Figures 112 and 113 plot the measured differential gain and phase, respectively, against the input signal level (the

[1] Signal to noise ratio, S/N = 20 × log(RMS signal/RMS noise).

[2] One way to do this is to sample the colorburst amplitude (the nominal peak-to-peak amplitude of the colorburst for NTSC is 40% of the peak luminance) with a sample-and-hold and peak detector.

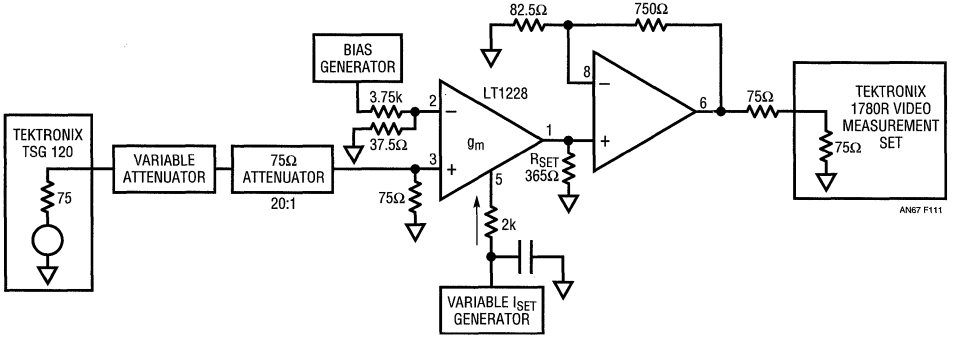


Figure 111. Schematic Diagram

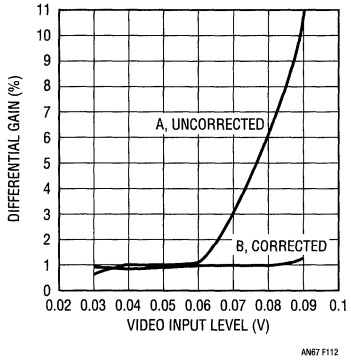


Figure 112. Differential Gain vs Input Level

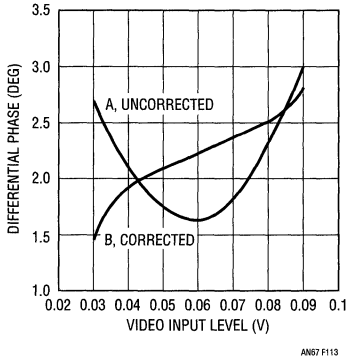


Figure 113. Differential Phase vs Input Level

curves labeled "A" show the uncorrected data from Table 1). The plots show that increasing the input signal level beyond 0.06V results in a rapid increase in the gain distortion, but comparatively little change in the phase distortion. Further attenuating the input signal (and consequently increasing the set current) would improve the differential gain performance but degrade the S/N. What this circuit needs is a good tweak.

Optimizing for Differential Gain

Referring to the small-signal transconductance versus DC input voltage graph (Figure 114), observe that the transconductance of the amplifier is linear over a region centered around 0V.[3] The 25°C g_m curve starts to become quite nonlinear above 0.050V. This explains why the differential gain (see Figure 112, curve A) degrades so quickly with signals above this level. Most RF signals do

[3]Notice also that the linear region expands with higher temperature. Heating the chip has been suggested.

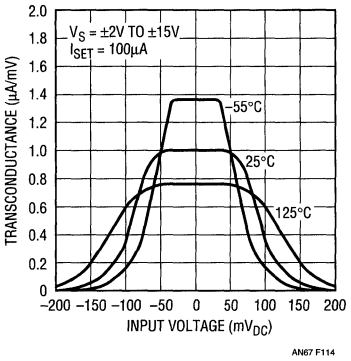


Figure 114. Small-Signal Transconductance vs DC Input Voltage

not have DC bias levels but the composite video signal is mostly unipolar.

Video is usually clamped at some DC level to allow easy processing of sync information. The sync tip, the chroma reference burst and some chroma signal information swing negative, but 80% of the signal that carries the critical color information (chroma) swings positive. Efficient use of the dynamic range of the LT1228 requires that the input signal have little or no offset. Offsetting the video signal so that the critical part of the chroma waveform is centered in the linear region of the transconductance amplifier allows a larger signal to be input before the onset of severe distortion. A simple way to do this is to bias the unused input (in this circuit the inverting input, Pin 2) with a DC level.

In a video system, it might be convenient to clamp the sync tip at a more negative voltage than usual. Clamping the signal prior to the gain-control stage is good practice because a stable DC reference level must be maintained.

The optimum value of the bias level on Pin 2 used for this evaluation was determined experimentally to be about 0.03V. The distortion tests were repeated with this bias voltage added. The results are reported in Table 2 and Figures 112 and 113 (curves B). The improvement to the differential phase is inconclusive, but the improvement in the differential gain is substantial.

Table 2. Measured Performance Data (Corrected)

INPUT (V)	BIAS VOLTAGE	I_{SET} (mA)	DIFFERENTIAL GAIN	DIFFERENTIAL PHASE	S/N
0.03	0.03	1.935	0.9%	1.45°	55dB
0.06	0.03	0.889	1.0%	2.25°	56dB
0.09	0.03	0.584	1.4%	2.85°	57dB

Differential Gain and Phase

Differential gain and phase are sensitive indications of chroma signal distortion. The NTSC system encodes color information on a separate subcarrier at 3.579545MHz. The color subcarrier is directly summed to the black and white video signal. (The black and white information is a voltage proportional to image intensity and is called luminance or luma.) Each line of video has a burst of 9 to 11 cycles of the subcarrier (so timed that it is not visible) that is used as a phase reference for demodulation of the color information of that line. The color signal is relatively immune to distortions, except for those that cause a phase shift or an amplitude error to the subcarrier during the period of the video line.

Differential gain is a measure of the gain error of a linear amplifier at the frequency of the color subcarrier. This distortion is measured with a test signal called a modulated ramp (shown in Figure 115). The modulated ramp consists of the color subcarrier frequency superimposed on a linear ramp (or sometimes on a stair step). The ramp has the duration of the active portion of a horizontal line of video. The amplitude of the ramp varies from zero to the maximum level of the luminance, which in this case, is 0.714V. The gain error corresponds to compression or expansion by the amplifier (sometimes called "incremental gain") and is expressed as a percentage of the full amplitude range. An appreciable amount of differential gain will cause the luminance to modulate the chroma, producing visual chroma distortion. The effect of differential gain errors is to change the saturation of the color being displayed. Saturation is the relative degree of dilution of a pure color with white. A 100% saturated color has 0% white, a 75% saturated color has 25% white, and so on. Pure red is 100% saturated, whereas pink is red with some percentage of white and is therefore less than 100% saturated.

Differential phase is a measure of the phase shift in a linear amplifier at the color subcarrier frequency when the modulated ramp signal is used as an input.

The phase shift is measured relative to the colorburst on the test waveform and is expressed in degrees. The visual effect of the distortion is a change in hue. Hue is that quality of perception which differentiates the frequency of the color, red from green, yellow-green from yellow, and so forth.

Three degrees of differential phase is about the lower limit that can unambiguously be detected by observers. This level of differential phase is just detectable on a video monitor as a shift in hue, mostly in the yellow-green region. Saturation errors are somewhat harder to see at these levels of distortion—3% of differential gain is very difficult to detect on a monitor. The test is performed by switching between a reference signal, SMPTE (Society of Motion Picture and Television Engineers) 75% color bars and a distorted version of the same signal, with matched signal levels. An observer is then asked to note any difference.

In professional video systems (studios, for instance) cascades of processing and gain blocks can reach hundreds of units. In order to maintain a quality video signal, the distortion contribution of each processing block must be a small fraction of the total allowed distortion budget[4] (the errors are cumulative). For this reason, high quality video amplifiers will have distortion specifications as low as a few thousandths of a degree for differential phase and a few thousandths of a percent for differential gain.

[4] From the preceding discussions, the limits on visibility are about 3° differential phase, 3% differential gain. Please note that these are not hard and fast limits. Tests of perception can be very subjective.

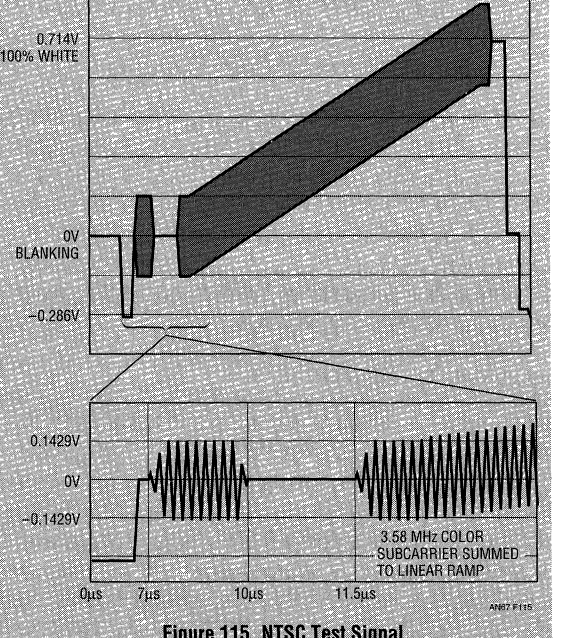


Figure 115. NTSC Test Signal

LT1190 FAMILY ULTRAHIGH SPEED OP AMP CIRCUITS

by John Wright and Mitchell Lee

Introduction

The LT1190 series op amps combine bandwidth, slew rate and output drive capability to satisfy the demands of many high speed applications. This family offers up to 350MHz gain bandwidth product and slew rates of 450V/µs while driving 150Ω (75Ω, double terminated) loads. In 50Ω systems, the LT1190 family can deliver 13.5dBm to a double terminated load. These parts are based on the familiar, easy-to-use, voltage mode feedback topology.

Small-Signal Performance

Figures 116 and 117 show the small-signal performance of the LT1190 and LT1191 when configured for gains of +1 and –1. The noninverting plots show peaking at 130MHz, which is characteristic of the socketed test fixture and supply bypass components. A tight PC board layout would reduce the LT1190 peaking to 2dB. The small-signal performance of an LM118 is shown for comparison.

Fast Peak Detectors

Fast peak detectors place unusual demands on amplifiers. The output stage must have a high slew rate in order to keep up with the intermediate stages of the amplifier. This condition causes either a long overload or DC accuracy errors. To maintain a high slew rate at the output, the amplifier must deliver large currents into the capacitive load of the detector. Other problems include amplifier instability with large capacitive loads and preservation of output voltage accuracy.

The LT1190 is the ideal candidate for this application, with a 450V/µs slew rate, 50mA output current and 70° phase margin. The closed-loop peak detector circuit of Figure 118 uses a Schottky diode inside the feedback loop to obtain good accuracy. A 20Ω resistor (R_O) isolates the 10nF load and prevents oscillation.

DC error with a sine wave input is plotted in Figure 119 for various input amplitudes. The DC value is read with a DVM. At low frequencies, the error is small and is dominated by the decay of the detector capacitor between cycles. As frequency rises, the error increases because capacitor charging time decreases. During this time the overdrive becomes a very small portion of a sine wave cycle. Finally, at approximately 4MHz, the error rises rapidly owing to the slew-rate limitation of the op amp. For comparison purposes, the error of an LM118 is also plotted for $V_{IN} = 2V_{P-P}$.

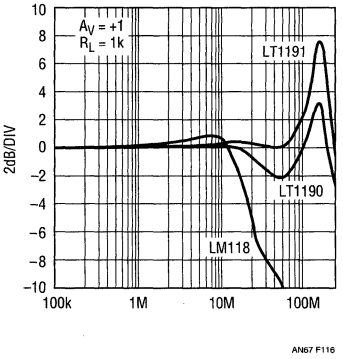


Figure 116. Small-Signal Response A_V = +1. 130MHz Peaking Due to Socket and Bypass Components

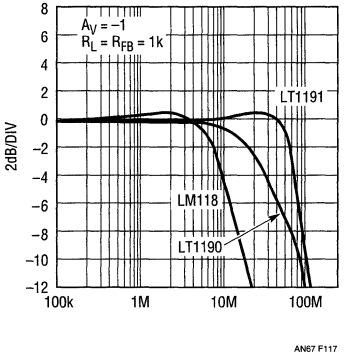


Figure 117. Small-Signal Response A_V = –1

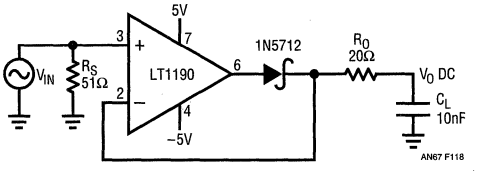


Figure 118. Closed-Loop Peak Detector

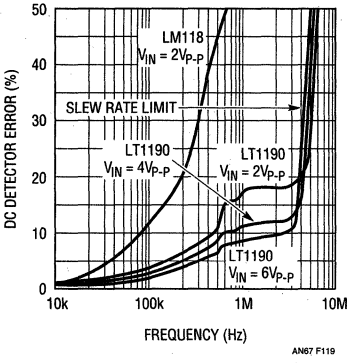


Figure 119. Closed-Loop Peak Detector Error vs Frequency

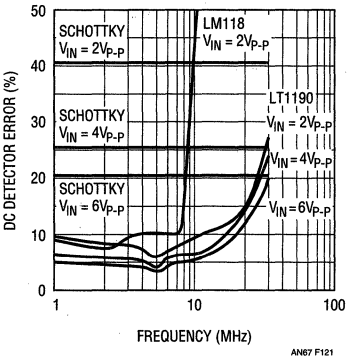


Figure 121. Open-Loop Peak Detector Error vs Frequency

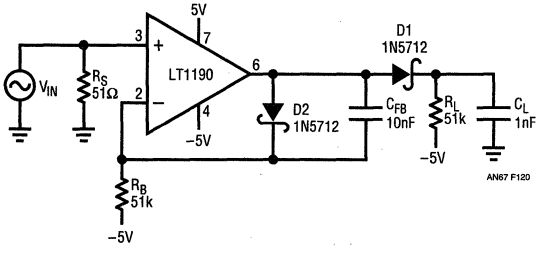


Figure 120. Open-Loop, High Speed Peak Detector

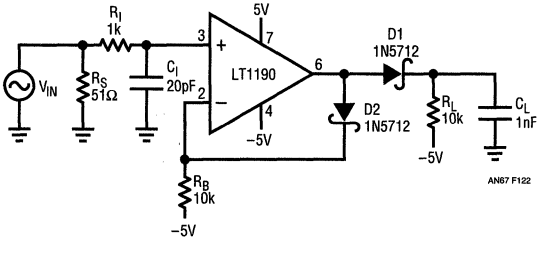


Figure 122. Fast Pulse Detector

A Schottky diode peak detector can be built with a 1nF capacitor and a 10kΩ pulldown. Although this simple circuit is very fast, it has limited usefulness because of the error of the diode threshold and its low input impedance. The accuracy of this simple detector can be improved with the LT1190 circuit of Figure 120.

In this open loop design, D1 is the detector diode and D2 is a level shifting or compensating diode. A load resistor, R_L, is connected to –5V and an identical bias resistor, R_B, is used to bias the compensating diode. Equal value resistors ensure that the diode drops are equal. Low values of R_L and R_B (1k to 10k) provide fast response, but at the expense of poor low frequency accuracy. High values of R_L and R_B provide good low frequency accuracy but cause the amplifier to slew rate limit, resulting in poor high frequency accuracy. A good compromise can be made by adding a feedback capacitor, C_{FB}, which enhances the negative slew rate on the (–) input.

The DC error with a sine wave input, as read with a DVM, is plotted in Figure 121. For comparison purposes the LM118 error is plotted as well as the error of the simple Schottky detector.

Pulse Detector

A fast pulse detector can be made with the circuit of Figure 122. A very fast input pulse will exceed the amplifier's slew rate and cause a long overload recovery time. Some amount of dV/dt limiting on the input can help this overload condition; however, it will delay the response.

Figure 123 shows the detector error versus pulse width. Figure 124 is the response to a $4V_{P-P}$ input pulse that is 80ns wide. The maximum output slew rate in the photo is 70V/μs. This rate is set by the 70mA current limit driving 1nF. As a performance benchmark, the LM118 takes 1.2μs to peak detect and settle, given the same amplitude input.

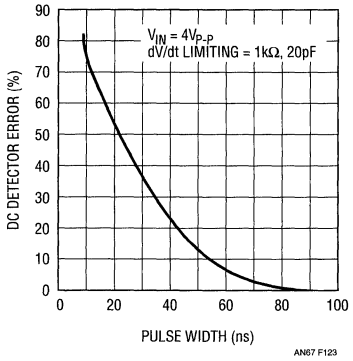


Figure 123. Detector Error vs Pulse Width

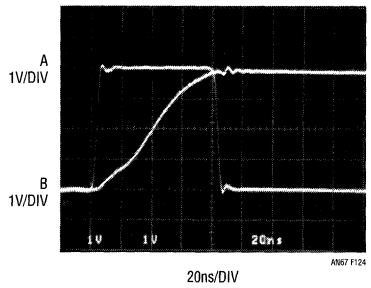


Figure 124. Open-Loop Peak Detector Response

This slower response is due in part to the much lower slew rate and lower phase margin of the LM118.

Instrumentation Amplifier Rejects High Voltage

Instrumentation amplifiers are normally used to process slowly varying outputs from transducers, rather than fast signals. However, it is possible to make an instrumentation amplifier that responds very quickly, with good common mode rejection. For the circuit of Figure 125, an LT1192 is used to obtain 50dB of CMRR from a 120V_{P-P} signal. In this application, the CMRR is limited by the matching of the resistors, which should match to better than 0.01%.

An LT1192 is used in this application because the circuit has a noise gain of 100 and because the higher gain

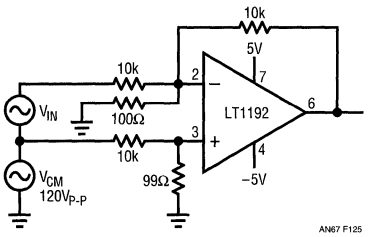


Figure 125. 3.5MHz Instrumentation Amplifier Rejects 120V_{P-P}

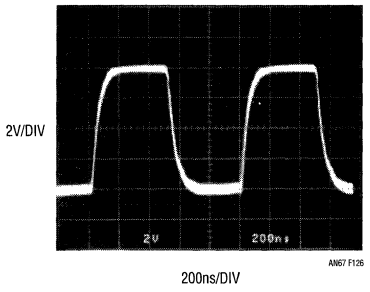


Figure 126. Open-Loop Peak Detector Response

bandwidth of the LT1192 allows a –3dB bandwidth of 3.5MHz. Note also that the 100:1 attenuation of the common mode signal presents a common mode voltage to the amplifier of only 1.2V_{P-P}. Figure 126 shows the amplifier output for a 1MHz square wave riding on a 120V_{P-P}, 60Hz signal. The circuit exhibits 50dB rejection of the common mode signal.

Crystal Oscillator

Op amps have found wide use in low frequency (≤100kHz) crystal oscillator circuits, but just haven't had the bandwidth to operate successfully at higher frequencies. The LT1190 and LT1191 make excellent gain stages for high-frequency Colpitts oscillators. A practical implementation is shown in Figure 127.

Gain limiting is provided by two Schottky diodes, which maintain the output at approximately +11dBm—sufficient to directly drive +7 or +10dBm diode-ring mixers. Output-stage clipping is not recommended as a means of gain

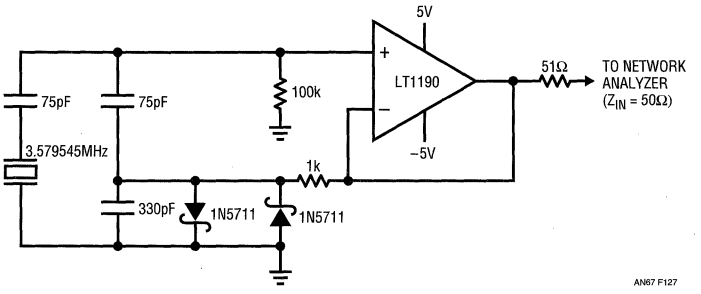


Figure 127. High Frequency Colpitts Oscillator

limiting, as this increases distortion and allows internal nodes to be overdriven. The recovery time would add excessive phase shift in the oscillator loop, degrading frequency stability.

Distortion performance is good, considering that the oscillator consists of one stage and can deliver useful output power. Figure 128 shows a spectral plot of the oscillator's output. The second harmonic is approximately 37dB down, limited primarily by the clipping action of the Schottky diodes. Power supply rejection is excellent, showing a frequency sensitivity of approximately 0.1ppm/V. The LT1190 gives acceptable performance to 10MHz, while the LT1191 extends the circuit's operating range to 20MHz.

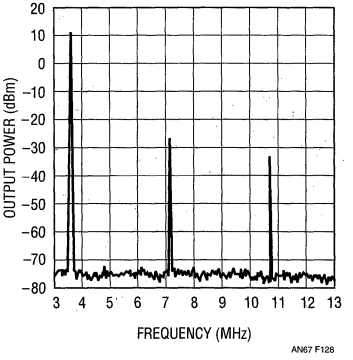


Figure 128. Oscillator Output Spectrum

AN LT1112 DUAL OUTPUT BUFFERED REFERENCE

by George Erdi

A dual output buffered reference application is shown in Figure 129.

Figure 129 works on two AA batteries, which can be discharged to ±1.3V. With two equal 20k resistors, two equal but opposite sign reference voltages are available. Changing the ratio of the two 0.1% resistors allows for other values: one positive and one negative.

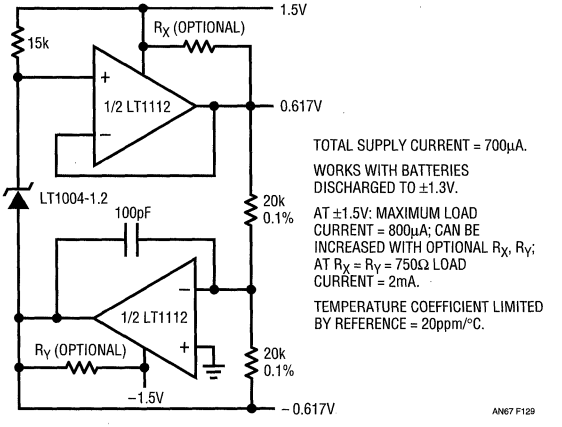


Figure 129. Dual Output Reference Operates on Two AA Cells

THREE OP AMP INSTRUMENTATION AMP USING THE LT1112/LT1114

by George Erdi

The LT1112/LT1114 are dual and quad universal precision op amps. All important precision specifications have been maintained:

1. Microvolt offset voltage; the low cost grades (including the small outline, 8-pin surface mount package) are guaranteed to 75μV.
2. Drift guaranteed to 0.5μV/°C (0.75μV/°C low cost grades)
3. Bias and offset currents are in the picoampere range, even at 125°C
4. Low noise: 0.32μV peak-to-peak, 0.1Hz to 10Hz
5. Supply current is 400μA max per amplifier
6. Voltage gain is in excess of one million

The LT1112/LT1114 also provide a full set of matching specifications, facilitating their use in such matching dependent applications as the three op amp instrumentation amplifier shown in Figure 130. The performance of this instrumentation amplifier depends only on the matching parameters not the specifications of the individual amplifiers.

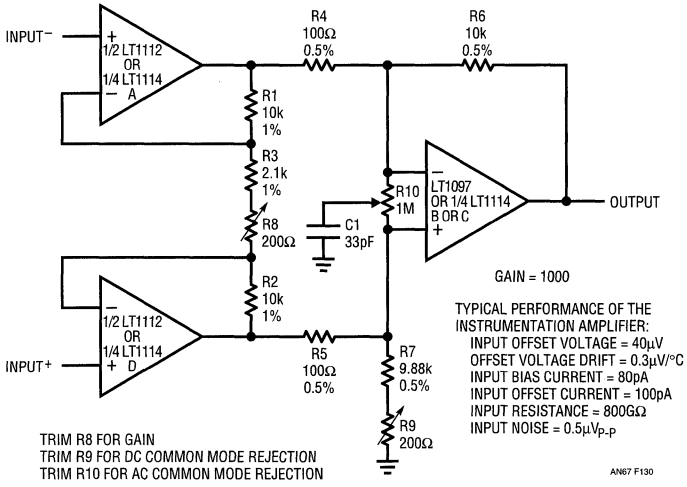


Figure 130. Three Op Amp Instrumetation Amp with Gain = 100

ULTRALOW NOISE, THREE OP AMP INSTRUMENTATION AMPLIFIER

by George Erdi and Alexander Strong

Op amp instrumentation amplifiers usually have op amps with a fixed gain greater than one at the input stage (Figure 131). At low frequencies, decompensated op amps work well, but at high frequencies and with one input grounded, the virtual ground begins to lose its integrity. As the frequency of the input signal increases, the amplitude at the virtual ground increases, making the virtual ground look inductive, eventually requiring a unity-gain stable amplifier. The LT1028 can be made stable under these conditions with bypass capacitors and a little experimenting, but the LT1128 is unconditionally stable.

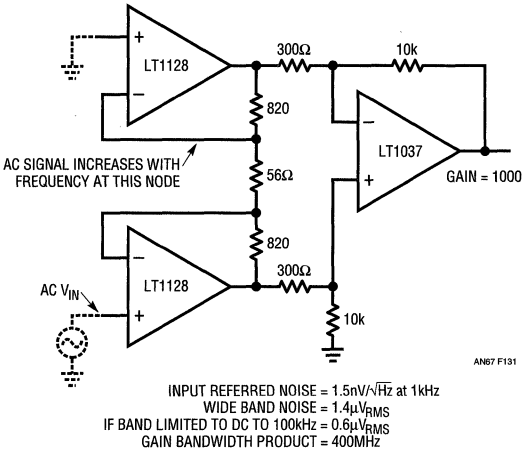


Figure 131. Three Op Amp, Ultralow Noise Instrumentation Amplifier

A TEMPERATURE COMPENSATED, VOLTAGE-CONTROLLED GAIN AMPLIFIER USING THE LT1228

by Frank Cox

It is often convenient to control the gain of a video or intermediate frequency (IF) circuit with a voltage. The LT1228, along with a suitable voltage-to-current converter circuit, forms a versatile gain control building block ideal for many of these applications. In addition to gain control over video bandwidths this circuit can add a differential input and has sufficient output drive for 50Ω systems.

The transconductance of the LT1228 is inversely proportional to absolute temperature at a rate of –0.33%/°C. For circuits using closed-loop gain control (i.e., IF or video automatic gain control) this temperature coefficient does not present a problem. However, open-loop gain control circuits that require accurate gains may require some compensation. The circuit described here uses a simple thermistor network in the voltage-to-current converter to achieve this compensation. Table 1 summarizes the circuit's performance.

Table 1. Characteristics of Example

Input Signal Range	0.5V to 3.0V pk
Desired Output Voltage	1.0V pk
Frequency Range	0Hz to 5MHz
Operating Temperature Range	0°C to 50°C
Supply Voltages	±15V
Output Load	150Ω (75Ω + 75Ω)
Control Voltage vs Gain Relationship	0V to 5V Min to Max Gain
Gain Variation Over Temperature	±3% from Gain at 25°C

Figure 132 shows the complete schematic of the gain control amplifier. Please note that these component choices are not the only ones that will work nor are they necessarily the best. This circuit is intended to demonstrate one approach out of many for this very versatile part and, as always, the designer's engineering judgment must be fully engaged. Selection of the values for the input attenuator, gain-set resistor and current feedback amplifier resistors is relatively straightforward, although some iteration is usually necessary. For the best bandwidth, remember to keep the gain-set resistor, R1, as small as possible and the set current as large as possible (with due regard for gain

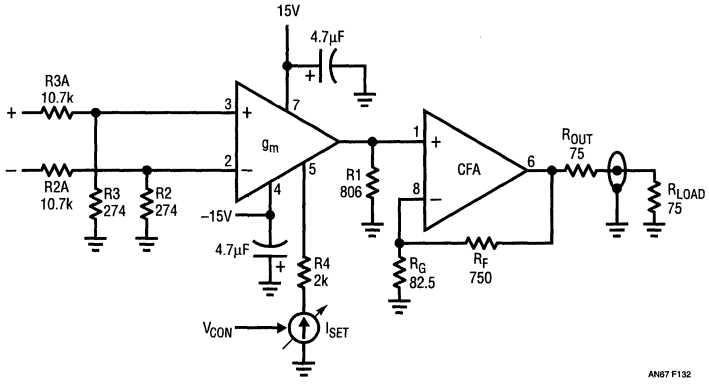


Figure 132. Differential Input, Variable Gain Amplifier

compression). The voltage-controlled current source (I_{SET}) is detailed in the boxed section.

Several of these circuits have been built and tested using various gain options and different thermistor values. Test results for one of these circuits are shown in Figure 133. The gain error versus temperature for this circuit is well within the limit of ±3%. Compensation over a much wider range of temperatures or to tighter tolerances is possible, but would generally require more sophisticated methods, such as multiple thermistor networks.

The VCCS is a standard circuit with the exception of the current set resistor R5, which is made to have a temperature coefficient of –0.33%/°C. R6 sets the overall gain and is made adjustable to trim out the initial tolerance in the LT1228 gain characteristic. A resistor (R_P) in parallel with the thermistor will tend, over a relatively small range, to linearize the change in resistance of the combination with temperature. R_S trims the temperature coefficient of the network to the desired value.

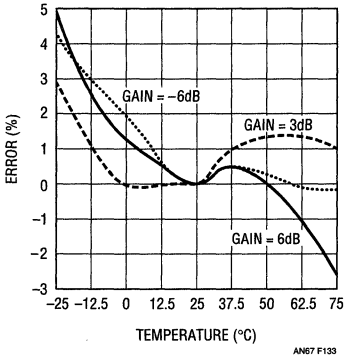


Figure 133. Gain Error for the Circuit in Figure 132 Plus the Temperature Compensation Circuit Shown in Figure 134 (Normalized to Gain at 25°C)

Voltage Controlled Current Source (VCCS) with a Compensating Temperature Coefficient

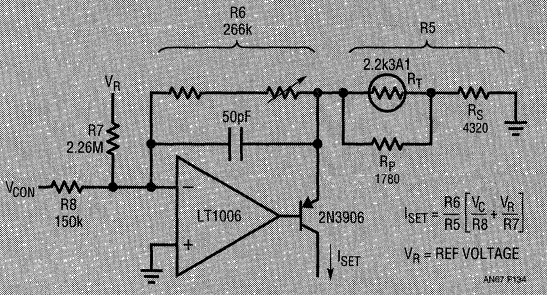


Figure 134. Voltage Controlled Current Source (VCCS) with a Compensating Temperature Coefficient

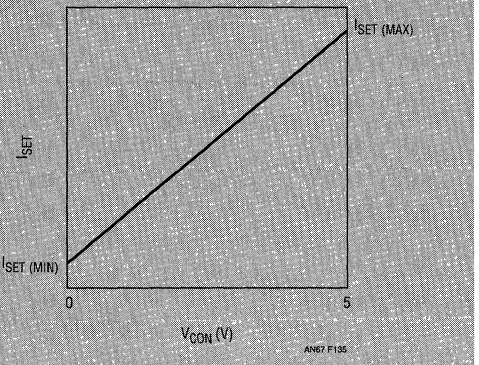


Figure 135. Voltage Control of I_{SET} with Temperature Compensation

VCCS Design Steps

1. Measure or obtain from the data sheet the thermistor resistance at three equally spaced temperatures (in this case 0°C, 25°C and 50°C). Find R_P from:

$$RP = \frac{(R0 \bullet R25 + R25 \bullet R50 - 2 \bullet R0 \bullet R50)}{(R0 + R50 - 2 \bullet R25)}$$

where: R0 = thermistor resistance at 0°C
R25 = thermistor resistance at 25°C
R50 = thermistor resistance at 50°C

2. Resistor R_P is placed in parallel with the thermistor. This network has a temperature dependence that is approximately linear over the range given (0°C to 50°C).

3. The parallel combination of the thermistor and R_P ($R_P||R_T$) has a temperature coefficient of resistance (TC) given by:

$$TC\ R_P||R_T = \left(\frac{R0||R_P - R50||R_P}{R25||R_P}\right)\left(\frac{100}{T_{HIGH} - T_{LOW}}\right)$$

where: T_{HIGH} = the high temperature
T_{LOW} = the low temperature
R_T = the thermistor

4. The desired temp. co. to compensate the LT1228 gain temperature dependence is −0.33%/°C. A series resistance (R_S) is added to the parallel network to trim its TC to the proper value. R_S is given by:

$$\left(\frac{TC\ R_P||R_T}{-0.33}\right)(R_P||R25) - (R_P||R_T)$$

5. R6 contributes to the resultant temperature and so is made large with respect to R5.

6. The other resistors are calculated to give the desired range of I_{SET}.

This procedure was performed using a variety of thermistors (one possible source is BetaTHERM Corporation—phone 508-842-0516). Figure 5 shows typical results reported as errors normalized to a resistance with a −0.33%/°C temperature coefficient. As a practical matter, the thermistor need only have about a 10% tolerance for this gain accuracy. The sensitivity of the gain accuracy to the thermistor tolerance is decreased by the linearization network, in the same ratio as is the temperature coefficient; the room temperature gain may be trimmed with R6. Of course, particular applications require analysis of aging stability, interchangeability, package style, cost, and the contributions of the tolerances of the other components in the circuit.

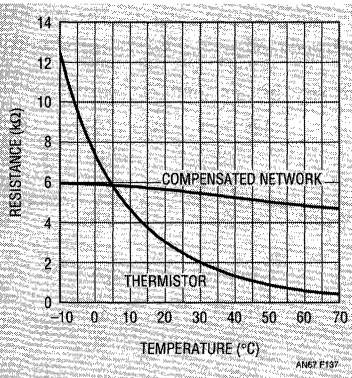


Figure 136. Thermistor and Thermistor Network Resistance vs Temperature

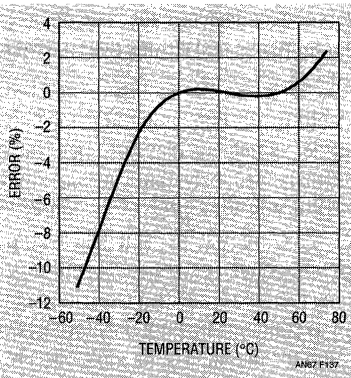


Figure 137. Thermistor Network Resistance Normalized to a Resistor with Exact –0.33%/°C Temperature Coefficient

THE LTC1100, LT1101 AND LT1102: A TRIO OF EFFECTIVE INSTRUMENTATION AMPLIFIERS

by George Erdi

Next to the universally used op amp, perhaps the most useful linear IC building block is the instrumentation amp, or "IA." Using IAs effectively can in some ways be more challenging than selecting op amps, because IAs have different specs and can also use different topologies. However, the basic task is a fixed gain, differential input, single-ended output amplifier, the definition of an IA. The differential signal typically rides on top of a common mode signal; the differential input is amplified and the common mode voltage is rejected by the IA.

The instrumentation amplifier can be implemented with dedicated IA designs, or with one to three op amps to realize the gain function, and a minimum of four ratio-matched precision resistors configured as two like ratio pairs.

The most familiar IA type is the single op amp variety, usually called a difference amplifier and shown in Figure 138. Using just two parts (one op amp and one resistor network), this IA is the height of simplicity and utility. For modest requirements it is built with just a general purpose op amp and four precision resistors. A drawback to this type of IA is that the resistor bridge loads the source. The three op amp configuration uses seven resistors and has high input impedance. It is obviously more difficult to implement than the single op amp version. A nice compromise between these two approaches is illustrated in Figure 139. This IA design uses two op amps to buffer the signal inputs and requires only four resistors. The use of two op

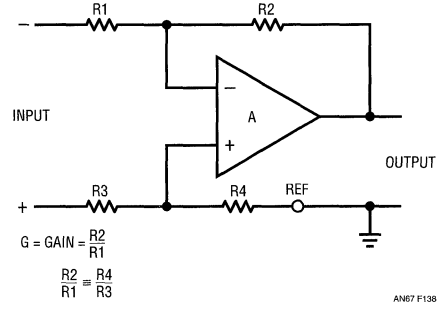


Figure 138. Basic Single Op Amp Instrumentation Amplifier

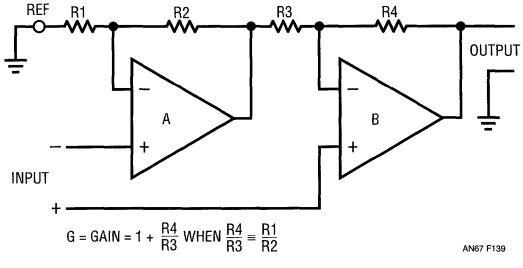


Figure 139. Buffered Dual Op Amp Instrumentation Amplifier

amps with modern dual devices causes no penalty, and in fact this arrangement has real virtues over the more basic setup of Figure 138.

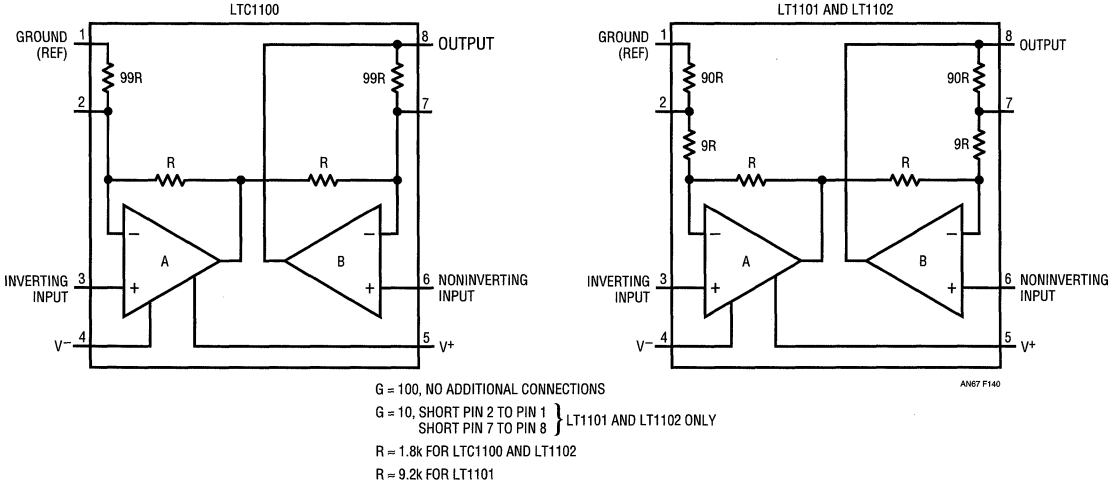
This IA architecture presents minimum loading to the differential source, namely the bias current of the op amp used, which is balanced between the two inputs. The resistor network needs very precise trimming for high common mode rejection (CMRR) and gain accuracy. The trimming is noninteractive; first the R4/R3 ratio is trimmed for gain accuracy then the R1/R2 ratio is trimmed for high CMRR. Trimming compensates not only for resistor inaccuracies, but also for the finite gain and CMRR of the op amps. The amplified difference appears between the output terminal and the voltage applied to the REF terminal (normally grounded).

As a basic building block, this IA can be performance optimized for various applications by a choice of op amps. LTC has taken this step with the LTC1100, LT1101 and LT1102, an instrumentation amplifier series offered in an 8-pin footprint with connections as shown in Figure 140. As illustrated, the gain of these IAs is user programmed by taps on the resistor array, for pre-trimmed precision gains of either 10 or 100 for the LT1101 and LT1102. The 8-pin LTC1100 has a fixed gain of 100, but makes the summing points available for user connections. The key specifications of these three devices are summarized in Table 1.

Table 1. LTC Instrumentation Amplifier Specifications[1]

	LTC1100C	LT1101C/I/M	LT1102C/I/M
Available Gains	100[2]	10/100	10/100
Gain Error (%)	0.01	0.01	0.01
Gain Nonlinearity (ppm)	3	3	7
Gain Drift (ppm/°C)	2	2	10
V_{OS} (µV)	1	60	200
V_{OS} Drift (µV/°C)	0.005	0.5	3
I_B (pA)	2.5	6000	4
I_{OS} (pA)	10	150	4
e_n	1.9µV_{P-P} (DC to 10Hz)	0.9µV_{P-P} (0.1Hz to 10Hz)	20nV/(Hz)$^{1/2}$ (at 1kHz)
CMRR (dB)	110	112	98
PSRR (dB)	130	114	102
V_S (Total, Mode)	4V to 18V (Single/Dual)	1.8V to 44V (Single/Dual)	10V to 44V (Dual)
I_S (mA)	2.4	0.09	3.4
Gain Bandwidth (MHz)	2	0.37	35
SR (V/µs)	4	0.1	30

[1] Unless otherwise stated all specifications are typical at $T_A = 25°C$. $V_S = \pm 15V$ for LT1101/LT1102 and ±5V for LTC1100.
[2] A gain option of 10/100 is available in LTC1100CS (16-Lead SW)



G = 100, NO ADDITIONAL CONNECTIONS
G = 10, SHORT PIN 2 TO PIN 1, SHORT PIN 7 TO PIN 8 } LT1101 AND LT1102 ONLY
R = 1.8k FOR LTC1100 AND LT1102
R = 9.2k FOR LT1101

Figure 140. Instrumentation Amplifiers in 8-Pin Packages

It is apparent from Table 1 that for these three IAs, there are no output contributions to input errors. With dedicated IA's or with the three op amp configuration there are separate specifications for input and output offset voltage, input and output drift and noise, and input and output power supply rejection ratio. To calculate system errors these input and output terms must be combined. With the LTC1100/01/02 these error calculations are simple.

With these three IA choices, the user can optimize performance for a variety of factors. The LTC1100 operates with dual or single supplies ranging from 4V to 18V, whereas the LTC1101 accepts a supply range of from 1.8V to 40V. In addition, the LT1101 consumes only 100μA standby current. For applications that require very low offset voltage and drift, the LTC1100 excels with 1μV of offset and 5nV/°C drift. Where both high speed and low bias current are important, the LT1102 is the IA of choice, albeit at a cost of slightly higher power consumption and dual supplies. As can be seen from the table, all of these devices are outstanding with regard to gain accuracy, linearity and stability. The LTC1100, which is based on a dual chopper amplifier prototype (the LTC1051), is by far the best in terms of offset and drift. Either the LTC1100 or the LT1102 could be the unit of choice in terms of lowest bias current, with the LT1102 gaining an edge at higher temperatures.

Applications Considerations

While this IA type is generally outstanding in terms of performance and simplicity, independent of the op amps, some caveats apply to using it most effectively. One concern is AC CMRR. As noted in Figure 140, the first op amp (A) is configured for unity gain, and the second op amp (B) provides all of the voltage gain. This has the effect of making the respective CMRR's frequency mismatched, since the CMRR of the higher gain, "B" side, corners at a much lower frequency. The resulting differential CMRR will therefore degrade more quickly with frequency than that of a topology with better AC balance. On the LT1102 this problem is resolved by decompensating amplifier B to gain-of-ten stability. This increases slew rate and bandwidth and also matches the CMRR rolloff with the frequencies of the two op amps when G = 10. At a gain of 100, this rolloff match no longer holds. However, connecting an 18pF capacitor between Pins 1 and 2 matches the CMRRs

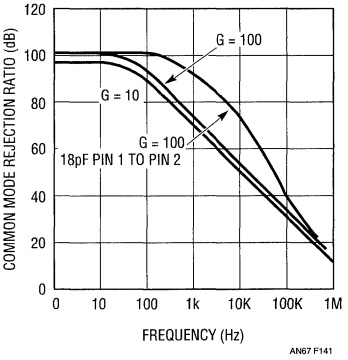


Figure 141. LT1102 Common Mode Rejection Ratio vs Frequency

of the two sides and improves CMRR by an order of magnitude in the 300Hz to 30kHz range (Figure 141). As shown on the LTC1100 and LTC1101 data sheets, similar improvements can be obtained from those devices by connecting external capacitors.

The LTC1100 and LT1101 also present some important usage considerations because of their single supply abilities, i.e., when operating with the V^- terminal tied to ground. In this configuration, these devices handle CM inputs near ground and voltage swings to ground and their reference terminals can be tied to ground. One of the most common uses of these two IAs is as bridge amplifiers in conjunction with single supply powered DC strain gauges. As such, these IAs have a unique ability to deliver high gain with precision, while operating with a 1/2 supply voltage CM input. At first glance, it appears that a dual supply IA could operate, for example, on a 9V battery supply with 4.5V common mode input, but its output will not swing to ground and its reference terminal cannot be tied to ground.

For SPICE simulation purposes, a model for the LT1101 is included in the LTC macromodel library. The model is configured as the resistor network shown for the LT1101, combined with a model for the LT1078. A similar model for the LTC1100 can be made by scaling the four resistors appropriately, and using an LTC1051 model from the same library. A close model approximation for the LT1102 can be made with the LT1102 resistor values, combined with an LT1057 model for the "A" side, and a LT1022 model for the "B" side (both also in the library).

Miscellaneous Circuits

DRIVING A HIGH LEVEL DIODE RING MIXER WITH AN OPERATIONAL AMPLIFIER

by Mitchell Lee

One of the most popular RF building blocks is the diode ring mixer. Consisting of a diode ring and two coupling transformers, this simple device is a favorite with RF designers anywhere a quick multiplication is required, as in frequency conversion, frequency synthesis or phase detection. In many applications these mixers are driven from an oscillator. Rarely does anyone try building an oscillator capable of delivering 7dBm for a "minimum geometry" mixer, let alone one of higher level. One or more stages of amplification are added to achieve the drive level required by the mixer. The new LT1206 high speed amplifier makes it possible to amplify an oscillator to 27dBm in one stage.

Figure 143 shows the complete circuit diagram for a crystal oscillator, LT1206 op amp/buffer and diode-ring mixer. Most of the components are used in the oscillator itself, which is of the Colpitts class. Borrowing from a technique used in Hewlett Packard's Unit Oscillator, the current of the crystal is amplified rather than the voltage. There are several advantages to this method, the most important of which is low distortion. Although the voltages present in this circuit have poor wave shape and are sensitive to loading, the crystal current represents essentially a filtered version of the voltage waveform and is relatively tolerant of loading effects.

The impedance, and therefore the voltage at the bottom of the crystal, is kept low by injecting the current into the summing node of an LT1206 current feedback amplifier. Loop gain reduces the input impedance to well under 1Ω. Oscillator bias is adjustable, allowing control of the mixer drive. This also provides a convenient point for closing an output power servo loop.

Operating from ±15V supplies, the LT1206 can deliver 32dBm to a 50Ω load, and with a little extra headroom (the absolute maximum supply voltage is ±18V), it can reach 2W output power into 50Ω. Peak guaranteed output current is 250mA.

Shown in Figures 144 to 148 are spectral plots for various combinations of single and double termination at power levels ranging from +17dBm to +27dBm—not bad for an inductorless circuit. Double termination may be used to present a 50Ω source impedance to the mixer, or to isolate two or more mixers driven simultaneously from one LT1206 amplifier.

Although a 10MHz example has been presented here, the LT1206's 65MHz bandwidth makes it useful in circuits up to 30MHz. In addition, the shutdown feature can be used to interrupt drive to the mixer. When the LT1206 is shut

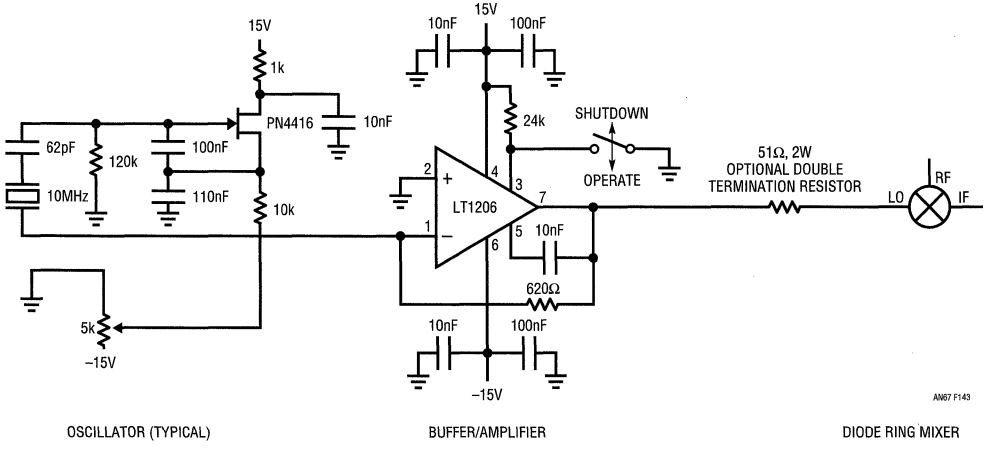


Figure 143. Oscillator Buffer Drives +17dBm to +27dBm Double Balanced Mixers

down, the oscillator will likely stop, since the crystal then sees a series impedance of 620Ω and the mixer itself. Upon re-enabling the LT1206 there will be some time delay before the oscillator returns to full power. The circuit works equally well with an LC version of the oscillator.

Note that the current feedback topology is inherently tolerant of stray capacitive effects at the summing node, making it ideal for this application. Another nice feature is the LT1206's ability to drive heavy capacitive loads while remaining stable and free of spurious oscillations.

For mixers below +17dBm, the LT1227 is a lower cost alternative, featuring 140MHz bandwidth in combination with the shutdown feature of the LT1206.

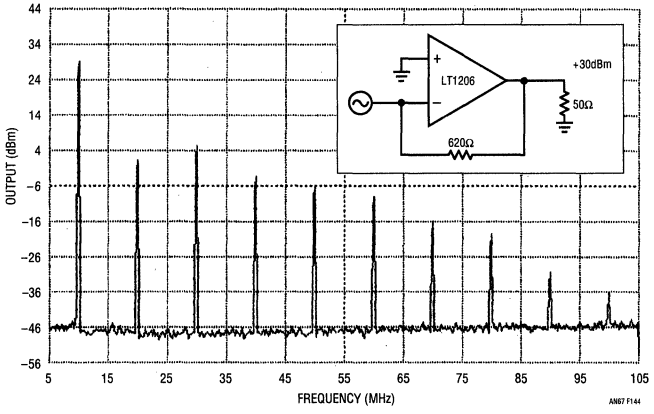


Figure 144. Spectrum Plot of Figure 143's Circuit Driving +30dBm into a 50Ω Load (Single Termination)

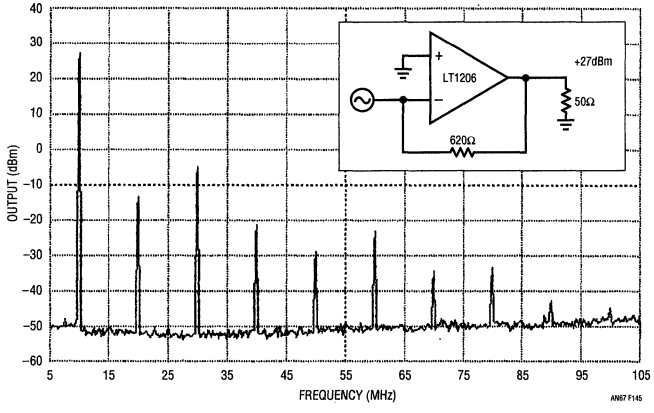


Figure 145. Spectrum Plot of Figure 143's Circuit Driving +27dBm into a 50Ω Load

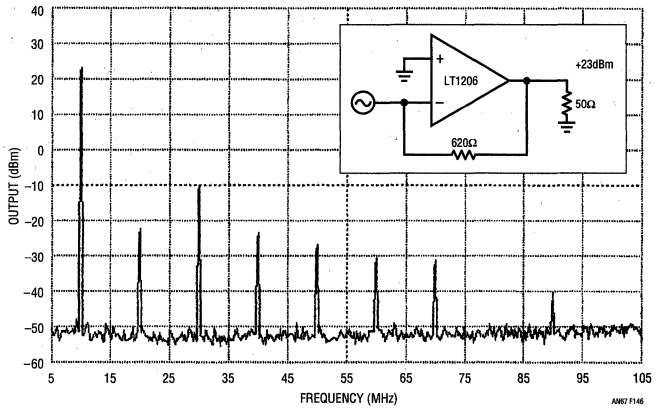


Figure 146. Spectrum Plot of Figure 143's Circuit Driving +23dBm into a 50Ω Load

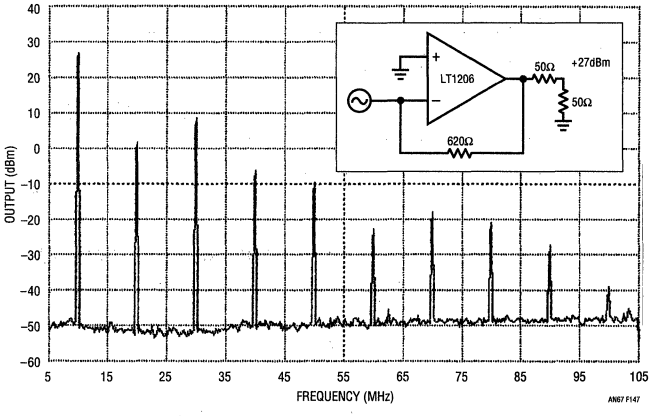


Figure 147. Spectrum Plot of Figure 143's Circuit Driving +27dBm into a 50Ω, Double Terminated Load

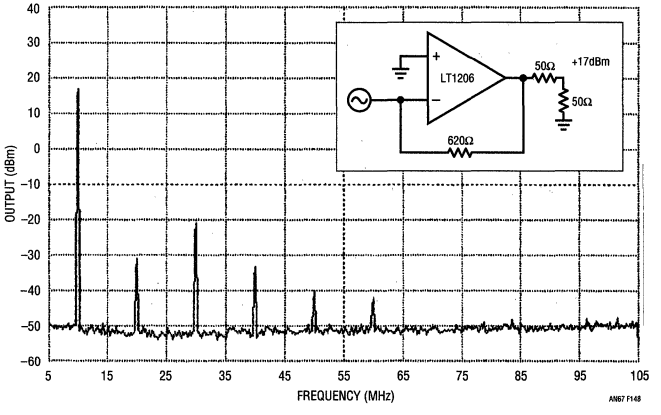


Figure 148. Spectrum Plot of Figure 143's Circuit Driving +17dBm into a 50Ω, Double Terminated Load

LT1510 Design Manual

Applications Engineering Staff

INTRODUCTION

The ever-growing popularity of portable equipment in recent years has pushed battery technologists to search for battery types that store more energy in a smaller volume, weigh less and are safer. Also, the power source selection for charging the batteries has diversified. For example, a notebook computer can be connected to a car battery, a power adapter, a docking station or even to solar cells.

The variety of input voltages, coupled with the need for high efficiency and the need for accurate constant voltage and constant current, as in the case of Li-Ion batteries (see below), have led to the introduction of a switching type constant-voltage, constant-current battery charger IC, the LT®1510.

Being a switching regulator, the LT1510 can operate over a large range of input voltages, up to 28V, with efficiency in the 90% range. Because the LT1510 operates in current mode, its output performance is not affected by input voltage changes.

An important feature of the LT1510 is its constant-current output (see Figure 1). Although other switching regulators offer current limiting, the LT1510 offers constant current with 5% accuracy. In addition, the transition from constant current to constant voltage and back is very smooth.

Only a few basic calculations are required to design with the LT1510. As the reader will see later, a voltage divider (two resistors) and a current programming resistor need to be selected for the constant voltage and constant current, respectively.

In constant-current/constant-voltage operation, the LT1510 can charge lithium-ion (Li-Ion) and sealed-lead-acid (SLA) batteries. In constant-current only operation, the LT1510 can charge nickel-metal-hydride (NiMH) and nickel-cadmium (NiCd) batteries.

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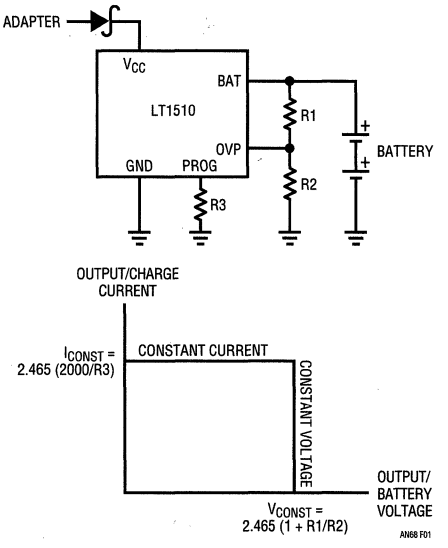


Figure 1. Constant-Current and Constant-Voltage Modes of the LT1510 with Simplified Schematic (Above)

Other advantages of designing with the LT1510 include:

- Efficiency in the 90% range
- High constant-voltage and constant-current accuracy
- An internal sense resistor that can be connected to either terminal of the battery
- Wide range of battery voltages (2V to above 20V)
- Small inductor
- Internal power switch
- Low drain in sleep mode
- Soft start
- Shutdown control
- Up to 1.5A charge current

This application note will show how to design with the LT1510 and will describe various methods of terminating the charge. Test results and test methods are included in the appendices. The circuits in this application note are constant-current and constant-current/constant-voltage battery charger circuits developed by Linear Technology Corporation. These examples are intended to serve as starting points in your design process. Most of them can be adapted to your specific application and battery chemistry needs.

Another product in the Linear Technology Corporation line of constant-current /constant-voltage battery charger ICs is the LT1511. The LT1511 offers higher charge current (3A) and total system current control. The LT1511 can be configured so that when the system current requirement increases, the charge current decreases and the total system current matches the power adapter's maximum current.

ON BATTERIES AND CHARGERS

Developing a stand-alone or embedded battery charger for today's portable products, incorporating the latest battery technology, requires careful consideration of how the system elements, including battery, charger, system controller and system load, work together.

An understanding of the charging characteristics of the battery and the application's requirements is necessary in order to design a reliable battery charger. A fast battery charger must quickly recharge a battery to full charge. Fast charging batteries requires accurate charge termination when the battery is fully charged in order to prevent damage or reduced battery life. Similarly, excessive discharging can damage any battery type.

Battery Charger Checklist

In order to organize your approach, start with the following checklist of design considerations:

- Select an appropriate battery for your application's needs
- Know your battery charging needs
  - ✓ Charging current
  - ✓ Charging voltage and its temperature dependence
  - ✓ Primary charge termination method for the battery
  - ✓ Secondary (safety) charge termination method

- ✓ Can you include a temperature sensor in your battery pack?
- ✓ Recommended charging method to achieve longest battery life
- ✓ Effect of cell temperature on charging method and charge level

- Stand-alone or embedded charger?
- What charger power source is available?
- Single or multiple battery pack charging capability?
- Environmental operating conditions
- Charging interval: standard (overnight) or fast (< 4 hours)
- Will your application draw current during battery charging?
- What kind of control do you need over your battery charger? (shutdown, fault signals, charge level signals, charge completion signals)
- What will your charger do when the battery is removed?
- What happens when a fully charged battery is "hot plugged" or "cold plugged" into the charger?
- What happens when the adapter is plugged live into the system?

Comparing Four Rechargeable Battery Chemistries

The major rechargeable batteries readily available today are nickel-cadmium (NiCd), nickel-metal-hydride (NiMH), sealed-lead-acid (SLA) and lithium-ion (Li-Ion). These batteries serve the common function of supplying renewable energy to user applications, but not every battery type is appropriate for every application. Different battery technologies have distinctive characteristics that determine their suitability for a particular use. These characteristics include energy density, cell voltage, battery internal resistance, maximum charge rate, discharge profile, life (number of charge/discharge cycles), self-discharge rate and discharge rate. Table 1 shows typical characteristics of batteries of each chemistry.

Table 1. Battery Type Characteristics

	SLA	NiCd	NiMH	Li-Ion
Energy Density (W-Hr/kg)	30	40	60	90
Energy Density (W-Hr/l)	60	100	140	210
Operating Cell Voltage (V)	2.0	1.2	1.2	3.6**
Discharge Profile	Sloping	Flat	Flat	Sloping
Life in Cycles*	500	1000	800	1000
Self-Discharge	3%/mo	15%/mo	20%/mo	6%/mo
Internal Resistance	Low	Lowest	Moderate	Highest
Discharge Rate	<5C	<10C	<3C	<2C

* Until only 80% of initial charge capacity is achievable upon recharge.
** The operating cell voltage drops during discharge. This is an average voltage.

Understand the Charging Requirements for Your Battery: Different battery chemistries have different charge requirements. The descriptions below indicate the most common charging methods for these battery types. Additional methods, such as pulse charging, are not covered here.

System reliability may require a primary and a secondary termination method for preventing overcharge.

Battery capacity is described by the bold letter **C**, which represents the capacity in ampere-hours. Charging at **C** rate means charging at a current of **C** amps (for instance, charging a 1.3AH battery at 1.3A rate). Batteries are not 100% efficient in converting charge current into stored charge. It therefore takes longer than one hour to charge a battery to full capacity when charging at the **C** rate. Consult your battery manufacturers for their recommended charging rates and methods.

- *Nickel-Cadmium:* NiCd batteries are charged with a constant-current profile. NiCd batteries can be continuously charged at the standard **C**/10 trickle rate indefinitely without excessive temperature rise or damage.

  Fast charging NiCd batteries requires a charge termination method. Primary termination can be based upon $\Delta T/\Delta t$ (rate of temperature rise) or $-\Delta V$ (cell voltage decrease at full charge) sensing. It is recommended that the secondary termination be a ΔT_{CO} (temperature rise over ambient) termination. Many manufacturers' NiCd batteries can be charged at significantly greater than the **C**/1 rate, reducing the charge time to as little as fifteen minutes.

- *Nickel-Metal-Hydride:* NiMH batteries are charged with a constant-current profile. The standard **C**/10 rate charging works well for overnight charges. NiMH batteries are more susceptible to damage from overcharging than NiCd batteries; the charge must therefore be reduced to **C**/40 or switched to a pulsed trickle charge after 16 hours. This can be implemented with a timer.

  Fast charging NiMH cells also require charge termination. NiMH cells exhibit a slower increase in cell voltage during charge than NiCd cells and a flatter peak. Primary termination can be based on sensing the zero dV/dt condition of the battery voltage characteristic (voltage peak) or ΔT_{CO}. Following this, the charging circuit should reduce the current to a maintenance charge of **C**/40 or a pulsed trickle charge to counteract the batteries' self-discharge characteristic. Secondary termination can be temperature related or controlled by a timer.

- *Sealed-Lead-Acid:* SLA batteries can be charged with a constant-voltage, current-limited supply or with a constant-current supply. For standby power applications, constant-voltage (float) charging is the traditional method. Charge is delivered at the current limit until the "float" voltage across the battery is reached and the voltage is then held constant while the current into the battery decreases naturally as the cells reach full charge. The float voltage of approximately 2.25V per cell can be maintained indefinitely. For longer battery life, the float voltage should change by –1mV to –5mV per °C per cell to match the cell voltage temperature dependence.

  Fast charging with the constant-voltage method is achieved by increasing the charging voltage to approximately 2.45V per cell, which extends the charging time at the current limit and reduces total charge time. When the battery voltage reaches the constant charging voltage, the current decreases naturally as the cells reach full charge. After a minimum charge-current level is reached, the charging voltage is reduced to a nominal float voltage or stopped.

  Fast charging with the constant-current method requires monitoring the battery voltage. Consult manufacturers' data sheets for battery characteristic details.

- *Lithium-Ion:* Li-Ion batteries are charged with a constant-voltage, current-limited supply. These batteries require special attention due to their susceptibility to damage in overcharge, deep-discharge and short-circuit conditions. Constant current is supplied until the cell voltage reaches 4.1V or 4.2V per cell (depending on the manufacturer), followed by constant-voltage charging with the required accuracy of ±50mV per cell. The charging current then tapers down naturally. Increased battery cycle life may be achieved by terminating the charge 30 to 90 minutes after the charging current drops below some current threshold.

  Several manufacturers include fault-sensing and current-balancing circuits within the battery pack. The fault-sensing circuit will open a series connection within the battery pack in the event of excessive cell voltage, discharge current or temperature, or in the event of an undervoltage condition. The use of battery packs containing appropriate cell monitor/control devices is recommended. The current-balancing circuit diverts charge current from fully charged cells to partially charged cells.

Charge Termination Techniques: To prevent battery damage and extend battery cycle life with fast charging, it is necessary to terminate charging after NiCd and NiMH cells have reached full charge. In addition, it is a recommended practice to provide a secondary charge termination method as a safety measure. Some charge algorithms include "top-off" charge stages before completing the charge.

A number of methods have been used to detect the fully charged condition of a battery and terminate the charge. Several reliable termination methods are based on the thermal release of energy in the battery near full charge. The voltage characteristic of a battery during constant-current charge is also an indicator of the electrochemical process of battery cell recharging, and several of the following methods are based on battery voltage. Not all termination methods are good for all battery types.

The most common termination techniques are discussed below. The best suited battery for the termination is given in parenthesis.

- I_{MIN}: After the charger has reached a constant-voltage state, the charge current tapers off. Termination is triggered when the current drops below a set current threshold. (Li-Ion, SLA)
- dT/dt detects the rate of change in temperature with time. Termination can be based on a maximum dT/dt, such as 1°C/min for NiCd. (NiCd)
- ΔT_{CO} (delta temperature cutoff) detects temperature rise over ambient temperature. Terminates on preset threshold temperature differential. (NiCd, SLA)
- T_{CO} (temperature cutoff) represents an absolute battery temperature at which the charge is terminated. (NiCd, NiMH)
- $-\Delta V$ (negative delta V): At constant current, NiCd and NiMH batteries exhibit a temperature rise toward the end of charge. Since they have a negative temperature coefficient, their voltage drops. Termination is activated when a decrease in battery voltage is detected. (NiCd, NiMH)
- dV/dt (slope of voltage time curve) detects the rate of change of battery voltage with time at constant-current charge. (NiCd)
- Zero dV/dt (zero voltage change) detects the actual peak voltage at constant-current charge. (NiMH)
- Slope inflection method (using the second derivative of V_{BAT} versus time) detects the negative going, zero-crossing rate of change in slope of the voltage/time curve just before charge completion. (NiCd)
- Threshold voltage detection terminates charge or reduces charge current significantly when the battery reaches a certain maximum voltage.
- Timer sets the maximum charging time limit and terminates when the limit is reached. (Li-Ion, NiCd, NiMH, SLA)

Table 2 summarizes the standard charge and fast charge information.

Table 2. Battery Charging Characteristics

	SLA	NiCd	NiMH	Li-Ion
	Current Limit Float Voltage	Constant Current	Constant Current	Current Limit Constant Voltage
Standard Charge				
Constant Current (A)	0.25**C**	0.1**C**	0.1**C**	0.1**C**
Constant Voltage (V/Cell)	2.25	1.50	1.50	4.1V or 4.2V±50mV
Time (hours)	24	16	16	
Temperature Range	0°/45°C	5°/40°C	5°/40°C	5°/40°C
Termination	None	None	Timer	Timer
Fast Charge				
Constant Current	>1.5**C**	>1**C**	>1**C**	1**C**
Constant Voltage (V/Cell)	2.45	1.50	1.50	4.1 or 4.2V±50mV
Typical Time (hours)	<1.5	<3	<3	<2.5
Temperature Range	0°/30°C	15°/40°C	15°/40°C	10°/40°C
Primary Termination	I_{MIN}*	dT/dt	Zero dV/dt	I_{MIN}*+ Timer
	ΔT_{CO}	$-\Delta V$	$-\Delta V$	dT/dt
		Slope Inflection		ΔT_{CO}
		ΔT_{CO}		
Secondary Termination	Timer	T_{CO}	T_{CO}	T_{CO}
	ΔT_{CO}	Timer	Timer	Timer

*I_{MIN} is minimum current threshold termination.

LT1510 OPERATION/BLOCK DIAGRAM

The LT1510 is a current mode, PWM (pulse-width modulated), positive buck switcher that operates in one of two states: constant current or constant voltage. Figure 2 shows a block diagram of the LT1510 along with a typical charger circuit. The main functions in the diagram can be divided into three major groups: the PWM switcher function, the constant-current function and the constant-voltage function. Only constant-current or constant-voltage components can be active at any given time. The PWM switcher function is active as long as the charger is not disabled; it includes a 200kHz oscillator, set-reset flip-flop, switch Q_{SW}, PWM comparator C1, buffer B1 and current amplifier CA2. The constant-current components include R_{S1} and CA1. The constant-voltage components include R_{S1}, CA1 and voltage amplifier VA.

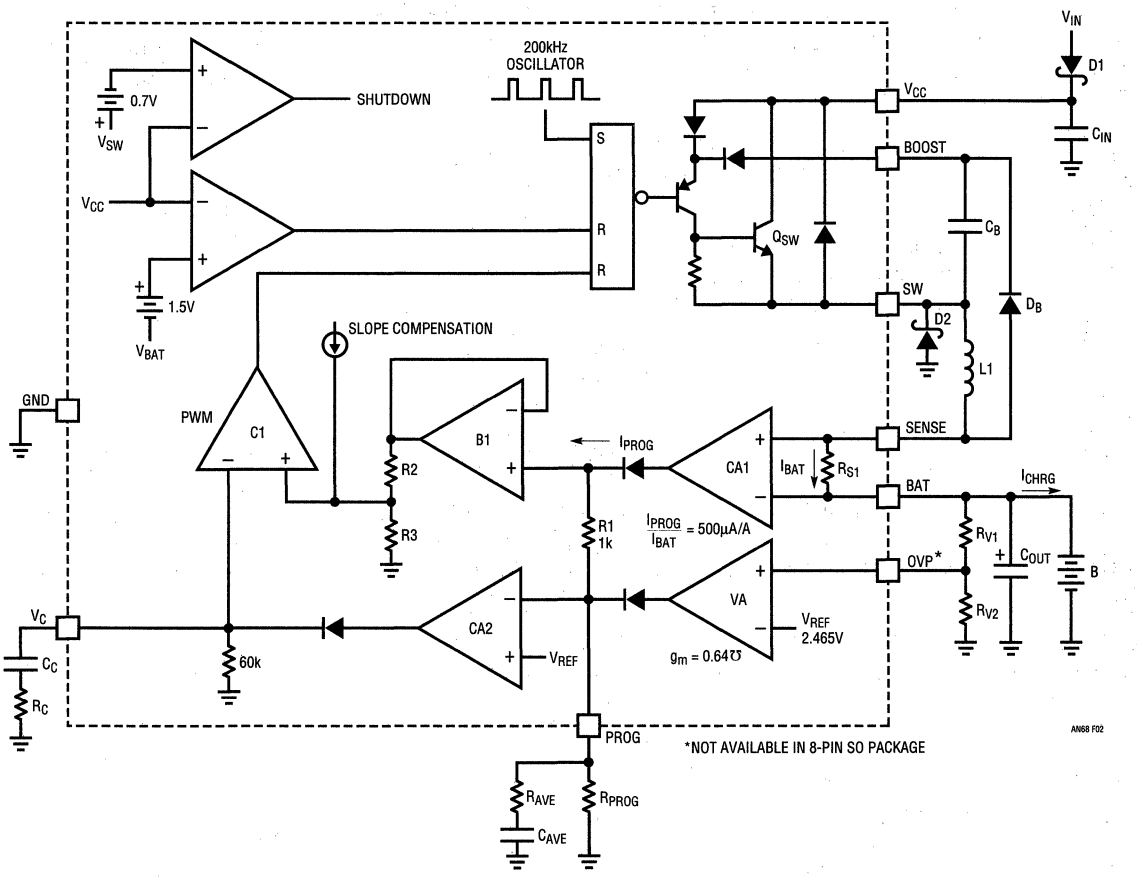


Figure 2. LT1510 Block Diagram Showing Basic Charger Circuit

In constant-current operation, the 200kHz oscillator sets the set-reset flip-flop (SR-FF), which turns Q_{SW} on. The current rise through L1, R_{S1} and B is amplified by CA1, converted from current to voltage by R1, buffered by B1 and compared to the steady-state voltage at the V_C pin by C1. When the V_C level is reached at the positive input of C1, the SR-FF resets and waits for the next 200kHz oscillator set signal. Current regulation is achieved by a slow loop containing R_{AVE}, C_{AVE}, CA2, C_C and R_C. Since CA2 and the 60k resistor constitute a high gain voltage amplifier, the voltages at its negative input (or the PROG pin) and its positive input are equal. In other words, in current mode the voltage at the PROG pin is equal to V_{REF} (2.465V).

Since the current gain of R_{S1} and CA1 is 2000, R_{PROG}'s value prescribes the constant-current current level. The charge current level can be calculated from:

$$I_{CONST} = 2.465\left(\frac{2000}{R_{PROG}}\right) \quad (01)$$

In constant-voltage operation, the 200kHz loop operates similarly to that in constant-current, but the voltage regulation is achieved by overriding R_{S1} and CA1 with voltage divider R_{V1}, R_{V2} and voltage amplifier VA. The loop regulates the voltage at the OVP pin to equal V_{REF}. The voltage at the BAT pin in a constant-voltage state is:

$$V_{CONST} = 2.465\left(\frac{R_{V1}+R_{V2}}{R_{V2}}\right) \quad (02)$$

R_{AVE} and C_{AVE} smooth the output of CA1 in the constant-current state or VA in the constant-voltage state. C_C and R_C compensate the regulation loop.

C_{IN} bypasses the input and C_{OUT} smoothes the charge current into the battery B.

Pin Descriptions

GND: This is the ground pin. There are two kinds of ground pins for the LT1510: electrical and fused. The function of the electrical ground pin is to serve as the analog ground reference for the LT1510. For best regulation in constant-voltage operation, connect the bottom side of R_{V2} as close as possible to this pin or run a separate trace from the resistor to this pin. The four pins at the corners of the 16-pin package are fused to the internal die for heat sinking. Connect these pins to expanded printed circuit board copper areas for proper heat removal.

SW: The LT1510 topology is positive buck. The NPN switch (Q_{SW}) in the positive buck topology is connected between the input supply and the inductor/catch diode node. Inside the LT1510, the bipolar switch is connected between the V_{CC} and SW pins. Keep the trace from the SW pin to D2 short and wide. To minimize generated electromagnetic interference (EMI), keep the trace from the SW pin to L1 as short and wide as possible.

BOOST: The monolithic NPN transistor selected for the switch Q_{SW} is superior to a PNP in terms of speed and collector resistance. However, its saturation voltage is limited by its base-emitter drop. The LT1510's BOOST pin provides a means of bootstrapping the drive to Q_{SW}, thereby allowing it to saturate against the input rail. Capacitor C_B, which is charged and refreshed during the off time through diode D_B and SENSE pin, acts as a bootstrap. C_B delivers base drive to Q_{SW} through the BOOST pin. For best switch performance and, consequently, best efficiency and highest switching duty cycle, connect the anode of D_B to a source of 3V to 6V that is active when the charger is.

OVP: The OVP (overvoltage protection) pin is used to program the output voltage in the constant-voltage state. The output voltage is sensed through a voltage divider comprising R_{V1} and R_{V2} and fed back to the OVP pin. The OVP feedback sense voltage is 2.465V.

SENSE: Inductor current and average charging current are controlled by monitoring an on-chip 0.08Ω sense resistor R_{S1}. This resistor is internally connected between the SENSE pin and the BAT pin. Inductor current information is used to control the buck regulator and the average current information is used to control the battery charging current. In most applications the sense resistor appears in series with the output side of the buck regulator inductor, but it is also possible to sense current at ground in the negative terminal of the battery. Do not bypass the SENSE pin. Note that the total pin-to-pin resistance is higher (0.2Ω) than the value of the sense resistor itself.

BAT: The "downstream" side of the sense resistor (see SENSE pin description) is connected to the BAT pin. In most applications the BAT pin is connected directly to the positive terminal of the battery. The BAT pin constitutes the output of the buck regulator and must therefore be bypassed. If the sense resistor is used to measure current in the negative terminal of the battery, the BAT pin can be grounded.

V_C: The V_C pin is used for frequency compensation of the buck regulator in both constant-current and constant-voltage operation. The V_C pin is also used for soft start and shutdown. A C_C capacitor of at least 0.1µF filters out noise and controls the rate of soft start. Switching starts at 0.7V; higher V_C corresponds to higher charging current in normal operation. For switching shutdown pull V_C to ground with a transistor.

PROG: The PROG pin is used to program the constant current by selecting the R_{PROG} value. C_{AVE} and R_{AVE} must be connected to the PROG pin. C_{AVE} averages the current monitored through R_{S1} so the constant-current control loop regulates the average current into the battery. During normal operation, the PROG pin voltage stays close to 2.465V. If the PROG pin is shorted to ground, the switching will stop. When a current sinking device is connected to PROG pin for the purpose of changing the constant current charge, the device has to be able to sink current at a compliance of up to 2.465V.

V_{CC}: This is the input supply to the LT1510. Short V_{CC1} and V_{CC2} together when using the 16-pin package. The

operating voltage range is 8V to 28V. Below 8V the undervoltage lockout may be activated and switching may stop; 28V is the absolute maximum value. V_{CC} must be at least 2V above the highest battery voltage. V_{CC} should not be forced to >0.7V below the SW pin because there is a parasitic diode connected from the SW pin to the V_{CC} pin. For good bypassing, a low ESR capacitor of 10µF or higher is required. The trace from the bypass capacitor to the V_{CC} pin should be as short as possible.

COMPONENT SELECTION

This section provides the user with the criteria for selecting the components of a typical circuit with 2-level constant-current (I_{CONST}) charge, constant-voltage (V_{CONST}) charge and charge disable, as shown in Figure 3.

When selecting components, keep the following points in mind:

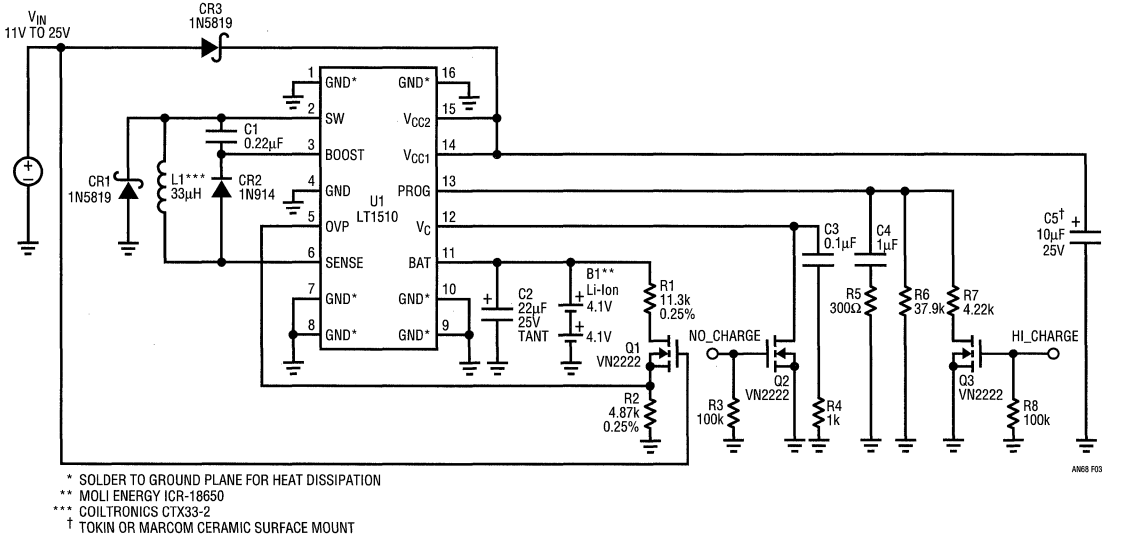
- The topology of the LT1510 is positive buck.
- The average output current is regulated in the constant-current state.
- The average output voltage is regulated in the constant-voltage state.
- The switching frequency is 200kHz.
- The recommended parts will operate over the full input and output ranges at a constant current of up to 1.3A.

The critical parameters for parts selection are discussed in the following paragraphs. The designer must apply safety margins as necessary for the system.

CA1 (internal to the LT1510) has 700µA of input bias current typically. (This current flows *into* the BAT pin or SENSE pin.) This current is supplied by the step-down converter (through the SENSE pin) when the charger is active. When the charger is in shutdown mode (V_C < 0.3V), there is an inherent BAT pin source current of 375µA maximum that flows *out* of the BAT pin. When the battery is present, it will absorb this current regardless of the values of R1 and R2. However, if the battery is removed and the charger is in shutdown mode, the output voltage at BAT pin can rise to a voltage as high as:

[(R1 + R2)(375µA)] volts

If the output voltage must stay below battery voltage when the battery is removed, the divider current must be at least 375µA. Adding a switch transistor, Q1, as shown in Figure 3, takes care of the increased battery drain. When V_{IN} is



* SOLDER TO GROUND PLANE FOR HEAT DISSIPATION
** MOLI ENERGY ICR-18650
*** COILTRONICS CTX33-2
† TOKIN OR MARCOM CERAMIC SURFACE MOUNT

Figure 3. A Typical LT1510 Based Li-Ion Charger Circuit

removed, Q1 is off and battery drain is prevented. If there are high frequency components at V_{IN}, they may pass through the gate to source capacitance of Q1 to the OVP pin. An added 220k resistor between V_{IN} and the gate of Q1 attenuates the high frequency signal.

For better efficiency, it is recommended that the anode of CR2 be connected to a voltage source between 3V and 6V. A 10µF ceramic bypass capacitor should be connected to the anode with a short lead.

Care must be taken when selecting input and output capacitors. They should be rated at 200kHz and have adequate ripple current rating. Poor choice of input or output capacitors may be detected too late. The input capacitor should be able to withstand the high surge current that occurs when a power adaptor is hot-plugged to the charger. The output capacitor should be able to withstand the high surge current that occurs when a battery is replaced. Tantalum capacitors have a known failure mechanism when subjected to high surge currents. The surge current ratings of tantalum capacitors are proportional to their voltage ratings. Consult the manufacturer. The actual capacitance is not critical in most cases.

High capacity ceramic capacitors by Tokin or United Chemi-Con/MARCOM and electrolytic OS-CON capacitors by Sanyo are recommended for the input. Solid tantalum capacitors such as AVX TPS and Sprague 593D are recommended for the output.

Boost Capacitor (C1) Selection

A 0.22µF ceramic capacitor will work under all conditions. The voltage across C1 is the battery voltage. An AVX 12065C224MAT2A surface mount capacitor performs well.

Output Capacitor (C2) Selection

C2 removes the high frequency components of (smoothes) the battery charge current.

The highest transient current through C2 occurs when the battery is plugged in and the power adapter is not live. The transient current magnitude depends on circuit construction and the components in the power path (traces, leads, solder joints, etc.). The AVX TPSD226M025R0200 (22µF, 25V, tantalum, SMT) withstands transient current equal to the operating voltage in amps (in other words, 25A for 25V operating voltage).

The RMS ripple current can be calculated from:

$$I_{RIPPLE} = \frac{(V_{CC} - V_{BAT})(V_{BAT})(0.29)}{(L)(V_{CC})(f)} \quad (03)$$

where:

V_{CC} is the maximum voltage at the V_{CC} pin

V_{BAT} is the voltage at BAT pin

f is the switching frequency (200kHz)

L is the minimum inductance of L1

For example, if the input voltage is 12V to 20V, the inductor, L1, is 30µH ±8% and drops 35% maximum at the charge current of 1A and the battery is a 3-cell NiCd, the following values should be plugged into the equation above:

V_{BAT} = (1.6)(3) = 4.8V

V_{CC} = 20V

L = (30)(0.92)(0.65) = 17.9µH

After plugging the numbers in, the calculated maximum ripple current is 0.3A RMS.

Compensation Capacitor (C3) Selection

A 0.1µF ceramic surface mount capacitor, such as the AVX 12065C104MAT2A, performs well and gives a soft start duration of 3ms. For a longer soft start duration, a larger value is required.

PROG Pin Capacitor (C4) Selection

This capacitor averages the output of CA1 (PROG pin) for the constant-current loop. A 1µF ceramic capacitor is recommended. The AVX 12063G105ZAT2A surface mount capacitor performs well. A 300Ω resistor (see PROG pin resistor) is required in series with C4.

Input Capacitor (C5) Selection

C5 bypasses the input supply for the LT1510. It is assumed that C5 conducts all input AC switching current. The maximum RMS ripple current through C5 is approximately half the DC charging current. A high transient current flows through the input capacitor when a power adapter is "hot plugged" to the charger. A Tokin 1E106Z5YU-C304F-T (10µF, 25V, ceramic, SMT) performs well. Other alternatives are ceramic capacitors by United Chemi-Con/MARCON, OS-CON capacitors by Sanyo and high ripple current electrolytics. Caution must be exercised when using tantalum capacitor for bypassing. Only a few tantalum capacitor types, such as AVX TPS and Sprague 593D series, have the ripple and transient current ratings required. Consult the manufacturer.

The trace from C5 to the V_{CC} pin of the LT1510 and to the ground plane should be as short and wide as possible.

Catch Diode (CR1) Selection

CR1 serves as the catch diode in the schematic of Figure 3. The reverse voltage across it is V_{IN} and the maximum average forward current is:

$$I_{CR1(AVE)} = \left(\frac{I_{OUT}}{V_{IN}}\right)\left(V_{IN} - V_{OUT}\right) \quad (04)$$

where:

I_{OUT} is the maximum output current,

V_{IN} is the maximum input voltage and

V_{OUT} is the lowest output voltage.

A high speed Schottky power rectifier is recommended. A Motorola 1N5819 (leaded) or MBRS140LT3 (SMT) performs well.

Boost Diode (CR2) Selection

The maximum reverse voltage of CR2 is V_{IN}. The average current is the BOOST pin current, which can be found in the "Switch Current vs Boost Current vs Boost Voltage" graph in Figure 4. The peak current is higher. A switching diode, such as the Motorola 1N914 (leaded) or MMBD914LT1 (SMT), performs well here.

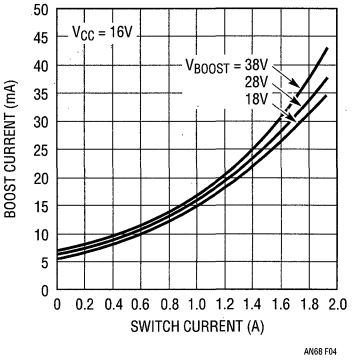


Figure 4. Switch Current vs Boost Current vs Boost Voltage

Input Diode (CR3) Selection

CR3 provides polarity protection, prevents battery drain and eliminates current transient spikes. When the power adapter is removed without the input diode, there could be battery drain through the following path; positive battery terminal, BAT pin to SENSE pin through the internal sense resistor, L1 and the SW pin to the V_{CC} pin through the internal parasitic diode.

CR3 also eliminates large current transient spikes that can occur when a power adapter with a large output capacitor is cold-plugged into the system. The current transient may compromise the input capacitor (C5) and the connector contacts unless CR3 is installed.

A low forward voltage rectifier will increase charger efficiency. The reverse voltage is the maximum battery voltage. The average forward current is:

$$I_{CR3(AVE)} = \frac{\left(I_{CHRG}\right)\left(V_{BAT}\right)}{V_{IN}} \quad (05)$$

CR3 should be able to withstand the current transient that occurs when the power adapter is "hot-plugged" to the charger. A Motorola 1N5819 (leaded) or MBRS140LT3 (SMT) performs well.

Switching Inductor (L1) Selection

L1 is an essential part of the positive buck topology as shown in Figure 3. The average current that flows through

L1 is the charge current. A 30µH inductor is acceptable for most applications. A Coiltronics CTX33-2 with windings in parallel or a Coiltronics CTX8-1 with windings in series performs well.

L1's maximum peak current can be calculated from:

$$I_{L1(PEAK)} = I_{CHRG} + \frac{(0.5)(V_{IN} - V_{OUT})(V_{OUT})}{(V_{IN})(L)(f)} \quad (06)$$

where:

V_{IN} is the maximum input voltage,

V_{OUT} is the lowest output (battery) voltage,

f is the switching frequency (200kHz),

L is the minimum inductance (H) of L1 and

I_{CHRG} is the maximum charge current.

Battery Drain Inhibit MOSFET (Q1) Selection

Q1's drain current is $V_{BAT}/(R1 + R2)$, when the charger is active, or 375µA when the charger is in shutdown mode. If the V_{IN} line has high frequency noise that can penetrate through the gate-to-source capacitance of Q1, it is recommended that a 220k resistor be added in series with the gate. A VN2222 or 2N7002 are typical choices for leaded or SMT parts.

Shutdown MOSFET (Q2) Selection

If the manufacturer does not recommend a float voltage (indefinite constant voltage across the battery), as in the case of Li-Ion, the charger must shut down at the end of the charge regimen. This can be achieved by forcing the V_C pin low with MOSFET Q2. The drain current is 1mA. A VN2222 or 2N7002 are typical choices for leaded or SMT parts.

High Charge MOSFET (Q3) Selection

When Q3 is on, the equivalent value of R6 and R7 in parallel becomes the constant-current programming resistor (see R6, R7 selection). The off-state drain leakage current of Q3 should be significantly lower than the programming current through R6. A VN2222 or 2N7002 are typical choices for leaded or SMT parts.

Constant-Voltage Programming Resistors (R1, R2) Selection

The programming resistors R1 and R2 divide the battery voltage (constant voltage) down to the threshold level of 2.465V. It is recommended that the voltage divider resistance R1 + R2 have a high value so that the battery drain is kept to minimum and the need for Q1 is eliminated. There is, however, a restriction: shutdown output voltage (see Page 8). If there is a limit to the output voltage when the battery is removed and the charger is in shutdown mode, then maximum allowed branch resistance is, $V_{BAT(MAX)}/375\mu A$.

If output voltage with battery removed is not an issue, divider current can be much lower. As an example, with V_{BAT} = 8.2V, and drain current of 25µA:

$$R2 \cong \frac{2.465V}{25\mu A} = 98.6k \quad (07)$$

R2 is selected as 100k.

$$R1 \cong \frac{(V_{BAT} - V_{REF})}{(2.465/R2) + 50nA} = 232.2k \quad (08)$$

R1 is selected as 232k.

Another example for a 2-cell Li-Ion battery that requires 8.2V ±100mV. The maximum output voltage in shutdown mode (with battery removed) is 8.5V.

The maximum value for R2 is:

$$R2 \leq \frac{2.465}{375\mu A} = 6.57k \quad (08.1)$$

R2 is selected as 4.87k. R1 is calculated as:

$$R1 \cong \frac{(8.2 - 2.465)}{\frac{2.465}{4.87k} + 50nA} = 11.33k \quad (09)$$

R1 is selected as 11.3k.

The battery drain current for an inactive charger is 8.4V/(4.87kΩ + 11.3kΩ) = 0.52mA. Q1 can be added to eliminate this drain current.

The recommended tolerance for R1 and R2 is 0.25%.

Compensation Resistor (R4) Selection

This resistor is part of the compensation loop. A 1k, 5% resistor is recommended for most cases. The stability of the current loop can be tested by forcing a voltage step across the output while in a constant-current state.

PROG Pin Resistor (R5) Selection

This resistor is part of the compensation loop. A 300Ω, 5% is recommended for most cases. The stability of the voltage loop can be tested by forcing a current step across the output while in a constant-voltage state.

Constant-Current Programming Resistors (R6, R7) Selection

The values of R6 and R7 can be found from the following formula:

$$R_{EQU} = \frac{(2.465)(2000)}{I_{CONST}} \quad (10)$$

where R_{EQU} equals R6 for the low constant-current charge and R6 in parallel with R7 for high constant-current charge. As an example, a 1.3AH battery has to be charged at **C** and trickle charged at **C**/10 (0.13A).

$$R6 \cong \frac{(2.465)(2000)}{0.13} = 37.9k \quad (11)$$

R6 is selected as 38.3k.

$$R_{EQU} \cong \frac{(2.465)(2000)}{1.3} = 3.79k \quad (12)$$

$$\frac{1}{R7} \cong \frac{1}{3.79} - \frac{1}{38.3};\ R7 \cong 4.206k \quad (13)$$

R7 is selected as 4.22k.

The LT1510 (U1) Package Selection

An 8-pin package can be used if only constant-current operation is required, but a 16-pin package must be used for constant-current and constant-voltage operation and for better heat dissipation. The four corner pins of the SO-16 package are fused (connected to the die internally) and it is recommended that these pins be soldered to the ground plane. With these pins soldered to expanded PC lands, the thermal resistance of the SO-16 package is 50°C/W. The thermal resistance of the DIP package is 75°C/W.

The plots in Figure 5 can be used for selecting an SO-8 or SO-16 package based on input voltage, output voltage and output current. These curves can be used to a maximum ambient temperature of 60°C. Refer to the data sheet for more accurate thermal calculations.

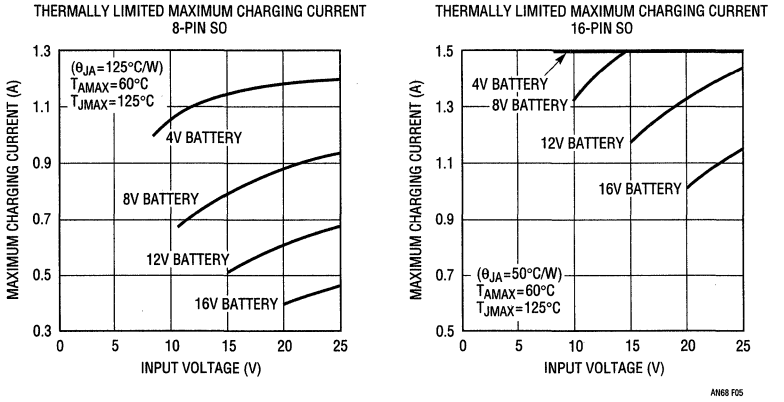


Figure 5. Comparing SO-8 and SO-16 Packages Thermal Limits

INTEGRATING THE LT1510 INTO A SYSTEM

When an LT1510 based charger is integrated into a system with a power adapter or power supply as a source, and a battery and a switching regulator as a load, some issues need to considered. The next paragraphs describe a few of them.

Minimum Operating Input Voltage

The minimum operating input voltage of an LT1510 based battery charger has to satisfy three LT1510 requirements: undervoltage lockout (V_{IN1}), minimum $V_{CC} - V_{BAT}$ voltage difference (V_{IN2}) and maximum duty cycle (V_{IN3}). See equations below. Other factors that affect the minimum operating input voltage are maximum output voltage, input diode forward voltage, resistance along the power path (including sense resistor, switch on resistance, trace resistance, solder joint resistance and connector resistance) coupled with maximum charge current.

The undervoltage lockout is 8V. The input-to-output voltage difference ($V_{CC} - V_{BAT}$) is 2V and is defined by two parameters: "maximum V_{BAT} with switch on" and "input common mode limit (high)," as found in the data sheet. The maximum duty cycle is 0.93. The following equations can be used for calculating the minimum input voltage V_{IN}.

$$V_{IN1} = 8 + V_{DIN}$$
$$V_{IN2} = 2 + V_{DIN} + V_{BAT} \quad (14)$$

$$V_{IN3} = V_{DIN} + \frac{V_{BAT} + (I_{CONST})(0.7)}{D} \quad (15)$$

where:

V_{IN} is the charger minimum input voltage. Use the highest of V_{IN1}, V_{IN2} or V_{IN3}.

V_{DIN} is the forward voltage of the input diode. The input diode can be replaced by a PMOSFET switch, in which case this term is removed.

I_{CONST} is the programmed charge current.

V_{BAT} is the maximum battery voltage.

D is the maximum duty cycle. D = 0.93.

To give the designer preliminary data about the typical lowest input voltage, the circuit in Figure 6 was tested. The constant current was adjusted with a trim pot connected to the PROG pin and the output voltage (V_{OUT}) was forced with the battery simulator board (see Appendix B). The results are shown in Figure 7.

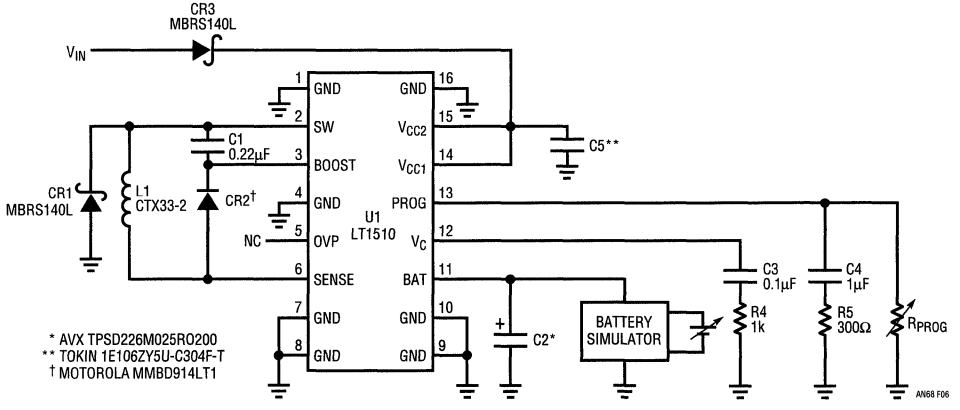


Figure 6. Minimum Operating Voltage Test

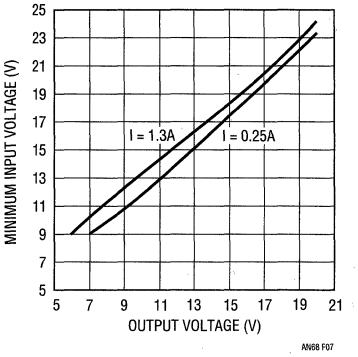


Figure 7, Typical Minimum Operating Voltage of an LT1510 Based Charger vs Output Voltage and Output Current

Efficiency

The circuit in Figure 6 was used to test efficiency. The plots in Figure 8 show the results for output voltage of 8V. Some power is dissipated in the input diode. See the data sheet for a circuit with a PMOSFET switch that bypasses the input diode when V_{IN} is on and saves power.

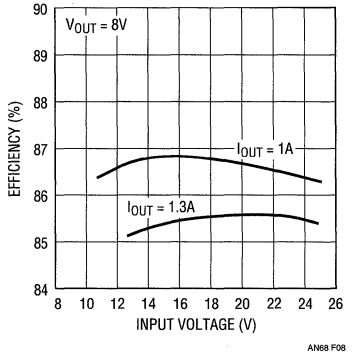


Figure 8. Efficiency vs Input Voltage and Output Voltage

Measuring Constant Voltage Without a Battery

At times, it may be necessary to measure the constant voltage of the charger with high accuracy and with the battery removed. Since the battery is an integral part of the regulation loop, some low frequency, low amplitude ripple may appear on the BAT pin and the DC voltage measurement at the BAT pin will not be accurate. It is recommended that a 2200µF capacitor be connected in place of the battery before making the measurement. (Be sure to observe capacitor polarity and to connect the capacitor when the charger is not running.)

Connecting the System Circuits to the BAT Pin or SENSE Pin

It is possible to connect the portable system circuitry directly to the battery (BAT pin), but two facts should be taken into consideration. First, the *total* current will be limited and so the system will "steal" battery charge current. In this case it is not possible to have a termination such as $-\Delta V$ that relies on constant charge current. Second, when the charger is active and the system is turned off, the full constant current will charge the battery, so the battery should be able to absorb it.

It is also possible to bypass the sense resistor and connect the system circuits to the SENSE pin, as shown in Figure 9. In this case the sum of the charging current and system current should not exceed the LT1510 maximum output current (limited by thermal considerations or switch peak current). However, since the system circuitry is capacitive in nature (input capacitor of a DC-to-DC converter), it should not be connected directly to the SENSE pin. This is because the internal sense resistor between the SENSE and BAT pins will have a large capacitance across it, which will cause instability. A 2.2µH inductor, such as the DT1608C-222 by Coilcraft, isolates the input capacitance of the system circuits well (L2 in Figure 9).

CR4 limits the transient current through the LT1510's internal sense resistor when the system is switched on in battery operation. Q1 is required if the series resistance of 0.2Ω between BAT pin and SENSE pin causes the efficiency to drop. The Si9433's on-resistance is 0.075Ω. The charge pump (C3/C4/CR5/CR6/R2) biases the gate of Q1. Q2 and R1 turn Q1 off when the system operates from the AC wall adaptor (V_{IN} active). R8 is required if there is no circuitry connected to V_{IN}.

Switching Between AC and Battery Operation, 2-Diode Configuration

Most systems that employ battery chargers also require glitch-free switching between AC operation and battery operation. Figure 10 shows a way to connect the load (switching regulator) to V_{IN} (when it is present) for AC

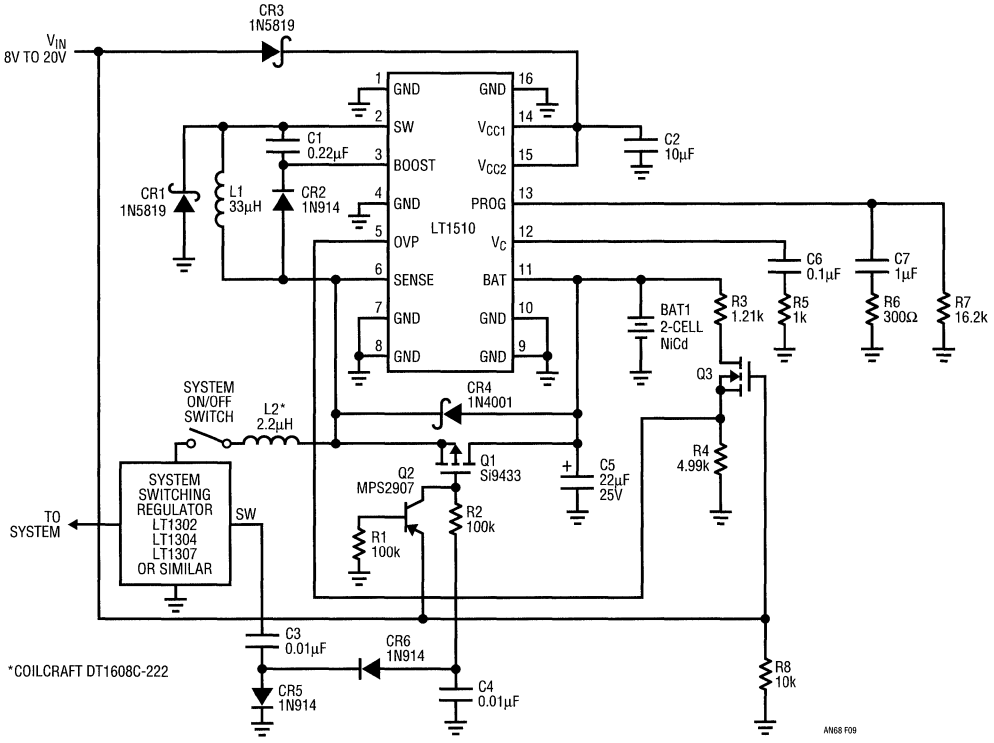


Figure 9. Connecting the System to SENSE Pin

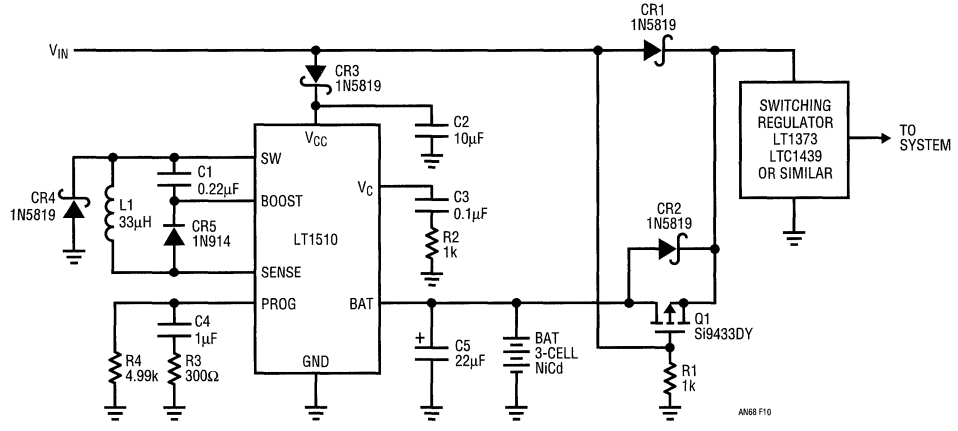


Figure 10. LT1510 Charger System, 2-Diode Configuration

operation or to the battery when V_{IN} is unavailable. When V_{IN} is active, CR1 conducts the load current, CR2 is reverse biased and Q1 is off. When V_{IN} is removed, Q1 conducts the load current from the battery. The voltage drop across Q1 is very low. Note that CR2 is in parallel with the body diode of Q1. The load has typically high input capacitance and also demands high current if the battery voltage is low. CR2 conducts at the transition to battery operation when Q1 is not fully on (the body diode has excessive forward voltage drop). R1 is required if there is no circuitry connected to V_{IN}. Low voltage drop across Q1 is essential for high efficiency when the system is operating from the battery. It was measured at 33mV with a load of 0.5A and the battery at 3V.

Switching Between AC and Battery Operation, Current Boost Configuration

Placing the system circuits in parallel with the battery achieves glitch-free switching between AC wall adaptor and battery operation. In AC operation, however, the system circuits "steal" charge current from the battery. This can be circumvented by boosting the output current by the same amount that is "stolen."

Figure 11 shows how the charge current can remain constant regardless of the load. The system circuits' current is sensed by R_S. Q1, U2, R1, R2 and R3 boost the LT1510's PROG pin current and thus the output current increases with the system circuits' current so that the current charging the battery remains unchanged. The LT1510 based charger should be designed for an output current that is the sum of currents into the battery and the load.

The Next Generation Battery Charger IC, the LT1511

The next generation constant-voltage/constant-current battery charger IC, the LT1511, performs like the LT1510, but has two additional features: input current limiting and peak switch current of 4A.

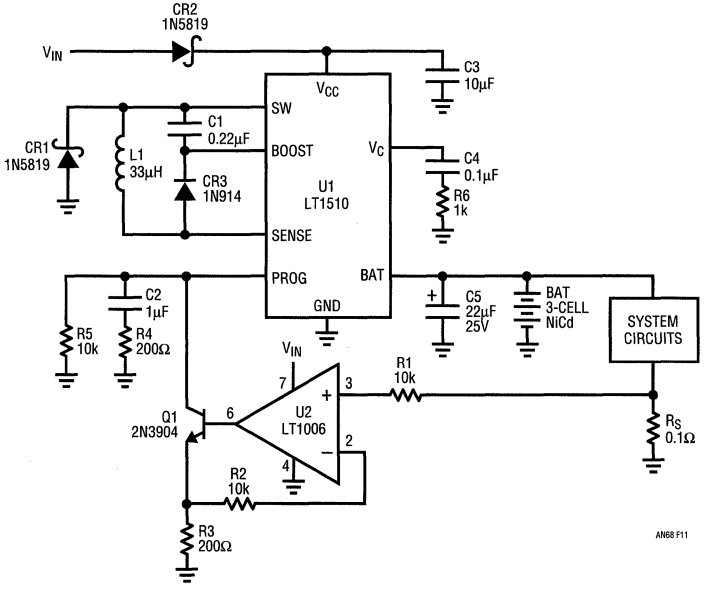


Figure 11. LT1510 Charger System, Current Boost Configuration

A control loop is provided to regulate the current drawn from the power adapter. This allows simultaneous operation of the portable system and battery charging without overloading the adapter. When system current increases, the charging current is reduced to keep the adapter current within the specified level.

The internal switch of the LT1511 is capable of delivering 3A DC current (4A peak current) for charging the battery. This is a 100% increase over the LT1510.

CHARGING BATTERIES/TERMINATION METHODS

Any portable equipment that requires fast charge needs to have proper charge termination. Commonly, the LT1510 is used in conjunction with a microcontroller that has an internal analog-to-digital converter (ADC) or in conjunction with a microprocessor and an ADC IC.

Sometimes, however, a microcontroller is not available or is not suitable for fast charge termination. The following paragraphs describe solutions for both cases.

Charging NiCd Batteries

dT/dt Termination: A safe and reliable way to terminate fast charging of NiCd and NiMH batteries is based on detecting the rate at which the battery temperature increases during constant-current charging. With constant-current charging, the battery temperature increases rapidly as the battery nears full charge status (see Figure 12).

The circuit in Figure 13 monitors the battery temperature with a negative temperature coefficient (NTC) thermistor R_T and detects the rate at which the temperature rises over a 20-second period.

The thermistor output is amplified by differentiator U1A and integrator U1B (which, together, form an AC coupled amplifier). The differentiator is AC coupled and thus eliminates the DC voltage of the R_T and R1 network; the integrator is reset every twenty seconds by the timer U2 and transistor Q1. The output of the integrator is monitored by U1C, a comparator and latch. When U1B's output voltage exceeds a threshold, the output of U1C is latched high and turns Q2 on, pulling the LT1510 V_C pin to ground and shutting the charger off.

The bias voltage (V_{BIAS}) for the circuit is generated by voltage divider (R13/R14) and buffer U1D. The V_{BIAS} level chosen is close to the thermistor network (R_T/R1) output voltage in order to minimize the turn-on time needed for charging C1. This also minimizes the effect of C1's leakage. C1 is a ceramic capacitor.

R2 allows C1 to stabilize rapidly upon turn-on. R2, R3, R6 and R7 supply bias current to U1A and U1B.

The design equations for the dT/dt termination circuit are presented in the following box.

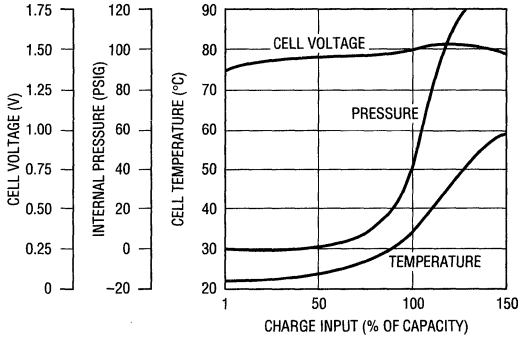


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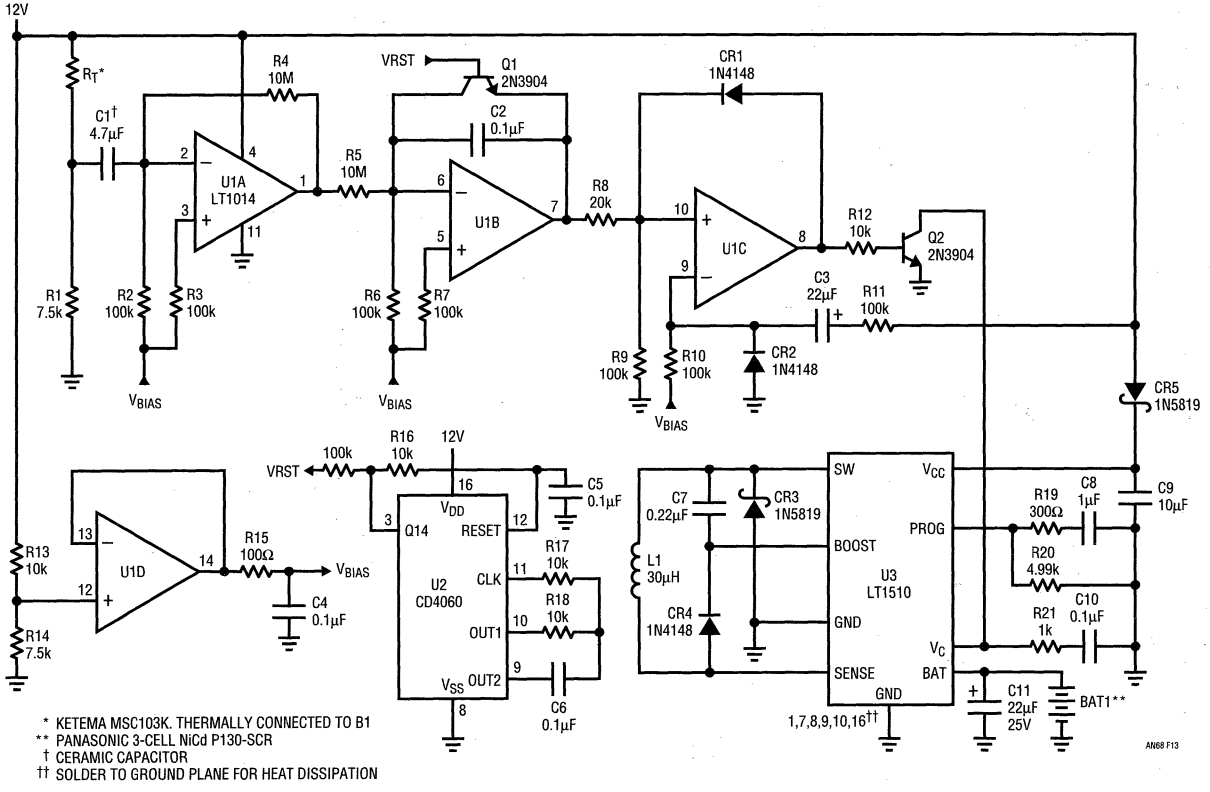
Figure 12. Voltage, Pressure and Temperature During 1C Charge of NiCd Battery



* KETEMA MSC103K. THERMALLY CONNECTED TO B1
** PANASONIC 3-CELL NiCd P130-SCR
† CERAMIC CAPACITOR
†† SOLDER TO GROUND PLANE FOR HEAT DISSIPATION

Figure 13. LT1510 NiCd Charger with dT/dt Termination

Design Equations for dT/dt Termination

Thermistor Design

$$(1)\quad \beta = \left(T\frac{T_0}{T_0 - T}\right)\left(\ln\frac{R_T}{R_{T0}}\right) \tag{16}$$

$$(2)\quad R1 = \frac{R_{T0}\left(\beta - 2T_0\right)}{\beta + 2T_0} \tag{17}$$

$$(3)\quad \frac{dV_{DIV}}{dT} = V_{DIVT0}\left(\frac{-\beta}{2T_0^2} + \frac{1}{T_0}\right) \tag{18}$$

where:
β is a constant depending on the thermistor material,
T is temperature in °K at which R_T is characterized,
T_0 is temperature in °K at which R_{T0} is characterized,
dV_{DIV}/dT is the rate of divider output voltage change vs temperature and V_{DIVT0} is the divider DC voltage at T_0

Integrator U1A and Differentiator U1B Gain

$$(4)\quad G = (R4)(s)(C1)\frac{1}{(R5)(s)(C2)}$$

$$\text{for } R4 = R5,\quad G = \frac{C1}{C2} \tag{19}$$

Threshold of the Latch U1C Stage

$$(5)\quad V_{TH} = \left(\frac{dT}{dt}\right)(t)\frac{(dV_{DIV})}{(dT)}(G) \tag{20}$$

where:
dT/dt is the selected slope
t is the timer period

R8 and R9 Selection

$$(6)\quad \frac{V_{TH}}{R8} = \frac{V_{BIAS}}{R9} \text{ or:}$$

$$R8 \cong (V_{TH})\left(\frac{R9}{V_{BIAS}}\right) \tag{21}$$

where:

$$(7)\quad V_{BIAS} = \frac{(V_{IN})(R14)}{R13 + R14} \tag{22}$$

For the design shown in Figure 13:
R_T is a Ketema MSC103k, a 10k thermistor with R_{25}/R_{125} = 29.25.

$$(1)\quad \beta = \left(398\frac{298}{398 - 298}\right)(\ln 29.25) = 4004 \tag{23}$$

$$(2)\quad R1 \cong \frac{10k\left[4004 - 2(298)\right]}{4004 + 2(298)} = 7.41k \tag{24}$$

R1 is selected as 7.5k.

The gain of the R_T, R1 network is:

$$(3)\quad \frac{dV_{DIV}}{dT} = 12\left[\frac{10}{10 + 7.5}\right]\left[\frac{-4004}{2(298^2)} + \frac{1}{298}\right] = -0.132V/°C \tag{25}$$

For C1 = 4.7µF and C2 = 0.1µF, the gain of the integrator and differentiator can be written as:

$$(4)\quad G = \frac{4.7\mu F}{0.1\mu F} = 47 \tag{26}$$

The selected slope that will trigger termination is 0.5°C/min. (a conservative half of the typical 1°C/minute). The selected timer period is 20 seconds (0.33 minute).

(5) V_{TH} = (0.5)(0.33)(0.132)(47) = 1.023V

V_{IN} is selected as 12V, R13 = R_T = 10k, R14 = R1 = 7.5k

$$(7)\quad V_{BIAS} = \frac{12(7.5)}{10 + 7.5} = 5.14V \tag{27}$$

R9 is selected as 100k.

$$(6)\quad R8 \cong 1.02\frac{100}{5.14} = 19.9k \tag{28}$$

R8 is selected as 20k.

A secondary termination for the charger is recommended. Depending on system reliability requirements, the secondary termination circuit may use existing components such as R_T or U1 for absolute temperature or time-out,

respectively. Also, to avoid premature termination, the temperature rise rate that results from bringing the system indoors from the lowest outdoor temperature should be considered.

–ΔV Termination: The internal battery temperature rise towards the end of charge, coupled with the negative temperature coefficient of NiCd and NiMH, causes the battery voltage to drop. The drop can be detected and used for terminating a fast charge with the LT1510.

In the example shown, Figure 14, the charge current was selected as 0.8A. To determine the voltage droop rate for –ΔV termination, a fully charged 3-cell (Panasonic P140-SCR) NiCd battery was connected to an LT1510 charger circuit programmed for a 0.8A rate. The negative slope in voltage, as seen in Figure 14, is calculated to be –0.6mV/s. It can be seen that the total voltage drop is about 300mV (100mV per cell). After the battery voltage dropped 300mV from the peak of 4.93V (100mV per cell), the charger was disabled.

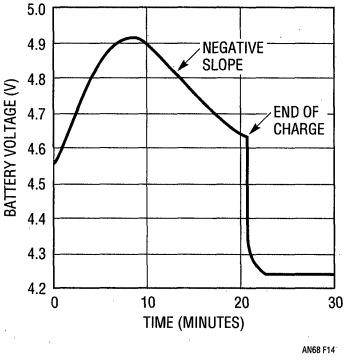


Figure 14. –ΔV Test

At the heart of the circuit in Figure 15 is U3, a sample-and-hold IC, LF398. The output of U3, Pin 5, samples the input level, Pin 3, at every clock pulse at Pin 8. When the battery voltage drops, the input to U3 also drops. If the update step at the output of U3 is sufficiently negative, U2B latches in the high state and Q1 turns on and terminates the charge by pulling V_C pin of the LT1510 down and disabling it.

U2A and the associated passive components smooth, amplify and level shift the battery voltage. The timer U4 updates the hold capacitor C8 every fifteen seconds. The timer signal stays high for 7ms, sufficient for the hold capacitor to be charged to the input level. U2B and the associated parts form a latch that requires a momentary negative voltage at Pin 6 to change state. R15 supplies the negative feedback and Q2, R16, R17 and C10 reset the latch on turn-on.

U3's output voltage droops at a rate proportional to the hold capacitor's internal leakage and the leakage current at Pin 6 (10pA typical).This droop is very low and does not affect the operation of the circuit.

The minimum negative battery voltage slope required to trigger termination can be calculated from:

$$-\frac{dV}{dT}=\frac{V_{TRIG}}{(t_{CLK})(G_{U2A})} \quad (29)$$

where:

$$V_{TRIG}=\frac{(V_{REF})(R12)}{R11+R12}=5\frac{1}{101}=49.5mV, \quad (30)$$

t_{CLK} is the clock period, 15 seconds,

$$G_{U2A} \text{ is the gain of the first stage } =\frac{R8}{R4\,||\,R5}=11 \quad (31)$$

hence:

$$\frac{-dV}{dT}=\frac{49.5mV}{(15)(11)}=0.3mV/s \quad (32)$$

Charging Sealed-Lead-Acid (SLA) Batteries

Standard Charge: The LT1510 is ideal for standard charging of SLA batteries because of its constant-current and constant-voltage features. To extend the battery life, the float voltage can be temperature matched to the battery specifications. The circuit in Figure 16 was designed for the Panasonic SLC-214P, which is a 2-cell, 2.1AH SLA battery with a maximum charge current of 0.8 amps.

The thermistor R_T, selected for temperature matching, is a Ketema MSC103K. Figure 17 shows minimum and maximum float voltage vs. temperature, as recommended by the manufacturer. The output voltage of the charger vs. temperature fits in this range.

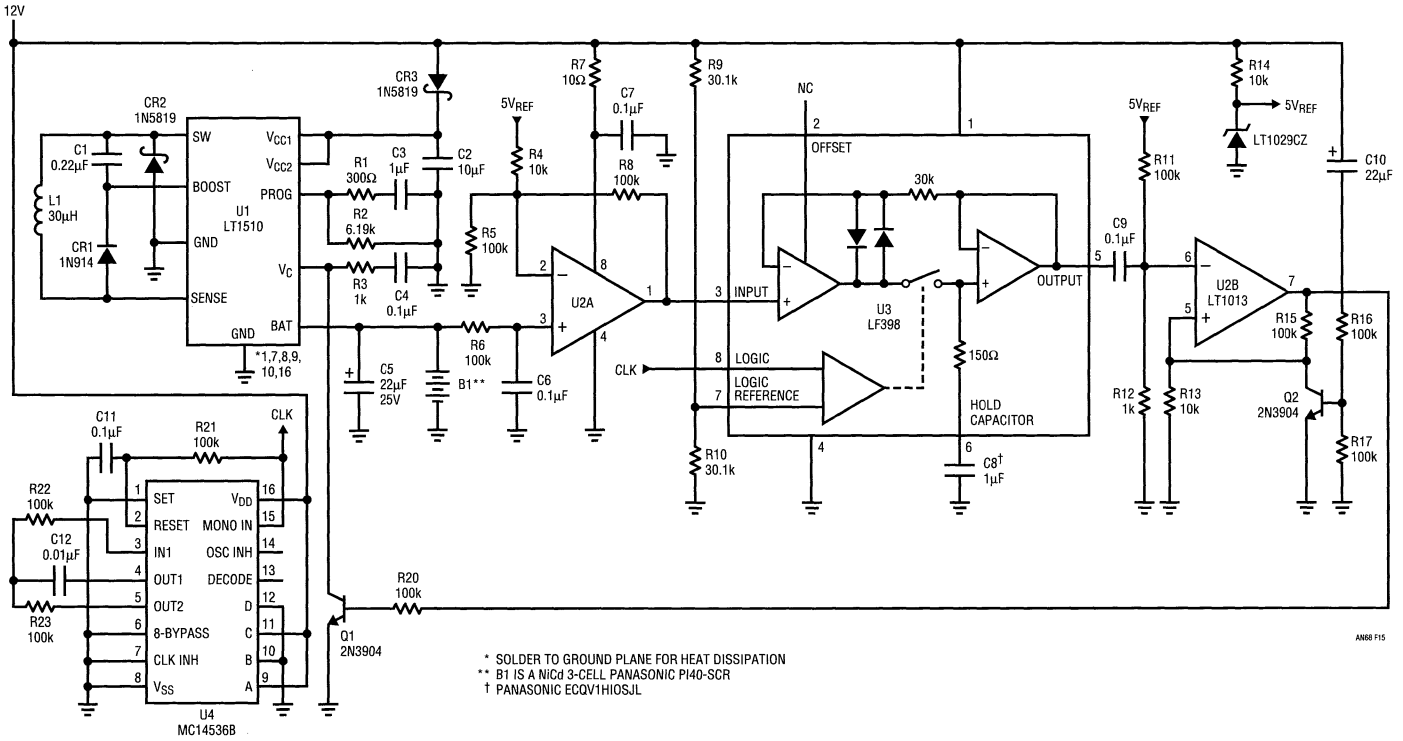


Figure 15. LT1510 NiCd Charger with –ΔV Termination

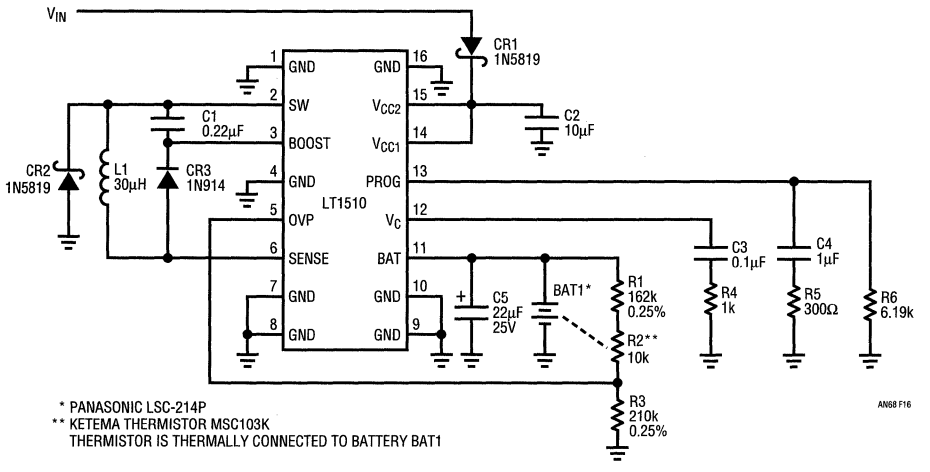


Figure 16. Temperature Compensated Standard Sealed-Lead-Acid Battery Charger

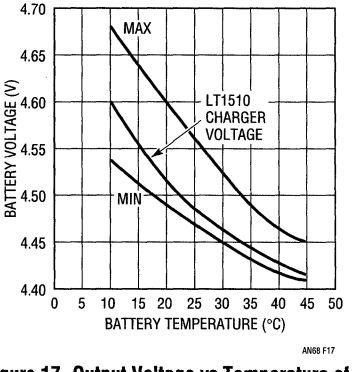


Figure 17. Output Voltage vs Temperature of SLA Charger and MIN/MAX Float Voltage vs Temperature (as Recommended by Panasonic)

Fast Charge: The circuit in Figure 18 is a fast SLA battery charger. It is based on the standard SLA battery charger circuit in Figure 16. When the charge current is high, the constant-voltage level increases from 4.5V to 5V. At a constant voltage of 5V, the battery reaches a full charge state faster than at a constant voltage of 4.5V.

R9's value programs the constant current of the LT1510 to 0.8A. R1, R2 and R3 program the constant voltage to 4.5V. U2, an open-collector voltage comparator, is at low state when the voltage across the internal LT1510 sense resistor is higher than the voltage across R7 or equivalent to the charge current being above 0.4A. As long as U1's output is low, the charging voltage is boosted to 5V by changing the OVP voltage divider ratio by switching R4 in parallel with R3.

Charging Li-Ion Batteries

Li-Ion batteries are charged with a constant-voltage/constant-current charger. Constant current is supplied until the output voltage reaches 4.1V or 4.2V per cell (depending on the manufacturer) followed by constant-voltage charging with required accuracy of ±50mV per cell. The charging current then tapers down naturally.

I_{MIN} + Timer Termination: To maximize battery cycle life, several lithium-ion battery manufacturers recommend termination of constant-voltage float mode 30 to 90 minutes after charge current has dropped below a specified threshold level, I_{MIN}. The float voltage is 4.1V or 4.2V per cell and the charge current threshold level is typically 50mA to 100mA. Check with the battery manufacturer for details.

Figure 19 shows a constant-current, constant-voltage charger with I_{MIN} + 30-minute termination. When the LT1510 is charging, U2 compares the voltage across the LT1510 internal 0.2Ω sense resistor to the voltage across

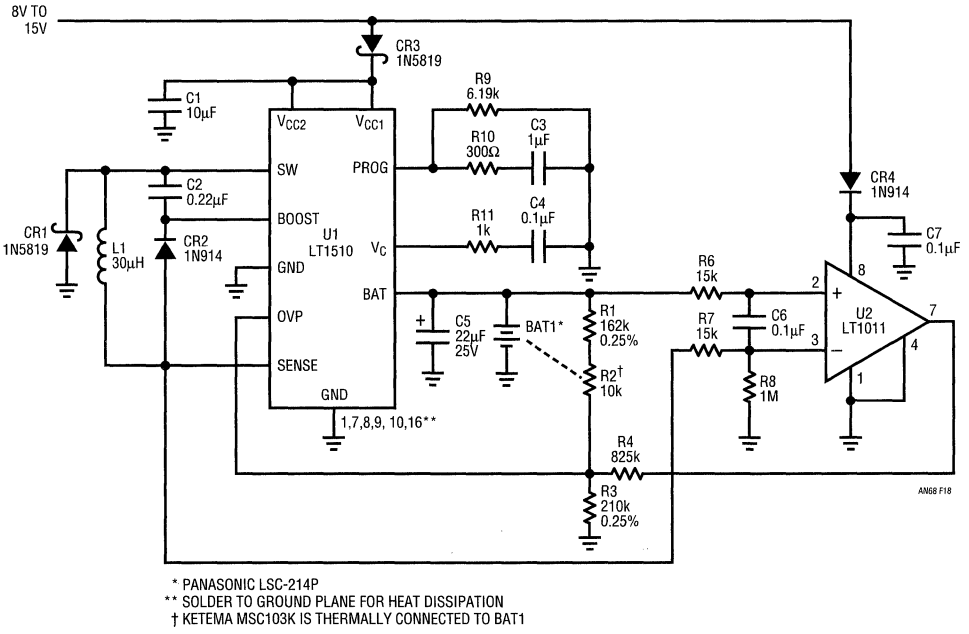


Figure 18. Fast, Temperature Compensated SLA Charger

R7. When the voltage across the sense resistor is lower than the voltage across R7 (or, alternatively, when the charge current drops below 75mA), U2's output voltage drops. When U2's output voltage drops, U2 latches at low state via CR5. U2's output is connected to the RESET pin of U3; when switched, this signal releases the reset (active high) of U3. U3, a timer, starts clocking and 30 minutes later its DECODE output (Pin 13) changes to a high state. The DECODE output is connected to the SET input of U3 (active high). This signal latches U3's DECODE pin high. The high at the DECODE pin also terminates the charge by pulling the LT1510's V_C pin down via Q2.

Q3, R14, C8, R15 and CR6 reset U2 and U3 on turn-on.

A secondary termination can be based on total charge time.

Terminating with a Microprocessor

The LT1510 gives the designer an easy solution for the power section of a battery charger and also a smooth transition from constant-current to constant-voltage operation. When a sophisticated charging regimen is required, connecting a dedicated or system microprocessor to the charger is the solution of choice.

NiCd or NiMH Charger: The charger in Figure 20 has two charge rates that depend on the HI_CHARGE signal and are programmed by R1 and R7 (see the Component Selection section). The microprocessor reads the battery voltage by clocking U2, a serial data ADC. C7 smoothes the ADC input, but averaging a number of ADC readings is recommended. The voltage divider R4/R5/R6 divides the voltage at the BAT pin for both the ADC and the OVP pin. The LT1510 is programmed to 5V in constant-voltage mode. The microprocessor can terminate charge based on $-\Delta V$, zero ΔV or dV/dt. After termination, the low charge can serve as trickle for NiCd type batteries; the charger may have to shut down for NiMH cells. Check the battery manufacturer's specifications.

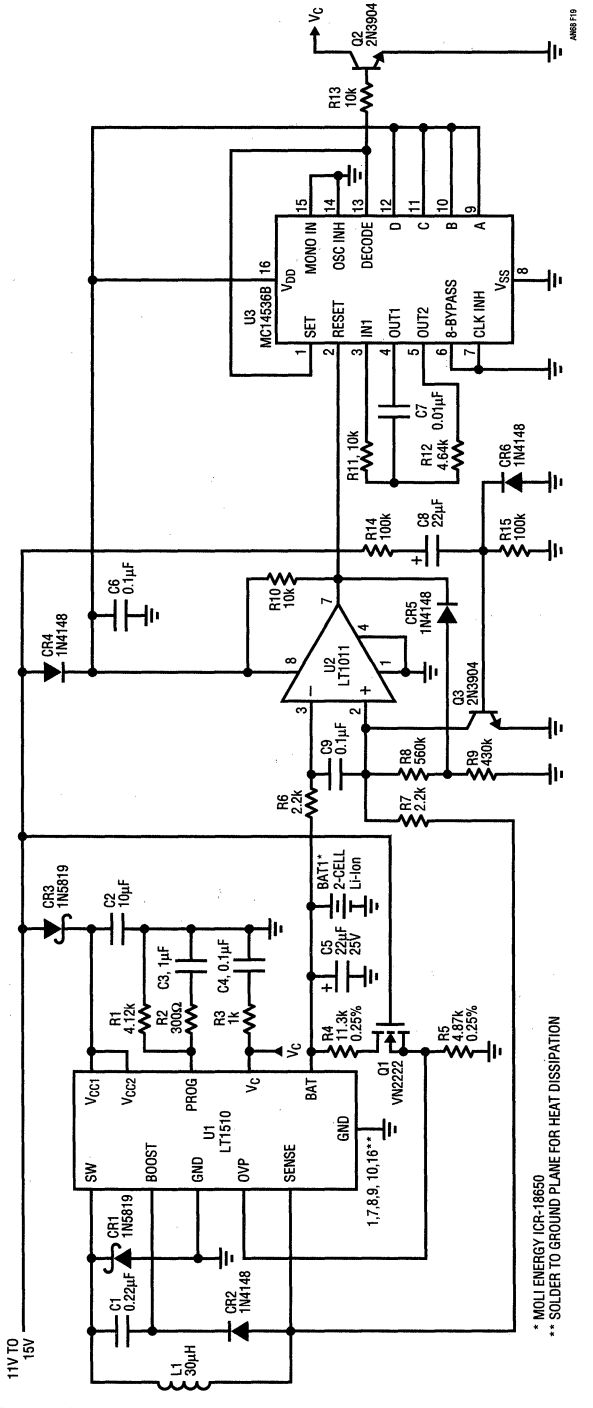


Figure 19. Li-Ion I_{MIN} + Timer Charger

Controlling the LT1510 Charger with a Microprocessor

PWM Charge Current Control: Figure 21 shows how to control the charge current with the PWM output of the microcontroller. The constant-current charge can be calculated from:

$$I_{CONST} = \frac{(2.465)(2000)(D)}{R_{PROG} + 300\Omega} \quad (33)$$

Where R_{PROG} is the value of the programming resistor and D is the duty cycle of the PWM signal. The maximum value of D is 1. D can be calculated from:

$$D = \frac{(N)_{10}}{2^8} \quad (34)$$

Where $(N)_{10}$ is the decimal value of the data entered into the PWM register of the microprocessor and 2^8 is the maximum decimal value of an 8-bit register representing D = 1.

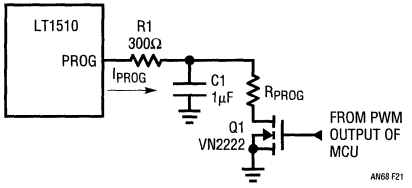


Figure 21. PWM Charge Current Control

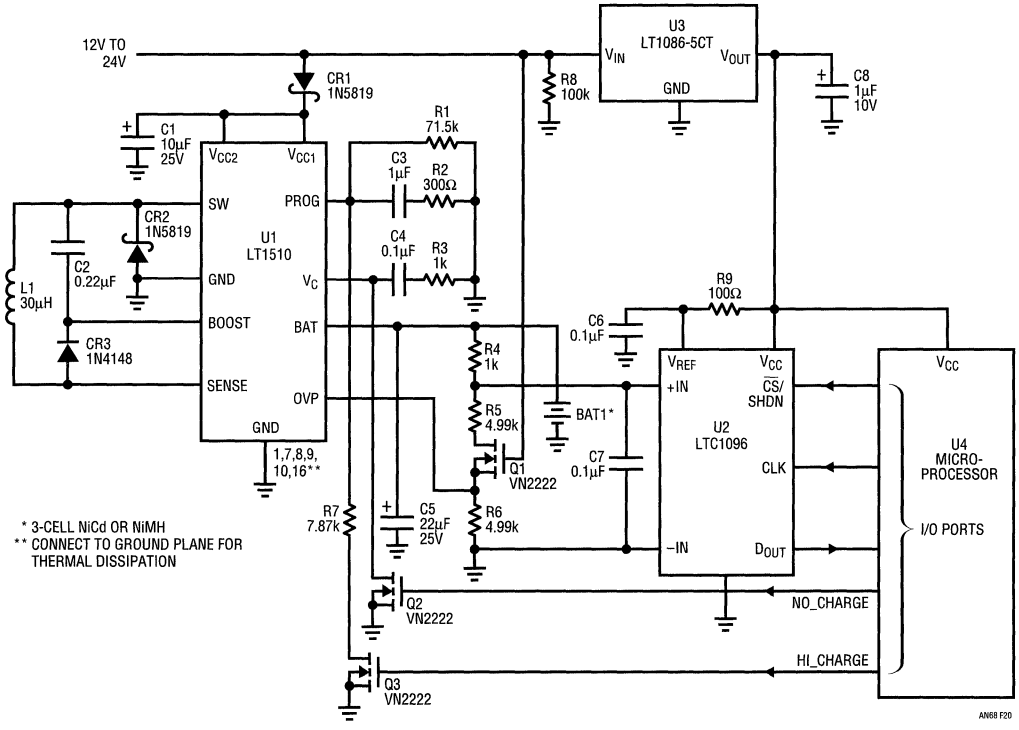


Figure 20. NiCd or NiMH Microprocessor Controlled Charger

Parallel and Serial Control: There are many ways to control the constant current and constant voltage of the charger. Some of them are described here.

In the circuit in Figure 22, U2, U3 and Q1 form a microprocessor-controlled current sink. The data on the microprocessor parallel bus controls the voltage at the OUT1 pin of U2. U3 regulates the voltage across R2 to equal that at the OUT1 pin of U2. The current through R2 flows out of the PROG pin of the LT1510 and thus the charge current is controlled by the microprocessor.

In the circuit in Figure 23, U2, U3 and Q1 form a microprocessor-controlled current sink. The data on the microprocessor serial bus controls the voltage at the OUT1 pin of U2. U3 regulates the voltage across R2 to equal that at the OUT1 pin of U2. The current through R2 flows out of the PROG pin of the LT1510 and thus the charge current is controlled by the microprocessor.

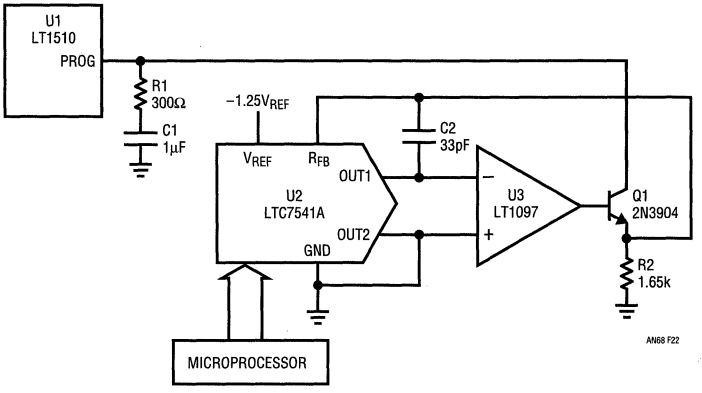


Figure 22. 12-Bit, Parallel Loading Microprocessor Charge Current Control

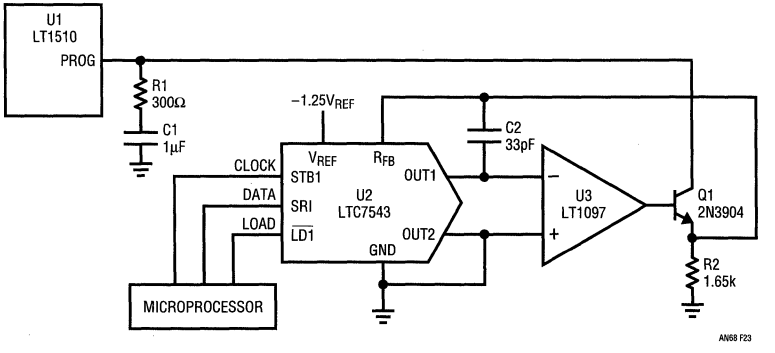


Figure 23. 12-Bit Serial Interface Microprocessor Charge Current Control

Figure 24 shows a circuit to control the constant-voltage output of an LT1510-based battery charger. U2, R1, and R2 invert the polarity of the battery voltage. U3 and U4 act as a voltage divider and also change the polarity of the voltage back to positive. The divided voltage is fed to the OVP pin of the LT1510.

U3 can be LTC7541A for parallel data interface with the microprocessor or LTC7543 for serial data interface with the microprocessor. The programmed voltage V_{CONST} can be calculated from the following:

$$V_{CONST} = 2.465\frac{2^{12}}{(N)_{10}} \quad (35)$$

where $(N)_{10}$ is the decimal value of the microprocessor bus data and 2^{12} is the maximum data value based on 12-bit data.

CONCLUSION

The LT1510 is a high efficiency charger building block that relieves the designer of the burdens of switcher design, heat sinking, and even power-transistor and sense resistor selection. In some cases, the LT1510 and a few passive parts are all that is necessary to build a high efficiency battery charger. Its high accuracy constant-voltage and constant-current features make the LT1510 an excellent choice for Li-Ion, NiCd, NiMH and SLA charging. Its control over all charging parameters makes the LT1510 an easy device with which to design.

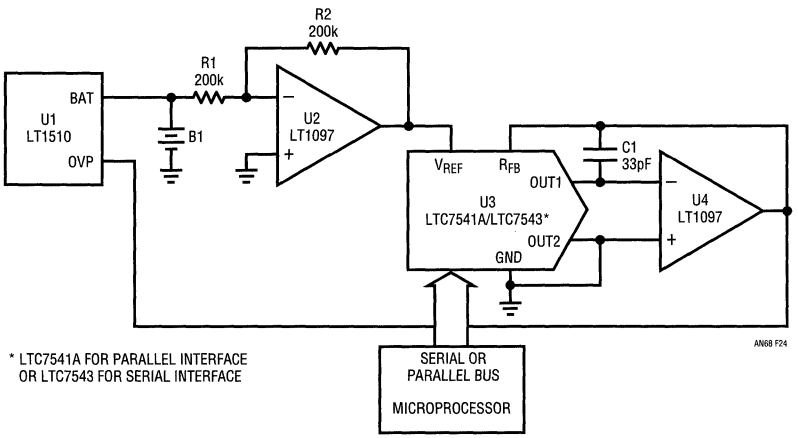


Figure 24. Microprocessor Voltage Control

APPENDIX A: TEST RESULTS

Testing a statistically significant number of batteries and charge/discharge cycles is essential for validating a charger design. The circuits in the body of this document were tested and the results are presented in this appendix.

Output Current Boost Configuration Test

The purpose of this test is to see how stable the charge current is with a dynamic load. The 0.5A charger circuit in Figure 11 was connected to the constant-current load (Figure B2), which was adjusted to 0.5A and connected to a function generator as shown in Figure A1. The function generator switched the load between 0A and 0.5A at 100Hz with a 50% duty cycle. The battery charge current was monitored with an oscilloscope across a 0.1Ω sense resistor connected in series with the battery.

The test results are shown in Figure A2. The battery charge current is affected by the dynamic load only at the transition times; otherwise it is regulated at 0.5A. The LT1510 control loop corrects the charge current at a rate of 0.5A per 1ms. If the load changes at a slower rate, it will not affect the charge current.

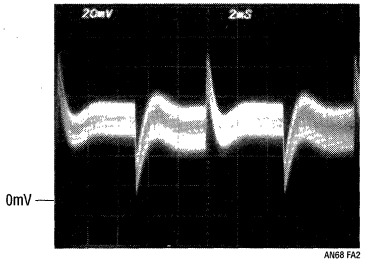


Figure A2. Battery Charge Current of Current Boost System with Dynamic Load

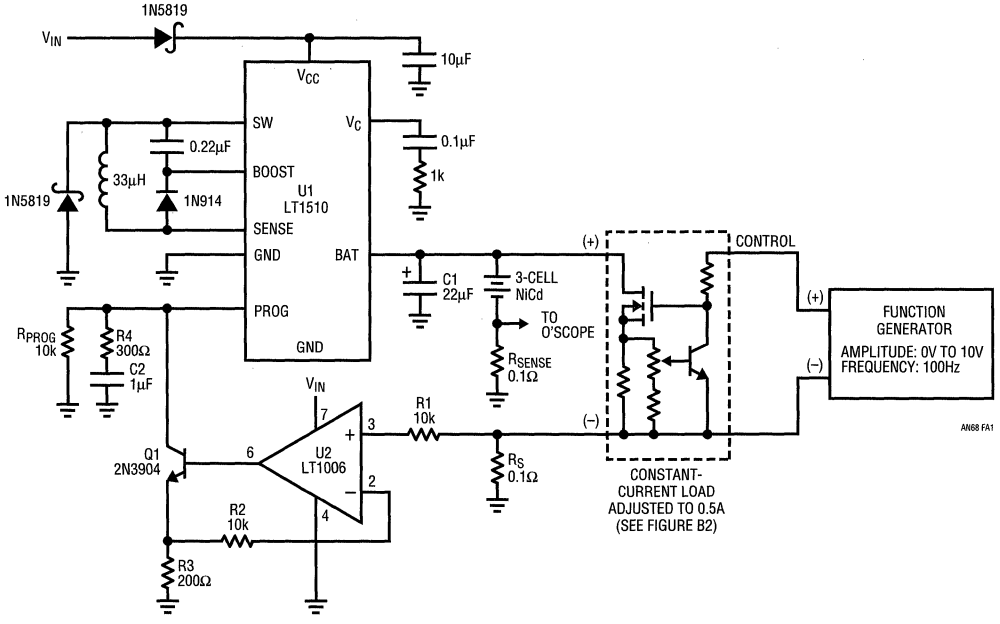


Figure A1. Battery Charging Current System Test Circuit

dT/dt Termination Test

The purpose of this test is to establish that the charger circuit in Figure A3 is reliable and terminates consistently. The circuit was connected to a test system that discharged the battery to the same level after termination and reactivated the charger circuit. Data from nineteen charge/discharge cycles was collected. The test conditions are given in Table A1.

Table A1

Battery	3 NiCd Cells of Panasonic P130-SCR in Series (1.3AH)
Constant Charge Current	1 A
Discharge Current	1 A
Minimum dT/dt Slope That Will Trigger Termination	0.5°C/minute
Required Duration of the Above Slope to Trigger Termination	20 seconds

The test results are presented below. Figure A4 shows a typical battery voltage during one charge/discharge cycle. The data collected was analyzed and presented in Table A2.

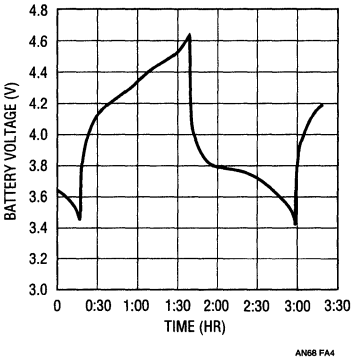


Figure A4. Typical Battery Voltage at Charge/Discharge Cycle of NiCd Charger with dT/dt Termination

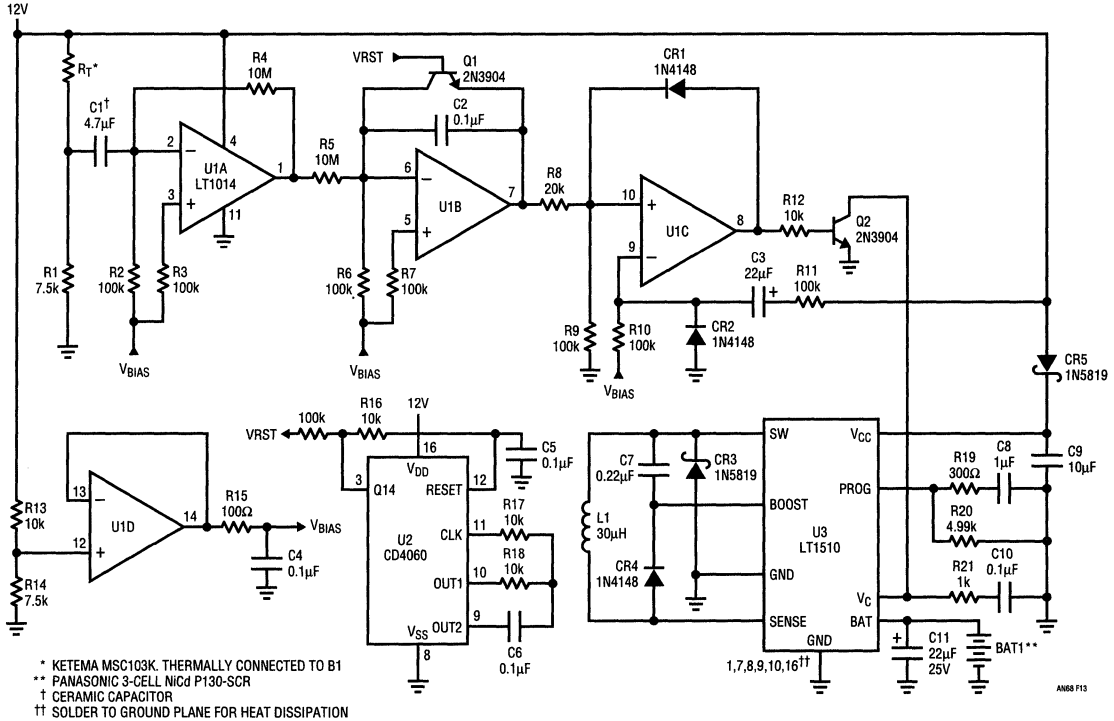


Figure A3. LT1510 NiCd Charger with dT/dt Termination

Table A2

Average Charge Time	1:20:22 hours
Standard Deviation of Charge Time	0:01:00 hours (1 minute)
Average Discharge Time	1:19:25 hours
Standard Deviation of Discharge Time	0:00:58 hours (58 seconds)

The consistent discharge time (58 seconds standard deviation with constant-current load) proves that the charge termination is repeatable and that the LT1510 charger performs well. Also, because there is no "top-off" or trickle charge, the charge efficiency (discharge ampere-hours over charge ampere-hours) is close to 100%.

NiCd –ΔV Termination Test

The purpose of this test is to establish that the charger circuit in Figure A5 is reliable and terminates consistently. The circuit was connected to a test system that discharged the battery to the same level after termination and reactivated the charger circuit. Data from 68 charge/discharge cycles was collected. Test conditions are given in Table A3.

Table A3

Battery	3 NiCd Cells of Panasonic P140-SCR in Series (1.4AH)
Constant Charge Current	0.8A
Discharge Current	0.8A
–ΔV That Will Trigger Termination	4.5mV
End of Discharge Voltage	2.7V

The test results are presented below. Figure A6 shows typical battery voltage during charge/discharge cycle. The data collected was analyzed and presented in Table A4.

Table A4

Average Charge Time	2:00:55 hours
Standard Deviation of Charge Time	0:05:37 hours
Average Discharge Time	1:59:14 hours
Standard Deviation of Discharge Time	0:00:48 hours (48 seconds)

The consistent discharge time (48 seconds standard deviation with constant-current load) proves that the charge termination is repeatable and that the LT1510 charger performs well. Also, because there is no "top-off" or trickle charge, the charge efficiency (discharge ampere-hours over charge ampere-hours) is close to 100%.

SLA Fast Charge Test

The purpose of this test is to establish that the SLA fast charge circuit in Figure A7 is reliable and terminates consistently. The circuit was connected to a test system that, after about four hours of charging, discharged the battery to the same level every cycle and then reactivated the charger circuit. Data from seventeen charge/discharge cycles was collected. Test conditions are presented in Table A5.

Table A5

Battery	2-Cell SLA Panasonic LSC-214P
Constant Charging Voltage	4.5V
Boosted Constant Charging Voltage (Until Charge Current Drops Below 0.4A)	5V
Constant Charge Current	0.8A
Average Charge Time	3:53 hours
Standard Deviation of Charge Time	0:04:15 hours
Discharge Current	1A
End of Discharge Voltage	3.6V

The test results are presented below. Figure A8 shows typical current during the charge and discharge (positive and negative, respectively) of one cycle. The data collected was analyzed and is presented in Table A6.

Table A6

Average Discharge Time	1:31:39 hours
Standard Deviation of Discharge Time	0:02:06 hours

The consistent discharge time (standard deviation is 2 minutes) proves that the charger and regimen are reliable. Charge current of 0.8A and charge level of 1.5AH (discharge time of 1.5 hours at 1A) are conservative for a 2.1AH battery. To reach full charge at the required four hours, a higher charge current battery can be used, or a current threshold lower than 0.4A can be programmed.

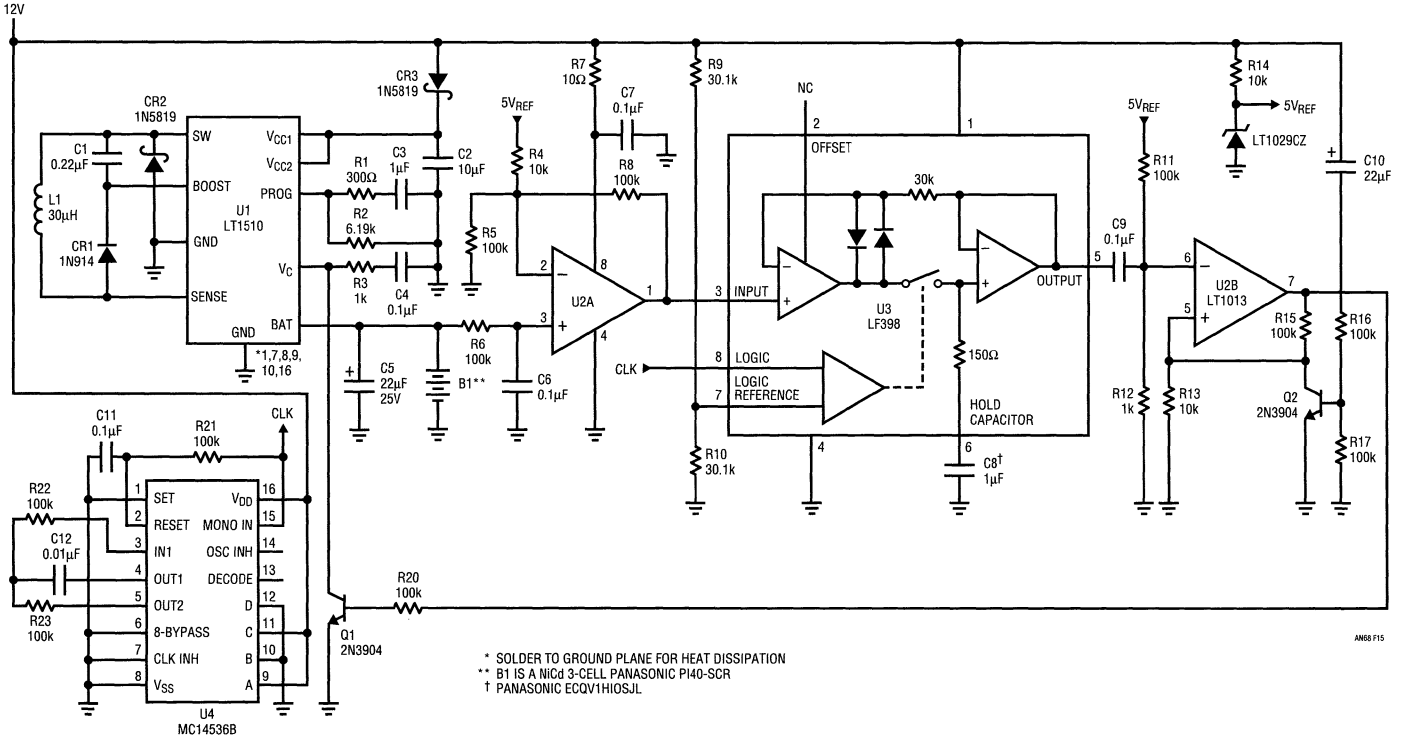


Figure A5. LT1510 NiCd Charger with –ΔV Termination

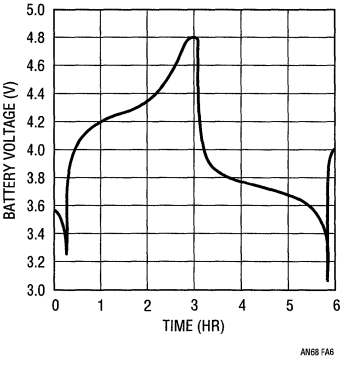


Figure A6. Typical Battery Voltage During Charge/Discharge Cycle of NiCd Charger with –ΔT Termination

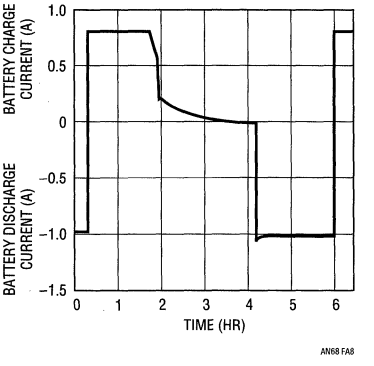
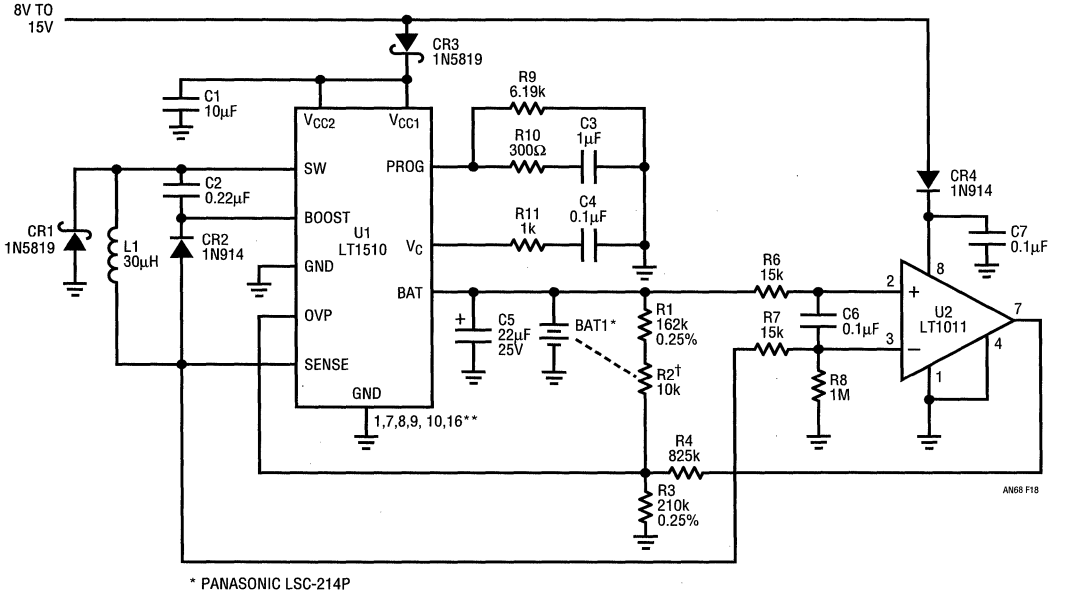


Figure A8. Typical Battery Current at Charge/Discharge Cycle of SLA Fast Charger



* PANASONIC LSC-214P
** SOLDER TO GROUND PLANE FOR HEAT DISSIPATION
† KETEMA MSC103K IS THERMALLY CONNECTED TO BAT1

Figure A7. Fast, Temperature Compensated SLA Charger

Li-Ion with Time-Out Termination Test

The purpose of this test is to establish that the charger circuit in Figure A9 is reliable and terminates consistently. The circuit was connected to a test system that, after termination, discharged the battery to the same level and reactivated the charger circuit. Data from thirty-two charge/discharge cycles was collected. Other test conditions are given in Table A7.

Table A7

Battery	2 Li-Ion Cells of Moli Energy ICR18650 in Series
Constant Voltage	8.2V
Constant Charge Current	1.3A
Discharge Current	1A
Charge Current That Will Trigger Timer	<100mA
Timer Duration	30 minutes

The test results are presented below. Figure A10 shows a typical charge/discharge battery voltage. The test data is analyzed and given in Table A8.

Table A8

Average Charge Time	2:14:12 hours
Standard Deviation of Charge Time	0:01:00 hours
Average Discharge Time	1:11:33 hours
Standard Deviation of Discharge Time	0:00:40 hours

The consistent discharge time (40 seconds standard deviation with 1A constant-current load) proves that the charge termination is reliable and that the LT1510 is a good solution for Li-Ion charging.

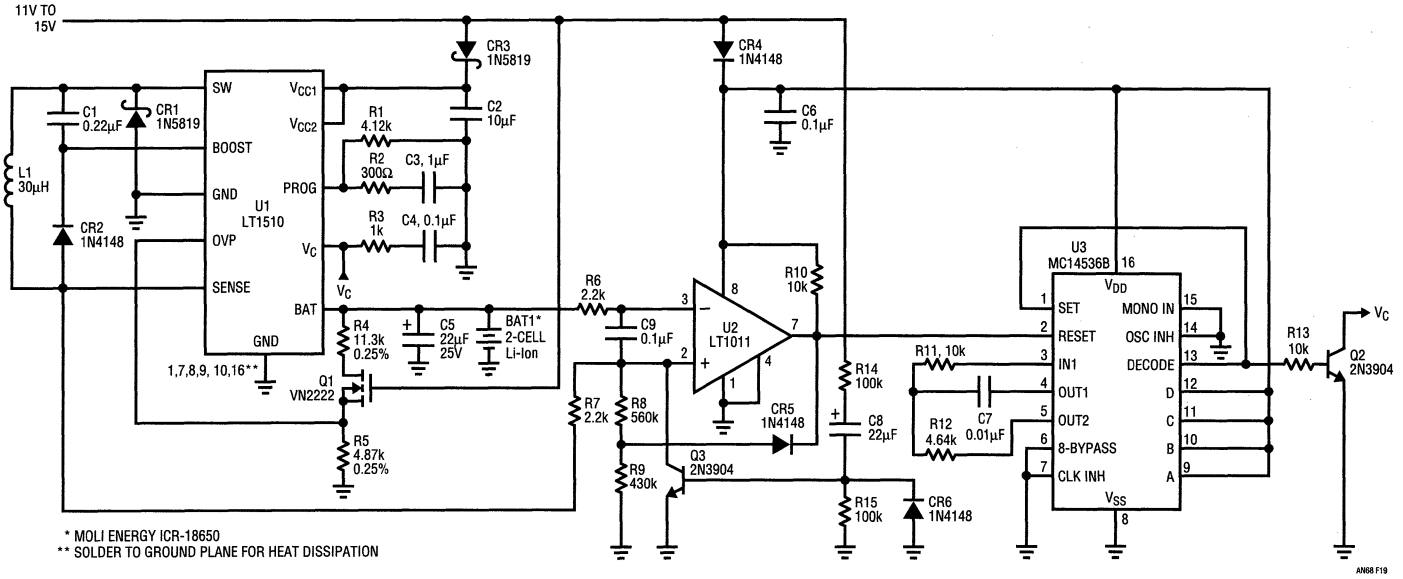


Figure A9. Li-Ion Charger with Time-Out Termination

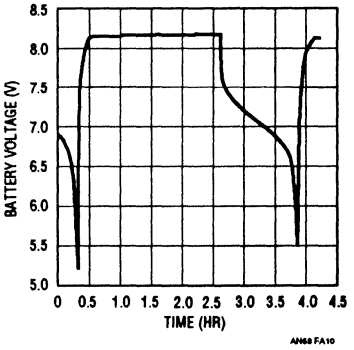


Figure A10. Typical Li-Ion Battery Voltage at Charge/Discharge with Time-Out Termination

APPENDIX B: AUXILIARY CIRCUITS FOR TESTING BATTERIES AND CHARGERS

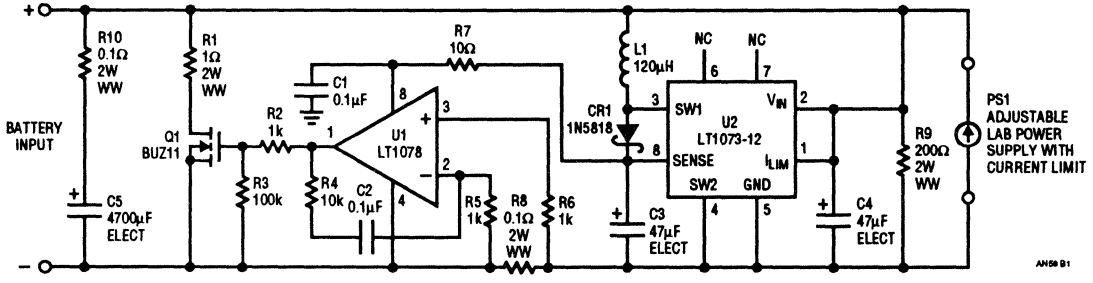
While working on battery charger design and testing, two "home-brewed" circuits were frequently used: a battery simulator and a controlled constant-current load. The former was used for checking the operation of the charger and the latter for charge/discharge tests. A variety of timers, charge/discharge controllers and the like were constructed as the need arose.

The Battery Simulator

There are two advantages to using the battery simulator (Figure B1) over a battery in board tests. In case of an accidental short, the power supply has current limiting, whereas a shorted battery can conduct more than 20 amperes and vaporize everything, including traces. Also, the simulator voltage is static and controllable, which makes it easy for testing (efficiency, for instance).

The user has to adjust the power supply to the desired voltage and connect the positive and negative "battery input" terminals of the simulator in place of the battery.

In discharge mode, the battery simulator uses the current limited lab power supply PS1 as the source and the simulator circuit is inactive. In charge mode, current is forced through the battery input terminals. The low voltage that develops across R8 is amplified by U1 and causes Q1 to shunt the charge current while maintaining the



NOTE: UNLESS OTHERWISE SPECIFIED:
CAPACITORS ARE 25V, CERAMIC

Figure B1. Battery Simulator

power supply PS1 voltage. U2, L1, CR1, C3 and C4 produce housekeeping 12V that is required to operate U1 and drive Q1. The power supply range is 1.5V to 15V. Q1 requires a heat sink. R1 is used for measuring the charge current. R10 and C5 simulate the AC characteristics of the battery.

Controlled Constant-Current Load

Although a constant-power load is a more realistic load, the constant-current load (Figure B2) works better for battery discharge testing because the discharge time gives immediate data on the battery charge level. All that needs to be done is to multiply the current by the discharge time.

For operation in DIRECT mode, the control input has to be above 7V. If the control voltage available is less than 7V, switch to BOOST. The minimum control voltage is then 3.3V. The user has to adjust the potentiometer to the desired current. This can be done by connecting a power supply or battery at above 2V in series with a current meter to the (+) and (–) terminals and adjusting R4.

When the load is connected to a battery, Q1 and Q2 operate in a negative feedback mode and maintain the V_{BE} of Q1 at 0.5V. The voltage across R6 must be between 0.5V and 1.5V, depending on the wiper position of R4, a trim pot. Since the value of R6 is 1Ω, this translates to a constant current of 0.5A to 1.5A. Q1 requires a heat sink.

A voltage doubler (U1, C1, C2, C3, C4, CR1, CR2, R1 and R2) boosts the voltage for the gate of Q2.

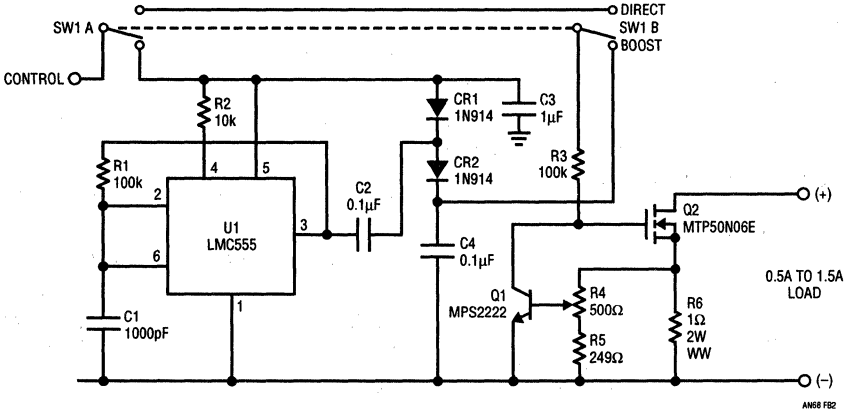


Figure B2. Controlled Constant Current Load

Note: Linear Technology would like to thank Arie Ravid for contributing the majority of the material in this application note.

LT1575 UltraFast Linear Controller Makes Fast Transient Response Power Supplies

Craig Varga

Introduction

The current generation of microprocessors places stringent demands on the power supply that powers the processor core. Allowable supply voltage variations are as low as ±100mV and transient currents are in the range of 5A with 20ns rise and fall times. These requirements demand very accurate, very high speed regulators. The linear solutions employed to date rely on monolithic regulators or PNP transistors driven by low cost control circuits. Because, under the best of circumstances, the response times of these circuits to transient loads are measured in microseconds, these solutions depend on the presence of several hundred microfarads of low ESR decoupling capacitance surrounding the CPU. The cost of these capacitors is a significant percentage of the total power supply cost.

The LT®1575 is an UltraFast™ linear controller that drives a low cost, N-channel, power MOSFET pass transistor and does so with sufficient bandwidth that the bulk decoupling can be *completely* eliminated. As an example, a 200MHz Pentium® processor can operate with only the twenty-four 1µF ceramic capacitors that Intel already requires for the microprocessor. The design uses no tantalum or aluminum electrolytic capacitors on the output. By selecting a sufficiently low on-resistance FET, the dropout voltage of the regulator can be made arbitrarily low. In general, the best performance is obtained with the highest on-resistance (hence, lowest cost) FET that will meet the dropout requirement. Overall system cost and parts count are significantly reduced compared to competing solutions. Reference accuracy is specified as ±0.6% at room temperature and ±1% over the full operating temperature range. Line regulation is typically unmeasureable and load regulation is approximately 1mV for a 5A load change. The LT1575 permits the addition of no-cost current limiting, provides on/off control and has the ability to incorporate thermal limiting for the cost of an external NTC thermistor. The part is available with adjustable outputs or fixed output voltages, in singles and duals (LT1577).

LT1575 Functional Description

Figure 1 shows a block diagram of the LT1575. The basic control circuit consists of a precision bandgap reference, a high gain, wide bandwidth error amplifier and a high speed, low impedance gate-drive stage. The control circuitry is intended to be powered by a nominal 12V (22V absolute max) supply in a typical application, while a lower supply voltage, typically 5V or 3.3V, is used to provide the main input power. The output can be set to any voltage greater than or equal to the reference voltage by proper selection of the feedback divider resistors. The reference is trimmed to a nominal 1.21V. An internal bias supply regulator ensures that the reference will not drift as the supply voltage varies.

Since the MOSFET pass transistor is connected as a source follower, the power-path gain is much more predictable than that of designs that employ PNP bipolar transistors as pass devices. Also, MOSFETs are very high speed devices and are therefore more suitable than PNPs for a wide bandwidth power stage. Another advantage of the follower design is inherently good line rejection. Disturbances on the input supply are not propagated through to the load.

The output driver is designed to be tolerant of capacitive loads, which is precisely what a MOSFET gate will look like to the driver. Driver output impedance is on the order of 2Ω. If the MOSFET used is a very small geometry device with less than approximately 2000pF gate capacitance, it may prove necessary to add between 2Ω and 10Ω in series with the gate. (See page AN69-7 for details.) The error amplifier has an open-loop DC gain of greater than 80dB

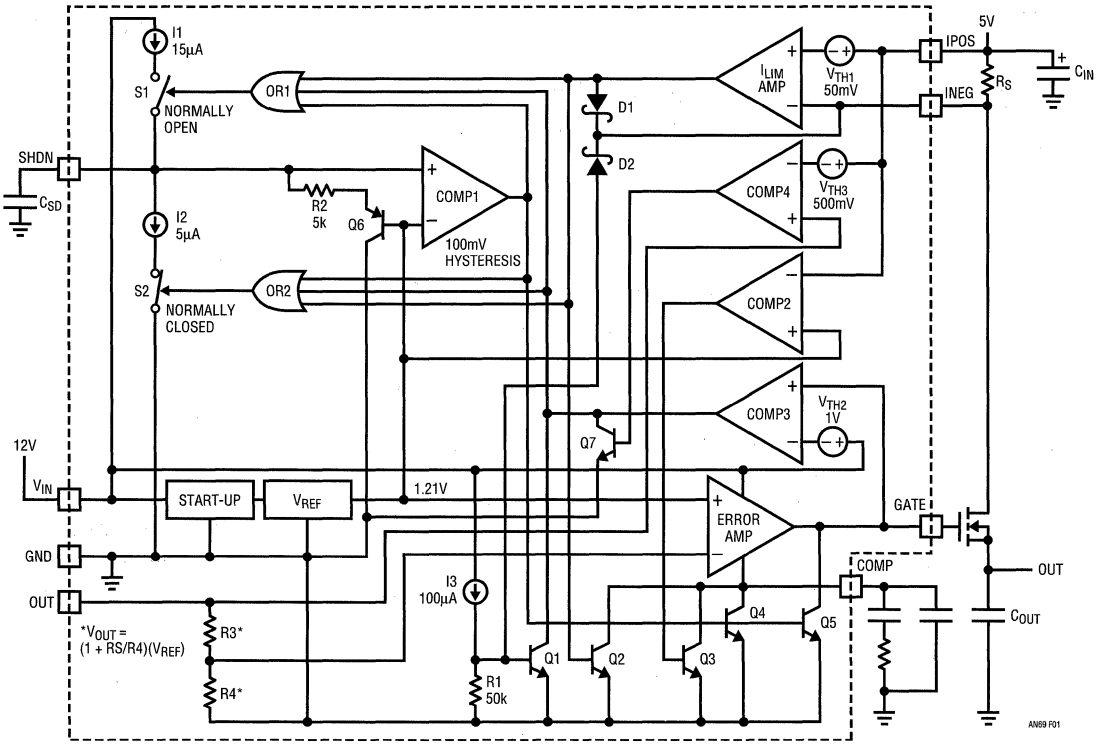


Figure 1. Simplified Circuit of the LT1575

and a typical uncompensated unity-gain frequency of 75MHz. This permits the loop to be crossed over at frequencies on the order of 1MHz and still maintain good phase and gain margins.

Several additional features were included in the design. There are two ways to obtain current limiting. One approach is to add a sense resistor in series with the pass transistor's drain pin to sense load current. The other technique doesn't even need a sense resistor. Let's look at the sense resistor approach first.

The entire load current must flow through the MOSFET drain pin. By connecting a sense resistor between the FET drain and the input supply, the load current can be sensed without reducing the FET's gain. This sense resistor develops a voltage equal to the load current times the sense resistor value. A comparator in the LT1575 looks at the voltage across this resistor, and if this voltage exceeds a 50mV threshold, activates current limit. The 50mV threshold was chosen as a good compromise between low power loss in the sense resistor and reasonable noise immunity.

Several actions are taken when current limit is detected. First, the current limit loop takes control over the output stage. The gate drive voltage is reduced to regulate the current sense voltage to 50mV. In other words, the regulator becomes a current source. Also, referring to Figure 1, current source I2 (5µA sink) turns off and I1 (15µA source) turns on. This starts to charge C_{SD} with approximately 15µA. C_{SD} charges linearly until comparator COMP1 detects that C_{SD}'s voltage has exceeded the 1.21V reference. At this point the chip shuts down, reducing the pass transistor dissipation to zero. This condition is latched. The comparator has approximately 100mV hysteresis to prevent chattering; (this hysteresis is also helpful when using this pin for thermal limit).

There are two ways to restore normal operation after the fault has been cleared. One option is to recycle the input power. The other approach is to pull the Shutdown pin to a voltage below V_{REF}. The time required to latch the output off depends on the value of C1. Use the following formula to select C1: C1 = $(0.012)t_d$, where t_d is delay time in milliseconds and C1 is in µF. By holding shutdown below V_{REF}, the latch-off feature may be disabled and the regulator will continue to output a constant current into a short. This requires being able to sink more than 15µA from the Shutdown pin at less than 1.2V.

The "senseless" current limit technique is activated by grounding Pin 7, the negative current-sense pin. This disables the current limit comparator. A circuit is now enabled (COMP3) that looks at the output driver stage and detects saturation at the positive rail. As soon as saturation is detected, the delay timer is activated, as in the previous case. When the time-out occurs, the output is shut down and latched off. Note that this approach does not limit current while the timer is running. The output current will only be constrained by the input supply and MOSFET limitations. By keeping the timer period short, less than 1ms, the temperature rise in the power FET can be kept under control. Peak currents in this mode of operation may be on the order of 50A to 100A.

There is a slight difference in the operation of this circuit in the fixed-output and adjustable-output versions. In fixed-output parts, comparator, COMP4 of Figure 1, monitors the input/output differential voltage. If this voltage is less than 500mV, the timer will not be allowed to start. This helps prevent false current limit trip-offs caused by turn-on inrush currents, allowing use of a very fast current limit timer. Adjustable parts don't have access to the actual output voltage, only a divided-down version of the output, so this feature is disabled on these devices.

In some cases this can cause a problem. The very large short-circuit currents this circuit can deliver are capable of "dragging down" the input supply in a very short time. The LT1575 undervoltage lockout will then disable the timer and prevent the desired shutdown from occurring.

There are several ways around this problem if it should occur. One solution is to simply set a very short turn-off delay time. As long as the circuit doesn't trip off at turn-on, this is a viable solution. If nuisance tripping at turn-on does occur, two possible solutions exist. The addition of a small RC or a diode/capacitor at the IPOS pin will fix the problem. See Figure 2.

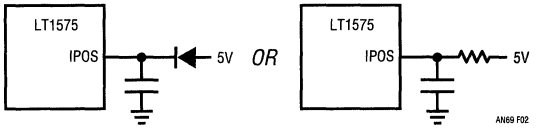


Figure 2. Collapsed-Supply Survival Techniques

The current into IPOS is approximately 1mA. The voltage at IPOS must stay above approximately 2V until the timer shuts the system down. The capacitor value is probably going to be on the order of 5µF to 10µF with the diode circuit for time delays of about 1ms. A low cost aluminum electrolytic capacitor is adequate. The RC circuit won't easily accommodate as long a delay, but for short delays is a little less costly than the diode circuit.

There are no unusual problems related to power sequencing. It makes no difference which supply comes up first. If the 12V supply is late, there is no gate drive available, and thus there is no output. If the main power supply comes up late, there is an undervoltage lockout circuit (COMP2) that ensures that the output remains off until the input rises to approximately 1.2V. Due to the high speed nature of the regulator, turn-on overshoot is virtually nonexistent in a properly designed system.

Typical Applications

Figure 3 shows a typical application circuit. The input voltage is a standard 5V "silver box" and the output is set to 3.50V. This design uses a fixed voltage LT1575 and requires no external feedback divider resistors. Nominal output current is 7A. The current limit of 10A is set by R1, which is a trace on the PC board (see Appendix A for details on designing with trace resistors). The limit need not be very accurate, since the timer circuit will limit temperature rise in the MOSFET. The output filter consists of twenty-four 1µF X7R ceramic, surface mount capacitors. *Proper layout of the decoupling network is crucial to proper operation of this circuit*—see the Board Layout section for details. C7 is set to 0.22µF for approximately 10ms delay time. The MOSFET chosen is an International Rectifier IRFZ24. The specified on-resistance is 0.1Ω and the input capacitance is approximately 1000pF with 1V drain to source. Minimum input voltage for $3.5V_{OUT}$ is determined by the hot on-resistance, which is approximately

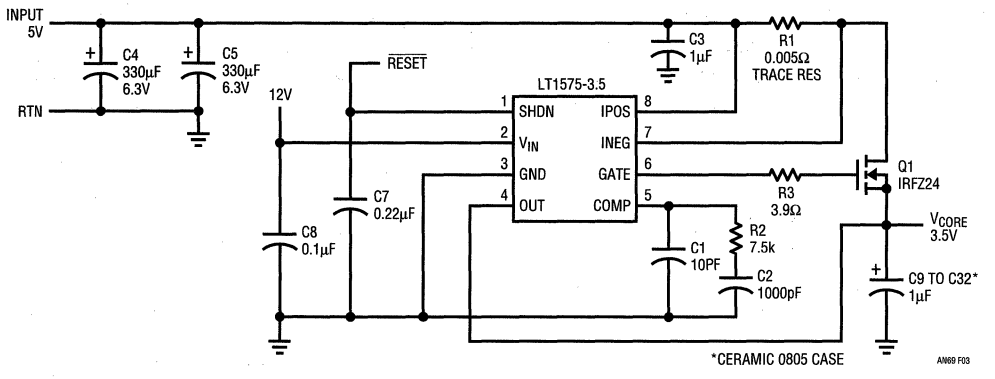


Figure 3. 5V to 3.5V ±100mV Supply

1.5 times the room temperature $R_{DS(ON)}$. The dropout voltage is therefore (0.10Ω)(1.5)(7A) = 1.05V.

Minimum required input voltage is 3.50V + 1.05V = 4.55V.

Figure 4 shows the output voltage transient response to a load step of 200mA to 5A.

Figure 5 shows a circuit that provides a 2.8V output at 5.7A from a 3.3V input. An IRL3303 MOSFET with an on-resistance spec of 0.026Ω is used to meet the low dropout requirement. Decoupling capacitance is the same as in the example above and transient response is similar.

Figure 6 shows the LT1577, a dual regulator. All functions are identical to those of the LT1575. One section is

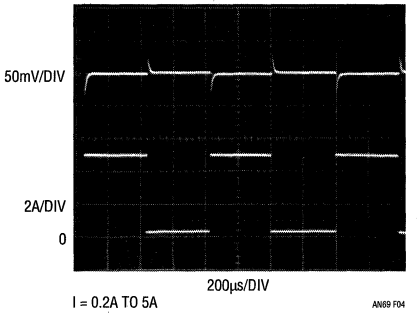


Figure 4. Transient Response

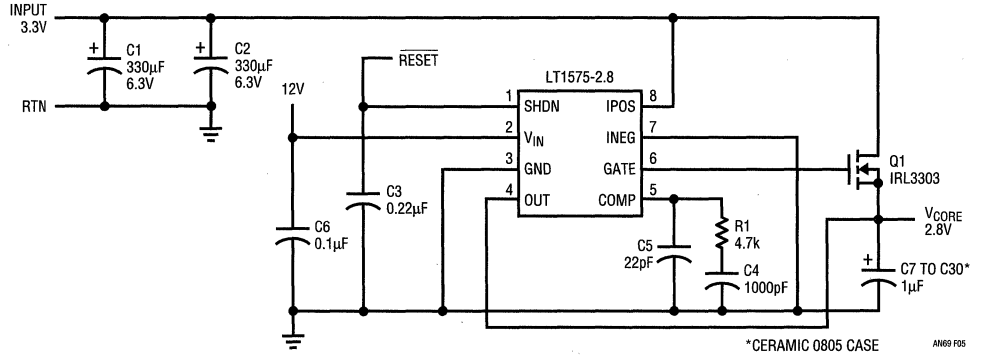


Figure 5. 3.3V to 2.8V ±100mV at 5.7A

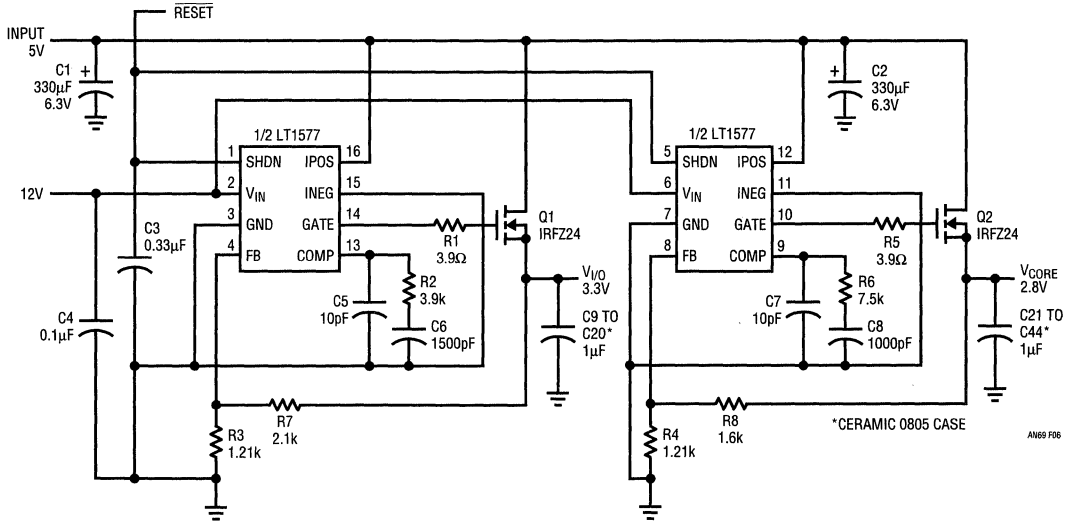


Figure 6. Dual Regulator for "Split-Plane" Systems

configured for a 3.3V output and the other is set up for 2.8V. This circuit provides all the power requirements for a split-plane system: 3.3V for logic and 2.8V for the processor core supply. Both sections use the resistorless current sense for minimum parts count. Note that both Shutdown pins are tied to a common time-delay capacitor. This reduces the charging current from 15µA to 10µA.

If thermal limiting is desired, as might be the case in a relatively low power system that uses a surface mount pass transistor, a low cost NTC thermistor can be configured as shown in Figure 7 or Figure 8. The thermistor used is a Dale NTHS-1206N02. As shown, the trip-off temperature is approximately 120°C for all of these circuits.

In the first case, the design is configured so that the thermal limit will shut the regulator down at 120°C and return to normal operation when the temperature has dropped to approximately 50°C. The regulator will turn back on when the Shutdown pin's voltage has dropped by 100mV. Current limit latch-off is disabled in this case, but if a current sense resistor is employed, current limiting will still be available. The regulator will operate in current limit until the thermal limit is exceeded, then shut off.

Note that the thermistor temperature will be quite a bit lower than the MOSFET tab temperature, even if they are

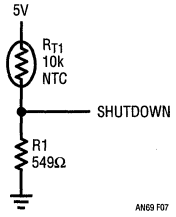


Figure 7. Basic Thermal Limit

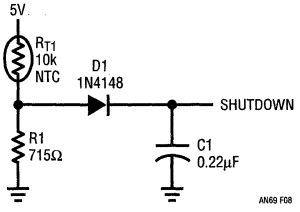


Figure 8. Thermal Limit with Current Limit

in very close physical proximity. It will most likely be necessary to empirically determine the value of the lower divider resistor. This can be done by installing an approximate value for the divider resistor and attaching a thermocouple to the FET drain tab. Run the circuit with normal air

flow and adjust the load current to achieve the desired maximum tab temperature. If the thermal design is good, you may need to disable current limit (short the sense resistor) and operate into a substantial overload to get to the desired temperature. Measure the voltage at the divider center and calculate the thermistor resistance required to produce this voltage. Use this figure to recalculate the divider to get 1.21V across the low leg of the divider at the chosen trip-off temperature.

In the second example, current limit latch-off is enabled, but the accuracy of the temperature limiting suffers due to the variability in the diode V_F. The 1N4148 diode shown here has a V_F of approximately 316mV with a 5μA forward current at 45°C. In this configuration, thermal shutdown is latched off, as is current limit. The Shutdown pin must be pulled low to reenable the supply.

Figure 9 shows an overvoltage protection circuit. If the output exceeds the desired trip level (in this case, 3.36V for a 2.8V supply) the regulator latches off. Current limit latch-off is still functional. Figure 9's circuit could just as easily be connected to the input supply to prevent overheating from excessive input voltage. Figure 10 combines current limit, overvoltage and thermal limiting in one design.

Figure 11 shows how to implement foldback current limiting. A short explanation of the current limit comparator's operation may be helpful. Figure 12 is a simplified schematic of the current limit comparator. The 50mV trip level of the current sense comparator is determined by a 250μA current source and a 200Ω internal resistor in series with the IPOS pin. This current does not flow through the INEG pin. If resistors are added in series with the current sense inputs, they will alter the nominal current sense trip level slightly. Any resistance in series with IPOS will increase the trip threshold by an amount equal to 250μA times R. This can be used to raise the trip threshold above 50mV if desired. The foldback circuit design minimizes alteration of the current limit threshold by keeping the series resistance low (in this case, 10Ω). The two 1N4148 diodes generate an offset voltage of approximately 1.4V so that with a normal input/output differential, the current limit onset is not significantly altered.

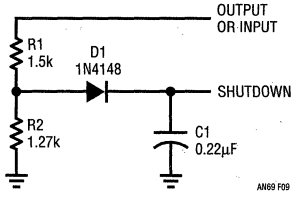


Figure 9. Overvoltage Shutdown

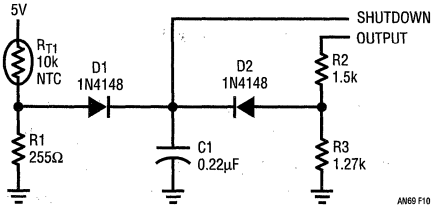


Figure 10. Overvoltage, Thermal Limit with Current Limit

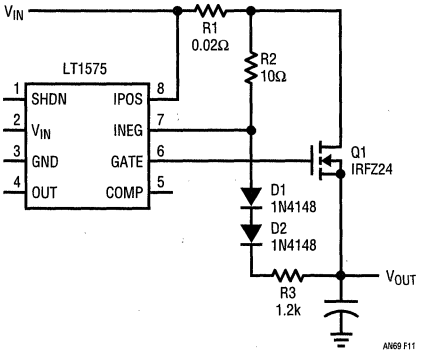


Figure 11. Foldback Current Limit Circuit

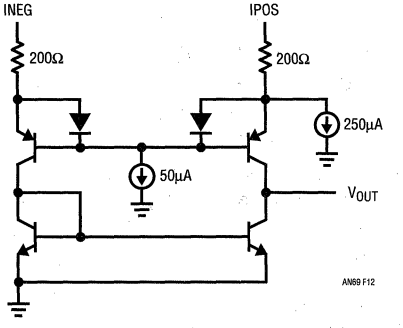


Figure 12. Current Sense Comparator

With V_{IN} = 5V and V_{OUT} = 2.8V, the nominal current through R3 will be quite small, as long as the full output voltage is present. However, when an overload exists, the output voltage falls at the onset of current limit, causing more current to flow through R3. This produces a small offset voltage across the 10Ω resistor. In a hard short, this offset is approximately 30mV; therefore, the voltage across the current sense resistor need only be 20mV instead of 50mV to hold the regulator in current limit. As such, the short-circuit current limit is only 40% of the maximum current. The power dissipation of the pass transistor is greatly reduced with this current limit technique. Figure 13 shows the measured current limit curve for this circuit. Be careful using foldback with nonlinear loads such as lamps or current sources. It is possible for such loads to cause the regulator to get stuck at less than full output voltage.

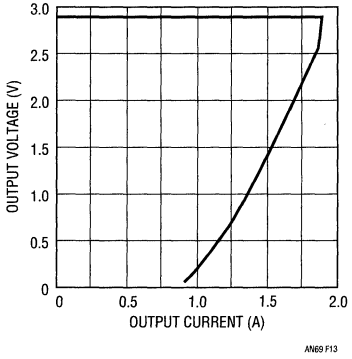


Figure 13. Foldback Current Limit

High Speed Considerations and Component Selection

The secret to success for an LT1575-based design is the ability to achieve very high speed closed-loop performance. As usual, Murphy's law conspires to make life more difficult than we would like. The parasitic elements contained in the PC board traces, as well as the circuit components themselves, conspire to degrade performance. If these parasitics are not properly managed, circuit operation may be disappointing. A good understanding of the critical circuit elements is essential. The following brief tutorial explains the major concerns.

In order to obtain high speed transient response, the LT1575 must develop a large voltage slew rate on the FET gate. The key parameter for FET selection is the FET's transconductance, g_{fs}. The higher this number, the less the total gate voltage excursion required to force a given change in output current; therefore, high gain devices are desired. The FET's input capacitance, C_{ISS}, is less critical. The LT1575's ultimate slew rate will generally be limited by the loop compensation, not the output stage's load capacitance. In tests of typical applications, it was found that a FET with very high gate capacitance and high transconductance will be faster to respond than a very low capacitance device with low transconductance. Higher speeds can generally be obtained from logic-level FETs than from conventional parts. This is due to the much higher g_{fs} specification of logic-level parts.

To reduce cost, select the MOSFET with the highest on-resistance that will meet the dropout specification of the system. There is an inverse relationship between on-resistance and die size. The lower the $R_{DS(ON)}$ specification, the larger the die. More silicon will typically cost more money. For most 5V input to 3.3V or 3.5V output designs, a 0.1Ω MOSFET is sufficient. A standard threshold device such as an IRFZ24 has been shown to be adequate for powering most current-generation processor loads. If faster response is desired, the logic-level IRLZ24 or IRL3303 may be substituted.

MOSFET transconductance is not generally specified at current levels useful for these applications. It may be necessary to calculate a more realistic number from the transfer characteristics of the FET at the current level of interest. A transfer curve plots drain current on the Y-axis against gate source voltage on the X-axis. Find the points on the curve that correspond to the minimum and maximum load conditions. The average incremental transconductance over the load range is $\Delta I_D/\Delta V_{GS}$. The gate voltage will need to change by ΔV_{GS} as the load increases from minimum to maximum. To estimate the slew rate of the LT1575, assume a maximum current out of the COMP pin of approximately 775μA. The slew rate will be 775μA/C_{COMP}, where C_{COMP} is the capacitance from the COMP pin to ground. If there is a series RC to ground, it may be necessary to consider this in the calculation. As long as $\Delta V_{GS}/R_{COMP}$ is much less than 775μA, the series RC can be ignored.

Be sure to look for very high frequency gate oscillations. Small MOSFETs are the most susceptible to this problem. Monitor the gate voltage with an oscilloscope and vary the

load from zero to full load. Look for oscillations in the range of 2MHz to 10MHz. Figure 14 shows an example of a gate oscillation. If such oscillations appear, add a small resistor in series with the FET gate. Start with about 2Ω and gradually increase the value until the oscillations stop. It would be wise to increase the resistor value at least 50% to ensure design margins. It may be possible to reoptimize the loop compensation after adding the gate resistor. The value of the capacitor from COMP to ground (C1 in Figure 3) may be reduced somewhat, since the gate resistor lowers the high frequency gain of the loop.

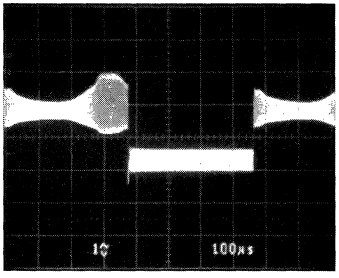


Figure 14. Example of a Gate Oscillation

The MOSFET exhibits several nanohenries of inductance, which appear in series with the device's source and drain leads. The source inductance is by far the most critical. This inductance acts as ballast to degenerate the circuit's high frequency gain. Unfortunately, there isn't anything the user can do to minimize the internal package inductance of the MOSFET. Be careful, however, to minimize the total inductance of the power trace between the FET and the output decoupling capacitors. It appears in series with the internal inductance and must be carefully controlled. Be sure to connect the feedback divider after this inductance, close to the load rather than close to the FET source. Place the FET as close to the load capacitors as possible, and therefore as close to the processor as possible. Unsatisfactory results will be obtained if the FET is placed more than a few centimeters from the load. The additional inductance in the power path will force a significant reduction in the loop crossover frequency to maintain stability. Also, be sure to run a wide (at least 2cm) plane from the FET to the load.

Capacitor selection is very important for proper CPU operation. The load decoupling capacitors must be low impedance devices. They must exhibit minimum levels of ESR (equivalent series resistance) and ESL (equivalent series inductance). Test results on a cleanly laid out board with a 5A load step produced the following data:

Table 1

NUMBER OF CAPACITORS	ΔV FOR 5A LOAD STEP
12	85mV
16	70mV
20	60mV
24	50mV

This test used 1µF, 0805 case surface mount capacitors with X7R dielectric material. Ceramics such as Y5V or Z5U exhibit horrible temperature and bias voltage coefficients. Because there is no bulk capacitance in LT1575 applications, the feedback-loop phase and gain characteristics are largely determined by the value of these capacitors. If the capacitance value changes radically as a function of operating parameters, the chances of loop oscillation increase. In applications where the capacitor temperature is less than 45°C, the low cost Y5V ceramic is adequate. If the temperature is expected to be substantially greater than that, the temperature stability of the X7R material makes it the best choice. The 0805 case parts are also more cost effective than the 1206 case 1µF capacitors. It is preferable to use a large number of low value capacitors in parallel rather than a few larger value parts. The ESR and ESL do not scale with the capacitance and these parasitics will be the parameters that largely control the design. For less demanding applications, it may prove cost effective to use 0.47µF capacitors rather than 1µF. The cost per capacitor is less and the performance hit will not be as large as might be expected. For very cost sensitive applications it may be possible to use Y5V or Z5U material, but only if the expected temperature excursions are small. The loop gain should also be reduced, since more design margin will be needed to prevent oscillations. Use larger capacitor values and a smaller resistor on the COMP node. The transient recovery speed will be lower than can be achieved with the better X7R capacitors.

Board Layout

PC board layout is another critical consideration. A careful analysis of the circuit's parasitics shows that the stray inductance of the power planes and the decoupling capacitors will introduce a double pole at 1MHz to 1.5MHz. The loop must cross over prior to the frequency of this double pole if it is to be stable. Inadvertently doubling the parasitic inductance will make it impossible to stabilize the loop at a frequency high enough to permit adequate transient response. Moreover, the leading edge of the voltage transient due to nearly instantaneous load changes will have excessive amplitude if total inductance isn't carefully controlled. The importance of clean layout cannot be overemphasized. Fortunately, it is not difficult to achieve the required performance. Any layout that will not work with an LT1575 will probably prove unreliable with any regulator.

It is essential to minimize the stray inductance in the interconnects between the decoupling capacitors and the power planes. It is recommended that the capacitors be connected to power and ground islands brought up into the processor socket cavity. These islands then connect to the inner power and ground planes with a liberal sprinkling of vias. In general, plan on a minimum of two vias per end per capacitor. Therefore, in a 24-capacitor system, there should be a total of 96 vias connecting the decoupling capacitors to the power and ground planes.

If the island approach is not used and vias are connected directly to the capacitors' pads, the connections between pads and vias should be as short as possible. Many board designers like to run a 3mm to 4mm length of trace from a pad to a via for good thermal relief. This is far longer than required and produces much more inductance than can be tolerated. A pair of 0.25mm x 4mm traces used to connect a capacitor to a couple of vias will exhibit approximately 1.6nH of inductance. That's more than the capacitor's own ESL by at least a factor of two. It makes little sense to buy a quality, low ESL capacitor and then hook it up with an unintended inductor. Keep vias tangent to the capacitors' solder pads and use two vias per pad.

The LT1575 should have its Ground pin connected directly to the output ground. Run a trace from the LT1575 Ground pin to the closest edge of the processor socket. Keep the trace width at least 0.8mm wide and no more than 5cm long. The controller's own bypass capacitors, feedback divider return and loop compensation return should all connect directly to the chip Ground pin. Do not just drop these connections into the ground plane at the easiest location. Also, be very careful to keep the gate lead far from the Feedback pin. A very clean, high frequency oscillator can be produced by routing these pins too close together. Maintain a minimum of 3mm spacing between these traces. A bit of ground trace placed between these two signals is advisable.

Loop Compensation

Due to the wide bandwidth of the power stage and error amplifier, care must be taken when compensating the feedback loop. The mathematics of the loop-gain analysis is rather complex and is well beyond the scope of this article. Suffice it to say that rather small parasitic elements will cause migraines for the analytical types. An empirical approach will ensure that the desired performance is achieved. After extensive testing, the following recommendations were developed. These compensation values are reasonably conservative and further optimization is possible. However, it is unlikely that a carefully laid out circuit will oscillate if these guidelines are followed. Refer to the Figure 3 schematic:

Table 2

MOSFET TYPE	g_{fs}	C2	R2	C1	R3
IRFZ24	3.1 S	1500pF	7.5k	10pF	3.9Ω
IRLZ24	5.8 S	1500pF	5.6k	10pF	3.9Ω
IRFZ34	4.2 S	1000pF	6.2k	10pF	0Ω
IRLZ34	5.9 S	1000pF	5.6k	10pF	0Ω
IRFZ44	5.3 S	680pF	5.6k	0pF	0Ω
IRLZ44	8.1 S	1000pF	5.6k	10pF	0Ω
IRL3303	6.4 S	1000pF	4.7k	22pF	0Ω

Transconductance numbers used in the above table are average values obtained from stepping the load from approximately 500mA to 5A. The load was changed and the change in gate voltage recorded. g_{fs} was calculated from the results. Capacitor C2 is in series with resistor R2 from the COMP pin (Pin 5) to ground. C1 is connected directly from the COMP pin to ground. R3 is a series gate resistor connected from the gate-drive pin (Pin 6) to the MOSFET gate lead. All of these compensations assume twenty-four 1µF, 0805 case ceramic capacitors with X7R temperature coefficient.

If a smaller quantity of capacitors is used, the value of R2 can be decreased in proportion to the capacitor decrease. This will prove valid down to approximately 50% of the specified capacitor quantity. For example, if an IRFZ24 MOSFET is used with sixteen capacitors, the value of R2 will be (7.5k)(16/24) = 5.0k. Use only the compensation capacitor values in the table.

The circuit should be tested for transient response performance to ensure proper behavior. In order to get a valid test of the design's performance, it is necessary to generate load steps with fast enough edges to excite the loop beyond the crossover frequency. If the edge rates are too slow, the loop will simply track the disturbance without exhibiting its true high frequency behavior. The load steps produced by commercially available electronic loads are completely inadequate for testing this type of circuit. A fast load step generator, such as Intel's Power Validator, which is designed to simulate Pentium processor type load steps, is required. Another approach is to use a power MOSFET to switch a load resistor into and out of the circuit. The load should consist of several surface mount resistors connected in parallel and then connected in series with the FET, as in Figure 15. Drive the FET gate with a square wave from a low impedance driver. Keep the connections between the load pulse circuit and the board as short as possible. Short foils are best used for these interconnects. The inductance of even short wires is excessively high and will produce a great deal of ringing on the output voltage waveform.

It is also desirable, if the equipment is available, to run Bode plots of the open-loop gain and phase. The design should show a minimum of 45° of phase margin under worst-case conditions to ensure stability.

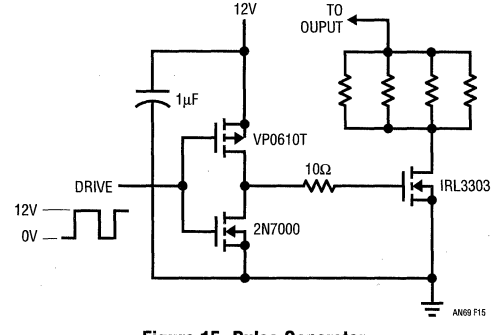


Figure 15. Pulse Generator

Input Filter Considerations

In most 5V input, 3.3V to 3.6V output, monolithic linear regulator designs, the headroom margin is quite small. As a result, a large amount of input filter capacitance is required to ensure that the regulator does not drop out of regulation during a load transient event. Another problem arises because the input source is also likely to be a 5V TTL logic power supply. If large perturbations are induced on the input supply, logic circuits powered by this 5V supply will become unreliable. All of this is still true with LT1575-based designs, but now the designer has an additional option.

Since the dropout voltage of an LT1575-based regulator can be made arbitrarily low by selecting an appropriate MOSFET, the option of adding an input LC filter is now available. Only a very small inductor is required to limit the rate of current rise seen by the input supply. The capacitance on the 5V supply can be greatly reduced as a result of the lowered edge rates. The penalty incurred is a little extra droop at the input to the regulator. However, as was already mentioned, it's a simple matter to meet a lower dropout spec. Figure 16 shows a 5V supply's response to a 5A load step with two 330µF OS-CON capacitors at the regulator input. As would be expected, the instantaneous droop is equal to the capacitor's ESR times the load delta (in this case, $0.015\Omega \times 5A = 75mV$). The MOSFET in this circuit is an IRFZ24. In Figure 17, the MOSFET has been changed to an IRFZ34, which, for a 5A supply, lowers the dropout voltage by about 250mV. A 1µH inductor was added in series with the input supply line, forming an LC lowpass filter. Only one OS-CON capacitor is used on the FET drain. This circuit is shown in Figure 18. The perturbation on the 5V supply is essentially gone. Only the static load regulation error appears on the input supply. The MOSFET drain voltage is now greatly perturbed, as seen in Figure 19. The improved dropout afforded by the larger MOSFET allows for the additional drop at the input without affecting transient response.

The inductor need not be a costly, closed magnetic structure. A very low cost rod core structure is adequate. Magnetic field radiation is limited by the extremely low AC flux swing this type of application induces in the core. In general, this approach can be implemented for the same or slightly less cost than brute force, "throw capacitors at the problem" designs, while affording significantly better system performance.

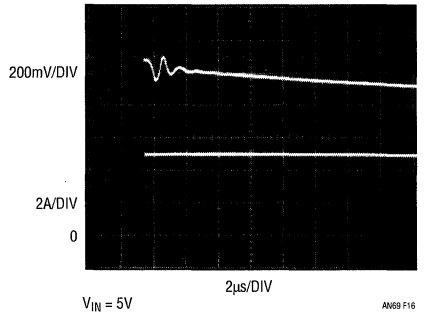


Figure 16. 5V Supply Voltage Ⓐ: Two OS-CONs

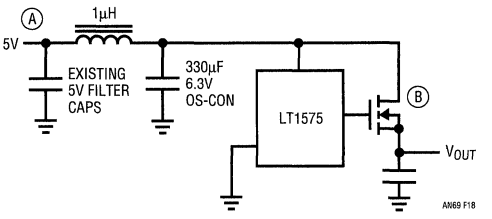


Figure 18. Input Filter Configuration

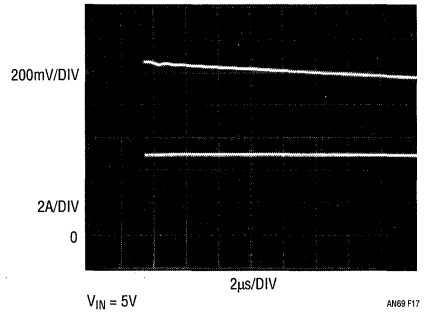


Figure 17. 5V Supply Voltage Ⓐ: One OS-CON + Small Inductor

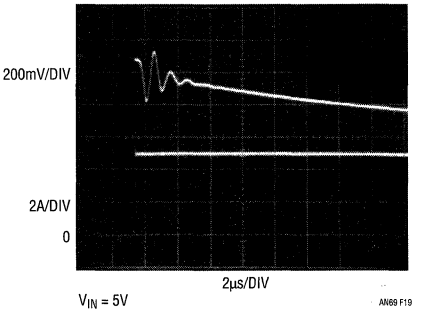


Figure 19. Voltage at FET Drain Ⓑ: One OS-CON + Small Inductor

APPENDIX A

Using PC Board Material as Low Value Resistors

Producing low value resistors for current sense applications is a fairly straightforward process, but a few details must be observed to achieve good results. To obtain the design value of a sense resistor, it is essential that the board's resistivity be well controlled. This is best accomplished by designing the resistors into inner layers rather than outer layers. In a normal board fabrication process, several plating steps deposit additional materials, typically copper and tin, on the outer trace layers. These plating processes are rather poorly controlled. As a result, the resistivity of the outer layers can vary substantially. The inner layers, on the other hand, do not undergo multiple plating operations. The resistivity is quite well defined and is determined largely by the sheet resistance of the starting copper laminate.

The size of the resistance element is determined by several parameters. One must consider the magnitude of the current and the copper sheet thickness to determine the width of the trace. The length is then determined by the desired resistor value.

Recommended Trace Width as a Function of Load Current for a 20°C Rise

Table A1

	0.5oz Cu	1oz Cu	2oz Cu
1A	0.015" (0.38mm)	0.007" (0.18mm)	0.004" (0.10mm)
2A	0.036" (0.91mm)	0.018" (0.46mm)	0.009" (0.23mm)
4A	0.100" (2.54mm)	0.050" (1.27mm)	0.025" (0.64mm)
6A	0.160" (4.06mm)	0.080" (2.03mm)	0.040" (1.02mm)
8A	0.250" (6.35mm)	0.125" (3.18mm)	0.065" (1.65mm)
10A	0.360" (9.14mm)	0.180" (4.57mm)	0.090" (2.29mm)

After selecting the appropriate trace width from Table A1, calculate the required length using the formula below. This equation assumes a trace temperature of 70°C. Also, a generalized formula is presented to use with an arbitrary sheet thickness and temperature.

$$L = (R_S)(1.667)(T_W)(\rho)$$

where:

L is the trace length

R_S is the desired resistance

T_W is the chosen trace width and

ρ is the sheet weight in oz.

The general equation is:

$$L = \frac{(R_S)(T_W)(S_T)}{R_{CU}\left[1+(T_{MAX}-25°C)(T_C)\right]}$$

where:

S_T is the sheet thickness (mm):

for 0.5oz Cu: S_T = 0.017mm

for 1oz Cu: S_T = 0.034mm

for 2oz Cu: S_T = 0.069mm

T_W is the trace width (mm)

R_{CU} is the resistivity of Cu: 18.22μΩ • mm

T_{MAX} is the maximum trace temperature, °C

T_C is the temperature coefficient of Cu, 0.00393/°C

The calculated length is the mean path length of the trace, in other words, the length measured along the trace center line. A serpentine trace may be used to save space if desired.

The resistor should be tied in to the power plane with multiple vias if it is on a different layer than the plane. The best approach is to use a fairly large diameter via (0.8mm to 1mm). If the solder mask is then pulled back from the edge of the hole, the via will solder fill, allowing quite a bit more current carrying ability than an unfilled hole. Allow 2A/via for filled holes and 1A/via for unfilled holes.

If accuracy is desired, Kelvin sensing must be employed. To do this, extend the resistor beyond the calculated length by approximately 2mm on each end, then add a via inboard from each end of the trace such that the distance between these vias is the calculated length. Connect a signal trace to each via. An alternative is to "T" off of the resistor trace with sense leads. See the following sketches.

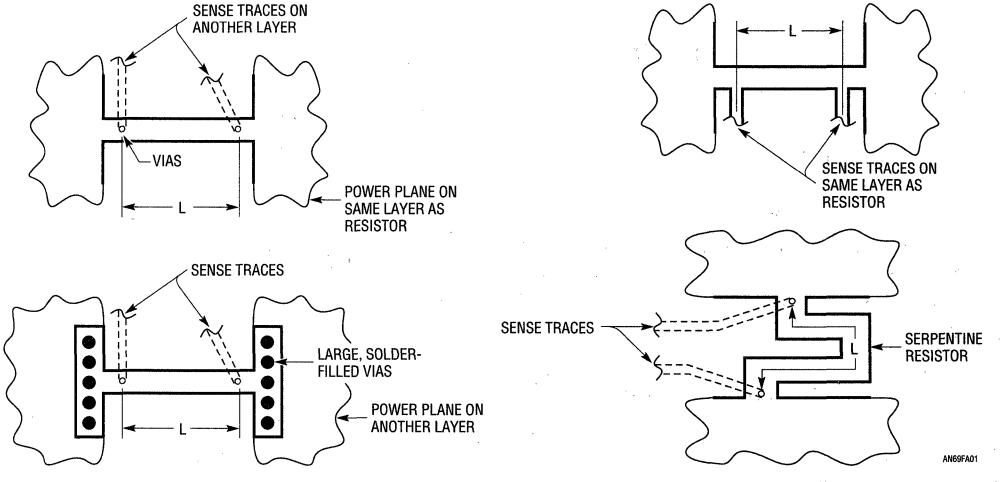


Figure A1. Trace Resistor Configurations

SECTION 2: DESIGN NOTES

SECTION 2—DESIGN NOTES

NOTES

LINEAR TECHNOLOGY

DESIGN NOTES

A Broadband Random Noise Generator – Design Note 70

Jim Williams

Filter, audio and RF communication testing often requires a random noise source. The circuit in Figure 1 provides an RMS amplitude regulated noise source with selectable bandwidth. The RMS output is 300mV with a 1kHz to 5MHz bandwidth selected in decade ranges.

The A1 amplifier, biased from the LT1004 reference, provides optimum drive for D1, the noise source. AC coupled A2 takes a broadband gain of 100. The A2 output feeds a gain control stage via a simple selectable lowpass filter. The filter's output is applied to LT1228 A3, an operational transconductance amplifier. A3's output feeds LT1228 A4, a current feedback amplifier. A4's output, the circuit's output, is sampled by the A5 based gain control configuration. This closes a gain control loop back at A3. A3's I_{SET} input current controls its gain, allowing overall output level control.

To adjust this circuit, place the filter in the 1kHz position and trim the 5k potentiometer for maximum negative bias at A3, pin 5.

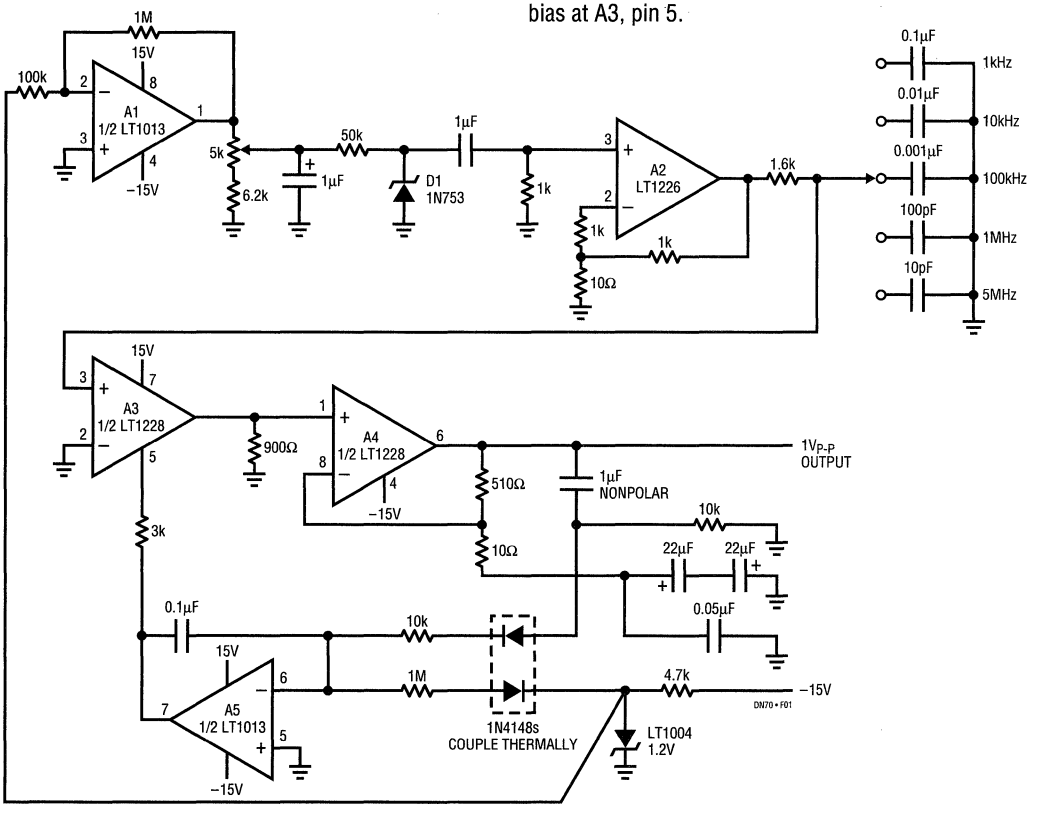


Figure 1. Random Noise Generator with Selectable Bandwidth and RMS Voltage Regulation

Figure 2 shows noise at a 1MHz bandpass while Figure 3 plots amplitude vs RMS noise in the same bandpass. Figure 4 plots similar information at full bandwidth. RMS output is essentially flat to 1.5MHz with about ±2dB control to 5MHz before sagging badly.

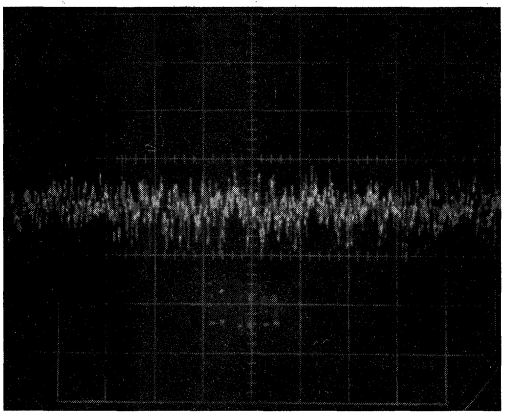


Figure 2. Figure 1's Output in the 1MHz Filter Position

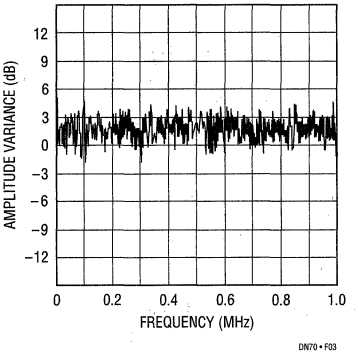


Figure 3. RMS Amplitude vs Frequency for the Random Noise Generator Is Essentially Flat to 1MHz.

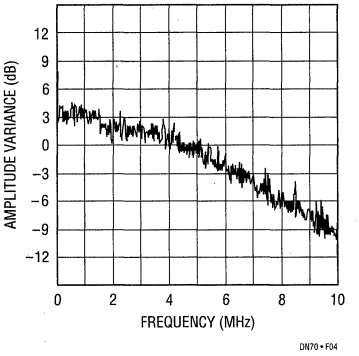


Figure 4. RMS Amplitude Holds Within ±2dB Before Sagging Beyond 5MHz

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DESIGN NOTES

Regulator Circuit Generates Both 3.3V and 5V Outputs from 3.3V or 5V to Run Computers and RS232 – Design Note 71

David Dinsmore and Richard Markell

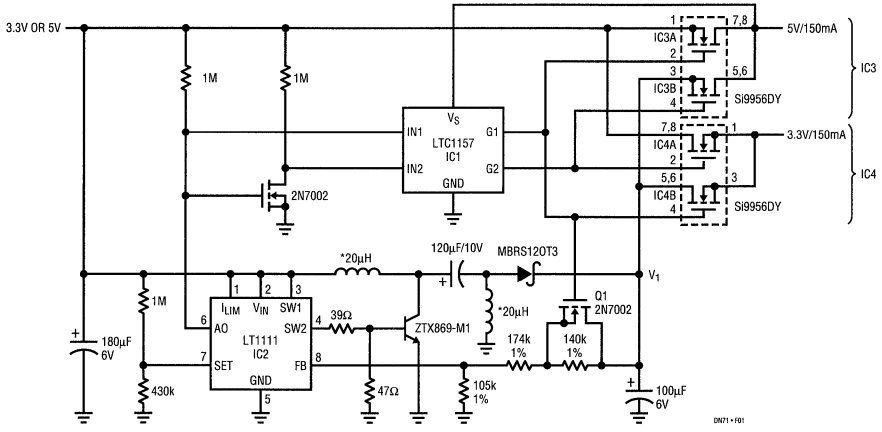
Many portable microprocessor-based systems use a mix of 3.3V and 5V circuits. Some are still using only 5V and inevitably some systems will end up being solely 3.3V based. If accessories are to be plugged into, or connected to any of these systems, a voltage conversion/power generation problem presents itself. The circuit shown in Figure 1 addresses the situation where *either* 5V or 3.3V power is available from the bus, but the accessory needs *both* 5V and 3.3V power.

The circuit consists of two sections, one being a DC/DC converter and the other being a pair of dual N-channel MOSFETs and their associated high-side drivers that effectively form a DPDT switch.

When first powered up, a comparator inside of the LT1111 (IC2) determines the state of the circuit. The comparator's output (IC2, pin 6) is wired to the input of the LTC1157 MOSFET driver (IC1). The LTC1157 internally generates a gate drive voltage which is 8.8V above the supply voltage and efficiently turns on and off the appropriate MOSFETs.

IC2 also forms a flying capacitor buck/boost DC/DC converter circuit. This topology is used so that no transformers are necessary. Q1 is used to control this section's voltage (V_1). When V_{IN} is at 5V, Q1 is off, forcing this section to operate as a step-down converter. It produces 3.3V which is sent to the 3.3V output of the circuit through IC4B. In this state, 5V power is sent directly through IC3A while IC3B and IC4A are off.

When V_{IN} is at 3.3V, IC1 turns on Q1 shorting out the 140k resistor and forcing the DC/DC converter into step-up mode so that it generates 5V at V_1 which is sent to the 5V output through IC3B, while 3.3V power is sent from input to output through IC4A. IC3A and IC4B are off.



*CTX20-3 COILTRONICS
COILTRONCIS (305) 781-8900
ZTX = ZETEX (516) 543-7100

Figure 1.

No load quiescent current is about 500µA. By replacing the LT1111 with the lower frequency LT1173 this could be reduced to 315µA, at the expense of a larger inductor size.

Overall efficiency of the circuit exceeds 80% with V_{IN} = 3.3V and 86% with V_{IN} = 5V. All components are available in surface mount.

Mixed 3.3V and 5V RS232 Operation

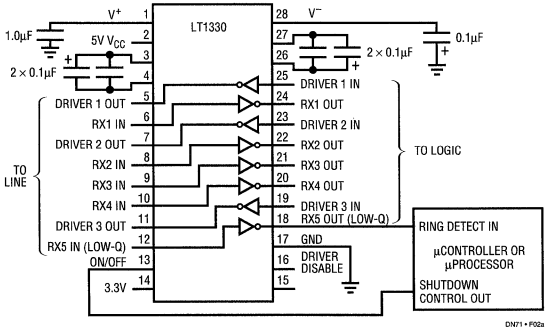
Portable computers also require RS232 interfacing circuitry for inter-computer and mouse interfacing applications. Most portable computers now use a mix of 3.3V and 5V logic. Linear Technology offers a wide variety of interfacing circuits that can, not only work with these voltages, but upgrade to single 3.3V supplies when that is required.

Figure 2 shows the LT1330, a 3-driver/5-receiver, PC compatible, RS232 interface running on both 3.3V and 5V supplies. The LT1330's charge pump power is taken from the 5V supplies maximizing the RS232 transmitters load driving capability. The center trace of the photo demonstrates the ability of the transmitters to drive a 3000Ω/2500pF load at 120k Baud. The drive level shown here are –6V to 7V when fully loaded.

The LT1330's receivers are powered by the 3.3V supply on pin 14. This allows the logic levels to be compatible with either TTL or 3.3V logic since the output logic levels are typically 0.2V to 2.7V. Logic inputs to the transmitters respond to TTL levels, so they can be driven from either 3.3V or 5V logic families.

When the entire system can be operated on 3.3V, an LT1331 may be directly substituted for the LT1330. The LT1331 can be operated at 120k Baud with the only limitation being transmitter output levels are –3.5V to 4V. While these levels are not RS232 compliant, they can be used to interface with all known RS232/RS562 systems. In all cases the LT1331 operated at 3.3V would provide a reliable communications link. The table below shows the details of 3-driver/5-receiver RS232 transceivers for 3.3V and mixed 5V/3.3V systems.

	LT1342	LT1330	LT1331	LTC1327
ESD Protection	±10kV	±10kV	±10kV	±10kV
3V Logic Interface	✓	✓	✓	✓
Power Supply	3V/5V	3V/5V	3V, 5V or 3V/5V	3V
Supply Current in SHUTDOWN	1µA	60µA	60µA	1µA
Receiver Active in SHUTDOWN		✓	✓	
Driver Disable	✓	✓	✓	
External Capacitors	0.1, 0.2µF	0.1, 0.2, 1µF	0.1, 0.2µF	0.1µF
Rx Output (Typ)	0.2V-2.7V	0.2V-2.7V	0.2V-2.7V	0V-3.3V
RS232 Tx Compliant	✓	✓		
RS232 Tx Compatible	✓	✓	✓	✓



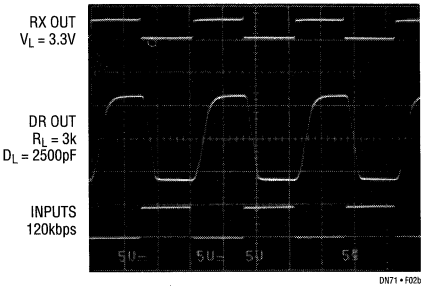


Figure 2. LT1330 Mixed 5V/3V Operation

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LINEAR TECHNOLOGY

DESIGN NOTES

Single LTC1149 Delivers 3.3V and 5V at 17W – Design Note 72

Peter Schwartz

This Design Note shows how one LTC1149 synchronous switching regulator can deliver both 3.3V and 5V outputs. The design's simplicity, low cost, and high efficiency make it a strong contender for portable, battery-powered applications. The circuit described accepts input voltages from 8V to 24V, to power **any** combination of 3.3V and 5V loads totalling 17W or less. For input voltages in the 8V to 16V range, the LTC1148 may be used, reducing both quiescent current and cost. For operation at input voltages below 8V, please contact the factory.

For convenience, the test circuit was built using mostly through-hole components. A follow-on Design Note will give details on building this circuit with surface mount parts.

Performance

Efficiency of this circuit is excellent, generally approaching and frequently exceeding 90% (Figure 1). The cross- regulation between the two outputs (a measure of their interdependency) is quite good (Table 1). At low power levels, the LTC1149 cleanly enters Burst Mode™ operation with a quiescent current of only 0.7mA.

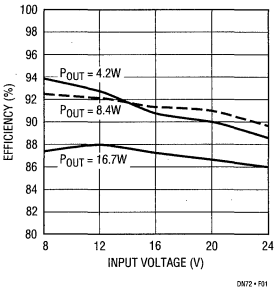

Figure 1. Efficiency vs V_{IN} and P_{OUT}

Table 1. Cross-Regulation vs V_{IN} and I_{OUT}

V_{IN}	$I_{3.3V}$	$V_{3.3V}$	I_{5V}	V_{5V}
8V	0mA	3.43V	0mA	5.14V
	5A	3.27V	0mA	5.19V
	2A	3.42V	2A	4.95V
	0mA	3.52V	3A	4.84V
24V	0mA	3.42V	0mA	5.14V
	5A	3.26V	0mA	5.12V
	2A	3.32V	2A	4.97V
	0mA	3.42V	3A	4.93V

Theory of Operation

The complete circuit is shown in Figure 2. To develop the 3.3V output, the LTC1149 acts as a synchronous step-down (buck) converter. L1A and L1B in series form the 3.3V buck inductor, and the C1/C2 combination is the 3.3V output filter capacitor. When Q1/Q2 are ON, the current through L1 ramps up. When Q1/Q2 turn OFF, Q3 is turned ON to provide the current in L1 with a low resistance recirculation path. This use of Q3 as a synchronous rectifier increases efficiency by virtually eliminating conduction voltage drop.

The 5V output is produced by L1, L2, Q4, and C3/C4. Since Q3 has essentially zero voltage drop when turned ON, the voltage across L1 is fixed at 3.3V during that time. With the voltage across L1 known, transformer action develops a predictable voltage across L2. If Q4 is turned on for the same interval as Q3 (forming a second synchronous rectifier), current will flow from L2 into C3/C4. Using a turns ratio of 2:1 between L1A/L1B and L2, C3/C4 will charge to a total voltage of (0.5×3.3V) + 3.3V = 5V. Feedback to the LTC1149's error amplifier comes from the 3.3V and 5V outputs through R1 and R2 (this "split feedback" enhances cross regulation).

In addition to simplicity, this topology offers some more subtle advantages over other dual output techniques:

1) The 3.3V and 5V outputs are inherently synchronous to each other.

2) Both outputs achieve their rated voltage at the same time after power-up or after a short circuit.

3) A short to ground on either output will automatically disable the other output. This is difficult to achieve with techniques employing two independent control loops.

Circuit Particulars

There are three areas of this circuit which require special attention. They are the transformer (L1A, L1B, L2), the input and output capacitors, and the layout.

The transformer must be trifilar-wound. Trifilar winding is a standard production technique in which three wires are wound at the same time on the same magnetic core. The three resulting coils form a transformer with excellent magnetic coupling. In this circuit these attributes improve cross-regulation and efficiency. Two of the three coils are connected in series to form L1. The third coil becomes the boost winding, L2. This inherently provides the required 2:1 turns ratio between L1 and L2. The test transformer was made by using three windings of ten turns #23 wire, on a Kool Mμ® 77050-A7 toroid (finished size: 0.625" diameter × 0.25" high). If an off-the-shelf transformer is desired, Coiltronics, Inc. and Hurricane Labs both carry suitable parts. Coiltronics can be reached at (305) 781-8900; Hurricane's number is (801) 635-2003.

Kool Mμ is a registered trademark of Magnetics, Inc.

The values and sizes of the input and output capacitors are determined by ESR and ripple current ratings. The following lists critical parameters. Specific vendors and types are suggested in Figure 2.

C1, C2: Total parallel ESR ≤ 0.035Ω
Total I_{RMS} rating ≥ 2.5A
C3, C4: Total I_{RMS} rating ≥ 2.5A
C5, C6: Total I_{RMS} rating ≥ 1.6A

In general, layout practices should follow those for other switching power supplies. Some examples are: keep separate types of grounds separate (e.g., signal ground, main power ground), and return the various grounds to a single common point. Power and ground leads should be kept short and isolated as much as possible from signal traces. Details for the successful layout of circuits using the LTC1148/LTC1149 can be found on the data sheets for these parts, which should be consulted for routing recommendations. As noted above, a surface mount layout for this circuit will appear in the follow-on Design Note.

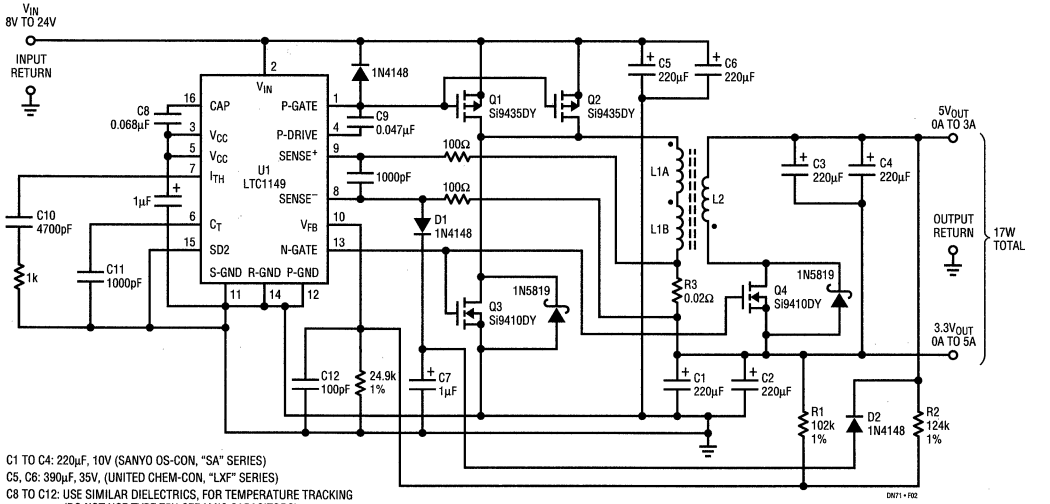

Figure 2. Dual Output LTC1149 Supply Provides High Efficiency at Low Cost

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LINEAR TECHNOLOGY

DESIGN NOTES

A Simple High Efficiency, Step-Down Switching Regulator

Design Note 73

San-Hwa Chee

The new LTC1174 requires only 4 external components to construct a complete high efficiency step-down regulator. Using Burst Mode™ operation, efficiency of 90% is achievable at output currents as low as 10mA. The LTC1174 is protected against output shorts by an internal current limit which is pin selectable to either 340mA or 600mA. This current limit also sets the inductor's peak current. This allows the user to optimize the converter's efficiency depending upon the output current requirement.

To help the user get the most out of their battery source, the internal 0.9Ω (at supply voltage of 9V) power P-channel MOSFET switch is turned on continuously (DC) at dropout. In addition, an active low shutdown pin is included to power down the LTC1174, reducing the no load quiescent current from 130μA to just 1μA. An on-chip low battery detector is also included, with the trip point set by two external resistors.

Figure 1 shows a typical LTC1174 surface mount application. It provides 5V at 175mA from an input voltage range of 5.5V to 12.5V. Figure 2 shows the circuit's efficiency approaching 93% at an input voltage of 9V. Peak inductor current is limited to 340mA by connecting pin 7 (I_{PGM}) to ground. The advantages of controlling the inductor's current include: excellent line and load transient response, short-circuit protection and controlled startup current.

For applications requiring higher output current, connect pin 7 (I_{PGM}) to V_{IN}. Under this condition, the maximum load current is increased to 425mA. Figure 3 shows the resulting circuit. Note that all components remain the same as in Figure 1. The new efficiency curve is shown in Figure 4.

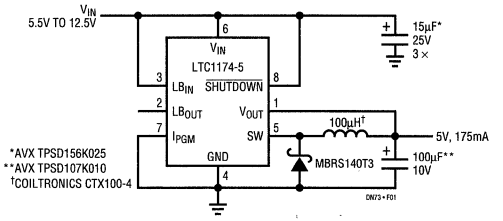

Figure 1. LTC1174 5V, 175mA Surface Mount

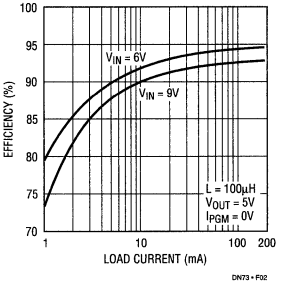

Figure 2. LTC1174 5V, 175mA Efficiency

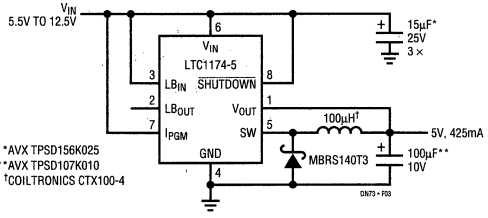

Figure 3. LTC1174 5V, 425mA Surface Mount

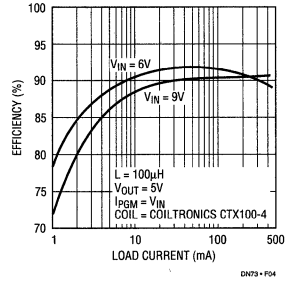

Figure 4. LTC1174 5V, 425mA Efficiency

To have good control of inductor ripple current, a constant off-time architecture is used for the LTC1174. This scheme allows the ripple current to remain constant while the input voltage varies, easing the inductor's selection. However, the switching frequency is a function of input voltage. For an input voltage range of 6V to 12V with an output voltage of 5V, the operating frequency varies from about 42kHz to 146kHz. Figure 5 shows a normalized plot of the switching frequency as a function of the differential input/output voltage. The normalized value of 1 is equivalent to 111kHz.

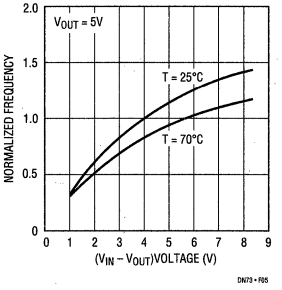

Figure 5. Operating Frequency vs $V_{IN} - V_{OUT}$

100% Duty Cycle in Dropout

When the input voltage decreases, the switching frequency decreases. With the off-time constant, the on-time is increased to maintain the same peak-to-peak ripple current in the inductor. Ultimately, a steady state condition will be reached where Kirchoff's Voltage Law determines the dropout voltage. When this happens, the P-channel power MOSFET is turned on DC (100% duty cycle). The dropout voltage is then governed by the load current multiplied by the total DC resistance of the MOSFET, inductor, and the internal 0.1Ω current sense resistance. Figure 6 shows the dropout voltage as a function of load current.

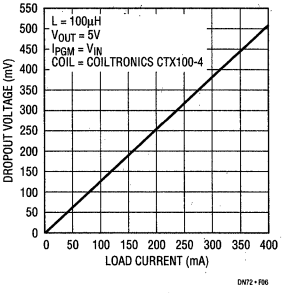

Figure 6. Dropout Voltage vs Output Current

Positive-to-Negative Converter

The LTC1174 can easily be set up for a negative output voltage. If –5V is desired, the LTC1174-5 is ideal for this application as it requires the least components. Figure 7 shows the schematic for this application including low battery detection capability. The LED will turn on at input voltages less than 4.9V. The corresponding efficiency curve is shown in Figure 8.

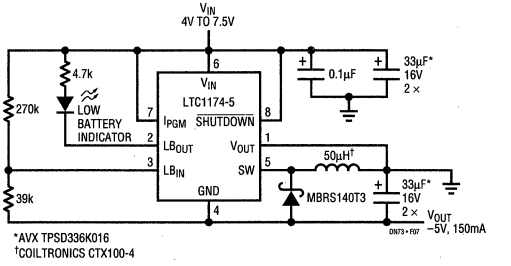

Figure 7. Positive to –5V Converter with Low Battery Detection

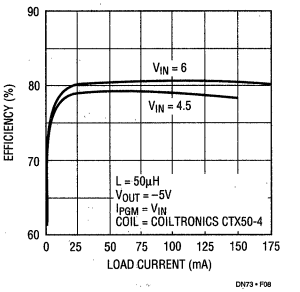

Figure 8. Efficiency vs Load Current for a –5V Output Regulator

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LINEAR TECHNOLOGY

DESIGN NOTES

Techniques for Deriving 3.3V from 5V Supplies – Design Note 74

Mitchell Lee

Microprocessor chip sets and logic families that operate from 3.3V supplies are gaining acceptance in both desktop and portable computers. Computing rates, and in most cases, energy consumed by these circuits show a strong improvement over 5V technology. The main power supply in most systems is still 5V, necessitating a local 5V to 3.3V regulator.

Linear regulators are viable solutions at lower ($I_O \leq 1A$) currents, but they must have a low dropout voltage in order to maintain regulation with a worst case input of only 4.5V.

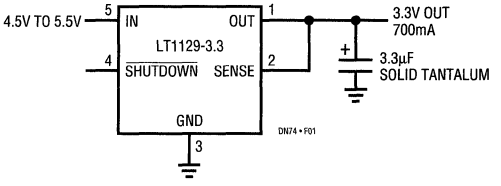

Figure 1. Low Dropout Regulator Delivers 3.3V from 5V Logic Supply

Figure 1 shows a circuit that converts a 4.5V minimum input to 3.3V with an output tolerance of only 3% (100mV). The LT1129-3.3 can handle up to 700mA in surface mount configurations, and includes both 16µA shutdown and 50µA standby currents for system sleep modes. Unlike other linear regulators, the LT1129-3.3 combines both low dropout and low voltage operation. Small input and output capacitors facilitate compact, surface mount designs.

For the LT1129-3.3, dissipation amounts to a little under 1.5W at full output current. The 5-lead surface mount DD package handles this without the aid of a heat sink, provided the device is mounted over at least 2500mm^2 of ground or power supply plane. Efficiency is around 62%.

Dissipation in linear regulators becomes prohibitive at higher current levels where they are supplanted by high efficiency switching regulators. A 2A, 5V to 3.3V switching regulator is shown in Figure 2. This synchronous buck converter is implemented with an LTC1148-3.3 converter. The LTC1148 uses both Burst Mode™ operation and continuous, constant off-time control to regulate the output

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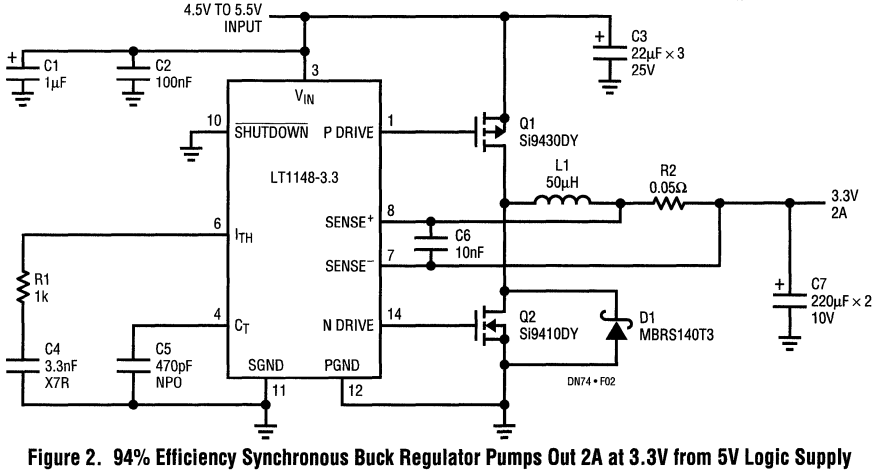

Figure 2. 94% Efficiency Synchronous Buck Regulator Pumps Out 2A at 3.3V from 5V Logic Supply

voltage, and maintain high efficiency across a wide range of output loading conditions. Efficiency as a function of output current is plotted in Figure 3.

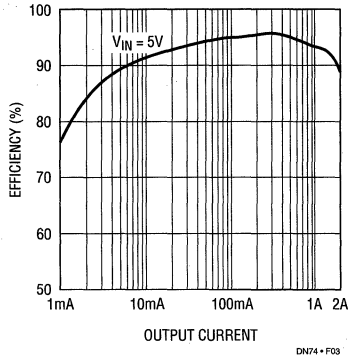

Figure 3. LTC1148-3.3: Measured Efficiency

All of the components used in the Figure 2 switching regulator are surface mount types, including the inductor and shunt resistor, which are traditionally associated with through hole assembly techniques.

Depending on the application, a variety of linear and switching regulator circuits are available for output currents ranging from 150mA to 20A. Choices in linear regulators are summarized in Table 1. There are some cases, such as in minicomputers and workstations, where higher dissipations may be an acceptable compromise against the circuit complexity and cost of a switching regulator, hence the >1A entries. Heat sinks are required.

Table 2 summarizes the practical current range of a number of switching regulators for 5V to 3.3V applications, along with their typical efficiencies.

A 5V to 3.3V converter circuit collection is presented in Application Note 55, covering the entire range of currents listed in Tables 1 and 2.

Table 1. Linear Regulators for 5V to 3.3V Conversion

LOAD CURRENT	DEVICE	FEATURES
150mA	LT1121-3.3	Shutdown, Small Capacitors
700mA	LT1129-3.3	Shutdown, Small Capacitors
800mA	LT1117-3.3	SOT-223
1.5A	LT1086	DD Package
3A to 7.5A	LT1083 LT1084 LT1085	High Current, Low Quiescent Current at High Loads
10A	2 × LT1087	Parallel, Kelvin Sensed

Table 2. Switching Regulators for 5V to 3.3V Conversion

LOAD CURRENT	DEVICE	EFFICIENCY	FEATURES
200mA to 400mA	LTC1174-3.3	90%	Internal P-Channel Switch, 1µA Shutdown
0.5A to 2A	LTC1147-3.3	92%	8-Pin SO, High Efficiency Converter
1A to 5A	LTC1148-3.3	94%	Ultra-High Efficiency Synchronous Converter
5A to 20A	LT1158	91%	Ultra-High Current Synchronous Converter

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LINEAR TECHNOLOGY

DESIGN NOTES

RS232 Interface Circuits for 3.3V Systems – Design Note 75

Gary Maulding

The rapid, widespread use of 3.3V logic circuits complicates the selection of RS232 interface circuits. The optimum choice of an interface circuit should be based upon several application dependent factors:

1) Logic circuitry connected to interface chip
2) Power supply voltages available
3) Power consumption constraints
4) Serial interface environment
5) Mouse driving requirements

As Figure 1 illustrates, 5V interface circuits cannot be used to directly connect to 3.3V CMOS logic circuits. The receiver output level will forward bias the logic circuit's input protection diode, causing large current flow. In the worst case the CMOS logic circuit may latch up. Resistor voltage dividers or level shift buffers may be used to prevent forward biasing the CMOS input diode, but an RS232 transceiver designed for 3V logic application prevents this problem without extra components or power dissipation.

Many of today's systems have both 5V and 3V power supplies. In these systems, an RS232 interface chip which uses the 5V supply for charge pump and driver operation and the 3V supply for receiver output levels, provides the best performance. The 5V operation of the charge pump and drivers gives full RS232 output levels and sufficient current drive for operating a serial port mouse. The LT1342, LT1330, and LT1331 are all good RS232 transceiver choices for systems with both 5V and 3V power. Typical performance waveforms for the LT1342 operating with V_{CC} = 5V and V_L = 3.3V are shown in Figure 2.

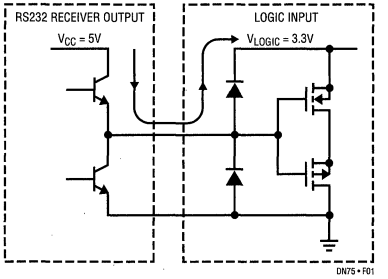

Figure 1. 5V Receiver Forward Biases Logic Input Diode

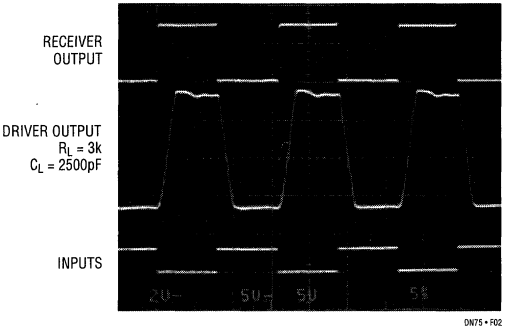

Figure 2. LT1342 Outputs for V_{CC} = 5V and V_L = 3.3V

Systems with only a 3V power supply are unable to use 5V powered RS232 interface circuits. Charge pump triplers (or quadruplers) have losses too great for generating RS232 voltage and current levels from a 3.3V supply. The LT1331 and LTC1327 provide solutions for 3V only systems. The LT1331 circuit is usable in both 5V/3V mixed or 3V only systems. When the charge pump is operated from 3V supplies, it powers the driver circuitry to provide RS562 output levels (see Figure 3). RS562 is a newer serial data interface standard than RS232 with lower (±3.7V) driver output levels and extended (64k baud vs 20k baud) data rates. RS562 systems and RS232 systems are universally interoperable.

The LTC1327 also provides RS562 output levels from a 3V supply. This circuit features ultra-low 300µA supply current to maximize battery life. An advanced CMOS process makes this low current operation possible without compromising the rugged overvoltage and ESD protection available on Linear Technology's bipolar interface circuits.

VPP Switcher Drives 3V RS232

When fully RS232 compliant operation or mouse driving is required in a 3V only system, the LT1332 provides the

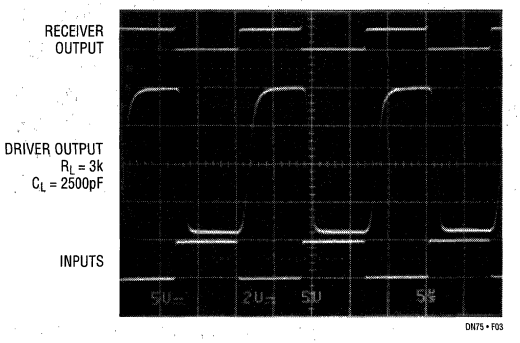

Figure 3. LT1331 Outputs for V_{CC} = V_L = 3.3V

solution. The LT1332 is specifically designed to be used in conjunction with a micropower switching regulator like the LT1109A. The switcher provides 12V needed for flash memory VPP and the RS232 V^+. A capacitor from the switcher's drive pin (V_{SW}) to on-chip diodes in the LT1332 form a charge pump to generate the V^- needed for the RS232 drivers. This two chip solution for VPP generation and RS232 interface is a very economical solution in 3V systems where both these needs coexist. The output driver levels of the LT1332 are fully RS232 compliant and capable of driving serial mice, a capability which cannot be met by other 3V operating circuits.

Battery-powered 3V systems can use the RS232 transceiver's SHUTDOWN and Driver Disable controls to maximize battery charge life. These operating mode controls reduce power consumption when communications needs allow the transceiver to be partially or fully turned off. Keep-alive receivers, available on some transceivers, consume little power (60µA) while monitoring a data line. When data is detected, the system can be fully powered up to accept and process the incoming data.

ESD Protection

ESD transient protection of data lines is essential for equipment reliability. Traditional protection measures using TransZorbs® and diodes are a large percentage of total interface port component costs. Linear Technology's RS232 and RS562 interface circuits reduce this cost by providing 10kV "Human Body Model" ESD protection on the RS232 data lines without external components. This level of protection is adequate in most applications, but when even higher levels of protection are needed, a simple RC network (see Figure 4) may be used. The RC network raises the ESD protection level to 10kV "Machine Model" discharges at a lower cost than TransZorb® based protection networks.

Table 1. RS232/RS562 Transceivers for 5V/3V and 3V Systems

Part No.	5V/3V RS232	3V RS562	10kV ESD	Comments
LT1342	✓		✓	LT1137A Pin Compatible
LT1330	✓		✓	Low Power Burst Mode™
LT1331	✓	✓	✓	V_{CC} Not Used in SHUTDOWN
LT1327		✓	✓	300µA Supply Current
LT1332	3V RS232 Used with LT1109A VPP Generator			

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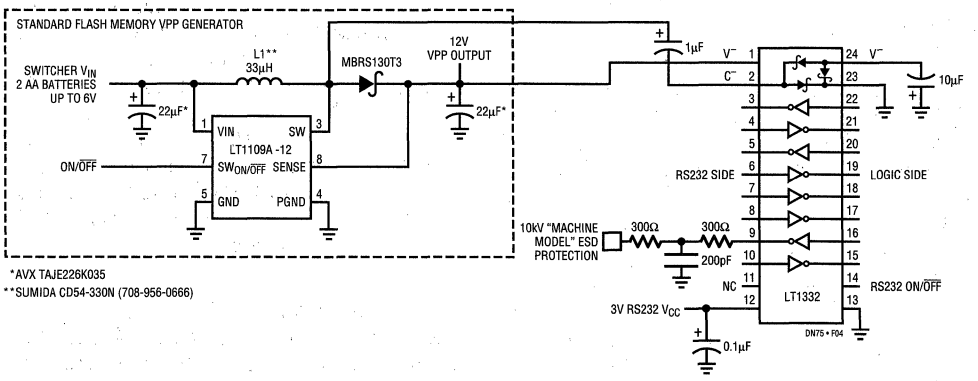

Figure 4. LT1109A-12 and LT1332 Provide VPP Supply and RS232 Interface

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LINEAR TECHNOLOGY

DESIGN NOTES

PC Card Power Management Techniques – Design Note 76

Tim Skovmand

Most portable computers have sockets built in to accept small PC cards for use as extended memories, data/fax modems, network interfaces, wireless communicators, etc. The Personal Computer Memory Card International Association (PCMCIA) has released specifications, 1.0 and 2.0, which outline the general voltage and power requirements for these cards.

Power is provided by the host computer to the PC card through the card socket via the main V_{CC} supply pin(s) and the VPP programming supply pins. Both supplies can be switched to different voltages to accommodate a wide range of card types and applications.

The V_{CC} supply can be switched from 5V to 3.3V and must be capable of supplying upwards of 1A for short periods of time and hundreds of milliamps continuously. Three low resistance MOSFET switches are typically used to select the card V_{CC} power as shown in Figure 1. The LTC1165 inverting triple MOSFET driver accepts active-low logic commands directly from a common PCMCIA controller and generates gate drive voltages above the positive rail to fully enhance low $R_{DS(ON)}$ N-channel MOSFET switches. Two back-to-back MOSFET switches, Q2 and Q3, isolate the parasitic body diode in Q2.

The LTC1165 drives the three MOSFET gates at roughly the same rate producing a smooth transition between supply voltages. Further, the LTC1165 provides a natural break-before-make action due to the asymmetry between the turn-on times and the turn-off times; i.e., no external delays are required. A noninverting version, the LTC1163, is also available. Both devices are available in 8-lead surface mount packaging.

The second path for card power is via the two VPP programming pins on each card socket which are typically tied together. These two pins were originally intended for programming flash memories but are sometimes used as an alternate power source for the card. The VPP supply voltage is therefore capable of being switched between four operating states: 12V, V_{CC}, 0V and Hi-Z. Figures 2 and 3 are two different

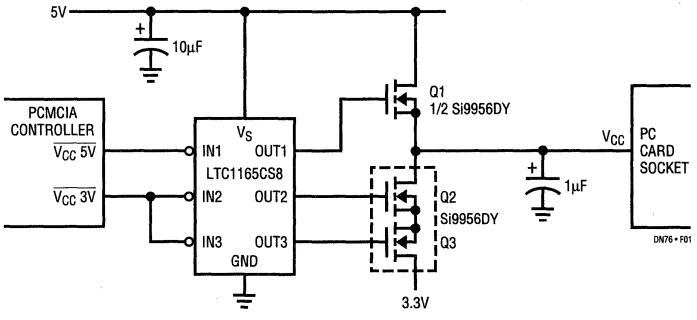

Figure 1. Card V_{CC} 5V, 3.3V Switch

approaches to solving the four state output problem. Figure 2 shows a circuit that produces 12V "locally" by converting the incoming V_{CC} supply through a step-up converter for programming flash memories, etc. This circuit has the unique capability of supplying up to 500mA when the VPP pin is programmed to V_{CC}. Figure 3 is a switched output voltage linear regulator which is powered from a auxiliary 13V to 20V unregulated supply. This circuit supplies 120mA at 12V and protects the card slot from overcurrent damage. The supply currents are listed in the truth table to the right of each schematic. All components shown, including the integrated circuits, are available in surface mount packaging.

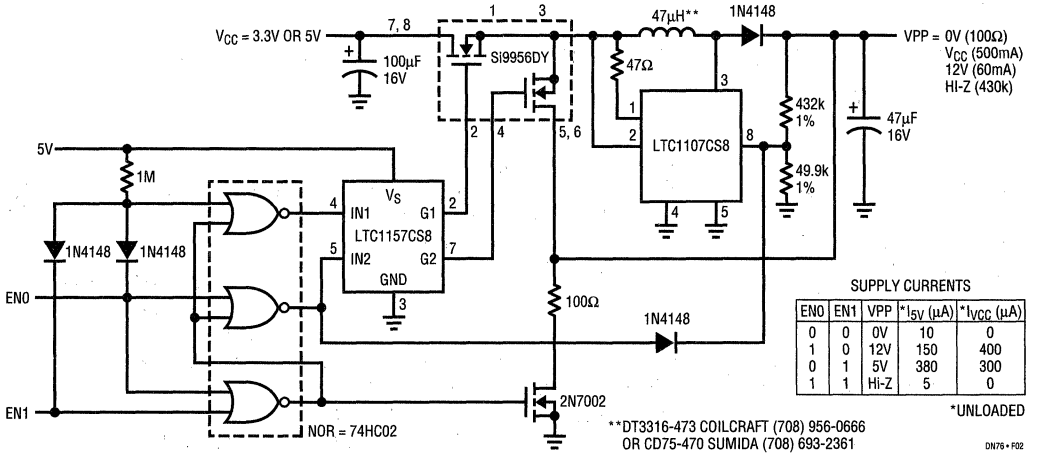

Figure 2. Step-Up Regulator VPP Power Management

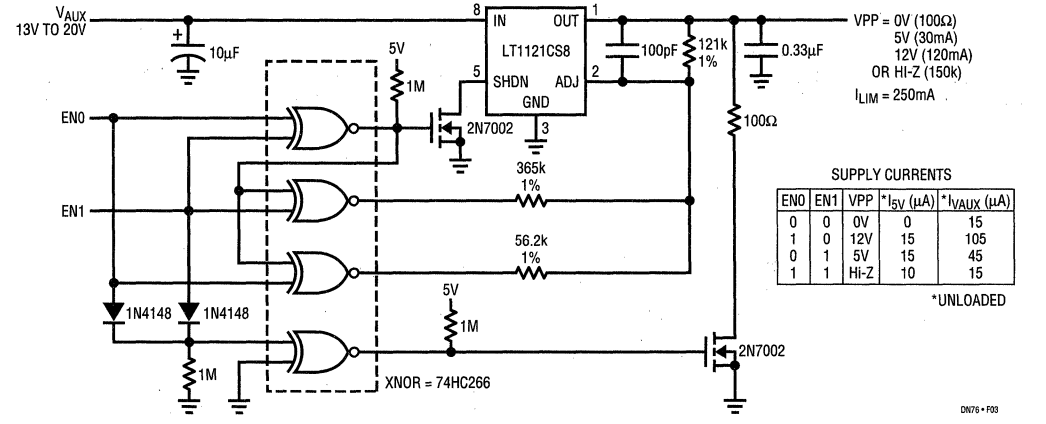

Figure 3. Current-Limited Linear Regulator VPP Power Management

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LINEAR TECHNOLOGY

DESIGN NOTES

Single LTC1149 Provides 3.3V and 5V in Surface Mount

Design Note 77

Peter Schwartz

This Design Note describes a circuit which uses one LTC1149 to regulate both a 3.3V and a 5V output with a 17W capability. The circuit presented is an improved version of the one detailed in Design Note 72 (DN72). Enhancements include an emphasis upon the use of surface mount components and an extended input voltage range (6V to 24V vs 8V to 24V).

The schematic diagram is given in Figure 3. For the principles of operation, please refer to DN72 (copies are available from any LTC representative). One significant difference between this circuit and that of DN72 is that QN2's gate drive is AC-coupled, ensuring full enhancement of QN2 even at low input voltages. The circuit as shown operates down to V_{IN} = 7V. Adding two 220µF capacitors in parallel with C3/C4 extends minimum V_{IN} to 6V or less.

The assembled circuit (Demo Circuit 027A) measures only 2.15" × 1.63" (Figure 1). This compact and inexpensive design provides excellent efficiency, generally approaching and often exceeding 90% (Figure 2).[1] Cross-regulation between the two outputs is also quite good (Table 1).[1] Additionally, network D1/D2/C7 ensures that the 3.3V and 5V outputs both reach their rated voltages at the same time following power-up.

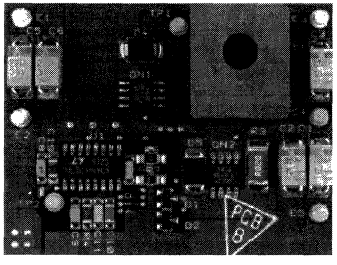

Figure 1. Demonstration Circuit Board

[1]Data at V_{IN} = 6V taken with C_{5V} = (4 × 220µF).

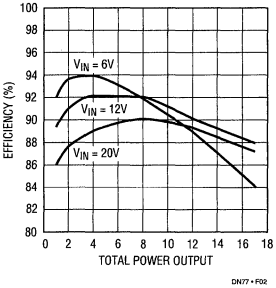

Figure 2. Efficiency vs P_{OUT} and V_{IN}

Table 1. Cross-Regulation vs V_{IN} and I_{OUT}

V_{IN}	$I_{3.3V}$	$V_{3.3V}$	I_{5V}	V_{5V}
6.00V	0mA	3.36V	0mA	5.03V
	5A	3.23V	0mA	5.06V
	2.12A	3.41V	2A	4.80V
	0mA	3.55V	3A	4.68V
8.00V	0mA	3.36V	0mA	5.04V
	5A	3.24V	0mA	5.07V
	2.12A	3.39V	2A	4.90V
	0mA	3.47V	3A	4.81V
24.00V	0mA	3.38V	0mA	5.14V
	5A	3.24V	0mA	5.12V
	2.12A	3.31V	2A	4.98V
	0mA	3.36V	3A	4.93V

Customizing the Circuit

The circuit of Figure 3 is the result of a significant R&D effort by LTC, providing a 3.3V/5V power solution combining performance and price benefits with manufacturability and reliability. At the same time the circuit flexible enough to accommodate a number of variations. Some of these are:

1. **Peak Power > 17W:** Useful for starting disk drives and other "surge" loads, increased peak power is obtained by lowering the value of R3, and if necessary adding capacitance to the 3.3V output to meet equivalent series resistance requirements. Under most conditions, the total ripple current rating of the 3.3V output

capacitance is determined by maximum **continuous** power, (capacitor current ratings are determined by I^2R heating and have an associated thermal time constant). For additional details and assistance, contact the factory.

2. **Lower Power Output:** When the full 17W capability featured here is not needed, some input and output filter capacitors can be removed from the circuit. Frequently QP2 can be deleted as well, and a smaller transformer used. Please consult LTC for further information.

3. **Lowest Cost:** Circuit cost can be reduced by using aluminum electrolytic capacitors for C1 to C6 and C15 to C18. The Nichicon "PL" or United Chemi-Con "LXF" series are good choices. On the outputs, Sanyo 10SA220M OS-CON capacitors (220µF, 10V) provide excellent performance in a small case size. Deleting D5 will save area and cost with only a slight efficiency reduction. In low voltage applications, the LTC1148 can be substituted for the LTC1149, with quiescent current and price advantages. For applications where $V_{IN} \geq 12V$, QP2 can often be removed with little or no effect on efficiency.

Construction Notes:

1. Figure 3 shows several ground lines. These should be run separately (single point ground). Heavy line widths in the schematic indicate wide power and ground traces on the PC board.

2. Pin 10 of the LTC1149 is sensitive to switching noise. The PCB layout should take this into account.

3. The Demonstration Board uses tantalum input filter capacitors (C5/C6 and C17/C18) for space reasons. For best life, specific voltage and current derating criteria apply to tantalum devices. **If these capacitors are to be subjected to voltages in excess of 18V DC, contact the capacitor vendor. For applications where the input will be subjected to high dv/dt or high di/dt surges (e.g., switch closure to a battery pack), aluminum electrolytic input capacitors are definitely preferred due to their higher reliability under such conditions.**

Other:

Linear Technology has a Gerber file of this Demonstration Board (DC027A) available along with a complete parts list. For this Demonstration Board, a Hurricane Electronics Lab throughhole transformer (HL-8700) was used to reduce overall height. Beckman Industrial Corporation has developed a very low profile, surface mount transformer suitable for applications where $V_{IN} \geq 9V$ (HM00-93839). Capacitors C1 to C6 and C15 to C18 are AVX "TPS" series capacitors and **should not** be casually substituted. For more information, Hurricane can be reached at (801) 635-2003, Beckman at (714) 447-2656, and AVX Application Assistance at (800) 282-4975.

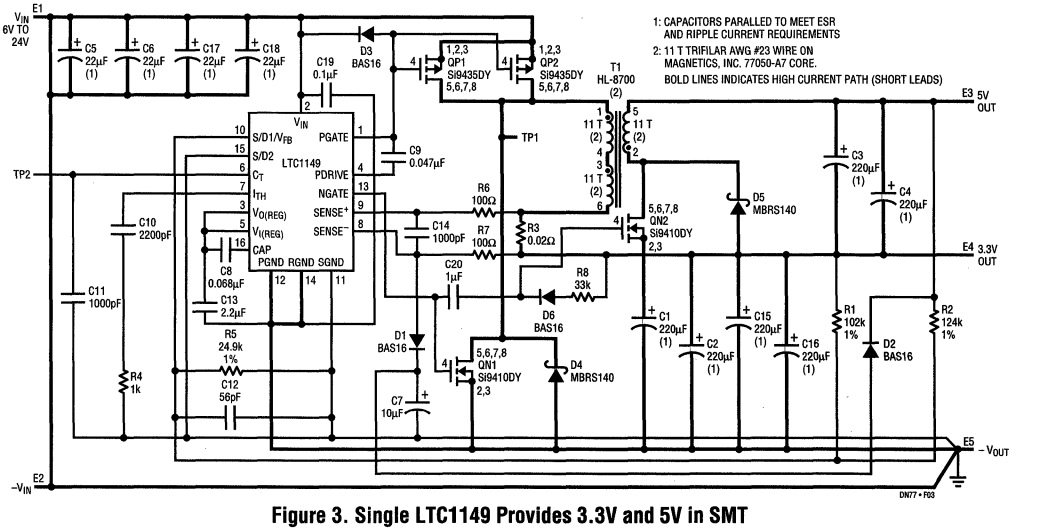

Figure 3. Single LTC1149 Provides 3.3V and 5V in SMT

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LINEAR TECHNOLOGY

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DESIGN NOTES

Triple Output 3.3V, 5V, and 12V High Efficiency Notebook Power Supply – Design Note 78

Randy G. Flatness

The new LTC1142 is a dual 5V and 3.3V synchronous step-down switching regulator controller featuring automatic Burst Mode™ operation to maintain high efficiencies at low output currents. Two independent regulator sections, each driving a pair of complementary MOSFETs, may be shut down separately to less than 20µA/output. This feature is an absolute necessity to maximize battery life in portable applications. Additionally, the input voltage to each regulator section can be individually connected to different potentials (20V maximum) allowing a wide range of novel applications.

The operating current levels for both regulator sections are user programmable, via external current sense resistors, to set current limit. A wide input voltage range for the LTC1142 allows operation from 4V to 16V. The LTC1142HV extends this voltage range to 20V, permitting operation with up to 12-cell battery packs.

Both regulator blocks in the LTC1142 and LTC1142HV use a constant off-time current mode architectures with Burst Mode™ operation. This results in a power supply that has very high efficiency over a wide load current range, fast transient response, and very low dropout. The LTC1142 is ideal for applications requiring 5V and 3.3V output voltages with high conversion efficiencies over a wide load current range in a small amount of board space.

The application circuit in Figure 2 is configured to provide output voltages of 3.3V, 5V, and 12V. The current capability of both the 3.3V and 5V outputs is 2A (2.5A peak). The logic controlled 12V output can provide 150mA (200mA peak), which is ideal for flash memory applications. The operating efficiency shown in Figure 1 exceeds 90% for both the 3.3V and 5V sections.

The 3.3V section of the circuit in Figure 2 is comprised of the main switch Q4, synchronous switch Q5, inductor L1, and current shunt R_{SENSE3}. The current sense resistor

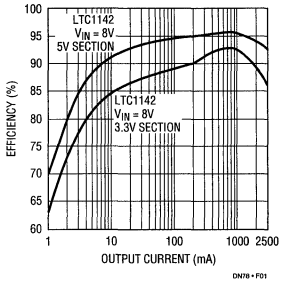

Figure 1. LTC1142 Efficiency

R_{SENSE} monitors the inductor current and is used to set the output current according to the formula $I_{OUT} = 100mV/R_{SENSE}$. Advantages of current control include excellent line and load transient rejection, inherent short-circuit protection and controlled start-up currents. Peak inductor currents for L1 and T1 of the circuit in Figure 2 are limited to $150mV/R_{SENSE}$ or 3.0A and 3.75A respectively.

When the output current for either regulator section drops below approximately $15mV/R_{SENSE}$, that section automatically enters Burst Mode™ operation to reduce switching losses. In this mode the LTC1142 holds both MOSFETs off and sleeps at 160µA supply current while the output capacitor supports the load. When the output capacitor discharges 50mV, the LTC1142 briefly turns this section back on, or "bursts" to recharge the output capacitor. The timing capacitor pins, which go to 0V during the sleep interval, can be monitored with an oscilloscope to observe burst action. As the load current is decreased the circuit will burst less and less frequently.

The timing capacitors C_{T3} and C_{T5} set the off-time according to the formula $t_{OFF} = 1.3 \times 10^4 \times C_T$. The constant off-time architecture maintains a constant ripple current while the operating frequency varies with input voltage. The 3.3V

section has an off-time of approximately 5µs resulting in a operating frequency of 120kHz at 8V input voltage. The 5V section has an off-time of 3.5µs and a switching frequency of 107kHz at 8V input voltage.

The operation of the 5V section is identical to the 3.3V section with inductor L1 replaced by transformer T1. The 12V output voltage is derived from an auxiliary winding on the 5V inductor T1. The output from this additional winding is rectified by diode D3 and applied to the input of an LT1121 regulator. The 12V output voltage is set by resistors R3 and R4. A turns ratio of 1:1.8 is used for T1 to ensure that the input voltage to the LT1121 is high enough to keep the regulator out of dropout while maximizing efficiency.

The LTC1142 synchronous switch removes the normal limitation that power must be drawn from the primary 5V inductor winding in order to extract power from the auxiliary winding. With synchronous switching the auxiliary 12V output may be loaded without regard to the 5V primary output load providing that the loop remains in continuous mode operation.

When the 12V output is activated by a TTL high (6V maximum) on the 12V enable line, the 5V section of the LTC1142 is forced into continuous mode. A resistor divider composed of R1, R5 and switch Q1 forces an offset subtracting from the internal 25mV offset at pin 14. When this external offset cancels the built-in 25mV offset Burst Mode™ operation is inhibited.

For additional high efficiency circuits see Application Note 54.

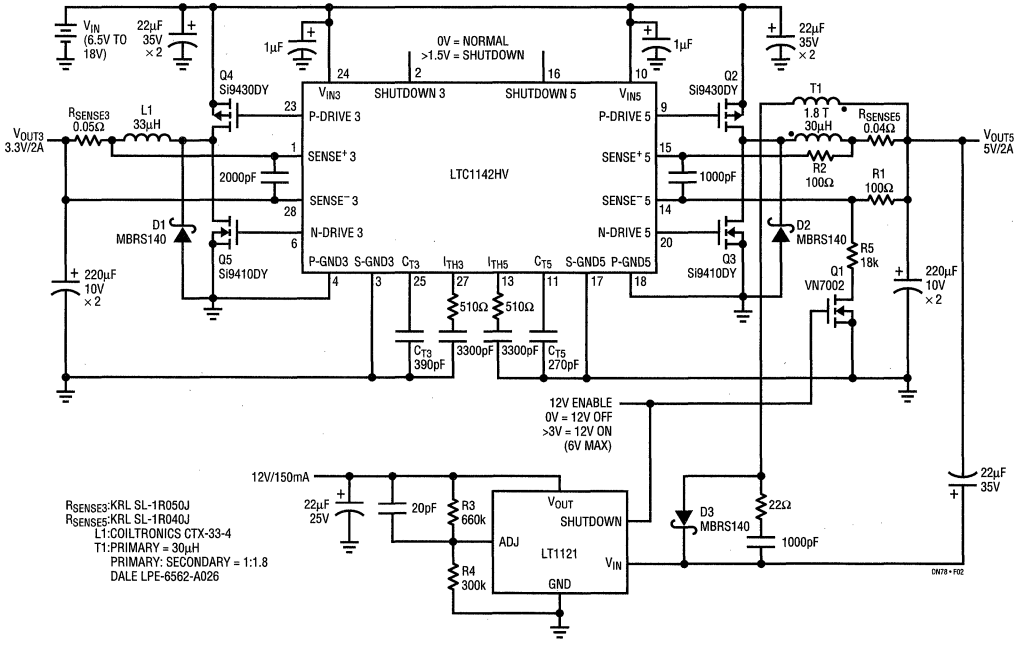

Figure 2. LTC1142 Triple Output High Efficiency Power Supply

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LINEAR TECHNOLOGY

DESIGN NOTES

Single 4-Input IC Gives Over 90dB Crosstalk Rejection at10MHz and is Expandable – Design Note 79

John Wright

Introduction

Professional video systems need to multiplex between many signals without interference from adjacent video sources that are not selected. Final system crosstalk rejection of all non-selected or "Hostile" signals of 72dB is regarded as "professional quality." This level of isolation is very difficult to achieve because every doubling in the number of inputs degrades the crosstalk by 6dB. In the past because no single IC was good enough, cascades of discrete switches and amplifiers were used to achieve the necessary isolation. An additional requirement of some video multiplexers is the ability to switch quickly and cleanly so the sources can be changed in picture without visible lines or distortion. New emerging multimedia systems require the performance of professional systems in the PC environment.

The new LT1204 four-input video multiplexer IC speeds the design of high performance video selection products. It features easy input expansion, and over 90dB crosstalk rejection on a PC board up to 10MHz even when expanded to 16 inputs. Additionally, this new multiplexer has low switching transients and includes a 75MHz current feedback amplifier to drive 75Ω cables. Figure 1 shows the LT1204 in a typical application.

Expanding the Number of Inputs

To expand the number of MUX inputs LT1204s can be paralleled by shorting their outputs together. The Disable feature ensures that amplifier outputs that are not selected do not alter the cable termination. When the LT1204 is disabled (pin 11 low), the output stage is turned off and the feedback resistors are bootstrapped, effectively removing them from the circuit. This has the effect of raising the "true" output impedance to about 25k in Figure 1. The LT1204 disable logic has been designed to prevent shoot-through current when two or more amplifiers have their outputs shorted together. The LT1204 also has a logic controlled shutdown (pin 12 low) that drops the supply current from 19mA to 1.5mA. When shut down, the feedback resistors load the output because the bootstrapping is inoperative. Figure 2 shows this loading effect for a 16-to-1 MUX made with four LT1204s using the Disable feature vs the Shutdown feature.

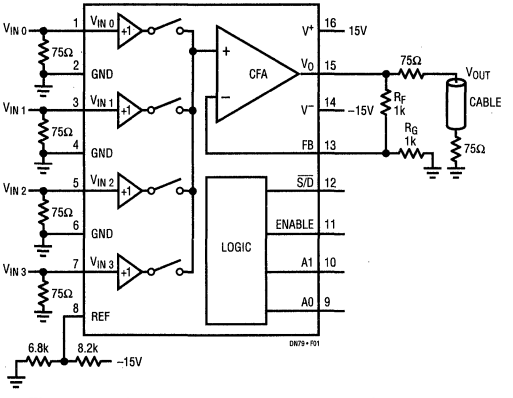


Figure 1. 4-Input Video Multiplexer with Cable Driver

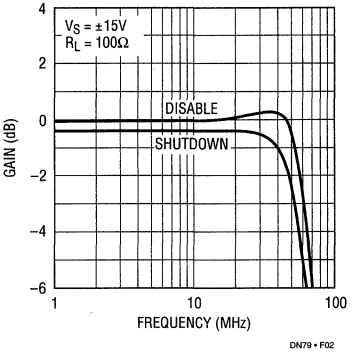
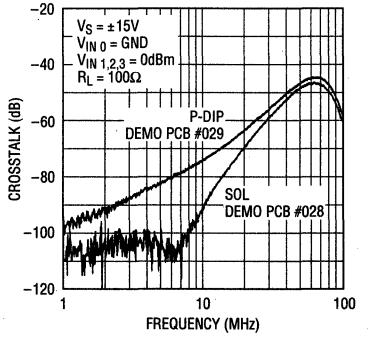


Figure 2. 16-to-1 Multiplexer Response Using Disable Feature vs Shutdown Feature

PC Board Layouts

Crosstalk is a strong function of the IC package, the PC board layout, as well as the IC design. Layout of a PC board that has over 90dB crosstalk rejection at 10MHz is not trivial. PC boards have been fabricated to show the component and ground placement required to attain this level of performance. It has been found empirically from these PC boards that capacitive coupling across the package of greater than 3fF (0.003pF) will diminish the rejection. Keys to the layout are: placing ground plane between inputs, minimizing the feedback pin trace length, putting feedback resistors on the back side of the surface mount PC board, and guarding pin 13 with ground plane.

Crosstalk in P-DIP and SOL vs Frequency

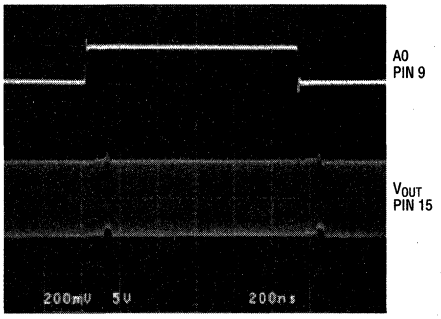


LT1204 • AI01

Switching Transients

Multimedia systems switch active video "in-picture" to create special effects and this requires fast clean transitions with low "glitch" energy. In the past video source selection was made during the blanking period and switching transients were not visible. The LT1204 has input buffers that isolate the internal make-before-break switches. These buffers ensure glitches are minimized at the inputs. This is important because loop-through connections send these glitches to other equipment. When two channels are on momentarily the more positive voltage passes through; if both are equal, there is only a 40mV error at the input of the CFA. The time of this 40mV error can be reduced by adjusting the voltage on the Reference (pin 8). The Reference pin is used to trade off positive input voltage range for switching time. On ±15V supplies, settling the voltage on pin 8 to –6.8V reduces the switching transient to a 50ns duration, and the positive input range reduces from 6V to 2.35V. The negative input range remains unchanged at –6V. Included are photos of the switching transients for the new LT1204 as well as competitive CMOS and bipolar MUXs.

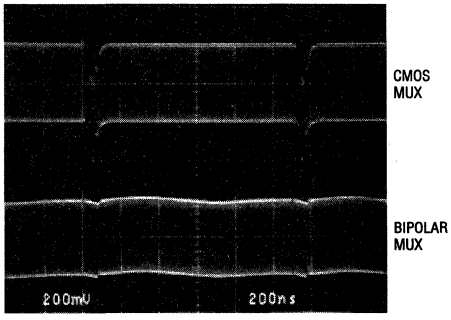
LT1204 Output Switching Transients



$V_{IN\ 0}$ AND $V_{IN\ 1}$ CONNECTED TO A 2MHz SINEWAVE
V_{REF} = –6.8V

DN79 • AI02

Competitive MUXs



$V_{IN\ 0}$ AND $V_{IN\ 1}$ CONNECTED TO A 2MHz SINEWAVE

DN79 • AI03

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LINEAR TECHNOLOGY

DESIGN NOTES

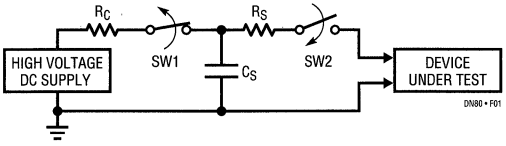
ESD Testing for RS232 Interface Circuits – Design Note 80

Gary Maulding

In 1992 Linear Technology introduced the first RS232 interface circuits capable of surviving in excess of ±10kV ESD transients. Since that time, LTC has introduced more than 30 products with this level of protection. The inherent ruggedness of these products eliminates the need to use external protection devices in most applications. Not one unit has been returned from the field to Linear Technology for an ESD related failure analysis since the enhanced ESD protected devices were introduced.

The ±10kV ESD voltage rating is based on the Human Body ESD Model. When evaluated with other standard ESD test methods, the superior ESD ruggedness of LTC's transceivers gives equally impressive results when compared to older conventional designs.

The various ESD test methodologies all share a common configuration as shown in Figure 1. A source capacitor is first charged to a high voltage, then the high voltage power supply is disconnected from the capacitor, and the capacitor is connected to the device under test through a limiting resistor. The value of the test capacitor and the limiting resistor differ among the various test standards.



ESD Test Model	C_S	R_S
Human Body	100pF	1.5k
Machine	200pF	0
IEC-801	150pF	330Ω

Figure 1. ESD Test Standards

The Human Body Model is the most commonly used ESD test in the United States and is the test method prescribed by Mil-Std-883. This method simulates the ESD discharge waveform seen form human contact to a piece of electronic equipment. The source capacitor is 100pF, limited by 1.5kΩ for the human body model. Linear Technology's RS232 transceivers can withstand in excess of ±10kV when tested with the Human Body Model.

The machine model, commonly used for ESD testing in Japan, is a more severe ESD test. This model simulates metallic contact between the device under test and a charged body. The source capacitor is 200pF with no limiting resistor. The higher source capacitance and the absence of a limiting resistor causes the device under test to be subjected to more voltage, energy, and current than human body model testing. Therefore failures occur at lower test voltages with machine model than with human body model testing. LTC's RS232 transceivers can withstand ±3.5kV when tested with the machine model.

The IEC-801 test method fits between the human body and machine methods in severity. The source capacitor is 150pF with a 330Ω limiting resistor. LTC's RS232 transceivers pass test voltages of ±7.5kV with the IEC-801 method.

The performance of LTC's ±10kV protected RS232 transceivers to each of these test conditions is summarized in Table 1. Also included are protection levels achieved to machine model testing by including a simple RC network on the RS232 line pins. The RC network used is a "T" network formed with two 200Ω resistors and a 220pF capacitor to ground. The added resistance and capacitance are small enough to have negligible effect on RS232 signals, but provide a great increase in ESD protection at a lower cost than using TransZorbs® with a diode network, which is commonly used for ESD protection. Test voltages higher than those shown in

TransZorb® is a registered trademark of General Instruments, GSI

Table 1 sometimes cause device damage. The damage seen most commonly is an increase in driver output leakage with functionality failures occurring at even higher voltages.

Table 1. LTC RS232 Transceiver ESD Test Results

ESD Test Model	Driver Pin Protection	Receiver Pin Protection
Human Body	±10kV	±10kV
Machine	±3.5kV	±6kV
IEC-801	±7.5kV	±8kV
Machine Model with RC Network on RS232 Pins	±10kV	±10kV

ESD Transients During Powered Operation

The test methods discussed so far involve testing for permanent damage to the integrated circuit from ESD transients. In today's portable electronics, interconnection of cables to the communications ports may occur while the equipment is operating. This makes it imperative that the circuit can tolerate the ESD transient with minimal disruption of system operation. LTC's RS232 interface circuits can withstand 10kV ESD transients while operating, shut down, or powered down. Disruption of data transfer is unavoidable during the ESD transient event, but data transmission may resume upon the completion of the event.

Figure 2 is a scope photograph of the data transmission interruption and recovery seen when a –10kV ESD transient strikes a communications line. The test circuit of Figure 3 was used to record this event. The ESD strike is applied to the driver output of an LT1180A and the receiver input of an LT1331. The ESD transient is of too short a duration to be recorded on the photograph, but the effects of the transient can be seen by the corruption of data after the strike. The circuits require about 20µs to recover from the event, after which data transmission continues normally.

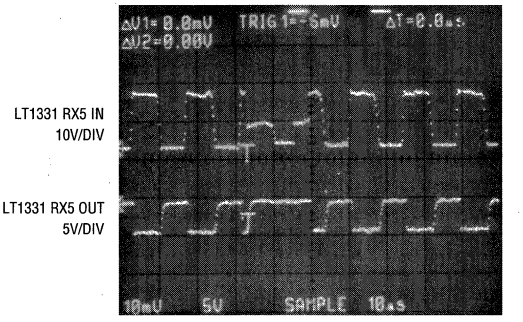


Figure 2. Effects of ESD Transient on Data Transmission Through an LT1331

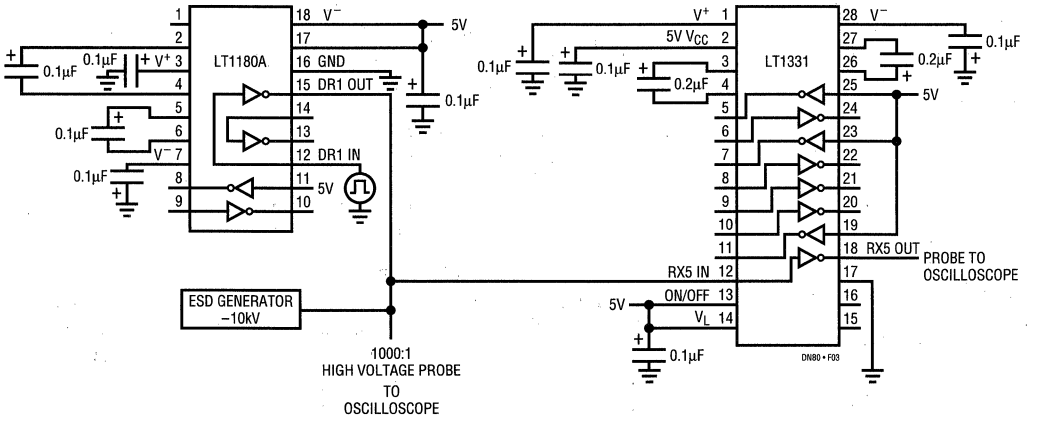


Figure 3. Operating Condition ESD Test Circuit

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LINEAR TECHNOLOGY

DESIGN NOTES

4 × 4 Video Crosspoint Has 100MHz Bandwidth and 85dB Rejection at 10MHz – Design Note 81

John Wright

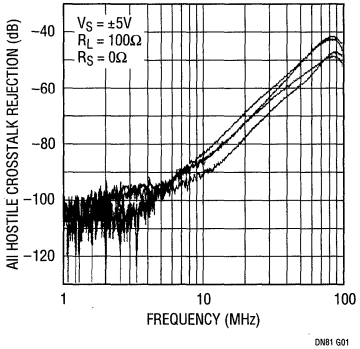
4 × 4 Crosspoint

The compact high performance 4 × 4 crosspoint shown in Figure 1 uses four LT1205s to route any input to any or all outputs. The complete crosspoint uses only six SO packages, and less than six square inches of PC board space. The LT1254 quad current feedback amplifier serves as a cable driver with a gain of 2. A ±5V supply is used to ensure that the maximum 150°C junction temperature of the LT1254 is not exceeded in the SO package. With this supply voltage the crosspoint can operate at a 70°C ambient temperature and drive 2V (peak or DC) on to a double-terminated 75Ω video cable. The feedback resistors of these output amplifiers have been optimized for this supply voltage. The –3dB bandwidth of the crosspoint is over 100MHz with only 0.8dB of peaking. All Hostile Crosstalk Rejection is 85dB at 10MHz when a shorted input is routed to all outputs. Keys to attaining this high rejection include:

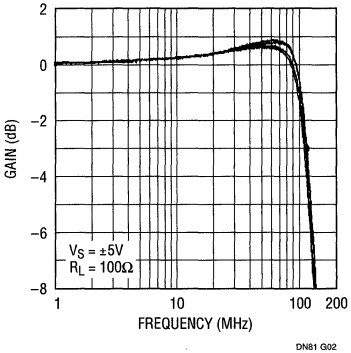
1. Mount the feedback resistors for the surface mount LT1254 on the backside of the PC board.
2. Keep the (–) input traces of LT1254 as short as possible.
3. Route V^+ and V^- for the LT1205s on the component (top) side and under the devices (between inputs and outputs).
4. Use the backside of the PC board as a solid ground plane. Connect the LT1205 device grounds and bypass capacitor's grounds as vias to the backside ground plane.
5. Surround the LT1205 output traces by ground plane and route them away from (–) inputs of the other three LT1254s.

Each pair of logic inputs labeled SELECT LOGIC OUTPUT is used to select a particular output. The truth table is used to select the desired input, and is applied to each pair of logic inputs. For example, to route Channel 1 Input to Output 3, the fourth pair of logic inputs labeled SELECT LOGIC OUTPUT 3 is coded A = Low and B = High. To route Channel 3 Input to all outputs, set all 8 logic inputs High. Channel 3 is the default input with all logic inputs open. To shut off all channels, a pair of LT1259s can be substituted for the LT1254. The LT1259 is a dual current feedback amplifier with a shutdown pin that reduces the supply current to 0μA.

4 × 4 Crosspoint All Hostile Crosstalk



4 × 4 Crosspoint Response



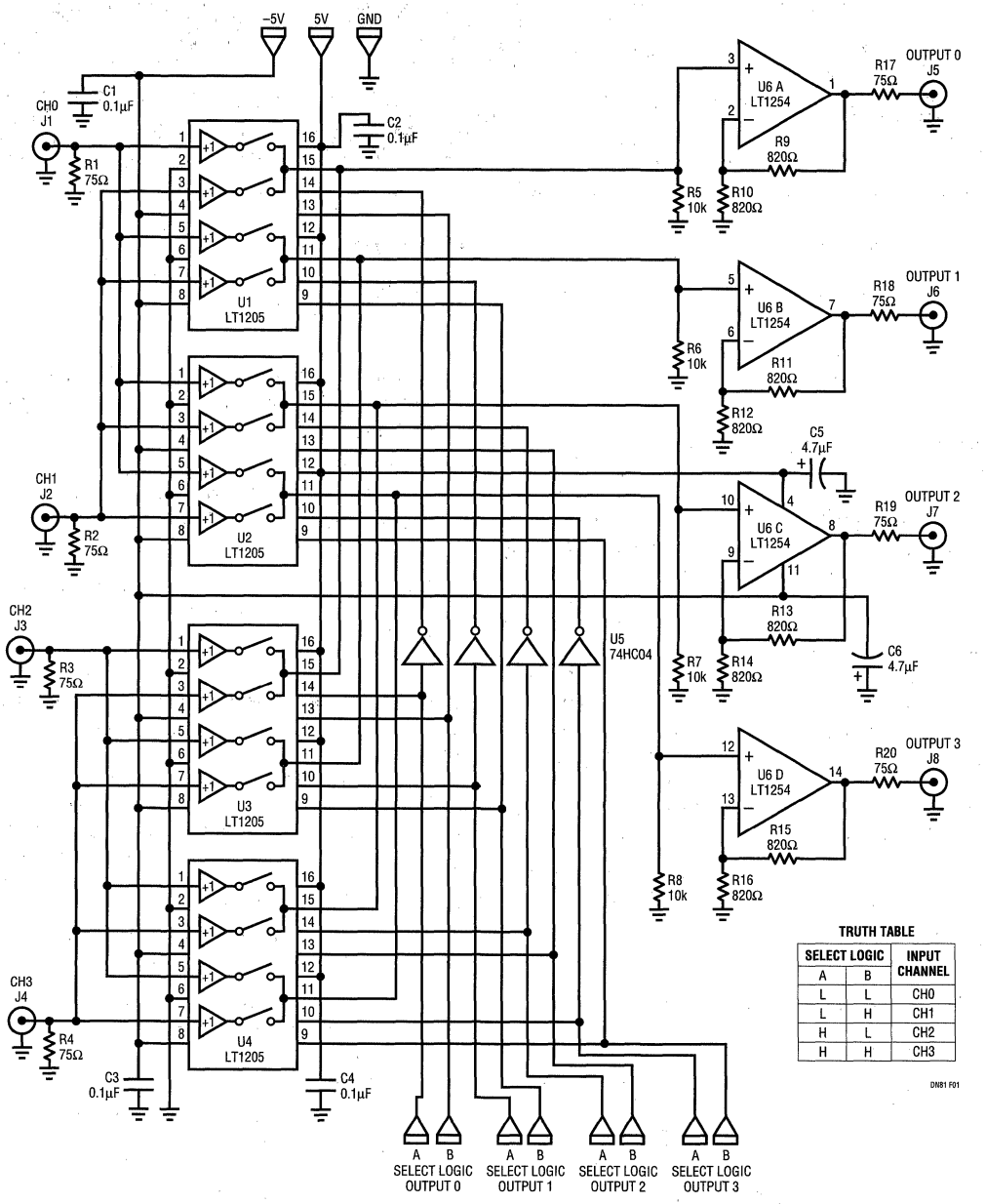


Figure 1. 4 × 4 Crosspoint and Truth Table

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LINEAR TECHNOLOGY

DESIGN NOTES

5V to 3.3V Regulator with Fail-Safe Switchover – Design Note 82

Mitchell Lee

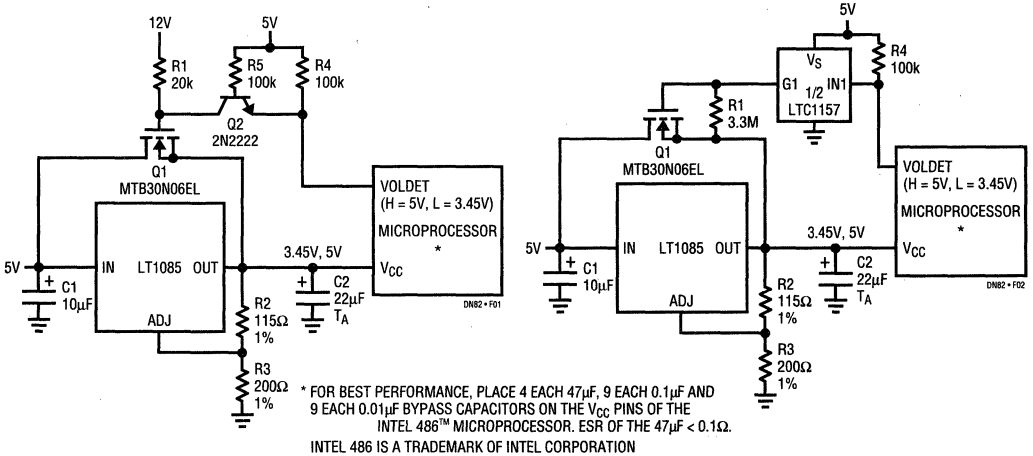
Newer microprocessors designed for replacing existing 5V units operate from lower voltage supplies. In the past a processor swap was simply a matter of removing one IC and replacing it with an updated version. But now the upgrade path involves switching from a 5V chip to one that requires 3.xxV.

One means of changing supply voltage from 5V to 3.xxV is to clip a jumper that bypasses a local 3.xxV regulator. This is not a good solution since it leaves too much to chance. Failure to remove the jumper can result in the instant destruction of the new microprocessor upon application of power. A means of automatically sensing the presence of a 3.xxV or 5V processor is necessary.

Intel microprocessors include a special pin called "VOLDET" which can be used to determine whether or not a particular chip needs 3.xxV or 5V. Figure 1 shows a simple circuit that takes advantage of this pin to automatically "jumper out" a 3.xxV regulator whenever a 5V processor is inserted into the socket. VOLDET is pulled low on 3.xx processors; it is buffered by transistor Q2 which grounds the gate of a bypassing switch (Q1). Q1 is turned off leaving the LT1085 to regulate the microprocessor's V_{CC} line.

For 5V microprocessors the VOLDET pin is high; Q2 is turned off allowing Q1's gate to pull up to 12V, turning itself on. With the LT1085 shorted from input to output by the MOSFET, 5V flows directly to the microprocessor. No service intervention is required to ensure correct V_{CC} potential.

The circuit in Figure 1 is fine for cases where 12V is available to enhance the MOSFET switch. However, in portable applications, 12V is frequently not available or available only on an intermittent basis. Figure 2 shows a second solution using a high-side gate driver to control the MOSFET. A VOLDET pull-up resistor is required in both figures because in some cases VOLDET



* FOR BEST PERFORMANCE, PLACE 4 EACH 47µF, 9 EACH 0.1µF AND 9 EACH 0.01µF BYPASS CAPACITORS ON THE V_{CC} PINS OF THE INTEL 486™ MICROPROCESSOR. ESR OF THE 47µF < 0.1Ω.

INTEL 486 IS A TRADEMARK OF INTEL CORPORATION

Figure 1. Bypass Circuit for 3.xxV and 5V Microprocessor Swaps Using Transistor Buffer

Figure 2. Bypass Circuit for 3.xxV and 5V Microprocessor Swaps Using High-Side Gate Driver (No 12V Supply Required)

is an open circuit or a shorting link, and in other cases it is an open-drain output.

VOLDET is pulled up to 5V in both circuits. This could pose a problem for 3.xxV processors with open-drain VOLDET pins, but for 3.xxV devices VOLDET is always pulled low and 5V never reaches it. The 5V reaches VOLDET only on 5V devices.

For certain families of microprocessors, 3.3V is required. The circuits shown in Figures 1 and 2 are fully compatible with 3.3V applications by simply substituting a fixed 3.3V version of the regulator (use an LT1085-3.3). Higher current operation is also possible. The LT1085 is suitable for 3A applications; use an LT1084 and an MTB50N06EL for up to 5A. Table 1 shows the wide range of linear regulators available at currents of up to 10A.

In some applications the complexity of a high efficiency switching regulator may be justified for reasons of battery life. Figure 3 shows a switcher that not only converts 5V to 3.45V but also acts as its own bypass switch for applications where a 5V output is required. An open drain or collector pulling the V_{FB} pin low causes the top side P-channel MOSFET to turn on 100%, effectively shorting the output to the 5V input. If the open collector is turned off, the LTC1148 operates as a high efficiency buck mode power converter, delivering a regulated 3.45V to the load. For 3.3V applications a fixed 3.3V version of the LTC1148 is available.

Table 1. Linear Regulators for 5V to 3.3V Conversion

LOAD CURRENT	DEVICE	FEATURES
150mA	LT1121-3.3	Shutdown, Small Capacitors
700mA	LT1129-3.3	Shutdown, Small Capacitors
800mA	LT1117-3.3	SOT-223
1.5A	LT1086	DD Package
3A to 7.5A	LT1083 LT1084 LT1085	High Current, Low Quiescent Current at High Loads
10A	2 × LT1087	Parallel, Kelvin Sensed

The topic of powering low voltage microprocessors in a 5V environment is covered extensively in Application Note 58, available on request. Both linear and switching solutions are discussed.

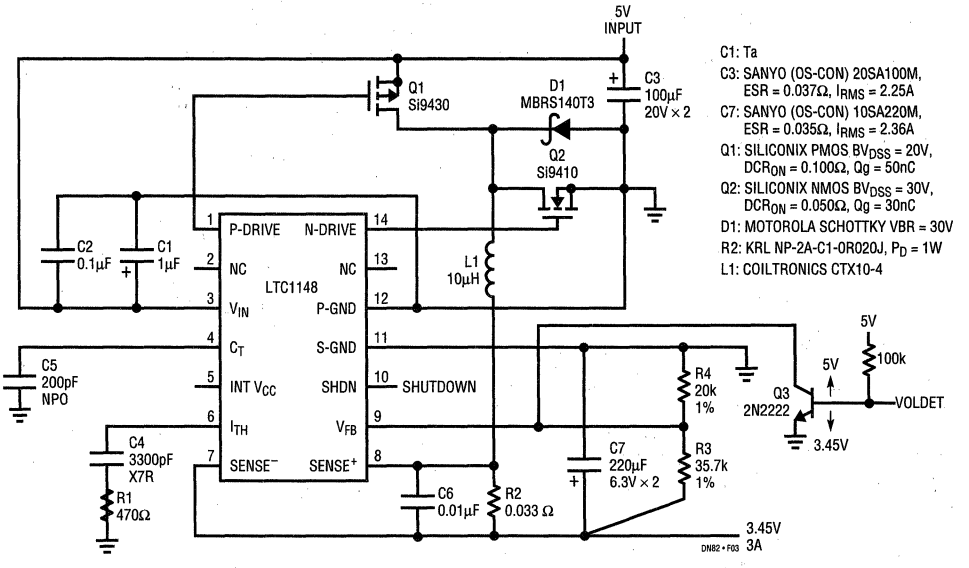


Figure 3

For literature on our Linear Regulators, call **1-800-4-LINEAR**. For applications help, call (408) 432-1900, Ext. 361

LINEAR TECHNOLOGY

DESIGN NOTES

C-Load™ Op Amps Tame Instabilities – Design Note 83

Richard Markell, George Feliz and William Jett

Introduction

By taking advantage of advances in process technology and innovative circuit design, Linear Technology Corporation has developed a series of C-Load op amps which are tolerant of capacitive loading, including the ultimate, amplifiers which are stable with any capacitive load. These amplifiers span a range of bandwidths from 1MHz to 140MHz. They are suited for a wide range of applications from coaxial cable drivers to capacitive transducer exciters.

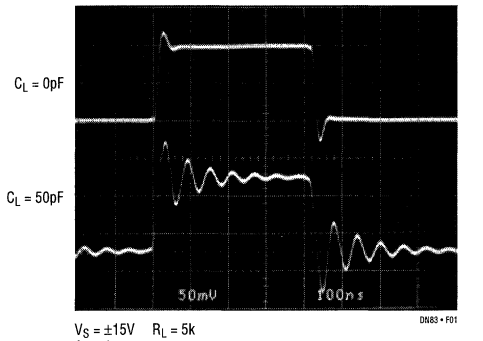
The Problem

The cause of the capacitive load stability problem in most amplifiers is the pole formed by the load capacitance and the open-loop output impedance of the amplifier. This output pole increases the phase lag around the loop which reduces the phase margin of the amplifier. If the phase lag is great enough the amplifier will oscillate.

External networks can be used to improve the amplifier's stability with a capacitive load but have serious drawbacks. For instance, most designers are familiar with the use of a series resistor R_S between the load and the amplifier output. The optimum value of R_S depends on the load capacitance, so this approach isn't useful for ill-defined loads. Further disadvantages of the external approach include reduced output swing and drive current, and increased component count.

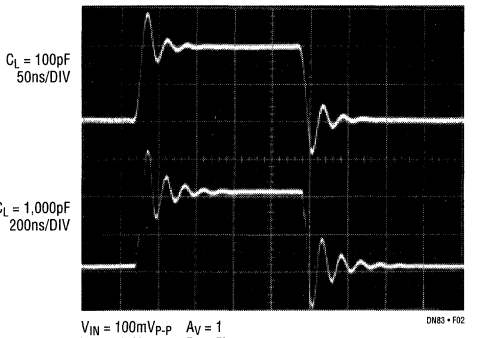
An Example

Figure 1 shows an example of a competitor's medium speed device which is sensitive to capacitive loading. When 50pF is paralleled with a 5kΩ load, the response exhibits considerable ringing. With a 75pF load the device oscillates. By comparison, the transient responses of the 50MHz LT1360 voltage feedback amplifier (Figure 2) shows the improvement in stability achieved in the latest generation of C-Load op amps. In fact the LT1360 maintains a stable transient response for any capacitive load.



V_S = ±15V R_L = 5k
A_V = 1

Figure 1. Medium Speed Non-LTC Op Amps



V_{IN} = 100mV_{P-P} A_V = 1
V_S = ±15V R_L = 5k

Figure 2. LT1360

The Solution

LTC's new family of voltage feedback amplifiers adjusts the frequency response of the op amp to maintain adequate phase margin regardless of the capacitive load thus, the amplifiers cannot oscillate. These C-Load amplifiers are great in systems where the load is not fixed or is ill-defined. Examples include driving coaxial cables that

C-Load is a trademark of Linear Technology Corporation

may or may not be terminated, driving twisted-pair transmission lines, and buffering the inputs of sampling A/D converters that present time varying impedances.

Table 1 lists LTC's *unconditionally stable* voltage feedback C-Load amplifiers. Table 2 lists other voltage feedback C-Load amplifiers that are stable with loads up to 10,000pF. Figure 3 shows overshoot as a function of capacitive load being driven for a wide variety of LTC op amps. Note that the unconditionally stable amplifiers (LT1355, LT1358 and LT1363) have the greatest overshoot for C_L = 10nF. Overshoot actually declines as C_L is increased beyond 10nF.

Table 1. Unity-Gain Stable C-Load Amplifiers Stable with All Capacitive Loads

Singles	Duals	Quads	GBW (MHz)	I_S/Amp (mA)
LT1200	LT1201	LT1202	11	1
LT1220	—	—	45	8
LT1224	LT1208	LT1209	45	7
LT1354	LT1355	LT1356	12	1
LT1357	LT1358	LT1359	25	2
LT1360	LT1361	LT1362	50	4
LT1363	LT1364	LT1365	70	6

Table 2. Unity-Gain Stable C-Load Amplifiers Stable with $C_L \leq$ 10,000pF

Singles	Duals	Quads	GBW (MHz)	I_S/Amp (mA)
LT1012	—	—	0.6	0.4
—	LT1112	LT1114	0.65	0.32
LT1097	—	—	0.7	0.35
—	LT1457	—	2	1.6

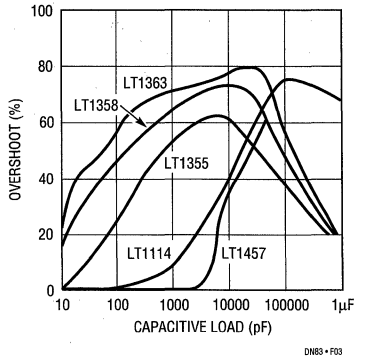


Figure 3. Overshoot vs Capacitive Load

All LTC op amps with adjustable bandwidth can be stabilized for a range of capacitive loads. The bandwidth of current feedback amplifiers is set by the external feedback resistor. Graphs which allow selection of the proper feedback resistor for C_L values to 10,000pF appear in the data sheets of most LTC current feedback amplifiers. As an example, Figure 4 shows the LT1206, a 60MHz current feedback amplifier with 250mA output current, driving loads of 1000pF and 10,000pF while remaining stable.

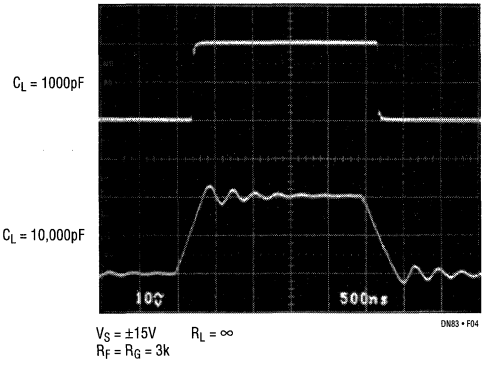


Figure 4. LT1206

Conclusions

Linear Technology has developed families of medium and high speed amplifiers which are much easier to apply than their predecessors. Stable operation with capacitive loads can be achieved without critical external components or loss of output drive. Amplifiers which are stable with any capacitive load are ideal for applications where the load is not well defined. These amplifiers can simplify even low frequency designs by insuring stability under all conditions of loading. For more information on C-Load op amps see the February 1994 issue of *Linear Technology* Magazine.

For literature on our Operational Amplifiers, call **1-800-4-LINEAR**. For applications help, call (408) 432-1900, Ext. 456

LINEAR TECHNOLOGY

DESIGN NOTES

Source Resistance Induced Distortion in Op Amps

Design Note 84

William H. Gross

Introduction

Almost all op amp data sheets have Typical Characteristic Curves that show amplifier total harmonic distortion (THD) as a function of frequency. These curves usually show various gains and output levels but almost always the input source resistance is low, typically 50Ω. In some applications, such as active filters, the source impedance will be much larger. If the input impedance of the op amp is nonlinear with voltage, the resulting distortion will be significantly higher than the values indicated in the data sheet.

Test Circuit

It is quite easy to evaluate source resistance induced distortion. Connect the amplifier as a unity-gain buffer operating on ±15V supplies. Feed a low distortion $20V_{P-P}$ signal to the noninverting input through a source resistor and measure the output signal distortion. The setup is shown in Figure 1. The readings at 1kHz and 10kHz were recorded for various values of source resistance from 100Ω to 100k. The measured results for several op amps are plotted in Figures 2 and 3.

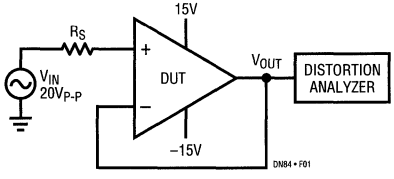


Figure 1

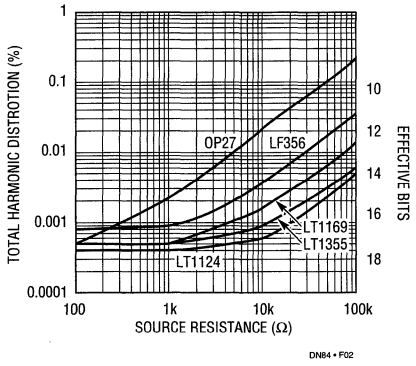


Figure 2. 1kHz Distortion vs Source Resistance

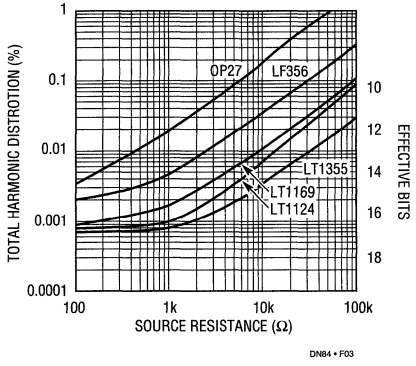


Figure 3. 10kHz Distortion vs Source Resistance

Results

Unfortunately there is no easy way to predict which amplifiers will have the lowest source resistance induced distortion from the data sheets. There are two main causes of the distortion: nonlinear input resistance and nonlinear input capacitance. At first thought, one would not expect the small input capacitance of an op amp to cause distortion at a few kHz. But a 10k source is loaded 0.01% by 1pF at 1.6kHz! Therefore a change in input capacitance of 1pF will cause measurable distortion at 1kHz. For lowest distortion we want an amplifier with low input capacitance as well as very high (and constant) input resistance.

FET input op amps have the highest input resistance but they also have a significant nonlinear input capacitance. The LF356 is a typical FET input op amp; the distortion is 5 to 20 times worse with a 10k source compared with a low source resistance. The LT1169 is a new dual FET input op amp with very low input capacitance (1.5pF) and therefore has about three times lower distortion than the LF356.

The OP27 is a popular high speed precision op amp that has very low distortion when driven from a 50Ω source. Unfortunately the input bias current cancellation circuit works well only at very low frequencies; at 1kHz the input resistance is very nonlinear. The distortion from the OP27 is 50 times worse with a 10k source than with a 100Ω source. The LT1124 is a dual low noise precision op amp that uses a different input bias current cancellation circuit. The LT1124 has the least source resistance induced distortion at 1kH of any of the op amps tested. The LT1355 is a member of a new family of low power, high slew rate op amps that have outstanding high frequency performance. The LT1355 has the least source resistance induced distortion at 10kHz of any op amp tested.

Figure 4 shows a 20kHz Butterworth active filter as might be used for anti-aliasing or band limiting in a data acquisition system. Figure 5 shows the frequency response of the circuit. Note that for signals well below the cutoff frequency, the capacitors have no effect and the op amp sees a 6.2k source resistance. Distortion was measured with several op amps in the circuit to confirm the data shown in Figures 2 and 3. Table 1 shows the results of the best op amps.

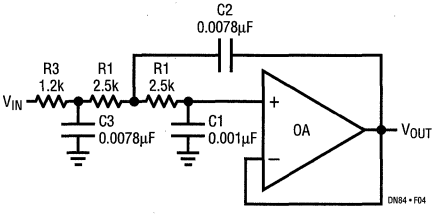


Figure 4

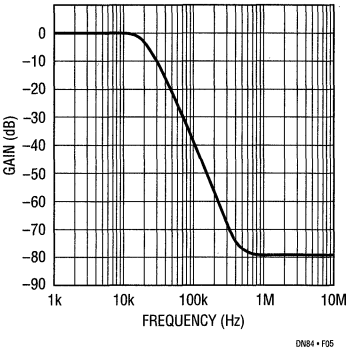


Figure 5. Filter Frequency Response

Table 1. Filter Distortion

Amplifier	100Hz	1kHz	2kHz	5kHz	10kHz
LT1124	0.0004%	0.0005%	0.0008%	0.0021%	0.0090%
LT1355	0.0005%	0.0006%	0.0010%	0.0035%	0.0052%
LT1169	0.0005%	0.0012%	0.0024%	0.0080%	0.0100%

Source resistance induced distortion usually limits the dynamic range of unity-gain RC active filters. An interesting high performance alternative is the LTC1063 and LTC1065. These fifth order, switched-capacitor low-pass filters are not only smaller and easier to use, their distortion is less than 0.01% even with 10k source resistance.

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LINEAR TECHNOLOGY

DESIGN NOTES

Interfacing to Apple LocalTalk® Networks

Design Note 85

Robert Reay

LocalTalk Overview

Of the many connection technologies available for linking an AppleTalk® network, LocalTalk is one of the most common because it is designed to connect local work groups using inexpensive and easily configurable plug-and-play cabling. LocalTalk is laid out in a bus topology with all devices joined in a line with no circular connections. LocalTalk conforms to the EIA RS422 electrical standard to provide a balanced differential voltage signal transmitting at 230.4kbs over a maximum distance of 300 meters with up to 32 devices connected to a twisted-pair network. The balanced configuration provides good isolation from ground noise currents and is not susceptible to fluctuating potentials between system grounds or common-mode electromagnetic interference (EMI).

LTC1323

The original LocalTalk hardware design uses an AM26LS32 chip for the receivers and an AM26LS30 chip for the drivers of a LocalTalk port. The drawback of the design is that it requires two chips per port and an external –5V supply. The bipolar chips also draw large supply currents, making them undesirable for battery-powered applications. A better solution is to use the LTC1323CS24 which provides a complete low power serial I/O interface while generating it's own –5V supply as shown in Figure 1.

The LTC1323 uses the differential driver output stage of Figure 2. The driver swings between ground and V_{CC} when a differential LocalTalk load is connected between TXD^+ and TXD^- while meeting the EIA RS422 differential voltage swing requirement of ±2.0V into 100Ω. When a single-ended load is connected from TXD^+ to ground or TXD^- to ground, the driver will swing between V_{EE} and V_{CC} while meeting the EIA 562 voltage swing requirement of ±3.7V into 3kΩ. Because the differential LocalTalk load requires a large current drive, the charge pump that generates V_{EE} would be unreasonably large if the driver were to swing to V_{EE} with a differential load. By limiting the current flowing into V_{EE} to 15mA, the charge pump can easily be integrated into the chip.

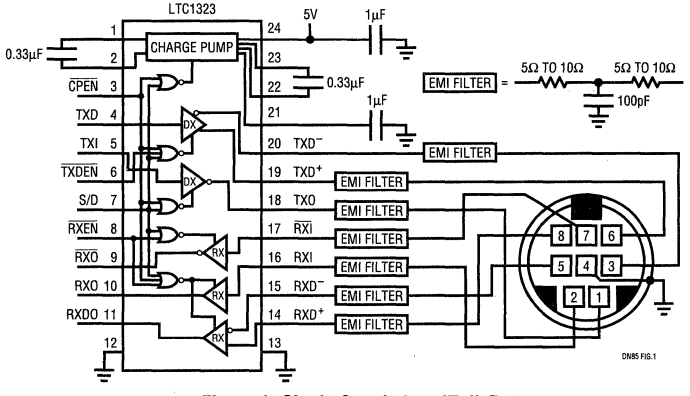

Figure 1. Single Supply LocalTalk Port

AppleTalk and LocalTalk are registered trademarks of Apple Computer, Inc.

For applications where the single-ended control signals are not required, such as PhoneNet®, the LTC1323CS16 can be used as shown in Figure 3. The differential driver is still able to drive a single-ended load to V_{EE} when not connected to a LocalTalk network.

LTC491

For PhoneNet-type applications where the differential driver is not required to drive a single-ended load below ground, the LTC491 can be used as shown in Figure 4. Only RS485 drivers will work in this application. RS422 drivers will not work because they load the cable when the chip power is removed.

EMI Filter

Most LocalTalk applications use an electromagnetic interference (EMI) filter consisting of a resistor-capacitor T network between each driver and receiver and the connector (Figure 5). Unfortunately, the resistors significantly attenuate the driver's signal applied to the cable. Because the LTC1323 and LTC491 are single supply drivers, the resistor values should be reduced to 5Ω to 10Ω to insure enough voltage swing on the cable. In most applications, removing the resistors completely does not cause an increase in EMI as long as a shielded connector and cable are used. With the resistors removed, the only DC load becomes the primary of the LocalTalk transformer. This will increase the DC standby current when the drivers are active, but does not adversely affect the drivers because they can handle a direct short circuit indefinitely. For maximum swing and EMI immunity, a ferrite bead and capacitor could be used.

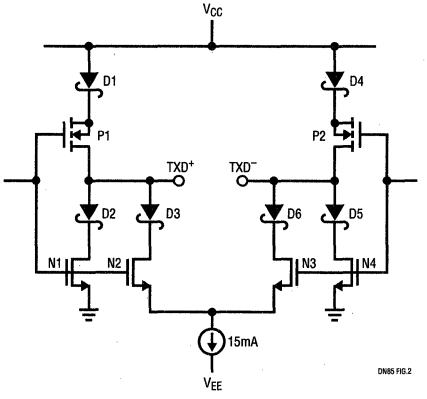

Figure 2. LTC1323 Differential Drive Output Stage

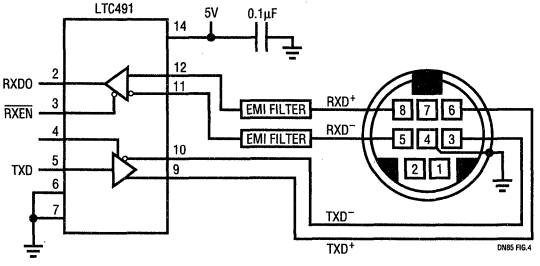

Figure 4. PhoneNet Application

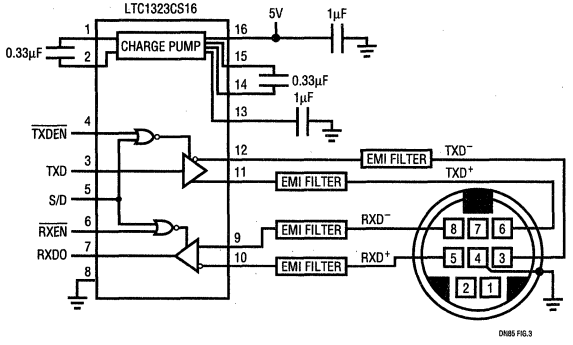

Figure 3. PhoneNet Application

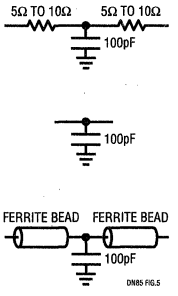

Figure 5. EMI Filters

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LINEAR TECHNOLOGY

DESIGN NOTES

Ultra-Low Power, High Efficiency DC/DC Converter Operates Outside the Audio Band – Design Note 86

Mitchell Lee

Portable communications products are densely packed with signal processing, microprocessor, radio frequency, and audio circuits. Digital clock noise must be eliminated not only from the audio sections, but also from the antenna which, by the very nature of the product, is located only inches from active circuitry. If a switching regulator is used in the power supply, it becomes another source of noise. The LTC1174 step-down converter is designed specifically to eliminate noise at audio frequencies while maintaining high efficiency at low output currents.

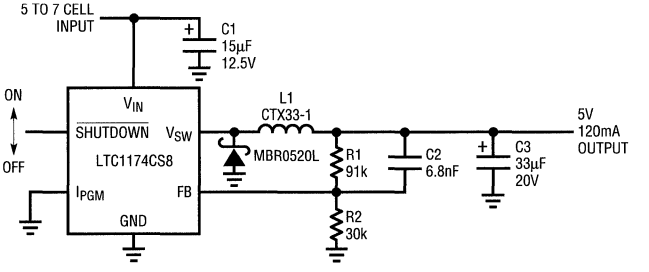
Figure 1 shows an all surface mount solution for a 5V, 120mA output derived from 5 to 7 NiCd or NiMH cells. Small input and output capacitors that are capable of handling the necessary ripple currents help conserve space. In applications where shutdown is desired this feature is available (otherwise short this pin to V_{IN}).

The LTC1174's internal switch, connected between V_{IN} and V_{SW}, is current controlled at a peak of approximately 340mA. Low peak switch current is one of the key features that allows the LTC1174 to minimize system noise compared to other chips which carry significantly higher peak currents, easing shielding and filtering requirements and decreasing component stresses. Output currents of up to 450mA are possible with this device by connecting the I_{PGM} pin to V_{IN}. This increases the peak current to 600mA, allowing for a high average output current.

To conserve power and maintain high efficiency at light loads, the LTC1174 uses Burst Mode™ operation. Unfortunately, this control scheme can also generate audio frequency noise at both light and heavy loads. In addition to electrical noise, acoustical noise can emanate from capacitors and coils under these conditions. A feed-forward capacitor (C2) shifts the noise spectrum up and out of the audio band, eliminating these problems. C2 also reduces peak-to-peak output ripple to approximately 30mV over the entire load range.

A toroidal surface mount inductor (L1) is chosen for its excellent self-shielding properties. Open magnetic structures such as drum and rod cores are to be avoided since they inject high flux levels into their surroundings. This can become a major source of noise in any converter circuit.

Burst Mode™ is a trademark of Linear Technology Corporation.



C1: PANASONIC SP SERIES (201) 348-4630
C3: AVX TAJ SERIES (803) 956-0690
L1: COILTRONICS OCTAPAK (407) 241-7876

Figure 1. Low Noise, High Efficiency Step-Down Regulator for Personal Communications Devices

The interactions of load current, efficiency, and operating frequency are shown in Figure 2. High efficiency is maintained at even low current levels, dropping below 70% at around 800µA. No load supply current is less than 200µA, dropping to approximately 1µA in shutdown. The operating frequency rises above the telephony bandwidth of 3kHz at a load of 1.2mA. Most products draw milliampere range load currents only in standby with the audio circuits squelched, when low frequency noise is not an issue.

The frequency curve depicted in Figure 2 was measured with a spectrum analyzer, not a counter. This ensures that the lowest frequency noise peak is observed rather than a faster switching frequency component. Any tendency to generate subharmonic noise is quickly exposed using this measurement method.

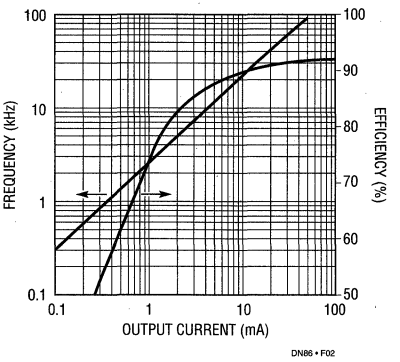


Figure 2. Parameter Interaction

A spectrum analysis of noise from 100kHz to 10MHz is shown in Figure 3. The fundamental switching component in this test was approximately 85kHz, and the second harmonic shows up at twice that frequency. It measures approximately $3mV_{RMS}$. Harmonics of the 85kHz fundamental disappear into a 10µV "mud" between 1MHz and 2MHz. Noise in the critical 455kHz region ranges from 10µV to 300µV, depending on operating frequency. At 10.7MHz, an important and sensitive intermediate frequency, the noise is broadband and well below $10\mu V_{RMS}$.

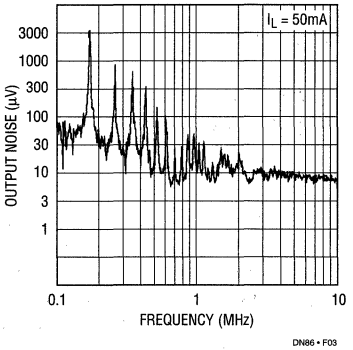
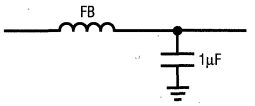


Figure 3. Noise in the 100kHz to 10MHz Band

Further noise reduction is possible by adding an output filter (see Figure 4). A small surface mount ferrite bead is placed in series with the 5V output, close to the LTC1174 and bypassed by a 1µF surface mount ceramic capacitor. Noise attenuation at 10MHz exceeds 20dB.



FB: DALE ILB-1206 31 25% (605) 665-9301
1µF: AVX 12063G105ZAT (803) 448-9411 DN86 • F04

Figure 4. An Effective Filter for Attenuating Noise Components Above 1MHz

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LINEAR TECHNOLOGY

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DESIGN NOTES

Fast Regulator Paces High Performance Processors

Design Note 87

Mitchell Lee and Craig Varga

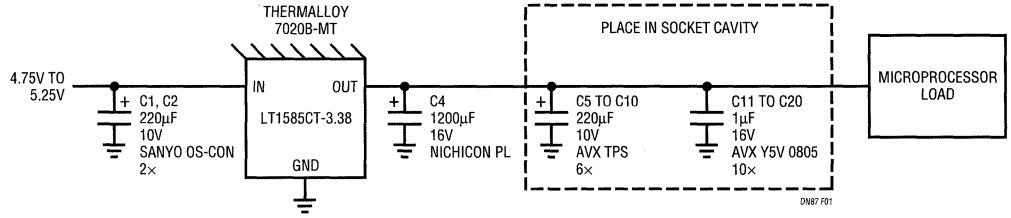
New high performance microprocessors require a fresh look at power supply transient response. Pentium™ processors, for example, have current demands that go from a low idle mode of 200mA to a full load current of 4A in 20ns. A transition of the same magnitude occurs as the processor reenters its power saving mode. In addition, the overall supply tolerances have been narrowed significantly from the traditional ±5% for 5V supplies and include transient conditions. When all possible DC error terms are accounted for, the transient response of the power supply when subject to the load step mentioned above must be within ±46mV!

To address this problem Linear Technology has developed the LT1585 linear regulator. It features 1% initial accuracy, excellent temperature drift and load regulation, and virtually perfect line regulation. Complementing superb DC characteristics, the LT1585 exhibits extremely fast response to transients. The regulator is offered as an adjustable regulator requiring two resistors to set the operating point, as well as fixed versions which have been trimmed and optimized for 3.3V, 3.38V, 3.45V, and 3.6V outputs. Fixed versions are fully specified for worst-case DC error bounds; in adjustable designs the effects of the external voltage-setting resistors must be taken into account.

Transient response is affected by more than the regulator itself. Stray inductances in the layout and bypass capacitors, as well as capacitor ESR dominate the response during the first 400ns of transient. Figure 1 shows a bypassing scheme developed to meet all of the requirements for the Intel P54C-VR microprocessor. Multiple capacitors are required to reduce the total ESR and ESL, which affect the transient response.

Input capacitors C1 and C2 function primarily to decouple load transients from the 5V logic supply. The values used here are optimized for a typical 5V desktop computer "silver box" power supply input. C5 to C10 provide bulk capacitance at low ESR and ESL, and C11 to C20 keep the ESR and ESL low at high (>100kHz) frequencies. C4 is a damper and it minimizes ringing during settling.

A good place to locate the surface mount decoupling components is in the center of the Pentium socket cavity on the top side of the circuit board. Consider using concentric rings of power and ground plane on the top layer of the board within the socket center for bussing the



AVX CORPORATION: (803) 448-9411
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SANYO VIDEO COMPONENTS (USA) CORPORATION: (619) 661-6322
THERMALLOY INCORPORATED: (214) 243-4321
FOR CORRECT OPERATION OF MICROPROCESSOR, DO NOT SUBSTITUTE COMPONENTS

Figure 1. Recommended Bypassing Scheme for Correct Transient Response

capacitors together. Tie the main power and ground planes to these cavity planes with a minimum of two vias per capacitor. This will minimize parasitic inductance. The regulator and damper capacitor should be located close to (<1") the microprocessor socket to minimize circuit trace inductance.

Verifying the regulator and microprocessor layout can be accomplished with a controlled load such as the Power Validator™ manufactured by Intel. This device plugs directly into the microprocessor socket and simulates worst-case load transients conditions.

An oscilloscope photograph of the LT1585's response to a worst-case 200mA to 4A load step is shown in Figure 2. Trace C is the load current step, which is essentially flat at 4A with a 20ns rise time. Trace A is the output settling response at 20mV per division. Cursor trace B marks −46mV relative to the initial output voltage. At the onset of load current, the microprocessor socket voltage dips to −38mV as a result of inductive effects in the board and capacitors, and the ESR of the capacitors. The inductive effects persist for approximately 400ns. For the next 3µs the output droops as load current drains the bypass capacitors. The trend then reverses as the LT1585 catches up with the load demand, and the output settles after approximately 50µs.

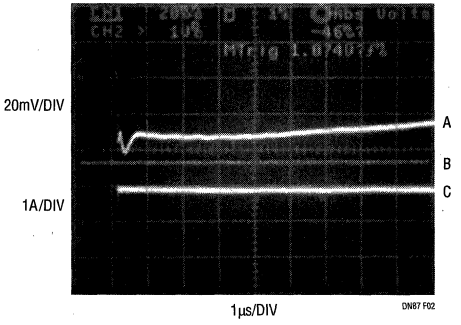

Figure 2. Transient Response at Onset of 4A Load Current Step

Running 4A with a 1.7V drop, the regulator dissipates 6.8W. The heat sink shown in Figure 1, with 100ft/min air flow is adequate for worst-case operating conditions.

The adjustable version of the LT1585 makes it relatively easy to accommodate multiple mircoprocessor power supply voltage specifications (see Figure 3). To retain the tight tolerance of the LT1585 internal reference, 0.5% adjustment resistors are recommended. R1 is sized to carry approximately 10mA idling current (≤124Ω), and R2 is calculated from:

$$R2 = \frac{V_O - V_{REF}}{\frac{V_{REF}}{R1} + I_{ADJ}}$$

where:

I_{ADJ} = 60µA and V_{REF} = 1.250V

Figure 3 shows the connections for R1 and R2. Note that C5 to C10 are reduced in value from Figure 1 without compromising the transient response. The addition of C3 makes this possible and also eliminates the need for C4.

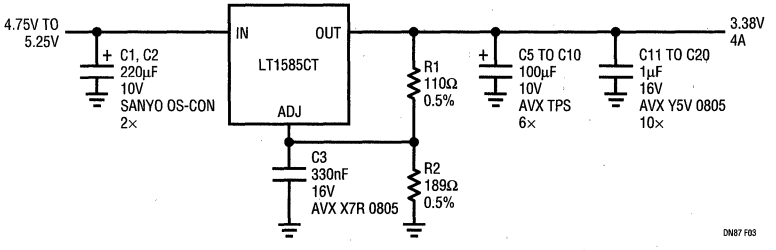

Figure 3. Recommended Adjustable Circuit

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LINEAR TECHNOLOGY

DESIGN NOTES

New 500ksps and 600ksps ADCs Match Needs of High Speed Applications – Design Note 88

Kevin R. Hoskins

Introduction

Combining high speed analog-to-digital conversion with low power dissipation, the 500ksps LTC®1278 and 600ksps LTC1279 12-bit ADCs solve major challenges confronting designers of high speed systems: conversion performance, power dissipation, circuit board real estate, complexity, and cost. Applications for the LTC1278/LTC1279 include telecom, communication, PC data acquisition board, and high speed and multiplexed data acquisition systems. In addition to requiring no external references, crystals, or clocks the LTC1278/LTC1279 offer system designers the following significant system-enhancing improvements:

- Power Shutdown: 5mW
- Wakes Up in a Scant 300ns
- Single 5V or ±5V Supply Voltage Operation
- Low Power Dissipation: 150mW (Max), 75mW (Typ)
- Small 24-Pin SO or 24-Pin Narrow DIP Packages

The LTC1278/LTC1279's DC performance includes ±1LSB INL and DNL, no missing codes, and an internal voltage reference with a full-scale drift of only 25ppm/°C.

The AC performance includes 70dB (Min) SINAD, –78dB (Max) THD, and –82dB (Max) spurious-free dynamic range. These specifications were measured at f_S = 500ksps (LTC1278) or f_S = 600ksps (LTC1279), f_{IN} = 100kHz, and are guaranteed over the operating temperature range. The plot of effective-number-of-bits (ENOB) shown in Figure 1 clearly indicates that the LTC1278/LTC1279 can accurately sample signals that contain spectral energy beyond the Nyquist frequency.

Newest High Speed ADC Family Members

The LTC1278/LTC1279 are self-contained ADC systems composed of a fast capacitively-based charge redistribution Successive Approximation Register (SAR) sampling ADC, internal reference, power shutdown, and internally generated and synchronized conversion clock. The digital interface's flexibility eases connection to external latches, FIFOs, and DSPs. Table 1 shows more members of the high speed 12-bit ADC family.

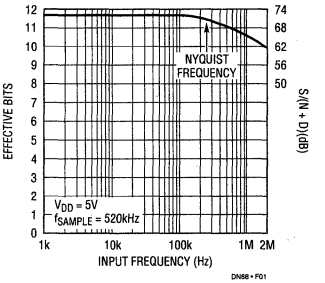

Figure 1. The LTC1278 Can Accurately Digitize Input Signals Up to the Nyquist Frequency and Beyond

Table 1. LTC's High Speed ADC Family Includes 5V and 3V Devices

Device	Sampling Frequency	S/(N + D) @ Nyquist	Input Range	Power Supply	Power Dissipation
LTC1272	250kHz	65dB	0V to 5V	5V	75mW
LTC1273	300kHz	70dB	0V to 5V	5V	75mW
LTC1275	300kHz	70dB	±2.5V	±5V	75mW
LTC1276	300kHz	70dB	±5V	±5V	75mW
LTC1278	**500kHz**	**70dB**	**0V to 5V or ±2.5V**	**5V or ±5V**	**75mW 5mW***
LTC1279	**600kHz**	**70dB**	**0V to 5V or ±2.5**	**5V or ±5V**	**75mW 5mW***
LTC1282	140kHz	68dB	0V to 2.5V or ±1.25V	3V or ±3V	12mW

*5mW power shutdown with instant wake-up

The LTC1278/LTC1279 convert input signals in the 0V to 5V or –2.5V to 2.5V ranges at full speed when operating on a 5V or ±5V supply voltage, respectively. The ±2.5V input range complements the new generation of operational amplifiers that operate on ±5V.

Important Applications

The LTC1278's features benefit at least four different application areas: telecom, communication, PC data acquisition boards, and high speed and multiplexed data acquisition.

Telecom digital-data transmission applications such as High-bit-rate Digital Subscriber Line (HDSL) with its high speed T1 data rate benefit from the LTC1278's low power dissipation since these telecom systems usually derive their power from the phone line. While the LTC1278's 500ksps conversion rate easily covers T1 data rates, the LTC1279's 600ksps is ideal for HDSL's faster E1 data rates. Further, these applications use noise and echo cancellation that require excellent dynamic performance from the ADC's sample-and-hold. The LTC1278 satisfies this requirement as indicated by the device's excellent dynamic performance shown in Figure 1.

Communication applications also benefit from the LTC1278/LTC1279's wide input bandwidth and undersampling capability. The application shown in Figure 2 uses the LTC1278 to undersample (at 227.5ksps) a 455kHz I.F. amplitude-modulated by a 5kHz sinewave. Figures 3A and 3B show, respectively, the 455kHz I.F. carrier and the recovered 5kHz sinewave that results from a 12-bit DAC reconstruction.

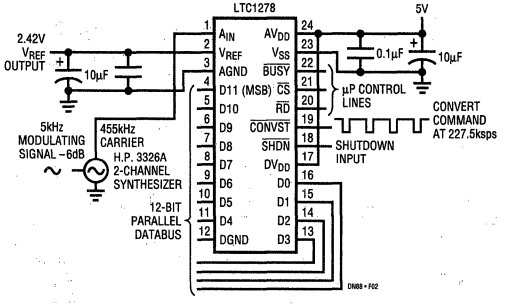

Figure 2. The LTC1278 Undersamples the 455kHz Carrier to Recover the 5kHz Modulating Signal

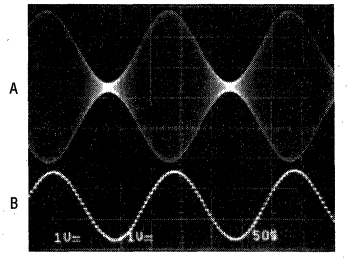

Figure 3. Demodulating an I.F. by Undersampling

Figure 2 also shows that by taking advantage of surface mount devices, this simple configuration occupies only $0.43IN^2$ of circuit board real estate.

PC data acquisition cards are another broad application area. The LTC1278's high sampling rate, simple and complete configuration, small outline package, and low cost make this converter ideal for these applications. Additionally, the LTC1278's synchronized internal conversion clock minimizes conversion noise that results when the conversion clock and the sampling command are not synchronized. This internal clock and sampling synchronization overcomes what, in PC environments, can be a cumbersome task.

Both single channel and multiplexed high speed data acquisition systems benefit from the LTC1278/LTC1279's dynamic conversion performance. The 1.6µs and 1.4µs conversion and 200ns and 180ns S/H acquisition times enable the LTC1278/LTC1279 to convert at 500ksps and 600ksps, respectively. Figure 4 shows a 500ksps 8-channel data acquisition system. The LTC1278's high input impedance eliminates the need for a buffer amplifier between the multiplexer's output and the ADC's input.

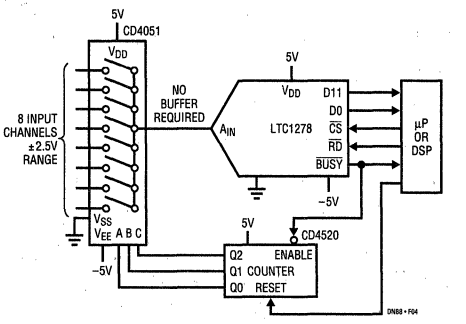

Figure 4. The High Input Impedance of the LTC1278 Allows Multiplexing Without a Buffer Amplifier

Conclusion

The LTC1278/LTC1279's new features simplify, improve, and reduce the cost of high speed data acquisition systems. This makes them the converters of choice for telecom, communication, PC data acquisition board, and high speed and multiplexed data acquisition system designers.

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DESIGN NOTES

Applicatons of the LT1366 Rail-to-Rail Amplifier – Design Note 89

William Jett and Sean Gold

The LT1366 is Linear Technology's first bipolar dual operational amplifier to combine rail-to-rail input and output operation with precision V_{OS} specifications. The LT1366 maintains precision specifications over a wide range of operating conditions. The device will operate with supply voltages as low as 1.8V and is fully specified for 3V, 5V, and ±15V operation. Offset voltage is typically 200µV when operating from a single 5V supply. Open-loop gain, A_{VOL}, is 2 million driving a 2kΩ load. Supply current is typically 375µA per amplifier. The combination of precision specifications and rail-to-rail operation makes the LT1366 a versatile amplifier, suitable for signal processing tasks that demand the widest possible common-mode range.

Precision Low Dropout Regulator

Microprocessors and complex digital circuits frequently specify tight control of power supply characteristics. The circuit shown in Figure 1 provides a precise 3.6V, 1A output from a minimum 3.8V input voltage. The circuit's nominal operating voltage is 4.75V ±5%. The voltage reference and resistor ratios determine output voltage accuracy, while the LT1366's high gain enforces 0.2% line and 0.2% load regulation. Quiescent current is about 1mA and does not change appreciably with supply or load. All components are available in surface mount packages.

The regulator's main loop consists of A1 and a logic level FET, Q1. The output is fed back to the op amp's positive input because of the phase inversion through Q1. The regulator's frequency response is limited by Q1's roll-off and the phase lead introduced by the output capacitor's effective series resistance (ESR). Two pole-zero networks compensate for these effects. The pole formed with R5 and C2 rolls off the gain set with the feedback network, while the pole formed with R7 and C3 rolls off A1's gain directly, which is the dominant influence on settling time. The zeros formed with R6 and C2, and R8 and C3 provide phase boost near the unity-gain crossover, which increases the regulator's phase margin. Although not directly part of the compensation, R9 decouples the op amp's output from the Q1's large gate capacitance.

A second loop provides a foldback current limit. A2 compares the sense voltage across R1 with 50mV referenced to the positive rail. When the sense voltage exceeds the

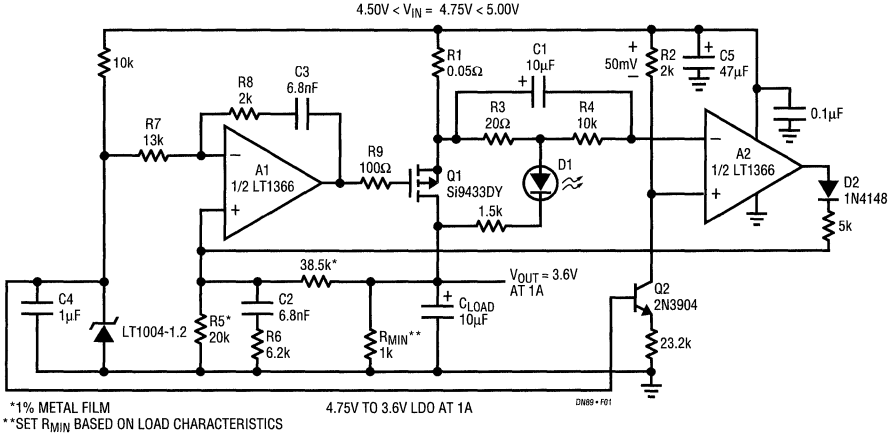

Figure 1. Precision 3.6V, 1A Low Dropout Regulator

reference, A2's output drives Q2's gate positive via A1. In current limit, the output voltage collapses and the current limit LED (D1) turns on causing about 30mV to drop across R3. A2 regulates Q1's drain current so that the deficit between the 50mV reference and the voltage across R3 is made up across the sense resistor. The reduced sense voltage is 20mV, which sets the current limit to about 400mA. As the supply voltage increases, the voltage across R3 increases, and the current limit folds back to a lower level. The current limit loop deactivates when the load current drops below the regulated output current. When the supply turns on rapidly, C1 bypasses the fold back circuit allowing the regulator to start-up into a heavy load.

Q1 does not require a heat sink. When mounted on a type FR4 PC board, Q1 has a thermal resistance of 50°C/W. At 1.4W worst case dissipation, Q1 can operate up to 80°C.

Single Supply, 1kHz, 4th Order Butterworth Filter

The LT1366 is also available as a quad op amp (LT1367), which is used in Figure 2 to form a 4th order Butterworth filter. The filter is a simplified state variable architecture consisting of two cascaded 2nd order sections. Each section uses the 360 degree phase shift around the 2 op amp loop to create a negative summing junction at A1's positive input.[1] The circuit has low sensitivities for center frequency and Q, which are set with the following equations:

$$\omega_0^2 = 1/(R1 \times C1 \times R2 \times C2)$$

where,

$$R1 = 1/(\omega_0 \times Q \times C1) \text{ and } R2 = Q/(\omega_0 \times C2).$$

The DC bias applied to A2 and A4, half supply, is not needed when split supplies are available. The circuit swings rail-to-rail in the passband making it an excellent anti-aliasing filter for A/Ds. The amplitude response is flat to 1kHz then rolls off at 80dB/decade.

Buffering A/D Converters

Figure 3 shows the LT1366 driving an LTC1288 two-channel micropower A/D. The LTC1288 can accommodate voltage references and input signals equal to the supply rails. The sampling nature of this A/D eliminates the need for an external sample-and-hold, but may call for a drive amplifier because of the A/D's 12µs settling requirement. The LT1366's rail-to-rail operation and low input offset voltage make it well suited for low power, low frequency A/D applications. In addition, the op amp's output settles to 1% in response to a 3mA load step through 100pF in less than 1.5µs.

[1] James Hahn, "State Variable Filter Trims Predecessor's Component Count", *Electronics*, April 21, 1982.

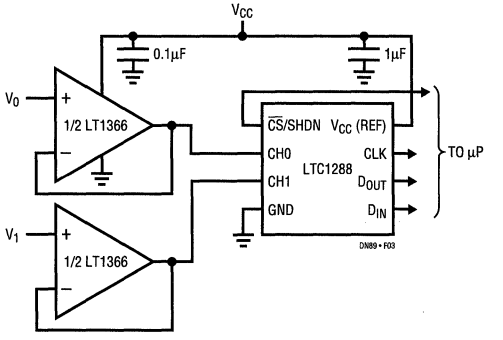

Figure 3. Two-Channel Low Power A/D

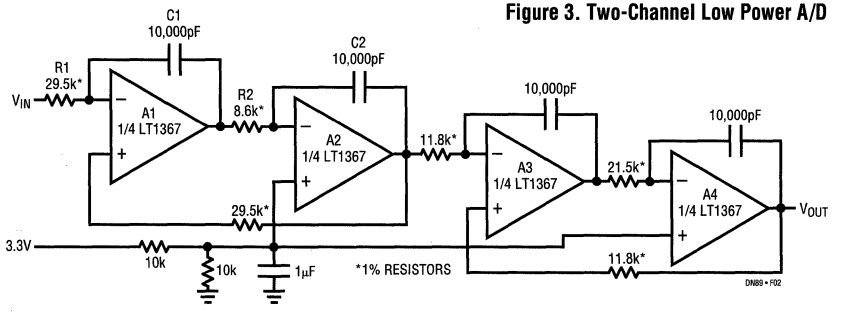

Figure 2. Single Supply Stage Variable Filter Using the LT1367

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LINEAR TECHNOLOGY

DESIGN NOTES

High Efficiency Power Sources for Pentium™ Processors

Design Note 90

Craig Varga

In many applications, particularly portable computers, the efficiency of power conversion is critical both from the standpoint of battery life and thermal management. Desktop machines may also benefit from higher efficiency, particularly a "green PC." While linear regulators can offer low cost and high performance solutions, they can only offer 67% efficiency in 5V to 3.3V applications. Switching regulators are more efficient and minimize or even eliminate the need for heat sinks at a higher cost for the components. Efficiencies around 90% are routinely obtained with Linear Technology's best regulator designs (see Figure 2). The LTC1148 based circuit (Figure 1) meets the requirements of the P54-VR specification for output voltage transient response with the indicated decoupling network.

Selection of Input Source

Several options exist as to where to derive raw power for the regulator input. In most desktop systems a large amount of 5V power is available. Also, there is usually a reasonable source of 12V at hand. The 5V supply will most likely have the highest power output capability since it is called upon to power the bulk of the system logic. This logic can be sensitive to voltage changes outside of ±5%.

When the processor draws large transient currents, the 5V supply will be perturbed. In all "buck" type switching regulators there is an inductor in the path between the raw input supply and the load. This has the effect of limiting the rise time of the input currents and minimizing the disturbance to the 5V supply. However, the typical cheap off-line "brick" supply has terrible transient response, and the 5V

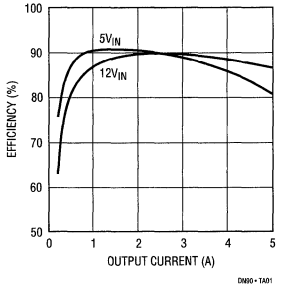


Figure 2. Efficiency vs Load

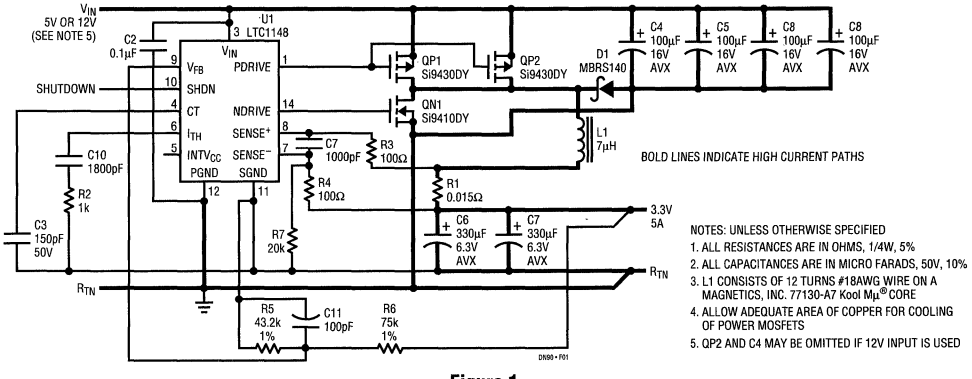


Figure 1.

supply may still be disturbed enough to cause logic problems. This is especially true as the load currents rise to the levels expected in multiprocessor systems.

If this is the case, using the 12V supply may prove advantageous. Since the 12V supply is not directly regulated, nothing that is terribly sensitive to voltage level is normally powered off the 12V bus. Moreover, with switching regulators, as a first order approximation, as the supply voltage rises the input current drops. As such, even though the input power is nominally the same whether running from a 5V or 12V supply, the current requirement is much lower if 12V is utilized for the input source.

The downside of 12V operation is lower light load efficiency than 5V operation. The efficiency with a 5V input powering a 3.3V switcher is likely to be several percentage points better than at 12V due to a reduction in switching losses. Every situation is somewhat different and a thorough analysis of the trade-offs must be undertaken to optimize the design. The schematic shown in Figure 1 offers the option to run from several supply choices. Each circuit was optimized for the specified input voltage, but will function well over a fairly wide range of supply voltages.

Transient Response Considerations

As with a linear regulator, the first several microseconds of a transient are out of the hands of the regulator and dropped squarely in the lap of the decoupling capacitor network. In the case of the switcher, the ultimate response of the regulator will be quite slow compared to a linear regulator. In the circuits shown, the approximate time required to ramp the regulator current to equal the high load condition is 11µs, about 2.4 time that of an LT1585 high speed linear regulator in the same application. This means in layman's terms, that the LT1585 linear regulator requires less bulk capacitance than the LTC1148 switcher solution.

Circuit Operation

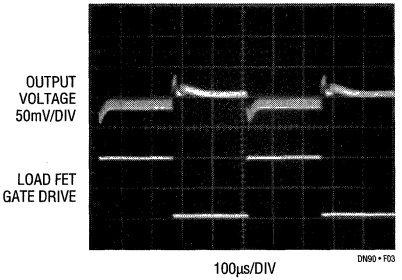
Figure 1 is a schematic of the two regulators. For the 12V input, omit QP2 and C4. The design is a standard synchronous buck regulator that is discussed in detail in several Linear Technology Application Notes as well as the LTC1148 data sheet. Since the required output voltage is not the standard 3.3V, which is available factory set, an adjustable regulator is used. R5 and R6 set the output voltage to the desired level, in this case 3.38V. R7 is used to inhibit Burst Mode™ operation at light loads. If the system were permitted to operate in Burst Mode, the output voltage would rise by about 50mV at low load currents. If added low load efficiency is desired and the slightly higher low load output voltage can be tolerated, this resistor can be omitted.

To meet the transient requirements of the P54-VR, a fairly large amount of capacitance is needed beyond what is required to make the regulator function correctly. A viable decoupling scheme is to use 10 each, 1µF surface mount ceramics and 7 each, 220µF, 10V surface mount tantalums at the processor socket. In addition to the socket decoupling, two pieces of a 330µF, 6.3V surface mount tantalums are required at the power supply.

The input capacitors were selected for their ability to handle the input ripple current. At a 5A load current this is a little over 4A with a 5V input and 2.6A for a 12V input. The capacitors are rated at slightly over 1A each at 85°C. If the input can be switched on very rapidly, the input capacitor voltage rating should be at least two times the supply voltage to prevent dV/dt failures.

By running the operating frequency at 150kHz, the small inductor used is sufficient. Also, since the design is synchronous, the ripple current may be permitted to get quite high without causing any problems for the regulator control loop. This would not be true in a non-synchronous design. A major advantage of high ripple current is the regulator's ability to ramp output current rapidly. The rate of rise of output current is directly proportional to input/output differential and inversely proportional to the inductor value. Using a small inductor aids in achieving fast response to transients.

5V Input, 0.2A to 4A Load Step



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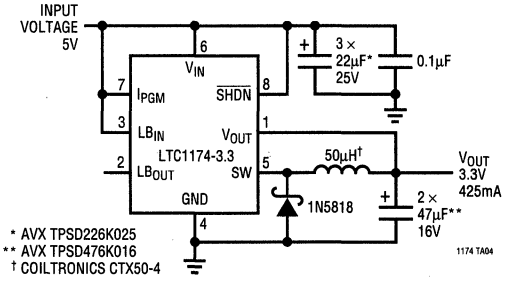
LINEAR TECHNOLOGY

DESIGN NOTES

5V to 3.3V Circuit Collection – Design Note 91

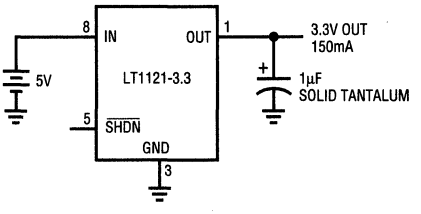
Richard Markell and Craig Varga

High Efficiency 3.3V Regulator



The LTC®1174-3.3 current mode DC/DC converter provides efficiencies better than 90% over a wide load current range while requiring only 1µA in Shutdown.

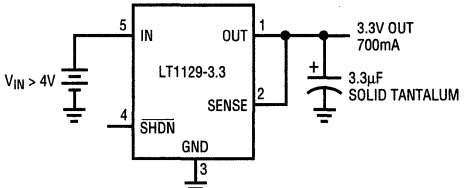
3.3V Battery-Powered Supply with Shutdown



V_{SHDN} (PIN 5)	OUTPUT
< 0.25	OFF
> 2.8	ON
NC	ON

The LT1121-3.3 low dropout linear regulator provides up to 150mA output current with 30µA quiescent current.

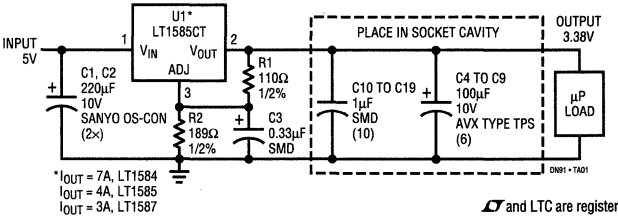
3.3V Supply with Shutdown



V_{SHDN} (PIN 4)	OUTPUT
< 0.25	OFF
> 2.8	ON
NC	ON

The LT1129-3.3 low dropout linear regulator provides more output current (to 700mA) with only a slight increase in quiescent current (50µA).

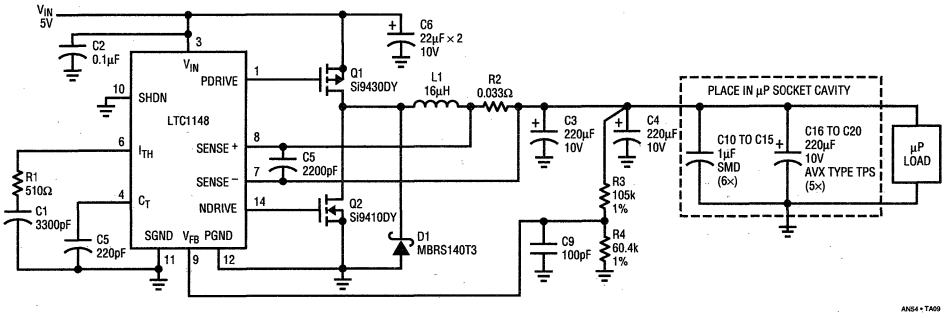
LT1585 Linear Regulator Optimized for Desktop Pentium™ Processor Applications



Linear regulator circuits provide simple solutions with superior transient performance for desktop resident Pentium processor-based systems

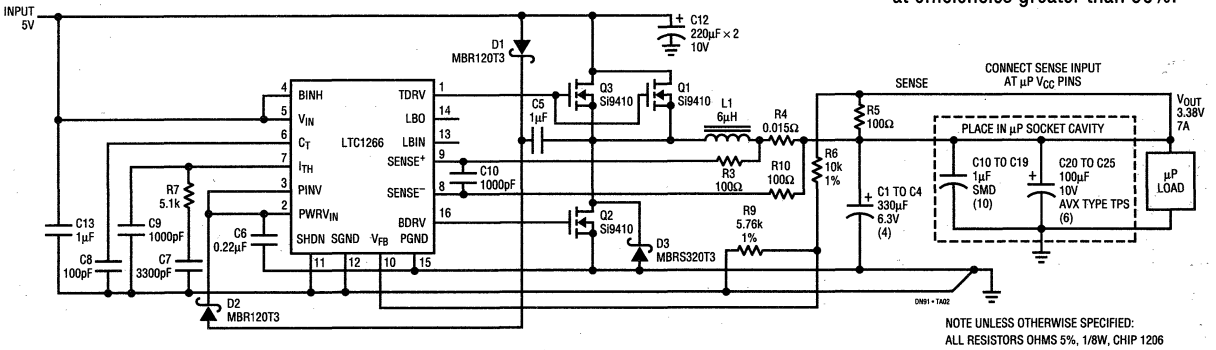
Pentium is a trademark of Intel Corporation

LTC1148 5V to 3.38V Pentium Power Solution 3.5A Output Current



This circuit achieves >90% efficiency using an LTC1148 synchronous switching regulator which consumes a mere 180µA quiescent current.

LTC1266 Switching Regulator Converts 5V to 3.38V at 7A for Pentium and Other High Speed µPs



The LTC1266 drives N-channel MOSFETs directly and provides 7A output current at efficiencies greater than 90%.

NOTE UNLESS OTHERWISE SPECIFIED:
ALL RESISTORS OHMS 5%, 1/8W, CHIP 1206
ALL CAPACITORS CERAMIC, 10%, CHIP 1206
ALL POLARIZED CAPACITORS TANTALUM, 20% SMT, LOW ESR, AVX TPS-SERIES

LINEAR TECHNOLOGY

DESIGN NOTES

An Adjustable Video Cable Equalizer Using The LT1256

Design Note 92

Frank Cox

This design note presents a voltage controlled cable equalizer based on the LT1256 video fader. The circuit features ease of adjustment, simplicity and the capability for remote control. The amount of equalization can be adjusted continuously from the maximum allowed by the passive components to none at all. While the example shows video, this high performance equalizer can be used in any system using long runs of coaxial cable or twisted pair to transmit analog signals.

A voltage or current controlled equalizer is essential in systems which automatically set cable compensation. In systems where cable equalization is set manually, a voltage controlled equalizer is still preferred as it does not require routing the signal path to the control. Instead, only a DC control voltage passes from the front panel to the equalizer.

Automatic equalization is possible for properly characterized video cables. Maximum equalization is set to coincide with the maximum length of cable expected; the equalizer is controlled by a servo loop. One method of generating the necessary control voltage is to sample the color burst amplitude and compare this with a reference voltage using a summing integrator. Since the frequency roll-off of the cable is known (and fixed for a given cable) only the amount of equalization needs to be adjusted.

In many applications color video is transmitted down long runs of coaxial or twisted-pair cable. Losses in the cable increase with signal frequency and cable length. The type of cable will determine the rate of high frequency loss. Color information in NTSC video is contained primarily in the high frequency portion of the spectrum. Besides causing a loss of detail in the picture, excessive high frequency loss will make reliable decoding of the composite color signal more difficult or impossible. Most commercial distribution amplifiers have provisions for equalizing the cable losses, but many times these units come at a high cost.

Figure 1 is a complete schematic of the cable equalizer. The LT1256 (U1) is a two input, one output 40MHz current feedback amplifier with a linear control circuit that sets the

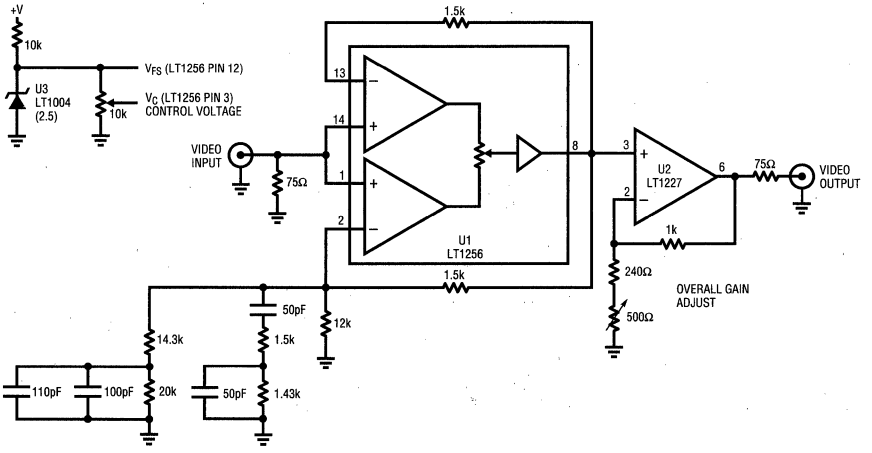


Figure 1. LT1256 Cable Equalizer

DN92 • F01

amount each input contributes to the output. One amplifier (input pins 13 and 14) of the LT1256 is configured as a gain of one with no frequency equalization. The other amplifier (input pins 1 and 2) has frequency equalizing components in parallel with the 12k gain resistor. The equalization components for this demonstration circuit where chosen empirically as no data on the cable was available. As the control voltage is varied the output contains a summation of the two separate input channels; one containing the input video with no compensation and the other with the maximum depth of equalization. By adjusting this mix it is possible to smoothly adjust the equalizer depth. An additional amplifier (U2, LT1227) is used to set the overall gain. Two amplifiers were used here to make setting the gain a single adjustment, but in a production circuit the LT1256 can be configured to have the necessary gain and the whole function can be done with one chip.

In this demonstration a spool of over 250 feet[1] of good quality coax was used to transmit NTSC video. The LT1256 equalizer is placed at the receive end[2] and is adjusted with the use of a test pattern and a video waveform monitor (or oscilloscope). Figure 2 shows the video after transiting the cable and without equalization. Three standard video test signals were used; the mulitburst, the 2T and the 12.5T. The 2T and the 12.5T test signals are sensitive indicators of phase and amplitude distortion in the video signal. The effect of the equalization circuit is shown in Figure 3. The resultant frequency response is flat and the time domain behavior is also excellent. Network analyzer plots of gain vs frequency for various settings of equalizer depth are given in Figure 4.

[1] It should also be noted that the LT1256 can be used to equalize much longer coaxial and twisted-pair cable than the one in this demonstration.

[2] Since the equalizer provides gains at high frequencies there is a possibility of overload if the circuit is placed at the transmit end of the cable rather than the receive end of the cable, especially if there is a need for a great deal of equalization. For example, 2000 feet of Belden 8281 precision video cable will have about 11dB of loss at 5MHz. This requires the driving amp to swing 3.5 times normal if the transmit end is boosted to compensate for the cable.

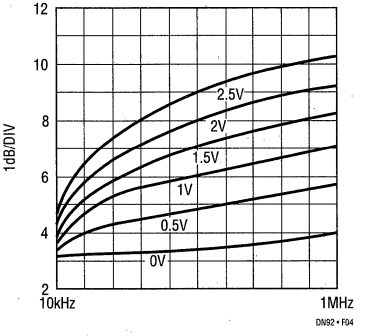


Figure 4. Frequency Response vs Control Voltage

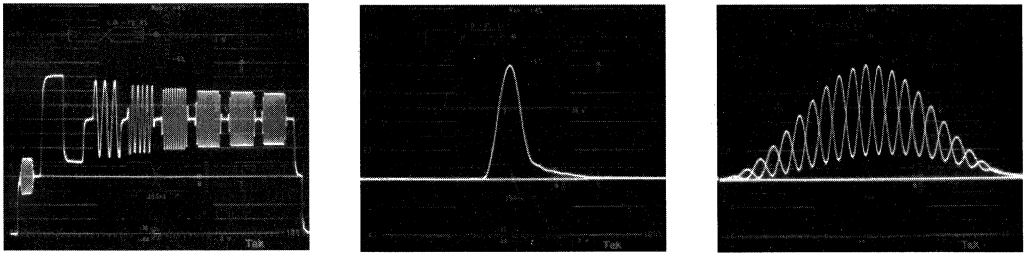


Figure 2. Multiburst, 2T and 12.5T After 250 Feet of Coax

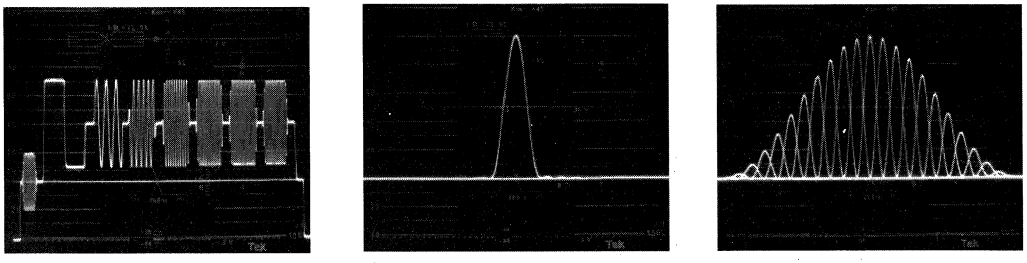


Figure 3. Multiburst, 2T and 12.5T After 250 Feet of Coax and Equalization, Circuit in Fig. 1

LINEAR TECHNOLOGY

DESIGN NOTES

PCMCIA Socket Voltage Switching – Design Note 93

Why Your Portable System Needs SafeSlot™ Protection

Doug La Porte

Introduction

Most portable systems have built-in PCMCIA sockets as the sole means of expansion. The requirements of the PCMCIA specification have led to some confusion among system designers. This Design Note will attempt to lessen the confusion and highlight other practical system issues.

Host power delivery to the PC card socket flows through two paths: the main V_{CC} supply pins and the VPP programming pins. Both supplies are switchable to different voltages to accommodate a wide range of card types. The V_{CC} main card supply must be capable of delivering up to 1A at either 3.3V or 5V. The 1A rating is an absolute maximum derived from the contact rating of 500mA per pin for both V_{CC} pins and assumes that both pins are in good condition and current is shared equally. One of the most stringent actual current requirements is during hard drive spin-up. Present hard drives require 5V at 600mA to 800mA for a short duration during spin-up. Current draw drops to 300mA to 420mA during read and write operations. A low switch resistance on the 3.3V switch is critical to assure that the specified 3.0V minimum is maintained. The VPP supply must source 12V at up to 120mA and 3.3V or 5V at lesser currents. The VPP supply is intended solely for flash memory programming. The 120mA current requirement allows writing to flash devices and simultaneously erasing two other parts as required by many flash drives.

The host PCMCIA socket designer also has several other practical aspects of the design to consider. The exposed socket pins are vulnerable to being shorted by foreign objects such as paper clips. In addition the users will attempt to install damaged cards. In short, once in the hands of the consumer, the designer and manufacturer have little control over use and abuse. To ensure a robust system and a satisfied customer, switch protection features such as current limiting and thermal shutdown are a necessity. The nature of the PC cards and portable systems requires the card being powered on and off as needed to conserve power. Many PC cards have large input capaci-

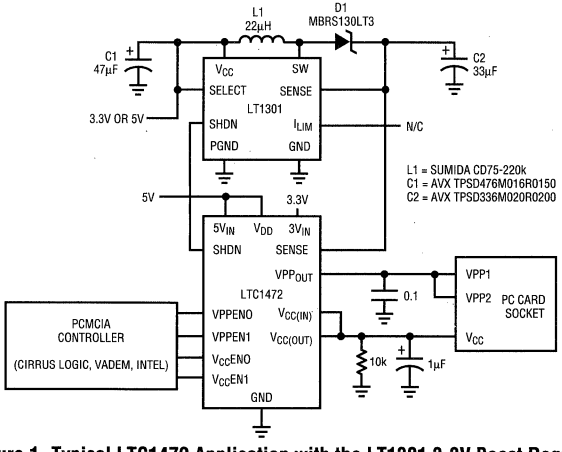


Figure 1. Typical LTC1472 Application with the LT1301 3.3V Boost Regulator

tance and draw over 2W. The power up/down sequencing can put demanding transient requirements on your system power supply. To make the transient response of the system supply manageable, the PCMCIA switch should have break-before-make switching, controlled rise and fall times and current limiting. The slowed rise time coupled with current limiting are critical in controlling the immense in-rush current difficulties seen when charging the large input capacitance of many cards

LTC®1472: Complete V_{CC} and VPP PCMCIA Switch Matrix with SafeSlot Protection

The LTC1472 is a complete, fully integrated V_{CC} and VPP switch matrix that addresses all of the PCMCIA socket switching needs. Figure 1 shows a typical LTC1472 application used in conjunction with the LT®1301 to supply 12V for flash memory programming. The LTC1472's logic inputs allow direct interfacing with both logic high and logic low industry standard controllers without any external glue logic. The LTC1472 is available in the space saving narrow 16-pin SOIC package. The V_{CC} switch's $R_{DS(ON)}$ is 0.14Ω to support the 1A current requirement. The V_{CC} output is switched between 3.3V, 5V and high impedance. The VPP output pin is switched between 0V, V_{CC}, 12V and high impedance. Table 1 shows the V_{CC} and VPP truth tables.

Table 1. LTC1472 Truth Table

V_{CC} Switch

V_{CC}EN0	V_{CC}EN1	$V_{CC(OUT)}$
0	0	off
1	0	5V
0	1	3.3V
0	1	off

VPP Switch

VPPEN0	VPPEN1	VPP_{OUT}
0	0	0V
0	1	$V_{CC(IN)}$
1	0	VPP_{IN}
1	1	Hi-Z

The LTC1472 features SafeSlot protection. The built-in SafeSlot current limiting and thermal shutdown features are vital to ensuring a robust and reliable system. The V_{CC} current limit is above 1A to maintain compatibility with all existing cards yet provide protection. The VPP current limit is above 120mA to also maintain compatibility. All switches are break-before-make type with controlled, slowed rise and fall times for minimal system supply impact. In-rush current, from even the largest card input capacitance, is kept under control by the LTC1472's slowed rise-time switching and current limiting.

The LTC1472 has on-chip charge pumps for switch driving. For this reason, the device does not require a continuous 12V source. Most of the time the LT1301 is in shutdown mode, consuming only 10µA. The LT1301 becomes operational only during flash memory programming. The LTC1472 itself conserves power by going to a low 1µA standby mode when V_{CC} and VPP outputs are switched off. The use of the LT1301 is optional. Any suitable 12V supply can be directly connected to the VPP_{IN} pin. Caution should be exercised when using a general purpose 12V supply; make certain that it does not have spikes or transients exceeding the flash memory 14V maximum voltage rating and that the regulation is within the 5% flash memory tolerance.

Conclusion

PCMCIA sockets are the preferred method of expansion in portable systems. As these devices proliferate to less sophisticated users, there will be greater opportunity for abuse. To counter this trend the portable system design must take safeguards to protect the system. The high level of integration, SafeSlot protection features and controlled rise and fall switching make the LTC1472 the ideal solution for portable systems.

Linear Technology has a family of PCMCIA socket voltage control products to suit a broad range of customer's needs. Table 2 lists the present part offerings. For assistance on your specific design needs, call Linear Technology.

Table 2. Linear Technology's PCMCIA Host Socket Voltage Control Products

Part Number	Remarks
LT1312	VPP Linear Regulator
LT1313	Dual Slot VPP Linear Regulator
LT1314	Low Cost V_{CC} and VPP Switch Matrix
LT1315	Dual Low Cost V_{CC} and VPP Switch Matrix
LTC1470	Complete SafeSlot Protected V_{CC} Switch Matrix
LTC1471	Dual Complete SafeSlot Protected V_{CC} Switch Matrix
LTC1472	Complete SafeSlot Protected V_{CC} and Switch Matrix

For literature on our PCMCIA Power Management devices call **1-800-4-LINEAR**. For applications help, call (408) 432-1900, Ext. 361

LINEAR TECHNOLOGY

DESIGN NOTES

Interfacing to V.35 Networks – Design Note 94

Y. K. Sim and Robert Reay

What is V.35?

V.35 is a CCITT recommendation for data transmission at 48kbs. The electrical interface between data communication equipment (DCE) and data terminal equipment (DTE) includes a set of balanced differential circuits conforming to Appendix II of Recommendation V.35 and a set of control circuits conforming to Recommendation V.28 (equivalent to RS232). A typical V.35 interface uses five differential signals and five single-ended handshaking signals. The V.35 electrical specifications are summarized in Table 1.

Table 1

Specification	Condition	Transmitter	Receiver
Source Impedance	Differential Measurement	50Ω to 150Ω	100Ω ±10Ω
Common-Mode Impedance	Terminals Shorted	150Ω ±15Ω	150Ω ±15Ω
Voltage Swing	100Ω Load	0.55V ±20%	
Common-Mode Swing	100Ω Load	0.6V Max	
Common-Mode Range	Between Dx and Rx Grounds	±4V	±4V

Problems with Traditional Implementations

The tight tolerance of the transmitter's impedance and voltage swing specifications makes the implementation of the transmitter a little tricky. The traditional approach is to use an RS422 differential driver such as the AM26LS30 (Figure 1). Because the chip has a voltage output, the signal must go through a resistive divider to meet the 0.55V swing specification. The problem is that the output voltage is a function of supply voltage, temperature and IC processing, making the 20% tolerance of the swing hard to meet for all conditions. Another problem is meeting the common-mode impedance specification of 150Ω ±15Ω because the output impedance of the driver is not well controlled. For the interface to meet the CCITT specifications under all conditions, another approach is needed.

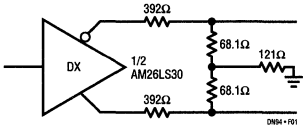


Figure 1. Traditional V.35 Implementation

LTC®1345

The LTC1345 is a single 5V V.35 transceiver with three drivers and three receivers that are fully compliant with the V.35 electrical specifications. The chip can be configured for DTE or DCE operation or shutdown using two select pins. In the shutdown mode, supply current is reduced to 1μA.

Each driver or receiver is terminated by an external Y or Δ resistor network (Figure 2), guaranteeing compliance with the V.35 impedance specification. The transmitter output consists of complementary switched-current sources of 11mA as shown in Figure 3. With a 100Ω test termination

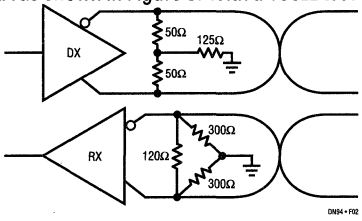


Figure 2. Y and Δ Termination Networks

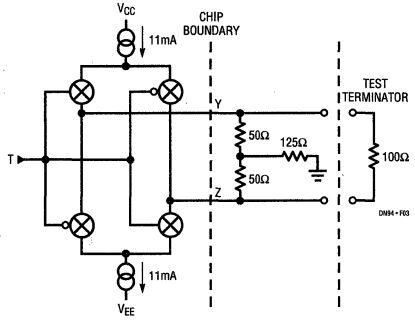


Figure 3. Simplified Transmitter Schematic

resistor, the differential output voltage is set at 0.55V (11mA×50Ω), and the common-mode voltage is set to 0V, thus meeting the V.35 voltage swing specifications under all conditions. A five Y-termination resistor network in a single narrow body S14 package is available from Beckman Industrial (part number: Beckman 627T500/1250, phone: 714-447-2357).

The differential input receiver has a 40mV input hysteresis to improve noise immunity and a common-mode range from –7V to 12V, allowing the receivers to be used for V.11 (RS422) applications, The output can be forced into high impedance by an output enable ($\overline{OE}$) pin or when the receiver is deselected. The negative supply is required to meet the ±4V common-mode operating range requirement. A charge pump generates the negative supply voltage (V_{EE}) with three external 1µF capacitors allowing single 5V operation.

Complete V.35 Port

Figure 4 shows the schematic of a complete single 5V DTE and DCE V.35 port using three ICs and eight capacitors per port. The LTC1345 with the Beckman 627T500/1250 resistor network is used to transmit and receive the differential clock and data signals. The LT®1134 is used to transmit and receive the single-ended control signals.

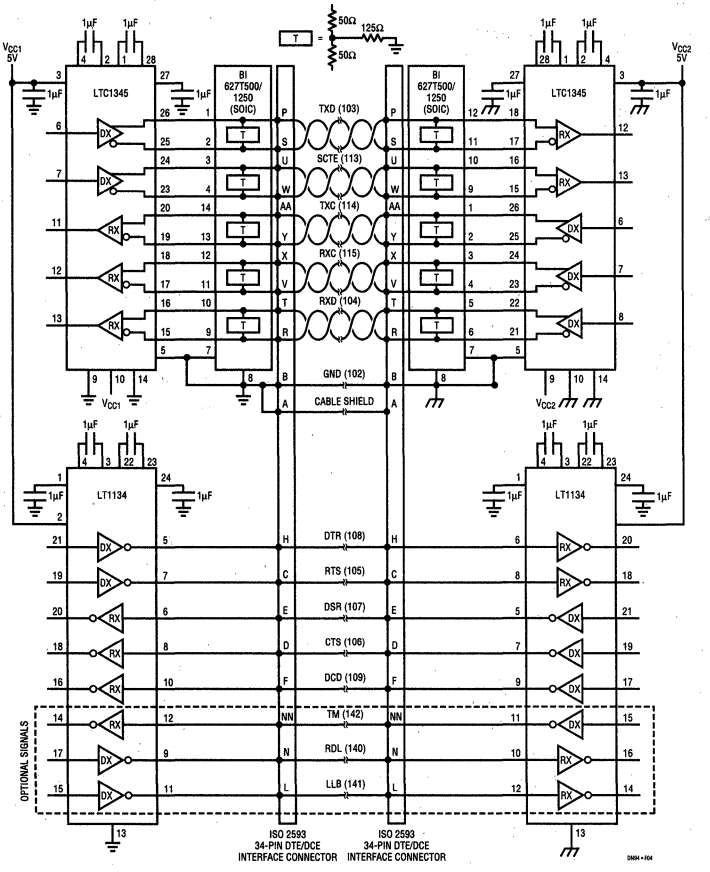


Figure 4. Complete Single 5V V.35 Interface

For literature on our Interface Products, call **1-800-4-LINEAR**. For applications help, call (408) 432-1900, Ext. 453

LINEAR TECHNOLOGY

DESIGN NOTES

Capacitor and EMI Considerations for New High Frequency Switching Regulators – Design Note 95

Carl Nelson and Bob Essaff

The LT®1372 family of boost and flyback converters and the LT1376 buck converter form a new line of high frequency switching regulators offered by Linear Technology. Up to 10 times faster (250kHz to 1MHz) than older devices, these new converters are actually more efficient than older designs. Several design considerations for high frequency switchers are discussed here.

Capacitor Technology Considerations

At lower frequencies, magnetics dominates the size of DC-to-DC converters, but at frequencies above 200kHz the largest component is typically the input and output bypass capacitors. This makes it important to pick the right capacitor technology in critical size applications. The most important parameter in choosing the capacitor is cost versus size and impedance. The input and output capacitors must have low impedance at the switching frequency to limit voltage ripple and power dissipation.

It is also desirable to have low impedance at much higher frequencies because high amplitude narrow spikes are created if the capacitor has even a few nH of inductance. The amplitude of these spikes is determined by the rate-of-rise of current (dI/dt) fed to the capacitor. For a high speed converter, dI/dt may be as high as 0.5A/ns. Even 3nH of capacitor lead inductance will create $(0.5\,e^{9})\,(3\,e^{-9}) = 1.5V$ spikes. The second part of this Design Note shows how to attenuate these spikes using parasitic PC board elements.

Figure 1 details the impedance characteristics of the most popular switching regulator capacitors. These are aluminum electrolytic, solid tantalum, OS-CON, and ceramic. Within one technology, impedance at lower frequencies tends to closely track physical volume of the capacitor, with larger volume giving lower impedance.

Aluminum electrolytics perform poorly and are rarely used at frequencies above 100kHz, but their low cost and higher voltage capability may cause them to be used for input bypass applications.

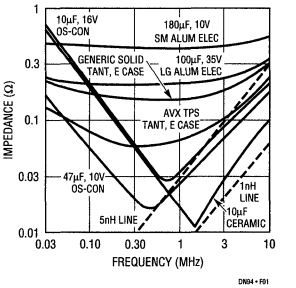


Figure 1. Capacitor Impedance

Solid tantalum capacitors offer small size, low impedance, and low Q (to prevent loop stability problems). The down side of tantalum is limited voltage, typically 50V maximum, and a tendency for a small percentage of units to self-destruct when subjected to very high turn-on surge currents. AVX addresses the problem with their TPS line which features more rugged construction and special surge testing. Even TPS units must be voltage derated by 2:1 if high turn-on surges are expected, limiting practical operating voltage to 25V. Even with their shortcomings, solid tantalum seems to be the technology of choice for medium to high frequency DC-to-DC converters.

OS-CON capacitors from Sanyo and Marcon are made with a semiconductor-like dielectric that gives very low impedance per unit volume. They greatly outperform aluminum units, but have a few pitfalls of their own. Maximum voltage is 25V, height is significantly greater than solid tantalum, and most units are not surface mount. The very low ESR (effective series resistance) of OS-CON capacitors can also cause a problem with loop stability in switching regulators.

Ceramic capacitors offer the lowest impedance at 500kHz and beyond, but they suffer from high cost, large footprint, and limited temperature range. They are probably best suited for input bypassing at higher voltages, and very high frequency (≥1MHz) applications.

Note that at high frequencies, most of the capacitors approach an inductive line of about 1nH to 5nH. Smaller units in parallel will reduce effective inductance, but cost goes up.

Controlling EMI: Conducted and Radiated

EMI strikes terror into system designers because its causes and cures are not well understood. There are two separate issues involved; meeting external FCC standards and avoiding internal system malfunctions. Higher frequency switching regulators would seem to make the whole problem much worse, but there are several mitigating circumstances that have allowed nearly all systems to use high frequency converters with few problems.

Contrary to popular misconceptions, older switching regulators rarely were a major contributor to overall system noise problems if the system contained reasonable amounts of logic chips. The noise created by a microprocessor, databusses, clock drivers, etc. usually swamps out switcher noise. This can be seen very simply by connecting a linear regulator temporarily in place of the switcher. Radiated noise using standard FCC methods, and supply line noise often show almost no change when the switcher is turned off.

The second reason for reduced high frequency switcher noise problems is that the components used are physically smaller. Radiated noise is proportional to radiating line length, so smaller, tightly packed components radiate significantly less.

Conducted EMI usually makes its appearance as ripple current fed back into the input supply, or as ripple voltage at the regulator output. Figure 2 shows how both of these effects can be virtually eliminated by using parasitic inductance in input or output lines. At 500kHz each inch of board trace represents nearly 0.1Ω of reactance, and for the higher harmonics the impedance is much higher. This impedance can be used in combination with existing capacitors to create "free" filter action.

At the input, as shown in Figure 3, the switching ripple current will all disappear into the input bypass capacitor if the reactance in the input lines is large compared to the capacitor impedance. For instance, an OS-CON 33µF, 20V capacitor has an impedance of about 0.02Ω at 500kHz. If the supply lines have an effective length of six inches (input plus return), the line reactance will be about 0.6Ω at 500kHz. The fundamental of the ripple current will be attenuated by the ratio of line impedance to capacitor impedance = 0.6/0.02 = 30:1. Higher harmonics will virtually disappear.

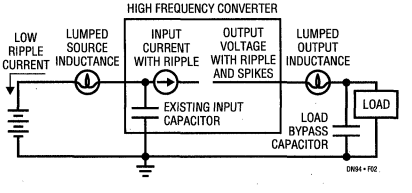


Figure 2. Free High Frequency Filters Using Parasitics

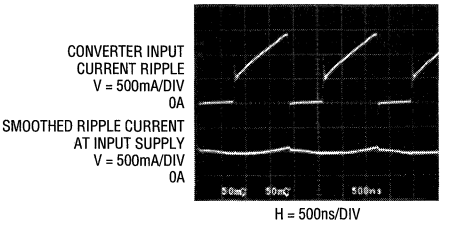


Figure 3.

Output ripple can be filtered by utilizing the reactance of output lines in conjunction with load bypass capacitors as shown in Figure 4. With two inches of output trace (0.16Ω at 500kHz) and 0.15Ω capacitor impedance, fundamental ripple will be attenuated by two-to-one and output noise spikes virtually eliminated. The Fourier components of these spikes start above 25MHz where line reactance is 4Ω per inch.

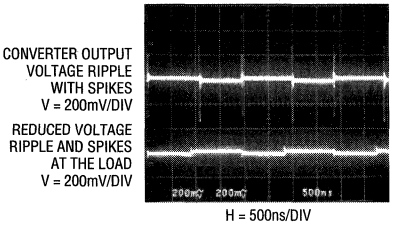


Figure 4.

A common cause of radiated noise is the use of "open core" magnetics. The lowest cost high frequency inductors are wound on ferrite rods or barrels, which do not have a closed magnetic field path. This generates large local B fields that can play havoc with sensitive low level circuitry such as disk drives, A-to-D converters, and IF strips. Each application needs to be evaluated separately, but in situations where low signal levels exist in close proximity to the converter, closed core magnetics such as toroids or E cores should be used until extensive system level testing has proved out a cheaper solution.

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LINEAR TECHNOLOGY

DESIGN NOTES

LTC1451/52/53: 12-Bit Rail-to-Rail Micropower DACs in an SO-8

Design Note 96

Hassan Malik and Jim Brubaker

The LTC®1451, LTC1452 and LTC1453 are complete, single supply, rail-to-rail voltage output 12-bit digital-to-analog (DAC) converters. They include an output buffer amplifier and a space saving SPI compatible three-wire serial interface. There is also a data output pin that allows daisy-chaining multiple DACs. These DACs use a proprietary architecture which guarantees a DNL (Differential Nonlinearity) error of less than 0.5LSB. The typical DNL error is about 0.2LSB as shown in Figure 1. There is a built-in power-on reset that resets the output to zero scale. The output amplifier can swing to within 5mV of V_{CC} when unloaded and can source or sink 5mA even at a 4.5V supply. These DACs come in an 8-pin PDIP and SO-8 package.

5V and 3V Operation

The LTC1451 has an on-board reference of 2.048V and a nominal output swing of 4.095V. It operates from a single 4.5V to 5.5V supply dissipating 2mW ($I_{CC(TYP)}$ = 400µA).

The LTC1452 is a multiplying DAC with no on-board reference and a full-scale output of twice the reference input. It operates from a single supply that can range from 2.7V to 5.5V. It dissipates 1.125mW ($I_{CC(TYP)}$ = 225µA) at a 5V supply and a mere 0.5mW ($I_{CC(TYP)}$ = 160µA) at a 3V supply.

The LTC1453 has a 1.22V on-board reference and a convenient full scale of 2.5V. It can operate on a single supply with a wide range of 2.7V to 5.5V as shown in Figure 2. It dissipates 0.75mW ($I_{CC(TYP)}$ = 220µA) at a 3V supply. The digital inputs can swing above V_{CC} for easy interfacing with 5V logic.

True Rail-to-Rail Output

The output rail-to-rail amplifier can source or sink 5mA over the entire operating temperature range while pulling to within 300mV of the positive supply voltage or ground. The output swings to within a few millivolts of either

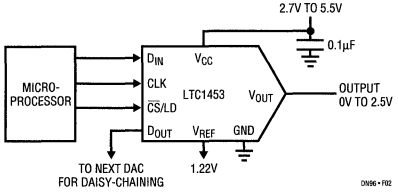
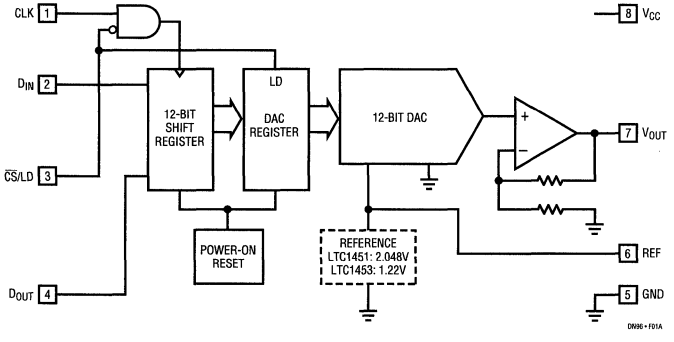


Figure 2. The 3V LTC1453 is SPI Compatible and Talks to Both 5V and 3V Processors



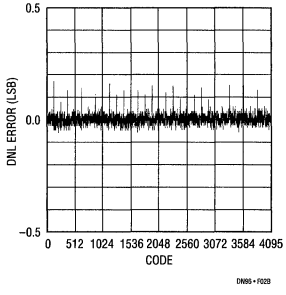


Figure 1. Proprietary Architecture Guarantees Excellent DNL

supply rail when unloaded and has an equivalent output resistance of 50Ω when driving to either rail. The output can drive a capacitive load of up to 1000pF without oscillating.

Wide Range of Applications

Some of the applications for this family include digital calibration, industrial process control, automatic test equipment, cellular telephones and portable battery-powered applications where low supply current is essential. Figure 3 shows how to use an LTC1453 to make an opto-isolated digitally controlled 4mA to 20mA process controller. The controller circuitry, including the opto-isolator, is powered by the loop voltage that can have a wide range of 3.3V to 30V. The 1.22V reference output of the LTC1453 is used for the 4mA offset current and V_{OUT} is used for the digitally controlled 0mA to 16mA current. R_S is a sense resistor and the LT®1077 op amp modulates the transistor Q1 to provide the 4mA to 20mA current through this resistor. The potentiometers allow for offset and full-scale adjustment. The control circuitry consumes well under the 4mA budget at zero scale.

Flexibility, True Rail-to-Rail Performance and Micropower; All In a Tiny SO-8

The LTC1451, LTC1452 and LTC1453 are the most flexible micropower, stand alone DACs that offer true rail-to-rail performance. This flexibility along with the tiny SO-8 package allows these parts to be used in a wide range of applications where size, power, DNL and single supply operation are important.

Table 1. LTC Serial Voltage Output DACs

Part	V_{CC} Range	Reference	Full Scale	I_{CC}
LTC1451	4.5V to 5.5V	2.048V-Internal	4.095V	400µA at 5V
LTC1452	2.7V to 5.5V	External	2 × REF	225µA at 5V
LTC1453	2.7V to 5.5V	1.22V-Internal	2.5V	250µA at 3V
LTC1257	4.75V to 15.75V	2.048V-Internal (2.5V to 12V-External)	2.048V (2.5V to 12V)	350µA at 5V

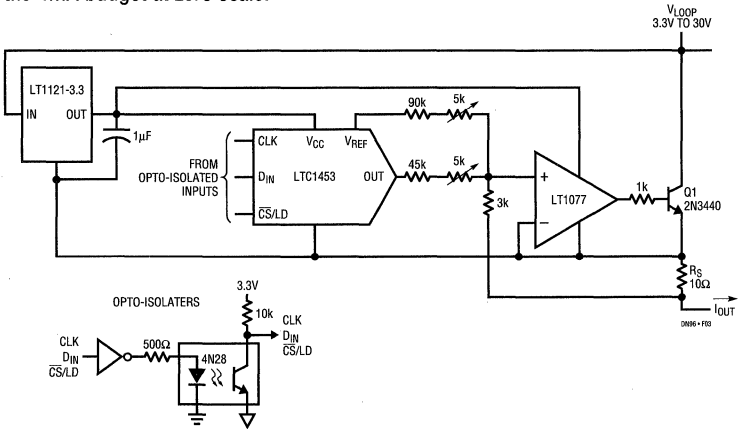


Figure 3. 4mA to 20mA Process Controller Has 3.3V Minimum Loop Voltage

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LINEAR TECHNOLOGY

DESIGN NOTES

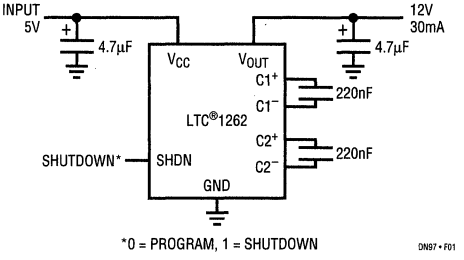
Flash Memory VPP Generator Reference Designs

Design Note 97

Mitchell Lee

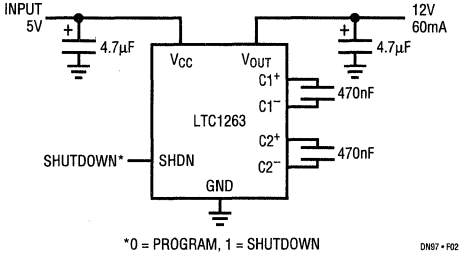
The VPP generator circuits shown here cover a range of 30mA to 240mA with 3.3V or 5V inputs as noted. Table 1 summarizes these circuits for quick reference.

30mA from 5V Input



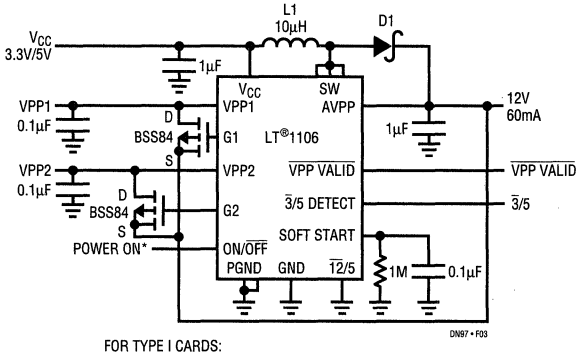
Charge pump design uses no inductors. This is a minimum component count, minimum size solution.

60mA from 5V Input



Charge pump design uses no inductors. This is a minimum component count, minimum size solution.

60mA from 3.3V/5V Input



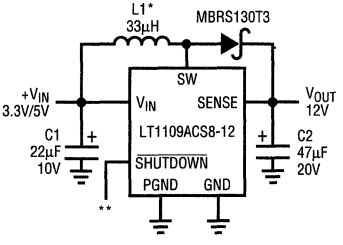
FOR TYPE I CARDS:
L1: DALE ILS-3825-01
D1: 4 BAT54Cs IN PARALLEL (PHILIPS), 1.1mm MAXIMUM HEIGHT

FOR TYPE II CARDS:
L1: MURATA ERIE LQH3C100K04M00
D1: MOTOROLA MBRS0520, 2.1mm MAXIMUM HEIGHT

*1 = PROGRAM, 0 = SHUTDOWN

Designed for PCMCIA Type I or Type II in-card use. The LT1106 includes VPP bypass switching for sockets supporting flash cards.

60mA/120mA from 3.3V/5V Input

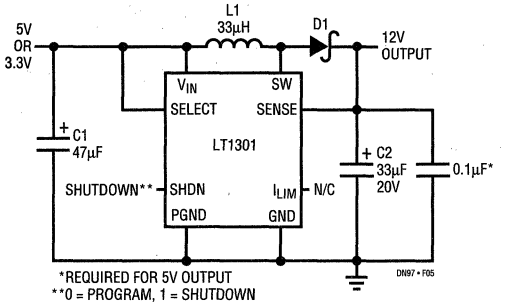


* COILTRONICS CTX33-2
SUMIDA CD54-330LC

** 1 = PROGRAM
0 = SHUTDOWN

All surface mount, minimum component count solution.

60mA/120mA from 3.3V/5V Input

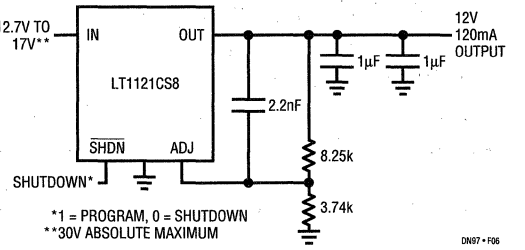


*REQUIRED FOR 5V OUTPUT
**0 = PROGRAM, 1 = SHUTDOWN

L1: COILCRAFT DO3316-333 OR SUMIDA CD73-330KC
D1: 1N5817 OR MOTOROLA MBRS130LT3
C1: AVX TPSD476M016R0100 OR SANYO OS-CON 165A47M
C2: AVX TPSD336M020R0100 OR SANYO OS-CON 205A33M

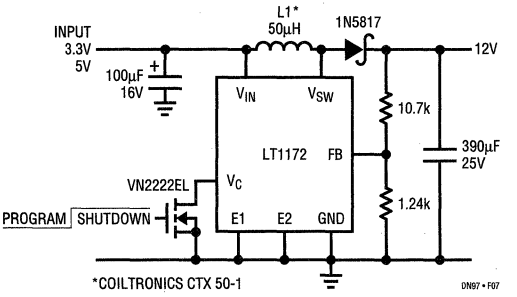
Efficiency is 84% to 88% at full load.

120mA from 12.7V to 17V Input



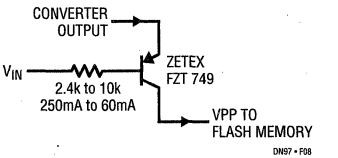
This circuit serves as a post regulator for flyback converters or overwindings. Output automatically falls to zero in shutdown.

120mA/240mA from 3.3V/5V Input



High output current converter programs up to eight memory chips simultaneously.

Output Disconnect



This shutdown circuit allows output to drop to zero when switching converter is disabled.

Table 1. Summary of Flash Memory VPP Generator Solutions

Number of Flash Chips				
V_{IN} = 3.3V	V_{IN} = 5V	V_{IN} = 12.6V To 17V	Regulator	Advantages
—	1	—	LTC1262	No Inductors
—	2	—	LTC1263	No Inductors
2	2	—	LT1106	PCMCIA Type I In-Card Use. Includes VPP Bypass Switching
2	4	—	LT1109A	Low Cost
2	4	—	LT1301	High Efficiency
—	—	4	LT1121	Linear Post Regulator
4	8	—	LT1172	High Current

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LINEAR TECHNOLOGY

DESIGN NOTES

Highly Integrated High Efficiency DC/DC Conversion

Design Note 98

San-Hwa Chee and Howard Haensel

The LTC®1574 and LTC1265 high efficiency step-down regulators minimize external components by using integrated low RDS(ON) P-channel switches. The LTC1574 goes one step further by including a low forward drop Schottky diode—an industry first. Both regulators also include on-chip low-battery detectors.

Burst Mode™ operation allows the LTC1574 and LTC1265 to achieve over 90% efficiency for load currents as low as 10mA. Current mode operation provides clean start-up, accurate current limit, and excellent line and load regulation. Inherent 100% duty cycle in dropout allows the user to extract maximum battery life. Both regulators can be shut down to a few microamperes.

LTC1574

The LTC1574 features the highest level of integration for a switching regulator. Besides an on-chip power MOSFET, it includes a low forward drop Schottky diode. The user needs only to provide an inductor and input/output filter capacitors for a complete high efficiency step-down converter. The current limit is pin selectable to either 340mA or 600mA, optimizing efficiency for a wide range of load currents.

Figure 1 shows a typical LTC1574 surface mount application requiring only three external components. It provides 3.3V at 150mA from an input voltage of 5V. Peak inductor current is limited to 340mA by connecting pin 6 (I_{PGM}) to ground. For applications requiring higher output current, connect pin 6 to V_{IN}. Under this condition the maximum load current is increased to 425mA. Efficiency curves for the two conditions on I_{PGM} are graphed in Figure 2. Note that all components remain the same for the two curves.

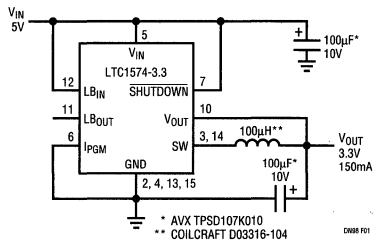

Figure 1. LTC1574 3.3V, 150mA Surface Mount

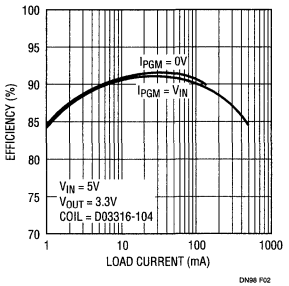

Figure 2. LTC1574 5V to 3.3V Efficiency

Low Noise Regulator

In some applications, it is important not to introduce any switching noise within the audio frequency range. Due to the Burst Mode nature of the LTC1574, there is a possibility that the regulator will introduce audio noise at some load currents. To circumvent this problem, a feed-forward capacitor can be used to shift the noise spectrum up and out of the audio band. Figure 3 shows the low noise connection with C2 being the feed-forward capacitor. The peak-to-peak output ripple is reduced to 30mV over the entire load range. A toroidal surface mount inductor L1 is chosen for its excellent self-shielding properties. Open magnetic structures such as drum and rod cores are to be avoided since they inject high flux levels into their surroundings. This can become a major source of noise in any converter circuit.

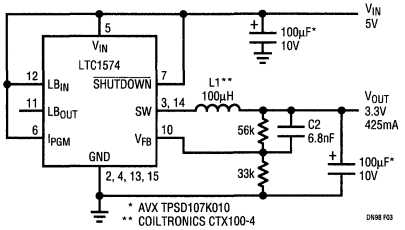

Figure 3. Low Noise 5V to 3.3V Regulator

LTC1265

Whereas the LTC1574 can only supply a load current up to 425mA, the LTC1265 can source up to 1.2A. It features a low 0.3Ω (V_{IN} = 10V) internal P-channel MOSFET to provide high efficiency at high load current. The inductor current is user-programmable via an external current sense resistor. Operation up to 700kHz permits the use of small surface mount inductors and capacitors. The LTC1265 employs an external Schottky diode.

Unlike the LTC1574 which always operates in Burst Mode, the LTC1265 only operates in Burst Mode at light loads and switches to continuous operation at heavier loads. For the LTC1265 to operate in Burst Mode, the load current has to be less than 15mV/R_{SENSE}.

Figure 4 shows a typical LTC1265 surface mount application. It provides 3.3V at 1A from an input voltage range of 4V to 12V. Efficiency at various input voltages is plotted in Figure 5. Here the sense resistor is chosen as 0.1Ω, therefore the LTC1265 will go into continuous mode operation for load currents greater than 150mA. The peak efficiency approaches 93% at mid-current levels.

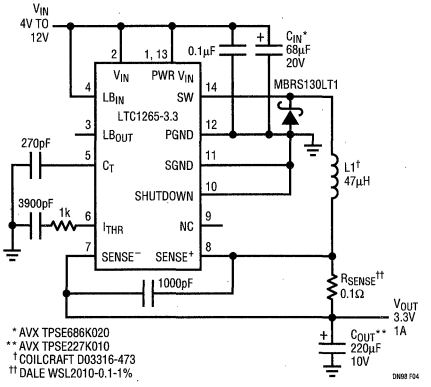

Figure 4. LTC1265 3.3V, 1A Surface Mount

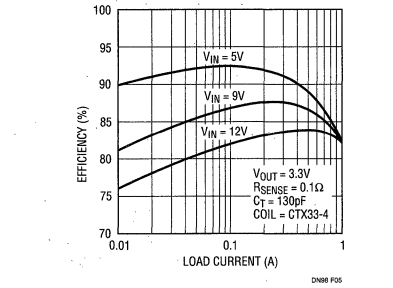

Figure 5. LTC1265 5V to 3.3V Efficiency

Battery Charger Application

In Figure 6, the LTC1265 is configured as a battery charger for a four-NiCd stack. It has the capability of performing a fast charge of 1A, a trickle charge of 100mA or the charger can be shut off. In shut-off, diode D1 serves two purposes. First, it prevents the LTC1265 circuitry from drawing battery current and second, it eliminates "back powering" the LTC1265 which avoids a potential latch condition at power-up.

LTC1574 or LTC1265?

The LTC1574 and LTC1265 are differentiated by both the output current level and operating mode. For loads less than 425mA, the LTC1574 is the ideal choice because of its simplicity and ease of use. However, for applications requiring continuous mode operation, or more than 425mA output current, the LTC1265 must be used. Both devices can be tailored to meet a wide range of requirements.

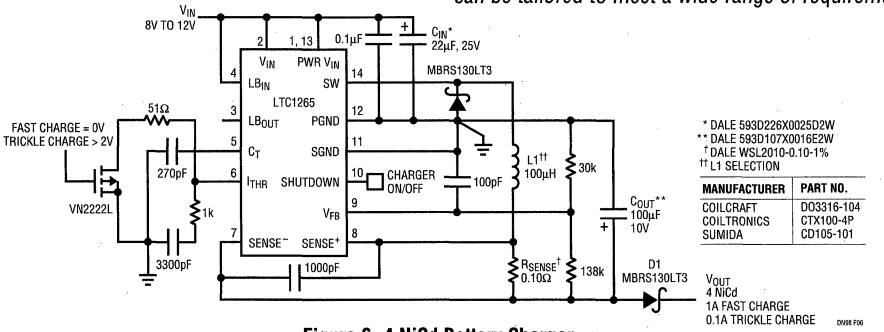

Figure 6. 4 NiCd Battery Charger

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LINEAR TECHNOLOGY

DESIGN NOTES

LT1182 Floating CCFL with Dual Polarity Contrast – Design Note 99

Anthony Bonte

Current generation portable computers and instruments use backlit liquid-crystal displays (LCDs). Cold-cathode fluorescent lamps (CCFLs) provide the highest available efficiency for backlighting the display. The lamp requires high voltage AC to operate, mandating an efficient, high voltage DC/AC converter. The LCD also requires a bias supply for contrast control. The supply's output must regulate and provide adjustment over a wide range.

Manufacturers offer a wide array of monochrome and color displays. These displays vary in size, lamp drive current, contrast voltage polarity, operating voltage range and power consumption. The small size and battery-powered operation associated with LCD-equipped apparatus dictate low component count and high efficiency. Size constraints place limitations on circuit architecture and long battery life is a priority. All components, including PC board and hardware, must fit within the LCD enclosure with a height restriction of 5mm to 10mm.

Linear Technology addresses these requirements by introducing the LT®1182/LT1183/LT1184F/LT1184. The LT1182/LT1183 are dual fixed frequency, current mode switching regulators that provide the control function for cold-cathode fluorescent lighting and liquid-crystal display contrast. The LT1184F/LT1184 provide only the CCFL function.

The ICs include high current, high efficiency switches, an oscillator, a reference, output drive logic, control blocks and protection circuitry. All of the devices support grounded lamp or floating lamp configurations using a unique lamp current control circuit. The LT1182/LT1183 support nega-

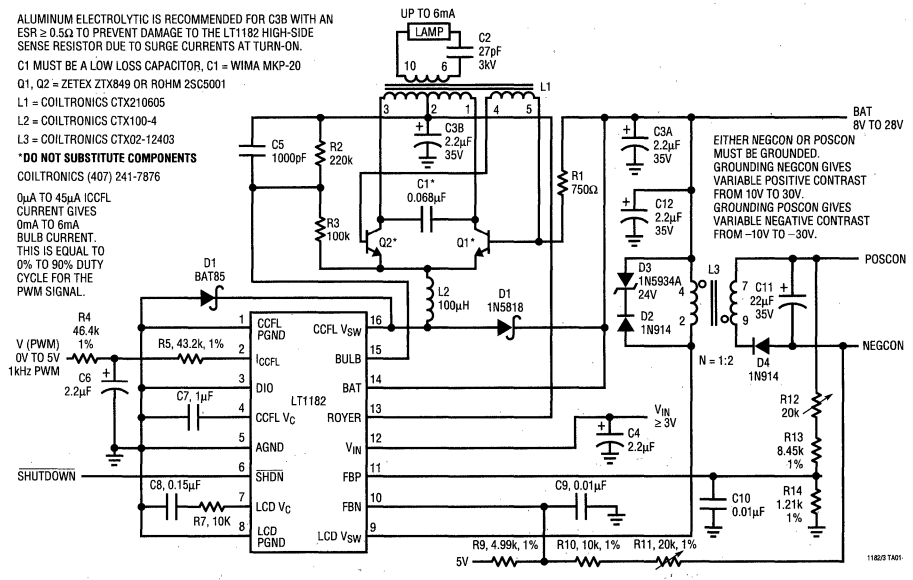

Figure 1. LT1182 Floating CCFL Configuration with Variable Positive/Variable Negative LCD Contrast

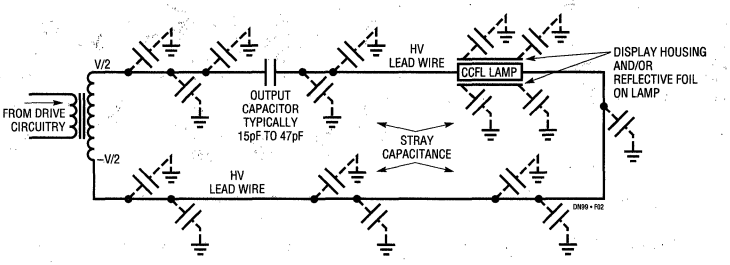

Figure 2. Loss Path Due to Stray Capacitance in a Floating LCD Installation. Differential, Balanced Lamp Drive Reduces This Loss Term and Improves Efficiency

tive voltage or positive voltage LCD contrast operation with a new dual polarity error amplifier. In short, this new family reduces system power dissipation, requires fewer external components, reduces overall system cost and permits a high level of system integration for a backlight/LCD contrast solution.

Figure 1 is a complete floating CCFL circuit with variable negative/variable positive contrast voltage capability based on the LT1182. Lamp current is programmable from 0mA to 6mA using a 0V to 5V 1kHz PWM signal at 0% to 90% duty cycle. LCD contrast output voltage polarity is determined by which side of the transformer secondary (either POSCON or NEGCON) the output connector grounds. In either case, LCD contrast output voltage is variable from an absolute value of 10V to 30V. The input supply voltage range is 8V to 28V. The CCFL converter is optimized for photometric output per watt of input power. CCFL electrical efficiency up to 90% is possible and requires strict attention to detail. LCD contrast efficiency is 82% at full power.

Achieving high efficiency for a backlight design requires careful attention to the physical layout of the lamp, its leads and the construction of the display housing. Parasitic capacitance from any high voltage point to DC or AC ground creates paths for unwanted current flow. This parasitic current degrades electrical efficiency. The loss term is related to $1/2CV^2f$ where C is the parasitic capacitance, V is the voltage at any point on the lamp and f is the royer operating frequency. Losses up to 25% have been observed in practice. Figure 2 indicates the loss paths present in a typical LCD enclosure for a floating lamp configuration. Layout techniques that increase parasitic capacitance include long high voltage lamp leads, reflective metal foil around the lamp and displays supplied in metal enclosures.

Lossy displays are the primary reason to use a floating lamp configuration. Providing symmetric, differential drive to the lamp reduces the total parasitic loss term by one-half in comparison to a grounded lamp configuration. As an added benefit, floating lamp configurations eliminate field imbalance along the length of the lamp. Figure 3 illustrates this effect. Eliminating field imbalance improves the illumination range from about 6:1 for a grounded lamp configuration to 30:1 for a floating lamp configuration. Figure 4 is a graph of normalized Nits/Watt versus lamp current for a typical manufacturer's display with a 6mA lamp. Performance for the display is compared in a floating lamp configuration versus a grounded lamp configuration. The benefit of reduced parasitic loss is readily apparent.

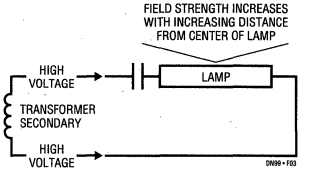

Figure 3. Field Strength vs Distance for a Floating Lamp. Improving Field Imbalance Permits Extended Illumination Range at Low Levels

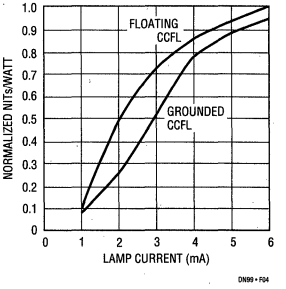

Figure 4. Normalized Nits/Watts vs Lamp Current

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LINEAR TECHNOLOGY

DESIGN NOTES

Dual Output Regulator Uses Only One Inductor – Design Note 100

Carl Nelson

Many modern circuit designs still need a dual polarity supply. Communication and data acquisition are typical areas where both 5V and –5V are needed for some of the IC chips. It would be nice if a single switching regulator could supply both outputs with good regulation and a minimum of magnetic components. The circuit in Figure 1 is a good example of exploiting the best advantages of components and topologies to achieve a very small, dual output regulator with a single magnetic component.

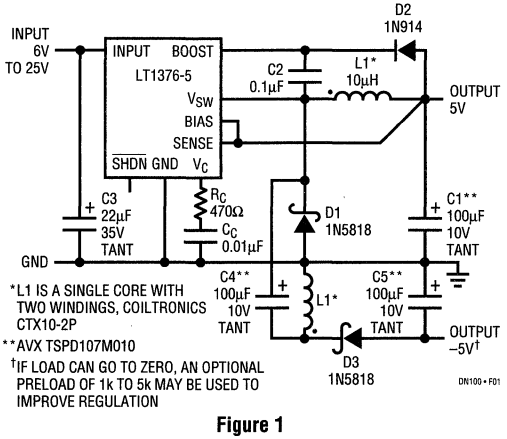


Figure 1

The 5V output is generated using the LT®1376 buck converter. This device uses special design techniques and high speed processing to create a 500kHz design that is much smaller and more efficient than previous monolithic circuits. The current mode architecture and saturating switch design allow the LT1376 to deliver up to 1.5A load current from the tiny 8-pin SO package. L1 is a 10µH surface mount inductor from Coiltronics. It is manufactured with two identical windings that can be connected in series or parallel. One of the windings is used for the buck converter.

The second winding is used to create a negative output SEPIC (Single Ended Primary Inductance Converter) topology using D3, C4, C5, and the second half of L1. This converter takes advantage of the fact that the switching signal driving L1 as a positive buck converter is already the correct amplitude for driving a –5V SEPIC converter. During switch off time, the voltage across L1 is equal to the 5V output plus the forward voltage of D1. An identical voltage is generated in the second winding, which is connected to generate –5V using D3 and C5. Without C4, this would be a simple flyback winding connection with modest regulation. The addition of C4 creates the SEPIC topology. Note that the voltage swing at both ends of C4 is theoretically identical even without the capacitor. The undotted end of both windings goes to a zero AC voltage node, so the equal windings will have equal voltages at the opposing ends. Unfortunately, coupling between windings is never perfect, and load regulation at the negative output suffers as a result. The addition of C4 forces the winding potentials to be equal and gives much better regulation.

Regulation Performance and Efficiency

Figure 2 details the regulation performance of the circuit. The positive output combined load and line regulation is better than 1%, and this was considered good enough to forgo a graph. Negative output voltage is graphed as a function of negative load current for several values of positive load current. For best regulation, the negative output should have a preload of at least 1% of the maximum positive load.

Total output current of this circuit is limited by the maximum switch current of the LT1376. The following formula gives peak switch current, which cannot exceed 1.5A. This formula, in the spirit of simplicity, is simplified, so caution must be used if it indicates close to 1.5A peak current.

$$I_{PEAK} = 0.25A + (I^+) + (2)(I^-) \text{ (Must be less than 1.5A)}$$

Maximum negative load current is limited by the +5V load. A typical limit is one half of 5V current, but a more exact number can be found from:

$$\text{Max Negative Load} = (I^+)(0.07)(V_{IN} - 2)$$

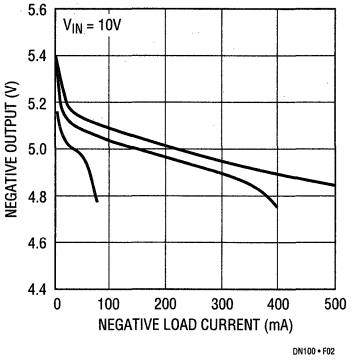


Figure 2. –5V Regulation

Note that as input voltage drops, less and less current is available from the negative output.

Efficiency of the switching regulator is not as good as a single buck converter, but still is very respectable, exceeding 80% over a wide current range. The inductor called out on the circuit schematic is a low cost off-the-shelf Coiltronics part made with a powdered iron core. Replacing that part with a Magnetics, Inc. Kool Mμ® core #77130 with 13 turns of #24 wire will raise efficiency by 3% across most of the load current range.

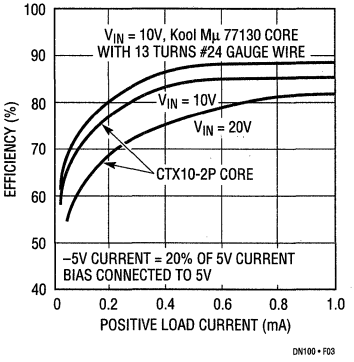
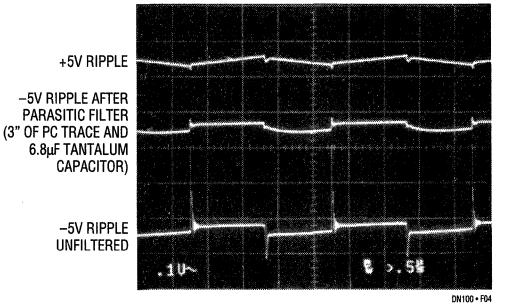


Figure 3. Dual Output Efficiency

Output Ripple Voltage

Output ripple voltage is determined by the ESR of the output capacitors. The capacitors shown are AVX type TPS surface mount solid tantalum which are specially constructed for low ESR (<0.1Ω). Peak-to-peak ripple current into the +5V output capacitor is a triwave, typically $0.3A_{P-P}$, so an ESR of 0.1Ω in C1 will give $30mV_{P-P}$ output ripple. It is interesting to note that this ripple current is about one half of what would be expected for a buck converter. This occurs because the two windings are driven in parallel, so magnetizing current divides equally between the windings.

Ripple current peak-to-peak into the –5V output capacitor is approximately equal to twice the negative load current. The wave shape is roughly rectangular, and so is the resultant output ripple voltage. A 100mA negative load and 0.1Ω ESR output capacitor will have (2)(0.1A)(0.1Ω) = $20mV_{P-P}$ ripple. A word of caution, however; the current waveform contains fast edges, so the inductance of the output capacitor multiplied by the rate-of-rise of the current will generate very narrow spikes superimposed on the output ripple. With capacitor inductance of 5nH, and dI/dt = 0.05A/ns, the spike amplitude will be 250mV! Now for the good news. The effective bandwidth of the spikes is all above 20MHz, so it is very easy to filter them out. In fact, the inductance of the output PC board traces (20nH/in) coupled with load bypass capacitors will normally filter out the spikes. The only caveat is that if the load bypass capacitors are very low ESR types like ceramic, they should be paralleled with a larger tantalum capacitor to reduce the Q of the filter.



Both outputs can be shut down simultaneously by driving the LT1376 shutdown pin low. An undervoltage lockout function can also be implemented by connecting a resistor divider to the shutdown pin. See the LT1376 data sheet for details.

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LINEAR TECHNOLOGY

DESIGN NOTES

A Precision Wideband Current Probe for LCD Backlight Measurement – Design Note 101

Jim Williams

Evaluation and optimization of Cold Cathode Fluorescent Lamp (CCFL) performance requires highly accurate AC current measurement. CCFLs, used to backlight LCD displays, typically operate at 30kHz to 70kHz with measurable harmonic content into the low MHz region[1]. Accurate determination of RMS operating current is important for electrical and emissivity efficiency computations and to ensure long lamp life. Additionally, it is desirable to be able to perform current measurements in the presence of high common-mode voltage (>1000V_{RMS}). This capability allows investigation and quantification of display and wiring induced losses, regardless of their origins in the lamp drive circuitry.

Current Probe Circuitry

Figure 1's circuitry meets the discussed requirements. It signal conditions a commercially available "clip-on" current probe with a precision amplifier to provide 1% measurement accuracy to 10MHz. The "clip-on" probe provides convenience, even in the presence of the high common voltages noted. The current probe biases A1, operating at a gain of about 3.75. No impedance matching is required due to the probe's low output impedance termination. Additional amplifiers provide distributed gain, maintaining wide bandwidth with an overall gain of about 200. The individual amplifiers avoid any possible crosstalk-based error that could be introduced by a monolithic quad amplifier. D1 and Rx are selected for polarity and value to trim overall amplifier offset. The 100Ω trimmer sets gain, fixing the scale factor. The output drives a thermally-based, wideband RMS voltmeter. In practice, the circuit is built into a 2.25" × 1" × 1" enclosure which is *directly* connected, via BNC hardware, to the voltmeter. No cable is used. The result is a "clip-on" current probe with 1% accuracy over a 20kHz to 10MHz bandwidth. Figure 2 shows response for the probe-amplifier as measured on a Hewlett-Packard HP-4195A network analyzer.

[1] Williams, Jim, "Techniques for 92% Efficient LCD Illumination." Linear Technology Corporation AN55, August 1993.

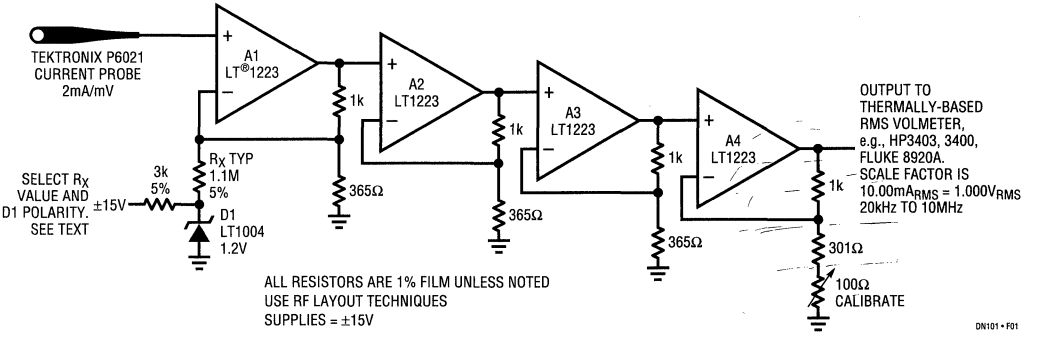

Figure 1. Precision "Clip-On" Current Probe for CCFL Measurements Maintains 1% Accuracy Over 20kHz to 10MHz Bandwith

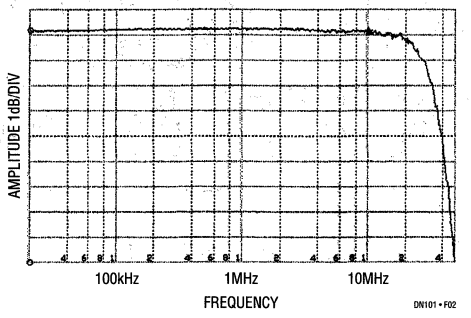

Figure 2. Amplitude vs Frequency Output of HP4195A Network Analyzer. Current Probe-Amplifier Maintains 1% (0.1dB) Error Bandwidth from 20kHz to 10MHz. Small Aberrations Between 10MHz and 20MHz Are Test Fixture Related

Current Calibrator

Figure 3's circuit, a current calibrator, permits calibration of the probe-amplifier and can be used to periodically check probe accuracy. A1 and A2 form a Wein bridge oscillator. Oscillator output is rectified by A4 and A5 and compared to a DC reference at A3. A3's output controls Q1, closing an amplitude stabilization loop. The stabilized amplitude is terminated into a 100Ω, 0.1% resistor to provide a precise 10.00mA, 60kHz current through the series current loop. Trimming is performed by altering the nominal 15k resistor for exactly 1.000V_{RMS} across the 100Ω unit.

In use, this current probe has shown 0.2% baseline stability with 1% absolute accuracy over one year's time. The sole maintenance requirement for preserving accuracy is to keep the current probe jaws clean and avoid rough or abrupt handling of the probe[2].

[2] Private Communication. Tektronix, Inc.

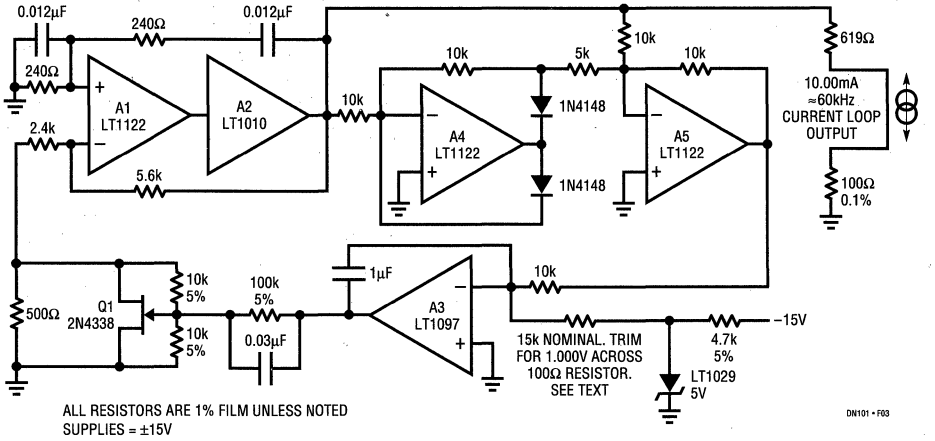

Figure 3. Current Calibrator for Probe Trimming and Accuracy Checks. Stabilized Oscillator Forces 10.00mA Through Output Current Loop at 60kHz

LINEAR TECHNOLOGY

DESIGN NOTES

RS485 Transceivers Reduce Power and EMI – Design Note 102

Dave Dwelley, Teo Yang Long, Yau Khai Cheong and Bob Reay

Recent innovations in process and circuit design have enabled the release of three new RS485 transceivers: the LTC®1481, LTC1483 and LTC1487. These devices share an improved receiver circuit which features 80µA quiescent current operation (driver disabled) with no loss in AC performance relative to standard RS485 devices, and a new 1µA shutdown mode (Figure 1). All three new devices are pin compatible with the industry standard LTC485 pinout, and feature Linear Technology's exclusive ±10kV ESD protection (Human Body Model) at the line I/O pins, eliminating the need for external ESD protection in most cases.

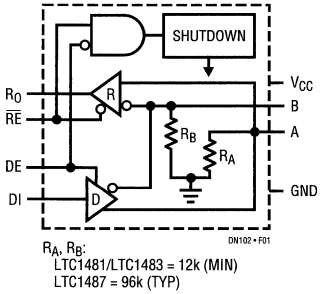

Figure 1. LTC1481/LTC1483/LTC1487 Block Diagram

LTC1481

The LTC1481 provides full 2.5Mbaud driver and receiver speeds with the low power and improved ruggedness features shared by all three members of the family. Like all Linear Technology RS485 products, it features full RS485 and RS422 compatibility, guaranteed operation over the –7V to 12V common-mode range and a unique driver output circuit that prevents CMOS latch-up and maintains high impedance at the line pins, even when the power is off. An internal driver short-circuit current limit and a thermal overload protection circuit prevent damage under severe fault conditions. The LTC1481 is ideally suited for designs which need to transmit high speed data with minimum power consumption.

LTC1483

The LTC1483 is a reduced EMI version of the LTC1481 intended for use in systems where electromagnetic interference concerns take precedence over high data rates. The LTC1483 driver slew rate is deliberately limited to reduce the high frequency electromagnetic emissions (Figures 2a and 2b) while improving signal fidelity by reducing reflections due to misterminated cables. The

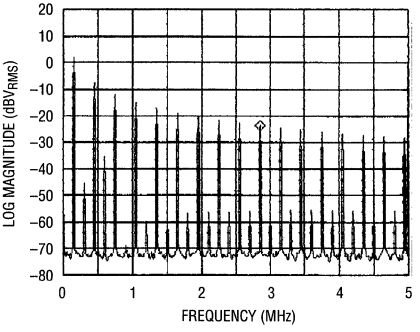

Figure 2a. Typical RS485 Driver Output Spectrum Transmitting at 150kHz

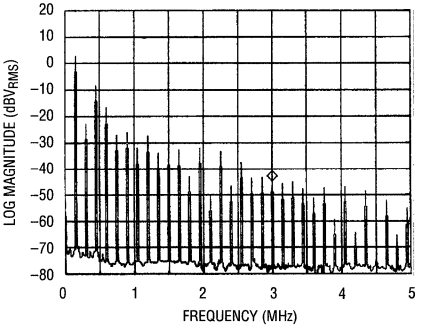

Figure 2b. Slew Rate Limited LTC1483 Driver Output Spectrum Transmitting at 150kHz

maximum operating frequency of the LTC1483 driver is limited to 250kbaud. All other performance parameters are unchanged from the LTC1481, including the low power receiver operation and the 1μA shutdown mode.

LTC1487

The LTC1487 shares the low power and low slew rate features of the LTC1483. Additionally, the LTC1487 is designed with a high input impedance of 96kΩ (typical) to allow up to 256 transceivers to share a single RS485 differential data line. This exceptionally high input impedance enables additional transceivers to be connected to a single RS485 line, reducing cabling costs and complexity in systems with many nodes.

The RS485 specification requires that a transceiver be able to drive as many as 32 "unit loads." One unit load (UL) is defined as an impedance that draws a maximum of 1mA with up to 12V across it. Most standard RS485 transceivers, including the LTC1481 and LTC1483, have an input resistance of approximately 12k, equivalent to 1UL, which limits a single RS485 bus to 32 nodes. With its high 96kΩ input impedance, the LTC1487 presents only 0.125UL to the line, allowing up to 256 transceivers (32UL/0.125UL = 256) to be connected to the data bus line without overloading the driver (Figure 3).

Conclusions

The LTC1481, LTC1483 and LTC1487 make up the third generation of the Linear Technology CMOS RS485 transceiver family, all started by the original CMOS RS485 transceiver, the LTC485. These three new devices put exceptional ruggedness features and the lowest power operation available in the industry into three unique niches in the RS485 market: high performance (LTC1481), low EMI (LTC1483) and high input impedance (LTC1487).

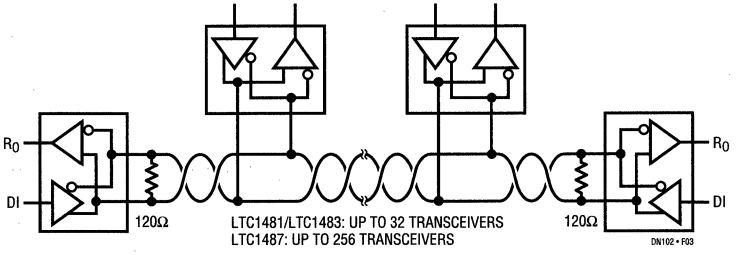

Figure 3. Mulitple Transceivers On One RS485 Bus

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LINEAR TECHNOLOGY

DESIGN NOTES

New LTC1266 Switching Regulator Provides High Efficiency at 10A Loads – Design Note 103

Greg Dittmer

The new LTC®1266 is a synchronous, step-down switching regulator controller that can drive two external, N-channel MOSFET switches. The superior performance of N-channel MOSFETs enables the LTC1266 to achieve high efficiency at loads of 10A or more with few additional components. Burst Mode™ operation provides high efficiency at light loads—efficiency is greater than 90% for loads from 10mA to 10A. The ability to provide 10A at high efficiency is critical for supplying power to Pentium™ processor applications.

The LTC1266 is based on the LTC1148 architecture and has most of the features of this successful product including constant off-time, current mode architecture with automatic Burst Mode operation. Pin selectable shutdown reduces the DC supply current to 40µA. The LTC1266 also provides pin selectable phase of the top-side driver which allows it to implement, in addition to an all N-channel step-down regulator, a low dropout regulator with high-side P-channel or a boost regulator. Other new features of the LTC1266 include an on-chip low-battery comparator, pin-defeatable Burst Mode operation, a wider voltage supply range (3.5V to 20V), 1% load regulation and a higher maximum frequency of 400kHz.

N-Channel vs P-Channel

The key to the LTC1266's ability to drive large loads at high efficiencies is its ability to drive both top-side and bottom-side N-channel MOSFETs. The superiority of N-channel MOSFETs over P-channels at high currents is due to the lower $R_{DS(ON)}$ and lower gate capacitance of the N-channel parts. To compensate for the higher $R_{DS(ON)}$, the P-channel size is usually made larger, resulting in higher gate capacitance. Efficiency is inversely proportional to both $R_{DS(ON)}$ and gate capacitance. Higher $R_{DS(ON)}$ decreases efficiency due to higher I^2R losses and limits the maximum current the MOSFET can handle without exceeding thermal limitations. Higher gate capacitance increases losses due to the increased charge required to switch the MOSFETs on and off during each switching cycle.

Nonetheless, P-channel MOSFETs still have a home in lower current and low dropout applications due to the fact they can operate at 100% duty cycle. The LTC1266 offers the capability of driving either N-channel or P-channel.

Driving N-Channel MOSFETs

P-channels have another distinct advantage—simplicity of the gate drive. Because of the negative threshold of the P-channel, the gate potential must decrease below the source (which is at V_{IN}) by at least $V_{GS(ON)}$ to turn it on. Hence, the top-side MOSFET can be gated between the available supply rail V_{IN} and ground.

Driving an N-channel top-side MOSFET isn't so straightforward. When the top-side MOSFET is turned on, the source is pulled up to V_{IN}. Because the N-channel has a positive threshold voltage, the gate must be above the source by at least $V_{GS(ON)}$. Thus, the top-side drive must swing between ground and $V_{IN} + V_{GS(ON)}$. This requires a second, higher supply rail equal to at least $V_{IN} + V_{GS(ON)}$.

There are two ways to obtain this higher rail. The most straightforward way is to use a higher rail that is already available, as is the case in most desktop systems with 12V supplies. Note that the PWR V_{IN} input to the LTC1266 is dedicated to powering the internal drivers and is separate from the main supply input. The PWR V_{IN} voltage cannot exceed 18V (20V max), limiting the input voltage to 18V – $V_{GS(ON)}$. For a converter with logic-level MOSFETs, this limits V_{IN} to about 13.5V. The PWR V_{IN} voltage must also meet its minimum requirement of $V_{IN} + V_{GS(ON)}$ (about 10V for a 5V-to-3.3V converter) in order not to burn up the high-side MOSFET due to insufficient conductance at larger output loads. If a higher supply rail is not available, a charge-pump circuit can be used to pump V_{IN} to the required level.

Basic Circuit Configurations

Figures 1 and 2 show two basic circuit configurations for the LTC1266. Figure 1 shows an LTC1266 in the charge pump configuration designed to provide a 3.3V/10A output. The Si4410s are new logic-level, surface mount N-channel MOSFETs from Siliconix that provide a mere 0.02Ω of on-resistance at V_{GS} = 4.5V, and thus provide a 10A solution with minimal components. The efficiency plot shows that the converter still is close to 90% efficient at 10A. Because the charge pump configuration is used, PWR V_{IN} = 2 × V_{IN} plus any additional ringing on the switch node. Due to the high AC currents in this circuit, we recommend low ESR OS-CON or AVX input/output capacitors to maintain efficiency and stability.

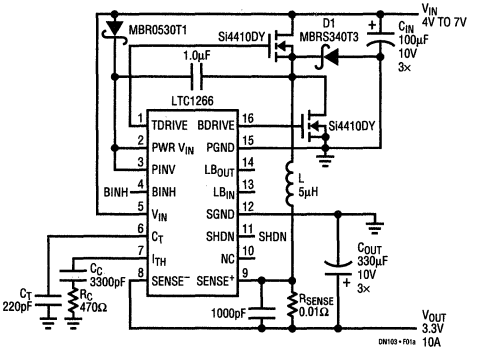

Figure 1a. All N-Channel Single Supply 5V to 3.3V/10A Regulator

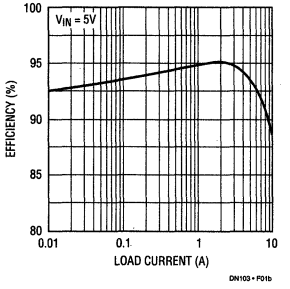

Figure 1b. Figure 1a Circuit Efficiency

The all N-channel, external PWR V_{IN} circuit shown in Figure 2 is a 3.3V/5A surface mount converter. The current sense resistor value is chosen to set the maximum current to 5A, according to the formula I_{OUT} = 100mV/R_{SENSE}. With V_{IN} = 5V, the 5µH inductor and 130pF timing capacitor provide an operating frequency of 175kHz and a ripple current of 1.25A. The $V_{GS(ON)}$ of the Si9410 N-channel MOSFETs is 4.5V; thus the minimum allowable voltage at the external PWR V_{IN} is $V_{IN(MAX)}$ + 4.5V. At the other end, PWR V_{IN} should be kept under the maximum safe level of 18V, limiting V_{IN} to 18V – 4.5V = 13.5V.

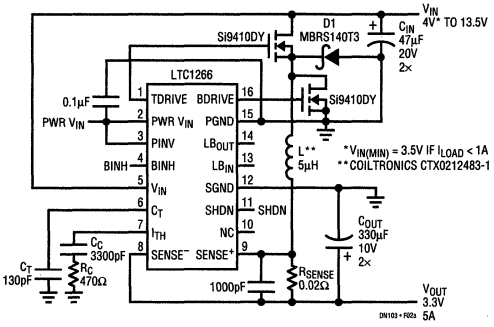

Figure 2a. All N-Channel 3.3V/5A Regulator with Drivers Powered from External Power V_{IN} Supply

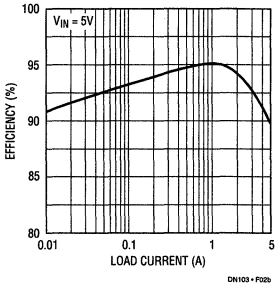

Figure 2b. Figure 2a Circuit Efficiency

The two application circuits demonstrate the fixed 3.3V version of the LTC1266. The LTC1266 is also available in fixed 5V and adjustable versions. All three versions are available in 16-pin narrow SOIC packages.

Conclusion

The new LTC1266 synchronous step-down regulator controller is the first Linear Technology synchronous controller with the ability to exploit the superior performance of N-channel MOSFETs to maximize efficiency and provide a low cost, compact solution for high current converters. The extra features provided in this product, Burst Mode inhibit and a low-battery comparator, make it ideal in a wide variety of applications.

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LINEAR TECHNOLOGY

DESIGN NOTES

LTC1410: 1.25Msps 12-Bit A/D Converter Cuts Power Dissipation and Size – Design Note 104

Dave Thomas and Kevin R. Hoskins

Introduction

Until now, high speed system designers had to compromise when selecting 1Msps 12-bit A/D converters. While hybrids typically had the best performance, they were big, power hungry (~1W) and costly (>$100). A few manufacturers offered monolithics, but they compromised either AC or DC performance.

That has now changed. The new LTC®1410 monolithic 1.25Msps 12-bit ADC performs better than hybrids with the power dissipation, size and cost of monolithics.

Some of the LTC1410's key benefits include:

- 1.25Msps throughput rate
- Fully differential inputs
- 60dB CMRR that remains constant to 1MHz
- Low power: 160mW (typ) from ±5V supplies
- "Instant on" NAP and µpower SLEEP shutdown modes
- Small package: 28-pin SO

The LTC1410's features can increase the performance and decrease the cost of current data acquisition systems and optimize new applications.

High Accuracy Conversions: AC or DC

In Figure 1 the LTC1410 combines a wide bandwidth differential sample-and-hold (S/H) with an extremely fast successive approximation register (SAR) ADC and an on-chip reference. Together they deliver a very high level of both AC and DC performance.

An ADC's S/H determines its overall dynamic performance. The LTC1410's S/H has a very wide bandwidth (20MHz) and generates very low total harmonic distortion (–84db) for the 625kHz Nyquist bandwidth.

Important DC specifications include excellent differential linearity error ≤0.8LSB, linearity error ≤0.5LSB and no missing codes over temperature. The on-chip 10ppm/°C

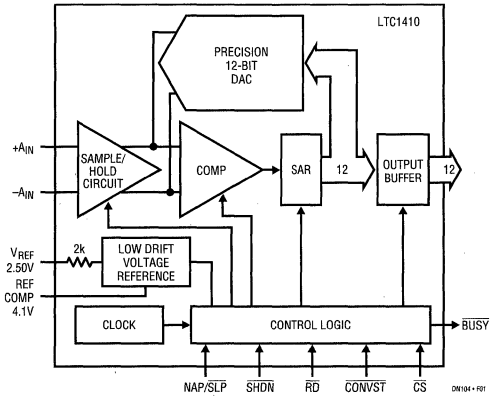

Figure 1. LTC1410 Features a True Differential S/H with Excellent Bandwidth and CMRR

curvature corrected 2.5V bandgap reference assures low drift over temperature.

If an application requires an external reference, it can easily overdrive the on-chip reference's 2kΩ output impedance.

Important Multiplexed Applications

The LTC1410's high conversion rate allows very high sample rate multiplexed systems. The S/H's high input impedance eliminates DC errors caused by a MUX's switch resistance. Also, the LTC1410's low input capacitance ensures fast 100ns acquisition times, even with high source impedance.

Ideal for Telecommunications

Telecommunications applications such as HDSL, ADSL and modems require high levels of dynamic performance. A key indicator of a sampling ADC's dynamic performance is its signal-to-noise plus distortion ratio (SINAD). The LTC1410's minimum SINAD is 72dB, or 11.67 Effective

Number of Bits (ENOB), up to input frequencies of 100kHz. At the Nyquist frequency (625kHz) the SINAD is still a robust 70dB. Figure 2 shows that the LTC1410 can undersample signals well beyond the Nyquist rate.

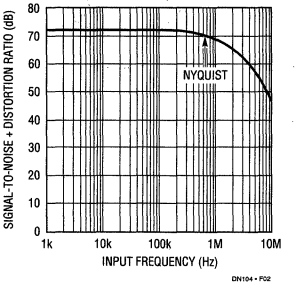

Figure 2. The Wideband S/H Captures Signals Well Beyond Nyquist

Differential Inputs Reject Noise

The LTC1410's differential inputs are ideal for applications whose desired signals must compete with EMI noise. The LTC1410's differential inputs provide a new way to fight noise.

Figure 3a shows a single-ended sampling system whose accuracy is limited by ground noise. When a single-ended signal is applied to the ADC's input, the ground noise adds directly to the applied signal. While a filter can reduce this noise, this does not work for in-band noise or common-mode noise at the same frequency as the input signal. However, Figure 3b shows how the LTC1410 provides relief. Because of its excellent CMRR, the LTC1410's differential inputs reject the ground noise even if it is at the same frequency as the desired input frequency. Further, the LTC1410's wideband CMRR can eliminate extremely wideband noise, as shown in Figure 4.

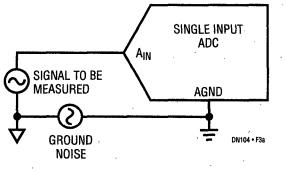

Figure 3a. An Input Signal is Contaminated by Ground Noise with a Single Input ADC

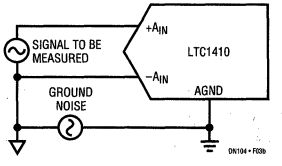

Figure 3b. The LTC1410's Differential Inputs Reject Common-Mode Noise and Preserve the Input Signal

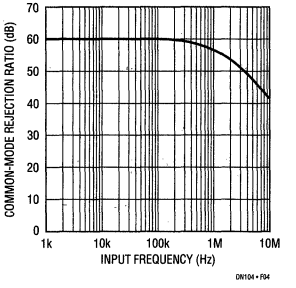

Figure 4. The LTC1410 Rejects Common-Mode Noise Out to 10MHz and Beyond

Low Power Applications

High speed applications with limited power budgets will greatly benefit from the LTC1410's low 160mW power dissipation. Power can be further reduced by using the power shutdown modes, NAP and SLEEP.

NAP reduces power consumption by 95% (to 7.5mW) leaving only the internal reference powered. The "wake-up" time is a very fast 200ns. The most recent conversion data is still accessible and $\overline{CS}$ and $\overline{RD}$ still control the output buffers. NAP is appropriate for those applications that require conversions instantly after periods of inactivity.

SLEEP reduces power consumption to less than 5µW. It is useful for applications that must maximize power savings. SLEEP mode shuts down all bias currents, including the reference. SLEEP mode wake-up time is dependent on the reference compensation capacitor's size. With the recommended 10µF, the wake-up time is 10ms. Typically, NAP mode is used for inactive periods shorter that 10ms and SLEEP is used for longer periods.

Conclusion

Available in 28-pin SO packages, the new LTC1410 is optimized for many high speed dynamic sampling applications including ADSL, compressed video and dynamic data acquisition.

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LINEAR TECHNOLOGY

DESIGN NOTES

LTC1265: A New, High Efficiency Monolithic Buck Converter

Design Note 105

San-Hwa Chee

The LTC®1265 is a 14-pin SOIC step-down converter capable of operating at frequencies up to 700kHz. High frequency operation permits the use of small inductors for size sensitive applications. The LTC1265 has an internal 0.3Ω (at a supply voltage of 10V) P-channel power MOSFET switch, which is capable of supplying up to 1.2A of output current. With no load, the converter requires only 160µA of quiescent current; this decreases to a mere 5µA in shutdown conditions. In dropout mode, the internal P-channel power MOSFET switch is turned on continuously (at DC), thereby maximizing battery life. The part is protected from output shorts by its built-in current limiting. In addition to the features already mentioned, the LTC1265 incorporates a low-battery detector.

The LTC1265 is a current mode DC/DC converter with Burst Mode™ operation. The current mode architecture gives the LTC1265 excellent load and line regulation. Burst Mode operation results in high efficiency with both high and low load currents. The LTC1265 comes in three versions: LTC1265-5 (5V output), LTC1265-3.3 (3.3V output) and LTC1265 (adjustable). All versions operate down to an input voltage of 3.5V and up to an absolute maximum of 13V.

Efficiency

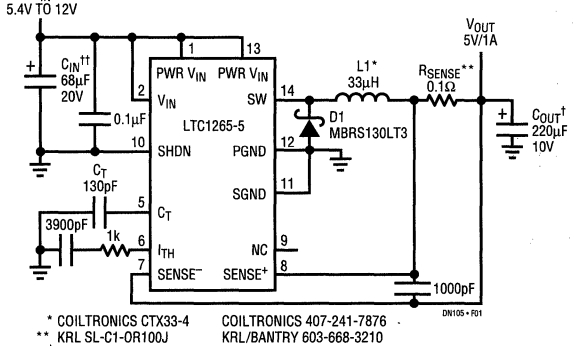
Figure 1 shows a typical LTC1265-5 application circuit. The efficiency curves for two different input voltages are shown in Figure 2. Note that the efficiency for a 6V input exceeds 90% over a load range from less than 10mA to 850mA. This makes the LTC1265 attractive for all battery-operated products and efficiency sensitive applications.

High Frequency Operation

Although the LTC1265 is capable of operation at frequencies up to 700kHz, the highest efficiency is achieved at an operating frequency of about 200kHz. As the frequency increases, losses due to the gate charge of the P-channel power MOSFET increase. In space sensitive applications, high frequency operation allows the use of smaller components at the cost of four to five efficiency points.

Constant Off-Time Architecture

The LTC1265 uses a constant off-time, current mode architecture. This results in a power supply that has very high efficiency over a wide load current range, fast transient response and very low dropout characteristics. The



* COILTRONICS CTX33-4 COILTRONICS 407-241-7876
** KRL SL-C1-0R100J KRL/BANTRY 603-668-3210
† AVX TPSE227K010
†† AVX TPSE686K020

Figure 1. High Efficiency 5V/1A Step-Down Converter

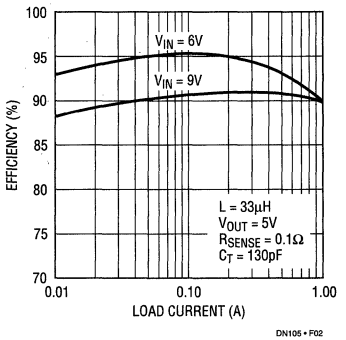


Figure 2. Efficiency vs Load Current

off-time is set by an external timing capacitor C_T and is constant whenever the output is in regulation. When the output is not in regulation, the off-time is inversely proportional to the output voltage. By using a constant off-time scheme, the inductor's ripple current is predictable and well controlled under all operating conditions, making the selection of the inductor much easier. The inductor's peak-to-peak ripple current is inversely proportional to the inductance in continuous mode. If a lower ripple current is desired, a larger inductor can be used for a given value of timing capacitor.

100% Duty Cycle in Dropout Mode

When the input voltage decreases, the switching frequency decreases. With the off-time constant, the on-time is increased to maintain the same peak-to-peak ripple current in the inductor. When the input-to-output voltage differential drops below 2.0V, the off-time is reduced. This prevents the operating frequency from dropping below 20kHz as the regulator approaches the dropout region. As the input voltage drops further, the P-channel switch is turned on for 100% of the cycle. The dropout voltage is governed by the switch resistance, load current and current sense resistor.

Good Start-Up and Transient Behavior

The LTC1265 exhibits excellent start-up behavior when it is initially powered on or recovering from a short circuit. This is achieved by making the off-time inversely proportional to the output voltage while the output is still in the process of reaching its regulated value. When the output is shorted to ground, the off-time is extended long enough to prevent inductor current runaway. When the short is removed, the output capacitor begins to charge and the off-time gradually decreases.

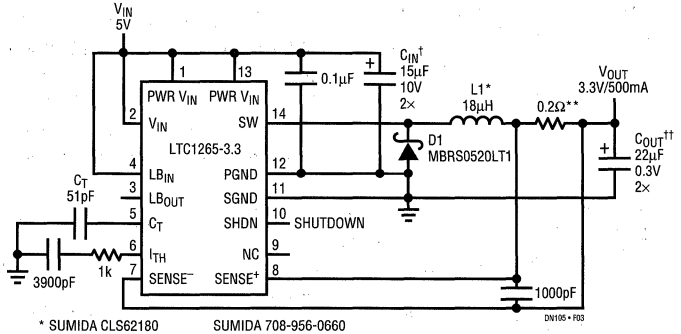
In addition, the LTC1265 has excellent load transient response. When the load current drops suddenly, the feedback loop responds quickly by turning off the internal P-channel switch. Sudden increases in output current will be met initially by the output capacitor, causing the output voltage to drop slightly. Tight control of the inductor's current, as mentioned above, means that output voltage overshoot and undershoot are virtually eliminated.

2.5mm Typical Height 5V-to-3.3V Regulator

Figure 3 shows the schematic for a very thin 5V-to-3.3V converter. For the LTC1265 to be able to source 500mA output current and yet meet the height requirement, a small value inductor must be used. The circuit operates at a high frequency (typically 500kHz), increasing the gate charge losses.

Conclusion

The LTC1265, with its low dropout and high efficiency, is ideal for battery-operated products and efficiency sensitive applications. In addition, its ability to operate at high frequencies allows the use of small inductors for size sensitive applications.



* SUMIDA CLS62180 SUMIDA 708-956-0660
** KRL SL-C1-0R200J KRL/BANTRY 603-668-3210
† AVX TAJB155K010
†† AVX TAJB225K06

Figure 3. 2.5mm High 5V-to-3.3V Converter (500mA Output Current)

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LINEAR TECHNOLOGY

DESIGN NOTES

The LTC1392: Temperature and Voltage Measurement in a Single Chip – Design Note 106

Ricky Chow and Dave Dwelley

Introduction

The LTC®1392 is a new micropower, multifunction data acquisition system designed to measure ambient temperature, system power supply voltage and power supply current or differential input voltage. No external components are required for temperature or voltage measurements, and current measurements can be made with a single low value external resistor. An on-board 10-bit A/D converter provides a digital output through a 3- or 4-wire serial interface. Supply current is only 350µA when performing a measurement; this automatically drops to less than 1µA when the chip is not converting. The LTC1392 is designed to be used for PC board temperature and supply voltage/current monitoring or as a remote temperature and voltage sensor for monitoring almost any kind of system. It is available in SO-8 and DIP packages allowing it to fit onto almost any circuit board.

Measurement Performance

Wafer level trimming allows the LTC1392 to achieve guaranteed accuracy of ±2°C at room temperature and ±4°C over the entire operating temperature range. The 10-bit A/D converter gives 0.25° resolution over the 0°C to 70°C (LTC1392C) or –40°C to 85°C (LTC1392I) range. Temperature is output as (ADC code/4) – 130°C with a theoretical maximum range of –130°C to 125.75°C. Figure 1 shows the typical output temperature error of the LTC1392 over temperature.

In supply voltage monitor mode, the A/D converter makes a differential measurement between the 2.42V reference and the actual power supply voltage. Each LSB step is equal to approximately 4.727mV, giving a theoretical measurement range of 2.42V to 7.2V. The LTC1392 has guaranteed accuracy over a voltage range of 4.5V to 6V, with a total absolute error of ±25mV or ±40mV respectively, over the commercial or industrial temperature range.

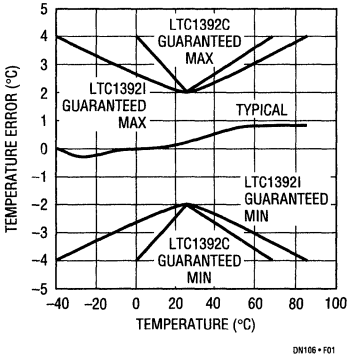

Figure 1. Output Temperature Error

Voltage is output as (ADC code × 4.727mV) + 2.42V. Figure 2 shows typical integral and differential nonlinearity performance of V_{CC} measurement.

The differential voltage input mode can be configured to operate in either 1V or 0.5V unipolar full-scale mode. Each mode converts the differential voltage between input pins V^+ and V^- directly to bits with the output code equal to ADC code × (full scale/1024). The 1V mode is specified at 8 bits accuracy with the eighth bit accurate to ±0.5LSB or ±2mV, while the 0.5V full-scale mode is specified to seven bits accuracy ±0.5LSB, giving the same ±2mV accuracy. The differential inputs include a common-mode input range including both power supply rails allowing them to be used to measure the voltage across a sense resistor in either leg of the power supply. They can also be used to make a unipolar differential transducer bridge measurement or to make a single-ended voltage measurement by grounding the V^- pin.

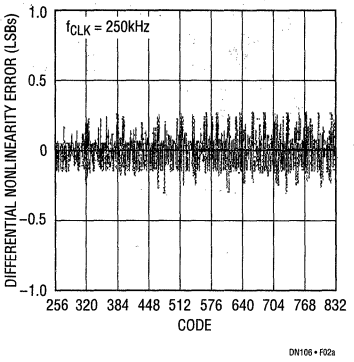

Figure 2a. Differential Nonlinearity, Power Supply Voltage Mode

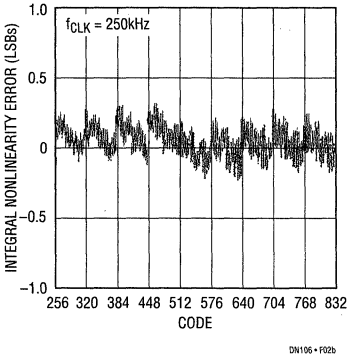

Figure 2b. Integral Nonlinearity, Power Supply Voltage Mode

The serial interface in the LTC1392 allows all of its functionality to be implemented in an 8-pin SO or DIP package and makes connection easy to virtually any MPU. Four pins are dedicated to the serial interface: active low chip select ($\overline{CS}$), clock (CLK), data input (D_{IN}) and data output (D_{OUT}). The D_{IN} pin is used to configure the LTC1392 for the next measurement and the D_{OUT} pin outputs the A/D conversion data. The D_{IN} pin is disabled after a valid configuration word is received and the D_{OUT} pin is in three-state mode until a valid configuration word is recognized, allowing the two pins to be tied together in a 3-wire system. The serial link allows several devices to be attached to a common serial bus, with separate $\overline{CS}$ lines to select the active chip.

Typical Application

A typical LTC1392 application is shown in Figure 3. A single point "star" ground is used along with a ground plane to minimize errors in the voltage measurements. The power supply is bypassed directly to the ground plane with a 1µF tantalum capacitor in parallel with a 0.1µF ceramic capacitor.

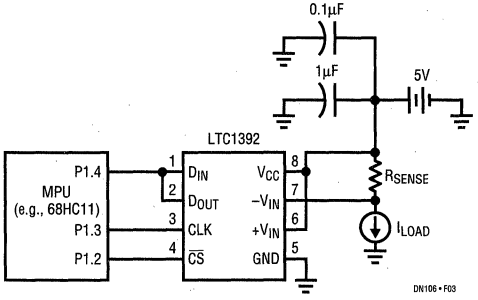

Figure 3. Typical Application

Conclusion

The LTC1392 provides a versatile data acquisition and environmental monitoring system with an easy-to-use interface. Its low supply current, coupled with space-saving SO-8 or DIP packaging make the LTC1392 ideal for systems which require temperature, voltage and current measurement while minimizing space, power consumption and external component count. The combination of temperature and voltage measuring capability on one chip make the LTC1392 unique in the market providing the smallest, lowest power multifunction data acquisition system available.

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LINEAR TECHNOLOGY

DESIGN NOTES

C-Load™ Op Amps Conquer Instabilities – Design Note 107

Kevin R. Hoskins

Introduction

Linear Technology Corporation has taken advantage of advances in process technology and circuit innovations to create a series of C-Load operational amplifiers that are tolerant of capacitive loading, including the ultimate, amplifiers that remain stable driving any capacitive load. This series of amplifiers has a bandwidth that ranges from 160kHz to 140MHz. These amplifiers are appropriate for a wide range of applications from coaxial cable drivers to analog-to-digital converter (ADC) input buffer/amplifiers.

Driving ADCs

Most contemporary ADCs incorporate a sample-and-hold (S/H). A typical S/H circuit is shown in Figure 1. The hold capacitor's (C1) size varies with the ADC's resolution but is generally in the range of 5pF to 20pF, 10pF to 30pF and 10pF to 50pF for 8-, 10- and 12-bit ADCs, respectively.

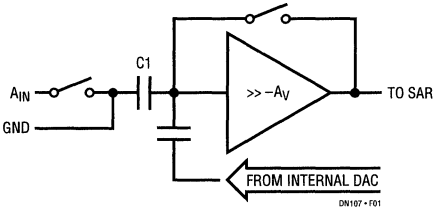

Figure 1. Typical ADC Input Stage Showing Input Capacitors

At the beginning of a conversion cycle, this circuit samples the applied signal's voltage magnitude and stores it on its hold capacitor. Each time the switch opens or closes, the amplifier driving the S/H's input faces a dynamically changing capacitive load. This condition generates current spikes on the input signal. This capacitive load and the spikes produced when they are switched constitutes a very challenging load that can potentially produce instabilities in an amplifier driving the ADC's input. These instabilities make it difficult for an amplifier to quickly settle. If the output of an amplifier has not settled to a value that falls within the error band of the ADC, conversion errors will result. That is unless the amplifier is designed to gracefully and accurately drive capacitive loads, such as Linear Technology's C-Load line of monolithic amplifiers. Table 1 lists Linear Technology's unconditionally stable voltage feedback C-Load amplifiers. Table 2 lists other voltage feedback C-Load amplifiers that are stable with loads up to 10,000pF.

Table 1. Unity-Gain Stable C-Load Amplifiers Stable with All Capacitive Loads

SINGLES	DUALS	QUADS	GBW (MHz)	I_S/AMP (mA)
—	LT®1368	LT1369	0.16	0.375
LT1200	LT1201	LT1202	11	1
LT1220	—	—	45	8
LT1224	LT1208	LT1209	45	7
LT1354	LT1355	LT1356	12	1
LT1357	LT1358	LT1359	25	2
LT1360	LT1361	LT1362	50	4
LT1363	LT1364	LT1365	70	6

Table 2. Unity-Gain Stable C-Load Amplifiers Stable with $C_L \leq 10{,}000pF$

SINGLES	DUALS	QUADS	GBW (MHz)	I_S/AMP (mA)
LT1012	—	—	0.6	0.4
—	LT1112	LT1114	0.65	0.32
LT1097	—	—	0.7	0.35
—	LT1457	—	2	1.6

Remaining Stable in the Face of Difficult Loads

As can be seen in Figure 2, an amplifier whose design is not optimized for handling a large capacitive load, has some trouble driving the hold capacitor of the LTC®1410's S/H. While the LT1006 has other very desirable characteristics such as very low V_{OS}, very low offset drift, and low

power dissipation, it has difficulty accurately responding to dynamically changing capacitive loads and the current glitches and transients they produce (as indicated by the instabilities that appear in the lower trace of Figure 2a.

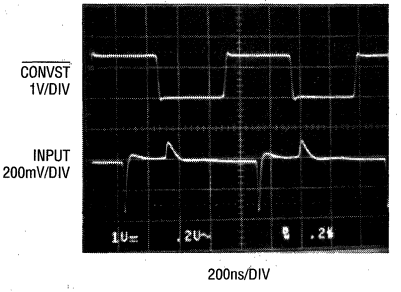

Figure 2a. Input Signal Applied to an LTC1410 Driven by an LT1006

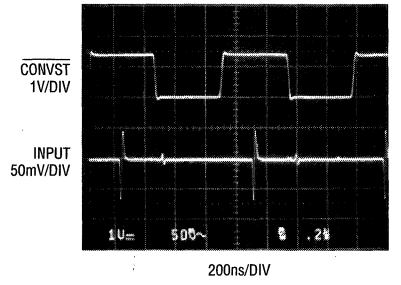

Figure 2b. Input Signal Applied to an LTC1410 Driven by an LT1360

By contrast, Figure 2b shows the LT1360 C-Load op amp driving the same LTC1410 input. The photo shows that the LT1360 is an ideal solution for driving the ADC's input capacitor quickly and cleanly with excellent stability. Its wide 50MHz gain-bandwidth and 800V/µs slew rate very adequately complement the LTC1410's 20MHz full power bandwidth. The LT1360 is specified for ±5V operation.

Figure 3 shows the circuit used to test the performance of op amps driving the LTC1410's input and measure the input waveforms.

Conclusion

Linear Technology's C-Load amplifiers meet the challenging and difficult capacitive loads of contemporary ADC analog inputs by remaining stable and settling quickly.

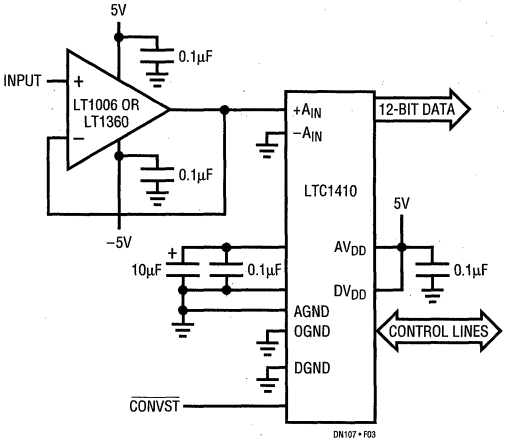

Figure 3. Test Circuit Used to Measure LTC1410 Input Signal Waveform

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LINEAR TECHNOLOGY

DESIGN NOTES

250kHz, 1mA I_Q Constant Frequency Switcher Tames Portable Systems Power – Design Note 108

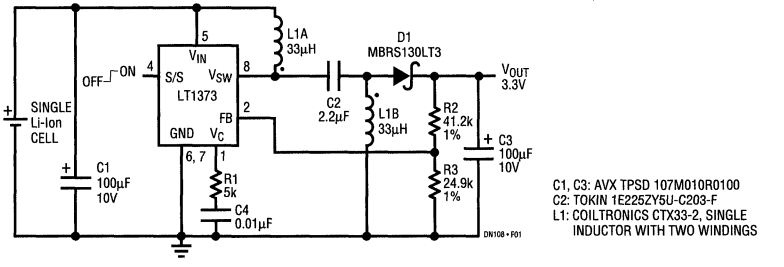
Bob Essaff

DC-to-DC power conversion remains one of the toughest tasks for portable system designers. Dealing with various battery technologies and output voltage requirements dictate the need for creative circuit solutions. The two circuits discussed are tailored for operation from a single lithium-ion (Li-Ion) cell. These new batteries are finding widespread use due to their high energy storage capabilities. The first circuit has a 3.3V output and the second circuit has both 5V and –5V outputs for applications requiring dual supplies.

At the heart of each circuit is the LT®1373 current mode switching regulator. Guaranteed to operate down to 2.7V, this part allows the full energy storage capacity of a single Li-Ion battery to be used. The LT1373 draws only 1mA of quiescent current for high efficiency at light loads and has a low resistance 1.5A switch for good efficiency at higher loads. Switching at 250kHz saves space by reducing the size of the magnetics, and the fixed-frequency switching also reduces the noise spectrum generated. To avoid sensitive system frequencies the part can be externally synchronized to a specific frequency from 300kHz to 360kHz. The LT1373 can also be shut down where it draws only 12µA supply current.

3.3V SEPIC Converter

Generating a 3.3V output from a single Li-Ion cell is not straight forward because at full charge the battery voltage is above the output voltage and when discharged, the battery voltage is below the output voltage. A conventional buck or boost regulator topology will not work. The circuit in Figure 1 uses the SEPIC (single-ended primary inductance converter) topology which allows the input voltage to be higher or lower than the output voltage. The circuit's two inductors, L1A and L1B, are actually two identical windings on the same inductor core, though two individual inductors can be used. The topology is essentially identical to a 1:1 transformer-flyback circuit except for the addition of capacitor C2 which forces identical AC voltages across both windings. This capacitor performs three tasks. First, it eliminates the power loss and spikes created by flyback-converter leakage inductance. Secondly, it forces the input current to be a triangular waveform riding on top of a DC component instead of forming a large amplitude square wave. Finally, it eliminates the voltage spike across the output diode when the switch turns on. Another feature of the SEPIC topology is that, unlike a typical boost converter, there is no DC path from the input to the output. This means that when the LT1373 is shut down, the load is completely disconnected from the input power source. Figure 2 shows that the 3.3V SEPIC converter maintains reasonable efficiency over two decades of output load current even though 3.3V circuits typically have low efficiency due to catch diode losses.



C1, C3: AVX TPSD 107M010R0100
C2: TOKIN 1E225ZY5U-C203-F
L1: COILTRONICS CTX33-2, SINGLE INDUCTOR WITH TWO WINDINGS

Figure 1. Single Li-Ion Cell to 3.3V SEPIC Converter

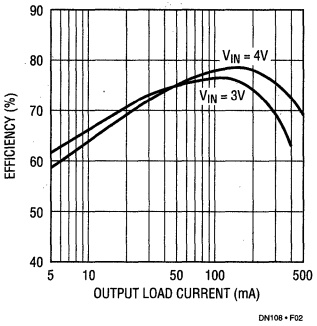


Figure 2. 3.3V Efficiency

Dual Output Converter

Many portable systems still require a negative bias voltage to operate interface or other circuitry, where the voltage accuracy is not critical. Using a single inductor, the circuit in Figure 3 generates a regulated 5V output and a quasi-regulated –5V output for such applications. The circuit first converts a single Li-Ion cell input voltage to a well-regulated 5V output. It then takes advantage of the switching waveform on the V_{SW} pin to generate the –5V output in a charge pump fashion. The voltage on the V_{SW} pin is 5V plus D1's forward voltage when V_{SW} is high. At this time, C3 charges to the V_{SW} voltage minus D2's forward voltage or about 5V. When the V_{SW} pin goes low, the minus side of C3 goes to –5V which turns on D3 and charges C5 to –5V. This generates a –5V supply which is only quasi-regulated due to diode drop and switch saturation losses. Figure 4 shows the regulation of the negative output for various positive output load currents. As shown in Figure 5, the dual output converter has high efficiency over two decades of load current.

For more information, please consult the LT1373 data sheet. For parts similar to the LT1373 with higher switching frequencies (500kHz and 1MHz), consult the LT1372/LT1377 data sheet.

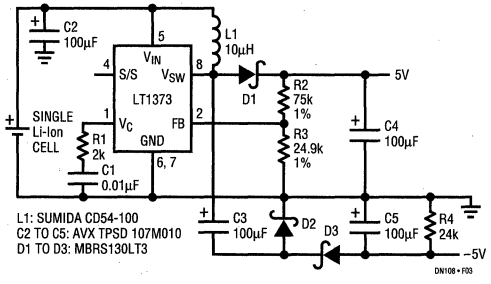


Figure 3. Single Li-Ion to ±5V

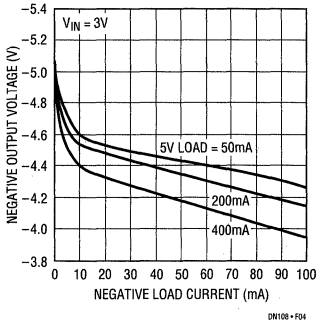


Figure 4. –5V Regulation

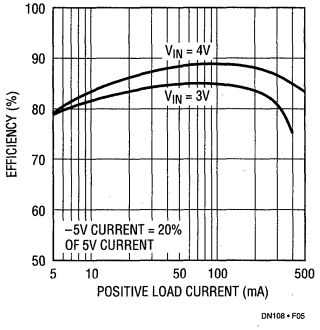


Figure 5. Dual Output Efficiency

For literature on our Switching Regulators, call **1-800-4-LINEAR**. For applications help, call (408) 432-1900, Ext. 361

LINEAR TECHNOLOGY

DESIGN NOTES

Micropower Buck/Boost Circuits, Part 1: Converting Three Cells to 3.3V* – Design Note 109

Mitchell Lee

Two combinations of cell count and output voltage are to be strictly avoided: three cells converted to 3.3V and four cells converted to 5V. These combinations are troublesome because no ordinary regulator (boost, buck or linear) can accommodate a situation where the input voltage range overlaps the desired output voltage.

This design note presents four circuits capable of solving the 3-cell dilemma. Design Note 110 will discuss 4-cell, 5V circuits. The LT®1303 and LT1372 high efficiency DC/DC converters are used throughout, giving a fair comparison of each topology's efficiency. The LT1303 is optimized for battery operation and includes a low-battery detector which is required to implement one of the topologies. The LT1372 500kHz converter is used for compact layouts at higher current levels.

You can expect 200mA output from LT1303 based circuits and 300mA from the LT1372 circuit without modification. All of the circuits feature output disconnect; in shutdown the outputs fall to 0V. The input range of LT1303 based converters extends well beyond the 3-cell source shown. These function at 1.8V, and although not fully characterized for efficiency, can accept inputs of up to 10V. The LT1372 converter operates from 2.7V to 10V.

*For 4-cell to 5V buck/boost circuits, see Design Note 110.

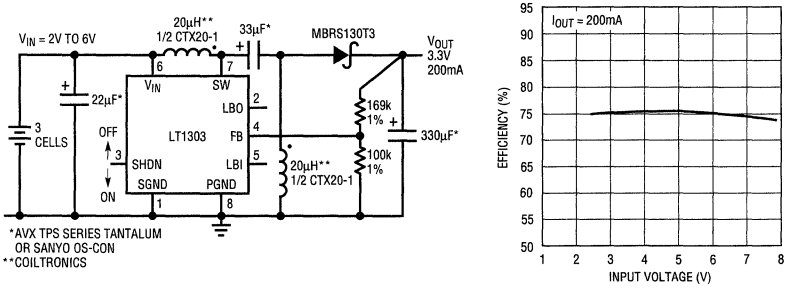


Figure 1. 3-Cell to 3.3V SEPIC

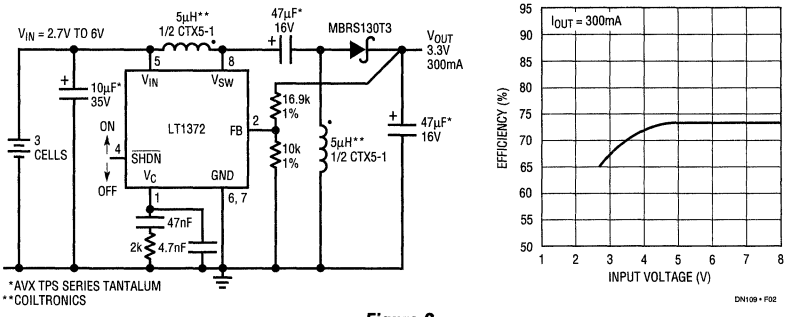


Figure 2

The circuits in Figures 1 and 2 are based on the SEPIC (Single-Ended Primary Inductance Converter) topology. Although not stellar, the efficiency is quite consistent over a wide input voltage range. Peculiar to the SEPIC topology is its use of two inductors. These, however, are wound together on a single core and consume no more space than a simple 2-terminal inductor of similar rating. A wide selection of stock 2-winding, 4-terminal inductors are available from Coiltronics and other magnetics vendors.

Peak efficiency improves in Figure 3 using a bipolar buck/boost topology. This circuit is essentially a boost converter with a linear post regulator. For $V_{IN} < V_{OUT}$, the LT1303 boosts the input driving the bipolar emitter just high enough to maintain the desired output voltage—the transistor is saturated. For $V_{IN} > V_{OUT}$, the LT1303 drives the emitter to a value just higher than the *input voltage* sufficient to develop the base current necessary to support any load current. In this condition the transistor serves as a linear post regulator, cascoding the output of the boost converter and dissipating power as would any linear regulator.

Highest peak efficiency is obtained with the circuit in Figure 4 using a MOSFET buck/boost converter. For $V_{IN} < V_{OUT}$, the circuit operates as a boost converter and the MOSFET, driven by the LT1303's low-battery detector/amplifier, is held 100% ON. The output voltage is developed and controlled by the boost converter.

For $V_{IN} > V_{OUT}$, the boost function can no longer control the output voltage and it begins to rise. Staggered feedback (R3, R4, R5) allows the low-battery detector/amplifier to take control using the MOSFET as a linear pass element. Because the MOSFET requires no base drive, and because it has such a low ON resistance, the efficiency peaks at well over 90%. Furthermore, the efficiency peak occurs in the vicinity of a NiCd's nominal terminal voltage of $3 \times 1.25 = 3.75V$, right where the efficiency is needed most.

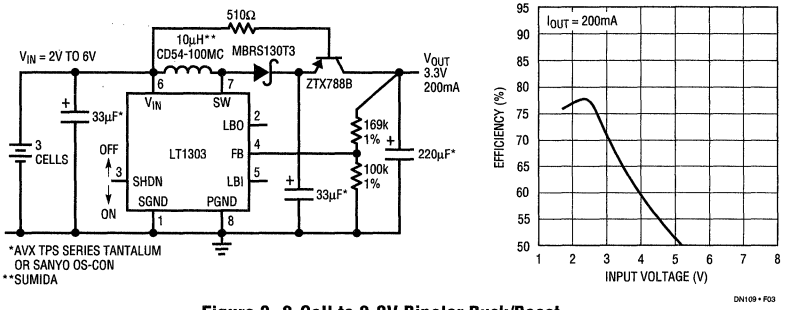


Figure 3. 3-Cell to 3.3V Bipolar Buck/Boost

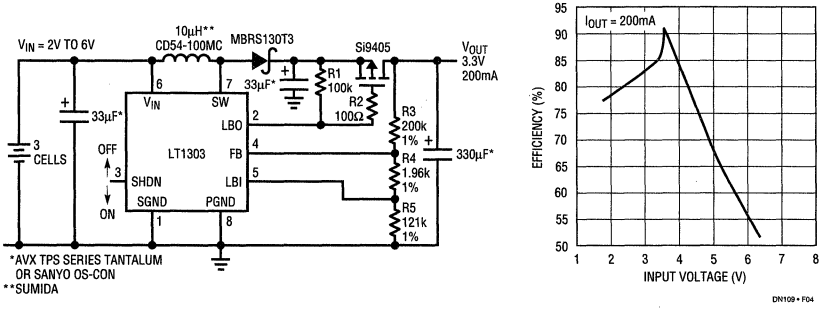


Figure 4. 3-Cell to 3.3V MOSFET Buck/Boost

For literature on our DC/DC Converters, call **1-800-4-LINEAR**. For applications help, call (408) 432-1900, Ext. 361

LINEAR TECHNOLOGY

DESIGN NOTES

Micropower Buck/Boost Circuits, Part 2: Converting Four Cells to 5V* – Design Note 110

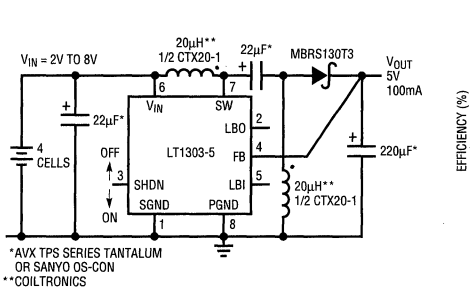
Mitchell Lee

Two combinations of cell count and output voltage are to be strictly avoided: three cells converted to 3.3V and four cells converted to 5V. These combinations are troublesome because no ordinary regulator (boost, buck or linear) can accommodate a situation where the input voltage range overlaps the desired output voltage.

This design note presents four circuits capable of solving the 4-cell dilemma. Design Note 109 discussed 3-cell, 3.3V circuits. The LT®1303 and LT1372 high efficiency DC/DC converters are used throughout, giving a fair comparison of each topology's efficiency. The LT1303 is optimized for battery operation and includes a low-battery detector which is required to implement one of the topologies. The LT1372 500kHz converter is used for compact layouts at higher current levels.

You can expect 100mA output from LT1303 based circuits and 300mA from the LT1372 circuit without modification. All of the circuits feature output disconnect; in shutdown the outputs fall to 0V. The input range of LT1303 based converters extends well beyond the 3-cell source shown. These function at 1.8V, and although not fully characterized for efficiency, can accept inputs of up to 10V. The LT1372 converter operates from 2.7V to 10V.

*For 3-cell to 3.3V buck/boost circuits, see Design Note 109.



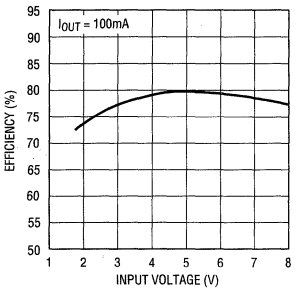
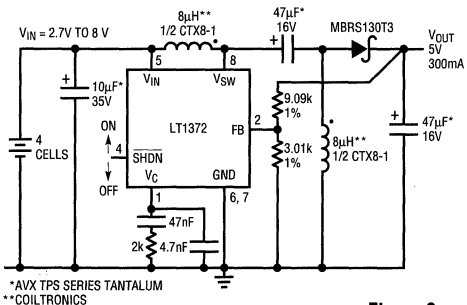


Figure 1. 4-Cell to 5V SEPIC



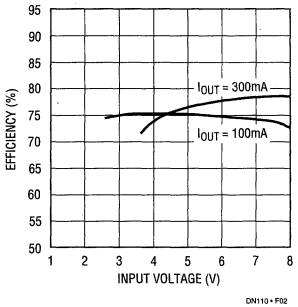


Figure 2

The circuits in Figures 1 and 2 are based on the SEPIC (Single-Ended Primary Inductance Converter) topology. Although not stellar, the efficiency is quite consistent over a wide input voltage range. Peculiar to the SEPIC topology is its use of two inductors. These, however, are wound together on a single core and consume no more space than a simple 2-terminal inductor of similar rating. A wide selection of stock 2-winding, 4-terminal inductors are available from Coiltronics and other magnetics vendors.

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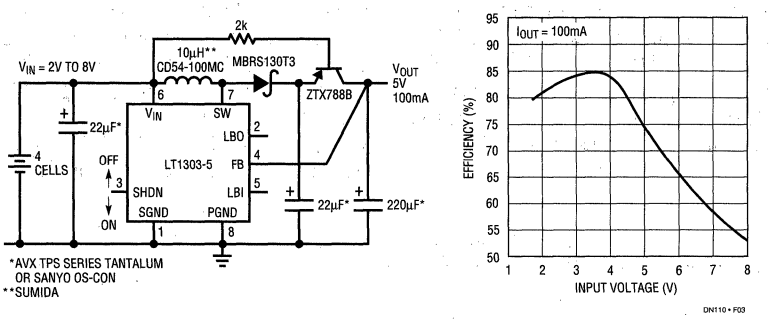

Figure 3. 4-Cell to 5V Bipolar Buck/Boost

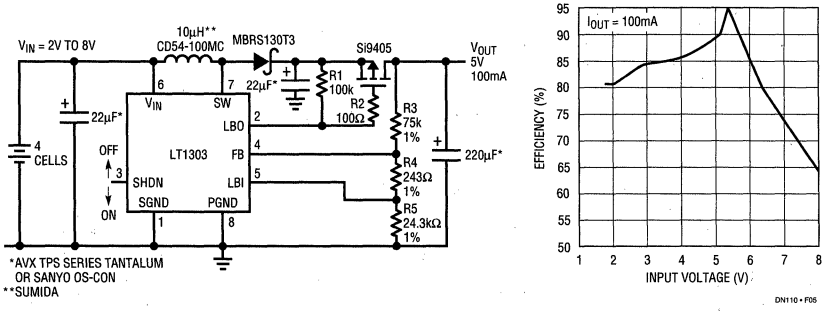

Figure 4. 4-Cell to 5V MOSFET Buck/Boost

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LINEAR TECHNOLOGY

DESIGN NOTES

LT1510 High Efficiency Lithium-Ion Battery Charger

Design Note 111

Chiawei Liao

The LT®1510 current mode PWM battery charger is the simplest, most efficient solution for fast charging modern rechargeable batteries including lithium-ion (Li-Ion), nickel-metal-hydride (NiMH) and nickel-cadmium (NiCd) that require constant current and/or constant voltage charging. The internal switch is capable of delivering 1.5A DC current (2A peak current). The onboard current sense resistor (0.1Ω) makes the charge current programming very simple. One resistor (or a programming current from a DAC) is used to set the charging current to within 5% accuracy. With 0.5% reference voltage accuracy, the LT1510 16-lead S package meets the critical constant voltage charging requirement for lithium cells.

The LT1510 can charge batteries ranging from 1V to 20V. A blocking diode is not required between the chip and the battery because the chip goes into sleep mode and drains only 3μA when the wall adaptor is unplugged. Soft start and shutdown features are also provided.

Lithium-Ion Battery Charger

The circuit in Figure 1 uses the 16-lead LT1510 to charge lithium-ion batteries at a constant 1.3A until battery voltage reaches 8.4V set by R3 and R4. The charger will then automatically go into a constant voltage mode with current decreasing toward near zero over time as the battery reaches full charge. This is the normal regimen for lithium-ion charging, with the charger holding the battery at "float" voltage indefinitely. In this case, no external sensing of full charge is needed. Figure 2 shows typical charging characteristics.

The battery DC charging current is programmed by a resistor R_{PROG} (or a DAC output current) at the PROG pin. High DC accuracy is achieved with averaging capacitor C_{PROG}. The basic formula for full charging current is:

$$I_{BAT} = (I_{PROG})(2000) = (2.465/R_{PROG})(2000)$$
$$= (2.465/3.83k)(2000) = 1.3A$$

Approximately 0.25mA flows out of the BAT pin at all times when adapter power is applied. Therefore, to ensure a regulated output even when the battery is removed, the voltage divider current should be set at 0.5mA. Q3 is used to eliminate this current drain when adapter power is off, with a 47k resistor to pull its gate low.

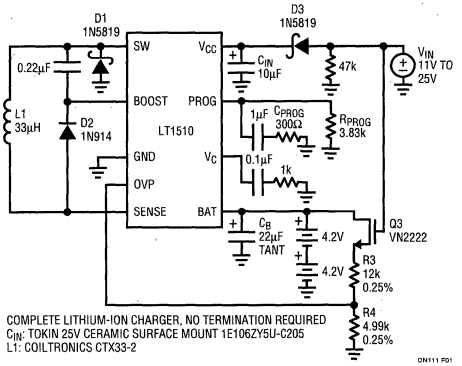


Figure 1. Charging Lithium-Ion Batteries (Efficiency at 1.3A = 86%)

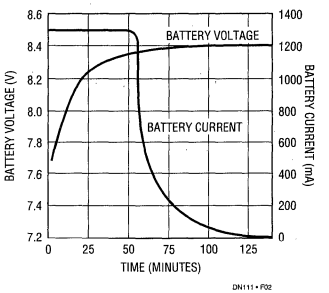


Figure 2. Battery Charging Characteristics

With divider current set as 0.5mA, R4 = 2.465/0.5mA = 4.93k, let R4 = 4.99k:

$$R3 = R4\left(\frac{V_{BAT}}{2.465} - 1\right) = 4.99k\left(\frac{8.4}{2.465} - 1\right) = 12k$$

V_{IN} has to be at least 3V higher than battery voltage and between 8.5V to 25V.

Lithium-ion batteries typically require float voltage accuracy of 1% to 2%. The LT1510 OVP voltage has 0.5% accuracy at 25°C and 1% over full temperature. This may suggest that very accurate (0.1%) resistors are needed for R3 and R4. Actually, in float mode the charging currents have tapered off to a low value and the LT1510 will rarely heat up past 50°C, so 0.25% resistors will provide the required level of overall accuracy.

Thermal Calculations

Although the battery charger achieves efficiency of approximately 86% at 1.3A, a thermal calculation should be done to ensure that junction temperature will not exceed 125°C. Power dissipation in the IC is caused by bias and driver current, switch resistance, switch transition losses and the current sense resistor. The 16-lead SO, with a thermal resistance of 50°C/W, can provide a full 1.5A charging current in many situations. Figure 3 shows the efficiency for charging currents up to 1.5A.

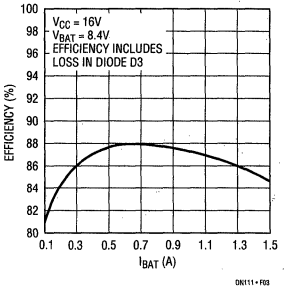


Figure 3. Efficiency of Figure 1 Circuit

$$P_{BIAS} = (3.5mA)(V_{CC}) + (1.5mA)(V_{BAT}) + \frac{(V_{BAT})^2(7.5mA + 0.012 \bullet I_{BAT})}{V_{CC}}$$

$$P_{DRIVE} = \frac{(I_{BAT})(V_{BAT})^2}{50\ (V_{CC})}$$

$$P_{SWITCH} = \frac{(I_{BAT})^2(R_{SW})(V_{BAT})}{V_{CC}} + (T_{OL})(V_{CC})(I_{BAT})$$

$$P_{SENSE} = (0.18\Omega)(I_{BAT})^2$$

R_{SW} = Switch on resistance ≈ 0.35Ω
T_{OL} = Effective switch overlap time ≈ 10ns
$V_{CC} = V_{IN} - 0.4V$

Example: V_{IN} = 16V, V_{BAT} = 8.4V, I_{BAT} = 1.3A

$$P_{BIAS} = (3.5mA)(15.6) + (1.5mA)(8.4) + \frac{(8.4)^2(7.5mA + 0.012 \bullet 1.3)}{15.6} = 0.10W$$

$$P_{DRIVE} = \frac{(1.3)(8.4)^2}{50\ (15.6)} = 0.12W$$

$$P_{SWITCH} = \frac{(1.3)^2(0.35)(8.4)}{15.6} + (10^{-8})(15.6)(1.3)(200kHz) = 0.36W$$

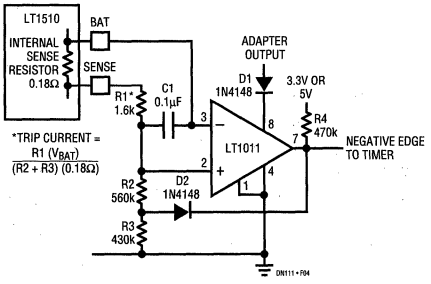
$$P_{SENSE} = (0.18)(1.3)^2 = 0.30W$$

Total power in the IC is 0.1 + 0.12 + 0.36 + 0.30 = 0.88W

Temperature rise in the IC will be: (50°C/W)(0.88W) = 44°C

Some battery manufacturers recommend termination of constant voltage float mode 30 to 90 minutes after charging current has dropped below a specified level (typically 50mA to 100mA). Check with the manufacturers for details. The circuit in Figure 4 will detect when charging current has dropped below 75mA. This logic signal is used to initiate a timeout period, after which the LT1510 can be shut down by pulling the V_C pin low with an open collector or drain. Some external means may be used to detect the need for additional charging or the charger may be turned on periodically to complete a short float voltage cycle. The current trip level is determined by the battery voltage, R1 through R3, and the internal LT1510 sense resistor (≈ 0.18Ω pin-to-pin). D2 generates hysteresis in the trip level to avoid multiple comparator transitions. R2 and R3 are chosen to total about 1M to minimize battery loading. D2 is assumed to be off during high current charging when the comparator output is high. To ensure this, the ratio of R2 to R3 is chosen to make the center node voltage less than the logic supply. R4 is somewhat arbitrary and does not affect trip point. R1 is adjusted to set the trip level:

$$R1 = \frac{(I_{TRIP})(R2 + R3)(0.18\Omega)}{V_{BAT}} = \frac{(75mA)(560k + 430k)(0.18)}{8.4V} = 1.6k$$



For literature on our Battery Chargers, call **1-800-4-LINEAR**. For applications help, call (408) 432-1900, Ext. 361

LINEAR TECHNOLOGY

DESIGN NOTES

LTC1390: A Versatile 8-Channel Multiplexer – Design Note 112

Kevin R. Hoskins

Introduction

Available in either 16-pin DIP or narrow body SOIC packages, the CMOS LTC®1390 is a high performance 8-to-1 analog multiplexer. It is addressed through a 3-wire digital interface featuring bidirectional serial data.

The LTC1390 features a typical on-resistance of 45Ω, typical switch leakage of 50pA and guaranteed break-before-make switch operation. Charge injection is ±10pC (max). All digital inputs remain logic compatible whether operating on single or dual supplies. The inputs are robust, easily withstanding 100mA fault currents. The LTC1390 operates over a wide power supply voltage range of 3V to ±15V.

Low Power, Daisy-Chain Serial Interface, 8-Channel A/D System

Figure 1 shows the LTC1390 connected to the LTC1286 12-bit micropower A/D converter. The Clock (CLK) and Chip Select ($\overline{CS}$) signals are connected in parallel to the LTC1390 and LTC1286. Both the LTC1390 and the LTC1286 are designed for serial data transfer. The LTC1390 also includes provisions for daisy-chain operation. This

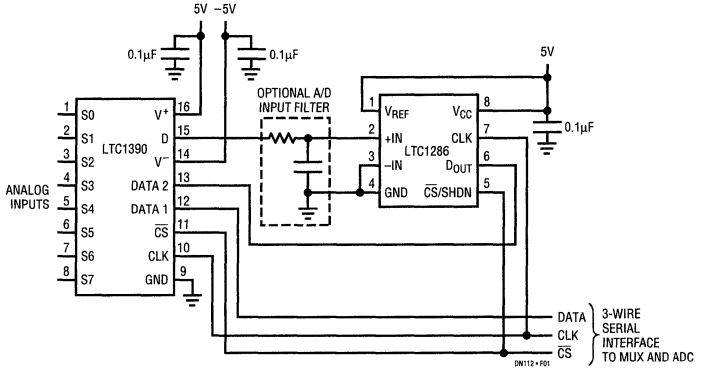


Figure 1. The LTC1390 Expands the 12-Bit Micropower LTC1286 ADC Input Capacity to Eight Channels

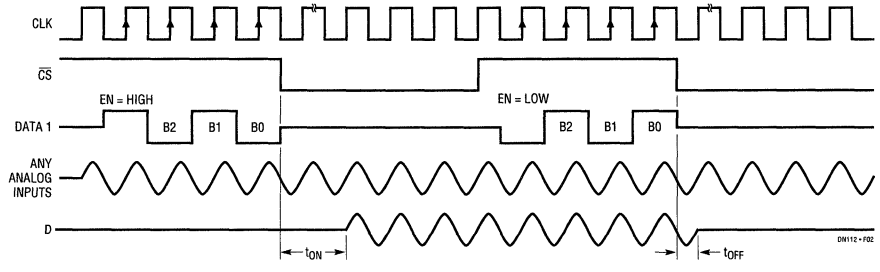


Figure 2. The LTC1390 Clocks in Data While $\overline{CS}$ is High and Latches the Data, Enabling the Selected Channel, When $\overline{CS}$ Goes low

allows full bidirectional communication over a single serial data line. While $\overline{CS}$ is high the LTC1286 is inactive. The serial data used to select a multiplexer channel is applied to the LTC1390 DATA 1 input. Four bits are clocked into the LTC1390. The LTC1286 D_{OUT} is in a high impedance state, ignoring these bits. The LTC1390 latches the four data bits when the $\overline{CS}$ signal goes low, selecting a channel and initiating an A/D conversion from the LTC1286. Subsequent clock cycles shift out LTC1286 conversion data through the LTC1390 (from DATA 1 to DATA 2) to a host microprocessor. Figure 2 shows the LTC1390 timing diagram.

It is very easy to expand the width of the multiplexer and take advantage of the LTC1390 daisy-chain capability. Figure 3 shows the simple connections needed to add multiplexer channels. The Data 2 on each additional LTC1390 is connected to the Data 1 on the preceding LTC1390. When operating with multiple LTC1390s, the channel selecting data is sent in groups of four bits.

Another useful feature of the LTC1390 is the ability to add analog signal processing between the LTC1390 output and an A/D input. This helps save overall system cost because only one signal processing circuit is needed instead of one circuit per multiplexer input channel.

Figure 4 shows an active 2nd order lowpass filter connected between the LTC1390 output and the LTC1286 input. The heart of the lowpass filter is the single supply rail-to-rail precision LT®1366 operational amplifier. The filter's cutoff frequency is set to 1kHz.

Conclusion

The LTC1390 provides designers of a serially interfaced data acquisition system with a flexible, low power and cost-effective way to expand the number of A/D channels.

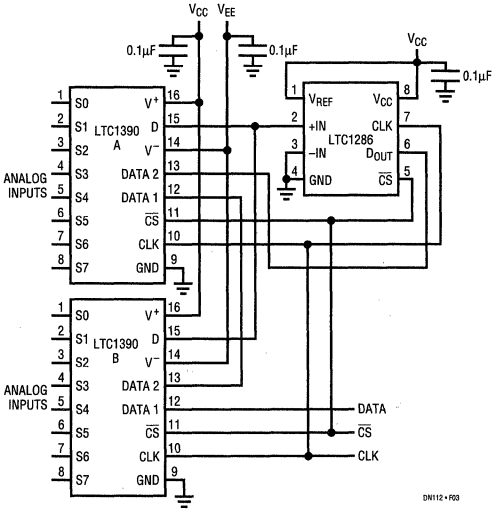


Figure 3. Additional Multiplexer Channels Are Easy to Add Without Adding Additional Serial Lines

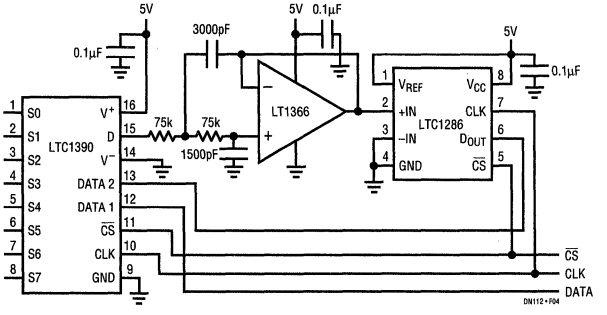


Figure 4. The Connection Between the LTC1390 Output and the LTC1286 Input Is the Perfect Place for Signal Conditioning Circuits Such as the LT1366-Based 2nd Order Active Lowpass Filter

For literature on our Multiplexers, call **1-800-4-LINEAR**. For applications help, call (408) 432-1900, Ext. 525

LINEAR TECHNOLOGY

DESIGN NOTES

Big Power for Big Processors: The LTC1430 Synchronous Regulator – Design Note 113

Dave Dwelley

Linear Technology introduces the LTC®1430 switching regulator controller for high power 5V step-down applications where efficiency, output voltage accuracy and board space requirements are critical. The LTC1430 is designed to be configured as a synchronous buck converter with a minimum of external components. It runs at a fixed switching frequency (nominally 200kHz) and provides all timing and control functions, adjustable current limit and soft start, and level shifted output drivers designed to drive an all N-channel synchronous buck converter architecture. The switch driver outputs are capable of driving multiple, paralleled power MOSFETs with submicrosecond slew rates, providing high efficiency at very high current levels and eliminating the need for a heat sink in most designs.

The LTC1430 is usable in converter designs providing from a few amps to over 50A of output current, allowing it to supply 3.xV power to current hungry arrays of microprocessors. A novel "safety belt" feedback loop provides excellent large-signal transient response with the simplicity of a voltage feedback design. The LTC1430 also includes a micropower shutdown mode that drops the quiescent current to 1µA. An all N-channel synchronous buck architecture allows the use of cost-effective, high power N-channel MOSFETs. The on-chip output drivers feature separate power supply inputs and internal level shifters allowing the MOSFET gate drive to be tailored for logic level or standard devices. External component count in the high current path is minimized by eliminating low value current sense resistors. Voltage feedback eliminates the need for current sensing under normal operating conditions and output current limit is sensed by monitoring the voltage drop across the $R_{DS(ON)}$ of M1 during its ON state.

LTC1430 Performance Features

The LTC1430 uses a voltage feedback loop to control output voltage. It includes two additional internal feedback loops to improve high frequency transient response. A MAX loop responds within a single clock cycle when the output exceeds the set point by more than 3%, forcing the duty cycle to 0% and holding M2 on continuously until the output drops back into the acceptable range. A MIN loop kicks in when the output sags 3% below the set point, forcing the LTC1430 to 90% duty cycle until the output recovers. The 90% maximum ensures that charge pump drive continues to be supplied to the top MOSFET driver, preventing the gate drive to M1 from deteriorating during extended transient loads. The MAX feedback loop is always

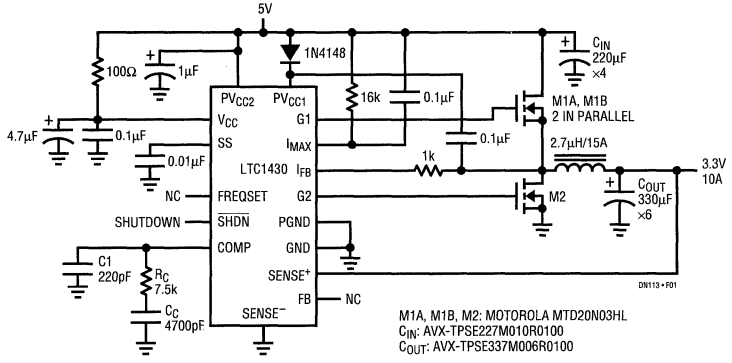


Figure 1. Typical 5V to 3.3V, 10A LTC1430 Application

active, providing a measure of protection even if the 5V input supply is accidentally shorted to the lower microprocessor supply. The MIN loop is disabled at start-up or during current limit to allow soft start to function and to prevent MIN from taking over when the current limit circuit is active.

The LTC1430 includes an onboard reference trimmed to 1.265V ±10mV and an onboard 0.1% resistor divider string that provides a fixed 3.3V output. It specifies load regulation of better than 20mV and line regulation of 5mV, resulting in a total worst-case output error of ±1.7% when used with the internal divider or 0.1% external resistors. The internal reference will drift an additional ±5mV over the 0° C to 70°C temperature range, providing a ±2.1 total error budget over this temperature range.

The LTC1430 includes an internal oscillator that free runs at any frequency between 100kHz and 500kHz. The oscillator runs at a nominal 200kHz frequency with the FREQ pin floating. An external resistor from FREQ to ground will speed up the internal oscillator, whereas a resistor to V_{CC} will slow the oscillator. The LTC1430 will shut down if the $\overline{SHDN}$ pin is low continuously for more than 50µs, reducing the supply current to 1µA.

A Typical 5V to 3.3V Application

The typical application for the LTC1430 is a 5V to 3.xV converter on a PC motherboard. The output is used to power a Pentium® processor and the input is taken from the system 5V ±5% supply. The LTC1430 provides the precisely regulated voltage required without an external precision reference or trimming. Figure 1 shows a typical application with a 3.3V ±1% output voltage and a 12A output current limit. The power MOSFETs are sized so as not to require a heat sink under ambient temperature conditions up to 50°C. Typical efficiency is shown in Figure 2.

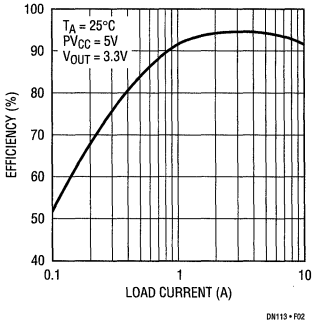


Figure 2. Figure 1 Circuit Efficiency. Note That Efficiency Peaks at a Respectable 95%

The 12A current limit is set by the 16k resistor R1 from PV_{CC} to I_{MAX} in conjunction with the 0.035Ω on resistance of the MOSFETs (M1a, M1b). The 0.1µF capacitor in parallel with R1 improves power supply rejection at I_{MAX}, providing consistent current limit performance with voltage spikes present at PV_{CC}. C_{SS} sets the soft start time; the 0.01µF value shown provides a 3ms start-up time. The 2.7µH, 15A inductor allows the peak current to rise to the full current limit value without saturating the inductor core. This allows the circuit to withstand extended output short circuits. The inductor value is a compromise between peak ripple current and output current slew rate, which affects large-signal transient response. If the output load is expected to generate large output current transients (as large microprocessors tend to do) the inductor value will need to be quite low, in the 1µH to 10µH range.

Loop compensation is critical for obtaining optimum transient response with a voltage feedback system. The compensation components shown here give good response when used with the output capacitor values and brands shown (Figure 3). The output capacitor ESR has a significant effect on the transient response of the system; for best results, use the largest value, lowest ESR capacitors that will fit the budget and space requirements. Several smaller capacitors wired in parallel can help reduce total output capacitor ESR to acceptable levels. Input bypass capacitor ESR is also important to keep input supply variations to a minimum with $10A_{P-P}$ square wave current pulses flowing into M1. AVX TPS series surface mount tantalum capacitors and Sanyo OS-CON organic electrolytic capacitors are recommended for both input and output bypass duty.

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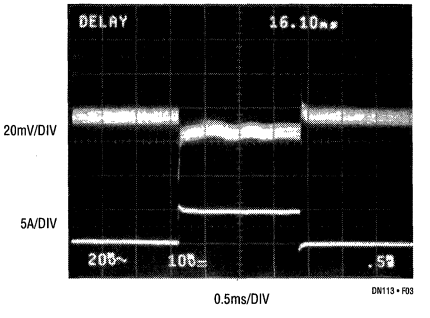

Figure 3. Transient Response: 0A to 5A Load Step Imposed on Figure 1's Output

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LINEAR TECHNOLOGY

DESIGN NOTES

The LTC1267 Dual Switching Regulator Controller Operates from High Input Voltages – Design Note 114

Randy G. Flatness and Craig Varga

Introduction

The LTC®1267 dual switching regulator controller is the latest addition to Linear Technology's family of better than 90% efficient step-down DC/DC converters. The LTC1267 features an extremely wide 4V to 40V input operating voltage range and reduced supply currents. The quiescent current is a low 320µA and current in Shutdown mode drops to less than 20µA. The combination of low supply currents and high input voltage capability is ideal for battery-powered applications that require high voltage AC wall adapters.

Linear Technology offers three versions of the LTC1267, all in the space-saving 28-lead SSOP package. The LTC1267 provides fixed output voltages of 3.3V and 5V with individual shutdown capability. The LTC1267-ADJ provides two user-programmable output voltages set by external resistive dividers. The LTC1267-ADJ5 is configured with a fixed 5V output and a programmable output set by an external resistor divider.

High Efficiency with Dual Output Voltages

To boost efficiency, a unique EXT V_{CC} pin on the LTC1267 (also present on the single output LTC1159) allows the MOSFET drivers and control circuitry to be powered from an external source, such as the output of the regulator itself. Obtaining control and driver power from V_{OUT} improves efficiency at high input voltages, since the resulting current drawn from V_{IN} is scaled by the duty cycle of the regulator. During start-up and short-circuit conditions, operating power is supplied by an internal 4.5V low dropout regulator. This regulator automatically turns off when the EXT V_{CC} pin rises above 4.5V.

This 28-pin controller uses Linear Technology's high performance, current mode architecture and Burst Mode™ operation. The LTC1267 automatically switches to Burst Mode operation at low output currents to maintain high efficiency over two decades of load current range. The wide operating range is illustrated by the typical efficiency curve of Figure 1. Battery life is extended by providing high efficiencies at load currents from a few milliamps (when the device is in standby or sleep modes) to amps (under full power conditions).

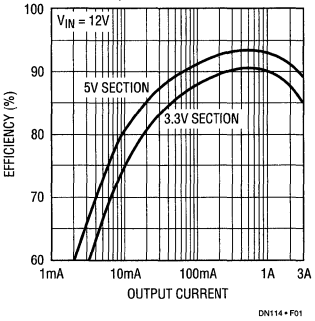

Figure 1. LTC1267 Efficiency vs Output Current of the Figure 2 Circuit

Description

Both regulator blocks in the LTC1267 use a constant off time, current mode architecture. This results in a power supply that has very high efficiency over a wide load current range, fast transient response and very low dropout. The LTC1267 is ideal for applications that require 3.3V and 5V to be implemented with the highest conversion efficiencies over a wide load current range in a small board space. The LTC1267-ADJ has two externally adjustable outputs which allow remote load sensing and user customized output voltages.

Each regulator section employs a pair of external, complementary MOSFETs and a user programmable current sense resistor to set the operation current level to optimize performance for each application. A master Shutdown pin turns off both main outputs and the 4.5V LDO. Both outputs in the LTC1267 and LTC1267-ADJ5 have individual Shutdown capability, whereas the LTC1267-ADJ has a Shutdown pin for only one of its two outputs.

The higher input voltage capability of the LTC1267 is required by battery-powered systems that use many cells in series to provide more power and longer battery life. For applications requiring 12 cells or more, the AC adapter voltage can be as high as 30V, well below the 40V maximum of the LTC1267, allowing operation directly from the AC adapter. At low input voltages, the internal 4.5V low dropout regulator stays in regulation with an input of only 5V, extracting the maximum possible energy from the battery pack.

All members of the LTC1142/LTC1267 family are capable of 100% duty cycle, providing very low dropout operation (lower than that of most linear low dropout regulators) and all have built-in current limiting. As the input voltage on the LTC1267 drops, the loop extends the on time for the P-channel switch (off time is constant) thereby keeping the inductor ripple current constant. Eventually the on time extends so far that the P-channel MOSFET is on at DC or 100% duty cycle. Load and line regulation are excellent for a wide variety of conditions, including making the transition from Burst Mode operation to continuous mode operation.

Fixed Output 3.3V and 5V Converter

A fixed LTC1267 application circuit creating 3.3V/3A and 5V/3A is shown in Figure 2. The operating efficiency shown in Figure 1 exceeds 90% for both the 3.3V and 5V sections. The 3.3V section of the circuit in Figure 2 comprises the main switch Q1, synchronous switch Q2, inductor L1 and current shunt R_{SENSE3}.

The 5V section is similar and comprises Q3, Q4, L2 and R_{SENSE5}. Each current sense resistor (R_{SENSE}) monitors the inductor current and is used to set the output current according to the formula $I_{OUT} = 100mV/R_{SENSE}$. Advantages of current control include excellent line and load transient rejection, inherent short-circuit protection and controlled start-up currents. Peak inductor currents for L1 and L2 are limited to $150mV/R_{SENSE}$ or 4.5A. The EXT V_{CC} pin is connected to the 5V output, increasing efficiency at high input voltages. The maximum input voltage is limited by the external MOSFETs and should not exceed 28V.

Conclusion

The LTC1267 adds even more versatility to Linear Technology's family of high efficiency step-down regulator controllers. Providing for up to 40V input voltage, the LTC1267 allows the use of higher voltage wall adapters. The 28-lead SSOP package and associated external components make dual output voltage, high efficiency DC/DC conversion feasible in the extremely small board space available in today's portable electronics.

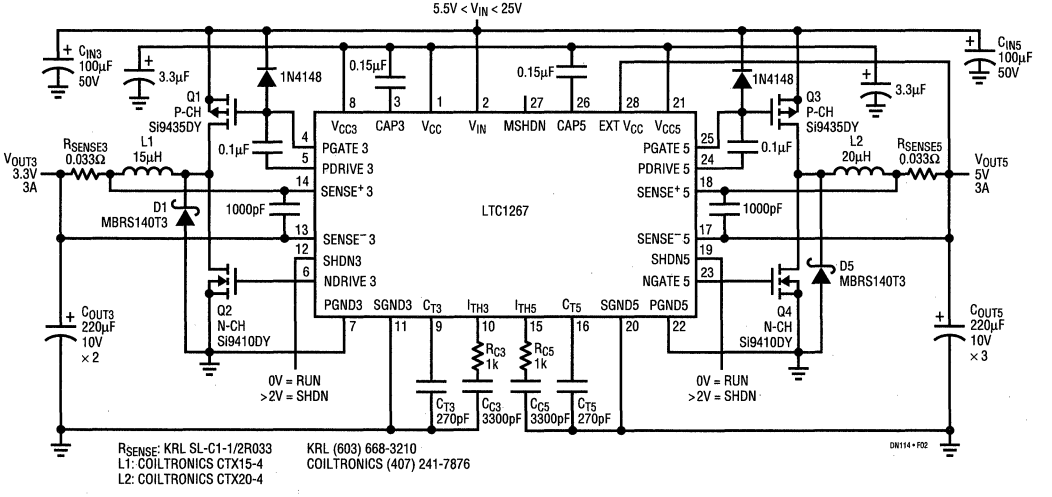

Figure 2. LTC1267 Dual Output 3.3V and 5V High Efficiency Regulator

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LINEAR TECHNOLOGY

DESIGN NOTES

Create a Virtual Ground with the LT1118-2.5 Sink/Source Voltage Regulator – Design Note 115

Gary Maulding

Analog signal processing functions embedded in dominantly digital systems usually require the addition of a negative power supply. Although many single supply analog components are available, optimum performance characteristics are often available only in devices that require both positive and negative power supplies. Even the use of single supply components does not solve all of the problems of single 5V operation of analog functions. Signal swings are restricted to a positive direction and may approach but not reach ground potential. The LT®1118-2.5 source/sink voltage regulator, used as a supply splitter, provides the designer with an alternative to adding a negative supply. Referencing the signal levels to the regulator's 2.5V output allows symmetrical signal swings and also allows the selection of op amps, active filters and other components that do not have common mode range to ground.

Resistive dividers are frequently used as supply splitters to establish a virtual ground. This approach is often effective, but the circuit designer must work around the resistive divider's severe performance limitations. A fundamental limitation of a resistive divider is the high power dissipation required to obtain any suitable output impedance. A divider made from 240Ω resistors, as in Figure 1a, pulls over 10mA of quiescent current and has a DC output impedance of 120Ω. In contrast, the LT1118-2.5 splitter shown in Figure 1b achieves an output impedance of less than 0.025Ω with a quiescent current of 600μA. The resistive divider's high output impedance restricts its use to high impedance, low frequency signal sources; otherwise, the

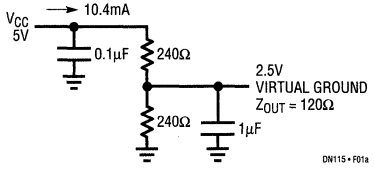

Figure 1a. Resistive Divider Supply Splitter

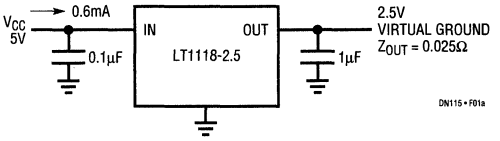

Figure 1b. LT1118-2.5 Supply Splitter

output impedance of the splitter will cause gain errors and AC response degradation in all op amp configurations except unity-gain buffers. Use of large feedback network resistors will limit frequency response and noise performance.

Figure 2 shows the LT1118-2.5 output impedance vs frequency for several output current loads. Examination of this plot reveals several operating characteristics of the regulator. At low frequencies, the output impedance is below 0.025Ω at all operating points. No passive divider can approach this low impedance. The quiescent current condition has the maximum impedance, with both sink or source current loads causing further output impedance reduction. This level of impedance variation is so low however, that no measurable distortion is introduced in the

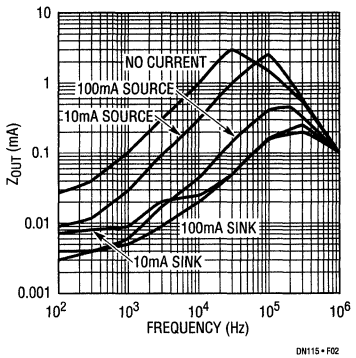

Figure 2. LT1118-2.5 Output Impedance vs Frequency

signal. The low output impedance also allows low feedback resistance video amplifiers to operate from the virtual ground without gain errors or distortion. As frequencies increase, the output impedance of the regulator increases, until the output capacitor's impedance dominates and rolls the impedance off to lower values again. With the 1µF capacitor used in this example, maximum output impedance is 3Ω at 30kHz. Larger output capacitors will reduce this maximum impedance by intersecting the regulator's output impedance curve at lower frequencies. Only in the most demanding applications should a larger capacitor be required.

The LT1118 family of regulators are all capable of sourcing 800mA and sinking 400mA of load current. This high level of current will handle almost any signal levels encountered in supply splitter applications. Figure 3 shows the fast (less than 5µs) load transient settling characteristics of the LT1118-2.5. This response was obtained using a 1µF output capacitor with 800mA to –400mA load steps. The regulator is stable with any output capacitance greater than 0.2µF, with larger capacitance reducing the output voltage transient amplitude. Competing supply splitter circuits do not exhibit well-behaved transient behavior. This is illustrated in Figure 4, which shows a competitor's load transient response from –25mA to 25mA, the circuit's full output capability. With 1µF of output capacitance the regulator is almost unstable.

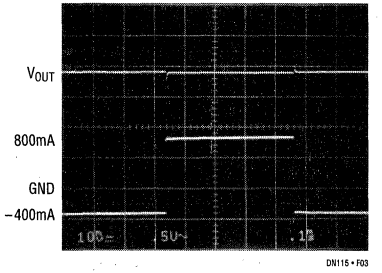

Figure 3. LT1118-2.5 Load Transient Response

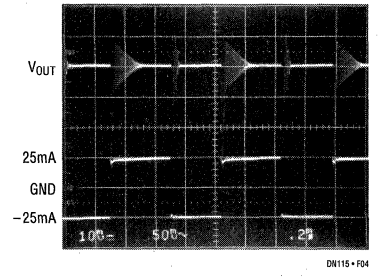

Figure 4. Competitor's Supply Splitter Load Transient

The LT1118-2.5, like the LT1118-2.85/LT1118-5, is offered in both SOT-223 and SO-8 packages. The SO-8 version includes a Shutdown pin, which turns the output high impedance and drops supply current to zero. The SO-8 versions can be used to minimize power consumption when the analog functions are not in use. All members of the LT1118 family share the performance features of fast settling and excellent transient response for loads between 400mA sinking to 800mA sourcing.

The LT1118-5 is a useful regulator for applications requiring very fast settling to full load transients. The current sinking output limits output voltage overshoot compared to conventional regulators.

The LT1118-2.85 is an ideal choice for SCSI terminator applications. The increasing use of active negation drivers to improve noise immunity in fast SCSI systems causes conventional voltage regulators to lose regulation. The current sinking output mode of the LT1118-2.85 maintains a solid 2.85V output with the maximum 24 of 27 data lines negated. The use of one LT1118-2.85 and twenty-seven 110Ω surface mount resistors provides a more economical, higher performance solution for terminating fast wide SCSI data busses than SCSI terminators with on-chip resistors. Terminators with on-chip resistors have serious deficiencies in power dissipation and output capacitance compared to an LT1118-2.85 solution. Up to 3.5W of power is dissipated terminating a 27-line SCSI bus. Terminators with on-chip resistors cannot dissipate this much power from a surface mount IC package, so multiple chips must be used to terminate the entire bus. One LT1118-2.85 with external resistors can do the whole job, since 2W is dissipated in the resistors and only 1.5W in the IC. The LT1118-2.85 plus external resistors also provides better noise immunity than terminators with on-chip resistors. The pin capacitance of the IC can be as high as 2pF. Capacitance on the SCSI data lines causes reflections and loss of noise immunity at high data rates. With the LT1118-2.85 plus external resistor solution, the data line capacitance is minimized to the PC board stray capacitance.

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LINEAR TECHNOLOGY

DESIGN NOTES

Micropower 12-Bit ADCs Shrink Board Space – Design Note 116

Kevin R. Hoskins

Introduction

The LTC®1286/LTC1298 are serial interfaced, micropower 12-bit analog-to-digital converters. In the realm of 12-bit ADCs they bring a new low in power dissipation and the small size of an SO-8 package to low cost, battery-powered electronic products. These micropower devices consume just 250µA (LTC1286) and 340µA (LTC1298) at full conversion speed and feature autoshutdown.

Many portable and battery-powered systems require internal analog-to-digital conversion. Some, such as pen-based computers, have ADCs at their very cores digitizing the pen screen. Other systems use ADCs more peripherally to monitor voltages or other parameters inside the equipment. Regardless of the use, it has been difficult to obtain small ADCs at power levels and prices that are low enough. The LTC1286/LTC1298 meet these low power dissipation and package size needs.

Micropower and 12-Bits in an SO-8 Package

The LTC1286/LTC1298 are the latest members of the growing family of SO-8 packaged parts (Table 1). As the first of their kind in SO-8 packages, these are improvements to the 8-bit micropower LTC1096/LTC1098 ADCs. The LTC1286/LTC1298 use a successive approximation register (SAR) architecture. Both converters contain sample-and-holds and serial data I/O. The LTC1286 has a fully differential analog input and the LTC1298 has a two input multiplexer. While running at a full speed conversion rate of 12.5ksps, the LTC1286 consumes only 250µA from a single 5V supply voltage. The device automatically shuts down to 1nA (typ) when not converting. Figure 1 shows how this automatically reduces power at lower sample rates. At a 1ksps conversion rate, the supply current drops to just 20µA (typ). Battery-powered designs will benefit tremendously from this user transparent automatic power dissipation optimization.

Table 1. LTC Micropower 3V and 5V 12-Bit ADCs

DEVICE	POWER DISSIPATION AT 200ksps	SAMP FREQ	S/(N+D) AT NYQUIST	INPUT RANGE	POWER SUPPLY
LTC1285	12µW 3nW*	7.5ksps	72dB	0V to V_{CC}	2.7V to 6V
LTC1286	25µW 5nW*	12.5ksps	71dB	0V to V_{CC}	4.5V to 9V
LTC1288	12µW 3nW*	6.6ksps	72dB	0V to V_{CC}	2.7V to 6V
LTC1298	12µW 5nW*	11.1ksps	71dB	0V to V_{CC}	4.5V to 5.5V

*5nW and 3nW power dissipation during shutdown

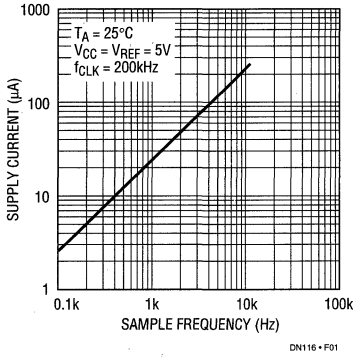

Figure 1. The LTC1286/LTC1298's Autoshutdown Feature Automatically Conserves Power When Operating at Reduced Sample Rates

The DC specifications include an excellent differential linearity error of 0.75LSB (max) and no missing codes. Both are guaranteed over the operating temperature range. Pen screen and other monitoring applications benefit greatly from these tight specifications.

The attractiveness of the LTC1286/LTC1298's small SO-8 design is further enhanced by the use of just one surface mount bypass capacitor (1µF or less). Figure 2 shows a typical connection to a microcontroller's serial port. For ratiometric applications that require no external reference voltage, the LTC1286/LTC1298's reference input is tied to signal source's drive voltage. With their very low supply

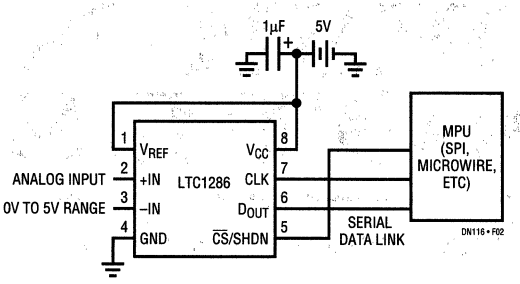

Figure 2. The No-Glue Serial Interface Simplifies Connection to SPI, QSPI or Microwire Compatible Microcontrollers

current requirements, the ADCs can even be powered directly from an external voltage reference. This eliminates the need for a separate voltage regulator.

The LTC1286/LTC1298 contain everything required except an internal reference (not needed by many applications) keeping systems costs low. The serial interface makes a very space efficient interface and significantly reduces cost of applications requiring isolation. The ADC's high input impedance eliminates the need for buffer amplifiers. All of these features, combined with a very attractive price, make the LTC1286/LTC1298 ideal for new designs.

Resistive Touchscreen Interface

Figure 3 shows the LTC1298 in a 4-wire resistive touchscreen application. Transistor pairs Q1 and Q3, Q2 and Q4 apply 5V and ground to the X axis and Y axis, respectively. The LTC1298 (U1), with its 2-channel multiplexer, digitizes the voltage generated by each axis and transmits the conversion results to the system's processor through a serial interface. RC combinations R1C1, R2C2 and R3C3 form lowpass filters that attenuate noise from possible sources such as the processor clock, switching power supplies and bus signals. Inverter U2A is used to detect screen contact both during a conversion sequence and to trigger its start. Using the single channel LTC1286, 5-wire resistive touchscreens are as easily accommodated.

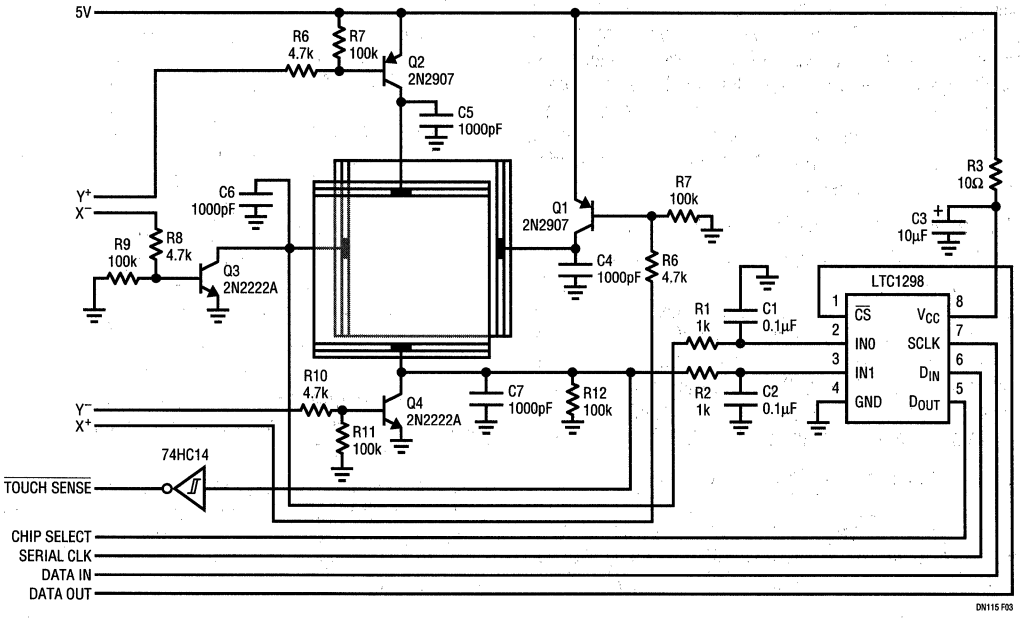

Figure 3. The LTC1298 Digitizes Resistive Touchscreen X and Y Axis Voltages. The ADC's Autoshutdown Feature Helps Maximize Battery Life in Portable Touchscreen Equipment

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LINEAR TECHNOLOGY

DESIGN NOTES

70mΩ Protected Load Management Switch – Design Note 117

Mitchell Lee and Tim Skovmand

In an effort to conserve energy, simple shutdown schemes are incorporated into many battery-operated circuits. Not all circuits lend themselves to direct control, however, and instead the supply must be turned off by a switch. The LTC®1477 high side switch is designed for this purpose and includes short-circuit current limit and thermal shutdown to guard against faulty loads. Figure 1 shows a simplified block diagram of the LTC1477.

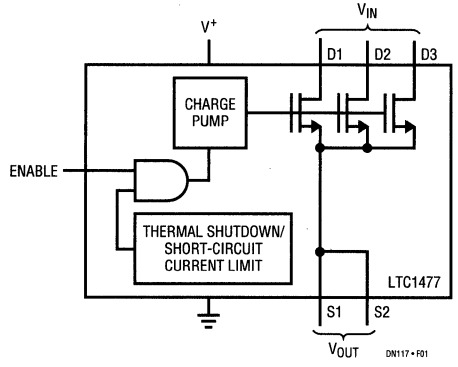

Figure 1. LTC1477 Block Diagram

At the heart of the LTC1477 is a 70mΩ N-channel MOSFET. The split drains allow for selection of 0.85A, 1.5A or 2A current limit. While enabled, the LTC1477 draws about 100µA quiescent current, dropping to 10nA in its disabled state.

Figure 2 shows the LTC1477 and LTC699 conjoined in an undervoltage disconnect application. The LTC699 microprocessor supervisor disables the LTC1477 and hence the load whenever the input voltage falls below 4.65V. An external logic signal applied to the gate of Q1 can also disable the LTC1477. When enabled, the LTC1477 output ramps over a period of approximately 1ms, thereby limiting the peak current in the load capacitor to 500mA. This prevents glitches on the 5V source line that might otherwise affect adjacent loads.

An LT®1301 is used in Figure 3 to boost a 3.3V or 5V input to 12V, such as VPP for Flash memory. Although the LT1301 features a shutdown control, the input supply can still feed through to the output through L1 and D1. Similarly, a short circuit on the output could drag down the input supply. With the addition of the LTC1477 the circuit furnishes 100% load shutdown and output short-circuit protection.

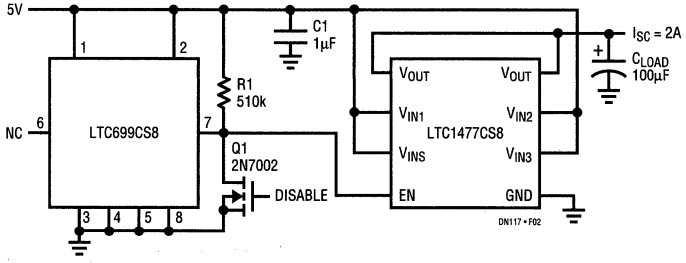

Figure 2. Switched 5V Line with Undervoltage Lockout and Current Limiting

Low voltage cutoff is desirable in battery-operated systems to prevent deep discharge damage to the battery. The LT1304 micropower boost regulator (Figure 4) contains a low-battery detector which is active even when the regulator is shut down. The output of the detector controls both the LTC1477 and the LT1304 5V boost regulator. In this application the LTC1477 serves to protect against short circuits (850mA limit selected) and completely disconnects the load under a low-battery condition. In shutdown, the circuit draws less than 25µA from the battery.

A dual version, the LTC1478 is available in a 16-pin narrow body SO package. This device is well suited for dual voltage (5V/3.3V) switching applications.

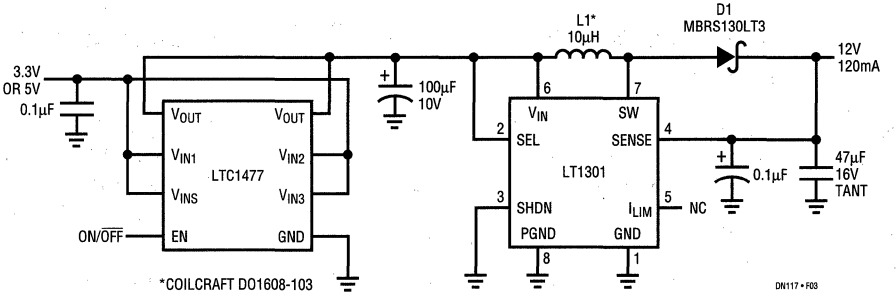

Figure 3. Short-Circuit Protection and 100% Shutdown for a Micropower Boost Regulator

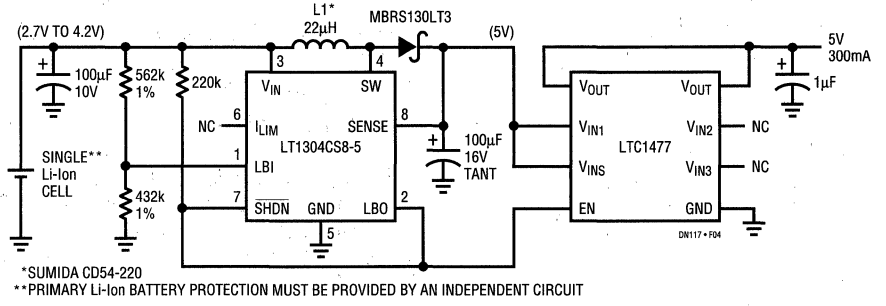

Figure 4. Situated Downstream, the LTC1477 Is Controlled by the LT1304's Low-Battery Detector

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LINEAR TECHNOLOGY

DESIGN NOTES

IR LocalTalk Link Has Superior Range and Ambient Rejection

Design Note 118

Frank Cox

Infrared links are becoming increasingly popular for wireless point-to-point communication between portable computers, PDAs (Personal Digital Assistants), desktop computers and peripherals. A key element in processing these signals for minimum error rate and maximum range is the photodiode receiver. The function of the receiver is to transform modulated photodiode current to a voltage and to process this voltage before converting it back to a digital signal. Processing includes amplification, filtering, clamping and thresholding. The LT®1319 is a flexible, general purpose building block that contains all the active circuitry necessary to build the receiver except the photodiode itself[1].

LocalTalk® is a 230kBd, biphased encoded, serial communications standard developed by Apple Computer, Inc. for hardwired peripheral connection. Infrared LocalTalk uses modified pulse position modulation (PPM) to encode two bits of information in a time frame 8.7µs long. PPM is a method of modulating data by encoding its value as the position of a pulse within a time interval. Extending the maximum range of a data link and at the same time minimizing errors, IR LocalTalk improves on simple PPM. The improvement is made by sending a burst of narrow pulses instead of a single pulse. Each burst consists of a group of four 125ns pulses spaced 125ns apart. Sending a burst instead of a single pulse also reduces the LED duty cycle allowing higher peak current and consequently more range. Because the burst has a more complicated structure than a simple pulse, digital pattern recognition (done in the digital decoder) can be used to improve the minimum discernible signal level and reject false signals, thereby increasing the maximum error-free range of the link.

Compared to industry standard IrDA-SIR (Infrared Data Association Serial Infrared), IR LocalTalk serial links provide superior range, data rate and rejection of ambient light interference. The spectrum used by IR serial links is full of interference from sunlight, TV remotes and fluorescent lights. The new high efficiency fluorescent lights are a significant source of light interference at frequencies from 40kHz to 80kHz because of their switched mode active ballast circuits. Results of tests comparing IrDA-SIR and IR LocalTalk are summarized in Table 1.

Table 1

MODULATION	RANGE	DATA RATE	AMBIENT REJECTION
IR LocalTalk	2m	230kbps	Reject a 15W 80kHz Fluorescent at 25cm
IrDA-SIR	1m	115kbps	Reject a 15W 80kHz Fluorescent at 1.1m

As shown in Figure 1, the time frame is divided into four 2.18µs sections. As the baud rate for IR LocalTalk is fixed at 230kBd, one bit of information is transmitted every 4.35µs and two bits are transmitted in the complete 8.7µs frame. Each frame begins with a burst that is used for synchronizing. The position (or absence) of the subsequent burst within the frame encodes the two bits to be transmitted. One important thing to note about this waveform is that the duty cycle is relatively constant. This is important because the receiver is AC coupled. A very wide range of duty cycles will make it difficult to choose a good compromise for the highpass break frequency. A mismatch between the AC-coupling time constants and the

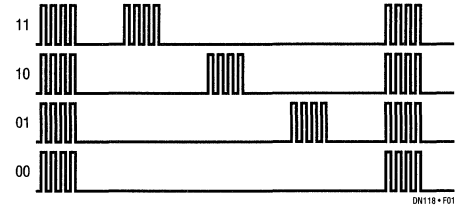

Figure 1. Pulse Position Coding for IR LocalTalk

[1]The LT1319 is designed to have great flexibility to accommodate communication standards that are just emerging or not yet defined. The ability to change the external photodiode helps accomplish this task by allowing the user to choose the ideal photodiode for the application. The LED transmitter is also external to the LT1319 for the same reason.

duty cycle of the receive pulse can cause baseline shifts and false triggering when the signals are converted to digital levels.

Figure 2 is a block diagram of the LT1319 and the necessary components to construct an IR LocalTalk link. The LT1319 is intended to function in a wide range of applications, but this note will focus only on IR LocalTalk because of limited space. A low noise (2pA/$\sqrt{Hz}$), high bandwidth (7MHz) current-to-voltage converter formed by the preamplifier and its associated components transforms the reverse current from an external photodiode to a voltage. Although the 7MHz bandwidth of the preamp supports 4Mbit data rates, a lowpass filter on the preamp output is used to reduce the bandwidth to just the required amount in order to reduce noise. Proper filtering and the low noise of the preamp allow for links of two meters or more.

As shown in Figure 2, capacitor C_{F1} sets the break frequency of an AC highpass loop around the preamp to 180kHz. This loop rejects unwanted ambient light pollution, including sunlight, incandescent and fluorescent lights.

The preamp stage is followed by two separate channels each containing a high impedance filter buffer, two gain stages, highpass loops and a comparator. The only difference between the two channels is the response time of the comparators: 25ns and 60ns. For the 125ns pulses of IR LocalTalk, the 25ns comparator with its active pull-up output is used. The low frequency comparator with its open collector output (with 5kΩ internal pull-up) is suitable for more modest speeds such as the 1.6µs pulses or IrDA-SIR. Each gain path has an AC coupling loop similar to the one on the preamp. Capacitor CF5 sets the highpass corner at 140kHz for IR LocalTalk. The loops serve the additional purpose here of maintaining an accurate threshold for the comparators by forcing the DC level of the differential gain stages to zero.

As the preamp output is brought out and the inputs to the two comparator channels are buffered, the user is free to construct the exact filter required for the application by the careful selection of external components. R_{F1}, C_{F2}, C_{F3}, R_{F2}, C_{F4} and R_{F3} form a bandpass filter with a center frequency of 3.5MHz and 3dB points of 1MHz and 12MHz. Together with the highpass AC loop in the preamp and the 7MHz response of the preamp, this forms an optimal filter response for IR LocalTalk.

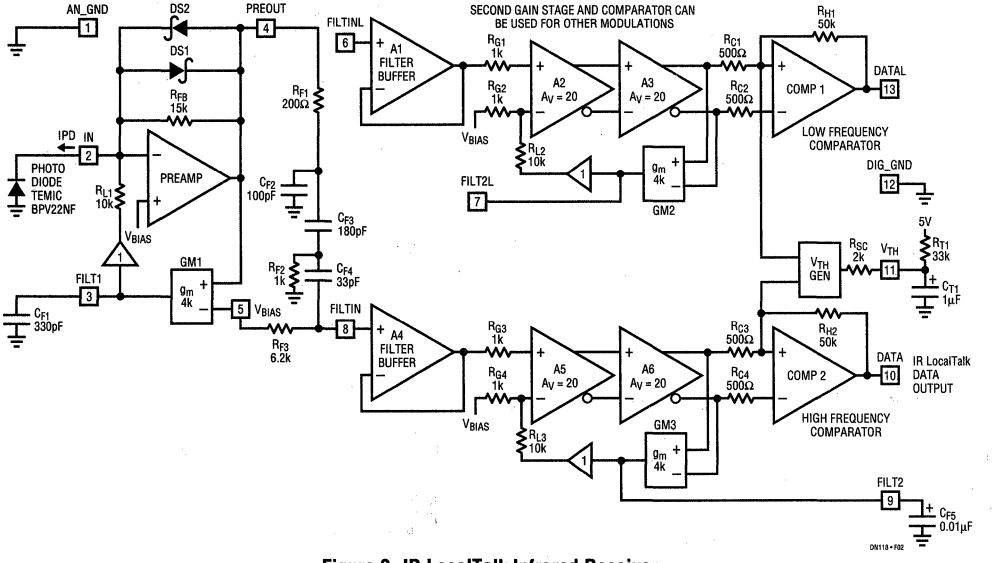

Figure 2. IR LocalTalk Infrared Receiver

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LINEAR TECHNOLOGY

DESIGN NOTES

LT1580 Fast Response Low Dropout Regulator Achieves 0.4 Dropout at 4 Amps – Design Note 119

Craig Varga

Low dropout regulators have become more common in desktop computer systems as microprocessor manufacturers have moved away from 5V only CPUs. A wide range of supply requirements exists today with new voltages just over the horizon. In many cases, the input-output differential is very small, effectively disqualifying many of the low-dropout regulators on the market today. Several manufacturers have chosen to achieve lower dropout by using PNP-based regulators. The drawbacks of this approach include much larger die size, inferior line rejection and poor transient response.

ENTER THE LT®1580

The new LT1580 NPN regulator is designed to make use of the higher supply voltages already present in most systems. The higher voltage source is used to provide power for the control circuitry and supply the drive current to the NPN output transistor. This allows the NPN to be driven into saturation, thereby reducing the dropout voltage by a V_{BE} compared to a conventional design. Applications for the LT1580 include 3.3V to 2.5V conversion with a 5V control supply, 5V to 4.2V conversion with a 12V control supply, or 5V to 3.6V conversion with a 12V control supply. It is easy to obtain dropout voltages as low as 0.4V at 4A, along with excellent static and dynamic specifications.

The LT1580 is capable of 7A maximum with approximately 0.8V input-to-output differential. The current requirement for the control voltage source is approximately 1/100 of the output load current or about 70mA for a 7A load. The LT1580 presents no supply-sequencing issues. If the control voltage comes up first, the regulator will not try to supply the full-load demand from this source. The control voltage must be at least 1V greater than the output to obtain optimum performance. For adjustable regulators, the adjust-pin current is approximately 60µA and varies directly with absolute temperature. In fixed regulators, the ground pin current is about 10mA and stays essentially constant as a function of load. Transient response performance is similar to that of the LT1584 fast-transient-response regulator. Maximum input voltage from the main power source is 7V and the absolute maximum control voltage is 13V. The part is fully protected from overcurrent and overtemperature conditions. Both fixed voltage and adjustable voltage versions are available. The adjustables are packaged in 5-pin TO-220s, whereas the fixed-voltage parts are 7-pin TO-220s.

The LT1580 Brings Many New Features

Why so many pins? The LT1580 includes several innovative features that require additional pins. Both the fixed and adjustable versions have remote-sense pins, permitting very accurate regulation of output voltage at the load, where it counts, rather than at the regulator. As a result, the typical load regulation over a range of 100mA to 7A with a 2.5V output is approximately ±1mV. The Sense pin and the V_{CONT} pin, plus the conventional three pins of an LDO regulator, give a pin count of five for the adjustable design. The fixed voltage part adds a GND pin for the bottom of the internal feedback divider, bringing the pin count to six. Pin 7 is a no connect.

Note that the Adjust pin is brought out even on the fixed voltage parts. This allows the user to greatly improve the dynamic response of the regulator by bypassing the feedback divider with a capacitor. In the past, using a fixed regulator meant suffering a loss of performance due to the lack of such a bypass. A capacitor value of 0.1µF to approximately 1µF will generally provide optimum transient response. The value chosen depends on the amount of output capacitance in the system.

In addition to the enhancements already mentioned, the reference accuracy has been improved by a factor of two, with a guaranteed 0.5% tolerance. Temperature drift is also very well controlled. When combined with ratiometrically accurate internal divider resistors, the part can easily hold 1% output accuracy over temperature, guaranteed, while operating with an input/output differential of well under 1V.

In some cases, a higher supply voltage for the control voltage will not be available. If the Control pin is tied to the main supply, the regulator will still function as a conventional LDO and offer a dropout specification approximately 70mV better than conventional NPN-based LDOs. This is the result of eliminating the voltage drop of the on-die connection to the control circuit that exists in older designs. This connection is now made externally, on the PC board, using much larger conductors than are possible on the die.

Circuit Example

Figure 1 shows a circuit designed to deliver 2.5V from a 3.3V source with 5V available for the control voltage. Figure 2 shows the response to a load step of 200mA to 4.0A. The circuit is configured with a 0.33µF adjust-pin bypass capacitor. The performance without this capacitor is shown in Figure 3. This difference in performance is the reason for providing the Adjust pin on the fixed-voltage devices. A substantial savings in expensive output decoupling capacitance may be realized by adding a small ceramic capacitor at this pin.

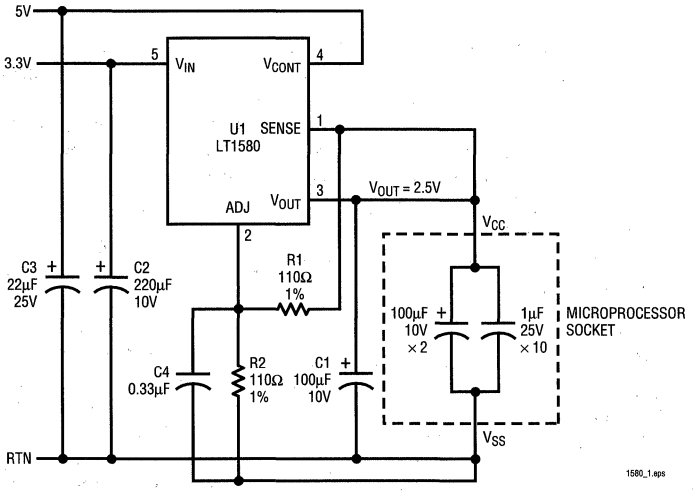

Figure 1. LT1580 Delivers 2.5V from 3.3V at Up to 6A

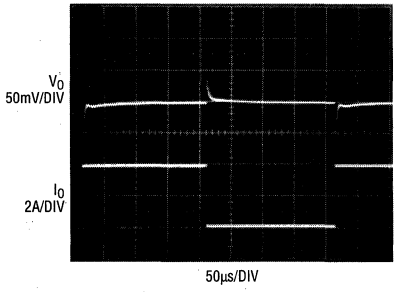

Figure 2. Transient Response of Figure 1's Circuit with Adjust-Pin Bypass Capacitor. Load Step Is from 200mA to 4 Amps

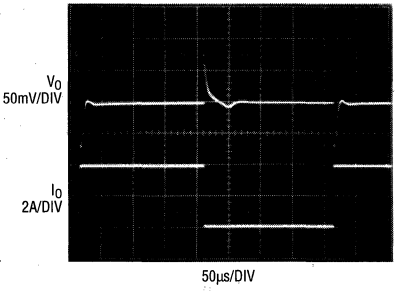

Figure 3. Transient Response Without Adjust-Pin Bypass Capacitor. Otherwise, Conditions Are the Same as in Figure 2

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LINEAR TECHNOLOGY

DESIGN NOTES

The LT1304: Micropower DC/DC Converter with Independent Low-Battery Detector – Design Note 120

Steve Pietkiewicz

In the expanding world of low power portable electronics, a 2- or 3-cell battery remains a popular power source. Designers have many options for converting the 2V to 4V battery voltage to 5V, 3.3V and other required system voltages using low voltage DC/DC converter ICs. The LT®1304 offers users a micropower step-up DC/DC converter featuring Burst Mode™ operation and a low-battery detector that stays alive when the converter is shut down. The device consumes only 125µA when active, yet can deliver 5V at up to 200mA from a 2V input. High frequency operation up to 300kHz allows the use of tiny surface mount inductors and capacitors. When the device is shut down the low-battery detector draws only 10µA. An efficient internal power NPN switch handles 1A with a drop of 500mV. Up to 85% efficiency is obtainable in 2-cell to 5V converter applications. The fixed output LT1304-5 and LT1304-3.3 versions have internal resistor dividers that set the output voltage to 5V or 3.3V, respectively.

A 2-Cell to 5V Converter

A compact 2-cell to 5V converter can be constructed using the circuit of Figure 1. The LT1304-5 fixed output device eliminates the need for external voltage setting resistors, lowering component count. As the battery voltage drops, the circuit continues to function until the LT1304's undervoltage lockout disables the part at approximately V_{IN} = 1.5V. Up to 200mA output current is available at a battery voltage of 2V. As the battery voltage decreases below 2V, cell impedance starts to quickly increase. End-of-life is usually assumed to be around 1.8V, or 0.9V per cell. Burst Mode micropower operation keeps efficiency above 70% even for load current below 1mA. Efficiency, detailed in Figure 2, reaches 85% for a 3.3V input. Load transient response is illustrated in Figure 3. Since the LT1304 uses a hysteretic comparator in place of the traditional linear feedback loop, the circuit responds immediately to changes in load current. Figure 4 details start-up behavior. After the device is enabled, output voltage reaches 5V in approximately 2ms while delivering 200mA.

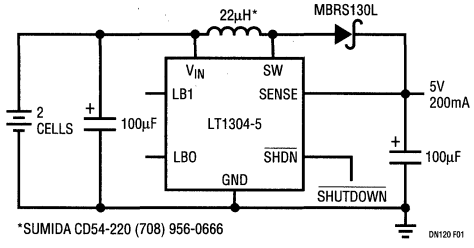

Figure 1. 2-Cell to 5V/200mA Boost Converter Requires Only Four External Parts

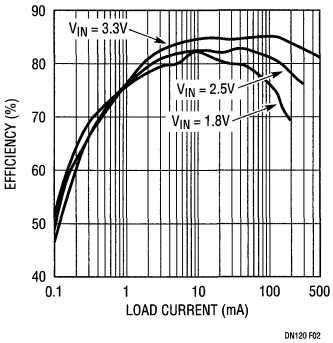

Figure 2. 2-Cell to 5V Converter Efficiency

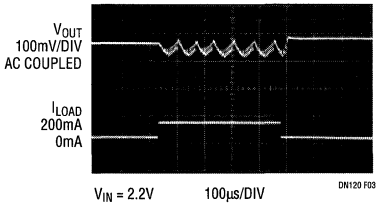

Figure 3. Boost Converter Load Transient Response

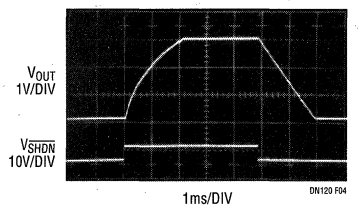

Figure 4. Start-Up Response into 200mA Load. V_{OUT} Reaches 5V in Just Over 2ms

Super Burst™ Mode Operation: 5V/80mA DC/DC with 15µA Quiescent Current

The LT1304's low-battery detector can be used to control the DC/DC converter. The result is a reduction in quiescent current by almost an order of magnitude. Figure 5 details this Super Burst mode operation circuit. V_{OUT} is monitored by the LT1304's LBI pin via resistor divider R1/R2. When LBI is above 1.2V, LBO is high, forcing the LT1304 into shutdown mode and reducing current drain from the battery to 15µA. When V_{OUT} decreases enough to overcome the low-battery detector's hysteresis (about 35mV) LBO goes low. Q1 turns on, pulling SHDN high and turning on the rest of the IC. R3 limits peak current to 500mA; it can be removed for higher output power. Efficiency is shown in Figure 6. The converter is approximately 70% efficient at a 100µA load, 20 points higher than the circuit of Figure 1. Even at a 10µA load, efficiency is in the 40% to 50% range, equivalent to 100µW to 120µW total power drain from the battery. In contrast, Figure 1's circuit consumes approximately 300µW to 400µW unloaded.

An output capacitor charging cycle or "burst" is shown in Figure 7 with the circuit driving a 50mA load. The slow response of the low-battery detector results in the high number of individual switch cycles or "hits" within the burst.

Figure 8 depicts output voltage at the modest load of 100µA. The burst repetition rate is around 4Hz. With the load removed, the repetition rate drops to approximately 0.2Hz, or one burst every 5 seconds. Systems that spend a high percentage of operating time in sleep mode can benefit from the greatly reduced quiescent power drain of Figure 5's circuit.

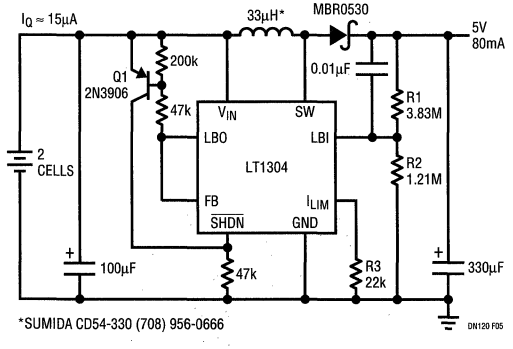

Figure 5. Super Burst Mode Operation 2-Cell to 5V DC/DC Converter Draws Only 15µA Unloaded. Two AA Alkaline Cells Will Last for Years

Super Burst is a trademark of Linear Technology Corporation.

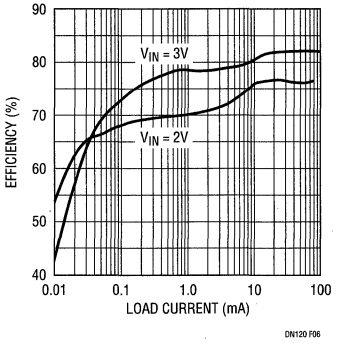

Figure 6. Super Burst Mode Operation DC/DC Converter Efficiency

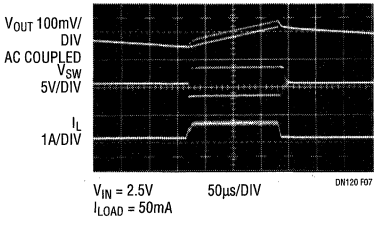

Figure 7. Super Burst Mode Operation in Action

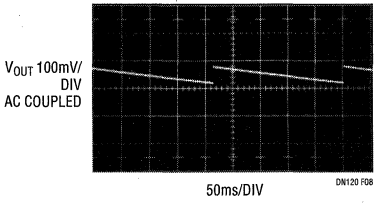

Figure 8. Figure 5's Circuit, 100µA Load. Burst Occurs Approximately Once Every 240ms

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DESIGN NOTES

New Micropower, Low Dropout Regulators Ease Battery Supply Designs – Design Note 121

Mitchell Lee and John Seago

Three new linear regulators simplify the design of battery-operated equipment. The LT®1521 is a 300mA, positive low dropout regulator with micropower quiescent current and shutdown. The LT1175 is a 500mA negative complement with adjustable current limit. A third product, the LT1118, has the unique capability of maintaining output regulation while sourcing or sinking load current.

The LT1521 contains all of the features associated with battery-operated applications. In designs where memory must be powered continuously, the LT1521's 12μA quiescent current eliminates the need for a separate micropower backup supply. In shutdown the quiescent current drops to 6μA. Figure 1 shows an example application using the LTC®1477 as a means of disconnecting all circuitry except for memory and ON/OFF control logic. The LTC1477 protected high side switch draws only 10nA in shutdown, eliminating itself as well as its load as a factor in battery shelf life.

In battery-backed memory applications, the output of the LT1521 can be held up by the backup battery while in shutdown or even with the input power removed. No series output diode is required as reverse current flow is internally limited to about 5μA.

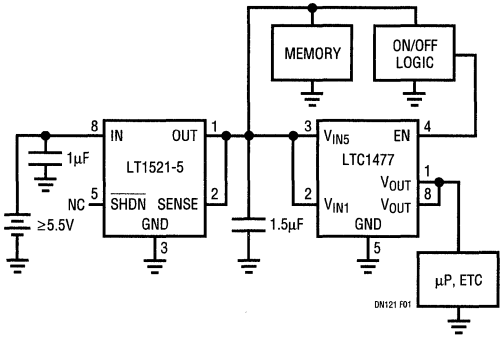


Figure 1. The LT1521's 12μA Standby Current Eliminates the Need for a Separate Memory Backup Supply

A common problem in portable equipment is the chance of installing the batteries backwards, thereby destroying the electronics contained within. The LT1521 needs no reverse protection diode to guard against this condition, as it is designed to withstand up to –20V input while also protecting the load. Low dropout is preserved.

Most important for battery applications is low dropout, a characteristic not neglected in the design of the LT1521. At 300mA the dropout is just 500mV, dropping to approximately 290mV at a 50mA load. This enables the LT1521 to maintain regulation while draining the last drop of power from the battery.

Like the LT1521, the LT1175 also features low dropout, running 500mV at 500mA load current. Quiescent current is 45μA dropping to 10μA in shutdown.

The LT1175 offers several unique features not available in other negative regulators. First, the current limit is adjustable by pin strapping to 200mA, 400mA, 600mA or 800mA. This allows the current limit to be tailored to suit normal load requirements while not exceeding the maximum safe current drain from the battery during a short-circuit fault.

Shutdown on a negative regulator could be a mixed blessing, particularly if positive logic was used to control a negative input. The LT1175 solves this problem by accepting either positive or negative shutdown signals. Holding the Shutdown pin within 0.8V of ground disables the LT1175. If pulled to 2.5V or more *positive or negative* with respect to ground, the regulator is enabled. If shutdown is not desired, either float or connect the Shutdown pin to V_{IN} and the regulator will be enabled whenever power is applied.

The LT1521 and LT1175 work well together as the basis for a split supply as shown in Figure 2. Low output capacitance requirements allow the use of ceramic units instead of larger, more expensive electrolytic or tantalum capacitors.

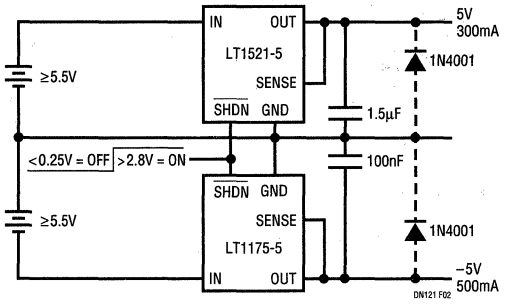


Figure 2. In a Split Supply Application the Shutdown Pins May Be Commanded in Parallel Using Positive Logic

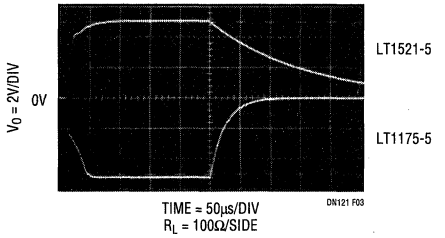


Figure 3. Clean Start-Up and Shutdown is Assured by Utilizing Ganged Shutdown Control of the LT1521 and LT1175.

Owing to the LT1175's unique Shutdown pin, the Shutdown pins of both devices can be joined together as shown and driven from a positive control logic signal. Behavior of the outputs relative to shutdown control is shown in Figure 3.

Although the LT1521-5 can tolerate up to –20V forced output potential with respect to its input, supply reversal diodes (1N4001) are often required to protect both linear and digital load circuitry from damage under transient start-up or fault conditions. The LT1175 is designed to withstand up to +2V forced output voltage. For both devices, start-up and recovery from short-circuit or thermal shutdown is guaranteed under these conditions.

As anyone who has designed and built a "single supply" op amp circuit can attest, few can be implemented without the use of a mid-supply bias point or resistive divider providing that same function. The LT1118 serves as a low power means of obtaining a regulated, low dropout bias point for critical applications. This device features the ability to both source and sink load current (+800mA, –400mA), and exhibits an output impedance of about 16µH across a wide range of frequencies. The output remains stable irrespective of any bypass capacitance of 220nF or more. An output impedance of less than 3Ω can be acheived across a 10MHz bandwidth with the addition of a 1µF bypass; less than 1Ω with a 10µF bypass.

The LT1118 is available in 5V, 2.85V and 2.5V versions. Where the 5V version might serve as a stand alone regulator, the 2.5V version is a good choice for splitting an existing 5V rail (see Figure 4). In addition to greatly reducing power consumption, the DC output impedance is less than 0.025Ω—unmatched by any resistive divider solution. A separate Enable pin shuts off the LT1118, reducing its supply current to 1µA. Figure 5 shows typical output impedance under a variety of operating conditions.

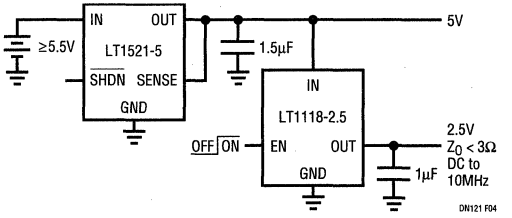


Figure 4. Splitting the Supply Saves Power and Holds Bias Point DC Resistance to Less Than 0.025Ω

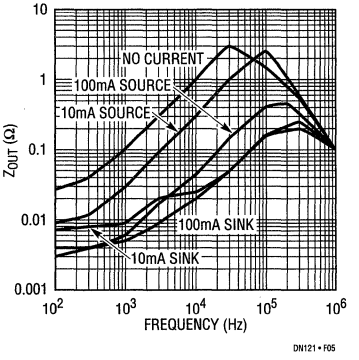


Figure 5. LT1118-2.5 Output Impedance vs Frequency

For literature on our Linear Regulators, call **1-800-4-LINEAR**. For applications help, call (408) 432-1900, Ext. 361

DESIGN NOTES

Dual Regulators Power Pentium® Processor or Upgrade CPU

Design Note 122

Craig Varga

Many manufacturers of Pentium® processor-based motherboards have been searching for an economical solution to the problem of powering the present generation Pentium P54C and accommodating the upgrade processors that will soon become available. The existing processor uses a single supply for both the processor core and the I/O. For the highest frequency offerings, the supply required is 3.5V ±100mV (VRE specification). For the lower performance end of the clock frequency spectrum, a supply voltage of 3.3V ±5% is adequate. Recently, Intel respecified the standard 3.3V CPUs for operation at 3.5V. This allows designs for any clock frequency to be operated from a single 3.5V supply. The I/O ring and chipset should be powered by the same voltage as the CPU core, whether that is 3.3V or 3.5V.

The P55C upgrade processor, which will soon be available, requires separate supplies for the core and the I/O. The nominal core voltage is targeted at 2.500V ±5%, whereas the I/O supply is still nominally 3.3V. There is also a processor pin, V_{CC2DET}, at location AL1, that is bonded to ground on the P55C, but is open on the P54C. A significant complication is introduced by the core and I/O power pins of the P54C being shorted together on-chip. Figure 1 shows the system block diagram. If the core and I/O supplies don't deliver proportional currents, damage to the P54 metallization may occur. The LT®1580/LT1587-based circuit shown in Figure 2 will automatically supply the required voltages to the CPU and the I/O circuitry based on the status of the V_{CC2DET} pin and share the load between the two regulators.

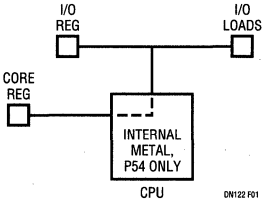
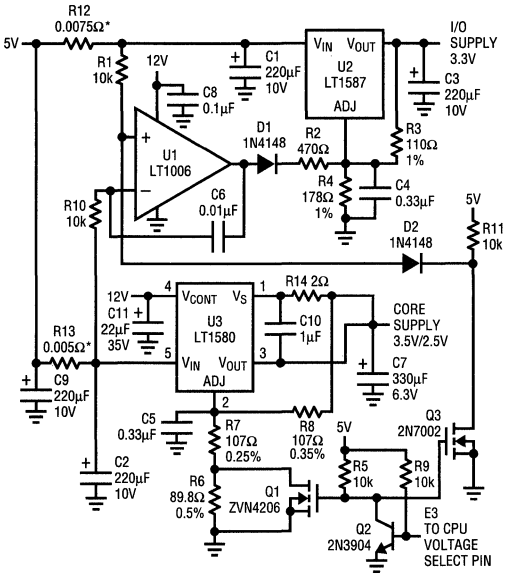


Figure 1. System Configuration

A Simple Solution

This dual linear regulator circuit employs an LT1580 for the CPU core supply and an LT1587 for the I/O supply. The LT1580 has a precision reference, remote sense and exceptionally low dropout voltage. It is capable of meeting the stringent VRE voltage specification when subjected to the scrutiny of worst-case analysis. The LT1587 is rated at 3.0A maximum current and is adequate to power the I/O supply of most desktop systems. If more than 3A of I/O current is required—your design has a very large L2



*RESISTORS ARE IMPLEMENTED AS COPPER TRACES ON PCB
IF 1 OZ COPPER, TRACE WIDTHS ARE 0.05 INCH
IF 2 OZ COPPER, TRACE WIDTHS ARE 0.025 INCH
R13 IS 0.83 INCHES LONG, R12 IS 1.24 INCHES LONG

E3	CPU TYPE
0	P55C
1	P54C

Figure 2. Power Supply Schematic Diagram

cache, for example—an LT1585A, which is capable of 5.0A, may be substituted for the LT1587 by changing one resistor value (R12). See the Design Equations for details.

Op amp U1 forces the two regulators to share the load current when the outputs are shorted together by the CPU metalization. The load current is sensed by the two low value current sense resistors R12 and R13. These resistors are actually implemented as short traces on the PC board. The design does not depend on the sense resistors' absolute values being accurate; only ratiometric matching is required for the circuit to function properly. The resistance ratio will be very well-controlled across PC board production lots.

Amplifier U1 pulls up on the Adjust pin of U2, raising the output voltage of the I/O regulator until the proper current ratio between the two regulators is established. This condition is met when the voltage drop across the sense resistors is equal. The regulator currents are inversely proportional to the sense resistor values, and hence, to the resistor trace lengths. If a different current ratio is desired, just refigure the trace lengths per the equations given. The voltage drop across the resistors at full load is approximately 25mV. Of course, discrete resistors may be used if desired, but they are quite costly compared to a PC board trace.

Nonideal components will translate into errors in the current sharing ratio. With the components shown, the largest contributor to current-sharing errors is the error amplifier offset voltage. The very low offset of the economical LT1006CS8 (400μV max) ensures a worst-case share error of only 1.6%. If the through hole version of the LT1006 is used, this error drops by a factor of five. It is possible to further reduce the value of the sense resistors with this op amp.

If a user should upgrade to a P55C, E3 is now connected to ground. This turns off Q2, allowing Q1 and Q3 to turn on. Q1 shorts out part of the feedback divider of the LT1580, lowering its output to 2.500V. Q3 pulls the noninverting input of U1 low, forcing the op amp output to ground. D1 is now back biased, effectively disconnecting the op amp from the circuit, which causes the I/O regulator's output to drop to 3.3V. Resistor R11 pulls up the cathode of D2 when powering a P54 so that diode leakage current does not cause an error in current sharing.

The LT1580 permits remote sensing of the load voltage at the CPU. Also, by inserting a low value resistor in the sense line, a small intentional load regulation error is introduced, which, it can be shown, will reduce the peak-to-peak transient response of the regulator. The regulation error is well-controlled at the load and is not a function of any trace resistance or parasitics. This technique realizes a reduction in the amount of output capacitance required to control the core voltage transients.

Conclusion

With a small number of low cost components, it is possible to eliminate the need for replaceable power supply modules and still accommodate the desire to upgrade the microprocessor to improved technology. Moreover, the solution results in an "idiot proof" design, preventing the application of an inappropriate supply voltage, which could damage an expensive CPU.

Design Equations:

Assume V_S of approximately 25mV,

$$R13 = \frac{V_S}{I_{CORE}} \quad R12 = \frac{I_{CORE}}{I_{I/O}}(R13)$$

1oz copper thickness is 0.0036cm

2oz copper thickness is 0.0071cm

for 1oz copper PC board, use 0.127cm (0.050") wide traces

for 2oz copper PC board, use 0.064cm (0.025") wide traces

$$L = \frac{R}{R_S}(t)(w)$$

Where L is the trace length in cm

R is the desired resistance

R_S is the specific resistivity of copper: 1.72μΩ cm

t is the copper thickness of the PC board in cm

For literature on our Low Dropout Regulators, call **1-800-4-LINEAR**. For applications help, call (408) 432-1900, Ext. 2360

LINEAR TECHNOLOGY

DESIGN NOTES

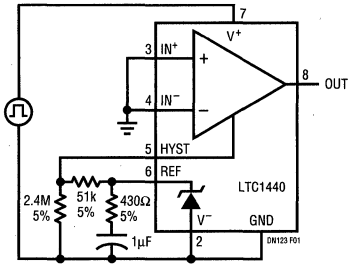
Ultralow Power Comparators Include Reference

Design Note 123

Robert Reay

With the explosion of battery-powered products has come the need for circuits that draw as little supply current as possible in order to extend battery life. Linear Technology's new family of micropower comparators with built-in references is designed to meet that need. Drawing only 1µA of supply current per comparator, the LTC®1440–LTC1445 family provides the perfect solution to battery-powered system monitoring problems.

The LTC1440–LTC1445 family features 1µA comparators, adjustable hysteresis, TTL/CMOS outputs that sink and source current and a 1µA reference that can drive a bypass capacitor of up to 0.01µF without oscillation. The parts operate from a 2V to 11V single supply or a ±1V to ±5V dual supply. Each comparator's input voltage range swings from the negative supply rail to within 1.3V of the positive supply. The comparator propagation delay is 12µs with a 10mV overdrive, and the supply current glitches that commonly occur when comparators change logic states have been eliminated. Table 1 summarizes the features of each member of the family.



Test Circuit

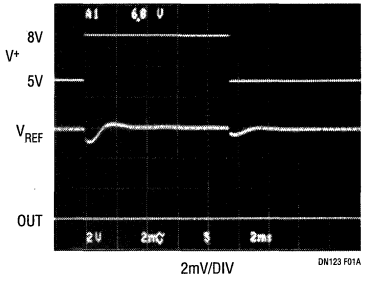


Figure 1. Reference Settling

Voltage Reference

The internal bandgap voltage reference has an output voltage of 1.182V above V– for the LTC1440–LTC1443 and 1.22V ±1% for the LTC1444 and LTC1445. The reference output is capable of sourcing up to 200µA and sinking 15µA. The reference output can directly drive an external bypass capacitor up to 0.01µF without oscillation. By placing a resistor in series with the bypass capacitor, ringing at the reference output can be eliminated and a greater capacitance value can be used. The bypass capacitor prevents reference load transients or power supply glitches from

Table 1.

PART NUMBER	NUMBER OF COMPARATORS	SUPPLY	SUPPLY CURRENT	ADJUSTABLE HYSTERESIS	REFERENCE	COMPARATOR OUTPUT
LTC1440	1	Dual	2.5µA	Yes	1.182V ±1%	CMOS
LTC1441	2	Single	3.5µA	No	1.182V ±1%	CMOS
LTC1442	2	Single	3.5µA	Yes	1.182V ±1%	CMOS
LTC1443	4	Dual	5.0µA	No	1.182V ±1%	CMOS
LTC1444	4	Single	5.0µA	Yes	1.221V ±1%	Open Drain
LTC1445	4	Single	5.0µA	Yes	1.221V ±1%	CMOS

disturbing the reference voltage, which helps eliminate false triggering of the comparators when they are connected to the reference. Figure 1 shows the reference voltage settling during a power supply transient.

Undervoltage/Overvoltage Detector

The LTC1442 can be easily configured as an undervoltage and overvoltage detector as shown in Figure 2. R1, R2 and R3 form a resistive divider from V_{CC} so that comparator A goes low when V_{CC} drops below 4.5V, and comparator B goes low when V_{CC} rises above 5.5V. A 10mV hysteresis band is set by R4 and R5 to prevent oscillations near the trip points.

Single Cell Lithium-Ion Battery Supply

Figure 3 shows a single cell lithium-ion battery to 5V supply with the low-battery warning, low-battery shutdown and reset functions provided by the LTC1444. The LT®1300 micropower step-up DC/DC converter boosts the battery voltage to 5V using L1 and D1. Capacitors C2 and C3 provide input and output filtering.

The voltage monitoring circuitry takes advantage of the LTC1444's open-drain outputs and low supply voltage operation. Comparators A and B, along with R1, R2 and R3, monitor the battery voltage. When the battery voltage drops below 2.6V, comparator A's output pulls low to generate a nonmaskable interrupt to the microprocessor to warn of a low-battery condition. To protect the battery from

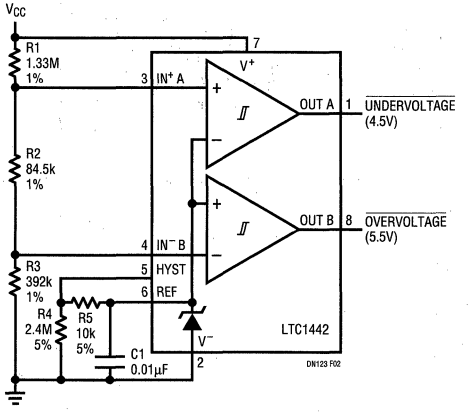


Figure 2. Undervoltage/Overvoltage Detector

overdischarge, the output of comparator B is pulled high by R7 when the battery voltage falls below 2.4V. P-channel Q1 and the LT1300 are turned off, dropping the quiescent current to 20µA. Q1 is needed to prevent the load circuitry from discharging the battery through L1 and D1.

Comparators C and D provide the reset input to the microprocessor. As soon as the boost converter output rises above the 4.65V threshold set by R8 and R9, comparator C turns off and R10 starts to charge C4. After 200ms, comparator D turns off and the Reset pin is pulled high by R12.

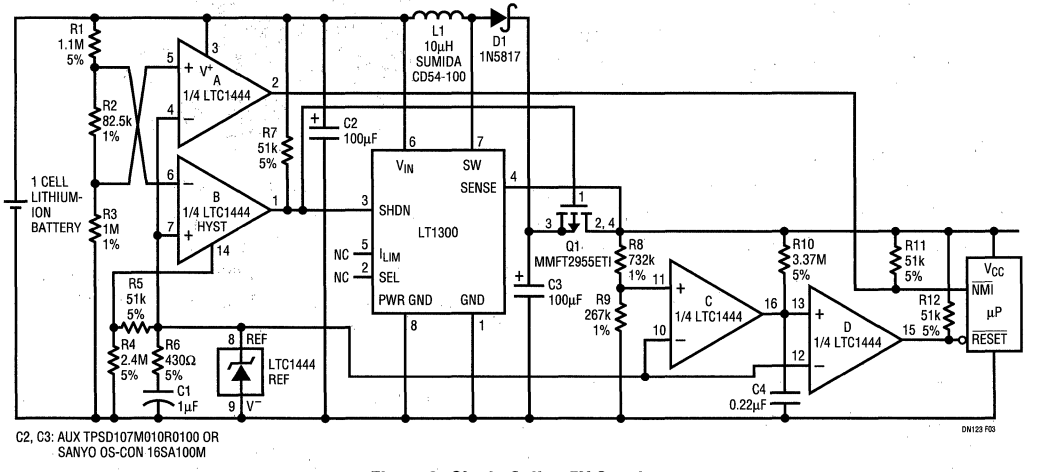


Figure 3. Single Cell to 5V Supply

For literature on our Comparators, call **1-800-4-LINEAR**. For applications help, call (408) 432-1900, Ext. 456

LINEAR TECHNOLOGY

DESIGN NOTES

New Battery Charger ICs Need No Heat Sinks

Design Note 124

Carl Nelson

The LT®1510 and LT1511 are high efficiency battery-charging chips capable of output powers up to 25W and 50W, respectively. These chips are intended for fast-charging batteries in modern portable equipment where space is at a premium. They are therefore packaged in low profile surface mount packages and run at a fairly high frequency (200kHz) to minimize the height and footprint of the complete battery charger. To minimize thermal resistance, these packages are specially constructed with the die-attach paddle connected (fused) directly to multiple package leads.

When operating these chips near their maximum power levels, extra care should be taken to minimize chip power dissipation and to keep the overall thermal resistance of the package-board combination as low as possible. Figure 1 shows a simple way to reduce power dissipation with no loss in performance. The LT1510 and LT1511 use an external diode (D2) and capacitor (C_X) to generate a voltage that is higher than the input voltage. This voltage is used to supply the base drive to the internal NPN power switch to allow it to saturate with a forced h_{FE} of about 50. Switching speed and on-resistance losses are minimized with this technique. The *required* boost voltage is only 3V, but with the normal connection of D2, the resulting boost voltage is equal to the battery voltage. Unnecessarily high base drive losses result with high battery voltages. Connecting D2 to a 3.3V or 5V supply (V_X) instead of to the battery reduces chip dissipation by approximately:

$$\text{Power reduction} = (V_{BAT} - V_X)(I_{CHRG})(V_{BAT})/(50)(V_{IN})$$

With a 20V adapter charging a 12.6V battery at 3A, and V_X = 3.3V, chip power is reduced by 0.35W.

Fused-lead packages conduct most of their heat out the leads. This makes it very important to provide as much PC board copper around the leads as is practical. Total thermal resistance of the package-board combination is dominated by the characteristics of the board in the immediate area of the package. This means both lateral thermal resistance across the board and vertical thermal resistance through the board to other copper layers. Each layer acts as a thermal heat spreader that increases the heat sinking effectiveness of extended areas of the board.

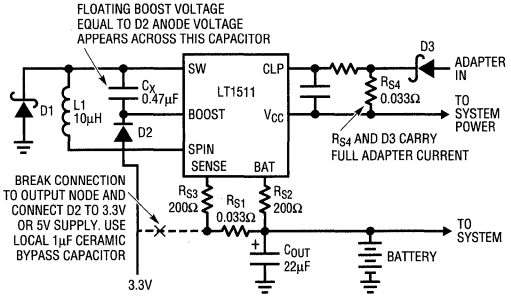


Figure 1

Total board area becomes an important factor when the area of the board drops below about 20 square inches. The graphs in Figures 2 and 3 show thermal resistance versus board area for 2-layer and 4-layer boards. Note that 4-layer boards have significantly lower thermal resistance, but both types show a rapid increase for reduced board areas. Figures 4 and 5 show actual measured lead temperatures for chargers operating at full current. Battery voltage and input voltage will affect device power dissipation, so the data sheet power calculations must be used to extrapolate these readings to other situations.

Vias should be used to connect board layers together. Planes under the charger area can be cut away from the rest of the board and connected with vias to form both a low thermal resistance system and to act as a ground plane for reduced EMI.

Glue-on, chip-mounted heat sinks are effective only in moderate power applications where the PC board copper cannot be used, or where the board size is small. They offer very little improvement in a properly laid out multilayer board of reasonable size.

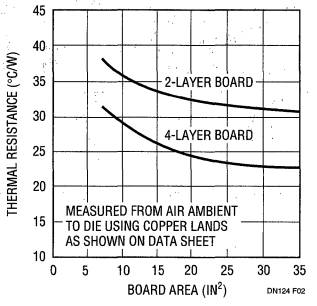


Figure 2. LT1511 Thermal Resistance

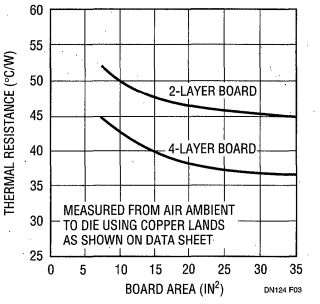


Figure 3. LT1510 Thermal Resistance

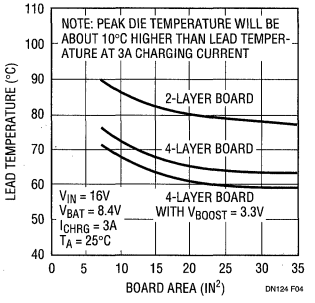


Figure 4. LT1511 Lead Temperature

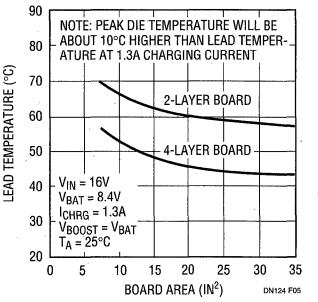


Figure 5. LT1510 Lead Temperature

The suggested methods for a final check on chip operating temperature are to solder a small thermocouple on top of one of the IC ground leads or to use an IR sensor on top of the package. Using either method, the temperature measured either way will be about 10°C lower than actual peak die temperature when the charger is delivering full current. The 125°C rating of these charger chips means that lead temperature readings as high as 100°C (with maximum ambient temperature) are still comfortably within the device ratings.

Another consideration is the power dissipation of other parts of the charger and the surrounding circuitry used for other purposes. The catch diode (D1) will dissipate a power equal to:

$$P_{DIODE} = (I_{CHRG})(V_F)(V_{IN} - V_{BAT})/V_{IN}$$

With the V_{IN} = 16V, V_{BAT} = 8.4V, V_F = 0.45V, and I_{CHRG} = 3A, the diode dissipates 0.64W. Unfortunately, it must be located very close to the charger chip to prevent inductive spikes on the Switch pin. Increase in charger chip temperature due to power dissipation in D1 is about 12°C/W. D3 is used for input protection and can also dissipate significant power but it can be located away from the charger. The current sense resistors used with the LT1511 dissipate power equal to:

$$P(R_{S1}) = R_{S1}(I_{CHRG})^2$$

$$P(R_{S4}) = R_{S4}(I_{ADPT})^2$$

R_{S4} power depends only on charger output current, but R_{S1} carries full adapter current. These resistors, which typically dissipate a total of about 0.5W, will also increase chip temperature at about 12°C/W, assuming that they are close to the charger chip.

It is assumed that L1 contributes only slightly to chip temperature rise because its power dissipation is normally fairly low compared to its heat sinking ability. This will be true if a low loss core is used (Kool Mμ®, etc.), and the winding resistance is less than $0.2V/I_{CHRG}$. If the charger is located near other high power dissipation circuitry, direct temperature testing may be the only accurate way to ensure safe device temperatures.

Finally, don't forget about losses in PC board trace resistance. A 100mil wide trace is huge by modern standards, but a pair of these traces six inches long, in 1/2oz copper, delivering 3A, would have a resistance of ≈ 0.12Ω, and a power loss of 1.1W!

For literature on our Battery Chargers, call **1-800-4-LINEAR**. For applications help, call (408) 432-1900, Ext. 361

Kool Mμ is a registered trademark of Magnetics, Inc.

LINEAR TECHNOLOGY

DESIGN NOTES

Monolithic DC/DC Converters Break Speed Limits to Shrink Board Space

Design Note 125

Mitchell Lee

In the never-ending quest for board space, operating frequency remains the most important variable in a DC/DC converter design. Higher frequency equates with smaller coils and capacitors. A new family of fast monolithic converters that allows circuit designers to reduce the size of their finished products is now available. Other improvements include quiescent currents well below those of slower converters and a new switch-drive technique that reduces dynamic losses by at least four fold over previous methods, virtually eliminating these losses as a concern in efficiency calculations.

Table 1 shows the salient features of each member of the family. Each is configured as a grounded-switch step-up converter, but is equally useful in positive and negative high efficiency buck, SEPIC, inverting and flyback circuits. The converters are all based on the LT®1372 design, which operates at 500kHz, draws 4mA quiescent current and contains a 1.5A, 0.5Ω switch. The LT1371 is designed for higher power applications, with a 3A, 0.25Ω switch. Supply current and operating frequency remain unchanged. Reduced quiescent current (1mA) makes the LT1373 useful in low power designs or in applications where the load current has a wide dynamic range. For the ultimate in miniaturization, the LT1377 features 1MHz operating frequency—especially helpful where post filtering is employed.

Table 1. Family Characteristics

DEVICE	I_Q	SWITCH	FREE RUNNING FREQUENCY	SYNCHRONIZATION LIMIT
LT1371	4mA	3A	500kHz	800kHz
LT1372	4mA	1.5A	500kHz	800kHz
LT1373	1mA	1.5A	250kHz	360kHz
LT1377	4mA	1.5A	1MHz	1.6MHz

All devices share the same constant-frequency PWM core, up to 90% duty cycle and 2.7V to 30V supply range with a maximum switch rating of 35V. Unique to these devices is a synchronization input that allows the internal oscillator to be overridden by an external clocking signal. The synchronization limit for each part is also shown in Table 1. Another unique feature is a second Feedback pin that allows direct regulation of negative outputs.

A simple boost converter using the LT1372 is shown in Figure 1. 350mA output current is available at 12V from a 5V input. Adaptive switch drive and a 0.5Ω collector resistance result in a peak efficiency of 87%, as shown in Figure 2.

Figure 3 shows a buck-boost (SEPIC) converter built around the 3-ampere LT1371. Inputs of 2.7V to 20V are converted to a 5V regulated output at up to 1.8A (see Figure 4). In spite

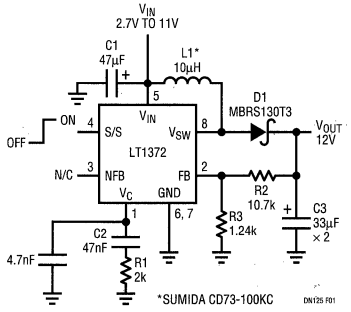


Figure 1. Schematic Diagram: LT1372 Boost Converter

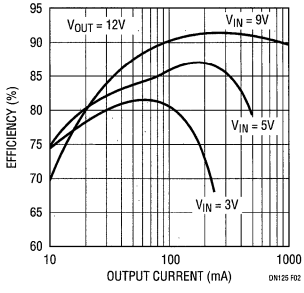


Figure 2. Efficiency of Boost Converter Shown in Figure 1

of handling 9W output power, the 500kHz operating frequency of the LT1371 allows a 0.37-inch toroidal core to be used for the coupled inductor, with excellent efficiency. In shutdown, the output is completely disconnected from the input source.

The latest generation of disk drives has adopted magneto-resistive (MR) read-write heads. These operate with a low noise bias supply of –3V. Figure 5 shows a Cuk-configured LT1373 capable of generating –3V at 250mA. This converter topology exhibits inherently low output ripple and noise and uses a single-core coupled inductor. Operating at 250kHz allows the use of relatively small filter components. The speed-to-power ratio of the LT1373 is quite high; with only 1mA quiescent current, it maintains higher efficiency at light loads.

At the other end of the spectrum is the 1MHz LT1377. It has the same high speed-to-power ratio as the LT1373. In Figure 6 the LT1377 is used as a 50mA charger for 4 to 6 NiCd cells, operating from a 5V input. The charger is clamped against excessive output voltage at 11V, and maintains constant output current from 0V to 11V.

1MHz operation is also useful in radio applications where a 455kHz IF is present, as it gives one octave separation from that critical frequency. Figure 7 shows the LT1377 configured as a high efficiency buck converter, with a 5V, 1A output. A 20µH inductor is used in this application to maintain a low ripple current (10%), thus easing output filtering requirements.

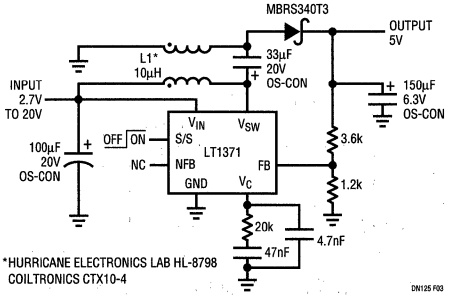


Figure 3. 5V, 9W Converter Operates Over Wide Input Range with Good Efficiency

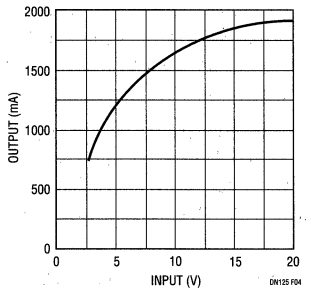


Figure 4. Maximum Available Output Current of LT1371 9W Converter (Figure 3)

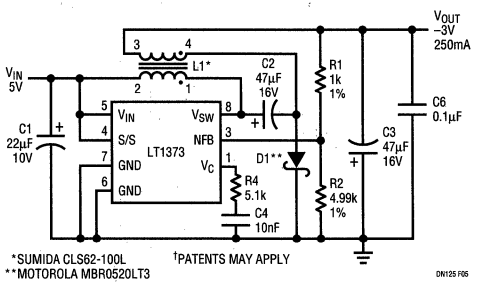


Figure 5. Low Ripple 5V to –3V "Cuk"† Converter

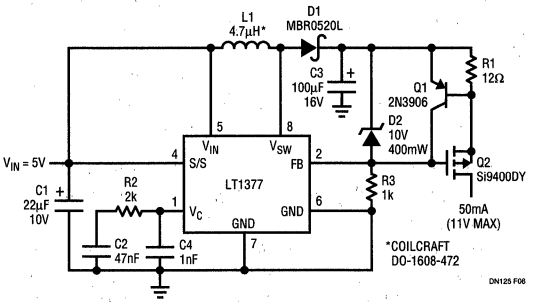


Figure 6. Battery Charger

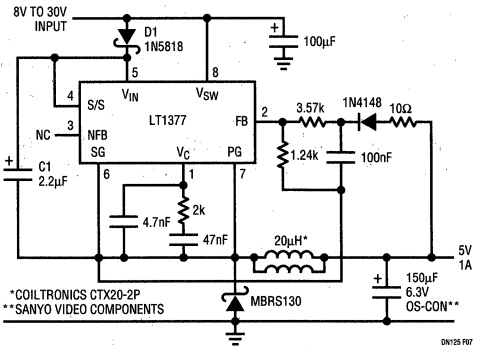


Figure 7. 1MHz LT1377-Based Buck Converter

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LINEAR TECHNOLOGY

DESIGN NOTES

The LT1166: Power Output Stage Automatic Bias System Control IC – Design Note 126

Dale Eagar

Class AB amplifiers are popular because of their "near Class A" performance and their ability to operate on considerably less quiescent power than Class A. Class AB amplifiers are easy to construct, rugged and reliable. However, there is an aspect of these amplifiers that can cause perplexity, consternation and finally hair loss—their bias scheme. The problem is that the very parameter that makes Class AB so good, namely, low quiescent current, is poorly controlled. The LT®1166 offers control over the quiescent current directly, removing the necessity of temperature tracking, matching transistors or trim pots. In addition, it removes all excess crossover distortion caused by improperly set quiescent current, and significantly reduces the distortion caused by the effects of nonlinear transconductance in the output transistors.

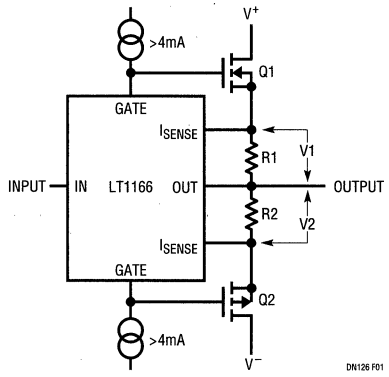


Figure 1. Basic LT1166 Circuit Configuration

Functional Description

The LT1166 (Figure 1), combined with external transistors, implements a unity-gain buffer. The circuit controls the Class AB output stage by incorporating two control loops, the current-control loop and the voltage-control loop. The current-control loop (Figure 2) operates independently of the voltage loop while keeping the product of V1 and V2 constant. The voltage loop maintains the output voltage at the input voltage level by driving both gates up or down. The two loops, although mutually independent, act in harmony to provide a component insensitive, temperature insensitive, simple Class AB bias network.

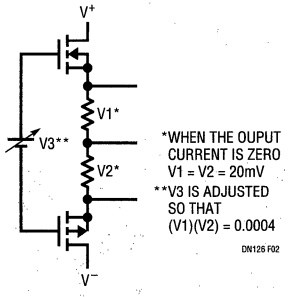


Figure 2. LT1166 Current-Control Loop

Parallel Operation

Parallel operation is an effective way to get more output power by connecting multiple power drivers. All that is required is a small ballast resistor to ensure current sharing between the drivers and an inductor to isolate the drivers at high frequencies. In Figure 3 one power slice can deliver ±6A at $100V_{PK}$ or $300W_{RMS}$ into 16Ω. Adding another slice boosts the power output to $600W_{RMS}$ into 8Ω and adding two or more drivers theoretically raises the power output to $1200W_{RMS}$ into 4Ω. Due to IR losses across the sense resistors, the FET R_{ON} resistance at 10A and some sagging of the power supply, the circuit of Figure 3 actually delivers $350W_{RMS}$ into 8Ω. Performance photos are shown in Figures 4 and 5. Frequency compensation is provided by the 2k input resistor, 180µH inductor and the 1nF compensation capacitors. The common node in the auxiliary power supplies is connected to the amplifier output to generate the floating ±15V supplies.

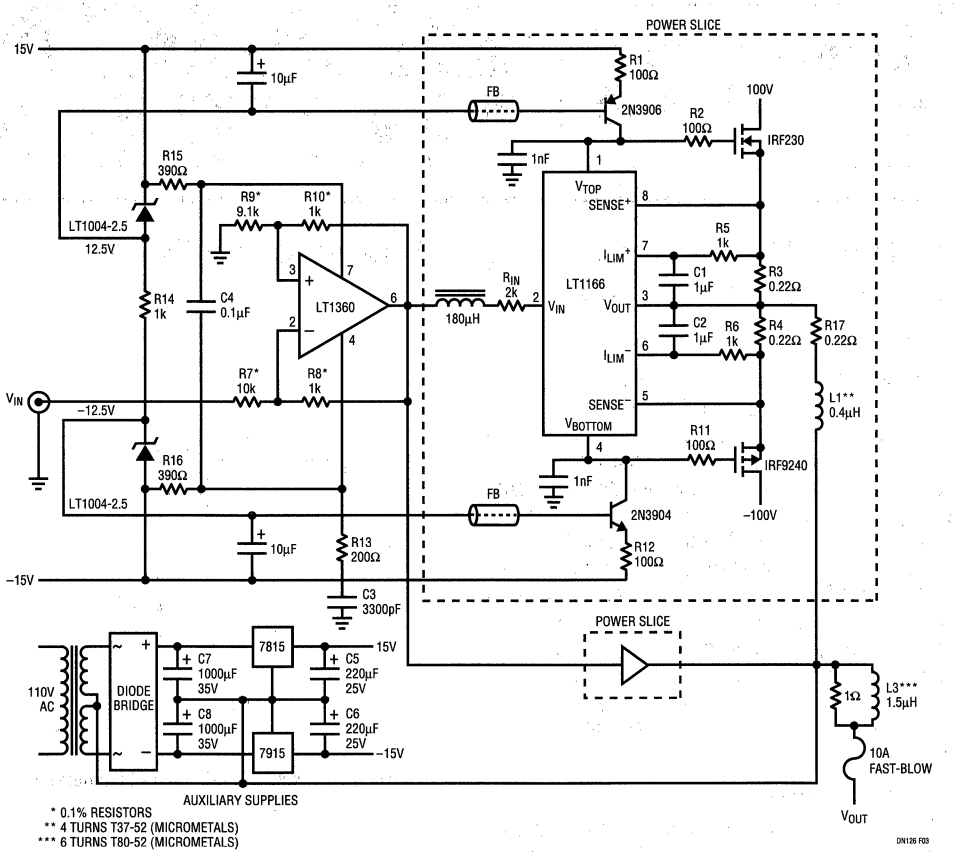
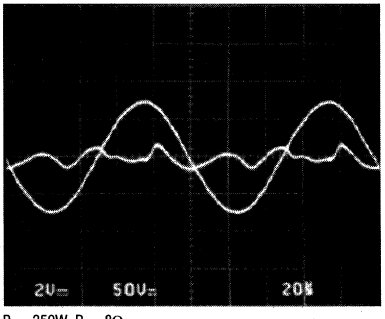


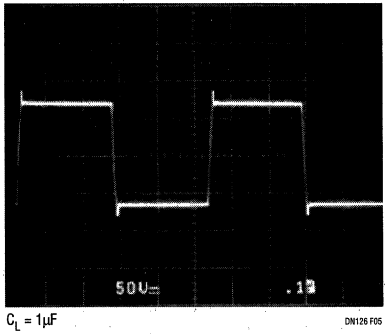
Figure 3. 350W Power Amplifier



P_O = 350W, R_L = 8Ω

DN126 F04

Figure 4. 0.3% THD at 10kHz



C_L = 1µF

DN126 F05

Figure 5. 2kHz Square Wave

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LINEAR TECHNOLOGY

DESIGN NOTES

3V and 5V 12-Bit Rail-to-Rail Micropower DACs Combine Flexibility and Performance – Design Note 127

Roger Zemke and Hassan Malik

The LTC®1450 and LTC1450L are complete single supply rail-to-rail voltage output, 12-bit DACs in 24-pin SSOP and PDIP packages. They include an output buffer amplifier, a reference and a double-buffered parallel digital interface. These DACs use a proprietary architecture which guarantees a maximum DNL error of 0.5LSB. A built-in power-on reset ensures that the output of the DAC is initialized to zero scale.

The rail-to-rail buffered output can source or sink 5mA while pulling to within 300mV of the positive supply voltage or ground. The output swings to within a few millivolts of either supply rail when unloaded and has an equivalent output resistance of 40Ω when driving a load to the rails.

Low Power, 5V or 3V Single Supply Operation

The LTC1450 draws only 400µA from a 4.5V to 5.5V supply. The DAC can be configured for a 0V to 4.095V or 0V to 2.048V output range. It has a 2.048V internal reference.

The LTC1450L draws 250µA from a 2.7V to 5.5V supply. It can be configured for a 0V to 2.5V or 0V to 1.22V output range. It has a 1.22V internal reference.

Flexibility with Stand-Alone Performance

The LTC1450/LTC1450L are complete stand-alone DACs requiring no external components. Reference output, reference input and gain setting pins provide the user with added flexibility.

Figure 1 shows how these DACs may typically be used. REF HI is tied to REF OUT and REF LO and X1/X2 are grounded.

4-Quadrant Multiplying DAC Application

Figure 2 shows the LTC1450L configured as a single supply 4-quadrant multiplying DAC. It uses a 5V supply and only one external component, a 5k resistor tied from REF OUT to ground. (The LTC1450 can be used in a similar fashion.) The

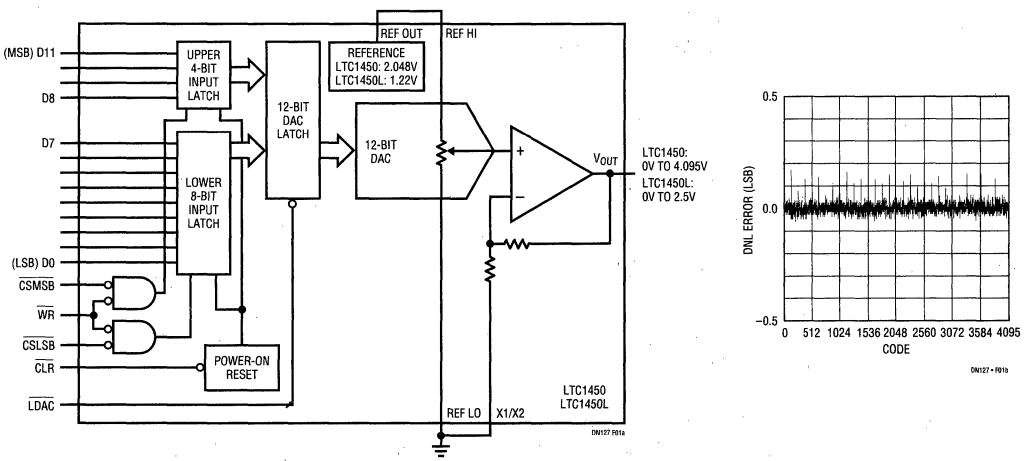

Figure 1. Byte/Parallel Input, Internal/External Reference, Power-On Reset and Gain Select Provide Application Flexibility. The Patented Architecture Guarantees Excellent DNL

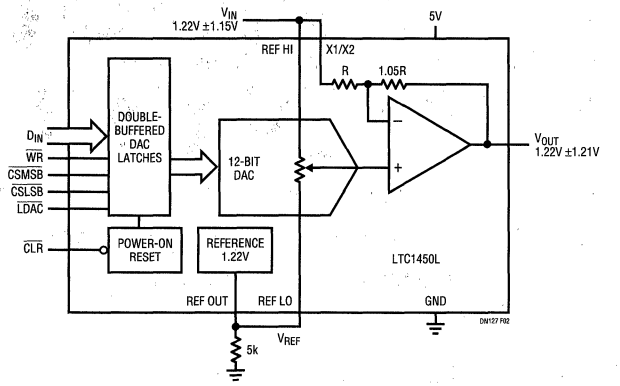

Figure 2. Internal Reference, REF LO/REF HI Pins, Gain Adjust and Wide Supply Voltage Range Allow 4-Quadrant Multiplying on a 5V Single Supply

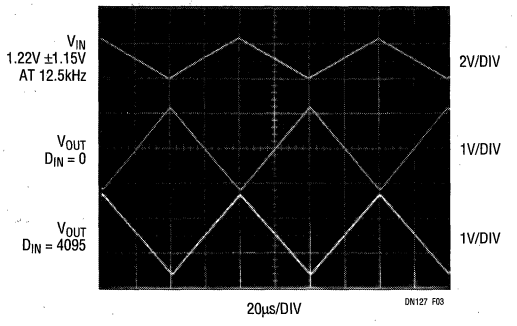

Figure 3. Clean 4-Quadrant Multiplying Is Shown in the Output Waveforms for Zero-Scale and Full-Scale DAC Settings

multiplying DAC allows the user to digitally change the amplitude and polarity of an AC input signal whose voltage is centered around an offset signal ground provided by the 1.22V reference voltage. The transfer function is shown in the following equations.

$$V_{OUT} = (V_{IN} - V_{REF})\left[\text{Gain}\left(\frac{D_{IN}}{4096} - 1\right) + 1\right] + V_{REF}$$

For the LTC1450L Gain = 2.05 and V_{REF} = 1.22V

$$V_{OUT} = (V_{IN} - 122V)\left[2.05\left(\frac{D_{IN}}{4096}\right) - 1.05\right] + 1.22V$$

Table 1 shows the expressions for V_{OUT} as a function of V_{IN}, V_{REF} and D_{IN}. Figure 3 shows a 12.5kHz, 2.3V_{P-P} triangle wave input signal and the corresponding output waveforms for zero-scale and full-scale DAC codes.

Table 1. Binary Code Table for 4-Quadrant, Multiplying DAC Application

BINARY DIGITAL INPUT CODE IN DAC REGISTER			ANALOG OUTPUT (V_{OUT})
MSB		LSB	
1111	1111	1111	$(4094/4096)(V_{IN} - V_{REF}) + V_{REF}$
1100	0001	1001	$0.5(V_{IN} - V_{REF}) + V_{REF}$
1000	0011	0010	V_{REF}
0100	0100	1011	$-0.5(V_{IN} - V_{REF}) + V_{REF}$
0000	0110	0100	$-1.0(V_{IN} - V_{REF}) + V_{REF}$
0000	0000	0000	$-1.05(V_{IN} - V_{REF}) + V_{REF}$

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LINEAR TECHNOLOGY

DESIGN NOTES

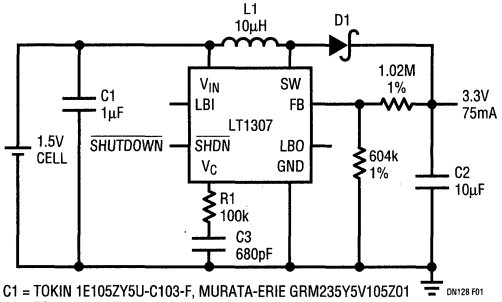
LT1307 Single-Cell Micropower Fixed-Frequency DC/DC Converter Needs No Electrolytic Capacitors – Design Note 128

Steve Pietkiewicz

Today's low power boost converter ICs have been rejected by designers of products incorporating RF communications for two reasons. First, the converters use some form of variable-frequency control to maintain acceptable efficiency during periods of light load. Significant spectral energy in the sensitive 455kHz band can occur, introducing difficult interference problems with the system's IF amplifier. Second, large output capacitors are required to keep output ripple voltage at an acceptable level. Most battery-powered products have neither the space nor budget for the D-case size tantalum capacitor usually required. The LT®1307 current mode PWM switching regulator eliminates these concerns by using small, low cost ceramic capacitors for both input and output and by employing fixed frequency 575kHz operation to keep spectral energy out of the 455kHz band. Dense high speed bipolar process technology enables the LT1307 to fit in the subminiature MSOP package. The LT1307 consumes just 60µA at no load and includes a low-battery detector comparator with a 200mV reference voltage. The internal power switch is rated at 500mA with a V_{CESAT} of 300mV.

Single-Cell Boost Converter

A complete single cell to 3.3V converter is shown in Figure 1. The circuit generates 3.3V at up to 75mA from a 1V input. The 10µF ceramic output capacitor can be obtained from several vendors. Efficiency, detailed in Figure 2, exceeds 70% over the 1:500 load range of 200µA to 100mA at a 1.25V input. Figure 3 shows output voltage and inductor current as the load current is stepped from 5mA to 55mA. The oscillograph reveals substantial detail about the operation of the LT1307. With a 5mA load, V_{OUT} (top trace) exhibits a ripple voltage of 60mV at 4kHz. The device is in Burst Mode™ operation at this output current level. Burst Mode operation enables the converter to maintain high efficiency at light loads by turning



C1 = TOKIN 1E105ZY5U-C103-F, MURATA-ERIE GRM235Y5V105Z01
C2 = TOKIN 1E106ZY5U-C304-F, MURATA-ERIE GRM235Y5V106Z01
D1 = MOTOROLA MBR0520
L1 = SUMIDA CD43-100

Figure 1. Single Cell to 3.3V Boost Converter Delivers 75mA at a 1V Input

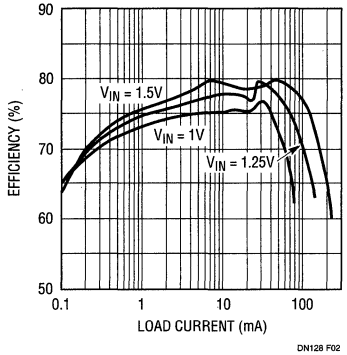


Figure 2. 3.3V Converter Efficiency

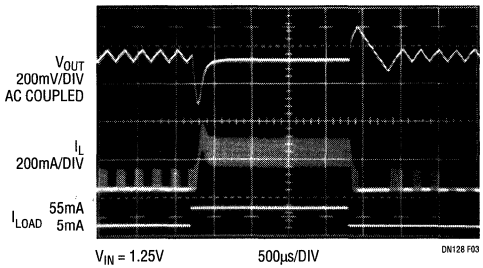


Figure 3. Transient Response with 5mA to 55mA Load Step

off all circuitry inside the LT1307 except the reference and error amplifier. When the LT1307 is not switching, quiescent current decreases to 60μA. When switching, inductor current (middle trace) is limited to approximately 100mA. Switching frequency inside the "bursts" is 575kHz. As the load is stepped to 55mA, the device shifts from Burst Mode operation to constant switching mode. Inductor current increases to about 300mA peak and the low frequency Burst Mode ripple goes away. R1 and C3 stabilize the loop.

455kHz Noise Considerations

Switching regulator noise is a significant concern in many communication systems. The LT1307 is designed to keep noise energy out of the 455kHz band at all load levels while consuming only 60μW to 100μW at no load. At light load levels, the device is in Burst Mode operation, causing low frequency ripple to appear at the output. Figure 4 details spectral noise directly at the output of Figure 1's circuit in a 1kHz to 1MHz bandwidth. The converter supplies a 5mA load from a 1.25V input. The Burst Mode fundamental at 5.1kHz and its harmonics are quite evident, as is the 575kHz switching frequency. Note, however, the absence of significant energy at 455kHz. Figure 5's plot reduces the frequency span from 255kHz to 655kHz with a 455kHz center. Burst Mode low frequency ripple creates sidebands around the 575kHz switching fundamental. These sidebands have low signal amplitude at 455kHz, measuring $-55dBmV_{RMS}$. As load current is further reduced, the Burst Mode frequency decreases. This spaces the sidebands around the switching frequency closer together, moving spectral energy further away from 455kHz. Figure 6 shows the noise spectrum of the converter with the load increased to 20mA. The LT1307 shifts out of Burst Mode operation eliminating low frequency ripple. Spectral energy is present only at the switching fundamental and its harmonics. Noise voltage measures $-5dBmV_{RMS}$ or $560\mu V_{RMS}$ at the 575kHz switching frequency, and is below $-60dBmV_{RMS}$ for all other frequencies in the range. By combining Burst Mode operation with fixed frequency operation the LT1307 keeps noise away from 455kHz making the device ideal for RF applications where the absence of noise in the 455kHz band is critical.

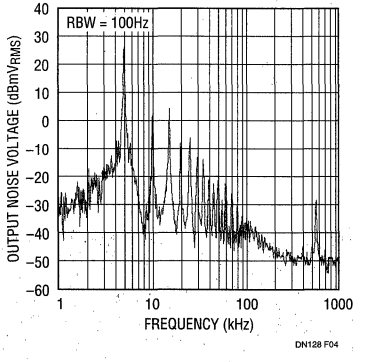


Figure 4. Spectral Noise Plot of 3.3V Converter Delivering 5mA Load. Burst Mode Operation at 5.1kHz is $23dBmV_{RMS}$ or $14mV_{RMS}$. Switching Fundamental at 575kHz is $-31dBmV_{RMS}$ or $28\mu V_{RMS}$

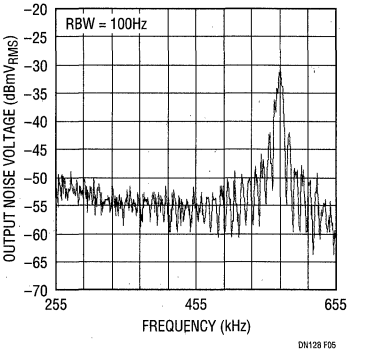


Figure 5. Span Centered at 455kHz Shows $-55dBmV_{RMS}$ ($1.8\mu V_{RMS}$) at 455kHz. Burst Mode Operation Creates Sidebands 5.1kHz Apart About Switching Fundamental of 575kHz

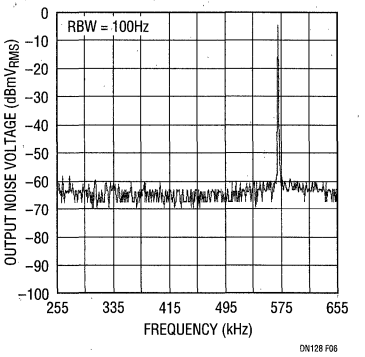


Figure 6. With Converter Delivering 20mA, Low Frequency Sidebands Disappear. Noise is Present Only at the 575kHz Switching Frequency and its Harmonics

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LINEAR TECHNOLOGY

DESIGN NOTES

Precision Receiver Delay Improves Data Transmission

Design Note 129

Victor Fleury

Moving data from one board to another over a backplane places stringent requirements on channel-to-channel and part-to-part skew and delay. The propagation delay of typical CMOS line receivers can vary as much as 500% over process and temperature. In high speed synchronous systems where clock and data signal timing are critical, transmission rates must often be reduced to minimize the effects of propagation delay and skew uncertainties in the receiver. The LTC®1518/LTC1519/LTC1520 family of high speed line receivers solves this problem, reducing propagation delay changes to less than ±17% over production variations and temperature, a better than 10 times improvement over previous solutions.

The LTC1518/LTC1519/LTC1520 family of 50Mbps quad line receivers translate differential input signals into CMOS/TTL output logic levels. The receivers employ a unique architecture that guarantees excellent performance over process and temperature with propagation delay of 18ns ±3ns. The architecture affords low same channel skew ($|t_{PHL} - t_{PLH}|$ 500ps typ), and low channel-to-channel propagation delay variation (400ps typ). The propagation delay and skew performance are unmatched by any CMOS, TTL or ECL line receiver/comparator.

Circuit Description

Figure 1 shows a block diagram of the LTC1520 signal path. The input differential pair amplifies the minimum 500mV input signal level. A resistor network expands the input common mode range of the LTC1520 from 0V to 5V, and expands that of the LTC1518/LTC1519 from –7V to 12V while operating on a single 5V supply. A second differential amplifier (g_m) switches a fixed current into its load capacitance. The output of the second stage is a valid logic level that feeds inverters.

To guarantee tight delay and skew performance, delay within each receiver and between channels must be carefully matched. For the LTC1518/LTC1519/LTC1520, the inherent temperature and process tolerance, along with bias and delay trimming, make it possible to guarantee a propagation delay window more than an order of magnitude tighter than that of the typical CMOS line receiver. Since skew is caused by the unequal charging versus discharging of both internal and external capacitances, the first stages are differential to minimize these effects.

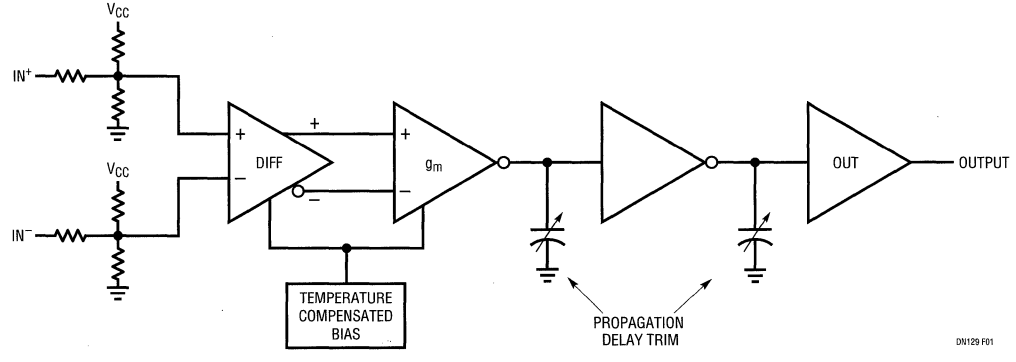

Figure 1. LTC1520 Block Diagram

Additional Features

Other features include novel short-circuit protection. If the output remains in the wrong state for longer than 60ns, the output current is throttled back to 20mA. When the short is removed and the output returns to the correct state, full output drive is restored. Because of its high input impedance (even when unpowered), the LTC1518/LTC1519/LTC1520 can be "hot swapped" without corrupting backplane signal integrity or causing latchup. The outputs remain high with shorted or floating inputs (LTC1518/LTC1519 only) and can be disabled to a high impedance state. High input resistance (≥18k) also allows multiple parallel receivers.

Applications

The LTC1520 is designed for high speed data/clock transmission over short to medium distances. Its rail-to-rail input common mode range allows it to be driven via long PC board traces, coaxial lines or long (hundreds of feet) twisted pairs. Figure 2 shows the LTC1520 in a backplane application. 5V single-ended signals are received with a 2.5V slicing threshold. This configuration can be adapted as a coaxial receiver. In Figure 3, the LTC1518 is shown in an RS485-like application, but capable of operating at up to 50Mbps, limited only by cable characteristics.

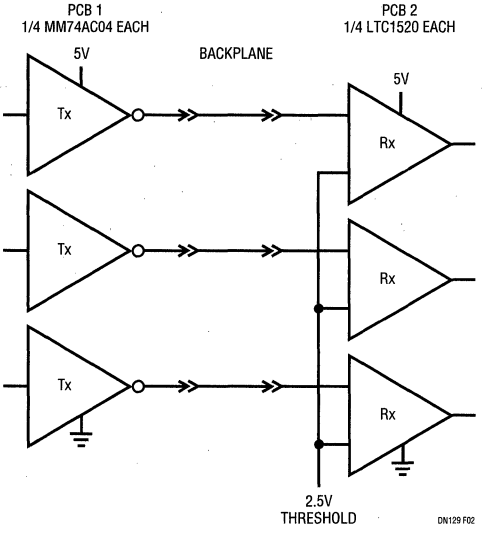

Figure 2

Figure 4 shows actual waveforms of the LTC1518 connected in the Figure 3 configuration (100 feet of unshielded twisted pair was used). Note that the delay of the twisted pair is almost 200ns versus the receiver's 18ns delay.

The waveforms of Figure 5 show 50Mbps operation using the LTC1518 with 100 feet of twisted pair.

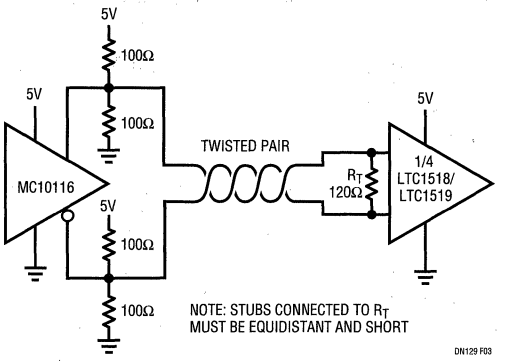

Figure 3. LTC1518 Typical Application

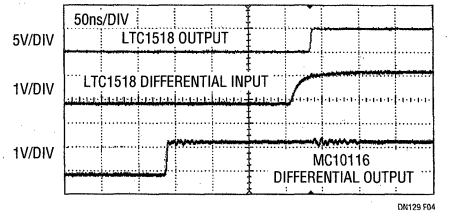

Figure 4. LTC1518 100 Feet Twisted-Pair Connection

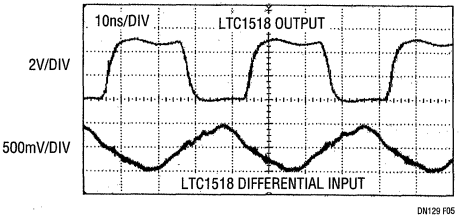

Figure 5. 50Mbps Operation Using 100 Feet of Twisted Pair

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LINEAR TECHNOLOGY

DESIGN NOTES

Power Supplies for Subscriber Line Interface Circuits

Design Note 130

Eddie Beville

As the demand for world wide networking grows, so will the need for advanced data transmission products. In particular, ISDN services have become popular because of the recent development of the Internet. ISDN provides higher speed data transmission than standard modems used in PCs. Also, ISDN supports the standard telephone interface (voice and fax), which includes the Subscriber Line Interface Circuit. A Subscriber Line Interface Circuit requires a negative power supply for the interface and the ringer voltages. The power supplies described herein are designed for these applications. Specifically, these designs address the AMD79R79 SLIC device with on-chip ringing.

CIRCUIT DESCRIPTIONS

LT®1171 Supplies –23.8V at 50mA and –71.5V at 60mA

Figure 1 shows a current mode flyback power supply using the LT1171CQ device. This current mode device has a wide input voltage range of 3V to 60V, current limit protection and an on-chip 65V, 0.30Ω bipolar switch. The input voltage range for the circuit is 9V to 18V. This circuit is intended for small wall adapters that power ISDN boxes. The output voltages are –23.8V at 50mA and –71.5V at 60mA.

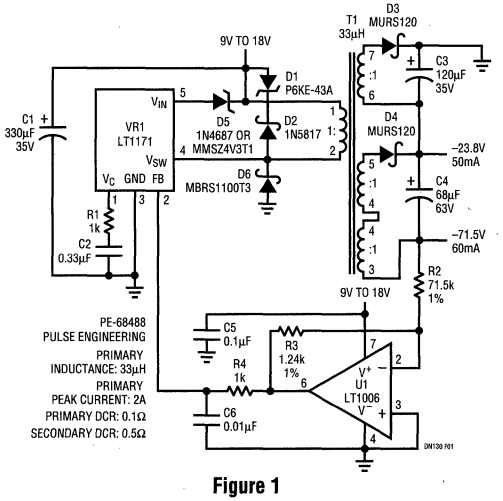


Figure 1

The circuit shown in Figure 1 uses the LT1171 in standard flyback topology. The transformer's turns ratio is 1:1:1:1, where 23.8V appears across each secondary winding and the primary during the switch off time. The remaining secondary windings are stacked in series to develop –47V. The –47V section is then stacked onto the –23.8V section to get –71.5V. This technique provides very good cross regulation, lowers the voltage rating required on the output capacitors and lowers the RMS currents, allowing the use of cheaper output capacitors. Either the –23.8V output or the –71.5V output can be at full load without effecting the other corresponding output. The circuit's step response is very good; no significant overshoot occurs after either output is shorted and released. Also, the transformer windings are all quadrafilar to lower the leakage inductance and cost.

LT1269 Supplies –23.5V at 60mA and –71.5V at 120mA from 5V Input

Figure 2 shows a current mode flyback power supply using the LT1269CQ device. This current mode device has a wide input voltage range, current limit protection and an onboard 60V, 0.20Ω bipolar switch. The input voltage range for the circuit is 5V to 18V. This design provides a wider input voltage range and greater output power than that of Figure 1. The output voltages are –23.5V at 60mA and –71.5V at 120mA (8.6W). This circuit is designed to power two SLIC devices. The circuit operation is identical to Figure 1, except for a larger switching regulator device (VR1) and a different transformer (T1). These changes allow for 5V operation and higher output power. This circuit is designed for full load on the –71V or –23.5V output. This accommodates the ringing on two SLICs or off hook on two SLICs. R5 and R6 are preload resistors for maintaining an accurate –23.5V output at full load with the –71V output at minimum load.

Figure 1 Bill of Materials

REFERENCE DESIGNATOR	QUANITITY	PART NUMBER	DISCRIPTION	VENDOR	TELEPHONE
C1*	1	ECA-1VFQ331	Capacitor, 330µF, 35V HFQ	Panasonic	
C2, C5	1	0805	Capacitor, 0.33µF Ceramic		
C3	1	UPL1V121MPH	Capacitor, 120µF, 35V Plastic	Nichicon	(708) 843-7500
C4	1	UPL1J680MPH	Capacitor, 68µF, 63V Plastic	Nichicon	
C6	2	0805	Capacitor, 0.01µF		
D1	1	P6KE-43A (MOT), TGL41-43A (GI)	Diode, 0.5W Zener	Motorola or Equiv	
D2	1	1N5817	Diode, 1A Schottky	Motorola or Equiv	
D3, D4	2	MURS120	Diode, Ultrafast	Motorola or Equiv	
D5	1	1N4687, MMSZ4V3T1	Diode, Zener	Motorola or Equiv	
D6	1	MBRS1100T3	Diode	Motorola or Equiv	
R1, R4	2	0805	Resistor, 1k, 5% SMT		
R2	1	0805	Resistor, 71.5k, 1% SMT		
R3	1	0805	Resistor, 1.24k, 1% SMT		
T1*	1	PE-68488	Transformer	Pulse Eng	
U1	1	LT1006S8	IC	LTC	(408) 432-1900
VR1*	1	LT1171CQ	IC	LTC	(408) 432-1900
***Changes and Additions for Figure 2's Circuit**					
C1	1	205A100M	Capacitor, 100µF, 20V OS-CON	Sanyo	(619) 661-6835
D5, D7	2	1N4001	Diode		
R5, R6	2		Resistor, 50k 0.25W SMT or Through Hole		
T1	1	HM00-96553	Transformer	BI Technology	(714) 447-2656
VR1	1	LT1269CQ	IC	LTC	(408) 432-1900

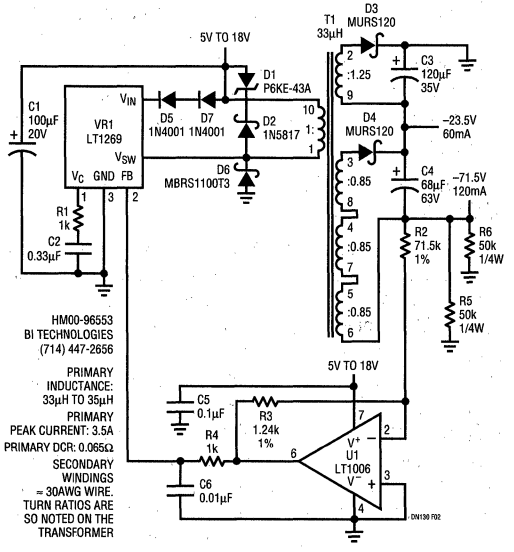


Figure 2

LAYOUT AND THERMAL CONSIDERATIONS

Printed circuit board layout is an important consideration in the design of switching regulator circuits. A good ground plane is required for all ground connections. The path from the input capacitor to the primary winding of the transformer is a high current path, and requires a short, wide copper trace (0.080" to 0.1"). The V_{SW} pin connection also needs a short, wide copper trace. R1 and C2 need to be placed close to VR1. The secondary windings can be connected to their associated components with 0.025" to 0.030" traces. The feedback circuitry needs to be placed close to the FB pin of VR1. Place C5 close to U1 to decouple the op amp power supply. The LT1171CQ and LT1269CQ are surface mount devices that require about a 1" copper pad for heat sink mounting. Heat sinking is most critical for the LT1269CQ because of its high output power. Also, vias from the copper pad to the internal ground layers are highly recommended.

BILL OF MATERIALS

A bill of materials has been provided with each schematic.

For literature on our Power Products, call **1-800-4-LINEAR**. For applications help, call (408) 432-1900, Ext. 2361

LINEAR TECHNOLOGY

DESIGN NOTES

The LTC1446/LTC1446L: World's First Dual 12-Bit DACs in SO-8

Design Note 131

Hassan Malik and Kevin R. Hoskins

The LTC®1446/LTC1446L are the first dual, single supply, rail-to-rail voltage output 12-bit DACs. Both parts include an internal reference and two DACs with rail-to-rail output buffer amplifiers, packaged into a space-saving 8-pin SO or PDIP package. The LTC1446's patented architecture is inherently monotonic and has excellent 12-bit DNL, guaranteed to be less than 0.5LSB. These parts have an easy-to-use SPI compatible interface that allows daisy-chaining.

Low Power 5V or 3V Single Supply

The LTC1446 has an output swing of 0V to 4.095V, with each LSB equal to 1mV. It operates from a single 4.5V to 5.5V supply, drawing 1mA. The LTC1446L has an output swing of 0V to 2.5V, operates on a single 2.7V to 5.5V supply and draws 650µA.

Complete Stand-Alone Performance

Figure 1 shows a block diagram of the LTC1446/LTC1446L. The data inputs for both DAC A and DAC B are clocked into one 24-bit shift register. The first 12-bit segment is for DAC A and the second is for DAC B. Each 12-bit segment is loaded MSB first and latched into the shift register on the rising edge of the clock. When all the data has been shifted in, it is loaded into the DAC registers when the signal on the $\overline{CS}$/LD pin changes to a logic high. This updates both 12-bit DACs and internally disables the CLK signal. The D_{OUT} pin allows the user to daisy-chain several DACs together. Power-on reset initializes the outputs to zero scale.

Rail-to-Rail Outputs

The on-chip output buffer amplifiers can source or sink over 5mA with a 5V supply. More over, they have true rail-to-rail performance. This results in excellent load regulation up to the 4.095V full-scale output with a 4.5V supply. When sinking current with outputs close to zero scale, the effective output impedance is about 50Ω. The midscale glitch on the output is 20nV • s and the digital feedthrough is a negligible 0.15nV • s.

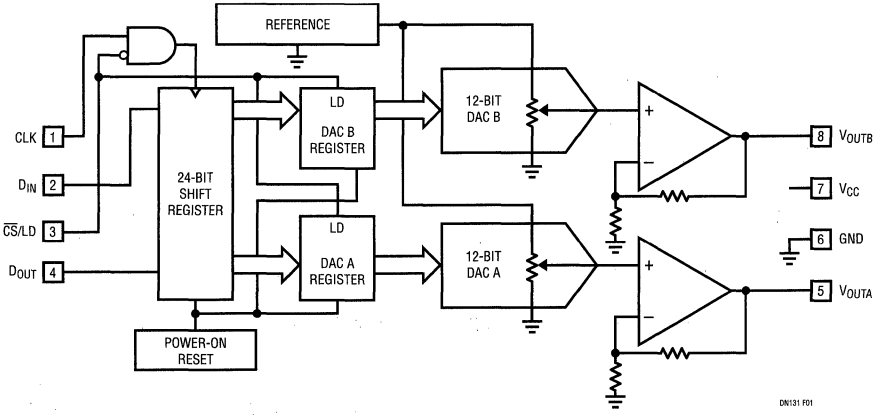


Figure 1. Dual 12-Bit Rail-to-Rail Performance in an SO-8 Package

A Wide Range of Applications

Some of the typical applications for these parts include digital calibration, industrial process control, automatic test equipment, cellular telephones and portable battery-powered applications. Figure 2 shows how easy these parts are to use.

Figure 3 shows how to use one LTC1446 to make an autoranging ADC. The microprocessor adjusts the ADC's reference span and offset by loading the appropriate digital code into the LTC1446. V_{OUTA} controls the common pin for the analog inputs to the LTC1296 and V_{OUTB} controls the reference span by setting the LTC1296's REF^+ pin. The LTC1296 has a Shutdown pin whose output is a logic low in shutdown mode. During shutdown, this logic low turns off the PNP transistor that supplies power to the LTC1446. The resistors and capacitors lowpass filter the LTC1446 outputs, attenuating noise.

Figure 4 shows how to use an LTC1446 and an LT®1077 to make a wide bipolar output swing 12-bit DAC with a digitally programmable offset. The voltage on DAC A's output (V_{OUTA}) is used as the offset voltage. Figure 4 also shows how the circuit's output voltage changes as a function of the input digital code.

Conclusion

The LTC1446/LTC1446L are the world's only DACs that offer dual 12-bit stand-alone performance in an 8-pin SO or PDIP package. Along with their amazing density, these DACs do not compromise performance, offering excellent 12-bit DNL, rail-to-rail voltage outputs and very low power dissipation. This allows users to save circuit board space without sacrificing performance.

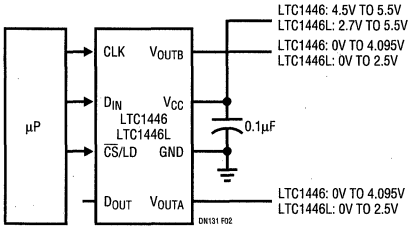


Figure 2. Easy Stand-Alone Application for the LTC1446 or LTC1446L

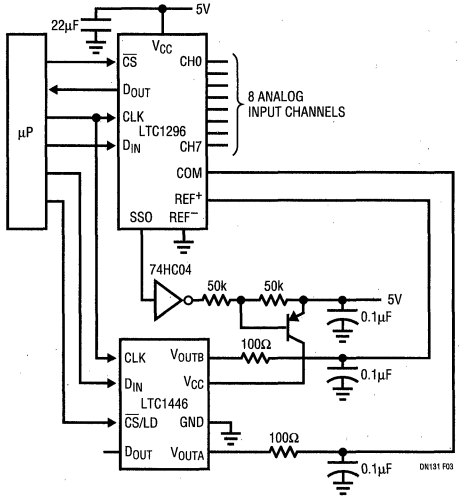


Figure 3. An Autoranging 8-Channel ADC with Shutdown

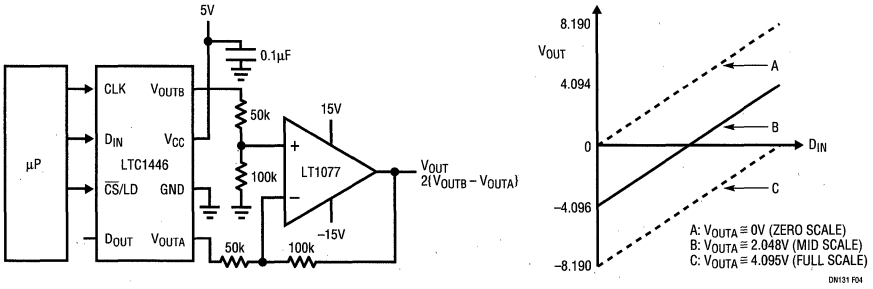


Figure 4. A Wide-Swing, Bipolar Output DAC with Digitally Controlled Offset

For literature on our Digital-to-Analog Converters, call **1-800-4-LINEAR**. For applications help, call (408) 432-1900, Ext. 2525

LINEAR TECHNOLOGY

DESIGN NOTES

Fast Current Feedback Amplifiers Tame Low Impedance Loads – Design Note 132

Sean Gold and William Jett

Introduction

Three current feedback amplifiers (CFAs) now available from Linear Technology can considerably ease the task of driving low impedance loads. This Design Note reviews the capabilities of the LT®1206, LT1207 and LT1210 CFAs and addresses some design issues encountered when using them. These CFAs are fast and capable of delivering high levels of current. They can be readily compensated for reactive loads and are fully protected against thermal and short-circuit faults. Table 1 summarizes their electrical characteristics.

Driving Transformer-Coupled Loads

Transformer coupling is frequently used to step up transmission line signals. Voltage signals amplified in this way are not constrained by local supply voltages, so the amplifier's rated current rather than its voltage swing usually limits the power delivered to the load. Amplifiers with high output current drive are therefore appropriate for transformer-coupled systems.

Figure 1 shows a transformer-coupled application for ADSL in which an LT1210 drives a 100Ω twisted pair. The 1:3 transformer turns ratio allows just over 1W to reach the load at full output. Resistor R_T acts as a primary side back-termination and also prevents large DC currents from flowing in the coil. The overall frequency response is flat to within 1dB from 500Hz to 2MHz. Distortion products at 1MHz are below –70dBc at a total output power of 0.56W (load plus termination), rising to –56dBc at 2.25W. If R_T is removed, the amplifier will see a load of about 11Ω and the maximum output power will increase to 5W. A DC blocking capacitor should be used in this case.

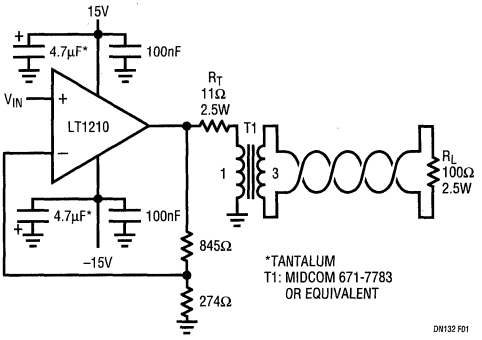


Figure 1. Twisted Pair Driver ADSL. Voltage Gain is About 6; $5V_{P-P}$ Input Corresponds to Full Output

Bridging can be used to increase the output power transferred to a transformer. Differential operation also promotes the cancellation of even-order distortion. Figure 2 shows a differential application using an LT1207 as a bridge driver for HDSL. The dual CFA is configured for a gain of ten,

Table 1. Fast Current Feedback Amplifier Specifications

PART NUMBER	NUMBER OF CFAs	BANDWIDTH (MHz)	RATED OUTPUT CURRENT (A)	SUPPLY RANGE (V)	SLEW RATE (V/µs) (NOTE 1)	THERMAL RESISTANCE θ_{JA} (°C/W) (NOTE 2)	SUPPLY CURRENT (mA)	LOW POWER OP/ SHUTDOWN
LT1206	1	60	0.25	±5 to ±15	I_{LIM}/C_{LOAD} to 900	DD = 25, PDIP = 100. SO = 60, TO-220 = 5	20	Yes
LT1207	2	60	0.25	±5 to ±15	I_{LIM}/C_{LOAD} to 900	SO = 40	2 × 20	Yes
LT1210	1	35	1	±5 to ±15	I_{LIM}/C_{LOAD} to 1000	DD = 25, SO = 40 TO-220 = 5	30	Yes

Note 1: Slew rate depends on circuit configuration and capacitive load.
Note 2: θ_{JA} on SO packages measured with part mounted to a 2.5mm thick FR4 2oz copper PC board with 5000mm² area.

delivering a $10V_{P-P}$ signal to the nominal 35Ω load impedance. The output signal amplitude remains flat over an 8MHz bandwidth.

Driving Capacitive Loads

The devices in Table 1 combine the high output current required to slew large capacitances with appropriate frequency compensation. All of the CFAs described here are C-Load™ amplifiers and are stable with capacitive loads up to 10,000pF.

C-Load is a trademark of Linear Technology Corporation.

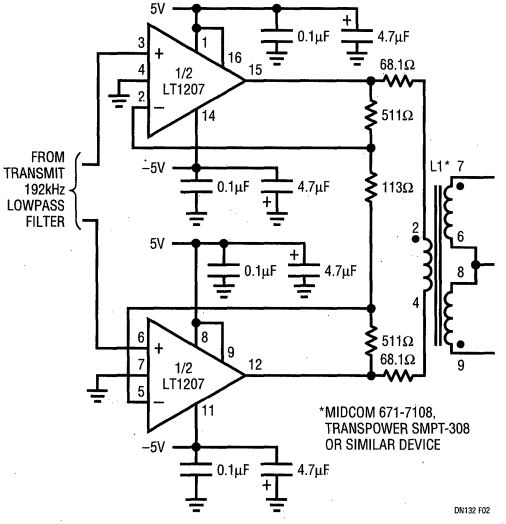


Figure 2. Bridge Driver for HDSL

A good example of a difficult capacitive load is a clock driver for a charge-coupled device (CCD). These devices require precise multiphase clock signals to initiate the transfer of light-generated pixel charge from one charge reservoir to the next. Noise, ringing or overshoot on the clock signal must be avoided. Two problems complicate clock generation. First, CCDs present an input capacitance (typically 100pF to 3300pF) which is directly proportional to the number of sensing elements (pixels). Second, CCDs often require the clock's amplitude to exceed the logic supply. The amplifying filter in Figure 3 addresses these issues. Both CFAs in the LT1207 are configured for a third-order Gaussian lowpass response with 1.6MHz cutoff frequency (one section is shown). This transfer function produces clean clock signals with controlled rise and fall times. Figure 4 shows the LT1207's quadrature outputs driving two 3300pF loads that simulate a CCD image sensor. Ringing and overshoot are notably absent from the clock signals, which have rise and fall times of approximately 300ns.

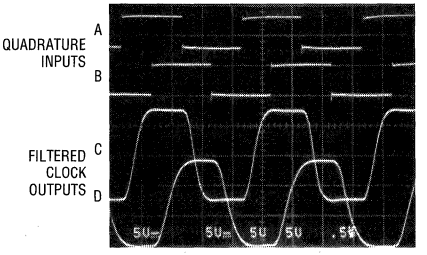


Figure 4. CCD Clock Driver Waveforms

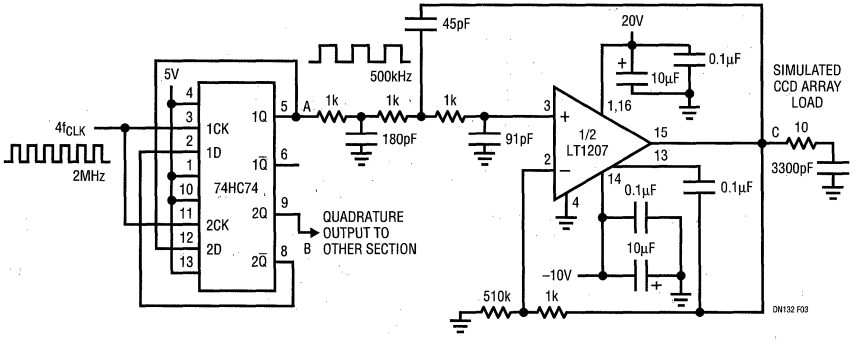


Figure 3. CCD Clock Driver

For literature on our Current Feedback Amplifiers, call **1-800-4-LINEAR**. For applications help, call (408) 432-1900, Ext. 2456

LINEAR TECHNOLOGY

DESIGN NOTES

Low Input Voltage CCFL Power Supply – Design Note 133

Fran Hoffart

Cold cathode fluorescent lamps (CCFLs) are often used to illuminate liquid crystal displays (LCDs). These displays appear in laptop computers, gas pumps, automobiles, test equipment, medical equipment and the like. The lamps themselves are small, relatively efficient and inexpensive, but they must be driven by specialized power supplies. High AC voltage (significantly higher than the operating voltage) is needed to start the lamp. A sinusoidal waveform is desired, the current must be regulated, efficiency should be high and the power supply must be self-protecting in the event of an open-lamp condition.

CCFL power supplies consisting of a Royer class, self-oscillating sine wave converter driven by an LT®1513 switching regulator are shown in Figures 1 and 2. These circuits are especially suited for low voltage operation, with guaranteed operation for input voltages as low as 2.7V and as high as 20V. High voltage output regulated Royer converters, although capable of 90% efficiency, are not well-suited for low input voltage operation and have difficulty operating with input voltages below 5V. The circuits shown here overcome this limitation while providing efficiency exceeding 70%.

The LT1513 is a 500kHz current mode switching regulator featuring an internal 3A switch and unique feedback circuitry. In addition to the Voltage Feedback pin (V_{FB}), a second feedback node (I_{FB}) provides a simple means of controlling output current in a flyback or SEPIC (single-ended primary inductance converter) topology.

Two CCFL driver circuits are shown. The first (Figure 1) drives one end of the lamp, with the other end effectively grounded. Lamp current is directly sensed at the low side of the lamp, half-wave rectified by D4, and then used to develop a feedback voltage across R2. This voltage, filtered by R3 and C6, drives the V_{FB} pin (2) to complete the feedback loop. The RMS lamp current is tightly regulated and is equal to 2.82V/R2.

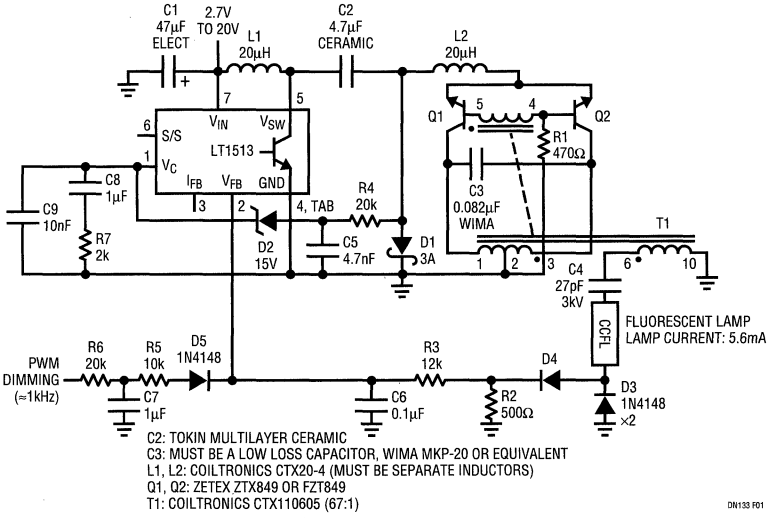


Figure 1. CCFL Power Supply for Grounded Lamp Configuration Operates on 2.7V

Because of the high voltage 60kHz lamp drive used by the CCFL lamps, any stray capacitance from the lamp and lamp leads to ground will result in unwanted parasitic current flow, thus lowering efficiency. The lamp and display housing often have relatively high stray capacitance, which can dramatically lower the overall circuit efficiency.

In some displays that exhibit high capacitance, a floating lamp drive can provide much higher overall efficiency. The operation of the floating lamp circuit shown in Figure 2 is similar to that of the grounded lamp, except for the transformer secondary and the feedback method used. In this circuit, the lamp current is controlled by sensing and regulating the Royer input current. This current is sensed by R2, filtered by R3 and C6 and fed into the I_{FB} pin (3) of the LT1513, thus completing the feedback loop. The sense voltage required at the I_{FB} pin is –100mV. Because the Royer input current rather than the actual lamp current is regulated, the regulation of Figure 2 is not as tight as that of Figure 1.

There are three considerations to keep in mind when laying out a PC board for these supplies. The first is related to high frequency switcher characteristics. The 500kHz switching frequency allows very small surface mount components to be used, but it also requires that PC board traces be kept short (especially the input capacitor, Schottky diode and LT1513 ground connections). The second item is the high voltage section, which includes T1's secondary, the ballasting capacitor C3 and the lamp wiring. Lamp starting voltages can easily exceed 1000V, which can cause a poorly designed board to arc, resulting in catastrophic failure. Board leakages can also increase dramatically with time, resulting in destructive field failures. Third, surface mount components rely on the PC board copper to conduct the heat away from the components and dissipate it to the surrounding air. Good thermal PC board layout practices are necessary.

In both circuits, lamp current can be adjusted downward to provide lamp dimming. A 5V pulse width modulated (PWM) 1kHz signal or an adjustable DC voltage can provide a full range of dimming. In Figure 1, 100% duty cycle represents minimum lamp brightness, whereas in Figure 2, 100% duty cycle is maximum lamp brightness.

The lamp drive is a constant current, and without protection circuitry, voltages could become very high in the event of an open-lamp connection, causing transformer arcing or LT1513 failures. Open-lamp or high input voltage fault protection is provided by R4, C5 and the 15V Zener D2, which limit the maximum voltage available for the Royer converter.

See Application Notes 49 and 65, Design Note 99 and the LT1513 Data Sheet for additional information on driving CCFL lamps.

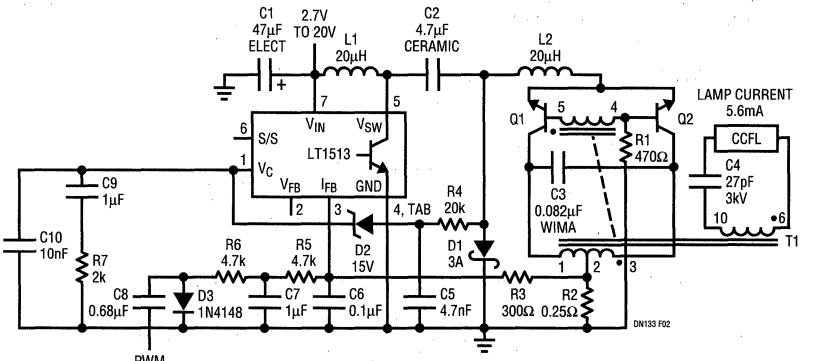


Figure 2. CCFL Power Supply for Floating Lamp Configuration Operates on 2.7V

For literature on our Switching Regulators, call **1-800-4-LINEAR**. For applications help, call (408) 432-1900, Ext. 2361

LINEAR TECHNOLOGY

DESIGN NOTES

Telephone Ring-Tone Generation – Design Note 134

Dale Eagar

Requirements

When your telephone rings, exactly what is the phone company doing? This question comes up frequently, as it seems everyone is becoming a telephone company. Deregulation opens many new opportunities, but if you want to be the phone company your have to ring bells.

An Open-Architecture Ring-Tone Generator

Here is a design that you can own, tailor to your specific needs, layout on your circuit board and put on your bill of materials. Finally, you will be in control of the black magic (and high voltages) of ring-tone generation.

Not Your Standard Bench Supply

Ring-tone generation requires not one but two high voltages, 60VDC and –180VDC (this arises from the need to put $87V_{RMS}$ on –48VDC). Figure 1 details the switching power supply that delivers the volts needed to run the ring-tone circuit. This switcher can be powered from any voltage from 5V to 30V and shuts down when not in use. Figure 2 is the build diagram of the transformer used in the switching power supply.

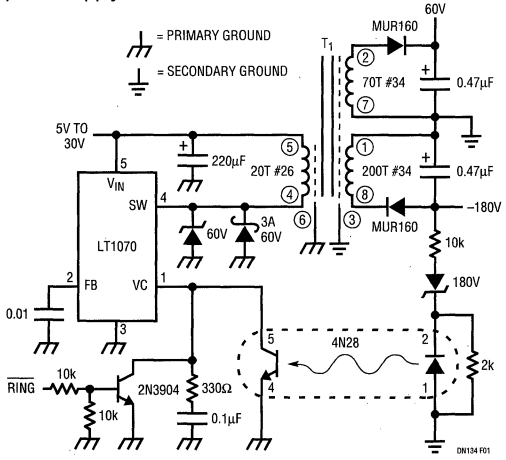


Figure 1. The Switching Power Supply

Quad Op Amp Rings Phones

When a phone rings, it rings with a cadence, a sequence of rings and pauses. The standard cadence is one second ringing followed by two seconds of silence. We use the first 1/4 of LT®1491 as a cadence oscillator, whose output is at V_{CC} for one second and then at V_{EE} for two seconds. This sequence repeats every three seconds, producing the all-too-familiar pattern. The actual ringing of the bell is done by a 20Hz AC sine wave signal at a signal level of $87V_{RMS}$ superimposed on –48VDC. The 20Hz signal is implemented with the second amplifier in the LT1491 which acts as a gated 20Hz oscillator (see Figure 3).

The third amplifier in the LT1491, which is configured as a lowpass filter, converts the square wave output of the oscillator to a sine wave by filtering out unwanted harmonics. Finally, the $87V_{RMS}$ and the –48VDC parts are handled by the fourth amplifier in the LT1491 and its steering of two external 15V regulators.

MATERIALS	
2	EFD 20-15-3F8 Cores
1	EFD 20-15-8P Bobbin
2	EFD 20- Clip
2	0.007" Nomex Tape for Gap
Winding 1	Start Pin 1 200T #34
	Term Pin 8
	1 Wrap 0.002" Mylar Tape
Winding 2	Start Pin 2 70T #34
	Term Pin 7
	1 Wrap 0.002" Mylar Tape
Shields	Connect Pin 3 1T Foil Tape Faraday Shield
	1 Wrap 0.002" Mylar Tape
	Connect Pin 6 1T Foil Tape Faraday Shield
	1 Wrap 0.002" Mylar Tape
Winding 3	Start Pin 4 20T #26
	Term Pin 5
	Finish with Mylar Tape

Figure 2. Ring-Tone High Voltage Transformer Build Diagram

The rest of what we do, the part that is most difficult to follow, involves the output amplifier. In the output amplifier, the $6V_{P-P}$ signal from the waveform synthesizer is imposed across R12 (see Figure 4) into a virtual ground, creating a sine wave signal current. This current is added to the DC current flowing through R15 and the resulting current is imposed across R13. This stage amplifies the sine wave and offsets it to become an $87V_{RMS}$ sine wave imposed on a −48VDC bias. The trick here is that the voltage gain is in the ±15V regulators, not the LT1491 which is merely steering currents.

This complete circuit (Figure 4) includes the ring-trip sense circuit to detect when the phone receiver is picked up. This circuit is fully protected for output shorts to any voltage within the power supply window of −180V to 60V.

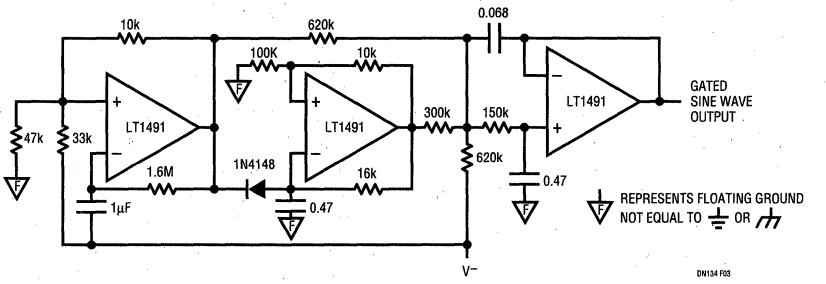


Figure 3. Wave Form Synthesizer

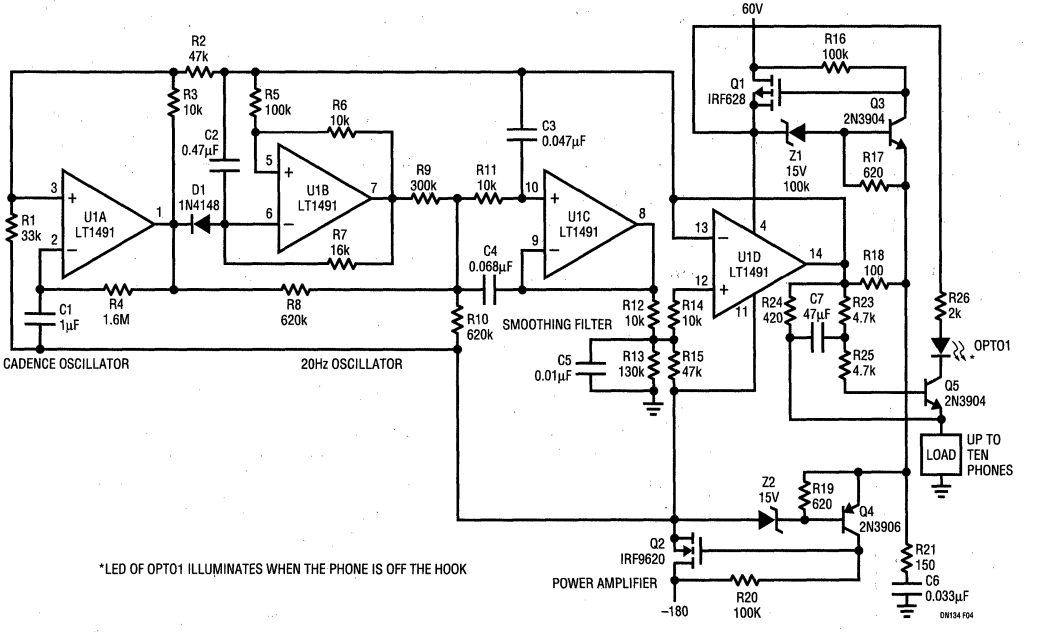


Figure 4. Complete Ring-Tone Generator Circuit

For literature on our Operational Amplifiers, call **1-800-4-LINEAR**. For applications help, call (408) 432-1900, Ext. 2593

DESIGN NOTES

Efficient Processor Power System Needs No Heat Sink

Design Note 135

John Seago

New designs require more functionality in an ever decreasing package size. Compact, efficient high frequency power supplies are required and there is seldom room for a heat sink. Portable computers have some of the most demanding requirements. Powering the Pentium® processor adds additional challenges for the power system designer.

New IC Powers Portable Pentium Processor and Much More

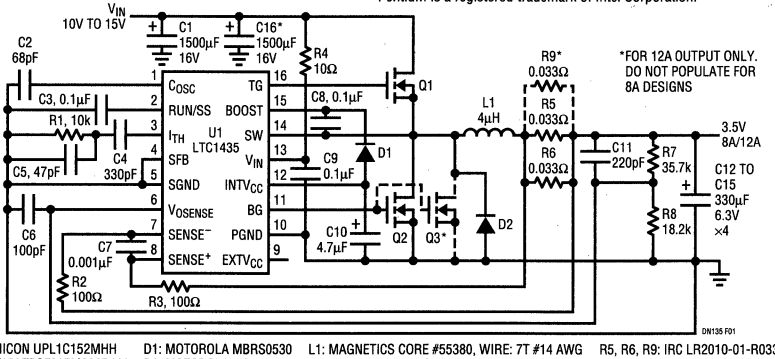
The LTC®1435 is a current mode, constant frequency, synchronous step-down switching regulator that uses external N-channel MOSFETs for very high efficiency. With the wide input voltage range of 3.5V to 36V and low dropout (99% duty cycle) capability, the LTC1435 is a good choice for battery-powered circuits where the voltage of four NiCd cells can drop to 3.6V at the end of discharge. The ability to operate with 36V inputs allows application of a wide range of AC adapter voltages. The LTC1435 achieves battery-powered efficiencies of 90% to 95% and features Burst Mode™ operation for longest battery life under light load conditions. For constant frequency at all load conditions, the Burst Mode operation can be defeated easily on the LTC1435. The Adaptive Power™ mode, available on the LTC1436, provides constant frequency at light loads with greatly improved efficiency. With a "silver box" power supply or other high current voltage source, the LTC1435 can easily provide an output current of 12A.

The LTC1435's current mode architecture and 1% voltage reference provide a tightly controlled output voltage with excellent load and line regulation and outstanding set-point accuracy. The switching frequency can be selected between 50kHz and 400kHz, so total circuit cost, efficiency, component size and transient response can be properly balanced. The LTC1435 also features both logic-level on/off control and output current soft start. When the controller is in the shutdown mode, voltage is removed from the load and quiescent input current drops to a mere 15µA. The LTC1435 is available in the popular 16-pin SO and SSOP packages.

High Performance Pentium Processor Power

The 150MHz Pentium load current changes from 0.2A to 4.5A in about 15ns. The core voltage must be maintained at 3.5V ±0.1V under all conditions.

The LTC1435 circuit shown in Figure 1 was used to power an Intel Power Validator to simulate the typical Pentium



C1, C16: NICHICON UPL1C152MHH
C12 TO C15: AVX TPSE337M006R100
D1: MOTOROLA MBRS0530
D2: MOTOROLA MBRD835L
L1: MAGNETICS CORE #55380, WIRE: 7T #14 AWG
Q1TO Q3: SILICONIX SI4410DY
R5, R6, R9: IRC LR2010-01-R033-F
U1: LINEAR TECHNOLOGY LTC1435CS

Figure 1. 12V to 3.5V Regulator for 8A or 12A Applications

processor load transient of 0.2A to 4.5A. The transient waveform in Figure 2 shows a ±0.04V variation in output voltage with 700µF of local decoupling capacitance at the Power Validator and the 1300µF capacitance at the regulator output. The same base circuit was used to power both 8A and 12A static loads. By changing the value of R8, the output voltage can be set from 1.8V to 5V at a full 12A. Outputs of up to 9V are possible with some minor changes.

Portable Pentium Processor Power

The portable Pentium processor requires a core voltage of 2.9V ±0.165V and switches between 0.25A and 2.65A in about 30ns. This load was simulated by the Power Validator and powered by the circuit of Figure 3. Although this circuit works very well over the input voltage range of 5.5V to 28V, it will continue to provide portable Pentium processor core voltage down to a 3.5V input by adding C13 and C14.

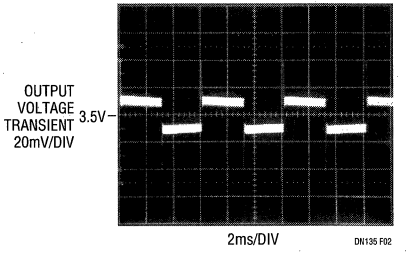


Figure 2. High Performance Pentium Processor Load Transient Waveform

Figure 4 shows the output voltage transient and load current waveforms with an input voltage of 3.5V. Figure 5 shows circuit efficiency over load and line conditions.

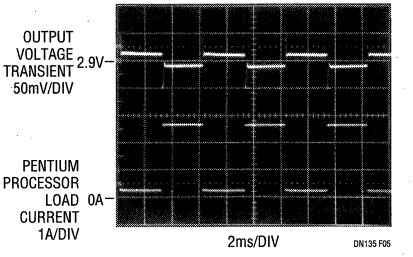


Figure 4. Portable Pentium Processor Load Transient Waveform

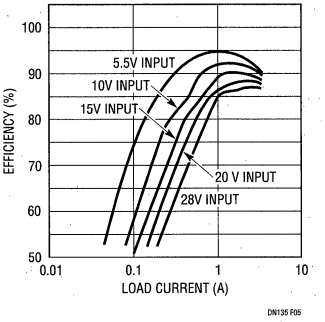
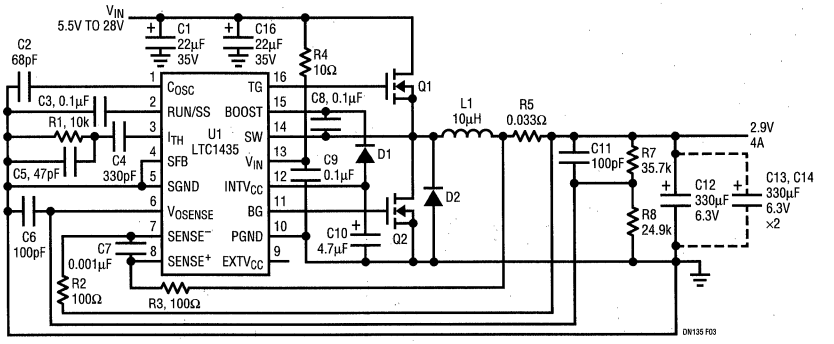


Figure 5. LTC1435 Efficiency Curves for Different Input Voltages



C1, C16: AVX TPSE226M035R300
C12 TO C14: AVX TPSE337M006R100
D1: MOTOROLA MBRS0530
D2: MOTOROLA MBRS140T3
L1: SUMIDA CDRH125-10
Q1, Q2: SILICONIX Si4412DY
R5: IRC LR2010-01-R033-F
U1: LINEAR TECHNOLOGY LTC1435CS

Figure 3. 2.9V Regulator for Portable Pentium Processor

For literature on our Switching Regulators, call **1-800-4-LINEAR**. For applications help, call (408) 432-1900, Ext. 2361

DESIGN NOTES

LT1462/LT1463/LT1464/LT1465: Micropower Dual and Quad JFET Op Amps Feature pA Input Bias Currents and C-Load™ Drive Capability – Design Note 136

Alexander Strong and Kevin R. Hoskins

Introduction

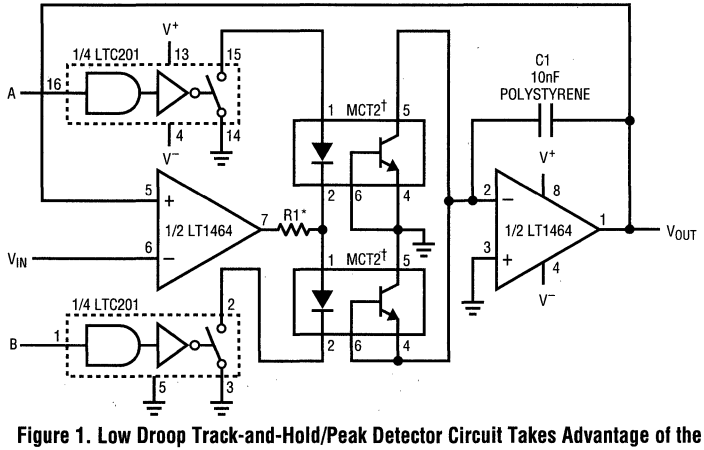
The LT®1462/LT1464 duals and the LT1463/LT1465 quads are the first micropower op amps to offer picoampere input bias currents and unity-gain stability when driving capacitive loads. For each amplifier, the LT1462/LT1463 consume only 28µA of supply current; the faster LT1464/LT1465, just 145µA. Low supply current and operation specified at ±5V supplies make these amplifiers appropriate for portable low power applications. The LT1462/3/4/5 family is especially suited for piezo transducer conditioning, strain gauge weight scales, very low droop track-and-holds, wide dynamic range photodiode amplifiers and other applications that benefit from pA input bias current. The LT1462/3/4/5 family also exhibits very low noise current, important to circuits such as low frequency filters. These op amps allow high value resistors to be used with easily obtainable, low value precision capacitors to set a filter's frequency characteristics without compromising noise performance.

Driving Large Capacitive Loads

Though the LT1462/3/4/5 consume very small amounts of supply current, they can easily drive 10nF loads while remaining stable. Instead of increasing their idling current to drive heavy load capacitance, these op amps use a clever compensation technique to lower bandwidth. As load capacitance increases, these op amps automatically reduce their bandwidth by reflecting a portion of the load capacitance back to the gain node, increasing the compensation capacitance. Now instead of a 1MHz op amp trying to drive a large capacitor, a lower bandwidth op amp is able to drive the load capacitance.

Applications

A benefit of the LT1464/LT1465's low power consumption is very low junction leakage current, which in turn, keeps the input bias current below 500fA typically. Track-and-hold applications are a natural for this family of op amps.



FUNCTION	MODE	IN A	IN B
Track-and-Hold	Track	0	0
	Hold	1	1
Positive Peak Det	Reset	0	0
	Store	0	1
Negative Peak Det	Reset	0	0
	Store	1	0

LTC®201 switch is open for logic "1"

TYPICAL DROOP = $\frac{0.5pA}{10nF}$ = 0.05mV/s

TOTAL SUPPLY CURRENT = 460µA MAX

* R1 = 600Ω FOR ±15V SUPPLIES
R1 = 0Ω FOR ±5V SUPPLIES

† MOTOROLA (602) 244-5768

DN136 F01

Figure 1. Low Droop Track-and-Hold/Peak Detector Circuit Takes Advantage of the LT1464s 0.5pA Input Bias Current

Figure 1 is a track-and-hold circuit that uses a low cost optocoupler as a switch. Leakage for these parts is usually in the nA region with 1V to 5V across the output. Since there is less than 0.8mV across the junctions, the leakage is so small that the op amp's I_B dominates. The input signal is buffered by one op amp while the other buffers the stored voltage; this results in a droop of 50μV/s with a 10nF capacitor.

The LT1462/LT1463s low input bias current make it a natural for amplifying low level signals from high impedance transducers. The 1pA input bias current contributes only 0.4fA/√Hz of current noise or 0.4nV/√Hz voltage noise with a 1MΩ source impedance. A 1MΩ impedance's thermal noise of 130nV/√Hz dominates the op amp's noise, showing that even with high source impedances, the LT1462/LT1463 contribute very little to total input-referred noise. Taking advantage of these features, Figure 2's photodiode logging amplifier uses two LT1462 duals or an LT1463 quad. Here, the photodiode current is converted to a voltage by the first op amp and D1 and amplified by the first, second and third logarithmic compression amplifiers.

A DC feedback path comprising R8, R9, C6 and Q1 is active only for no light conditions. Q1 is off when light is present, isolating the photodiode from C6. When feedback is needed, a small filtered current through R8 prevents the op amp outputs from saturating when no signal is present.

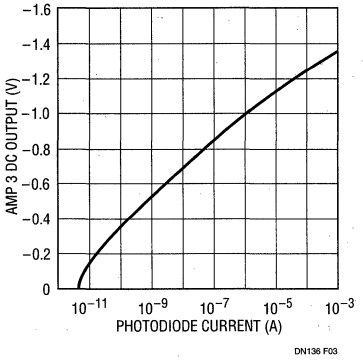


Figure 3. Logging Photodiode Amplifier DC Output

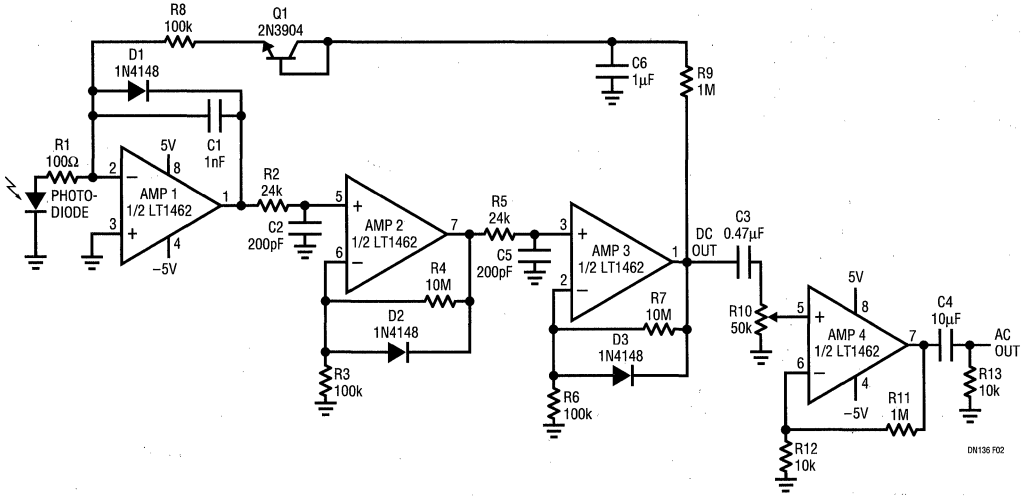


Figure 2. This Logging Photodiode Amplifier Takes Advantage of the LT1462s 1pA Input Bias Current to Amplify the Low Level Signal from The Photodiode's High Source Impedance

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LINEAR TECHNOLOGY

DESIGN NOTES

New Comparators Feature Micropower Operation Under All Conditions – Design Note 137

Jim Williams

Some micropower comparators have operating modes that allow excessive current drain. In particular, poorly designed devices can conduct large transient currents during switching. Such behavior causes dramatically increased power drain with rising frequency, or when the inputs are nearly balanced, as in battery monitoring applications.

Figure 1 shows a popular micropower comparator's current consumption during switching. Trace A is the input pulse, trace B is the output response and trace C is the supply current. The device, specified for micropower level supply drain, pulls 40mA during switching. This undesirable surprise can upset a design's power budget or interfere with associated circuitry's operation.

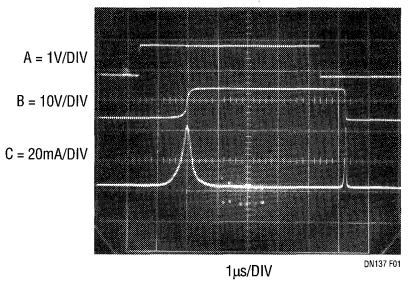

Figure 1. Poorly Designed "Micropower" Comparator Pulls Huge Currents During Transitions. Result Is Excessive Current Consumption with Frequency

The LTC®1440 series comparators are true micropower devices. They eliminate current peaking during switching, resulting in greatly reduced power consumption versus frequency, or when the inputs are nearly balanced. Figure 2's plot contrasts the LTC1440's power consumption versus frequency with that of another comparator specified as a micropower component. The LTC1440 has about 200 times lower current consumption at higher frequencies, while maintaining a significant advantage below 1kHz.

Table 1 shows some LTC1440 family characteristics. A voltage reference and programmable hysteresis are included in some versions, with 5µs response time for all devices.

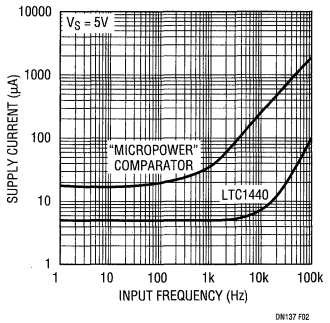

Figure 2. The LTC1440 Family Draws 200 Times Lower Current at Frequency Then Another Comparator

Table 1. Some Characteristics of the LTC1440 Family of Micropower Comparators

PART NUMBER	NUMBER OF COMPARATORS	REFERENCE	PROGRAMMABLE HYSTERESIS	PACKAGE	PROP. DELAY (100mV OVERDRIVE)	SUPPLY RANGE	SUPPLY CURRENT
LTC1440	1	1.182V	Yes	8-Lead PDIP, SO	5µs	2V to 11V	4.7µA
LTC1441	2	No	No	8-Lead PDIP, SO	5µs	2V to 11V	5.7µA
LTC1442	2	1.182V	Yes	8-Lead PDIP, SO	5µs	2V to 11V	5.7µA
LTC1443	4	1.182V	No	16-Lead PDIP, SO	5µs	2V to 11V	8.5µA
LTC1444	4	1.221V	Yes	16-Lead PDIP, SO	5µs	2V to 11V	8.5µA
LTC1445	4	1.221V	Yes	16-Lead PDIP, SO	5µs	2V to 11V	8.5µA

The new devices permit high performance circuitry with low power drain. Figure 3's quartz oscillator, using a standard 32.768kHz crystal, starts under all conditions with no spurious modes. Current drain is only 9μA at a 2V supply.

Figure 4's voltage-to-frequency converter takes full advantage of the LTC1441's low power consumption under dynamic conditions. A 0V to 5V input produces a 0Hz to 10kHz output, with 0.02% linearity, 60ppm/°C drift and 40ppm/V supply rejection. Maximum current consumption is only 26μA, 100 times lower than currently available circuits. C1 switches a charge pump, comprising Q5, Q6 and the 100pF capacitor, to maintain its negative input at 0V. The LT1004s and associated components form a temperature-compensated reference for the charge pump. The 100pF capacitor charges to a fixed voltage; hence, the repetition rate is the circuit's only degree of freedom to maintain feedback. Comparator C1 pumps uniform packets of charge to its negative input at a repetition rate precisely proportional to the input voltage derived current. This action ensures that circuit output frequency is strictly and solely determined by the input voltage.

Start-up or input overdrive can cause the circuit's AC-coupled feedback to latch. If this occurs, C1's output goes low; C2, detecting this via the 2.7M/0.1μF lag, goes high. This lifts C1's positive input and grounds the negative input with Q7, initiating normal circuit action.

Figure 5 shows the circuit's power consumption versus frequency. Zero frequency current is just 15μA, increasing to only 26μA at 10kHz.

A detailed description of this circuit's operation appears in the August 1996 issue of *Linear Technology* magazine.

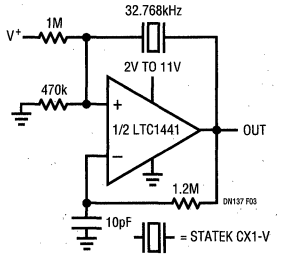

Figure 3. 32.768kHz "Watch Crystal" Oscillator Has No Spurious Modes. Circuit Pulls 9μA at V_S = 2V

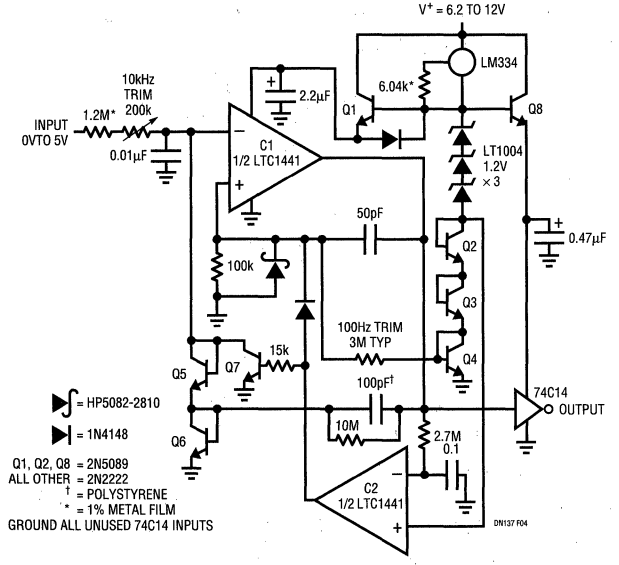

Figure 4. LTC1441-Based 0.02% V/F Converter Requires Only 26μA Supply Current

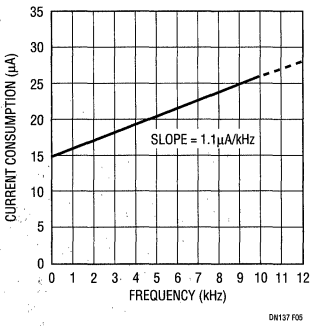

Figure 5. Current Consumption vs Frequency for the V-to-F Converter. Discharge Cycles Dominate 1.1μA/kHz Current Drain Increase

For literature on our Micropower Comparators, call **1-800-4-LINEAR**. For applications help, call (408) 432-1900, Ext. 2456

LINEAR TECHNOLOGY

DESIGN NOTES

Micropower ADC and DAC in SO-8 Give PCs a 12-Bit Analog Interface – Design Note 138

Kevin R. Hoskins

Introduction

Adding two channels of analog input/output to a PC computer is simple, inexpensive, low powered and compact when using the LTC®1298 ADC and LTC1446 DAC. The LTC1298 and the LTC1446 are the first SO-8 packaged 2-channel devices of their kind. While the application shown is for PC data acquisition, the two converters provide the smallest, lowest power solutions for many other analog I/O applications.

Small, Micropower ADC and DAC

The LTC1298 features a 12-bit ADC, 2-channel multiplexer, and an input S/H. Operating on a 5V supply at maximum conversion rate, the LTC1298 draws just 340µA. A built-in auto shutdown further reduces power dissipation at reduced sampling rates (to 30µA at 1ksps). The serial interface allows remote operation.

The LTC1446 is the first 12-bit dual micropower SO-8 packaged DAC. It features a 1mV/LSB (0V to 4.095V) rail-to-rail output, internal 2.048V reference and a simple, cost-effective, 3-wire serial interface. A D_{OUT} pin allows cascading multiple LTC1446s without increasing the number of serial interconnections. Operating on a supply of 5V, the LTC1446 draws just 1mA (typ).

PC 2-Channel Analog I/O Interface

The circuit shown in Figure 1 connects to a PC's serial interface using four interface lines: DTR, RTS, CTS and TX. DTR is used to transmit the serial clock signal, RTS is used to transfer data to the DAC and ADC, CTS is used to receive conversion results from the LTC1298, and the signal on TX selects either the LTC1446 or the LTC1298 to receive input data. The LTC1298's and LTC1446's low power dissipation allow the circuit to be powered from the serial port. The TX and RTS lines charge capacitor C4 through diodes D5 and D6. An LT®1021-5 regulates the voltage to 5V. Returning the TX and RTS lines to a logic high after sending data to the DAC or completion of an ADC conversion provides constant power to the LT1021-5.

Using a 486-33 PC, the throughput was 3.3ksps for the LTC1298 and 2.2ksps for the LTC1446. Your mileage may vary.

Listing 1 is C code that prompts the user to either read a conversion result from the ADC's CH0 or write a data word to both DAC channels.

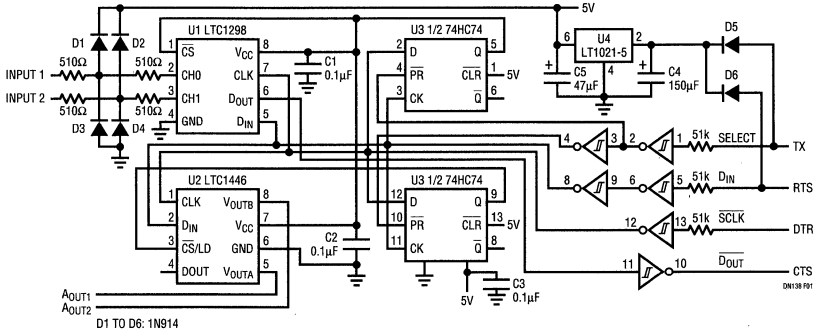

Figure 1. Communicating Over the Serial Port, the LTC1298 and LTC1446 in SO-8 Create a Simple, Low Power 2-Channel Analog Interface for PCs

Conclusion

These SO-8 packaged data converters offer unprecedented space, power and economy to data acquisition system designers. They form a very nice 12-bit analog interface to a wide variety of portable, battery-powered and size constrained products. They are extremely easy to apply and require a minimum of passive support components and interconnections.

Listing 1. Configure Analog Interface with this C Code

```
#define port 0x3FC/* Control register, RS232 */
#define inprt 0x3FE/* Status  reg.  RS232 */
#define LCR  0x3FB/* Line Control Register */
#define high 1
#define low  0
#define Clock 0x01/* pin 4, DTR */
#define Din 0x02/* pin 7, RTS */
#define Dout 0x10/* pin 8, CTS input */
#include<stdio.h>
#include<dos.h>
#include<conio.h>
/* Function module sets bit to high or low */
void set_control(int Port,char bitnum,int flag)
{
        char temp;
        temp = inportb(Port);
        if (flag==high)
    temp |= bitnum; /* set output bit to high */
    else
       temp &= ~bitnum; /* set output bit to low */
        outportb(Port,temp);
}
/* This function brings CS high or low (consult the
schematic) */
void CS_Control(direction)
{
        if (direction)
{
    set_control(port,Clock,low);/* set clock high for Din to
be read */
set_control(port,Din,low); /* set Din low */
set_control(port,Din,low);/* set Din high to make CS goes
high */
    }
    else {
        outportb(port, 0x01);/* set Din & clock low */
        Delay(10);
        outportb(port, 0x03);/* Din goes high to make CS
goes low */
    }
}
/* This function outputs a 24 bit(2x12) digital code to
LTC1446L */
void Din_(long code,int clock)
{
    int x;
    for(x = 0; x<clock; ++x)
    {
        code  <<= 1;/* align the Din bit */
        if (code & 0x1000000)
        {
    set_control(port,Clock,high);\/* set Clock low */
    set_control(port,Din,high);/* set Din bit high */
        }
        else  {
         set_control(port,Clock,high); /* set Clock low  */
         set_control(port,Din,low);/* set Din low */
            }
        set_control(port,Clock,low);/* set Clock high for
DAC to latch */
    }
}
/* Read bit from ADC to PC */
Dout_()
{
    int temp, x, volt =0;
    for(x = 0; x<13; ++x)
 {
        set_control(port,Clock,high);
        set_control(port,Clock,low);
        temp = inportb(inprt);/* read status reg. */
        volt <<= 1;/* shift left one bit for serial
transmission */
        if(temp & Dout)
        volt += 1;    /* add 1 if input bit is high */
 }
    return(volt & 0xfff);
}
/* menu for the mode selection */
char menu()
{
    printf("Please select one of the following:\na: ADC\nd:
DAC\nq: quit\n\n");
    return (getchar());
}
void main()
{
    long code;
    char  mode_select;
    int  temp,volt=0;
/* Chip select for DAC & ADC is controlled by RS232 pin
3 TX line.  When LCR's bit 6 is set, the DAC is selected
and the reverse is true for the ADC. */
    outportb(LCR,0x0);/* initialize DAC */
    outportb(LCR,0x64);/* initialize ADC */
    while((mode_select = menu()) != 'q')
 {
   switch(mode_select)
    {
      case 'a':
      {
            outportb(LCR,0x0);/* selecting ADC */
            CS_Control(low);/* enabling the ADC CS */
            Din_(0x680000, 0x5);/* channel selection */
            volt = Dout_();
            outportb(LCR,0x64);/* bring CS high */
            set_control(port,Din,high);/* bring Din signal
high */
            printf("\ncode: %d\n",volt);
            }
       break;
    case 'd':
    {
  printf("Enter DAC input code (0 - 4095):\n");
  scanf("%d", &temp);
  code = temp;
  code += (long)temp << 12;/*  converting 12 bit to 24 bit
word */
  outportb(LCR,0x64);/* selecting DAC */
  CS_Control(low);/* CS enable */
  Din_(code,24);/* loading digital data to DAC */
      outportb(LCR,0x0);/* bring CS high */
      outportb(LCR,0x64);/* disabling ADC */
      set_control(port,Din,high);/* bring Din signal high */
      }
       break;
    }
 }
}
```

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LINEAR TECHNOLOGY

DESIGN NOTES

Safe Hot Swapping Using the LTC1421 – Design Note 139

James Herr and Robert Reay

When a circuit board is inserted into a live backplane, the large bypass capacitors on the board can draw huge inrush currents from the backplane power bus as they charge. The inrush current, on the order of 10A to 100A, can destroy the board's bypass capacitors, metal traces or connector pins. The inrush current can also cause a glitch on the backplane power bus, which could force all of the other boards in the system to reset. In addition, the system data bus can be disrupted when the board's data pins make or break contact.

The LTC®1421 can turn on two positive and one negative board supply voltage at a programmable rate, allowing a board to be safely inserted in, or removed from, a live backplane. The chip provides internal charge pumps for driving the gates of external N-channel pass transistors, board connection sensing, flexible supply voltage monitoring, power on reset output, short-circuit protection and soft or hard reset via software control.

Typical Application

Figure 1 shows a typical application using the LTC1421.

The LTC1421 works best with a staggered, 3-level connector. Ground makes connection first to discharge any static build-up. V_{CC}, V_{DD} and V_{EE} make connection second and the data bus and all other pins last. The connection sense pins $\overline{CON1}$ and $\overline{CON2}$ are located on opposite ends of the connector to allow the board to be rocked back and forth during insertion.

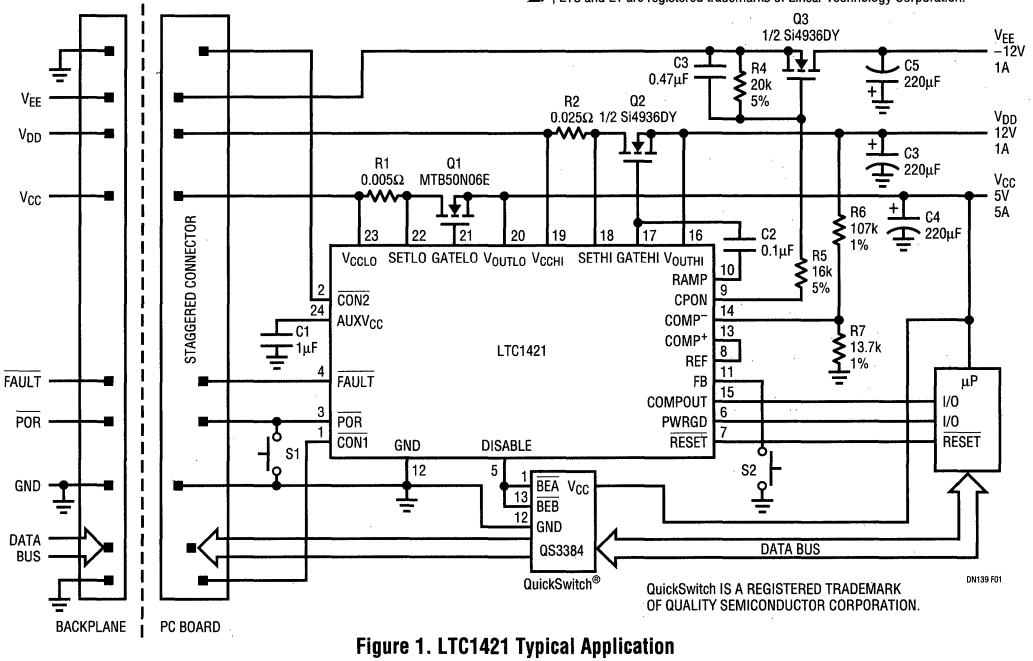

Figure 1. LTC1421 Typical Application

The power supplies on the board are controlled by placing external N-channel pass transistors Q1, Q2 and Q3 in the power path for V_{CC}, V_{DD} and V_{EE}, where V_{CC} and V_{DD} can range from 3V to 12V, and V_{EE} from –5V to –48V. By ramping up the voltage on the pass transistors' gates at a controlled rate, the transient surge current [I = (C)(dv/dt)] drawn from the main backplane supply will be limited to a safe value. The ramp rate is set by the value of capacitor C2.

The board's data bus is buffered by a QS3384 QuickSwitch from Quality Semiconductor. Disabling the QuickSwitch via the DISABLE pin during board insertion and removal prevents corruption of the system data bus.

Resistors R1 and R2 form an electronic circuit breaker function that protects against excessive supply current. When the voltage across the sense resistor is greater than 50mV for more than 20µs, the circuit breaker trips, immediately turning off Q1 and Q2 while the $\overline{FAULT}$ pin is pulled low. The chip will remain in the tripped state until the $\overline{POR}$ pin is pulsed low or the power on V_{CCLO} and V_{CCHI} is cycled. The circuit breaker can be defeated by shorting V_{CCLO} to SETLO and V_{CCHI} to SETHI.

The $\overline{RESET}$ signal is used to reset the system microcontroller. When the voltage on the V_{OUTLO} pin rises above the reset threshold, PWRGD immediately goes high and $\overline{RESET}$ goes high 200ms later. When the V_{OUTLO} supply voltage drops below the reset threshold, PWRGD immediately goes low, and $\overline{RESET}$ goes low 60µs later, allowing the PWRGD signal to be used as an early warning that a reset is about to occur. When the FB is left floating, the reset threshold is 4.65V; when the FB pin is tied to V_{OUTLO}, the reset threshold is 2.90V.

The uncommitted comparator and internal voltage reference, along with resistors R6 and R7, are used to monitor the 12V supply. When the supply drops below 10.8V, the COMPOUT pin will go low. The comparator can be used to monitor any voltage in the system.

Push-button switches S1 and S2 are used to generate a hard and soft reset, respectively. A hard or soft reset may also be initiated by a logic signal from the backplane. Pushing S1 shorts the $\overline{POR}$ pin to ground, generating a hard reset that cycles the board's power. Pass transistors Q1 to Q3 are turned off and V_{OUTLO} and V_{OUTHI} are actively pulled to ground. When V_{OUTLO} discharges to within 100mV of ground, the LTC1421 is reset and a normal power-up sequence is started.

Pushing S2 shorts the FB pin to ground, generating a soft reset that doesn't cycle the board's power. PWRGD immediately goes low, followed 64µs later by $\overline{RESET}$. When S2 is released, PWRGD immediately goes high, followed 200ms later by $\overline{RESET}$.

Board Insertion Timing

When the board is inserted, GND pin makes contact first, followed by V_{CCHI} and V_{CCLO} (Figure 2, time point 1). DISABLE is immediately pulled high, so the data bus switch is disabled. At the same time CON1 and CON2 make contact and are shorted to ground on the host side (time point 3). When CON1 and CON2 are both forced to ground for more than 20ms, the LTC1421 assumes that the board is fully connected to the host and power-up can begin. When V_{CCLO} and V_{CCHI} exceed the 2.45V undervoltage lockout threshold, the 20µA current reference is connected from RAMP to GND, the charge pumps are turned on and CPON is forced high (time point 4). V_{OUTHI} and V_{OUTLO} begin to ramp up. When V_{OUTLO} exceeds the reset threshold voltage, PWRGD will immediately be forced high (time point 5). After a 200ms delay, RESET will be pulled high and DISABLE will be pulled low, enabling the data bus (time point 6).

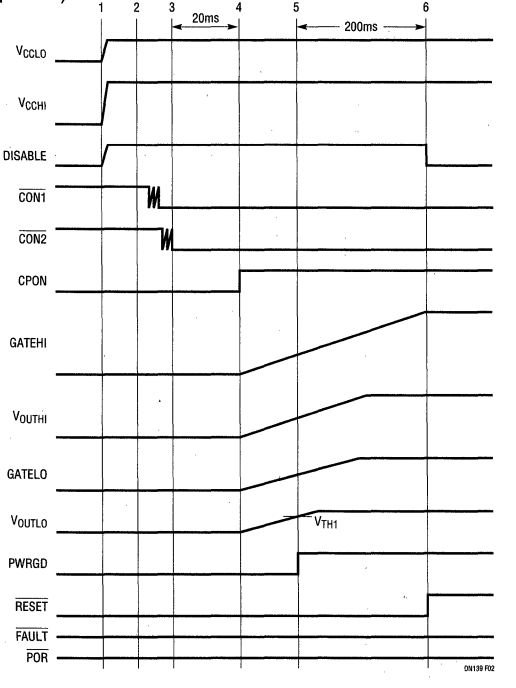

Figure 2. Board Insertion Timing

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LINEAR TECHNOLOGY

DESIGN NOTES

Updated Operational Amplifier Selection Guide for Optimum Noise Performance – Design Note 140

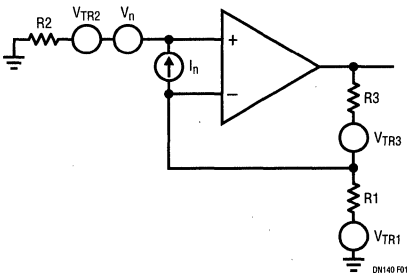
Frank Cox

Eight years ago, George Erdi wrote a very useful Design Note (DN6) that presented information to aid in the selection of op amps for optimum noise performance, in both graphical and tabular form. Design Note 140 is an update of DN6. It covers new low noise op amps as well as some high speed op amps. Although a great deal has changed in eight years, especially in electronics, noise is still a critical issue in op amp circuit design and the LT®1028 is still the lowest noise op amp for low source impedance applications.

The amount of noise an op amp circuit will produce is determined by the device used, the total resistance in the circuit, the bandwidth of the measurement, the temperature of the circuit and the gain of the circuit. A convenient figure of merit for the noise performance of an op amp is the spectral density or spot noise. This is obtained by normalizing the measurement to a unit of bandwidth. Here the unit is 1Hz and the noise is reported as "nV/$\sqrt{Hz}$." The noise in a particular application bandwidth can be calculated by multiplying the spot noise by the square root of the application bandwidth.

Some other simplifications are made to facilitate comparison. For instance, the noise is referred to the input of the circuit so that the effect of the circuit gain, which will vary with application, does not confuse the issue. Also, the calculations assume a temperature of 27°C or 300°K.

The formula used to calculate the spot noise and the schematic of the circuit used are shown in Figure 1. Figures 2 through 4 plot the spot noise of selected op amps vs the equivalent source resistance. The first two plots show precision op amps intended for low frequency applications, whereas the last plot shows high speed voltage-feedback op amps. There are two plots for the low frequency op amps because at very low frequencies (less than about 200Hz) an additional noise mechanism, which is inversely proportional to frequency, becomes important. This is called 1/f or flicker noise. Figure 2 shows slightly higher levels of noise due to this contribution.



WHERE: V_{TR1}, V_{TR2} AND V_{TR3} ARE THERMAL NOISE FROM RESISTORS

$$R_{eq} = R2 + \left(\frac{(R1)(R3)}{R1 + R3}\right)$$

$$4kT = (16.56)(10)^{-21}\ J$$

AND V_n IS THE VOLTAGE SPOT NOISE AND I_n IS THE CURRENT SPOT NOISE OF THE OP AMP AS GIVEN ON THE DATA SHEET.

$$V = \sqrt{(4kT)R_{eq} + V_n^2 + I_n^2(R_{eq}^2)}$$

IS THE INPUT REFERRED SPOT NOISE IN A 1Hz BANDWIDTH.

Figure 1

Studying the formula and the plots leads to several conclusions. The values of the resistors used should be as small as possible to minimize noise, but since the feedback resistor is a load on the output of the op amp, it must not be too small. For a small equivalent source resistance, the voltage noise dominates. As the resistance increases, the resistor noise becomes most important. When the source resistance is greater than 100k, the current noise dominates because the contribution of the current noise is proportional to R_{eq}, whereas the resistor noise is proportional to the $\sqrt{R_{eq}}$.

For low frequency applications and a source resistance greater than 100k, the LT1169 JFET input op amp is the obvious choice. Not only does the LT1169 have an extremely low current noise of 0.8fA/$\sqrt{Hz}$, it also has a very low voltage noise of 6nV/$\sqrt{Hz}$. The LT1169 also has excellent DC specifications, with a very low input bias current of 3pA (typical), which is maintained over the input common mode range, and a high gain of 120dB.

High speed op amps, here defined by slew rates greater than 100V/µs, are plotted in Figure 4. These op amps come in a wider range of speeds than the precision op amps plotted in Figures 2 and 3. The faster parts will generally have slightly more spot noise, but because they will most likely be selected on the basis of speed, a selection of parts is plotted. For example, the LT1354–LT1363 (these are single op amps; duals and quads are available) are close in noise performance and consequently cluster close together on the plot, but have a speed range of 12MHz GBW to 70MHz GBW.

The same information is presented in tabular form in Table 1.

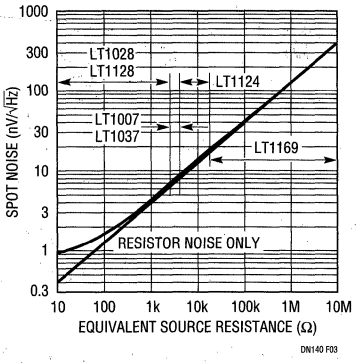


Figure 3. 1kHz Spot Noise vs Equivalent Source Resistance

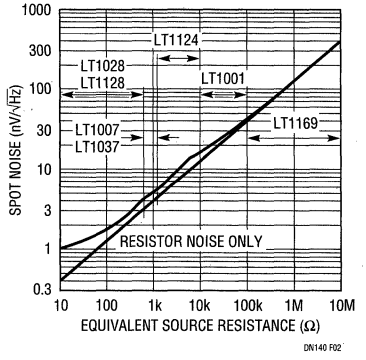


Figure 2. 10Hz Spot Noise vs Equivalent Source Resistance

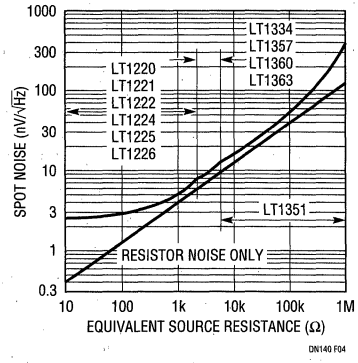


Figure 4. 10kHz Spot Noise vs Equivalent Source Resistance (High Speed Amplifiers)

Table 1. Best Op Amp for Lowest Noise vs Source Resistance

	BEST OP AMP		
SOURCE R (R_{eq})	**10Hz PRECISION**	**1000Hz PRECISION**	**10kHz HIGH SPEED**
0Ω to 500Ω	LT1028, LT1115, LT1128	LT1028, LT1115, LT1128	LT1220/21/22/24/25/26
500Ω to 1.5k	LT1007, LT1037	LT1028, LT1115, LT1128	LT1220/21/22/24/25/26
1.5k to 3k	LT1124/25/26/27	LT1028, LT1115, LT1128	LT1220/21/22/24/25/26
3k to 5k	LT1124/25/26/27	LT1007, LT1037	LT1220/21/22/24/25/26
5k to 10k	LT1124/25/26/27	LT1124/25/26/27	LT1354/57/60/63
10k to 20k	LT1001/02	LT1113, LT1124/25/26/27	LT1354/57/60/63
20k to 100k	LT1001/02	LT1055/56/57/58, LT1113, LT1169	LT1351
100k to 1M	LT1022, LT1055/56/57/58, LT1113, LT1122, LT1169	LT1022, LT1055/56/57/58, LT1113 LT1122, LT1169, LT1457	LT1351
1M to 10M	LT1022, LT1055/56/57/58, LT1113, LT1122, LT1169	LT1022, LT1055/56/57/58, LT1113 LT1122, LT1169, LT1457	

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LINEAR TECHNOLOGY

DESIGN NOTES

LTC1436-PLL Low Noise Switching Regulator Helps Control EMI

Design Note 141

John Seago

Electromagnetic interference (EMI) is a potential problem for the circuit designer. Switching regulators can cause EMI in many products. Linear Technology has developed new techniques like spread-spectrum modulation, phase-locked synchronization and Adaptive Power™ mode that can reduce the amount of unwanted interference.

New IC Solves Old Problems

The LTC®1436-PLL is a constant-frequency, current mode, synchronous step-down switching regulator that controls external N-channel MOSFETs for very efficient power conversion. It also features Adaptive Power mode, which provides constant frequency switching with good efficiency at light load currents. Figure 1a shows the audio frequencies generated by the 5V output of the circuit in Figure 2, while supplying 3mA of load current (0.1% of full load) using a cycle-skipping mode of operation. This mode may cause many cycles to be skipped between bursts of energy to the output capacitor. These energy bursts intrude into the audio band at sufficiently low output currents. Figure 1b shows that audio frequency noise is completely eliminated by the Adaptive Power mode under the same conditions.

Traditionally, efficiency is sacrificed to accomplish the audio frequency response shown in Figure 1b. Large synchronous MOSFETs are used to force continuous inductor current at the switching frequency, regardless of the load. The associated gate charge losses and losses caused by relatively large inductor ripple current result in very poor efficiency at light loads. The Adaptive Power mode uses only the small (SOT-23) MOSFET, Q3 and D2 in a conventional buck mode to allow constant frequency, discontinuous inductor current operation, which greatly decreases power loss. The gate-to-source capacitance of the small MOSFET is significantly less than either of the two large MOSFETs. Depending on component selection, there can be a 50-to-1 difference in gate-to-source capacitance between Q3 and Q1/Q2, so that Q3 requires only 2% of the gate drive power (loss) of Q1/Q2. This provides a substantial increase in efficiency at light loads.

New Feature Provides New EMI Control

In addition to audio frequency suppression, the LTC1436-PLL has three additional RF EMI control mechanisms:

1) The LTC1436-PLL allows switching frequency modulation to spread the spectrum of switching noise. Through frequency modulation, peak energy is decreased and spread over a wide range of frequencies as shown in Figure 3. The normal 190kHz switching frequency and its harmonics are shown by the bottom trace. The top (dashed) trace shows the result of modulating the phase-locked loop lowpass filter (PLL LPF) pin with a 100Hz sawtooth waveform. Switching frequency energy is reduced by over 20dB when modulated; second and third harmonics are attenuated even more in this example. Figure 4 shows the spectrum

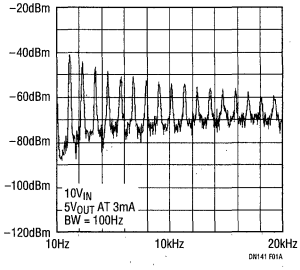

Figure 1a. Audio Frequency Generation in Cycle-Skipping Mode

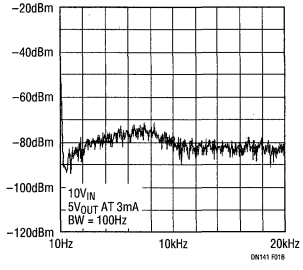

Figure 1b. Audio Frequency Amplitude with Adaptive Power Mode Operation

out to 100MHz resulting from PLL LPF modulation under the same conditions as in Figure 3.

2) The switching frequency can be programmed anywhere from 50kHz to 400kHz by selecting the appropriate value of oscillator capacitor. This places harmonics away from sensitive frequencies like 455kHz.

3) The switching frequency can be phase-locked to an external system clock so that harmonics and sidebands of the switching frequency are common with those generated by the system. This phase lock can be maintained over a ±30% frequency range around f_O.

Additional Features

The LTC1436-PLL provides a power-on reset timer function that flags an out-of-range output voltage condition, along with an auxiliary regulator that controls an external PNP transistor for an additional low noise, linear regulated output. The LTC1437 has all the features of the LTC1436-PLL plus an internal comparator with reference that can be used to detect a low-battery condition or provide other useful functions. The basic LTC1436 trades the phase-locked loop function for the additional comparator in the LTC1437.

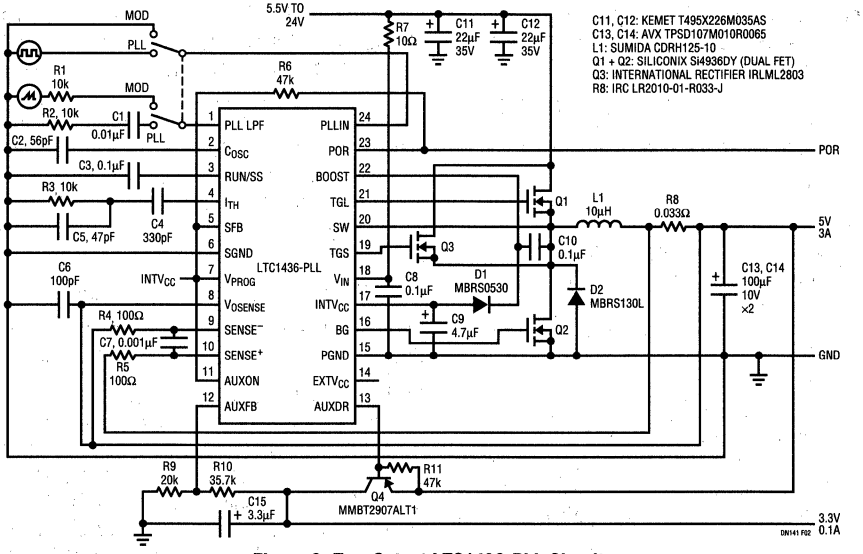

Figure 2. Two Output LTC1436-PLL Circuit

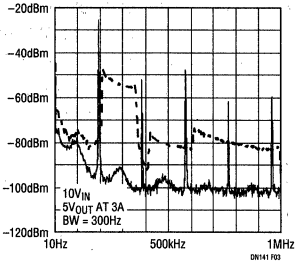

Figure 3. Before and After Frequency Spreading

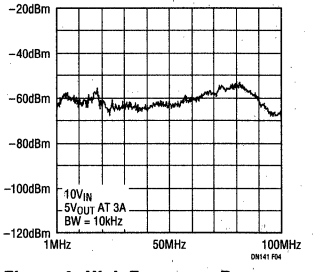

Figure 4. High Frequency Response with Frequency Spreading

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LINEAR TECHNOLOGY

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DESIGN NOTES

Ultralow Quiescent Current DC/DC Converters for Light Load Applications – Design Note 142

Sam Nork

In lightly loaded battery applications that require regulated power supplies, the quiescent current drawn by the DC/DC converter can represent a substantial portion of the average battery current drain. In such applications, minimizing the quiescent current of the DC/DC converter becomes a primary objective because this results in longer battery life and/or an increased power budget for the rest of the circuitry. The following two circuits provide regulated step-up and step-down DC/DC conversion and consume extremely low quiescent current.

2-Cell to 5V Conversion with I_Q = 12µA

The circuit in Figure 1 produces a regulated 5V output from a 2V to 5V input and consumes only 12µA (typical) of supply current. The LTC®1516 is a charge pump DC/DC converter that uses Burst Mode™ operation to provide a regulated 5V output.

This circuit achieves ultralow quiescent current by disabling the internal charge pump when the output is in regulation. The charge pump is enabled only when the output load forces the voltage on C_{OUT} to droop by approximately 80mV. External capacitors C1 and C2 are then used to transfer charge from V_{IN} to V_{OUT} until the output climbs back into regulation. This regulation method results in approximately 100mV of voltage ripple at the output.

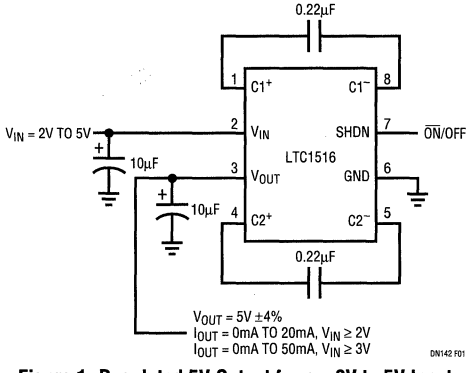

Figure 1. Regulated 5V Output from a 2V to 5V Input

The circuit is capable of providing up to 50mA of output current (for $V_{IN} \geq 3V$). As shown in Figure 2, typical efficiency exceeds 70% with load currents as low as 50µA.

The low quiescent current of the LTC1516 may render shutdown of the 5V supply unnecessary because the 12µA quiescent current is lower than the self-discharge rate of many batteries. However, the part is also equipped with a 1µA shutdown mode for additional power savings.

Ultralow Quiescent Current (I_Q < 5µA) Regulated Supply

The LTC1516 contains an internal resistor divider that draws only 1.5µA (typ) from V_{OUT}. During no-load conditions, the internal load causes a droop rate of only 150mV per second on V_{OUT} with C_{OUT} = 10µF. Applying a 5Hz to

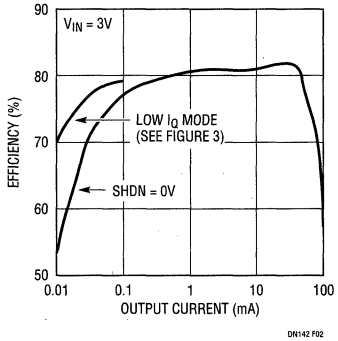

Figure 2. Efficiency vs Output Current

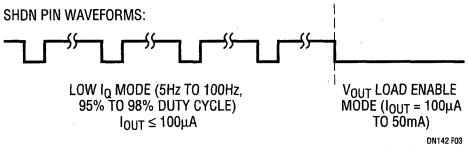

Figure 3. SHDN Pin Waveforms for Ultralow Quiescent Current Supply

100Hz, 95% to 98% duty cycle signal to the SHDN pin ensures that the circuit of Figure 1 comes out of shutdown frequently enough to maintain regulation during no-load or low-load conditions. Since the part spends nearly all of its time in shutdown, the no-load quiescent current (see Figure 4) is approximately equal to $(V_{OUT})(1.5\mu A)/(V_{IN})$(Efficiency).

The LTC1516 must be out of shutdown for a minimum duration of 200µs to allow enough time to sense the output and keep it in regulation. As the V_{OUT} load current increases, the frequency with which the part is taken out of shutdown must also be increased to prevent V_{OUT} from drooping below 4.8V during the OFF phase. A 100Hz 98% duty cycle signal on the SHDN pin ensures proper regulation with load currents as high as 100µA. When load current greater than 100µA is needed, the SHDN pin must be forced low, as in normal operation. The typical no-load supply current for this circuit with V_{IN} = 3V is only 3.2µA.

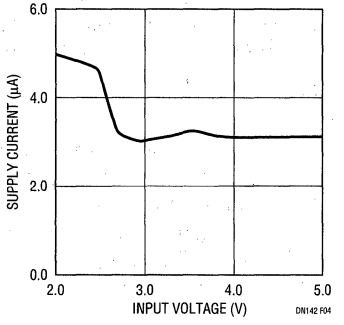

Figure 4. No-Load I_{CC} vs Input Voltage for Low I_Q Mode

Micropower LDO Regulator Consumes <5µA

The micropower linear regulator shown in Figure 5 delivers a regulated 3.3V output using less than 5µA quiescent current. With such low operating current, a standard 9V alkaline battery can power this regulator for 10 years.

Circuit operation is very straightforward. The LTC1440's internal reference connects to one input of the feedback comparator. A feedback voltage divider formed by R2 and R3 establishes the output voltage. The output of the comparator enables the current source formed by Q1, Q2, R1 and R4. When LTC1440's output is low, Q1 is turned on, allowing current to charge output capacitor C4. Local feedback formed by R4, Q1 and Q2 creates a constant current source from V_{IN} to C4. Peak charging current is set by R4 and the V_{BE} of Q2, which also provides current limiting in case of an output short to ground. With the values shown in Figure 5, the regulator is guaranteed to deliver at least 10mA output current with inputs as low as 4.8V (that is, from a fully discharged 9V battery).

Because the regulator implements a hysteretic feedback loop in place of the traditional linear feedback loop, no compensation is needed for loop stability. Furthermore, the extremely high gain of the comparator provides excellent load regulation and transient response. However, as with the LTC1516, the comparator hysteresis necessarily produces a small amount of output ripple. Output ripple can be reduced to 10mV–20mV peak-to-peak with feedforward capacitor C3 (see Figure 6), but no-load quiescent current increases by approximately 1.5µA. Without C3 the quiescent current is about 4.5µA, but output ripple is 50mV to 100mV peak-to-peak.

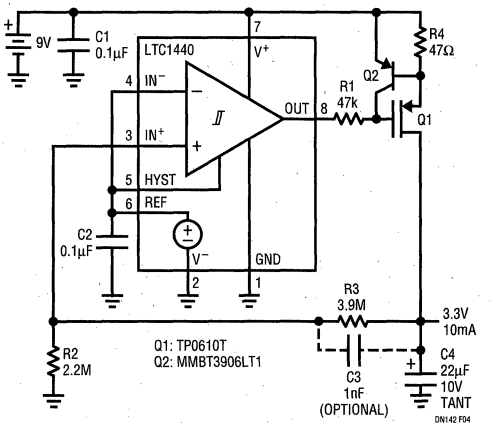

Figure 5. Micropower LDO Regulator

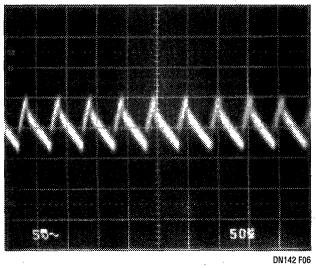

Figure 6. Typical Output Ripple Using 1nF Feedforward Capacitor

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LINEAR TECHNOLOGY

DESIGN NOTES

Single IC, Power Factor Corrected, Off-Line Supply

Design Note 143

Kurk Mathews

An ever increasing number of off-line power supplies now include power factor correction (PFC) in order to reduce input current and meet future regulatory requirements. Switching power supplies that incorporate a bridge rectifier followed by bulk capacitance create harmonic currents. These harmonics only increase the supply's RMS input current, while contributing nothing to real power. The typical solution to this problem has been to add a PFC preregulator and a separate controller to an existing design.

The LT®1508 (voltage mode) and LT1509 (current mode) eliminate the need for separate controllers by combining the PFC and a pulse width modulator (PWM) function in a single 20-pin IC. PFC is achieved by programming the input current of a boost regulator to follow the input line voltage. This results in a near-unity power factor compared to 0.5 to 0.7 for a typical capacitive input switcher. Linear's unique architecture maintains 0.99 power factor over a 20:1 load range. Figure 1 shows input current with output powers of 30W, 150W and 300W.

A number of issues associated with a 2-IC approach are addressed within the LT1508 and LT1509, resulting in a lower part count and improved PC board layout. Start-up is controlled by separate PFC and PWM soft start pins. The PWM Soft Start pin is held low, disabling the PWM output until the PFC stage is in regulation. The PWM will remain enabled as long as the PFC output voltage stays above 73% of its preset value (typically 280V out of 383V for universal input). A separate overvoltage protection pin can be connected to the output through an independent resistor divider. This ensures overvoltage protection during safety agency abnormal testing conditions, such as opening the main feedback path. The two stages are synchronized and the PWM turn-on is delayed for 50% of the oscillator cycle. This minimizes noise and conducted emission problems. 2A peak current gate drivers and a 1.2V optoisolator offset on the V_C pin further simplify the design.

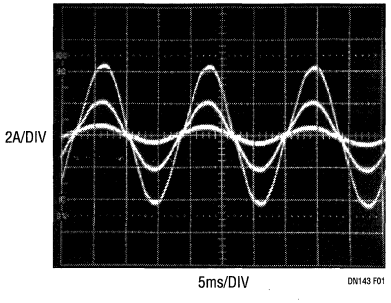

Figure 1. Input Current at 30W, 150W and 300W

A universal input, 24VDC, 300W converter using the LT1508 is shown in Figure 2. The circuit's user benefits include low cost, customizable footprint and off-the-shelf magnetics designed to meet UL and EC safety standards. Following the PFC boost preregulator is a 2-transistor forward converter that features low voltage (500VDC) switches, low peak currents and automatic nondissipative core reset. Under worst case conditions (low line, full power), the PFC and PWM stages have efficiencies of 90% and 92% respectively. See the graph in Figure 2 for typical overall efficiency versus input line and output power. The LT1508's low start-up current (250μA) minimizes start-up resistor power dissipation. An overwinding on T1 provides the bootstrapped chip supply. The intermediate bus voltage of 382V is well controlled, simplifying the post regulator and increasing capacitor holdup time compared to a typical off-line converter. This results in lower transformer primary current and simplified magnetics design. Different or additional outputs are easily accommodated with this topology by modifying T2 and L1.

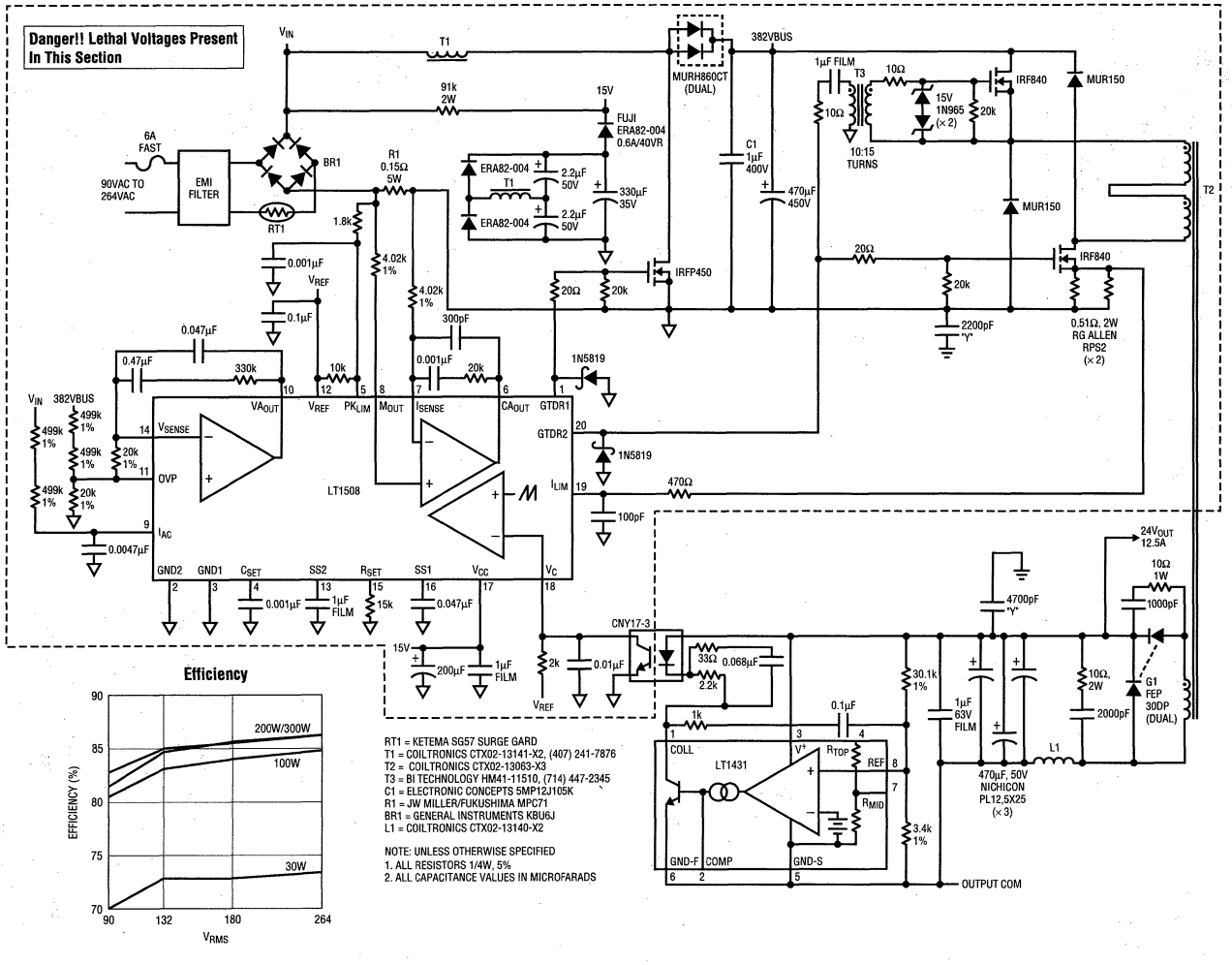

Figure 2. 24V, 300W Off-Line PFC Supply

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LINEAR TECHNOLOGY

LINEAR TECHNOLOGY

DESIGN NOTES

LT1511 Low Dropout, Constant-Current/Constant-Voltage 3A Battery Charger – Design Note 144

Chiawei Liao

Introduction

The LT®1511 current mode PWM battery charger is the simplest, most efficient solution for fast charging modern rechargeable batteries that require constant-current and/or constant-voltage charging including lithium-ion (Li-Ion), nickel-metal-hydride (NiMH) and nickel-cadmium (NiCd).

Higher Duty Cycle for the LT1511 Battery Charger

Maximum duty cycle for the LT1511 constant-current/constant-voltage battery charger is typically 90%, but this may be too low for some applications. For example, if an 18V ±3% adapter is used to charge ten NiMH cells, the charger must put out 15V maximum. A total of 1.6V is lost in the input diode, switch resistance, inductor resistance and parasitics, so the required duty cycle is 15/16.4 = 91.4%. As it turns out, duty cycle can be extended to 93% by restricting boost voltage to 5V instead of using V_{BAT}, as is normally done. This lower boost voltage also reduces power dissipation in the LT1511. Connect an external source of 3V to 6V at the V_X node in Figure 1 with a 10µF C_X bypass capacitor.

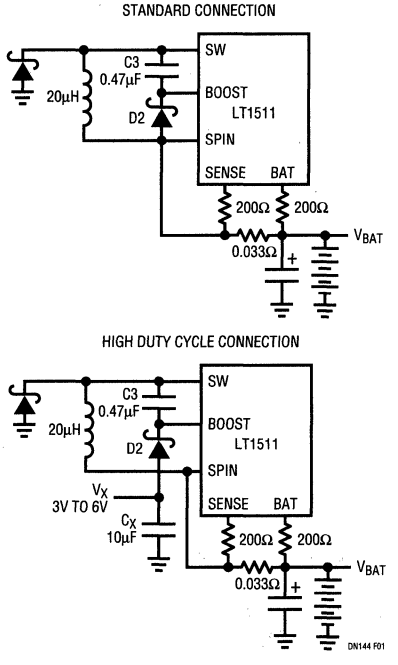


Figure 1. High Duty Cycle

Enhancing Dropout Voltage

For even lower dropout and/or to reduce heat on the board, the input diode can be replaced with a FET (see Figure 2). It is straightforward to connect a P-channel FET across the input diode and connect its gate to the battery so that the FET commutates off when the input goes low. The problem is that the gate must be pumped low so that the FET is fully turned on even when the input is only a volt or two above the battery voltage. There is also a turnoff speed issue. To avoid large current surges from the battery back through the charger into the FET, the FET should turn off instantly when the input is dead shorted.

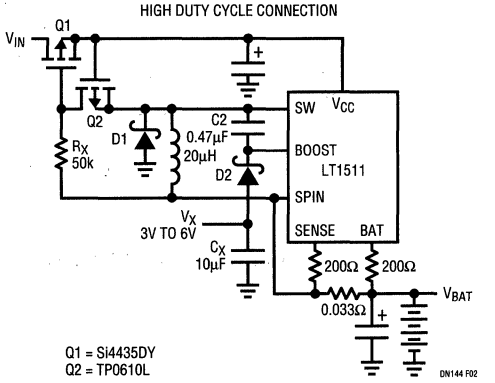


Figure 2. Replacing the Input Diode

Gate capacitance slows turnoff, so a small P-channel (Q2) is used to discharge the gate capacitance quickly in the event of an input short. The body diode of Q2 creates the necessary pumping action to keep the gate of Q1 low during normal operation. Note the Q1 and Q2 have a V_{GS} spec limit of 20V. This restricts V_{IN} to a maximum of 20V.

Figure 3 is a 3A complete constant-current/constant-voltage charger for 15V batteries. Input is from an 18V ±3% adapter. For adapter current limit and undervoltage lockout functions, please see the LT1511 data sheet.

For $V_{IN} > 20V$, the circuit in Figure 4 can be used to clamp V_{GS} to < 20V. R_{X1} and R_{X2} are chosen to draw 1mA or less to ensure that the 2.5V on PROG is sufficient to turn Q2 on. This gives a value for R_{X1} of about 6.2k and R_{X2} is calculated from:

$$R_{X2} = R_{X1}\left(\frac{V_{BAT}}{V_{GS} - V_{IN} + V_{BAT}} - 1\right)$$

V_{BAT} = Highest battery voltage
V_{GS} = Minimum Q1 gate drive
V_{IN} = Lowest input voltage

If R_{X1} = 6.2k, V_{BAT} = 19.5V, V_{GS} = 7V, V_{IN} = 21.5V,

Then R_{X2} = 18k

Note: Figure 1, 2 and 4 circuits are for 3A charging current. See the LT1511 data sheet for other design values.

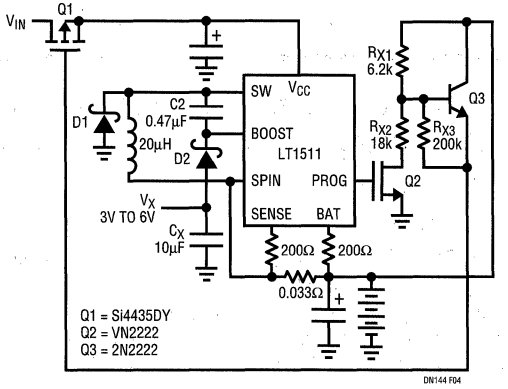


Figure 4. V_{IN} > 20V Low Dropout Charger

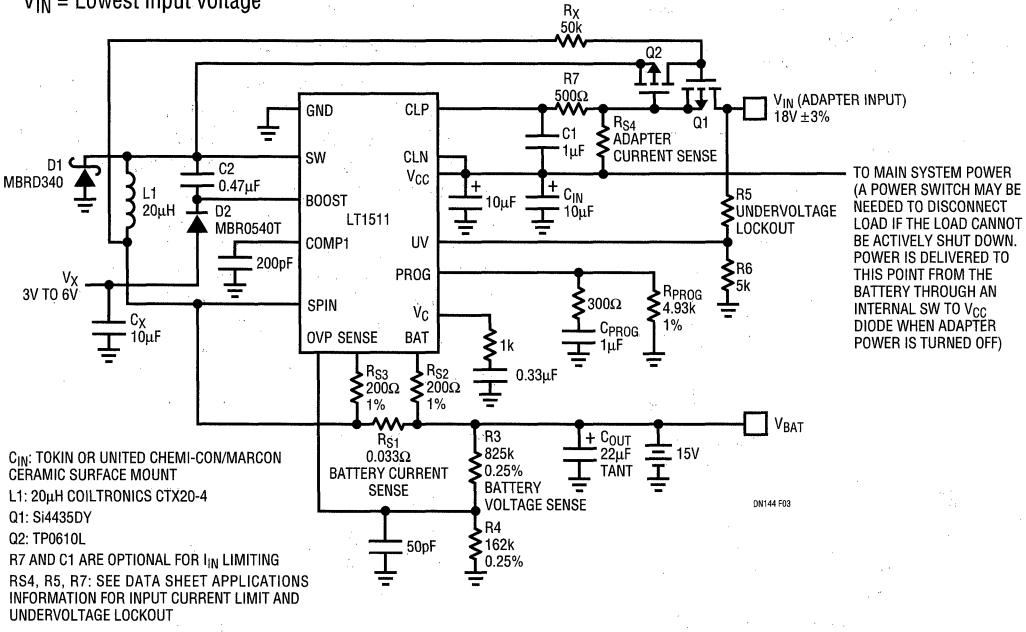


Figure 3. 3A Constant-Current/Constant-Voltage Low Dropout Battery Charger

For literature on our Battery Chargers, call **1-800-4-LINEAR**. For applications help, call (408) 432-1900, Ext. 2360

SECTION 3: REFERENCE READING

SECTION 3—REFERENCE READING

Avoid wiring-inductance problems.

Properly configured wiring can reduce unwanted coupling, troublesome feedback and noise pickup.

Do you know that there are 465 nH in just one foot of 30-AWG wire? And that a 10-ns current pulse of 10 mA produces a 0.5-V noise spike? But place the wire over a ground plane, and you reduce the inductance to 100 nH and the noise spike to 0.1 V.

Wiring inductance is often overlooked in the design of PC boards, back panels and cables. And many of the less obvious characteristics of inductance are not accounted for, even when an attempt is made to consider inductive effects. The result of this neglect is noise pickup, unwanted coupling and troublesome feedback.

You can calculate wiring inductances, however, and alleviate problems from this source. Let's see how.

What is inductance?

Inductance, L, can be defined by the equation

$$L = \frac{N\phi}{I}.$$

Magnetic flux "lines" ϕ, or linkages represented by the quantity $N\phi$ (turns $\times$ flux), accompany all current flow, I. Flux lines occur both internally and externally to the conductor. Inductance also is considered the parameter that represents how well flux lines can oppose changes in the flow of current in a circuit. The opposition to the change in flow of current, or self-inductance, is manifested by a back voltage, e, that develops in the circuit,

$$e = -L\, di/dt.$$

When the flux lines "cut" across, or couple, with other nearby conductors, voltage is induced in these conductors. The amount of induced voltage is determined by the degree of coupling, called mutual inductance.

Most engineers know how to calculate the self-inductance of an isolated wire, but they often overlook the mutual-inductance effect of a nearby return-current conductor. This neglect can lead to serious errors. If the return conductor is near, which is the usual case, the effect of the mutual inductance subtracts from the isolated self-inductance value and lowers the over-all self-inductance, L_s.

Fundamental formulas reviewed

The over-all self-inductance of two mutually coupled conductors in series (Fig. 1a) is given by the equation

$$L_s = L_1 + L_2 \pm 2L_m,$$

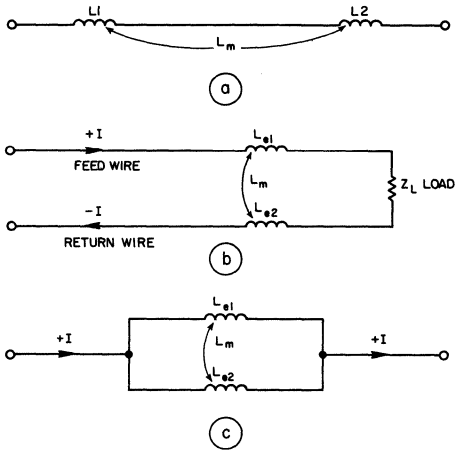
where

L_s = over-all self-inductance;
L_1 = self-inductance of one wire, if isolated;
L_2 = self-inductance of the other wire, if isolated;
L_m = mutual inductance between inductors.

If L_2 is a current-return conductor of the same length and diameter as L_1, then $L_1 = L_2$ and

$$L_s = 2(L_1 - L_m).$$

Usually, a load, Z_L, connects between the ends of a feed wire and its return (Fig. 1b). The ef-



1. **In calculating the inductance** between wired points in a circuit, you must take into account the mutual inductance (a) to nearby current paths, such as a return path (b) or between parallel feed paths (c).

Paul M. Rostek, Senior Circuit Design Engineer, NCR Corp., San Diego, CA 92127.

fective inductance, L_e, of each separate lead—feed or return wire—if the inductances are considered equal, is one-half of the over-all inductance, L_s. Thus

$L_{e1} = L_{e2} = (1/2)\ L_s = (L_1 - L_m)$ or $(L_2 - L_m)$.

Note that the effective inductance of each wire, L_e, is a lower value than the self-inductance of each wire when isolated.

The over-all self-inductance of two conductors in parallel (Fig. 1c) is given by

$$L_s = \frac{L_1 L_2 - L_m^2}{L_1 + L_2 - 2L_m}.$$

If the current in both conductors is in the same direction, and the conductors are equal in size and parallel, then L_m is positive. And since $L_1 = L_2$, then

$$L_s = \frac{L_1 + L_m}{2},$$

and

$$L_{e1} = L_{e2} = (L_1 + L_m) \text{ or } (L_2 + L_m).$$

Since the current flows in the same direction in both wiring legs, the mutual inductance, L_m, limits the reduction in over-all inductance. At large distances between the conductors, L_m approaches zero and L_s attains a maximum reduction of 50% in inductance.

Inductance changes with frequency

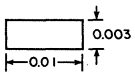
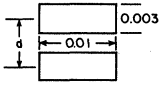
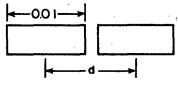
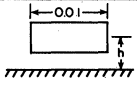
Magnetic flux traverses both the outside and inside of a wire that carries current. The self-inductance is thus composed of both the internal and external flux linkages. Since more total flux encloses, or links, the inside of a wire than its surface, a filament of the wire near the wire's center has greater inductance than a filament near its surface. Thus at high frequency, less current flows in the wire's interior. This phenomenon is known as the "skin effect," because the current concentrates at the wire's surface. Since the center of the wire carries less current,

Table of sample inductance calculations

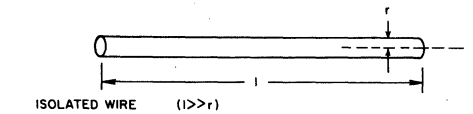
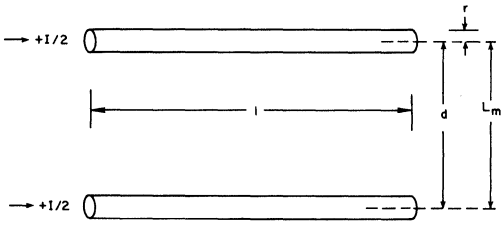
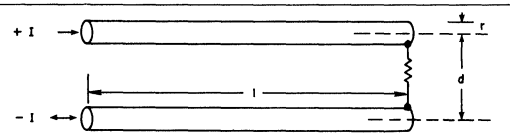
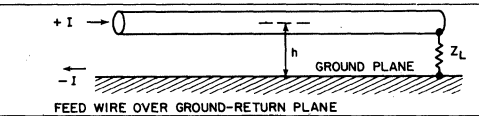
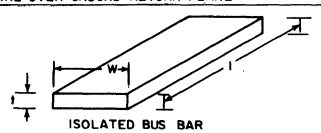
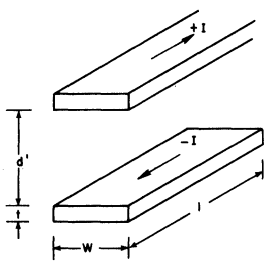
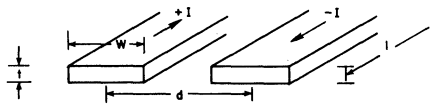
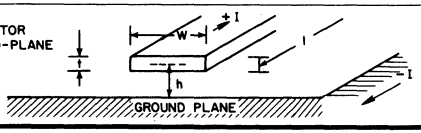
Self-inductance of 12 in. of 30-AWG circular wires at low frequencies

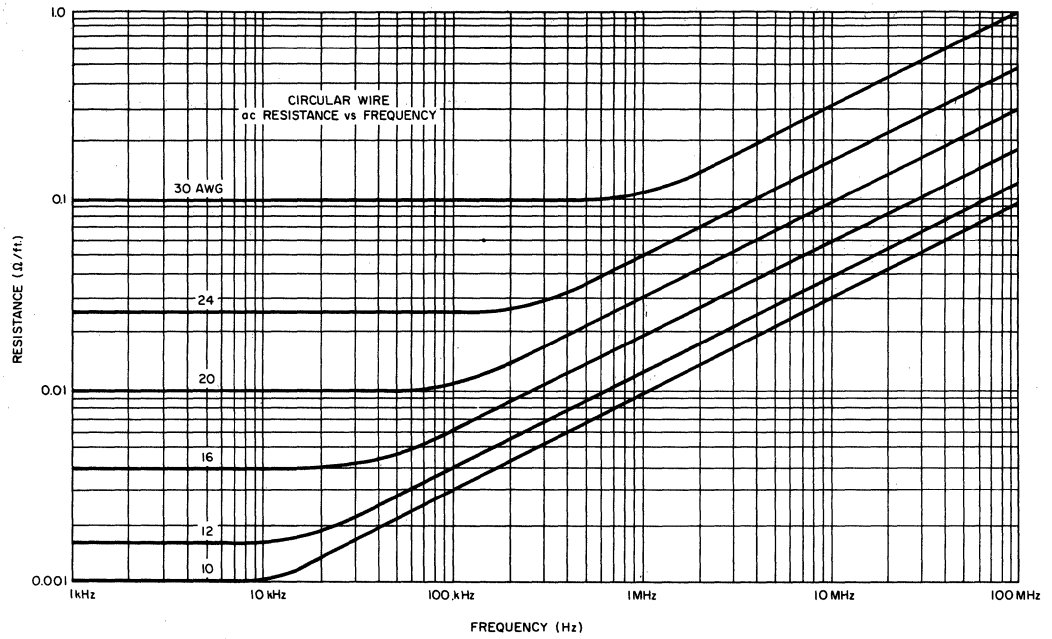
	SINGLE WIRE	PARALLEL CURRENTS	PARALLEL OPPOSING CURRENTS	RETURN CURRENT PLANE
SEPARATION	ISOLATED	d = 0.02 in.	d = 0.02 in.	h = 0.02 in.
INDUCTANCE	465 nH	415 nH	98 nH	140 nH
SEPARATION		d = 0.2 in.	d = 0.2 in.	h = 0.2 in.
INDUCTANCE		346 nH	236 nH	278 nH

Self-inductance of 12 in. of flat conductors at low frequencies

	SINGLE BUS	PARALLEL BUS	FLAT CABLE	BUS OVER GND PLANE
CONFIGURATION				
SEPARATION	ISOLATED	d = 0.02 in.	d = 0.02 in.	h = 0.02 in.
INDUCTANCE	482 nH	116 nH	116 nH	158 nH

Inductances for common wiring configurations

Configuration	Formulas All dimensions in inches, inductance is in nH
 ISOLATED WIRE (l>>r)	$L_s = 5\,l\left[\ln\frac{2\,l}{r} - 3/4\right]$ ---- Low frequency, $l >> r$, $\delta = 1/4$ $L_s = 5\,l\left[\ln\frac{2\,l}{r} - 1\right]$ ---- high frequency $l >> r$, limit as $f \to \infty$, $\delta \to 0$,
 FEED WIRES IN PARALLEL	$L_m = 5\,l\left[\ln\frac{2\,l}{d} - 1 + \frac{d}{l}\right]$ Mutual inductance between thin parallel wires.
	$L_s = \frac{L_1 + L_m}{2}$ or $\frac{L_2 + L_m}{2}$ $L_s = 5\,l\left[\ln\frac{2\,l}{\sqrt{r\,d}} - 1 + \frac{\mu\delta}{2}\right] l >> d$ Over-all self-inductance of two parallel wires, as used in distribution cables, or bus bars, where current is in the same direction.
 FEED AND RETURN WIRES	$L_e = L_s - L_m$ $L_e = 5\,l\left[\ln\frac{d}{r} + \mu\delta - \frac{d}{l}\right]$ Inductance of each of two wires in close proximity to each other, with current in each in opposite directions.
 FEED WIRE OVER GROUND-RETURN PLANE	$L_e = 5\,l\left[\ln\frac{2\,h}{r} + \mu\delta\right]$ Self-inductance of a wire only, when current return is via a ground plane.
 ISOLATED BUS BAR	$L_s = 5\,l\left[\ln\left(\frac{2\,l}{W+t}\right) + \frac{1}{2} + \frac{2}{9}\left(\frac{w+t}{l}\right)\right]$ Self-inductance of a flat etched conductor, bus bar or ground plane when isolated from a return path at low frequency.
 BUS BAR AND ADJACENT RETURN BUS	for low frequencies: $L_e = 5\,l\left[\ln\left(\frac{W}{W+t}\right) + 2.75\,\frac{d}{W}\right]$, for $W > d$, $W > t$ $L_e = 5\,l\left[\ln\left(\frac{d}{W+t}\right) + 1.5 - \frac{d}{l} + \frac{2}{9}\frac{W+t}{l}\right]$, for $d > W$, $W > t$ for high frequencies and $W >> t$: $L_e = \frac{14\,l}{W}\left[d' + \Delta\right]$, $\Delta = \frac{2.6}{\sqrt{f}}$, skin depth for copper Self-inductance of each conductor. Total inductance is the sum of inductances of the feed and return bus bar.
 FLAT CONDUCTOR AND ADJACENT RETURN-PATH CONDUCTOR	$L_e = 5\,l\left[\ln\frac{d}{W+t} + \frac{3}{2}\right]$ for low frequencies Self-inductance of each conductor. If feed conductor (+I) is flanked by two return flat conductors, the feed conductor's inductance remains the same.
 FLAT CONDUCTOR OVER GROUND-PLANE RETURN GROUND PLANE	$L_e = 5\,l\left[\ln\frac{6h}{t + .8W}\right] + \mu\delta$ Self-inductance of flat conductor only, when current return is via a ground plane.



2. **Skin effect causes an increase in the resistance** of a wire as the frequency increases.

the effective cross-section area is less and the wire's ac resistance is higher (Fig. 2). In addition the inductance is reduced by a skin-depth factor,[1] as follows for an isolated circular wire:

$$L_s = 5.08\,l\left[\,L_n\,\frac{2\,l}{r} + \mu\,\delta - 1 + \frac{r}{l}\right],$$

where

L_s = wire self-inductance in nanohenrys;
r = wire radius in inches;
l = wire length in inches;
μ = relative magnetic permeability (copper = 1.0);
δ = skin depth factor = $K/r\sqrt{\rho/\mu f}$ $(0 < \delta < 0.25)$;
ρ = volume resistivity in ohms-in. = 0.68×10^{-6} for copper;
K = conversion constant = 3168.

The change in inductance with frequency is small for a circular wire. Skin effect at very high frequencies decreases inductance by roughly 6% in short wires and about 2% in long wires. However, in parallel conductors, especially flat bus bars, the skin effect has greater influence and should not be neglected.

Lowering the self-inductance

The diameter of a wire does not have a major influence on its self-inductance (see table of sample calculations). For example, the self-inductance of a 2-AWG isolated wire with a diameter of 0.26 in. is approximately half the inductance of a 30-AWG wire with a diameter of 0.01 in. An increase of the wire size can provide a reduction of about 50% in self-inductance.

If the current is divided between two parallel conductors and flows in the same direction in each, the self-inductance can also be reduced to half if the wires are spaced far apart. For example, two 30-AWG wires, separated by 0.02 in., will reduce the over-all self-inductance only 18%; and for 0.2-in. separations, by 32%. A separation of several inches between wires reduces the over-all inductance approximately 50% of the self-inductance.

The most effective way to reduce inductance is to place the forward and return-current conductors in very close proximity. Two 30-AWG wires separated by 0.02 in., reduce the over-all self-inductance to one-fifth of a single isolated wire. Laminated bus bars or multilayer boards with closely spaced ground and voltage layers can reduce wiring inductance to one-tenth or less that of conductors isolated far from their return, or ground, plane. ■■

Reference

1. Grover, Frederick W., PhD., "Inductance Calculations," D. Van Nostrand Co., Inc., 1946.

SURGE IN SOLID TANTALUM CAPACITORS

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1.0 Introduction

With the introduction of high purity powders, automated assembly and real-time control systems, the base reliability of Tantalum capacitors has been increasing steadily in recent years. However, with the increasing usage of Tantalums in low impedance applications, the relative significance of the surge failure mode has also increased. With the present trend to use In Circuit Test machinery (ICTs) and fast rise time functional testers for board test purposes, the capacitors are more likely to experience a high current surge.

Another reason for the increasing level of awareness of the surge failure mode, is that Tantalum capacitors are increasingly being used in low impedance circuits, where previously Aluminum electrolytic capacitors were used. As a result they are more likely to see a surge condition. The change from Aluminum is because of their difficulty in conversion to surface mount technology packages.

It should be noted that surge fall-out is characterized by initial failures at the first power up of the board during in house manufacturing test, while the remaining population continue unaffected during operational life.

While the absolute ppm levels of failure would not normally be considered a problem, the failure mode in Tantalum capacitors is short circuit. Once a capacitor has become a short, if the current is not limited by a series resistance, the capacitor can overheat depending on the amount of fault power the capacitor has available to it. This makes the problem of concern to the industry.

Tantalum capacitor manufacturers have known of the problem for many years, and a great deal of Research and Development has gone into trying to understand the reason for the failure and a way of preventing its occurrence.

Investigation into surge failure has been complicated by the fact that Tantalum capacitors can "self-heal", and thus the failure could clear itself. One mechanism for this is given in Appendix 1.

Manufacturers have historically recommended 3 (or 1) Ohm/Volt resistance [16,17,20] be placed in series with each capacitor. This reduces the probability of a surge failure by limiting the amount of current available to the capacitor at switch on. Indeed for many years surge failures were not seen because the user either derated sufficiently or used the prescribed series resistor which prevented the failure occurring.

Manufacturers also recommend a voltage derating of between 50 and 75% [16,17,18] be applied if the capacitor is likely to experience fast switch on from a low impedance source, for example using a 35 Volt rated capacitor on a 12 Volt rail. The effect of voltage derating in steady-state conditions is well known, but derating has been empirically shown to reduce the number of failures in dynamic applications also, as will be demonstrated later in this paper.

Many companies have been analyzing the problem and trying to find a total solution. This document summarizes these findings and discusses some of the factors which can decrease the probability of a surge occurring and also explains what effect surge can have on a capacitor.

2.0 Cause

The conditions which can cause some Tantalum capacitors to fail by this mode are either a fast switch on from a low impedance circuit or a current spike seen by the capacitor during its operation. To date, research into the failure mechanism has shown that there are many factors which are known to increase the probability of a Tantalum capacitor to suffer a failure due to surge conditions.

2.1 Where to look for a surge condition.

Surge current conditions most commonly occur during the testing of a fully assembled board. Since the introduction of in circuit test machines into the vast majority of manufacturing plants throughout the world, this is by far the most common source of failures returned to the manufacturer for analysis.

Specialized test procedures can also produce failures. A typical example occurred with a switch mode power supply manufacturer. Once the power supply was assembled, it was functionally tested by powering it up with maximum working voltage with a maximum current being drawn from the supply. The power supply was then short circuited to simulate the user applying a screwdriver directly across the output terminals of the power supply. When the discharge current through the capacitors was measured it was found to be in the range 80 to 100 Amps, and dependent upon the point in the power supplies working cycle the short was applied.

Another possible cause is when the capacitor is being used to supply the energy required to energize an inductor, for example a relay coil, a DC motor or a loudspeaker, particular if the inductor is turned on or off by

means of a transistor. In this case large discharge currents can be seen by the capacitor, which can cause failure.

Another cause is particularly prevalent in racked electronic systems. It occurs when a card is plugged into a live motherboard. It is known as "hot-plugging" and causes very large current transients to be seen by the capacitors on the card.

2.2 What makes the number of surge failures increase?

The three major factors which decrease the likelihood of surge failures are:

(a) the amount of derating used by the circuit design engineer,

(b) the dielectric thickness designed into the capacitor by the manufacturer, and

(c) the circuit impedance in series with the capacitor.

But there are many others, such as the type of resin used as an encapsulant. If it has a significantly different expansion coefficient to that of Tantalum, then mechanical stress can be placed upon the Tantalum anode as the capacitor experiences thermal shock, which may result in internal damage to the anode, increasing the probability of a surge failure occurring.

The purity of the powder used also affects the surge performance, as it directly affects the capacitors' dielectric quality.

3.0 Effect

There are actually two theoretical mechanisms for a surge breakdown at present.

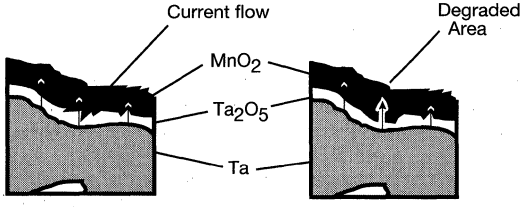

Figure 1. Cross section showing a degraded area of dielectric.

The first is a degraded dielectric due to an impurity in the original Tantalum powder. Figure 1 shows a section of dielectric, which is thinner than its neighboring sections due to an impurity in the Tantalum powder. When a large instantaneous current is now passed through the dielectric more current will pass through that thin section than its neighboring sections. This disproportionate amount of energy can cause self-healing to occur, as described in Appendix 1, or alternatively it can cause the capacitor to enter a thermal run away reaction which ultimately leads to failure of the capacitor.

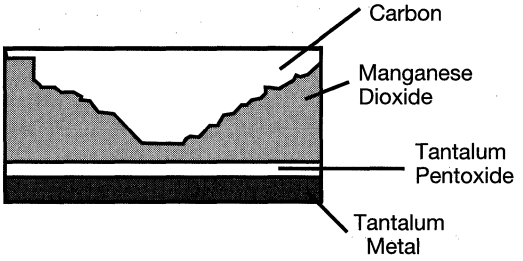

Figure 2. Cross section showing a degraded area of Manganese Dioxide.

The second is that a thin area of the negative electrode plate (Figure 2), Manganese Dioxide, plays a major role. In this theory, because the dielectric layer is uniform, the current is shared evenly throughout the anode. A thin area of dioxide has a lower resistance than a neighboring area, but power is I^2R, thus the dissipated energy is greater. Thus when a large instantaneous current flows, the power dissipated in the degraded area is higher than in neighboring areas. Again this causes a "hot spot" to develop and the dielectric to be broken down, ultimately leading to a short circuit failure. A more detailed explanation of these mechanisms is given in Appendix 3.

These areas of thin dielectric and manganese exist in all solid Tantalum Capacitors, and their presence does not mean that failures will occur. These features have been observed to be more prevalent in batches giving a higher fall-out on the accelerated surge test machinery used to ensure 100% of AVX SMT C, D, & E case product receives a minimum level of current surge.

When a Tantalum Capacitor fails it can become a short circuit. Thus a large amount of current can be drawn from the power supply. If this is not limited by means of a resistor, or power supply current limit, then the power will cause the capacitor to heat considerably. This may cause the capacitor's resin to blacken and char, which may be localized if associated with a low power level.

This is, of course, undesirable to both the Capacitor Manufacturer and the User. Again it should be remembered that this is a low ppm problem in certain applications only, thus the total number of capacitors affected is very small.

One way of reducing the probability of the Customer experiencing failures is for the Manufacturer to implement a screening program. Another is for the customer to apply derating, as stated in the introduction, or use a specialized part or if the problem is only associated with ICT machines then perhaps modify the voltage profile of the ICT or add resistance in the power line. All these reduce the incidence of failure still further.

Where the possibility of any heat damage or short circuit is required to be absolutely eliminated then AVX, along with several other manufacturers, has developed and introduced a fused range of capacitors.

These are designed to fail open circuit and not burn. For further information see Ian Salisbury's paper [15].

4.0 Cure

4.1 From the Manufacturer's viewpoint...

4.1.1 Tantalum powder purity.

As we stated in section 3.0, impurities in the Tantalum powder used to produce the capacitor are believed to cause points of lower dielectric strength to form, which during rapid turn-on conditions can lead to a dielectric breakdown. Over the last 10 years the impurity levels of all major contaminants in the tantalum powder have been reduced by joint development programs with the powder suppliers. The leakage current of a sintered Tantalum anode can be measured, and the level of this current is a good measure of the dielectric quality, and hence of the impurity levels. Figure 3 shows a comparison of the wet leakage current levels of a standard powder in use in previous years and one of the new high purity powders presently in use.

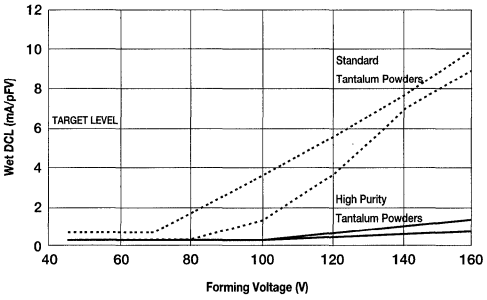

Figure 3. Wet leakage current against formation voltage.

These programs are of course ongoing and further improvements are planned.

4.1.2 Dielectric thickness.

To illustrate this factor four control batches of capacitors were made under the supervision of the Research and Development department at AVX. The batches were made the same capacitance value, but with different dielectric thicknesses (controlled by the forming voltage, the higher the value the thicker the dielectric). 500 units from each of the batches were then "surged" in the accelerating surge failure circuit described in Appendix 2 at rated voltage, and 75% rated voltage. To determine any relationship between power supply current limit and the number of failures, 500 units from each batch were also surged at a higher current limit and 75% rated voltage. The results are shown in Table 1.

The four batches were all 47µF capacitors and their rated voltage was 16 Volts. This capacitor was chosen because it is the highest CV value (752 µFV) manufactured in the D case package, and thus has the largest surface area. The more surface area the greater the probability of a weak area in the dielectric. It is also one of the most popular ratings.

Table 1.
Dielectric thickness against surge voltage

Capacitor Working Voltage (V)	16	16	16	20
Formulation Ratio	3.4 : 1	3.8 : 1	4.1 : 1	4.3 : 1
Formulation Voltage (V)	54.4	61.2	65.7	87.1
Dielectric Thickness (nm)	**92.5**	**104.0**	**111.7**	**148.1**
12V Current Limit = 3A	0.4%	0.2%	0%	0%
12V Current Limit = 5A	0.4%	0.2%	0%	0%
16V Current Limit - 3A	6.8%	6.6%	2.4%	0.2%

It can be seen from Table 1 that as the forming voltage increases, the number of failures decreases. It can also be seen that as the derating is increased, fewer failures occur. Derating will be discussed in more detail later in this paper.

The two sets of results in Table 1 for the 12 Volt surge (25% derating) show that the current limit set on the power supply has no effect on the number of failures which are seen. This is due to the relative slowness of the vast majority of power supply current limiting circuits (usually of the order of milliseconds) compared with the microseconds it takes to reach the peak current.

All that the power supply's current limit does is limit the fault current which is seen by a failed Tantalum capacitor. The more fault power available to the capacitor, the more catastrophic the failure will be [7]. At low fault powers it may be seen only as a slight crack in the casing, at higher fault powers the exterior of the capacitor may become completely charred.

4.1.3 Ensuring an even Manganese Dioxide coat.

Since the introduction of the 100% surge testing at AVX (the original equipment used did not distinguish surge fallout from the normal line fallout at final test) it has become possible for AVX to characterize individual batches for this parameter. This is due to the development of dedicated equipment capable of dynamic testing of capacitors, at low series resistance with test statistics being maintained for the individual batches. In addition, this fallout statistic can be monitored using statistical methods, such as SPC, on a code by code basis.

Methodical failure analysis of the surge fallout compared to capacitors which exhibited satisfactory performance revealed a common trend, standard in the external manganese dioxide coating, for failed parts.

Although the average manganese thickness was consistent over all the anode area surfaces, these parts typically demonstrated larger variations in porosity and morphology of the outer layers, as shown in Figure 4.

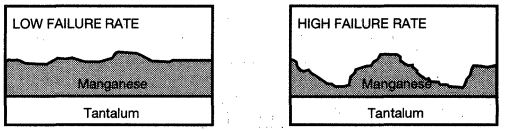

Figure 4. Variations in Manganese layer.

Again it should be remembered that these areas of thin manganese exist in all solid Tantalum capacitors, and their presence does not mean that failure will occur.

The Manganese Dioxide layer is built up by dipping the anodized Tantalum pellet into varying specific densities of Manganese Nitrate solution. The Nitrate is then decomposed to Dioxide by heating the pellet. By varying the specific densities and number of dips it is possible to finely adjust the coverage of the Tantalum pellet with Dioxide to ensure an even thick layer on the outer surface, and excellent coverage of the surface inside the pellet. This is then verified by means of a scanning electron microscope sample from each batch of processed anodes.

4.1.4 Surge screening.

This is where the Tantalum capacitor manufacturer tries to simulate the conditions seen at the customer by simulating a worst case surge scenario. Test methodology already in existence has required much refining as it was not geared to current applications or 100% test capability.

This is one area that is not clearly defined by the Tantalum Industry at present. Each Tantalum capacitor manufacturer has their own set of conditions for this test.

For example, one standard test requires 24 sample units to be connected in parallel to a very large reservoir capacitor through a mercury wetted relay. The reservoir capacitor is charged to 1.3 times the capacitors' under test rated voltage. The total circuit resistance seen by the first capacitor under test, and the reservoir capacitor is less than 0.1 Ohm. As will be shown later in section 4.3.1, this means that the first capacitors in line will receive a very large transient current, but the capacitor farthest away will see very little. As such, the test unequally stresses the capacitors.

4.1.4.1 What screen conditions does AVX use?

AVX uses a circuit as shown in Figure 5.
The test sequence is as follows:

(a) The 2200µF capacitor is charged to the capacitor's rated voltage.
(b) The probes are brought down onto the capacitor under test. The switching FET is OFF at this stage so no current will flow.
(c) The FET is turned ON, thus allowing current to flow and the capacitor to charge.
(d) The current is monitored by means of the 0.1Ω resistor in the source log of the transistor and the part dynamically sentenced according to the following rules. Figure 6 shows the expected current waveform. Figure 7 shows a part which has not received the minimum level of surge current, possibly due to a bad contact, this part will be rejected. Figure 8 shows a part which has failed, because the current has not fallen to around zero after a set time delay.
(e) The FET is turned OFF, thus stopping the charging process.
(f) Finally, the probes are lifted and the process starts again with the next capacitor.

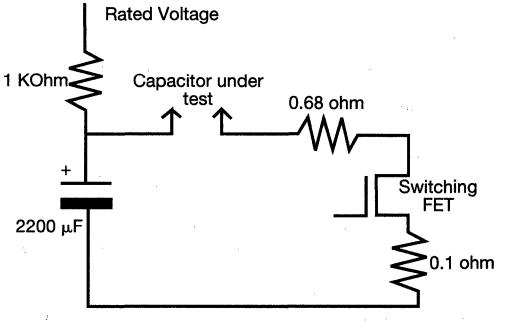

Figure 5. Circuit schematic

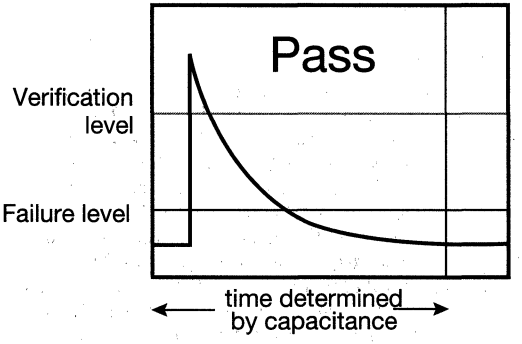

Figure 6. A Pass profile

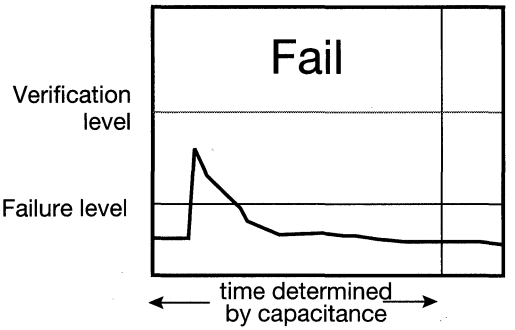

Figure 7. Not enough current seen

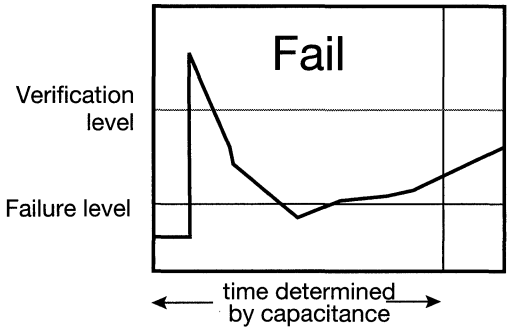

Figure 8. Part failed due to surge mechanism

AVX uses a circuit as shown in figure 5 to test large case size surface mount (chip) product. The lower case size chips inherently have a high ESR which self limits the maximum surge current the capacitor can see, and as such are not tested in the same way. Dipped product use a similar circuit to the large case size chip tester.

The reason for not testing parts in banks (in parallel) will become clear in a following section. The method used by AVX provides verification that 100% of capacitors have survived a minimum level of current surge and gives valuable feedback to the manufacturing engineers on a statistical basis to further enhance the process and design parameters.

4.1.4.2 How many surges should the capacitor receive?

The vast majority of surge failures occur on the first surge, as reported in 1980 by H. W. Holland[1] as occuring on the first pulse. Since then experiments carried out at AVX have shown that even under accelerated conditions this percentage has grown to almost 100%. This is due to the improvement of capacitor technology and the increasing severity of the surge screen test picking up more of the potential failures. The results of a trial of 578,676 capacitors carried out recently prove this. The capacitors were passed through the previously described surge equipment (section 4.1.4.1) 3 times at maximum stress and the number of failures recorded at each stage.

Thus 99.2% were seen to fail on the first surge and 0.8% subsequently. These figures were determined using a piece of equipment designed to induce failures.

In standard designs (where less current is available and 50% derating is incorporated, see 4.2.1) the acceleration is less aggressive and residual failures after the first surge are unlikely. As such, field surge failures are extremely rare and any residual surge failure is usually confined to manufacturers' testing of completed boards.

State of the art surge testing, as used at AVX, thus includes several acceleration factors over that of a typical customer ICT or functional tester.

In addition to the acceleration factors, product is tested 100% through this system, prior to the final parametric test sequence (see appendix 2).

4.1.5 Leakage current.

A commonly held misconception is that the leakage current of a Tantalum capacitor can predict whether or not the unit will fail on a surge screen. Although the short circuit failure mechanisms can, under lower stress conditions, be so localized as to still allow good readings for other parameters, the resultant leakage current will be high. This fault current is independent of the initial leakage characteristics as shown by the results of an experiment carried out at AVX on 47µF 10V surface mount capacitors. The results are summarized in Table 2.

Table 2.
Leakage current vs number of surge failures.

	Number tested	Number failed surge
Standard leakage range 0.1µA to 1µA	10,000	25
Over Catalog limit 5µA to 50µA	10,000	26
Classified Short Circuit 50µA to 500µA	10,000	25

It must be remembered that these results were derived from a highly accelerated surge test machine, used to induce a measurable failure rate.

4.2 From the user's viewpoint...

4.2.1 Derating.

Most manufacturers of Tantalum capacitors recommend that on a particular voltage rail, say 5 volts, a capacitor rated at twice that value (10 volts in this case) be used, if the capacitor is likely to be subjected to a rapid turn-on from a low impedance source. The capacitor is said to be derated by 50%.

Derating is

$$\left(1- \frac{\text{user's working voltage}}{\text{capacitors rated voltage}}\right) \times 100\%.$$

The reason for this is that experience has shown that a Tantalum capacitor is less likely to fail the higher the derating applied.

A 10 volt capacitor has a thicker dielectric than a 6.3 volt part, and as such the probability of a defect site existing which has a low enough activation energy to cause a short circuit when 5 volts is applied is lower than with the 6.3 volt part. Thus there are fewer failures than when a 10 volt part is placed on a 5 volt rail and a surge applied, than when a 6.3 volt part is subjected to the same conditions.

Derating can best be summed up by Table 3.

Table 3.

Voltage Rail	Working Cap Voltage
3.3	6.3
5	10
10	20
12	25
15	35
≥24	Series Combinations (11)

Recommended derating table.

Results of experiments, like those in Table 1, show this rule's effect on the surge fall-out.

This experiment was scaled up using production equipment with several million capacitors being tested. The results are shown in Table 4.

Table 4.

Capacitance and Voltage	No. of units tested	50% derating applied	No derating applied
47µF 16V	1,547,587	0.03%	1.1%
100µF 10V	632,875	0.01%	0.5%
22µF 25V	2,256,258	0.01%	0.3%

Results of production scale derating experiment

As can clearly be seen from the results of this experiment, the more derating applied by the user, the less likely the probability of a surge failure occurring.

It must be remembered that these results were derived from a highly accelerated surge test machine, and ICT failure rates in the low ppm are more likely with the end customer.

An example: a major manufacturer was experiencing a 4100 ppm failure rate with 22µF 20V product. This part was used on both the 12 and 5 volt rails. When the application was examined more closely it was seen that the failure rate on the 5 volt line was only 20 ppm. 25 volt parts were supplied for trial with the customer who reported that the failure rate had dropped down to 231 ppm. This clearly shows that when the 50% derating rule is applied failure can be dramatically reduced, and by close cooperation between the customer and supplier, this can be eliminated altogether.

An added bonus of increasing the derating applied in a circuit, to improve the ability of the capacitor to withstand surge conditions, is that the steady-state reliability is improved by up to an order. Consider the example of a 6.3 volt capacitor being used on a 5 volt rail. The steady state reliability of a Tantalum capacitor is affected by three parameters; temperature, series resistance and voltage derating. Assuming 40°C operation and 0.1Ω/volt of series resistance, the scaling factor for temperature will be 0.05 and for resistance unity. The factor for derating will be 0.15. The capacitor's reliability will therefore be

$$\begin{aligned}\text{Failure rate} &= F_U \times F_T \times F_R \times 1\%/1000 \text{ hours} \\ &= 0.15 \times 0.05 \times 1 \times 1\%/1000 \text{ hours} \\ &= \frac{7.5 \times 10^{-3}/1000 \text{ hours}}{1}\end{aligned}$$

$$\text{or an MTBF of } \frac{}{7.5\times10^{-3}} \times 1000 = 133{,}333 \text{ hours}$$

If a 10 volt capacitor was used instead the new scaling factor would be 0.017, thus the steady-state reliability would be

$$\begin{aligned}\text{Failure rate} &= F_U \times F_T \times F_R \times 1\%/1000 \text{ hours} \\ &= 0.017 \times 0.05 \times 1 \times 1\%/1000 \text{ hours} \\ &= 8.5 \times 10^{-4}/1000 \text{ hours}\end{aligned}$$

$$\text{or an MTBF of } \frac{1}{8.5\times10^{-4}} \times 1000 = 1176{,}470 \text{ hours}$$

So there is an order improvement in the capacitor's steady-state reliability.

4.2.2 Voltage profile shaping.

Figure 9 below shows the profile of a 33µF capacitor subjected to a 12 volt fast turn-on voltage profile with 1 Ohm of circuit resistance in series with it. It can be seen that the peak current is about 12 Amps.

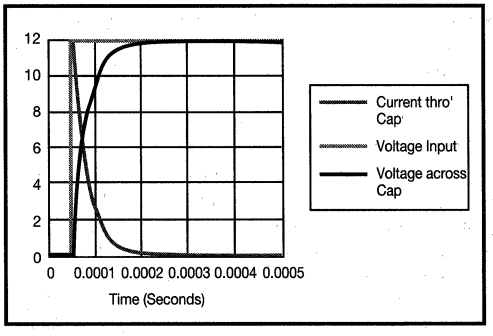

Figure 9. 33µF capacitor, 12 Volt surge, 1 Ohm resistance.

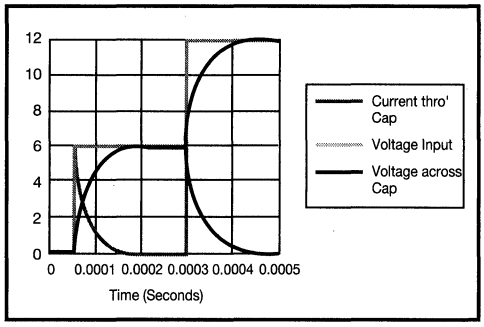

Figure 10. Two stage turn-on for a 33µF capacitor

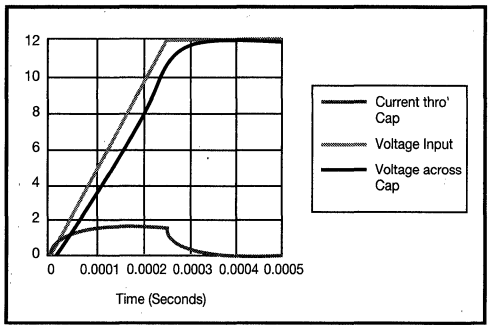

Figure 11. Ramp profile for a 33µF capacitor.

If the profile were then modified to be a two stage turn-on, see Figure 10, the capacitor would then be subjected to two current surges of peak amplitude 6 Amps. This is a less severe test, and even though the capacitor is experiencing twice the number of surges the probability of a failure is less.

Figure 11 shows a voltage profile which is slowly ramped up to its final value. In this case the peak current is less than 2 Amps, and thus this is the least severe of the test conditions. It should be remembered that the slower the ramp up the lower the probability of a failure.

This method of reducing the probability of failure is again of course out of the hands of the Manufacturer, however, he must be aware of the various factors which may cause surge. Thus the voltage and current profiles of a board experiencing failures can help when diagnosing the failure mechanism.

4.2.3 Series Resistance.

The peak current and rise time of the voltage profile are determined by the amount of circuit resistance in series with the capacitor. The instantaneous peak current at turn-on will be limited by the capacitors ESR and the series resistance, thus the peak current can be calculated from Ohms Law.

Example: a 33µF 20V capacitor with a maximum ESR value of 200 mΩ at 100KHz is used on a 10 Volt power line. The power is supplied to the card through a motherboard. Power is supplied to the motherboard by a linear regulator which has an output impedance of 150 mΩ. The contact resistance of the motherboard connector is 100 mΩ maximum. The daughter board's connector has a similar contact resistance. The track resistance is estimated at 50 mΩ maximum. This gives a maximum circuit resistance, external to the capacitor of 150 + 100 + 100 + 50 = 400 mΩ. The theoretical peak current is:

Equivalent resistance = 0.4 + 0.2 = 0.6 Ω
Peak current = Voltage/Resistance = 10/0.6 = 16.7 Amps

From this example calculation it is obvious that the larger the series resistor the smaller the peak current, and thus the less likely the capacitor will be to fail.

Example: a major disk drive manufacturer was experiencing problems with 47µF 16V capacitors being used on a 12 volt rail. The capacitor had a 2.2Ω resistor in series with it, across a 12 volt rail. The 12 volt rail supplied the drive motors, which were turned on and off by means of FETs. The resistor was changed to 10Ω, which still allowed the circuit to be operated within its design parameters, but prevented the capacitors experiencing the rapid discharge when the motors were turned on. The failures stopped. Another solution to this would be to redesign the board and utilize two 22µF 25V capacitors of the same case size in parallel to provide the minimum 50% derating that is recommended (as described in section 4.2.1). In highly inductive circuits such as this with no additional resistance available then derating up to 70% may be necessary.

Of course it is usually not possible for the customer to insert a series resistor in his power supply line. But, the customer could reduce the peak current by altering the voltage profile using methods which were described in section 4.2.2.

On one occasion it was necessary for a customer to measure the profile of his ICT tester for a particular board. As no current probe was available a 1Ω resistor was placed in series between the return path from the board and the ICT machine's power supply's ground terminal. Measurements were made but no unusual stresses were seen in the boards tested could be found. However, after the measurements had been made, the line ppm was seen to drop dramatically. During a follow up visit, it was noted that the 1Ω resistor had been left in place, which thus provided an effective example of series resistance reducing surge fall-out.

Most power supplies, and a large number of plug in boards, now have a diode between the power line and the capacitor. This acts as a series resistance during the surge condition. Figure 12 shows the surge on a 22µF 25V capacitor, running on a 10 volt rail in a telecommunications line conditioning card. In the circuit there was no diode. Figure 134 shows the same circuit with a 1N4001 diode in series between the connector and the capacitor.

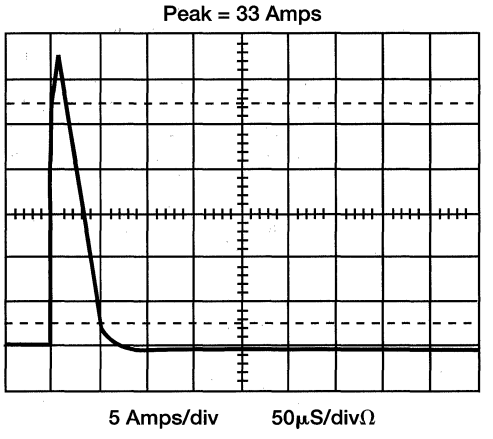

Figure 12. Current waveform without diode.

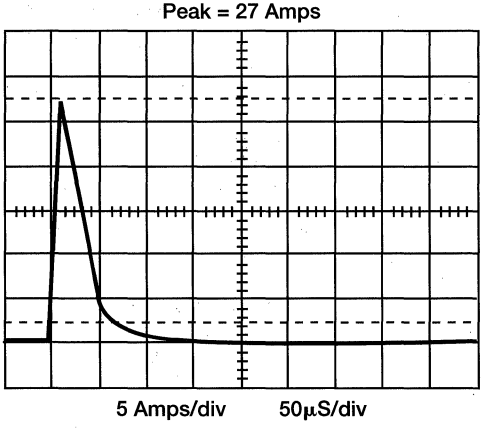

Figure 13. Current waveform with diode

If the resistance is then calculated for these two waveforms, using Ohm's Law, Figure 12 yields 30mΩ and Figure 13 yields 370mΩ. It can thus be assumed that the diode has added 70mΩ to the circuit.

This example shows that a diode may only contribute as little as 70mΩ of series resistance to a circuit and thus the capacitor can still experience the large current surges which can cause failures.

4.3 From the application viewpoint...

4.3.1 Capacitors surged in parallel.

In the vast majority of applications, a board will have more than one capacitor on each power rail. These capacitors are generally scattered throughout a board.

When a failure is reported, if the surge mechanism is the culprit, it will be noticed that one location fails more frequently than the other capacitors on the same voltage line. The usual location is that nearest to the connector through which power is applied.

To illustrate the reason why this is the case, a test board was constructed with three 22μF 25V capacitors in parallel on a piece of strip board. The capacitors positive terminals were connected to the strip board by pieces of wire to enable a current probe to be used for monitoring the current through each capacitor during a fast turn-on condition.

The resulting waveforms are shown in Figures 14, 15 and 16.

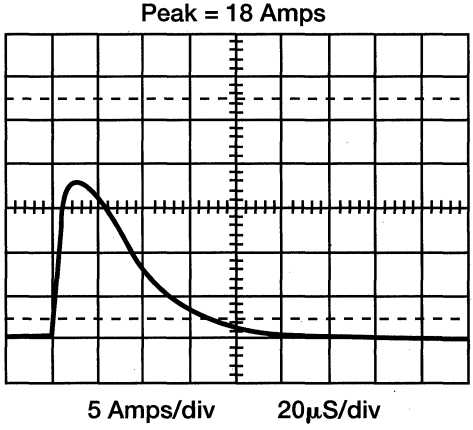

Figure 14. Current through **First Capacitor**

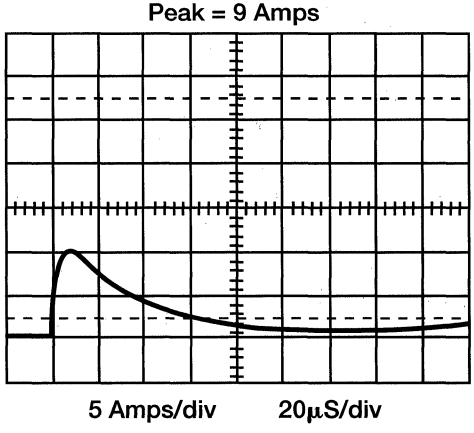

Figure 15. Current through **Second Capacitor.**

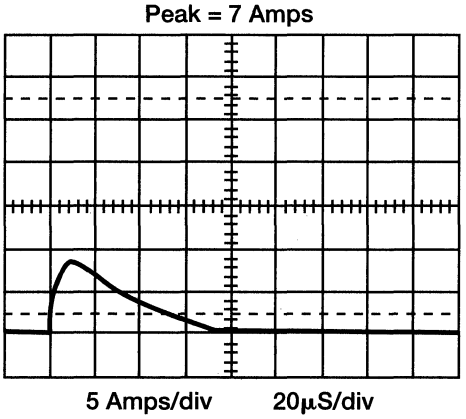

Figure 16. Current through **Third Capacitor.**

As can be clearly seen the capacitor nearest the power supply takes the "lion's share" of the available current and the farther away from the power supply the capacitor is, the less severe the current surge condition seen. It is for this reason that the capacitor nearest the power supply usually fails more frequently than the others.

5.0 Steady-State Reliability of Tantalum capacitors subjected to single and repetitive surges

The reliability of screened Tantalum capacitors is the same as unscreened components[5]. Thus they have identical failure rates and life expectancies. It only reduces the capacitors' probability of failing due to the surge mechanism.

50 x 22μF 25V capacitors were surged 500 times at rated voltage and 20 Amps. Another sample of 50 pieces was subjected to 10,000 surges at rated voltage and 20 Amps. These were submitted to an independent test house for life test analysis together with a control sample which had received no surges. The results showed that there was no detectable difference between the three samples. That is to say the steady state reliability of the capacitors had not been affected.

6.0 Conclusions

(1) The only real way to screen for components likely to fail under turn-on conditions in low impedance circuits which have a high current availability is to 100% test capacitors manufactured, and verify that the parts have received the required screening current.

(2) Capacitors should be individually tested by the manufacturer otherwise the current is shared between all the capacitors under test. This makes the test less severe, and the screening less effective.

(3) The customer should use a derating of 50% where the capacitor is likely to experience a current surge condition and in highly inductive circuits this may need to be increased to 70%.

(4) The current limit of the power supply should be set to the minimum required to power the board under test, as the lower the current limit the less severe the consequences of a surge failure.

(5) If possible the voltage profile should be a ramp turn-on, as this reduces the peak current seen by the capacitor.

(6) **Don't always assume that the failure is due to surge,** it may be a random failure. A surge failure will mainly occur the first time the board is powered up, particularly if an ICT "shorts/open circuit test" on the board previously showed all components to be good. Surge failures will, however, tend to occur at the specific high stress locations rather than randomly over the board.

(7) Because derating is one of the biggest contributing factors to irradicating surge failures, AVX has embarked on a program of producing extended range capacitors, specifically for this type of circuit location. For example, AVX was the first manufacturer to produce a 22μF 25V capacitor in a D case, and also has an E case capacitor which allows a 22μF 35V capacitor to be available to the designer.

Acknowledgements

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Further reading

[1] H. W. Holland, "Effects of high current transients on solid Tantalum capacitors", Kemet, 1976.

[2] B. M. Mogilevsky & G. A. Shirn, "Surge Current Failure in Solid Electrolyte Tantalum Capacitors", IEE Transactions on Components, Hybrids and manufacturing technology, Vol. CHMT-9, No. 4, December 1986.

[3] Y. Hasegawa, "A Study of Field Failures of Solid Tantalum Capacitors", NEC Res. & Develop., No. 82, July 1986.

[4] J. D. Moynihan, "Unshackle the Solid Tantalum Capacitor", Sprague, 1979.

[5] J. D. Moynihan, "Life evaluation of Solid Tantalum Capacitors under ON-OFF cycled conditions", Sprague.

[6] Dr. A. M. Holladay & J. D. Moynihan, "Effectiveness of Surge Current Screening of Solid Tantalum Capacitors", Sprague TP83-2.

[7] R. W. Franklin, "Over-Heating in Failed Tantalum Capacitors", AVX.

[8] R. W. Franklin, "Upgraded surge performance of tantalum capacitors", Electronic Engineering, 1985.

[9] R. W. Franklin, "Screening beats surge threat", Electronics Manufacture & Test, June 1985.

[10] R. W. Franklin, "Surge current testing of resin dipped Tantalum Capacitors", CARTS 1985, p147-154.

[11] J. A. Gill, "Investigation into the effects of connecting Tantalum capacitors in series", AVX.

[12] "Tantalum Capacitors Technical Summary", AVX.

[13] C. Reynolds, "Reliability Management of Tantalum capacitors", AVX.

[14] I. Salisbury, "Thermal Management of Tantalum capacitors", AVX.

[15] I. Salisbury, "Analysis of fusing technology for Tantalum capacitors", AVX.

[16] Panasonic capacitors, "Technical guide of Tantalum electrolytic capacitors", First edition, July 1992, Matsushita/Panasonic capacitors, p38.

[17] "Tantalum Capacitors Technical Summary", AVX.

[18] Hitachi, "TMC series" data sheet, CAT-No. 0502-6209-3KT, p3.

[19] D. Richardson, "Low ESR surface mount solid Tantalum capacitors", CARTS 1994, p93-98.

[20] "Aluminum – und Tantal – Elektrolyte" Kondersatoren Datenbuch 1989/1990, Siemens.

Appendix 1

Self-healing in Tantalum Capacitors

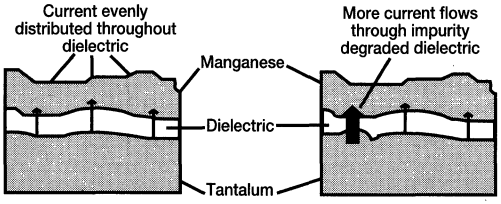


Figure 17. Cross section showing a degraded area.

If there is an area on the Tantalum "slug" (the industries term for an anode) which has a thinner dielectric than the surrounding area, then the larger proportion of the capacitor's current (charging, leakage, etc.) will flow through that site, see Figure 17, thus that area will heat up. If the temperature at the fault site increases to between 400 and 500°C then a reaction [3] takes place which converts the conductive Manganese Dioxide, which has a resistivity of between 1 to 10 Ohm/cm^3, to the less conductive Manganese Oxide (Mn_2O_3) which has a resistivity of between 10^6 - 10^7 Ohm/cm^3. Thus the defective site is effectively "plugged" or "capped", as shown in Figure 18, and the fault site clears.

$$2MnO_2 + \text{Energy} \rightarrow Mn_2O_3 + 1/2\ O_2$$

The oxygen produced is used up by any Tantalum oxides other than Tantalum Pentoxide (Ta_2O_5) present in the capacitors dielectric layer, such as TaO_2 or any Mn O in the cathode coating.

This can also occur at sites where cracks have appeared in the Ta_2O_5 dielectric due to mechanical stress being placed on the component during temperature cycling, due to the different expansion coefficients of the materials used (particularly the resin).

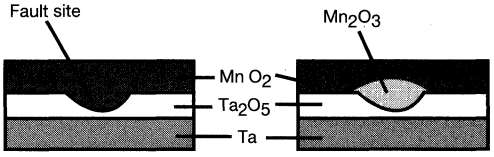


Figure 18. Schematic showing a healed site.

Appendix 2

The development of a surge accelerator and test method.

Because of the low levels of failure being dealt with, a way of accelerating the number of failures which are seen had to be found. The factor known to influence the number of surge failures most is the circuit series resistance. Thus a 'zero' series resistance surge tester was designed for use as the accelerator. The circuit resistance was, of course, not zero, however multi-ganged FETs were used together with thick copper cabling between the power supply and the capacitor under test. The reservior capacitor used was a 10,000µF, 100V low-ESR (<21 mΩ) Aluminum capacitor. In this way the resistance was kept to below 200 mΩ. A circuit schematic is shown in Figure 19.

Relays were not used as the method of switching because of their unreliable nature, and also to cut out any possibility of contact bounce. The FETs were driven hard to ensure a fast turn-on time. The capacitors were tested at their rated voltage. No derating was applied (except where the test condition was to show the effect of derating on a surge performance).

An additional result from the analysis of the data showed that the surge test must be applied 100% to be effective.

Although it has been shown that some batches do suffer more from surge failure than others, it has also been proven that there is capacitor to capacitor variation within a batch. Thus a sampling technique is not really applicable to surge screening. This is particularly true since the number of failures is at the ppm level.

Example: If the fall-out generated for a given batch by surge screening is 100 ppm, the probability of a capacitor failing is 0.0001. If an average batch size is 10000 units, then the number of failures likely in a batch is 1. If each batch is checked by sampling 50 units at random then the probability of catching that failure is 0.005. That is, **the odds on missing faulty units would be 200 to 1.**

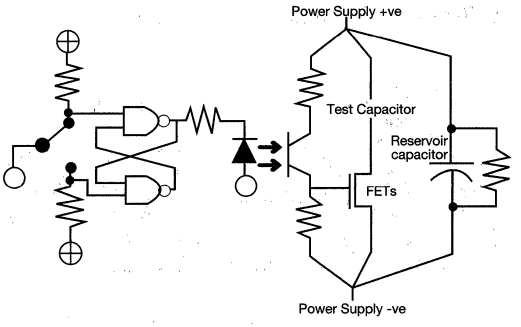


Figure 19. Schematic of the accelerated surge tester.

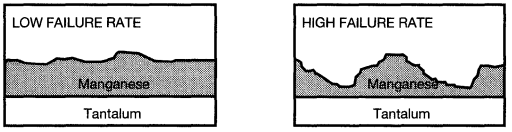
A failure was defined as being a component which exhibited a voltage or current profile which was not the norm or a component which when measured was outside the components limits.

Appendix 3

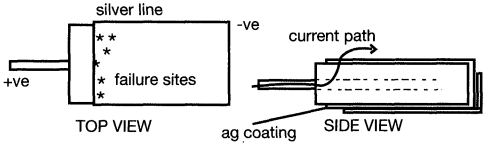
Surge Breakdown in Tantalum Capacitors

a) Manganese

Methodical failure analysis of the surge fallout compared to capacitors which exhibited satisfactory performance revealed a common trend standard in the external manganese dioxide coating of the failed parts. Although the average manganese thickness was consistent over all anode surfaces, these parts typically demonstrated larger variations in the porosity and morphology of the outer layers:



Chemical stripping of the failed parts to expose the dielectric scars indicated a failure location pattern:



The failure sites were noted to be a single point, intense breakdown area coincident with the current flow path of least resistance between the positive termination wire and the external cathode silver coat.

In order to further understand the association of the visual information collected as compared to the occurrence of surge related failures, a possible model was created.

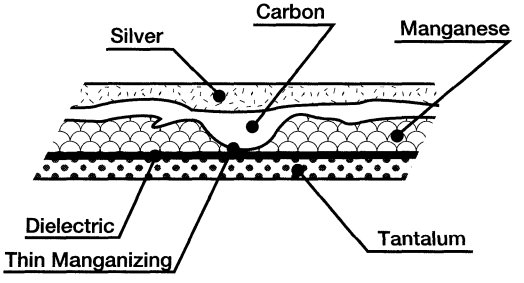


Figure 20.

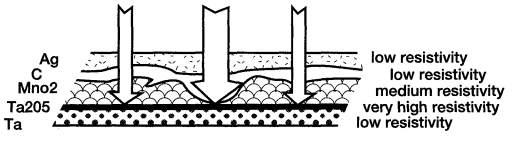


Figure 21.

Figure 20 illustrates an area of thin manganizing on the external body of the Tantalum capacitor, infilled with the higher resistivity coating.

Figure 21 illustrates the uneven current distribution that occurs during a rapid switch-on from a low impedance source. More current will flow locally as indicated by vector B producing a localized "hot spot" as described in Figure 22.

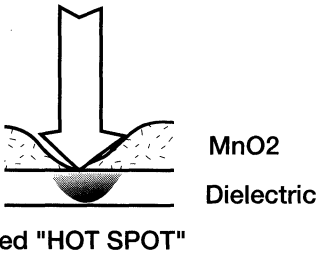


Figure 22.

The intense local current causes an increase in local temperature due to Joule heating at the point of thin manganizing. If this temperature reaches a sufficiently high level, the normally amorphous dielectric will be converted to its crystalline phase and may develop an extremely localized conductive track through the dielectric, at that site. The probability of developing such a site is also proportional to the intrinsic impurity level of the dielectric. In applications where series resistance is incorporated, this can initiate a self healing mechanism. However, if the current availability is unrestricted, then further heating will occur and the area of affected dielectric will increase until catastrophic failure occurs.

(b) Dielectric

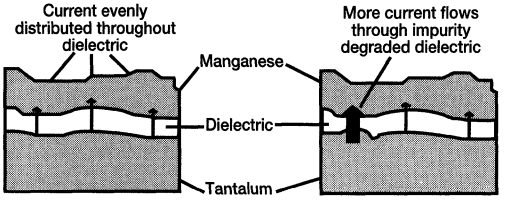


Figure 23. Cross section showing a degraded area.

If there is a degraded area of dielectric (Figure 23), perhaps due to an impurity in the original Tantalum powder used to manufacture the capacitor, and the capacitor is subjected to a rapid charge, more of the current will pass through the degraded area than the neighboring areas of dielectric. This causes the degraded area to heat up.

If the energy has been limited by addition of external

series resistance or sufficient derating has been, the capacitor can self heal, as described previously in Appendix 1. If, however, this is not the case the extreme heat generated causes the Tantalum Pentoxide dielectric layer to change state from the amorphous state to a crystalline state. The crystalline oxide has a lower density than the amorphous oxide, and thus a crack appears in the dielectric.

This allows more current to flow, thus more heat is generated, and more oxide changes to the crystalline form.

The final outcome is that the capacitor becomes a short circuit.

The level of current (or power) then applied to the capacitor determines whether the unit suffers minimal damage, chars or flames. R. W. Franklin's paper on overheating in failed Tantalum capacitors[7] shows that a TAJ surface mount capacitor can withstand 1 Watt with no external damage, but above this level charring will occur.

These areas of thin dielectric and manganese exist in all solid Tantalum capacitors, and their presence does not mean that failures will occur. These features have been observed to be more prevalent in batches giving a higher fall-out on the accelerated surge test machinery used to ensure 100% of AVX product receives a mini-

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