COMMUNICATION ICs

solutions

quality

control

support

confidence

reliability

LEVEL ONE®

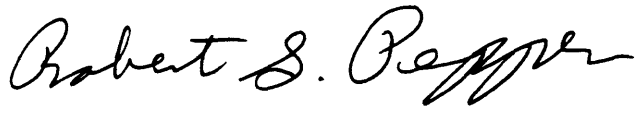
DATA BOOK 1997

THE LEVEL ONE CREDO

OUR MISSION: We shall strive to be the leader in supplying Silicon Connectivity Solutions and to provide a fair return on investment to our shareholders while being a responsible corporate citizen in our community.

OUR QUALITY GOAL: We shall strive to achieve Total Customer Satisfaction.

OUR PLEDGE: We pledge to both external and internal customers that we shall strive to anticipate, understand, and fulfill their needs. We shall continuously improve each of our work functions to enhance the value of our products and services.



Robert S. Pepper, Ph.D.
President and Chief Executive Officer

A leading producer
of mixed-signal Silicon Connectivity Solutions
for high-speed digital communications networks

1997
Data Book

Current Product Information

Here are two ways to obtain the most current product information:

Literature Request Hotline: **(916) 854-1155**
Web Site URL: **http://www.level1.com**

Product Status Indicators

For Level One product documentation, the term "Preliminary Information" has the following meaning:

Preliminary Information: Indicates a product which has not been released to production. Some specifications may be changed or added until full qualification and production release.

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General Information

Providing Silicon Connectivity Solutions for Communications Systems

Background

Level One Communications, Incorporated of Sacramento, California, is a leading supplier of Silicon Connectivity Integrated Circuit (IC) Solutions for complex analog and digital (mixed-signal) transmission and networking applications. The company specializes in the development of integrated circuit Application Specific Standard Products (ASSPs), such as transceivers, repeaters and related devices used in two key areas of the telecommunications and data communications industry. These are:

1. Interface solutions for digital access and transport transmission systems, including fast-growing T1/E1, and
2. Local/Wide Area Networking (LAN and WAN) solutions, including Ethernet LAN, and datacom.

A majority of Level One's products contain complex functions integrated onto a single silicon chip for applications formerly requiring multiple chip or board level solutions.

The company's products target the mixed-signal communications IC market which was estimated to be $4.9 billion in 1995. This market is projected to reach $10.8 billion by 2000, according to VLSI Research.

History & Revenue Growth

Level One was founded in November 1985. The company completed an initial public offering in August, 1993, followed by a secondary offering which was completed in February, 1994. Level One is traded on the Nasdaq exchange under the symbol LEVL. As its name implies, Level One's initial focus was related to the physical layer (layer one) of the Open Systems Interconnection (OSI) seven-layer network reference model developed by the International Standards Organization.

In April 1994, Level One moved from its original Folsom, California location to a new 87,000 square foot facility in Sacramento, California. In April 1996, company operations were expanded with the addition of a 51,000 square foot building in the same industrial park.

During 1995, the company acquired San Francisco Telecom of San Francisco, California, a design firm specializing in system and IC level designs related to SONET/SDH, cable modems, and wireless applications. The company also made an investment in Maker Communications of Waltham, Massachusetts, which specializes in ATM cell processing.

In December 1996, Level One acquired Silicon Design Experts, Inc. (SDE.). This strategic technology acquisition enhances Level One's mixed-signal connectivity expertise with the addition of world class, customizable DSP technology, tools and cores immediately applicable for accelerated development of 1 gigabit Ethernet and other high speed DSP-based communications applications.

Level One achieved 80% annual compound revenue growth for the five year period from 1992 to 1996. The company's revenues were $112 million in 1996, and it has been profitable in each quarter since the first quarter of 1992. Total assets were $112 million at year end 1996.

The Electronic Communications Infrastructure

Level One's advanced Silicon Connectivity Solutions are key building blocks for digitized voice, data and multimedia networks, linking homes and businesses across the nation and around the world. While the telephone and cable TV operating companies in North America today have a total installed plant of 430,000 miles of coaxial cable and 12 million miles of fiber optic cable, there is a total of 1.2 billion miles of copper phone wire in place.

Demand is increasing for mixed-signal Silicon Connectivity Solutions. Level One will continue to leverage the installed base of copper wire to implement the growing number of advanced interactive, multimedia, and enterprise networking applications. These include videoconferencing, Group IV Fax, telecommuting, image retrieval, teleconferencing, wide area connectivity, leased line backup, file transfer, PC access, remote LAN, CAD, CAE, and CAM. Simultaneously, the company has initiated programs to provide solutions which serve the growing needs of the future mixed-media, coax cable, fiber and wireless environments.

New Products

Level One continues to add to its portfolio of more than 60 products by integrating higher layers of the OSI model into its IC functions, such as data transfer/conditioning functions (layer two), as well as network switching, routing and control functions (layer three). Level One's products are aimed directly at the rapidly growing digital telecom/datacom market. These Level One Silicon Connectivity Solutions are essential in an age when new technologies and

customer demands are increasing the need for higher transmission speeds and greater system performance.

As demand increases for higher data transmission speeds—(beyond 64 kilobits per second) to megabit and gigabit levels—Level One continues to implement its product migration strategy by developing mixed-signal devices required at these higher bit rates. The technologies and IC design techniques Level One has perfected for current mixed-signal communication markets are also applicable for the development of solutions addressing broadband coaxial cable or fiber optic transmission environments.

Industry Leadership

Major ingredients of a firm's success can be found in the number of industry leadership positions a company achieves for itself, as well as by the number of industry "firsts" and proprietary products it develops. With a growing list of patents, Level One maintains an extensive research and development program to develop state-of-the-art Silicon Connectivity Solutions for the mixed-signal transmission and networking markets. Level One's R&D program has already yielded significant successes, as evidenced by the following partial list of accomplishments:

Transmission Achievements

- A world leader in twisted-pair telecom/datacom transceivers
- World's first supplier of long-haul T1 transceivers with a one-chip CSU for networking applications
- A complete line of fully integrated T1/E1 short-haul transceivers (Level One is the number one supplier in this market)
- The industry's first fully integrated quad T1/E1 receivers used in the growing SONET multiplexing and T1/E1 test, monitoring and performance market
- Exclusive worldwide provider of integrated Clock Rate Adapters for E1 and T1 interfaces
- The world's only integrated T1 and E1 repeater chips (Level One offers four repeaters: single T1, dual T1, single E1 and dual E1)
- Organized consortium of leading manufacturers to develop chips compliant with the new industry standard for High bit rate Digital Subscriber Line (HDSL) interface at T1 or E1 speeds: our Level One HDSL data pump is the world's most integrated solution
- Level One's new MDSL data pump chip set, introduced in February 1997, delivers high-speed internet access to homes and small business up to ten times faster than today's analog modems at a lower component cost

Networking Achievements

- Developed the world's first fully integrated extended range transceivers for Digital Data Service (DDS)—originally called Dataphone Digital Service by AT&T— and Switched 56 service
- Assisted in the rapid growth of the LAN market with 10BASE-T Ethernet network interface connectivity designs
- Introduced a single-chip Media Attachment Unit (MAU) used to connect to an Ethernet LAN and a hub transceiver for multipoint repeaters. Level One is one of the world's top three 10BASE-T transceiver suppliers (Source: DataQuest)
- Introduced the industry's first Ethernet twisted-pair-to-coaxial cable adapter IC
- The first firm (in 1992) to address the data communications industry's electromagnetic interference needs by integrating transmit filter functions onto a chip
- Developed the first multiport quad hub repeater chip, the LXT914, with integrated transmit filters for 10BASE-T networks
- Introduced the LXT970, one of the industry's first commercially available CMOS, single-chip 10/100 Mbps Ethernet solutions

Unique Design and Modeling/ Simulation Systems

At the heart of Level One's product development effort is a world-class team of silicon designers specializing in mixed-signal communications. This rare breed of IC design engineer is very much in demand among original equipment manufacturers and also among developers of telecom/datacom chip-level components. To assist this team in its R&D pursuits, Level One is using a state-of-the-art Computer Aided Design (CAD) system as well as a proprietary software modeling and simulation system (LxWAVE®). This unique design environment enables Level One to develop fully simulated mixed-signal products quickly, taking the characteristics of target transmission lines into account.

LxWAVE is a very effective proprietary software simulation tool used to model both the physical-level communications system and the associated metallic transmission networks. It is composed of two modules: LxNET® and LxSYS™. LxNET is transmission simulation software used to model dispersion and attenuation of baseband signals for a given set of twisted-pair transmission line characteristics. The LxSYS software module simulates interrelated functional blocks as a system, and models the transceiver's resulting behavior and performance. Together

LxNET and LxSYS accurately predict system-level performance of Silicon Connectivity Solutions in actual transmission networks. These software tools, combined with very powerful automatic test equipment, enable Level One to test its ICs as if they were transmitting in the real world.

Multiple Foundry Strategy

Level One's flexible design methodology utilizes multiple independent wafer foundries to fabricate its integrated circuits. This enables Level One to optimize its manufacturing base to take advantage of process innovations and production schedules. The Company has entered into long-term wafer supply agreements with some of its suppliers.

Quality and Reliability Assurance

Extremely stringent quality and reliability standards are every employee's responsibility. Level One's quality and reliability assurance focus starts at the product definition stage and continues through every aspect of product design, manufacture, testing and customer support.

The company has developed an exacting quality assurance process that has proven successful in reducing failure rates to an absolute minimum for the more than fifteen million ICs produced by the company to date. A rigorous program of wafer foundry and assembly subcontractor selection, audit, qualification and monitoring — as well as internal controls — ensures a consistent supply of high quality and reliable devices.

To qualify to be a Level One wafer foundry or assembly subcontractor, each site must meet an established benchmark performance level. Once qualified, all parties must continue to comply with these benchmarks to maintain Level One's exacting, state-of-the-art manufacturing and production standards.

Low Failure Rates

The success of Level One's quality and reliability assurance program is demonstrated by the company's extremely low failure/return rate. Level One's defect return rate is less than 0.2 percent of annual sales. The average Mean Time Before Failure (MTBF) for Level One's ICs is in excess of 10 million hours.

ISO 9001 Worldwide Registration

In February 1997, Level One achieved registration of its quality management system to the International Organization for Standardization ISO 9001 standard. Registration was granted by Underwriters Laboratories Inc. (UL) under UL's accreditation by Raad voor Accreditatie (RVA), the Dutch Council for Accreditation, and by ANSI-RAB.

ISO 9001 is one of the ISO 9000 series of quality system standards developed by the International Organization for Standardization, a worldwide federation of national standards bodies. The importance of the ISO 9000 movement is being driven by a global marketplace that demands a baseline for verifying the quality systems of suppliers worldwide. ISO 9001 provides a model for quality assurance (and continuous improvement) in Design/Development, Production, Installation and Servicing which focuses on meeting customer requirements.

"Achieving ISO 9001 certification status reinforces Level One's dedication to providing the highest quality products to our customers," said Dr. Robert Pepper, president and CEO, Level One Communications, Incorporated. "ISO certification shows our customers that we are committed to world-class standards while also laying the foundation to manage the continued growth of our company and the growing demand for our products. This is another significant milestone in Level One's growth."

"Our customers include the world's largest telecom and network system providers, who have zero tolerance for error and require extreme confidence in the components they use," said Dan Koellen, vice president, quality and reliability assurance for Level One Communications. "As demand for our products grows, ISO 9001 certification is a reflection of our continued daily commitment to quality and innovation. It is also a recognition of the disciplines and processes we use to manage our business."

Summary

Level One's goal is to become the prime source for the best-performing, highest quality communication IC products. Our goal will be achieved by delivering products on time with strong field sales and application support, and better customer service than any other semiconductor provider in the market. The company is focused on developing the most cost-effective Silicon Connectivity Solutions. To maintain its leadership position, Level One strives to continue to reduce the cost of its products and to provide its customers with higher added-value Silicon Connectivity Solutions.

Quality and Reliability

Designing in Quality

Level One has developed a unique approach to transceiver design and testing. This approach enables us to ensure that all of the devices we manufacture meet performance specifications. We use LxWAVE™, our proprietary simulation tool, to generate analog signals that model transmission through various networks and systems. This enables Level One to test designs and finished devices under simulated conditions to ensure performance to specifications in extremely demanding scenarios.

LxWAVE consists of two simulation tools: LxNET™ and LxSYS™. LxNET starts with a transmission line model using stored transmission line parameters, many of which are actual laboratory measured values. Level One has constructed a wide variety of line models of various gauges , including single and multi-pair bundles. The transmission loop environment can then be modeled by simulating the effect of topology on the transmission network. The topology can include transformers, inductors, capacitors, resistors, active circuitry, bridge taps and other external disturbers. With a given line model, LxNET calculates the response of the loop anywhere along the loop.

LxSYS, the second part of LxWAVE, simulates the behavior of the transceiver in design. To construct the behavior model, LxSYS uses software modules corresponding to circuitry in the Level One design library. Jitter and noise, analog offsets and non-linearities, and bandwidth limitations may also be added.

In the design stage, Level One engineers use LxWAVE to simulate the response of the transceiver for various inputs and under various operating conditions. With these responses, we develop a template defining the range into which the transceiver's output should fall. These templates are saved for later testing.

Designing In Reliability

During design, the reliability aspect of the device is as important to Level One as performance, die size, and yield. Therefore, Level One has established design/layout rules and guidelines aimed at ensuring reliability. These guidelines are followed carefully for all Level One designs; they are updated as required by processing and packaging advances, as well as failure analysis history.

Design and layout guidelines used for Level One designs are intended to ensure reliable circuit operation. Included in the guidelines are rules intended to reduce susceptibility to latch-up, enhance circuit ESD robustness, avoid trace and contact electromigration, ensure dielectric integrity, reduce metal stress, and provide compatibility with packaging. These guidelines are determined in conjunction with the wafer foundries to guarantee compatibility with their processes. Packaging and assembly related guidelines are developed with the assembly house to enhance package reliability and die protection.

In addition, Level One designs are conservative. Chip components are not designed to the limits of process capabilities or operated under conditions that could lead to instability. Designs are subjected to in-depth circuit simulation at temperature, voltage and processing extremes before being committed to silicon. In order to guarantee operation at these extremes, circuit designs must be conservative.

Level One devices are designed for fabrication at more than one targeted foundry. The processes used by these different foundries are similar, but not identical. Therefore, our designs must be able to encompass the process differences between foundries. This results in devices less sensitive to variations that may occur during processing or during the life of the device.

Foundry and Assembly House Selection and Qualification

The process of choosing and qualifying a wafer foundry or an assembly house starts long before any product is built at the facility. Each subcontractor is studied in detail by a team consisting of representatives from quality and reliabilty, operations, production, and design. This ensures compatibility with Level One requirements.

Factors examined at an assembly house include: package capabilities, attach types, temperature profiles, mold compound and epoxy types, inspections, process control, moisture sensitivity, and quality procedures.

Foundries are evaluated for their ability to produce Level One designs. The foundry's device models or Level One generated models are used to determine the foundry's compatibility. Extensive simulation is performed at process,

voltage and temperature extremes to ensure circuit functionality. The process flow and construction topology are evaluated for top coat effectiveness, glassivation and metallization step coverages, effectiveness of planarization, electromigration performance, etc. Reliability data is evaluated for compliance with Level One reliability requirements.

The manufacturing and quality procedures followed by the foundry are evaluated carefully to be sure they can control the process to Level One specifications. Also, complete lot traceability must be retained.

Finally, both the foundry and the assembly house must be committed to constant quality improvement through the use of control charts, quality groups, and corrective/preventive actions on anomalies reported by customers. Currently, the company has qualified foundries in North America, Europe and Asia. Multiple foundries reduce the risks associated with dependency on a single vendor.

Level One assembly in plastic DIP, PLCC, TQFP and PQFP packages is currently being handled by assembly houses in Asia and the USA.

Level One product is used to assess the capability of the subcontractor to meet Level One requirements through product verification, characterization, and reliability qualification.

Subcontractor Control

Subcontractor control is important to ensure consistent performance. Control is a continuous process, accomplished through a multifaceted approach. Subcontractor surveillance is an important part of the Level One standard product flow. Electrical measurements of basic transistor and topology structures are examined for each wafer lot received. Each incoming packaged device lot is subjected to material verification and QC monitor report review. In addition, incoming wafers and packaged devices are visually inspected on a sample basis. Any anomalies or trends are detected and reported early in the process.

A team consisting of quality engineering, operations, and purchasing monitors the performance of the subcontractor. This team meets with the subcontractor periodically to evaluate performance. In addition, this team maintains continuous contact with the subcontractor to ensure a good working relationship. The subcontractor's performance is monitored by evaluating the results of subcontractor surveillance, product monitor, quick reaction quality and reliability monitor, and process capability index reports.

Periodically, Level One audits foundry and assembly house process monitor and control procedures, quality and reliability monitoring, incoming material quality assurance, and process capability indexes.

Product Reliability Qualification

Level One products must undergo a strenuous reliability qualification procedure before production shipments begin. Product reliability qualification includes: establishment of functional and parametric test procedures; reliability qualification of the device; reliability qualification of the process to be used; and reliability qualification of the package.

A device built using a new foundry or a new assembly house must undergo the most encompassing reliability qualification procedure. Because subsets of the reliability qualification procedure are specific to foundry processes and packages, products using pre-qualified processes or packages require qualification only of the portions of the procedure not satisfied by prior qualification. Every qualified product is capable of meeting each applicable reliability qualification requirement.

Among the tests and stresses included in the reliability qualification procedure are the following:

- operating life tests
- Temperature Humidity Bias (THB)
  85 °C/85% RH or 130 °C/85% RH
- autoclave
- temperature cycling
- thermal shock
- latch-up immunity
- ESD susceptibility
- package and lead mechanical integrity
- moisture sensitivity evaluation

Such comprehensive testing stresses the device design, process and package. For example, operating life tests stress the device with bias (in a static or dynamic mode) at elevated temperatures to accelerate possible failure mechanisms that could occur during the life of the device. Failure mechanisms accelerated during life testing include parameter shifts, leakages, electromigration and oxide defects. These failure mechanisms have been thoroughly studied, and found to follow the Arrhenius relationship for reaction rate acceleration with temperature. This enables Level One to simulate life at a nominal operating temperature in a relatively short time.

Autoclave and THB tests are used to evaluate the resistance to moisture of devices packaged in plastic. The ability of the package to protect the die is evaluated in autoclave, in an unbiased, high temperature, pressurized steam environment. Metallization corrosion is the dominant failure mechanism. Bias-dependent moisture effects are enhanced through THB, which is a humid (85% RH), high temperature (85 °C or 130 °C) environment. Failure mechanisms include metallization corrosion, leakages and voltage shifts. The package, process, and circuit design are all stressed with THB.

Package and bond integrity are evaluated using temperature cycling, thermal shock, and package and lead mechanical testing. Level One also evaluates the moisture sensitivity of surface mount devices according to JEDEC and IPC standards.

Destructive physical analysis (DPA) is used to evaluate the details of construction, workmanship, and potential reliability. In this analysis, the package and/or die is dissected and examined in detail, using X-ray, optical microscopy, and scanning electron microscopy. Items such as bond wire dress, ball formation, die attach, lead frame, package or mold compound, passivation integrity, die construction and workmanship are analyzed.

Product Monitoring

After a product is qualified, Level One's product monitoring program continues to verify quality and long-term reliability. Under this program, the Quality and Reliability Department takes periodic samples of the product from finished goods and subjects them to selected product qualification tests. Process related tests are performed on a quarterly basis. Each process/foundry used in production is monitored separately. Package reliability testing is performed biannually-annually. Each production package type/assembly is monitored individually.

The results of the reliability testing performed for the product monitoring program are published in Level One Reliability Reports.

An important area of product monitoring is reviewing failure history for indications of process or assembly anomalies. If trends are seen, the anomaly is identified through failure analysis, pinpointing possible process or assembly influences. Level One then implements corrective actions, working with the foundry or assembly house. Design rules and guidelines are modified, if necessary, to prevent future recurrence of the failure mechanism.

Quick Reaction Quality and Reliability Monitor $(QR)^2M$

Assembled devices are monitored monthly in the $(QR)^2M$ using tests of short duration. These tests include solderability, x-ray, ball shear, physical dimensions, autoclave, and others. These tests provide insight into the performance of the subcontractors' processes. The key points of the program are to provide quick feedback, to enable quick detection of trends, and to establish a baseline for each processes' capability.

Production Flow

The Level One production flow is shown in Figure 1. Level One participates in quality and reliability monitoring through each aspect of the production cycle by reviewing electrical and inspection data from the foundry and assembly house. All device testing and lot certification, as well as wafer and package inspections, are performed by Level One and certified subcontractors.

With each wafer lot, the foundry sends results of electrical measurements of basic transistor and topology structures. These measurements are reviewed and compared to specified values for the process. If the deviation falls outside the specification limits, the material is held by the foundry until disposition by Level One. Feedback to the foundry is immediate, and a mutually-agreed-upon corrective action plan is executed.

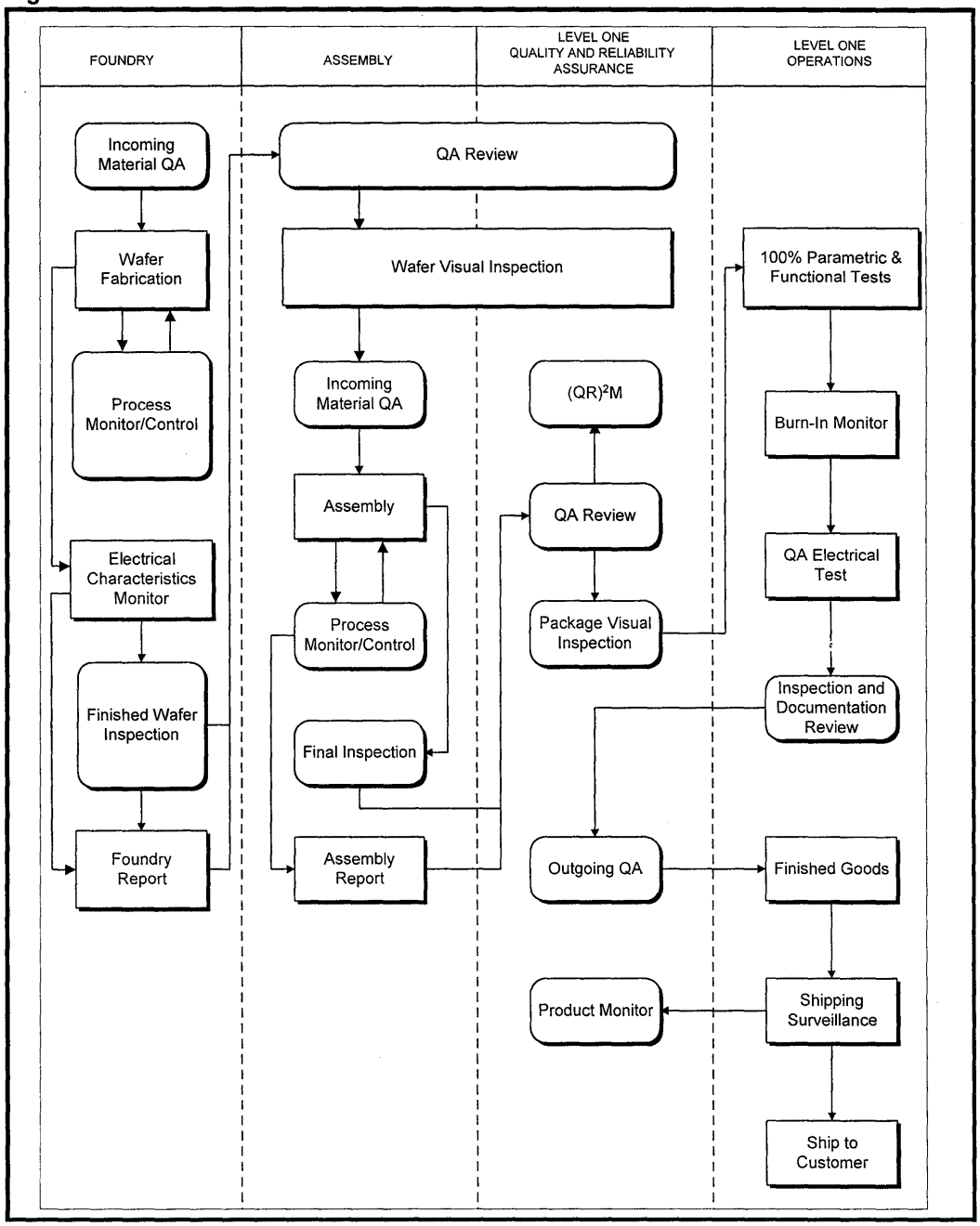
A similar inspection and QC monitoring report is received with each assembled lot from the assembly house. This report is reviewed for each incoming lot.

Before disposition to finished goods, the lot traveler is reviewed by Quality Assurance to ensure that all test, inspection and production steps have been performed.

A sample of the product must pass a rigorous quality acceptance test before authorization to ship is given. Upon successful completion of this test, authorization to ship is given by Quality Assurance.

By maintaining close working relationships with the foundries and assembly houses, Level One is involved throughout the production of the product.

Figure 1: Level One Production Flow



Testing

The test development effort starts at the first stages of design to ensure that the device will be able to be tested completely. This may include special requirements on the design to maximize test effectiveness.

All devices are 100% tested using parametric and functional tests using analog waveforms and digital test vectors. Test vectors are downloaded to the production tester for incorporation into test programs. The analog and digital signals transmitted through various networks are reconstructed by the tester and used as stimuli to the device under test (DUT). Noise can be added to further evaluate the device's response under less than optimum operating conditions. The response is sampled by the tester and compared to the template constructed for the particular input stimulus. Using the reconstructed waveforms, the DUT is also tested for response to various line lengths and superimposed noise amplitudes.

These dynamic functional tests, combined with parametric tests, ensure that the devices are rigorously tested under various operating conditions without the use of cable spools or other hardware.

Product Traceability

To ensure traceability, each lot traveler tracks the product history as follows: foundry lot, assembly, inspections, tests, burn-in monitor, quality control and quality acceptance testing, and shipping destination. This documentation is retained for future reference. The lot traveler enables Level One to determine which lots were shipped to a particular customer. In addition, each device is branded with the lot number and a special trace code to enable complete traceability. The trace code identifies the wafer foundry, assembly, and die revision immediately by inspection.

Electrostatic Discharge

Electrostatic discharge (ESD) can damage sensitive semiconductor devices. Damage occurs unless precautions are taken to eliminate the generation of dangerous static levels, and to design robust circuitry with sufficient protection. Level One uses both approaches to ensure that the devices shipped to our customers are not compromised, and that they will survive industry accepted handling for semiconductor devices.

Level One's design guidelines for ESD protection produce devices which tolerate nominal ESD levels without damage. Before use in device designs, we test the susceptibility to ESD damage of standard input and output cells. In addition, the ESD susceptibility of each device type is determined as part of the product qualification before release to production.

Proper ESD handling of devices is policy at Level One. Those who handle devices are fully trained in the proper procedures for handling static-sensitive devices and know that handling devices incorrectly may damage them. Packaged devices are handled only at special workstations designed to eliminate damaging static levels. All equipment used in the handling of devices is designed to ensure damaging static levels are not present. Packaged devices are shipped in containers designed to eliminate risk of damage caused by ESD.

Constant Improvement Program

To assure shipment of high-quality, highly reliable devices, Level One pursues constant improvement in all aspects of production and testing. Small group problem-solving teams have been assembled. The teams consist of personnel from both operations and quality, working together to solve problems and improve our manufacturing flow.

Periodic quality system reviews examine the effectiveness of internal Level One quality, manufacturing, and product development systems. Recommendations for improvement are made to and approved by Level One senior management.

Level One Telecom Product Reference Guide

APPLICATIONS	PRODUCT FAMILY	PART NUMBER	COMMENTS
Test Equipment Line Monitors Line Interface	*Quad Receiver*	**LXT325**	• Industry's first quad receiver • Incorporates four independent receivers in 28-pin DIP or PLCC • Sensitivity allows for up to 20 dB of jack/cable attenuation • Includes loss of signal indication output for each receiver
Access Systems • MUXes • PBXs • DSUs • CSUs • Routers • Concentrators • Bridges • PCs • Video Conferencing • Channel Extenders	*Short-Haul T1/E1 Transceivers*	**LXT300Z**	• Constant output impedance independent of marks and spaces • Low power consumption (400 mW typ.) • Enhanced DPM monitor detects single line shorts • Output tristate capability • Pulse amplitude stabilization • Includes receive Jitter Attenuation starting at 3 Hz
		LXT301Z	• Similar to LXT300Z without Jitter Attenuator • Meets BABT E1 short circuit limit of 50 mA with ext. resistors
Transport Systems • Channel Banks • Digital Cross-Connects • Trunk Cards for C.O.s and PBXs • DLC Systems • PDH/SDH MUXes		**LXT304A**	• Includes receive Jitter Attenuation starting at 3 Hz • Low power consumption of 400 mW max • Constant low output impedance driver for high return loss • Meets new ETSI TBR 12 standard on output jitter • Low receive clock quantization jitter of $< 1/16$ U.I. • Analog/Digital LOS processor meets G.775 • Programmable Transmit Return LOS using ext. resistors • Output driver tristate capability

Level One Telecom Product Reference Guide

APPLICATIONS	PRODUCT FAMILY	PART NUMBER	COMMENTS
Access Systems • MUXes • PBXs • DSUs • CSUs • Routers • Concentrators • Bridges • PCs • Video Conferencing • Channel Extenders **Transport Systems** • Channel Bank • Digital Cross-Connects • Trunk Cards for C.O.s and PBXs • DLC Systems • PDH/SDH MUXes	*Short-Haul T1/E1 Transceivers*	**LXT305A**	• Includes Transmit Jitter Attenuation starting at 3 Hz • Low power consumption of 400 mW max • Constant low output impedance driver for high return loss • Meets new ETSI TBR-12 standard on output jitter • Low receive clock duty cycle variation • Low intrinsic receive clock quantization jitter • 32-bit FIFO accommodates up to 28 U.I. of gapped clocks without overflow • Output driver tristate capability • Analog/Digital LOS processor meets G.775 • Meets BABT E1 short circuit limit of 50 mA with ext. resistors
		LXT307	• E1 only transceiver without jitter attenuation • Analog/Digital processor meets G.775 • Meets BABT short circuit limit of 50 mA with ext. resistors • 75/120Ω operation without component changes • Low 2.048 MHz reference clock • Constant low output impedance driver for high return loss • Low receive clock duty cycle variation • Output driver tristate capability

Level One Telecom Product Reference Guide

APPLICATIONS	PRODUCT FAMILY	PART NUMBER	COMMENTS
Access Systems • MUXes • PBXs • DSUs • CSUs • Routers • Concentrators • Bridges • PCs • Video Conferencing • Channel Extenders **Transport Systems** • Channel Banks • Digital Cross-Connects • Trunk Cards for C.O. and PBXs • DLC Systems • PDH/SDH MUXes	*Short-Haul T1/E1 Transceivers*	**LXT331**	• Single chip dual T1 transceiver • High transmit and receive return loss • Complete line driver and data recovery functions • Meets industry specifications including ITU G.703, ANSI T1.403 and AT&T Pub 62411
		LXT332	• Single chip dual T1/E1 transceiver • Tx/Rx switchable crystal-less Jitter Attenuator • On-chip driver short circuit monitoring (DFM) • On-chip encoder/decoder • QRSS detector/generator • AIS/BPV insert and detect • Software switchable between T1 and E1 operation • Low-frequency reference clock (1.544 or 2.048 MHz)
		LXT334	• Quad E1 transceiver • Low power consumption of 410 mW • On-chip HDB3 and AMI encoder/decoders, and clock recovery function • Independent Loss of Signal processor for each channel conforms to ITU G.775 recommendation • Line driver patent pending
		LXT335	• Quad E1 analog interface • Low power consumption of 410 mW • Simple design for use with integrated digital back-end circuits
		LXT350	• Single channel version of LXT332 • Serial microprocessor control port
		LXT351	• Single channel version of LXT332 • 8-bit parallel microprocessor control port

Level One Telecom Product Reference Guide

APPLICATIONS	PRODUCT FAMILY	PART NUMBER	COMMENTS
Access Systems • Network Access • ISDN-PRIs • CSUs • NTUs **Transport Systems** • Office Repeaters • Cellular Bays • Base Station Networking	*Long-Haul T1 Transceiver*	**LXT310**	• Industry's first fully compliant T1 CSU/ISDN transceiver • Operates over 6,000 feet of Twisted-Pair cable
	Long-Haul DECT Transceiver	**LXT317**	• Fully integrated Long-Haul transceiver @ 1.152 Mbit/s • Operates over 3.5 km of 0.6mm cable • Optimized to address Digital European Cordless Telecommunications (DECT) and Personal Communications Service (PCS) standards
	Long-Haul E1 Transceiver	**LXT318**	• Similar to LXT310, used in E1 applications • Fully compliant with ITU-T specifications for E1 Short-Haul (6dB) or Long-Haul (43dB) applications • Meets new ETSI TBR 12/13 standard on output jitter
	Short-Haul/ Long-Haul T1/E1 Transceiver	**LXT360/ LXT361**	• T1/E1 Short-Haul and Long-Haul transceiver • Software programmable T1/E1 operation • On-chip QRSS, BPV and AIS generator/ detector • Analog/Digital LOS processor meets G.775 • Crystal-less Jitter Attenuator • Serial (LXT360) and parallel (LXT361) control port
T1/E1 Repeaters • Line Repeaters • Office Repeaters • Test and Monitor Equipment	*T1 Repeaters*	**LXT312**	• Industry's only fully integrated Dual T1 repeater • Requires only a crystal and a few other components to complete a repeater design • No tuning coil required • Low power consumption • 0 to 36 dB dynamic range
		LXT315	• Single version of LXT312
	E1 Repeaters	**LXT313**	• Industry's only fully integrated Dual T1 repeater • Requires only a crystal and a few other components to complete a repeater design • No tuning coil required • Low power consumption • 0 to 43 dB dynamic range
		LXT316	• Single version of LXT313

Level One Telecom Product Reference Guide

APPLICATIONS	PRODUCT FAMILY	PART NUMBER	COMMENTS
Frame Relay DDS and SW/56 DSU's • Leased-line DDS • Internet Service Provider (ISP) Equipment • Frame Relay Access Devices (FRAD)	*DDS/ Switched 56 Transceivers*	**LXT400**	• Fully integrated all-rate extended range transceiver • Receive equalizer filter can handle up to 40 dB at rates below 56 kbps, and up to 49 dB at 56 kbps and 72 kbps
		LXT441	• Single-chip Digital Modem for 56/64 kbps DSUs • Allows direct connection between serial port and analog leased lines
Access Systems • PBXs • NTUs • CSUs **Transport Systems** • DACs • Office Repeater Bays • Mobile Switches	*Low Jitter T1/E1 Clock Rate Adapters*	**LXP600A**	• Industry's first Clock Adapter (CLAD) for use as internal system timing generator • Converts between T1 and E1 • Patented locking method enables frequency conversion with no external devices • Meets AT&T 62411 and ITU-T G.732 jitter specs when teamed with Level One transceivers • Provides 6 MHz High Frequency Output (HFO)
		LXP602	• Similar to LXP600A, with 8 MHz HFO
		LXP604	• Converts between 1.544 MHz and 4.096 MHz, with 6 and 8 MHz HFO
		LXP610	• Multi-rate Clock Adapter • Pin-selectable frequency conversion between 11 different rates (1.544 MHz to 8 MHz) • Accepts seven CLK1 input frequencies and provides five HFO output frequencies
PDH MUX • E1, E2, E3 multiplexers • T1 multiplexing (point to point applications)	*PDH Multiplexers*	**SXT6234**	• Performs four-E1 to E2 or four-E2 to E3 multiplexing • Compliant with ITU-T G742 and G.751 recommendations • Usable for four T1 multiplexing • Optimized for microwave radio

Level One Telecom Product Reference Guide

APPLICATIONS	PRODUCT FAMILY	PART NUMBER	COMMENTS
HDSL • T1 or E1 (2-pair) and fractional T1 or E1 transport • Digital pair-gain • Wireless base stations to switch interfaces • Campus and private networking • High-speed digital modems	*High Bit Rate Digital Subscriber Line (HDSL) Products*	**SK70704/ SK70706**	• HDSL chip set for 784 kbps data transmission • Fully-integrated analog core chip • Integrated activation/start-up • Optimized for one-pair operation
		SK70704/ SK70707/ SK70708	• HDSL chip set for 1168 kbps data transmission • Fully-integrated analog core chip • Integrated activation/start-up • Optimized for one-pair operation
		LXP710 Advance Information	• HDSL framer/mapper • Compliant with ETSI ETR-152 requirements • E1 to HDSL loop multiplexing/ demultiplexing • HDSL overhead management • DPLL for E1 timing recovery • HDSL transmit stuffing control
Multi-Rate DSL • High speed residential Internet access • Extended range fractional T1/E1 transport • 4, 6, 8 or 12-channel digital pair-gain • Wireless base station to switch access • WAN access for LAN routers	*Multi-Rate Digital Subscriber Line (MDSL) Products*	**SK70720/ SK70721**	• Chip set configurable to 272, 400, 528, and 784 kbps data transmission • Fully integrated analog core chip • Supports transparent repeater applications without an external processor or glue-logic • Supports processor directed rate selection driven by receive signal level and noise margin • Continuously adaptive echo canceller and equalizers perform to changing noise and line characteristics

Level One Networking Product Reference Guide

APPLICATIONS	PART NUMBER	FEATURES
Wide Area Networking		
T1/E1 Repeaters • Line Repeaters • Office Repeaters • Test and Monitor Equipment	**LXT312**	• Industry's only fully integrated Dual T1 repeater • Requires only a crystal and a few other components to complete a repeater design • No tuning coil required • Low power consumption • 0 to 36 dB dynamic range
	LXT315	• Single version of LXT312
	LXT313	• Industry's only fully integrated Dual E1 repeater • Requires only a crystal and a few other components to complete a repeater design • No tuning coil required • Low power consumption • 0 to 43 dB dynamic range
	LXT316	• Single version of LXT313
Frame Relay DDS and SW/56 DSU's • Leased-line DDS • Internet Service Provider (ISP) Equipment • Frame Relay Access Devices (FRAD)	**LXT400**	• Fully integrated all-rate extended range transceiver • Receive equalizer filter can handle up to 40 dB at rates below 56 kbps, and up to 49 dB at 56 kbps and 72 kbps
	LXT441	• Single-chip Digital Modem for 56/64 kbps DSUs • Allows direct connection between serial port and analog leased lines
Specialty Ethernet Transceivers		
Ethernet Twisted-Pair MAUs • External AUI to TP Transceivers • Internal MAUs	**LXT902**	• Six LED drivers for diagnostics and status reporting • Full-duplex capability • Signal Quality Error (SQE) can be disabled for hub and switch applications • Automatic AUI/RJ45 selection for internal MAU applications
Ethernet Twisted-Pair to Coax Adapters • BNC-TP External Converters	**LXT906**	• Industry exclusive • Direct interface to coax Ethernet transceiver and RJ45 Twisted-Pair connector • Level shifted data pass-through • Collision detection / correction • Reversed polarity detection/ correction • LED drivers for Tx, Rx, collision, reversed polarity and link functions

Level One Networking Product Reference Guide

APPLICATIONS	PART NUMBER	FEATURES
10 Mbps Ethernet Transceivers		
Ethernet Interface Adapter (Universal) • Computer/Laptop/Workstation Interface Boards • LAN Repeaters • Printer Network Attachments • PCMCIA LAN Cards • Workstation/Graphic Terminals • PC-PC Servers (Adapter/ Motherboard) • 10BASE-T Interconnects (MAU) • Bridges/Routers • Terminal Servers • Point-Of-Sale Interfaces • Switching Networks	**LXT901A/ LXT907A**	• Integrated filters • Provides all active circuitry for interfacing 802.3 controllers to an Attachment Unit Interface (AUI) or 10BASE-T media • Integrated Manchester encoder/decoder, reversed polarity detection/correction • LED drivers • Full duplex capability • Power Down Mode • Four Loopback Modes • Selectable termination impedance for use with shielded or unshielded twisted-pair (*LXT901A Only*) • Signal Quality Error (SQE) Disable function for hub and switch applications (*LXT907A Only*)
Ethernet Interface Adapter (AUI) • Bridges, Routers • LAN-to-WAN access equipment	**LXT904**	• Provides all active circuitry for interfacing 802.3 controllers to an Attachment Unit Interface (AUI) • Manchester encoder/ decoder • LED drivers • Full duplex capability
Ethernet Interface Adapter (10BASE-T) • Portable computers • PDAs • Switching Hubs • Printer Adapter Cards • PCMCIA Cards	**LXT905**	• 3.3V or 5V operation • Power down mode for battery operation • Provides all active circuitry for interfacing 802.3 controllers to a 10BASE-T media • Includes Manchester Encoder/ decoder, reversed polarity detection/correction, integrated filters • LED drivers • Full duplex capability • Signal Quality Error (SQE) can be disabled for hub & switch applications
Ethernet Interface Adapter (Universal) • 10BASE-T Hub and Switching products • 10BASE-T LAN adapter boards for computers/workstations	**LXT908**	• Improved Filters - Simplifies FCC Compliance • Single 3.3V or 5V operation • Integrated Manchester Encoder/Decoder • 10BASE-T compliant Transceiver • AUI Transceiver • Supports Standard and Full-Duplex Ethernet • Automatic/Manual AUI/RJ45 Selection • Automatic Polarity Correction • SQE Disable/Enable function • Power Down Mode with tristated outputs • Four loopback modes • Four LED Drivers

Level One Networking Product Reference Guide

APPLICATIONS	PART NUMBER	FEATURES
Universal Quad Ethernet Interface Adapter • Ethernet Switches • Multiport File Servers and Print Servers	**LXT944**	• Four independent 10BASE-T transceivers with integrated filter, Manchester encoder/decoders • Four LED drivers per port • Full duplex capability on each port • Signal Quality Error (SQE) can be disabled for hub and switch applications
Fast Ethernet Transceivers		
Fast Ethernet Transceiver • 10/100 Network Interface Cards (NICs) • 10/100 Switches • 10/100 Repeaters • 100BASE-FX NICs, Switches and Repeaters	**LXT970**	• IEEE 802.3-compliant 10BASE-T and 100BASE-TX using a single RJ45 connection • Baseline wander correction • 100BASE-FX fiber optic capable • Standard CSMA/CD or full duplex operation at 10 or 100 Mbps • Supports both Auto-Negotiation and parallel detection for legacy 10BASE-T or 100BASE-TX systems • LED drivers • MII interface with extended register capability • Configurable for DTE, repeater or switch applications • Encoder bypass for symbol mode applications • Exceptional performance on long line lengths
Fast Ethernet Quad Transceiver • 10BASE-T, 10/100-TX, or 100BASE-FX Switches • 10BASE-T, 10/100-TX, or 100BASE-FX Repeaters	**LXT974 Advance Information**	• Four independent IEEE 802.3-compliant 10BASE-T or 100BASE-TX ports in a single chip • 100BASE-FX fiber optic capable • Standard CSMA/CD or full duplex operation at 10 or 100 Mbps • Compliant with IEEE 802.3u auto-negotiation protocol and with legacy 10BASE-T and 100BASE-T systems without auto-negotiation capability • On-chip transmit and receive filtering for 10BASE-T and 100BASE-TX • Baseline wander correction • Configurable on-chip LED drivers as well as serial LED output • Super MII Interface Mode for reducing customer ASIC pin requirements. • Configurable through MII serial port or via external control pins

Level One Networking Product Reference Guide

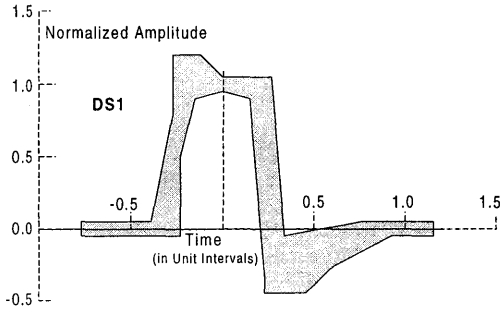
APPLICATIONS	PART NUMBER	FEATURES
Ethernet Repeaters		
Managed Repeaters • Stackable and stand-alone workgroup hubs • Embedded Applications • Print Servers • Multi-port routers • Remote Access SOHOs	**LXT914**	• Four 10BASE-T ports • Reversible AUI port • Configuration/status interface • 4 LED modes • Cascadeable backplane (no glue logic required) • Integrated filters • Programmable squelch
LED Managed Or Unmanaged Repeaters • "Personal" hubs • Stackable and stand-alone workgroup hubs • Embedded Applications – Multi-port Routers – Print Servers	**LXT915**	• Four 10BASE-T ports • Simple AUI port • 4 LED modes • Cascadeable backplane (no glue logic required) • Integrated filters • Programmable squelch
RMON Managed Repeaters • Stackable/Modular Workgroups • Embedded Applications – Multi-port – File Server	**LXT916/ LXT917**	• Eight 10BASE-Tports (*LXT916*) Twelve 10BASE-T ports (*LXT917*) • Supports RMON and the repeater MIB • High speed serial management interface • Cascadeable backplane improved for stackability • 7-pin MAC interface • Reversible AUI port (DTE/MAU) • Two address-tracking registers per port • Integrated filters • Activity, collision and per-port status LEDs
Hybrid Repeater/Switches • Next generation port-switching applications	**LXT918**	• Four independent 10Mb Ethernet Repeaters • Twelve 10BASE-T ports • Reversible AUI port (DTE/MAU) • Internal switch allows the external ports to be switched to any repeater segment • When a port is switched to a new segment, its counters will follow • Per-segment and per-port support for RMON and the repeater MIB • High speed serial management interface • 7-pin "roaming" MAC interface • Cascadeable backplane • Two address-tracking registers per port • Integrated filters • Activity, collision and per-port status LEDs

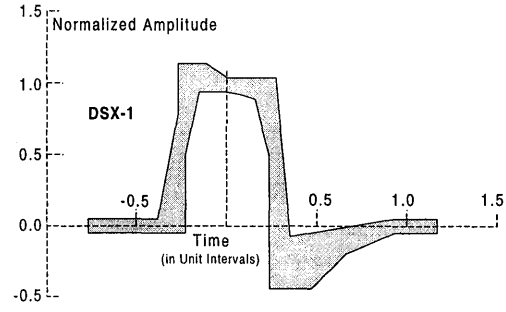
2

T1/E1 Short-Haul Transceivers and Receivers

and General Specifications

1.544 Mbps Pulse Mask (DS1 and DSX-1)

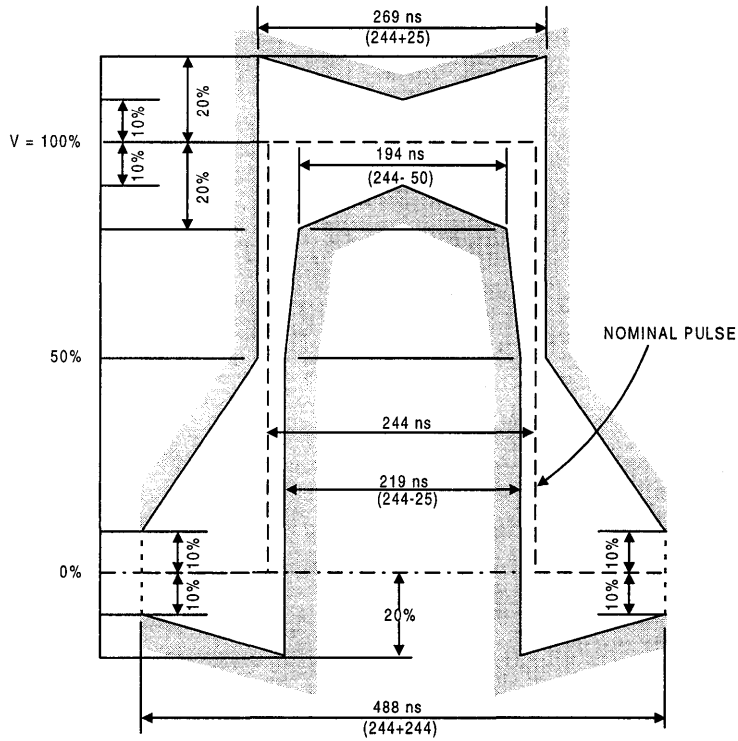




1.544 MHz T1 Pulse Mask Corner Point Specifications

DS1 Template *(per ANSI T1. 403-1995)*				**DSX-1 Template** *(per ANSI T1. 102-1993)*			
Minimum Curve		**Maximum Curve**		**Minimum Curve**		**Maximum Curve**	
Time *(UI)*	**Amplitude**	**Time** *(UI)*	**Amplitude**	**Time** *(UI)*	**Amplitude**	**Time** *(UI)*	**Amplitude**
-0.77	-0.05	-0.77	0.05	-0.77	-0.05	-0.77	0.05
-0.23	-0.05	-0.39	0.05	-0.23	-0.05	-0.39	0.05
-0.23	0.50	-0.27	0.80	-0.23	0.50	-0.27	0.80
-0.15	0.90	-0.27	1.20	-0.15	0.95	-0.27	1.15
0.0	0.95	-0.12	1.20	0.0	0.95	-0.12	1.15
0.15	0.90	0.0	1.05	0.15	0.90	0.0	1.05
0.23	0.50	0.27	1.05	0.23	0.50	0.27	1.05
0.23	-0.45	0.34	-0.05	0.23	-0.45	0.35	-0.07
0.46	-0.45	0.77	0.05	0.46	-0.45	0.93	0.05
0.61	-0.26	1.16	0.05	0.66	-0.20	1.16	0.05
0.93	-0.05			0.93	-0.05		
1.16	-0.05			1.16	-0.05		

2.048 Mbps E1 Pulse Mask



2.048 MHz E1 Pulse Mask Specifications

Parameter	TWP	Coax	Unit
Test load impedance	120	75	Ω
Nominal peak mark voltage	3.0	2.37	V
Nominal peak space voltage	0 ±0.30	0 ±0.237	V
Nominal pulse width	244	244	ns
Ratio of positive and negative pulse amplitudes at center of pulse	95-105	95-105	%
Ratio of positive and negative pulse amplitudes at nominal half amplitude	95-105	95-105	%

LXT300Z/LXT301Z

Advanced T1/E1 Short-Haul Transceivers

General Description

The LXT300Z and LXT301Z are fully integrated transceivers for both North American 1.544 Mbps (T1) and International 2.048 Mbps (E1) applications. They are pin and functionally compatible with standard LXT300/301 devices, with some circuit enhancements.

The LXT300Z provides receive jitter attenuation starting at 3 Hz, and is microprocessor controllable through a serial interface. The LXT301Z is pin compatible, but does not provide jitter attenuation or a serial interface. An advanced transmit driver architecture provides constant low output impedance for both marks and spaces, for improved Bit Error Rate performance over various cable network configurations. Both transceivers offer a variety of diagnostic features including transmit and receive monitoring. Clock inputs may be derived from an on-chip crystal oscillator or from digital inputs. They use an advanced double-poly, double-metal CMOS process and require only a single 5-volt power supply.

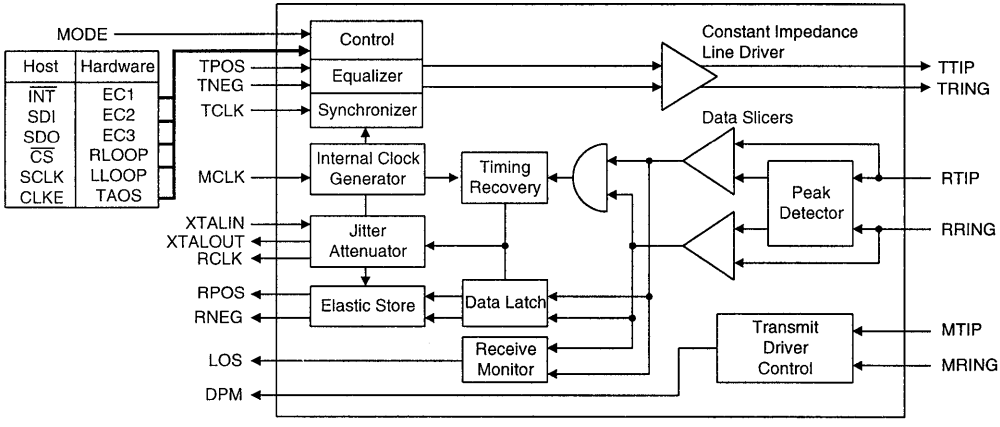
Applications

- PCM/Voice Channel Banks
- Data Channel Bank/Concentrator
- T1/E1 multiplexer
- Digital Access and Cross-connect Systems (DACS)
- Computer to PBX interface (CPI & DMI)
- High-speed data transmission lines
- Interfacing Customer Premises Equipment to a CSU
- Digital Loop Carrier (DLC) terminals

Features

- Data recovery and clock recovery functions
- Receive jitter attenuation starting at 3 Hz exceeds AT&T Pub 62411, Pub 43801, Pub 43802, ITU G.703, and ITU G.823 (LXT300Z only)
- Line driver with constant low mark and space impedance (3 Ω typical)
- Minimum receive signal of 500 mV
- Adaptive and selectable (E1/DSX-1) slicer levels for improved SNR
- Programmable transmit equalizer shapes pulses to meet DSX-1 pulse template from 0 to 655 ft
- Local and remote loopback functions
- Digital Transmit Driver Monitor
- Digital Receive Monitor with Loss of Signal (LOS) output and first mark reset
- Receiver jitter tolerance 0.4 UI from 40 kHz to 100 kHz
- Microprocessor controllable (LXT300Z only)
- Compatible with most popular PCM framers
- Available in 28-pin DIP or PLCC

LXT300Z Block Diagram



PIN ASSIGNMENTS & SIGNAL DESCRIPTIONS

Figure 1: Pin Assignments

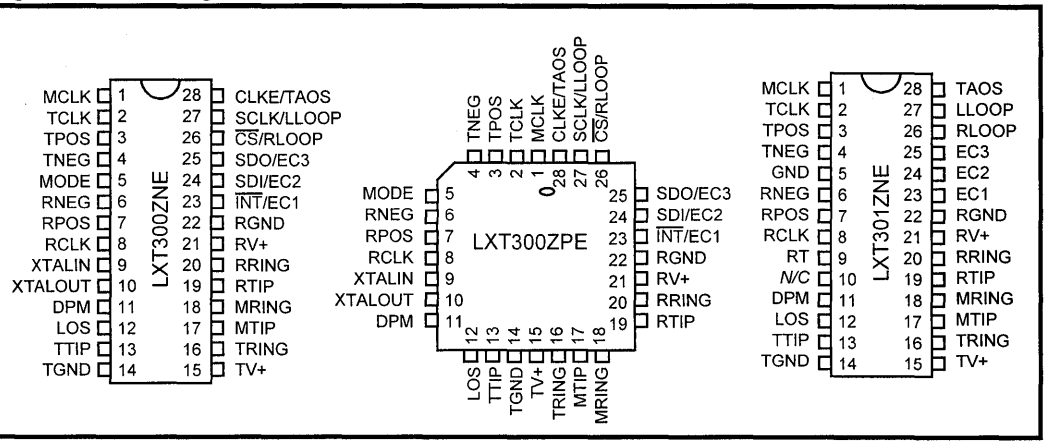


Table 1: Pin Descriptions

Pin #	Sym	I/O[1]	Description
1	MCLK	DI	**Master Clock.** A 1.544 or 2.048 MHz clock input used to generate internal clocks. Upon Loss of Signal (LOS), RCLK is derived from MCLK. *LXT300Z Only: If MCLK is not applied, this pin should be grounded.*
2	TCLK	DI	**Transmit Clock.** Transmit clock input. TPOS and TNEG are sampled on the falling edge of TCLK. If TCLK is grounded, the output drivers enter a high-Z state, except during Remote Loopback.
3	TPOS	DI	**Transmit Positive Data.** Input for positive pulse to be transmitted on the twisted-pair line.
4	TNEG	DI	**Transmit Negative Data.** Input for negative pulse to be transmitted on the twisted-pair line.
5	MODE	DI	**Mode Select *(LXT300z).*** Setting MODE High puts the LXT300Z in the Host Mode. In the Host Mode, the serial interface is used to control the LXT300Z and determine its status. Setting MODE Low puts the LXT300Z in the Hardware (H/W) mode. In the Hardware Mode, the serial interface is disabled and hard-wired pins are used to control configuration and report status.
	GND	S	**Ground *(LXT301Z).*** Tie to Ground.

1. Entries in I/O column are: DI = Digital Input; DO = Digital Output; AI = Analog Input; AO = Analog Output; S = Supply.

Table 1: Pin Descriptions – continued

Pin #	Sym	I/O[1]	Description
6	RNEG	DO	**Receive Negative Data; Receive Positive Data.** Received data outputs. A signal on RNEG corresponds to receipt of a negative pulse on RTIP and RRING. A signal on RPOS corresponds to receipt of a positive pulse on RTIP and RRING. RNEG and RPOS outputs are Non-Return-to-Zero (NRZ). Both outputs are stable and valid on the rising edge of RCLK. *LXT300Z only: In the Host Mode, CLKE determines the clock edge at which these outputs are stable and valid. In the Hardware Mode both outputs are stable and valid on the rising edge of RCLK.*
7	RPOS	DO	
8	RCLK	DO	**Recovered Clock.** This is the clock recovered from the signal received at RTIP and RRING.
9	XTALIN	AI	**Crystal Input; Crystal Output *(LXT300Z).*** An external crystal operating at four times the bit rate (6.176 MHz for DSX-1, 8.192 MHz for E1 applications with an 18.7 pF load) is required to enable the jitter attenuation function of the LXT300Z. These pins may also be used to disable the jitter attenuator by connecting the XTALIN pin to the positive supply through a resistor, and floating the XTALOUT pin.
10	XTALOUT	AO	
9	RT	AI	**Receive Termination *(LXT301Z).*** Connect to RV+ through a 1 k Ω resistor.
10	N/C	–	**No Connection *(LXT301Z).***
11	DPM	DO	**Driver Performance Monitor.** DPM goes High when the transmit monitor loop (MTIP and MRING) does not detect a signal for 63 ±2 clock periods. DPM remains High until a signal is detected.
12	LOS	DO	**Loss of Signal.** LOS goes High when 175 consecutive spaces have been detected. LOS returns Low when a mark is detected.
13	TTIP	AO	**Transmit Tip; Transmit Ring.** Differential Driver Outputs. These outputs are designed to drive a 25 Ω load. The transmitter will drive 100 Ω shielded twisted-pair cable through a 1:2 step-up transformer without additional components. To drive 75 Ω coaxial cable, two 2.2 Ω resistors are required in series with the transformer.
16	TRING	AO	
14	TGND	S	**Transmit Ground.** Ground return for the transmit drivers power supply TV+.
15	TV+	S	**Transmit Power Supply.** +5 VDC power supply input for the transmit drivers. TV+ must not vary from RV+ by more than ±0.3 V.
17	MTIP	AI	**Monitor Tip; Monitor Ring.** These pins are used to monitor the tip and ring transmit outputs. The transceiver can be connected to monitor its own output or the output of another LXT300Z or LXT301Z on the board.
18	MRING	AI	
19	RTIP	AI	**Receive Tip; Receive Ring.** The AMI signal received from the line is applied at these pins. A center-tapped, center-grounded, 2:1 step-up transformer is required on these pins. Data and clock from the signal applied at these pins are recovered and output on the RPOS/RNEG and RCLK pins.
20	RRING	AI	
21	RV+	S	**Receive Power Supply.** +5 VDC power supply for all circuits except the transmit drivers. (Transmit drivers are supplied by TV+.)
22	RGND	S	**Receive Ground.** Ground return for power supply RV+.

1. Entries in I/O column are: DI = Digital Input; DO = Digital Output; AI = Analog Input; AO = Analog Output; S = Supply.

Table 1: Pin Descriptions – continued

Pin #	Sym	I/O[1]	Description
23	$\overline{INT}$	DO	**Interrupt** ***(Host Mode).*** This *LXT300Z Host Mode* output goes Low to flag the host processor when LOS or DPM go active. $\overline{INT}$ is an open-drain output and should be tied to power supply RV+ through a resistor. $\overline{INT}$ is reset by clearing the respective register bit (LOS and/or DPM).
	EC1	DI	**Equalizer Control 1** ***(H/W Mode).*** The signal applied at this pin in the *LXT300Z Hardware Mode and LXT301Z* is used in conjunction with EC2 and EC3 inputs to determine shape and amplitude of AMI output transmit pulses.
24	SDI	DI	**Serial Data In** ***(Host Mode).*** The serial data input stream is applied to this pin when the *LXT300Z* operates in the *Host Mode.* SDI is sampled on the rising edge of SCLK.
	EC2	DI	**Equalizer Control 2** ***(H/W Mode).*** The signal applied at this pin in the *LXT300Z Hardware Mode and LXT301Z* is used in conjunction with EC1 and EC3 inputs to determine shape and amplitude of AMI output transmit pulses.
25	SDO	DO	**Serial Data Out** ***(Host Mode).*** The serial data from the on-chip register is output on this pin in the *LXT300Z Host Mode.* If CLKE is High, SDO is valid on the rising edge of SCLK. If CLKE is Low SDO is valid on the falling edge of SCLK. This pin goes to a high-impedance state when the serial port is being written to and when $\overline{CS}$ is High.
	EC3	DI	**Equalizer Control 3** ***(H/W Mode).*** The signal applied at this pin in the *LXT300Z Hardware Mode and LXT301Z* is used in conjunction with EC1 and EC2 inputs to determine shape and amplitude of AMI output transmit pulses.
26	$\overline{CS}$	DI	**Chip Select** ***(Host Mode).*** This input is used to access the serial interface in the *LXT300Z Host Mode.* For each read or write operation, $\overline{CS}$ must transition from High to Low, and remain Low.
	RLOOP	DI	**Remote Loopback** ***(H/W Mode).*** This input controls loopback functions in the *LXT300Z Hardware Mode and LXT301Z.* Setting RLOOP High enables the Remote Loopback mode. Setting both RLOOP and LLOOP High causes a Reset.
27	SCLK	DI	**Serial Clock** ***(Host Mode).*** This clock is used in the *LXT300Z Host Mode* to write data to or read data from the serial interface registers.
	LLOOP	DI	**Local Loopback** ***(H/W Mode).*** This input controls loopback functions in the *LXT300Z Hardware Mode and LXT301Z.* Setting LLOOP High enables the Local Loopback Mode.
28	CLKE	DI	**Clock Edge** ***(Host Mode).*** Setting CLKE High causes RPOS and RNEG to be valid on the falling edge of RCLK, and SDO to be valid on the rising edge of SCLK. When CLKE is Low, RPOS and RNEG are valid on the rising edge of RCLK, and SDO is valid on the falling edge of SCLK.
	TAOS	DI	**Transmit All Ones** ***(H/W Mode).*** When High, TAOS causes the *LXT300Z (Hardware Mode) and LXT301Z* to transmit a continuous stream of marks at the TCLK frequency. Activating TAOS causes TPOS and TNEG inputs to be ignored. TAOS is inhibited during Remote Loopback.

1. Entries in I/O column are: DI = Digital Input; DO = Digital Output; AI = Analog Input; AO = Analog Output; S = Supply.

FUNCTIONAL DESCRIPTION

The LXT300Z and LXT301Z are fully integrated PCM transceivers for both 1.544 Mbps (DSX-1) and 2.048 Mbps (E1) applications. Both transceivers allow full-duplex transmission of digital data over existing twisted-pair installations. The first page of this data sheet shows a simplified block diagram of the LXT300Z; Figure 2 shows the LXT301Z. The LXT301Z is similar to the LXT300Z, but does not incorporate the Jitter Attenuator and associated Elastic Store, or the serial interface port.

The LXT300Z and LXT301Z transceivers each interface with two twisted-pair lines (one twisted-pair for transmit, one twisted-pair for receive) through standard pulse transformers and appropriate resistors.

Power Requirements

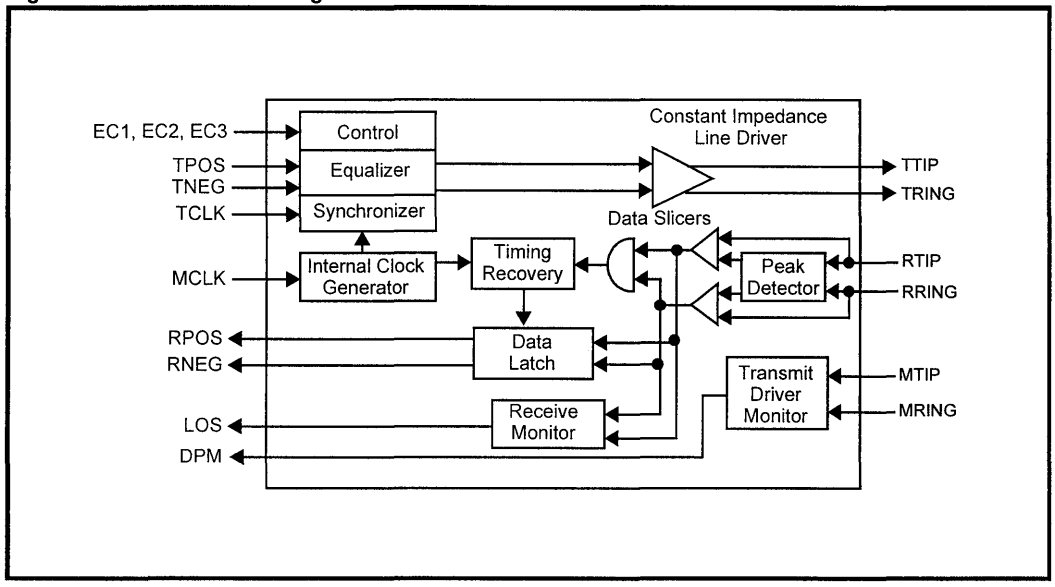
The LXT300Z and LXT301Z are low-power CMOS devices. Each operates from a single +5 V power supply which can be connected externally to both the transmitter and receiver. However, the two inputs must be within ± .3V of each other, and decoupled to their respective grounds separately. Refer to Application Information for typical decoupling circuitry. Isolation between the transmit and receive circuits is provided internally.

Reset Operation *(LXT300Z and LXT301Z)*

Upon power up, the transceiver is held static until the power supply reaches approximately 3 V. Upon crossing this threshold, the device begins a 32 ms reset cycle to calibrate the transmit and receive delay lines and lock the Phase Lock Loop to the receive line. A reference clock is required to calibrate the delay lines. The transmitter reference is provided by TCLK. MCLK provides the receiver reference for the LXT301Z. The crystal oscillator provides the receiver reference in the LXT300Z. If the LXT300Z crystal oscillator is grounded, MCLK is used as the receiver reference clock.

The transceiver can also be reset from the Host or Hardware Mode. In Host Mode, reset is commanded by simultaneously writing RLOOP and LLOOP to the register. In Hardware Mode, reset is commanded by holding RLOOP and LLOOP High simultaneously for 200 ns. Reset is initiated on the falling edge of the reset request. In either mode, reset clears and sets all registers to 0 and then begins calibration.

Figure 2: LXT301Z Block Diagram



Receiver

The LXT300Z and LXT301Z receivers are identical except for the Jitter Attenuator and Elastic Store. The following discussion applies to both transceivers except where noted.

The signal is received from one twisted-pair line on each side of a center-grounded transformer. Positive pulses are received at RTIP and negative pulses are received at RRING. Recovered data is output at RPOS and RNEG, and the recovered clock is output at RCLK. Refer to the Test Specifications section for receiver timing.

The signal received at RPOS and RNEG is processed through the peak detector and data slicers. The peak detector samples the inputs and determines the maximum value of the received signal. A percentage of the peak value is provided to the data slicers as a threshold level to ensure optimum signal-to-noise ratio. For DSX-1 applications (determined by Equalizer Control inputs EC1~EC3 ≠ 000) the threshold is set to 70% of the peak value. This threshold is maintained above 65% for up to 15 successive zeros over the range of specified operating conditions. For E1 applications (EC inputs = 000) the threshold is set to 50%.

The receiver is capable of accurately recovering signals with up to -13.6 dB of attenuation (from 2.4 V), corresponding to a received signal level of approximately 500 mV. Maximum line length is 1500 feet of ABAM cable (approximately 6 dB). Regardless of received signal level, the peak detectors are held above a minimum level of 300 mV to provide immunity from impulsive noise. (During LOS, RPOS and RNEG are squelched if the received input signal drops to 300 mV.)

After processing through the data slicers, the received signal is routed to the data and clock recovery sections, and to the receive monitor. *In the LXT300Z only, recovered clock signals are supplied to the jitter attenuator and the data latch. The recovered data is passed to the elastic store where it is buffered and synchronized with the dejittered recovered clock (RCLK).* The data and clock recovery circuits have an input jitter tolerance significantly better than required by Pub 62411.

Receive (Loss of Signal) Monitor

The receive monitor generates a Loss of Signal (LOS) output upon receipt of 175 consecutive zeros (spaces). The receiver monitor loads a digital counter at the RCLK frequency. The count is incremented each time a zero is received, and reset to zero each time a one (mark) is received. Upon receipt of 175 consecutive zeros the LOS pin goes High, and the RCLK output is replaced with the MCLK. LOS is reset when the first mark is received.

(*In the LXT300Z only, if MCLK is not supplied the RCLK output will be replaced with the centered crystal clock.*)

Jitter Attenuation (LXT300Z Only)

In the LXT300Z only, recovered clock signals are supplied to the jitter attenuator and the data latch. The recovered data is passed to the elastic store where it is buffered and synchronized with the dejittered recovered clock (RCLK). Jitter attenuation of the LXT300Z clock and data outputs (see Figure 4) is provided by a Jitter Attenuation Loop (JAL) and an Elastic Store (ES). An external crystal oscillating at 4 times the bit rate provides clock stabilization. Refer to Application Information for crystal specifications. The ES is a 32 x 2-bit register. Recovered data is clocked into the ES with the recovered clock signal, and clocked out of the ES with the dejittered clock from the JAL. When the bit count in the ES is within two bits of overflowing or underflowing, the ES adjusts the output clock by 1/8 of a bit period. The ES produces an average delay of 16 bits in the receive path.

Transmitter

The transmitter circuits in the LXT300Z and LXT301Z are identical. The following discussion applies to both models. Data received for transmission onto the line is clocked serially into the device at TPOS and TNEG. Input synchronization is supplied by the transmit clock (TCLK). The transmitted pulse shape is determined by Equalizer Control signals EC1 through EC3 as shown in Table 2. Refer to the Test Specifications section for master and transmit clock timing characteristics. Shaped pulses are applied to the AMI line driver for transmission onto the line at TTIP and TRING. Equalizer Control signals are hard-wired to the LXT301Z.

LXT300Z Only: Equalizer Control signals may be hard-wired in the Hardware Mode, or input as part of the serial data stream (SDI) in the Host Mode.

Pulses can be shaped for either 1.544 or 2.048 Mbps applications. DSX-1 applications with 1.544 Mbps pulses can be programmed to match line lengths from 0 to 655 feet of ABAM cable. The LXT300Z and LXT301Z also match FCC specifications for CSU applications. Pulses at 2.048 Mbps can drive coaxial or shielded twisted-pair lines using appropriate resistors in line with the output transformer.

Driver Performance Monitor

The transceiver incorporates an advanced Driver Performance Monitor (DPM) in parallel with the TTIP and TRING at the output transformer. The DPM circuitry uses four comparators and a 150 ns pulse discriminator to filter glitches. The DPM output level goes high upon detection of 63 consecutive zeros, and is cleared when a one is detected on the transmit line, or when a reset command is received. The DPM output also goes High to indicate a ground on TTIP or TRING. A ground fault induced DPM flag is automatically cleared when the ground condition is corrected (chip reset is not required).

Line Code

The LXT300Z and LXT301Z transmit data as a 50% AMI line code as shown in Figure 3. Power consumption is reduced by activating the AMI line driver only to transmit a mark. The output driver is disabled during transmission of a space.

Operating Modes

The LXT300Z and LXT301Z transceivers can be controlled through hard-wired pins (Hardware Mode). Both transceivers can also be commanded to operate in one of several diagnostic modes.

LXT300Z Only: The LXT300Z can be controlled by a microprocessor through a serial interface (Host Mode). The mode of operation is set by the MODE pin logic level.

Host Mode Operation (LXT300Z Only)

To allow a host microprocessor to access and control the LXT300Z through the serial interface, MODE is set to 1. The serial interface (SDI/SDO) uses a 16-bit word consisting of an 8-bit Command/Address byte and an 8-bit Data byte. Figure 4 shows the serial interface data structure and relative timing.

The Host Mode provides a latched Interrupt output ($\overline{INT}$) which is triggered by a change in the Loss of Signal (LOS) and/or Driver Performance Monitor (DPM) bits. The Interrupt is cleared when the interrupt condition no longer exists, and the host processor enables the respective bit in the serial input data byte. Host Mode also allows control of the serial data and receive data output timing. The Clock Edge (CLKE) signal determines when these outputs are valid, relative to the Serial Clock (SCLK) or RCLK as listed in Table 3.

The LXT300Z serial port is addressed by setting bit A4 in the Address/Command byte, corresponding to address 16. The LXT300Z contains only a single output data register so no complex chip addressing scheme is required. The register is accessed by causing the Chip Select ($\overline{CS}$) input to transition from High to Low. Bit 1 of the serial Address/Command byte provides Read/Write control when the chip is accessed. A logic 1 indicates a read operation, and a logic 0 indicates a write operation. Table 4 lists serial data output bit combinations for each status. Serial data I/O timing characteristics are shown in the Test Specifications section.

Hardware Mode Operation *(LXT300Z and LXT301Z)*

In Hardware Mode the transceiver is accessed and controlled through individual pins. With the exception of the $\overline{INT}$ and CLKE functions, Hardware Mode provides all the functions provided in the Host Mode. In the Hardware Mode RPOS and RNEG outputs are valid on the rising edge of RCLK. The LXT301Z operates in Hardware Mode at all times.

LXT300Z Only: To operate in Hardware Mode, MODE must be set Low. Equalizer Control signals (EC1 through EC3) are input on the Interrupt, Serial Data In and Serial Data Out pins. Diagnostic control for Remote Loopback (RLOOP), Local Loopback (LLOOP), and Transmit All Ones (TAOS) modes is provided through the individual pins used to control serial interface timing in the Host Mode.

Figure 3: 50% AMI Coding

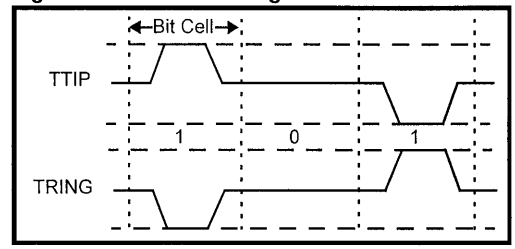


Table 2: LXT300Z Serial Data Output Bits
(See Figure 4)

Bit D5	Bit D6	Bit D7	Status
0	0	0	Reset has occurred, or no program input.
0	0	1	TAOS is active.
0	1	0	Local Loopback is active.
0	1	1	TAOS and Local Loopback are active.
1	0	0	Remote Loopback is active.
1	0	1	DPM has changed state since last Clear DPM occurred.
1	1	0	LOS has changed state since last Clear LOS occurred.
1	1	1	LOS and DPM have both changed state since last Clear DPM and Clear LOS occurred.

Table 3: Valid CLKE Settings

CLKE	Output	Clock	Valid Edge
Low	RPOS RNEG SDO	RCLK RCLK SCLK	Rising Rising Falling
High	RPOS RNEG SDO	RCLK RCLK SCLK	Falling Falling Rising

Table 4: Equalizer Control Inputs

EC3	EC2	EC1	Line Length[1]	Cable Loss[2]	Application	Bit Rate
0	1	1	0 ~ 133 ft ABAM	0.6 dB	DSX-1	1.544 Mbps
1	0	0	133 ~ 266 ft ABAM	1.2 dB		
1	0	1	266 ~ 399 ft ABAM	1.8 dB		
1	1	0	399 ~ 533 ft ABAM	2.4 dB		
1	1	1	533 ~ 655 ft ABAM	3.0 dB		
0	0	0	ITU Recommendation G.703		E1	2.048 Mbps
0	1	0	FCC Part 68, Option A		CSU	1.544 Mbps

1. Line length from transceiver to DSX-1 cross-connect point.
2. Maximum cable loss at 772 kHz.

Diagnostic Mode Operation

Transmit All Ones

In Transmit All Ones (TAOS) mode the TPOS and TNEG inputs to the transceiver are ignored. The transceiver transmits a continuous stream of ones when the TAOS mode is activated. TAOS can be commanded simultaneously with Local Loopback, but is inhibited during Remote Loopback.

Remote Loopback

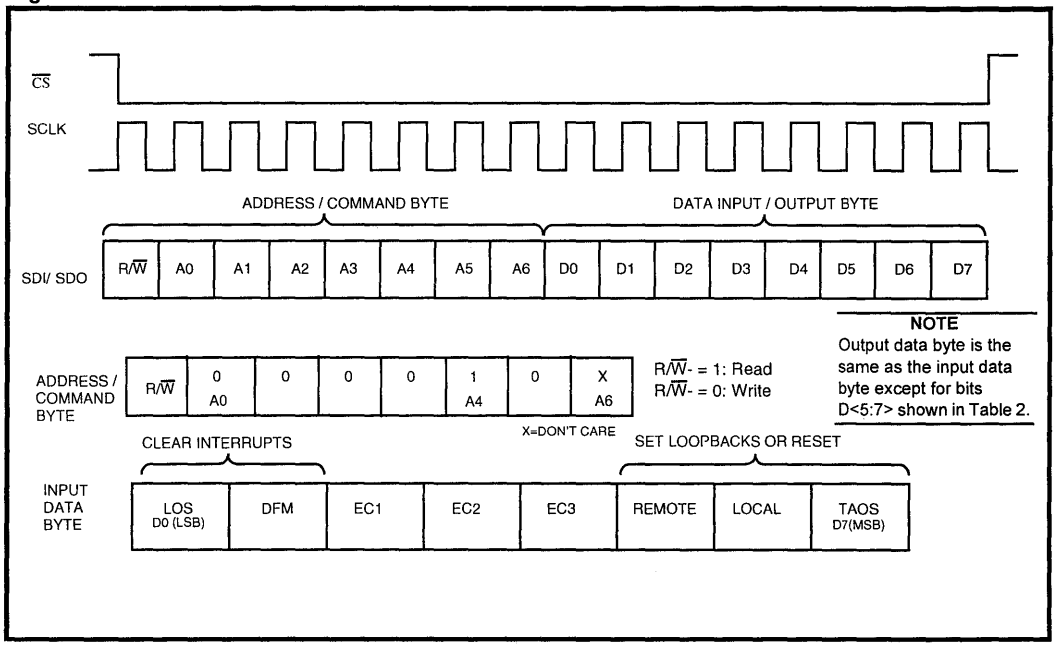
In Remote Loopback (RLOOP) mode, the transmit data and clock inputs (TPOS, TNEG and TCLK) are ignored. The RPOS and RNEG outputs are looped back through the transmit circuits and output on TTIP and TRING at the RCLK frequency. Receiver circuits are unaffected by the RLOOP command and continue to output the RPOS, RNEG and RCLK signals received from the twisted-pair line.

Local Loopback

In Local Loopback (LLOOP) mode, the receiver circuits are inhibited. The transmit data and clock inputs (TPOS, TNEG and TCLK) are looped back onto the receive data and clock outputs (RPOS, RNEG and RCLK) through the Rx jitter attenuator. The transmitter circuits are unaffected by the LLOOP command. The TPOS and TNEG inputs (or a stream of ones if the TAOS command is active) will be transmitted normally.

LXT300Z Only: When used in this mode with a crystal, the transceiver can be used as a stand-alone jitter attenuator.

Figure 4: LXT300Z Serial Interface Data Structure

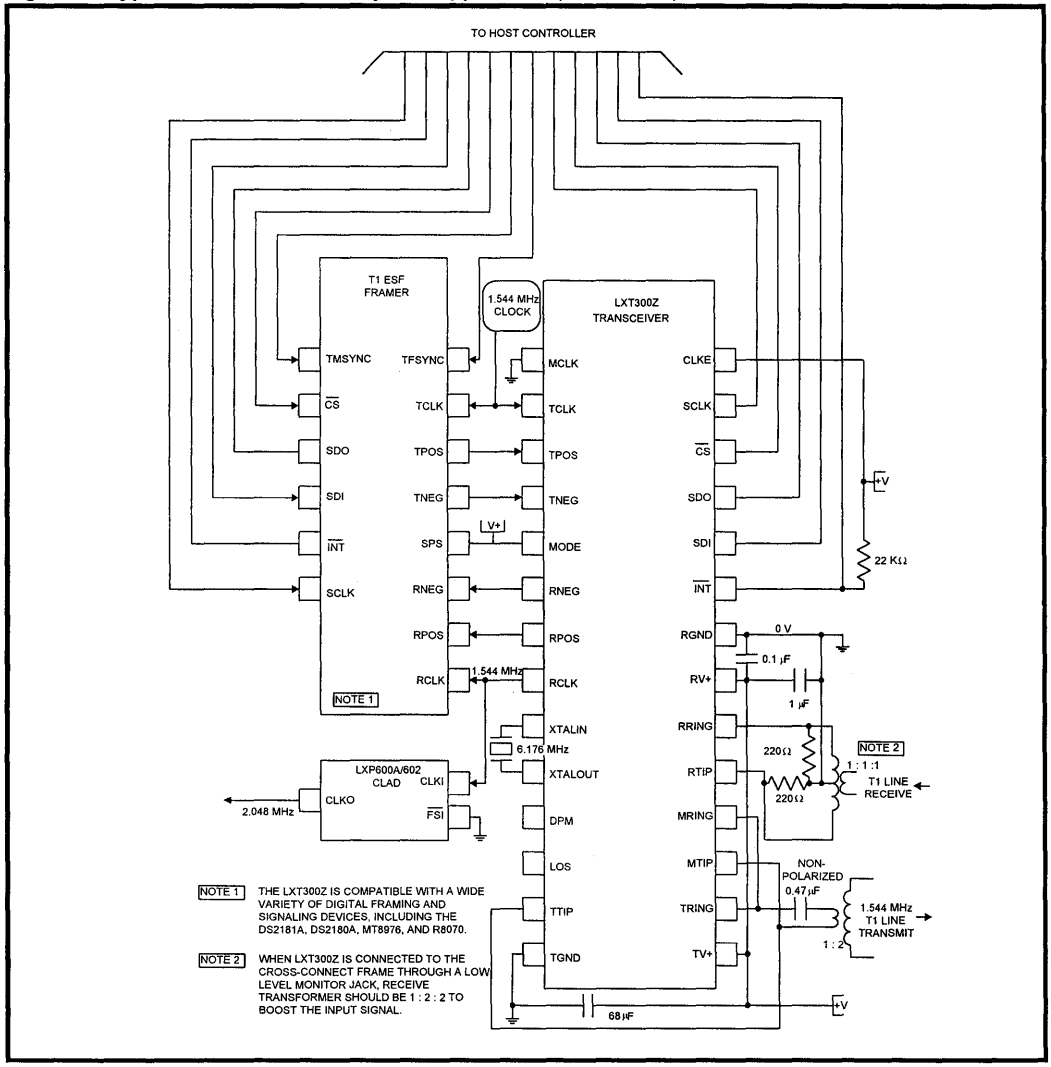


APPLICATION INFORMATION

LXT300Z Host Mode 1.544 Mbps T1 Interface Application

Figure 5 is a typical 1.544 Mbps T1 application. The LXT300Z is shown in the Host Mode with a typical T1/ESF framer providing the digital interface with the host controller. Both devices are controlled through the serial interface. An LXP600A Clock Adapter (CLAD) provides the 2.048 MHz system backplane clock, locked to the recovered 1.544 MHz clock signal. The power supply inputs are tied to a common bus with appropriate decoupling capacitors installed (68 µF on the transmit side, 1.0 µF and 0.1 µF on the receive side).

Figure 5: Typical LXT300Z 1.544 Mbps T1 Application (Host Mode)



LXT300Z Hardware Mode E1 Interface Application

Figure 6 is a typical 2.048 Mbps E1 application. The LXT300Z is shown in Hardware Mode with a typical E1/CRC4 framer. Resistors are installed in line with the transmit transformer for loading a 75 Ω coaxial cable. The inline resistors are not required for transmission on 120 Ω shielded twisted-pair lines. As in the T1 application Figure 5, this configuration is illustrated with a crystal in place to enable the LXT300Z Jitter Attenuation Loop, and a single power supply bus. The hard-wired control lines for TAOS, LLOOP and RLOOP are individually controllable, and the LLOOP and RLOOP lines are also tied to a single control for the Reset function

Figure 6: Typical LXT300Z 75 Ω E1 Application (Hardware Mode)

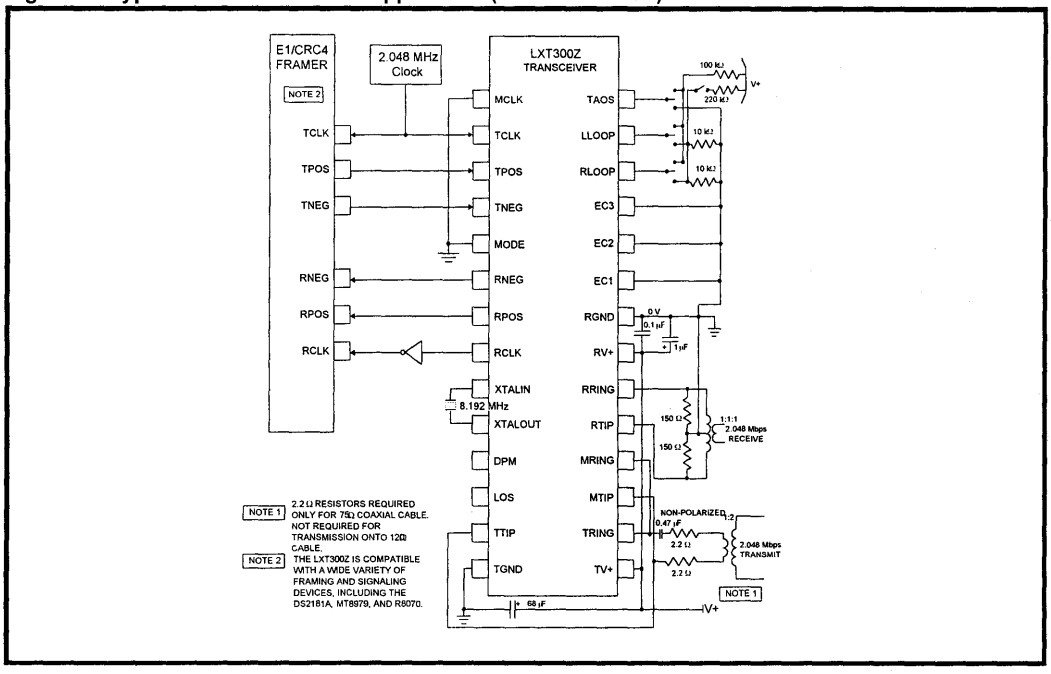


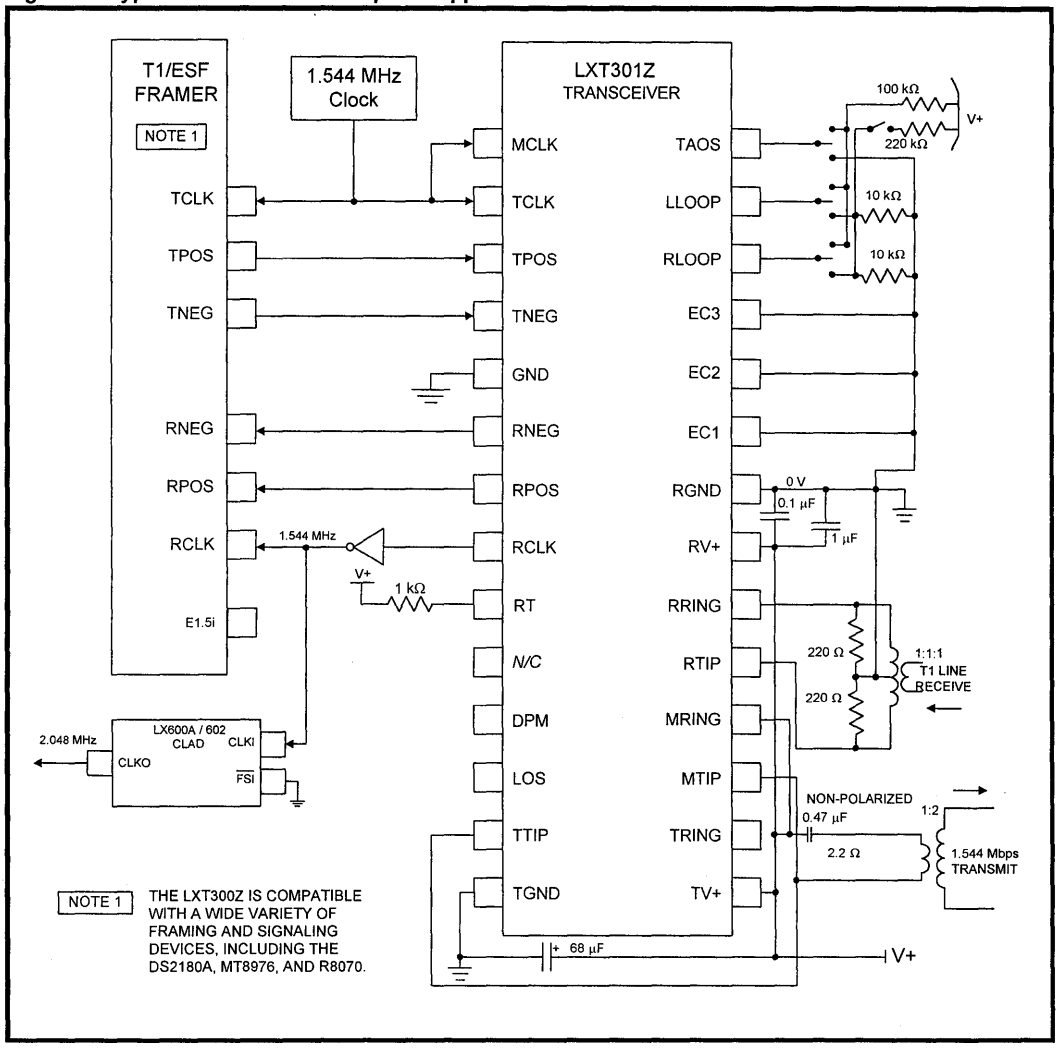
Table 5: LXT300Z Crystal Specifications (External)

Parameter	T1	E1
Frequency	6.176 MHz	8.192 MHz
Frequency stability	± 20 ppm @ 25 °C ± 25 ppm from -40 °C to 85 °C (Ref 25 °C reading)	± 20 ppm @ 25 °C ± 25 ppm from -40 °C to +85 °C (Ref 25 °C reading)
Pullability	CL = 11 pF to 18.7 pF, +ΔF = 175 to 195 ppm CL = 18.7 pF to 34 pF, -ΔF = 175 to 195 ppm	CL = 11 pF to 18.7 pF, +ΔF = 95 to 115 ppm CL = 18.7 pF to 34 pF, -ΔF = 95 to 115 ppm
Effective series resistance	40 Ω Maximum	30 Ω Maximum
Crystal cut	AT	AT
Resonance	Parallel	Parallel
Maximum drive level	2.0 mW	2.0 mW
Mode of operation	Fundamental	Fundamental
Crystal holder	HC49 (R3W), Co = 7 pF maximum C_M = 17 fF typical	HC49 (R3W),Co = 7 pF maximum C_M = 17 fF typical

LXT301Z 1.544 Mbps T1 Interface Application

Figure 7 is a typical 1.544 Mbps T1 application of the LXT301Z. The LXT301Z is shown with a typical T1/ESF framer. An LXP600A Clock Adapter (CLAD) provides the 2.048 MHz system backplane clock, locked to the recovered 1.544 MHz clock signal. The power supply inputs are tied to a common bus with appropriate decoupling capacitors installed (68 µF on the transmit side, 1.0 µF and 0.1 µF on the receive side).

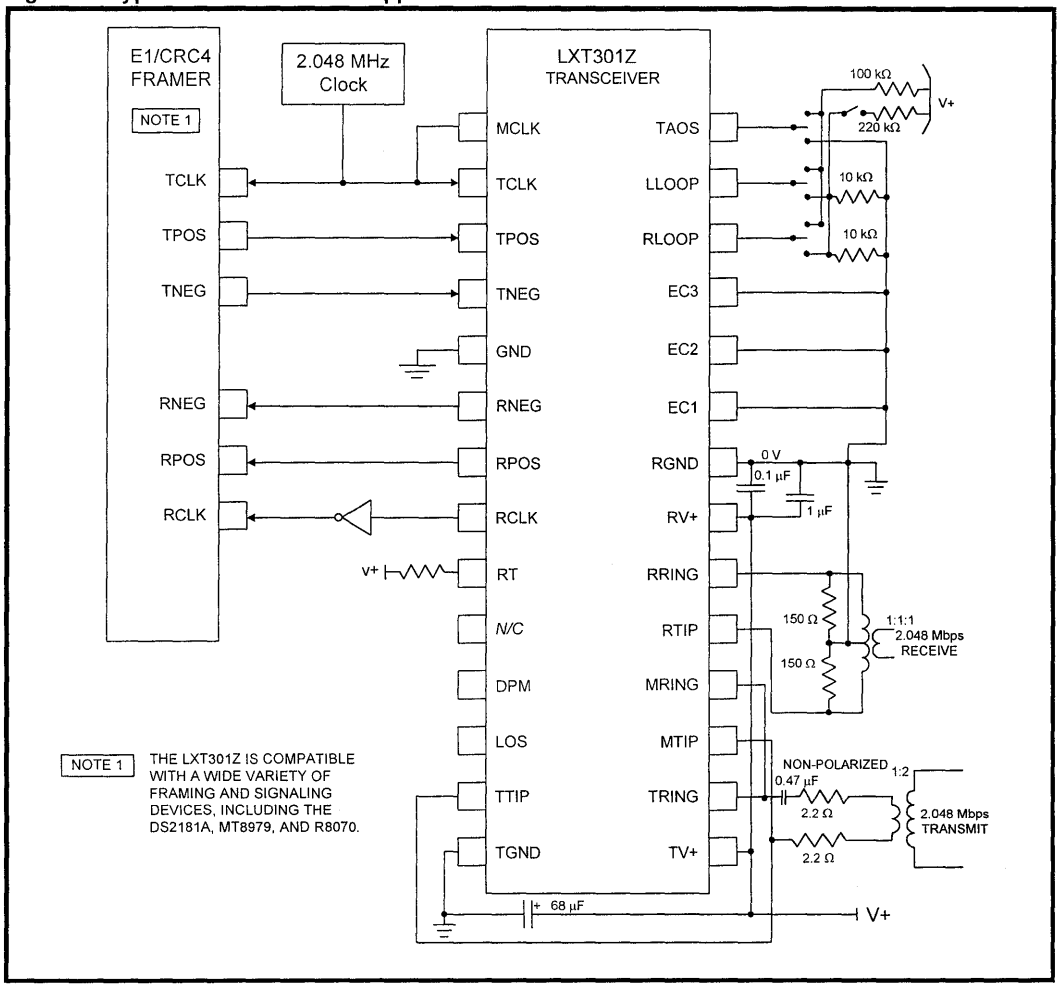
Figure 7: Typical LXT301Z 1.544 Mbps T1 Application



LXT301Z 2.048 Mbps E1 Interface Application

Figure 8 is a typical 2.048 Mbps E1 application of the LXT301Z. The LXT301Z is shown with a typical E1/CRC4 framer. Resistors are installed in line with the transmit transformer for loading a 75 Ω coaxial cable. The in-line resistors are not required for transmission on 120 Ω shielded twisted-pair lines. As in the T1 application Figure 7, this configuration is illustrated with a single power supply bus. The hard-wired control lines for TAOS, LLOOP and RLOOP are individually controllable, and the LLOOP and RLOOP lines are also tied to a single control for the Reset function.

Figure 8: Typical LXT301Z 75 Ω E1 Application



TEST SPECIFICATIONS

NOTE

The minimum and maximum values in Tables 6 through 13 and Figures 11 through 15 represent the performance specifications of the LXT300Z/LXT301Z and are guaranteed by test, except where noted by design.

Table 6: Absolute Maximum Ratings

Parameter	Sym	Min	Max	Units
DC supply (referenced to GND)	RV+, TV+	-0.3	6.0	V
Input voltage, any pin[1]	V_{IN}	RGND - 0.3	RV+ + 0.3	V
Input current, any pin[2]	I_{IN}	-10	10	mA
Storage temperature	T_{STG}	-65	150	°C

CAUTION

Operations at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

1. Excluding RTIP and RRING which must stay between -6V and (RV+ + 0.3) V.
2. Transient currents of up to 100 mA will not cause SCR latch up. TTIP, TRING, TV+ and TGND can withstand a continuous current of 100 mA.

Table 7: Recommended Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
DC supply[1]	RV+, TV+	4.75	5.0	5.25	V
Ambient operating temperature	T_A	-40	25	85	° C

1. TV+ must not exceed RV+ by more than 0.3 V.

Table 8: Electrical Characteristics (Under Recommended Operating Conditions)

Parameter	Sym	Min	Typ	Max	Units	Test Conditions
High level input voltage[1,2] (pins 1-5, 10, 23-28)	V_{IH}	2.0	–	–	V	
Low level input voltage[1,2] (pins 1-5, 10, 23-28)	V_{IL}	–	–	0.8	V	
High level output voltage[1,2](pins 6-8, 11, 12, 23, 25)	V_{OH}	2.4	–	–	V	I_{OUT} = -400 µA
Low level output voltage[1,2] (pins 6-8, 11, 12, 23, 25)	V_{OL}	–	–	0.4	V	I_{OUT} = 1.6 mA
Input leakage current (pins 1-5, and 23-28)	I_{LL}	-10	–	+10	µA	
Input leakage current (pins 9, 17, and 18)	I_{LL}	-50	–	+50	µA	
Three-state leakage current[1] (pin 25)	I_{3L}	-10	–	+10	µA	
Total power dissipation[3]	P_D	–	–	700	mW	100% ones density & maximum line length @ 5.25 V

1. Functionality of pins 23 and 25 depends on mode. See Host/Hardware Mode descriptions.
2. Output drivers will output CMOS logic levels into CMOS loads.
3. Power dissipation while driving a 25 Ω load over operating temperature range. Includes device and load. Digital input levels are within 10% of the supply rails and digital outputs are driving a 50 pF capacitive load.

Table 9: Analog Characteristics (Under Recommended Operating Conditions)

Parameter		Min	Typ[1]	Max	Units	Test Conditions
AMI output pulse amplitudes	DSX-1	2.4	3.0	3.6	V	measured at the DSX
	E1 (120 Ω)	2.7	3.0	3.3	V	measured at line side
	E1 (75 Ω)	2.14	2.37	2.6	V	@ 772 kHz
Transmit amplitude variation with supply			1	2.5	%	
Recommended output load at TTIP and TRING		–	25	–	Ω	RTIP to RRING
Driver output impedance[2]		–	3	10	Ω	@ 10 kHz
Jitter added by the transmitter[3]	10 Hz - 8 kHz[2]	–	–	0.01	UI	
	8 kHz - 40 kHz	–	–	0.025	UI	
	10 Hz - 40 kHz	–	–	0.025	UI	
	Broad Band	–	–	0.05	UI	
Output power levels[2] DS1 2 kHz BW	@ 772 kHz	12.6	–	17.9	dBm	
	@ 1544 kHz[5]	-29.0	–	–	dB	
Positive to negative pulse imbalance		–	–	0.5	dB	
Sensitivity below DSX[6] (0 dB = 2.4 V)		13.6	–	–	dB	
		500	–	–	mV	
Receiver input impedance		–	40	–	kΩ	
Loss of Signal threshold		–	0.3	–	V	
Data decision threshold	DSX-1	63	70	77	% peak	
	E1	43	50	57	% peak	
Allowable consecutive zeros before LOS		160	175	190	–	
Input jitter tolerance	10 Hz	–	1200	–	UI	
	775 Hz	14	–	–	UI	
	10 kHz - 100 kHz	0.4	–	–	UI	
Jitter attenuation curve corner frequency[4]		–	3	–	Hz	
Jitter attenuation		–	50	–	db	
Jitter attenuation tolerance before FIFO Overflow[2]		28	–	–	UI	

1. Typical values are measured at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Not production tested but guaranteed by design and other correlation methods.
3. Input signal to TCLK is jitter-free.
4. Circuit attenuates jitter at 20 dB/decade above the corner frequency.
5. Referenced to power in 2 kHz band.
6. With a maximum of 6 dB of cable attenuation.

Figure 9: LXT300Z Rx Jitter Tolerance (Typical)

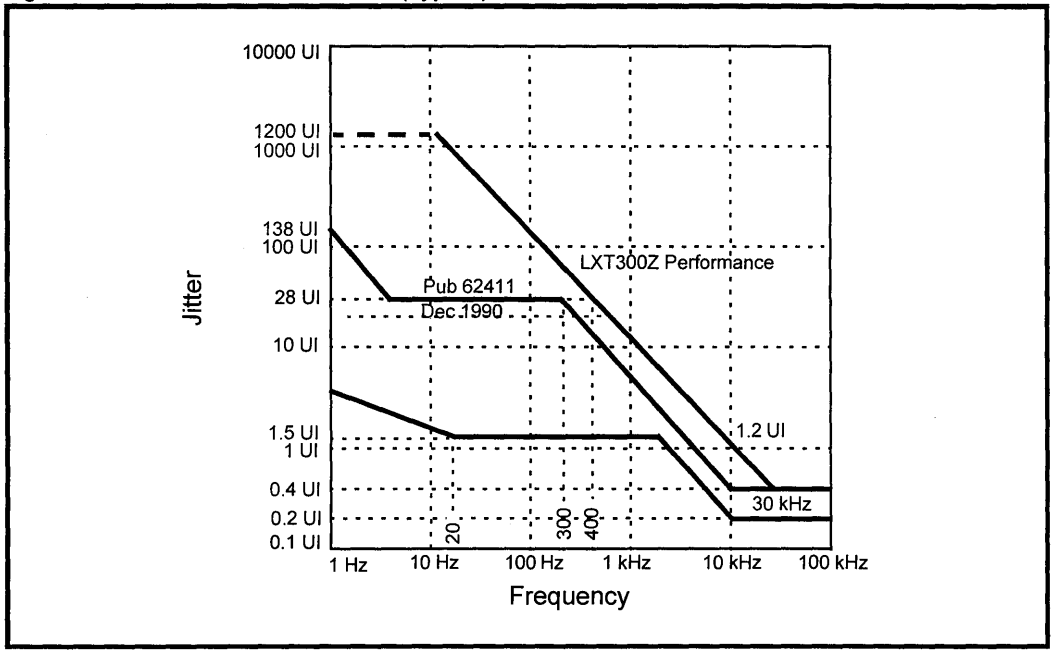


Figure 10: LXT300Z Rx Jitter Transfer Performance (Typical)

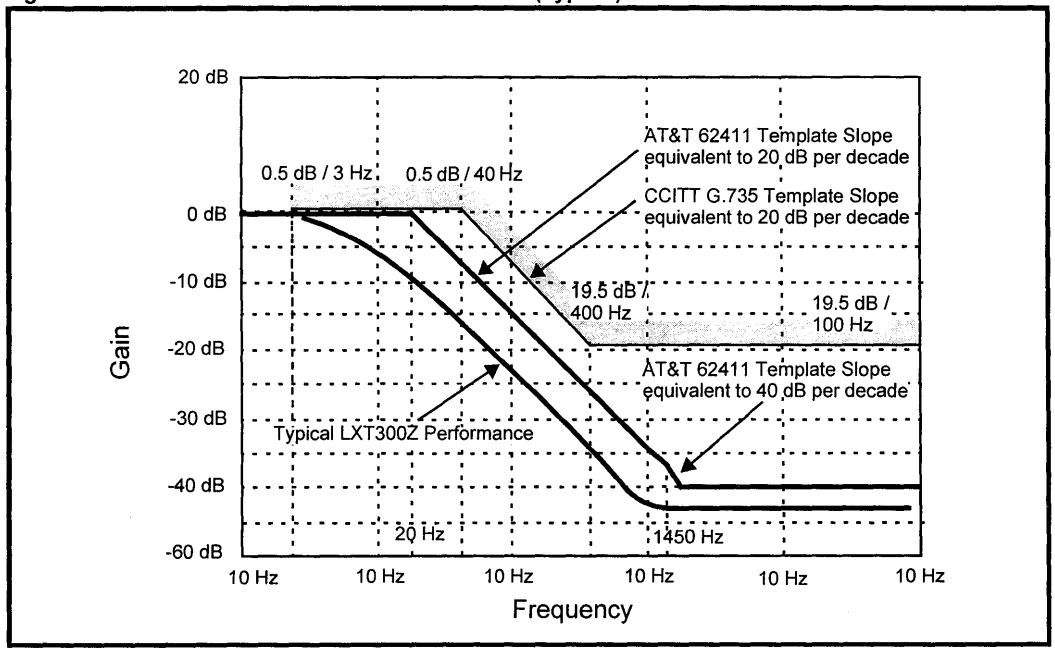


Table 10: **LXT300Z Receiver Timing Characteristics** (See Figure 11)

Parameter		Sym	Min	Typ[1]	Max	Units	Test Conditions
Receive clock duty cycle		RCLKd	40	-	60	%	
Receive clock pulse width[2]	DSX-1	t_{PW}	–	324	–	ns	
	E1	t_{PW}	–	244	–	ns	
RPOS/RNEG to RCLK rising setup time	DSX-1	t_{SUR}	–	274	–	ns	
	E1	t_{SUR}	–	194	–	ns	
RCLK rising to RPOS/RNEG hold time	DSX-1	t_{HR}	–	274	–	ns	
	E1	t_{HR}	–	194	–	ns	

1. Typical values are at 25 °C and are for design aid only; they are not guaranteed and not subject to production testing.

Figure 11: LXT300Z Receive Clock Timing Diagram

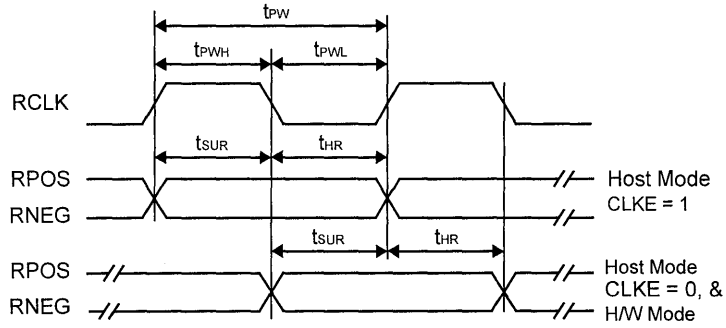


Table 11: LXT301Z Receive Timing Characteristics (See Figure 12)

Parameter		Sym	Min	Typ[1]	Max	Units	Test Conditions
Receive clock duty cycle[2]	DSX-1	RCLKd	40	50	60	%	
	E1	RCLKd	40	50	60	%	
Receive clock pulse width[2]	DSX-1	t_{PW}	594	648	702	ns	
	E1	t_{PW}	447	488	529	ns	
Receive clock pulse width high	DSX-1	t_{PWH}	–	324	–	ns	
	E1	t_{PWH}	–	244	–	ns	
Receive clock pulse width low	DSX-1	t_{PWL}	270	324	378	ns	
	E1	t_{PWL}	203	244	285	ns	
RPOS/RNEG to RCLK rising setup time	DSX-1	t_{SUR}	50	270	–	ns	
	E1	t_{SUR}	50	203	–	ns	
RCLK rising to RPOS/RNEG hold time	DSX-1	t_{HR}	50	270	–	ns	
	E1	t_{HR}	50	203	–	ns	

1. Typical values are at 25 °C and are for design aid only; they are not guaranteed and not subject to production testing.
2. RCLK duty cycle widths will vary depending on extent of received pulse jitter displacement. Max and Min RCLK duty cycles are for worst case jitter conditions (0.4 UI clock displacement for 1.544 MHz, 0.2 UI clock displacement for 2.048 MHz).

Figure 12: LXT301Z Receive Clock Timing Diagram

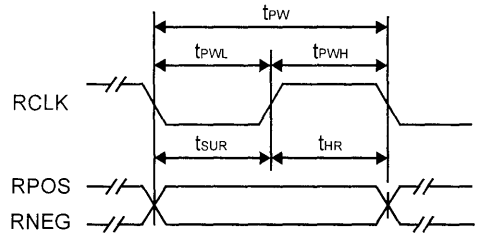


Table 12: LXT300Z/301Z Master Clock and Transmit Timing Characteristics (See Figure 13)

Parameter		Sym	Min	Typ[1]	Max	Units
Master clock frequency	DSX-1	MCLK	–	1.544	–	MHz
	E1	MCLK	–	2.048	–	MHz
Master clock tolerance		MCLKt	–	±100	–	ppm
Master clock duty cycle		MCLKd	40	–	60	%
Crystal frequency *(LXT300Z only)*	DSX-1	fc	–	6.176	–	MHz
	E1	fc	–	8.192	–	MHz
Transmit clock frequency	DSX-1	TCLK	–	1.544	–	MHz
	E1	TCLK	–	2.048	–	MHz
Transmit clock tolerance		TCLKt	–	±50	–	ppm
Transmit clock duty cycle		TCLKd	10	–	90	%
TPOS/TNEG to TCLK setup time		t_{SUT}	25	–	–	ns
TCLK to TPOS/TNEG hold time		t_{HT}	25	–	–	ns

1. Typical values are at 25 °C and are for design aid only; they are not guaranteed and not subject to production testing.
2. Not production tested but guaranteed by design and other correlation methods.

Figure 13: LXT300Z/301Z Transmit Clock Timing Diagram

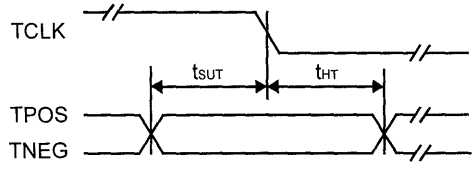


Table 13: LXT300Z Serial I/O Timing Characteristics (See Figures 14 and 15)

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Rise/Fall time - any digital output	t_{RF}	–	–	100	ns	Load 1.6 mA, 50 pF
SDI to SCLK setup time	t_{DC}	50	–	–	ns	
SCLK to SDI hold time	t_{CDH}	50	–	–	ns	
SCLK low time	t_{CL}	240	–	–	ns	
SCLK high time	t_{CH}	240	–	–	ns	
SCLK rise and fall time	t_R, t_F	–	–	50	ns	
$\overline{CS}$ to SCLK setup time	t_{CC}	50	–	–	ns	
SCLK to $\overline{CS}$ hold time	t_{CCH}	50	–	–	ns	
$\overline{CS}$ inactive time	t_{CWH}	250	–	–	ns	
SCLK to SDO valid	t_{CDV}	–	–	200	ns	
SCLK falling edge or $\overline{CS}$ rising edge to SDO high Z	t_{CDZ}	–	100	–	ns	

1. Typical values are at 25° C and are for design aid only; they are not guaranteed and not subject to production testing.

Figure 14: LXT300Z Serial Data Input Timing Diagram

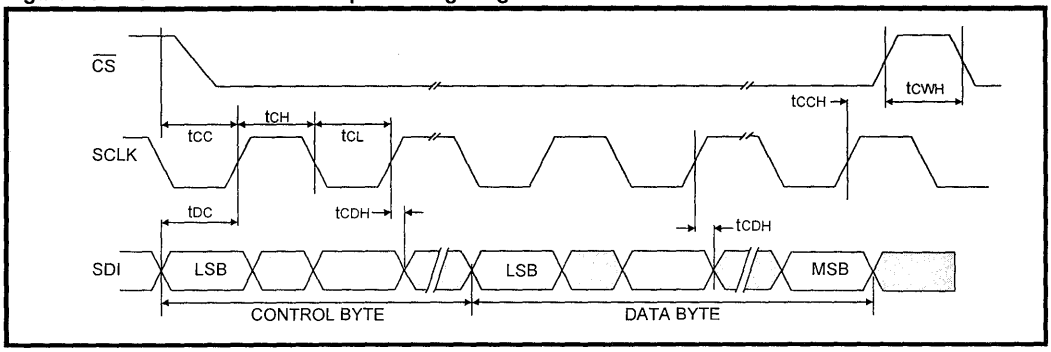
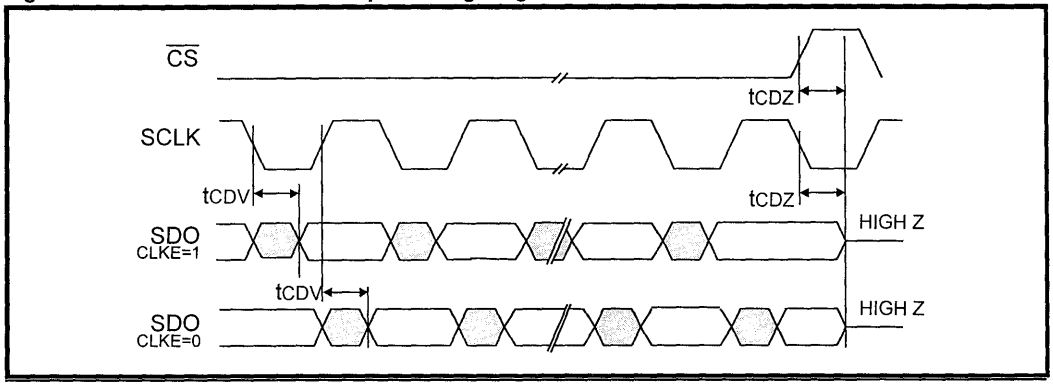


Figure 15: LXT300Z Serial Data Output Timing Diagram



LXT304A

Low-Power T1/E1 Short-Haul Transceiver with Receive JA

General Description

The LXT304A is a fully integrated low-power transceiver for both North American 1.544 Mbps (T1), and International 2.048 Mbps (E1) applications. It features a constant low output impedance transmitter allowing for high transmitter return loss in T1/E1 applications. Transmit pulse shapes (DSX-1 or E1) are selectable for various line lengths and cable types.

The LXT304A provides receive jitter attenuation starting at 3 Hz, and is microprocessor controllable through a serial interface.

It offers a variety of diagnostic features including transmit and receive monitoring. The device incorporates an on-chip crystal oscillator, and also accepts digital clock inputs. It uses an advanced double-poly, double-metal CMOS process and requires only a single 5-volt power supply.

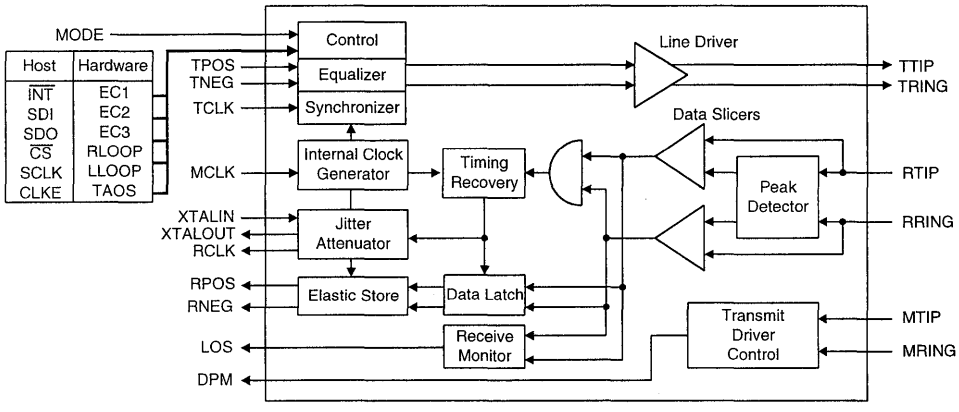
Applications

- PCM/Voice Channel Banks
- Data Channel Bank/Concentrator
- T1/E1 multiplexer
- Digital Access and Cross-connect Systems (DACS)
- Computer to PBX interface (CPI & DMI)
- High-speed data transmission lines
- Interfacing Customer Premises Equipment to a CSU
- Digital Loop Carrier (DLC) terminals

Features

- Low power consumption (400 mW maximum) 40% less than the LXT300
- Constant low output impedance transmitter regardless of data pattern (3 Ω typical)
- High transmit and receive return loss exceeds ETSI ETS 300166 and G.703 recommendations
- Meets or exceeds all industry specifications including ITU G.703, ANSI T1.403 and AT&T Pub 62411
- Compatible with most popular PCM framers
- Line driver, data recovery and clock recovery functions
- Minimum receive signal of 500 mV
- Selectable slicer levels (E1/DSX-1) improve SNR
- Programmable transmit equalizer shapes pulses to meet DSX-1 pulse template from 0 to 655 ft
- Local and remote loopback functions
- Transmit/Receive performance monitors with DPM and LOS outputs
- Receiver jitter tolerance 0.4 UI from 40 kHz to 100 kHz
- Receive jitter attenuation starting at 3 Hz meets TBR12/13 specification
- Serial control interface
- Analog/digital LOS monitor per G.775
- Available in 28-pin DIP or PLCC

LXT304A Block Diagram



PIN ASSIGNMENTS & SIGNAL DESCRIPTIONS

Figure 1: Pin Assignments

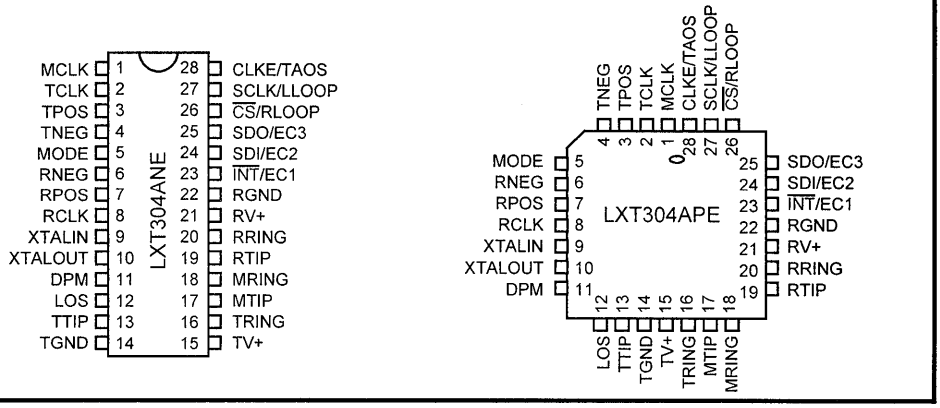


Table 1: Pin Descriptions

Pin #	Sym	I/O[1]	Description
1	MCLK	DI	**Master Clock.** A 1.544 or 2.048 MHz clock input used to generate internal clocks. Upon Loss of Signal (LOS), RCLK is derived from MCLK. If MCLK is not applied, this pin should be grounded.
2	TCLK	DI	**Transmit Clock.** Transmit clock input. TPOS and TNEG are sampled on the falling edge of TCLK. If TCLK is not supplied, the transmitter remains powered down.
3	TPOS	DI	**Transmit Positive Data.** Input for positive pulse to be transmitted on the twisted-pair line.
4	TNEG	DI	**Transmit Negative Data.** Input for negative pulse to be transmitted on the twisted-pair line.
5	MODE	DI	**Mode Select.** Setting MODE to logic 1 puts the LXT304A in the Host Mode. In the Host Mode, the serial interface is used to control the LXT304A and determine its status. Setting MODE to logic 0 puts the LXT304A in the Hardware (H/W) Mode. In the Hardware Mode, the serial interface is disabled and hard-wired pins are used to control configuration and report status.
6	RNEG	DO	**Receive Negative Data; Receive Positive Data.** Received data outputs. A signal on RNEG corresponds to receipt of a negative pulse on RTIP and RRING. A signal on RPOS corresponds to receipt of a positive pulse on RTIP and RRING. RNEG and RPOS outputs are Non-Return-to-Zero (NRZ). Both outputs are stable and valid on the rising edge of RCLK. In the Host Mode, CLKE determines the clock edge at which these outputs are stable and valid. In the Hardware Mode both outputs are stable and valid on the rising edge of RCLK.
7	RPOS	DO	

1. Entries in I/O column are: DI = Digital Input; DO = Digital Output; AI = Analog Input; AO = Analog Output; S = Supply.

Table 1: Pin Descriptions – continued

Pin #	Sym	I/O[1]	Description
8	RCLK	DO	**Recovered Clock.** This is the clock recovered from the signal received at RTIP and RRING.
9	XTALIN	AI	**Crystal Input; Crystal Output.** An external crystal operating at four times the bit rate (6.176 MHz for DSX-1, 8.192 MHz for E1 applications with an 18.7 pF load) is required to enable the jitter attenuation function of the LXT304A. These pins may also be used to disable the jitter attenuator by connecting the XTALIN pin to the positive supply through a resistor, and tying the XTALOUT pin to ground.
10	XTALOUT	AO	
11	DPM	DO	**Driver Performance Monitor.** DPM goes to a logic 1 when the transmit monitor loop (MTIP and MRING) does not detect a signal for 63 ±2 clock periods. DPM remains at logic 1 until a signal is detected.
12	LOS	DO	**Loss of Signal.** LOS goes to a logic 1 when 175 consecutive spaces have been detected. LOS returns to a logic 0 when the received signal reaches 12.5% ones density, based on 4 ones in any 32-bit period with no more than 15 consecutive zeros.
13	TTIP	AO	**Transmit Tip; Transmit Ring.** Differential Driver Outputs. These low impedance outputs achieve maximum power savings through a 1:1.15 transformer (T1), or a 1:1 (75 Ω) or 1:1.26 (120 Ω) transformer (E1) without additional components. To provide higher return loss, resistors may be used in series with a transformer as specified in Application Information.
16	TRING	AO	
14	TGND	S	**Transmit Ground.** Ground return for the transmit drivers power supply TV+.
15	TV+	S	**Transmit Power Supply.** +5 VDC power supply input for the transmit drivers. TV+ must not vary from RV+ by more than ±0.3 V.
17	MTIP	AI	**Monitor Tip; Monitor Ring.** These pins are used to monitor the tip and ring transmit outputs. The transceiver can be connected to monitor its own output or the output of another LXT304A on the board. To prevent false interrupts in the Host Mode if the monitor is not used, apply a clock signal to one of the monitor pins and tie the other monitor pin to approximately the clock's mid-level voltage. The monitor clock can range from 100 kHz to the TCLK frequency.
18	MRING	AI	
19	RTIP	AI	**Receive Tip; Receive Ring.** The AMI signal received from the line is applied at these pins. A center-tapped, center-grounded, 2:1 step-up transformer is required on these pins. Data and clock from the signal applied at these pins are recovered and output on the RPOS/RNEG and RCLK pins.
20	RRING	AI	
21	RV+	S	**Receive Power Supply.** +5 VDC power supply for all circuits except the transmit drivers. (Transmit drivers are supplied by TV+.)
22	RGND	S	**Receive Ground.** Ground return for power supply RV+.

1. Entries in I/O column are: DI = Digital Input; DO = Digital Output; AI = Analog Input; AO = Analog Output; S = Supply.

Table 1: Pin Descriptions – continued

Pin #	Sym	I/O[1]	Description
23	$\overline{INT}$	DO	**Interrupt** ***(Host Mode).*** This LXT304A Host Mode output goes Low to flag the host processor when LOS or DPM go active. $\overline{INT}$ is an open-drain output and should be tied to power supply RV+ through a resistor. $\overline{INT}$ is reset by clearing the respective register bit (LOS and/or DPM.)
	EC1	DI	**Equalizer Control 1** ***(H/W Mode).*** The signal applied at this pin in the LXT304A Hardware Mode is used in conjunction with EC2 and EC3 inputs to determine shape and amplitude of AMI output transmit pulses.
24	SDI	DI	**Serial Data In** ***(Host Mode).*** The serial data input stream is applied to this pin when the LXT304A operates in the Host Mode. SDI is sampled on the rising edge of SCLK.
	EC2	DI	**Equalizer Control 2** ***(H/W Mode).*** The signal applied at this pin in the LXT304A Hardware Mode is used in conjunction with EC1 and EC3 inputs to determine shape and amplitude of AMI output transmit pulses.
25	SDO	DO	**Serial Data Out** ***(Host Mode).*** The serial data from the on-chip register is output on this pin in the LXT304A Host Mode. If CLKE is High, SDO is valid on the rising edge of SCLK. If CLKE is Low, SDO is valid on the falling edge of SCLK. This pin goes to a high-impedance state when the serial port is being written to and when $\overline{CS}$ is High.
	EC3	DI	**Equalizer Control 3** ***(H/W Mode).*** The signal applied at this pin in the LXT304A Hardware Mode is used in conjunction with EC1 and EC2 inputs to determine shape and amplitude of AMI output transmit pulses.
26	$\overline{CS}$	DI	**Chip Select** ***(Host Mode).*** This input is used to access the serial interface in the LXT304A Host Mode. For each read or write operation, $\overline{CS}$ must transition from High to Low, and remain Low.
	RLOOP	DI	**Remote Loopback** ***(H/W Mode).*** This input controls loopback functions in the LXT304A Hardware Mode. Setting RLOOP High enables the Remote Loopback Mode. Setting both RLOOP and LLOOP causes a Reset.
27	SCLK	DI	**Serial Clock** ***(Host Mode).*** This clock is used in the LXT304A Host Mode to write data to or read data from the serial interface registers.
	LLOOP	DI	**Local Loopback** ***(H/W Mode).*** This input controls loopback functions in the LXT304A Hardware Mode. Setting LLOOP High enables the Local Loopback Mode.
28	CLKE	DI	**Clock Edge** ***(Host Mode).*** Setting CLKE High causes RPOS and RNEG to be valid on the falling edge of RCLK, and SDO to be valid on the rising edge of SCLK. When CLKE is Low, RPOS and RNEG are valid on the rising edge of RCLK, and SDO is valid on the falling edge of SCLK.
	TAOS	DI	**Transmit All Ones** ***(H/W Mode).*** When set High, TAOS causes the LXT304A (Hardware Mode) to transmit a continuous stream of marks at the TCLK frequency. Activating TAOS causes TPOS and TNEG inputs to be ignored. TAOS is inhibited during Remote Loopback.

1. Entries in I/O column are: DI = Digital Input; DO = Digital Output; AI = Analog Input; AO = Analog Output; S = Supply.

FUNCTIONAL DESCRIPTION

The LXT304A is a fully integrated PCM transceiver for both 1.544 Mbps (DSX-1) and 2.048 Mbps (E1) applications. It allows full-duplex transmission of digital data over existing twisted-pair installations.

The LXT304A transceiver interfaces with two twisted-pair lines, one twisted-pair for transmit, one twisted-pair for receive.

Power Requirements

The LXT304A is a low-power CMOS device. It operates from a single +5 V power supply which can be connected externally to both the transmitter and receiver. However, the two inputs must be within ± .3 V of each other, and decoupled to their respective grounds separately. Refer to Application Information for typical decoupling circuitry. Isolation between the transmit and receive circuits is provided internally. During normal operation, TAOS or LLOOP, the transmitter powers down if TCLK is not supplied.

Reset Operation

Upon power up, the transceiver is held static until the power supply reaches approximately 3 V. Upon crossing this threshold, the device begins a 32 ms reset cycle to calibrate the transmit and receive delay lines and lock the Phase Lock Loop to the receive line. A reference clock is required to calibrate the delay lines. The transmitter reference is provided by TCLK. MCLK provides the receiver reference. If the crystal oscillator is grounded, MCLK is used as the receiver reference clock.

The transceiver can also be reset from the Host or Hardware Mode. In Host Mode, reset is commanded by simultaneously writing RLOOP and LLOOP to the register. In Hardware Mode, reset is commanded by holding RLOOP and LLOOP High simultaneously for 200 ns. Reset is initiated on the falling edge of the reset request. In either mode, reset clears and sets all registers to 0 and then begins calibration.

Receiver

The LXT304A receives the signal input from one twisted-pair line on each side of a center-grounded transformer. Positive pulses are received at RTIP and negative pulses are received at RRING. Recovered data is output at RPOS and RNEG, and the recovered clock is output at RCLK. Refer to Test Specifications for LXT304A receiver timing.

The signal received at RPOS and RNEG is processed through the peak detector and data slicers. The peak detector samples the inputs and determines the maximum value of the received signal. A percentage of the peak value is provided to the data slicers as a threshold level to ensure optimum signal-to-noise ratio. For DSX-1 applications (determined by Equalizer Control inputs EC1 - EC3 ≠ 000) the threshold is set to 70% of the peak value. This threshold is maintained above 65% for up to 15 successive zeros over the range of specified operating conditions. For E1 applications (EC inputs = 000 or 001) the threshold is 50%.

The receiver is capable of accurately recovering signals with up to -13.6 dB of attenuation (from 2.4 V), corresponding to a received signal level of approximately 500 mV. Maximum line length is 1500 feet of ABAM cable (approximately 6 dB of attenuation). Regardless of received signal level, the peak detectors are held above a minimum level of .3 V to provide immunity from impulsive noise.

After processing through the data slicers, the received signal is routed to the data and clock recovery sections, and to the receive monitor. The data and clock recovery circuits are highly tolerant with an input jitter tolerance significantly better than required by Pub 62411. Refer to Test Specifications for additional information.

The receiver monitor loads a digital counter at the RCLK frequency. The count is incremented each time a zero is received, and reset to zero each time a one (mark) is received. Upon receipt of 175 consecutive zeros the LOS pin goes high, and a smooth transition replaces the RCLK output with the MCLK. (If MCLK is not supplied the RCLK output will be replaced with the centered crystal clock.) The LOS pin is reset when the received signal reaches 12.5% ones density (4 marks in 32 bits) with no more than 15 consecutive zeros.

Recovered clock signals are supplied to the Jitter Attenuator and the data latch. The recovered data is passed to the Elastic Store where it is buffered and synchronized with the dejittered recovered clock (RCLK).

Jitter Attenuation

Jitter attenuation of the LXT304A clock and data outputs is provided by a Jitter Attenuation Loop (JAL) and an Elastic Store (ES). An external crystal oscillating at 4 times the bit rate provides clock stabilization. Refer to Application Information for crystal specifications. The ES is a 32 x 2-

bit register. Recovered data is clocked into the ES with the recovered clock signal, and clocked out of the ES with the dejittered clock from the JAL. When the bit count in the ES is within two bits of overflowing or underflowing, the ES adjusts the output clock by 1/8 of a bit period. The ES produces an average delay of 16 bits in the receive path.

Transmitter

Data received for transmission onto the line is clocked serially into the device at TPOS and TNEG. Input synchronization is supplied by the transmit clock (TCLK). If TCLK is not supplied the transmitter remains powered down, except during remote loopback. Refer to Test Specifications for master and transmit clock timing characteristics.

The transmitted pulse shape is determined by Equalizer Control signals EC1 through EC3 as shown in Table 2. Equalizer Control signals may be hardwired in the Hardware mode, or input as part of the serial data stream (SDI) in the Host mode. Shaped pulses are applied to the AMI line driver for transmission onto the line at TTIP and TRING. The line driver provides a constant low output impedance of 3 Ω (typical). This well controlled output impedance provides excellent return loss (> 18 dB) when used with external 9.1 Ω precision resistors (± 1% accuracy) in series with a transmit transformer with a turns ratio of 1:2.3 (± 2% accuracy). Series resistors also provide increased surge protection and reduce short circuit current flow.

Pulses can be shaped for either 1.544 or 2.048 Mbps applications. 1.544 Mbps pulses for DSX-1 applications can be programmed to match line lengths from 0 to 655 feet of ABAM cable. The LXT304A also matches FCC and ECSA specifications for CSU applications. A 1:1.15 transmit transformer is used for 1.544 Mbps systems. For higher return loss in DSX-1 applications, use 9.1 Ω resistors in series with a 1:2.3 transmit transformer.

2.048 Mbps pulses can drive coaxial or shielded twisted-pair lines. For E1 systems, a 1:2 transmit transformer and series resistors are recommended. This design meets or exceeds all ITU and ETSI specifications for transmit and receive return loss. A 1:1 or 1:1.26 transformer may be used without series resistors.

Driver Performance Monitor

The transceiver incorporates a Driver Performance Monitor (DPM) in parallel with TTIP and TRING at the output transformer. The DPM output goes High upon detection of 63 consecutive zeros. It is reset when a one is detected on the transmit line, or when a reset command is received.

Line Code

The LXT304A transmits data as a 50% AMI line code as shown in Figure 2. The output driver maintains a constant low output impedance regardless of whether it is driving marks or spaces.

Operating Modes

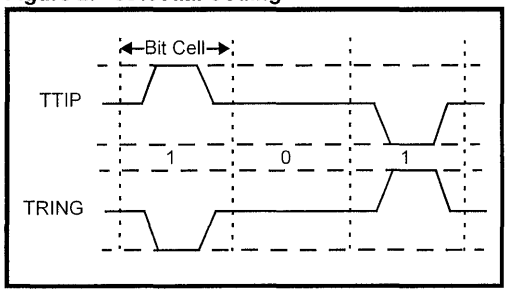
The LXT304A can be controlled through hard-wired pins (Hardware Mode) or by a microprocessor through a serial interface (Host Mode). The mode of operation is set by the MODE pin logic level. The LXT304A can also be commanded to operate in one of several diagnostic modes.

Table 2: Equalizer Control Inputs

EC3	EC2	EC1	Line Length[1]	Cable Loss[2]	Application	Bit Rate
0	1	1	0 ~ 133 ft ABAM	0.6 dB	DSX-1	1.544 Mbps
1	0	0	133 ~ 266 ft ABAM	1.2 dB		
1	0	1	266 ~ 399 ft ABAM	1.8 dB		
1	1	0	399 ~ 533 ft ABAM	2.4 dB		
1	1	1	533 ~ 655 ft ABAM	3.0 dB		
0	0	0	ITU Recommendation G.703		E1 - Coax (75 Ω)	2.048 Mbps
0	0	1			E1 - Twisted-pair (120 Ω)	
0	1	0	FCC Part 68, Option A		CSU (DS-1)	1.544 Mbps

1. Line length from transceiver to DSX-1 cross-connect point.
2. Maximum cable loss at 772 kHz.

Figure 2: 50% AMI Coding



Host Mode Operation

To allow a host microprocessor to access and control the LXT304A through the serial interface, MODE is set High.

The serial interface (SDI/SDO) uses a 16-bit word consisting of an 8-bit Command/Address byte and an 8-bit Data byte. Figure 3 shows the serial interface data structure and relative timing.

The Host Mode provides a latched Interrupt output ($\overline{INT}$) which is triggered by a change in the Loss of Signal (LOS) and/or Driver Performance Monitor (DPM) bits. The Interrupt is cleared when the interrupt condition no longer exists, and the host processor enables the respective bit in the serial input data byte. Host Mode also allows control of the serial data and receive data output timing. The Clock Edge (CLKE) signal determines when these outputs are valid, relative to the Serial Clock (SCLK) or RCLK as listed in Table 3.

Table 3: Valid CLKE Settings

CLKE	Output	Clock	Valid Edge
LOW	RPOS RNEG SDO	RCLK RCLK SCLK	Rising Rising Falling
HIGH	RPOS RNEG SDO	RCLK RCLK SCLK	Falling Falling Rising

Table 4: LXT304A Serial Data Output Bits (See Figure 4)

Bit D5	Bit D6	Bit D7	Status
0	0	0	Reset has occurred, or no program input.
0	0	1	TAOS is active.
0	1	0	Local Loopback is active.
0	1	1	TAOS and Local Loopback are active.
1	0	0	Remote Loopback is active.
1	0	1	DPM has changed state since last Clear DPM occurred.
1	1	0	LOS has changed state since last Clear LOS occurred.
1	1	1	LOS and DPM have both changed state since last Clear DPM and Clear LOS occurred.

The LXT304A serial port is addressed by setting bit A4 in the Address/Command byte, corresponding to address 16. The LXT304A contains only a single output data register so no complex chip addressing scheme is required. The register is accessed by causing the Chip Select ($\overline{CS}$) input to transition from High to Low. Bit 1 of the serial Address/Command byte provides Read/Write control when the chip is accessed. A logic 1 indicates a read operation, and a logic 0 indicates a write operation. Table 4 lists serial data output bit combinations for each status. Serial data I/O timing characteristics are shown in the Test Specifications section.

Hardware Mode Operation

In Hardware Mode the transceiver is accessed and controlled through individual pins. With the exception of the INT and CLKE functions, Hardware Mode provides all the functions provided in the Host Mode. In the Hardware Mode RPOS and RNEG outputs are valid on the rising edge of RCLK. To operate in Hardware Mode, MODE must be set Low. Equalizer Control signals (EC1 through EC3) are input on the Interrupt, Serial Data In and Serial Data Out pins. Diagnostic control for Remote Loopback (RLOOP), Local Loopback (LLOOP), and Transmit All Ones (TAOS) modes is provided through the individual pins used to control serial interface timing in the Host Mode.

Diagnostic Mode Operation

Transmit All Ones

In Transmit All Ones (TAOS) mode the TPOS and TNEG inputs to the transceiver are ignored. The transceiver transmits a continuous stream of ones when the TAOS mode is activated. TAOS can be commanded simultaneously with Local Loopback, but is inhibited during Remote Loopback.

Remote Loopback

In Remote Loopback (RLOOP) mode, the transmit data and clock inputs (TPOS, TNEG and TCLK) are ignored. The RPOS and RNEG outputs are looped back through the transmit circuits and output on TTIP and TRING at the RCLK frequency. Receiver circuits are unaffected by the RLOOP command and continue to output the RPOS, RNEG and RCLK signals received from the twisted-pair line.

Local Loopback

In Local Loopback (LLOOP) mode, the receiver circuits are inhibited. The transmit data and clock inputs (TPOS, TNEG and TCLK) are looped back onto the receive data and clock outputs (RPOS, RNEG and RCLK) through the Rx jitter attenuator. The transmitter circuits are unaffected by the LLOOP command. The TPOS and TNEG inputs (or a stream of ones if the TAOS command is active) will be transmitted normally.

Figure 3: LXT304A Serial Interface Data Structure

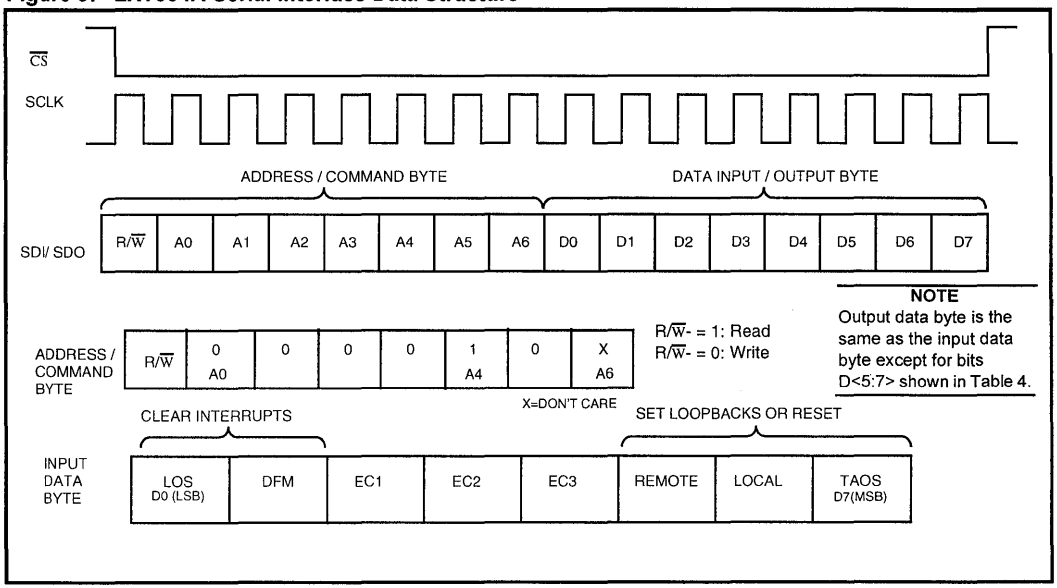


Table 5: LXT304A Crystal Specifications (External)

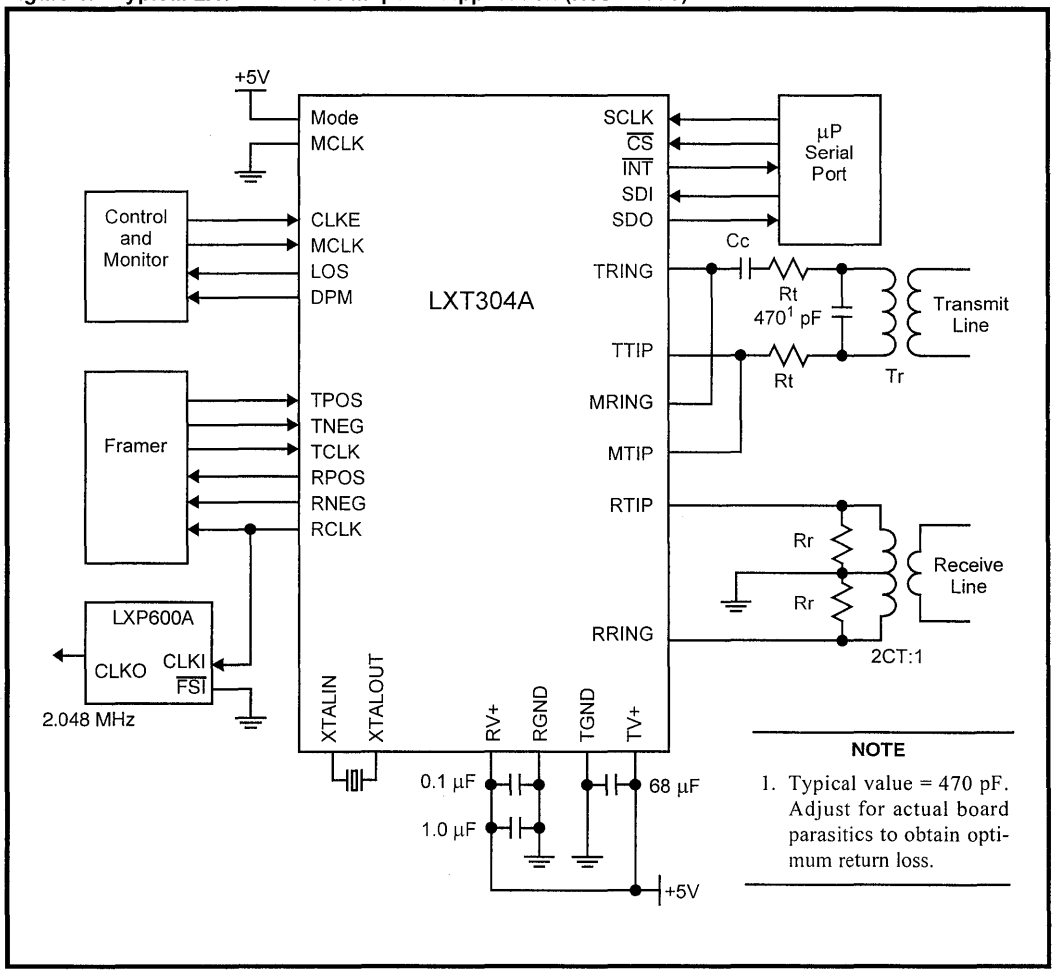
Parameter	T1	E1
Frequency	6.176 MHz	8.192 MHz
Frequency stability	± 20 ppm @ 25 °C ± 25 ppm from -40 °C to 85 °C (Ref 25 °C reading)	± 20 ppm @ 25 °C ± 25 ppm from -40 °C to +85 °C (Ref 25 °C reading)
Pullability	CL = 11 pF to 18.7 pF, +ΔF = 175 to 195 ppm CL = 18.7 pF to 34 pF, -ΔF = 175 to 195 ppm	CL = 11 pF to 18.7 pF, +ΔF = 95 to 115 ppm CL = 18.7 pF to 34 pF, -ΔF = 95 to 115 ppm
Effective series resistance	40 Ω Maximum	30 Ω Maximum
Crystal cut	AT	AT
Resonance	Parallel	Parallel
Maximum drive level	2.0 mW	2.0 mW
Mode of operation	Fundamental	Fundamental
Crystal holder	HC49 (R3W), C_O = 7 pF maximum C_M = 17 fF typical	HC49 (R3W), C_O = 7 pF maximum C_M = 17 fF typical

APPLICATION INFORMATION

1.544 Mbps T1 Interface Application

Figure 4 is a typical 1.544 Mbps T1 application. The LXT304A is shown in the Host Mode with a T1/ESF framer providing the digital interface with the host controller. Both devices are controlled through the serial interface. An LXP600A Clock Adapter (CLAD) provides the 2.048 MHz system backplane clock, locked to the recovered 1.544 MHz clock signal. The power supply inputs are tied to a common bus with appropriate decoupling capacitors installed (68 µF on the transmit side, 1.0 µF and 0.1 µF on the receive side).

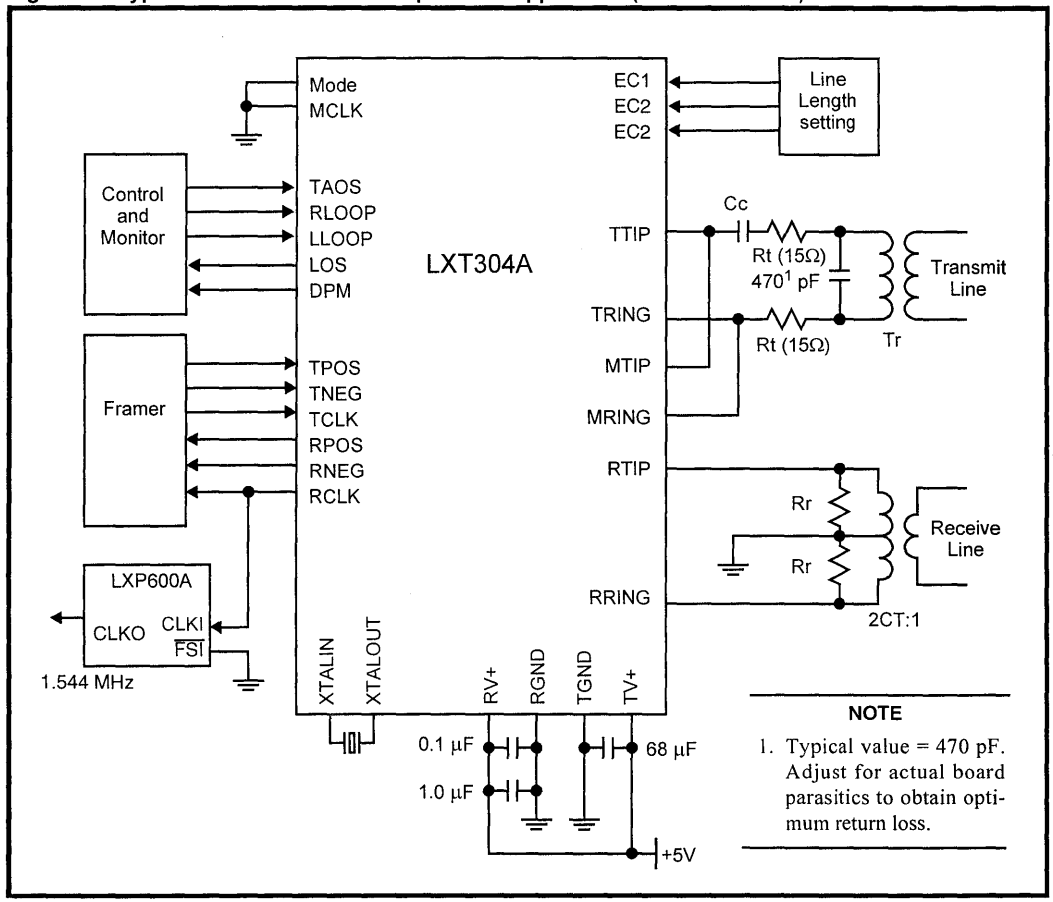
Figure 4: Typical LXT304A 1.544 Mbps T1 Application (Host Mode)



2.048 Mbps E1 Interface Applications

Figure 5 is a 2.048 Mbps E1 TWP application using 15 Ω Rt resistors in line with the transmit transformer to provide high return loss and surge protection. When high return loss is not a critical factor, a 1:1 or 1:1.26 transformer without in-line resistors provides maximum power savings. The LXT304A is shown in Hardware Mode with a typical E1/CRC4 Framer. The hard-wired control lines for TAOS, LLOOP and RLOOP are individually controllable, and the LLOOP and RLOOP lines are also tied to a single control for the Reset function. This configuration is illustrated with a crystal in place to enable the LXT304A Jitter Attenuation Loop, and a single power supply bus.

Figure 5: Typical LXT304A E1 2.048 Mbps 120 Ω Application (Hardware Mode)



D4 Channel Bank Applications

Existing D4 Channel Bank architectures frequently employ: (1) a plug-in card for T1 pulse generation (6.0 V peak); and (2) a separate card for pulse shaping and Line Build-Out (LBO). The LXT304A integrates the functions of both cards on a single chip producing a DSX-1 compatible, 3.0 V peak output pulse with a standard transformer. In new designs, the LXT304A can replace two cards with one. However, the LXT304A is also compatible with existing dual-card architectures. With an appropriate output transformer, the LXT304A can produce full 6.0 V peak amplitude pulses suitable for D4 Channel Bank applications with separate pulse shaping/LBO cards.

To achieve the 6.0 V peak output, the FCC Part 68-010 Equalizer Code setting is used. (EC = 010.) With the standard 1:1.15 transformer, this code produces a 3.0 V peak pulse. However, doubling the transformer turns ratio to 1:2.30 produces the desired 6.0 V peak pulse.

Table 6: T1/E1 Input/Output Configurations

Bit Rate (Mbps)	Crystal XTAL	Cable (Ω)	Rr[2] (Ω)	EC3/2/1	Transmit Transformer[1] (Tr)	Rt[2] (Ω)	Typical TX Return Loss[3] (dB)	Cc (μF)
1.544 (T1)	LXC6176	100	200	0/1/1 - 1/1/1	1:1.15	0	0.5	0.47
					1:2	9.1	18	0
					1:2.3	9.1	18	0
				0/1/0[4]	1:2.3	0	0[4]	0.47
2.048 (E1)	LXC8192	120	240	0/0/0	1:1.26	0	0.5	0.47
				0/0/0	1:2	9.1	12	0
				0/0/1	1:1	0	0.5	0.47
				0/0/1	1:2	1.5	18	0
		75	150	0/0/0	1:1	0	0.5	0.47
				0/0/0	1:2	9.1	18	0
				0/0/1	1:1	10	5	0
				0/0/1	1:2	14.3	10	0

1. Transformer turns ratio accuracy is ± 2%.
2. Rr and Rt values are ± 1%.
3. Typical return loss, 51 kHz to 3.072 MHz band.
4. D4 Channel Bank application.

TEST SPECIFICATIONS

NOTE

The minimum and maximum values in Tables 7 through 13 and Figures 6 through 11 represent the performance specifications of the LXT304A and are guaranteed by test, except where noted by design.

Table 7: Absolute Maximum Ratings

Parameter	Sym	Min	Max	Units
DC supply (referenced to GND)	RV+, TV+	–0.3	6.0	V
Input voltage, any pin[1]	V_{IN}	RGND - 0.3	RV+ + 0.3	V
Input current, any pin[2]	I_{IN}	-10	10	mA
Storage temperature	T_{STG}	-65	150	°C

CAUTION

Operations at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

1. Excluding RTIP and RRING which must stay between -6V and (RV+ + 0.3) V.
2. Transient currents of up to 100 mA will not cause SCR latch up. TTIP, TRING, TV+ and TGND can withstand a continuous current of 100 mA.

Table 8: Recommended Operating Conditions and Characteristics

Parameter	Sym	Min	Typ	Max	Units
DC supply[1]	RV+, TV+	4.75	5.0	5.25	V
Ambient operating temperature	T_A	-40	25	85	° C

1. TV+ must not exceed RV+ by more than 0.3 V.

Table 9: Electrical Characteristics (Under Recommended Operating Conditions)

Parameter	Sym	Min	Max	Units	Test Conditions
Total power dissipation[1,3]	P_D	–	400	mW	100% ones density & maximum line length @ 5.25 V
High level input voltage[2,3] (pins 1-5, 10, 23-28)	V_{IH}	2.0	–	V	
Low level input voltage[2,3] (pins 1-5, 10, 23-28)	V_{IL}	–	0.8	V	
High level output voltage[2,3] (pins 6-8, 11, 12, 23, 25)	V_{OH}	2.4	–	V	I_{OUT} = -400 µA

1. Power dissipation while driving 75 Ω load over operating temperature range. Includes device and load. Digital input levels are within 10% of the supply rails and digital outputs are driving a 50 pF capacitive load.
2. Functionality of pins 23 and 25 depends on mode. See Host/Hardware Mode descriptions.
3. Output drivers will output CMOS logic levels into CMOS loads.
4. Except MTIP and MRING ILL = ± 50 µA.

Table 9: Electrical Characteristics (Under Recommended Operating Conditions) – continued

Parameter	Sym	Min	Max	Units	Test Conditions
Low level output voltage[2,3] (pins 6-8, 11, 12, 23, 25)	V_{OL}	–	0.4	V	I_{OUT} = 1.6 mA
Input leakage current[4]	I_{LL}	-10	+10	µA	
Three-state leakage current[2] (pin 25)	I_{3L}	-10	+10	µA	

1. Power dissipation while driving 75 Ω load over operating temperature range. Includes device and load. Digital input levels are within 10% of the supply rails and digital outputs are driving a 50 pF capacitive load.
2. Functionality of pins 23 and 25 depends on mode. See Host/Hardware Mode descriptions.
3. Output drivers will output CMOS logic levels into CMOS loads.
4. Except MTIP and MRING ILL = ± 50 µA.

Table 10: Analog Characteristics (Under Recommended Operating Conditions)

Parameter		Min	Typ[1]	Max	Units	Test Conditions
AMI output pulse amplitudes	DSX-1	2.4	3.0	3.6	V	measured at the DSX
	E1	2.7	3.0	3.3	V	measured at line side
Recommended output load at TTIP and TRING		–	75	–	Ω	
Jitter added by the transmitter[2]	10 Hz - 8 kHz	–	–	0.01	UI	
	8 kHz - 40 kHz	–	–	0.025	UI	
	10 Hz - 40 kHz	–	–	0.025	UI	
	Broad Band	–	–	0.05	UI	
Sensitivity below DSX	(0 dB = 2.4 V)	13.6	–	–	dB	
		500	–	–	mV	
Loss of Signal threshold		–	0.3	–	V	
Data decision threshold	DSX-1	63	70	77	% peak	
	E1	43	50	57	% peak	
Allowable consecutive zeros before LOS		160	175	190	–	
Input jitter tolerance	10 kHz - 100 kHz	0.4	–	–	UI	
Jitter attenuation curve corner frequency[3]		–	3	–	Hz	
Minimum return loss[4,5]		**Transmit** Min	Typ	**Receive** Min	Typ	dB
	51 kHz - 102 kHz	18	–	20	–	dB
	102 kHz - 2.048 kHz	18	–	20	–	dB
	2.048 kHz - 3.072 kHz	18	–	20	–	dB

1. Typical values are measured at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Input signal to TCLK is jitter-free.
3. Circuit attenuates jitter at 20 dB/decade above the corner frequency.
4. In accordance with ITU G.703/ETS 300166 return loss specifications when wired per Figure 7 (E1).
5. Guaranteed by design.

Figure 6: Typical Receive Input Jitter Tolerance (Loop Mode)

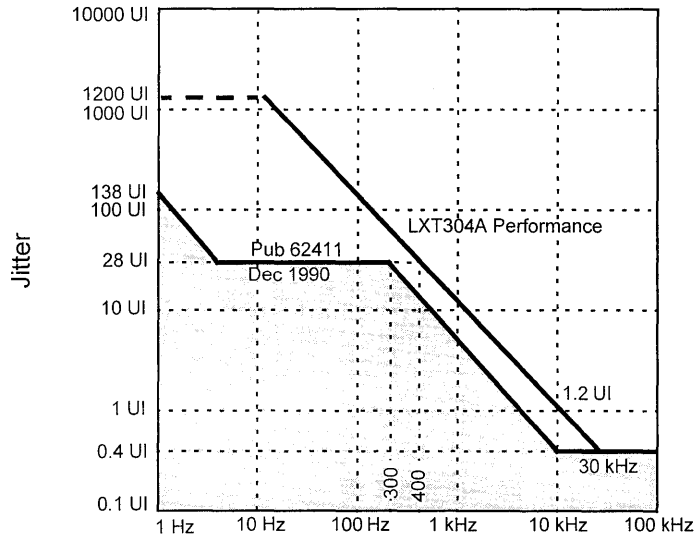


Figure 7: LXT304A Receive Jitter Transfer Performance (Typical)

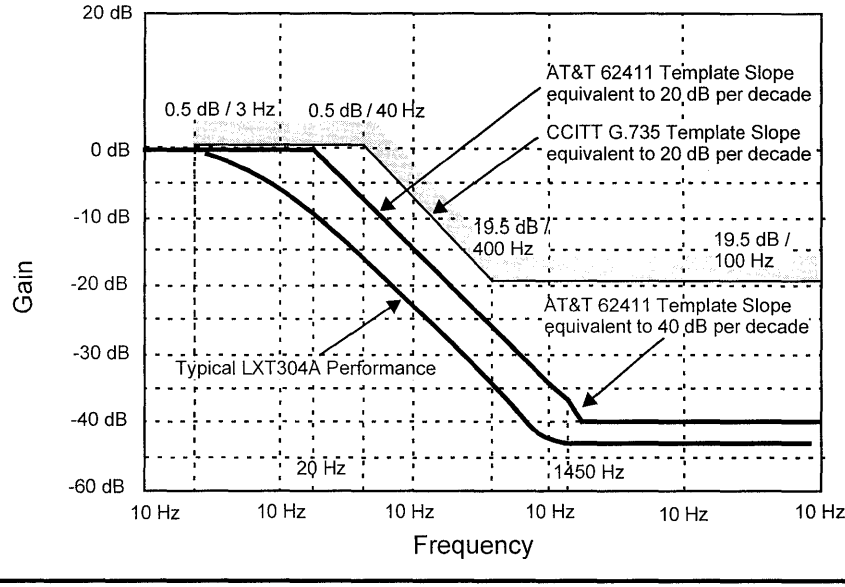


Table 11: LXT304A Receive Timing Characteristics (See Figure 8)

Parameter		Sym	Min	Typ[1]	Max	Units	Test Conditions
Receive clock duty cycle		RCLKd	40	–	60	%	
Receive clock pulse width	DSX-1	t_{PW}	–	324	–	ns	
	E1	t_{PW}	–	244	–	ns	
RPOS/RNEG to RCLK rising setup time	DSX-1	t_{SUR}	–	274	–	ns	
	E1	t_{SUR}	–	194	–	ns	
RCLK rising to RPOS/RNEG hold time	DSX-1	t_{HR}	–	274	–	ns	
	E1	t_{HR}	–	194	–	ns	

1. Typical values are at 25 °C and are for design aid only; they are not guaranteed and not subject to production testing.

Figure 8: LXT304A Receive Clock Timing Diagram

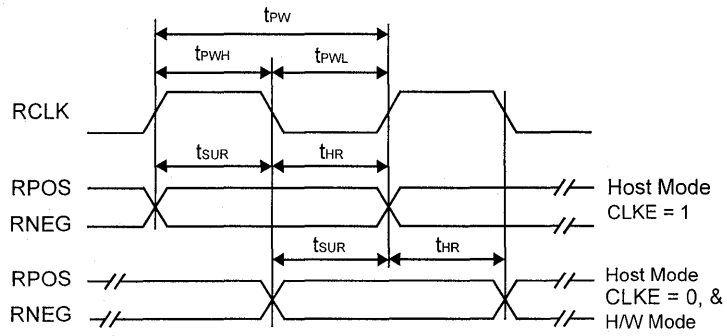


Table 12: LXT304A Master Clock and Transmit Timing Characteristics
(See Figure 9)

Parameter		Sym	Min	Typ[1]	Max	Units
Master clock frequency	DSX-1	MCLK	–	1.544	–	MHz
	E1	MCLK	–	2.048	–	MHz
Master clock tolerance		MCLKt	–	±100	–	ppm
Master clock duty cycle		MCLKd	40	–	60	%
Crystal frequency	DSX-1	fc	–	6.176	–	MHz
	E1	fc	–	8.192	–	MHz
Transmit clock frequency	DSX-1	TCLK	–	1.544	–	MHz
	E1	TCLK	–	2.048	–	MHz
Transmit clock tolerance		TCLKt	–	±50	–	ppm
Transmit clock duty cycle		TCLKd	10	–	90	%
TPOS/TNEG to TCLK setup time		t_{SUT}	25	–	–	ns
TCLK to TPOS/TNEG hold time		t_{HT}	25	–	–	ns

1. Typical values are at 25 °C and are for design aid only; they are not guaranteed and not subject to production testing.

Figure 9: LXT304A Transmit Clock Timing Diagram

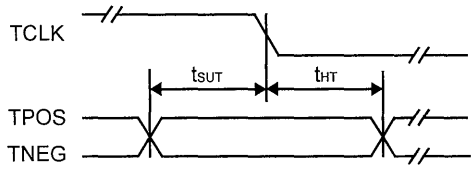


Table 13: LXT304A Serial I/O Timing Characteristics (See Figures 10 and 11)

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Rise/Fall time - any digital output	t_{RF}	–	–	100	ns	Load 1.6 mA, 50 pF
SDI to SCLK setup time	t_{DC}	50	–	–	ns	
SCLK to SDI hold time	t_{CDH}	50	–	–	ns	
SCLK low time	t_{CL}	240	–	–	ns	
SCLK high time	t_{CH}	240	–	–	ns	
SCLK rise and fall time	t_R, t_F	–	–	50	ns	
$\overline{CS}$ to SCLK setup time	t_{CC}	50	–	–	ns	
SCLK to $\overline{CS}$ hold time	t_{CCH}	50	–	–	ns	
$\overline{CS}$ inactive time	t_{CWH}	250	–	–	ns	
SCLK to SDO valid	t_{CDV}	–	–	200	ns	
SCLK falling edge or $\overline{CS}$ rising edge to SDO high Z	t_{CDZ}	–	100	–	ns	

1. Typical values are at 25° C and are for design aid only; they are not guaranteed and not subject to production testing.

Figure 10: LXT304A Serial Data Input Timing Diagram

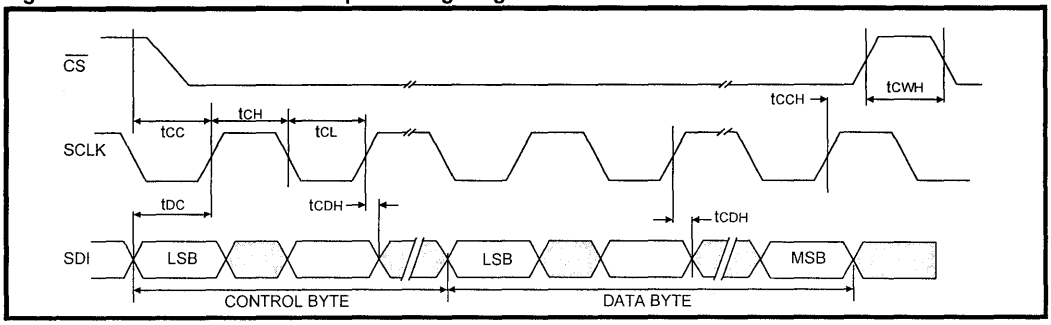
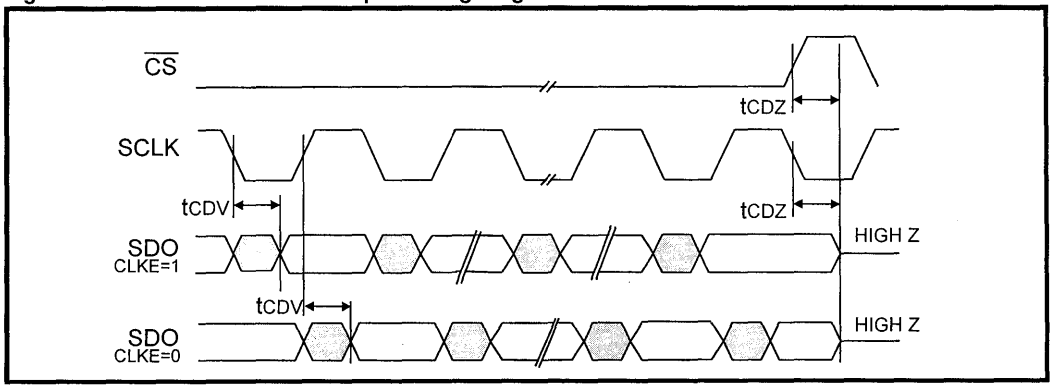


Figure 11: LXT304A Serial Data Output Timing Diagram



LXT305A

Integrated T1/E1 Short-Haul Transceiver with Transmit JA

General Description

The LXT305A is a fully integrated transceiver for both North American 1.544 Mbps (T1) and International 2.048 Mbps (E1) applications. Transmit pulse shapes (T1 or E1) are selectable for various line lengths and cable types.

The LXT305A provides transmit jitter attenuation starting at 3 Hz, and is microprocessor controllable through a serial interface. It is especially well suited for applications in which the T1/E1 signals are demultiplexed from a higher rate service such as DS3 or SONET/SDH. This demultiplexing results in a gapped clock which the 305A smooths out.

The LXT305A, an advanced double-poly, double-metal CMOS device, requires only a single 5-volt power supply.

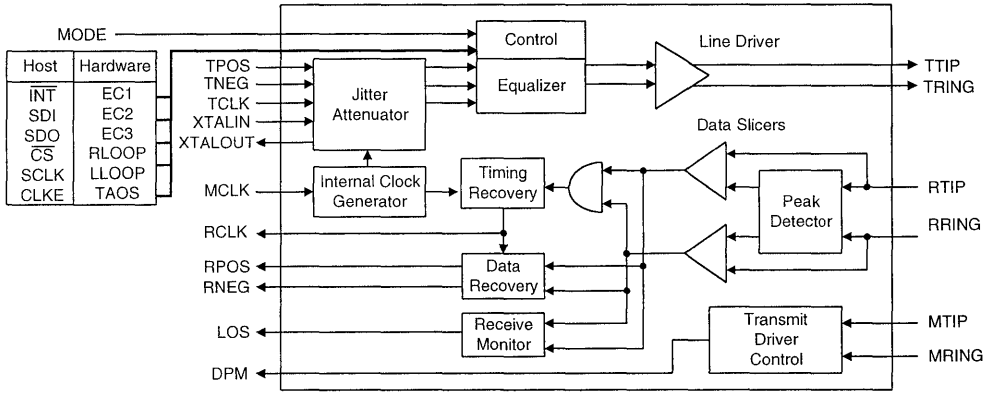
Applications

- SDH / SONET Equipment
- M13 Multiplexers
- Digital microwave Radio
- PCM / Voice Channel Banks
- Data Channel Bank / Concentrator
- T1 / E1 multiplexer
- Digital Access and Cross-connect Systems (DACS)
- Computer to PBX interface (CPI & DMI)
- High-speed data transmission lines
- Interfacing Customer Premises Equipment to a CSU
- Digital Loop Carrier (DLC) terminals

Features

- Low power consumption (400 mW maximum)
- Constant low output impedance transmitter, regardless of data pattern (3 Ω typical)
- High transmit and receive return loss exceeds ETS 300166 and G.703
- Compatible with most popular PCM framers
- Line driver, data recovery and clock recovery functions
- Minimum receive signal of 500 mV
- Selectable slicer levels (T1/E1) improve SNR
- Programmable transmit equalizer shapes pulses to meet DSX-1 pulse template from 0 to 655 ft
- Local and remote loopback functions
- Transmit Driver Performance Monitor (DPM) output
- Receive monitor with analog/digital Loss of Signal (LOS) output per G.775
- Receiver jitter tolerance 0.4 UI from 40 kHz to 100 kHz
- Transmit jitter attenuation starting at 3 Hz
- Serial control interface
- Available in 28-pin DIP and PLCC

LXT305A Block Diagram



PIN ASSIGNMENTS AND SIGNAL DESCRIPTIONS

Figure 1: Pin Assignments

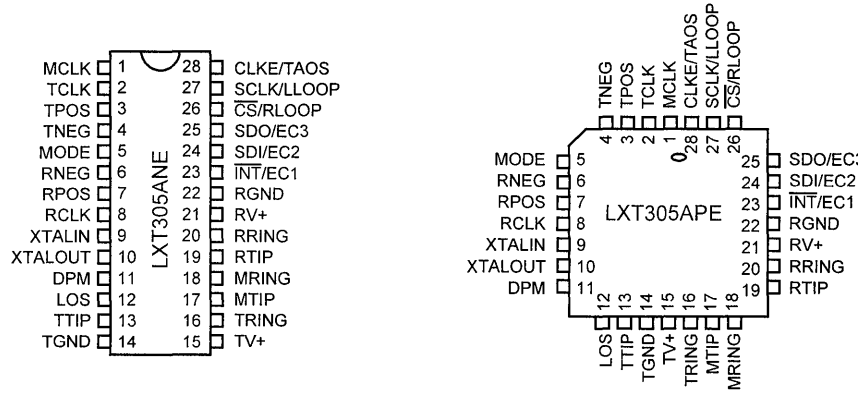


Table 1: Pin Descriptions

Pin #	Sym	I/O[1]	Description
1	MCLK	DI	**Master Clock.** A 1.544 or 2.048 MHz clock input used to generate internal clocks. Upon Loss of Signal (LOS), RCLK is derived from MCLK. If MCLK is not applied, this pin should be grounded.
2	TCLK	DI	**Transmit Clock.** Transmit clock input. TPOS and TNEG are sampled on the falling edge of TCLK.
3	TPOS	DI	**Transmit Positive Data.** Input for positive pulse to be transmitted on the twisted-pair line.
4	TNEG	DI	**Transmit Negative Data.** Input for negative pulse to be transmitted on the twisted-pair line.
5	MODE	DI	**Mode Select.** Setting MODE High puts the LXT305A in the Host Mode. In the Host Mode, the serial interface is used to control the LXT305A and determine its status. Setting MODE Low puts the LXT305A in the Hardware (H/W) Mode. In the Hardware Mode, the serial interface is disabled and hard-wired pins are used to control configuration and report status.
6	RNEG	DO	**Receive Negative Data; Receive Positive Data.** Received data outputs. A signal on RNEG corresponds to receipt of a negative pulse on RTIP and RRING. A signal on RPOS corresponds to receipt of a positive pulse on RTIP and RRING. RNEG and RPOS outputs are Non-Return-to-Zero (NRZ). Both outputs are stable and valid on the rising edge of RCLK. In the Host Mode, CLKE determines the clock edge at which these outputs are stable and valid. In the Hardware Mode both outputs are stable and valid on the rising edge of RCLK.
7	RPOS	DO	

1. Entries in I/O column are: DI = Digital Input; DO = Digital Output; AI = Analog Input; AO = Analog Output; S = Supply.

Table 1: Pin Descriptions – continued

Pin #	Sym	I/O[1]	Description
8	RCLK	DO	**Recovered Clock.** This is the clock recovered from the signal received at RTIP and RRING.
9	XTALIN	AI	**Crystal Input; Crystal Output.** An external crystal operating at four times the bit rate (6.176 MHz for DSX-1, 8.192 MHz for E1 applications with an 18.7pF load) is required to enable the jitter attenuation function of the LXT305A. These pins may also be used to disable the jitter attenuator by connecting the XTALIN pin to the positive supply through a resistor, and tying the XTALOUT pin to ground.
10	XTALOUT	AO	
11	DPM	DO	**Driver Performance Monitor.** DPM goes High when the transmit monitor loop (MTIP and MRING) does not detect a signal for 63 ±2 clock periods. DPM remains High until a signal is detected.
12	LOS	DO	**Loss of Signal.** LOS goes High when 175 consecutive spaces have been detected. LOS returns Low when the received signal reaches 12.5% ones density (based on 4 ones in any 32-bit period) with no more than 15 consecutive zeros.
13	TTIP	AO	**Transmit Tip; Transmit Ring.** Differential Driver Outputs. These low impedance outputs achieve maximum power savings through a 1:1.15 transformer (T1), or a 1:1 (75 ý) or 1:1.26 (120 ý) transformer (E1) without additional components. To provide higher return loss, resistors may be used in series with a transformer as specified in Application Information.
16	TRING	AO	
14	TGND	S	**Transmit Ground.** Ground return for the transmit drivers power supply TV+.
15	TV+	S	**Transmit Power Supply.** +5 VDC power supply input for the transmit drivers. TV+ must not vary from RV+ by more than ±0.3 V.
17	MTIP	AI	**Monitor Tip; Monitor Ring.** These pins are used to monitor the tip and ring transmit outputs. The transceiver can be connected to monitor its own output or the output of another LXT305A on the board. Host Mode only: To prevent false interrupts in the Host Mode if the monitor is not used, apply a clock signal to one of the monitor pins and tie the other monitor pin to approximately the clock's mid-level voltage. The monitor clock can range from 100 kHz to the TCLK frequency.
18	MRING	AI	
19	RTIP	AI	**Receive Tip; Receive Ring.** The AMI signal received from the line is applied at these pins. A center-tapped, center-grounded, 2:1 step-up transformer is required on these pins. Data and clock from the signal applied at these pins are recovered and output on the RPOS/RNEG and RCLK pins.
20	RRING	AI	
21	RV+	S	**Receive Power Supply.** +5 VDC power supply for all circuits except the transmit drivers. (Transmit drivers are supplied by TV+.)
22	RGND	S	**Receive Ground.** Ground return for power supply RV+.

1. Entries in I/O column are: DI = Digital Input; DO = Digital Output; AI = Analog Input; AO = Analog Output; S = Supply.

Table 1: Pin Descriptions – continued

Pin #	Sym	I/O[1]	Description
23	$\overline{INT}$	DO	**Interrupt** ***(Host Mode).*** This LXT305A Host Mode output goes Low to flag the host processor when LOS or DPM go active. $\overline{INT}$ is an open-drain output and should be tied to power supply RV+ through a resistor. $\overline{INT}$ is reset by clearing the respective register bit (LOS and/or DPM).
	EC1	DI	**Equalizer Control 1** ***(H/W Mode).*** The signal applied at this pin in the LXT305A Hardware Mode is used in conjunction with EC2 and EC3 inputs to determine shape and amplitude of AMI output transmit pulses.
24	SDI	DI	**Serial Data In** ***(Host Mode).*** The serial data input stream is applied to this pin when the LXT305A operates in the Host Mode. SDI is sampled on the rising edge of SCLK.
	EC2	DI	**Equalizer Control 2** ***(H/W Mode).*** The signal applied at this pin in the LXT305A Hardware Mode is used in conjunction with EC1 and EC3 inputs to determine shape and amplitude of AMI output transmit pulses.
25	SDO	DO	**Serial Data Out** ***(Host Mode).*** The serial data from the on-chip register is output on this pin in the LXT305A Host Mode. If CLKE is High, SDO is valid on the rising edge of SCLK. If CLKE is Low SDO is valid on the falling edge of SCLK. This pin goes to a high-impedance state when the serial port is being written to and when $\overline{CS}$ is High.
	EC3	DI	**Equalizer Control 3** ***(H/W Mode).*** The signal applied at this pin in the LXT305A Hardware Mode is used in conjunction with EC1 and EC2 inputs to determine shape and amplitude of AMI output transmit pulses.
26	$\overline{CS}$	DI	**Chip Select** ***(Host Mode).*** This input is used to access the serial interface in the LXT305A Host Mode. For each read or write operation, $\overline{CS}$ must transition from High to Low, and remain Low.
	RLOOP	DI	**Remote Loopback** ***(H/W Mode).*** This input controls loopback functions in the LXT305A Hardware Mode. Setting RLOOP High enables the Remote Loopback Mode. Setting both RLOOP and LLOOP High causes a Reset.
27	SCLK	DI	**Serial Clock** ***(Host Mode).*** This clock is used in the LXT305A Host Mode to write data to or read data from the serial interface registers.
	LLOOP	DI	**Local Loopback** ***(H/W Mode).*** This input controls loopback functions in the LXT305A Hardware Mode. Setting LLOOP High enables the Local Loopback Mode.
28	CLKE	DI	**Clock Edge** ***(Host Mode).*** Setting CLKE High causes RPOS and RNEG to be valid on the falling edge of RCLK, and SDO to be valid on the rising edge of SCLK. When CLKE is Low, RPOS and RNEG are valid on the rising edge of RCLK, and SDO is valid on the falling edge of SCLK.
	TAOS	DI	**Transmit All Ones** ***(H/W Mode).*** When set High, TAOS causes the LXT305A (Hardware Mode) to transmit a continuous stream of marks at the MCLK frequency. Activating TAOS causes TPOS and TNEG inputs to be ignored. TAOS is inhibited during Remote Loopback.

1. Entries in I/O column are: DI = Digital Input; DO = Digital Output; AI = Analog Input; AO = Analog Output; S = Supply.

FUNCTIONAL DESCRIPTION

The LXT305A is a fully integrated PCM transceiver for both 1.544 Mbps (DSX-1) and 2.048 Mbps (E1) applications. It allows full-duplex transmission of digital data over existing twisted-pair installations.

The first page of this data sheet shows a simplified block diagram of the LXT305A. The LXT305A transceiver interfaces with two twisted-pair lines (one twisted-pair for transmit, one twisted-pair for receive) through standard pulse transformers and appropriate resistors.

Power Requirements

The LXT305A is a low-power CMOS device. It operates from a single +5 V power supply which can be connected externally to both the transmitter and receiver. However, the two inputs must be within ± .3V of each other, and decoupled to their respective grounds separately. Refer to Application Information for typical decoupling circuitry. Isolation between the transmit and receive circuits is provided internally.

The transmitter powers down to conserve power when the required clock input is not supplied. The LXT305A enters the power down mode during normal operation and local loopback if TCLK is not supplied, and during TAOS if MCLK is not supplied.

Reset Operation

Upon power up, the transceiver is held static until the power supply reaches approximately 3 V. Upon crossing this threshold, the device begins a 32 ms reset cycle to calibrate the transmit and receive delay lines and lock the Phase Lock Loop to the receive line. A reference clock is required to calibrate the delay lines. MCLK provides the receiver reference. The crystal oscillator provides the transmitter reference. If the crystal oscillator is grounded, MCLK is used as the transmitter reference clock.

The transceiver can also be reset from the Host or Hardware Mode. In Host Mode, reset is commanded by simultaneously writing RLOOP and LLOOP to the register. In Hardware Mode, reset is commanded by holding RLOOP and LLOOP High simultaneously for 200 ns. Reset is initiated on the falling edge of the reset request. In either mode, reset clears and sets all registers to 0 and then begins calibration.

Receiver

The LXT305A receives the signal input from one twisted-pair line on each side of a center-grounded transformer. Positive pulses are received at RTIP and negative pulses are received at RRING. Recovered data is output at RPOS and RNEG, and the recovered clock is output at RCLK. Refer to Test Specifications for LXT305A receiver timing.

The signal received at RPOS and RNEG is processed through the peak detector and data slicers. The peak detector samples the inputs and determines the maximum value of the received signal. A percentage of the peak value is provided to the data slicers as a threshold level to ensure optimum signal-to-noise ratio. For T1 applications (determined by Equalizer Control inputs EC1 - EC3 ≠ 000 or 001) the threshold is set to 70% of the peak value. This threshold is maintained above 65% for up to 15 successive zeros over the range of specified operating conditions. For E1 applications (EC inputs = 000 or 001) the threshold is 50%.

The receiver is capable of accurately recovering signals with up to -13.6 dB of attenuation (from 2.4 V), corresponding to a received signal level of approximately 500 mV. Maximum line length is 1500 feet of ABAM cable (approximately 6 dB of attenuation). Regardless of received signal level, the peak detectors are held above a minimum level of .3 V to provide immunity from impulsive noise.

After processing through the data slicers, the received signal is routed to the data and clock recovery sections, and to the receive monitor. The data and clock recovery circuits are highly tolerant with an input jitter tolerance significantly better than required by Pub 62411. Refer to Test Specifications for additional information.

The receiver monitor loads a digital counter at the RCLK frequency. The count is incremented each time a zero is received, and reset to zero each time a one (mark) is received. Upon receipt of 175 consecutive zeros the LOS pin goes High, and a smooth transition replaces the RCLK output with the MCLK. Received marks are output regardless of the LOS status, but the LOS pin will not reset until the ones density reaches 12.5%. This level is based on receipt of at least 4 ones in any 32-bit period with no more than 15 consecutive zeros.

Transmitter

Data received for transmission onto the line is clocked serially into the device at TPOS and TNEG. Input synchronization is supplied by the transmit clock (TCLK). The transmitted pulse shape is determined by Equalizer Control signals EC1 through EC3 as shown in Table 4. Refer to Test Specifications for master and transmit clock timing characteristics. Shaped pulses are applied to the AMI line driver for transmission onto the line at TTIP and TRING. Equalizer Control signals may be hardwired in the Hardware Mode, or input as part of the serial data stream (SDI) in the Host Mode

Pulses can be shaped for either 1.544 or 2.048 Mbps applications. 1.544 Mbps pulses for DSX-1 applications can be programmed to match line lengths from 0 to 655 feet of ABAM cable. The LXT305A also matches FCC and ECSA specifications for CSU applications. 2.048 Mbps pulses can drive coaxial or shielded twisted-pair lines.

Jitter Attenuation

Jitter attenuation of the LXT305A transmit outputs is provided by a Jitter Attenuation Loop (JAL) and an Elastic Store (ES). An external crystal oscillating at 4 times the bit rate provides clock stabilization. Refer to Application Information for crystal specifications. The ES is a 32 x 2-bit register. Transmit data is clocked into the ES with the transmit clock (TCLK) signal, and clocked out of the ES with the dejittered clock from the JAL. When the bit count in the ES is within two bits of overflowing or underflowing, the ES adjusts the output clock by 1/8 of a bit period. The ES produces an average delay of 16 bits in the receive path.

Driver Performance Monitor

The transceiver incorporates a Driver Performance Monitor (DPM) in parallel with TTIP and TRING at the output transformer. The DPM output goes High upon detection of 63 consecutive zeros. It is reset when a one is detected on the transmit line, or when a reset command is received.

Line Code

The LXT305A transmits data as a 50% AMI line code as shown in Figure 2. The output driver maintains a constant low output impedance regardless of whether it is driving marks or spaces. This well controlled output impedance provides excellent return loss (> 18 dB) when used with external 9.1 " precision (± 1 % accuracy) in series with a transmit transformer with a turns ratio of 1:2.3 (± 2% accuracy). Series resistors also provide increased surge protection and reduced short circuit current flow.

Figure 2: 50% AMI Coding

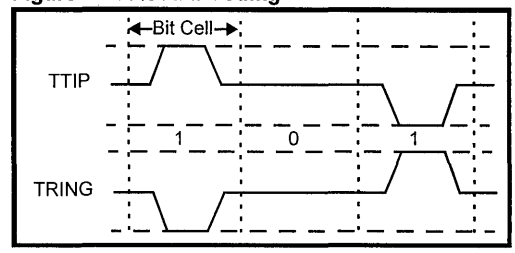


Table 2: LXT305A Serial Data Output Bits (See Figure 4)

Bit D5	Bit D6	Bit D7	Status
0	0	0	Reset has occurred, or no program input.
0	0	1	TAOS is active.
0	1	0	Local Loopback is active.
0	1	1	TAOS and Local Loopback are active.
1	0	0	Remote Loopback is active.
1	0	1	DPM has changed state since last Clear DPM occurred.
1	1	0	LOS has changed state since last Clear LOS occurred.
1	1	1	LOS and DPM have both changed state since last Clear DPM and Clear LOS occurred.

Operating Modes

The LXT305A can be controlled through hard-wired pins (Hardware Mode) or by a microprocessor through a serial interface (Host Mode). The mode of operation is set by the MODE pin logic level. The LXT305A can also be commanded to operate in one of several diagnostic modes.

Host Mode Operation

To allow a host microprocessor to access and control the LXT305A through the serial interface, MODE is set High.

The serial interface (SDI/SDO) uses a 16-bit word consisting of an 8-bit Command/Address byte and an 8-bit Data byte. Figure 3 shows the serial interface data structure and relative timing.

The Host Mode provides a latched Interrupt output (INT) which is triggered by a change in the Loss of Signal (LOS) and/or Driver Performance Monitor (DPM) bits. The Interrupt is cleared when the interrupt condition no longer exists, and the host processor enables the respective bit in the serial input data byte. Host Mode also allows control of the serial data and receive data output timing. The Clock Edge (CLKE) signal determines when these outputs are valid, relative to the Serial Clock (SCLK) or RCLK as listed in Table 3.

Table 3: Valid CLKE Settings

CLKE	Output	Clock	Valid Edge
Low	RPOS RNEG SDO	RCLK RCLK SCLK	Rising Rising Falling
High	RPOS RNEG SDO	RCLK RCLK SCLK	Falling Falling Rising

Figure 3: LXT305A Serial Interface Data Structure

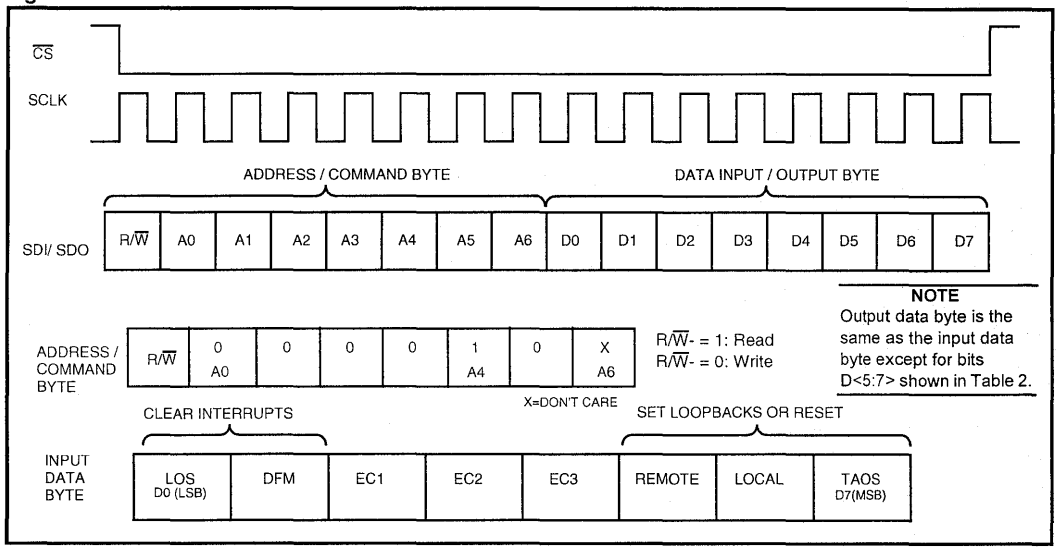


Table 4: Equalizer Control Inputs

EC3	EC2	EC1	Line Length[1]	Cable Loss[2]	Application	Bit Rate
0	1	1	0 ~ 133 ft ABAM	0.6 dB	DSX-1	1.544 Mbps
1	0	0	133 ~ 266 ft ABAM	1.2 dB		
1	0	1	266 ~ 399 ft ABAM	1.8 dB		
1	1	0	399 ~ 533 ft ABAM	2.4 dB		
1	1	1	533 ~ 655 ft ABAM	3.0 dB		
0	0	0	ITU Recommendation G.703		E1 - Coax (75 Ω)	2.048 Mbps
0	0	1			E1 - Twisted-pair (120 Ω)	
0	1	0	FCC Part 68, Option A		CSU (DS-1)	1.544 Mbps

The LXT305A serial port is addressed by setting bit A4 in the Address/Command byte, corresponding to address 16. The LXT305A contains only a single output data register so no complex chip addressing scheme is required. The register is accessed by causing the Chip Select (CS) input to transition from High to Low. Bit 1 of the serial Address/Command byte provides Read/Write control when the chip is accessed. A logic 1 indicates a read operation, and a logic 0 indicates a write operation. Table 2 lists serial data output bit combinations for each status. Serial data I/O timing characteristics are shown in the Test Specifications section.

Hardware Mode Operation

In Hardware Mode the transceiver is accessed and controlled through individual pins. With the exception of the INT and CLKE functions, Hardware Mode provides all the functions provided in the Host Mode. In the Hardware Mode RPOS and RNEG outputs are valid on the rising edge of RCLK.

To operate in Hardware Mode, MODE must be set Low. Equalizer Control signals (EC1 through EC3) are input on the Interrupt, Serial Data In and Serial Data Out pins. Diagnostic control for Remote Loopback (RLOOP), Local Loopback (LLOOP), and Transmit All Ones (TAOS) modes is provided through the individual pins used to control serial interface timing in the Host Mode.

Diagnostic Mode Operation

Transmit All Ones

In Transmit All Ones (TAOS) Mode the TPOS and TNEG inputs to the transceiver are ignored. The transceiver transmits a continuous stream of ones when the TAOS mode is activated. TAOS can be commanded simultaneously with Local Loopback, but is inhibited during Remote Loopback. During TAOS, the transmitter is locked to MCLK. If MCLK is not supplied, the transmitter powers down.

Remote Loopback

In Remote Loopback (RLOOP) Mode, the transmit data and clock inputs (TPOS, TNEG and TCLK) are ignored. The RPOS and RNEG outputs are looped back through the transmit circuits and output on TTIP and TRING at the RCLK frequency. Receiver circuits are unaffected by the RLOOP command and continue to output the RPOS, RNEG and RCLK signals received from the twisted-pair line.

Local Loopback

In Local Loopback (LLOOP) Mode, the receiver circuits are inhibited. The transmit data and clock inputs (TPOS, TNEG and TCLK) are looped back onto the receive data and clock outputs (RPOS, RNEG and RCLK). The transmitter circuits are unaffected by the LLOOP command. The TPOS and TNEG inputs (or a stream of ones if the TAOS command is active) will be transmitted normally. During local loopback if TCLK is not supplied, the transmitter powers down. If LOS and LLOOP are both active, LLOOP takes precedence, forcing RCLK = TCLK.

Table 5: LXT305A Crystal Specifications (External)

Parameter	T1	E1
Frequency	6.176 MHz	8.192 MHz
Frequency stability	± 20 ppm @ 25 °C ± 25 ppm from -40 °C to 85 °C (Ref 25 °C reading)	± 20 ppm @ 25 °C ± 25 ppm from -40 °C to 85 °C (Ref 25 °C reading)
Pullability	CL = 11 pF to 18.7 pF, +ΔF = 175 to 195 ppm CL = 18.7 pF to 34 pF, -ΔF = 175 to 195 ppm	CL = 11 pF to 18.7 pF, +ΔF = 95 to 115 ppm CL = 18.7 pF to 34 pF, -ΔF = 95 to 115 ppm
Effective series resistance	40 Ω Maximum	30 Ω Maximum
Crystal cut	AT	AT
Resonance	Parallel	Parallel
Maximum drive level	2.0 mW	2.0 mW
Mode of operation	Fundamental	Fundamental
Crystal holder	HC49 (R3W),Co = 7 pF maximum C_M = 17 fF typical	HC49 (R3W), Co = 7 pF maximum C_M = 17 fF typical

APPLICATION INFORMATION

1.544 Mbps T1 Interface Applications

Figure 4 is a typical 1.544 Mbps T1 interface application. Use a 1:1.15 transmit transformer without in-line resistors for maximum power savings. The LXT305A is shown in the Host Mode with a T1/ESF Framer providing the digital interface with the host controller. An LXP600A Clock Adapter (CLAD) provides the 2.048 MHz system backplane clock, locked to the recovered 1.544 MHz clock signal. The power supply inputs are tied to a common bus with appropriate decoupling capacitors installed (68 µF on the transmit side, 1.0 µF and 0.1 µF on the receive side).

For DSX-1 applications, series resistors can be used in line with the transmit transformer to provide higher return loss.

2.048 Mbps E1 Interface Applications

Figure 5 is a typical 2.048 Mbps E1 application. The LXT305A is shown in Hardware Mode with an E1/CRC4 Framer. As in the DSX-1 application Figure 4, this configuration is illustrated with a crystal in place to enable the LXT305A Jitter Attenuation Loop, and a single power supply bus. The hard-wired control lines for TAOS, LLOOP and RLOOP are individually controllable, and the LLOOP and RLOOP lines are also tied to a single control for the Reset function. With the 1:1 transformer ratio and code 000 selected on the EC inputs, the LXT305A outputs the ITU specified 2.37 V pulse onto 75 " coaxial cable. Simply changing the EC code to 001 allows the LXT305A to match the 3.0 V pulse specification for 120 " shielded twisted-pair cable. No transformer change is required. For situations where at 1:1.26 transformer is desired, EC code 000 selects the correct output for 120 " twisted-pair cable.

To achieve higher return loss, increased surge protection and lower output short circuit current, series resistors can be used in line with the transmit transformer.

Table 6: T1/E1 Input/Output Configurations

Bit Rate (Mbps)	Crystal XTAL	Cable (Ω)	Rr[2] (Ω)	EC3/2/1	Transmit Transformer[1] (Tr)	Rt[2] (Ω)	Typical TX Return Loss[3] (dB)	Cc (µF)
1.544 (T1)	LXC6176	100	200	0/1/1 - 1/1/1	1:1.15 1:2 1:2.3	0 9.1 9.1	0.5 18 18	0.47 0 0
2.048 (E1)	LXC8192	120	240	0/0/0 0/0/0 0/0/1 0/0/1	1:1.26 1:2 1:1 1:2	0 9.1 0 15	0.5 12 0.5 18	0.47 0 0.47 0
		75	150	0/0/0 0/0/0 0/0/1 0/0/1	1:1 1:2 1:1 1:2	0 9.1 10 14.3	0.5 18 5 10	0.47 0 0 0

1. Transformer turns ratio accuracy is ± 2%.
2. Rr and Rt values are ± 1%.
3. Typical return loss, 51 kHz to 3.072 MHz band.

Figure 4: Typical LXT305A 1.544 Mbps T1 Application (Host Mode)

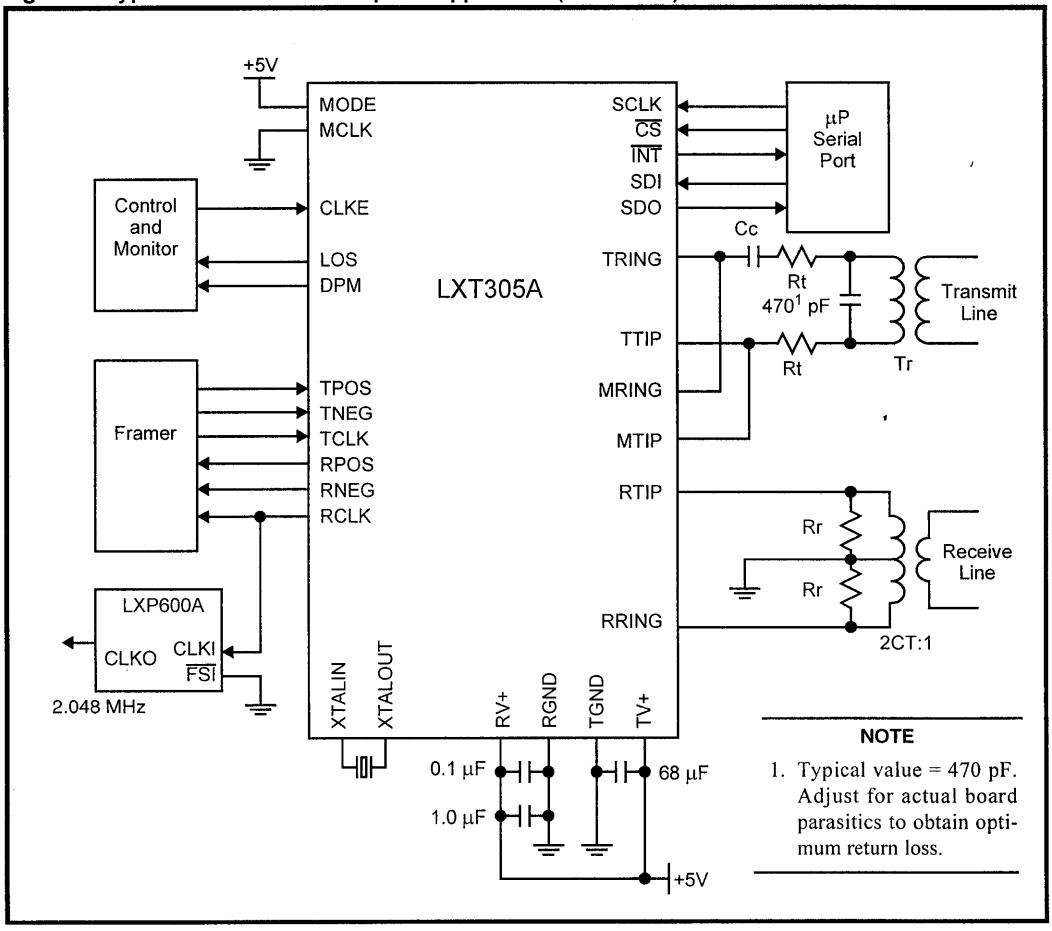
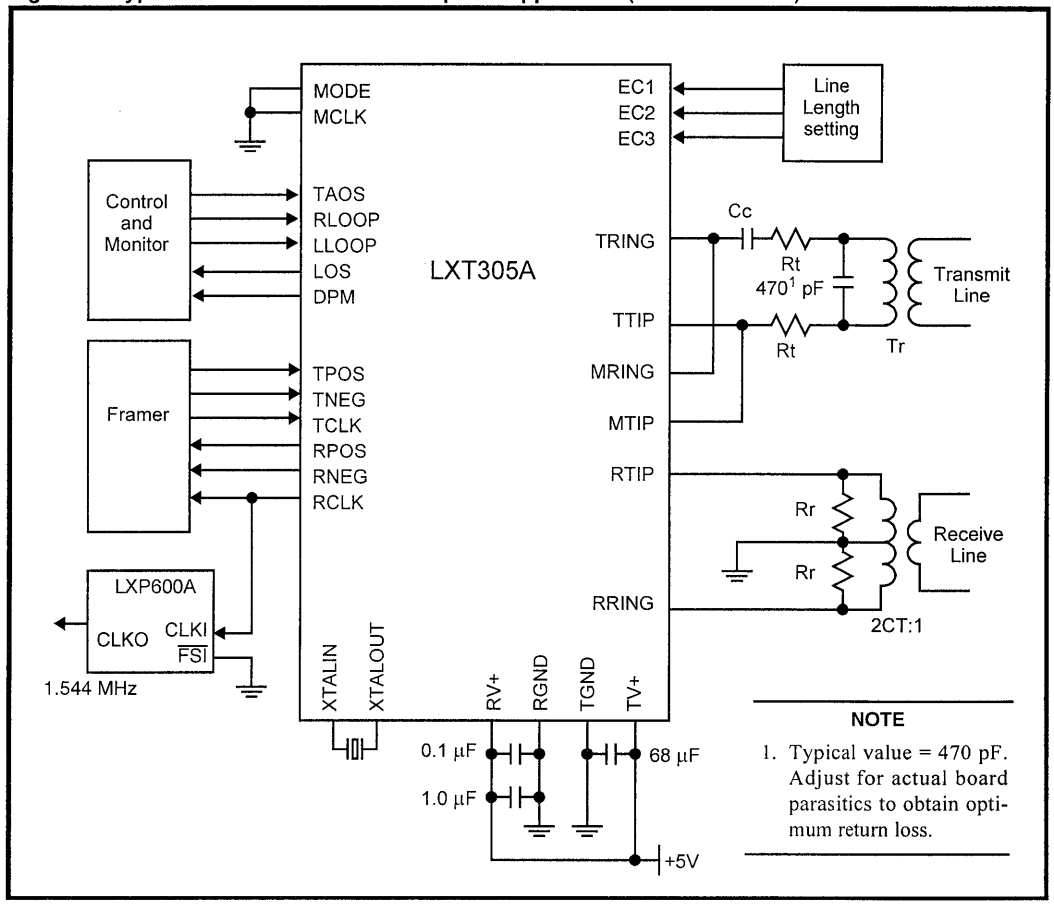


Figure 5: Typical LXT305A 120 Ω 2.048 Mbps E1 Application (Hardware Mode)



TEST SPECIFICATIONS

NOTE

The minimum and maximum values in Tables 7 through 13 and Figures 6 through 11 represent the performance specifications of the LXT305A and are guaranteed by test, except where noted by design.

Table 7: Absolute Maximum Ratings

Parameter	Sym	Min	Max	Units
DC supply (referenced to GND)	RV+, TV+	-0.3	6.0	V
Input voltage, any pin[1]	V_{IN}	RGND - 0.3	RV+ + 0.3	V
Input current, any pin[2]	I_{IN}	-10	10	mA
Storage temperature	T_{STG}	-65	150	°C

CAUTION

Operations at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

1. Excluding RTIP and RRING which must stay between -6V and (RV+ + 0.3) V.
2. Transient currents of up to 100 mA will not cause SCR latch up. TTIP, TRING, TV+ and TGND can withstand a continuous current of 100 mA.

Table 8: Recommended Operating Conditions and Characteristics

Parameter	Sym	Min	Typ	Max	Units
DC supply[1]	RV+, TV+	4.75	5.0	5.25	V
Ambient operating temperature	T_A	-40	25	85	° C

1. TV+ must not exceed RV+ by more than 0.3 V.

Table 9: Electrical Characteristics (Under Recommended Operating Conditions)

Parameter	Sym	Min	Max	Units	Test Conditions
Total power dissipation[1]	P_D	–	400	mW	100% ones density & maximum line length @ 5.25 V
High level input voltage[2,3] (pins 1-5, 10, 23-28)	V_{IH}	2.0	–	V	
Low level input voltage[2,3] (pins 1-5, 10, 23-28)	V_{IL}	–	0.8	V	
High level output voltage[2,3] (pins 6-8, 11, 12, 23, 25)	V_{OH}	2.4	–	V	I_{OUT} = -400 µA
Low level output voltage[2,3] (pins 6-8, 11, 12, 23, 25)	V_{OL}	–	0.4	V	I_{OUT} = 1.6 mA
Input leakage current[4]	I_{LL}	0	±10	µA	
Three-state leakage current[2] (pin 25)	I_{3L}	0	±10	µA	

1. Power dissipation while driving 75 Ω load over operating temperature range. Includes device and load. Digital input levels are within 10% of the supply rails and digital outputs are driving a 50 pF capacitive load.
2. Functionality of pins 23 and 25 depends on mode. See Host/Hardware Mode descriptions.
3. Output drivers will output CMOS logic levels into CMOS loads.
4. Except MTIP and MRING Ill = ± 50 µA.

Table 10: Analog Characteristics (Under Recommended Operating Conditions)

Parameter		Min	Typ[1]	Max	Units	Test Conditions
AMI output pulse amplitudes	DSX-1	2.4	3.0	3.6	V	measured at the DSX
	E1	2.7	3.0	3.3	V	measured at line side
Recommended output load at TTIP and TRING		–	75	–	Ω	
Jitter added by the transmitter[2]	10 Hz - 8 kHz	–	–	0.01	UI	
	8 kHz - 40 kHz	–	–	0.025	UI	
	10 Hz - 40 kHz	–	–	0.025	UI	
	Broad Band	–	–	0.05	UI	
Sensitivity below DSX (0 dB = 2.4 V)		13.6	–	–	dB	
		500	–	–	mV	
Loss of Signal threshold		–	0.3	–	V	
Data decision threshold	DSX-1	63	70	77	% peak	
	E1	43	50	57	% peak	
Allowable consecutive zeros before LOS		160	175	190	–	
Input jitter tolerance 10 kHz - 100 kHz		0.4	–	–	UI	
Jitter attenuation curve corner frequency[3]		–	3	–	Hz	
Minimum return loss[4,5]		**Transmit** Min	Typ	**Receive** Min	Typ	dB
	51 kHz - 102 kHz	18	–	20	–	dB
	102 kHz - 2.048 kHz	18	–	20	–	dB
	2.048 kHz - 3.072 kHz	18	–	20	–	dB

1. Typical values are measured at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Input signal to TCLK is jitter-free.
3. Circuit attenuates jitter at 20 dB/decade above the corner frequency.
4. In accordance with ITU G.703/ETS 300166 return loss specifications when wired per Figure 5 (E1).
5. Guaranteed by design.

Figure 6: Typical Receive Jitter Tolerance

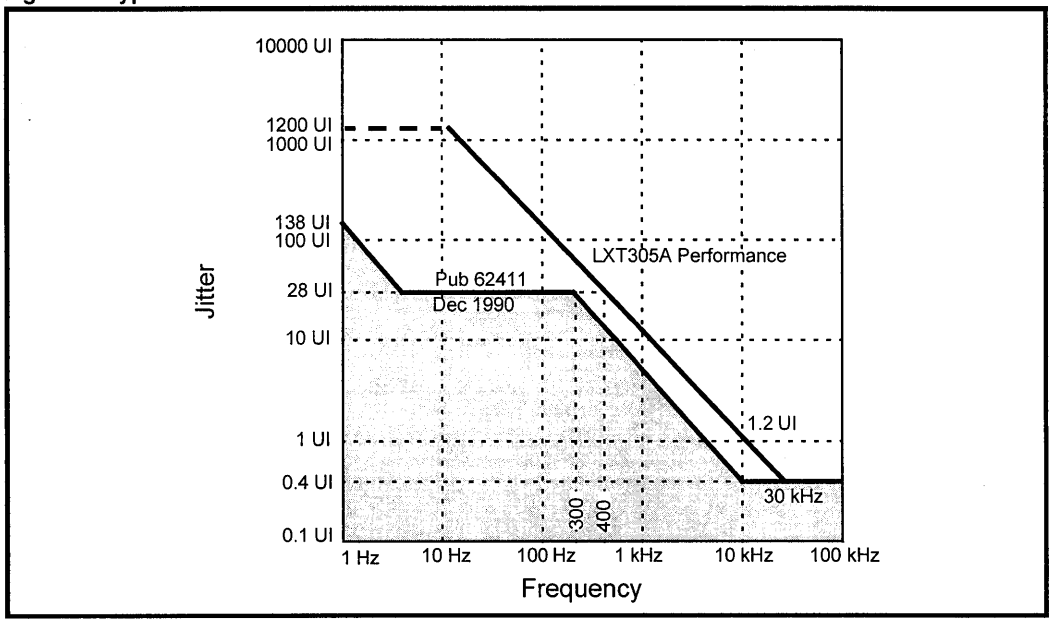


Figure 7: LXT305A Transmit Jitter Transfer Performance (Typical)

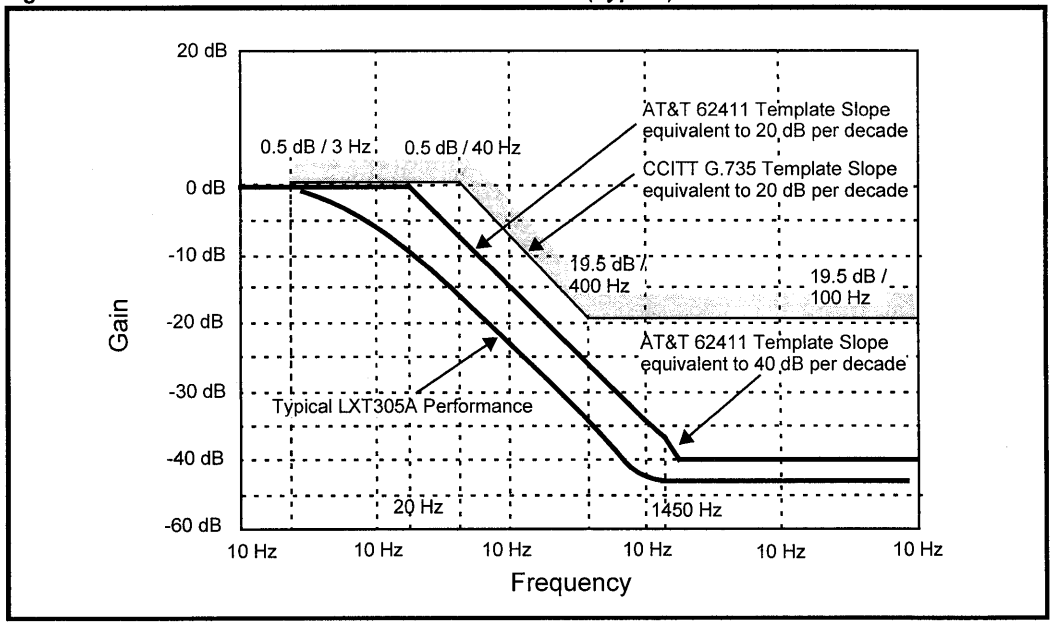


Table 11: LXT305A Receive Timing Characteristics (See Figure 8)

Parameter		Sym	Min	Typ[1]	Max	Units	Test Conditions
Receive clock duty cycle[2]	T1	RCLKd	40	50	60	%	
	E1	RCLKd	40	50	60	%	
Receive clock pulse width[2]	T1	t_{PW}	594	648	702	ns	
	E1	t_{PW}	447	488	529	ns	
Receive clock pulse width high	T1	t_{PWH}	–	324	–	ns	
	E1	t_{PWH}	–	244	–	ns	
Receive clock pulse width low	T1	t_{PWL}	270	324	378	ns	
	E1	t_{PWL}	203	244	285	ns	
RPOS/RNEG to RCLK rising setup time	T1	t_{SUR}	50	270	–	ns	
	E1	t_{SUR}	50	203	–	ns	
RCLK rising to RPOS/RNEG hold time	T1	t_{HR}	50	270	–	ns	
	E1	t_{HR}	50	203	–	ns	

1. Typical values are at 25 °C and are for design aid only; they are not guaranteed and not subject to production testing.
2. RCLK duty cycle widths will vary depending on extent of received pulse jitter displacement. Max and Min RCLK duty cycles are for worst case jitter conditions (0.4 UI clock displacement for 1.544 MHz, 0.2 UI clock displacement for 2.048 MHz).

Figure 8: LXT305A Receive Clock Timing Diagram

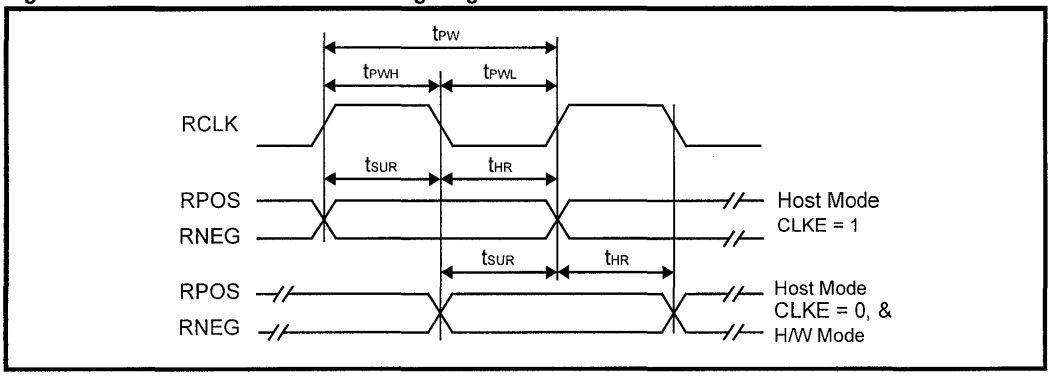


Table 12: LXT305A Master Clock and Transmit Timing Characteristics (See Figure 9)

Parameter		Sym	Min	Typ[1]	Max	Units
Master clock frequency	DSX-1	MCLK	–	1.544	–	MHz
	E1	MCLK	–	2.048	–	MHz
Master clock tolerance		MCLKt	–	±100	–	ppm
Master clock duty cycle		MCLKd	40	–	60	%
Crystal frequency	DSX-1	fc	–	6.176	–	MHz
	E1	fc	–	8.192	–	MHz
Transmit clock frequency	DSX-1	TCLK	–	1.544	–	MHz
	E1	TCLK	–	2.048	–	MHz
Transmit clock tolerance		TCLKt	–	±50	–	ppm
Transmit clock duty cycle		TCLKd	10	–	90	%
TPOS/TNEG to TCLK setup time		t_{SUT}	25	–	–	ns
TCLK to TPOS/TNEG hold time		t_{HT}	25	–	–	ns

1. Typical values are at 25 °C and are for design aid only; they are not guaranteed and not subject to production testing.

Figure 9: LXT305A Transmit Clock Timing Diagram

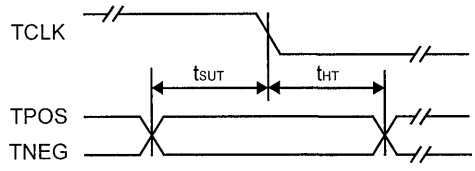


Table 13: LXT305A Serial I/O Timing Characteristics (See Figures 10 and 11)

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Rise/Fall time - any digital output	t_{RF}	–	–	100	ns	Load 1.6 mA, 50 pF
SDI to SCLK setup time	t_{DC}	50	–	–	ns	
SCLK to SDI hold time	t_{CDH}	50	–	–	ns	
SCLK low time	t_{CL}	240	–	–	ns	
SCLK high time	t_{CH}	240	–	–	ns	
SCLK rise and fall time	t_R, t_F	–	–	50	ns	
$\overline{CS}$ to SCLK setup time	t_{CC}	50	–	–	ns	
SCLK to $\overline{CS}$ hold time	t_{CCH}	50	–	–	ns	
$\overline{CS}$ inactive time	t_{CWH}	250	–	–	ns	
SCLK to SDO valid	t_{CDV}	–	–	200	ns	
SCLK falling edge or $\overline{CS}$ rising edge to SDO high Z	t_{CDZ}	–	100	–	ns	

1. Typical values are at 25° C and are for design aid only; they are not guaranteed and not subject to production testing.

Figure 10: LXT305A Serial Data Input Timing Diagram

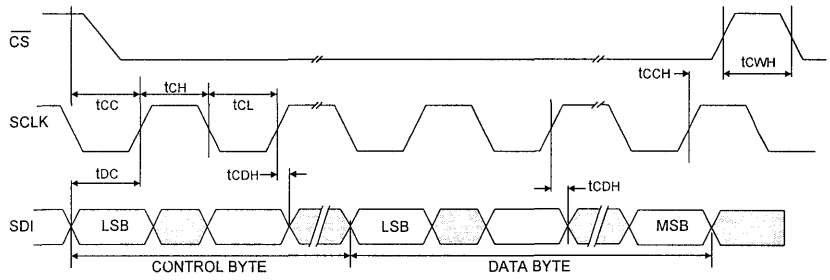
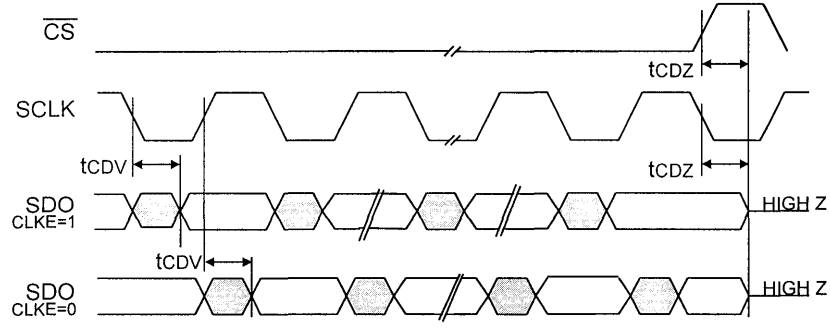


Figure 11: LXT305A Serial Data Output Timing Diagram



NOTES

LXT307

Low-Power E1 Integrated Short-Haul Transceiver

General Description

The LXT307 is a fully integrated low-power transceiver optimized for G.703 2.048 Mbps (E1) applications. It features a constant low output impedance transmitter allowing for high transmitter return loss. Transmit pulse amplitudes are selectable for various cable types. It is designed to exceed the latest international specifications, including G.775 and ETS 300 166.

The LXT307 is microprocessor controllable through a serial interface. It can also be controlled through individual pins in Hardware Mode.

The LXT307 offers a variety of diagnostic features, including transmit and receive monitoring. The device requires a single 2.048 MHz clock reference for the on chip high performance clock recovery system. It uses an advanced double-poly, double-metal CMOS process and requires only a single 5-volt power supply.

Applications

- PCM G.703 Interfaces
- E1 multiplexer
- Digital Access and Cross-connect Systems (DACS)
- G.703 Trunk line cards for Public Switching Systems and PABX
- High-speed data transmission lines

Features

- Low power dissipation 260 mW typical
- Constant low output impedance transmitter regardless of data pattern (3 Ω typical)
- Low speed reference clock to reduce PC board noise coupling
- Driver short circuit current limited to 50 mA per OFTEL/BABT recommendations
- 75/120 Ω Operation without component changes
- Transmit and receive return loss exceeds ETSI ETS 300 166 and G.703
- Meets or exceeds all ITU specifications including G.703, G.823 (03/93) and G.775
- Compatible with most popular PCM framers
- Line driver, data recovery and clock recovery functions
- Minimum receive signal of 500 mV
- Programmable transmit amplitude for 75 Ω and 120 Ω operation without component changes
- Local and remote loopback functions
- Transmit performance monitor with DPM detecting single line shorts for improved reliability
- Analog/digital LOS monitor per G.775
- Receiver jitter tolerance 0.4 UI from 40 kHz to 100 kHz
- Serial Control Interface
- Available in 28-pin DIP or PLCC

LXT307 Block Diagram

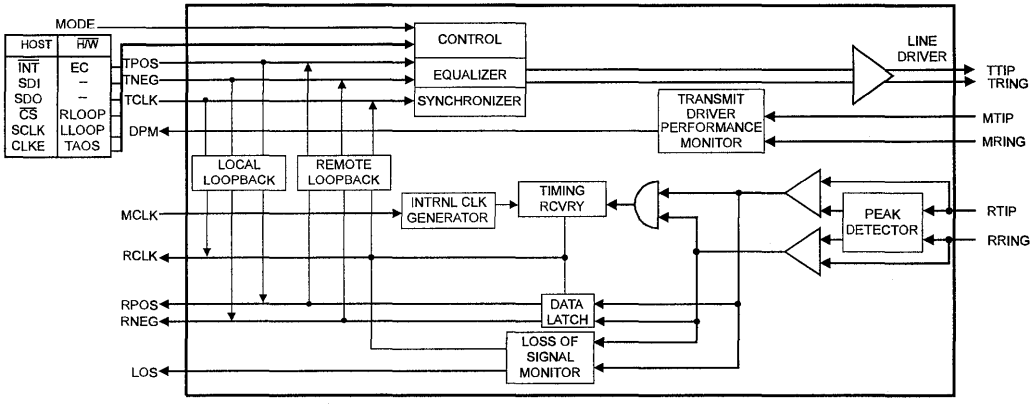


Figure 1: Pin Assignments

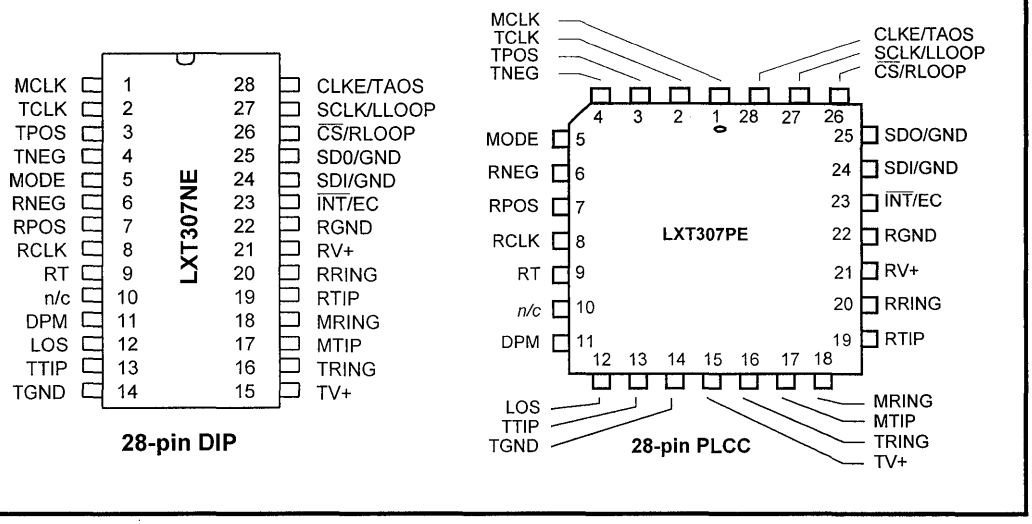


Table 1: Pin Assignments and Signal Descriptions

Pin #	Sym	I/O[1]	Description
1	MCLK	DI	**Master Clock.** A 2.048 MHz clock input used to generate internal clocks. Upon Loss of Signal (LOS), RCLK is derived from MCLK.
2	TCLK	DI	**Transmit Clock.** Transmit clock input. TPOS and TNEG are sampled on the falling edge of TCLK. If TCLK is not supplied, the transmitter remains powered down.
3	TPOS	DI	**Transmit Positive Data.** Input for the positive pulse to be transmitted on the line.
4	TNEG	DI	**Transmit Negative Data.** Input for the negative pulse to be transmitted on the line.
5	MODE	DI	**Mode Select.** Setting MODE High puts the LXT307 in the Host Mode. In the Host Mode, the serial interface is used to control the LXT307 and determine its status. Setting MODE Low puts the LXT307 in the Hardware (H/W) mode. In the Hardware mode the serial interface is disabled and hard-wired pins are used to control configuration and report status.
6	RNEG	DO	**Receive Negative Data; Receive Positive Data.** Received data outputs. A signal on RNEG corresponds to receipt of a negative pulse on RTIP and RRING. A signal on RPOS corresponds to receipt of a positive pulse on RTIP and RRING. RNEG and RPOS outputs are Non-Return-to-Zero (NRZ). In the Host mode, CLKE determines the clock edge at which these outputs are stable and valid. In the Hardware mode, both outputs are stable and valid on the rising edge of RCLK.
7	RPOS	DO	
8	RCLK	DO	**Recovered Clock.** This is the clock recovered from the signal received at RTIP and RRING.
9	RT	AI	**Resistor Termination.** Connect to RV+ through a 1 kΩ resistor.

1. Entries in I/O column are: DI = Digital Input; DO = Digital Output; AI = Analog Input; AO = Analog Output; S = Supply.

Table 1: Pin Assignments and Signal Descriptions – continued

Pin #	Sym	I/O[1]	Description
10	N/C	–	**No connection.**
11	DPM	DO	**Driver Performance Monitor.** DPM goes High when the transmit monitor (MTIP and MRING) does not detect a signal for 63±2 clock periods. DPM remains High until a signal is detected. It is reset to Low with the first transition on MTIP and MRING.
12	LOS	DO	**Loss of Signal.** LOS goes High when the signal falls below 20 dB below nominal for more than 175 consecutive bit periods. LOS returns Low when the received signal detects 4 transitions in any 32-bit window (12.5% 1s density) with no more than 15 consecutive 0s.
13	TTIP	AO	**Transmit Tip; Transmit Ring.** Differential Driver Outputs. These low-impedance outputs achieve high return loss with resistors used in series with a transformer as specified in Tables 9 and 10.
16	TRING	AO	
14	TGND	–	**Transmit Ground.** Ground return for the transmit drivers power supply TV+.
15	TV+	S	**Transmit Power Supply.** +5 VDC power supply input for the transmit drivers. TV+ must not vary from RV+ by more than ±0.3 V during all operating conditions including start-up.
17	MTIP	AI	**Monitor Tip; Monitor Ring.** These pins are used to monitor the TTIP and TRING transmit outputs. The transceiver can be connected to monitor its own output or the output of another LXT307 on the board. To prevent false interrupts in the host mode if the monitor is not used, apply a clock signal to one of the monitor pins and tie the other monitor pin to approximately the clock's midrange voltage. The monitor clock can range from 100 kHz to the TCLK frequency.
18	MRING	AI	
19	RTIP	AI	**Receive Tip; Receive Ring.** The AMI signal received from the line is applied at these pins. A center-tapped, center-grounded, 2:1 step-up transformer for 75 Ω and 120 Ω is required on these pins. Data and clock from the signal applied at these pins are recovered and output on the RPOS/RNEG and RCLK pins.
20	RRING	AI	
21	RV+	S	**Receive Power Supply.** +5 VDC power supply for all circuits except the transmit drivers. (Transmit drivers are supplied by TV+.)
22	RGND	S	**Receive Ground.** Ground return for power supply RV+.
23	$\overline{INT}$	DO	**Interrupt** ***(Host Mode).*** This LXT307 Host mode output goes Low to flag the host processor when LOS or DPM go active. $\overline{INT}$ is an open-drain output and should be tied to power supply RV+ through a resistor. $\overline{INT}$ is reset by clearing the respective register bit (LOS and/or DPM).
	EC	DI	**Equalizer Control** ***(H/W Mode).*** The signal applied at this pin in the LXT307 Hardware mode is used to determine the amplitude of AMI output transmit pulses.
24	SDI	DI	**Serial Data In** ***(Host Mode).*** The serial data input stream is applied to this pin when the LXT307 operates in the Host mode. SDI is sampled on the rising edge of SCLK.
	GND	DI	**GND** ***(H/W Mode).*** Signal ground.
25	SDO	DO	**Serial Data Out** ***(Host Mode).*** The serial data from the on-chip register is output on this pin in the LXT307 Host mode. If CLKE is High, SDO is valid on the rising edge of SCLK. If CLKE is Low, SDO is valid on the falling edge of SCLK. This pin goes to a high-impedance state when the serial port is being written to and when $\overline{CS}$ is High.
	GND	DI	**GND** ***(H/W Mode).*** Signal ground.

1. Entries in I/O column are: DI = Digital Input; DO = Digital Output; AI = Analog Input; AO = Analog Output; S = Supply.

Table 1: Pin Assignments and Signal Descriptions – continued

Pin #	Sym	I/O[1]	Description
26	$\overline{CS}$	DI	**Chip Select** ***(Host Mode).*** This input is used to access the serial interface in the LXT307 Host mode. For each read or write operation, $\overline{CS}$ must transition from High to Low, and remain Low.
	RLOOP	DI	**Remote Loopback** ***(H/W Mode).*** This input controls loopback functions in the LXT307 Hardware mode. Setting RLOOP to a logic H enables the Remote Loopback mode. Setting both RLOOP and LLOOP High causes a Reset.
27	SCLK	DI	**Serial Clock** ***(Host Mode).*** This clock is used in the LXT307 Host mode to write data to or read data from the serial interface registers.
	LLOOP	DI	**Local Loopback** ***(H/W Mode).*** This input controls loopback functions in the LXT307 Hardware mode. Setting LLOOP High enables the Local Loopback Mode.
28	CLKE	DI	**Clock Edge** ***(Host Mode).*** Setting CLKE High causes RPOS and RNEG to be valid on the falling edge of RCLK, and SDO to be valid on the rising edge of SCLK. When CLKE is Low, RPOS and RNEG are valid on the rising edge of RCLK, and SDO is valid on the falling edge of SCLK.
	TAOS	DI	**Transmit All Ones** ***(H/W Mode).*** When set High, TAOS causes the LXT307 (Hardware mode) to transmit a continuous stream of marks at the TCLK frequency. Activating TAOS causes TPOS and TNEG inputs to be ignored. TAOS is inhibited during Remote Loopback.

1. Entries in I/O column are: DI = Digital Input; DO = Digital Output; AI = Analog Input; AO = Analog Output; S = Supply.

Functional Description

The LXT307 is a fully integrated PCM transceiver for G.703 2.048 Mbps (E1) applications. A simplified block diagram of the transceiver appears on page 1. The LXT307 allows full-duplex transmission of digital data over existing twisted-pair or coax installations. It interfaces with two lines, one for receive, one for transmit.

Power Requirements

The LXT307 is a low-power CMOS device. It operates from a single +5 V power supply which can be connected externally to both the transmitter and receiver. However, the two inputs must be within ±0.3 V of each other, and decoupled separately to their respective grounds. Isolation between transmit and receive circuits is provided internally. During normal operation, and LLOOP, the transmitter powers down if TCLK is not supplied. The transmitter also powers down during TAOS operation if TCLK is not supplied.

Reset Operation

Upon power up, the transceiver is held static until the power supply reaches approximately 3 V. Upon crossing this threshold, the device begins a 32 ms reset cycle to calibrate the transmit and receive delay lines and locks the Phase Lock Loop to the receive line. A reference clock is required to calibrate the delay lines The transmitter reference is provided by TCLK. MCLK is used as the receiver reference clock.

The transceiver can also be reset from the Host or Hardware mode. In Host mode, reset is commanded by simultaneously writing RLOOP and LLOOP to the register. In Hardware mode, reset is commanded by holding RLOOP and LLOOP high simultaneously for 200 ns. Reset is initiated on the falling edge of the reset request. In either mode, reset clears and sets all registers to 0 and then calibration begins.

Receiver

The LXT307 receives the signal input from one line on each side of a center-grounded transformer. Positive pulses are received at RTIP and negative pulses are received at RRING.

The signal received at RTIP and RRING is processed through the peak detector and data slicers. The peak detector samples the inputs and determines the maximum value of the received signal. A percentage of the peak value is provided to the data slicers as a threshold level to ensure optimum signal-to-noise ratio. The threshold is 50% and is maintained over the whole input range.

The receiver is capable of accurately recovering signals with up to -13.6 dB of attenuation (from 2.4 V), corresponding to a received signal level of approximately 500 mV. Regardless of received signal level, the peak detectors are held above a minimum level of 0.3 V to provide immunity from impulsive noise.

After processing through the data slicers, the received signal is routed to the data and clock recovery sections, and to the receive monitor. The data and clock recovery circuits are highly tolerant with an input jitter tolerance significantly better than required by G.823, as shown in Figure 17. Recovered clock signals are supplied to the data latch. Recovered data is output at RPOS and RNEG, and the recovered clock is output at RCLK. Refer to Table 15 and Figure 13 for LXT307 receiver timing.

Loss of Signal Processor

Declaring the LOS Condition

Recommendation G.775 defines basic criteria for detection and clearance of Loss of Signal (LOS) defects.

LXT307 uses a digital-and-analog detection scheme to comply with G.775. If the signal level falls below 20 dB typical, the LXT307 begins to count consecutive bit times and declares LOS after approximately 175 (160 to 190) consecutive zeros. Refer to Table 2.

Clearing the LOS Condition

LXT307 clears LOS with a three-step process:

1. The signal must first exceed the 20 dB signal level.
2. Then a 32-bit repeating window checks for 12.5% 1s density. (To meet this parameter, there must be at least four 1s out of the 32 bits in the window.)
3. Finally, there must be no more than 15 consecutive 0s to clear the LOS condition.

Transmitter

Data received for transmission onto the line is clocked serially into the device at TPOS and TNEG. Input synchronization is supplied by the transmit clock (TCLK). If TCLK is not supplied, the transmitter remains powered down, except during remote loopback and TAOS. Refer to Table 16 and Figure 14 for master and transmit clock timing characteristics.

Line Code

The LXT307 transmits data as a 50% AMI line code as shown in Figure 2. The output driver maintains a constant low output impedance under dynamic conditions regardless of whether it is driving marks or spaces.

The transmitted pulse amplitude is determined by the equalizer control signal EC as shown in Table 3.

The equalizer control signal may be hardwired in Hardware mode or input as part of the serial data stream (SDI) in Host mode. Shaped pulses are applied to the AMI line driver for transmission onto the line at TTIP and TRING. The line driver provides a constant low output impedance of 3 Ω (typical). This well-controlled output impedance provides excellent return loss when used with external precision resistors (±1% accuracy) in series with a transmit transformer. Series resistors also provide increased surge protection and reduce short circuit current flow.

Pulses can drive coaxial or shielded twisted-pair lines. A 1:2 transmit transformer and series resistors are recommended. This design meets or exceeds all ETSI 300 166 and European PTT specifications for transmit and receive return loss when series resistors are used.

Figure 2: 50% AMI Coding

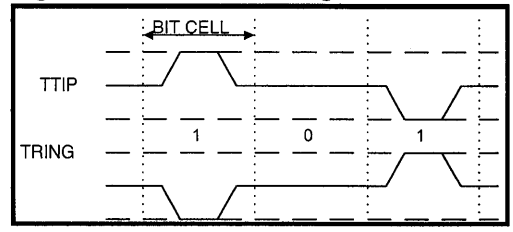


Table 2: G.775 Requirements and LXT307 Implementation of LOS Detection

Condition	G.775 Recommendation	Level One Implementation
Detect LOS	Signal with no transitions[1] less than or equal to signal level of 35 dB below nominal for N consecutive intervals where 10 ≤N ≤255.	Signal level below 20 dB and no consecutive transition for 160 to 190 (typical 175) pulse intervals.
Clear LOS	Signal has transitions[1] and level greater than or equal to 9 dB below nominal for N consecutive pulse intervals where 10 ≤N ≤255.	Signal level above 20 dB with bit density greater than 12.5% for 32-bit positions, and with fewer than 15 consecutive zeros.

1. A signal with "transitions" corresponds to a G.703 compliant signal.

Table 3: Equalizer Control Inputs for Pulse Amplitude Selection

EC	Line Length & Cable Loss	Application
0	ITU Recommendation G.703	E1 - Coax (75 Ω)
1	ITU Recommendation G.703	E1 - Twisted-Pair (120 Ω)

Driver Performance Monitor

The transceiver incorporates an advanced Driver Performance Monitor (DPM) that can be connected in parallel with the TTIP and TRING at the output transformer. The DPM circuitry uses four comparators and a 150 ns pulse discriminator to filter glitches. The DPM output level goes High upon detection of 63 consecutive zeros, and is cleared when a transition is detected on the transmit line or when a reset command is received. The DPM output also goes High to indicate a signal line short to ground on TTIP or TRING. A ground fault induced DPM flag is automatically cleared when the ground condition is corrected (chip reset is not required).

Operating Modes

The LXT307 transceiver can be controlled through hardwired pins (Hardware Mode–default) or by a microprocessor through a serial interface (Host Mode) depending on the input to pin 5 (MODE). The mode of operation is set by the MODE pin logic level. The LXT307 can also be commanded to operate in one of several diagnostic modes.

Hardware Mode Operation

In Hardware mode the transceiver is controlled through individual pins. With the exception of the $\overline{INT}$ and CLKE functions, Hardware mode provides all the functions provided in the Host mode. In the Hardware mode RPOS and RNEG outputs are valid on the rising edge of RCLK. To operate in Hardware mode, the MODE must be set to 0. Diagnostic Control for Remote Loopback (RLOOP), Local Loopback (LLOOP), and Transmit All 1s (TAOS) modes is provided through the individual pins.

If MODE is set Low, LXT307 operates in Hardware Mode. In Hardware Mode the transceiver is controlled through individual pins; a microprocessor is not required. RPOS and RNEG are valid on the rising edge of RCLK.

The equalizer is controlled through pin 23 (EC). Diagnostic control for Remote Loopback (RLOOP), Local Loopback (LLOOP), and Transmit All 1s (TAOS) is provided through pins 26, 27, and 28.

Host Mode Control

The LXT307 operates in the Host mode when pin 5 (MODE) is asserted High. In Host mode a microprocessor controls the LXT307 through the serial I/O port (SIO) which provides access to the LIU. The LIU contains a pair of data registers, one for command inputs and one for status outputs. An SIO transaction is initiated by a falling edge on the Chip Select pin. A High-to-Low transition on $\overline{CS}$ is required for each subsequent access to the Host mode registers.

The LIU responds by writing the incoming serial word from the SDI pin into its command register. Figure 3 shows an SIO write operation. The 16-bit serial word consists of an 8-bit Command/Address byte and an 8-bit Data byte. If the command word contains a read request, the LIU subsequently outputs the contents of its status register onto the SDO pin. Figure 4 shows an SIO read operation. The Clock Edge (CLKE) signal determines when the SDO and receive data outputs are valid, relative to the Serial Clock (SCLK) or RCLK as listed in Table 4. Table 17 and Figures 15 and 16 show SIO timing.

Serial Input Word

Figure 3 shows the Serial Input data structure. The LXT307 is addressed by setting bit A4 in the Address/Command byte, corresponding to address 16. Bit 1 of the serial Address/Command byte provides Read/Write (R/$\overline{W}$) control when the chip is accessed. The R/$\overline{W}$ bit is set to logic 1 to read the data output byte from the chip, and set to logic 0 to write the input data byte to the chip.

The second eight bits of a write operation, clear Loss of Signal (LOS) and Driver Performance Monitor (DPM) interrupts, reset the chip, and control diagnostic modes. The first 2 bits (D0 - D1) clear and/or mask LOS and DPM interrupts. The last three bits (D5 - D7) control operating modes (normal and diagnostic) and chip reset. Refer to Table 5 for details on bits D5 - D7.

Serial Output Word

Figure 4 shows the Serial Output data structure. SDO is high impedance when SDI receives an Address/Command byte. If SDI receives a read command (R/$\overline{W}$ = 1), then SDO becomes active after the last Command/Address bit (A6) and remains active for eight SCLK cycles. Typically the first bit out of SDO changes the state of SDO from high-Z to a Low/High.

The first five bits (D0-D4) of the output data byte reports Loss of Signal (LOS) and Driver Performance Monitor (DPM) conditions, equalizer settings, and operating modes (normal or diagnostic). The last three bits (D5 through D7) report operating modes and interrupt status.

If the $\overline{INT}$ line is High (no interrupt is pending), bits D5 through D7 report the status of the operating mode as listed in Table 6. If the $\overline{INT}$ line is Low, the interrupt

status overrides all other reports and bits D5 - D7 reflect the interrupt status as listed in Table 6.

Interrupt Handling

The Host mode provides a latched Interrupt output pin, $\overline{INT}$. Any change in the LOS or DPM bits (D0 and D1 of the output data byte, respectively) triggers an interrupt. As shown in Figure 5, writing a one to the respective bit of the input data byte (D0 = LOS, D1 = DPM) masks either or both interrupt generators. When an interrupt has occurred the $\overline{INT}$ output pin is pulled Low. The output stage of the $\overline{INT}$ pin consists of a pulldown device. Hence, an external pull-up resistor is required. clear the interrupt as follows:

1. If one or both interrupt bits (LOS or DPM, D0 and D1 of the output data byte) = 1, writing a 1 to the input bit (D0 or D1, respectively), of the input data byte will clear the interrupt. Leaving a 1 in either of these bit positions will effectively mask the associated interrupt. To re-enable the interrupt capability, reset D0 and/or D1 to 0.
2. If neither LOS or DPM = 1, the interrupt will be cleared by resetting the chip. To reset the chip, set data input bits D5 and D6 = 1, and D7 = 0.

Table 4: CLKE Settings

CLKE	Output	Clock	Valid Edge
LOW	RPOS/RNEG SDO	RCLK SCLK	Rising Falling
HIGH	RPOS/RNEG SDO	RCLK SCLK	Falling Rising

Table 5: SIO Input Bit Settings

(see Figure 3)

Mode	RLOOP Bit D5	LLOOP Bit D6	TAOS Bit D7
RLOOP	1	0	–
LLOOP	0	1	0
LLOOP + TAOS	0	1	1
TAOS	0	0	1
RESET	1	1	0

Table 6: Serial Data Output Bit Coding

Bit D5	Bit D6	Bit D7	Status
0	0	0	Reset has occurred, or no program input. (*i.e.*, normal operation)
0	0	1	TAOS is active.
0	1	0	Local Loopback is active.
0	1	1	TAOS and Local Loopback are active.
1	0	0	Remote Loopback is active.
			Interrupt Status
1	0	1	DPM has changed state since last clear DPM occurred.
1	1	0	LOS has changed state since last clear LOS occurred.
1	1	1	LOS and DPM have both changed state since last clear DPM and clear LOS occurred.

Figure 3: LXT307 SIO Write Operation

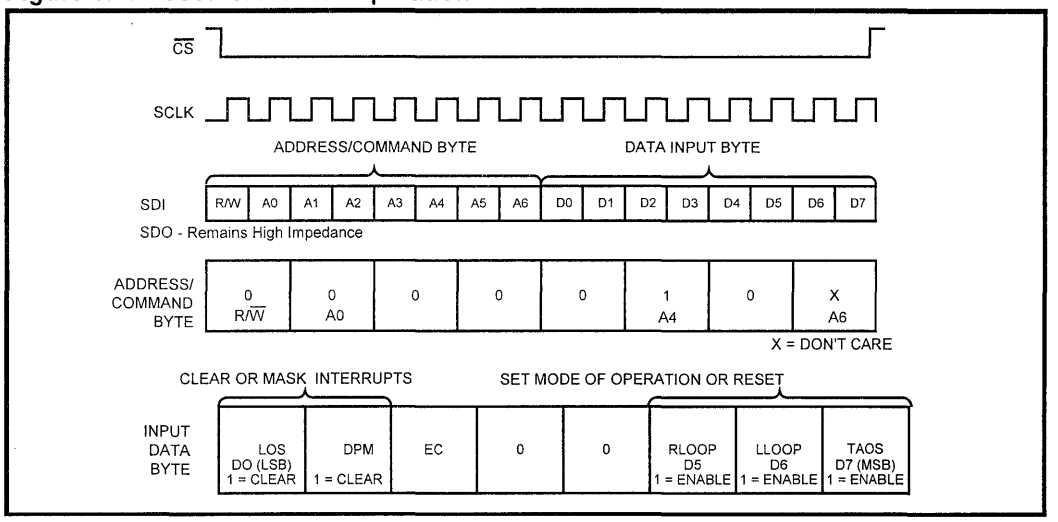


Figure 4: LXT307 SIO Read Operation

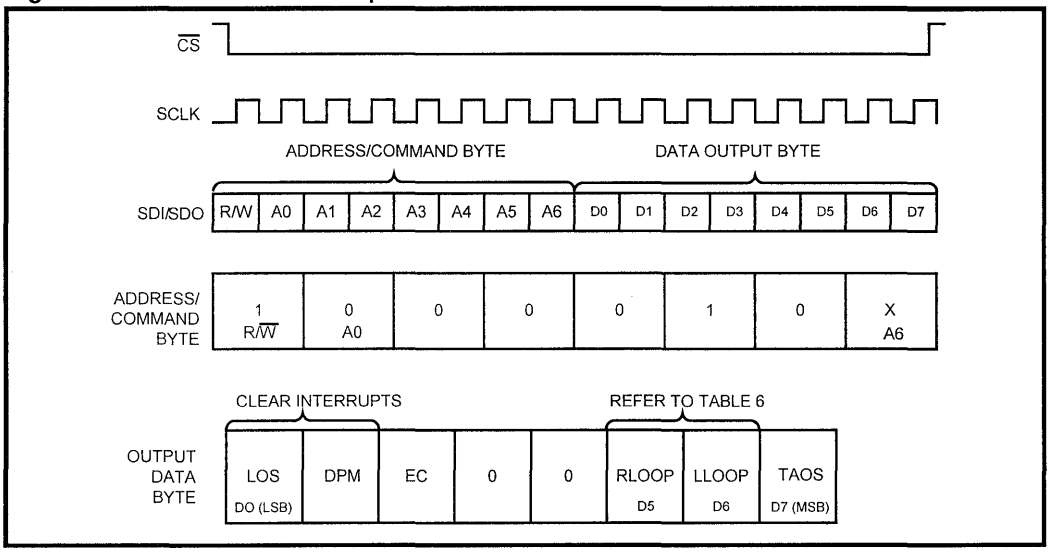
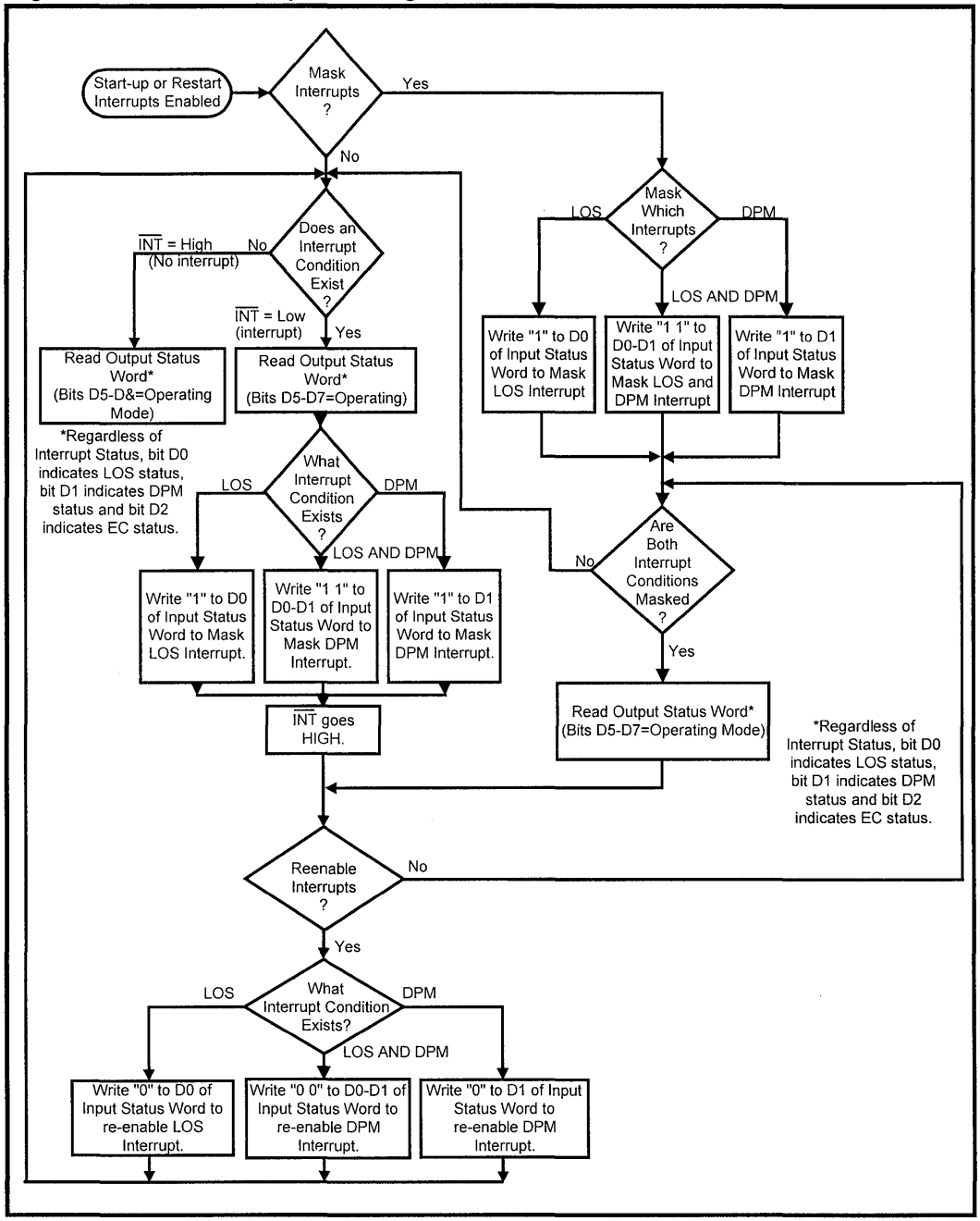


Figure 5: LXT307 Interrupt Handling



Diagnostic Mode Operation

TAOS

See Figures 6 and 7. In Transmit All Ones (TAOS) mode, the TPOS and TNEG inputs to the transceiver are ignored. The transceiver transmits a continuous stream of 1s at the TCLK frequency when TAOS is activated. TAOS can be commanded simultaneously with Local Loopback, but is inhibited during Remote Loopback.

Figure 6: TAOS

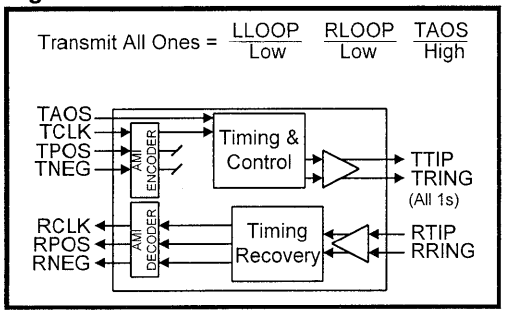
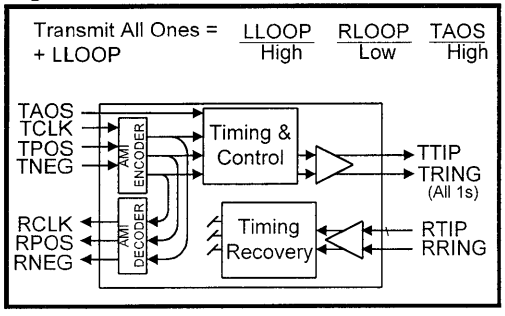


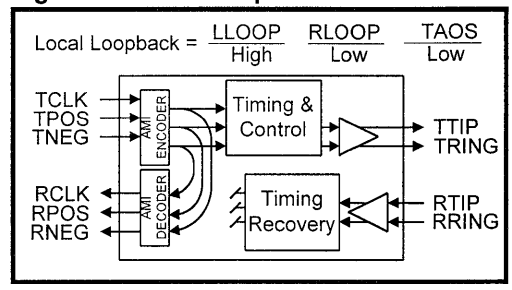
Figure 7: TAOS with LLOOP



LLOOP

See Figure 8. In Local Loopback (LLOOP) mode, the receiver circuits are inhibited. The transmit data and clock inputs (TPOS, TNEG and TCLK) are looped back onto the receive data and clock outputs (RPOS, RNEG and RCLK). The transmitter circuits are unaffected. The TPOS and TNEG inputs (or a stream of 1s if the TAOS command is active) will be transmitted normally.

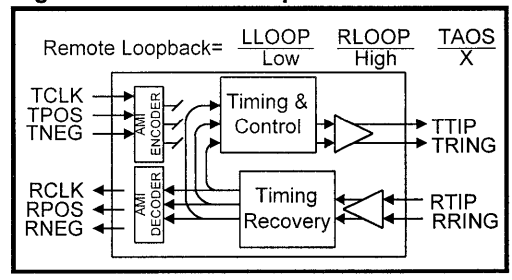
Figure 8: Local Loopback



RLOOP

See Figure 9. In Remote Loopback (RLOOP) mode, the transmit data and clock inputs (TPOS, TNEG and TCLK) are ignored. The RPOS and RNEG outputs are looped back through the transmit circuits and output on TTIP and TRING at the RCLK frequency. Receiver circuits are unaffected by the RLOOP command and continue to output the RPOS, RNEG and RCLK signals received from the twisted-pair line.

Figure 9: Remote Loopback



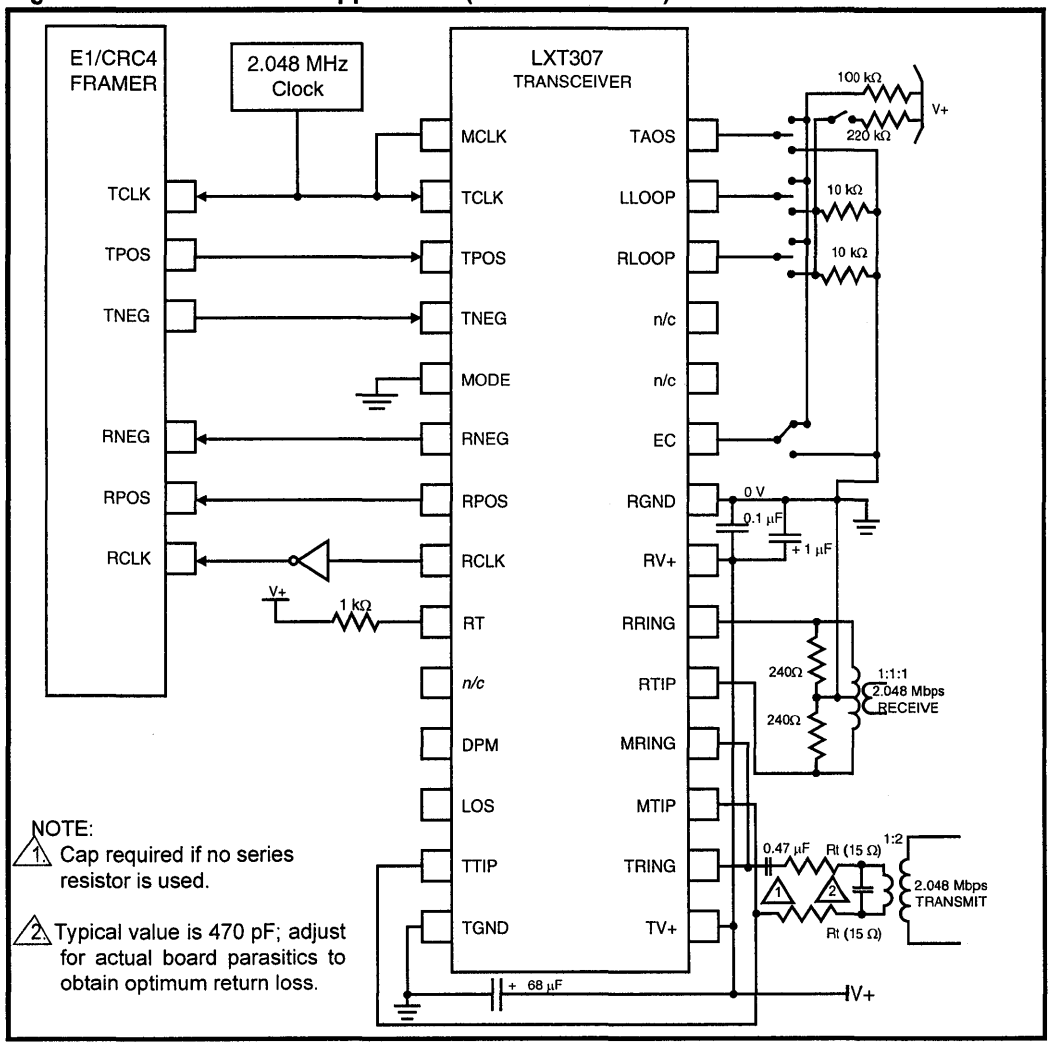
Application Information

NOTE

This application information is for design aid only.

Figure 10 is a 2.048 Mbps E1 120 Ω Twisted-Pair Wire application using EC code 1 and 15 Ω Rt resistors in line with the transmit transformer to provide high return loss and surge protection. When high return loss is not a critical factor, a 1:1 transformer without in-line resistors provides maximum power savings. Tables 7 and 8 list typical return loss figures for various transformer ratios, Rt values and the associated EC code for 75 Ω coax and 120 Ω twisted-pair applications, respectively. The LXT307 is shown in Hardware mode with a general G.704 Framer. The hard-wired control lines for TAOS, LLOOP and RLOOP are individually controllable, and the LLOOP and RLOOP lines are also tied to a single control for the Reset function.

Figure 10: LXT307 120 Ω Application (Hardware Mode)



E1 Coaxial Applications

Figure 11 shows the line interface for a typical E1 coaxial (75 Ω) application. The EC code should be set to 0 for coax. With 9.1 Ω Rt resistors in line with the 1:2 output transformers, the LXT307 produces 2.37 V peak pulses as required for coax applications. A 1:1:1 transformer is used on the receive side.

Table 7: Transformer Specifications

Parameter	Value
Turns Ratio Tx	1:2 (±2%)
Primary Inductance	1.2 mH min
Leakage Inductance	0.5 µH max
Interwinding Capacitance	25 pF max
Series Resistance	1.0 Ω PRI

Table 8: Transformer Selection Guide

Transformer Manufacturer	Part Number	Turns Ratio	Description
Pulse Engineering	PE65861	1:2	Dual SMD
	PE 65351	1:2	Single through hole
Bel Fuse	0553-5006	1:2	Dual
Schott	67127370	1:2	Single through hole
Midcom	671-5832	1:2	Single through hole

Figure 11: Line Interface for E1 Coax Applications

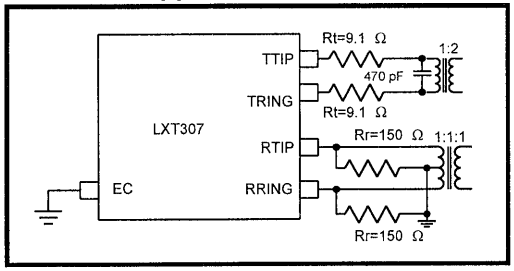


Table 9: 75 Ω Output Combinations

EC	Xfmr Ratio[1]	Rt Value[2]	Rtn Loss[3]
1	1: 1	Rt = 10 Ω	5 dB
1	1: 2	Rt = 14.3 Ω	10 dB
0	1: 1	Rt = 0 Ω[4]	0.5 dB
0	1: 2	Rt = 9.1 Ω	18 dB

1. Transformer turns ratio accuracy is ±2%.
2. Rt values are ±1%.
3. Typical return loss, 51 kHz - 3.0728 kHz.
4. Cap required if no series resistor is used.

Table 10: 120 Ω Output Combinations

EC	Xfmr Ratio[1]	Rt Value[2]	Rtn Loss[3]
1	1: 1	Rt = 0 Ω[4]	0.5 dB
1	1: 2	Rt = 15 Ω	18 dB
0	1: 2	Rt = 9.1 Ω	10 dB

1. Transformer turns ratio accuracy is ±2%.
2. Rt values are ±1%.
3. Typical return loss, 51 kHz - 3.0728 kHz.
4. Cap required if no series resistor is used.

Test Specifications

NOTE

The minimum and maximum values in Tables 11 through 17 and Figures 12 through 17 represent the performance specifications of the LXT307 and are guaranteed by test, except where noted by design.

Table 11: Absolute Maximum Ratings

Parameter	Sym	Min	Max	Units
DC supply (referenced to GND)	RV+, TV+	–	6.0	V
Input voltage, any pin[1]	VIN	RGND - 0.3	RV+ + 0.3	V
Input current, any pin[2]	IIN	-10	10	mA
Storage temperature	TSTG	-65	150	°C

CAUTION

Operations at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

1. Excluding RTIP and RRING which must stay between -6V and (RV+ + 0.3) V.
2. Transient currents of up to 100 mA will not cause SCR latch up. TTIP, TRING, TV+ and TGND can withstand a continuous current of 100 mA.

Table 12: Recommended Operating Conditions and Characteristics

Parameter	Sym	Min	Typ	Max	Units
DC Supply[1]	RV+, TV+	4.75	5.0	5.25	V
Ambient operating temperature	TA	-40	25	85	° C

1. TV+ must not exceed RV+ by more than 0.3 V.

Table 13: Electrical Characteristics (Over recommended operating conditions)

Parameter		Sym	Min	Typ	Max	Units	Test Conditions
Total power dissipation[1, 2]	75 Ω (EC = 0)	PD	–	260	320	mW	50% 1s density
	120 Ω (EC = 1)	PD	–	270	320	mW	
Total power consumption[3]	120 Ω (EC = 1)	PD	–	400	T.B.D.	mW	100% 1s density
High level input voltage[4] (pins 1-5, 23)		VIH	2.0	–	–	V	
Low level input voltage[4] (pins 1-5, 23)		VIL	–	–	0.8	V	
High level output voltage[4, 5] (pins 6-8, 11, 12, 23, 25)		VOH	2.4	–	–	V	IOUT = -400 µA
Low level output voltage[4, 5] (pins 6-8, 11, 12, 23, 25)		VOL	–	–	0.4	V	IOUT = 1.6 mA
Input leakage current[6]		ILL	0	–	±10	µA	
Three-state leakage current (pin 25)		I3L	0	–	±10	µA	

1. Device power dissipation while driving a 75 or 120 Ω load over operating temperature range. Digital input levels are within 10% of the supply rails and digital outputs are driving a 50 pF capacitive load. Rt = 0 Ω; transformer ratio = 1:1.
2. Guaranteed by design and other correlation methods.
3. Power consumption while driving a 60 Ω effective load. Includes device and load. Rt = 15 Ω; transformer ratio = 1:2; EC = 1.
4. Functionality of pin 23 depends on mode. See Host/Hardware Mode Descriptions.
5. Output drivers will output CMOS logic levels into CMOS loads.
6. Except MTIP and MRING ILL = ±50 µA.

Table 14: Analog Characteristics (Over recommended operating conditions)

Parameter		Min	Typical[1]	Max	Units	Test Conditions
AMI output pulse amplitudes	75 Ω	2.14	2.37	2.6	V	G.703
	120 Ω	2.7	3.0	3.3	V	G.703
Peak voltage of a space	75 Ω	-0.237	0	+0.237	V	
	120 Ω	-0.3	0	+0.3	V	
Ratio of the widths of positive and negative pulses at the nominal half amplitude		95	–	105	%	
Ratio of the amplitudes of positive and negative pulses at the center of the pulse interval		95	–	105	%	
Recommended output load at TTIP and TRING		–	75	–	Ω	
Driver output impedance[4]			3	10	Ω	
Driver short circuit current[2]				50	mA	
Jitter added by the transmitter	10 Hz - 8 kHz[4]	–	–	0.01	UI	G.823
	18 kHz - 100 kHz[4]	–	–	0.025	UI	G.823
	20 Hz - 100 kHz[4]	–	–	0.025	UI	G.823
	Broad Band[3]	–	0.025	0.050	UI	
Receiver sensitivity	(0 dB = 2.4 V)	13.6	–	–	dB	
		500	–	–	mV	
Receiver input impedance		–	40	–	kΩ	
Signal to interference ratio (FEXT)[4]		15	–	–	dB	G.703, O.151
Input jitter tolerance 18 kHz - 100 kHz		0.4	–	–	UI	G.823
Loss of Signal threshold		–	20	–	dB	below nominal
Data decision threshold[4]		43	50	57	% peak	
Allowable consecutive zeros before LOS[4]		160	175	190	–	G.775
LOS reset transition window[4]		–	32	–	bit	four transitions

		Transmit		Receive			
		Min	Typ[1]	Min	Typ[1]		
Minimum return loss[4]	51 Hz – 102 kHz	18	20	20	–	dB	Dynamic conditions per ETS 300 166 and ITU G.703. See Figures 10, 11.
	102 kHz –2.048 MHz	18	20	20	–	dB	
	2.048 MHz – 3.072 MHz	18	20	20	–	dB	

1. Typical values are measured at 25 °C and are for design aid only. Not guaranteed or subject to production testing.
2. Per OFTEL OTR-001/BABT BS4650 with 15 Ω termination resistors and a 1:2 transmit transformer on a 0.5 Ω test load.
3. Input signal to TCLK is jitter-free.
4. Guaranteed by design or other correlation methods.

Figure 12: 2.048 Mbps Pulse Mask Template

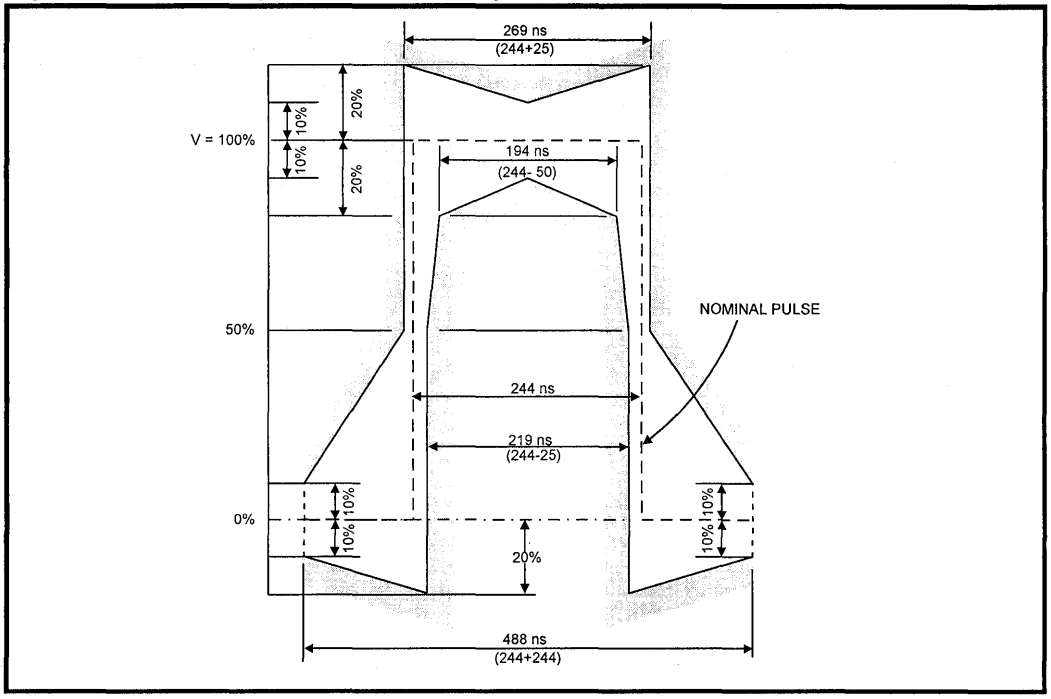


Table 15: Receive Timing Characteristics *(Over recommended operating conditions)*

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Receive clock duty cycle	RCLKd	40	–	60	%	
Receive clock pulse width	tPW	–	244	–	ns	
RPOS/RNEG to RCLK rising setup time	tSUR	–	194	–	ns	
RCLK rising to RPOS/ RNEG hold time	tHR	–	194	–	ns	

1. Typical values are at 25 °C and are for design aid only; they are not guaranteed and not subject to production testing.

Figure 13: LXT307 Receive Clock Timing

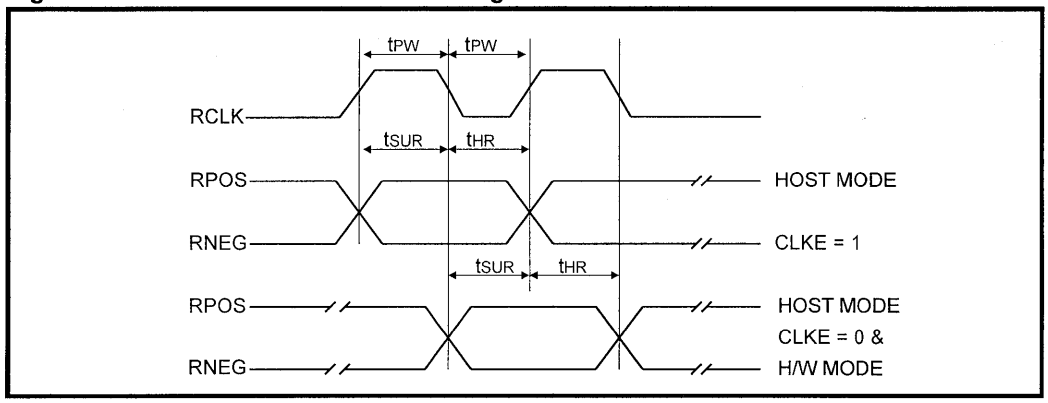


Figure 14: LXT307 Transmit Clock Timing

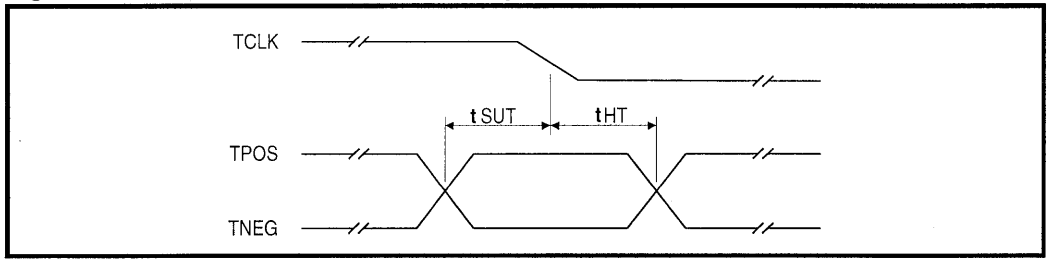


Table 16: Transmit Timing Characteristics *(over recommended operating conditions)*

Parameter	Sym	Min	Typ[1]	Max	Units
Master clock frequency	MCLK	–	2.048	–	MHz
Master clock tolerance	MCLKt	–	±100	–	ppm
Master clock duty cycle	MCLKd	40	–	60	%
Transmit clock frequency	TCLK	–	2.048	–	MHz
Transmit clock tolerance	TCLKt	–	±50	–	ppm
Transmit clock duty cycle	TCLKd	10	–	90	%
TPOS/TNEG to TCLK setup time	tSUT	25	–	–	ns
TCLK to TPOS/TNEG hold time	tHT	25	–	–	ns

1. Typical values are at 25 °C and are for design aid only; they are not guaranteed and not subject to production testing.

Table 17: Serial I/O Timing Characteristics (Over recommended operating conditions)

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Rise time - any digital output	tR	–	–	100	ns	Load 1.6 mA, 50 pF
Fall time - any digital output	tF	–	–	100	ns	Load -400 µA, 50 pF
SDI to SCLK setup time	tDC	50	–	–	ns	
SCLK to SDI hold time	tCDH	50	–	–	ns	
SCLK low time	tCL	240	–	–	ns	
SCLK high time	tCH	240	–	–	ns	
SCLK rise and fall time	tR, tF	–		50	ns	
$\overline{CS}$ to SCLK setup time	tCC	50	–	–	ns	
SCLK to $\overline{CS}$ hold time	tCCH	50	–	–	ns	
$\overline{CS}$ inactive time	tCWH	250	–	–	ns	
SCLK to SDO valid	tCDV	–	–	200	ns	
SCLK falling edge or $\overline{CS}$ rising edge to SDO high Z	tCDZ	–	100	–	ns	

1. Typical values are at 25° C and are for design aid only; they are not guaranteed and not subject to production testing.

Figure 15: LXT307 Serial Data Input Timing Diagram

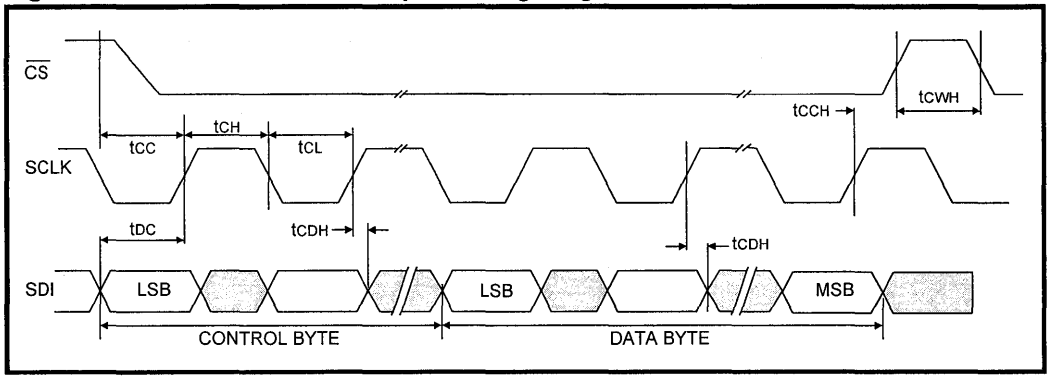


Figure 16: LXT307 Serial Data Output Timing Diagram

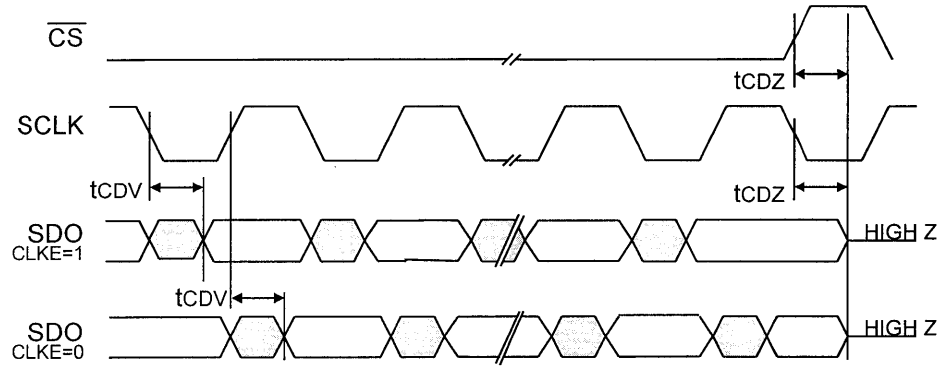
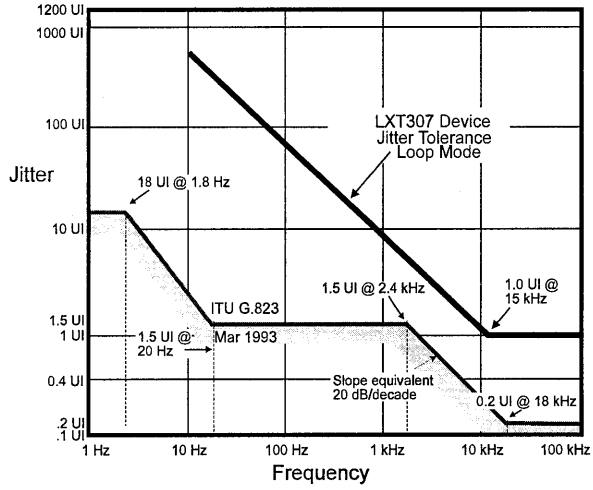


Figure 17: Typical Receiver Input Jitter Tolerance (Loop Mode)



NOTES

LXT325

T1/E1 Integrated Quad Receiver

General Description

The LXT325 quad receiver is a fully-integrated, quadruple-PCM receiver for both 1.544 Mbps, and 2.048 Mbps applications. It incorporates four independent receivers in a single 28-pin DIP or PLCC, or a 44-pin QFP. Each LXT325 receiver also incorporates a Loss Of Signal (LOS) detection circuit and output driver. The operating frequency is pin selectable.

These receivers perform data and timing recovery, and use peak detection and a variable threshold to reduce impulsive noise. Receiver sensitivity down to 500 mV allows for up to 13.6 dB of attenuation.

The LXT325 quad receiver is an advanced, double-poly, double-metal CMOS device and requires only a single 5-volt power supply.

Applications

- High-density T1/E1 line cards
- M13, E13 line interfaces
- Test equipment
- Line monitoring
- Receive line interface

Features

- Four independent 1.544/2.048 Mbps receivers
- Loss Of Signal (LOS) output for each receiver
- Circuit functions include data and clock recovery
- Single Master Clock input
- Meets or exceeds AT&T PUB 62411 ITU-T G.703 and ITU G.823 requirements for jitter tolerance
- Unipolar RPOS and RNEG outputs
- Minimum receive signal of 500 mV
- Selectable slicer levels (DSX-1/E1) to provide improved SNR
- CMOS technology requires only single 5 V power input
- Available in 28-pin plastic DIP and PLCC and 44-pin QFP packages
- -40 °C to 85 °C operating temperature range

LXT325 Block Diagram

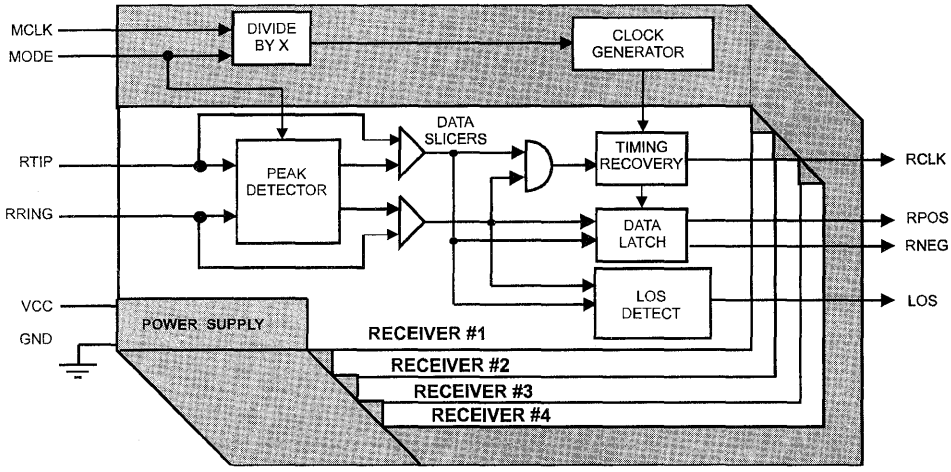


Figure 1: LXT325 Pin Assignments

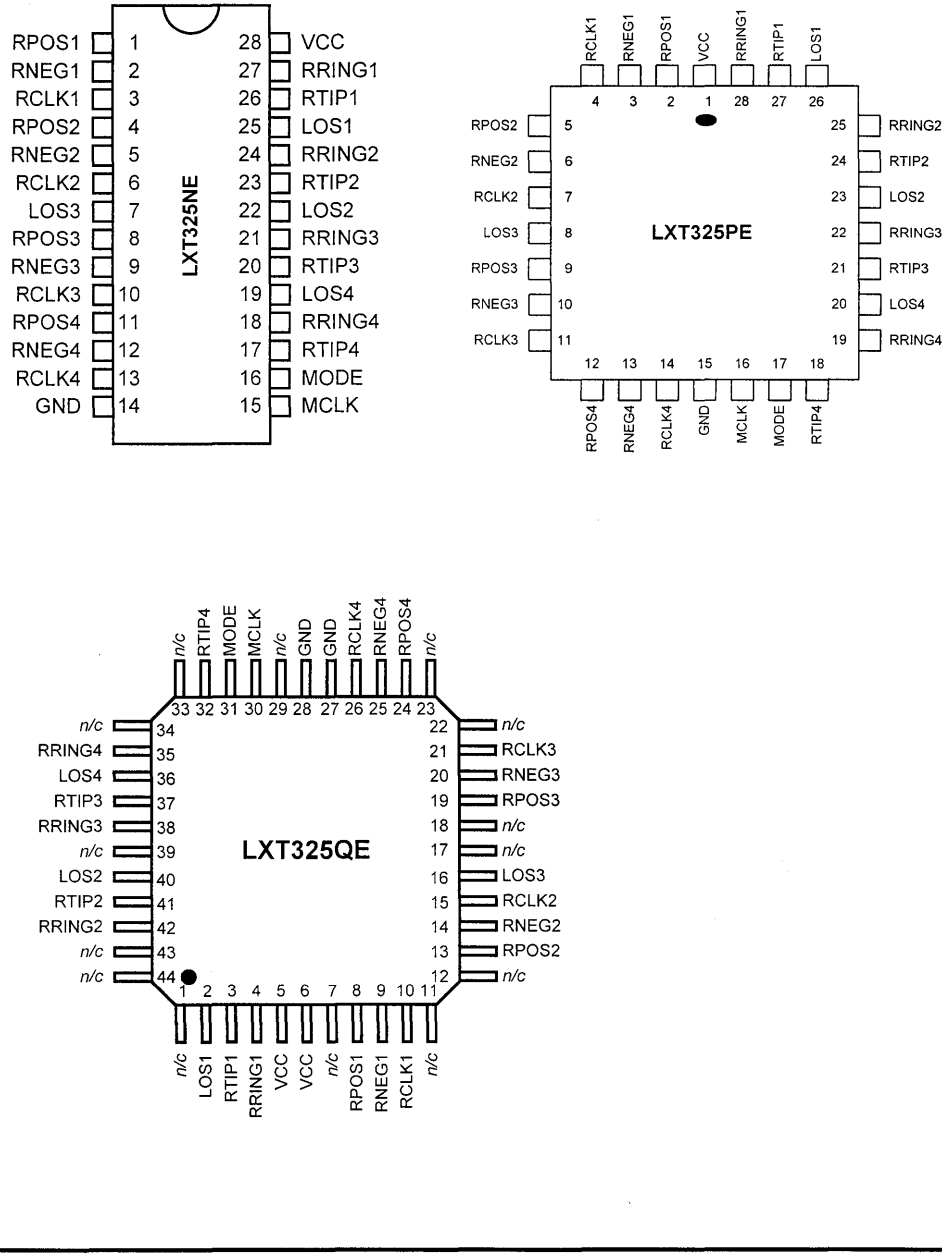


Table 1: Pin Assignments and Descriptions

Pin #			Symbol	I/O[2]	Description
DIP	PLCC	QFP[1]			
1 2	2 3	8 9	RPOS1 RNEG1	DO	**Receiver 1 Positive and Negative Data outputs**. A signal on RNEG*x* corresponds to receipt of a negative pulse on RTIP*x* and RRING*x*. A signal on RPOS*x* corresponds to receipt of a positive pulse on RTIP*x* and RRING*x*. RNEG*x* and RPOS*x* outputs are Non-Return-to-Zero (NRZ) signals. Both outputs are stable and valid on the rising edge of RCLK*x*.
3	4	10	RCLK1	DO	**Receiver 1 Recovered Clock**. Clock recovered from the inputs to RTIP1 and RRING1. See RPOS1/RNEG1.
4 5 6	5 6 7	13 14 15	RPOS2 RNEG2 RCLK2	DO	**Receiver 2 Data and Clock outputs.** Signals recovered from the inputs to RTIP2 and RRING2. See RPOS1/RNEG1/RCLK1.
7	8	16	LOS3	DO	**Receiver 3 Loss of Signal Detector**. LOS*x* pins go high when the associated receiver detects 175 consecutive spaces. The LOS output returns low when a mark is received.
8 9 10	9 10 11	19 20 21	RPOS3 RNEG3 RCLK3	DO	**Receiver 3 Data and Clock outputs.** Signals recovered from the inputs to RTIP3 and RRING3. See RPOS1/RNEG1/RCLK1.
11 12 13	12 13 14	24 25 26	RPOS4 RNEG4 RCLK4	DO	**Receiver 4 Data and Clock outputs**. Signals recovered from the inputs to RTIP4 and RRING4. See RPOS1/RNEG1/RCLK1.
14	15	27 28	GND	–	**Ground.**
15	16	30	MCLK	DI	**Master Clock**. A 1.544 MHz or 2.048 MHz clock input used to generate internal clocks. Upon loss of signal, MCLK serves as the source for all the RCLK*x* signals.
16	17	31	MODE	DI	**Mode Selection**. Set MODE high for 50% slicer level. This setting is mandatory for 2.048 Mbit/s operation and provides maximum sensitivity in 1.544 Mbit/s designs. Where undershoot will exceed 45% in 1.544 MHz applications, pull MODE low to set the slicer levels to 70%.
17 18	18 19	32 35	RTIP4 RRING4	AI	**Receiver 4 Tip and Ring**. The AMI signal received from the 4th twisted-pair line is applied at these pins. A center-tapped, center-grounded transformer is required on these pins. Data and clock from the signal applied at these pins are recovered and output on the RPOS*x*/RNEG*x*, and RCLK*x* pins.
19	20	36	LOS4	DO	**Receiver 4 Loss of Signal Detector**. See LOS3.
20 21	21 22	37 38	RTIP3 RRING3	AI	**Receiver 3 Tip and Ring Inputs**. See RTIP4/RRING4.
22	23	40	LOS2	DO	**Receiver 2 Loss of Signal detector**. See LOS3.

1. Pins 1, 7, 11, 12, 17, 18, 22, 23, 29, 33, 34, 39, 43 and 44 have no function in the 44-pin QFP package. All applications should leave them unconnected.
2. Entries in the I/O column are DI = Digital Input; DO = Digital Output; AI = Analog Input.

Table 1: Pin Assignments and Descriptions – continued

Pin #			Symbol	I/O[2]	Description
DIP	PLCC	QFP[1]			
23 24	24 25	41 42	RTIP2 RRING2	AI	**Receiver 2 Tip and Ring Inputs**. See RTIP4/RRING4.
25	26	2	LOS1	DO	**Receiver 1 Loss of Signal Detector**. See LOS3.
26 27	27 28	3 4	RTIP1 RRING1	AI	**Receiver 1 Tip and Ring Inputs**. See RTIP4/RRING4.
28	1	5,6	VCC	–	+5 VDC Power Supply

1. Pins 1, 7, 11, 12, 17, 18, 22, 23, 29, 33, 34, 39, 43 and 44 have no function in the 44-pin QFP package. All applications should leave them unconnected.
2. Entries in the I/O column are DI = Digital Input; DO = Digital Output; AI = Analog Input.

FUNCTIONAL DESCRIPTION

The LXT325 quad receiver is a fully-integrated, PCM receiver for both 1.544 Mbit/s (DSX-1) and 2.048 Mbit/s (E1) applications. The MCLK frequency and the MODE pin input level set the mode of operation. The LXT325 is a low-power CMOS device operating from a single +5 V power supply.

The figure at the front of the Data Sheet shows a simplified block diagram of the LXT325. The input signal is received from the twisted-pair line on each side of a center-grounded transformer. (Positive pulses are received at RTIP and negative pulses are received at RRING.) This differential signal is processed through the peak detector and data slicers. The peak detector samples the inputs and determines the maximum value of the received signal. A percentage of the peak value is provided to the data slicers as a threshold level to ensure optimum signal-to-noise ratio.

For E1 applications the threshold is set to 50% of the peak value (MODE set High). In 1.544 Mbit/s applications where undershoot does not exceed 45%, MODE may be set High (50% of the peak value) for the maximum sensitivity and noise margin. In applications where the undershoot exceeds 45% the MODE must be set Low. With MODE Low, the slicer threshold is set to 70% of the peak value. This threshold is maintained above 65% for up to 15 consecutive zeros over the range of specified operating conditions.

The slicer threshold is maintained through a capacitive storage arrangement and a combination of Refresh and Bleed-off circuitry. This design balance prevents the refresh circuitry from driving the threshold too high, while ensuring that it is maintained over long strings of successive zeros.

These receivers are capable of accurately recovering signals with up to 13.6 dB of attenuation (from 2.4 V), corresponding to a received signal level of 500 mV. Maximum cable length is 1500 feet of ABAM cable (approximately 6 dB), with the additional attenuation being resistive flat loss. Regardless of received signal level, the peak detectors are held above a minimum level of 150 mV to provide immunity from impulsive noise.

After processing through the data slicers, the received signal is routed to the data and clock recovery sections. Recovered clock signals are supplied to the data latch. The recovered data is synchronized with the recovered clock (RCLK), then output at RNEG and RPOS. RPOS and RNEG outputs are valid on the rising edge of RCLK.

LINE INTERFACE

The LXT325 quad receiver interfaces with four twisted-pair lines (one twisted-pair for each receiver) through standard pulse transformers and appropriate resistors. Recommended transformer characteristics are listed in Table 2.

Table 2: Recommended Transformer Characteristics

Parameter		1:1:1	1:2:2	Unit
DC Resistance	Primary	1.0 Maximum	1.0 Maximum	Ω
	Secondary	1.0 Maximum	1.0 Maximum	Ω
Primary inductance (Line Side)		1.2 typical	0.5 Maximum	mH
Leakage inductance		0.5 Maximum	1.0 Maximum	µH
Interwinding capacitance		25 Maximum	40 Maximum	pF

APPLICATION INFORMATION

The LXT325 quad receiver is compatible with both DSX-1 and E1 systems. Low, +5 V only, power consumption simplifies design considerations where multiple receivers are required. The LXT325 is well-suited for use in both line interface equipment and monitor applications. The primary difference in circuit design between these two applications is the input transformer. The typical DSX-1 pulse seen in test equipment requires a 1:1:1 transformer at the receiver input. The attenuated pulse seen in monitor applications may require a 1:2:2 transformer to boost the input signal. Figure 2 is a typical 1.544 Mbit/s DSX-1 application. The LXT325 is shown tapped into the cross connect frame with 800 Ω resistors across each leg of the center-tapped, center-grounded, 1:2:2 step-up transformer.

Figure 2: Typical T1 Test/Monitor Equipment Application

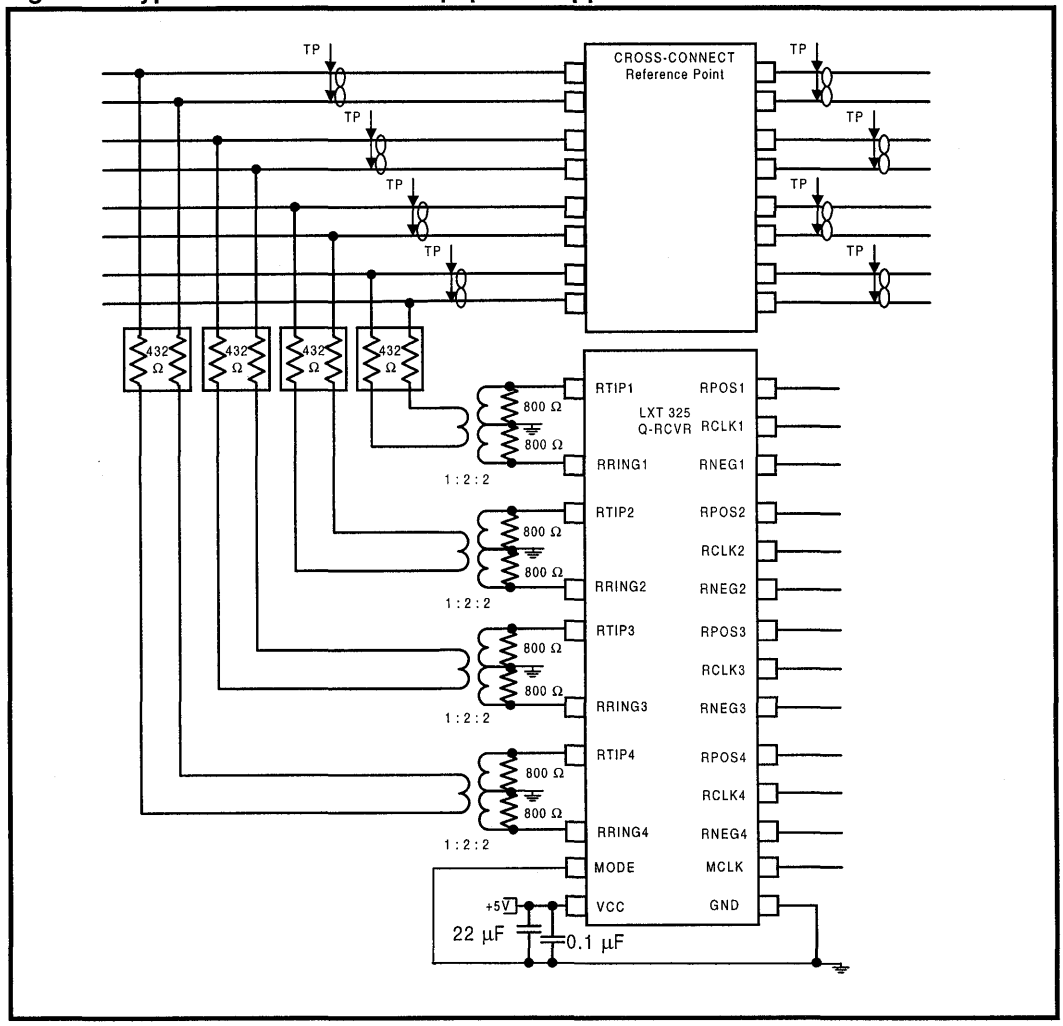
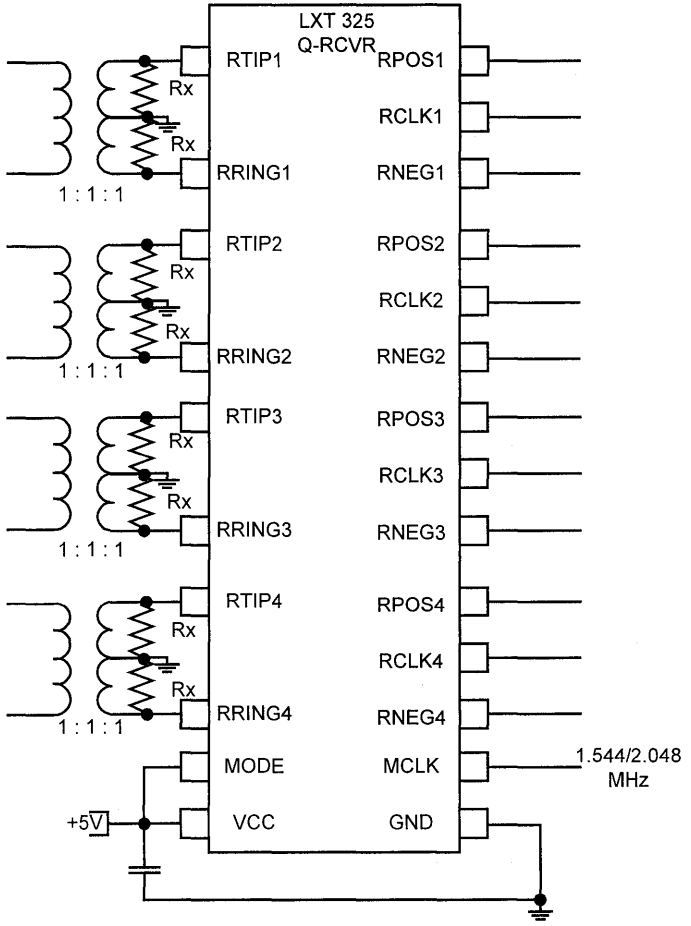


Figure 3: Typical DSX-1/E1 Receiver Application



NOTES:
Rx = 200 Ω for DSX-1 (100 Ω, TP, T1) applications
Rx = 240 Ω for E1 (120 Ω, TP, E1) applications
Rx = 150 Ω for E1 (75 Ω, coax, E1) applications

TEST SPECIFICATIONS

NOTE

The minimum and maximum values in Tables 3 through 6 and Figures 4 represent the performance specificatons of the LXT325 and are guaranteed by test, except where noted by design.

Table 3: Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Supply voltage	VCC	-0.3 V	6 V	V
Input voltage, any I/O pin[1]	VI/O	GND - 0.3 V	VCC + 0.3 V	V
Input current, any I/O pin[2]	II/O	-10	10	mA
Storage temperature	TST	-65	150	°C

CAUTION

Exceeding these values may cause permanent damage to the device. Operation under these conditions is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1. Excluding RTIP and RRING which must stay within -6 V to VCC +0.3 V
2. Transient currents of up to 100 mA will not cause SCR latch-up.

Table 4: Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Supply Voltage[1]	VCC	4.75	5	5.25	V
Power dissipation	PD	1	–	1	W
Operating Temperature	TOP	-40	–	85	°C

1. Voltages are with respect to ground unless otherwise stated.

Table 5: DC Electrical Characteristics[1]

Parameter	Sym	Min	Typ	Max	Units	Test Conditions
Supply current	ICC	–	–	40	mA	
Input High voltage	VIH	2.0	–	–	V	Digital Inputs
Input Low voltage	VIL	–	–	0.8	V	Digital Inputs
Output High voltage	VOH	2.4	–	–	V	IO = 0.4 mA
Output Low voltage	VOL	–	–	0.4	V	IO = 1.6 mA
Input leakage current	ILL	–	–	±10	µA	Digital inputs
Output current	IH	–	–	1.6	mA	VO = 0.4 V
Output rise/fall time	TRF	–	–	25	ns	15 pF load

1. Clocked operation over recommended temperature and power supply ranges.

Table 6: Receiver Characteristics

Parameter		Sym	Min	Typ[1]	Max	Units	Test Conditions
Slicer ratio	Mode=Low	SRD	63	70	77	%	
	Mode=High	SRC	43	50	57	%	
Dynamic Range		DR	0.50	–	3.6	VPEAK	
Undershoot		US	–	–	62	%	
Sensitivity below DSX (0 dB = 2.4 V)		–	13.6	–	–	dB	maximum of 6 dB cable loss, with balance being resistive loss.
		–	500	–	–	mV	
Error-Free Signal-to-Crosstalk ratio	2.048 MHz	S/X	14	–	–	dB	Single frequency interference production test guarantees error-free operation as specified in G.703, *f* 6.3.4 (Testing for 1.544 MHz systems uses a 1.544 Mbit/s QRSS interfering signal; MODE = 1.)
	1.544 MHz	S/X	12	–	–	dB	

1. Typical figures are at 25 °C and are design aids only; not guaranteed and not subject to production testing.

Figure 4: Clock Timing Diagram

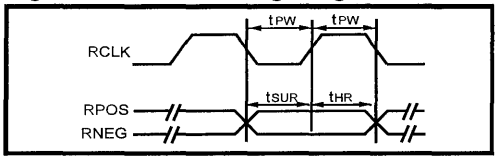


Table 7: Master and Receive Clock Timing Characteristics (See Figure 4)

Parameter		Sym	Min	Typ[1]	Max	Units	Test Conditions
Master Clock Frequency	DSX-1	MCLK	–	1.544	–	MHz	
	E1	MCLK	–	2.048	–	MHz	
Master Clock Tolerance		MCLKt	–	±100	–	ppm	
Master Clock duty cycle		MCLKd	40	50	60	%	
Receive Clock duty cycle		RCLKd	40	50	60	%	
Receive Clock pulse width	1.544 Mbit/s	tPW	270	325	378	ns	
	2.048 Mbit/s	tPW	203	244	285	ns	
RPOS/RNEG to RCLK rising setup time	1.544 Mbit/s	tSUR	50	270	–	ns	
	2.048 Mbit/s	tSUR	50	203	–	ns	
RCLK rising to RPOS/RNEG hold time	1.544 Mbit/s	tHR	50	270	–	ns	
	2.048 Mbit/s	tHR	50	203	–	ns	
Rise/fall time–any digital output		TRF	–	–	25	ns	

1. Typical figures are at 25 °C and are design aids only; not guaranteed and not subject to production testing.

NOTES

LXT331

Dual T1/E1 Line Interface Unit

General Description

The LXT331 is a Dual Line Interface Unit (DLIU) optimized for North America 1.544 Mbps (T1) and international 2.048 Mpbs (E1/CEPT) applications. It features a constant low output impedance transmitter for high return loss. Transmit pulse shape is selectable for various line lengths and cable types. The data recovery circuit also offers selectable slicer ratios for T1 or E1 applications.

The LXT331 offers both a serial interface (SIO) for microprocessor control and a hardware control mode for standalone operation.

The LXT331 offers a variety of advanced diagnostic and performance monitoring features. It uses an advanced double-poly, double-metal CMOS process and requires only a single 5-volt power supply.

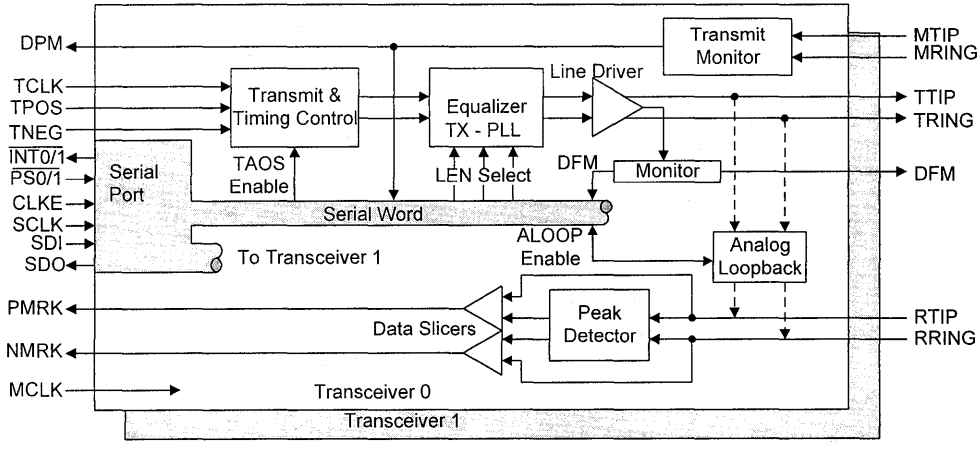
Applications

- Digital Access and Cross-connect Systems (DACS)
- T1 / E1 Multiplexer
- SONET/SDH Multiplexers
- Digital Loop Carrier (DLC) terminals
- Cost efficient analog frontend for Digital Backend ASICS
- Analog LOS using PMRK/NMRK

Features

- Complete line driver and data recovery functions
- Constant low output impedance transmitter with programmable equalizer shapes pulses to meet DSX-1 pulse template from 0 to 655 ft
- High transmit and receive return loss
- Meets or exceeds industry specifications including ITU G.703 and ANSI T1. 102-1993
- Compatible with industry standard framers
- Minimum receive signal of 500 mV, with selectable slicer levels (E1/DSX-1) to improve SNR
- Analog loopback function
- Transmit performance monitors with Driver Fail Monitor (DFM) output for transmit driver short circuit detection
- Transmit Driver Performance Monitor (DPM) output with external monitor pins MTIP and MRING
- Available in 44-pin PLCC and 44-pin QFP

LXT331 Block Diagram



PIN ASSIGNMENTS & SIGNAL DESCRIPTION

Figure 1: LXT331 Pin Assignments

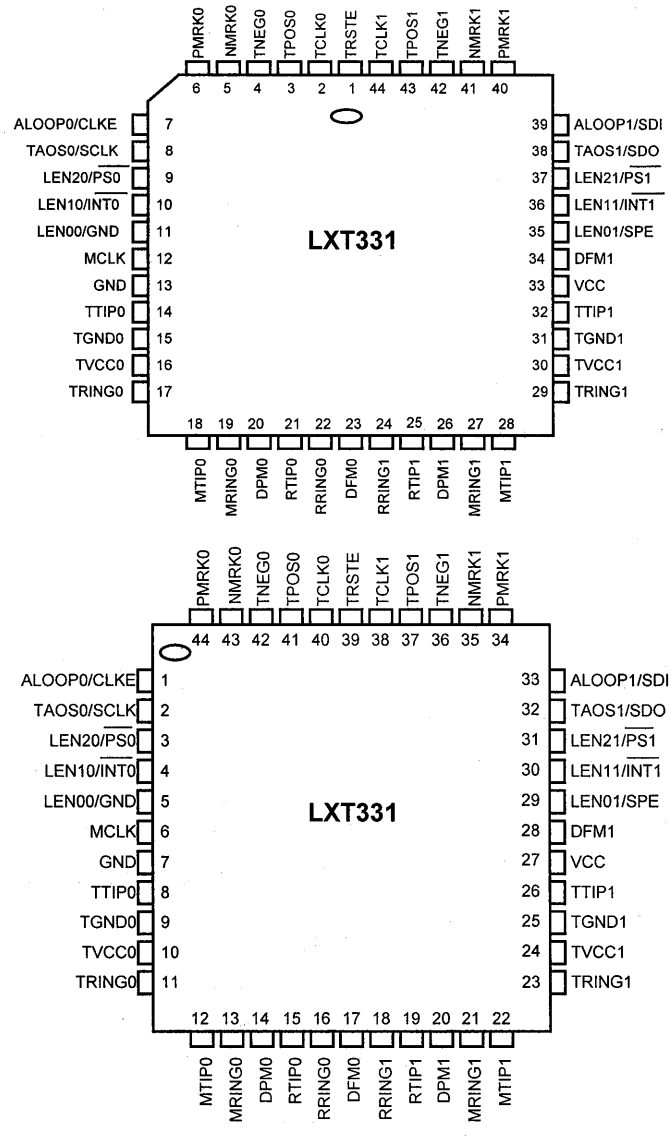


Table 1: Pin Descriptions

Pin PLCC	Pin QFP	Symbol	I/O[1]	Description
1	39	TRSTE	DI	**Tristate Enable**. Forces all output pins to tri-state when held High and forces chip into reset mode. Holds reset mode for 6 µs after TRSTE returns Low.
2	40	TCLK0	DI	**Transmit Clock — Port 0**. 1.544 MHz for T1, 2.048 MHz for E1. The transmit data inputs are sampled on the falling edge of TCLK. If TCLK0 is pulled Low, the transmit drivers are powered down and TTIP0 and TRING0 transmit outputs go to a high impedance state.
3 4	41 42	TPOS0 TNEG0	DI DI	**Transmit Positive and Negative Data — Port 0**. These pins are the positive and negative sides of a bipolar input pair for port 0. Data to be transmitted onto the line is input at these pins.
5 6	43 44	NMRK0 PMRK	DO DO	**Receive Negative and Positive Marks — Port 0**. These pins are the data outputs from port 0. A signal on NMRK corresponds to receipt of a negative pulse on RTIP/RRING. A signal on PMRK corresponds to receipt of a positive pulse on RTIP/RRING. NMRK/PMRK outputs are Return-to-Zero (RZ).
12	6	MCLK	DI	**Master Clock (1.544 MHz for T1. 2.048 MHz for E1)**. Can be held Low if TCLK is present.
13	7	GND	S	**Ground.** Ground return for power supply VCC.
14	8	TTIP0	AO	**Transmit Tip — Port 0**. The tip and ring pins for each port are differential driver outputs designed to drive a 35-200 Ω load. Line matching resistors and transformers can be selected to give the desired pulse height.
15	9	TGND0	S	**Ground**. Ground return for supply TVCC0.
16	10	TVCC0	S	**+ 5 volt power supply input for the port 0 transmit driver**. TVCC0 must not vary from TVCC1 or VCC by more than ± 0.3 V.
17	11	TRING0	AO	**Transmit Ring — Port 0**. The tip and ring pins for each port are differential driver outputs designed to drive a 35-200 Ω load. Line matching resistors and transformers can be selected to give the desired pulse height.
18 19	12 13	MTIP0 MRING0	AI AI	**Monitor Tip and Ring — Port 0**. These pins monitor tip and ring outputs, either its own or those of an adjacent LXT331 on the same board. If the application does not use this feature, tie one of these pins to a clock source and the other to a mid-level (referenced to the clock signal) voltage. (The clock frequency can range from 100 kHz to the TCLK frequency).
20	14	DPM0	DO	**Driver Performance Monitor — Port 0**. Output goes High on detection of 63 consecutive zeros, and goes Low on receipt of a one on transmit monitor loop (MTIP/MRING).
21 22	15 16	RTIP0 RRING0	AI AI	**Receive Tip and Ring — Port 0**. RTIP and RRING comprise the receive line interface. This input pair should be connected to the line through a 1:1 transformer.
23	17	DFM0	DO	**Driver Fail Monitor — Port 0**. Signal goes High to indicate driver output short.
24 25	18 19	RRING1 RTIP1	AI AI	**Receive Tip and Ring — Port 1**. Refer to pins RRING0 and RTIP0.
26	20	DPM1	DO	**Driver Performance Monitor — Port 1**. Refer to pin 20.
27 28	21 22	MRING1 MTIP0	AI	**Monitor Ring and Tip — Port 1**. Refer to pins MRING0 and MTIP0.
29	23	TRING1	AO	**Transmit Ring — Port 1**. Refer to pin TRING0.
30	24	TVCC1	DI	**+ 5 volt power supply** input for the port 0 transmit driver. TVCC1 must not deviate from TVCC0 or VCC by more than ± 0.3 V.
31	25	TGND1	S	**Ground**. Ground return for power supply TVCC1.
32	26	TTIP1	AO	**Transmit Tip — Port 1**. Refer to pin TTIP0.

Table 1: Pin Descriptions – continued

Pin PLCC	Pin QFP	Symbol	I/O[1]	Description
33	27	VCC	DI	**+ 5 VDC power supply** input for all circuits except the transmit drivers.
34	28	DFM1	DO	**Driver Fail Monitor — Port 1**. Refer to pin DFM0.
40 41	34 35	PMRK1 NMRK1	DO	**Receive Negative and Positive Marks — Port 1**. Refer to pins PMRK0 and NMRK0.
42 43	36 37	TNEG1 TPOS1	DI DI	**Transmit Negative and Positive Data — Port 1**. Refer to pins TNEG0 and TPOS0.
44	38	TCLK1	DI	**Transmit Clock — Port 1**. Refer to pin TCLK0.

Table 2: Host Mode Pin Descriptions

Pin PLCC	Pin QFP	Symbol	I/O[1]	Description
7	1	CLKE	DI	**Clock Edge Select**. When CLKE is High, SDO is valid on the rising edge of SCLK.When CLKE is Low, SDO is valid on the falling edge of SCLK.
8	2	SCLK	DI	**Serial Clock**. Shifts data into or our from the serial interface register of the selected port.
9	3	$\overline{PS0}$	DI	**Port Select — Port 0**. Inputs access the serial interface registers for the respective port. For each read or write operation, PS*n* must transition from High to Low, and remain Low.
10	4	$\overline{INT0}$	DO	**Interrupt — Port 0**. Outputs go Low to flag the host processor that the respective port has changed state. INT0 and INT1 are open drain outputs. Each must be tied to VCC through a resistor.
11	5	GND	S	**Ground**. Tie to ground.
35	29	SPE	DI	**Serial Port Enable**. SPE must be clocked with MCLK, TCLK0 or TCLK1 to enable Host Mode control through the serial port.
36	30	$\overline{INT1}$	DO	**Interrupt — Port 1**. Refer to pin $\overline{INT0}$.
37	31	$\overline{PS1}$	DI	**Port Select — Port 1**. Refer to pin $\overline{PS0}$.
38	32	SDO	DO	**Serial Data Output**. If CLKE is High, SDO is valid on the rising edge of SCLK. If CLKE is Low, SDO is valid on the falling edge of SCLK.
39	33	SDI	DI	**Serial Data Input**. SDI is sampled on the rising edge of SCLK.

1. I/O Designations: AI = Analog Input, AO = Analog Output, DI = Digital Input, DO = Digital Output, S = Power Supply

Table 3: Hardware Mode Pin Descriptions

Pin PLCC	Pin QFP	Symbol	I/O[1]	Description
7	1	ALOOP0	DI	**Analog Local Loopback Enable — Port 0**. When ALOOP is High, the RTIP/RRING inputs from the port 0 twisted-pair line are disconnected and the transmit data outputs (TTIP/TRING) are routed back into the receive inputs. For normal operation, hold ALOOP Low.
8	2	TAOS0	DI	**Transmit All Ones Enable — Port 0**. When TAOS is High, the TPOS/TNEG input is ignored and Port 0 transmits a stream of ones at the TCLK frequency. With no TCLK the MCLK input becomes the transmit reference. For normal operation, hold TAOS Low.
9 10 11	3 4 5	LEN20 LEN10 LEN00	DI DI DI	**Line Length Equalizer — Port 0**. Determine the shape and amplitude of the transmit pulse.
35 36 37	29 30 31	LEN01 LEN11 LEN21	DI DI DI	**Line Length Equalizer — Port 1**. Determine the shape and amplitude of the transmit pulse.
38	32	TAOS1	DI	**Transmit All Ones Enable — Port 1**. Refer to pin TAOS0.
39	33	ALOOP1	DI	**Analog Local Loopback Enable — Port 1**. Refer to pin ALOOP1.

1. I/O Designations: AI = Analog Input, AO = Analog Output, DI = Digital Input, DO = Digital Output, S = Power Supply

FUNCTIONAL DESCRIPTION

The LXT331 is a Dual Line Interface Unit (DLIU), which contains two ports. Refer to the simplified block diagram on page 1. The DLIU is designed for both 1.544 Mbps (DSX-1) and 2.048 Mbps (E1) applications. Both ports operate at the same frequency, which is determined by the TCLK input.

Each DLIU port front end interfaces with two lines, one line for transmit, one line for receive. These two lines comprise a digital data loop for full duplex transmission.

Each DLIU port back-end interfaces with a layer processor through bipolar data I/O channels. The DLIU may be controlled by a microprocessor through the serial port (Host control mode), or by hard-wired pins for stand-alone operation (Hardware control mode).

Receiver

The two receivers in the LXT331 DLIU are identical. The following paragraphs describe the operation of a single receiver.

The input signal is received via a 1:1 transformer. The receiver requires fully differential inputs which are internally self-biased into 2.5 V. Recovered data is output at PMRK and NMRK. Refer to Test Specifications for receiver timing.

The receive signal is processed through an adaptive peak detector and data slicers. The peak detector samples the received signal and determines its maximum value. A percentage of the peak value is provided to the data slicers as a threshold level to ensure optimum signal-to-noise ratio. For DSX-1 applications (line length inputs LEN0-LEN2 ≠ 000 or 001) the threshold is set to 70% (typical) of the peak value. This threshold is maintained above the specified level for up to 15 successive zeros over the range of specified operating conditions. For E1 applications (LENxn inputs = 000 or 001) the threshold is 50% (typical).

The receiver is capable of accurately recovering signals with up to -13.6 dB of attenuation (from 2.4 V), corresponding to a received signal level of approximately 500 mV. Maximum line length is 1500 feet of ABAM cable (approximately 6 dB of attenuation). Regardless of received signal level, the peak detectors are held above a minimum level of 0.3 V (typical) to provide immunity from impulsive noise. Built in pulse stretching circuitry maintains a minimum positive and negative mark pulse width (see Table 15 and Figure 14 on page 105).

Transmitter

The two transmitters in the LXT331 DLIU are identical. The following paragraphs describe the operation of a single transmitter.

Transmit data is clocked serially into the device at TPOS/TNEG. Input synchronization is supplied by the transmit clock (TCLK). The TPOS/TNEG inputs are sampled on the falling edge of TCLK. If TCLK is held Low the transmitter remains powered down and the TTIP/TRING outputs are held in a high-Z state, except during TAOS if MCLK is available. Each output driver is supplied by a separate power supply (TVCC0 or TVCC1). Current limiters on the output drivers provide short circuit protection. Refer to Test Specifications for TCLK timing characteristics. The LXT331 transmits data as a 50% AMI line code as shown in Figure 2.

Table 4: Equalizer Control Inputs - Hardware Mode[1]

LEN2	LEN1	LEN0	Line Length[2]	Cable Loss[3]	Application	Frequency
Low	High	High	0 - 133 ft ABAM	0.6 dB	DSX-1	1.544 MHz
High	Low	Low	133-266 ft ABAM	1.2 dB		
High	Low	High	266-399 ft ABAM	1.8 dB		
High	High	Low	399-533 ft ABAM	2.4 dB		
High	High	High	533-655 ft ABAM	3.0 dB		
Low	Low	Low	ITU Recommendation G.703		E1 - Coax (75 Ω) E1 - Twisted-pair (120 Ω)	2.048 MHz
Low	Low	High				
Low	High	Low	FCC Part 68, Option A		CSU	1.544 MHz

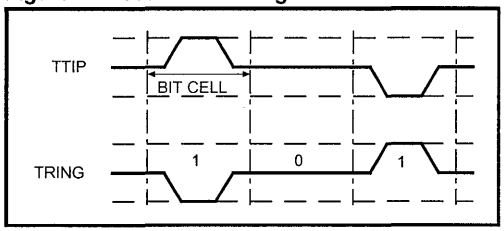
1. LEN*n* inputs are shown as High or Low for Hardware mode. For Host Mode serial inputs, High = 1 and Low = 0.
2. Line length from LXT331 to DSX-1 cross-connect point.
3. Maximum cable loss at 772 kHz.

Pulse Shape

The transmitted pulse shape is determined by Line Length equalizer control signals LEN0 through LEN2. Equalizer codes are hard-wired in Hardware mode as shown in Table 4. In Host mode the LEN*xn* codes are input through the serial interface. Shaped pulses are applied to the AMI line driver for transmission onto the line at TTIP and TRING. The line driver provides a constant Low output impedance of < 3 Ω (typical) regardless of whether it is driving marks or spaces or during transitions. This well-controlled impedance provides excellent return loss when used with external precision resistors (±1% accuracy). See Tables 8 and 9 for recommended transformer specifications, ratios, series resistor (Rt) values, and typical return losses for various LEN*xn* codes. To minimize power consumption the DC block capacitor and LXT331 can be connected directly to a 1:1.15 transformer without series resistors.

Pulses can be shaped for either 1.544 or 2.048 Mbps applications. 1.544 Mbps pulses for DSX-1 applications can be programmed to match line lengths from 0 to 655 feet of 22 AWG ABAM cable. A combination of 9.1 Ω resistors and a 1:2.3 transformer is recommended for DSX-1 applications and maximum transmit return loss. The LXT331 also matches FCC pulse mask specifications for CSU applications.

Figure 2: 50% AMI Coding



The LXT331 produces 2.048 Mbps pulses for both 75 Ω coaxial (2.37 V) or 120 Ω shielded twisted-pair (3.0 V) lines through an output transformer with a 1:2 turns ratio.

Driver Performance Monitor

The LXT331 incorporates a Driver Performance Monitor (DPM) as shown in Figure 3 on page 94. The DPM output goes High on receipt of 63 consecutive zeros and returns Low on receipt of a transition. A reset command also drives the output signal Low.

The LXT331 uses its MTIP and MRING pins to monitor its own TTIP and TRING outputs or those of an adjacent chip. Mark detection involves two measures:

3. Voltage threshold: a pulse must trip a threshold voltage above or below (depending on its polarity) the input bias voltage level. The LXT331 bias voltage is 2.5 V and the threshold for a mark is 2.5 ± 0.79 V.
4. Pulse width: the monitor distinguishes between marks and noise pulses by the pulse width. LXT331 requires a mark pulse to be at least 120 ns wide (typically).

There are two type of marks: Figure 2 labels them "A" and "B". C1 and C2 detect "A" marks; the AND gate (A1) ensures that both mark signals are present at the same time. If the pulse widths are adequate, with both a positive mark on MTIP and a negative mark on MRING, the A1 output goes High. Likewise C3 and C4 detect "B" marks. If the pulse meets the minimum width requirement, the AND gate (A2) output goes High when there are both a negative mark on MTIP and a positive mark on MRING. The OR gate (O1) passes the mark, as the signal "zero", on to the clock/counter circuit which controls the DPM output.

A latch samples the counter which goes High if the DPM circuit sees 63 consecutive zeros. Any mark resets the counter. The DPM signal goes High after the 63rd zero.

Driver Failure Monitor

The transceiver incorporates an internal Driver Failure Monitor (DFM) in parallel with TTIP and TRING. A capacitor, charged via a measure of the driver output current and discharged by a measure of the maximum allowable current detects driver failure. Shorted lines draw excess current, overcharging the cap. When the capacitor charge deviates outside the nominal charge window, a driver failure is reported. In Host mode the DFM bit is set in the serial word. In both Hardware and Host modes the DFM pin goes High. During a long string of spaces, a short-induced overcharge eventually bleeds off, clearing the DFM flag.

Control Modes

The LXT331 transceiver operates in standalone Hardware (default) Mode or Host Mode depending on the input to pin 35. When pin 35 is clocked by MCLK, TCLK0 or TCLK1, it acts as a Serial Port Enable (SPE) signal to force the LXT331 into the Host mode.

Host Mode Control

The LXT331 operates in the Host mode when pin 35 (SPE) is clocked. In Host mode a microprocessor controls the LXT331 through the serial I/O port (SIO) which provides common access to both LIUs. Each of the two LIUs contains a pair of data registers, one for command inputs and one for status outputs. An SIO transaction is initiated by a falling pulse on one of the two Port Select pins, $\overline{PS0}$ or $\overline{PS1}$. Only one LIU can be selected at a time. A High-to-Low transition on PS*n* is required for each subsequent access to the Host mode registers. If both $\overline{PS0}$ and $\overline{PS1}$ are active simultaneously, Port 0 has priority over Port1.

The LIU addressed by the $\overline{PSn}$ pulse responds by writing the incoming serial word from the SDI pin into its command register. Figure 4 on page 95 shows an SIO write operation. The 16-bit serial word consists of an 8-bit Command/Address byte and an 8-bit Data byte. If the command word contains a read request, the addressed LIU subsequently outputs the contents of its status register onto the SDO pin.

Figure 5 on page 96 shows an SIO read operation. The Clock Edge(CLKE) signal determines when the SDO output is valid, relative to the Serial Clock (SCLK) as follows:

If CLKE = High, SDO is valid on the rising edge of SCLK.
If CLKE = Low, SDO is valid on the falling edge of SCLK.
Refer to Test Specifications for SIO timing.

Serial Input Word

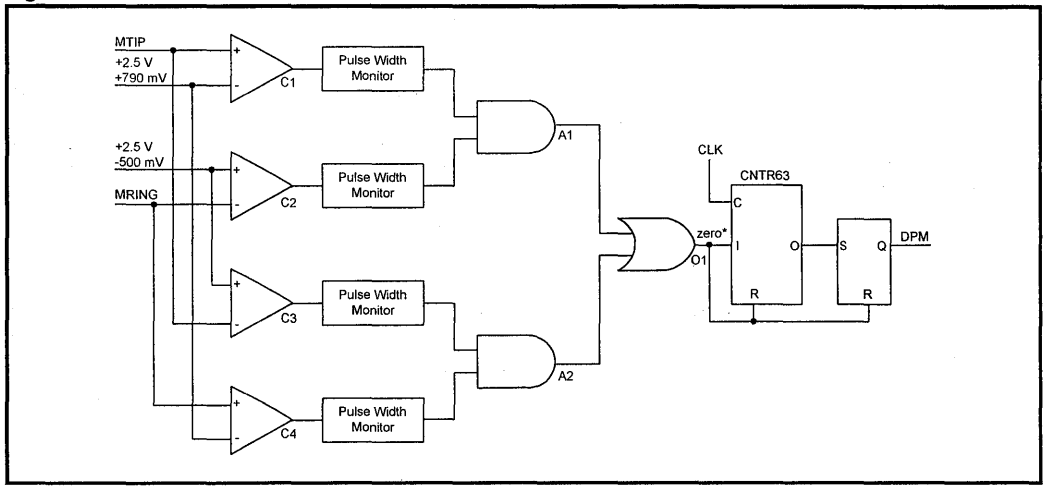
Figure 4 shows the Serial Input data structure. The LXT331 is addressed by setting bit A4 in the Address/Command byte, corresponding to address 16. Bit 1 of the serial Address/Command byte provides Read/Write (R/W) control when the chip is accessed. The R/W bit is set to logic 1 to read the data output byte from the chip, and set to logic 0 to write the input data byte to the chip.

The second 8 bits of a write operation, the Data Input byte, clear the Driver Performance Monitor (DPM) and Driver Fail Monitor (DFM) interrupts, reset the chip, and control diagnostic modes. The first and second bits (D0-1) clear and/or mask the DPM and DFM interrupts, and the last 2 bits (D6-7) control operating modes (normal and diagnostic) and chip reset. Refer to Table 5 for details on bits D6-7.

Table 5: SIO Input Bit Settings (See Figure 4)

Mode	TST Bit D5	ALOOP Bit D6	TAOS Bit D7
ALOOP	0	1	0
TAOS	0	X	1
RESET	1	1	0

Figure 3: LXT331 Driver Performance Monitor



Serial Output Word

Figure 5 shows the Serial Output data structure. SDO is high impedance when SDI receives an Address/Command byte. If SDI receives a write command (R/$\overline{W}$ = 0), SDO remains in high impedance. If the command is a read (R/$\overline{W}$ = 1), then SDO becomes active after the last Command/Address bit (A6) and remains active for eight SCLK cycles. Typically the first bit out of SDO changes the state of SDO from high Z to a Low/High. This occurs approximately 100 ns after the eighth following edge of SCLK.

The output data byte reports DPM and DFM conditions, equalizer settings, and operating modes (normal or diagnostic). The first 5 bits (D0-4) report DPM and DFM status and the Line Length Equalizer settings. The last 3 bits (D5-7) report operating modes and interrupt status as defined in Table 6 on page 96.

If the $\overline{INT}$ line for the respective port is High (no interrupt is pending), bits D5-7 report the operating modes listed in Table 6 on page 96. If the $\overline{INT}$ line for the respective port is Low, the interrupt status overrides all other reports and bits D5-7 reflect the interrupt status as listed in Table 6.

Interrupt Handling

The Host mode provides two latched Interrupt output pins, $\overline{INT0}$ and $\overline{INT1}$, one for each LIU. An interrupt is triggered by a change in the DPM or DFM bit (D0=DPM, D1=DFM). As shown in Figure 6, either or both interrupt generators can be masked by writing a 1 to the corresponding bit (D0 or D1) of the input data byte. When an interrupt has occurred, the $\overline{INT}$ output pin is pulled Low. The output stage of each $\overline{INT}$ pin consists only of a pull-down device. Hence, an external pull-up resistor is required. Clear the interrupts as follows:

1. If one or both interrupt bits (DPM or DFM - D0 or D1 of the output data byte) are high, write a 1 to the corresponding bit of the input data byte to clear the interrupt. Leave a 1 in either bit position to effectively mask that interrupt. To re-enable the interrupt capability, reset either D0 or D1 or both to 0.
2. If neither DPM nor DFM is high, reset the chip to clear the interrupt. To reset the chip, set data input bits D5 and D6 = 1, and D7 = 0.

Figure 4: LXT331 SIO Write Operations

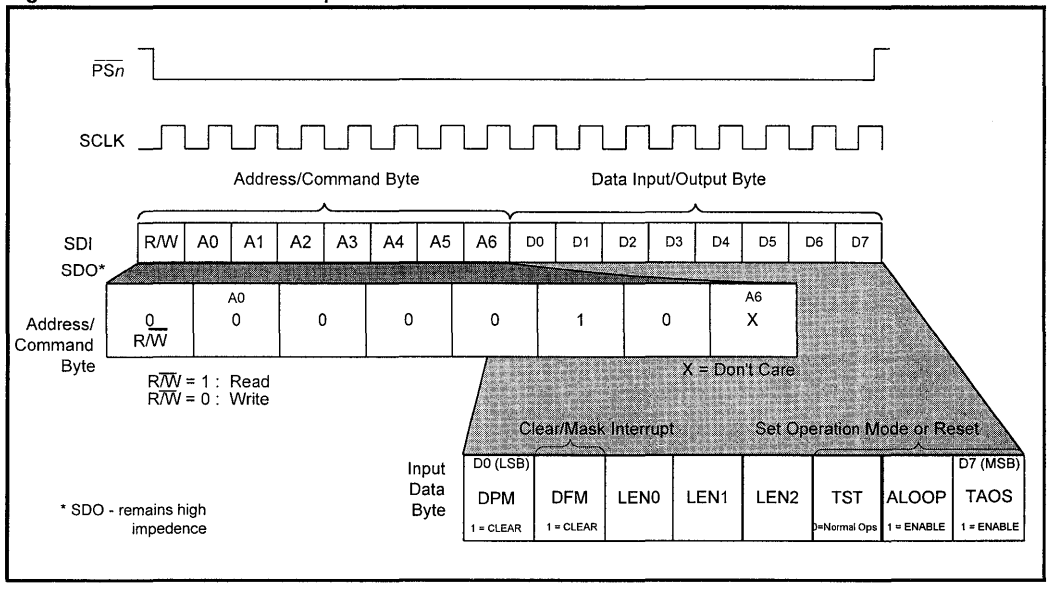


Figure 5: LXT331 SIO Read Operation

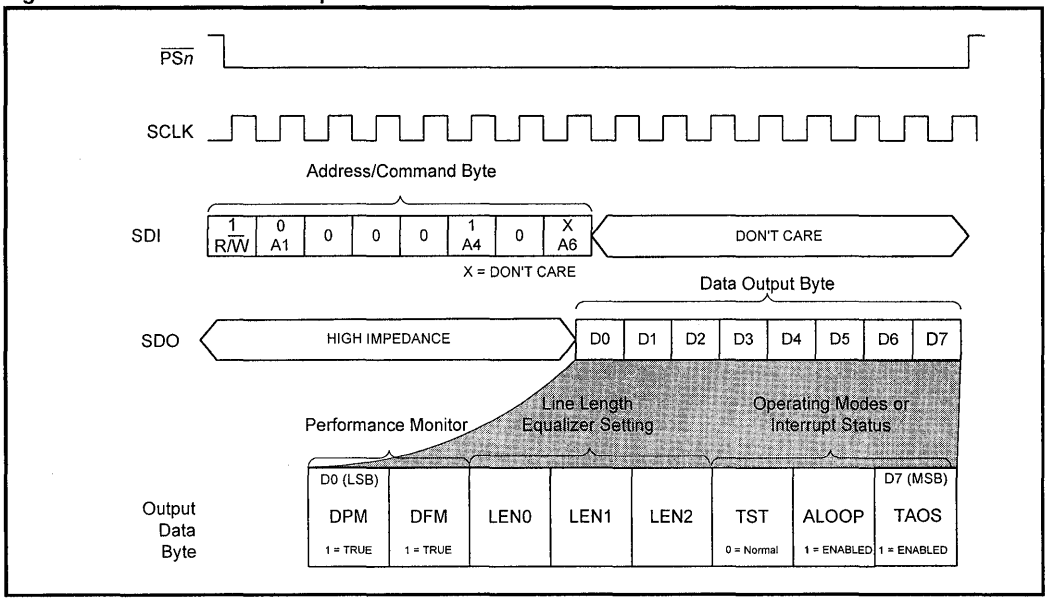
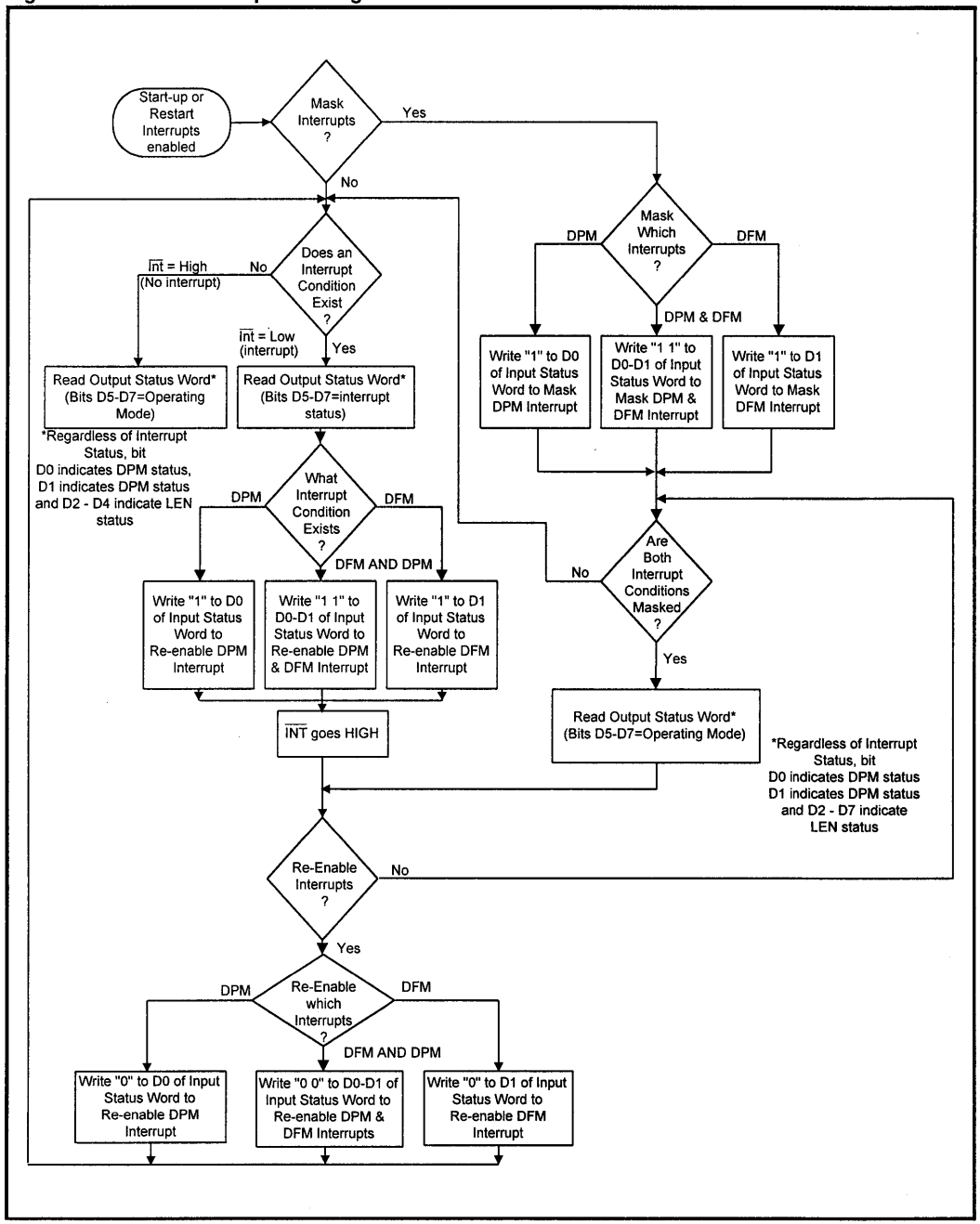


Table 6: LXT331 Serial Data Output Bit Coding

Bit D5	Bit D6	Bit D7	Operating Modes
0	0	0	Reset has occurred, or no program input (i.e, normal operation).
0	0	1	TAOS active
0	1	0	ALOOP active
0	1	1	TAOS and ALOOP active
Bit D5	**Bit D6**	**Bit D7**	**Interrupt Status**
1	0	1	DFM has changed state since the last Clear DFM occurred
1	1	0	DPM has changed state since the last Clear DPM occurred
1	1	1	DPM and DFM have changed state since the last Clear DPM and DMF occurred

Figure 6: LXT331 Interrupt Handling



Hardware Mode Control

Hardware control is the default operating mode; the LXT331 operates in Hardware mode unless pin 35 (LEN21/SPE) is clocked. In Hardware mode the transceiver is controlled through individual pins; a µP is not required. The SIO pins are re-mapped to provide control functions. In Hardware mode the PMRK/NMRK outputs are valid on the rising edge of RCLK.

Diagnostic Mode Operation

The LXT331 offers two diagnostic modes. Analog Loopback (ALOOP) and Transmit All Ones (TAOS) are available under both Host and Hardware control modes.

In Host mode, diagnostic modes are selected by writing the appropriate SIO bits. In Hardware mode, diagnostic modes are selected by a combination of pin settings. The pins must be held at the specified levels for a minimum of 20 ns (typically). Table 7 lists Hardware Mode control settings for the various diagnostic modes.

Transmit All Ones. See Figure 7. Transmit All Ones (TAOS) is selected when TAOS = 1. In TAOS mode the TPOS and TNEG inputs are ignored, but the transmitter remains locked to the TCLK input. When TAOS is selected, the transceiver transmits a continuous stream of 1s at the TCLK frequency. If TCLK is not supplied, MCLK is used as the transmit reference. TAOS and Analog Loopback can be selected simultaneously as shown in Figure 8.

Analog Loopback. See Figure 9. Analog Loopback (ALOOP) is selected when ALOOP = 1. In ALOOP mode the receive line input (RTIP/RRING) is blocked. The transmit outputs (TTIP and TRING) are looped back through the receiver input and output at PMRK and NMRK. The transmitter circuits are unaffected by ALOOP. Transmitting onto an improperly terminated line may produce unexpected pulse widths at PMRK and NMRK.

Tri-State. By holding pin 1 (TRSTE) High for at least 200 ns all output drivers (both digital and analog) go to high Z state and the chip logic goes into a reset condition which lasts 6 µs longer than in the tri-state. All pins go to a high-Z condition, and the internal circuits go to a known condition.

Table 7: Hardware Mode Diagnostic Settings

Mode	TRSTE	ALOOP	TAOS
ALOOP	L	H	L
TAOS	L	X	H
RESET	H	X	X

Initialization/Reset Operation

Upon initial power up, the transceiver is held static until the power supply reaches approximately 3 V. Upon crossing this threshold, the device clears all internal registers. TCLK is the transmit reference, and MCLK is the bias reference. The PLLs are continuously calibrated.

The transceiver can be reset from the Host or Hardware mode. In Host mode, reset is commanded by writing 1s to TST and ALOOP, and a 0 to TAOS (bits D5, D6 and D7, respectively, of the SIO input data byte). In either mode, command reset by holding TRSTE High for approximately 200 ns. All output signals are tri-stated at this time. The falling edge of the TRSTE initiates reset. Both modes reset each port independently. Reset clears and sets all SIO registers to 0 at the affected port. Reset is not generally required for the port to be operational.

Figure 7: TAOS Data Path

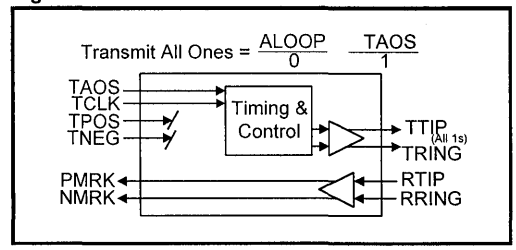


Figure 8: TAOS with ALOOP

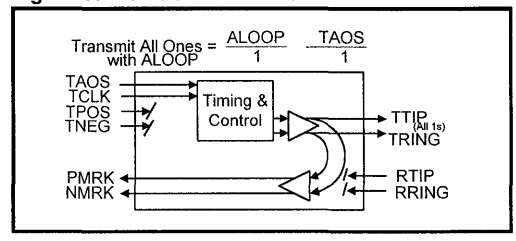
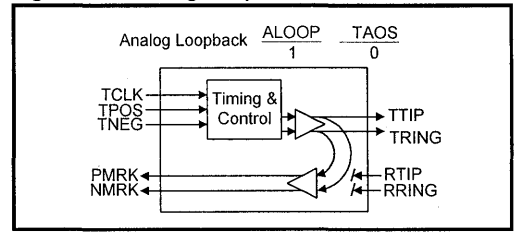


Figure 9: Analog Loopback



APPLICATION INFORMATION

Power Requirements

The LXT331 is a low-power CMOS device. It operates from a single +5 V power supply which can be tied to all three VCC inputs. However, all inputs must be within ± .3 V of each other, and decoupled to their respective grounds separately. Isolation between the transmit and receive circuits is provided internally. During normal operation or analog loopback, the transmitter powers down if TCLK is not supplied.

Line Interface Requirements

Table 8 lists transformer values for 1.544 Mbps and 2.048 Mbps applications. Table 9 shows combinations of transformers, series resistors and the LEN*xn* settings that produce a variety of return loss values.

Table 8: Recommended Transformer Values

Parameter	Value
Turns Ratio (T1)	1:2.3 (Tx) / 1: 1 (Rx)
Turns Ratio (E1)	1:2 (Tx) / 1: 1 (Rx)
Primary Inductance	1.2 mH minimum
Leakage Inductance	0.5 µH maximum
Interwinding Capacitance	25 pF maximum
DC Resistance (Primary)	1 Ω maximum
ET (Breakdown Voltage)	1 kV minimum

1.544 Mbps T1 Applications

Figure 11 on page 100 shows a typical host mode application. The eight serial interface pins are grouped at the top. Host mode is selected by the clock input to SPE. Other mode selection pins are shown at the bottom. With the TRSTE pin pulled Low, the LXT331 operates normally. Pulling this pin High causes all outputs to go to a high impedance state.

Figure 11 on page 100 shows a pair of framers. An LXP600A Clock Adapter (CLAD) converts the 2.048 MHz backplane clock to provide the 1.544 MHz input to the MCLK and TCLK inputs of both LIU ports.

The DFM indicator shown in the diagram lower left is available to drive optional external circuits. The driver power supply inputs (bottom) are tied to a common bus with 68 µF decoupling capacitors installed. The power supply for the remaining (non-driver) circuitry is shown at center right with 1.0 µF and 0.1 µF decoupling capacitors.

The line interface circuitry is identical for both LIU ports. The precision resistors in line with the transmit transformer provide optimal return loss. The recommended transformer/resistor combination is listed at the bottom of Figure 10. 1:1 transformers are used on the receive side.

Table 9: Transformer Combinations

LEN	Xfmr Ratio[1]	Rt Value[2]	Rtn Loss[3]
For T1/DSX-1 100 Ω Twisted-Pair Applications:			
011-111	1:2	Rt = 9.1 Ω	14dB
011-111	1:2.3	Rt = 9.1 Ω	18dB
011-011	1:1.15	Rt = 0 Ω	1dB
For E1 120 Ω Twisted-Pair Applications:			
001	1:2	Rt = 15 Ω	18dB
000	1:2	Rt = 9.1 Ω	10dB
For E1 75 Ω Coaxial Applications:			
001	1:2	Rt = 14.3 Ω	10dB
000	1:2	Rt = 9.1 Ω	18dB

2. Transformer turns ratio accuracy is ± 2%.
3. Rt values are ± 1%.
4. Typical return loss, 51kHz - 3.072 MHz band, with a capacitor in parallel with the primary side of the transformer.

2.048 Mbps E1 Applications

E1 Coaxial Applications

Figure 11 on page 100 shows the line interface for a typical 2.048 Mbps E1/CEPT coaxial (75 Ω) application. The LEN code should be set to 000 for coax. With 9.1 Ω Rt resistors in line with the 1:2 output transformers, the LXT331 produces 2.37 V peak pulses as required for coax applications. As in the T1 application shown in Figure 10, 1:1 transformers are used on the receive side.

Figure 10: Line Interface for E1 Coax

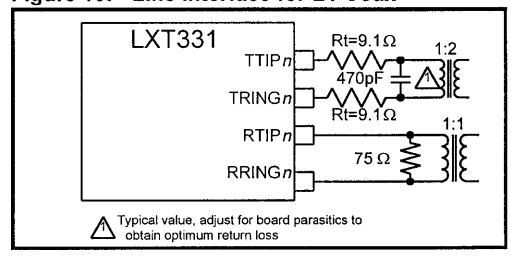
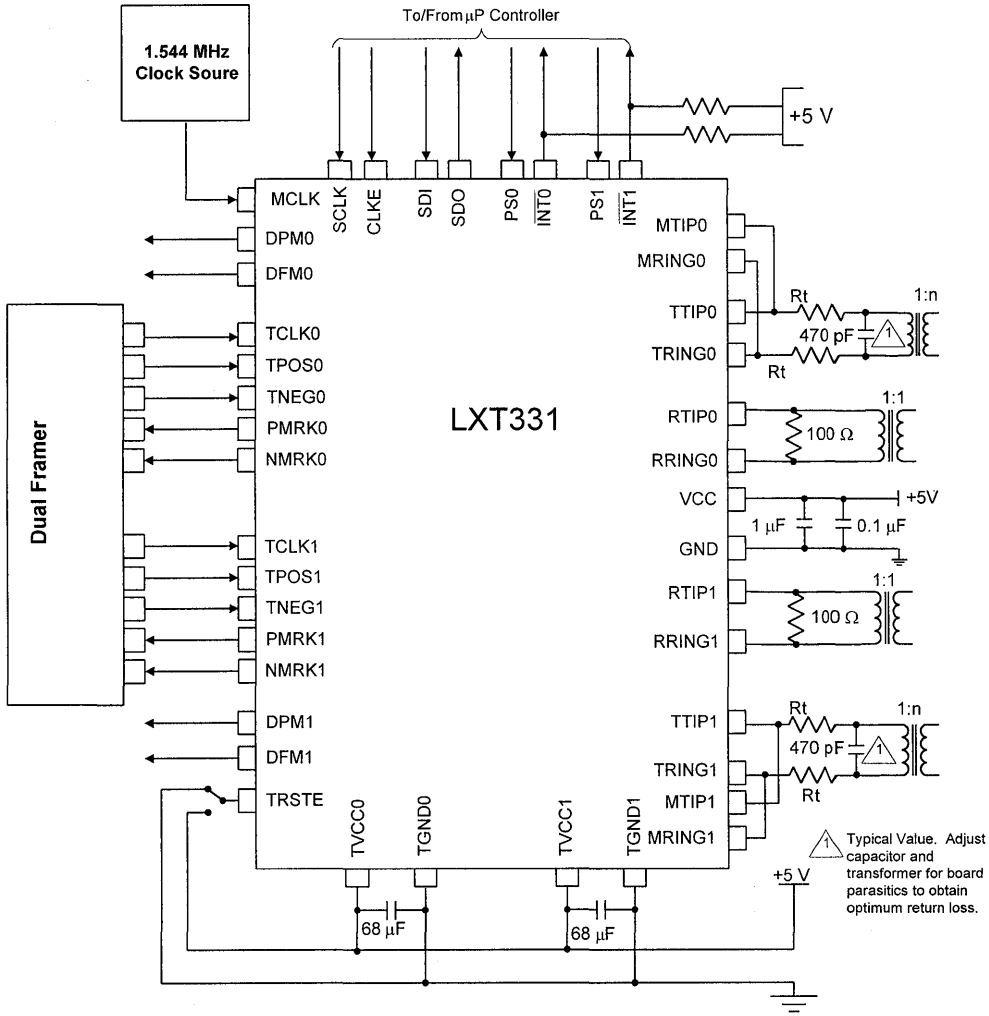


Figure 11: Typical LXT331 T1 Application (Host Control Mode, Bipolar I/O))



Media: 100 Ω Twisted Pair

LEN	Xfmr Ratio[1]	Rt Value[2]	Rtn Loss[3]
011-111	1:2.3	Rt = 9.1 Ω	18 dB

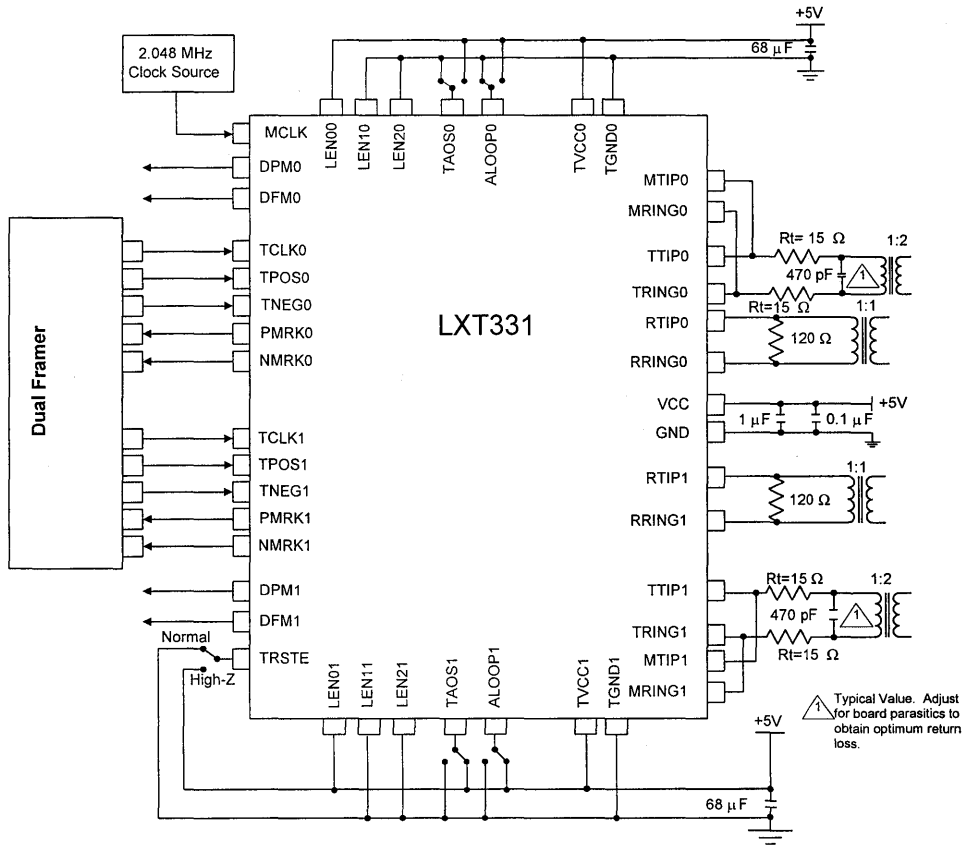
NOTES:

1. Transformer turns ratio accuracy is ± 2%.
2. Rt values are ± 1%.
3. Typical return loss, 51 kHz - 3.072 MHz band.

E1 Twisted-Pair Applications

Figure 12 shows a typical 2.048 Mbps E1 twisted-pair (120 Ω) application. The line length equalizers are controlled by the hardwired LEN inputs. With the LEN code set to 001 and 15 Ω Rt resistors in line with the 1:2 output transformers, the LXT331 produces the 3.0 V peak pulses required for this application.

Figure 12: Typical LXT331 E1 120 Ω Twisted Pair Application (Hardware Control Mode))



Media	LEN	Xfmr Ratio[1]	Rt[2]	Rr	Rtn Loss[3]
120 TWP	001	1:2	15 Ω	240 Ω	18 dB
75 Coax	000	1:2	9.1Ω	150 Ω	18 dB

NOTES:

1. Transformer turns ratio accuracy is ± 2%.
2. Rt values are ± 1%.
3. Typical return loss, 51 kHz - 3.072 MHz band.

TEST SPECIFICATIONS

Table 10: Absolute Maximum Ratings

Parameter	Sym	Min	Max	Units
DC supply (referenced to GND)	VCC, TVCC0, TVCC1	-0.3	6.0	V
Input voltage, any pin [1]	V_{IN}	GND - 0.3	Vcc + 0.3	V
Input current, any pin [2]	I_{IN}	-10	10	mA
Storage temperature	T_{ST}	-65	150	°C

CAUTION

Operations at or beyond these limits may result in permanent damage to the device. Normal operation not guaranteed or implied at these extremes.

1. Excluding RTIP and RRING which must stay within - 6 V to VCC + 0.3 V.
2. Transient currents of up to 100 mA will not cause SCR latch-up. TTIP0 & 1, TRING0 & 1, VCC, TVCC0 & 1 and TGND0 & 1 can withstand continuous current of 100 mA.

Table 11: Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical[1]	Maximum	Units
DC supply [2]	VCC, TVCC0, TVCC1	4.75	5.0	5.25	V
Ambient operating temperature [3]	T_A	-40	25	85	°C
Ambient operating temperature [4]	T_A	-5	25	85	°C

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Variation between TVCC0, TVCC1 and VCC must be - 0.3 V.
3. LXT331PE & QE
4. LXT331PH & QH

Table 12: Electrical Characteristics (Over Recommended Operating Range)

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Total power dissipation - T1 [2] (Maximum line length, 75 Ω load)	PP	-	-	680	mW	-40 to +85 °C
	PD	-	-	650	mW	0 to +85 °C
Total power dissipation - T1 [3] (Maximum line length, 43 Ω load)	PP	-	-	1000	mW	-40 to +85 °C
	PD	-	-	980	mW	0 to +85 °C
Total power dissipation - E1 [2]	PD	-	-	520	mW	100% ones density
High level input voltage [4,5]	VIH	2.0	-	-	V	
Low level input voltage [4,5]	VIL	-	-	0.8	V	
High level output voltage [4,5]	VOH	2.4	-	-	V	IOUT = - 400 µA
Low level output voltage [4,5]	VOL	-	-	0.4	V	IOUT = 1.6 mA
Input leakage current [6]	ILLD	0	-	± 10	µA	
Input leakage current [7]	ILLM	0	-	± 50	µA	
Three-state leakage current [4]	ISL	-	-	± 10	µA	
TTIP/TRING leakage current	ITR	-	-	1.2	mA	in power down and tri-state

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. 100% 1s density and maximum line length. Driving 75 Ω load over operating temperature range. Includes device and load. Digital input levels are within 10% of the supply rails and digital outputs are driving a 50 pF capacitive load.
3. 100% 1s density and maximum line length. Driving 43 Ω load (corresponding to an Rt value of 9.1 Ω and a 1:2 transformer ratio) over operating range. include device and load. Digital input levels are within 10% of the supply rails and digital outputs are driving a 50 pF capacitive load.
4. Functionality of pins depends on mode.
5. Output drivers will output CMOS logic levels into CMOS loads.
6. All digital input pins.
7. For MTIP0, MRING0, MTIP1 AND MRING1.

Table 13: Analog Specifications (Over Recommended Operating Range)

Parameter		Min	Typ[1]	Max	Units	Test Conditions
AMI output pulse amplitudes	DSX-1	2.4	3.0	3.6	V	measured at the DSX
	E1 (120 Ω)	2.7	3.0	3.3	V	measured at line side
	E1 (75 Ω)	2.13	2.37	2.61	V	measured at line side
Transmit amplitude variation with supply [3]		-	1	2.5	%	
Recommended output load at TTIP and TRING		-	75	-	Ω	
Driver output impedance [3]		-	3	10	Ω	@ 772 kHz
Jitter added by the transmitter [2]	10 Hz - 8kHz [3]	-	0.005	0.01	UI	T1 Jitter Bands
	8 kHz - 40 kHz [3]	-	0.015	0.025	UI	
	10 Hz - 40 Hz [3]	-	0.02	0.025	UI	
	Broad band	-	0.03	0.05	UI	

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Input signal at TCLK is jitter-free.
3. Not production tested, but guaranteed by design and other correlation methods.

Table 13: Analog Specifications (Over Recommended Operating Range) – continued

Parameter		Min	Typ[1]	Max	Units	Test Conditions
Jitter added by the transmitter [2]	20 Hz - 100 kHz	-	-	0.05	UI	E1 Jitter Band
Output power levels [3] DSI 2 kHz BW	@ 772 kHz	12.6	-	17.9	dBm	
	@ 1544 kHz	-29	-	-	dB	
Positive-to-negative pulse imbalance		-	-	0.5	dB	
Differential		-	40	-	kΩ	
Sensitivity below DSX (0 dB = 2.4 V) (max 6 dB cable attenuation)		13.6	-	-	dB	
		500	-	-	mV	
Peak detector sqelch level		-	226	-	mV	
Data decision threshold	DSX-1	63	70	77	% peak	
	E1	43	50	57	% peak	

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Input signal at TCLK is jitter-free.
3. Not production tested, but guaranteed by design and other correlation methods.

Table 14: LXT331 Master Clock and Transmit Timing Characteristics (See Figure 13)

Parameter		Sym	Min	Typ[1]	Max	Units
Master clock frequency	DSX-1	MCLK	-	1.544	-	MHz
	E1	MCLK	-	2.048	-	MHz
Master clock tolerance		MCLKt	-	± 50	-	ppm
Master clock duty cycle		MCLKd	40	-	60	%
Transmit clock frequency	DSX-1	TCLK	-	1.544	-	MHz
	E1	TCLK	-	2.048	-	MHz
Transmit clock tolerance		TCLKt	-	± 50	-	ppm
Transmit clock duty cycle		TCLKd	10	-	90	%
TPOS/TNEG to TCLK setup time		tSUT	25	-	-	ns
TCLK to TPOS/TNEG Hold time		tHT	25	-	-	ns

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 13: LXT331 Transmit Clock Timing

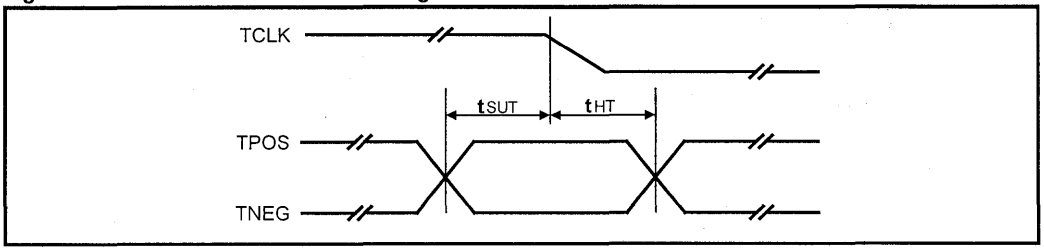


Table 15: LXT331 Receive Characteristics (See Figure 14)

Parameter		Sym	Min	Typ[1]	Max	Units	Test Conditions
PMRK/NMRK pulse width	T1	tMPW	-	324	-	ns	
	E1	tMPW	-	244	-	ns	
Receiver throughput delay		tRXD	-	65	-	ns	3.0 V pulse

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 16: LXT331 Serial I/O Timing Characteristics (See Figures 15 and 16)

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Rise/Fall time - any digital output	tRF	-	-	100	ns	Load 1.6 mA, 50pF
SDI to SCLK setup time	tDC	50	-	-	ns	
SCLK to SDI hold time	tCDH	50	-	-	ns	
SCLK low time	tCL	240	-	-	ns	
SCLK high time	tCH	240	-	-	ns	
SCLK rise and fall time	tR, tF	-	-	50	ns	
PS to SCLK setup time	tPC	50	-	-	ns	
SCLK to PS hold time	tCPH	50	-	-	ns	
PS inactive time	tPWH	250	-	-	ns	
SCLK to SDO valid	tCDV	-	-	200	ns	
16th SCLK falling edge or PS rising edge to SDO high Z	tCDZ	-	100	-	ns	

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 14: LXT331 Receive Timing

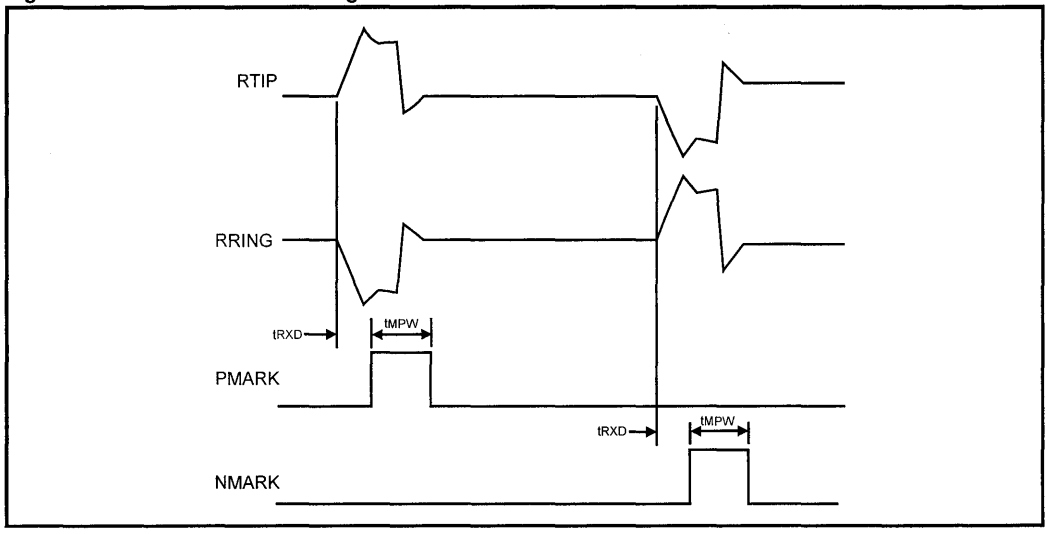


Figure 15: LXT331 Serial Input Timing Diagram

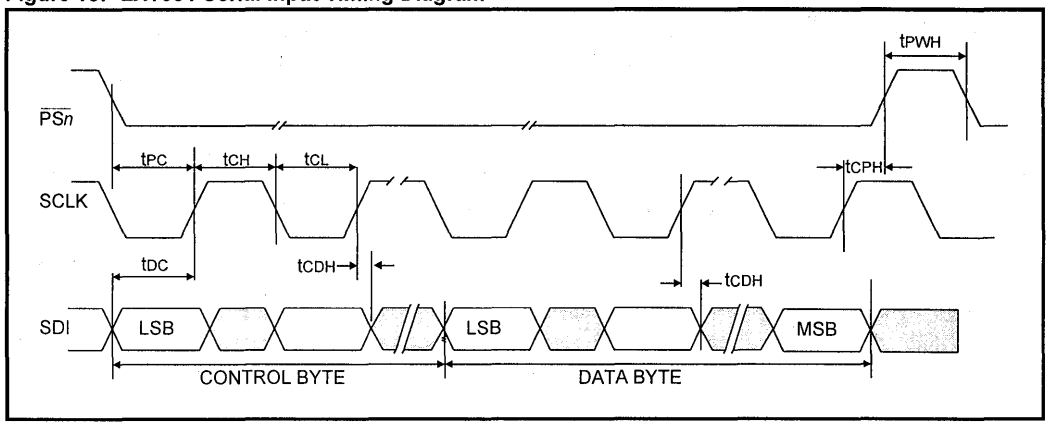
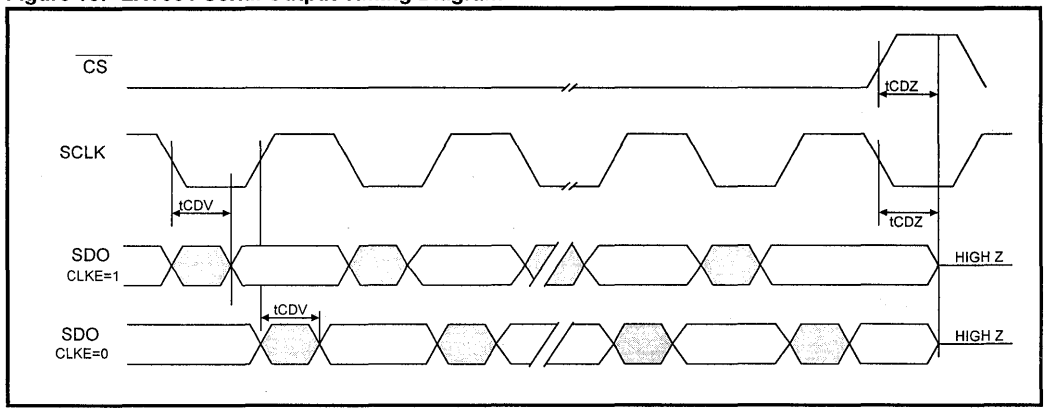


Figure 16: LXT331 Serial Output Timing Diagram



LXT332

Dual T1/E1 Line Interface Unit with Crystal-less Jitter Attenuation

General Description

The LXT332 is a fully integrated Dual Line Interface Unit (DLIU) for both 1.544 Mbps (T1) and 2.048 Mbps (E1) applications. It features B8ZS/HDB3 encoders and decoders, and a constant low output impedance transmitter for high return loss. Transmit pulse shape is selectable for various line lengths and cable types.

The LXT332 incorporates an advanced crystal-less digital jitter attenuator, switchable to either the transmit or receive side. This eliminates the need for an external quartz crystal. It offers both a serial interface (SIO) for microprocessor control and a hardware control mode for stand-alone operation.

The LXT332 offers a variety of advanced diagnostic and performance monitoring features. It uses an advanced double-poly, double-metal CMOS process and requires only a single 5-volt power supply.

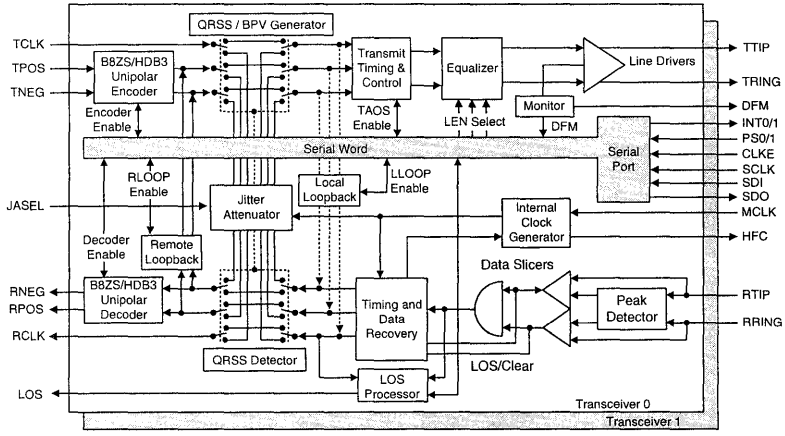
Applications

- PCM / Voice Channel Banks
- Data Channel Bank / Concentrator
- T1 / E1 multiplexer
- Digital Access and Cross-connect Systems (DACS)
- Computer to PBX interface (CPI & DMI)
- SONET/SDH Multiplexers
- Interfacing Customer Premises Equipment to a CSU
- Digital Loop Carrier (DLC) terminals

Features

- Digital (crystal-less) jitter attenuation, selectable for receive or transmit path, or may be disabled
- High transmit and receive return loss
- Constant low output impedance transmitter with programmable equalizer shapes pulses to meet DSX-1 pulse template from 0 to 655 ft
- Meets or exceeds industry specifications including ITU G.703, ANSI T1.403 and AT&T Pub 62411
- Compatible with most industry standard framers
- Complete line driver, data recovery and clock recovery functions
- Minimum receive signal of 500 mV, with selectable slicer levels (E1/DSX-1) to improve SNR
- Local, remote, and dual loopback functions
- Built-In Self Test with QRSS Pattern Generator
- Transmit / Receive performance monitors with Driver Fail Monitor (DFM) and Loss of Signal (LOS) outputs
- Receiver jitter tolerance 0.4 UI from 40 kHz to 100 kHz
- Available in 44-pin PLCC and 44-pin QFP

LXT332 Block Diagram



OVERVIEW

In addtion to the inherent advantages of a DLIU, the LXT332 also provides several advanced features which are not available in other LXT30x-series devices. All of the added features are easily implemented. Many require only a clock pulse to change from one mode to another. Some features are available in Host Mode only.

- Two complete LIUs in a single PLCC or QFP package
- Simplifies board design, saves real estate
- Proven architecture (LXT3xx series)
- Crystal-less Jitter Attenuation
- New Features

Standard LXT332 Features

- **Tri-state Outputs**
  - All LXT332 output pins can be forced to a high-Z Tri-state mode. The Tri-state mode is enabled or disabled by the TRSTE pin.
- **Bipolar or Unipolar Data I/O**
  - The LXT332 / Framer interface can be either bipolar (default) or unipolar (selectable). The unipolar mode is selected by applying MCLK to the TRSTE pin.
- **B8ZS or HDB3 Zero Suppression**
  - The LXT332 incorporates zero suppression encoders and decoders for use in the unipolar data I/O mode. The encoders/decoders can be activated or deactivated by changing the logic level on the remapped TNEG pin.
- **Selectable Jitter Attenuation**
  - Jitter attenuation can be placed in either the transmit or receive path or deactivated. The Jitter Attenuation Select (JASEL) pin determines the jitter attenuation mode. No crystal required.
- **Dual Loopback**
  - This option enables simultaneous loopbacks to both the framer and the line. The TCLK, TPOS and TNEG framer inputs are routed through the jitter attenuator and looped back to the RCLK, RPOS and RNEG outputs. The RTIP/RRING line inputs are looped back through the timing recovery block and line driver onto the TTIP/TRING outputs.

Additional Host-Mode Features

- **High Frequency Clocks**
  - The LXT332 provides a pair of high frequency clock outputs, one for each LIU. These 8x clocks (12.352 MHz for T1, 16.384 MHz for E1) are tied to the de-jittered clock from the JA of the respective LIU.
- **Bipolar Violation Insertion**
  - The same pins which provide the High Frequency Clocks can also be used to insert bipolar violations into the outgoing data stream. Violations can be inserted into each LIU channel independently.
- **Built-In Self Test (QRSS)**
  - The LXT332 can generate and transmit a QRSS pattern to Built-In Self Test (BIST) applications. Logic errors and bipolar violations can be inserted into the QRSS output. The LXT332 also detects QRSS pattern synchronization and reports bit errors in the received QRSS pattern data stream.
- **AIS Detection**
  - The LXT332 detects the AIS alarm signal on the receive side independent of the loopback modes. When AIS is detected (less than 3 zeros in 2048 bits), the LXT332 provides an indicator output.

PIN ASSIGNMENTS AND SIGNAL DESCRIPTIONS

Figures 1 and 2 show the pinout diagrams for the PLCC and QFP packages, respectively. Table 1 describes the Host Mode signal functions, except signals that change when in Unipolar Host Mode. Table 2 describes signal functions that change when in Unipolar Most Mode. Table 3 describes all Hardware Mode signal functions, except signals that change when in Unipolar Mode. Table 4 describes signal functions that change when in Unipolar Hardware Mode.

Figure 1: LXT332 Pin Assignments (PLCC Package)

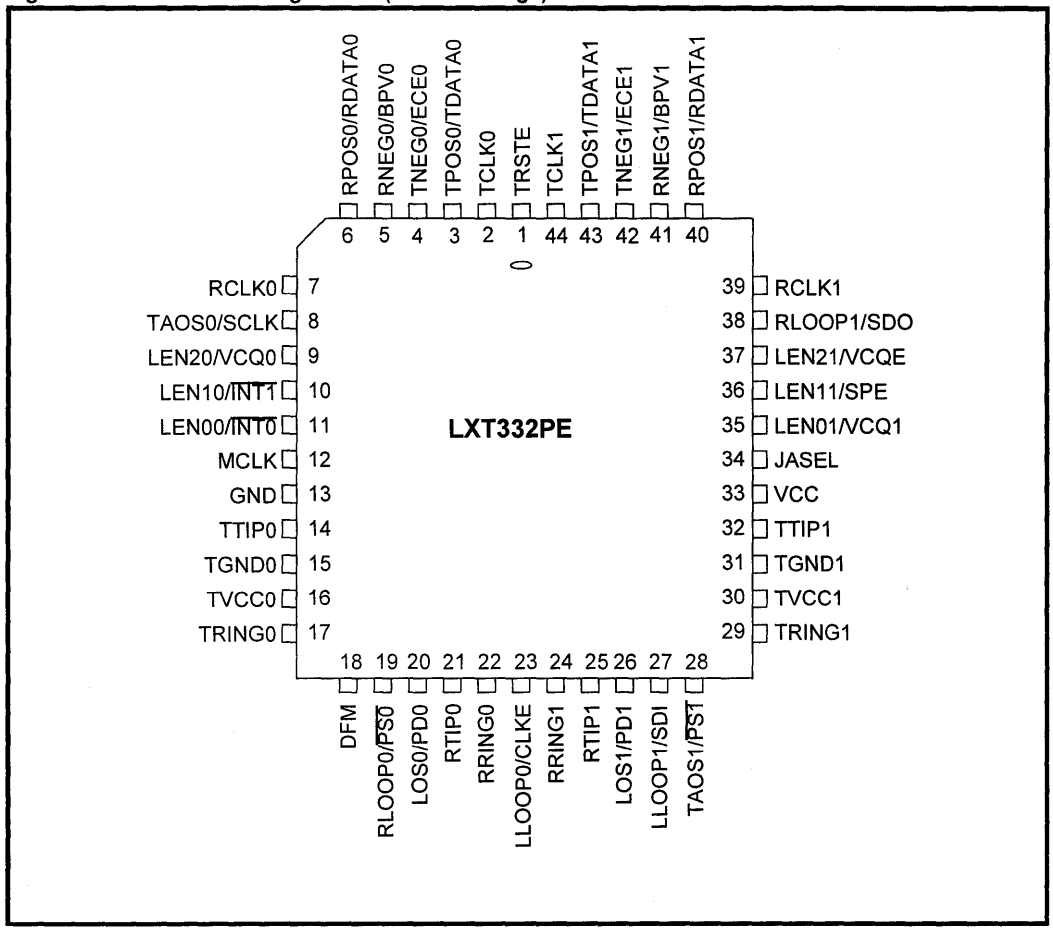


Figure 2: LXT332 Pin Assignments (QFP Package)

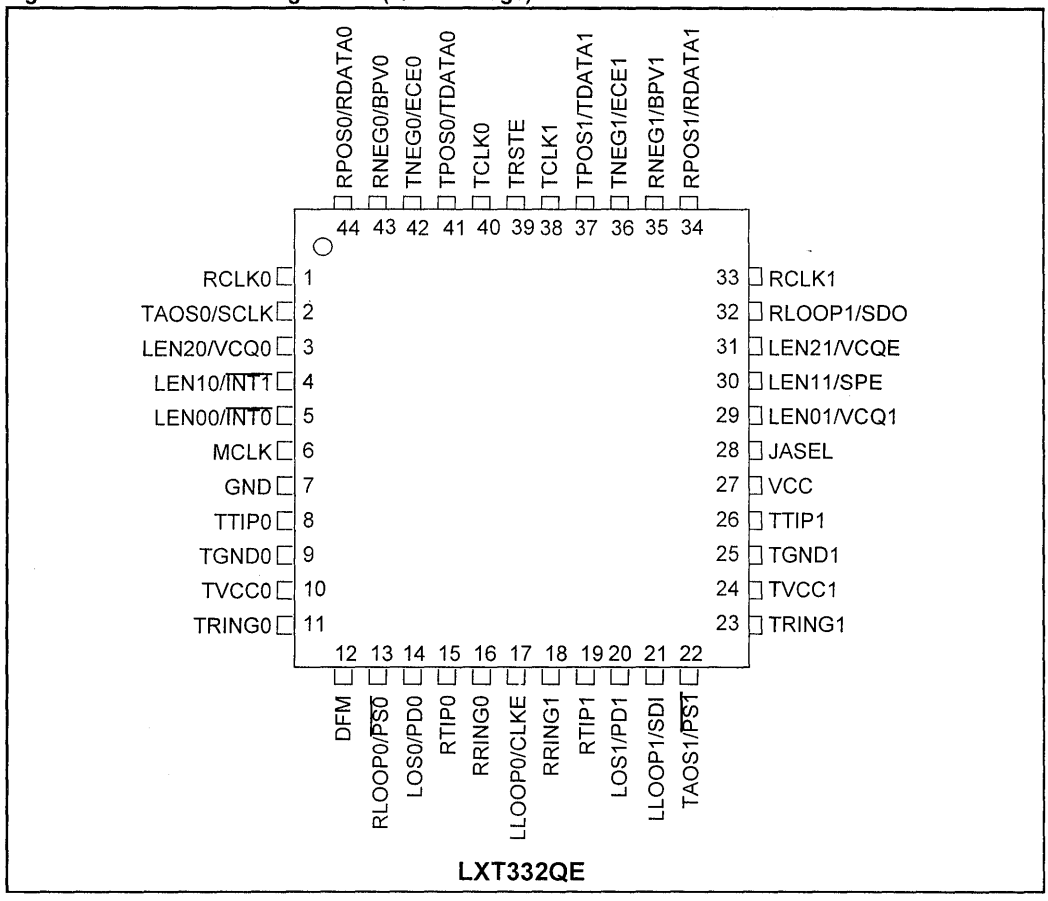


Table 1: Host Mode Pin and Bipolar Host Mode Pin Descriptions

Pin QFP	Pin PLCC	Symbol	I/O[1]	Description
39	1	TRSTE	DI	**Tristate Output Enable Input Pin.** Forces all output pins to high-Z tri-state when held High. Enables Bipolar I/O mode when held Low. In this mode the framer interface is bipolar (TPOS/TNEG and RPOS/RNEG), and the B8ZS/HDB3 encoders are disabled. Enables Unipolar I/O mode when clocked by MCLK. In this mode the framer interface is unipolar (TDATA and RDATA), and the TNEG and RNEG pins are re-mapped. The TNEG pins are re-mapped as Encoder Enable (ECE) to individually enable the B8ZS/HDB3 encoder/decoder for each port. The RNEG pins are re-mapped as Bipolar Violation (BPV) indicators to report BPVs received at the respective ports.
40	2	TCLK0	DI	**Transmit Clock - Port 0.** 1.544 MHz for T1, 2.048 MHz for E1. The transmit data inputs are sampled on the falling edge of TCLK.

1 DI = Digital Input; DO = Digital Output; DI/O = Digital Input/Output; AI = Analog Input; AO = Analog Output

Table 1: Host Mode Pin and Bipolar Host Mode Pin Descriptions – continued

Pin QFP	Pin PLCC	Symbol	I/O[1]	Description
41	3	TPOS0 (Bipolar)	DI	**Transmit Positive and Negative Data - Port 0.** In the Bipolar I/O mode, these pins are the positive and negative sides of a bipolar input pair for port 0. Data to be transmitted onto the twisted-pair line is input at these pins. However, when the TRSTE pin is clocked by MCLK, the LXT332 switches to a unipolar mode. Table 2 describes Unipolar mode pin functions.
42	4	TNEG0 (Bipolar)	DI	
43	5	RNEG0 (Bipolar)	DO	**Receive Positive and Negative Data - Port 0.** In the Bipolar I/O mode, these pins are the data outputs from port 0. A signal on RNEG corresponds to receipt of a negative pulse on RTIP/RRING. A signal on RPOS corresponds to receipt of a positive pulse on RTIP/RRING. RNEG/RPOS outputs are Non-Return-to-Zero (NRZ). In Host mode, CLKE determines the clock edge at which these outputs are stable and valid.
44	6	RPOS0 (Bipolar)	DO	
1	7	RCLK0	DO	**Receive Clock - Port 0.** This clock is recovered from the input signal. Under Loss of Signal (LOS) conditions, this output is derived from MCLK.
2	8	SCLK	DI	**Serial Clock.** The Serial Clock shifts data into or out from the serial interface register of the selected port.
3	9	VCQ0	DI/O	Provides Violation insert, High Frequency Clock, or QRSS generation/detection functions for Port 0. Pin operation is determined by the VCQE pin. **Violation Insertion Function.** When the Violation insertion function is enabled, this pin is sampled on the falling edge of TCLK to control bipolar violation (BPV) insertion. If High, a BPV is inserted at the next available mark transmitted from port 0. A Low-to-High transition is required for each subsequent violation insertion. (B8ZS and HDB3 zero suppression codes are not violated.) **Clock Function.** When the Clock function is enabled, this pin outputs a High Frequency Clock (12.352 MHz for T1, 16.384 MHz for E1) tied to the jitter attenuated clock of port 0. If no JA clock is available, HFC is locked to the 8x receive timing recovery clock. **Quasi Random Signal Source (QRSS) Function.** When the QRSS function is enabled, a High on this pin enables the QRSS detection circuit and causes the LXT332 to transmit the QRSS pattern onto the twisted-pair line from port 0. For error-free QRSS transmission, TPOS0 must be held Low. To insert errors into the pattern, TPOS must transition from Low to High (TPOS is sampled on the falling edge of MCLK). A Low-to-High transition is required for each subsequent violation insertion. (B8ZS and HDB3 zero suppression codes are not violated.)
4	10	$\overline{\text{INT1}}$	DO	**Interrupt Outputs.** The interrupt outputs go Low to flag the host processor that the respective port has changed state. INT0 and INT1 are open drain outputs. Each must be tied to VCC through a resistor.
5	11	$\overline{\text{INT0}}$	DO	
6	12	MCLK	DI	**Master Clock.** The master clock (1.544 MHz for T1, 2.048 MHz for E1) input must be independent, free-running, continuously active and jitter free for receiver operation. Since the transceivers derive their RCLK timing from the MCLK input on Loss of Signal (LOS), MCLK cannot be derived from RCLK.
7	13	GND	–	**Ground.** Ground return for power supply VCC.

1 DI = Digital Input; DO = Digital Output; DI/O = Digital Input/Output; AI = Analog Input; AO = Analog Output

Table 1: Host Mode Pin and Bipolar Host Mode Pin Descriptions – continued

Pin QFP	Pin PLCC	Symbol	I/O[1]	Description
8 11	14 17	TTIP0 TRING0	AO AO	**Transmit Tip and Ring - Port 0.** The tip and ring pins for each port are differential driver outputs designed to drive a 35 - 200 Ω load. Line matching resistors and transformers can be selected to give the desired pulse height. See Figures 19 through 21.
9	15	TGND0	–	**Ground.** Ground return for power supply TVCC0.
10	16	TVCC0	I	**+ 5 volt power supply input for the port 0 transmit driver.** TVCC0 must not vary from TVCC1 or VCC by more than ± 0.3 V.
12	18	DFM	O	**Driver Fail Monitor.** This signal goes High to indicate a driver output short in one or both ports.
13	19	$\overline{PS0}$	I	**Port Select - Port 0.** This input accesses the serial interface registers for port 0. For each read or write operation, PS must transition from High to Low, and remain Low.
14	20	PD0	DO	**Pattern Detect - Port 0.** Unless the QRSS function is selected by the VCQE pin, PD0 functions as an AIS alarm indicator. The AIS pattern is detected by the receiver, independent of any loopback mode. AIS goes High when less than three zeros have been detected in any string of 2048 bits. AIS returns Low when the received signal contains more than three zeros in 2048 bits. (LOS is available via the SIO register and interrupt.) If the QRSS function is enabled by the VCQE pin, PD0 remains High until pattern sync is reached with the received signal. Once pattern lock is obtained, PD0 goes Low. (The sync/out-of-sync criteria is less than 3/4 errors in 128 bits.) After sync acquisition, bit errors cause PD0 to go High for half a clock cycle. This output can be used to trigger an external error counter.
15 16	21 22	RTIP0 RRING0	DI DI	**Receive Tip and Ring - Port 0.** RTIP and RRING comprise the receive line interface. This input pair should be connected to the line through a center-tapped 1:2 transformer.
17	23	CLKE	DI	**Clock Edge Select.** When CLKE is High, RPOS/RNEG or RDATA outputs are valid on the falling edge of RCLK, and SDO is valid on the rising edge of SCLK. When CLKE is Low, RPOS/RNEG or RDATA outputs are valid on the rising edge of RCLK, and SDO is valid on the falling edge of SCLK.
18 19	24 25	RRING1 RTIP1	AI AI	**Receive Tip and Ring - Port 1.** RTIP and RRING comprise the receive line interface. This input pair should be connected to the line through a center-tapped 1:2 transformer.
20	26	PD1	DO	**Pattern Detect - Port 1.** Reports AIS and QRSS pattern reception. See PD0 signal description for details.
21	27	SDI	DI	**Serial Data Input.** SDI is sampled on the rising edge of SCLK.
22	28	$\overline{PS1}$	DI	**Port Select - Port 1.** This input accesses the serial interface registers for port 1. For each read or write operation, PS must transition from High to Low, and remain Low.
23 26	29 32	TRING1 TTIP1	AO AO	**Transmit Tip and Ring - Port 1.** The tip and ring pins for each port are differential driver outputs designed to drive a 35 - 200 Ω load. Line matching resistors and transformers can be selected to give the desired pulse height. See Figures 13 through 15.

1 DI = Digital Input; DO = Digital Output; DI/O = Digital Input/Output; AI = Analog Input; AO = Analog Output

Table 1: Host Mode Pin and Bipolar Host Mode Pin Descriptions – continued

Pin QFP	Pin PLCC	Symbol	I/O[1]	Description
24	30	TVCC1	AI	**+ 5 volt power supply input for the port 1 transmit driver.** TVCC1 must not vary from TVCC0 or VCC by more than ± 0.3 V.
25	31	TGND1	–	**Ground.** Ground return for power supply TVCC1.
27	33	VCC	AI	**+5 VDC power supply** input for all circuits, except the transmit drivers.
28	34	JASEL	DI	**Jitter Attenuation Select.** Selects jitter attenuation for both ports. When JASEL = 1, JA circuits are placed in the receive paths. When JASEL = 0, JA circuits are placed in the transmit paths. When JASEL is clocked with MCLK, the JA circuit is disabled.
29	35	VCQ1	DI/O	**Violation insert, Clock, or QRSS.** Function (Violation insert, Clock, or QRSS) is determined by the VCQE pin. Provides Violation Insertion, High Frequency Clock or QRSS Generation functions for Port 1. Refer to VCQ0 signal description for details.
30	36	SPE	DI	**Serial Port Enable.** SPE must be clocked with MCLK to enable Host Mode control through the serial port.
31	37	VCQE	DI	**Violation - Clock - QRSS Enable.** When set High, enables the Bipolar Violation Insert functions of VCQ0 and VCQ1 pins. When set Low, enables the High Frequency Clock functions of VCQ0 and VCQ1. When clocked with MCLK, enables the QRSS functions of VCQ0 and VCQ1, and enables the QRSS Generate and Detect function of PD0 and PD1 pins.
32	38	SDO	DO	**Serial Data Output.** If CLKE is High, SDO is valid on the rising edge of SCLK. If CLKE is Low, SDO is valid on the falling edge of SCLK.
33	39	RCLK1	DO	**Receive Clock - Port 1.** This clock is recovered from the input signal. Under Loss of Signal (LOS) conditions, this output is derived from MCLK.
34 35	40 41	RPOS1 (Bipolar) RNEG1 (Bipolar)	DO DO	**Receive Positive and Negative Data - Port 1.** In the Bipolar I/O mode, these pins are the data outputs from port 1. A signal on RPOS corresponds to receipt of a positive pulse on RTIP/RRING. A signal on RNEG corresponds to receipt of a negative pulse on RTIP/RRING. RNEG/RPOS outputs are Non-Return-to-Zero (NRZ). CLKE determines the clock edge at which these outputs are stable and valid.
36 37	42 43	TNEG1 (Bipolar) TPOS1 (Bipolar)	DI DI	**Transmit Positive and Negative Data - Port 1.** In the Bipolar I/O mode, these pins are TPOS and TNEG, the positive and negative sides of a bipolar input pair for port 1. Data to be transmitted onto the twisted-pair line is input at these pins. However, when TRSTE is clocked by MCLK, the LXT332 switches to a unipolar mode. Unipolar mode pin functions are described separately.
38	44	TCLK1	DI	**Transmit Clock - Port 1.** 1.544 MHz for T1, 2.048 MHz for E1. The transmit data inputs are sampled on the falling edge of TCLK.

1 DI = Digital Input; DO = Digital Output; DI/O = Digital Input/Output; AI = Analog Input; AO = Analog Output

Table 2: Unipolar Host Mode Pin Descriptions[1]

Pin QFP	Pin PLCC	Symbol	I/O	Description
41	3	TDATA0	DI	**Transmit Data - Port 0.** In the Unipolar mode, the data to be transmitted onto the twisted-pair line from port 0 is input at this pin.

1 Table 1 describes the pins that do not change function in Unipolar Host Mode and functions of pins unique to Bipolar Mode.

Table 2: Unipolar Host Mode Pin Descriptions[1] – continued

Pin QFP	Pin PLCC	Symbol	I/O	Description
42	4	ECE0	DI	**Encoder Enable - Port 0.** In the Unipolar mode, a High on this pin enables the B8ZS or HDB3 encoder and decoder for port 0.
43	5	BPV0	DO	**Bipolar Violation - Port 0.** In the Unipolar mode this indicator output goes High when a bipolar violation is received at port 0.
44	6	RDATA0	DO	**Receive Data - Port 0.** In the Unipolar mode, RDATA is a Non-Return-to-Zero (NRZ) output. CLKE determines the RCLK edge which RDATA is stable and valid.
34	40	RDATA1	DO	**Receive Data - Port 1.** In the Unipolar mode, RDATA is a Non-Return-to-Zero (NRZ) output. CLKE determines the RCLK edge which RDATA is stable and valid.
35	41	BPV1	DO	**Bipolar Violation - Port 1.** In the Unipolar mode this indicator output goes High when a bipolar violation is received at port 1.
36	42	ECE1	DI	**Encoder Enable - Port 1.** In the Unipolar mode, a High on this pin enables the B8ZS or HDB3 encoder and decoder for port 1.
37	43	TDATA1	DI	**Transmit Data - Port 1.** In the Unipolar mode, the data to be transmitted onto the twisted-pair line from port 1 is input at this pin.

1 Table 1 describes the pins that do not change function in Unipolar Host Mode and functions of pins unique to Bipolar Mode.

Table 3: Hardware Mode Pin and Bipolar Hardware Mode Pin Descriptions[1]

Pin QFP	Pin PLCC	Symbol	I/O[2]	Description
39	1	TRSTE	DI	**Tristate Output Enable Input Pin.** Forces all output pins to high-Z Tri-state when held High. Enables Bipolar I/O mode when held Low. In this mode the framer interface is bipolar (TPOS/TNEG and RPOS/RNEG), and the B8ZS/HDB3 encoders are disabled. Enables Unipolar I/O mode when clocked by MCLK. In this mode the framer interface is unipolar (TDATA and RDATA), and the TNEG and RNEG pins are re-mapped. The TNEG pins are re-mapped as Encoder Enable (ECE) to individually enable the B8ZS/HDB3 encoder/decoder for each port. The RNEG pins are re-mapped as Bipolar Violation (BPV) indicators to report BPVs received at the respective ports.
40	2	TCLK0	DI	**Transmit Clock - Port 0.** 1.544 MHz for T1, 2.048 MHz for E1. The transmit data inputs are sampled on the falling edge of TCLK.
41 42	3 4	TPOS0 (Bipolar) TNEG0 (Bipolar)	DI	**Transmit Data Positive and Negative - Port 0.** In the Bipolar I/O mode, these pins are the positive and negative sides of a bipolar input pair for port 0. Data to be transmitted onto the twp line is input at these pins. However, when TRSTE is clocked by MCLK, the LXT332 switches to a unipolar mode. Unipolar mode pin functions are described separately.
43 44	5 6	RNEG0 (Bipolar) RPOS0 (Bipolar)	DO	**Receive Data Positive and Negative - Port 0.** In the Bipolar I/O mode, a signal on RNEG corresponds to receipt of a negative pulse on RTIP/RRING. A signal on RPOS corresponds to receipt of a positive pulse on RTIP/RRING. RNEG/RPOS outputs are Non-Return-to-Zero (NRZ). RPOS and RNEG are stable and valid on the rising edge of RCLK.

1 Table 4 describes the pins used in Unipolar Hardware Mode.
2. DI = Digital Input; DO = Digital Output; DI/O = Digital Input/Output; AI = Analog Input; AO = Analog Output

Table 3: Hardware Mode Pin and Bipolar Hardware Mode Pin Descriptions[1] – continued

Pin QFP	Pin PLCC	Symbol	I/O[2]	Description
1	7	RCLK0	DO	**Receive Clock - Port 0.** This clock is recovered from the input signal. Under Loss of Signal (LOS) conditions, this output is derived from MCLK.
2	8	TAOS0	DI	**Transmit All Ones Enable - Port 0.** When TAOS is High and RLOOP is Low, the TPOS/TNEG or TDATA input is ignored and port 0 transmits a stream of ones at the TCLK frequency. If TCLK is not provided, the MCLK input is used as the transmit reference.
3 4 5	9 10 11	LEN20 LEN10 LEN00	DI DI DI	**Line Length Equalizer Inputs - Port 0.** This pins determine the shape and amplitude of the transmit pulse.
6	12	MCLK	DI	**Master Clock.** The master clock (1.544 MHz for T1, 2.048 MHz for E1) input must be independent, free-running, continuously active and jitter free for receiver operation. Since the transceivers derive their RCLK timing from the MCLK input on Loss of Signal (LOS), MCLK cannot be derived from RCLK.
7	13	GND	–	**Ground.** Ground return for power supply VCC.
8 11	14 17	TTIP0 TRING0	AO AO	**Transmit Tip and Ring - Port 0.** The tip and ring pins for each port are differential driver outputs designed to drive a 35 - 200 Ω load. Line matching resistors and transformers can be selected to give the desired pulse height. See Figures 13 through 15.
9	15	TGND0	–	**Ground.** Ground return for power supply TVCC0.
10	16	TVCC0	AI	**+ 5 volt** power supply input for the port 0 transmit driver. TVCC0 must not vary from TVCC1 or VCC by more than ± 0.3 V.
12	18	DFM	DO	**Driver Fail Monitor.** This signal goes High to indicate a driver output short in one or both ports.
13	19	RLOOP0	DI	**Remote Loopback Enable - Port 0.** When RLOOP = 1, the port 0 clock and data inputs from the framer are ignored and the data received from the twisted-pair line is transmitted back onto the line at the RCLK frequency. **(LLOOP0 must be Low for RLOOP0 to occur.)**
14	20	LOS0	DO	**Loss of Signal - Port 0.** LOS goes High when 175 consecutive spaces have been detected. LOS returns Low when the received signal reaches a mark density of 12.5% (determined by receipt of four marks with a sliding 32-bit period with no more than 15 consecutive zeros). Received marks are output on RPOS/RNEG or RDATA even when LOS is High.
15 16	21 22	RTIP0 RRING0	AI AI	**Receive Tip and Ring - Port 0.** RTIP and RRING comprise the receive line interface. This input pair should be connected to the line through a center-tapped 1:2 transformer.
17	23	LLOOP0	DI	**Local Loopback Enable - Port 0.** When LLOOP is High, the RTIP/RRING inputs from the port 0 line are disconnected and the transmit data inputs are routed back into the receive inputs (through JA if enabled). **(RLOOP0 must be Low for LLOOP0 to occur.)**
18 19	24 25	RRING1 RTIP1	AI AI	**Receive Tip and Ring - Port 1.** RTIP and RRING comprise the receive line interface. This input pair should be connected to the line through a center-tapped 1:2 transformer.

1 Table 4 describes the pins used in Unipolar Hardware Mode.
2. DI = Digital Input; DO = Digital Output; DI/O = Digital Input/Output; AI = Analog Input; AO = Analog Output

Table 3: Hardware Mode Pin and Bipolar Hardware Mode Pin Descriptions[1] – continued

Pin QFP	Pin PLCC	Symbol	I/O[2]	Description
20	26	LOS1	DO	**Loss of Signal - Port 1.** LOS goes High when 175 consecutive spaces have been detected. LOS returns to a logic 0 when the received signal reaches a mark density of 12.5% (refer to LOS0 signal description for details).
21	27	LLOOP1	DI	**Local Loopback Enable - Port 1. (RLOOP1 must be Low for LLOOP1 to occur.)**
22	28	TAOS1	DI	**Transmit All Ones Enable - Port 1. (RLOOP1 must be Low for TAOS1 to occur.)**
23 26	29 32	TRING1 TTIP1	AO AO	**Transmit Ring - Port 1.** The tip and ring pins for each port are differential driver outputs designed to drive a 35 - 200 Ω load. Line matching resistors and transformers can be selected to give the desired pulse height. See Figures 19 through 21.
24	30	TVCC1	AI	**+ 5 volt** power supply input for the port 1 transmit driver. TVCC1 must not vary from TVCC0 or VCC by more than ± 0.3 V.
25	31	TGND1	–	**Ground.** Ground return for power supply TVCC1.
27	33	VCC	AI	**+5 VDC** power supply input for all circuits, except the transmit drivers.
28	34	JASEL	DI	**Jitter Attenuation Select.** Selects jitter attenuation for both ports. When JASEL = 1, JA circuits are placed in the receive paths. When JASEL = 0, JA circuits are placed in the transmit paths. When JASEL is clocked with MCLK, the JA circuit is disabled.
29 30 31	35 36 37	LEN01 LEN11 LEN21	DI DI DI	**Line Length Equalizer inputs - Port 1.** These pins determine the shape and amplitude of the transmit pulse.
32	38	RLOOP1	DI	**Remote Loopback Enable - Port 1. (LLOOP1 must = 0 for RLOOP to occur.)**
33	39	RCLK1	DO	**Receive Clock - Port 1.** This clock is recovered from the twisted-pair input signal. Under Loss of Signal (LOS) conditions, this output is derived from MCLK.
34 35	40 41	RPOS1 (Bipolar) RNEG1 (Bipolar)	DO DO	**Receive Data Positive and Negative - Port 1.** In the Bipolar I/O mode, these pins are the data outputs from port 1. A signal on RPOS corresponds to receipt of a positive pulse on RTIP/RRING. A signal on RNEG corresponds to receipt of a negative pulse on RTIP/RRING. RNEG/RPOS outputs are Non-Return-to-Zero (NRZ). RPOS and RNEG are stable and valid on the rising edge of RCLK.
36 37	42 43	TNEG1 TPOS1	DI DI	**Transmit Data Positive and Negative - Port 1.** In the Bipolar I/O mode, these pins are TPOS and TNEG, the positive and negative sides of a bipolar input pair for port 1. Data to be transmitted onto the twisted-pair line is input at these pins. However, when the TRSTE pin is clocked by MCLK, the LXT332 switches to a unipolar mode. Unipolar mode pin functions are described separately.
38	44	TCLK1	DI	**Transmit Clock - Port 1.** 1.544 MHz for T1, 2.048 MHz for E1. The transmit data inputs are sampled on the falling edge of TCLK.

1 Table 4 describes the pins used in Unipolar Hardware Mode.
2. DI = Digital Input; DO = Digital Output; DI/O = Digital Input/Output; AI = Analog Input; AO = Analog Output

Table 4: Unipolar Hardware Mode Pin Descriptions[1]

Pin QFC	Pin PLCC	Symbol	I/O	Description
41	3	TDATA0	DI	**Transmit Data - Port 0.** In the Unipolar mode, the data to be transmitted onto the line from port 0 is input at this pin.
42	4	ECE0	DI	**Encoder Enable - Port 0.** In the Unipolar mode, a High on this pin enables the B8ZS or HDB3 encoder and decoder for port 0.
43	5	BPV0	DO	**Bipolar Violation - Port 0.** In the Unipolar mode this indicator output goes High when a bipolar violation is received at port 0.
44	6	RDATA0	DO	**Receive Data - Port 0.** In the Unipolar mode, RDATA is a Non-Return-to-Zero (NRZ) output. RDATA is stable and valid on the rising edge of RCLK.
34	40	RDATA1	DO	**Receive Data - Port 1.** In the Unipolar mode, RDATA is a Non-Return-to-Zero (NRZ) output. RDATA is stable and valid on the rising edge of RCLK.
35	41	BPV1	DO	**Bipolar Violation - Port 1.** In the Unipolar mode this indicator output goes High when a bipolar violation is received at port 1.
36	42	ECE1	DI	**Encoder Enable - Port 1.** In the Unipolar mode, a High on this pin enables the B8ZS or HDB3 encoder and decoder for port 1.
37	43	TDATA1	DI	**Transmit Data - Port 1.** In the Unipolar mode, the data to be transmitted onto the line from port 1 is input at this pin.

1 Table 3 describes the pins that do not change function in Unipolar Hardware Mode and the functions of pins unique to Bipolar Mode.

FUNCTIONAL DESCRIPTION

The figure at the beginning of this Data Sheet shows a simplified block diagram of the LXT332. The LXT332 is a fully integrated Dual Line Interface Unit (DLIU) which contains two complete transceivers. The DLIU is designed for both 1.544 Mbps (DSX-1) and 2.048 Mbps (E1) applications. Both transceivers operate at the same frequency, which is determined by the MCLK input.

Each DLIU transceiver front end interfaces with two twisted-pair lines, one pair for transmit, one pair for receive. These two twisted-pair lines comprise a digital data loop for full duplex transmission. The integrated crystal-less jitter attenuator may be positioned in either the transmit or receive path, or disabled.

Each DLIU transceiver back-end interfaces with a framer through either bipolar or unipolar data I/O channels. The DLIU may be controlled by a microprocessor through the serial port (Host control mode), or by hard-wired pins for stand-alone operation (Hardware control mode).

Receiver

The two receivers in the LXT332 DLIU are identical. The following paragraphs describe the operation of one.

The twisted-pair input is received via a center-tapped 1:2 transformer. Positive pulses are received at RTIP, negative pulses at RRING. Recovered data is output at RPOS and RNEG in the bipolar mode and at RDATA in the unipolar mode. The recovered clock is output at RCLK. RPOS/RNEG or RDATA outputs are valid on the rising edge of RCLK. Refer to the Test Specifications Section for receiver timing.

The receive signal is processed through the peak detector and data slicers. The peak detector samples the received signal and determines its maximum value. A percentage of the peak value is provided to the data slicers as a threshold level to ensure optimum signal-to-noise ratio. For DSX-1 applications (line length inputs LEN0 - LEN2 $\neq$ 000 or 001) the threshold is set to 70% (typical) of the peak value. This threshold is maintained above the specified level for up to 15 successive zeros over the range of specified operating conditions. For E1 applications (LEN inputs = 000 or 001), the threshold is 50 % (typical).

The receiver is capable of accurately recovering signals with up to -13.6 dB of attenuation (from 2.4 V), corresponding to a received signal level of approximately 500 mV. Maximum line length is 1500 feet of ABAM cable (approximately 6 dB of attenuation). Regardless of received signal level, the peak detectors are held above a minimum level of 0.3 V (typical) to provide immunity from impulsive noise.

After processing through the data slicers, the received signal goes to the data and timing recovery section, and to the receive monitor. The data and timing recovery circuits provide an input jitter tolerance better than required by Pub 62411 or ITU G.823, as shown in Test Specifications.

The receiver monitor loads a digital counter at the RCLK frequency. The count is incremented each time a zero is received, and reset to zero each time a one (mark) is received. Upon receipt of 175 consecutive zeros the LOS flag is set, and the recovered clock is replaced by MCLK at the RCLK output in a smooth transition. (MCLK is required for receive operation.) When the received signal reaches 12.5% ones density (4 marks in a sliding 32-bit period) with no more than 15 consecutive zeros, the LOS flag is reset and another smooth transition replaces MCLK with the recovered clock at RCLK. During LOS conditions, received data is output on RPOS/RNEG (or RDATA if unipolar I/O is selected).

Depending on the options selected, recovered clock and data signals may be routed through the jitter attenuator, through the B8ZS/HDB3 decoder, and may be output to the framer as either bipolar or unipolar data. In unipolar data I/O mode, the LXT332 reports bipolar violations via an output for one RCLK period on the respective BPV pin.

Transmitter

The two transmitters in the LXT332 DLIU are identical. The following paragraphs describe the operation of a single transmitter.

Transmit data from the framer is clocked serially into the device at TPOS/TNEG in the bipolar mode or at TDATA in the unipolar mode. The transmit clock (TCLK) supplies the input synchronization. The transmitter samples TPOS/TNEG or TDATA inputs on the falling edge of TCLK. If TCLK is not supplied, the transmitter remains powered down and the TTIP/TRING outputs are held in a high-Z state, except during RLOOP, DLOOP, QRSS or TAOS modes. A separate power supply (TVCC0 or TVCC1) supplies each output driver. Current limiters on the output drivers provide short circuit protection. Refer to the Test Specifications Section for MCLK and TCLK timing characteristics. The LXT332 transmits data as a 50% AMI line code as shown in Figure 3. Enabling the zero suppression encoders/decoders overrides the default and the transmission complies with the selected encoding scheme.

Zero suppression is available only in Unipolar Mode. The two zero-suppression types are B8ZS, used in T1 environ-

ments, and HDB3, used in E1 environments. The scheme selected depends on whether the application is T1 or E1.

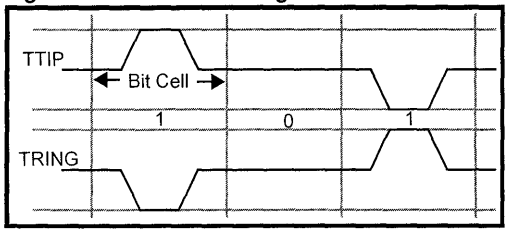
Bipolar Violation Insertions

In the Host mode with unipolar data I/O selected, a Bipolar Violation (BPV) insert function is available. When the VCQE pin is held High, VCQ0 and VCQ1 pins control bipolar Violation Insertion (VI) for ports 0 and 1, respectively. TDATA and VI are both sampled on the falling edge of TCLK. If VI is High, the next available mark is transmitted as a BPV, except as follows:

1. B8ZS and HDB3 zero suppression is not violated.
2. If Local Loopback (LLOOP) and Transmit All Ones (TAOS) are both active, the BPV is looped back to RDATA but the line driver transmits All Ones (no violations).
3. During Remote Loopback (RLOOP = 1), BPV Insert is disabled.

A Low-to-High transition on VI is required for each subsequent BPV insertion.

Figure 3: 50% AMI Coding



Pulse Shape

The transmitted pulse shape is determined by Line Length equalizer control signals LEN0 through LEN2 as shown in Table 5. Equalizer codes are hardwired in Hardware mode. In Host mode the LEN codes are input through the serial interface. Shaped pulses are applied to the AMI line driver for transmission onto the line at TTIP and TRING. The line driver provides a constant low output impedance of < 3Ω (typical), regardless of whether it is driving marks or spaces. This well controlled impedance provides excellent return loss when used with external precision resistors (± 1 % accuracy) in series with the transformer. Table 8 lists recommended transformer specifications. The Application Information Section lists transformer specifications, recommended transformer ratios, series resistor (Rt) values, and typical return losses for various LEN codes. To minimize power consumption the LXT332 can be tied directly to a 1:1.15 transformer without series resistors.

Pulses can be shaped for either 1.544 Mbps or 2.048 Mbps applications. 1.544 Mbps pulses for DSX-1 applications can be programmed to match line lengths from 0 to 655 feet of 22 AWG ABAM cable. A combination of 9.1 Ω resistors and a 1:2.3 transformer is recommended for DSX-1 applications. The LXT332 also matches FCC pulse mask specifications for CSU applications.

The LXT332 produces 2.048 Mbps pulses for both 75Ω coaxial (2.37 V) or 120Ω shielded (3.0 V) lines through an output transformer with a 1:2 turns ratio. For coaxial systems, 9.1 Ω series resistors are recommended. For twisted-pair lines, use 15 Ω resistors.

Table 5: Equalizer Control Inputs

LEN2	LEN1	LEN0	Line Length[1]	Cable Loss[2]	Application	Transmit Rate
0	1	1	0 – 133 ft. ABAM	0.6 dB	DSX-1	1.544 Mbps
1	0	0	133 – 266 ft ABAM	1.2 dB		
1	0	1	266 – 399 ft ABAM	1.8 dB		
1	1	0	399 – 533 ft ABAM	2.4 dB		
1	1	1	533 – 655 ft ABAM	3.0 dB		
0	0	0	ITU Recommendation G.703		E1 – Coax (75Ω)	2.048 Mbps
0	0	1			E1 – Twisted-pair (120Ω)	
0	1	0	FCC Part 68, Option A		CSU	1.544 Mbps

1 Line length from LXT332 to DSX-1 cross-connect point
2. Maximum cable loss at 772 kHz

Driver Failure Monitor

The transceiver incorporates an internal Driver Failure Monitor (DFM) in parallel with TTIP and TRING. A capacitor, charged via a measure of the driver output current and discharged by a measure of the maximum allowable current detects driver failure. Shorted lines draw excess current, overcharging the cap. When the capacitor charge deviates outside the nominal charge window, a driver fail is reported. In Host mode the DFM bit is set in the serial word. In Hardware mode the DFM pin goes High. During a long string of spaces, a short-induced overcharge eventually bleeds off, clearing the DFM flag.

Jitter Attenuation

A digital Jitter Attenuation Loop (JAL) combined with an Elastic Store (ES) provides Jitter attenuation. The JAL is internal and requires no external crystal nor high-frequency (higher than line rate) clock. When JASEL = 1, the JAL is positioned in the receive path. When JASEL = 0, the JAL is positioned in the transmit path. With JASEL clocked by MCLK, the JAL is disabled. MCLK is the reference for the JAL.

The ES is a 32 x 2-bit register. Data is clocked into the ES with the associated clock signal (TCLK or RCLK), and clocked out of the ES with the dejittered JAL clock. When the ES is within two bits of overflowing or underflowing, the ES adjusts the output clock by 1/8 of a bit period. The ES produces an average delay of 16 bits in the associated path.

Host Mode provides a dejittered High Frequency Clock (HFC). This 8x clock (12.352 MHz for T1, 16.384 MHz for E1) is tied to the output clock from the JAL. With JA active in the receive path, HFO is tied to RCLK and under LOS conditions defaults to MCLK. With JA active in the transmit path, HFO is tied to TCLK and defaults to MCLK if TCLK is not available. If JA is disabled, HFO is tied to MCLK.

Built-In Self Test

In Host mode, the LXT332 provides a Built-In Self Test (BIST) mode. Quasi-Random Signal Source (QRSS) generation and detection circuitry is integrated into the LXT332. When the QRSS BIST mode is selected, the LXT332 detects and reports QRSS pattern sync on the incoming signal. When triggered, the LXT332 also transmits the QRSS pattern onto the line. Pattern transmission and detection is independently triggered and reported for each port. Refer to Diagnostic Mode Operation for detailed description.

Control Modes

The LXT332 transceiver operates in stand alone Hardware (default) Mode or Host Mode depending on the input to the SPE pin. When tied to SPE, MCLK acts as a Serial Port Enable signal to force the LXT332 into its Host mode. The data I/O mode, bipolar or unipolar, is controlled by the TRSTE pin. With TRSTE Low, bipolar I/O is selected. With TRSTE clocked, unipolar I/O is selected. Several diagnostic modes are available on command.

Host Mode Control

The LXT332 operates in the Host mode when the SPE pin is clocked with MCLK. In Host mode a microprocessor controls the LXT332 through the serial I/O port (SIO) which provides common access to both LIUs. Each of the two LIUs contains a pair of data registers, one for command inputs and one for status outputs. Only one LIU can be selected at a time. If both PS0 and PS1 are active, Port 0 has priority over Port 1. An SIO transaction is initiated by a falling pulse on one of the two Port Select pins, PS0 or PS1. A High-to-Low transition on PS0/1 is required for each subsequent access to the Host mode registers. If both PS0 and PS1 are active simultaneously, Port 0 has priority over Port 1.

The LIU addressed by the PS pulse responds by writing the incoming serial word from the SDI pin into its command register. Figure 4 shows an SIO write operation. The 16-bit serial word consists of an 8-bit Command/Address byte and an 8-bit Data byte. If the command word contains a read request, the addressed LIU subsequently outputs the contents of its status register onto the SDO pin. Figure 5 shows an SIO read operation. The Clock Edge (CLKE) signal determines when the SDO and receive data outputs are valid, relative to the Serial Clock (SCLK) or RCLK as listed in Table 6. Refer to the Test Specifications section for SIO timing.

Serial Input Word

Figure 4 shows the Serial Input data structure. The LXT332 is addressed by setting bit A4 in the Address/Command byte, corresponding to address 16. Bit 1 of the serial Address/Command byte provides Read/Write (R/$\overline{W}$) control when the chip is accessed. The R/$\overline{W}$ bit is set to logic 1 to read the data output byte from the chip, and set to logic 0 to write the input data byte to the chip.

The second 8 bits of a write operation, the Data Input byte, clear Loss of Signal (LOS) and Driver Fail Monitor (DFM) interrupts, reset the chip, and control diagnostic modes. The first 2 bits (D0 – D1) clear and/or mask LOS and DFM interrupts, and the last 3 bits (D5 - D7) control operating

modes (normal and diagnostic) and chip reset. Refer to Table 7 for details on bits D5 – D7 Serial Output Word.

Serial Output Word

Figure 4 shows the Serial Output data structure. SDO is high impedance when SDI receives an Address/Command byte. If SDI receives a write command (R/W = 0), SDO remains in high impedance. If the command is a read (R/W = 1), then SDO becomes active after the last Command/Address bit (A6) and remains active for eight SCLK cycles. Typically the first bit out of SDO changes the state of SDO from high-z to a Low/High. This occurs approximately 100 µs after the eighth following edge of SCLK.

The output data byte reports Loss of Signal (LOS) and Driver Fail Monitor (DFM) conditions, equalizer settings, and operating modes (normal or diagnostic). The first 5 bits (D0 - D4) report LOS and DFM status, and the Line Length Equalizer settings. The last 3 bits (D5 - D7) report operating modes and interrupt status.

If the $\overline{\text{INT}x}$ line for port x is High (no interrupt is pending), bits D5 - D7 report the operating modes listed in Table 8. If the $\overline{\text{INT}x}$ line for port x is Low, the interrupt status overrides all other reports and bits D5 - D7 reflect the interrupt status as listed in Table 8.

Table 6: CLKE Settings

CLKE	Output	Clock	Valid Edge
LOW	RPOS/RNEG RDATA SDO	RCLK RCLK SCLK	Rising Rising Falling
HIGH	RPOS/RNEG RDATA SDO	RCLK RCLK SCLK	Falling Falling Rising

Table 7: SIO Input Bit Settings (See Figure 4)

Mode	RLOOP Bit D5	LLOOP Bit D6	TAOS Bit D7
RLOOP	1	0	N/A
LLOOP	0	1	N/A
DLOOP	1	1	1
TAOS	0	*n/a*	1
RESET	1	1	0

Table 8: LXT332 Serial Data Output Bit Coding (See Figure 5)

Bit			Operating Modes
D5	D6	D7	
0	0	0	Reset has occurred, or no program input (*i.e.*, normal operation) or DLOOP active.[1]
0	0	1	TAOS active
0	1	0	LLOOP active
0	1	1	TAOS and LLOOP active
1	0	0	RLOOP active
			Interrupt Status
1	0	1	DFM has changed state since last Clear DFM occured
1	1	0	LOS has changed since last Clear LOS occurred
1	1	1	DFM and LOS have changed since last Clear DFM and Clear LOS occurred

1 No explicit status information is available on DLOOP.

Figure 4: LXT332 SIO Write Operation

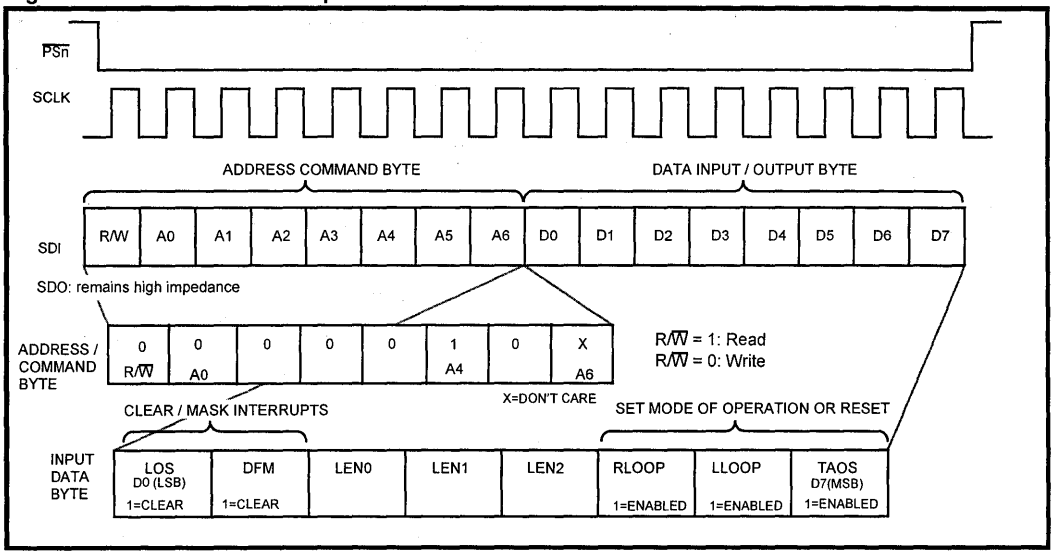
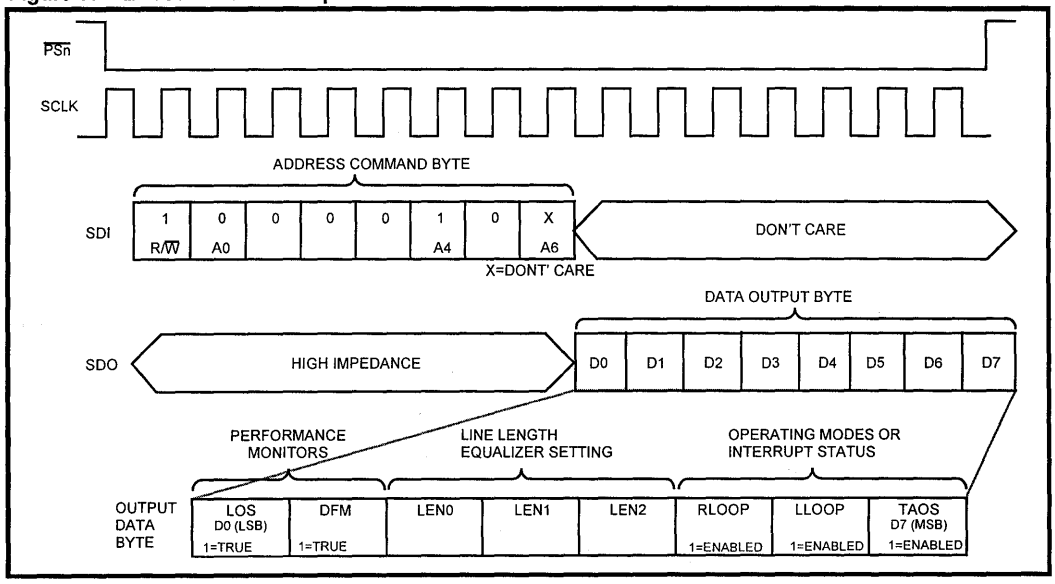


Figure 5: LXT332 SIO Read Operation



Interrupt Handling

The Host mode provides two latched Interrupt output pins, INT0 and INT1, one for each LIU. An interrupt is triggered by a change in the LOS or DFM bits (D0 and D1 of the output data byte, respectively). As shown in Figure 6, either or both interrupt generators can be masked by writing a one to the respective bit of the input data byte (D0 = LOS, D1 = DFM). When an interrupt has occurred, the INTx output pin is pulled Low. The output stage of each INTx pin consists only of a pull-down device. Hence, an external pull-up resistor is required. The interrupt is cleared as follows:

1. If one or both interrupt bits (LOS or DFM, D0 and D1 of the output data byte) =1, writing a 1 to the respective input bit (D0 or D1, respectively, of the input data byte) will clear the interrupt. Leaving a 1 in either of these bit positions will effectively mask the associated interrupt. To re-enable the interrupt capability, reset D0 and/or D1 to 0.
2. If neither LOS or DFM=1, the interrupt will be cleared by resetting the chip. To reset the chip, set data input bits D5 and D6 = 1, and D7 = 0.

Hardware Mode Control

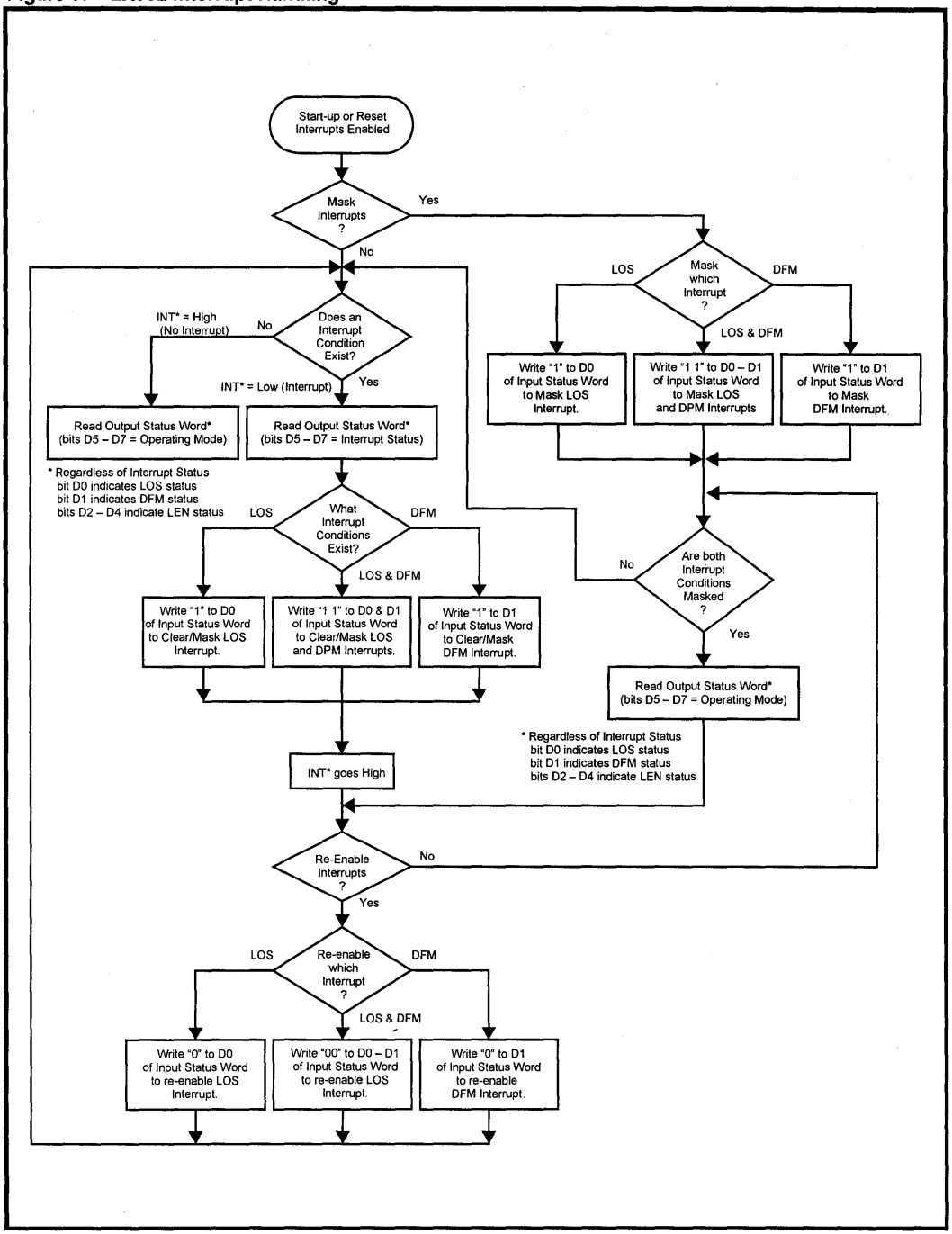
Hardware control is the default operating mode; the LXT332 operates in Hardware mode unless LEN11/SPE pin is clocked. In Hardware mode the transceiver is controlled through individual pins; a µP is not required. The SIO pins are re-mapped to provide control functions. (Data I/O mode selection is unaffected by the control mode. The TRSTE pin selects either unipolar or bipolar data I/O.) In Hardware mode the RPOS/RNEG or RDATA/BPV outputs are valid on the rising edge of RCLK.

Diagnostic Mode Operation

The LXT332 offers multiple diagnostic modes. Local Loopback (LLOOP), Remote Loopback (RLOOP), Dual Loopback (DLOOP) and Transmit All Ones (TAOS) are available under both Host and Hardware control. An additional Quasi-Random Signal Source (QRSS) mode is available under Host control only.

Under Host control, diagnostic modes are selected by writing the appropriate SIO bits. Under Hardware control, diagnostic modes are selected by a combination of pin settings. The pins must be held at the specified levels for a minimum of 20 ns. The SIO bit names (Host Mode) and pin identifiers (Hardware Mode) for diagnostic functions are identical. Where a particular function can be enabled in either mode, 1=High and 0=Low.

Figure 6: LX332 Interrupt Handling



Transmit All Ones. See Figure 7. Transmit All Ones (TAOS) is selected when TAOS = 1 and RLOOP = 0. In TAOS mode the TPOS and TNEG inputs are ignored. The TAOS reference clock is determined by setting the jitter attenuator. When jitter attenuation is set for the transmit side, MCLK is used as the reference clock and TCLK is the fall back clock. When JA is set for the receive side, TCLK is the reference clock and MCLK is the fall back clock. When JA is inactive, MCLK is the TAOS reference clock and TCLK is the fall back. TAOS can be commanded simultaneously with Local Loopback as shown in Figure 8, but is inhibited during Remote and Dual Loopback.

Local Loopback. See Figures 8 and 9. Local Loopback (LLOOP) is selected when LLOOP = 1 and RLOOP = 0. In LLOOP mode the receiver circuits are inhibited. The transmit clock and data inputs (TCLK and TPOS/TNEG or TDATA) are looped back and output at RCLK and RPOS/RNEG or RDATA. During local loopback, the JASEL input functions as follows: If JASEL=0, JA is enabled and active in both the Transmit path and the loopback circuit. If JASEL=1, JA is enabled in the Loopback circuit only. If JASEL = MCLK, JA is disabled.

The transmitter circuits are unaffected by LLOOP. The TPOS/TNEG or TDATA inputs (or a stream of 1s if the TAOS command is active) will be transmitted normally. When used in this mode, the transceiver can be used as a stand-alone jitter attenuator.

Remote Loopback. See Figure 10. Remote Loopback (RLOOP) is selected when RLOOP = 1 and LLOOP = 0. (Under this condition, TAOS is ignored. TAOS cannot be commanded simultaneously with RLOOP.) In RLOOP mode, the transmit clock and data inputs (TCLK and TPOS/TNEG or TDATA) are ignored. The RPOS/RNEG or RDATA outputs are looped back to the transmit circuits and output on TTIP and TRING at the RCLK frequency. Receiver circuits are unaffected by the RLOOP command and continue to output the data and clock signals received from the line. During remote loopback, the JASEL input functions as follows: If JASEL = 1, JA is enabled and active in both the Receive path and the loopback circuit. If JASEL = 0, JA is enabled in the Loopback circuit only. If JASEL = MCLK, JA is disabled.

Dual Loopback. See Figure 11. Dual Loopback (DLOOP) is selected when RLOOP = 1, LLOOP = 1 and TAOS = 1. In DLOOP mode, the transmit clock and data inputs (TCLK and TPOS/TNEG or TDATA) are looped back through the jitter attenuator (unless disabled by a clock input to the JASEL pin) and output at RCLK and RPOS/RNEG or RDATA. The data and clock recovered from the line are looped back through the transmit circuits and output on TTIP and TRING without jitter attenuation. Unlike the other diagnostic modes, no explicit SIO status indicator is available for DLOOP in the SIO status register.

Figure 7: TAOS Data Path

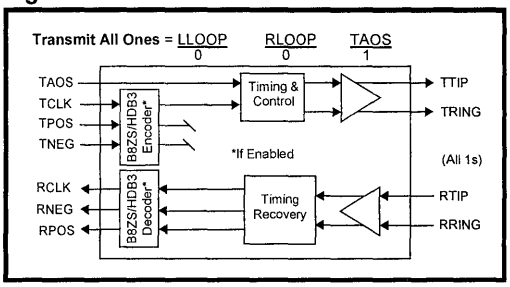


Figure 8: TAOS with LLOOP & Selectable JA

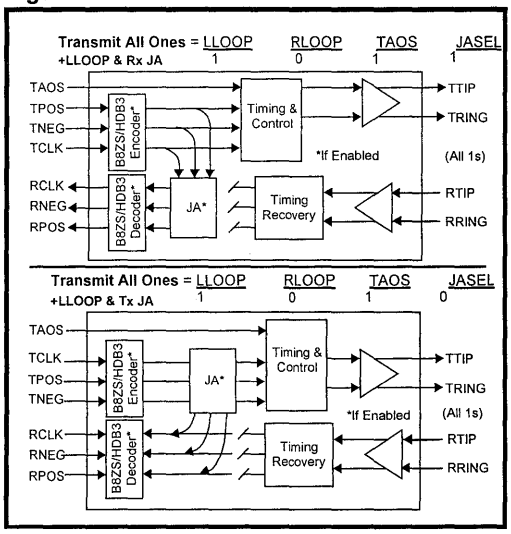
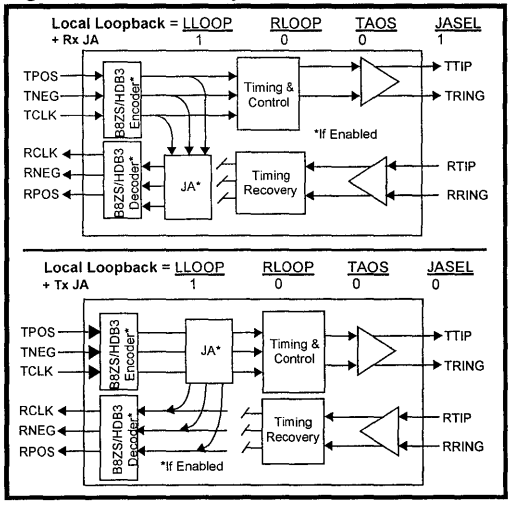


Figure 9: Local Loopback with Selectable JA



QRSS Built-In Self Test (Host Mode only). See Figure 12. The QRSS Built-In Self Test (BIST) mode is available only under Host control. The QRSS BIST mode is selected by clocking the VCQE pin with MCLK. Once the QRSS BIST mode is selected, the VCQ0 and VCQ1 pins are re-mapped to trigger the QRSS transmission. A High on one of these pins triggers QRSS pattern transmission from the appropriate port. The QRSS pattern for DSX-1 systems is 2^{20}-1, with no more than 14 consecutive zeros. For CEPT systems the QRSS pattern is 2^{15}-1. The QRSS pattern is locked to MCLK. Once the QRSS transmission is activated, errors can be inserted into the transmit data stream by causing a Low-to-High transition on the TPOS/TDATA pin for the respective port. In Bipolar mode, Low-High transitions cause both a logic error and a bipolar violation to be inserted into the QRSS data stream. In Unipolar mode, only a logic error is inserted.

The Pattern Detect circuitry is activated by the QRSS BIST mode, although the basic receive circuits are unaffected. The Pattern Detect (PD*n*) pins indicate QRSS pattern sync. The Pattern Detect pin stays High until synchronization is achieved on the QRSS pattern. The QRSS pattern is considered in sync when there are fewer than 4 errors in 128 bits. The PD pin goes High indicating an out-of-sync conditions if 4 or more errors are detected in 128 bits (i.e. sync is defined as fewer than 4 errors in 128 bits).

Initialization/Reset Operation

Upon initial power up, the transceiver is held static until the power supply reaches approximately 3 V. Upon crossing this threshold, the device clears all internal registers and begins calibration of the delay lines. A reference clock is required to calibrate the delay lines. TCLK is the transmit reference, and MCLK is the receive reference. The PLLs are continuously calibrated.

The transceiver can be reset from the Host or H/W mode. In Host mode, reset is commanded by writing 1s to RLOOP and LLOOP, and a 0 to TAOS (bits D5, D6 and D7, respectively, of the SIO input data byte). In H/W mode, reset is commanded by simultaneously holding RLOOP and LLOOP High, and TAOS Low, for approximately 200 ns. Reset is initiated on the falling edge of the reset request. In either mode, each port is reset independently. Reset clears and sets all SIO registers to 0 at the affected port. Reset is not generally required for the port to be operational.

Figure 10: Remote Loopback with Selectable JA

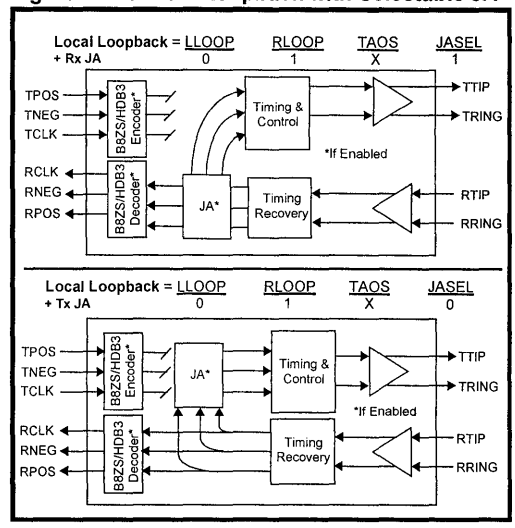


Figure 11: Dual Loopback

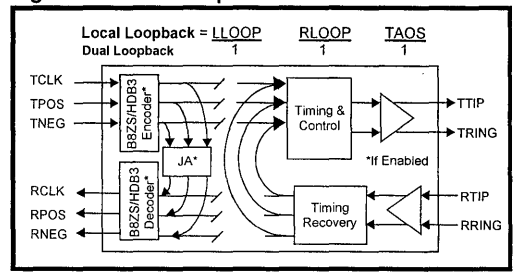
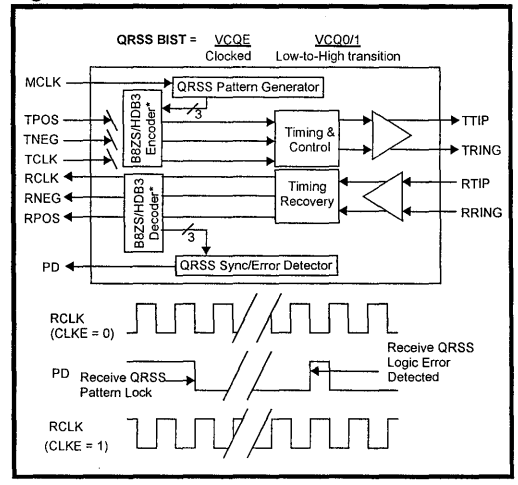


Figure 12: QRSS BIST Mode



APPLICATION INFORMATION

Power Requirements

The LXT332 is a low-power CMOS device. It operates from a single +5 V power supply which can be tied to all three VCC inputs. However, all inputs must be within ± .3 V of each other, and decoupled to their respective grounds separately. Isolation between the transmit and receive circuits is provided internally. During normal operation or local loopback, the transmitter powers down if TCLK is not supplied.

Transformers

The transformer specifications listed in Table 9 give the correct impedance matching for balanced transmit or receive lines. Table 10 shows the combinations of resistors and transformers to produce a variety of return loss values depending on the LEN code settings chosen for a specific design

1.544 Mbps T1 Applications

Figure 13 shows a typical host mode application. The eight serial interface pins are grouped at the top. Host mode is selected by the clock input to SPE. Other mode selection pins are shown at the bottom. With the TRSTE pin switched Low, the LXT332 operates in the bipolar I/O mode. Driving JASEL Low switches the jitter attenuation circuits into the transmit paths for both LIU ports.

Figure 13 shows a pair of framers (a dual framer could also be used). A LXP600A Clock Adapter (CLAD) converts the 2.048 MHz backplane clock to provide the 1.544 MHz input to the MCLK and TCLK inputs of both LIU ports.

The DFM and PD indicators and High frequency clocks are grouped in the diagram lower left. These outputs are available to drive optional external circuits. The driver power supply inputs (lower right) are tied to a common bus with 1.0 µF decoupling capacitors installed. The power supply for the remaining (non-driver) circuitry is shown at center right with 68 µF and 0.1 µF decoupling capacitors.

The line interface circuitry is identical for both LIU ports. The precision resistors in line with the transmit transformer provide optimal return loss. The recommended transformer/resistor combinations are listed at the bottom of Figure 15. Center tapped 2:1 transformers are used on the receive side.

Table 9: Recommended Transformer Values

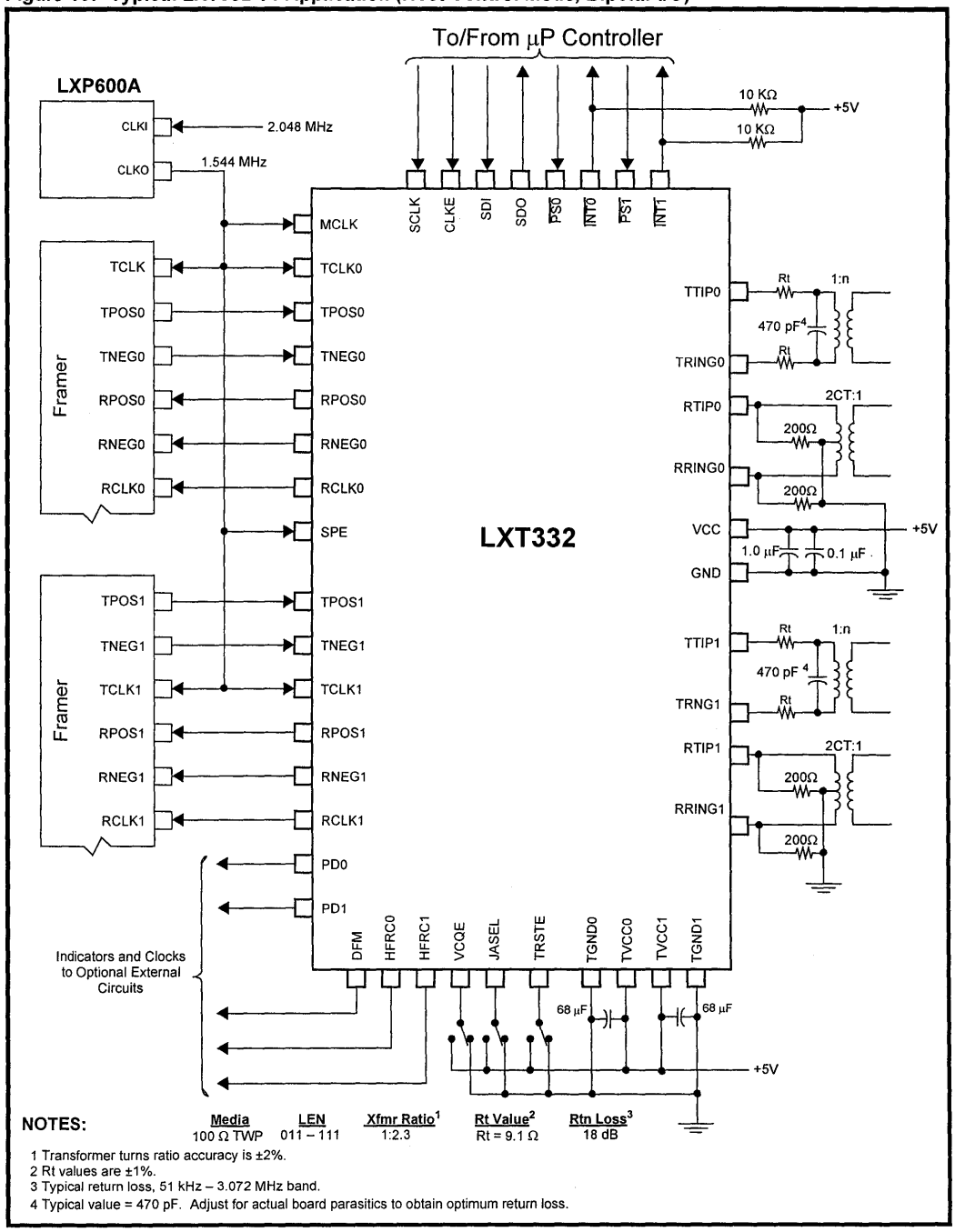
Parameter	Value
Turns Ratio (T1)	1:2.3 (Tx) / 1:2 CT (Rx)
Turns Ratio (E1)	1:2 (Tx) / 1:2 CT (Rx)
Primary Inductance	1.2 mH maximum
Leakage Inductance	0.5 µH maximum
Interwinding Capacitance	25 pF maximum
DC Resistance (Pri.)	1 Ω maximum
ET (Breakdown Voltage)	1 kV minimum

Table 10: Transformer Combinations

LEN	Xfmr Ratio[1]	Rt Value[2]	Rtn Loss[3]
For T1/DSX-1 100 Ω Twisted-Pair Applications:			
011 – 111	1:2	Rt = 9.1 Ω	14 dB
011 – 111	1:2.3	Rt = 9.1 Ω	18 dB
011 – 111	1:1.15	Rt = 0 Ω	18 dB
For E1 120 Ω Twisted-Pair Applications:			
001	1:2	Rt = 15 Ω	18 dB
000	1:2	Rt = 9.1 Ω	10 dB
For E1 75 Ω Coaxial Applications:			
001	1:2	Rt = 14.3 Ω	10 dB
000	1:2	Rt = 9.1 Ω	18 dB

1 Transformer turns ratio accuracy is ±2 %.
2. Rt values are ±1 %.
3. Typical return loss, 51 kHz – 3.072 MHz, with a capacitor in parallel with the primary side of the transformer.

Figure 13: Typical LXT332 T1 Application (Host Control Mode, Bipolar I/O)



2.048 Mbps E1/CEPT Interface Applications

E1 Coaxial Applications

Figure 14 shows the line interface for a typical 2.048 Mbps E1 coaxial (75Ω) application. The LEN code should be set to 000 for coax. With 9.1Ω Rt resistors in line with the 1:2 output transformers, the LXT332 produces 2.37 V peak pulses as required for coax applications. As in the T1 application shown in Figure 13, center tapped 1:2 transformers are used on the receive side.

E1 Twisted-Pair Applications

Figure 15 shows a typical 2.048 Mbps E1 twisted-pair (120Ω) application. With the TRSTE pin tied to ground the LXT332 operates in the bipolar data I/O mode. The JA circuit is placed in the transmit path by the Low on JASEL The line length equalizers are controlled by the hardwired LEN inputs. With the LEN code set to 001 and 15Ω Rt resistors in line with the 1:2 output transformers, the LXT332 produces the 3.0 V peak pulses required for this application. Center tapped 1:2 transformers are used on the receive side.

A single clock source provides the 2.048 MHz input to MCLK and TCLK. The DFM pin may routed to an LED driver or other indicator, or be left unconnected. Switches on the TAOS, LLOOP and RLOOP inputs provide mode control and hardware reset capability.

As in Figure 15, the power supply inputs are tied to a common bus with appropriate decoupling capacitors installed (1.0 µF on the transmit side, 68 µF and 0.1 µF on the receive side.)

Figure 14: Line Interface for E1 Coax Applications

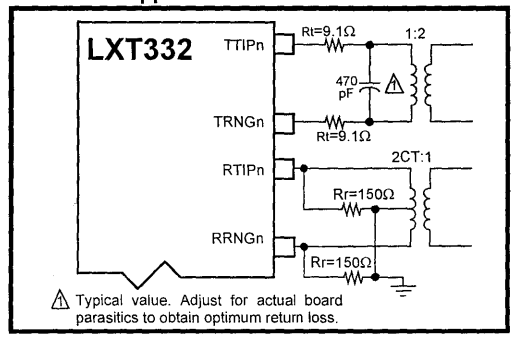
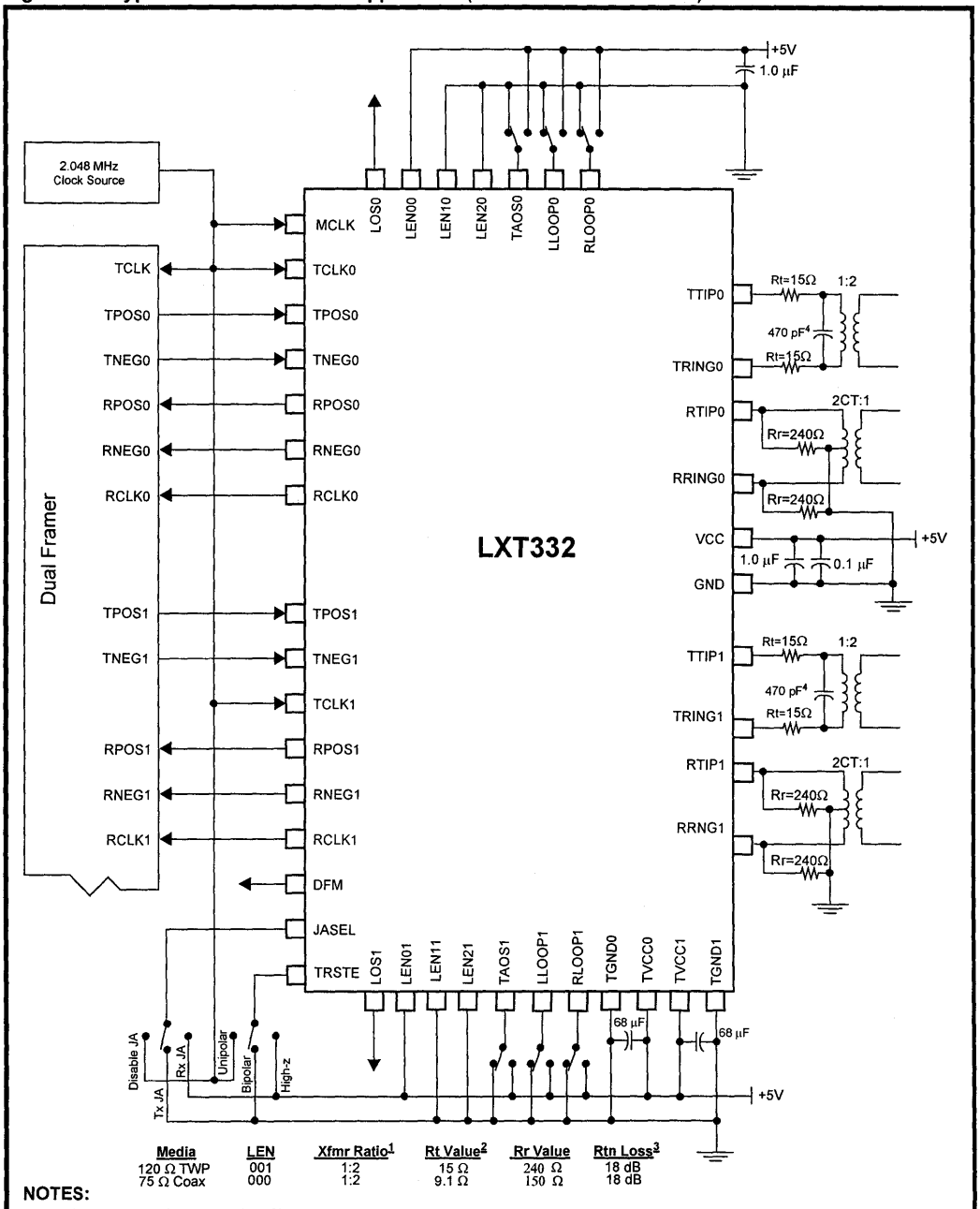


Figure 15: Typical LXT332 E1 120 Ω Application (Hardware Control Mode)



Media	LEN	Xfmr Ratio[1]	Rt Value[2]	Rr Value	Rtn Loss[3]
120 Ω TWP	001	1:2	15 Ω	240 Ω	18 dB
75 Ω Coax	000	1:2	9.1 Ω	150 Ω	18 dB

NOTES:

1 Transformer turns ratio accuracy is ±2%.
2 Rt values are ±1%.
3 Typical return loss, 51 kHz – 3.072 MHz band.
4 Typical value = 470 pF. Adjust for actual board parasitics to obtain optimum return loss.

TEST SPECIFICATIONS

NOTE

Information in Tables 11 through 17 and Figures 16 through 21 represent the performance specifications of the LXT332 Dual Line Interface Unit and are guaranteed by test, except as noted, by design.

Table 11: Absolute Maximum Ratings

Parameter	Sym	Min	Max	Units
DC supply (referenced to GND)	VCC, TVCC0, TVCC1	–	6.0	V
Input voltage, any pin [1]	VIN	GND - 0.3	VCC + 0.3	V
Input current, any pin [2]	IIN	-10	10	mA
Storage temperature	TSTG	-65	+150	°C

CAUTION

Operations at or beyond these limits may result in damage to the device.
Normal operation not guaranteed at these extremes.

1 Excluding RTIP and RRING which must stay between -6 V and Vcc + 0.3 V.
2. Transient currents of up to 100 mA will not cause SCR latch-up. TTIP, TRING, TV+, and TGND can withstand continuous current of 100 mA.

Table 12: Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Units
DC supply [1]	VCC, TVCC0, TVCC1	4.75	5.0	5.25	V
Ambient operating temperature	TA	-40	25	85	°C

1 Variation between TVCC0, TVCC1 and VCC must be within ±0.3 V of each other during steady state and transient conditions.

Table 13: Electrical Characteristics (Over Recommended Range)

Parameter	Sym	Min	Typ	Max	Units	Test Conditions
Total power dissipation – T1 [1] (Maximum line length)	PD	–	700	900	mW	100% ones density
	PD	–	550	700	mW	50% ones density
Total power dissipation – E1 [1]	PD	–	575	700	mW	100% ones density
	PD	–	490	600	mW	50% ones density
High level input voltage [2,3]	VIH	2.0	–	–	V	
Low level input voltage [2,3]	VIL	–	–	0.8	V	
High level output voltage [2,3]	VOH	2.4	–	–	V	IOUT = -400 µA
Low level output voltage [2,3]	VOL	–	–	0.4	V	IOUT = 1.6 mA
Input leakage current [4]	ILL	0	–	±10	µA	
Three-state leakage current [2]	ISL	0	–	±10	µA	
Input pull down current (MCLK)[5]			–	100	µA	
TTIP/TRING leakage current	ITR	–	–	1.2	mA	In tri-state and power down modes

1 Total power dissipation includes the device power consumption and load power dissipation while driving a 75 Ω load on the secondary side. The T1 test circuit is a 100 Ω line load connected to the driver outputs via a 1:1.15 turns ratio transformer without series resistors.
2. Functionality of pins depends on mode.
3. Output drivers will output CMOS logic levels into CMOS loads.
4. Except for MCLK, RTIP0, RRING0, RTIP1, and RRING1.
5. Applies to pins 8,11,23,26

Table 14: Analog Specifications (Over Recommended Range)

Parameter		Min	Typ	Max	Units	Test Conditions
AMI Output Pulse Amplitudes	DSX-1	2.4	3.0	3.6	V	measured at the DSX
	E1 (120 Ω)	2.7	3.0	3.3	V	measured at line side
	E1 (75 Ω)	2.13	2.37	2.61	V	measured at line side
Transmit amplitude variation with supply [3]		–	1	2.5	%	
Recommended output load at TTIP and RRING		–	75	–	Ω	
Driver output impedance [3]		–	3	10	Ω	@ 772 kHz
Jitter added by the transmitter [1]	10 Hz - 8 kHz [3]	–	0.005	0.01	UI	T1 Jitter based
	8 kHz - 40 kHz [3]	–	0.015	0.025	UI	
	10 Hz - 40 kHz [3]	–	0.02	0.025	UI	
	Broad Band	–	0.03	0.05	UI	
Jitter added by the transmitter [1]	20 Hz – 100 kHz	–	–	0.05	UI	E1 Jitter Band
Output power levels [3]	@772 kHz	12.6	–	17.9	dBm	
DS1 2 kHz BW	@ 1544 kHz	-29	–	–	dB	referenced to power in 2 kHz band at 772 kHz
Positive to negative pulse imbalance		–	–	0.5	dB	
Receive input impedance		–	40	–	kΩ	
Sensitivity below DSX (0 dB = 2.4 V)		13.6	–	–	dB	
(max 6 dB cable attenuation)		500	–	–	mV	
Loss of Signal threshold		–	0.3	–	V	
Data decision threshold	DSX-1	60	70	77	% peak	
	E1	43	50	57	% peak	
Input jitter tolerance	10 Hz	–	1200	–	UI	
	750 Hz	14	–	–	UI	
	10 kHz – 100 kHz	0.4	–	–	UI	
Allowable consecutive zeros before LOS		160	175	190	–	
Jitter attenuation curve corner frequency [2,3]	T1	–	6	–	Hz	
	E1	–	10	–	Hz	
Attenuation input jitter tolerance before FIFO overflow [3]		28	–	–	UI	
Jitter attenuation @ 10 kHz			45	–	dB	

1 Input signal to TCLK is jitter-free.
2. Circuit attenuates jitter at 20 dB/decade above the corner frequency.
3. Not production tested, but guaranteed by design and other correlation models.

Table 15: LXT332 Serial I/O Timing Characteristics (See Figures 16 and 17)

Parameter	Sym	Min	Typ[1]	Max	Units	
Rise/Fall time - any digital output	t_{RF}	–	–	100	ns	Load 1.6 mA, 50 pF
SDI to SCLK setup time	tDC	50	–	–	ns	
SCLK to SDI hold time	t_{CDH}	50	–	–	ns	
SCLK Low time	t_{CL}	240	–	–	ns	
SCLK High time	t_{CH}	240	–	–	ns	
SCLK rise and fall time	t_R, t_F	–	–	50	ns	
PS to SCLK setup time	t_{PC}	50	–	–	ns	
SCLK to PS hold time	t_{CPH}	50	–	–	ns	
PS inactive time	t_{PWH}	250	–	–	ns	
SCLK to SDO valid	t_{CDV}	–	–	200	ns	
SCLK falling edge or PS rising edge to SDO high-z	t_{CDZ}	–	100	–	ns	

1 Typical figures are at 25 °C and are design aid only; not guaranteed and not subject to production testing.

Figure 16: LXT332 Serial Data Input Timing Diagram

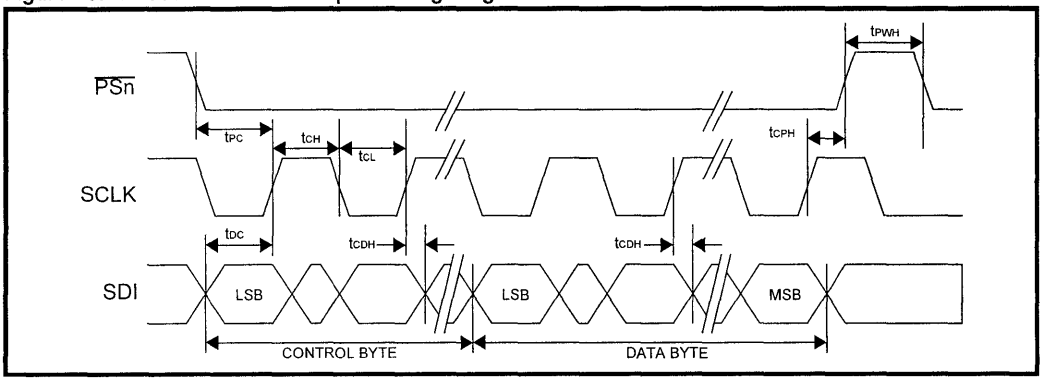


Figure 17: LXT332 Serial Data Output Timing Diagram

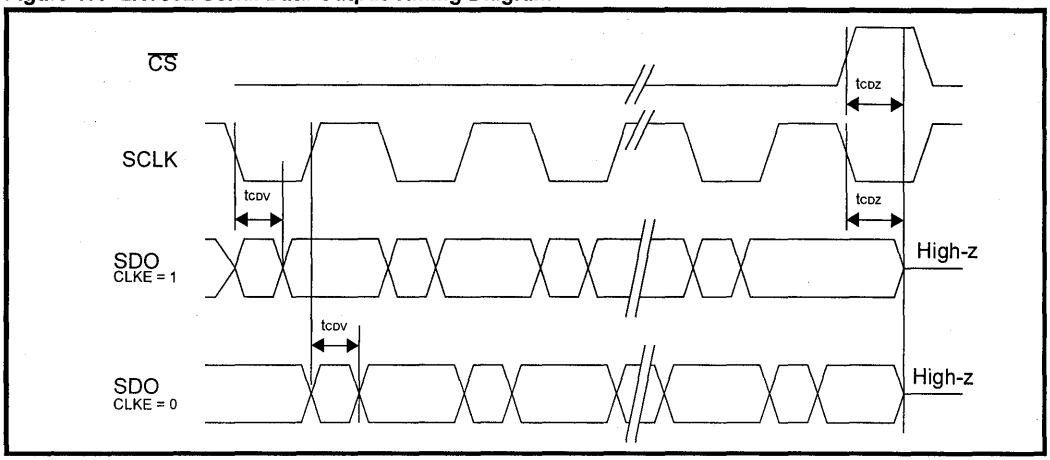


Figure 18: LXT332 Receive Clock Timing

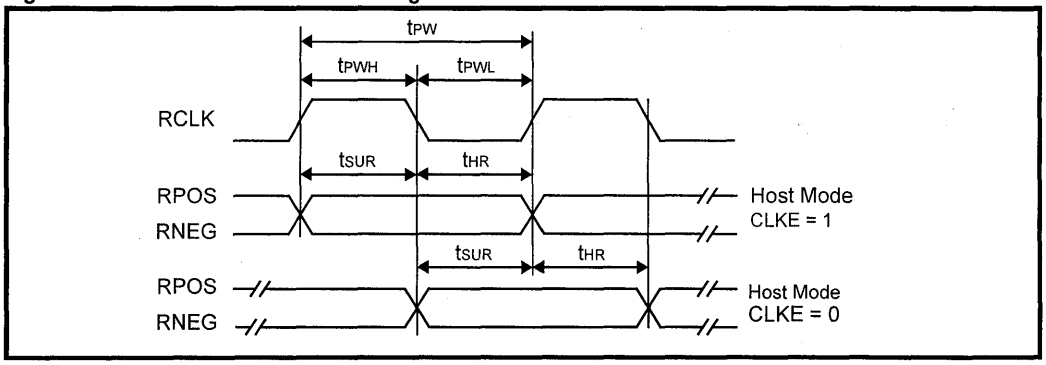


Figure 19: LXT332 Transmit Clock Timing

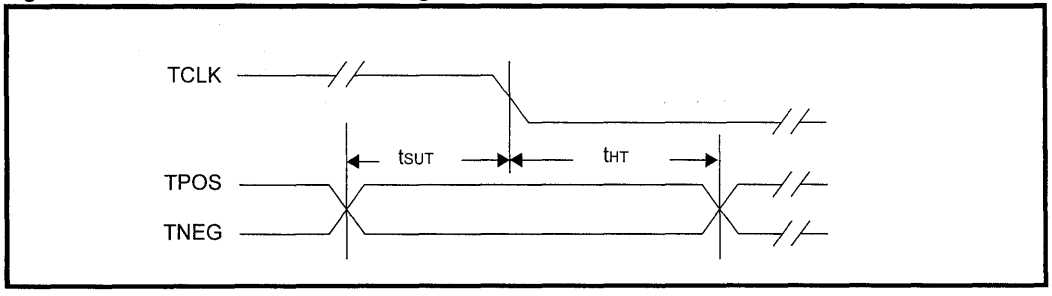


Table 16: LXT332 Receive Timing Characteristics (See Figure 18)

Parameter		Sym	Min	Typ[1]	Max	Units	Test Conditions
Receive clock period	DSX-1	tPW	583	648	713	ns	Elastic store not in overflow or underflow.
	E1	tPW	439	488	537	ns	
Receive clock duty cycle		RCLKd	40	50	60	ns	
Receive clock pulse width High	DSX-1	tPWH	259	324	389	ns	
	E1	tPWH	195	244	293	ns	
Receive clock pulse width Low	DSX-1	tPWL	259	324	389	ns	
	E1	tPWL	195	244	293	ns	
RPOS / RNEG to RCLK rising setup time	DSX-1	tSUR	50	274	–	ns	
	E1	tSUR	50	194	–	ns	
RCLK rising to RPOS / RNEG hold time	DSX-1	tHR	50	274	–	ns	
	E1	tHR	50	194	–	ns	

1 Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 17: LXT332 Master Clock and Transmit Timing Characteristics (See Figure 19)

Parameter		Sym	Min	Typ[1]	Max	Units
Master clock frequency	DSX-1	MCLK	–	1.544	–	MHz
	E1	MCLK	–	2.048	–	MHz
Master clock tolerance		MCLKt	–	±50	–	ppm
Master clock duty cycle		MCLKd	40	–	60	%
Transmit clock frequency	DSX-1	TCLK	–	1.544	–	MHz
	E1	TCLK	–	2.048	–	MHz
Transmit clock tolerance		TCLKt	–	±50	–	ppm
Transmit clock duty cycle		TCLKd	10	–	90	%
TPOS/TNEG to TCLK setup time		tSUT	50	–	–	ns
TCLK to TPOS/TNEG Hold time		tHT	50	–	–	ns

1 Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 20: Typical Receiver Input Jitter Tolerance (Loop Mode)

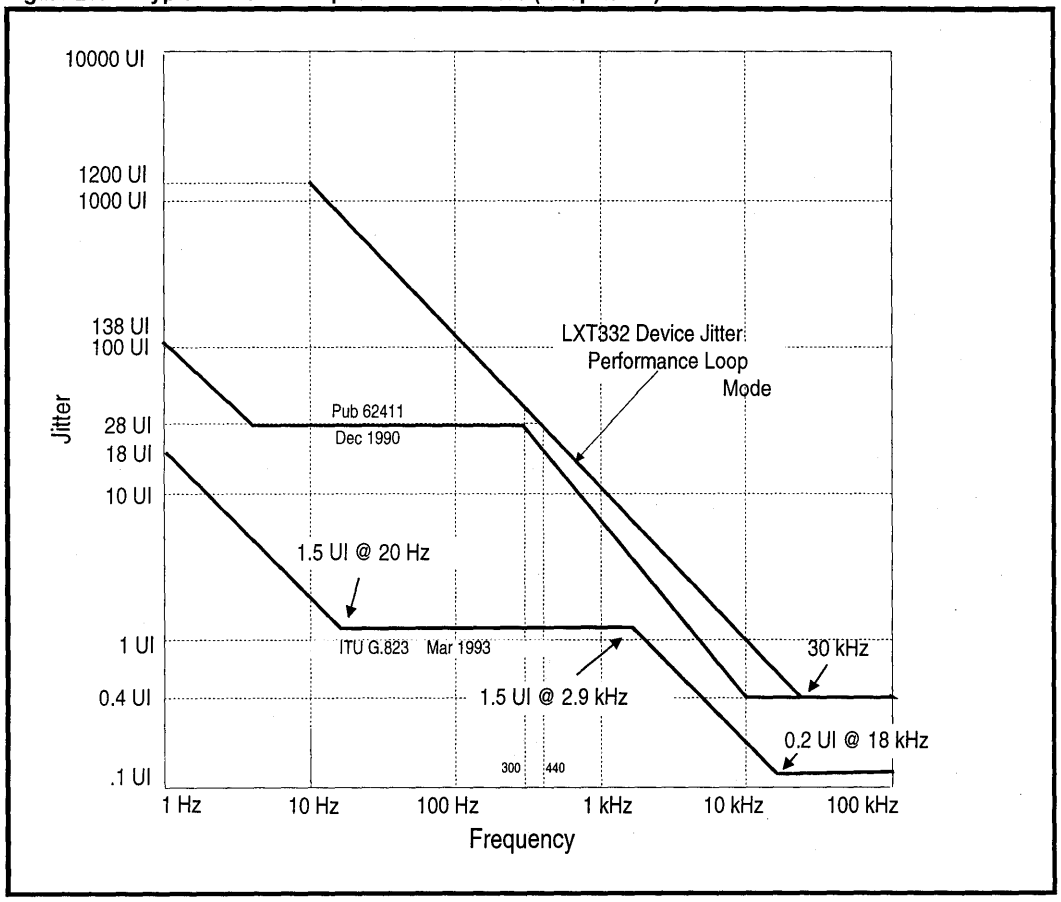
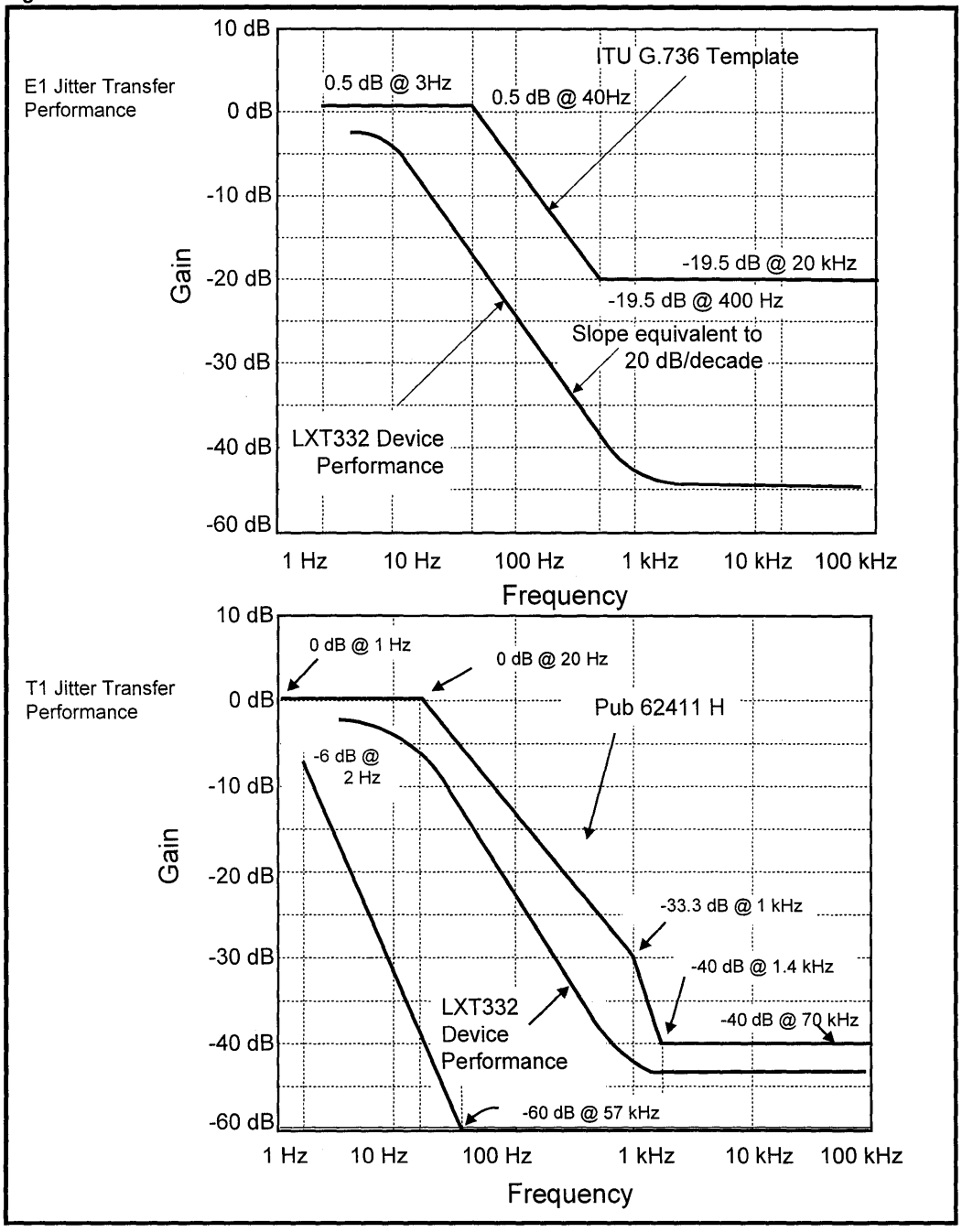


Figure 21: Jitter Transfer Performance



APPENDIX A

Data Sheet Changes

The following table lists changes that have been made to the February 1997 printing of the LXT332 data sheet. The previous version of the data sheet is dated May 1996.

Page Number	Section/Figure/Table	Change Made
12	Functional Description, Receiver subhead	For T1 applications, changed to say LEN does not equal 000 to 001
14	Functional Description, Driver Failure Monitor subhead	Removed sentences pertaining to the assertion of an interrupt line in host mode—already covered in the "Interrupt Handling" section on page 17.
19	Functional Description, Transmit All Ones subsection	Information added about how jitter attenuator affects TAOS reference clock.
20	Figure 10: Remote Loopback with Selectable JA	In second figure, changed JASEL from 1 to 0
24	Figure 15: Typical 120 Ω Application (Hardware Mode)	Swapped High Z and Unipolar switches at the bottom left corner of the figure
26	Table 14: Analog Specifications	The Typical value of data decision threshold for DSX-1 was changed from 50 to 70 % peak.
28	Figure 18: LXT332 Receive Clock Timing	New figure
29	Table 17: Master Clock and Transmit Timing Characteristics	Minimum values for TCLK setup and hold times (last two rows) changed from 25 ns to 50 ns

LXT334

Quad Short Haul Transceiver with Clock Recovery

General Description

The LXT334 is a quad, short-haul, PCM transceiver for 2.048 MHz or 1.544 MHz transmission systems. Its low impedance transmit output drivers provide constant line impedance whether transmitting marks or spaces. The output pulse amplitudes are also constant, stabilized against supply voltage variations.

The LXT334 can be configured for balanced 100/120 Ω or unbalanced 75 Ω systems and exceeds the latest ETSI return loss recommendations. An on-chip pulse shaping circuit generates accurate transmit pulses independent of the transmit clock duty cycle. All transmitters and receivers incorporate a power down mode with output tri-stating.

The LXT334 features differential receiver architecture with high noise interference margin. It uses peak detection with a variable threshold for reliable recovery of data as low as 500 mV (up to 12 dB of cable attenuation).

The receiver is programmable for transformer-coupled line interfaces. The fully digital clock recovery system uses a low frequency master clock of 2.048 MHz or 1.544 MHz as its reference. Each receiver incorporates a combination analog/digital Loss Of Signal (LOS) processor that meets the latest ITU G.775 standard. The LXT334 features a driver failure monitoring circuit in parallel to TTIP and TRING that reports driver shorts.

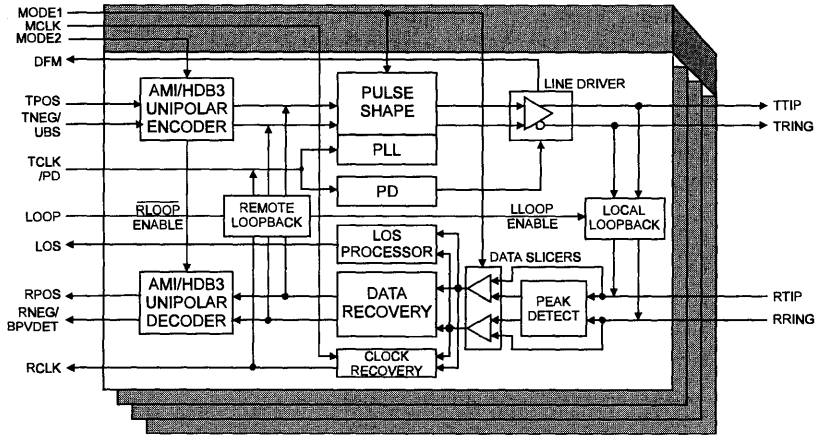
Features

- Fully integrated quad, short-haul PCM transceiver for G.703 2.048 Mbps or I.431 1.544 Mbps operation
- Single rail supply voltage of 5 V (typical)
- Low power consumption of 410 mW (typical)
- Programmable G.703 transmit pulse shaping for G.703 75 Ω and 120 Ω and I.431 100 Ω systems
- High performance line drivers with constant low impedance for 20 dB return loss (typical) exceeds ETSI 300 166
- On-chip band gap voltage reference for stabilized, constant output amplitude
- High-performance receivers recover data with up to 12 dB cable attenuation
- Low frequency 1.544 or 2.048 MHz reference clock
- On-chip clock recovery function
- Programmable unipolar and bipolar PCM interface
- On-chip AMI and HDB3 encoder/decoder
- On-chip Driver Failure Monitoring circuit
- Local and remote loopback testing function
- Independent Loss of Signal processor for each channel conforms to ITU G.775 recommendation
- Small-footprint 64-pin QFP

Applications

- High density line cards using digital backend ASICs

LXT334 Block Diagram



PIN ASSIGNMENTS & SIGNAL DESCRIPTIONS

Figure 1: LXT334 Pin Assignments

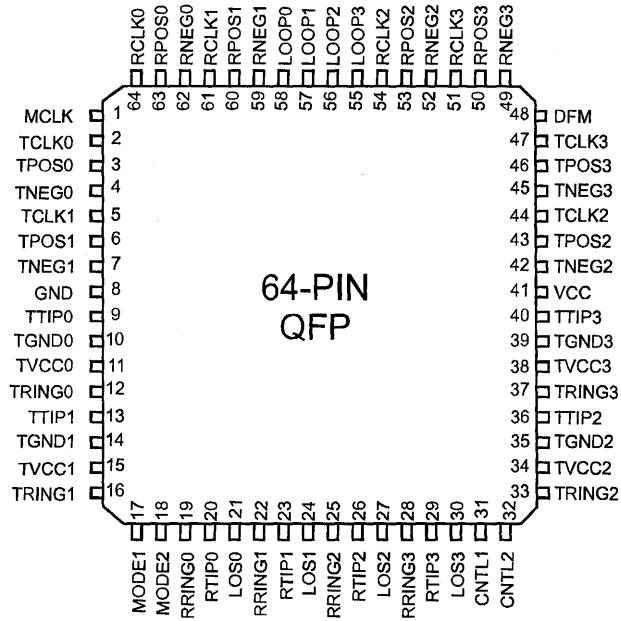


Table 1: LXT334 Pin Descriptions

Pin #	Sym	I/O[1]	Description
1	MCLK	DI	**Master Clock Input.** An independent and free-running 2.048 or 1.544 MHz clock input generates the internal reference clocks for all transceivers. On Loss of Signal (LOS), the LXT334 derives RCLKx from this master clock. With MCLK asserted High, the LXT334 disables the PLL clock recovery circuits. The transceiver then feeds RPOSx and RNEGx to an internal XOR gate that performs logically-exclusive ORs for both data signals and connects this output to RCLKx for external clock recovery. In this mode, the LXT334 operates as a data recovery circuit. With MCLK asserted Low, the LXT334 powers down its clock and data recovery circuits and switches the output pins RCLKx, RPOSx and RNEGx to tri-state mode. Driving both MCLK and TCLKx Low powers the device down. MCLK — Operating Mode Clocked — Data/Clock Recovery L — Power Down H — Data Recovery

1. Entries in I/O column are: DI = digital input; DO = digital output; DI/O = digital input/output; AI = analog input; AO = analog output; S = supply.
Note: do not leave digital inputs floating, with the exception of pins 17, 18, and 55-58.

Table 1: LXT334 Pin Descriptions – continued

Pin #	Sym	I/O[1]	Description
2	TCLK0	DI	**Transmit Clock/Transmit Power Down Input–Port 0.** All TCLKx pins are identical. The LXT334 samples TPOSx and TNEGx on the falling edge of TCLKx. With TCLKx asserted Low, the total transmit path, including the output drivers, enters a low-power, high-Z mode with all analog and digital circuitry powered down. With TCLKx asserted High for more than 16 clock cycles, the TPOSx and TNEGx duty cycles determine the transmit output pulse widths. In this mode, the LXT334 operates as a line driver. TCLKx Operating Mode Clocked Transmitter H Line Driver (or TAOS if MCLK is Clocked) L Power Down MCLK active with TCLKx High sets TAOS (Transmit All Ones) Mode.
3	TPOS0/ TDATA0	DI	**Transmit Positive Data/Transmit Data Input–Port 0.** All TPOSx/TDATAx pins are identical. In bipolar mode this pin (TPOSx) acts as active High input for the positive pulse to be transmitted. In unipolar mode this pin (TDATAx) acts as active High input for the data to be transmitted on the line.
4	TNEG0/ UBS0	DI	**Transmit Negative Data/Unipolar-Bipolar Select Input–Port 0.** All TNEGx/UBSx pins are identical. In bipolar mode, this pin acts as input for the negative pulse to be transmitted. If this pin is asserted High for more than 16 TCLK cycles, the LXT334 switches to unipolar mode. The device immediately returns to bipolar mode once this pin goes Low. UBSx Operating Mode L Bipolar Mode H Unipolar Mode
5	TCLK1	DI	**Transmit Clock/Transmit Power Down Input–Port 1.** See TCLK0, pin 2.
6	TPOS1/ TDATA1	DI	**Transmit Positive Data/Transmit Data Input–Port 1.** See TPOS0/TDATA0, pin 3.
7	TNEG1/ UBS1	DI	**Transmit Negative Data/Unipolar-Bipolar Select Input–Port 1.** See TNEG0/UBS0, pin 4.
8	GND	S	**Ground.**
9	TTIP0	AO	**Transmit Tip Output–Port 0.** All pin pairs TTIPx/TRINGx are identical. Pin pairs TTIPx/TRINGx are differential line driver outputs designed to drive 75Ω unbalanced or 100 Ω/120 Ω balanced cables using transformer coupling.
10	TGND0	S	**Transmit Ground–Port 0.** Ground return for transmit driver 0.
11	TVCC0	S	**Transmit Positive Supply–Port 0.** +5 VDC power supply input for transmit driver 0.
12	TRING0	AO	**Transmit Ring Output–Port 0.** All pin pairs TTIPx/TRINGx are identical. Pin pairs TTIPx/TRINGx are differential line driver outputs designed to drive 75 Ω unbalanced or 100 Ω/120 Ω balanced cables using transformer coupling. See TTIP0, pin 9.
13	TTIP1	AO	**Transmit Tip Output–Port 1.** See TTIP0, pin 9.

1. Entries in I/O column are: DI = digital input; DO = digital output; DI/O = digital input/output; AI = analog input; AO = analog output; S = supply.
Note: do not leave digital inputs floating, with the exception of pins 17, 18, and 55-58.

Table 1: LXT334 Pin Descriptions – continued

Pin #	Sym	I/O[1]	Description
14	TGND1	S	**Transmit Ground–Port 1.** Ground return for transmit driver 1.
15	TVCC1	S	**Transmit Positive Supply–Port 1.** +5 VDC power supply input for transmit driver 1.
16	TRING1	AO	**Transmit Ring Output–Port 1.** See TRING0, pin 12.
17	MODE1	DI	**Mode 1 Select Input.** While CNTL1 is Low, and if this pin is asserted Low, all the LXT334 drivers are configured for low power mode with a typical peak pulse output voltage of 3 V. If this pin is asserted High, the LXT334 configures its line drivers for matched line drive mode with a typical peak pulse output voltage of 4 V. Both the driver and the receivers are set to drive transformers. MODE1 Operating Mode L Low Power Mode (See Figures 3 and 6) H Matched Line Drive Mode (See Figures 4 and 5) If CNTL1 is High, MODE1 controls the load-matching circuitry in the transceiver: MODE1 Load H 75 Ω L 120 Ω
18	MODE2	DI	**Mode 2 Select Input.** If this pin is pulled Low, all transceivers operate in E1 mode using AMI encoding. With this pin pulled High, all transceivers enter E1 mode using HDB3 encoding if operated in Unipolar Mode. With this pin left open the LXT334 enters T1 mode according to Recommendation G.703. MODE2 Operating Mode L E1 Mode with AMI Encoding H E1 Mode with HDB3 Encoding Open T1 Mode with AMI Encoding
19 20	RRING0 RTIP0	AI AI	**Receive Ring Input–Port 0/Receive TIP Input–Port 0.** These pins are the inputs of the fully differential line receiver.
21	LOS0	DO	**Loss of Signal Output–Port 0.** All LOSx pins are identical. This output is High when the incoming signal has no transitions, i.e., when it is more than 22 dB below the nominal 0 dB level for more than 32 consecutive pulse intervals. The LOS condition is cleared and the output pin returns Low when the incoming signal has transitions (i.e., when the signal level is equal to or greater than 21 dB below the nominal 0 dB level and the average ones density reaches 12.5%.). In data receiver mode, LOSx is a pure analog energy detector. In case of a driver fail condition (DFM = High) this pin acts as a Driver Fail Monitor change of status output to identify the specific driver with the problem.
22 23	RRING1/ RTIP1	AI AI	**Receive Ring Input–Port 1/Receive TIP Input–Port 1.** See RRING0, pin 19; RTIP0, pin 20.
24	LOS1	DO	**Loss of Signal Output–Port 1.** See LOS0, pin 21.
25 26	RRING2/ RTIP2	AI AI	**Receive Ring Input–Port 2/Receive TIP Input–Port 2.** See RRING0, pin 19; RTIP0, pin 20.

1. Entries in I/O column are: DI = digital input; DO = digital output; DI/O = digital input/output; AI = analog input; AO = analog output; S = supply.
Note: do not leave digital inputs floating, with the exception of pins 17, 18, and 55-58.

Table 1: LXT334 Pin Descriptions – continued

Pin #	Sym	I/O[1]	Description
27	LOS2	DO	**Loss of Signal Output–Port 2.** See LOS0, pin 21.
28 29	RRING3/ RTIP3	AI AI	**Receive Ring Input–Port 3/Receive TIP Input–Port 3.** See RRING0, pin 19; RTIP0, pin 20.
30	LOS3	DO	**Loss of Signal Output–Port 3.** See LOS0, pin 21.
31 32	CNTL1 CNTL2	DI DI	**Control 1/Control 2.** Settings CNTL1 CNTL2 Result L L RPOS, RNEG valid on falling edge of RCLK L H RPOS, RNEG valid on rising edge of RCLK H L RPOS, RNEG valid on falling edge of RCLK; 120 Ω, 75 Ω load matching selected by MODE1 pin. H H *reserved–do not use this setting.*
33	TRING2	AO	**Transmit Ring Output–Port 2.** See TRING0, pin 12; TTIP0, pin 9.
34	TVCC2	S	**Transmit Power Supply–Port 2.** +5 VDC power supply input for transmit driver 2.
35	TGND2	S	**Transmit Ground–Port 2.** Ground return for transmit driver 2.
36	TTIP2	AO	**Transmit Tip Output–Port 2.** See TTIP0, pin 9.
37	TRING3	AO	**Transmit Ring Output–Port 3.** See TRING0, pin 12; TTIP0, pin 9.
38	TVCC3	S	**Transmit Power Supply–Port 3.** +5 VDC power supply input for transmit driver 3.
39	TGND3	S	**Transmit Ground–Port 3.** Ground return for transmit driver 3.
40	TTIP3	AO	**Transmit Tip Output–Port 3.** See TTIP0, pin 9.
41	VCC	S	**Positive Supply.**
42	TNEG2/ UBS2	DI	**Transmit Negative Data/Unipolar-Bipolar Select Input–Port 2.** See TNEG0/UBS0, pin 4.
43	TPOS2/ TDATA2	DI	**Transmit Positive Data/Transmit Data Input–Port 2.** See TPOS0/TDATA0, pin 3.
44	TCLK2	DI	**Transmit Clock/Transmit Power Down Input–Port 2.** See TCLK0, pin 2.
45	TNEG3/ UBS3	DI	**Transmit Negative Data/Unipolar-Bipolar Select Input–Port 3.** See TNEG0/UBS0, pin 4.
46	TPOS3/ TDATA3	DI	**Transmit Positive Data/Transmit Data Input–Port 3.** See TPOS0/TDATA0, pin 3.

1. Entries in I/O column are: DI = digital input; DO = digital output; DI/O = digital input/output; AI = analog input; AO = analog output; S = supply.
Note: do not leave digital inputs floating, with the exception of pins 17, 18, and 55-58.

Table 1: LXT334 Pin Descriptions – continued

Pin #	Sym	I/O[1]	Description
47	TCLK3	DI	**Transmit Clock/Transmit Power Down Input–Port 3.** See TCLK0, pin 2.
48	DFM	DO	**Driver Failure Monitor Output.** When High, indicates a driver short in one of the output drivers. The LOSx output identifies the specific failing driver in this case.
49	RNEG3/ BPV3	DO	**Receive Negative Data/Bipolar Violation Indication Output–Port 3.** All RNEGx/BPVx pins are identical. In bipolar mode these pins act as active High bipolar non-return-to-zero (NRZ) receive signal outputs. A High signal on RNEGx corresponds to receipt of a negative pulse on RTIPx/RRINGx. A High signal on RPOSx corresponds to receipt of a positive pulse on RTIPx/RRINGx. Both signals are valid on the same edge of RCLKx, as determined by CNTL1 and CNTL2. In unipolar mode, the LXT334 asserts the BPV*x* pin High any time it senses an In-Service Line Code violation. (*In data recovery mode, this pin is active Low.*) See RPOS3/RDATA3, pin 50; and Functional Description.
50	RPOS3/ RDATA3	DO	**Receive Positive Data/Receive Data Output–Port 3.** A High signal on RPOSx corresponds to receipt of a positive pulse on RTIPx/RRINGx. This signal is valid on the edge of RCLKx determined by CNTL1 and CNTL2. In unipolar mode (selected by pulling TNEG*x* High for more than 16 TCLK*x* periods) the LXT334 asserts RDATA*x* High when a mark has been received and is valid on the falling edge of RCLK*x*. RDATA*x* is an NRZ receive data output. (*In Data Recovery mode, this pin is active Low.*) See RNEG3/BPV3, pin 49.
51	RCLK3	DO	**Receive Clock Output–Port 3.** All RCLKx pins are identical. This pin provides the recovered clock from the signal received at RTIPx and RRINGx. In loss of signal conditions the LXT334 connects MCLK to this pin through internal circuitry. Asserting the MCLK pin High disables the clock recovery circuit and internally connects RPOS*x* and RNEG*x* to an XOR that is fed to the RCLK*x* output for external clock recovery applications.
52	RNEG2/ BPV2	DO	**Receive Negative Data/Violation Indication Output–Port 2.** See RNEG3/BPV3, pin 49; RPOS3/RDATA3, pin 50.
53	RPOS2/ RDATA2	DO	**Receive Positive Data/Receive Data Output–Port 2.** ***(In Data Recovery Mode, this signal is active Low.)*** See RPOS3/RDATA3, pin 50; RNEG3/BPV3, pin 49.
54	RCLK2	DO	**Receive Clock Output–Port 2.** See RCLK3, pin 51.

1. Entries in I/O column are: DI = digital input; DO = digital output; DI/O = digital input/output; AI = analog input; AO = analog output; S = supply.
Note: do not leave digital inputs floating, with the exception of pins 17, 18, and 55-58.

Table 1: LXT334 Pin Descriptions – continued

Pin #	Sym	I/O[1]	Description
55	LOOP3	DI	**Loopback Mode Select Input–Port 3.** All LOOPx pins are identical. Driving this pin Low selects Remote Digital Loopback which causes the LXT334 to ignore any incoming data on TPOSx and TNEGx. It then retransmits data from RTIPx and RRINGx back to TTIPx and TRINGx at the RCLKx rate. Driving this pin High selects Local Loopback which causes the LXT334 to ignore data received on RTIP*x* and RRING*x* and loop data internally from TTIP*x* and TRING*x* back around to the receive inputs. Leaving this pin open selects normal operation mode. LOOP1 Operating Mode L Remote Loopback H Local Loopback Open Normal Operation Mode
56	LOOP2	DI	**Loopback Mode Select Input–Port 2.** See LOOP3, pin 55.
57	LOOP1	DI	**Loopback Mode Select Input–Port 1.** See LOOP3, pin 55.
58	LOOP0	DI	**Loopback Mode Select Input–Port 0.** See LOOP3, pin 55.
59	RNEG1/ BPV1	DO	**Receive Negative Data/Bipolar Violation Indication Output–Port 1.** See RNEG3/BPV3, pin 49; RPOS3/RDATA3, pin 50.
60	RPOS1/ RDATA1	DO	**Receive Positive Data/Receive Data Output–Port 1.** ***(In Data Recovery Mode, this signal is active Low.)*** See RPOS3/RDATA3, pin 50; RNEG3/BPV3, pin 49.
61	RCLK1	DO	**Receive Clock Output–Port 1.** See RCLK3, pin 51.
62	RNEG0/ BPV0	DO	**Receive Negative Data/Bipolar Violation Indication Output–Port 0.** See RNEG3/ BPV3, pin 49; RPOS3/RDATA3, pin 50.
63	RPOS0/ RDATA0	DO	**Receive Positive Data/Receive Data Output–Port 0.** ***(In Data Recovery Mode, this signal is active Low.)*** See RPOS3/RDATA3, pin 50; RNEG3/BPV3, pin 49.
64	RCLK0	DO	**Receive Clock Output–Port 0.** See RCLK3, pin 51.

1. Entries in I/O column are: DI = digital input; DO = digital output; DI/O = digital input/output; AI = analog input; AO = analog output; S = supply.
Note: do not leave digital inputs floating, with the exception of pins 17, 18, and 55-58.

FUNCTIONAL DESCRIPTION

The LXT334 is a fully integrated, quad line interface unit (QLIU) with four complete, independent transceivers. It supports G.703 applications at both 2.048 Mbps and 1.544 Mbps. All transceivers operate at the same frequency, determined by the MCLK input. Refer to the LXT334 block diagram on page 1.

The front end of each transceiver interfaces with four lines, one pair for transmit, and one pair for receive. Each transmit/receive line set constitutes a digital data loop for full duplex transmission.

Each transceiver also interfaces with back-end processors through bipolar or unipolar data I/O channels, and allows control by hardwired pins for stand-alone operation.

Receiver

The four receivers in the LXT334 are identical. The following paragraphs describe the operation of a single receiver.

In Transformer Coupled Mode, the LXT334 receives the input signal at RTIP/RRING via a 1:1 transformer.

Data slicers and a peak detector process the received signal. The peak detector samples the received signal and determines its maximum value. A data-rate dependent percentage of peak value goes to the data slicers as a threshold level to ensure an optimum signal-to-noise ratio.

The receiver accurately recovers signals with up to -12 dB of cable loss. The minimum receiver sensitivity signal level is approximately 500 mV. Regardless of the received signal level, the LXT334 holds its peak detectors above a minimum level (0.225 V) to provide immunity from impulse noise.

After the data slicers process the received signal, it is fed to the data and timing recovery section, and to the receive monitor. The data and timing recovery circuits provide an input jitter tolerance significantly better than required by G.823 as shown in the Test Specifications section.

The recovered clock is output at RCLK in both bipolar and unipolar modes.

In bipolar mode, recovered data is active High and output at RPOS and RNEG; in unipolar mode recovered data is active High and output at RDATA.

If CNTL2 is Low, RPOS and RNEG outputs are valid on the falling edge of RCLK. IF CNTL1 is Low and CNTL2 is High, RPOS and RNEG outputs are valid on the rising edge of RCLK.

Asserting MCLK High disables the clock recovery function and switches all receivers to data recovery mode. In data recovery mode the RPOS/RNEG outputs are active Low. Asserting MCLK Low powers all receivers down and holds RPOS/RNEG and RCLK in a high impedance state.

Loss Of Signal Detector

LOS Detection at 2.048 MHz

During 2.048 MHz operation, the Loss of Signal (LOS) detector uses a combination analog and digital detection scheme and complies with the ITU G.775 recommendation.

The receiver monitor loads a digital counter at the RCLK frequency. The monitor increments the counter with each received 0, and resets it to 0 with each received 1 (mark). Any signal ~21 dB below the nominal 0 dB signal for 32 consecutive pulse intervals generates a LOS condition.

The LXT334 sets the LOS flag, and replaces the recovered clock with MCLK at the RCLK output in a smooth transition. (Receive operation requires MCLK.) LOS is cleared again when the signal level rises above ~21 dB (typical) below the minimum 0 dB level and the average 1s density reaches 12.5% (4 marks in a 32-bit window). Another smooth transition replaces MCLK with the recovered clock at RCLK. During LOS conditions, received data is output on RPOS/RNEG (or RDATA in unipolar I/O mode).

In data recovery mode, the LOS detector uses an analog detection scheme and complies with G.775. During LOS conditions, received data is output on RPOS/RNEG. Any signal 22 dB (typical) below the nominal 0 dB signal for more than approximately 16 µs generates a LOS condition. LOS is cleared when the signal level of the first 1 rises to more than 21 dB (typical) below the minimum 0 dB level.

LOS Detection at 1.544 MHz

During 1.544 MHz operation, the LXT334 asserts LOS if it receives 175 consecutive zeros, and deasserts LOS when the signal reaches 12.5% ones density (16 marks in a 128-bit window with no more than 99 consecutive zeros).

In-Service Code Violation Monitoring

In unipolar AMI I/O Mode, the LXT334 reports bipolar violations using an active High output for one RCLK cycle on the BPV output. A bipolar violation in AMI encoding mode is two consecutive marks of the same polarity. With the HDB3 detector enabled (pulling MODE2 High), the decoder will detect AMI code violations that are not part of a zero substitution code.

HDB3 code violations omit sequences of zeros that violate the coding rules. If an HDB3 code violation occurs, the decoder asserts the BPV output for one RCLK cycle during the period of the violating bit. In the event the decoder input receives a sequence of four or more zeros, it asserts the BPV output during the entire sequence of violating data bits.

Transmitter

The four low-power transmitters in the LXT334 are identical. The following paragraphs describe the operation of a single transmitter. The LXT334 has separate power supply (TVCC*x*/TGND*x*) for each output driver.

The LXT334 clocks transmit data from the back end serially into the device at TPOS/TNEG in the bipolar mode, or at TDATA in the unipolar mode.

The transmit clock (TCLK) supplies input synchronization. The LXT334 samples the TPOS/TNEG or TDATA input on the falling edge of TCLK. With no TCLK, the transmitter remains powered down and the TTIP/TRING outputs stay in their high-Z state.

Current limiters on the output drivers provide short circuit protection. (Refer to the Test Specifications section.) The LXT334 transmits data as a 50% AMI line code as shown in Figure 2. Pulling TCLK High with no MCLK input bypasses the transmitter PLL. In this case, TPOS and TNEG control the pulse width and polarity on TTIP and TRING.

The line driver provides a constant low output impedance of <3 Ω (typical), regardless of whether it is driving marks or spaces. This well-controlled impedance provides excellent return loss when used with external precision resistors (±1% accuracy) in series with the transformer.

The Application Information section lists recommended transformer specifications and ratios, and series resistor (Rt) values.

Transmit All Ones Mode

Pulling TCLK High for more than 16 MCLK cycles activates Transmit All Ones Mode (TAOS) Mode. In TAOS Mode, the LXT334 ignores the TPOS and TNEG inputs and transmits marks continuously at the MCLK frequency.

Pulse Shape

The LXT334 generates transmit pulse shapes internally using a high-speed PLL and digital-to-analog converters and applies them to the AMI line driver for transmission onto the line at TTIP and TRING.

Driver Failure Monitor

In the event of a short circuit on any transmit line, the Driver Failure Monitor (DFM, common to all transceivers) goes High. The LOS pin (LOS*x*) for that specific port changes its indication status to flag a driver short condition.

DFM is in parallel with TTIP and TRING. The LXT334 uses a capacitor, charged by a measure of the driver output current and discharged by a measure of the maximum allowable current, to detect driver failure.

Shorted lines draw excessive current, overcharging the capacitor. When the capacitor charge is outside the nominal charge window, the LXT334 reports a driver short circuit failure. During a long string of spaces, this short-induced overcharge eventually bleeds off, clearing the DFM flag.

Figure 2: 50% AMI Pulse Form

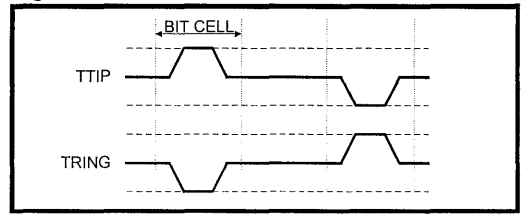


Table 2: Operating Mode Summary

MCLK	TCLK	LOOP	Receive Mode	Transmitter Mode	Loop
clocked	clocked	Open	Data/Clock Recovery	Normal	No Loopback
clocked	clocked	L	Data/Clock Recovery	Normal	Remote Loopback
clocked	clocked	H	Data/Clock Recovery	Normal	Local Loopback
L	clocked	Open	Power Down	Normal	No Loopback
L	clocked	L	Power Down	Normal	No Remote Loopback
L	clocked	H	Power Down	Normal	No Effect on Operation
L	H	Open	Power Down	Line Driver	No Loopback
L	H	L	Power Down	Line Driver	No Remote Loopback
L	H	H	Power Down	Line Driver	No Effect on Operation
L	L	X	Power Down	Power Down	No Loopback
H	clocked	Open	Data Recovery	Normal	No Loopback
H	clocked	L	Data Recovery	Line Driver	Remote Loopback
H	clocked	H	Data Recovery	Normal	Local Loopback
H	L	Open	Data Recovery	Power Down	No Loopback
H	L	L	Data Recovery	Power Down	No Effect on Operation
H	L	H	Data Recovery	Power Down	No Local Loopback
H	H	Open	Data Recovery	Line Driver	No Loopback
H	H	L	Data Recovery	Line Driver	Remote Loopback
H	H	H	Data Recovery	Line Driver	Local Loopback
clocked	L	Open	Data/Clock Recovery	Power Down	No Loopback
clocked	L	L	Data/Clock Recovery	Power Down	No Effect on Operation
clocked	L	H	Data/Clock Recovery	Power Down	No Local Loopback
clocked	H	Open	Data/Clock Recovery	Transmit All Ones	No Loopback
clocked	H	L	Data/Clock Recovery	Normal	Remote Loopback
clocked	H	H	Data/Clock Recovery	Transmit All Ones	Local Loopback

APPLICATION INFORMATION

Figure 3: E1 Low Power Tx I/F for Coax Cables

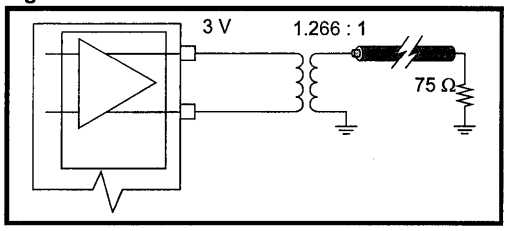


Figure 4: E1 Matched Line Tx I/F for Coax Cables for High Return Loss

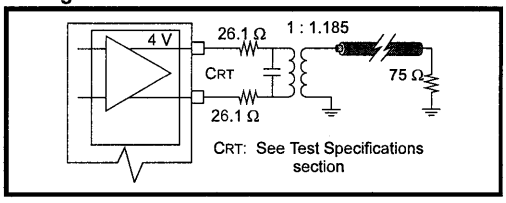


Figure 5: E1 Matched Line Tx I/F for Twisted-Pair Lines for High Return Loss

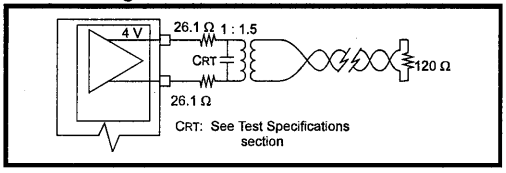


Figure 6: E1 Low Power Tx I/F for Twisted-Pair Lines

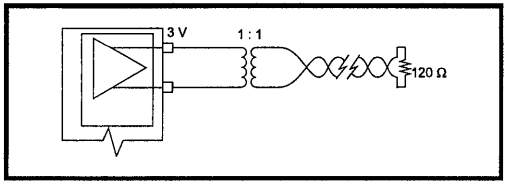


Figure 7: E1 Rx I/F for Coax Cables

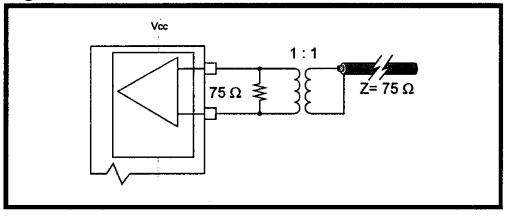


Figure 8: E1 Rx I/F for Twisted-Pair Lines

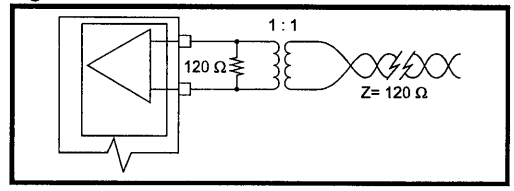


Figure 9: T1 Low Power Tx I/F for Twisted-Pair Lines

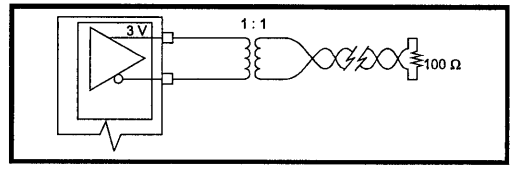


Figure 10: T1 Matched Line Tx I/F for Twisted-Pair Lines

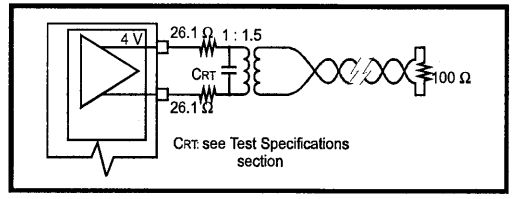


Figure 11: T1 Rx I/F for Twisted-Pair Lines

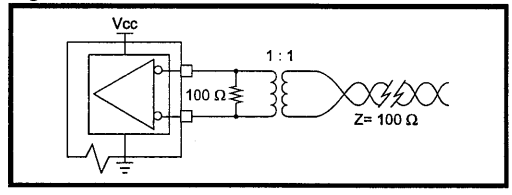


Table 3: Transformer Selection Guide[1]

Manufacturer	Transmit Side		Receive side (1:1 Ratio) (20 dB Return Loss)
	Part Number	Transformer Turns Ratio	Type
Pulse Engineering	PE-65586	1:1.36	Quad
	PE-65766	1:1.266	Dual
	PE-68789	1:1.5	Dual
	PE-65762	1:1.36	Dual
	PE-65861	1:2	Dual
	PE-65861	1:1	Dual
	PE-68789	1:1.185	Single
	PE-65389	1.266:1	Single
HALO	TG27-1505NX	1:1.36	Octal
	TD64-1205D	1:1.26	Dual
	TG29-1205NX	1:2	Octal
Bel-Fuse	0553-0013	1:1.36	Dual
	5006-1C	1:2	Dual
Schott Corp	67129300	1:2	Single

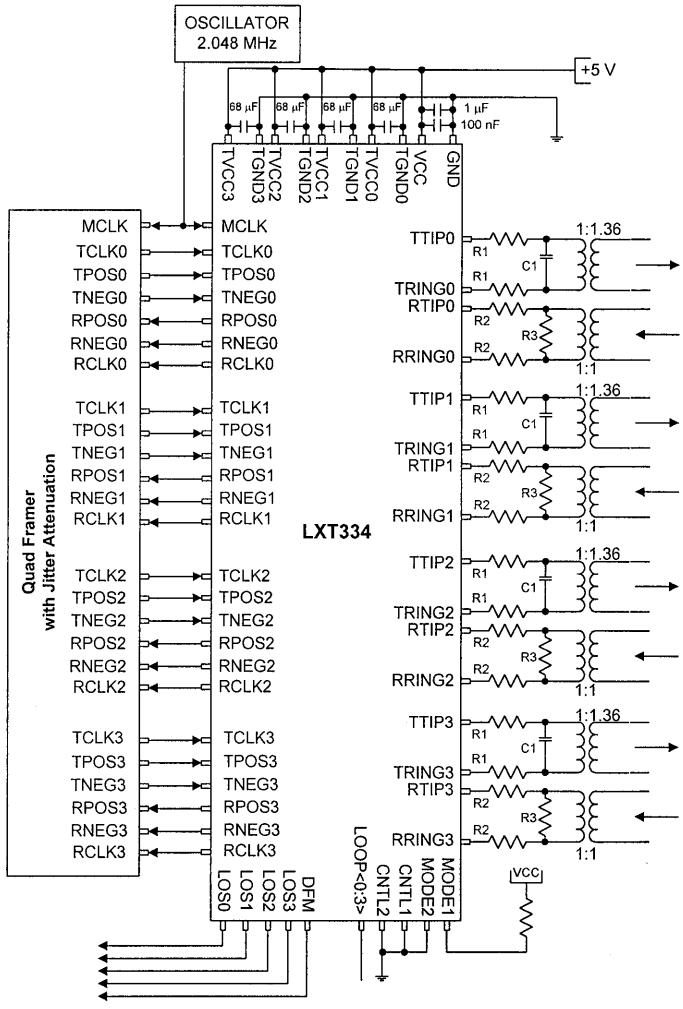
1. As of the publication date, Level One Communications, Inc., has tested the transformers listed in this table. However, part numbers and specifications change without notice. Design engineers should validate components before committing to their use.

Table 4: Transmit Transformer and Resistor Combinations

Transformer	Resistor	Return Loss[1]	CNTL1	MODE1	Impedance
1.266:1	0 Ω	< 1 dB	Low	Low	75 Ω
1:1	0 Ω	< 1 dB	Low	Low	120 Ω
1:1.185	26.1 Ω	20 dB	Low	High	75 Ω
1:1.5	26.1 Ω	20 dB	Low	High	120 Ω
1:1.36	25 Ω	18 dB	Low	High	75 Ω
1:1.36	25 Ω	18 dB	Low	High	120 Ω
1:2	15 Ω	≥ 8 dB	High	High	75 Ω
1:2	15 Ω	≥ 8 dB	High	Low	120 Ω

1. Typical values 51 kHz - 3.078 MHz

Figure 12: E1 120 Ω and 75 Ω Matched Line Applications



Component	Application	
	120 Ω	**75 Ω**
R1. Transmit resistor	25 Ω	25 Ω
R2. Receive resistor	1 kΩ	1 kΩ
R3. Receive terminating resistor	120 Ω	75 Ω
C1. Transmit capacitor (typical)	180 pF	180 pF

TEST SPECIFICATIONS

NOTE

The minimum and maximum values in Tables 5 through 14 and Figures 13 through 18 represent the performance specifications of the LXT334 and are guaranteed by test except, where noted, by design or other correlation methods.

Table 5: Absolute Maximum Ratings

Parameter	Sym	Min	Max	Unit
DC supply voltage	RVCC, RGND	-0.3	6.0	V
Input voltage on any pin[1]	VIN	GND -0.3	RVCC + 0.3	V
Input voltage on RTIP/RRING	VIN	-6	RVCC + 0.3	V
Transient latchup current on any pin[2]	IIN	–	100	mA
Input current on any digital pin[3]	IIN	-10	10	mA
DC input current on TTIP, TRING[3]	IIN	–	±100	mA
DC input current on RTIP, RRING[3]	IIN	–	±20	mA
Storage temperature	TSTOR	-65	+150	°C
Total package power dissipation	–	–	1	W

CAUTION

Exceeding these values may cause permanent damage to the device. Operation is not guaranteed under these conditions. Exposure to absolute maximum rating conditions for extended periods may adversely affect device reliability.

1. Referenced to ground.
2. Exceeding these values will cause SCR latch-up.
3. Constant input current.

Table 6: Recommended Operating Conditions

Parameter	Sym	Min	Typ	Max	Unit	Test Condition
DC supply voltage[1]	V+	4.75	5.0	5.25	V	
Ambient operating temperature	TA	-40	25	+85	° C	

1. TVcc must not differ from RVCC by more than ± 0.3 V.

Table 7: DC Characteristics (over recommended range)

Parameter		Sym	Min	Typ[1]	Max	Unit	Test Condition
Digital I/O pins	High level input voltage	VIH	2.0	–	–	V	
	Low level input voltage	VIL	—	–	0.8	V	
	High level output voltage[2]	VOH	3.5	–	–	V	IOUT= -400µA
	Low level output voltage[2]	VOL	—	–	0.4	V	IOUT= 1.6 mA
Input leakage current (digital input pins)		IIL	-10	–	+10	µA	
Tristate leakage current[5]		IHZ	-10		+10	µA	
Driver short circuit current	E1	–	–	–	50	mA	See Figures 4 and 5
	T1	–	–	–	150	mA	See Figure 9
MODE input pins	Low level input voltage	VINL	–	–	1.5	V	pins 17, 18, 55, 56, 57, 58
	High level input voltage	VINH	3.5	–	–	V	
	Midrange input voltage	VINM	2.3	2.5	2.7	V	
	Low level input current	IINL	–	–	50	µA	
	High level input current	IINH	–	–	50	µA	
Total power dissipation [3]	75 Ω system (MODE1=H)	PD	–	660	750	mW	Figure 4
	120 Ω system (MODE1=H)	PD	–	660	750	mW	Figure 5
	100 Ω system (MODE1=H; MODE2=Open)	–	–	680	895	mW	Figure 10
Total power dissipation[4]	75 Ω system (MODE1=L)	PD	–	410	470	mW	Figure 3
	120 Ω system (MODE1=L)	PD	–	410	470	mW	Figure 6
	100 Ω system (MODE1=L; MODE2=Open)	–	–	370	500	mW	Figure 9
Power down current		ICCO	–	–	10	mA	

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Output Drivers will output CMOS logic levels into CMOS loads.
3. 100% 1s density. Power dissipation including device load while driving a matched line over the operating temperature range. Digital inputs are within 10% of the supply rails and digital outputs are driving a 50 pF load.
4. 50% 1s density. Power dissipation including device load while driving a line without matching resistors over the operating temperature range. Digital inputs are within 10% of the supply rails and digital outputs are driving a 50 pF load.
5. Applies to the following pins: 9, 12, 13, 16, 33, 36, 37, 40, 49-54, 59-64.

Table 8: 2.048 MHz Transmit Characteristics in Transformer Coupling Mode
(over recommended range)

Parameter		Sym	Min	Typ[1]	Max	Unit	Test Condition
Output pulse amplitude	75 Ω	–	2.13	2.37	2.61	V	Tested at the line side.
	120 Ω	–	2.7	3.0	3.3	V	Tested at the line side.
Peak voltage of a space	75 Ω	–	-0.237	0	0.237	V	
	120 Ω	–	-0.3	0	0.3	V	
Positive to negative pulse imbalance		–	0.95	–	1.05	–	
Transmit amplitude variation with supply		–	–	1	–	%	
Driver output impedance[4]		–	–	3	–	Ω	
Difference between pulse sequences[2, 4]		–	–	–	200	mV	
Transmit output jitter	20 Hz to 100 kHz[3]	–	–	–	0.04	U.I.	peak to peak
Output jitter in loopback mode[4]	20 Hz to 100 kHz	–	–	–	0.09	U.I.	peak to peak
Pulse width ratio of the positive and negative pulses		–	0.95	–	1.05	–	At the nominal half amplitude.
Transmit return loss[4]	51 kHz to 102 kHz	–	20	–	–	dB	See Application Information, Figures 4, 5.
	102 kHz to 2.048 MHz	–	20	–	–	dB	
	2.048 MHz to 3.072 MHz	–	20	–	–	dB	
Transmit load capacitance		CRT	–	180	–	pF	

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Per ITU I.431 recommendation (4.1.2.3.) for a window of 17 consecutive bits.
3. With no jitter at the input used for synchronization or when using an externally supplied jitter free master clock the peak to peak jitter will not exceed the specified value.
4. Guaranteed by design and other correlation methods.

Table 9: 1.544 MHz Transmit Characteristics (over recommended range)

Parameter		Sym	Min	Typ[1]	Max	Unit	Test Condition
Output pulse amplitude		–	2.4	3.0	3.6	V	Z_L = 100 Ω.
Peak voltage of a space		–	-0.15	0	0.15	V	Z_L = 100 Ω.
Transmit amplitude variation with supply		–	–	1	–	%	
Driver output impedance[4]		–	–	3	–	Ω	
Positive to negative pulse imbalance		–	–	–	0.5	dB	
Transmit output jitter [2]	10 Hz to 8 kHz[4]	–	–	–	0.02	U.I	peak to peak
	8 kHz to 40 kHz[4]	–	–	–	0.025	U.I.	
	10 Hz to 40 kHz[4]	–	–	–	0.025	U.I.	
	Broad Band	–	–	–	0.05	U.I.	
Output power level	772 kHz[3, 4]	–	12	–	19	dB	
Output power	1544 kHz relative to power at 772 kHz[4]	–	-29	–	–	dB	
Ratio of the pulse widths of the positive and negative pulses at the nominal half amplitude		–	0.95	–	1.05	–	
Transmit return loss [4]	51 kHz to 102 kHz	–	18	–	–	dB	See Applications Information section Figure 10.
	102 kHz to 2.048 MHz	–	18	–	–	dB	
	2.048 MHz to 3.072 MHz	–	18	–	–	dB	
Transmit load capacitance		CRT	–	180	–	pF	

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. With no jitter at the input used for synchronization or when using an externally supplied jitter free master clock the peak to peak jitter will not exceed the specified value.
3. The signal level is the power level measured in a 3 kHz bandwidth at the point where the signal arrives at the distribution frame for an all 1s pattern transmitted.
4. Guaranteed by design and other correlation methods.

Table 10: 2.048 MHz Receive Characteristics (over recommended range)

Parameter		Sym	Min	Typ[1]	Max	Unit	Test Condition
Permissible cable attenuation[2]		–	–	–	12	dB	@1024 kHz
Receiver dynamic range		DR	0.5	–	4.2	Vp	
Signal to noise interference margin [2, 6]		S/I	15	–	–	dB	Per G.703, O.151, 6 dB of cable.
Signal to single tone interference margin		S/X	14	–	–	dB	O.151, 6 dB of cable
Data decision threshold		SRE	43	50	57	%	Relative to peak input voltage.
Analog loss of signal threshold		–	–	225[5]	–	mV	
Loss of signal threshold hysteresis		–	–	2.5	–	dB	
Consecutive zeros before loss of signal		–	–	32	–		G.775 recommendation
Low limit input jitter tolerance [3]	1.2E-5 Hz to 20 Hz[6]	–	36	–	–	U.I.	G.735 recommendation See Note 1.
	20 Hz to 2.4 kHz[4]	–	1.5	–	–	U.I.	
	8 kHz to 100 kHz	–	0.2	–	–	U.I.	
RCLK output jitter[4, 6]	0 Hz to100 kHz	–	–	0.01	–	U.I.	peak to peak
Clock recovery PLL 3 dB bandwidth		–	–	10	–	kHz	
PLL peaking[6]		–	–	–	0	dB	
Receiver input impedance		–	–	40	–	kΩ	@1024 kHz RTIP to RRING
Receiver return loss[6]	51 kHz–102 kHz	–	20	–	–	dB	See Application Information section, Figures 7, 8.
	102–2048 kHz	–	20	–	–	dB	
	2048 kHz–3072 kHz	–	20	–	–	dB	

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. No errors shall occur when the combined signal attenuated by the maximum specified interconnecting cable loss is applied to the input port. See ITU O.151 recommendation for further details.
3. Sine wave jitter and wander with a peak to peak amplitude that corresponds at least to what is specified in Figure 17 shall not cause either a bit error or loss of frame alignment. As test signal an HDB3-coded digital signal with an electrical characteristic that complies with what is set forth in ITU G.703 shall be used. Test sequence is pseudo-random 2^{15}-1. See also ITU O.151.
4. If the LXT334 is configured as data receiver only and if a jitter free signal is applied to RTIP and RRING the added jitter must not exceed the specified value.
5. Equal to 22 dB below the nominal 0 dB level in 120 Ω systems.
6. Guaranteed by design and other correlation methods.

Table 11: 1.544 MHz Receive Characteristics (over recommended range)

Parameter		Sym	Min	Typ[1]	Max	Unit	Test Condition
Permissible cable attenuation		–	–	–	12	dB	@772 kHz
Receiver dynamic range		DR	0.5	–	4.2	Vp	
Undershoot		US	–	–	62	%	
Data decision threshold		SRT	63	70	77	%	Relative to peak input voltage.
Loss of signal threshold		–	–	0.225	–	V	
Allowable consecutive 0s before LOS		–	–	175	–		
Low limit input jitter tolerance	18 kHz to 100 kHz	–	0.430	–	–	U.I.	C.735 recommendation
Clock recovery PLL 3 dB bandwidth		–	–	10	–	kHz	
PLL peaking[2]		–	–	–	0	dB	
Receiver input impedance		–	–	40	–	kΩ	RTIP to RRING @ 772 kHz
Input return loss[2]	51 kHz–102 kHz	–	20	–	–	dB	See Application Information section, Figure 11.
	102–2048 kHz	–	20	–	–	dB	
	2048 kHz–3072 kHz	–	20	–	–	dB	

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Guaranteed by design and other correlation methods.

Table 12: Transmit Timing Characteristics (over recommended range)

Parameter		Sym	Min	Typ[1]	Max	Units	Test Condition
Master clock frequency	E1	MCLK	–	2.048	–	MHz	
	T1	MCLK	–	1.544	–	MHz	
Master clock tolerance		MCLKt	–	±50	–	ppm	
Master clock duty cycle		–	40	–	60	%	
Output pulse width	E1	tPW	219	244	269	ns	
	T1	tPW	274	324	374	ns	
Transmit clock frequency	E1	TCLK	–	2.048	–	MHz	
	T1	TCLK	–	1.544	–	MHz	
Transmit clock tolerance		TCLKt	–	±50	–	ppm	
Transmit clock duty cycle		TCLKd	10	–	90	%	Normal mode
TPOS/TNEG duty cycle		TPNd	48.4	–	51.6	%	Line driver mode
TPOS/TNEG to TCLK setup time		tSUT	25	–	–	ns	
TCLK to TPOS/TNEG hold time		tHT	25	–	–	ns	

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 13: LXT334 Transmit Timing Diagram

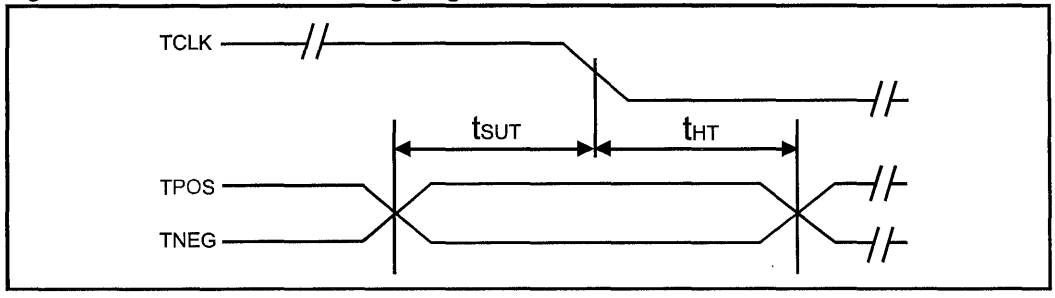


Table 13: Receive Timing Characteristics (over recommended range)

Parameter		Sym	Min	Typ[1]	Max	Unit	Test Condition
Receive clock capture range		–	–	±80	–	ppm	
Receive clock duty cycle [2]		RLCKd	40	50	60	%	
Receive clock pulse width [2]	E1	tPW	447	488	529	ns	
	T1	tPW	594	648	702	ns	
Receive clock pulse width low time	E1	tPWL	203	244	285	ns	
	T1	tPWL	270	324	378	ns	
Receive clock pulse width high time	E1	tPWH	–	244	–	ns	
	T1	tPWH	–	324	–	ns	
RPOS/RNEG data low time (MCLK=H) [3,4]		tPWD1	200	244	300	ns	
RPOS/RNEG to RCLK rising setup time	E1	tSUR	50	203	–	ns	
	T1	tSUR	50	270	–	ns	
RCLK rising to RPOS/RNEG hold time	E1	tHR	50	203	–	ns	
	T1	tHR	50	270	–	ns	
Delay time between RPOS/RNEG and RCLK		–	–	5	–	ns	MCLK = H

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. RCLK duty cycle will vary depending on extent of received pulse jitter displacement. Maximum and minimum RCLK duty cycles are for worst case jitter conditions (0.2 U.I. displacement for E1 and 0.4 U.I. for T1 operation).
3. This mode disables clock recovery.
4. If MCLK is High, the PLL clock recovery circuits are disabled. RPOSx and RNEGx are fed to an internal XOR gate that connects this output to RCLKx for external clock recovery.

Figure 14: LXT334 Receive Timing Diagram

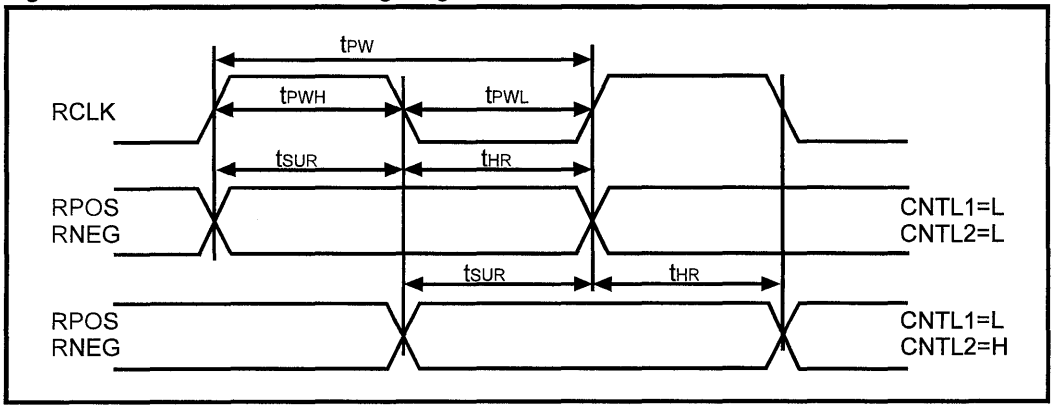


Figure 15: 2.048 MHz Pulse Mask G.703

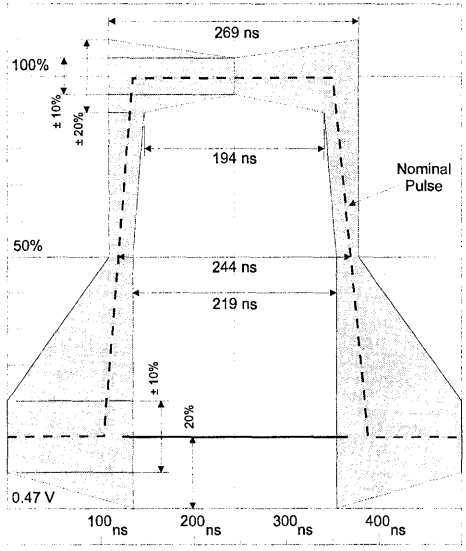


Figure 16: 1.544 MHz Pulse Mask I.431

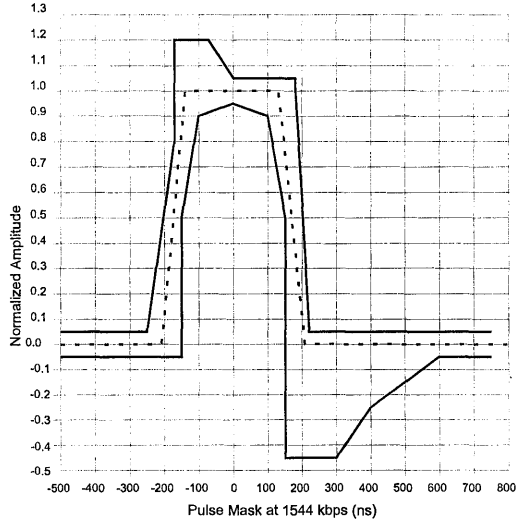


Figure 17: Jitter Tolerance—G.823

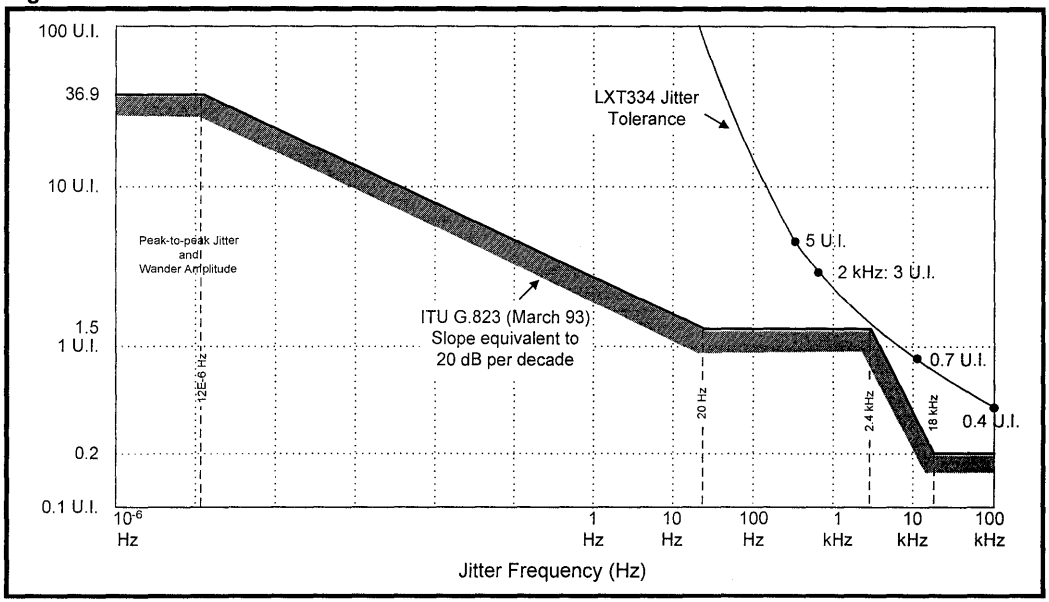


Figure 18: Jitter Attenuation—G.735

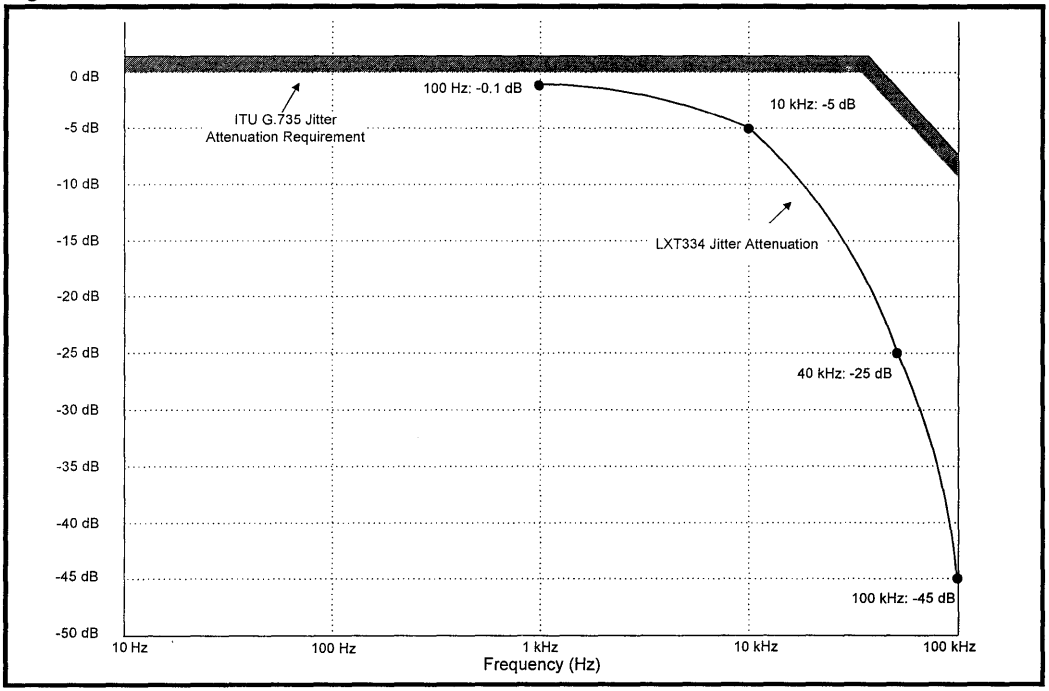


Table 14: Relevant Recommendations

Recommendation	Description
ITU	
G.703	Physical/electrical characteristics of hierarchical digital interfaces
G.704	Functional characteristics of interfaces associated with network nodes
G.735	Characteristics of Primary PCM multiple equipment operating at 2048 kbit/s and offering digital access at 384 kbit/s and/or synchronous digital access at 64 kbit/s
G.736	Characteristics of a synchronous digital multiplex equipment operating at 2048 kbit/s
G.775	Loss of signal (LOS) and alarm indication (AIS) defect detection and clearance criteria
G.823	The control of jitter and wander within digital networks which are based on the 2048 kbit/s hierarchy
O.151	Specification of instruments to measure error performance in digital systems
I.431	ISDN Primary Rate: user netework interface layer 1 specification
ETSI	
ETS 300 166	Transmission and Multiplexing (TM); Physical and electrical characteristics of hierarchical digital interfaces for equipment using the 2.048 kbp/s-based plesiochronous or synchronous digital hierarchies

SEPTEMBER 97
Revision 0.1

LXT335

Quad Short Haul PCM Analog Interface

General Description

The LXT335 is a quad, short-haul, PCM analog line interface for 2.048 Mhz transmission systems. It includes four independent data receivers and four independent line drivers in a single, 64-pin QFP package. Its low impedance transmit output drivers provide constant line impedance whether transmitting marks or spaces. The output pulse amplitudes are also constant, and are stabilized against supply voltage variations. The LXT335 is configurable for either balanced 120 Ω or unbalanced 75 Ω systems and exceeds latest ETSI return loss recommendations. .All transmitters incorporate a power down mode with output tri-stating.

The LXT335 features a differential receiver architecture with high noise interference margin. It uses peak detection with a variable threshold for reliable data recovery as low as 500 mV (up to 12 dB of cable attenuation). Each receiver incorporates an analog loss of signal (LOS) detector that meets latest ITU standards. The LXT335 features a driver failure monitoring circuit in parallel to TTIP and TRING that reports driver shorts.

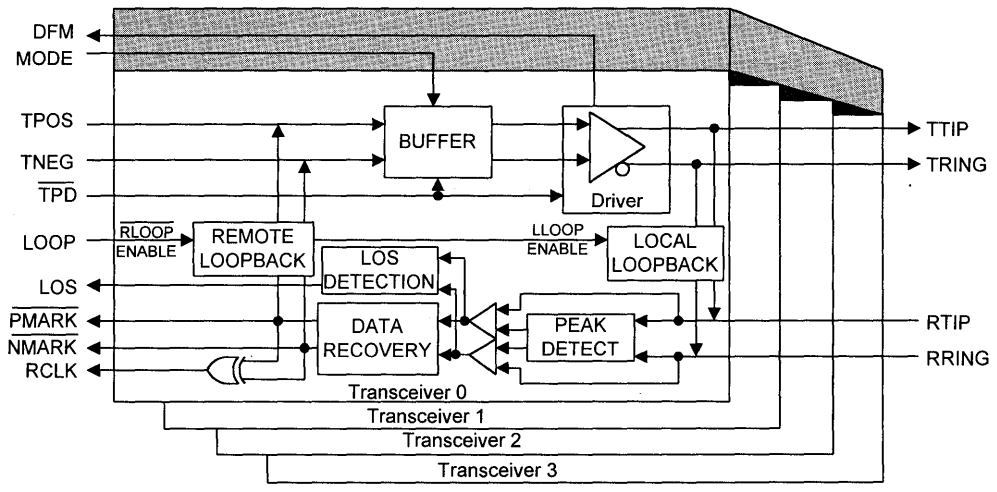
Applications

- High-density E1 line interface cards using digital backend ASICS
- Multiplexers, digital crossconnects, SDH systems

Features

- Quad E1 short haul PCM analog front-end per ITU G.703
- Single rail supply voltage of 5 V (typical)
- Low power consumption of 410 mW (typical)
- Four independent high-performance line drivers with constant low impedance for typical 20 db return loss
- Voltage stabilized output amplitudes
- Four high performance line receivers with 14 db, single tone interference margin
- Data recovery for cable attenuation of up to 12 db at 1024 khz
- On-chip driver short circuit monitoring function
- Local and remote loopback testing function
- Small footprint 64-pin QFP package

LXT335 Block Diagram



PIN ASSIGNMENTS AND SIGNAL DESCRIPTIONS

Figure 1: LXT335 (QE) Pinout Diagram

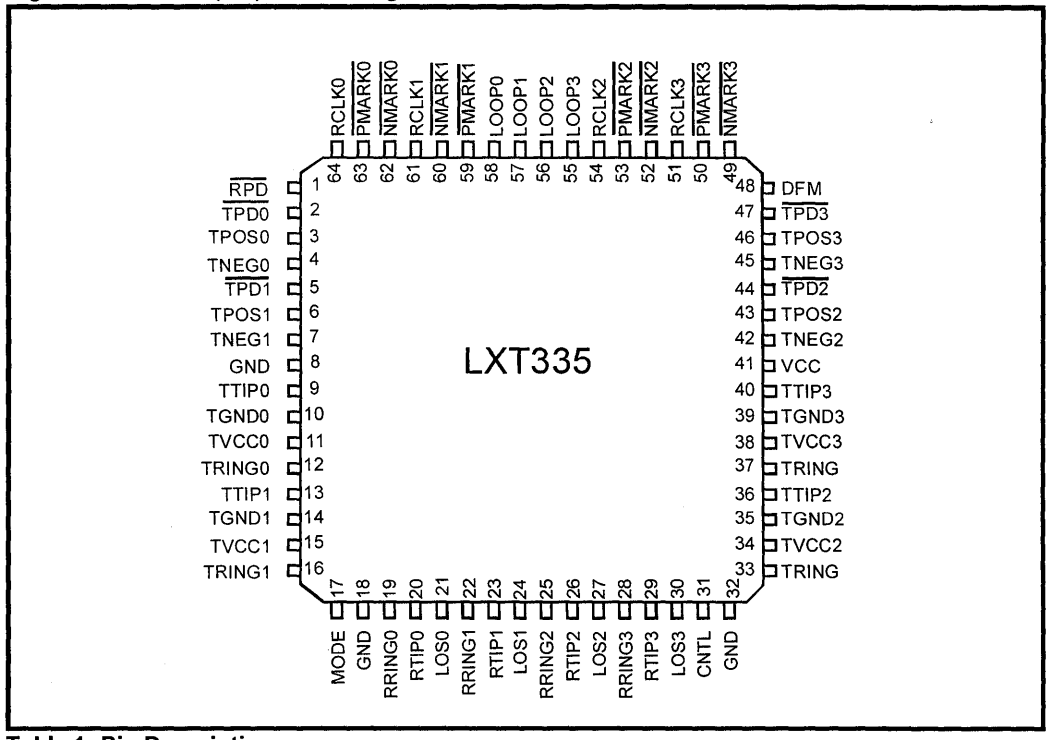


Table 1: Pin Descriptions

Pin #	Sym	I/O[1]	Description
1	$\overline{\text{RPD}}$	DI	**Receive Power Down.** When this pin is asserted Low, LXT335 powers down all four receivers and switches the receiver output pins $\overline{\text{PMARK}}$, $\overline{\text{NMARK}}$ and RCLK to tri-state mode.
2	$\overline{\text{TPD0}}$	DI	**Transmit Power Down Input–Port 0.** All TPD*x* pins are identical. With TPD asserted Low, the transmit drivers enter a low-power, High-Z mode with all analog and digital circuitry powered down. TPD — Operating Mode H — Normal Operation Mode L — Power Down Transmitter

1. Entries in I/O column are DI = Digital Input; DO = Digital Output; DIO = Digital Input Output; AI = Analog Input; AO = Analog Output; High Z = high impedance input/output; S = power/ground pins

Table 1: Pin Descriptions – continued

Pin #	Sym	I/O[1]	Description
3	TPOS0	DI	**Transmit Positive Data-Port 0.**
4	TNEG0	DI	**Transmit Negative Data-Port 0.** All TPOS*x*/TNEG*x* pins are identical. These pins act as active High RZ data inputs for the positive and negative pulse to be transmitted to the line. The transmit pulse width is determined by the duty cycle of TPOS and TNEG.
5	$\overline{\text{TPD1}}$	DI	**Transmit Power Down Input–Port 1.** See $\overline{\text{TPD0}}$, pin 2.
6	TPOS1	DI	**Transmit Positive Data–Port 1.**
7	TNEG1	DI	**Transmit Negative Data–Port 1.** See TPOS0/TNEG0, pins 3 and 4.
8	GND	S	**Ground.**
9	TTIP0	AO	**Transmit Tip Output–Port 0.** All TTIP*x* pins are identical. The TTIP0/TRING0 pins are the differential line driver outputs of transceiver 0.
10	TGND0	S	**Transmit Ground-Port 0.**
11	TVCC0	S	**Transmit Positive Supply–Port 0.**
12	TRING0	AO	**Transmit Ring Output–Port 0.** All TRING*x* are identical. The TTIP0/TRING0 pins are the differential line driver outputs of transceiver 0.
13	TTIP1	AO	**Transmit Tip Output–Port 1.** See TTIP0, pin 9.
14	TGND1	S	**Transmit Ground-Port 1.**
15	TVCC1	S	**Transmit Positive Supply–Port 1.**
16	TRING1	AO	**Transmit Ring Output–Port 1.** See TRING0, pin 12.
17	MODE	DI	**Mode Select Input.** If this pin is asserted Low all LXT335 drivers are configured for low power unmatched line drive mode. If this pin is asserted High all LXT335 line drivers are configured for matched line drive mode. MODE — Operating Mode L — Unmatched Line Drive Mode H — Matched Line Drive Mode
18	GND	S	**Ground.**

1. Entries in I/O column are DI = Digital Input; DO = Digital Output; DIO = Digital Input Output; AI = Analog Input; AO = Analog Output; High Z = high impedance input/output; S = power/ground pins

Table 1: Pin Descriptions – continued

Pin #	Sym	I/O[1]	Description
19 20	RRING0 RTIP0	AI AI	**Receive Ring Input–Port 0.** **Receive Tip Input–Port 0.** All RTIP*x*/RRING*x* pins are identical. These pins are the inputs of the fully differential line receiver.
21	LOS0	DO High Z	**Loss of Signal Output–Port 0.** All LOS*x* pins are identical. This output is asserted High when the incoming signal is more than 22 dB below the nominal 0 dB level. The LOS condition is cleared and the output is deasserted if the incoming signal is equal to or greater than 21 dB below the nominal 0 dB level. During a driver fail condition this pin acts as driver 0 fail monitor output.
22 23	RRING1/ RTIP1	AI AI	**Receive Ring Input–Port 1.** **Receive TIP Input–Port 1.** See RTIP0/RRING0, pins 19 and 20.
24	LOS1	DO	**Loss of Signal Output–Port 1.** See LOS0, pin 21.
25 26	RRING2/ RTIP2	AI AI	**Receive Ring Input–Port 2.** **Receive TIP Input–Port 2.** See RTIP0/RRING0, pins 19 and 20.
27	LOS2	DO	**Loss of Signal Output–Port 2.** See LOS0, pin 21.
28 29	RRING3/ RTIP3	AI AI	**Receive Ring Input–Port 3.** **Receive TIP Input–Port 3.** See RTIP0/RRING0, pins 19 and 20.
30	LOS3	DO	**Loss of Signal Output–Port 3.** See LOS0, pin 21.
31	CNTL	DI	**Pulse Amplitude Control Input.** If this pin is asserted High the transmitter operation mode is pin selectable via MODE between 75 and 120 Ohm without changing external components. If this pin is asserted Low the line driver operation modes may be selected via MODE. CNTL MODE Result L L Unmatched Line Driver Mode L H Matched Line Driver Mode H L Pin Selectable Driver Mode (120 Ω) H H Pin Selectable Driver Mode (75 Ω)
32	GND	S	**Ground.**

1. Entries in I/O column are DI = Digital Input; DO = Digital Output; DIO = Digital Input Output; AI = Analog Input; AO = Analog Output; High Z = high impedance input/output; S = power/ground pins

Table 1: Pin Descriptions – continued

Pin #	Sym	I/O[1]	Description
33	TRING2	AO	**Transmit Ring Output–Port 2.** See TRING0, pin 12.
34	TVCC2	S	**Transmit Power Supply-Port 2.**
35	TGND2	S	**Transmit Ground-Port 2.**
36	TTIP2	AO	**Transmit Tip Output–Port 2.** See TTIP0, pin 9.
37	TRING3	AO	**Transmit Ring Output–Port 3.** See TRING0, pin 12.
38	TVCC3	S	**Transmit Power Supply-Port 3.**
39	TGND3	S	**Transmit Ground-Port 3**
40	TTIP3	AO	**Transmit Tip Output–Port 3** See TTIP0, pin 9.
41	VCC	S	**Receiver Positive Supply.**
42	TNEG2	DI	**Transmit Negative Data Input–Port 2.** **Transmit Positive Data Input–Port 2.** See TPOS0/TNEG0, pins 3 and 4.
43	TPOS2	DI	
44	$\overline{\text{TPD2}}$	DI	**Transmit Power Down Input–Port 2.** See $\overline{\text{TPD0}}$, pin 2.
45	TNEG3	DI	**Transmit Negative Data Input–Port 3.** **Transmit Positive Data Input–Port 3.** See TPOS0/TNEG0, pins 3 and 4.
46	TPOS3	DI	
47	$\overline{\text{TPD3}}$	DI	**Transmit Power Down Input–Port 3.** See $\overline{\text{TPD0}}$, pin 2.
48	DFM	DO	**Driver Failure Monitor Output.** When this pin is High it indicates that a driver short has been detected in one of the four drivers. The transceiver LOS*x* output identifies the specific failing driver in this case.
49	$\overline{\text{NMARK3}}$	DO	**Receive Negative Data Output–Port 3.** **Receive Positive Data Output–Port 3.** All $\overline{\text{NMARKx}}$/$\overline{\text{PMARKx}}$ pins are identical. These pins act as active Low bipolar return-to-zero (RZ) receive data outputs. A Low on an $\overline{\text{NMARKx}}$ pin corresponds to a receipt of a positive pulse on RRING. A Low on a $\overline{\text{PMARKx}}$ pin corresponds to a receipt of a positive pulse on RTIP.
50	$\overline{\text{PMARK3}}$	DO	

1. Entries in I/O column are DI = Digital Input; DO = Digital Output; DIO = Digital Input Output; AI = Analog Input; AO = Analog Output; High Z = high impedance input/output; S = power/ground pins

Table 1: Pin Descriptions – continued

Pin #	Sym	I/O[1]	Description
51	RCLK3	DO	**Receive Clock Output–Port 3.** All RCLK*x* pins are identical. This pin provides a timing signal from the received data at RTIP and RRING. $\overline{\text{PMARK3}}$ and $\overline{\text{NMARK3}}$ are internally connected to an XOR gate. The output of this gate goes to the RCLK3 output for external clock recovery applications.
52	$\overline{\text{NMARK2}}$	DO	**Receive Negative Data Output–Port 2.** **Receive Positive Data–Port 2.** SEE $\overline{\text{NMARK3}}$/$\overline{\text{PMARK3}}$, pins 49, 50.
53	$\overline{\text{PMARK2}}$	DO	
54	RCLK2	DO	**Receive Clock Output–Port 2** See RCLK3, pin 51.
55	LOOP3	DI	**Loopback Mode Select Input–Port 3.** **Loopback Mode Select Input–Port 2.** **Loopback Mode Select Input–Port 1.** **Loopback Mode Select Input–Port 0.** All LOOP*x* pins are identical. If this pin is asserted High Local Analog Loopback is selected which causes LXT335 to ignore data received on RTIP and RRING and loop data internally from TTIP and TRING back to the receive inputs. If this pin is asserted Low Remote Loopback is selected which causes LXT335 to ignore data on $\overline{\text{NMARK}}$ and $\overline{\text{PMARK}}$ and to loop internally data received on RTIP and RRING to TTIP and TRING. If this pin is left open or unconnected normal operation mode is selected. LOOP*x* — Operating Mode L — Remote Loopback H — Local Loopback Open — Normal Operation Mode
56	LOOP2	DI	
57	LOOP1	DI	
58	LOOP0	DI	
59	$\overline{\text{NMARK1}}$	DO	**Receive Negative Data / Bipolar Violation Indication Output–Port 1** **Receive Positive Data/ Receive Data Output–Port 1** See $\overline{\text{NMARK3}}$/$\overline{\text{PMARK3}}$, pins 49, 50.
60	$\overline{\text{PMARK1}}$	DO	
61	RCLK1	DO	**Receive Clock Output–Port 1** See RCLK3, pin 51.
62	$\overline{\text{NMARK0}}$	DO	**Receive Negative Data Output–Port 0** **Receive Positive Data/ Receive Data Output–Port 0** See $\overline{\text{NMARK3}}$/$\overline{\text{PMARK3}}$, pins 49, 50.
63	$\overline{\text{PMARK0}}$	DO	
64	RCLK0	DO	**Receive Clock Output–Port 0** See RCLK3, pin 51.

1. Entries in I/O column are DI = Digital Input; DO = Digital Output; DIO = Digital Input Output; AI = Analog Input; AO = Analog Output; High Z = high impedance input/output; S = power/ground pins

FUNCTIONAL DESCRIPTION

Page 1 shows a simplified block diagram of the LXT335. The LXT335 is a quad line interface unit with four on-chip transmit drivers and four data receivers optimized for G.703 2.048 MHz applications. The front end of each line interface interfaces with four lines, one pair for transmit, one pair for receive. These two lines comprise a digital data loop for full duplex transmission. Each line interface also interfaces with back-end processors, through bipolar data I/O channels, and allows control by hardwired pins for stand-alone operation.

Receiver

The four LXT335 receivers are identical. The following paragraphs describe the operation of a single receiver. LXT335 receives the input signal via a 1:1 transformer. Recovered data is active low and output at $\overline{\text{PMARK}}$ and $\overline{\text{NMARK}}$. Timing information for external clock recovery is output at RCLK.

A peak detector and data slicers process the received signal. The peak detector samples the received signal and determines its maximum value. A percentage of the peak value is provided to the data slicers as a threshold level of 50% to ensure an optimum signal-to-noise ratio.

The receiver is capable of accurately recovering signals with up to 12 dB of cable attenuation (from 2.4 V), corresponding to a received signal level of approximately 500 mV. Regardless of received signal level, LXT335 holds its peak detectors above a minimum level of 0.225 V (typical) to provide immunity from impulsive noise.

After the data slicers process, the received signal goes to the data recovery and pulse stretcher section and then to the receive outputs $\overline{\text{PMARK}}$ and $\overline{\text{NMARK}}$.

Loss Of Signal Detector

The Loss of Signal Detector uses an analog detection scheme and complies with the ITU G.775 recommendation. During LOS conditions, received data is output on $\overline{\text{PMARK}}$/$\overline{\text{NMARK}}$. Any signal ~22 dB below the nominal 0 dB signal generates a loss of signal condition. LOS is deactivated again when the signal level rises to more than ~21 dB (typical) below the minimum 0 dB level. The $\overline{\text{PMARK}}$ and $\overline{\text{NMARK}}$ outputs stay active for external digital signal transition detection.

Transmitter

The four LXT335 low power transmitters are identical. The following paragraphs describe the operation of a single transmitter.

Bipolar transmit data from the digital backend processor is fed into the device at TPOS/TNEG and is passed through "as is". If $\overline{\text{TPD}}$ is asserted Low the transmitter remains powered down and the TTIP/TRNG outputs are held in a High-Z state. This feature allows use of the LXT335 in fully redundant applications.

Each output driver is supplied by a separate power supply (TVCC0 to TVCC3, TGND0 to TGND3). Current limiters on the output drivers provide short circuit protection and generate a driver failure monitoring signal in case the current limit is exceeded.

The transmitted pulse shape must be generated externally. Pulses are applied to the line drivers for transmission onto the line at TTIP and TRING. The line driver provides a constant low output impedance of < 3 Ω (typical) regardless of whether it is driving marks or spaces or during transitions. LXT335 provides programmable pulse amplitude output voltages.

If MODE is asserted High, the LXT335 is configured for matched line driver applications. In conjunction with external series resistors a well controlled driver output impedance provides excellent transmit return loss exceeding ETSI ETS300166 and Swiss PTT recommendations. If MODE is asserted Low, the LXT335 is configured for unmatched low power line driver applications where it drives a transformer without series resistors.

Asserting CNTL High and MODE Low, configures the LXT335 for 120 Ω loads. Asserting CNTL High and MODE High configures the LXT335 for 75 Ω loads. In transformer coupled applications the LXT335 produces 2.048 MHz pulses for both 75 Ω coaxial (2.37 V) and 120 Ω shielded twisted-pair (3.0 V) lines. Different transformer and resistor combinations are used for optimum transmit return loss performance. Internal circuitry stabilizes the output pulse amplitudes against supply variations and references them to an on-chip bandgap voltage reference.

Certain applications require common 1:2 transformers for the transmitter and receiver and software switchable 75/120 Ω operation while maintaining return loss in compliance with ETS300166. The LXT335 can be used with 25Ω transmit series resistors for both 75Ω and 120Ω operation (Figure 8).

Driver Failure Monitor

All transceiver incorporate internal Driver Failure Monitors (DFM) in parallel with TTIP and TRING. A capacitor, charged via a measure of the driver output current and discharged by a measure of the maximum allowable current, is used to detect driver failures. Shorted lines draw excess current, overcharging the cap. When the capacitor charge deviates outside the nominal charge window for one of the 4 drivers, the common DFM output pin reports a driver short circuit fail. The individual driver failure monitor output takes precedence and overwrites the transceiver specific LOS output. During a long string of spaces, a short-induced overcharge eventually bleeds off, clearing the DFM flag.

Diagnostic Mode Of Operation

Loopback

All LOOP*x* pins are identical. If this pin is asserted High, Local Analog Loopback is selected which causes LXT335 to ignore data received on RTIP and RRING and loop data internally from TTIP and TRING back to the receive inputs. If this pin is asserted Low, Remote Loopback is selected which causes LXT335 to ignore data on $\overline{\text{NMARK}}$ and $\overline{\text{PMARK}}$ and to loop internally data received on RTIP and RRING to TTIP and TRING.

If this pin is left open or unconnected normal operation mode is selected.

APPLICATION INFORMATION

Figure 2: Low Power Transmit Interface for Coax Cables

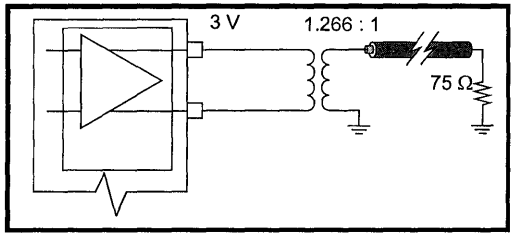


Figure 3: Transmit Interface for Coax Cables

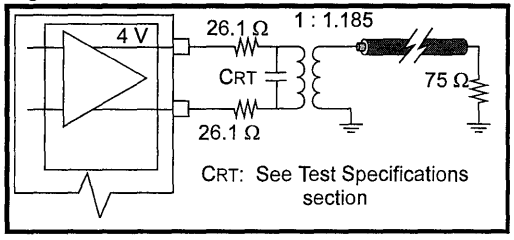


Figure 4: Low Power Transmit Interface for Twisted Pair Lines

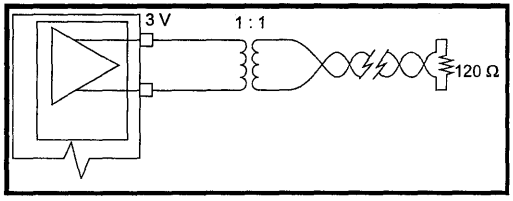


Figure 5: Transmit Interface for Twisted Pair Lines

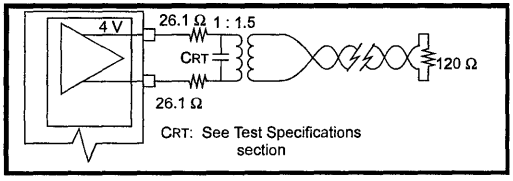


Figure 6: Receive Interface for Twisted Pair Lines

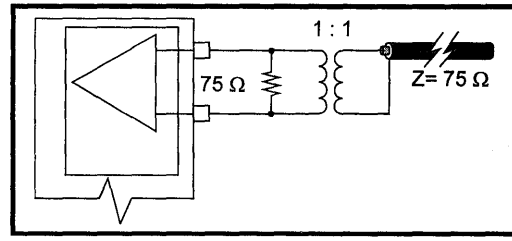


Figure 7: Receive Interface for Twisted-Pair Lines

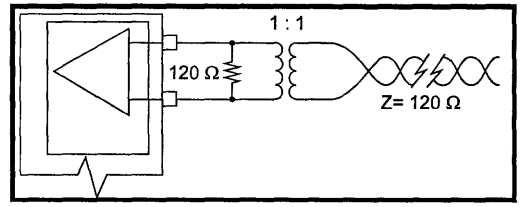


Table 2: Transformer Selection Guide[1]

Manufacturer	Transmit Side		Receive side (1:1 Ratio) (20 dB Return Loss)
	Part Number	Transformer Turns Ratio	Type
Pulse Engineering	PE-65586	1:1.36	Quad
	PE-65766	1:1.266	Dual
	PE-68789	1:1.5	Dual
	PE-65762	1:1.36	Dual
	PE-65861	1:2	Dual
	PE-65861	1:1	Dual
	PE-68789	1:1.185	Single
	PE-65389	1.266:1	Single
HALO	TG27-1505NX	1:1.36	Octal
	TD64-1205D	1:1.26	Dual
	TG29-1205NX	1:2	Octal
Bel-Fuse	0553-0013	1:1.36	Dual
	5006-1C	1:2	Dual
Schott Corp	67129300	1:2	Single

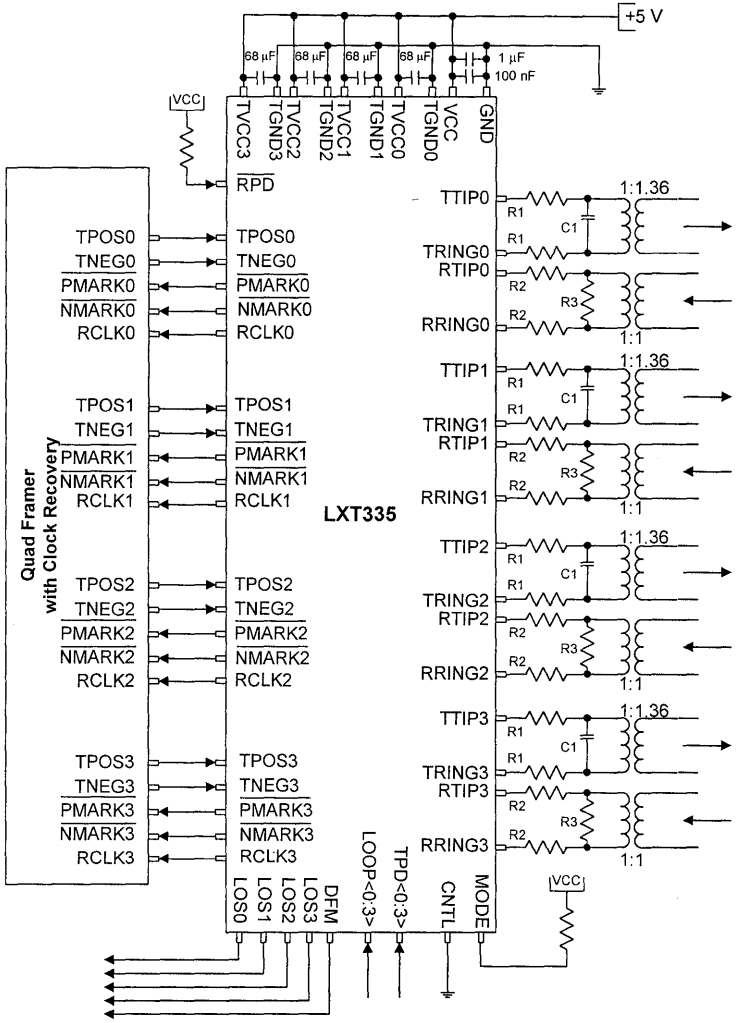
1. As of the publication date, Level One Communications, Inc., has tested the transformers listed in this table. However, part numbers and specifications change without notice. Design engineers should validate components before committing to their use.

Table 3: Transmit Transformer and Resistor Combinations

Transformer	Resistor	Return Loss[1]	CNTL1	MODE1	Impedance
1.266:1	0 Ω	< 1 dB	Low	Low	75 Ω
1:1	0 Ω	< 1 dB	Low	Low	120 Ω
1:1.185	26.1 Ω	20 dB	Low	High	75 Ω
1:1.5	26.1 Ω	20 dB	Low	High	120 Ω
1:1.36	25 Ω	18 dB	Low	High	75 Ω
1:1.36	25 Ω	18 dB	Low	High	120 Ω
1:2	15 Ω	≥ 8 dB	High	High	75 Ω
1:2	15 Ω	≥ 8 dB	High	Low	120 Ω

1. Typical values 51 kHz - 3.078 MHz

Figure 8: E1 120 Ω and 75 Ω Matched Line Applications



Component	Application	
	120 Ω	**75 Ω**
R1. Transmit resistor	25 Ω	25 Ω
R2. Receive resistor	1 kΩ	1 kΩ
R3. Receive terminating resistor	120 Ω	75 Ω
C1. Transmit capacitor (typical)	180 pF	180 pF

TEST SPECIFICATIONS

NOTE

The minimum and maximum values in Tables 4 through 9 and Figures 9 and 10 are performance specifications of the LXT335 and are guaranteed by test except, where noted, by design.

Table 4: Absolute Maximum Ratings

Parameter	Sym	Min.	Max.	Unit
DC supply voltage	VCC, GND	-0.3	6.0	V
Input voltage on any pin [1]	VIN	GND-0.3	RVCC + 0.3	V
Input voltage on RTIP, RRING	VIN	-6	RVCC + 0.3	V
Transient latchup current on any pin[2]	IIN	–	100	mA
Input current on any digital pin[3]	IIN	-10	10	mA
DC input current on TTIP, TRING[3]	IIN	–	±100	mA
DC input current on RTIP, RRING[3]	IIN	–	±20	mA
Storage temperature	TSTOR	-65	+150	° C
Total package power dissipation	–	–	1	W

CAUTION

Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to absolute maximum ratings conditions for external periods may affect device reliability.

1. Reference to ground.
2. Exceeding these values will cause SCR latchup.
3. Constant input current.

Table 5: Recommended Operating Conditions

Parameter	Sym	Min	Typ	Max	Units	Test Condition
DC supply voltage [1]	VCC	4.75	5.0	5.25	V	
Ambient operating temperature	TA	-40	+25	+85	° C	

1. TVCC must not exceed RVCC BY 0.3 V

Table 6: DC Characteristics (over recommended range)

Parameter		Sym	Min	Typ[1]	Max	Unit	Test Condition
Digital I/O pins	High-level input voltage	VIH	2.0	–	–	V	
	Low-level input voltage	VIL	—	–	0.8	V	
	High-level output voltage[2]	VOH	3.5	–	–	V	IOUT= -400µA
	Low-level output voltage[2]	VOL	—	–	0.4	V	IOUT= 1.6 mA
Input leakage current (digital input pins)		IIL	-10	–	+10	µA	
Tristate leakage current[5]		IHZ	-10		+10	µA	
Driver short circuit current		–	–	–	50	mA	See Figures 3 and 5
MODE input pins	Low-level input voltage	VINL	–	–	1.5	V	pins 17, 55, 56, 57, 58
	High-level input voltage	VINH	3.5	–	–	V	
	Mid-range input voltage	VINM	2.3	2.5	2.7	V	
	Low-level input current	IINL	–	–	50	µA	
	High-level input current	IINH	–	–	50	µA	
Total power dissipation [3]	75 Ω system (MODE=H)	PD	–	660	750	mW	Figure 3
	120 Ω system (MODE=H)	PD	–	660	750	mW	Figure 5
Total power dissipation[4]	75 Ω system (MODE=L)	PD	–	410	470	mW	Figure 2
	120 Ω system (MODE=L)	PD	–	410	470	mW	Figure 4
Power down current		ICCO	–	–	10	mA	

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Output Drivers will output CMOS logic levels into CMOS loads.
3. 100% 1s density. Power dissipation including device load while driving a matched line over the operating temperature range. Digital inputs are within 10% of the supply rails and digital outputs are driving a 50 pF load.
4. 50% 1s density. Power dissipation including device load while driving a line without matching resistors over the operating temperature range. Digital inputs are within 10% of the supply rails and digital outputs are driving a 50 pF load.
5. Applies to the following pins: 9, 12, 13, 16, 33, 36, 37, 40, 49-54, 59-64.

Table 7: Receive Characteristics

Parameter		Sym	Min	Typ	Max	Units	Test Condition
Permissible cable attenuation		–	500	–	–	mV	
		–	–	–	12	dB	@1024 kHz
Receiver dynamic range		DR	0.5	–	4.2	VP	
Signal to noise interference margin[1]		S/I	15	–	–	dB	per G.703, O.151
Signal to single tone interference margin		S/X	14	–	–	dB	O.151
$\overline{\text{PMARK}}$ / $\overline{\text{NMARK}}$ output Jitter		–	–	0.01	–	U.I.	peak to peak
Slicer ratio		SRE	43	50	57	%	rel. to peak input voltage
Analog loss of signal threshold		–	22	–	–	dB	
Loss of signal threshold		–	–	1	–	dB	
Receiver input impedance		–	–	40	–	kΩ	@ 1.024 kHz, RTIP to RRING
Input return loss[2]	51 kHz – 102 kHz	–	20	–	–	dB	measured against nominal impedance, Figures 6, 7.
	102 – 2048 kHz	–	20	–	–	dB	
	2048 kHz – 3072 kHz	–	20	–	–	dB	

1. No errors shall occur when the combined signal attenuated by the maximum specified interconnting cable loss is applied to the input port. See ITU O.151 recommendation for further details.
2. Guaranteed by design and other correlation factors.

Table 8: Transmit Timing Characteristics

Parameter	Sym	Min	Typ	Max	Unit	Test Condition
Transmit data rate	–	–	2.048	–	Mbps	
Transmit data tolerance	–	-50	–	50	ppm	
Output pulse width	tPW	–	244	–	ns	

Table 9: Receive Timing Characteristics (See Figure 9)

Parameter	Sym	Min	Typ	Max	Units	Test Condition
$\overline{\text{PMARK}}$/$\overline{\text{NMARK}}$ pulse width	tMPW	200	244	300	ns	
Receiver throughput delay	tRXD	–	65	–	ns	
Receive data rate tolerance	–	–	±80	–	ppm	
Receive data to receive clock delay time	–	–	5	–	ns	

Figure 9: Receive Timing Specifications

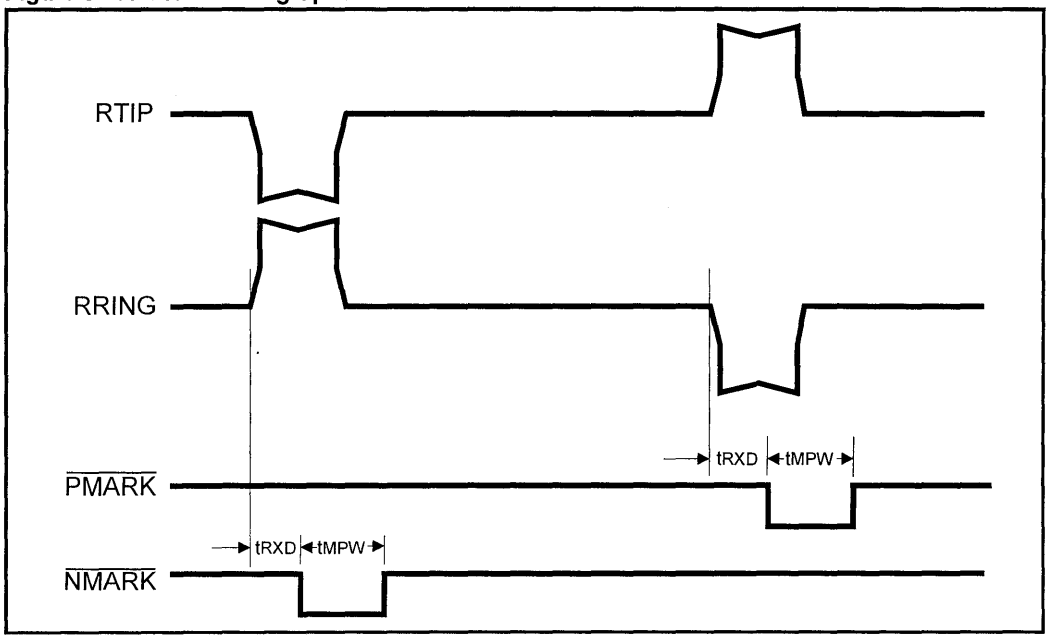
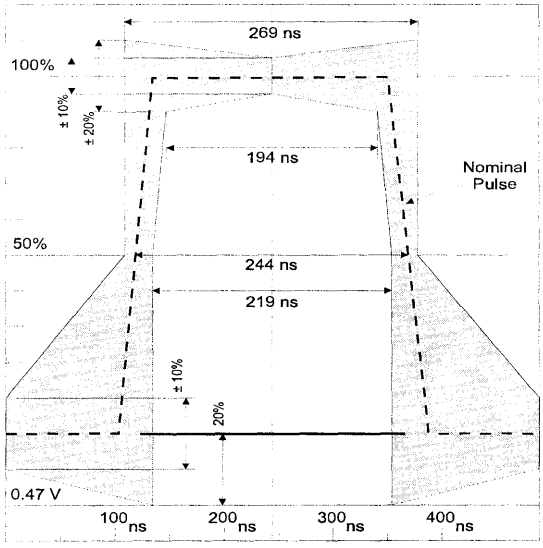


Figure 10: 2.048 MHz Pulse Mask G.703



NOTES

JULY 1996
Revision 0.0

LXT350/351 Integrated T1/E1 S/H Transceivers With Crystal-less Jitter Attenuation

General Description

The LXT350 and LXT351 are full-featured, fully-integrated transceivers for T1 and E1 short-haul applications. They are software switchable between T1 and E1 operation, and offer pulse equalization settings for all short-haul T1 and E1 line interface (LIU) applications.

The LXT350 and LXT351 are identical except for their control interface. The LXT350 provides both a serial I/O port for microprocessor control and a hardware control mode for stand alone operation. The LXT351 offers an Intel- or Motorola-bus compatible parallel I/O port for microprocessor control. Both incorporate advanced crystal-less digital jitter attenuation in either the transmit or receive data path starting at 3 Hz. B8ZS/HDB3 encoding/decoding and unipolar or bipolar data I/O are available. Both LIUs provide loss of signal monitoring and a variety of diagnostic loopback modes.

The LXT350/351 design uses an advanced double-poly, double-metal fabrication process and requires only a single 5-volt power supply.

Applications

- T1/E1 Asynchronous Multiplexers
- Digital Loop Carrier - Subscriber Carrier Systems
- SDH/SONET Multiplexers
- T1/E1 LAN/WAN interfaces for Bridges
- Digital Cross Connects

Features

- Fully integrated transceiver for short-haul T1 or E1 interfaces
- Crystal-less digital jitter attenuation
  - –Selectable either transmit or receive path
  - –No crystal or high-speed external clock required
- Meet or exceed specifications in ANSI T1.403 and T1.408; ITU G.703, G.736, G.775 and G.823; ITU-T I.431; ETSI 300-166 and 300-233; and AT&T Pub 62411
- Support 75 Ω (E1 coax), 100 Ω (T1 twisted-pair) and 120 Ω (E1 twisted-pair) applications
- Fully restores the received signal after transmission through a cable with attenuation of 18dB, at 1024 kHz
- Five Pulse Equalization Settings for T1 short-haul applications
- Transmit/receive performance monitors with Driver Fail Monitor Open (DFM) and Loss of Signal (LOS) outputs
- Selectable unipolar or bipolar data I/O and B8ZS/HDB3 encoding/decoding
- QRSS generator/detector for testing or monitoring
- Output short circuit current limit protection
- Local, remote and analog loopback capability
- Multiple-register serial- or parallel-control interface
- Compatible with Level One's LXT360/361 T1/E1 Long Haul/Short Haul Transceiver (Universal LIU)

LXT350 Transceiver Block Diagram

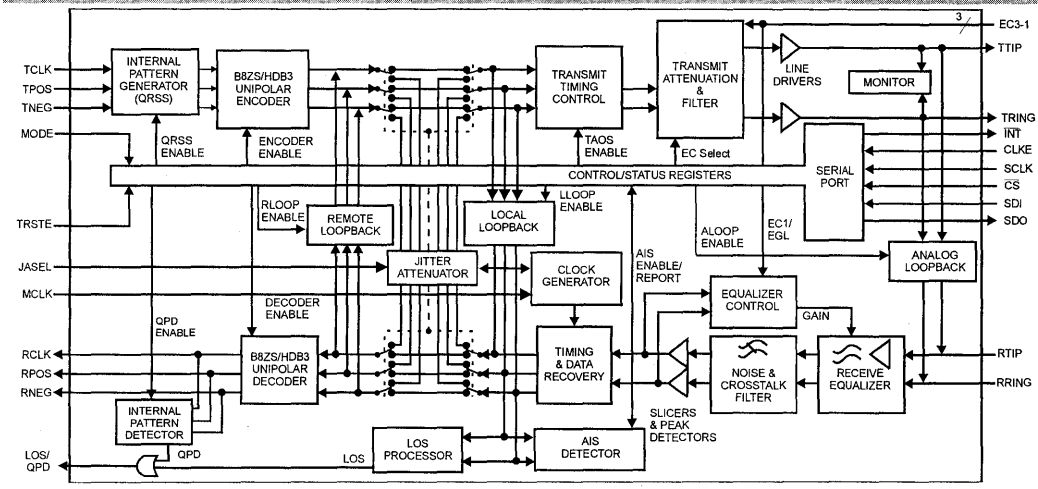


Figure 1: LXT350 Hardware Controlled Bipolar Mode Pin Assignments

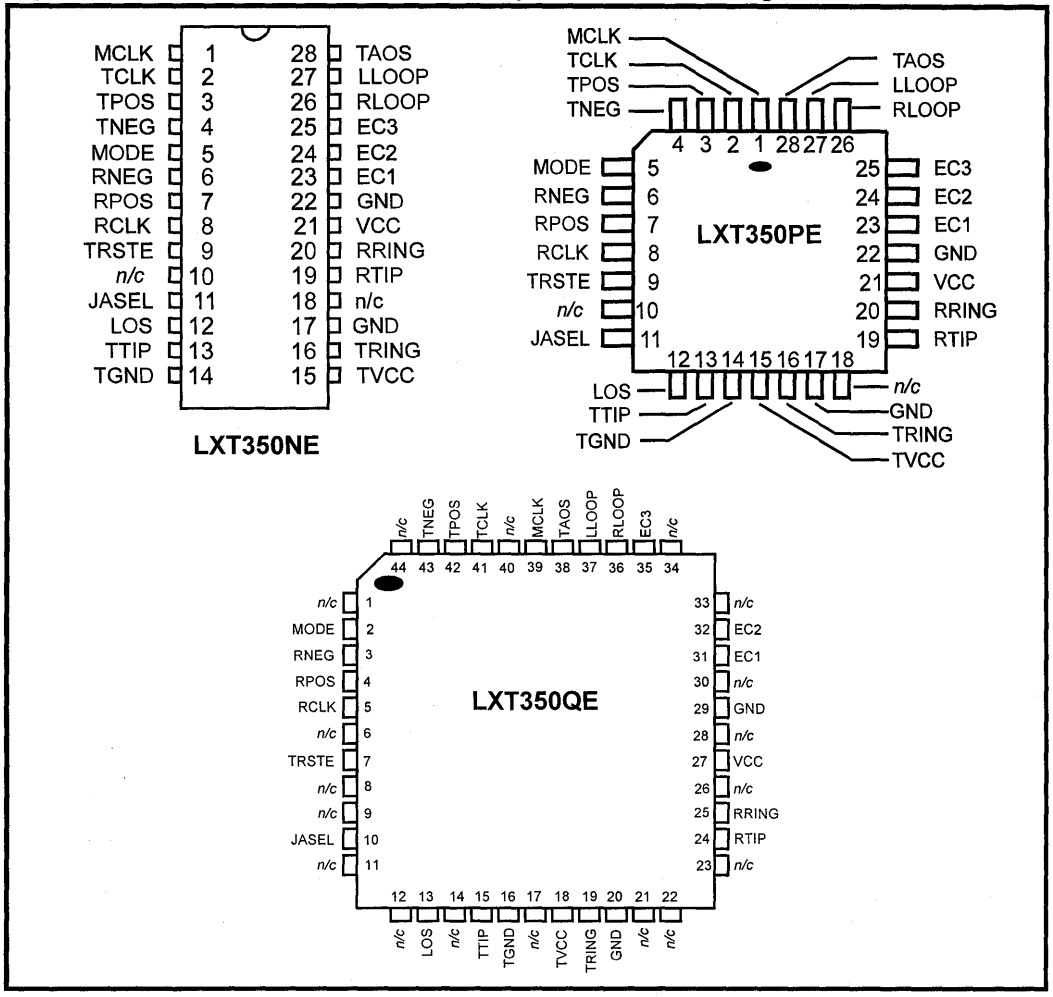


Table 1: LXT350 Clock and Data Pin Assignments by Mode[1]

Pin # NE/ PE	Pin # QE	External Data Modes		QRSS Modes	
		Bipolar Mode	Unipolar Mode	Bipolar Mode	Unipolar Mode
1	39	MCLK			
2	41	TCLK			
3	42	TPOS	TDATA	INSLER	

1. Data pins change based on whether external data or internal QRSS mode is active. Clock pins remain the same in both Hardware and Host Modes

Table 1: LXT350 Clock and Data Pin Assignments by Mode[1]

Pin # NE/ PE	Pin # QE	External Data Modes		QRSS Modes	
		Bipolar Mode	Unipolar Mode	Bipolar Mode	Unipolar Mode
4	43	TNEG	INSBPV	INSBPV	
6	3	RNEG	BPV	RNEG	BPV
7	4	RPOS	RDATA	RPOS	RDATA
8	5	RCLK			
13	15	TTIP			
14	16	TGND			
15	18	TVCC			
16	19	TRING			
19	24	RTIP			
20	25	RRING			
21	27	VCC			
22	29	GND			

1. Data pins change based on whether external data or internal QRSS mode is active. Clock pins remain the same in both Hardware and Host Modes

Table 2: LXT350 Control Pins by Mode

Pin NE/ PE	Pin QE	Hardware Modes		Host Modes		Pin NE/ PE	Pin QE	Hardware Modes		Host Modes	
		Unipolar/ Bipolar	QRSS	Unipolar/ Bipolar	QRSS			Unipolar/ Bipolar	QRSS	Unipolar/ Bipolar	QRSS
5	2	MODE		MODE		24	32	EC2		SDI	
9	7	TRSTE		TRSTE		25	35	EC3		SDO	
11	10	JASEL		*Low*		26	36	RLOOP		$\overline{CS}$	
12	13	LOS	LOS/ QPD	LOS	LOS/ QPD	27	37	LLOOP		SCLK	
23	31	EC1		$\overline{INT}$		28	38	TAOS	QRSS	CLKE	

Table 3: LXT350 Hardware Controlled Bipolar Mode Signal Descriptions

Pin NE/ PE	Pin QE[1]	Symbol	I/O[2]	Description
1	39	MCLK	DI	**Master Clock**. Connect to 1.544 MHz for T1 operation; to 2.048 MHz for E1. MCLK requires an external, independent input to generate internal clocks. Required accuracy is better than ± **32 ppm** with a typical duty cycle of 50%. Upon Loss of Signal (LOS), RCLK is derived from MCLK.
2	41	TCLK	DI	**Transmit Clock**. 1.544 MHz or 2.048 MHz clock input. Transceiver samples TPOS and TNEG on the falling edge of TCLK
3 4	42 43	TPOS TNEG	DI	**Transmit Data – Positive and Negative**. In the Bipolar I/O mode, these pins are the positive and negative sides of a bipolar input pair. Data to be transmitted onto the line is input at these pins. Table 4 describes Unipolar Mode functions.
5	2	MODE	DI	**Mode Select**. Connecting MODE Low puts the LXT350 in Hardware Mode. In Hardware Mode, the serial interface is disabled and hardwired pins are used to control configuration and report status. Leaving MODE open activates Hardware Mode and enables the B8ZS/HDB3 encoder/ decoder and Unipolar Mode. Connecting MODE High puts the LXT350 in Host Mode. In Host Mode, the serial interface controls the LXT350 and displays its status.
6 7	3 4	RNEG RPOS	DO	**Receive Data – Negative and Positive**. In the Bipolar I/O mode, these pins are the positive and negative sides of a bipolar output pair. Data recovered from the line interface is output on these pins. A signal on RNEG corresponds to receipt of a negative pulse on RTIP/RRING. A signal on RPOS corresponds to receipt of a positive pulse on RTIP/ RRING. RNEG/RPOS outputs are Non-Return-to-Zero. Both outputs are stable and valid on the rising edge of RCLK. Refer to Table 4 for Unipolar mode function descriptions.
8	5	RCLK	DO	**Recovered Clock**. The clock recovered from the line input signal is output on this pin. Under LOS conditions there is a smooth transition from RCLK to MCLK output.
9	7	TRSTE	DI	**Tristate**. Connecting TRSTE High forces all output pins to a high-impedance state. Connecting TRSTE Low sets the LXT350 to the Hardware Bipolar Mode. Leaving TRSTE open enables the Unipolar Mode. (See Table 4 for Unipolar function descriptions.)

1. Pins 1, 6, 8, 11, 12, 14, 17, 20, 22, 23, 26, 28, 33, 34, 40 and 44 are not connected (*n/c*). Pins 9 and 21 must be left floating.
2. I/O column entries: DI = Digital Input; DO = Digital Output; AI = Analog Input; AO = Analog Output.

Table 3: LXT350 Hardware Controlled Bipolar Mode Signal Descriptions – continued

Pin NE/ PE	Pin QE[1]	Symbol	I/O[2]	Description
10	–	*n/c*	DO	*No connection. Leave this pin floating.*
11	10	JASEL	DI	**Jitter Attenuation Select**. Selects jitter attenuation location. Connecting JASEL High activates the jitter attenuator in the receive path. Connecting JASEL Low activates the jitter attenuator in the transmit path. Leaving JASEL open disables JA.
12	13	LOS	DO	**Loss of Signal Indicator**. In T1 mode, LOS goes High on receipt of 175 consecutive spaces and returns Low when the received signal reaches a mark density of 12.5% (determined by receipt of 16 marks within a sliding window of 128 bits with fewer than 100 consecutive zeros). In E1 modes, LOS goes High on receipt of 32 consecutive spaces, and returns Low when the receiver detects 12.5% mark density (determined by receipt of 4 marks within a sliding window of 32 bits with fewer than 16 consecutive zeros). The transceiver outputs receives marks on RPOS and RNEG even when LOS is High.
13 16	15 19	TTIP TRING	AO	**Transmit Tip and Ring**. Differential Driver Outputs. These outputs are designed to drive a 50 - 200 Ω load. The transformer and line matching resistors should be selected to give the desired pulse height and return loss performance.
14	16	TGND	–	**Ground.** Ground return for the transmit driver power supply TVCC.
15	18	TVCC	DI	**+5 VDC Power Supply** input for the transmit drivers. TVCC must not vary from VCC by more than ± 0.3 V.
17	29	GND	–	**Ground**. Tie this pin to ground.
18	–	*n/c*	–	*Leave this pin open.*
19 20	24 25	RTIP RRING	AI	**Receive Tip and Ring**. The AMI signal received from the line is applied at these pins. A 1:1 transformer is required. Data and clock from the signal applied at these pins are recovered and output on the RPOS/RNEG, and RCLK pins.
21	27	VCC	–	**+5 VDC Power Supply** for all circuits except the transmit drivers. (Transmit drivers are supplied by TVCC.)
22	29	GND	–	**Ground.** Ground return for power supply VCC.
23 24 25	31 32 35	EC1 EC2 EC3	DI	**Equalization Control 3-1**. These pins define the **Pulse Equalization** settings. See Table 12 for additional details.
26	36	RLOOP	DI	**Remote Loopback.** When held High, the clock and data inputs from the framer (TPOS/TNEG or TDATA) are ignored and the data received from the line is transmitted back onto the line at the RCLK frequency. During remote loopback, the device ignores the in-line encoders/decoders. See Figure 8.
27	37	LLOOP	DI	**Local Loopback**. When held High, the data on TPOS and TNEG loops back digitally to RPOS and RNEG outputs (through JA if enabled). Leaving this pin open enables Analog Loopback (TTIP and TRING looped back to RTIP and RRING). See Figures 5, 6, and 7.
28	38	TAOS	DI	**Transmit All Ones**. When held High the transmit data inputs are ignored and the LXT350 transmits a stream of 1s at the TCLK frequency. (If TCLK is not supplied, MCLK is the transmit clock reference.) TAOS is inhibited during Remote Loopback. Leaving this pin open enables QRSS pattern generation and detection. See Figures 5, 10, and 11.

1. Pins 1, 6, 8, 11, 12, 14, 17, 20, 22, 23, 26, 28, 33, 34, 40 and 44 are not connected (*n/c*). Pins 9 and 21 must be left floating.
2. I/O column entries: DI = Digital Input; DO = Digital Output; AI = Analog Input; AO = Analog Output.

Table 4: LXT350 Hardware Controlled Unipolar Mode Signal Assignments

Pin NE/ PE	Pin QE	Symbol	I/O[1]	Description
3	42	TDATA	DI	**Transmit Data**. Unipolar input for data to be transmitted onto the line.
4	43	INSBPV	DI	**Insert Bipolar Violation**. This pin is sampled on the falling edge of TCLK to control Bipolar Violation Insertions in the transmit data stream. A Low-to-High transition is required to insert subsequent BPVs.
6	3	BPV	DO	**Bipolar Violation.** BPV goes High to report receipt of a bipolar violation from the line. This is an NRZ output, valid on the rising edge of RCLK.
7	4	RDATA	DO	**Receive Data**. RDATA is a unipolar NRZ output of data recovered from the line interface. In Hardware Mode RDATA is stable and valid on the rising edge of RCLK.

1. I/O Column entries: DI = Digital Input; DO = Digital Output; AI = Analog Input; AO = Analog Output.

Table 5: LXT350 Hardware Controlled QRSS Unipolar Mode Signal Assignments

Pin NE/ PE	Pin QE	Symbol	I/O[1]	Description
3	42	INSLER	DI	**Insert Logic Error**. When this pin goes from Low to High, the transceiver inserts a logic error into the transmitted QRSS data pattern. The error follows the data flow in whatever loopback mode is in effect. The LXT350 samples this pin on the falling edge of TCLK (or MCLK, if TCLK is not present).
4	43	INSBPV	DI	**Insert Bipolar Violation**. When this pin goes from Low to High, the transceiver inserts a bipolar violation error into the transmitted QRSS data pattern. A subsequent insertion requires another Low to High transition. The LXT350 samples this pin on the falling edge of TCLK (or MCLK, if TCLK is not present).
6	3	BPV[2]	DO	**Bipolar Violation**. BPV goes High to report receipt of a bipolar violation from the line. This is an NRZ output, valid on the rising edge of RCLK.
7	4	RDATA[2]	AO	**Received Data**. RDATA is a unipolar NRZ output of data recovered from the line interface. In hardware Mode, RDATA is stable and valid on the rising edge of RCLK.
12	13	LOS/QPD	DO	**Loss of Signal/QRSS Pattern Detect**. This pin acts as a QPD indicator as well as LOS indicator. The QRSS Pattern synchronization criterion is fewer than four errors in 128 bits. In this mode, as long as the transceiver does not detect a QRSS pattern QPD stays High. As soon as the device does detect a QRSS pattern, the pin goes Low; any bit errors cause QPD to go High for half a clock cycle. This output can trigger an external error counter. An LOS condition also makes this pin go High. See Figure 11.
28	38	QRSS	DI	**QRSS**. Leaving this pin open, enables QRSS pattern generation and detection. The transceiver transmits the QRSS pattern at the TCLK rate (or MCLK, if TCLK is not present).

1. I/O Column entries: DI = Digital Input; DO = Digital Output; AI = Analog Input; AO = Analog Output.
2. In QRSS Bipolar Mode, pins 6 and 7 (or pins 3 and 4 on the QFP package) act as RNEG and RPOS output, respectively.

Table 6: LXT350 Host Controlled Bipolar Mode Signal Assignments [1,2]

Pin NE/ PE	Pin QE	Symbol	I/O[3]	Description
6 7	3 4	RNEG RPOS	DO	**Received Data–Negative and Positive**. In the Bipolar I/O Mode, these pins are the negative and positive sides of a bipolar output pair. The transceiver outputs the data recovered from the line interface on these pins. A signal on RNEG corresponds to receipt of a negative pulse on RTIP/RRING. A signal on RPOS corresponds to receipt of a positive signal on RTIP/RRING. RNEG/RPOS outputs are Non-Return-to-Zero (NRZ). CLKE determine the clock edge at which these outputs are stable and valid. See Figure 19.
9	7	TRSTE	DI	**Tristate**. Connecting TRSTE High forces all output pins to high-impedance state. Connect this pin Low for normal operation.
10	–	*n/c*	–	*Not connected.*
11	10	GND	–	*Tie this pin to ground.*
17	29	GND	–	*Tie this pin to ground*
23	31	$\overline{INT}$	DO	**Interrupt** (Active Low–Maskable). $\overline{INT}$ goes Low to flag the host when any of LOS, AIS, QRSS or DFMO changes state or when there is an Elastic Store overflow or underflow. $\overline{INT}$ is an open drain output which requires a connection to power supply VCC through a resistor. Reset $\overline{INT}$ by writing a one to the respective bit in the Interrupt Clear Register.
24	32	SDI	DI	**Serial Data Input**. Input port for the 16-bit serial address/command and data word. LXT350 samples SDI on the rising edge of SCLK. See Figure 20.
25	35	SDO	DO	**Serial Data Output**. If CLKE is High, SDO is valid on the rising edge of SCLK. If CLKE is Low, SDO is valid on the falling edge of SCLK. This pin goes to a high-impedance state when the serial port is being written to or when $\overline{CS}$ is High. See Figure 21.
26	36	$\overline{CS}$	DI	**Chip Select** (Active Low). This input is used to access the serial interface. For each read or write operation, $\overline{CS}$ must transition from High to Low, and remain Low.
27	37	SCLK	DI	**Serial Clock**. This clock is used to write data to or read data from the serial interface registers. The clock frequency can be any rate up to 2.048 MHz.
28	38	CLKE	DI	**Clock Edge**. Setting CLKE High causes RPOS and RNEG to be valid on the falling edge of RCLK, with SDO valid on the rising edge of SCLK. Setting CLKE Low makes RPOS and RNEG valid on the rising edge of RCLK and SDO valid on the falling edge of SCLK.

1. For pins not described in this table, see Table 3. Pin out for data pins in Unipolar and QRSS Modes remains the same as in Tables 4 and 5. In Host Mode, the control pins (23-28 for NE/PE or 31-38 for QE) change as shown in Table 6.
2. In QRSS Bipolar Mode, pins 6 and 7 (or pins 3 and 4 on the QFP package) seven act as RNEG and RPOS, respectively.
3. I/O Column entries: DI = Digital Input; DO = Digital Output; AI = Analog Input; AO = Analog Output.

Figure 2: LXT351 Bipolar Mode Pin Assignments

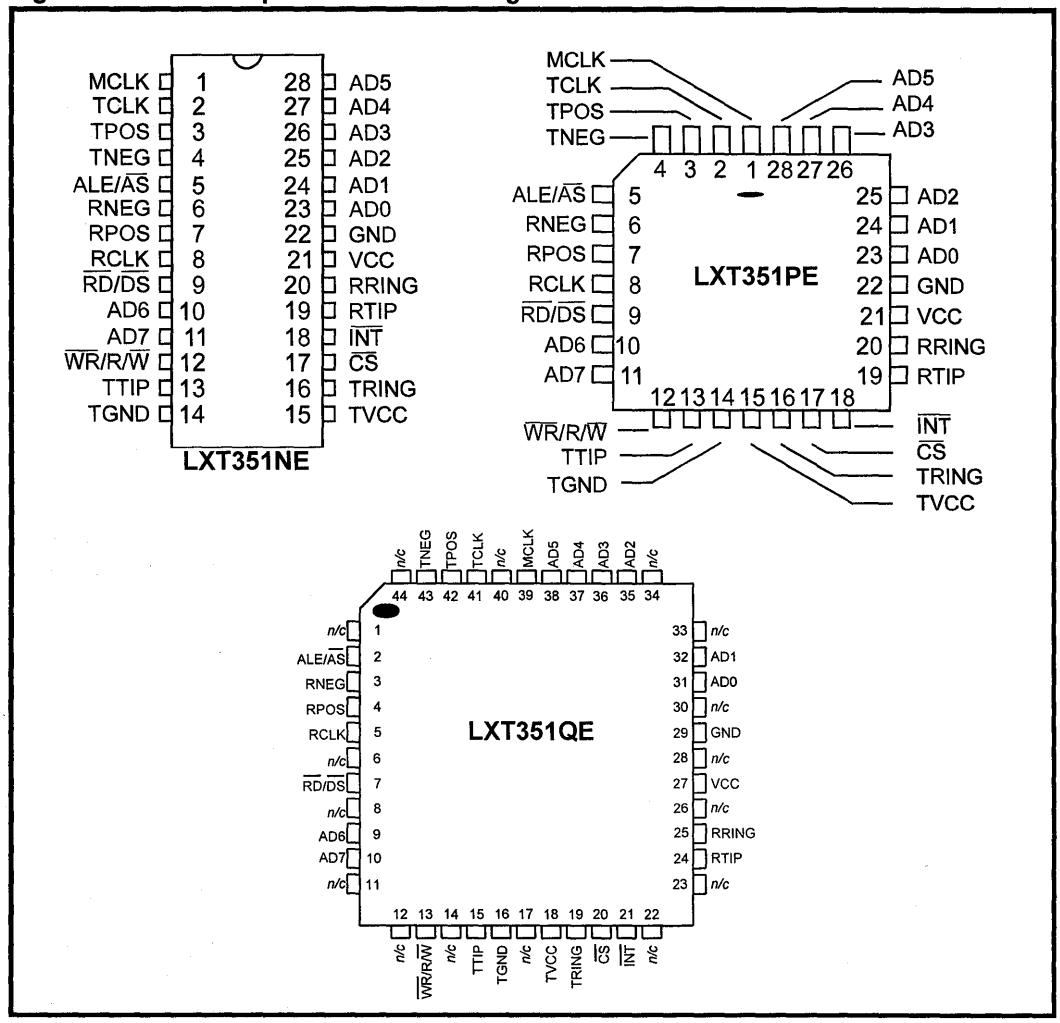


Table 7: LXT351 Clock and Data Pin Assignments by Mode[1]

Pin NE/ PE	Pin QE	External Data Modes		QRSS Modes	
		Bipolar Mode	Unipolar Mode	Bipolar Mode	Unipolar Mode
1	39	MCLK			
2	41	TCLK			
3	42	TPOS	TDATA	INSLER	

1. Data pins change based on whether external data or internal QRSS mode is active. These pins remain the same in both Hardware and Host Modes.

Table 7: LXT351 Clock and Data Pin Assignments by Mode[1]

Pin NE/ PE	Pin QE	External Data Modes		QRSS Modes	
		Bipolar Mode	Unipolar Mode	Bipolar Mode	Unipolar Mode
4	43	TNEG	INSBPV	INSBPV	
6	3	RNEG	BPV	RNEG	BPV
7	4	RPOS	RDATA	RPOS	RDATA
8	5	RCLK			
13	15	TTIP			
14	16	TGND			
15	18	TVCC			
16	19	TRING			
19	24	RTIP			
20	25	RRING			
21	27	VCC			
22	29	GND			

1. Data pins change based on whether external data or internal QRSS mode is active. These pins remain the same in both Hardware and Host Modes.

Table 8: LXT351 Processor Interface Pins

Pin NE/ PE	Pin QE	Address/Data Bus Type		Pin NE/ PE	Pin QE	Address/Data Bus Type	
		Intel	Motorola			Intel	Motorola
5	2	ALE	$\overline{AS}$	25	35	AD2	
9	7	$\overline{RD}$	DS	26	36	AD3	
12	13	$\overline{WR}$	R/$\overline{W}$	27	37	AD4	
17	20	$\overline{CS}$		28	38	AD5	
18	21	$\overline{INT}$		10	9	AD6	
23	31	AD0		11	10	AD7	
24	32	AD1					

Table 9: LXT351 Bipolar Mode Signal Assignments

Pin NE/ PE	Pin QE[2]	Symbol	I/O[1]	Description
1	39	MCLK	DI	**Master Clock**. Connect to 1.544 MHz for T1 operation; to 2.048 MHz for E1. MCLK requires an external, independent input to generate internal clocks. Required accuracy is better than ± 32 ppm with a typical duty cycle of 50%. Upon Loss of Signal (LOS), the transceiver derives RCLK from MCLK.
2	41	TCLK	DI	**Transmit Clock**. 1.544 MHz or 2.048 MHz bit rate clock input. The transceiver samples TPOS and TNEG on the falling edge of TCLK
3 4	42 43	TPOS TNEG	DI	**Transmit Data – Positive and Negative**. In the Bipolar I/O Mode, these pins are the positive and negative sides of a bipolar input pair. Data for transmission onto the line is input at these pins.
5	2	ALE $\overline{AS}$	DI	**Address Latch Enable/Address Strobe** (Active Low). Connects to Intel (ALE) or Motorola ($\overline{AS}$) signal. On Motorola bus, this signal is Active Low. **Leaving this pin floating forces all output pins into a high impedance state.**
6 7	3 4	RNEG RPOS	DO	**Receive Data – Negative and Positive**. In the Bipolar I/O mode, these pins are the positive and negative sides of a bipolar output pair. Data recovered from the line interface is output on these pins. A signal on RNEG corresponds to receipt of a negative pulse on RTIP/RRING. A signal on RPOS corresponds to receipt of a positive pulse on RTIP/RRING. RNEG/RPOS outputs are Non-Return-to Zero. Both outputs are stable and valid on the rising edge of RCLK. Refer to Table 10 for Unipolar mode function descriptions.
8	5	RCLK	DO	**Recovered Clock**. The output on this pin is the clock recovered from the line input signal. Under LOS conditions there is a smooth transition from RCLK to MCLK output.
9	7	$\overline{RD}$ $\overline{DS}$	DI	**Read** (Active Low)/**Data Strobe** (Active Low). On an Intel bus, this signal, Read, goes Low to command a read operation. On a Motorola bus, this signal, Data Strobe, goes Low when data is being driven on the address/data bus. Data is valid on the rising edge of $\overline{DS}$.
10	9	AD6	DI/ O	**Address/Data bus lines 6 and 7**. Used with pins 24-28 as the address/data bus.
11	10	AD7	DI/ O	
12	13	$\overline{WR}$ R/$\overline{W}$	DI	**Write** (Active Low) or **Write/Read**. On an Intel bus, driving this signal (Write) Low enables a write operation on the Address/Data bus. On a Motorola bus, driving this signal (Read/Write) High commands a read operation, driving it Low commands a write operation.
13 16	15 19	TTIP TRING	AO	**Transmit Tip and Ring**. Differential Driver Outputs. The design load for these outputs is 50 - 200 Ω. Select the transformer and line matching resistors to give the desired pulse height.
14	16	TGND	–	**Ground.** Ground return for the transmit drivers power supply TVCC.

1. I/O column entries DI = Digital Input; DO = Digital Output, DI/O = Digital Input and Output; AI = Analog Input , AO = Analog Output.
2. Pins 1, 6, 8, 11, 12, 17, 22, 23, 26, 28, 30, 33, 34, 40 and 44 are not connected *(n/c)*.

Table 9: LXT351 Bipolar Mode Signal Assignments – continued

Pin NE/ PE	Pin QE[2]	Symbol	I/O[1]	Description
15	18	TVCC		**+5 VDC Power Supply** input for the transmit drivers. TVCC must not vary from VCC by more than ± 0.3 V.
17	20	$\overline{CS}$	DI	**Chip Select** (Active Low). For each read or write on the Address/Data bus, this pin must go Low during the operation. See Figures 22 and 23 for timing requirements. In the case of a single processor controlling several chips, this is the line it uses to command a specific transceiver.
18	21	$\overline{INT}$	DO	**Interrupt** (Active Low). This pin goes Low to signal an interrupt on the chip. To identify the specific interrupt, read the Performance Status Register. To clear or mask an interrupt, write a one to the appropriate bit in the Clear Interrupt Register.
19 20	24 25	RTIP RRING	AI	**Receive Tip and Ring**. The AMI signal received from the line is applied at these pins. A 1:1 transformer is required. Data and clock from the signal applied at these pins are recovered and output on the RPOS/RNEG, and RCLK pins.
21	27	VCC		**+5 VDC Power Supply** for all circuits except the transmit drivers. (Transmit drivers are supplied by TVCC.)
22	29	GND		**Ground** return for power supply VCC.
23 24 25 26 27 28	31 32 35 36 37 38	AD0 AD1 AD2 AD3 AD4 AD5	DI/ O	**Address/Data Lines 0-5**. (Also pins 10, 11–AD6 and 7) Conform to Intel and Motorola Address/Data bus specifications.

1. I/O column entries DI = Digital Input; DO = Digital Output, DI/O = Digital Input and Output; AI = Analog Input , AO = Analog Output.
2. Pins 1, 6, 8, 11, 12, 17, 22, 23, 26, 28, 30, 33, 34, 40 and 44 are not connected *(n/c)*.

Table 10: LXT351 Unipolar Mode Signal Assignments[1]

Pin NE/ PE	Pin QE	Symbol	I/O[2]	Description
3	42	TDATA	DI	**Transmit Data**. Unipolar data for transmission onto the line.
4	43	INSBPV	DI	**Insert Bipolar Violation**. Controls bipolar violation insertions, requires Low-to-High transition to insert each violation, the LXT351 samples the signal on the falling edge of TCLK.
6	3	BPV	DO	**Bipolar Violation**. BPV goes High on receipt of a bipolar violation from the line. This is an NRZ output, valid on the rising edge of RCLK.
7	4	RDATA	DO	**Received Data**. RDATA is an NRZ output of the data recovered from the line interface. RDATA is valid on the rising edge of RCLK.

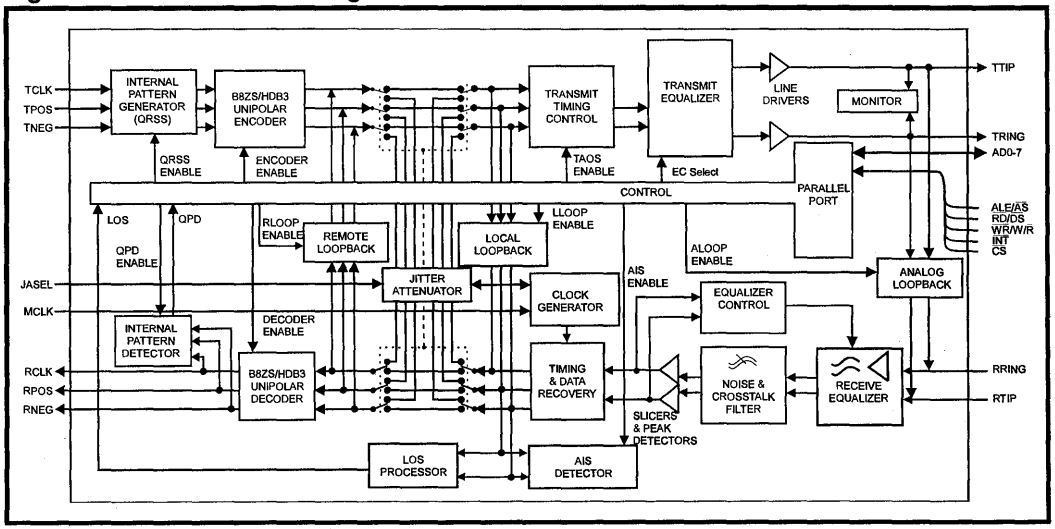
1. For the descriptions of pins not identified in this table, see Table 9: LXT351 Bipolar Mode Signal Assignments.
2. I/O column entries DI = Digital Input; DO = Digital Output, DI/O = Digital Input and Output; AI = Analog Input , AO = Analog Output.

Table 11: LXT351 QRSS Unipolar Mode Signal Assignments[1,2]

Pin NE/ PE	Pin QE	Symbol	I/O[3]	Description
3	42	INSLER	DI	**Insert Logic Error**. When this pin goes from Low to High, the transceiver inserts a logic error into the transmitted QRSS data pattern. The error follows the data flow in whatever loopback mode is in effect. The LXT351 samples this pin on the falling edge of TCLK (or MCLK, if TCLK is not present).
4	43	INSBPV	DI	**Insert Bipolar Violation**. When this pin goes from Low to High, the transceiver inserts a bipolar violation error into the transmitted QRSS data pattern. A subsequent insertion requires another Low to High transition. The LXT351 samples this pin on the falling edge of TCLK (or MCLK, if TCLK is not present).
6	3	BPV	DO	**Bipolar Violation**. BPV goes High on receipt of a bipolar violation from the line. This is an NRZ output, valid on the rising edge of SCLK.
7	4	RDATA	DO	**Received Data**. RDATA is an NRZ output of the data recovered from the line interface. RDATA is valid on the rising edge of RCLK.

1. For the descriptions of pins not identified in this table, see Table 9: LXT351 Bipolar Mode Signal Assignments.
2. In QRSS Bipolar Mode, pins 6 and 7of the NE/PE packages or pins 3 and 4 of the QE package act as RNEG and RPOS, respectively.
3. I/O column entries DI = Digital Input; DO = Digital Output, DI/O = Digital Input and Output; AI = Analog Input, AO = Analog Output.

Figure 3: LXT351 Block Diagram



FUNCTIONAL DESCRIPTION

The LXT350 and LXT351 are fully-integrated, PCM transceivers for or short-haul, 1.544 Mbps (T1) or 2.048 Mbps (E1) applications allowing full-duplex transmission of digital data over existing twisted-pair installations. They interface with two lines (one pair each for transmit and receive) through standard pulse transformers and appropriate resistors.

The figure on the front of this Data Sheet shows a block diagram of the LXT350. In Host Mode the device is controlled through a serial microprocessor. In Hardware Mode it is controlled via individual pins. Figure 3 is a block diagram of the LXT351. The LXT351 has a parallel port for microprocessor control. Both transceivers provide a high-precision, crystal-less jitter attenuator. The user may place it in the transmit or receive path, or bypass it completely. The transceivers meet or exceed ANSI, ITU and E1 requirements.

INITIALIZATION

During power up, the transceiver remains static until the power supply reaches approximately 3 V. On crossing this threshold, the device begins a 32 ms reset cycle to calibrate the Phase Locked Loops. The transceiver uses a reference clock to calibrate the PLL–the transmitter reference is TCLK, and the receiver reference clock is MCLK. MCLK is mandatory for chip operation.

Reset Operation

Reset clears and sets all registers to 0 and resets the status and state machines for the LOS, AIS and QRSS blocks. In Hardware Mode, holding pins RLOOP, LLOOP and TAOS High for at least one clock cycle resets the device. Writing a 1 to the bit CR2.RESET commands reset in Host Mode. Allow 32 ms for the device to settle after removing all reset conditions.

TRANSMITTER

Digital Data Interface

Input data for transmission onto the line is clocked serially into the device at the TCLK rate. TPOS and TNEG are the bipolar data inputs. TDATA accepts unipolar data. (Leaving TRSTE open enables Hardware Unipolar Mode.)

Input data may pass through either the Jitter Attenuator or B8ZS/HDB3 encoder or both. Bit CR1.ENCENB = 1 enables B8ZS/HDB3 encoding in Host Mode. In Hardware Mode, leaving the MODE pin open selects zero suppression coding. With zero suppression enabled, the EC*x* inputs (see Table 12) determine the coding scheme (B8ZS for T1 or HDB3 for E1 mode). For the HDB3 scheme, set EC3-1 to 000 or 001. Other EC*x* settings select the B8ZS option. The transmit clock (TCLK) supplies input synchronization. The Test Specifications section defines the transmit timing requirements for TCLK and the Master Clock (MCLK).

Short Circuit Current Limit

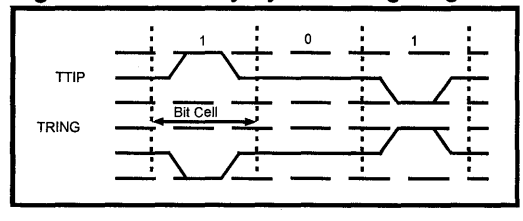
The transmitter includes a short-circuit limiter. This limits the current sourced into a low-impedance load. It automatically resets when the load current drops below the limit. The current is determined by the interface circuitry (total resistance on transmit side).

In Host Mode, the Performance Status Register flags open circuits in bit PSR.DFMO. A transition on DFMO will provide an interrupt and the transition sets bit TSR.DFMO = 1. Writing a 1 in bit ICR.CDFMO clears the interrupt; leaving a 1 in the bit masks that interrupt.

Output Drivers

The transceivers transmit data as a 50% line code as shown in Figure 4. Activating the line driver only during a mark reduces power consumption. The output driver is disabled during transmission of a space. Biasing of the transmit DC level is on-chip.

Figure 4: 50% Duty Cycle Coding Diagram



Idle Mode

Transmit Idle Mode is a normal operational mode (as opposed to modes) which allows multiple transceivers to be connected to a single line for redundant applications. TTIP and TRING remain in a high impedance state when TCLK is not present. Remote or Dual Loopback, TAOS or any internal transmit patterns temporarily disable the high impedance state.

Pulse Shape

The Equalizer Control inputs (EC3 through EC1) determine the transmitted pulse shape. In Host Mode, the I/O port controls the EC*x* values. For the LXT350 in Hardware Mode, three individual pins provide the EC*x* inputs.

Shaped pulses meeting the T1 DSX-1 and E1 specifications are applied to the AMI line driver for transmission onto the line at TTIP and TRING. Refer to the Test Specifications section for pulse mask specifications.

RECEIVER

A 1:1 transformer provides the interface to the line. Recovered data is output at RPOS/RNEG (RDATA in Unipolar mode), and the recovered clock is output at RCLK. The Test Specifications section shows receiver timing.

The transceiver filters the equalized signal and applies it to the peak detector and data slicers. The peak detector samples the inputs and determines the maximum value of the received signal. The data slicers are set at 50% of the peak value to ensure optimum signal-to-noise performance for T1 or E1 operation.

After processing through the data slicers, the received signal goes to the data and timing recovery section, then to the B8ZS/HDB3 decoder (if selected) and to the receive monitor. The data and timing recovery circuits provide input jitter tolerance significantly better than required by AT&T Pub 62411 and ITU G.823. See the Test Specifications section.

Table 12: Equalizer Control Input Settings

EC3	EC2	EC1	Function	Pulse	Cable	Coding[1]
0	0	0	E1	ITU Rec G.703	75 Ω Coax/120 Ω TP	HDB3
0	1	1	T1	0-133 ft / 0.6 dB	100 Ω TP	B8ZS
1	0	0	T1	133-266 ft / 1.2 dB	100 Ω TP	B8ZS
1	0	1	T1	266-399 ft / 1.8 dB	100 Ω TP	B8ZS
1	1	0	T1	399-533 ft / 2.4 dB	100 Ω TP	B8ZS
1	1	1	T1	533-655 ft / 3.0 dB	100 Ω TP	B8ZS

1. When enabled.

Digital Data Interface

In either Host or Hardware Control Mode the recovered data goes to the Loss of Signal (LOS) Monitor. In Host Control Mode, it also goes through the Alarm Indication Signal (AIS, Blue Alarm) Monitor. The jitter attenuator circuit may be enabled or disabled in the receive data path or the transmit path. Received data may go through either the B8ZS or HDB3 decoder or neither. Finally, the device may send the digital data to the framer as either unipolar or bipolar data.

When transmitting unipolar data to the framer, the device reports receiving bipolar violations by driving the BPV pin High. During E1 operation in Host Control Mode, the device can report HDB3 code violations and Zero Substitution Violations on the BPV pin. The diagnostics section explains these options in more detail.

JITTER ATTENUATION

A Jitter Attenuation Loop (JAL) with an Elastic Store (ES) provides jitter attenuation as shown in the Test Specifications section. The JAL requires no special circuitry, such as an external quartz crystal or high-frequency clock (higher than the line rate). Its timing reference is the master clock, MCLK.

In Hardware Control Mode the ES is a 32 x 2-bit register. Setting the JASEL pin High places the JA circuitry in the received data path; setting JASEL Low places the JA in the transmit data path; leaving it open disables the JA.

In Host Mode, bit CR1.JASEL0 enables or disables the JA circuit. With bit CR1.JASEL0 = 1, bit CR1.JASEL1 controls the JA circuit placement (see Table 17). The ES can be either a 32 x 2-bit or 64 x 2-bit register depending on the value of bit CR3.ES64 (see Table 19.)

The device clocks data into the ES using either TCLK or RCLK depending on whether the JA circuitry is in the transmit or receive data path, respectively. Data is shifted out of the elastic store using the dejittered clock from the JAL. When the FIFO is within two bits of overflowing or underflowing, the ES adjusts the output clock by $^1/_8$ of a bit period. The ES produces an average delay of 16 bits (or 32 bits, with the 64-bit ES option selected in Host Control Mode) in the associated data path. When the Jitter Attenuator is in the receive path, the output RCLK transitions smoothly to MCLK in the event of an LOS condition.

The Transition Status Register bits TSR.ESOVR and TSR.ESUNF indicate an overflow or underflow, respectively in the ES. These are sticky bits: Once set to 1, they remain set until the host reads the register. The ES can also provide a maskable interrupt on either overflow or underflow.

DIAGNOSTIC MODE OPERATION

LXT350/351 offers multiple diagnostic modes as shown in Table 13. In Hardware Mode, the diagnostic modes are selected by a combination of pin settings. In Host Mode, the diagnostic modes are selected by writing appropriate bits in the Diagnostic Control Register.

Table 13: Diagnostic Mode Availability

Diagnostic Mode	Availability[1]		Host Mode[2] Maskable
	H/W	Host	
Loopback Modes			
Local Loopback (LLOOP)	Yes	Yes	No
Analog Loopback (ALOOP)	Yes	Yes	No
Remote Loopback (RLOOP)	Yes	Yes	No
Dual Loopback (DLOOP)	Yes	Yes	No
Internal Data Pattern Generation and Detection			
Transmit All Ones (TAOS)	Yes	Yes	No
Quasi-Random Signal Source (QRSS)	Yes	Yes	Yes
Error Insertion and Detection			
Bipolar Violation Insertion (INSBPV)	Yes	Yes	No
Logic Error Insertion (INSLER)	Yes	Yes	No
Bipolar Violation Detection (BPV)	Yes	Yes	No
Logic Error Detection, QRSS (QPD)	Yes	Yes	No
HDB3 Code Violation Detection (CODEV)	No	Yes	No
HDB3 Zero violation Detection (ZEROV)	No	Yes	No
Alarm Condition Monitoring			
Receive Loss of Signal (LOS) Monitoring	Yes	Yes	Yes
Receive Alarm Indication Signal (AIS) Monitoring	No	Yes	Yes
Transmit Driver Failure Monitoring—Open (DFMO)	No	Yes	Yes
Elastic Store Overflow and Underflow Monitoring	No	Yes	Yes
Built-In Self Test (BIST)	No	Yes	Yes

1. In Hardware Control Mode, a combination of pin settings selects the Diagnostic Modes; in Host Control Mode, writing appropriate bits into the Control Registers selects the Diagnostic Modes.
2. Host Control Mode allows interrupt masking by writing a "1" to the corresponding bit in the Interrupt Clear Register. Hardware Control Mode has no interrupt masking feature.

LOOPBACK MODES

NOTE

Hardware Mode pins discussed in this section refer to the LXT350 only.

Local Loopback

See Figures 5 and 6. In Hardware Mode, Local Loopback (LLOOP) is selected by tying LLOOP High; in Host Mode, by setting CR2.ELLOOP to 1. LLOOP inhibits the receiver circuits. The transmit clock and data inputs (TCLK and TPOS/TNEG or TDATA) loop back through the jitter attenuator (if enabled) and show up at RCLK and RPOS/RNEG or RDATA. (During LLOOP, the JASEL input is strictly an Enable/Disable control; it does not affect the placement of the JAL. If JA is enabled, it is active in the loopback circuit. If JA is bypassed, it is not active in the loopback circuit.)

The transmitter circuits are unaffected by LLOOP. LXT350/351 transmits the TPOS/TNEG or TDATA inputs (or a stream of 1s if TAOS is asserted) normally. When used in this mode, the transceiver can function as a stand-alone jitter attenuator.

Figure 5: TAOS with LLOOP (JA Selected)

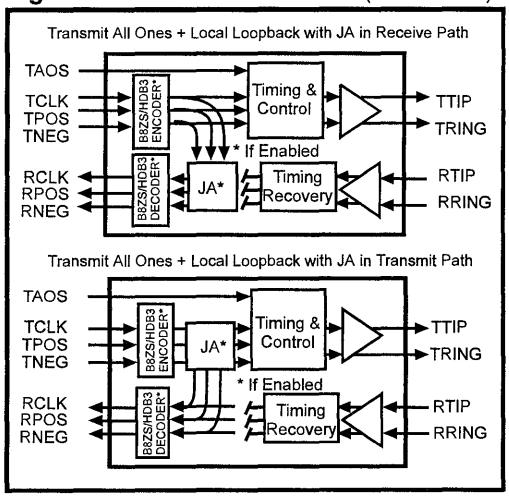
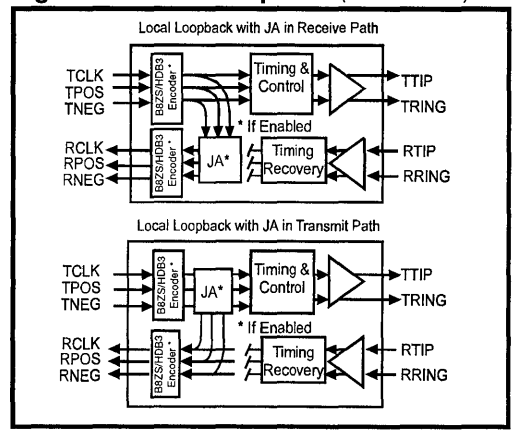


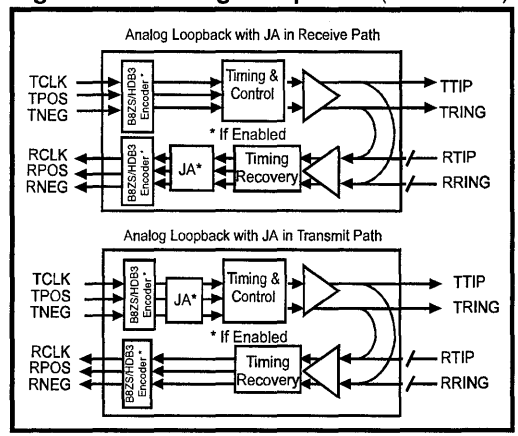
Figure 6: Local Loopback (JA Selected)



Analog Loopback

See Figure 7. Analog Loopback (ALOOP) exercises the maximum number of functional blocks. ALOOP operation disconnects the RTIP/RRING inputs from the line and routes the transmit outputs back into the receive inputs. This tests the encoders/decoders, jitter attenuator, transmitter, receiver and timing recovery sections. In Hardware Mode, leaving pin 27 open commands Analog Loopback; in Host Mode, writing a 1 to bit CR2.EALOOP enables the function. The ALOOP function overrides all other loopback modes.

Figure 7: Analog Loopback (JA Selected)



Remote Loopback

See Figure 8. In Remote Loopback (RLOOP) mode, the device ignores the transmit data and clock inputs (TCLK and TPOS/TNEG or TDATA), and bypasses the in-line encoders/decoders. The RPOS/RNEG or RDATA outputs loop back through the transmit circuits to TTIP and TRING at the RCLK frequency. The RLOOP command does not affect the receiver circuits which continue to output the RCLK and RPOS/RNEG or RDATA signals received from the twisted-pair line. In Host Mode, command RLOOP by writing a 1 to bit CR2.ERLOOP. In Hardware Mode, RLOOP is commanded by setting pin 26 High.

Dual Loopback

See Figure 9. To select Dual Loopback (DLOOP), set both RLOOP and LLOOP High in Hardware Mode or set bits CR2.ERLOOP and CR2.ELLOOP to 1 in Host Mode. In DLOOP mode, the transmit clock and data inputs (TCLK and TPOS/TNEG or TDATA) loop back through the Jitter Attenuator (unless disabled) to RCLK and RPOS/RNEG or RDATA. The data and clock recovered from the line loop back through the transmit circuits to TTIP and TRING without jitter attenuation.

Figure 8: Remote Loopback (JA Selected)

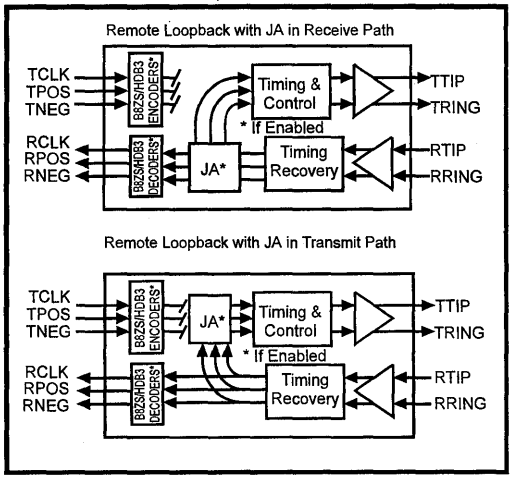
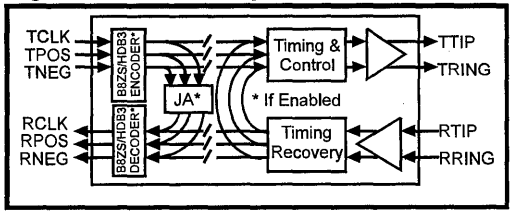


Figure 9: Dual Loopback

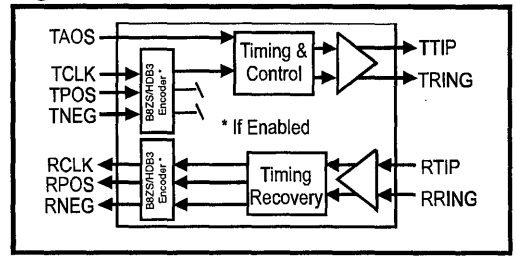


INTERNAL PATTERN GENERATION AND DETECTION

Transmit All Ones

See Figure 10. In Transmit All Ones (TAOS) Mode the transceiver ignores the TPOS and TNEG inputs and transmits a continuous stream of 1s at the TCLK frequency. (With no TCLK, the TAOS output clock is MCLK.) This can be used as the Alarm Indication Signal (AIS–also called the Blue Alarm). In Host Mode, TAOS is commanded by writing a 1 to bit CR2.ETAOS. In Hardware Mode setting pin 28 High does so. Both TAOS and Local Loopback can occur simultaneously as shown in Figure 5, but Remote Loopback inhibits TAOS. When both TAOS and LLOOP are active, TCLK and TPOS/TNEG loop back to RCLK and RPOS/RNEG through the jitter attenuator (if enabled), and an all ones pattern goes to TTIP/TRING.

Figure 10: TAOS Data Path



Quasi-Random Signal Source (QRSS)

For T1 operation the Quasi-Random Signal Source (QRSS) is a 2^{20}-1 pseudo-random bit sequence (PRBS) with no more than 14 consecutive zeros. For E1 operation, QRSS is 2^{15}-1 PRBS with inverted output.

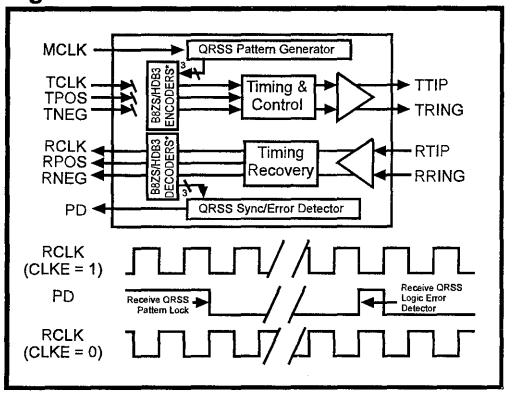
Both Hardware and Host Modes allow QRSS Mode. The QRSS pattern is normally locked to TCLK; but if there is no TCLK, MCLK is the clock source. Bellcore Pub 62411 defines the T1 QRSS transmit format and ITU G.703 defines the E1 format.

Leaving TAOS (pin 28) open enables QRSS transmission in Hardware Mode. In Host Mode, setting bits CR2.EPAT0 = 0 and CR2.EPAT1=1enables this function.

With QRSS transmission enabled, it is possible to insert a logic error into the transmit data stream by causing a Low-to-High transition on INSLER (pin 3). However, if no logic or bit errors are to be inserted into the QRSS pattern, INSLER must remain Low. Logic Error insertion waits until the next bit if the current bit is "jammed". (When there are more than 14 consecutive 0s, the output is jammed to a 1.)

Furthermore a bipolar violation in the QRSS pattern is possible by causing a Low-to-High transition on INSBPV (pin 4) without regard to whether the device is in bipolar or unipolar operating mode.

Figure 11: QRSS Mode



Choosing QRSS Mode also enables the QRSS Pattern Detection (QPD) in the receive path. The QRSS pattern is synchronized when there are fewer than four errors in 128 bits. After achieving synchronization the device drives QPD (pin 12) Low (QPD output is available on LXT350 only). The LXT351 does not support bit error detection in QRSS Mode. In the LXT350 QRSS Mode, any subsequent bit error in the QRSS pattern causes QPD to go High for half an RCLK clock cycle (the precise relationship to RCLK depends on the value of CLKE–when CLKE is Low, QPD goes High while RCLK is High; if CLKE is High, QPD goes High while RCLK is Low). This signal edge can serve as a trigger for an external bit-error counter. An LOS condition or a loss of QRSS synchronization will cause this output to go High continuously. In this case, and with either Unipolar Mode or the encoders/decoders enabled, the BPV pin indicates BPVs, CODEVs or ZEROVs as chosen.

Host Mode offers an additional interrupt to indicate that QRSS detection and sychronization have occurred, or that synchronization is lost. This interrupt is available when bit ICR.CQRSS = 0. If the QPD signal triggers a bit error counter, the interrupt could start or reset the counter.

Also in Host Mode, the PSR.QRSS bit provides an indication of the QRSS pattern synchronization. This bit goes Low with no QRSS pattern detected (*i.e.*, when there are more than four errors in 128 bits). The TQRSS bit in the Transition Status Register indicates that QRSS status has changed since the last QRSS Interrupt Clear command.

ERROR INSERTION AND DETECTION

Bipolar Violation Insertion (INSBPV)

In Unipolar Mode, both Hardware and Host Modes provide for Bipolar Violation Insertion (INSBPV). Choosing Unipolar Mode configures pin 4 as INSBPV. Bipolar violation insertion requires a Low-to-High transition on INSBPV. Sampling occurs on the falling edge of TCLK. When INSBPV goes High a BPV is inserted on the next available mark except in the three following situations:

- Zero suppression (HDB3 or B8ZS) is not violated
- If LLOOP and TAOS are both active, the BPV is looped back to RNEG/BPV indicator and the line driver transmits all ones with no violation.
- BPV insertion is disabled with RLOOP (remote loopback) active.

With the LXT350/351 configured to transmit internally generated QRSS data patterns a BPV can be inserted on the transmit pattern independent of whether the device is in the unipolar or bipolar mode of operation.

Logic Error Insertion (INSLER)

When configured to transmit internally generated QRSS data patterns, the device can insert a logic error on the transmit data pattern when there is a Low-to-High transition on INSLER. The transceiver treats data patterns the same way it treats data applied to TPOS/TNEG, so the inserted logic error will follow the data flow path as defined by the loopback mode in effect.

Logic Error Detection (QPD) (LXT350 Only)

After receiving pattern synchronization when configured in the QRSS Mode, LXT350 reports logic errors on QPD (pin 12). To indicate a logic error, this pin goes High for half an RCLK cycle (during the High period of RCLK if CLKE is Low but during the Low RCLK period if CLKE is High). To monitor logic errors, connect an error counter to QPD. A continuous High level on this pin indicates loss of either the QRSS pattern lock or LOS condition. The QRSS section has additional details on QRSS pattern lock criteria.

Bipolar Violation Detection (BPV)

With the internal encoders/decoders enabled or when configured in Unipolar Mode, the LXT350/351 reports received Bipolar Violations at BPV (pin 6). The pin goes High for a full clock cycle to indicate receipt of a BPV. However, if the encoders/decoders are enabled, LXT350/351 does not report bipolar violations due to the line coding scheme.

HDB3 Code Violation Detection (CODEV)

LXT350/351 can detect HDB3 code violations in Host Mode with HDB3 encoders enabled. This requires CR1.ENCENB = 1 and CR1.EC3-1 = 000, 001 or 010, which establishes E1 operation. To enable CODEV, set bit CR4.CODEV = 1.

An HDB3 code violation (CODEV) occurs when the device receives two consecutive bipolar violations of the same polarity (refer to ITU O.161). With CODEV detection enabled, LXT350/351 reports a violation on the BPV pin along with received BPVs and ZEROVs (if these options are enabled). LXT350/351 forces the BPV pin High for a full RCLK cycle to report a CODEV.

HDB3 Zero Substitution Violation Detection (ZEROV)

With encoders/decoders enabled, the LXT350/351 can detect HDB3 zero substitution violations (ZEROV) in Host Mode. This requires CR1.ENCENB = 1 and CR1.EC3-1 = 000, 001, or 1010, which establish E1 operation, and CR4.ZEROV = 1.

LXT350/351 forces the BPV pin High for a full RCLK cycle to report a ZEROV. An HDB3 ZEROV is the receipt of four or more consecutive zeros. This does not occur with correctly encoded HDB3 data unless there are transmission errors. With ZEROV detection enabled, the device reports a violation on the BPV pin along with received BPVs and CODEVs (if these options are enabled).

ALARM CONDITION MONITORING

Loss of Signal (LOS)

The LXT350/351 Loss of Signal (LOS) monitor function is compatible with ITU G.775 and ETSI 300233. They use a combination analog and digital detection scheme. The receiver LOS monitor loads a digital counter at the RCLK frequency. The counter increments with each received 0 and it resets to 0 on receipt of a 1. Any signal that remains 25 dB typical below the nominal 0dB signal for n consecutive pulse generates an internal LOS condition. For T1 operations, n = 175; for E1 operations, n = 32. In Host Mode, either number can be changed to 2048 by setting bit CR4.LOS2048 to 1. MCLK replaces the recovered clock at the RCLK output in a smooth transition.

For T1 operation, when the received signal has 12.5% 1s density (16 marks in a sliding 128-bit period, with fewer than 100 consecutive 0s), the LOS flag returns Low and the recovered clock replaces MCLK at the RCLK output in another smooth transition.

For E1 operation, the LOS condition is cleared when the received signal rises above 25 dBtypical below the minimum 0 dB level and has 12.5% 1s density (four 1s in a sliding 32-bit window with fewer than 16 consecutive 0s). In Host Mode E1 operation, the out-of-LOS criterion can be modified from 12.5% marks density to 32 consecutive marks by setting bit CR4.COL32CM = 1.

During LOS, the device sends received data to the RPOS/RNEG pins (or RDATA in Unipolar Mode). LXT350 reports an LOS condition on the LOS pin in Hardware Mode. In Host Mode, the LOS bit in the Performance Status Register goes High to indicate an LOS condition and will interrupt the host controller if so programmed.

Alarm Indication Signal Detection (AIS)

The Alarm Indication Signal (AIS) is available only in Host Mode. The receiver detects an AIS pattern when it receives fewer than three 0s in any string of 2048 bits. The device clears the AIS condition when it receives three or more 0s in a string of 2048 bits.

The AIS bit in the Performance Status Register indicates AIS detection. When the AIS status changes, the TAIS bit in the Transition Status Register goes High. The change of status interrupts the host controller by pulling $\overline{INT}$ Low, unless the interrupt is masked. Writing a 1 to the ICR.CAIS bit masks the interrupt until the bit returns to 0.

Driver Failure Mode Open (DFMO)

In Host Mode a DFM Open (DFMO) bit is available in the Performance Status Register to indicate an open condition on the lines. DFMO can generate an $\overline{INT}$ to the host controller. The Transition Status Register bit DFMO indicates a transition in the status of the bit. Writing a 1 to ICR.CDFMO will clear or mask the interrupt.

Elastic Store Overflow/Underflow (ESOVR/ESUNF)

When the bit count in the Elastic Store (ES) is within two bits of overflowing or underflowing the ES adjusts the output clock by $^1/_8$ of a bit period. In Host Mode, the ES provides an indication of overflow and underflow in the TRS.ESOVR and TSR.ESUNF. These are sticky bits and will stay set to 1 until the host controller reads the register. These interrupts can be cleared or masked by writing a 1 to the bits ICR.CESO and ICR.CESU, respectively.

OTHER DIAGNOSTIC MODES

Built-In Self Test (BIST)

LXT350/351 provides a Built-In Self Test (BIST) capability in Host Mode. The BIST exercises the internal circuits

by providing an internal QRSS pattern, running it through the encoders and the transmit drivers then looping it back through the receive equalizer, Jitter Attenuator and decoders to the QRSS pattern detection circuitry. If all the blocks in this data path work correctly, the receive pattern detector locks onto the pattern. It then pulls $\overline{INT}$ Low and sets the following bits High:

- TSR.TQRSS
- PSR.QRSS
- PSR.BIST

The QPD pin (pin 12) also indicates completion status of the test. Starting the test forces this pin High. During the test, it remains High until the test finishes successfully at which time it goes Low.

OPERATING MODES

The LXT350/351 share many features. However, their control modes are very different.

- The LXT350 operates in either Hardware or (Serial Port) Host Mode
- The LXT351 operates in (Parallel Port) Host Mode only.

In the Hardware Mode (LXT350 only) individual pins control the transceiver.

The logic level at the MODE pin sets the LXT350 mode of operation. In Host Mode (LXT350/351), a microprocessor controls the device through a data interface. The LXT350 has a serial interface and the LXT351 uses a parallel interface.

Hardware Mode Operation (LXT350 Only)

The LXT350 operates in Hardware Mode when MODE is left open or set Low. In Hardware Mode individual pins access and control the transceiver. The outputs (RPOS/RNEG or RDATA) are valid on the rising edge of RCLK.

There are some advanced functions provided only in Host Mode. Interrupt ($\overline{INT}$), AIS detection indicator, DFM open indicator and CLKE functions are some of the features available in Host Mode.

Table 14: Control and Operational Mode Selection for LXT350 Transceiver

Input to Pin[1]		Mode of Operation						
Mode	TRSTE	Hardware	Software	Unipolar	Bipolar	AMI Enc/Dec	B8ZS/HDB3 Encoder/Decoder	All Outputs Tristated
Low	Low	On	Off	Off	On	Off[3]	Off	No
Low	High	On	Off	Off	On	Off[3]	Off	Yes
Low	Open	On	Off	On	Off	On	Off	No
High[2]	Low	Off	On	x	x	x	x	No
High[2]	High	Off	On	x	x	x	x	Yes
High[2]	Open	Off	On	x	x	x	x	No
Open	Low	On	Off	On	Off	Off	On	No
Open	High	On	Off	On	Off	Off	On	Yes
Open	Open	On	Off	On	Off	Off	On	No

1. Open is either a midrange voltage or the pin is floating
2. In Software Mode, the contents of register CR1 determine the operation mode.
3. Encoding is done externally.

Host Mode Operation

The LXT350 operates in Host Mode when MODE is set High. In Host Mode a microprocessor accesses and controls the transceiver through a data port using the internal registers. The outputs (RPOS/RNEG or RDATA) are valid on the rising edge of RCLK

In Host Mode there are eight control and status registers–five read/write and three read-only registers. The LXT350 accesses them through its serial interface (SIO). The LXT351 provides this access using an 8-bit parallel interface (PIO).

The host processor/controller can completely configure the device as well as get a full diagnostic/status report

through the SIO or PIO. Only the clocks and data for Bipolar Mode and BPV/Logic Error insertions for Unipolar or QRSS Mode need to be provided directly to the input pins. Similarly, the recovered clock, data, and BPV/Logic Error occurrences are available only at output pins. All other mode settings and diagnostic information are available through the data port.

Table 15 shows the address used by the SIO or PIO to access each register on the LXT350 or LXT351, respectively. Table 16 summarizes the control and status registers and labels each bit they contain. Tables 17 through 23 identify the bits in each register.

Table 15: Serial (LXT350) and Parallel (LXT351) Port Register Addresses

Register		Address[1]	
Name	Abbr	Serial Port (A7-A1)	Parallel Port (A7-A0)
Control #1	CR1	x010000	x010000x
Control #2	CR2	x010001	x010001x
Control #3	CR3	x010010	x010010x
Interrupt Clear	ICR	x010011	x010011x
Transition Status	TSR	x010100	x010100x
Performance Status	PSR	x010101	x010101x
Control #4	CR4	x010111	x010111x

1. x = "don't care".

Table 16: Register Addresses and Bit Names

Register		Type	Bit							
Name	Sym		7	6	5	4	3	2	1	0
Control #1	CR1	R/W	JASLE1	JASEL0	ENCEB	UNIENB	*reserved*[2]	EC3	EC2	EC1
Control #2	CR2	R/W	RESET	EPAT1	EPAT0	ETAOS	*reserved*[2]	EALOOP	ELLOOP	ERLOOP
Control #3	CR3	R/W	JA6HZ	PCLKE[1]	SBIST	*reserved*[2]	*reserved*[2]	ES64	ESCEN	ESJAM
Interrupt Clear	ICR	R/W	CESU	CESO	CDFMO	*reserved*[3]	CQRSS	CAIS	*reserved*[3]	CLOS
Transition Status	TSR	R	ESUNF	ESOVR	TDFMO	*reserved*[2]	TQRSS	TAIS	*reserved*[2]	TLOS
Performance Status	PSR	R	*reserved*[2]	BIST	DFMO	*reserved*[2]	QRSS	AIS	*reserved*[2]	LOS
Control #4	CR4	R/W	*reserved*[2]	*reserved*[2]	*reserved*[2]	*reserved*[2]	COL32CM	LOS2048	ZEROV	CODEV

1. Bit CR3.PCLKE is available only in the LXT351; for the LXT350, set this bit to zero.
2. In write registers, bits labeled reserved should be set to 0 (except as in note 3 below) for normal operation and ignored in read only registers.
3. Write a 1 into this bit for normal operation.

Table 17: Control Register #1 Read/Write, Address (A7-A1) = x010000

Bit	Name	Function	Jitter Attenuation		
			JASEL0	JASEL1	Position
0	EC1	Set the Equalizer Control codes (see Table 12).	1	0	Transmit
1	EC2		1	1	Receive
2	EC3		0	X	disabled
3	—	*reserved, set this bit to 0, ignore when reading.*			
4	UNIENB	Enables Unipolar I/O Mode and insertion/detection of BPVs.			
5	ENCENB	Enables B8ZS/HDB3 encoders/decoders; device enters Unipolar Mode and pins 3, 4, 6 and 7 change to their unipolar functions.			
6	JASEL0	Jitter Attenuation Mode, selects jitter attenuation circuitry position in data path or disables it. See right hand section of table for values. ↗			
7	JASEL1				

Table 18: Control Register #2 Read/Write, Address (A7-A1) = x010001

Bit	Name	Function	Pattern		
			EPAT0	EPAT1	Selected
0	ERLOOP[1]	Enables Remote Loopback (RLOOP)	0	0	Transmit TPOS/TNEG
1	ELLOOP[1]	Enables Local Loopback (LLOOP)	0	1	Detect and transmit QRSS
2	EALOOP	Enables Analog Loopback (ALOOP)			
3	—	*reserved, set this bit to 0, ignore when reading.*			
4	ETAOS	Enables Transmit All Ones (TAOS)			
5	EPAT0	Enables internal data pattern transmission. See right hand section of table for values.			
6	EPAT1				
7	RESET	RESET = 1 resets device state and all registers.			

1. To enable Dual Loopback (DLOOP), set both ERLOOP = 1, ELLOOP = 1.

Table 19: Control Register #3 Read/Write, Address (A7-A1) = x010010

Bit	Name	Description
0	ESJAM	Disables Jamming of Elastic Store Read Out Clock ($^1/_8$ bit-time adjustment for over/underflow).
1	ESCEN	Centers ES pointer for a difference of 16 or 32 (depending on depth-clears automatically).
2	ES64	Increases ES depth from 32 to 64 bits.
3	—	*reserved–set to 0 for normal operation.*
4	—	*reserved–set to 0 for normal operation.*
5	SBIST	Starts Built-In Self Test.
6	PLCKE	This bit is meaningful only in the LXT351–*for LXT350, set this bit to 0.* PCLKE = 0 sets RPOS/RNEG valid on the rising edge of RCLK. PCLKE = 1 sets RPOS/RNEG valid on the falling edge of RCLK .
7	JA6HZ	When JA6HZ = 1, changes bandwidth of Jitter Attenuation Loop from 3 Hz (default) to 6 Hz.

Table 20: Interrupt Clear Register Read/Write, Address (A7-A1) = x010011

Bit	Name	Function[1]
0	CLOS	Clears/Masks LOS Interrupt.
1	—	*reserved, set this bit to 1* for normal operation.
2	CAIS	Clears/Masks AIS Interrupt.
3	CQRSS	Clears/Masks QRSS Interrupt.
4	—	*reserved–set this bit to 1 for normal operation.*
5	CDFMO	Clears/Masks DFMO.
6	CESO	Clears/Masks ES Overflow Interrupt.
7	CESU	Clears/Masks ES Underflow Interrupt.

1. Leaving a one in any of these bits masks the associated interrupt.

Table 21: Transition Status Register Read Only, Address (A7-A1) = x010100

Bit	Name	Function
0	TLOS	Loss of Signal (LOS) has changed since last clear LOS interrupt occurred.
1	—	*reserved-ignore.*
2	TAIS	AIS has changed since last clear AIS interrupt occurred.
3	TQRSS	QRSS has changed since last clear QRSS interrupt occurred[1].
4	—	*reserved-ignore.*
5	TDFMO	DFMO has changed since last clear DFMS interrupt occurred.
6	ESOVR	ES overflow status sticky bit[2].
7	ESUNF	ES underflow status sticky bit[2].

1. A QRSS transition indicates receive QRSS pattern sync or loss. A simple error in QRSS pattern is not reported as a transition.
2. Tripping the overflow or underflow indicator in the ES sets the ESOVR/ESUNF status bit(s). Reading the Transition Status Register clears these bits. Setting CESO and CESU in the Interrupt Clear Register masks these interrupts.

Table 22: Performance Status Register Read Only, Address (A7-A1) = x010101

Bit	Name	Function
0	LOS	Loss of Signal (LOS) Status.
1	—	*reserved-ignore.*
2	AIS	Alarm Indicator (AIS) Status.
3	QRSS	QRSS Pattern Detect Status.
4	—	*reserved–ignore.*
5	DFMO	Driver Open Indication.
6	BIST	Built-In Self Test Status.
7	—	*reserved–ignore*

Table 23: Control Register #4 Read/Write, Address (A7-A1) = x010111

Bit	Name	Function
0	CODEV	Enables detection of HDB3 code violation on the BPV pin along with bipolar violations and ZEROVs (as enabled).
1	ZEROV	Enables detection of four consecutive zeros (an HDB3 coding violation) on the BPV pin along with bipolar violation and ZEROVs (as enabled).
2	LOS2048	Changes LOS detection threshold from 32 consecutive zeros (for E1 operation) or 175 consecutive zeros (T1 operation) to 2048 consecutive zeros in either environment.
3	COL32CM	In E1 Mode, changes "clear LOS condition" criterion from 12.5% marks density (default) to receipt of 32 consecutive marks.
4	—	*reserved–set to 0 for normal operation; ignore when reading.*
5	—	*reserved–set to 0 for normal operation; ignore when reading.*
6	—	*reserved–set to 0 for normal operation; ignore when reading.*
7	—	*reserved–set to 0 for normal operation; ignore when reading.*

Serial Port Operation (LXT350 Only)

The LXT350 operates in Host Mode when the MODE pin is set High. Figure 12 shows the SIO data structure. The registers are accessible through a 16-bit word: an 8-bit Command/Address byte (bits R/$\overline{W}$ and A1-A7) and a subsequent 8-bit data byte (bits D0-7). Bit R/$\overline{W}$ determines whether a read or a write operation occurs. Bits A6-1 in the Command/Address byte address specific registers (the address decoder ignores bit A7). The data byte depends on both the value of bit R/$\overline{W}$ and the address of the register as set in the Command/Address byte.

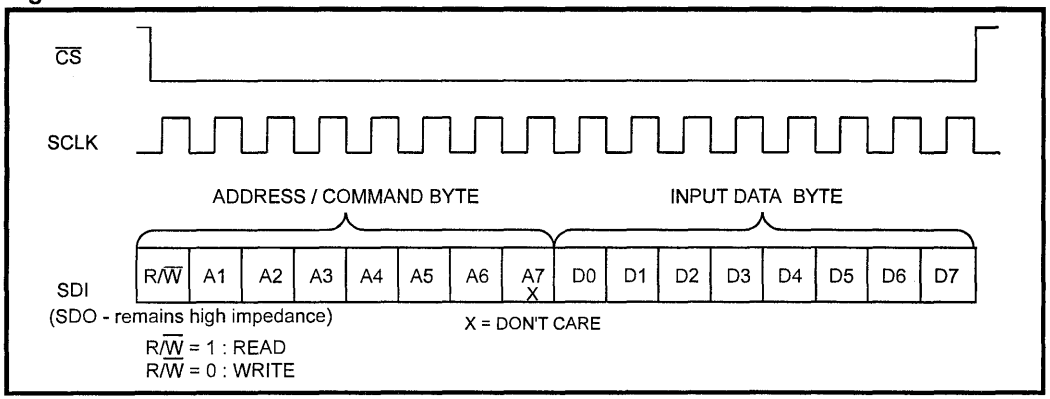
Host Mode provides a latched interrupt output ($\overline{INT}$). A change in the state of any of the following bits in the Performance Status Register will drive $\overline{INT}$ Low: LOS, AIS, QRSS, or DFMO. An interrupt will also occur when there is an elastic store overflow or underflow. When the interrupt has occurred, the $\overline{INT}$ output pin is pulled Low. The output stage of each $\overline{INT}$ pin consists only of a pull-down device, so each one requires an external pull-up resistor. The interrupt is cleared when the interrupt condition no longer exists, and the host processor writes a 1to the respective interrupt causing bit(s) in the Interrupt Register. Leaving a 1 in any of these interrupt status bits masks that interrupt.

Host Mode also allows control of the serial data and receive data output timing. The clock edge (CLKE) signal determines when the outputs are valid, relative to the Serial Clock (SCLK) or RCLK as shown in Table 24.

Table 24: CLKE Settings

CLKE	Output	Clock	Valid Edge
Low	RPOS	RCLK	Rising
	RNEG	RCLK	Rising
	SDO	SCLK	Falling
High	RPOS	RCLK	Falling
	RNEG	RCLK	Falling
	SDO	SCLK	Rising

Figure 12: LXT350 Serial Interface Data Structure



Parallel Port Operation (LXT351 Only)

The LXT351 address/control bus pins and control pins are compatible with both the Intel and Motorola address/data buses. See Figures 22 and 23 for the I/O timing diagram for each bus. The device automatically detects bus timing based on the Intel and Motorola microprocessor bus specifications. The maximum recommended processor speed for an Intel device is 20 MHz; for a Motorola device, 16.78 MHz. Table 17 summarizes the control and status registers for the LXT351. Tables 17 through 23 identify and explain the bits in the control registers.

The LXT351 provides a latched interrupt output ($\overline{INT}$). A change in the state of any of the following bits in the Performance Status Register will drive $\overline{INT}$ Low: LOS, AIS, QRSS, DFMO. When the interrupt has occurred, the $\overline{INT}$ output pin is pulled Low. The output stage of $\overline{INT}$ pin consists only of a pull-down device, so each pin requires an external pull-up resistor. The interrupt is cleared when the interrupt condition no longer exists, and the host processor writes a 1 to the respective interrupt causing bit(s) in the Interrupt Register. Leaving a 1 in any of these interrupt status bits masks that interrupt.

The received data output is valid on the rising edge of RCLK, when bit CR3.PCLKE = 0. The data output is valid on the falling edge of RCLK when CR3.PCLKE =1.

There are five read/write and three read-only registers. Only bits A6-1 in the address byte are valid. (The address decoder ignores bits A7 and A0.) Tables 17 through 23 show the register address bits A7-1, without regard to bit A0.

APPLICATION INFORMATION

NOTE

This application information is for design aid only.

Table 25 shows the specification for transmit return loss in E1 applications. (The G.703/CH PTT specification is a Swiss Telecommunications Ministry specification.)

Table 26 shows the transmit return loss values for T1 applications. Table 34 shows the receive return loss values.

Table 25: E1 Transmit Return Loss Requirements

Frequency Band	Return Loss	
	ETS 300 166	G.703/CH PTT
51-102 kHz	6 dB	8 dB
102-2048 kHz	8 dB	14 dB
2048 - 3072 kHz	8 dB	10 dB

Table 26: Transmit Return Loss (2.048 Mbps)

EC3-1	Xfrmr/ Rt	Rload (Ω)	Cl (pF)	Return Loss (dB)
000	1:2/ 9.1 Ω	75	0	14
			470	16
		120	0	12
			470	13
	1:2.3/ 9.1 Ω	120	0	13
			470	16

Table 27: Transmit Return Loss (1.544 Mbps)

EC3-1	Xfrmr/ Rt	Rload (Ω)	Cl (pF)	Return Loss (dB)
011[2]	1:2/ 9.1 Ω	100	0	16
			470	17
	1:1.15[1]/ 0.0 Ω	100	0	2
			470	2

1. A 1:1.15 transmit transformer keeps the total transceiver power dissipation at a low level, a 0.47 µF DC blocking capacitor must be placed on TTIP or TRING.
2. Refer to Table 12.

Table 28: Transformer Specifications for LXT350/LXT351

Tx/ Rx	Frequency MHz	Turns Ratio	Primary Inductance µH (minimum)	Leakage Inductance µH (max)	Interwinding Capacitance pF (max)	DCR Ω (maximum)	Dielectric[1] Breakdown V (minimum)
Tx	1.544	1:1.15	600	0.80	60	0.90 pri 1.70 sec	1500 VRMS
	2.048	1:2.3	600	0.80	60	0.70 pri 1.20 sec	1500 VRMS[2] (3000 VRMS)
	1.544/2.048	1:2	600	0.80	60	1.0 pri 1.70 sec	1500 VRMS[2] (3000 VRMS)
Rx	1.544/2.048	1:1	600	1.10	60	1.10 pri 1.10 sec	1500 VRMS[2] (3000 VRMS)

1. Some ETSI applications may require a 2.3 kV dielectric breakdown voltage.
2. Some applications require transformers to guarantee performance in extended temperature range (-40° to +85° C) ETSI applications require a dielectric breakdown voltage of 3000 VRMS.

Table 29: Recommended Transformers for LXT350/LXT351

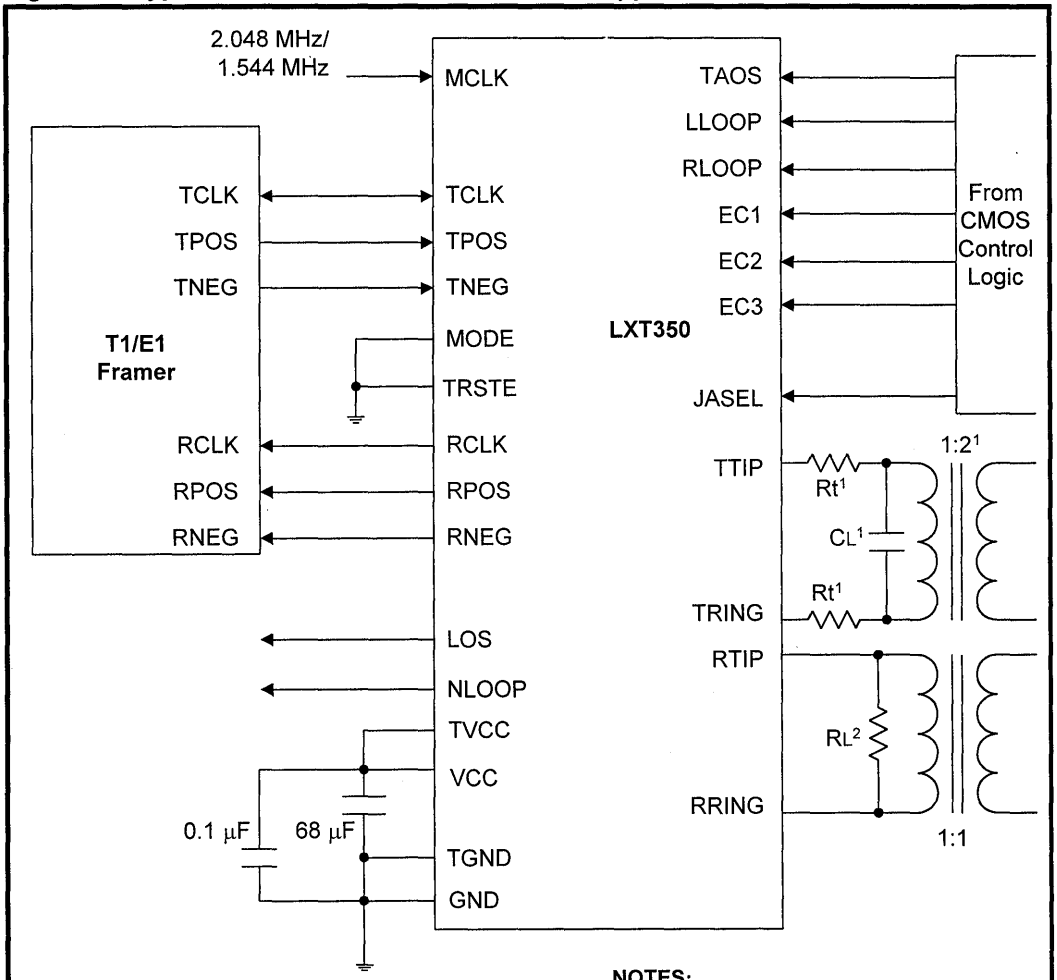
Tx/Rx	Turns Ratio	Part Number	Manufacturer
Tx	1:1.15	PE-65388	Pulse Engineering
		PE-65770	
		16Z5952	Vitec
	1:2	PE-65351	Pulse Engineering
		PE-65771	
		0553-5006-IC	Bell-Fuse
		66Z-1308	Fil-Mag
		671-5832	Midcom
		67127370	Schott Corp
		67130850	
		TD61-1205D	HALO (combination Tx/Rx set)
		TG26-1205NI	HALO (surface mount dual transformer 1CT:2CT & 1CT:2CT)
		TG48-1205NI	HALO (surface mount dual transformer 1CT:2CT & 1:1)
		16Z5946	Vitec
	1:2.3	PE-65558	Pulse Engineering
Rx	1:1	FE 8006-155	Fil-Mag
		671-5792	Midcom
		PE-64936	Pulse Engineering
		PE-65778	
		67130840	Schott Corp
		67109510	
		TD61-1205D	HALO (combination Tx/Rx set)

Figure 13 shows a typical LXT350 application in either or T1 or E1 environment. See Tables 26 through 31 to select the transformers (T1 and T2), resistors (Rt and Rl) and capacitors (Cl) needed for this application.

NOTE

If the application includes surge protection, such as a varistor or sidactor on the TTIP/TRING lines, it may also require reducing the value of the capacitor CL or eliminating it completely. Excessive capacitance at CL will distort the transmitted signals.

Figure 13: Typical T1/E1 LXT350 Hardware Mode Application



NOTES:

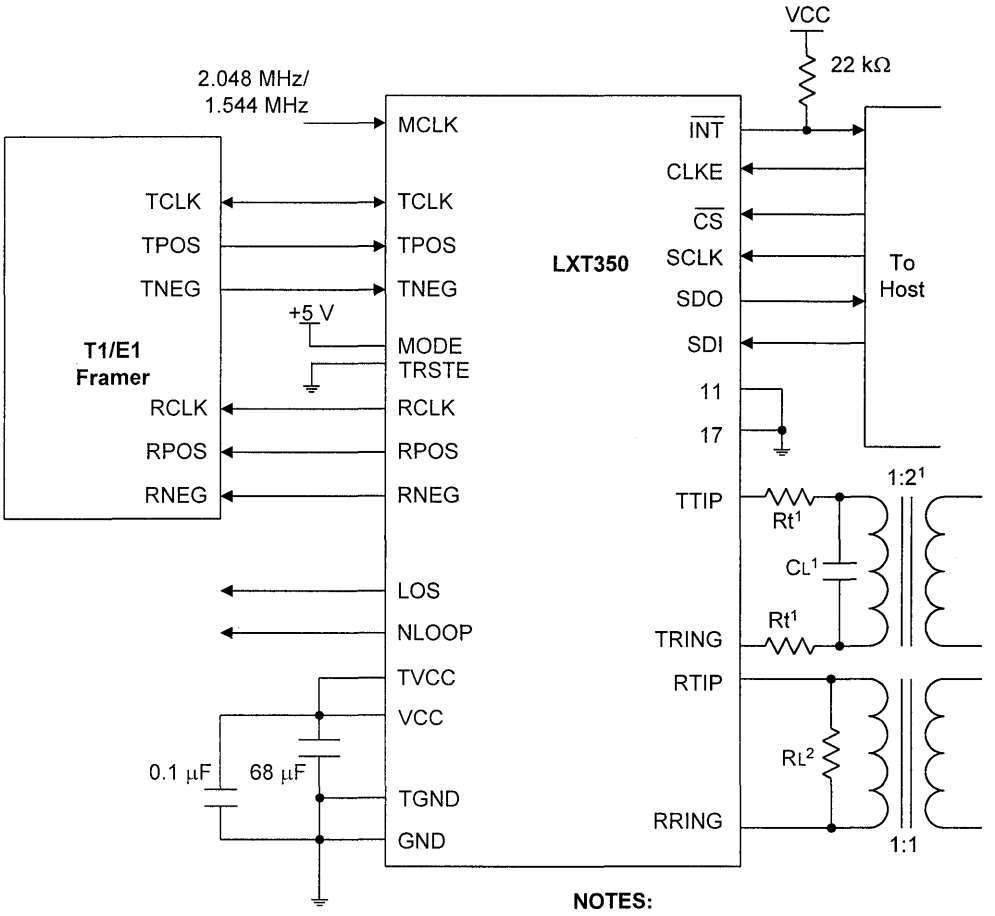
1. See Tables 26, 27 for Cl, Rt and Transformer selection..
2. RL = 100 Ω for T-1
   RL = 120 Ω for E-1/120 Ω twisted pair
   RL = 75 Ω for E-1/75 Ω coax

Figure 14 shows an application using the LXT350 in its Host Controlled Mode. See Tables 26 through 27 to select the transformers (T1 and T2), resistors (Rt and Rl) and capacitors (Cl) needed for this application.

NOTE

If the application includes surge protection, such as a varistor or sidactor on the TTIP/TRING lines, it may also require reducing the value of the capacitor CL or eliminating it completely. Excessive capacitance at CL will distort the transmitted signals.

Figure 14: Typical T1/E1 LXT350 Host Mode Application



NOTES:

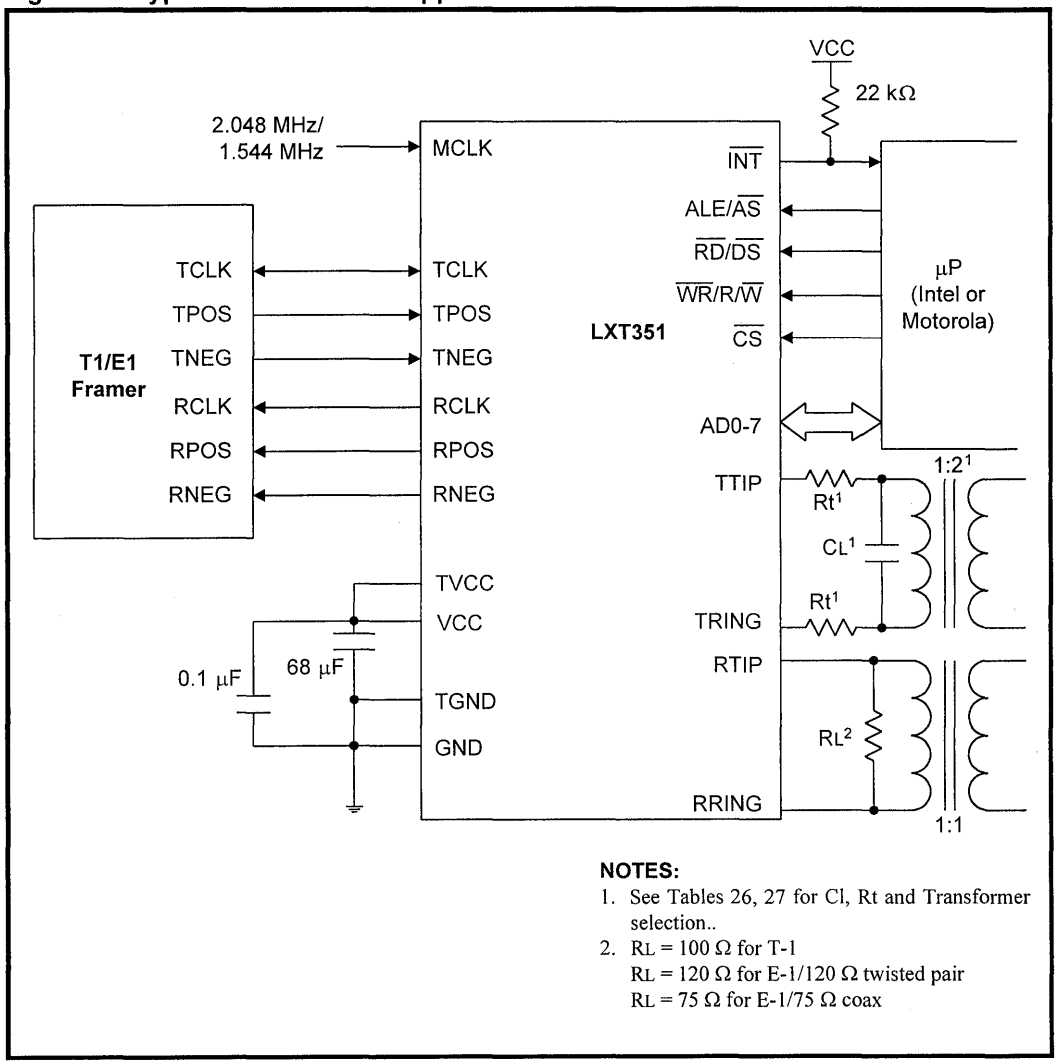
1. See Tables 26, 27 for Cl, Rt and Transformer selection..
2. RL = 100 Ω for T-1
   RL = 120 Ω for E-1/120 Ω twisted pair
   RL = 75 Ω for E-1/75 Ω coax

Figure 15 shows an application using the LXT351. See Tables 26 through 27 to select the transformers (T1 and T2), resistors (Rt and Rl) and capacitors (Cl) needed for this application.

NOTE

If the application includes surge protection, such as a varistor or sidactor on the TTIP/TRING lines, it may also require reducing the value of the capacitor CL or eliminating it completely.

Figure 15: Typical T1/E1 LXT351 Application



NOTES:

1. See Tables 26, 27 for Cl, Rt and Transformer selection..
2. RL = 100 Ω for T-1
   RL = 120 Ω for E-1/120 Ω twisted pair
   RL = 75 Ω for E-1/75 Ω coax

TEST SPECIFICATIONS

NOTE

The minimum and maximum values in Tables 30 to 42 and Figures 16 through 26 represent the performance specifications of the LXT350 and LXT351 and are guaranteed by test, except where noted by design.

Table 30: Absolute Maximum Ratings

Parameter	Sym	Min	Max	Units
DC supply (reference to GND)	VCC,TVCC	–	6.0	V
Input voltage, any pin [1]	VIN	GND -0.3 V	VCC + 0.3 V	V
Input current, any pin [2]	IIN	- 10	10	mA
Storage Temperature	TSTG	-65	150	°C

CAUTION

Operation at these limits may permanently damage the device.
Normal operation at these extremes not guaranteed.

1. TVCC and VCC must not differ by more than 0.3 V during operation. TGND and GND must not differ by more than 0.3 V during operation.
2. Transient currents of up to 100 mA will not cause SCR latch-up. TTIP, TRING, TVCC, and TGND can withstand continuous currents of up to 100 mA.

Table 31: Recommended Operating Conditions

Parameter		Sym	Min	Typ[1]	Max	Units	Test Conditions
DC Supply [2]		VCC,TVCC	4.75	5.0	5.25	V	
Ambient Operating Temperature		TA	- 40	25	85	° C	
Total Power Dissipation[3]	T1	PD	–	310	380	mW	100% mark density
		PD	–	225	295	mW	50% mark density
	E1	PD	–	275	330	mW	100% mark density
		PD	–	215	270	mW	50% mark density

1. Typical figures are at 25° C and are for design aid only; not guaranteed and not subject to production testing.
2. TVCC and VCC must not differ by more than 0.3 V.
3. Power dissipation while driving 75 Ω load over operating range for T1 operation or 60 Ω load for E1 operation. Includes power dissipation on device and load. Digital levels are within 10% of the supply rails and digital outputs driving a 50 pF capacitive load.

Table 32: LXT350 DC Electrical Characteristics (over recommended operating range)

Parameter		Sym	Min	Typ	Max	Units	Test Conditions
Digital I/O Pins							
High level input voltage [1,2] (pins 1-4, 23-25)[4]		VIH	2.0	–	–	V	
Low level input voltage [1,2] (pins 1-4, 23-25)[4]		VIL	–	–	0.8	V	
High level output voltage [1,2] (pins 6-8, 12, 23, 25)[4]		VOH	2.4	–	–	V	IOUT = -400 µA
Low level output voltage [1,2] (pins 6-8, 12, 23, 25)[4]		VOL	–	–	0.4	V	IOUT = 1.6 mA
Tri-state leakage current [1] (all outputs)		I3L	0	–	±10	µA	
Mode Input Pins							
High level input voltage [3] (pins 5, 9, 11, 26-28)[4]		VIH	3.5	–	–	V	
Midrange output voltage [3] (pins 5, 9, 11, 26-28)[4]		VOM	2.3	–	2.7	V	
Low level input voltage [3] (pins 5, 9, 11, 26-28)[4]	Host Mode H/W Mode	VIL VIL	– –	– –	0.8 1.5	V V	
Input leakage current (pins 5, 9, 11, 26-28)[4]		ILL	0	–	±50	µA	
Tri-state Leakage current[1] (all outputs)		I3L	0	–	±10	µA	
TTIP/TRING Leakage current		ITR	–	–	1.2	mA	In power down and tristate

1. Functionality of pin 23 and 25 depends on mode. See Host Mode and Hardware Mode description
2. Output drivers will output CMOS logic levels into CMOS loads.
3. As an alternative to supplying 2.3 - 2.7 V to these pins, they may be left open.
4. Listed pins are for 28-pin DIP and PLCC packages. Refer to I/O description for 44-pin QFP package.

Table 33: LXT351 DC Electrical Characteristics (over recommended operating range)

Parameter	Sym	Min	Typ	Max	Units	Test Conditions
Digital I/O Pins						
High level input voltage [1,2] (pins 1-5, 9-12, 17, 23-28)[3]	VIH	2.0	–	–	V	
Low level input voltage [1,2] (pins 1-5, 9-12, 17, 23-28)[3]	VIL	–	–	0.8	V	
High level output voltage [1,2] (pins 6-8, 10, 11,23, 28)[3]	VOH	2.4	–	–	V	IOUT = -400 µA
Low level output voltage [1,2] (pins 6-8, 10, 11,23, 28)[3]	VOL	–	–	0.4	V	IOUT = 1.6 mA
Input leakage current	ILL	–	–	±10	µA	

1. Functionality of pins 23 and 25 depends on mode. See Host Mode description.
2. Output drivers will output CMOS logic levels into CMOS loads.
3. Listed pins are for 28-pin DIP and PLCC packages. Refer to I/O description for 44-pin QFP package.

Table 34: Analog Characteristics (over recommended operating range)

Parameter		Min	Typ[1]	Max	Units	Test Conditions
Recommended output load on TTIP/TRING		50	–	200	Ω	
AMI Output Pulse Amplitudes	T1	2.4	3.0	3.6	V	R_L = 100 Ω
	E1	2.7	3.0	3.3	V	R_L = 120 Ω
Jitter added by the transmitter[2]	10 Hz - 8 kHz [3]	–	–	0.02	UI	
	8 kHz - 40 kHz [3]	–	–	0.025	UI	
	10 Hz - 40 kHz[3]	–	–	0.025	UI	
	Broad Band	–	–	0.05	UI	
Receiver Sensitivity		0	–	18	dB	@ 1024 kHz 1.431
Allowable consecutive zeros before LOS (T1)		160	175	190	–	
Allowable consecutive zeros before LOS (E1)		–	32	–	–	
Input jitter tolerance (T1)	10 kHz - 100 kHz	0.4	–	–	UI	0 dB line AT&T Pub 62411
	1 Hz[3]	138	–	–	UI	
Input jitter tolerance (E1)	10 kHz - 100 kHz	0.2	–	–	UI	0 dB line ITU (G.823)
	1 Hz[3]	37	–	–	UI	
Jitter attenuation curve corner frequency [4]		–	3	–	Hz	selectable in data port
Driver Output Impedance		–	3	–	Ω	
Receiver Input Impedance		–	40	–	kΩ	RTIP to RRING
Receive Return Loss (E1)	51 kHz - 102 kHz[3]	20	22	–	dB	
	102 kHz - 2.048 MHz[3]	20	28	–	dB	
	2.048 MHz - 3.072 MHz[3]	25	30	–	dB	

1. Typical figures are at 25° C and are for design aid only; not guaranteed and not subject to production testing.
2. Input signal to TCLK is jitter-free. The Jitter Attenuator is in the receive path or disabled.
3. Guaranteed by characterization; not subject to production testing.
4. Circuit attenuates jitter at 20 dB/decade above the corner frequency.

Figure 16: 2.048 Mbps E1 Pulse (See Table 35)

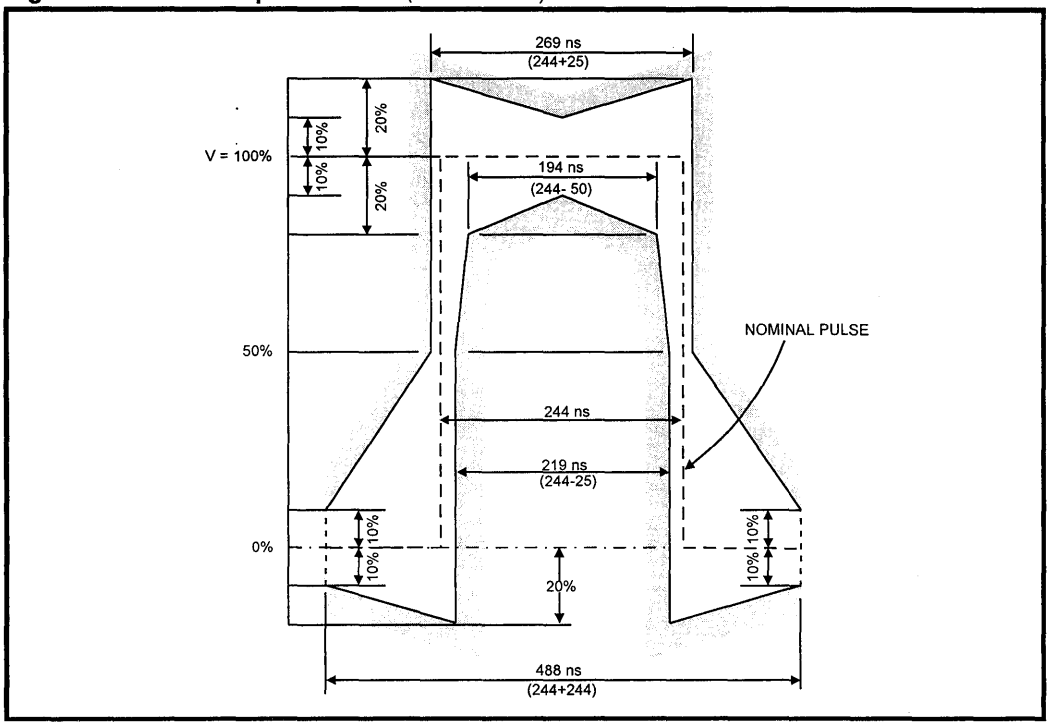


Table 35: 2.048 Mbps E1 Pulse Mask Specifications

Parameter	TPW	Coax	Unit
Test load impedance	120	75	Ω
Nominal peak mark voltage	3.0	2.37	V
Nominal peak space voltage	0 ±0.30	0 ±0.237	V
Nominal pulse width	244	244	ns
Ratio of positive and negative pulse amplitudes at center of pulse	95-105	95-105	%
Ratio of positive and negative pulse amplitudes at nominal half amplitude	95-105	95-105	%

Figure 17: 1.544 Mbps T1 Pulse (DSX-1) (See Table 36)

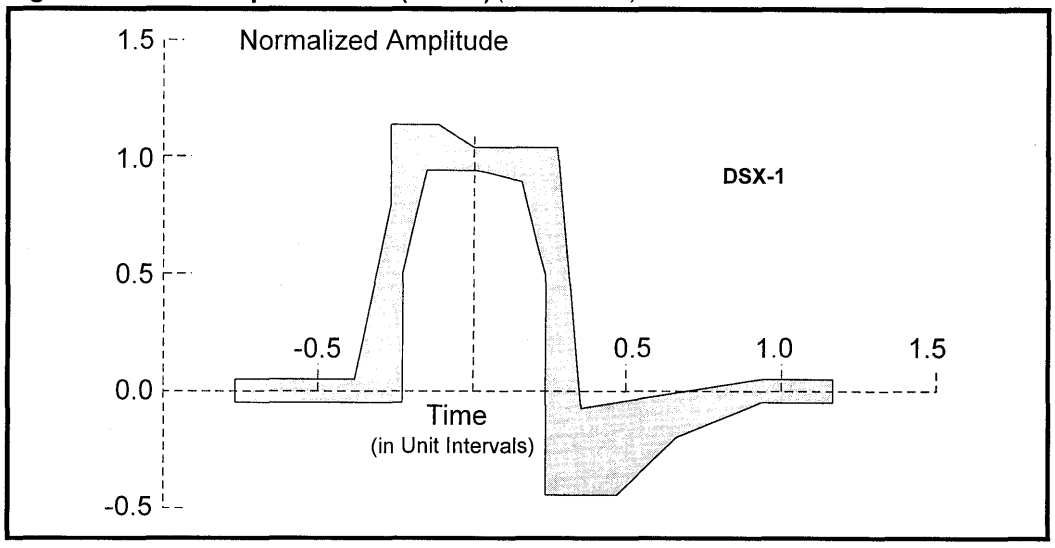


Table 36: 1.544 Mbps T1 (DSX-1) Pulse Mask Corner Point Specifications

DSX-1 Template *(per ANSI T1. 102-1993)*			
Minimum Curve		**Maximum Curve**	
Time *(UI)*	**Amplitude**	**Time** *(UI)*	**Amplitude**
-0.77	-0.05	-0.77	0.05
-0.23	-0.05	-0.39	0.05
-0.23	0.50	-0.27	0.80
-0.15	0.95	-0.27	1.15
0.0	0.95	-0.12	1.15
0.15	0.90	0.0	1.05
0.23	0.50	0.27	1.05
0.23	-0.45	0.35	-0.07
0.46	-0.45	0.93	0.05
0.66	-0.20	1.16	0.05
0.93	-0.05		
1.16	-0.05		

Table 37: Master and Transmit Clock Timing Characteristics for T1 Operation

(over recommended operating range) (see Figure 18)

Parameter	Sym	Min	Typ[1]	Max	Units	Notes
Master clock frequency	MCLK	–	1.544	–	MHz	must be supplied
Master clock tolerance	MCLKt	–	±32	–	ppm	
Master clock duty cycle	MCLKd	40	–	60	%	
Transmit clock frequency	TCLK	–	1.544	–	MHz	
Transmit clock tolerance	TCLKt	–	–	±100	ppm	
Transmit clock duty cycle	TCLKd	10	–	90	%	
TPOS/TNEG to TCLK setup time	tSUT	50	–	–	ns	
TCLK to TPOS/TNEG hold time	tHT	50	–	–	ns	

1. Typical figures are at 25° C and are for design aid only; not guaranteed and not subject to production testing.

Table 38: Master and Transmit Clock Timing Characteristics for E1 Operation

(see Figure 18)

Parameter	Sym	Min	Typ[1]	Max	Units	Notes
Master clock frequency	MCLK	–	2.048	–	MHz	must be supplied
Master clock tolerance	MCLKt	–	±32	–	ppm	
Master clock duty cycle	MCLKd	40	–	60	%	
Transmit clock frequency	TCLK	–	2.048	–	MHz	
Transmit clock tolerance	TCLKt	–	–	±100	ppm	
Transmit clock duty cycle	TCLKd	10	–	90	%	
TPOS/TNEG to TCLK setup time	tSUT	50	–	–	ns	
TCLK to TPOS/TNEG hold time	tHT	50	–	–	ns	

1. Typical figures are at 25° C and are for design aid only; not guaranteed and not subject to production testing.

Figure 18: Transmit Clock Timing

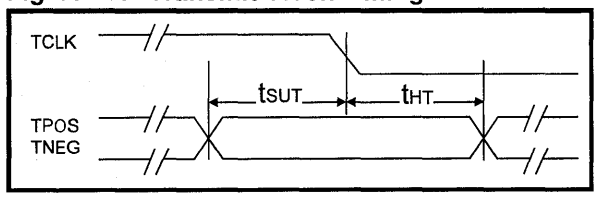


Table 39: Receive Timing Characteristics for T1 Operation (See Figure 19)

Parameter	Sym	Min	Typ[1]	Max	Units
Receive clock duty cycle [2, 3]	RLCKd	40	50	60	%
Receive clock pulse width [2, 3]	tPW	–	648	–	ns
Receive clock pulse width high	tPWH	–	324	–	ns
Receive clock pulse width low[1,3]	tPWL	260	324	388	ns
RPOS/RNEG to RCLK rising time	tSUR	–	274	–	ns
RCLK rising to RPOS/RNEG hold time	tHR	–	274	–	ns

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. RCLK duty cycle widths will vary according to extent of received pulse jitter displacement. Max and Min RCLK duty cycles are for worst case jitter conditions.
3. Worst case conditions guaranteed by design only.

Table 40: Receive Timing Characteristics for E1 Operation (See Figure 19)

Parameter	Sym	Min	Typ[1]	Max	Units
Receive clock duty cycle [2, 3]	RLCKd	40	50	60	%
Receive clock pulse width [2, 3]	tPW	–	488	–	ns
Receive clock pulse width high	tPWH	–	244	–	ns
Receive clock pulse width low[1,3]	tPWL	195	244	293	ns
RPOS/RNEG to RCLK rising time	tSUR	–	194	–	ns
RCLK rising to RPOS/RNEG hold time	tHR	–	194	–	ns

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. RCLK duty cycle widths will vary according to extent of received pulse jitter displacement. Max and Min RCLK duty cycles are for worst case jitter conditions (0.4 UI clock displacement for 1.544 MHz.)
3. Worst case conditions guaranteed by design only.

Figure 19: Receive Clock Timing

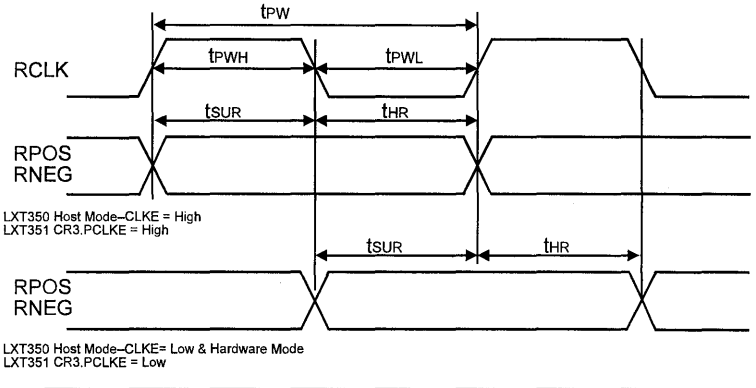


Table 41: LXT350 Serial I/O Timing Characteristics (See Figures 20 and 21)

Parameter	Sym	Min	Typ[1]	Max	Units	Parameter
Rise/fall time—any digital output	tRF	–	–	100	ns	Load 1.6 mA, 50 pF
SDI to SCLK setup time	tDC	50	–	–	ns	
SCLK to SDI hold time	tCDH	50	–	–	ns	
SCLK low time	tCL	240	–	–	ns	
SCLK high time	tCH	240	–	–	ns	
SCLK rise and fall time	tR, tF	–	–	50	ns	
$\overline{CS}$ falling edge to SCLK rising edge	tCC	50	–	–	ns	
Last SCLK edge to $\overline{CS}$ rising edge	tCCH	50	–	–	ns	
$\overline{CS}$ inactive time	tCWH	250	–	–	ns	
SCLK to SDO valid time	tCDV	–	–	200	ns	
SCLK falling edge or $\overline{CS}$ rising edge to SDO high-Z	tCDZ	–	100	–	ns	

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 20: LXT350 Serial Data Input Timing Diagram

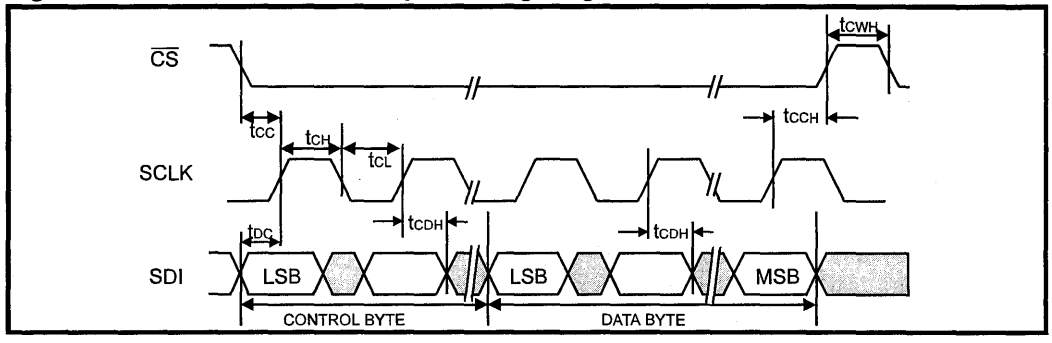


Figure 21: Serial Data Output Timing Diagram

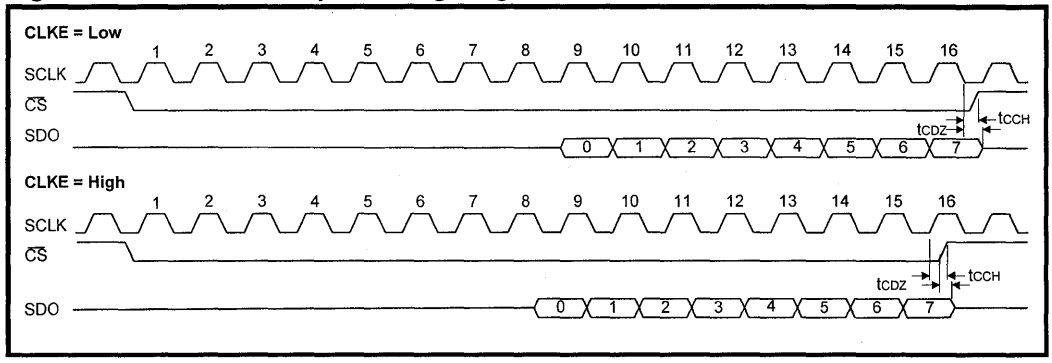


Table 42: LXT351 20 MHz Intel Bus Parallel I/O Timing Characteristics (See Figure 22)

Parameter	Sym	Min	Max	Units	Test Conditions
ALE pulse width	TLHLL	35	–	ns	
Address valid to ALE falling edge	TAVLL	10	–	ns	
ALE falling edge to address hold time	TLLAX	10	–	ns	
ALE falling edge to $\overline{RD}$ falling edge	TLLRL	10	–	ns	
ALE falling edge to $\overline{WR}$ falling edge	TLLWL	10	–	ns	
$\overline{CS}$ falling edge to $\overline{RD}$ falling edge	TCLRL	10	–	ns	
$\overline{CS}$ falling edge to $\overline{WR}$ falling edge	TCLWL	10	–	ns	
$\overline{RD}$ low pulse width	TRLRH	95	–	ns	
$\overline{RD}$ falling edge to data valid	TRLDV	10	55	ns	
Data hold time after $\overline{RD}$ rising edge	TRHDX	5	35	ns	
$\overline{RD}$ rising edge to ALE rising edge	TRHLH	15	–	ns	
$\overline{RD}$ rising edge to address valid	TRHAV	35	–	ns	
$\overline{CS}$ low hold time after $\overline{RD}$ rising edge	TRHCH	0	–	ns	
$\overline{WR}$ low pulse width	TWLWH	95	–	ns	
Data setup time before $\overline{WR}$ rising edge	TDVWH	40	–	ns	
Data hold time after $\overline{WR}$ rising edge	TWHDX	30	–	ns	
$\overline{WR}$ rising edge to ALE rising edge	TWHLH	15	–	ns	
$\overline{CS}$ low hold time after $\overline{WR}$ rising edge	TWHCH	15	–	ns	

Figure 22: LXT351 I/O Timing Diagram for Intel Address/Data Bus

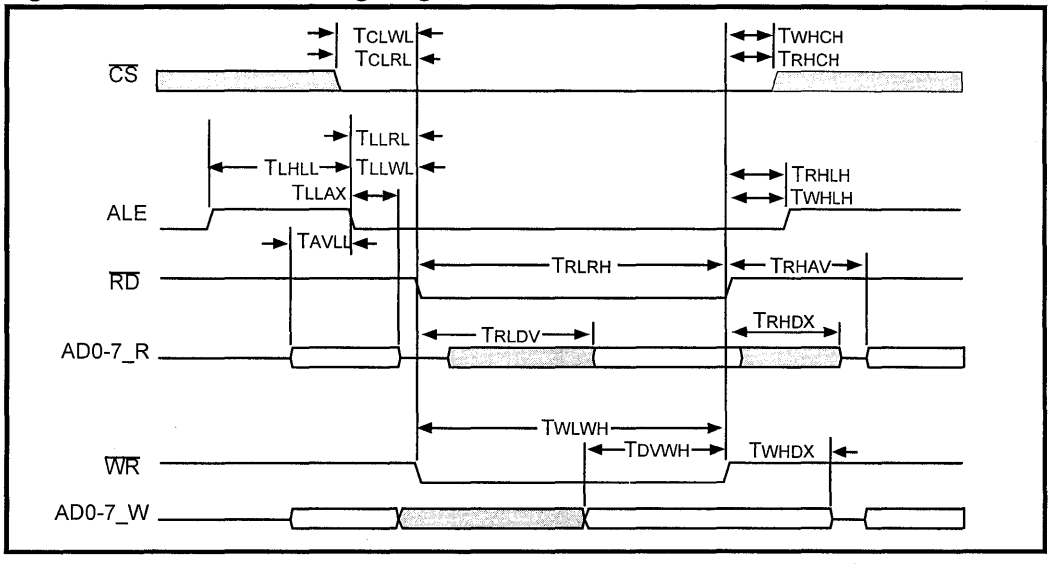


Table 43: LXT351 16.78 MHz Motorola Bus Parallel I/O Timing Characteristics

(See Figure 23)

Parameter	Sym	Min	Max	Units	Test Conditions
$\overline{DS}$ rising edge to $\overline{AS}$ rising edge	TDSHASH	15	–	ns	
$\overline{AS}$ high pulse width	TASHASL	35	–	ns	
Address valid setup time at $\overline{AS}$ falling edge	TAVASL	10	–	ns	
$\overline{AS}$ falling edge to Address valid hold time	TASLAX	10	–	ns	
$\overline{AS}$ falling edge to $\overline{DS}$ falling edge	TASLDSL	20	–	ns	
$\overline{CS}$ falling edge to $\overline{DS}$ falling edge	TCSLDSL	10	–	ns	
$\overline{DS}$ low pulse width	TDSLDSH	95	–	ns	
$\overline{DS}$ falling edge to data valid	TDSLDV	10	55	ns	
Data hold time after $\overline{DS}$ rising edge	TDSHDX	5	35	ns	
R/$\overline{W}$ falling edge to $\overline{DS}$ falling edge	TRWLDSL	10	–	ns	
Data setup time before $\overline{DS}$ rising edge	TDVDSH	40	–	ns	
Data hold time after DS rising edge	TDXDSH	30	–	ns	
R/$\overline{W}$ low hold time after $\overline{DS}$ rising edge	TDSHRWH	15	–	ns	
$\overline{CS}$ low hold time after $\overline{DS}$ rising edge	TDSHCSH	15	–	ns	

Figure 23: LXT351 I/O Timing Diagram for Motorola Address/Data Bus

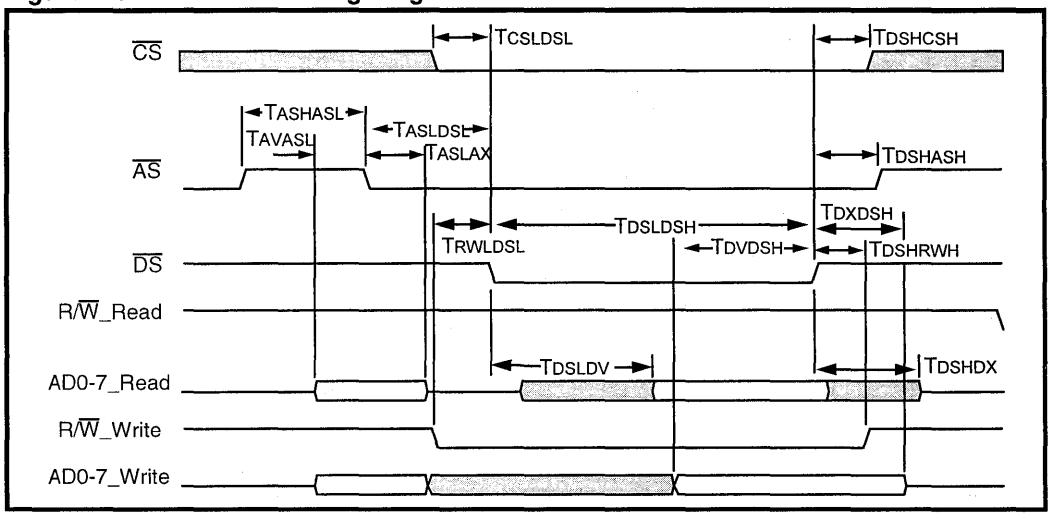
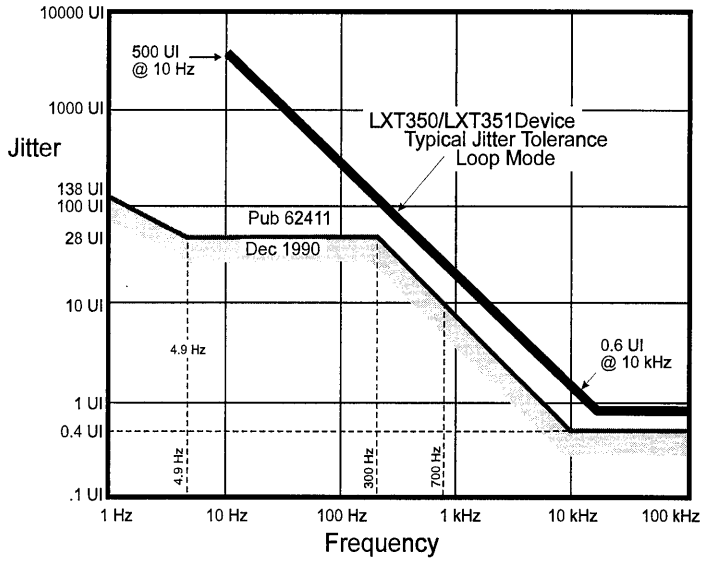


Figure 24: Input Jitter Tolerance (Typical)

Typical T1 Input Jitter Tolerance



Typical E1 Input Jitter Tolerance

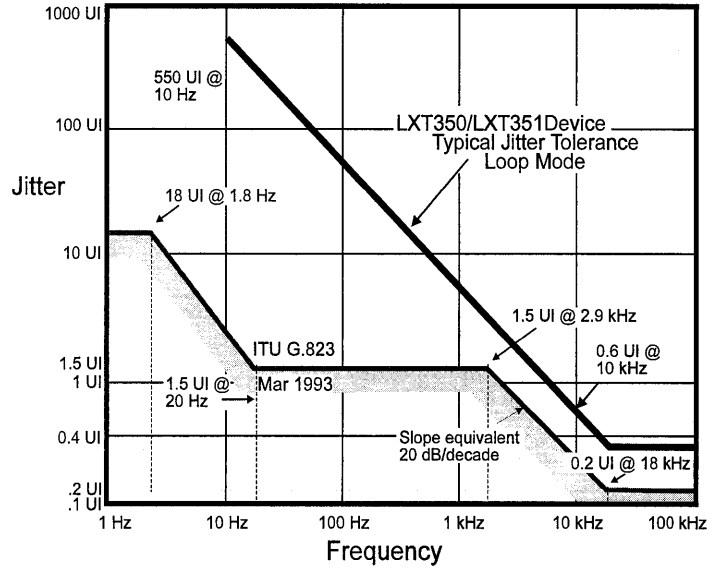


Figure 25: E1 Jitter Transfer Performance (Typical)

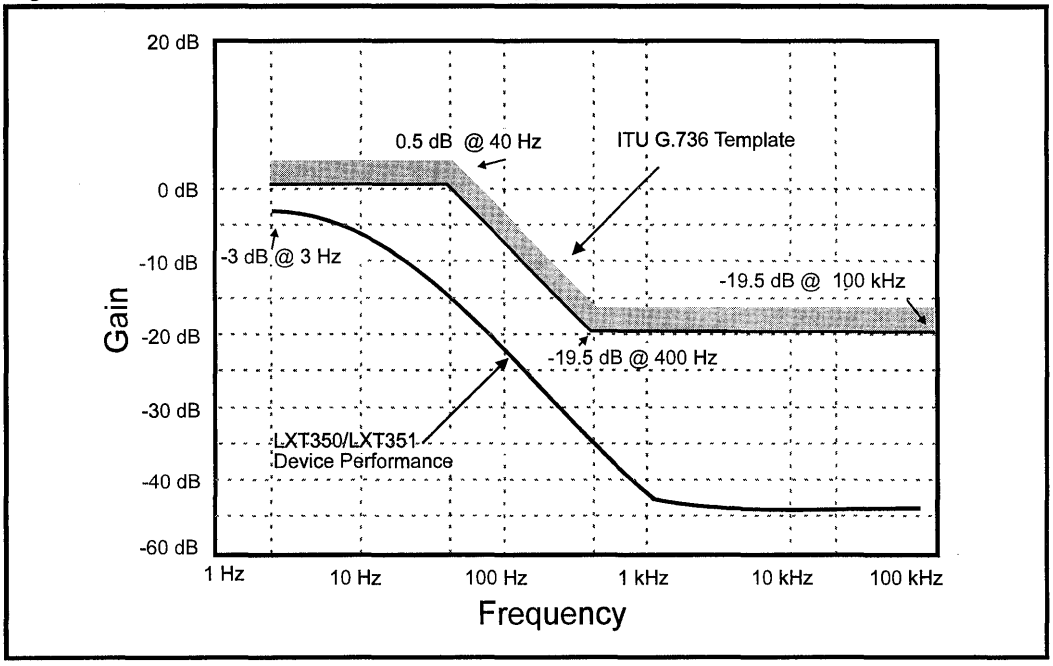
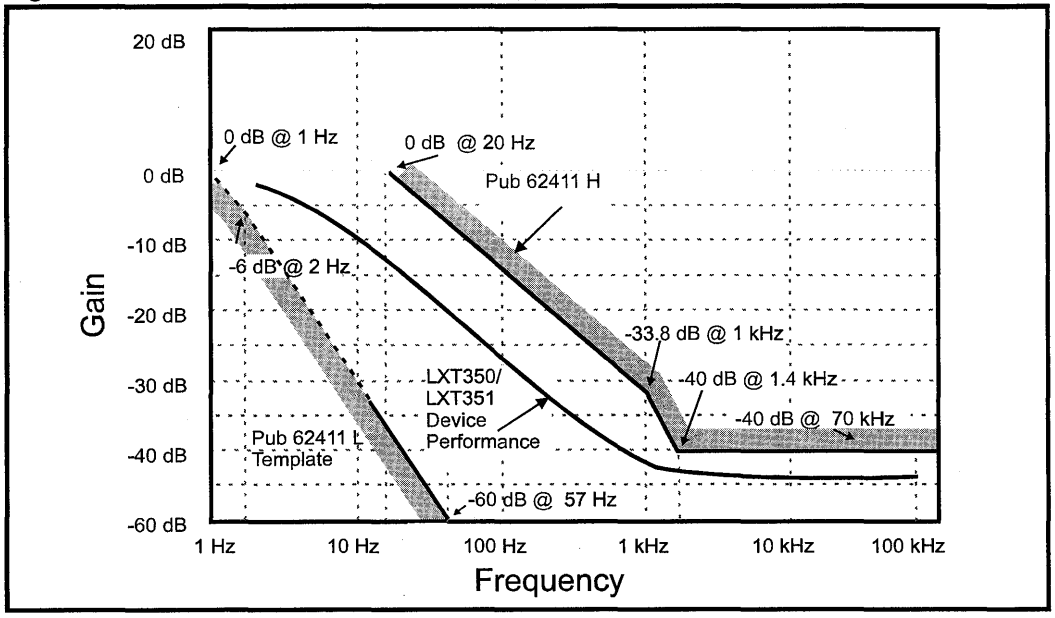


Figure 26: T1 Jitter Transfer Performance (Typical)



T1/E1 Long-Haul Transceivers

LXT310

T1 CSU/ISDN PRI Transceiver

General Description

The LXT310 is the first fully integrated transceiver for T1 CSU and ISDN Primary Rate Interface (ISDN PRI) applications at 1.544 Mbps. This transceiver operates over 6,000 feet of 22 AWG twisted-pair cable without any external components. To compensate for shorter lines, 7.5 dB, 15 dB, and 22.5 dB frequency-dependent transmit Line Build-Outs (LBOs) are provided.

The device offers selectable B8ZS encoding/decoding, and unipolar or bipolar data I/O. The LXT310 also provides jitter attenuation in either the transmit or receive direction starting at 6 Hz, and incorporates a serial interface (SIO) for microprocessor control.

The LXT310 offers a variety of diagnostic features including loopbacks and loss of signal monitoring. It uses an advanced double-poly, double-metal CMOS process and requires only a single 5-volt power supply.

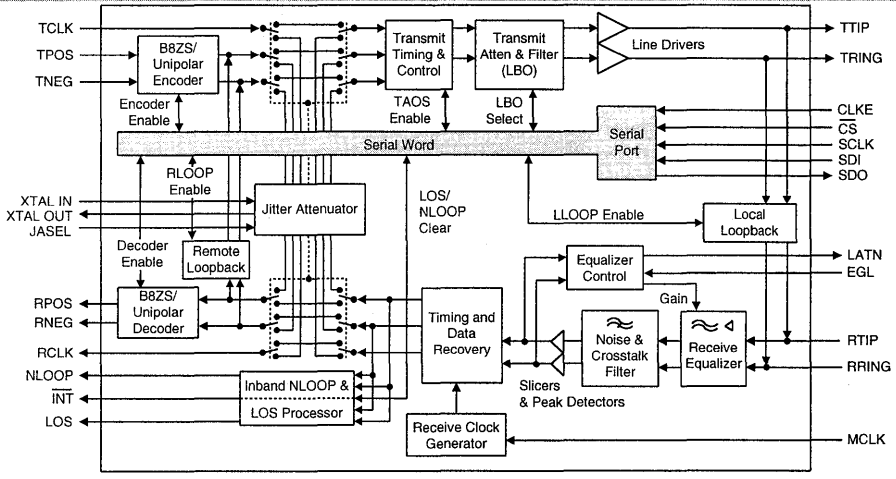
Applications

- ISDN Primary Rate Interface (PRI) (ANSI T1.408)
- CSU Interface to T1 Service (Pub 62411)
- DS1 Metallic Interface (ANSI T1.403)
- T1 LAN bridge
- CPU to CPU Channel Extenders
- Digital Loop Carrier - Subscriber Carrier Systems
- T1 Mux
- Channel Banks

Features

- Fully integrated transceiver comprising: on-chip equalizer; timing recovery/control; data processor; receiver; and transmitter with Line Build-Out and digital control
- Meets or exceeds ANSI and ITU specifications including T1.403, T1.408, and AT&T Pub 62411
- Selectable Receiver Sensitivity. Fully restores the received signal after transmission through a cable with attenuation of either 0 to 26 dB, or 0 to 36 dB @ 772 kHz
- Selectable Unipolar or Bipolar data I/O
- Selectable B8ZS encoding/decoding
- Line attenuation indication output
- 138 UI jitter tolerance at 1 Hz
- Output short circuit current limit protection
- On-line idle mode for redundant systems
- 7.5 dB, 15 dB, and 22.5 dB transmit LBOs
- Local, remote and inband network loopback functions
- Receive monitor with Loss of Signal (LOS) output
- Jitter attenuation starting at 6 Hz, switchable to transmit or receive path
- Microprocessor controllable

LXT310 Block Diagram



PIN ASSIGNMENTS AND SIGNAL DESCRIPTIONS

Figure 1: Pin Assignments

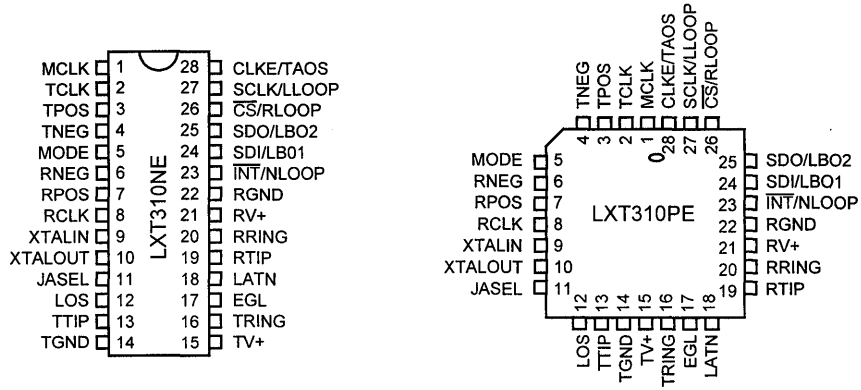


Table 1: Pin Descriptions

Pin #	Sym	I/O	Description
1	MCLK	I	**Master Clock.** A 1.544 MHz clock input used to generate internal clocks. Upon Loss of Signal (LOS), RCLK is derived from MCLK. If MCLK is not applied, this pin should be grounded.
2	TCLK	I	**Transmit Clock.** Transmit clock input. TPOS and TNEG are sampled on the falling edge of TCLK.
3	TPOS/ TDATA	I	**Transmit Data Input; Data Input/Polarity Select.** Input data to be transmitted on the twisted-pair line. Normally, pin 3 is TPOS and pin 4 is TNEG, the positive and negative sides of a bipolar input pair. However, if pin 4 is held High for at least 16 TCLK cycles (equivalent to 15 successive bipolar violations), the LXT310 switches to a unipolar mode. The LXT310 returns to bipolar I/O when pin 4 goes Low.
4	TNEG/ UBS	I	
5	MODE	I	**Mode Select.** Setting MODE High selects the Host Mode. In Host Mode, the serial interface is enabled for control and status reporting. Setting MODE Low selects the Hardware (H/W) Mode. In Hardware Mode the serial interface is disabled; hard-wired pins control configuration and report status. Tying MODE to RCLK enables Hardware Mode and the B8ZS encoder/decoder.
6	RNEG	O	**Receive Negative Data; Receive Positive Data.** In Bipolar Data I/O Mode pins 6 and 7 are bipolar data outputs. A signal on RNEG corresponds to receipt of a negative pulse on RTIP/RRING, and a signal on RPOS corresponds to a positive pulse on RTIP/ RRING. RNEG/RPOS outputs are Non-Return-to-Zero (NRZ). In Host Mode, CLKE determines the clock edge at which these outputs are stable and valid. In Hardware Mode both outputs are stable and valid on the RCLK rising edge.
7	RPOS	O	
6	BPV	O	**Bipolar Violation.** In Unipolar Data I/O Mode, pin 6 goes High to indicate receipt of a Bipolar Violation of the AMI code.

Table 1: Pin Descriptions – continued

Pin #	Sym	I/O	Description
7	RDATA	O	**Bipolar Violation.** In Unipolar Mode, data received from the twisted-pair line is output at pin 7.
8	RCLK	O	**Recovered Clock.** This is the clock recovered from the signal received at RTIP and RRING.
9	XTALIN	I	**Crystal Input; Crystal Output.** An external crystal (18.7 pF load capacitance, pullable) operating at 6.176 MHz (four times the bit rate) is required to enable the jitter attenuation function of the LXT310. These pins may also be used to disable the jitter attenuator by connecting the XTALIN pin to the positive supply through a resistor, and leaving the XTALOUT pin unconnected.
10	XTALOUT	O	
11	JASEL	O	**Jitter Attenuation Select.** Selects jitter attenuation location. When JASEL is High, the jitter attenuator is active in the receive path. When JASEL is Low, the jitter attenuator is active in the transmit path.
12	LOS	O	**Loss of Signal.** LOS goes High when 175 consecutive spaces have been detected. LOS returns Low when the received signal reaches a mark density of 12.5% (determined by receipt of four marks within 32 bit periods). Received marks are output on RPOS and RNEG even when LOS is High.
13	TTIP	O	**Transmit Tip; Transmit Ring.** Differential Driver Outputs. These outputs are designed to drive a 50 - 200 Ω load. Line matching resistors and transformer can be selected to give the desired pulse height.
16	TRING	O	
14	TGND	–	**Transmit Ground.** Ground return for the transmit drivers power supply TV+.
15	TV+	I	**Transmit Power Supply.** +5 VDC power supply input for the transmit drivers. TV+ must not vary from RV+ by more than ±0.3 V.
17	EGL	I	**Equalizer Gain Limit.** Input sets equalizer gain. When EGL is Low, up to 36 dB of equalizer gain may be added. When EGL is High, equalizer gain is limited to no more than 26 dB.
18	LATN	O	**Line Attenuation Indication (See Figure 2).** Encoded output. Pulse width, relative to RCLK, indicates receive equalizer gain setting (line insertion loss at 772 kHz) in 7.5 dB steps. When LATN = 1 RCLK pulse, the equalizer is set at 7.5 dB gain, 2 pulses = 15 dB, 3 pulses = 22.5 dB and 4 pulses = 0 dB. Output is valid on the rising edge of RCLK.
19	RTIP	I	**Receive Tip; Receive Ring.** The AMI signal received from the line is applied at these pins. A 1:1 transformer is required. Data and clock from the signal applied at these pins are recovered and output on the RPOS/RNEG and RCLK pins.
20	RRING	I	
21	RV+	I	**Receive Power Supply.** +5 VDC power supply for all circuits except the transmit drivers. (Transmit drivers are supplied by TV+.)
22	RGND	–	**Receive Ground.** Ground return for power supply RV+.

Table 1: Pin Descriptions – continued

Pin #	Sym	I/O	Description
23	NLOOP	O	**Network Loopback** ***(H/W Mode).*** When High, indicates Inband Network Loopback has been activated by reception of 00001 pattern for five seconds. NLOOP is reset by reception of 001 for five seconds, or by activation of RLOOP or LLOOP.
	$\overline{INT}$	I	**Interrupt** ***(Host Mode).*** This LXT310 Host Mode output goes Low to flag the host processor when LOS or NLOOP changes state. $\overline{INT}$ is an open-drain output and should be tied to power supply RV+ through a resistor. $\overline{INT}$ is reset by clearing the LOS or NLOOP register bit.
24	SDI	I	**Serial Data In** ***(Host Mode).*** The serial data input stream is applied to this pin when the LXT310 operates in the Host Mode. SDI is sampled on the rising edge of SCLK.
	LBO1	I	**Line Build-Out Select 1** ***(H/W Mode).*** In Hardware Mode this input is used in conjunction with LBO2 to select the transmit line build-outs: 00 = 0 dB, 01 = 7.5 dB, 10 = 15 dB, and 11 = 22.5 dB.
25	SDO	O	**Serial Data Out** ***(Host Mode).*** The serial data from the on-chip register is output on this pin in the LXT310 Host Mode. If CLKE is High, SDO is valid on the rising edge of SCLK. If CLKE is Low, SDO is valid on the falling edge of SCLK. This pin goes to a high-impedance state when the serial port is being written to and when $\overline{CS}$ is High.
	LBO2	I	**Line Build-Out Select 2** ***(H/W Mode).*** The signal applied at this pin in the LXT310 Hardware Mode is used in conjunction with LBO1 to select the transmit line build-outs. 00 = 0 dB, 01 = 7.5 dB, 10 = 15 dB, and 11 = 22.5 dB.
26	$\overline{CS}$	I	**Chip Select** ***(Host Mode).*** This input is used to access the serial interface in the Host Mode. For each read or write operation, $\overline{CS}$ must transition from High to Low, and remain Low.
	RLOOP	I	**Remote Loopback** ***(H/W Mode).*** This input controls loopback in the Hardware Mode. Setting RLOOP High enables Remote Loopback. During Remote Loopback, in-line encoders and decoders are bypassed. Setting both RLOOP and LLOOP High while holding TAOS Low causes a Reset. Setting both RLOOP and LLOOP with TAOS High (or tying RCLK to RLOOP) enables Network Loopback detection.
27	SCLK	I	**Serial Clock** ***(Host Mode).*** This clock is used in the Host Mode to write data to or read data from the serial interface registers.
	LLOOP	I	**Local Loopback** ***(H/W Mode).*** This input controls loopback functions in the Hardware Mode. Setting LLOOP High enables the Local Loopback Mode. Setting both LLOOP and RLOOP while holding TAOS Low causes a Reset.
28	CLKE	I	**Clock Edge** ***(Host Mode).*** Setting CLKE High causes RPOS and RNEG to be valid on the falling edge of RCLK, and SDO to be valid on the rising edge of SCLK. When CLKE is Low, RPOS and RNEG are valid on the rising edge of RCLK, and SDO is valid on the falling edge of SCLK.
	TAOS	I	**Transmit All Ones** ***(H/W Mode).*** When set High in the Hardware Mode, TAOS causes the LXT310 to transmit a stream of marks at the TCLK frequency. Activating TAOS causes TPOS and TNEG inputs to be ignored. TAOS is inhibited during Remote Loopback. Setting TAOS, LLOOP and RLOOP High simultaneously enables Network Loopback detection.

FUNCTIONAL DESCRIPTION

The LXT310 is a fully integrated PCM transceiver for 1.544 Mbps (T1) applications. It allows full-duplex transmission of digital data over existing twisted-pair installations.

The LXT310 interfaces with two twisted-pair lines (one pair for transmit, one pair for receive) through standard pulse transformers and appropriate resistors.

The figure on the front page of this section is a block diagram of the LXT310. The transceiver may be controlled by a microprocessor through the serial port (Host Mode), or by individual pin settings (Hardware Mode). The jitter attenuator may be positioned in either the transmit or receive path.

Power Requirements

The LXT310 is a low-power CMOS device. It operates from a single +5 V power supply which can be connected externally to both the transmitter and receiver. However, the two inputs must be within ± .3 V of each other, and decoupled to their respective grounds separately. Refer to Application Information for typical decoupling circuitry. Isolation between the transmit and receive circuits is provided internally.

Initialization and Reset Operations

Upon power up, the transceiver is held static until the power supply reaches approximately 3 V. Upon crossing this threshold, the device begins a 32 ms reset cycle to calibrate the transmit and receive delay lines and lock the Phase Lock Loop to the receive line. A reference clock is required to calibrate the delay lines. The transmitter reference is provided by TCLK. The crystal oscillator provides the receiver reference. If the crystal oscillator is grounded, MCLK is used as the receiver reference clock.

The transceiver can also be reset from the Host or Hardware Mode. In Host Mode, reset is commanded by simultaneously writing ones to RLOOP and LLOOP, and a zero to TAOS. In Hardware Mode, reset is commanded by holding RLOOP and LLOOP High simultaneously for 200 ns while holding TAOS Low. In either mode, reset clears and sets all registers to 0.

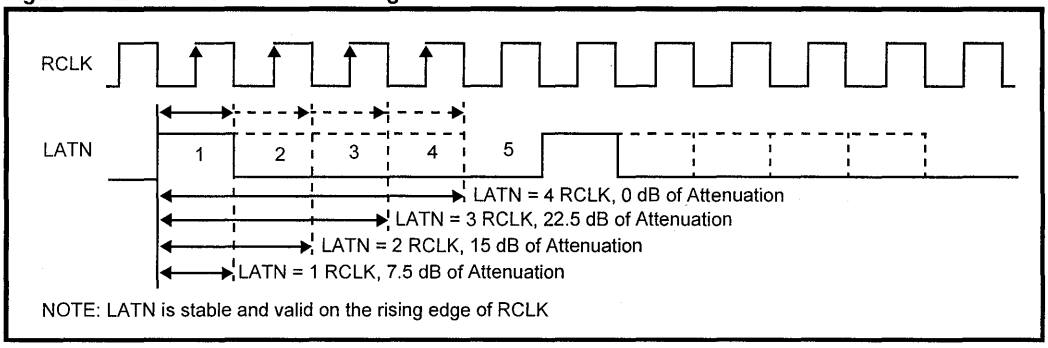
Receiver

The twisted-pair input is received via a 1:1 transformer. Recovered data is output at RPOS/RNEG (RDATA in unipolar mode), and the recovered clock is output at RCLK. Refer to Test Specifications for receiver timing.

The signal received at RPOS and RNEG is processed through the receive equalizer. The Equalizer Gain Limit (EGL) input determines the maximum gain that may be applied at the equalizer. When set Low, up to 36 dB of gain may be applied.

When EGL is High, gain is limited to no more than 26 dB providing for increased noise margin in shorter loop operation. Insertion loss of the line in 7.5 dB steps, as indicated by the receive equalizer setting, is encoded in the LATN output as shown in Figure 2.

Figure 2: LATN Pulse Width Encoding



The equalized signal is filtered and applied to the peak detector and data slicers. The peak detector samples the inputs and determines the maximum value of the received signal. A percentage of the peak value is provided to the data slicers as a threshold level to ensure optimum signal-to-noise ratio. The threshold is set to 50% of the peak value. The receiver is capable of accurately recovering signals with up to 36 dB of cable attenuation (from 2.4 V)

After processing through the data slicers, the received signal is routed to the data and timing recovery section, then to the B8ZS decoder (if selected) and to the LOS processor. The LOS Processor loads a digital counter at the RCLK frequency. The count is incremented each time a zero (space) is received, and reset to zero each time a one (mark) is received. Upon receipt of 175 consecutive zeros the LOS pin goes High, and a smooth transition replaces the RCLK output with the MCLK. (During LOS if MCLK is not supplied and JASEL = 1, the RCLK output is replaced with the centered crystal clock.)

Received marks will be output regardless of the LOS status, but the LOS pin will not reset until the ones density reaches 12.5 %. This level is based on receipt of at least 4 ones in any 32-bit period.

Transmitter

Input data (bipolar or unipolar) for transmission onto the line is clocked serially into the device. Bipolar data is input at pin 3 (TPOS) and pin 4 (TNEG). Unipolar data is input at pin 3 (TDATA) only. (Unipolar mode is enabled by holding pin 4 high for 16 RCLK cycles). Input data may be passed through the Jitter Attenuator and/or B8ZS encoder, if selected. In Host Mode, B8ZS is selected by setting bit D3 of the input data byte. In Hardware Mode, B8ZS is selected by connecting the MODE pin to RCLK. Input synchronization is supplied by the transmit clock (TCLK). Timing requirements for TCLK and the Master Clock (MCLK) are defined in Test Specifications.

Idle Mode

The LXT310 incorporates a transmit idle mode. This allows multiple transceivers to be connected to a single line for redundant applications. TTIP and TRING remain in a high- impedance state when TCLK is not present (TCLK grounded). The high-impedance state can be temporarily disabled by enabling either TAOS, Remote Loopback or Network Loopback.

The transmitted pulse shape is determined by Line Build Out (LBO) inputs LBO1 and LBO2 as follows:

Line Build-Out (dB)	0	7.5	15	22.5
LBO1	0	1	0	1
LBO2	0	0	1	1

LBO settings are input through the serial port in the Host Mode. In the Hardware Mode, LBO inputs are applied through individual pins. Shaped pulses meeting the various T1 CSU and ISDN PRI requirements are applied to the AMI line driver for transmission onto the line at TTIP and TRING. Refer to Test Specifications for T1 pulse mask specifications.

Short Circuit Limit

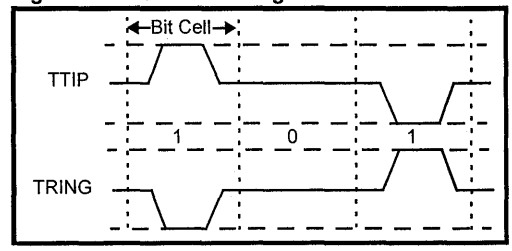
The LXT310 transmitter is equipped with a short-circuit limiter. This feature limits to approximately 120 mA RMS the current the transmitter will source into a low-impedance load. The limiter trips when the RMS current exceeds the limit for 100 µs (~ 150 marks). It automatically resets when the load current drops below the limit.

The LXT310 meets or exceeds FCC and AT&T specifications for CSU and NI applications, as well as ANSI T1E1, and CCITT requirements for ISDN PRI.

Line Code

The LXT310 transmits data as a 50% AMI line code as shown in Figure 3. Power consumption is reduced by activating the AMI line driver only to transmit a mark. The output driver is disabled during transmission of a space. Biasing of the transmit DC level is on-chip.

Figure 3: 50% AMI Coding



Jitter Attenuation

Jitter attenuation is provided by a Jitter Attenuation Loop (JAL) and an Elastic Store (ES). An external crystal oscillating at 4 times the bit rate provides clock stabilization. Refer to Table 6 for crystal specifications. The ES is a 32 x 2-bit register. When JASEL = 1, the JAL is positioned in the receive path. When JASEL = 0, the JAL is positioned in the transmit path.

Data (TPOS/TNEG / TDATA or RPOS/RNEG / RDATA) is clocked into the ES with the associated clock signal (TCLK or RCLK), and clocked out of the ES with the dejittered clock from the JAL. When the bit count in the ES is within two bits of overflowing or underflowing, the ES adjusts the output clock by 1/8 of a bit period. The ES produces an average delay of 16 bits in the associated path.

Operating Modes

The LXT310 can be controlled by a microprocessor through a serial interface (Host Mode), or through individual pins (Hardware Mode). The mode of operation is set by the MODE pin logic level.

Host Mode Operation

The LXT310 operates in the Host Mode when MODE is set High. The 16-bit serial word consists of an 8-bit Command/Address byte and an 8-bit Data byte. Table 3 lists the output data bit combinations. Figure 4 shows the serial interface data structure and timing. The Host Mode provides a latched Interrupt output (INT) which is triggered by a change in the LOS or NLOOP bits. The Interrupt is cleared when the interrupt condition no longer exists, and the host processor writes a one to the respective bit in the serial input data byte.

Host Mode also allows control of the serial data and receive data output timing. The Clock Edge (CLKE) signal determines when these outputs are valid, relative to the Serial Clock (SCLK) or RCLK as listed in Table 2.

Table 2: CLKE Settings

Output	Clock	CLKE = 0	CLKE = 1
RPOS/RNEG SDO	RCLK SCLK	Rising Falling	Falling Rising

The LXT310 serial port is addressed by setting bit A4 in the Address/Command byte, corresponding to address 16. The LXT310 contains only a single output data register so no complex chip addressing scheme is required. The register is accessed by causing the Chip Select (CS) input to transition from High to Low. Bit 1 of the serial Address/Command byte provides Read/Write control when the chip is accessed. A logic 1 indicates a read operation, and a logic 0 indicates a write operation. Serial data I/O timing characteristics are shown in Table 14, and Figures 11 and 12 in the Test Specifications section.

Figure 4: LXT310 Serial Interface Data Structure

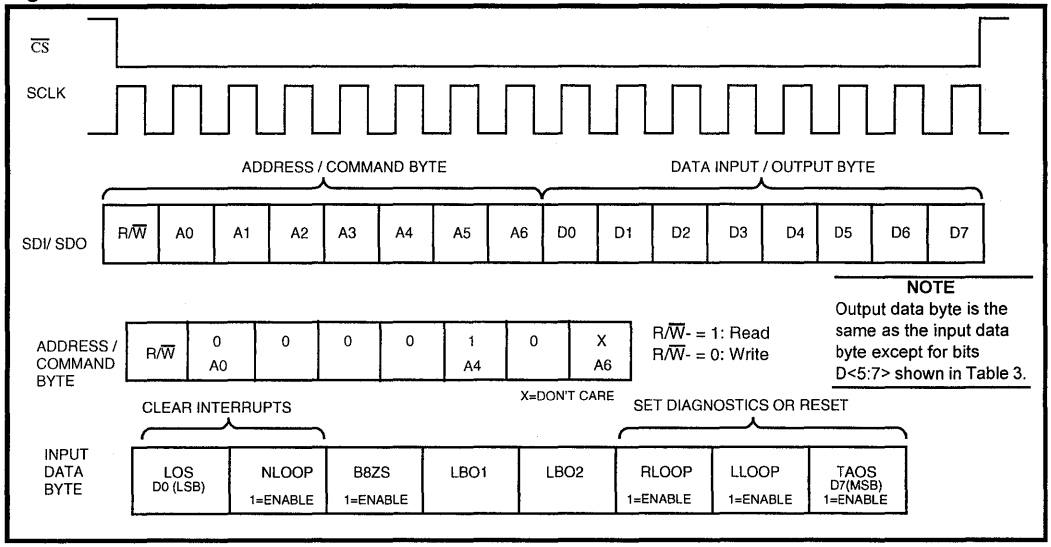


Table 3: LXT310 Serial Data Output Bits
(See Figure 4)

Bit D5	Bit D6	Bit D7	Status
0	0	0	Reset has occurred, or no program input.
0	0	1	TAOS is active.
0	1	0	Local Loopback is active.
0	1	1	TAOS and Local Loopback are active.
1	0	0	Remote Loopback is active.
1	0	1	DPM has changed state since last Clear DPM occurred.
1	1	0	LOS has changed state since last Clear LOS occurred.
1	1	1	LOS and DPM have both changed state since last Clear DPM and Clear LOS occurred.

Hardware Mode Operation

In Hardware Mode the transceiver is accessed and controlled through individual pins. With the exception of the INT and CLKE functions, Hardware Mode provides all the functions provided in the Host Mode. In the Hardware Mode RPOS/RNEG or RDATA outputs are valid on the rising edge of RCLK. The LXT310 operates in Hardware Mode only when MODE is set Low or connected to RCLK.

Diagnostic Mode Operation

Transmit All Ones

In Transmit All Ones (TAOS) Mode, the TPOS and TNEG inputs to the transceiver are ignored and the transceiver transmits a continuous stream of ones at the TCLK frequency. (If TCLK is not provided, TAOS is locked to the MCLK.) This can be used as the Blue Alarm Indicator (AIS). In Host Mode, TAOS is commanded by writing a one to bit D7 of the input data byte. In Hardware Mode, TAOS is commanded by setting pin 28 High. TAOS can be commanded simultaneously with Local Loopback, but is inhibited during Remote Loopback.

Local Loopback

Local Loopback (LLOOP) is designed to exercise the maximum number of functional blocks. During LLOOP operation, the RTIP/RRING inputs from the line are disconnected. Instead, the transmit outputs are routed back into the receive inputs. This tests the encoders/decoders, jitter attenuator, transmitter, receiver and timing recovery sections. In Host Mode, Local Loopback is commanded by writing a one to bit D6 of the input data byte. In Hardware Mode, Local Loopback is commanded by setting pin 27 High. If TAOS and LLOOP are both set, the All Ones pattern is transmitted onto the line while the TPOS/TNEG input data is looped back to the RPOS/RNEG outputs.

Remote Loopback

In Remote Loopback (RLOOP) Mode, the transmit data and clock inputs (TCLK and TPOS/TNEG or TDATA) are ignored, and the in-line encoders and decoders are bypassed. The RPOS/RNEG or RDATA outputs are looped back through the transmit circuits and output on TTIP and TRING at the RCLK frequency. Receiver circuits are unaffected by the RLOOP command and continue to output the RCLK and RPOS/RNEG or RDATA signals received from the twisted-pair line. In Host Mode, Remote Loopback is commanded by writing a one to bit D5 of the input data byte. In Hardware Mode, Remote Loopback is commanded by setting pin 26 High.

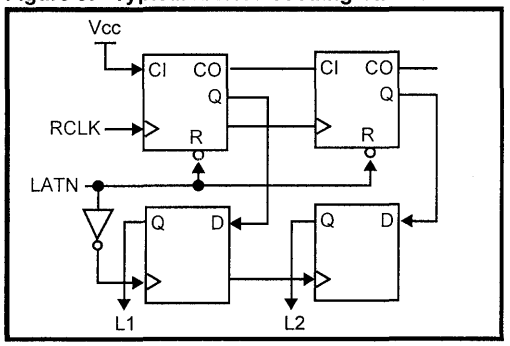
Network Loopback

Network Loopback can be commanded from the network when the Network Loopback detect function is enabled. In Host Mode, Network Loopback (NLOOP) detection is enabled by simultaneously writing ones to RLOOP, LLOOP and TAOS, then writing zeros in the next cycle. In Hardware Mode, Network Loopback detection is enabled by holding RLOOP, LLOOP and TAOS High simultaneously for 200 ns then bringing them Low, or by tying RCLK to RLOOP. NLOOP detection may be disabled by resetting the chip.

When NLOOP detection is enabled, the receiver monitors the input data stream for the NLOOP data patterns (00001 = enable, 001 = disable). When an NLOOP enable data pattern is repeated for a minimum of five seconds (with 10-3 BER), the device begins remote loopback operation. The LXT310 responds to both framed and unframed NLOOP patterns. Once remote network loopback detection is enabled at the chip and activated by the correct data pattern, it is identical to remote loopback initiated at the chip. NLOOP is reset by receiving the disable pattern for 5 seconds, or by activation of RLOOP. NLOOP is temporarily interrupted by LLOOP, but the NLOOP state is not reset.

APPLICATION INFORMATION

Figure 5: Typical LATN Decoding Circuit



LATN Decoding Circuits and External Components

To conserve pins, the line attenuation output is encoded as a simple serial bit stream. Table 4 provides the decoded output for each equalizer setting. Figure 5 is a typical decoding circuit for the LATN output. It uses a 2-bit synchronous counter (half of a 4-bit counter) with synchronous reset, and a pair of flip-flops. Table 5 lists approved crystals and transformers.

Table 4: LATN Output Coding

L1	L2	Line Attenuation
0	0	0.0 dB
0	1	-7.5 dB
1	0	-15.0 dB
1	1	-22.5 dB

Table 5: Approved Crystals and Transformers

Component	Manufacturer	Part Numbers
Crystal (6.176 MHz)	M-Tron Monitor Products CTS Knights Valpey Fisher U.S. Crystal	MP-1 3808-010 / 4144-002 MSC1311-01B 6176-180 VF49A16FN1 U18-18-6176SP
Tx Transformer (1 : 2)	Bell Fuse FEE Fil-Mag Midcom Pulse Engineering Schott Corp HALO	0553-5006-IC 66Z1308 671-5832 65351, 65771 67127370 and 67130850 TD61-1205G and TD67-1205G (combo Tx/Rx)
Rx Tranformer (1 : 1)	FEE Fil-Mag Midcom Pulse Engineering Schott Corp HALO	FE 8006-155 671-5792 64936 and 65778 67130840 and 67109510 TD61-1205G and TD67-1205G (combo Tx/Rx)

Host Mode Applications

Figure 6 shows a typical T1 CSU application with the LXT310 operating in the Host Mode (MODE pin tied high). A T1/ESF Framer provides the digital interface with the host controller. Both devices are controlled through the serial interface. In the Host Mode, the LOS alarm is reported via the serial port so the LOS pin is allowed to float.

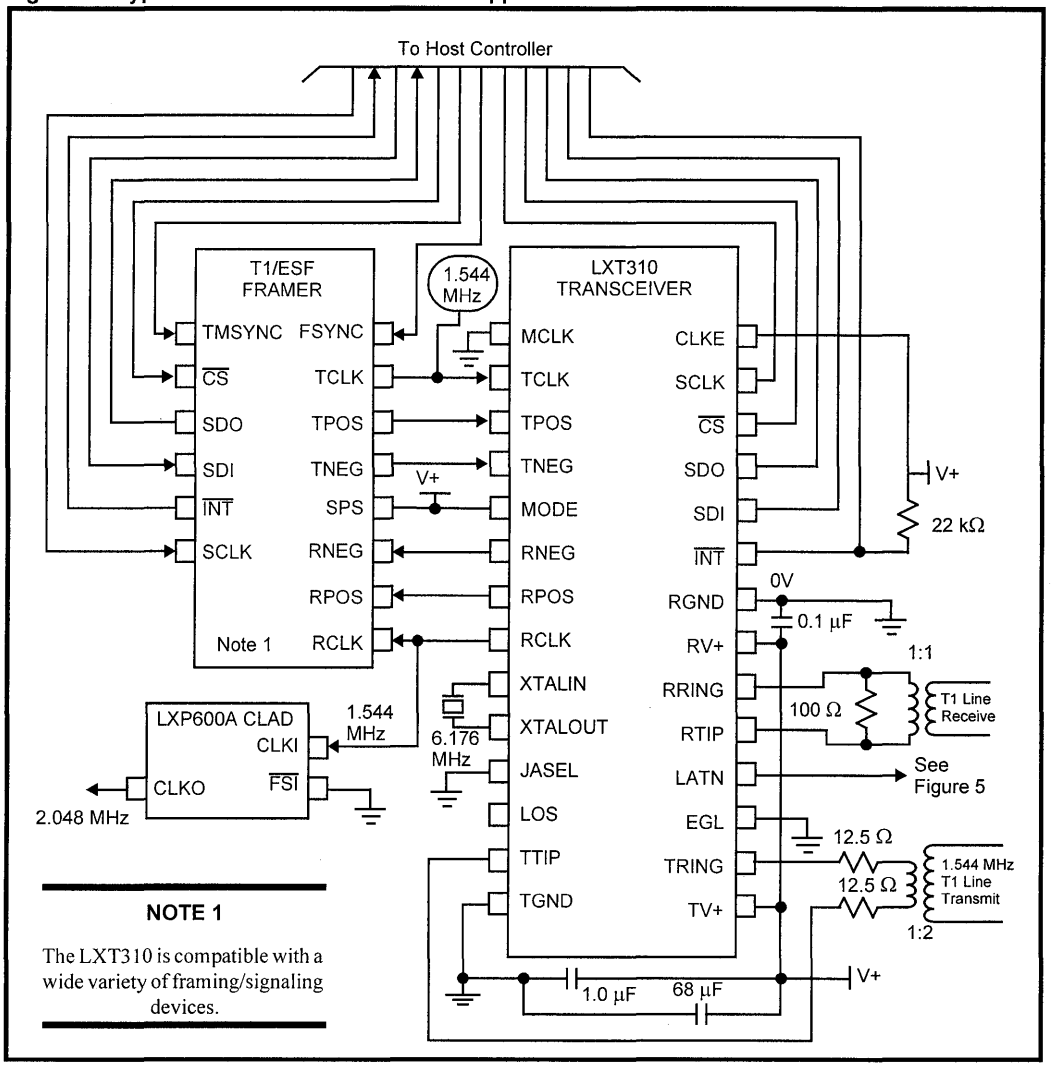
An LXP600A Clock Adapter (CLAD) provides the 2.048 MHz system backplane clock, locked to the recovered 1.544 MHz clock signal. The 6.176 MHz crystal across XTALIN and XTALOUT enables the JAL which is switched to the transmit side by the ground on JASEL. (Refer to Table 5 for approved crystals and transformers.) The power supply inputs are tied to a common bus with appropriate decoupling capacitors (68 µF and 0.1 µF) installed on each side.

The twisted-pair interfaces are relatively simple. A 100 Ω resistor across the input of a 1:1 transformer is used on the receive side, and a pair of 12.5 Ω resistors are installed in line with the 1:2 output transformer.

Table 6: LXT310 Crystal Specifications (External)

Parameter	Specification
Frequency	6.176 MHz
Frequency stability	± 20 ppm @ 25 °C ± 25 ppm from -40 °C to 85 °C (Ref 25 °C reading)
Pullability	CL = 11 pF to 18.7 pF, +ΔF = 175 to 195 ppm CL = 18.7 pF to 34 pF, -ΔF = 175 to 195 ppm
Effective series resistance	40 Ω Maximum
Crystal cut	AT
Resonance	Parallel
Maximum drive level	2.0 mW
Mode of operation	Fundamental
Crystal holder	HC49 (R3W), C_O = 7 pF maximum C_M = 17 fF typical

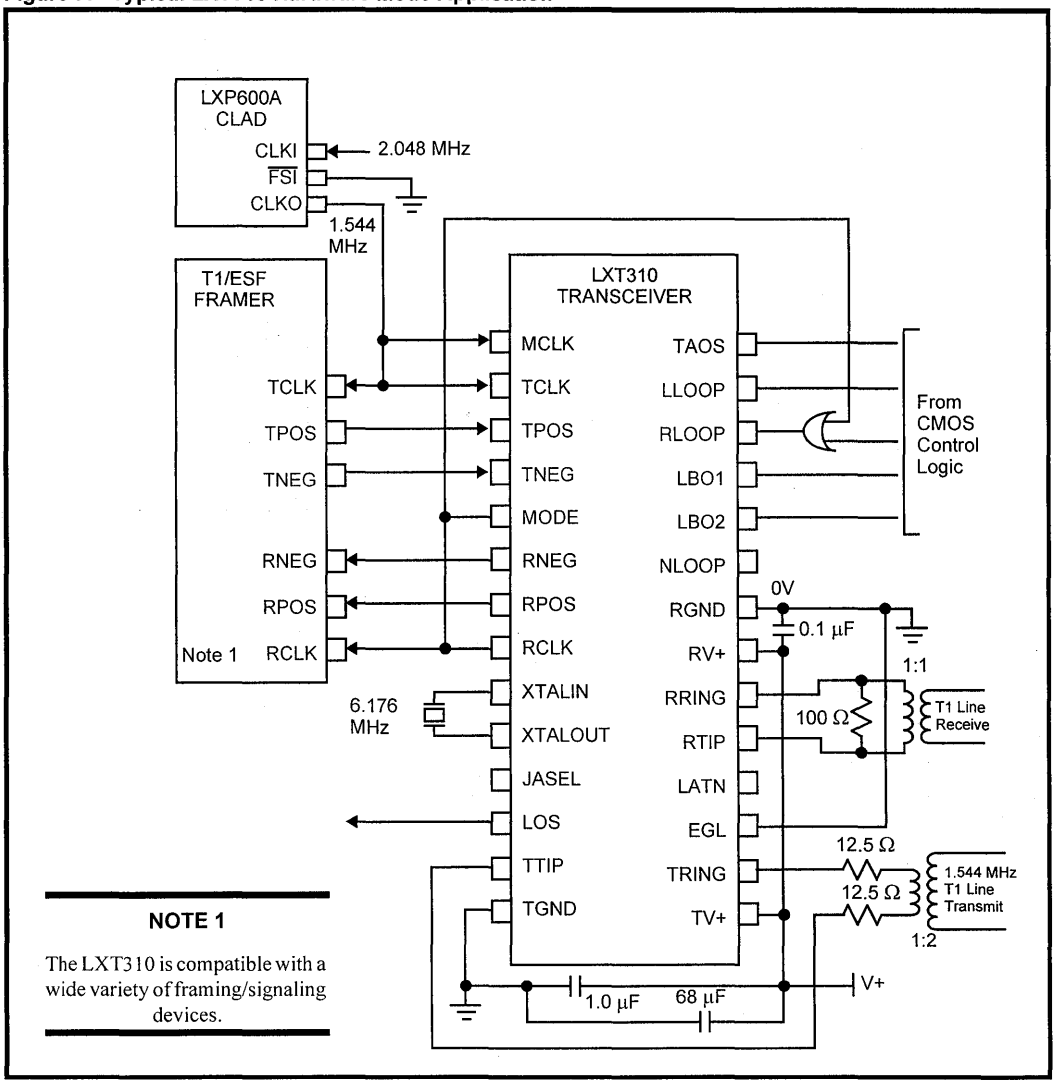
Figure 6: Typical LXT310 Host Mode T1/CSU Application



LXT310 Hardware Mode Applications

Figure 7 is a typical 1.544 Mbps ISDN PRI application with the LXT310, a T1/ESF framer and an LXP600A clock adapter. The LXT310 is operating in the Hardware Mode with B8ZS encoding enabled (MODE pin 5 tied to RCLK). As in the T1/CSU application, Figure 6, this configuration is illustrated with a single power supply bus. CMOS control logic is used to set both LBO pins high, selecting the 22.5 dB LBO, and the EGL pin is tied low, allowing for full receiver gain. The TAOS, LLOOP and RLOOP diagnostic modes are individually controllable. The RCLK input to the OR gate at RLOOP allows for clocking of the RLOOP pin, which enables network loopback detection. The receive and transmit line interfaces are identical to the Host Mode application shown in Figure 6.

Figure 7: Typical LXT310 Hardware Mode Application



NOTE 1

The LXT310 is compatible with a wide variety of framing/signaling devices.

TEST SPECIFICATIONS

NOTE

The minimum and maximum values in Tables 7 through 14 and Figures 8 through 12 represent the performance specifications of the LXT310 and are guaranteed by test, except where noted by design.

Table 7: Absolute Maximum Ratings

Parameter	Sym	Min	Max	Units
DC supply (referenced to GND)	RV+, TV+	-0.3	6.0	V
Input voltage, any pin	V_{IN}	RGND - 0.3	RV+ + 0.3	V
Input current, any pin[1]	I_{IN}	-10	10	mA
Ambient operating temperature	T_A	-40	85	°C
Storage temperature	T_{STG}	-65	150	°C

CAUTION

Operations at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

1. Transient currents of up to 100 mA will not cause SCR latch up. TTIP, TRING, TV+ and TGND can withstand a continuous current of 100 mA.

Table 8: Recommended Operating Conditions and Characteristics

Parameter	Sym	Min	Typ	Max	Units
DC supply[1]	RV+, TV+	4.75	5.0	5.25	V
Ambient operating temperature	T_A	–	25	–	° C

1. TV+ must not exceed RV+ by more than 0.3 V.

Table 9: Electrical Characteristics (Under Recommended Operating Conditions)

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
High level input voltage[2,3] (pins 1-5, 10, 23-28)	V_{IH}	2.0	–	–	V	
Low level input voltage[2,3] (pins 1-5, 10, 23-28)	V_{IL}	–	–	0.8	V	
High level output voltage[2,3] (pins 6-8, 11, 12, 23, 25)	V_{OH}	2.4	–	–	V	I_{OUT} = -400 µA
Low level output voltage[2,3] (pins 6-8, 11, 12, 23, 25)	V_{OL}	–	–	0.4	V	I_{OUT} = 1.6 mA
Input leakage current	I_{LL}	0	–	±10	µA	

1. Typical values are measured at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Functionality of pins 23 and 25 depends on mode. See Host/Hardware Mode descriptions.
3. Output drivers will output CMOS logic levels into CMOS loads.
4. TTIP, TRING only in Idle or Power Down Mode.
5. Power dissipation while driving a 25 Ω load over operating temperature range. Includes device and load. Digital input levels are within 10% of the supply rails and digital outputs are driving a 50 pF capacitive load.

Table 9: Electrical Characteristics (Under Recommended Operating Conditions)

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Three-state leakage current[2] (pin 25)	I_{3L}	0	–	±10	µA	
Driver power down current[4]	I_{PD}	–	–	±1.2	mA	Direct connection to Vcc or GND
Total power dissipation[5]	P_D	–	620	–	mW	100% ones density & maximum line length @ 5.25 V

1. Typical values are measured at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Functionality of pins 23 and 25 depends on mode. See Host/Hardware Mode descriptions.
3. Output drivers will output CMOS logic levels into CMOS loads.
4. TTIP, TRING only in Idle or Power Down Mode.
5. Power dissipation while driving a 25 Ω load over operating temperature range. Includes device and load. Digital input levels are within 10% of the supply rails and digital outputs are driving a 50 pF capacitive load.

Table 10: Analog Characteristics (Over Recommended Range)

Parameter		Min	Typ[1]	Max	Units	Test Conditions
Recommended output load at TTIP and TRING		50	–	200	Ω	
AMI Output Pulse Amplitudes		2.4	3.0	3.6	V	
Jitter added by the transmitter[2]	10 Hz - 8 kHz	–	–	0.01	UI	Measured at the output with LBO1 = 0, and LBO2 = 0
	8 kHz - 40 kHz	–	–	0.02	UI	
	10 Hz - 40 kHz	–	–	0.02	UI	
	Broad Band	–	–	0.04	UI	
Receive signal attenuation range @ 772 kHz	Mode 1 (EGL = 1)	0	26	–	dB	
	Mode 2 (EGL = 0)	0	36	–	dB	
Allowable consecutive zeros before LOS		160	175	190	–	
Input jitter tolerance	10 kHz - 100 kHz	0.4	–	–	UI	
	1 Hz	13.8	–	–		
Jitter attenuation curve corner frequency[3]		–	3	–	Hz	

1. Typical values are measured at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Input signal to TCLK is jitter-free.
3. Guaranteed by characterization; not subject to production testing.
4. Circuit attenuates jitter at 20 dB/decade above the corner frequency.

Figure 8: 1.544 Mbps DS1 Pulse Mask (T1.403 - 1995)

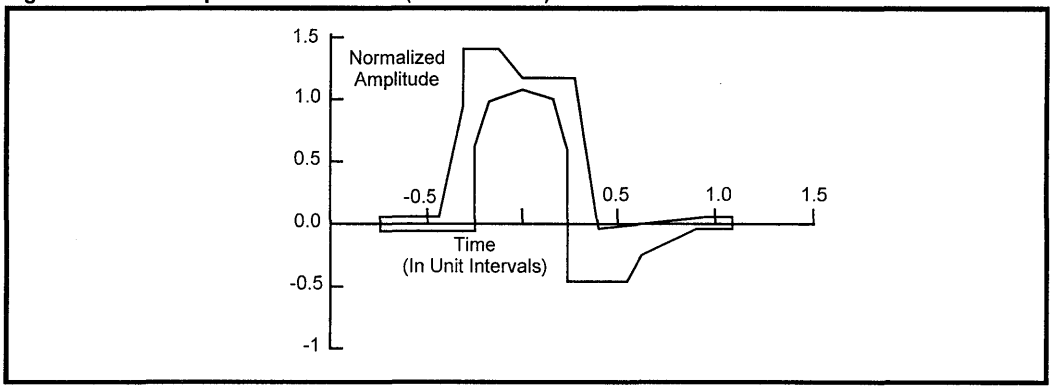


Table 11: Pulse Mask Corner Point Specifications

Maximum Curve		Minimum Curve	
Time (ns)	**% V**	**Time (ns)**	**% V**
0	5	0	-5
250	5	350	-5
325	80	350	50
325	120	400	90
425	120	500	95
500	105	600	90
675	105	650	50
725	5	650	-45
1100	5	800	-45
1250	5	896	-26
		1100	-5
		1250	-5

Table 12: LXT310 Receive Timing Characteristics (See Figure 9)

Parameter	Sym	Min	Typ[1]	Max	Units
Receive clock duty cycle[2]	RCLKd	40	50	60	%
Receive clock pulse width	t_{PW}	600	648	700	ns
Receive clock pulse width high	t_{PWH}	–	324	–	ns
Receive clock pulse width low	t_{PWL}	303	324	345	ns
RPOS/RNEG to RCLK rising setup time	t_{SUR}	–	274	–	ns
RCLK rising to RPOS/RNEG hold time	t_{HR}	–	274	–	ns

1. Typical values are at 25 °C and are for design aid only; they are not guaranteed and not subject to production testing.
2. .RCLK duty cycle widths will vary depending on extent of received pulse jitter displacement. Max and Min RCLK duty cycles are for worst case jitter conditions (0.4 UI clock displacement for 1.544 MHz).

Figure 9: LXT310 Receive Clock Timing Diagram

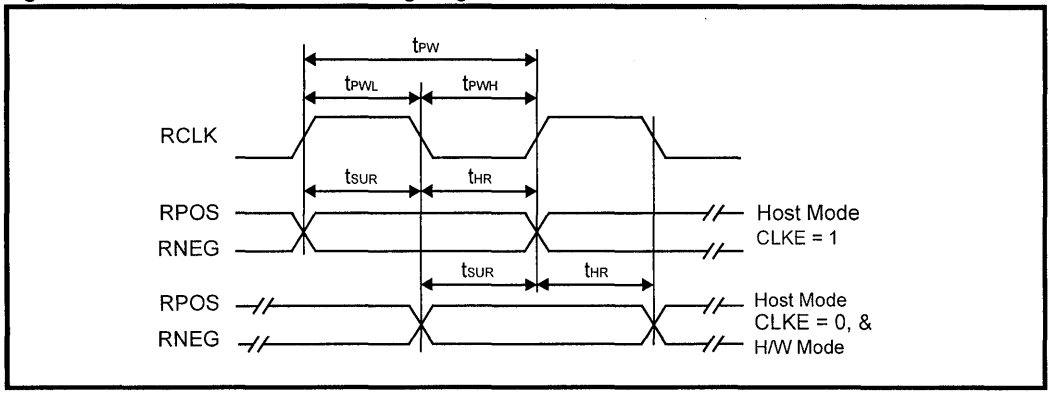


Table 13: LXT310 Master Clock and Transmit Timing Characteristics
(See Figure 10)

Parameter	Sym	Min	Typ[1]	Max	Units	Notes
Master clock frequency	MCLK	–	1.544	–	MHz	
Master clock tolerance	MCLKt	–	±100	–	ppm	
Master clock duty cycle	MCLKd	40	–	60	%	
Crystal frequency	fc	–	6.176	–	MHz	LXT310 only
Transmit clock frequency	TCLK	–	1.544	–	MHz	
Transmit clock tolerance	TCLKt	–	–	±100	ppm	
Transmit clock duty cycle	TCLKd	10	–	90	%	
TPOS/TNEG to TCLK setup time	tSUT	50	–	–	ns	
TCLK to TPOS/TNEG hold time	tHT	50	–	–	ns	

1. Typical values are at 25 °C and are for design aid only; they are not guaranteed and not subject to production testing.

Figure 10: LXT310 Transmit Clock Timing Diagram

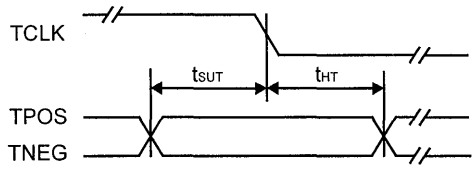


Table 14: LXT310 Serial i/O Timing Characteristics (See Figures 11 and 12)

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Rise/Fall time - any digital output	t_{RF}	–	–	100	ns	Load 1.6 mA, 50 pF
SDI to SCLK setup time	t_{DC}	50	–	–	ns	
SCLK to SDI hold time	t_{CDH}	50	–	–	ns	
SCLK low time	t_{CL}	240	–	–	ns	
SCLK high time	t_{CH}	240	–	–	ns	
SCLK rise and fall time	t_R, t_F	–	–	50	ns	
$\overline{CS}$ to SCLK setup time	t_{CC}	50	–	–	ns	
SCLK to $\overline{CS}$ hold time	t_{CCH}	50	–	–	ns	
$\overline{CS}$ inactive time	t_{CWH}	250	–	–	ns	
SCLK to SDO valid	t_{CDV}	–	–	200	ns	
SCLK falling edge or $\overline{CS}$ rising edge to SDO high Z	t_{CDZ}	–	100	–	ns	

1. Typical values are at 25° C and are for design aid only; they are not guaranteed and not subject to production testing.

Figure 11: LXT310 Serial Data Input Timing Diagram

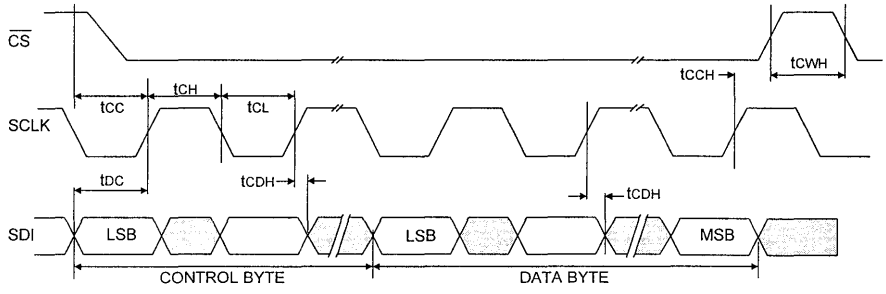
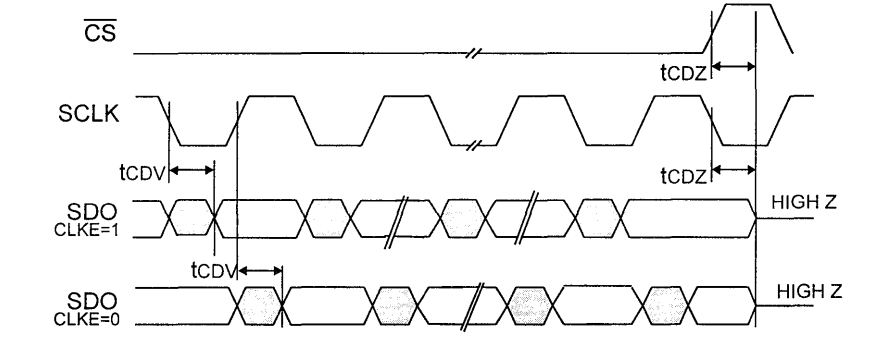


Figure 12: LXT310 Serial Data Output Timing Diagram



NOTES

LXT317

DECT Twisted-Pair LIU Transceiver

General Description

The LXT317 is the first fully integrated, long-haul transceiver for Digital European Cordless Telephony (DECT) base station interface applications at 1.152 Mbps. The transceiver operates over twisted-pair cable to a maximum of 43 dB (3.5 km at 0.6 mm, 40 nF/km cable) with no external components.

The LXT317 offers selectable HDB3 encoding/decoding, and unipolar or bipolar data I/O. The LXT317 also offers a variety of diagnostic features including loopbacks and Loss of Signal monitoring.

Its advanced double-poly, double-metal CMOS process requires only a single 5-volt power supply.

Applications

- DECT base stations to switch/PBX interface
- NTU (interface to E1 Service)
- LAN bridge
- Private network data pump

Features

- Fully integrated transceiver comprising:
  - on-chip equalizer
  - timing recovery/control
  - data processor
  - receiver
  - transmitter
  - digital control
- Fully restores the received signal after transmission via a cable with attenuation of 43 dB @ 576 kHz
- Selectable Unipolar or Bipolar data I/O
- Selectable HDB3 encoding/decoding
- Output short circuit current limit protection
- On-line idle mode for testing or for redundant systems
- Local and remote loopback functions
- Receive monitor with Loss of Signal (LOS) output
- High input jitter tolerance
- Constant through-chip delay
- Available in 28-pin DIP and PLCC
- -40 °C to +85 °C operating temperature

LXT317 Block Diagram

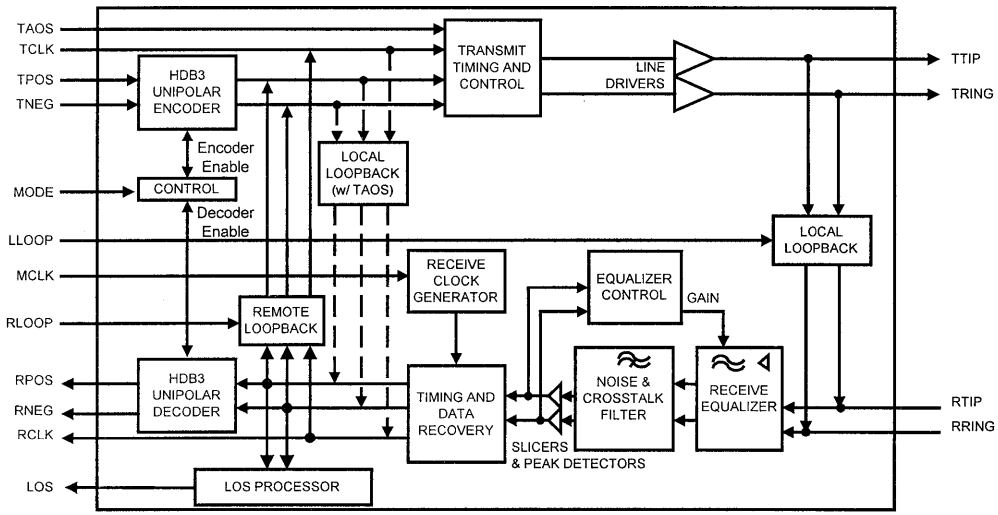
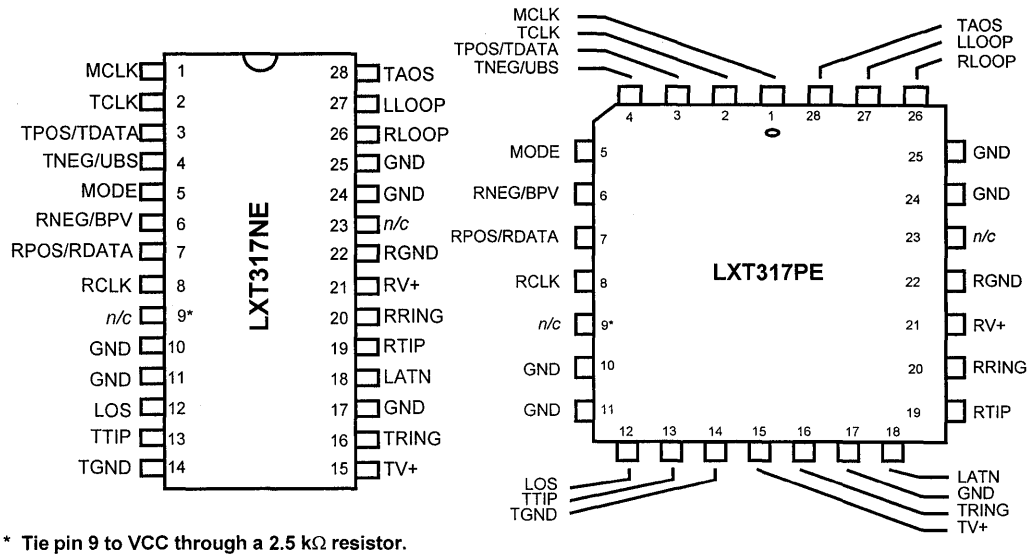


Figure 1: LXT317 Pin Assignments



* Tie pin 9 to VCC through a 2.5 kΩ resistor.

Table 1: Pin Descriptions

Pin #	Symbol	I/O	Description
1	MCLK	I	**Master Clock.** A 1.152 MHz clock input used to generate internal clocks. Upon Loss of Signal (LOS), RCLK is derived from MCLK. If MCLK is not applied tie this pin Low.
2	TCLK	I	**Transmit Clock.** Transmit clock input. TPOS and TNEG are sampled on the falling edge of TCLK. If TCLK is not supplied tie this pin Low.
3	TPOS/ TDATA	I	**Transmit Data Input; Data Input/Polarity Select.** Bipolar input for data to be transmitted on the twisted-pair line. Normally, pin 3 is TPOS and pin 4 is TNEG, the positive and negative sides of a bipolar input pair. However, when pin 4 is held High for at least 16 TCLK cycles (equivalent to 15 successive bipolar violations), the LXT317 switches to a unipolar mode. See Table 2 for Unipolar mode pin functions.
4	TNEG/ UBS	I	
5	MODE	I	**Mode Select.** Enables or disables zero suppression. Enables the HDB3 encoder/ decoder when tied to RCLK. Disables HDB3 encoder/decoder when tied Low.
6	RNEG/ BPV	O	**Receive Negative Data; Receive Positive Data.** Bipolar data outputs. A signal on RNEG corresponds to receipt of a negative pulse on RTIP/RRING. A signal on RPOS corresponds to receipt of a positive pulse on RTIP/RRING. RNEG/RPOS outputs are Non-Return-to-Zero (NRZ). Both outputs are stable and valid on the rising edge of RCLK. In Unipolar mode, pin 6 output is a bipolar violation indicator and pin 7 is the unipolar data output. See Table 2 for Unipolar mode functions.
7	RPOS/ RDATA	O	
8	RCLK	O	**Receive Clock.** This is the clock recovered from the signal received at RTIP and RRING.
9	–	–	***not used.*** Tie this pin to VCC through a 2.5 kΩ resistor.

Table 1: Pin Descriptions–continued

Pin #	Symbol	I/O	Description
10	GND	–	**Ground.** Tie this pin to ground.
11	GND	–	**Ground.** Tie this pin to ground.
12	LOS	O	**Loss Of Signal.** LOS goes High after 175 consecutive spaces and returns Low when the received signal reaches 12.5% mark density (minimum of four 1s within 32 bit periods, with no more than 15 consecutive 0s). Received marks are output on RPOS and RNEG even when LOS is High (during LOS condition).
13	TTIP	O	**Transmit Tip; Transmit Ring.** Differential Driver Outputs. These outputs are designed to drive a 50 - 200 Ω load. Line matching resistors and transformer can be selected to give the desired pulse height.
16	TRING	O	
14	TGND	–	**Tx Ground.** Ground return for the transmit drivers power supply TV+.
15	TV+	I	**Transmit Power Supply.** +5 VDC power supply input for the transmit drivers. TV+ must not vary from RV+ by more than ±0.3 V.
17	GND	–	**Ground.** This pin must be tied to ground.
18	LATN	O	**Line Attenuation Indication.** Encoded output. Pulse width, relative to RCLK, indicates receive equalizer gain setting (line insertion loss at 1024 kHz). When LATN = one RCLK pulse, the equalizer is set at 10 dB of gain; two pulses = 21 dB; three pulses =32 dB and four pulses = 0 dB. Output is valid on the rising edge of RCLK.
19	RTIP	I	**Receive Tip; Receive Ring.** The AMI signal received from the line is applied at these pins. A 1:1 transformer is required. Data and clock from the signal applied at these pins are recovered and output on the RPOS/RNEG, and RCLK pins.
20	RRING	I	
21	RV+	I	**Receive Power Supply.** +5 VDC power supply for all circuits except the transmit drivers. (Transmit drivers are supplied by TV+.)
22	RGND	–	**Rx Ground.** Ground return for power supply RV+.
23	–	–	***not used.*** This pin is inactive–*leave this pin floating.*
24	GND	–	**Ground.** This pin is inactive–*tie this pin to ground.*
25	GND	–	**Ground.** This pin is inactive–*tie this pin to ground.*
26	RLOOP	I	**Remote Loopback.** This input controls remote loopback. Setting RLOOP High enables Remote Loopback. During Remote Loopback, inline encoders and decoders are bypassed. Setting both RLOOP and LLOOP High while holding TAOS Low causes a Reset.
27	LLOOP	I	**Local Loopback.** This input controls local loopback. Setting LLOOP High enables Local Loopback Mode. Setting both RLOOP and LLOOP High while holding TAOS Low causes a Reset. Allow 32 ms to recover from Reset.
28	TAOS	I	**Transmit All Ones.** This pin controls the TAOS function. When tied High, TAOS causes the LXT317 to transmit a stream of marks at the TCLK frequency. Activating TAOS causes TPOS and TNEG inputs to be ignored. TAOS is inhibited during Remote Loopback, but can be activated simultaneously with Local Loopback.

Table 2: Unipolar Data I/O Pin Descriptions[1]

Pin #	Symbol	I/O	Description
3	TDATA	I	**Transmit Data.** Unipolar input for data to be transmitted on the twisted-pair line.
4	UBS	I	**Unipolar/Bipolar Select.** When pin 4 is held High for at least 16 TCLK cycles (equivalent to 15 successive bipolar violations), LXT317 switches to unipolar data I/O. The device immediately returns to bipolar I/O when pin 4 goes Low.
6	BPV	O	**Bipolar Violation.** Pin 6 goes High when a bipolar violation is received.
7	RDATA	O	**Receive Data.** Unipolar data output. RDATA is a Non-Return-to-Zero (NRZ) output. RDATA is stable and valid on the rising edge of RCLK.

1. Table 2 lists only those pins which are affected by the switch to unipolar data I/O.

FUNCTIONAL DESCRIPTION

NOTE

This functional description information is for design aid only

The LXT317 is a fully integrated PCM transceiver for 1.152 Mbps DECT applications. It allows full-duplex transmission of digital data over existing twisted-pair installations.

Table 1 lists the LXT317 pin assignments and signal descriptions. Table 2 lists the alternative pin assignments for unipolar data I/O mode. The LXT317 transceiver interfaces with two twisted-pair lines (one twisted-pair for transmit, one twisted-pair for receive) through standard pulse transformers and appropriate resistors.

The figure on the front of this Data Sheet shows a block diagram of the LXT317. Individual hard-wired pins control the transceiver. It can operate in either a bipolar (default) or unipolar data transmission mode. The LXT317 can also operate in one of several diagnostic modes, including Local Loopback, Remote Loopback and Transmit All Ones (TAOS).

TRANSMITTER

Input data (bipolar or unipolar) for transmission onto the line is clocked serially into the LXT317. The bipolar data inputs are at pin 3 (TPOS) and pin 4 (TNEG). The unipolar data input is at pin 3 (TDATA) only. Input data passes through the HDB3 encoder, if selected by connecting the MODE pin to RCLK. Input synchronization is supplied by the transmit clock (TCLK). Refer to the Test Specifications section for transmit timing.

Idle Mode

The LXT317 incorporates a transmit idle mode. This allows multiple transceivers to be connected to a single line for redundant applications or for testing purposes. TTIP and TRING remain in a high impedance state when TCLK is not present (TCLK grounded). Enabling Remote Loopback temporarily disables the high impedance state.

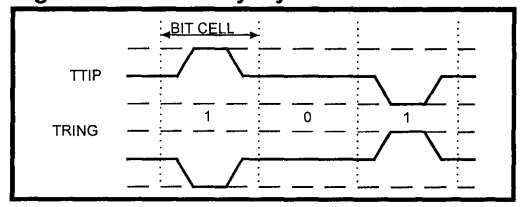
Short Circuit Limit

The LXT317 transmitter is equipped with a short-circuit limiter. This feature limits to approximately 120 mA RMS the current the transmitter will source into a low-impedance load. The limiter trips when the RMS current exceeds the limit for 120 µs (~ 150 marks). It automatically resets when the load current drops below the limit.

Line Code

The LXT317 transmits data as a 50% AMI line code as shown in Figure 2. Biasing of the transmit DC level is on-chip. Shaped pulses meeting the DECT requirements are applied to the AMI line driver for transmission onto the line at TTIP/TRING. The pulse conforms to the mask defined in ITU G.703, with the time scale expanded by a factor of $^{16}/_{9}$ for a nominal pulse width of 434 ns. Refer to Figure 11 and Table 8 for 1.152 Mbps pulse mask specifications.

Figure 2: 50% Duty Cycle Transmit Pulse



RECEIVER

The input from the twisted-pair is received via a 1:1 transformer. Recovered data is output at RPOS/RNEG (RDATA in unipolar mode), and the recovered clock is output at RCLK. Refer to the Test Specifications section for receiver timing.

The signal received at RTIP and RRING is processed through the receive equalizer which may apply up to 43 dB of gain. Insertion loss of the line, as indicated by the receive equalizer setting, is encoded in the LATN output as shown in Figure 5.

The equalized signal is filtered and applied to the peak detector and data slicers. The peak detector samples the inputs and determines the maximum value of the received signal. Fifty percent of the peak value is provided to the data slicers as a threshold level to ensure optimum signal-to-noise ratio.

The receiver is capable of accurately recovering signals with up to 43 dB of cable attenuation (from 2.7 V).

After processing through the data slicers, the received signal is routed to the data and timing recovery section, then to the HDB3 decoder (if selected) and to the LOS processor. The data and timing recovery sections provide an input jitter tolerance significantly better than required by ITU G.823, as shown in the Test Specifications section. The Test Specifications section also includes the jitter tolerance template.

If the incoming bit stream has jitter, the jitter transfer limit for the LXT317 is less than 1 dB up to 25 kHz; it then decreases by 20 dB per decade from 25 kHz to 100 kHz (using a 2^{15}-1 bit, PRBS signal). Refer to Figure 15 for the jitter transfer template.

The LOS processor loads a digital counter at the RCLK frequency. The count is incremented each time a 0 (space) is received, and reset to 0 each time a 1 (mark) is received. Upon receipt of 175 consecutive 0s the LOS pin goes High, and a smooth transition replaces the RCLK output with the MCLK.

Received marks will be output regardless of the LOS status, but the LOS pin will not reset until the 1s density reaches 12.5% (receipt of at least four 1s in any 32-bit periods, with no more than 15 consecutive 0s).

SELECTING UNIPOLAR OR BIPOLAR DATA MODE

The LXT317 operates in Bipolar Data mode by default. To enable Unipolar Mode, hold pin 4 High for 16 TCLK cycles. To return to Bipolar Mode immediately, pull pin 4 Low. To enable the HDB3 encoder/decoder circuits, connect pin 5 to RCLK.

INITIALIZATION AND RESET OPERATION

Upon power up, the transceiver is held static until the power supply reaches approximately 3V. Upon crossing this threshold, the device begins a 32 ms reset cycle to lock the transmit and receive Phase Lock Loops. The transmitter reference is provided by TCLK; the receive reference is provided by MCLK. All PLLs are continuously calibrated.

Command reset by holding RLOOP and LLOOP High simultaneously for 200 ns while holding TAOS Low. When the reset conditions end, the device begins the 32 ms cycle to calibrate the transmit and receive PLLs.

DIAGNOSTIC MODE OPERATION

Transmit All Ones. See Figure 3. In Transmit All Ones (TAOS) mode the TPOS and TNEG inputs to the transceiver are ignored and the transceiver transmits a continuous stream of 1s at the TCLK frequency. If there is no TCLK provided, TAOS is locked to the MCLK. This can be used as the AIS Alarm Indicator (AIS also called the Blue Alarm). Command TAOS by setting pin 28 High. TAOS can be commanded simultaneously with LLOOP as shown in Figure 4, but is inhibited during Remote Loopback.

Figure 3: Transmit All Ones

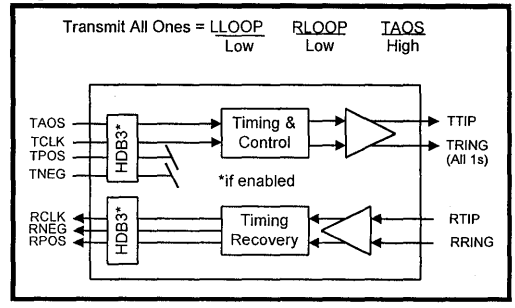


Figure 4: TAOS with LLOOP Data Path

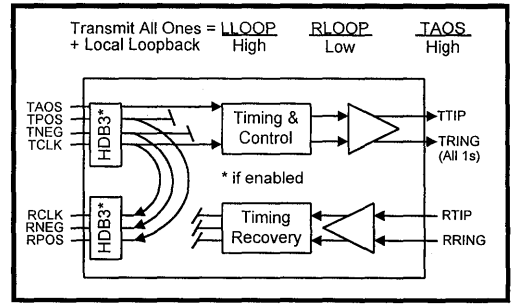
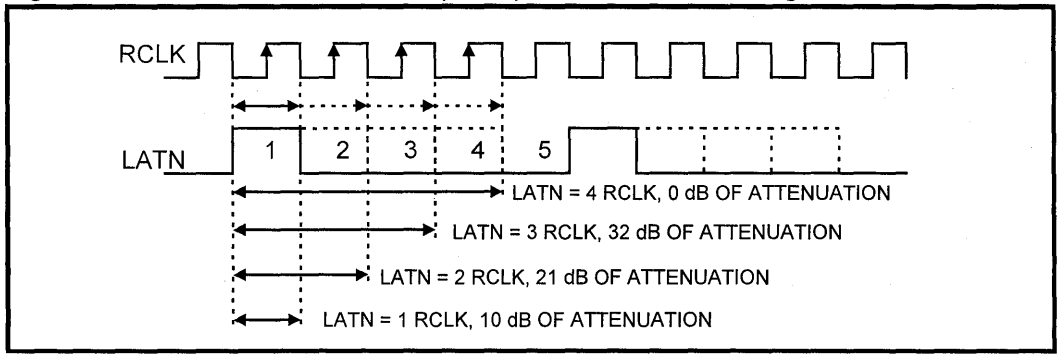


Figure 5: LXT317 Line Attenuation (LATN) Pulse Width Encoding



Local Loopback. Local Loopback (LLOOP) is designed to exercise the maximum number of functional blocks (See Figure 7). During LLOOP operation, the RTIP/RRING inputs from the line are disconnected. Instead, the transmit outputs are routed back into the receive inputs. This tests the encoders/decoders, transmitter, receiver and timing recovery sections. Enable Local Loopback by setting pin 27 High. If TAOS and LLOOP are both active, the All Ones pattern is transmitted onto the line while the TPOS/TNEG input data loops back to the RPOS/RNEG outputs.

Remote Loopback. See Figure 7. In Remote Loopback (RLOOP) mode, the transmit clock and data inputs (TCLK and TPOS/TNEG or TDATA) are ignored, and the in-line encoders and decoders are bypassed. The RPOS/RNEG or RDATA outputs are looped back through the transmit circuits and output on TTIP and TRING at the RCLK frequency. Receiver circuits are unaffected by the RLOOP command and continue to output the RCLK and RPOS/RNEG or RDATA signals received from the twisted-pair line. Command Remote Loopback by setting pin 26 High.

3

Figure 6: Local Loopback

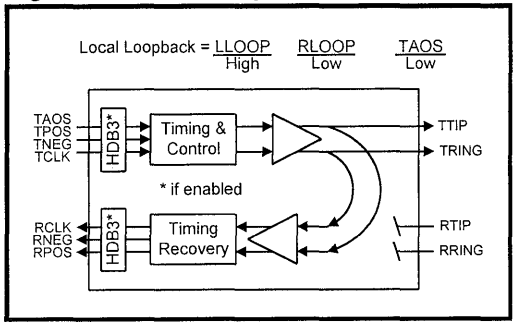
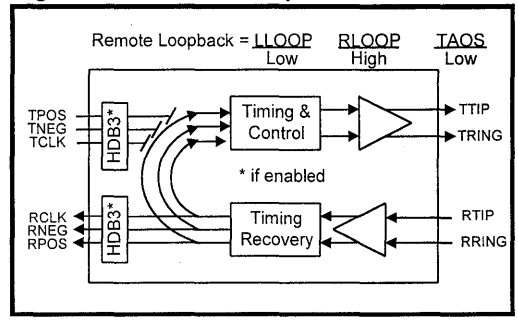


Figure 7: Remote Loopback



APPLICATION INFORMATION

NOTE

This application information is for design aid only.

LATN DECODING CIRCUITS AND EXTERNAL COMPONENTS

The line attenuation (LATN) output is encoded as a simple serial bit stream for use in line monitoring applications. Figure 8 is a typical decoding circuit for the LATN output. It uses a 2-bit synchronous counter (half of a 4-bit counter) with synchronous reset, and a pair of flip-flops. Table 3 provides the decoded output for each equalizer setting.

Figure 8: Typical LATN Decoding Circuit

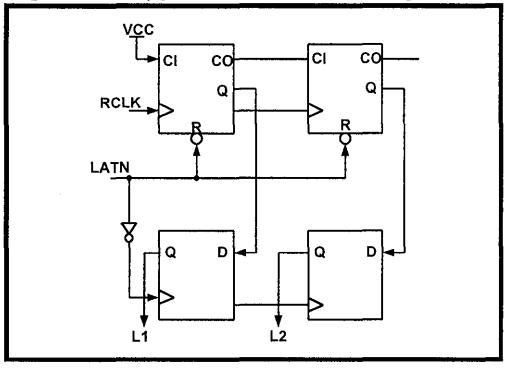


Table 3: Line Attenuation Decoding

L2	L1	Line Attenuation
0	0	0.0 dB
0	1	-10 dB
1	0	-21 dB
1	1	-32 dB

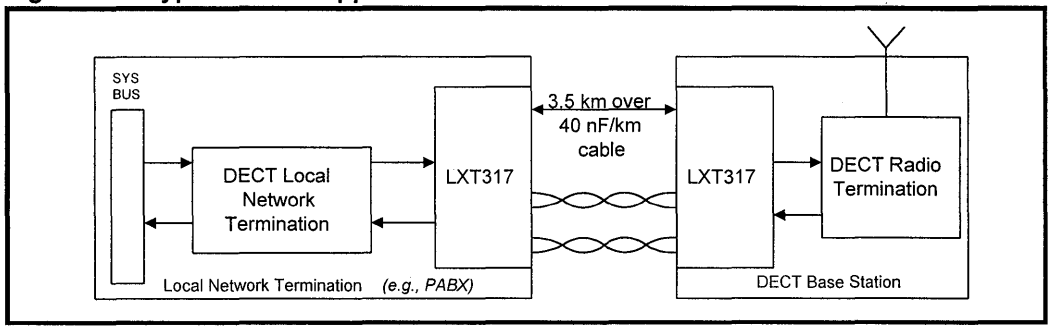
POWER REQUIREMENTS

The LXT317 is a low-power CMOS device. It operates from a single +5 V power supply which can be connected externally to both the transmitter and receiver. However, the two inputs must be within ±.3 V of each other, and decoupled separately to their respective grounds, as shown in Figure 10. Isolation between the transmit and receive circuits is provided internally.

Table 4: Approved Transformers

Transformer Type	Manufacturer	Part Number
Transmit (1:2)	Bell Fuse	0553-50061C
	Fil-Mag	66Z1308
	Midcom	671-5832
	Pulse	PE 65351
	Engineering	PE65771
	Schott	67127370
	Corp	67130850
Receive (1:1)	Fil-Mag	FE 8006-155
	Midcom	671-5792
	Pulse	PE 64936
	Engineering	PE 65778
	Schott	67130840
	Corp	67109510
Combination (Tx & Rx)	HALO	TD61-1205D2
	VALOR	PT5083

Figure 9: Typical DECT Application

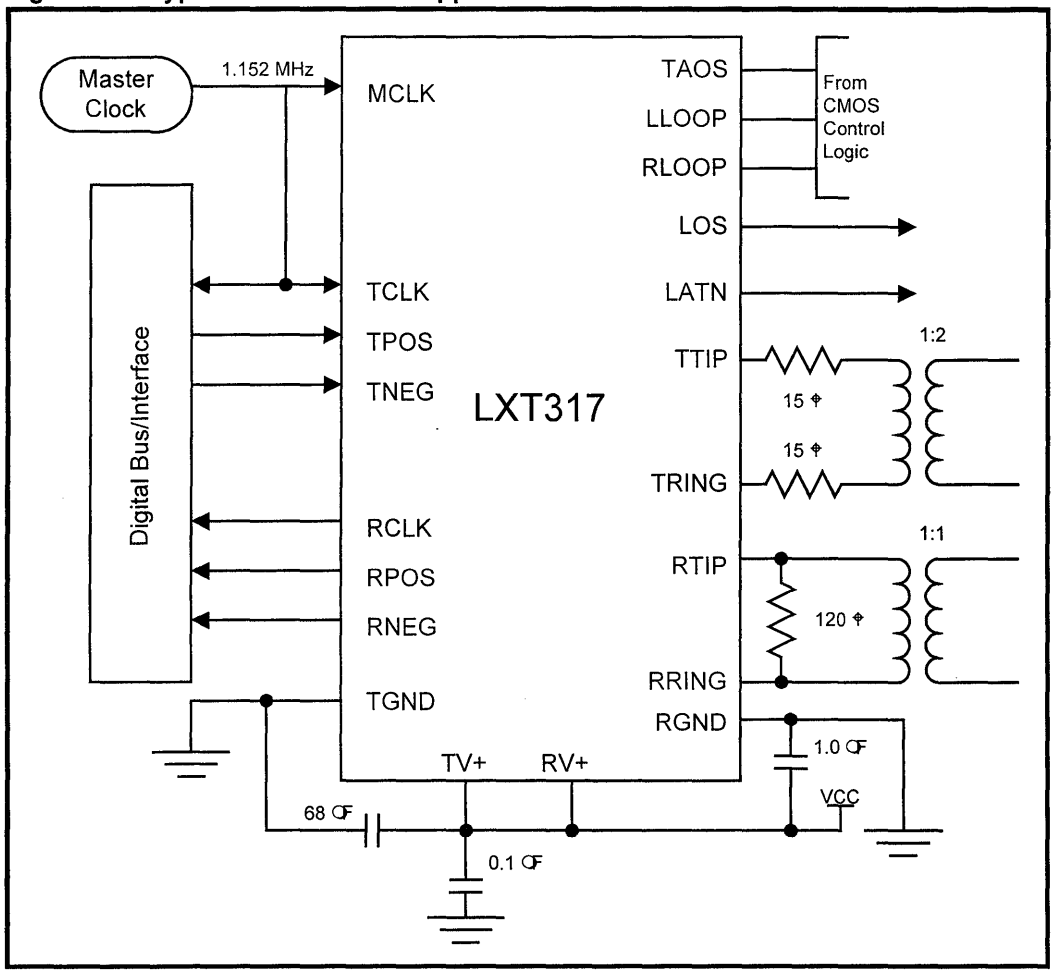


LXT317 CIRCUITRY

Figure 9 shows a typical DECT application with the LXT317. Figure 10 shows typical LXT317 circuit connections. The power supply inputs are tied to a common bus with appropriate decoupling capacitors (68 µF and 1.0 µF) installed on each side.

The line interfaces are relatively simple. A 120 Ω resistor (for TWP applications) across the input of a 1:1 transformer is used on the receive side, and a pair of 15 Ω resistors are installed in series with the 1:2 transmit transformer. (Table 4 lists approved transformers.)

Figure 10: Typical LXT317 DECT Application



TEST SPECIFICATIONS

NOTE

The minimum and maximum values in Tables 5 through 11 and Figures 11 through 15 represent the performance specifications of the LXT317 and are not guaranteed by test, except where noted by design.

Table 5: Absolute Maximum Ratings

Parameters	Symbol	Min	Max	Units
DC supply (referenced to GND)	RV+, TV+	–	6.0	V
Input voltage, any pin	VIN	RGND, -0.3	RV+, +0.3	V
Input current, any pin [1]	IIN	-10	10	mA
Ambient operating temperature	TA	-40	85	° C
Storage temperature	TSTG	-65	150	° C

CAUTION
Operation at or beyond these limits may permanently damage the device.
Normal operation is not guaranteed at these extremes.

1. Transient Currents of up to 100 mA will not cause SCR latch-up. TTIP, TRING, TV+, TGND can withstand continuous current of 100 mA.

Table 6: Recommended Operating Conditions and Characteristics

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
DC supply[2]	RV+, TV+	4.75	5.0	5.25	V	
Ambient operating temperature	T_A	-40	–	+85	°C	
Power dissipation[3]	P_D	–	300	400	mW	100% ones density & maximum line length @ 5.25 V

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. TV+ must not differ from RV+ by more than 0.3 V.
3. Power dissipation while driving 25 Ω load over operating temperature range. Includes device and load. Digital input levels are within 10% of the supply rails and digital outputs are driving a 50 pF capacitive load.

Table 7: Digital Characteristics (over the Recommended Range)

Parameter	Sym	Min	Typ	Max	Units	Test Conditions
High level input voltage (pins 1-5, 10, 26-28)	VIH	2.0	–	–	V	
Low level input voltage (pins 1-5, 10, 26-28)	VIL	–	–	0.8	V	
High level output voltage[1] (pins 6-8, 12)	VOH	3.8	–	–	V	IOUT = -400 µA
Low level output voltage[1] (pins 6-8, 12)	VOL	–	–	0.4	V	IOUT = 1.6 mA
Input leakage current	ILL	0	–	±10	µA	
Driver power down current[2]	IPD	–	–	±1.2	mA	direct connection to VCC or GND

1. Output drivers will output CMOS logic levels into CMOS loads.
2. TTIP,TRING only in Idle or Power Down Mode.

Figure 11: 1.152 MHz Pulse Mask

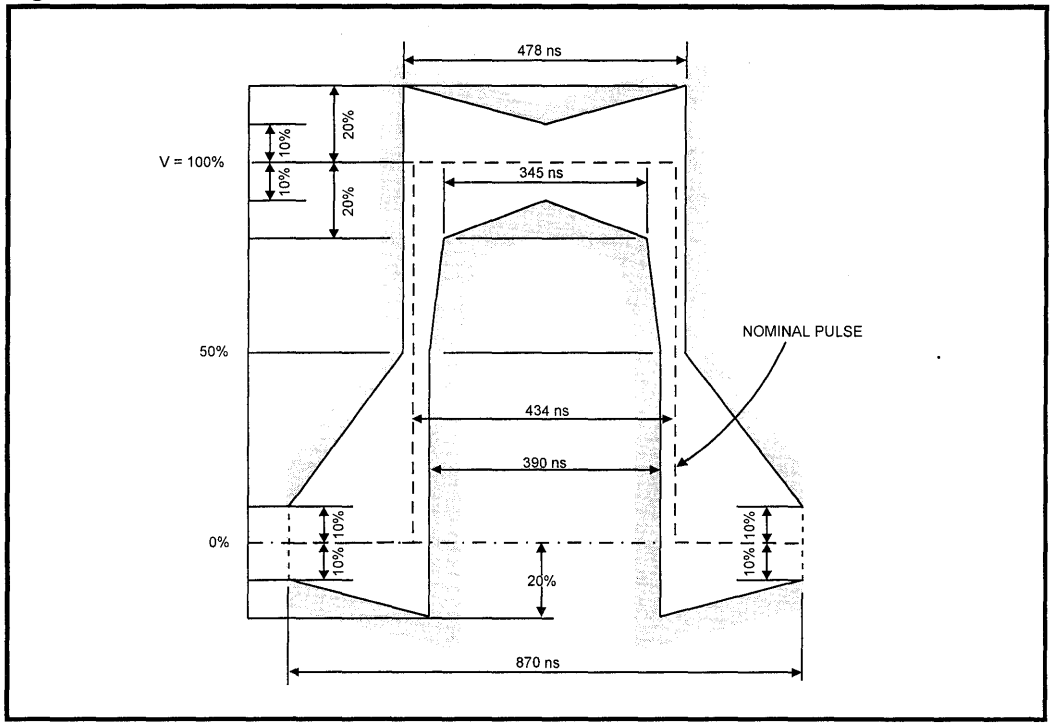


Table 8: 1.152 MHz Pulse Mask Parameters

Parameter	TPW	Units
Test load impedance	120	Ω
Nominal peak mark voltage	3.0	V
Nominal peak space voltage	0 ± 0.30	V
Nominal pulse width	434	ns
Ratio of positive and negative pulse amplitude at center of pulse	95-105	%
Ratio of positive and negative pulse amplitudes at nominal half amplitude	95-105	%

Table 9: Analog Characteristics (over the Recommended Range)

Parameter		Min	Typ[1]	Max	Units	Test Conditions
Recommended output load at TTIP and TRING		50	120	200	Ω	
AMI output pulse amplitudes		2.7	3.0	3.3	V	Measured at the output
Jitter added by the transmitter[2]	20 Hz - 100 kHz	–	–	0.05	UI (pp)	
Input jitter tolerance	20 kHz - 100 kHz	0.2	0.3	–	UI	0 - 43 dB line
	10 Hz	100	500	–	UI	
Round Trip Chip Data Delay[2, 3, 4]	TDATA to Transmitter	–	5.5	–	bits	
	Receiver to RDATA	–	7.0	–	bits	
Receive signal attenuation range @ 576 kHz		+1	-43.0	–	dB	
Allowable consecutive 0s before LOS declared		160	175	190		
Return loss[3]		**Transmit**		**Receive**		
		Min	**Typ**	**Min**	**Typ**	
	29 kHz - 58 kHz	12	15	12	15	dB
	58 kHz - 1.152 MHz	15	16	16	18	dB
	1.152 MHz - 2.304 MHz	14	18	14	18	dB

1. Typical values are at 25 °C and are for design aid only, not guaranteed and not subject to production testing.
2. Input signal to TCLK is jitter free.
3. Guaranteed by characterization; not subject to production testing.
4. Using HDB3 encoders and decoders in data path.

Table 10:LXT317 Master Clock and Transmit Timing Characteristics (See Figure 12)

Parameter	Sym	Min	Typ[1]	Max	Units	Notes
MCLK frequency	MCLK	–	1.152	–	MHz	
MCLK tolerance	MCLKt	–	–	±100	ppm	
MCLK duty cycle	MCLKd	40	–	60	%	
TCLK frequency	TCLK	–	1.152	–	MHz	
TCLK tolerance	TCLKt	–	–	±100	ppm	
TCLK duty cycle	TCLKd	10	–	90	%	
TPOS/TNEG to TCLK setup time	tSUT	50	–	–	ns	
TCLK to TPOS/TNEG hold time	tHT	50	–	–	ns	

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 12: LXT317 Transmit Clock Timing

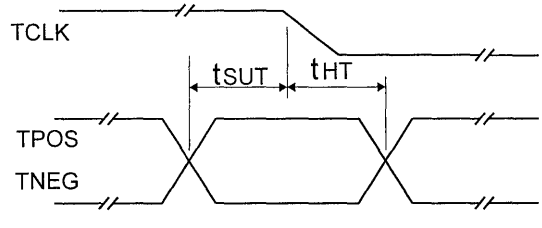


Table 11: LXT317 Receive Timing Characteristics (see Figure 13)

Parameter	Sym	Min	Typ[1]	Max	Units	Notes
RCLK duty cycle[2]	RCLKd	40	50	60	%	
RCLK width[2]	tPW	–	868	–	ns	
RCLK pulse width high	tPWH	398	434	–	ns	
RCLK pulse width low	tPWL	398	434	470	ns	
RPOS/RNEG to RCLK rising setup time	tSUR	300	384	–	ns	
RCLK rising to RPOS/RNEG hold time	tHR	300	384	–	ns	

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. RCLK duty cycle widths will vary depending on extent of received pulse jitter displacement. Max and min RCLK duty cycles are for worst case jitter conditions (0.4 UI clock displacement for 1.152 MHz.)

Figure 13: LXT317 Receive Clock Timing

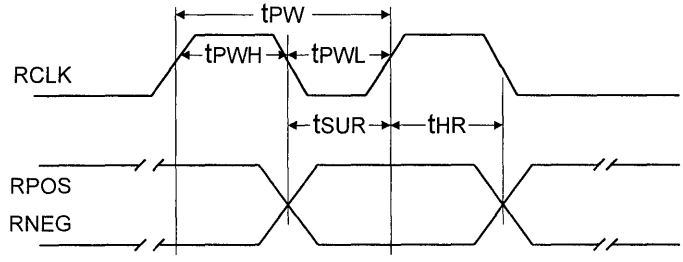


Figure 14: Typical LXT317 Jitter Tolerance @ 43 dB

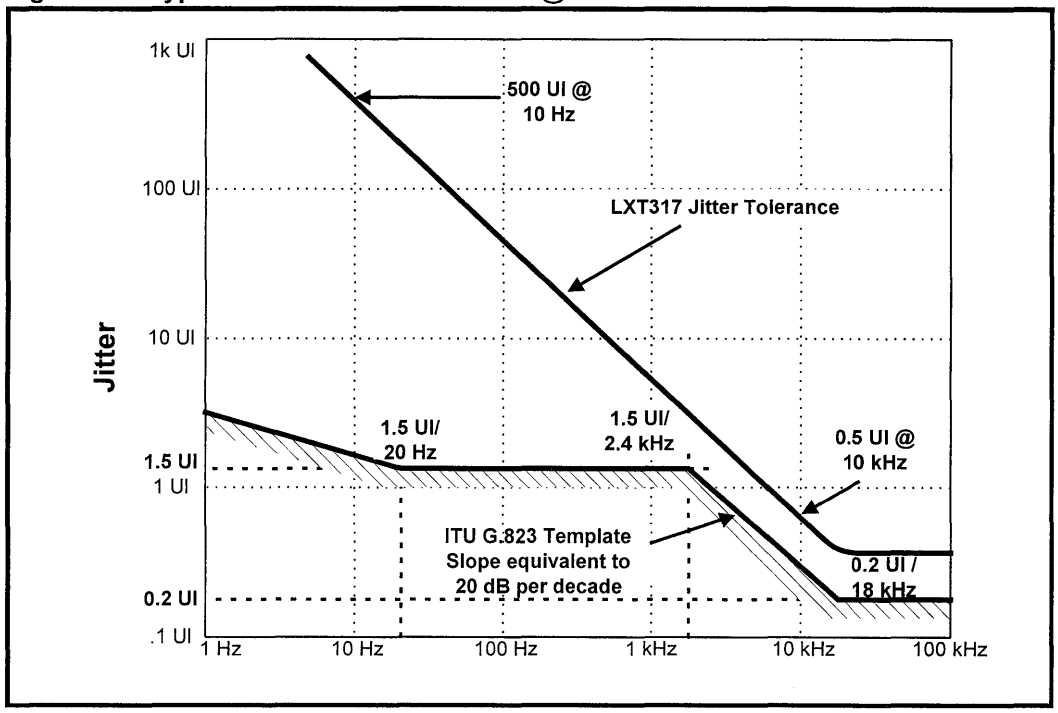
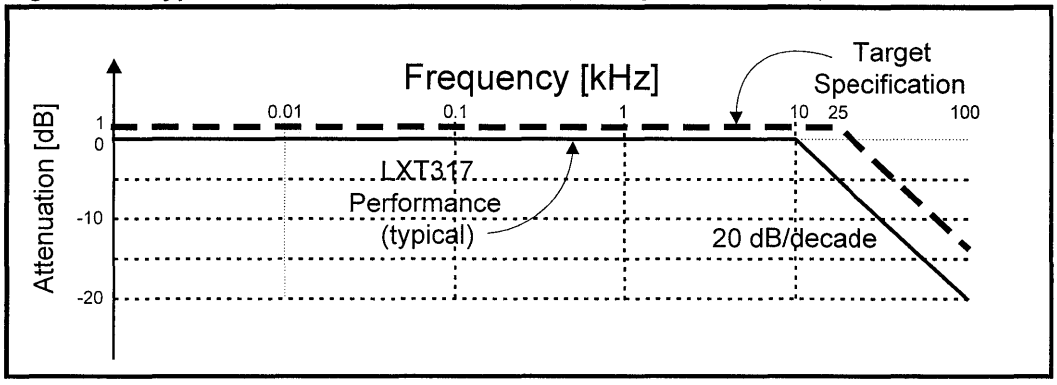


Figure 15: Typical LXT317 Jitter Attenuation (Test Signal PRBS = 2^{15}-1)



NOTES

LXT318

E1 NTU/ISDN PRI Transceiver

General Description

The LXT318 is the first fully integrated transceiver for E1 Network Termination Unit (NTU) and ISDN Primary Rate Interface (ISDN PRI) applications at 2.048 Mbps. The transceiver operates from 0.0 km to 2.6 km of 0.6 mm (22 AWG) twisted-pair cable with no external components.

The LXT318 offers selectable HDB3 encoding/decoding, and unipolar or bipolar data I/O. The LXT318 also provides jitter attenuation in either the transmit or receive direction starting at 3 Hz, and incorporates a serial interface (SIO) for microprocessor control.

The LXT318 offers a variety of diagnostic features including loopbacks and loss of signal monitoring. It is built using an advanced double-poly, double-metal CMOS process and requires only a single 5-volt power supply.

Applications

- PCM 30/ISDN PRI Interface (ITU G.703, I.431)
- NTU (interface to E1 Service)
- E1 Mux or LAN bridge - Campus Networking
- Wireless Base Stations/Networking
- CPU to CPU Channel Extenders
- Digital Loop Carrier — Subscriber Carrier Systems
- Channel Banks
- HDSL - E1 Extension

Features

- Fully integrated transceiver comprising: on-chip equalizer; timing recovery/control; data processor; receiver; transmitter and digital control
- Pin compatible with the LXT310 T1 CSU/ISDN PRI (1.544 Mbps) transceiver
- Meets or exceeds latest ITU specifications including G.703, G.736, G.823, and I.431
- Meets ETSI 300011 and 300233 standards
- Jitter attenuation starting at 3 Hz, switchable to transmit or receive path
- Exceeds ETSI TBR12/13 jitter transfer performance specifications
- Fully restores the received signal after transmission via a cable with attenuation of 43 dB @ 1024 kHz
- Selectable Unipolar or Bipolar data I/O
- Selectable HDB3 encoding/decoding
- Output short circuit current limit protection
- Meets 50 mARMS short-circuit current limit (per OFTEL OTR-001)
- On-line idle mode for testing or for redundant systems
- Local and remote loopback functions
- Receive monitor with Loss of Signal (LOS) output
- Microprocessor controllable
- Available in 28-pin DIP and PLCC
- Extended Temperature Range (-40° C to +85° C)

LXT318 Block Diagram

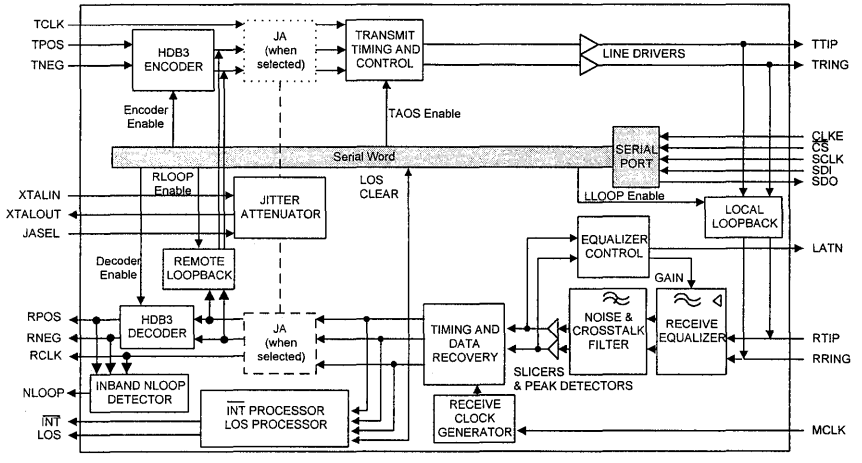


Figure 1: LXT318 Pin Assignments

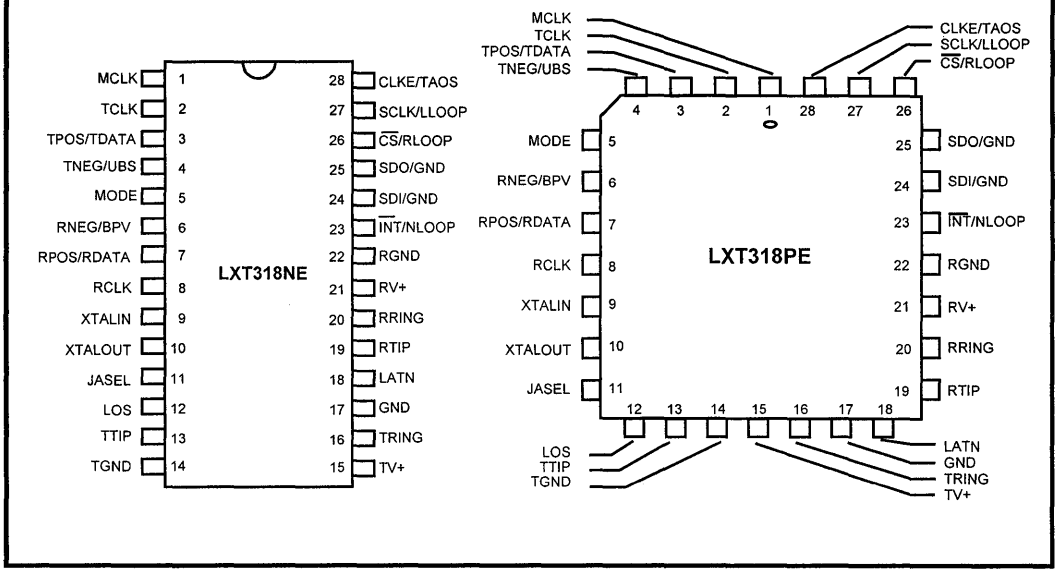


Table 1: Pin Descriptions

Pin #	Symbol	I/O	Description
1	MCLK	I	**Master Clock.** A 2.048 MHz clock input used to generate internal clocks. Upon loss of Signal (LOS), RCLK is derived from MCLK. If MCLK is not applied, this pin should be grounded.
2	TCLK	I	**Transmit Clock.** Transmit clock input. TPOS and TNEG are sampled on the falling edge of TCLK. Ground this pin if TCLK is not supplied.
3	TPOS/ TDATA	I	**Transmit Data Input; Data Input/Polarity Select.** Input for data to be transmitted on the twisted-pair line. Normally, pin 3 is TPOS and pin 4 is TNEG, the positive and negative sides of a bipolar input pair. However, when pin 4 is held High for at least 16 TCLK cycles (equivalent to 15 successive bipolar violations), the LXT318 switches to a unipolar mode. Unipolar mode pin functions are listed in Table 2.
4	TNEG/UBS	I	
5	MODE	I	**Mode Select.** Setting MODE High puts the LXT318 in the Host mode. In the Host mode, the serial interface is used to control the LXT318 and determine its status. Setting MODE Low puts the LXT318 in the Hardware (H/W) mode. In the Hardware mode the serial interface is disabled and hard-wired pins are used to control configuration and report status. Tying MODE to RCLK activates the Hardware mode and enables the HDB3 encoder/decoder.
6	RNEG/BPV	O	**Receive Negative Data; Receive Positive Data.** Bipolar data outputs. A signal on RNEG corresponds to receipt of a negative pulse on RTIP/RRING. A signal on RPOS corresponds to receipt of a positive pulse on RTIP/RRING. RNEG/RPOS outputs are Non-Return-to-Zero (NRZ). In Host mode, CLKE determines the clock edge at which these outputs are stable and valid. In Hardware mode both outputs are stable and valid on the rising edge of RCLK. In Unipolar mode, pin 6 output is a bipolar Violation indication and pin 7 is the unipolar data output. See Table 2 for Unipolar mode functions.
7	RPOS/ RDATA	O	

Table 1: Pin Descriptions – continued

Pin #	Symbol	I/O	Description
8	RCLK	O	**Receive Clock.** This is the clock recovered from the signal received at RTIP and RRING.
9	XTALIN	I	**Crystal Input; Crystal Output.** An external crystal (18.7 pF load capacitance, pullable) operating at four times the bit rate (8.192 MHz) is required to enable the jitter attenuation function of the LXT318. These pins may also be used to disable the jitter attenuator by connecting the XTALIN pin to the positive supply through a resistor, and leaving the XTALOUT pin unconnected or tied to ground.
10	XTALOUT	O	
11	JASEL	I	**Jitter Attenuation Select.** Selects jitter attenuation location. When JASEL is High, the jitter attenuator is active in the receive path. When JASEL is Low, the jitter attenuator is active in the transmit path.
12	LOS	O	**Loss Of Signal.** LOS goes High after 175 consecutive spaces and returns Low when the received signal reaches 12.5% mark density (minimum of four marks within 32 bit periods, with no more than 15 consecutive 0s). Received marks are output on RPOS and RNEG even when LOS is High.
13 16	TTIP TRING	O	**Transmit Tip.** Differential Driver Outputs. These outputs are designed to drive a 50 - 200 Ω load. Line matching resistors and transformer can be selected to give the desired pulse height.
14	TGND	–	**Tx Ground.** Ground return for the transmit drivers power supply TV+.
15	TV+	I	**Transmit Power Supply.** +5 VDC power supply input for the transmit drivers. TV+ must not vary from RV+ by more than ±0.3V.
17	GND	–	**Ground.** This pin must be tied to ground.
18	LATN	O	**Line Attenuation Indication.** Encoded output. Pulse width, relative to RCLK, indicates receive equalizer gain setting (line insertion loss at 1024 kHz) in 9.5 dB steps. When LATN is High for one RCLK pulse, the equalizer is set at 9.5 dB gain; 2 pulses = 19 dB; 3 pulses = 28.5 dB and 4 pulses = 0 dB. Output is valid on the rising edge of RCLK.
19	RTIP	I	**Receive Tip; Receive Ring.** The HDB3 signal received from the line is applied at these pins. A 1:1 transformer is required. Data and clock from the signal applied at these pins are recovered and output on the RPOS/RNEG, and RCLK pins.
20	RRING	I	
21	RV+	I	**Receive Power Supply.** +5 VDC power supply for all circuits except the transmit drivers. (Transmit drivers are supplied by TV+.)
22	RGND	–	**Rx Ground.** Ground return for power supply RV+.
23	$\overline{\text{INT}}$	O	**Interrupt *(Host Mode)*.** In Host mode, this pin goes Low to flag the host processor when LOS changes state. $\overline{\text{INT}}$ is an open drain output and should be tied to power supply RV+ through a resistor. Reset $\overline{\text{INT}}$ by clearing the LOS register bit.
	NLOOP	O	**Network Loopback Detection *(H/W Mode)*.** In Hardware mode, this pin indicates that inband network loopback is active by going High. To set this signal High, the device must receive the NLOOP activation pattern (00001) for five seconds. To reset it Low, either the device must receive the deactivation pattern (001) for five seconds or either RLOOP or LLOOP must be activated.
24	SDI	I	**Serial Data In *(Host Mode)*.** The serial data input stream is applied to this pin when the LXT318 operates in the Host mode. SDI is sampled on the rising edge of SCLK.
	GND	–	**Ground *(H/W Mode)*.** This pin is inactive in the Hardware mode and should be tied to ground.

Table 1: Pin Descriptions – continued

Pin #	Symbol	I/O	Description
25	SDO	O	**Serial Data Out** ***(Host Mode).*** In the Host mode, serial data from the on-chip register is output on this pin. If CLKE is High, SDO is valid on the rising edge of SCLK. If CLKE is Low, SDO is valid on the falling edge of SCLK. SDO goes to a high-impedance state when the serial port is being written to.
	GND	–	**Ground** ***(H/W Mode).*** This pin is inactive in the Hardware mode and should be tied to ground.
26	$\overline{CS}$	I	**Chip Select** ***(Host Mode).*** In the Host mode, this input is used to access the serial interface. For each read or write operation, $\overline{CS}$ must transition from High to Low, and remain Low.
	RLOOP	I	**Remote Loopback** ***(H/W Mode).*** In the Hardware mode, this input controls remote loopback. Setting RLOOP High enables Remote Loopback. During Remote Loopback, inline encoders and decoders are bypassed. Setting both RLOOP and LLOOP while holding TAOS Low causes a Reset.
27	SCLK	I	**Serial Clock** ***(Host Mode).*** In the Host mode, this clock is used to write data to, or read data from the serial interface register.
	LLOOP	I	**Local Loopback** ***(H/W Mode).*** In the Hardware mode, this input controls local loopback. Setting LLOOP High enables Locale Loopback Mode. Setting both RLOOP and LLOOP while holding TAOS Low causes a Reset.
28	CLKE	I	**Clock Edge** ***(Host Mode).*** In the Host mode, this pin controls transitions of the data outputs. Setting CLKE High causes RPOS and RNEG to be valid on the falling edge of RCLK, and SDO to be valid on the rising edge of SCLK. When CLKE is Low, RPOS and RNEG are valid on the rising edge of RCLK, and SDO is valid on the falling edge of SCLK.
	TAOS	I	**Transmit All Ones** ***(H/W Mode).*** In the Hardware mode, this pin controls the TAOS function. When set High, TAOS causes the LXT318 to transmit a stream of marks at the TCLK frequency. Activating TAOS causes TPOS and TNEG inputs to be ignored. TAOS is inhibited during Remote Loopback.

Table 2: Unipolar Data I/O Pin Descriptions[1]

Pin #	Symbol	I/O	Description
3	TDATA	I	**Transmit Data.** Unipolar input for data to be transmitted on the twisted-pair line.
4	UBS	I	**Unipolar/Bipolar Select.** When pin 4 is held High for at least 16 TCLK cycles (equivalent to 15 successive bipolar violations), LXT318 switches to unipolar data I/O. The device immediately returns to bipolar I/O when pin 4 goes Low.
6	BPV	O	**Bipolar Violation.** Pin 6 goes High when a bipolar violation is received.
7	RDATA	O	**Receive Data.** Unipolar data output. RDATA is a Non-Return-to-Zero (NRZ) output. In Host mode, CLKE determines the clock edge at which RDATA is stable and valid. In Hardware mode RDATA is stable and valid on the rising edge of RCLK.

1. Table 2 lists only those pins which are affected by the switch to unipolar data I/O.

FUNCTIONAL DESCRIPTION

NOTE

This functional description is for design aid only.

The LXT318 is a fully integrated PCM transceiver for 2.048 Mbps (E1) applications. It allows full-duplex transmission of digital data over existing twisted-pair installations.

The LXT318 transceiver interfaces with two twisted-pair lines (one twisted-pair for transmit, one twisted-pair for receive) through standard pulse transformers and appropriate resistors.

The figure on the front page of this data sheet shows a block diagram of the LXT318. This transceiver may be controlled by a microprocessor through the serial port (Host Mode), or by individual pin settings (Hardware Mode). The jitter attenuator may be positioned in either the transmit or receive path, as determined by JASEL.

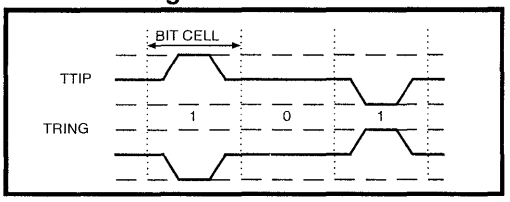
TRANSMITTER

Input data (bipolar or unipolar) for transmission onto the line is clocked serially into the LXT318. Bipolar data is input at TPOS and TNEG. Unipolar data is input at TDATA only (Unipolar mode is enabled by holding TNEG High for 16 RCLK cycles). Input data may be passed through the Jitter Attenuator and/or HDB3 encoder, if selected. In Host mode, HDB3 is selected by setting bit D2 of the input data byte. In Hardware mode, HDB3 is selected by connecting the MODE pin to RCLK. Input synchronization is supplied by the transmit clock (TCLK). Timing requirements for TCLK and the Master Clock (MCLK) are defined in the Test Specifications section. When TCLK is not supplied, the TCLK pin must be grounded.

Line Code

The LXT318 transmits data as a 50% HDB3 line code as shown in Figure 2. Biasing of the transmit DC level is on-chip. Shaped pulses meeting the various ITU requirements are applied to the HDB3 line driver for transmission onto the line at TTIP and TRING. Refer to Figure 22 and Table 15 for 2.048 Mbps pulse mask specifications.

Figure 2: 50% Duty Cycle Coding Diagram



Idle Mode

The LXT318 incorporates a transmit idle mode. This allows multiple transceivers to be connected to a single line for redundant applications or for testing purposes. TTIP and TRING remain in a high impedance state when TCLK is not present (TCLK grounded). The high impedance state can be temporarily disabled by enabling Remote Loopback.

Short Circuit Limit

The LXT318 transmitter is equipped with a short-circuit limiter. This feature limits to approximately 120 mA RMS the current the transmitter will source into a low-impedance load. The limiter trips when the RMS current exceeds the limit for 100 µs (~ 150 marks). It automatically resets when the load current drops below the limit.

The LXT318 will meet or exceed the OFTEL OTR-001 short circuit limit (50 mARMS) when the design includes a 1:2 transmit transformer and 15 Ω resistors on TTIP and TRING. The device also meets or exceeds ITU specifications for NTU applications, as well as requirements for ISDN PRI.

RECEIVER

The receiver input from the twisted-pair is received via a 1:1 transformer. Recovered data is output at RPOS/RNEG (RDATA in unipolar mode), and the recovered clock is output at RCLK. Refer to the Test Specifications section.

The signal received at RTIP and RRING is processed through the receive equalizer which may apply up to 43 dB of gain. Insertion loss of the line, as indicated by the receive equalizer setting, is encoded in the LATN output as shown in Figure 3.

The equalized signal is filtered and applied to the peak detector and data slicers. The peak detector samples the inputs and determines the maximum value of the received signal. A percentage of the peak value is provided to the data slicers as a threshold level to ensure optimum signal-to-noise ratio. The threshold is set to 50% of the peak value. The receiver is capable of accurately recovering signals with up to 43 dB of cable attenuation (from 2.7 V).

After processing through the data slicers, the received signal is routed to the data and timing recovery section, then to the HDB3 decoder (if selected) and to the LOS processor. The data and timing recovery sections provide an input jitter tolerance significantly better than required by ITU G.823, as shown in the Test Specifications section.

The LOS Processor loads a digital counter at the RCLK frequency. The count is incremented each time a 0 (space)

is received, and reset to 0 each time a one (mark) is received. Upon receipt of 175 consecutive 0s the LOS pin goes High, and a smooth transition replaces the RCLK output with the MCLK. (During LOS, if MCLK is not supplied and JASEL is High, the RCLK output is replaced with the centered quartz crystal frequency.)

Received marks will be output regardless of the LOS status, but the LOS pin will not reset until the ones density reaches 12.5%. This level is based on receipt of at least four 1s in any 32 bit periods, with no more than 15 consecutive 0s.

Jitter Attenuation

Jitter attenuation is provided by a Jitter Attenuation Loop (JAL) and an Elastic Store (ES). The Test Specifications show the LXT318 jitter attenuation performance compared with the jitter template specified by ITU G.736. The 3 dB corner frequency for the LXT318 is at 3 Hz. The performance complies with ETSI TBR-12 and TBR-13. An external crystal oscillating at four times the bit rate provides clock stabilization. The ES is a 32 x 2-bit register. When JASEL is High, the JAL is positioned in the receive path. When JASEL Low, the JAL is positioned in the transmit path.

Data (TPOS/TNEG or TDATA; or RPOS/RNEG or RDATA) is clocked into the ES with the associated clock signal (TCLK or RCLK), and clocked out of the ES with the dejittered clock from the JAL. When the bit count in the ES is within two bits of overflowing or underflowing, the ES adjusts the output clock by $^1/_8$ of a bit period. The ES produces an average delay of 16 bits in the associated path.

CONTROL MODES

The LXT318 transceiver can be controlled by a microprocessor through a serial interface (Host mode), or through individual hard-wired pins (Hardware mode). The mode of operation is determined by the input to MODE. With MODE set High, the LXT318 operates in the Host mode. With MODE set Low, the LXT318 operates in the Hardware mode. With MODE tied to RCLK, the LXT318 operates in the Hardware mode with the HDB3 encoder/decoder enabled. The LXT318 can also be commanded to operate in one of several diagnostic modes.

Host Mode Control

The LXT318 operates in the Host mode when MODE is set High. In Host mode the LXT318 is controlled through the serial I/O port (SIO) by a microprocessor. The LXT318 provides a pair of data registers, one for command inputs and one for status outputs, and an interrupt output.

An SIO transaction is initiated by a High-to-Low transition on $\overline{CS}$. The LXT318 responds by writing the incoming serial word from the SDI pin into its command register. If the command word contains a read request, the LXT318 subsequently outputs the contents of its status register onto the SDO pin. The Clock Edge (CLKE) signal determines when the SDO and receive data outputs are valid, relative to the Serial Clock (SCLK) or RCLK as in Table 3.

The 16-bit serial word consists of an 8-bit Command/Address byte and an 8-bit Data byte as shown in Figures 4 and 5. SIO timing characteristics are shown in Table 14.

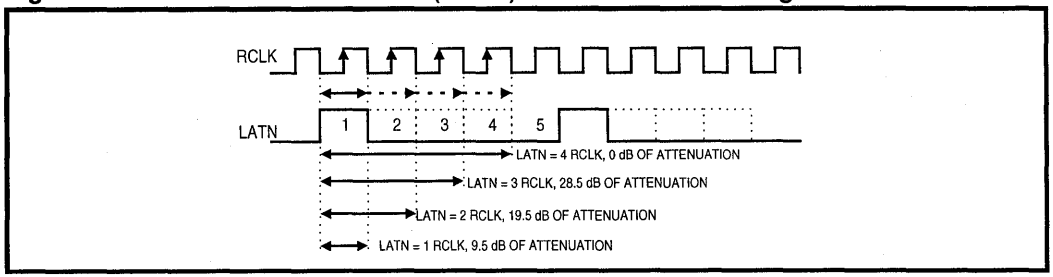
Table 3: CLKE Settings

CLKE	Output	Clock	Valid Edge
LOW	RPOS	RCLK	Rising
	RNEG	RCLK	Rising
	SDO	SCLK	Falling
HIGH	RPOS	RCLK	Falling
	RNEG	RCLK	Falling
	SDO	SCLK	Rising

Table 4: SIO Input Bit Settings (Figure 4)

Mode	RLOOP Bit D5	LLOOP Bit D6	TAOS Bit D7
RLOOP	1	0	n/a
LLOOP	0	1	n/a
TAOS	0	n/a	1
RESET	1	1	0

Figure 3: LXT318 Line Attenuation (LATN) Pulse Width Encoding



SERIAL INPUT WORD

Figure 4 shows the Serial Input data structure. The LXT318 is addressed by setting bit A4 in the Address/Command byte, corresponding to address 16. Bit 1 of the serial Address/Command byte provides Read/Write (R/$\overline{W}$) control when $\overline{CS}$ is Low. The R/$\overline{W}$ bit is set to logic 1 to read the data output byte from the chip, and set to logic 0 to write the input data byte to the chip.

The Data Input byte is the second eight bits of a write operation. The first bit (D0) clears and/or masks LOS interrupts. The second bit (D1) clears and/or masks NLOOP detection interrupts. The third bit (D2) enables or disables HDB3 coding/decoding, and the last 3 bits (D5 - D7) control operating modes (normal and diagnostic) and chip reset. Refer to Table 4 for details on bits D5 - D7.

SERIAL OUTPUT WORD

Figure 5 shows the Serial Output data structure. When the Serial Input word has bit A0 = 1, the LXT318 drives the output data byte onto the SDO pin. The output data byte reports Loss of Signal (LOS) conditions, NLOOP detection status, HDB3 code setting, and operating modes (normal or diagnostic as shown in Table 5. The first bit (D0) reports LOS status. The second bit (D1) reports network loopback detection status. The third bit (D2) reports the HDB3 setting. The last 3 bits (D5 - D7) report operating modes and interrupt status.

The Host mode provides a latched Interrupt output pin, $\overline{INT}$. An interrupt is triggered by a change in the LOS bit (D0 of the output data byte). If the $\overline{INT}$ line is High (no interrupt is pending), bits D5 - D7 report the operating modes listed in Table 5. If the $\overline{INT}$ line is Low, the interrupt status overrides all other reports and bits D5 - D7 reflect the interrupt status as listed in Table 5.

Hardware Mode Operation

In Hardware mode the transceiver is accessed and controlled through individual pins. With the exception of the $\overline{INT}$ and CLKE functions, Hardware mode provides all the functions provided in the Host mode. In the Hardware mode RPOS/RNEG or RDATA outputs are valid on the rising edge of RCLK. The LXT318 operates in Hardware mode only when MODE is Low or connected to RCLK.

INITIALIZATION AND RESET OPERATION

Upon power up, the transceiver is held static until the power supply reaches approximately 3V. Upon crossing this threshold, the device begins a 32 ms reset cycle to calibrate the transmit and receive delay lines and lock the Phase Lock Loop to the receive line. A reference clock is required to calibrate the delay lines. The transmitter reference is provided by TCLK. The crystal oscillator provides the receiver reference. If the crystal oscillator is grounded, MCLK is used as the receiver reference clock. All PLLs are continuously calibrated.

The transceiver can also be reset from the Host or Hardware mode. In Host mode, command reset by simultaneously writing 1s to RLOOP and LLOOP, and a 0 to TAOS. In Hardware mode, reset by holding RLOOP and LLOOP High simultaneously for 200 ns while holding TAOS Low. In either mode, reset sets all registers to 0.

Table 5: LXT318 Serial Data Output Bit Coding (See Figure 5)

Bit			Status
D5	D6	D7	
Operating Modes			
0	0	0	Reset has occurred, or no program input.
0	0	1	TAOS active
0	1	0	LLOOP active
0	1	1	TAOS and LLOOP active
1	0	0	RLOOP active
Interrupt Status			
1	0	1	NLOOP has changed state since last Clear NLOOP occurred.
1	1	0	LOS has changed state since last Clear LOS occurred.
1	1	1	LOS and NLOOP have both changed state since last Clear NLOOP and Clear LOS occurred.

Figure 4: LXT318 Serial I/O Input Data Structure

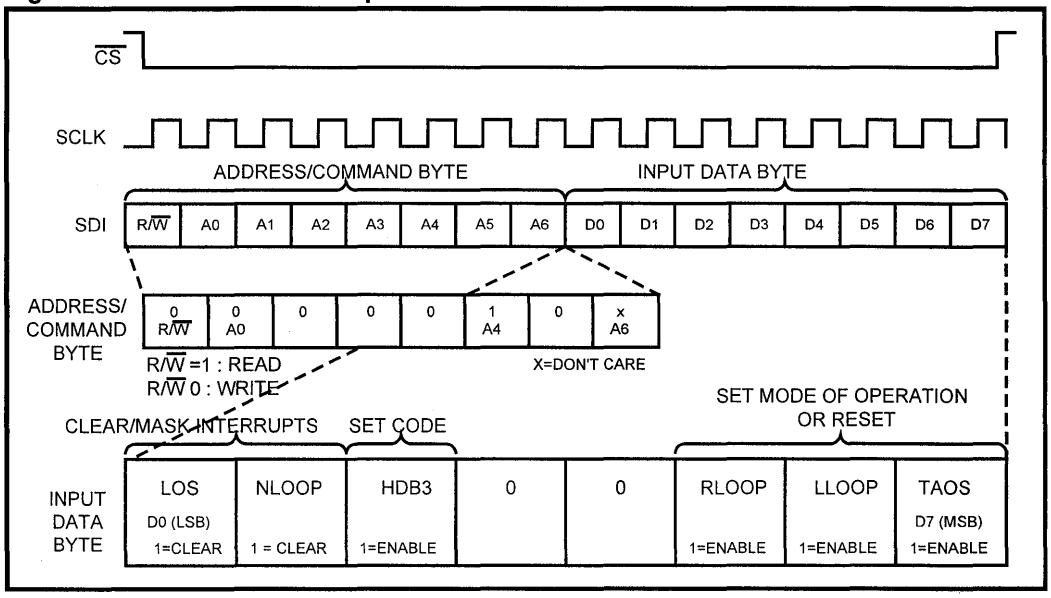
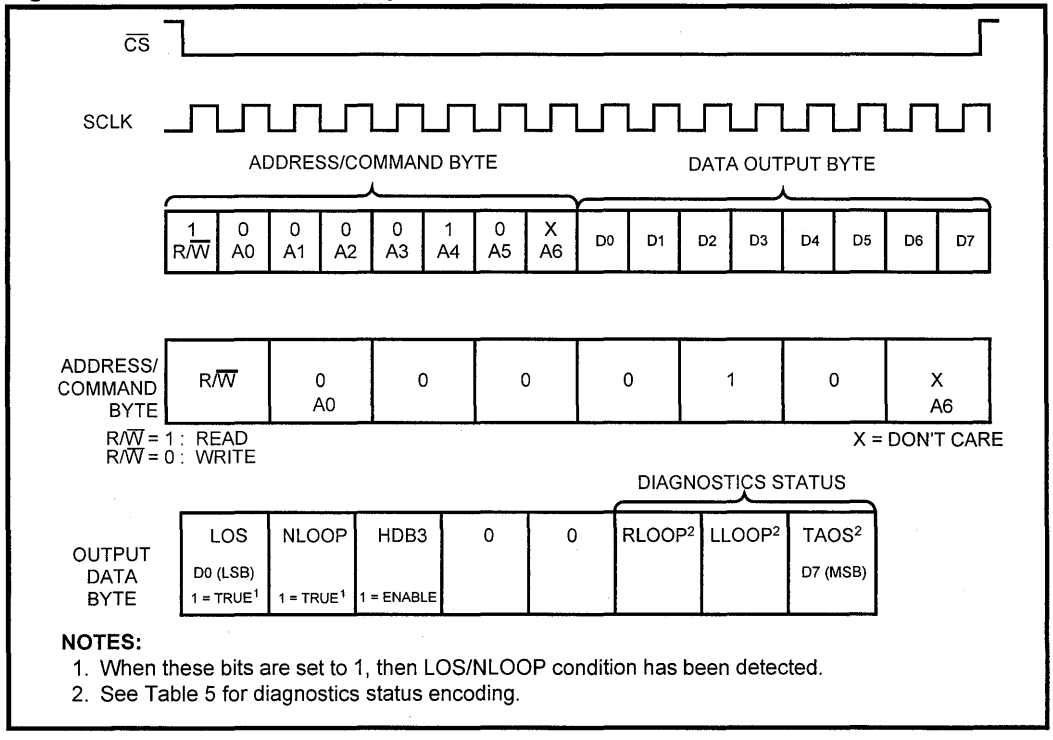


Figure 5: LXT318 Serial I/O Output Data Structure



NOTES:

1. When these bits are set to 1, then LOS/NLOOP condition has been detected.
2. See Table 5 for diagnostics status encoding.

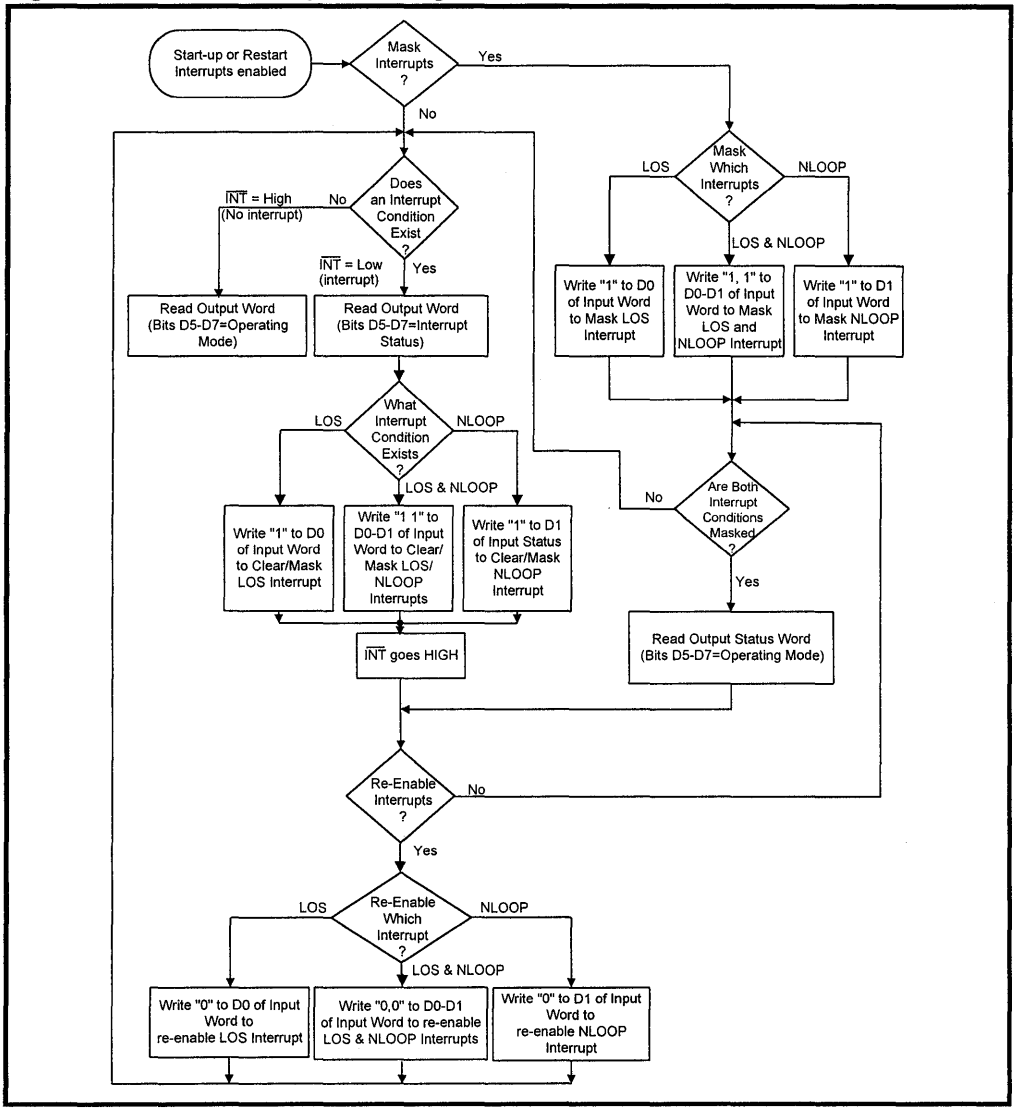
Interrupt Handling

Figure 6 shows how to mask the interrupt generator by writing a one to the respective bit of the input data byte LOS (D0) or NLOOP (D1). Either interrupt pulls the $\overline{INT}$ output pin Low. The output stage of the $\overline{INT}$ pin consists only of a pull-down device which requires an external pull-up resistor for it to function. To clear either interrupt:

1. If either of the interrupt bits LOS (D0) and NLOOP (D1) of the output data byte) is High, writing a one to the respective input bit (D0 or D1, of the input data byte) will clear the interrupt. Leaving a one in this bit position will effectively mask the interrupt. To re-enable the interrupt capability, reset D0 and/or D1 to 0.
2. If either the LOS or the NLOOP bit is Low, resetting the device will clear both interrupts. To reset the chip, set input bits D5 and D6 to one, and D7 to 0.

3

Figure 6: LXT318 Interrupt Handling



Diagnostic Mode Operation

Transmit All Ones. See Figure 7. In Transmit All Ones (TAOS) mode the TPOS and TNEG inputs to the transceiver are ignored and the transceiver transmits a continuous stream of 1s at the TCLK frequency. (In the LXT318 with JASEL set Low and TCLK not provided, TAOS is locked to the MCLK.) This can be used as the Blue Alarm Indicator (AIS). In Host mode, TAOS is commanded by writing a one to bit D7 of the input data byte. In Hardware mode, TAOS is commanded by setting TAOS High. TAOS can be commanded simultaneously with Local Loopback as shown in Figure 7B, but is inhibited during Remote Loopback.

Figure 7: Transmit All Ones

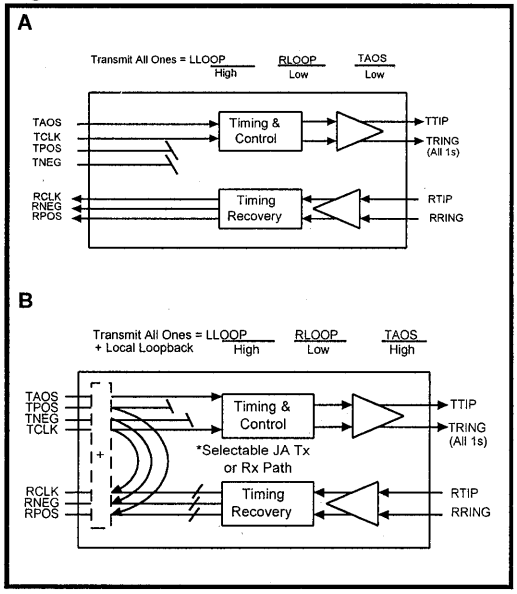
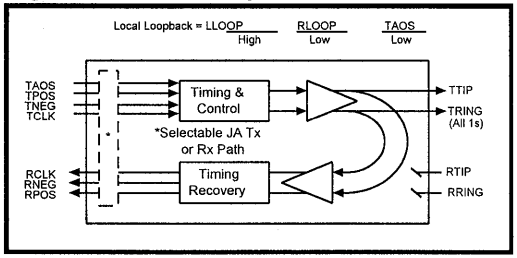


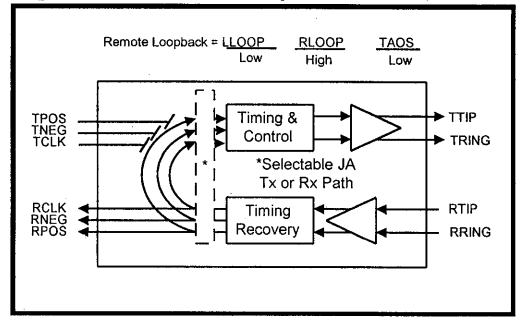
Figure 8: Local Loopback



Local Loopback. See Figure 8. Local Loopback (LLOOP) is designed to exercise the maximum number of functional blocks. During LLOOP operation, the RTIP/RRING inputs from the line are disconnected. Instead, the transmit outputs are routed back into the receive inputs. This tests the encoders/decoders, jitter attenuator, transmitter, receiver and timing recovery sections. In Host mode, writing a one to bit D6 of the input data byte commands Local Loopback In Hardware mode, Local Loopback is commanded by setting LLOOP High. If TAOS and LLOOP are both active, the All Ones pattern is transmitted onto the line while the TPOS/TNEG input data loops back to the RPOS/RNEG outputs through the jitter attenuator.

Remote Loopback. See Figure 9. In Remote Loopback (RLOOP) mode, the transmit data and clock inputs (TCLK and TPOS/TNEG or TDATA) are ignored, and the in-line encoders and decoders are bypassed. The RPOS/RNEG or RDATA outputs are looped back through the transmit circuits and output on TTIP and TRING at the RCLK frequency. Receiver circuits are unaffected by the RLOOP command and continue to output the RCLK and RPOS/RNEG or RDATA signals received from the twisted-pair line. In Host mode, writing a one to bit D5 of the input data byte commands Remote Loopback. In Hardware mode, Remote Loopback is commanded by setting RLOOP High.

Figure 9: Remote Loopback



Network Loopback Detection. In Host mode, to start the Network Loopback detection mode, write a one to each of RLOOP, LLOOP, and TAOS simultaneously and write all 0s in the next cycle. In Hardware mode, hold RLOOP, LLOOP and TAOS High simultaneously for 200 ns, then pull them all Low. Alternatively, tying RLOOP to RCLK will enable NLOOP.

With NLOOP detection enabled, the receiver monitors the input data for the NLOOP enable data pattern (00001). When either pattern repeats for five seconds, the device begins remote loopback operation. The LXT318 responds to either framed or unframed NLOOP patterns. Once the device begins NLOOP operation, the function is identical to remote loopback. When it detects the disable pattern (001) for five seconds or if RLOOP is enabled, the chip resets NLOOP. Activating LLOOP interrupts NLOOP temporarily, but it does not reset NLOOP.

APPLICATION INFORMATION

NOTE

This application information is for design aid only.

LATN DECODING CIRCUITS AND EXTERNAL COMPONENTS

The line attenuation (LATN) output is encoded as a simple serial bit stream for use in line monitoring applications. Figure 10 is a typical decoding circuit for the LATN output. Table 6 provides the decoded output for each equalizer setting. It uses a 2-bit synchronous counter (half of a 4-bit counter) with synchronous reset, and a pair of flip-flops.

Figure 10:Typical LATN Decoding Circuit

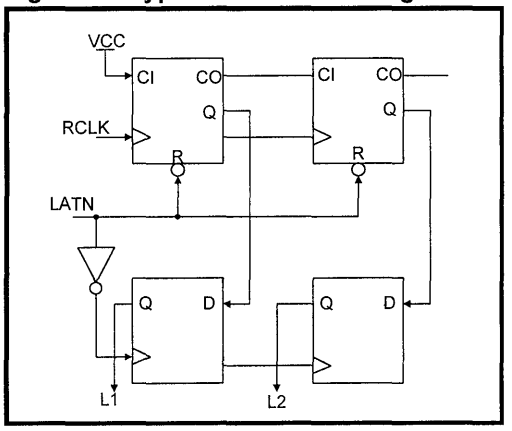


Table 6: Line Attenuation Decoding

L2	L1	Line Attenuation
0	0	0.0 dB
0	1	-9.5 dB
1	0	-19.5 dB
1	1	-28.5 dB

POWER REQUIREMENTS

The LXT318 is a low-power CMOS devices. It operates from a single +5 V power supply which can be connected externally to both the transmitter and receiver. However, the two inputs must be within ±.3V of each other, and decoupled to their respective grounds separately, as shown in Figure 11. Isolation between the transmit and receive circuits is provided internally.

JITTER ATTENUATION CIRCUITRY EXTERNAL CRYSTAL SPECIFICATIONS

Table 7 shows the minimum specifications for the external crystal used by the LXT318 jitter attenuation loop.

Table 7: LXT318 Crystal Specifications
(External)

Parameter	Specification
Frequency	8.192 MHz
Frequency stability	±20 ppm @ 25° C ±25 ppm @ -40° to +85° C (ref 25° C reading)
Pullability (Pull range may be slightly asymmetrical)	C_L = 19 pF to 37 pF, crystal should pull -95 ppm to -115 ppm from nominal frequency C_L = 19 pF to 11.6 pF, crystal should pull +95 ppm to +130 ppm from nominal frequency
Effective series resistance	30 Ω maximum
Crystal cut	AT
Resonance	Parallel
Drive level	2.0 mW maximum
Mode of operation	Fundamental
Crystal holder	HC49 (R3W), C_O = 7 pF maximum C_M = 17 fF typical;

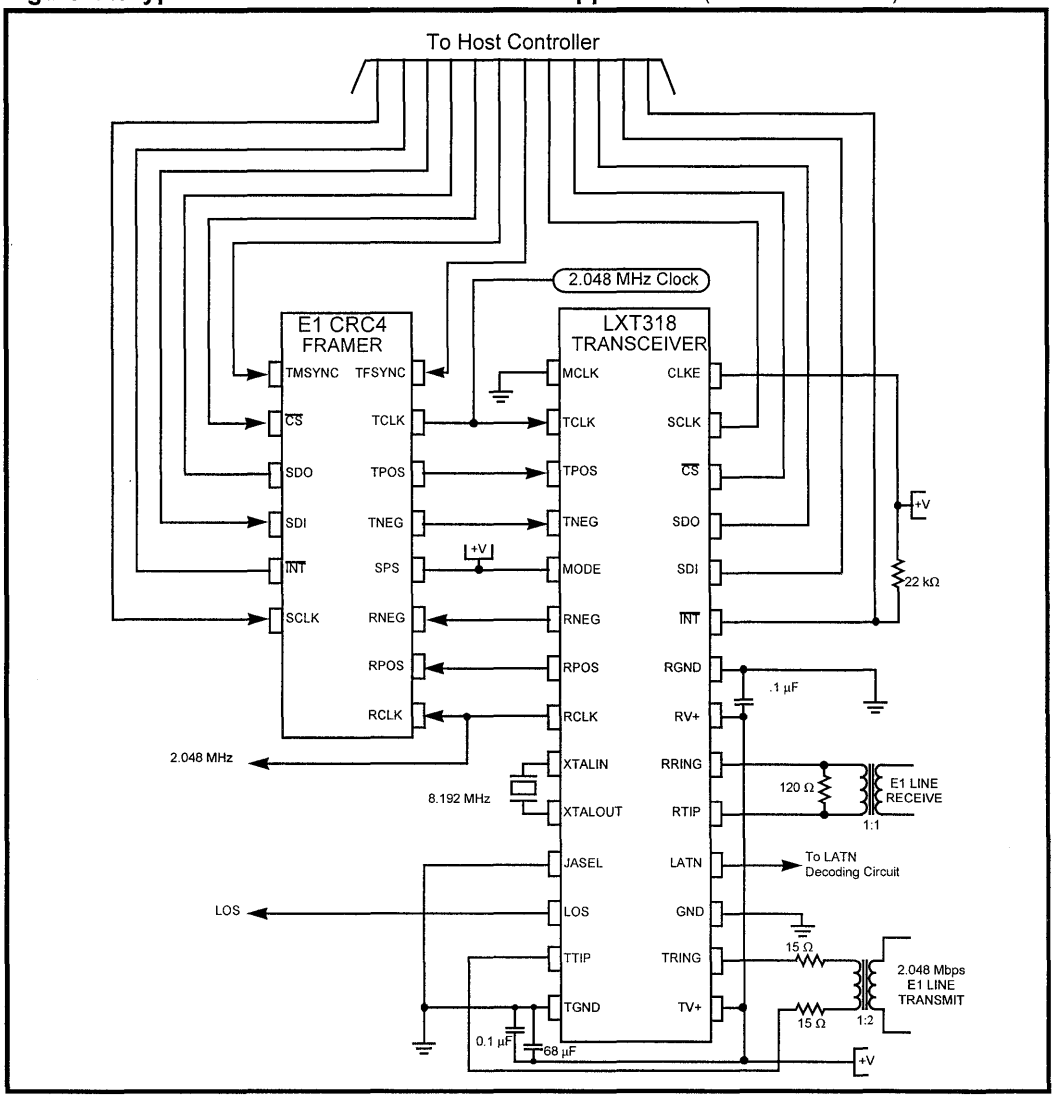
LXT318 Host Mode Applications

Figure 11 shows a typical E1 NTU application with the LXT318 operating in the Host mode (MODE pin tied High). The E1/CRC Framer provides the digital interface with the host controller. Both devices are controlled through the serial interface. In the Host mode, the LOS alarm is reported via the serial port so the LOS pin is not used (although it still reports valid LOS status.)

The 8.192 MHz crystal across XTALIN and XTALOUT enables the JAL which is switched to the transmit side by the ground on JASEL. The power supply inputs are tied to a common bus with appropriate decoupling capacitors (68 mF and 0.1 µF) installed on each side.

The line interfaces are relatively simple. A 120 Ω resistor (for TWP applications) across the input of a 1:1 transformer is used on the receive side, and a pair of 15 Ω resistors are installed in series with the 1:2 transmit transformer.

Figure 11:Typical LXT318 Host Mode E1/NTU Application (120 Ω Twisted Pair)



LXT318 Hardware Mode Applications

Figure 12 shows a typical 2.048 Mbps application with the LXT318 operating in the Hardware mode. This configuration is illustrated with a single power supply bus. CMOS control logic is used to set the TAOS, LLOOP and RLOOP diagnostic modes individually. The RCLK output is tapped to clock the MODE pin, enabling HDB3 encoding. The receive and transmit line interfaces are identical to the Host mode application shown in Figure 11.

Figure 12:Typical LXT318 Hardware Mode Application (120 Ω Twisted Pair)

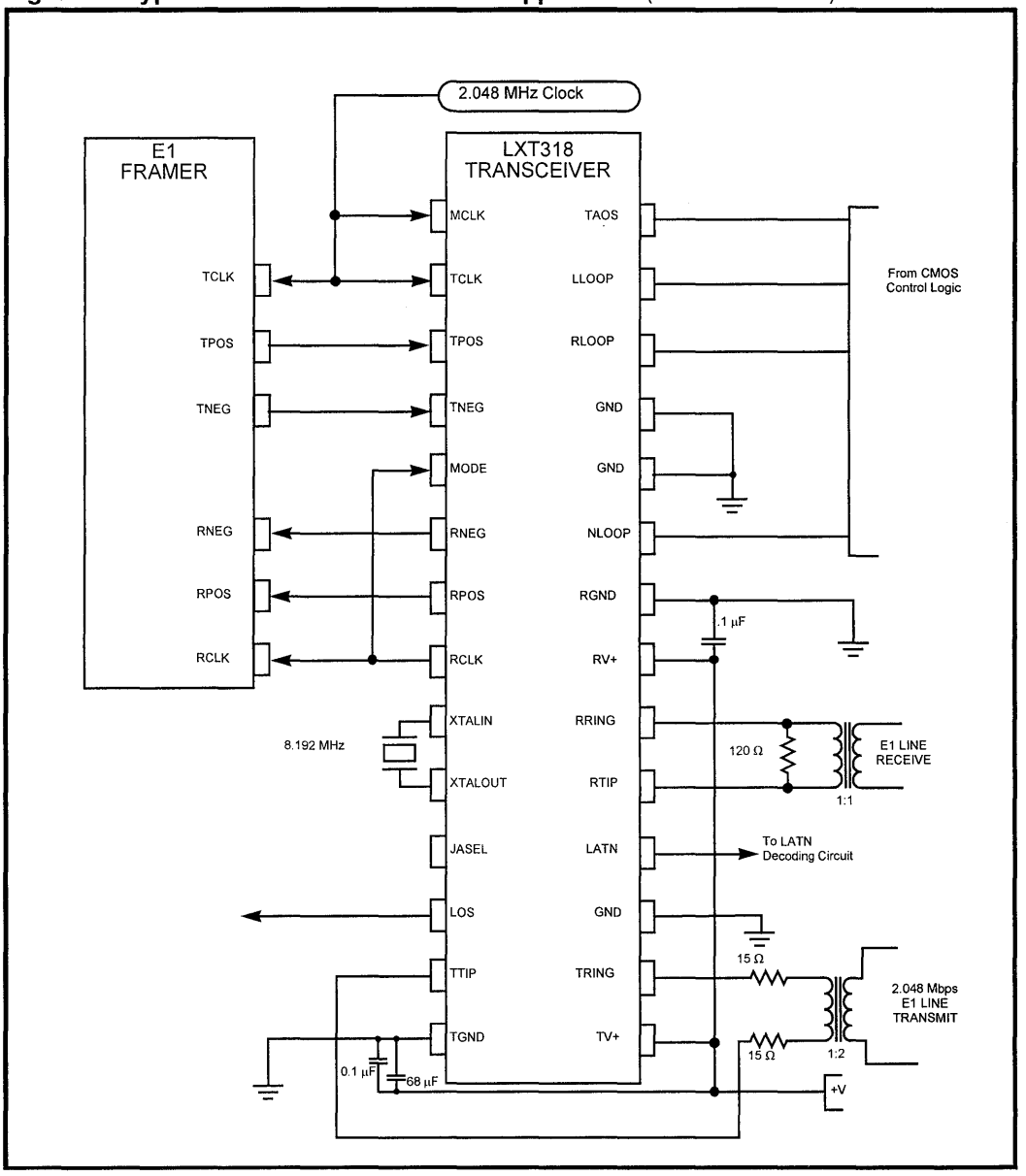
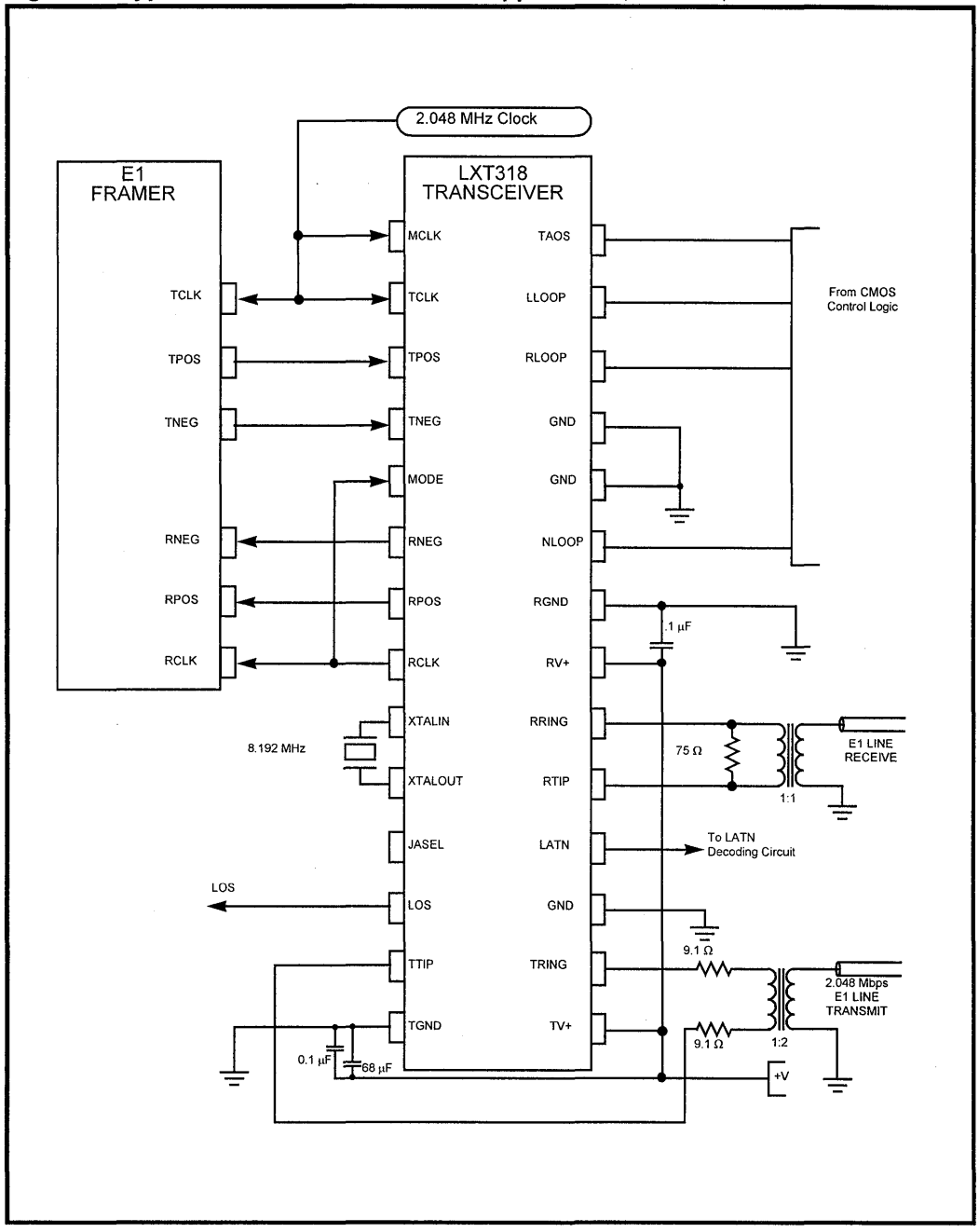


Figure 13:Typical LXT318 Hardware Mode Application (75 Ω Coax)



TEST SPECIFICATIONS

NOTE

The minimum and maximum values in Tables 8 through 14 and Figures 18 through 22 represent the performance specifications of the LXT318 and are guaranteed by test , except where noted by design.

Table 8: Absolute Maximum Ratings

Parameters	Symbol	Min	Max	Units
DC supply (referenced to GND)	RV+, TV+	–	6.0	V
Input voltage, any pin	VIN	RGND, -0.3	RV+, +0.3	V
Input current, any pin [1]	IIN	-10	10	mA
Storage temperature	TSTG	-65	150	° C

CAUTION

Operation at or beyond these limits may permanently damage the device. Normal operation not guaranteed at these extremes.

1. Transient Currents of up to 100 mA will not cause SCR latch-up. TTIP TRING, TV+, TGND can withstand continuous current of 100 mA.

Table 9: Operating Conditions and Characteristics

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
DC supply[2]	RV+, TV+	4.75	5.0	5.25	V	
Ambient operating temperature	TA	-40	-	+85	°C	
Power dissipation[3]	PD	-	300	400	mW	100% ones density & maximum line length @ 5.25 V

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. TV+ must not differ from RV+ by more than 0.3 V.
3. Power dissipation while driving 25 Ω load over operating temperature range. Includes device and load. Digital input levels are within 10% of the supply rails and digital outputs are driving a 50 pF capacitive load.

Table 10: Digital Characteristics (TA = -40 to 85 °C, V+ = 5.0 V ±5%, GND = 0 V)

Parameter	Sym	Min	Typ	Max	Units	Test Conditions
High level input voltage[1,2] (pins 1-5, 10, 23-28)	VIH	2.0	–	–	V	
Low level input voltage[1,2] (pins 1-5, 10, 23-28)	VIL	–	–	0.8	V	
High level input voltage[1,2] (pins 6-8, 12, 23, 25)	VOH	2.4	–	–	V	IOUT = -400 µA
Low level input voltage[1,2] (pins 6-8, 12, 23, 25)	VOL	–	–	0.4	V	IOUT = 1.6 mA
Input leakage current	ILL	0	–	±10	µA	
Three-state leakage current[1] (pin 25)	I3L	0	–	±10	µA	
Driver power down current[3]	IPD	–	–	±1.2	mA	Direct connection to Vcc or GND

1. Functionality of pins 23 and 25 depends on mode. See Host/Hardware Mode descriptions.
2. Output drivers will output CMOS logic levels into CMOS loads.
3. TTIP, TRING only in Idle or Power Down Mode.

Table 11: Analog Characteristics (T_A = -40 to 85 °C, V+ = 5.0 V ±5%, GND = 0 V)

Parameter		Min	Typ[1]	Max	Units	Test Conditions
Recommended output load at TTIP and TRING		50	120	200	Ω	
AMI output pulse amplitudes		2.7	3.0	3.3	V	Measured at the output
Jitter added by the transmitter[2]	20 Hz - 100kHz[3]	–	–	0.05	UI	
Input jitter tolerance	20 Hz - 100kHz	0.2	0.3	–	UI	0 - 43 dB line
	10 Hz	100	500	–	UI	
Jitter attenuation curve corner frequency[4]		–	3	–	Hz	
Receive signal attenuation range		0	43	–	dB	
Allowable consecutive zeros before LOS		160	175	190	–	
Transmitter return loss[3]	51 kHz - 102 kHz	–	18	–	dB	
	102 kHz - 2.048 MHz	–	24	–	dB	
	2.048 MHz - 3.072 MHz	–	22	–	dB	
Receiver return loss[3, 5]	51 kHz - 102 kHz	–	20	–	dB	
	102 kHz - 2.048 MHz	–	24	–	dB	
	2.048 MHz - 3.072 MHz	–	22	–	dB	

1. Typical figures are at 25 °C and are for design aid only, not guaranteed and not subject to production testing.
2. Input signal to TCLK is jitter free.
3. Guaranteed by characterization; not subject to production testing.
4. Circuit attenuates jitter at 20 dB/decade above the corner frequency.
5. Measured with 1:1 transformer terminated with 120 Ω resistance.

Table 12: LXT318 Master Clock and Transmit Timing Characteristics (See Figure 14)

Parameter	Sym	Min	Typ[1]	Max	Units	Notes
Master clock frequency	MCLK	–	2.048	–	MHz	
Master clock tolerance	MCLKt	–	±100	–	ppm	
Master clock duty cycle	MCLKd	40	–	60	%	
Crystal frequency	fc	–	8.192	–	MHz	
Transmit clock frequency	TCLK	–	2.048	–	MHz	
Transmit clock tolerance	TCLKt	–	–	±100	ppm	
Transmit clock duty cycle	TCLKd	10	–	90	%	
TPOS/TNEG to TCLK setup time	tSUT	50	–	–	ns	
TCLK to TPOS/TNEG hold time	tHT	50	–	–	ns	

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 14:LXT318 Transmit Clock Timing

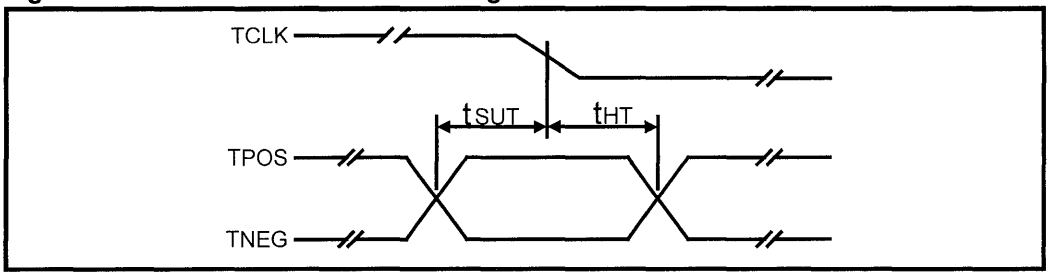


Figure 15: LXT318 Receive Clock Timing

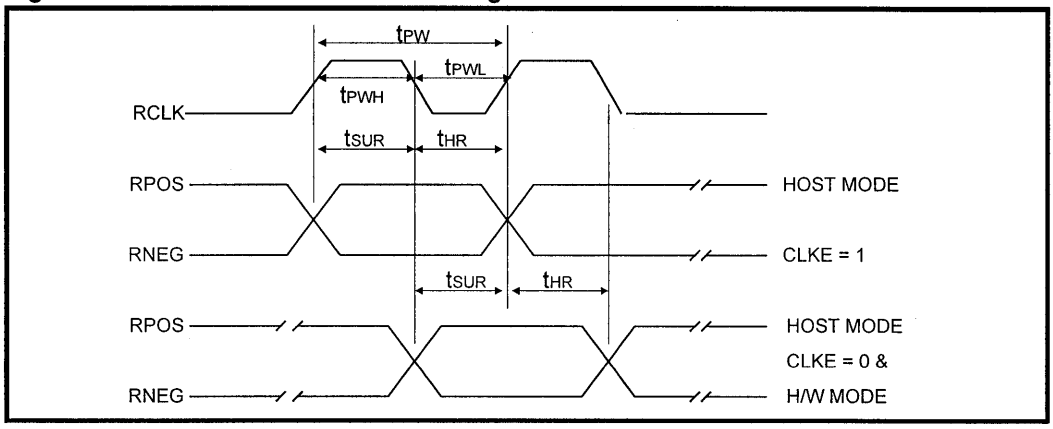


Table 13: LXT318 Receive Timing Characteristics (See Figure 15)

Parameter	Sym	Min	Typ[1]	Max	Units	Notes
Receive clock duty cycle[2]	RCLKd	40	50	60	%	
Receive clock pulse width[2]	tPW	-	488	-	ns	
Receive clock pulse width High	tPWH	-	244	-	ns	
Receive clock pulse width Low	tPWL	220	244	268	ns	
RPOS/RNEG to RCLK rising setup time	tSUR	-	194	-	ns	
RCLK rising to RPOS/RNEG hold time	tHR	-	194	-	ns	

1. Typical figures are at 25° C and are for design aid only; not guaranteed and not subject to production testing.
2. RCLK duty cycle widths will vary depending on extent of received pulse jitter displacement. Max and min RCLK duty cycles are for worst case jitter conditions (0.4 UI clock displacement for 2.048 Mbps.)

Table 14: LXT318 Serial I/O Timing Characteristics (See Figures 16 and 17)

Parameter	Sym	Min	Typ[1]	Max	Units	Parameter
Rise/fall time—any digital output	tRF	–	–	100	ns	Load 1.6 mA, 50 pF
SDI to SCLK setup time	tDC	50	–	–	ns	
SCLK to SDI hold time	tCDH	50	–	–	ns	
SCLK low time	tCL	240	–	–	ns	
SCLK high time	tCH	240	–	–	ns	
SCLK rise and fall time	tR, tF	–	–	50	ns	
$\overline{CS}$ falling edge to SCLK rising edge	tCC	50	–	–	ns	
Last SCLK edge to $\overline{CS}$ rising edge	tCCH	150	–	–	ns	
$\overline{CS}$ inactive time	tCWH	250	–	–	ns	
SCLK to SDO valid time	tCDV	–	–	200	ns	
SCLK falling edge or $\overline{CS}$ rising edge to SDO high-Z	tCDZ	–	100	–	ns	

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 16: LXT318 Serial Data Input Timing Diagram

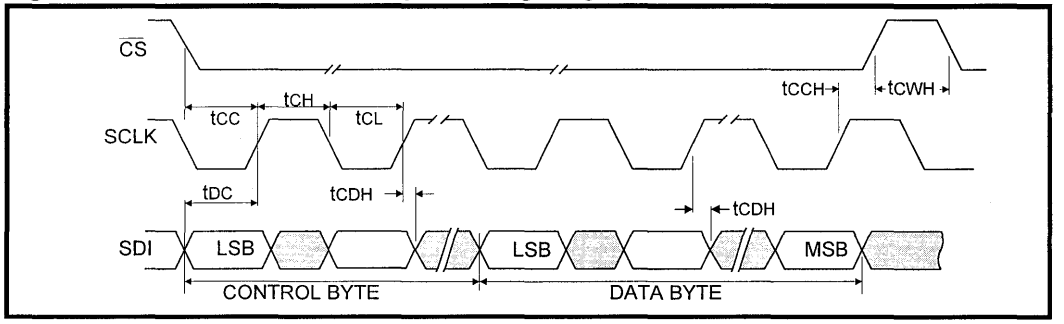


Figure 17: LXT318 Serial Data Output Timing Diagram

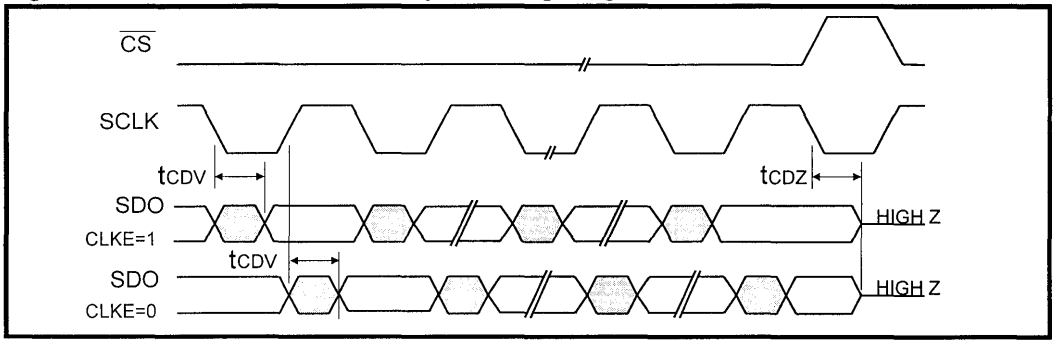


Figure 18: LXT318 Jitter Tolerance @ 43 dB (Typical)

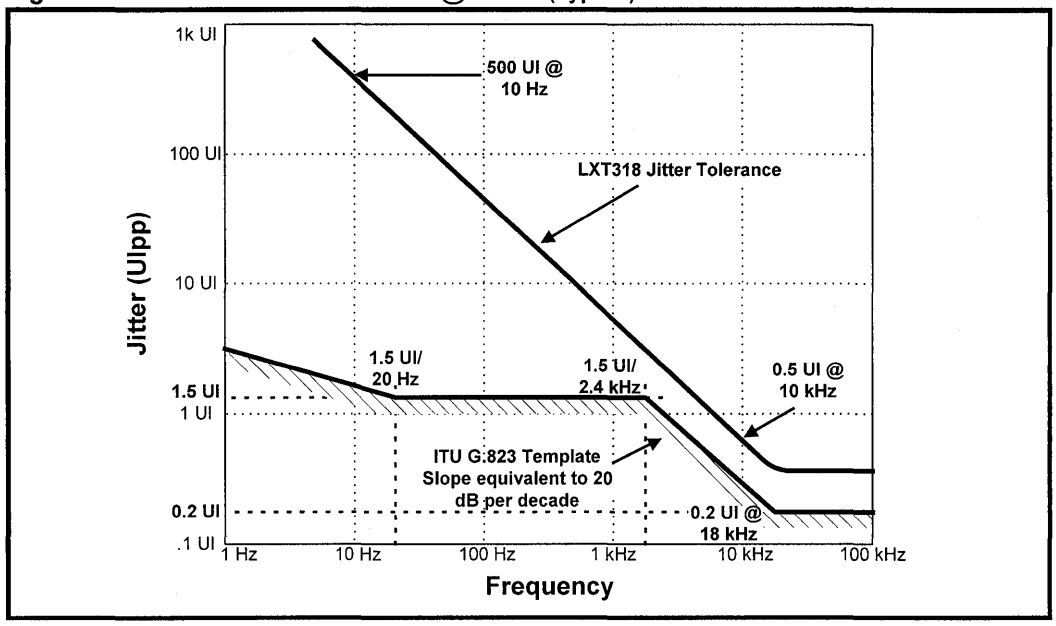


Figure 19: LXT318 Jitter Attenuation (Typical)

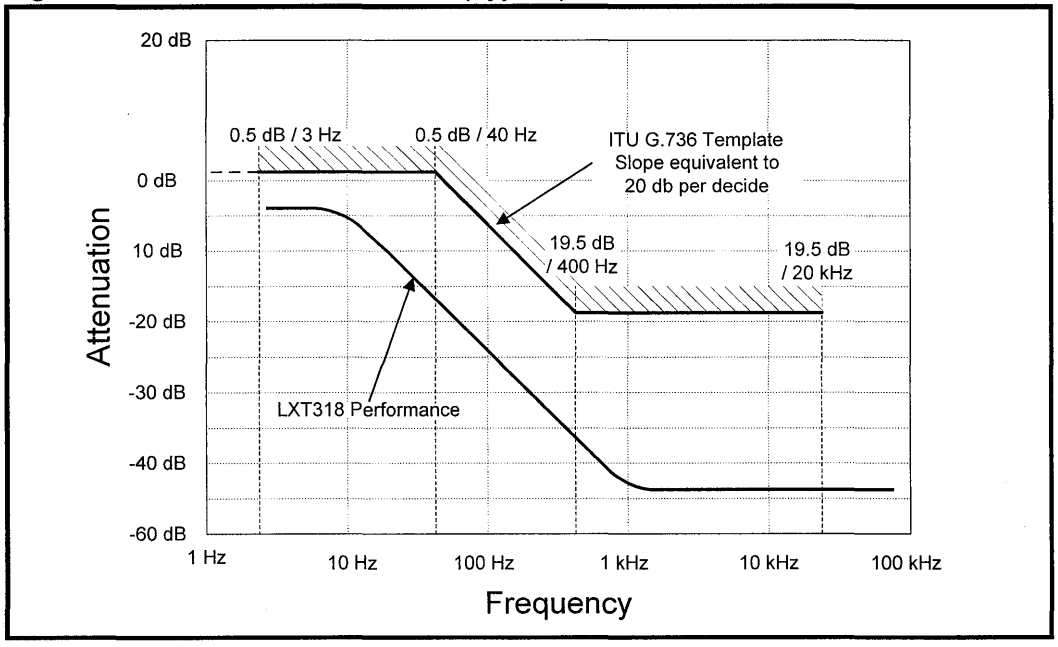


Figure 20: Input and Maximum Output Jitter Specified by TBR12/13

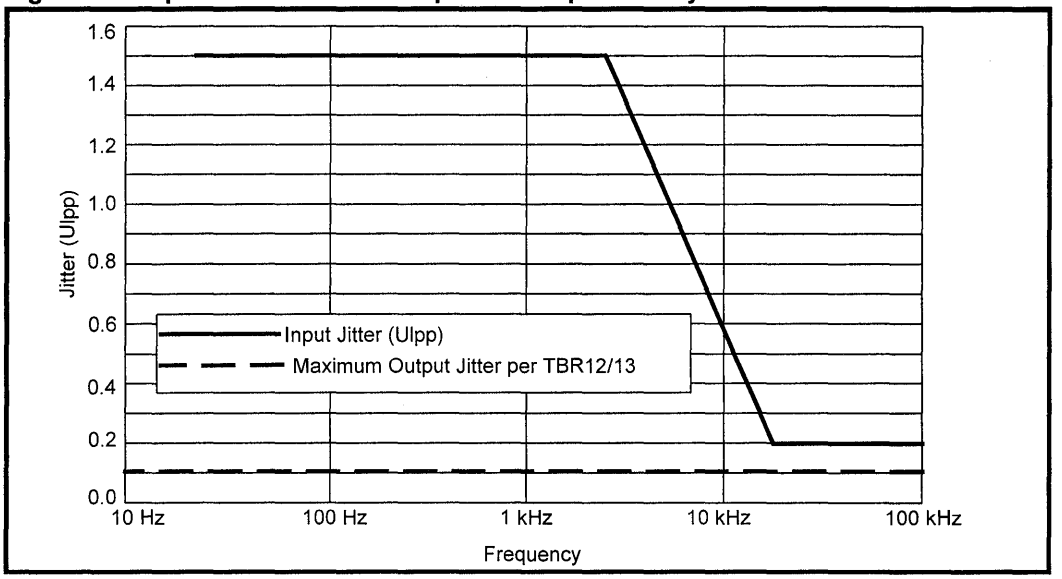


Figure 21: LXT318 Jitter Attenuation Performance (Typical–Measured Against TBR12/13)

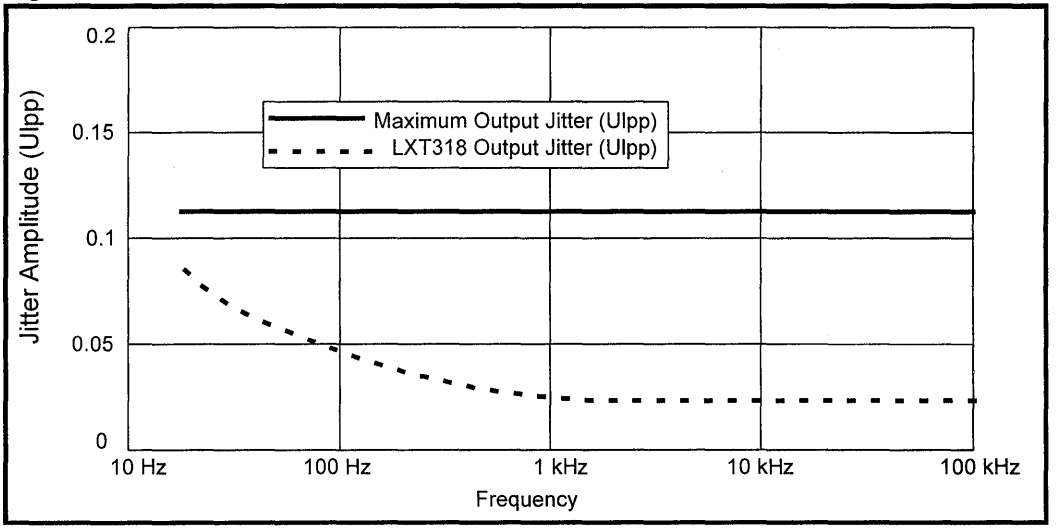


Figure 22: 2.048 Mbps Pulse Mask

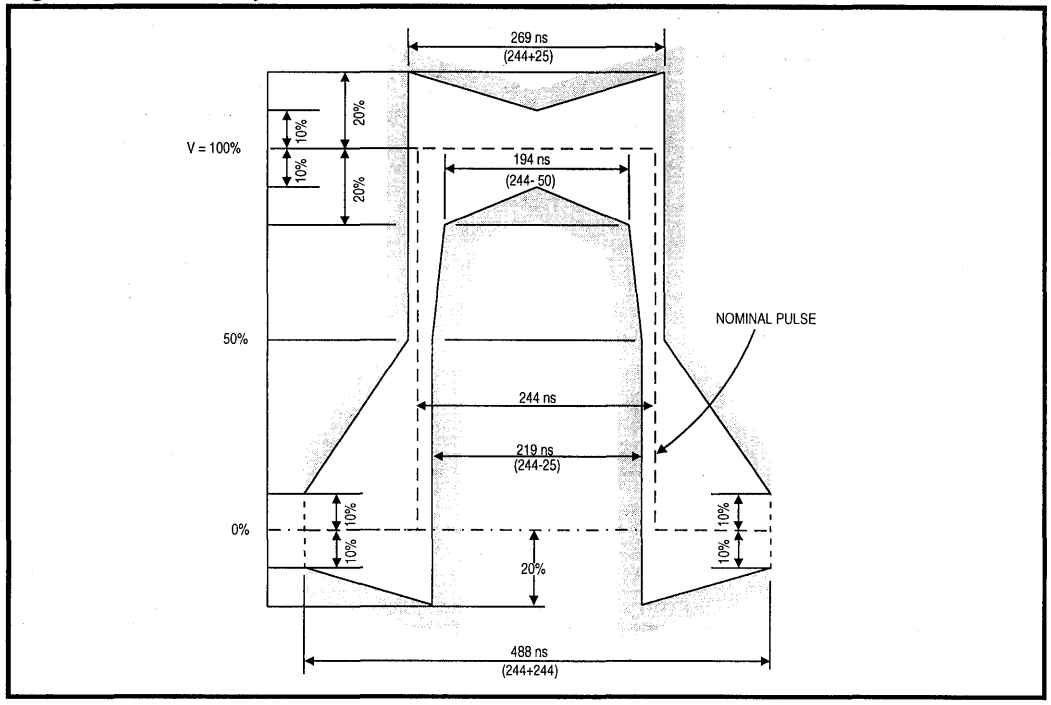


Table 15: 2.048 Mbps Pulse Mask Parameters

Parameter	TPW	Units
Test load impedance	120	Ω
Nominal peak mark voltage	3.0	V
Nominal peak space voltage	0 ± 0.30	V
Nominal pulse width	244	ns
Ratio of positive and negative pulse amplitude at center of pulse	95-105	%
Ratio of positive and negative pulse amplitudes at nominal half amplitude	95-105	%

LXT360/361 Integrated T1/E1 LH/SH Transceivers for DS1/DSX-1/CSU or NTU/ISDN PRI Applications

General Description

The LXT360 and LXT361 are the first full-featured, fully integrated, combination transceivers for E1 ISDN Primary Rate Interface and T1 long- and short-haul applications. They operate over 0.63 mm (22 AWG) twisted-pair cables for 0 to 2 km (6 kft) and offer Line Build-Outs and pulse equalization settings for all T1 and E1 Line Interface Unit (LIU) applications.

The LXT360 and LXT361 are identical except for their control options. The LXT361 offers an Intel or Motorola compatible parallel port for microprocessor control. The LXT360 provides both a serial port for microprocessor control and a hardware control mode for stand alone operation. Both incorporate advanced crystal-less digital jitter attenuation in either the transmit or receive data path starting at 3 Hz. B8ZS/HDB3 encoding/decoding and unipolar or bipolar data I/O are available. Both LIUs provide loss of signal monitoring and a variety of diagnostic loopback modes.

The LXT360/361 uses an advanced double-poly, double-metal fabrication process and requires only a single 5-volt power supply.

Applications

- ISDN Primary Rate Interface (ISDN PRI)
- CSU/NTU interface to T1/E1 Service
- Wireless Base Station interface
- T1/E1 LAN/WAN bridge/routers
- T1/E1 Mux; Channel Banks
- Digital Loop Carrier - Subscriber Carrier Systems

Features

- Fully integrated transceivers for Long- or Short-Haul T1 or E1 interfaces
- Crystal-less digital jitter attenuation
  - Select either transmit or receive path
  - No crystal or high speed external clock required
- Meet or exceed specifications in ANSI T1.403 and T1.408; ITU I.431, G.703, G.736, G.775 and G.823; ETSI 300-166 and 300-233; and AT&T Pub 62411
- Support 75 Ω (E1 coax), 100 Ω (T1 twisted-pair) and 120 Ω (E1 twisted-pair) applications
- Selectable receiver sensitivity – Fully restores the received signal after transmission through a cable with attenuation of either 0 to 26 dB, or 0 to 36 dB @ 772 kHz and 0 to 43 dB @ 1024 kHz
- Five Pulse Equalization Settings for T1 short-haul applications
- Four Line Build-Outs for T1 long-haul applications from 0 dB to -22.5 dB
- Transmit/receive performance monitors with Driver Fail Monitor Open and Loss of Signal outputs
- Selectable unipolar or bipolar data I/O and B8ZS/HDB3 encoding/decoding
- Line attenuation indication output in 2.9 dB steps
- QRSS generator/detector for testing or monitoring
- Output short circuit current limit protection
- Local, remote, analog and inband network loopback generation and detection
- Multiple-register serial- or parallel-interface for microprocessor control
- Available in 28-pin DIP, 28-pin PLCC, and 44-pin PQFP packages

LXT360 Block Diagram

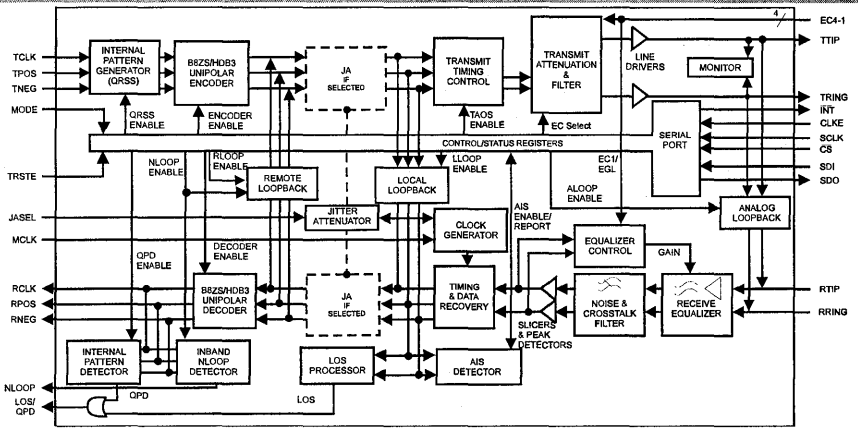


Figure 1: LXT360 Hardware Controlled Bipolar Mode Pin Assignments

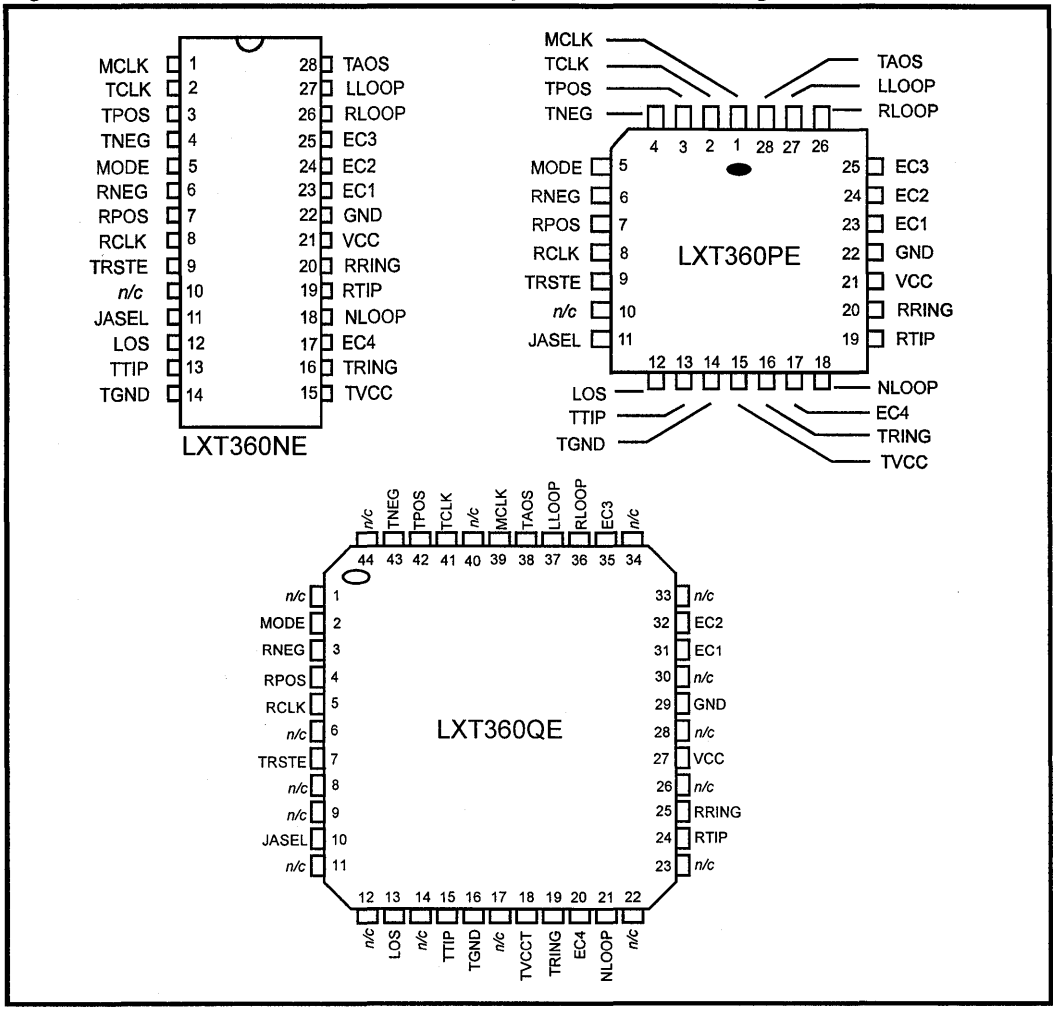


Table 1: LXT360 Clock and Data Pin Assignments by Mode[1]

Pin # DIP/ PLCC	Pin # QEP	External Data Modes		QRSS Modes	
		Bipolar Mode	Unipolar Mode	Bipolar Mode	Unipolar Mode
1	39	MCLK			
2	41	TCLK			
3	42	TPOS	TDATA	INSLER	
4	43	TNEG	INSBPV	INSBPV	
6	3	RNEG	BPV	RNEG	BPV

1. Data pins change based on whether external data or internal QRSS mode is active. Clock pins remain the same in both Hardware and Host Modes.

Table 1: LXT360 Clock and Data Pin Assignments by Mode[1]– *continued*

Pin # DIP/ PLCC	Pin # QEP	External Data Modes		QRSS Modes	
		Bipolar Mode	Unipolar Mode	Bipolar Mode	Unipolar Mode
7	4	RPOS	RDATA	RPOS	RDATA
8	5	RCLK			
13	15	TTIP			
14	16	TGND			
15	18	TVCC			
16	19	TRING			
19	24	RTIP			
20	26	RRING			
21	27	VCC			
22	29	GND			

1. Data pins change based on whether external data or internal QRSS mode is active. Clock pins remain the same in both Hardware and Host Modes.

Table 2: LXT360 Control Pins by Mode

Pin # DIP/ PLCC	Pin # QFP	Hardware Modes		Host Modes		Pin # DIP/ PLCC	Pin # QFP	Hardware Modes		Host Modes	
		Unipolar/ Bipolar	QRSS	Unipolar/ Bipolar	QRSS			Unipolar/ Bipolar	QRSS	Unipolar/ Bipolar	QRSS
5	2	MODE		MODE		25	35	EC3		SDO	
9	7	TRSTE		TRSTE		17	20	EC4		*Low*	
11	10	JASEL		*Low*		18	21	NLOOP		NLOOP	
12	13	LOS	LOS/ QPD	LOS	LOS/ QPD	26	36	RLOOP		$\overline{CS}$	
23	31	EC1		$\overline{INT}$		27	37	LLOOP		SCLK	
24	32	EC2		SDI		28	38	TAOS	QRSS	CLKE	

Table 3: LXT360 Hardware Controlled Bipolar Mode Signal Descriptions

Pin # DIP/ PLCC	Pin # QFP[4]	Symbol	I/O[2]	Description
1[1]	39[1]	MCLK	DI	**Master Clock**. Connect to 1.544 MHz for T1 operation; to 2.048 MHz for E1. MCLK input requires an external, independent clock signal to generate internal clocks. Required accuracy is better than ± **32 ppm** with a typical duty cycle of 50%. Upon Loss of Signal (LOS), RCLK is derived from MCLK.
2[1]	41[1]	TCLK	DI	**Transmit Clock**. 1.544 MHz or 2.048 MHz clock input. Transceiver samples TPOS and TNEG on the falling edge of TCLK
3 4	42 43	TPOS TNEG	DI	**Transmit Data – Positive and Negative**. In the Bipolar I/O mode, these pins are the positive and negative sides of a bipolar input pair. Data to be transmitted onto the twisted-pair line is input at these pins. Table 4 describes Unipolar Mode functions.
5[1]	2	MODE	DI	**Mode Select**. Connecting MODE Low puts the LXT360 in the Hardware Mode. In Hardware Mode, the serial interface is disabled and hardwired pins are used to control configuration and report status. Connecting MODE to Midrange[3] activates the Hardware Mode and enables the B8ZS/HDB3 encoder/decoder and Unipolar Mode. Connecting MODE High puts the LXT360 in the Host Mode. In the Host Mode, the serial interface controls the LXT360 and displays its status.
6 7	3 4	RNEG RPOS	DO	**Receive Data – Negative and Positive**. In the Bipolar I/O mode, these pins are the positive and negative sides of a bipolar output pair. Data recovered from the line interface is output on these pins. A signal on RNEG corresponds to receipt of a negative pulse on RTIP/RRING. A signal on RPOS corresponds to receipt of a positive pulse on RTIP/RRING. RNEG/RPOS outputs are Non-Return-to-Zero. Both outputs are stable and valid on the rising edge of RCLK. Refer to Table 4 for Unipolar Mode function descriptions.
8	15	RCLK	DO	**Recovered Clock**. The clock recovered from the line input signal is output on this pin. Under LOS conditions there is a smooth transition from RCLK signal (derived from the recovered data) to MCLK signal at the RCLK output.
9	7	TRSTE	DI	**Tristate**. Connecting **TRSTE** High forces all output pins to a high impedance state. Connecting TRSTE Low sets LXT360 to the Hardware Bipolar Mode. Connecting TRSTE to Midrange[3] enables the Unipolar Mode. (See Table 4 for Unipolar function descriptions.)
10	–	*n/c*	–	*No connection. Leave this pin floating.*

1. These pins do not change function as the operating mode changes. Tables 4 through 6 do not describe these pins.
2. I/O column entries: DI = Digital Input; DO = Digital Output; DI/O = Digital Input/Output; AI = Analog Input; AO = Analog Output.
3. Midrange is a voltage level such that 2.3 V ≤ Midrange ≤ 2.7 V or the pin may float.
4. Pins 1, 6, 8, 11, 12, 14, 17, 22, 23, 26, 28, 30, 33, 34, 40, and 44 are not connected (*n/c*).

Table 3: LXT360 Hardware Controlled Bipolar Mode Signal Descriptions – *continued*

Pin # DIP/ PLCC	Pin # QFP[4]	Symbol	I/O[2]	Description
11	10	JASEL	DI	**Jitter Attenuation Select**. Selects jitter attenuation location. Connecting JASEL High activates the jitter attenuator in the receive path. Connecting JASEL Low activates the jitter attenuator in the transmit path. Connecting JASEL to Midrange[3] disables JA.
12	13	LOS	DO	**Loss of Signal Indicator**. In T1 modes, LOS goes High on receipt of 175 consecutive spaces and returns Low when the received signal reaches a mark density of 12.5% (determined by receipt of 16 marks within a sliding window of 128 bits with fewer than 100 consecutive zeros). In E1 modes, LOS goes High on receipt of 32 consecutive spaces, and returns Low when the receiver detects 12.5% mark density (determined by receipt of 4 marks within a sliding window of 32 bits with fewer than 16 consecutive zeros). The transceiver outputs received marks on RPOS and RNEG even when LOS is High.
13[1] 16[1]	15[1] 19[1]	TTIP TRING	AO	**Transmit Tip and Ring**. Differential Driver Outputs. These outputs are designed to drive a 50 - 200 Ω load. The transformer and line matching resistors should be selected to give the desired pulse height and return loss performance.
14[1]	16[1]	TGND		**Ground** return for the transmit drivers power supply TVCC.
15[1]	18[1]	TVCC	DI	**+5 VDC Power Supply** input for the transmit drivers. TVCC must not vary from VCC by more than ± 0.3 V.
17	20	EC4	DI	**Equalization Control 4**. Used with EC3-1 (pins 23-25) for **pulse equalization** and LBO settings.
18[1]	21[1]	NLOOP	DO	**Network Loopback Detection**. If the LXT360 is configured to detect Network Loopback (NLOOP) (by connecting the RLOOP pin to Midrange[3]), this pin goes High when an Inband Network Loopback has been activated by the reception of a 00001 pattern for five seconds. NLOOP is reset by reception of 001 for five seconds, or by activation of RLOOP.
19[1] 20[1]	24[1] 25[1]	RTIP RRING	AI	**Receive Tip and Ring**. The AMI signal received from the line is applied at these pins. A 1:1 transformer is required. Data and clock from the signal applied at these pins are recovered and output on the RPOS/RNEG, and RCLK pins.
21[1]	27[1]	VCC		**+5 VDC Power Supply** for all circuits except the transmit drivers. (Transmit drivers are supplied by TVCC.)
22[1]	29[1]	GND		**Ground** return for power supply VCC.

1. These pins do not change function as the operating mode changes. Tables 4 through 6 do not describe these pins.
2. I/O column entries: DI = Digital Input; DO = Digital Output; DI/O = Digital Input/Output; AI = Analog Input; AO = Analog Output.
3. Midrange is a voltage level such that 2.3 V ≤ Midrange ≤ 2.7 V or the pin may float.
4. Pins 1, 6, 8, 11, 12, 14, 17, 22, 23, 26, 28, 30, 33, 34, 40, and 44 are not connected (*n/c*).

Table 3: LXT360 Hardware Controlled Bipolar Mode Signal Descriptions – *continued*

Pin # DIP/ PLCC	Pin # QFP[4]	Symbol	I/O[2]	Description
23 24 25	31 32 35	EC1 EC2 EC3	DI	**Equalization Control 3-1**. EC4-1 (including pin 17) define the **Pulse Equalization, Line Build Outs** and **Equalizer Gain Limit** settings. See Table 12 for additional details.
26	36	RLOOP	DI	**Remote Loopback.** When held High, the clock and data inputs from the framer (TPOS/TNEG or TDATA) are ignored and the data received from the twisted-pair line is transmitted back onto the line at the RCLK frequency. During remote loopback, the device ignores the in-line encoders/decoders. Connecting this pin to Midrange enables Network Loopback. See Figure 8.
27	37	LLOOP	DI	**Local Loopback**. When held High, the data on TPOS and TNEG loops back digitally to RPOS and RNEG outputs (through JA if enabled). Connecting this pin to Midrange[3] enables Analog Loopback (TTIP and TRING looped back to RTIP and RRING). See Figures 5, 6, and 7.
28	38	TAOS	DI	**Transmit All Ones**. When held High the transmit data inputs are ignored and the LXT360/361 transmits a stream of 1s at the TCLK frequency. (If TCLK is not supplied, MCLK is the transmit clock reference.) TAOS is inhibited during Remote Loopback. Connecting this pin to Midrange enables QRSS pattern generation and detection. See Figure 5, 10, and 11.

1. These pins do not change function as the operating mode changes. Tables 4 through 6 do not describe these pins.
2. I/O column entries: DI = Digital Input; DO = Digital Output; DI/O = Digital Input/Output; AI = Analog Input; AO = Analog Output.
3. Midrange is a voltage level such that 2.3 V ≤ Midrange ≤ 2.7 V or the pin may float.
4. Pins 1, 6, 8, 11, 12, 14, 17, 22, 23, 26, 28, 30, 33, 34, 40, and 44 are not connected (*n/c*).

Table 4: LXT360 Hardware Controlled Unipolar Mode Signal Assignments

Pin # DIP/ PLCC	Pin# QFP	Symbol	I/O[1]	Description
3	42	TDATA	DI	**Transmit Data**. Unipolar input for data to be transmitted onto the twisted-pair line.
4	43	INSBPV	DI	**Insert Bipolar Violation**. This pin is sampled on the falling edge of TCLK to control Bipolar Violation Insertions in the transmit data stream. A Low-to-High transition is required to insert subsequent BPVs.
6	3	BPV	DO	**Bipolar Violation.** BPV goes High to report receipt of a bipolar violation from the line. This is an NRZ output, valid on the rising edge of RCLK.
7	4	RDATA	DO	**Receive Data**. RDATA is a unipolar NRZ output of data recovered from the line interface. In Hardware Mode RDATA is stable and valid on the rising edge of RCLK.

1. I/O column entries: DI = Digital Input; DO = Digital Output; DI/O = Digital Input/Output; AI = Analog Input; AO = Analog Output.

Table 5: LXT360 Hardware Controlled QRSS Unipolar Mode Signal Assignments

Pin # DIP/ PLCC	Pin # QFP	Symbol	I/O[1]	Description
3	42	INSLER	DI	**Insert Logic Error**. When this pin goes from Low to High, the transceiver inserts a logic error into the transmitted QRSS data pattern. The error follows the data flow in whatever loopback mode is in effect. The LXT360 samples this pin on the falling edge of TCLK (or MCLK, if TCLK is not present).
4	43	INSBPV	DI	**Insert Bipolar Violation**. When this pin goes from Low to High, the transceiver inserts a bipolar violation error into the transmitted QRSS data pattern. A subsequent insertion requires another Low to High transition. The LXT360 samples this pin on the falling edge of TCLK (or MCLK, if TCLK is not present).
6	3	BPV[3]	DO	**Bipolar Violation**. BPV goes High to report receipt of a bipolar violation from the twisted-pair line. This is an NRZ output, valid on the rising edge of RCLK.
7	4	RDATA[3]	AO	**Received Data**. RDATA is a unipolar NRZ output of data recovered from the line interface. In hardware Mode, RDATA is stable and valid on the rising edge of RCLK.
12	13	LOS/ QPD	DO	**Loss of Signal/QRSS Pattern Detect**. This pin acts as a QPD indicator as well as LOS indicator. The QRSS Pattern synchronization criterion is fewer than four errors in 128 bits. In this mode, as long as the transceiver does not detect a QRSS pattern QPD stays High. As soon as the device does detect a QRSS pattern, the pin goes Low; any bit errors cause QPD to go High for half a clock cycle. This output can trigger an external error counter. An LOS condition will also make this pin go High. See Figure 11.
28	38	QRSS	DI	**QRSS**. Setting this pin to Midrange[2], enables QRSS pattern generation and detection. The transceiver transmits the QRSS pattern at the TCLK rate (or MCLK, if TCLK is not present).

1. I/O column entries: DI = Digital Input; DO = Digital Output; DI/O = Digital Input/Output; AI = Analog Input; AO = Analog Output.
2. Midrange is a voltage level such that 2.3 V ≤ Midrange ≤ 2.7 V or the pin may float.
3. In QRSS Bipolar Mode, pins 6 and 7 for NE/PE pckg. or 3 and 4 for QE pckg. act as RNEG and RPOS, respectively.

Table 6: LXT360 Host Controlled Bipolar Mode Signal Assignments [1,2]

Pin # DIP/ PLCC	Pin # QFP[4]	Symbol	I/O[3]	Description
5	2	MODE	DI	**Mode**. Connecting MODE High puts the LXT360 in Host Mode. In Host Mode, the serial interface controls the LXT360 and displays its states.
6 7	3 4	RNEG RPOS	DO	**Received Data–Negative and Positive**. In the Bipolar I/O Mode, these pins are the negative and positive sides of a bipolar output pair. The transceiver outputs the data recovered from the line interface on these pins. A signal on RNEG corresponds to receipt of a negative pulse on RTIP/RRING. A signal on RPOS corresponds to receipt of a positive signal on RTIP/RRING. RNEG/RPOS outputs are Non-Return-to-Zero (NRZ). CLKE determine the clock edge at which these outputs are stable and valid. See Figure 19.

1. For pins not described in this table, see Table 3. Pin out for data pins in Unipolar and QRSS Modes remains the same as in Tables 4 and 5. In Host Mode, the control pins (23-28) change as shown in Table 6.
2. In QRSS Bipolar Mode, pins 6 and 7 seven act as RNEG and RPOS, respectively.
3. I/O column entries: DI = Digital Input; DO = Digital Output; DI/O = Digital Input/Output; AI = Analog Input; AO = Analog Output.
4. Pins 1, 6, 8, 11, 12, 14, 17, 22, 23, 26, 28, 30, 33, 34, 40, and 44 are not connected (*n/c*).

Table 6: LXT360 Host Controlled Bipolar Mode Signal Assignments– *continued*[1,2]

Pin # DIP/ PLCC	Pin # QFP[4]	Symbol	I/O[3]	Description
9	7	TRSTE	DI	**Tristate.** Connecting TRSTE High forces all output pins to high-impedance state. Connect this pin Low for normal operation.
10	–	*n/c*	–	*Not connected.*
11	10	*n/c*	–	*Connect Low.*
17	20	*n/c*	–	*Connect Low.*
18	21	NLOOP	DO	**Network Loopback.** This pin goes High when an Inband Network Loopback has been activated.
23	31	$\overline{\text{INT}}$	DO	**Interrupt** (Active Low–Maskable). $\overline{\text{INT}}$ goes Low to flag the host when any of the LOS, NLOOP, AIS, QRSS, DFMS or DFMO changes state or when there is an Elastic Store overflow or underflow. $\overline{\text{INT}}$ is an open drain output which requires a connection to power supply VCC through a resistor. Reset $\overline{\text{INT}}$ by writing a one to the respective bit in the Interrupt Clear Register.
24	32	SDI	DI	**Serial Data Input.** Input port for the 16-bit serial address/command and data word. LXT360 samples SDI on the rising edge of SCLK. See Figures 20 and 21.
25	35	SDO	DO	**Serial Data Output.** If CLKE is High, SDO is valid on the rising edge of SCLK. If CLKE is Low, SDO is valid on the falling edge of SCLK. This pin goes to a high-impedance state when the serial port is being written to or when $\overline{\text{CS}}$ is High. See Figure 21.
26	36	$\overline{\text{CS}}$	DI	**Chip Select** (Active Low). This input is used to access the serial interface. For each read or write operation, $\overline{\text{CS}}$ must transition from High to Low, and remain Low.
27	37	SCLK	DI	**Serial Clock.** This clock is used to write data to or read data from the serial interface registers. The clock frequency can be any rate up to 2.048 MHz.
28	38	CLKE	DI	**Clock Edge.** Setting CLKE High causes RPOS and RNEG to be valid on the falling edge of RCLK, with SDO valid on the rising edge of SCLK. Setting CLKE Low makes RPOS and RNEG valid on the rising edge of RCLK and SDO valid on the falling edge of SCLK.

1. For pins not described in this table, see Table 3. Pin out for data pins in Unipolar and QRSS Modes remains the same as in Tables 4 and 5. In Host Mode, the control pins (23-28) change as shown in Table 6.
2. In QRSS Bipolar Mode, pins 6 and 7 seven act as RNEG and RPOS, respectively.
3. I/O column entries: DI = Digital Input; DO = Digital Output; DI/O = Digital Input/Output; AI = Analog Input; AO = Analog Output.
4. Pins 1, 6, 8, 11, 12, 14, 17, 22, 23, 26, 28, 30, 33, 34, 40, and 44 are not connected (*n/c*).

Figure 2: LXT361 Bipolar Mode Pin Assignments

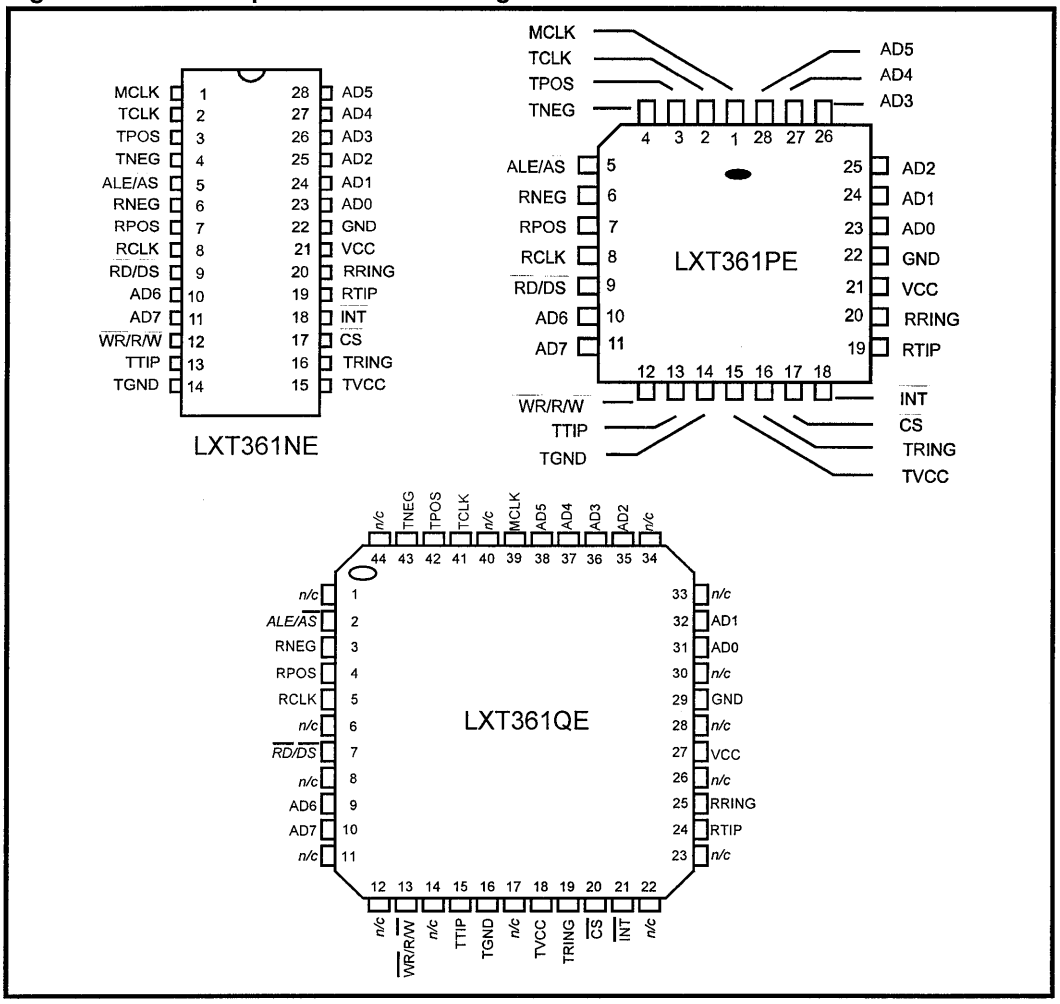


Table 7: LXT361 Clock and Data Pin Assignments by Mode[1]

Pin # DIP/ PLCC	Pin # QFP	External Data Modes		QRSS Modes	
		Bipolar Mode	Unipolar Mode	Bipolar Mode	Unipolar Mode
1	39	MCLK			
2	41	TCLK			
3	42	TPOS	TDATA	INSLER	
4	43	TNEG	INSBPV	INSBPV	

1. Data pins change based on whether external data or internal QRSS mode is active. These pins remain the same in both Hardware and Host Modes.

Table 7: LXT361 Clock and Data Pin Assignments by Mode[1]

Pin # DIP/ PLCC	Pin # QFP	External Data Modes		QRSS Modes	
		Bipolar Mode	Unipolar Mode	Bipolar Mode	Unipolar Mode
6	3	RNEG	BPV	RNEG	BPV
7	4	RPOS	RDATA	RPOS	RDATA
8	5	RCLK			
13	15	TTIP			
14	16	TGND			
15	18	TVCC			
16	19	TRING			
19	24	RTIP			
20	25	RRING			
21	27	VCC			
22	29	GND			

1. Data pins change based on whether external data or internal QRSS mode is active. These pins remain the same in both Hardware and Host Modes.

Table 8: LXT361 Processor Interface Pins

Pin # DIP/ PLCC	Pin # QFP	Address/Data Bus Type		Pin # DIP/ PLCC	Pin # QFP	Address/Data Bus Type	
		Intel	Motorola			Intel	Motorola
5	2	ALE	$\overline{AS}$	25	35	AD2	
9	7	$\overline{RD}$	$\overline{DS}$	26	36	AD3	
12	13	$\overline{WR}$	R/$\overline{W}$	27	37	AD4	
17	20	$\overline{CS}$		28	38	AD5	
18	21	$\overline{INT}$		10	9	AD6	
23	31	AD0		11	10	AD7	
24	32	AD1		--	--	--	

Table 9: LXT361 Bipolar Mode Signal Assignments

Pin # DIP/ PLCC	Pin # QFP[2]	Symbol	I/O[1]	Description
1	39	MCLK	DI	**Master Clock**. Connect to 1.544 MHz for T1 operation; to 2.048 MHz for E1. MCLK requires an external, independent input to generate internal clocks. Required accuracy is ± 32 ppm with a typical duty cycle of 50%. Upon Loss of Signal (LOS), the transceiver derives RCLK from MCLK.
2	41	TCLK	DI	**Transmit Clock**. 1.544 MHz or 2.048 MHz bit rate clock input. The transceiver samples TPOS and TNEG on the falling edge of TCLK
3 4	42 43	TPOS TNEG	DI	**Transmit Data – Positive and Negative**. In the Bipolar I/O Mode, these pins are the positive and negative sides of a bipolar input pair. Data for transmission onto the twisted-pair line is input at these pins.
5	2	ALE $\overline{AS}$	DI	**Address Latch Enable/Address Strobe** (Active Low). Connects to Intel (ALE) or Motorola ($\overline{AS}$) signal. On Motorola bus, this signal is Active Low. **Leaving this pin floating forces all output pins into a high impedance state.**
6 7	3 4	RNEG RPOS	DO	**Receive Data – Negative and Positive**. In the Bipolar I/O mode, these pins are the positive and negative sides of a bipolar output pair. Data recovered from the line interface is output on these pins. A signal on RNEG corresponds to receipt of a negative pulse on RTIP/RRING. A signal on RPOS corresponds to receipt of a positive pulse on RTIP/RRING. RNEG/RPOS outputs are Non-Return-to Zero. Both outputs are stable and valid on the rising edge of RCLK. Refer to Table 10 for Unipolar Mode function descriptions.
8	5	RCLK	DO	**Recovered Clock**. The output on this pin is the clock recovered from the line input signal. Under LOS conditions there is a smooth transition from RCLK to MCLK output.
9	7	$\overline{RD}$ $\overline{DS}$	DI	**Read** (Active Low)/**Data Strobe** (Active Low). On an Intel bus, this signal, Read, goes Low to command a read operation. On a Motorola bus, this signal, Data Strobe, goes Low when data is being driven on the address/data bus. Data is valid on the rising edge of $\overline{DS}$.
10 11	9 10	AD6 AD7	DI/O DI/O	**Address/Data bus lines 6 and 7**. Used with pins 24-28 as the address/data bus.
12	13	$\overline{WR}$ R/$\overline{W}$	DI	**Write** (Active Low) or **Write/Read**. On an Intel bus, driving this signal, Write, Low enables a write operation on the Address/Data bus. On a Motorola bus, driving this signal, Read/Write, High commands a read operation, driving it Low commands a write operation.
13 16	15 19	TTIP TRING	AO	**Transmit Tip and Ring**. Differential Driver Outputs. The design load for these outputs is 50 - 200 Ω. Select the transformer and line matching resistors to give the desired pulse height.

1. I/O column entries: DI = Digital Input; DO = Digital Output; DI/O = Digital Input/Output; AI = Analog Input; AO = Analog Output.
2. Pins 1, 6, 8, 11, 12, 14, 17, 22, 23, 26, 28, 30, 33, 34, 40, and 44 are not connected (*n/c*).

Table 9: LXT361 Bipolar Mode Signal Assignments – *continued*

Pin # DIP/ PLCC	Pin # QFP[2]	Symbol	I/O[1]	Description
14	16	TGND	–	**Ground** return for the transmit drivers power supply TVCC.
15	18	TVCC	–	**+5 VDC Power Supply** input for the transmit drivers. TVCC must not vary from VCC by more than ± 0.3 V.
17	20	$\overline{CS}$	DI	**Chip Select** (Active Low). For each read or write on the Address/Data bus, this pin must go Low during the operation. See Figures 22 and 23 for timing requirements. In the case of a single processor controlling several chips, this is the line it uses to command a specific transceiver.
18	21	$\overline{INT}$	DO	**Interrupt** (Active Low). This pin goes Low to signal an interrupt on the chip. To identify the specific interrupt, read the Performance Status Register. To clear or mask an interrupt, write a one to the appropriate bit in the Clear Interrupt Register.
19 20	24 25	RTIP RRING	AI	**Receive Tip and Ring**. The AMI signal received from the line is applied at these pins. A 1:1 transformer is required. Data and clock from the signal applied at these pins are recovered and output on the RPOS/RNEG, and RCLK pins.
21	27	VCC	–	**+5 VDC Power Supply** for all circuits except the transmit drivers. (Transmit drivers are supplied by TVCC.)
22	29	GND	–	**Ground** return for power supply VCC.
23 24 25 26 27 28	31 32 35 36 37 38	AD0 AD1 AD2 AD3 AD4 AD5	DI/ O	**Address/Data Lines 0-5**. (Also pins 10, 11–AD6 and 7) Conform to Intel and Motorola Address/Data bus specifications.

1. I/O column entries: DI = Digital Input; DO = Digital Output; DI/O = Digital Input/Output; AI = Analog Input; AO = Analog Output.
2. Pins 1, 6, 8, 11, 12, 14, 17, 22, 23, 26, 28, 30, 33, 34, 40, and 44 are not connected (*n/c*).

Table 10: LXT361 Unipolar Mode Signal Assignments[1]

Pin # DIP/ PLCC	Pin # QFP	Symbol	I/O[2]	Description
3	42	TDATA	DI	**Transmit Data**. Unipolar data for transmission onto the twisted-pair line.
4	43	INSBPV	DI	**Insert Bipolar Violation**. Controls bipolar violation insertions, requires Low-to-High transition to insert each violation, the LXT361 samples the signal on the falling edge of TCLK.
6	3	BPV	DO	**Bipolar Violation**. BPV goes High on receipt of a bipolar violation from twisted-pair line. This is an NRZ output, valid on the rising edge of RCLK.
7	4	RDATA	DO	**Received Data**. RDATA is an NRZ output of the data recovered from the line interface. RDATA is valid on the rising edge of RCLK.

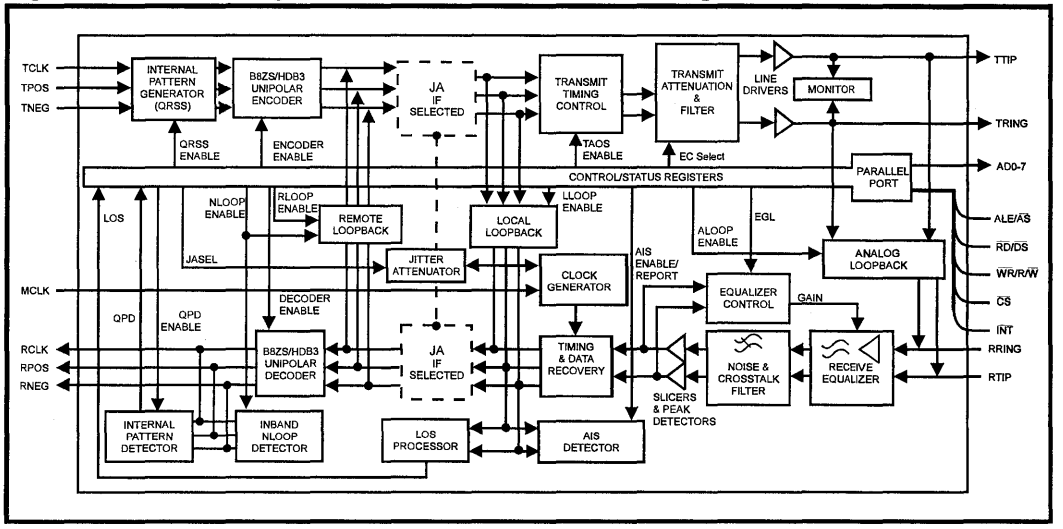
1. For the descriptions of pins not identified in this table, see Table 9: LXT361 Bipolar Mode Signal Assignments.
2. I/O column entries DI = digital input; DO = digital output, DI/O = digital input and output; AI = analog input , AO = analog output.

Table 11: LXT361 QRSS Unipolar Mode Signal Assignments[1,2]

Pin # DIP/ PLCC	Pin# QFP	Symbol	I/O[3]	Description
3	42	INSLER	DI	**Insert Logic Error**. When this pin goes from Low to High, the transceiver inserts a logic error into the transmitted QRSS data pattern. The error follows the data flow in whatever loopback mode is in effect. The LXT361 samples this pin on the falling edge of TCLK (or MCLK, if TCLK is not present).
4	43	INSBPV	DI	**Insert Bipolar Violation**. When this pin goes from Low to High, the transceiver inserts a bipolar violation error into the transmitted QRSS data pattern. A subsequent insertion requires another Low to High transition. The LXT361 samples this pin on the falling edge of TCLK (or MCLK, if TCLK is not present).
6	3	BPV	DO	**Bipolar Violation**. BPV goes High on receipt of a bipolar violation from twisted-pair line. This is an NRZ output, valid on the rising edge of SCLK.
7	4	RDATA	DO	**Received Data**. RDATA is an NRZ output of the data recovered from the line interface. RDATA is valid on the rising edge of RCLK.

1. For the descriptions of pins not identified in this table, see Table 9.
2. In QRSS Bipolar Mode, pins 6 and 7 for NE/PE pckg. or 3 and 4 for QE pckg. act as RNEG and RPOS, respectively.
3. I/O column entries DI = digital input; DO = digital output, DI/O = digital input and output; AI = analog input, AO = analog output.

Figure 3: LXT361 Integrated T1/E1 Transceiver Block Diagram



FUNCTIONAL DESCRIPTION

The LXT360 and LXT361 are fully integrated, PCM transceivers for long- or short-haul, 1.544 Mbps (T1) or 2.048 Mbps (E1) applications allowing full-duplex transmission of digital data over existing twisted-pair installations. They interface with two twisted-pair lines (one pair each for transmit and receive) through standard pulse transformers and appropriate resistors.

The figure at the front of this Data Sheet shows a block diagram of the LXT360. Control of this chip is via either a serial microprocessor port or, in Hardware Mode, via individual pin settings. Figure 3 is a block diagram of the LXT361. The LXT361 has a parallel port for microprocessor control. Both transceivers provide a high-precision, crystal-less jitter attenuator. The user may place it in the transmit or receive path, or bypass it completely.

The transceivers meet or exceed FCC and AT&T specifications for CSU and DSX-1 applications, as well as ANSI T1/E1, and ITU and ETSI requirements for E1 ISDN PRI applications.

INITIALIZATION

During power up, the transceiver remains static until the power supply reaches approximately 3 V. On crossing this threshold, the device begins a 32 ms reset cycle to calibrate the Phase Lock Loops (PLL). The transceiver uses a reference clock to calibrate the PLL; the transmitter reference is TCLK, and the receiver reference clock is MCLK. MCLK is mandatory for chip operation.

Reset Operation

Reset clears and sets all registers to 0 and resets the status and state machines for the LOS, AIS, NLOOP, and QRSS blocks. In Hardware Mode, holding pins RLOOP, LLOOP and TAOS High for at least one clock cycle resets the device. Writing a 1 to the bit CR2.RESET commands reset in Host Mode. Allow 32 ms for the device to settle after removing all reset conditions.

TRANSMITTER

Digital Data Interface

Input data for transmission onto the line is clocked serially into the device at the TCLK rate. TPOS and TNEG are the bipolar data inputs. TDATA accepts unipolar data. (Setting the TRSTE pin to Midrange enables Hardware Unipolar Mode.)

Input data may pass through either the Jitter Attenuator or B8ZS/HDB3 encoder or both. Bit CR1.ENCENB = 1 enables B8ZS/HDB3 encoding in Host Mode. In Hardware Mode, connecting the MODE pin to Midrange selects zero suppression coding. With zero suppression enabled, the EC*x* inputs (see Table 12) determine the coding scheme (B8ZS for T1 or HDB3 for E1 mode). To select the HDB3 scheme, set EC4-1 to 1000, 1001 or 1010. Other EC*x* settings select the B8ZS option. The transmit clock (TCLK) supplies input synchronization. The Test Specifications section defines the transmit timing requirements for TCLK and the Master Clock (MCLK).

Short Circuit Limit

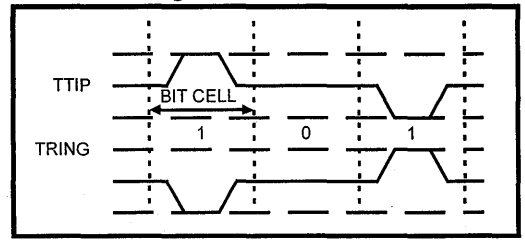
The transmitter includes a short circuit limiter. This limits the current sourced into a low impedance load. It automatically resets when the load current drops below the limit. The current is determined by the interface circuitry (total resistance on transmit side).

In Host Mode, the Performance Status Register flags open circuits in bit PSR.DFMO. A transition on DFMO will provide an interrupt and the transition sets bit TSR.DFMO = 1. Writing a 1 in bit ICR.CDFMO clears the interrupt; leaving a 1 in the bit masks that interrupt.

Output Drivers

The transceivers transmit data as a 50% line code as shown in Figure 4. Activating the line driver only during a mark reduces power consumption. The output driver is disabled during transmission of a space. Biasing of the transmit DC level is on-chip.

Figure 4: 50% Duty Cycle Coding Diagram



Idle Mode

Transmit Idle Mode is a normal operational mode (as opposed to modes) which allows multiple transceivers to be connected to a single line for redundant applications. TTIP and TRING remain in a high impedance state when TCLK is not present. Remote or Dual Loopback, TAOS or any internal transmit patterns temporarily disable the high impedance state as will detection of Network Loop Up code in the receive direction.

Pulse Shape

The Equalizer Control inputs (EC4-1) determine the transmitted pulse shape as in Table 12. In Host Mode, the I/O port controls the EC*x* values. For the LXT360 in Hardware Mode, four individual pins provide the EC*x* inputs.

Shaped pulses meeting the various T1, DS1, DSX-1 and E1 specifications are applied to the AMI line driver for transmission onto the line at TTIP and TRING. The transceivers produce DSX-1 pulses for short-haul T1 applications (settings from 0 dB to +3.0 dB), DS1 pulses for long-haul T1 applications (settings from 0 dB to -22.5 dB), and a G.703 pulse for E1 applications. Refer to the Test Specifications section for pulse mask specifications.

RECEIVER

A 1:1 transformer provides the interface to the twisted-pair line. Recovered data is output at RPOS/RNEG (RDATA in Unipolar Mode), and the recovered clock is output at RCLK. The Test Specifications section shows receiver timing.

Receiver Equalizer

The receive equalizer processes the signal received at RTIP and RRING. The equalizer gain is up to 43 dB in E1 long-haul applications. In T1 long-haul applications, the equalizer control (EC*x*) input pins or register bits determine the maximum gain applied at the equalizer. With EC1 Low, up to 36 dB of gain may be applied. When EC1 is High, 26 dB is the gain limit to provide an increased noise margin in shorter loop operations.

The receiver can accurately recover signals with up to 36 dB of cable attenuation (from 2.4 V) for T1 and up to 43 dB of cable attenuation (from 2.7 V) for E1 operation.

Data Recovery

The transceiver filters the equalized signal and applies it to the peak detector and data slicers. The peak detector samples the inputs and determines the maximum value of the received signal. The data slicers are set at 50% of the peak value to ensure optimum signal-to-noise performance.

After processing through the data slicers, the received signal goes to the data and timing recovery section, then to the B8ZS/HDB3 decoder (if selected) and to the receive monitor. The data and timing recovery circuits provide input jitter tolerance significantly better than required by AT&T Pub 62411 and ITU G.823. See the Test Specifications section.

Digital Data Interface

In either Host or Hardware Control Mode the recovered data goes to the Loss of Signal (LOS) Monitor. In Host Control Mode, it also goes through the Alarm Indication Signal (AIS, Blue Alarm) Monitor. The jitter attenuator circuit may be enabled or disabled in the receive data path or the transmit path. Received data may go through either the B8ZS or HDB3 decoder or neither. Finally, the device may send the digital data to the framer as either unipolar or bipolar data.

When transmitting unipolar data to the framer, the device reports receiving bipolar violations by driving the BPV pin High. During E1 operation in Host Control Mode, the device can report HDB3 code violations and Zero Substitution Violations on the BPV pin. The diagnostics section explains these options in more detail.

Receiver Monitor Mode

The receive equalizer of the LXT360/361 can be used in Monitor Mode applications. Monitor Mode applications are those requiring a resistive attenuation of the signal in addition to a small amount of cable attenuation (less than 6 dB). Setting bit CR3.EQZMON = 1 configures the device to work in its Monitor Mode. The device must be in its long-haul receiver mode (set bits CR1.EC*x* = 0xx0 or 1001 or 1010) for Monitor Mode. This feature is not available in the LXT360 Hardware Mode.

With the device in Monitor Mode, the receive equalizer handles signals attenuated resistively by 20 to 30 dB, along with 0 to 6 dB of cable attenuation for both E1 and T1 applications.

JITTER ATTENUATION

A Jitter Attenuation Loop (JAL) with an Elastic Store (ES) provides jitter attenuation as shown in the Test Specifications section. The JAL requires no special circuitry, such as an external quartz crystal or high-frequency clock (higher than the line rate). Its timing reference is the master clock, MCLK.

In Hardware Control Mode the ES is a 32 x 2-bit register. Setting the JASEL pin High places the JA circuitry in the received data path; setting JASEL Low places the JA in the transmit data path; tying it to Midrange disables the JA.

In Host Mode, bit CR1.JASEL0 enables or disables the JA circuit. With bit CR1.JASEL0 = 1, bit CR1.JASEL1 controls the JA circuit placement (see Table 17). The ES can be either a 32 x 2-bit or 64 x 2-bit register depending on the value of bit CR3.ES64 (see Table 19.)

The device clocks data into the ES using either TCLK or Receiver Recovered Clock depending on whether the JA circuitry is in the transmit or receive data path, respectively. Data is shifted out of the elastic store using the dejittered clock from the JAL. When the FIFO is within two bits of overflowing or underflowing, the ES adjusts the output clock by $^1/_8$ of a bit period. The ES produces an average delay of 16 bits (or 32 bits, with the 64-bit ES option selected in Host Control Mode) in the associated data path. When the Jitter Attenuator is in the receive path, the output RCLK transitions smoothly to MCLK in the event of an LOS condition.

The Transition Status Register bits TSR.ESOVR and TSR.ESUNF indicate an overflow or underflow, respectively, in the ES. These are sticky bits: once set to 1, they remain set until the host reads the register. The ES can also provide a maskable interrupt on either overflow or underflow.

Table 12: Equalizer Control Input Settings

EC4	EC3	EC2	EC1[1]	Function	Pulse	Cable	Gain	Coding[2]
0	0	0	0	T1 Long Haul	0.0 dB pulse	100 Ω TP	36 dB	B8ZS
0	0	1	0	T1 Long Haul	-7.5 dB pulse	100 Ω TP	36 dB	B8ZS
0	1	0	0	T1 Long Haul	-15.0 dB pulse	100 Ω TP	36 dB	B8ZS
0	1	1	0	T1 Long Haul	-22.5 dB pulse	100 Ω TP	36 dB	B8ZS
0	0	0	1	T1 Long Haul	0.0 dB pulse	100 Ω TP	26 dB	B8ZS
0	0	1	1	T1 Long Haul	-7.5 dB pulse	100 Ω TP	26 dB	B8ZS
0	1	0	1	T1 Long Haul	-15.0 dB pulse	100 Ω TP	26 dB	B8ZS
0	1	1	1	T1 Long Haul	-22.5 dB pulse	100 Ω TP	26 dB	B8ZS
1	0	0	0	E1 Short Haul	ITU G.703	120 Ω TP/75 Ω Coax	12 dB	HDB3
1	0	0	1	E1 Long Haul	ITU G.703	120 Ω TP	43 dB	HDB3
1	0	1	0	E1 Long Haul	ITU G.703	120 Ω TP/75 Ω Coax	43 dB	HDB3
1	0	1	1	T1 Short Haul	0-133 ft / 0.6 dB	100 Ω TP	12 dB	B8ZS
1	1	0	0	T1 Short Haul	133-266 ft / 1.2 dB	100 Ω TP	12 dB	B8ZS
1	1	0	1	T1 Short Haul	266-399 ft / 1.8 dB	100 Ω TP	12 dB	B8ZS
1	1	1	0	T1 Short Haul	399-533 ft / 2.4 dB	100 Ω TP	12 dB	B8ZS
1	1	1	1	T1 Short Haul	533-655 ft / 3.0 dB	100 Ω TP	12 dB	B8ZS

1. EC1 sets the receive equalizer gain (EGL) during T1 long-haul operation.
2. When enabled.

DIAGNOSTIC MODE OPERATION

LXT360/361 offers multiple diagnostic modes as shown in Table 13. In Hardware Mode, the diagnostic modes are selected by a combination of pin settings. In Host Mode, the diagnostic modes are selected by writing appropriate bits in the Diagnostic Control Register.

Table 13: Diagnostic Mode Availability

Diagnostic Mode	Availability[1]		Host Mode[2] Maskable
	H/W	Host	
Loopback Modes			
Local Loopback (LLOOP)	Yes	Yes	No
Analog Loopback (ALOOP)	Yes	Yes	No
Remote Loopback (RLOOP)	Yes	Yes	No
In-band Network Loopback (NLOOP)	Yes	Yes	Yes
Dual Loopback (DLOOP)	Yes	Yes	No
Internal Data Pattern Generation and Detection			
Transmit All Ones (TAOS)	Yes	Yes	No
Quasi-Random Signal Source (QRSS)	Yes	Yes	Yes
In-band loop up/down code generator	No	Yes	No
Error Insertion and Detection			
Bipolar Violation Insertion (INSBPV)	Yes	Yes	No
Logic Error Insertion (INSLER)	Yes	Yes	No
Bipolar Violation Detection (BPV)	Yes	Yes	No
Logic Error Detection, QRSS (QPD)	Yes	Yes	No
HDB3 Code Violation Detection (CODEV)	No	Yes	No
HDB3 Zero violation Detection (ZEROV)	No	Yes	No
Alarm Condition Monitoring			
Receive Loss of Signal (LOS) monitoring	Yes	Yes	Yes
Receive Alarm Indication Signal (AIS) monitoring	No	Yes	Yes
Transmit Driver Failure Monitoring—Open (DFMO)	No	Yes	Yes
Elastic store overflow and underflow monitoring	No	Yes	Yes
Other Diagnostic Reports			
Receive Line Attenuation Indicator (LATN)	No	Yes	No
Built-In Self Test (BIST)	No	Yes	Yes

1. In Hardware Control Mode, a combination of pin settings selects the Diagnostics Modes; in Host Control Mode, writing appropriate bits in the Control Registers selects the Diagnostic Modes.
2. Host Control Mode allows interrupt masking by writing a "1" to the corresponding bit in the Interrupt Clear Register. Hardware Control Mode has no interrupt masking feature.

LOOPBACK MODES

NOTE
Hardware Mode pins discussed in this section refer to the LXT360 only.

Local Loopback

See Figures 5 and 6. In Hardware Mode, Local Loopback (LLOOP) is selected by tying LLOOP High; in Host Mode, by setting CR2.ELLOOP to 1. LLOOP inhibits the receiver circuits. The transmit clock and data inputs (TCLK and TPOS/TNEG or TDATA) loop back through the jitter attenuator (if enabled) and show up at RCLK and RPOS/RNEG or RDATA. (During LLOOP, the JASEL input is strictly an Enable/Disable control; it does not affect the placement of the JAL. If JA is enabled, it is active in the loopback circuit. If JA is bypassed, it is not active in the loopback circuit.)

The transmitter circuits are unaffected by LLOOP. LXT360/361 transmits the TPOS/TNEG or TDATA inputs (or a stream of 1s if TAOS is asserted) normally. When used in this mode, the transceiver can function as a stand-alone jitter attenuator.

Figure 5: TAOS with LLOOP *(JA Selected)*

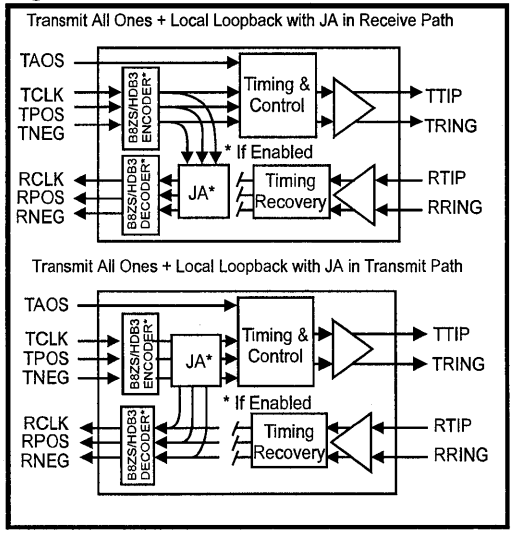
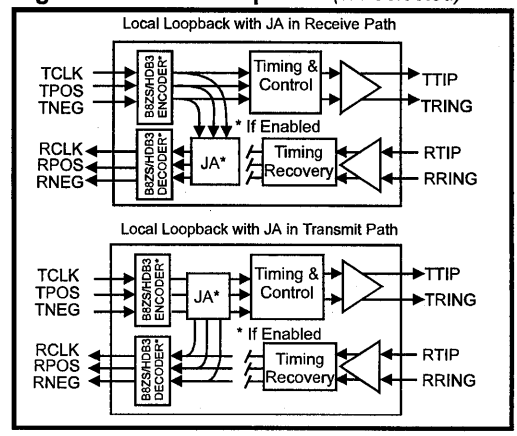


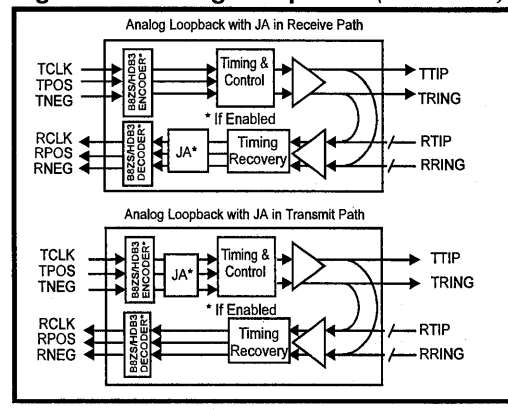
Figure 6: Local Loopback *(JA Selected)*



Analog Loopback

See Figure 7. Analog Loopback (ALOOP) exercises the maximum number of functional blocks. ALOOP operation disconnects the RTIP/RRING inputs from the line and routes the transmit outputs back into the receive inputs. This tests the encoders/decoders, jitter attenuator, transmitter, receiver and timing recovery sections. In Hardware Mode, tying pin 27 to Midrange commands Analog Loopback; in Host Mode, writing a 1 to bit CR2.EALOOP enables the function. The ALOOP function overrides all other loopback modes.

Figure 7: Analog Loopback *(JA Selected)*



Remote Loopback

See Figure 8. In Remote Loopback (RLOOP) mode, the device ignores the transmit data and clock inputs (TCLK and TPOS/TNEG or TDATA), and bypasses the in-line encoders/decoders. The RPOS/RNEG or RDATA outputs loop back through the transmit circuits to TTIP and TRING at the RCLK frequency. The RLOOP command does not affect the receiver circuits which continue to output the RCLK and RPOS/RNEG or RDATA signals received from the twisted-pair line. In Host Mode, command RLOOP by writing a 1 to bit CR2.ERLOOP. In Hardware Mode, RLOOP is commanded by setting pin 26 High.

Network Loopback

Network Loopback (NLOOP) can be initiated only when the Network Loopback detect function is enabled. In Host Mode, writing a 1 to CR2.ENLOOP enables NLOOP detection. In Hardware Mode, setting RLOOP to Midrange enables Network Loopback detection.

With NLOOP detection enabled, the receiver looks for the NLOOP data patterns (00001 = enable, 001 = disable) in the input data stream. When the receiver detects an NLOOP enable data pattern repeated for a minimum of five seconds, the device enables RLOOP. The device responds to both framed and unframed NLOOP patterns. Once NLOOP detection is enabled at the chip and activated by the appropriate data pattern, it is identical to Remote Loopback (RLOOP). NLOOP is disabled by receiving the 001 pattern for five seconds, or by activating RLOOP or ALOOP, or by disabling NLOOP detection. The device goes into Dual Loopback Mode (DLOOP) in the case where it detects both the NLOOP and LLOOP functions.

Dual Loopback

See Figure 9. To select Dual Loopback (DLOOP), set both RLOOP and LLOOP High in Hardware Mode or set bits CR2.ERLOOP and CR2.ELLOOP to 1 in Host Mode. In DLOOP mode, the transmit clock and data inputs (TCLK and TPOS/TNEG or TDATA) loop back through the Jitter Attenuator (unless disabled) to RCLK and RPOS/RNEG or RDATA. The data and clock recovered from the twisted-pair line loop back through the transmit circuits to TTIP and TRING without jitter attenuation.

3

Figure 8: Remote Loopback *(JA Selected)*

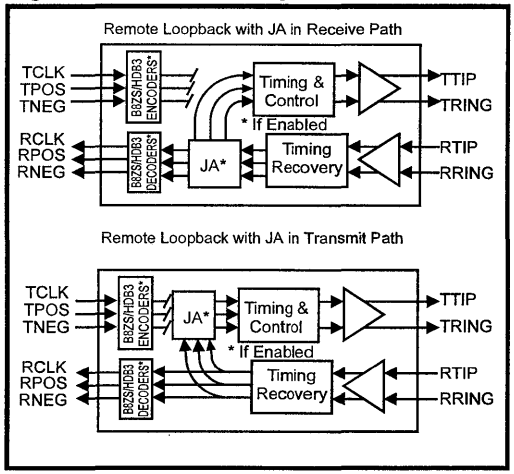
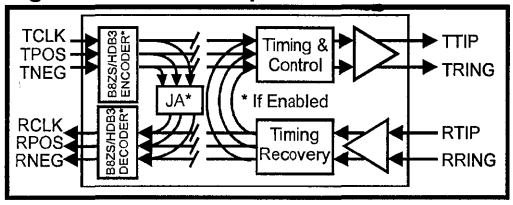


Figure 9: Dual Loopback

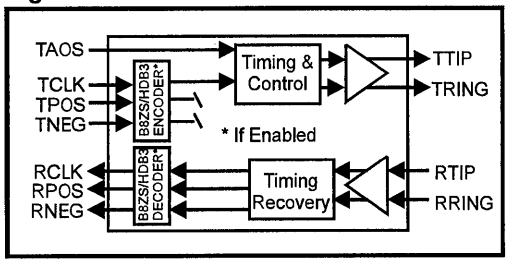


INTERNAL PATTERN GENERATION AND DETECTION

Transmit All Ones

See Figure 10. In Transmit All Ones (TAOS) Mode the transceiver ignores the TPOS and TNEG inputs and transmits a continuous stream of 1s at the TCLK frequency. (With no TCLK, the TAOS output clock is MCLK.) This can be used as the Alarm Indication Signal (AIS–also called the Blue Alarm). In Host Mode, TAOS is commanded by writing a 1 to bit CR2.ETAOS. In Hardware Mode setting pin 28 High does so. Both TAOS and Local Loopback can occur simultaneously as shown in Figure 5, but Remote Loopback inhibits TAOS. When both TAOS and LLOOP are active, TCLK and TPOS/TNEG loop back to RCLK and RPOS/RNEG through the jitter attenuator (if enabled), and an all ones pattern goes to TTIP/TRING.

Figure 10: TAOS Data Path



Quasi-Random Signal Source (QRSS)

See Figure 11. For T1 operation, the Quasi-Random Signal Source (QRSS) is a 2^{20}-1 pseudo-random bit sequence (PRBS) with no more than 14 consecutive zeros. For E1 operation, QRSS is 2^{15}-1 PRBS with inverted output.

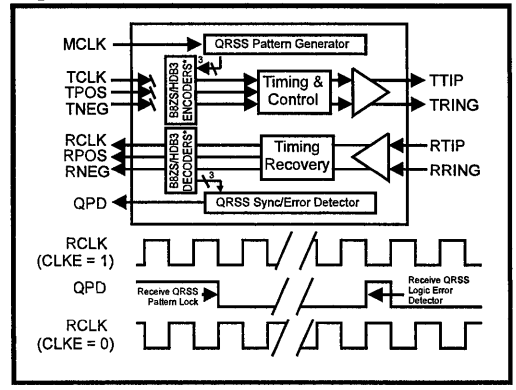
Both Hardware and Host Modes allow QRSS Mode. The QRSS pattern is normally locked to TCLK; but if there is no TCLK, MCLK is the clock source. Bellcore Pub 62411 defines the T1 QRSS transmit format and ITU G.703 defines the E1 format.

Connecting TAOS (pin 28) Midrange enables QRSS transmission in Hardware Mode. In Host Mode, setting bits CR2.EPAT0 = 0 and CR2.EPAT1=1enables this function.

With QRSS transmission enabled, it is possible to insert a logic error into the transmit data stream by causing a Low-to-High transition on INSLER (pin 3). However, if no logic or bit errors are to be inserted into the QRSS pattern, INSLER must remain Low. Logic Error insertion waits until the next bit if the current bit is "jammed". (When there are more than 14 consecutive 0s, the output is jammed to a 1.)

Furthermore a bipolar violation in the QRSS pattern is possible by causing a Low-to-High transition on INSBPV (pin 4) without regard to whether the device is in bipolar or unipolar operating mode.

Figure 11: QRSS Mode



Choosing QRSS Mode also enables the QRSS Pattern Detection (QPD) in the receive path. The QRSS pattern is synchronized when there are fewer than four errors in 128 bits. After achieving synchronization the device drives QPD (pin 12) Low (QPD output is available on LXT360 only). The LXT361 does not support bit error detection in QRSS Mode. In the LXT360 QRSS Mode, any subsequent bit error in the QRSS pattern causes QPD to go High for half an RCLK clock cycle (the precise relationship to RCLK depends on the value of CLKE–when CLKE is Low, QPD goes High while RCLK is High; if CLKE is High, QPD goes High while RCLK is Low). This signal edge can serve as a trigger for an external bit-error counter. An LOS condition or a loss of QRSS synchronization will cause this output to go High continuously. In this case, and with either Unipolar Mode or the encoders/decoders enabled, the BPV pin indicates BPVs, CODEVs or ZEROVs as chosen.

Host Mode offers an additional interrupt to indicate that QRSS detection and sychronization have occurred, or that synchronization is lost. This interrupt is available when bit ICR.CQRSS = 0. If the QPD signal triggers a bit error counter, the interrupt could start or reset the counter.

Also in Host Mode, the PSR.QRSS bit provides an indication of the QRSS pattern synchronization. This bit goes Low with no QRSS pattern detected (*i.e.*, when there are more than four errors in 128 bits). The TQRSS bit in the Transition Status Register indicates that QRSS status has changed since the last QRSS Interrupt Clear command.

In-Band Network Loop Up or Down Code Generator

In Host Mode, LXT360/361 can transmit in-band Network Loop Up or Loop Down code. The Loop Up code is 00001; Loop Down code is 001. A Loop Up code transmission occurs when Control Register #2 bits EPAT0 = 1 and EPAT1 = 0. A Loop Down code transmission requires that both EPAT0 and EPAT1 = 1.

With this mode enabled, logic errors and bipolar violations can be inserted into the transmit data stream. Inserting a logic error requires a Low-to-High transition in INSLER (pin 3). (If there are no logic or bit errors to insert, INSLER must remain Low.) Inserting a bipolar violation requires a Low-to-High transition on INSBPV (pin 4), independent of Unipolar or Bipolar operation.

ERROR INSERTION AND DETECTION

Bipolar Violation Insertion *(INSBPV)*

In Unipolar Mode, both Hardware and Host Modes provide for Bipolar Violation Insertion (INSBPV). Choosing Unipolar Mode configures pin 4 as INSBPV. Bipolar violation insertion requires a Low-to-High transition on INSBPV. Sampling occurs on the falling edge of TCLK. When INSBPV goes High a BPV is inserted on the next available mark except in the four following situations:

- Zero suppression (HDB3 or B8ZS) is not violated
- If LLOOP and TAOS are both active, the BPV is looped back to RNEG/BPV indicator and the line driver transmits all ones with no violation.
- BPV insertion is disabled with RLOOP (remote loopback) active.
- BPV insertion is disabled with NLOOP asserted (pin 10 High) .

With the LXT360/361 configured to transmit internally generated data patterns (QRSS or NLOOP), a BPV can be inserted on the transmit pattern independent of whether the device is in the unipolar or bipolar mode of operation.

LOGIC ERROR INSERTION *(INSLER)*

When configured to transmit internally generated data patterns (QRSS or NLOOP Up/Down codes), the device can insert a logic error on the transmit data pattern when there is a Low-to-High transition on INSLER. In QRSS Mode, there is no logic error insertion on a jammed bit (a bit forced to one to suppress transmission of more than 14 consecutive zeros). The transceiver treats data patterns the same way it treats data applied to TPOS/TNEG, so the inserted logic error will follow the data flow path as defined by the loopback mode in effect.

Logic Error Detection *(QPD) (LXT360 Only)*

After receiving pattern synchronization when configured in the QRSS Mode, LXT360 reports logic errors on QPD (pin 12). To indicate a logic error, this pin goes High for half an RCLK cycle (during the High period of RCLK if CLKE is Low but during the Low RCLK period if CLKE is High). To tally logic errors, connect an error counter to QPD. A continuous logic one on this pin indicates loss of either the QRSS pattern lock or LOS condition. The QRSS section has additional details on QRSS pattern lock criteria.

Bipolar Violation Detection *(BPV)*

With the internal encoders/decoders enabled or when configured in Unipolar Mode, the LXT360/361 reports received Bipolar Violations at BPV (pin 6). The pin goes High for a full clock cycle to indicate receipt of a BPV. However, if the encoders/decoders are enabled, LXT360/361 does not report bipolar violations due to the line coding scheme.

HDB3 Code Violation Detection *(CODEV)*

LXT360/361 can detect HDB3 code violations in Host Mode with HDB3 encoders enabled. This requires CR1.ENCENB = 1 and CR1.EC4-1 = 100x or 1010, which establishes E1 operation. To enable CODEV, set bit CR4.CODEV = 1.

An HDB3 code violation (CODEV) occurs when the device receives two consecutive bipolar violations of the same polarity (refer to ITU O.161). With CODEV detection enabled, LXT360/361 reports a violation on the BPV pin along with received BPVs and ZEROVs (if these options are enabled). LXT360/361 forces the BPV pin High for a full RCLK cycle to report a CODEV.

HDB3 Zero Substitution Violation Detection *(ZEROV)*

With encoders/decoders enabled, the LXT360/361 can detect HDB3 zero substitution violations (ZEROV) in Host Mode. This requires CR1.ENCENB = 1 and CR1.EC4-1 = 100x or 1010, which establish E1 operation, and CR4.ZEROV = 1.

LXT360/361 forces the BPV pin High for a full RCLK cycle to report a ZEROV. An HDB3 ZEROV is the receipt of four or more consecutive zeros. This does not occur with correctly encoded HDB3 data unless there are transmission errors. With ZEROV detection enabled, the device reports a violation on the BPV pin along with received BPVs and CODEVs (if these options are enabled).

ALARM CONDITION MONITORING

Loss of Signal *(LOS)*

The LXT360/361 Loss of Signal (LOS) monitor function is compatible with ITU G.775 and ETSI 300233. The receiver LOS monitor loads a digital counter at the RCLK frequency. The count increments with each received 0 and the counter resets to 0 on receipt of a 1. When the count reaches "n" 0s, the LOS flag goes High, and the MCLK replaces the recovered clock at the RCLK output in a smooth transition. For T1 operations, the number of 0s, n = 175, and for E1 operations, n = 32. In Host Mode, either number can be changed to 2048 by setting bit CR4.LOS2048 to 1.

For T1 operation, when the received signal has 12.5% 1s (16 marks in a sliding 128-bit period, with fewer than 100 consecutive 0s), the LOS flag returns Low and the recovered clock replaces MCLK at the RCLK output in another smooth transition.

For E1 operation, the LOS condition is cleared when the received signal has 12.5% 1s density (four 1s in a sliding 32-bit window with fewer than 16 consecutive 0s). In Host Mode E1 operation, the out-of-LOS criterion can be modified from 12.5% marks density to 32 consecutive marks by setting bit CR4.COL32CM = 1.

During LOS, the device sends received data to the RPOS/RNEG pins (or RDATA in Unipolar Mode). LXT360 reports an LOS condition on the LOS pin in Hardware Mode. In Host Mode, the LOS bit in the Performance Status Register goes High to indicate an LOS condition and will interrupt the host controller if so programmed.

Alarm Indication Signal Detection *(AIS)*

The Alarm Indication Signal (AIS) is available only in Host Mode. The receiver detects an AIS pattern when it receives fewer than three 0s in any string of 2048 bits. The device clears the AIS condition when it receives three or more 0s in a string of 2048 bits.

The AIS bit in the Performance Status Register indicates AIS detection. When the AIS status changes, the TAIS bit in the Transition Status Register goes High. The change of status interrupts the host controller by pulling $\overline{INT}$ Low, unless the interrupt is masked. Writing a 1 to the ICR.CAIS bit masks the interrupt until the bit returns to 0.

Driver Failure Open Mode *(DFMO)*

In Host Mode a DFM Open (DFMO) bit is available in the Performance Status Register to indicate an open condition on the lines. DFMO can generate an $\overline{INT}$ to the host controller. The Transition Status Register bit DFMO indicates a transition in the status of the bit. Writing a 1 to ICR.CDFMO will clear or mask the interrupt.

Elastic Store Overflow/Underflow *(ESOVR/ESUNF)*

When the bit count in the Elastic Store (ES) is within two bits of overflowing or underflowing the ES adjusts the output clock by $^1/_8$ of a bit period. In Host Mode, the ES provides an indication of overflow and underflow in the TRS.ESOVR and TSR.ESUNF. These are sticky bits and will stay set to 1 until the host controller reads the register. These interrupts can be cleared or masked by writing a 1 to the bits ICR.CESO and ICR.CESU, respectively.

OTHER DIAGNOSTIC REPORTS

Receive Line Attenuation Indication *(LATN)*

The equalizer status register (ESR) provides an approximation of the line attenuation encountered by the device. The four most significant bits of the register (ESR.LATN7-4) indicate line attenuation in approximately 2.9 dB steps for both T1 and E1 operation of the receive equalizer. For instance, if ESR.LATN7-4 is 10 (decimal), then the receiver is seeing a signal attenuated by approximately 29 dB (2.9 dB * 10) of cable loss.

Built-In Self Test *(BIST)*

LXT360/361 provides a Built-In Self Test (BIST) capability in Host Mode. The BIST exercises the internal circuits by providing an internal QRSS pattern, running it through the encoders and the transmit drivers then looping it back through the receive equalizer, Jitter Attenuator and decoders to the QRSS pattern detection circuitry. If all the blocks in this data path work correctly, the receive pattern detector locks onto the pattern. It then pulls $\overline{INT}$ Low and sets the following bits High:

- TSR.TQRSS
- PSR.QRSS
- PSR.BIST

The QPD pin (pin 12) also indicates completion status of the test. Starting the test forces this pin High. During the test, it remains High until the test finishes successfully at which time it goes Low.

The most reliable test will result with separate TCLK and MCLK and LBO = -22.5 dB (CR1.EC4-1 = 011x).

OPERATING MODES

The LXT360/361 share many features. However, their control modes are very different.

- The LXT360 operates in either Hardware or (Serial Port) Host Mode
- The LXT361 operates in (Parallel Port) Host Mode only.

In the Hardware Mode (LXT360 only) individual pins control the transceiver.

The logic level at the MODE pin sets the LXT360 mode of operation. In Host Mode (LXT360/361), a microprocessor controls the device through a data interface. The LXT360 has a serial interface and the LXT361 uses a parallel interface.

Hardware Mode Operation *(LXT360 Only)*

The LXT360 operates in Hardware Mode when MODE is set to Midrange or Low. In Hardware Mode individual pins access and control the transceiver. The outputs (RPOS/RNEG or RDATA) are valid on the rising edge of RCLK

There are some advanced functions provided only in Host Mode. Interrupt ($\overline{INT}$), AIS detection indicator, DFM open indicator and CLKE functions are some of the features available in Host Mode.

Table 14: Control and Operational Mode Selection for LXT360 Transceiver

Input to Pin[1]		Mode of Operation						
Mode	TRSTE	Hardware	Software	Unipolar	Bipolar	AMI Enc/Dec	B8ZS/HDB3 Encoder/Decoder	All Outputs Tristated
Low	Low	On	Off	Off	On	Off[3]	Off	No
Low	High	On	Off	Off	On	Off[3]	Off	Yes
Low	Open	On	Off	On	Off	On	Off	No
High[2]	Low	Off	On	x	x	x	x	No
High[2]	High	Off	On	x	x	x	x	Yes
High[2]	Open	Off	On	x	x	x	x	No
Open	Low	On	Off	On	Off	Off	On	No
Open	High	On	Off	On	Off	Off	On	Yes
Open	Open	On	Off	On	Off	Off	On	No

1. Open is either a midrange voltage or the pin is floating
2. In Software Mode, the contents of register CR1 determine the operation mode.
3. Encoding is done externally.

Host Mode Operation

The LXT360 operates in Host Mode when MODE is set High. In Host Mode a microprocessor accesses and controls the transceiver through a data port using the internal registers. The outputs (RPOS/RNEG or RDATA) are valid on the rising edge of RCLK

In Host Mode there are eight control and status registers–five read/write and three read-only registers. The LXT360 accesses them through its serial interface (SIO). The LXT361 provides this access using an 8-bit parallel interface (PIO).

The host processor/controller can completely configure the device as well as get a full diagnostic/status report through the SIO or PIO. Only the clocks and data for Bipolar Mode and BPV/Logic Error insertions for Unipolar or QRSS Mode need to be provided directly to the input pins. Similarly, the recovered clock, data, and BPV/Logic Error occurrences are available only at output pins. All other mode settings and diagnostic information are available through the data port.

Table 15 shows the address used by the SIO or PIO to access each register on the LXT360 or LXT361, respectively. Table 16 summarizes the control and status registers and labels each bit they contain. Tables 17 through 24 identify the bits in each register.

Table 15: Serial (LXT360) and Parallel (LXT361) Port Register Addresses

Register		Address[1]	
Name	Abbr	Serial Port (A7-A1)	Parallel Port (A7-A0)
Control #1	CR1	x010000	x010000x
Control #2	CR2	x010001	x010001x
Control #3	CR3	x010010	x010010x
Interrupt Clear	ICR	x010011	x010011x
Transition Status	TSR	x010100	x010100x
Performance Status	PSR	x010101	x010101x
Equalizer Status	ESR	x010110	x010110x
Control #4	CR4	x010111	x010111x

Table 16: Register Addresses and Bit Names

Register		Type	Bit							
Name			7	6	5	4	3	2	1	0
Control #1	CR1	R/W	JASEL1	JASEL0	ENCEB	UNIENB	EC4	EC3	EC2	EC1
Control #2	CR2	R/W	RESET	EPAT1	EPAT0	ETAOS	ENLOOP	EALOOP	ELLOOP	ERLOOP
Control #3	CR3	R/W	JA6HZ	PCLKE[1]	SBIST	EQZMON	*reserved*[2]	ES64	ESCEN	ESJAM
Interrupt Clear	ICR	R/W	CESU	CESO	CDFMO	*reserved*[3]	CQRSS	CAIS	CNLOOP	CLOS
Transition Status	TSR	R	ESUNF	ESOVR	TDFMO	*reserved*[2]	TQRSS	TAIS	TNLOOP	TLOS
Performance Status	PSR	R	*reserved*[2]	BIST	DFMO	*reserved*[2]	QRSS	AIS	NLOOP	LOS
Equalizer Status	ESR	R	LATN7	LATN6	LATN5	LATN4	*reserved*[2]	*reserved*[2]	*reserved*[2]	*reserved*[2]
Control #4	CR4	R/W	*reserved*[2]	*reserved*[2]	*reserved*[2]	*reserved*[2]	COL32CM	LOS2048	ZEROV	CODEV

1. Bit CR3.PCLKE is available only in the LXT361; for the LXT360, set this bit to zero.
2. In write registers, bits labeled *reserved* should be set to 0 (except as in note 3 below) for normal operation and ignored in read only registers.
3. Write a 1 into this bit for normal operation.

Table 17: Control Register #1 *Read/Write, Address (A7-A1) = x010000*

Bit	Name	Function	Jitter Attenuation		
			JASEL0	JASEL1	Position
0	EC1	Set the Equalizer Control codes (see Table 12).	1	0	Transmit
1	EC2		1	1	Receive
2	EC3		0	X	disabled
3	EC4				
4	UNIENB	Enables Unipolar I/O Mode and insertion/detection of BPVs.			
5	ENCENB	Enables B8ZS/HDB3 encoders/decoders; device enters Unipolar Mode and pins 3, 4, 6 and 7 change to their unipolar functions.			
6	JASEL0	Jitter Attenuation Mode, selects jitter attenuation circuitry position in data path or disables it. See right hand section of table for values. ↗			
7	JASEL1				

Table 18: Control Register #2 *Read/Write, Address (A7-A1) = x010001*

Bit	Name	Function	Pattern		
			EPAT0	EPAT1	Selected
0	ERLOOP[1]	Enables Remote Loopback (RLOOP)	0	0	Transmit TPOS/TNEG
1	ELLOOP[1]	Enables Local Loopback (LLOOP)	0	1	Detect and transmit QRSS
2	EALOOP	Enables Analog Loopback (ALOOP)	1	0	In-band Loop Up Code 00001
3	ENLOOP	Enables Network Loopback Detection (NLOOP)	1	1	In-band Loop Down Code 001
4	ETAOS	Enables Transmit All Ones (TAOS)			
5	EPAT0	Enables internal data pattern transmission. See right hand section of table for values. ↗			
6	EPAT1				
7	RESET	RESET = 1 resets device state and all registers.			

1. To enable Dual Loopback (DLOOP), set both ERLOOP = 1, ELLOOP = 1.

Table 19: Control Register #3 *Read/Write, Address (A7-A1) = x010010*

Bit	Name	Description
0	ESJAM	Disables jamming of elastic store read out clock ($^1/_8$ bit-time adjustment for over/underflow).
1	ESCEN	Centers ES pointer for a difference of 16 or 32 (depending on depth-clears automatically).
2	ES64	Increases ES depth from 32 to 64 bits.
3	—	*reserved–set to 0 for normal operation.*
4	EQZMON	Configures receiver equalizer for monitor mode application .
5	SBIST	Starts built-in self test.
6	PLCKE	This bit is available only in the LXT361–*for LXT360, set this bit to 0.* PCLKE = 0 sets RPOS/RNEG valid on the rising edge of RCLK. PCLKE = 1 sets RPOS/RNEG valid on the falling edge of RCLK .
7	JA6HZ	When JA6HZ = 1, changes bandwidth of Jitter Attenuation Loop from 3 Hz (default) to 6 Hz.

Table 20: Interrupt Clear Register *Read/Write, Address (A7-A1) = x010011*

Bit	Name	Function[1]
0	CLOS	Clears/Masks LOS interrupt.
1	CNLOOP	Clears/Masks NLOOP interrupt.
2	CAIS	Clears/Masks AIS interrupt.
3	CQRSS	Clears/Masks QRSS Interrupt.
4	—	*reserved–set to 1 for normal operation.*
5	CDFMO	Clears/Masks DFMO.
6	CESO	Clears/Masks ES overflow interrupt.
7	CESU	Clears/Masks ES underflow interrupt.

1. Leaving a one of in any of these bits masks the associated interrupt.

Table 21: Transition Status Register *Read Only, Address (A7-A1) = x010100*

Bit	Name	Function
0	TLOS	Loss of Signal (LOS) has changed since last clear LOS interrupt occurred.
1	TNLOOP	NLOOP has changed since last clear NLOOP interrupt occurred.

1. A QRSS transition indicates receive QRSS pattern sync or loss. A simple error in QRSS pattern is not reported as a transition.
2. Tripping the overflow or underflow indicator in the ES sets the ESOVR/ESUNF status bit(s). Reading the Transition Status Register clears these bits. Setting CESO and CESU in the Interrupt Clear Register masks these interrupts.

Table 21: Transition Status Register *Read Only, Address (A7-A1) = x010100*

Bit	Name	Function
2	TAIS	AIS has changed since last clear AIS interrupt occurred.
3	TQRSS	QRSS has changed since last clear QRSS interrupt occurred[1].
4	—	*reserved-ignore.*
5	TDFMO	DFMO has changed since last clear DFMS interrupt occurred.
6	ESOVR	ES overflow status sticky bit[2].
7	ESUNF	ES underflow status sticky bit[2].

1. A QRSS transition indicates receive QRSS pattern sync or loss. A simple error in QRSS pattern is not reported as a transition.
2. Tripping the overflow or underflow indicator in the ES sets the ESOVR/ESUNF status bit(s). Reading the Transition Status Register clears these bits. Setting CESO and CESU in the Interrupt Clear Register masks these interrupts.

Table 22: Performance Status Register *Read Only, Address (A7-A1) = x010101*

Bit	Name	Function
0	LOS	Loss of signal (LOS) status.
1	NLOOP	Network Loop (NLOOP) status.
2	AIS	Alarm Indicator (AIS) status.
3	QRSS	QRSS pattern detect status.
4	—	*reserved–ignore.*
5	DFMO	Driver open indication.
6	BIST	Built-in self test status.
7	—	*reserved–ignore*

Table 23: Equalizer Status Register *Read Only, Address (A7-A1) = x010110*

Bit	Name	Function
0	—	*reserved–ignore* (Least Significant Bit)
1	—	*reserved–ignore*
2	—	*reserved–ignore*
3	—	*reserved–ignore*
4	LATN4	Receive Line Attenuation Indicators. Convert this binary output to a decimal number and multiply by 2.9 dB to determine the approximate cable attenuation as seen by the receiver. For instance, if LATN7-4 = 1010 $_{BIN}$ (= 10 $_{DEC}$), then the receiver is seeing a signal attenuated by approximately 29 dB (2.9 dB x 10) of cable.
5	LATN5	
6	LATN6	
7	LATN7	

Table 24: Control Register #4 *Read/Write, Address (A7-A1) = x010111*

Bit	Name	Function
0	CODEV	Enables detection of HDB3 code violation on the BPV pin along with bipolar violations and ZEROVs (as enabled).
1	ZEROV	Enables detection of four consecutive zeros (an HDB3 coding violation) on the BPV pin along with bipolar violation and ZEROVs (as enabled).
2	LOS2048	Changes LOS detection threshold from 32 consecutive zeros (for E1 operation) or 175 consecutive zeros (T1 operation) to 2048 consecutive zeros in either environment.
3	COL32CM	In E1 Mode, changes "clear LOS condition" criterion from 12.5% marks density (default) to receipt of 32 consecutive marks.
4	—	*reserved–set to 0 for normal operation; ignore when reading.*
5	—	*reserved–set to 0 for normal operation; ignore when reading.*
6	—	*reserved–set to 0 for normal operation; ignore when reading.*
7	—	*reserved–set to 0 for normal operation; ignore when reading.*

Serial Port Operation *(LXT360 Only)*

The LXT360 operates in Host Mode when the MODE pin is set High. Figure 12 shows the SIO data structure. The registers are accessible through a 16-bit word: an 8-bit Command/Address byte (bits R/$\overline{W}$ and A1-A7) and a subsequent 8-bit data byte (bits D0-7). Bit R/$\overline{W}$ determines whether a read or a write operation occurs. Bits A6-1 in the Command/Address byte address specific registers (the address decoder ignores bit A7). The data byte depends on both the value of bit R/$\overline{W}$ and the address of the register as set in the Command/Address byte.

Host Mode provides a latched interrupt output ($\overline{INT}$). A change in the state of any of the following bits in the Performance Status Register will drive $\overline{INT}$ Low: LOS, NLOOP, AIS, QRSS, or DFMO. An interrupt will also occur when there is an elastic store overflow or underflow. When the interrupt has occurred, the $\overline{INT}$ output pin is pulled Low. The output stage of each $\overline{INT}$ pin consists only of a pull-down device, so each one requires an external pull-up resistor. The interrupt is cleared when the interrupt condition no longer exists, and the host processor writes a 1to the respective interrupt causing bit(s) in the Interrupt Register. Leaving a 1 in any of these interrupt status bits masks that interrupt.

Table 25: CLKE Settings

CLKE	Output	Clock	Valid Edge
Low	RPOS	RCLK	Rising
	RNEG	RCLK	Rising
	SDO	SCLK	Falling
High	RPOS	RCLK	Falling
	RNEG	RCLK	Falling
	SDO	SCLK	Rising

Host Mode also allows control of the serial data and receive data output timing. The clock edge (CLKE) signal determines when the outputs are valid, relative to the Serial Clock (SCLK) or RCLK as shown in Table 25.

Parallel Port Operation *(LXT361 Only)*

The LXT361 address/control bus pins and control pins are compatible with both the Intel and Motorola address/data buses. See Figures 22 and 23 for the I/O timing diagram for each bus. The device automatically detects bus timing based on the Intel and Motorola microprocessor bus specifications. The maximum recommended processor speed for an Intel device is 20 MHz; for a Motorola device, 16.78 MHz. Table 17 summarizes the control and status registers for the LXT361. Tables 17 through 24 identify and explain the bits in the control registers.

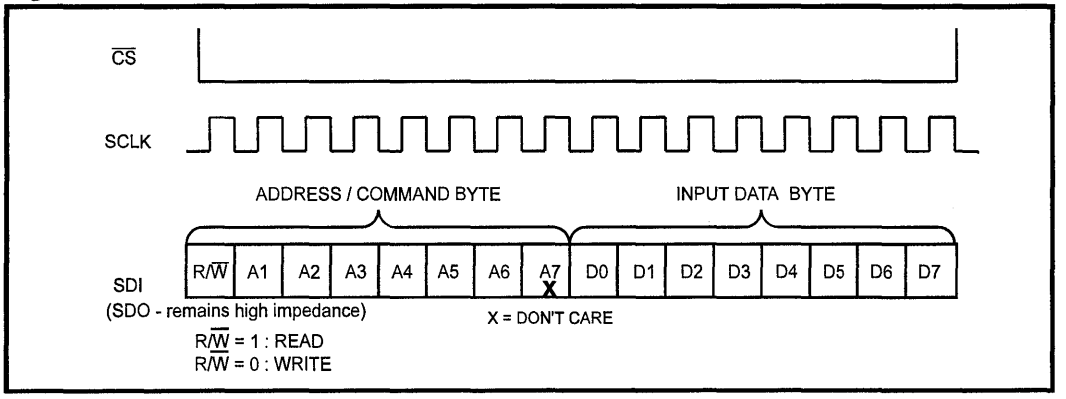
The LXT361 provides a latched interrupt output ($\overline{INT}$). A change in the state of any of the following bits in the Performance Status Register will drive $\overline{INT}$ Low: LOS, NLOOP, AIS, QRSS, DFMO. When the interrupt has occurred, the $\overline{INT}$ output pin is pulled Low. The output stage of $\overline{INT}$ pin consists only of a pull-down device, so each pin requires an external pull-up resistor. The interrupt is cleared when the interrupt condition no longer exists, and the host processor writes a 1 to the respective interrupt causing bit(s) in the Interrupt Register. Leaving a 1 in any of these interrupt status bits masks that interrupt.

The received data output is valid on the rising edge of RCLK, when bit CR3.PCLKE = 0. The data output is valid on the falling edge of RCLK when CR3.PCLKE =1.

There are five read/write and three read-only registers. Only bits A6-1 in the address byte are valid. (The address decoder ignores bits A7 and A0.) Tables 17 through 24 show the register address bits A7-1, without regard to bit A0.

3

Figure 12: LXT360 Serial Interface Data Structure



APPLICATION INFORMATION

NOTE

This application information is for design aid only.

Table 26 shows the specification for transmit return loss in E1 applications. (The G.703/CH PTT specification is a Swiss Telecommunications Ministry specification.)

Tables 27 through 30 show the transmit return loss values for E1 short- and long-haul and T1 applications. Table 37 shows the receive return loss values.

Table 26: E1 Transmit Return Loss Requirements

Frequency Band	Return Loss	
	ETS 300 166	G.703/CH PTT
51-102 kHz	6 dB	8 dB
102-2048 kHz	8 dB	14 dB
2048 - 3072 kHz	8 dB	10 dB

Table 27: Transmit Return Loss (2.048 Mbit/s–Short-Haul)

EC4-1	Xfrmr/Rt	Rload (Ω)	Cl (pF)	Return Loss (dB)
1000	1:2/ 9.1 Ω	75	0	14
			470	16
		120	0	12
			470	13
	1:2.3/ 9.1 Ω	120	0	13
			470	16

Table 28: Transmit Return Loss (2.048 Mbit/s–Long-Haul) *High Return Loss Configuration*

EC4-1	Xfrmr/ Rt	Rload (Ω)	Cl (pF)	Return Loss (dB)
1001	1:2/ 15 Ω	120	0	19
			470	28
	1:1.53/ 15 Ω	75	0	18
			470	28

Table 29: Transmit Return Loss (2.048 Mbit/s–Long-Haul)

EC4-1	Xfrmr/ Rt	Rload (Ω)	Cl (pF)	Return Loss (dB)
1010	1:2/ 9.1 Ω	120	0	12
			470	13
		75	0	16
			470	18

Table 30: Transmit Return Loss (1.544 Mbit/s–Long- or Short-Haul)

EC4-1	Xfrmr/Rt	Rload (Ω)	Cl (pF)	Return Loss (dB)
Refer to Table 12	1:2/9.1 Ω	100	0	16
			470	17
	1:1.15[1]/ 0 Ω	100	0	2 dB
			470	2 dB

1. A 1:1.15 transmit transformer keeps the total transceiver power dissipation at a low level, a 0.47 µF DC blocking capacitor must be placed on TTIP or TRING.

Table 31: Transformer Specifications for LXT360/LXT361

Tx/Rx	Frequency MHz	Turns Ratio	Primary Inductance µH (minimum)	Leakage Inductance µH (max)	Interwinding Capacitance pF (max)	DCR Ω (maximum)	Dielectric[1] Breakdown V (minimum)
Tx	1.544	1:1.15	600	0.80	60	0.90 pri 1.70 sec	1500 VRMS
	2.048	1:2.3	600	0.80	60	0.70 pri 1.20 sec	1500 VRMS[2]
	1.544/2.048	1:2	600	0.80	60	0.70 pri 1.20 sec	1500 VRMS[2]
Rx	1.544/2.048	1:1	600	1.10	60	1.10 pri 1.10 sec	1500 VRMS[2]

1. Some ETSI applications may require a 2.3 kV dielectric breakdown voltage.
2. Some applications require transformers with center tap (Long-Haul applications with DC current in the E1/T1 loop).

Table 32: Recommended Transformers for LXT360/LXT361

Tx/Rx	Turns Ratio	Part Number	Manufacturer
Tx	1:1.53	PE-68663	Pulse Engineering
	1:1.15	PE-65388	
		PE-65770	
		16Z5952	Vitec
	1:2	PE-65351	Pulse Engineering
		PE-65771	
		0553-5006-IC	Bell-Fuse
		66Z-1308	Fil-Mag
		671-5832	Midcom
		67127370	Schott Corp
		67130850	
		TD61-1205D	HALO (combination Tx/Rx set)
		TG26-1205NI	HALO (surface mount dual transformer 1CT:2CT & 1CT:2CT)
		TG48-1205NI	HALO (surface mount dual transformer 1CT:2CT & 1:1)
		16Z5946	Vitec
	1:2.3	PE-65558	Pulse Engineering
Rx	1:1	FE 8006-155	Fil-Mag
		671-5792	Midcom
		PE-64936	Pulse Engineering
		PE-65778	
		67130840	Schott Corp
		67109510	
		TD61-1205D	HALO (combination Tx/Rx set)
		16Z5936	Vitec
		16Z5934	

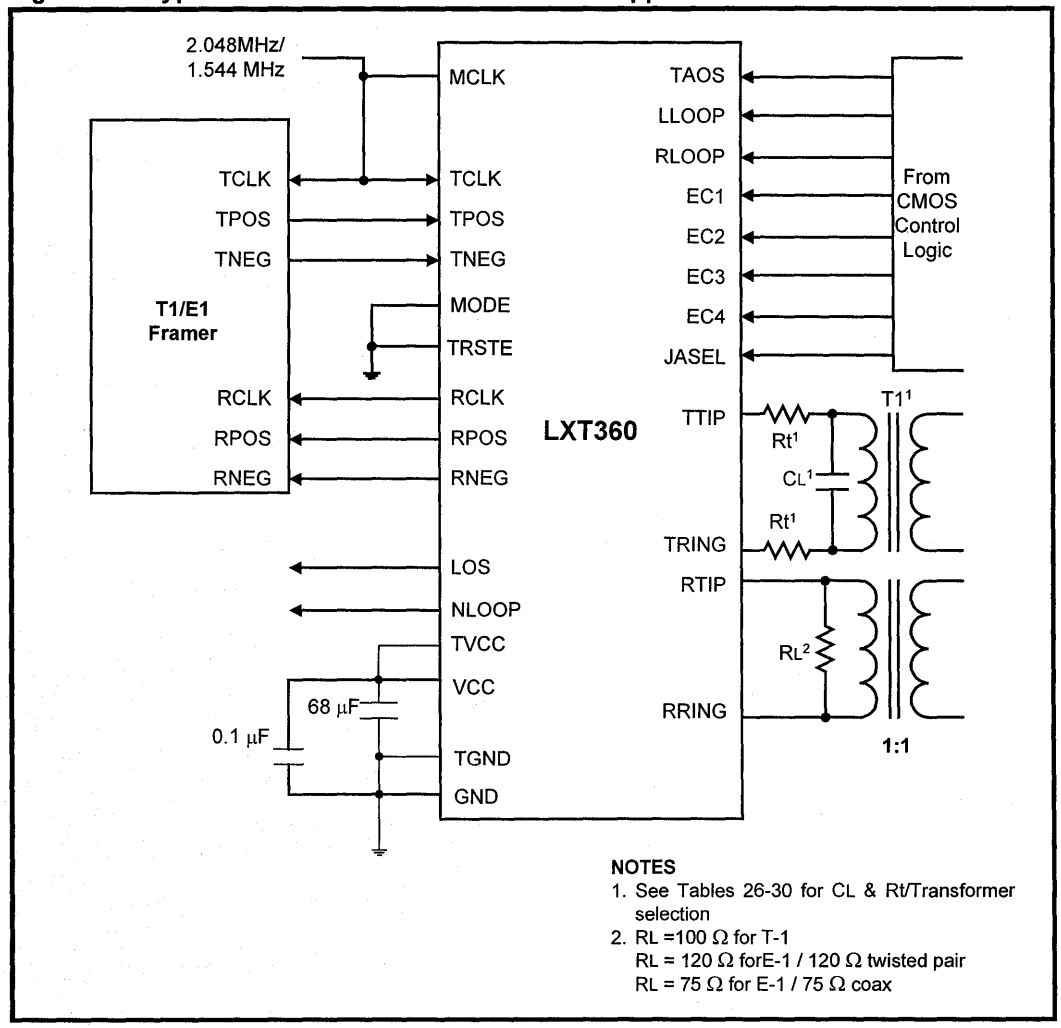
NOTE

Figure 13 shows a typical LXT360 application in either or T1 or E1 environment. See Tables 27 through 31 to select the transformers (T1 and T2), resistors (Rt and Rl) and capacitors (Cl) needed for this application.

NOTE

If the application includes surge protection, such as a varistor or sidactor on the TTIP/TRING lines, it may also require reducing the value of the capacitor C_L or eliminating it completely. Excessive capacitance at C_L will distort the transmitted signals.

Figure 13: Typical T1/E1 LXT360 Hardware Mode Application



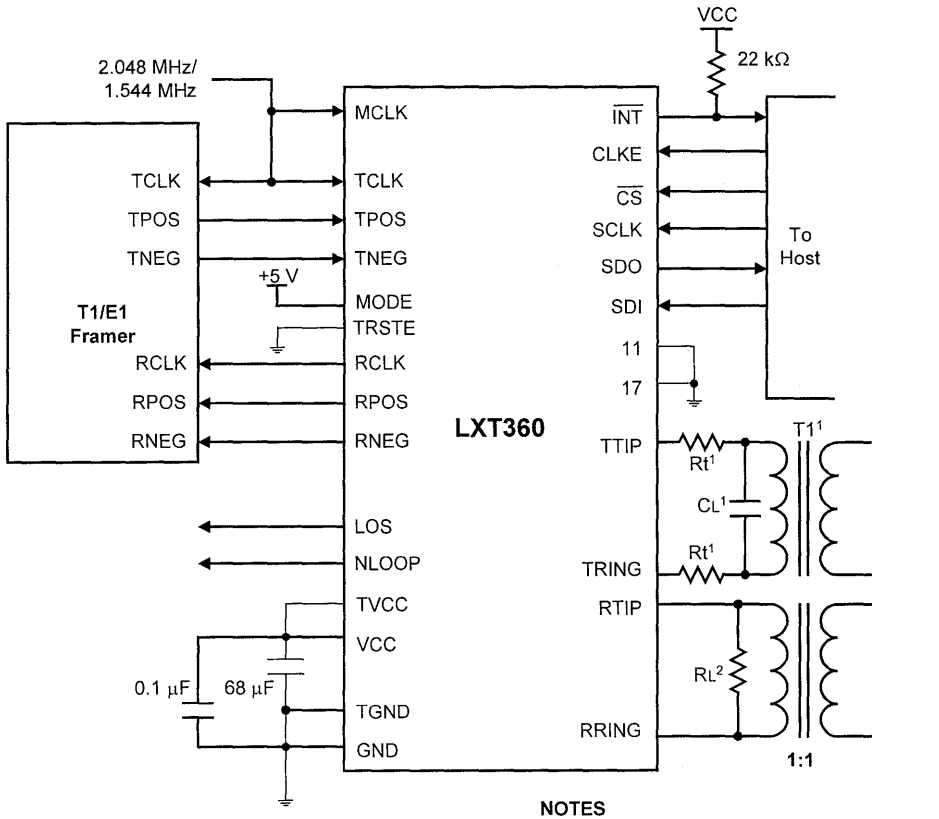
NOTE

Figure 14 shows an application using the LXT360 in its Host Controlled Mode. See Tables 27 through 31 to select the transformers (T1 and T2), resistors (Rt and RI) and capacitors (CI) needed for this application.

NOTE

If the application includes surge protection, such as a varistor or sidactor on the TTIP/TRING lines, it may also require reducing the value of the capacitor CL or eliminating it completely. Excessive capacitance at CL will distort the transmitted signals.

Figure 14: Typical T1/E1 LXT360 Host Mode Application



NOTES

1. See Tables 26-30 for CL & Rt/Transformer selection
2. RL =100 Ω for T-1
   RL = 120 Ω forE-1 / 120 Ω twisted pair
   RL = 75 Ω for E-1 / 75 Ω coax

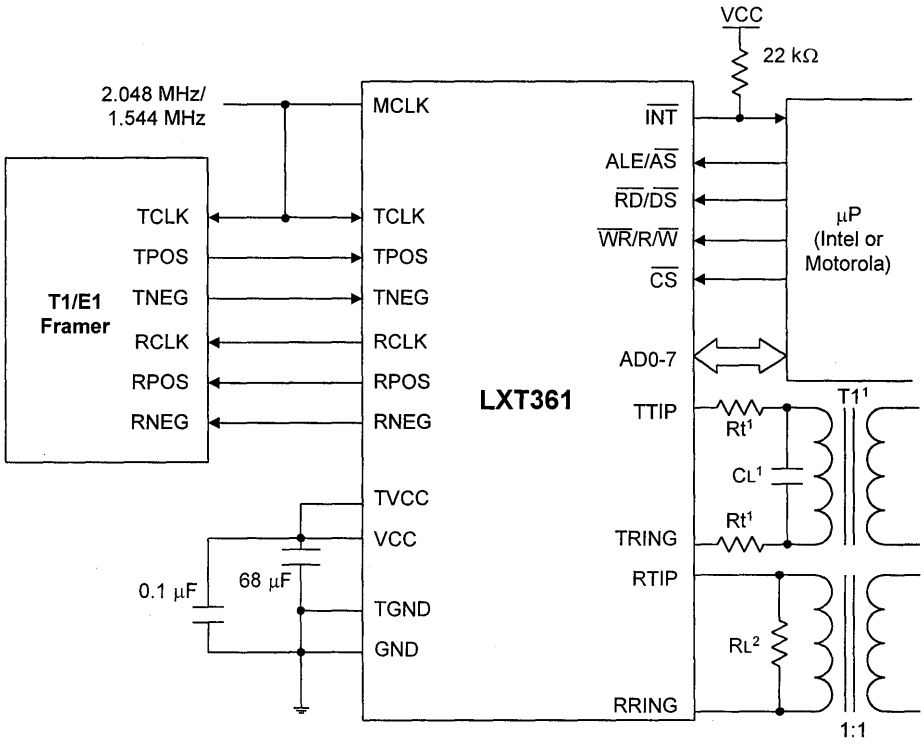
NOTE

Figure 15 shows an application using the LXT361. See Tables 27 through 31 to select the transformers (T1 and T2), resistors (Rt and Rl) and capacitors (Cl) needed for this application.

NOTE

If the application includes surge protection, such as a varistor or sidactor on the TTIP/TRING lines, it may also require reducing the value of the capacitor CL or eliminating it completely.

Figure 15: Typical T1/E1 LXT361 Application



NOTES

1. See Tables 26-30 for CL & Rt/Transformer selection
2. RL =100 Ω for T-1
   RL = 120 Ω forE-1 / 120 Ω twisted pair
   RL = 75 Ω for E-1 / 75 Ω coax

TEST SPECIFICATIONS

NOTE

The minimum and maximum values in Tables 33 to 45 and Figures 16 through 26 represent the performance specifications of the LXT360 and LXT361 and are guaranteed by test, except where noted by design.

Table 33: Absolute Maximum Ratings

Parameter	Sym	Min	Max	Units
DC supply (reference to GND)	VCC, TVCC	–	6.0	V
Input voltage, any pin [1]	VIN	GND -0.3 V	VCC + 0.3 V	V
Input current, any pin [2]	IIN	- 10	10	mA
Storage Temperature	TSTG	-65	150	° C

CAUTION
Operation at these limits may permanently damage the device.
Normal operation at these extremes not guaranteed.

1. TVCC and VCC must not differ by more than 0.3 V during operation. TGND and GND must not differ by more than 0.3 V during operation.
2. Transient currents of up to 100 mA will not cause SCR latch-up. TTIP, TRING, TVCC, and TGND can withstand continuous currents of up to 100 mA.

Table 34: Operating Conditions/Characteristics

Parameter			Sym	Min	Typ[1]	Max	Units	Test Conditions
DC Supply [2]			VCC, TVCC	4.75	5.0	5.25	V	
Ambient operating temperature			TA	-40	–	85	° C	
Total Power Dissipation[3]	T1	Short Haul	PD	–	310	380	mW	100% mark density
			PD	–	225	295	mW	50% mark density
		Long Haul	PD	–	245	325	mW	100% mark density
			PD	–	195	265	mW	50% mark density
	E1	Short Haul/ Long Haul	PD	–	275	330	mW	100% mark density
			PD	–	215	270	mW	50% mark density

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. TVCC and VCC must not differ by more than 0.3 V.
3. Power dissipation while driving 75 Ω load over operating range for T1 operation or 60 Ω load for E1 operation. Includes power dissipation on device and load. Digital levels are within 10% of the supply rails and digital outputs driving a 50 pF capacitive load.

Table 35: LXT360 Digital Characteristics *(Ta = -40 to 85 °C, V+ = 5.0 V ± 5%, GND = 0 V)*

Parameter		Sym	Min	Typ	Max	Units	Test Conditions
High level input voltage [1,2] (pins 1-4, 17, 23-25)[4]		VIH	2.0	–	–	V	
Low level input voltage [1,2] (pins 1-4, 17, 23-25)[4]		VIL	–	–	0.8	V	
High level output voltage [1,2] (pins 6-8, 10, 12, 23, 25)[4]		VOH	2.4	–	–	V	IOUT = 400 µA
Low level output voltage [1,2] (pins 6-8, 10, 12, 23, 25)[4]		VOL	–	–	0.4	V	IOUT = 1.6 mA
High level input voltage [3] (pins 5, 9, 11, 26-28)[4]		VIH	3.5	–	–	V	
Midrange input voltage [3] (pins 5, 9, 11, 26-28)[4]		VIM	2.3	–	2.7	V	
Low level input voltage [3] (pins 5, 9, 11, 26-28)[4]	Host Mode H/W Mode	VIL VIL	– –	– –	0.8 1.5	V V	
Input leakage current		ILL	0	–	±50	µA	
Three-state leakage current [1] (all outputs)		I3L	0	–	±10	µA	
TTIP/TRING leakage current (pins 13, 16)[4]		ITR	–	–	±1.2	mA	in Idle and Power Down

1. Functionality of pin 23 and 25 depends on mode. See Host Mode and Hardware Mode description
2. Output drivers will output CMOS logic levels into CMOS loads.
3. As an alternative to supplying 2.3 - 2.7 V to these pins, they may be left open.
4. Referenced pin numbers are for the NE and PE packages only. Refer to the diagram on page 2 for the appropriate LXT360QE pin assignments.

Table 36: LXT361 Digital Characteristics *(Ta = -40 to 85 °C, V+ = 5.0 V ± 5%, GND = 0 V)*

Parameter	Sym	Min	Typ	Max	Units	Test Conditions
High level input voltage [1,2] (pins 1-5, 9-12, 17, 23-28)[3]	VIH	2.0	–	–	V	
Low level input voltage [1,2] (pins 1-5, 9-12, 17, 23-28)[3]	VIL	–	–	0.8	V	
High level output voltage [1,2] (pins 6-8, 10, 11,23, 28)[3]	VOH	2.4	–	–	V	IOUT = 400 µA
Low level output voltage [1,2] (pins 6-8, 10, 11,23, 28)[3]	VOL	–	–	0.4	V	IOUT = 1.6 mA
Input leakage current	ILL	–	–	±50	µA	

1. Functionality of pins 23 and 25 depends on mode. See Host Mode description.
2. Output drivers will output CMOS logic levels into CMOS loads.
3. Referenced pin numbers are for the NE and PE packages only. Refer to the diagram on page 2 for the appropriate LXT360QE pin assignments.

Table 37: Analog Characteristics *(Ta = -40 to 85 °C, V+ = 5.0 V ± 5%, GND = 0 V)*

Parameter		Min	Typ[1]	Max	Units	Test Conditions
Recommended output load on TTIP/TRING		50	–	200	Ω	
AMI Output Pulse Amplitudes	DSX-1, DS1	2.4	3.0	3.6	V	RL = 100 Ω
	CEPT (ITU)	2.7	3.0	3.3	V	RL = 120 Ω
Jitter added by the transmitter[2]	10 Hz - 8 kHz [3]	–	–	0.02	UI	
	8 kHz - 40 kHz [3]	–	–	0.025	UI	
	10 Hz - 40 kHz[3]	–	–	0.025	UI	
	Broad Band	–	–	0.05	UI	
Receiver sensitivity @ 772 kHz (T1)	Mode 1 (EC1 = 1) (T1 Long-Haul)	0	–	26	dB	See Table 12 for Gain Setting
	Mode 2 (EC1 = 0) (T1 Long-Haul)	0	–	36	dB	
	Mode 3 (EC4 = 1) (T1 Short-Haul)	0	–	13.6	dB	
Receiver Sensitivity @ 1024 kHz (E1 line loss)	Mode 1 (EC4-1 = 1000) (E1 Short-Haul/12 dB)	0	–	13.6	dB	
	Mode 2 (EC4-1 = 1001 or EC4-1 = 1010) (E1 Long-Haul/43 dB)	0	–	43	dB	
Allowable consecutive zeros before LOS (T1)		160	175	190	–	
Allowable consecutive zeros before LOS (E1)		–	32	–	–	
Input jitter tolerance (T1)	10 kHz - 100 kHz	0.4	–	–	UI	0 dB line AT&T Pub 62411
	1 Hz [3]	138	–	–	UI	
Input jitter tolerance (E1)	10 kHz - 100 kHz	0.2	–	–	UI	0 dB line ITU (G.823)
	1 Hz [3]	37	–	–	UI	
Jitter attenuation curve corner frequency [4]		–	3	–	Hz	selectable in data port
Receive Return Loss (E1)	51 kHz - 102 kHz	–	22	–	dB	
	102 kHz - 2.048 MHz	–	28	–	dB	
	2.048 MHz - 3.072 MHz	–	30	–	dB	

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Input signal to TCLK is jitter-free. The Jitter Attenuator is in the receive path or disabled.
3. Guaranteed by characterization; not subject to production testing.
4. Circuit attenuates jitter at 20 dB/decade above the corner frequency.

Figure 16: 2.048 MHz E1 Pulse *(See Table 38)*

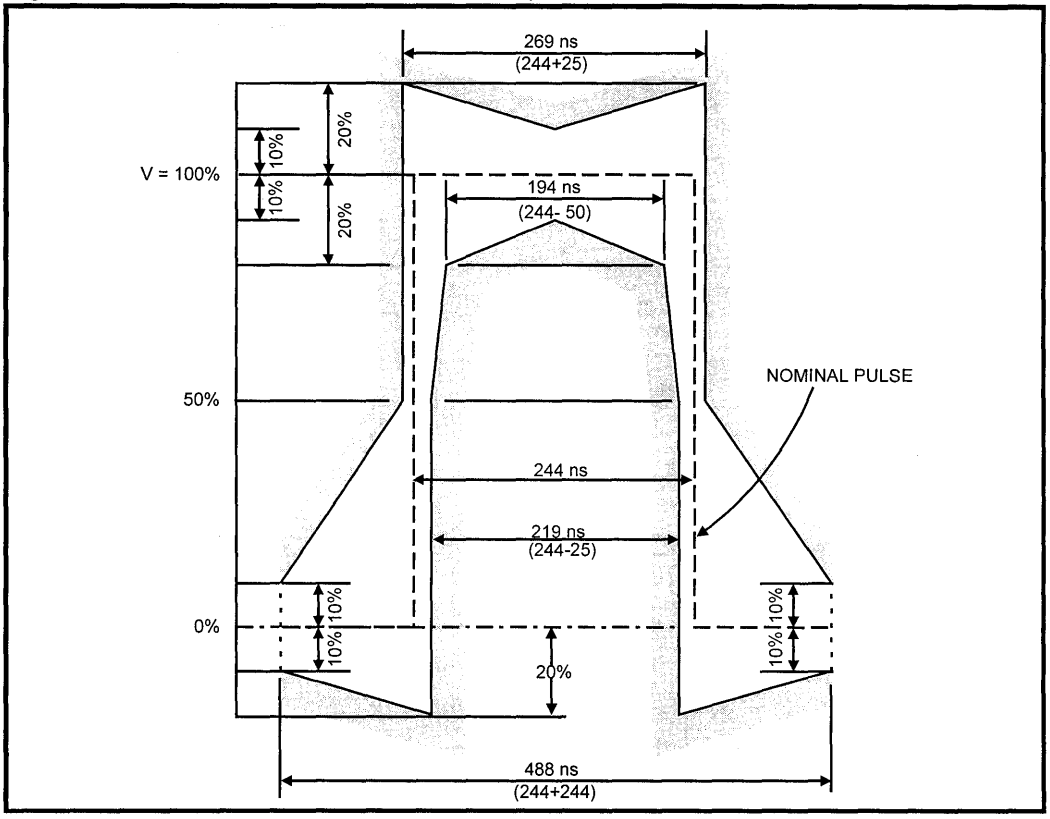


Table 38: 2.048 MHz E1 Pulse Mask Specifications

Parameter	TWP	Coax	Unit
Test load impedance	120	75	Ω
Nominal peak mark voltage	3.0	2.37	V
Nominal peak space voltage	0 ±0.30	0 ±0.237	V
Nominal pulse width	244	244	ns
Ratio of positive and negative pulse amplitudes at center of pulse	95-105	95-105	%
Ratio of positive and negative pulse amplitudes at nominal half amplitude	95-105	95-105	%

Figure 17: 1.544 MHz T1 Pulse (DS1 and DSX-1) *(See Table 39)*

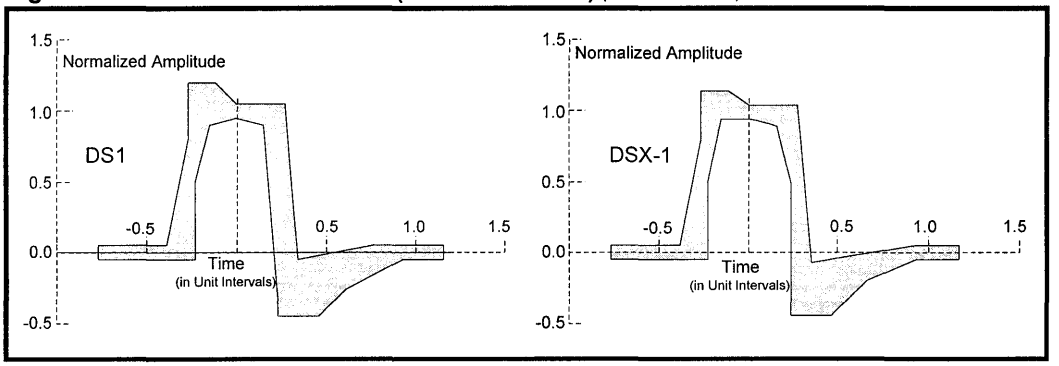


Table 39: 1.544 MHz T1 Pulse Mask Corner Point Specifications

DS1 Template *(per ANSI T1. 403-1995)*				**DSX-1 Template** *(per ANSI T1. 102-1993)*			
Minimum Curve		**Maximum Curve**		**Minimum Curve**		**Maximum Curve**	
Time *(UI)*	**Amplitude**	**Time** *(UI)*	**Amplitude**	**Time** *(UI)*	**Amplitude**	**Time** *(UI)*	**Amplitude**
-0.77	-0.05	-0.77	0.05	-0.77	-0.05	-0.77	0.05
-0.23	-0.05	-0.39	0.05	-0.23	-0.05	-0.39	0.05
-0.23	0.50	-0.27	0.80	-0.23	0.50	-0.27	0.80
-0.15	0.90	-0.27	1.20	-0.15	0.95	-0.27	1.15
0.0	0.95	-0.12	1.20	0.0	0.95	-0.12	1.15
0.15	0.90	0.0	1.05	0.15	0.90	0.0	1.05
0.23	0.50	0.27	1.05	0.23	0.50	0.27	1.05
0.23	-0.45	0.34	-0.05	0.23	-0.45	0.35	-0.07
0.46	-0.45	0.77	0.05	0.46	-0.45	0.93	0.05
0.61	-0.26	1.16	0.05	0.66	-0.20	1.16	0.05
0.93	-0.05			0.93	-0.05		
1.16	-0.05			1.16	-0.05		

Table 40: Master and Transmit Clock Timing Characteristics (T1 Operation) *(Figure 18)*

Parameter	Sym	Min	Typ[1]	Max	Units	Notes
Master clock frequency	MCLK	–	1.544	–	MHz	must be supplied
Master clock tolerance	MCLKt	–	±32	–	ppm	
Master clock duty cycle	MCLKd	40	–	60	%	
Transmit clock frequency	TCLK	–	1.544	–	MHz	
Transmit clock tolerance	TCLKt	–	–	±100	ppm	
Transmit clock duty cycle	TCLKd	10	–	90	%	
TPOS/TNEG to TCLK setup time	tSUT	50	–	–	ns	
TCLK to TPOS/TNEG hold time	tHT	50	–	–	ns	

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 41: Master and Transmit Clock Timing Characteristics (E1 Operation) *(Figure 18)*

Parameter	Sym	Min	Typ[1]	Max	Units	Notes
Master clock frequency	MCLK	–	2.048	–	MHz	must be supplied
Master clock tolerance	MCLKt	–	±32	–	ppm	
Master clock duty cycle	MCLKd	40	–	60	%	
Transmit clock frequency	TCLK	–	2.048	–	MHz	
Transmit clock tolerance	TCLKt	–	–	±100	ppm	
Transmit clock duty cycle	TCLKd	10	–	90	%	
TPOS/TNEG to TCLK setup time	tSUT	50	–	–	ns	
TCLK to TPOS/TNEG hold time	tHT	50	–	–	ns	

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 18: Transmit Clock Timing

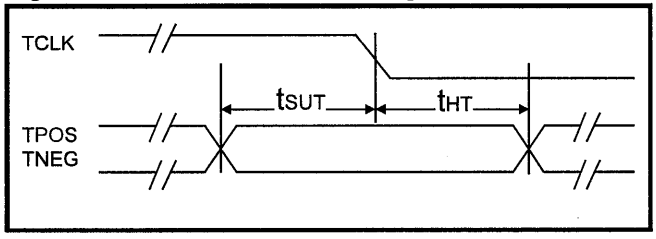


Table 42: Receive Timing Characteristics for T1 Operation *(See Figure 19)*

Parameter	Sym	Min	Typ[1]	Max	Units
Receive clock duty cycle [2, 3]	RLCKd	40	50	60	%
Receive clock pulse width [2, 3]	tPW	–	648	–	ns
Receive clock pulse width high	tPWH	–	324	–	ns
Receive clock pulse width low[1,3]	tPWL	260	324	388	ns
RPOS/RNEG to RCLK rising time	tSUR	–	274	–	ns
RCLK rising to RPOS/RNEG hold time	tHR	–	274	–	ns

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. RCLK duty cycle widths will vary according to extent of received pulse jitter displacement. Max and Min RCLK duty cycles are for worst case jitter conditions.
3. Worst case conditions guaranteed by design only.

Table 43: Receive Timing Characteristics for E1 Operation *(See Figure 19)*

Parameter	Sym	Min	Typ[1]	Max	Units
Receive clock duty cycle [2, 3]	RLCKd	40	50	60	%
Receive clock pulse width [2, 3]	tPW	–	488	–	ns
Receive clock pulse width high	tPWH	–	244	–	ns
Receive clock pulse width low[1,3]	tPWL	195	244	293	ns
RPOS/RNEG to RCLK rising time	tSUR	–	194	–	ns
RCLK rising to RPOS/RNEG hold time	tHR	–	194	–	ns

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. RCLK duty cycle widths will vary according to extent of received pulse jitter displacement. Max and Min RCLK duty cycles are for worst case jitter conditions (0.4 UI clock displacement for 1.544 MHz.)
3. Worst case conditions guaranteed by design only.

Figure 19: Receive Clock Timing

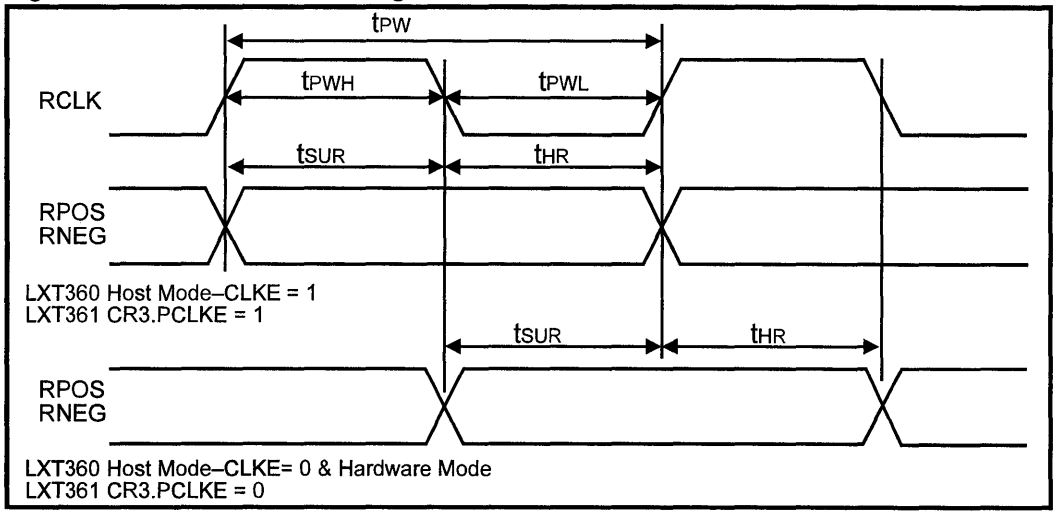


Table 44: LXT360 Serial I/O Timing Characteristics *(See Figures 20 and 21)*

Parameter	Sym	Min	Typ[1]	Max	Units	Parameter
Rise/fall time—any digital output	tRF	–	–	100	ns	Load 1.6 mA, 50 pF
SDI to SCLK setup time	tDC	50	–	–	ns	
SCLK to SDI hold time	tCDH	50	–	–	ns	
SCLK low time	tCL	240	–	–	ns	
SCLK high time	tCH	240	–	–	ns	
SCLK rise and fall time	tR, tF	–	–	50	ns	
$\overline{CS}$ falling edge to SCLK rising edge	tCC	50	–	–	ns	
Last SCLK edge to $\overline{CS}$ rising edge	tCCH	50	–	–	ns	
$\overline{CS}$ inactive time	tCWH	250	–	–	ns	
SCLK to SDO valid time	tCDV	–	–	200	ns	
SCLK falling edge or $\overline{CS}$ rising edge to SDO high-Z	tCDZ	–	100	–	ns	

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 20: LXT360 Serial Data Input Timing Diagram

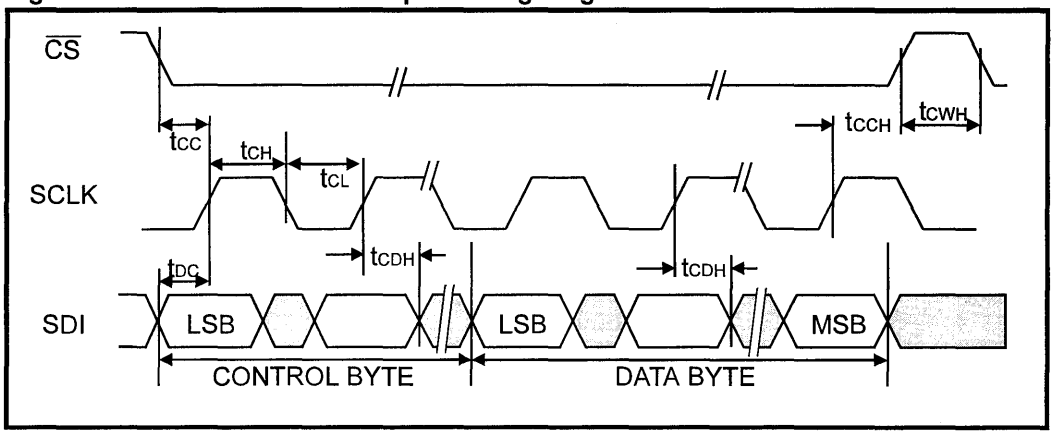


Figure 21: LXT360 Serial Data Output Timing Diagram

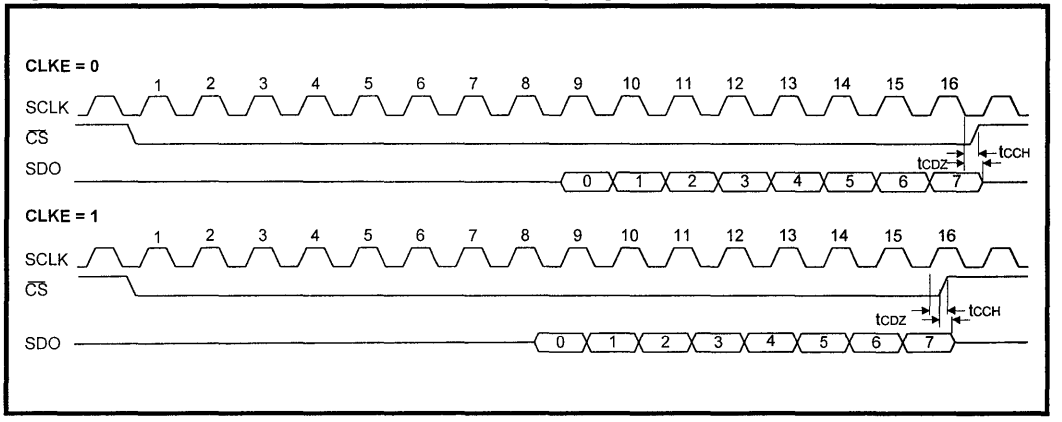


Table 45: LXT361 20 MHz Intel Bus Parallel I/O Timing Characteristics *(See Figure 22)*

Parameter	Sym	Min	Max	Units	Test Conditions
ALE pulse width	TLHLL	35	–	ns	
Address valid to ALE falling edge	TAVLL	10	–	ns	
ALE falling edge to address hold time	TLLAX	10	–	ns	
ALE falling edge to $\overline{RD}$ falling edge	TLLRL	10	–	ns	
ALE falling edge to $\overline{WR}$ falling edge	TLLWL	10	–	ns	
$\overline{CS}$ falling edge to $\overline{RD}$ falling edge	TCLRL	10	–	ns	
$\overline{CS}$ falling edge to $\overline{WR}$ falling edge	TCLWL	10	–	ns	
$\overline{RD}$ low pulse width	TRLRH	95	–	ns	
$\overline{RD}$ falling edge to data valid	TRLDV	10	55	ns	
Data hold time after $\overline{RD}$ rising edge	TRHDX	5	35	ns	
$\overline{RD}$ rising edge to ALE rising edge	TRHLH	15	–	ns	
$\overline{RD}$ rising edge to address valid	TRHAV	35	–	ns	
$\overline{CS}$ low hold time after $\overline{RD}$ rising edge	TRHCH	0	–	ns	
$\overline{WR}$ low pulse width	TWLWH	95	–	ns	
Data setup time before $\overline{WR}$ rising edge	TDVWH	40	–	ns	
Data hold time after $\overline{WR}$ rising edge	TWHDX	30	–	ns	
$\overline{WR}$ rising edge to ALE rising edge	TWHLH	15	–	ns	
$\overline{CS}$ low hold time after $\overline{WR}$ rising edge	TWHCH	15	–	ns	

Figure 22: LXT361 I/O Timing Diagram for Intel Address/Data Bus

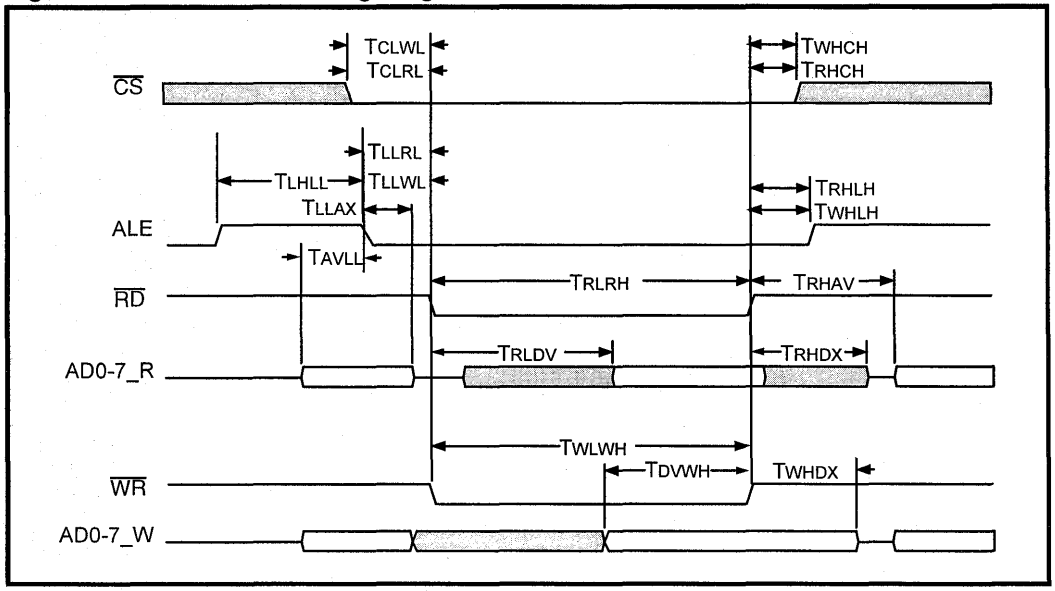


Table 46: LXT361 16.78 MHz Motorola Bus Parallel I/O Timing Characteristics

(See Figure 23)

Parameter	Symbol	Min	Max	Units	Test Conditions
$\overline{DS}$ rising edge to $\overline{AS}$ rising edge	TDSHASH	15	–	ns	
$\overline{AS}$ high pulse width	TASHASL	35	–	ns	
Address valid setup time at $\overline{AS}$ falling edge	TAVASL	10	–	ns	
$\overline{AS}$ falling edge to Address valid hold time	TASLAX	10	–	ns	
$\overline{AS}$ falling edge to $\overline{DS}$ falling edge	TASLDSL	20	–	ns	
$\overline{CS}$ falling edge to $\overline{DS}$ falling edge	TCSLDSL	10	–	ns	
$\overline{DS}$ low pulse width	TDSLDSH	95	–	ns	
$\overline{DS}$ falling edge to data valid	TDSLDV	10	55	ns	
Data hold time after $\overline{DS}$ rising edge	TDSHDX	5	35	ns	
R/$\overline{W}$ falling edge to $\overline{DS}$ falling edge	TRWLDSL	10	–	ns	
Data setup time before $\overline{DS}$ rising edge	TDVDSH	40	–	ns	
Data hold time after $\overline{DS}$ rising edge	TDXDSH	30	–	ns	
R/$\overline{W}$ low hold time after $\overline{DS}$ rising edge	TDSHRWH	15	–	ns	
$\overline{CS}$ low hold time after $\overline{DS}$ rising edge	TDSHCSH	15	–	ns	

Figure 23: LXT361 I/O Timing Diagram for Motorola Address/Data Bus

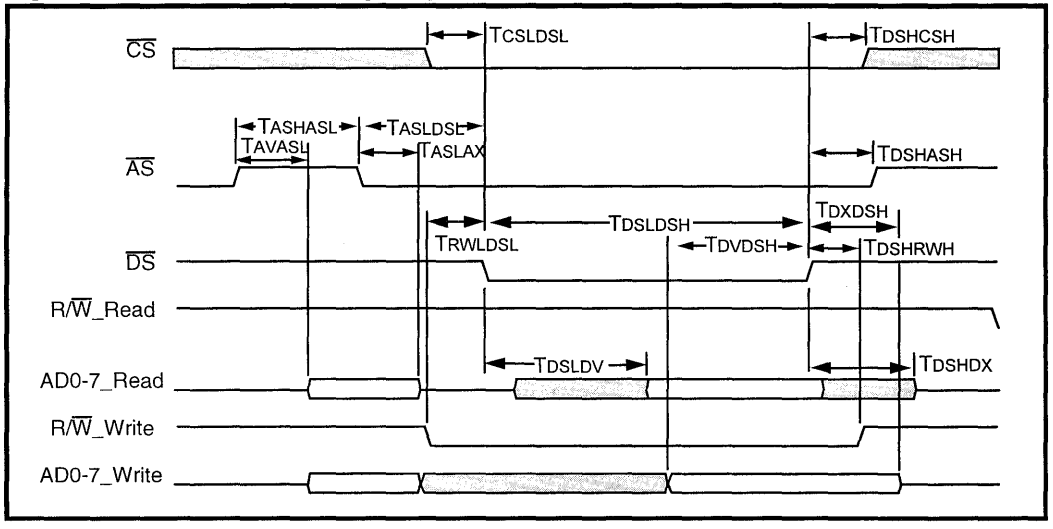


Figure 24: Jitter Tolerance *(Typical)*

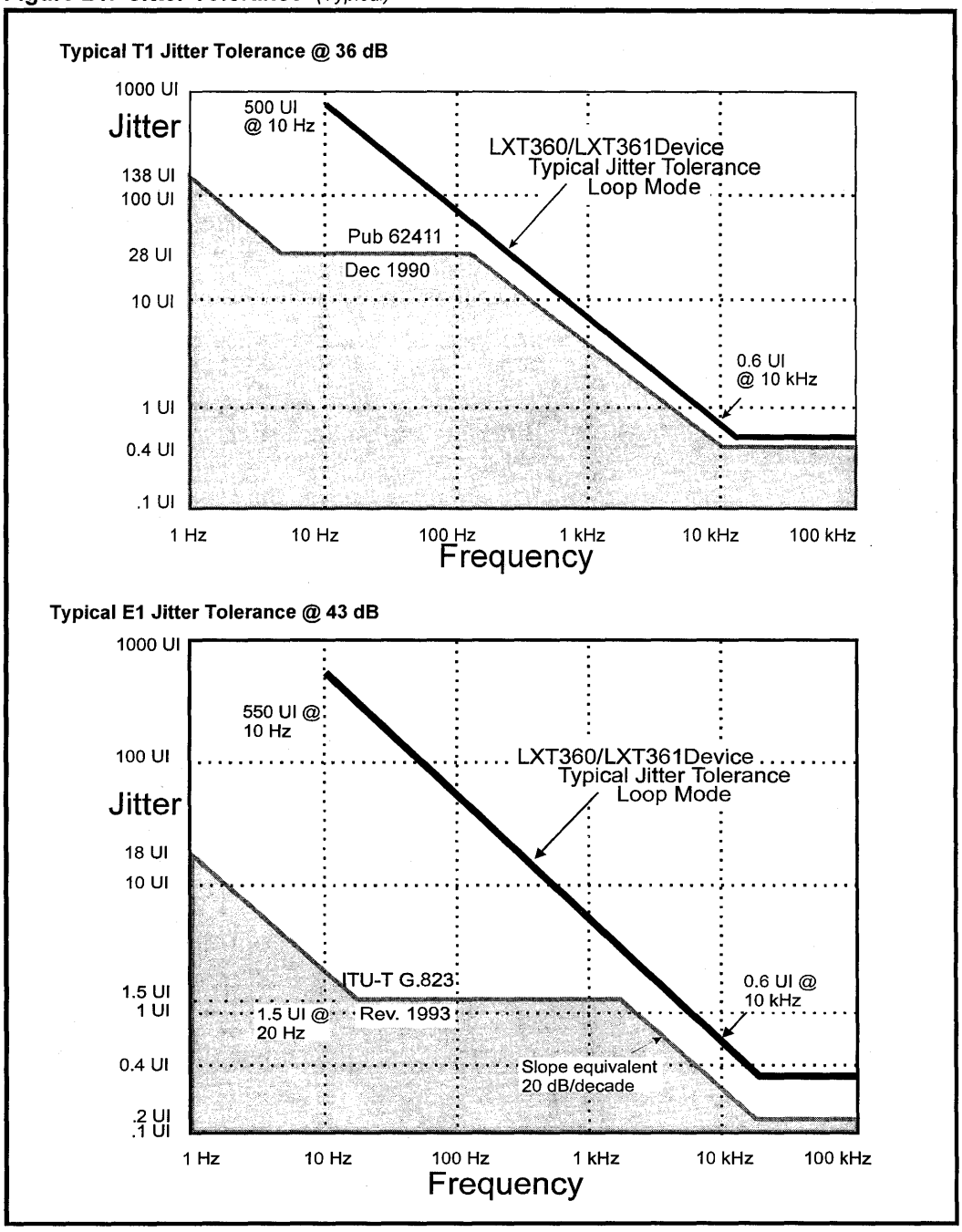


Figure 25: E1 Jitter Attenuation *(Typical)*

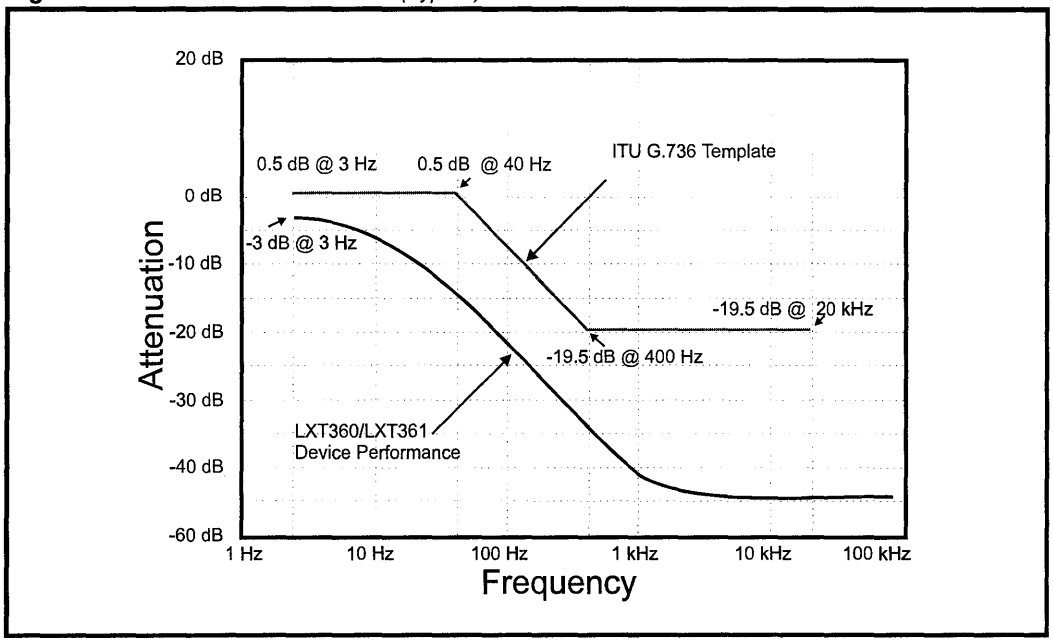
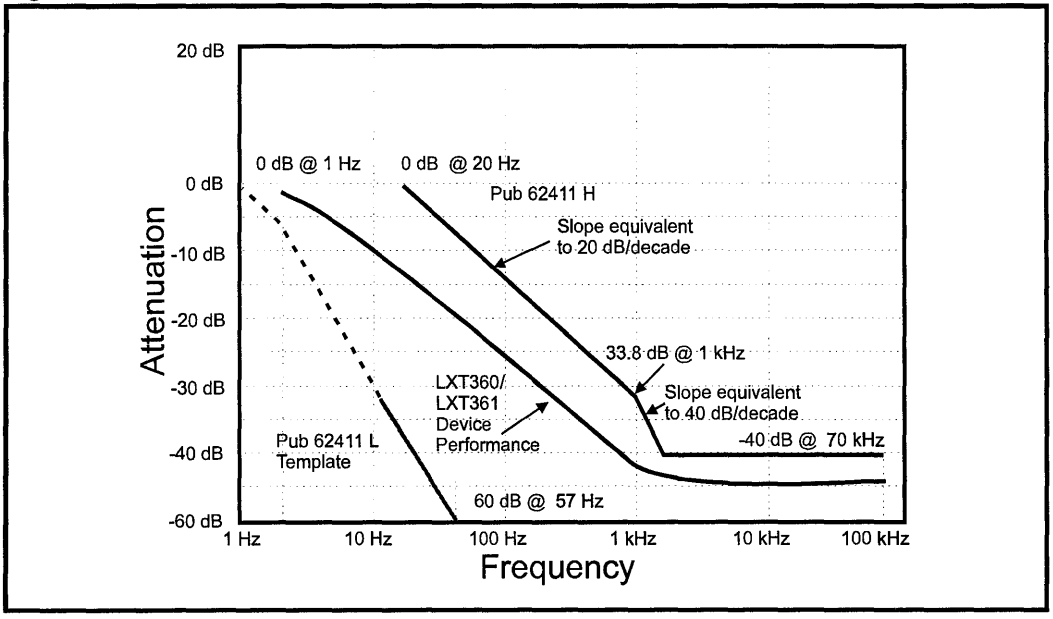


Figure 26: T1 Jitter Attenuation *(Typical)*



NOTES

T1/E1 Repeaters

DATA SHEET

APRIL 1997
Revision 2.1

LXT312 / LXT315

Low Power T1 PCM Repeaters / Transceivers

4

General Description

The LXT312 and LXT315 are integrated repeater/transceiver circuits for T1 carrier systems. The LXT312 is a dual repeater/transceiver and the LXT315 is a single repeater/transceiver. The LXT312 and LXT315 are designed to operate as regenerative repeaters/transceivers for 1.544 Mbps data rate PCM lines. Each includes all circuits required for a regenerative repeater/transceiver system including the equalization network, automatic line build-out (ALBO), and a state-of-the-art analog/digital clock extraction network tuned by an external crystal.

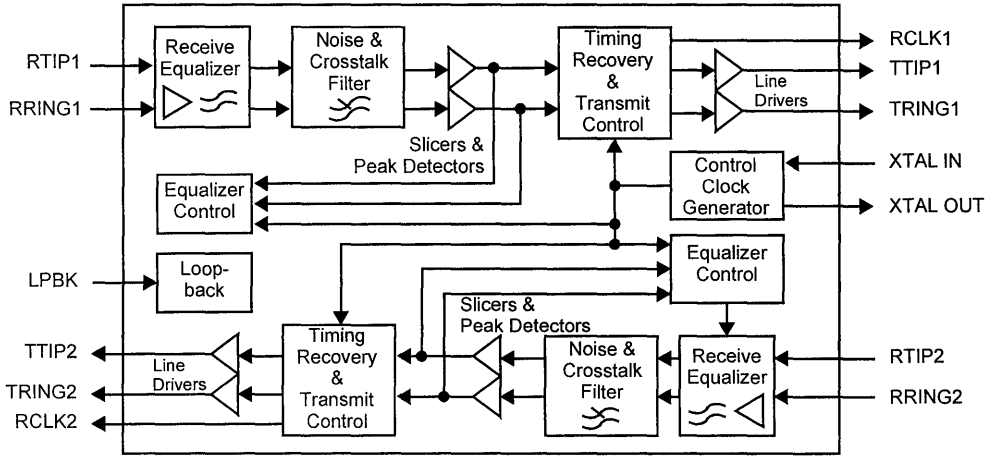
The key feature of the LXT312 family is that it requires only a crystal and a minimum of other components to complete a repeater/transceiver design. Compared with traditional tuned coil-type repeaters/transceivers, they offer significant savings in component and labor costs, along with reduced voltage drop/power consumption, and improved reliability. To ensure performance for all loop lengths, the LXT312 and LXT315 are 100% AC/DC tested using inputs generated by Level One's proprietary transmission line and network simulator.

The LXT312 and LXT315 are advanced CMOS devices which require only a single 5-volt power supply.

Features

- Integrated repeater/transceiver circuit on a single CMOS chip
- On-chip equalization network
- On-chip ALBO
- Low power consumption
- No tuning coil
- On-chip Loopback
- Recovered Clock Output
- 0 to 36 dB dynamic range
- -11 dB interference margin
- Compatible with CB113/TA24 specifications
- Single 5 V only CMOS technology
- Available in 16-pin PDIP and 44-pin PLCC

LXT312 / LXT315 Block Diagram



PIN ASSIGNMENTS AND SIGNAL DESCRIPTIONS

Figure 1: LXT312 / LXT315 Pin Assignments

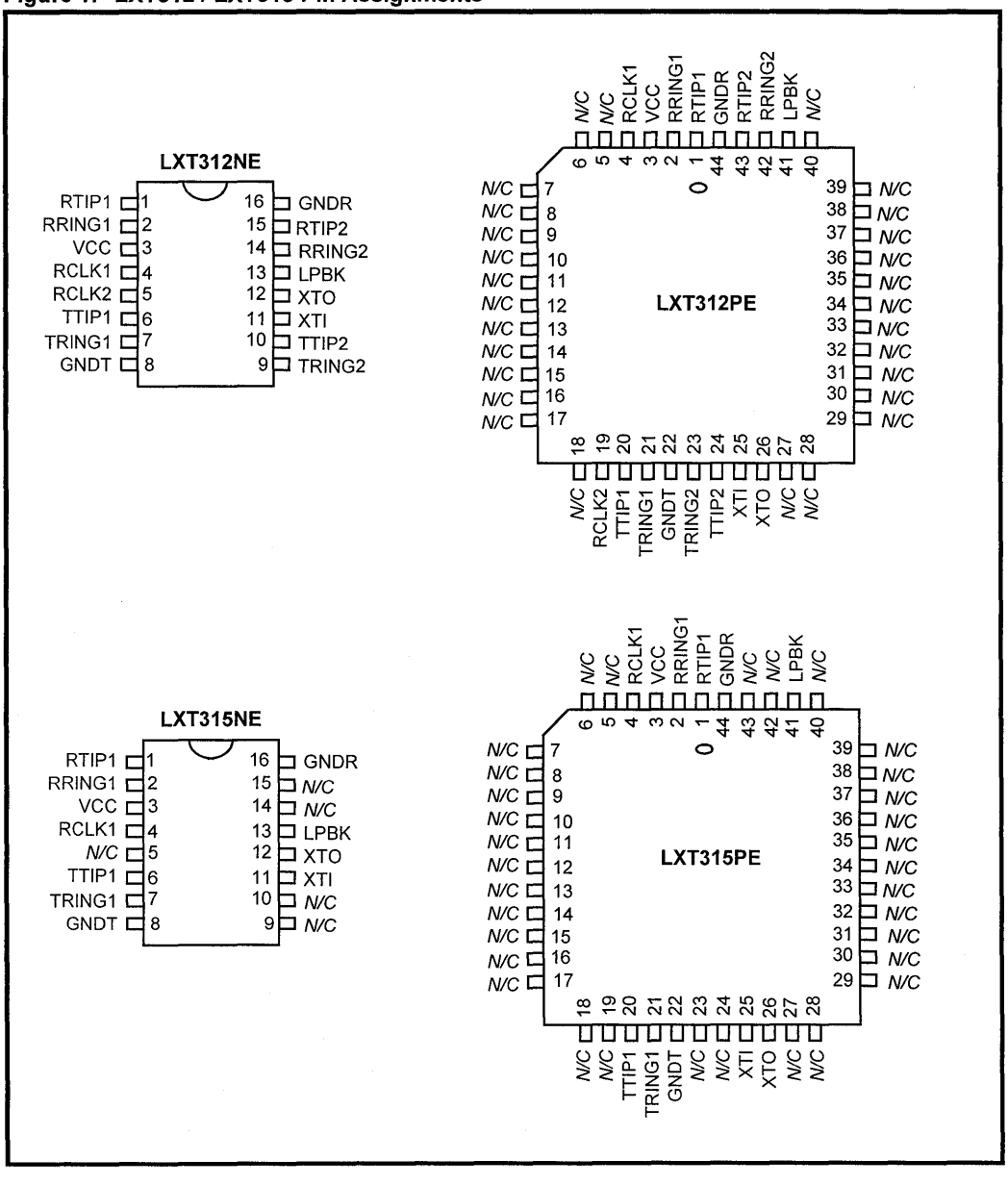


Table 1: LXT 312 / LXT315 Signal Descriptions

Pin #		Symbol	I/O	Description
PDIP	PLCC			
1 2	1 2	RTIP1 RRING1	I I	**Repeater Tip and Ring Inputs.** Tip and ring receive inputs for Channel 1.
4	4	RCLK1	O	**Recovered Clock.** Clock output recovered from Channel 1 receive input.
6 7	20 21	TTIP1 TRING1	O O	**Repeater Tip and Ring Outputs.** Open-drain output drivers for Channel 1.
11 12	25 26	XTI XTO	I O	**Crystal Oscillator Pins.** A 6.176 MHz crystal must be connected across these two pins.
3	3	VCC	–	**Power Supply.** Power supply input for all circuits. +5 V (±0.25 V).
8	22	GNDT	–	**Transmit Ground.** Ground return for transmit circuits.
16	44	GNDR	–	**Receive Ground.** Ground return for receive circuits.
9[1] 10[1]	23[1] 24[1]	TRING2 TTIP2	O O	**Side 2 Ring and Tip Outputs.** On the LXT312 dual repeater/transceiver, these are open-drain output drivers for Channel 2.
14[1] 15[1]	42[1] 43[1]	RRING2 RTIP2	I I	**Side 2 Ring and Tip Inputs.** On the LXT312 repeater/transceiver, these are tip and ring receive inputs for Channel 2.
5[1]	19[1]	RCLK2	O	**Recovered Clock.** On the LXT312 dual repeater/transceiver, this is the recovered clock output for Channel 2.
13	41	LPBK	I	**Loopback Control.** On the LXT312, this pin controls Loopback Selection: High = Loopback side 1 data to side 2. Low = No Loopback. ***On LXT315 single repeater/transceiver, this pin must be connected to GND.***

1. On the LXT315NE and LXT315PE single repeater/transceiver, these pins are not connected (N/C).
2. On the LXT312PE and LXT315PE, pins 5 through 18 and 27 through 40 are not connected (N/C).

FUNCTIONAL DESCRIPTION

Introduction

PCM signals are attenuated and dispersed in time as they travel down a transmission line. Repeaters/transceivers are required to amplify, reshape, regenerate and retime the PCM signal, then retransmit it.

The LXT312 and LXT315 each contain all the circuits required to build a complete PCM repeater/transceiver. The operational range of the repeaters/transceivers is 0 to 36 dB of cable loss at 772 kHz (equal to 6300 feet of 22 gauge pulp-insulated cable between repeaters).

Receive Function

The signal is received through a 1:1 transformer at RTIP and RRING and equalized for up to 36 dB of cable loss. The receive equalizer uses a proprietary on-chip adaptive filter technique which is equivalent to a 3-port ALBO equalizer design. The monolithic structure of the filter and the absence of external components provide excellent ISI and dispersion elimination, and accurate data transfer over temperature.

Receiver noise immunity is optimized by a proprietary crosstalk elimination filter which eliminates the unneeded high-frequency components of the received signal.

Timing Recovery Function

The equalized signal is full wave rectified and used to generate information for the timing recovery circuit. This circuit uses a mixed analog/digital technique to provide a low-jitter PLL similar to a tuned tank with excellent jitter tracking ability. But unlike a tuned tank, the free running frequency of the PLL clock is accurately controlled by the external reference crystal. No adjustment is required. Refer to Application Information for crystal specifications.

Recovered clock signals are available on the RCLK pins for applications that require synchronization to the bit stream.

Transmit Function

Recovered data is re-synchronized to the recovered clock signal by the timing recovery and transmit control section. The data is then retransmitted to the network via two open-drain, high-voltage transistors.

Loopback Function (LXT312 Only)

The LXT312 includes a loopback function for network diagnostics. With the LPBK pin Low, the repeater/transceiver operates in the normal mode. When the LPBK pin is pulled High, the data is looped back from side 1 to side 2.

APPLICATION INFORMATION

Introduction

Figure 2 shows a typical T1 dual repeater/transceiver application using an LXT312 repeater/transceiver with standard PCB edge connectors. It includes a jumper-selectable shorting option (dashed lines at connector pins 2 and 7) for the fault location circuitry. Table 2 lists the specifications required for the crystal used with the LXT312 or LXT315 repeater/transceiver.

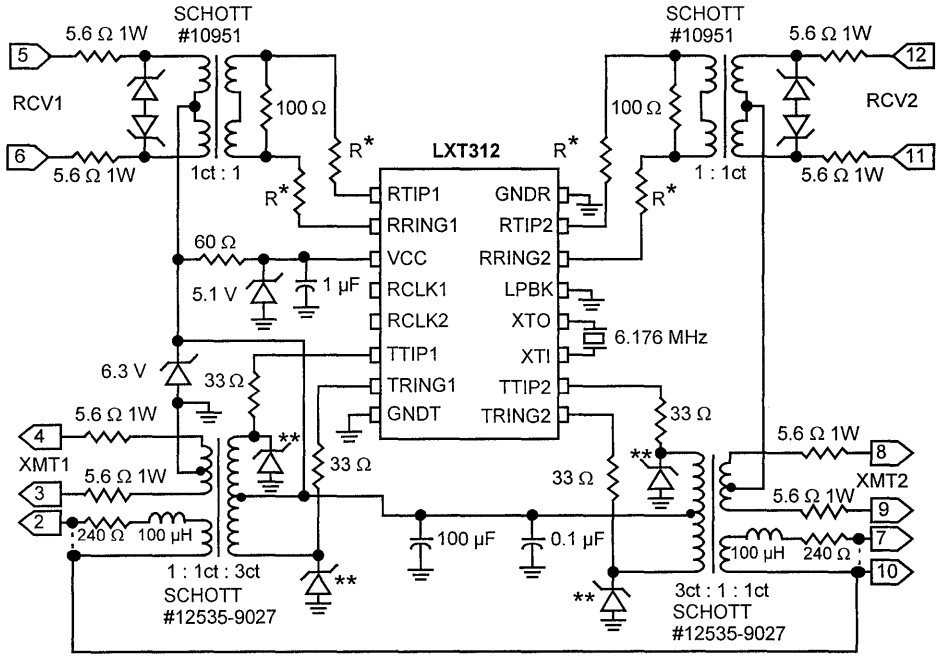
Table 2: Crystal Specifications

Parameter	Specification
Frequency	6.176 MHz
Frequency tolerance[1]	± 50 ppm
Effective series resistance	40 Ω Maximum
Crystal cut	AT
Resonance	Parallel
Maximum drive level	2.0 mW
Mode of operation	Fundamental

1. @ 25 °C, C Load = 10 pF; and from -40 °C to +85 °C (Ref 25 °C reading)

4

Figure 2: Typical T1 Dual Repeater/Transceiver Application



NOTES:

* RTIP/RRING Resistors are used to provide surge protection. Values can be 0 – 100 Ω.

** TTIP/TRING Zeners are used to reduce surge susceptibility. Values can be 12 – 14 V.

TEST SPECIFICATIONS

NOTE

Minimum and maximum values in Table 3 through Table 6 and Figure 3 through Figure 11 represent the performance specifications of the LXT312/315 repeaters/transceivers and are guaranteed by test except, as noted, by design

Table 3: Absolute Maximum Ratings

Parameter	Symbol	Units
Supply voltage (min to max)	VCC	-0.3 V to +6 V
Driver Voltage	VOH	18 V
Receiver Current	ICC	100 mA
Operating temperature (min to max)	TOP	-40 °C to +85 °C
Storage temperature (min to max)	TST	-65 °C to +150 °C

CAUTION

Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 4: Recommended Operating Conditions (Voltages are with respect to ground.)

Parameter	Symbol	Min	Typ	Max	Units
Supply voltage	VCC	4.75	5.0	5.25	V
Operating temperature	TOP	-40	—	85	° C

Table 5: Electrical Characteristics (Over Recommended Range)

Parameter		Symbol	Min	Typ[1]	Max	Units
Interference Margin		SNR	-11	–	–	dB
Receiver Dynamic Range		–	-36	–	0	dB
Digital Outputs - Low	(IOL = 1.6 mA	VOL	–	–	0.4	V
	(IOL = 10 µA)	VOL	–	0.2	–	V
Digital Outputs - High	(IOH = 0.4 mA	VOH	2.4	–	–	V
	(IOH < 10 µA)	VOH	–	4.5	–	V
Digital Inputs - High		VIH	2.0	–	–	V
Digital Inputs - Low		VIL	–	–	0.8	V
Supply Current (from VCC supply)[2]	All zeros	ICC	–	15	22	mA
	All ones	ICC	–	–	23	mA
Driver Leakage Current (VDVR = 18 V)		ILL	–	–	100	µA
Driver Pulse Amplitude (Driver output IO = 20 mA)		AP	0.65	–	0.95	V

1. Typical values are at 25° C and are for design aid only; they are not guaranteed and not subject to production testing.
2. Measured with CLOAD ≤ 10 pF, RLOAD > 100 kΩ.

Figure 3: Digital Timing Characteristics

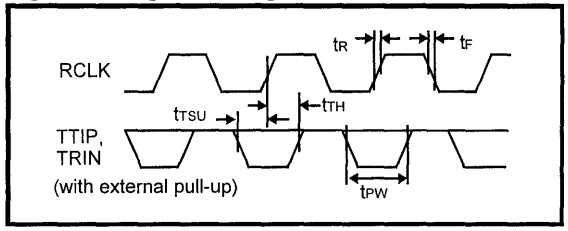


Table 6: Digital Timing Characteristics (Over Recommended Range) see Figure 3

Parameter	Symbol	Min	Typ[1]	Max	Units
Driver Pulse Width	t_{PW}	299	324	349	ns
Driver Pulse Imbalance	–	–	–	15	ns
Rise and Fall Time (any digital output[2])	t_R / t_F	–	–	18	ns
Setup Time - TTIP/TRING to RCLK	t_{TSU}	90	–	–	ns
Hold Time - TTIP/TRING from RCLK	t_{TH}	90	–	–	ns

1. Typical values are at 25° C and are for design aid only; they are not guaranteed and not subject to production testing.
2. Measured with $C_{LOAD} \leq 10$ pF, $R_{LOAD} > 100$ kΩ.

Test Setups

Introduction

Both the LXT312 and LXT315 are fully tested (100% AC and DC parameters) using inputs generated by Level One's proprietary transmission line and network simulator. Device testing includes receiver jitter tolerance, jitter transfer and interference margin, and receiver immunity to gaussian and 60 Hz noise. Specifications and bench test setups are shown in Figures 4 through 11.

Receiver Jitter Tolerance Testing

Receiver jitter tolerance meets the template shown in Figure 4, when operated at line losses from 0 to 36 dB. Figure 6 shows the setup used for jitter tolerance testing.

Receiver Jitter Transfer Testing

Receiver jitter transfer meets the template shown in Figure 5, when operated with line losses from 0 to 36 dB and input jitter amplitude of 0.15 UI peak-to-peak. Jitter gain at a given frequency is defined as the difference between intrinsic jitter and additive jitter at the measurement frequency, divided by the amplitude of the input jitter. Figure 7 shows the setup used for jitter transfer testing.

Figure 4: Receiver Jitter Tolerance Template

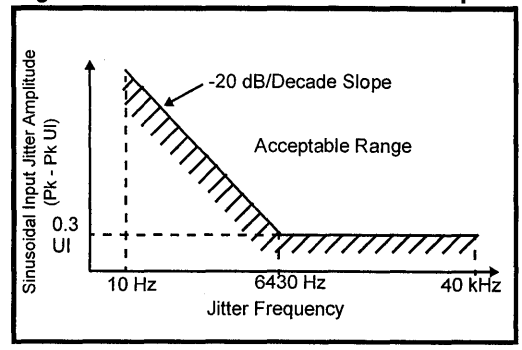


Figure 5: Receiver Jitter Transfer Template

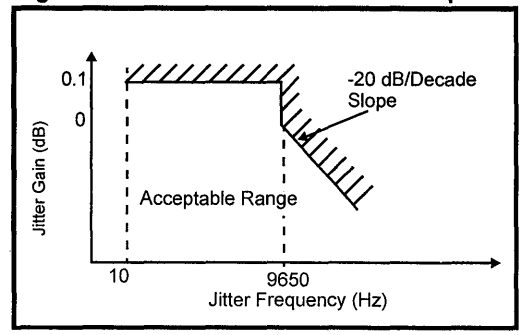


Figure 6: Receiver Jitter Tolerance Test Setup

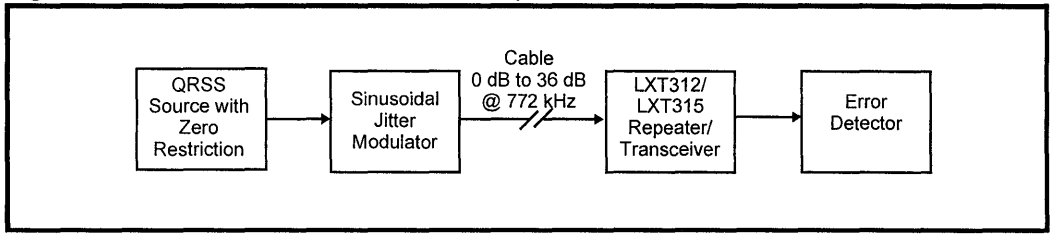
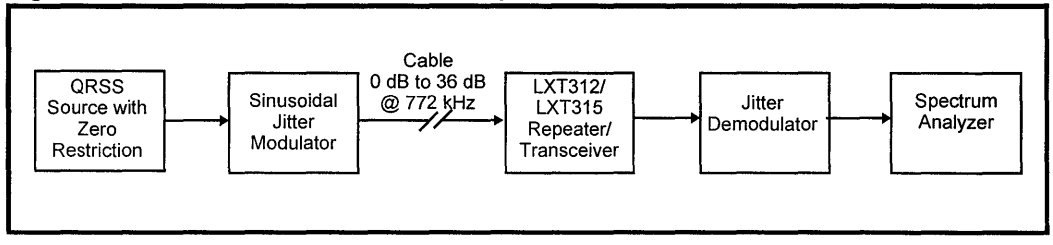


Figure 7: Receiver Jitter Transfer Test Setup



Interference Margin Testing

The LXT312 and LXT315 receiver noise interference margin is specified at a minimum of -11 dB for line losses from 0 dB to 36 dB. The test setup used to measure noise margin is shown in Figure 8.

Gaussian Noise Immunity Testing

Receiver immunity to gaussian noise is specified at a maximum BER of 10^{-7} for a quasi-random T1 signal at 1.544 MHz (±130 ppm). The receiver must be immune to noise power expressed as Np = -(L + 4.7) dBm, where L corresponds to the line loss and is valid for 0 to 36 dB.

Figure 9 shows the setup used to test gaussian noise immunity. The noise source is gaussian to at least 6 sigma and filtered to simulate expected noise in a binder group (per AT&T TA #24/CB113).

60 Hz Pulse Modulation Immunity Testing

Receiver immunity to 60 Hz pulse amplitude modulation is specified using the gaussian noise source described in the previous paragraph on gaussian noise immunity. Pulse amplitude modulation is specified between 10% and 30% of the nominal amplitude (see AT&T TA #24/CB113 for details on the modulation envelope). Figure 10 shows the setup used for testing receiver immunity to 60 Hz pulse amplitude modulation. The following data reflect noise power for 10^{-7} BER at each modulation level, where L corresponds to the line loss and is valid for 0 to 36 dB:

Modulation Level	Noise Power
10%	Np = -(L + 5.7) dBm
20%	Np = -(L + 6.7) dBm
30%	Np = -(L + 8.7) dBm

Receiver Timing Recovery Testing

Receiver timing recovery phase shift modulation for repetitive 8-bit patterns is specified at less than 0.07 UI. This is tested using any two out of 35 possible 8-bit patterns and measuring the change in output pulse timing from one pattern to the other (see AT&T TA #24/CB113 for details on the patterns). Switching rate from one pattern to the other is specified at between 300 Hz and 500 Hz. The setup used to test receiver timing recovery phase shift modulation is shown in Figure 11.

Figure 8: Receiver Noise Interference Margin Test Setup

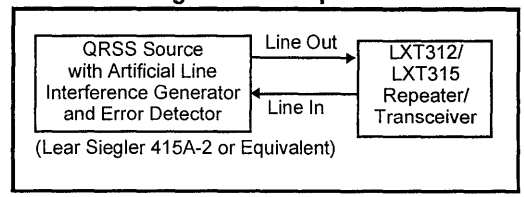


Figure 9: Receiver Gaussian Noise Immunity Test Setup

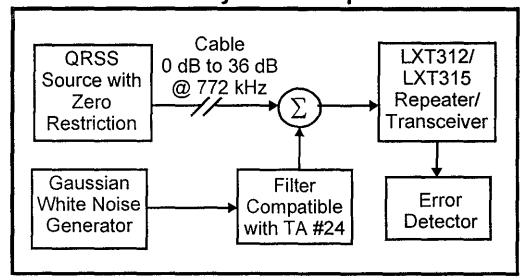


Figure 10: Receiver 60 Hz Pulse Amplitude Modulation Immunity Test Setup

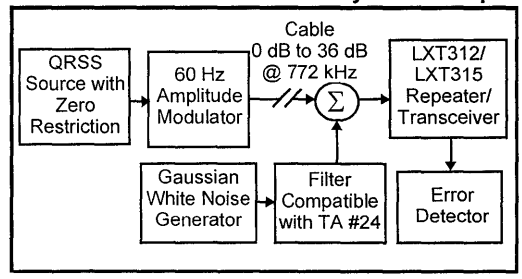
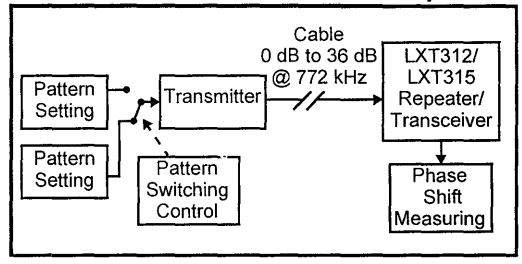


Figure 11: Receiver Timing Recovery Phase Shift Modulation Test Setup



NOTES

JULY 1997
Revision 2.2

LXT313 / LXT316

Low Power E1 PCM Repeaters / Transceivers

General Description

The LXT313 and LXT316 are integrated repeater/transceiver circuits for E1 carrier systems. The LXT313 is a dual repeater/transceiver and the LXT316 is a single repeater/transceiver. The LXT313 and LXT316 are designed to operate as regenerative repeaters/transceivers for 2.048 Mbps data rate PCM lines. Each includes all circuits required for a regenerative repeater/transceiver system including the equalization network, automatic line build-out (ALBO), and a state-of-the-art analog/digital clock extraction network tuned by an external crystal.

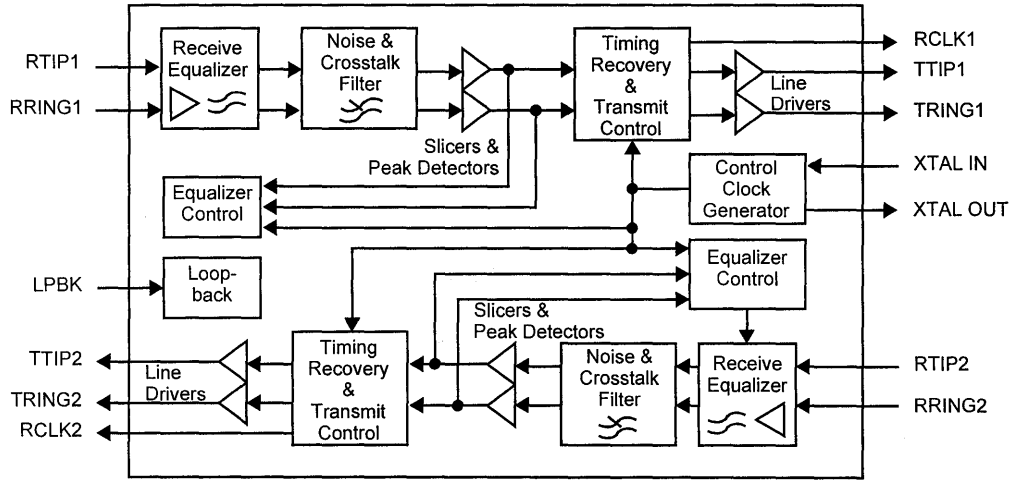
The key feature of the LXT313 family is that it requires only a crystal and a minimum of other components to complete a repeater/transceiver design. Compared with traditional tuned coil-type repeaters/transceivers, they offer significant savings in component and labor costs, along with reduced voltage drop/power consumption, and improved reliability. To ensure performance for all loop lengths, the LXT313 and LXT316 are 100% AC/DC tested using inputs generated by Level One's proprietary transmission line and network simulator.

The LXT313 and LXT316 are advanced CMOS devices which require only a single 5-volt power supply.

Features

- Integrated repeater/transceiver circuit on a single CMOS chip
- On-chip equalization network
- On-chip ALBO
- Low power consumption
- No tuning coil
- On-chip Loopback
- Recovered Clock Output
- 0 to 43 dB dynamic range
- -14 dB interference margin
- Single 5 V only CMOS technology
- Available in 16-pin PDIP and 44-pin PLCC

LXT313 / LXT316 Block Diagram



PIN ASSIGNMENTS AND SIGNAL DESCRIPTIONS

Figure 1: LXT313 / LXT316 Pin Assignments

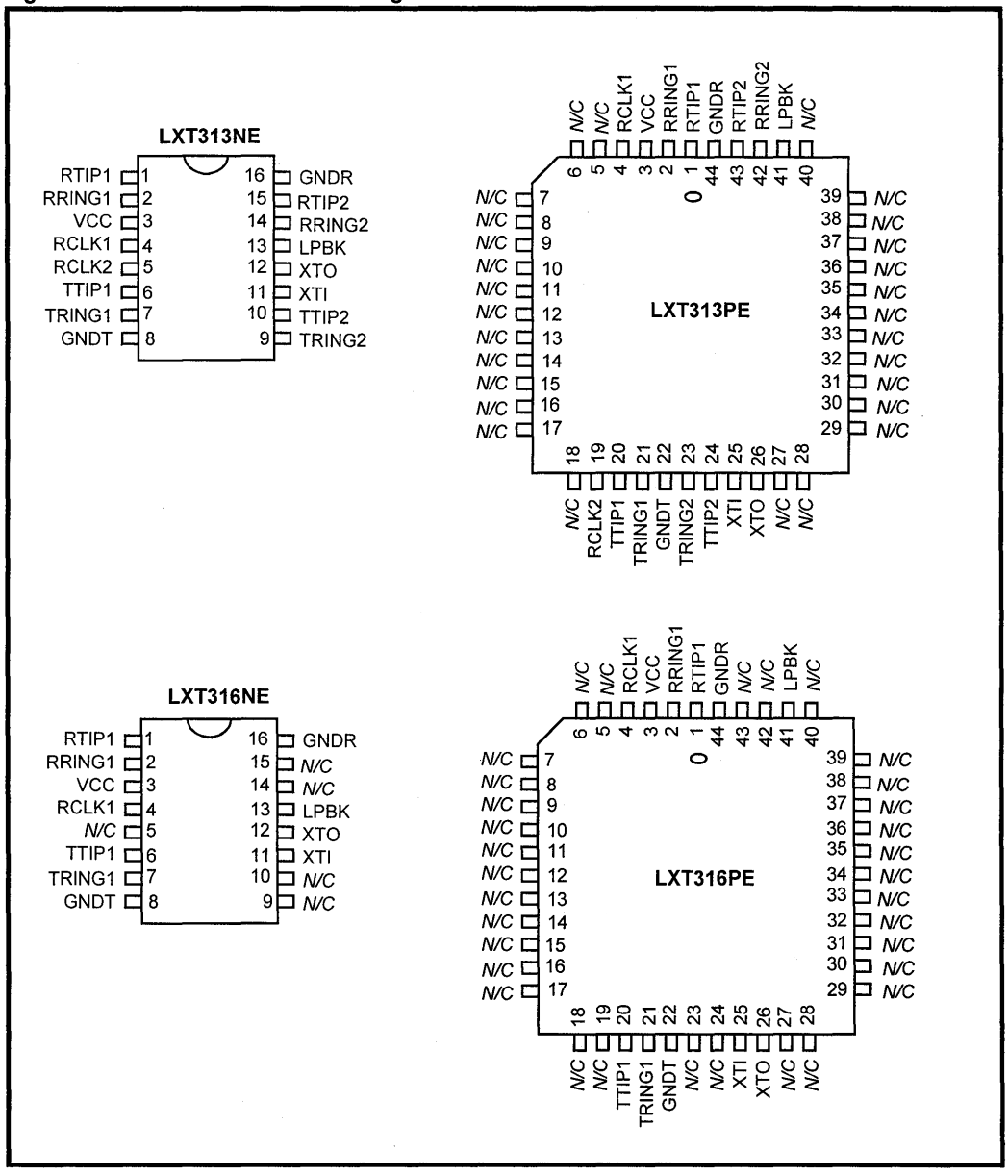


Table 1: LXT313 / LXT316 Signal Descriptions

Pin #		Symbol	I/O	Description
DIP	PLCC			
1	1	RTIP1	I	**Repeater Tip and Ring Inputs.** Tip and ring receive inputs for Channel 1.
2	2	RRING1	I	
4	4	RCLK1	O	**Recovered Clock.** Clock output recovered from Channel 1 receive input.
6	20	TTIP1	O	**Repeater Tip and Ring Outputs.** Open-drain output drivers for Channel 1.
7	21	TRING1	O	
11	25	XTI	I	**Crystal Oscillator Pins.** An 8.192 MHz crystal should be connected across these two pins. For alternative timing references, refer to Application Information.
12	26	XTO	O	
3	3	VCC	–	**Power Supply.** Power source for all circuits. +5 V (±0.25 V).
8	22	GNDT	–	**Transmit Ground.** Ground return for transmit circuits.
16	44	GNDR	–	**Receive Ground.** Ground return for receive circuits.
9[1]	23[1]	TRING2	O	**Side 2 Ring and Tip Outputs.** On the LXT313 dual repeater/transceiver, these are open-drain output drivers for Channel 2.
10[1]	24[1]	TTIP2	O	
14[1]	42[1]	RRING2	I	**Side 2 Ring and Tip Inputs.** On the LXT313 repeater/transceiver, these are tip and ring receive inputs for Channel 2.
15[1]	43[1]	RTIP2	I	
5[1]	19[1]	RCLK2	O	**Recovered Clock.** On the LXT313 dual repeater/transceiver, this is the recovered clock output for Channel 2.
13	41	LPBK	I	**Loopback Control.** On the LXT313, this pin controls Loopback Selection: High = Loopback side 1 data to side 2; Low = No Loopback. ***On the LXT316 single repeater/transceiver, this pin must be connected to GND.***

1. On the LXT316NE and LXT316PE single repeater/transceiver, these pins are not connected (N/C).
2. On the LXT313PE and LXT316PE, pins 5 through 18 and 27 through 40 are not connected (N/C).

FUNCTIONAL DESCRIPTION

Introduction

CM signals are attenuated and dispersed in time as they travel down a transmission line. Repeaters/transceivers are required to amplify, reshape, regenerate and retime the PCM signal, then retransmit it.

The LXT313 and LXT316 each contain all the circuits required to build a complete PCM repeater/transceiver. The operational range of the repeaters/transceivers is 0 to 43 dB of cable loss at 1.024 MHz (equal to 2 km of 22 gauge pulp-insulated cable between repeaters).

Receive Function

The signal is received through a 1 : 1 transformer at RTIP and RRING and equalized for up to 43 dB of cable loss. The receive equalizer uses a proprietary on-chip adaptive filter technique which is equivalent to a 3-port ALBO equalizer design. The monolithic structure of the filter and the absence of external components provide excellent ISI and dispersion elimination, and accurate data transfer over temperature.

Receiver noise immunity is optimized by a proprietary crosstalk elimination filter which eliminates the unneeded high frequency components of the received signal.

Timing Recovery Function

The equalized signal is full wave rectified and used to generate information for the timing recovery circuit. This circuit uses a mixed analog/digital technique to provide a low-jitter PLL similar to a tuned tank with excellent jitter tracking ability. But unlike a tuned tank, the free running frequency of the PLL clock is accurately controlled by the external reference crystal. No adjustment is required. Refer to Application Information for crystal specifications.

Recovered clock signals are available on the RCLK pins for applications that require bit stream synchronization.

Transmit Function

Recovered data is re-synchronized to the recovered clock signal by the timing recovery and transmit control section. The data is then retransmitted to the network via two open-drain, high-voltage transistors.

Loopback Function (LXT313 Only)

The LXT313 includes a loopback function for network diagnostics. With the LPBK pin Low, the repeater/transceiver operates in the normal mode. When the LPBK pin is pulled High, the data is looped back from side 1 to side 2.

APPLICATION INFORMATION

Typical Application

Figure 2 shows a typical E1 dual repeater/transceiver application circuit using standard repeater/transceiver card edge connections. It includes a jumper-selectable shorting option for the fault location circuitry (dashed lines at connector pins 2 and 7). Table 2 lists the specifications for the crystal used with the LXT313 or LXT316 repeater.

Alternate Timing Reference

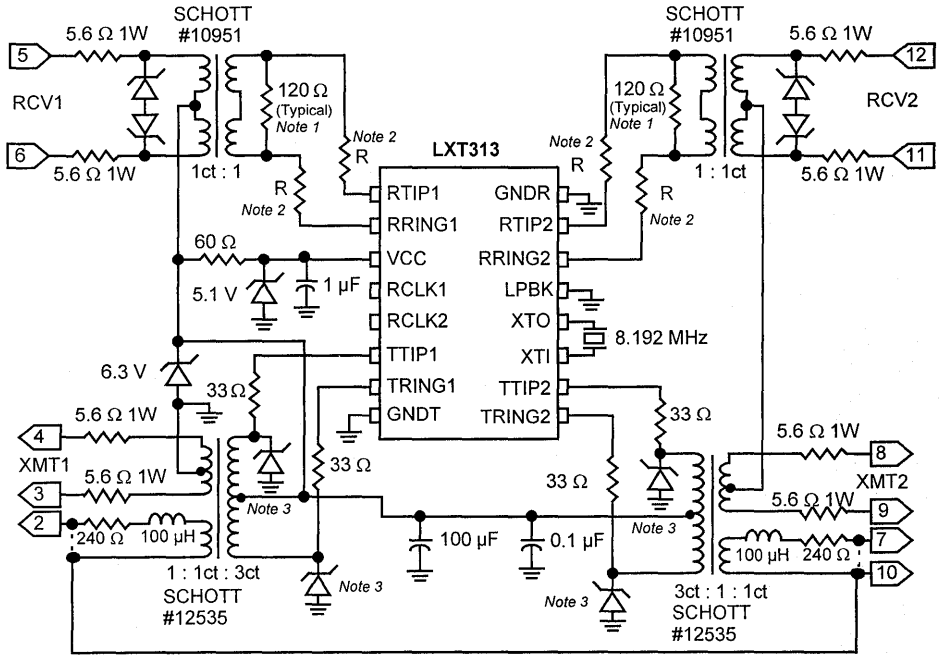
For applications where a crystal is not appropriate, a 2.048 MHz or 8.192 MHz, CMOS-level (High ≥ 4.5V, Low ≤ 0.5V) oscillator may be connected to XTI. In this situation, XTO must be tied to Vcc and GND via a voltage divider as shown in Figure 3

Table 2: Crystal Specifications

Parameter	Specification
Frequency	8.192 MHz
Frequency tolerance[1]	± 50 ppm
Effective series resistance	30 Ω Maximum
Crystal cut	AT
Resonance	Parallel
Maximum drive level	2.0 mW
Mode of operation	Fundamental

1. @ 25 °C, C Load = 10 pF; and from -40 °C to +85 °C (Ref 25 °C reading)

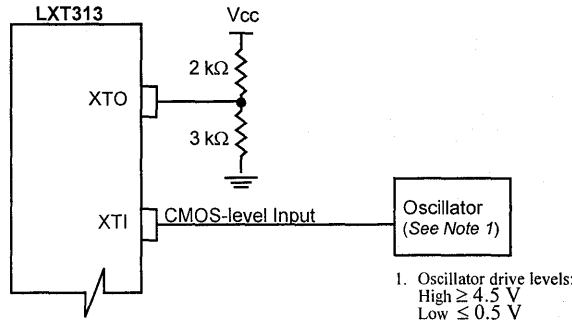
Figure 2: Typical E1 Dual Repeater/Transceiver Application



NOTES:

1. Check cable impedance required by the approving telecom agency.
2. RTIP/RRING Resistors are used to provide surge protection. Values can be 0 – 100 Ω.
3. TTIP/TRING Zeners are used to reduce surge susceptibility. Values can be 12 – 14 V.

Figure 3: Alternate Timing Reference Circuitry



TEST SPECIFICATIONS

NOTE

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Table 3: Absolute Maximum Ratings

Parameter	Symbol	Units
Supply voltage (min to max)	VCC	-0.3 V to +6 V
Driver Voltage	VOH	18 V
Receiver Current	ICC	100 mA
Operating temperature (min to max)	TOP	-40 °C to +85 °C
Storage temperature (min to max)	TST	-65 °C to +150 °C

CAUTION

Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

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Digital Outputs - Low	(IOL = 1.6 mA	VOL	–	–	0.4	V
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	(IOH < 10 µA)	VOH	–	4.5	–	V
Digital Inputs - High		VIH	2.0	–	–	V
Digital Inputs - Low		VIL	–	–	0.8	V
Supply Current (from VCC supply)[2]	All zeros	ICC	–	15	23	mA
	All ones	ICC	–	–	25	mA
Driver Leakage Current (VDVR = 18 V)		ILL	–	–	100	µA
Driver Pulse Amplitude (Driver output IO = 20 mA)		AP	0.65	–	0.95	V

1. Typical values are at 25° C and are for design aid only; they are not guaranteed and not subject to production testing.
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Figure 4: Digital Timing Characteristics

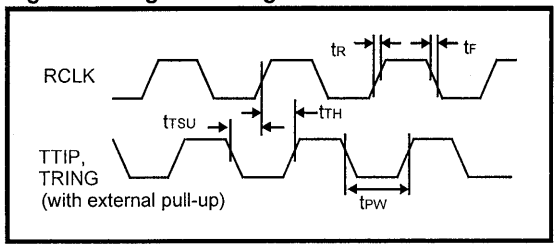


Table 6: Digital Timing Characteristics (Over Recommended Range) see Figure 4

Parameter	Symbol	Min	Typ[1]	Max	Units
Driver Pulse Width	tPW	219	244	269	ns
Driver Pulse Imbalance	–	–	–	15	ns
Rise and Fall Time (any digital output[2])	tR / tF	–	–	25	ns
Setup Time - TTIP/TRING to RCLK	tTSU	90	–	–	ns
Hold Time - TTIP/TRING from RCLK	tTH	90	–	–	ns

1. Typical values are at 25° C and are for design aid only; they are not guaranteed and not subject to production testing.
2. Measured with $C_{LOAD} \leq 10$ pF, $R_{LOAD} > 100$ kΩ.

Test Setups

Introduction

Both the LXT313 and LXT316 are fully tested (100% AC and DC parameters) using inputs generated by Level One's proprietary transmission line and network simulator. Device testing includes receiver jitter tolerance, jitter transfer and interference margin for line losses from 0 dB to 43 dB @ 1.024 MHz. Specifications and bench test setups are shown in Figures 5 through 9.

Receiver Jitter Tolerance Testing

Receiver jitter tolerance meets the template shown in Figure 5, when operated at line losses from 0 to 43 dB. Figure 7 shows the setup used for jitter tolerance testing.

Receiver Jitter Transfer Testing

Receiver jitter transfer meets the template shown in Figure 6, when operated with line losses from 0 to 43 dB and input jitter amplitude of 0.15 UI peak-to-peak. Jitter gain at a given frequency is defined as the difference between intrinsic jitter and additive jitter at the measurement frequency, divided by the amplitude of the input jitter. Figure 8 shows the setup used for jitter transfer testing.

Figure 5: Receiver Jitter Tolerance Template

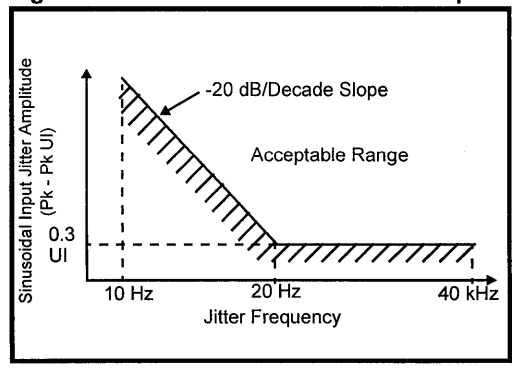


Figure 6: Receiver Jitter Transfer Template

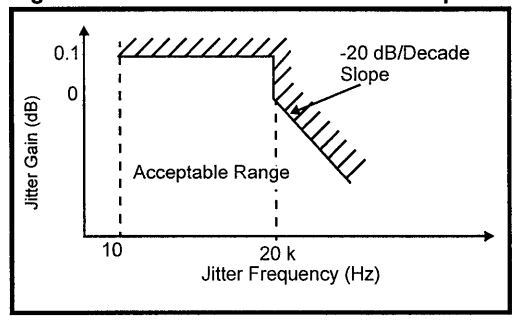


Figure 7: Receiver Jitter Tolerance Test Setup

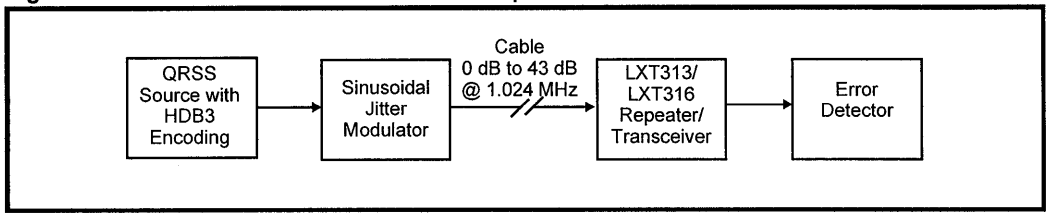
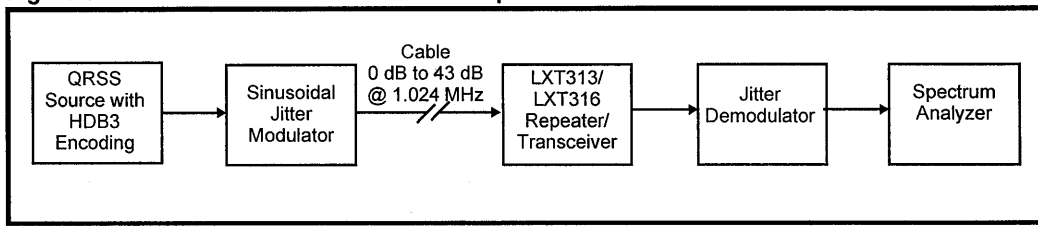


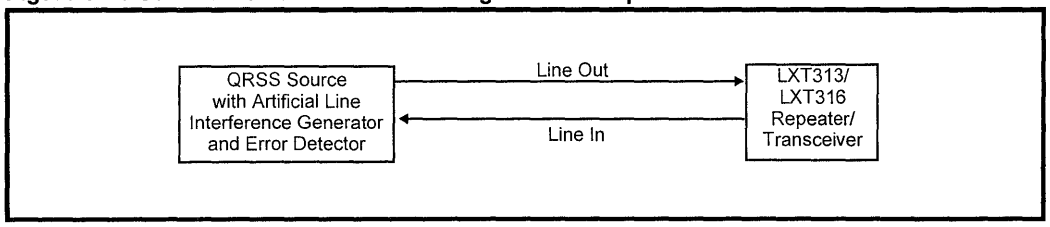
Figure 8: Receiver Jitter Transfer Test Setup



Interference Margin Testing

The LXT313 and LXT316 receiver noise interference margin is specified at a minimum of -14 dB for line losses from 0 dB to 43 dB. The test setup used to measure noise margin is shown in Figure 9.

Figure 9: Receiver Noise Interference Margin Test Setup



NOTES

Switched 56/DDS Products

APRIL 1997
Revision 3.1

LXT400

All Rate Extended Range Switched 56/DDS Transceiver

General Description

The LXT400 is an integrated line interface circuit for Switched 56 (SW 56) and Digital Data Service (DDS), compatible with any combination of 19 to 26 AWG cable. The LXT400 operates at any of 17 preset data rates from 2.4 kbps to 72.0 kbps, providing appropriate transmit pulse shaping, receive signal detection and timing recovery at the metallic interface between the carrier and the customer installation. The LXT400 offers a variety of diagnostic features including loopback, line status and equalizer monitor outputs, while conforming to AT&T, ANSI and Bellcore specifications.

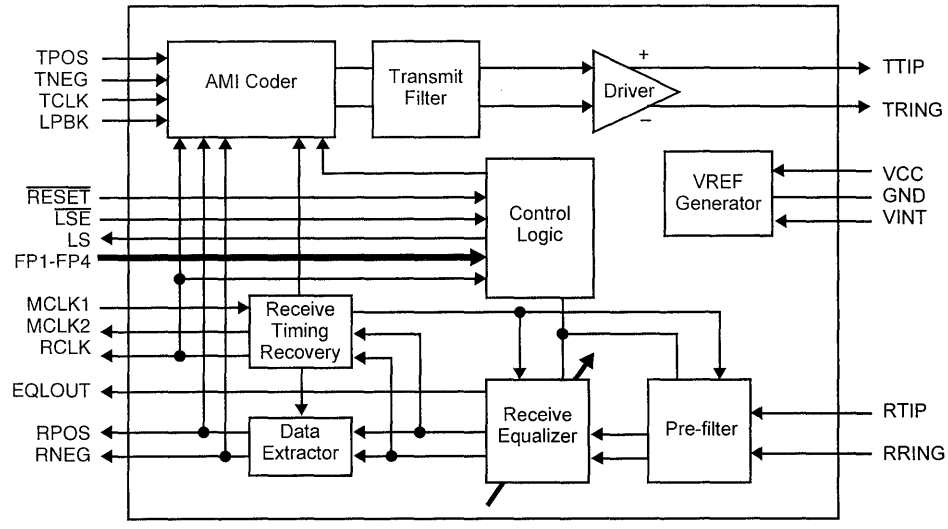
The LXT400 transmit section includes switched capacitor filters, continuous reconstruction filters, and a 50% AMI encoder. The AMI pulse is synchronized with the transmit clock.

The LXT400 receive section performs line equalization, data extraction and timing recovery. The LXT400 has a BER of less than 10^{-7} with up to 49 dB of cable attenuation at the Nyquist frequency for 56, 64 and 72 kbps, and 40 dB at the lower rates. The LXT400 is an advanced CMOS device which requires only a single +5 V power supply.

Features

- Enhancements:
  - Three new data rates: 38.4, 51.2, and 64.0 kbps
  - Improved accuracy in line attenuation reporting
  - Simplified transmit digital timing
- Integrated transmitter, receiver and timing recovery on a single CMOS chip
- Transparent to framing and coding
- Receive equalizer filters allow data recovery from signals with up to 40 dB of attenuation at the Nyquist frequency at line rates below 56 kbps, and up to 49 dB at the 56, 64 and 72 kbps line rates
- Single 4.096 MHz crystal or master clock input
- Digital back-end loopback
- Equalizer output monitor pin
- Line status (loop length, RLOS, etc.) information available for maintenance purposes
- Low power consumption (200 mW typical)
- Available in 28-pin plastic DIP and PLCC
- Single 5 V only CMOS technology

LXT400 Block Diagram



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PIN ASSIGNMENTS AND SIGNAL DESCRIPTIONS

Figure 1: LXT400 Pin Assignments

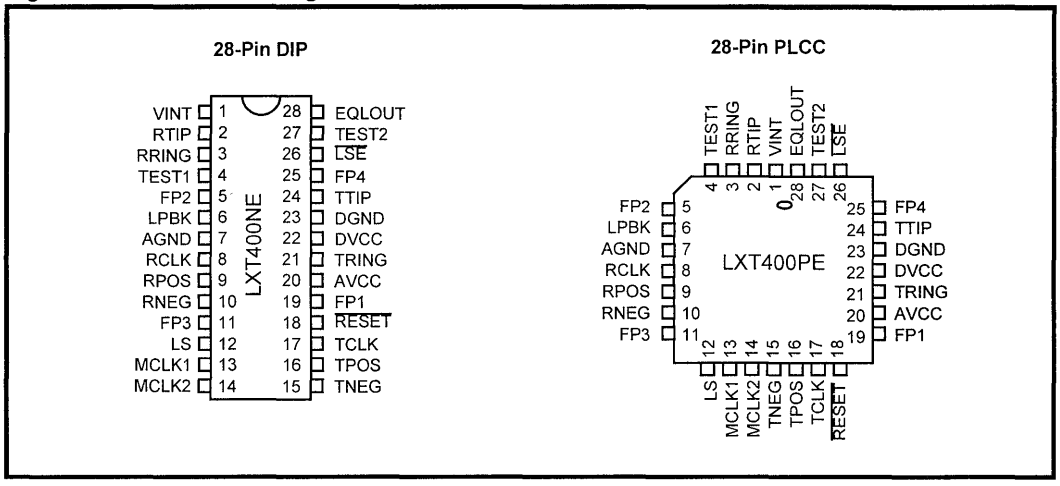


Table 1: LXT400 Signal Descriptions

Pin #	Sym	I/O	Description
1	VINT	I	**Intermediate Voltage Reference.** Reference voltage used for internal analog circuits. This pin must be connected through a 1kΩ resistor (Rv) to the center node between the two termination resistors, Rr, as shown in Figure 8 and 9.
2 3	RTIP RRING	I	**Receive Tip** and **Receive Ring.** Receive data input pair. RTIP and RRING are a fully differential input for the receive line interface.
4	TEST1	I	**Test 1.** Factory Test Pin. *Do not connect.*
19 5 11 25	FP1 FP2 FP3 FP4	I I I I	**Frequency Programming Inputs 1 through 4.** The LXT400 data rate is set by the logic levels present at the FP1 through FP4 inputs as shown in Table 2. For operation at 38.4, 51.2, and 64.0 kbps, the RCLK output must be applied to the FP3 input.
6	LPBK	I	**Loopback.** When set High, activates digital back-end loopback.
7	AGND	-	**IC Ground.** Ground for all IC circuitry except the transmit driver.
8	RCLK	O	**Recovered Clock.** Clock recovered from signal input at RTIP and RRING, based on the data rate setting on the FP1 - FP4 inputs.
9 10	RPOS RNEG	O O	**Receive Data Positive** and **Negative.** Receive data outputs. A signal on RPOS corresponds to receipt of a positive pulse on RTIP and RRING. A signal on RNEG corresponds to a negative pulse on RTIP and RRING. Both outputs transition on the rising edges of RCLK, and are never High simultaneously.

Table 1: LXT400 Signal Descriptions – continued

Pin #	Sym	I/O	Description
12	LS	O	**Line Status Output.** A 16-bit serial word indicating activation state, line loss, and loss of signal (LOS). LS transitions occur on falling edges of RCLK. LS goes to a high impedance state when $\overline{LSE}$ is High. If $\overline{LSE}$ is tied Low, the LS output represents LOS only.
13 14	MCLK1 MCLK2	I O	**Master Clock 1** and **Master Clock 2**. The required 4.096 MHz master clock may be provided by a crystal connected across these pins, or by a digital clock connected to MCLK1. If a clock is provided on MCLK1, MCLK2 must be left unconnected.
15 16	TNEG TPOS	I I	**Transmit Data Negative** and **Positive.** These inputs are sampled on the falling edges of TCLK. AMI pulses are encoded as follows: TPOS TNEG Transmit Signal 0 0 Space 0 1 Negative Pulse 1 0 Positive Pulse 1 1 Space
17	TCLK	I	**Transmit Clock.** Transmit clock at the data rate set by the FP1 - FP4 inputs.
18	$\overline{RESET}$	I	**Reset**. Hardware reset pin. Must be pulsed Low on power-up to initialize all internal circuits. Must also be pulsed Low after changing the data rate setting, and after forcing or releasing any loopback condition.
20	AVCC	-	**IC Power**. Power supply for all IC circuits except the transmit driver. +5 V (±5%).
21 24	TRING TTIP	O O	**Transmit Ring** and **Transmit Tip.** Differential driver outputs. Designed to drive the 135Ω twisted-pair cable through the transmit line interface shown in application diagrams (see Figure 8 and 9).
22	DVCC	-	**Driver Power.** Transmit driver power supply. +5 V (±5%). Tie to AVCC, pin 20.
23	DGND	-	**Driver Ground**. Transmit driver ground. Tie to AGND, pin 7.
26	$\overline{LSE}$	I	**Line Status Enable.** Active Low enable for the LS serial port. This pin must transition from High to Low to read LS serial data. $\overline{LSE}$ is sampled on the rising edges of RCLK.
27	TEST2	I	**Test 2.** Analog test pin. *Must be tied to ground.*
28	EQLOUT	O	**Equalizer Output Monitor.** Monitors Equalizer. *Must be left open when not used.*

FUNCTIONAL DESCRIPTION

Introduction

The LXT400 comprises three basic sections: transmit, receive and control logic.

The transmit section includes a 50% AMI encoder, a programmable switched-capacitor low-pass filter, a low-pass notch filter, a transmit timing re-synchronizer and a continuous reconstruction filter. An on-chip CMOS driver is also incorporated to drive a 135Ω line through a transformer.

The receive section includes pre-filters and line equalizers, and the timing recovery and data extraction blocks. An internal digital phase-locked loop (DPLL) is used in conjunction with the MCLK input to synchronize the recovered clock and data.

The control logic block initializes the transceiver, selects receive filters and reports status information on the serial port. Control logic inputs FP1 through FP4 determine the data rate as specified in Table 2. The control logic executes the initialization procedure upon automatic re-synchronization or external $\overline{\text{RESET}}$. Filter selection optimizes the receive signal-to-noise ratio (SNR) by matching the filter in the equalizer section to the strength of the received signal (a function of loop length/line loss). The control logic block also reports receiver status, estimated line length (as indicated by filter selection) and a receive loss of signal (RLOS) alarm on the serial port.

Initialization

Upon power-up, or after changing the baud rate or loopback condition of the line interface, a $\overline{\text{RESET}}$ pulse is required to initialize the LXT400. On receipt of the $\overline{\text{RESET}}$ pulse, the LXT400 executes an iterative cycle of level detection and offset cancellation to select the appropriate equalizer settings for the received signal. Receiver initialization can be monitored on the serial channel. When received data has a 50% ones density, full operation is achieved within one second after $\overline{\text{RESET}}$. Under the minimum ones density condition specified in Table 3, full operation is achieved within eight seconds after $\overline{\text{RESET}}$. Correct initialization assumes the presence of an AMI-coded signal at the RTIP and RRING inputs. The LXT400 will not correctly initialize unless a stable signal which meets the network interface specifications of AT&T Pub 62310 is present at the RTIP and RRING inputs during the entire initialization process. The RPOS/RNEG outputs are not valid until full operation is achieved. During offset cancellation, the RPOS/RNEG outputs do not adhere to the AMI rule. However, once initialized (assuming that a proper baud rate is selected), RPOS and RNEG outputs are never simultaneously High.

Reset

A hardware reset is required after any of the following changes in transceiver configuration:

1. A change in Data Rate setting
2. A change in the local analog loopback configuration
3. A local change in the line upon which the transceiver is communicating (for example, configurations for changing lines in a "1 for n" redundancy scheme).

5

Table 2: Data Rate Programming

FP4	FP3	FP2	FP1	Data Rate[1]
Low	Low	Low	Low	2.4 kbps
Low	Low	Low	High	3.2 kbps
Low	Low	High	Low	4.8 kbps
Low	Low	High	High	6.4 kbps
Low	High	Low	Low	9.6 kbps
Low	High	Low	High	12.8 kbps
Low	High	High	Low	19.2 kbps
Low	High	High	High	25.6 kbps
High	Low	Low	Low	56.0 kbps
High	Low	Low	High	72.0 kbps
High	Low	High	Low	3.5 kbps
High	Low	High	High	7.0 kbps
High	High	Low	Low	14.0 kbps
High	High	Low	High	28 kbps
Low	RCLK[1]	Low	Low	38.4 kbps
Low	RCLK[1]	Low	High	51.2 kbps
Low	RCLK[1]	High	Low	64.0 kbps

1. These data rates are activated when RCLK output on pin 8 is applied to the FP3 input on pin 11.

Table 3: Ones Density Requirements

Data Rate (kbps)	Minimum Average Ones Density
2.4, 4.8, 9.6, 19.2, 38.4	1 / 12
3.2, 6.4, 12.8, 25.6, 51.2	1 / 16
56.0	1 / 14
64.0	1 / 16
72.0	1 / 18
3.5, 7.0, 14.0, 28.0	≈ 1 / 16

Automatic re-initialization may be triggered by changes in received signal strength as follows:

- If received signal strength increases by more than about 6 dB after full operation is achieved, automatic re-initialization occurs.
- If received signal strength decreases by more than about 4 dB, re-initialization occurs. If the decrease in received signal strength exceeds 6 dB, the LXT400 reports an LOS condition and performs an automatic re-initialization.

The time required to achieve full operation after re-initialization, is the same as required for power-on initialization (i.e., 1 second max with 50% ones density, 8 seconds under minimum ones density conditions). Re-initialization is not triggered by impulse noise events.

Transmission

TPOS and TNEG must have transitions coincident with the rising edges of TCLK. The transmit section generates a 50% AMI pulse according to the pulse encoding rules, which is synchronized with the TCLK input. In DSU applications, RCLK is typically routed back into the TCLK input. The instantaneous baud period varies with the receive DPLL phase adjustments, however, the pulse duty cycle is maintained at 50% of the nominal baud period by internal re-synchronization to TCLK. The AMI pulse is then processed through a set of frequency dependent filters.

Initial filtering at all rates is accomplished by a programmable, switched-capacitor, low-pass filter. This filter is a single-pole type with the pole set at 1.3 times the bit rate (as determined by inputs FP1 - FP4).

For data rates of 2.4, 3.2, 4.8, 6.4, 9.6 and 12.8 kbps, the filtered pulses go through an additional low-pass notch filter. The notch filter is required to protect other DDS services with specific band requirements, and provides the attenuation listed in Table 4. The additional rejection requirement is weighted within each band by "C-Message" weighting over double speech sidebands around a carrier in the middle of each band (28 kHz and 76 kHz). The C-Message weighting function is graphed in Figure 2. Depending on the data rate, the frequency template extends to different limits as shown in Table 5. (An alternate notch filter is used for data rates of 3.5 and 7.0 kbps.) The single pole, low-pass filter would maintain the frequency within ± 5%. The notch filter attenuation is added to this.

A continuous filter, common to all data rates, is the final stage. The continuous filter removes high frequency components which remain after processing by the low-pass filter stages. The pulse is then applied to the line driver for transmission onto the twisted-pair line.

Figure 2: C-Message Weighting

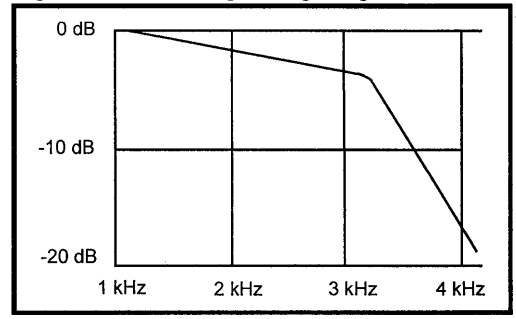


Table 4: Notch Filter Attenuation

OCU/Loop Data Rate (kbps)	Customer (Primary Channel) Data Rate (kbps)	Rejection Band	
		22 - 32 kHz	72 - 80 kHz
2.4 or 3.2	2.4	5 dB	1 dB
4.8 or 6.4	4.8	13 dB	9 dB
9.6 or 12.8	9.6	17 dB	8 dB

Reception

RTIP and RRING inputs are differentially detected, then processed through the pre-filters and equalizer section. The continuous pre-filter removes high frequency noise and prevents aliasing problems for the switched capacitor (SC) line equalizers which follow. Pulse reshaping is achieved by the receive equalizer, which consists of an SC step equalizer and an adaptive decision feedback equalizer (DFE). The DFE eliminates residual inter-symbol interference (ISI) due to echoing by multiple bridged tap connections and the quantized frequency responses of the SC step filters. The DFE is continuously adapted to compensate for ISI due to time-varying line characteristics such as temperature, humidity and age. Nine different filter selections based on signal strength are available.

Changes in Received Signal Strength

During initialization, the LXT400 selects filters appropriate to the strength of the received signal. After initialization, the LXT400 continually monitors the receive signal strength to ensure the optimum signal/filter match. Data reception is not affected by impulsive noise events or by slow changes in signal amplitude, such as may be caused by temperature and humidity changes on the line. (The maximum constant rate of change which the LXT400 can track is 6 dB per minute.) However, instantaneous "step" changes (see Figure 3) may temporarily interfere with data reception. Step changes may be due to sudden changes in loop loss, far end transmitter output, etc.

After normal operation has been established, an instantaneous single-step change may cause one of three conditions, as shown in Figure 4.

Under Condition 1, the LXT400 automatically adapts to minor step changes in signal strength (assuming that the new input is a valid DDS signal).

Under Condition 3, the LXT400 responds to significant step changes by re-initializing.

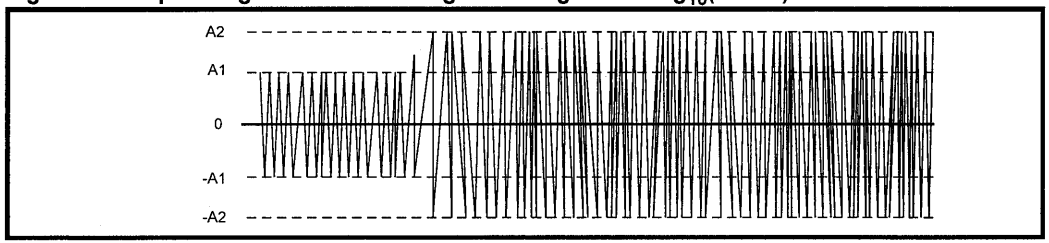
Condition 2, while unlikely to occur in an actual DDS implementation, may be observed in the laboratory due to artificial line simulators. Condition 2, which results from a 6 - 20 dB step increase in received signal strength, may result in a signal/filter mismatch. This condition is characterized by excessive bipolar violations (BPVs) which can be observed on RPOS and RNEG. External signal quality detection circuitry can be used to detect excessive BPVs that are not recognized as standard DDS BPV code words. Upon detection of unrecognized BPVs, the user may force a reset on the LXT400 to resume error-free operation.

Under normal operating conditions, step changes in received signal strength are all under local control. Thus, the user can reset the LXT400 once the new receive signal has stabilized at the chip inputs. Remote changes typically involve disconnecting one line and re-connecting another line of different length. These changes trigger the RLOS report and automatic re-initialization. Any remote changes in line length or transceiver configuration are beyond the local user's control. Remote changes in data rate are not detected.

Table 5: Frequency Limits per Data Rate

Data Rate (kbps)	Upper Frequency Limit (kHz)
2.4 (3.2)	100
4.8 (6.4)	150
9.6 (12.8)	150
19.2 (25.6)	150
38.4 (51.2)	150
56.0 (72.0)	150
64.0	150
3.5	100
7.0	150
14.0	150
28.0	150

Figure 3: Step Changes in Received Signal Strength = 20 $\log_{10}$(A2/A1) dB

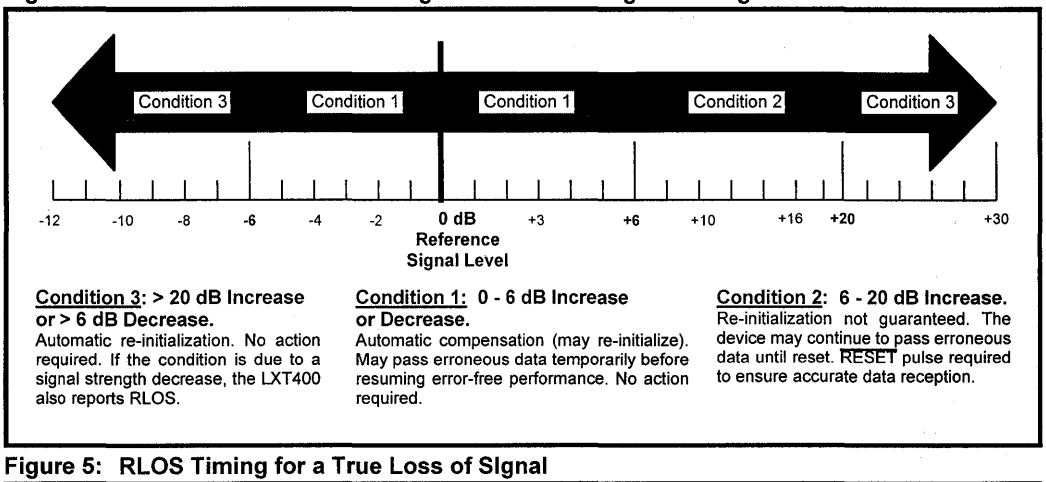


Receive Loss of Signal

RLOS goes High when more than 32 consecutive zeros are received, caused either by a true loss of signal, or a signal strength drop greater than 6 dB. The LXT400 automatically re-initializes when RLOS goes High, and 40 consecutive zeros are counted. Figure 5 shows the RTIP/RRING input and RLOS output timing relationships for a true loss of signal. When signal energy returns to the chip input, the LXT400 executes one full activation cycle in the presence of this signal. The result is that RLOS will remain High for a period of time (0.13 s < tH < 16 s) after signal energy reappears.

Figure 6 shows the RTIP/RRING input timing and RLOS output timing relationship for a signal strength decrease greater than 6 dB. In this case, RLOS will go High for a time 0.26 s < tP < 16 s.

Figure 4: Conditions Based on Changes in Received Signal Strength



Condition 3: > 20 dB Increase or > 6 dB Decrease.
Automatic re-initialization. No action required. If the condition is due to a signal strength decrease, the LXT400 also reports RLOS.

Condition 1: 0 - 6 dB Increase or Decrease.
Automatic compensation (may re-initialize). May pass erroneous data temporarily before resuming error-free performance. No action required.

Condition 2: 6 - 20 dB Increase.
Re-initialization not guaranteed. The device may continue to pass erroneous data until reset. RESET pulse required to ensure accurate data reception.

Figure 5: RLOS Timing for a True Loss of Signal

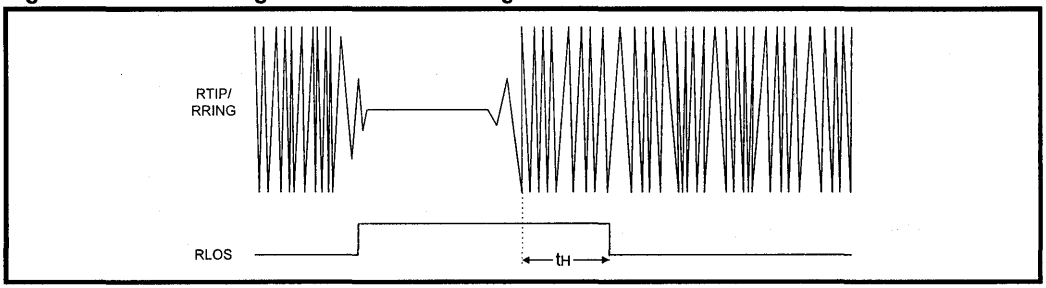
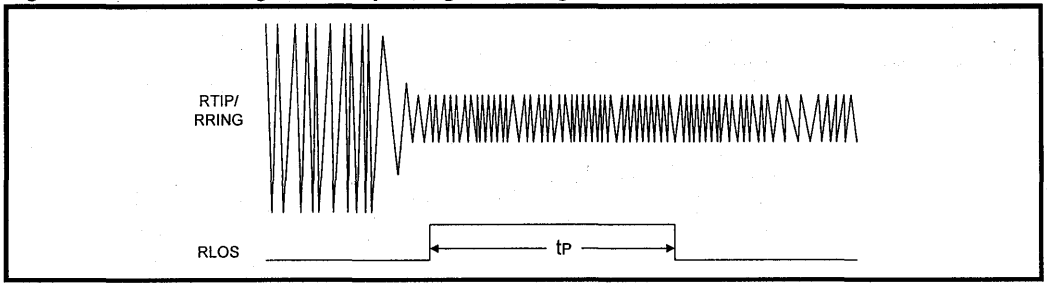


Figure 6: RLOS Timing for a Drop in Signal Strength > 6 dB



Timing Recovery

The timing recovery circuit uses a rate synchronizer to generate a high frequency internal clock from the MCLK input. A DPLL is used to synchronize this internal clock to the received data pulses. The output clock from the DPLL is divided down to generate RCLK and all other required clocks (except TCLK which is an external input).

Data Extraction

The data extraction block provides RPOS and RNEG outputs. A positive differential pulse received between RTIP and RRING results in a High on RPOS. A negative differential pulse between RTIP and RRING results in a High on RNEG. RPOS and RNEG are output at the received data rate and are valid on the falling edge of RCLK.

Receiver operation is not affected by the data patterns, provided the ones density requirements of Table 3 are met with no more than 26 consecutive zeros. RLOS is declared after 32 consecutive zeros. However, the RCLK output remains synchronized to the RTIP/RRING input for up to 40 consecutive zeros, after which re-initialization occurs. Bipolar violations are received properly. The bipolar violation coding rule that successive violations be of alternating polarity must be followed. However, if this rule is temporarily broken (due to channel noise, etc.), long term LXT400 data reception will not be adversely affected.

Loopback Operation

When the LPBK pin is set High, the recovered data and clock are sent back through the transmit section and onto the line interface, as well as being output on the RPOS/RNEG and RCLK pins. TPOS/TNEG and TCLK inputs are ignored in the loopback mode.

Serial Port Operation

The line status (LS) output is an 8-bit or 16-bit serial word enabled by pulling $\overline{LSE}$ Low for 8 or 16 bit-periods as shown in Figures 12 and 13. Refer to Test Specifications for Serial Port Timing. Bit assignments are listed in Table 6. Approximate line loss and loop length (based on received signal strength/filter selection, assuming far-end pulse transmission compliant with AT&T Pub 62310 or T1E1/90-051) are reported via bits b0 through b3 as listed in Table 7. When combined with the receive signal magnitude bits in positions b8-b15, the line attenuation may be calculated to within ±1 dB of actual value using the following equation:

$$\text{Insertion loss} = \left[\begin{array}{l}\text{Insertion loss value in}\\ \text{dB from Table 7 based}\\ \text{on LL3-LL0 value.}\end{array}\right] + 20\,\text{Log}_{10}\left(\frac{\text{3c hex}}{\text{Mag<7:0>hex}}\right);\text{dB}$$

Bits b4 through b6 indicate the receiver activation state. Bit b7 is the RLOS alarm.

Figure 7 shows the serial output for a typical LXT400 initialization sequence. Bits b0 - b3 report filter selection and bits b4 - b6 report receiver status. Bit b6 toggles to indicate that the receiver is alternating between offset cancellation (b6 - b4 = 100) and receive level detection (b6 - b4 = 000). The receiver starts with the highest-gain filter (b3 - b0 = 0111), cancels systematic voltage offset at the filter output, and then detects the receive signal level at the filter output. If the signal exceeds the threshold for that filter, the LXT400 steps down to the filter with the next-highest gain (b3 - b0 = 1000). This process is repeated until the receive signal level does not exceed the filter threshold.

Once the appropriate filter is selected, the receiver phase-locked loop (PLL) and slicer levels converge to match the receive signal for optimum SNR. During receiver convergence (b6 - b4 = 001), the PLL adapts to sample the peak of the receive pulses and the slicer level adapts to the midway point between zero and the pulse peak voltage. Once convergence is complete, the LXT400 begins full operation (b6 - b4 = 010).

Figure 7: Typical Serial Port Output for Receive Activation @ 72 kbps

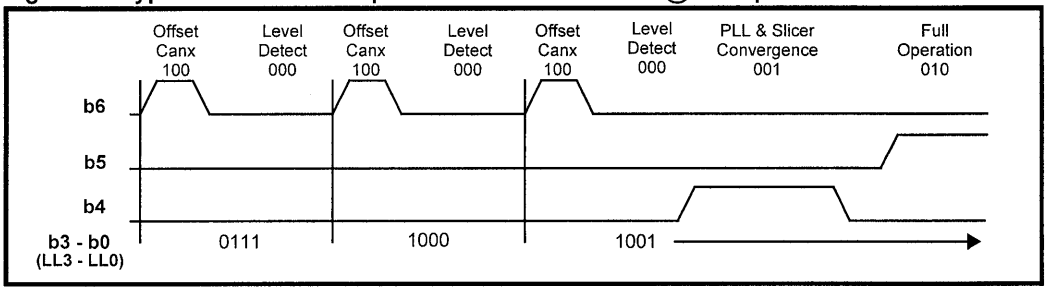


Table 6: LS Word Bit Assignments

Bit #	Name	Description	Bit #	Name	Description
b0	LL0	Loop Length Indication, bit 0	b8	MAG0	Rx signal magnitude bit 0
b1	LL1	Loop Length Indication, bit 1	b9	MAG1	Rx signal magnitude bit 1
b2	LL2	Loop Length Indication, bit 2	b10	MAG2	Rx signal magnitude bit 2
b3	LL3	Loop Length Indication, bit 3	b11	MAG3	Rx signal magnitude bit 3
b4	S1	Receiver Converging when High	b12	MAG4	Rx signal magnitude bit 4
b5	S2	Full Operation when High	b13	MAG5	Rx signal magnitude bit 5
b6	S0	Level Detection when High	b14	MAG6	Rx signal magnitude bit 6
b7	RLOS	Receive Loss of Signal when High	b15	MAG7	Rx signal magnitude bit 7

Table 7: LS Loop Length Bits LL3 - LL0

Rate kbps	Insertion Loss @ fb/2 in dB / Line Range in km (24 AWG PIC, no bridged taps) for LL3 - LL0 Values are for optimum receiver slicer level, with MAG7 - MAG0 = 3C hex								
	0111	1000	1001	1010	1011	1100	1101	1110	1111
2.4	N/A	42.3 / 23	36.0 / 19.2	30.0 / 15.3	24.2 / 11.5	20.0 / 8.6	15.5 / 5.0	10.6 / 2.4	3.4 / 0.8
3.2	N/A	42.0 / 19.9	36.0 / 16.9	30.7 / 14.3	25.2 / 11.6	20.0 / 7.8	15.0 / 4.9	10.3 / 2.4	3.0 / 0.7
4.8	N/A	42.3 / 17.3	36.3 / 14.7	30.5 / 12.0	24.7 / 9.3	18.8 / 6.7	13.5 / 4.0	9.3 / 2.0	3.1 / 0.7
6.4	N/A	42.4 / 15.4	36.5 / 13.2	31.2 / 11.0	25.6 / 8.8	20.0 / 6.6	15.0 / 4.4	10.0 / 2.2	3.3 / 0.7
9.6	N/A	40.0 / 12.5	35.0 / 10.7	29.6 / 8.9	24.2 / 7.1	18.9 / 5.4	13.8 / 3.6	9.0 / 1.8	2.5 / 0.5
12.8	N/A	42.3 / 11.7	36.2 / 10.0	30.7 / 8.3	25.0 / 6.7	19.3 / 5.0	13.8 / 3.3	8.8 / 1.7	2.6 / 0.5
19.2	N/A	42.2 / 10.0	36.2 / 8.6	30.5 / 7.1	24.9 / 5.7	14.0 / 4.3	13.0 / 2.9	7.7 / 1.4	1.0 / 0.2
25.6	N/A	42.0 / 9.0	36.0 / 7.7	30.2 / 6.4	24.5 / 5.1	18.4 / 3.9	13.6 / 2.6	7.5 / 1.3	0.5 / 0.1
38.4	N/A	42.5 / 8.4	36.5 / 7.1	30.7 / 6.0	25.0 / 4.7	18.9 / 3.6	14.0 / 2.4	7.4 / 1.2	1.0 / 0.2
51.2	N/A	43.0 / 7.7	37.0 / 6.6	31.2 / 5.5	25.5 / 4.4	19.4 / 3.3	14.0 / 2.2	7.4 / 1.1	0.5 / 0.1
56.0	50.5 / 8.5	44.4 / 7.5	38.4 / 6.4	32.3 / 5.3	26.0 / 4.2	19.7 / 3.2	13.6 / 2.1	7.3 / 1.1	0.0 / 0.0
72.0	50.7 / 8.0	45.0 / 7.0	38.8 / 6.0	32.5 / 5.0	26.3 / 4.0	20.0 / 3.0	14.0 / 2.0	7.4 / 1.0	0.0 / 0.0
64.0	50.0 / 8.3	44.0 / 7.2	38.0 / 6.2	32.0 / 5.3	26.0 / 4.1	19.7 / 3.1	14.0 / 2.1	7.4 / 1.1	0.0 / 0.0
3.5	N/A	43.0 / 20.4	37.4 / 17.3	31.5 / 14.2	26.0 / 11.2	20.2 / 8.1	15.0 / 5.0	10.3 / 2.5	4.1 / 1.0
7.0	N/A	43.8 / 15.4	37.8 / 13.2	32.3 / 11.0	26.4 / 8.8	20.5 / 6.6	15.0 / 4.4	10.0 / 2.2	3.6 / 0.8
14.0	N/A	43.0 / 11.7	37.5 / 10.1	31.9 / 8.34	25.6 / 6.67	19.8 / 5.0	13.9 / 3.3	8.5 / 1.7	2.5 / 0.5
28.0	N/A	43.7 / 9.0	37.5 / 7.7	31.9 / 6.4	25.7 / 5.1	19.5 / 3.9	13.0 / 2.6	7.5 / 1.3	0.5 / 0.1
NOTE: A MAG7 - MAG0 value of 3C hex represents a 1V slicer level at the point of receive data detection.									

APPLICATION INFORMATION

Introduction

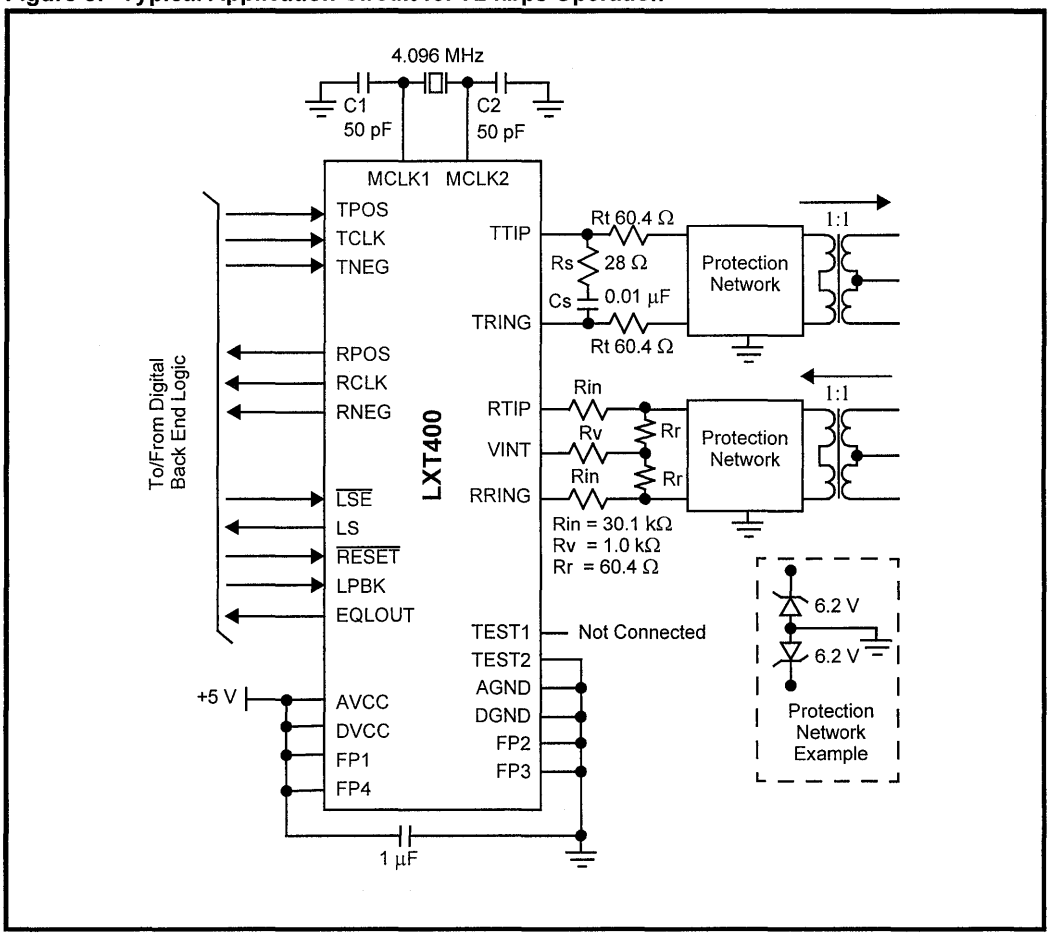
Figure 8 shows a typical LXT400 application circuit. A DSU crystal (4.096 MHz) is connected across MCLK1 and MCLK2, with two grounded loading capacitors. The line interface consists of a pair of 1:1 transformers, center-tapped on the line side, with appropriate load resistors. The Rs/Cs shunt network provides high frequency compensation for the transmit driver. The input signal is developed across the Rr/Rin network. Rv limits current into the low-impedance VINT driver during over-voltage conditions on the line. Table 8 lists external component recommendations.

Crosstalk

It is important to prevent crosstalk between the transmitter and receiver circuits. Steps were taken to reduce this interference inside the LXT400, but precautions must be taken with the line interface circuitry outside the chip as well. Crosstalk is especially high when the idle pattern (alternate positive and negative pulses) is being transmitted because the transmit power is concentrated around the Nyquist frequency (half the baud rate).

5

Figure 8: Typical Application Circuit for 72 kbps Operation



PCB Layout

The external line interface circuit must be laid out to minimize coupling of other digital and analog signals into RTIP and RRING (see Figure 9). These inputs, pins 2 and 3, are high impedance nodes which can pick up interference from adjacent PCB traces. The line interface circuit must be designed for loops with up to 50 dB of loss at the Nyquist frequency, even if the product will never be used on such long lines. When no receive signal is present, the LXT400 will switch to the highest gain filter, which at 56, 64 and 72 kbit/s produces an internal gain of about 50 dB. Unless precautions are taken, substantial interference coupling into RTIP and RRING could exceed the internal slicer levels and prevent the RLOS report. Layout considerations for LXT400 application circuits include:

1. Minimum PCB trace lengths between the LXT400 and the 4.096 MHz crystal and loading capacitors.
2. Minimum PCB trace lengths between resistors Rin and the RTIP and RRING pins. Shield these connections with ground traces.
3. Minimum PCB trace lengths between the receive transformer and the receive termination network.

Even with good PCB layout practices, RLOS reporting can be unreliable if the twisted pair line cable is not connected to the OCU or CSU/DSU when the LXT400 is set for operation at 56, 64, or 72 kbit/s. The unterminated receive lines can pick up enough noise to trip the data detectors and force RLOS Low. However, equipment designers can safely assume that the highest-gain filter with 50 dB of signal amplification will never be selected for normal operation on lines with up to 45 dB of attenuation at the Nyquist frequency. Therefore, the status word on the LS output can be used as a secondary LOS indicator - the occurrence of RLOS=0 and LL3-0 = 0111 at 56, 64 or 72 kbps reliably indicates the loss of carrier condition.

The 50dB filters were designed for applications in which the line attenuation is 48 dB or greater. The DDS specification requires an insertion loss at 56, 64, and 72 kbit/s of 43 dB or less. The LXT400 incorporates built-in headroom up to 45 dB. So for standard applications, the highest-gain filter will never be selected. The critical element is operating frequency. The highest gain filter (50 dB) is only available at 56, 64, and 72 kbit/s settings. At the lower operating frequencies, the highest-gain filter is about 44 dB, well above the interference levels arising from unterminated lines.

Figure 9: Suggested LXT400 PCB Layout

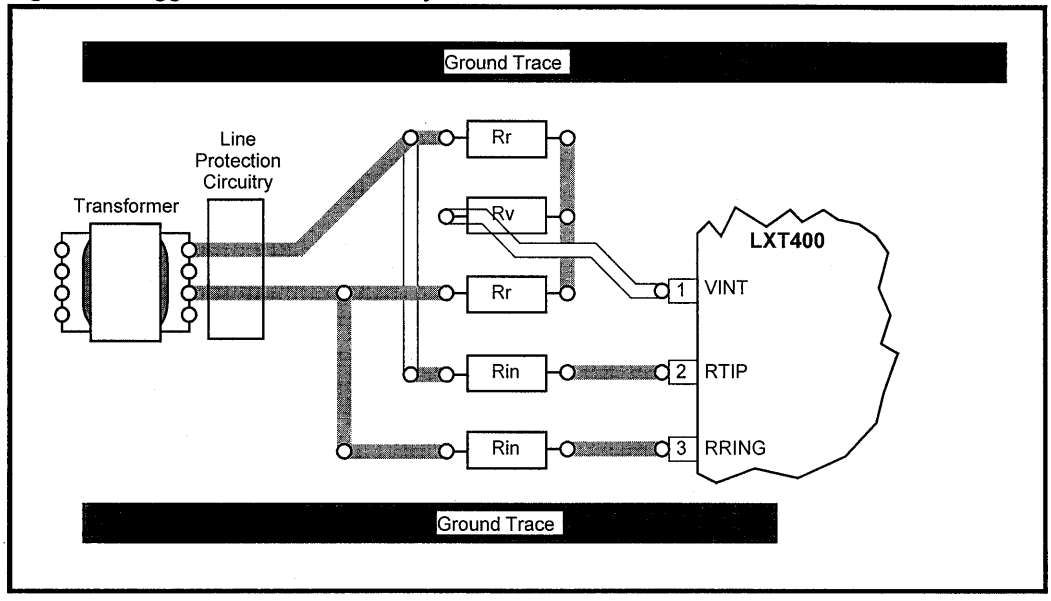


Table 8: External Component Recommendations

Component	Parameter	Recommended Value
Line Transformer	Turns ratio	1:1, ± 1%
	Structure	Center tapped (line side only)
Suggested Manufacturers	Primary Inductance	200 mH minimum
Midcom - Phone 800/643-2661	Leakage Inductance	22 to 43 µH maximum
Schott - Phone 615/889-8800	Interwinding Capacitance	350 pF maximum
	DC Resistance (Primary, Rwp)	7 to 15 Ω
	DC Resistance (Secondary, Rws)	7 to 15 Ω, See Rt, Rr calculation
Rin	Resistance, Tolerance, Rating	30.1 kΩ, ± 1%, 1/4 W
Rt, Rr	Resistance, Tolerance, Rating	(135 Ω - Rwp - Rws) / 2, ± 1%, 1/4 W
Rv	Resistance, Tolerance, Rating	1 kΩ, ± 5%, 1/4 W
DSU Crystal	Nominal frequency	4.096 MHz
	Holder style	HC-49/U
Suggested Manufacturers	Operating Mode	Fundamental, parallel resonant
Fox - Phone 813/693-0099	Load Capacitance	28 pF nominal
Monitor - Phone 815/432-5296	Tolerance	± 35 ppm @ 25 °C
	Range	± 50 ppm, -40 to 85 °C
	Aging	3 ppm per year maximum
	Maximum ESR	100 Ω
	Drive Level	1 mW maximum
DSU Crystal Loading Capacitors	Capacitance, Tolerance, Rating	50 pF, ±5%, 10 V
	Construction	NPO ceramic or equivalent
Transmit Shunt Network		
Rs	Resistance, Tolerance, Rating	28 Ω, ± 5%, 1/4 W
Cs	Capacitance, Tolerance, Rating	0.01 µF, ± 20%, 10 V

TEST SPECIFICATIONS

NOTE

The minimum and maximum values in Tables 9 through 13 and Figures 10 through 14 represent the performance specifications of the LXT400 and are guaranteed by test, except where noted by design.

Table 9: Absolute Maximum Ratings

Parameter		Minimum	Maximum	Units
DC Supply	AVCC referenced to AGND	-0.3	6.0	V
	DVCC referenced to DGND	-0.3	6.0	V
	DVCC referenced to AVCC	-0.3	0.3	V
	DGND referenced to AGND	-0.3	0.3	V
Input Voltage, any pin[1,2]		AGND - 0.3	AVCC + 0.3	V
Input or output diode current, any pin [2]		–	±20	mA
Continuous output current, any pin [2]		–	±25	mA
Continuous current, VCC or GND pins		–	±60	mA
Storage Temperature		-40	±150	°C

CAUTION

Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

1. TTIP and TRING are referenced to DVCC and DGND.
2. Except DC supply pins.

Table 10: Recommended Operating Conditions and Characteristics

Parameter	Sym	Min	Typ	Max	Units
DC supply	AVCC/DVCC	4.75	5.0	5.25	V
Ambient operating temperature	T_A	-40	–	85	° C

Table 11: DC Electrical Characteristics (Under Recommended Operating Conditions)

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Supply current (transmitting spaces)	I_{CC}	–	40	60	mA	270 Ω resistor across TTIP and TRING
Supply current (transmitting all marks)	I_{CC}	–	47.5	60	mA	270 Ω resistor across TTIP and TRING
Input Low voltage	V_{IL}	–	–	0.8	V	Digital inputs
Input High voltage	V_{IH}	2.0	–	–	V	Digital inputs

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 11: DC Electrical Characteristics (Under Recommended Operating Conditions) – continued

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Output Low voltage	V_{OL}	–	–	0.4	V	I_{OL} = 1.6 mA
Output Low voltage	V_{OL}	–	0.2	–	V	I_{OL} < 10 µA
Output High voltage	V_{OH}	2.4	–	–	V	I_{OH} = 0.4 mA
Output High voltage	V_{OH}	–	4.5	–	µA	I_{OH} < 10 µA
Input leakage current	I_{IL}	-40	–	40	µA	0 < V_{IN} < Vcc

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 12: AC Electrical Characteristics

Parameter		Sym	Min	Typ[1]	Max	Units
Input capacitance		C_{IN}	–	7	–	pF
TCLK jitter at DSU with respect to RCLK		t_{JIT}	–	–	2	% tpr at DSU
RCLK isochronous distortion at DSU		r_{JIT}	–	–	5	% tpt at OCU
Transmit output jitter with respect to TCLK		o_{JIT}	–	–	3	% tpt at DSU
Transmit pulse amplitude at TTIP/TRING 2	at 9.6 and 12.8 kbps	A_T	1.44	1.55	1.75	V
	at all other rates	A_T	2.56	2.74	2.92	V

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. The instantaneous peak amplitude of an isolated pulse (i.e. a mark between two spaces) into a 270 Ω resistive load.

Table 13: Timing Characteristics

Parameter		Sym	Min	Typ[1]	Max	Unit
Receive Timing Figure 10	RCLK period	t_{PR}	–	1/fb	–	ns
	RCLK pulse width High	t_{RWH}	1/ (2 fb) - 150	1/ (2 fb)	1/(2 fb)+150	ns
	RPOS/RNEG delay from RCLK rising edge[2]	t_{DP}	–	–	200	ns
	Transition time on any digital output[2]	t_{TO}	–	10	20	ns
Transmit Timing Figure 11	TCLK period	t_{PT}	–	1/ fb	–	µs
	TCLK pulse width High	t_{TWH}	400	–	–	ns
	TPOS/TNEG setup time to TCLK falling edge	t_{TSU}	200	–	–	ns
	TPOS/TNEG hold time from TCLK falling edge	t_{TH}	200	–	–	ns
	Transition time on any digital input	t_{TI}	–	–	40	ns
	TCLK frequency tolerance	f_{TTOL}	-50	0	+50	ppm

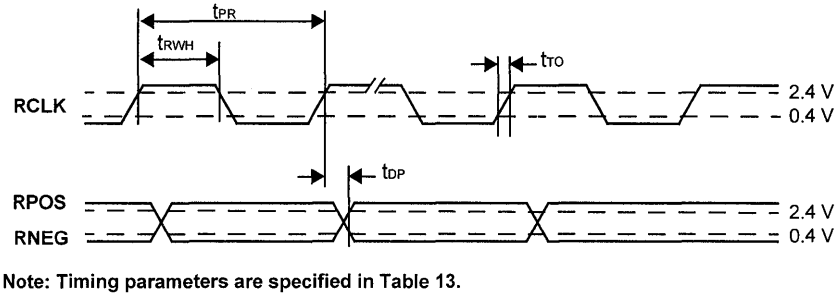
1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Measured with 15pf load.

Table 13: Timing Characteristics – continued

Parameter		Sym	Min	Typ[1]	Max	Unit
LS Serial Port Timing Figure 12 Figure 13	LS delay from RCLK falling edge[2]	t_{LSP}	–	–	200	ns
	$\overline{LSE}$ setup to RCLK rising edge	t_{LSU}	200	–	–	ns
	$\overline{LSE}$ hold time from RCLK rising edge	t_{LSH}	t_{RWH}	–	–	ns
	$\overline{LSE}$ Low to low Z state	t_{LZ}	–	–	100	ns
	$\overline{LSE}$ High to high Z state	t_{HZ}	–	–	100	ns
MCLK & $\overline{RESET}$ Timing Figure 14	MCLK1 input frequency	f_{MCLK}	–	4.096	–	MHz
	MCLK1 frequency tolerance	f_{MTOL}	-100	0	+100	ppm
	MCLK1 pulse width High	t_{MWH}	98	122	146	ns
	$\overline{RESET}$ pulse width Low	t_{RWL}	1000	–	–	ns

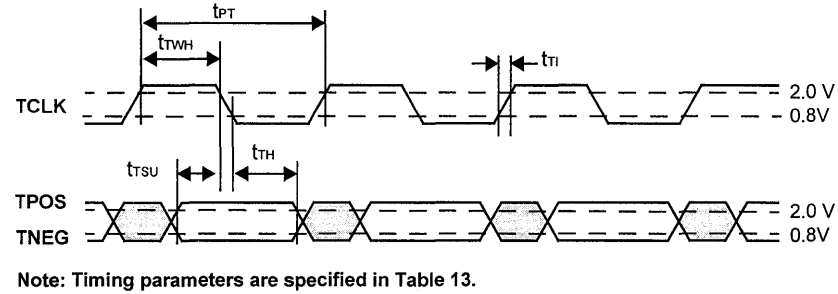
1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Measured with 15pf load.

Figure 10: Receive Digital Timing



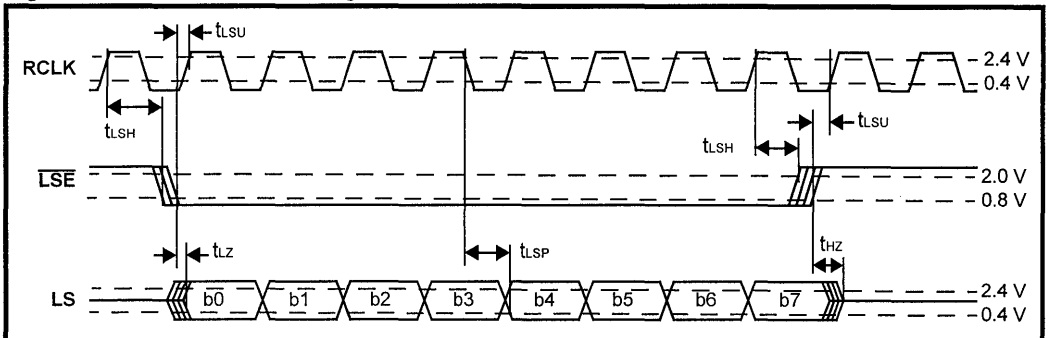
Note: Timing parameters are specified in Table 13.

Figure 11: Transmit Digital Timing



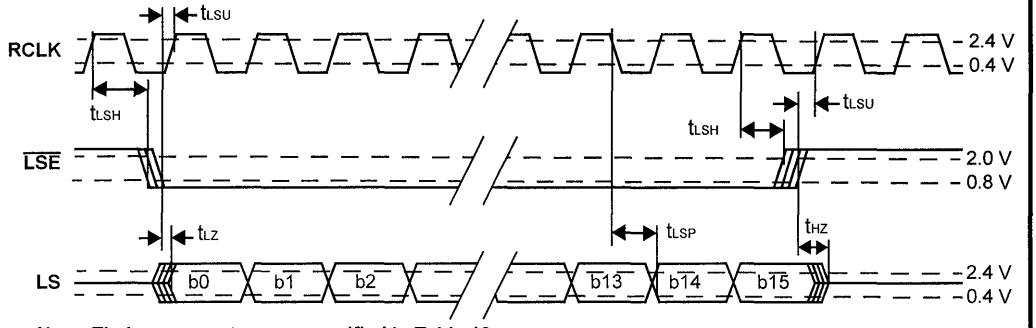
Note: Timing parameters are specified in Table 13.

Figure 12: LS Serial Port Timing - 8-Bit Word



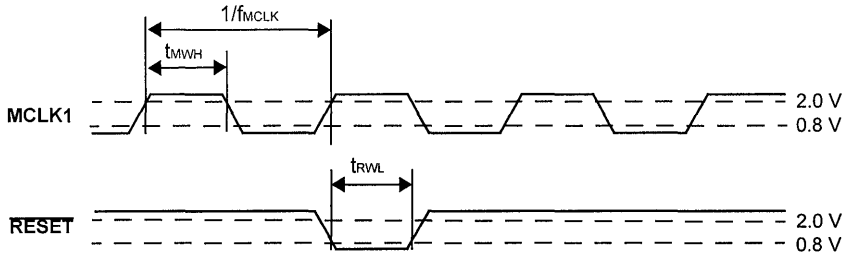
Note: Timing parameters are specified in Table 13.

Figure 13: LS Serial Port Timing - 16-Bit Word



Note: Timing parameters are specified in Table 13.

Figure 14: MCLK and RESET Timing



Note: Timing parameters are specified in Table 13.

NOTES

LXT441

APRIL 1997
Revision 1.1

Switched 56 / DDS Integrated DSU / CSU

General Description

The LXT441 is an integrated transceiver and data formatter for Switched 56 (SW56) and Digital Data Service (DDS) Data Service Unit/Channel Service Unit (DSU/CSU) and Office Channel Unit (OCU) applications.

The LXT441 line interface section performs transmit pulse shaping and receive signal data and timing recovery at the user-network 4-wire metallic interface. The device operates at loop speeds of 56 kbps and 72 kbps, supporting SW56, 56 kbps DDS with or without secondary channel (SC) and 64 kbps clear channel DDS services.

The integrated DSU circuit provides a DCE interface and connects directly to data terminal equipment (DTE) using standard EIA530 control leads. Data formatting includes DDS framing, control code handling, loop code generation and detection, and zero code suppression processing.

The LXT441 has an on-chip 8-bit microprocessor interface that simplifies device configuration, status reporting, and SW56 call processing, and may be used for parallel data transfer to and from the 4-wire physical link.

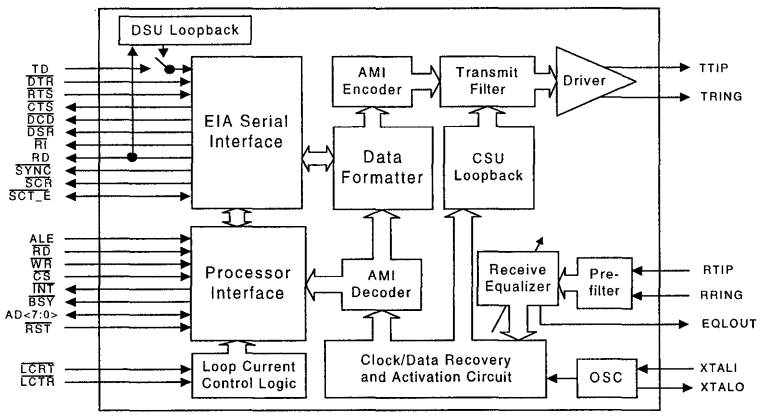
Features

- Supports most popular data rates for new DSU/CSUs
  - Switched 56 and 56 kbps DDS (DDS-PRI, 56 kbps loop speed)
  - 56 kbps DDS with secondary channel (DDS-SC, 72 kbps loop speed)
  - 64 kbps clear-channel DDS (CC-64K, 72 kbps loop speed)
- Switched 56 Call Control via EIA control leads or microprocessor
- Receiver performance monitoring
- Idle Code Transmission (CMI, DMI)
- Transmit timing recovered from network or supplied by system
- Network Control Code Detection and Generation
- CSU and DSU latching and non-latching loopbacks
- Available in 44-pin PLCC
- Single 8.192 MHz crystal or clock input
- 5V only CMOS process technology

Applications

- Leased-line DDS and Switched 56 DSU/CSUs
- Internet Service Provider (ISP) Equipment
- Internal DSU for Routers, Bridges and PC add-in cards
- Frame Relay Access Devices (FRAD)
- OCU Cards for Channel Banks and DLC Systems

LXT441 Block Diagram



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PIN ASSIGNMENTS AND SIGNAL DESCRIPTIONS

Figure 1: LXT441 Pin Assignments

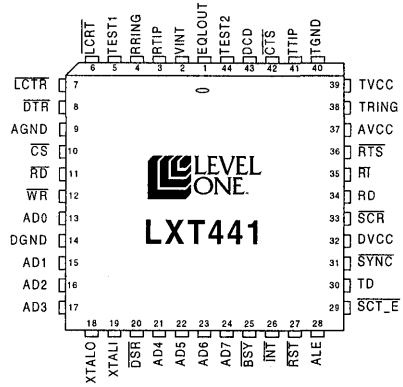


Table 1: LXT441 Microprocessor Interface Signal Descriptions

Pin	Symbol	I/O	Name / Description
10	$\overline{CS}$	I	**Chip Select**. Active Low. A Low on this pin enables the 8-bit parallel interface to perform read and write operations.
11	$\overline{RD}$	I	**Read**. Active Low. During read cycles, a Low on this pin turns on the internal drivers to present data to the 8-bit address/data bus.
12	$\overline{WR}$	I	**Write**. Active Low. During write cycles, a Low-to-High transition on this pin latches data present on the 8-bit bus into internal registers.
13 15 16 17 21 22 23 24	AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7	I/O	**Address Data Bus**. Multiplexed 8-bit parallel address data bus. These pins are used to access the read and write registers located within the LXT441.
25	$\overline{BSY}$	O	**Busy**. Active Low open-drain indication. Signal to host microcontroller that device has not completed read or write operation.
26	$\overline{INT}$	O	**Interrupt**. Active Low open-drain Interrupt. Signal to host microcontroller that an unmasked interrupt condition has been detected.
27	$\overline{RST}$	I	**Reset**. Active Low hardware reset pin. Must be pulsed Low on power-up to initialize all internal circuits. Must also be pulsed Low after changing the data rate setting, and after certain receive line conditions occur.
28	ALE	I	**Address Latch Enable**. When High, internal address latch is transparent. A High-to-Low transition latches the address present on pins AD<7:0>.

Table 2: LXT441 EIA Serial Interface Signal Descriptions

Pin	Symbol	I/O	Name / Description
8	$\overline{\text{DTR}}$	I	**Data Terminal Ready**. Active Low EIA signaling lead from DTE.
20	$\overline{\text{DSR}}$	O	**Data Set Ready**. Active Low EIA signaling lead to DTE.
29	$\overline{\text{SCT\_E}}$	I/O	**Extended Transmit Serial Clock**. Input or Output transmit clock dependent upon setting of TCCT control bit.
30	TD	I	**Transmit Data**. Transmit NRZ data from DTE.
31	$\overline{\text{SYNC}}$	O	**Word/Bit Synchronization**. 1-bit wide active Low output indicates word boundaries at DTE interface.
33	$\overline{\text{SCR}}$	O	**Receive Serial Clock**. Smooth 56 kHz for DDS-PRI, gapped 72 kHz (64 kHz) for DDS-SC and CC-64K.
34	RD	O	**Receive Data**. Receive NRZ data to DTE.
35	$\overline{\text{RI}}$	O	**Ring Indicator**. Indicates the presence of receive data (not control codes) when the receiver is in the control sequence mode (CALLMD = 1). Signifies incoming call for SW56 operation.
36	$\overline{\text{RTS}}$	I	**Request to Send**. Indicates a request by the DTE to transmit data. When High, CMI is transmitted on the line in DDS-PRI and DDS-SC. When this line goes High for a time greater than one byte period, the transmitter enters data mode for at least four byte periods.
42	$\overline{\text{CTS}}$	O	**Clear to Send**. Active Low EIA signaling lead indicates DCE readiness to transmit live data.
43	$\overline{\text{DCD}}$	O	**Data Carrier Detect**. Active Low EIA signaling lead indicating that the LIU receiver is fully operational; meaning that it is active, and that frame or bit sync is achieved, if enabled.

Table 3: LXT441 Line Interface Signal Descriptions

Pin	Symbol	I/O	Name / Description
1	EQLOUT	O	**Equalizer Monitor**. Must be left open when not used.
2	VINT	I	**Intermediate Voltage Reference**. Reference voltage used for internal analog circuits. This pin must be connected through a 1 kΩ resistor (Rv) to the center node between the two termination resistors, Rr, as shown in Figure 8.
3 4	RTIP RRING	I I	**Receive Tip and Ring**. Receive data input pair. RTIP and RRING are a fully differential input for the receive line interface.
6	$\overline{\text{LCRT}}$	I	**Loop Current Rx/Tx**. A Low input, supplied by an external current sensing circuit, indicates the presence of loop current flowing from the receive to the transmit twisted pair wires, and initiates a CSU loopback.
7	$\overline{\text{LCTR}}$	I	**Loop Current Tx/Rx**. A Low input supplied by an external current sensing circuit indicates the presence of loop current flowing from the transmit to the receive twisted pair wires.
38 41	TRING TTIP	O O	**Transmit Ring and Tip**. Differential driver outputs. Designed to drive 135Ω twisted-pair cable through transmit line interface shown in application diagram, Figure 8.

Table 4: LXT441 Miscellaneous Signal Descriptions

Pin	Symbol	I/O	Name / Description
39	TVCC	–	**Transmit Supply.** Line driver power supply.
40	TGND	–	**Transmit Ground.** Line driver ground.
9	AGND	–	**Analog Ground**. Reference for all analog LIU circuits except the transmit driver.
37	AVCC	–	**Analog Supply**. Line interface primary power supply.
18 19	XTALO XTALI	O I	**Crystal Oscillator**. The required 8.192 MHz master clock may be provided by a crystal connected across these pins, or by a digital clock connected to XTALI. If a clock is provided on XTALI, XTALO must be left unconnected.
14	DGND	–	**Digital Ground**. Ground reference for all internal digital circuitry.
32	DVCC	–	**Digital Supply**. Digital circuitry power supply.
5 44	TEST1 TEST2	I I	**Factory Test Pins**. *Leave unconnected.*

FUNCTIONAL DESCRIPTION

The LXT441 is comprised of five basic sections: receiver, transmitter, microprocessor interface, data formatter and back-end system serial interface.

The receive section includes pre-filters and line equalizers, and the timing recovery and data extraction blocks. An internal digital phase-locked loop (DPLL) is used in conjunction with the oscillator circuit to synchronize the recovered clock and data.

The transmit section includes a 50% AMI encoder, a programmable switched-capacitor low-pass filter, a low-pass notch filter, a transmit timing re-synchronizer and a continuous reconstruction filter. An on-chip CMOS driver is also incorporated to drive a 135Ω line through a coupling transformer.

The microprocessor block employs an 8-bit multiplexed parallel interface to transfer status and control information to and from the system host controller. This processor port connects to both Intel® multiplexed and Motorola® non-multiplexed controllers with a minimum of external 'glue' logic.

The system serial interface facilitates the connection of a DTE (data terminal equipment) device to the LXT441, which in turn behaves as a DCE (data communication equipment.) The LXT 441 uses 6 standard EIA530 control leads ($\overline{DTR}$, $\overline{RTS}$, $\overline{CTS}$, $\overline{DCD}$, $\overline{DSR}$ and $\overline{RI}$) for flow control, status reporting and SW56 signaling. The serial interface supports both DSU and OCU operation, with the transmit clock provided by either the recovered receive clock, or an external reference.

Initialization

A hardware reset ($\overline{RST}$) is required under any of the following circumstances:

- Initial power-up
- A change in Data Rate setting
- A change in the local analog loopback configuration
- A local change in the line upon which the transceiver is communicating (for example, configurations for changing lines in a "1 for n" redundancy scheme)
- The detection of an invalid line condition by the LXT441 receiver. (This will be indicated by either an XBPV or V_OFL interrupt.)

On receipt of the $\overline{RST}$ pulse, the LXT441 executes an iterative cycle of level detection and offset cancellation to select the appropriate equalizer settings for the received signal. When received data has a 50% ones density, full operation is achieved within one second after $\overline{RST}$. Under the minimum ones density condition specified in Table 5, full operation is achieved within eight seconds after $\overline{RST}$. Correct initialization assumes the presence of an AMI-coded signal at the RTIP and RRING inputs. The LXT441 will not correctly initialize unless a stable signal which meets the network interface specifications of AT&T Pub 62310 is present at the RTIP and RRING inputs during the entire initialization process. The RD output is not valid until full operation is achieved.

Table 5: Ones Density Requirements

Data Rate (kbps)	Minimum Average Ones Density
56.0	1/14
72.0	1/18

Automatic re-initialization may be triggered by changes in received signal strength as follows:

- If received signal strength increases by more than about 6 dB after full operation is achieved, automatic re-initialization occurs.
- If received signal strength decreases by more than about 4 dB, re-initialization occurs. If the decrease in received signal strength exceeds 6 dB, the LXT441 reports an LOS (Loss of Signal) condition and performs an automatic re-initialization.

The time required to achieve full operation after reinitialization, is the same as required for power-on initialization (i.e., 1 second max with 50% ones density, 8 seconds under minimum ones density conditions). Reinitialization is not triggered by impulse noise events.

Frame Alignment

When in DDS-SC or CC-64K modes, the LXT441 begins a frame alignment search at channel connection time. Channel connection time is defined as the time when the ACTIVE bit changes to a '1'.

The mean time to Frame Alignment is less than 5 ms. This means that, at 72 kHz on average, fewer than five frame comparisons are required to establish frame alignment.

Frame alignment is declared when the LXT441 detects three consecutive Frame Alignment Word (FAW) sequences matching the FAW. Detection of consecutive FAW sequences requires that each FAW sequence matches the FAW, and that each FAW sequence is exactly one frame apart.

Reception

RTIP and RRING inputs are differentially detected, then processed through the pre-filters and equalizer section. The continuous pre-filter removes high frequency noise and prevents aliasing problems for the line equalizers which follow. Receive pulses are reconstructed by the receive equalizer, which is comprised of a step equalizer stage and an adaptive decision feedback equalizer (DFE). The DFE eliminates residual inter-symbol interference (ISI) due to echoing by multiple bridged tap connections and time varying line characteristics such as temperature, humidity and age.

Clock Recovery

The clock recovery circuit uses a rate synchronizer to generate a high frequency internal clock from the oscillator input. A DPLL is used to synchronize this internal clock to the received data pulses. The output clock from the DPLL is divided down to generate $\overline{SCR}$ and all other required clocks (except $\overline{SCT\_E}$ when it is supplied as an external input).

Data Extraction

The data extraction block delivers raw recovered bipolar line data to the data formatter and decoder so that it may output the NRZ RD stream to the EIA interface and the receive EIA microprocessor register. A positive or negative differential pulse received between RTIP and RRING results in a logic 1 sent to the formatter, while no pulse is reported to the formatter as a logic 0. After decoding in the formatter section, the final RD output at the received data rate is valid on the falling edge of $\overline{SCR}$.

Receiver operation is not affected by the data patterns, provided the ones density requirements of Table 5 are met, and the receive line signal contains at least one valid pulse every 26 bit periods. Loss of signal is declared after 32 consecutive zeros. However, the $\overline{SCR}$ output remains synchronized to the RTIP/RRING input for up to 40 consecutive zeros, after which re-initialization occurs. Spurious bipolar violations (due to channel noise, etc.), will not adversely affect long term LXT441 data reception.

Receiver Bipolar to NRZ Conversion

The receiver converts Bipolar data into NRZ data in the following manner:

- Bipolar B's are marks (of alternate polarity with respect to last mark) converted to NRZ 1s.
- Bipolar V's are marks (of same polarity with respect to last mark) converted to NRZ 1s.
- Bipolar O's are spaces converted to NRZ 0s.

This conversion process takes 1 byte plus 1 bit period, with corresponding NRZ data available 8 bit periods after the Bipolar data is received. There are, however, a few exceptions to this. Reception of the DSU Loopback control code and reception of the Zero Suppression control code require that a code replacement be performed upon the received data prior to conversion to NRZ format. See Table 28 for RX_DLP & RX_ZSC code replacement.

In DDS-SC mode, there are no violations. Thus, the receiver only converts O's and B's (bipolar data) to NRZ 0s or 1s respectively. Frame synchronization must be established to enable network code detection. Reception of the DSU Loopback code requires a code replacement operation to be performed prior to conversion to NRZ format. See Table 28 for R_DLP code replacement.

CC-64K mode is very much the same as DDS-SC mode. There are no byte replacements, and the only code is idle data (RX_DMI). See Table 28 for control codes & replacement policy for various modes.

Receiver Code Detection

The receiver converts bipolar received data into NRZ data. In DDS-PRI mode, this process requires bipolar violation (BPV) detection, valid/invalid BPV detection, and control code detection. A violation is detected upon receipt of Bipolar data which violates the Alternate Mark Inversion (AMI) Rule. A BPV is valid if, and only if, it belongs to a 7-bit Control Code, satisfying the following set of criteria:

- At least seven bit periods have passed without a violation since receipt of the violation in question.
- An odd number of B's (non-violation marks) were received since the last violation.
- The bit received prior to the violation was an O (a space).

Control Code Detection

The data presented at the RTIP/RRING pins undergoes bipolar to NRZ conversion, with automatic detection and decoding of control codes according to the following criteria:

- Detection of Idle (CMI), OOS, and OOF codes in DDS-PRI mode.
- Detection and conversion of DSU Loop code in DDS-PRI mode, and DSU Loop control code in DDS-SC mode.
- Detection of DDS-SC control codes for DDS-SC mode.
- Detection of the DDS-SC six-bit frame pattern for byte alignment of data and control streams for DDS-SC mode, and 8-bit data for CC-64K mode.
- Control of EIA handshake signals based on receiver status from the line interface unit.

All control codes except RX_DMI are encoded into valid BPVs. Thus, upon receipt of a valid BPV, control codes are decoded (as listed in Table 28). Any valid BPV which doesn't match a control code listed in the table results in an 'unmatched' code. The exception, RX_DMI, is detected when an all-marks (all B's and no V's) code is received. All control codes remain active for 7 bit periods after detection.

Bipolar received codes in both DDS-SC and CC-64K modes contain no violations. Therefore, data must be synchronized with the frame pattern, to establish the beginning of each word. The C/S bit is used to determine whether the unit is receiving network codes or data. When two of three consecutive C-bits are 0s the network code detector is enabled which tests if the data matches any of the control codes listed in Table 27. When two of three consecutive C-bits are 1s the unit reverts to data mode.

Loss of Frame Alignment

The LXT441 declares loss of frame alignment when it receives five consecutive Frame Alignment Word (FAW) sequences in error. Here, consecutive FAW sequences implies that each FAW sequence is expected to occur an integral number of frames after the FAW sequence which produced alignment. The initial alignment algorithm is the same as the frame recovery algorithm.

Recovery of Frame Alignment

The LXT441 begins recovery of frame alignment immediately after detecting loss of frame alignment. Frame Alignment Recovery is identical to the initial Frame Alignment search process described under Initialization.

Changes in Received Signal Strength

During initialization, the LXT441 selects filters appropriate to the strength of the received signal. After initialization, the LXT441 continually monitors the receive signal strength to ensure the optimum signal/filter match. Data reception is not affected by impulse noise events or by slow changes in signal amplitude caused by normal temperature and humidity variations (The maximum constant rate of change which the LXT441 can track is 6 dB per minute.) However, instantaneous "step" changes (see Figure 2) may temporarily interfere with data reception. Step changes may be caused by sudden changes in loop attenuation, far end transmitter output, etc.

After normal operation has been established, an instantaneous single-step change may cause one of three conditions, as shown in Figure 3.

Under Condition 1, the LXT441 automatically adapts to minor step changes in signal strength (assuming that the new input is a valid DDS signal).

Under Condition 3, the LXT441 responds to significant step changes by re-initializing.

Condition 2, while unlikely to occur in an actual DDS implementation, may be observed in the laboratory when working with artificial line simulators. Condition 2, which results from a 6 - 20 dB step increase in received signal strength, may result in a signal/filter mismatch. This condition is characterized by excessive bipolar violations (BPVs). Excessive BPVs which are not valid code words are detected and counted by the LXT441. The XBPV interrupt flag will be set when excessive BPVs are detected by the LXT441 receiver. The device should be reinitialized via the application of a valid $\overline{RST}$ pulse in the presence of excessive BPVs.

Under normal operating conditions, step changes in received signal strength are all under local control. Thus, the user can reset the LXT441 once the new receive signal has stabilized at the chip inputs. Remote changes typically involve disconnecting one line and re-connecting another line of different length. These changes trigger the RLOS report and automatic re-initialization.

Receive Loss of Signal

Receive loss of signal (RLOS) is detected when more than 32 consecutive zeros are received, caused either by a true loss of signal, or a signal strength drop greater than 6 dB. The LXT441 automatically re-initializes when RLOS is present, and 40 consecutive zeros are counted. Figure 4 shows the RTIP/RRING input and RLOS control bit timing relationships for a true loss of signal. When signal energy returns to the chip input, the LXT441 executes one full activation cycle in the presence of this signal. The result is that RLOS will remain active for a period of time (0.13 s < tH < 16 s) after signal energy reappears.

Figure 5 shows the RTIP/RRING input timing and RLOS output timing relationship for a signal strength decrease greater than 6 dB. In this case, RLOS will go High for a time 0.26 s < tP < 16 s.

Figure 2: Step Changes in Receive Signal Strength = 20 $\log_{10}$ ($^{A2}/_{A1}$) dB

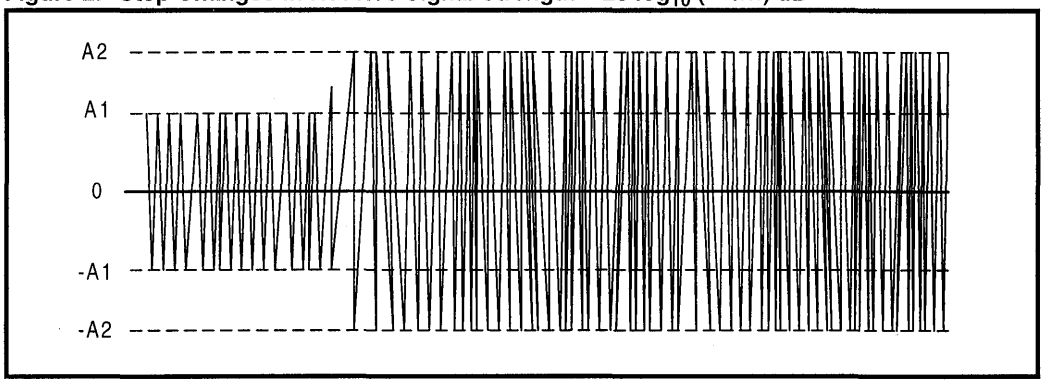
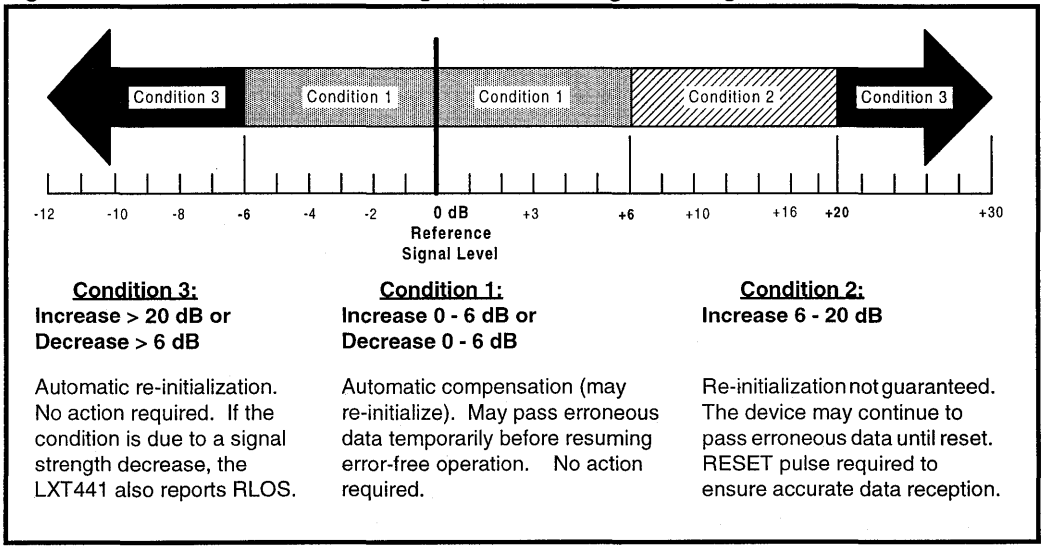


Figure 3: Conditions Based on Changes in Receive Signal Strength



Condition 3:
Increase > 20 dB or
Decrease > 6 dB

Automatic re-initialization. No action required. If the condition is due to a signal strength decrease, the LXT441 also reports RLOS.

Condition 1:
Increase 0 - 6 dB or
Decrease 0 - 6 dB

Automatic compensation (may re-initialize). May pass erroneous data temporarily before resuming error-free operation. No action required.

Condition 2:
Increase 6 - 20 dB

Re-initialization not guaranteed. The device may continue to pass erroneous data until reset. RESET pulse required to ensure accurate data reception.

Figure 4: RLOS Timing for a True Loss of Signal

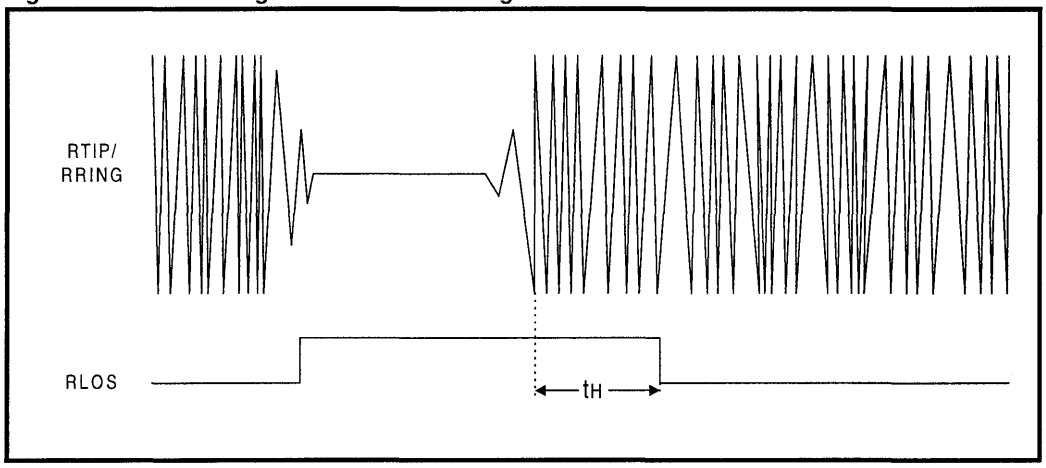
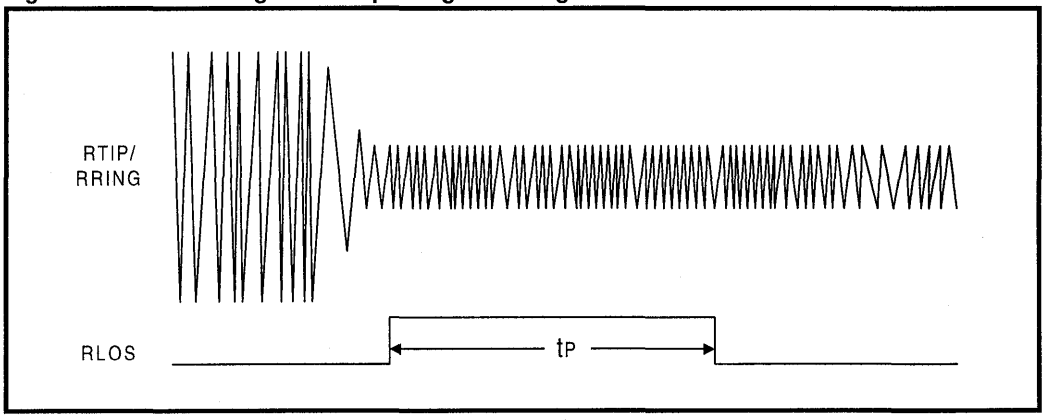


Figure 5: RLOS Timing for a Drop in Signal Strength > 6 dB



Transmission

Transmit data (TD) from the DTE is sampled on the rising edge of $\overline{SCT\_E}$. The transmit section generates a 50% AMI pulse according to the pulse encoding rules, which is synchronized with the $\overline{SCT\_E}$ input/output clock. In DSU applications with TCCT=0, $\overline{SCR}$ is typically routed back out of the $\overline{SCT\_E}$ input/output pin to serve as a transmit demand clock. If EIAREG=1, then data at the serial interface is ignored, and the Transmit EIA 8-bit microprocessor register is used as the source of transmit data.

Once the transmit data is sampled and encoded, resulting AMI output pulses are processed through a set of frequency dependent filters. Initial filtering at all rates is accomplished by a programmable, switched-capacitor, low-pass filter. This filter is a single-pole type with the pole set at 1.3 times the bit rate (as determined by control bits MODE0 and MODE1.) A continuous filter, common to all data rates, is the final stage. The continuous filter removes high frequency components which remain after processing by the low-pass filter stages. The resulting transmit pulses are then applied to the line driver for transmission onto the twisted-pair line.

Transmit Serial Interface

User data presented at the TD pin undergoes NRZ to bipolar conversion, with automatic generation of zero suppression code for DDS-PRI. In DDS-PRI mode, controlled generation of Control Mode Idle (CMI), and Data Mode Idle (DMI) may be accomplished by manipulating the $\overline{DTR}/\overline{RTS}$ control leads, or by writing to the TX_CMI or TX_DMI control bits. The microprocessor control bits take precedence over the $\overline{DTR}/\overline{RTS}$ for commanding CMI/DMI transmission.

In DDS-SC and CC-64K modes, controlled generation of the DDS-SC control codes may be selected, and the six-bit frame pattern is automatically inserted into the transmitted data stream.

Transmit timing is derived from the receive clock for a loop timed DSU/CSU, or from the $\overline{SCT\_E}$ input for tail-circuit loop timing, or in OCU applications.

Transmit NRZ to Bipolar Conversion

The Transmitter converts NRZ data and control codes into bipolar transmitted data. It is possible that several control codes are requested for transmission, thus a priority encoder must resolve which code should be transmitted; if no control code is requested, the transmitter sends out converted NRZ data (see Table 28 for priority of transmit control codes). The position of injected code words is set arbitrarily by a free-running internal bit counter. In DSU operation without a 'tail-circuit' (TCCT=0), the transmit word position is aligned to the receive word position. In DDS-SC and CC-64K modes, the receive word position is determined by the receive frame pattern, while in DDS-PRI mode, the receive word position is arbitrary.

In DDS-PRI MODE, code injection must take into account the polarity of the last transmitted mark (B or V), and whether an even or odd number of B's have been sent since the last V. The first criterion is used to assure that violations are transmitted correctly. The second criterion assures that any X's will be transmitted correctly - as O or B to maintain an odd number of B's since the last V.

In DDS-SC and CC-64K modes, code injection is accompanied by the injection of a frame pattern as the 8th bit of every outgoing data byte or code word. When no code is requested, the transmitter simply converts NRZ 0s and 1s into Bipolar O's and B's, respectively, and injects the frame bit at the proper location. See Table 28 for control codes in DDS-SC and CC-64K modes.

Transmit Code Generation

CONTROL-MODE-IDLE (CMI) can be generated from a logic-Low on EIA handshake signal $\overline{RTS}$ in DDS-PRI mode and DDS-SC mode.

Clear-To-Send ($\overline{CTS}$) goes High after receiving a Request-To-Send ($\overline{RTS}$) with delay based upon the time required to transmit the last complete CMI code, plus three idle data bytes.

DSU Loopback Code Generation in an OCU Application

If the TX_DLP control is set (register WR2-bit 6), then the controls which normally force transmission of CMI will now force transmission of DSU Loopback Code (DLP). The user can inject test data by pulling $\overline{RTS}$ High, and waiting for $\overline{CTS}$ High; indicating the end of a DLP byte and the start of a test data byte. In this case, the $\overline{RTS}$-to-$\overline{CTS}$ delay is not three to four bytes, but is less than one byte.

Loopback Operation

The LXT441 incorporates both a CSU loopback and a DSU loopback.

CSU Loopback

When the $\overline{\text{LCRT}}$ pin is set Low, a CSU loopback is engaged, with the recovered line data and clock being sent back through the transmit section and onto the line interface, as well as being output on the RD and $\overline{\text{SCR}}$ pins. TD and $\overline{\text{SCT\_E}}$ inputs are ignored in the loopback mode.

DSU Nonlatching Loopback

A nonlatching loopback operates upon receipt of a minimum of four consecutive bytes of the specified loopback code at the proper data rate, and continues for a minimum of four consecutive bytes after receipt of the last loopback code. The loopback is terminated upon receipt of five successive byte intervals without the loopback code (refer to Table 28 for the DSU-Loopback codes for all data rates). The four consecutive bytes must be contiguous; having no "filler" bits between DLP code bytes. In DDS-PRI operation, a loopback code byte is a 7-bit word, and in DDS-SC and CC-64K operation, a loopback code byte is an 8-bit word, with a ninth framing bit injected between the 7th and 8th bits of the code word.

System Serial Interface and Data Formatting

The LXT441 provides a EIA DCE serial interface with TD, RD, $\overline{\text{SCT}}$/$\overline{\text{SCT\_E}}$, $\overline{\text{SCR}}$, $\overline{\text{DTR}}$, $\overline{\text{RTS}}$, $\overline{\text{DSR}}$, $\overline{\text{DCD}}$, $\overline{\text{RI}}$, & $\overline{\text{CTS}}$ pins for attaching data terminal equipment (DTE). The signal levels are TTL/CMOS compatible, allowing a direct connection to Serial Communication Controllers (SCC), while connection to external terminals require standard V.35/RS449 transceivers. User data for transmission undergoes processing in the data formatter to insert required zero suppression codes for DDS-PRI, and framing information for DDS-SC and CC-64K. Receive line data has zero suppression codes removed from DDS-PRI streams, while the framing bits are stripped from DDS-SC and CC-64K data. Secondary channel bits are passed to the RD and TD pins in DDS-SC, allowing transparent secondary channel processing. Refer to Figures 6 and 7 for EIA interface data structure and relative timing. For specific timing parameters, refer to Test Specifications.

Device Configuration

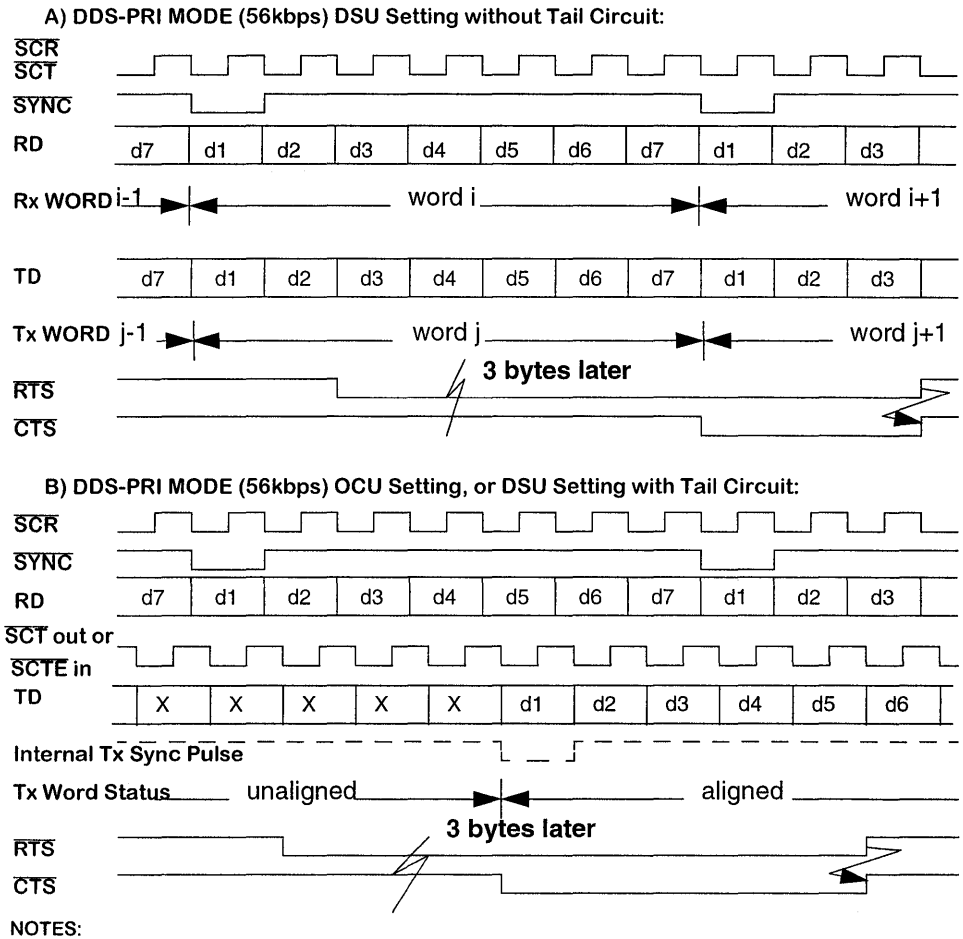
The user can select the operating mode and loop rate (DDS-PRI, DDS-SC, CC-64K) by writing the appropriate values to control bits MODE0 and MODE1.

Transmit timing modes are selected by configuring bits OCU and TCCT. Switched 56 call flow control is performed using either the EIA handshake lines or the microprocessor port. In DDS-SC mode, the secondary channel bandwidth is available transparently by interpreting transmit and receive data in relation to the $\overline{\text{SYNC}}$ signal.

Switched 56 Call Control

Switched 56 call control is performed between OCU and DSU by the interpretation of CMI and DMI codes sent from one end-point to the other. These codes correspond to 'on-hook' and off-hook' conditions on the metallic trunk. Refer to the TIA/EIA-596 specification for specific signalling and timing requirements. The DSU 'dials' a call by seizing the trunk, waiting for a valid network 'wink' and then sending alternating CMI/DMI sequences which are interpreted as dial digits, much in the manner of pulse dialing. The DSU 'answers' a call by detecting non-CMI data from the OCU. CMI/DMI detection is performed by the LXT441 and may be monitored via the host controller. CMI/DMI transmission may be accomplished using either the $\overline{\text{RTS}}$ signal or the TXCODE register.

Figure 6: EIA Interface Data Structure & Timing - DDS-PRI Mode



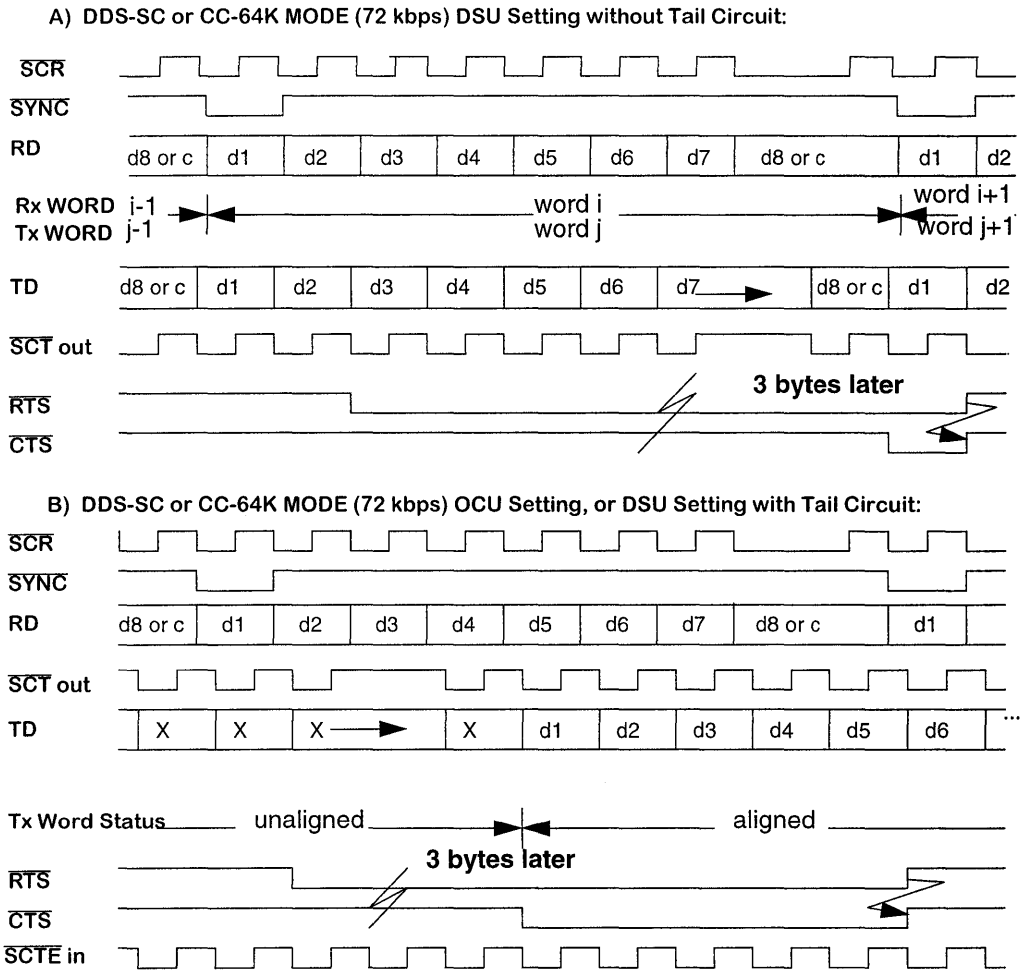
NOTES:

In DDS-PRI Mode when OCU= 0 and TCCT = 0, $\overline{SCR}$ and $\overline{SCT\_E}$ are output clocks with identical bit phase. The $\overline{SYNC}$ pulse indicates both the Transmit and Receive word positions. When $\overline{RTS}$ is pulled Low, $\overline{CTS}$ will go Low at the beginning of the fourth following transmit word position.

In DDS-PRI Mode when OCU = 1 and TCCT = 0, $\overline{SCR}$ and $\overline{SCT\_E}$ are output clocks having arbitrary relative phase. The transmit word alignment may be detected by the DTE by asserting $\overline{RTS}$ and observing the transmit bit period in which CTS goes Low.

In DDS-PRI Mode when TCCT = 1, $\overline{SCR}$ is an output, and $\overline{SCT\_E}$ is the transmit serial clock input with arbitrary phase position. Again, the DTE may detect the transmit word position by using the $\overline{RTS}$ and $\overline{CTS}$ lines.

Figure 7: EIA Interface Data Structure & Timing - DDS-SC or CC-64K Mode



NOTES:

In DDS-SC or CC-64K Modes the serial clock outputs SCR and SCT are each "gapped" 72 kHz clocks with an aggregate rate of 64 kHz. The single-period "gap" occurs during the 'd7' bit position.

In configurations with TCCT=1, the SCTE input must be a 72 kHz. 'smooth' (ungapped) clock, and the transmit word position is determined using RTS and CTS.

APPLICATION INFORMATION

Design Considerations

Figure 8 shows a typical LXT441 application circuit. A DSU crystal (8.192 MHz) is connected across XTALI and XTALO, with two grounded loading capacitors. The line interface consists of a pair of 1:1 transformers, center-tapped on the line side, with appropriate load resistors. The Rs/Cs shunt network provides high frequency compensation for the transmit driver. The input signal is developed across the Rr/Rin network. Rv limits current into the low-impedance VINT driver during over-voltage conditions on the line.

The DTE is connected to the LXT441 EIA interface. NRZ data is required at TD and RD, so level conversion is required for standard bipolar signals such as V.35 and RS-232. Device configuration pins may be tied to Vcc or GND, or may be supplied with logic inputs from an external control circuit. Figure 9 provides details of typical protection and current sensing circuits. Table 6 lists external component recommendations. Refer to the following documents for DDS electrical specifications:

- ANSI T1.410 - 1992
- AT&T TR 62310 - 1993

Microprocessor Interfacing

The microprocessor interface is an 8-bit parallel port with multiplexed address/data pins and associated bus control signals. Interfacing to Motorola, Intel and Zilog controllers may be accomplished with a minimum of glue logic by following the guidelines below, and observing the timing parameters in Figures 11 and 12.

$\overline{CS}$ does not have to be asserted before ALE transitions Low, latching the address present on the multiplexed address/data bus.

The $\overline{INT}$ signal is cleared to inactive High following a read of the Interrupt Status register at address 08h.

BSY Operation

$\overline{BSY}$ indicates stable data available for read on $\overline{RD}$ cycles, and the proper internal latching of data on write cycles. Consecutive write cycles require that $\overline{BSY}$ goes inactive High before the next write. $\overline{BSY}$ may be used to 'stretch' the RD strobe. RD should not go High before $\overline{BSY}$ goes inactive High.

Crosstalk

It is important to prevent crosstalk between the transmitter and receiver circuits. Steps were taken to reduce this interference inside the LXT441, but precautions must be taken with the line interface circuitry outside the chip as well. Crosstalk is especially high when the idle pattern (alternate positive and negative pulses) is being transmitted because the transmit power is concentrated around the Nyquist frequency (half the baud rate).

PCB Layout

The external line interface circuit must be laid out to minimize coupling of other digital and analog signals into RTIP and RRING (see Figure 8.) These inputs, pins 3 and 4, are high impedance nodes which can pick up interference from adjacent PCB traces. The line interface circuit must be designed for loops with up to 50 dB of loss at the Nyquist frequency, even if the product will never be used on such long lines. When no receive signal is present, the LXT441 will switch to the highest gain filter, which produces an internal gain of about 50 dB. Unless precautions are taken, substantial interference coupling into RTIP and RRING could exceed the internal slicer levels and prevent the RLOS report.

Layout considerations for LXT441 application circuits include:

- Minimum PCB trace lengths between the LXT441 and the 8.192 MHz crystal and loading capacitors.
- Minimum PCB trace lengths between resistors Rin and the RTIP and RRING pins. Shield these connections with ground traces.
- Minimum PCB trace lengths between the receive transformer and the receive termination network.

Even with good PCB layout practices, RLOS reporting can be unreliable if the twisted pair line cable is not connected to the OCU or CSU/DSU. The unterminated receive lines can pick up enough noise to trip the data detectors and cause an inaccurate RLOS reading. However, equipment designers can safely assume that the highest-gain filter with 50 dB of signal amplification will never be selected for normal operation on lines with up to 45 dB of attenuation at the Nyquist frequency.

The 50 dB filters were designed for applications in which the line attenuation is 48 dB or greater. The DDS specification requires an insertion loss at 56 and 72 kbps of 43 dB or less. The LXT441 incorporates built-in headroom up to 45 dB. So, for standard applications, the highest-gain filter will never be selected.

Power Supply Decoupling

Each +5V input should be tied to the same power plane, and each should be bypassed by a 0.47 µF decoupling capacitor. The bypass caps should be located as closely as possible to the device power and ground pins.

Figure 8: Typical LXT441 Application

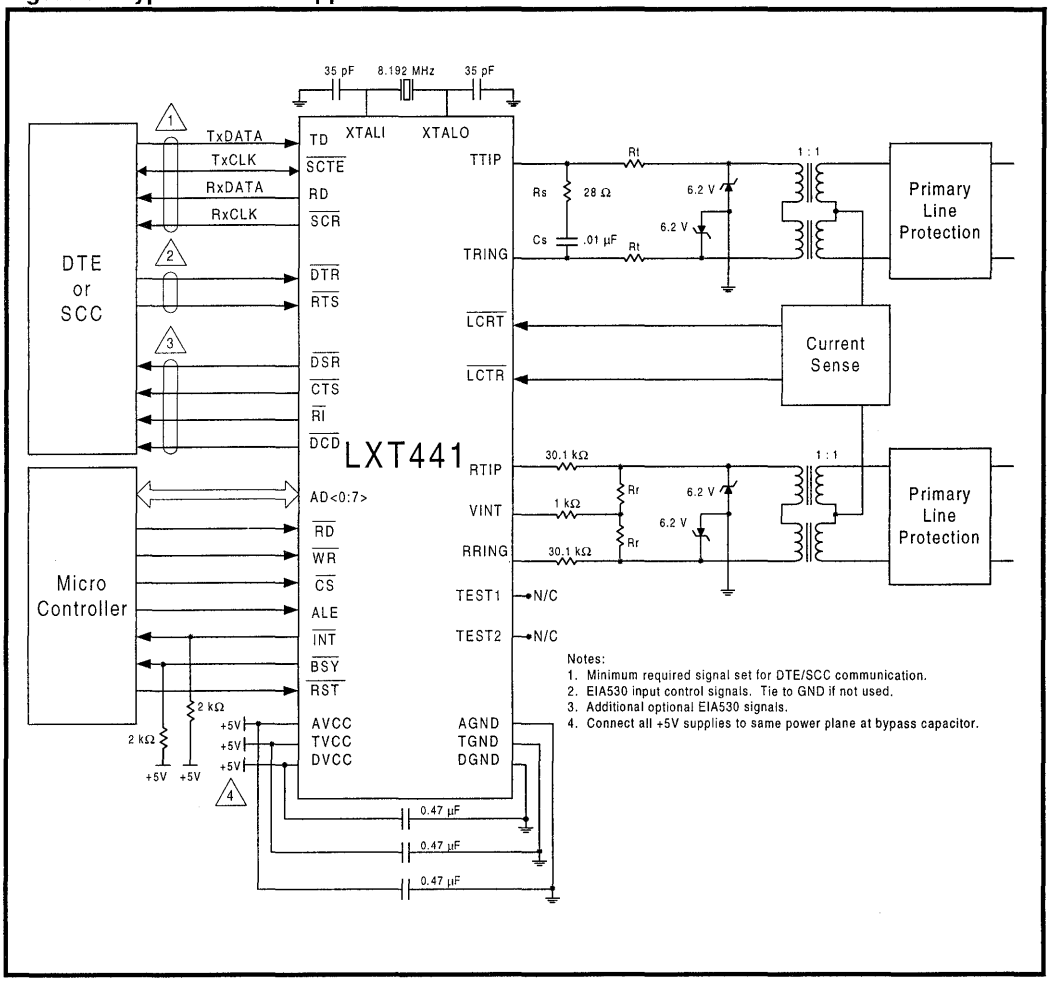
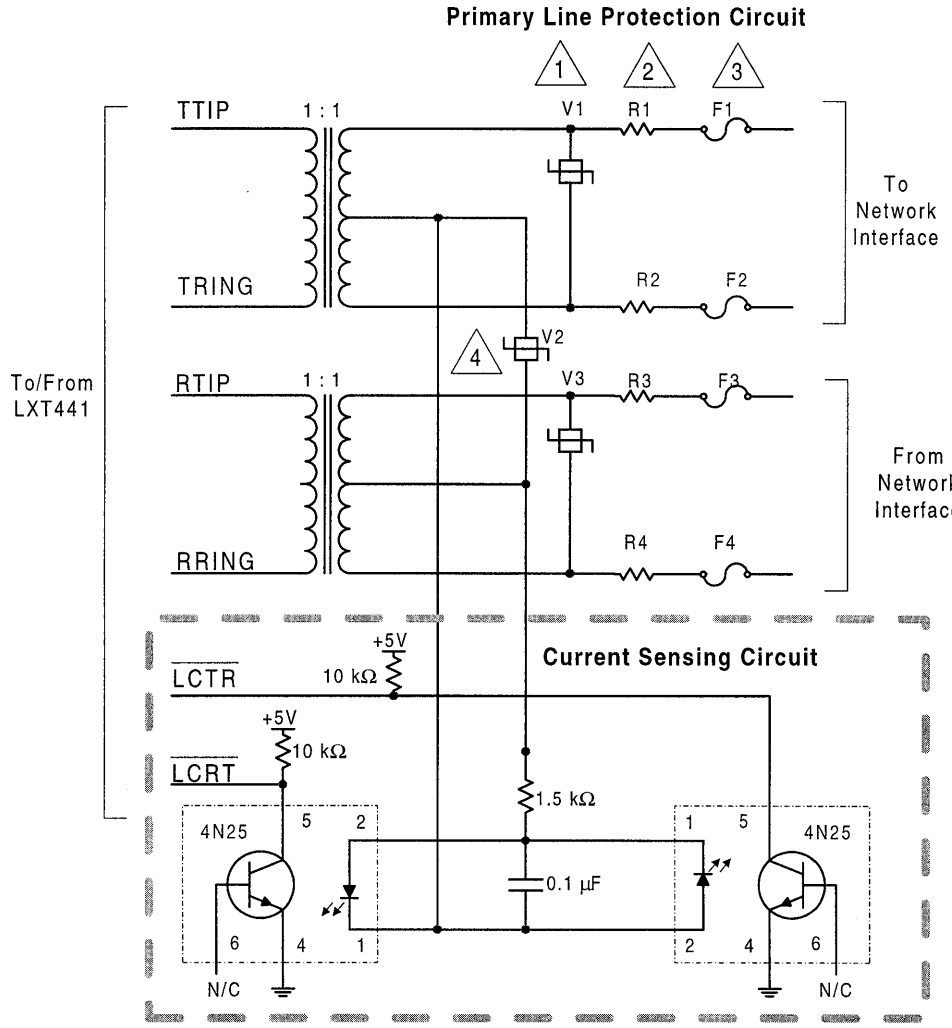


Figure 9: Typical Primary Line Protection and Current Sensing Circuits



Notes:

1. V1, V3 provide secondary overvoltage protection. Turn on above ≈ 3V
2. R1 - R4 are current limiting resistors. One per Rx/Tx pair is sufficient. Two per pair provide impedance symmetry.
3. F1 - F4 provide series current protection. One per Rx/Tx pair is sufficient. Two per pair provide impedance symmetry.
4. V2 provides pair-to-pair overvoltage protection. Turn on above ≈ 30V.

Table 6: External Component Recommendations

Component	Parameter	Recommended Value	
		LXT400 Compatible	LXT441 Only
Line Transformer Suggested Manufacturers: Midcom (800) 643-2661 B and H (612) 894-9590 Vitec (209) 651-1535	Turns ratio	1:1, ± 1%	1:1, ± 1%
	Structure	Center tapped (for line side)	Center tapped (for line side)
	Primary Inductance	200 mH minimum	40 mH minimum
	Leakage Inductance	22 to 43 µH maximum	43 µH maximum
	DC Resistance (Primary, Rwp)	7 - 17 Ω	8 Ω maximum (6Ω ± 10% preferred)
	DC Resistance (Secondary, Rws)	7 - 17 Ω	8 Ω maximum (6Ω ± 10% preferred)
	Interwinding Capacitance	350 pF maximum	80 pF maximum
Rin	Resistance, Tolerance, Rating	30.1 kΩ, ± 1 %, ¼ W	
Rt, Rr	Resistance Calculation, Tolerance, Rating	(135 Ω - Rwp - Rws)/2, ± 1%, ¼ W [1]	
Rv	Resistance, Tolerance, Rating	1 kΩ, ± 5%, ¼ W	
DSU Crystal	Nominal frequency	8.192 MHz	
	Holder style	HC-49/U	
	Operating Mode	Fundamental, parallel resonant	
	Cut	AT	
	Load Capacitance	22 pF nominal (excluding crystal C0)	
	Tolerance	± 35 ppm @ 25 °C	
	Range	± 50 ppm, -40 to +85 °C	
	Aging	3 ppm per year maximum	
	Maximum ESR	100 Ω	
	Drive Level	1 mW maximum	
DSU Crystal Loading Capacitors	Capacitance, Tolerance, Rating	35 pF, ± 5 %, 10 V	
	Construction	NPO ceramic or equivalent	
Transmit Shunt Network			
Rs	Resistance, Tolerance, Rating	28 Ω, ± 5 %, ¼ W	
Cs	Capacitance, Tolerance, Rating	0.01 µF, ± 20 %, 10 V	

1. Rwp = Primary winding resistance + resistance of series current limiting resistors and series protection devices.

5

TEST SPECIFICATIONS

NOTE

The minimum and maximum values in Tables 7 through 11 and Figures 10 through 12 represent the performance specifications of the LXT441 and are guaranteed by test, except where noted by design

Table 7: Absolute Maximum Ratings

Parameter		Symbol	Min	Max	Units
Supply Voltage	AVCC referenced to AGND	V_{CC}	-0.3	6	V
	DVCC referenced to DGND	V_{CC}	-0.3	6	V
	TVCC referenced to TGND	V_{CC}	-0.3	6	V
Supply Variation	AVCC referenced to DVCC	V_{CCV}	-0.3	0.3	V
	DVCC referenced to TVCC	V_{CCV}	-0.3	0.3	V
	AVCC referenced to TVCC	V_{CCV}	-0.3	0.3	V
Ground Variation	AGND referenced to DGND	G_{NDV}	-0.3	0.3	V
	DGND referenced to TGND	G_{NDV}	-0.3	0.3	V
	AGND referenced to TGND	G_{NDV}	-0.3	0.3	V
Input voltage, any pin[1, 2]		-	AGND - 0.3	AVCC + 0.3	V
Input or output diode current, any pin[2]		-	-	±20	mA
Continuous output current, any pin[2]		-	-	±25	mA
Continuous current, any VCC or GND pin		-	-	±50	mA
Storage Temperature		T_{ST}	-50	150	°C

CAUTION

Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

1. TTIP and TRING are referenced to DVCC and DGND.
2. Except supply pins.

Table 8: Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Recommended Supply Voltage TVCC, AVCC, DVCC	V_{CC}	4.75	5.0	5.25	V
Recommended Operating Temperature	T_{OP}	-40	-	85	°C

Table 9: Electrical Characteristics (Over Recommended Range)

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Supply Current	ICC	-	60	80	mA	VCC = 5.0 V
Input Low Voltage [2]	VIL	-	-	0.8	V	Digital Inputs
Input High Voltage [2]	VIH	2.0	-	-	V	Digital Inputs
Output Low Voltage	VOL	-	-	0.4	V	IOL= 1.6 mA (TTL)
	VOL	-	0.2	-	V	IOL< 10µA (CMOS)
Output High Voltage	VOH	2.4	-	-	V	IOH= 400µA (TTL)
	VOH	-	4.5	-	V	IOL < 10µA (CMOS)
Input Leakage Current	IIL	-40	-	40	µA	0 < VIN < VCC
Open Drain Leakage Current [3]	IODL	-	-	10	µA	

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Limited functional test patterns are performed at these input levels. The majority of functional tests are performed at levels of 0V and 3V.
3. Applies to $\overline{INT}$ and $\overline{BSY}$ only.

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Table 10: AC Timing Characteristics (Over Recommended Range)

Parameter		Symbol	Min	Typ[1]	Max	Units	Test Conditions
Receive Timing (Figure 10)	$\overline{SCR}$ period - out of lock	TPR (ol)	$1\text{-}5x10^{-3}$ / $\overline{fb(rec)}$	1 / $\overline{fb(rec)}$	$1+5x10^{-3}$ / $\overline{fb(rec)}$	µs	no Rx input at RTIP/RRING
	$\overline{SCR}$ period - in lock	TPR (il)	-	1 / fb(rec)	-	µs	Rx input present at RTIP/ RRING
	$\overline{SCR}$ pulse width High	TRCH	TPR/2 - 200	TPR / 2	TPR/2 + 200	ns	
	Rx signal input at RTIP/ RRING frequency tolerance	RXTOL	-50	0	+50	ppm	
	RD delay from $\overline{SCR}$ falling edge	TRDD	-500	-	500	ns	into 20 pF load
	Transition time on any digital output	TTO	-	-	20	ns	into 20 pF load
Transmit Timing (Figure 10)	$\overline{SCT\_E}$ period	TPT	-100ppm	1/Data Rate	+100ppm	µs	
	$\overline{SCT\_E}$ input pulse width High	TTWHI	3	1 / $\overline{2fb(tx)}$	10	µs	
	$\overline{SCT\_E}$ output pulse width High	TTWHO	1/2fb(tx) -200	1 / $\overline{2fb(tx)}$	1/2fb(tx) + 200	µs	
	TD setup to $\overline{SCT\_E}$ rising edge	TTSU	700	-	-	ns	

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. fb (rec) = Frequency of incoming recovered datastream.
3. fb(tx) = Frequency of transmit bitrate clock on $\overline{SCT\_E}$ input.

Table 10: AC Timing Characteristics (Over Recommended Range) – continued

Parameter		Symbol	Min	Typ[1]	Max	Units	Test Conditions
Transmit Timing (Figure 10)	TD hold time after $\overline{SCT\_E}$ rising edge	TTH	700	-	-	ns	
	Transition time on any digital input	TTI			40	ns	
	$\overline{SCT\_E}$ input frequency tolerance (with respect to fb(tx)	TXTOL	-100	0	+100	ppm	
Crystal Tolerances	XTALI input frequency	FXTAL	–	8.192	–	MHz	
	XTALI frequency tolerance	FMTOL	-100	0	+100	ppm	
Reset Timing	$\overline{RST}$ pulse width Low	TRWL	1000	-	-	ns	

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. fb (rec) = Frequency of incoming recovered datastream.
3. fb(tx) = Frequency of transmit bitrate clock on $\overline{SCT\_E}$ input.

Figure 10: EIA Timing

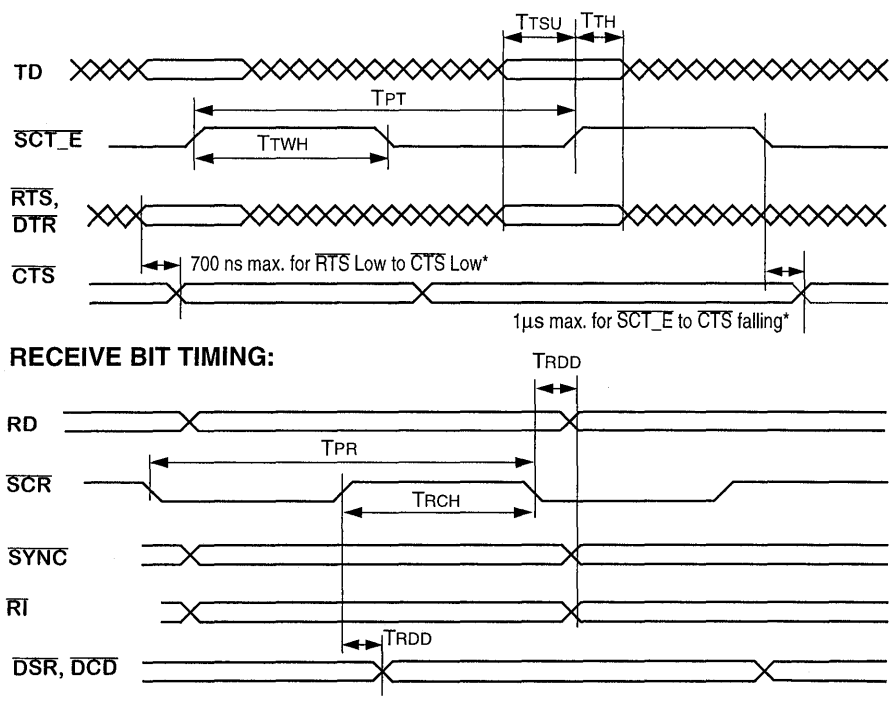


Table 11: Microprocessor Timing Characteristics (Over Recommended Range)

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
$\overline{CS}$ setup to $\overline{RD}$ or $\overline{WR}$ falling edge	TCSU	15	-	-	ns	CLOAD = 20 pF
$\overline{CS}$ hold from $\overline{RD}$ or $\overline{WR}$ rising edge	TCHR TCHW	15	-	-	ns	CLOAD = 20 pF
ALE pulse width High	TALPW	35	-	-	ns	CLOAD = 100 pF
$\overline{RD}$ or $\overline{WR}$ hold from ALE rising edge	TRWH	10	-	-	ns	CLOAD = 100 pF
ALE hold from $\overline{RD}$ or $\overline{WR}$ rising edge	TALH	15	-	-	ns	CLOAD = 100 pF
ADDR setup to ALE falling edge	TASU	15	-	-	ns	CLOAD = 100 pF
ADDR hold from ALE falling edge	TAH	15	-	-	ns	CLOAD = 100 pF
$\overline{WR}$ pulse width Low	TWPW	95	-	-	ns	CLOAD = 100 pF
$\overline{RD}$ hold time after $\overline{BSY}$ High	TRDH	0	-	-	ns	CLOAD = 100 pF on $\overline{RD}$
DATA valid from $\overline{RD}$ falling edge	TDPR	5	-	70	ns	CLOAD = 100 pF
DATA hold from $\overline{RD}$ rising edge	TDHR	2	-	15	ns	CLOAD = 100 pF
$\overline{BSY}$ Low delay from $\overline{RD}$ or $\overline{WR}$ Low	TBP	5	-	55	ns	CLOAD = 20 pF / 2 kΩ
$\overline{BSY}$ Low duration	TBWL	122	-	344	ns	CLOAD = 20 pF / 2 kΩ
DATA setup to $\overline{WR}$ rising edge	TDSUW	30	-	-	ns	CLOAD = 100 pF
DATA hold from $\overline{WR}$ rising edge	TDHW	25	-	-	ns	CLOAD = 100 pF
$\overline{INT}$ clear after $\overline{RD}$ High for ADDR = 08h	TDCI	244	-	470	ns	CLOAD = 20 pF / 2 kΩ

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.

Figure 11: Microprocessor Timing - Read Operations

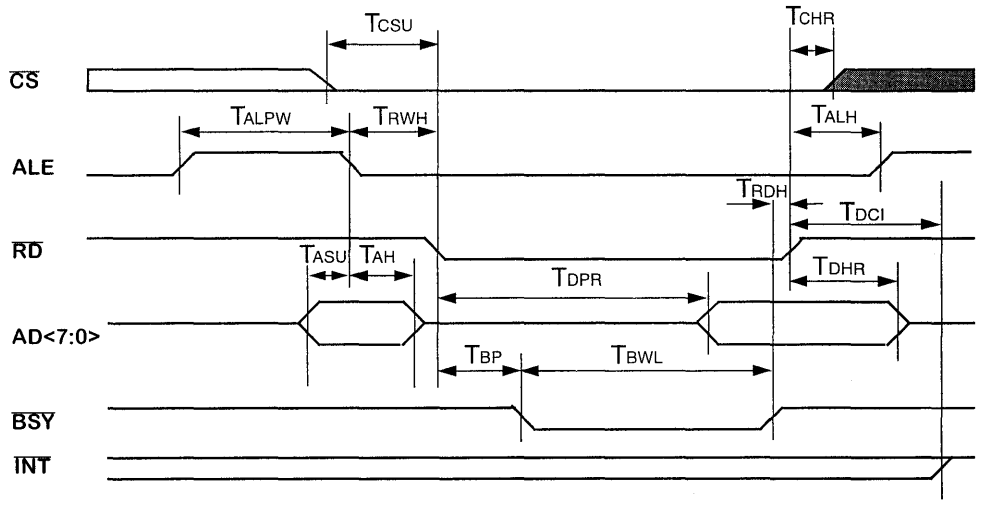
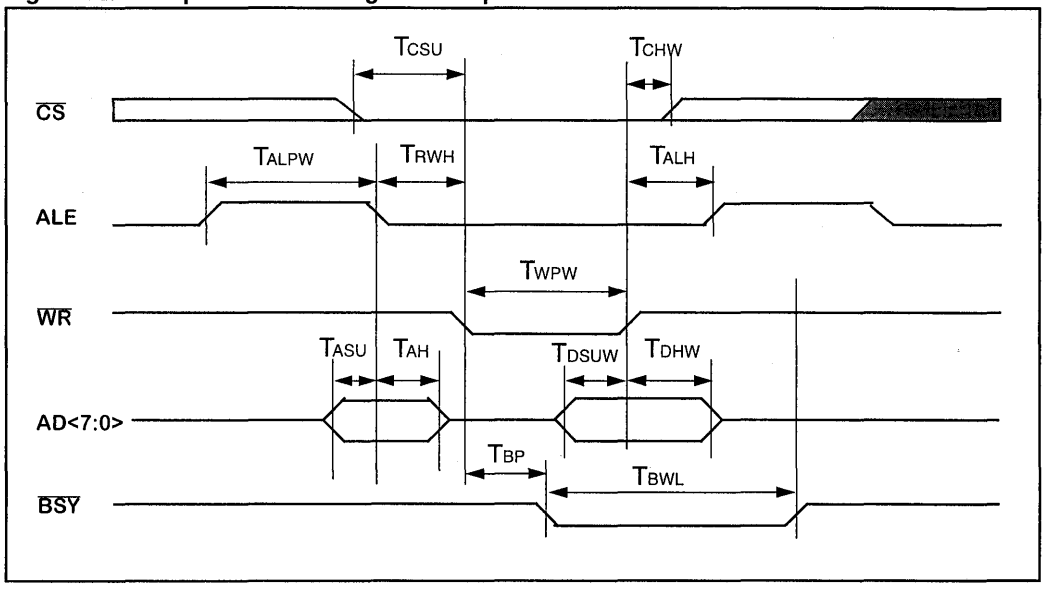


Figure 12: Microprocessor Timing - Write Operations



REGISTER DEFINITIONS

Introduction

The LXT441 incorporates a total of 19 registers, 8 Write and 11 Read registers. Refer to Table 12 for a complete list of register designations and addresses. Register addresses and other hexadecimal numbers are represented as "0xnn" where "nn" is the hex value.

Table 12: LXT441 Register Set

Address	Write Registers		Read Registers	
AD<7:0>	WRx	Name	RDx	Name
xxx00000	WR0	Device Control Register	RD0	readback of WR0
xxx00001	WR1	Transmit Control Register	RD1	readback of WR1
xxx00010	WR2	Receive Control Register	RD2	readback of WR2
xxx00011	Reserved			
xxx00100	Reserved			
xxx00101	WR5	EIA Select Register	RD5	readback of WR5
xxx00110	Reserved			
xxx00111	WR7	Transmit EIA Data Register	RD7	Receive EIA Data Register
xxx01000	WR8	Interrupt Enable Register	RD8	Interrupt Status Register
xxx01001	WR9	EIA Control Register	RD9	EIA Status Register
xxx01010	Reserved		RDA	Device Status Register
xxx01011	Reserved		RDB	Rx Slicer Level Register
xxx01100	WRC	Rx Code Interrupt Enables	RDC	Rx Codes Register
xxx01101	Reserved		RDD	Invalid BPV Counter
xxx01110	Reserved			
xxx01111	Reserved			

Table 13: LXT441 Register Bit Mapping

Register	R/W	Addr	b7	b6	b5	b4	b3	b2	b1	b0
Device Control	R/W	0x00	0	OCU	TCCT	SCT_EN	0	0	MODE1	MODE0
Transmit Control	R/W	0x01	BONDEN	CALLMD	0	TX_MRK	ZS_DIS	TX_CMI	TX_OOS	TX_OOF
Receive Control	R/W	0x02	DSU_LP	TX_DLP	CSU_LP	FILFCE	FFILT3	FFILT2	FFILT1	FFILT0
EIA Select	R/W	0x05	0	0	EIAREG	0	0	0	0	0
Tx EIA Data	W	0x07	D1	D2	D3	D4	D5	D6	D7	X, C, or D8
Rx EIA Data	R	0x07	D1	D2	D3	D4	D5	D6	D7	X, BF, C, or D8
Interrupt Enable	W	0x08	EIADEL	IDEL	RX_CODE	V_OFL	XBPV	FSYNC	RSYNC	ACTIVE
Interrupt Status	R	0x08	EIADEL	IDEL	RX_CODE	V_OFL	XBPV	FSYNC	RSYNC	ACTIVE
EIA Control (reset value)	W	0x09	FC_DCE (0)	DSR (1)	DCD (1)	RI (0)	CTS (1)	FC_DTE (0)	DTR (1)	RTS (1)
EIA Status	R	0x09	FC_DCE	DSR	DCD	RI	CTS	FC_DTE	DTR	RTS
Device Status	R	0x0A	RLOS	FSYNC	ACTIVE	ISTATE	LL3	LL2	LL1	LL0
Rx Slicer Level	R	0x0B	MAG7	MAG6	MAG5	MAG4	MAG3	MAG2	MAG1	MAG0
Rx Code Interrupt Enable (reset value)	W	0x0C	MRK_EN (1)	ZSC_EN (0)	CMI_EN (1)	OOS_EN (0)	OOF_EN (0)	DLP_EN (0)	0 (0)	UNM_EN (0)
Rx Codes	R	0x0C	RX_DMI	RX_ZSC	RX_CMI	RX_OOS	RX_OOF	RX_DLP	RX_UMC	UNMTCH
BPV Count	R	0x0D	IBPV7	IBPV6	IBPV5	IBPV4	IBPV3	IBPV2	IBPV1	IBPV0

1. A Low on the $\overline{RST}$ input will force all register bits to 0, except where specified.

Table 14: Register WR0 - Device Control - Address 0x00

b7	b6	b5	b4	b3	b2	b1	b0
-	OCU	TCCT	SCT_EN	-	FTEST	MODE1	MODE0

Bit	Mnemonic	Function
b7	-	**Reserved.** Program to 0.
b6	OCU	**OCU and DSU Mode Selection.** Controls timing sources in conjunction with TCCT (see TCCT bit description for additional information).
b5	TCCT	**Tail Circuit.** Controls timing sources in conjunction with OCU as follows: Bits<6:5> / Source for $\overline{SCT\_E}$ / Source for TCLK 10 / XTALI via Internal Oscillator / XTALI via Internal Oscillator[1] 11 / N/A / $\overline{SCT\_E}$ input pin 00 / RCLK / RCLK 01 / N/A / $\overline{SCT\_E}$ input pin
b4	SCT_EN	**Serial Clock Transmit Enable.** 0 = $\overline{SCT\_E}$ pin set to high impedance state; 1 = $\overline{SCT\_E}$ pin enabled as an output.
b3	-	**Reserved.** Program to 0.
b2	FTEST	**Factory Test (FTEST).** Program to 0.
b<1:0>	MODE<1:0>	**Mode Select (MODE<1:0>).** Sets Mode and Line Rate as follows: Bits<1:0> / Operating Mode / Line Rate 00 / DDS-PRI / 56 kbps 11 / DDS-PRI / 56 kbps 01 / DDS-SC / 72 kbps 10 / CC-64K / 72 kbps

1. Only applicable for DDS-PRI 56 kbps applications (MODE<1:0> = 00 or 11).

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Table 15: Register WR1 - Transmit Control (DDS-PRI Mode) - Address 0x01

b7	b6	b5	b4	b3	b2	b1	b0
BONDEN	CALLMD	-	TX_MRK	ZS_DIS	TX_CM	TX_OOS	TX_OOF

Bit	Mnemonic	Function
b7	BONDEN	**Bonding Enable.** 0 = Bonding frame detection disabled; 1 = Bonding frame detection enabled.
b6	CALLMD	**Call Mode.** 0 = Allow data transfer from DTE; 1 = Indicate to DTE that call processing is underway
b5	-	**Reserved.** Program to 0.
b4	TX_MRK	**Transmit All Marks.** 1 = Transmit All Marks, the Data Mode Idle (DMI) sequence. (also sends all 1s DMI in CC-64K mode)
b3	ZS_DIS	**Zero Suppression Disable.** 1 = Disable Transmit Zero Suppression
b2	TX_CMI	**Transmit Control Mode Idle.** 1 = Transmit Control Mode Idle sequence
b1	TX_OOS	**Transmit Out Of Service.** 1 = Transmit Out Of Service sequence
b0	TX_OOF	**Transmit Out Of Frame.** 1 = Transmit Out Of Frame sequence

Table 16: Register WR1 - Transmit Control (DDS-SC Mode) - Address 0x01

b7	b6	b5	b4	b3	b2	b1	b0
T_UMC	-	-	T_IDLE	T_ZER	T_CMI	T_ASC	T_MOS

Bit	Mnemonic	Function
b7	T_UMC	**Transmit UMC.** 1 = Transmit Unassigned Multiplex Code sequence
b<6:5>	-	**Reserved.** Program to 0.
b4	T_IDLE	**Transmit Idle.** 1 = Transmit the Data Mode Idle (DMI) sequence. (also sends all 1s DMI in CC-64K mode)
b3	T_ZER	**Transmit All 0s.** 1 = Transmit all Zeros
b2	T_CMI	**Transmit Control Mode Idle.** 1 = Transmit Control Mode Idle sequence.
b1	T_ASC	**Transmit Abnormal Station Code.** 1 = Transmit Abnormal Station Code sequence
b0	T_MOS	**Transmit Mux Out of Sync.** 1 = Transmit Multiplexer Out of Sync sequence

Table 17: Register WR2 - Receive Control - Address 0x02

b7	b6	b5	b4	b3	b2	b1	b0
DSU_LP	TX_DLP	CSU_LP	FILFCE	FFILT3	FFILT2	FFILT1	FFILT0

Bit	Mnemonic	Function
b7[1]	DSU_LP	**DSU Loopback.** 1 = Forces local DSU loopback (EIA RD connected to TD)
b6	TX_DLP	**Transmit Non-Latching DSU Loopback.** 1 = Transmit Non-Latching DSU Loopback Code in DDS-SC, or BPV sequence in DDS-PRI. Not used in CC-64K
b5[2]	CSU_LP	**CSU Loopback.** 1 = Forces CSU loopback
b4	FILFCE	**Filter Force Enable.** 0 = Filter Forcing Disabled (Program to 0 for normal operation.); 1 = Filter Forcing Enabled
b<3:0>	FFILT<3:0>	**Filter Forcing Control Bits.** Filter Gain = (0X0F - FFILT<3:0>)*6dB.

1. Readback of RD2 yields the logical OR of the value written to bit b7 (DSU_LP) and DSU loop status.
2. Readback of RD2 yields the logical OR of the value written to bit b5 (CSU_LP) and CSU loop status.

Table 18: Register WR5 - EIA Select - Address 0x05

b7	b6	b5	b4	b3	b2	b1	b0
-	-	EIAREG	-	-	-	-	-

Bit	Mnemonic	Function
b<7:6>	-	**Reserved.** Program to 0.
b5	EIAREG	**EIA Register Mode.** 0 = Transmit data sourced by EIA TD pin; 1 = Transmit data sourced by transmit EIA data register.
b<4:0>	-	**Reserved.** Program to 0.

Table 19: Register WR7 - Transmit EIA Data - Address 0x07

b7	b6	b5	b4	b3	b2	b1	b0
D1	D2	D3	D4	D5	D6	D7	X, C, D8

Bit	Mnemonic	Function
b<7:1>	D<1:7>	**Data Bits.** Data transmitted on 4-wire link when EIAREG = 1. Refer to Table 20 for data formats.
b0	X,C,D8	**EIA Register Mode.** X = Don't Care in DDS-PRI. C = Secondary channel bit in DDS-SC. D8 = Data bit 8 in CC-64K.

Table 20: Register WR7 - Transmit EIA Data Formats

Mode	Line Rate	4-Wire Data Format									Comments
DDS-PRI	56 kbps	D1	D2	D3	D4	D5	D6	D7			7-bit byte
DDS-SC	72 kbps	D1	D2	D3	D4	D5	D6	D7	F	C	9-bit byte
CC-64K	72 kbps	D1	D2	D3	D4	D5	D6	D7	F	D8	9-bit byte
Mode	**DTE Clock**	**DTE Serial Data Format**									**Comments**
DDS-PRI	56 kbps smooth	D1	D2	D3	D4	D5	D6	D7			7-bit byte
DDS-SC	64 kbps gapped	D1	D2	D3	D4	D5	D6	D7	C		8-bit byte
CC-64K	64 kbps gapped	D1	D2	D3	D4	D5	D6	D7	D8		8-bit byte

1. Dx = Data bits to/from DTE
2. C = DDS secondary channel control bits
3. F = DDS framing bits

Table 21: Register RD7 - Rx EIA Data - Address 0x07

b7	b6	b5	b4	b3	b2	b1	b0
D1	D2	D3	D4	D5	D6	D7	X, BF, C, D8

Bit	Mnemonic	Function
b<7:1>	D<1:7>	**Data Bits.** Data received on 4-wire link
b0	X,BF,C,D8	**EIA Register Mode.** X = Don't Care in DDS-PRI. BF = Bonding Frame indicator in DDS-PRI, if BONDEN=1. C = Secondary channel bit in DDS-SC. D8 = Data bit 8 in CC-64K

Table 22: Register WR8 - Interrupt Enable - Address 0x08

b7	b6	b5	b4	b3	b2	b1	b0
EIADEL	IDEL	RX_CODE	V_OFL	XBPV	FSYNC	RSYNC	ACTIVE

Bit	Mnemonic	Function
b7	EIADEL	**EIA Control Lead Change Interrupt Enable.** 0 = Disable; 1 = Enable.
b6	IDEL	**Loop Current Change Interrupt Enable.** 0 = Disable; 1 = Enable.
b5	RX_CODE	**Receive BPV Control Code Interrupt Enable.** 0 = Disable; 1 = Enable.
b4	V_OFL	**Violations Count Overflow Interrupt Enable.** 0 = Disable; 1 = Enable.
b3	XBPV	**Excess Invalid BPV Interrupt Enable.** 0 = Disable; 1 = Enable.
b2	FSYNC	**Bonding, or DDS FAW Sync Interrupt Enable.** 0 = Disable; 1 = Enable.
b1	RSYNC	**Receive $\overline{\text{SYNC}}$ Interrupt Enable.** 0 = Disable; 1 = Enable.
b0	ACTIVE	**Active State Interrupt Enable.** 0 = Disable; 1 = Enable.

1. On power-up, this register contains all-zeros, which disables all interrupts.

Table 23: Register RD8 - Interrupt Status - Address 0x08

b7	b6	b5	b4	b3	b2	b1	b0
EIADEL	IDEL	RX_CODE	V_OFL	XBPV	FSYNC	RSYNC	ACTIVE

Bit	Mnemonic	Function
b7	EIADEL	**EIA Control Lead Change Interrupt.** 1 = Interrupt has occurred. This interrupt is generated when either the $\overline{\text{DTR}}$ or $\overline{\text{RTS}}$ input line changes state in the LXT441.
b6	IDEL	**Loop Current Change Interrupt.** 1 = Interrupt has occurred. This interrupt is generated when the loop current state changes. For changes in loop current direction, both inputs $\overline{\text{LCTR}}$ and $\overline{\text{LCRT}}$ will change state. State transitions of these two signals are debounced for 1.5 ms and multiple transitions within this time period are resolved into only one IDEL event.
b5	RX_CODE	**Receive BPV Code Interrupt.** 1 = Interrupt has occurred. This interrupt is generated upon reception of or cessation of reception of the codes listed in Table 27 (Register RDC description) as enabled by the corresponding bits in register WRC. In DDS-PRI mode, RX_DMI will generate an interrupt only when CALLMD (in register WR1) is set to logic 1 by the user. In DDS-SC mode, RX_DMI will never generate an interrupt.
b4	V_OFL	**Violations Count Overflow Interrupt.** 1 = Interrupt has occurred. This interrupt is generated when the Invalid Bipolar Violations Counter (V_CNT0 to V_CNT7) overflows at an invalid BPV count of 256.
b3	XBPV	**Excess Invalid BPV Interrupt.** 1 = Interrupt has occurred. If eight or more occurrences of invalid BPV events in sixteen groups of consecutive mark symbols are received, the XBPV interrupt is generated. This high density of BPV's requires re-activation of the LXT441, via an external $\overline{\text{RST}}$ pulse.
b2	FSYNC (BSYNC)	**Bonding, or DDS FAW Sync.** 1 = Interrupt has occurred. The Bonding Frame Sync (BSYNC) or Bit Frame Sync (FSYNC) interrupt is generated when either going into or out of synchronization for Bonding Sync or DDS-SC/CC-64K FAW sync.
b1	RSYNC	**Receive $\overline{\text{SYNC}}$ Interrupt.** 1 = Interrupt has occurred. The RSYNC interrupt is generated coincident with the falling edge of the $\overline{\text{SYNC}}$ pulse.
b0	ACTIVE	**Active State Interrupt.** 1 = Interrupt has occurred. The ACTIVE interrupt is generated when the LXT441 enters or exits the receiver active state. When activation sequence has completed, and reliable data transmission is achieved, the receiver enters the active state. When receive signal energy is lost, or is detected to be outside the range required for optimal equalization, the receiver exits the active state, and attempts to re-activate.

1. On power-up, this register contains all-zeros. All RD8 bits which are High will be cleared along with the interrupt when RD8 is read.

Table 24: Register WR9 - EIA Control - Address 0x09

b7	b6	b5	b4	b3	b2	b1	b0
FC_DCE	DSR	DCD	RI	CTS	FC_DTE	DTR	RTS

Bit	Mnemonic	Function
b7	FC_DCE	**Force DCE Enable.** 0 (Default) = Disables User Programming of DCE Control Leads; 1 = Enables User Programming of DCE Control Leads.
b6	DSR	**Data Set Ready.** 0 = DSR Inactive; 1 (Default) = DSR Active.
b5	DCD	**Data Carrier Detect.** 0 = DCD Inactive; 1 (Default) = DCD Active.
b4	RI	**Ring Indicator.** 0 (Default)= RI Inactive; 1 = RI Active.
b3	CTS	**Clear to Send.** 0 = CTS Inactive; 1 (Default) = CTS Active.
b2	FC_DTE	**Force DTE Enable.** 0 (Default) = Disables User Programming of DTE Control Leads; 1 = Enables User Programming of DTE Control Leads.
b1	DTR	**Data Terminal Ready.** 0 = DTR Inactive; 1 (Default) = DTR Active.
b0[1]	RTS	**Request to Send.** 0 = RTS Inactive; 1 (Default) = RTS Active.

1. Forcing this bit will not cause CTS transition.

Table 25: Register RD9 - EIA Status - Address 0x09

b7	b6	b5	b4	b3	b2	b1	b0
FC_DCE	DSR	DCD	RI	CTS	FC_DTE	DTR	RTS

Bit	Mnemonic	Function
b7	FC_DCE	**Force DCE Enable.** 0 (Default) = User Programming of DCE Control Leads Disabled; 1 = User Programming of DCE Control Leads Enabled
b6[1]	DSR	**Data Set Ready.** 0 = DSR Inactive; 1 (Default) = DSR Active.
b5[1]	DCD	**Data Carrier Detect.** 0 = DCD Inactive; 1 (Default) = DCD Active.
b4[1]	RI	**Ring Indicator.** 0 (Default) = RI Inactive; 1 = RI Active.
b3[1]	CTS	**Clear to Send.** 0 = CTS Inactive; 1 (Default) = CTS Active.
b2	FC_DTE	**Force DTE Enable.** 0 (Default) = User Programming of DTE Control Leads Disabled; 1 = User Programming of DTE Control Leads Enabled.
b1[2]	DTR	**Data Terminal Ready.** 0 = DTR Inactive; 1 (Default) = DTR Active.
b0[2]	RTS	**Request to Send.** 0 = RTS Inactive; 1 (Default) = RTS Active.

1. For DCE control leads, status is actual line condition - not value forced via WR9.
2. For DTE control leads, status is actual value on device pin - not value forced via WR9.

Table 26: Register WRC - Rx Code Interrupt Enable - Address 0x0C

b7	b6	b5	b4	b3	b2	b1	b0
IDLE	ZSC	CMI	OOS	OOF	DLP	UMC	UNM

Bit	Mnemonic	Function
b7	IDLE	**RX_DMI Interrupt Enable.** 0 = Disable; 1 = Enable.
b6	ZSC	**Zero Code Interrupt Enable.** 0 = Disable; 1 = Enable.
	(ZERO)	**(all zeros in DDS-SC/CC-64K).** 0 = Disable; 1 = Enable.
b5	CMI	**Receive Control mode Idle Interrupt Enable.** 0 = Disable; 1 = Enable.
b4	OOS	**Out of Sync.** 0 = Disable; 1 = Enable.
	(ASC)	**Abnormal Station Code Interrupt Enable.** 0 = Disable; 1 = Enable.
b3	OOF	Out of Frame Interrupt Enable. 0 = Disable; 1 = Enable.
	(MOS)	**Mux out of Sync Interrupt Enable.** 0 = Disable; 1 = Enable.
b2	DLP	**DSU Loopback Interrupt Enable.** 0 = Disable; 1 = Enable.
b1	UMC	**Unassigned Mux Code Interrupt Enable.** 0 = Disable; 1 = Enable.
b0	UNM	**Unmatched Code Interrupt Enable.** 0 = Disable; 1 = Enable.

Table 27: Register RDC - Rx Codes - Address 0x0C

b7	b6	b5	b4	b3	b2	b1	b0
RX_DMI	RX_ZSC	RX_CMI	RX_OOS	RX_OOF	RX_DLP	RX_UMC	UNMTCH

Bit	Mnemonic	Function[1,2]
b7	RX_DMI	**Receiving DMI.** 1 = Receiving Data Mode Idle
b6	RX_ZSC	**Receiving ZSC.** 1 = Receiving Zero Suppression Code in DDS-PRI
	(RX_ZER)	**(All Zeros).** 1 = Receiving All 0s in DDS-SC
b5	RX_CMI	**Receiving CMI.** 1 = Receiving Control Mode Idle
b4	RX_OOS	**Receiving OOS.** 1 = Receiving Out of Service code in DDS-PRI
	(RX_ASC)	**(Receiving ASC).** 1 = Receiving Abnormal Station Code in DDS-SC
b3	RX_OOF	**Receiving OOF.** 1 = Receiving Out of Frame code in DDS-PRI
	(RX_MOS)	**(Receiving MOS).** 1 = Receiving Mux Out of Sync Code in DDS-SC
b2	RX_DLP	**Receiving DLP.** 1 = Receiving valid DSU Non-latching loopback code
b1	RX_UMC	**Receiving UMC.** 1 = Receiving Unassigned Mux Code in DDS-SC
b0	UNMTCH	**Unmatched Code.** 1 = Receiving control code that does not match codes in Table 28

1. An interrupt will be generated due to the presence of a control code if the corresponding enable bit in WRC is set. Only one code word need be received for the corresponding bit to go High in all cases except for RX_DLP. In the case of DSU loopback code, four consecutive repetitions of the RX_DLP code are required. The code must be absent for at least five consecutive word periods for the bit to be cleared.
2. The bits in this register are not latched, and are updated every 125 µs.

Table 28: Summary of Transmit and Receive Control Codes

Code Description	DDS-PRI Code								DDS-SC Code										CC-64K	Tx Priority
	Name	D1	D2	D3	D4	D5	D6	D7	Name	D1	D2	D3	D4	D5	D6	D7	F	C		
Data Mode Idle	MRK	B	B	B	B	B	B	B	IDLE	1	1	1	1	1	1	1	F	1	IDLE	Priority 1 (highest)
Control Mode Idle	CMI	B	B	B	B	X	O	V	CMI	1	1	1	1	1	1	1	F	0	N/A	Priority 2; Priority 6[1] with TX_DLP =0
DSU Loopback	DLP	N	O	B	O	X	O	V	DLP	N	0	1	0	1	1	0	F	0	N/A	Priority 2; Priority 6[1] with TX_DLP =1
		replace with								replace with										
		O	O	B	O	O	O	O		N	0	1	0	0	0	0	F	1		
Out of Service or Abnormal Station	OOS	N	O	O	B	X	O	V	ASC	N	0	0	1	1	1	1	F	0	N/A	Priority 3
Out of Sync	OOF	N	O	B	B	X	O	V	MOS	N	0	0	1	1	0	1	F	0	N/A	Priority 4
Unassigned Mux	N/A	N/A							UMC	N	0	0	1	1	0	0	F	0	N/A	Priority 5
Zero-Suppression (All Zeros)	ZSC	_	O	O	O	X	O	V	ZER	0	0	0	0	0	0	0	F	0	N/A	Priority 6; For DDS-PRI replace OOOOOOO with OOOOXOV
		replace with																		
		_	O	O	O	O	O	O												
Data	---	---							---	---									---	Priority 7

1. Transmit CMI priority is 6 for RTS=0 on the EIA interface.
2. B = a mark (pulse); V = bipolar violation mark; O = a space; X = B or O to make # of B's since last V odd. N = 1/0.
3. F = DDS-SC and CC-64K frame bit.
4. Bit numbering <D1:D7> is arbitrary for DDS-PRI codes.

Table 29: Register RDA - Device Status - Address 0x0A

b7	b6	b5	b4	b3	b2	b1	b0
RLOS	FSYNC	ACTIVE	ISTATE	LL3	LL2	LL1	LL0

Bit	Mnemonic	Function
b7	RLOS	**Receive Loss of Signal.** 1 = LXT441 Receiver has lost signal due to level being below threshold, or step change in signal magnitude. RLOS indicator, goes High after initial activation if receive signal level drops to zero volts, or drops by more than 6 dB. RLOS will then stay High until the receiver automatically re-initializes in the presence of the receive signal at a new voltage level, or the return of the signal at the old voltage level. An ACTIVE interrupt is generated in register RD8 when RLOS goes High, and again when RLOS goes Low to indicate the resumption of normal data reception. RLOS is not a latched bit.
b6	FSYNC	**FAW Sync.** 1 = DDS FAW Sync in DDS-SC or CC-64k
b5	ACTIVE	**Receiver Active.** 1 = LXT441 Receiver Activated
b4	ISTATE	**Loop Current Present.** 1 = Presence of loop current determined by a logic 0 level at $\overline{\text{LCRT}}$ or $\overline{\text{LCTR}}$ device pins. The $\overline{\text{LCRT}}$ and $\overline{\text{LCTR}}$ inputs are debounced for 1.5 ms after the initial transition by either signal. Also, up to 1.5 ms of skew between the state transitions in these signals is resolved into only one IDEL interrupt event as reported in RD8.
b<3:0>	LL<3:0>	**Loop Loss Indicator Bits.** Value of the receive filter selected by receive activation circuit. Refer to Table 30 for the nominal Nyquist frequency loop loss (+/-3dB) corresponding to the LL<3:0> value.

Table 30: Insertion Loss and Line Length Values for bits LL<3:0>

Line Rate	Parameter	Bit Codes LL<3:0>								
		0111	1000	1001	1010	1011	1100	1101	1110	1111
56 kbps	Insertion Loss (dB)	50.5	44.4	38.4	32.3	26.0	19.7	13.6	7.3	0.0
	Line Length (km)	8.5	7.5	6.4	5.3	4.2	3.2	2.1	1.1	0.0
72 kbps	Insertion Loss (dB)	50.7	45.0	38.8	32.5	26.3	20.0	14.0	7.4	0.0
	Line Length (km)	8.0	7.0	6.0	5.0	4.0	3.0	2.0	1.0	0.0

1. Insertion Loss @ fb/2 in dB.
2. Line Range in km (24 AWG PIC, no bridged taps)

Table 31: Register RDB - Rx Slicer Level - Address 0x0B

b7	b6	b5	b4	b3	b2	b1	b0
MAG7	MAG6	MAG5	MAG4	MAG3	MAG2	MAG1	MAG0

Bit	Mnemonic	Function
b<7:0>	MAG<7:0>	**Receive Signal Magnitude.** MAG<7:0> represents the receive slicer level, and is used with the LL0-LL3 bits from register RD_A to calculate the twisted-pair loop attenuation using the following formula[1]: Nyquist frequency Loop Attenuation in dB equals [Attenuation Value in dB for LL<3:0> at selected data rate[2]] + 20log10(0x3C/MAG<7:0>hex).

1. The attenuation values for LL<3:0> at 56 and 72 kbps and the values for 20log10(0x3C/MAG<7:0>hex) can be added together to compute an estimate of the actual line loss to +/-1 dB.
2. Refer to Table 30 for attenuation values.

Table 32: Register RDD - Rx Invalid BPV Count - Address 0x0D

b7	b6	b5	b4	b3	b2	b1	b0
IBPV7	IBPV6	IBPV5	IBPV4	IBPV3	IBPV2	IBPV1	IBPV0

Bit	Mnemonic	Function
b<7:0>	IBPV<7:0>	**Invalid BPV Count.** IBPV<7:0> is an 8-bit count of receive pulses that are judged to be BPVs that are not legal DDS-PRI codes. When this counter is read, it is reset 00h. If this counter overflows, the V_OFL interrupt is set.

T1/E1 Clock Adapters

LXP600A, LXP602 and LXP604

Low-Jitter Clock Adapters (CLADs)

General Description

The LXP600A, LXP602 and LXP604 Clock Adapters (CLADs) incorporate Level One's patented frequency conversion circuitry. The LXP600A and LXP602 convert a 1.544 MHz input clock to a 2.048 MHz output clock, or vice versa. The LXP604 converts between 1.544 MHz and 4.096 MHz. Each CLAD produces two different high frequency output (HFO) clocks for applications which require a higher-than-baud rate backplane or system clock.

Level One's patented locking method enables the CLAD to perform frequency conversion with no external components, while generating very little jitter on the output clock. The conversion is digitally controlled so the output clock (CLKO) is as accurate as the input clock (CLKI), and the two clocks are frequency-locked together. When an input frame sync pulse (FSI) is provided, the CLAD also phase-locks CLKI and CLKO together, and locks the output frame sync pulse ($\overline{FSO}$) to 600.

Features

- Generates a 1.544 MHz clock and its frame sync from a 2.048 MHz or 4.096 MHz clock and its frame sync, or vice versa
- Low output jitter meets AT&T Publication 62411 for 1.544 MHz, and ITU Recommendation G.823 for 2.048 MHz
- Digital control of frequency conversion process
- No external components
- Available in 8-pin plastic DIP
- Pin-selectable operation mode
- Advanced CMOS device requires only a single +5 V power supply

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Frequency Conversion

CLAD	CLKI	CLKO	HFO
LXP600A	1.544	2.048	6.144
	2.048	1.544	6.178
LXP602	1.544	2.048	8.192
	2.048	1.544	6.176
LXP604	1.544	4.096	8.192
	4.096	1.544	6.176

Applications

- Internal timing system for Channel Banks, Digital Loop Carriers, Multiplexers, Internal Timing Generators, PBX, etc.
- Conversion between 2.048 MHz or 4.096 MHz backplane rates and 1.544 MHz T1 clock rate
- Conversion between North American and International standards (T1/E1 Converter)

LXT600 Block Diagram

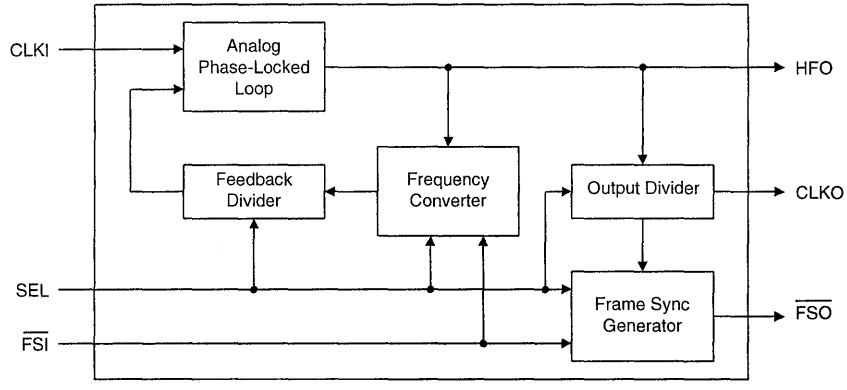
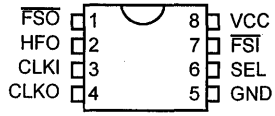


Figure 1: LXT600 Pin Assignments



LXP600ANE,
LXP602NE,
LXP604NE

Table 1: Pin Descriptions

Pin #	Sym	I/O	Description
1	FSO	O	**Frame Sync Output.** Frame synchronization output at 8 kHz. $\overline{\text{FSO}}$ is synced to CLKO and to $\overline{\text{FSI}}$ (if $\overline{\text{FSI}}$ is provided).
2	HFO	O	**High Frequency Output.** HFO is used to derive CLKO. HFO can also clock external devices. HFO is always a multiple of CLKO (CLKO x2, x3, or x4). Actual frequencies are determined by device, CLKI and CLKO frequencies and Mode Select (SEL) input, as listed in Table 2.
3	CLKI	I	**Clock Input.** Input clock (1.544, 2.048 or 4.096 MHz) to be converted.
4	CLKO	O	**Clock Output.** Output clock (1.544, 2.048 or 4.096 MHz) derived from CLKI.
5	GND	–	**Ground.**
6	SEL	I	**Mode Select.** controls frequency conversion as listed in Table 2. When SEL = High, higher frequency CLKI (2.048 for LXP600A and LXP602, or 4.096 MHz for LXP604) is converted to 1.544 MHz CLKO. When SEL = Low, 1.544 MHz CLKI is converted to higher frequency CLKO (2.048 for LXP600A and LXP602, or 4.096 MHz for LXP604).
7	$\overline{\text{FSI}}$	I	**Frame Sync Input.** 8 kHz frame synchronization pulse. Tie High or Low if not used.
8	VCC	–	**Power Supply.** +5 V power supply input.

FUNCTIONAL DESCRIPTION

The CLADs convert an input clock (CLKI) at a particular frequency to an output clock (CLKO) at a different frequency. They also produce a frame sync output ($\overline{FSO}$) and a high frequency output (HFO) clock. The HFO is a multiple (2x, 3x, or 4x) of CLKO. The HFO and CLKI/CLKO conversion frequencies are different for each device, and controlled by the Mode Select input as listed in Table 2.

The LXP600A and LXP602 convert between 1.544 MHz and 2.048 MHz. When converting from 2.048 MHz to 1.544 MHz, both CLADs produce a 6.176 MHz HFO. However, when converting from 1.544 MHz to 2.048 MHz, the LXP600A produces a 6.144 MHz HFO and the LXP602 produces an 8.192 MHz HFO.

The LXP604 converts between 1.544 MHz and 4.096 MHz. When converting from 4.096 to 1.544 MHz the LXP604 HFO is 6.176. When converting from 1.544 MHz to 4.096 MHz, the LXP604 produces an 8.192 MHz HFO.

Mode Select

The Mode Select (SEL) input controls whether the device converts to a higher or lower frequency as described below:

- 2.048 or 4.096 to 1.544 MHz: To produce a 1.544 MHz output clock from a 2.048 MHz or 4.096 MHz input clock, SEL must be set High. In this mode HFO = 6.176 MHz for all CLADs.
- 1.544 to 2.048 MHz or 4.096 MHz: To produce a 2.048 MHz or 4.096 MHz output clock from a 1.544 MHz input clock, SEL must be set Low. In this mode the LXP600A HFO = 6.144 MHz, and the LXP602 and LXP604 HFO = 8.192 MHz.

In both frequency modes, CLKO is frequency-locked to CLKI. When $\overline{FSI}$ is applied, CLKO and CLKI are also phase- locked with $\overline{FSO}$ and $\overline{FSI}$ synchronized. Refer to Test Specifications for detailed timing.

When $\overline{FSI}$ is first asserted, the CLKI and CLKO rising edges will be aligned within a maximum of 500 ms.

If $\overline{FSI}$ is not provided, pin 7 should be tied High or Low. CLKO and $\overline{FSO}$ are still generated with the CLKO frequency-locked to CLKI.

Output Jitter

2.048 MHz or 4.096 MHz to 1.544 MHz

In this mode of operation, the CLADs meet the output jitter requirements of AT&T Publication 62411. When there is no jitter on input clock CLKI, the maximum jitter on CLKO is 0.020 UI pp with no bandlimiting, 0.010 UI pp over the range of 10 Hz to 40 kHz, and 0.012 UI pp in the 8 - 40 kHz band.

1.544 MHz to 2.048 MHz or 4.096 MHz

In this mode of operation, the CLADs meet the output jitter requirements of CCITT Recommendation G.823. When there is no jitter on input clock CLKI, the maximum jitter on CLKO is 0.035 UI pp over the range of 20 Hz to 100 kHz, and 0.025 UI pp in the 18 - 100 kHz band.

Jitter Transfer

The CLADs are sensitive to jitter on the input clock in certain frequency bands. The jitter transfer curve is determined by the frequency and amplitude of the input jitter. Test Specification Figures 4 and 5 show nominal jitter transfer measured in nanoseconds. These figures graph output jitter (less intrinsic jitter) divided by input jitter (0.25 UI). Jitter transfer from a 2.048 MHz CLKI to a 1.544 MHz CLKO is shown in Figure 4. In this mode, jitter in the critical 8 kHz band is slightly attenuated while jitter in the 18 - 70 kHz band is transferred with a small net gain. Jitter transfer from a 1.544 MHz CLKI to a 2.048 MHz CLKO is shown in Figure 5. In both modes, with an input jitter level of 0.25 UI, jitter transfer is held below a net gain of 1.110.

(Jitter transfer varies with input jitter. Performance in a specific application should be verified in the actual circuit.)

Table 2: CLAD Frequency Conversions

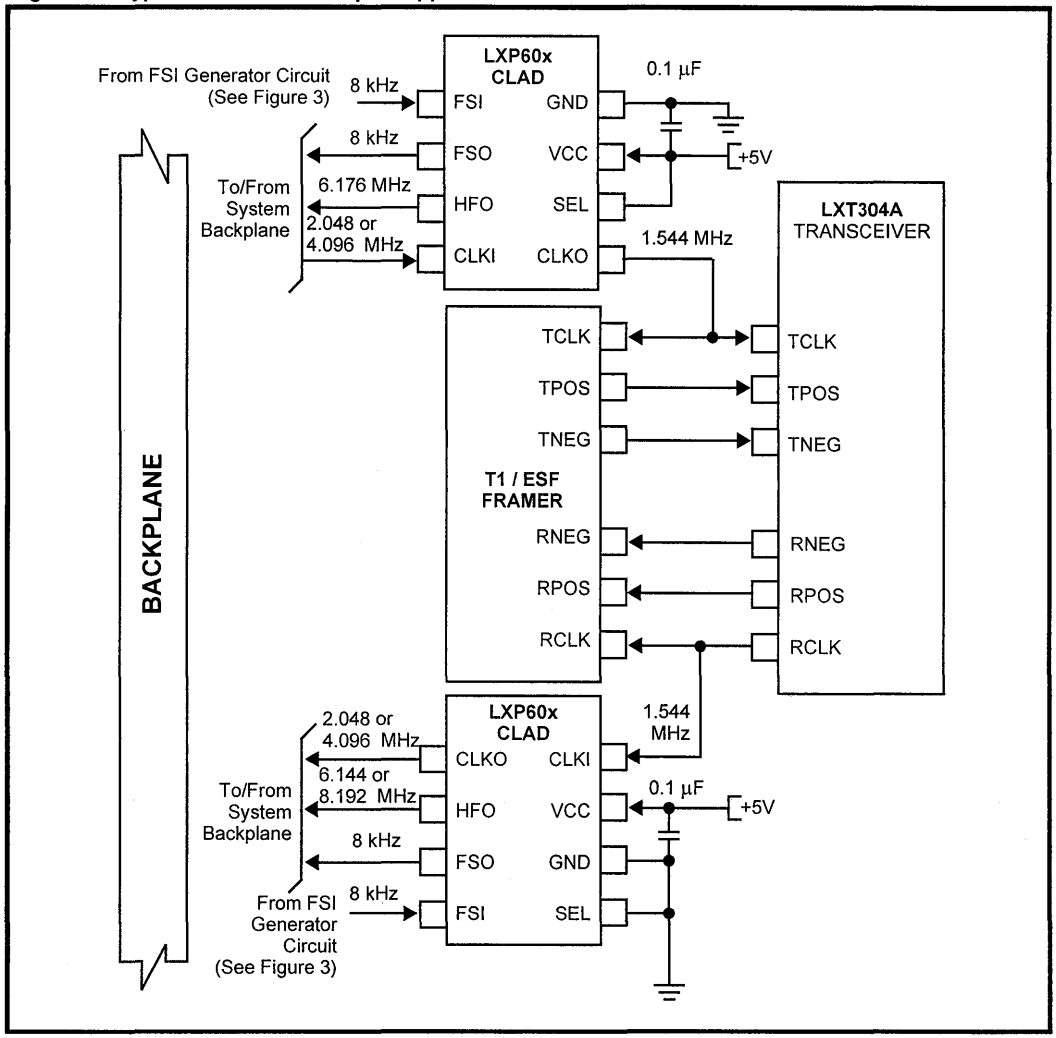
CLAD	CLKI	CLKO	HFO	SEL
LXP600A	1.544	2.048	6.144	0
	2.048	1.544	6.178	1
LXP602	1.544	2.048	8.192	0
	2.048	1.544	6.176	1
LXP604	1.544	4.096	8.192	0
	4.096	1.544	6.176	1

APPLICATION INFORMATION

Power-up

Standard CMOS device precautions apply to the CLAD. Inputs must be applied either simultaneously with or after the power supply VCC. CLAD input signals include CLKI, $\overline{FSI}$ and SEL. The CLAD internal circuitry takes a maximum of 200 ms to stabilize. There is an additional delay of 500 ms maximum for CLKO to be phase-locked to the incoming clock CLKI during frame synchronization FSI.

Figure 2: Typical TP to Coax Adapter Application Circuit



Power Supply Decoupling and Filtering

The CLADs are designed to meet AT&T Publication 62411 specifications for jitter in the range from 10 Hz to 100 kHz. Proper power supply decoupling is critical for meeting these specifications. As shown in Figure 2, a typical application with a pair of CLADs for backplane frequency conversion, a standard 0.1 µF bypass capacitor is recommended.

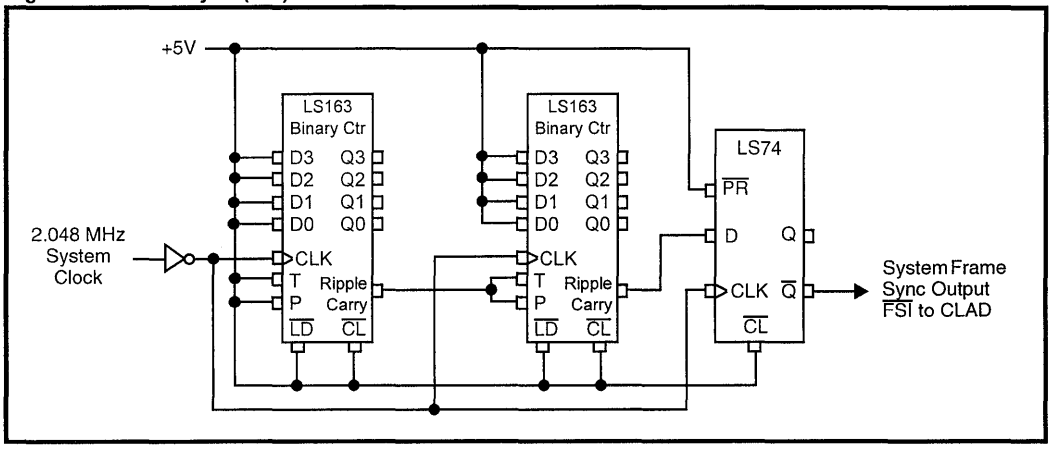
The CLADs are monolithic silicon devices which incorporate both analog and digital circuits. CLAD application circuit design may require closer attention to power supply filtering and bypassing than required for strictly digital devices.

Switching power supplies which operate below 100 kHz may produce noise spikes which can affect the analog sections of the CLAD. These spikes should be filtered with an RC network at the CLAD VCC pin.

Frame Sync Generation

A frame sync pulse is required to synchronize the input and output clocks. If a frame sync pulse is not provided on the backplane, one can be generated from the existing 2.048 MHz backplane clock. A typical FSI generation circuit is shown in Figure 3.

Figure 3: Frame Sync (FSI) Generation Circuit



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TEST SPECIFICATIONS

NOTE

The minimum and maximum values in Tables 3 through 8 and Figures 4 through 11 represent the performance specifications of the LXT600 and are guaranteed by test, except where noted by design.

Table 3: Absolute Maximum Values

Parameter	Symbol	Min	Max	Units
Supply voltage	RV+, TV+	-0.3	7.0	V
Voltage, any I/O pin	VIO	GND - 0.3	VCC + 0.3	V
Current, any I/O pin[1]	IIO	-10	10	mA
Storage temperature	TSTG	-65	+150	°C
Power dissipation	PD	–	340	mW

CAUTION

Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

1. Transient currents of up to 100 mA will not cause SCR latch-up.

Table 4: Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Supply voltage[1]	VCC	4.75	5.0	5.25	V	
Supply current	ICC	–	–	8	mA	No TTL loading
	ICC	–	–	14	mA	Full TTL loading
Operating temperature	TOP	-40	–	85	°C	

1. Voltages with respect to ground unless otherwise specified.

Table 5: Digital Electrical Characteristics (Over Recommended Range)

Parameter	Sym	Min	Max	Units
Input Low voltage	VIL	–	0.8	V
Input High voltage	VIH	2.0	–	V
Output Low voltage (IOL = +1.6 mA)	VOL	–	0.4	V
Output Low voltage (IOL < +10µA)	VOL	–	0.2	V
Output High voltage (IOH = -0.4 mA)	VOH	2.4	–	V
Output High voltage (IOH < -10µA)	VOH	4.5	–	V
Input leakage current	ILL	-10	10	µA

Table 6: Output Jitter Specifications

Parameter	Sym	Frequency	Spec[1]	Typ[2]	Max	Units	Test Conditions
Output Jitter on CLKO CLKO=1.544 MHz (All CLADS)	TJ1	No Bandlimiting	0.050	0.010	0.20	UI pp	CLKI=2.048 or 4.096 MHz JI=0 $\overline{FSI}$ applied
		10 Hz to 40 kHz	0.025	0.005	0.010	UI pp	
		8 kHz to 40 kHz	0.025	0.006	0.012	UI pp	
Output Jitter on CLKO CLKO=2.048 Mhz (LXP600A and 602 only)	TJ2	20 Hz to 100 kHz	1.500	0.025	0.035	UI pp	CLKI=1.544 MHz, JI=0 $\overline{FSI}$ applied
		18 kHz to 100 kHz	0.200	0.015	0.025	UI pp	

1. Specifications from AT&T Publication 62411 and ITU Recommendations G.823 (for 1.544 MHz and 2.048 MHz, respectively).
2. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 4: Nominal Jitter Transfer - 2.048 MHz CLKI to 1.544 MHz CLKO (Input Jitter = 0.25 UI)

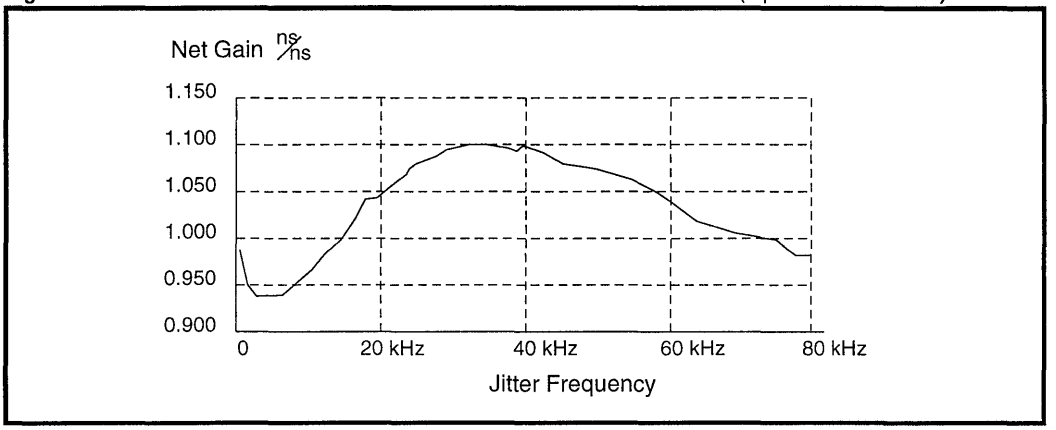

Figure 5: Nominal Jitter Transfer - 1.544 MHz CLKI to 2.048 MHz CLKO (Input Jitter = 0.25 UI)

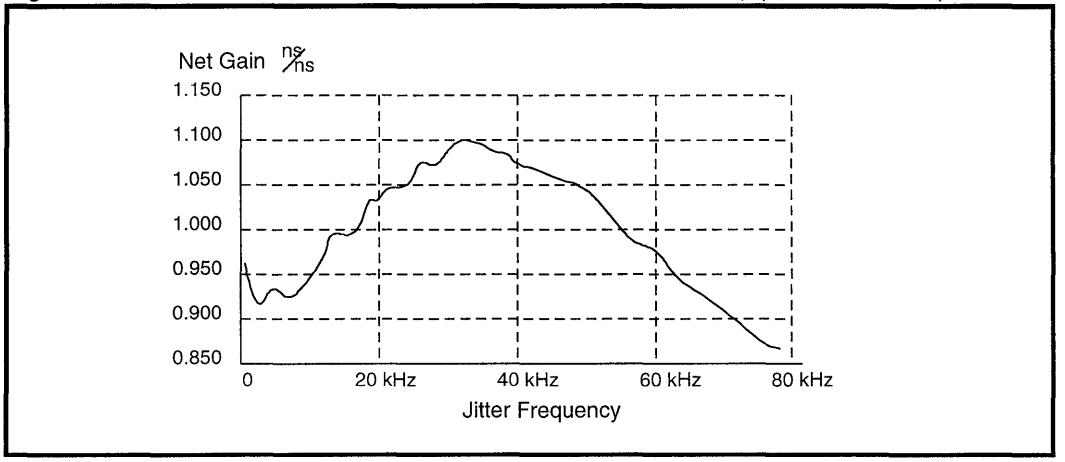

Table 7: Timing Values (see Figure 6)

Parameter	Sym	Minimum	Maximum	Units
Capture range on CLKI	–	±10000	–	ppm
Lock range on CLKI	–	±10000	–	ppm
Input clock duty cycle	–	35	65	%
Rise/fall time on CLKI, $\overline{FSI}$	Trf	–	40	ns
Rise/fall time on CLKO, $\overline{FSO}$, HFO with a 25 pF load	Trf	–	40	ns

Figure 6: Rise and Fall Times

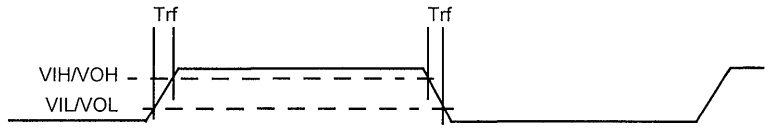

Table 8: Timing Values (see Figures 7 through 11)

Parameter	Sym	Minimum	Typ[1]	Maximum	Units
$\overline{FSI}$ setup time from CLKI rising	Tsui	46	–	–	ns
$\overline{FSI}$/CKLI hold time	Thi	30	–	–	ns
$\overline{FSI}$ pulse width (low)	Twi	76	–	TCLKI[2]	ns
CLKO delay from CLKI	TdC	-15	0	+15	ns
CLKO duty cycle	Cdc	49	–	51	%
$\overline{FSO}$ delay from HFO	TdF	-5	–	30	ns
$\overline{FSO}$ pulse width (low)	TWO	–	–	TCLKO[3]	ns
CLKO delay from HFO	TdH	-15	–	+15	ns

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. TCLKI is the period of CLKI.
3. TCLKO is the period of CLKO.

Figure 7: LXP600A and LXP602 High to Low Frequency Conversion Frame Sync Alignment)

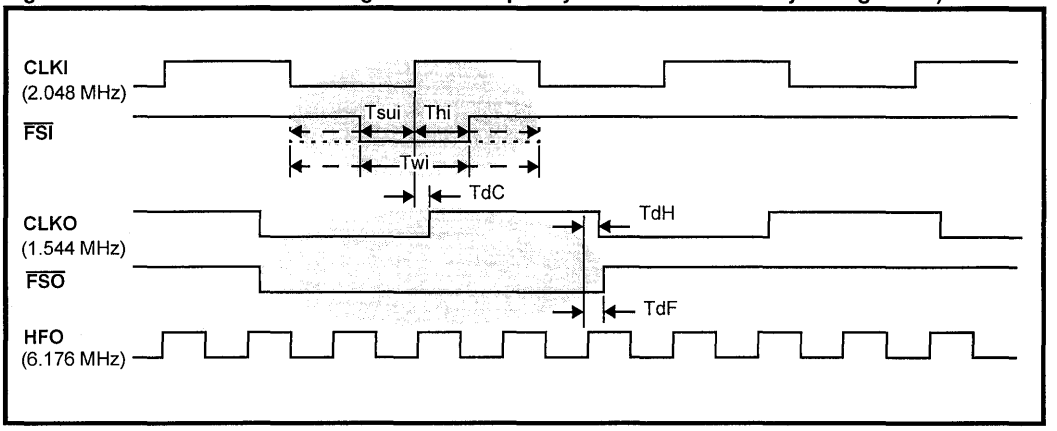

Figure 8: LXP604 High to Low Frequency Conversion Frame Sync Alignment)

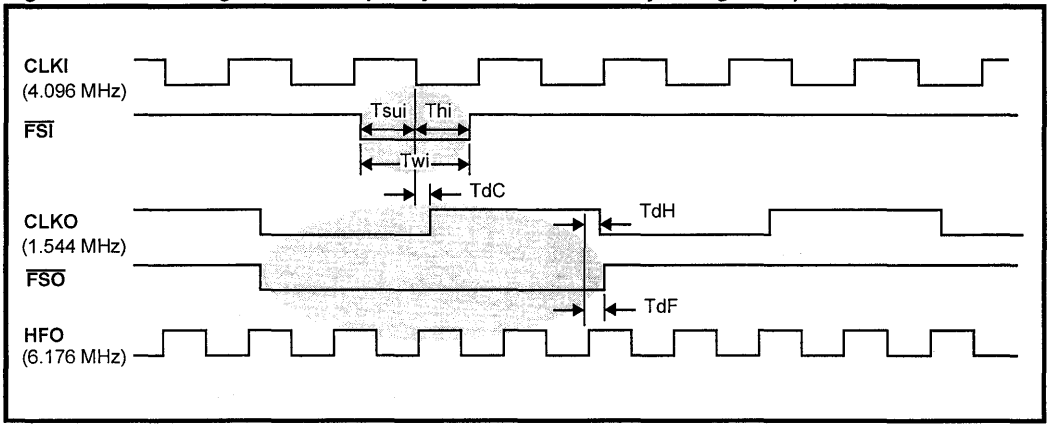

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Figure 9: LXP600A Low to High Frequency Conversion Frame Sync Alignment

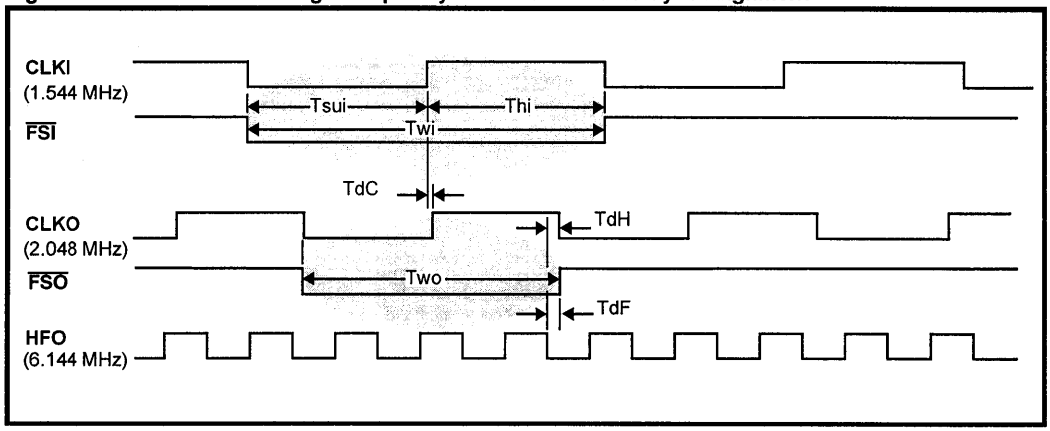


Figure 10: LXP602 Low to High Frequency Conversion Frame Sync Alignment)

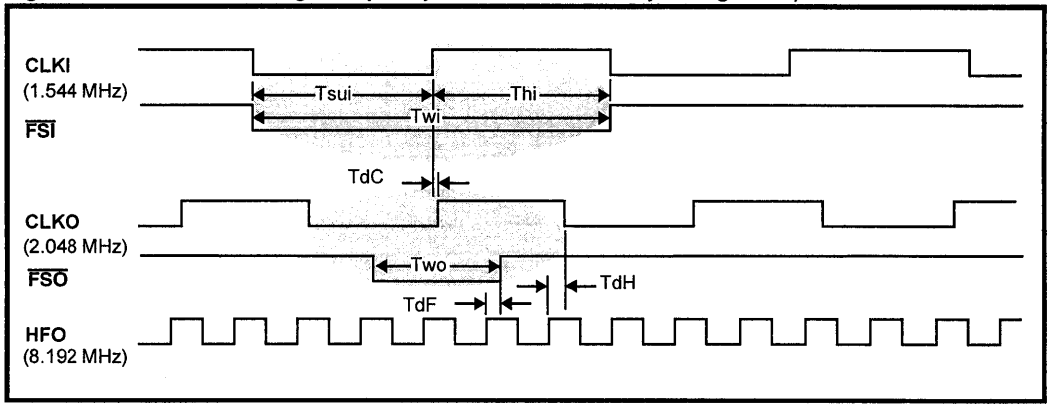
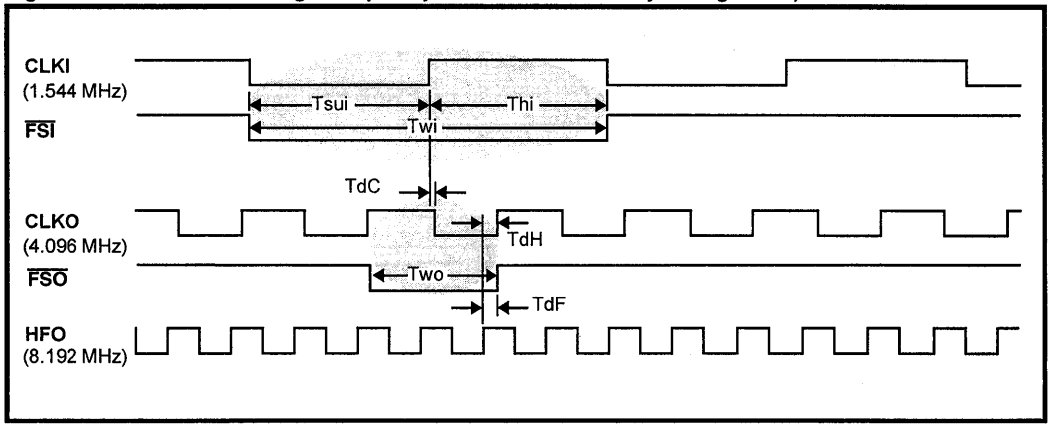


Figure 11: LXP604 Low to High Frequency Conversion Frame Sync Alignment)



LXP610

Low-Jitter Multi-Rate Clock Adapter (CLAD)

General Description

The LXP610 Multi-Rate Clock Adapter (CLAD) offers pin-selectable frequency conversion between T1 and E1 rates as well as 8 additional rates from 1.544 MHz to 8.192 MHz. The output clock is frequency-locked to the input clock. When an input frame sync pulse is provided, the CLAD phase-locks the input and output clocks together, and locks the 8 kHz output frame sync pulse to the input frame sync pulse. The frame sync polarity is also pin-selectable.

Five different high frequency output clocks are available for applications which require a higher-than-baud rate backplane or system clock. The high frequency output (HFO) clock varies with the input clock frequency.

Level One's patented locking method enables the CLAD to perform frequency conversion with no external components, while generating very little jitter on the output clock. The conversion is digitally controlled so the output clock is as accurate as the input clock.

The CLAD is an advanced CMOS device. It requires only a single +5 V power supply.

Features

- Translates between 10 different frequencies. Generates basic and high frequency output clocks and frame sync from an input clock and its frame sync.
- High Frequency Output clock for higher-than-baud rate backplane systems
- Low output jitter meets AT&T Publication 62411 for 1.544 MHz, and ITU Recommendation G.823 for 2.048 MHz
- Digital control of frequency conversion process
- No external components
- Pin-selectable operation mode
- Low-power 5 V only CMOS in 14-pin plastic DIP or 28-pin PLCC

Applications

- Internal timing system for Channel Banks, Digital Loop Carriers, Multiplexers, Internal Timing Generators, etc.
- Conversion between T1/E1 clock rates and higher frequency backplane rates (T1/E1 converter)
- Special backplane interfaces (e.g. NTI 2.56 MHz)

LXT610 Block Diagram

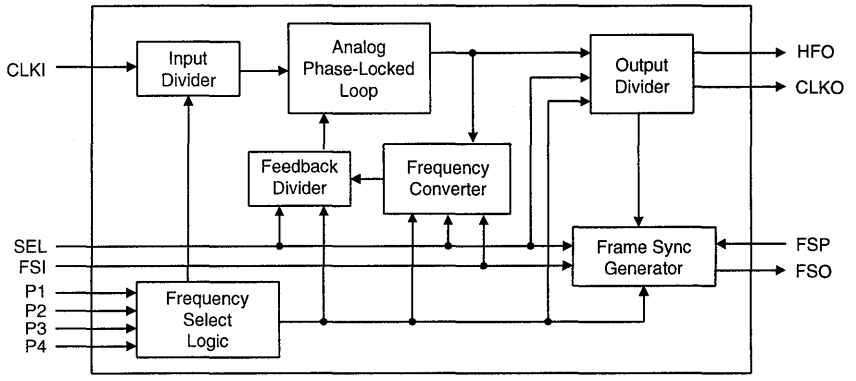


Figure 1: LXT610 Pin Assignments

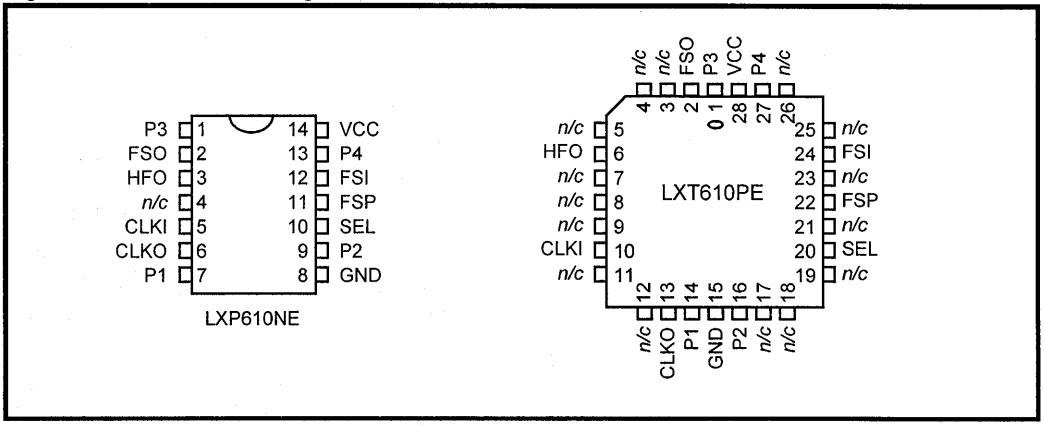


Table 1: Pin Descriptions

Pin #		Sym	I/O	Description
DIP	PLCC			
1 7 9 13	1 14 16 27	P3 P1 P2 P4	I I I I	**Program Pins 3, 1, 2, 4.** Program pins control frequency conversion and FSO pulse width in conjunction with the SEL pin as listed in Table 2.
2	2	FSO	O	**Frame Sync Output.** Frame synchronization output at 8 kHz. FSO is synched to CLKO and to FSI (if FSI is provided.) Active Low unless FSP = 1.
3	6	HFO	O	**High Frequency Output.** A high frequency output which can be used to clock external devices. HFO outputs are determined in accordance with Table 2.
5	10	CLKI	I	**Clock Input.** Primary rate clock to be converted.
6	13	CLKO	0	**Clock Output.** Primary rate clock derived from CLKI.
8	15	GND		**Ground.**
10	20	SEL	I	**Mode Select.** Controls frequency conversion and FSO pulse width in conjunction with Program pins 1-4, as listed in Table 2.
11	22	FSP	I	**Frame Sync Polarity.** When High, causes FSI and FSO to be active High pulses.
12	24	FSI	I	**Frame Sync Input**. Frame synchronization pulse (8 kHz or any sub-rate multiple). Active Low when FSP = 0. Active High when FSP = 1.
14	28	VCC	I	**Power Supply Input.** +5 V power supply input.

FUNCTIONAL DESCRIPTION

The CLAD converts an input clock (CLKI) at a particular frequency to an output clock (CLKO) at a different frequency. It also produces a frame sync output (FSO) and a high frequency output clock (HFO). The HFO frequency is a multiple (2x, 3x, 4x, or 5x) of CLKO. The specific frequencies are determined by the Mode Select (SEL) and Program (P1 - P4) inputs. Tables 2 and 3 list the CLKO and HFO frequencies available with a given input CLKI. (Table 2 is keyed to Program Pin settings; Table 3 is keyed to CLKI frequencies.) Refer to Test Specifications for output frame sync alignments.

CLKO is always frequency-locked to CLKI. When a frame sync input (FSI) is supplied, CLKI and CLKO are also phase-locked. The CLAD accepts FSI pulses at 8 kHz, or at any sub-rate multiple (i.e., 1, 2 or 4 kHz). The frame sync output (FSO) pulse is synchronized to the FSI pulse.

When an 8 kHz FSI is first asserted, the CLKI and CLKO rising edges will be aligned within a maximum of 500 ms. For other FSI rates, the alignment period is correspondingly lengthened. For example, at 4 kHz, the FSI/FSO alignment is completed within a maximum of one second.

If an input frame sync pulse is not provided, the FSI pin should be tied High or Low. CLKO and FSO are still generated with the CLKO frequency locked to CLKI.

Output Jitter

The CLAD output jitter meets the following specifications:

- 2.048 MHz or 4.096 MHz to 1.544 MHz: In this mode of operation, the CLAD meets the output jitter requirements of AT&T Publication 62411. When there is no jitter on input clock CLKI, the maximum jitter on CLKO is 0.020 UI pp with no bandlimiting, 0.010 UI in the 10 Hz - 40 kHz band, and 0.012 UI in the 8 - 40 kHz band.
- 1.544 MHz to 2.048 MHz or 4.096 MHz: In this mode of operation when there is no on, jitter input clock CLKIjitter on input clock CLKI, maximum, the jitter on CLKO is 0.035 UI pp over the maximum jitter on CLKO is 0.035 UI pp over the range of 20 Hz to 100 kHz, 0.025, and UP pp in the 18-100 KHz and 0.025 UP pp in the 18-100 kHz band.

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Table 2: Program Pin Functions

Mode Select				SEL = 0				SEL = 1			
P4	P3	P2	P1	CLKI	CLKO	HFO	FSO	CLKI	CLKO	HFO	FSO
0	0	0	0	1.544	2.048	6.144	Long (L)	2.048	3.088	6.176	L
0	0	0	1	3.088	2.048	8.192	Short (S)	2.048	3.088	6.176	L
0	0	1	0	1.544	2.048	6.144	L	2.048	1.544	6.176	L
0	0	1	1	1.544	2.048	8.192	S	2.048	1.544	6.176	L
0	1	0	0	1.544	2.560	7.680	L	2.560	1.544	7.720	L
0	1	0	1	6.176	4.096	8.192	L	8.192	3.088	6.176	L
0	1	1	0	1.544	2.560	7.680	L	2.560	1.544	7.720	L
0	1	1	1	6.176	2.048	8.192	S	8.192	1.544	6.176	L
1	0	0	0	3.088	2.048	6.144	L	2.048	3.088	6.176	L
1	0	0	1	3.088	4.096	8.192	L	4.096	3.088	6.176	L
1	0	1	0	3.088	2.048	6.144	L	2.048	3.088	6.176	L
1	0	1	1	1.544	4.096	8.192	L	4.096	1.544	6.176	L
1	1	0	0	6.176	2.560	7.680	L	2.560	1.544	7.720	L
1	1	0	1	6.176	4.096	8.192	L	8.192	3.088	6.176	L
1	1	1	0	6.176	2.560	7.680	L	2.560	1.544	7.720	L
1	1	1	1	6.176	4.096	8.192	L	8.192	1.544	6.176	L

Jitter Transfer

The CLAD is sensitive to jitter on the input clock in certain frequency bands The jitter transfer curve is determined by the frequency and amplitude of the input jitter. Test Specification Figures 4 and 5 show nominal jitter transfer measured in nanoseconds. These figures graph output jitter (less intrinsic jitter) divided by input jitter (0.25 UI). Jitter transfer from a 2.048 MHz CLKI to a 1.544 MHz CLKO is shown in Figure 4. In this mode, jitter in the critical 8 kHz band is attenuated while jitter in the 18 - 70 kHz band is transferred with a small net gain. Jitter transfer from a 1.544 MHz CLKI to a 2.048 MHz CLKO is shown in Figure 5. In both modes, with an input jitter level of 0.25 UI, jitter transfer is held below a net gain of 1.110. (Jitter transfer varies with the input jitter level. Performance in a particular application should be verified in the actual circuit.)

Table 3: Input to Output Frequency Conversion Options

CLKI	CLKO	HFO	FSO	P4	P3	P2	P1	SEL
1.544	2.048	6.144	Long (L)	0	0	X	0	0
1.544	2.048	8.192	Short (S)	0	0	1	1	0
1.544	2.560	7.680	L	0	1	X	0	0
1.544	4.096	8.192	L	1	0	1	1	0
2.048	1.544	6.176	L	0	0	1	X	1
2.048	3.088	6.176	L	0	0	0	X	1
2.048	3.088	6.176	L	1	0	X	0	1
2.560	1.544	7.720	L	X	1	X	0	1
3.088	2.048	6.144	L	1	0	X	0	0
3.088	2.048	8.192	S	0	0	0	1	0
3.088	4.096	8.192	L	1	0	0	1	0
4.096	1.544	6.176	L	1	0	1	1	1
4.096	3.088	6.176	L	1	0	0	1	1
6.176	2.048	8.192	S	0	1	1	1	0
6.176	2.560	7.680	L	1	1	X	0	0
6.176	4.096	8.192	L	0	1	0	1	0
6.176	4.096	8.192	L	1	1	X	1	0
8.192	1.544	6.176	L	X	1	1	1	1
8.192	3.088	6.176	L	X	1	0	1	1

APPLICATION INFORMATION

Frame Sync Generation

A frame sync pulse is required to synchronize the input and output clocks. If a frame sync pulse is not provided on the backplane, one can be generated from the existing 2.048 MHz backplane clock. A typical FSI generation circuit is shown in Figure 2.

Power Supply Decoupling and Filtering

The LXP610 CLAD is designed to meet AT&T Publication 62411 specifications for jitter in the range from 10 Hz to 100 kHz. Proper power supply decoupling is critical for meeting these specifications. As shown in Figure 3, a standard 0.1 µF bypass capacitor is recommended.

The CLAD is a monolithic silicon device which incorporates both analog and digital circuits. CLAD application circuit design may require closer attention to power supply filtering and bypassing than required for strictly digital devices.

Switching power supplies which operate below 100 kHz may produce noise spikes which can affect the analog sections of the CLAD. These spikes should be filtered with an RC network at the CLAD VCC pin.

Typical Application

Figure 3 shows a typical application circuit using a pair of LXP610 CLADs to convert between the 2.56 MHz backplane frequency and the 1.544 MHz T1 rate. The CLAD at the top of the figure provides the 1.544 MHz TCLK for the T1 framer and transceiver. For conversion from 2.56 MHz to 1.544 MHz, P1, P2, and P4 are tied Low; and P1 and SEL are tied High. In this configuration, the LXP610 HFO is 7.720 MHz.

The CLAD at the bottom of Figure 3 produces the 2.56 MHz backplane clock. For conversion from 1.544 MHz to 2.56 MHz, P1, P2, P3 and P4 are tied High; and SEL is tied Low. The HFO produced in this configuration is 7.680 MHz.

Figure 2: Frame Sync (FSI) Generation Circuit

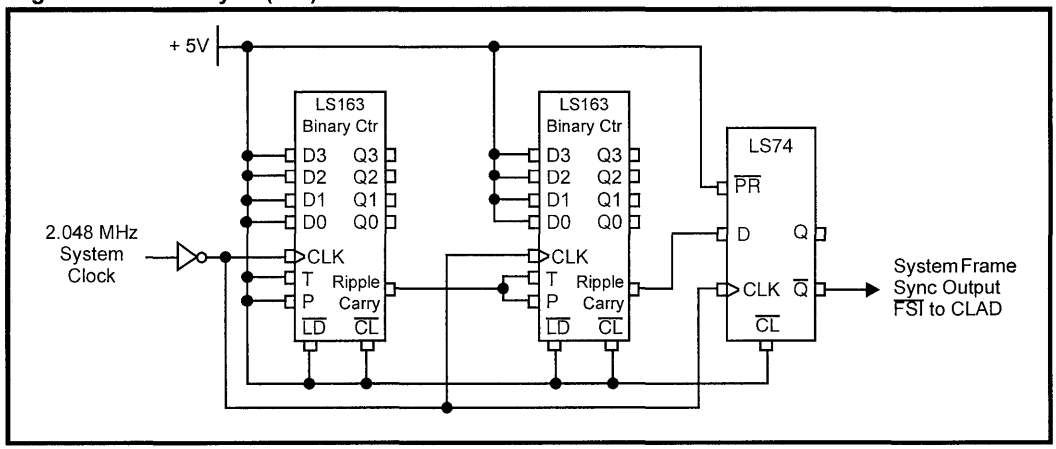
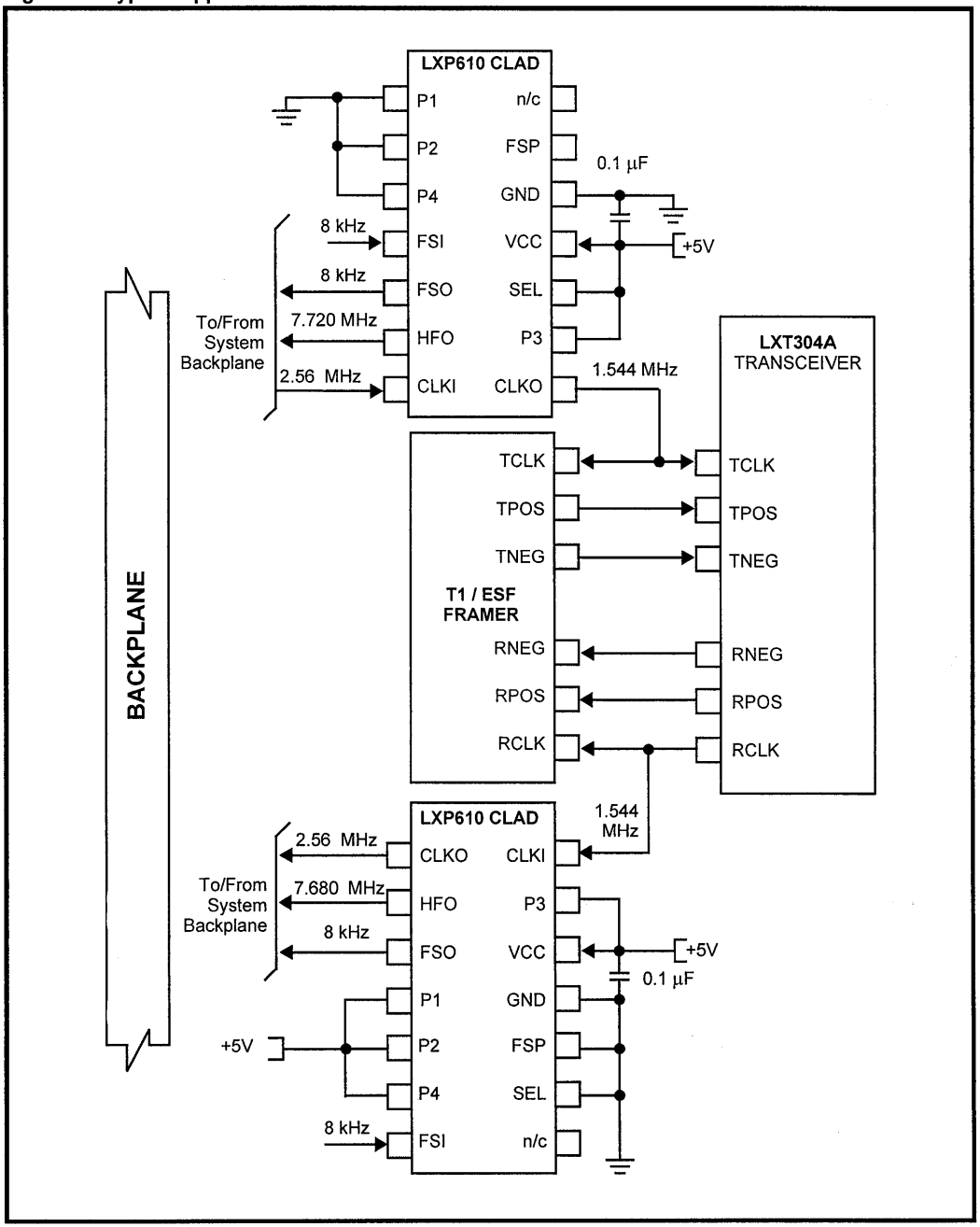


Figure 3: Typical Application Circuit



TEST SPECIFICATIONS

NOTE

The minimum and maximum values in Tables 4 through 8 and Figures 4 through 11 represent the performance specifications of the LXT610 and are guaranteed by test, except where noted by design.

Table 4: Absolute Maximum Values

Parameter	Symbol	Min	Max	Units
Supply voltage (referenced to GND)	RV+, TV+	-0.3	7.0	V
Voltage, any I/O pin	VIO	GND - 0.3	VCC + 0.3	V
Current, any I/O pin[1]	IIO	-10	10	mA
Storage temperature	TSTG	-65	+150	°C
Power dissipation	PD	–	340	mW

CAUTION

Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

1. Transient currents of up to 100 mA will not cause SCR latch-up.

Table 5: Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Supply voltage[1]	VCC	4.75	5.0	5.25	V	
Supply current	ICC	–	–	8	mA	No TTL loading
	ICC	–	–	14	mA	Full TTL loading
Operating temperature	TOP	-40	–	85	°C	

1. Voltages with respect to ground unless otherwise specified.

Table 6: Digital Electrical Characteristics (Over Recommended Range)

Parameter	Sym	Min	Max	Units
Input Low voltage	VIL	–	0.8	V
Input High voltage	VIH	2.0	–	V
Output Low voltage (IOL = +1.6 mA)	VOL	–	0.4	V
Output Low voltage (IOL < +10 µA)	VOL	–	0.2	V
Output High voltage (IOH = -0.4 mA)	VOH	2.4	–	V
Output High voltage (IOH < -10 µA)	VOH	4.5	–	V
Input leakage current	ILL	-10	10	µA

Table 7: Output Jitter Specifications

Parameter	Sym	Frequency	Spec[1]	Typ[2]	Max	Units	Test Conditions
Output Jitter on CLKO CLKO=1.544 MHz	TJ1	No Bandlimiting	0.050	0.010	0.20	UI pp	CLKI=2.048 or 4.096 MHz
		10 Hz to 40 kHz	0.025	0.005	0.010	UI pp	JI=0
		8 kHz to 40 kHz	0.025	0.006	0.012	UI pp	$\overline{FSI}$ applied
Output Jitter on CLKO CLKO=2.048 MHz	TJ2	20 Hz to 100 kHz	1.500	0.025	0.035	UI pp	CLKI=1.544 MHz, JI=0 $\overline{FSI}$ applied
		18 kHz to 100 kHz	0.200	0.015	0.025	UI pp	

1. Specifications from AT&T Publication 62411 and ITU Recommendations G.823 (for 1.544 MHz and 2.048 MHz, respectively).
2. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 4: Nominal Jitter Transfer - 2.048 MHz CLKI to 1.544 MHz CLKO (Input Jitter = 0.25 UI)

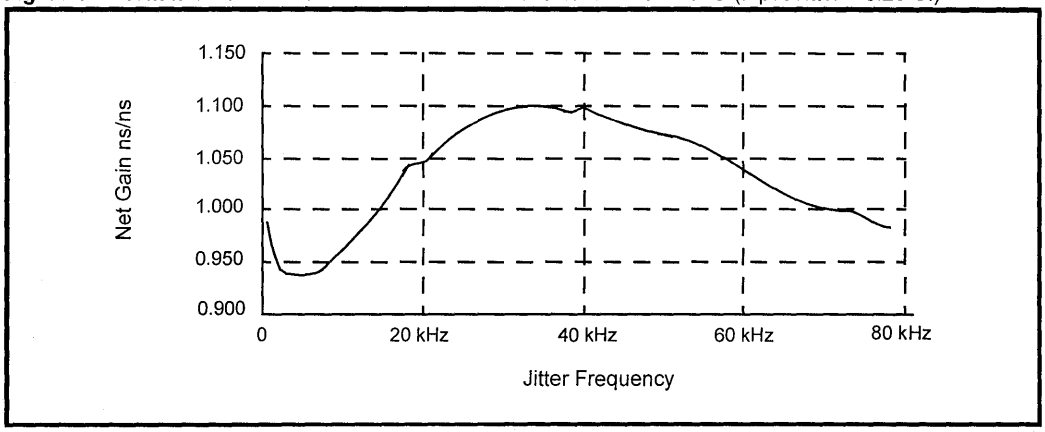


Figure 5: Nominal Jitter Transfer - 1.544 MHz CLKI to 2.048 MHz CLKO (Input Jitter = 0.25 UI)

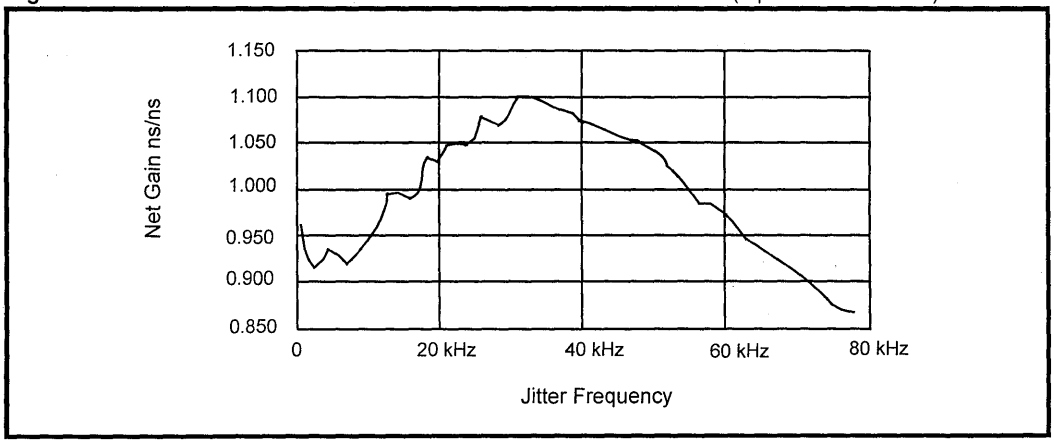


Table 8: Timing Values (see Figure 6)

Parameter	Sym	Minimum	Maximum	Units
Capture range on CLKI	–	±10000	–	ppm
Lock range on CLKI	–	±10000	–	ppm
Input clock duty cycle	–	35	65	%
Rise/fall time on CLKI, FSI	Trf	–	40	ns
Rise/fall time on CLKO, FSO, HFO with a 25 pF load	Trf	–	40	ns

Figure 6: Rise and Fall Times

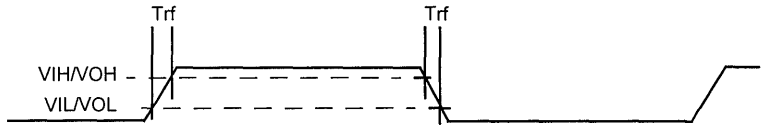


Table 9: Timing Values (see Figure 7 through Figure 11)

Parameter	Sym	Minimum	Typ	Maximum	Units
$\overline{FSI}$ setup time from CLKI rising	Tsui	46	–	–	ns
$\overline{FSI}$/CKLI hold time	Thi	30	–	–	ns
$\overline{FSI}$ pulse width (Low)	Twi	76	–	TCLKI[1]	ns
CLKO delay from CLKI	TdC	-15	0	+15	ns
CLKO duty cycle	Cdc	49	–	51	%
FSO delay from HFO	TdF	-5	–	30	ns
FSO pulse width (low)	TWO	–	–	TCLKO[2]	ns
CLKO delay from HFO	TdH	-15	–	+15	ns

1. TCLKI is the period of CLKI.
2. TCLKO is the period of CLKO.

Figure 7: Timing Relationships - FSI / CLKI to CLKO / FSO and HFO

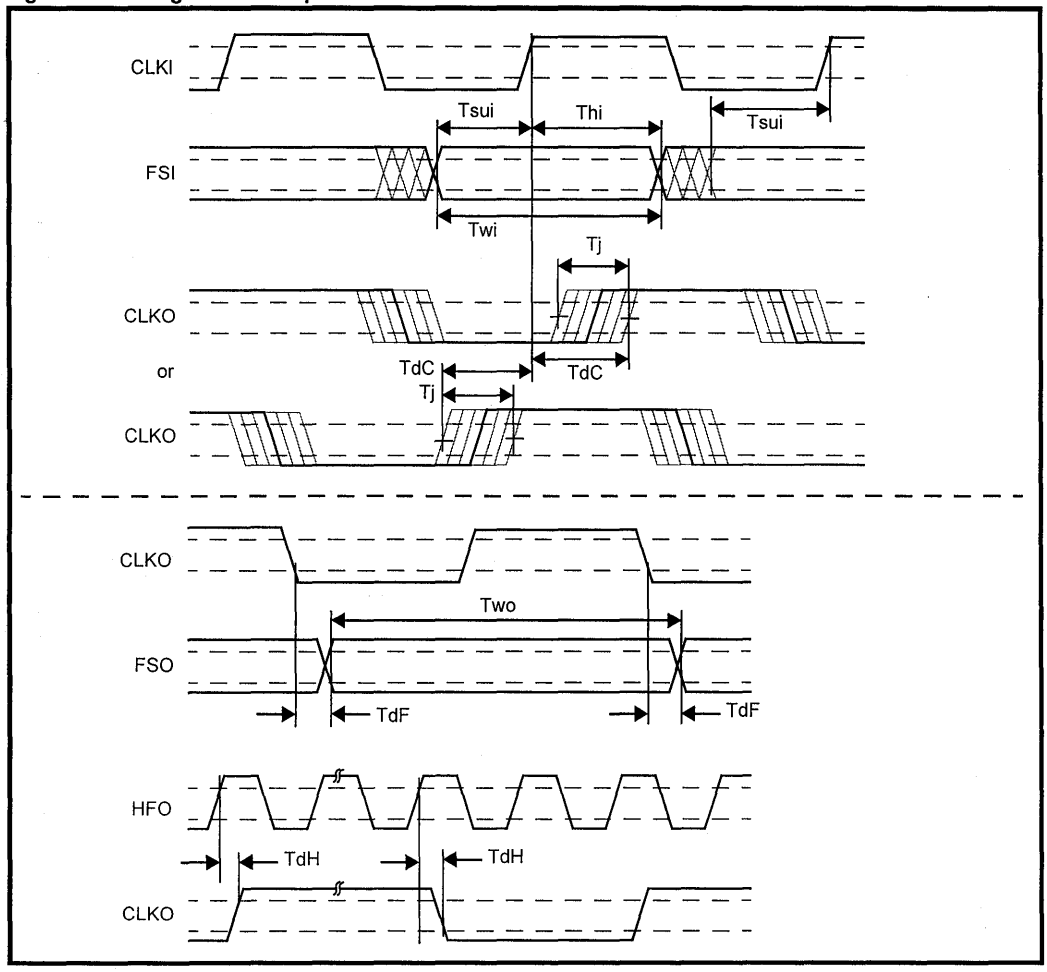


Figure 8: Output Frame Sync Alignment when HFO = 2 x CLKO

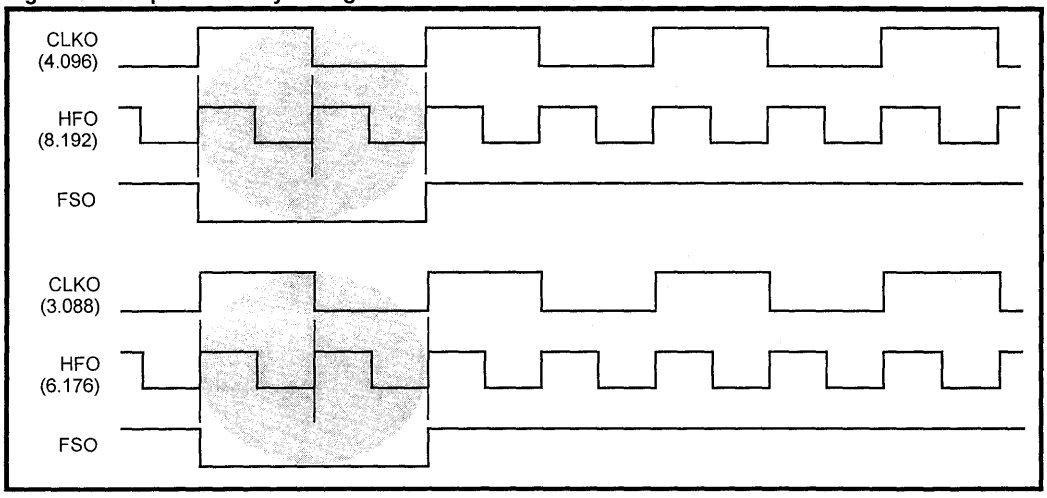


Figure 9: Output Frame Sync Alignment when HFO = 3 x CLKO

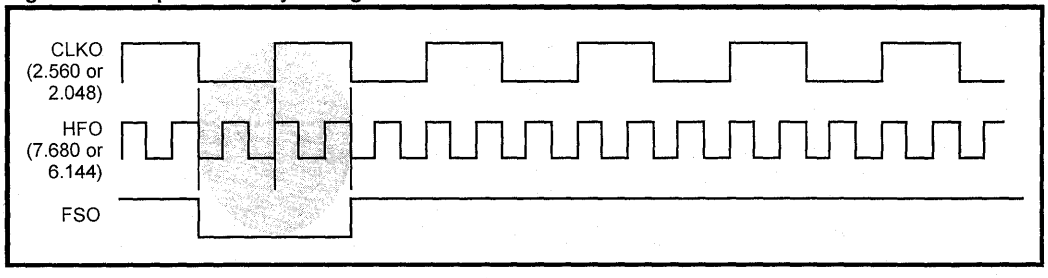


Figure 10: Output Frame Sync Alignment when HFO = 4 x CLKO

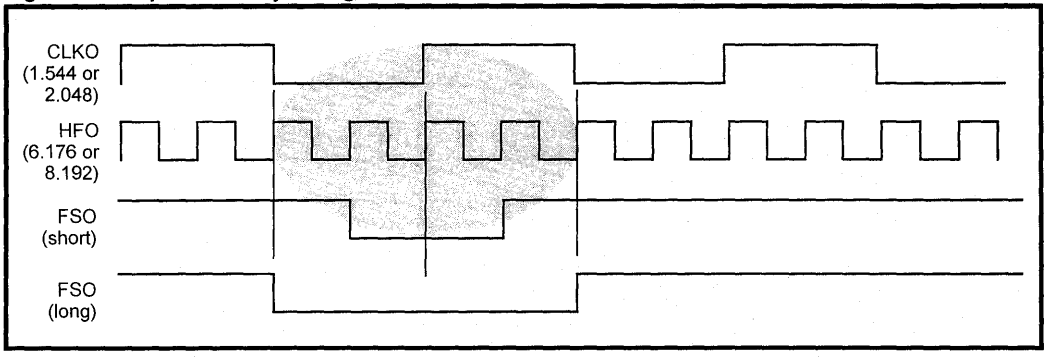
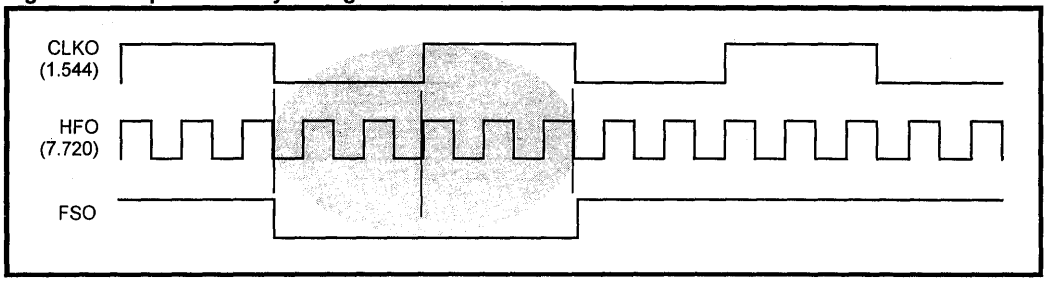


Figure 11: Output Frame Sync Alignment when HFO = 5 x CLKO



Digital Subscriber Line (DSL) Products

AUGUST 1997
Revision 2.0

SK70704/SK70706

784 kbps HDSL Data Pump Chip Set

General Description

The HDSL Data Pump is a chip set consisting of the following two devices:

- SK70704 Analog Core Chip (ACC)
- SK70706 HDSL Digital Transceiver (HDX)

The HDSL Data Pump is a 2-wire transceiver which provides echo-cancelling and 2B1Q line coding. It incorporates transmit pulse shaping, filtering, line drivers, receive equalization, timing and data recovery to provide 784 kbps, clear-channel, "data pipe" transmission. The Data Pump provides Near-End Cross-Talk (NEXT) performance in excess of that required over all ANSI and ETSI test loops. Typical transmission range on 26 AWG (0.4 mm) cable exceeds 13 kft (4 km) in a noise-free environment or 9.5 kft (2.9 km) with ANSI-specified noise levels.

The Data Pump meets the requirements of Bellcore TA-NWT-001210, ANSI T1 Technical Report No. 28-1994 and ETSI ETR-152. It provides one end of a single-channel HDSL transmission system from the twisted pair interface back to the Data Pump/HDSL data interface. The Data Pump can be used at either the HTU-R or the HTU-C end of the interface.

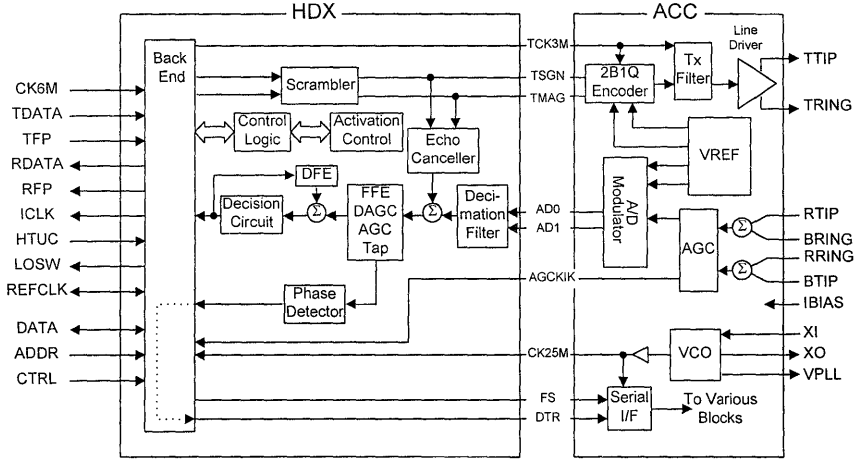
Applications

- T1 (2-pair) and fractional T1 transport
- N-channel digital pair-gain
- Wireless base station to switch interface
- Campus and private networking
- High-Speed digital modems

Features

- Fully integrated, 2-chip set for interfacing to 2-wire HDSL lines at 784 kbps
- Single +5 V supply
- Integrated line drivers, filters and hybrid circuits result in greatly reduced external logic and simplified support circuitry requirements
- Simple line interface circuitry, via transformer coupling, to twisted pair line
- Internal ACC voltage reference
- Converts serial binary data to scrambled 2B1Q encoded data
- Self-contained activation/start-up state machine for simplified single loop designs
- Programmable for either central office (HTU-C) or remote site (HTU-R) applications
- Compliant with:
  - Bellcore TA-NWT-001210
  - ANSI HDSL Technical Report No. 28-1994
  - ETSI ETR-152 (1995)
- Design allows for operation in either Software Control or stand alone Hardware Control mode
- Typical power consumption less than 1.0 W allowing remote power feeding for repeater and HTU-R equipment
- Input or Output Reference Clock of 12.544 MHz
- Digital representation of receive signal level and noise margin values available for SNR controlled activation.

HDSL Data Pump Block Diagram



7

PIN ASSIGNMENTS AND SIGNAL DESCRIPTIONS

The ACC is packaged in a 28-pin PLCC. Figure 1 shows the ACC pin locations. Table 1 lists signal descriptions for each pin, except pins 18 and 19, which are not connected.

The HDX is packaged in a 44-pin PLCC. Figure 2 shows the HDX pin locations. Table 2 lists signal descriptions for each pin, including pin 29, which is not connected.

Figure 1: SK70704 ACC Pin Locations

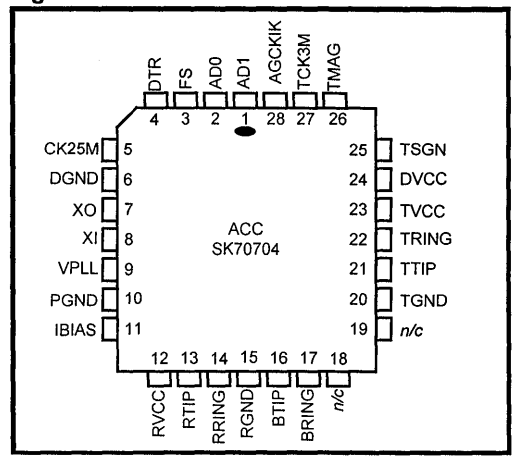


Table 1: SK70704 ACC Pin Assignments/Signal Descriptions

Group	Pin #	Symbol	I/O[1]	Description
Line	13	RTIP	AI	**Receive Tip and Ring inputs.** Connect these pins to the line transformer per network requirements.
	14	RRING	AI	
	16	BTIP	AI	**Bias Tip and Ring.** Inputs provide a bias setting for the receiver. Provide balanced network inputs.
	17	BRING	AI	
	21	TTIP	AO	**Transmit Tip and Ring.** Line driver outputs.
	22	TRING	AO	
PLL	7	XO	AO	**Crystal Oscillator.** Connect a 25.088 MHz crystal across these two pins.
	8	XI	AI	
	9	VPLL	AO	**PLL Voltage Control.** Supplies control voltage to the VCXO.
Power	10	PGND	S	**PLL Ground.** 0 V.
	12	RVCC	S	**Receive Power supply.** +5 V (± 5%).
	23	TVCC	S	**Transmit Power supply.** +5 V (± 5%).
	24	DVCC	S	**Digital Power Supply.** +5 V (± 5%).
	6	DGND	S	**DVCC Ground.** 0 V.
	15	RGND	S	**RVCC Ground.** 0 V.
	20	TGND	S	**TVCC Ground.** 0 V.

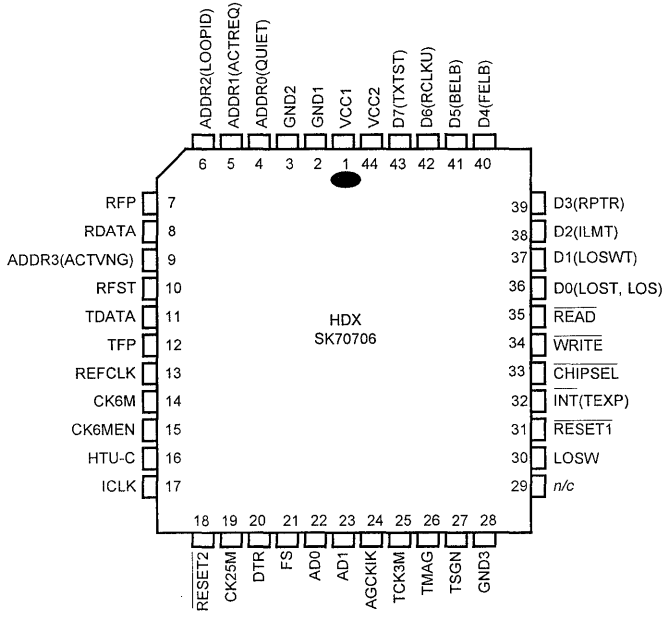
1 I/O column entries: DI = Digital Input; DO = Digital Output; DI/O = Digital Input/Output; AI = Analog Input; AO = Analog Output; AI/O = Analog Input/Output; S = Supply.

Table 1: SK70704 ACC Pin Assignments/Signal Descriptions – continued

Group	Pin #	Symbol	I/O[1]	Description
Clock and Control	3	FS	DI	**392 kHz Clock Input.** From HDX FS.
	4	DTR	DI	**Serial Control Data.** Input from HDX at 12.544 Mbps.
	5	CK25M	DO	**25.088 MHz HDSL Reference Clock.** Used as the receive timing reference for the HDX. Tie to HDX CK25M.
	27	TCK3M	DI	**3.136 MHz Clock.** Input from HDX TCK3M.
Data Input and Output	28	AGCKIK	DO	**AGC Adjust Signal.** Output to HDX AGCKIK.
	1	AD1	DO	**A-to-D Converter Data Line 1.** Connect to HDX AD1.
	2	AD0	DO	**A-to-D Converter Data Line 0.** Connect to HDX AD0.
	25	TSGN	DI	**Transmit Quat Sign.** Input from HDX.
	26	TMAG	DI	**Transmit Quat Magnitude.** Input from HDX.
Analog Input	11	IBIAS	AI	**Input Bias.** Provides input bias current.

1 I/O column entries: DI = Digital Input; DO = Digital Output; DI/O = Digital Input/Output; AI = Analog Input; AO = Analog Output; AI/O = Analog Input/Output; S = Supply.

Figure 2: SK70706 HDX Pin Assignments



NOTE:
Pin Functions in Hardware Control Mode are shown in parentheses.

Table 2: SK70706 HDX Pin Assignments/Signal Descriptions

Group	Pin #	Symbol	I/O[4]	Description
Power	1	VCC1	S	**Logic supply input.** (Refer to Table 27)
	44	VCC2	S	**I/O supply input.**
	2	GND1	S	**Ground.**
	3	GND2	S	**Ground.**
	28	GND3	S	**Ground.**
User Port	10	RFST	DO	**Receive Frame and Stuff Bit Indicator.** Goes High for 18 consecutive ICLK periods to indicate four stuffing bits (b4703 - 4706) and 14 frame bits (b1-14) on RDATA.
	13	REFCLK	DI[1] DO	**12.544 MHz HDSL Reference Clock.** In HTU-C Mode, this clock generates transmit and receive timing and must have ±32 ppm accuracy. In HTU-R Mode, this output is derived by dividing CK25M by two.
	16	HTU-C	DI	**Operation Mode Select.** When HTU-C is High, the Data Pump operates in HTU-C mode; when HTU-C is Low, the Data Pump operates in HTU-R mode. Tied to internal pull-up device.
	17	ICLK	DO	**Bit Rate Clock.** Nominally 784 kHz, REFCLK is the source of ICLK in HTU-C Mode. CK25M is the source of ICLK in HTU-R Mode.
	30	LOSW	DO	**Loss of Sync Word Indicator.** Normally Low in Active States, goes High to indicate receipt of six consecutive mismatched frame synch words. LOSW is logic High in all states except Active States.
	8	RDATA	DO	**Receive HDSL Data Stream.** Output data to HDSL framer at 784 kbps: HDSL payload of Loop 1 or Loop 2 bytes plus the F-bits, **eoc, crc, losd, febe, ps, bpv, hrp, indc/indr** and **uib** bits, Sync bits for frame positions b1-14, Stuff bits for frame positions b4703 - 4706. RDATA bits are forced high in all states except the Active State.
	7	RFP	DO	**Receive Frame Pulse.** Low for one ICLK cycle during the last bit of the current HDSL receive frame on RDATA, either b4702 or b4706. Period is within one baud time of 6 ms.[2] RFP is valid when LOSW transitions Low.
	11	TDATA	DI[1]	**Transmit HDSL Data Stream.** Input data from HDSL framer at 784 kbps: HDSL payload of Loop 1 or Loop 2 bytes plus the F-bits, **eoc, crc, losd, febe, ps, bpv, hrp, indc/indr** and **uib** bits, Sync bits for frame positions b1-14, Stuff dummy bits; may be 1s or 0s. Tied to internal pull-up device. When ACTIVE, the Data Pump is transparent and the HDSL framer must generate the appropriate bits on TDATA as shown in Table 5.
	12	TFP	DI[1]	**Transmit Frame Pulse.** Should be Low for one ICLK cycle the during last bit of the current HDSL frame on TDATA, either b4702 or b4706. Period is within one baud time of 6 ms.[2] If TFP is pulled Low and is Low again three ICLK cycles later, RDATA, RFP, RFST, ICLK, CK6MEN, and LOSW go to tri-state. Tied to internal pull-up device.

1. This input is a Schmidt Triggered circuit and includes an internal pull-up device.
2. The period is 6 ms $\pm^{1}/_{392}$ ms.
3. This input is a Schmidt Triggered circuit and includes an internal pull-down device.
4. I/O column entries: DI = Digital Input; DO = Digital Output; DI/O = Digital Input/Output; AI = Analog Input; AO = Analog Output; AI/O = Analog Input/Output; S = Supply.

Table 2: SK70706 HDX Pin Assignments/Signal Descriptions – continued

Group	Pin #	Symbol	I/O[4]	Description
Hardware Interface *(Hardware Control Mode)*	4	QUIET	DI[3]	**Quiet Mode Enable.** Pull High to force HDX into Deactivated State. Any later transition to Low will not return HDX to Active State. See ACTREQ.
	5	ACTREQ	DI[3]	**Activation Request (HTU-C mode) or no function (HTU-R mode).** Tie this pin Low in HTU-R mode. If QUIET is Low, a rising edge on this pin initiates activation, but the signal is ignored after activation. See QUIET.
	6	LOOPID	DI[3]/O	**Loop Number Control (HTU-C mode) or Loop Number Indicator (HTU-R mode).** Low = loop 1; High = loop 2. Input Signal for HTU-C mode, output for HTU-R mode. In HTU-R mode valid only when LOSW is Low. *Note: The ETSI recommendation uses overhead bits for loop identification.*
	9	ACTVNG	DO	**Activating State Indication.** High when the HDX is in the Activating State.
	18	$\overline{\text{RESET2}}$	DI[1]	**Reset Pulse.** Pull Low on power up to initialize circuits and stop all clocks.
	31	$\overline{\text{RESET1}}$	DI[1]	**Reset Pulse.** Pull Low to initialize internal circuits.
	32	TEXP	DO	**Timer Expiry.** Goes High to indicate 30 second timer expiration in all states.
	33	$\overline{\text{CHIPSEL}}$	DI[3]	**Chip Select** — *Assert these three pins Low to activate Hardware Control Mode. When any of them goes High, the HDX reverts immediately to Software Control Mode.*
	34	$\overline{\text{WRITE}}$	DI[3]	**Write Pulse**
	35	$\overline{\text{READ}}$	DI[3]	**Read Pulse**
	36	LOST *(HTU-C)*	DO	**Loss of Signal Timer Expiration.** In HTU-C mode, LOST goes High when the Data Pump enters the Inactive State. The transition from the Deactivated to the Inactive State occurs 1 second after the end of transmission by the HTU-R when deactivation began from either the Active-1 or Active-2 State. When the Data Pump transitions from the Activating State to the Deactivated State it may immediately enter the Inactive State without waiting for HTU-R transmission to cease. (See Figure 6.)
		LOS *(HTU-R)*	DO	**Loss of Signal Energy Indicator.** In HTU-R mode LOS goes High to indicate loss of signal energy on entering the Inactive State. (See Figure 8.)
	37	LOSWT	DO	**Loss of Sync Word Timer.** LOSWT goes High when LOSW is sustained for longer than 2 sec.
	38	ILMT	DI[1]	**Insertion Loss Measurement Test.** Set High to transmit a framed & scrambled, "all 1s", 2B1Q pulse sequence. Pulse sequence will have a valid sync word. In the HTU-R configuration, when the ILMT mode is selected, the Data Pump may begin activation.
	39	RPTR	DI[1]	**Repeater Mode Enable.** When in HTU-C mode, ICLK output phase is aligned to the TFP input pulse width. Ignored in HTU-R mode.
	40	FELB	DI[1]	**Front-End Loopback (HTU-C only).** In Inactive State, set High to cause the ACC to loopback. The returned signal activates the HDX which receives its own transmitted data. The system ignores incoming data from HTU-R during loopback irrespective of status.

1. This input is a Schmidt Triggered circuit and includes an internal pull-up device.
2. The period is 6 ms $\pm^{1}/_{392}$ ms.
3. This input is a Schmidt Triggered circuit and includes an internal pull-down device.
4. I/O column entries: DI = Digital Input; DO = Digital Output; DI/O = Digital Input/Output; AI = Analog Input; AO = Analog Output; AI/O = Analog Input/Output; S = Supply.

Table 2: SK70706 HDX Pin Assignments/Signal Descriptions – continued

Group	Pin#	Symbol	I/O[4]	Description
Hardware Interface *(Hardware Control Mode) -cont'd*	41	BELB	DI[1]	**Back-End Loopback.** In Active State a High forces an internal, transparent loopback with RDATA connected to TDATA and RFP connected to TFP.
	42	RCLKU	DO	**Receive Baud Rate (392 kHz) Clock.** Aligned with ICLK in HTU-R mode, phase synchronous with receive pulse stream, However, during Activating State, the clocks may not be aligned. In the HTU-C mode RCLKU has a constant, arbitrary, phase relationship with ICLK in Active State.
	43	TXTST	DI[1]	**Transmit Test.** Set high to enable isolated transmit pulse generation. The time between pulses is approximately 6 ms. TDATA controls the sign and TFP controls the magnitude of the transmitted quat pulses according to the 2B1Q encoding rules. In the HTU-R configuration, when the TXTST mode is selected, the Data Pump may begin activation.
Processor Interface *(Software Control Mode)*	36	D0	DI[1]/O	**Data bit 0.** Eight-bit, parallel data bus.
	37	D1	DI[1]/O	**Data bit 1**
	38	D2	DI[1]/O	**Data bit 2**
	39	D3	DI[1]/O	**Data bit 3**
	40	D4	DI[1]/O	**Data bit 4**
	41	D5	DI[1]/O	**Data bit 5**
	42	D6	DI[1]/O	**Data bit 6**
	43	D7	DI[1]/O	**Data bit 7**
	4	ADDR0	DI[3]	**Address bit 0.** Four-bit address, selects read or write register.
	5	ADDR1	DI[3]	**Address bit 1**
	6	ADDR2	DI[3]	**Address bit 2**
	9	ADDR3	DI[3]	**Address bit 3**
	18	$\overline{\text{RESET2}}$	DI[1]	**Reset Pulse.** Pull Low on power up to initialize circuits and stop all clocks.
	31	$\overline{\text{RESET1}}$	DI[1]	**Reset Pulse.** Pull Low to initialize internal circuits. ICLK continues.
	32	$\overline{\text{INT}}$	DO	**Interrupt Output.** Open drain output. Requires an external 10 kΩ pull up resistor. Goes Low on interrupt.
	33	$\overline{\text{CHIPSEL}}$	DI[3]	**Chip Select.** Pull Low to read or write to registers.
	34	$\overline{\text{WRITE}}$	DI[3]	**Write Pulse.** Pull Low to write to registers.
	35	$\overline{\text{READ}}$	DI[3]	**Read Pulse.** Pull Low to read from registers.
Misc.	29	*n/c*	–	*No internal connection*

1. This input is a Schmidt Triggered circuit and includes an internal pull-up device.
2. The period is 6 ms ± $^1/_{392}$ ms.
3. This input is a Schmidt Triggered circuit and includes an internal pull-down device.
4. I/O column entries: DI = Digital Input; DO = Digital Output; DI/O = Digital Input/Output; AI = Analog Input; AO = Analog Output; AI/O = Analog Input/Output; S = Supply.

Table 2: SK70706 HDX Pin Assignments/Signal Descriptions – continued

Group	Pin #	Symbol	I/O[4]	Description
Clock and Control	14	CK6M	DI[3]	**6.272 or 12.544 MHz Reference Clock.** Mandatory in HTU-R mode. Tie High or Low in HTU-C Mode. Clock input requires ± 32 ppm accuracy.
	15	CK6MEN	DO	**CK6M Enable.** Active High enable for CK6M clock. In HTU-R mode, this pin goes Low to indicate the PLL is tracking the input signal from the HTU-C. Not used in HTU-C.
	19	CK25M	DI	**Receive Timing Clock (25.088 MHz).** Tie to CK25M on ACC.
	20	DTR	DO	**Serial Control Data Link.** Transfers data at 12.544 Mbps. Tie to DTR on ACC.
	21	FS	DO	**392 kHz Clock .** Derived from CK25M. Tie to FS on ACC.
	22	AD0	DI	**Analog to Digital Converter input pin.** Tie to AD0 on ACC
	23	AD1	DI	**Analog to Digital Converter input pin.** Tie to AD1 on ACC
	24	AGCKIK	DI	**AGC Adjust Signal.** Controls analog gain circuit. Tie to AGCKIK on ACC.
	25	TCK3M	DO	**Transmit Clock.** Tie to TCK3M on ACC.
	26	TMAG	DO	**Transmit Magnitude Bit.** Tie to TMAG on ACC.
	27	TSGN	DO	**Transmit Sign Bit.** Tie to TSGN on ACC.

1. This input is a Schmidt Triggered circuit and includes an internal pull-up device.
2. The period is 6 ms $\pm^{1}/_{392}$ ms.
3. This input is a Schmidt Triggered circuit and includes an internal pull-down device.
4. I/O column entries: DI = Digital Input; DO = Digital Output; DI/O = Digital Input/Output; AI = Analog Input; AO = Analog Output; AI/O = Analog Input/Output; S = Supply.

FUNCTIONAL DESCRIPTION

The HDSL Data Pump is a fully-integrated, two-chip solution (see block diagram on front page) which includes an SK70704 Analog Core Chip (ACC) and an SK70706 HDSL Digital Transceiver (HDX).

Transmit

The transmit data stream is supplied to the HDX at the TDATA input in a binary fashion. The HDX scrambles and 2B1Q encodes the data and adds the sync word and stuff quats based on the TFP frame pulse position. The injected stuff quats in a frame are equal to the last scrambled data symbol in that frame. The 2B1Q encoded transmit quat data stream (TSGN / TMAG) is then passed to the ACC which filters and drives it onto the line. For additional details on the transmit function, refer to Component Description.

Receive

The composite waveform of the receive signal plus transhybrid echo is filtered and converted to digital words at a rate of 392 k-words/second in the ACC. The ACC passes the digitized receive quat stream (AD0 and AD1) to the HDX. The HDX performs digital filtering, linear echo cancellation, frame recovery and descrambling. The HDX uses the transmit quat stream to generate the echo estimates and estimate error values. Using this error and the delayed transmit quat stream, the echo canceller coefficients are updated. The recovered, decoded and descrambled data is then output to the framer-mux from the HDX RDATA pin. For additional details on the receive function, refer to Component Description.

Control

The Data Pump offers two control modes - Hardware Mode and Software Mode. In Hardware mode the HDX receives control inputs via individually designated pins. In Software mode the HDX control data is supplied via an 8-bit parallel port. In either mode, communication between the HDX and the ACC is established via a unidirectional serial port (DTR).

Component Description

The following paragraphs describe the chip set components individually with reference to internal functions and the interfaces between Data Pump components.

Analog Core Chip (ACC)

The ACC incorporates the following analog functions:

- the transmit driver
- transmit and receive filters
- Phase-Locked Loop (PLL)
- hybrid circuitry analog-to-digital converter

The ACC provides the complete analog front end for the HDSL Data Pump. It performs transmit pulse shaping, line driving, receive A/D, and the VCO portion of the receiver PLL function. Transmit and receive controls are implemented through the serial port. The ACC line interface uses a single twisted pair line for both transmit and receive. Table 1 lists the ACC pin descriptions. Refer to Test Specifications for ACC electrical and timing specifications.

ACC Transmitter

The ACC performs the pulse shaping and driving functions. The ACC transmitter generates a 4-level output of 1/(8*f(TCK3M)) defined by TMAG and TSGN. Table 3 lists 2B1Q pulse coding parameters. Refer to Test Specifications for frequency and voltage templates.

ACC Receiver

The ACC receiver is a sophisticated sigma-delta converter. It sums the differential signal at RTIP/RRING minus the signal at BTIP/BRING. The first A/D signal comes out of AD0 at a bit stream rate of 12.544 MHz. The second stage of the A/D samples the noise of the first and generates the AD1 bit stream at 12.544 MHz.

Receiver gain is controlled by the HDX via the AGC2-0 bits in the DTR serial control stream. The AGCKIK output from the ACC is normally Low. It goes High when the signal level in the sigma delta A/D is approaching its clipping level, signaling the HDX to lower the gain.

The VCO is part of a phase-locked loop (PLL) locked to the receive data baud rate using an external phase detector. The VCO frequency is varied by pulling an external crystal with external varactor diodes that are controlled by the VPLL output. The VPLL output is, in turn, controlled by the serial port VCO and PLL bits.

Table 3: ACC Transmit Control

TSGN	TMAG	Output Symbol (quat)
1	0	+3
1	1	+1
0	1	-1
0	0	-3

HDSL Digital Transceiver (HDX)

The HDX incorporates the following digital functions:

- bit-rate transmit and receive signal-processing
- adaptive Echo-Cancelling (EC)
- adaptive decision feedback-equalization (DFE) using the receive quat stream and the internal error signal
- fixed and adaptive digital-filtering functions
- activation/start-up control and the microprocessor interface to the HDSL framer.

The HDX also provides the Data Pump Back-End interface for the customer defined/developed HDSL framer via serial data channels and clock signals. A simple, parallel 8-bit microprocessor interface on the HDX allows high-speed access to control, status and filter coefficient words. Table 2 lists the HDX pin descriptions. Refer to Test Specifications for HDX electrical and timing specifications.

The microprocessor interface on the HDX provides bit flags for signal presence, synchronization, activation completion, and loss of synchronization for a time greater than two seconds. Single-byte words representing receive signal level and the noise margin of the transceiver are also available on the microprocessor interface. One control byte allows the user to start the Data Pump activation sequence. The HDX controls the complete activation/start-up sequence, allowing flexible, single-loop, fractional applications.

HDX/ACC Interface

The ACC provides the 25.088 MHz master clock, CK25M, to the HDX. The serial control stream framing signal FS is sampled inside the ACC with the CK25M rising edge. The serial control stream, DTR, is sampled inside the ACC by the rising edge of an internally-generated clock at f(CK25M)/2. This ACC internal clock has the same phase relationship with a similar clock inside the HDX, as established by the FS signal. In the HDX, the half-rate clock CK25M/2 and FS transition on the rising edge of CK25M, and DTR transitions coincide with the falling edge of CK25M/2. The output REFCLK in HTU-R Mode is equal to CK25M/2.

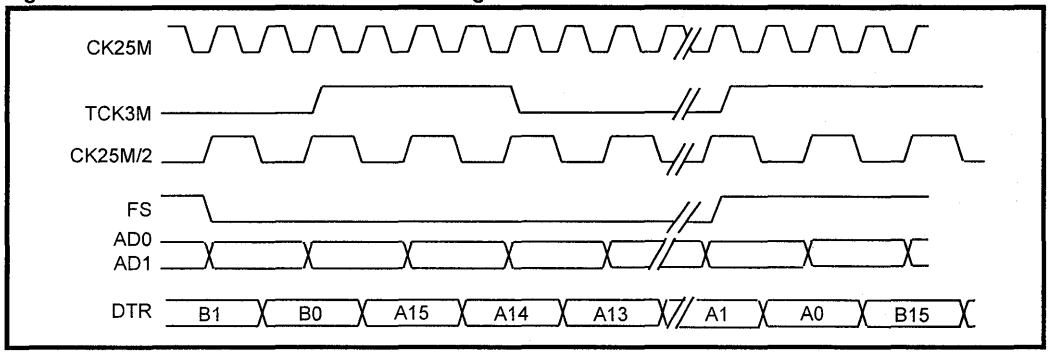
The A/D converter outputs, AD0 and AD1, are clocked out of the ACC with CK25M, having transitions coincidental with the rising edge of CK25M/2. The HDX samples AD0 and AD1 with the falling edge of its internal CK25M/2.

Transmit data, represented by TSGN and TMAG, is clocked from the HDX using the falling edge of TCK3M, the 3.136 MHz (f(REFCLK)/4) transmit time base clock. The ACC uses the rising edge of TCK3M to sample TSGN and TMAG. TSGN and TMAG change state at the baud rate, or every 8 cycles of TCK3M. Figure 3 shows relative timing for the HDX/ACC interface.

HDX/ACC Serial Port

The HDX continually writes to the ACC serial port. This serial stream consists of two 16-bit words as shown in Table 4. The data flows from the HDX to the ACC at a rate of f(CK25M)/2. Refer to the Test Specifications section for serial port timing relationships and electrical parameters.

Figure 3: HDX/ACC Interface – Relative Timing



Line Interface

The Data Pump line interface consists of three differential pairs. The transmit outputs TTIP and TRING, receive inputs RTIP and RRING, and the balance inputs BTIP and BRING, all connect through a common transformer to a single twisted-pair line (see Figures 12 and 13). The transmit outputs require resistors in series with the transformer. A passive prefilter is required for the receive inputs. The balance inputs feed the transmit signals back to the Data Pump providing passive echo cancellation. Protection circuitry should be inserted between all Data Pump line interface pins and the transformer. Refer to the Applications section for typical schematics.

Table 4: HDX/ACC Serial Port Word Bit Definitions (See Figure 3)

Bit	Word A (on DTR)	Word B (on DTR)
15	INIT	COR4
14	*n/a*	COR3
13	*n/a*	COR2
12	TXOFF	COR1
11	TXDIS	COR0
10	TXTST	VCO2
9	AGC2	VCO1
8	AGC1	VCO0
7	AGC0	PLL7
6	FELB	PLL6
5	*n/a*	PLL5
4	PTR4	PLL4
3	PTR3	PLL3
2	PTR2	PLL2
1	PTR1	PLL1
0	PTR0	PLL0

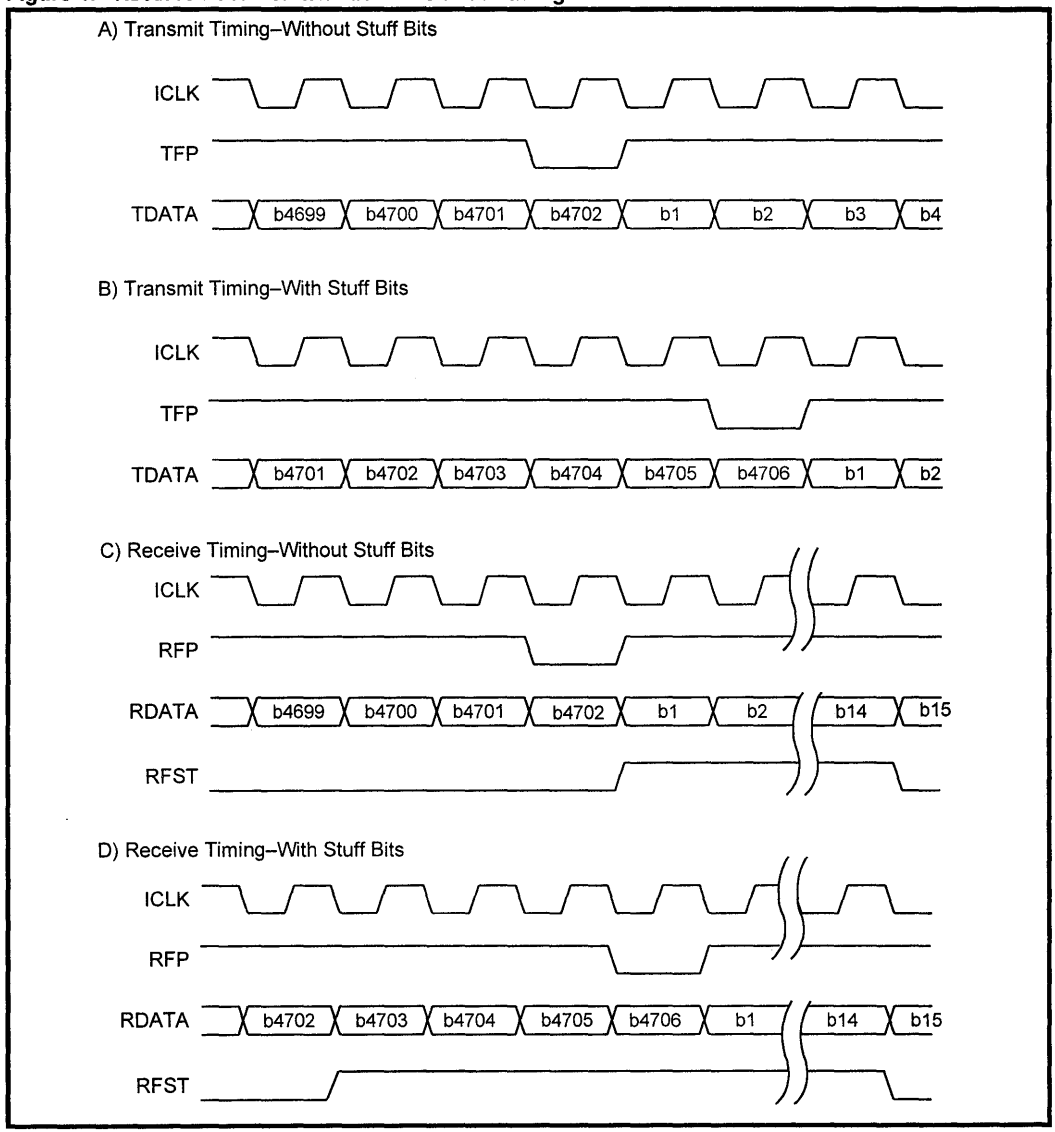
HDSL Data Interface

The HDSL data interface includes the transmit and receive binary data streams, transmit and receive frame pulses, the 784 kHz clock (ICLK) and the receive frame and stuff quat indicator (RFST). Figure 4 shows relative timing for the framer interface. Refer to Test Specifications section for details on the Data Pump/framer interface. Figure 6 shows a complete HDSL system with both the remote HTU-R and central office HTU-C HDSL framer interfaces illustrated. Table 5 shows the TDATA requirements for the framer interface through the activation sequence. Once the ACTIVE 0-to-1 transition occurs, the Data Pump becomes transparent. Therefore, the HDSL framer must supply appropriate data to TDATA. Table 5 summarizes this requirement.

Table 5: HDSL Framer TDATA Requirements

Activation Process		TDATA	
Framer	**Data Pump**	**Overhead**	**Data**
Idle	Activating	*don't care*	*don't care*
Idle	Active 1	live	all 1s
Active-R	Active 1	live	all 1s
Active-T	Active 1	live	live
Link Active	Active 1	live	live
Link Active	Active 2	live	live

Figure 4: HDX/ACC Framer Interface – Relative Timing

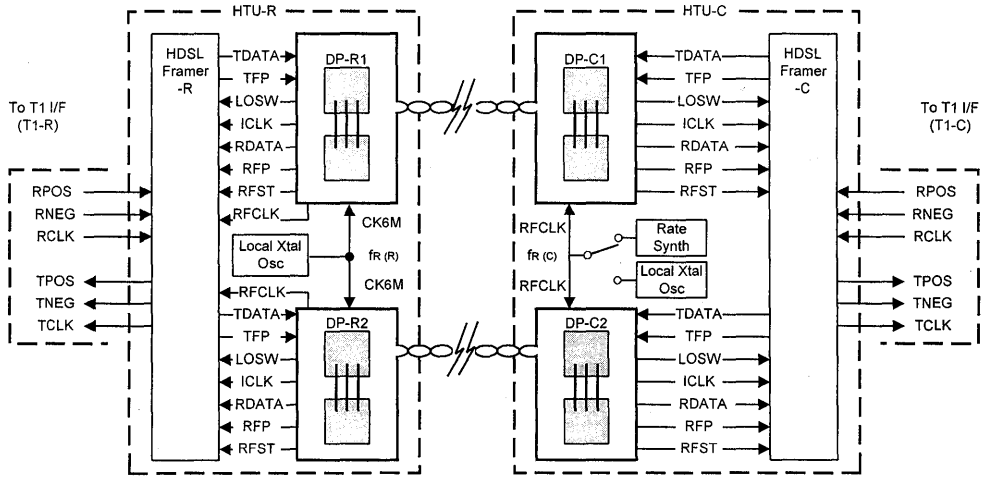


The HDSL framer interface is subject to the following rules:

1. When frame sync is not present (LOSW is High), all RDATA bits are set to 1.
2. If frame sync is lost on both Data Pump-R1 and Data Pump-R2, both units will fall back on the local reference frequency with ± 32 ppm tolerance, and stuff bits will be injected in their RDATA streams on every other frame.If frame sync is lost on either Data Pump-R1 or Data Pump-R2, that unit can be made to fall back on the REFCLK from the Data Pump-R which is still in frame sync, and stuff bits will be injected in the RDATA stream on every other frame of the out-of-frame Data Pump-R.
3. If frame sync is lost on either Data Pump-C1 or Data Pump-C2, both unit's receiver will fall back on the reference clock with ± 32 ppm or ± 5 ppm tolerance, and inject stuff bits in the RDATA stream on every other frame.
4. If either T1-R or T1-C loses sync or signal, it is assumed that the corresponding T1 receiver will fall back on a local reference with ± 32 ppm tolerance, and that transmit bit-stuffing control will still be applied through the TFP signal from the HDSL framer.
5. The HDSL framer should provide TFP signal with a period of 6 ms ± 1/392 ms prior to an activation request for the HTU-C Data Pump(s). The framer should provide a valid TFP after power-up, before or immediately after LOS goes Low for the HTU-R Data Pump(s).
6. If for any reason the TFP signal from the HDSL framer is inactive (always High or unconnected), then the Data Pump will inject stuff bits in the TDATA stream in every other frame, although the Data Pump will not be synchronized to the HDSL framer. When a new TFP is provided the Data Pump will immediately reset the transmit frame alignment, typically causing loss of alignment at the other end.
7. A simultaneous $\overline{\text{RESET2}}$ to all HTU-C Data Pumps which use a common REFCLK eliminates phase shift between the ICLK outputs which may exist after power-up.

   The ICLK outputs of all HTU-R Data Pumps may have an arbitrary phase difference even using a common CK6M reference.

Figure 5: Model for HDSL Data Pump and HDSL Framer Applications



Frequency Relationships

1. f_{TCLK} (DS1-C) = (DS1-R); tolerance = ±32 ppm, even with loss of signal on DS1-R
2. f_{TCLK} (DS1-R) = (DS1-C); tolerance = ±32 ppm, even wit loss of signal on DS1-C
3. f_{ICLK} (C) = $f_{R(C)}/16$; tolerance = ±32 ppm if sourced by local crystal oscillator (stratum 4)
   = ±5 ppm if sourced by office clock (stratum 3)
4. f_{ICLK} (R) = f_{ICLK} (C) if loop is activated with receive frame sync acquired
   = $f_{R(R)}/16$ if receive sync is lost; tolerance = ±32 ppm. (f_R(R) = 12.544 MHz)
   = $f_{R(R)}/8$ if f_R(R) = 6.272 MHz

Microprocessor Interface (HDX)

Three primary control pins, $\overline{\text{CHIPSEL}}$ (Chip Select), $\overline{\text{READ}}$ and $\overline{\text{WRITE}}$, execute the Software Mode which also uses an interrupt output pin to report status changes. Four additional pins are used for the parallel bus addressing and eight pins for data I/O. Refer to Test Specifications for µprocessor interface timing in Software Mode.

Control Pins

Chip Select: The Chip Select ($\overline{\text{CHIPSEL}}$) pin requires an active Low signal to enable Data Pump read or write transfers over the data bus. To enable Hardware Mode hold this pin Low, along with $\overline{\text{READ}}$ and $\overline{\text{WRITE}}$.

Data Read: The Data Read pin ($\overline{\text{READ}}$) requires an active Low pulse to enable a read transfer on the data bus. When $\overline{\text{READ}}$ is pulled Low, the Data Pump data bus lines go from tristate to active and output the data from the register addressed by ADDR0-ADDR3. To avoid reading data during register updates, reads should be synchronized to the falling edge of FS. Alternatively, each read should be repeated until the same data is read twice within one baud time.

Data Write: The Data Write pin ($\overline{\text{WRITE}}$) requires an active Low pulse to enable a write transfer on the data bus. Data transfer is triggered by the rising edge of the $\overline{\text{WRITE}}$ pulse. To ensure data is written to the register addressed by ADDR0-ADDR3, valid data must be present on the HDX data bus lines before $\overline{\text{WRITE}}$ goes High.

Interrupt: The Interrupt pin ($\overline{\text{INT}}$) is an open drain output requiring an external pull-up resistor. The $\overline{\text{INT}}$ output is pulled active Low when an internal interrupt condition occurs. $\overline{\text{INT}}$ is latched and held until Main Status Register RD0 is read. An internal interruption results from a Low-to-High transition in any of four status indicators: ACTIVE, LOSW, LOSWT or TEXP. Any transition on LOS will also generate an interrupt. If an interrupt mask bit in register WR2 is set, any transition of the corresponding status bit will not trigger the $\overline{\text{INT}}$ output.

Register Access

Write

To write to an HDX register, proceed as follows:

1. Drive $\overline{\text{CHIPSEL}}$ Low.
2. Drive an address (0000, 0010, or 0011) onto ADDR0-ADDR3.
3. Observe address setup time.
4. Set 8-bit input data word on D0-D7.
5. Pull $\overline{\text{WRITE}}$ Low, observing minimum pulse width.
6. Pull $\overline{\text{WRITE}}$ High, observing hold time for data and address lines.

Read

Procedures for reading the HDX registers vary according to which register is being read. Accessing registers RD0, RD1, RD2, RD5 and RD6 is relatively simple. Reading registers RD3 and RD4 is more complex. *Unless parallel port reads are synchronized with the falling edge of FS, all read operations should be repeated until the same data is read twice within one baud time.*

To read register RD0, RD1, RD2, RD5 or RD6 proceed as follows:

1. Drive $\overline{\text{CHIPSEL}}$ Low.
2. Pull $\overline{\text{READ}}$ Low, observing minimum pulse width.
3. Pull $\overline{\text{READ}}$ High to complete the read cycle.

Registers RD3 and RD4 hold the coefficient values from the DFE, EC, FFE and AGC as shown in Table 9. Register RD3 holds the lower byte value and register RD4 holds the upper byte value. To reconstruct the complete 16-bit word, concatenate the least significant and most significant bytes.

To read registers RD3 and RD4 proceed as follows:

1. Select the desired coefficient by writing the appropriate code from Table 9 to register WR3.
2. Enable the Coefficient Read Register by writing a 1 to bit b0 (CRD1) in register WR2.
3. Perform standard register read procedure listed in steps 1 through 6 above to read the lower byte from RD3 and the upper byte from RD4.
4. Concatenate the RD3 and RD4 to obtain the complete 16-bit word.

Registers

Three write registers and seven read registers are available to the user. Table 6 lists these registers and the following paragraphs describe them in more detail.

Some of the registers contain *reserved* bits. Software must deal correctly with reserved fields. For reads, software must use appropriate masks to extract the defined bits and not rely on reserved bits being any particular value. In some cases, software must program reserved bit positions to a particular value. This value is defined in the individual bit descriptions.

After asserting the $\overline{\text{RESET1}}$ or $\overline{\text{RESET2}}$ signal, the Data Pump initializes its registers to the default value.

Table 6: Register Summary

ADDR	Write Registers			Read Registers		
A3-A0	WR#	Name	Table	RD#	Name	Table
0000	WR0	Main Control	7	RD0	Main Status	10
0001		*reserved*	*n/a*	RD1	Receiver Gain Word	11
0010	WR2	Interrupt Mask	8	RD2	Noise Margin	12
0011	WR3	Read Coefficient Select	9	RD3	Coefficient Read Register (lower byte)	13
0100		*reserved*		RD4	Coefficient Read Register (upper byte)	13
0101		*reserved*		RD5	Activation Status	14
0110		*reserved*		RD6	Receiver AGC and FFE Step Gain	15
0111-1001		*reserved*			*reserved*	

WR0—Main Control Register

Address: A3-0 = 0000
Default 00h
Attributes: Write Only
Control Register bits serve the same purpose in Software Mode as the like-named individual pins in Hardware Mode. Table 7 lists bit assignments for the WR0 register.

Table 7: Main Control Register WR0

Bit	Description
b7	**Transmit Test Pattern Enable (TXTST).** Set TXTST to 1 to enable isolated transmit pulse generation. The time between pulses is 6 ms. TDATA controls the sign and TFP controls the magnitude of the transmitted symbols according to the 2B1Q encoding rules. In the HTU-R configuration when the TXTST mode is selected, the Data Pump may begin activation.
b6	**Back-End Loop Back (BELB).** In the Active State, set BELB to 1 to enable an internal, transparent loopback of the HDX RDATA to TDATA and RFP to TFP.
b5	**Front End Loop Back (FELB).** In the HTU-C mode with the Data Pump in the Inactive State, set FELB to 1 to enable an ACC front-end loopback. The Data Pump will begin activation and transmission on the line, but will ignore any signal from the HTU-R instead synchronizing to its own transmit signal.
b4	**Repeater Mode (RPTR).** The RPTR bit is set to 1 and the HTU-C pin is pulled High to program the Data Pump for operation on the side of the HDSL repeater driving the remote HTU-R. RPTR is set to 0 and the HTU-C pin is tied Low to program the Data Pump for operation on the side of the repeater driven by the central office HTU-C.
b3	**Loop Control (LOOPID).** For 2-pair ANSI HDSL applications, LOOPID defines the frame sync word format to encode the loop number in HTU-C mode. Set LOOPID to 0 for Loop1 or to 1 for Loop2. The Data Pump transmits a 7-quat, time-reversed, double-Barker code on Loop2. For 3-pair ETSI HDSL applications, LOOPID should be set to 0 on all loops because the loop number is encoded in the HDSL overhead using the Z bits.
b2	**Insertion Loss Measurement Test (ILMT).** Set ILMT to 1 to enable transmission of a scrambled all ones insertion loss measurement test pattern. In the HTU-R configuration when the ILMT mode is selected, the Data Pump may begin activation.
b1	**Quiet Mode (QUIET).** Set QUIET to 1 to force the Data Pump into the De-Activated State with the transmitter silent. Setting QUIET to 0 will not cause the Data Pump to reactivate. In the HTU-R mode, the Data Pump will not respond to an S0 signal from the HTU-C when QUIET is set to 1, but may activate after QUIET is set to 0 even if the HTU-C transmission has already ceased.
b0	**Activation Request (ACTREQ).** In the HTU-C mode when the Data Pump is in the Inactive State and Quiet is set to 0, setting the ACTREQ bit to 1 will initiate an activation sequence. Because ACTREQ is a level- rather than an edge-triggered signal, it should be reset to 0 again within approximately 25 seconds to prevent the immediate start of another activation cycle if the current activation attempt fails. If an activation attempt fails, the processor should allow the Data Pump to remain in the Inactive State where the transmitter is silent for 32 seconds before generating another activation request to allow the HTU-R to return to the Inactive State. It is possible to shorten this quiet period following a failed activation by implementing additional algorithms described in the section entitled "Activation State Machines."

WR2—Interrupt Mask Register

Address: A3-0 = 0010
Default: 00h
Attributes: Write Only
Table 8 shows the various interrupt masks provided in register WR2.

Table 8: Interrupt Mask Register WR2

Bit	Description
b7:6	***Reserved.*** *Must be set to 0.*
b5	**LOSMSK.** 1=Masked. 0=Not Masked. Interrupt mask for the LOS condition
b4	**LSWTMSK.** 1=Masked. 0=Not Masked. Interrupt mask for the LOSWT condition
b3	**LSWMSK.** 1=Masked. 0=Not Masked. Interrupt mask for the LOSW condition
b2	**ACTMSK.** 1=Masked. 0=Not Masked. Interrupt mask for the TEXP condition and the ACTIVE condition
b1	***Reserved.*** *Must be set to 0.*
b0	**Enable coefficient read register (CRD1).** 1=Enable. 0=Disable. Used in conjunction with WR3 for reading coefficient values.

WR3—Read Coefficient Select Register

Address: A3-0 = 0011
Default: 00h
Attributes: Write Only
Table 9 lists the bit maps used to select the coefficient read from the HDX.

Table 9: Read Coefficient Select Register WR3

Hex Value	Selected Registers	Description
00-07	DFE1-DFE8	DFE coefficients
08-0F	EC1-EC8	Echo Cancellation
10-15	FFE1-FFE6	FFE coefficients 1-6
16-19	*reserved*	
1A	AGC Tap	AGC Tap
1B-FF	*reserved*	

RD0—Main Status Register

Address: A3-0 = 0000
Default: xxh (x=undefined)
Attributes: Read Only

Status Register bits serve the same purpose in Software Mode as the like-named individual pins in Hardware mode. Table 10 lists the bit assignments in this register.

Table 10: Main Status Register RD0

Bit	Active Description
b7	**Timer Expiry (TEXP).** Set to 1 to indicate 30-second timer expiration in the Active State. • Causes interrupt on changing from 0 to 1; masked by ACTMSK = 1. • Latched event; reset on read, with persistence while in the Active State.
b6	**TIP/RING polarity reversed ($\overline{\text{INVERT}}$).** 0 = polarity reversal. Valid only in Active State.
b5	**Change Of Frame Alignment (COFA).** Indicates that re-acquisition of frame sync is in a different position with respect to the last frame position. Does not cause interrupt. Latched event; reset on read
b4	**Loss Of Signal for HTU-R (LOS).** 1 = loss of line signal energy on entering Inactive State.
	Loss of Signal Timer Expiration for HTU-C (LOST). 1 = loss of signal for 1 second on entering Inactive State. • Causes interrupt on transitions from 0 to 1 or 1 to 0 that are masked by LOSMSK = 1. • LOS/LOST is not a latched event.
b3	**Loop Number Control (LOOPID).** 0 = loop 1; 1 = loop 2. Valid only in Active States, 0 in all others *Note: This bit is used only for ANSI systems. The ETSI recommendation defines overhead bits for loop identification.*
b2	**Loss of Sync Word Timer Expiry (LOSWT).** Indicates two seconds of LOSW. • Causes interrupt on changing from 0 to 1; masked when LSWTMSK = 1. • Latched event; reset on read; with persistence while in the Deactivated State.
b1	**Loss of Sync Word (LOSW).** • Causes interrupt on changing from 0 to 1; masked by LSWMSK = 1. • Latched event; reset on read; with persistence while in the Pending Deactivation State.
b0	**Active State (ACTIVE).** 1 = Completion of layer 1 activation. • Causes interrupt on changing from 0 to 1; masked by ACTMSK = 1. • Latched event; reset on read with persistence if still in the Active State.

RD1—Receiver Gain Word Register

Address: A3-0 = 0001
Default: xxh (x=undefined)
Attributes: Read Only

The 8-bit word in this register is the eight most significant bits of the main FFE AGC tap, which, along with the AGC and DAGC values (RD6), represent the receiver gain required to compensate for line loss, and to normalize the receive 2B1Q pulses to a fixed threshold. Bit b7 (sign bit, always 0) is the MSB with bit b0 the LSB. The AGC tap value is determined as follows:

$$\text{AGC Tap} = \sum_{i=0}^{6} b_i * 2^{i-6}$$

Table 11: Receiver Gain Word Register

Bit	Description
b7-b0	**FFE AGC Tap Value** (eight most significant bits).

RD2—Noise Margin Register

Address: A3-0 = 0010
Default: xxh (x=undefined)
Attributes: Read Only

The noise margin of the received signal is an input to the HDSL framer's Activation State Machine. The noise margin must reach a threshold level before the HDSL framer can transition to the fully Active State. The HDX provides a calculated, logarithmic noise margin value used by the HDSL framer. This eight-bit word, stored in register RD2, is available every baud, although updated only every 64 baud. Table 12 shows the noise margin coding. To calculate the SNR, use this equation:

SNR =Noise Margin + 21.5 dB

Error propagation in the DFE and de-scrambler may introduce some fractional errors in this formula, however, the relationship between the SNR and the noise margin remains valid as long as the noise follows a Gaussian distribution.

Since the average period of the calculation is very short (64 baud = 163 µs), the recommended procedure for evaluating transmission quality is to average at least 1000 samples over a 163 ms period.

Table 12: Noise Margin Register RD2
(Noise Margin Coding)

MSB							LSB	Noise
b7	b6	b5	b4	b3	b2	b1	b0	Margin[1]
0	0	1	1	0	1	0	1	+26.5
0	0	1	0	1	1	1	1	+23.5
0	0	1	0	1	0	1	1	+21.5
0	0	1	0	1	0	0	1	+20.5
0	0	1	0	0	1	1	1	+19.5
0	0	1	0	0	1	0	1	+18.5
0	0	1	0	0	1	0	0	+18.0
0	0	1	0	0	0	1	0	+17.0
0	0	1	0	0	0	0	0	+16.0
0	0	0	1	1	1	1	0	+15.0
0	0	0	1	1	1	0	0	+14.0
0	0	0	1	1	0	1	0	+13.0
0	0	0	1	1	0	0	0	+12.0
0	0	0	1	0	1	1	0	+11.0
0	0	0	1	0	1	0	0	+10.0
0	0	0	1	0	0	1	0	+9.0
0	0	0	1	0	0	0	0	+8.0
0	0	0	0	1	1	1	0	+7.0
0	0	0	0	1	1	0	0	+6.0
0	0	0	0	1	0	1	0	+5.0
0	0	0	0	1	0	0	0	+4.0
0	0	0	0	0	1	1	0	+3.0
0	0	0	0	0	1	0	0	+2.0
0	0	0	0	0	0	1	0	+1.0
0	0	0	0	0	0	0	0	0.0
1	1	1	1	1	1	1	0	-1.0
1	1	1	1	1	1	0	0	-2.0
1	1	1	1	1	0	1	0	-3.0
1	1	1	1	1	0	0	0	-4.0
1	1	1	1	0	1	1	0	-5.0
1	1	1	1	0	1	0	0	-6.0

1. Accuracy of noise margin is ±1 dB.

RD3 (LSB), RD4 (MSB)—Coefficient Read Register

Address: RD3 (A3-0 = 0011)
RD4 (A3-0 = 0100)
Default: xxh (x=undefined)
Attributes: Read Only
Coefficient Read Word (read from the HDX) comes from the location configured in the Read Coefficient Select Register (WR3, Address A3-0 = 0011). The HDX updates this word on the rising edge of the receive clock, FS. Read register RD3 is the lower byte, and RD4 is the upper byte.

Table 13: Coefficient Read Register

Bit	Description
b7-b0	**Coefficient Word Value.** RD3 contains the lower byte; RD4 the upper byte.

RD5—Activation Status Register

Address: A3-0 = 0101
Default: xxh (x=undefined)
Attributes: Read Only
The ACT bits indicate the current state of the HDX transceiver during the Activating State as listed in Table 14. (For any state other than the Activating State, the ACT bits will be "0000".)

Table 14: Activation Status Register RD5

ACT Bits 3-0	State in HTU-C Mode	State in HTU-R Mode
0000	Inactive	Inactive
0001	Pre-AGC	Wait
0010	Pre-EC	AAGC
0011	SIGDET	EC
0100	AAGC	PLL1
0101	EC	PLL2
0110	PLL	4LVLDET
0111	4LVLDET	FRMDET
1000	FRMDET	–

RD6—Receive Step Gain Register

Address: A3-0 = 0110
Default: xxh (x=undefined)
Attributes: Read Only

This 8-bit register represents AGC and FFE gain coefficients (GAGC and GFFE, respectively). Bit assignments are listed in Table 15. The approximate line loss (LL) can be determined using these values in the following equation:

$$LL = 20\log_{10}(GFFE * AGC\ tap) + GAGC + 28\ dB$$

GFFE corresponds to DAGC in the HDX and GAGC is from the ACC. Bits ST0-ST2 indicate the Data Pump activation states as shown in Figures 6 and 8 and Table 16.

Table 15: Receiver AGC and FFE Step Gain Register RD6

Bit	Description
b7	**ST2.** Data Pump Activation State–bit 2
b6	**ST1.** Data Pump Activation State–bit 1
b5-b4	**GFFE1, GFFE0.** Digital Gain Word–bit 1 and Digital Gain Word–bit 0. **Bits <5:4>** **GFFE Value** 00 $2^0 = 1$ 01 $2^1 = 2$ 10 $2^2 = 4$ 11 $2^3 = 8$
b3	**ST0.** Data Pump Activation State–bit 0
b2-b0	**GAGC2-GAGC0.** Analog Gain Word–bit 2,1 and 0. **Bits <2:0>** **GAGC Value (dB)** 000 -12 001 -10 010 -8 011 -6 100 -4 101 -2 110 0 111 +2

Activation State Machines

The Data Pump Activation/Start-Up circuitry is compatible with ANSI T1E1.4/94-006. Full HTU-C activation is partitioned between the Data Pump and the framer. Figure 6 represents the HTU-C Data Pump Activation State Machine, and Figure 7 shows the HTU-C framer activation state machine. Figures 8 and 9 present the corresponding HTU-R state machines. Table 16 lays out the correspondence between the Data Pump and Framer state machines. In Software Mode, the ST*n* bits in Read Register 6 (ADDR 0110) show the current status of the state machine.

HTU-C Data Pump Activation

When the HTU-C Data Pump is powered up and reset is applied, the chip is in the Inactive State as shown at the top of Figure 6. Starting at the Inactive State, the device progresses in a clockwise direction through the Activating, Active-1, Active-2, Pending De-Activation and De-Activated States.

In the hardware mode when the Data Pump is in the Inactive State and the QUIET pin is Low, a Low-to-High transition on the ACTREQ pin initiates activation of the link. In the software mode when the Data Pump is in the Inactive State and the QUIET bit is set to 0, setting the ACTREQ bit to 1 initiates activation of the link. Because the ACTREQ control bit is level sensing, it should be set to 1 and then reset to 0 again within 25 seconds to generate a single activation request.

During the Activating State, the echo canceller, equalizer and timing recovery circuits are all adapting during the simultaneous transmission and reception of the framed, scrambled-ones data transmitted as a two-level code (S0) or as the four-level code (S1). If the receive frame sync word is not detected in two consecutive frames within 30 seconds, the timer expires and the device moves to the De-Activated State and ceases transmission. It will then immediately transition to the Inactive State (setting LOST regardless of whether HTU-R transmission has ceased). Another activation request should not be generated for 32 seconds allowing the HTU-R to timeout, detect LOS and move from the De-Activated to the Inactive State. In microprocessor-based systems, this time may be shortened by implementing a processor routine to reset the HTU-R Data Pumps which are in the Activating State when no HTU-C signal is present.

Successful detection of the sync word drives the State machine to the Active-1 State. This is indicated by a 0-to-1 transition of the ACTIVE bit (Software Mode). If the HTU-C Data Pump remains locked to the sync word until the Activation Timer expires, the device transitions to the Active-2 (fully active) State. If sync is lost, as indicated by a 0-to-1 transition on LOSW, the HTU-C Data Pump transitions to the Pending De-Activation State.

In Pending De-Activation, the HTU-C Data Pump progresses to the De-Activated and Inactive States with the expiration of the respective timers. If the sync word is detected before the LOSW timer expires, the HTU-C Data Pump returns to either Active 1 or Active-2. (The HTU-C Data Pump returns to whichever state it occupied before transitioning to Pending De-Activation.)

The HTU-C Data Pump will exit the Active-2 State in one of two ways. A Low-to-High transition on the QUIET pin (Hardware Mode) or the QUIET bit (Software Mode), forces the HTU-C Data Pump directly to the De-Activated State. The only other means of exiting the Active State is through a loss of receive sync word (LOSW). LOSW is set when six consecutive frames occur without a sync word match. The LOSW event puts the HTU-C Data Pump into the Pending De-Activation State.

The HTU-C Data Pump remains in the Pending De-Activation State for a maximum of two seconds. If a sync word is detected within two seconds after the LOSW event, the HTU-C Data Pump reenters the Active State. If the LOSW condition exceeds two seconds, an LOSWT event occurs which sends the chip to the De-Activated State. When the De-Activated State is reached from Pending De-Activation, the HTU-C Data Pump returns to the Inactive State and declares LOST when it detects no signal from the HTU-R for one second. The Data Pump should remain in the Inactive State for 15 seconds before another activation attempt.

Table 16: Data Pump/Framer Activation State Machine Correspondences

ST2	ST1	ST0	Data Pump State	Framer State
0	0	0	Inactive	Idle
0	0	1	Activating – 30 s timer running	Idle
0	1	0	Active – 30 s timer running (Active-1)[1]	Idle, Active-R or Active-T, or Link Active
0	1	1	Active – 30 s timer expired (Active-2)[1]	Link Active
1	0	0	Pending De-Activation[1]	Link Active or Active-R or Active-T
1	0	1	De-Activated	Idle
1	1	0	*unused*	*unused*
1	1	1	*unused*	*unused*

1. The data pump samples the TDATA input for all transmit data except the 14 sync bits at the start of each frame during states 010, 011 and 100.

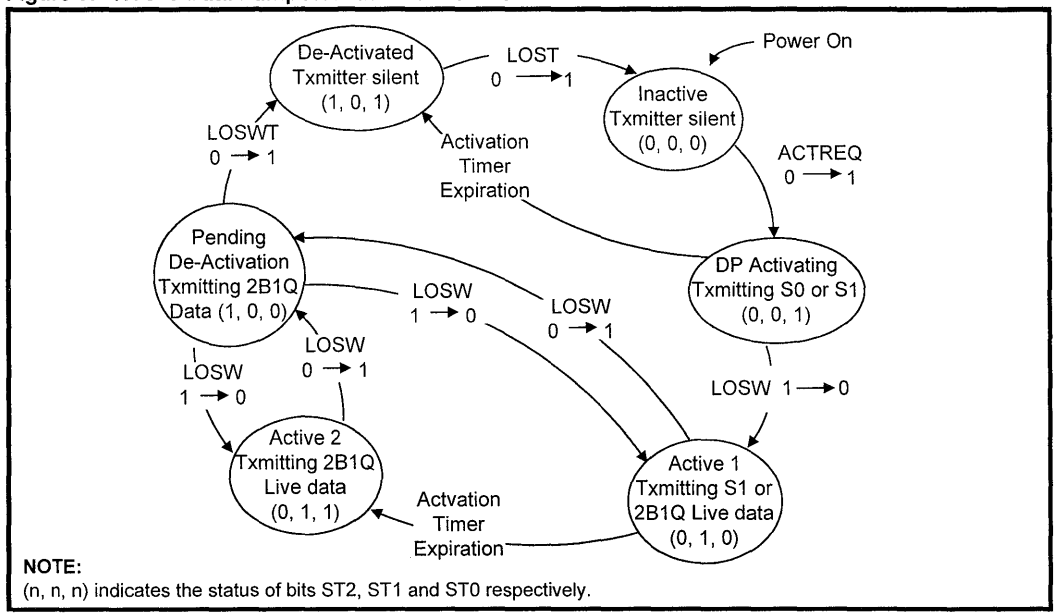
HTU-C Framer Activation

Figure 7 shows the activation state machine for the HTU-C HDSL framer. Transition to the Link Active stage from the Idle stage (upper left) requires successful exchange of a pair of indicator bits, **indc** and **indr**. ("INDC" and "INDR" are internal status signals within the HDSL framer; "**indc**" and "**indr**" are bits in the overhead channel.) The HTU-C device transmits the **indc** bit, and the HTU-R device transmits the **indr** bit. The overhead frame carries these indicator bits during transmission of the S1 training pattern.

Figure 7 illustrates the two partially active states (Active-R and Active-T) which may serve as transitions between the Idle and Link Active States. If the HTU-C device reaches the SNR threshold, its framer sets the INDC bit and the device transitions to the Active-R State. If the HTU-R device reaches the SNR threshold, it will transmit the **indr** bit to the HTU-C. The HTU-C will then transition to the Active-T State. From either of the partially Active States, the devices transition to the full Link Active State only with both Indication bits set.

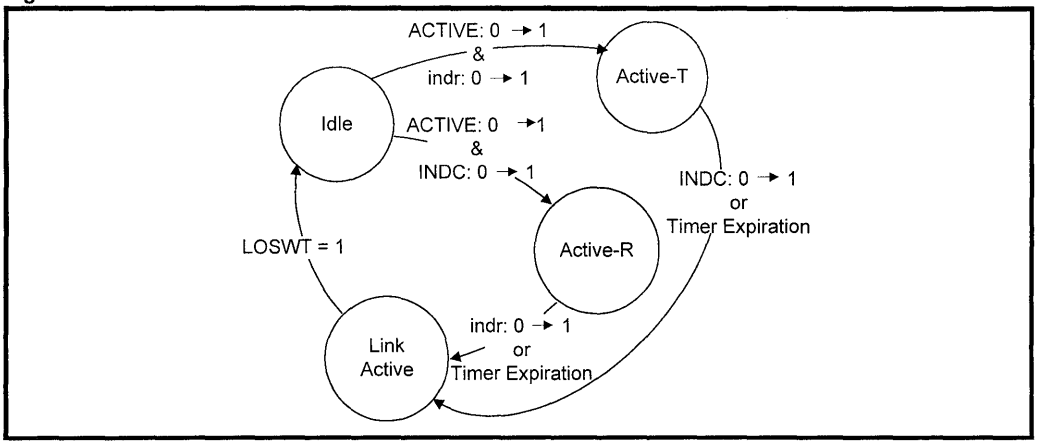
Upon entering the Active States (Active-R, Active-T or Link Active), the chip will open up the full duplex communication link with the HTU-R. Only the Active and Pending De-Activation States allow full payload transmission. In all states except Active-1 and Active-2, the RDATA output is clamped High.

Figure 6: HTU-C Data Pump Activation State Machine



NOTE:
(n, n, n) indicates the status of bits ST2, ST1 and ST0 respectively.

Figure 7: HTU-C HDSL Framer Activation State Machine



HTU-R Data Pump Activation

Figures 8 and 9 represent the HTU-R Data Pump Activation State Machine and the HTU-R HDSL Framer State Machine. The activation state machines for HTU-R and HTU-C devices are similar. Both Data Pump machines start at the Inactive State and progress clockwise through the Activating, Active-1, Active-2, Pending De-Activation, and De-Activated States. One difference between them is in the initial condition required to exit from the Inactive State. The HTU-C Data Pump responds to the Activation Request (ACTREQ) signal. The HTU-R device responds only to the presence of signal energy on the link. Thus, only an active HTU-C device can bring up the link. Once the HTU-C begins transmitting, the HTU-R device will automatically activate and attempt synchronization.

The other difference between the Data Pump state machines is the impetus for the change from the De-Activated to the Inactive State. In the HTU-C Data Pump, expiration of a one-second loss of signal timer (LOST) causes the transition. In the HTU-R the transition occurs immediately on Loss of Signal (LOS).

HTU-R Framer Activation

The HDSL framer activation state machines for HTU-C and HTU-R are also similar. The difference is in the indicator bits which cause the transition to either the Active-T or Active-R State. On the HTU-R side, the INDR bit causes the transition to the Active-R State, and the **indc** bit causes the transition to the Active-T State. From either partially active state, receipt of the remaining indicator bit or timer expiry causes the transition to the full Link Active State.

HDSL Synchronization State Machine

Figure 10 shows the HDSL Synchronization State Machine incorporated in the HDX. It applies to both HTU-C and HTU-R devices. Table 17 lists the correspondence between the Synchronization states and Activation states. The Sync state machine is clocked by the receive signal framing. Starting at the initial Out-of-Sync condition (State 0), the device progresses in a clockwise direction through State 1 until Sync is declared in State 2. Two consecutive frame sync word matches are required to achieve synchronization.

Once the In-Sync condition is declared, six consecutive frame sync mismatches will cause the device to transition through States 3 through 7 and declare an Out-of-Sync condition in State 8. From State 8, the device will return either to State 2 or to State 0. If the 2-second timer expires without reestablishing frame sync (LOSWT = 1) or if the receive signal is lost entirely (LOS = 1), the device returns directly to State 0.

If frame sync is reestablished, the device will return to the In-Sync condition (State 2) through State 9 if two consecutive frames are received without any change of frame alignment (COFA = 0). If a change of frame alignment does occur (COFA = 1), two consecutive matches are required to transition through State 10 back to State 2.

Table 17: Activation – Synchronization

Activation State	Synchronization States
Inactive	State 0
Activating	State 1
Active	States 2, 3, 4, 5, 6, and 7
Pending De-Activation	States 8, 9, and 10

Figure 8: HTU-R Data Pump Activation State Machine

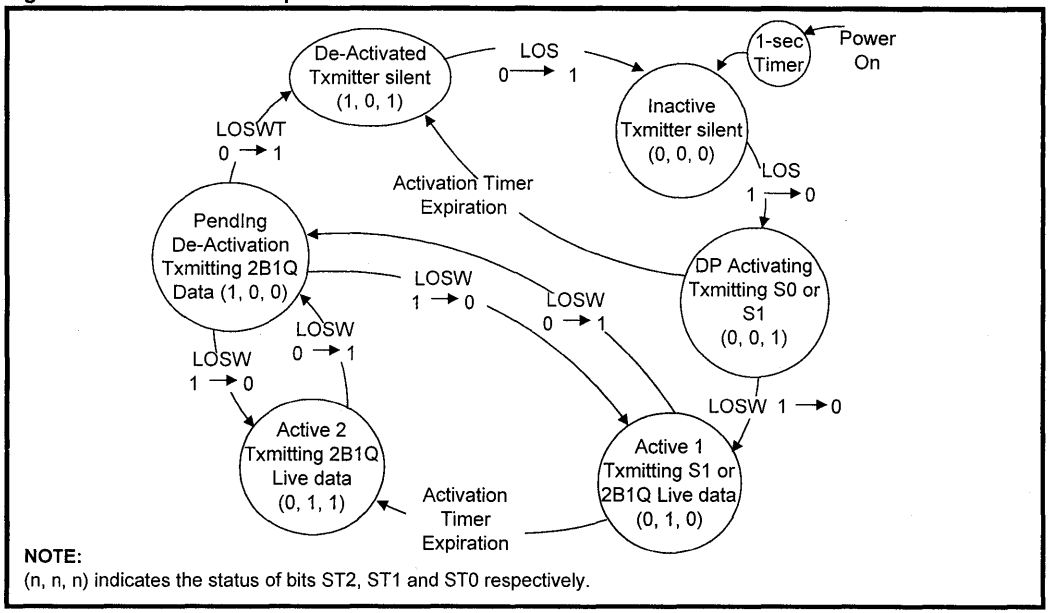


Figure 9: HTU-R HDSL Framer Activation State Machine

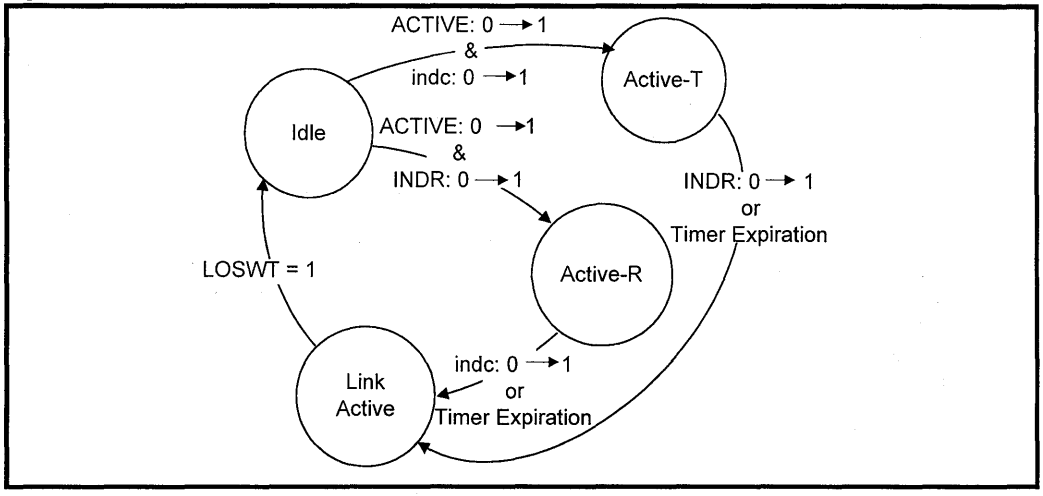
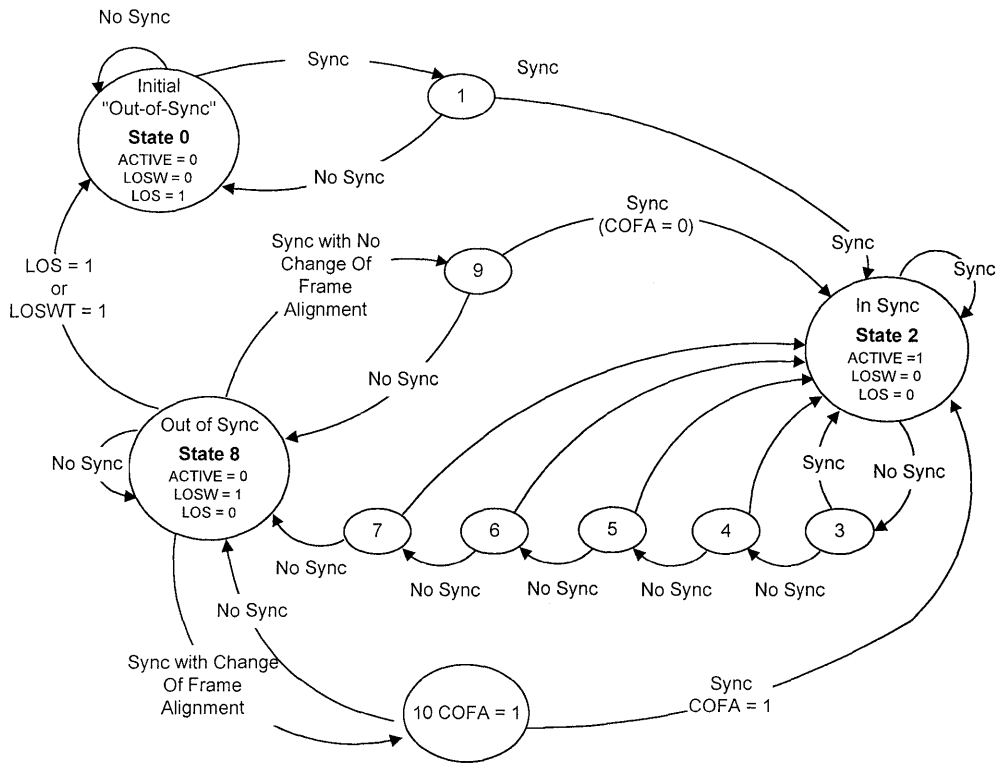


Figure 10: HDSL Synchronization State Machine



NOTES:

1. "Sync" = Frame Sync Word Match. "No Sync" = Frame Sync Word Mismatch.
2. A 0-to-1 transition on QUIET will set the Sync State Machine from any State to State 0.
3. Expiration of the Activation Timer will set the Sync State Machine from State 1 to State 0.

7

APPLICATION INFORMATION

HDSL Framer State Machine Design

Because of data transparency characteristics of the Data Pump, two issues impact on implementing the HDSL Framer Activation State machines for both HTU-C and HTU-R devices:

1. Once the ACTIVE 0-to-1 transition occurs, the Data Pump becomes transparent. Therefore, the HDSL framer must put appropriate data in TDATA. Table 5 summarizes this requirement.
2. The link indicator bits (**indc** and **indr**) must stabilize before the device makes the transition from the Idle to the Active-T State. Thus, the HDSL framer design may detect 6 consecutive matches for the indication bit transition. This is particularly important for non-CSA loops where a lower SNR may be experienced.

PCB Layout

The following are general considerations for PCB layout using the HDSL Data Pump chip set:

- Refer to Figures 12 and 13, and Table 18. Keep all shaded components close to the pins they connect to.
- Use a four-layer or more PCB layout, with embedded power and ground planes.
- Break up the power and ground planes into the following regions. Tie these regions together at the common point where power connects to the circuit:
  - Digital Region
  - Analog Region
    - –VCXO subregion
    - –ACC, Line I/F, and IBIAS subregion
- Use larger feedthroughs ("vias") and tracks for connecting the power and ground planes to the power and ground pins of the ICs than for signal connections. Place the decoupling capacitors right at the feedthrough power/ground plane ties, or on the tracks to the IC power/ground pins as close to the pins as possible.
- On the User Interface Connector, route digital signals to avoid proximity to the TIP, RING, and CT lines.
- Provide at least 100 µF or more of bulk power supply decoupling at the point where power is connected to the Data Pump circuit.

Digital Section

- Keep all digital traces separated from the analog region of the Data Pump layout.
- Provide high frequency decoupling capacitors (0.01 µF ceramic or monolithic) around the HDX as shown in Figures 12 and 13.
- It is possible to replace the NAND gate (shown in Figure 13) with an AND gate.

Analog Section

The analog section of the PCB consists of the following subsections:

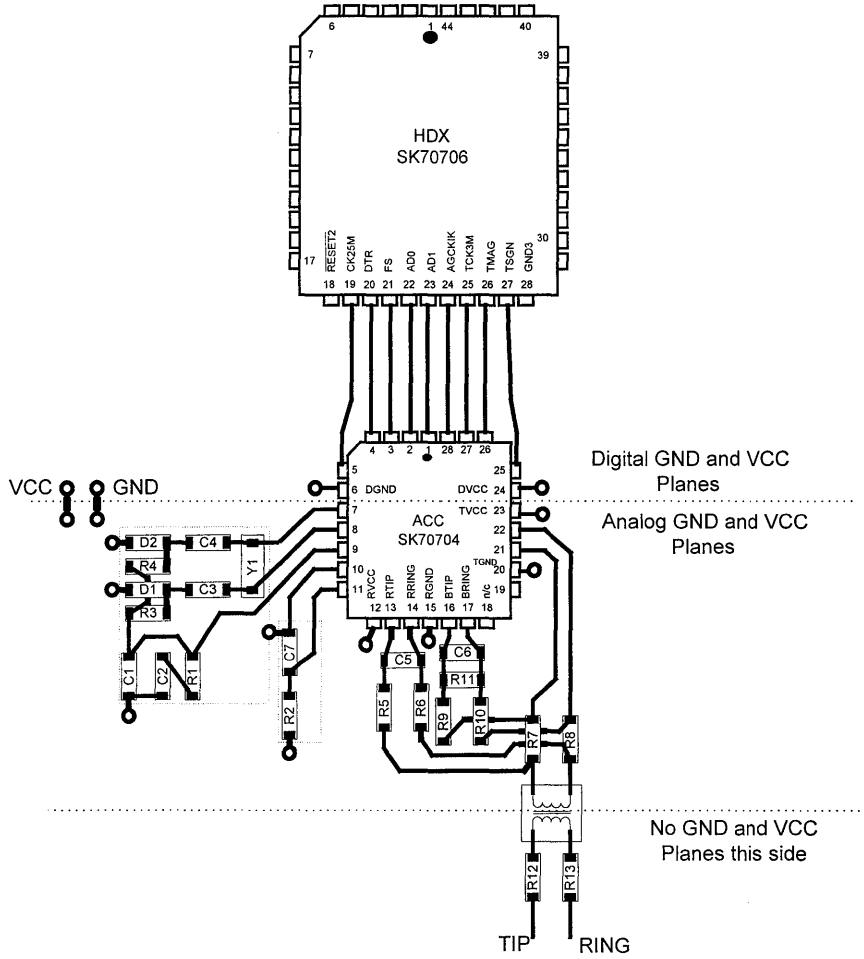
1. ACC and power supply decoupling capacitors
2. Bias Current Generator
3. Voltage Controlled Crystal Oscillator
4. Line Interface Circuit
   - Route digital signals AD0, AD1, FS, DTR, TSGN, TMAG, TCK3M, and AGCKIK on the solder side of the PCB, and route all analog signals on the component side as much as possible.
   - Route the following signal pairs as adjacent traces:
     - TTIP/TRING
     - BTIP/BRING
     - RTIP/RRING

     but keep the pairs separated from each other as much as possible.
   - Do not run the analog ground plane under the transformer line side to maximize high voltage isolation.

User Interface

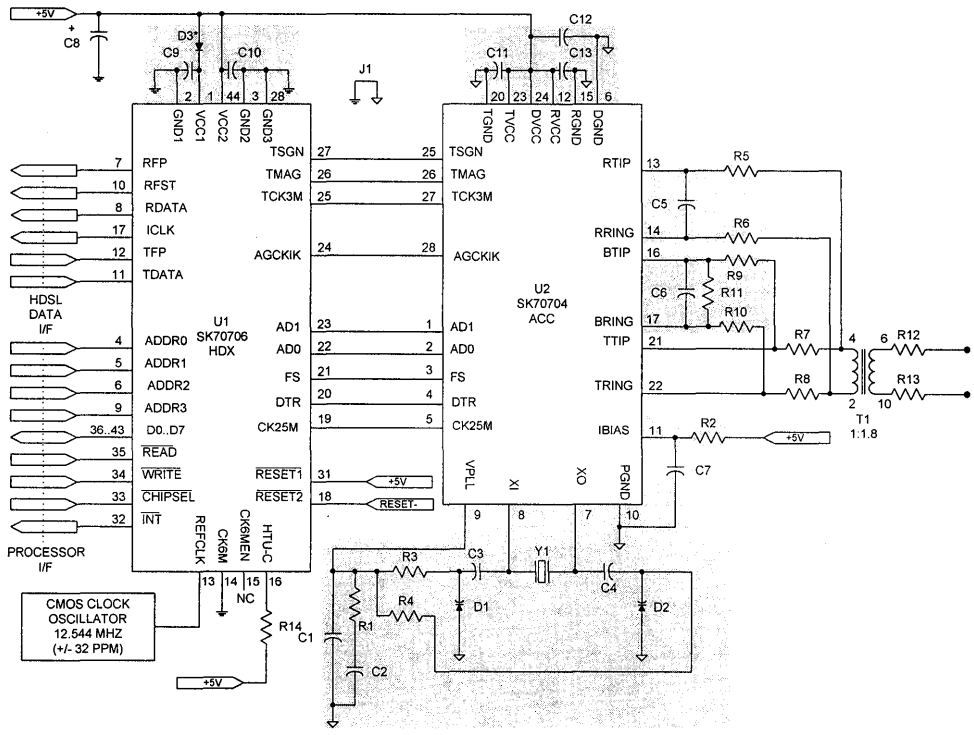
The REFCLK and CK6M signals are sensitive to capacitive loading and rise time. Keep the rise time (from 10%-90%) for these signals less than 5 ns.

Figure 11: PCB Layout Guidelines



NOTE: The VCC and GND planes for Digital and Analog sides should be connected at a single point.

Figure 12: Typical Support Circuitry for HTU-C Applications



NOTES:
The HDX and ACC should have independent ground planes connected at a single point.
Diode D3 is optional.

Table 18: Components for Suggested Circuitry (See Figures 12 and 13)

Ref	Description	Ref	Description	Ref	Description
C1, 9, 10	0.01 µF, ceramic, 10%	R1	5.11 kΩ, 1%	R12, 13	5.6 Ω, line feed fuse resistor (ALFR-2-5.6-1 IRC)
C2	100 µF, electrolytic, 20% low leakage ≤5 µA @ 25° C	R2	35.7 kΩ, 1%		
		R3, 4	20.0 kΩ, 1%	D1, 2	Varicap diode (Motorola MV209)
C3, 4	1000 pF, ceramic, 20%	R5, 6	301 Ω, 1%	D3	Silicon rectifier diode (1N4001)
C5, 6	470 pF, COG or mica, 10%	R7, 8[1]	18.2 Ω, 1%	Y1	25.088 MHz crystal (Hy-Q International 80546/1)
C7, 11-13	0.1 µF, ceramic, 10%	R9, 10	604 Ω, 1%		
C8	100 µF, electrolytic, 20%	R11	909 Ω, 1%	T1	1:1.8 (Midcom 671-7376 or Pulse Engineering PE-68614)
		R14,R15	10.0 kΩ, 1%		

1. R7, R8 should be 20 Ω, when R12 and R13 (the 5.6 Ω fuse links) are not used.

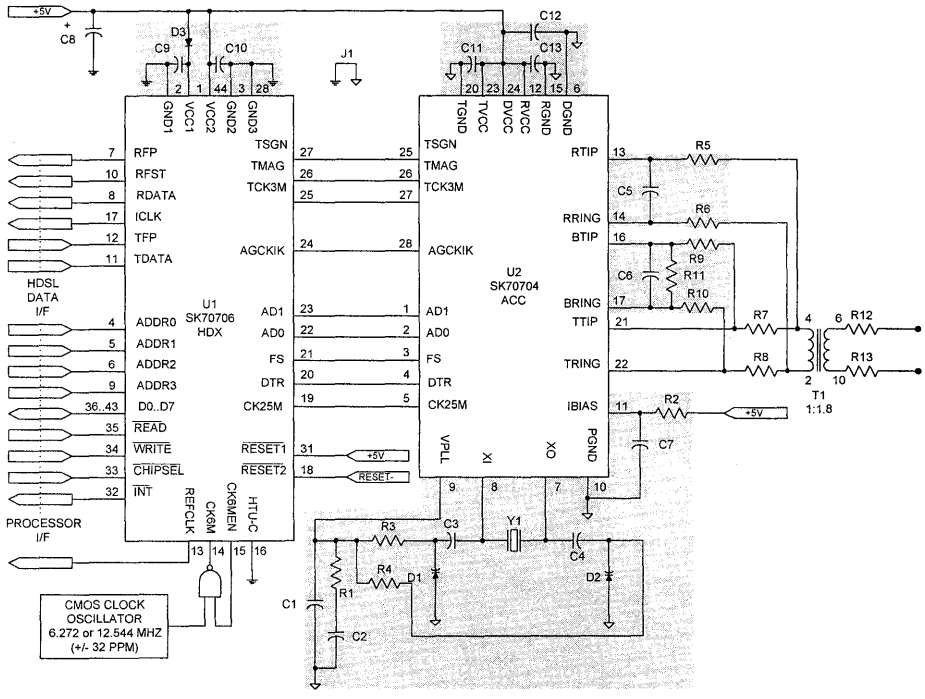
Table 19: Transformer Specifications
(Figures 12 and 13, Reference T1)

Measure	Value	Tolerance
Turns Ratio (IC:Line)	1:1.8	±1%
Secondary Inductance (Line Side)	2.75 mH	±6%
Leakage Inductance	≤ 50 µH	
Interwinding Capacitance	≤ 60 pF	
THD	≤ -70 dB	
Longitudinal Balance	≥ 50 dB	5-196 kHz
Return Loss	≥ 20 dB	40-200 kHz
Isolation	2000 VRMS	
Primary DC Resistance	≤ 3.2 Ω	
Secondary DC Resistance	≤ 6.0 Ω	
Operating Temperature	-40 to +85° C	

Table 20: Crystal Specifications
(Figures 12 and 13, Reference Y1)

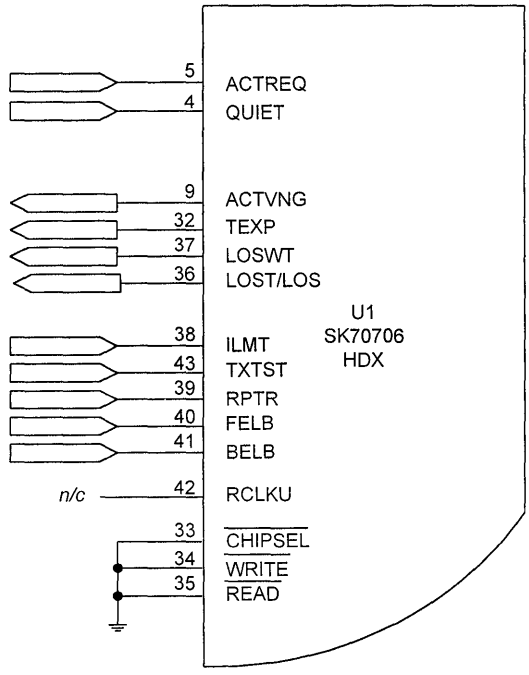
Measure	Value	Tolerance
Calibration Frequency	25.088 MHz @C_L = 20 pF	+0-+40 ppm
Mode	Fundamental, Parallel Resonance	
Pullability (C_L = 24 pF ⇨ 16 pF)	≥ +160 ppm	
Operating Temperature	-40-+85 ° C	
Temperature Drift	≤ ±30 ppm	
Aging Drift	≤ 5 ppm/year	
Series Resistance	≤ 15 Ω	
Drive Level	0.5 mW	
Holder	HC-49	

Figure 13: Typical Support Circuitry for HTU-R Applications



NOTES:
The HDX and ACC should have independent ground planes connected at a single point.
Diode D3 is optional.

Figure 14: SK70706 HDX Control and Status Signals (Stand-alone Mode)



NOTE:
This figure illustrates the HDX control and status signals in stand-alone mode. All other HDX and ACC signals are connected as shown in Figures 12 and 13.

TEST SPECIFICATIONS

NOTE

The minimum and maximum values in Tables 21 through 31 and Figures 14 through 20 represent the performance specifications of the Data Pump and are guaranteed by test, except where noted by design.

Table 21: ACC Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Supply voltage[1] reference to ground[2]	TVCC, RVCC, DVCC	-0.3	+6.0	V
Input voltage[2, 3], any input pin	TVCC, RVCC, DVCC	- 0.3V	VCC + 0.3	V
Continuous output current, any output pin	–	–	±25	mA
Storage temperature	TSTOR	-65	+150	° C

CAUTION

Operations at the limits shown may result in permanent damage to the Analog Core Chip. Normal operation at these limits is neither implied nor guaranteed

1. No supply input may have a maximum potential of more than ±0.3 V from any other supply input.
2. TGND = 0V; RGND = 0V; DGND = 0V.
3. TVCC = RVCC = DVCC = VCC.

Table 22: ACC Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
DC supply	TVCC, DVCC, RVCC	4.75	5.0	5.25	V
Ambient operating temperature	TA	-40	+25	+85	° C

Table 23: ACC DC Electrical Characteristics (Over Recommended Range)

Parameter	Sym	Min	Typ[1]	Max	Unit	Test Conditions
Supply current (full operation)	ICC	–	92	120	mA	83 Ω resistor across TTIP and TRING
DVCC current		–	3	6	mA	
RVCC current		–	26	33	mA	
TVCC current		–	63	79	mA	Normal Mode 8+3, 8-3, 8+3, ...
		–	38	48	mA	Off Mode
Input Low voltage	VIL	–	–	0.5	V	IIL < 40 µA
Input High voltage	VIH	4.5	–	–	V	IIH < 40 µA
Output Low voltage	VOL	–	–	0.2	V	IOL < 40 µA
Output High voltage	VOH	4.5	–	–	V	IOH < 40 µA

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.
2. Applies to pins 3, 4, 25, 26 and 27.

Table 23: ACC DC Electrical Characteristics (Over Recommended Range) – continued

Parameter	Sym	Min	Typ[1]	Max	Unit	Test Conditions
Input leakage current[2]	I_{IL}	–	–	±50	µA	$0 < V_{IN} < V_{CC}$
Input capacitance (individual pins)	C_{IN}	–	12	–	pF	
Load capacitance (REFCLK output)	C_{LREF}	–	–	20	pF	

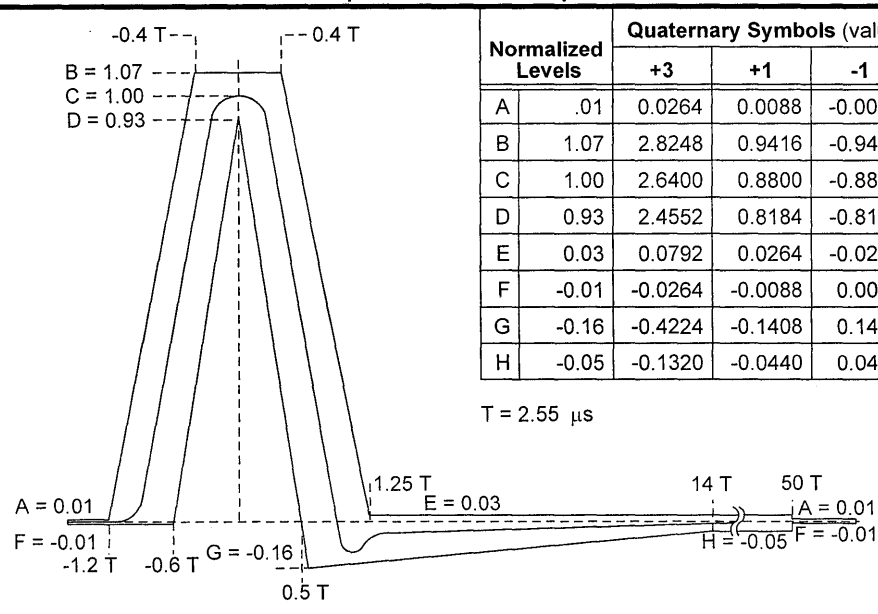
1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.
2. Applies to pins 3, 4, 25, 26 and 27.

Table 24: ACC Transmitter Electrical Parameters (Over Recommended Range)

Parameters	Sym	Min	Typ	Max	Unit	Test Conditions
Isolated pulse height at TTIP, TRING		+2.455	+2.640	+2.825	Vp	TDATA High, TFP Low (+3)
		-2.825	-2.640	-2.455	Vp	TDATA Low, TFP Low (-3)
		+0.818	+0.880	+0.941	Vp	TDATA High, TFP High (+1)
		-0.941	-0.880	-0.818	Vp	TDATA Low, TFP High (-1)
Setup time (TSGN, TMAG)	tTSMSU	5	–	–	ns	
Hold time (TSGN, TMAG)	tTSMH	12	–	–	ns	

1. Pulse amplitude measured across a 135 Ω resistor on the line side of the transformer using the application circuit shown in Figure 12 and Table 18.

Figure 15: ACC Normalized Pulse Amplitude Transmit Template



Normalized Levels		Quaternary Symbols (values in Volts) +3	+1	-1	-3
A	.01	0.0264	0.0088	-0.0088	-0.0264
B	1.07	2.8248	0.9416	-0.9416	-2.8248
C	1.00	2.6400	0.8800	-0.8800	-2.6400
D	0.93	2.4552	0.8184	-0.8184	-2.4552
E	0.03	0.0792	0.0264	-0.0264	-0.0792
F	-0.01	-0.0264	-0.0088	0.0088	0.0264
G	-0.16	-0.4224	-0.1408	0.1408	0.4224
H	-0.05	-0.1320	-0.0440	0.0440	0.1320

T = 2.55 µs

Figure 16: ACC Transmitter Timing

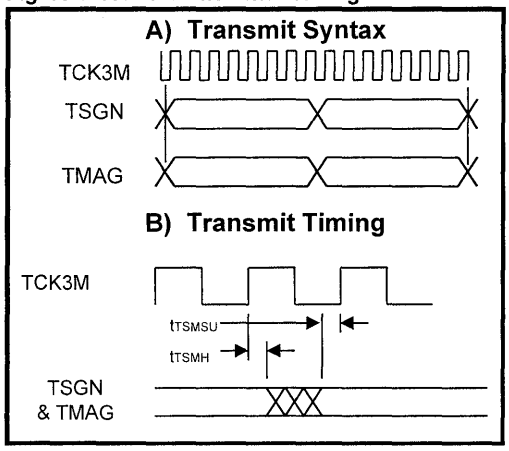


Figure 17: ACC Transmit Power Spectral Density

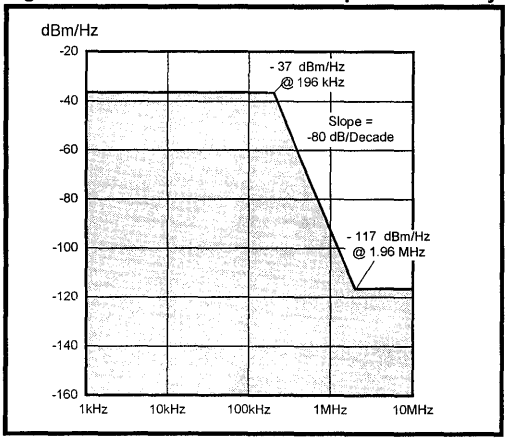


Table 25: ACC Receiver Electrical Parameters (Over Recommended Range)

Parameter	Sym	Min	Typ	Max	Unit	Test Conditions
Propagation delay (AD0, AD1)	tADD	–	–	25	ns	
Total harmonic distortion		–	-80	–	dB	V(RTIP, RRING) = 3 Vpp @ 50 kHz
RTIP, RRING, to BTIP, BRING gain ratio		–	1.0	1%	V/V	

7

Figure 18: ACC Receiver Syntax and Timing

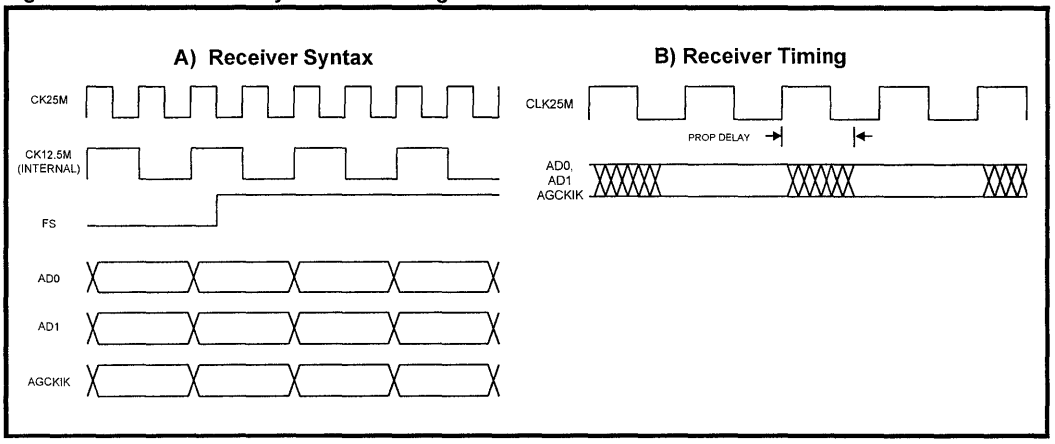


Table 26: HDX Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Supply voltage[1] reference to ground[2]	VCC2, VCC1	-0.3	+6.0	V
Input voltage[2], any input pin	–	- 0.3	VCC2 + 0.3	V
Continuous output current, any output pin	–	–	±25	mA
Storage temperature	TSTOR	-65	+150	° C

CAUTION

Operations at the limits shown may result in permanent damage to the HDSL Digital Transceiver (HDX). Normal operation at these limits is neither implied nor guaranteed

1. The maximum potential between VCC2 and VCC1 must never exceed ±1.2 V.
2. GND3 = 0V; GND2 = 0V; GND1 = 0V.

Table 27: HDX Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
DC supply	VCC1[1]	3.95	5.0	5.25	V
	VCC2	4.75	5.0	5.25	V
	VCC2-VCC1	-0.25	–	+0.9	V
Ambient operating temperature	TA	-40		+85	° C

1. To derive this supply, a 1N4001 (or equivalent) diode may be connected between VCC2 and VCC1 as shown in Figures 12 and 13. The diode should be selected to meet VCC1 minimum specifications.

Table 28: HDX DC Electrical Characteristics (Over Recommended Range)

Parameter	Sym	Min	Typ[1]	Max	Unit	Test Conditions
Supply current (full operation)		–	100	175	mA	
Input Low voltage	VIL	–	–	0.5	V	IIL < 40 µA
Input High voltage	VIH	4.0	–	–	V	IIH < 40 µA
Output Low voltage	VOL	–	–	GND +0.3	V	IOL < 40 µA
Output High voltage	VOH	VCC2-0.5	–	–	V	IOH < 40 µA
Input leakage current[2]	IIL	–	–	±50	µA	$0 < V_{IN} < V_{CC_2}$
Tristate leakage current[3]	ITOL	–	–	±30	µA	$0 < V < V_{CC_2}$
Input capacitance (individual pins)	CIN	–	12	–	pF	
Load capacitance (REFCLK output)	CLREF	–	–	15	pF	

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.
2. Applies to pins 4, 5, 11, 12, 14, 16, 18, 19, 22, 23, 24, 29, 31, 33, 34 and 35. Applies to pins 5, 6, 9, 13, and 36-43, when configured as inputs.
3. Applies to pins 7, 8, 10, 15, 17, 30, 32 and 36-43, when tristated.

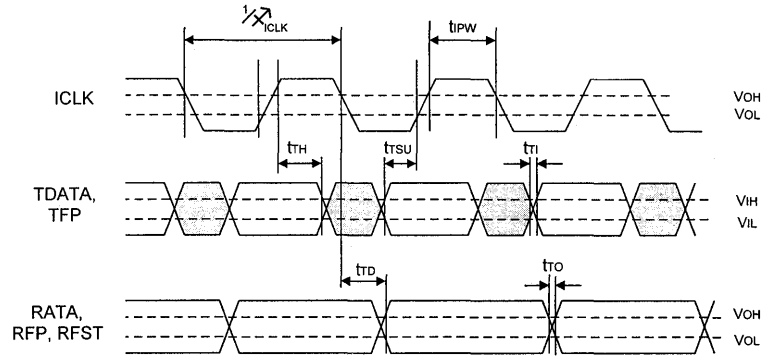
Table 29: HDX/HDSL Data Interface Timing Specifications *(See Figure 18)*

Parameter	Symbol	Min	Typ[1]	Max	Unit
ICLK frequency	f_{ICLK}	–	784	–	kHz
REFCLK frequency	f_{REFCLK}	–	12.544	–	MHz
REFCLK frequency tolerance (HTU-C Mode)	tol_{RCLK}	-32	0	+32	ppm
CK6M frequency tolerance (HTU-R Mode)[2]	tol_{CK6M}	-32	0	+32	ppm
ICLK pulse width high	t_{IPW}	–	638	–	ns
Transition time on any digital output[3]	t_{TO}	–	5	10	ns
Transition time on any digital input	t_{TI}	–	–	25	ns
TDATA, TFP setup time to ICLK rising edge	t_{TSU}	100	–	–	ns
TDATA, TFP hold time from ICLK rising edge	t_{TH}	100	–	–	ns
RDATA, RFP, RFST delay from ICLK falling edge	t_{TD}	0	–	150	ns
TFP pulse width[4]	t_{TFPW}	1248	1276	1304	ns
TFP falling edge to ICLK rising edge[4]	t_{TFIR}	480	–	610	ns
TFP setup time to REFCLK rising edge[4]	t_{TSUR}	25	–	–	ns

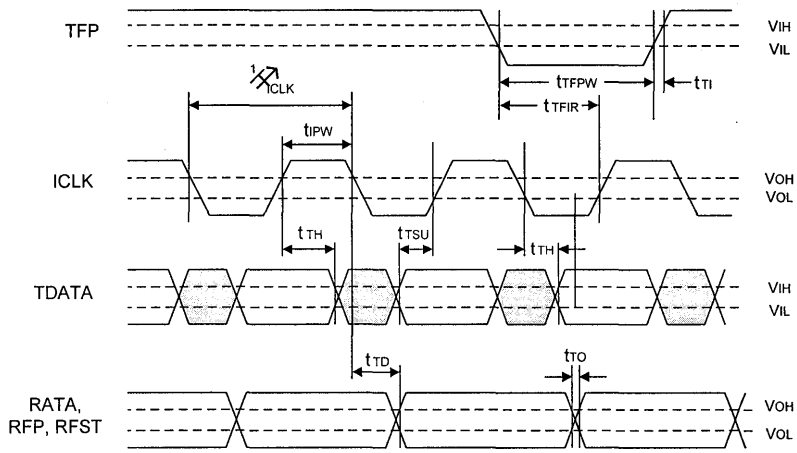
1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.
2. CK6M must meet this tolerance about an absolute frequency of 6.272000 MHz or 12.544000 MHz in HTU-R mode.
3. Measured with 15 pF load.
4. These parameters apply only to an HTU-C mode Data Pump programmed for repeater applications as shown in Figure 19.

Figure 19: HDX/HDSL Data Interface Timing

A) Non-Repeater Mode



B) Repeater Mode



C) Repeater Mode

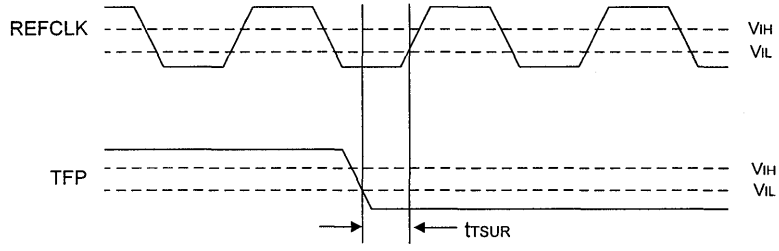


Table 30: HDX/Microprocessor Interface Timing Specifications *(See Figures 19 and 20)*

Parameter	Symbol	Min	Typ	Max	Unit
$\overline{\text{RESET2}}$ pulse width Low	tRPWL	0.1	–	1,000	µs
$\overline{\text{RESET2}}$ to $\overline{\text{INT}}$ clear (10 kΩ resistor from $\overline{\text{INT}}$ to VCC2)	tINTH	–	–	300	ns
$\overline{\text{RESET2}}$ to data tristate on D0-7	tDTHZ	–	–	100	ns
$\overline{\text{CHIPSEL}}$ pulse width Low	tCSPWL	200	–	–	ns
$\overline{\text{CHIPSEL}}$ Low to data active on D0-7	tCDLZ	–	–	80	ns
$\overline{\text{CHIPSEL}}$ High to data tristate on D0-7	tCDHZ	–	–	80	ns
$\overline{\text{READ}}$ pulse width Low	tRSPWL	100	–	–	ns
$\overline{\text{READ}}$ Low to data active	tRDLZ	–	–	80	ns
$\overline{\text{READ}}$ High to data tristate	tRDHZ	–	–	80	ns
Address to valid data	tPRD	–	–	80	ns
Address setup to $\overline{\text{WRITE}}$ rising edge	tASUW	20	–	–	ns
Address hold from $\overline{\text{WRITE}}$ rising edge	tAHW	10	–	–	ns
$\overline{\text{WRITE}}$ pulse width Low	tWPWL	100	–	–	ns
Data setup to $\overline{\text{WRITE}}$ rising edge	tDSUW	20	–	–	ns
Data hold from $\overline{\text{WRITE}}$ rising edge	tDHW	10	–	–	ns
$\overline{\text{READ}}$ High to $\overline{\text{INT}}$ clear when reading register RD0	tINTR	–	–	400	ns

1. Timing for all outputs assumes a maximum load of 30 pF.
2. "Address" refers to input signals CHIPSEL, A0, A1, A2, and A3. "Data" refers to I/O signals D0, D1, D2, D3, D4, D5, D6, and D7.

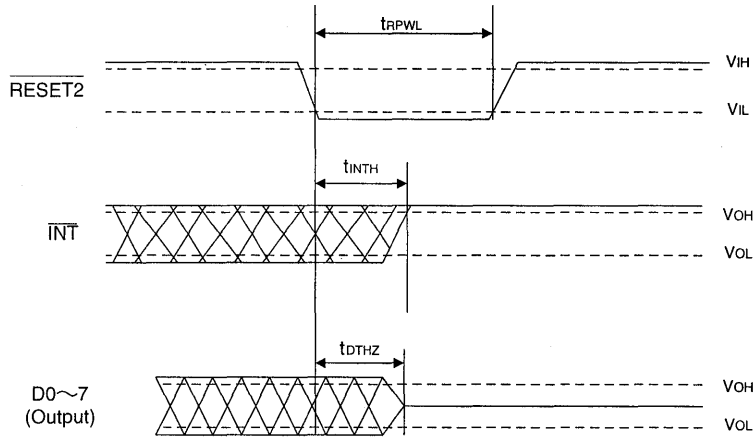
Table 31: General System and Hardware Mode Timing

Parameter		Min	Typ[1]	Max	Unit
Throughput delay	TDATA to TTIP/TRING	–	10.2	12.5	µs
	RTINP/RRING to RDATA	–	53.6	72	µs
Hardware Mode	"ACTREQ" input transitional pulse width (High or Low)	5	–	–	µs
	"QUIET" transitional pulse width (High-to-Low)	5	–	–	µs

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 20: RESET and INTERRUPT Timing (μP Control Mode)

A) Reset Timing



B) Interrupt Timing

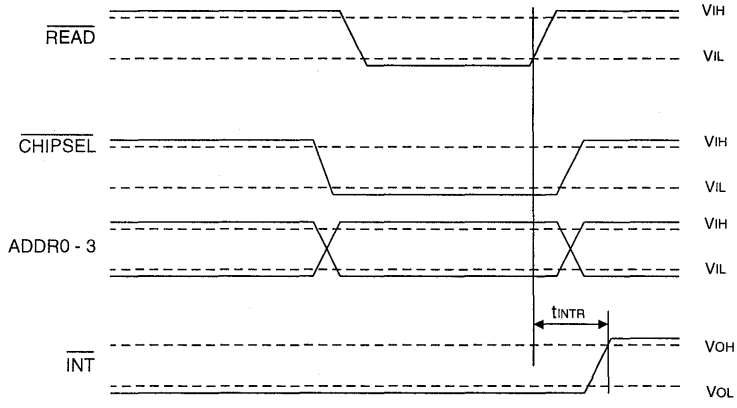
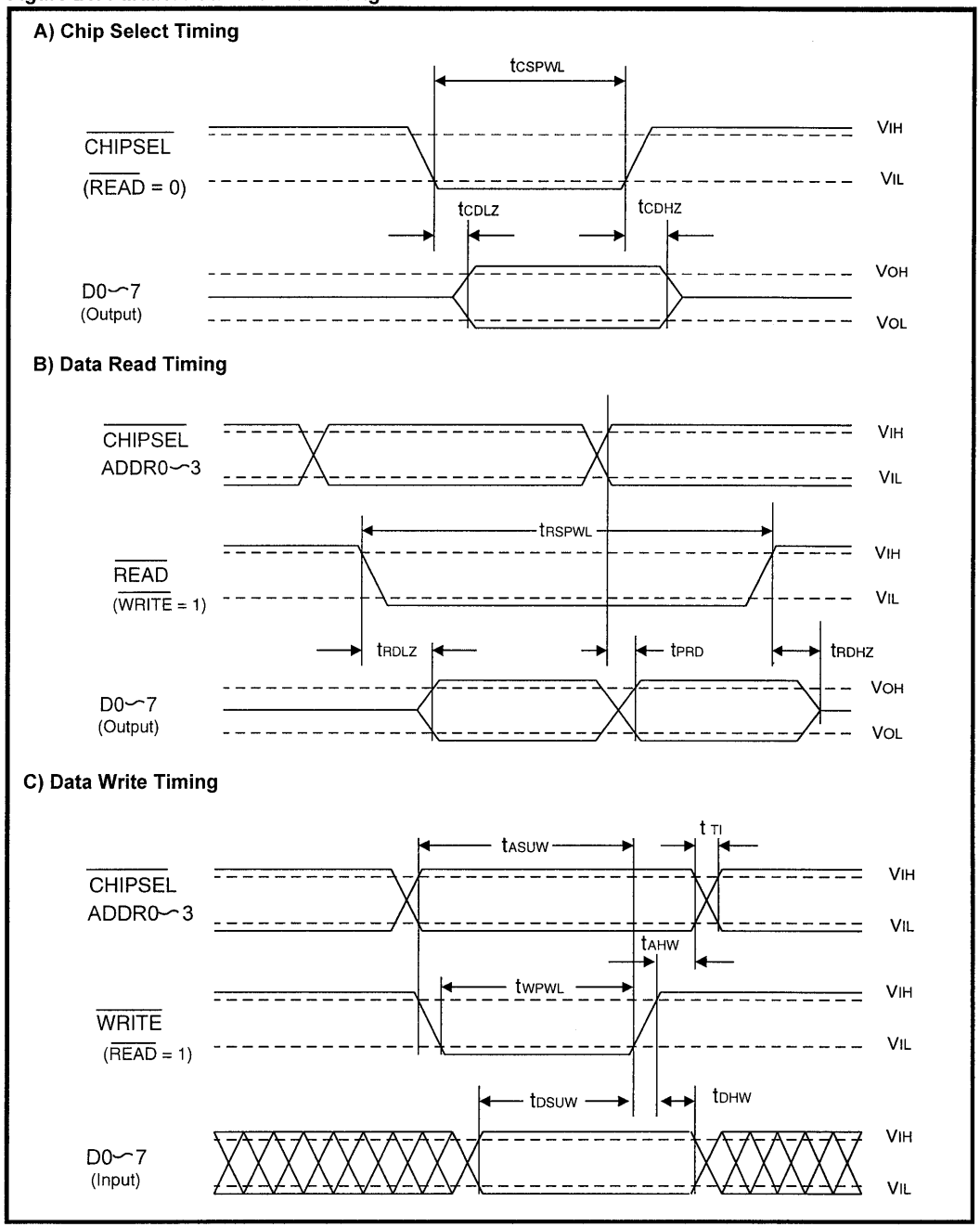


Figure 21: Parallel Data Channel Timing



NOTES

SK70704/SK70707 or SK70708

1168 kbps HDSL Data Pump Chip Set

General Description

The HDSL Data Pump is a chip set consisting of the following two devices:

- SK70704 Analog Core Chip (ACC)
- SK70707 (68-pin PLCC) or SK70708 (44-pin PLCC) HDSL Digital Transceiver (HDX)

The HDSL Data Pump is a 2-wire transceiver which provides echo-cancelling and 2B1Q line coding. It incorporates transmit pulse shaping, filtering, line drivers, receive equalization, timing and data recovery to provide 1168 kbps, clear-channel, "data pipe" transmission. The Data Pump provides Near-End Cross-Talk (NEXT) performance in excess of that required over all ETSI test loops. Typical transmission range on 0.4 mm cable exceeds 3.6 km in a noise-free environment or 2.8 km with a 0 dB margin over 10 $\mu V/\sqrt{Hz}$ ETSI noise.

The Data Pump meets the requirements of ETSI ETR-152. It provides one end of a single-channel HDSL transmission system from the twisted pair interface back to the Data Pump/HDSL data interface. The Data Pump can be used at either the NTU or the LTU end of the interface.

Applications

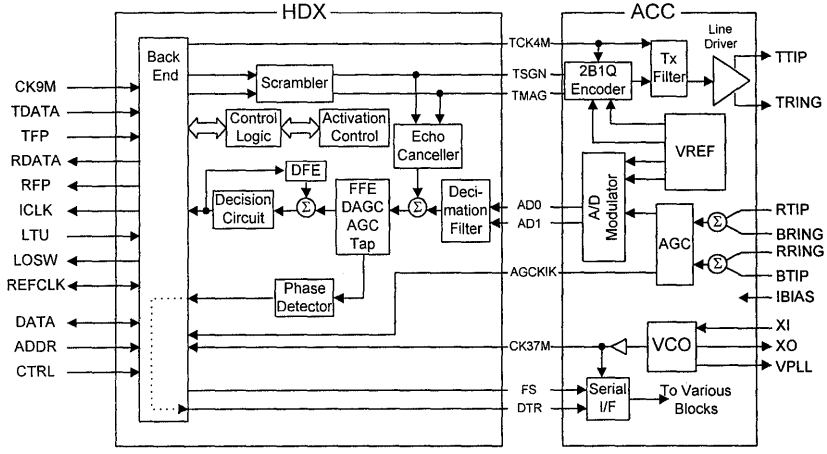
- E1 (2-pair) and fractional E1 transport
- N-channel digital pair-gain
- Wireless base station to switch interface
- Campus and private networking
- High-Speed digital modems

Features

- Fully integrated, 2-chip set for interfacing to 2-wire HDSL lines at 1168 kbps
- Single +5 V supply
- Integrated line drivers, filters and hybrid circuits result in greatly reduced external logic and simplified support circuitry requirements
- Simple line interface circuitry, via transformer coupling, to twisted pair line
- Internal ACC voltage reference
- Integrated VCXO circuitry
- Converts serial binary data to scrambled 2B1Q encoded data
- Self-contained activation/start-up state machine for simplified single loop designs
- Programmable for either line termination (LTU) or network termination (NTU) applications
- Compliant with ETSI ETR-152 (1995)
- Design allows for operation in either Software Control or stand alone Hardware Control mode
- Typical power consumption less than 1.2 W allowing remote power feeding for repeater and NTU equipment
- Input or Output Reference Clock of 18.688 MHz
- Digital representation of receive signal level and noise margin values available for SNR controlled activation

7

HDSL Data Pump Block Diagram



PIN ASSIGNMENTS AND SIGNAL DESCRIPTION

The ACC is packaged in a 28-pin PLCC. Figure 1 shows the ACC pin locations. Table 2 lists signal descriptions for each pin, except pins 18 and 19 which are not connected.

The HDX is available in two packages: 68-pin PLCC (SK70707) and 44-pin PLCC (SK70708). Figure 1 shows the HDX pin assignments. Table 3 lists signal descriptions for each pin, corresponding to the specific package.

Figure 1: SK70704 ACC Pin Locations

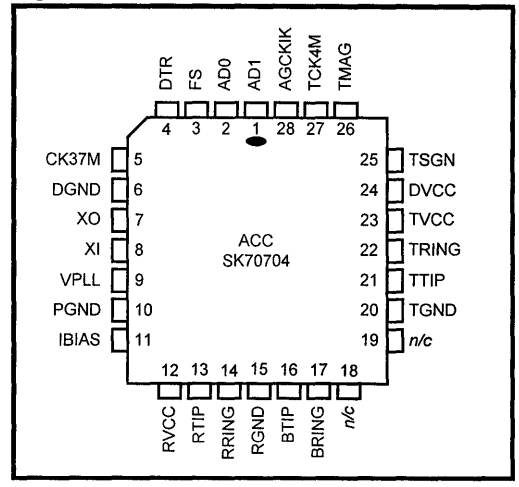
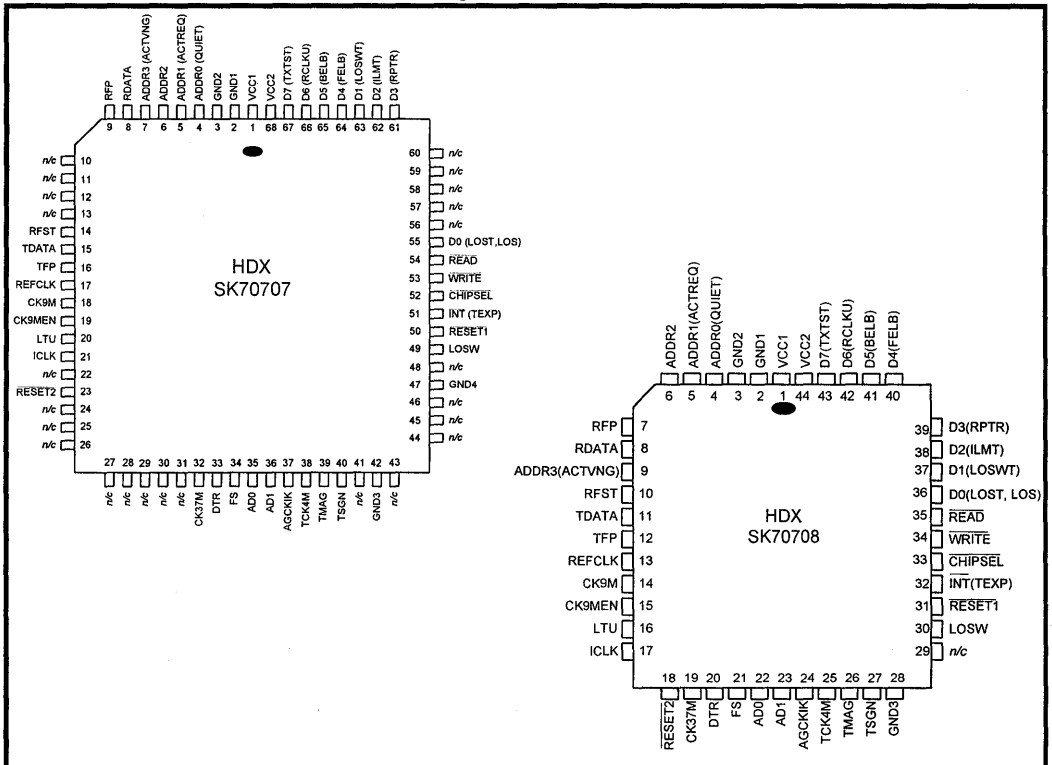


Table 1: SK70707/SK70708 HDX Pin Assignments



NOTE: Pin Functions in Hardware Control Mode are shown in parentheses.

Table 2: SK70704 ACC Pin Assignments/Signal Descriptions

Group	Pin #	Symbol	I/O	Description
Line	13	RTIP	I	**Receive Tip and Ring.** Connected these input pins to the line transformer per network requirements.
	14	RRING	I	
	16	BTIP	I	**Bias Tip and Ring.** Inputs provide a bias setting for the receiver. Provide balanced network inputs.
	17	BRING	I	
	21	TTIP	O	**Transmit Tip and Ring.** Line driver outputs.
	22	TRING	O	
PLL	7	XO	O	**Crystal Oscillator.** Connect a 37.376 MHz crystal across these two pins.
	8	XI	I	
	9	VPLL	O	**PLL Voltage Control.** Supplies control voltage to the VCXO.
Power	10	PGND	I	**PLL Ground.** 0 V.
	12	RVCC	I	**Power supply.** + 5 V (± 5%).
	23	TVCC	I	**Power supply.** + 5V (± 5%).
	24	DVCC	I	**Digital Power Supply.** +5 V (± 5%).
	6	DGND	I	**DVCC Ground.** 0V.
	15	RGND	I	**RVCC Ground.** 0V.
	20	TGND	I	**TVCC Ground.** 0V.
Clock and Control	3	FS	I	**584 kHz clock.** Input from HDX FS.
	4	DTR	I	**Serial control data.** Input from the HDX at 18.688 Mbps.
	5	CK37M	O	**37.376 MHz HDSL Reference Clock.** Used as the receive timing reference for the HDX. Tie to HDX CK37M.
	27	TCK4M	I	**4.672 MHz Clock.** Input from HDX TCK4M.
Data Input and Output	28	AGCKIK	O	**AGC adjust signal.** Output to HDX AGCKIK.
	1	AD1	O	**A-to-D converter data line 1.** Connect to HDX AD1.
	2	AD0	O	**A-to-D converter data line 0.** Connect to HDX AD0.
	25	TSGN	I	**Transmit quat sign.** Input from HDX.
	26	TMAG	I	**Transmit quat magnitude.** Input from HDX.
Analog Input	11	IBIAS	I	**Input BIAS.** Provides input bias current.

Table 3: SK70707/SK70708 HDX Pin Assignments/Signal Descriptions

Group	707 Pin #	708 Pin #	Symbol	I/O	Description
User Port	14	10	RFST	O	**Receive Frame and Stuff Bit Indicator.** Goes High for 18 consecutive ICLK periods to indicate four stuffing bits (b7007 - 7010) and 14 frame bits (b1-14) on RDATA.
	17	13	REFCLK	I[1] O	**18.688 MHz HDSL Reference Clock.** In LTU Mode, this clock generates transmit and receive timing and must have ±32 ppm accuracy. In NTU Mode, this output is derived by dividing CK37M by two.
	20	16	LTU	I	**Operation Mode Select.** When LTU is High, the Data Pump operates in LTU mode; when LTU is Low, the Data Pump operates in NTU mode. Tied to internal pull-up device.
	21	17	ICLK	O	**Bit Rate Clock.** Nominally 1168 kHz, REFCLK is the source of ICLK in LTU Mode. CK37M is the source of ICLK in NTU Mode.
	49	30	LOSW	O	**Loss of Sync Word Indicator.** Normally Low in Active States, goes High to indicate receipt of six consecutive mismatched frame synch words. LOSW is logic High in all states except Active States.
	8	8	RDATA	O	**Receive HDSL Data Stream.** Output data to HDSL framer at 1168 kbps: HDSL payload of Loop 1 or Loop 2 bytes plus the Z-bits, **eoc, crc, losd, febe, ps, bpv, hrp, indc/indr** and **uib** bits, Sync bits for frame positions b1-14, Stuff bits for frame positions b7007 - 7010. RDATA bits are forced high in all states except the Active State.
	9	7	RFP	O	**Receive Frame Pulse.** Low for one ICLK cycle during the last bit of the current HDSL receive frame on RDATA, either b7006 or b7010. Period is within one baud time of 6 ms.[2] RFP is valid when LOSW transitions Low.
	15	11	TDATA	I[1]	**Transmit HDSL Data Stream.** Input data from HDSL framer at 1168 kbps: HDSL payload of Loop 1 or Loop 2 bytes plus the Z-bits, **eoc, crc, losd, febe, ps, bpv, hrp, indc/indr** and **uib** bits, Sync bits for frame positions b1-14, Stuff dummy bits; may be 1s or 0s. Tied to internal pull-up device. When ACTIVE, the Data Pump is transparent and the HDSL framer must generate the appropriate bits on TDATA as shown in Table 6.

1. This input is a Schmidt Triggered circuit and includes an internal pull-up device.
2. The period is 6 ms $\pm^{1}/_{584}$ ms.
3. This input is a Schmidt Triggered circuit and includes an internal pull-down device.

Table 3: SK70707/SK70708 HDX Pin Assignments/Signal Descriptions – continued

Group	707 Pin #	708 Pin #	Symbol	I/O	Description
User Port	16	12	TFP	I[1]	**Transmit Frame Pulse.** Must be Low for one ICLK cycle during the last bit of the current HDSL frame on TDATA, either b7006 or b7010. Period is within one baud time of 6 ms.[2] If TFP is pulled Low and is Low again three ICLK cycles later, RDATA, RFP, RFST, ICLK, CK9MEN and LOSW go to tri-state. Tied to internal pull-up device.
Hardware Interface *(Hardware Control Mode)*	4	4	QUIET	I[3]	**Quiet Mode Enable.** Pull High to force HDX into Deactivated State. Any later transition to Low will not return HDX to Active State. See ACTREQ.
	5	5	ACTREQ	I[3]	**Activation Request (LTU mode) or no function (NTU mode).** Tie this pin Low in NTU mode. If QUIET is Low, a rising edge on this pin initiates activation, but the signal is ignored after activation. See QUIET.
	6	6	*reserved*	–	*Pull Low in LTU mode, leave open in NTU mode.*
	7	9	ACTVNG	O	**Activating State Indication.** High when the HDX is in the Activating State.
	23	18	$\overline{\text{RESET2}}$	I[1]	**Reset Pulse.** Pull Low on power up to initialize circuits and stop all clocks.
	50	31	$\overline{\text{RESET1}}$	I[1]	**Reset Pulse.** Pull Low to initialize internal circuits.
	51	32	TEXP	O	**Timer Expiry.** Goes High to indicate 30 second timer expiration in all states.
	52	33	$\overline{\text{CHIPSEL}}$	I[3]	**Chip Select** — *Assert these three pins Low to activate Hardware Control Mode. When any of them goes High, the HDX reverts immediately to Software Control Mode.*
	53	34	$\overline{\text{WRITE}}$	I[3]	**Write Pulse**
	54	35	$\overline{\text{READ}}$	I[3]	**Read Pulse**
	55	36	LOST (LTU)	O	**Loss of Signal Timer Expiration.** In LTU mode, LOST goes High when the Data Pump enters the Inactive State. The transition from the Deactivated to the Inactive State occurs 1 second after the end of transmission by the NTU when deactivation began from either the Active-1 or Active-2 State. When the Data Pump transitions from the Activating State to the Deactivated State it may immediately enter the Inactive State without waiting for NTU transmission to cease. (See Figure 5.)
			LOS (NTU)	O	**Loss of Signal Energy Indicator.** In NTU mode LOS goes High to indicate loss of signal energy on entering the Inactive State. (See Figure 7.)

1. This input is a Schmidt Triggered circuit and includes an internal pull-up device.
2. The period is 6 ms $\pm^{1}/_{584}$ ms.
3. This input is a Schmidt Triggered circuit and includes an internal pull-down device.

Table 3: SK70707/SK70708 HDX Pin Assignments/Signal Descriptions – continued

Group	707 Pin #	708 Pin #	Symbol	I/O	Description
Hardware Interface	63	37	LOSWT	O	**Loss of Sync Word Timer.** LOSWT goes High when LOSW is sustained for longer than 2 sec.
(Hardware Control Mode) -cont'd	62	38	ILMT	I^1	**Insertion Loss Measurement Test.** Set High to transmit a framed & scrambled, "all 1s", 2B1Q pulse sequence. Pulse sequence will have a valid sync word. In the NTU configuration, when the ILMT mode is selected, the Data Pump may begin activation.
	61	39	RPTR	I^1	**Repeater Mode Enable.** When in LTU mode, ICLK output phase is aligned to the TFP input pulse width. Ignored in NTU mode.
	64	40	FELB	I^1	**Front-End Loopback (LTU only).** In Inactive State, set High to cause the ACC to loopback. The returned signal activates the HDX which receives its own transmitted data. The system ignores incoming data from NTU during loopback irrespective of status.
	65	41	BELB	I^1	**Back-End Loopback.** In Active State a High forces an internal, transparent loopback with RDATA connected to TDATA and RFP connected to TFP.
	66	42	RCLKU	O	**Receive Baud Rate (584 kHz) Clock.** Aligned with ICLK in NTU mode, phase synchronous with receive pulse stream, However, during Activating State, the clocks may not be aligned. In the LTU mode RCLKU has a constant, arbitrary, phase relationship with ICLK in Active State.
	67	43	TXTST	I^1	**Transmit Test.** Set high to enable isolated transmit pulse generation. The time between pulses is approximately 6 ms. TDATA controls the sign and TFP controls the magnitude of the transmitted quat pulses according to the 2B1Q encoding rules. In the NTU configuration, when the TXTST mode is selected, the Data Pump may begin activation.
Processor Interface *(Software Control Mode)*	55	36	D0	I^1/O	**Data bit 0.** Eight-bit, parallel data bus.
	63	37	D1	I^1/O	**Data bit 1**
	62	38	D2	I^1/O	**Data bit 2**
	61	39	D3	I^1/O	**Data bit 3**
	64	40	D4	I^1/O	**Data bit 4**
	65	41	D5	I^1/O	**Data bit 5**
	66	42	D6	I^1/O	**Data bit 6**
	67	43	D7	I^1/O	**Data bit 7**
	4	4	ADDR0	I^3	**Address bit 0.** Four-bit address, selects read or write register.
	5	5	ADDR1	I^3	**Address bit 1**
	6	6	ADDR2	I^3	**Address bit 2**
	7	9	ADDR3	I^3	**Address bit 3**
	23	18	$\overline{\text{RESET2}}$	I^1	**Reset Pulse.** Pull Low on power up to initialize circuits and stop all clocks.

1. This input is a Schmidt Triggered circuit and includes an internal pull-up device.
2. The period is 6 ms $\pm^1/_{584}$ ms.
3. This input is a Schmidt Triggered circuit and includes an internal pull-down device.

Table 3: SK70707/SK70708 HDX Pin Assignments/Signal Descriptions – continued

Group	707 Pin #	708 Pin #	Symbol	I/O	Description
Processor Interface *(Software Control Mode)*	50	31	$\overline{\text{RESETI}}$	I[1]	**Reset Pulse.** Pull Low to initialize internal circuits. ICLK continues.
	51	32	$\overline{\text{INT}}$	O	**Interrupt Output.** Open drain output. Requires an external 10 kΩ pull up resistor. Goes Low on interrupt.
	52	33	$\overline{\text{CHIPSEL}}$	I[3]	**Chip Select.** Pull Low to read or write to registers.
	53	34	$\overline{\text{WRITE}}$	I[3]	**Write Pulse.** Pull Low to write to registers.
	54	35	$\overline{\text{READ}}$	I[3]	**Read Pulse.** Pull Low to read from registers.
Clock and Control	18	14	CK9M	I[3]	**9.344 or 18.688 MHz Reference Clock.** Mandatory in NTU mode. Tie High or Low in LTU Mode. Clock input requires ± 32 ppm accuracy.
	19	15	CK9MEN	O	**CK9M Enable.** Active High enable for CK9M clock. In NTU mode, this pin goes Low to indicate the PLL is tracking the input signal from the LTU. Not used in LTU.
	32	19	CK37M	I	**Receive Timing Clock (37.376 MHz).** Tie to CK37M on ACC.
	33	20	DTR	O	**Serial Control Data Link.** Transfers data at 18.688 Mbps. Tie to DTR on ACC.
	34	21	FS	O	**584 kHz Clock.** Derived from CK37M. Tie to FS on ACC.
	35	22	AD0	I	**Analog to Digital Converter input pin.** Tie to AD0 on ACC
	36	23	AD1	I	**Analog to Digital Converter input pin.** Tie to AD1 on ACC
	37	24	AGCKIK	I	**AGC Adjust.** Controls analog gain circuit. Tie to AGCKIK on ACC.
	38	25	TCK4M	O	**Transmit Clock.** Tie to TCK4M on ACC.
	39	26	TMAG	O	**Transmit Magnitude Bit.** Tie to TMAG on ACC.
	40	27	TSGN	O	**Transmit Sign Bit.** Tie to TSGN on ACC.

1. This input is a Schmidt Triggered circuit and includes an internal pull-up device.
2. The period is 6 ms $\pm^{1}/_{584}$ ms.
3. This input is a Schmidt Triggered circuit and includes an internal pull-down device.

Table 3: SK70707/SK70708 HDX Pin Assignments/Signal Descriptions – continued

Group	707 Pin #	708 Pin #	Symbol	I/O	Description
Power	1	1	VCC1	I	**Logic supply input.** (Refer to Table 28)
	68	44	VCC2	I	**I/O supply input.**
	2	2	GND1	I	**Ground.**
	3	3	GND2	I	**Ground.**
	42	28	GND3	I	**Ground.**
	47	–	GND4	I	**Ground.**
Misc	10 11 12 13 22 24 25 26 27 28 29 30 31 41 43 44 45 46 48 56 57 58 59 60	29	–	–	*No internal connection.*

1. This input is a Schmidt Triggered circuit and includes an internal pull-up device.
2. The period is 6 ms $\pm^{1}/_{584}$ ms.
3. This input is a Schmidt Triggered circuit and includes an internal pull-down device.

FUNCTIONAL DESCRIPTION

The HDSL Data Pump is a fully-integrated, two-chip solution (see front page block diagram) which includes an SK70704 Analog Core Chip (ACC) and an SK70707/ SK70708 HDSL Digital Transceiver (HDX).

Transmit

The transmit data stream is supplied to the HDX at the TDATA input in a binary fashion. The HDX scrambles and 2B1Q encodes the data and adds the sync word and stuff quats based on the TFP frame pulse position. The injected stuff quats in a frame are equal to the last scrambled data symbol in that frame. The 2B1Q encoded transmit quat data stream (TSGN/TMAG) is then passed to the ACC which filters and drives it onto the line.

Receive

The composite waveform of the receive signal plus transhybrid echo is filtered and converted to digital words at a rate of 584 k-words/second in the ACC. The ACC passes the digitized receive quat stream (AD0 and AD1) to the HDX. The HDX performs digital filtering, linear echo cancellation, frame recovery and descrambling. The HDX uses the transmit quat stream to generate the echo estimates and estimate error values. Using this error and the delayed transmit quat stream, the echo canceller coefficients are updated. The recovered, decoded and descrambled data is then output to the framer-mux from the HDX RDATA pin.

Control

The Data Pump offers two control modes - Hardware Mode and Software Mode. In Hardware mode the HDX receives control inputs via individually designated pins. In Software mode the HDX control data is supplied via an 8-bit parallel port. In either mode, the HDX and the ACC communicate via a unidirectional serial port (DTR).

ACC and HDX Overview

The following paragraphs describe the chip set components individually with reference to internal functions and the interfaces between Data Pump components.

Analog Core Chip (ACC)

The ACC incorporates the following analog functions:

- the transmit line driver
- transmit and receive filters
- Phase-Locked Loop (PLL), including VCXO
- hybrid circuitry analog-to-digital converter.

The ACC provides the complete analog front end for the HDSL Data Pump. It performs transmit pulse shaping, line driving, receive A/D, and the VCO portion of the receiver PLL function. Transmit and receive controls are implemented through the serial port. The ACC line interface uses a single twisted pair line for both transmit and receive. Table 1 lists the ACC pin descriptions. Refer to Test Specifications section for ACC electrical and timing specifications.

ACC Transmitter

The ACC performs the pulse shaping and driving functions. The ACC transmitter generates a 4-level output of 1/(8*f(TCK4M)) defined by TMAG and TSGN. Table 4 lists 2B1Q pulse coding parameters. Refer to Test Specifications for frequency and voltage templates.

ACC Receiver

The ACC receiver is a sophisticated sigma-delta converter. It sums the differential signal at RTIP/RRING minus the signal at BTIP/BRING. The first A/D signal comes out of AD0 at a bit stream rate of 18.688 MHz. The second stage of the A/D samples the noise of the first and generates the AD1 bit stream at 18.688 MHz.

Receiver gain is controlled by the HDX via the AGC2-0 bits in the DTR serial control stream. The AGCKIK output from the ACC is normally Low. It goes High when the signal level in the sigma-delta A/D is approaching its clipping level, signaling the HDX to lower the gain.

The VCO is part of a phase-locked loop (PLL) locked to the receive data baud rate using an external phase detector. The VCO frequency is varied by pulling an external crystal with external varactor diodes that are controlled by the VPLL output. The VPLL output is, in turn, controlled by the serial port VCO and PLL bits.

HDSL Digital Transceiver (HDX)

The HDX incorporates the following digital functions:

- bit-rate transmit and receive signal-processing
- adaptive echo-cancelling (EC)
- adaptive decision feedback-equalization (DFE) using the receive quat stream and the internal error signal
- fixed and adaptive digital-filtering functions
- activation/start-up control and the microprocessor interface to the HDSL framer.

The HDX also provides the Data Pump Back-End interface for the customer defined/developed HDSL framer via serial data channels and clock signals. A simple, parallel 8-bit microprocessor interface on the HDX allows high-speed access to control, status and filter coefficient words. Table 3 lists the HDX pin descriptions. Refer to Test Specifications section for HDX electrical and timing specifications.

The microprocessor interface on the HDX provides bit flags for signal presence, synchronization, activation completion, and loss of synchronization for a time greater than two seconds. Single-byte words representing receive signal level and the noise margin of the transceiver are also available on the microprocessor interface. One control byte allows the user to start the Data Pump activation sequence. The HDX controls the complete activation/start-up sequence, allowing flexible, single-loop, fractional applications.

Table 4: ACC Transmit Control

TSGN	TMAG	Output Symbol (quat)
1	0	+3
1	1	+1
0	1	-1
0	0	-3

HDX/ACC Interface

The ACC provides the 37.376 MHz master clock, CK37M, to the HDX. The serial control stream framing signal FS is sampled inside the ACC with the CK37M rising edge. The serial control stream, DTR, is sampled inside the ACC by the rising edge of an internally-generated clock at f(CK37M)/2. This ACC internal clock has the same phase relationship with a similar clock inside the HDX, as established by the FS signal. In the HDX, the half-rate clock CK37M/2 and FS transition on the rising edge of CK37M, and DTR transitions come on the falling edge of CK37M/2. The output REFCLK in NTU Mode equals CK37M/2.

The A/D converter outputs, AD0 and AD1, are clocked out of the ACC with CK37M, having transitions coincidental with the rising edge of CK37M/2. The HDX samples AD0 and AD1 with the falling edge of its internal CK37M/2.

Transmit data, represented by TSGN and TMAG, is clocked from the HDX using the falling edge of TCK4M, the 4.672 MHz (f(REFCLK)/4) transmit time base clock. The ACC uses the rising edge of TCK4M to sample TSGN and TMAG. TSGN and TMAG change state at the baud rate, or every 8 cycles of TCK4M. Figure 2 shows relative timing for the HDX/ACC interface.

HDX/ACC Serial Port

The HDX continually writes to the ACC serial port. This serial stream consists of two 16-bit words as shown in Table 5. The data flows from the HDX to the ACC at a rate of f(CK37M)/2. Refer to the Test Specifications section for serial port timing relationships and electrical parameters.

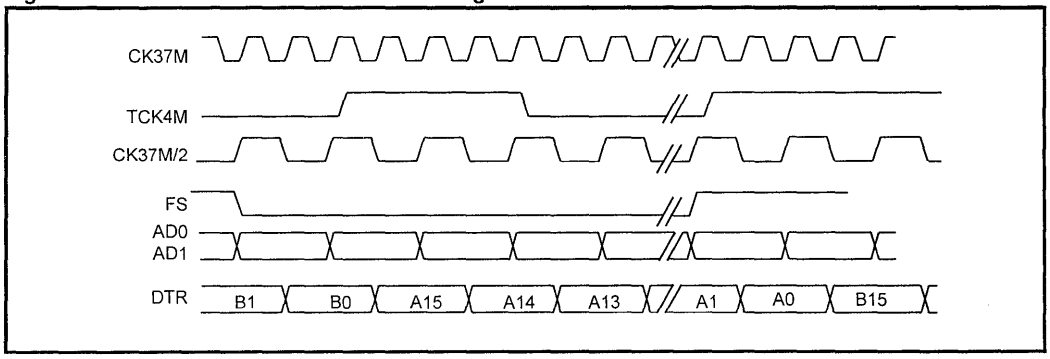
Line Interface

The Data Pump line interface consists of three differential pairs. The transmit outputs TTIP and TRING, receive inputs RTIP and RRING, and the balance inputs BTIP and BRING, all connect through a common transformer to a single twisted-pair line (see Figures 11 and 14). The transmit outputs require resistors in series with the transformer. A passive prefilter is required for the receive inputs. The balance inputs feed the transmit signals back to the Data Pump providing passive echo cancellation. Protection circuitry should be inserted between all Data Pump line interface pins and the transformer. Refer to the Applications section for typical schematics.

Table 5: HDX/ACC Serial Port Word Bit Definitions (See Figure 2)

Bit	Word A (on DTR)	Word B (on DTR)
15	INIT	COR4
14	*n/a*	COR3
13	*n/a*	COR2
12	TXOFF	COR1
11	TXDIS	COR0
10	TXTST	VCO2
9	AGC2	VCO1
8	AGC1	VCO0
7	AGC0	PLL7
6	FELB	PLL6
5	*n/a*	PLL5
4	PTR4	PLL4
3	PTR3	PLL3
2	PTR2	PLL2
1	PTR1	PLL1
0	PTR0	PLL0

Figure 2: HDX/ACC Interface – Relative Timing



HDSL Data Interface

The HDSL data interface includes the transmit and receive binary data streams, transmit and receive frame pulses, the 1168 kHz clock (ICLK) and the receive frame and stuff quat indicator (RFST). Figure 3 shows relative timing for the framer interface. Refer to Test Specifications section for details on the Data Pump/framer interface. Figure 6 shows a complete HDSL system with both the remote NTU and central office LTU HDSL framer interfaces illustrated. Table 6 shows the TDATA requirements for the framer interface through the activation sequence. Once the ACTIVE Low-to-High transition occurs, the Data Pump becomes transparent. Therefore, the HDSL framer must supply appropriate data to TDATA. Table 6 summarizes this requirement.

The HDSL framer interface is subject to the following rules:

1. When frame sync is not present (LOSW is High), all RDATA bits are set to 1.
2. If frame sync is lost on both Data Pump-R1 and Data Pump-R2, both units will fall back on the local reference frequency with ±32 ppm tolerance, and stuff bits will be injected in their RDATA streams on every other frame.

Table 6: HDSL Framer TDATA Requirements

Activation Process		TDATA	
Framer	**Data Pump**	**Overhead**	**Data**
Idle	Activating	*don't care*	*don't care*
Idle	Active 1	live	all 1s
Active-R	Active 1	live	all 1s
Active-T	Active 1	live	live
Link Active	Active 1	live	live
Link Active	Active 2	live	live

3. If frame sync is lost on either Data Pump-R1 or Data Pump-R2, that unit can be made to fall back on the REFCLK from the Data Pump-R which is still in frame sync, and stuff bits will be injected in the RDATA stream on every other frame of the out-of-frame Data Pump-R.
4. If frame sync is lost on either Data Pump-C1 or Data Pump-C2, both unit's receiver will fall back on the reference clock with ±32 ppm or ±5 ppm tolerance, and inject stuff bits in the RDATA stream on every other frame.
5. If either E1-R or E1-C loses sync or signal, it is assumed that the corresponding T1 receiver will fall back on a local reference with ±32 ppm tolerance, and that transmit bit-stuffing control will still be applied through the TFP signal from the HDSL framer.
6. The HDSL framer should provide TFP signal with a period of 6 ms $\pm^{1}/_{584}$ ms prior to an activation request for the LTU Data Pump(s). The framer should provide a valid TFP after power-up, before or immediately after LOS goes Low for the NTU Data Pump(s).

   If the TFP signal from the HDSL framer is inactive (always High or unconnected), the Data Pump will inject stuff bits in the TDATA stream in every other frame, although the Data Pump will not be synchronized to the HDSL framer. When a new TFP is provided, the Data Pump will immediately reset the transmit frame alignment, typically causing loss of alignment at the other end.
7. A simultaneous $\overline{\text{RESET2}}$ to all LTU Data Pumps which use a common REFCLK eliminates phase shift between the ICLK outputs which may exist after power-up.
   The ICLK outputs of all NTU Data Pumps may have an arbitrary phase difference even using a common CK9M reference.

Figure 3: HDX/ACC Framer Interface – Relative Timing

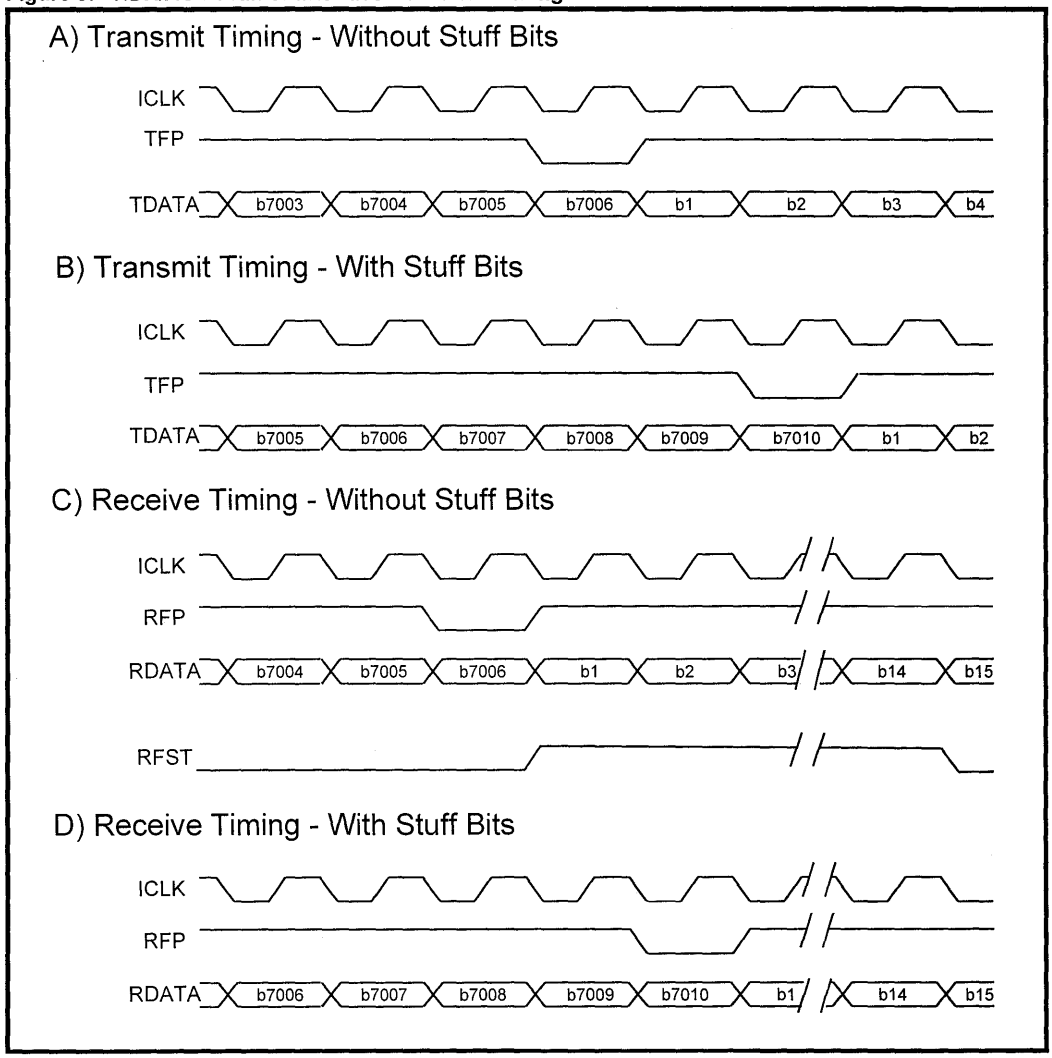
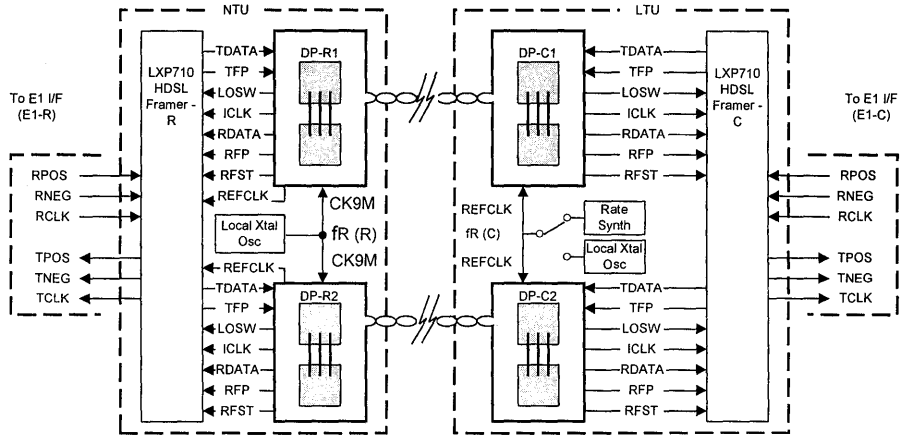


Figure 4: Model for HDSL Data Pump and HDSL Framer Applications



Frequency Relationships. 1.

1. f_{TCLK} (E1-C) = (E1-R); tolerance = ±32 ppm, even with loss of signal on E1-R.
2. f_{TCLK} (E1-R) = (E1-C); tolerance = ±32 ppm, even with loss of signal on E1-C.
3. f_{ICLK} (C) = $f_{R(C)}/_{16}$; tolerance = ±32 ppm if sourced by local crystal oscillator (stratum 4), = ±5 ppm if sourced by office clock (stratum 3).
4. f_{ICLK} (R) = f_{ICLK} (C) if loop is activated with receive frame sync acquired, = $f_{R(R)}/_{16}$ if receive sync is lost; tolerance = ±32 ppm (f_{R}(R) = 18.688 MHz). = $f_{R(R)}/_{8}$ if f_{R}(R) = 9.344 MHz.

Microprocessor Interface (HDX)

Three primary control pins, $\overline{\text{CHIPSEL}}$ (Chip Select), $\overline{\text{READ}}$ and $\overline{\text{WRITE}}$, execute the Software Mode which also uses an interrupt output pin to report status changes. Four additional pins are used for the parallel bus addressing and eight pins for data I/O. Refer to Test Specifications for µprocessor interface timing in Software Mode. The following control pins are used during register access.

Control Pins

Chip Select: The Chip Select ($\overline{\text{CHIPSEL}}$) pin requires an active Low signal to enable Data Pump read or write transfers over the data bus. To enable Hardware Mode hold this pin Low, along with $\overline{\text{READ}}$ and $\overline{\text{WRITE}}$.

Data Read: The Data Read pin ($\overline{\text{READ}}$) requires an active Low pulse to enable a read transfer on the data bus. When $\overline{\text{READ}}$ is pulled Low, the Data Pump data bus lines go from tristate to active and output the data from the register addressed by ADDR0-ADDR3. To avoid reading data during register updates, reads should be synchronized to the falling edge of FS. Alternatively, each read should be repeated until the same data is read twice within one baud time.

Data Write: The Data Write pin ($\overline{\text{WRITE}}$) requires an active Low pulse to enable a write transfer on the data bus. Data transfer is triggered by the rising edge of the $\overline{\text{WRITE}}$ pulse. To ensure data is written to the register addressed by ADDR0-ADDR3, valid data must be present on the HDX data bus lines before $\overline{\text{WRITE}}$ goes High.

Interrupt: The Interrupt pin ($\overline{\text{INT}}$) is an open drain output requiring an external pull-up resistor. The $\overline{\text{INT}}$ output is pulled active Low when an internal interrupt condition occurs. $\overline{\text{INT}}$ is latched and held until Main Status Register RD0 is read. An internal interruption results from a Low-to-High transition in any of four status indicators: ACTIVE, LOSW, LOSWT or TEXP. Any transition on LOS will also generate an interrupt. If an interrupt mask bit in register WR2 is set, any transition of the corresponding status bit will not trigger the $\overline{\text{INT}}$ output.

Register Access

Write: To write to an HDX register, proceed as follows:

1. Drive $\overline{\text{CHIPSEL}}$ Low.
2. Drive an address (0000, 0010, or 0011) onto ADDR0-ADDR3.
3. Observe address setup time.
4. Set 8-bit input data word on D0-D7.
5. Pull $\overline{\text{WRITE}}$ Low, observing minimum pulse width.
6. Pull $\overline{\text{WRITE}}$ High, observing hold time for data and address lines.

Read: Procedures for reading the HDX registers vary according to which register is being read. Accessing registers RD0, RD1, RD2, RD5 and RD6 is relatively simple. Reading registers RD3 and RD4 is more complex. *Unless parallel port reads are synchronized with the falling edge of FS, all read operations should be repeated until the same data is read twice within one baud time.*

To read register RD0, RD1, RD2, RD5 or RD6 proceed as follows:

1. Drive $\overline{\text{CHIPSEL}}$ Low.
2. Drive the desired address onto ADDR0-ADDR3.
3. Pull $\overline{\text{READ}}$ Low, observing minimum pulse width.
4. Pull $\overline{\text{READ}}$ High to complete the read cycle.

Registers RD3 and RD4 hold the coefficient values from the DFE, EC, FFE and AGC as shown in Table 10. Register RD3 holds the lower byte value and register RD4 holds the upper byte value. To reconstruct the complete 16-bit word, concatenate the least significant and most significant bytes.

To read registers RD3 and RD4 proceed as follows:

1. Select the desired coefficient by writing the appropriate code from Table 10 to register WR3.
2. Enable the Coefficient Read Register by writing a 1 to bit b0 (CRD1) in register WR2.
3. Perform standard register read procedure listed in steps 1 through 6 above to read the lower byte from RD3 and the upper byte from RD4.
4. Concatenate the RD3 and RD4 to obtain the complete 16-bit word.

Registers

Three write registers and seven read registers are available to the user. Table 7 lists these registers and the following paragraphs describe them in more detail.

Some of the registers contain *reserved* bits. Software must deal correctly with *reserved* fields. For reads, software must use appropriate masks to extract the defined bits and not rely on *reserved* bits being any particular value. In some cases, software must program *reserved* bit positions to a particular value. This value is defined in the individual bit descriptions.

After asserting the $\overline{\text{RESET1}}$ and $\overline{\text{RESET2}}$ signals, the Data Pump initializes its registers to the **default** value.

Table 7: Register Summary

ADDR	Write Registers			Read Registers		
A3-A0	WR#	Name	Table	RD#	Name	Table
0000	WR0	Main Control	8	RD0	Main Status	11
0001		*reserved*		RD1	Receiver Gain Word	12
0010	WR2	Interrupt Mask	9	RD2	Noise Margin	13
0011	WR3	Read Coefficient Select	10	RD3	Coefficient Read Register (lower byte)	14
0100		*reserved*		RD4	Coefficient Read Register (upper byte)	14
0101		*reserved*		RD5	Activation Status	15
0110		*reserved*		RD6	Receiver AGC and FFE Step Gain	16
0111-1001		*reserved*			*reserved*	

WR0—Main Control Register

Address: A3-0 = 0000
Default: 00h
Attributes: Write Only

Control Register bits serve the same purpose in Software Mode as the like-named individual pins in Hardware Mode. Table 8 lists bit assignments for the WR0 register.

Table 8: Main Control Register WR0

Bit	Description
b7	**Transmit Test Pattern Enable (TXTST).** Set TXTST to 1 to enable isolated transmit pulse generation. The time between pulses is 6 ms. TDATA controls the sign and TFP controls the magnitude of the transmitted symbols according to the 2B1Q encoding rules. In the NTU configuration when the TXTST mode is selected, the Data Pump may begin activation.
b6	**Back-End Loop Back (BELB).** In the Active State, set BELB to 1 to enable an internal, transparent loopback of the HDX RDATA to TDATA and RFP to TFP.
b5	**Front End Loop Back (FELB).** In the LTU mode with the Data Pump in the Inactive State, set FELB to 1 to enable an ACC front-end loopback. The Data Pump will begin activation and transmission on the line, but will ignore any signal from the NTU instead synchronizing to its own transmit signal.
b4	**Repeater Mode (RPTR).** The RPTR bit is set to 1 and the LTU pin is pulled High to program the Data Pump for operation on the side of the HDSL repeater driving the remote NTU. RPTR is set to 0 and the LTU pin is tied Low to program the Data Pump for operation on the side of the repeater driven by the central office LTU.
b3	***reserved.*** *This bit must be set to 0.*
b2	**Insertion Loss Measurement Test (ILMT).** Set ILMT to 1 to enable transmission of a scrambled all ones insertion loss measurement test pattern. In the NTU configuration when the ILMT mode is selected, the Data Pump may begin activation.
b1	**Quiet Mode (QUIET).** Set QUIET to 1 to force the Data Pump into the De-Activated State with the transmitter silent. Setting QUIET to 0 will not cause the Data Pump to reactivate. In the NTU mode, the Data Pump will not respond to an S0 signal from the LTU when QUIET is set to 1, but may activate after QUIET is set to 0 even if the LTU transmission has already ceased.
b0	**Activation Request (ACTREQ).** In the LTU mode when the Data Pump is in the Inactive State and Quiet is set to 0, setting the ACTREQ bit to 1 will initiate an activation sequence. Because ACTREQ is a level- rather than an edge-triggered signal, it should be reset to 0 again within approximately 25 seconds to prevent the immediate start of another activation cycle if the current activation attempt fails. If an activation attempt fails, the processor should allow the Data Pump to remain in the Inactive State where the transmitter is silent for 32 seconds before generating another activation request to allow the NTU to return to the Inactive State. It is possible to shorten this quiet period following a failed activation by implementing additional algorithms described in the section entitled "Activation State Machines."

WR2—Interrupt Mask Register

Address: A3-0 = 0010
Default: 00h
Attributes: Write Only

Table 9 shows the various interrupt masks provided in register WR2.

Table 9: Interrupt Mask Register WR2

Bit	Description
b7-b6	***Reserved.*** *Must be set to 0.*
b5	**LOSMSK.** 1=Masked. 0=Not Masked. Interrupt mask for the LOS condition
b4	**LSWTMSK.** 1=Masked. 0=Not Masked. Interrupt mask for the LOSWT condition
b3	**LSWMSK.** 1=Masked. 0=Not Masked. Interrupt mask for the LOSW condition
b2	**ACTMSK.** 1=Masked. 0=Not Masked. Interrupt mask for the TEXP condition and the ACTIVE condition
b1	***Reserved.*** *Must be set to 0.*
b0	**CRD1.** Enable coefficient read register. Used in conjunction with WR3 for reading coefficient values.

WR3—Read Coefficient Select Register

Address: A3-0 = 0011
Default: 00h
Attribute: Write Only

Table 10 lists the bit maps used to select the coefficient read from the HDX.

Table 10: Read Coefficient Select Register WR3

Hex Value	Selected Registers	Register Description
00-07	DFE1-DFE8	DFE coefficients
08-0F	EC1-EC8	Echo Cancellation
10-15	FFE1-FFE6	FFE coefficients 1-6
16-19	*reserved*	
1A	AGC Tap	AGC Tap
1B-FF	*reserved*	

RD0—Main Status Register

Address: A3-0 = 0000
Default: xxh (x=undefined)
Attribute: Read Only

Status Register bits serve the same purpose in Software Mode as the like-named individual pins in Hardware mode. Table 11 lists the bit assignments in this register

Table 11: Main Status Register RD0

Bit	Active Description
b7	**Timer Expiry (TEXP).** Set to 1 to indicate 30-second timer expiration in the Active State. • Causes interrupt on changing from 0 to 1; masked by ACTMSK = 1. • Latched event; reset on read, with persistence while in the Active State.
b6	**TIP/RING polarity reversed ($\overline{\text{INVERT}}$).** 0 = polarity reversal. Valid only in Active State.
b5	**Change Of Frame Alignment (COFA).** Indicates that re-acquisition of frame sync is in a different position with respect to the last frame position. Does not cause interrupt. Latched event; reset on read
b4	**Loss Of Signal (NTU) (LOS).** 1 = loss of line signal energy on entering Inactive State.
	Loss of Signal Timer Expiration (LTU) (LOST). 1 = loss of signal for 1 second on entering Inactive State. • Causes interrupt on transitions from 0 to 1 or 1 to 0 that are masked by LOSMSK = 1. • LOS/LOST is not a latched event.
b3	***reserved.*** *This bit should be ignored.*
b2	**Loss of Sync Word Timer Expiry (LOSWT).** Indicates two seconds of LOSW. • Causes interrupt on changing from 0 to 1; masked when LSWTMSK = 1. • Latched event; reset on read; with persistence while in the Deactivated State.
b1	**Loss of Sync Word (LOSW).** • Causes interrupt on changing from 0 to 1; masked by LSWMSK = 1. • Latched event; reset on read; with persistence while in the Pending Deactivation State.
b0	**Active State (ACTIVE).** 1 = Completion of layer 1 activation. • Causes interrupt on changing from 0 to 1; masked by ACTMSK = 1. • Latched event; reset on read with persistence if still in the Active State.

RD1—Receiver Gain Word Register

Address: A3-0 = 0001
Default: xxh (x=undefined)
Attributes: Read Only

The 8-bit word in this register is the eight most significant bits of the main FFE AGC tap, which, along with the AGC and DAGC values (RD6), represent the receiver gain required to compensate for line loss, and to normalize the receive 2B1Q pulses to a fixed threshold. Bit b7 (sign bit, always 0) is the MSB with bit b0 the LSB. The AGC tap value is determined as follows:

$$\text{AGC Tap} = \sum_{i=0}^{6} b_i * 2^{i-6}$$

Table 12: Receiver Gain Word Register

Bit	Description
b7-b0	**FFE AGC Tap Value** (eight most significant bits).

RD2—Noise Margin Register

Address: A3-0 = 0010
Default: xxh (x=undefined)
Attributes: Read Only

The noise margin of the received signal is an input to the HDSL framer's Activation State Machine. The noise margin must reach a threshold level before the HDSL framer can transition to the fully Active State. The HDX provides a calculated, logarithmic noise margin value used by the HDSL framer. This eight-bit word, stored in register RD2, is available every baud, although updated only every 64 baud. Table 22 shows the noise margin coding. To calculate the SNR, use this equation:

SNR =Noise Margin + 21.5 dB

Error propagation in the DFE and de-scrambler may introduce some fractional errors in this formula, however, the relationship between the SNR and the noise margin remains valid as long as the noise follows a Gaussian distribution.

Since the average period of the calculation is very short (64 baud = 110 µs), the recommended procedure for evaluating transmission quality is to average at least 1000 samples over a 110 ms period.

Table 13: Noise Margin Register RD2
Noise Margin Coding[1]

MSB							LSB	Noise Margin
b7	b6	b5	b4	b3	b2	b1	b0	
0	0	1	1	0	1	0	1	+26.5
0	0	1	0	1	1	1	1	+23.5
0	0	1	0	1	0	1	1	+21.5
0	0	1	0	1	0	0	1	+20.5
0	0	1	0	0	1	1	1	+19.5
0	0	1	0	0	1	0	1	+18.5
0	0	1	0	0	1	0	0	+18.0
0	0	1	0	0	0	1	0	+17.0
0	0	1	0	0	0	0	0	+16.0
0	0	0	1	1	1	1	0	+15.0
0	0	0	1	1	1	0	0	+14.0
0	0	0	1	1	0	1	0	+13.0
0	0	0	1	1	0	0	0	+12.0
0	0	0	1	0	1	1	0	+11.0
0	0	0	1	0	1	0	0	+10.0
0	0	0	1	0	0	1	0	+9.0
0	0	0	1	0	0	0	0	+8.0
0	0	0	0	1	1	1	0	+7.0
0	0	0	0	1	1	0	0	+6.0
0	0	0	0	1	0	1	0	+5.0
0	0	0	0	1	0	0	0	+4.0
0	0	0	0	0	1	1	0	+3.0
0	0	0	0	0	1	0	0	+2.0
0	0	0	0	0	0	1	0	+1.0
0	0	0	0	0	0	0	0	0.0
1	1	1	1	1	1	1	0	-1.0
1	1	1	1	1	1	0	0	-2.0
1	1	1	1	1	0	1	0	-3.0
1	1	1	1	1	0	0	0	-4.0
1	1	1	1	0	1	1	0	-5.0
1	1	1	1	0	1	0	0	-6.0

1. Accuracy of noise margin is ± 1 dB

RD3(LSB), RD4(MSB)—Coefficient Read Register

Address: RD3 (A3-0 = 0011)
RD4 (A3-0 = 0100)
Default: xxh (x=undefined)
Attributes: Read Only

Coefficient Read Word (read from the HDX) comes from the location configured in the Read Coefficient Select Register (WR3, Address A3-0 = 0011). The HDX updates this word on the rising edge of the receive clock, FS. Read register RD3 is the lower byte, and RD4 is the upper byte.

Table 14: Coefficient Read Register

Bit	Description
b7-b0	**Coefficient Word Value.** RD3 contains the lower byte; RD4 the upper byte.

RD5—Activation Status Register

Address: A3-0 = 0101
Default: xxh (x=undefined)
Attributes: Read Only

The ACT bits indicate the current state of the HDX transceiver during the Activating State as listed in Table 15. (For any state other than the Activating State, the ACT bits will be "0000".)

Table 15: Activation Status Register RD5

ACT Bits 3-0	State in LTU Mode	State in NTU Mode
0000	Inactive	Inactive
0001	Pre-AGC	Wait
0010	Pre-EC	AAGC
0011	SIGDET	EC
0100	AAGC	PLL1
0101	EC	PLL2
0110	PLL	4LVLDET
0111	4LVLDET	FRMDET
1000	FRMDET	–

RD6—Receive Step Gain Register

Address: A3-0 = 0110

Default: xxh (x=undefined)

Attributes: Read Only

This 8-bit register represents AGC and FFE gain coefficients (GAGC and GFFE, respectively). Bit assignments are listed in Table 16. The approximate line loss (LL) can be determined using these values in the following equation:

$$LL = 20\log_{10}(GFFE * AGC\ tap) + GAGC + 28\ dB$$

GFFE corresponds to DAGC in the HDX and GAGC is from the ACC. Bits ST0-ST2 indicate the Data Pump activation states as shown in Figures 5 and 7 and Table 17.

Table 16: Receiver AGC and FFE Step Gain Register RD6

Bit	Description
b7	**Data Pump Activation State–bit 2 (ST2).**
b6	**Data Pump Activation State–bit 1 (ST1).**
b5-b4	**Digital Gain Word–bit 1 and 0 (GFFE1,0).** **Bits <5:4> GFFE Value** 00 $2^0 = 1$ 01 $2^1 = 2$ 10 $2^2 = 4$ 11 $2^3 = 8$
b3	**Data Pump Activation State–bit 0 (ST0).**
b2-b0	**Analog Gain Word–bit 2,1 and 0 (GAGC2,1,0).** **Bits <2:0> GAGC Value (db)** 000 -12 001 -10 010 -8 011 -6 100 -4 101 -2 110 0 111 +2

Activation State Machines

The Data Pump Activation/Start-Up circuitry is compatible with ETSI ETR-152. Full LTU activation is partitioned between the Data Pump and the framer. Figure 5 represents the LTU Data Pump Activation State Machine, and Figure 6 shows the LTU framer activation state machine. Figures 7 and 8 present the corresponding NTU state machines. Table 17 lays out the correspondence between the Data Pump and Framer state machines. In Software Mode, the ST*n* bits in Read Register 6 (ADDR 0110) show the current status of the state machine.

LTU Data Pump Activation

When the LTU Data Pump is powered up and reset is applied, the chip is in the Inactive State as shown at the top of Figure 5. Starting at the Inactive State, the device progresses in a clockwise direction through the Activating, Active-1, Active-2, Pending De-Activation and De-Activated States.

In the hardware mode when the Data Pump is in the Inactive State and the QUIET pin is Low, a Low-to-High transition on the ACTREQ pin initiates activation of the link. In the software mode when the Data Pump is in the Inactive State and the QUIET bit is set to 0, setting the ACTREQ bit to 1 initiates activation of the link. Because the ACTREQ control bit is level sensing, it should be set to 1 and then reset to 0 again within 25 seconds to generate a single activation request.

During the Activating State, the echo canceller, equalizer and timing recovery circuits are all adapting during the simultaneous transmission and reception of the framed, scrambled-ones data transmitted as a two-level code (S0) or as the four-level code (S1). If the receive frame sync word is not detected in two consecutive frames within 30 seconds, the timer expires and the device moves to the De-Activated State and ceases transmission. It will then immediately transition to the Inactive State (setting LOST regardless of whether NTU transmission has ceased). Another activation request should not be generated for 32 seconds allowing the NTU to timeout, detect LOS and move from the De-Activated to the Inactive State. In microprocessor-based systems, this time may be shortened by implementing a processor routine to reset the NTU Data Pumps which are in the Activating State when no LTU signal is present.

Successful detection of the sync word drives the State machine to the Active-1 State. This is indicated by a 0-to-1 transition of the ACTIVE bit (Software Mode). If the LTU Data Pump remains locked to the sync word until the Activation Timer expires, the device transitions to the Active-2 (fully active) State. If sync is lost, as indicated by a 0-to-1 transition on LOSW, the LTU Data Pump transitions to the Pending De-Activation State.

In Pending De-Activation, the LTU Data Pump progresses to the De-Activated and Inactive States with the expiration of the respective timers. If the sync word is detected before the LOSW timer expires, the LTU Data Pump returns to either Active 1 or Active-2. (The LTU Data Pump returns to whichever state it occupied before transitioning to Pending De-Activation.)

The LTU Data Pump will exit the Active-2 State in one of two ways. A Low-to-High transition on the QUIET pin (Hardware Mode) or the QUIET bit (Software Mode), forces the LTU Data Pump directly to the De-Activated State. The only other means of exiting the Active State is through a loss of receive sync word (LOSW). LOSW is set when six consecutive frames occur without a sync word match. The LOSW event puts the LTU Data Pump into the Pending De-Activation State.

The LTU Data Pump remains in the Pending De-Activation State for a maximum of two seconds. If a sync word is detected within two seconds after the LOSW event, the LTU Data Pump re-enters the Active State. If the LOSW condition exceeds two seconds, an LOSWT event occurs which sends the chip to the De-Activated State. When the De-Activated State is reached from Pending De-Activation, the LTU Data Pump returns to the Inactive State and declares LOST when it detects no signal from the NTU for one second. The Data Pump should remain in the Inactive State for 15 seconds before another activation attempt.

Table 17: Data Pump/Framer Activation State Machine Correspondences

ST2	ST1	ST0	Data Pump State	Framer State
0	0	0	Inactive	Idle
0	0	1	Activating – 30 sec timer running	Idle
0	1	0	Active – 30 sec timer running (Active-1)[1]	Idle, Active-R or Active-T, or Link Active
0	1	1	Active – 30 sec timer expired (Active-2)[1]	Link Active
1	0	0	Pending De-Activation[1]	Link Active or Active-R or Active-T
1	0	1	De-Activated	Idle
1	1	0	*unused*	*unused*
1	1	1	*unused*	*unused*

1. The data pump samples the TDATA input for all transmit data except the 14 sync bits at the start of each frame during states 010, 011 and 100.

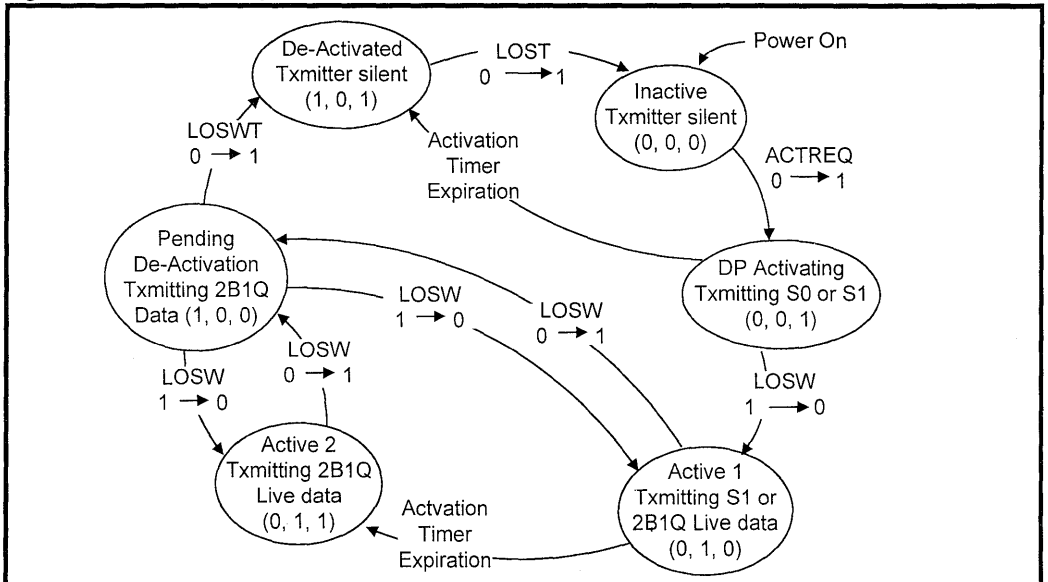
LTU Framer Activation

Figure 6 shows the activation state machine for the LTU HDSL framer. Transition to the Link Active stage from the Idle stage (upper left) requires successful exchange of a pair of indicator bits, **indc** and **indr**. ("INDC" and "INDR" are internal status signals within the HDSL framer; "**indc**" and "**indr**" are bits in the overhead channel.) The LTU device transmits the **indc** bit, and the NTU device transmits the **indr** bit. The overhead frame carries these indicator bits during transmission of the S1 training pattern.

Figure 6 illustrates the two partially active states (Active-R and Active-T) which may serve as transitions between the Idle and Link Active States. If the LTU device reaches the SNR threshold, its framer sets the INDC bit and the device transitions to the Active-R State. If the NTU device reaches the SNR threshold, it will transmit the **indr** bit to the LTU. The LTU will then transition to the Active-T State. From either of the partially Active States, the devices transition to the full Link Active State only with both Indication bits set.

Upon entering the Active States (Active-R, Active-T or Link Active), the chip will open up the full duplex communication link with the NTU. Only the Active and Pending De-Activation States allow full payload transmission. In all states except Active-1 and Active-2, the RDATA output is clamped High.

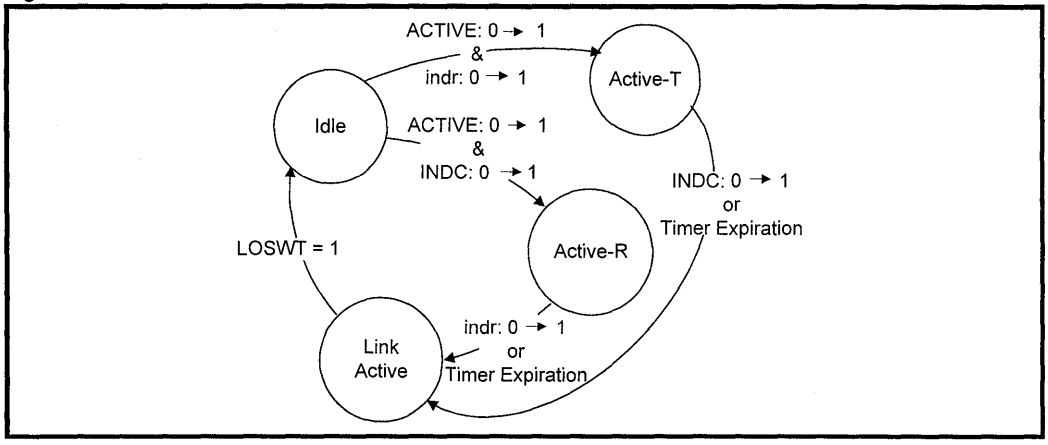
Figure 5: LTU Data Pump Activation State Machine



NOTE: (n, n, n) indicates the status of bits ST2, ST1 and ST0 respectively.

7

Figure 6: LTU HDSL Framer Activation State Machine



NTU Data Pump Activation

Figures 7 and 8 represent the NTU Data Pump Activation State Machine and the NTU HDSL Framer State Machine. The activation state machines for NTU and LTU devices are similar. Both Data Pump machines start at the Inactive State and progress clockwise through the Activating, Active-1, Active-2, Pending De-Activation, and De-Activated States. One difference between them is in the initial condition required to exit from the Inactive State. The LTU Data Pump responds to the Activation Request (ACTREQ) signal. The NTU device responds only to the presence of signal energy on the link. Thus, only an active LTU device can bring up the link. Once the LTU begins transmitting, the NTU device will automatically activate and attempt synchronization.

The other difference between the Data Pump state machines is the impetus for the change from the De-Activated to the Inactive State. In the LTU Data Pump, expiration of a one-second loss of signal timer (LOST) causes the transition. In the NTU the transition occurs immediately on Loss of Signal (LOS).

NTU Framer Activation

The HDSL framer activation state machines for LTU and NTU are also similar. The difference is in the indicator bits which cause the transition to either the Active-T or Active-R State. On the NTU side, the INDR bit causes the transition to the Active-R State, and the **indc** bit causes the transition to the Active-T State. From either partially active state, receipt of the remaining indicator bit or timer expiry causes the transition to the full Link Active State.

HDSL Synchronization State Machine

Figure 9 shows the HDSL Synchronization State Machine incorporated in the HDX. It applies to both LTU and NTU devices. Table 18 lists the correspondence between the Synchronization states and Activation states. The Sync state machine is clocked by the receive signal framing. Starting at the initial Out-of-Sync condition (State 0), the device progresses in a clockwise direction through State 1 until Sync is declared in State 2. Two consecutive frame sync word matches are required to achieve synchronization.

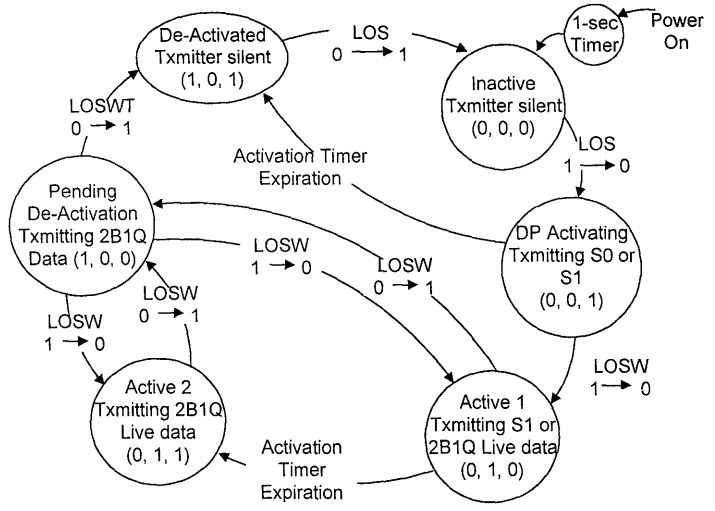
Once the In-Sync condition is declared, six consecutive frame sync mismatches will cause the device to transition through States 3 through 7 and declare an Out-of-Sync condition in State 8. From State 8, the device will return either to State 2 or to State 0. If the 2-second timer expires without re-establishing frame sync (LOSWT = 1) or if the receive signal is lost entirely (LOS = 1), the device returns directly to State 0.

If frame sync is re-established, the device will return to the In-Sync condition (State 2) through State 9 if two consecutive frames are received without any change of frame alignment (COFA = 0). If a change of frame alignment does occur (COFA = 1), two consecutive matches are required to transition through State 10 back to State 2.

Table 18: Activation – Synchronization

Activation State	Synchronization States
Inactive	State 0
Activating	State 1
Active	States 2, 3, 4, 5, 6, and 7
Pending De-Activation	States 8, 9, and 10

Figure 7: NTU Data Pump Activation State Machine



NOTE: (n, n, n) indicates the status of bits ST2, ST1 and ST0 respectively.

Figure 8: NTU HDSL Framer Activation State Machine

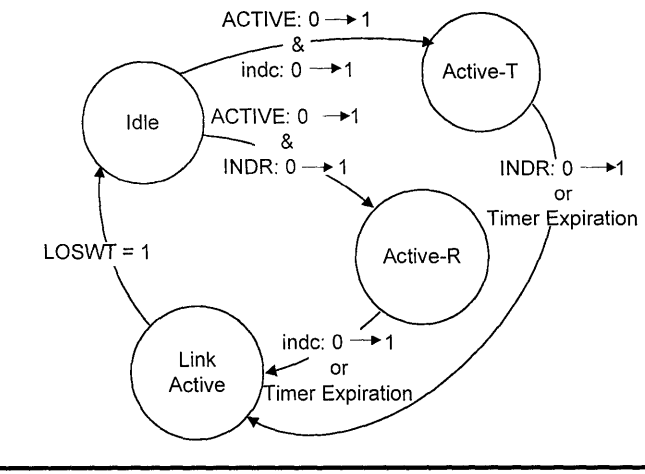
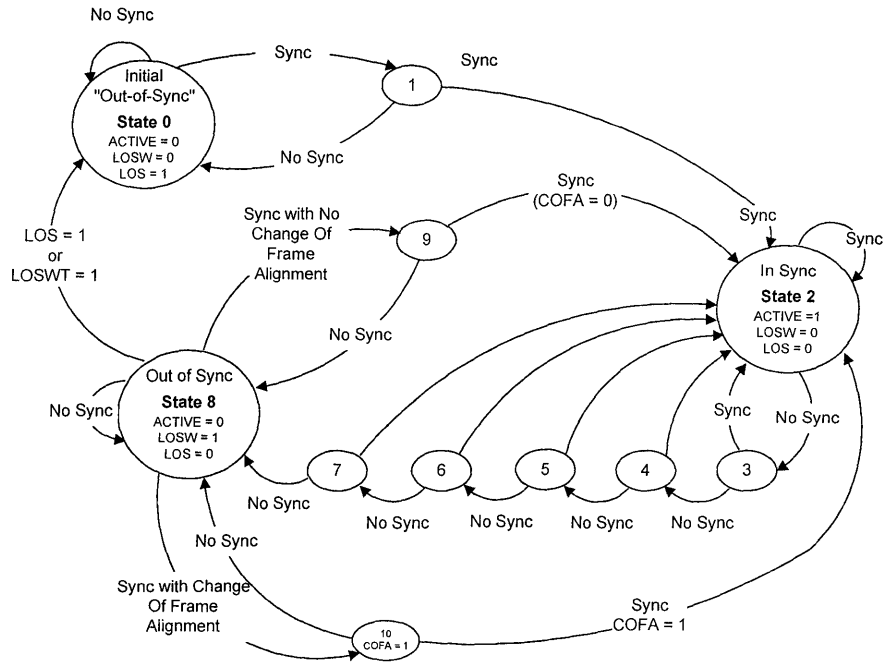


Figure 9: HDSL Synchronization State Machine



NOTES:

1. "Sync" = Frame Sync Word Match. "No Sync" = Frame Sync Word Mismatch.
2. A 0-to-1 transition on QUIET will set the Sync State Machine from any State to State 0.
3. Expiration of the Activation Timer will set the Sync State Machine from State 1 to State 0.

APPLICATION INFORMATION

HDSL Framer State Machine Design

Because of data transparency characteristics of the Data Pump, two issues impact on implementing the HDSL Framer Activation State machines for both LTU and NTU devices:

1. Once the ACTIVE 0-to-1 transition occurs, the Data Pump becomes transparent. Therefore, the HDSL framer must put appropriate data in TDATA. Table 5 summarizes this requirement.
2. The link indicator bits (**indc** and **indr**) must stabilize before the device makes the transition from the Idle to the Active-T State. Thus, the HDSL framer design may detect 6 consecutive matches for the indication bit transition. This is particularly important for non-CSA loops where a lower SNR may be experienced.

PCB Layout

The following are general considerations for PCB layout using the HDSL Data Pump chip set:

- Refer to Figures 10, 11, 12 and 13, and Table 19. Keep all shaded components close to the pins they connect to.
- Use a four-layer or more PCB layout, with embedded power and ground planes.
- Break up the power and ground planes into the following regions, and tie these regions together at the common point where power connects to the circuit:
  - Digital Region
  - Analog Region
    - VCXO subregion
    - ACC, Line I/F, and IBIAS subregion
- Use larger feedthroughs ("vias") and tracks for connecting the power and ground planes to the power and ground pins of the ICs than for signal connections. Place the decoupling capacitors right at the feedthrough power/ground plane ties, or on the tracks to the IC power/ground pins as close to the pins as possible.
- On the User Interface Connector, route digital signals to avoid proximity to the TIP, RING, and CT lines.
- Provide at least 100 µF or more of bulk power supply decoupling at the point where power is connected to the Data Pump circuit.

User Interface

The REFCLK and CK9M signals are sensitive to capacitive loading and rise time. Keep the rise time (from 10%-90%) for these signals less than 5 ns.

Digital Section

- Keep all digital traces separated from the analog region of the Data Pump layout.
- Provide high frequency decoupling capacitors (0.01 µF ceramic or monolithic) around the HDX as shown in Figures 11 and 12. The capacitor on the HDX VCC1 pin (pin 1) should be on the IC side of the diode.
- It is possible to replace the NAND gate (shown in Figure 12) with an AND gate.

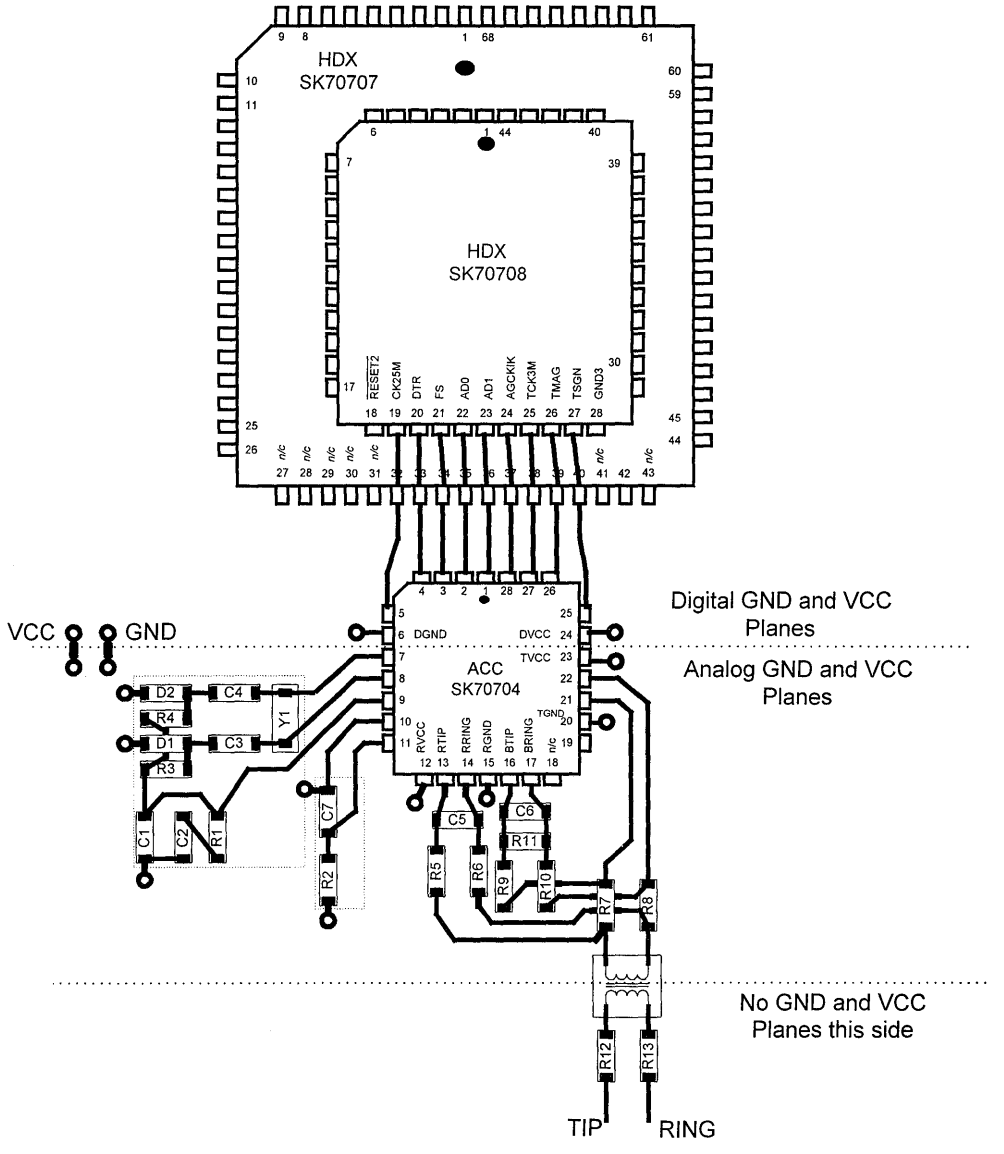
Analog Section

The analog section of the PCB consists of the following subsections:

1. ACC and power supply decoupling capacitors
2. Bias Current Generator
3. Voltage Controlled Crystal Oscillator
4. Line Interface Circuit

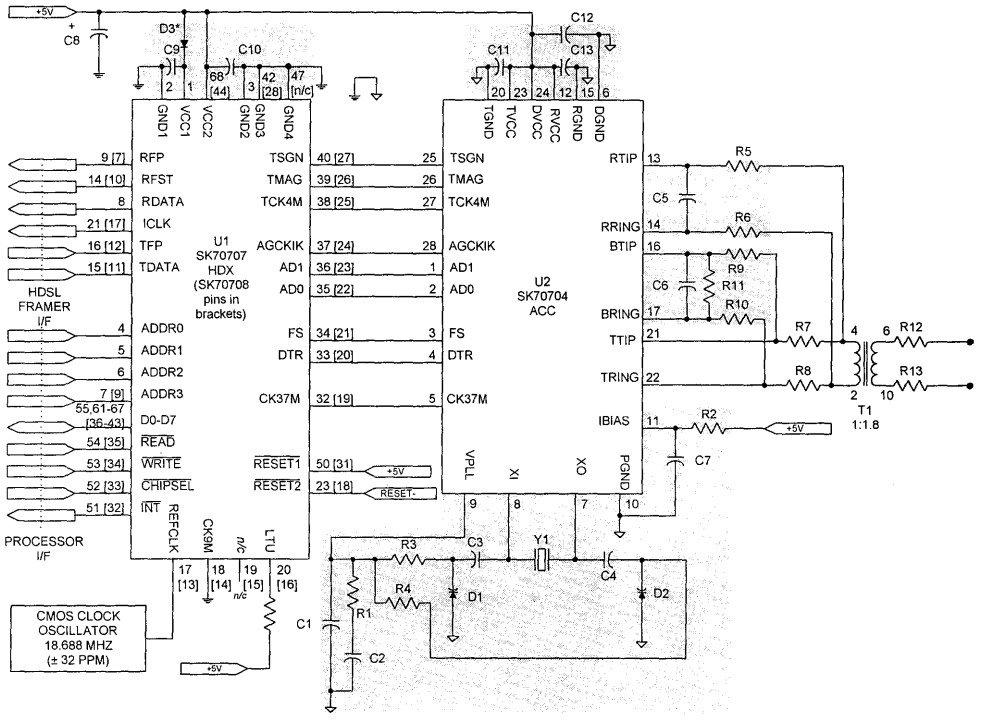
- Route digital signals AD0, AD1, FS, DTR, TSGN, TMAG, TCK4M, and AGCKIK on the solder side of the PCB, and route all analog signals on the component side as much as possible.
- Route the following signal pairs as adjacent traces:
- TTIP/TRING
- BTIP/BRING
- RTIP/RRING
- but keep the pairs separated from each other as much as possible.
- To maximize high voltage isolation, do not run the analog ground plane under the transformer line side.

Figure 10: PCB Layout Guidelines



NOTE: The VCC and GND planes for Digital and Analog sides should be connected at a single point.

Figure 11: Typical Support Circuitry for LTU Applications



NOTES:
Diode D3 is optional.
The HDX and ACC should have independent ground planes connected at a single point near pin 5 of the ACC.

Table 19: Components for Suggested Circuitry (See Figures 11 and 12)

Ref	Description	Ref	Description	Ref	Description
C1, 9, 10	0.01 µF, ceramic, 10%	R1	10.0 kΩ, 1%	R12, 13	5.6 Ω, line feed fuse resistor (ALFR-2-5.6-1 IRC)
C2	33 µF, electrolytic, 20% low leakage ≤5 µA @ 25° C	R2	35.7 kΩ, 1%		
		R3, 4	20.0 kΩ, 1%	D1, 2	Varicap diode (Motorola MV209)
C3, 4	1000 pF, ceramic, 20%	R5, 6	301 Ω, 1%	D3	Silicon rectifier diode (1N4001)
C5, 6	470 pF, COG or mica, 10%	R7, 8[1]	18.2 Ω, 1%	Y1	37.376 MHz crystal (Hy-Q International 81256/1)
C7, 11-13	0.1 µF, ceramic, 10%	R9, 10	604 Ω, 1%		
C8	100 µF, electrolytic, 20%	R11	1.43 kΩ, 1%	T1	1:1.8 (Midcom 671-7671 or Pulse Engineering PE-68650)
		R14	10.0 kΩ, 1%		

1. R7, R8 should be 20 Ω, when R12 and R13 (the 5.6 Ω fuse links) are not used.

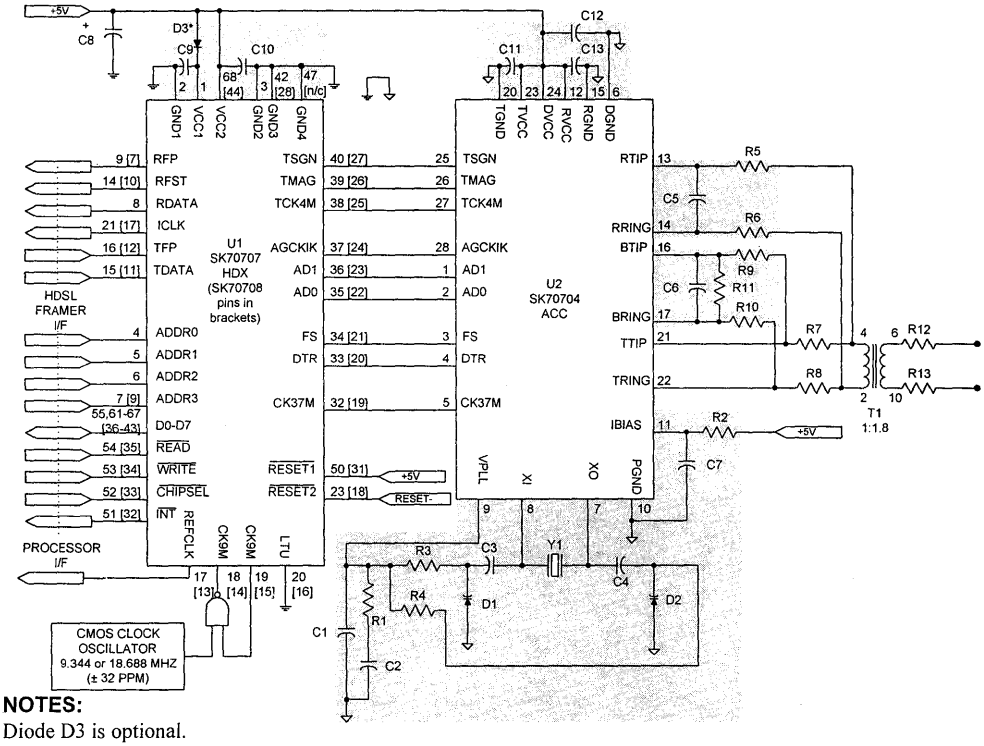
Table 20: Transformer Specifications
(Figures 11 and 12, Reference T1)

Measure	Value	Tolerance
Turns Ratio (IC:Line)	1:1.8	±1%
Secondary Inductance (Line Side)	2.05 mH	±6%
Leakage Inductance	≤ 50 µH	
Interwinding Capacitance	≤ 60 pF	
THD	≤ -70 dB	
Longitudinal Balance	≥ 50 dB	5-292 kHz
Return Loss	≥ 20 dB	40-200 kHz
Isolation	2000 VRMS	
Primary DC Resistance	≤ 2.0 Ω	
Secondary DC Resistance	≤ 4.0 Ω	
Operating Temperature	-40 to +85 °C	

Table 21: Crystal Specifications
(Figures 11 and 12, Reference Y1)

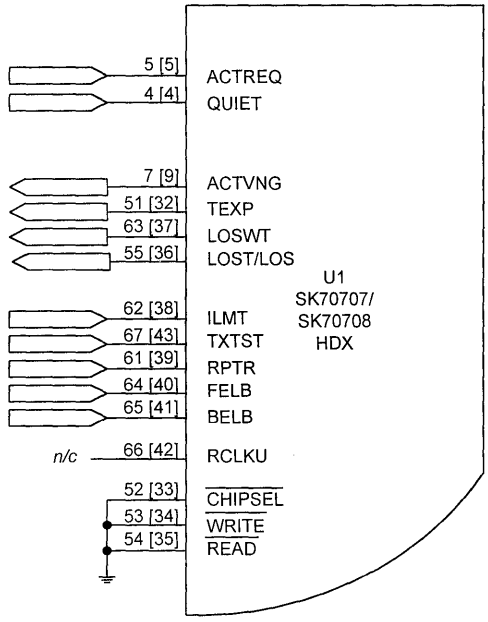
Measure	Value	Tolerance
Calibration Frequency	37.376 MHz @ C_L = 20 pF	0 to +40 ppm
Mode	Fundamental, Parallel Resonance	
Pullability (C_L = 24 pF ⇨ 16 pF)	≥ +160 ppm	
Operating Temperature	-40 to +85 °C	
Temperature Drift	≤ ±30 ppm	
Aging Drift	≤ 5 ppm/year	
Series Resistance	≤ 15 Ω	
Drive Level	0.5 mW	
Holder	HC-49	

Figure 12: Typical Support Circuitry for NTU Applications



NOTES:
Diode D3 is optional.
The HDX and ACC should have independent ground planes connected at a single point near pin 5 of the ACC.

Figure 13: SK70707/SK70708 HDX Control and Status Signals (Hardware Mode)



NOTES:

1. This figure illustrates the HDX control and status signals in Hardware Mode. All other HDX and ACC signals are connected as shown in Figures 11 and 12.
2. Pin numbers for SK70708 are shown in brackets [ ]. Pin numbers outside brackets are for SK70707.

7

TEST SPECIFICATIONS

NOTE

The minimum and maximum values in Tables 22 through 32 and Figures 14 through 20 represent the performance specifications of the Data Pump and are guaranteed by test, except where noted by design.

Table 22: ACC Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Supply voltage[1] reference to ground[2]	TVCC, RVCC, DVCC	-0.3	+6.0	V
Input voltage[2, 3], any input pin	TVCC, RVCC, DVCC	- 0.3V	VCC + 0.3	V
Continuous output current, any output pin	–	–	±25	mA
Storage temperature	TSTOR	-65	+150	°C

CAUTION

Operations at the limits shown may result in permanent damage to the Analog Core Chip. Normal operation at these limits is neither implied nor guaranteed

1. No supply input may have a maximum potential of more than ±0.3 V from any other supply input.
2. TGND = 0V; RGND = 0V; DGND = 0V.
3. TVCC = RVCC = DVCC = VCC.

Table 23: ACC Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
DC supply	TVCC, DVCC, RVCC	4.75	5.0	5.25	V
Ambient operating temperature	TA	-40	+25	+85	°C

Table 24: ACC DC Electrical Characteristics (Over Recommended Range)

Parameter	Sym	Min	Typ[1]	Max	Unit	Test Conditions
Supply current (full operation)	ICC	–	102	137	mA	83 Ω resistor across TTIP and TRING
DVCC current		–	7	12	mA	
RVCC current		–	30	50	mA	
TVCC current		–	65	75	mA	Normal Mode 8+3, 8-3, 8+3, ...
		–	38	48	mA	Off Mode
Input Low voltage	VIL	–	–	0.5	V	IIL < 40 µA
Input High voltage	VIH	4.5	–	–	V	IIH < 40 µA
Output Low voltage	VOL	–	–	0.2	V	IOL < 40 µA

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.
2. Applies to pins 3, 4, 25, 26 and 27.

Table 24: ACC DC Electrical Characteristics (Over Recommended Range) – continued

Parameter	Sym	Min	Typ[1]	Max	Unit	Test Conditions
Output High voltage	VOH	4.5	–	–	V	$I_{OH} < 40\ \mu A$
Input leakage current[2]	IIL	–	–	±50	µA	$0 < V_{IN} < V_{CC}$
Input capacitance (individual pins)	CIN	–	12	–	pF	
Load capacitance (REFCLK output)	CLREF	–	–	20	pF	

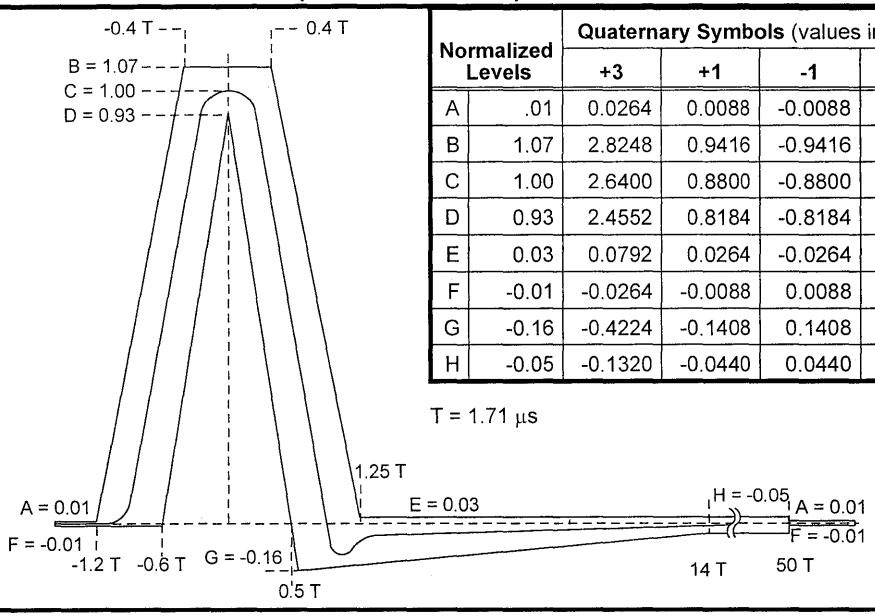
1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.
2. Applies to pins 3, 4, 25, 26 and 27.

Table 25: ACC Transmitter Electrical Parameters (Over Recommended Range)

Parameters	Sym	Min	Typ	Max	Unit	Test Conditions
Isolated pulse height at TTIP, TRING		+2.455	+2.640	+2.825	Vp	TDATA High, TFP Low (+3)
		-2.825	-2.640	-2.455	Vp	TDATA Low, TFP Low (-3)
		+0.818	+0.880	+0.941	Vp	TDATA High, TFP High (+1)
		-0.941	-0.880	-0.818	Vp	TDATA Low, TFP High (-1)
Setup time (TSGN, TMAG)	tTSMSU	5	–	–	ns	
Hold time (TSGN, TMAG)	tTSMH	12	–	–	ns	

NOTE:
Pulse amplitude measured across a 135 Ω resistor on the line side of the transformer using the application circuit shown in Figure 11 and Table 19.

Figure 14: ACC Normalized Pulse Amplitude Transmit Template



Normalized Levels		Quaternary Symbols (values in Volts) +3	+1	-1	-3
A	.01	0.0264	0.0088	-0.0088	-0.0264
B	1.07	2.8248	0.9416	-0.9416	-2.8248
C	1.00	2.6400	0.8800	-0.8800	-2.6400
D	0.93	2.4552	0.8184	-0.8184	-2.4552
E	0.03	0.0792	0.0264	-0.0264	-0.0792
F	-0.01	-0.0264	-0.0088	0.0088	0.0264
G	-0.16	-0.4224	-0.1408	0.1408	0.4224
H	-0.05	-0.1320	-0.0440	0.0440	0.1320

T = 1.71 µs

Figure 15: ACC Transmitter Timing

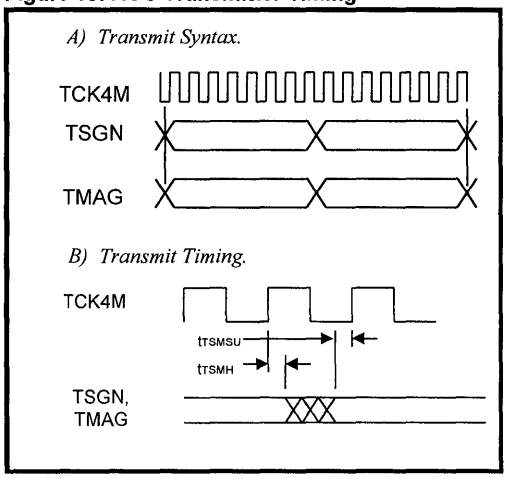


Figure 16: Upper Bound of Transmit Power Spectral Density

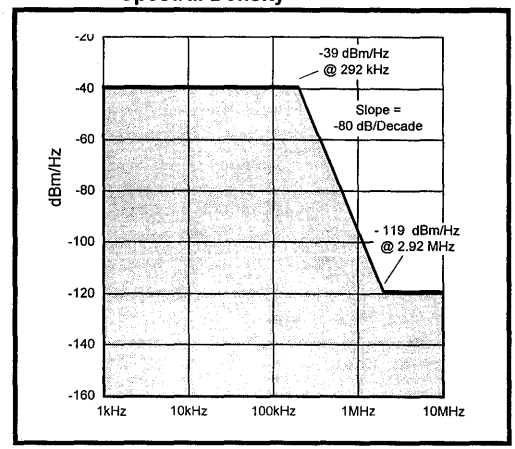


Table 26: ACC Receiver Electrical Parameters (Over Recommended Range)

Parameter	Sym	Min	Typ	Max	Unit	Test Conditions
Propagation delay (AD0, AD1)	tADD	–	–	25	ns	
Total harmonic distortion		–	-80	–	dB	V(RTIP, RRING) = 3 Vpp @ 50 kHz
RTIP, RRING, to BTIP, BRING gain ratio		–	1.0	1%	V/V	

Figure 17: ACC Receiver Syntax and Timing

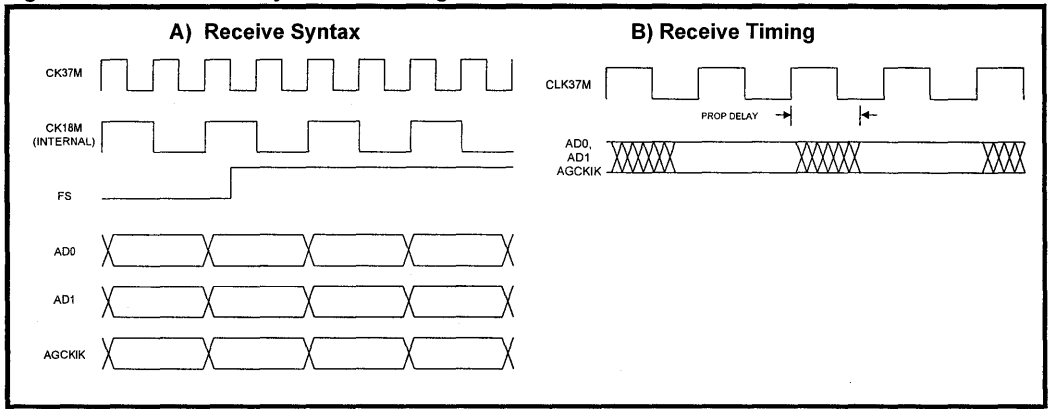


Table 27: HDX Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Supply voltage[1] reference to ground[2]	VCC2, VCC1	-0.3	+6.0	V
Input voltage[2], any input pin	–	- 0.3	VCC2 + 0.3	V
Continuous output current, any output pin	–	–	±25	mA
Storage temperature	TSTOR	-65	+150	°C

CAUTION

Operations at the limits shown may result in permanent damage to the HDSL Digital Transceiver (HDX). Normal operation at these limits is neither implied nor guaranteed

1. The maximum potential between VCC2 and VCC1 must never exceed ±1.2 V.
2. GND4 = GND3 = 0V; GND2 = 0V; GND1 = 0V.

Table 28: HDX Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
DC supply	VCC1[1]	3.95	5.0	5.25	V
	VCC2	4.75	5.0	+5.25	V
	VCC2-VCC1	-0.25	–	+0.9	V
Ambient operating temperature	TA	-40	–	+85	°C

1. To derive this supply, a 1N4001 (or equivalent) diode may be connected between VCC2 and VCC1 as shown in Figures 11 and 12. The diode should be selected to meet VCC1 minimum specifications.

Table 29: HDX DC Electrical Characteristics (Over Recommended Range)

Parameter	Sym	Min	Typ[1]	Max	Unit	Test Conditions
Supply current (full operation)	ICC	–	125	175	mA	
Input Low voltage	VIL	–	–	0.5	V	IIL < 40 µA
Input High voltage	VIH	4.0	–	–	V	IIH < 40 µA
Output Low voltage	VOL	–	–	GND +0.3	V	IOL < 40 µA
Output High voltage	VOH	VCC2-0.5	–	–	V	IOH < 40 µA
Input leakage current[2]	IIL	–	–	±50	µA	0 < VIN < VCC2
Tristate leakage current[3]	ITOL	–	–	±30	µA	0 < V < VCC2
Input capacitance (individual pins)	CIN	–	12	–	pF	
Load capacitance (REFCLK output)	CLREF	–	–	15	pF	

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Applies to all pins that can be configured as inputs. Refer to Table 3 for a complete list of signals.
3. Applies to SK70707 pins 8, 9, 14, 19, 21, 49, 51, 55, and 61-67 or SK70708 pins 7, 8, 10, 15, 17, 30, 32, and 36-43 when tristated.

Table 30: HDX/HDSL Data Interface Timing (See Figure 18)

Parameter	Symbol	Min	Typ[1]	Max	Unit
ICLK frequency	f_{ICLK}	–	1168	–	kHz
REFCLK frequency	f_{REFCLK}	–	18.688	–	MHz
REFCLK frequency tolerance (LTU Mode)	tol_{RCLK}	-32	0	+32	ppm
CK9M frequency tolerance (NTU Mode)[2]	tol_{CK6M}	-32	0	+32	ppm
ICLK pulse width high	t_{IPW}	–	428	–	ns
Transition time on any digital output[3]	t_{TO}	–	5	10	ns
Transition time on any digital input	t_{TI}	–	–	25	ns
TDATA, TFP setup time to ICLK rising edge	t_{TSU}	100	–	–	ns
TDATA, TFP hold time from ICLK rising edge	t_{TH}	100	–	–	ns
RDATA, RFP, RFST delay from ICLK falling edge	t_{TD}	0	–	150	ns
TFP pulse width[4]	t_{TFPW}	828	856	884	ns
TFP falling edge to ICLK rising edge[4]	t_{TFIR}	300	–	400	ns
TFP setup time to REFCLK rising edge[4]	t_{TSUR}	25	–	–	ns

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. CK9M must meet this tolerance about an absolute frequency of 9.344000 MHz or 18.688000 MHz in NTU mode.
3. Measured with 15 pF load.
4. These parameters apply only to an LTU mode Data Pump programmed for repeater applications as shown in Figure 18.

Figure 18: HDX/HDSL Data Interface Timing

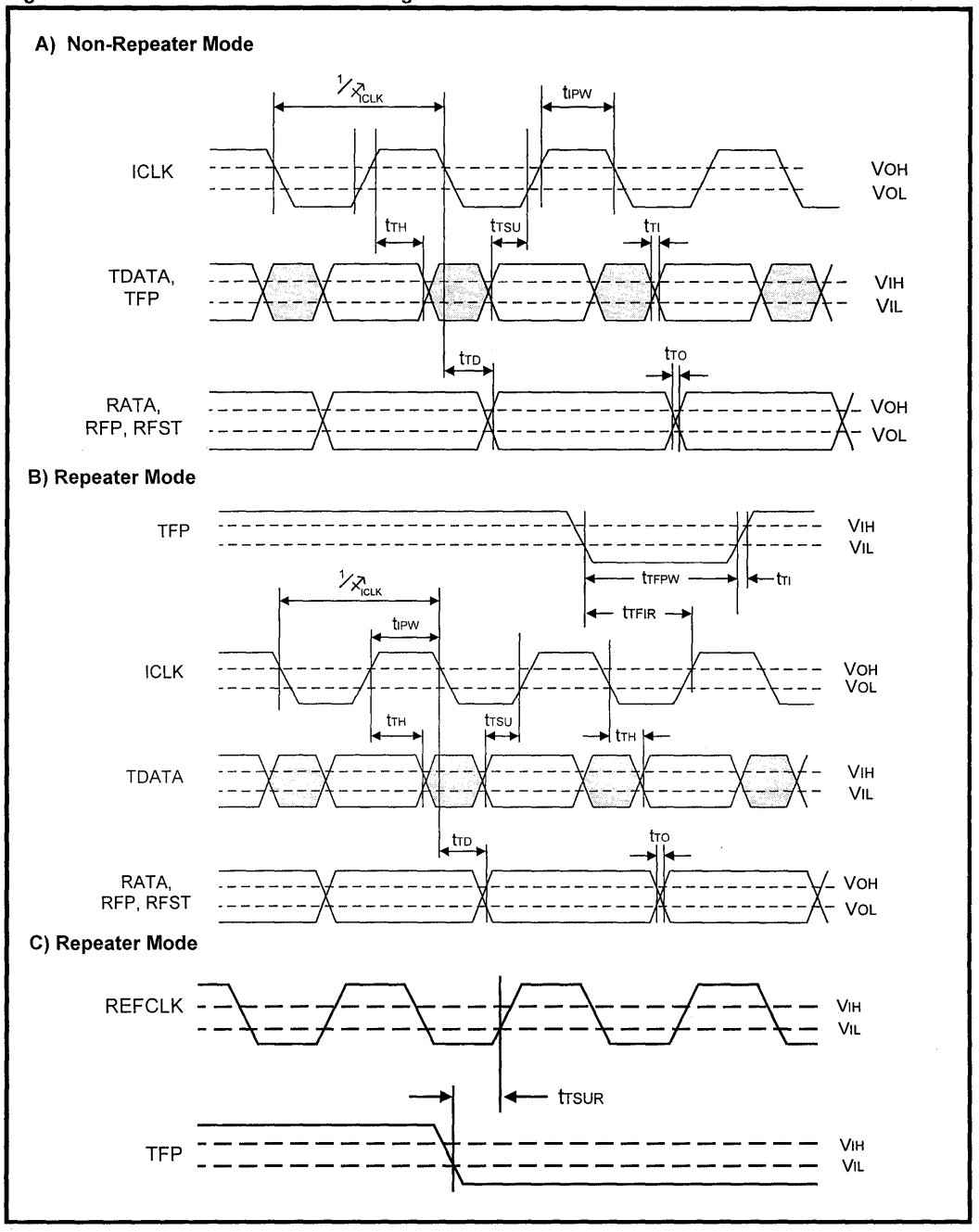


Table 31: HDX/Microprocessor Interface Timing Specifications[1] (See Figures 19 and 20)

Parameter	Symbol	Min	Typ	Max	Unit
$\overline{\text{RESET2}}$ pulse width Low	tRPWL	0.1	–	1,000	µs
$\overline{\text{RESET2}}$ to $\overline{\text{INT}}$ clear (10 kΩ resistor from $\overline{\text{INT}}$ to VCC2)	tINTH	–	–	300	ns
$\overline{\text{RESET2}}$ to data tristate on D0-7	tDTHZ	–	–	100	ns
$\overline{\text{CHIPSEL}}$ pulse width Low	tCSPWL	200	–	–	ns
$\overline{\text{CHIPSEL}}$ Low to data active on D0-7	tCDLZ	–	–	80	ns
$\overline{\text{CHIPSEL}}$ High to data tristate on D0-7	tCDHZ	–	–	80	ns
$\overline{\text{READ}}$ pulse width Low	tRSPWL	100	–	–	ns
$\overline{\text{READ}}$ Low to data active	tRDLZ	–	–	80	ns
$\overline{\text{READ}}$ High to data tristate	tRDHZ	–	–	80	ns
Address to valid data[2]	tPRD	–	–	80	ns
Address setup to $\overline{\text{WRITE}}$ rising edge[2]	tASUW	20	–	–	ns
Address hold from $\overline{\text{WRITE}}$ rising edge[2]	tAHW	10	–	–	ns
$\overline{\text{WRITE}}$ pulse width Low	tWPWL	100	–	–	ns
Data setup to $\overline{\text{WRITE}}$ rising edge	tDSUW	20	–	–	ns
Data hold from $\overline{\text{WRITE}}$ rising edge	tDHW	10	–	–	ns
$\overline{\text{READ}}$ High to $\overline{\text{INT}}$ clear when reading register RD0	tINTR	–	–	400	ns

1. Timing for all outputs assumes a maximum load of 30 pF.
2. "Address" refers to input signals $\overline{\text{CHIPSEL}}$, A0, A1, A2, and A3. "Data" refers to I/O signals D0, D1, D2, D3, D4, D5, D6, and D7.

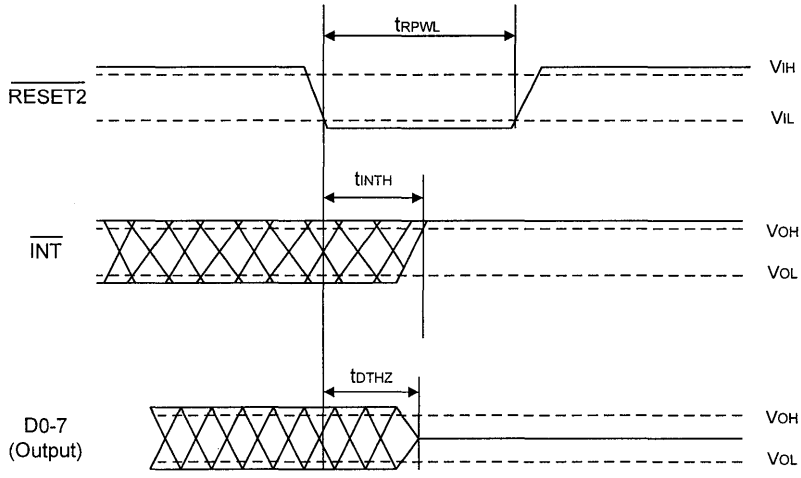
Table 32: General System and Hardware Mode Timing

Parameter		Min	Typ[1]	Max	Unit
Throughput delay	TDATA to TTIP/TRING	–	6.85	12.5	µs
	RTINP/RRING to RDATA	–	36.0	72	µs
Hardware mode	"ACTREQ" input transitional pulse width (High or Low)	5	–	–	µs
	"QUIET" transitional pulse width (High-to-Low)	5	–	–	µs

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.

Figure 19: Reset and Interrupt Timing (μP Control Mode)

A) Reset Timing



B) Interrupt Timing

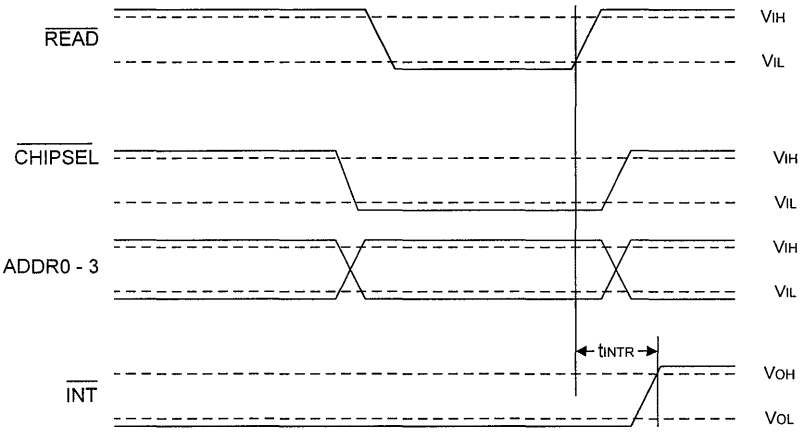


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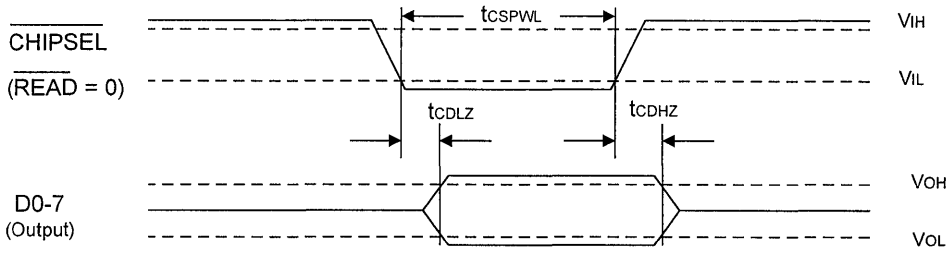
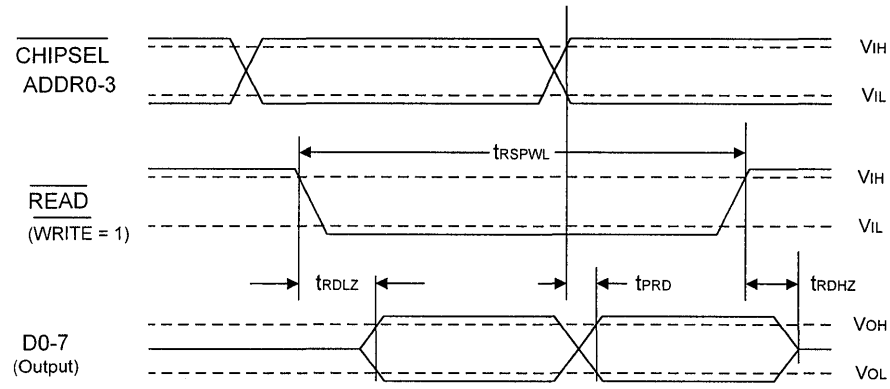
Figure 20: Parallel Data Channel Timing

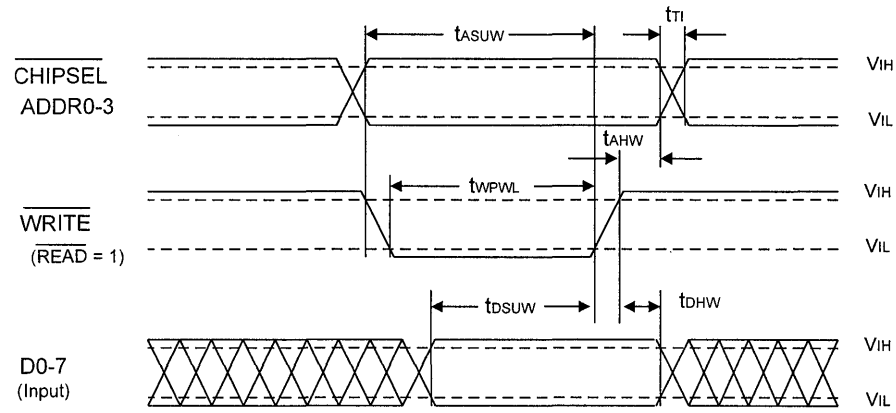
A) Chip Select Timing



B) Data Read Timing



C) Data Write Timing



LXP710

HDSL Framer/Mapper for 1168 kbps Applications

General Description

The LXP710 is a complete HDSL framer/mapper that multiplexes and demultiplexes a framed or unframed 2.048 Mbps E1 data stream onto two 1168 kbps HDSL lines. The LXP710 also supports point-to-point and point-to-multipoint fractional E1 applications with 1, 2 or 3 HDSL lines.

The LXP710 interfaces directly with the Level One SK70704/SK70707 1168 kbps HDSL data pump and industry standard E1 Framers or Line Interface ICs. The framer/mapper is controlled and monitored by an external processor using an 8-bit Intel or Motorola compatible parallel interface. The framer/mapper provides both programmable and 6ms interrupts synchronized to the HDSL frame rate.

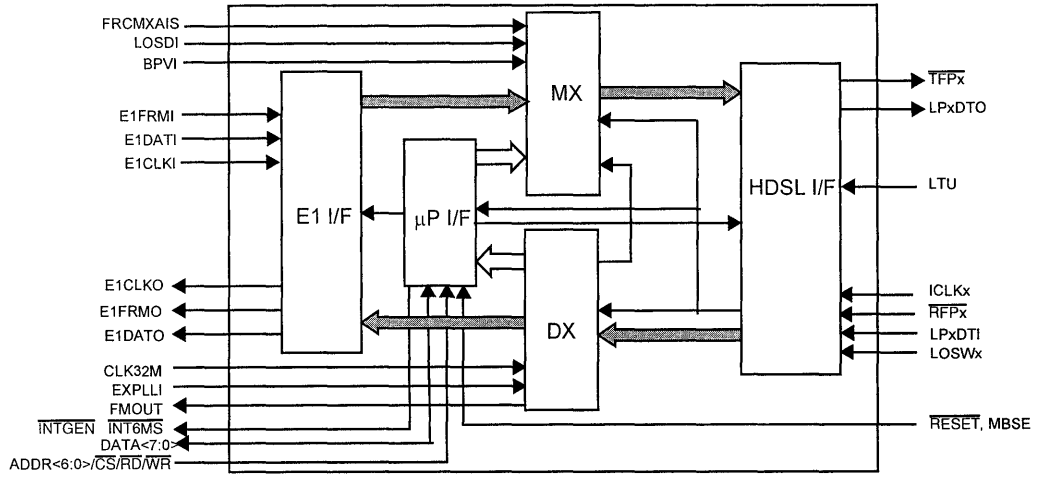
The LXP710 provides fully programmable mapping between the E1 and HDSL interfaces on one or more loops. The LXP710 provides support for system performance monitoring with internal CRC, FEBE and BPV error counters and the capability to inject these errors.

The framer/mapper automatically controls the synchronization between the HDSL loop timing and the E1 payload timing using a digital PLL for E1 timing recovery and a transmitter stuffing control circuit.

Features

- Compliant with ETSI ETR-152 requirements
- Interfaces with 1, 2 or 3 Level One HDSL Data Pumps and industry standard E1 Framers or Line Interface ICs
- 8-bit, Intel or Motorola compatible parallel processor interface with programmable and 6ms interrupts
- E1 to HDSL Loop Multiplexing/Demultiplexing
  - Programmable timeslot mapping
  - Accepts framed or unframed E1 data
  - IDLE Code Insertion provides channel blocking in mux and demux directions
  - DS0 Channel Grouping
  - Loopbacks toward E1 and HDSL interfaces
- Diagnostics/Performance Monitoring
  - QRSS Pattern Generation and Detection
  - CRC, BPV and FEBE counters and error generators
- User definable 10 kbps overhead channel
- HDSL Overhead Management
- DPLL for E1 Timing Recovery
- HDSL Transmit Stuffing Control

LXP710 Block Diagram



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SK70720/SK70721

Multi-Rate DSL Data Pump Chip Set

General Description

The Multi-Rate DSL Data Pump is a complete, variable-rate transceiver that provides full duplex communication on two wires using echo-canceller-with-hybrid and 2B1Q line coding technology. It provides symmetrical line rates from 272 to 784 kbps. Performance specifications are defined at the 272, 400, 528 and 784 kbps data rates which provide a payload of 4, 6, 8 or 12 64 kbps channels with a 16 kbps overhead channel. The MDSL Data Pump also supports applications where the payload is unchannelized.

The MDSL Data Pump chip set consists of two devices:

- SK70720 MDSL Digital Signal Processor (MDSP)
- SK70721 Integrated Analog Front-End (IAFE)

The IAFE is a fully integrated CMOS analog front-end IC which includes transmitter line drivers, filters, and 2B1Q encoding functions along with the receiver hybrid, AGC, A/D converter modulator and VCXO functions. The MDSP incorporates all digital signal processing required for A/D conversion, echo-cancellation, data scrambling and adaptive equalization as well as transceiver activation state machine control.

Applications

- High speed residential Internet access
- Extended Range fractional T1/E1 transport
- 4, 6, 8 or 12-channel digital pair-gain
- Wireless base station to switch access
- WAN access for LAN routers

Features

- Fully integrated, 2-chip transceiver for interfacing to twisted-pair lines at 272 to 784 kbps
- Integrated line drivers, filters and hybrid circuits reduce the number of external components required
- Self-contained activation/start-up control eliminates an external microprocessor in many applications
- Parallel interface for processor control or monitoring
- Programmable for either link master or slave operation
- Single +5V supply
- Typical power dissipation less than 500 mW—good for applications with remote power feeding
- Supports transparent repeater applications without an external processor or glue-logic
- Supports processor directed rate selection driven by receive signal level and noise margin
- Continuously adaptive echo canceller and equalizers maintain excellent transmission performance with changing noise and line characteristics
- Typical noise-free transmission range:
  <u>784 kbps</u>
  17.0 kft (5.2 km) on #24 AWG (0.5 mm) cable
  12.8 kft (3.9 km) on #26 AWG (0.4 mm) cable
  <u>272 kbps</u>
  22 kft (6.7 km) on #24 AWG (0.5 mm) cable
  16 kft (4.9 km) on #26 AWG (0.4 mm) cable

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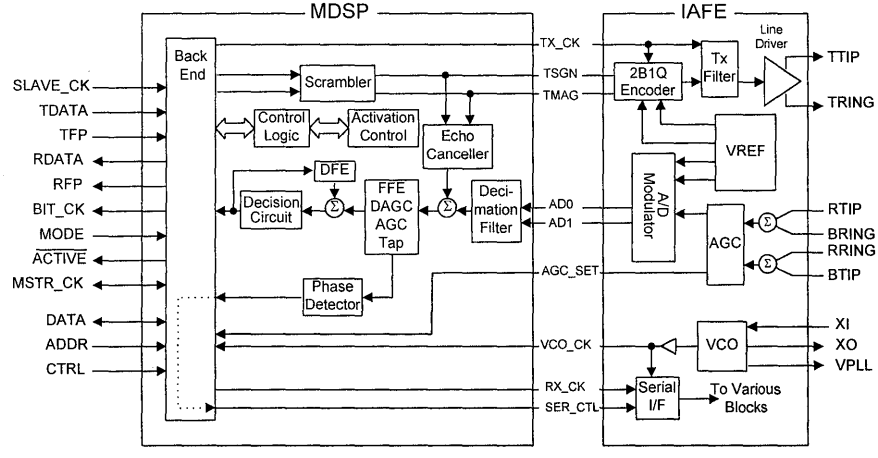
Multi-Rate DSL Data Pump Block Diagram



PIN ASSIGNMENTS AND SIGNAL DESCRIPTIONS

The IAFE is packaged in a 28-pin PLCC. Figure 1 shows the IAFE pin locations. Table 1 lists signal descriptions for each pin, except pins 18 and 19, which are not connected.

The MDSP device is packaged in a 44-pin PLCC. Figure 2 shows MDSP pin designations. Table 2 lists signal descriptions for each pin.

Figure 1: SK70721 IAFE Pin Locations

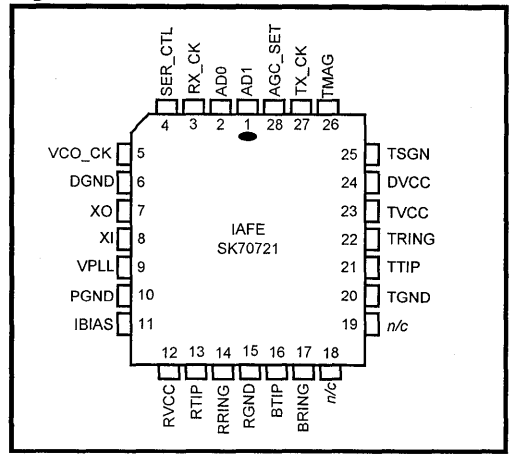


Table 1: SK70721 IAFE Pin Assignments/Signal Descriptions

Group	Pin #	Symbol	I/O[1]	Description
Line	13	RTIP	AI	**Receive Tip and Ring.** Receiver differential inputs.
	14	RRING	AI	
	16	BTIP	AI	**Receive Balance Tip and Ring.** Receiver hybrid balance inputs.
	17	BRING	AI	
	21	TTIP	AO	**Transmit Tip and Ring.** Line driver outputs.
	22	TRING	AO	
PLL	7	XO	AO	**Crystal Oscillator Input and Output.** Connect a pullable crystal whose frequency is 32 times the bit rate between these two pins. Refer to the Applications Section for crystal specifications.
	8	XI	AI	
	9	VPLL	AO	**PLL Control Voltage.** Control signal for the VCXO.
Power	10	PGND	S	**PLL Ground.** 0 V.
	12	RVCC	S	**Receive Power supply.** +5 V (± 5%).
	23	TVCC	S	**Transmit Power supply.** +5 V (± 5%).
	24	DVCC	S	**Digital Power Supply.** +5 V (± 5%).
	6	DGND	S	**DVCC Ground.** 0 V.
	15	RGND	S	**RVCC Ground.** 0 V.
	20	TGND	S	**TVCC Ground.** 0 V.

1. I/O column entries: DI = Digital Input; DO = Digital Output; DI/O = Digital Input/Output; AI = Analog Input; AO = Analog Output; AI/O = Analog Input/Output; S = Supply.

Table 1: SK70721 IAFE Pin Assignments/Signal Descriptions – continued

Group	Pin #	Symbol	I/O[1]	Description
Clock and Control	3	RX_CK	DI	**Receive Baud Rate Clock Input.**
	4	SER_CTL	DI	**Serial Control Input.**
	5	VCO_CK	DO	**MDSL Reference Clock Output.** Used as the receive timing reference for the MDSP.
	27	TX_CK	DI	**Transmit Symbol Clock Input.**
Data Input and Output	28	AGC_SET	DO	**AGC Adjust Output.**
	1	AD1	DO	**A-to-D Converter Data Line 1.**
	2	AD0	DO	**A-to-D Converter Data Line 0.**
	25	TSGN	DI	**Transmit Quat Sign Input.**
	26	TMAG	DI	**Transmit Quat Magnitude.**
Analog Input	11	IBIAS	AI	**Input Bias.** This input sets internal bias currents.

1. I/O column entries: DI = Digital Input; DO = Digital Output; DI/O = Digital Input/Output; AI = Analog Input; AO = Analog Output; AI/O = Analog Input/Output; S = Supply.

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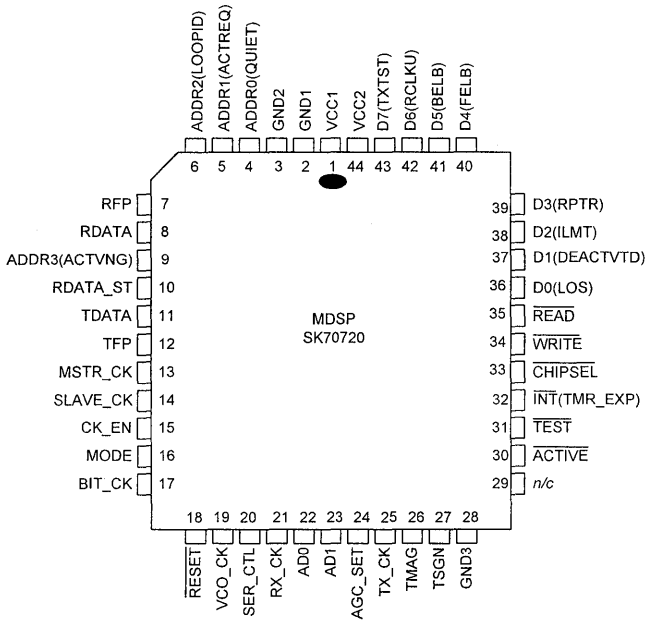
Figure 2: SK70720 MDSP Pin Assignments



NOTE:
Pin Functions in Hardware Control Mode are shown in parentheses.

Table 2: SK70720 MDSP Pin Assignments/Signal Descriptions

Group	Pin #	Symbol	I/O[4]	Description
Power	1	VCC1	S	**Logic Power Supply.** (Refer to Table 27)
	44	VCC2	S	**I/O Power Supply.** +5 V (± 5%).
	2	GND1	S	**Ground 1.** 0 V.
	3	GND2	S	**Ground 2.** 0 V.
	28	GND3	S	**Ground 3.** 0 V.
Misc	29	*n/c*	–	No internal connection.
	31	$\overline{\text{TEST}}$	DI[1]	**Test.** Reserved for factory testing. Tie High for normal operation.
	18	$\overline{\text{RESET}}$	DI[1]	**Reset.** Pulse Low to initialize internal circuits.
User Port	10	RDATA_ST	DO	**Receive Data Strobe.** RDATA_ST goes High for 18 consecutive BIT_CK periods to indicate four stuffing bits (b4703 - 4706) and 14 frame bits (b1-14) on RDATA.
	16	MODE	DI	**Mode Select.** When MODE is High, the Data Pump operates in Master mode so that it is the link timing source and initiates activation. When MODE is Low, the Data Pump operates in Slave mode. Tied to internal pull-up device. *The MDSP must be reset after the MODE is changed.*
	17	BIT_CK	DO	**Bit Rate Clock.** This clock transfers data into and out of the MDSL data interface at the bit rate. MSTR_CK is the source of BIT_CK in Master Mode. VCO_CK is the source of BIT_CK in Slave Mode.
	30	$\overline{\text{ACTIVE}}$	DO	**Link Active Indicator.** $\overline{\text{ACTIVE}}$ goes Low upon the receipt of two consecutive frame sync words. $\overline{\text{ACTIVE}}$ goes High when the frame sync word is not detected in six consecutive frames.
	8	RDATA	DO	**MDSL Receive Data Output.** When $\overline{\text{ACTIVE}}$ is Low, the receive data including frame sync and stuff bits are output on RDATA. RDATA is High when $\overline{\text{ACTIVE}}$ is High.
	7	RFP	DO	**Receive Frame Pulse.** Low for one BIT_CK cycle during the last bit of the current MDSL receive frame on RDATA, either b4702 or b4706. RFP is valid when $\overline{\text{ACTIVE}}$ is Low.
	11	TDATA	DI[1]	**MDSL Transmit Data Stream.** When $\overline{\text{ACTIVE}}$ is Low, the Data Pump samples data on TDATA except during frame sync and stuff bits.
	12	TFP	DI[1]	**Transmit Frame Pulse.** TFP should be Low for one BIT_CK cycle the during last bit of the current MDSL frame on TDATA. *If TFP is pulled Low and is Low again three BIT_CK cycles later, RDATA, RFP, RDATA_ST, BIT_CK, CK_EN, and $\overline{\text{ACTIVE}}$ will tri-state until the device is reset.* Tied to an internal pull-up device.

1. This input is a Schmidt Triggered circuit and includes an internal pull-up device.
2. The period is 2351 or 2353 baud times.
3. This input is a Schmidt Triggered circuit and includes an internal pull-down device.
4. I/O column entries: DI = Digital Input; DO = Digital Output; DI/O = Digital Input/Output; AI = Analog Input; AO = Analog Output; AI/O = Analog Input/Output; S = Supply.

Table 2: SK70720 MDSP Pin Assignments/Signal Descriptions – continued

Group	Pin#	Symbol	I/O[4]	Description
Hardware Interface *(Hardware Control Mode)*	4	QUIET	DI[3]	**Quiet Mode Enable.** Set High to force the MDSP into the Deactivated State. Set Low to enable activation requests (see ACTREQ).
	5	ACTREQ	DI[3]	**Activation Request (Master mode) (no function in Slave mode).** Tie this pin Low in Slave mode. When QUIET is Low, a rising edge on this pin initiates activation. The signal is ignored after activation (see QUIET).
	6	LOOPID	DI[3]/O	**Loop Number Input (Master mode) or Loop Number Indicator (Slave mode).** This indicator is transmitted from the link Master to the slave and can be used for loop identification in systems that multiplex data onto multiple MDSL lines. In Slave mode LOOPID is valid only when $\overline{\text{ACTIVE}}$ is Low.
	9	ACTVNG	DO	**Activating State Indication.** ACTVNG goes High when the MDSP is in the Activating State.
	32	TMR_EXP	DO	**Timer Expiration Indicator.** TMR_EXP goes High to indicate the expiration of the activation timer.
	33	$\overline{\text{CHIPSEL}}$	DI[3]	**Chip Select** — *Assert these three pins Low to activate Hardware Control Mode. When any of them is High, the MDSP reverts immediately to Software Control Mode.*
	34	$\overline{\text{WRITE}}$	DI[3]	**Write Pulse**
	35	$\overline{\text{READ}}$	DI[3]	**Read Pulse**
	36	LOS *(Master)*	DO	**Loss of Signal Indicator.** In Master mode, LOS goes High when the Data Pump enters the Inactive State. When the Data Pump reaches the Deactivated State from Active-1 or Active-2, it starts the Loss of Signal (LOS) timer after Slave transmission stops. When the LOS timer expires, the Data Pump goes to the Inactive State. When the Data Pump transitions from the Activating State directly to the Deactivated State, it may immediately enter the Inactive State without waiting for Slave transmission to cease. (See Figure 9.)
		LOS *(Slave)*	DO	**Loss of Signal Indicator.** In Slave mode, LOS goes High immediately when loss of signal energy is detected and the data pump enters the Inactive State. (See Figure 10.)
	37	DEACTVTD	DO	**Deactivation Indicator.** DEACTVTD goes High when the Deactivation timer expires and the data pump goes from the Pending Deactivation state to the Deactivated state.
	38	ILMT	DI[1]	**Insertion Loss Measurement Test.** Set High to transmit a framed & scrambled, "all 1s", 2B1Q pulse sequence. Pulse sequence will have a valid sync word. In the Slave configuration, when the ILMT mode is selected, the Data Pump may begin activation.
	39	RPTR	DI[1]	**Repeater Mode Enable.** When in Master mode, setting RPTR High configures the data pump to derive timing from the MSTR_CK output of an adjacent device for transparent repeater applications. The BIT_CK output phase is aligned to the TFP input pulse width. RPTR is ignored in Slave mode.

1. This input is a Schmidt Triggered circuit and includes an internal pull-up device.
2. The period is 2351 or 2353 baud times.
3. This input is a Schmidt Triggered circuit and includes an internal pull-down device.
4. I/O column entries: DI = Digital Input; DO = Digital Output; DI/O = Digital Input/Output; AI = Analog Input; AO = Analog Output; AI/O = Analog Input/Output; S = Supply.

Table 2: SK70720 MDSP Pin Assignments/Signal Descriptions – continued

Group	Pin #	Symbol	I/O[4]	Description
Hardware Interface *(Hardware Control Mode) -cont'd*	40	FELB	DI[1]	**Front-End Loopback (Master only).** In the Inactive State, set High to cause the IAFE to loopback. The returned signal activates the MDSP which receives its own transmitted data. The chip set ignores incoming data from the Slave during loopback.
	41	BELB	DI[1]	**Back-End Loopback.** In the Active-1 or Active-2 states, setting BELB High forces an internal, transparent loopback with RDATA connected to TDATA and RFP connected to TFP.
	42	RCLKU	DO	**Receive Baud Rate Clock.** Aligned with BIT_CK in Slave mode, phase synchronous with receive pulse stream, However, during Activating State, the clocks may not be aligned. In the Master mode RCLKU has a constant, arbitrary, phase relationship with BIT_CK in Active State.
	43	TXTST	DI[1]	**Transmit Test.** Set high to enable isolated transmit pulse generation. TDATA controls the sign and TFP controls the magnitude of the transmitted quat pulses according to the 2B1Q encoding rules. In the Slave configuration, when the TXTST mode is selected, the Data Pump may begin activation.
Processor Interface *(Software Control Mode)*	36	D0	DI[1]/O	**Data bit 0.** Eight-bit, parallel data bus.
	37	D1	DI[1]/O	**Data bit 1**
	38	D2	DI[1]/O	**Data bit 2**
	39	D3	DI[1]/O	**Data bit 3**
	40	D4	DI[1]/O	**Data bit 4**
	41	D5	DI[1]/O	**Data bit 5**
	42	D6	DI[1]/O	**Data bit 6**
	43	D7	DI[1]/O	**Data bit 7**
	4	ADDR0	DI[3]	**Address bit 0.** Four-bit address, selects read or write register.
	5	ADDR1	DI[3]	**Address bit 1**
	6	ADDR2	DI[3]	**Address bit 2**
	9	ADDR3	DI[3]	**Address bit 3**
	32	$\overline{\text{INT}}$	DO	**Interrupt Output.** Open drain output. Requires an external 10 kΩ pull up resistor. Goes Low on interrupt.
	33	$\overline{\text{CHIPSEL}}$	DI[3]	**Chip Select.** Pull Low to read or write to registers.
	34	$\overline{\text{WRITE}}$	DI[3]	**Write Pulse.** Pull Low to write to registers.
	35	$\overline{\text{READ}}$	DI[3]	**Read Pulse.** Pull Low to read from registers.

1. This input is a Schmidt Triggered circuit and includes an internal pull-up device.
2. The period is 2351 or 2353 baud times.
3. This input is a Schmidt Triggered circuit and includes an internal pull-down device.
4. I/O column entries: DI = Digital Input; DO = Digital Output; DI/O = Digital Input/Output; AI = Analog Input; AO = Analog Output; AI/O = Analog Input/Output; S = Supply.

Table 2: SK70720 MDSP Pin Assignments/Signal Descriptions – continued

Group	Pin#	Symbol	I/O[4]	Description
Clock and Control	14	SLAVE_CK	DI[3]	**Slave Mode Reference Clock.** Mandatory in Slave mode. Tie High or Low in Master Mode. Clock input requires ± 32 ppm accuracy.
	15	CK_EN	DO	**Slave Mode Reference Clock Enable.** Active High enable for the SLAVE_CK clock. In slave mode, this pin goes Low to indicate the PLL is tracking the input signal from the master. Not used in master mode.
	13	MSTR_CK	DI[1] DO	**16x MDSL Reference Clock.** In Master Mode, this clock generates transmit and receive timing and must have ±32 ppm accuracy. In Slave Mode, this output is derived by dividing VCO_CK by two so that it may drive the MSTR_CK input of another data pump configured for Master mode as a repeater (with RPTR High).
	19	VCO_CK	DI	**32x Receive Clock Input.**
	20	SER_CTL	DO	**Serial Control Output.**
	21	RX_CK	DO	**Receive Baud Rate Clock.** Derived from VCO_CK.
	22	AD0	DI	**Analog to Digital Converter Data Line 0.**
	23	AD1	DI	**Analog to Digital Converter Data Line 1.**
	24	AGC_SET	DI	**AGC Adjust Input.**
	25	TX_CK	DO	**Transmit Symbol Clock Output.**
	26	TMAG	DO	**Transmit Quat Magnitude Bit.**
	27	TSGN	DO	**Transmit Quat Sign Bit.**

1. This input is a Schmidt Triggered circuit and includes an internal pull-up device.
2. The period is 2351 or 2353 baud times.
3. This input is a Schmidt Triggered circuit and includes an internal pull-down device.
4. I/O column entries: DI = Digital Input; DO = Digital Output; DI/O = Digital Input/Output; AI = Analog Input; AO = Analog Output; AI/O = Analog Input/Output; S = Supply.

FUNCTIONAL DESCRIPTION

The MDSL Data Pump (MDP) provides synchronous, full duplex transmission on a single pair of wires using 2B1Q line coding and echo cancellation. The Data Pump supports symmetrical line rates from 272 to 784 kbps and provides complete start up and operation without an external processor. The MDP may be used to transport framed or unframed data which is synchronous, asynchronous, or near-synchronous to the clock rate of the data pump. This section provides an overview of how the MPD data interface functions to support these applications. For a detailed explanation on the how to configure the MPD for a specific application refer to the section entitled "MDSL Data Interface".

Figure 3 illustrates data transport using the MDSL system. Data is clocked into a transmitter, sent over the line, and clocked out of the receiver of the far-end transceiver. Data is transmitted simultaneously in both directions.

Framing

The MDP embeds a 14-bit frame synchronization word (FSW) in the data stream that divides the data into 4702-bit MDSL frames as shown in Figure 4. The framing signal serves three purposes:

1. It allows automatic activation and deactivation based on receiver frame sync word detection.
2. It allows the average data rate in each direction of transmission to be adjusted while maintaining a constant line rate.
3. It provides an MDSL frame position indicator that may be used in unframed time-division-multiplexed systems to relate time slots in the MDSL frame to those in an application frame. (See Note below)

NOTE

The MDP frame sync word format and frame length are fully compatible with those defined for 784 kbps HDSL applications in the ETSI ETR-152 and Committee T1 TR-28 technical reports. However, the MPD is fully transparent to all data except the frame sync word, so it does not impose the other framing functions defined for HDSL.

Each frame contains 4688 payload data bits, and there are no restrictions on the data patterns which can be transmitted in the payload data. The application synchronizes data to the MDP framing by generating a pulse on the transmit frame pulse input, TFP. The transmitter sends the FSW in the first 14 bits following the rising edge of TFP. Application data is not transmitted or buffered during the transmission of the FSW.

Figure 3: MDSL System Data Transport

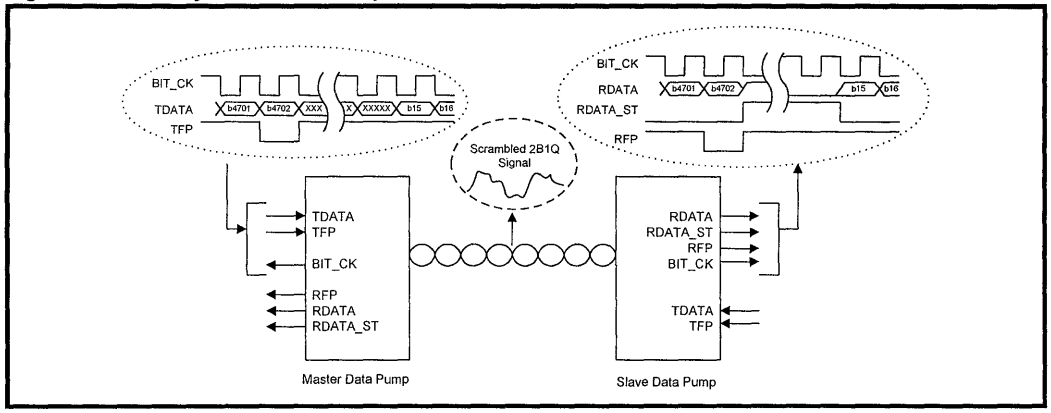
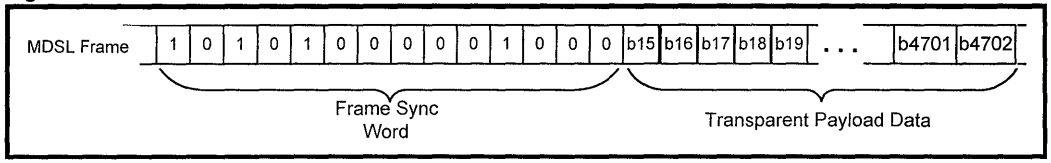


Figure 4: MDSL Frame



The MDP receiver detects the incoming FSW and provides a blanking signal (RDATA_ST) at its output to indicate that payload data is not present during the FSW. The RDATA_ST signal can also be used to gate the receiver clock signal (BIT_CK) so that clock transitions are present only when payload data is available. The resulting gapped clock is similar to that found in many other data transport systems.

The MDP has two modes of operation: Fixed Data Rate and Variable Data Rate.

Fixed Data Rate Mode

In Fixed Data Rate Mode, the MDP transports one data bit for each cycle of the bit clock (BIT_CK) except during the 14-bit FSW at the start of each frame. Data may be either synchronous (one data bit per available clock cycle) or asynchronous (data sent only when available). In both cases, the transmitter samples the transmit data signal (TDATA) on the rising edge of BIT_CK and reproduces that signal at the output of the receiver (RDATA) so that it is valid on the rising edge of the receiver BIT_CK. An external frame counter is required to provide a transmit frame pulse every 4702 BIT_CK cycles to synchronize the Data Pump frame position to the gapped data.

In applications where the data is formatted into logical frames or packets there is no requirement for a fixed mapping between the application frames and MDSL frames since the data contains the framing information required to give it meaning. Unless the application frame size divides evenly into the MDSL frame size, it is best to embed application framing information with the data rather than to create a fixed mapping between specific time slots in the MDSL and application frames. With unframed, time-division multiplexed data defined relative to an application frame pulse it is necessary to establish a fixed mapping between application frame and MDSL frame boundaries.

Table 3 shows the payload data rate and frame length for some common values of line rates.

Table 3: Data Rate and Frame Length Examples

Line Rate (kbps)	Payload Data Rate (kbps)	Frame Length (ms)
272	271.190	17.287
400	398.809	11.755
528	526.428	8.905
784	781.666	5.997

Variable Data Rate Mode

Some applications require that data be transported at a rate which is externally controlled and varies a small amount from a nominal payload data rate. The MDP has a variable rate operating mode which allows the application to modify the payload data rate without changing the line rate so that each of the payload bits contains a valid data bit. To operate in this mode, the MDP uses a mechanism known as stuffing. By properly choosing the line rate of the MDSL system and using the stuffing mechanism, the application can transmit data at slightly different rates in both directions simultaneously while still using a common, fixed MDSL line rate.

When stuffing is employed, the application inserts an additional four bits not carrying payload data in the data stream between the end of the 4688 payload bits and the beginning of the next FSW as shown in Figure 5. This is accomplished by delaying the TFP pulse by four BIT_CK periods from its normal position. The MDP receiver detects this four bit change in the location of the FSW and adjusts its payload data strobe indicator (RDATA_ST) to indicate that the four additional bits do not contain payload data and should be suppressed along with the FSW which follows them. This mode of operation is frequently used in the transport of T1 signals where the upstream data rate is not identical to the downstream data rate.

Figure 5: Variable Data Rate Mode Framing

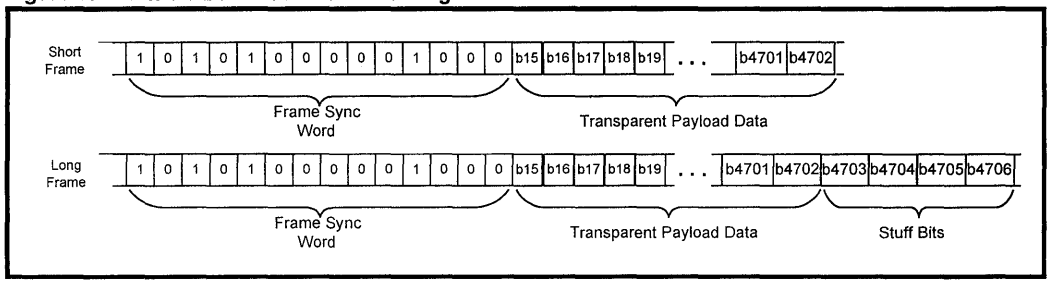


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Table 4 provides the minimum and maximum data rates and frame times for several line rates. Although the MDP can only transport data at either of these two instantaneous rates, it can support any average data rate between them by adjusting the ratio of frames with stuffing to those without stuffing. When 50% stuffing is used the MDP will transport data at the nominal rate shown below. If necessary, a PLL tracking the receive frame pulse output (RFP) can be used to create a continuous (i.e., not gapped) clock whose frequency follows the average receive data rate.

Component Description

The following paragraphs describe the chip set components individually with reference to internal functions and the interfaces between Data Pump components.

Integrated Analog Front End (IAFE)

The IAFE incorporates the following analog functions:

- the transmit driver
- transmit and receive filters
- Phase-Locked Loop (PLL)
- hybrid circuitry analog-to-digital converter.

The IAFE provides the complete analog front end for the MDSL Data Pump. It includes transmit pulse shaping, line driver, receive A/D modulator, and the VCO portion of the receiver PLL function. Transmit and receive controls are implemented through the serial port. The IAFE line interface uses a single twisted pair line for both transmit and receive. Table 5 lists the IAFE pin descriptions. Refer to Test Specifications for IAFE electrical and timing specifications.

IAFE Transmitter

The IAFE performs the pulse shaping and driving functions. The IAFE transmitter generates a 4-level output of 1/(8*f(TX_CK)) defined by TMAG and TSGN. Table 5 lists 2B1Q pulse coding parameters. Refer to Test Specifications for frequency and voltage templates.

IAFE Receiver

The IAFE receiver is a sophisticated sigma-delta converter. It sums the differential signal at RTIP/RRING minus the signal at BTIP/BRING. The first A/D signal comes out of AD0 at the rate of 64 times the 2B1Q symbol rate. The second stage of the A/D samples the noise of the first and generates the AD1 bit stream at the rate of 64 times the symbol rate.

Receiver gain is controlled by the MDSP via the AGC2-0 bits in the SER_CTL serial control stream. The AGC_SET output from the IAFE is normally Low. It goes High when the signal level in the sigma delta A/D is approaching its clipping level, signaling the MDSP to lower the gain.

The VCO is part of a phase-locked loop (PLL) locked to the receive data. The VCO frequency is varied by pulling an external crystal with varactor diodes that are biased by the VPLL output. The VPLL output is, in turn, controlled by the serial port PLL bits.

MDSL Digital Signal Processor (MDSP)

The MDSP incorporates the following digital functions:

- bit-rate transmit and receive signal-processing
- adaptive Echo-Cancelling (EC)
- adaptive decision feedback-equalization (DFE) using the receive quat stream and the internal error signal
- fixed and adaptive digital-filtering functions
- activation/start-up control and the microprocessor interface

The MDSP also provides the digital data interface. A simple, parallel 8-bit microprocessor interface on the MDSP allows high-speed access to control, status and filter coefficient words. Table 6 lists the MDSP pin descriptions. Refer to Test Specifications for MDSP electrical and timing specifications.

The microprocessor interface on the MDSP provides bit flags for signal presence, synchronization, activation completion. Single-byte words representing receive signal level and the noise margin of the transceiver are also available on the microprocessor interface. One control bit allows the user to start the Data Pump activation sequence. The MDSP controls the complete activation/start-up sequence.

Table 4: Minimum and Maximum Data Rate/Frame Time Examples

Line Rate (kbps)	Frame Length (ms) 4702 bit Frame	Frame Length (ms) 4706 bit Frame	Min. Payload Data Rate (kbps)	Nominal Rate (kbps) (50% stuffing)	Max. Payload Data Rate (kbps)
272	17.287	17.301	270.960	271.075	271.190
400	11.755	11.765	398.470	397.453	398.809
528	8.905	8.913	525.980	524.637	526.428
784	5.997	6.003	781.001	779.007	781.666

Table 5: IAFE Transmit Control

TSGN	TMAG	Output Symbol (quat)
1	0	+3
1	1	+1
0	1	-1
0	0	-3

MDSP/IAFE Interface

The IAFE provides the receiver recovered clock, VCO_CK, to the MDSP. The serial control stream framing signal RX_CK is sampled inside the IAFE with the VCO_CK rising edge. The serial control stream, SER_CTL, is sampled inside the IAFE by the rising edge of an internally-generated clock at f(VCO_CK)/2. This IAFE internal clock has the same phase relationship with a similar clock inside the MDSP, as established by the RX_CK signal. In the MDSP, the half-rate clock VCO_CK/2 and RX_CK transition on the rising edge of VCO_CK, and SER_CTL transitions coincide with the falling edge of VCO_CK/2. The output MSTR_CK in Slave Mode is equal to VCO_CK/2.

The A/D converter outputs, AD0 and AD1, are clocked out of the IAFE with VCO_CK, having transitions coincidental with the rising edge of VCO_CK/2. The MDSP samples AD0 and AD1 with the falling edge of its internal VCO_CK/2.

Transmit data, represented by TSGN and TMAG, is clocked from the MDSP using the falling edge of TX_CK, the transmit clock. The IAFE uses the rising edge of TX_CK to sample TSGN and TMAG. TSGN and TMAG change state at the baud rate, or every 8 cycles of TX_CK. Figure 6 shows relative timing for the MDSP/IAFE interface.

MDSP/IAFE Serial Port

The MDSP continually writes to the IAFE serial port. This serial stream consists of two 16-bit words as shown in Table 6. The data flows from the MDSP to the IAFE at a rate of f(VCO_CK)/2. Refer to the Test Specifications section for serial port timing relationships and electrical parameters.

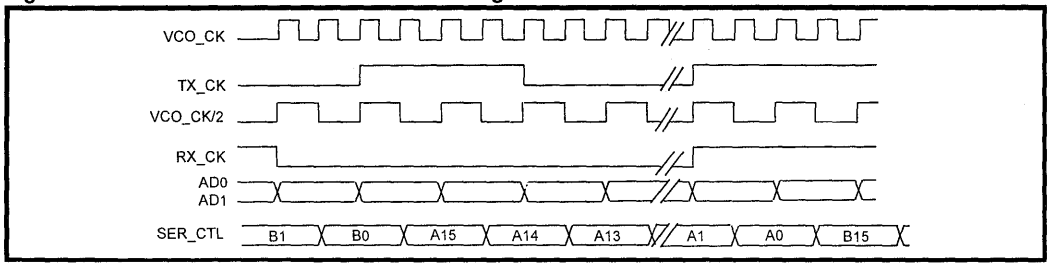
Line Interface

The Data Pump line interface consists of three differential pairs. The transmit outputs TTIP and TRING, receive inputs RTIP and RRING, and the balance inputs BTIP and BRING, all connect through a common transformer to a single twisted-pair line (see Figures 13 and 14). The transmit outputs require resistors in series with the transformer. A passive prefilter is required for the receive inputs. The balance inputs feed the transmit signals back to the Data Pump providing passive echo cancellation. Protection circuitry should be inserted between all Data Pump line interface pins and the transformer. Refer to the Applications section for typical schematics.

Table 6: MDSP/IAFE Serial Port Word Bit Definitions (See Figure 6)

Bit	Word A (on SER_CTL)	Word B (on SER_CTL)
15	INIT	COR4
14	*n/a*	COR3
13	*n/a*	COR2
12	TXOFF	COR1
11	TXDIS	COR0
10	TXTST	VCO2
9	AGC2	VCO1
8	AGC1	VCO0
7	AGC0	PLL7
6	FELB	PLL6
5	*n/a*	PLL5
4	PTR4	PLL4
3	PTR3	PLL3
2	PTR2	PLL2
1	PTR1	PLL1
0	PTR0	PLL0

Figure 6: MDSP/IAFE Interface – Relative Timing



MDSL Data Interface

The "Functional Description" section of this data sheet presents an overview of data transport in an MDSL system. This section provides detailed information on the operation of the data interface and how it is configured to support variable data rate and fixed data rate applications.

Clock Distribution

Figure 7 shows an MDSL link between a master and slave transceiver. This figure illustrates the clock/timing architecture of the data pump in both modes. Link activation is initiated by the master mode device which also operates as the MDSL timing source. The slave mode device responds to an activation request and is "loop-timed" (i.e., it recovers the MDSL clock from the master and uses this clock to transmit upstream).

In the master mode, the data pump derives its line transmit clock and data interface BIT_CK by dividing the clock supplied at the MSTR_CK input by 16. MSTR_CK also provides a ±32 ppm accurate local training reference for the receiver clock recovery VCXO before activation. When active, the master data pump uses this VCXO in a PLL for data recovery from the line, but an internal FIFO is provided so that the receive data can be clocked out using the BIT_CK divided down from the MSTR_CK.

In the slave mode after activation, the data pump derives its line transmit clock and data interface BIT_CK from the receiver PLL. In this mode, the clock supplied at the SLAVE_CK input is only used to train the VCXO frequency within ±32 ppm before activation. To minimize switching noise, the SLAVE_CK can be turned off when CK_EN is Low.

To select the clock and crystal frequencies required for a specific application, the required line rate must first be calculated from the specified payload data rate. This process is outlined below for fixed data rate and variable data rate configurations.

Fixed Data Rate Operation

For fixed data rate operation, the line rate is calculated from the payload data rate as follows:

line_rate = data_rate (4702/4688).

The time required to transmit a complete frame is:

frame_time = 4702 / line_rate.

The Master transceiver requires a clock whose frequency is:

MSTR_CK = 16 (line_rate).

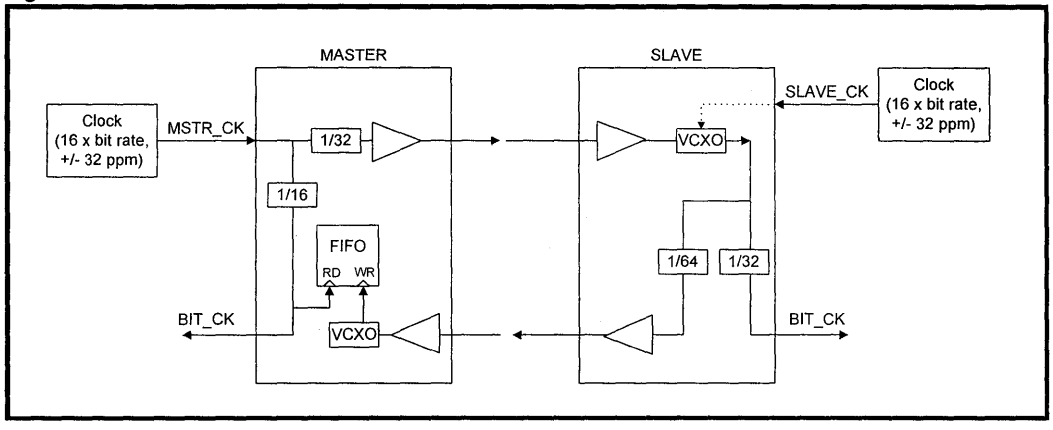
The slave transceiver requires a clock whose frequency is:

SLAVE_CK = 16 (line_rate).

Both transceivers require a VCXO crystal whose frequency is:

fxtal = 32 (line_rate).

Figure 7: MDSL Clock Distribution In Master and Slave Modes



Variable Data Rate Operation

For variable data rate operation, the line rate is calculated from the payload data rate as shown below:

line_rate = average_data_rate (4704/4688)

At this line rate the data pump will transport data at the specified average data rate when 50% stuffing is used, however it will always operate at one of the instantaneous data rates given by the following two equations. By adjusting the number of BIT_CK cycles between TFP pulses an external controller may adjust the frame length to control the average data rate between the minimum and maximum instantaneous rates:

max_data_rate = line_rate (4688/4702), and
min_data_rate = line_rate (4688/4706).

The time required to transmit a complete frame is:

frame_time (min) = 4702 / line_rate, or
frame_time (max) = 4706 / line_rate.

The Master transceiver requires a clock whose frequency is:

MSTR_CK = 16 (line_rate).

The slave transceiver requires a clock whose frequency is:

SLAVE_CK = 16 (line_rate).

Both transceivers require a VCXO crystal whose frequency is:

fxtal = 32 (line_rate).

Data Interface Timing

The MDSL data interface provides for the transfer of binary data to and from the transceiver using the 272 to 784 kHz clock, BIT_CK, generated by data pump. Figure 8 shows the timing for the data interface. In the receive direction, the binary data output on RDATA contains the 14-bit frame sync word (b1-b14), the transparent payload data (b15-b4702) and optional stuff bits (b4703-b4706). During the activation process, RDATA is held High until $\overline{\text{ACTIVE}}$ goes Low to indicate link activation has been completed and recovered data is available. The data strobe signal RDATA_ST is High during the frame sync word and stuff bits and Low during payload data. RDATA_ST can be used to create a gapped receive payload data clock by suppressing BIT_CK cycles when RDATA_ST is High. RFP is the receive frame sync output that goes Low during the first bit of every MDSL frame. In variable data rate applications the original data timing can be recovered from RFP using a synthesizer PLL.

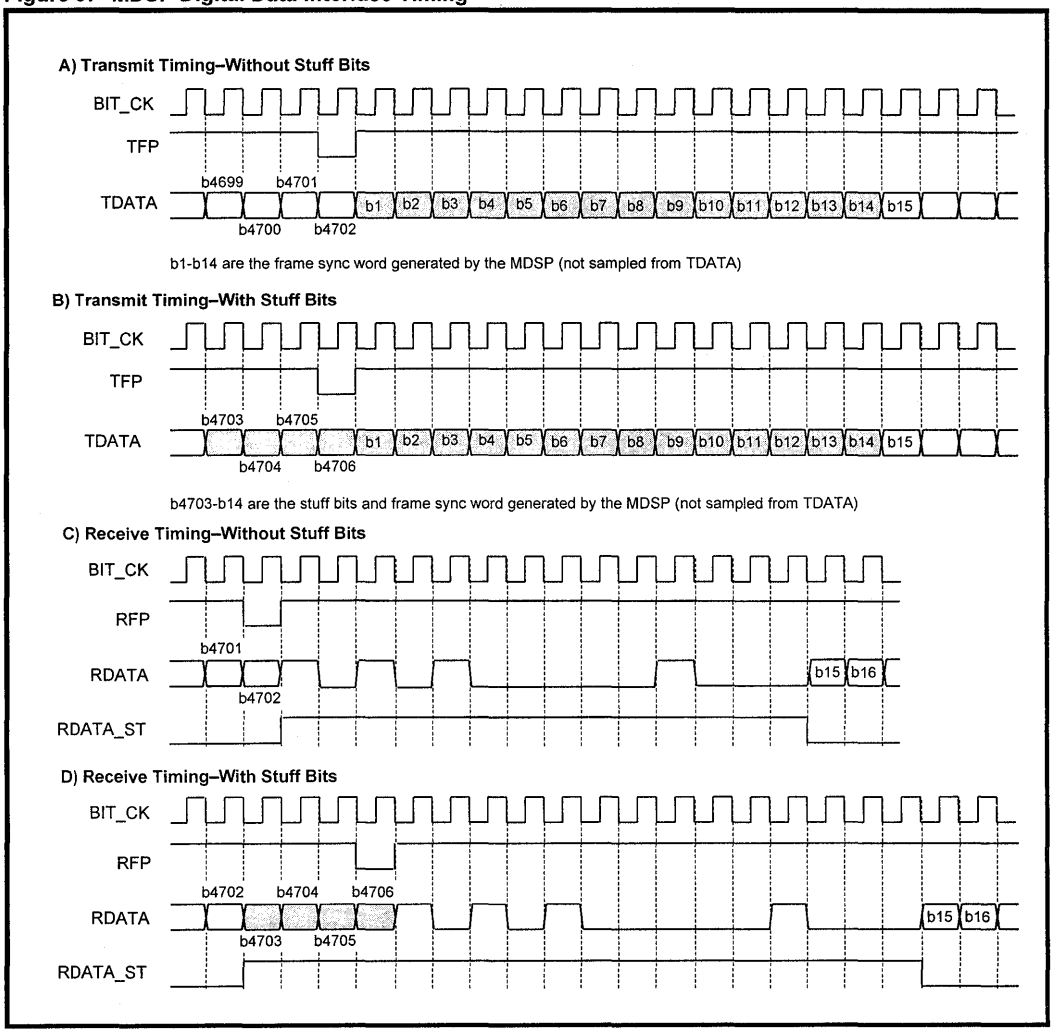
In the transmit direction, payload data is sampled from TDATA during bits b15-b4702 of each frame. Frame sync word bits (b1-b14) are internally generated in the MDSP and not sampled from TDATA, so any data supplied during b1-b14 is ignored. During the activation process, transmit data is internally generated by the MDSP and TDATA is not sampled until $\overline{\text{ACTIVE}}$ goes Low to indicate link activation has been completed. For fixed data rate applications an external counter is used to generate a one BIT_CK cycle long Low pulse for the TFP input. This frame sync pulse establishes the start of an MDSL frame and is needed to establish a gap in the payload data during the time the data pump internally generates the frame sync word. In variable rate applications stuffing control logic adjusts the time between TFP pulses to match the average data rate transmitted by the data pump to the rate at which it is supplied by the external source. In both cases, the TFP signal should be valid prior to an activation request for the Master Data Pump. A valid TFP signal should be generated after power-up, before or immediately after LOS goes Low for the Slave Data Pump. During initialization and anytime thereafter TFP must not be held low for more than 2 BIT_CK cycles or the data interface output signals will be disabled. Also, if the TFP signal is inactive (always High or unconnected) when activation starts, then the Data Pump may activate but will inject stuff bits in the TDATA stream in every other frame and sync bits in every frame. Since the Data Pump will not be synchronized to the data source these internally generated bits will overwrite payload data. If the phase of TFP jumps the Data Pump will immediately reset the transmit frame alignment, typically causing loss of alignment at the other end.

Loopbacks

The data pump provides data loopbacks toward the line and toward the digital interface. Front End Loopback (FELB) is the loopback toward the digital interface inside the IAFE and is available only in Master mode. FELB is initiated by bringing the FELB and ACTREQ signals High in hardware mode, or by setting the FELB and ACTREQ bits to 1 in the processor control mode. In FELB the data pump receiver activates with its own transmit data and ignores a signal at the IAFE receiver analog line interface. Data is transmitted on the line during FELB.

Back End Loopback (BELB) is a data loopback toward the analog line interface inside the MDSP. BELB is available in both Master and Slave modes after activation is complete. BELB is initiated by bringing the BELB signal High in hardware mode, or by setting the BELB bit to 1 in the processor control mode. In BELB the data pump receive data and frame pulse signals are supplied to the transmitter which ignores the TDATA and TFP inputs. Receive Data is output on RDATA during BELB.

Figure 8: MDSP Digital Data Interface Timing



Microprocessor Interface (MDSP)

Three primary control pins, $\overline{\text{CHIPSEL}}$ (Chip Select), $\overline{\text{READ}}$ and $\overline{\text{WRITE}}$, select the Software Mode which also uses an interrupt output pin to report status changes. Four additional pins are used for the parallel bus addressing and eight pins for data I/O. Refer to Test Specifications for microprocessor interface timing in Software Mode.

Control Pins

Chip Select: The Chip Select ($\overline{\text{CHIPSEL}}$) pin requires an active Low signal to enable Data Pump read or write transfers over the data bus. To enable Hardware Mode hold this pin Low, along with $\overline{\text{READ}}$ and $\overline{\text{WRITE}}$.

Data Read: The Data Read pin ($\overline{\text{READ}}$) requires an active Low pulse to enable a read transfer on the data bus. When $\overline{\text{READ}}$ is pulled Low, the Data Pump data bus lines go from tristate to active and output the data from the register addressed by ADDR0-ADDR3. To avoid reading data during register updates, reads should be synchronized to the falling edge of RX_CK. Alternatively, each read should be repeated until the same data is read twice within one baud time.

Data Write: The Data Write pin ($\overline{\text{WRITE}}$) requires an active Low pulse to enable a write transfer on the data bus. Data transfer is triggered by the rising edge of the $\overline{\text{WRITE}}$ pulse. To ensure data is written to the register addressed by ADDR0-ADDR3, valid data must be present on the MDSP data bus lines before $\overline{\text{WRITE}}$ goes High.

Interrupt: The Interrupt pin ($\overline{\text{INT}}$) is an open drain output requiring an external pull-up resistor. The $\overline{\text{INT}}$ output is pulled active Low when an internal interrupt condition occurs. $\overline{\text{INT}}$ is latched and held until Main Status Register RD0 is read. An internal interruption results from a Low-to-High transition in any of four status indicators: ACTIVE, $\overline{\text{ACTIVE}}$, DEACTVTD or TMR_EXP. Any transition on LOS will also generate an interrupt. If an interrupt mask bit in register WR2 is set, any transition of the corresponding status bit will not trigger the $\overline{\text{INT}}$ output.

Register Access

Write

To write to an MDSP register, proceed as follows:

1. Drive $\overline{\text{CHIPSEL}}$ Low.
2. Drive an address (0000, 0010, or 0011) onto ADDR0-ADDR3.
3. Observe address setup time.
4. Set 8-bit input data word on D0-D7.
5. Pull $\overline{\text{WRITE}}$ Low, observing minimum pulse width.
6. Pull $\overline{\text{WRITE}}$ High, observing hold time for data and address lines.

Read

Procedures for reading the MDSP registers vary according to which register is being read. Accessing registers RD0, RD1, RD2, RD5 and RD6 is relatively simple. Reading registers RD3 and RD4 is more complex. *Unless parallel port reads are synchronized with the falling edge of RX_CK, all read operations should be repeated until the same data is read twice within one baud time.*

To read register RD0, RD1, RD2, RD5 or RD6 proceed as follows:

1. Drive $\overline{\text{CHIPSEL}}$ Low.
2. Drive the desired address onto ADDR0-ADDR3.
3. Pull $\overline{\text{READ}}$ Low, observing minimum pulse width.
4. Pull $\overline{\text{READ}}$ High to complete the read cycle.

Registers RD3 and RD4 hold the coefficient values from the DFE, EC, FFE and AGC as shown in Table 10. Register RD3 holds the lower byte value and register RD4 holds the upper byte value. To reconstruct the complete 16-bit word, concatenate the least significant and most significant bytes.

To read registers RD3 and RD4 proceed as follows:

1. Select the desired coefficient by writing the appropriate code from Table 10 to register WR3.
2. Enable the Coefficient Read Register by writing a 1 to bit b0 (CRD1) in register WR2.
3. Perform standard register read procedure listed in steps 1 through 6 above to read the lower byte from RD3 and the upper byte from RD4.
4. Concatenate the RD3 and RD4 to obtain the complete 16-bit word.

Registers

Three write registers and seven read registers are available to the user. Table 7 lists these registers and the following paragraphs describe them in more detail.

Some of the registers contain *reserved* bits. Software must deal correctly with reserved fields. For reads, software must use appropriate masks to extract the defined bits and not rely on reserved bits being any particular value. In some cases, software must program reserved bit positions to a particular value. This value is defined in the individual bit descriptions.

After asserting the $\overline{\text{RESET}}$ signal, the Data Pump initializes its registers to the default value.

Table 7: Register Summary

ADDR	Write Registers			Read Registers		
A3-A0	WR#	Name	Table	RD#	Name	Table
0000	WR0	Main Control	8	RD0	Main Status	11
0001		*reserved*	*n/a*	RD1	Receiver Gain Word	12
0010	WR2	Interrupt Mask	9	RD2	Noise Margin	13
0011	WR3	Read Coefficient Select	10	RD3	Coefficient Read Register (lower byte)	14
0100		*reserved*		RD4	Coefficient Read Register (upper byte)	14
0101		*reserved*		RD5	Activation Status	15
0110		*reserved*		RD6	Receiver AGC and FFE Step Gain	16
0111-1001		*reserved*			*reserved*	

WR0—Main Control Register

Address: A<3:0> = 0000
Default 00h
Attributes: Write Only
Control Register bits serve the same purpose in Software Mode as the like-named individual pins in Hardware Mode. Table 8 lists bit assignments for the WR0 register.

Table 8: Main Control Register WR0

Bit	Description
7	**Transmit Test Pattern Enable (TXTST).** Set TXTST to 1 to enable isolated transmit pulse generation. One symbol is output every 4702 or 4706 BIT_CK cycles. TDATA controls the sign and TFP controls the magnitude of the transmitted symbols according to the 2B1Q encoding rules. In the Slave mode when the TXTST mode is selected, the Data Pump may begin activation.
6	**Back-End Loop Back (BELB).** In the Active State, set BELB to 1 to enable an internal, transparent loopback of the MDSP RDATA to TDATA and RFP to TFP.
5	**Front End Loop Back (FELB).** In the Master mode with the Data Pump in the Inactive State, set FELB to 1 to enable an IAFE front-end loopback. The Data Pump will begin activation and transmission on the line, but will ignore any signal from the Slave instead synchronizing to its own transmit signal.
4	**Repeater Mode (RPTR).** The RPTR bit is set to 1 and the MODE pin is pulled High to program the Data Pump for operation on the side of the MDSL repeater driving a remote slave. RPTR is set to 0 and the Master pin is tied Low to program the Data Pump for operation on the side of the repeater driven by the Master.
3	**Loop Number (LOOPID).** In two loop MDSL applications, LOOPID is set at the Master end of the loop to select the frame sync word format to encode the loop number.
2	**Insertion Loss Measurement Test (ILMT).** Set ILMT to 1 to enable transmission of a scrambled all ones insertion loss measurement test pattern. In the Slave configuration when the ILMT mode is selected, the Data Pump may begin activation.
1	**Quiet Mode (QUIET).** Set QUIET to 1 to force the Data Pump into the Deactivated State with the transmitter silent. Setting QUIET to 0 will not cause the Data Pump to reactivate. In the Slave mode, the Data Pump will not respond to a signal from the Master when QUIET is set to 1, but may activate after QUIET is set to 0 even if the Master transmission has already ceased.
0	**Activation Request (ACTREQ).** In the Master mode when the Data Pump is in the Inactive State and Quiet is set to 0, setting the ACTREQ bit to 1 will initiate an activation sequence. Because ACTREQ is a level- rather than an edge-triggered signal, it should be reset to 0 again within approximately 25 seconds to prevent the immediate start of another activation cycle if the current activation attempt fails. If an activation attempt fails, the processor should allow the Data Pump to remain in the Inactive State where the transmitter is silent for the Activation Timer duration (see Table 17) before generating another activation request. This delay will allow the Slave to return to the Inactive State. It is possible to shorten this quiet period following a failed activation by implementing additional algorithms described in the section entitled "Activation State Machines."

WR2—Interrupt Mask Register

Address: A<3:0> = 0010
Default: 00h
Attributes: Write Only
Table 9 shows the various interrupt masks provided in register WR2.

Table 9: Interrupt Mask Register WR2

Bit	Description
7:6	***Reserved.*** *Must be set to 0.*
5	**LOSMSK.** 1=Masked. 0=Not Masked. Interrupt mask for the LOS condition
4	**DEACTMSK.** 1=Masked. 0=Not Masked. Interrupt mask for the DEACTVTD condition
3	**ACTBMSK.** 1=Masked. 0=Not Masked. Interrupt mask for the $\overline{\text{ACTIVE}}$ condition
2	**ACTMSK.** 1=Masked. 0=Not Masked. Interrupt mask for the TMR_EXP condition and the ACTIVE condition
1	***Reserved.*** *Must be set to 0.*
0	**Enable coefficient read register (CRD1).** 1=Enable. 0=Disable. Used in conjunction with WR3 for reading coefficient values.

WR3—Read Coefficient Select Register

Address: A<3:0> = 0011
Default: 00h
Attributes: Write Only
Table 10 lists the bit maps used to select the coefficient read from the MDSP.

Table 10: Read Coefficient Select Register WR3

Hex Value	Selected Registers	Description
00-07	DFE1-DFE8	DFE coefficients
08-0F	EC1-EC8	Echo Cancellation
10-15	FFE1-FFE6	FFE coefficients 1-6
16-19	*reserved*	
1A	AGC Tap	AGC Tap
1B-FF	*reserved*	

RD0—Main Status Register

Address: A<3:0> = 0000
Default: xxh (x=undefined)
Attributes: Read Only

Status Register bits serve the same purpose in Software Mode as the like-named individual pins in Hardware mode. Table 11 lists the bit assignments in this register.

Table 11: Main Status Register RD0

Bit	Active Description
7	**Timer Expiry (TMR_EXP).** Set to 1 to indicate Activation timer expiration. • Causes interrupt on changing from 0 to 1; masked by ACTMSK = 1. • Latched event; reset on read, with persistence while in the Active State.
6	**TIP/RING polarity reversed ($\overline{\text{INVERT}}$).** 0 = polarity reversal. Valid only in Active-1 or Active-2 states.
5	**Change Of Frame Alignment (COFA).** Indicates that re-acquisition of frame sync is in a different position with respect to the last frame position. Does not cause interrupt. Latched event; reset on read
4	**Loss Of Signal (Slave).** 1 = loss of line signal energy detected and entry into the Inactive state.
	Loss of Signal (Master). 1 = loss of signal for 1 second on entering Inactive State. • Causes interrupt on transitions from 0 to 1 or 1 to 0 that are masked by LOSMSK = 1. • LOS/LOS is not a latched event.
3	**Loop Number Control (LOOPID).** 0 = loop 1; 1 = loop 2. Valid only in Active States, 0 in all others
2	**Deactivation Indicator (DEACTVTD).** 1 = expiration of the Deactivation timer and the transition from the Pending Deactivation state to the Deactivated state. • Causes interrupt on changing from 0 to 1; masked when DEACTMSK = 1. • Latched event; reset on read; with persistence while in the Deactivated State.
1	**Link Active Indicator, ($\overline{\text{ACTIVE}}$), active Low.** 1 = entry into the Pending Deactivation state. • Causes interrupt on changing from 0 to 1; masked by ACTBMSK = 1. • Latched event; reset on read; with persistence while in the Pending Deactivation State.
0	**Link Active Indicator, (ACTIVE), active High.** 1 = Completion of layer 1 activation and entry into the Active-1 state. • Causes interrupt on changing from 0 to 1; masked by ACTMSK = 1. • Latched event; reset on read with persistence if still in the Active State.

RD1—Receiver Gain Word Register

Address: A<3:0> = 0001
Default: xxh (x=undefined)
Attributes: Read Only

The 8-bit word in this register is the eight most significant bits of the main FFE AGC tap, which, along with the AGC and DAGC values (RD6), represent the receiver gain required to compensate for line loss, and to normalize the receive 2B1Q pulses to a fixed threshold. Bit b7 (sign bit, always 0) is the MSB with bit b0 the LSB. The AGC tap value is determined as follows:

$$\text{AGC Tap} = \sum_{i=0}^{6} b_i * 2^{i-6}$$

Table 12: Receiver Gain Word Register

Bit	Description
7:0	**FFE AGC Tap Value** (eight most significant bits).

RD2—Noise Margin Register

Address: A<3:0> = 0010
Default: xxh (x=undefined)
Attributes: Read Only

The noise margin of the received signal is an input to the MDSL framer's Activation State Machine. The noise margin must reach a threshold level before the MDSL framer can transition to the fully Active State. The MDSP provides a calculated, logarithmic noise margin value used by the MDSL framer. This eight-bit word, stored in register RD2, is available every baud, although updated only every 64 baud. Table 13 shows the noise margin coding. To calculate the SNR, use this equation:

SNR =Noise Margin + 21.5 dB

Error propagation in the DFE and de-scrambler may introduce some fractional errors in this formula, however, the relationship between the SNR and the noise margin remains valid as long as the noise follows a Gaussian distribution.

Since the average period of the calculation is very short (64 bauds), the recommended procedure for evaluating transmission quality is to average at least 1000 samples.

Table 13: Noise Margin Register RD2
(Noise Margin Coding)

MSB							LSB	Noise
7	6	5	4	3	2	1	0	Margin[1]
0	0	1	1	0	1	0	1	+26.5
0	0	1	0	1	1	1	1	+23.5
0	0	1	0	1	0	1	1	+21.5
0	0	1	0	1	0	0	1	+20.5
0	0	1	0	0	1	1	1	+19.5
0	0	1	0	0	1	0	1	+18.5
0	0	1	0	0	1	0	0	+18.0
0	0	1	0	0	0	1	0	+17.0
0	0	1	0	0	0	0	0	+16.0
0	0	0	1	1	1	1	0	+15.0
0	0	0	1	1	1	0	0	+14.0
0	0	0	1	1	0	1	0	+13.0
0	0	0	1	1	0	0	0	+12.0
0	0	0	1	0	1	1	0	+11.0
0	0	0	1	0	1	0	0	+10.0
0	0	0	1	0	0	1	0	+9.0
0	0	0	1	0	0	0	0	+8.0
0	0	0	0	1	1	1	0	+7.0
0	0	0	0	1	1	0	0	+6.0
0	0	0	0	1	0	1	0	+5.0
0	0	0	0	1	0	0	0	+4.0
0	0	0	0	0	1	1	0	+3.0
0	0	0	0	0	1	0	0	+2.0
0	0	0	0	0	0	1	0	+1.0
0	0	0	0	0	0	0	0	0.0
1	1	1	1	1	1	1	0	-1.0
1	1	1	1	1	1	0	0	-2.0
1	1	1	1	1	0	1	0	-3.0
1	1	1	1	1	0	0	0	-4.0
1	1	1	1	0	1	1	0	-5.0
1	1	1	1	0	1	0	0	-6.0

1 Accuracy of noise margin is ±1 dB.

RD3 (LSB), RD4 (MSB)—Coefficient Read Register

Address: RD3 (A<3:0> = 0011)
RD4 (A<3:0> = 0100)
Default: xxh (x=undefined)
Attributes: Read Only
Coefficient Read Word (read from the MDSP) comes from the location configured in the Read Coefficient Select Register (WR3, Address A<3:0> = 0011). The MDSP updates this word on the rising edge of the receive clock, RX_CK. Read register RD3 is the lower byte, and RD4 is the upper byte.

Table 14: Coefficient Read Register

Bit	Description
7:0	**Coefficient Word Value.** RD3 contains the lower byte; RD4 the upper byte.

RD5—Activation Status Register

Address: A<3:0> = 0101
Default: xxh (x=undefined)
Attributes: Read Only
The ACT bits indicate the current state of the MDSP transceiver during the Activating State as listed in Table 15. (For any state other than the Activating State, the ACT bits will be "0000".)

Table 15: Activation Status Register RD5

ACT Bits 3:0	State in Master Mode	State in Slave Mode
0000	Inactive	Inactive
0001	Pre-AGC	Wait
0010	Pre-EC	AAGC
0011	SIGDET	EC
0100	AAGC	PLL1
0101	EC	PLL2
0110	PLL	4LVLDET
0111	4LVLDET	FRMDET
1000	FRMDET	–

RD6—Receive Step Gain Register

Address: A<3:0> = 0110
Default: xxh (x=undefined)
Attributes: Read Only

This 8-bit register represents AGC and FFE gain coefficients (GAGC and GFFE, respectively). Bit assignments are listed in Table 16. The approximate line loss (LL) can be determined using these values in the following equation:

$$LL = 20\log_{10}(GFFE * AGC\ tap) + GAGC + 28\ dB$$

GFFE corresponds to DAGC in the MDSP and GAGC is from the IAFE. Bits ST0-ST2 indicate the Data Pump activation states as shown in Figures 9 and 10 and Table 18.

Table 16: Receiver AGC and FFE Step Gain Register RD6

Bit	Description
7	**ST2.** Data Pump Activation State–bit 2
6	**ST1.** Data Pump Activation State–bit 1
5:4	**GFFE1, GFFE0.** Digital Gain Word–bit 1 and Digital Gain Word–bit 0. **Bits <5:4>GFFE Value** 00 $2^0 = 1$ 01 $2^1 = 2$ 10 $2^2 = 4$ 11 $2^3 = 8$
3	**ST0.** Data Pump Activation State–bit 0
2:0	**GAGC2-GAGC0.** Analog Gain Word–bit 2,1 and 0. **Bits <2:0>GAGC Value (dB)** 000 -12 001 -10 010 -8 011 -6 100 -4 101 -2 110 0 111 +2

Activation

The MDSL Data Pump integrates all logic required to manage link activation and deactivation. Figure 9 illustrates the Activation State Machine for the Master mode. Figure 10 illustrates the Slave mode state machine. In software mode, the ST*n* bits in Read Register 6 (ADDR 0110) show the current status of the state machine.

Master Mode Activation Sequence

When the Master Data Pump is powered up and reset is applied, the chip set is in the Inactive State as shown at the top of Figure 9. Starting at the Inactive State, the device progresses in a clockwise direction through the Activating, Active-1, Active-2, Pending Deactivation and Deactivated States. In the hardware mode when the Data Pump is in the Inactive State and the QUIET pin is Low, a Low-to-High transition on the ACTREQ pin initiates activation of the link (See Table 17). In the software mode when the Data Pump is in the Inactive State and the QUIET bit is set to 0, setting the ACTREQ bit to 1 initiates activation of the link. Because the ACTREQ control bit is level sensing, to generate a single request, ACTREQ should be set to 1 and then reset to 0 again before the Activation Timer period elapses.

During the Activating State, the echo canceller, equalizers and timing recovery circuits are all adapting during the simultaneous transmission and reception of the framed, scrambled-ones data transmitted first as a two-level code (S0) and then as a four-level code (S1). If the receive frame sync word is not detected in two consecutive frames before the activation timer expires the device moves to the Deactivated State and ceases transmission. After reaching the Deactivated state this way, it will then immediately transition to the Inactive State (setting LOS regardless of whether Slave transmission ended). The next activation request should not be generated for one activation timer period to allow the Slave to timeout, detect LOS and move from the Deactivated to the Inactive State. Microprocessor-based systems may reduce this time by resetting the Slave data pump from the Activating State when no Master signal is present.

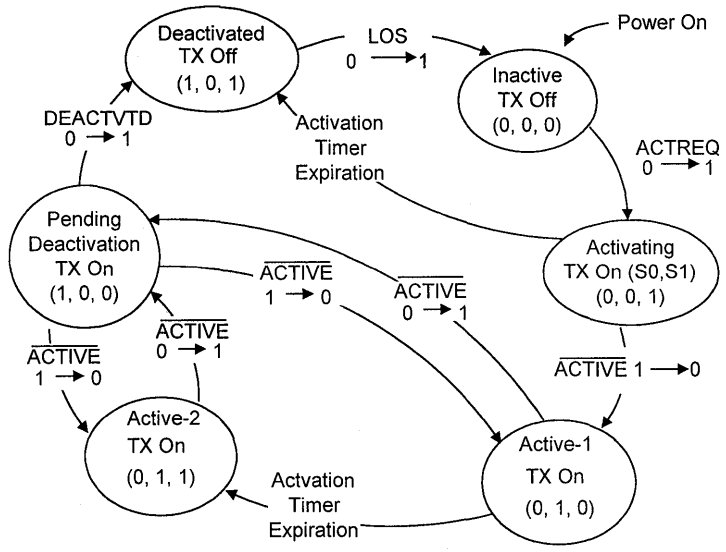
Successful detection of the sync word drives the State machine to the Active-1 State. This is indicated by a 0-to-1 transition of the ACTIVE bit or High to Low transition of the $\overline{\text{ACTIVE}}$ pin. If the Master Data Pump remains locked to the sync word until the activation timer expires, the device transitions to the Active-2 (fully active) State. If sync is lost, as indicated by a 0-to-1 transition on the $\overline{\text{ACTIVE}}$ pin, the Master Data Pump transitions to the Pending Deactivation State.

Table 17: State Machine Timer Durations (See Figures 9 and 10)

Timer	Nominal Timer Duration (seconds)				Description
	272 kbps	400 kbps	528 kbps	784 kbps	
Activation Timer[1]	86.5	59.0	44.5	30.0	**Master Mode**: Starts with an activation request. Restarts when a signal is detected from the Slave. **Slave Mode**: Starts when a signal is detected from the Master.
Deactivation Timer[2, 3]	6.0	4.0	3.0	2.0	Starts due to Loss of Sync Word for 6 consecutive frames, triggering the Pending Deactivation state.
LOS Timer[4]	3.0	2.0	1.5	1.0	**Master Mode**: Starts in Deactivated state once the Slave is quiet. **Slave Mode**: not used.
Delay required before next activation request	86.5	59.0	44.5	30.0	The amount of time the Master must be in the Inactive state before another activation request can be made after the Data Pump deactivates directly from the Activating State.

1. If time elapses and data pump has not moved to Active-1 state, the data pump enters the Deactivated State.
2. Pending Deactivation can be reached from either Active-1 or Active-2 states, if loss of sync word occurs for 6 frames.
3. If sync word detection does not occur before time elapses, the data pump deactivates.
4. When the data pump fails to activate in the Activating state, there is no waiting period in the Deactivated state; the data pump immediately goes Inactive.

Figure 9: Master Mode Activation State Machine



NOTE:
(n, n, n) indicates the status of bits ST2, ST1 and ST0 respectively.

In Pending Deactivation, the Master Data Pump progresses to the Deactivated and Inactive States with the expiration of the respective timers. If the sync word is detected before the Pending Deactivation timer expires, the Master Data Pump returns to either Active-1 or Active-2. (The Master Data Pump returns to which ever state it occupied before transitioning to Pending Deactivation.)

The Master Data Pump will exit the Active-2 State in one of two ways. A Low-to-High transition on the QUIET pin (Hardware Mode) or the QUIET bit (Software Mode), forces the Master Data Pump directly to the Deactivated State. The only other means of exiting the Active State is through a loss of receive sync word. $\overline{\text{ACTIVE}}$ goes Low when six consecutive frames occur without a sync word match sending the Master Data Pump into the Pending Deactivation State.

The Master Data Pump remains in the Pending Deactivation State for a maximum of two seconds. If a sync word is detected within the time limit, the Master Data Pump re-enters the Active State. If not, DEACTVTD goes High and the chip set goes to the Deactivated State. When the Deactivated State is reached from Pending Deactivation, the Master Data Pump returns to the Inactive State and declares LOS when it detects no signal from the Slave for one second. The Data Pump waits in the Inactive State before another activation attempt (See Table 17).

Slave Mode Activation Sequence

Figures 10 and 11 represent the Slave Data Pump Activation State Machine and the Slave MDSL Framer State Machine. The activation state machines for Slave and Master devices are similar. Both Data Pump machines start at the Inactive State and progress clockwise through the Activating, Active-1, Active-2, Pending Deactivation, and Deactivated States. One difference between them is in the initial condition required to exit from the Inactive State. The Master Data Pump responds to the Activation Request (ACTREQ) signal. The Slave device responds only to the presence of signal energy on the link. Thus, only an active Master device can bring up the link. Once the Master begins transmitting, the Slave device will automatically activate and attempt synchronization.

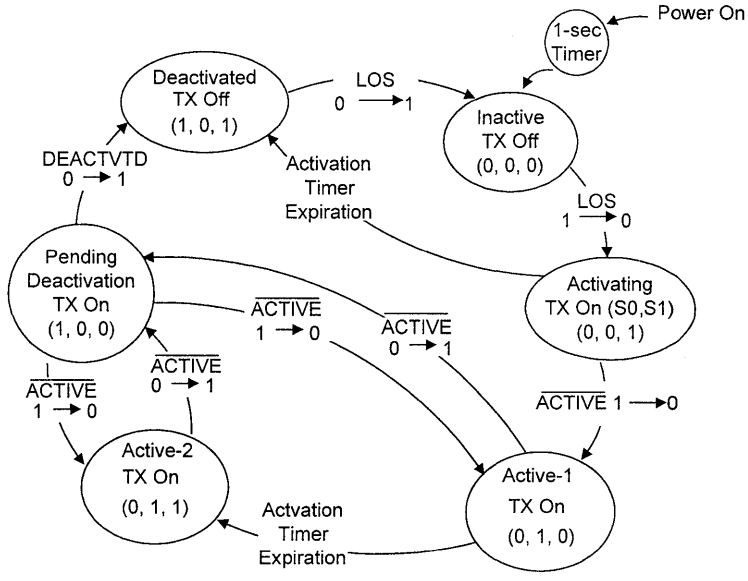
The other difference between the Data Pump state machines is the impetus for the change from the Deactivated to the Inactive State. In the Master Data Pump, expiration of a one-second loss of signal timer (after far end signal energy ceases) will cause the transition. In the Slave the transition occurs immediately on Loss of Signal (LOS).

Table 18: Data Pump Activation States

ST2	ST1	ST0	Data Pump State
0	0	0	Inactive
0	0	1	Activating – Activation timer running
0	1	0	Active – Activation timer running (Active-1)[1]
0	1	1	Active – Activation timer expired (Active-2)[1]
1	0	0	Pending Deactivation[1]
1	0	1	Deactivated
1	1	0	*unused*
1	1	1	*unused*

1. The data pump samples the TDATA input for all transmit data except the 14 sync bits at the start of each frame during states 010, 011 and 100.

Figure 10: Slave Mode Activation State Machine



NOTE:
(n, n, n) indicates the status of bits ST2, ST1 and ST0 respectively.

Synchronization State Machine

Figure 11 shows the MDSL Synchronization State Machine incorporated in the MDSP. It applies to both Master and Slave devices. Table 19 lists the correspondence between the Synchronization states and Activation states. The Sync state machine is clocked by the receive signal framing. Starting at the initial Out-of-Sync condition (State 0), the device progresses in a clockwise direction through State 1 until Sync is declared in State 2. Two consecutive frame sync word matches are required to achieve synchronization.

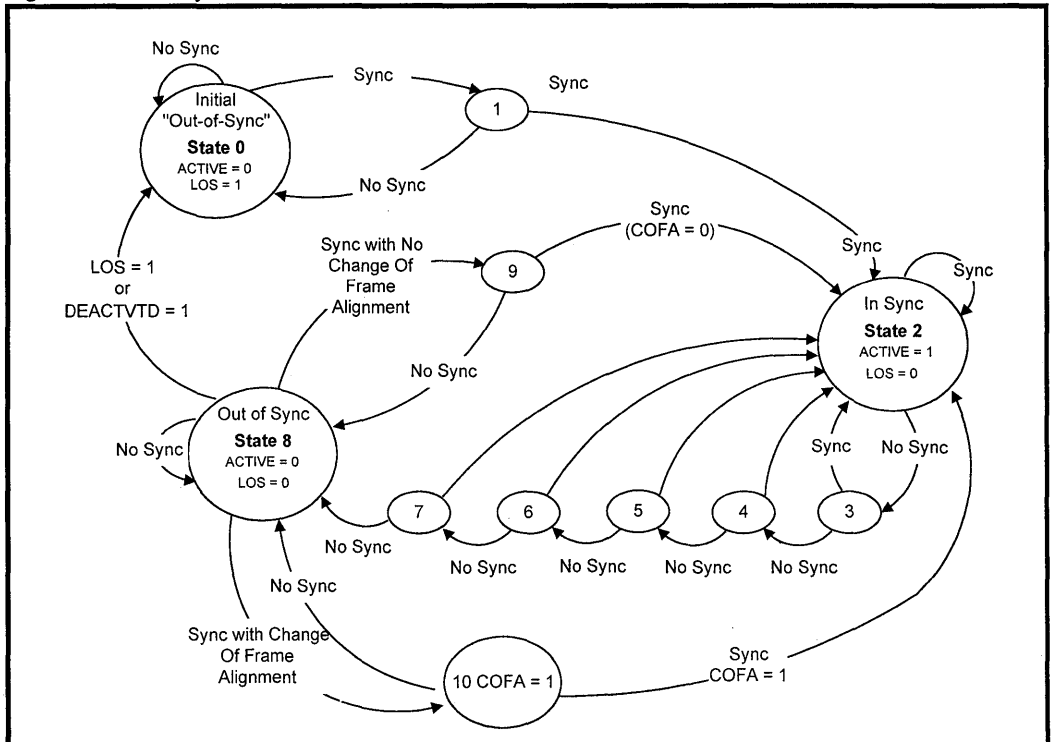
Once the In-Sync condition is declared, six consecutive frame sync mismatches will cause the device to transition through States 3 through 7 and declare an Out-of-Sync condition in State 8. From State 8, the device will return either to State 2 or to State 0. If the Pending Deactivation timer expires without re-establishing frame sync or if the receive signal energy is no longer detected, the device returns directly to State 0.

If frame sync is re-established, the device will return to the In-Sync condition (State 2) through State 9 if two consecutive frames are received without any change of frame alignment (COFA = 0). If a change of frame alignment does occur (COFA = 1), two consecutive matches are required to transition through State 10 back to State 2.

Table 19: Activation and Synchronization States

Activation State	Synchronization States
Inactive	State 0
Activating	State 1
Active	States 2, 3, 4, 5, 6, and 7
Pending Deactivation	States 8, 9, and 10

Figure 11: MDSL Synchronization State Machine



NOTES:
1. "Sync" = Frame Sync Word Match. "No Sync" = Frame Sync Word Mismatch.
2. A 0-to-1 transition on QUIET will set the Sync State Machine from any State to State 0.
3. Expiration of the Activation Timer will set the Sync State Machine from State 1 to State 0.

APPLICATION INFORMATION

PCB Layout

The following are general considerations for PCB layout using the MDSL Data Pump chip set:

- Refer to Figures 12, 13 and 14, and Table 20.
- Use a four-layer or more PCB layout, with embedded power and ground planes. Bring the digital power and ground planes down to include pins 1-6 and 24-28 of the IAFE.
- Break up the power and ground planes into the following regions. Tie these regions together at the common point where power connects to the circuit:
  - •Digital Region
  - •Analog Region
    - •VCXO subregion
    - •IAFE, Line I/F, and IBIAS subregion
- Use larger feedthroughs ("vias") and tracks for connecting the power and ground planes to the power and ground pins of the ICs than for signal connections. Place the decoupling capacitors right at the feedthrough power/ground plane ties, or on the tracks to the IC power/ground pins as close to the pins as possible.
- On the User Interface Connector, route digital signals to avoid proximity to the TIP, RING, and CT lines.
- Provide at least 100 µF or more of bulk power supply decoupling at the point where power is connected to the Data Pump circuit.

Digital Section

- Keep all digital traces separated from the analog region of the Data Pump layout.
- Provide high frequency decoupling capacitors (0.01 µF ceramic or monolithic) around the MDSP as shown in Figures 13 and 14. The capacitor on the MDSP VCC1 pin (pin 1) should be on the IC side of the
diode.
- It is possible to replace the NAND gate (shown in Figure 13) with an AND gate.

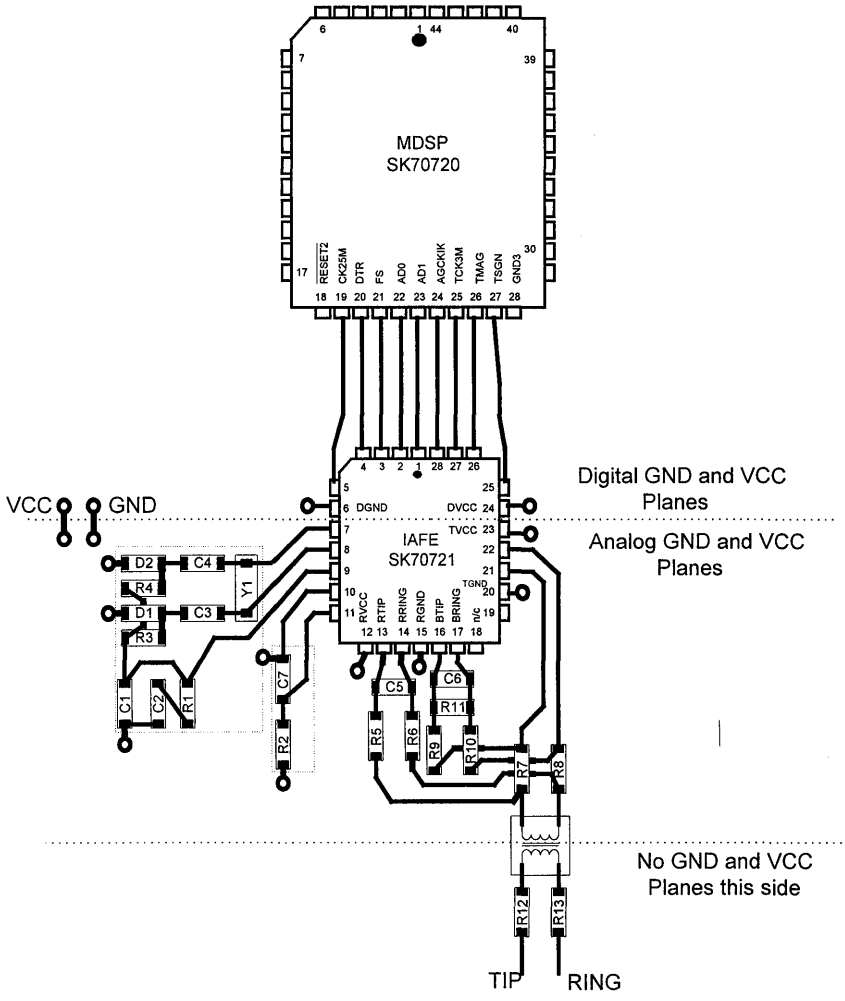
Analog Section

The analog section of the PCB consists of the following subsections:

1. IAFE and power supply decoupling capacitors
2. Bias Current Generator
3. Voltage Controlled Crystal Oscillator
4. Line Interface Circuit
   - Route digital signals AD0, AD1, RX_CK, SER_CTL, TSGN, TMAG, TX_CK, and AGC_SET on the solder side of the PCB, and route all analog signals on the component side as much as possible.
   - Route the following signal pairs as adjacent traces:
     - •TTIP/TRING
     - •BTIP/BRING
     - •RTIP/RRING

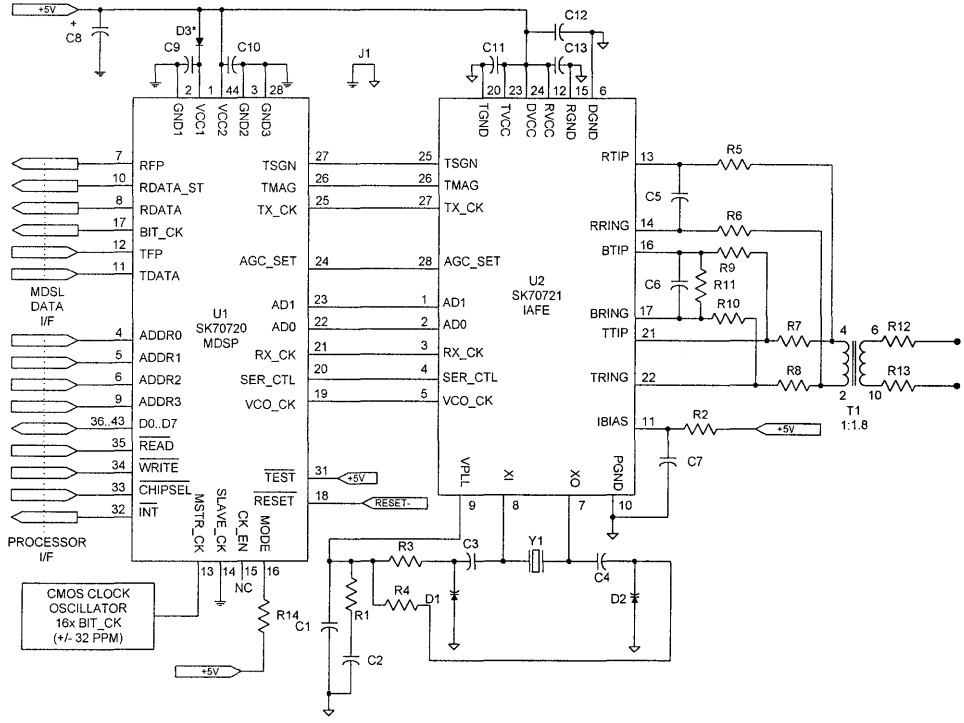
     but keep the pairs separated from each other as much as possible.
   - Do not run the analog ground plane under the transformer line side to maximize high voltage isolation.
   - The IAFE should be placed such that pin 1 is near pin 23 of the MDSP and pins 12-18 are near the edge of the PCB, with the line transformer and connector.

Figure 12: PCB Layout Guidelines



NOTE: The VCC and GND planes for Digital and Analog sides should be connected at a single point.

Figure 13: Typical Application for Master Mode Operation (Microprocessor Interface Mode)



NOTES:

Diode D3 is optional.

The MDSP and IAFE should have independent ground planes connected at a single point near pin 5 of the IAFE.

Table 20: Components for Suggested Circuitry (See Figures 13 and 14)

Ref	Description	Ref	Description	Ref	Description
C1, 9, 10	0.01 µF, ceramic, 10%	R1	5.11 kΩ, 1%	R12, 13	5.6 Ω, line feed fuse resistor (ALFR-2-5.6-1 IRC)
C2	100 µF, electrolytic, 20% low leakage ≤5 µA @ 25° C	R2	35.7 kΩ, 1%		
		R3, 4	20.0 kΩ, 1%	D1, 2	Varicap diode (Motorola MV209)
C3, 4	1000 pF, ceramic, 20%	R5, 6	499 Ω, 1%	D3	Silicon rectifier diode (1N4001)

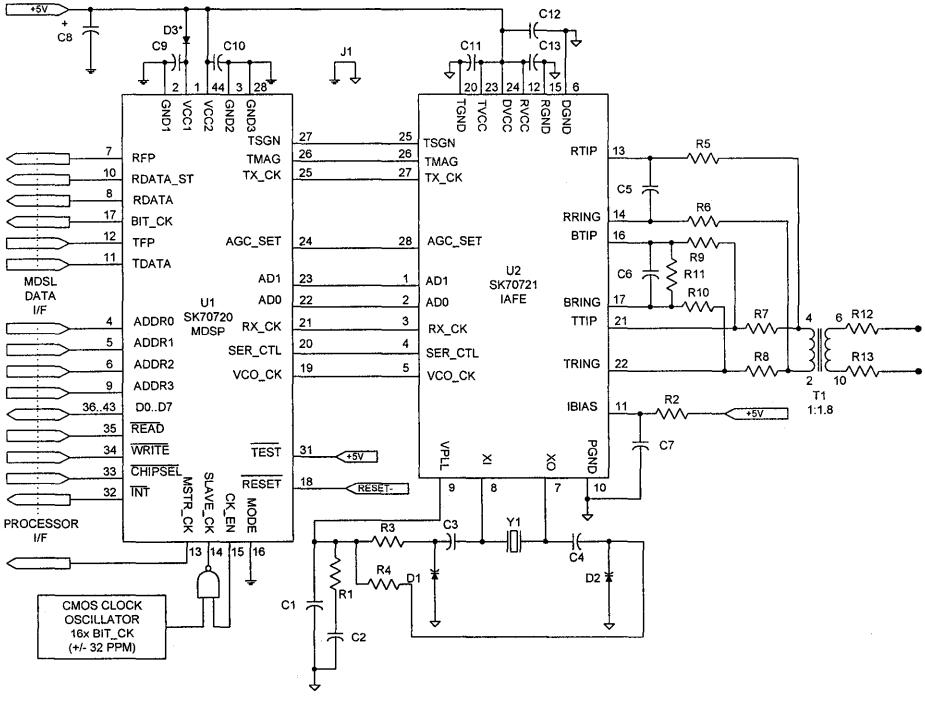
1. R7, R8 should be 20 Ω, when R12 and R13 (the 5.6 Ω fuse links) are not used.

Table 20: Components for Suggested Circuitry (See Figures 13 and 14) – continued

Ref	Description	Ref	Description	Ref	Description
C5, 6	470 pF, COG or mica, 10%	R7, 8[1]	18.2 Ω, 1%	Y1	Pullable Crystal 784 kbps: 25.088 MHz (pn:80546/1) 528 kbps: 16.896 MHz (pn:81522/1) 400 kbps: 12.800 MHz (pn:80546/5) 272 kbps: 8.704 MHz (pn:81523/1) (Hy-Q International)
C7, 11-13	0.1 µF, ceramic, 10%	R9, 10	806 Ω, 1%		
C8	100 µF, electrolytic, 20%	R11	2.49 kΩ, 1%	T1	1:1.8 Transformer ≥ 400 kbps: Midcom 671-7376 or Pulse Engineering PE-68614 < 400 kbps: Midcom 50109

1. R7, R8 should be 20 Ω, when R12 and R13 (the 5.6 Ω fuse links) are not used.

Figure 14: Typical Application for Slave Mode Operation



NOTES:

Diode D3 is optional.

The MDSP and IAFE should have independent ground planes connected at a single point near pin 5 of the IAFE.

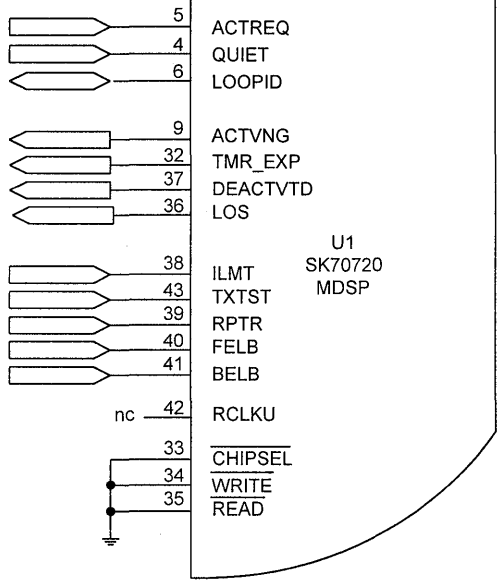
Table 21: Transformer Specifications
(Figures 13 and 14, Reference T1)

Measure	Value	Tolerance
Turns Ratio (IC:Line)	1:1.8	±1%
Line Side Inductance ≥ 400 kbps < 400 kbps	2.8 mH 11.7 mH	±10%
Leakage Inductance	≤ 50 µH	
Interwinding Capacitance	≤ 70 pF	
THD	≤ -70 dB	
Longitudinal Balance	≥ 50 dB	5-196 kHz
Return Loss	≥ 20 dB	40-200 kHz
Isolation	1500 VRMS	
Primary DC Resistance	≤ 3.2 Ω	
Secondary DC Resistance	≤ 6.0 Ω	
Operating Temperature	-40 to +85° C	

Table 22: Crystal Specifications
(Figures 13 and 14, Reference Y1)

Measure	Value	Offset
Frequency @C_L = 20 pF	8.704 to 25.088 MHz	-0, +40 ppm
Mode	Fundamental, Parallel Resonance	
Pullability (C_L = 24 pF ⇨ 16 pF)	≥ +160 ppm	
Operating Temperature	-40 to +85 ° C	
Temperature Drift	≤ ±30 ppm	
Aging Drift	≤ 5 ppm/year	
Series Resistance	≤ 15 Ω	
Drive Level	0.5 mW	

Figure 15: MDSP Control and Status Signals (Stand-alone Mode)



NOTE:
1. This figure illustrates the MDSP control and status signals in stand-alone mode. All other MDSP and IAFE signals are connected as shown in Figures 13 and 14.

TEST SPECIFICATIONS

NOTE

The minimum and maximum values in Tables 23 through 33 and Figures 16 through 23 represent the performance specifications of the Data Pump and are guaranteed by test, except where noted by design.

Table 23: IAFE Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Supply voltage[1] (reference to ground[2])	TVCC, RVCC, DVCC	-0.3	+6.0	V
Input voltage[2, 3], any input pin	TVCC, RVCC, DVCC	- 0.3V	VCC + 0.3	V
Continuous output current, any output pin	–	–	±25	mA
Storage temperature	TSTOR	-65	+150	° C

CAUTION

Operations at the limits shown may result in permanent damage to the Integrated Analog Front End. Normal operation at these limits is neither implied nor guaranteed

1. No supply input may have a maximum potential of more than ±0.3 V from any other supply input.
2. TGND = 0V; RGND = 0V; DGND = 0V.
3. TVCC = RVCC = DVCC = VCC.

Table 24: IAFE Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
DC supply	TVCC, DVCC, RVCC	4.75	5.0	5.25	V
Ambient operating temperature	TA	-40	+25	+85	° C

Table 25: IAFE DC Electrical Characteristics (Over Recommended Range)

Parameter	Sym	Min	Typ[1]	Max	Unit	Test Conditions
Supply current (full operation)	ICC	–	80	120	mA	83 Ω resistor across TTIP and TRING
Input low voltage	VIL	–	–	0.5	V	IIL < 40 µA
Input high voltage	VIH	4.5	–	–	V	IIH < 40 µA
Output low voltage	VOL	–	–	0.2	V	IOL < 40 µA
Output high voltage	VOH	4.5	–	–	V	IOH < 40 µA
Input leakage current[2]	IIL	–	–	±50	µA	0 < VIN < VCC
Input capacitance (individual pins)	CIN	–	12	–	pF	
Load capacitance (MSTR_CK output)	CLREF	–	–	20	pF	

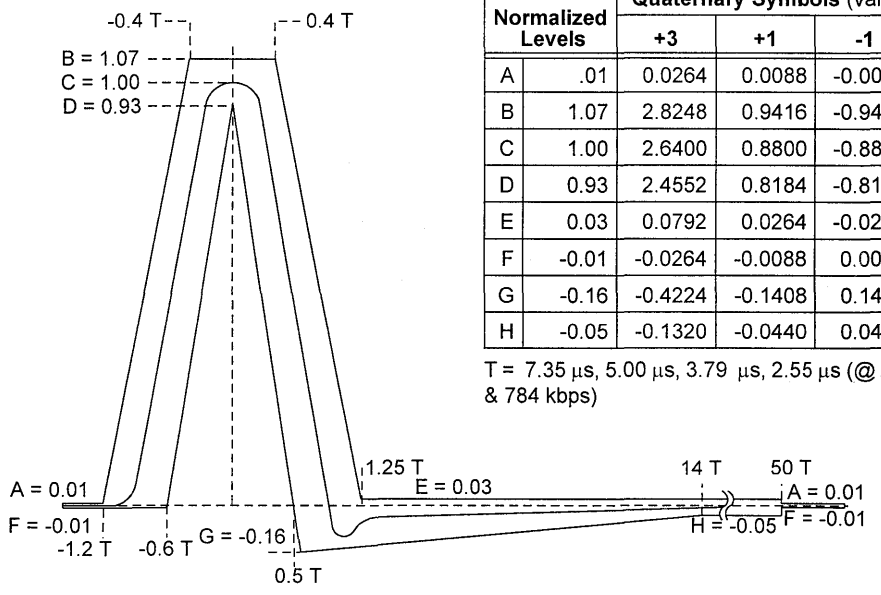
1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.
2. Applies to pins 3, 4, 25, 26 and 27.

Table 26: IAFE Transmitter Electrical Parameters (Over Recommended Range)

Parameters	Sym	Min	Typ	Max	Unit	Test Conditions
Isolated pulse height at TTIP, TRING	–	+2.455	+2.640	+2.825	Vp	TDATA High, TFP Low (+3)
	–	-2.825	-2.640	-2.455	Vp	TDATA Low, TFP Low (-3)
	–	+0.818	+0.880	+0.941	Vp	TDATA High, TFP High (+1)
	–	-0.941	-0.880	-0.818	Vp	TDATA Low, TFP High (-1)
Setup time (TSGN, TMAG)	tTSMSU	5	–	–	ns	
Hold time (TSGN, TMAG)	tTSMH	12	–	–	ns	

1. Pulse amplitude measured across a 135 Ω resistor on the line side of the transformer using the application circuit shown in Figure 13 and Table 21.

Figure 16: IAFE Normalized Pulse Amplitude Transmit Template



Normalized Levels		Quaternary Symbols (values in Volts) +3	+1	-1	-3
A	.01	0.0264	0.0088	-0.0088	-0.0264
B	1.07	2.8248	0.9416	-0.9416	-2.8248
C	1.00	2.6400	0.8800	-0.8800	-2.6400
D	0.93	2.4552	0.8184	-0.8184	-2.4552
E	0.03	0.0792	0.0264	-0.0264	-0.0792
F	-0.01	-0.0264	-0.0088	0.0088	0.0264
G	-0.16	-0.4224	-0.1408	0.1408	0.4224
H	-0.05	-0.1320	-0.0440	0.0440	0.1320

T = 7.35 µs, 5.00 µs, 3.79 µs, 2.55 µs (@ 272, 400, 528 & 784 kbps)

NOTE:
1. Pulse amplitude measured across a 135 W resistor on the line side of the transformer using the application circuit shown in Figure 13 and Table 21.

Figure 17: Transmit Power Spectral Density—Upper Bound

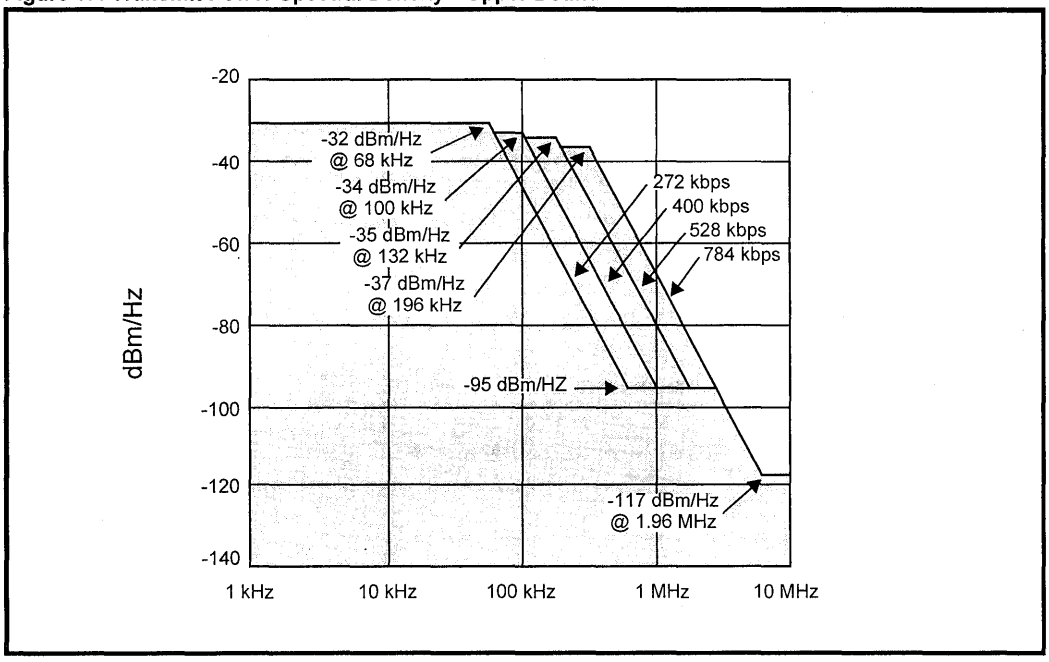


Table 27: IAFE Receiver Electrical Parameters (Over Recommended Range)

Parameter	Sym	Min	Typ	Max	Unit	Test Conditions
Propagation delay (AD0, AD1)	tADD	–	–	25	ns	
Total harmonic distortion	–	–	-80	–	dB	V(RTIP, RRING) = 3 Vpp @ 50 kHz
RTIP, RRING, to BTIP, BRING gain ratio	–	–	1.0	1%	V/V	

Figure 18: IAFE Receiver Syntax and Timing

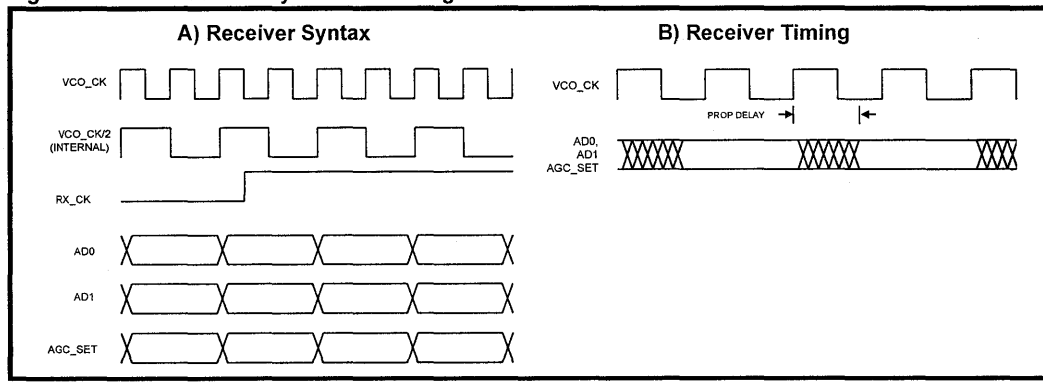
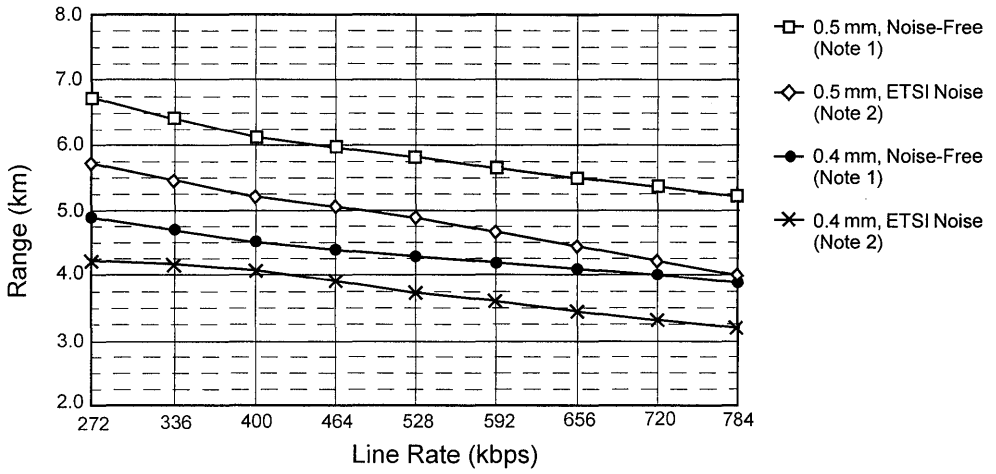


Figure 19: Typical Performance vs. Line Rate and Cable Gauge (Metric)

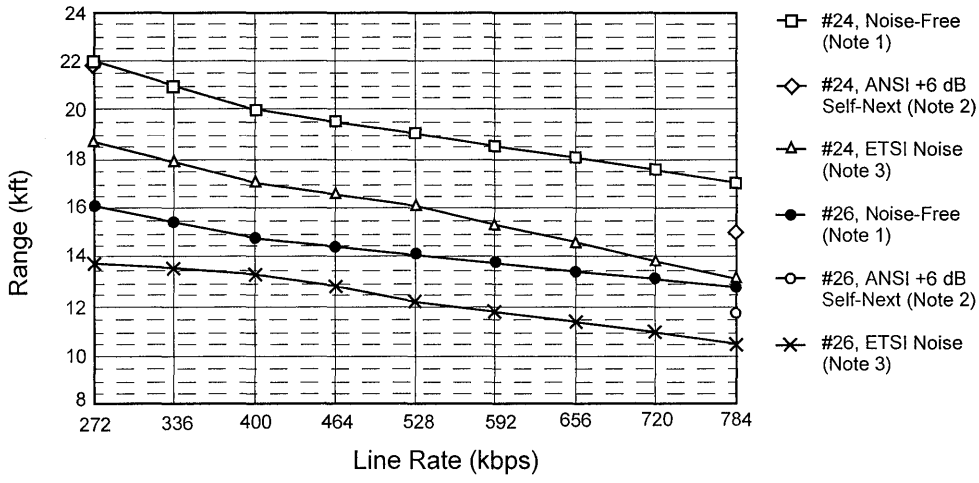


NOTES:

1. Noise-free range is specified with a Bit Error Rate (BER) less than or equal to 1.0×10^{-7}.
2. The range with ETSI shaped noise corresponds to a 0 dB margin with a BER less than or equal to 1.0×10^{-7}. The power spectral density for ETSI standard noise is defined in ETSI ETR-152 section 6.3.3.1.

7

Figure 20: Typical Performance vs. Line Rate and Cable Gauge (English)



NOTES:

1. Noise-free range is specified with a Bit Error Rate (BER) less than or equal to 1.0×10^{-7}.
2. There are no generally accepted noise models for MDSL systems. Performance simulations using ANSI Near End Cross Talk (NEXT) noise models indicate worst case performance degradation should be less than 2 kft (0.6 km) from the noise-free performance.
3. The range with ETSI shaped noise corresponds to a 0 dB margin with a BER less than or equal to 1.0×10^{-7}. The power spectral density for ETSI standard noise is defined in ETSI ETR-152 section 6.3.3.1.

Table 28: MDSP Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Supply voltage[1] (reference to ground[2])	VCC2, VCC1	-0.3	+6.0	V
Input voltage[2], any input pin	–	- 0.3	VCC2 + 0.3	V
Continuous output current, any output pin	–	–	±25	mA
Storage temperature	TSTOR	-65	+150	° C

CAUTION

Operations at the limits shown may result in permanent damage to the MDSL Digital Transceiver (MDSP). Normal operation at these limits is neither implied nor guaranteed

1. The maximum potential between VCC2 and VCC1 must never exceed ±1.2 V.
2. GND3 = 0V; GND2 = 0V; GND1 = 0V.

Table 29: MDSP Recommended Operating Conditions

Parameter		Symbol	Min	Typ	Max	Units
DC supply[1]		VCC1[2]	3.95	5.0	5.25	V
		VCC2	4.75	5.0	5.25	V
		VCC2-VCC1	-0.25	–	+0.9	V
Ambient operating temperature	SK70720PE	TA	-40		+85	° C

1. To derive this supply, a 1N4001 (or equivalent) diode may be connected between VCC2 and VCC1 as shown in Figures 13 and 14.
2. If a diode is used, it should be selected to meet VCC1 minimum specifications.

Table 30: MDSP DC Electrical Characteristics (Over Recommended Range)

Parameter	Sym	Min	Typ[1]	Max	Unit	Test Conditions
Supply current272 kbps 400 kbps 528 kbps 784 kbps	ICC	– – – –	35 48 62 100	45 60 80 135	mA	
Input low voltage	VIL	–	–	0.5	V	IIL < 40 µA
Input high voltage	VIH	4.0	–	–	V	IIH < 40 µA
Output low voltage	VOL	–	–	GND +0.3	V	IOL < 40 µA
Output high voltage	VOH	VCC2-0.5	–	–	V	IOH < 40 µA
Input leakage current[2]	IIL	–	–	±50	µA	0 < VIN < VCC2
Tristate leakage current[3]	ITOL	–	–	±30	µA	0 < V < VCC2
Input capacitance (individual pins)	CIN	–	12	–	pF	
Load capacitance (MSTR_CK output)	CLREF	–	–	15	pF	

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.
2. Applies to pins 4, 5, 11, 12, 14, 16, 18, 19, 22, 23, 24, 29, 31, 33, 34 and 35. Applies to pins 5, 6, 9, 13, and 36-43, when configured as inputs.
3. Applies to pins 7, 8, 10, 15, 17, 30, 32 and 36-43, when tristated.

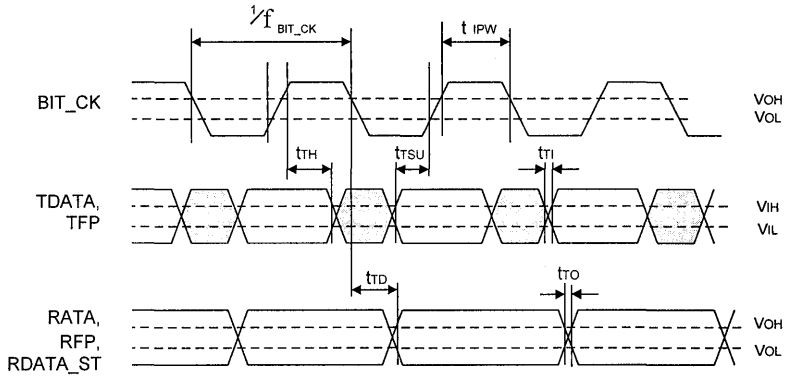
Table 31: MDSL Data Interface Timing Specifications *(See Figure 21)*

Parameter	Symbol	Min	Typ[1]	Max	Unit
BIT_CK frequency	fBIT_CLK	272	–	784	kHz
MSTR_CK frequency	fREFCLK	4.352	–	12.544	MHz
MSTR_CK frequency tolerance (Master Mode)	tolRCLK	-32	0	+32	ppm
SLAVE_CK frequency tolerance (Slave Mode)[2]	tolSLAVE_CK	-32	0	+32	ppm
BIT_CK pulse width high 272 kbps 400 kbps 528 kbps 784 kbps	tIPW	– – – –	1.840 1.250 0.950 0.638	– – – –	µs
Transition time on any digital output[3]	tTO	–	5	10	ns
Transition time on any digital input	tTI	–	–	25	ns
TDATA, TFP setup time to BIT_CK rising edge	tTSU	100	–	–	ns
TDATA, TFP hold time from BIT_CK rising edge	tTH	100	–	–	ns
RDATA, RFP, RDATA_ST delay from BIT_CK falling edge	tTD	0	–	150	ns

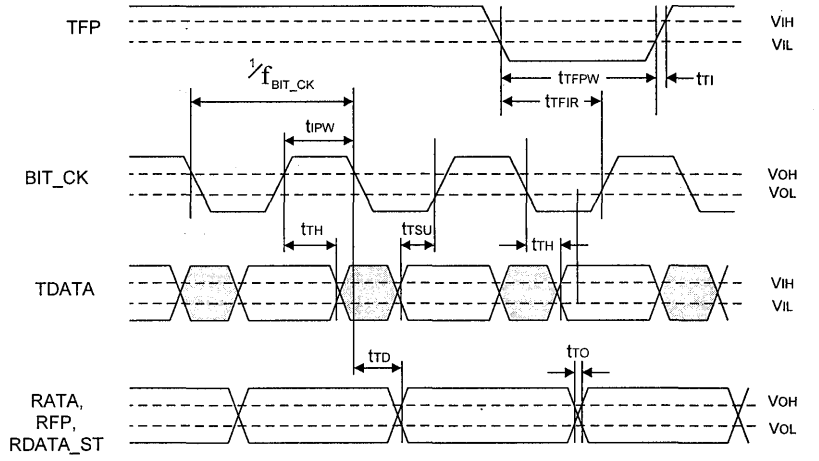
1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.
2. SLAVE_CK must meet this tolerance about a frequency of 16 times the BIT_CK frequency in slave mode.
3. Measured with 15 pF load.

Figure 21: MDSL Data Interface Timing

A) Non-Repeater Mode



B) Repeater Mode



C) Repeater Mode

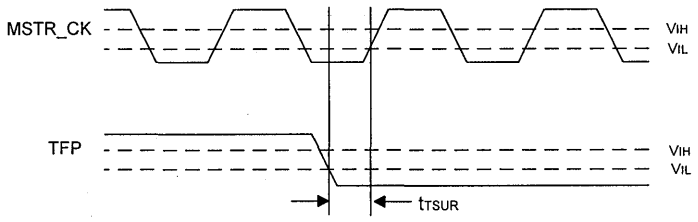


Table 32: MDSP/Microprocessor Interface Timing Specifications *(See Figures 18 & 19)*

Parameter	Symbol	Min	Typ	Max	Unit
$\overline{\text{RESET}}$ pulse width Low	tRPWL	0.1	–	5	s
$\overline{\text{RESET}}$ to $\overline{\text{INT}}$ clear (10 kΩ resistor from $\overline{\text{INT}}$ to VCC2)	tINTH	–	–	300	ns
$\overline{\text{RESET}}$ to data tristate on D0-7	tDTHZ	–	–	100	ns
$\overline{\text{CHIPSEL}}$ pulse width Low	tCSPWL	200	–	–	ns
$\overline{\text{CHIPSEL}}$ Low to data active on D0-7	tCDLZ	–	–	80	ns
$\overline{\text{CHIPSEL}}$ High to data tristate on D0-7	tCDHZ	–	–	80	ns
$\overline{\text{READ}}$ pulse width Low	tRSPWL	100	–	–	ns
$\overline{\text{READ}}$ Low to data active	tRDLZ	–	–	80	ns
$\overline{\text{READ}}$ High to data tristate	tRDHZ	–	–	80	ns
Address to Valid Data	tPRD	–	–	80	ns
Address setup to $\overline{\text{WRITE}}$ rising edge	tASUW	20	–	–	ns
Address hold from $\overline{\text{WRITE}}$ rising edge	tAHW	10	–	–	ns
$\overline{\text{WRITE}}$ pulse width Low	tWPWL	100	–	–	ns
Data setup to $\overline{\text{WRITE}}$ rising edge	tDSUW	20	–	–	ns
Data hold from $\overline{\text{WRITE}}$ rising edge	tDHW	10	–	–	ns
$\overline{\text{READ}}$ High to $\overline{\text{INT}}$ clear when reading register RD0	tINTR	–	–	400	ns

1. Timing for all outputs assumes a maximum load of 30 pF.
2. "Address" refers to input signals $\overline{\text{CHIPSEL}}$, A0, A1, A2, and A3. "Data" refers to I/O signals D0, D1, D2, D3, D4, D5, D6, and D7.

Table 33: General System and Hardware Mode Timing

Parameter		Min	Typ[1]	Max	Unit
Throughput delay	TDATA to TTIP/TRING				
	272 kbps	–	29.4	36.8	
	400 kbps	–	20.0	25.0	µs
	528 kbps	–	15.2	18.9	
	784 kbps	–	10.2	12.5	
	RTINP/RRING to RDATA				
	272 kbps	–	154	206	
	400 kbps	–	105	140	µs
	528 kbps	–	79.6	106	
	784 kbps	–	53.6	72	
Hardware Mode	"ACTREQ" input transitional pulse width (High or Low)	5	–	–	µs
	"QUIET" transitional pulse width (High-to-Low)	5	–	–	µs

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 22: RESET and INTERRUPT Timing (µP Control Mode)

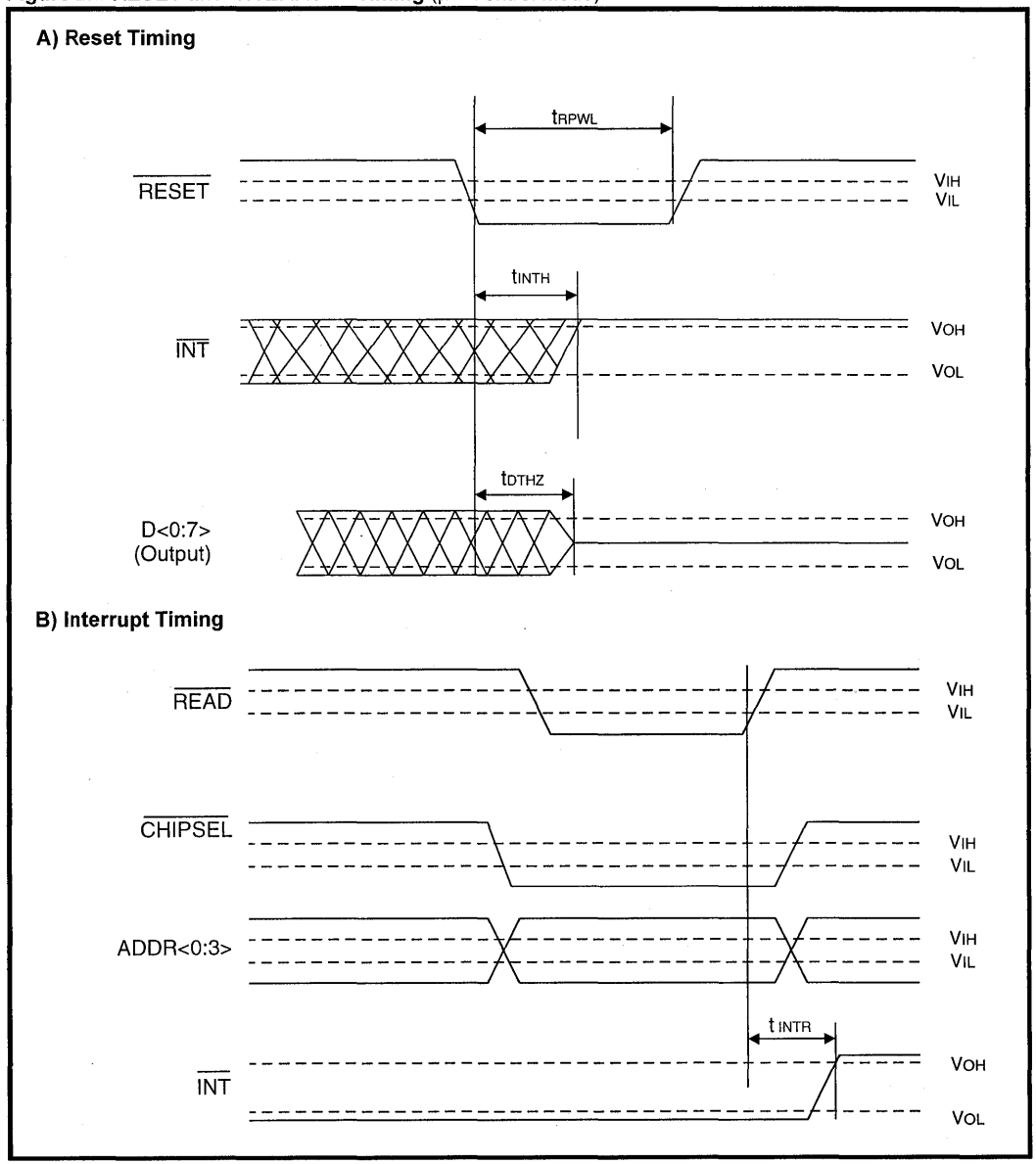
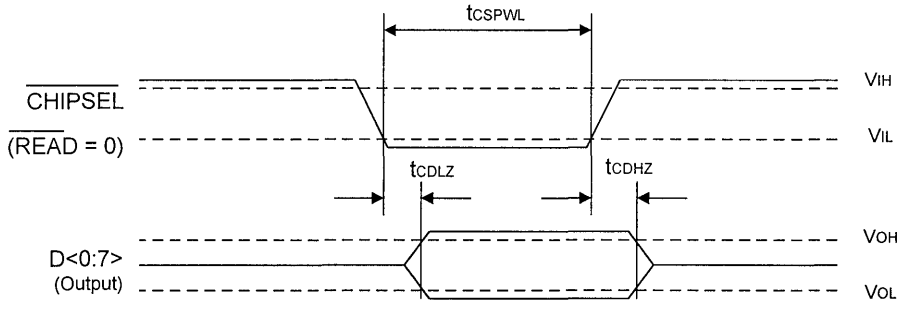
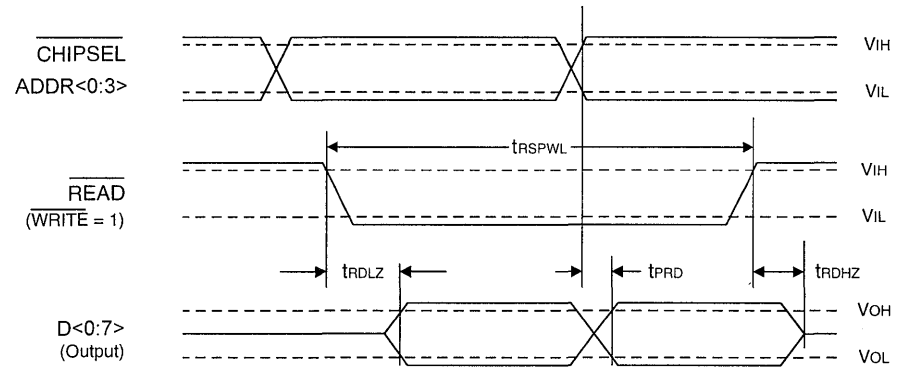


Figure 23: Parallel Data Channel Timing

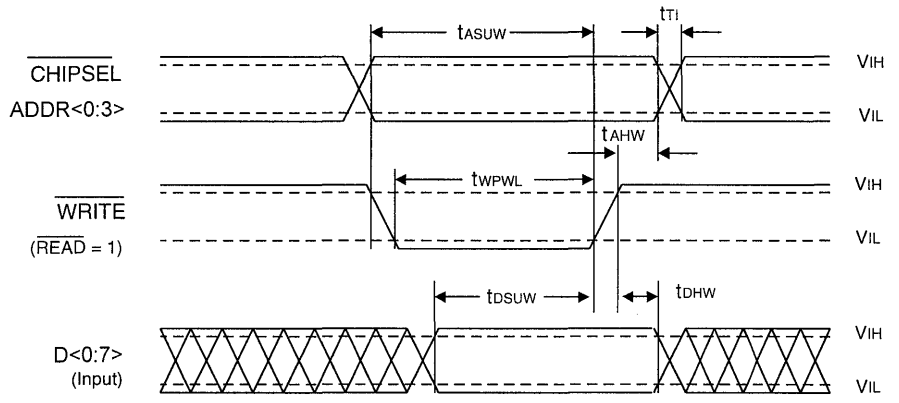
A) Chip Select Timing



B) Data Read Timing



C) Data Write Timing



7

NOTES

PDH Multiplexers

SXT6234

E-Rate Multiplexer

JUNE 1997
REVISION 1.1

General Description

The SXT6234 E-Rate Multiplexer is a single-chip solution for multiplexing four tributary channels into a single high speed data stream and for demultiplexing a high speed data stream back to four tributary channels. All of the necessary circuitry is integrated into the SXT6234 E-Rate Multiplexer; there is no need for an external framing device.

The SXT6234 E-Rate Multiplexer conforms to both the (ITU) G.742 and (ITU) G.751 multiplexing formats defined by the International Telecommunications Union (ITU; formerly known as CCITT): G.742 recommendation for multiplexing four E1 channels into an E2 frame; and the G.751 recommendation for multiplexing four E2 channels into an E3 frame.

The SXT6234 E-Rate Multiplexer also encodes and decodes HDB3 zero suppression line coding used on E1, E2, and E3 signals. The coder and decoder input/output pins are externally accessible, allowing either HDB3 or NRZ (non-return-to-zero) I/O to the multiplexer. The SXT6234 E-Rate Multiplexer can also serve as a five channel HDB3 coder and decoder.

Applications

- E1/E2 Multiplexer (2/8 Mbit/s)
- E2/E3 Multiplexer (8/34 Mbit/s)
- E1/E3 Multiplexer (2/34 Mbit/s)
- Digital Loop Carrier (DLC) Terminal
- Add / Drop Multiplexers (ADM)
- 4 - to - 1 Non-Standard Multiplexer

Features

- Performs four-E1 to one-E2, or four-E2 to one-E3 multiplexing. Five ICs will implement a sixteen-E1 to one-E3 Multiplexer.
- Fully compliant with the G.742 and G.751 ITU recommendations. Fully compliant with G.703 when used with LXT305/332 Line Interface.
- A robust frame-acquisition and frame-holding algorithm minimizes frame slippage, acquires and holds frame below 10^{-2} bit error rate.
- Four auxiliary low speed data or flag channels are available via the Stuffing Bits on each tributary channel.
- Access to the Alarm bit and the National bit. These can be used as recommended by ITU or for proprietary use.
- Five independent HDB3 CODECs allow Multiplexer I/O in either HDB3 or NRZ formats. The SXT6234 can also function as a stand alone five-channel HDB3 transcoder.

8

SXT6234 Block Diagram

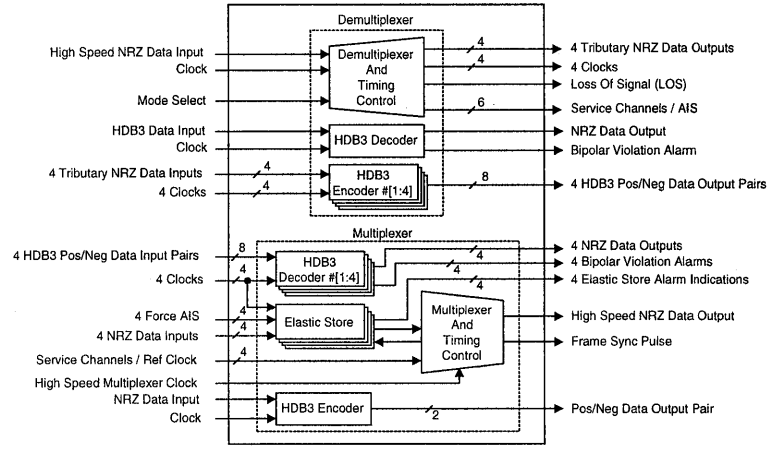


Figure 1: SXT6234 Pin Assignment

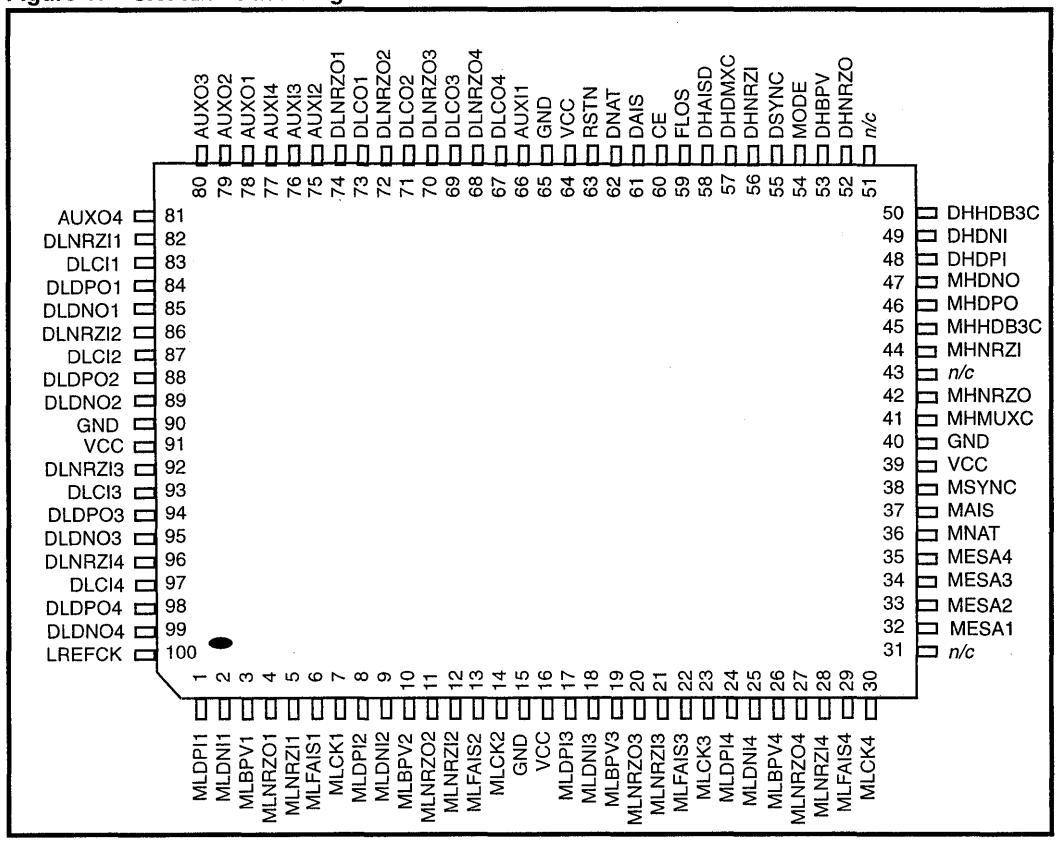


Table 1: Input Signals

Pin #	Sym	Description
1	MLDPI1	**HDB3 Decoder #1 Positive Data Input.** HDB3 Decoder #1 positive rail input clocked on the positive transitions of the clock signal MLCK1.
2	MLDNI1	**HDB3 Decoder #1 Negative Data Input.** HDB3 Decoder #1 negative rail input clocked on the positive transitions of the clock signal MLCK1.
8	MLDPI2	**HDB3 Decoder #2 Positive Data Input.** HDB3 Decoder #2 positive rail input clocked on the positive transitions of the clock signal MLCK2.
9	MLDNI2	**HDB3 Decoder #2 Negative Data Input.** HDB3 Decoder #2 negative rail input clocked on the positive transitions of the clock signal MLCK2.
17	MLDPI3	**HDB3 Decoder #3 Positive Data Input.** HDB3 Decoder #3 positive rail input clocked on the positive transitions of the clock signal MLCK3.
18	MLDNI3	**HDB3 Decoder #3 Negative Data Input.** HDB3 Decoder #3 negative rail input clocked on the positive transitions of the clock signal MLCK3.

Table 1: Input Signals–continued

Pin #	Sym	Description
24	MLDPI4	**HDB3 Decoder #4 Positive Data Input.** HDB3 Decoder #4 positive rail input clocked on the positive transitions of the clock signal MLCK4.
25	MLDNI4	**HDB3 Decoder #4 Negative Data Input.** HDB3 Decoder #4 negative rail input clocked on the positive transitions of the clock signal MLCK4.
7	MLCK1	**Multiplexer Tributary #1 Clock Input.** Clock input for Multiplexer side tributary channel #1. This clock is used by both the associated HDB3 decoder and the Multiplexer. For standard rate applications, this clock must have a frequency of ±50 ppm for 2048 kbit/s operation and ±30 ppm for the 8448 kbit/s operation as per ITU G.703.
14	MLCK2	**Multiplexer Tributary #2 Clock Input.** Idem as MLCK1 with tributary #2 in.
23	MLCK3	**Multiplexer Tributary #3 Clock Input.** Idem as MLCK1 with tributary #3 in.
30	MLCK4	**Multiplexer Tributary #4 Clock Input.** Idem as MLCK1 with tributary #4 in.
5	MLNRZI1	**Multiplexer Tributary #1 NRZ Data Input.** Multiplexer tributary NRZ input clocked on the falling edge of the clock signal MLCK1.
12	MLNRZI2	**Multiplexer Tributary #4 NRZ Data Input.** Multiplexer tributary NRZ input clocked on the falling edge of the clock signal MLCK2.
21	MLNRZI3	**Multiplexer Tributary #3 NRZ Data Input.** Multiplexer tributary NRZ input clocked on the falling edge of the clock signal MLCK3.
28	MLNRZI4	**Multiplexer Tributary #4 NRZ Data Input.** Multiplexer tributary NRZ input clocked on the falling edge of the clock signal MLCK4.
6	MLFAIS1	**Force AIS on Multiplexer Tributary #1.** Active high signal to force AIS (all 1's) data and LREFCK clock on Multiplexer tributary #1.
13	MLFAIS2	**Force AIS on Multiplexer Tributary #2.** Active high signal to force AIS (all 1's) data and LREFCK clock on Multiplexer tributary #2.
22	MLFAIS3	**Force AIS on Multiplexer Tributary #3.** Active high signal to force AIS (all 1's) data and LREFCK clock on Multiplexer tributary #3.
29	MLFAIS4	**Force AIS on Multiplexer Tributary #4.** Active high signal to force AIS (all 1's) data and LREFCK clock on Multiplexer tributary #4.
66	AUXI1	**Auxiliary Flag/Data #1 Input.** The signal on this pin is clocked into the frame at the stuffing bit location (J1) when justification is such that tributary data is NOT placed at this location. A high on alarm signal MESA1 indicates this condition during the current frame.
75	AUXI2	**Auxiliary Flag/Data #2 Input.** See AUXI1 Description. MESA2 is relevant indication signal.
76	AUXI3	**Auxiliary Flag/Data #3 Input.** See AUXI1 Description. MESA3 is relevant indication signal.
77	AUXI4	**Auxiliary Flag/Data #4 Input.** See AUXI1 Description. MESA4 is relevant indication signal.
36	MNAT	**National Bit Input.** National Bit input that is placed in the 12th bit of the frame as per ITU G.742, G.751 specifications.
37	MAIS	**AIS/Error Bit Input.** AIS Bit input that is placed in the 11th bit of the frame, as per ITU G.742, G.751 specifications.

Table 1: Input Signals–continued

Pin #	Sym	Description
41	MHMUXC	**High speed Multiplexer Clock Input.** Clock input for Multiplexer functions and NRZ high speed data output. For standard rate applications, this clock must have a frequency of ±30 ppm for the 8448 kbit/s operation and ±20 ppm for the 34368 kbit/s operation as per ITU G.703.
44	MHNRZI	**HDB3 Encoder #5 NRZ Input.** HDB3 Encoder #5 (High speed) NRZ input clocked on the rising edge of MHHDB3C.
45	MHHDB3C	**HDB3 Encoder #5 Clock Input.** When used in conjunction with the Multiplexer, this pin should be tied to the high speed Multiplexer Clock, MHMUXC, P41.
48	DHDPI	**HDB3 Decoder #5 Positive Data Input.** HDB3 Decoder #5 (High Speed) positive rail input clocked on the rising edge of DHHDB3C.
49	DHDNI	**HDB3 Decoder #5 Negative Data Input.** HDB3 Decoder #5 (High Speed) positive rail input clocked on the rising edge of DHHDB3C.
50	DHHDB3C	**HDB3 Decoder #5 Clock Input.** When used in conjunction with the Demultiplexer, this pin should be tied to the high speed Demultiplexer Clock, DHMUXC, P57.
56	DHNRZI	**Demultiplexer NRZ Data Input.** Demultiplexer NRZ input clocked on rising edge of DHDMXC.
57	DHDMXC	**High speed Demultiplexer Clock Input.** Clock input for Demultiplexer functions and NRZ high speed data in. For standard rate applications, this clock must have a frequency of ±30 ppm for the 8448 kbit/s operation and ±20 ppm for the 34368 kbit/s operation as per ITU G.703.
82	DLNRZI1	**HDB3 Encoder #1 NRZ Data Input.** HDB3 Encoder #1 NRZ input clocked on rising edge of DLCI1.
86	DLNRZI2	**HDB3 Encoder #2 NRZ Data Input.** HDB3 Encoder #2 NRZ input clocked on rising edge of DLCI2.
92	DLNRZI3	**HDB3 Encoder #3 NRZ Data Input.** HDB3 Encoder #3 NRZ input clocked on rising edge of DLCI3.
96	DLNRZI4	**HDB3 Encoder #4 NRZ Data Input.** HDB3 Encoder #4 NRZ input clocked on rising edge of DLCI4.
83	DLCI1	**HDB3 Encoder #1 Clock Input.** Clock input for HDB3 Encoder #1.
87	DLCI2	**HDB3 Encoder #2 Clock Input.** Clock input for HDB3 Encoder #2.
93	DLCI3	**HDB3 Encoder #3 Clock Input.** Clock input for HDB3 Encoder #3.
97	DLCI4	**HDB3 Encoder #4 Clock Input.** Clock input for HDB3 Encoder #4.
54	MODE	**E12/E23 Mode Select.** Mode selection for multiplexer/demultiplexer operation. A low signal selects 4E1/E2 multiplexing. A high signal selects 4E2/E3 multiplexing.
100	LREFCK	**Tributary Reference Clock.** This clock is used as a reference for the Force AIS functions (See Pin 6 Description). For standard rate applications, this clock must have a frequency of ±50 ppm for the 2048 kbit/s operation and ±30 ppm for the 8448 kbit/s operation as per ITU G.703.
60	CE	**Chip Enable.** A high signal forces all outputs into tri-state; used for PCB Testing. This signal should be low for normal operation.
63	RSTN	**Reset.** An active low reset pin. Must be pulsed low on power up to initialize all internal circuits after V_{CC} and clocks are stable.

Table 1: Input Signals–continued

Pin #	Sym	Description
15, 40 65, 90	GND	**Ground.** Ground Reference.
16, 39 64, 91	V_{CC}	**Voltage.** 5-volt supply voltage.

Table 2: Output Signals

Sym	Pin #	Description
MLNRZO1	4	**HDB3 Decoder #1 NRZ Output.** HDB3 Decoder #1 NRZ output clocked on the rising edge of MLCK1.
MLNRZO2	11	**HDB3 Decoder #2 NRZ Output.** HDB3 Decoder #2 NRZ output clocked on the rising edge of MLCK2.
MLNRZO3	20	**HDB3 Decoder #3 NRZ Output.** HDB3 Decoder #3 NRZ output clocked on the rising edge of MLCK3.
MLNRZO4	27	**HDB3 Decoder #4 NRZ Output.** HDB3 Decoder #4 NRZ output clocked on the rising edge of MLCK4.
MLBPV1	3	**HDB3 Decoder #1 Bipolar Violation Alarm.** This open collector output pulses every time a bipolar violation occurs in the decoding process.
MLBPV2	10	**HDB3 Decoder #2 Bipolar Violation Alarm.** This open collector output pulses every time a bipolar violation occurs in the decoding process.
MLBPV3	19	**HDB3 Decoder #3 Bipolar Violation Alarm.** This open collector output pulses every time a bipolar violation occurs in the decoding process.
MLBPV4	26	**HDB3 Decoder #4 Bipolar Violation Alarm.** This open collector output pulses every time a bipolar violation occurs in the decoding process.
MESA1	32	**Multiplexer Tributary #1 Elastic Store Alarm Indication.** Multiplexer justification status for tributary #1. A high indicates bit stuffing on the current frame. A low indicates an information bit. When externally filtered, this signal can be used to indicate elastic store failure or incorrect tributary frequency.
MESA2	33	**Multiplexer Tributary #2 Elastic Store Alarm Indication.** Idem as MESA1 with tributary channel 2.
MESA3	34	**Multiplexer Tributary #3 Elastic Store Alarm Indication.** Idem as MESA1 with tributary channel 3.
MESA4	35	**Multiplexer Tributary #4 Elastic Store Alarm Indication.** Idem as MESA1 with tributary channel 4.
MHNRZO	42	**High speed Multiplexer NRZ Output.** Multiplexer NRZ data clocked out on the rising edge of MHMUXC.
MHDPO	46	**HDB3 Encoder #5 Positive Data Output.** HDB3 Encoder #5 Positive rail clocked out on the rising edge of MHHDB3C.
MHDNO	47	**HDB3 Encoder #5 Negative Data Output.** HDB3 Encoder #5 Negative rail clocked out on the rising edge of MHHDB3C.
DLNRZO1	74	**Demux Tributary #1 NRZ Output.** This signal is clocked out on the rising edge of DHDMXC and transitions are coincident with the falling edge of DLCO1.

Table 2: Output Signals–continued

Sym	Pin #	Description
DLNRZO2	72	**Demux Tributary #2 NRZ Output.** This signal is clocked out on the rising edge of DHDMXC and transitions are coincident with the falling edge of DLCO2.
DLNRZO3	70	**Demux Tributary #3 NRZ Output.** This signal is clocked out on the rising edge of DHDMXC and transitions are coincident with the falling edge of DLCO3.
DLNRZO4	68	**Demux Tributary #4 NRZ Output.** This signal is clocked out on the rising edge of DHDMXC and transitions are coincident with the falling edge of DLCO4.
DLCO1	73	**Demux Tributary #1 Clock Output.** Demultiplexer side recovered clock of tributary #1. This clock has a duty cycle of 75% and is gapped at points in the frame where tributary data is not present (i.e., frame word). The maximum gap is 3 clocks at the frame word location. The frequency will match that of the far end multiplexer tributary input. This signal is clocked out on the rising edge of DHDMXC.
DLCO2	71	**Demux Tributary #2 Clock Output.** Demultiplexer side recovered clock of tributary #2. See DLCO1 description.
DLCO3	69	**Demux Tributary #3 Clock Output.** Demultiplexer side recovered clock of tributary #3. See DLCO1 description.
DLCO4	67	**Demux Tributary #4 Clock Output.** Demultiplexer side recovered clock of tributary #4. See DLCO1 description.
DLDPO1	84	**HDB3 Encoder #1 Output +.** HDB3 Encoder #1 positive rail output clocked out on the rising edge of DLCI1.
DLDNO1	85	**HDB3 Encoder #1 Output -.** HDB3 Encoder #1 negative rail output clocked out on the rising edge of DLCI1.
DLDPO2	88	**HDB3 Encoder #2 Output +.** HDB3 Encoder #2 positive rail output clocked out on the rising edge of DLCI2.
DLDNO2	89	**HDB3 Encoder #2 Output -.** HDB3 Encoder #2 negative rail output clocked out on the rising edge of DLCI2.
DLDPO3	94	**HDB3 Encoder #3 Output +.** HDB3 Encoder #3 positive rail output clocked out on the rising edge of DLCI3.
DLDNO3	95	**HDB3 Encoder #3 Output -.** HDB3 Encoder #3 negative rail output clocked out on the rising edge of DLCI3.
DLDPO4	98	**HDB3 Encoder #4 Output +.** HDB3 Encoder #4 positive rail output clocked out on the rising edge of DLCI4.
DLDNO4	99	**HDB3 Encoder #4 Output -.** HDB3 Encoder #4 negative rail output clocked out on the rising edge of DLCI4.
DHNRZO	52	**HDB3 Decoder #5 NRZ Data Output.** HDB3 Decoder #5 NRZ data clocked out on the rising edge of DHHDB3C.
DHBPV	53	**HDB3 Decoder #5 Bipolar Violation Alarm.** This active high signal pulses every time a bipolar violation occurs in the decoding process.
AUXO1	78	**Auxiliary Flag/Data #1 Output.** Auxiliary Data #1 output that contains data value input on AUXI1. See AUXI1 Description.
AUXO2	79	**Auxiliary Flag/Data #2 Output.** Auxiliary Data #2 output that contains data value input on AUXI2. See AUXI1 Description.

Table 2: Output Signals–continued

Sym	Pin #	Description
AUXO3	80	**Auxiliary Flag/Data #3 Output.** Auxiliary Data #3 output that contains data value input on AUXI3. See AUXI1 Description.
AUXO4	81	**Auxiliary Flag/Data #4 Output.** Auxiliary Data #4 output that contains data value input on AUXI4. See AUXI1 Description.
DNAT	62	**National Bit Output.** Updated every frame based on the contents of the 12th bit in the frame as per ITU G.742, G.751
DHAISD	58	**Demultiplexer Input AIS Detect.** Active high alarm occurs when an all 1's condition (AIS) is detected at the DHNRZI input. This alarm will not occur if the input is a framed signal (i.e. all tributaries are AIS on multiplexer side).
FLOS	59	**Demultiplexer Loss of Frame Alarm.** Active high Frame Loss Alarm that occurs when the Demux has not detected the Frame word.
MSYNC	38	**Multiplexer Frame Sync Pulse.** Pulse of one high speed clock cycle synchronous with the last bit of the frame (just before the frame word of the next frame).
DSYNC	55	**Dmx Frame Sync Pulse.** Pulse of one high speed clock cycle synchronous with the first bit of the frame word of the high speed incoming signal.
DAIS	61	**AIS Error Bit Output.** Updated every frame based on the contents of the 11th bit in the frame as per ITU G.742 and G.751.
NC	31, 43 51	**Not Connected.** These pins must be left unconnected.

FUNCTIONAL DESCRIPTION

NOTE

This Functional Description is for design aid only

The SXT6234 E-Rate Multiplexer consists of a multiplexer block, a demultiplexer block, five HDB3 decoders, and five HDB3 encoders. If the HDB3 codecs are used, the signal flow would be as follows:

Multiplexer: Four tributaries of data feed HDB3 decoders one through four. The NRZ outputs of the decoders are connected to the multiplexer tributary inputs. Within the multiplexer, the justification or stuffing for each tributary is determined; the frame word is added; and the high speed NRZ data sent out. The multiplexer output is connected to HDB3 encoder five where it is encoded and sent out as Positive Data Output (MHDPO) and Negative Data Output (MHDNO).

Demultiplexer: High speed encoded data feeds the HDB3 decoder five and is output as NRZ data. The decoder output is connected to the demultiplexer input where it enters both the frame search circuitry and the demultiplexing circuitry. Once the frame is detected, the NRZ data is demultiplexed into the four tributaries and the justification is removed. Tributary data is then sent out in NRZ format. These tributary outputs, both Clock Output (DLCO*x*) and NRZ Output (DLNRZO*x*), are connected to HDB3 encoders one through four, encoded, and output as Positive Data (MHDPO) and Negative Data (MHDNO).

FRAME FORMAT

The multiplexer and demultiplexer share the Mode Select (MODE) control pin. When MODE is low, the multiplexer conforms to the ITU G.742 format for four-E1 to E2 (Figure 3). An E2 frame is 848 bits long, with 205 data bits and one justification bit for each E1 tributary. When MODE is high, the multiplexer conforms to the ITU G.751 format for four-E2 to E3 (Figure 4). This E3 frame is 1536 bits long, with 377 data bits and one justification bit for each E2 tributary.

In both E2 and E3 formats, there are two flag bits per frame: the AIS bit and the National bit. The four justification bits may also be used as additional flag bits.

HDB3 CODECS

Five HDB3 codecs are included within the SXT6234 to allow easy integration with a wide range of line interface circuits. There are four low speed codecs for the tributary streams and one high speed codec to process the high speed output data. All five codecs are identical and all I/O pins are externally accessible for each device. All codecs can be operated at the maximum operating speed if the chip is used as a stand alone HDB3 transcoder. Note that the "low speed" decoders share a clock with the multiplexer tributary clocks.

Each HDB3 decoder is provided with Positive Data, Negative Data, and clock; they decode the data into a single NRZ bit stream. The HDB3 encoders are provided with NRZ data and clock; they produce the Positive Data and Negative Data bit streams.

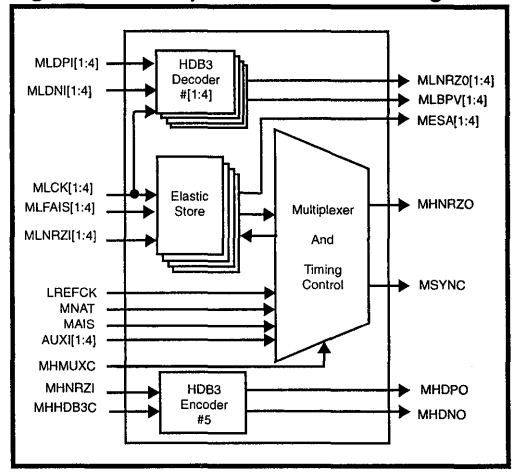
HDB3 DECODER ALARMS

A Bipolar Violation Alarm (MLBPV*x*, DHBPV) associated with each HDB3 decoder indicate detection of a coding violation error within the data. Coding violations include Bipolar Violations, a string of more than four zeros in a row, or encoding violations. The active high alarm is one clock cycle in duration.

MULTIPLEXER

The multiplexer formats four low speed NRZ tributaries into a single high speed bit stream (Figure 2). Tributary data rates are synchronized via internal elastic store memories using a positive justification process as specified in the ITU recommendations.

Figure 2: Multiplexer Side Block Diagram



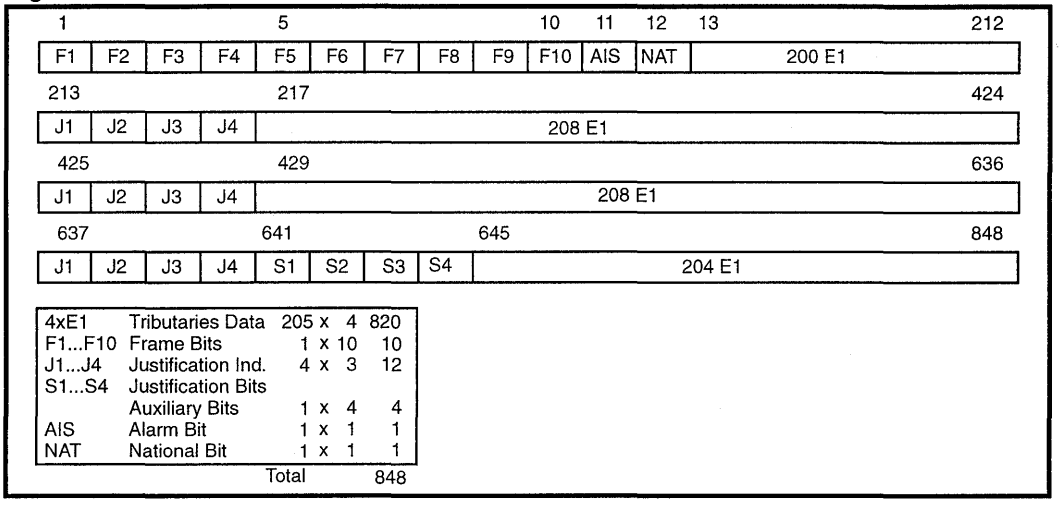
Data enters a first-in/first-out (FIFO) elastic store block. The FIFO receives the data along with the tributary clock and a pointer generated from the timing control. The output of the elastic store block is clocked by the tributary enable

pulses from the timing control, and the data is finally processed by the multiplexer. Processing normally places the output data bit into the high speed bit stream during the tributary enable. An once-per-frame exception occurs during justification. During this event the location of the pointer in the FIFO is determined and a decision made for justification. If the elastic store is less than half full, a justification bit (used for the auxiliary flag channels) is placed in the bit stream and the MESA*x* pin is set high. When the elastic store becomes over half full, a tributary bit is clocked out from the FIFO, placed in the bit stream, and the MESA*x* pin set low. There are three justification indicators spread throughout the frame to show the status of the justification bit to the demultiplexer. Finally, the National and AIS bits are added at the beginning of each frame, and the bit stream is clocked out on MHNRZO.

The multiplexer timing control receives a high speed clock and generates the frame structure and timing control according to the bit length of each frame. This is 848 bits for an E2 frame, and 1536 bits for an E3 frame. MODE provides for either E2 or E3 selection.

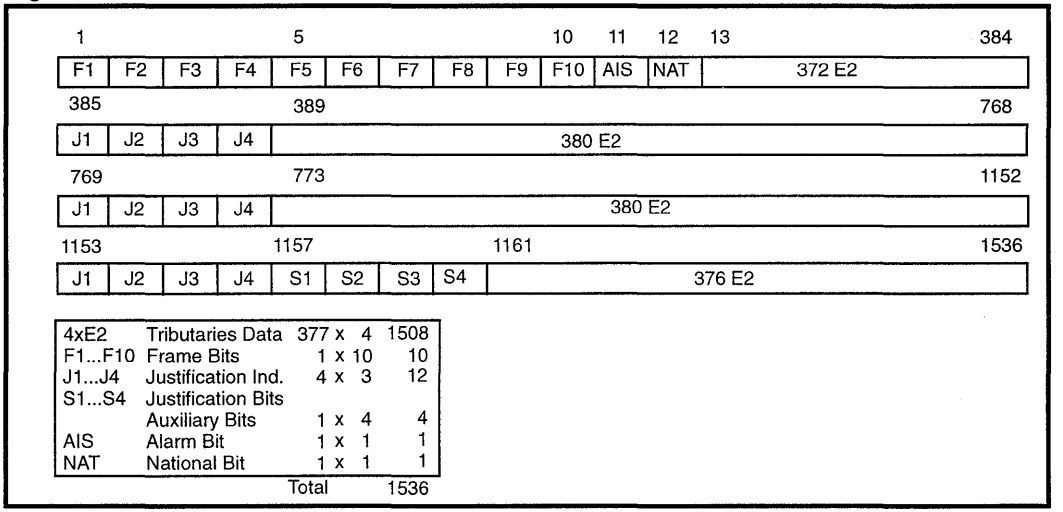
In case of tributary transmission failure or the loss of a signal, tributary data can be forced to an all 1's state. For each tributary this function is controlled at the MLFAIS*x* pin.

Figure 3: E2 Frame



4xE1	Tributaries Data	205 x 4	820
F1...F10	Frame Bits	1 x 10	10
J1...J4	Justification Ind.	4 x 3	12
S1...S4	Justification Bits		
	Auxiliary Bits	1 x 4	4
AIS	Alarm Bit	1 x 1	1
NAT	National Bit	1 x 1	1
	Total		848

Figure 4: E3 Frame



4xE2	Tributaries Data	377 x 4	1508
F1...F10	Frame Bits	1 x 10	10
J1...J4	Justification Ind.	4 x 3	12
S1...S4	Justification Bits		
	Auxiliary Bits	1 x 4	4
AIS	Alarm Bit	1 x 1	1
NAT	National Bit	1 x 1	1
	Total		1536

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Flag Bits

Two flag bits, defined as the National Bit (MNAT) and AIS/Error Bit (MAIS) are transmitted with each frame. At the appropriate time the bit values of the MNAT and MAIS inputs are inserted into the frame. There are also four auxiliary flag channels available (AUXIx) that use the justification bit. These flags are placed in the frame approximately 40% of the time, depending on the ratio of the tributary clock to the multiplexer clock. A high on MESA*x* indicates that the AUXI*x* flag will be inserted into the current frame.

Multiplexer Alarms

An indicator bit (MESAx) for each tributary monitors the status of the elastic store memory. This pin provides the justification status of the tributary. Under normal conditions this pin toggles at the frame rate with a 40% duty cycle. Large variation of the duty cycle indicates the tributary clock frequency is out of specification. Loss of clock would cause MESA to assume a rail value.

For use as a frequency alarm this signal should be filtered by a single-pole RC filter far below the frame frequency, and connected to a pair of voltage comparators. The unfiltered alarm signal can be used to clock the auxiliary data channel inputs.

DEMULTIPLEXER

Data entering the demultiplexer is sent to both the demultiplexing block and the framer. The framer, using a Sieve algorithm, examines the incoming data to find the framing word. A frame is declared found when three passes show the frame word has been found at the same location within the frame. The timing module is then synchronized to the incoming data frame and the Frame Loss Alarm turns off.

Valid tributary data can be extracted after the frame is found. For each tributary, three justification indicator bits are stored. A majority-rule determination decides whether the justification bit is sent as tributary data (with clock) or as an auxiliary bit (with no clock).

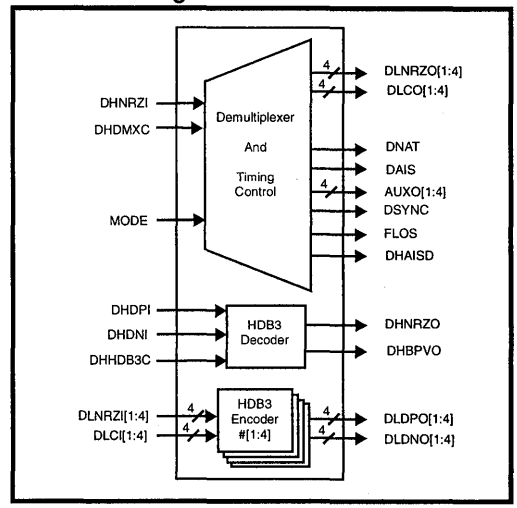
The DNAT and DAIS flag bits are updated for each frame and sent to their dedicated pins. The auxiliary flag bits AUXO*x* are updated when they are available on the frame.

Demultiplexer Alarms

The demultiplexer has two active-high alarms: Frame Loss (FLOS), and Demultiplexer Input AIS Detect (DHAISD).

- FLOS is active at power-up and clears after three consecutive frames are detected. During normal operation FLOS becomes active after missing four consecutive frames.
- DHAISD activates after 768 consecutive 1's pass through the high speed NRZ data stream. DHAISD will occasionally glitch if four tributaries are all 1's and the justification of all four channels is identical. This glitch is filtered with a single-pole RC filter.

Figure 5: Demultiplexer Side Block Diagram



GLOSSARY

AIS	Alarm Indication Signal.
AMI	Alternate Mark Inversion.
CCITT	Consultative Committee for International Telegraph and Telephone (now called the International Telecommunications Union - ITU).
CODEC	COder/DECoder; An assembly comprising an encoder and a decoder within the same unit.
HDB3	High Density Bipolar code of order 3, extension of AMI.
E1	The primary European digital rate of 2.048 MHz, or thirty-two 64 KB channels.
E2	The secondary European rate, four E1 channels at 8.448 MHz.
E3	The tertiary European rate, four E2 channels at 34.368 MHz.
FIFO	First-in/First-Out Memory.
ITU	International Telecommunications Union.
NRZ	Non-Return to Zero.
PCB	Printed Circuit Board.
RZ	Return to Zero.

APPLICATION INFORMATION

NOTE

This application information is for design aid only.

E1/E3 MULTIPLEXER BLOCK DIAGRAM

Figure 6 is a block diagram of the E1/E3 Multiplexer.

E1 Line Interface

- Receive clocks from the pulse data.
- Pass either HDB3 encoded signals to the E-Rate Multiplexer as clock and RZ data or as NRZ data[1]. (Both positive and negative RZ data.)

SXT6234, E1/E2 Stage

- The SXT6234 may interface with either HDB3 or non-HDB3 coded signals. Data from an LIU that does not perform HDB3 decoding must be connected to the HDB3 inputs on the SXT6234. These are the clock (MLCK*x*) and decoder data input signals (both positive - MLDP*x* and negative - MLDN*x*). When receiving data from an LIU which does perform HDB3 decoding, the NRZ data is connected to the MLNRZx input and the clock connects to the MLCK*x* in on the SXT6234
- The four tributaries are interleaved into a single, intermediary E2 rate data stream. An on-board crystal oscillator drives the data output frequency from the mux at the E2 rate of 8.448 MHz. A bit stuffing algorithm implemented in the SXT6234 ensures tributary rate integrity at the output. The SXT6234 contains elastic store buffers to manage bit-stuffing process.
- The NRZ data is sent to a tributary of the E-Rate Multiplexer, stage E2/E3.

SXT6234, E3 Stage

- The multiplexer portion of the SXT6234 interleaves four asynchronous E2 rate NRZ data streams into a single E3 data stream. Depending on the configuration, either an on-board crystal oscillator or an external reference clock drives the data output frequency from the mux at the rate of 34.368 Mbps. The bit stuffing algorithm implemented in the SXT6234 ensures tributary rate integrity at the output.
- If the LIU provides HDB3 encoding, then the NRZ data and clock are passed to the E3 line interface.
- If the LIU does not provide HDB3 encoding, then encoding is done by the SXT6234 and data is output as positive and negative data. An activity monitor provides tributary fail notification when necessary.

See Application Note 9501 for additional information.

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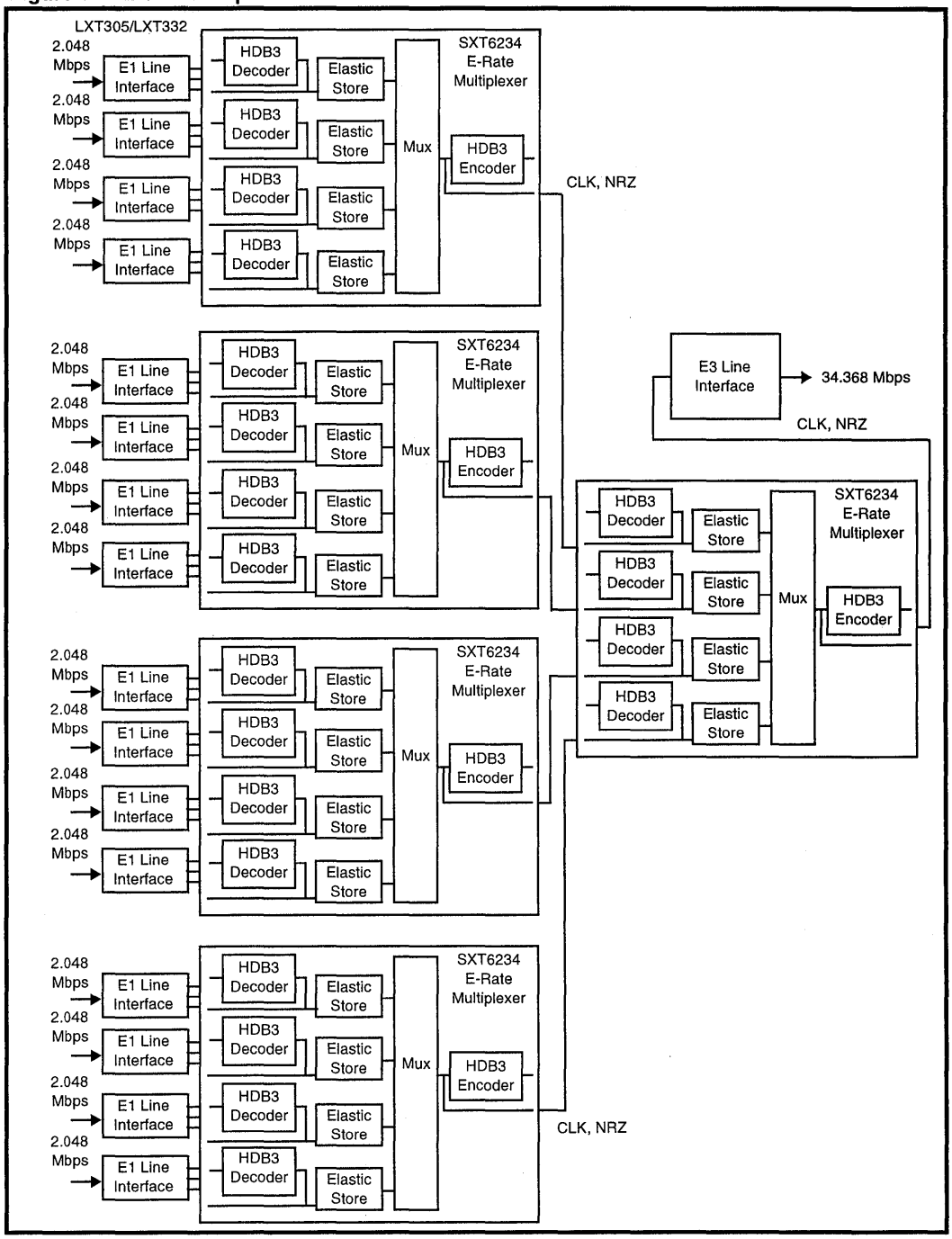
1. If the HDB3 decoder is on the line interface unit (LIU).

Figure 6: E1/E3 Multiplexer



TEST SPECIFICATIONS

NOTE

Minimum and maximum values in Tables 3 through 9 and Figures 7 through 11 represent the performance specifications of the SXT6234 E-Rate Multiplexer and are guaranteed by test except, where noted, by design. Typical values are not subject to production testing.

The SXT6234 E-Rate Multiplexer, fabricated with 1.2-micron CMOS technology, is currently available in a 100-pin plastic quad flat pack package (EIAJ standard 100PQFP). All device I/O comply with 5V CMOS standards. A list of input and output signals is provided with this data sheet. There are 46 input signals and 43 output signals. In addition, there are four V_{CC} power pins and four Ground power pins.

A Chip Enable is provided to facilitate board level, in-circuit testing during the PCB manufacturing process. The SXT6234 E-Rate Multiplexer is fully tested before shipment.

Table 3: Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
DC supply voltage	VCC	-0.3	7.0	V
Input voltage on any pin	VIN	0	VCC+ 0.3	V
Input current	IIN	--	10	µA
Ambient operating temperature	TAM	0	+70	°C
Storage temperature	TSTOR	-55	+150	°C

CAUTION

Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4: DC Characteristics (TA=0 to 70 °C, VCC=±5%, GND=0 V)

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
High level input voltage	VIH	70	--	--	% of VCC	
Low level input voltage	VIL	--	--	30	% of VCC	
High level output voltage	VOH	2.4	4.5	--	V	IOH = 4 mA VDD = 4.75 V
Low level output voltage	VOH	--	0.2	0.4	V	IOH = 4 mA VDD = 4.75 V
Input leakage current	IIL	--	--	10	µA	VDD = 5.25 V
Three state leakage current	IHZ	-10	1	10	µA	VDD = 5.25 V
Power dissipation 4E1/E2 mode 4E2/E3 mode	PD		 100 500		 mW mW	 VDD = 5.25 V VDD = 5.25 V
Static current	IDD	--	1	20	µA	VDD = 5.25 V

AC TIMING SPECIFICATIONS

NOTE

Unless otherwise specified, all timing specifications are referenced at ambient condition as $T_{Ambient}$ = 0° to 70°C, VCC = ±5%, GND = 0V.

Figure 7: HDB3 Encoder and Decoder Timing (Refer to Table 5)

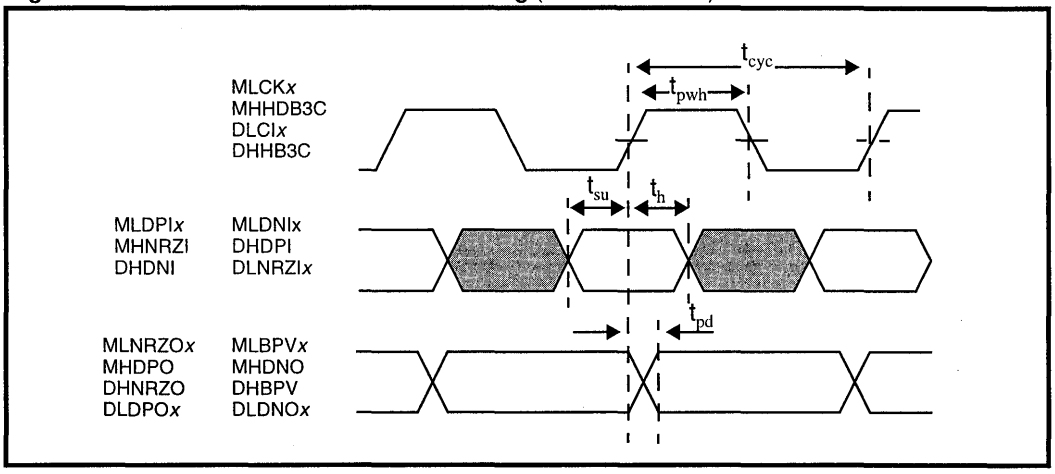


Table 5: HDB3 Encoder and Decoder (Refer to Figure 7)

Parameter	Symbol	Min	Typ	Max	Unit
Clock duty cycle	tPWH	40	--	75	%
Data to clock setup time	tSU	5	--	--	ns
Data to clock hold time	tH	6	--	--	ns
Clock to data propagation time (50pF capacitive load)	tPD	--	15	25	ns

Figure 8: Multiplexer Tributary Input Timing (Refer to Table 6)

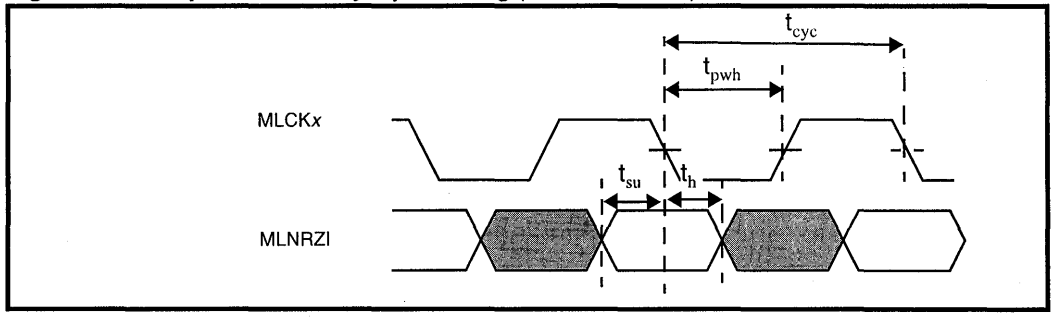


Table 6: Multiplexer Tributary Input (Refer to Figure 8)

Parameter	Symbol	Min	Typ	Max	Unit
Clock duty cycle	t_{PWH}	40	--	60	%
Data to clock setup time (falling edge)	t_{SU}	5	--	--	ns
Data to clock hold time (falling edge)	t_H	5	--	--	ns

Figure 9: High Speed Multiplexer Input & Output Timing (Refer to Table 7)

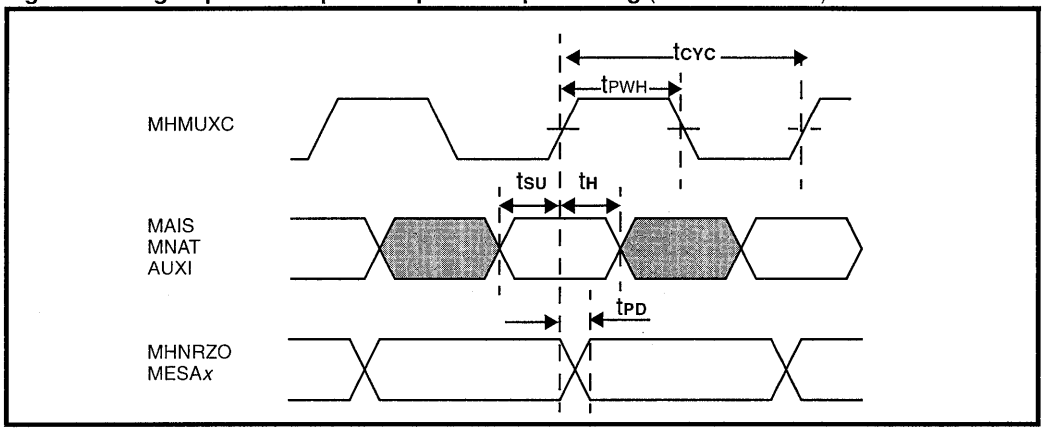


Table 7: High Speed Multiplexer Input & Output (Refer to Figure 9)

Parameter	Symbol	Min	Type	Max	Unit
Clock duty cycle	t_{PWH}	40	--	60	%
Data to clock setup time	t_{SU}	5	--	--	ns
Data to clock hold time	t_H	6	--	--	ns
Clock to data propagation time	t_{PD}	--	20	30	ns

Figure 10: High Speed Demultiplexer Input & Output Timing (Refer to Table 8)

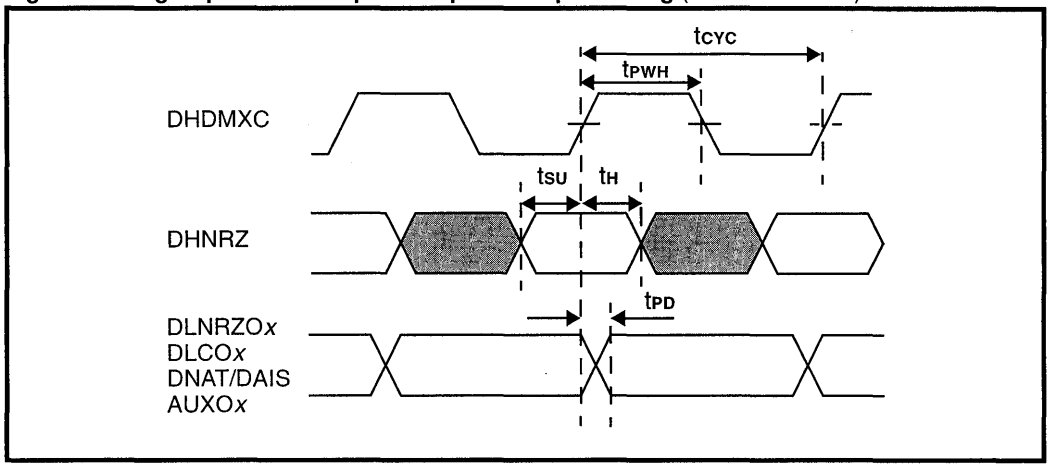


Table 8: High Speed Demultiplexer Input & Output (Refer to Figure 10)

Parameter	Symbol	Min	Type	Max	Unit
Clock duty cycle	tPWH	45	--	75	%
Data to clock setup time	tSU	8	--	--	ns
Data to clock hold time	tH	5	--	--	ns
Clock to data propagation time	tPD	--	20	30	ns

Figure 11: Chip Enable Timing (Refer to Table 9)

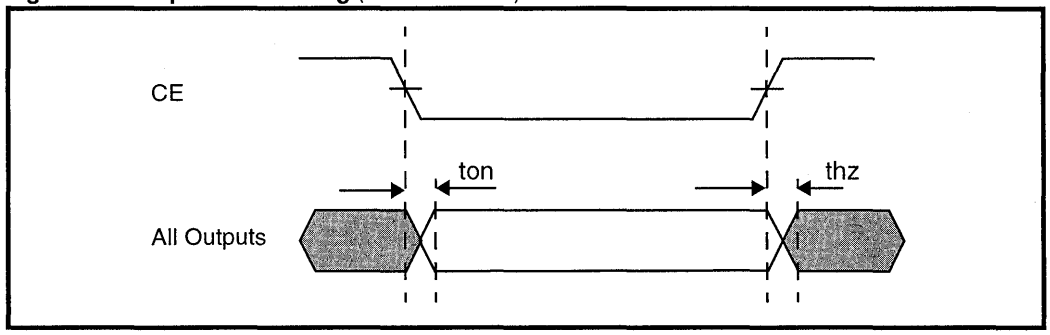


Table 9: Chip Enable (Refer to Figure 11)

Parameter	Symbol	Min	Type	Max	Unit
CE to outputs enabled	tON		20	30	ns
CE to outputs high impedance	tPWH		20	30	ns

Telecom Application Notes

APRIL 1996
Revision 0.0

LXT304A Transceiver

D4 Channel Bank Applications

General Description

Existing D4 Channel Bank architectures frequently employ: (1) a plug-in card for T1 pulse generation (6.0 V peak); and (2) a separate card for pulse shaping and Line Build-Out (LBO). The LXT304A integrates the functions of both cards on a single chip producing a DSX-1 compatible, 3.0 V peak output pulse with a standard transformer. In new designs, the LXT304A can replace two cards with one. However, the LXT304A is also compatible with existing dual-card architectures. With an appropriate output transformer, the LXT304A can produce full 6.0 V peak amplitude pulses suitable for D4 Channel Bank applications with separate pulse shaping/LBO cards.

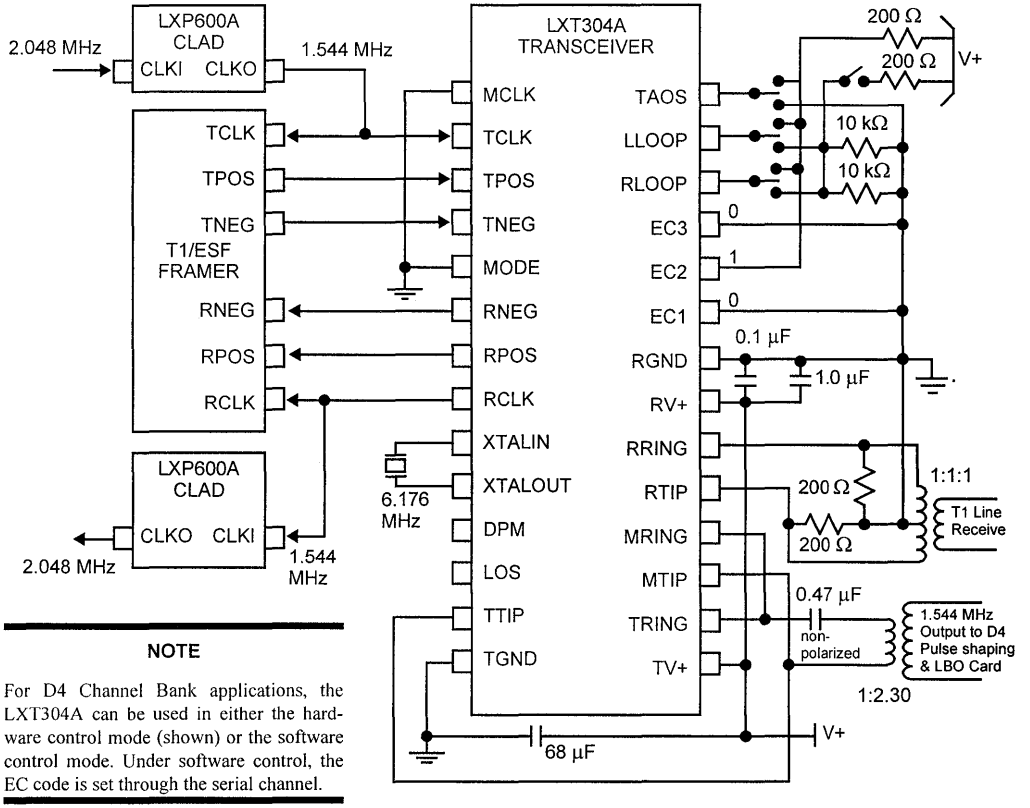
Line Interface Circuitry

To achieve the 6.0 V peak output, the FCC Part 68-010 Equalizer Code setting is used (EC = 010). With the standard 1:1.15 transformer, this code produces a 3.0 V peak pulse. However, doubling the transformer turns ratio to 1:2.30 produces the desired 6.0 V peak pulse.

The Application Diagram shows a D4 Channel Bank application circuit using the correct Equalizer Code setting and transformer. Transformer specifications are listed in Table 1.

NOTE: Typical pulse undershoot = 30% (±10%).

Application Diagram



NOTE

For D4 Channel Bank applications, the LXT304A can be used in either the hardware control mode (shown) or the software control mode. Under software control, the EC code is set through the serial channel.

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Table 1: Transformer Specifications

Parameter	Value
Turns Ratio	1:2.3 (±2%)
Primary Inductance	1.2 mH min
Leakage Inductance	0.5 µH max
Interwinding Capacitance	25 pF max
Series Resistance	1.0 Ω PRI

Vendors supplying suitable transformers include Pulse Engineering, Bel Fuse, Midcom and Schott.

Application circuit functionality was confirmed using a Pulse Engineering PE65558 transformer.

APRIL 1996
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LXT300 and LXT310 Interchangeability

Adapting Short-Haul T1 Boards to Long-Haul Applications

General Description

While the LXT300 is designed for short-haul (up to 200 m) T1/E1 applications and the LXT310 is designed for long-haul (up to 2 km) T1 applications, these transceivers are quite similar in function. There are only minor differences in line interfaces and pin configurations. Therefore, T1 equipment designed for short-haul applications (using the LXT300) can easily be adapted to provide long-haul capability (using the LXT310) as an option. This application note describes the steps necessary to adapt a single design so that it can be used for both long-haul and short-haul applications.

Functional Differences

- In the hardware Mode, thee Equalizer inputs on the LXT300 are replaced by two LBO inputs and an NLOOP output on the LXT310. These pins are identical in the Software Mode, but the bit register is defined differently.
- The LXT300 uses two inputs and an output for the Driver Performance Monitor (DPM) function. On the LXT310, these pins are replaced by inputs for Jitter Attenuation Select (JASEL) and Equalizer Gain Limitation (EGL), and an output for Line Attenuation (LATN).
- The LXT300 uses a 1:2 transformer for both the Tx and Rx line interfaces. The LXT310 uses a 1:2 transformer with two 12.5 Ω series resistors for the Tx line interface; it uses a 1:1 transformer for the Rx line interface.

Circuit Modifications

To adapt an LXT300 board to accommodate the LXT310, modify the circuit as follows:

1. Cut the DPM output trace from LXT300 pin 11, and tie the LXT310 JASEL input to VCC.
2. Cut the MTIP and MRING inputs to LXT300 pins 17 and 18. Reconfigure the LXT310 input at pin 17 to allow EGL switching, or simply tie pin 17 to ground. Connect the LXT310 output from pin 18 to a LATN decoding circuit.
3. Cut the EC1 input to LXT300 pin 23, and connect the LXT310 output from this pin to NLOOP monitoring circuitry.

Line Interface Modifications

On the transmit side, both the LXT300 and LXT310 use a 1:2 transformer. The LXT300 transformer connects directly to the chip as shown in Figure 1a. The LXT310 requires two 12.5 Ω serial resistors in line with the transformer, as shown in Figure 1b.

On the receive side, the LXT300 uses a 1:2 transformer with 400 Ω termination, as shown in Figure 2a. The LXT310 uses a 1:1 transformer with 100 Ω termination, as shown in Figure 2b.

(A 1:2 CT transformer can be used for both devices. For LXT310 boards, connect only one of the secondary windings, an effective 1:1 ratio.)

Figure 1: Transmit Line Interface

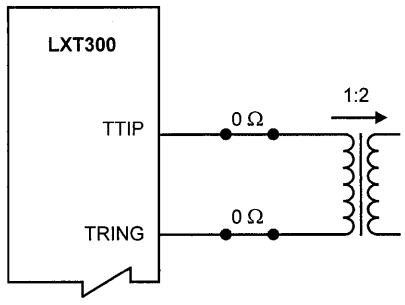

Figure 1a: LXT300 Transmit Line Interface

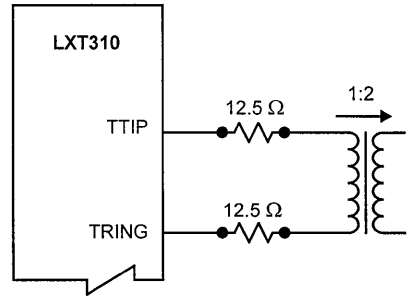

Figure 1b: LXT310 Transmit Line Interface

Figure 2: Receive Line Interface

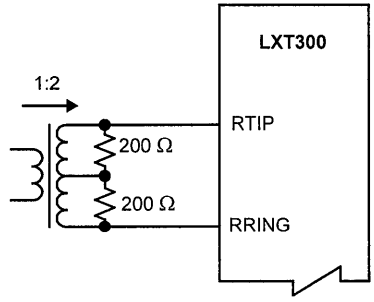

Figure 2a: LXT300 Receive Line Interface

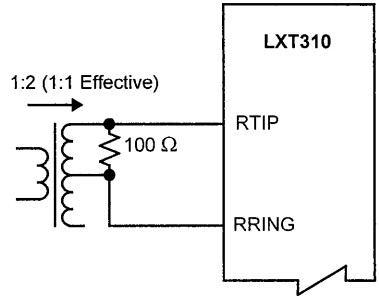

Figure 2b: LXT310 Receive Line Interface

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Revision 0.0

LXT310 Line Protection Circuitry

Application Guidelines

General Description

This application note provides guidelines for line protection circuitry required in network channel termination equipment (NCTE) Channel Service Units (CSU) and WAN network interfaces, typical LXT310 applications. NCTE is installed at the customer premises end of T1 lines. As these lines run between the customer facilities and the central office, they are subject to over voltage/current stresses from lightning strikes, power crosses, and other noise impairments. Protection circuitry is required to protect the line from injected impairments and the termination equipment (CSU, MUX, PBX, etc.) from overload stresses.

NOTE: protection requirements are specified in FCC Part 68 (lightning hazards), UL 1459 (AC hazards), Bellcore TR-TSY-000007 and AT&T Pub 62411. These documents differentiate between longitudinal stress (differential between tip/ring and ground) and metallic stress (differential between tip and ring). Longitudinal stresses are more common and include impulsive noise events such as lightning induced surges. Metallic stresses are less likely and are usually caused by power crosses during maintenance activity.

Since T1 acceptance testing does not meet formal FCC and safety requirements, the final board design should undergo this FCC testing at an approved lab.

Protective Circuitry

The figure below shows a typical LXT310 line interface.

- Resistors R1, 2, 3, 12, 13 (in the transmit and receive lines) values are selected to match the line impedance. They also provide some current limitation
- Positive Temperature Co-efficient Resistors (PTCs) (R10, 11, 16, 17) permit ìhealingî after an over-voltage event
- 5.6 Ω resistors and PTCs matched to T1 Line requirements using receive resistor pad and 2:1 transformers
- Line transformers T1 and T2 breakdown ratings should be a minimum of 1.5 kV
- Varistors must have sufficient stand-off voltage to allow normal operation (approximately 4 volts), with low off-state capacitance (< 50 pF)
- Final values for RF chokes, L1, 2, will vary with board design
- Interconnect the line side center taps of the line transformers if sealing currents are present
- No power or ground planes should be located on the circuit board in the area T1 Line connector back to the transformers

Suggested component values are listed in Table 1.

LXT310 Protection Circuitry

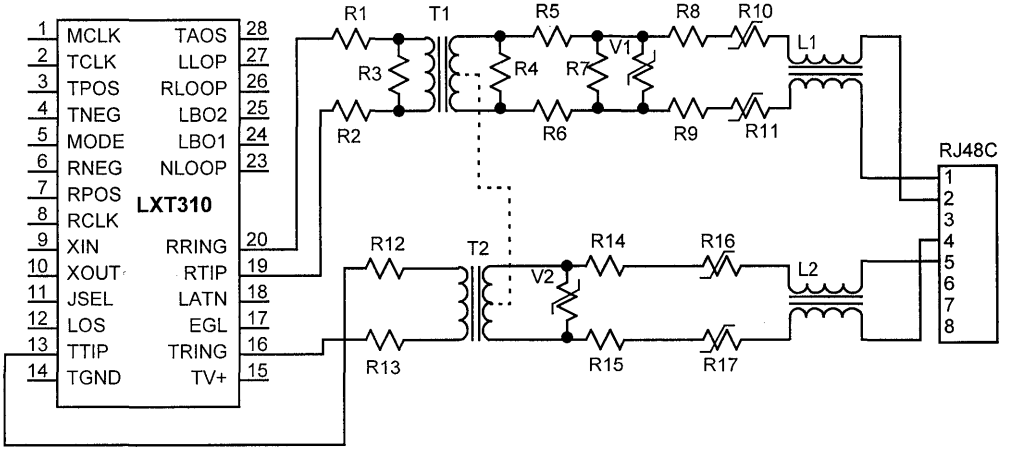

Table 1: Component Values

Ref #	Description
R1,2	100 Ω
R3	402 Ω, 1%
R4	301 Ω, 1%
R5, 6	22 Ω, 2W
R7	232 Ω
R8, 9	5.6 Ω, 1W
R10, 11 R16, 17	8.5 Ω, 600 V, positive temperature co-efficient resistor – typical: Raychem 21214B
R12, 13	6.8 Ω, 1/2 W
R14, 15	5.6 Ω, 1 W
V1, 2	Stand-off voltage 4~4.5 V, off-state capacitance < 50 pF – typical: EDAL Industries B529-2
T1, 2	Line transformer, 1:2 turns ratio – typical: Pulse Engineering PE65351
L1, 2	RF Choke, value varies by board design, approximately 33 µH – typical: BH Electronics 500-1164

Table 2: Suppliers

Company	Telephone Number
Raychem, Inc.	(800) 272-2436 ext 6900
Pulse Engineering	(619) 674-8130
EDAL Industries	(203) 467-2591
BH Electronics	(612) 894-9590

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LXT30x Transceiver/Framer Interface

Application Guidelines for Use with Mitel MT8976 and MT8979 Framers

General Description

This application note provides guidelines for interfacing the Level One LXT300 series (LXT300Z, 301Z, 304A and 305A) transceivers with Mitel framers in both T1 and E1 applications. Only minimal circuitry is required to implement the interface. For T1 (1.544 Mbps) applications, the transmit data pins may be connected directly between the two chips as shown below. A single 4-gate NAND package provides the signal inversion required on the receive side.

Receive-side signal inversion is also required for E1/CEPT (2.048 Mbps) applications. A similar setup using NAND gates in an E1 application is shown in Figure 1. Additional circuitry is also required to synchronize the transmit data stream in E1 applications. This synchronization is easily implemented with a pair of D-flip-flops, clocked by the common 2.048 MHz transmit clock.

LXT30x Interface to MT8976 T1 ESF Framer

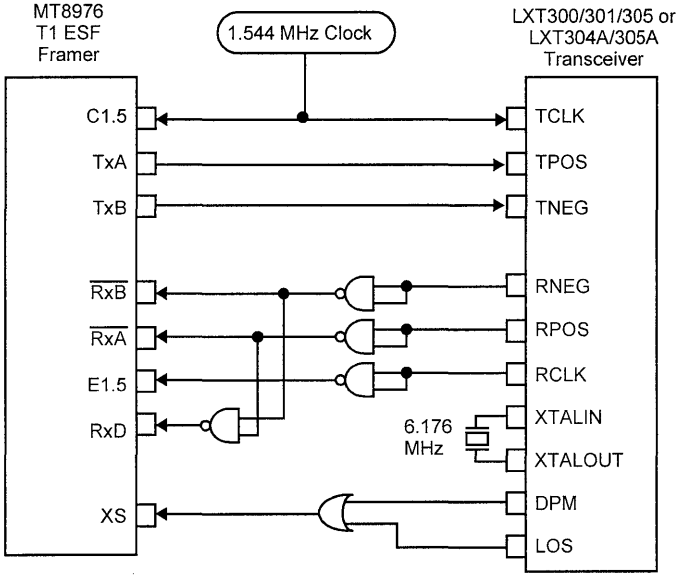
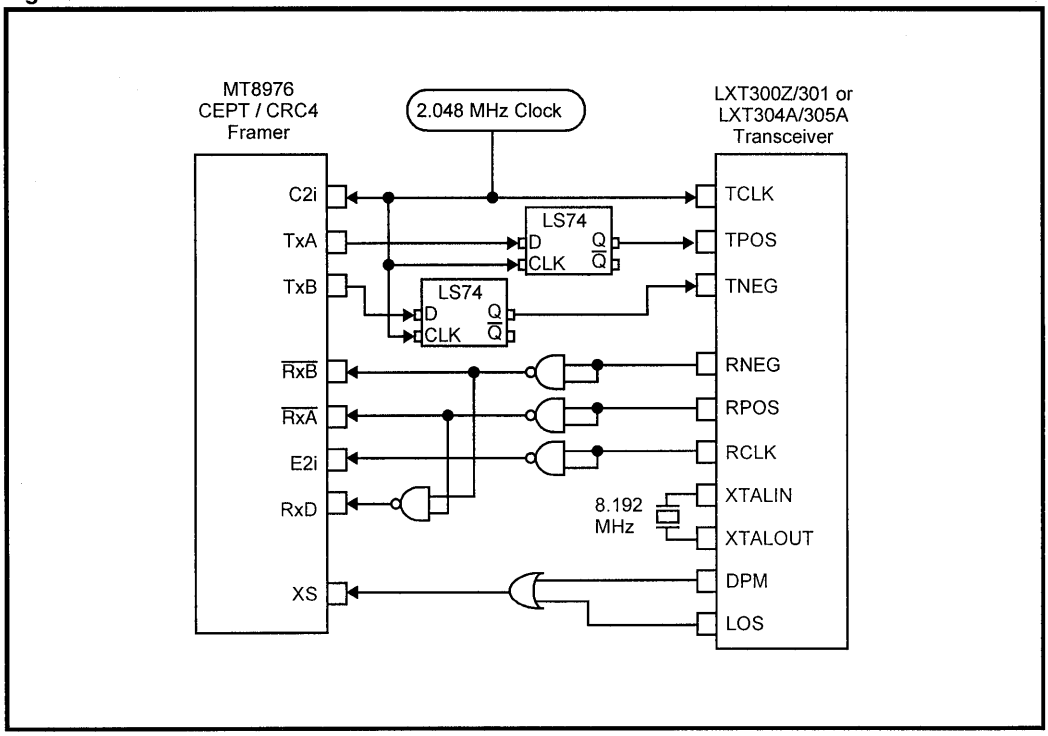


Figure 1: LXT300 Interface to MT8979 E1 CRC Framer



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LXT318 Long-Haul E1 Transceiver Solution

Migration from Dual-Chip (LXT304A/LXT316) to Single-Chip (LXT318) Implementation

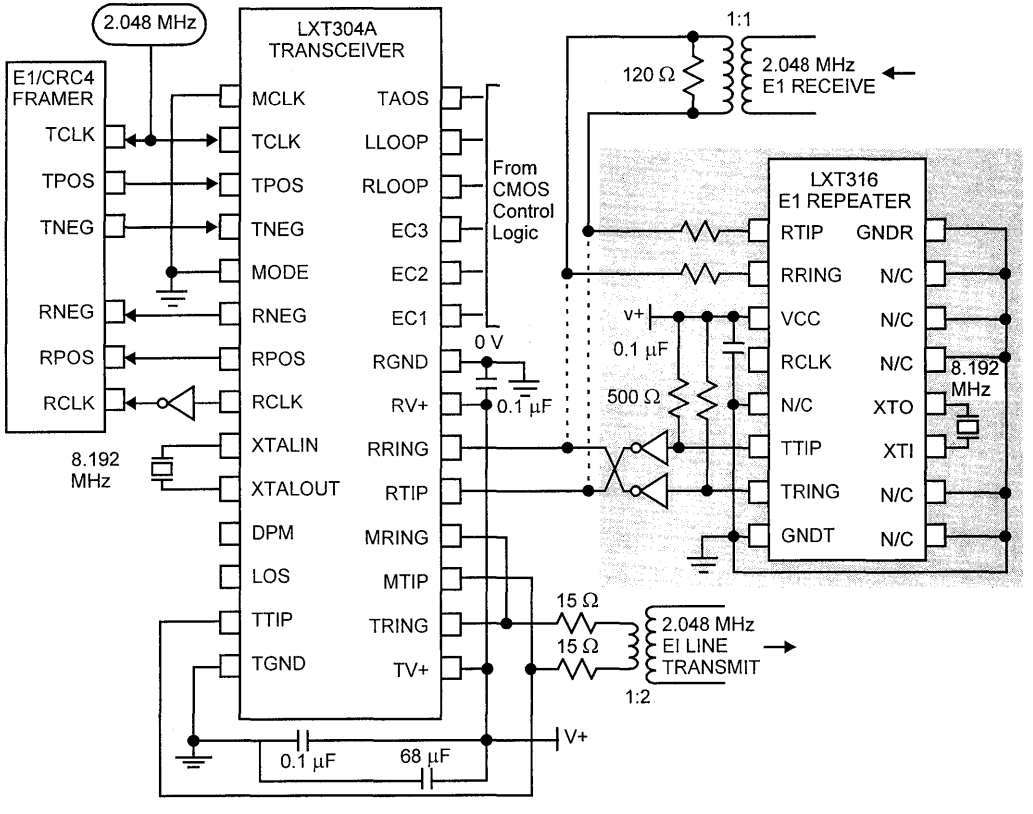
Introduction

This application note provides manufacturers of long-haul E1 (2.048 Mbps) transmission equipment with a smooth transition from Level One's LXT304A/316 dual-chip long-haul E1 solution to an advanced single-chip implementation, the LXT318.

There are only minor differences in the line interfaces for single- and dual-chip solutions. Therefore, E1 equipment designed around the dual-chip solution (using the LXT304A and LXT316) can easily be adapted to take advantage of the fully integrated LXT318.

This application note describes the steps necessary to modify a dual-chip design for use with the LXT318. Both solutions use the same transformers. The modification involves removing the repeater and associated circuitry (shown in the shadowed area of the figure below).

Long-Haul E1 2-Chip Solution



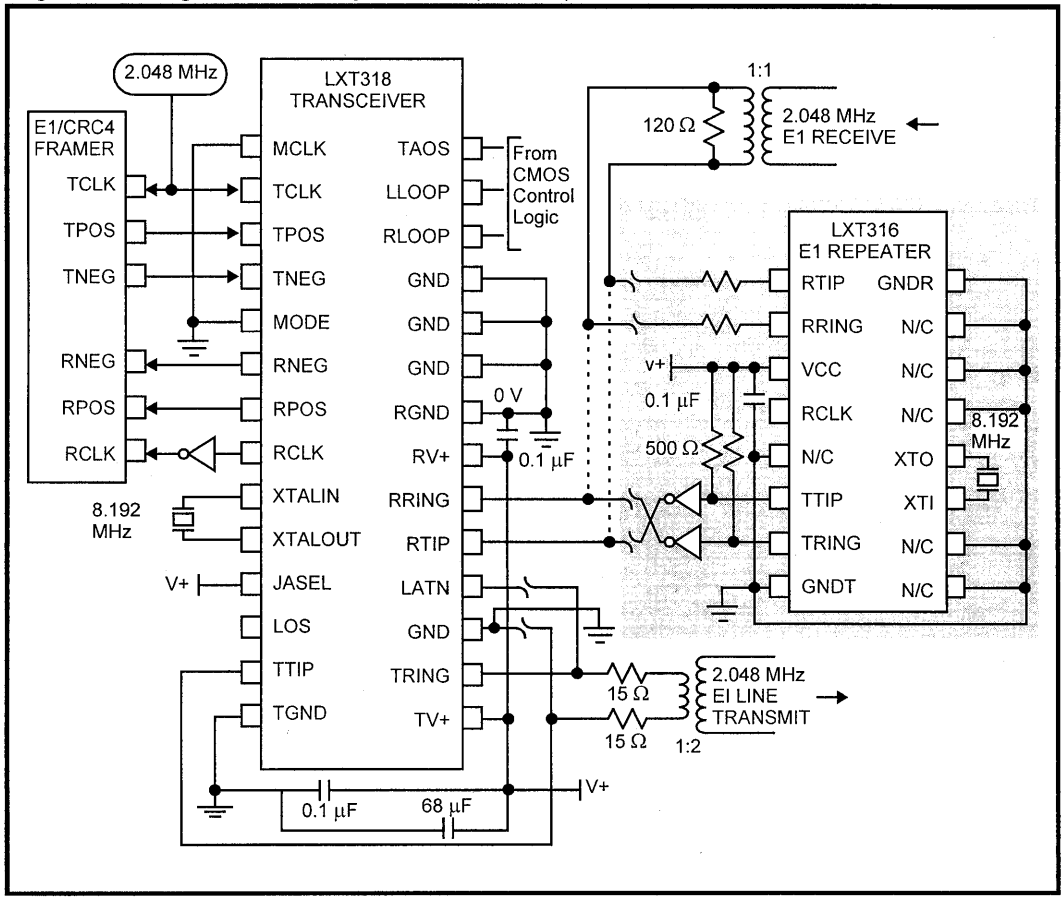
Functional Differences

- In Hardware Mode, the LXT304A uses three Equalizer Control inputs (EC1, EC2 and EC3), and two transmit driver monitor inputs (MTIP and MRING). These functions are not provided on the LXT318. On the LXT318, pins 17, 23, 24 and 25 must be tied to ground. LXT318 pin 18 is now the coded line attenuation (LATN) output.
- On the LXT318, pin 11 is used as an input for Jitter Attenuation Select (JASEL). It should be tied to VCC or ground, as desired.

Circuit Modifications

1. To modify a 2-chip long-haul PCB for use with the LXT318, cut the EC1, 2 and 3 inputs to LXT304A (pins 23, 24 and 25). Tie these three pins to ground.
2. Cut the MTIP and MRING inputs to LXT304A pins 17 and 18. Tie pin 17 to ground. Tie pin 18 to an LATN decoding circuit or let it float.
3. Cut the DPM output trace from LXT304A pin 11, and tie the LXT318 JASEL input to VCC (for receive jitter attenuation) or to ground (for transmit jitter attenuation).
4. Remove all the circuitry shown in the shadowed area of Figure 1 and connect the receive transformer to pins 19 and 20 of the LXT318.

Figure 1: Long-Haul E1 1-Chip Solution (LXT318)



T1 Jitter Performance Measurement

AT&T Pub 62411 Certification

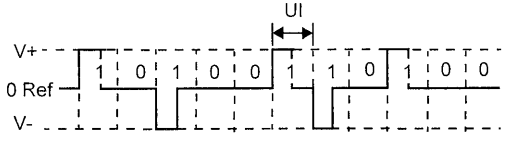
General Description

This application note provides a brief definition of jitter and then summarizes jitter performance requirements and measurement techniques specified for T1 (1.544 Mbps) Customer Premises Equipment (CPE).

Requirements for T1 systems are specified by AT&T Publication 62411, December 1990 - Accunet T1.5 Service Description and Interface Specification. (Similar requirements for E1 systems are specified by CCITT G.823 - The Control of Jitter and Wander within Digital Networks.)

Understanding Jitter

T1 signals are composed of square-wave pulses as shown below. A "1" is represented by a positive or negative pulse (the pulses alternate in polarity). A "0" is represented by the absence of a pulse. To enhance timing and data recovery, the duration of a "1" pulse is constrained to 1¦2 of the bit rate period. Deviations in time between when the pulse transitions occur and when the decoding circuits expect them to occur are referred to as jitter. Very low-frequency deviations (< 10 Hz) are referred to as wander. These deviations are equivalent to unintentional phase modulation. Any pulse that is phase-shifted by more than 50% will be sampled incorrectly.



Jitter is measured in Unit Intervals (UIs). A UI is equal to the bit rate period. A UI is, therefore, the reciprocal of the frequency. For T1 service, a UI equals 648 ns, while the "1" pulse duration is 324 ns. Jitter amplitude is measured in UI pp (peak-to-peak). Jitter specifications have both an amplitude component and a frequency component; that is, for a given jitter parameter, performance will be specified at a particular amplitude (in UI pp) within a particular frequency band.

Types of Jitter

There are three parameters of jitter performance which are specified and measured:

1. Input Jitter Tolerance (Jitter Accommodation)
2. Output Jitter Generation (Intrinsic Jitter)
3. Jitter Transfer (Jitter Attenuation)

Input Jitter Tolerance. Input jitter tolerance is defined as a system's ability to recover input data correctly in the presence of jitter. This value indicates how much input jitter a system or device can handle before bit errors occur. Individual devices should have as high a tolerance value as possible because the system's jitter tolerance is limited to the tolerance of its most restrictive element. Input jitter tolerance is also referred to as jitter accommodation.

Output Jitter Generation. Output jitter is defined as the amount of jitter generated in the system output when zero jitter is present in the input. Essentially, it is a measure of how "noisy" the system is. Individual system elements should have as low a value as possible because output jitter is additive. Each device in a system adds its own intrinsically generated jitter to the system total, hence the term "jitter budget." Output jitter is also referred to as intrinsic jitter or additive jitter.

Jitter Transfer. Jitter transfer, frequently referred to as jitter attenuation (JA), is defined as the percentage of input jitter which is present in the system output, expressed in dBs. While a certain amount of jitter attenuation is desirable, excessive jitter attenuation can cause problems with frame slippage and synchronization. Therefore, jitter attenuation specifications define an acceptable range of values for a given jitter frequency. (Jitter attenuation circuits typically use an elastic store as a buffer between input and output. Buffer size is directly related to throughput delay. Oversize buffers intended to maximize jitter attenuation may cause equipment to fail requirements for maximum throughput delay.)

AT&T PUB 62411 Compliance Testing

Jitter performance is strongly related to the transmitted bit pattern. AT&T Publication 62411 defines a standard quasi-random test signal (QRTS) used for jitter testing at 1.544 Mbps. The QRTS bit pattern is designed to simulate typical transmission patterns. Jitter performance testing should be conducted in a noise-free environment to eliminate, as far as possible, the effect of other factors on the performance of the device under test.

Input Jitter Tolerance Testing

The input jitter tolerance of a DTE is characterized by determining the level of jitter required to induce bit errors in a 60-second interval. At frequencies up to 10 kHz, one bit error is allowed. At higher frequencies, up to 5 errored bits are allowed in a 60-second period. (Synchronizers, which provide a system master clock, are held to a tighter spec. They are characterized by determining the level of jitter required to induce a loss of synchronization.) Jitter tolerance is tested at a number of spot frequencies to ensure full characterization across the spectrum. Figure 1A shows the jitter tolerance template for DTE. Figure 1B shows the jitter tolerance template for synchronizers.

Figure 1: Input Jitter Tolerance Specified by AT&T Publication 62411

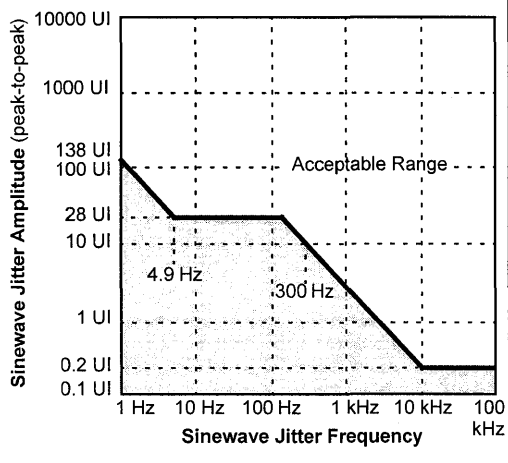


Figure 1A: Jitter Tolerance Template for DT

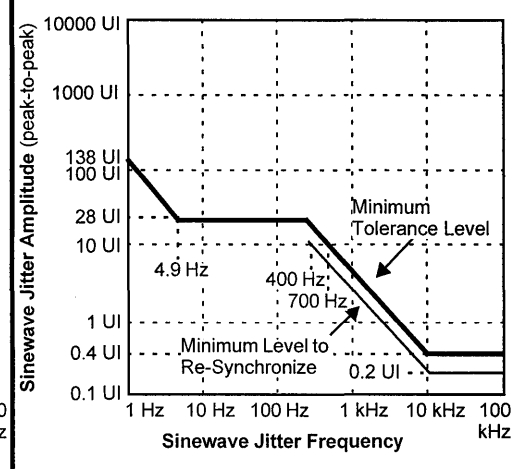


Figure 1B: Jitter Tolerance Template for Synchronizers

Jitter Tolerance Test Procedures

5. Connect the test equipment as shown in Figure 2.
6. Configure the device under test for remote loopback.
7. With its modulation input turned off, configure the RF signal generator for an appropriate output level to drive the external clock input of the BER, through an AC-coupled driver as shown in Figure 2. Test this jitter-free external clocking of the BER with the unit under test.
8. Enable the External FM Modulation mode of operation on the HP8656B.
9. Set the Frequency Synthesizer to the first jitter frequency to be tested. Set the amplitude of this sine wave frequency such that the high/low input LEDs on the HP8656B are off (approximately 2.1 V pp).

10a. DTE Testing. While observing the transmission tester for bit error indications, adjust the modulation index on the signal generator to the level required to produce the minimum error level. (For example, if the synthesizer is set for a jitter frequency of 10 Hz, adjust the modulation index as required to produce no more than one bit error in any 60-second period.)

10b. Synchronizer Testing. While observing the transmission tester for clock slips (loss of sync), adjust the modulation index on the signal generator to the level required to produce the loss of sync. Then, reduce the modulation index to the level required to achieve resynchronization. Record both values.

11. Determine the jitter tolerance using the formula:

$$UIpp = {}^{\Delta f}/_{\pi}\ fm$$

where fm = Jitter Frequency
(synthesizer modulation frequency), and

where Δf = FM Modulation Index
(as set on the signal generator).

for example,

$${}^{38\ kHz}/_{\pi} \cdot 10\ Hz = 1209\ UIpp\ @\ 10\ Hz$$

12. Repeat steps 5 through 7 for additional frequencies to be tested and plot the results as shown in Figure 3.

Figure 2: Input Jitter Tolerance Test Setup

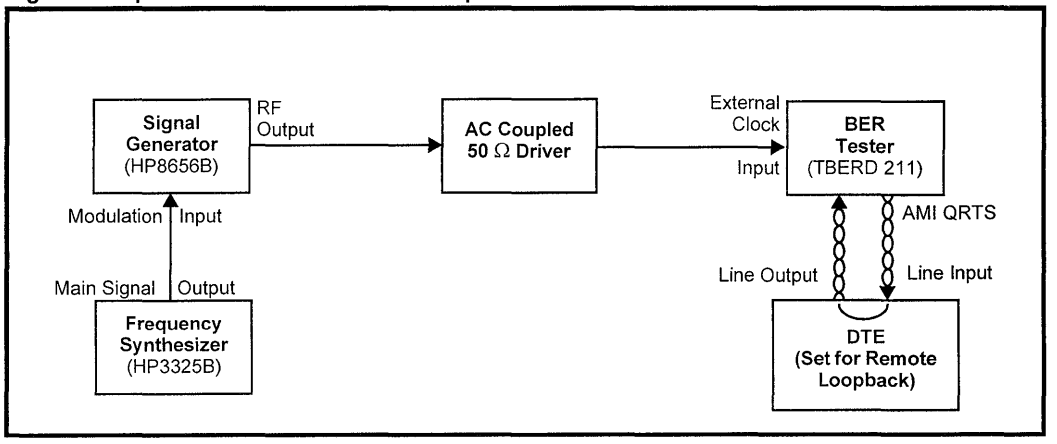


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Figure 3: Charting Input Jitter Tolerance Test Results

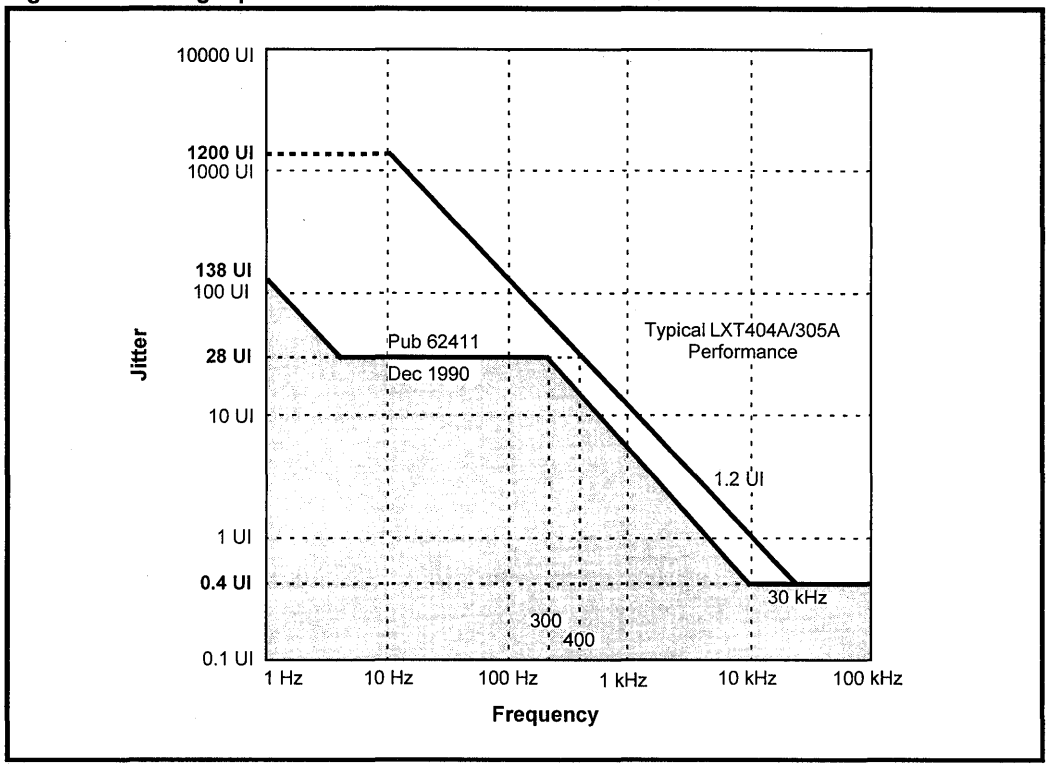
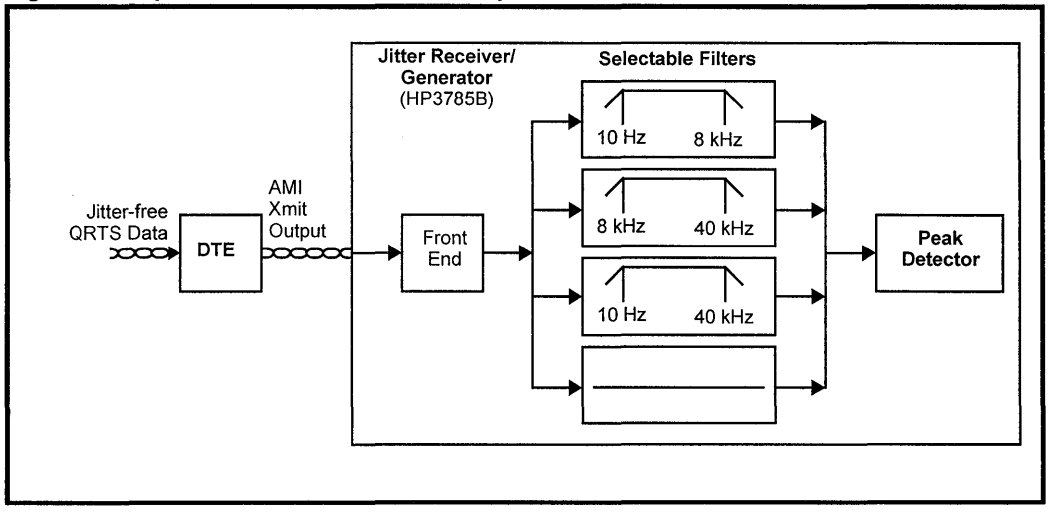


Figure 4: Output Jitter Generation Test Setup



Output Jitter Generation Testing

The intrinsic jitter generated by a DTE is characterized by configuring the device for remote loopback and then monitoring the line output when no jitter is present in the line input. AT&T Publication 62411 lists maximum output jitter values for three separate frequency bands, as well as a fourth value for the unlimited broadband output. Output jitter may be measured with a variety of instruments including peak detectors, true RMS voltmeters and spectrum analyzers. Figure 4 shows a typical test setup. Table 1 lists the maximum generated jitter allowed in each frequency band, as well as sample test measurements.

Output Jitter Generation Test Procedures

1. Connect a frequency synthesizer, signal generator and telecom tester to produce a jitter-free QRTS output. Figure 2 may be used as a reference.
2. Select the filters in the HP3785B as shown in Figure 4 and monitor the first frequency band.
3. Measure and record the output jitter peak values.
4. Repeat steps 2 and 3 for each remaining band.

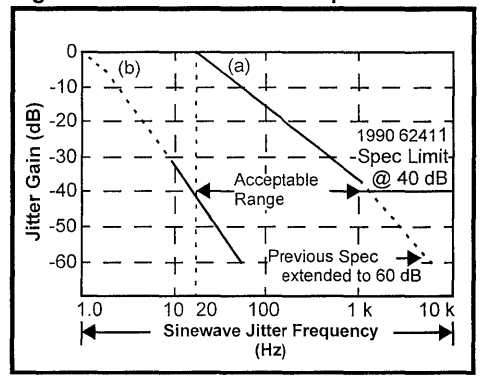
Table 1: Output Jitter Generation Specification

Frequency Band	62411 Specified Maximum	Typical 304A Performance
10 Hz - 8 kHz	0.02 UI (0.8 mV rms)	0.002 UI
10 Hz - 40 kHz	0.025 UI (1.25 mV rms)	0.016 UI
8 kHz - 40 kHz	0.025 UI (1 mV rms)	0.014 UI
No Bandlimiting	0.05 UI (2 mV rms)	0.025 UI

Jitter Attenuation Testing

Jitter attenuation is defined as the percentage of input jitter which is present in the system output, expressed in dBs. While a certain amount of jitter attenuation is desirable, excessive jitter attenuation can cause problems with frame slippage and synchronization. Therefore, jitter attenuation specifications define an acceptable range of values for a given jitter frequency as shown in Figure 5. (Jitter attenuation circuits typically use an elastic store as a buffer between input and output. Buffer size is directly related to throughput delay. Oversize buffers may cause equipment to fail requirements for maximum throughput delay.) Jitter attenuation is also referred to as jitter transfer.

Figure 5: Jitter Transfer Template



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Jitter Attenuation Test Procedures

1. Connect the test equipment as shown in Figure 8.
2. Set the frequency synthesizer to produce a square wave reference clock at 1.544 MHz.
3. Set the jitter generator as follows:
   a. Frequency: lowest frequency to be tested
   b. Amplitude: 75% of the level shown in Figure 1 (use appropriate DTE or Synchronizer template.)
4. Set the spectrum analyzer as follows:
   a. Center Frequency: same as 3a.
   b. Frequency Span: 200 Hz - 500 Hz.
5. Set the reference level (UIinp) on the spectrum analyzer by temporarily connecting the BERT transmit output directly into the data input of the jitter receiver/generator.
6. Re-connect the test equipment as shown in Figure 8 and set the synthesizer to the first jitter frequency to be tested.
7. Observe the spectrum analyzer (Figure 6) and record the difference between the reference level, UIinp, and the DTE line output level, UIout.
8. Repeat steps 3 through 7 for each frequency to be tested and plot the results as shown in Figure 7.

Figure 6: Spectrum Analyzer Display

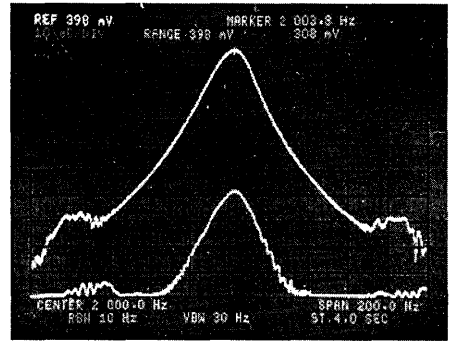


Figure 7: Typical LXT304A JA Performance

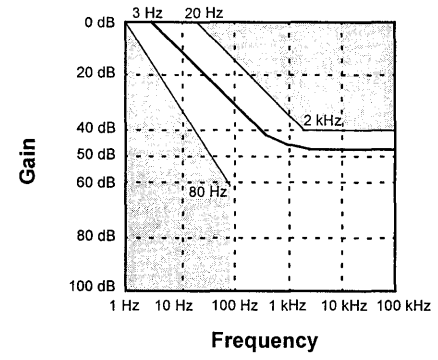
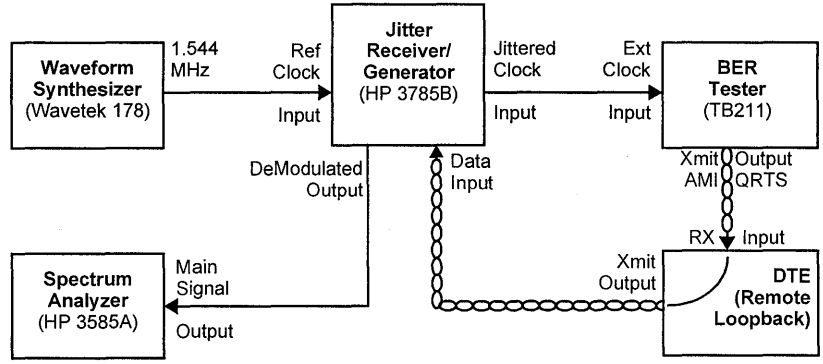


Figure 8: Jitter Attenuation Test Setup



NOTE: The test setup shown in Figure 8 is used to measure jitter amplitudes less than 10 UI (the limit of the HP3785B). Alternate test setups should be used for other jitter amplitudes or amplitude/frequency combinations.

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LXT30x and LXT318 Interchangeability

Adapting Short-Haul T1/E1 Boards to Long-Haul Applications

General Description

While the LXT300, 304A and 305A are designed for short-haul T1/E1 applications (up to 14 dB) and the LXT318 is designed for long-haul E1 applications (up to 43 dB), these transceivers are quite similar in function. There are only minor differences in line interfaces and pin configurations. Therefore, E1 equipment designed for short-haul applications (using LXT30x series transceivers) can easily be adapted to provide long-haul capability (using the LXT318). This application note describes the steps necessary to adapt a short-haul design so that it can be used for both long-haul and short-haul applications. (The LXT318 can support both E1 long-haul and E1 short-haul applications.)

Functional Differences

- The LXT30x uses three Equalizer inputs in the Hardware Mode. These pins are not used by the 318 and should be tied to ground. These pins are identical in the Software mode, but the bit register is defined differently.
- The LXT30x uses two inputs and an output for the Driver Performance Monitor (DPM) function. On the LXT318, these pins are replaced by an input for Jitter Attenuation Select (JASEL) and an output for Line Attenuation (LATN).
- The LXT30x uses a 1:2 transformer for both the Tx and Rx line interfaces. The LXT318 uses a 1:2 transformer with two 15 Ω series resistors for the Tx line interface, and a 1:1 transformer for the Rx line interface.

Circuit Modifications

To adapt an LXT30x board to accommodate the LXT318, modify the circuit as follows:

1. Cut the DPM output trace from LXT30x pin 11 and tie the LXT318 pin 11 (JASEL) to VCC (to select receive jitter attenuation), or to GND (to select transmit jitter attenuation).
2. Cut the MTIP and MRING inputs to LXT30x pins 17 and 18. Connect the LXT318 input at pin 17 to ground. Connect the LXT318 output from pin 18 to a LATN decoding circuit.
3. For Hardware Mode, cut the EC inputs to LXT30x (pins 23, 24 and 25), and connect these LXT318 pins to ground.

Line Interface Modifications

On the transmit side, both the LXT30x and LXT318 use a 1:2 transformer. The LXT30x transformer connects directly to the chip as shown in Figure 1a. The LXT318 requires two 15 Ω series resistors in line with the transformer, as shown in Figure 1b.

On the receive side, the LXT30x uses a 1:2 transformer with 480 Ω termination, as shown in Figure 2a. The LXT318 uses a 1:1 transformer with 120 Ω termination for TWP applications, as shown in Figure 2b.

(A 1:2 CT transformer can be used for both devices. For LXT318 boards, connect only one of the secondary windings, an effective 1:1 ratio.)

Figure 1: Transmit Line Interface

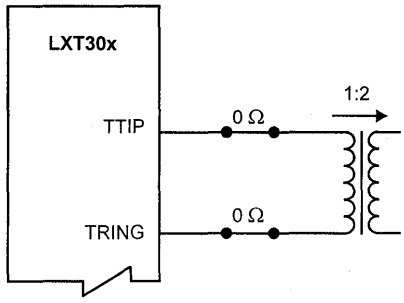


Figure 1a: LXT30x Transmit Line Interface

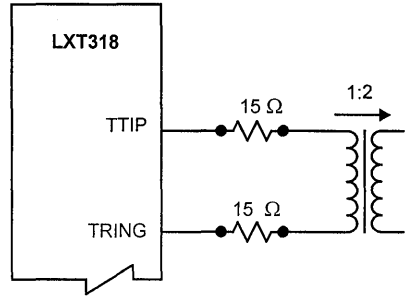


Figure 1b: LXT318 Transmit Line Interface

Figure 2: Receive Line Interface

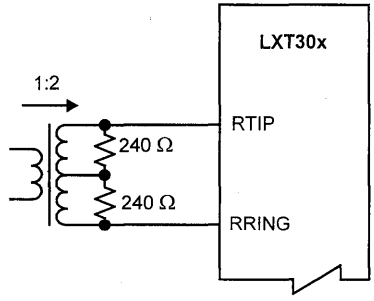


Figure 2a: LXT30x Receive Line Interface

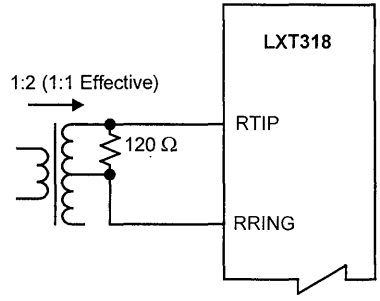


Figure 2b: LXT318 Receive Line Interface

LXT318 Long-Haul E1 Transceiver

Line Interface Design Guide

General Description

This application note describes a standard line interface for the LXT318 transceiver in a long-haul E1 environment. The interface uses two Pulse Engineering transformers designed specifically for this transceiver.

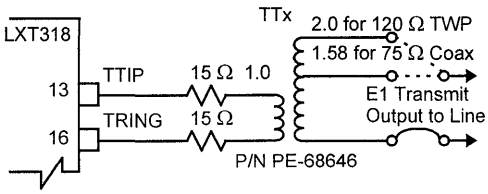
The design is simple and robust and will reduce in-house engineering and testing time.

Refer to the current LXT318 data sheet for complete information on the LXT318 transceiver.

Line Interface Features

- Provides correct impedance match for both 75 Ω coaxial and 120 Ω twisted-pair cables
- Meets 3 kV isolation requirement of many PTT ministries
- Standard interface requires one-time design
- Laboratory engineered and proven design requires minimal in-house testing
- Readily available parts make building fast and easy

Transmit Line Interface



Transmit Line Interface

The transmit line interface uses the following parts:

1. Pulse Engineering transformer, P/N PE68646 - 1:1.58:2 (one per transceiver)
2. 15 Ω resistors (two per transceiver)

Connect them to the Transmit Tip and Ring inputs (pins 13 and 16) of the transceiver as shown above.

Twisted-Pair Cable (120 Ω)

For a twisted-pair cable, use the full 1:2 step-up ratio provided at the end tap. This gives the required 120 Ω impedance.

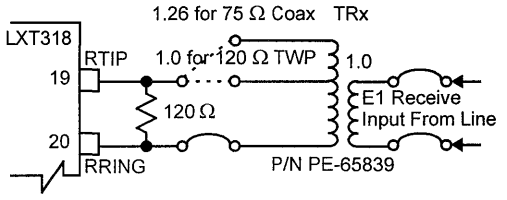
$Z = \Omega \times (\text{step-up ratio})^2 = (15\ \Omega + 15\ \Omega) \times 2^2 = 120\ \Omega$

Coaxial Cable (75 Ω)

For a coaxial cable, connect the circuit at the transformer center tap. The 1:1.58 step-up ratio gives a value within 0.2% of the 75 Ω impedance required.

$Z = \Omega \times (\text{step-up ratio})^2 = (15\ \Omega + 15\ \Omega) \times 1.58^2 = 74.89\ \Omega$

Receive Line Interface



Receive Line Interface

he receive line interface uses the following parts:

1. Pulse Engineering transformer, P/N PE65839 - 1:1:1.26 (one per transceiver)
2. 120 Ω resistors (one per transceiver)

Connect them to the Receive Tip and Ring inputs (pins 19 and 20) of the transceiver as shown above.

Twisted-Pair Cable (120 Ω)

For a twisted-pair cable, use the 1:1 step-down ratio provided at the center tap. This gives the required 120 Ω impedance

$$Z = \frac{\Omega}{(\text{set-down ratio})^2} = \frac{120\ \Omega}{(1)^2} = 120\ \Omega$$

Coaxial Cable (75 Ω)

For a coaxial cable, connect the circuit at the transformer center tap. The 1:1.26 step-down ratio gives a value within 1% of the 75 Ω impedance required.

$$Z = \frac{\Omega}{(\text{set-down ratio})^2} = \frac{120\ \Omega}{(1.26)^2} = 75.59\ \Omega$$

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NOTES

APRIL 1996
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LXT332 Dual Channel T1/E1 Transceiver Solution

Migration from Dual-Chip (Siemens PEB 2236) to Single-Chip (LXT332) Implementation

General Description

This application note provides manufacturers of multi-channel T1/E1 transmission equipment with a smooth upgrade from two Siemens PEB 2236 single-channel devices to an advanced implementation using a single LXT332 Dual Line Interface Unit (DLIU) integrated dual-channel device. This application note discusses Hardware Mode only.

There are some differences between the two devices in the back end and line interfaces. However, existing PEB 2236 designs can easily be adapted to take advantage of the fully integrated dual-channel LXT332 DLIU.

Advantages

- Meets or exceeds industry specifications including ANSI T1.403, ITU G.703 and AT&T Pub 62411
- Simplifies board design
- Crystal-less Jitter Attenuation
- Saves real estate
- Reduces inventory costs
- Improved jitter tolerance performance
- Improved return loss on both transmit and receive lines
- Reads switch settings dynamically in Hardware Mode
- No complicated reset conditions
- Transparent to ternary codes
- Single transformer turns ratio for both T1 and E1 applications
- Lower per-channel power consumption
- Additional features with Host Mode Serial I/O

Upgrade Issues

Upgrading from the PEB 2236 to the LXT332 DLIU requires minor framer interface modifications and some simple changes to the control circuitry. Specifically, the conversion requires removing the inverters on the data and control lines. In addition, the LXT332 DLIU includes internal jitter attenuation; any existing JA circuitry may not be necessary. The following paragraphs describe other differences between the two devices.

Tristate Output

The Tristate control forces all output pins to a high-impedance state. This is an especially valuable feature in applications such as in-circuit testing. The Siemens transceiver offers no similar operation.

AIS Generation

The LXT332 generates an AIS Alarm Signal when either TAOS0 or TAOS1 = 1. The PEB 2236 provides no comparable feature.

Reset Condition

On initial power up, the transceiver clears all internal registers, and does not require any external components or software control to establish a reset. The PEB 2236 requires one of three complex reset procedures.

Operating Temperatures

The LXT332 operates in the temperature range of 40 to 85 °C, exceeding the PEB 2236 operating range of 0 to 70 °C.

Return Loss

LXT332 device return loss for both the transmitter (if the design includes a capacitor) and receiver will exceed 20 dB. The Siemens device meets only minimum return loss specifications.

Line Length/Pulse Shape Control

Both the LXT332 and the PEB 2236 use 3-input codes to determine pulse shapes for various line lengths. Tables 1 and 3 show the two coding schemes.

Loopback Control

Both the LXT332 and the PEB 2236 provide RL and LL as shown in Tables 2 and 4. The LXT332 has an additional dual loopback capability.

Loss of Signal (Receive Line)

Both the LXT332 and the PEB 2236 provide Loss of Signal (LOS) outputs on the receive side. The internal detection circuitry which determines when an LOS condition exists is functionally different. The LXT332 provides both digital and analog LOS detection.

Transmit Driver Monitor

The LXT332 provides a single Driver Fail Monitor for both channels. The DFM output reports short conditions. The PEB 2236 does not include such a feature for the transmit circuit.

Table 1: PEB 2236 Line Length Codes

LS2	LS1	LS0	Line Length PIC/PULP Cable
0	0	1	0 ~ 50 m–24 awg
0	1	0	20 ~ 80 m–24 awg
0	1	1	60 ~ 130 m–24 awg
1	0	0	110 ~ 200 m–24 awg
1	0	1	140 ~ 230 m–24 awg
1	1	0	210 ~ 290 m–24 awg
1	1	1	270 ~ 320 m–24 awg
0	0	0	CEPT

Table 2: PEB 2236 Loopback Codes

Mode	LOOPA	LOOPB
RLOOP	1	0
LLOOP	0	1

Line Interface Modifications

The line interface must be modified when upgrading from the PEB 2236 to the LXT332. The T1 line interfaces are shown in Figure 1. The E1 line interfaces for 120 Ω twisted-pair are shown in Figure 2. The E1 line interfaces for 75 Ω coax are shown in Figure 3.

The applications illustrated here do not optimize return loss values. Instead they simplify design requirements. To design an application with the best possible return loss, see the LXT332 Dual Line Interface Unit Data Sheet for optimized Rt and transformer values.

Table 3: LXT332 Line Length Codes

LEN 2	LEN 1	LEN 0	Line Length	Cable Loss
0	1	1	0 ~ 41 m–22 awg	0.6 dB
1	0	0	41 ~ 81 m–22 awg	1.2 dB
1	0	1	81 ~ 122 m–22 awg	1.8 dB
1	1	0	122 ~ 162 m–22 awg	2.4 dB
1	1	1	162 ~ 198 m–22 awg	3.0 dB
0	0	0	75 Ω ITU	
0	0	1	120 Ω G.703	
0	1	0	FCC Part 68, Option A	

Table 4: LXT332 Loopback Codes

Mode	RLOOP	LLOOP	TAOS
RLOOP	1	0	n/a
LLOOP	0	1	n/a
DLOOP	1	1	1
TAOS	0	n/a	1
RESET	1	1	0

Figure 1: 100 Ω T1 Line Interface Upgrade

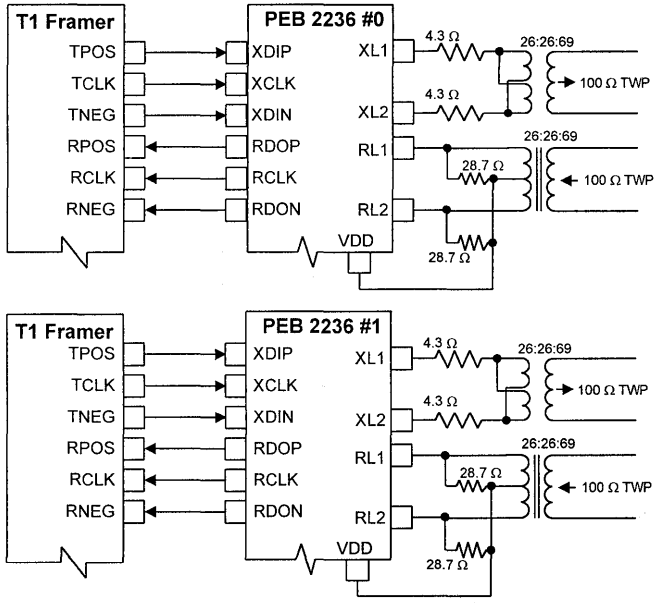

Figure 1A: PEB 2236 100 Ω T1 Line Interface

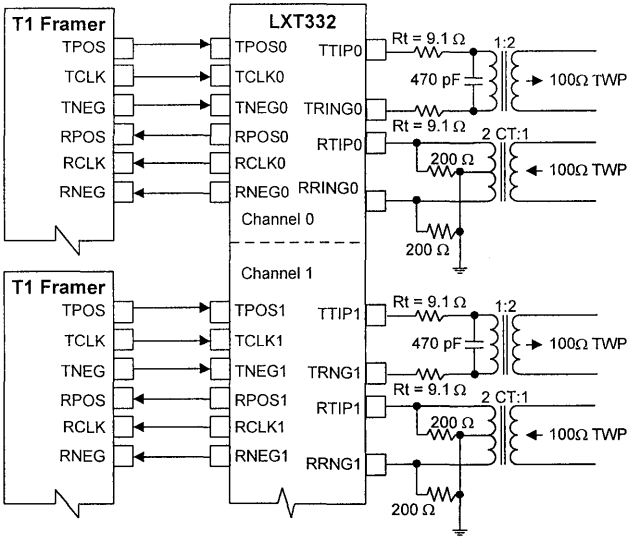

Figure 1B: LXT332 100 Ω T1 Line Interface

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Figure 2: 120 Ω E1 Line Interface Upgrade

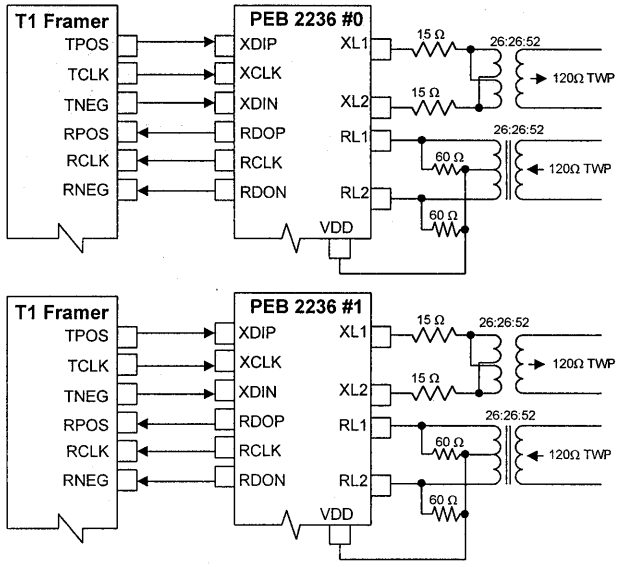


Figure 2A: PEB 2236 120 Ω E1 Line Interface

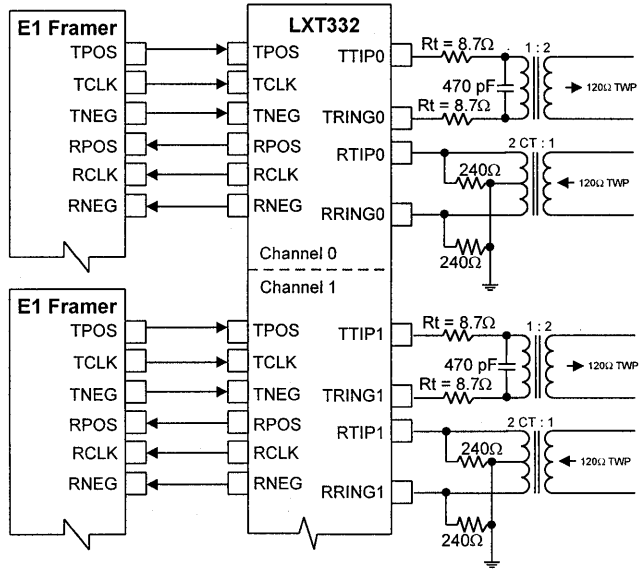


Figure 2B: LXT332 120 Ω E1 Line Interface

Figure 3: 75 Ω E1 Line Interface Upgrade

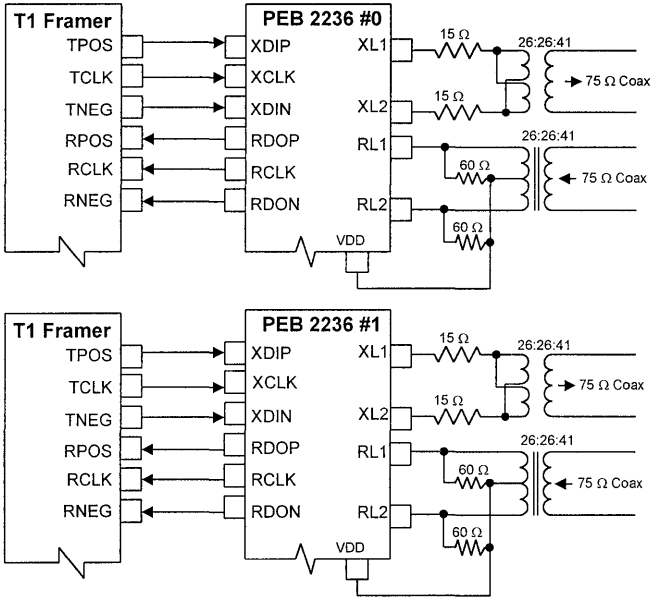


Figure 3A: PEB 2236 120 Ω E1 Line Interface

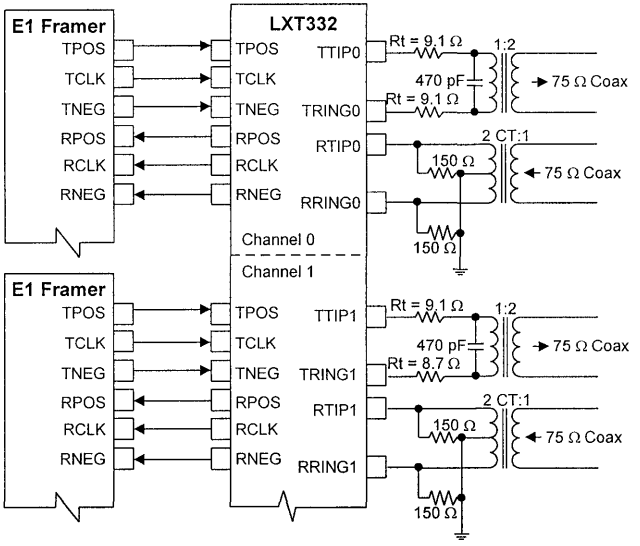


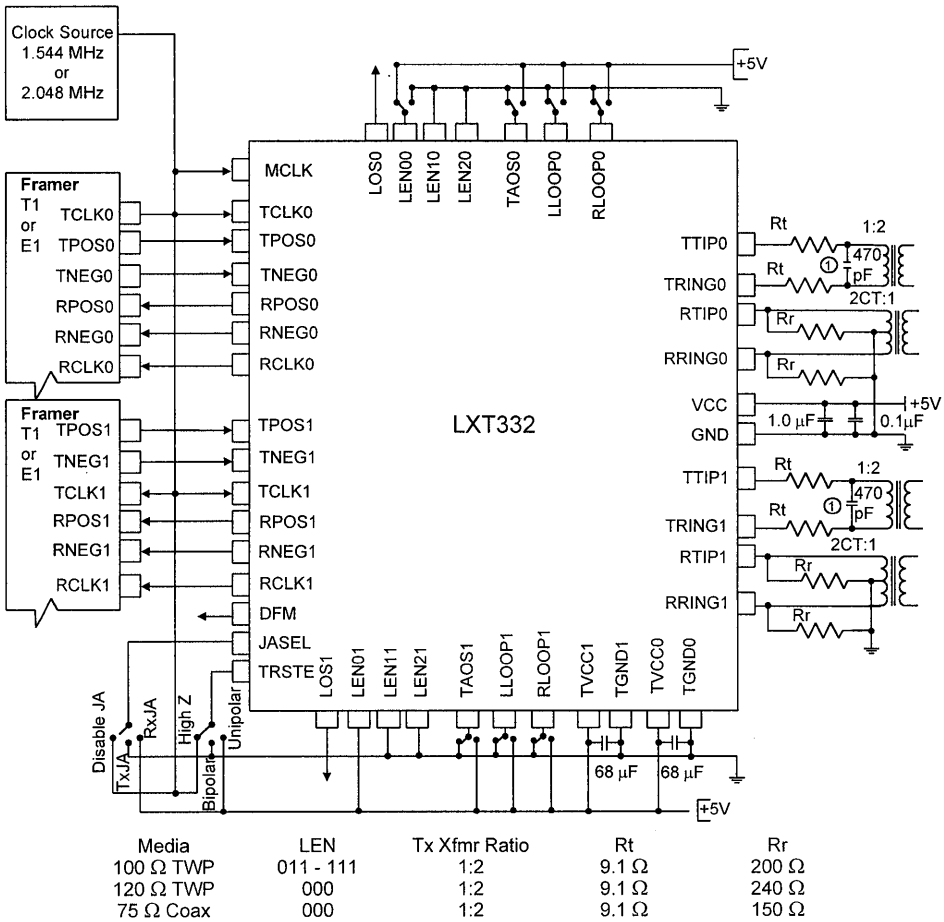
Figure 3B: LXT332 120 Ω E1 Line Interface

Typical LXT332 Application

A switchable interface board design is possible using the LXT332 device. Figure 4 shows a simplified application design for either T1 or E1 equipment which only requires changing the MCLK and Line Length inputs, and selecting appropriate resistors for Rt and Rr.

This application does not optimize return loss values. See the LXT332 Dual Line Interface Unit Data Sheet for Rt and transformer specifications for other possible components.

Figure 4: LXT332 Switchable T1/E1 Line Interface (Hardware Mode)



Media	LEN	Tx Xfmr Ratio	Rt	Rr
100 Ω TWP	011 - 111	1:2	9.1 Ω	200 Ω
120 Ω TWP	000	1:2	9.1 Ω	240 Ω
75 Ω Coax	000	1:2	9.1 Ω	150 Ω

NOTE:

① Typical value. Adjust for actual board parasitics to obtain optimum return loss.

APRIL 1996
Revision 0.0

LXT332 Dual Channel T1/E1 Transceiver Solution

Migration from Dual-Chip (AT&T T7290) to Single-Chip (LXT332) Implementation

General Description

This application note provides manufacturers of multi-channel T1/E1 transmission equipment with a smooth upgrade from a pair of AT&T T7290 single-channel devices to an advanced implementation using a single LXT332 integrated dual-channel device. This app note discusses Hardware Mode only. (No Host Mode is available in the T7290.)

There are some differences between the two devices in the back end and line interfaces. However, existing T7290 designs can easily be adapted to take advantage of the fully integrated dual channel LXT332.

Advantages

- Simplifies board design
- Single transformer turns ratio for both T1 and E1 applications
- Saves real estate
- Improves jitter performance
- No external crystal required
- Reduces inventory costs
- Additional features with Host Mode Serial I/O

Framer and Control Interface

No framer interface changes are required to upgrade from the T7290 to the LXT332. However, minor modifications to the control circuitry are required. There are also minor differences in the LOS and Transmit Driver monitor outputs.

Jitter Attenuation Select

The LXT332 JA circuitry is controlled by the JASEL and MCLK inputs. This function is implemented through the Mode 1 and Mode 2 pins on the T7290. Refer to Tables 1A and 1B for details.

Tristate Output

The Tristate control inputs on the two devices function similarly, but with inverted polarity. The T7290 TRI input is an active low; the LXT332 TRSTE input is an active high. To provide compatibility with existing designs, an inverter must be added to the existing TRI input.

Line Length/Pulse Shape Control

Both the LXT332 and the T7290 use 3-input codes to determine pulse shapes for various line lengths. The two coding schemes are shown in Tables 2A and 2B.

Loopback Control

Both the LXT332 and the T7290 provide various diagnostic loopbacks. The control codes for executing the various loopbacks are slightly different as shown in Tables 3A and 3B.

Loss of Signal

Both the LXT332 and the T7290 provide Loss of Signal (LOS) outputs. The internal detection circuitry which determines when an LOS condition exists is functionally different.

Transmit Driver Monitor

Both the LXT332 and the T7290 provide Driver Monitor detectors. The LXT332 DFM output reports short conditions. The T7290 TSC output differentiates between shorts to power supply, shorts to ground and shorts together.

Elastic Store Overflow

The T7290 provides an output to report ES overflow conditions. The LXT332 does not report overflow conditions.

Table 1A: AT&T JA Codes

JA Placement	Mode 1	Mode 2
Bypass	0	0
Transmit Path	0	1
Receive Path	1	0
Test Mode*	1	1
* Not used in normal operation.		

Table 1B:LXT332 JA Codes

JA Placement	JASEL
Bypass	MCLK*
Transmit Path	0
Receive Path	1
* JA is bypassed when JASEL is tied to MCLK.	

Table 2A:AT&T T7290 Line Length Codes

EC 3	EC 2	EC 1	Line Length	Cable Loss
1	0	0	0 - 131 ft ABAM	0.6 dB
0	1	0	131 - 262 ft ABAM	1.2 dB
1	1	0	262 - 393 ft ABAM	1.8 dB
0	0	1	393 - 524 ft ABAM	2.4 dB
1	0	1	524 - 655 ft ABAM	3.0 dB
0	1	1	75 Ω ITU	
1	1	1	120 Ω G.703	
0	0	0	FCC Part 68, Option A	

Table 2B:LXT332 Line Length Codes

LEN 2	LEN 1	LEN 0	Line Length	Cable Loss
0	1	1	0 - 133 ft ABAM	0.6 dB
1	0	0	133 - 266 ft ABAM	1.2 dB
1	0	1	266 - 399 ft ABAM	1.8 dB
1	1	0	399 - 533 ft ABAM	2.4 dB
1	1	1	533 - 655 ft ABAM	3.0 dB
0	0	0	75 Ω ITU	
0	0	1	120 Ω G.703	
0	1	0	FCC Part 68, Option A	

Table 3A:AT&T Loopback Codes

Mode	LOOPA	LOOPB	TBS
RLOOP	1	0	N/A
LLOOP	0	1	1 or 0
TBS	N/A	N/A	1
Full Local Loop	1	1	1 or 0

Table 3B:LXT332 Loopback Codes

Mode	RLOOP	LLOOP	TAOS
RLOOP	1	0	N/A
LLOOP	0	1	N/A
DLOOP	1	1	1
TAOS	0	N/A	1
RESET	1	1	0

Line Interface Modifications

The line interface must be modified when upgrading from the PEB 2236 to the LXT332. The T1 line interfaces are shown in Figures 1A and 1B. The E1 line interfaces for 120 Ω twisted-pair are shown in Figures 2A and 2B. The E1 line interfaces for 75 Ω coax are shown in Figures 3A and 3B.

Figure 1: 100 Ω T1 Line Interface Upgrade

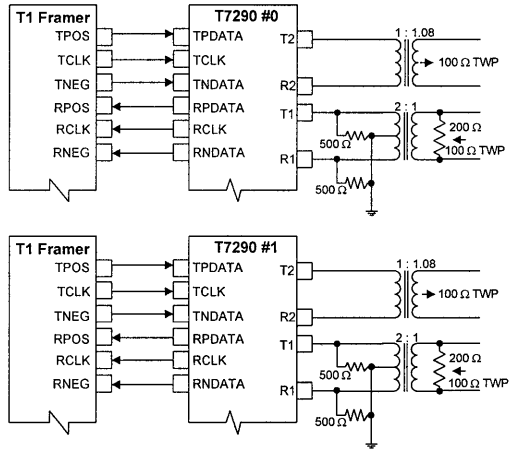


Figure 1A: T7290 100 Ω T1 Line Interface

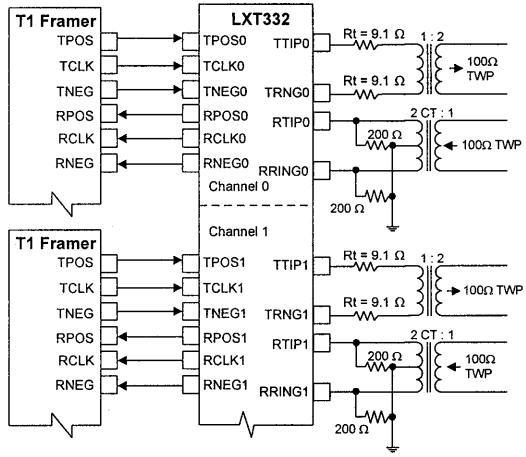


Figure 1B: LXT332 100 Ω T1 Line Interface

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Figure 2: 120 Ω E1 Line Interface Upgrade

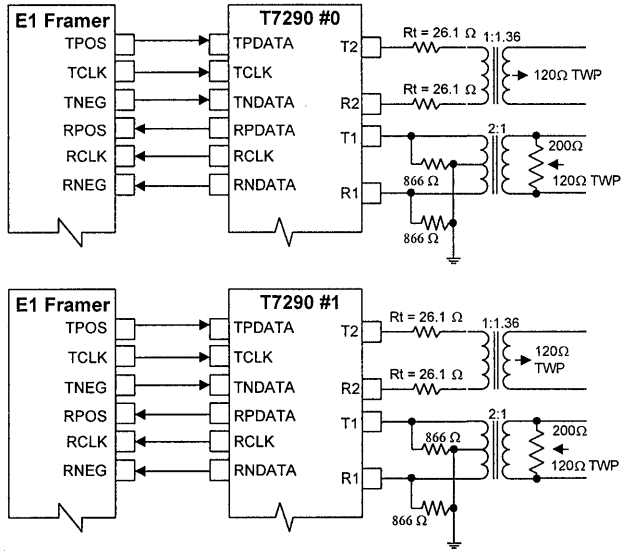


Figure 2A: T7290 120 Ω E1 Line Interface

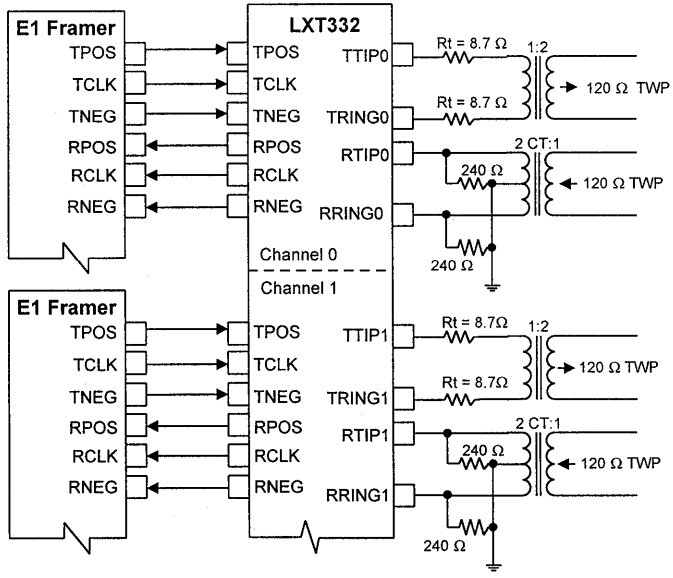


Figure 2B: LXT332 120 Ω E1 Line Interface

Figure 3: 75 Ω E1 Line Interface Upgrade

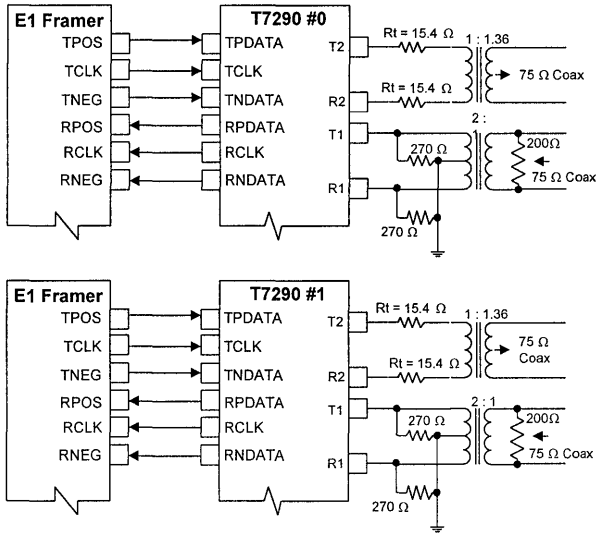


Figure 3A: T7290 120 Ω E1 Line Interface

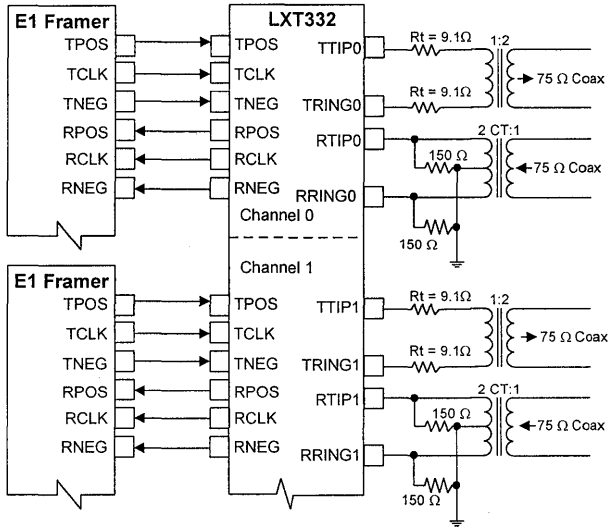
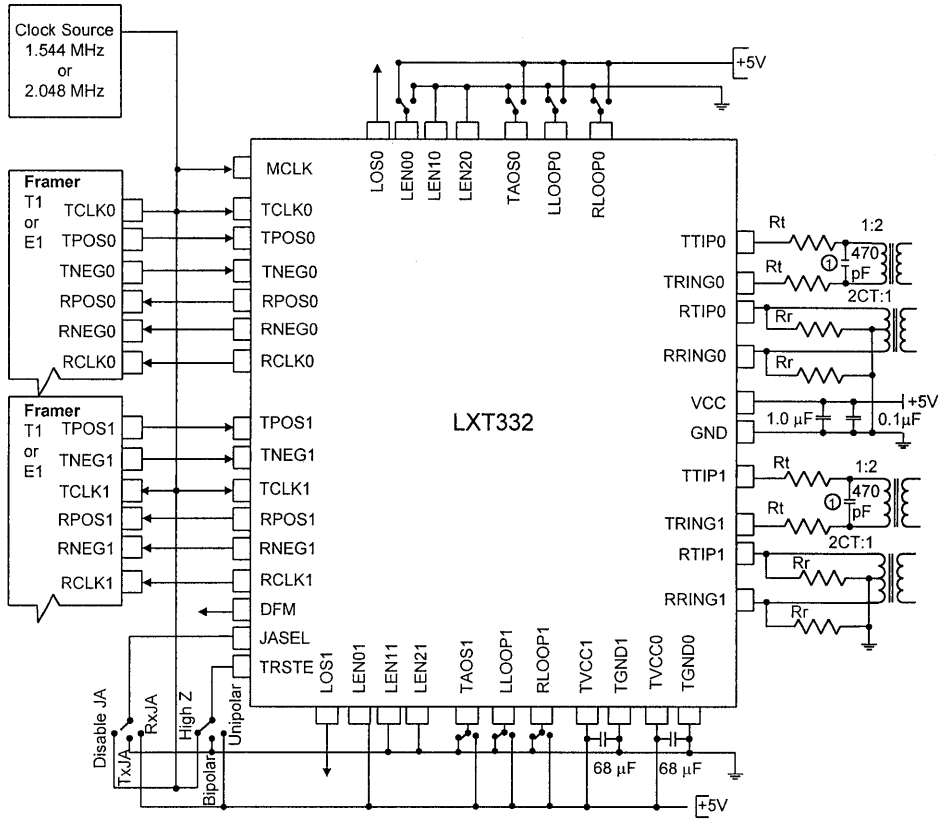


Figure 3B: LXT332 120 Ω E1 Line Interface

Using the LXT332, it is possible to design a switchable interface board. Figure 4 shows a simplified application which can be used for either T1 or E1 equipment by changing the MCLK and Line Length inputs, and selecting appropriate resistors for Rt and Rr.

Figure 4: LXT332 Switchable T1/E1 Line Interface (Hardware Mode)



Media	LEN	Tx Xfmr Ratio	Rt	Rr
100 Ω TWP	011 - 111	1:2	9.1 Ω	200 Ω
120 Ω TWP	000	1:2	9.1 Ω	240 Ω
75 Ω Coax	000	1:2	9.1 Ω	150 Ω

NOTE:

1. Typical value. Adjust for actual board parasitics to obtain optimum return loss.

Level One Short-Haul Devices

Application Guidelines

General Description

This application note documents the compliance of Level One Communications line of short-haul transceivers to ITU Recommendation G.775 for detecting and clearance of a loss of signal (LOS) condition. For purposes of illustration, data presented here are from the LXT304A transceiver. The logic circuitry related to LOS in the LXT304A is identical to that of all Level One short-haul transceivers.

To clarify the implementation of LOS detection and clearance, this application note explains ITU Recommendation G.775. The recommendation gives the criteria for the detection and clearance of both LOS and AIS defects at the intra-station interfaces conforming to recommendation G.703.

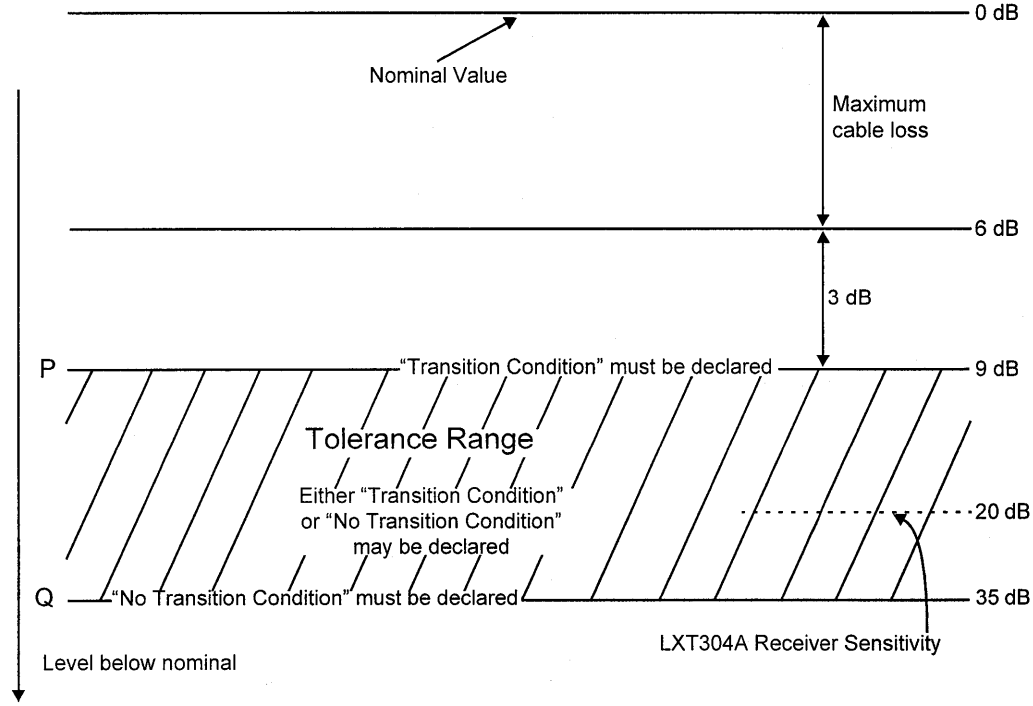
Recommendation G.775

Section 4.2 of ITU G.775 dated September 1993 states:

> A LOS defect at 2048 kbit/s interface is detected when the incoming signal has "no transitions", i.e., when the signal level is less than or equal to a signal level of Q dB below nominal, for N consecutive pulse intervals, where $10 \leq N \leq 255$.
>
> The LOS defect is cleared when the incoming signal has "transitions", i.e., when the signal level is greater than or equal to a signal level of P dB below nominal, for N consecutive pulse intervals, where $10 \leq N \leq 255$.

Refer to the figure on this page. The signal level P is (maximum cable loss +3 dB) dB below the nominal signal level. For a 2.048 Mbps transmission, P = 9 dB. The signal level Q is greater than the maximum expected cross talk level (Q = 35 dB).

G.775 LOS Tolerance Range with Receiver Sensitivity



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Declaring the Los Condition

Recommendation G.775 sets parameters for both signal levels and consecutive pulse period conditions. With reference to declaring the LOS Condition, it states, when the signal level without transition is less than or equal to Q dB below nominal, for N consecutive pulse intervals, where $10 \leq N \leq 255$, a LOS must be declared.î

This means if the signal level is below P yet still within the tolerance range, either LOS or clear from LOS is acceptable. However, the transceiver must declare LOS if the signal level falls below Q dB.

Level One transceivers use a digital-and-analog detection scheme to comply with the recommendation. If the signal level falls below 20 dB, the LXT304A[1] begins to count consecutive bit times and declares LOS after approximately 175 (160 to 190) consecutive zeros. This is in compliance with the recommendation. Refer to Table 1. Since the recommendation requires the receiver to have a minimum sensitivity of 9 dB, the 20 dB sensitivity provided by the Level One devices falls within the tolerance range.

Clearing the LOS Condition

In discussing clearing the LOS Condition, the recommendation says,

> The LOS defect is cleared when the incoming signal has transitions, i.e., when the signal level is greater than or equal to a signal level of P dB below nominal, for N consecutive pulse intervals, where $10 \leq N \leq 255$.
>
> The receiver must clear the LOS Condition above P dB if the pulse density falls within the window of N consecutive pulse intervals, where $10 \leq N \leq 255$.

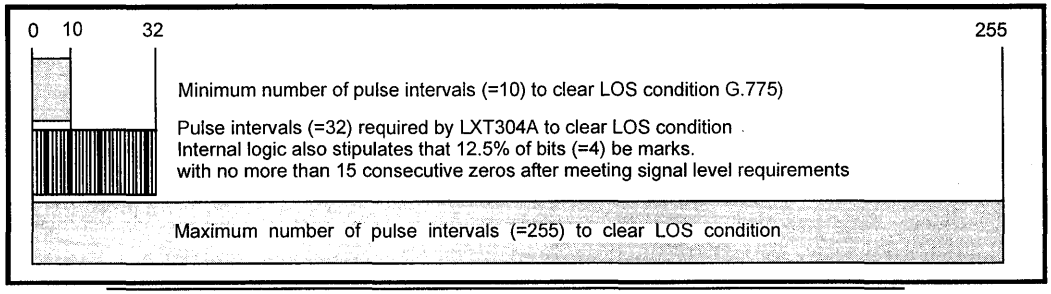
Level One transceivers meet these criteria by clearing LOS with a three step process: The signal level must first exceed the 20 dB signal level. Then a 32-bit repeating window checks for 12.5% ones density (to meet this parameter, there must be at least 4 ones out of the 32 bits in the window), and finally, there must be no more than 15 consecutive zeros. Figures 1 and 2 show this in graphic form.

Table 1: G.775 Requirements and Level One Implementation of LOS Detection

Condition	G.775 Recommendation	Level One Implementation
Detect LOS	Signal with no transitions[1] less than or equal to signal level of Q below nominal for N consecutive intervals where $10 \leq N \leq 255$.	Signal level below 20 dB and no consecutive transitions for 160 to 190 pulse intervals.
Clear LOS	Signal has transitions1 and level greater than or equal to P dB below nominal for N consecutive pulse intervals where $10 \leq N \leq 255$.	Signal level above 20 dB with bit density greater than 12.5% for 32 bit positions, but with fewer than 15 consecutive zeros.

2. A signal with "transitions" corresponds to a G.703 compliant signal.

Figure 1: G.775 Recommendation and Level One Transceiver Implementation to Clear LOS Condition

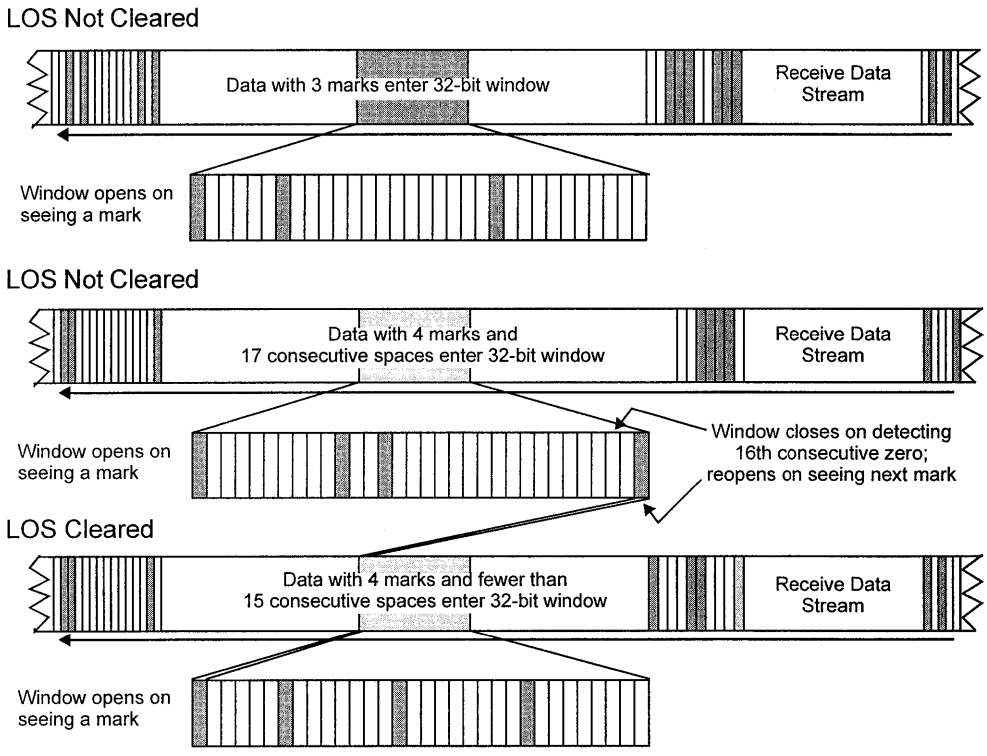


1 This document uses the LXT304A as an example. The LXT305, LXT305A and LXT332 transceivers meet the standard using the same LOS circuit design.

The window in these transceivers closes every time the 32 bits fail to include four marks. The window also closes any time the detector circuitry senses 16 consecutive zeros. It will only reopen when the circuitry detects a mark even if that mark was part of a window closed because of 16 consecutive zeros. This opening mark starts a new search for a pattern that will allow clearing the LOS condition. See Figure 2.

If the signal in the 32-bit sliding window meets the constraints described in this note, the transceiver will clear the LOS condition. This design is in compliance with ITU G.775 since the window of 32 bits fits within the N consecutive bits defined by $10 \leq N \leq 255$.

Figure 2: Level One Transceiver Requirements for Clearing the LOS Condition



Note: This illustration shows the digital detection scheme.

Crystal-less T1 Long-Haul Solutions

LXT310/360 Universal Line Interface Unit Design Guide

Introduction

This note describes applications for the crystal-less LXT360 transceiver in newer generation network access equipment. Use this application note as a guide when upgrading designs using the LXT360. Before designing a circuit using this new device, refer to the data sheets for both devices for complete information.

The LXT360 provides several advanced features. While the LXT360 provides for both T1 (1.544 Mbps) and E1 (2.044 Mbps) operation, this application note focuses only on hardware-controlled, T1 designs. Additional application notes detail migration paths for T1 and E1 design using other LXT360 features.

Identifying Major LXT360 Design Improvements

Jitter Attenuation Circuitry

- The LXT310 device requires a pullable 6.176 MHz crystal to provide selectable jitter attenuation. The jitter attenuation circuitry may be in either the transmit or the receive path, depending on the application.
- The LXT360 requires only the MCLK signal to provide the same selectable jitter attenuation functions since it uses digital JA circuitry. It needs no crystal or high-frequency external clock for jitter attenuation.

External Clock Requirements

- The MCLK input signal in the LXT310 is optional. If used, the clock must have an accuracy of ±100 ppm.
- The MCLK input signal in the LXT360 is mandatory. The clock must be a stand alone reference with an accuracy of ±32 ppm or better at 1.544 MHz for T1 applications.

Applications

- The LXT310 is a long-haul T1 transceiver only.
- The LXT360 operates as either a short- or long-haul transceiver in T1 or E1 applications.

Available Line Coding Schemes

- The LXT310 allows B8ZS encoding in either Unipolar or Bipolar mode.
- The LXT360 transceiver offers B8ZS line encoding only in the Unipolar Mode.

Reset Operation

- Reset on the LXT310 occurs when both LLOOP and RLOOP inputs are pulled High while TAOS is pulled Low for at least 200 ns.
- Reset on the LXT360 occurs when LLOOP, RLOOP and TAOS are pulled High simultaneously for at least 200 ns.

Output Control

- The LXT310 provides a high-impedance state option for the TTIP/TRING outputs only when TCLK is grounded.
- The LXT360 provides high-impedance state limited to the TTIP/TRING outputs when TCLK is pulled High. An additional high-impedance state option is available for all output pins when TRSTE is pulled High.

Line Attenuation Indication

- The LXT310 provides Line Attenuation Indication (LATN) in both Hardware and Host Modes.
- The LXT360 provides LATN in Software Mode only.

NLOOP Detection

- For the LXT310 transceiver, holding RLOOP, LLOOP and TAOS High simultaneously for 200 ns and then pulling all three Low enables the NLOOP detection function. Alternatively, tying RCLK to RLOOP also enables NLOOP. Resetting the device disables NLOOP detection.
- In the LXT360 setting the RLOOP input to 2.5 V ±0.2 V ("Midrange") enables NLOOP detection. Setting RLOOP Low or High disables NLOOP detection.

Loss of Signal Detection and LOS Clear Criteria

- The LXT310 device declares a Loss Of Signal (LOS) condition when it detects 175 consecutive spaces. It clears the LOS condition when the receiver detects 12.5% mark density (*i.e.*, 4 marks within a 32-bit period) with no more than 15 consecutive 0s.
- The LXT360 transceiver also declares the LOS condition when it detects 175 consecutive spaces. It clears the LOS condition when the receiver detects 12.5% mark density (determined by 16 marks in a sliding 128-bit period) with fewer than 100 consecutive 0s.

DIAGNOSTIC FUNCTIONS

The LXT360 provides several diagnostic features not provided on the LXT310 transceiver. These are Dual Loopback function, Error Insertion and Detection, AIS Condition Monitoring and Elastic Store Pointer Monitoring. The LXT360 data sheet has details on these functions.

In addition, the LXT360 provides both a Quasi-Random Signal Source and a Detector for diagnostic procedures.

Three-State Input Pins

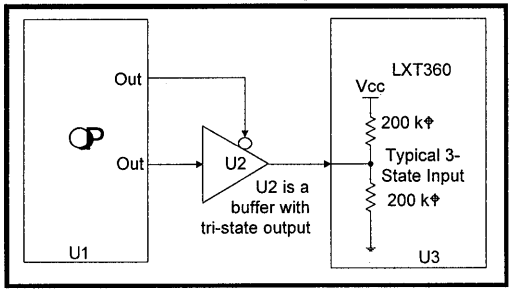
The LXT310 uses two-state (High and Low) configuration inputs but some LXT360 control inputs recognize three states. Typical values for these states are:

High – $V_{IN} > 3.5$ V.
Midrange – 2.3 V ≤ V_{IN} ≤ 2.7 V (or floating).
Low – $V_{IN} < 1.5$ V.

The control for three-state inputs may be a standard tri-state buffer. Figure 1 shows a typical driver circuit for these inputs. Setting the output buffer to its high-impedance state places the three-state input into its Midrange state.

Application designers must take into account the current drawn by the internal resistors (part of each three-state input) before choosing a buffer to drive these inputs to their High or Low states.

Figure 1: Typical Circuit for LXT360 Three-State Inputs



Line Interface Considerations

To improve transmit return loss, add a capacitor (CTX) to the transmit side as shown in Figures 2 through 4. This capacitor is typically 470 pF, but may vary depending on the resistor and transformer values, the board layout and the parasitics of the protection diodes.

Table 1 shows the combinations of transformers, resistors and capacitors needed for the transmit side as shown is these applications. Table 2 lists transformers that met Level One Communications specifications when tested with the LXT360 device.

Table 1: Transmit Return Loss (1.544 Mbit/s–Long- or Short-Haul)

EC4-1	Xfrmr/ Rt	Xmission Line	CTX (pF)	Return Loss
Refer to the LXT360 Data Sheet	1:2/ 9.1 W	100 Ω Twisted Pair	0	16 dB
			470	17 dB
	1:1.15[1]/ 0.0 W	100 Ω Twisted Pair	0	2 dB
			470	2 dB

1. A 1:1.15 transmit transformer keeps the total transceiver power dissipation at a low level, a 0.47 µF DC blocking capacitor must be placed on TTIP or TRING.

Table 2: Recommended Transformers for LXT360/LXT361

Tx/ Rx	Turns Ratio	Part Number	Manufacturer
Tx	1:1.15	PE-65388	Pulse Engineering
		PE-65770	
	1:2	PE-65351	
		PE-65771	
		0553-5006-IC	Bell-Fuse
		66Z-1308	Fil-Mag
		671-5832	Midcom
		67127370	Schott Corp
		67130850	
		TD61-1205G	HALO (combination Tx/ Rx set)
		TD67-1205G	
Rx	1:1	FE 8006-155	Fil-Mag
		671-5792	Midcom
		PE-64936	Pulse Engineering
		PE-65778	
		67130840	Schott Corp
		67109510	
		TD61-1205G	HALO (combination Tx/ Rx set)
		TD67-1205G	

Bipolar Mode with AMI Line Coding (without Zero Suppression)

Most pins on LXT360 have the same names and functions as those on the LXT310, although some differ. This section describes the modifications needed to change from the LXT310 to the LXT360 in Hardware Control Mode. The LXT360 pins not included in this discussion have the same connections and signal level requirements as those on the LXT310. Table 3 is a summary of the pins whose functions change when moving from LXT310 to LXT360.

The 6.176 MHz crystal required by the LXT310 must be deleted when migrating to the LXT360. The functions on pins 17, 18, and 23 on the LXT310 change pin locations on the LXT360 transceiver. **Pay particular attention to the new locations for these signals**. Figure 2 shows the connection differences between the two transceivers for this configuration.

Pin 1: The LXT360 requires an independent, external clock called MCLK. The MCLK input signal must have a nominal rate of 1.544 MHz and an accuracy of ±32 ppm or better. The LXT310 uses the same nominal frequency, but requires no better accuracy than ±100 ppm.

Pin 5: In the LXT310, pin 5 is called MODE. This pin can be pulled High or Low, or it can be tied to the RCLK pin. The RCLK signal at the MODE pin enables the B8ZS encoders and decoders.

In the LXT360, the MODE pin is a three-state input pin: High, Low or Midrange. Setting the pin to Midrange enables the B8ZS encoders and decoders in LXT360 for T1 applications (and also forces the transceiver into unipolar operation).

Pin 9: In LXT360, pin 9 is called TRSTE. It is a three-state input. With TRSTE pulled High all LXT360 device output pins go into a high-impedance state. In conjunction with MODE (pin 5), this pin also sets the operational mode of the transceiver.

To enable T1, Long-Haul, Bipolar, Hardware Control Mode, the TRSTE pin must be pulled Low. See the data sheet for a complete description of the operating modes.

Pin 10: This pin is the XTALOUT input on the LXT310. Leave this pin not connected on the LXT360.

Pin 17: Move the LXT310 signal (EGL) to pin 23 on the LXT360. In the LXT60, pin 17 is EC4 and must be pulled Low to enable T1, Long-Haul operation.

Pin 18: The LXT310 pin 18 signal (NLOOP) appears on pin 23 of the LXT360.

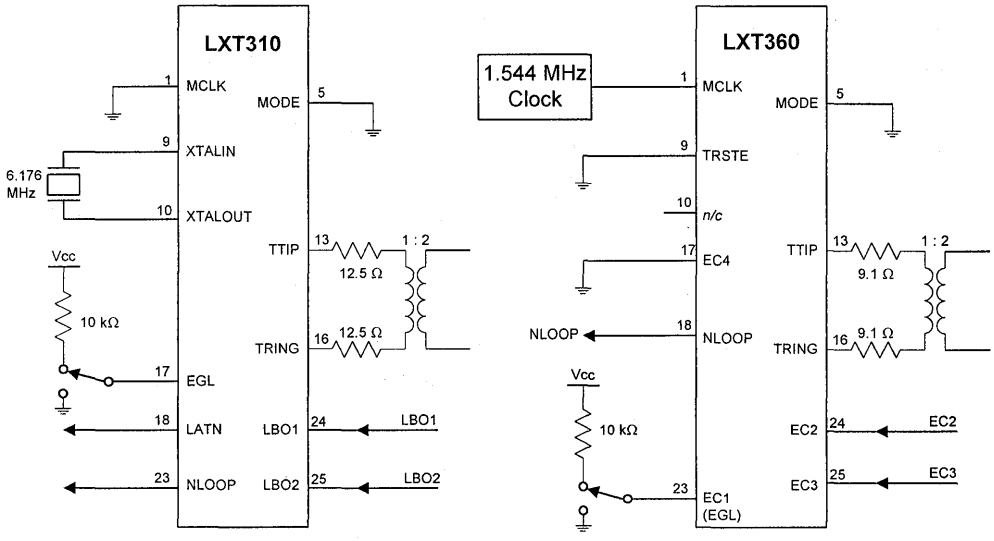
The LATN signal, which is on pin 18 of the LXT310, is not available in the Hardware Mode on the LXT360. However, a binary encoded equivalent to LATN is provided in the LXT360 Software Mode.

Pin 23: The EGL signal, which appears on pin 17 of the LXT310 appears on the LXT360 pin 23 (EC1).

The NLOOP signal, which appears on pin 23 of the LXT310, is available on pin 18 of the LXT360.

Pins 24 and 25: These pins retain their functions from the LXT310, but the names of the signals change. In the LXT310, pin 24 is LBO1 and pin 25 is LBO2. The LXT360 uses the names EC2 (pin 24) and EC3 (pin 25). The functions and connection remain the same. See the LXT360 Data Sheet for details.

Figure 2: Bipolar Mode Using AMI Line Coding (without Zero Suppression)[1]



NOTE:

1. Pins not shown on this figure have the same function on both the LXT310 and LXT360. They do not require modification for proper functioning.

Table 3: Bipolar Mode using AMI Line Coding (without Zero Suppression)

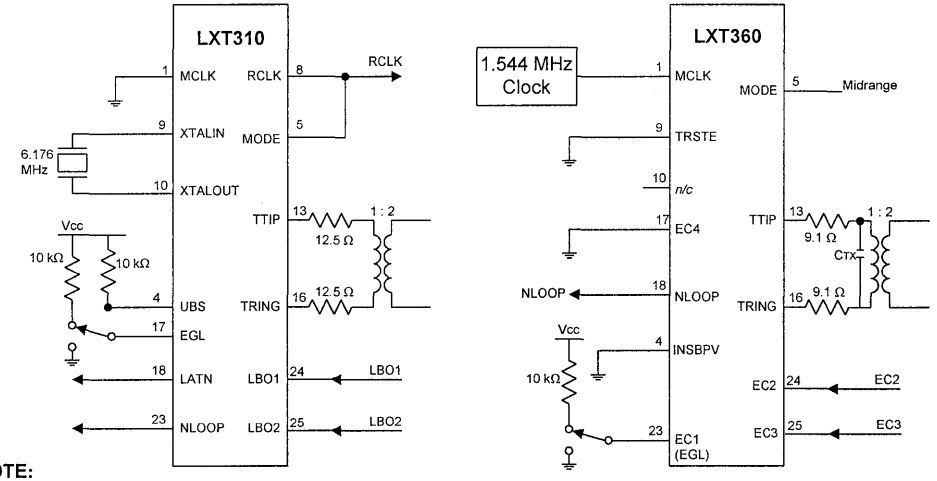
	LXT310		LXT360		
Pin#	**Name**	**Function/State**	**Name**	**Function/ State**	**Comments**
1	MCLK[1]	1.544 MHz/GND	MCLK	1.544 MHz	Mandatory in LXT360 applications
5	MODE	Low	MODE	Low	MODE and TRSTE set operation mode Crystal not used in LXT360
9	XTALIN	6.176 MHz Crystal	TRSTE	Low	
10	XTA-LOUT	6.176 MHz Crystal	—	*n/c*	No function assigned to this pin.
17	EGL	Input	EC4	Input–Low	EC4 = Low for T1 long-haul operation.
18	LATN	Output	NLOOP	Output	LATN not supported on LXT360 in Hardware Control Mode. NLOOP changes location.
23	NLOOP	Output	EC1	Set to select the Xmit line build-outs, including EC4, pin 17.	
24	LBO1	Set to select the Xmit line build outs.	EC2		Refer to Table 12 in LXT360 Data Sheet.
25	LBO2		EC3		

1. MCLK is optional in LXT310 applications. With the LXT310, if MCLK is not supplied, pin 1 must be grounded.

Using B8ZS Encoding/Decoding

The LXT310 supports B8ZS encoding/decoding in both Unipolar and Bipolar Modes. The LXT360 configures itself in Unipolar mode (*i.e.*, TPOS becomes TDATA and TNEG becomes INSBPV) when B8ZS is enabled. To enable B8ZS encoders and decoders, set the MODE pin to Midrange. Other connections are the same as for AMI line coding. Figure 3 shows the changes needed in connections for LXT310 and LXT360. See Table 4 for a summary of the modifications needed to adapt an LXT310 application to the LXT360.

Figure 3: Unipolar Mode (with B8ZS Zero Suppression)[1]



NOTE:

1. Pins not shown on this figure have the same function on both the LXT310 and LXT360. They do not require modification for proper functioning.

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Table 4: Unipolar Mode (B8ZS Zero Suppression Enabled)

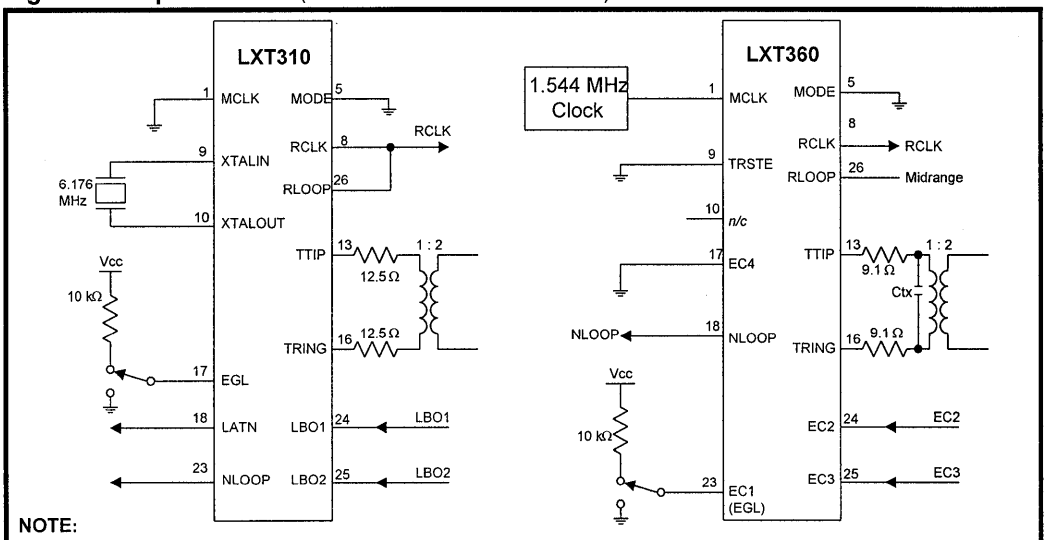
Pin #	LXT310		LXT360		Comments
	Name	Function/State	Name	Function/State	
1	MCLK[1]	1.544 MHz/GND	MCLK	1.544 MHz	Mandatory in LXT360 applications
5	MODE	Tie to RCLK	MODE	Midrange[2]	MODE and TRSTE set operation mode
4	UBS	High	INSBPV	Low	Refer to Data Sheet
9	XTALIN	8.152 MHz Crystal	TRSTE	Low	Crystal not used in LXT360
10	XTALOUT	8.152 MHz Crystal	—	*n/c*	
17	EGL	Input	EC4	Input–Low	EC4 = Low for T1 long-haul operation.
18	LATN	Output	NLOOP	Output	LATN not supported on LXT360 in Hardware Control Mode. NLOOP changes location.
23	NLOOP	Output	EC1	Set to select the Xmit Line Build Outs and receiver range.	
24	LBO1	Set to select the Xmit Line Build Outs.	EC2		Refer to Table 12 in LXT360 Data Sheet.
25	LBO2		EC3		

1. MCLK is optional in LXT310 applications. If MCLK is not supplied to the LXT310, pin 1 must be grounded.
2. "Midrange" means leave the pin unconnected or tie it to 2.5 V.

Enabling NLOOP Detection

Tying the RCLK output to the RLOOP input enables Network Loop detection (NLOOP) on the LXT310 transceiver. NLOOP detection is also enabled by holding RLOOP, LLOOP and TAOS all High simultaneously for 200 ns and then bringing them Low. To enable NLOOP detection on the LXT360 transceiver, tie the RLOOP input pin to Midrange as in Figure 4.

Figure 4: Bipolar Mode (with NLOOP Detection Enabled) [1]



NOTE:

1. Pins not shown on this figure have the same function on both the LXT310 and LXT360. They do not require modification for proper functioning.

APRIL 1996
Revision 0.0

Jitter Performance Requirements for E1 Leased Lines

ETSI TBR-12 & TBR-13 Conformance Testing

Introduction

This application note summarizes the new jitter performance requirements and appropriate conformance testing procedures for E1 (2.048 MHz) terminal equipment designed to attach to harmonized leased lines throughout the European Economic Community (EEC).

Directive 91/263/EEC implements a harmonized market for telecommunications equipment throughout the EEC by establishing unified procedures for testing, certification, marking and quality assurance. This allows vendors and service providers to market and use the same equipment in the public networks of all EEC member states. The Open Network Provision (ONP) directive 92/44/EEC mandates member states to provide leased lines having harmonized technical characteristics to facilitate inter-network operability across the EEC.

The European Telecommunications Standards Institute (ETSI) drafts two types of standards that define these harmonized requirements. The first, for which compliance is voluntary, is the European Telecommunications Standard (ETS). An ETS completely describes all details of the specified interface or equipment. The second standard, for which compliance is mandatory, is the Technical Basis for Regulation (TBR). A TBR defines the minimum necessary technical requirements for the interface or equipment and allows for no national deviations. The TBR technical requirements are combined with regulatory provisions to form a Common Technical Regulation, or CTR.

In Europe there are two categories of 2048 kbps leased-line service: unstructured and structured. ETS 300-248 fully describes the unstructured service interface and TBR-12 (December 1993) defines the necessary technical requirements. Unstructured service provides a usable bit rate of 2048 kbps with no network-provided timing or framing support.

Structured service provides a usable bit rate of 1984 kbps with network framing support. ETS 300-420 fully describes this interface. The current draft of TBR-13 (June 1994) defines the necessary technical requirements.
(By the end of 1995, CTR-13 should include the provisions of TBR-13.) Compliance with TBR-13 also insures compliance with TBR-12.

Maximum Output Jitter Specifications

TBR-12 and TBR-13 (draft) include a common Output Jitter section (5.2.1.4). For terminal equipment, this section defines a maximum output jitter of 0.11 UIpp in the band from 40 Hz to 100 kHz.

The output jitter limit applies to equipment in configurations where output timing is derived locally as well as configurations where output timing is derived from one or more leased lines. For such iloop-timedî applications these requirements also imply minimum jitter transfer requirements because they apply when the maximum allowed input jitter is present at all line inputs. These requirements also apply with a data rate offset of up to ±50 ppm from 2.048 MHz.

Figure 1 shows the input jitter amplitude and the maximum output jitter amplitude over frequency when measured across a 40 Hz - 100 kHz bandwidth. These specifications require loop-timed equipment to provide a significant amount of jitter attenuation at 20 Hz because the standards specify that conformance testing be done using a 40 Hz, first-order high pass filter which still allows the measurement of a significant portion of the 1.5 UIpp input jitter applied at 20 Hz.

At 20 Hz the terminal equipment must provide approximately 15 dB of jitter attenuation to insure that 1.5 UIpp is attenuated to 0.11 UIpp when measured using the first-order 40 Hz, high-pass filter providing approximately 7 dB of attenuation at 20 Hz. This will be the case as long as the equipment does not transfer significant components of the 20 Hz the input jitter to higher frequencies. Designs which do not have linear jitter transfer at 20 Hz with an input amplitude of 1.5 UIpp may shift jitter to higher frequencies inside the filter passband and thus fail to comply at this frequency.

CONFORMANCE TESTING

Terminal equipment is tested in configurations where it does and does not derive timing from an input (if it has the capability to do so). One way to configure a single line system for loop timing is to enable the line interface line-side (i.e., remote) loopback function.

Table 1 lists useful equipment for TBR-12 and TBR-13 characterization and conformance testing. Figure 2 illustrates the recommended test configuration using this equipment.

The HP3785A measures output jitter with an external 40 Hz RC high-pass filter and the 100 kHz internal low-pass filter. The high-pass filter consists of a 4 µF capacitor connected between the DEMOD output and the MEASURE input on the back of the HP3785A. The external 4 µF capacitor and the internal 1 kΩ input termination resistor in the MEASURE input combine to form the filter.

NOTE

Prior to testing, use the HP3785A to calibrate the filter by adjusting the capacitor to achieve a 40 Hz, -3 dB corner frequency.

Figure 1: Input and Maximum Output Jitter

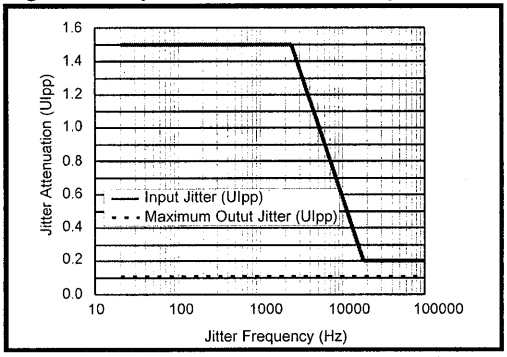


Table 1: Recommended Equipment for Jitter Conformance Testing

MODEL #	DESCRIPTION
Wavetek 145	Function Generator
HP3400A	RMS Voltmeter
HP3785A	Jitter Generator/Receiver
TTC Fireberd 6000A	E1 Pattern Generator
TTC 41800	2.048M interface module
Stanford Research	Synthesized Function
DS345	Generator

The filter should be calibrated with a network analyzer with high impedance inputs to prevent loading or with an audio oscillator and RMS voltmeter (as shown in Figure 3). Figure 4 illustrates the transfer function of a properly calibrated high pass filter implemented with a 4 µF capacitor in series with the MEASURE input of the HP3785A.

Configure the HP3785A jitter generator to generate a jittered clock using the clock input from the external clock synthesizer (e.g., the Stanford Research DS345). In addition, set the switch on the back of the HP3785A to enable the MEASURE input. Connect the jittered clock from the HP3785A so it clocks the Fireberd 6000A pattern generator which generates the HDB3 encoded, framed, 215 -1 PRBS input signal for the equipment under test.

The tested output port connects directly to the HP3785A jitter receiver input. Read the output jitter directly from the HP3785A front panel meter using the 1 UIpp input range. The reading will be from 40 Hz to 100 kHz. Test each output port on the equipment at several input jitter points along the curve in Figure 1. Adjust the data rate offset at each frequency and to obtain the largest measured output jitter. At all frequencies and data rate offsets, the output jitter amplitude must be less than 0.11 UIpp.

Figure 2: Confromance Test Configuration

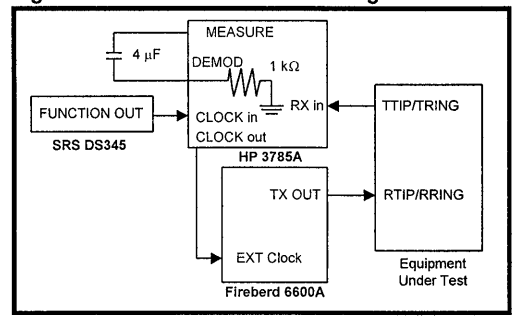
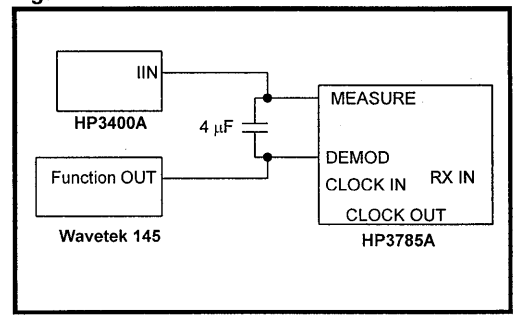


Figure 3: Filter Calibration



TYPICAL PERFORMANCE OF LEVEL ONE LINE INTERFACE ICS

The Level One LXT300Z, LXT304A, LXT305A and LXT318 transceivers provide the jitter attenuation needed to satisfy the TBR-12 and -13 requirements. These devices begin jitter attenuation at approximately 3 Hz insuring adequate margin against the TBR-12 and TBR-13 output jitter limit with 1.5 UIpp input at 20 Hz. Table 2 and Figure 5 present the data measured using the procedure outlined above with the LXT304A. The LXT304A meets the TBR-12 and TBR-13 requirements throughout the required frequency range. These data are also typical of the performance of the LXT300Z, LXT305A and LXT318.

Table 2: LXT304A Measured Performance

Jitter Freq.	Measured Output	Jitter Freq.	Measured Output
(Hz)	(UIpp)	(Hz)	(UIpp)
20	0.075	2400	0.008
50	0.053	5000	0.008
100	0.035	10000	0.008
250	0.019	15000	0.008
500	0.013	18000	0.007
750	0.012	25000	0.007
1000	0.011	50000	0.007
1500	0.008	75000	0.007
2000	0.008	100000	0.007

Figure 4: Transfer Function of a Properly Calibrated External Filter

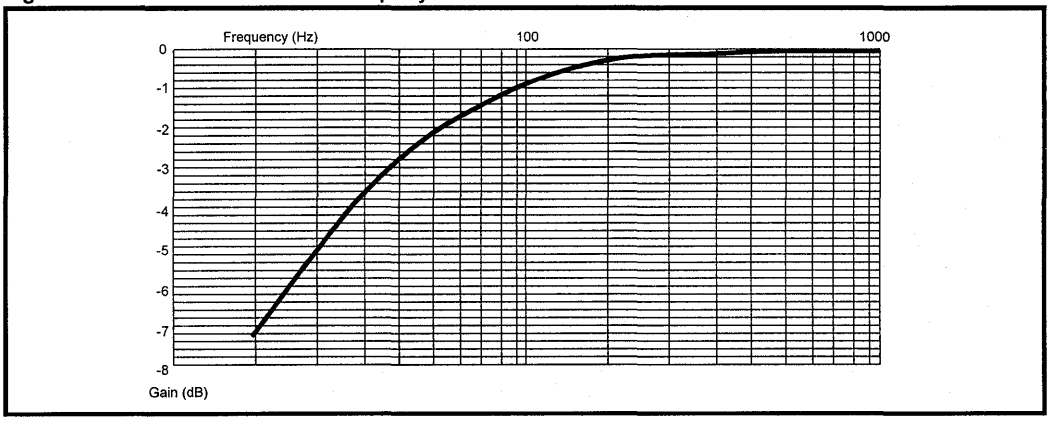
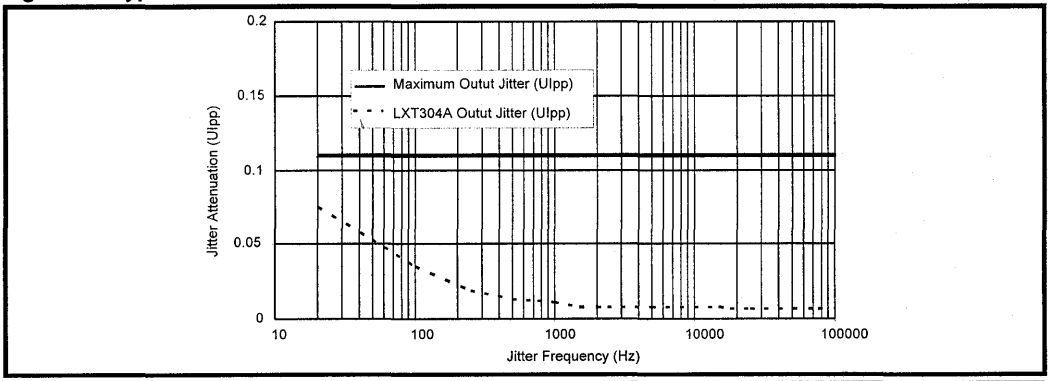


Figure 5: Typical LXT304A Jitter Attenuation Performance



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NOTES

LXT300/300Z/304A/305A Integrated Short-Haul Transceivers Crystal Layout Guidelines

General Description

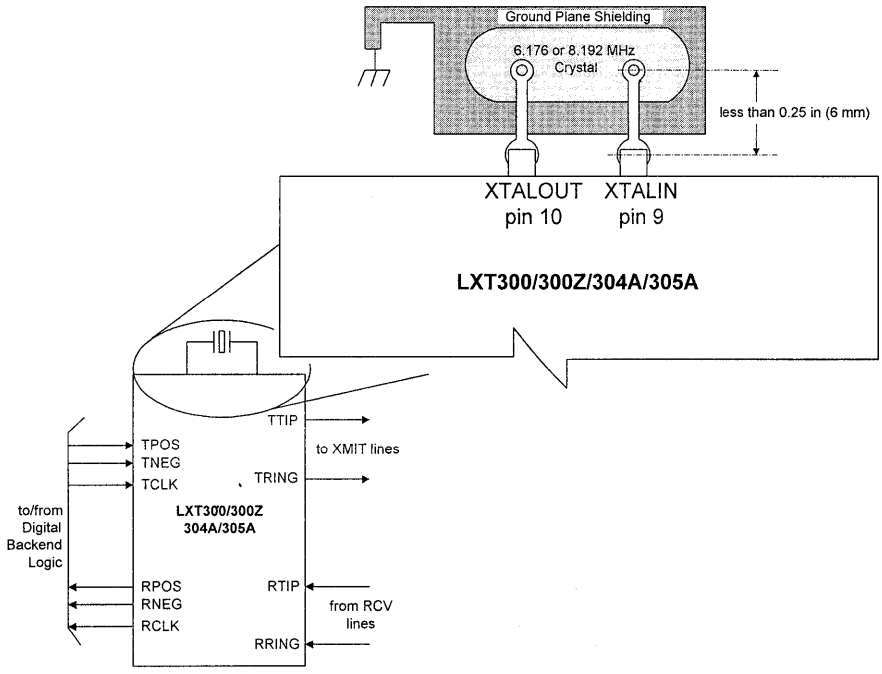
Level One transceivers are designed for robust operation. Good PCB design practices also contribute to overall application reliability. This application note reminds design engineers of PCB layout considerations that will make LXT300, LXT300Z, LXT304A and LXT305A transceiver applications even more effective.

The PCB designs should lay out the crystal input to any of these transceivers to minimize coupling of other digital and analog signals into XTALOUT and XTALIN. See the figure below. These inputs (pins 9 and 10 for all products included in this note) are high impedance nodes which can pick up interference from adjacent PCB traces and other components on the board. Adhering to these considerations will help ensure proper operation.

Before beginning a PCB design for any of the LXT300-series family transceivers, consider the following points:

- Use a crystal that meets the recommended crystal specifications (see the appropriate Data Sheet)
- Minimize the trace lengths between the transceiver and the 6.176 or 8.192 MHz crystal (typically less than 0.25 in or 6 mm)
- Shield these connections and the area around the crystal with ground planes
- Keep other high speed system clocks away from crystal leads and traces
- Locate all magnetic components well away from the crystal, its leads and traces
- Keep all high energy signals away from crystal leads and traces connected to pins 9 and 10

Crystal Layout for LXT300-Family Transceivers



NOTES

LXT360/361 Line Protection Circuitry

General Description

This application note provides guidelines for line protection circuitry required in typical LXT360/361 applications such as Network Channel Termination Equipment (NCTE), Channel Service Units (CSUs) and Wide Area Network (WAN) interfaces. NCTE is installed at the customer premises end of the T1 or E1 lines. As these lines run between the customer facilities and the central office, they are subject to overvoltage/overcurrent stresses from lightning strikes, power crosses and other noise impairments. Protection circuitry is required to protect the line from injected impairments and to protect the terminal equipment (CSU, NTU, mux, PBX, etc.) from overload stresses.

Protection requirements for T1 equipment are specified in FCC Part 68 (lightning hazards), UL 1459 (AC hazards), Bell Core TR-TSY-000007 and AT&T Pub 62411. These documents differentiate between longitudinal stress (differential tip/ring and ground) and metallic stress (differential between tip and ring). Longitudinal stresses are more common and include impulsive noise events such as lightning induced surges. Metallic stresses are less likely and are usually caused by power crosses during maintenance activity.

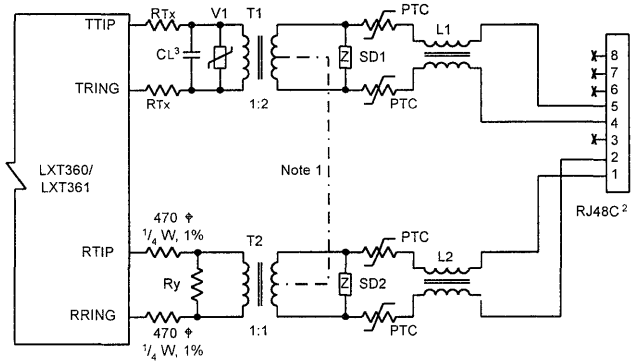
Similar protection circuitry is suggested for E1 applications of the LXT360/361. The network described in this application note targets compliance with ETS 300 046-3 and ITU K17-K20.

To ensure compliance with all applicable requirements, the final design should undergo appropriate testing at an approved lab.

Protective Circuitry Discussion

- No power or ground planes should be located on the circuit board in the area near the T1/E1 Line connector and back to the transformers.
- Select resistors RTx to match the line impedance. Their values impact the amplitude of the transmitted signal and the transmit return loss.
- Positive Temperature Coefficient Resistors (PTCs) permit healing after an overvoltage event. Their pre-trip resistance is specified at between 4 and 7 Ω .
- The PTCs will slightly reduce the amplitude of the transmitted signal. When using a 1:2 transformer, carefully selecting the series resistors (see Table 1) may negate this effect.
- The breakdown voltage of the line transformers (T1 and T2) must be at least 1.5 kV. (E1 designs may require a breakdown voltage of 3.0 kV.)
- Some harmful signal voltage from the interface lines will cross the T1/E1 transformer to the IC side; the recommended varistor (V1) with sufficient stand off voltage will provide additional protection to the LIU.
- Sidactors SD1 and SD2 provide the primary protection against bidirectional transient voltages on the transmit and receive sides.
- The final board design determines the values for the RF chokes (L1 and L2).
- Join the line side center taps of the Transmit and receive line transformers only for applications requiring a DC path for sealing currents (*i.e.*, some T1 CSU applications).
- The RJ48C configuration shown is recommended for T1 CSU applications.

LXT360/LXT361 Line Protection Circuitry



NOTES

1. Interconnection of transformers T1 and T2 is optional to support current in the E1/T1 loop.
2. Connections at RJ48C jack are for T1 CSU applications only. For E1 applications, refer to ITU standards.
3. Assign a space for Capacitor CL. CL can be installed to improve the Tx return loss if needed.

Table 1: Component Selection Guide–LXT360/LXT361 (E1/T1, Long-Haul/Short-Haul Applications)

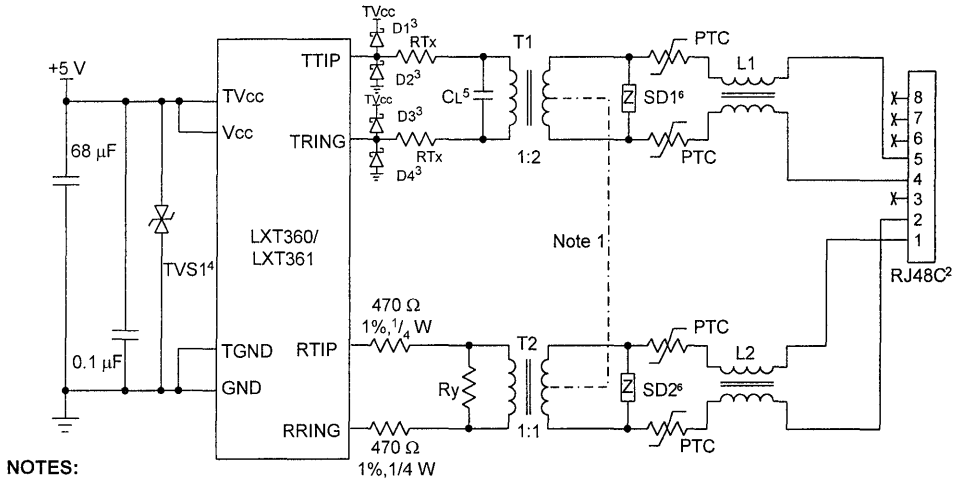
Application	Rtx[1] [Ω] 1.0% 1/8 Ω	Ry [Ω] 1.0% 1/2 Ω	Transmit Transformer[2]	Receive Transformer	EC4-1[3]			
					4	3	2	1
T1 Long-Haul 100 Ω twisted-pair lines (with line protection)	9.1	100	1:2	1:1	0	x	x	x
T1 Short-Haul 100 Ω twisted-pair lines (without line protection)	9.1	100	1:2	1:1	1 1	0 1	1 x	1 x
E1 Short-Haul 75 Ω coax lines (without line protection)	9.1	75	1:2	1:1	1	0	0	0
E1 Short-Haul 120 Ω twisted-pair lines (without line protection)	9.1	120	1:2	1:1	1	0	0	0
E1 Long-Haul 120 Ω twisted-pair/ 75 Ω coax (with line protection)	9.1	120/75	1:2	1:1	1	0	1	0
E1 Long-Haul 120 Ω twisted-pair lines (with line protection)	15	120	1:2	1:1	1	0	0	1
E1 Long-Haul 75 Ω coax lines (with line protection)	15	75	1:1.53	1:1	1	0	0	1

1. The protection circuit reduces the amplitude of the transmitted signal. Use a lower value for RTx to restore the amplitude to its nominal value. The lower value compensates for resistance of the protection resistors on the line side (PTC 4 Ω to 7 Ω used in this example).
2. The transmit and receive transformers must have a center tap (1:2 CT, 1:1 CT) to support simplex current in the E1/T1 loop if required.
3. "x" in the EC4-1 columns indicates "don't care". Refer to LXT360/361 Data Sheet for full description of transmit equalizer codes.

Table 2: Common Components for LXT360/LXT361 Applications

Ref #	Description	Typical Part (Manufacturer)	
SD1, SD2	Sidactor–Instantaneous clamping voltage 65 - 80 V TO-92 packaging	PO720EA70 (TECCOR Electronics)	
PTC	Positive Temperature Coefficient Resistors – 4 - 7 Ω, 600 V	TR600-160-RA-B-0.5-.130 (Raychem)	
LFR	Line Feed Resistor–Thermal, fused, 5.6 Ω	LFR-2-5.6-1 (IRC)	
V1	MSV Varistor–Stand-off voltage 3.7 V, Off-state capacitance ≤ 470pF	MSV701A (Microsemi)	B529-2 (EDAL Industries)
CL	Ceramic capacitor–0-470 pF, radial leaded, 50 V	any manufacturer (e.g., KEMET, AVX)	
L1, L2	RF Choke–Varies based on board design typically 33 mH	500-1164 (BH Electronics)	

Figure 1: Enhanced Line Protection Circuitry



NOTES:

1. Interconnecting transformers T1 and T2 is optional to support current looping in the E1/T1 loop.
2. Connections at RJ48C jack are for T1 CSU applications only. For E1 applications, refer to ITU standards.
3. Schottky diode 11DQ04 (International Rectifier) is a typical component for D1-4.
4. TVS1 is a 5 V bidirectional TVS. Semtech SMCJ5.0AC (surface mount part) is typical.
5. Value of Capacitor CL may vary between 0 and 470 pF to improve the transmit return loss. Test to determine the optimum value of CL for each design
6. Sidactors SD1 and SD2 can be replaced with low a capacitance TVS array. Semtech Corporation manufactures a suitable 1500 watt surface mount, low capacitance TVS array (part number LC01-6).

Figure 1 shows an enhanced version of the protection circuit for the LXT360/361 shown on the first page of this data sheet. Please notice that the circuit requires additional components, including Schottky diodes D1-4 and a 5 V bidirectional TVS (TVS1). The enhanced circuit provides better protection from metallic stresses and from surges coupled to VCC. However, these advantages come at the price of increased component count, PCB space, and a higher unit cost.

PTCs have the advantage of recovering from a stress condition once the condition disappears. Many similar designs use a Line Feed Resistor (LFR) like the **LFR-2-5.6.1** from **IRC, Inc.** An LFR is a combination precision resistor (5.6 Ω, 1%) and a thermal fuse. The primary benefit of the LFR is its stable resistance over temperature variances. However, it opens permanently and must be replaced. The affected line must be switched to a redundant circuit until the primary circuit is restored.

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Table 3: Manufacturers Mentioned in this Note

Company	Contact Information	Company	Contact Information
BH Electronics	12219 Wood Lake Drive Burnsville, MN 55337 (612) 894-9590 / Fax: (612) 894-9380	Raychem Corp	300 Constitution Drive Menlo Park, CA 94025-1164 (800) 227-2040 / Fax: (800) 227-4866
EDAL Industries	4 Short Beach Road East Haven, CT 06512 (203) 467-2591 / Fax: (203) 469-5928	SEMTECH Corp	652 Mitchell Road Newburg Park, CA 91320 (805) 498-2111 / Fax: (805) 498-3804
IRC, Inc	P.O. Box 1860 Boone, NC 28607 (704) 264-8861 / Fax: (704) 262-1972	TECCOR Electronics	1801 Hurd Drive Irving, TX 75038 (214) 580-1515 / Fax: (214) 550-1309
Microsemi Corp	8700 E. Thomas Road Scottsdale AZ 85251 (602) 941-6300 / Fax: (602) 947-1503		

NOTES

SCR Latch-up Model

Preventing Latch-up in Level One Transceivers

General Description

The purpose of this application note is to familiarize designers in the use of Level One CMOS transceivers. Level One devices are designed to meet, but not to exceed the absolute maximum specifications for Silicon Controlled Rectifier latch-up. SCR latch-up in CMOS devices is a condition that can cause maximum specifications to be exceeded. This application note provides the necessary design considerations to avoid SCR latch-up.

Following these design guidelines will:

- Avoid exceeding maximum transceiver ratings
- Simplify application maintenance
- Reduce SCR latch-up related downtime in systems
- Improve System reliability

Application Overview

Once triggered, an SCR latch-up condition turns on a parasitic SCR internal to CMOS circuits that creates a low resistance path from V_{CC} to ground. The resulting internal high currents can damage the devices.

Modeled as a cross coupled transistor, the SCR has two basic trigger mechanisms; one forces current into its gate and the other places a large voltage between anode and cathode. When forward biasing a diode, current injected into the base of Q2 turns this transistor on and the collector current (beta times its base current) flows into the base of Q1. This causes Q1 to be amplified by beta and fed back into the base of Q2, where the current is again amplified. If the beta of both transistors is greater than 1, the current gain continues until the transistors saturate and the SCR is triggered. Once the regenerative condition occurs, a large anode current flows. The SCR remains on after the gate current is removed, if enough anode current flows to sustain latch-up.

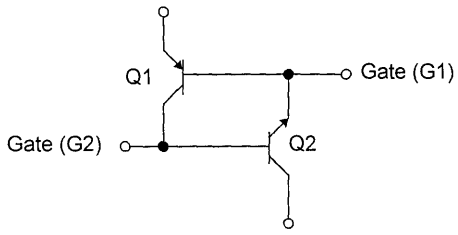
In the case of large voltages on its anode and cathode, a trigger condition can occur even if no current is applied to the gate. In the forward blocking state a small leakage current is present but will not trigger the SCR. If the voltage is increased to allow a significant leakage current, then a SCR could trigger. The beta of the NPN and PNP must be greater than one for the latch condition to occur.

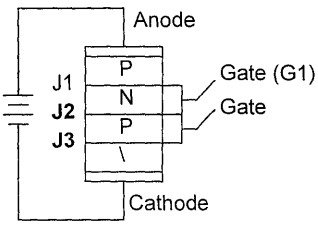
There are a number of scenarios that can cause a SCR trigger to occur at inputs and outputs (latch condition) including insertion and removal of a circuit card from a powered system. To be effectively controlled (either when integrated or at the system level) designers must have a clear understanding of the causes of SCR latch-up.

Design Guidelines

2. If the circuit card design includes "hot-swapping" capability, insure that power reaches the devices (transceivers, PALs, etc.) before applying any voltages to the input or output pins (*i.e.*, power and ground pins make contact before input and output pins).
3. With multiple power supplies feed the same device, arrange the pins so the supplies connect in ascending order. Thus, if a circuit card requires +5 V, +12 V, and -12 V, the +5 V pins should connect first, the +12 V pins next and finally the -12 V pins. In any event, before any voltage pins make contact, the ground should connect first to insure that the positive supplies do not pull the negative supplies or visa versa.

SCR Latch-Up Model





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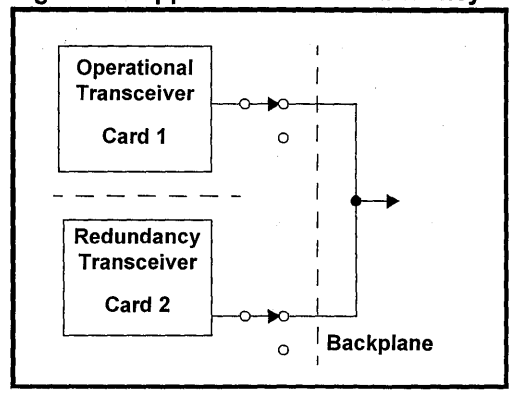
3. When devices drive other devices on separate boards be aware that large amounts of local decoupling can cause power supply ramps to be slower on some boards than others.

4. Insure that the voltages to the input/output pins do not exceed the supply voltage. Clamping circuits are needed to reduce the input voltage.

5. Insure that the input current does not exceed the absolute maximum rating of 100 mA. If this is expected, current limiting is necessary to prevent the SCR latching condition.

6. Never allow the output driver to drive another output driver in applications of redundancy (Figure 1). This can be accomplished only if a break before make connection of the two drivers is observed. These drivers are high current drivers, capable of exceeding the triggering currents necessary for a SCR latch condition.

Figure 1: Applications of Redundancy



Crystal-less E1 Long-Haul Solutions

LXT318/360 Universal Line Interface Unit Design Guide

Introduction

This note describes applications for the crystal-less LXT360 transceiver in newer generation network access equipment. Use this application note as a guide when upgrading designs using the LXT360. Before designing a circuit using this new device, refer to the data sheets for both devices for complete information.

The LXT360 provides several advanced features. While the LXT360 provides for both T1 (1.544 Mbps) and E1 (2.044 Mbps) operation, this application note focuses only on hardware-controlled, E1 designs. Additional application notes detail migration paths for T1 and E1 design using other LXT360 features.

Identifying Major LXT360 Design Improvements

Jitter Attenuation Circuitry

- The LXT318 device requires a pullable 8.192 MHz crystal to provide selectable jitter attenuation. The jitter attenuation circuitry may be in either the transmit or the receive path, depending on the application.
- The LXT360 requires only the MCLK signal to provide the same selectable jitter attenuation functions since it uses digital JA circuitry. It needs no crystal or high-frequency external clock for jitter attenuation.

External Clock Requirements

- The MCLK input signal in the LXT318 is optional. If used, the clock must have an accuracy of ±100 ppm.
- The MCLK input signal in the LXT360 is mandatory. The clock must be a stand alone reference with an accuracy of ±32 ppm or better at 2.048 MHz for E1 applications.

Applications

- The LXT318 is a long-haul E1 transceiver only.
- The LXT360 operates as either a short- or long-haul transceiver in E1 or T1 applications.

Available Line Coding Schemes

- The LXT318 allows HDB3 encoding in either Unipolar or Bipolar mode.
- The LXT360 transceiver offers HDB3 line encoding only in the Unipolar Mode.

Reset Operation

- Reset on the LXT318 occurs when both LLOOP and RLOOP inputs are pulled High while TAOS is pulled Low for at least 200 ns.
- Reset on the LXT360 occurs when LLOOP, RLOOP and TAOS are pulled High simultaneously for at least 200 ns.

Output Control

- The LXT318 provides a high-impedance state option for the TTIP/TRING outputs only when TCLK is grounded.
- The LXT360 provides high-impedance state limited to the TTIP/TRING outputs when TCLK is pulled High. An additional high-impedance state option is available for all output pins when TRSTE is pulled High.

Line Attenuation Indication

- The LXT318 provides Line Attenuation Indication (LATN) in both Hardware and Host Modes.
- The LXT360 provides LATN in Software Mode only.

NLOOP Detection

- For the LXT318 transceiver, holding RLOOP, LLOOP and TAOS High simultaneously for 200 ns and then pulling all three Low enables the NLOOP detection function. Alternatively, tying RCLK to RLOOP also enables NLOOP. Resetting the device disables NLOOP detection.
- In the LXT360 setting the RLOOP input to 2.5 V ±0.2 V ("Midrange") enables NLOOP detection. Setting RLOOP Low or High disables NLOOP detection.

Loss of Signal Detection and LOS Clear Criteria

- The LXT318 device declares a Loss Of Signal (LOS) condition when it detects 175 consecutive spaces. It clears the LOS condition when the receiver detects 12.5% mark density (*i.e.*, 4 marks within a 32-bit period) with no more than 15 consecutive 0s.
- The LXT360 transceiver declares the LOS condition when it detects 32 consecutive spaces. It clears the LOS condition when the receiver detects 12.5% mark density (*i.e.*, 4 marks within a 32-bit period) with no more than 15 consecutive 0s.

DIAGNOSTIC FUNCTIONS

The LXT360 provides several diagnostic features not provided on the LXT318 transceiver. These are Dual Loopback function, Error Insertion and Detection, AIS Condition Monitoring and Elastic Store Pointer Monitoring. Refer to the LXT360 data sheet for details on these functions.

In addition, the LXT360 provides both a Quasi-Random Signal Source and a Detector for diagnostic procedures.

Three-State Input Pins

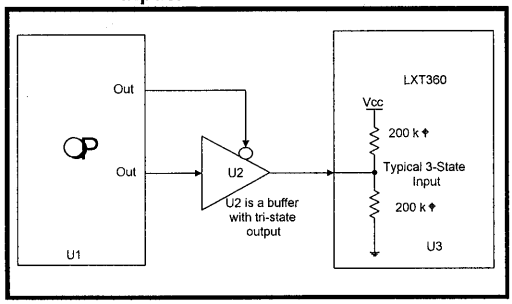
The LXT318 uses two-state (High and Low) configuration inputs but some LXT360 control inputs recognize three states. Typical values for these states are:

High–$V_{IN} > 3.5$ V.
Midrange–2.3 V $\leq V_{IN} \leq$ 2.7 V (or floating).
Low–$V_{IN} < 1.5$ V.

The control for three-state inputs may be a standard tri-state buffer. Figure 1 shows a typical driver circuit for these inputs. Setting the output buffer to its high-impedance state places the three-state input into its Midrange state.

Application designers must take into account the current drawn by the internal resistors (part of each three-state input) before choosing a buffer to drive these inputs to their High or Low states.

Figure 1: Typical Circuit for LXT360 Three-State Inputs



Line Interface Considerations

To improve transmit return loss, add a capacitor (C_{TX}) to the transmit side as shown in Figures 2 through 4. This capacitor is typically 470 pF, but may vary depending on the resistor and transformer values, the board layout and the parasitics of the protection diodes.

Tables 1 through 3 show the combinations of transformers, resistors and capacitors needed for the transmit side as shown in these applications. Table 4 lists transformers that meet Level One Communications specifications when tested with the LXT360 device.

Table 1: Transmit Return Loss (2.048 Mbit/s–Short-Haul 12 dB)

EC4-1	Xfrmr/ Rt	Xmission Line	C_{TX} (pF)	Return Loss (dB)
1000	1:2/ 9.1 W	75 Ω Coax	0	14
			470	16
		120 Ω Twisted Pair	470	13
	1:2.3/ 9.1 W	120 Ω Twisted Pair	0	13
			470	16

Table 2: Transmit Return Loss (2.048 Mbit/s–Long-Haul 43 dB) High Return Loss Configuration

EC4-1	Xfrmr/ Rt	Xmission Line	C_{TX} (pF)	Return Loss (dB)
1001	1:2/ 15 W	120 Ω Twisted Pair	0	19
			470	28
	1:1.53/ 15 W	75 Ω Coax	0	18
			470	28

Table 3: Transmit Return Loss (2.048 Mbit/s–Long-Haul 43 dB)

EC4-1	Xfrmr/ Rt	Xmission Line	C_{TX} (pF)	Return Loss (dB)
1010	1:2/ 9.1 W	120 Ω Twisted Pair	0	12
			470	13
		75 Ω Coax	0	16
			470	18

Table 4: Recommended Transformers for LXT360

Transmit Side			Receive Side		
Transformer Turns Ratio	**Manufacturer**	**Part Number**	**Transformer Turns Ratio**	**Manufacturer**	**Part Number**
1:2	Fil-Mag	FE 66Z1308	1:1	Fil-Mag	FE 80006-155
	HALO	TD 61-1205G		HALO	TD 61-1205G
		TD 67-1205G			TD 67-1205G
	Midcom	671-5832		Midcom	671-5792
	Pulse Engineering	PE-65351		Pulse Engineering	PE-64936
		PE-65771			PE-65778
	Schott Corp	67127370		Schott Corp	67109150
		67130850			67130840
1:1.53	Pulse Engineering	PE 68663			

Bipolar Mode with AMI Line Coding (without Zero Suppression)

Most pins on LXT360 have the same names and functions as those on the LXT318, although some differ. This section describes the modifications needed to change from the LXT318 to the LXT360 in Hardware Control Mode. The LXT360 pins not included in this discussion have the same connections and signal level requirements as those on the LXT318. Table 5 is a summary of the pins whose functions change when moving from LXT318 to LXT360.

The 8.192 MHz crystal required by the LXT318 must be deleted when migrating to the LXT360. The functions on pins 17, 18, and 23 on the LXT318 change pin locations on the LXT360 transceiver. **Pay particular attention to the new locations for these signals**. Figure 2 shows the connection differences between the two transceivers for this configuration.

Pin 1: The LXT360 requires an independent, external clock called MCLK. The MCLK input signal must have a nominal rate of 2.048 MHz and an accuracy of ±32 ppm or better. The LXT318 uses the same nominal frequency, but requires no better accuracy than ±100 ppm.

Pin 5: In the LXT318, pin 5 is called MODE. This pin can be pulled High or Low, or it can be tied to the RCLK pin. The RCLK signal at the MODE pin enables the HDB3 encoders and decoders.

In the LXT360, the MODE pin is a three-state input pin: High, Low or Midrange. Setting the pin to Midrange enables the HDB3 encoders and decoders in LXT360 for E1 applications (and also forces the transceiver into unipolar operation).

Pin 9: In LXT360, pin 9 is called TRSTE. It is a three-state input. With TRSTE pulled High all LXT360 device output pins go into a high-impedance state. In conjunction with MODE (pin 5), this pin also sets the operational mode of the transceiver.

To enable E1, Long-Haul (43 dB), Bipolar, Hardware Control Mode, the TRSTE pin must be pulled Low. See the data sheet for a complete description of the operating modes.

Pin 10: This pin is the XTALOUT input on the LXT318. Leave this pin not connected on the LXT360.

Pin 17: Pin 17 is grounded in LXT318 applications. In the LXT360, pull pin 17 (EC4) High to enable E1 long-haul operation.

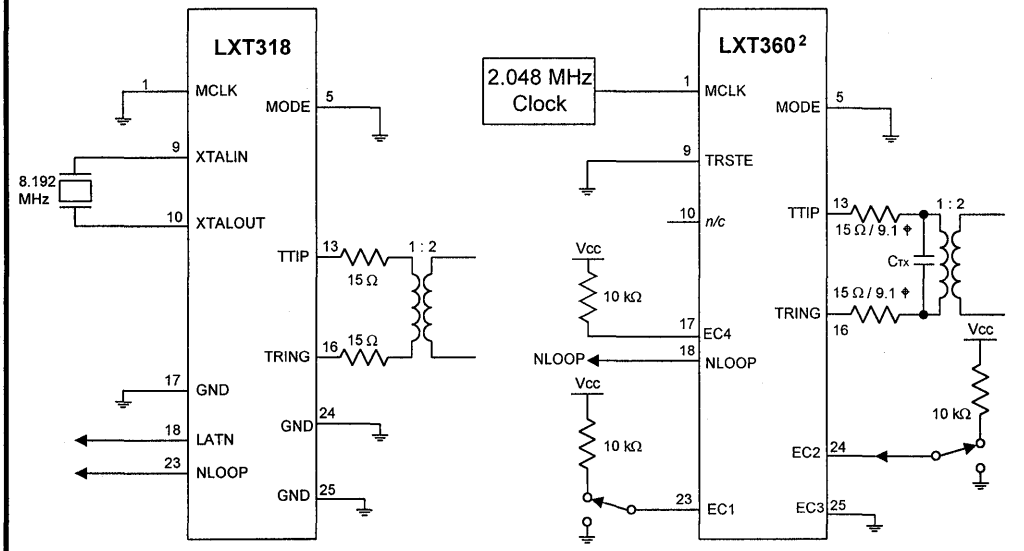
Pin 18: The LXT318 pin 18 signal (NLOOP) appears on pin 23 of the LXT360.

The LATN signal, which is on pin 18 of the LXT318, is not available in the Hardware Mode on the LXT360. However, a binary encoded equivalent to LATN is provided in the LXT360 Software Mode.

Pin 23: The NLOOP signal, which appears on pin 23 of the LXT318, is available on pin 18 of the LXT360.

Pins 24 and 25: In the LXT318, pins 24 and 25 are both grounded. The LXT360 uses these pins and gives them the names EC2 (pin 24) and EC3 (pin 25). EC4-1 control the equalizers on the LXT360. See the LXT360 Data Sheet for details.

Figure 2: Bipolar Mode Using AMI Line Coding (without Zero Suppression)[1]



NOTE:

1. Pins not shown on this figure have the same function on both the LXT318 and LXT360. They do not require modification for proper functioning.

Table 5: Bipolar Mode using AMI Line Coding (without Zero Suppression)

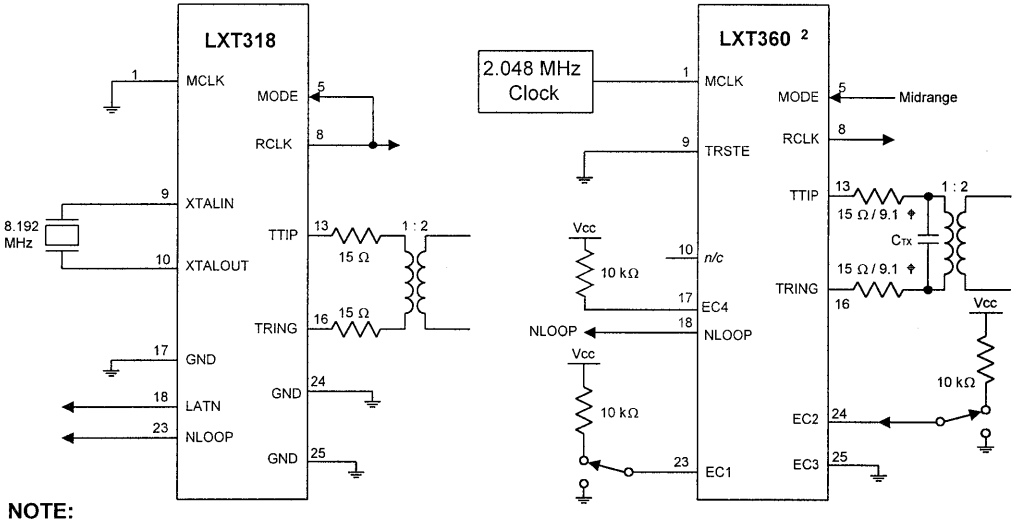
Pin#	LXT318		LXT360		Comments
	Name	Function/State	Name	Function/State	
1	MCLK[1]	2.048 MHz/GND	MCLK	2.048 MHz	Mandatory in LXT360 applications
5	MODE	Low	MODE	Low	MODE and TRSTE set operation mode
9	XTALIN	8.192 MHz Crystal	TRSTE	Low	Crystal not used in LXT360
10	XTALOUT	8.192 MHz Crystal	—	*n/c*	No function assigned to this pin.
17	GND	–	EC4	Input–High	EC4 = High for E1 operation.
18	LATN	Output	NLOOP	Output	LATN not supported on LXT360 in Hardware Control Mode. NLOOP changes location.
23	NLOOP	Output	EC1	Input	
24	GND	Low	EC2	Input	Refer to Table 12 in LXT360 Data Sheet.
25	GND	Low	EC3	Input/Low	

[1] MCLK is optional in LXT318 applications. With the LXT318, if MCLK is not supplied, pin 1 must be grounded.

Using HDB3 Encoding/Decoding

The LXT318 supports HDB3 encoding/decoding in both Unipolar and Bipolar Modes. The LXT360 configures itself in Unipolar mode (*i.e.*, TPOS becomes TDATA and TNEG becomes INSBPV) when HDB3 is enabled. To enable HDB3 encoders and decoders, set the MODE pin to Midrange. Other connections are the same as for AMI line coding. Figure 3 shows the changes needed in connections for LXT318 and LXT360. See Table 6 for a summary of the modifications needed to adapt an LXT318 application to the LXT360.

Figure 3: Unipolar Mode (with HDB3 Zero Suppression)[1]



NOTE:

1. Pins not shown on this figure have the same function on both the LXT318 and LXT360. They do not require modification for proper functioning.

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Table 6: Unipolar Mode with HDB3 Zero Suppression Enabled

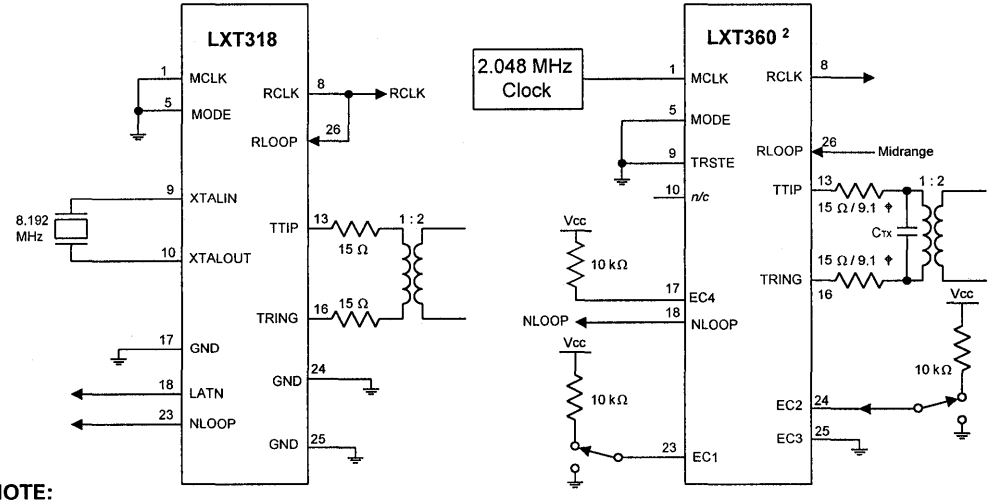
Pin#	LXT318		LXT360		Comments
	Name	Function/State	Name	Function/State	
1	MCLK[1]	2.048 MHz/GND	MCLK	2.048 MHz	Mandatory in LXT360 applications
5	MODE	Tie to RCLK	MODE	Midrange[2]	MODE and TRSTE set operation mode Crystal not used in LXT360
9	XTALIN	8.192 MHz Crystal	TRSTE	Low	
10	XTALOUT	8.192 MHz Crystal	—	*n/c*	
17	GND	–	EC4	Input–High	EC4 = High for E1 operation
18	LATN	Output	NLOOP	Output	LATN not supported on LXT360 in Hardware Control Mode. NLOOP changes location.
23	NLOOP	Output	EC1	Input	
24	GND	Low	EC2	Input	Refer to Table 12 in LXT360 Data Sheet.
25	GND	Low	EC3	Input/Low	

[1] MCLK is optional in LXT318 applications. With the LXT318, if MCLK is not supplied, pin 1 must be grounded.
7."Midrange" means leave the pin unconnected or tie it to 2.5 V.

Enabling NLOOP Detection

Tying the RLOOP and MODE inputs to the RCLK output enables Network Loop detection (NLOOP) on the LXT318 transceiver. NLOOP is also enabled by holding LLOOP, RLOOP, and TAOS all High simultaneously for 200 ns and pulling them Low. To enable NLOOP on the LXT360 transceiver, tie the RLOOP input pin to Midrange as in Figure 4. This function is available only in Bipolar Mode.

Figure 4: Bipolar Mode [1]



NOTE:

1. Pins not shown on this figure have the same function on both the LXT318 and LXT360. They do not require modification for proper functioning.

Migration from CS61574A/CS61575 to LXT350 T1/E1 Short-Haul Transceiver

Introduction

This application note provides guidelines for converting an existing design that utilizes the CS61574A/CS61575 to the Level One LXT350. The LXT350 is a new generation crystal-less T1/E1 LIU. Although it does require some minor schematic/PCB changes, migration from CS61574A/75 to LXT350 is straightforward. Our focus in this note is on three major operational modes of the CS61574A/75:

- Hardware Mode
- Extended Hardware Mode
- Software (Host) Mode

The advantages of the LXT350 over the CS61574A/75 are:

- The LXT350 does not require a pullable quartz crystal to perform jitter attenuation
- Cost, component and board space savings with the LXT350 are significant in high density T1 or E1 systems (2 or more T1/E1 lines per system)
- The master clock (MCLK) can be supplied to all LIUs from one common clock source, compared to the CS61574A/75's requirement of one crystal per LIU
- Jitter attenuation is selectable between the transmit and receive path
- The low frequency of MCLK (1.544 MHz for T1 and 2.048 for E1) helps to keep electromagnetic emissions at a lower level
- Superior transmit return loss with external resistors
- External resistors on TTIP and TRING provide a first order protection from environmental hazards, such as AC power-cross, electrostatic discharge, lightning and other surges
- On-chip QRSS pattern generation/detection and analog loopback available
- Driver short circuit current is limited to 50 mA per OFTEL/BABT recommendations
- In Host Mode of operation, the LXT350 supports two different criteria for loss of signal (LOS/E1)
- Level One's LXT350 requires only one type of transformer for both T1 and E1 applications (at 1:2 turn ratio) and facilitates dual mode T1/E1 designs
- Tristate output drivers support protection switching applications
- A design based on the LXT350 can easily be upgraded to the Universal T1/E1 Long-Haul/Short-Haul LIU LXT360
- Software selectable T1 or E1 operation mode without component changes
- Available in standard 28-pin DIP and PLCC, as well as 44-pin PQFP package

Jitter Attenuation Circuitry

The CS61574A/75 requires a 6.176 MHz (T1)/8.192 MHz (E1) pullable crystal to perform jitter attenuation. In some applications, the CS61574A/75 also needs an ACLKI signal at 1.544 MHz/2.048 MHz. The LXT350 only requires a MCLK clock signal. MCLK is 1.544 MHz ±32 ppm for T1 applications and 2.048 MHz ±32 ppm for E1 operation. The digital jitter attenuator has a corner frequency of 3 Hz and low latency time.

Hardware Operation Modes

Figures associated with each mode of operation show which pins of the CS61574A/75 transceiver require modifications. Pins not shown do not require changes when migrating from CS61574A/75 devices to the LXT350. It is recommended to have data sheets available for the LXT350 and the CS61574A/75 when working with this application note.

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* Pin numbers specified apply to 28-pin DIP and PLCC packages only

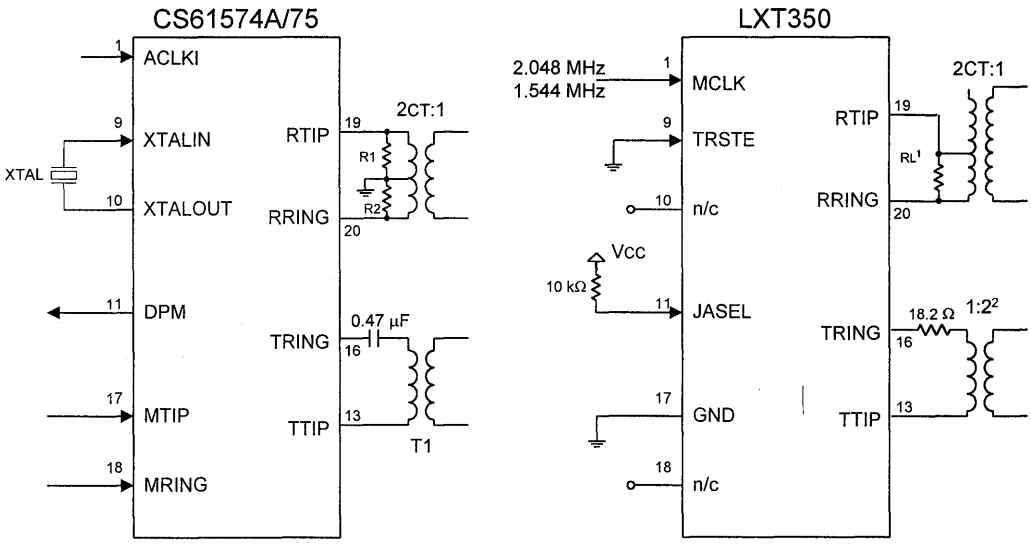
Hardware Mode with External Encoding and Jitter Attenuation

Figure 1 shows all the pins/signals of the CS61574A/75 which need to be modified when migrating to the LXT350 from CS61574A/75 in Hardware Mode with external line coding. Pins/signals not shown are identical for both devices. The LXT350 does not support DPM and MTIP/MRING features in Hardware Mode.

The following changes/steps are needed for the conversion:

- Supply 1.544 or 2.048 MHz clock with ±32 ppm stability to pin 1 (MCLK)
- Remove the crystal (XTAL)
- Pull pin 9 LOW*
- leave pin 10 not connected(floating) *
- Pull pin 11 HIGH (to place JA in receive path on LXT350) *
- Ground pin 17 *
- Leave pin 18 not connected or floating *
- Modify physical interface to the line as shown in Figure 1
  - Replace 0.47µF capacitor with a series resistor
  - Change Tx/Rx transformers and termination resistors as shown on Figure 1
- If the CS61574A/75 does not use JA, leave pin 11 on LXT350 floating (or not connected) *

Figure 1: Bipolar Hardware Mode with External Encoding



NOTES:

1. R_L = 100 Ω for DSX-1 applications; 120 Ω for E1/120 Ω twisted pair applications; 75 Ω for E1/75 Ω coax applications
2. Refer to the LXT350 data sheet for more information on transmit side transformers, capacitors, and RTX resistor selection.

* Pin numbers specified apply to 28-pin DIP and PLCC packages only

Extended Hardware Mode with B8ZS/HDB3 Encoder/Decoder and Jitter Attenuation

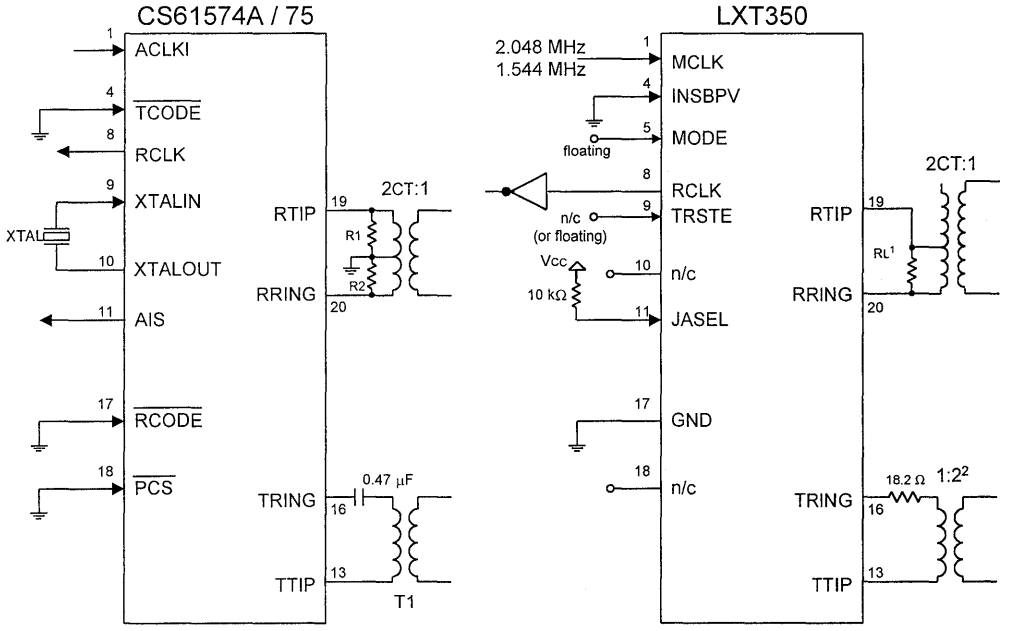
The CS61574A/75 must be used in Extended Hardware mode for applications which require B8ZS (T1) or HDB3 (E1) encoding/decoding. The LXT350 mode that corresponds to Extended Hardware Mode of CS61574A/75 is Hardware Unipolar Mode.

Figure 2 shows how to migrate from CS61574A/75 in Extended Hardware Mode with B8ZS/HDB3 encoder/decoder enabled to LXT350 and JA in the receive path. Please notice that pin 11 (AIS) on CS61574A becomes JASEL on LXT350. Pins/signals not shown are identical for both devices.

The following changes/steps are needed for the conversion:

- Supply 1.544 (T1) or 2.048 (E1) MHz clock with ±32 ppm stability to pin 1 (MCLK)
- Ground permanently (or pull LOW) pins 4 and 17*
- Receive clock (RCLK) signal on the LXT350 must be inverted to comply with the phase of CS61574A/75's RCLK. Add an inverter.
- Leave pins 9,10,18 of the LXT350 not connected*
- Pull pin 11 High (to place JA in the receive path on LXT350) *
- Modify physical interface to the line (TX and RX) as shown on Figure 2
  - Replace the 0.47 µF capacitor with a series resistor
  - Change Tx/Rx transformers and termination resistors as shown on Figure 2

Figure 2: Extended Hardware Mode With B8ZS/HDB3 Encoder/Decoder And JA



NOTES:

1. R_L = 100 Ω for DSX-1 applications
   R_L = 120 Ω for E1/120 Ω twisted pair applications
   R_L = 75 Ω for E1/75 Ω coax applications
2. Refer to the LXT350 data sheet for more information on transmit side transformers, capacitors, and R_{TX} resistor selection.

9

* Pin numbers specified apply to 28-pin DIP and PLCC packages only

Extended Hardware Mode with Internal AMI Encoding/Decoding

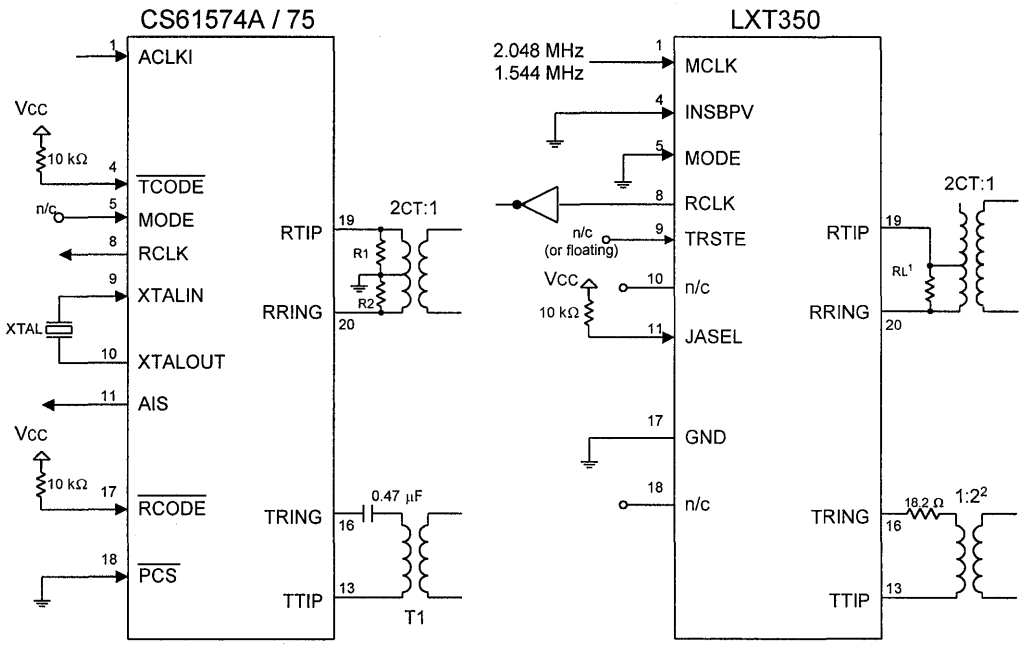
Like the LXT350, the CS61574A/75 can be configured to operate in Extended H/W Mode with internal AMI encoder/decoder turned on. However, there are some slight differences in configuring the two devices. For the Crystal device to operate in this mode, input $\overline{\text{TCODE}}$ and input $\overline{\text{RCODE}}$ must be pulled High.

Figure 3 shows the pin-to-pin modifications necessary to migrate from CS61574A/75 to LXT350 in Extended H/W mode with AMI encoding/decoding. Pins/signals not shown are identical for both devices.

The following changes/steps are required for the conversion:

- Supply 1.544 MHz ± 32 ppm (T1) or 2.048 ± 32 ppm (E1) clock signal to pin 1.*
- Ground or pull Low pins 4, 5, 17*
- Invert signal on pin 8 (RCLK)*
- Remove the crystal (XTAL)
- Leave pins 9, 10, 18 not connected*
- Pull pin 11 High to place jitter attenuator in the receive path*
- Modify physical interface to the transmit and receive lines as shown in Figure 3
- Replace the 0.47 µF capacitor with a series resistor
- Change Transmit/Receive transformers and line matching resistors as shown in Figure 3

Figure 3: Extended Hardware Mode with AMI Encoders/Decoders and Jitter Attenuation



NOTES:

1. R_L = 100 Ω for DSX-1 applications
   R_L = 120 Ω for E1/120 Ω twisted pair applications
   R_L = 75 Ω for E1/75 Ω coax applications
2. Refer to the LXT350 data sheet for more information on transmit side transformers, capacitors, and RTX resistor selection.

* Pin numbers specified apply to 28-pin DIP and PLCC packages only

HOST (SOFTWARE) MODE

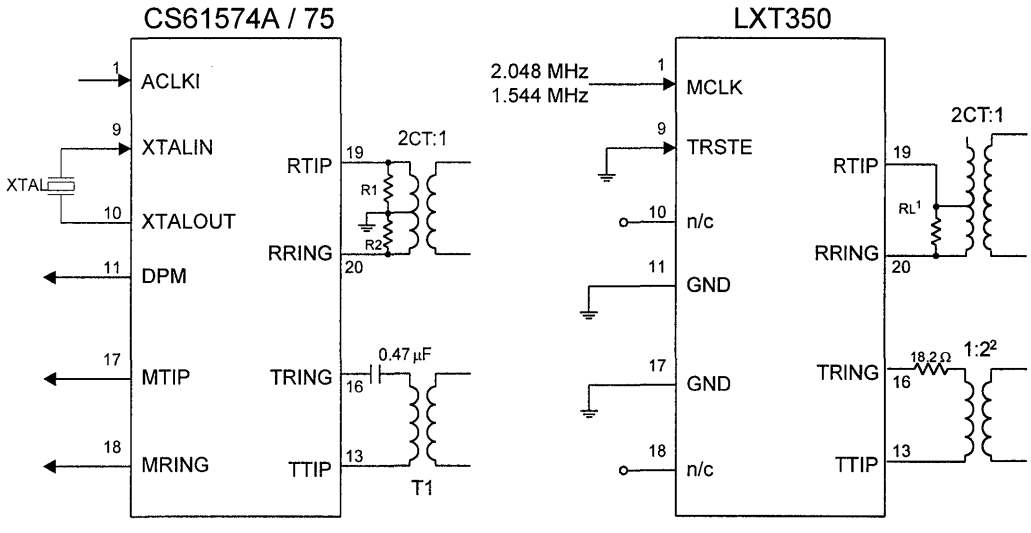
The LXT350 offers many unique features in Host Mode which are not available on CS61574A/75. Refer to the LXT350 Data Sheet for a complete description of all available features.

Migration from CS61574A/75 to LXT350 in software mode requires very few changes. The designer has to be aware of differences in register sets for CS61574A/75 and LXT350. Code changes are required when migrating from CS61574A/75 to LXT350. Figure 4 presents the required modifications. Pins/signals not shown are identical on both devices.

The following changes are needed for the conversion:

- Supply 1.544 (T1) or 2.048 (E1) MHz clock with ±32 ppm stability to pin 1 (MCLK)
- Remove the crystal (XTAL)
- Ground (or pull LOW pins 9, 11, 17) *
- Leave pins 10 and 18 not connected or floating *
- Modify the physical interface to the transmit and receive line as shown on Figure 4
  - Replace the 0.47 µF capacitor with a series resistor
  - Change Tx/Rx transformers and termination resistors as shown in Figure 4

Figure 4: Host Mode Migration



NOTES:

1. R_L = 100 Ω for DSX-1 applications
   R_L = 120 Ω for E1/120 Ω twisted pair applications
   R_L = 75 Ω for E1/75 Ω coax applications
2. Refer to the LXT350 data sheet for more information on transmit side transformers, capacitors, and R_{TX} resistor selection.

9

* Pin numbers specified apply to 28-pin DIP and PLCC packages only

MORE INFORMATION

For more detailed descriptions of the LXT350's operational modes and test specifications, consult the LXT350 data sheet. Level One literature can be obtained through your area Level One sales representative, or by contacting any of our corporate offices listed on the back of this application note.

* Pin numbers specified apply to 28-pin DIP and PLCC packages only

Migration from LXT324 to LXT325

Design Guidelines

Board Design Overview

This Application Note explains how to upgrade an existing LXT324-based design to accommodate the LXT325 Quad Receiver. Although both the LXT324 and LXT325 are Quad T1/E1 receivers, PC board modifications are required for proper implementation of the LXT325. By using either the 28-pin DIP or PLCC package, you will have drop-in compatability at the chip level. The two devices are functionally similar. The only difference is in the availability of a Loss of Signal feature in the LXT325. The LXT325 has four LOS outputs—one for each receive channel.

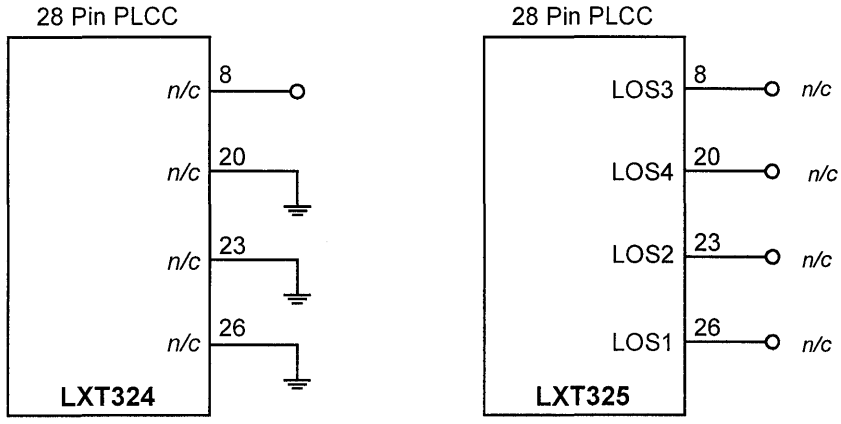
The LXT324 Data Sheet recommends that pins 20, 23 and 26 be grounded (using the 28-pin PLCC package). These pins are LOS outputs on the LXT325 and are not grounded. The table below shows the pin changes for both the 28-pin DIP and 28-pin PLCC packages.

No other changes are required in the device upgrade. The LXT325 will give the same or better performance than its predecessor, with minimal effort in making the transition.

Table 1: Changes to Pin Configuration–LXT324 to LXT325

LXT324/325 Pin #		LXT324 Required Pin Status	LXT325 Required Pin Status	Comments
28-pin DIP	28-pin PLCC			
7	8	Not Connected (*n/c*)	Not Connected (LOS3)	No PC board change
19	20	Ground (GND)	Not Connected (LOS4)	PC board change
22	23	Ground (GND)	Not Connected (LOS2)	PC board change
25	26	Ground (GND)	Not Connected (LOS1)	PC board change

Figure 1: Comparison of LXT324 and LXT325 Pin Configuration



NOTE: Leave all LOS outputs (LOS1, LOS2, LOS3, LOS4) not connected when replacing the LXT324 with the LXT325 Receiver.

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NOTES

Universal 120/100/75 Ohm Transceiver Termination for the LXT35x/36x

Introduction

This application note describes an example of a universal transceiver termination for T1/E1 designs which implement Level One LXT350/51 and LXT360/361 transceivers.

For each mode of operation (T1/E1), termination requirements differ. T1 designs require 100 Ω termination. At E1 rates, either 120 Ω or 75 Ω termination can be utilized. Programmable T1/E1 receiver termination helps to take full advantage of the universality of Level One LIUs.

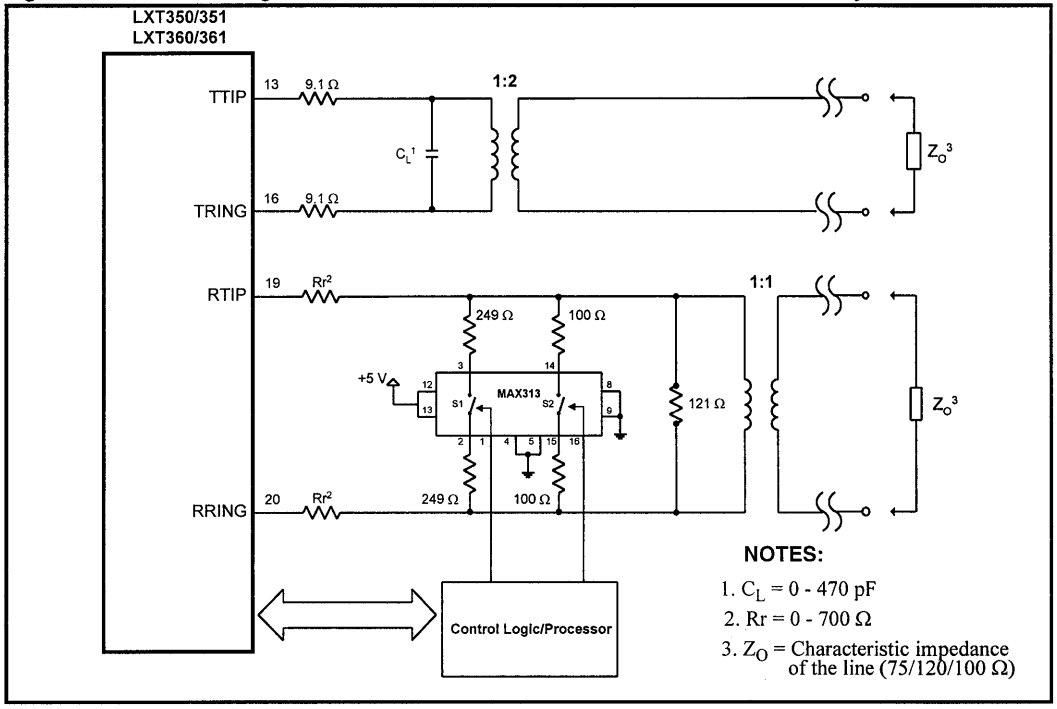
Changes to the receive side of the LIU should be done in a way that they do not impair the performance of the LIU. Receiver range (sensitivity) and noise immunity should not be affected. Additionally, it is important that the added circuitry does not impact the compliance to industry standards for receive return loss. The best way to accomplish such requirements is to employ terminating resistors that are as close as possible to the characteristic impedance of the line (T1: 100 Ω; E1: 120/75 Ω).

Termination Solutions

Figure 1 presents programmable resistive termination for both T1 and E1 designs, when deploying Level One Universal LIUs. Programmability is accomplished with a Maxim analog switch and control logic. In this case, the Max313, a quad single-pole/single-throw (SPST) analog switch, is used. The Max313 is normally open (NO) and features a low on-resistance (10 Ω maximum, 6.5 Ω typical). It offers low power consumption, low leakage over temperature, and low cost. A quad switch is recommended for designs with multiple T1/E1 ports per card. Single and dual analog switches are also available.

All shown resistors are standard values and 1% tolerance. The receive transformer has a 1:1 ratio, as recommended in the LXT360 data sheet. Table 1 shows how to select/program required termination resistance with switches S1 and S2. Resistors Rr are recommended to be between 0 and 700 Ω.

Figure 1: Universal Programmable T1/E1 Line Interface without Protection Circuitry



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PROTECTION CIRCUITRY

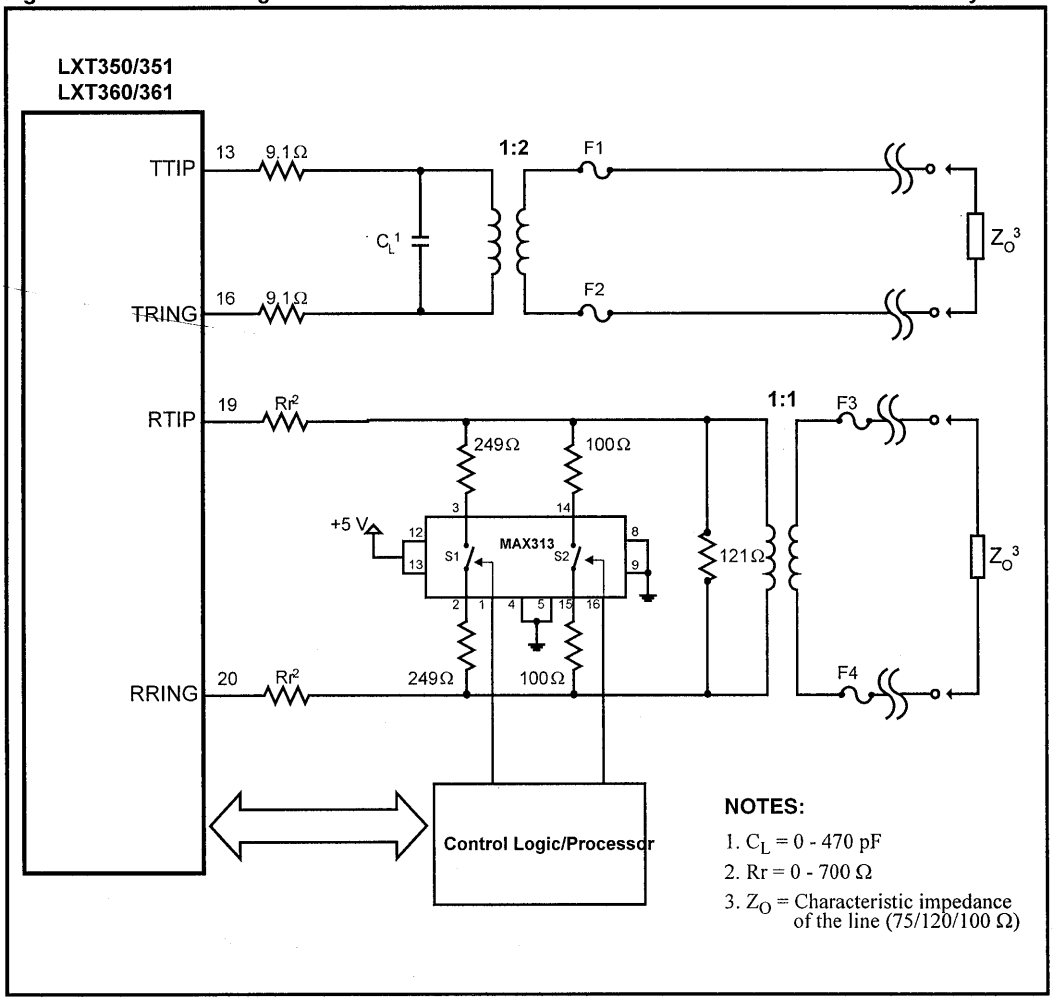
For the purpose of clarity, Figure 1 shows the basic configuration without power cross and lightning protection. However, most long-haul applications require protection circuitry. Figures 2 and 3 show how to design T1/E1 programmable LIU when protection circuitry is required. The design in Figure 2 utilizes fuses F1-F4, while Figure 3 employs PTCs or fused resistors. Fuses and resistors/PTCs are current-limiting components. A more extensive discussion on lightning and power-cross protection circuitry can be found in Application Note 47: *LXT360 Line Protection Circuitry.*

When fuses are used in the protection circuit, all resistors should be the same as in Figure 1. Fuses have very low resistance (near 0 Ω), and have no impact on the transmitted signal amplitude or receiver input impedance.

Table 1: Impedance Options by Switch Setting

S1	S2	Impedance
Off	Off	120 Ω
Off	On	75 Ω
On	Off	100 Ω
On	On	Do Not Use

Figure 2: Universal Programmable T1/E1 Line Interface with Fuses used in Protection Circuitry

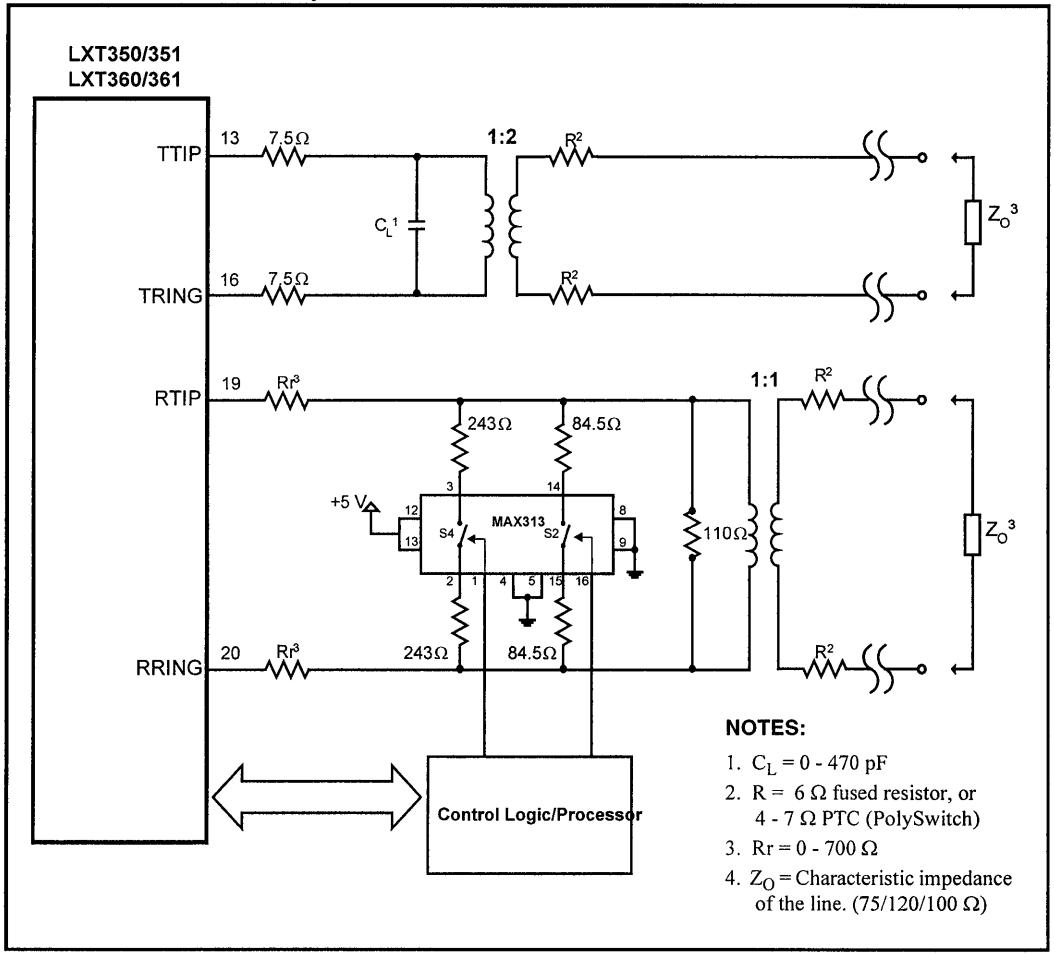


If the line card is protected by PTCs or fused resistors, the effect on line resistors must be taken into account. This includes reduction in the amplitude of the transmitted signal and changes to the input impedance on the receive side. To compensate, change the values of the resistors on both the transmit and receive side. Figure 3 shows a design with 6 Ω resistors or equivalent PTCs (PolySwitch). Notice that TTIP and TRING have changed from 9.1 Ω to 7.5 Ω. Also termination on the receive side is adjusted to compensate for protection resistors (R=6Ω).

BOARD DESIGN RECOMMENDATION

It is prudent to keep signal paths between the transceiver and edge connector as short and symmetrical as possible. For best results, place the switching component very close to the LIU.

Figure 3: Universal Programmable T1/E1 Line Interface with Resistive Components used in Protection Circuitry



9

NOTES

Designing an ITU G.742 Compliant PDH Multiplexer with the LXT332 Dual Transceiver

Introduction

This Application Note summarizes jitter performance requirements at the E1 line interface for digital multiplexing equipment as specified in ITU G.742. Appropriate conformance testing procedures using the SXT6234 PDH multiplexer device are explained. Typical performance results using the LXT332 E1 dual line interface are presented, showing that the combination of this transceiver with the SXT6234 provides a highly integrated solution when designing PDH multiplexing equipment with G.742 compliance requirements.

Recommendation G.742

The ITU-T recommendation G.742 specifies "second order digital multiplex equipment operating at 8448 Kbit/s and using positive justification". In other words, G.742 specifies the multiplexing of four E1 2.048 Mbps data streams into a single E2 8.448 Mbps signal using a positive justification mechanism. This kind of system can be easily implemented using the configuration shown in Figure 1.

The LXT332 dual E1 line interface provides a high level of integration and a digital crystal-less jitter attenuator. The SXT6234 provides a single chip solution for multiplexing the four E1 signals into one E2 8.448 Mbps aggregate signal. In addition, by using the configuration illustrated in Figure 2, an E1 to E3 multiplexer can also be easily implemented.

For the E1 tributary output ports, recommendation G.742 specifies that "the peak to peak jitter at a tributary output in the absence of input jitter should not exceed 0.25 UI when measured in the frequency range up to 100 KHz". The lower frequency limit should be as low as possible taking into account the limitations of measuring equipment.

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Figure 1: E1 to E2 Multiplexer

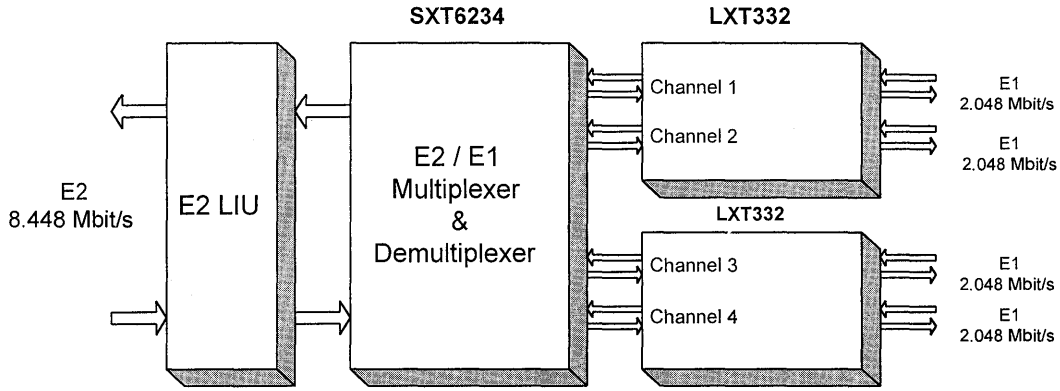
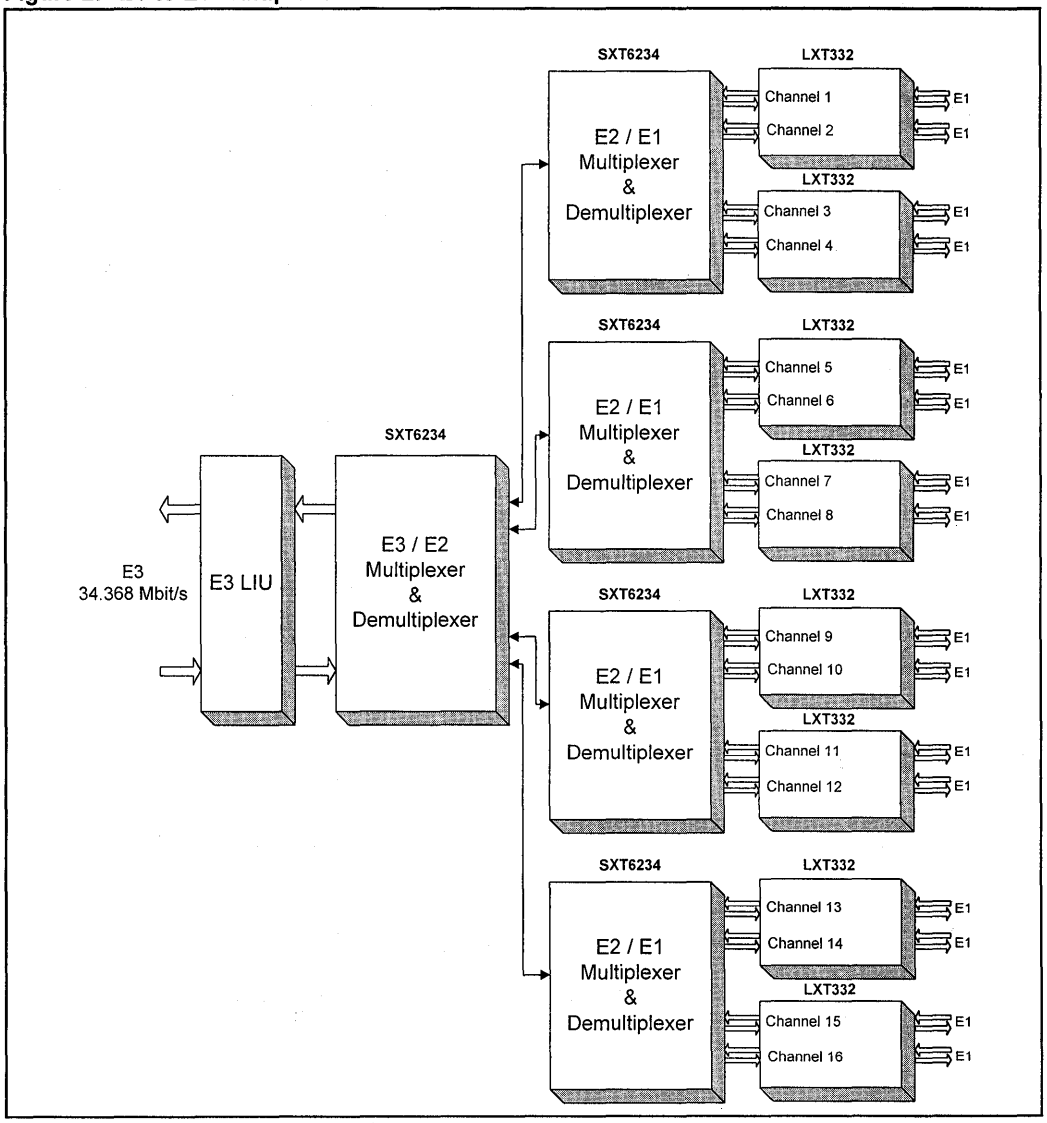


Figure 2: E1 to E3 Multiplexer



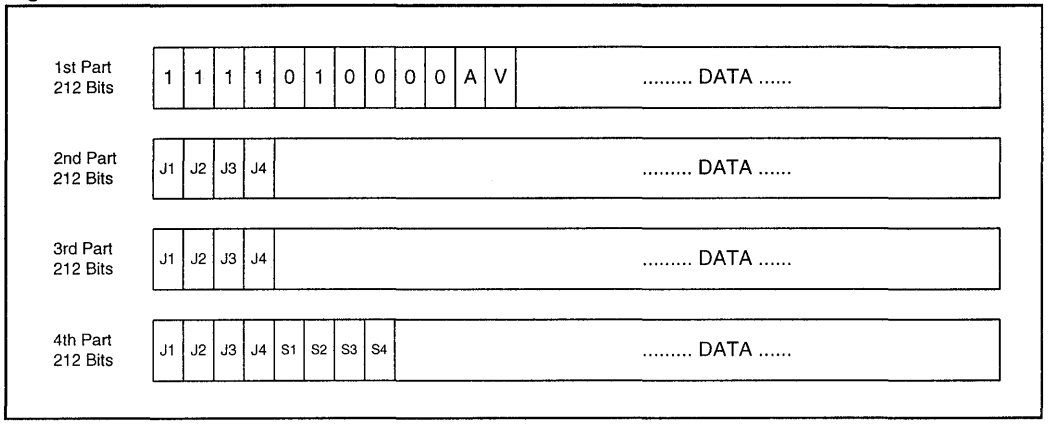
In the absence of jitter at the aggregate (E2) port, the two main sources of jitter that should be attenuated by the LXT332 jitter attenuator are the Multiplexing Jitter and the Stuffing Jitter. Both jitter sources result from extracting an E1 tributary out of the E2 frame. Figure 3 represents an E2 frame as described in G.742.

Multiplexing Jitter is due to clock gaps in the E1 transmission clock. These gaps occur as a result of discarding fixed control bits out of the E2 frame. This process translates into fixed 3-bit wide gaps from discarding the frame alignment word plus control bits (A,V) and 1-bit wide gaps from discarding the justification control bits (J1 to J4). These gaps occur at a fixed 8 KHz rate and have a fixed amplitude. The jitter component they originate is easily handled by the LXT332 jitter attenuator.

Stuffing Jitter is a consequence of the positive justification mechanism used to build the E2 frame. This mechanism is necessary to adapt the tributary E1 clock rate to the aggregate E2 clock rate. Normally , the S*n* bits (Stuff bits) in the E2 frame carry information pertaining to one of the tributaries. When a justification is needed to compensate for the asynchronous clock rates, the S*n* bits do not carry information. At the demultiplexer end, the J*n* bits (Justification control bits) indicate to the demultiplexer whether the S*n* bits carry information. If the S*n* bit does not carry information, the E1 transmission clock will be gapped at the S*n* position. This process is known as destuffing. The jitter originated by this mechanism is stuffing jitter.

The LXT332 has been refined for operation in gapped clock jitter environments and meets G.742 jitter requirements. *

Figure 3: E2 Frame Structure



*Older LXT332 two-micron devices do not meet this specification. Please call your area Level One representative for more information about the availability of newer parts.

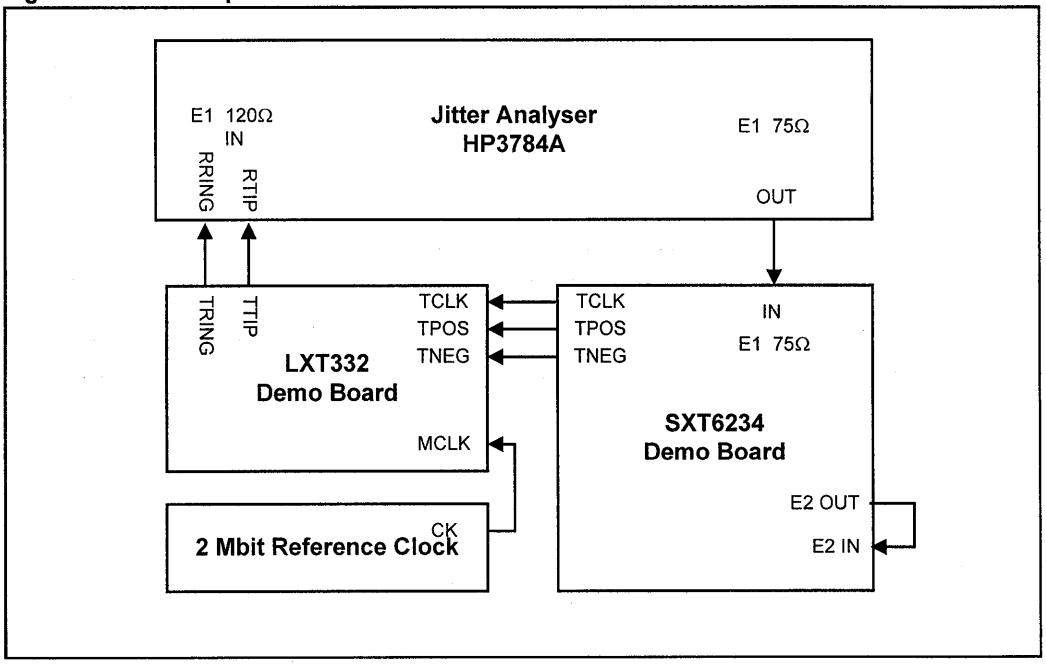
CONFORMANCE TESTING

Figure 4 illustrates the recommended configuration for G.742 conformance testing. The SXT6234 Evaluation Board is used in conjunction with the LXT332 Evaluation Board in order to perform the jitter measurements. The SDB6234 board is set to E1/E2 multiplexing (E1LLBA=ON). The E2 output is looped back to the E2 input, so that the incoming E1 data stream is multiplexed into an E2 signal and is demultiplexed back into E1 again. The SXT6234 board uses the LXT305A as the E1 line interface. The TCLK, TPOS and TNEG inputs to the LXT305A reproduce the effects of stuffing and destuffing that occurred within this multiplexing/demultiplexing process in the form of TCLK gaps. These three transmit signals are extracted from the SDB6234 board and delivered to the LXT332. The LXT332 demo board must be set with the jitter attenuator placed in the transmit direction and the equalizer control inputs set to 120 Ω E1 (LEN[2,1,0] = 001).

The conformance test will ensure that the output jitter of the LXT332 on the E1 transmit line is smaller than 0.25 UI in the frequency range up to 100 KHz. Configure the HP3784A jitter generator/analyzer to transmit a 75 Ω E1, HDB3 encoded, 2^{15} -1 pseudo-random pattern. The jitter analyzer on the HP3784A should be set to 120 Ω E1 and the jitter measurement filter to 100 KHz low pass (LP). For improved accuracy, the jitter measurements should be taken using the smaller measurement scale of 1 UI max. Provide an external free-running 2.048 MHz clock to be used as MCLK for the LXT332.

The stuffing jitter presented at TCLK is dependent on the E1 clock rate being fed to the SXT6234 demo board. Therefore, the LXT332 jitter attenuation performance should be tested with different E1 transmit clock rates coming from the HP3784 generator. Recommendation G.703 specifies that the E1 bit rate should be within ±50 ppm. The bit rate can be adjusted using the transmit clock offset feature on the HP3784A.

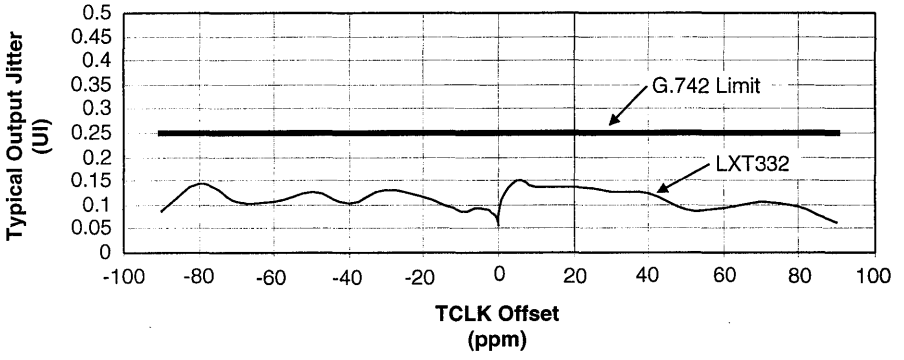
Figure 4: Test Setup for G.742 Conformance



TYPICAL PERFORMANCE OF THE LXT332

Figure 5 presents the typical LXT332 jitter performance measured in the frequency band up to 100 KHz using the procedure described above. Data was taken using transmission clock offsets over the ±90 ppm range. This extended range gives some margin to account for the MCLK allowable variation relative to the nominal 2.048 MHz frequency (±50 ppm).

Figure 5: Typical LXT332 Performance



NOTES

MARCH 1997
Revision 0.0

TBR12/13 Compliant Design Solutions for LXT360

Introduction

This application note shows how to design an E1 Line Interface which complies with Common Technical Regulations 12 and 13 (CTR12/13) jitter transfer requirements. The LXT304A is implemented as a standalone jitter attenuator in this design.

The European Telecommunications Standards Institute (ETSI) drafted two types of standards that define harmonized requirements. The first, for which compliance is voluntary, is the European Telecommunications Standard (ETS). The ETS completely describes all details of the specified interface or equipment. The Technical Basis for Regulation (TBR) requirements are combined with regulatory provisions to form a Common Technical Regulation, or CTR.

In Europe there are two categories of 2.048 Mbps leased line service: unstructured and structured. Unstructured service provides a usable bit rate of 2048 kbps with no network-provided timing or framing support. TBR-12 defines the necessary technical requirements for unstructured service.

Structured service provides a usable bit rate of 1984 kbps with network framing support. TBR-13 defines the technical requirements for structured leased line service.

Maximum Output Jitter Specifications

TBR-12 and TBR-13 include a common Output Jitter section (5.2.1.4). For terminal equipment, this section defines a maximum output jitter of 0.11 UIpp for frequencies from 20 Hz to 100 kHz when measured with a bandpass filter (40 Hz - 100 kHz). The input jitter is limited to 1.5 UIpp. The output jitter limit applies to equipment in configurations where output timing is derived locally as well as configurations where output timing is derived from one or more leased lines. These requirements also apply with a data rate offset of up to ±50 ppm from 2.048 MHz.

Design Considerations

Not all the equipment designed for the E1 market has to meet TBR12/13. The designer must check with the product specification to determine if such performance is needed. Many designs rely on external VCXO-based PLL circuits added to the transceiver to make the jitter performance TBR12/13 compliant.

This application note shows how to design a TBR-12/13 compliant E1 interface using LXT360 as the line interface and LXT304A as a jitter attenuator. The LXT304A is a cost effective, single chip jitter attenuator for TBR12/13 applications. It provides more than 50% cost savings, as well as board space savings, compared to VCXO based solutions. The LXT304A incorporates an on-chip crystal oscillator, using an external pullable quartz crystal. A specification for the crystal is provided in Table 1 on page 83. The LXT304A may be placed at the receive side between the LIU and Framer/ASIC to improve jitter transfer performance.

Figures 1 and 2 show a TBR12/13 compliant solution with the LXT360, using LXT304A as a jitter attenuator. The LXT360 is shown in Hardware Bipolar Mode with JA set in the receive path. The LXT360 can also be configured in Host Bipolar or Unipolar Mode. The TBR12/13 jitter requirements must be met in normal end-to-end operation and in remote loopback (RLOOP) operation. Most framers also support payload loopback. This loopback may be utilized in place of RLOOP. Figure 1 shows how to design for payload loopback using the LXT360 and a standalone jitter attenuator.

In cases where the framer does not support payload loopback, the solution shown in Figure 2 should be implemented. The 74HC157A Mux/Selector selects the transmit data either from the framer (normal operation) or from the receive path of the LIU (RLOOP mode), after it has passed the LXT304A jitter attenuator. Inverters U1 and U2 are needed to comply with the phase requirements between clock and data signals.

Refer to the LXT360 data sheet for detailed clock/data timing specifications. The U1 inverter may not be needed when the LXT360/61 is used in Host Mode. In Software Mode the LXT360/61 can use the rising or falling edge of RCLK to validate the RPOS/RNEG data. The inverter is

required when the data is valid on the rising edge of RCLK (this operation applies to Hardware Mode or Host Mode when register CR3.PCLKE=0).

Figure 3 on page 81 shows the appropriate pin configuration for the LXT304A transceiver when used as a jitter attenuator for TBR12/13 compliant designs. Notice that the device is hard-wired for Hardware Mode of operation, with LLOOP turned on. All I/O pins marked as "n/c" are irrelevant for this application and should be left unconnected on the PC board. Refer to the LXT304A data sheet for a full device specification.

For best performance, an 8.192 MHz crystal should be placed as close as possible to pins 9 and 10 of the LXT304A. Table 1 on page 83 shows specific crystal requirements.

According to TBR12/13, input jitter varies with frequency, while maximum output jitter is constant at 0.11 UIpp. Figure 4 on page 82 illustrates the TBR12/13 specification. Figure 5 shows the worst case combined jitter attenuation performance of LXT360 and LXT304A. This solution provides very good margins within TBR12/13 requirements.

Figure 1: TBR12/13 Compliant Design with LOC Standalone JA (with payload loopback)

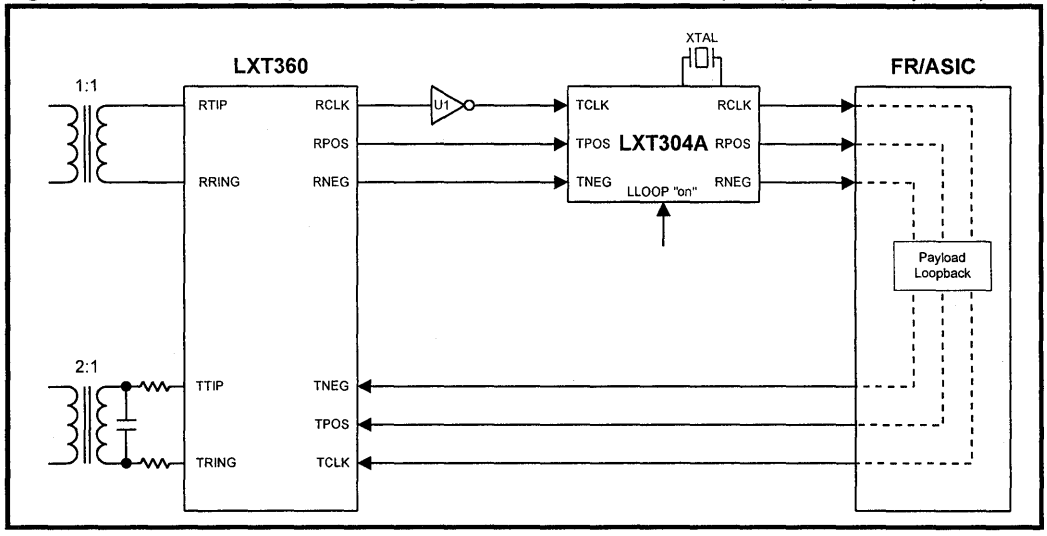


Figure 2: TBR12/13 Compliant Design with LOC Standalone JA (external loopback)

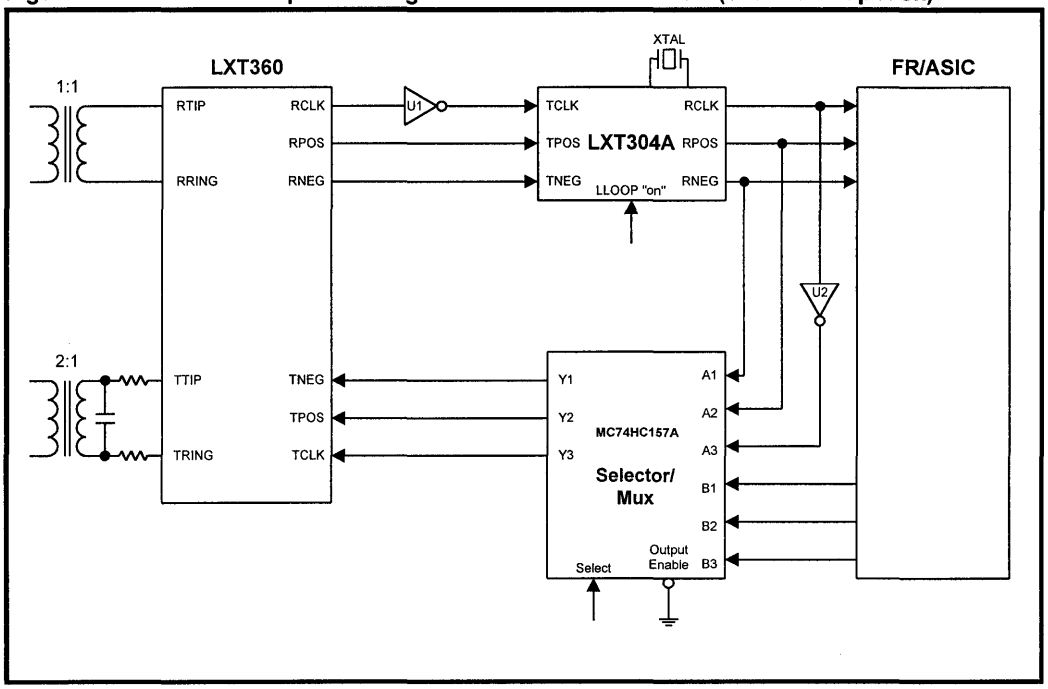


Figure 3: LXT304A Configuration as Standalone Jitter Attenuator

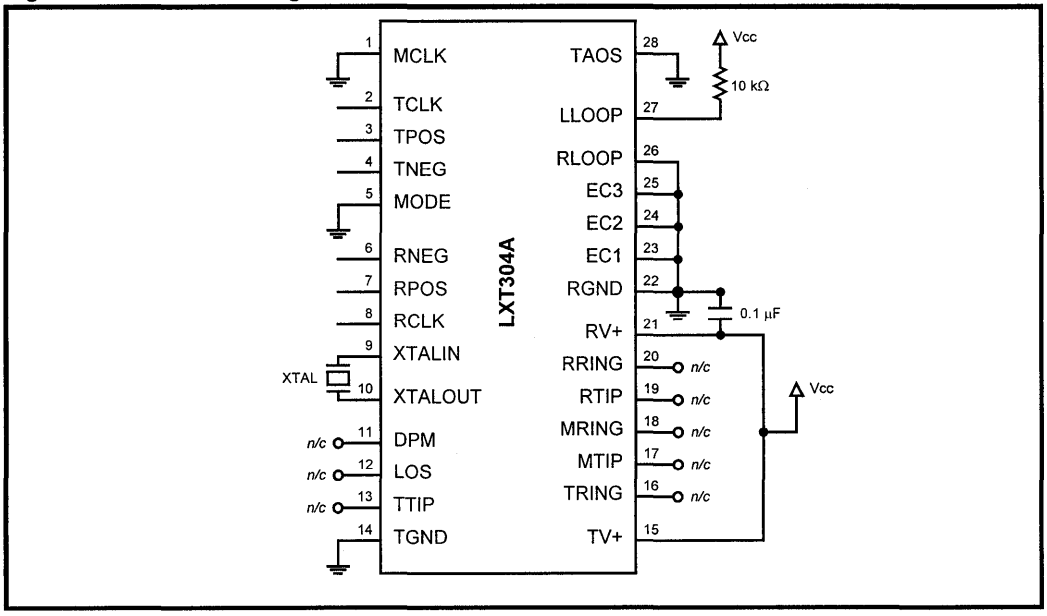


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Figure 4: Input and Maximum Output Jitter Specified by TBR12/13

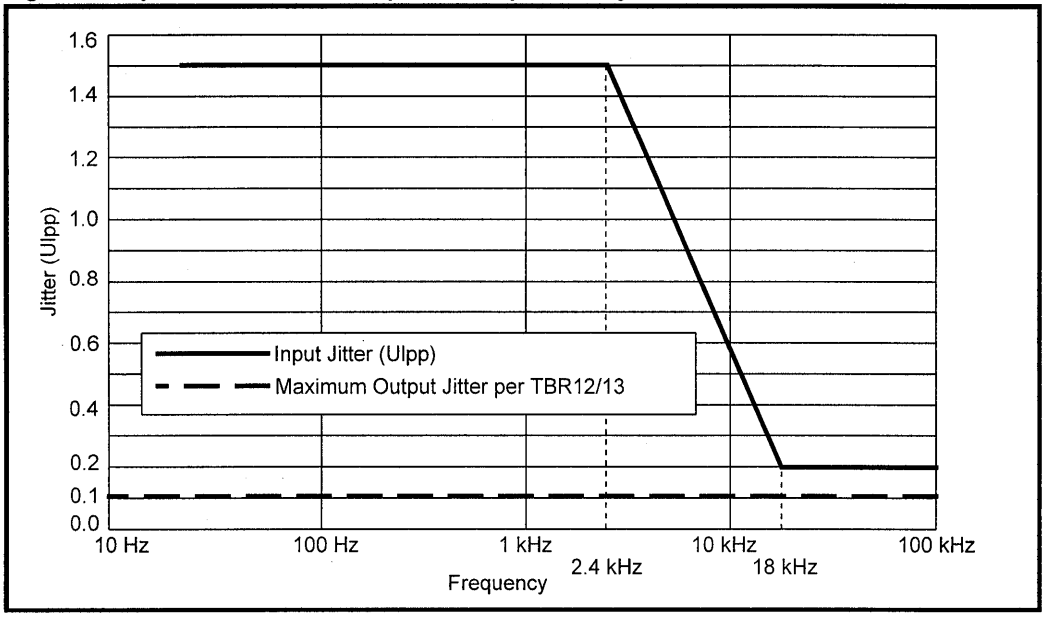

Figure 5: Combined Jitter Attenuation Performance (LXT304A and LXT360)

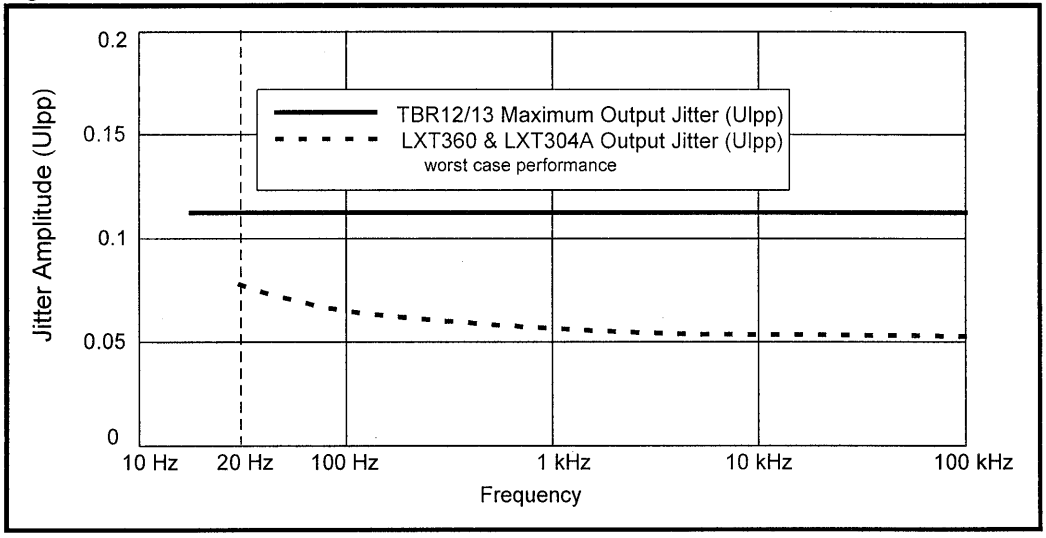

Table 1: LXT304A Crystal Specifications

Parameter	Specification
Frequency	8.192 MHz
Frequency Stability	±20 ppm @ 25 °C ±25 ppm @ -40 to +85 °C (ref 25 °C reading)
Pullability (Pull range may be slightly asymmetrical)	C_L = 19 pF to 37 pF, crystal should pull -95 ppm to -115 ppm from nominal frequency C_L = 19 pF to 11.6 pF, crystal should pull +95 ppm to +130 ppm from nominal frequency
Effective series resistance	30 Ω maximum
Crystal cut	AT
Resonance	Parallel
Drive level	2.0 mW maximum
Mode of operation	Fundamental
Crystal holder	HC49 (R3W), C_O = 7 pF maximum C_M = 17 fF typical
RECOMMENDATION: CXT8192 crystal manufactured by CTS Corporation, Tel: (815)786-8411	

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NOTES

SXT6234 E-Rate Multiplexer

For 16-E1/E3 Multiplexer/Demultiplexer

Introduction

The SXT6234 E-Rate Multiplexer offers a simple and economic approach to building E1/E2, E2/E3 and E1/E3 multiplexers and demultiplexers. This application note provides the system designer with a 16E1/E3 multiplexer/demultiplexer design example.

A brief overview of fundamental E1/E3 protocol is included to establish a common reference with readers. For additional information, refer to the ITU-T General Aspect of Digital Transmission Systems, Recommendations G.700-G.772. Related documentation includes the SXT6234 Data Sheet and the SDB6234 E1/E3 Demo Board User Guide.

E Standards

The International Telecommunication Union - Telecommunication Standardization Sector (ITU-T) standardized the E1, E2, and E3 specifications. The ITU-T was formerly known as the Consultive Committee for International Telephone and Telegraph (CCITT).

E Standard European Hierarchy

To accommodate higher transmission speeds, carriers developed the hierarchy levels shown in Table 1.

Table 1: E Standard Hierarchy

Level Number	System	Number of Voice Circuits	Bit rate Mbps
1	E1	30	2.048
2	E2	120	8.448
3	E3	480	34.368
4	E4	1920	139.264

E1 Standard

The E1 standard was designed to support transmission of thirty digitized voice channels. Analog-Digital conversion of each channel is based on the Nyquist sampling theory. This theory says that to digitize an analog signal so that it contains sufficient information to allow an accurate analog reconstruction, the signal must be sampled at a frequency that is at least twice the channel bandwidth. Sampling 8,000 per second is the industry-accepted rate. This rate allows the accurate reproduction of a voice-grade 4-kHz bandwidth channel.

The 8 kHz sampling produces a series of narrow pulses with a 125 microseconds (μsec) period. The magnitude or height of each analog sample is digitally encoded as an 8 bit binary value. Furthermore, the sampling pulse has a duration of less than 4 μsec during the 125 μsec period. Consequently, it is possible to interleave sampled pulses from other signals within the 125 μsec period. The E1 standard interleaves thirty-two channels; Thirty channels transmit digitized analog signals, and the remaining two channels send signaling and synchronization information. As shown in Table 2, each channel is assigned a specific time-slot.

Table 2: E1 Frame

Time slot	Type of information
0	Synchronization
1-15	Speech
16	Signaling
17-32	Speech

1. Frame length = 256 bits
2. Frame duration = 125 μsec
3. The 32 time slots constitute a frame. Each slot is 8 bits. Consequently one frame is:
4. 8 bits x 32 time slots = 256 bits/frame
5. Since 8000 frames are transmitted each second, the bit rate is: 256 bits /frame x 8000 frames/second = 2.048 Mbps.

E2 Standard

The second level is the E2 standard. The E2 standard multiplexes four E1 channels into a single 8.448 Mbps channel (4 X 2.048 Mbps = 8.448 Mbps). Two recommendations, defined in ITU-T G.742 and G.745, exist for this multiplexing. The G.742 for the SXT6234 is shown in Table 3. The G.742 uses positive justification and is intended for digital paths between countries.

Table 3: E2 Frame Bit Assignments

Bit Number	Bit Number by Set	Type of Information
1-10	1-10	Frame alignment
11	11	Alarm indication signal to the remote multiplex equipment
12	12	Bit reserved for national use
13-212	13-212	Bits from tributaries
213-216	1-4	Justification control bits Cj1
217-424	5-212	Bits from tributaries
425-428	1-4	Justification control bits Cj2
429-636	5-212	Bits from tributaries
637-640	1-4	Justification control bits Cj3
641-644	5-8	Bits from tributaries available for justification
645-848	9-212	Bits from tributaries available for negative justification

Table 4: E2 Frame

Standard	G 742
Bit rate	8.448 Kbits/s
Frame length	848 bits
Frame duration	100.39 µsec
Bits per tributaries	205 bits
Maximum justification rate per tributaries	10 Kbit/s

E3 Standard

The third level is the E3 standard. The nominal bit-rate of 34.368 Mbps is the result of the multiplexing of four 8.448 Mbps E2 channels.

Table 5: E3 Frame Bit Assignments

Bit Number	Bit Number by Set	Type of Information
1-10	1-10	Frame alignment
11	11	Alarm indication to remote digital multiplex equipment
12	12	Bit reserved for national use
13-384	13-384	Bits from tributaries
385-388	1-4	Justification service bits Cj1
389-768	5-384	Bits from tributaries
769-772	1-4	Justification service bits Cj2
773-1152	5 -384	Bits from tributaries
1153-1156	1-4	Justification service bits Cj3
1157-1160	5-8	Bits from tributaries available for justification
1161-1536	9-384	Bits from tributaries

Table 6: E2 Frame Bit Usage

# of bits	10	1	1	200	4	208	4	208	4	4	204
Usage	Frame	AIS	NAT	E1	Jus	E1	Jus	E1	Jus	Aux	E1

Table 7: E3 Frame Bit Usage

# of bits	10	1	1	372	4	380	4	380	4	4	376
Usage	Frame	AIS	NAT	E2	Jus	E2	Jus	E2	Jus	Aux	E2

Multiplexing Method

The multiplexing method uses cyclic bit interleaving in the tributary numbering order. This conforms with the positive justification recommendation of ITU-T G.742 and G.751.

Table 8: E3 Frame

Standard	G.751
Bit rate	34 368 kbit/s
Frame length	1536 bits
Frame duration	44.7 µsec
Bits per tributaries	378 bits
Maximum justification rate per tributary	22.375 kbit/s

Justification

Justification is the process of changing the data rate of a digital signal from its inherent rate to a different rate without loss of information. Positive justification is a method by which the data rate used to convey a signal has a higher bit-rate than the original signal. Positive justification is normally achieved by assigning some time-slots per frame to handle the additional information that may result from justification. If signal justification is unnecessary, these time-slots may contain regular channel information or they might remain empty. The justification service digits indicate if these time-slots contain information digits or justifying digits. The justification control signal in E standard is defined by the Cjn bits (see E2 and E3 frame tables). Three bits are used to show the type of justification; the fourth bit is the stuffing bit.

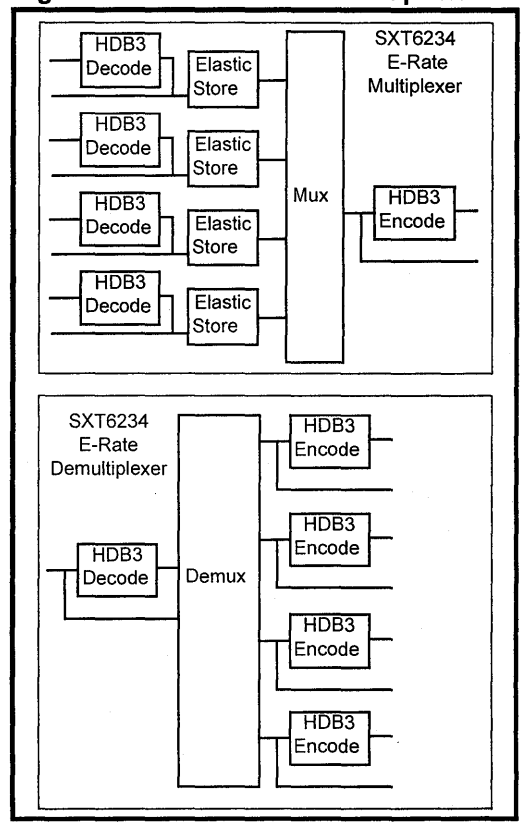
The E-Rate Multiplexer

The SXT6234 is a single-chip solution for multiplexing four tributaries into one high speed bit stream and the demultiplexing of the high speed bit stream back into four tributaries. All required circuitry has been integrated into the SXT6234; there is no need for an external framer.

The SXT6234, fabricated with 1.2-micron CMOS technology, is packaged in a 100-pin PQFP package. This device consists of the multiplexer block, the demultiplexer block, four HDB3 Encoder/Decoders for each tributary, and one HDB3 Encoder/Decoder for the high speed stream.

- The SXT6234 supports two multiplexing formats: One multiplexes four E1 channels into one E2 channel. The other format multiplexes four E2 channels into one E3 channel. Both are fully compliant with ITU-T recommendations, G.742 and G.751 respectively.
- All CODEC I/O pins are externally accessible, allowing either HDB3 or NRZ I/O to the multiplexer and demultiplexer. Alternatively, the SXT6234 can be used as a 5-channel HDB3 CODEC.
- Access is provided to the Alarm Indication Signal (AIS) and the National Bit.
- Four auxiliary low speed data or flag channels are available via the stuffing bits on each tributary channel.

Figure 1: SXT6234 E-Rate Multiplexer



E1/E3 Multiplexer Block Diagram

The block diagram of the E1/E3 Multiplexer is shown in Figure 2.

E1 LINE INTERFACE

- Receive clocks from the pulse data.
- Accepts either HDB3 encoded signals (clocks along with positive and negative RZ data), or NRZ data (clock and data). This depends on whether the Line Interface Unit (LIU) performs HDB3 coding.

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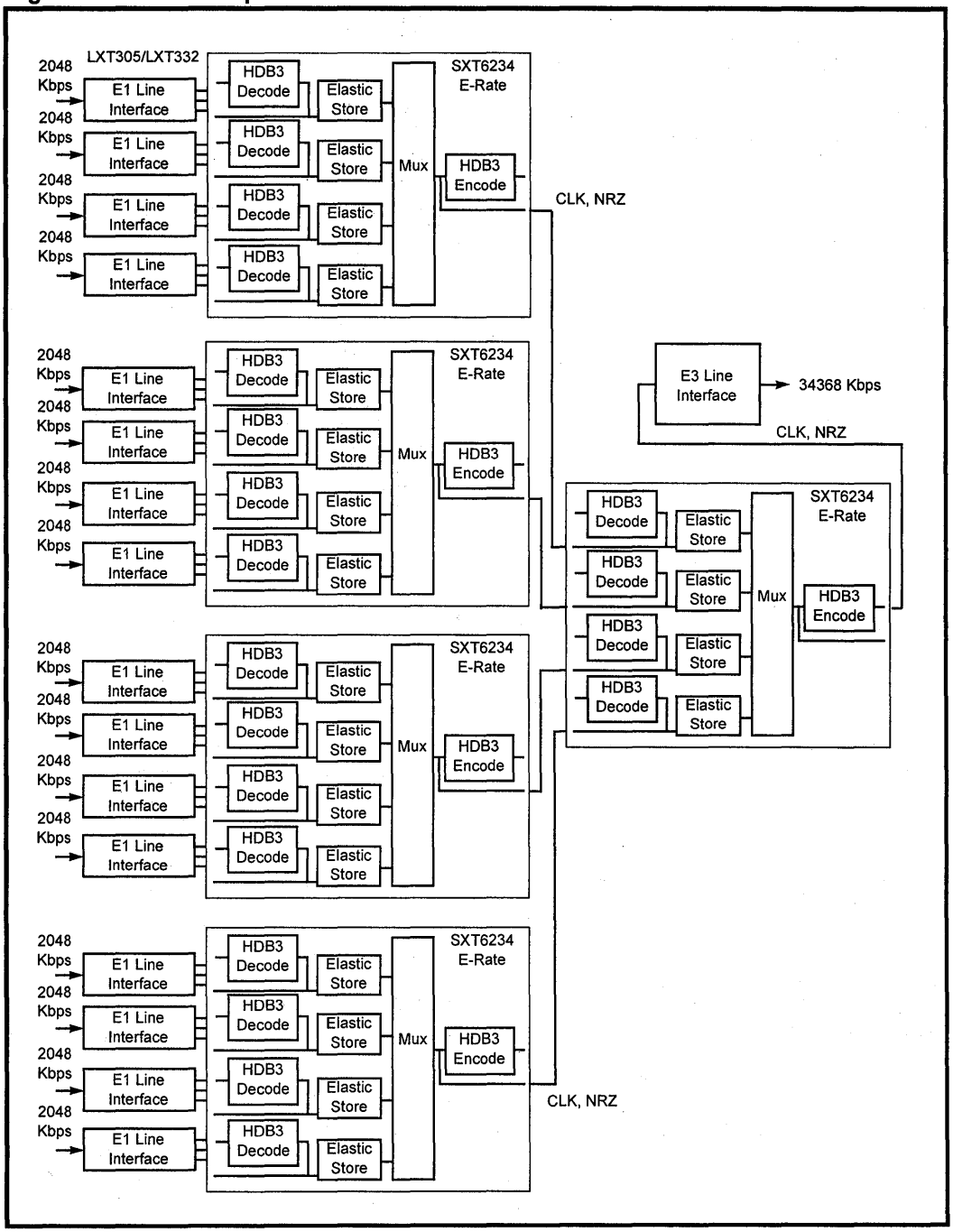
Figure 2: E1/E3 Multiplexer



SXT6234, E1/E2 STAGE

- If the tributary LIU does not perform HDB3 decoding, then the signals are routed to the SXT6234 onboard HDB3 decoder. The inputs are the clock and the decoder data input signals (both positive and negative). The onboard HDB3 decoder then outputs NRZ data and clock to the Elastic Store of the multiplexer portion of the SXT6234.
- If the LIU provides HDB3 decoding, then the NRZ data and clock are sent directly to the elastic store of the multiplexer portion of the SXT6234 via the external pin.
- Each four-tributary group is interleaved into a single, intermediary E2 data stream. An onboard crystal oscillator drives the data from the multiplexer at the E2 rate of 8.448 MHz. A bit stuffing algorithm implemented in the SXT6234 ensures tributary rate integrity at the output. The SXT6234 contains elastic store buffers to manage the bit-stuffing process.
- The NRZ data is sent to a tributary of the E-Rate Multiplexer, stage E2/E3.

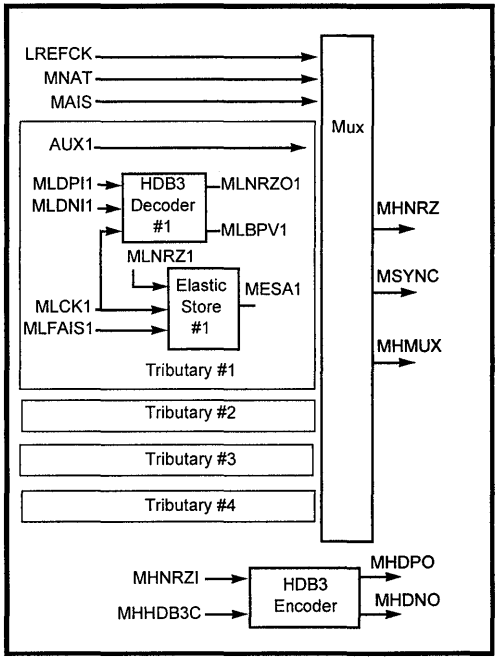
SXT6234, E3 STAGE

- If the tributary LIU does not provide HDB3 encoding, then encoding is performed in the SXT6234; positive and negative data output is provided. An activity monitor provides tributary fail notification when necessary.
- If the LIU provides HDB3 encoding, the NRZ data and clock are passed to the multiplexer input.
- The multiplexer portion of the SXT6234 interleaves the four asynchronous E2 rate NRZ data streams into a single E3 data stream. Depending on the user configuration, either an onboard crystal oscillator or an external reference clock drives the data output frequency from the multiplexer at the rate of 34.368 Mbps. The bit stuffing algorithm implemented in the SXT6234 ensures tributary rate integrity at the output.

E Multiplexer Block Diagram

The block diagram in Figure 3 shows the I/O used on the SXT6234 to accomplish the multiplexing function. Only I/O for tributary #1 has been referenced. I/O for tributaries #2, #3, and #4 are omitted for clarity, but they are the same as tributary #1.

Figure 3: SXT6234 Multiplexing Function



E1/E3 Demultiplexer Block Diagram

The block diagram of the E1/E3 demultiplexer is shown in Figure 4.

E3 LINE INTERFACE

- Receive clocks from the pulse data.
- If the LIU does not provide HDB3 decoding, then the LIU passes HDB3 encoded signals to the SXT6234. These signals consist of the clock and (positive and negative) RZ data.
- If the LIU does provide HDB3 decoding, then the LIU passes the NRZ data and clock to the SXT6234.

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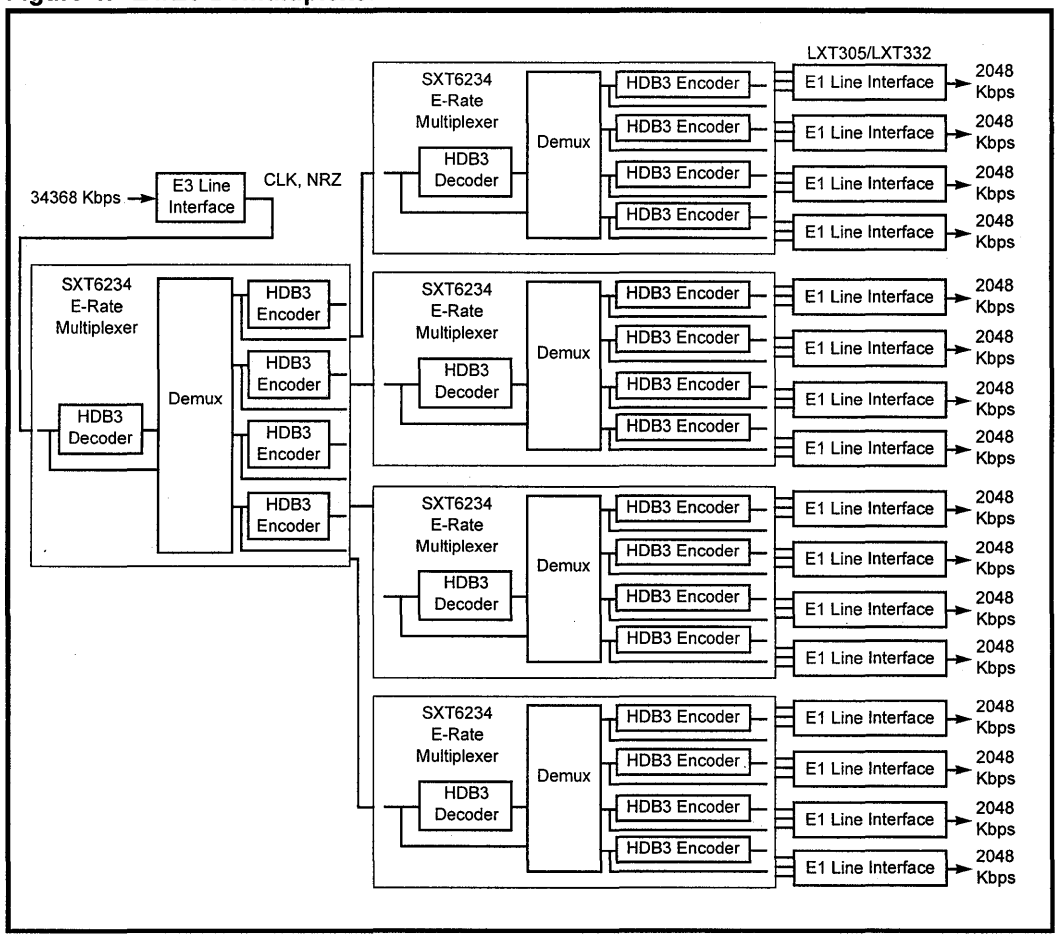
SXT6234, E3/E2 STAGE

- If the LIU does not do HDB3 decoding then the signals are routed to the SXT6234 onboard HDB3 decoder. The inputs are the clock and the decoder data input signals (both positive and negative). The onboard HDB3 decoder then outputs NRZ data and clock to the Elastic Store of the multiplexer portion of the SXT6234.
- If the LIU provides HDB3 decoding, NRZ data and clock are received by the demultiplexer portion of the SXT6234.
- The Four E2 rate data streams are recovered from the E3 NRZ data and are sent from the SXT6234 as four tributaries.

SXT6234, E2/E1 STAGE

- The demultiplexer portion of the SXT6234 recovers four E1 data streams from the E2 intermediary stream.
- If the LIU does not provide HDB3 encoding, the streams are HDB3 encoded and sent out as positive and negative voltages to the E1 line interface. (LXT305 or LXT332)
- If the LIU provides HDB3 encoding the stream is sent out as NRZ data to the E1 line interface.

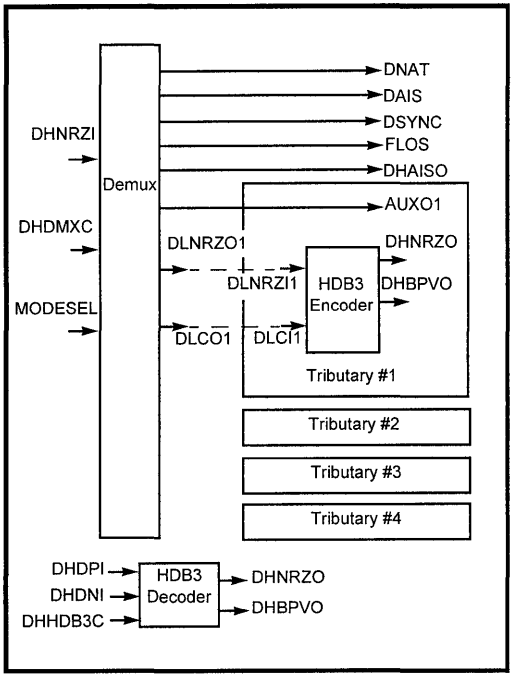
Figure 4: E1/E3 Demultiplexer



E Demultiplexer Block Diagram

Figure 5 shows the I/O used on the SXT6234 to perform the demultiplexing function. Only I/O for tributary #1 has been referenced. I/O for tributaries #2, #3, and #4 are omitted for clarity, but they are the same as tributary #1.

Figure 5: SXT6234 Demultiplexing Function



Alarms

The multiplexer and demultiplexer sides contain the following alarm provisions:

- Input Loss Alarms at all receive line interfaces.
- Output Fail Alarms at all transmit line interfaces.
- Frame Loss Alarm line.

With ME for multiplexer and DE for demultiplexer:
i = 1 to 16 for E1
j = 1 to 4 for E2

Alarm equations are:

ME1FAISi = MELOSi
DE1FAISi = DE2AISDj + DE2FLOSj + DE3LOS + DE3FLOS + DE3AISD
ME2FAISj = ME2LOSj

DE2FAISj = DE3LOS + DE3FLOS + DE3AISD
ME3AIS = DE3LOS + (DE3FLOS&~DE3LOS) + DEAISD

Auxiliary Channels

Within the E2 and E3 standards, there are four extra bits used for justification (bits 641-644 in the E2 frame, and bits 1157-1160 in the E3 frame). These bits may be used as four auxiliary channels that would provide an E2 rate of 10 KHz, or an E3 rate of 22 KHz.

Two examples how these may be used are:

- Voice Channel Maintenance.
- Data Counter implemented with a parity circuit that would count data bits during one frame of the incoming stream.

National and AIS Bits

The bits are accessible for compliance with the ITU-T recommendation. However, these two bits can also be used as auxiliary channel at the rate of 10 KHz for E2 or 22 KHz E3.

Microcontroller

E1/E3 multiplexer design can be improved by using a microcontroller to control the alarms and other settings. An 8 bit microcontroller, such as an Intel 87C51 is sufficient. The microcontroller could monitor alarms, provide an alarm history, update a control panel and even sound an audible alert if necessary. This microcontroller could monitor switches for loop-back instructions, test and update the National Bit, and check the configuration jumpers for E1/E2 or E2/E3 functions.

Table 9: Multiplexer Pin Description

Mux Input	
LFRECK	Reference clock for tributary data is used as reference for the AIS functions.
MNAT	National Bit Input.
MAIS	AIS bit input.
MHMUXC	High speed multiplexer clock input.
Tributary #1 Input	
AUX1	Auxiliary data input #1. The signal on this pin is clocked into the frame at the stuffing bit location (J1) when justification is such that tributary data is not placed at this location. A high on alarm signal MESA1 indicates this condition during the current frame.
MLDPI1	Positive data input. Clocked on the positive transition of the clock MCKL1.
MLDNI1	Negative data input. Clocked on the positive transition of the clock MCKL1.
MCKL1	Clock input for tributary channel 1.
MLFAIS1	Force AIS on tributary 1. Active high signal forces AIS (all 1) data and LREFCK clock.
Tributary #1 Output	
MLNRZO1	HDB3 decoder #1 NRZ output clocked on the rising edge of MCKL1.
MLNRZ1	Multiplexer tributary NRZ input clocked on the falling edge of the clock signal MLCK1.
MLBPV1	HDB3 decoder #1 bipolar violation alarm. This open collector output pulses when a bipolar violation occurs in the decoding process.
MESA1	Multiplexer justification status for tributary #1. A high indicates bit stuffing on the current frame. A low indicates an information bit. When externally filtered, this can be used to indicate elastic store failure or incorrect tributary frequency.
Mux Output	
MHRZO	Multiplexer NRZ output data is clocked out on the rising edge of MHMUXC.
MSYNC	Multiplexer frame synchronization pulse is one high speed clock cycle synchronous with the last bit of the frame.
HDB3 Decoder	
MHNRZI	HDB3 encoder #5 NRZ input clocked on the rising edge of MHHDB3C.
MHHDB3C	HDB3 encoder #5 clock input. When used in conjunction with the multiplexer, this pin should be tied to the multiplexer clock (MHMUXC).
MHDPO	HDB3 encoder #5 positive data output. Positive rail clocked out on the rising edge of MHHDB3C.
MHDNO	HDB3 encoder #5 negative data output. Negative rail clocked out on the rising edge of MHHDB3C.

Table 10:Demultiplexer Pin Description

Demultiplexer Input	
DHNRZI	NRZ input clocked on the rising edge of DHDMXC.
DHDMXC	Clock input.
MODESEL	Mode selection for multiplexer / demultiplexer operation. A low selects 4E1/E2 multiplexing. A high selects 4E2/E3 multiplexing.
HDB3 Decoder	
DHDPI	HDB3 decoder #5 positive rail input clocked on the rising edge of DHHDB3C.
DHDNI	HDB3 decoder #5 negative rail input clocked on the rising edge of DHHB3C.
DHHDB3C	Clock input for HDB3 decoder # 5. When used in conjunction with the demultiplexer this pin should be tied to the demultiplexer clock DHMUXC.
DHNRZO	HDB3 decoder #5 NRZ data clocked out on the rising edge of DHHDB3C.
DHBPVO	HDB3 decoder #5 bipolar violation alarm. This active high signal pulses when a bipolar violation occurs in the decoding process.
HDB3 Encoder	
DLNZO1	Tributary #1 NRZ output. This signal is clocked out on the rising edge of DHDMXC and transitions are coincident with the falling edge of DLCO1.
DLCO1	Demultiplexer side recovered clock of tributary #1. This clock has a duty cycle of 75% and is gapped at points in the frame where tributary data is not present. The maximum gap is 3 clocks at the frame word will match that of the far end multiplexer tributary input. This signal is clocked out on the rising edge of DHDMXC.
DLNRZI1	HDB3 encoder #1 NRZ input clocked on the rising edge of DLCI1.
DLCI1	Clock input for HDB3 encoder #1.
Multiplexer Output	
DNAT	National Bit output.
DAIS	AIS bit output.
DSYNC	Pulse of one high speed clock cycle synchronous with the last bit of the frame.
FLOS	Loss of frame alarm. Active high frame loss alarm that occurs when the demux has not detected the frame word.
DHAIS	Input AIS detect. Active high alarm occur when an all 1's condition (AIS) is detected at the DHNRZI input. This alarm does not trip if the input is a frame signal (i.e., all tributaries are AIS on the multiplexer side).
Auxiliary #1 Output	
AUXO1	Auxiliary flag data #1 output that contains data value input on AUX1.
DLDPO1	HDB3 encoder #1 positive rail output clocked out on the rising edge of DLCI1.
DLDNO1	HDB3 encoder #1 negative output clocked out on the rising edge of DLCI1.

NOTES

SXT6234 E-Rate Multiplexer

For Multiplexing/Demultiplexing any 4 data channels

Introduction

The SXT6234 E-Rate Multiplexer offers a simple and economic approach to building E1/E2, E2/E3 and E1/E3 multiplexers and demultiplexers compliant with the International Telecommunication Union - Telecommunication Standardization Sector (ITU-T). See Application Note 9501. However by changing the high speed reference clock the SXT6234 could be used in non-standard application to multiplex/demultiplex any four digital channels provided they all have the same data speed. The data speed could range from 256 kbps to 9 Mbps and give an output four time faster ranging from 1 Mbps to 36 Mbps.

This application note provides the system designer with a design example on how to multiplex and demultiplex four data channels with an input speed referred herein as F_{trib}.

The SXT6234 utilizes the E frames structure to transport data. Therefore two tables for E2 and E3 frames are included to establish a common reference with readers. Related documentation includes the SXT6234 data sheet and Application Note AN 9501 .

Multiplexing Method

The multiplexing method uses cyclic bit interleaving in the tributary numbering order. This conforms with the positive justification recommendation of ITU-T G.742 and G.751.

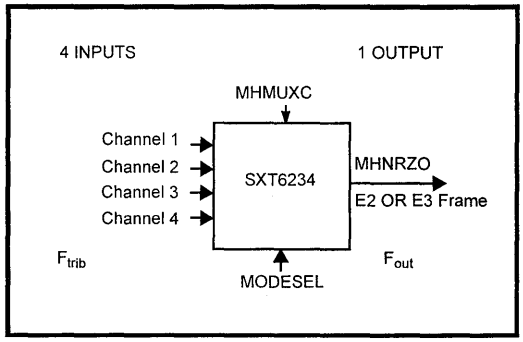


Table 1: E2 Frame Bit Usage

# of Bits	10	1	1	200	4	208	4	208	4	4	204
Usage	Frame	AIS	NAT	Data (Table 3)	Cj	Data (Table 3)	Cj	Data (Table 3)	Cj	Ji	Data (Table 3)

Table 2: E3 Frame Bit Usage

# of Bits	10	1	1	372	4	380	4	380	4	4	376
Usage	Frame	AIS	NAT	Data (Table 3)	Cj	Data (Table 3)	Cj	Data (Table 3)	Cj	Ji	Data (Table 3)

Table 3: Data: interleaved bit channels

# of Bits	1	1	1	1	1	1	1	1
Usage	Channel 1 bit 1	Channel 2 bit 1	Channel 3 bit 1	Channel 4 bit 1	Channel 1 bit 2	Channel 2 bit 2	Channel 3 bit 2	Channel 4 bit 2

MULTIPLEXING 4 CHANNELS

Mode selection

The SXT6234 supports two modes: E12 or E23. The pin to select the mode is MODESEL. Modesel is low for E12 mode. Modesel is high for E23 mode. See E12 and E23 mode choice paragraph for more information

Clock

MCKLx (x=1 to 4) is the clock input for tributary channel #x. MHMUXC is the multiplexer high speed clock input and defines the NRZ high speed output data rate.

Clock Rate

The data rate of all the tributaries is defined as F_{trib}
MHMUXC =(8,448/2,048) * F_{trib} in E12 mode or (34,368/ 8,448) * F_{trib} in E23 mode. The value of F_{trib} could be from 256 Kbits/s to 9 Mbps
MCKLx = F_{trib}

Data rate tolerance

By using the stuffing bits, the data rate between the 4 channels F_{trib} could be slightly different. The tolerance is +/- 50 ppm in E12 Mode and +/- 30 ppm in E23 Mode.

Data

MLNRZ1: is the data input for tributary one. The data are NRZ coded and do not need to go throught the HDB3 decoder. This data could be any NRZ data stream and do not need to conform to a E1 or E2 frame format.

Output Stream

The output will be NRZ data conforming to either the E2 or E3 frame format. The E2 frame (see table 3) contains 205 bits of tributary channel #x over 848 bits. The E3 frame (see table 4) contains 378 bits of tributary channel # x one over 1,536 bit. Bits from the tributaries will be interleaved in tributaries order 1,2,3,4.

DEMULTIPLEXING

Use the same clock speed as MHMUXC on DHDMXC. The SXT6234 can demux the output stream and data output from the tributary channel #1 are available on DLNZ01. Remark: it is best to mux and demux with the SXT6234 on both sides. The SXT6234 expects a E2 or a E3 frame at the demux input and won't work with any type of data stream at the demux input.

E12 AND E13 MODE CHOICE

The main differences between the two modes in a non-standard environment are minimal:

- frame length
  E12: 848 bits
  E13: 1536 bits

- total overhead
  E12 28/848 = 3.5%
  E23 28/1536 = 1.8%

-overhead channel data rate
  E12 = F_{out}/ 848
  E13 = F_{out}/ 1536

JUSTIFICATION: CJ BITS

Justification is the process of changing the data rate of a digital signal from its inherent rate to a different rate without loss of information. Positive justification is a method by which the data rate used to convey a signal which has a higher bit-rate capacity than the original signal. Positive justification is normally achieved by assigning time-slots per frame to handle the additional information that may result from justification. If signal justification is unnecessary, these time-slots may contain regular channel information or they might remain empty. The justification service digits indicate if these time-slots contain information digits or justifying digits. The justification control signal in E standard is defined by the Cj bits (see E2 and E3 frame tables). Three bits are used to show the type of justification a majority decision used to recover the justification.

JUSTIFICATION: JI BITS

Within the E2 and E3 standards, there are four extra bits used for justification (bits 641-644 in the E2 frame, and bits 1157-1160 in the E3 frame). If not used for justification, these bits may be used as four auxiliary channels with an approximate speed of 0.4*F_{out} /848 kHz for E2 mode or 0.4 *F_{out} /1536 kHz for E3 mode

- Voice Channel Maintenance.
- Data Counter implemented with a parity circuit that would count data bits during one frame of the incoming stream.

NATIONAL AND AIS BITS

The bits are accessible for compliance with the ITU-T recommendation. However, these two bits can also be used as auxiliary channel at the rate of F_{out} /848 kHz for E2 mode or F_{out} /1536 kHz for E3 mode

MICROCONTROLLER

E1/E3 multiplexer design can be improved by using a microcontroller to control the alarms and other settings. An 8 bit microcontroller, such as an Intel 87C51 is sufficient. The microcontroller could monitor alarms, provide an alarm history, update a control panel and even sound an audible alert if necessary. This microcontroller could monitor switches for loop-back instructions, test and update the National Bit, and check the configuration jumpers for E1/E2 or E2/E3 functions.

APPLICATION EXAMPLES

T-Rate multiplexer

Multiplexing 4 T1 (F_{trib} = 1,544 bits/s) or multiplexing 4 T2 (F_{trib} = 6,176 bits/s)

Warning the output of the multiplexer is not a T2 or T3 frame. The T1 or T2 bits are multiplexed in the E2 or E3 frame. This a non-standard compliant application for propriatory systems.

For multiplexing 4 T1:X= 1,544

- $MHMUXC_{E12}$ = 6,369 kHz
  - AIS = 7.54 kHz
  - NAT = 7.54 kHz
- $MHMUXC_{E23}$= 6,281 kHz
  - AIS = 4 kHz
  - NAT = 4 kHz

MPEG multiplexer

Broadcast quality video television signals, encoded MPEG 1 or 2, have bit rates ranging from 1.5 Mbps to 9 Mbps. The SXT6234 could be used to mulitplex four MPEG encoded video signals into one high-speed signal for transmission.

DSL multiplexer

With rate ranging from 384 Kbps to 6 Mbps at the end user location, the SXT6234 could be use to design a multiplexer at the distribution point. Twenty SXT6234 could be used to multiplex 64 DSL channels at 384 Kbps.

Double rate E1/T1 single board multiplexer

In the case of a point to point and point to multipoint application, it is possible to design one single board which will do either 4E1 or 4T1 operation by adjusting the clock speed. Same thing for 8E1 or 8T1.

9

NOTES

Transformer Specifications

for Level One Transceiver Applications

Transformer Specifications

Txcvr Part Number	Frequency (kHz)	Turns Ratio (±2%)	Primary Inductance (µH - Min)	Leakage Inductance (µH - Max)	Interwinding Capacitance (pF - Max)	Primary Resistance (Ω - Max)	Dielectric Breakdown (Vrms - Min)
LXT300Z LXT301Z Rx & Tx	1544/2048	1:2 CT	600 Pri	0.75 Pri	50	1.0 Pri 1.0 Sec	500
LXT304A LXT305A LXT307 Rx	1544/2048	1:2 CT	600 Pri	0.75 Pri	50	1.0 Pri	500
LXT304A LXT305A Tx	1544/2048	1:1.15 1:2 CT 1:1 1:1.126	600 Pri	0.75 Pri	50	1.0 Pri 1.0 Sec	500
LXT331 LXT332 Tx & Rx	1544/2048	1:2 CT 1:1.15 1:2.3	1200 Pri	0.5 Pri	25	1.0 Pri	1000
LXT334 LXT335 Tx & Rx	1544/2048	1:2 1:1.36 1:1.26	1200 Pri	0.4 Pri	30	1.0 Pri	1000
LXT310 LXT318 LXT350/351 LXT360/361 Rx	1544/2048	1:1 CT	600 Pri	0.75 Pri	50	1.0 Pri 1.0 Sec	1500
LXT310 LXT318 LXT350/351 LXT360/361 Tx	1544/2048	1:2 CT	600 Pri	0.75 Pri	50	1.0 Pri 1.0 Sec	1500
LXT325 Rx only	1544/2048	1:2:2	600 Pri	0.75 Pri	50	1.0 Pri 1.0 Sec	500
LXT312/15 LXT313/16 Rx	1544/2048	1:1 CT	1000 Pri	1.0 Pri	25	1.0 Pri 1.0 Sec	1000
LXT312/15 LXT313/16 Tx	1544/2048	1:1 CT :3 CT	1000 Pri	1.0 Pri	25	1.0 Pri 1.0 Sec	1000
LXT400 LXT441 Rx & Tx	1544/2048	1:1	700 Pri	22-43 Pri	350	1.0 Pri 1.0 Sec (± 1 Ω)	1000

Transformer Specifications for Level One Transceiver Applications

Table 4: Transformer Manufacturers

Transceiver	Application	Part Number	Manufacturer
LXT300Z/301Z	Tx	PE-64931, PE-64951	Pulse
LXT304A/305A		67112060, 67115100	Schott Corporation
		0553-5006-IC	Bell Fuse
		671-5832	Midcom
		6500-07-011	Nova Magnetics
		FE 8006-55, 8006-85	Fil-Mag
		16Z5946	Vitec
LXT310	Tx	0553-5006-IC	Bell Fuse
LXT318	(1:2)	66Z1308	Fil-Mag
LXT350/351		671-5832	Midcom
LXT360/361		65351, 65771	Pulse
		67127370, 67120850	Schott Corporation
		TD61-1205D, TG27-1205N1 (combination Tx/Rx)	HALO Electronics
		16Z5946	Vitec
LXT310	Rx	FE 8006-155	Fil-Mag
LXT318	(1:1)	671-5792	Midcom
LXT350/351		64936, 65778	Pulse
LXT360/361		67130840, 67109510	Schott Corporation
		TD61-1205D, TG27-1205N1 (combination Tx/Rx)	HALO Electronics
		16Z5934	Vitec
LXT312/315	Tx	12535	Schott Corporation
		FE 8006-175	Fil-Mag
LXT312/315	Rx	10951	Schott Corporation
		FE 8006-155	Fil-Mag
LXT332	Tx Rx	PE-65351, PE-68841	Pulse
	(1:2) (1:2 CT)	16Z5946	Vitec
		TG29-1205NX	HALO Electronics
		ST5174T	Valor
	(1:2 CT) (1:2 CT)	ST5086	Valor
		T1006, PE68841	Pulse
		TD15-1205A	HALO Electronics
	(1CT:2CT) (1CT:2CT)	ST5028	Valor
		PE65761	Pulse
	(1:2.3)	T1017	Pulse

Table 4: Transformer Manufacturers – continued

Transceiver	Application	Part Number	Manufacturer
LXT331	Rx	671-7816	Midcom
	(1:1)	ST5085	Valor
		PE65764	Pulse
LXT334	Tx	671-6599, 671-7815	Midcom
LXT335	(1:1.26, 1:1.36, 1:2)	ST5170T, ST5078, ST5143, ST5174T	Valor
		T1010	Pulse
LXT334	Rx	ST5085	Valor
LXT335	(1:1)		

NOTES

Quartz Crystals

for Level One T1/E1 Transceivers

General Information

The Level One LXT300Z, LXT304A, LXT305A, LXT310 and LXT318 transceivers require quartz crystals as companion devices. For the convenience of our customers, Level One buys crystals in volume from a qualified vendor stocks them and resells them at reasonable prices, in conjunction with Level One transceivers.

The LXC6176 is used in T1 applications, and the LXC8192 is used in E1 applications. Specifications for the LXC6176 and LXC8192 crystals are listed below.

Level One has evaluated and qualified several vendors for the benefit and convenience of our customers. We believe customers prefer to have multiple approved sources. Quartz crystals qualified for use with Level One transceivers are listed on the next page. We suggest that customers establish relations with one or more of these approved crystal suppliers and buy direct.

Crystal Specifications

Parameter	T1 Applications	E1 Applications
Frequency	6.176 MHz	8.192 MHz
Frequency stability	±20 ppm @ 25 °C ±25 ppm from -40 °C to 85 °C (Ref 25 °C reading)	±20 ppm @ 25 °C ±25 ppm from -40 °C to 85 °C (Ref 25 °C reading)
Pullability	C_L = 11 pF – 18.7 pF, +ΔF = 175–195 ppm C_L = 18.7 pF – 34 pF, -ΔF = 17–195 ppm	C_L = 19 pF – 11.6 pF, +ΔF = 95–130 ppm C_L = 18.7 pF – 37 pF, -ΔF = 95–115 ppm
Effective series resistance	40 Ω maximum	30 Ω maximum
Crystal cut	AT	AT
Resonance	Parallel	Parallel
Maximum drive level	2.0 mW	2.0 mW
Mode of operation	Fundamental	Fundamental
Crystal holder	HC49 (R3W), C_O = 7 pF maximum C_M = 17 fF typical	HC49 (R3W), C_O = 7 pF maximum C_M = 17 fF typical

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Table 5: Qualified Quartz Crystals

Manufacturer	Part Number	Frequency
M-Tron	MP-1 3808-010, MP-1 4144-002	6.176 MHz
Monitor Products	MSC-1311-01B-6.176	6.176 MHz
Monitor Products	MSC-1311-01B-8.192	8.192 MHz
CTS Knights	6176-180	6.176 MHz
CTS Knights[1]	8192-100	8.192 MHz
Valpey Fisher	VF49A16FN1-6.176	6.176 MHz
Valpey Fisher	VF49A16FN1-8.192	8.192 MHz
US Crystal	U18-18-6176SP	6.176 MHz
US Crystal	U18-18-8192SP	8.192 MHz

1. CTS Knights #8192-100 offers superior jitter attenuation to meet the CTR-12/13 jitter requirements for E1 applications.

Telecom Product Evaluation Boards

For information regarding pricing and availability of Telecom Product Evaluation Boards, please contact your local Level One sales representative.

LDB300

Evaluation Board for T1/E1 Transceivers

General Description

The LDB300 Evaluation Board is a versatile evaluation tool for Level One Communications short-haul and long-haul T1/E1 transceivers. The Evaluation Board works with any of the following:

Short-Haul Transceivers	Long-Haul Transceivers
LXT300Z/LXT301Z	LXT310(T1)
LXT304A/LXT305A	LXT318(E1)

This data sheet describes using the Evaluation Board with the LXT300 transceiver in both T1 (North American) and E1 (European) environments. We have also included information to set it up with the other short-haul transceivers.

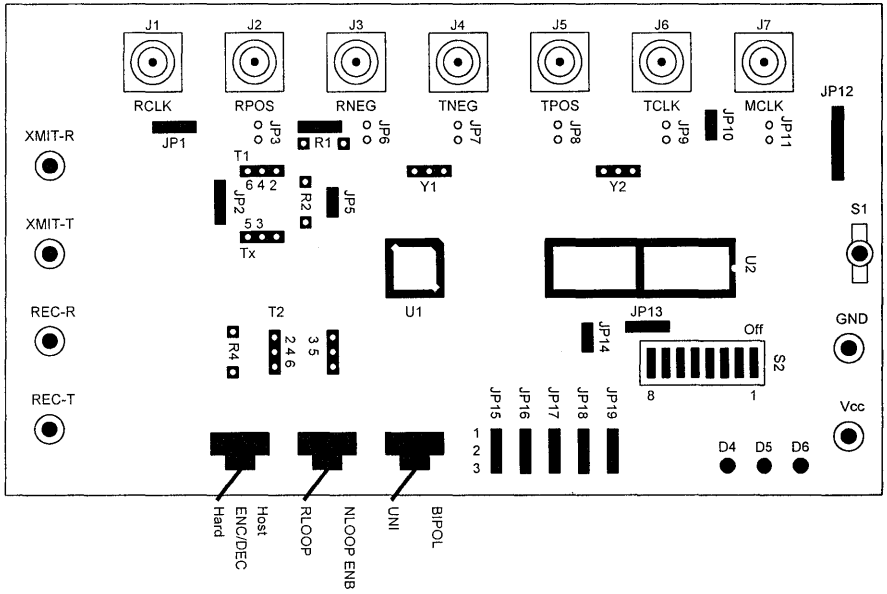
A later section has similar information describing applications in a long-haul environment using both the LXT310 and LXT318 transceivers.

To use this document, have the current data sheet for the chosen transceiver to insure having the correct information available.

Features

- Board design permits fast set-up, ease of use and clear visibility of application settings
- On board sockets accept either 6.176 or 8.192 MHz crystal for jitter attenuation
- Flexible design for numerous termination schemes
- On-board switches for Hardware Mode operation
- Ribbon-cable, serial-interface connector for Host Mode operation
- Banana jacks for quick TP and power connections
- BNC connectors allow tracing signals with oscilloscope
- LEDs indicate LOS, BPV and DPM conditions
- Design supports either short- or long-haul transceiver
- On-board sockets for both DIP and PLCC package

LDB300 Evaluation Board



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LDB332

Evaluation Board for T1/E1 Applications

General Description

The LDB332 Evaluation Board is a versatile evaluation tool for engineers involved in designing T1/E1 short-haul applications. It uses an LXT332 Dual Line Interface Unit (DLIU) and incorporates all supporting circuitry for either T1 or E1 applications using the DLIU.

The Evaluation Board provides banana jacks for the line interface and BNC connectors for the framer interface. A bit error rate tester (bert) or framer/mux may be used to provide the external signal needed for evaluation.

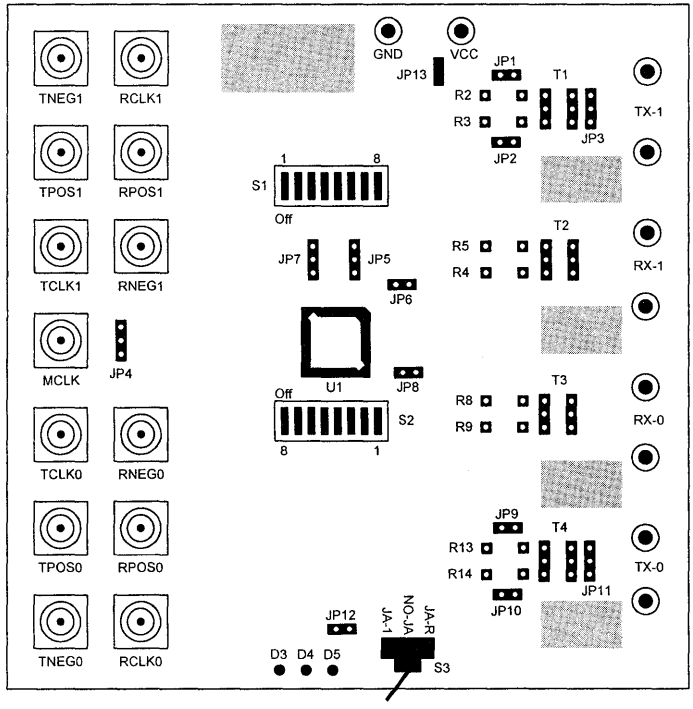
This document describes typical Evaluation Board setup procedures for both T1 (North American) and E1 (International) environments.

Before using the Evaluation Board, review the current LXT332 DLIU data sheet for complete information about this transceiver. An Evaluation Board schematic is also available.

Features

- Board design permits quick setup, ease of use and clear visibility of application settings
  - Local DLIU testing
  - Complete system evaluation
  - Individual circuit isolation
- Exploits crystal-less jitter attenuation of DLIU
- Jitter attenuation switchable into either transmit or receive data path
- Two twisted-pair line interfaces and all related digital signals available for analysis and testing
- Banana jacks for twisted-pair line interface
- BNC connectors for clock and framer interface
- LEDs indicators for DFM and LOS
- Design supports both E1 and T1 evaluation
- Switches emulate stand-alone Hardware Mode

LDB300 Evaluation Board



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LXD334

JUNE 1997
Revision 0.0

Evaluation Board for Quad E1 Applications

General Description

The LDB334 Evaluation Board is a versatile tool for engineers designing E1 short haul applications. To evaluate the LXT334 Quad E1 Transceiver (64-pin QFP), the specific evaluation board part number is LXD334-64.

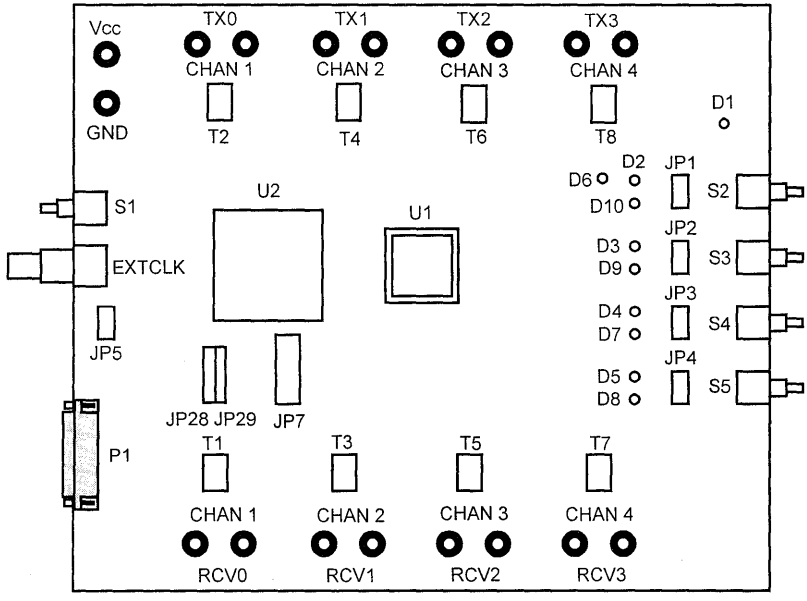
This board is designed to operate in two modes: Software Control Mode and Hardware Mode. In Software Control Mode, most device and individual channel control signals are controlled through a PC based configuration and monitoring program. In Hardware Mode, the device and channel controls are set using shorting blocks and toggle switches.

On-board LED indicators identify test conditions and transmission errors in both modes. The board provides banana jacks for power and for line interfaces. 10-pin connectors are provided for each framer interface. Either a framer/mux or a bit error rate tester (BERT) may provide the external signals for evaluation. Toggle switches control settings for bipolar or unipolar operation, and selection of on-board MCLK frequency. A 50 Ω terminated BNC connector provides the option to use an externally generated MCLK.

Features

- Banana jacks for power and line interfaces
- 10-pin connectors for clock and framer interfaces
- LED indicators for DFM, LOS, BPV and DCB Mode indication
- On-board oscillator and clock adapter for 1.544/2.048 MHz clock generation
- ZIF QFP socket for easy swapping of LXT334
- Switches and shorting blocks for Hardware Mode operation
- PC parallel port compatible interface and software for ease of use
- Quick setup and clear visibility of application settings
  - Local LIU testing
  - Complete system evaluation
  - Individual circuit isolation
- Socketed transformer and termination components for easy experimentation

LXD334 Evaluation Board



AUGUST 1996
Revision 1.0

LDB350/360 Evaluation Board

for T1/E1 Short- and Long-Haul Applications

General Description

The LDB350/360 Evaluation Board (Eval Board) is a versatile tool for engineers involved in designing T1/E1 short- or long-haul applications. It uses an LXT350, LXT351, LXT360 or LXT361 Line Interface Unit (LIU) and incorporates all supporting circuitry for either T1 or E1 applications. The LXT360/361 is the universal long-haul and short-haul transceiver. The LXT350/351 is the dedicated short-haul counterpart.

The LDB350/360 provides connector jacks for the line interface and BNC connectors for the framer interface. A bit error rate tester (BERT) or framer/mux may be used to provide the external signals needed for evaluation.

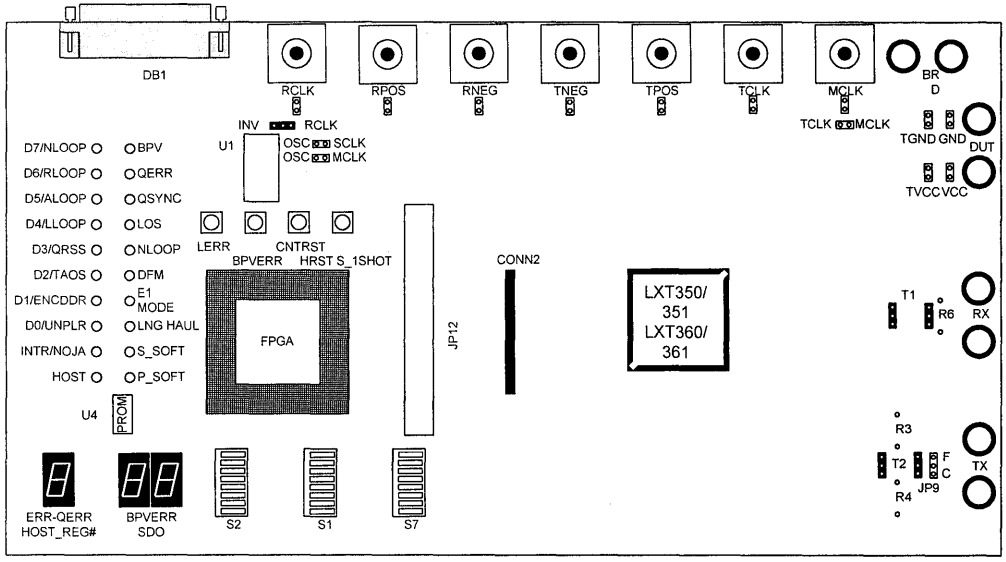
This document describes typical Eval Board setup procedures for both T1 and E1 environments.

Before using the Eval Board, review the latest LXT350/351 or LXT360/361 LIU data sheet for the most current information about these transceivers.

Features

- Quick setup, ease of use and clear visibility of application settings for:
  - Local LIU testing
  - Complete system evaluation
  - Individual circuit isolation
- Exercises crystal-less jitter attenuation of LIU
- Jitter attenuation switchable into either transmit or receive data path
- Twisted-pair line interface and all related digital signals available for analysis and testing
- Connector jacks for twisted-pair line interface
- BNC connectors for clock and framer interface
- LED indicators for major features
- Design supports both E1 and T1 evaluation
- Switches emulate stand-alone Hardware Mode and Software Mode with Serial Interface to the Host (for the LXT350 and LXT360)
- The LXT351 and LXT361 are controlled exclusively via an 8-bit parallel interface to the Host

LDB350/360 Evaluation Board



LDB70206

HDSL Evaluation Kit for 784 kbps Applications

General Description

The HDSL Evaluation Kit is a versatile tool for design engineers working with 784 kbps HDSL communications applications. The Development Kit for the Data Pump incorporates all the supporting circuitry needed for end-to-end testing of one HDSL line without external hardware or software. The Development Kit also supports connections to an external HDSL framer/mux and microprocessor to facilitate the development of a complete 2- or 3-loop HDSL system.

The Evaluation Kit includes two printed circuit boards that connect to each other through two PGA sockets:

- The HDSL Data Pump Development Board includes the power, signal, and digital data interfaces
- The HDSL Board contains the Data Pump and its supporting circuitry

The Evaluation Kit uses either of the two Data Pump control options:

- Hardware Control Mode (set up with DIP switches)
- Host Control Mode (set up through an external microprocessor)

Standard cable connectors and pin headers permit connection to signal analyzers, bit error rate testers (BERT), line emulators, and other instrumentation.

The Evaluation Kit design includes an RS422 interface for customized setups and RS449 interfaces for BERT connections.

Features

- Includes two complete Data Pumps and all supporting circuitry
- Facilitates system-wide design and evaluation
- RS449 connectors for BERT attachments
- RS422 connections for customized testing
- RJ45 connectors for twisted pair connections
- Hardware Mode operation uses DIP switches to control Data Pumps
- Host Mode operation using an external processor
- Basic error rate testing using all ones data requires only received clock and received data signals.
- Link Active indicator LEDs
- Independent reset switches for each loop

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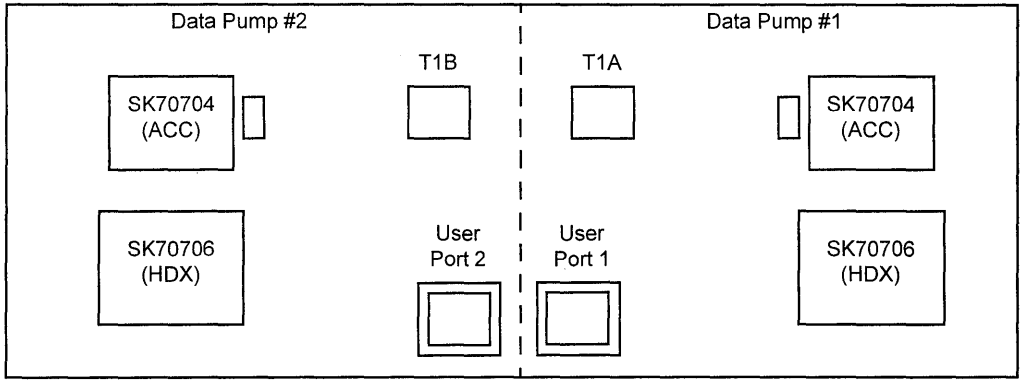
HDSL Data Pump Board



LDB70207

HDSL Evaluation Kit for 1168 kbps Applications

General Description

The HDSL Evaluation Kit is a versatile tool for design engineers working with 1168 kbps HDSL communications applications. The Evaluation Kit for the Data Pump incorporates all the supporting circuitry needed for end-to-end testing of one HDSL line without external hardware or software. The Evaluation Kit also supports connections to an external HDSL framer/mux and microprocessor to facilitate the development of a complete 2-loop HDSL system.

The Evaluation Kit includes two printed circuit boards that connect to each other through two PGA sockets:

- The HDSL Data Pump Development Board includes the power, signal, and digital data interfaces
- The HDSL Board contains the Data Pump and its supporting circuitry

The Evaluation Kit uses either of the two Data Pump control options:

- Hardware Control Mode (set up with DIP switches)
- Host Control Mode (set up through an external microprocessor)

Standard cable connectors and pin headers permit connection to signal analyzers, bit error rate testers (BERT), line emulators, and other instrumentation.

The Evaluation Kit design includes an RS422 interface for customized setups and RS449 interfaces for BERT connections.

Features

- Includes two complete Data Pumps and all supporting circuitry
- Facilitates system-wide design and evaluation
- RS449 connectors for BERT attachments
- RS422 connections for customized testing
- RJ45 connectors for twisted pair connections
- Hardware Mode operation uses DIP switches to control Data Pumps
- Host Mode operation using an external processor
- Basic error rate testing using all ones data requires only received clock and received data signals
- Link Active indicator LEDs
- Independent reset switches for each loop

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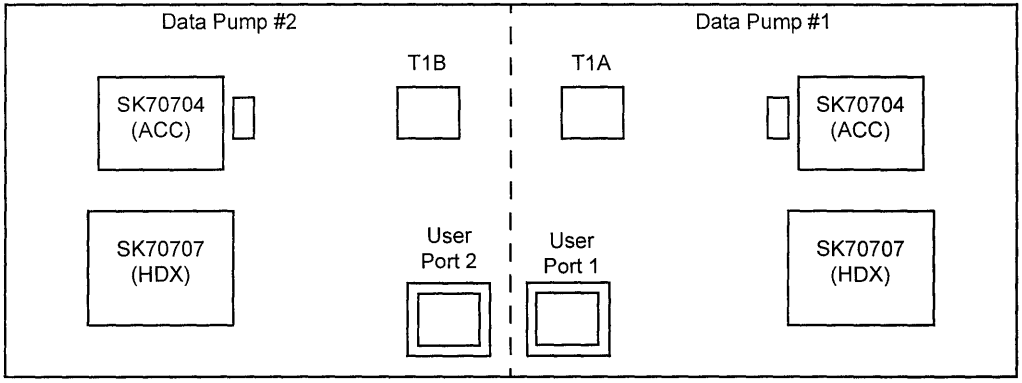
HDSL Data Pump Board



LXD710

Advance Information
JULY 1997

Evaluation Board for HDSL Framer/Mapper

General Description

The LXD710 Evaluation Board provides a development platform to aid in bringing an HDSL product to market in the shortest time. An entire Level One HDSL chip set can easily be evaluated with this board, which supports the SK70704 Analog Core Chip (ACC), the SK70707 1168 kbps HDSL Digital Transceiver Chip (HDX), and the LXP710 ETSI HDSL Framer/Mapper (HFMA).

Features

User Interface

- Display Demo Board Configuration
- Start Up Procedure
- Data Pump Control and Status
- HDSL Framer Control and Status
- E1 Framer and LIU Access Utility
- Test Utility and Loopback
- Diagnostic Program for System and HDSL Framer

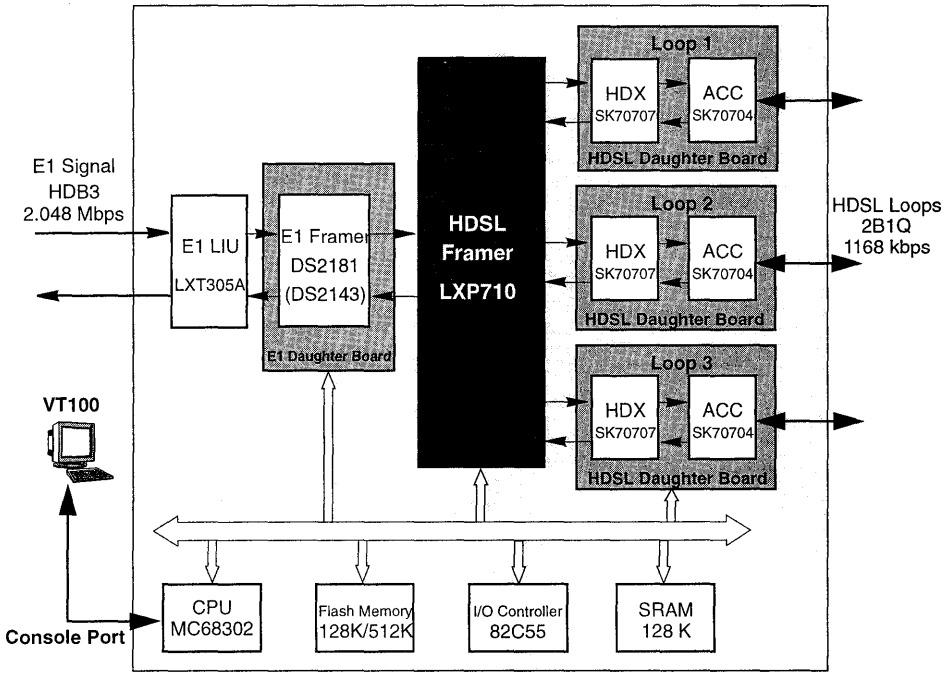
Performance Monitoring

- Remote E1 BPV indicate bit counter
- HDSL CRC check error counter
- HDSL FEBE indicate bit counter

Testability

- E1 LIU Loopback (Remote/Local)
- E1 Interface Loopback (Remote/Local)
- HDSL Interface Loopback (Local)
- HDSL Front-End Loopback
- HDSL Back-End Loopback
- QRSS test pattern generation and detection for each loop

LXD710 Evaluation Board System Architecture



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LXDMDSL

Multi-Rate DSL Transceiver Evaluation Board

General Description

The MDSL Transceiver Evaluation Board is a versatile tool for evaluating the performance of the Level One Multi-Rate Digital Subscriber Line (MDSL) transceiver chip set for line rates between 272 and 784 kbps. The Evaluation Board includes two transceivers and all components required to activate an MDSL link without external hardware or software.

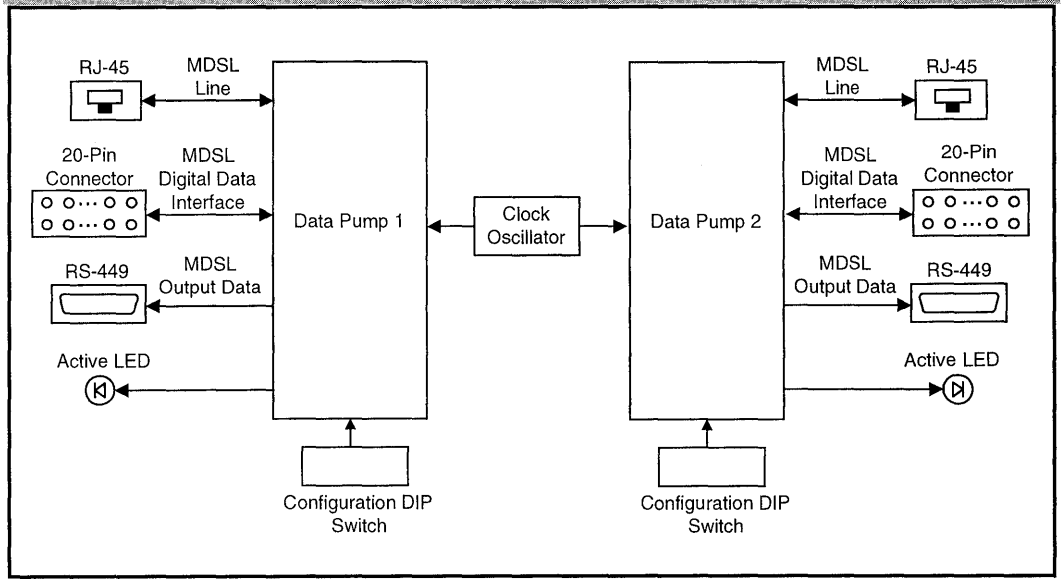
The evaluation board is composed of two printed circuit boards which mate with PGA connectors. The motherboard provides the clock oscillator, power supply and signal connectors, and is used for all line rates. The data pump daughtercard contains both transceiver chip sets and is configured and tested for one of the 272, 400, 528 or 784 kbps line rates. Each daughtercard is supplied with the correct clock oscillator which installs on the motherboard.

The Evaluation Board allows bit-error rate measurement with fixed data patterns to facilitate transmission reach and noise margin testing using a twisted pair-line or loop emulator. The Evaluation Board also supports the chip set test modes used for transmit pulse template, output power and power spectral density measurements.

Features

- Includes two transceivers for end-to-end testing
- Digital data interface connector facilitates system prototype development
- RS-449 Output Data Interface allows fixed data pattern bit-error rate measurements with a communication analyzer
- RJ45 connectors for twisted-pair line connections
- Stand-alone operation using DIP switches to control:
  - link activation & deactivation
  - master/slave mode selection
  - data loopbacks
  - transmitter test modes

LXDMDSL Evaluation Board



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JULY 1997
Revision 0.0

SDB6208

E12 Demonstration/Evaluation Board For The SXT6234

General Description

The SDB-6208 E12 Demonstration/Evaluation Board is a versatile, full featured evaluation tool designed specifically for engineering evaluation of the SXT6234 E-Rate Multiplexer. This tool uses one SXT6234 circuit and includes all supporting circuitry for E1 and E2 multiplexer/demultiplexer applications.

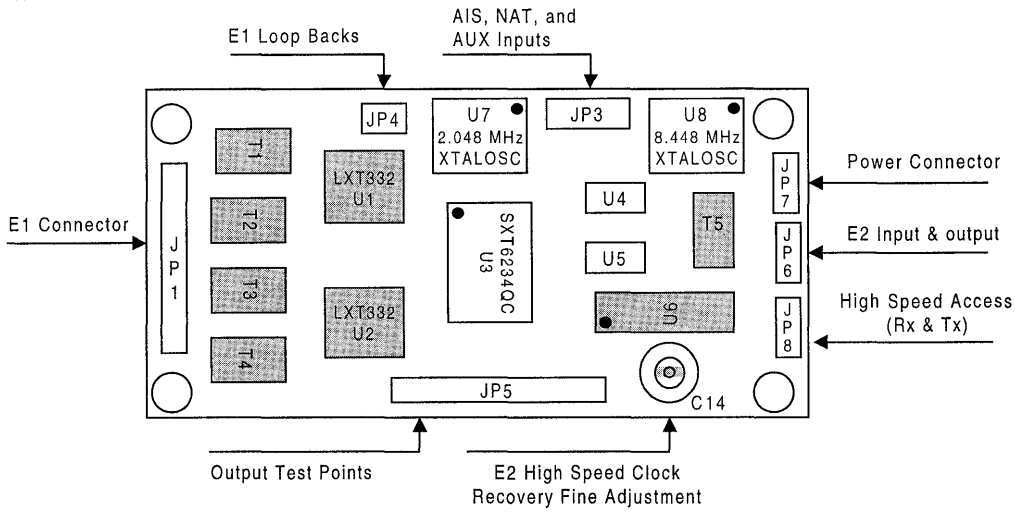
The Demo Board provides a keyed connector for power and ground. Pin connectors (JP1- JP6) are provided for input and output signals. JP1 is for E1 I/O and JP6 is for E2 I/O.
JP4 is for Local Loop Back and Remote Loop Back select.
JP3 sets various functions and JP5 provides a convenient way to monitor signals.
JP8 provides direct access to NRZ data clock at the output of the Mux as well as direct input to the Demultiplexer, to allow testing in proprietary scheme.

Before using the Demo Board, review the current SXT6234 data sheet for the most current information about this product.

Features

- Board design permits quick set-up, ease of use and clear visibility of application settings.
- Complete system evaluation including Line Interface Units.
- Test points for both NRZ data and Sync.
- Keyed connector for Vcc and ground.
- LED indicators for power.
- LED indicators for signal loss.
- Pin connectors for input and output signals.
- Jumper, for Loop Back.
- Fourteen-pin connector for monitoring the National, AIS, and Aux flag bits, and

SDB6208 Demo Board, Simplified Layout



SDB6234

Evaluation Board for the SXT6234

General Description

The SDB6234 Evaluation Board is a versatile, full featured evaluation tool designed specifically for engineering evaluation of the SXT6234 E-Rate Multiplexer. This tool uses two SXT6234 circuits and includes all supporting circuitry for E1, E2, and E3 multiplexer/demultiplexer applications.

The Evaluation Board provides banana jacks for power (J3) and ground (J2). BNC connectors are provided for input and output signals. DIP switch S1 selects various functions and connector J4 provides a convenient way to monitor signals.

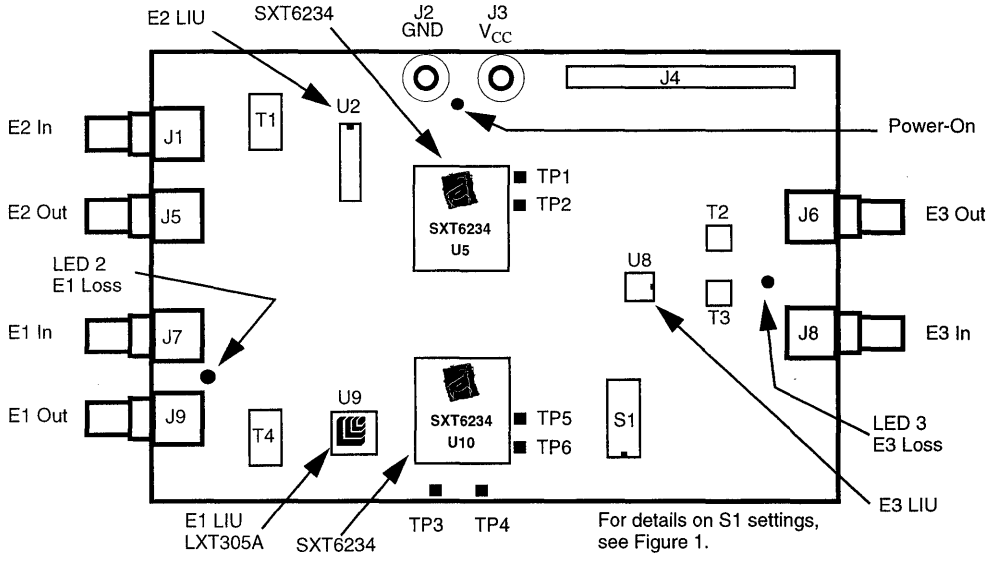
This document describes configurations for both E1-to-E2 and E1-to-E3 multiplexing with setup details for each. Note that each SXT6234 E-Rate multiplexer chip on the board is configured to use only one of the four tributary inputs.

Before using the Evaluation Board, review the current SXT6234 data sheet for the most current information about this product.

Features

- Board design permits quick set-up, ease of use and clear visibility of application settings
- Complete system evaluation including Line Interface Units
- Test points for both NRZ data and Sync
- Banana jacks for V_{CC} and ground
- LED indicators for power
- LED indicators for signal loss
- BNC connectors for input and output signals
- DIP switch for easy configuration set-up
- Eighteen-pin connector for monitoring the National, AIS, and Aux flag bits, and alarms
- Design supports:
  - E1 to E2 multiplexing/demultiplexing
  - E1 to E3 multiplexing/demultiplexing

SDB6234 Evaluation Board



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Ethernet Phy Products

JUNE 1997
Revision 1.0

LXT901A/907A

Universal Ethernet Transceiver

General Description

The LXT901A and LXT907A Universal Ethernet Transceivers are new-generation LXT901 and LXT907 replacements with improved noise immunity and output filtering. The feature set of the LXT901A/907A has been streamlined, removing Remote Signaling capabilities. The LXT901A and LXT907A provide all the active circuitry to interface most standard 802.3 controllers to either the 10BASE-T media or Attachment Unit Interface (AUI).

The LXT901A and LXT907A are identical except for the function of one pin. The LXT901A with selectable termination impedance ($\overline{STP}$) allows the use of either shielded or unshielded twisted-pair cable. The LXT907A offers a Signal Quality Error disable (DSQE) function.

LXT901A and LXT907A functions include Manchester encoding/decoding, receiver squelch and transmit pulse shaping, jabber, link testing and reversed polarity detection/correction.

Applications

- 10BASE-T hub and switching products
- Computer/workstation 10BASE-T LAN adapter boards

Features

Functional Features

- Integrated Filters - Simplify FCC Compliance
- Integrated Manchester Encoder/Decoder
- 10BASE-T Transceiver
- AUI Transceiver
- Full-Duplex Capable (20 Mbps)

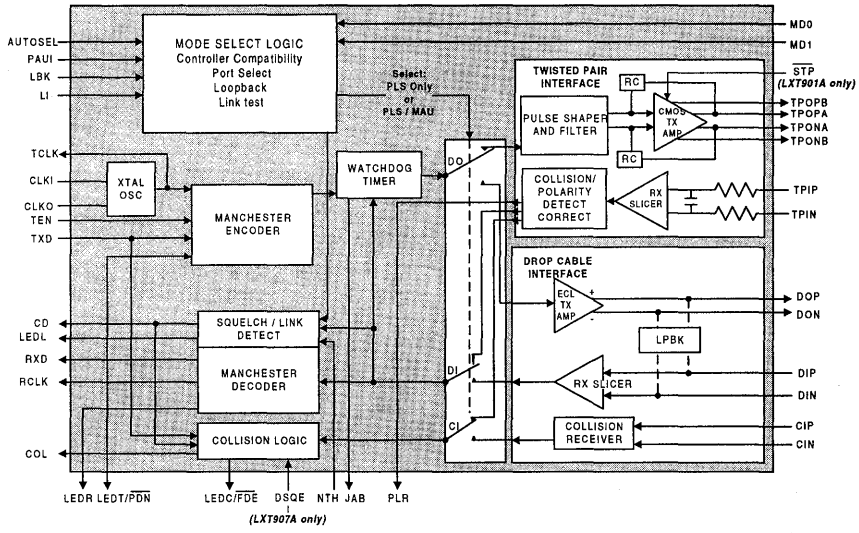
Convenience Features

- Automatic/Manual AUI/RJ45 Selection
- Automatic Polarity Correction
- DSQE Disable function (*LXT907A*)
- Programmable Impedance Driver (*LXT901A*)
- Power Down Mode and four loopback modes
- Available in 64-pin LQFP and 44-pin PLCC packages

Diagnostic Features

- Four LED Drivers
- AUI/RJ45 Loopback

LXT901A/907A Block Diagram



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PIN ASSIGNMENTS AND SIGNAL DESCRIPTIONS

Figure 1: LXT901A/907A Pin Assignments

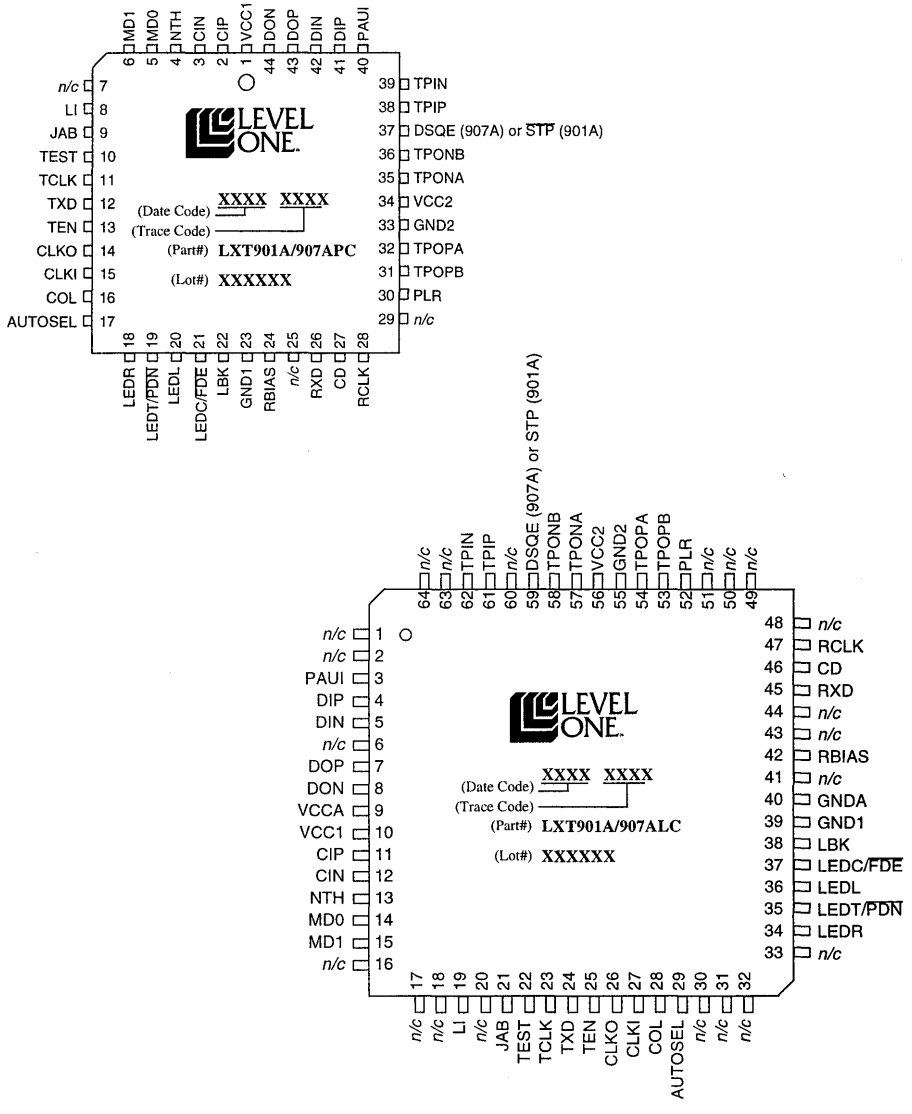

Table 1: LXT901A/907A Signal Descriptions

Pin #		Symbol	I/O[1]	Description
PLCC	LQFP			
1 34	10 56	VCC1 VCC2	– –	**Power Supply 1 and 2.** Power supply inputs of +5 volts.
2 3	11 12	CIP CIN	I I	**AUI Collision Pair.** Differential input to the AUI transceiver CI circuit. The input is collision signaling or SQE.
4	13	NTH	I	**Normal Threshold.** Selects normal or reduced threshold. When NTH is High, the normal TP squelch threshold is in effect. When NTH is Low, the normal TP squelch threshold is reduced by 4.5 dB.
5 6	14 15	MD0 MD1	I I	**Mode Select 0 (MD0) and Mode Select 1 (MD1).** Mode select pins determine the controller compatibility mode in accordance with Table 2.
8	19	LI	I	**Link Test Enable.** Controls Link Integrity Test; enabled when LI = High, disabled when LI = Low
9	21	JAB	O	**Jabber Indicator.** Output goes High to indicate Jabber state.
10	22	TEST	I	**Test.** For Level One internal use only. It is recommended to tie this pin High externally.
11	23	TCLK	O	**Transmit Clock.** A 10 MHz clock output. This clock signal should be directly connected to the transmit clock input of the controller.
12	24	TXD	I	**Transmit Data.** Input signal containing NRZ data to be transmitted on the network. Connect TXD directly to the transmit data output of the controller.
13	25	TEN	I	**Transmit Enable.** Enables data transmission and starts the watchdog timer. Synchronous to TCLK (see Test Specifications for details).
14 15	26 27	CLKO CLKI	O I	**Crystal Oscillator.** A 20 MHz crystal must be connected across these pins, or a 20 MHz clock applied at CLKI with CLKO left open.
16	28	COL	O	**Collision Detect.** Output which drives the collision detect input of the controller.
17	29	AUTOSEL	I	**Automatic Port Select.** When High, automatic port selection is enabled (the 901A/907A defaults to the AUI port only if TP link integrity = Fail). When Low, manual port selection is enabled (the PAUI pin determines the active port).
18	34	LEDR	OD	**Receive LED.** Open drain driver for the receive indicator LED. Output is pulled Low during receive.
19	35	LEDT/ PDN	OD	**Transmit LED (LEDT)/Power Down ($\overline{\text{PDN}}$).** Open drain driver for the transmit indicator. Output is pulled Low during transmit. If externally pulled Low, the LXT901A/907A goes to power down state.
20	36	LEDL	OD	**Link LED.** Open drain driver for link integrity indicator. Output is pulled Low during link test pass. If externally tied Low, internal circuitry is forced to "Link Pass" state and the 901A/907A will transmit link test pulses continuously.

1. I/O Column Coding: I = Input O= Output, OD = Open Drain

Table 1: LXT901A/907A Signal Descriptions – continued

Pin #		Symbol	I/O[1]	Description
PLCC	LQFP			
21	37	LEDC/ $\overline{\text{FDE}}$	OD	**Collision LED (LEDC)/Full Duplex Enable ($\overline{\text{FDE}}$).** Open drain driver for the collision indicator pulls Low during collision. LED "On" (i.e., Low output) time is extended by approximately 100 ms. If externally tied Low, enables full duplex operation by disabling the internal TP loopback and collision detection circuits in anticipation of external TP loopback or full duplex operation. If this pin is not used, tie high or directly to Vcc.
22	38	LBK	I	**Loopback.** Enables internal loopback mode. Refer to Functional Description for details.
23 33	39 40	GND1 GND2	– –	**Ground Returns 1 and 2.** Grounds
24	42	RBIAS	I	**Bias Control.** A 12.4 kΩ 1% resistor to ground at this pin controls operating circuit bias.
26	45	RXD	O	**Receive Data.** Output signal. Connect directly to the receive data input of the controller.
27	46	CD	O	**Carrier Detect.** An output to notify the controller of activity on the network.
28	47	RCLK	O	**Receive Clock.** A recovered 10 MHz clock which is synchronous to the received data. Connect to the controller receive clock input.
30	52	PLR	O	**Polarity Reverse.** Output goes High to indicate reversed polarity at the TP input.
31 36 32 35	53 58 54 57	TPOPB TPONB TPOPA TPONA	O O O O	**Twisted-Pair Transmit Pairs A & B.** Two differential driver pair outputs (A and B) to the twisted-pair cable. The outputs are pre-equalized. Each pair must be shorted together and tied to the transformer through a 24.9 Ω 1% series resistor to match impedance of 100 Ω Refer to Figure 15 in the Applications Section for information on 150Ω configurations.
37	59	$\overline{\text{STP}}$	I	**$\overline{\text{STP}}$ Select (LXT901A only).** When $\overline{\text{STP}}$ is Low, 150 Ω termination for shielded TP is selected. When $\overline{\text{STP}}$ is High, 100 Ω termination for unshielded TP is selected. LXT907A is designed for 100Ω UTP termination (not selectable).
		DSQE	I	**Disable SQE (LXT907A only).** When DSQE is High, the SQE function is disabled. When DSQE is Low, the SQE function is enabled. SQE must be disabled for normal operation in Hub/Switch applications. LXT901A operates with SQE enabled (not selectable).

1. I/O Column Coding: I = Input O= Output, OD = Open Drain

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Table 1: LXT901A/907A Signal Descriptions – continued

Pin #		Symbol	I/O[1]	Description
PLCC	LQFP			
38 39	61 62	TPIP TPIN	I I	**Twisted-Pair Receive Pair.** A differential input pair from the TP cable. Receive filter is integrated on-chip. No external filters are required.
40	3	PAUI	I	**Port/AUI Select.** In Manual Port Select mode (AUTOSEL Low), PAUI selects the active port. When PAUI is High, the AUI port is selected. When PAUI is Low, the TP port is selected. In Auto Port Select mode, PAUI must be tied to ground.
41 42	4 5	DIP DIN	I I	**AUI Receive Pair.** Differential input pair from the AUI transceiver DI circuit. The input is Manchester encoded.
43 44	7 8	DOP DON	O O	**AUI Transmit Pair.** A differential output driver pair for the AUI transceiver cable. The output is Manchester encoded.
7, 25, 29	1, 2, 6, 16, 17, 18, 20, 30, 31, 32, 33, 41, 43, 44, 48, 49, 50, 51, 60, 63, 64	N/C	–	**No Connect** (Internally tied to ground).

1. I/O Column Coding: I = Input O= Output, OD = Open Drain

FUNCTIONAL DESCRIPTION

The LXT901A/907A Universal Ethernet Interface Transceivers perform the physical layer signaling (PLS) and Media Attachment Unit (MAU) functions as defined by the IEEE 802.3 specification. They function as a PLS-Only device (for use with 10BASE-2 or 10BASE-5 coaxial cable networks) or as an Integrated PLS/MAU (for use with 10BASE-T twisted-pair networks). In addition to standard 10 Mbps operation, they also support full-duplex 20 Mbps operation.

The LXT901A/907A interfaces a back-end controller to either an AUI drop cable or a twisted-pair (TP) cable. The controller interface includes transmit and receive clock and NRZ data channels, as well as mode control logic and signaling. The AUI interface comprises three circuits: Data Output (DO), Data Input (DI) and Collision (CI). The twisted-pair interface comprises two circuits: Twisted-Pair Input (TPI) and Twisted-Pair Output (TPO). In addition to the three basic interfaces, the LXT901A/907A contains an internal crystal oscillator and four LED drivers for visual status reporting.

Functions are defined from the back-end controller side of the interface. The Transmit function refers to data transmitted by the back-end to the AUI cable (PLS-Only mode) or to the twisted-pair network (Integrated PLS/MAU mode). The Receive function refers to data received by the back-end from the AUI cable (PLS-Only) or from the twisted-pair network (Integrated PLS/MAU mode). In the integrated PLS/MAU mode, the LXT901A/907A performs all required MAU functions defined by the IEEE 802.3 10BASE–T specification such as collision detection, link integrity testing, signal quality error messaging, jabber control and loopback. In the PLS-Only mode, the LXT901A/907A receives incoming signals from the AUI DI circuit with ± 18 ns of jitter and drives the AUI DO circuit.

Controller Compatibility Modes

The LXT901A/907A are compatible with most industry standard controllers including devices produced by Motorola, AMD, Intel, Fujitsu, National Semiconductor, Seeq and Texas Instruments. Four different control signal timing and polarity schemes (Modes 1 through 4) are required to achieve this compatibility. Mode select pins (MD0 and MD1) determine Controller compatibility modes as listed in Table 2. Refer to Test Specifications for a complete set of timing diagrams for each mode.

Table 2: Controller Compatibility Modes

Controller Mode	Setting	
	MD1	MD0
Mode 1 For Motorola 68EN360, MPC860, Advanced Micro Devices AM7990 or compatible controllers	Low	Low
Mode 2 For Intel 82596 or compatible controllers[1]	Low	High
Mode 3 For Fujitsu MB86950, MB86960 or compatible controllers (Seeq 8005)[2]	High	Low
Mode 4 For National Semiconductor 8390 or compatible controllers (TI TMS380C26)	High	High

2. Refer to Level One Application Note 51 when designing with Intel Controllers.
3. SEEQ controllers require inverters on CLK1, LBK, RCLK and COL.

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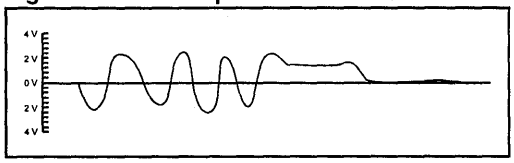
Transmit Function

The LXT901A/907A receives NRZ data from the controller at the TXD input, as shown in the block diagram on the first page of this Data Sheet, and passes it through a Manchester encoder. The encoded data is then transferred to either the AUI cable (the DO circuit) or the twisted-pair network (the TPO circuit). The advanced integrated pulse shaping and filtering network produces the output signal on TPON and TPOP as shown in Figure 2. The TPO output is pre-distorted and prefiltered to meet the 10BASE-T jitter template. An internal continuous resistor-capacitor filter is used to remove any high-frequency clocking noise from the pulse shaping circuitry. Integrated filters simplify the design work required for FCC compliant EMI performance. During idle periods, the LXT901A/907A transmits link integrity test pulses on the TPO circuit (if LI is enabled and integrated PLS/ MAU mode is selected). External resistors control the termination impedance for the LXT907A. External resistors and the $\overline{STP}$ Pin control termination impedance on the LXT901A.

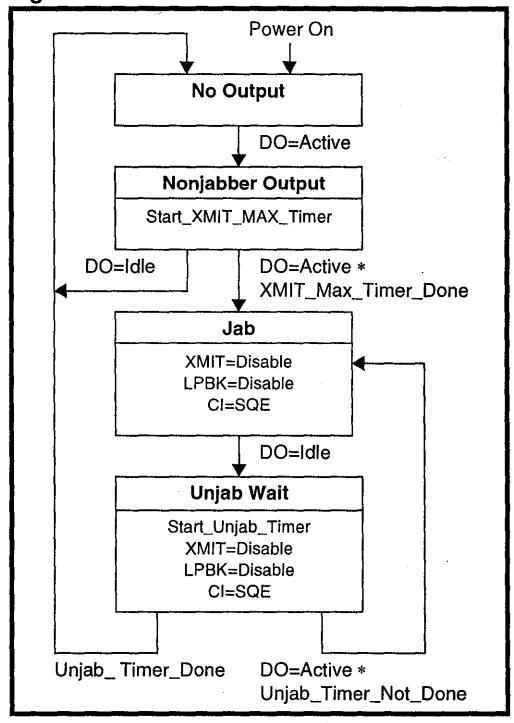
Figure 2: TPO Output Waveform



Jabber Control Function

Figure 3 is a state diagram of the LXT901A/907A Jabber control function. The on-chip watchdog timer prevents the DTE from locking into a continuous transmit mode. When a transmission exceeds the time limit, the watchdog timer disables the transmit and loopback functions, and activates the JAB pin. Once the LXT901A/907A is in the jabber state, the TXD circuit must remain idle for a period of 250 to 750ms before it will exit the jabber state.

Figure 3: Jabber Control Function



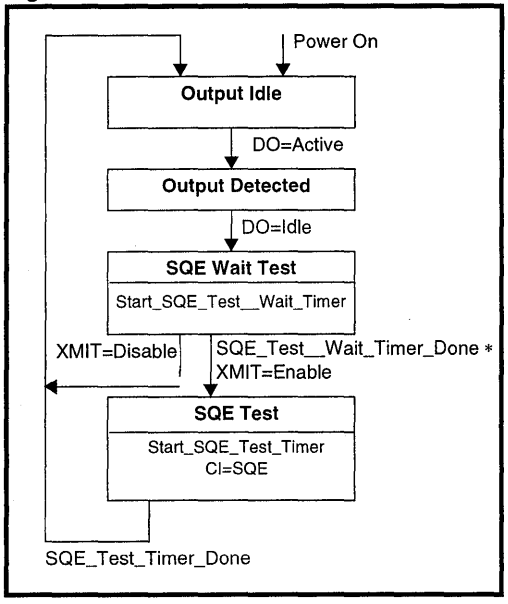
SQE Function

In the integrated PLS/MAU mode, the LXT901A/907A supports the signal quality error (SQE) function as shown in Figure 4, although the SQE function can be disabled on the LXT907A. After every successful transmission on the 10BASE-T network, when SQE is enabled, the LXT901A/907A transmits the SQE signal for 10BT ± 5BT over the internal CI circuit which is indicated on the COL pin of the device. When using the AUI of the LXT901A/907A, the SQE function is determined by the external MAU attached.

SQE Disable Function (LXT907A only)

SQE must be disabled for normal operation in hub and switch applications. The LXT907A is configured with an SQE Disable function. The SQE function is disabled when DSQE is set High, and enabled when DSQE is Low.

Figure 4: SQE Function



Receive Function

The LXT901A/907A receive function acquires timing and data from the twisted-pair network (the TPI circuit) or from the AUI (the DI circuit). Valid received signals are passed through the on-chip filters and Manchester decoder, then output as decoded NRZ data and receive timing on the RXD and RCLK pins, respectively.

An internal RC filter and an intelligent squelch function discriminate noise from link test pulses and valid data streams. The receive function is activated only by valid data streams above the squelch level and with proper timing. If the differential signal at the TPI or the DI circuit inputs falls below 75% of the threshold level (unsquelched) for 8 bit times (typical), the LXT901A/907A receive function enters the idle state. If the polarity of the TPI circuit is reversed, LXT901A/907A detects the polarity reverse and reports it via the PLR output. The LXT901A/907A automatically corrects reversed polarity.

Polarity Reverse Function

The LXT901A/907A polarity reverse function uses both link pulses and end-of-frame data to determine the polarity of the received signal. A reversed polarity condition is detected when eight opposite receive link pulses are detected without receipt of a link pulse of the expected polarity. Reversed polarity is also detected if four frames are received with a reversed start-of-idle. Whenever a correct polarity frame or a correct link pulse is received, these two counters are reset to zero. If the LXT901A/907A enters the link fail state and no valid data or link pulses are received within 96 to 128 ms, the polarity is reset to the default non-flipped condition. If Link Integrity Testing is disabled, polarity detection is based only on received data. Polarity correction is always enabled.

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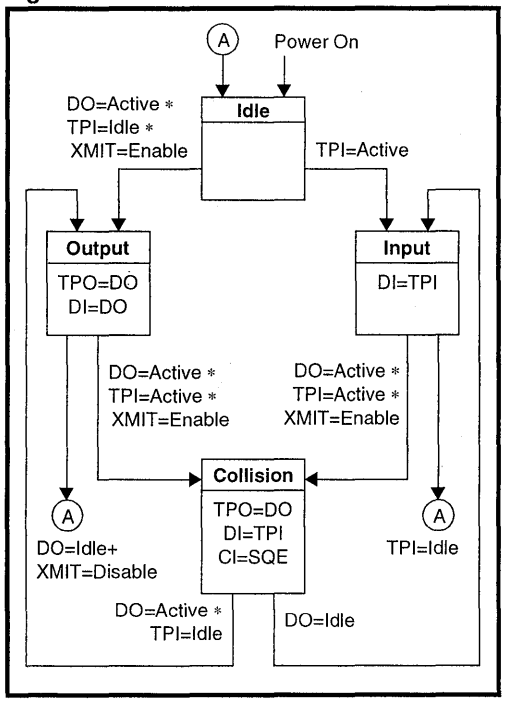
Collision Detection Function

The collision detection function operates on the twisted-pair side of the interface. For standard (half-duplex) 10BASE-T operation, a collision is defined as the simultaneous presence of valid signals on both the TPI circuit and the TPO circuit. The LXT901A/907A reports collisions to the back-end via the COL pin. If the TPI circuit becomes active while there is activity on the TPO circuit, the TPI data is passed to the back-end over the RXD circuit, disabling normal loopback. Figure 5 is a state diagram of the LXT901A/907A collision detection function. Refer to Test Specifications for collision detection and COL/CI output timing. (NOTE: For full-duplex operation on the TP or AUI port, the collision detection circuitry must be disabled by setting $\overline{\text{FDE}}$ Low.)

Figure 5: Collision Detection Function



Loopback Functions

Standard TP Loopback

The LXT901A/907A provides the standard loopback function defined by the 10BASE-T specification for the twisted-pair port. The loopback function operates in conjunction with the transmit function. Data transmitted by the back-end is internally looped back within the LXT901A/907A from the TXD pin through the Manchester encoder/decoder to the RXD pin and returned to the back-end. This standard loopback function is disabled when a data collision occurs, clearing the RXD circuit for the TPI data. Standard loopback is also disabled during link fail and jabber states. The LXT901A/907A also provides three additional loopback functions.

Forced TP Loopback

"Forced" TP loopback is controlled by the LBK pin. When the TP port is selected and LBK is High, TP loopback is "forced", overriding collisions on the TP circuit. When LBK is Low, normal loopback is in effect.

AUI Loopback

AUI loopback is also controlled by the LBK pin. When the AUI port is selected and LBK is High, data transmitted by the back-end is internally looped back from the TXD pin through the Manchester encoder/decoder to the RXD pin. When LBK is Low, no AUI loopback occurs.

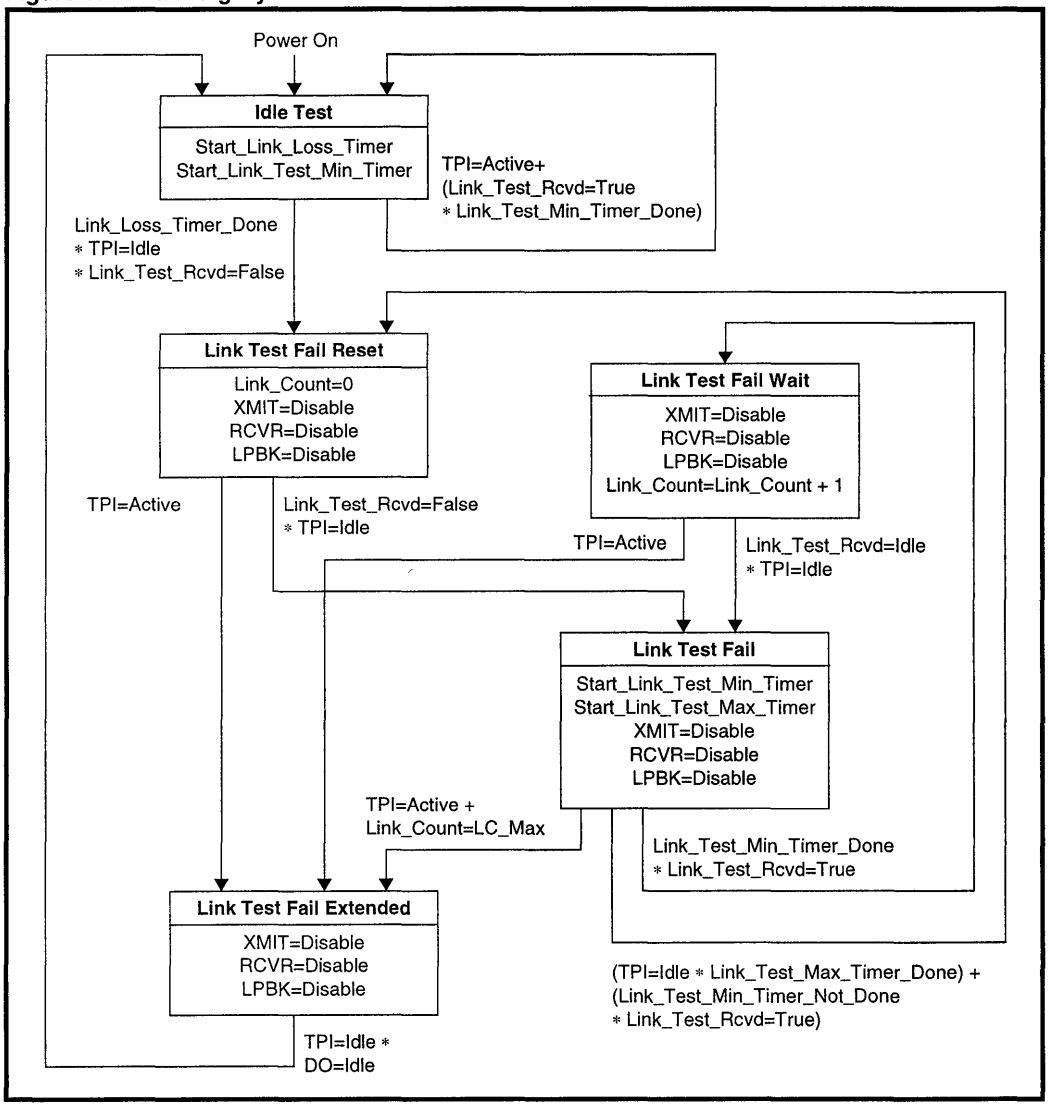
External Loopback

An external loopback mode, useful for system-level testing, is controlled by the LEDC/$\overline{\text{FDE}}$ pin. When LEDC/$\overline{\text{FDE}}$ is tied Low, the LXT901A/907A disables the collision detection and internal loopback circuits, to allow external loopback. External loopback mode can be set on either TP or AUI ports.

Link Integrity Test Function

Figure 6 is a state diagram of the LXT901A/907A Link Integrity test function. The link integrity test is used to determine the status of the receive side twisted-pair cable. Link integrity testing is enabled when the LI pin is tied High. When enabled, the receiver recognizes link integrity pulses which are transmitted in the absence of receive traffic. If no serial data stream or link integrity pulses are detected within 50 - 150 ms, the chip enters a link fail state and disables the transmit and normal loopback functions. The LXT901A/907A ignores any link integrity pulse with interval less than 2 - 7 ms. The LXT901A/907A will remain in the link fail state until it detects either a serial data packet or two or more link integrity pulses.

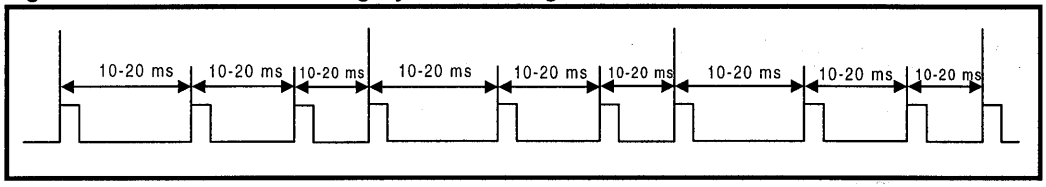
Figure 6: Link Integrity Test Function



Link pulse Transmission

When not transmitting data, the LXT901A/907A transmits 802.3-compliant standard link pulses. Figure 7 shows the link integrity pulse timing.

Figure 7: Transmitted Link Integrity Pulse Timing



APPLICATION INFORMATION

Twisted-Pair Impedance Matching

Resistors must be installed on each input and output pair to match impedance of the network media being used. The LXT907A is configured with 100Ω termination for Unshielded Twisted-Pair (UTP). In this case, the positive and negative sides of both output pairs are shorted together (TPOPA/TPOPB and TPONA/TPONB) and tied to the transformer through a 24.9 Ω 1% series resistor.

The LXT901A is designed with an $\overline{\text{STP}}$ Select pin that allows the device to match both 100Ω and 150Ω media. A dual resistor combination can be configured to accommodate either line termination as shown in Figure 15. When 100Ω termination is selected, both A and B pairs are driven in parallel. When 150Ω termination is selected, the B pair is tri-stated and only the A pair is driven.

Crystal Information

Designers should test and validate crystals before committing to a specific component. Based on limited evaluation, Table 3 lists some suitable crystals.

Table 3: Suitable Crystals

Manufacturer	Part Number
MTRON	MP-1
	MP-2

Magnetics Information

The LXT901A and LXT907A require a 1:1 ratio for the receive transformer and a 1:$\sqrt{2}$ ratio for the transmit transformer on the twisted-pair interface. The AUI Interface requires a 1:1 ratio for both the transmit and receive transformers. Table 4 lists some suitable magnetics.

Table 4: Suitable Magnetics

	Manufacturer	Part Number
Twisted-Pair	Fil-Mag	23Z128
		23Z128SM
	Valor	PT4069
		ST7011
	Belfuse	A553-0716
		S553-0716
	HALO	TD42-2006Q
		TG42-1406N1
AUI	Fil-Mag	23Z90
		23Z90SM
	Valor	LT6032
		ST7032
	HALO	TD01-0756K
		TG01-0756N

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Typical Applications

Figures 8 through 15 show typical LXT901A/907A applications.

Auto Port Select with External Loopback Control

Figure 8 is a typical LXT901A/907A application. The diagram is arranged to group similar pins together; it does not represent the actual LXT901A/907A pinout. The controller interface pins (transmit data, clock and enable; receive data and clock; and the collision detect, carrier detect and loopback control pins) are shown at the top left.

Programmable option pins are grouped center left. The PAUI pin is tied Low and all other option pins are tied High. This setup selects the following options:

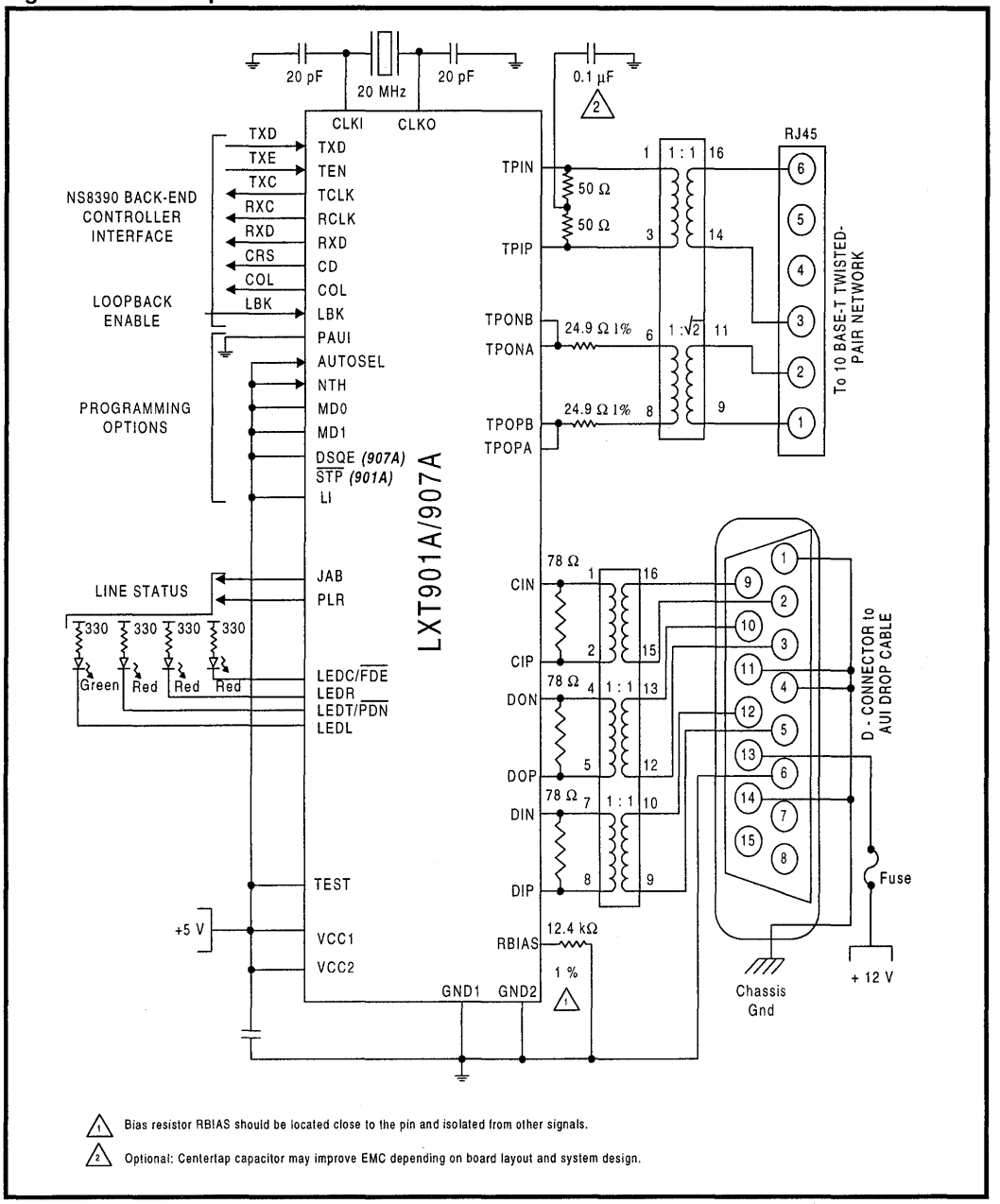
- Automatic Port Selection
  (PAUI Low and AUTOSEL High)
- Normal Receive Threshold (NTH High)
- Mode 4, compatible with National NS8390 controllers (MD0 High, MD1 High)
- SQE Disabled (DSQE High for LXT907A only)
- UTP is selected ($\overline{\text{STP}}$ High for LXT901A only)
- Link Testing Enabled (LI High)

Status outputs are grouped at lower left. Local status outputs drive LED indicators.

Power and ground pins are shown at the bottom of the diagram. A single power supply is used for both VCC1 and VCC2 with a decoupling capacitor installed between the power and ground busses.

The TP and AUI interfaces are shown at upper and lower right, respectively. Impedance matching resistors for 100Ω UTP are installed in each I/O pair and no external filters are required.

Figure 8: LAN Adapter Board - Auto Port Select with External LPBK Control

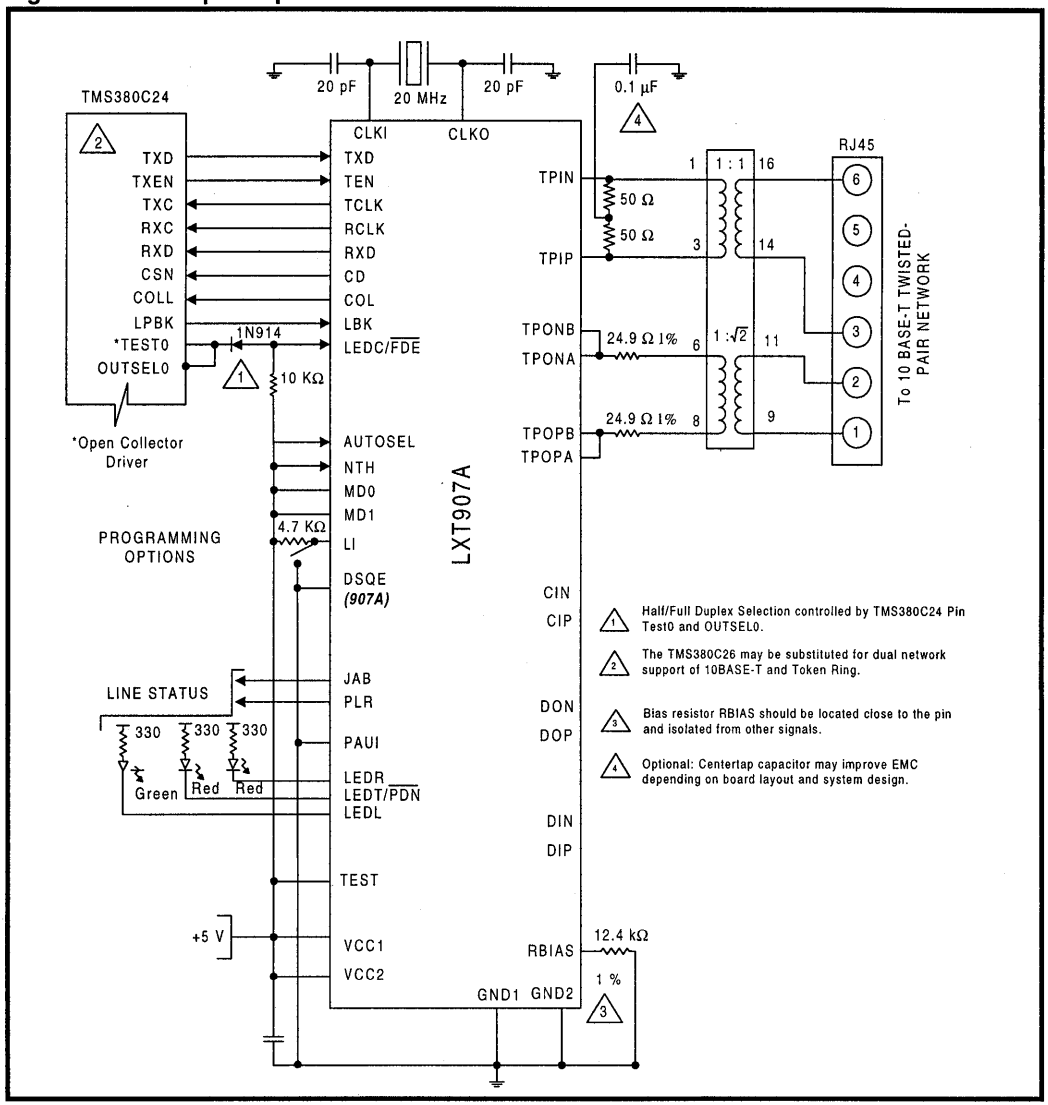


1. Bias resistor RBIAS should be located close to the pin and isolated from other signals.
2. Optional: Centertap capacitor may improve EMC depending on board layout and system design.

Full Duplex Support

Figure 9 shows the LXT907A with a Texas Instruments 380C24 CommProcessor. The 380C24 is compatible with Mode 4 (MD0 and MD1 both High). When used with the 380C24, or other full duplex-capable controller, the LXT907A supports full-duplex Ethernet, effectively doubling the available bandwidth of the network. In this application the SQE function is enabled (DSQE tied Low), and the AUI port is not used.

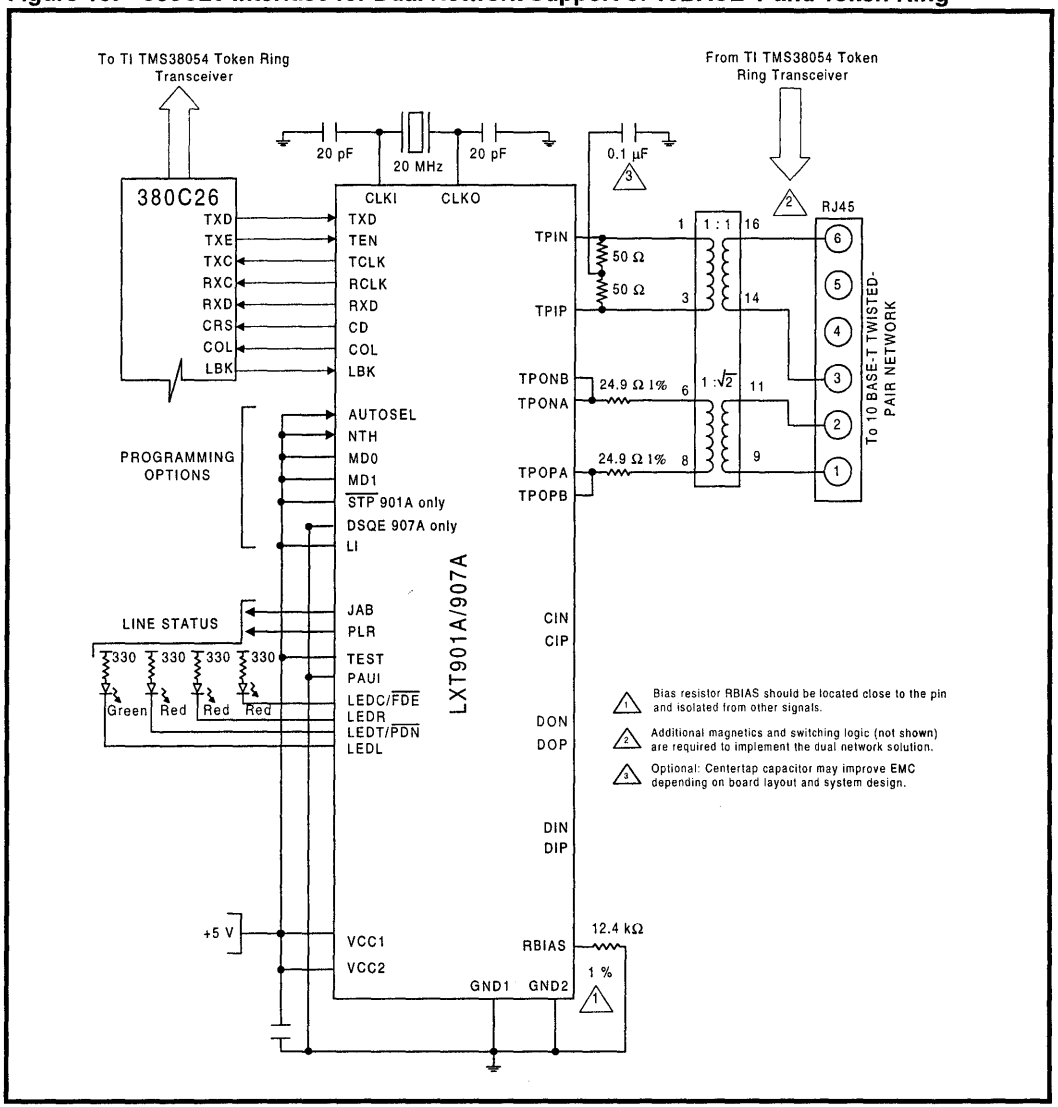
Figure 9: Full-Duplex Operation



Dual Network Support - 10Base-T and Token Ring

Figure 10 shows the LXT901A/907A with a Texas Instruments 380C26 CommProcessor. The 380C26 is compatible with Mode 4 (MD0 and MD1 both High). When used with the 380C26, both the LXT901A/907A and a TMS38054 Token Ring transceiver can be tied to a single RJ45 allowing dual network support from a single connector. The LXT901A/907A AUI port is not used. The DSQE pin on the LXT907A is tied Low and the $\overline{STP}$ pin on the LXT901A is tied High.

Figure 10: 380C26 Interface for Dual Network Support of 10BASE-T and Token Ring



Manual Port Select with Link Test Function

With MD0 tied Low and MD1 tied High, the LXT901A/907A logic and framing are set to Mode 3 (compatible with Fujitsu MB86950 and MB86960, and Seeq 8005 controllers). Figure 11 shows the setup for Fujitsu controllers. Figure 12 shows the four inverters required to interface with the Seeq 8005 controller. As in Figure 8 both these Mode 3 applications show the LI pin tied High, enabling Link Testing; and the $\overline{STP}$ (901A only) and NTH pins are both tied High, selecting the standard receiver threshold and 100 Ω termination for unshielded TP cable. However, in these applications AUTOSEL is tied Low, allowing external port selection through the PAUI pin.

Figure 11: LAN Adapter Board - Manual Port Select with Link Test Function

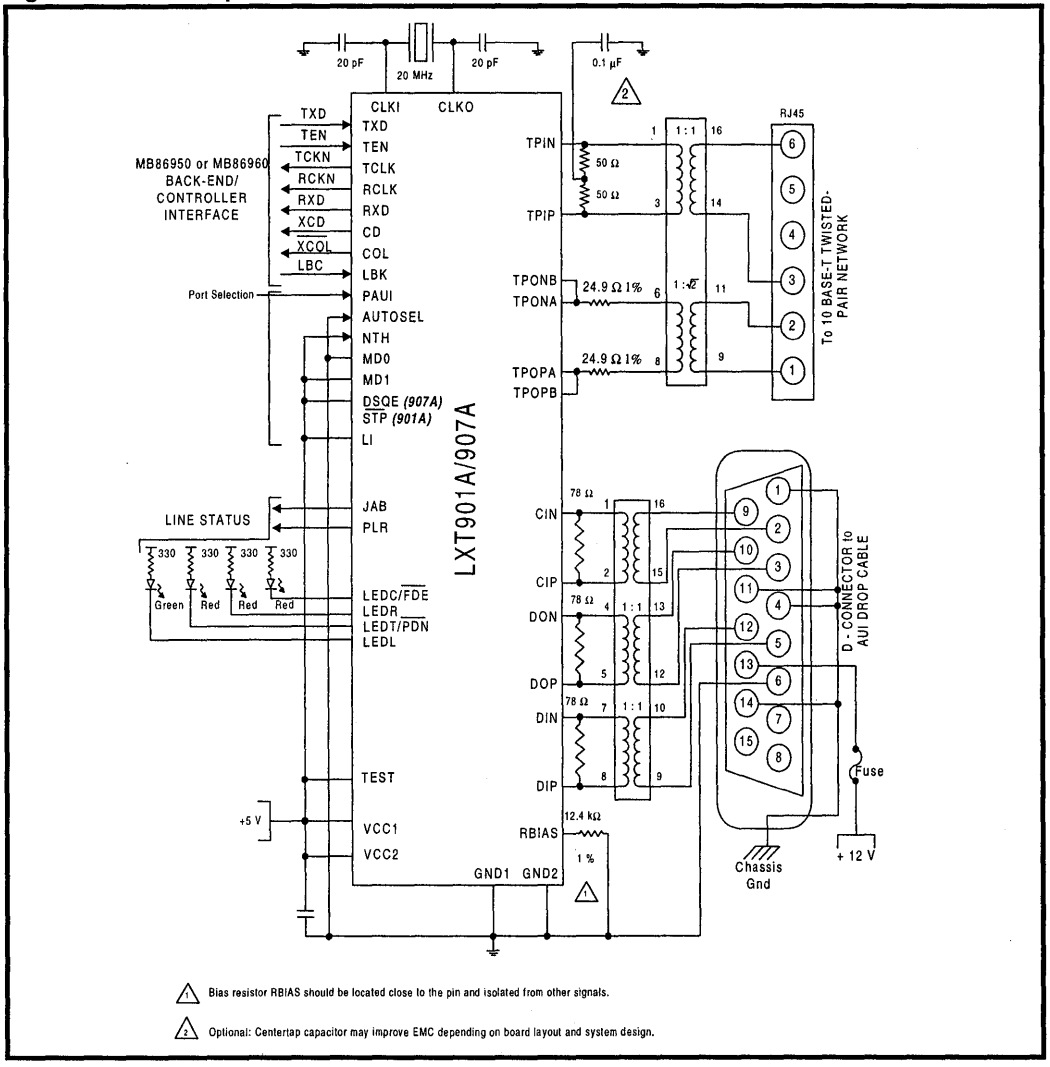
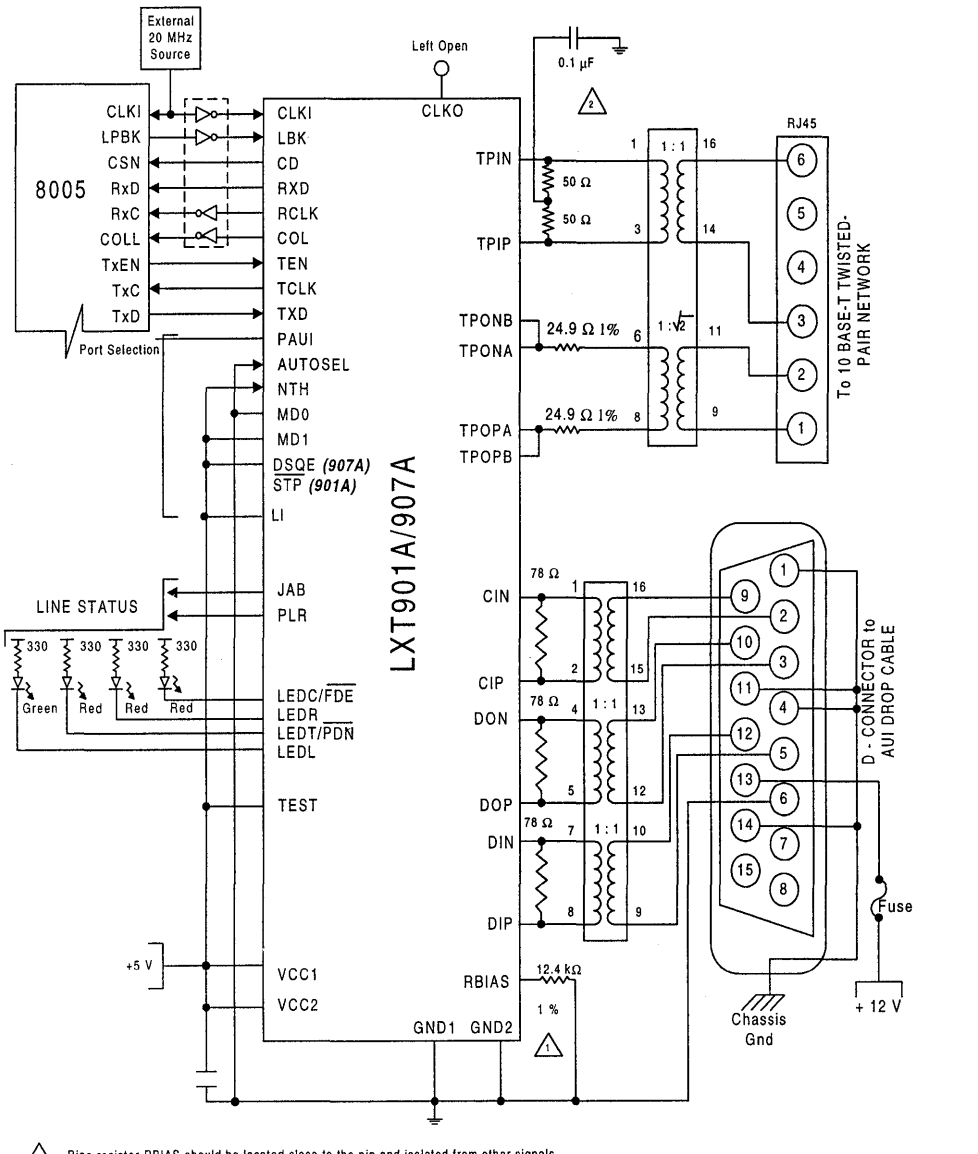


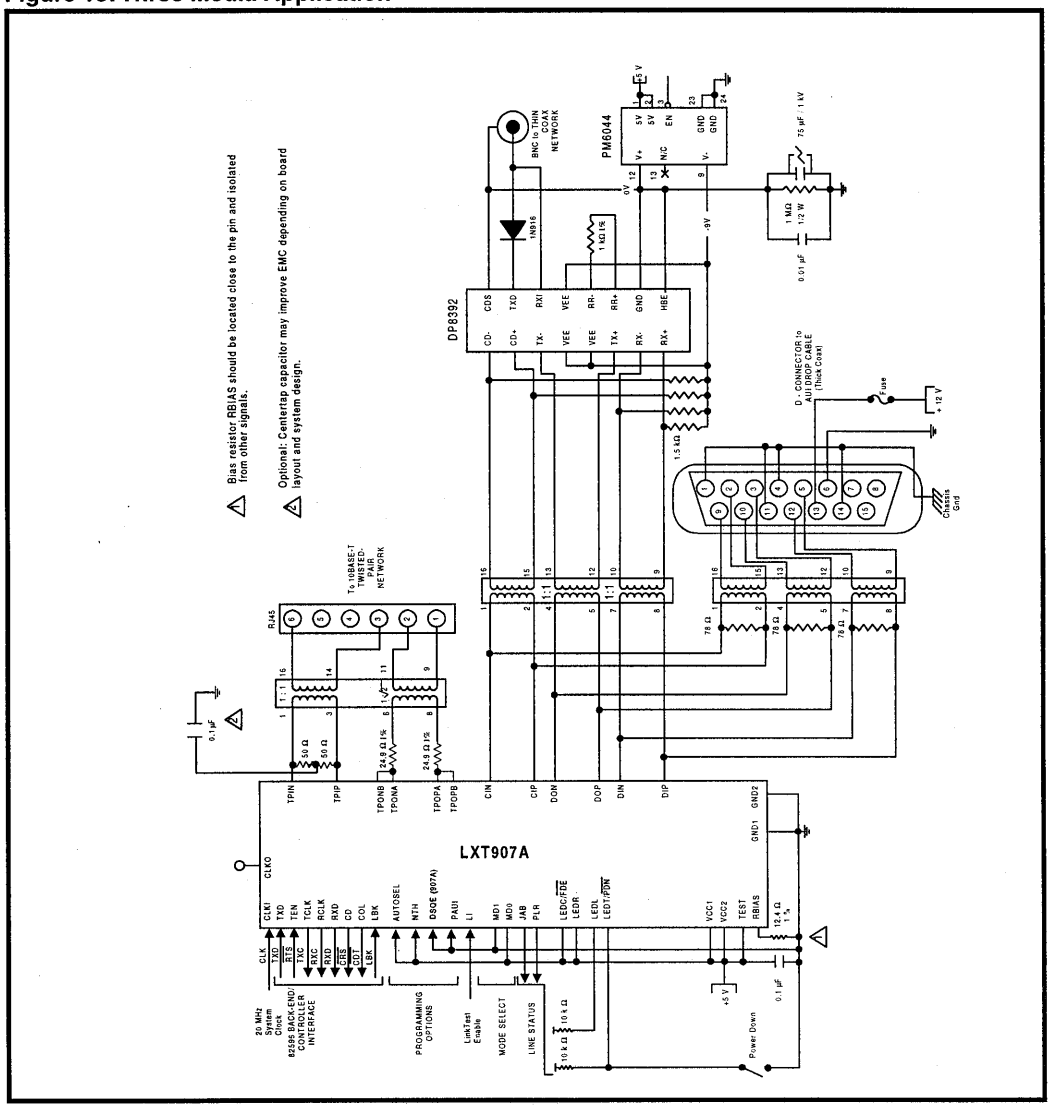
Figure 12: Manual Port Select with Seeq 8005 Controller



Three Media Application

Figure 13 shows the LXT907A in Mode 2 (compatible with Intel 82596 controllers) with additional media options for the AUI port. Two transformers are used to couple the AUI port to either a D-connector or a BNC connector. A DP8392 coax transceiver with PM6044 power supply are required to drive the thin coax network through the BNC.

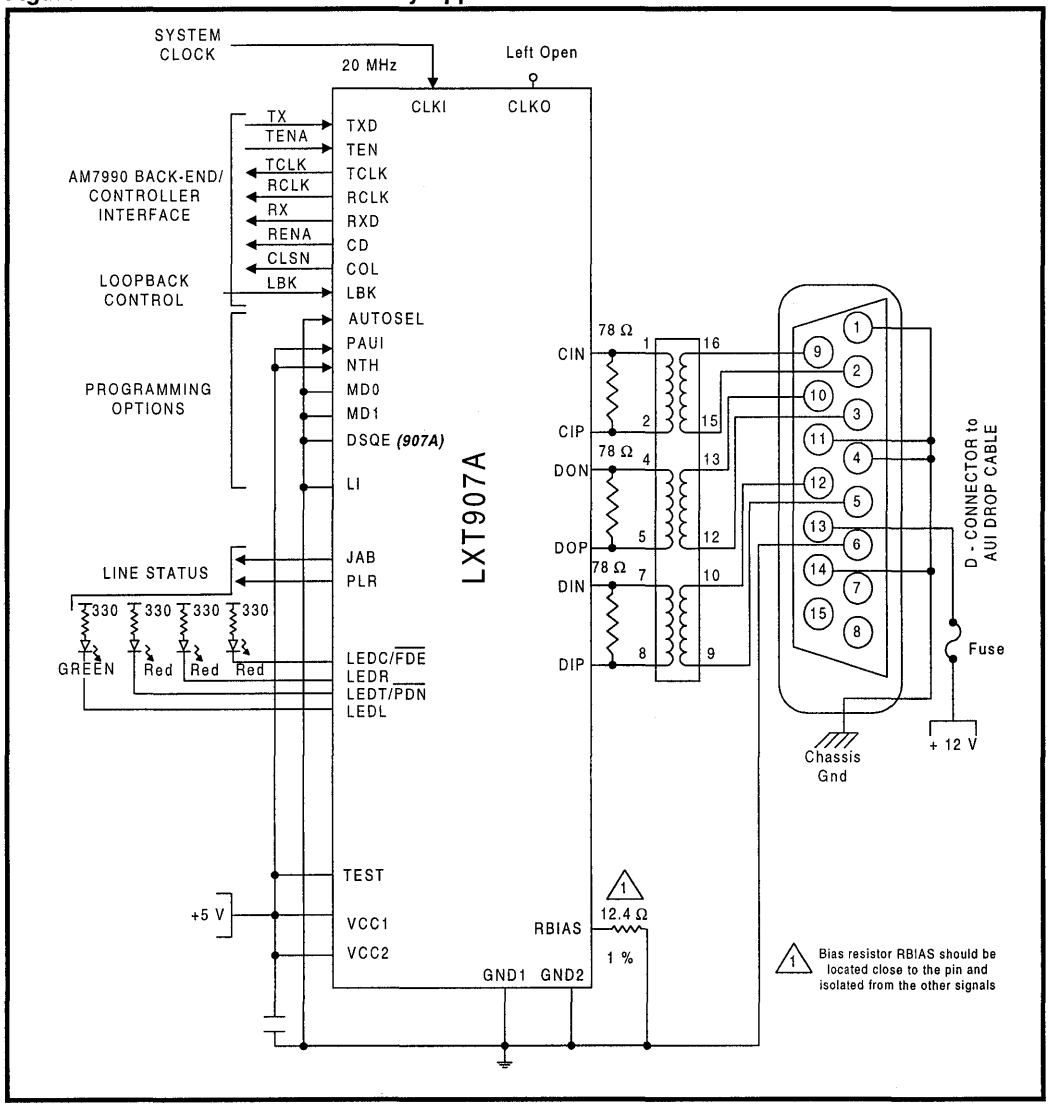
Figure 13: Three Media Application



AUI Encoder/Decoder Only

In this application (see Figure 14) the DTE is connected to a coaxial network through the AUI. AUTOSEL is tied Low and PAUI is tied High to manually select the AUI port. The twisted-pair port is not used. With MD1 and MD0 both Low, the logic and framing are set to Mode 1 (compatible with AMD AM7990 controllers). The LI pin is tied Low, disabling the link test function. The DSQE pin is also Low, enabling the SQE function on the LXT907A. The LBK input controls loopback. A 20 MHz system clock is supplied at CLK1 with CLK0 left open.

Figure 14: AUI Encoder/Decoder Only Application

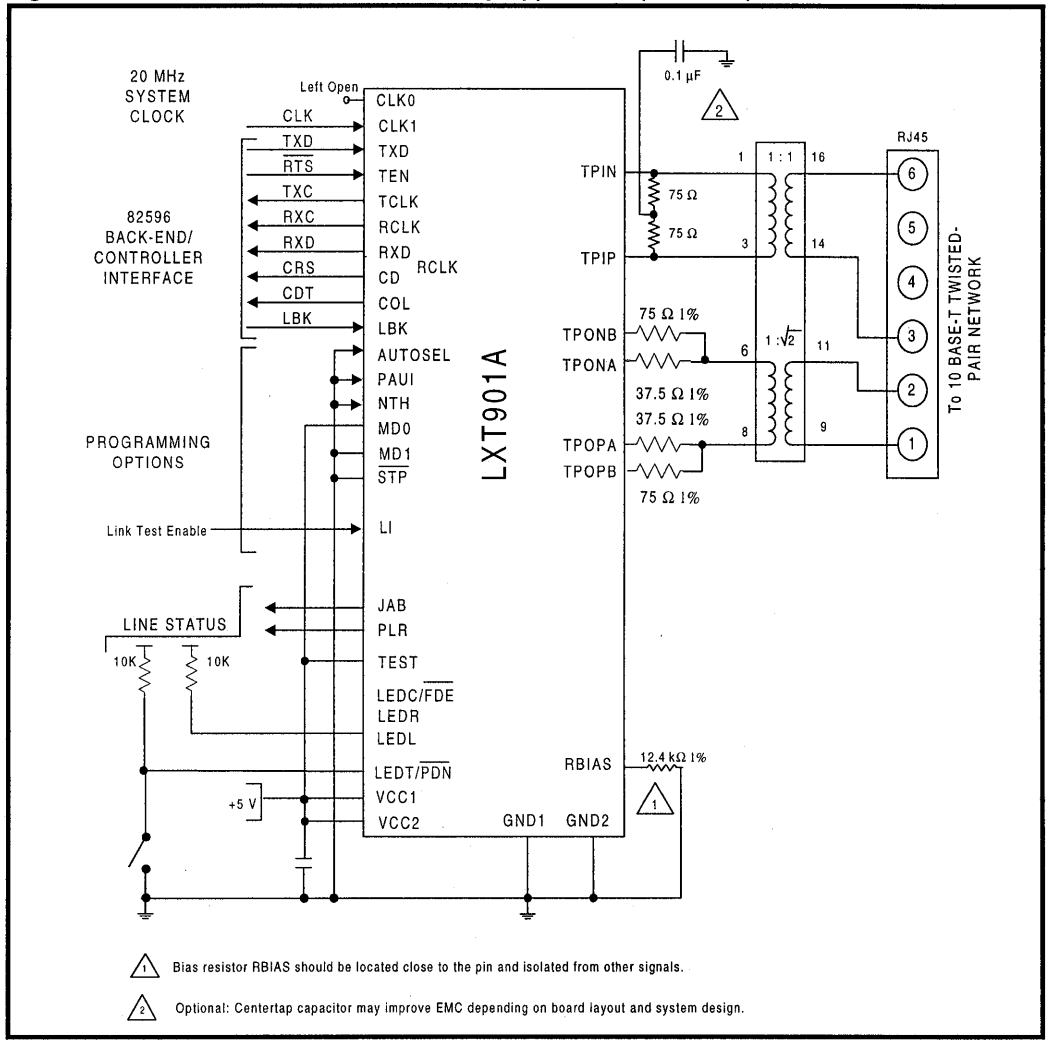


150 Ω Shielded Twisted-pair only (LXT901A only)

Figure 15 shows the LXT901A in a typical twisted-pair only application. The DTE is connected to a 10BASE-T network through the twisted-pair RJ45 connector. Note that the AUI port is not used. With MD0 tied High and MD1 Low, the LXT901A logic and framing are set to Mode 2 (compatible with Intel 82596 controllers).

A 20 MHz system clock input at CLK1 is used in place of the crystal oscillator. (CLK0 is left open). The L1 pin externally controls the link test function. The $\overline{\text{STP}}$ and NTH pins are both tied Low, selecting the reduced receiver threshold and 150 Ω termination for shielded TP cable. The switch at LEDT/$\overline{\text{PDN}}$ manually controls the power down mode.

Figure 15: 150 Ω Shielded Twisted-Pair Only Application (LXT901A)



TEST SPECIFICATIONS

NOTE

The minimum and maximum values in Tables 5 through 14 and Figures 16 through 41 represent the performance specifications of the LXT901A/907A and are guaranteed by test, except where noted by design.

Table 5: Absolute Maximum Values

Parameter	Symbol	Min	Max	Units
Supply voltage	V_{CC}	-0.3	6	V
Ambient operating temperature	T_A	0	70	°C
Storage temperature	T_{STG}	-65	+150	°C

CAUTION

Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 6: Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Recommended supply voltage[1]	V_{CC}	4.75	5.0	5.25	V
Recommended operating temperature	T_{OP}	0	–	70	°C

1. Voltages with respect to ground unless otherwise specified. Power supply should be filtered to suppress high frequency transients, consistent with good PCB design.

Table 7: I/O Electrical Characteristics (Over Recommended Range)

Parameter		Sym	Min	Typ[1]	Max	Units	Test Conditions
Input Low voltage[2]		VIL	–	–	0.8	V	
Input High voltage[2]		VIH	2.0	–	–	V	
Output Low voltage		VOL	–	–	0.4	V	IOL = 1.6 mA
		VOL	–	–	10	%VCC	IOL < 10 µA
Output Low voltage (Open drain LED driver)		VOLL	–	–	0.7	%VCC	IOLL = 10 mA
Output High voltage		VOH	2.4	–	–	V	IOH = 40 µA
		VOH	90	–	–	%VCC	IOH < 10 µA
Output rise time TCLK & RCLK	CMOS	–	–	7	12	ns	CLOAD = 20 pF
	TTL	–	–	7	8	ns	
Output fall time TCLK & RCLK	CMOS	–	–	7	12	ns	CLOAD= 20 pF
	TTL	–	–	7	8	ns	
CLKI rise time (externally driven)		–	–	–	10	ns	
CLKI duty cycle (externally driven)		–	–		40/60	%	
Supply current	Normal Mode	ICC	–	65	85	mA	Idle Mode
		ICC	–	95	120	mA	Transmitting on TP
		ICC	–	95	120	mA	Transmitting on AUI
	Power Down Mode	ICC	–	0.03	2	mA	

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Limited functional tests are performed at these input levels. The majority of functional tests are performed at levels of 0V and 3V.

Table 8: AUI Electrical Characteristics (Over Recommended Range)

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Input Low current	IIL	–	–	-700	µA	
Input High current	IIH	–	–	500	µA	
Differential output voltage	VOD	±550	–	±1200	mV	
Differential squelch threshold	VDS	150	250	350	mV	5 MHz square wave input

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 9: TP Electrical Characteristics (Over Recommended Range)

Parameter		Symbol	Min	Typ[1]	Max	Units	Test Conditions
Transmit output impedance		ZOUT	–	5	–	Ω	
Transmit timing jitter addition[2]		–	–	±3.3	±10	ns	0 line length for internal MAU
Transmit timing jitter added by the MAU and PLS sections[2, 3]		–	–	±3.3	±5.5	ns	After line model specified by IEEE 802.3 for 10BASE-T internal MAU
Receive input impedance		ZIN	–	20	–	kΩ	Between TPIP/TPIN, CIP/CIN & DIP/DIN
Differential squelch Threshold	Normal threshold; NTH = 1	VDS	300	400	585	mV	5 MHz square wave input
	Reduced threshold; NTH = 0	VDS	180	250	345	mV	5 MHz square wave input

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Parameter is guaranteed by design, not subject to production testing.
3. IEEE 802.3 specifies maximum jitter additions at 1.5 ns for the AUI cable, 0.5 ns from the encoder, and 3.5 ns from the MAU.

Table 10: Switching Characteristics (Over Recommended Range)

Parameter		Symbol	Minimum	Typical[1]	Maximum	Units
Jabber Timing	Maximum transmit time	–	20	–	150	ms
	Unjab time	–	250	–	750	ms
Link Integrity Timing	Time link loss receive	–	50	–	150	ms
	Link min receive	–	2	–	7	ms
	Link max receive	–	50	–	150	ms
	Link transmit period	–	8	10	24	ms

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 11: RCLK/Start-of-Frame Timing (Over Recommended Range)

Parameter		Symbol	Minimum	Typical[1]	Maximum	Units
Decoder acquisition time	AUI	tDATA	–	900	1100	ns
	TP	tDATA	–	1200	1500	ns
CD turn-on delay	AUI	tCD	–	25	200	ns
	TP	tCD	–	425	550	ns
Receive data setup from RCLK	Mode 1	tRDS	60	70	–	ns
	Modes 2, 3 and 4	tRDS	30	45	–	ns
Receive data hold from RCLK	Mode 1	tRDH	10	20	–	ns
	Modes 2, 3 and 4	tRDH	30	45	–	ns
RCLK shut off delay from CD assert (LXT907A only; Mode 3)		tSWS	–	±100	–	ns

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.

Table 12: RCLK/End-of-Frame Timing (Over Recommended Range)

Parameter	Type	Sym	Mode 1	Mode 2	Mode 3	Mode 4	Units
RCLK after CD off	Min	tRC	5	1	27	5	BT
Rcv data throughput delay	Max	tRD	400	375	375	375	ns
CD turn off delay[2]	Max	tCDOFF	500	475	475	475	ns
Receive block out after TEN off	Typ[1]	tIFG	5	50	–	–	BT
RCLK switching delay after CD off (LXT907A only; Mode 3)	Typ[1]	tSWE	–	–	120(±80)	–	ns

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.
2. CD turn-off delay measured from middle of last bit; timing specification is unaffected by the value of the last bit.

Table 13: Transmit Timing (Over Recommended Range)

Parameter	Symbol	Minimum	Typical [1]	Maximum	Units
TEN setup from TCLK	tEHCH	22	–	–	ns
TXD setup from TCLK	tDSCH	22	–	–	ns
TEN hold after TCLK	tCHEL	5	–	–	ns
TXD hold after TCLK	tCHDU	5	–	–	ns
Transmit start-up delay - AUI	tSTUD	–	220	450	ns
Transmit start-up delay - TP	tSTUD	–	430	450	ns
Transmit through-put delay - AUI	tTPD	–	–	300	ns
Transmit through-put delay - TP	tTPD	–	300	350	ns

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.

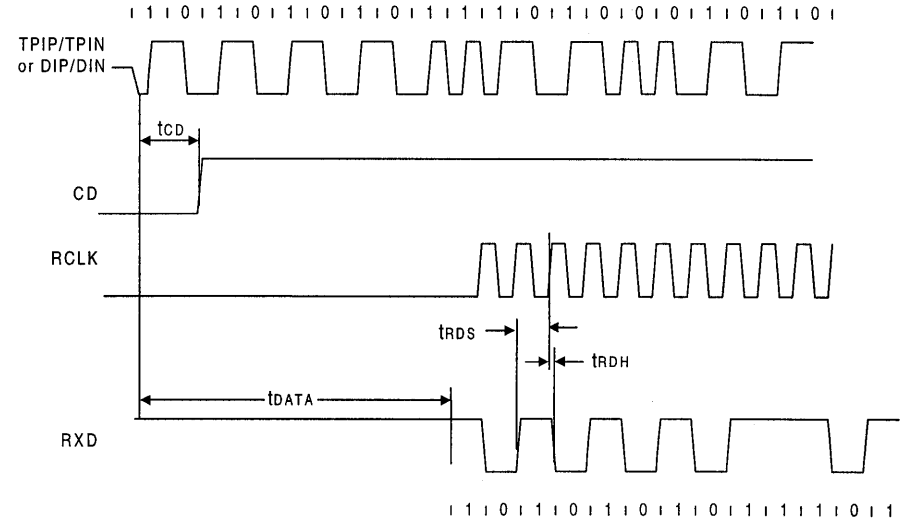
Table 14: Collision, COL/CI Output and Loopback Timing (Over Recommended Range)

Parameter	Symbol	Minimum	Typical[1]	Maximum	Units
COL turn-on delay	tCOLD	–	40	500	ns
COL turn-off delay	tCOLOFF	–	420	500	ns
COL (SQE) Delay after TEN off	tSQED	0.65	1.2	1.6	µs
COL (SQE) Pulse Duration	tSQEP	500	1000	1500	ns
LBK setup from TEN	tKHEH	10	25	–	ns
LBK hold after TEN	tKHEL	10	0	–	ns

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.

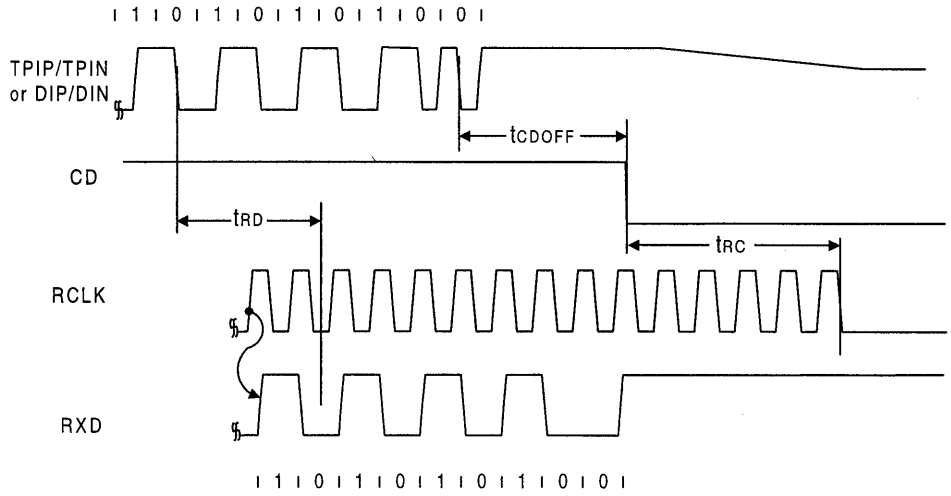
Timing Diagrams for Mode 1 (MD1 = Low, MD0 = Low) Figures 16 through 21

Figure 16: Mode 1 RCLK/Start-of-Frame Timing



NOTE:
1. RXD changes 25 ns after the rising edge of RCLK.

Figure 17: Mode 1 RCLK/End-of-Frame Timing



NOTE:
1. RXD changes 25 ns after the rising edge of RCLK.

Figure 18: Mode 1 Transmit Timing

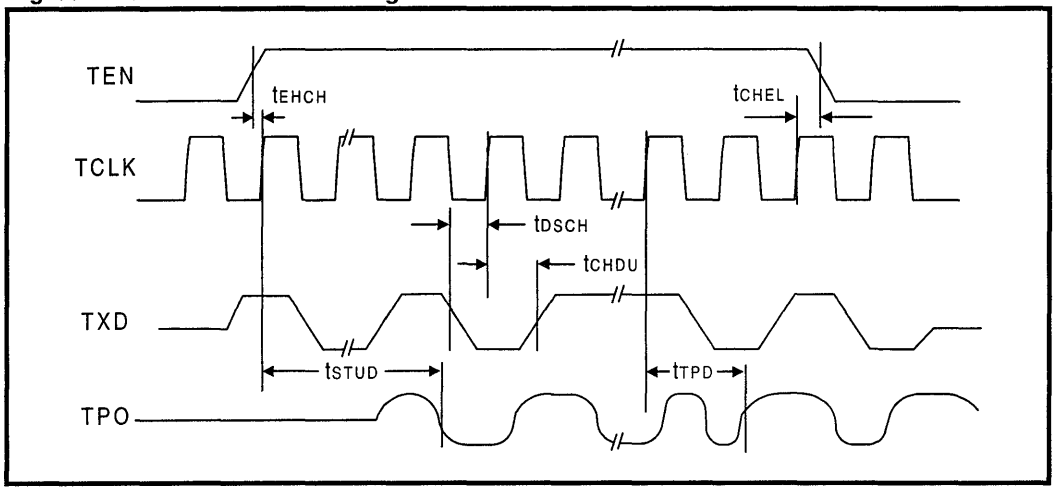


Figure 19: Mode 1 Collision Detect Timing

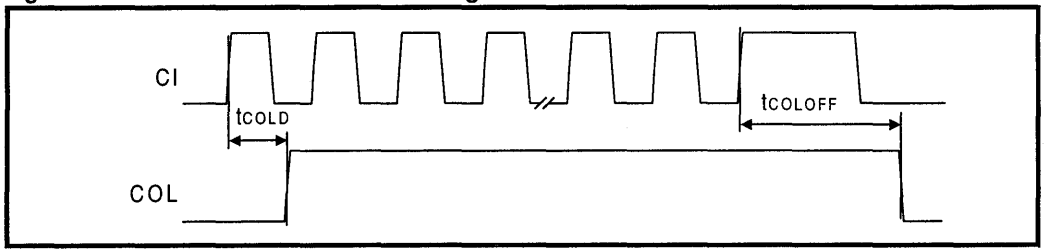


Figure 20: Mode 1 COL/CI Output Timing

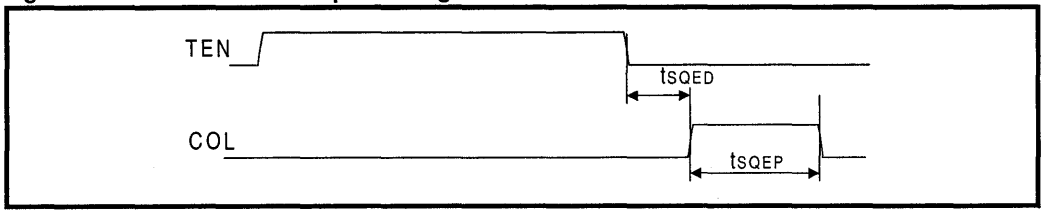
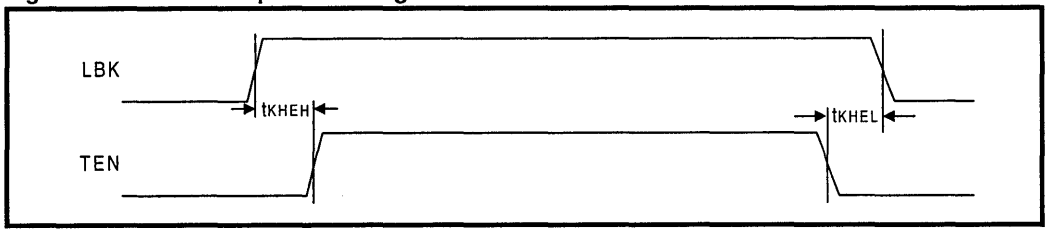
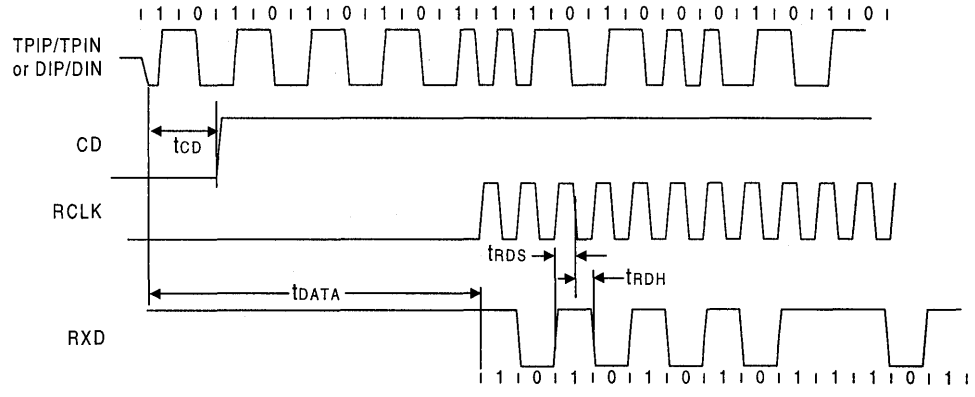


Figure 21: Mode 1 Loopback Timing



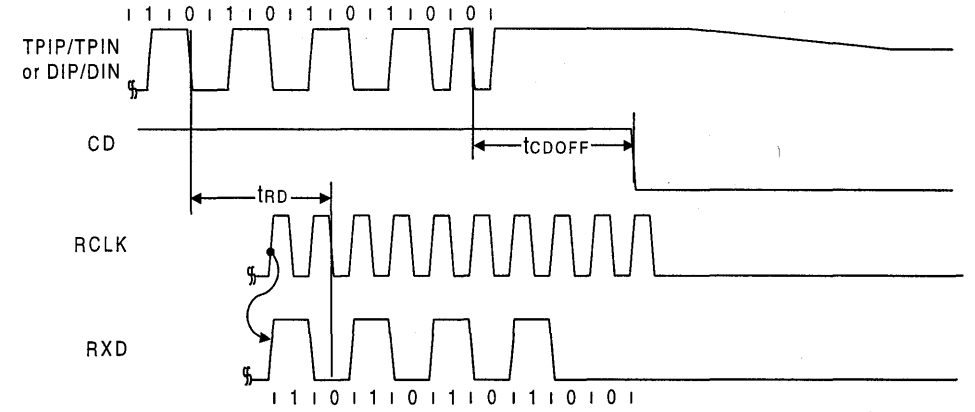
Timing Diagrams for Mode 2 (MD1=Low, MD0=High) Figures 22 through 27

Figure 22: Mode 2 RCLK/Start-of-Frame Timing



NOTE:
1. RXD changes at the rising edge of RCLK. The controller is sampled at the falling edge.

Figure 23: Mode 2 RCLK/End-of-Frame Timing



NOTE:
1. RXD changes at the rising edge of RCLK. The controller is sampled at the falling edge.

Figure 24: Mode 2 Transmit Timing

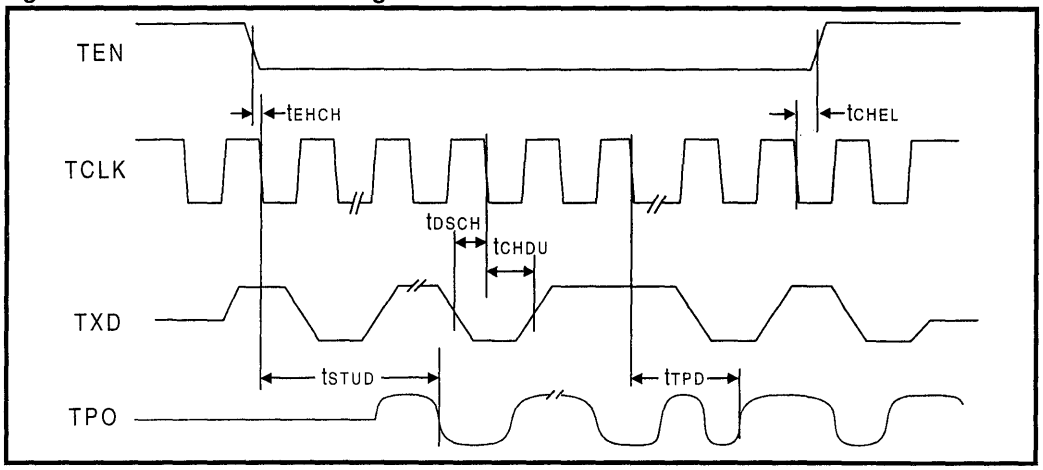


Figure 25: Mode 2 Collision Detect Timing

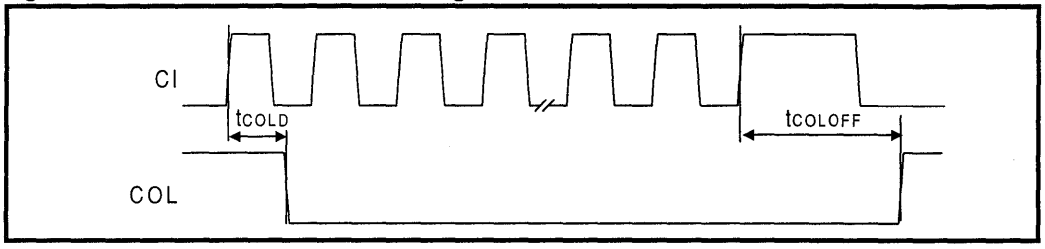
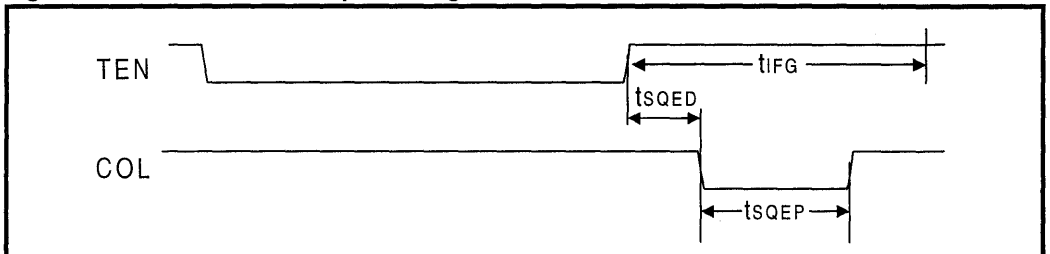
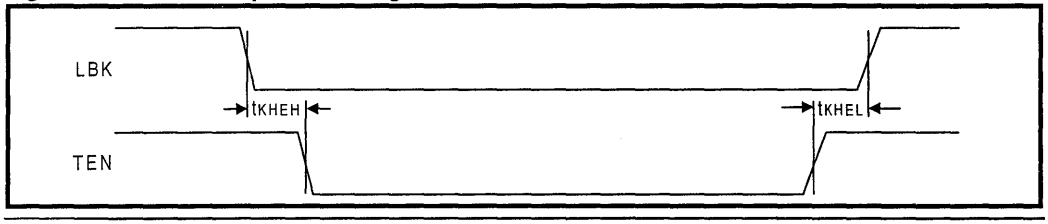


Figure 26: Mode 2 COL/CI Output Timing



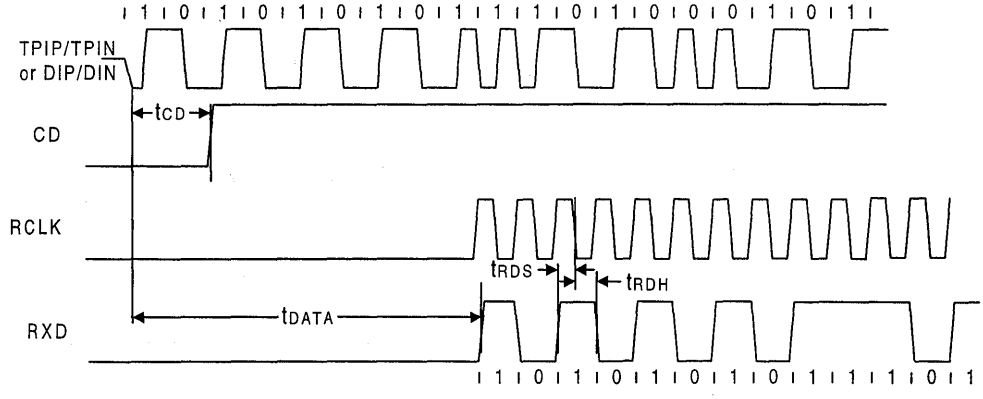
1. The CD output is disabled for a maximum of 55 bit times after TEN turns off.

Figure 27: Mode 2 Loopback Timing



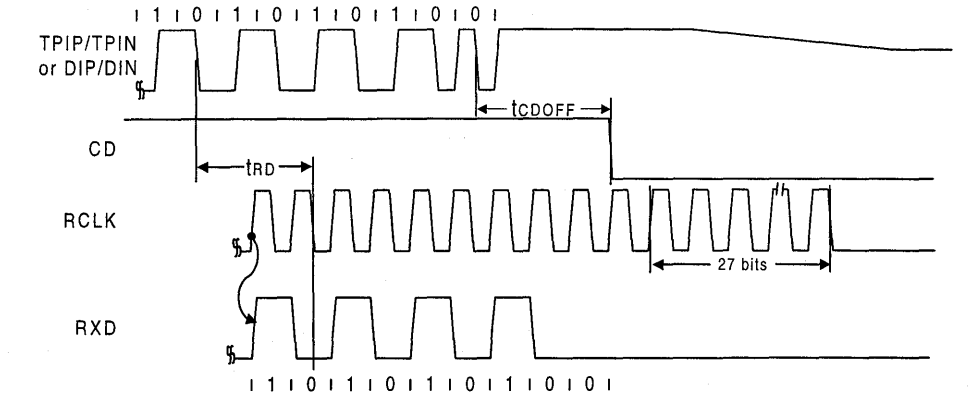
Timing Diagrams for Mode 3 (MD1 = High, MD0 = Low) Figures 28 through 35

Figure 28: Mode 3 RCLK/Start-of-Frame Timing (LXT901A)



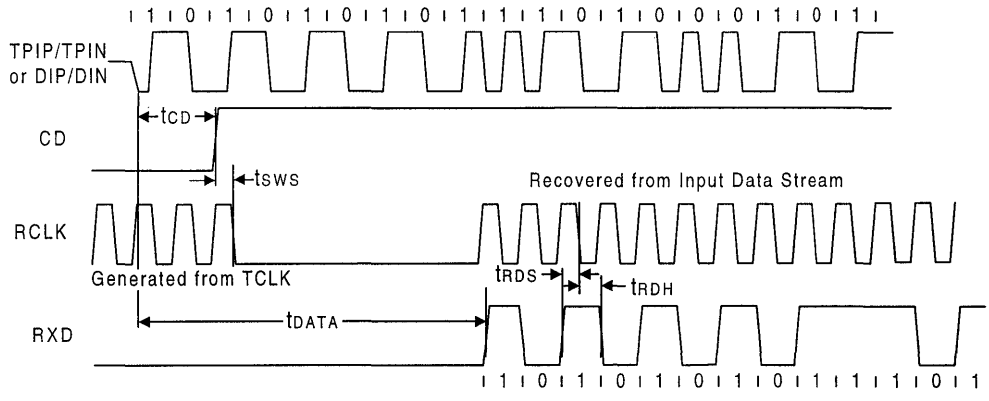
Note:
1. RXD changes at the rising edge of RCLK. The controller is sampled at the falling edge.

Figure 29: Mode 3 RCLK/End-of-Frame Timing (LXT901A)



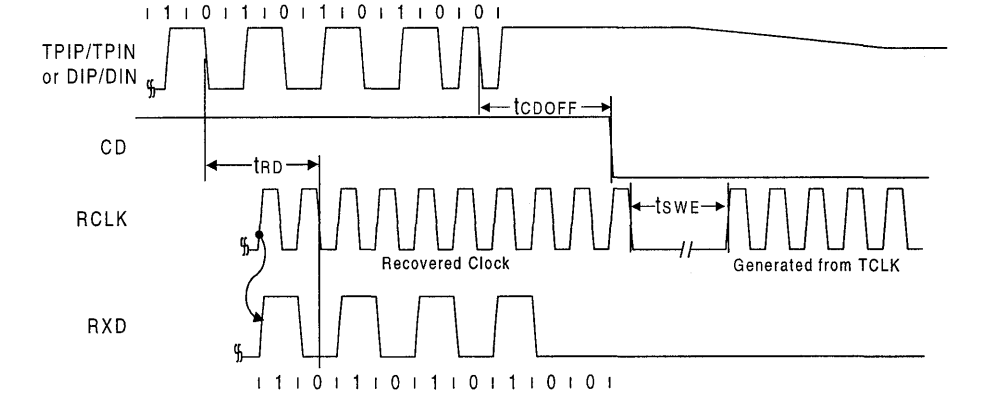
Note:
1. RXD changes at the rising edge of RCLK. The controller is sampled at the falling edge.

Figure 30: Mode 3 RCLK/Start-of-Frame Timing (LXT907A)



Note:
1. RXD changes at the rising edge of RCLK. The controller is sampled at the falling edge.

Figure 31: Mode 3 RCLK/End-of-Frame Timing (LXT907A)



Note:
1. RXD changes at the rising edge of RCLK. The controller is sampled at the falling edge.

Figure 32: Mode 3 Transmit Timing

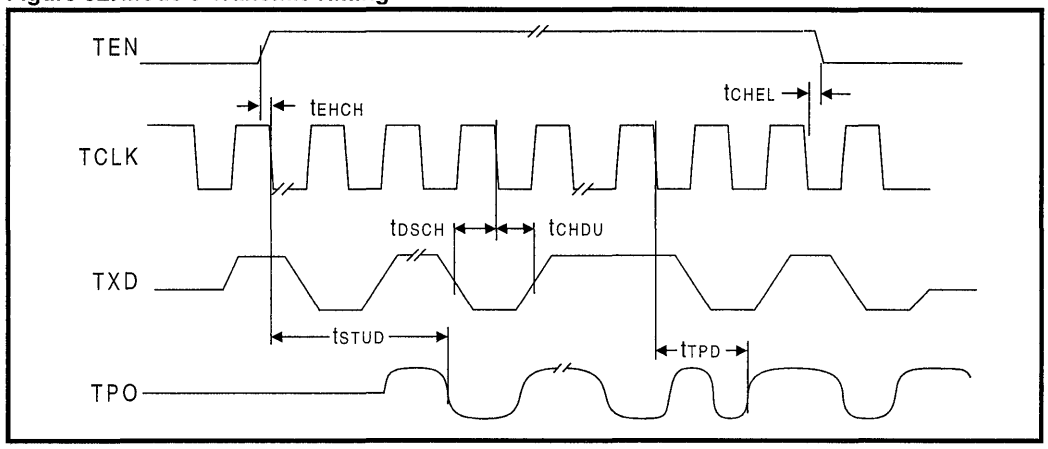


Figure 33: Mode 3 Collision Detect Timing

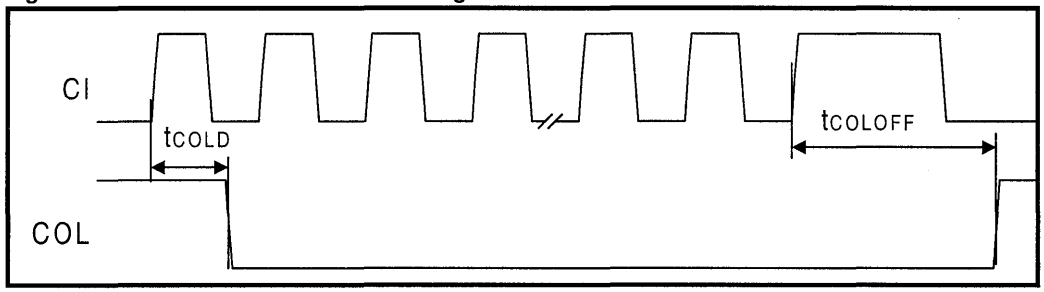
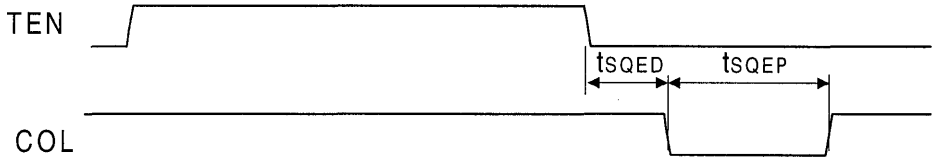
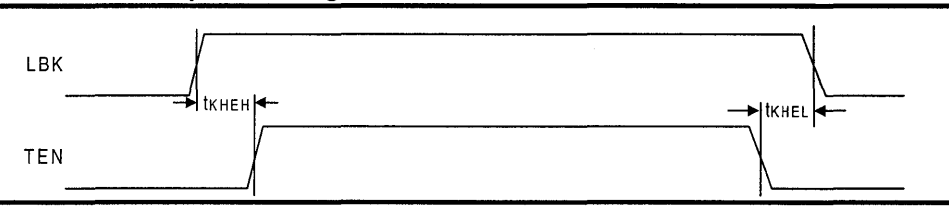


Figure 34: Mode 3 COL/CI Output Timing



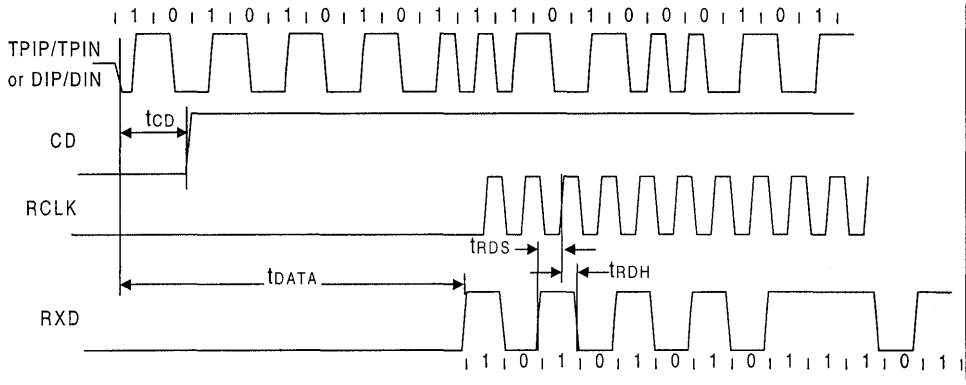
Note:
1. The CD output is disabled for a maximum of 55 bit times after TEN turns off.

Figure 35: Mode 3 Loopback Timing



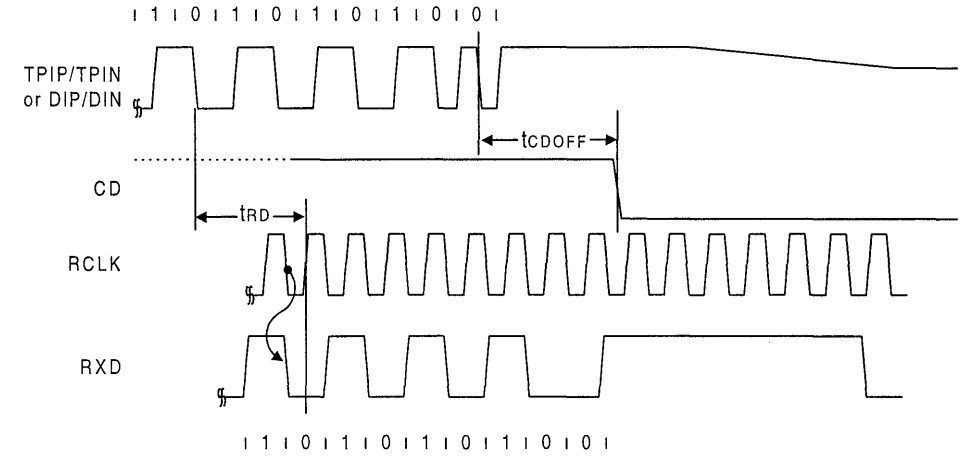
Timing Diagrams for Mode 4 (MD1 = High, MD0 = High) Figures 36 through 41

Figure 36: Mode 4 RCLK/Start-of-Frame Timing



Note:
1. RXD changes at the falling edge of RCLK. The controller is sampled at the rising edge.

Figure 37: Mode 4 RCLK/End-of-Frame Timing



Note:
1. RXD changes at the falling edge of RCLK. The controller is sampled at the rising edge.

Figure 38: Mode 4 Transmit Timing

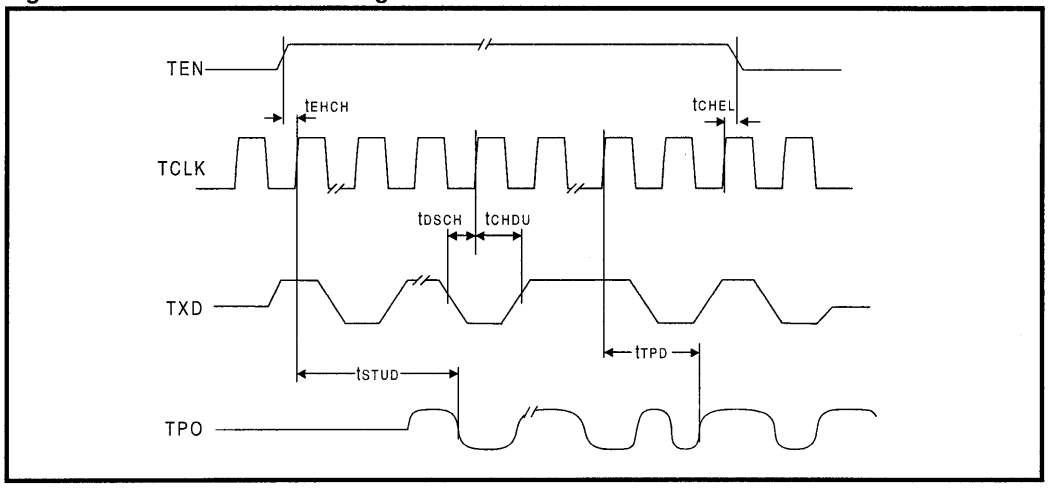


Figure 39: Mode 4 Collision Detect Timing

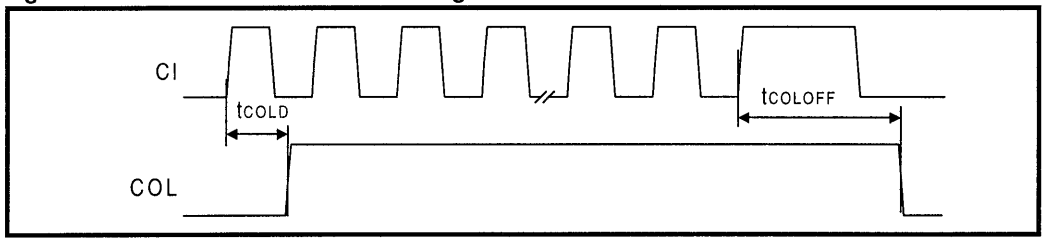


Figure 40: Mode 4 COL/CI Output Timing

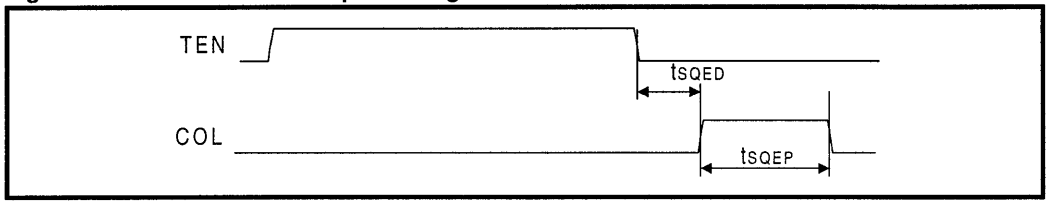
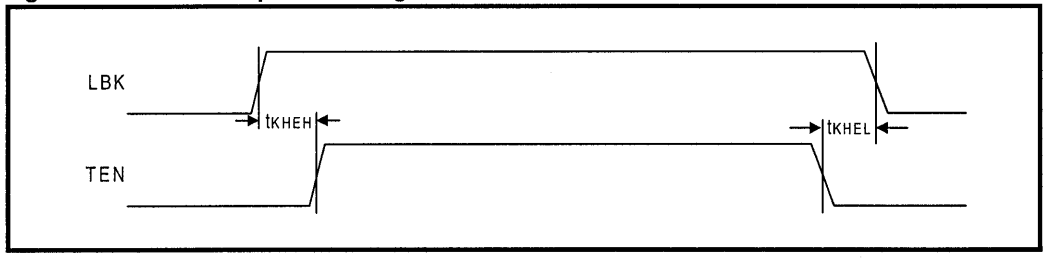


Figure 41: Mode 4 Loopback Timing



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NOTES

DATA SHEET

APRIL 1997
Revision 2.1

LXT902

Ethernet Twisted-Pair Media Attachment Unit

General Description

The LXT902 twisted-pair Media Attachment Unit (TP-MAU) is designed to allow Ethernet connections to use the existing twisted-pair wiring plant through an Ethernet Attachment Unit Interface (AUI). The LXT902 provides the electrical interface between the AUI and the twisted-pair wire.

LXT902 functions include level-shifted data pass-through from one transmission media to another, collision detection, Signal Quality Error (SQE) testing and automatic correction of polarity reversal on the twisted-pair input. It also includes LED drivers for transmit, receive, jabber, collision, reversed polarity detect and link functions. The LXT902 is an advanced CMOS device and requires only a single 5-volt power supply.

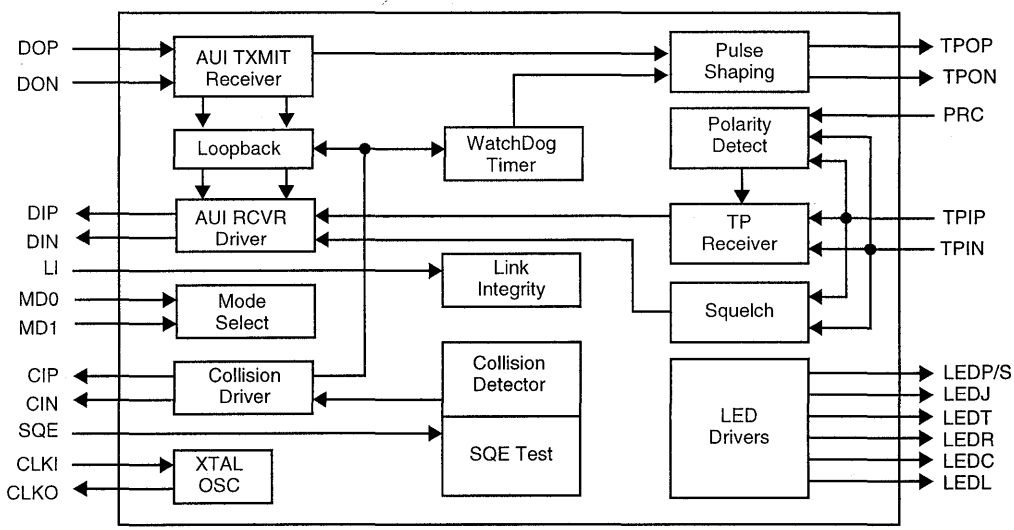
Applications

- Computer/workstation interface boards
- LAN repeater
- External 10BASE-T transceiver (MAU)

Features

- Meets or exceeds IEEE 802.3 standards for AUI and 10BASE-T interface
- Direct interface to AUI and RJ45 connectors
- Automatic AUI/RJ45 selection
- Internal pre-distortion generation
- Internal common mode voltage generation
- Jabber function
- Selectable link test, SQE test disable
- Twisted-pair receive polarity reverse detection and selectable polarity correction
- LED driver for transmit, receive, jabber, collision, link and reversed polarity indicators or for flashing status indicator
- Single 5 V supply, CMOS technology
- Available in 28-pin DIP or PLCC

LXT902 Block Diagram



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PIN ASSIGNMENTS AND SIGNAL DESCRIPTIONS

Figure 1: LXT902 Pin Assignments

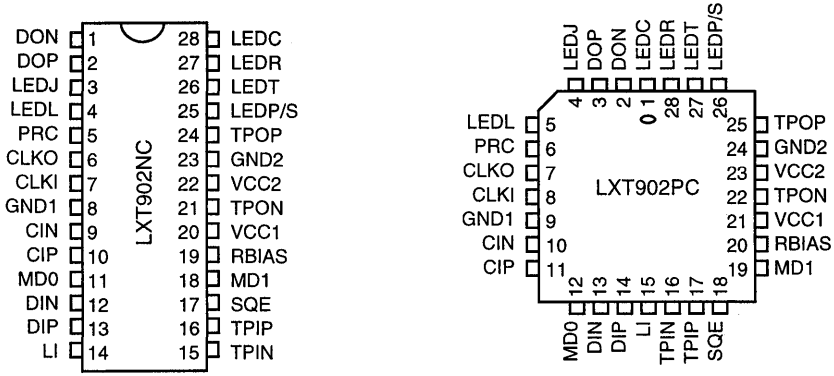


Table 1: LXT902 Signal Descriptions

DIP	PLCC	Symbol	I/O	Description
1 2	2 3	DON DOP	I I	**Data Out Negative and Data Out Positive.** Differential input pair from the AUI transceiver DO circuit.
3	4	LEDJ	I/O	**Jabber LED Driver.** Active Low, open drain driver for the Jabber indicator LED. Output goes active when watchdog timer begins jab, and stays active until end of the unjab wait period (491 - 525 ms). When tied to ground, causes LEDP/S to act as a multi-function blinking status indicator.
4	5	LEDL	O	**Link LED Driver.** Active Low, open drain driver for the Link indicator LED. Output is active except during Link Fail or when Link Integrity Test is disabled.
5	6	PRC	I/O	**Polarity Reverse Correction.** . The LXT902 automatically corrects reversed polarity at TPI when PRC is tied High. In Test mode, this pin is a 10 MHz output.
6 7	7 8	CLKO CLKI	O I	**Crystal Oscillator.** The LXT902 requires either a 20 MHz crystal (or ceramic resonator) connected across these pins, or a 20 MHz external clock applied at CLKI with CLKO left unconnected.
8	9	GND1	–	**Ground 1.** Ground
9 10	10 11	CIN CIP	O O	**Collision Negative and Collision Positive.** Differential driver output pair tied to the collision presence pair of the Ethernet transceiver AUI cable. The collision presence signal is a 10 MHz square wave. This output is activated when a collision is detected on the network, during self-test by the SQE sequence, or after the watchdog timer has expired to indicate the transmit wire pair has been disabled.

Table 1: LXT902 Signal Descriptions – continued

DIP	PLCC	Symbol	I/O	Description
11	12	MD0	I	**Mode Select 0.** Selects operating modes in conjunction with MD1. See Table 2 for mode select options.
12 13	13 14	DIN DIP	O O	**Data In Negative and Data In Positive.** Differential driver pair connected to the AUI transceiver DI circuit.
14	15	LI	I	**Link Integrity Test Enable.** Link integrity testing is enabled when this pin is tied High. With link test enabled, the LXT902 sends the link integrity signal in the absence of transmit traffic. It also recognizes received link test pulses, indicating the receive wire pair is present in the absence of transmit traffic.
15 16	16 17	TPIN TPIP	I I	**Twisted-Pair Receive Inputs.** Differential receive inputs from the twisted-pair input filter.
17	18	SQE	I/O	**Signal Quality Error Test Enable.** SQE is enabled when this pin is tied High. When enabled, the LXT902 sends the signal quality error test sequence to the CI of the AUI cable after every successful transmission to the media. In Test mode, SQE becomes a 20 MHz output.
18	19	MD1	I	**Mode Select 1.** Selects operating modes in conjunction with MD0. (See Table 2.) MD1 clock input between 2.0 and 2.5 MHz enables Test mode.
19	20	RBIAS	–	**Resistor Bias Control.** Bias control pin for the operating circuit. Bias set from external resistor to ground. External resistor value = 12.4 kΩ (± 1%).
20	21	VCC1	I	**Power Supply 1.** +5 V power supply.
21 24	22 25	TPON TPOP	O O	**Twisted-Pair Transmit Outputs.** Transmit drivers to the twisted-pair output filter. The output is Manchester encoded and pre-distorted to meet the 10BASE-T template.
22	23	VCC2	I	**Power Supply 2.** +5 V power supply.
23	24	GND2	–	**Ground 2.** Ground.
25	26	LEDP/S	O	**Polarity/Status LED Driver.** Active Low, open drain LED driver. In normal mode, LEDP/S is active when reversed polarity is detected. If LEDJ is tied to ground, LEDP/S indicates multiple status conditions as shown in Figure 11: On solid = Normal, 1 Blink = Link Down, 2 Blinks = Jabber, 5 Blinks = Polarity Reversed.
26	27	LEDT	O	**Transmit LED Driver.** Active Low, open drain driver for the Transmit indicator LED. Output is active during transmit.
27	28	LEDR	O	**Receive LED Driver.** Active Low, open drain driver for the Receive indicator LED. Output is active during receive.
28	1	LEDC	O	**Collision LED Driver.** Active Low, open drain driver for the Collision indicator LED. Output is active when a collision occurs.

FUNCTIONAL DESCRIPTION

Introduction

The LXT902 Media Attachment Unit (MAU) interfaces the Attachment Unit Interface (AUI) to the unshielded twisted-pair cables, transferring data in both directions between the two. The AUI side of the interface comprises three circuits: Data Output (DO), Data Input (DI) and Control Interface (CI). The twisted-pair network side of the interface comprises two circuits: Twisted-Pair Input (TPI) and Twisted-Pair Output (TPO). In addition to these five basic circuits, the LXT902 also contains: crystal oscillator circuitry, separate power and ground pins for analog and digital circuits, mode selection logic (see Table 2) and six LED drivers for status indications.

Table 2: Mode Select Options

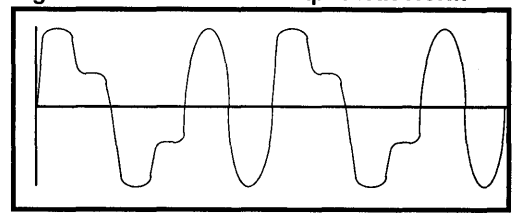
MD1	MD0	Mode
Low	Low	10BASE-T compliant MAU
Low	High	Reduced squelch level
High	Low	Half current AUI driver
High	High	DO, DI & CI ports disabled
High	Clock	Test Mode, Jabber on
Low	Clock	Test mode, Jabber disabled

Functions are defined from the AUI side of the interface. The LXT902 Transmit function refers to data transmitted by the Data Terminal Equipment (DTE) through the AUI and MAU to the twisted-pair network. The LXT902 Receive function refers to data received by the DTE through the MAU and AUI from the twisted-pair network. In addition to basic transmit and receive functions, the LXT902 performs all required functions defined by the IEEE 802.3 10BASE-T MAU specification such as collision detection, link integrity testing, Signal Quality Error (SQE), jabber control and loopback.

Transmit Function

The LXT902 transfers Manchester encoded data from the AUI port of the DTE (the DO circuit) to the twisted-pair network (the TPO circuit). The output signal on TPON and TPOP is pre-distorted to meet the 10 BASE-T jitter template, and filtered to meet FCC requirements. The output waveform (after the transmit filter) is shown in Figure 2. If the differential inputs at the DO circuit fall below 75% of the threshold level for 8 bit times (typical), the LXT902 transmit function will enter the idle state. During idle periods, the LXT902 transmits link integrity test pulses on the TPO circuit.

Figure 2: LXT902 TPO Output Waveform



Receive Function

The LXT902 receive function transfers serial data from the twisted-pair network (the TPI circuit) to the DTE (over the DI circuit of the AUI). An internal squelch function discriminates noise from link test pulses and valid data streams. Only valid data streams activate the receive function. If the differential inputs at the TPI circuit fall below 75% of the threshold level (unsquelched) for 8 bit times (typical), the LXT902 receive function will enter the idle state. The TPI threshold can be reduced by approximately 3 dB to allow for longer loops in low-noise environments. The reduced threshold is selected when MD1 = Low and MD0 = High.

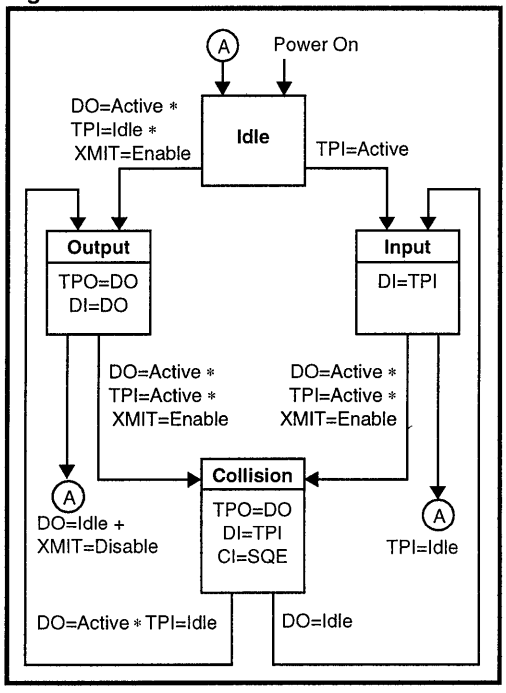
Polarity Reverse Function

The LXT902 polarity reverse function uses both link pulses and end-of-frame data to determine polarity of the received signal. A reversed polarity condition is detected when eight opposite receive link pulses are detected without receipt of a link pulse with the expected polarity. Reversed polarity is also detected if four frames are received with a reversed start-of-idle. Whenever polarity is reversed, these two counters are reset to zero. If the LXT902 enters the link fail state, and no data or link pulses are received within 96 to 128 ms, the polarity is reset to the default non-flipped condition. If Link Integrity is disabled, polarity detection is based only on received data pulses.

Collision Detection Function

The collision detection function operates on the twisted-pair side of the interface. A collision is defined as the simultaneous presence of valid signals on both the TPI circuit and the TPO circuit. The LXT902 reports collisions to the AUI by sending a 10 MHz signal over the CI circuit. The collision report signal is output no more than 9 bit times (BT) after the chip detects a collision. If the TPI circuit becomes active while there is activity on the TPO circuit, the TPI data is passed to the DTE over the DI circuit, disabling the loopback. Figure 3 is a state diagram of the LXT902 collision detection function (refer to IEEE 802.3 10BASE-T specification).

Figure 3: Collision Detection Function



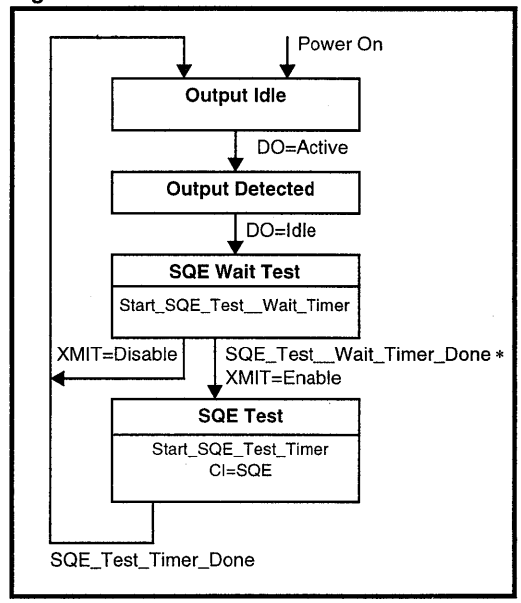
Loopback Function

The LXT902 loopback function operates in conjunction with the transmit function. Data transmitted by the DTE is internally looped back within the LXT902 from the DO pins to the DI pins and returned to the DTE. The loopback function is disabled when a data collision occurs, clearing the DI circuit for the TPI data. Loopback is also disabled during link fail and jabber states.

SQE Test Function

Figure 4 is a state diagram of the SQE Test function. The SQE test function is enabled when the SQE pin is tied High. When enabled, the SQE test sequence is transmitted to the controller after every successful transmission on the 10BASE-T network. When a successful transmission is completed, the LXT902 transmits the SQE signal to the AUI over the CI circuit for 10 BT ± 5 BT. The SQE function can be disabled for hub applications by tying the SQE pin to ground.

Figure 4: SQE Function



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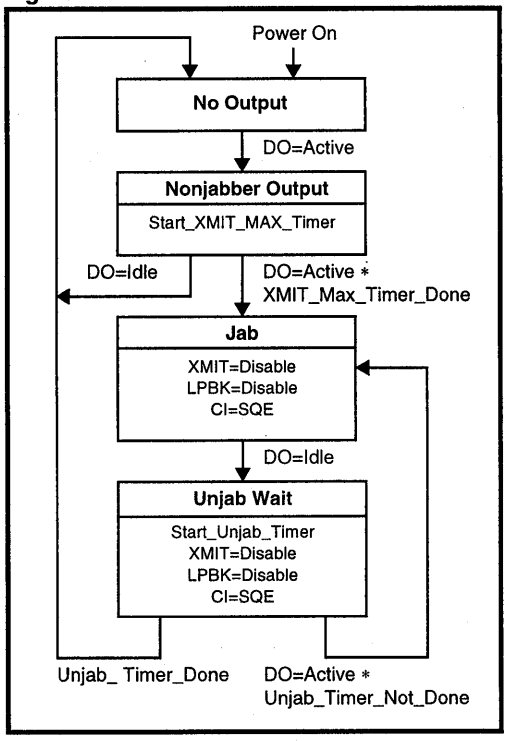
Jabber Control Function

Figure 5 is a state diagram of the LXT902 Jabber control function. The LXT902 on-chip watchdog timer prevents the DTE from locking into a continuous transmit mode. When a transmission exceeds the time limit, the Watchdog timer disables the transmit and loopback functions, and sends the SQE signal to the DTE over the CI circuit. Once the LXT902 is in the jabber state, the DO circuit must remain idle for a period of 491 to 525 ms before it will exit the jabber state.

Figure 5: Jabber Control Function



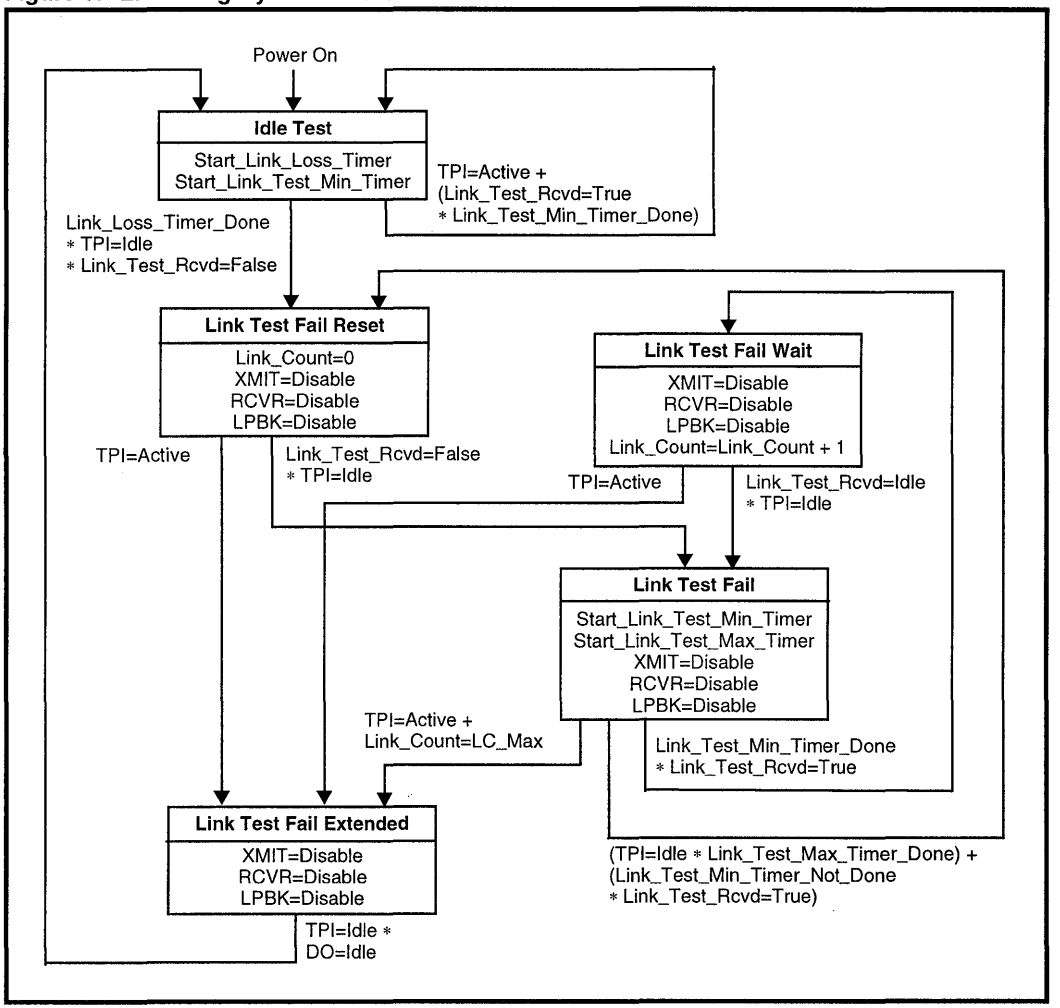
Link Integrity Test Function

Figure 6 is a state diagram of the LXT902 Link Integrity Test Function. The Link Integrity Test is used to determine the status of the receive side twisted-pair cable. The link integrity test is enabled when the LI pin is tied High. When enabled, the receiver recognizes link integrity pulses which are transmitted in the absence of receive traffic. If no serial data stream or link integrity pulses are detected within 50 - 150 ms, the chip enters a link fail state and disables the transmit and loopback functions. The LXT902 ignores any link integrity pulse with interval less than 2 - 7 ms. The LXT902 will remain in the link fail state until it detects either a serial data packet or two or more link integrity pulses.

Test Mode

The LXT902 Test mode is selected when a 2 - 2.5 MHz clock is input on the MD0 mode select pin. Test mode sets the internal counter chains to run at 1024 times their normal speed. The maximum transmit time, unjab time, Link Integrity timing and LED timing are reduced by a factor of 1024. During test operation, 10 MHz and 20 MHz signals are output on the PRC and SQE pins, respectively. When Test mode is selected, the SQE function cannot be disabled. In Test mode the PRC function can be disabled by the LI pin. Jabber can be disabled by setting MD1 Low.

Figure 6: Link Integrity Test Function



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APPLICATION INFORMATION

External MAU

Figure 7 shows the LXT902 in a typical external MAU application, interfacing between an AUI and the RJ45 connectors of the twisted-pair network. A 20 MHz crystal (or ceramic resonator) connected across CLKI and CLKO provides the required clock signal. Transmit and receive filters are required in the TPO and TPI circuits. Details of the transmit and receive filters are shown in Figures 8 and 9, respectively. (Differential filters are also recommended.)

Internal MAU

Figure 10 shows an internal MAU application which takes advantage of the LXT902's unique AUI/10BASE-T switching feature to select either the D-connector (AUI) or the RJ45 connector (10BASE-T). No termination resistors are used on the LXT902 side of the AUI interface to prevent impedance mismatch with the drop cable. The half current drive mode is used to maintain the same voltage levels in the absence of termination resistors. This application uses capacitive coupling instead of transformer coupling. MD1 is tied High so MD0 functions as the mode control switch.

When MD0 is Low, the half current drive mode is selected. When MD0 is High, the LXT902 is effectively removed from the circuit. The 902 AUI ports (DO, DI and CI) are disabled isolating the LXT902 from the AUI. The LXT902 DI and CI ports go to a high impedance state and the DO port is ignored. To implement an auto-select function, LEDL can be tied to MD0. This activates the 902/AUI interface when the TP link is active (data or link integrity pulses) and disables it when the link is inactive.

Figure 7: Typical External MAU Application

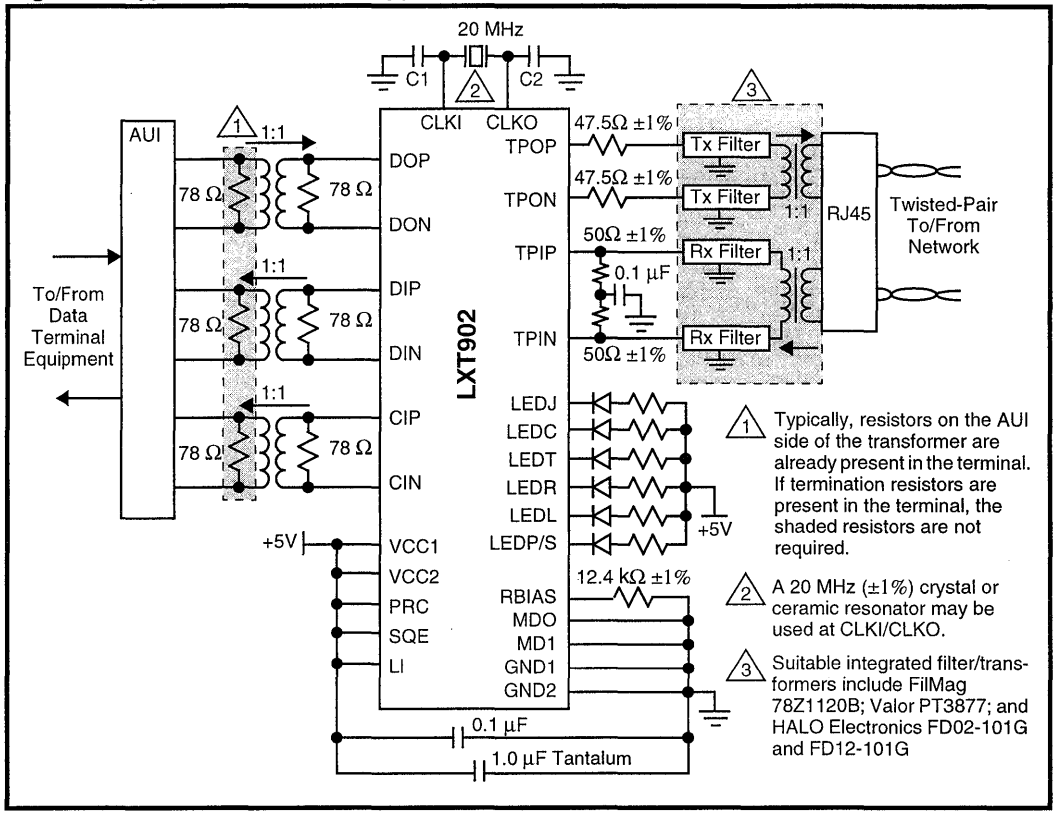


Figure 8: Typical Transmit Filter

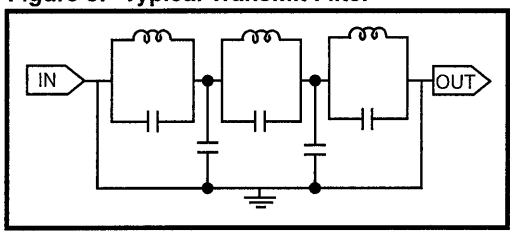


Figure 9: Typical Receive Filter

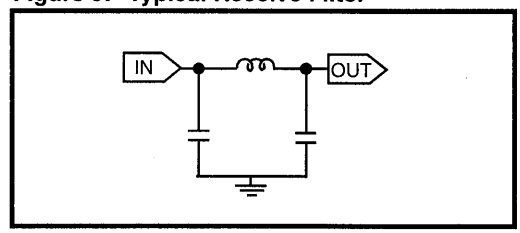
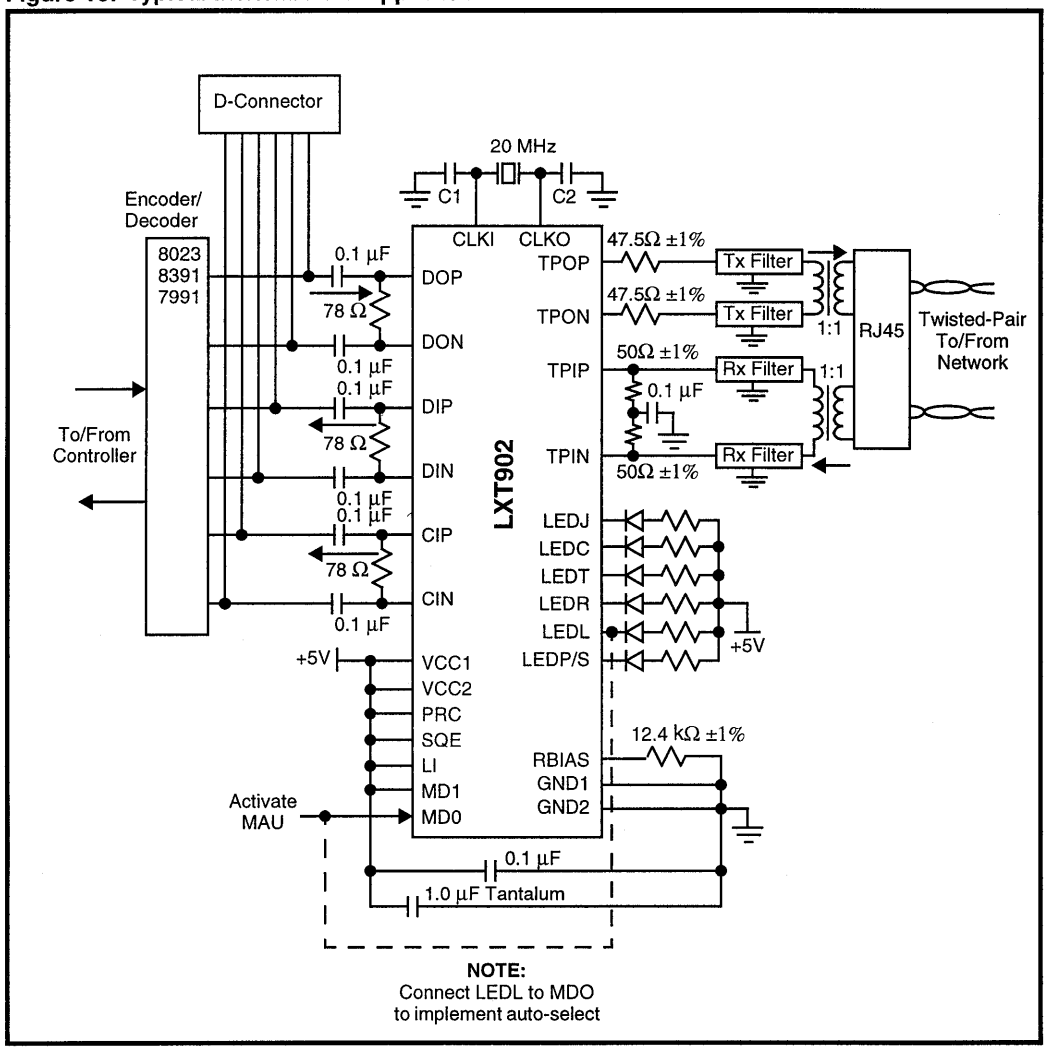


Figure 10: Typical Internal MAU Application



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TEST SPECIFICATIONS

NOTE

The minimum and maximum values in Tables 3 through 9 and Figure 11 represent the performance specifications of the LXT902 and are guaranteed by test, except where noted by design.

Table 3: Absolute Maximum Values

Parameter	Symbol	Min	Max	Units
Supply voltage	VCC	-0.3	6	V
Ambient operating temperature	TA	0	70	°C
Storage temperature	TSTG	-65	+150	°C

CAUTION

Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 4: Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Recommended supply voltage[1,2]	VCC	4.75	5.0	5.25	V	–
Recommended operating temperature	TOP	0	–	70	°C	–

2. Voltages with respect to ground unless otherwise specified.
3. Maximum voltage differential between VCC1 and VCC2 must not exceed 0.3 V.

Table 5: I/O Electrical Characteristics (Over Recommended Range)

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Input Low voltage[2]	VIL	–	–	0.8	V	–
Input High voltage[2]	VIH	2.0	–	–	V	–
Output Low voltage (Open drain LED driver)	VOLL	–	–	0.7	V	IOLL = 10 mA
Supply Current (VCC1=VCC2=5.25 V)	ICC	–	60	70	mA	Line Idle
		–	125	140	mA	Line Active, transmitting all ones
Input Leakage Current[3]	ILL	–	±1	±10	µA	Input between VCC and GND
Three state leakage current (high Z)	ITS	–	±1	±10	µA	Output between VCC and GND

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. MD0, MD1, SQE, PRC, and LI pins. MD0 clock (test mode) must be CMOS level input.
3. Not including TPIN, TPIP, DOP, or DON.

Table 6: AUI Electrical Characteristics (Over Recommended Range)

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Input Low current	IIL	–	–	-700	µA	–
Input High current	IIH	–	–	500	µA	–
Differential output voltage	VOD	±550	–	±1200	mV	–
Differential squelch threshold	VDS	–	220	–	mV	–
Receive input impedance	RZ	–	20	–	kΩ	Between DOP and DON

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 7: Transmit Characteristics (Over Recommended Range)

Parameter	Sym	Minimum	Typical[1]	Maximum	Units	Test Conditions
Transmit output impedance	ZOUT	–	5	–	Ω	–
Transmit timing jitter addition[2]	–	–	–	±8	ns	After Tx filter, 0 line length
Transmit timing jitter addition[2]	–	–	–	±3.5	ns	After Tx filter and line model specified by IEEE 802.3 for 10BASE-T

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.
2. Parameter is guaranteed by design; not subject to production testing.

Table 8: Receive Characteristics (Over Recommended Range)

Parameter	Sym	Minimum	Typical[1]	Maximum	Units	Test Conditions
Receive input impedance	ZIN	–	20	–	kΩ	Between TPIP/TPIN
Differential squelch threshold	VDS	–	420	–	mV	–
Reduced squelch threshold	VDSR	–	300	–	mV	–
Receive timing jitter addition[2]	–	–	–	1.5	ns	–

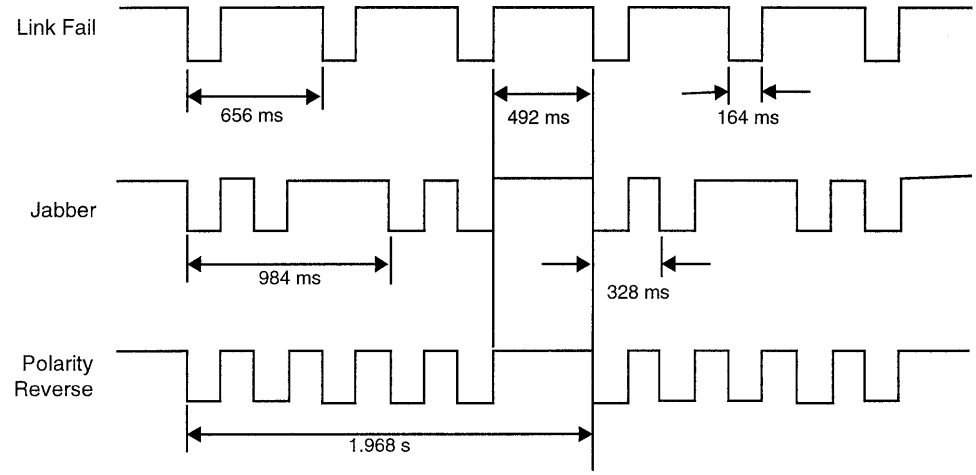
1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.
2. Parameter is guaranteed by design; not subject to production testing.

Table 9: Switching Characteristics (Over Recommended Range)

	Parameter	Min	Typ[1]	Max	Units
Jabber Timing	Maximum transmit time [2]	98.5	–	131	ms
	Unjab time [2]	491	–	525	ms
	Time from Jabber to CS0 on CIP/CIN [3]	0	–	900	ns
Link Integrity Timing	Time link loss [2]	65	–	66	ms
	Time between Link Integrity Pulses [2]	9	–	11	ms
	Interval for valid receive Link Integrity Pulses [2]	4.1	–	65	ms
Collision Timing	Simultaneous TPI/TPO to CSO state on CIN/CIP	0	–	900	ns
	DO loopback to TPI on DI [3]	300	–	900	ns
	CS0 state delay after TPI/DO idle	–	–	900	ns
	CS0 High pulse width	40	–	60	ns
	CS0 Low pulse width	40	–	60	ns
	CS0 frequency	–	10	–	MHz
SQE Timing	SQE signal duration	500	–	1500	ns
	Delay after last positive transition of DO	0.6	–	1.6	µs
LED Timing	LEDC, LEDT, LEDR on time [2]	100	–	–	ms
	LEDP/S on time [2] (See Figure 11)	–	164	–	ms
	LEDP/S period [2] (See Figure 11)	–	328	–	ms
General	Receive start-up delay	0	–	500	ns
	Transmit start-up delay	0	–	200	ns
	Loopback start-up delay	0	–	500	ns

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Switching times reduced by a factor of 1024 during Test mode.
3. Parameter is guaranteed by design; not subject to production testing.

Figure 11: LEDP/S Status Indication Timing



NOTE:

1. LEDP/S status indications are shown in order of priority, i.e., Link Fail indication supersedes Jabber indication which supersedes Polarity Reverse (when PRC = 1). Reversed polarity conditions supersede Link Fail conditions when PRC = 0 (Polarity Correction Disabled). At the LEDL indicator, reversed polarity conditions are reported as Link Fail when PRC = 0. This allows the user to distinguish between actual link failure and apparent link failure due to polarity reversal.

NOTES

DATA SHEET

LXT904

APRIL 1997
Revision 1.2

Ethernet Interface Adapter with EnDec and AUI

General Description

The LXT904 Ethernet Interface Adapter is designed for IEEE 802.3 applications. It provides all the active circuitry to adapt most standard 802.3 controllers to the Attachment Unit Interface (AUI). The LXT904 is a pin-compatible replacement for the LXT901 in applications that do not require a twisted-pair port. In addition to standard 10 Mbps Ethernet, the LXT904 also supports full-duplex operation at 20 Mbps.

LXT904 functions include Manchester encoding/decoding and AUI driving/receiving. The LXT904 can also be used to drive the AUI drop cable.

The LXT 904 is fabricated using an advanced CMOS process and requires only a single 5-volt power supply.

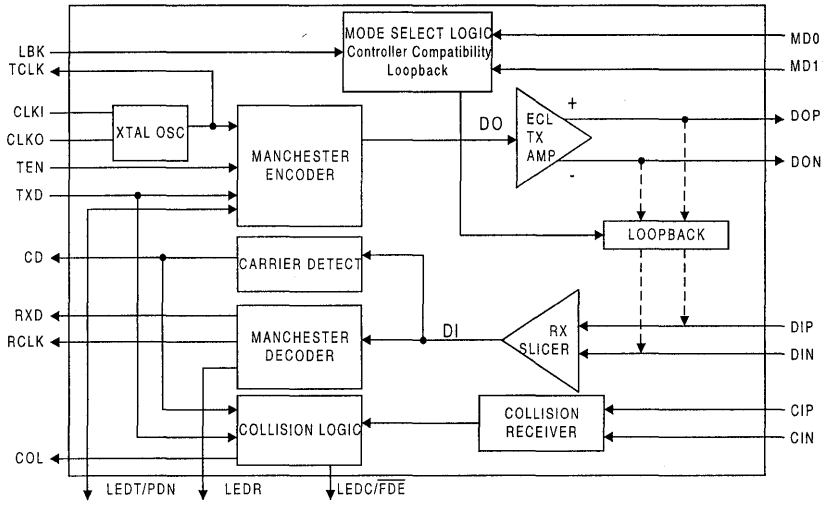
Features

- Integrated Manchester Encoder/Decoder
- AUI Transceiver
- Supports Standard and Full-Duplex Ethernet
- Power Down Mode
- AUI Loopback mode for better testing
- Three LED Drivers
- Available in 44-pin PLCC package

Applications

- Bridges, routers and Ethernet-to-WAN access equipment
- Computer/workstation LAN adapter boards

LXT904 Block Diagram



11

PIN ASSIGNMENTS AND SIGNAL DESCRIPTIONS

Figure 1: LXT904 Pin Assignments

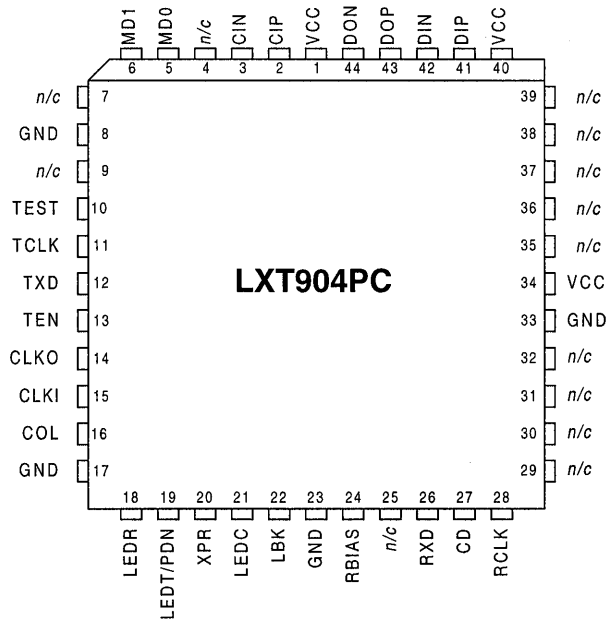


Table 1: LXT904 Pin Descriptions

Pin #	Sym	I/O	Description
1	VCC	I	**Power Input.** + 5 volt power supply input.
2	CIP	I	**AUI Collision Pair.** Differential input pair connected to the AUI transceiver CI circuit.
3	CIN	I	The input is collision signaling or SQE.
4	*n/c*	–	**No connection.** This pin must be left floating.
5	MD0	I	**Mode Select 0; Mode Select 1.** Mode select pins determine controller compatibility mode in accordance with Table 2.
6	MD1	I	
7	*n/c*	–	**No connection.** This pin must be left floating.
8	GND	–	**Ground.** Ground return.
9	*n/c*	–	**No connection.** This pin must be left floating.
10	TEST	I	**Test.** This pin must be tied High.
11	TCLK	O	**Transmit Clock.** A 10 MHz clock output. This clock signal should be directly connected to the transmit clock input of the controller.

Table 1: LXT904 Pin Descriptions – continued

Pin #	Sym	I/O	Description
12	TXD	I	**Transmit Data.** Input signal containing NRZ data to be transmitted on the network. TXD is connected directly to the transmit data output of the controller.
13	TEN	I	**Transmit Enable.** Enables data transmission and starts the watchdog timer. Synchronous to TCLK (see Figures 5, 11, 17 and 23 for details).
14 15	CLKO CLKI	O I	**Crystal Oscillator.** A 20 MHz crystal must be connected across these pins, or a 20 MHz clock applied at CLKI with CLKO left open.
16	COL	O	**Collision Detect.** Output which drives the collision detect input of the controller.
17	GND	–	**Ground.** Ground return.
18	LEDR	O	**Receive LED.** Open drain driver for the receive indicator LED. Output is pulled Low during receive.
19	LEDT/ PDN	O I	**Transmit LED/Power Down.** Open drain driver for the transmit indicator. Output is pulled Low during transmit. If externally tied Low, the LXT904 goes to power down state.
20	XPR	–	**External Pull Up.** Requires an external pull-up resister.
21	LEDC	O	**Collision LED.** Open drain driver for the collision indicator pulls Low during collision.
22	LBK	I	**Loopback.** Enables internal loopback mode. See Figure 8 (Mode 1), Figure 14 (Mode 2), Figure 20 (Mode 3) and Figure 26 (Mode 4) for details.
23	GND	–	**Ground.** Ground Return.
24	RBIAS	I	**Bias Control.** A 12.4 kΩ 1% resistor to ground at this pin controls operating circuit bias.
25	*n/c*	–	**No connection.** This pin must be left floating.
26	RXD	O	**Receive Data.** Output signal connected directly to the receive data input of the controller.
27	CD	O	**Carrier Detect.** An output to notify the controller of activity on the network.
28	RCLK	O	**Receive Clock.** A recovered 10 MHz clock which is synchronous to the received data and connected to the controller receive clock input.
29 30 31 32	*n/c* *n/c* *n/c* *n/c*	– – – –	**No connection.** These pins must be left floating.
33	GND	–	**Ground.** Ground Return.
34	VCC	I	**Power Input .** + 5 volt power supply input.
35 36 37 38 39	*n/c* *n/c* *n/c* *n/c* *n/c*	– – – – –	**No connection.** These pins must be left floating.
40	VCC	I	**Power Input.** + 5 volt power supply input.
41 42	DIP DIN	I I	**AUI Receive Pair.** Differential input pair from the AUI transceiver DI circuit. The input is Manchester encoded.
43 44	DOP DON	O O	**AUI Transmit Pair.** A differential output driver pair for the AUI transceiver cable. The output is Manchester encoded.

FUNCTIONAL DESCRIPTION

The LXT904 Ethernet Interface Transceiver performs the physical layer signaling (PLS) functions as defined by the IEEE 802.3 specification. It functions as a PLS-Only device for use with 10BASE-5 or 10BASE-2 coaxial cable networks. In addition to standard 10 Mbps operation, the LXT904 also supports full-duplex 20 Mbps operation.

Refer to the block diagram on the first page of this data sheet. The LXT904 interfaces a back end controller to an AUI drop cable. The controller interface includes transmit and receive clock and NRZ data channels, as well as mode control logic and signaling. The AUI interface comprises three circuits: Data Output (DO), Data Input (DI) and Collision (CI). In addition to these basic interfaces, the LXT904 contains an internal crystal oscillator and three LED drivers for visual status reporting.

Functions are defined from the back end controller side of the interface. The LXT904 Transmit function refers to data transmitted by the back end to the AUI cable. The LXT904 receive function refers to data received by the back end from the AUI cable. The LXT904 receives incoming signals from the AUI DI circuit with ±18 ns of jitter and drives the AUI DO circuit. The CI pins are monitored for collision status.

Transmit Function

The LXT904 receives NRZ data from the controller at the TXD input, and passes it through a Manchester encoder. The encoded data is then transferred to the AUI cable (the DO circuit).

Receive Function

The LXT904 receive function acquires timing and data from the AUI (the DI circuit). Valid received signals are passed through the on-chip decoder and then output as decoded NRZ data and receive timing on the RXD and RCLK pins, respectively.

The receive function is activated only by valid data streams above the squelch level with proper timing. If the differential signal at the DI circuit inputs falls below 75% of the threshold level (unsquelched) for 8 bit times (typical), the LXT904 receive function enters the idle state.

Loopback Function

Loopback is controlled by the LBK pin. When LBK is High, data transmitted by the back-end is internally looped back from the TXD pin through the Manchester encoder/decoder to the RXD pin. When LBK is Low, no AUI loopback occurs.

Controller Compatibility Modes

The LXT904 is compatible with most industry standard controllers including devices produced by Motorola, Advanced Micro Devices (AMD), Intel, Fujitsu, National Semiconductor, Seeq and Texas Instruments. Four different control signal timing and polarity schemes (Modes 1 through 4) are required to achieve this compatibility. Mode select pins (MD0 and MD1) determine the controller compatibility mode as listed in Table 2.

A complete set of timing diagrams and specifications for each mode is provided in the Test Specifications section.

Table 2: Controller Compatibility Modes

Controller Mode	Settings	
	MD1	MD0
Mode 1–For Motorola 68EN360, Advanced Micro Devices AM7990 or compatible controllers	Low	Low
Mode 2–For Intel 82596 or compatible controllers	Low	High
Mode 3–For Fujitsu MB86950 or MB86960, Seeq 8005 or compatible controllers[1]	High	Low
Mode 4–For National Semiconductor 8390, Texas Instruments TMS380C26 or compatible controllers	High	High

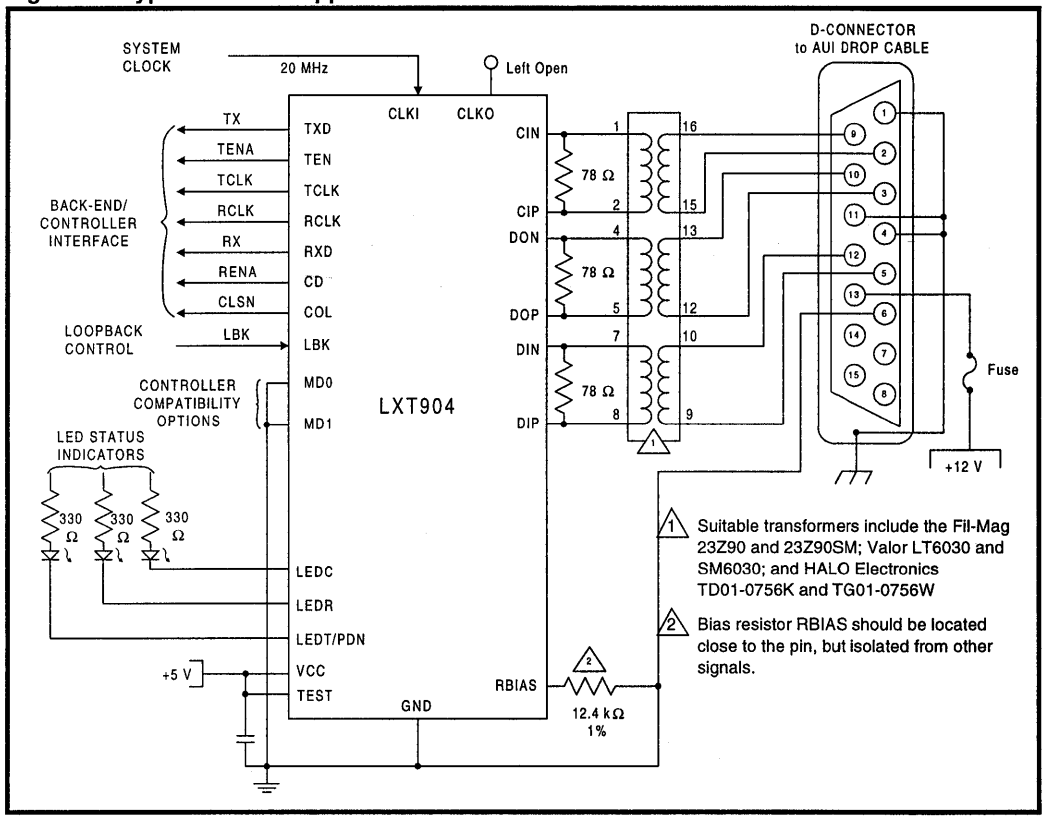
1. Seeq Controllers require inverters on CLKI, LBK, RCLK, and COL.

APPLICATION INFORMATION

Figure 2 is a typical LXT904 application. The diagram is arranged to group similar pins together; it does not represent the actual LXT904 pinout. The controller interface pins (transmit data, clock and enable; receive data and clock; and the collision detect, carrier detect and loopback control pins) are shown at the top left.

With MD1 and MD0 both Low, the LXT904 logic and framing are set to Mode 1 (compatible with AMD AM7990 controllers). The LBK input controls loopback. A 20 MHz system clock is supplied at CLKI with CLKO left open.

Figure 2: Typical LXT904 Application



TEST SPECIFICATIONS

NOTE

The minimum and maximum values in Tables 3 through 11 and Figures 3 through 26 represent the performance specifications of the LXT904 and are guaranteed by test, except where noted by design.

Table 3: Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
Supply Voltage	VCC	-0.3	-	6	V
Operating Temperature	TOP	0	-	70	°C
Storage Temperature	TST	-65	-	150	°C

CAUTION

Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 4: Operating Conditions (Voltage with respect to ground unless otherwise specified.)

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Recommended supply voltage	VCC	4.75	5.0	5.25	V	
Recommended operating temperature	TOP	0	-	70	°C	

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.

Table 5: Electrical Characteristics (Over Recommended Range)

Parameter		Symbol	Min	Typ[1]	Max	Units	Test Conditions
Input Low Voltage [2]		V_{IL}	-	-	0.8	V	
Input High Voltage [2]		V_{IH}	2.0	-	-	V	
Output Low Voltage		V_{OL}	-	-	0.4	V	I_{OL}= 1.6 mA
		V_{OL}	-	-	10	$\%V_{CC}$	I_{OL}< 10µA
Output Low Voltage (Open drain LED Driver)		V_{OLL}	-	-	0.7	V	I_{OLL}= 10mA
Output High Voltage		V_{OH}	2.4	-	-	V	I_{OH}= 40µA
		V_{OH}	90	-	-	$\%V_{CC}$	I_{OL} < 10µA
Supply current	Normal mode	I_{CC}	-	65	85	mA	Idle mode
		I_{CC}	-	70	90	mA	Transmitting on AUI
	Power Down mode	I_{CC}	-	0.75	2	mA	

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.
2. Limited functional test patterns are performed at these input levels. The majority of functional tests are performed at levels of 0 V and 3 V.

Table 6: Clock Timing (Over Recommended Range)

Parameter		Sym	Min	Typ[1]	Max	Units	Test Conditions
Output Rise Time	CMOS	-	-	3	12	ns	C_{LOAD} = 20 pF
TCLK & RCLK	TTL	-	-	2	8	ns	
Output Fall Time	CMOS	-	-	3	12	ns	C_{LOAD}= 20 pF
TCLK & RCLK	TTL	-	-	2	8	ns	
CLKI rise time (externally driven)		-	-	-	10	ns	
CLKI duty cycle (externally driven)		-	-	50/50	40/60	%	

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.

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Table 7: AUI Electrical Characteristics (Over Recommended Range)

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Input Low Current	I_{IL}	-	-	-700	mA	
Input High Current	I_{IH}	-	-	500	mA	
Differential Output Voltage	V_{OD}	±150	-	±1200	mV	
Differential Squelch Threshold	V_{DS}	150	220	350	mV	5 MHz square wave input

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.

Table 8: RCLK/Start-of-Frame Timing

Parameter		Symbol	Minimum	Typical[1]	Maximum	Units
Decoder acquisition time		tDATA	-	900	1100	ns
CD turn-on delay		tCD	-	50	200	ns
Receive data setup from RCLK	Mode 1	tRDS	60	70	-	ns
	Modes 2, 3 and 4	tRDS	30	45	-	ns
Receive data hold from RCLK	Mode 1	tRDH	10	20	-	ns
	Modes 2, 3 and 4	tRDH	30	45	-	ns

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.

Table 9: RCLK/End-of-Frame Timing

Parameter	Type	Sym	Mode 1	Mode 2	Mode 3	Mode 4	Units
RCLK after CD off	Minimum	tRC	5	1	27	5	bit times
Rx data throughput delay	Maximum	tRD	400	375	375	375	ns
CD turn off delay [2]	Maximum	tCDOFF	500	475	475	475	ns
Receive block out after TEN off	Typical[1]	tIFG	5	50	-	-	bit times

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.
2. CD turn-off delay is measured from the middle of the last bit; timing specification is unaffected by value of the last bit.

Table 10: Transmit Timing

Parameter	Symbol	Minimum	Typical [1]	Maximum	Units
TEN Setup from TCLK	tEHCH	22	-	-	ns
TXD Setup from TCLK	tDSCH	22	-	-	ns
TEN Hold after TCLK	tCHEL	5	-	-	ns
TXD Hold after TCLK	tCHDU	5	-	-	ns
Transmit Start-up Delay - AUI	tSTUD	-	200	450	ns
Transmit Through-put Delay - AUI	tTPD	-	-	300	ns

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.

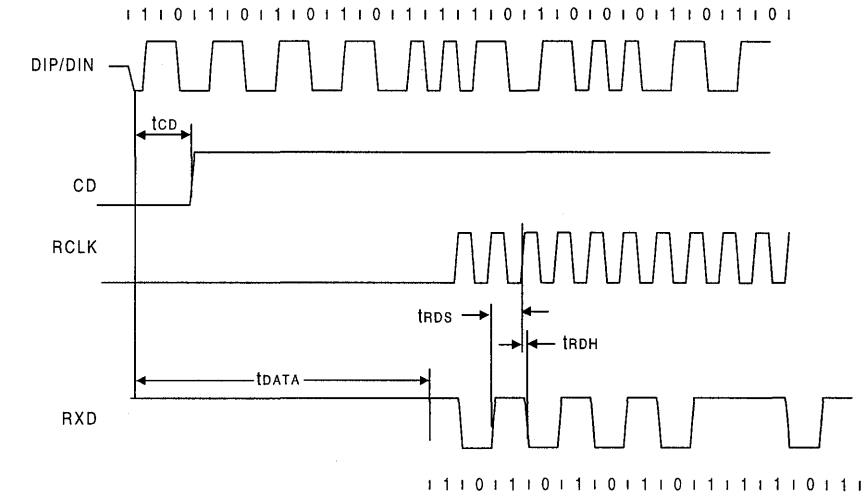
Table 11: Collision and Loopback Timing

Parameter	Symbol	Minimum	Typical [1]	Maximum	Units
COL turn on delay	tCOLD	-	-	500	ns
COL turn off delay	tCOLOFF	-	-	500	ns
COL (SQE) Delay after TEN off	tSQED	0.65	-	1.6	µs
COL (SQE) Pulse Duration	tSQEP	500	-	1500	ns
LBK setup from TEN	tKHEH	10	25	-	ns
LBK hold after TEN	tKHEL	10	0	-	ns

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.

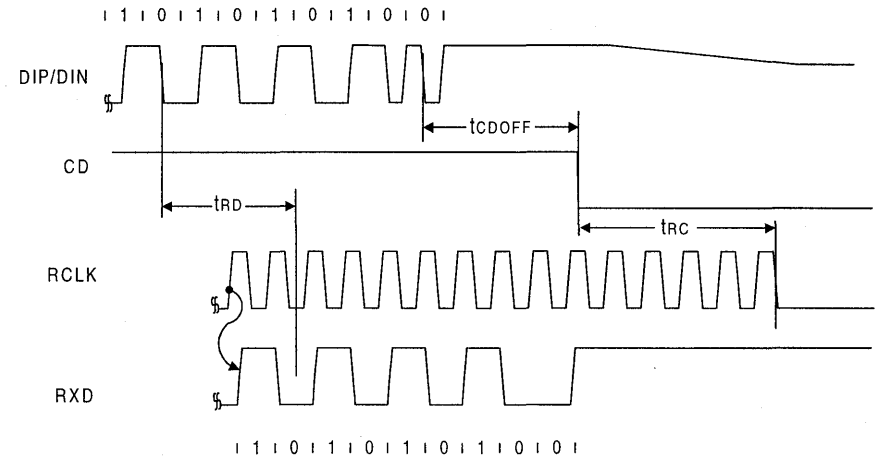
Timing Diagrams for Mode 1 (MD1 = Low, MD0 = Low)

Figure 3: Mode 1 RCLK/Start-of-Frame Timing



NOTE: 1. RXD changes 25 ns after the rising edge of RCLK.

Figure 4: Mode 1 RCLK/End-of-Frame Timing



NOTE: 1. RXD changes 25 ns after the rising edge of RCLK.

Figure 5: Mode 1 Transmit Timing

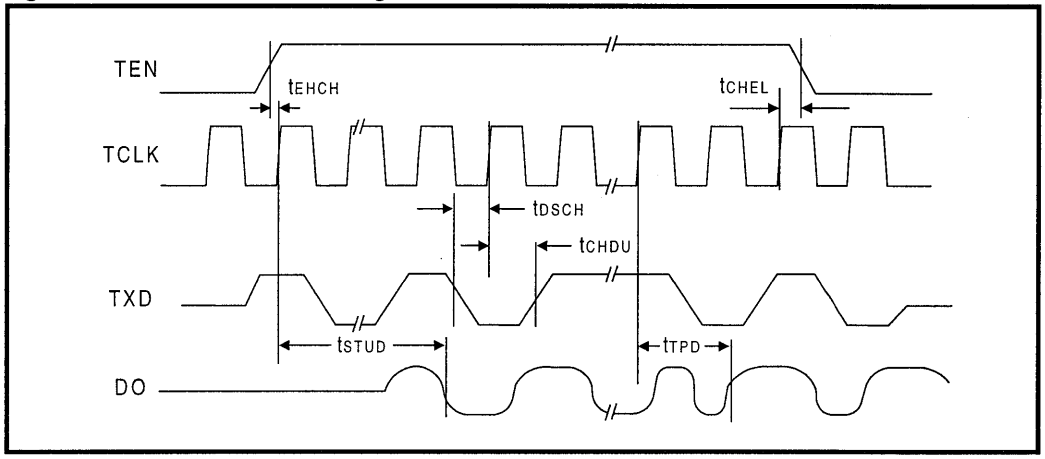


Figure 6: Mode 1 Collision Detect Timing

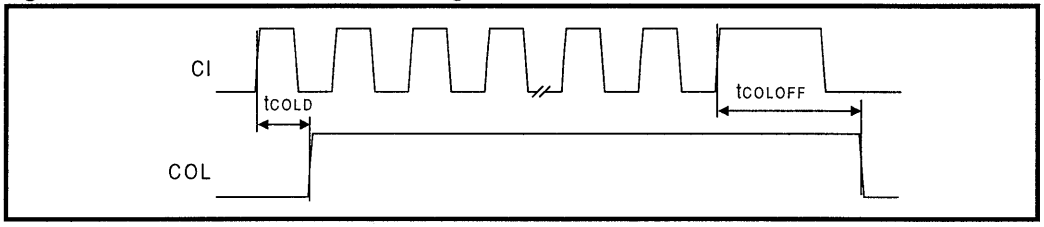


Figure 7: Mode 1 COL/CI Output Timing

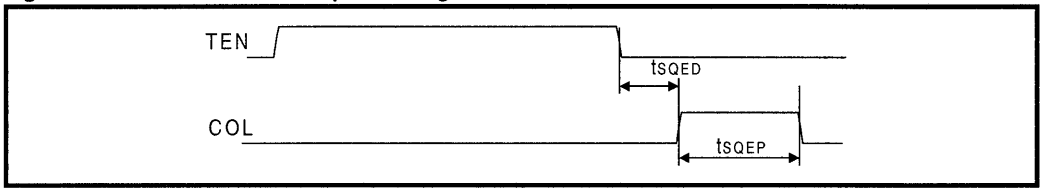
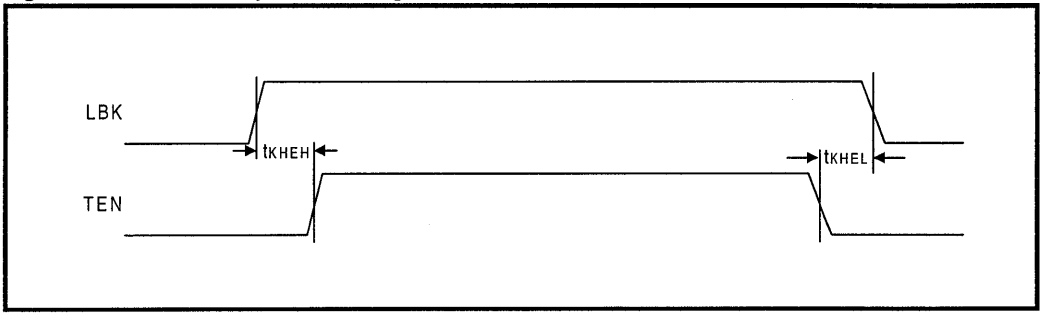
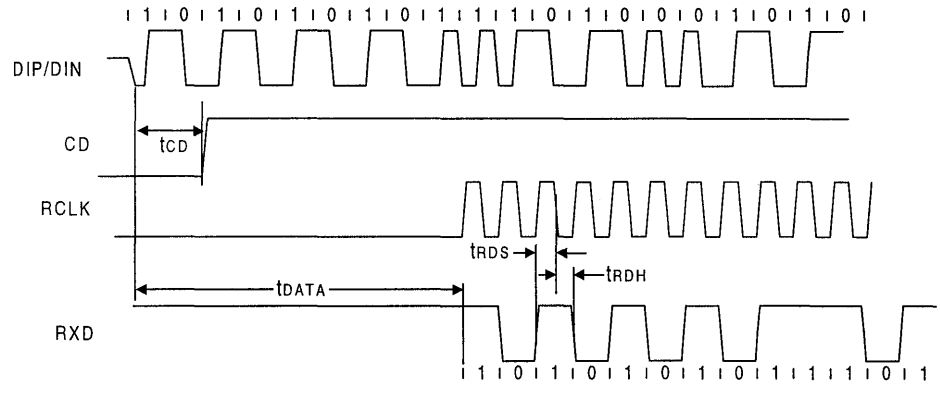


Figure 8: Mode 1 Loopback Timing



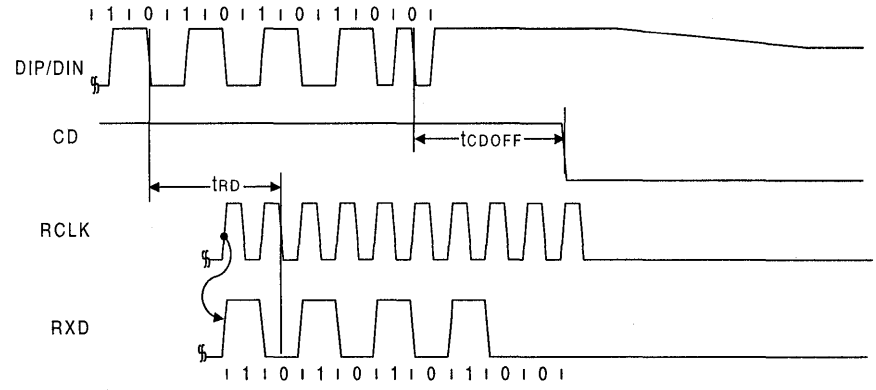
Timing Diagrams for Mode 2 (MD1 = Low, MD0 = High)

Figure 9: Mode 2 RCLK/Start-of-Frame Timing



NOTE: 1. RXD changes at the rising edge of RCLK. The controller is sampled at the falling edge.

Figure 10: Mode 2 RCLK/End-of-Frame Timing



NOTE: 1. RXD changes at the rising edge of RCLK. The controller is sampled at the falling edge.

Figure 11: Mode 2 Transmit Timing

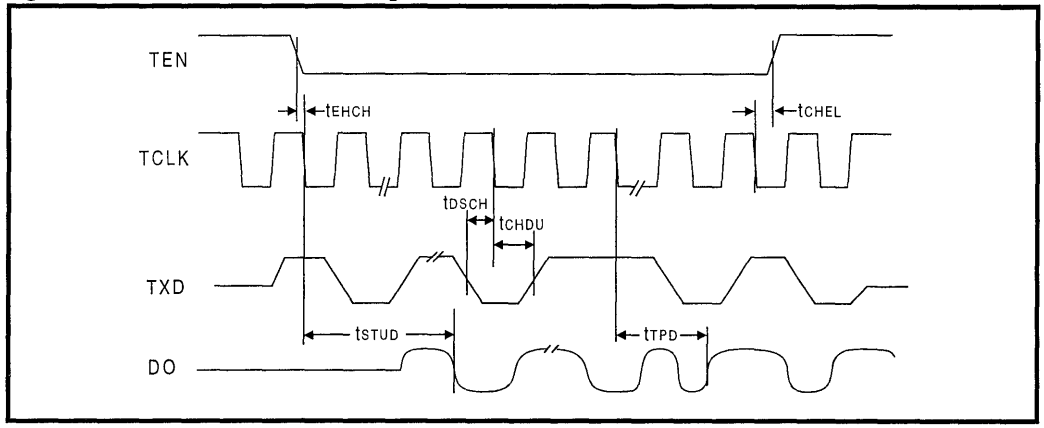


Figure 12: Mode 2 Collision Detect Timing

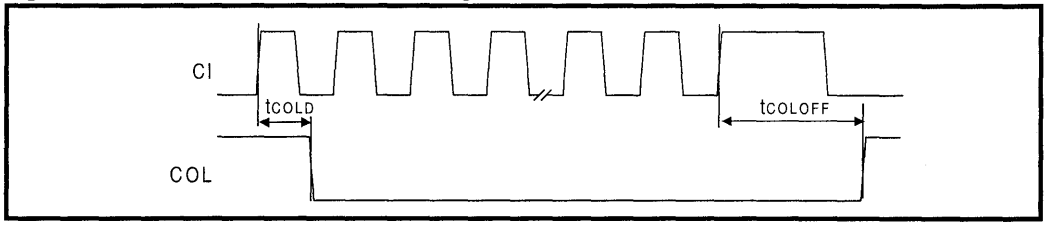
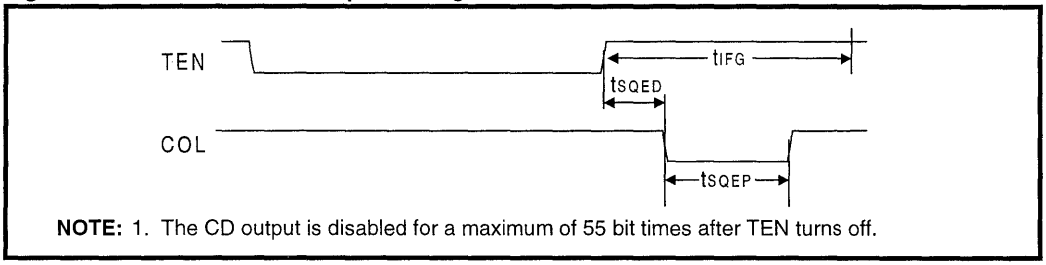
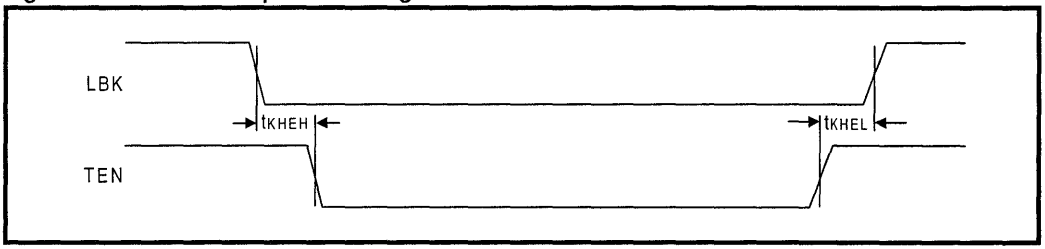


Figure 13: Mode 2 COL/CI Output Timing



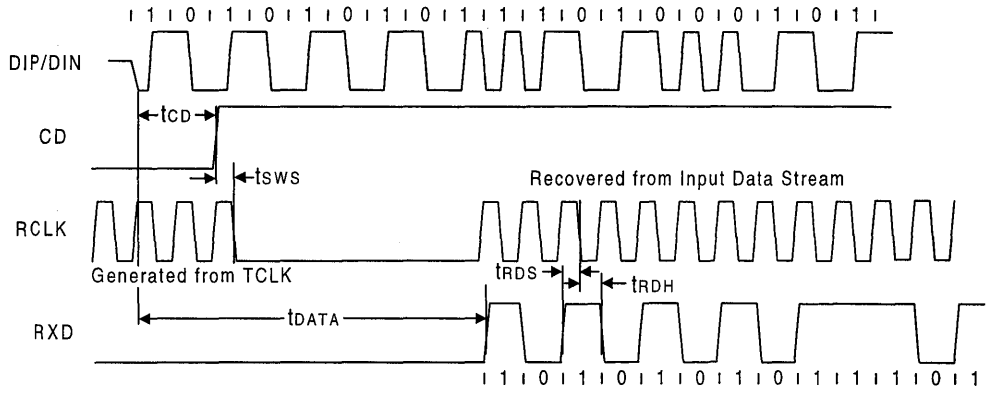
NOTE: 1. The CD output is disabled for a maximum of 55 bit times after TEN turns off.

Figure 14: Mode 2 Loopback Timing



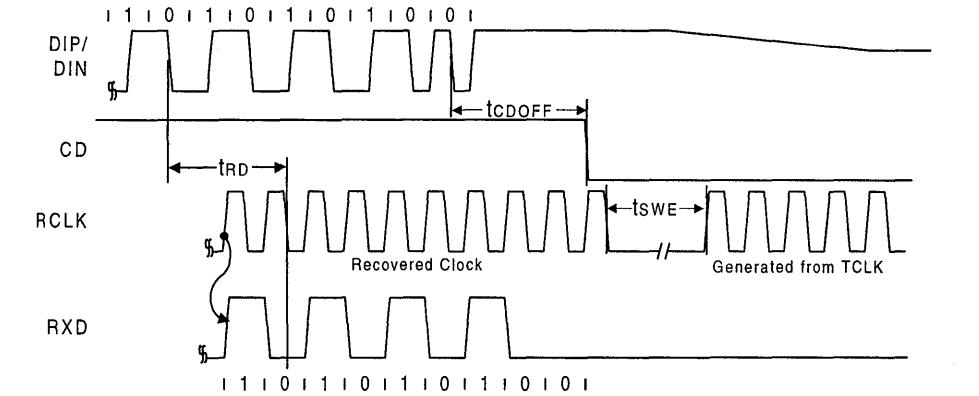
Timing Diagrams for Mode 3 (MD1 = High, MDO = Low)

Figure 15: Mode 3 RCLK/Start-of-Frame Timing



NOTE: 1. RXD changes at the rising edge of RCLK. The controller is sampled at the falling edge.

Figure 16: Mode 3 RCLK/End-of-Frame Timing



NOTE: 1. RXD changes at the rising edge of RCLK. The controller is sampled at the falling edge.

Figure 17: Mode 3 Transmit Timing

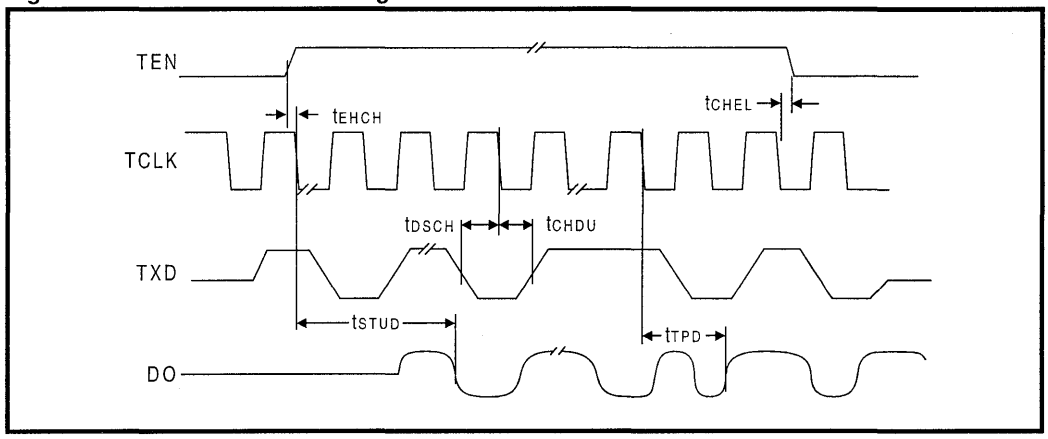


Figure 18: Mode 3 Collision Detect Timing

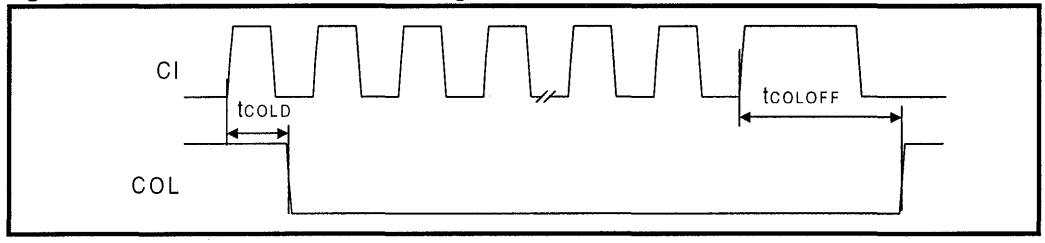
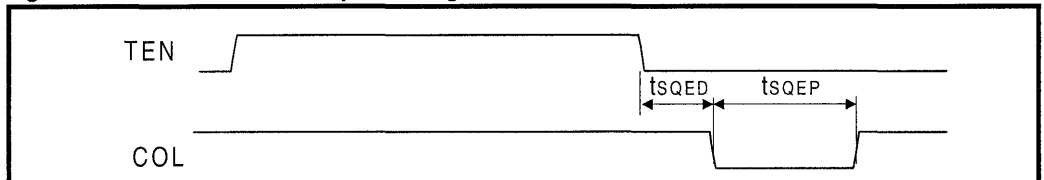
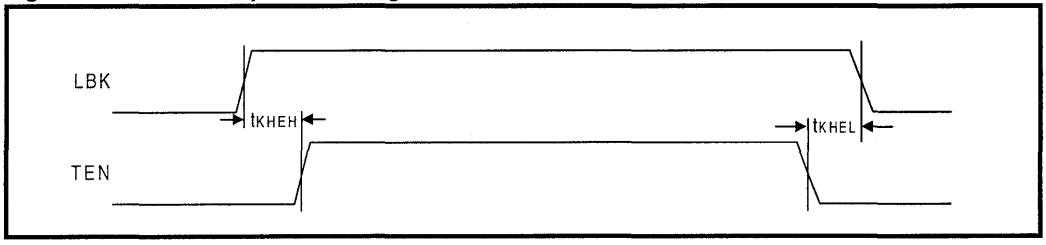


Figure 19: Mode 3 COL/CI Output Timing



NOTE: 1. The CD output is disabled for a maximum of 55 bit times after TEN turns off.

Figure 20: Mode 3 Loopback Timing



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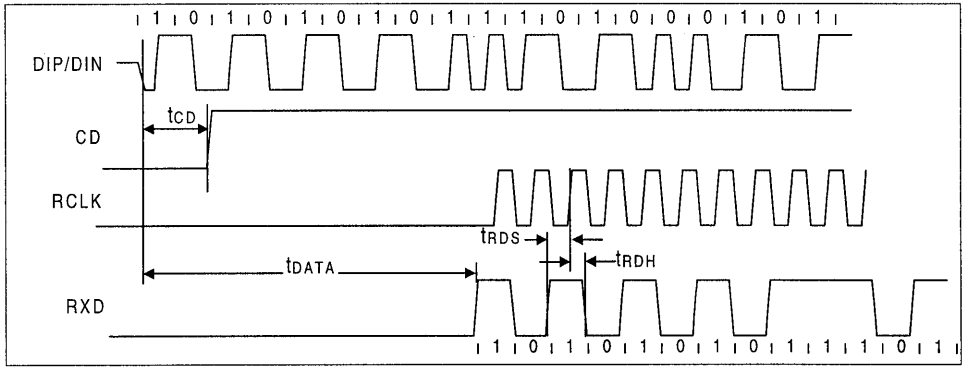
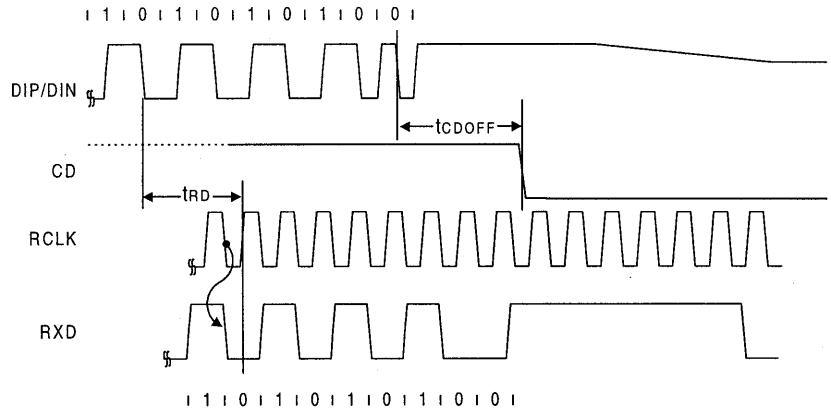
Timing Diagrams for Mode 4 (MD1 = High, MDO = High)

Figure 21: Mode 4 RCLK/Start of Frame Timing



NOTE: 1. RXD changes at the falling edge of RCLK. The controller is sampled at the rising edge.

Figure 22: Mode 4 RCLK/End of Frame Timing



NOTE: 1. RXD changes at the falling edge of RCLK. The controller is sampled at the rising edge.

Figure 23: Mode 4 Transmit Timing

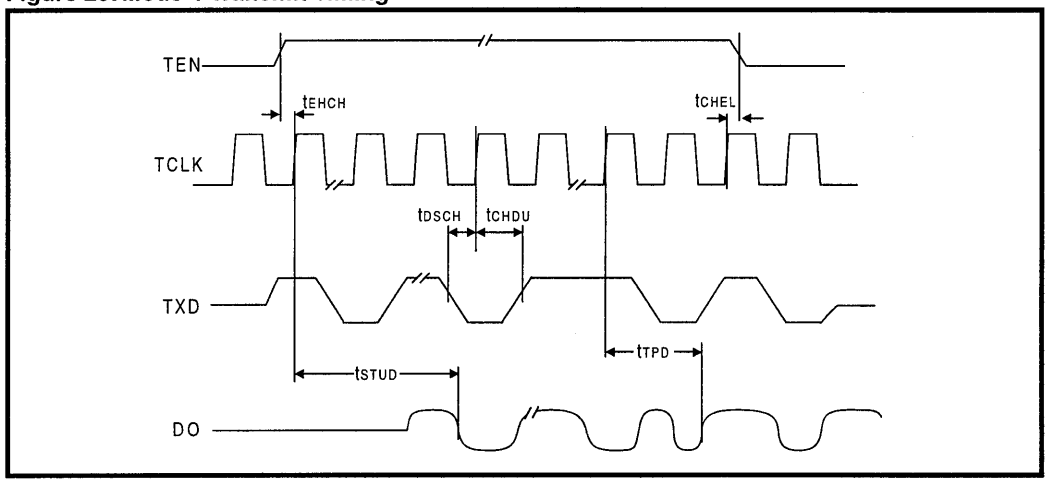


Figure 24: Mode 4 Collision Detect Timing

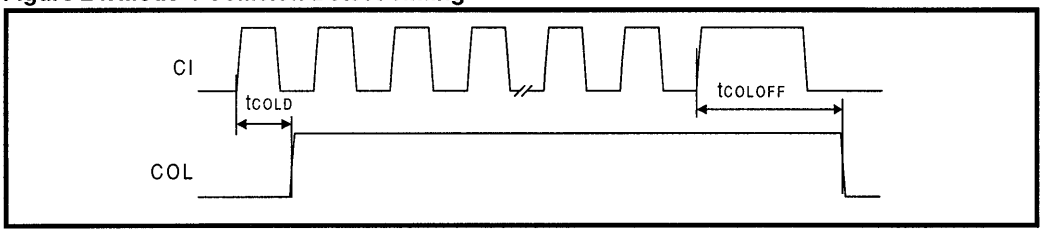


Figure 25: Mode 4 COL/CI Output Timing

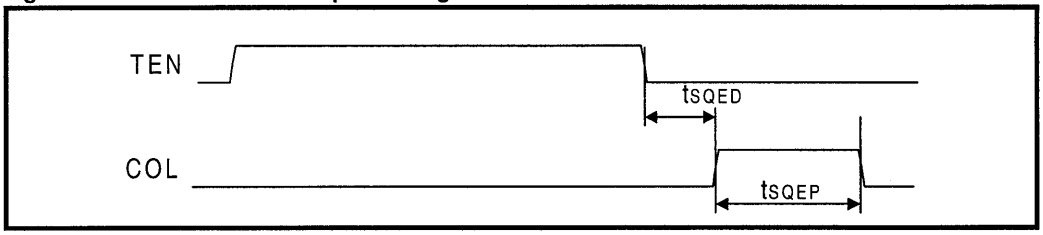
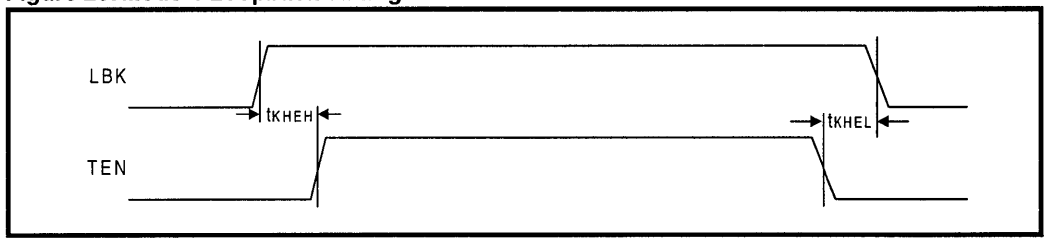


Figure 26: Mode 4 Loopback Timing



NOTES

LXT905

APRIL 1997
Revision 2.0

Universal Ethernet Interface Adapter

General Description

The LXT905 Universal Ethernet Interface Adapter is designed for IEEE 802.3 physical layer applications. It provides, in a single CMOS device, all the active circuitry for interfacing most standard 802.3 controllers to 10BASE-T media.

LXT905 functions include Manchester encoding/decoding, receiver squelch and transmit pulse shaping, jabber, link integrity testing and reversed polarity detection/correction. The LXT905 drives the 10BASE-T twisted-pair cable with only a simple isolation transformer. Integrated filters simplify the design work required for FCC compliant EMI performance.

The LXT905 is fabricated with an advanced process and requires only a single 5 or 3.3 volt power supply.

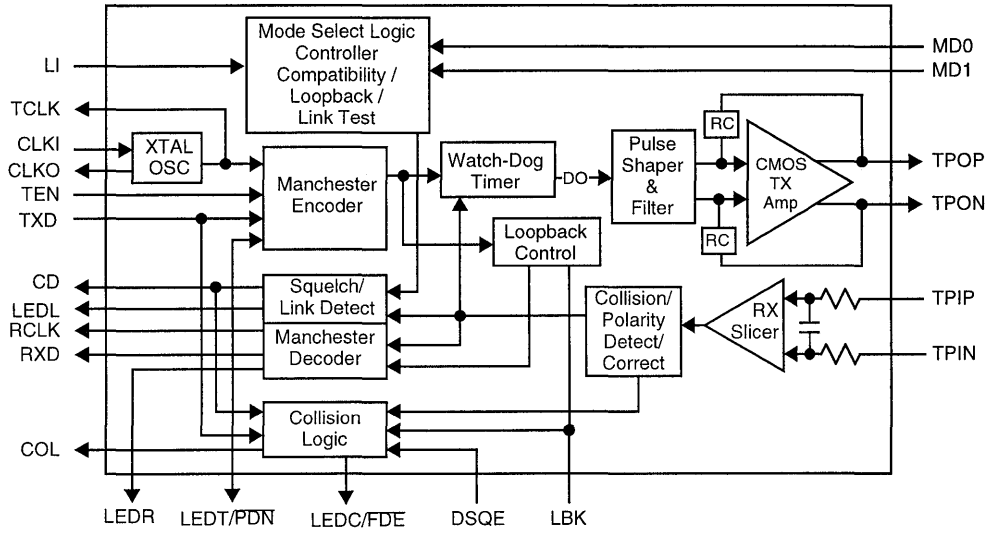
Applications

- Hub/Switched Dedicated LANs for 10BASE-T
- Desktop 10BASE-T LAN adapter boards
- Laptop and Portable applications

Features

- Transparent 3.3 V or 5 V operation
- Integrated filters – Simplifies FCC compliance
- Integrated Manchester encoder/decoder
- 10BASE-T compliant transceiver
- Automatic polarity correction
- Available in 28-pin PLCC and 32-pin LQFP packages
- SQE enable/disable
- Four LED drivers
- Full duplex capability
- Power-down mode with tristate

LXT905 Block Diagram



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PIN ASSIGNMENTS AND SIGNAL DESCRIPTIONS

Figure 1: LXT905 Pin Assignments

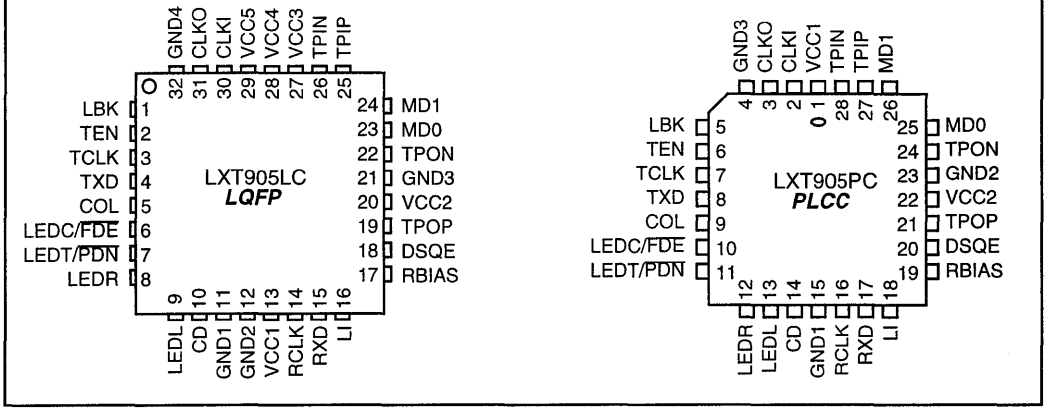

Table 1: LXT905 Signal Descriptions

LQFP Pin #	PLCC Pin #	Symbol	I/O	Description
13 20 27 28 29	1 22 – – –	VCC1 VCC2 VCC3 VCC4 VCC5	– – – – –	**Power Inputs 1 thru 5.** Power supply inputs of +5 volts or +3.3 volts.
30 31	2 3	CLKI CLKO	I O	**Crystal Oscillator.** A 20 MHz crystal must be connected across these pins, or a 20 MHz clock applied at CLKI with CLKO left open.
11 12 21 32	15 23 4 –	GND1 GND2 GND3 GND4	– – – –	**Ground.**
1	5	LBK	I	**Loopback.** When High, forces internal loopback. Disables collision and the transmission of both data and link pulses. Pulled Low internally.
2	6	TEN	I	**Transmit Enable.** Enables data transmission and starts the watchdog timer. Synchronous to TCLK. Pulled Low internally.
3	7	TCLK	O	**Transmit Clock.** A 10 MHz clock output. This clock signal should be directly connected to the transmit clock input of the controller.
4	8	TXD	I	**Transmit Data.** Input signal containing NRZ data to be transmitted on the network. TXD should be connected directly to the transmit data output of the controller. Pulled Low internally.
5	9	COL	O	**Collision Signal.** Output that drives the collision detect input of the controller.

Table 1: LXT905 Signal Descriptions – continued

LQFP Pin #	PLCC Pin #	Symbol	I/O	Description
6	10	LEDC/ FDE	O I	**LED Collision or Full Duplex Enable.** **LEDC** is an open drain driver for the collision indicator pulls Low during collision. LED "on" (*i.e.*, Low output) time is extended by approximately 100 ms. **FDE** enables full duplex mode (external loopback) if tied Low externally. Pulled high internally.
7	11	LEDT/ $\overline{\text{PDN}}$	O I	**LED Transmit or Power Down.** **LEDT** is an open drain driver for the transmit indicator. LED "on" (*i.e.*, Low output) time is extended by approximately 100 ms. Output is pulled Low during transmit. If externally tied Low, the LXT905 goes to power down state ($\overline{\text{PDN}}$). In Power-down Mode, all logic inputs and outputs are tristated.
8	12	LEDR	O	**LED Receive.** Open drain driver for the receive indicator LED. LED "on" (*i.e.*, Low output) time is extended by approximately 100 ms. Output is pulled Low during receive. Pulled High internally.
9	13	LEDL	O	**LED Link.** Open drain driver for link integrity indicator. Output is pulled Low during link test pass. Pulled High internally.
10	14	CD	O	**Carrier Detect.** An output for notifying the controller that activity exists on the network.
14	16	RCLK	O	**Receive Clock.** A recovered 10 MHz clock which is synchronous to the received data and connected to the controller receive clock input.
15	17	RXD	O	**Receive Data.** Output signal connected directly to the receive data input of the controller.
16	18	LI	I	**Link Enable.** Controls link integrity test; enabled when LI is High, disabled when LI is Low.
17	19	RBIAS	I	**Bias Circuitry.** A 7.5 kΩ 1% resistor to ground at this pin controls operating circuit bias.
18	20	DSQE	I	**SQE Disable.** When DSQE is High, the SQE function is disabled. When DSQE is Low, the SQE function is enabled. SQE should be disabled for normal operation in Hub/Switch/Repeater applications. Pulled Low internally.
19 22	21 24	TPOP TPON	O O	**Twisted Pair Outputs.** Differential outputs to the twisted-pair cable. The outputs are pre-equalized.
23 24	25 26	MDO MDI	I I	**Mode Select 0 and 1.** Mode select pins determine controller compatibility mode in accordance with Table 2. Pulled Low internally.
25 26	27 28	TPIP TPIN	I I	**Twisted-Pair Inputs.** A differential input pair from the twisted-pair cable. Receive filter is integrated on-chip. No external filters are required.

FUNCTIONAL DESCRIPTION

Introduction

The LXT905 Universal Ethernet Interface Transceiver performs the physical layer signaling (PLS) and Media Attachment Unit (MAU) functions as defined by the IEEE 802.3 specification. It functions as an integrated PLS/MAU for use with 10BASE-T twisted-pair networks.

The LXT905 interfaces a back end controller to a twisted-pair (TP) cable. The controller interface includes transmit and receive clock and NRZ data channels, as well as mode control logic and signaling. The twisted-pair interface comprises two circuits: Twisted-Pair Input (TPI) and Twisted-Pair Output (TPO). In addition to the two basic interfaces, the LXT905 contains an internal crystal oscillator and four LED drivers for visual status reporting.

Functions are defined from the back end controller side of the interface. The LXT905 Transmit function refers to data transmitted by the back end to the twisted-pair network. The LXT905 Receive function refers to data received by the back end from the twisted-pair network. The LXT905 performs all required functions defined by the IEEE 802.3 10BASE-T MAU specification such as collision detection, link integrity testing, signal quality error messaging, jabber control and loopback.

Controller Compatibility Modes

The LXT905 is compatible with most industry standard controllers including devices produced by Advanced Micro Devices (AMD), Intel, Fujitsu, National Semiconductor, Seeq, Motorola and Texas Instruments. Four different control signal timing and polarity schemes (Modes 1 through 4) are required to achieve this compatibility. Mode select pins MD0 and MD1 determine controller compatibility modes as listed in Table 2. Refer to the Test Specifications section for timing diagrams and parameters.

Transmit Function

The LXT905 receives NRZ data from the controller at the TXD input as shown in the block diagram, and passes it through a Manchester encoder. The encoded data is then transferred to the twisted-pair network (the TPO circuit). The advanced integrated pulse shaping and filtering network produces the output signal on TPON and TPOP, shown in Figure . The TPO output is pre-distorted and pre-filtered to meet the 10BASE-T jitter template. An internal continuous resistor-capacitor filter is used to remove any high-frequency clocking noise from the pulse shaping circuitry. Integrated filters simplify the design work required for FCC compliant EMI performance. During idle periods, the LXT905 transmits link integrity test pulses on the TPO circuit (if LI is enabled and LBK is disabled).

Figure 2: LXT905 TPO Output Waveform

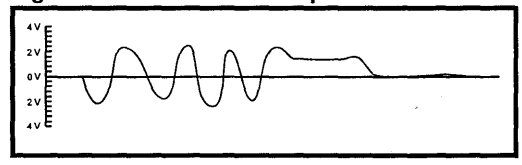

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Table 2: Controller Compatibility Mode Options

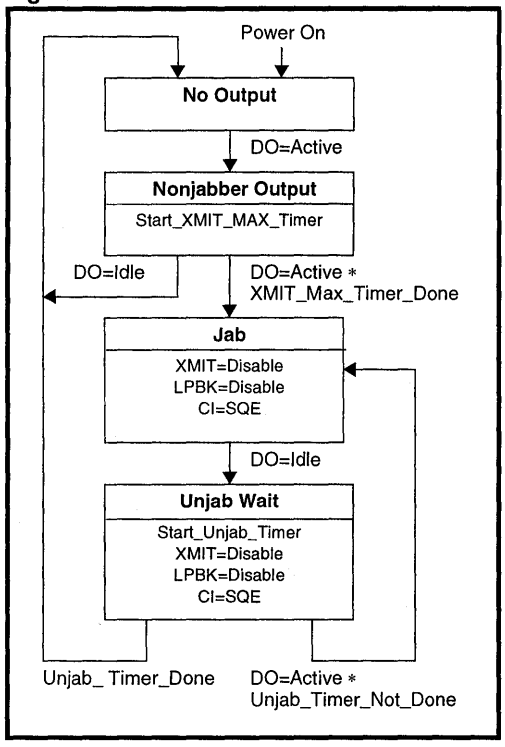
Controller Mode	MD1	MD0
Mode 1 - For Advanced Micro Devices AM7990 or compatible controllers	Low	Low
Mode 2 - For Intel 82596 or compatible controllers[1]	High	Low
Mode 3 - For Fujitsu MB86950, MB86960 or compatible controllers (Seeq 8005)[2]	Low	High
Mode 4 - For National Semiconductor 8390 or compatible controllers (TI TMS380C26)	High	High

2. Refer to Level One Application Note 51 when designing with Intel controllers.
3. SEEQ controllers require inverters on CLKI, LBK, RCLK and COL.

Jabber Control Function

Figure 3 is a state diagram of the LXT905 jabber control function. The LXT905 on-chip watchdog timer prevents the DTE from locking into a continuous transmit mode. When a transmission exceeds the time limit, the watchdog timer disables the transmit and loopback functions and activates the COL pin. Once the LXT905 is in the jabber state, the TXD circuit must remain idle for a period of 0.25 to 0.75 seconds before it will exit the jabber state.

Figure 3: Jabber Control Function

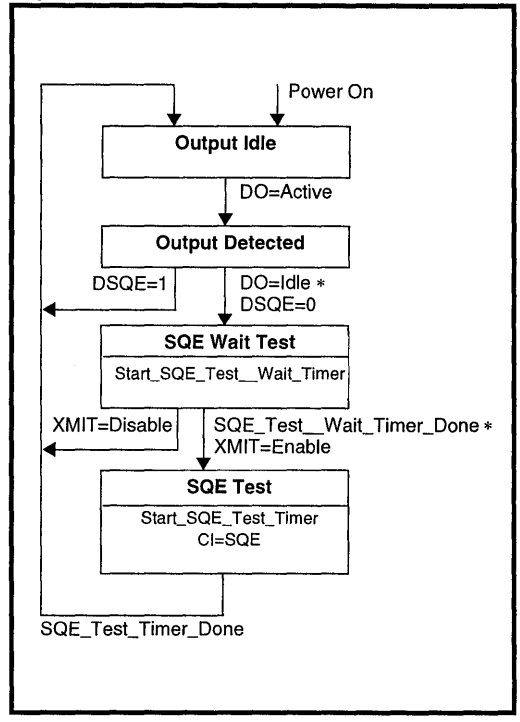


SQE Function

The LXT905 supports the signal quality error (SQE) function as shown in Figure 4. After every successful transmission on the 10BASE-T network, the LXT905 transmits the SQE signal for 10 bit times (BT) ± 5BT on the COL pin of the device.

The SQE can be disabled for repeater/switch applications. When DSQE is set High, the SQE function is disabled. When DSQE is Low, the SQE function is enabled.

Figure 4: SQE Function



Receive Function

The LXT905 receive function acquires timing and data from the twisted-pair network (the TPI circuit). Valid received signals are passed through the on-chip filters and Manchester decoder then output as decoded NRZ data and receive timing on the RXD and RCLK pins, respectively.

An internal RC filter and an intelligent squelch function discriminate noise from link test pulses and valid data streams. The receive function is activated only by valid data streams above the squelch level with proper timing.

If the differential signal at the TPI circuit inputs falls below 85% of the threshold level (unsquelched) for 8 bit times (typical), the LXT905 receive function enters the idle state. The LXT905 automatically corrects reversed polarity on the TPI circuit.

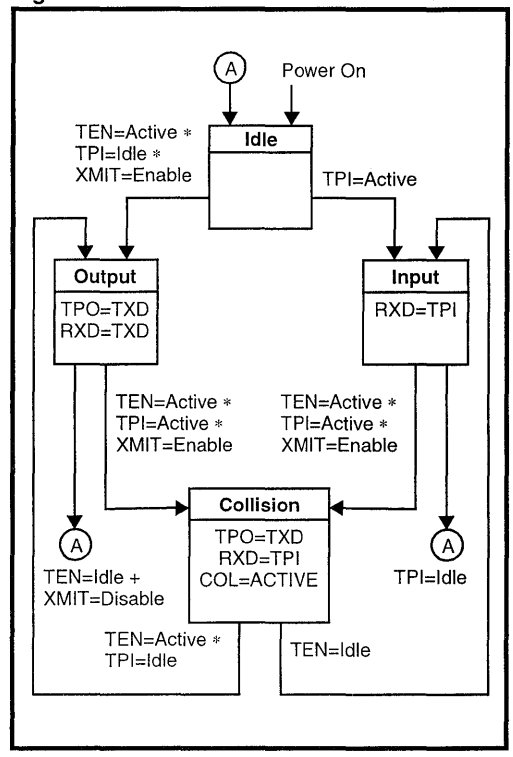
Polarity Reverse Function

The LXT905 polarity reverse function uses both link pulses and end-of-frame data to determine polarity of the received signal. If Link Integrity testing is disabled, polarity detection is based only on received data. A reversed polarity condition is detected when eight consecutive opposite receive link pulses are detected without receipt of a link pulse of the expected polarity. Reversed polarity is also detected if four consecutive frames are received with a reversed start-of-idle. Whenever a correct polarity frame or a correct link pulse is received, these two counters are reset to zero. If the LXT905 enters the link fail state and no valid data or link pulses are received within 96 to 128 ms, the polarity is reset to the default non-flipped condition. Polarity correction is always enabled.

Collision Detection Function

A collision is defined as the simultaneous presence of valid signals on both the TPI circuit and the TPO circuit. The LXT905 reports collisions to the back-end via the COL pin. If the TPI circuit becomes active while there is activity on the TPO circuit, the TPI data is passed to the back-end over the RXD circuit, disabling normal loopback. Figure 5 is a state diagram of the LXT905 collision detection function.

Figure 5: Collision Detection Function



Loopback Function

The LXT905 provides the normal loopback function specified by the 10BASE-T standard for the twisted-pair port, as well as a forced loopback function. The loopback function operates in conjunction with the transmit function. Data transmitted by the back-end is internally looped back within the LXT905 from the TXD pin through the Manchester encoder/decoder to the RXD pin and returned to the back-end. This "normal" loopback function is disabled when a data collision occurs, clearing the RXD circuit for the TPI data. Normal loopback is also disabled during link fail, jabber, and full duplex states. Loopback is always enabled during the forced loopback state.

The LXT905 provides an additional loopback function. External loopback mode, useful for system-level testing, is controlled by the LEDC/$\overline{\text{FDE}}$ pin. With both LEDC/$\overline{\text{FDE}}$ and LBK Low, the LXT905 device:

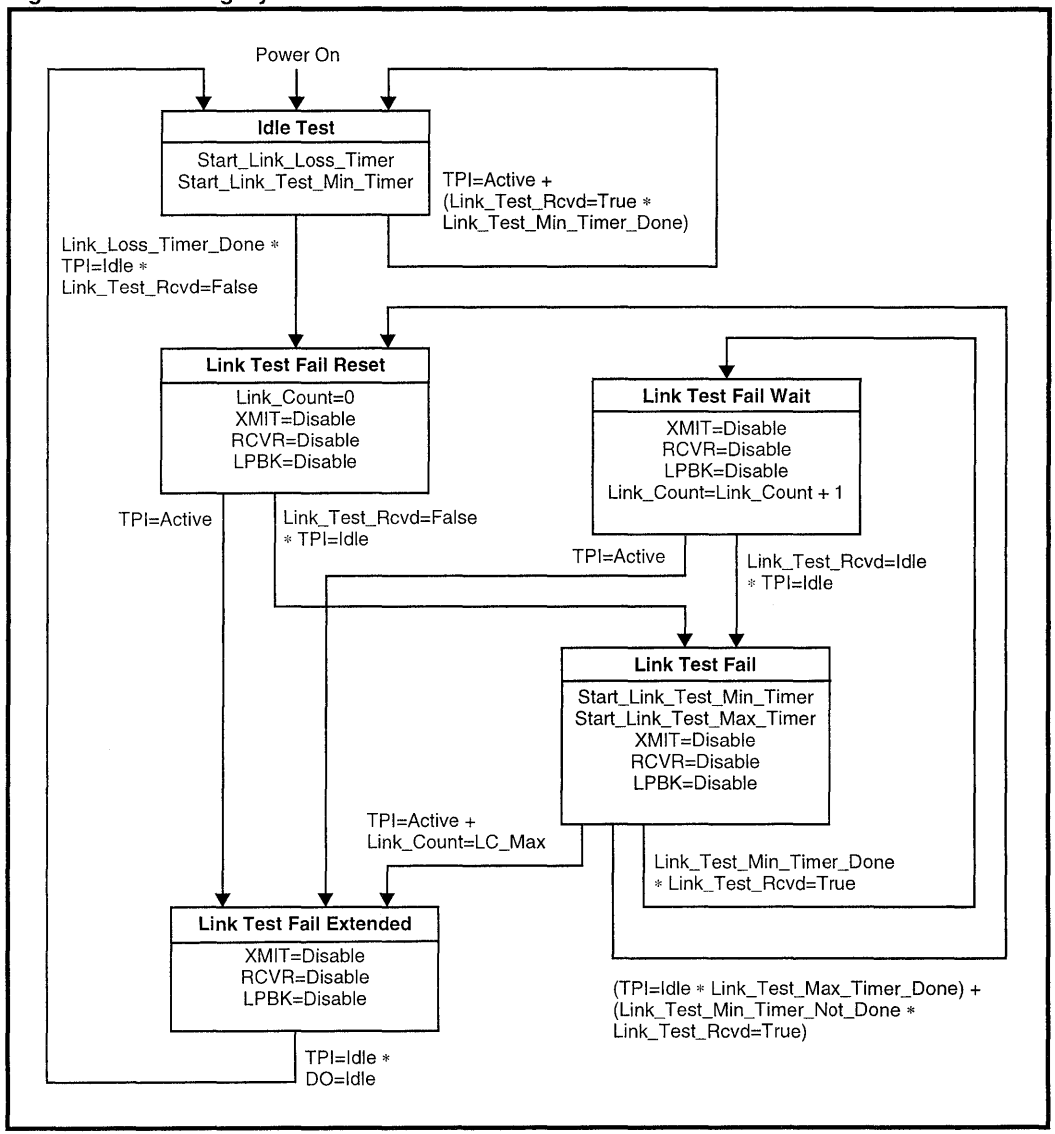
- disables internal loopback circuits
- disables SQE
- disables Collision Detection
- enables Full Duplex Mode

This allows external loopback testing.

Link Integrity Test Function

Figure 6 is a state diagram of the LXT905 Link Integrity test function. The link integrity test is used to determine the status of the receive side twisted-pair cable. Link integrity testing is enabled when pin 18 (LI) is tied High. When enabled, the receiver recognizes link integrity pulses which are transmitted in the absence of receive traffic. If no serial data stream or link integrity pulses are detected within 50~150 ms, the chip enters a link fail state and disables the transmit and normal loopback functions. The LXT905 ignores any link integrity pulse with interval less than 2~7 ms. The LXT905 will remain in the Link Fail State until it detects either a serial data packet or two or more link integrity pulses.

Figure 6: Link Integrity Test Function



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APPLICATION INFORMATION

Introduction

Figures 7 through 9 show typical LXT905 applications. These diagrams group similar pins; they do not portray the actual chip pinout. The controller interface pins; Transmit Data (TXD), Transmit Clock (TCLK) Transmit Enable (TEN), Receive Data (RXD), Receive Clock (RCLK), Collision Signal (COL) and Carrier Detect (CD) pins are at the upper left.

Power and ground pins are at the bottom of each diagram. VCC1 and VCC2 use a single power supply with decoupling capacitors installed between the power and ground busses. VCC may be powered by a 5V or 3.3V supply.

Twisted-Pair Interface

The Twisted-Pair interface (TPOP/N and TPIP/N) is at the upper right. The I/O pairs have impedance matching resistors for 100Ω UTP but no external filters are required.

RBIAS Pin

The RBIAS pin sets the levels for the LXT905 output drivers. The LXT905 requires a 7.5kΩ, 1% resistor directly connected between the RBIAS pin and ground. This resistor should be located as close to the device as possible. Keep the traces as short as possible and isolated from all other high speed signals.

Crystal Information

Based on limited evaluation, Table 3 lists some of the suitable crystals. Designers should test and validate all crystals before committing to a specific component.

Table 3: Suitable Crystals

Manufacturer	Part Number
MTRON	MP-1
	MP-2

Magnetic Information

The LXT905 requires a 1:1 turns ratio for the receive transformer and a 1:2 turns ratio for the transmit transformer. Table 4 lists transformers suitable for the applications described in this data sheet. Designers are advised to test and validate all magnetics before committing to a specific component.

Table 4: Suitable Magnetics

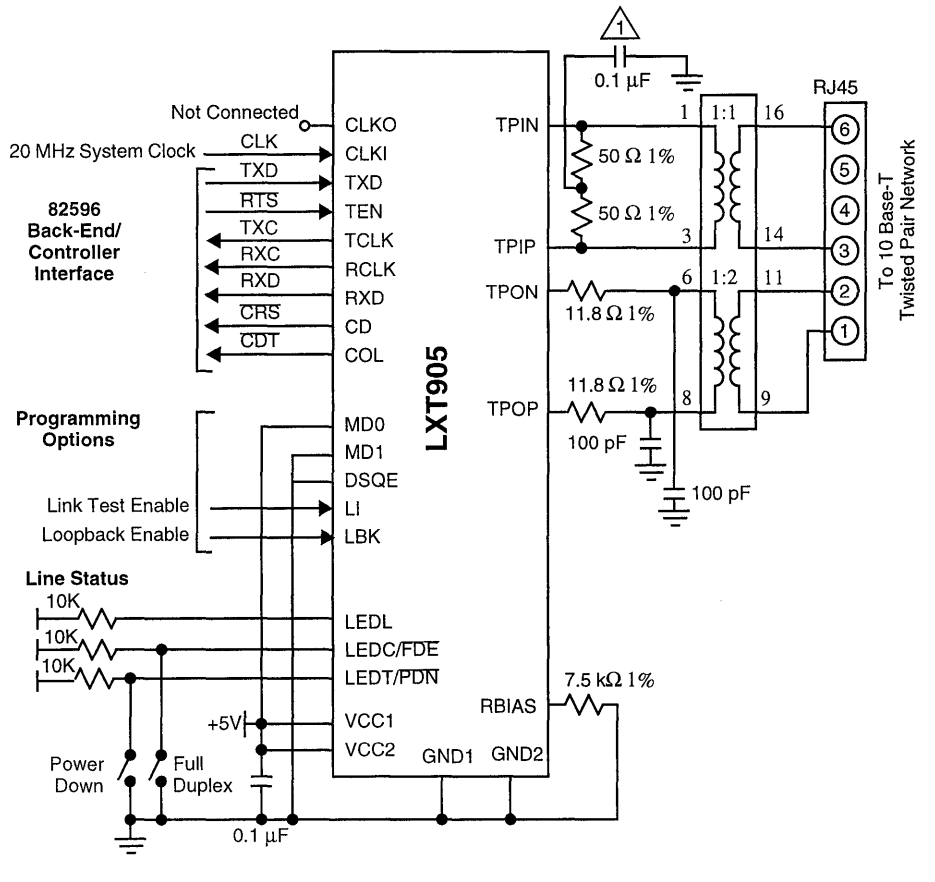
Manufacturer	Part Number	
	Surface Mount	Thru-hole
Valor	ST4160	–
	ST4202	–
	ST4167	–
HALO	TG74-1406N1	TG74-1406Q
	TG75-1406N	TG74-1406K
Fil-Mag	23Z441SM	23Z441

Typical 10BASE-T Application

Figure 7 is a typical LXT905 application. The DTE is connected to a 10BASE-T network through the twisted-pair RJ45 connector. With MD0 tied high and MD1 grounded, the LXT905 logic and framing are set to Mode 2 (compatible with Intel 82596 controllers*). Connect 20 MHz system clock input at CLKI. (Leave CLKO open.) The LI pin externally controls the link test function.

*Refer to Level One Application Note 51 when designing with Intel controllers.

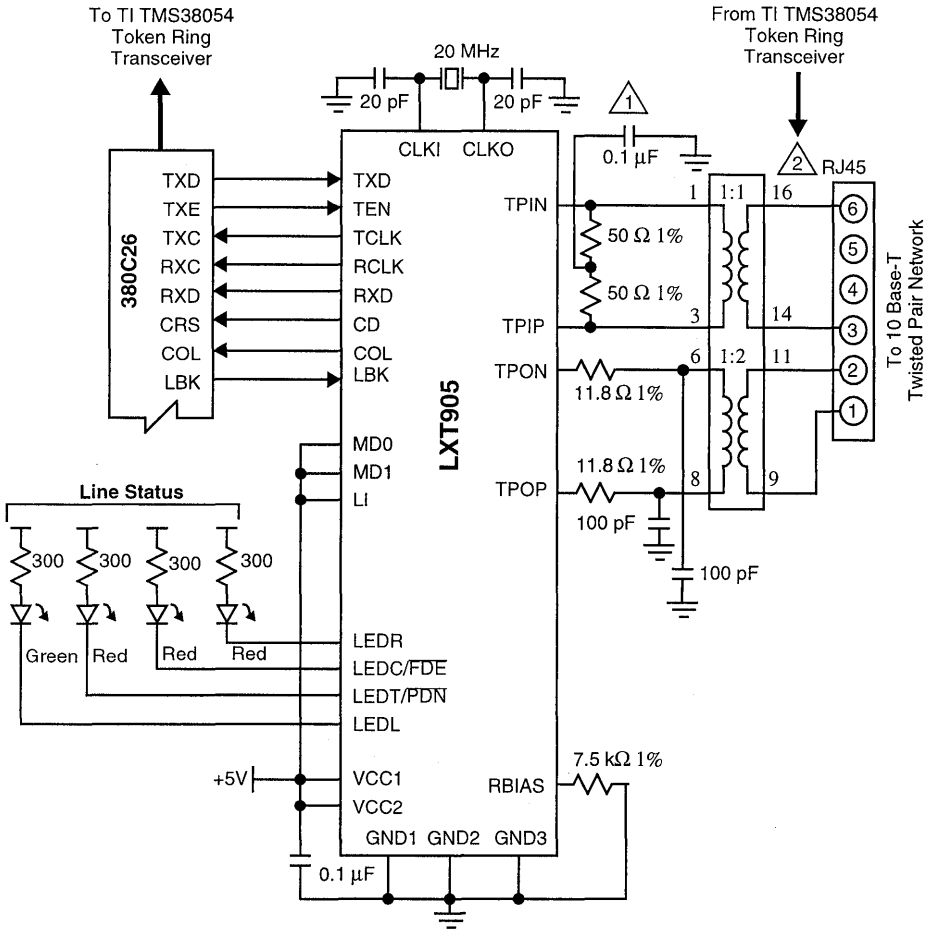
Figure 7: Intel Controller Application (Mode 2)



Dual Network Support - 10BASE-T and Token Ring

Figure 8 shows the LXT905 with a Texas Instruments 380C26 CommProcessor. The 380C26 is compatible with Mode 4 (MD0 and MD1 both high). When used with the 380C26, both the LXT905 and a TMS38054 Token Ring transceiver can be tied to a single RJ45 allowing dual network support from a single connector.

Figure 8: LXT905/380C26 Interface for Dual 10BASE-T & Token Ring Support (Mode 4)



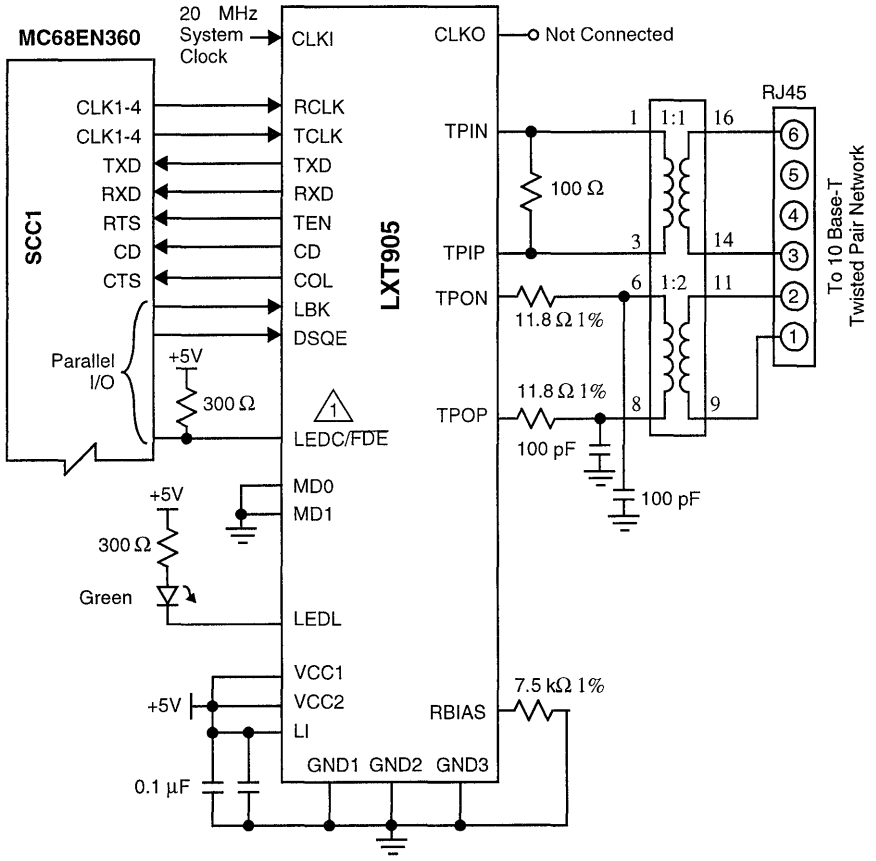
1 Optional: Centertap capacitor may improve EMC depending on board layout and system design.

2 Additional magnetics and switching logic (not shown) are required to implement the dual network solution.

Simple 10BASE-T Connection

Figure 9 shows a simple 10BASE-T application using an LXT905 transceiver and a Motorola MC68EN360. The MC68EN360 is compatible with Mode 1 (MD0 and MD1 both low).

Figure 9: LXT905/MC68EN360 Interface for Full Duplex 10BASE-T (Mode 1)



TEST SPECIFICATIONS

NOTE

The minimum and maximum values in Tables 5 through 13 and Figures 10 through 25 represent the performance specifications of the LXT905 and are guaranteed by test, except where noted by design.

Table 5: Absolute Maximum Values

Parameter	Symbol	Min	Max	Units
Supply voltage	VCC	-0.3	+6	V
Ambient operating temperature	TOP	0	+70	°C
Storage temperature	TST	-65	+150	°C

CAUTION

Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 6: Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Recommended supply voltage[1]	VCC	3.135	5.0	5.25	V	
Recommended operating temperature	TOP	0	–	70	°C	

1. Voltage is with respect to ground unless specified otherwise.

Table 7: I/O Electrical Characteristics (Over Recommended Range)

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Input low voltage[2]	VIL	–	–	0.8	V	
Input high voltage[2]	VIH	2.0	–	–	V	
Output low voltage	VOL	–	–	0.4	V	IOL = 1.6 mA
	VOL	–	–	10	%VCC	IOL < 10 µA
Output low voltage (Open drain LED driver)	VOLL	–	–	0.7	%VCC	IOLL = 10 mA
Output high voltage	VOH	2.4	–	–	V	IOH = 40 µA
	VOH	90	–	–	%VCC	IOH < 10 µA

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Limited functional tests are performed at these input levels. The majority of functional tests are performed at levels of 0V and 3V. This applies to all inputs except TPIP and TPIN.

Table 7: I/O Electrical Characteristics (Over Recommended Range) – continued

Parameter		Sym	Min	Typ[1]	Max	Units	Test Conditions
Output rise time	CMOS	–	–	3	15	ns	C_{LOAD} = 20 pF
TCLK & RCLK	TTL	–	–	2	15	ns	
Output fall time	CMOS	–	–	3	15	ns	C_{LOAD}= 20 pF
TCLK & RCLK	TTL	–	–	2	15	ns	
CLKI rise time (externally driven)		–	–	–	10	ns	
CLKI duty cycle (externally driven)		–	–	50/50	40/60	%	
Supply current	Normal	I_{CC}	–	40	80	mA	Idle Mode
	Mode	I_{CC}	–	70	100	mA	Transmitting on TP
	Power Down Mode	I_{CC}	–	0.01	1	µA	

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Limited functional tests are performed at these input levels. The majority of functional tests are performed at levels of 0V and 3V. This applies to all inputs except TPIP and TPIN.

Table 8: TP Electrical Characteristics (Over Recommended Range)

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Transmit output impedance	Z_{OUT}	–	5	–	Ω	
Transmit timing jitter addition[2]	–	–	±6.4	±10	ns	0 line length for internal MAU
Transmit timing jitter added by the MAU and PLS sections[2, 3]	–	–	±3.5	±5.5	ns	After line model specified by IEEE 802.3 for 10BASE-T internal MAU
Receive input impedance	Z_{IN}	–	24	–	kΩ	Between TPIP/TPIN
Differential squelch threshold	V_{DS}	300	420	585	mV	5 MHz square wave input

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Parameter is guaranteed by design; not subject to production testing.
3. IEEE 802.3 specifies maximum jitter additions at 0.5 ns from the encoder, and 3.5 ns from the MAU.

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Table 9: Switching Characteristics (Over Recommended Range)

Parameter		Symbol	Minimum	Typical[1]	Maximum	Units
Jabber Timing	Maximum transmit time	–	20	–	150	ms
	Unjab time	–	250	–	750	ms
Link Integrity Timing	Time link loss receive	–	50	–	150	ms
	Link min receive	–	2	–	7	ms
	Link max receive	–	50	–	150	ms
	Link transmit period	–	8	10	24	ms

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 10: RCLK/Start-of-Frame Timing (Over Recommended Range)

Parameter		Symbol	Min	Typ[1]	Max	Units
Decoder acquisition time		tDATA	–	1300	1500	ns
CD turn-on delay		tCD	–	400	550	ns
Receive data setup from RCLK	Mode 1	tRDS	60	70	–	ns
	Modes 2, 3 and 4	tRDS	30	45	–	ns
Receive data hold from RCLK	Mode 1	tRDH	10	20	–	ns
	Modes 2, 3 and 4	tRDH	30	45	–	ns
RCLK shut off delay from CD assert (Mode 3)		tsws	–	±100	–	ns

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.

Table 11: RCLK/End-of-Frame Timing (Over Recommended Range)

Parameter	Type	Sym	Mode 1	Mode 2	Mode 3	Mode 4	Units
RCLK after CD off	Min	tRC	5	1	–	5	bit times
Rcv data through-put delay	Max	tRD	400	375	375	375	ns
CD turn-off delay [2]	Max	tCDOFF	500	475	475	475	ns
Receive block out after TEN off [3]	Typical[1]	tIFG	5	50	–	–	bit times
RCLK switching delay after CD off	Typical[1]	tswe	–	–	120 (±80)	–	ns

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. CD Turnoff delay measured from middle of last bit; timing specification is unaffected by the value of the last bit.
3. Blocking of Carrier Detect is disabled during full duplex operation.

Table 12: Transmit Timing (Over Recommended Range)

Parameter	Symbol	Minimum	Typical[1]	Maximum	Units
TEN setup from TCLK	tEHCH	22	–	–	ns
TXD setup from TCLK	tDSCH	22	–	–	ns
TEN hold after TCLK	tCHEL	5	–	–	ns
TXD hold after TCLK	tCHDU	5	–	–	ns
Transmit start-up delay	tSTUD	–	350	450	ns
Transmit through-put delay	tTPD	–	338	350	ns

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.

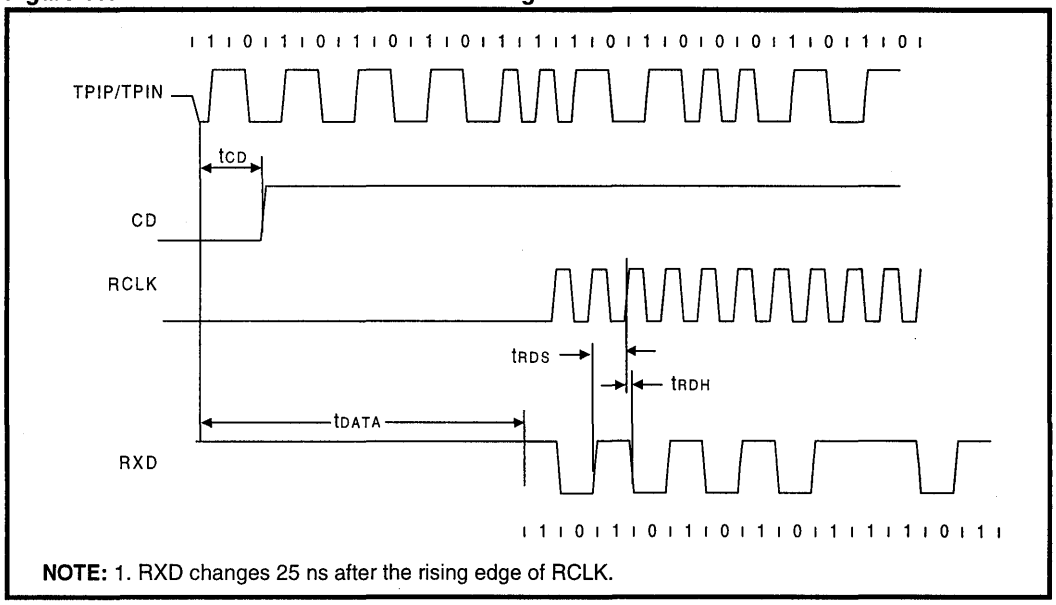
Table 13: Miscellaneous Timing (Over Recommended Range)

Parameter	Symbol	Minimum	Typical[1]	Maximum	Units
COL (SQE) Delay after TEN off [2]	tSQED	0.65	–	1.6	µs
COL (SQE) Pulse Duration[2]	tSQEP	500	–	1500	ns
Power Down recovery time	tPDR	–	25	–	ms

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.
2. When SQE is enabled (DSQE is Low).

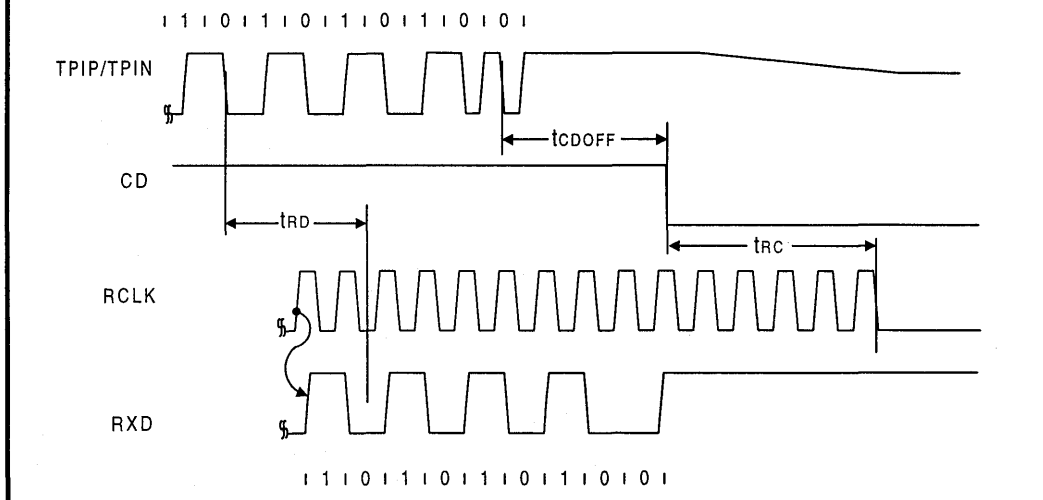
Timing Diagrams for Mode 1 (MD1 = Low, MD0 = Low) *Figures 10 through 13*

Figure 10: Mode 1 RCLK/Start-of-Frame Timing



NOTE: 1. RXD changes 25 ns after the rising edge of RCLK.

Figure 11: Mode 1 RCLK/End-of-Frame Timing



NOTE: 1. RXD changes 25 ns after the rising edge of RCLK.

Figure 12: Mode 1 Transmit Timing

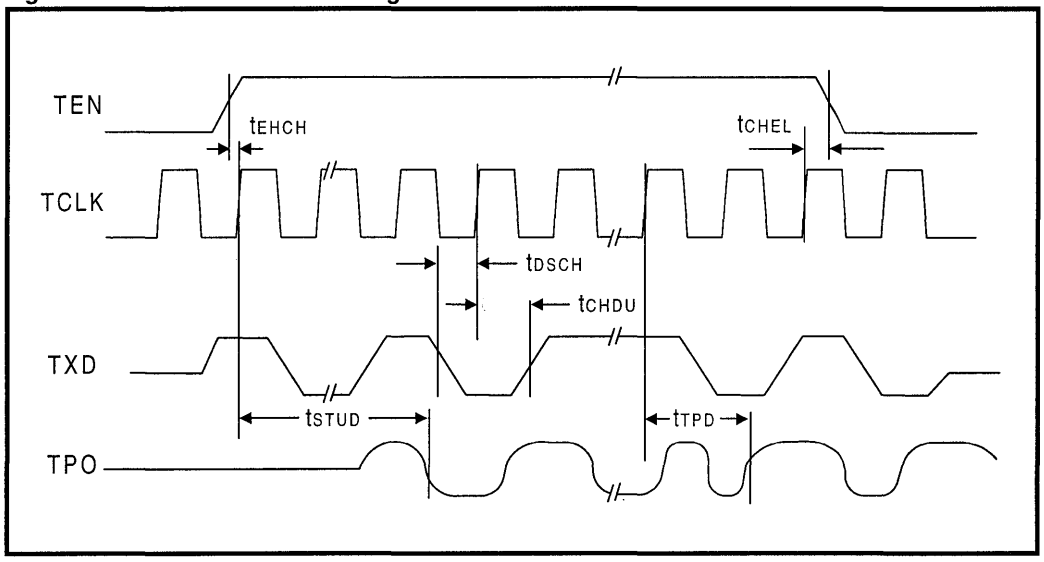
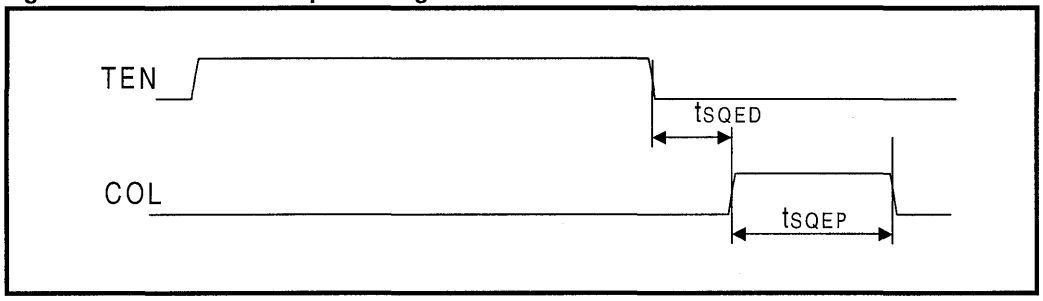
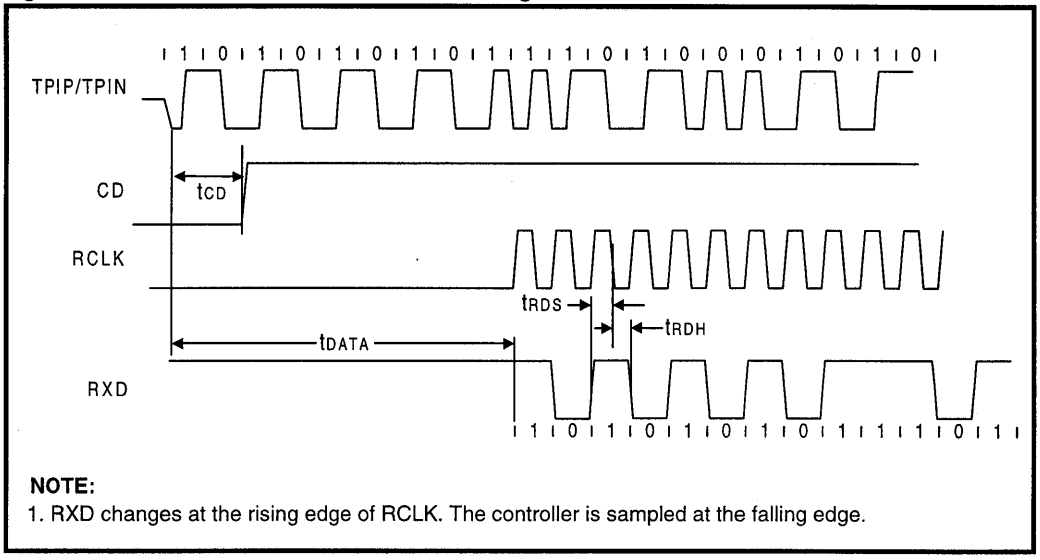


Figure 13: Mode 1 COL Output Timing



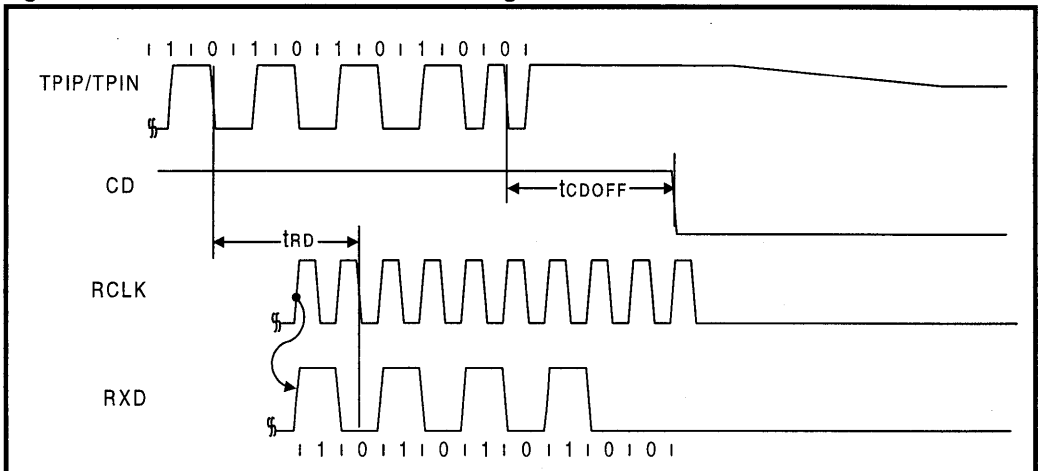
Timing Diagrams for Mode 2 (MD1=Low, MD0=High) *Figures 14 through 17*

Figure 14: Mode 2 RCLK/Start-of-Frame Timing



NOTE:
1. RXD changes at the rising edge of RCLK. The controller is sampled at the falling edge.

Figure 15: Mode 2 RCLK/End-of-Frame Timing



NOTE:
1. RXD changes at the rising edge of RCLK. The controller is sampled at the falling edge.

Figure 16: Mode 2 Transmit Timing

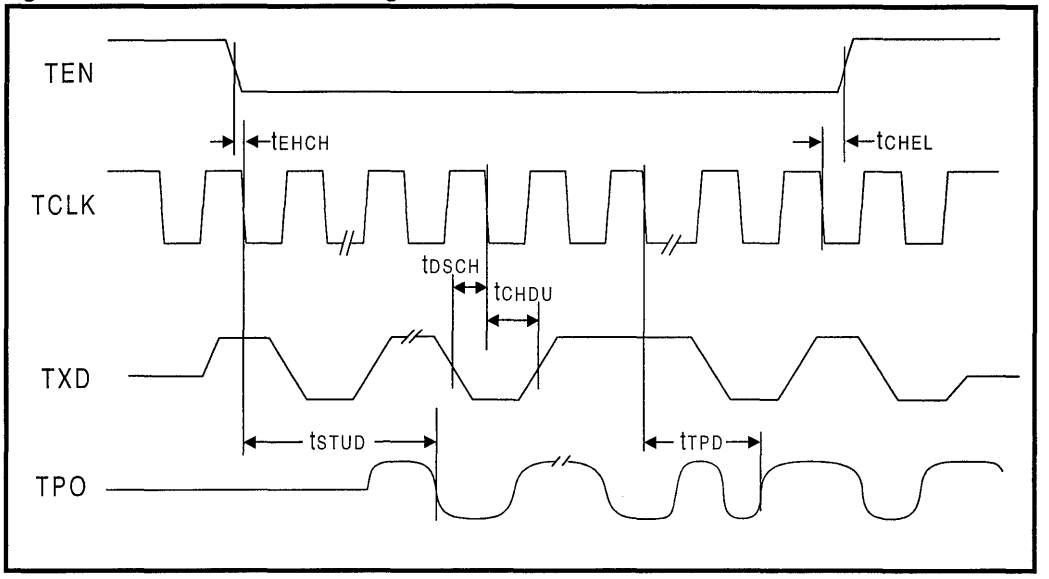
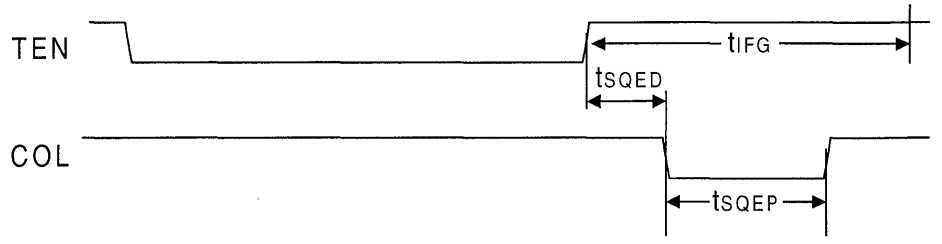


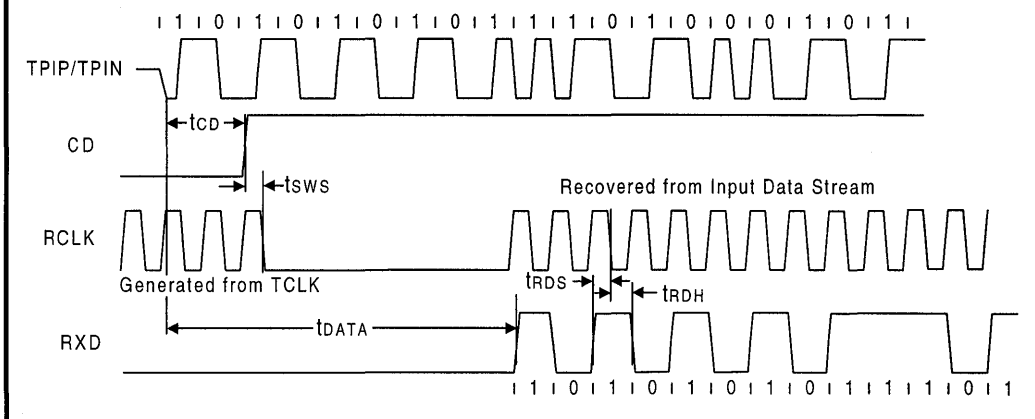
Figure 17: Mode 2 COL Output Timing



NOTE:
1. CD output is disabled for a maximum of 55 bit times after TEN turns off.

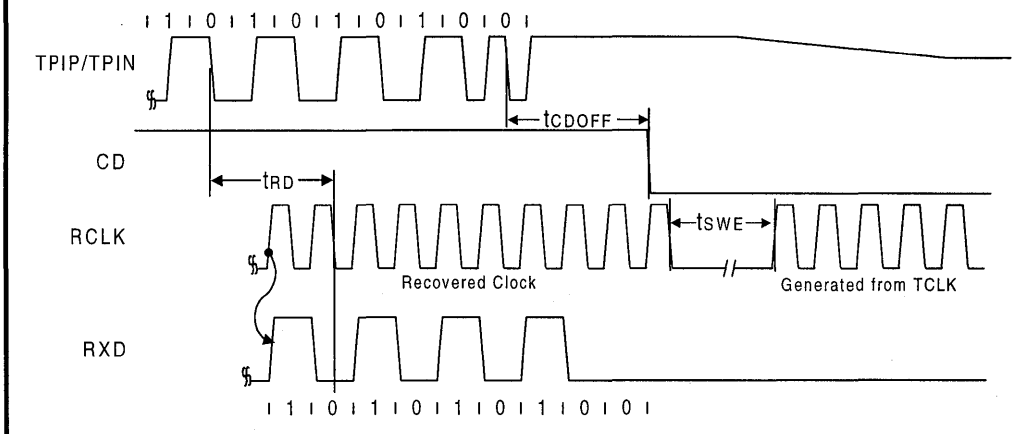
Timing Diagrams for Mode 3 (MD1 = High, MD0 = Low) *Figures 18 through 21*

Figure 18: Mode 3 RCLK/Start-of-Frame Timing



Note:
1. RXD changes at the rising edge of RCLK. The controller is sampled at the falling edge.

Figure 19: Mode 3 RCLK/End-of-Frame Timing



Note:
1. RXD changes at the rising edge of RCLK. The controller is sampled at the falling edge.

Figure 20: Mode 3 Transmit Timing

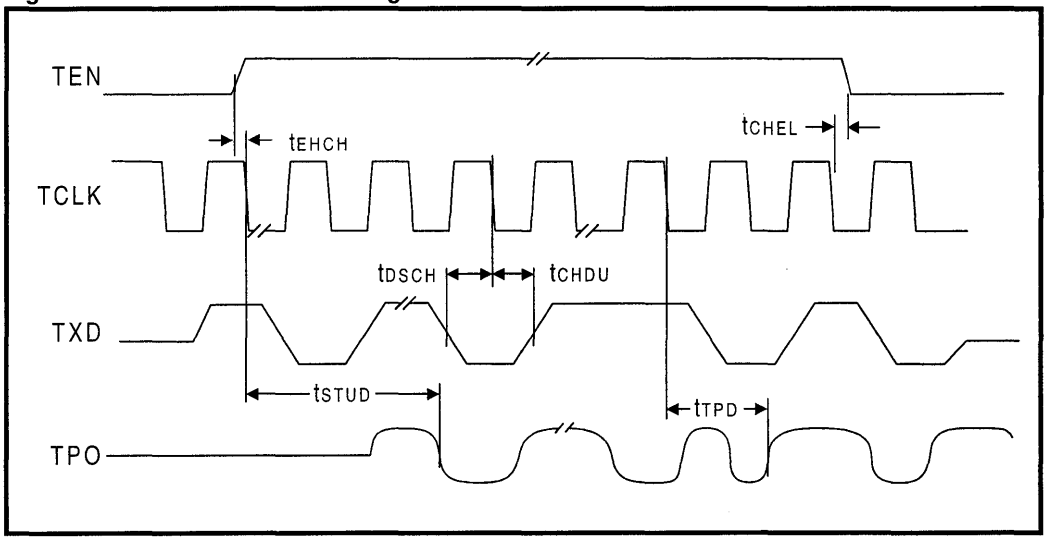
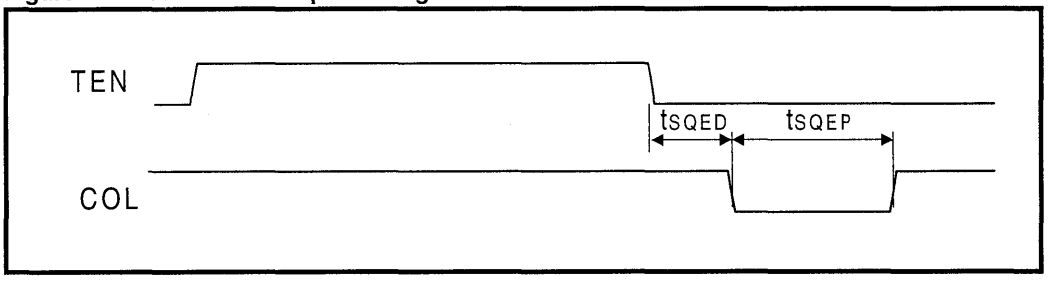
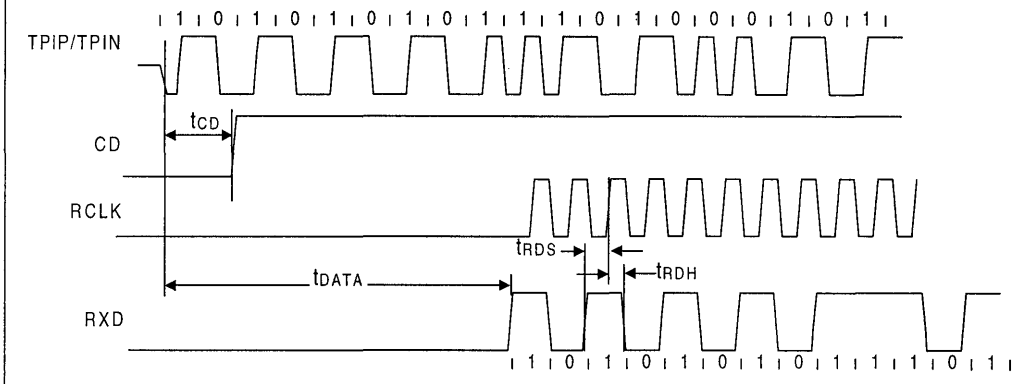


Figure 21: Mode 3 COL Output Timing



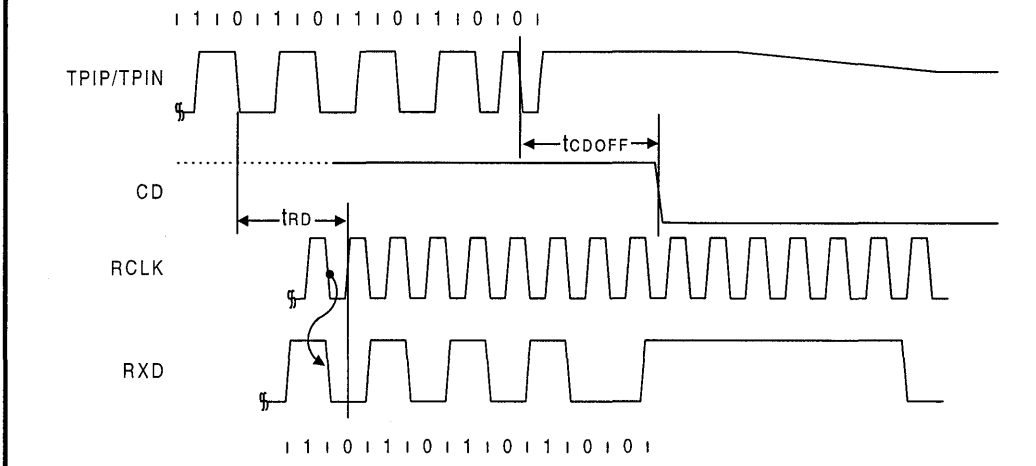
Timing Diagrams for Mode 4 (MD1 = High, MD0 = High) *Figures 22 through 25*

Figure 22: Mode 4 RCLK/Start-of-Frame Timing



Note:
1. RXD changes at the falling edge of RCLK. The controller is sampled at the rising edge.

Figure 23: Mode 4 RCLK/End-of-Frame Timing



Note:
1. RXD changes at the falling edge of RCLK. The controller is sampled at the rising edge.

Figure 24: Mode 4 Transmit Timing

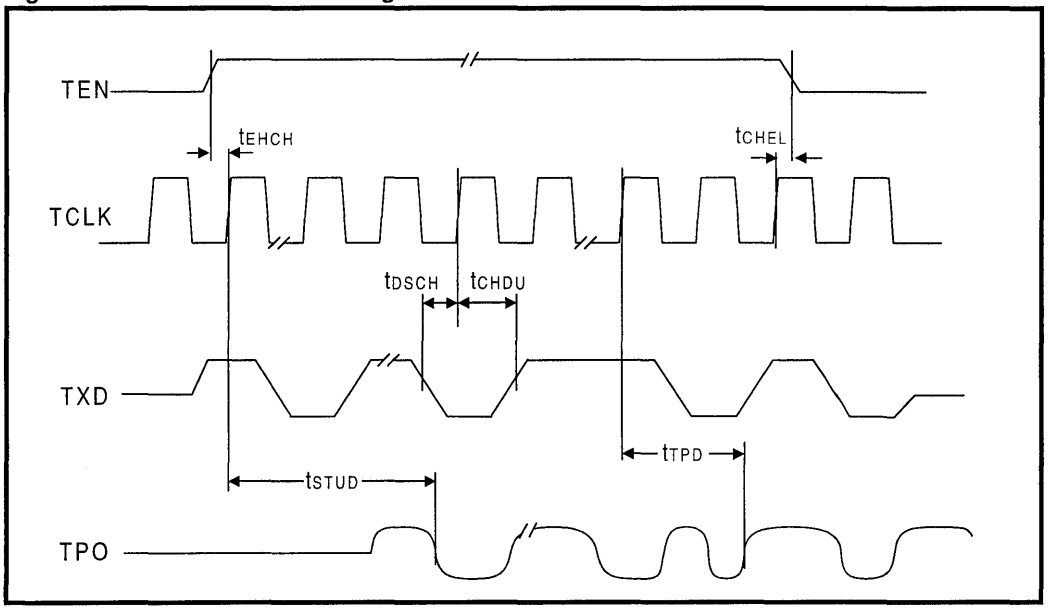
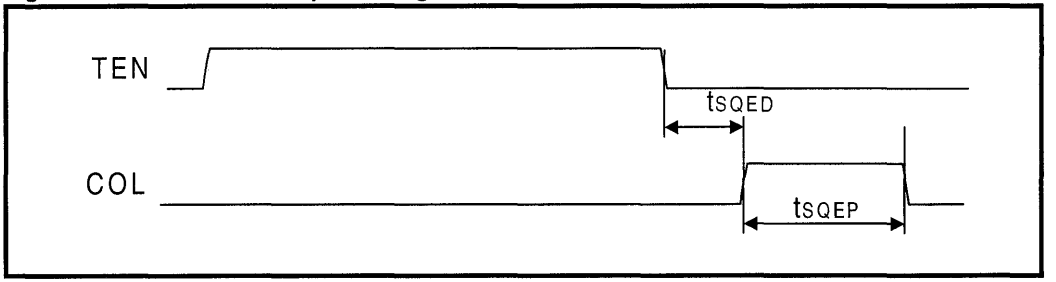


Figure 25: Mode 4 COL Output Timing



NOTES

DATA SHEET

MAY 1997

Revision 2.1

LXT906

Ethernet Twisted-Pair / Coax Adapter

General Description

The LXT906 Twisted-Pair/Coax Adapter is designed to allow a cost effective Ethernet implementation in a mixed media environment. Combined with a coax transceiver such as the DP8392, the LXT906 offers a complete adapter solution.

LXT906 functions include level-shifted data pass-through from one transmission media to another, collision detection and propagation, and automatic correction of polarity reversal on the twisted pair input. It also includes LED drivers for jabber, coax receive and collision, twisted pair receive and collision, reversed polarity detect and link indication functions.

The LXT906 is an advanced CMOS device and requires only a single 5 volt power supply.

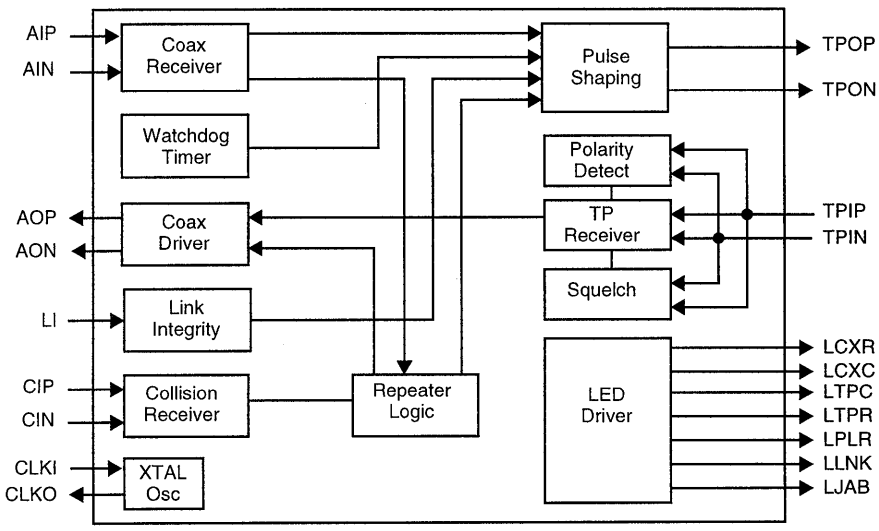
Applications

- 10BASE-T to Coax (10BASE5 or 10BASE2) converter

Features

- Direct interface to Coax transceiver and to RJ45 connector
- Collision detection and propagation
- Internal pre-distortion generation
- Internal common mode voltage generation
- Selectable link test
- Twisted-Pair receive polarity reverse detection and correction
- LED drivers for TP and coax receive; TP and coax collision; jabber, link active and reversed polarity indicators
- Single 5 V supply, CMOS technology
- Available in 28-pin PLCC

LXT906 Block Diagram



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PIN ASSIGNMENTS AND SIGNAL DESCRIPTIONS

Figure 1: LXT906 Pin Assignments

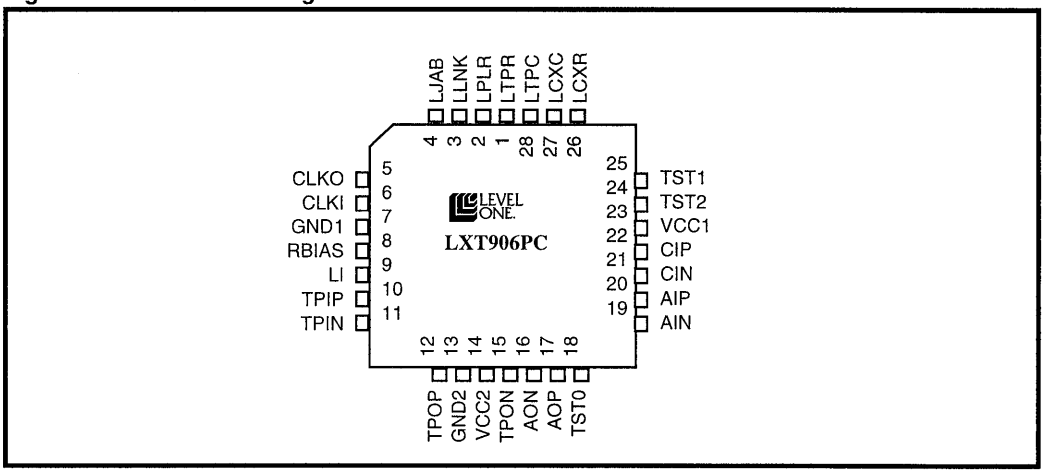


Table 1: LXT906 Signal Descriptions

Pin #	Sym	I/O	Description
1	LTPR	O	**Twisted-Pair Receive LED Driver.** Open drain driver for the TP Receive indicator LED. Output pulls Low whenever TP receiver is active.
2	LPLR	O	**Twisted-Pair Reverse Polarity LED Driver.** Open drain driver for the TP Reversed Polarity indicator LED. Output pulls Low whenever reversed polarity is detected.
3	LLNK	O	**Twisted-Pair Link LED Driver.** Open drain driver for the TP Link indicator LED. Output goes High whenever link is active.
4	LJAB	O	**Jabber LED Driver.** Open drain driver for the Jabber indicator LED. Output pulls Low whenever LXT906 is in a jabber condition.
5 6	CLKO CLKI	O I	**Crystal Oscillator.** The LXT906 requires either a 20 MHz crystal (or ceramic resonator) connected across these pins, or a 20 MHz external clock applied at CLKI with CLKO left unconnected.
7	GND1	–	**Ground 1.** Ground
8	RBIAS	I	**Resistor Bias Control.** Bias control pin for the operating circuit. Bias set from external resistor to ground. External resistor value = 12.4 kΩ (± 1%).
9	LI	I	**Link Integrity.** Enables Link Integrity testing when tied High.
10 11	TPIP TPIN	I I	**Twisted-Pair Receive Inputs.** Differential receive inputs from the twisted-pair input filter.
12 15	TPON TPOP	O O	**Twisted-Pair Transmit Outputs.** Transmit drivers to the twisted-pair output filter. Output data is Manchester encoded and pre-distorted to meet the 10BASE-T template.
13	GND2	–	**Ground 2.** Ground.
14	VCC2	–	**Power Supply 2.** +5 V power supply.

Table 1: LXT906 Signal Descriptions – continued

Pin #	Sym	I/O	Description
16	AON	O	**AUI Out Negative and AUI Out Positive.** Differential driver output pair connected to the Coax AUI.
17	AOP	O	
18	TST0	–	**Test Pin 0.** Test pin for factory use. *This pin must be left unconnected.*
19	AIN	I	**AUI In Negative and AUI In Positive.** Data input pair from the Coax AUI.
20	AIP	I	
21	CIN	I	**Collision Input Negative and Collision Input Positive.** Differential input pair tied to the collision presence pair of the Ethernet Coax transceiver.
22	CIP	I	
23	VCC1	–	**Power Supply 1.** +5 V power supply.
24	TST2	–	**Test Pin 2 and Test Pin 1.** Test pins reserved for factory use. *These pins must be left unconnected.*
25	TST1	–	
26	LCXR	O	**Coax (AUI) Receive LED Driver.** Open drain driver for the Coax Receive indicator LED. Pulls Low whenever coax receiver is active.
27	LCXC	O	**Coax Collision LED Driver.** Open drain driver for the Coax Collision indicator LED. Pulls Low whenever a collision is detected on the coax circuit.
28	LTPC	O	**TP Collision LED Driver.** Open drain driver for the TP Collision indicator LED. Pulls Low whenever a collision is detected on the TP lines.

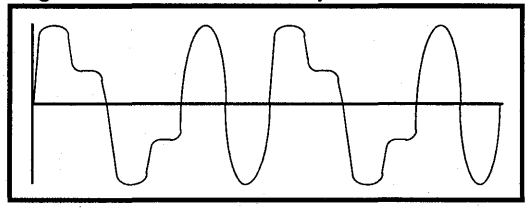
FUNCTIONAL DESCRIPTION

The LXT906 interfaces the coaxial transceiver (AUI) to the unshielded twisted-pair cables, allowing data transfer in both directions. The AUI side of the interface is comprised of three circuits: Data Input (AIP and AIN to the coax receiver), Data Output (AOP and AON from the coax driver), and Collision Interface (CIP and CIN to the collision receiver). The twisted-pair (TP) network side of the interface is comprised of two circuits: TP Output (TPOP and TPON from the pulse shaper) and TP Input (TPIP and TPIN to the TP receiver). In addition to these five basic circuits, the LXT906 contains crystal oscillator circuitry, various logic controls and seven LED drivers for status indications.

Coax to TP Function

The LXT906 receives data from the coax transceiver (via AIP and AIN) and re-transmits it to the twisted-pair (TP) network on the TP Output circuit. The TP Output signal (on TPON and TPOP) is pre-distorted to meet the 10BASE-T jitter template. The output waveform (after the transmit filter) is shown in Figure 2. If the differential inputs (AIP and AIN) fall below 75% of the threshold level for 8 bit times (typical), the LXT906 TP transmit function will enter the idle state. During idle periods, the LXT906 transmits link integrity test pulses on TPOP and TPON.

Figure 2: LXT906 TPO Output Waveform.



TP to Coax Function

The LXT906 receives data from the twisted-pair (TP) network on the TP Input circuit and re-transmits it to the coax transceiver on the AO circuit. An internal squelch function discriminates noise from link test pulses and valid data streams. Only valid data streams activate the TP receive function. If the differential inputs at the TP Input circuit fall below 75% of the threshold level (unsquelched) for 8 bit times (typical), the LXT906 TP receive function will enter the idle state. The Coax-to-TP data path is disabled when the TP-to-Coax path is active. The Coax-to-TP path is enabled 9 bit times after the end of TP-to-Coax transmission.

Polarity Reverse Function

The LXT906 polarity reverse function uses both link pulses and end-of-frame data to determine the polarity of the received signal. A reversed polarity condition is detected when eight link pulses of the opposite (unexpected) polarity are received without receipt of a link pulse with the expected polarity. Reversed polarity is also detected if four frames are received with a reversed start-of-idle. If the LXT906 enters the link fail state and no data or link pulses are received within 96 to 128 ms, the polarity is reset to the default (non-flipped) condition. Note that if the Link Integrity function is disabled, polarity detection is based only upon received data pulses. The LXT906 automatically corrects for reversed polarity.

Jabber Function

A Jabber condition is detected when the LXT906 has transmitted continuously for longer that 5 ms on TPOP/TPON or AOP/AON. If this occurs, the repeater state machine and output data transmission are disabled, and the Jabber LED signal (LJAB) goes Low. Transmission is re-enabled when no activity has been detected on TPIP/TPIN or AIP/AIN for 6.4 µs.

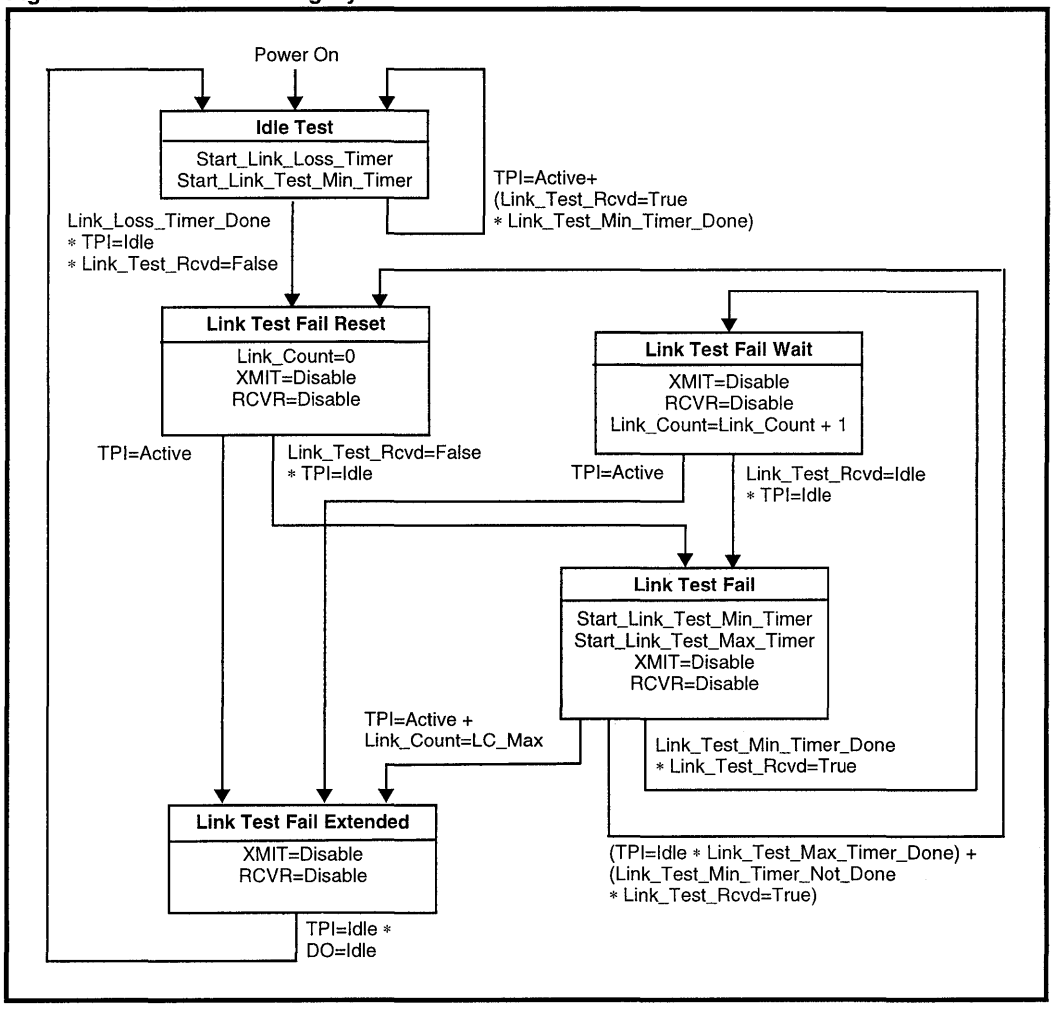
Link Integrity Test Function

Figure 3 is a state diagram of the LXT906 Link Integrity Test Function. The Link Integrity Test is used to determine the status of the twisted-pair cable. Link integrity testing is enabled when the LI pin is tied High. When enabled, the receiver recognizes link integrity pulses which are transmitted in the absence of receive traffic. If no serial data stream or link integrity pulses are detected within 50 - 150 ms, the chip enters a link-fail state and disables the transmit function and the repeater state machine. The LXT906 ignores any link integrity pulse with an interval of less than 2 - 7 ms. The LXT906 will remain in the link fail state until it detects either a serial data packet or two or more link integrity pulses.

Collision Propagation Function

A TP collision is defined as the simultaneous presence of valid signals on both the TP Input circuit and the TP Output circuit. A Coax collision is detected when a valid collision signal is present at CIP/CIN. If a collision is detected, the appropriate collision LED (TP or coax) is activated and a Jam frame is transmitted as described in Figure 4. The Jam length is always a minimum of 96 bits: 64 bits of alternating 1's and 0's, followed by an all 1's pattern.

Figure 3: LXT906 Link Integrity Test Function



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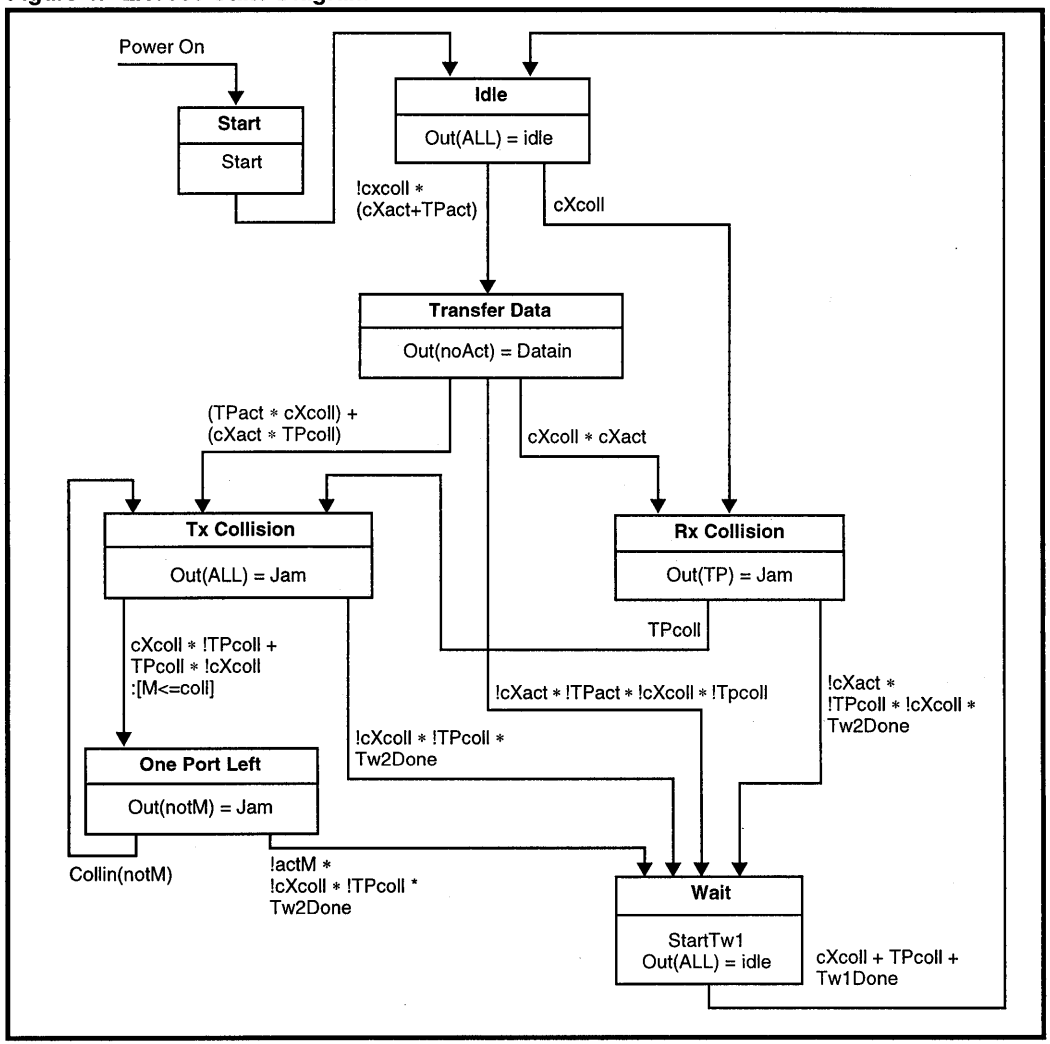
LXT906 State Diagram

The state diagram, shown in Figure 4, describes the operation of the LXT906. It is similar to a repeater state diagram, however the LXT906 does not provide re-timing, preamble regeneration or fragment extension. The LXT906 avoids fragment generation by using a minimum Jam size of 96 bits. Since the TP side does not have receive collision detection, it is not considered in this implementation.

State Diagram Variables

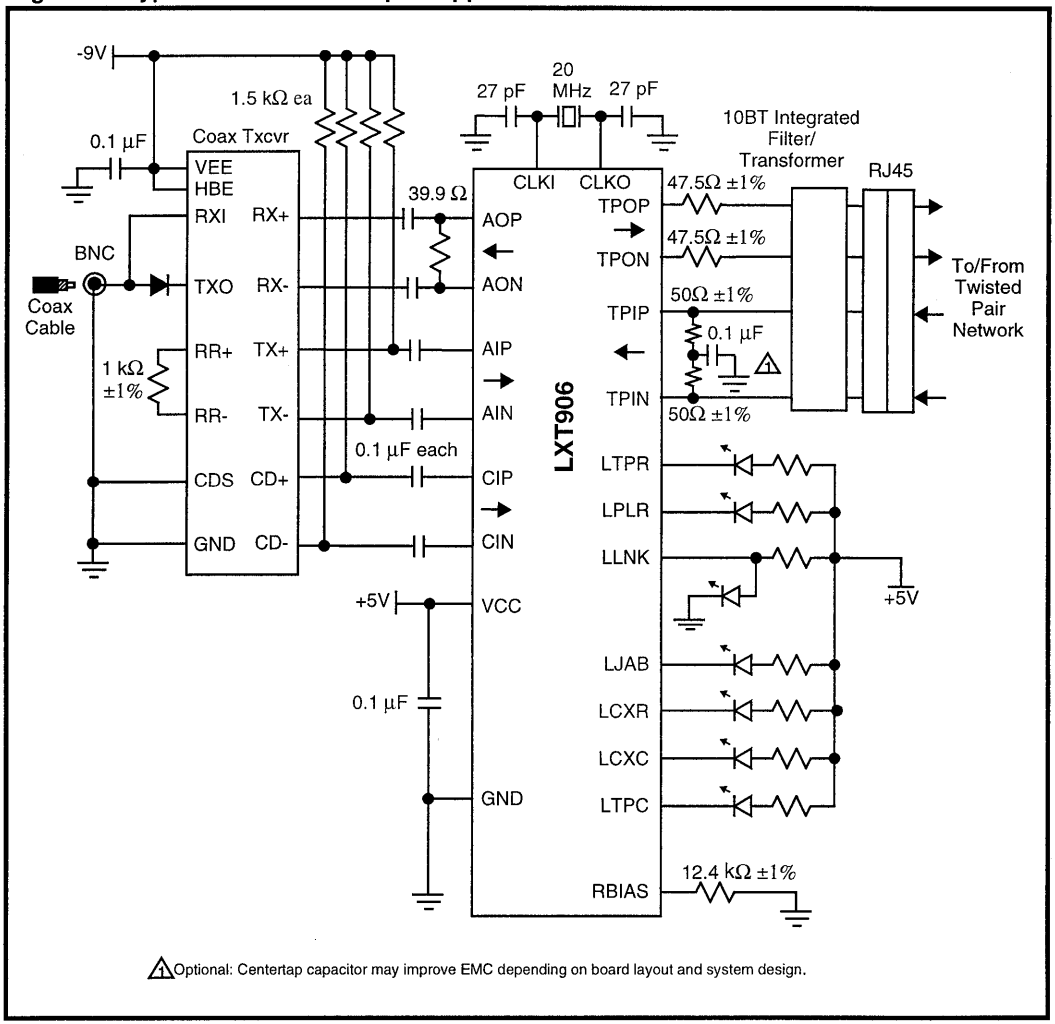
cXcoll = Coax collision active
TPcoll = TP collision active
cXact = Coax data active
TPact = TP data active
Tw1 = 9 bit times
Tw2 = 3 bit times
Jam = Minimum 96 bit times

Figure 4: LXT906 State Diagram



APPLICATION INFORMATION

Figure 5: Typical TP to Coax Adapter Application Circuit



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TEST SPECIFICATIONS

NOTE

The minimum and maximum values in Table 2 through 8 represent the performance specifications of the LXT906 and are guaranteed by test except, where noted, by design.

Table 2: Absolute Maximum Values

Parameter	Symbol	Min	Max	Units
Supply voltage	VCC	-0.3	6	V
Ambient operating temperature	TA	0	70	°C
Storage temperature	TSTG	-65	+150	°C

CAUTION

Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 3: Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Recommended supply voltage	VCC	4.75	5.0	5.25	V	
Recommended operating temperature	TOP	0	–	70	°C	

Table 4: I/O Electrical Characteristics (Over Recommended Range)

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Input Low voltage	VIL	–	–	0.8	V	–
Input High voltage	VIH	2.0	–	–	V	–
Output Low voltage (Open drain LED driver)	VOLL	–	–	0.7	V	IOLL = 10 mA
Supply Current (Vcc1=Vcc2=5.25 V)	ICC	–	60	80	mA	Line Idle
		–	125	150	mA	Line Active, transmitting all ones
Input Leakage Current[2]	ILL	–	±1	50	µA	Input between Vcc and GND

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Not including TPIN, TPIP, AIP, AIN, CIP, or CIN.

Table 5: AUI Electrical Characteristics (Over Recommended Range)

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Input Low current	I_{IL}	–	–	-700	µA	–
Input High current	I_{IH}	–	–	500	µA	–
Differential output voltage	V_{OD}	±550	–	±1200	mV	–
Differential squelch threshold	V_{DS}	–	220	–	mV	–
Receive input impedance	RZ	–	20	–	kΩ	Between AIP and AIN, and between CIP and CIN.

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 6: Switching Characteristics (Over Recommended Range)

Parameter		Min	Typ[1]	Max	Units
Jam Timing	Transmit time	96	–	–	bit
Link Integrity Timing	Time link loss[2]	65	–	66	ms
	Time between Link Integrity Pulses[2]	9	–	11	ms
	Interval for valid receive Link Integrity Pulses[2]	3.9	–	65	ms
Collision Timing	End of collision to end of jam	–	–	1200	ns
Jabber Timing	Maximum transmit time	–	–	5.1	ms
	Unjab time	–	6.4	–	µs
LED Timing	LED on time	100	–	–	ms
General Timing	Transmit recovery time	–	–	12	bit
	Carrier recovery time	–	–	3	bit
	TP receive to AUI transmit	0	–	500	ns
	AUI receive to TP transmit	0	–	200	ns

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Switching times reduced by a factor of 1024 during Test mode.

Table 7: Twisted-Pair Transmit Characteristics (Over Recommended Range)

Parameter	Sym	Minimum	Typical[1]	Maximum	Units	Test Conditions
Transmit output impedance	ZOUT	–	5	–	Ω	–
Transmit timing jitter addition[2]	–	–	–	±8	ns	After Tx filter, 0 line length

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.
2. Parameter is guaranteed by design; not subject to production testing.

Table 8: Twisted-Pair Receive Characteristics (Over Recommended Range)

Parameter	Sym	Minimum	Typical[1]	Maximum	Units	Test Conditions
Receive input impedance	ZIN	–	20	–	kΩ	Between TPIP/TPIN
Differential squelch threshold	VDS	–	420	–	mV	–
Receive timing jitter addition[2]	–	–		1.5	ns	–

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.
2. Parameter is guaranteed by design; not subject to production testing.

DATA SHEET

LXT908

APRIL 1997
Revision 1.0

Universal Ethernet Interface Adapter

General Description

The LXT908 Universal Ethernet Interface Adapter is designed for IEEE 802.3 physical layer applications. It provides all the active circuitry to interface most standard 802.3 controllers to either the 10BASE-T media or Attachment Unit Interface (AUI). In addition to standard 10 Mbps Ethernet, the LXT908 also supports full-duplex operation at 20 Mbps.

LXT908 functions include Manchester encoding/decoding, receiver squelch and transmit pulse shaping, jabber, link testing and reversed polarity detection/correction. The LXT908 can be used to drive either the AUI drop cable or the 10BASE-T twisted-pair cable with only a simple isolation transformer. Integrated filters simplify the design work required for FCC compliant EMI performance.

The LXT908 is fabricated with an advanced CMOS process and requires only a single 3.3 or 5 volt power supply.

Applications

- 10BASE-T Hub and Switching products
- Computer/workstation 10BASE-T LAN adapter boards

Features

Functional Features

- Improved Filters - Simplifies FCC Compliance
- Integrated Manchester Encoder/Decoder
- 10BASE-T compliant Transceiver
- AUI Transceiver
- Supports Standard and Full-Duplex Ethernet

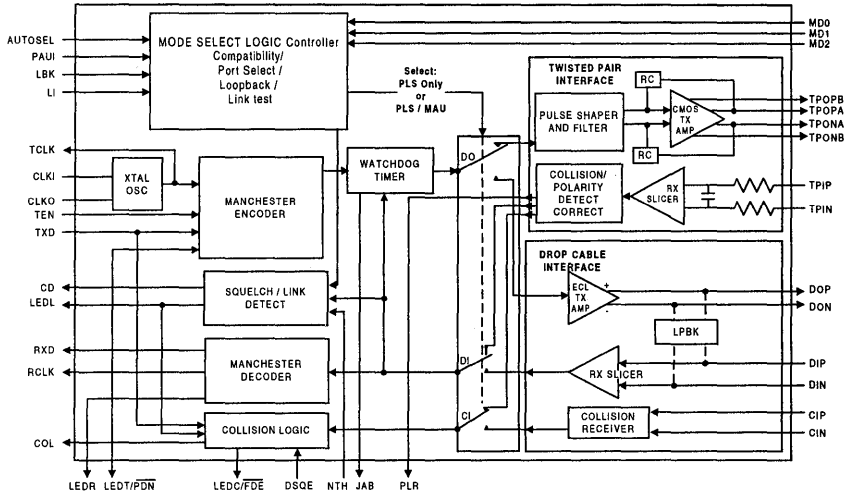
Convenience Features

- Automatic/Manual AUI/RJ45 Selection
- Automatic Polarity Correction
- SQE Disable/Enable function
- Power Down Mode with tristated outputs
- Four loopback modes
- Single 3.3V or 5V operation
- Available in 44-pin PLCC package

Diagnostic Features

- Four LED Drivers
- AUI/RJ45 Loopback

LXT908 Block Diagram



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PIN ASSIGNMENTS AND SIGNAL DESCRIPTIONS

Figure 1: LXT908 Pin Assignments

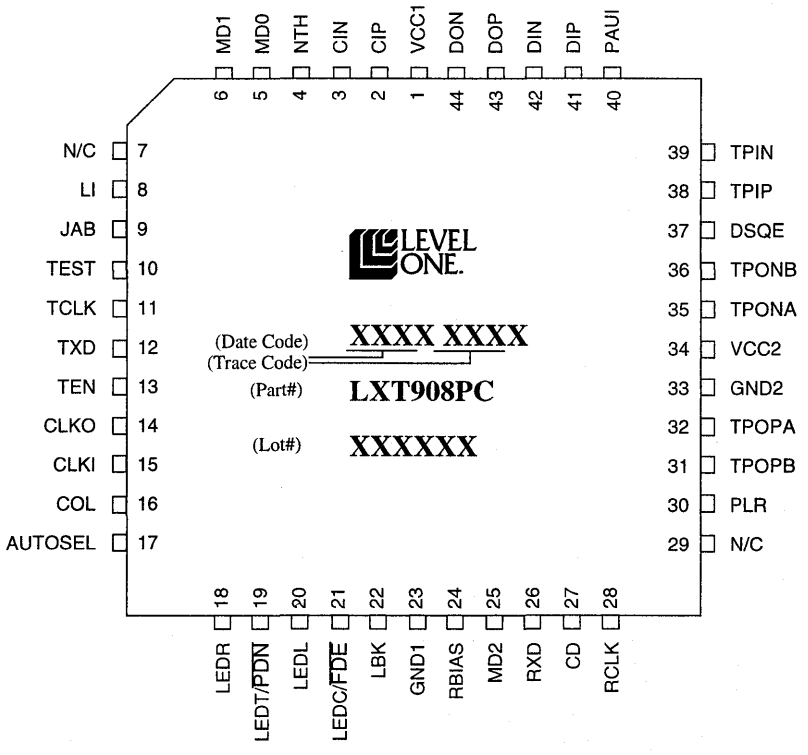


Table 1: LXT908 Signal Descriptions

Pin #	Symbol	I/O	Description
1 34	VCC1 VCC2	- -	**Power 1 and 2.** Connect to positive power supply terminal (+3.3VDC or +5 VDC).
2 3	CIP CIN	I I	**AUI Collision Pair.** Differential input pair connected to the AUI transceiver CI circuit. The input is collision signaling or SQE.
4	NTH	I	**Normal Threshold.** When NTH is High, the normal TP squelch threshold is in effect. When NTH is Low, the normal TP squelch threshold is reduced by 4.5 dB.
5 6 25	MD0 MD1 MD2	I I I	**Mode Select 0 (MD0), Mode Select 1 (MD1) and Mode Select 2 (MD2).** Mode select pins determine the controller compatibility mode as specified in Table 2.
7	N/C	-	**No Connect.** *This pin must be tied to ground or device damage may occur.*
8	LI	I	**Link Test Enable.** Controls Link Integrity Test; enabled when High, disabled when Low.
9	JAB	O	**Jabber Indicator.** Output goes High to indicate Jabber state.
10	TEST	I	**Test.** *This pin must be tied High.*
11	TCLK	O	**Transmit Clock.** A 10 MHz clock output. This clock signal should be directly connected to the transmit clock input of the controller. TCLK goes to high impedance (tri-state) when LEDT/$\overline{\text{PDN}}$ is pulled Low externally.
12	TXD	I	**Transmit Data.** Input signal containing NRZ data to be transmitted on the network. TXD is connected directly to the transmit data output of the controller.
13	TEN	I	**Transmit Enable.** Enables data transmission and starts the watchdog timer. Synchronous to TCLK (see Test Specifications for details).
14 15	CLKO CLKI	O I	**Crystal Oscillator.** A 20 MHz crystal must be connected across these pins, or a 20 MHz clock applied at CLKI with CLKO left open.
16	COL	O	**Collision Detect.** Output which drives the collision detect input of the controller. COL goes to high impedance (tri-state) when LEDT/$\overline{\text{PDN}}$ is pulled Low externally.
17	AUTOSEL	I	**Automatic Port Select.** When High, automatic port selection is enabled (the LXT908 defaults to the AUI port only if TP link integrity = Fail). When Low, manual port selection is enabled (the PAUI pin determines the active port).
18	LEDR	O	**Receive LED.** Open drain driver for the receive indicator LED. Output is pulled Low during receive, except when data is being looped back to DIN/DIP from a remote transceiver (external MAU). LED "On" time (i.e., Low output) is extended by approximately 100 ms.
19	LEDT/ $\overline{\text{PDN}}$	O I	**Transmit LED (LEDT)/Power Down ($\overline{\text{PDN}}$).** Open drain driver for the transmit indicator LED. Output is pulled Low during transmit. LED "On" time (i.e., Low output) is extended by approximately 100 ms. If externally tied Low, the LXT908 goes to power down state. In power down state, TCLK, COL, RXD, CD and RCLK (pins 11, 16, 26, 27 and 28, respectively) are tri-stated.
20	LEDL	O I	**Link LED.** Open drain driver for link integrity indicator LED. Output is pulled Low during link test pass. If externally tied Low, internal circuitry is forced to "Link Pass" state and the LXT908 will continue to transmit link test pulses.

Table 1: LXT908 Signal Descriptions – continued

Pin #	Symbol	I/O	Description
21	LEDC/ $\overline{\text{FDE}}$	O I	**Collision LED (LEDC)/Full Duplex Enable ($\overline{\text{FDE}}$).** Open drain driver for the collision indicator LED pulls Low during collision. LED "On" time (i.e., Low output) is extended by approximately 100 ms. If externally tied Low, the LXT908 disables the internal TP loopback and collision detection circuits to allow full duplex operation or external TP loopback.
22	LBK	I	**Loopback.** Enables internal loopback mode. Refer to Functional Description and Test Specifications for details.
23 33	GND1 GND2	– –	**Ground Returns 1 and 2.** Connect to negative power supply terminal (ground).
24	RBIAS	I	**Bias Control.** A 12.4 kΩ 1% resistor to ground at this pin controls operating circuit bias.
26	RXD	O	**Receive Data.** Output signal connected directly to the receive data input of the controller. RXD goes to high impedance (tri-state) when LEDT/$\overline{\text{PDN}}$ is pulled Low externally.
27	CD	O	**Carrier Detect.** An output to notify the controller of activity on the network. CD goes to high impedance (tri-state) when LEDT/$\overline{\text{PDN}}$ is pulled Low externally.
28	RCLK	O	**Receive Clock.** A recovered 10 MHz clock which is synchronous to the received data and connected to the controller receive clock input. RCLK goes to high impedance (tri-state) when LEDT/$\overline{\text{PDN}}$ is pulled Low externally.
29	N/C	-	**No Connect.** *This pin must be tied to ground or device damage may occur.*
30	PLR	O	**Polarity Reverse.** Output goes High to indicate reversed polarity at the TP input.
32 31 35 36	TPOPA TPOPB TPONA TPONB	O O O O	**Twisted-Pair Transmit Pairs A & B.** Two differential driver pair outputs (A and B) to the twisted-pair cable.The outputs are pre-equalized. Each pair must be shorted together with an 11.5 Ω 1% resistor to match an impedance of 100Ω.
37	DSQE	I	**Disable SQE.** When DSQE is High, the SQE function is disabled. When DSQE is Low, the SQE function is enabled. SQE must be disabled for normal operation in Hub/Switch applications.
38 39	TPIP TPIN	I I	**Twisted-Pair Receive Pair.** A differential input pair from the TP cable. Receive filter is integrated on-chip. No external filters are required.
40	PAUI	I	**Port/AUI Select.** In Manual Port Select mode (AUTOSEL Low), PAUI selects the active port. When PAUI is High, the AUI port is selected. When PAUI is Low, the TP port is selected. In Auto Port Select mode, PAUI must be tied to ground.
41 42	DIP DIN	I I	**AUI Receive Pair.** Differential input pair from the AUI transceiver DI circuit. The input is Manchester encoded.
43 44	DOP DON	O O	**AUI Transmit Pair.** A differential output driver pair for the AUI transceiver cable. The output is Manchester encoded.

FUNCTIONAL DESCRIPTION

Introduction

The LXT908 Universal Ethernet Interface Transceiver performs the physical layer signaling (PLS) and Media Attachment Unit (MAU) functions as defined by the IEEE 802.3 specification. It functions as an AUI (PLS-Only device) for use with 10BASE-2 or 10BASE-5 coaxial cable networks, or as an Integrated PLS/MAU for use with 10BASE-T twisted-pair networks. In addition to standard 10 Mbps operation, the LXT908 also supports full-duplex 20 Mbps operation.

The LXT908 interfaces a back end controller to either an AUI drop cable or a twisted-pair (TP) cable. The controller interface includes transmit and receive clock and NRZ data channels, as well as mode control logic and signaling. The AUI interface comprises three circuits: Data Output (DO), Data Input (DI) and Collision (CI). The twisted-pair interface comprises two circuits: Twisted-Pair Input (TPI) and Twisted-Pair Output (TPO). In addition to the three basic interfaces, the LXT908 contains an internal crystal oscillator and four LED drivers for visual status reporting.

Functions are defined from the back end controller side of the interface. The LXT908 Transmit function refers to data transmitted by the back end to the AUI cable (PLS-Only mode) or to the twisted-pair network (Integrated PLS/ MAU mode). The LXT908 Receive function refers to data received by the back end from the AUI cable (PLS-Only) or from the twisted-pair network (Integrated PLS/MAU mode). In the integrated PLS/MAU mode, the LXT908 performs all required MAU functions defined by the IEEE 802.3 10BASE–T specification such as collision detection, link integrity testing, signal quality error messaging, jabber control and loopback. In the PLS-Only mode, the LXT908 receives incoming signals from the AUI DI circuit with ± 18ns of jitter and drives the AUI DO circuit.

Controller Compatibility Modes

The LXT908 is compatible with most industry standard controllers including devices produced by Advanced Micro Devices (AMD), Motorola, Intel, Fujitsu, National Semiconductor, Seeq and Texas Instruments, as well as custom controllers. Five different control signal timing and polarity schemes (Modes 1 through 5) are required to achieve this compatibility. Mode select pins (MD2:0) determine Controller compatibility modes as listed in Table 2. Refer to Test Specifications for a complete set of timing diagrams for each mode.

Transmit Function

The LXT908 receives NRZ data from the controller at the TXD input as shown in the block diagram on the first page of this Data Sheet, and passes it through a Manchester encoder. The encoded data is then transferred to either the AUI cable (the DO circuit) or the twisted-pair network (the TPO circuit). The advanced integrated pulse shaping and filtering network produces the output signal on TPON and TPOP, shown in Figure 2. The TPO output is pre-distorted and pre-filtered to meet the 10BASE-T jitter template. An internal continuous resistor-capacitor filter is used to remove any high-frequency clocking noise from the pulse shaping circuitry. Integrated filters simplify the design work required for FCC-compliant EMI performance. During idle periods, the LXT908 transmits link integrity test pulses on the TPO circuit (if LI is enabled and integrated PLS/ MAU mode is selected). External resistors control the termination impedance.

Figure 2: LXT908 TPO Output Waveform

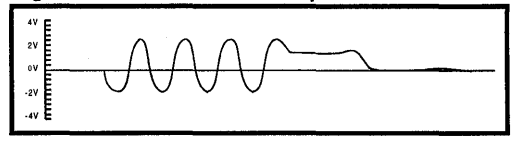


Table 2: Controller Compatibility Mode Options

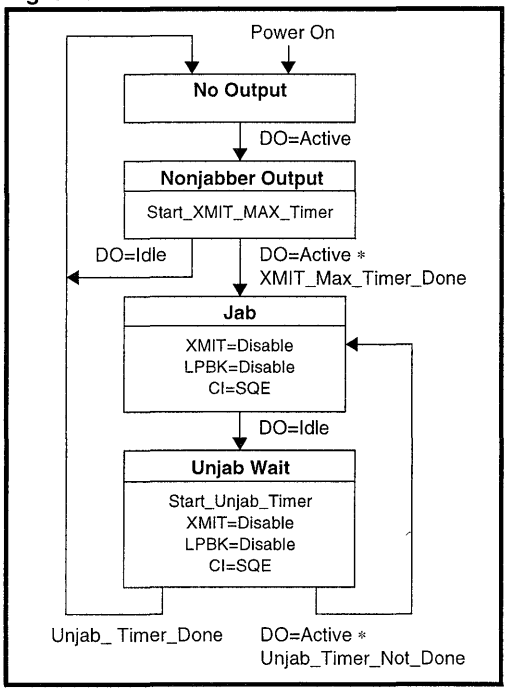
Controller Mode	MD2	MD1	MD0
Mode 1 - For AMD AM7990, Motorola 68EN360, MPC860 or compatible controllers	Low	Low	Low
Mode 2 - For Intel 82596 or compatible controllers	Low	Low	High
Mode 3 - For Fujitsu MB86950, MB86960 or compatible controllers (Seeq 8005)[1]	Low	High	Low
Mode 4 - For National Semiconductor 8390 or compatible controllers (TI TMS380C26)	Low	High	High
Mode 5 - For custom controllers (Mode 3 with TCLK, RCLK and COL inverted)	High	High	Low

1. SEEQ controllers require inverters on CLKI, LBK, RCLK and COL in Mode 3; or on CLKI, LBK and TCLK in Mode 5.

Jabber Control Function

Figure 3 is a state diagram of the LXT908 Jabber control function. The LXT908 on-chip watchdog timer prevents the DTE from locking into a continuous transmit mode. When a transmission exceeds the time limit, the watchdog timer disables the transmit and loopback functions, and activates the JAB pin. Once the LXT908 is in the jabber state, the TXD circuit must remain idle for a period of 0.25 to 0.75 seconds before it will exit the jabber state.

Figure 3: Jabber Control Function



Receive Function

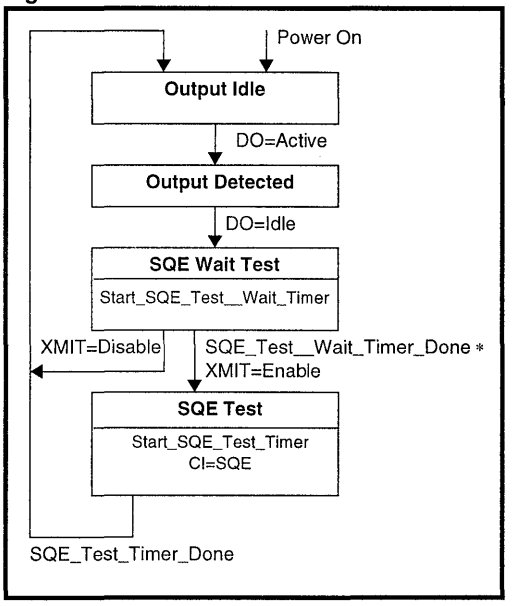
The LXT908 receive function acquires timing and data from the twisted-pair network (the TPI circuit) or from the AUI (the DI circuit). Valid received signals are passed through the on-chip filters and Manchester decoder then output as decoded NRZ data and recovered clock on the RXD and RCLK pins, respectively.

An internal RC filter and an intelligent squelch function discriminate noise from link test pulses and valid data streams. The receive function is activated only by valid data streams above the squelch level and with proper timing. If the differential signal at the TPI or the DI circuit inputs falls below 75% of the threshold level (unsquelched) for 8 bit times (typical), the LXT908 receive function enters the idle state. If the polarity of the TPI circuit is reversed, LXT908 detects the polarity reverse and reports it via the PLR output. The LXT908 automatically corrects reversed polarity.

SQE Function

In the integrated PLS/MAU mode, the LXT908 supports the signal quality error (SQE) function as shown in Figure 4, although the SQE function can be disabled. After every successful transmission on the 10BASE-T network when SQE is enabled, the LXT908 transmits the SQE signal for 10BT ± 5BT over the internal CI circuit which is indicated on the COL pin of the device. SQE must be disabled for normal operation in hub and switch applications. In twisted-pair applications, the SQE function is disabled when DSQE is set High, and enabled when DSQE is Low. When using the 10BASE-2 port of the LXT908, the SQE function is determined by the external MAU attached.

Figure 4: SQE Function



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Polarity Reverse Function

The LXT908 polarity reverse function uses both link pulses and end-of-frame data to determine polarity of the received signal. A reversed polarity condition is detected when eight opposite receive link pulses are detected without receipt of a link pulse of the expected polarity. Reversed polarity is also detected if four frames are received with a reversed start-of-idle. Whenever a correct polarity frame or a correct link pulse is received, these two counters are reset to zero. If the LXT908 enters the link fail state and no valid data or link pulses are received within 96 to 128 ms, the polarity is reset to the default non-flipped condition. (If Link Integrity Testing is disabled, polarity detection is based only on received data.). Polarity correction is always enabled.

Loopback Function

The LXT908 provides the normal loopback function specified by the 10BASE-T standard for the twisted-pair port. The loopback function operates in conjunction with the transmit function. Data transmitted by the back-end is internally looped back within the LXT908 from the TXD pin through the Manchester encoder/decoder to the RXD pin and returned to the back-end. This "normal" loopback function is disabled when a data collision occurs, clearing the RXD circuit for the TPI data. Normal loopback is also disabled during link fail and jabber states.

The LXT908 also provides three additional loopback functions. An external loopback mode, useful for system-level testing, is controlled by pin 21 (LEDC). When LEDC is tied Low, the LXT908 disables the collision detection and internal loopback circuits, to allow external loopback or full-duplex operation.

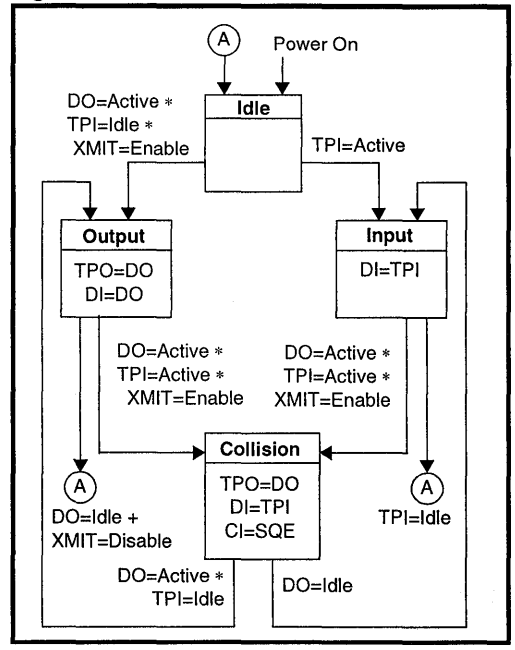
"Normal" TP loopback is controlled by pin 22 (LBK). When the TP port is selected and LBK is High, TP loopback is "forced", overriding collisions on the TP circuit. When LBK is Low, normal loopback is in effect.

AUI loopback is also controlled by the LBK pin. When the AUI port is selected and LBK is High, data transmitted by the back-end is internally looped back from the TXD pin through the Manchester encoder/decoder to the RXD pin. When LBK is Low, no AUI loopback occurs.

Collision Detection Function

The collision detection function operates on the twisted pair side of the interface. For standard (half-duplex) 10BASE-T operation, a collision is defined as the simultaneous presence of valid signals on both the TPI circuit and the TPO circuit. The LXT908 reports collisions to the back-end via the COL pin. If the TPI circuit becomes active while there is activity on the TPO circuit, the TPI data is passed to the back-end over the RXD circuit, disabling normal loopback. Figure 5 is a state diagram of the LXT908 collision detection function. Refer to Test Specifications for collision detection and COL/CI output timing (NOTE: For full-duplex operation, the collision detection circuitry must be disabled.)

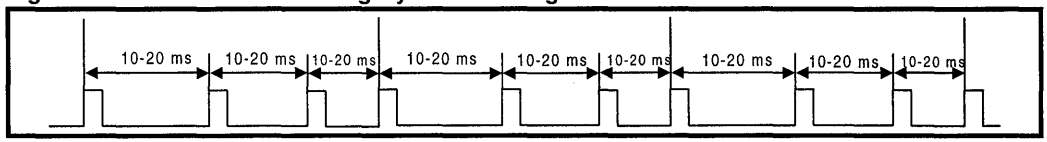
Figure 5: Collision Detection Function



Link Pulse Transmission

The LXT908 transmits standard link pulses which meet the 10BASE-T specifications. Figure 6 shows the link integrity pulse timing.

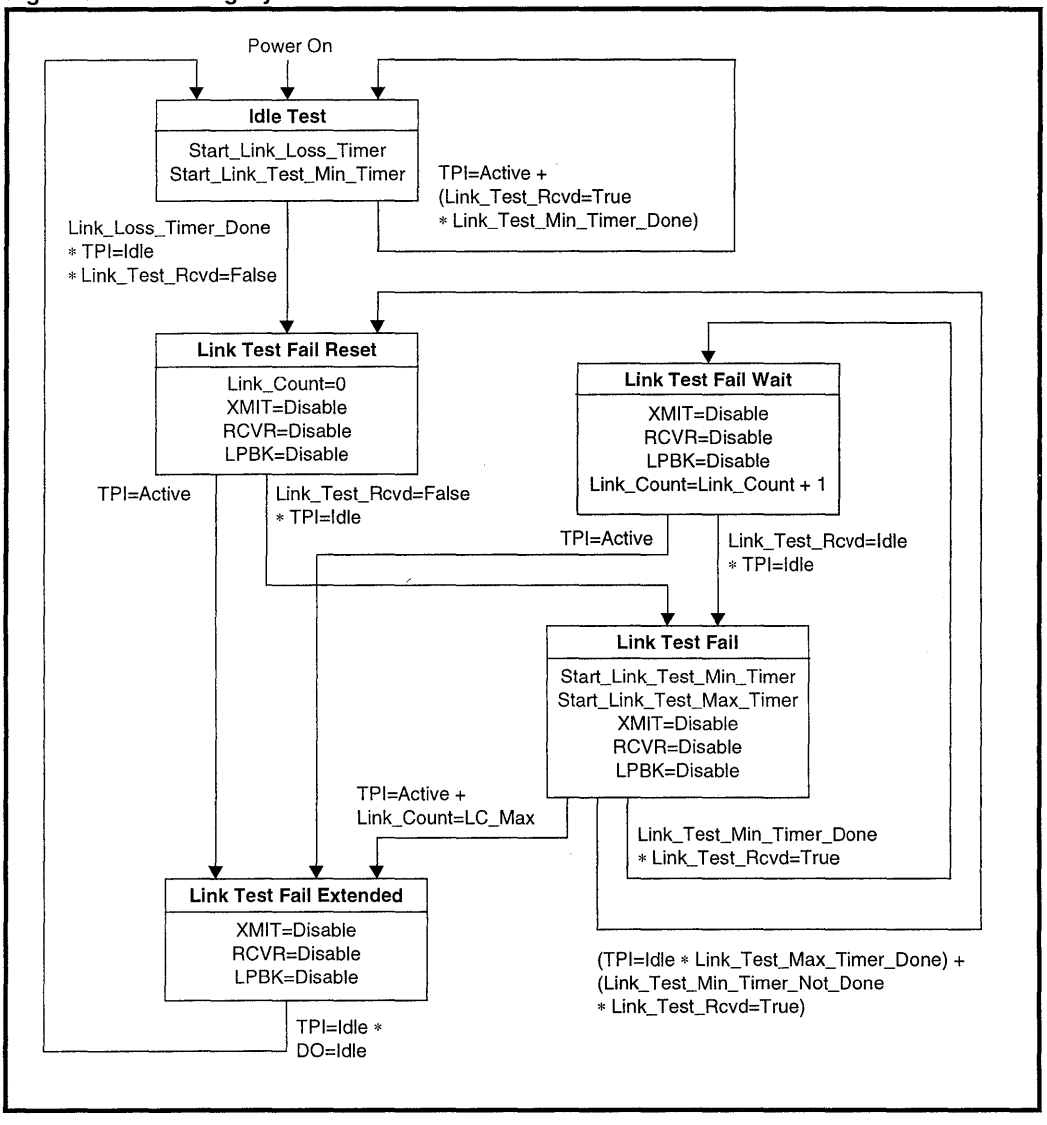
Figure 6: Transmitted Link Integrity Pulse Timing



Link Integrity Test Function

Figure 7 is a state diagram of the LXT908 Link Integrity test function. The link integrity test is used to determine the status of the receive side twisted-pair cable. Link integrity testing is enabled when pin 8 (LI) is tied High. When enabled, the receiver recognizes link integrity pulses which are transmitted in the absence of receive traffic. If no serial data stream or link integrity pulses are detected within 50 - 150ms, the chip enters a link fail state and disables the transmit and normal loopback functions. The LXT908 ignores any link integrity pulse with interval less than 2 - 7ms. The LXT908 will remain in the link fail state until it detects either a serial data packet or two or more link integrity pulses.

Figure 7: Link Integrity Test Function



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APPLICATION INFORMATION

Figures 8 through 14 show some typical LXT908 applications.

External Components

Crystal Information

Suitable crystals are available from various manufacturers. Table 3 lists some suitable crystals based on limited evaluation. Designers should test and validate all crystals before using them in production.

Table 3: Suitable Crystals

Manufacturer	Part Number
MTRON	MP-1
	MP-2

Magnetic Information

The LXT908 requires a 1:1 ratio for the receive transformer and a 1:2 ratio for the transmit transformer. Table 4 lists transformers suitable for the applications described in this data sheet. Designers should test and validate all magnetics before committing to a specific component.

Table 4: Suitable Magnetics

Manufacturer	Part Number	
	Twisted-Pair	AUI
Belfuse	S553-5999-52	S553-1006-AE
	S553-5999-86	-
Fil-Mag	23Z118	23Z90
	23Z118SM	23Z90SM
Halo	TD74-1406Q	TD01-0756K
	TG74-1406N1	TG01-0756N
Valor	PT4152	LT6032
	ST4152	ST7032

Layout Requirements

Auto Port Select with External Loopback Control

Figure 8 is a typical LXT908 application. The diagram is arranged to group similar pins together; it does not represent the actual LXT908 pin-out. The controller interface pins (transmit data, clock and enable; receive data and clock; and the collision detect, carrier detect and loopback control pins) are shown at the top left.

Programmable option pins are grouped center left. The PAUI pin is tied Low and all other option pins are tied High. This set-up selects the following options:

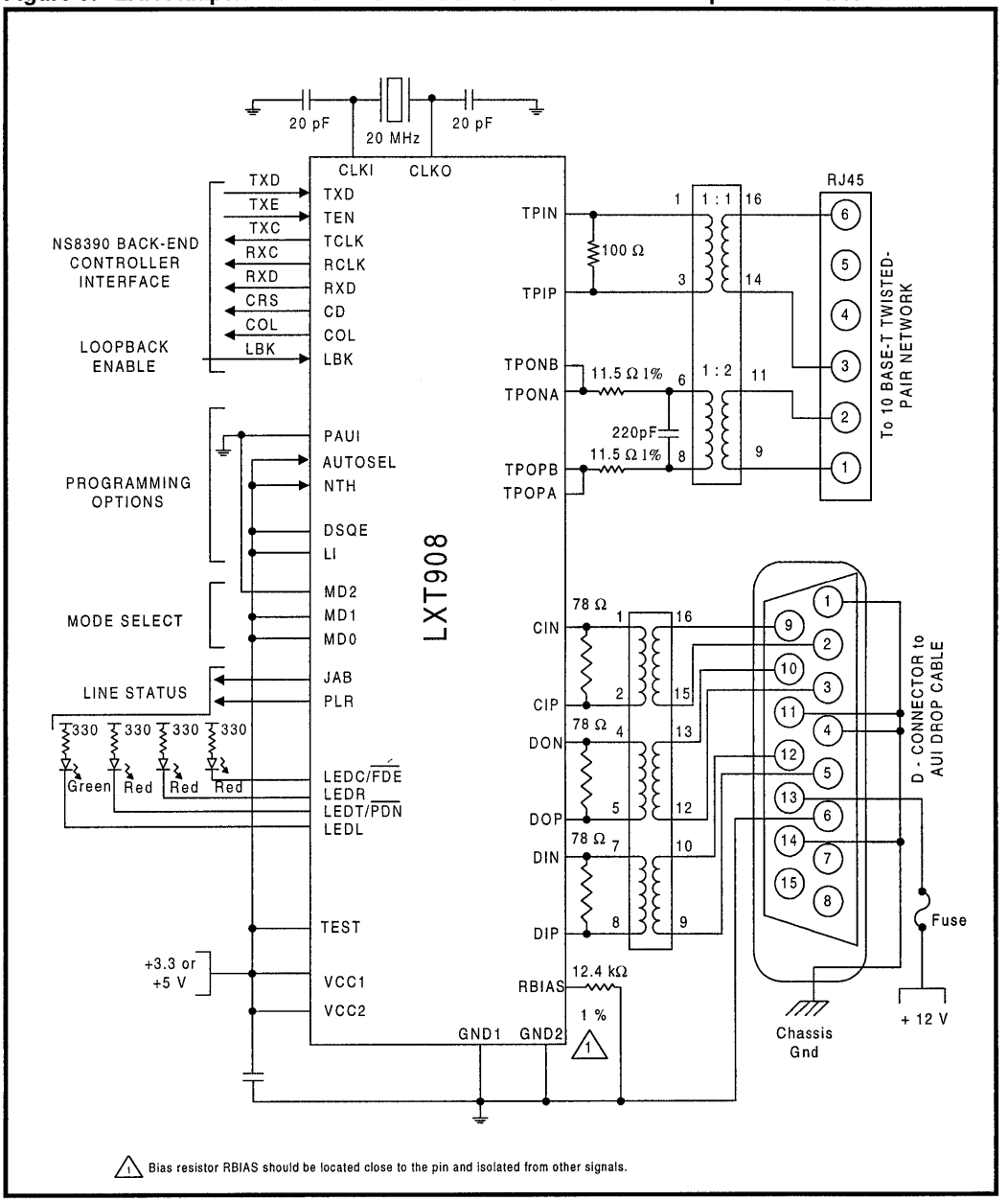
- Automatic Port Selection (PAUI Low and AUTOSEL High)
- Normal Receive Threshold (NTH High)
- Mode 4, compatible with National NS8390 controllers (MD2:0 = Low, High, High)
- SQE Disabled (DSQE High)
- Link Testing Enabled (LI High)

Status outputs are grouped at lower left. Line status outputs drive LED indicators and the Jabber and Polarity status indicators are available as required.

Power and ground pins are shown at the bottom of the diagram. A single power supply is used for both VCC1 and VCC2 with a decoupling capacitor installed between the power and ground busses.

The TP and AUI interfaces are shown at upper and lower right, respectively. Impedance matching resistors for 100 UTP are installed in each I/O pair but no external filters are required.

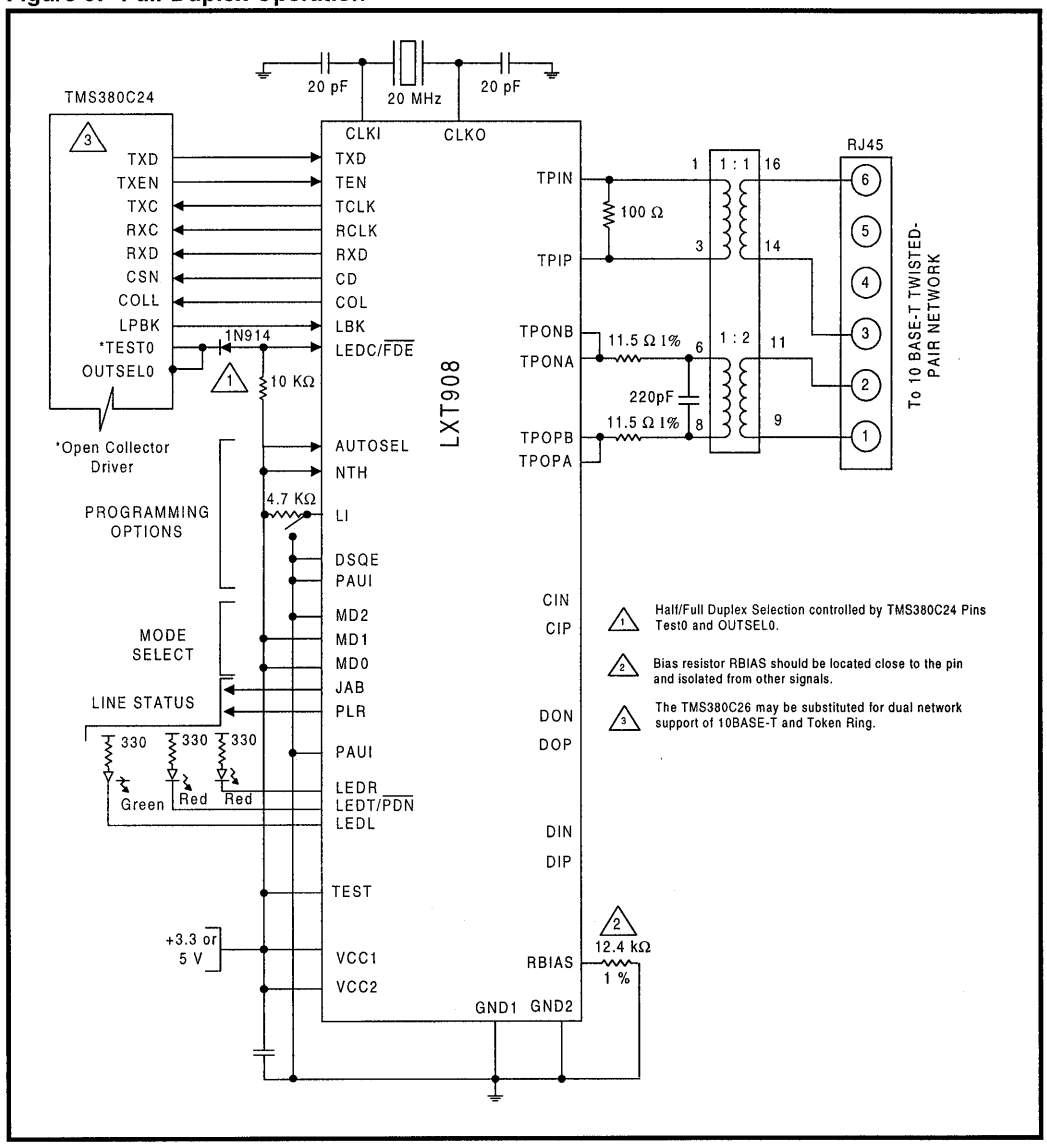
Figure 8: LAN Adapter Board - Auto Port Select with External Loopback Control



Full Duplex Support

Figure 9 shows the LXT908 with a Texas Instruments 380C24 CommProcessor. The 380C24 is compatible with Mode 4 (MD2:0 = Low, High, High). When used with the 380C24 or other full duplex-capable controller, the LXT908 supports full-duplex Ethernet, effectively doubling the available bandwidth of the network. In this application the SQE function is enabled (DSQE tied Low), and the LXT908 AUI port is not used.

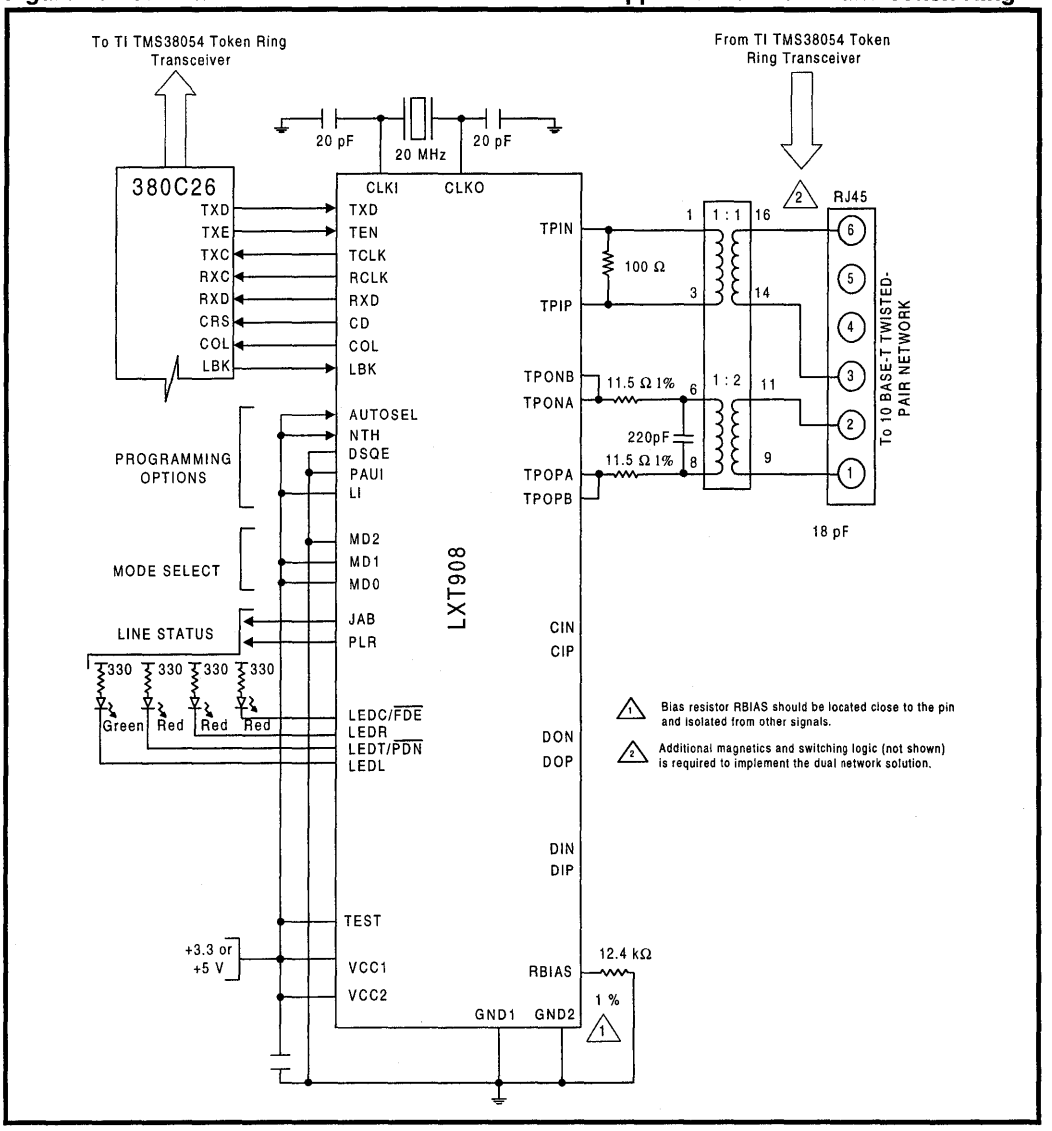
Figure 9: Full-Duplex Operation



Dual Network Support-10Base T and Token Ring

Figure 10 shows the LXT908 with a Texas Instruments 380C26 CommProcessor. The 380C26 is compatible with Mode 4 (MD2:0 = Low, High, High). When used with the 380C26, both the LXT908 and a TMS38054 Token Ring transceiver can be tied to a single RJ45 allowing dual network support from a single connector. The LXT908 AUI port is not used.

Figure 10: LXT908/380C26 Interface for Dual Network Support of 10BASE-T and Token Ring



Manual Port Select & Link Test Function

With MD2:0 = Low, High, Low, the LXT908 logic and framing are set to Mode 3 (compatible with Fujitsu MB86950 and MB86960, and Seeq 8005 controllers). Figure 11 shows the setup for Fujitsu controllers. Figure 12 shows the four inverters required to interface with the Seeq 8005 controller. As in Figure 8, both these Mode 3 applications show the LI pin tied High, enabling Link Testing; and the NTH and DSQE pins are both tied High, selecting the standard receiver threshold and disabling SQE. However, in these applications AUTOSEL is tied Low, allowing external port selection through the PAUI pin.

Figure 11: LAN Adapter Board - Manual Port Select with Link Test Function

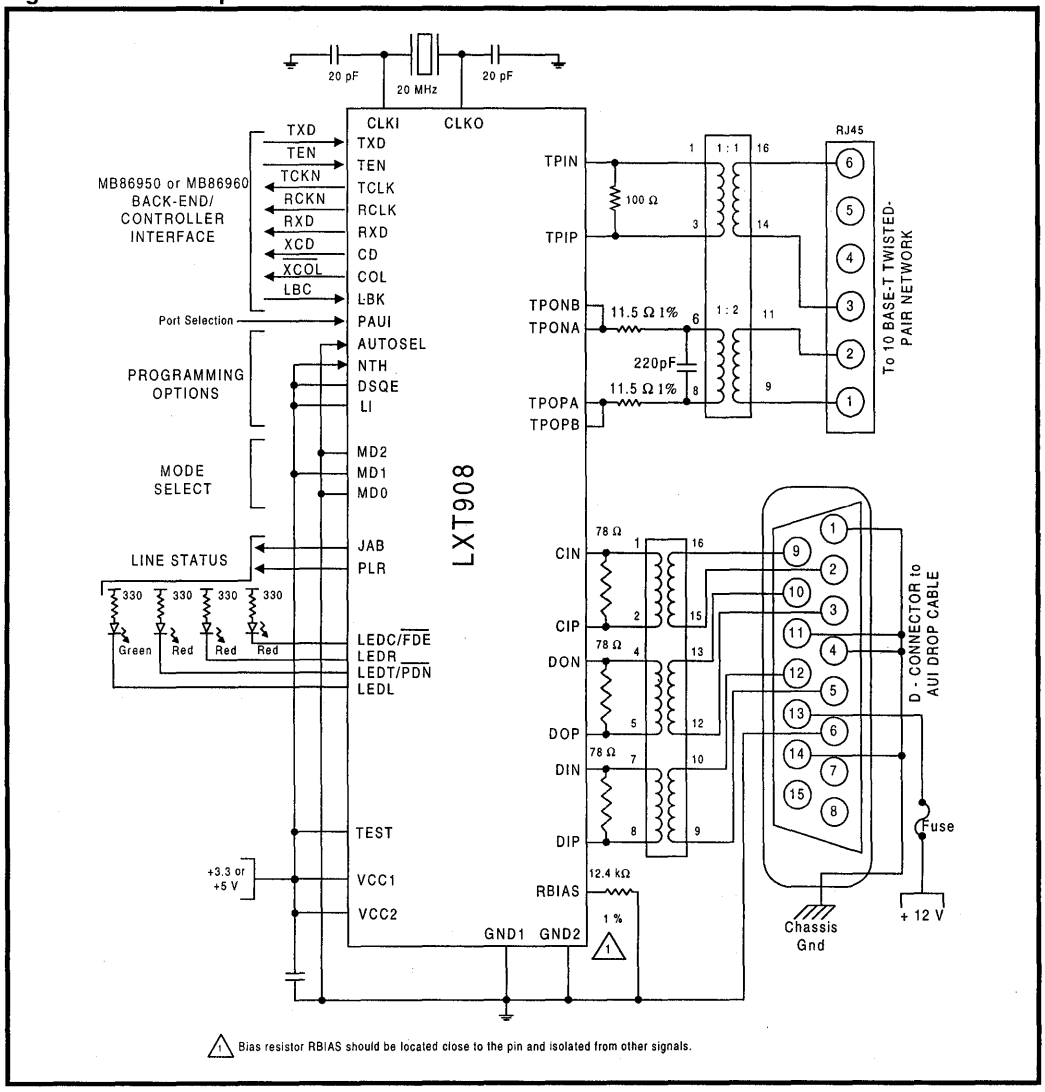
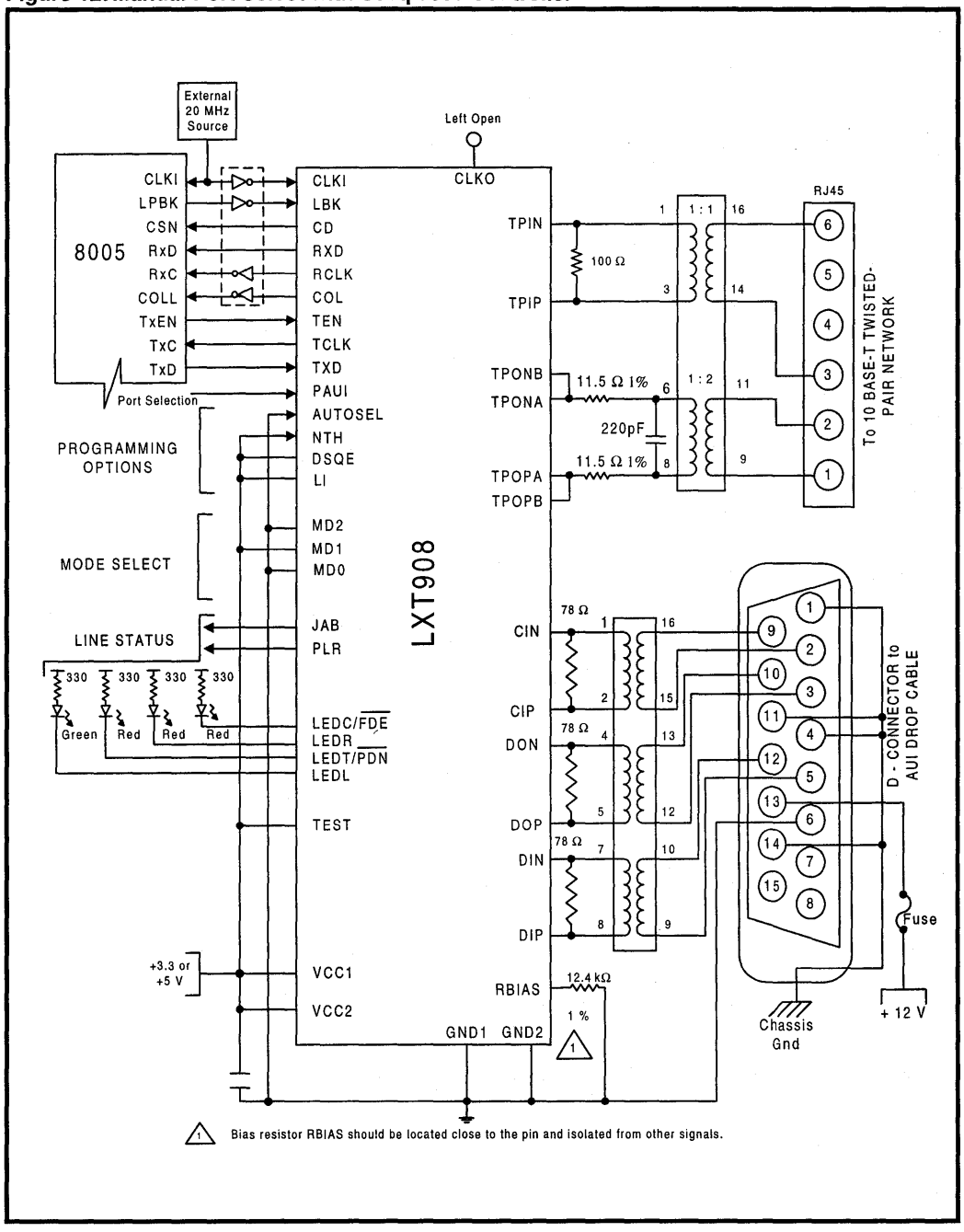


Figure 12: Manual Port Select with Seeq 8005 Controller

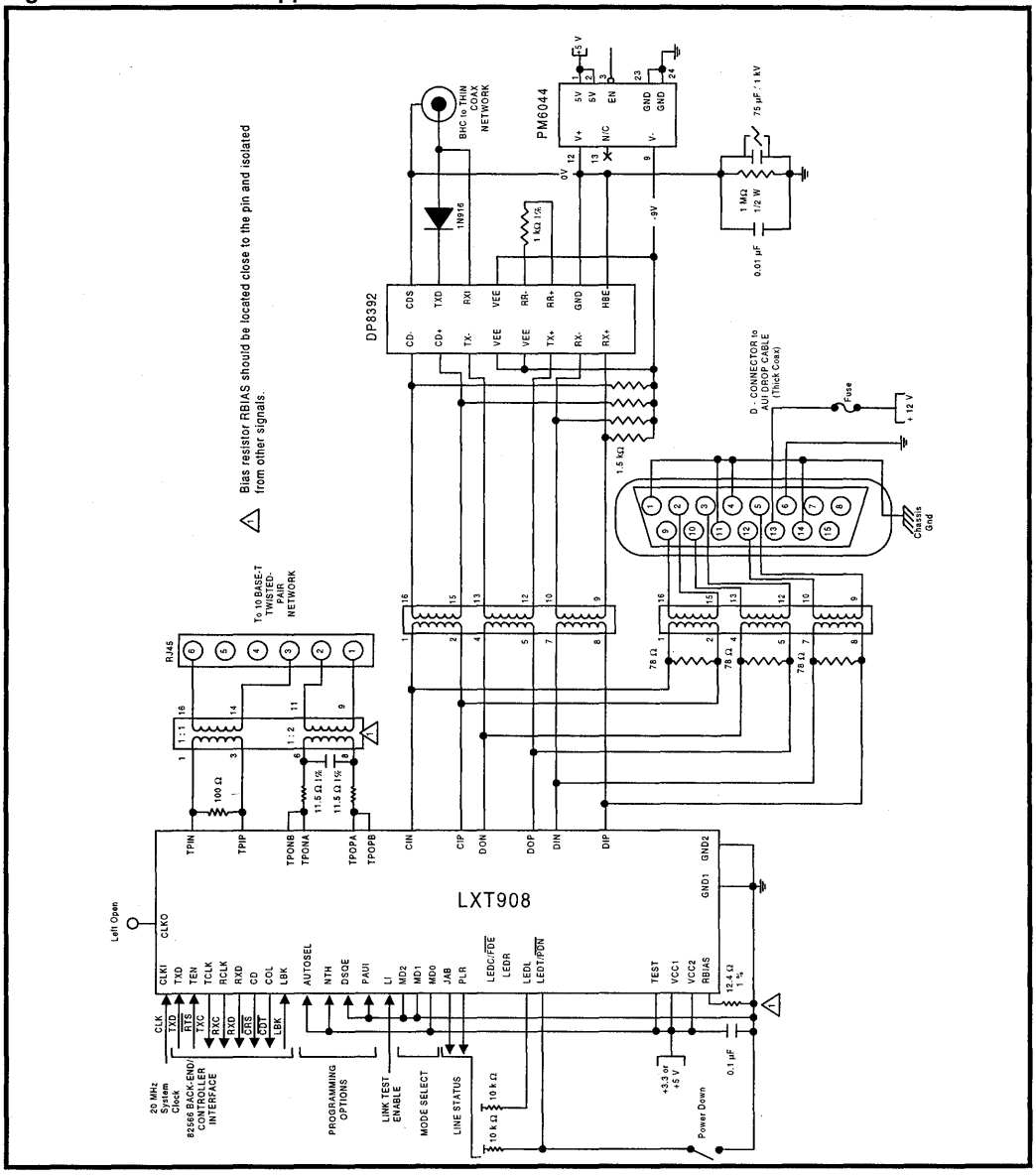


11

Three Media Application

Figure 13 shows the LXT908 in Mode 2 (compatible with Intel 82596 controllers) with additional media options for the AUI port. Two transformers are used to couple the AUI port to either a D-connector or a BNC connector. (A DP8392 coax transceiver with PM6044 power supply are required to drive the thin coax network through the BNC.)

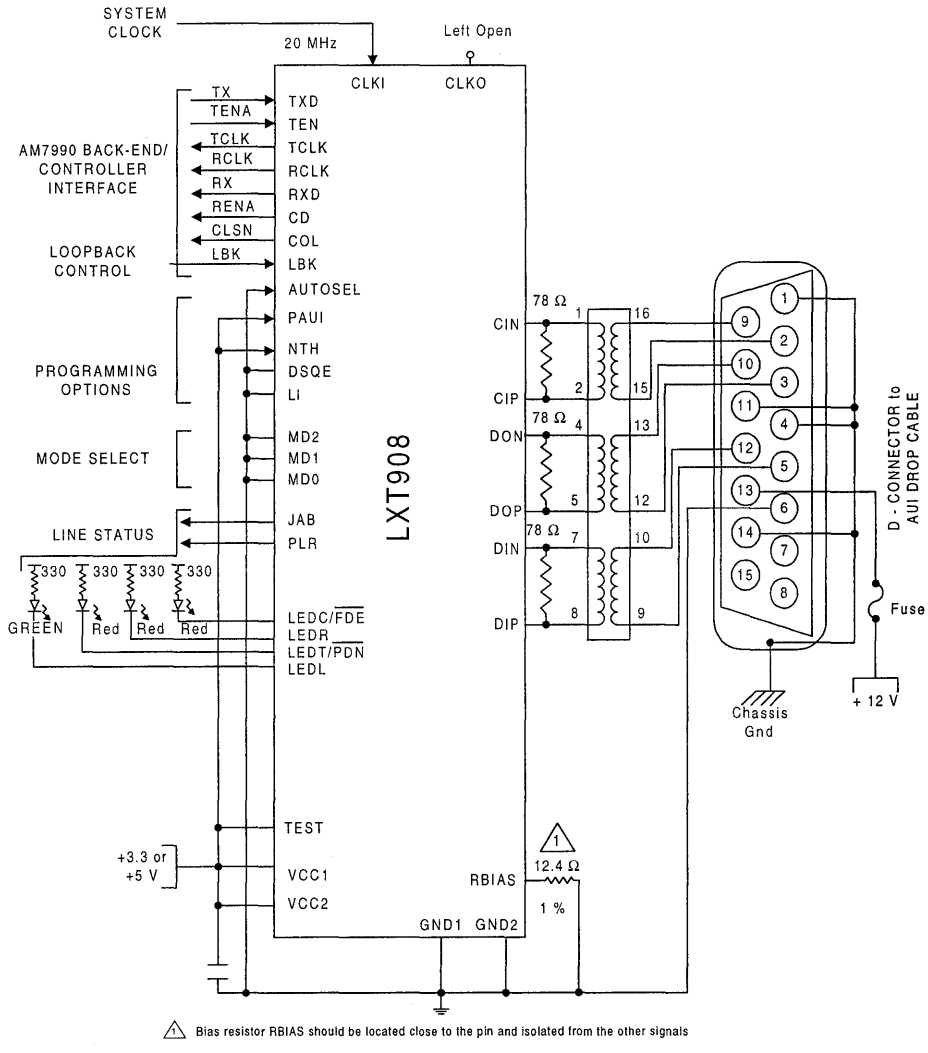
Figure 13: Three Media Application



AUI Encoder/Decoder Only

In the application shown in Figure 14, the DTE is connected to a coaxial network through the AUI. AUTOSEL is tied Low and PAUI is tied High, manually selecting the AUI port. The twisted-pair port is not used. With MD2:0 all tied Low, the LXT908 logic and framing are set to Mode 1 (compatible with AMD and Motorola controllers). The LI pin is tied Low, disabling the link test function. The DSQE pin is also Low, enabling the SQE function. The LBK input controls loopback. A 20 MHz system clock is supplied at CLKI with CLKO left open.

Figure 14: AUI Encoder/Decoder Only Application



TEST SPECIFICATIONS

NOTE

The minimum and maximum values in Tables 5 through 14 and Figures 15 through 44 represent the performance specifications of the LXT908 and are guaranteed by test, except where noted by design.

Table 5: Absolute Maximum Values

Parameter	Symbol	Min	Max	Units
Supply voltage	VCC	-0.3	6	V
Ambient operating temperature	TA	0	70	°C
Storage temperature	TSTG	-65	+150	°C

CAUTION

Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 6: Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Recommended supply voltage[1]	VCC	3.135	5.0	5.25	V	
Recommended operating temperature	TOP	0	–	70	°C	

1. Voltages with respect to ground unless otherwise specified.

Table 7: I/O Electrical Characteristics (Over Recommended Range)

Parameter		Sym	Min	Typ[1]	Max	Units	Test Conditions
Input Low voltage[2]		VIL	–	–	0.8	V	
Input High voltage[2]		VIH	2.0	–	–	V	
Output Low voltage		VOL	–	–	0.4	V	IOL = 1.6 mA
		VOL	–	–	10	%VCC	IOL < 10 µA
Output Low voltage (Open drain LED driver)		VOLL	–	–	0.7	V	IOLL = 10 mA
Output High voltage		VOH	2.4	–	–	V	IOH = 40 µA
		VOH	90	–	–	%VCC	IOH < 10 µA
Output rise time	CMOS	–	–	3	12	ns	CLOAD = 20 pF
TCLK & RCLK	TTL	–	–	2	8	ns	
Output fall time	CMOS	–	–	3	12	ns	CLOAD= 20 pF
TCLK & RCLK	TTL	–	–	2	8	ns	

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Limited functional tests are performed at these input levels. The majority of functional tests are performed at levels of 0V and 3V.

Table 7: I/O Electrical Characteristics (Over Recommended Range) – continued

Parameter		Sym	Min	Typ[1]	Max	Units	Test Conditions
CLKI rise time (externally driven)		–	–	–	10	ns	
CLKI duty cycle (externally driven)		–	–		40/60	%	
Supply current	Normal Mode	ICC	–	65	85	mA	Idle Mode
		ICC	–	95	120	mA	Transmitting on TP
		ICC	–	90	120	mA	Transmitting on AUI
	Power Down Mode	ICC	–	0.75	2	mA	

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Limited functional tests are performed at these input levels. The majority of functional tests are performed at levels of 0V and 3V.

Table 8: AUI Electrical Characteristics (Over Recommended Range)

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Input Low current	IIL	–	–	-700	µA	
Input High current	IIH	–	–	500	µA	
Differential output voltage	VOD	±550	–	±1200	mV	
Differential squelch threshold	VDS	150	260	350	mV	5 MHz square wave input

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 9: Twisted-Pair Electrical Characteristics (Over Recommended Range)

Parameter		Symbol	Min	Typ[1]	Max	Units	Test Conditions
Transmit output impedance		ZOUT	–	5	–	Ω	
Transmit timing jitter addition[2]		–	–	±6.4	±10	ns	0 line length for internal MAU
Transmit timing jitter added by the MAU and PLS sections[2, 3]		–	–	±3.5	±5.5	ns	After line model specified by IEEE 802.3 for 10BASE-T internal MAU
Receive input impedance		ZIN	–	20	–	kΩ	Between TPIP/TPIN, CIP/CIN & DIP/DIN
Differential Squelch Threshold	Normal Threshold NTH = High	VDS	300	395	585	mV	5 MHz square wave input
	Reduced Threshold NTH = Low	VDS	180	250	345	mV	5 MHz square wave input

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Parameter is guaranteed by design; not subject to production testing.
3. IEEE 802.3 specifies maximum jitter additions at 1.5 ns for the AUI cable, 0.5 ns from the encoder, and 3.5 ns from the MAU.

Table 10: Switching Characteristics (Over Recommended Range)

Parameter		Symbol	Minimum	Typical[1]	Maximum	Units
Jabber Timing	Maximum transmit time	–	20	–	150	ms
	Unjab time	–	250	–	750	ms
Link Integrity Timing	Time link loss receive	–	50	–	150	ms
	Link min receive	–	2	–	7	ms
	Link max receive	–	50	–	150	ms
	Link transmit period	–	8	10/20	24	ms

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 11: RCLK/Start-of-Frame Timing (Over Recommended Range)

Parameter		Symbol	Minimum	Typical[1]	Maximum	Units
Decoder acquisition time	AUI	tDATA	–	900	1100	ns
	TP	tDATA	–	1200	1500	ns
CD turn-on delay	AUI	tCD	–	25	200	ns
	TP	tCD	–	420	550	ns
Receive data setup from RCLK	Mode 1	tRDS	60	70	–	ns
	Modes 2 through 5	tRDS	30	45	–	ns
Receive data hold from RCLK	Mode 1	tRDH	10	20	–	ns
	Modes 2 through 5	tRDH	30	45	–	ns
RCLK shut off delay from CD assert (Mode 3 and Mode 5)		tSWS	–	±100	–	ns

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.

Table 12: RCLK/End-of-Frame Timing (Over Recommended Range)

Parameter	Type	Sym	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Units
RCLK after CD off	Min	tRC	5	1	–	5	–	BT
RXD throughput delay	Max	tRD	400	375	375	375	375	ns
CD turn off delay[2]	Max	tCDOFF	500	475	475	475	475	ns
Receive block out after TEN off	Typ[1]	tIFG	5	50	–	–	–	BT
RCLK switching delay after CD off (Mode 3 and 5)	Typ[1]	tSWE	–	–	120(±80)	–	120(±80)	ns

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.
2. CD turn-off delay measured from middle of last bit; timing specification is unaffected by the value of the last bit.

Table 13: Transmit Timing (Over Recommended Range)

Parameter	Symbol	Minimum	Typical [1]	Maximum	Units
TEN setup from TCLK	tEHCH	22	–	–	ns
TXD setup from TCLK	tDSCH	22	–	–	ns
TEN hold after TCLK	tCHEL	5	–	–	ns
TXD hold after TCLK	tCHDU	5	–	–	ns
Transmit start-up delay - AUI	tSTUD	–	220	450	ns
Transmit start-up delay - TP	tSTUD	–	430	450	ns
Transmit through-put delay - AUI	tTPD	–	–	300	ns
Transmit through-put delay - TP	tTPD	–	305	350	ns

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.

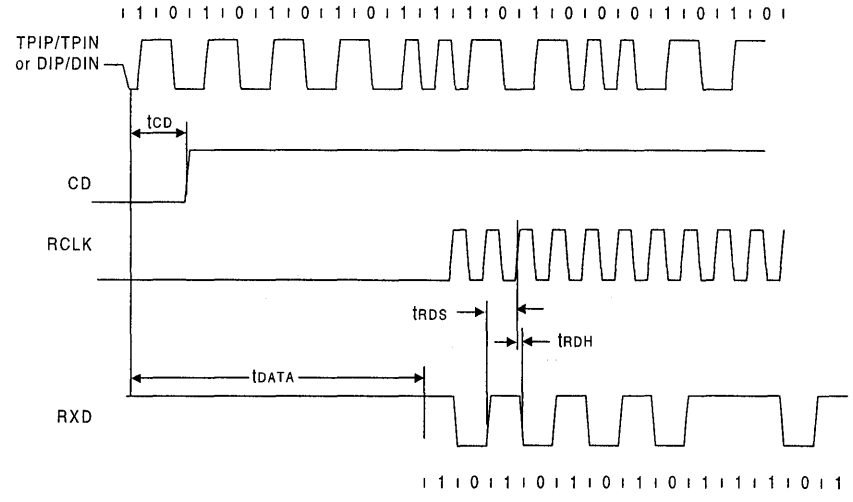
Table 14: Collision, COL/CI Output and Loopback Timing (Over Recommended Range)

Parameter	Symbol	Minimum	Typical[1]	Maximum	Units
COL turn-on delay	tCOLD	–	40	500	ns
COL turn-off delay	tCOLOFF	–	420	500	ns
COL (SQE) Delay after TEN off	tSQED	0.65	1.2	1.6	µs
COL (SQE) Pulse Duration	tSQEP	500	1000	1500	ns
LBK setup from TEN	tKHEH	10	25	–	ns
LBK hold after TEN	tKHEL	10	0	–	ns

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.

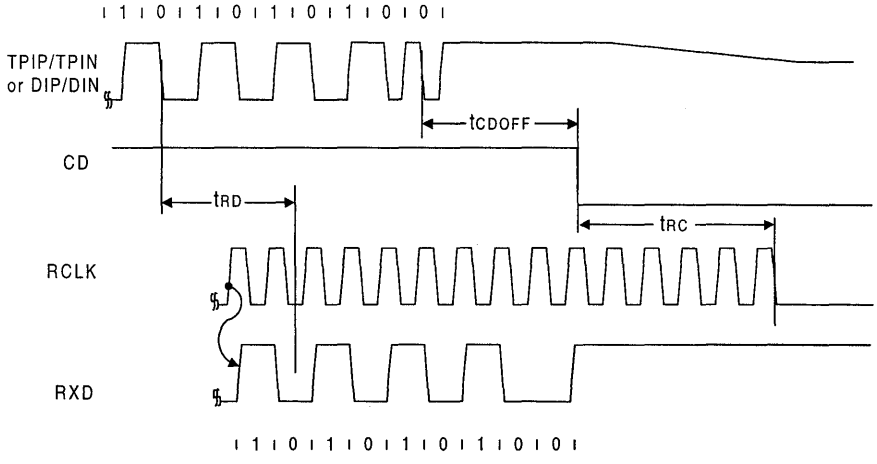
Timing Diagrams for Mode 1 *(MD2, 1, 0 = Low, Low, Low) Figures 15 through 20*

Figure 15: Mode 1 RCLK/Start-of-Frame Timing



NOTE: 1. RXD changes 25 ns after the rising edge of RCLK.

Figure 16: Mode 1 RCLK/End-of-Frame Timing



NOTE: 1. RXD changes 25 ns after the rising edge of RCLK.

Figure 17: Mode 1 Transmit Timing

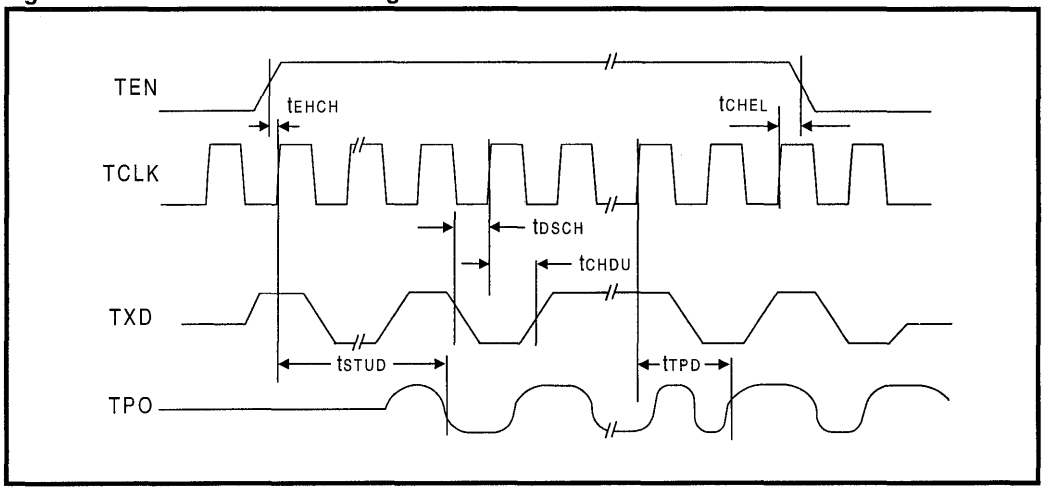


Figure 18: Mode 1 Collision Detect Timing

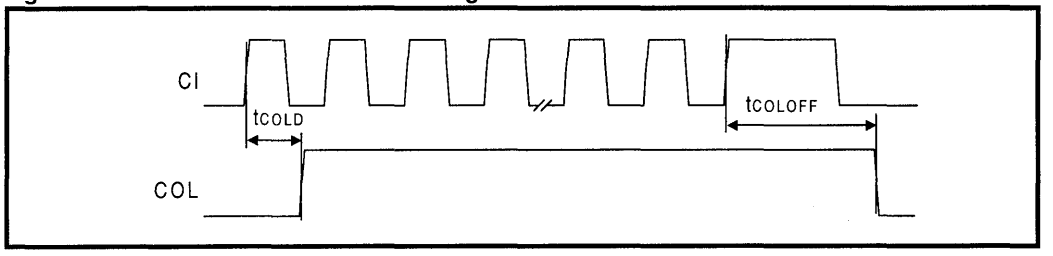


Figure 19: Mode 1 COL/SQE Output Timing/CI Output Timing

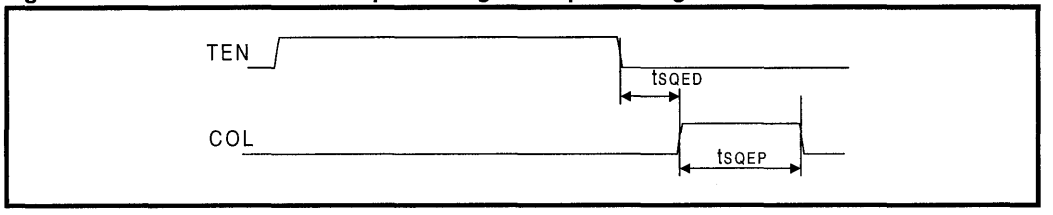
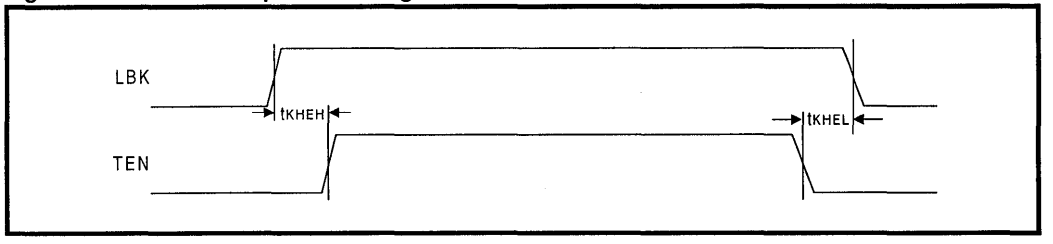
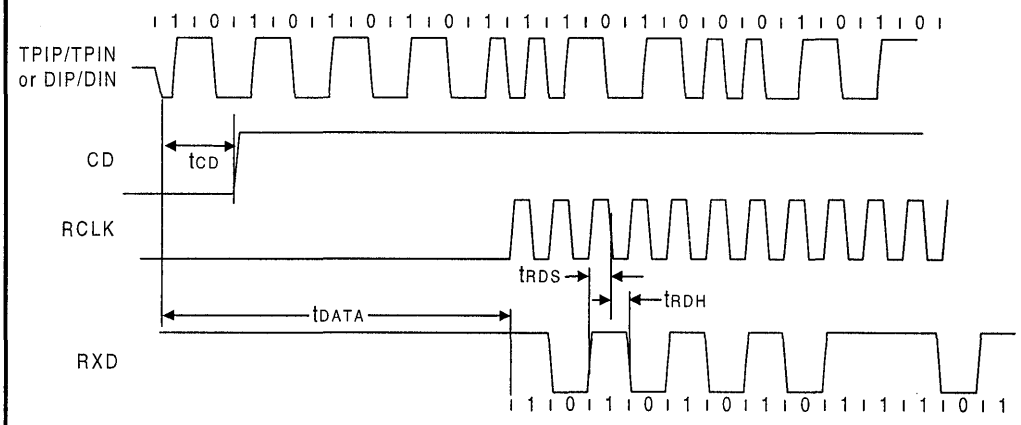


Figure 20: Mode 1 Loopback Timing



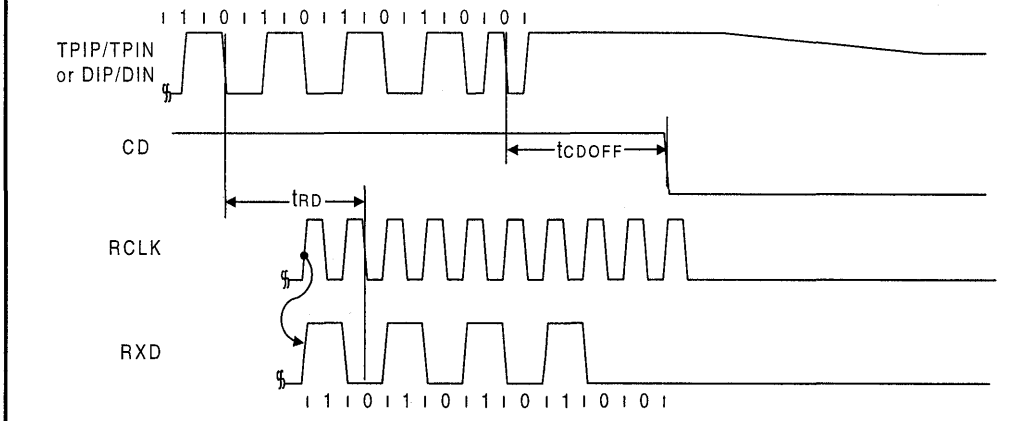
Timing Diagrams for Mode 2 *(MD2, 1, 0 = Low, Low, High) Figures 21 through 26*

Figure 21: Mode 2 RCLK/Start-of-Frame Timing



NOTE: 1. RXD changes at the rising edge of RCLK. The controller is sampled at the falling edge.

Figure 22: Mode 2 RCLK/End-of-Frame Timing



NOTE: 1. RXD changes at the rising edge of RCLK. The controller is sampled at the falling edge.

Figure 23: Mode 2 Transmit Timing

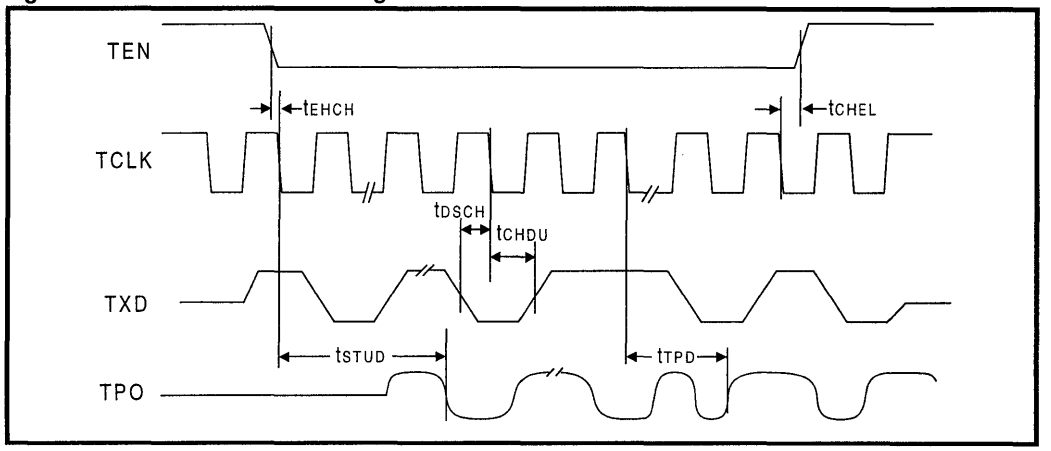


Figure 24: Mode 2 Collision Detect Timing

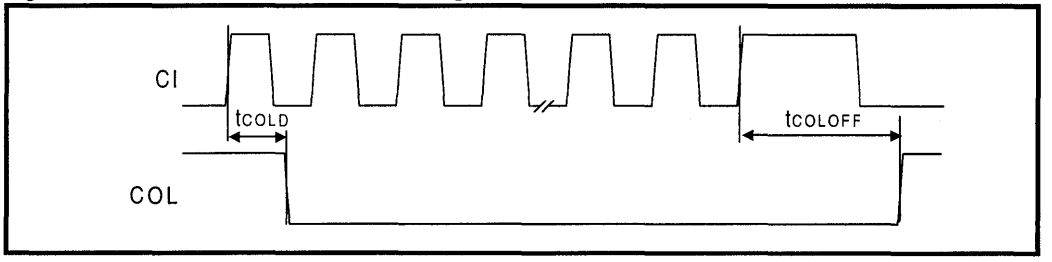
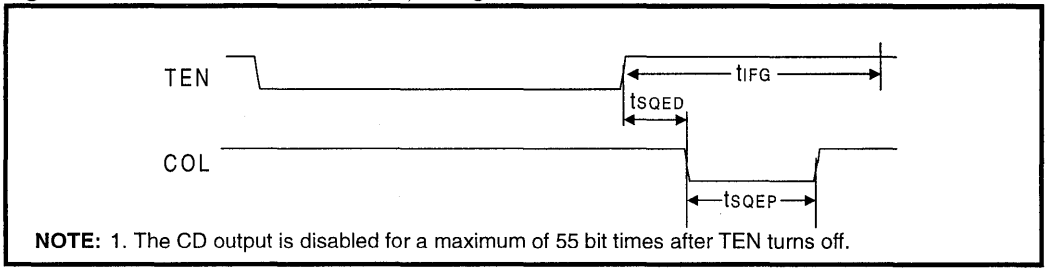
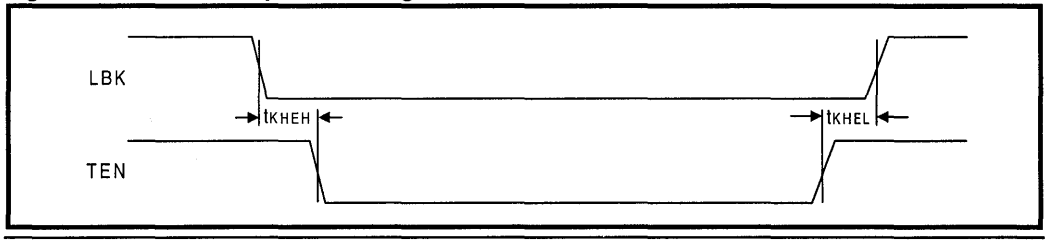


Figure 25: Mode 2 COL/SQE Output Timing



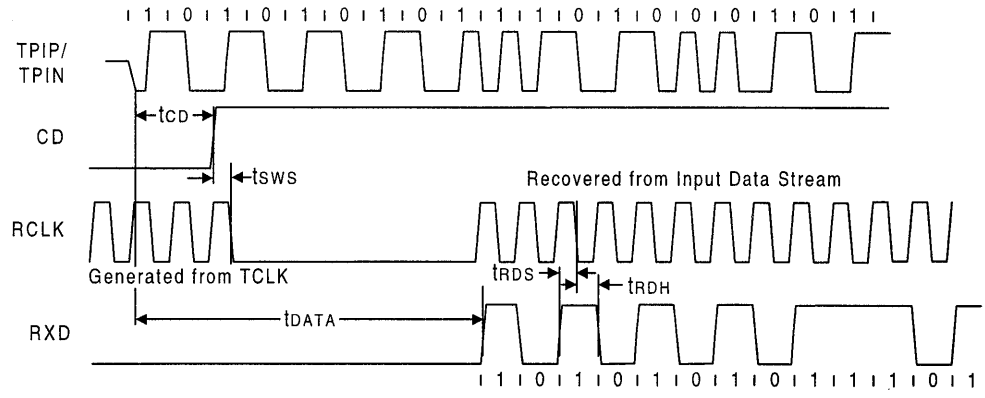
NOTE: 1. The CD output is disabled for a maximum of 55 bit times after TEN turns off.

Figure 26: Mode 2 Loopback Timing



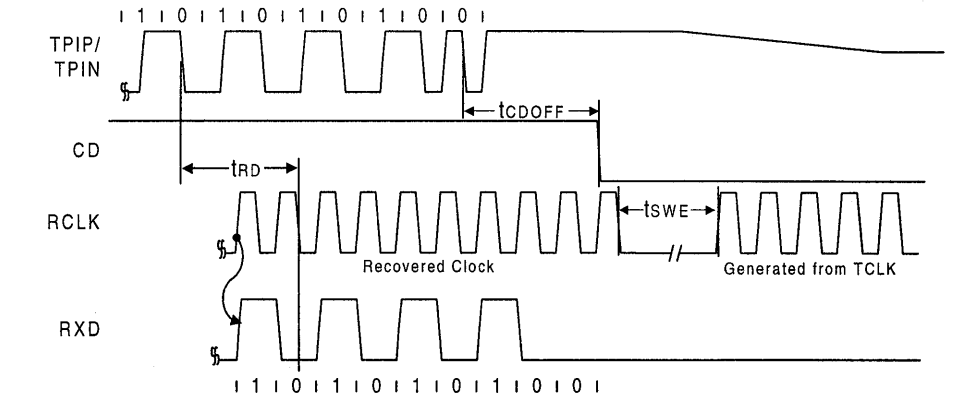
Timing Diagrams for Mode 3 *(MD2, 1, 0 = Low, High, Low) Figures 27 through 32*

Figure 27: Mode 3 RCLK/Start-of-Frame Timing



NOTE: 1. RXD changes at the rising edge of RCLK. The controller is sampled at the falling edge.

Figure 28: Mode 3 RCLK/End-of-Frame Timing



NOTE: 1. RXD changes at the rising edge of RCLK. The controller is sampled at the falling edge.

Figure 29: Mode 3 Transmit Timing

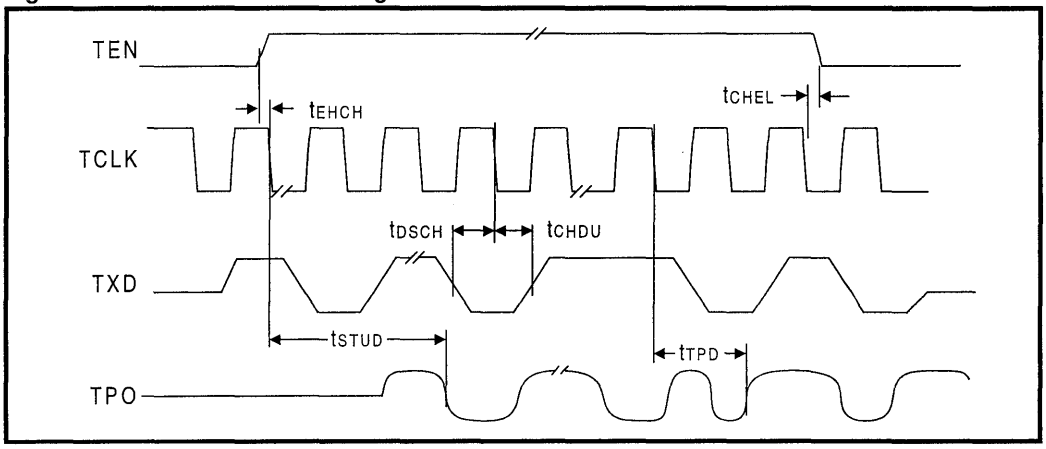


Figure 30: Mode 3 Collision Detect Timing

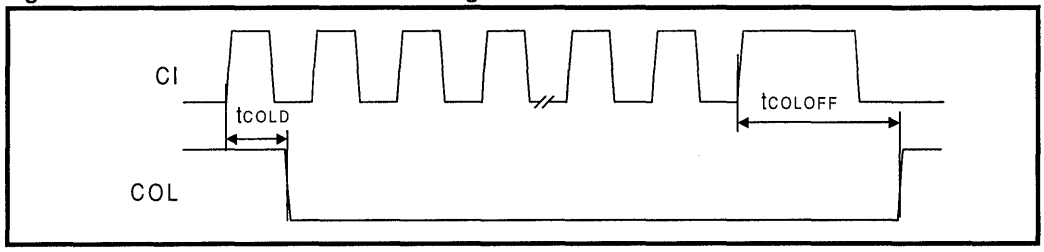
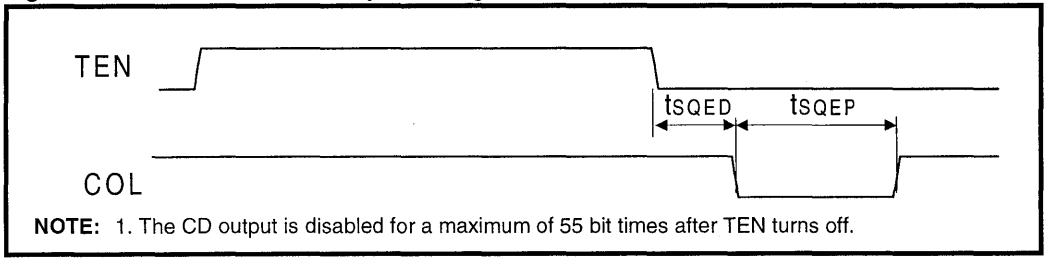
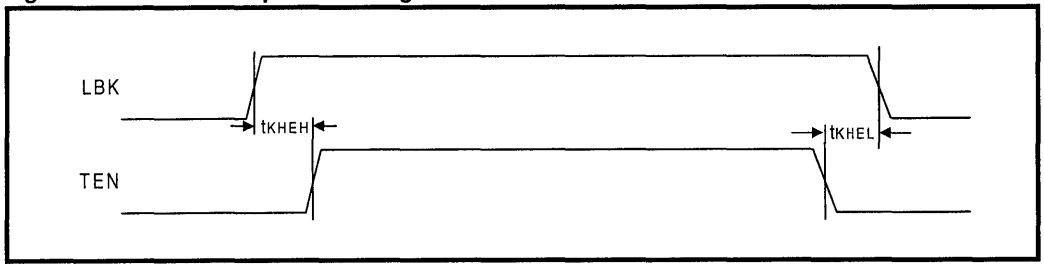


Figure 31: Mode 3 COL/SQE Output Timing



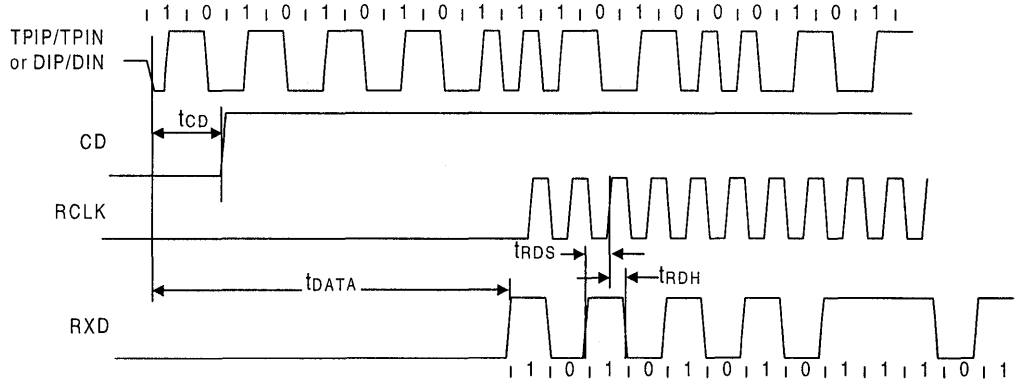
NOTE: 1. The CD output is disabled for a maximum of 55 bit times after TEN turns off.

Figure 32: Mode 3 Loopback Timing



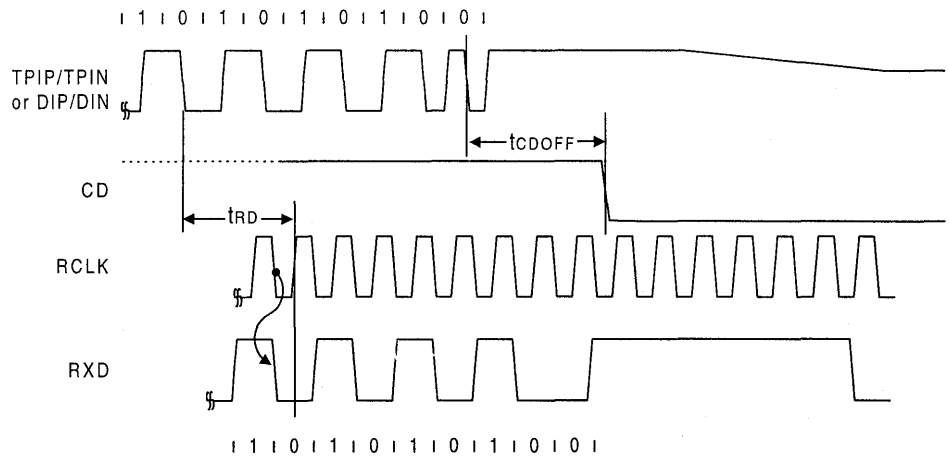
Timing Diagrams for Mode 4 *(MD2, 1, 0 = Low, High, High) Figures 33 through 38*

Figure 33: Mode 4 RCLK/Start-of-Frame Timing



NOTE: 1. RXD changes at the falling edge of RCLK. The controller is sampled at the rising edge.

Figure 34: Mode 4 RCLK/End-of-Frame Timing



NOTE: 1. RXD changes at the falling edge of RCLK. The controller is sampled at the rising edge.

Figure 35: Mode 4 Transmit Timing

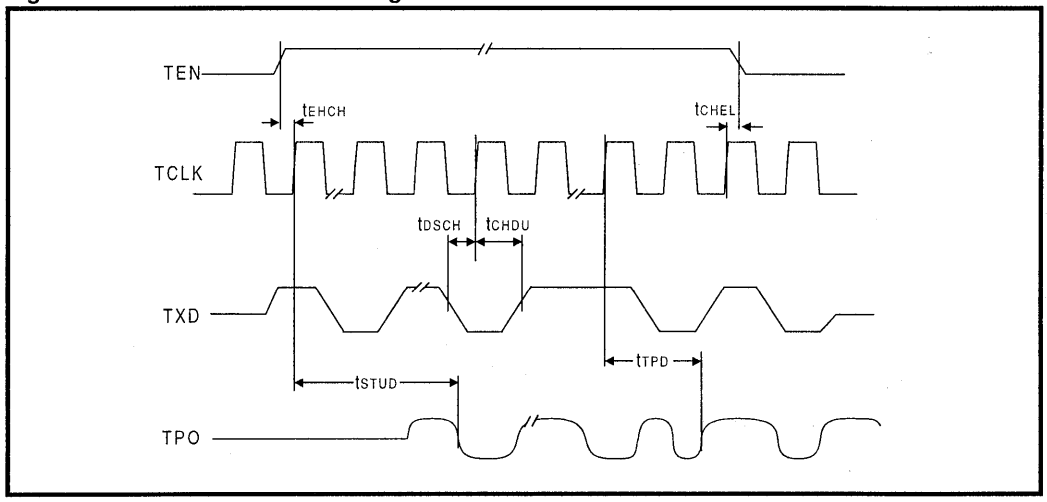


Figure 36: Mode 4 Collision Detect Timing

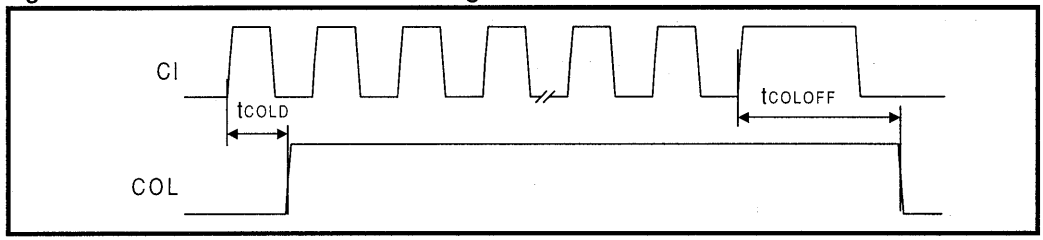


Figure 37: Mode 4 COL/SQE Output Timing

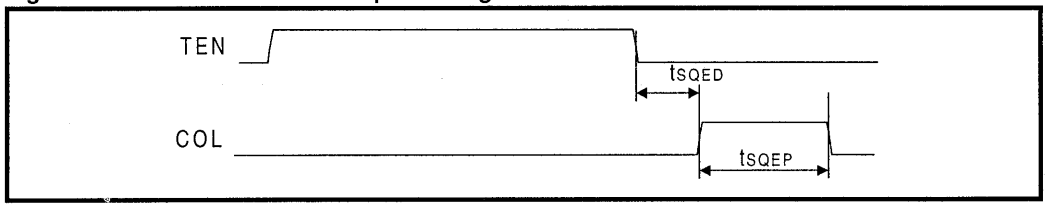
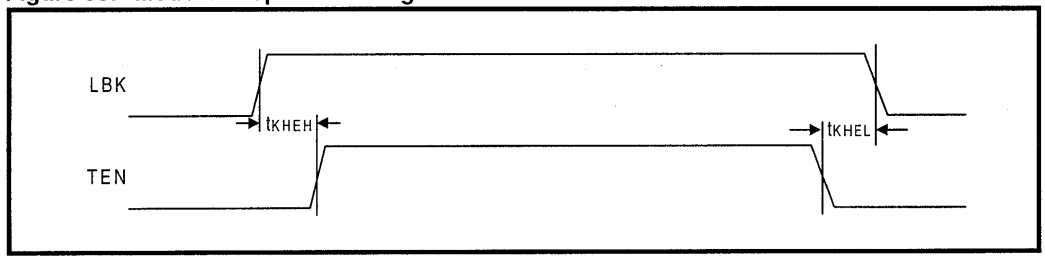
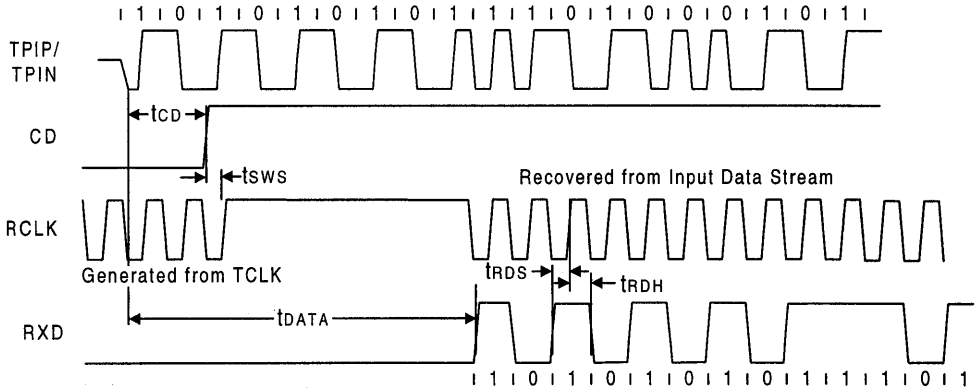


Figure 38: Mode 4 Loopback Timing



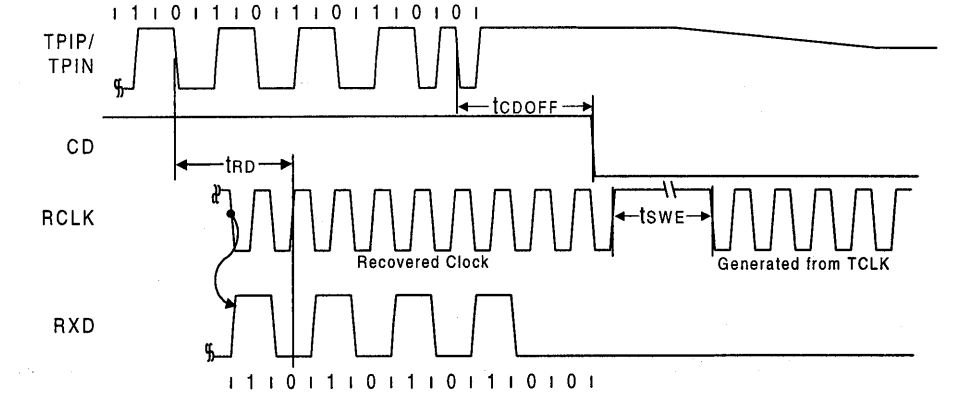
Timing Diagrams for Mode 5 *(MD2, 1, 0 = High, High, Low) Figures 39 through 44*

Figure 39: Mode 5 RCLK/Start-of-Frame Timing



NOTE: 1. RXD changes at the falling edge of RCLK. The controller is sampled at the rising edge.

Figure 40: Mode 5 RCLK/End-of-Frame Timing



NOTE: 1. RXD changes at the falling edge of RCLK. The controller is sampled at the rising edge.

Figure 41: Mode 5 Transmit Timing

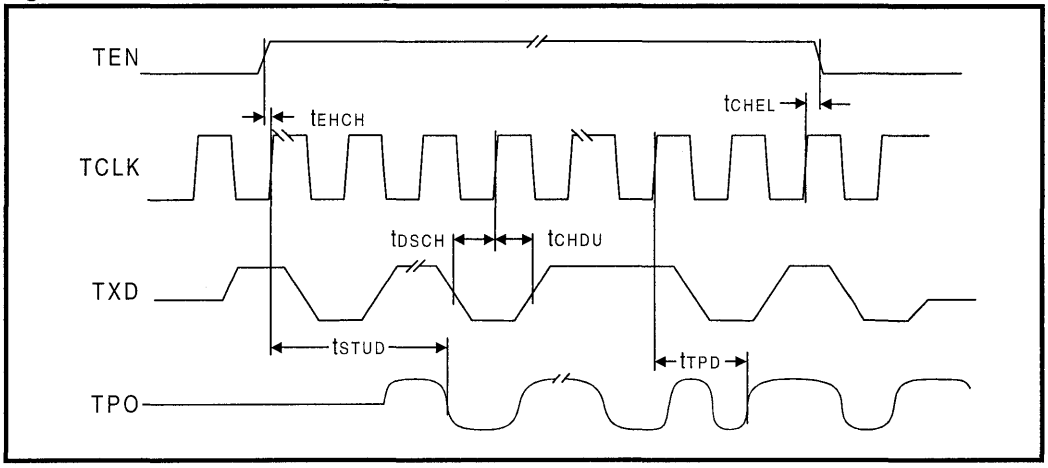


Figure 42: Mode 5 Collision Detect Timing

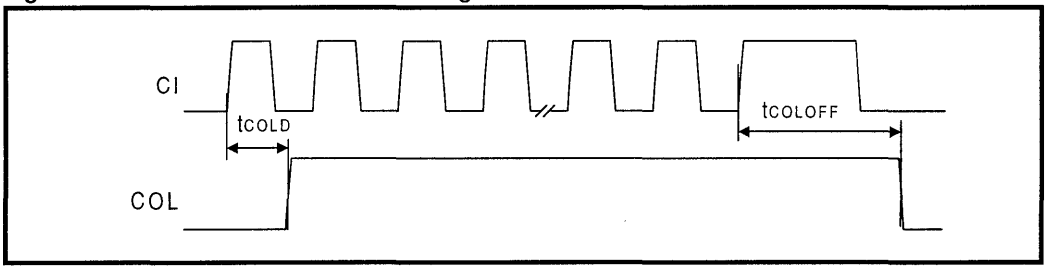


Figure 43: Mode 5 COL/SQE Output Timing

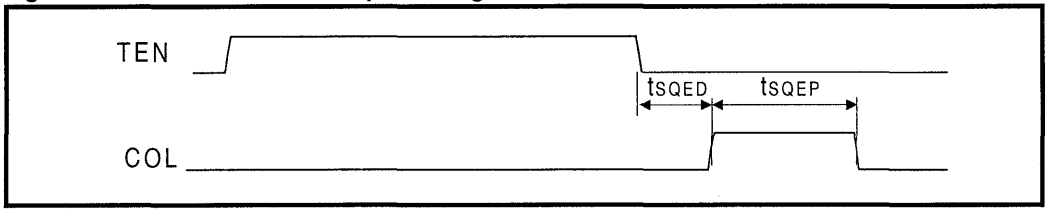
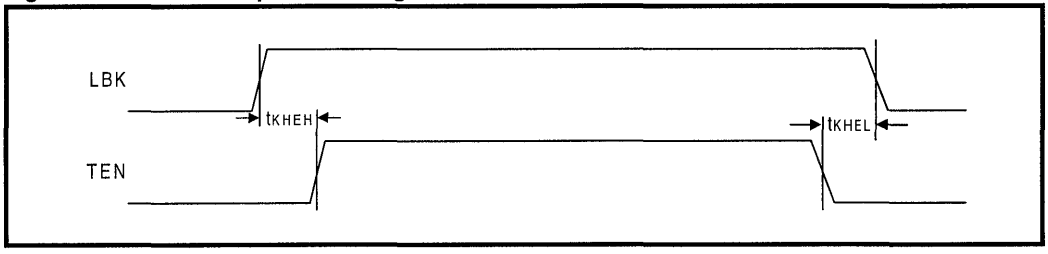


Figure 44: Mode 5 Loopback Timing



NOTES

DATA SHEET

LXT944

JUNE 1997
Revision 2.1

Quad Ethernet Interface Adapter

General Description

The LXT944 is the first quad 10BASE-T transceiver device with integrated filters. The LXT944 Quad Ethernet Adapter is designed for IEEE 802.3 physical layer applications. This single CMOS device includes all of the active circuitry for interfacing most standard 802.3 controllers to 10BASE-T media.

The LXT944 includes four Manchester encoders/decoders, receiver squelch and transmit pulse shaping, jabber, link integrity testing and reversed polarity detection and correction per port. The LXT944 drives four independent 10BASE-T twisted-pair cables with only isolation transformers. Integrated filters simplify the design work required for FCC compliant EMI performance.

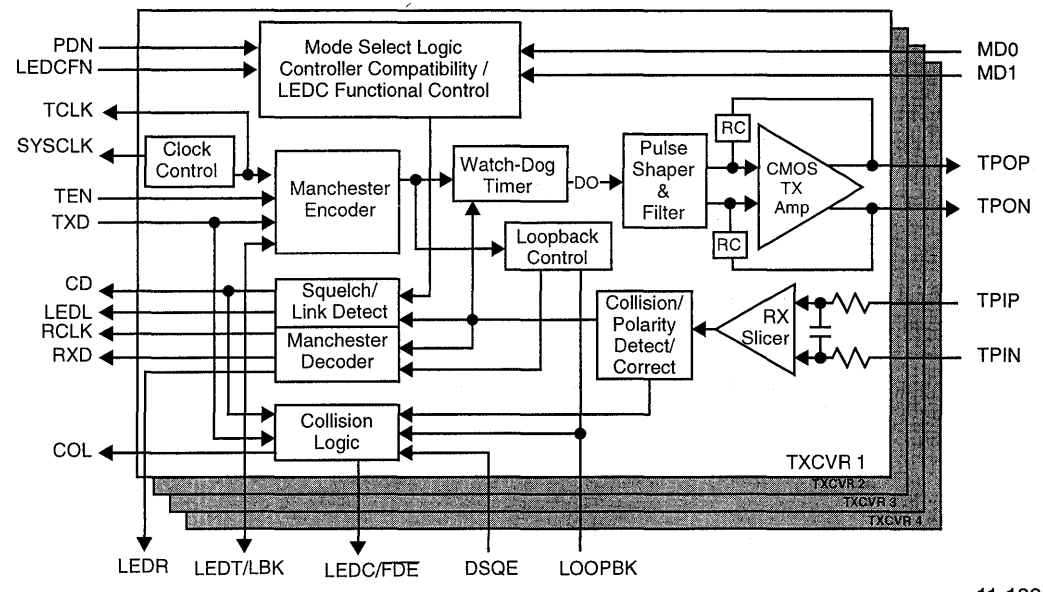
Applications

- Hub/switched Dedicated LANs for 10BASE-T
- Multi-port 10BASE-T Server products

Features

- Quad Independent 10BASE-T compliant transceivers with Integrated filters
- Quad Integrated Manchester encoder/decoder
- Power-down mode with tri-stated outputs
- Automatic Polarity Detection & Correction
- Global SQE enable/disable
- Four LED drivers per port
- Full duplex capability per port
- External Loopback with port disable
- Available in 100-pin Plastic Quad Flat Pack

LXT944 Block Diagram



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PIN ASSIGNMENTS AND SIGNAL DESCRIPTIONS

Figure 1: LXT944 Pin Assignments

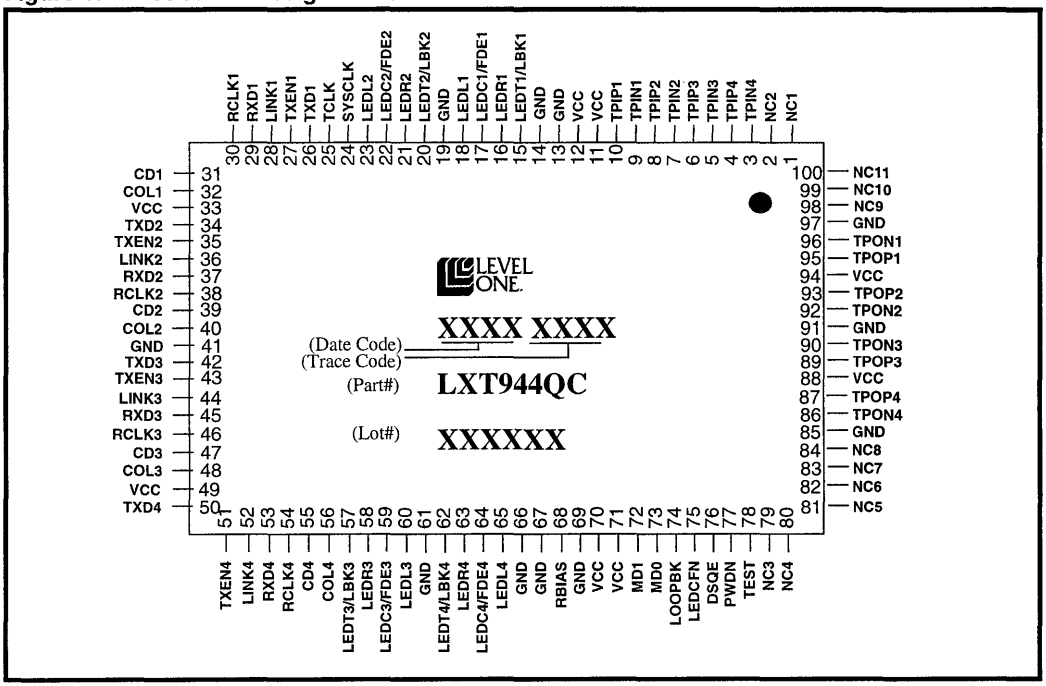

Table 1: Twisted-Pair Interface Signal Descriptions

Pin	Symbol	I/O	Description
10	TPIP1	I	**Twisted Pair Data Inputs, Positive & Negative (ports 1–4).** These pins are the positive (TPIP) and negative (TPIN), twisted-pair data input pins for ports 1 - 4, respectively.
9	TPIN1	I	
8	TPIP2	I	
7	TPIN2	I	
6	TPIP3	I	
5	TPIN3	I	
4	TPIP4	I	
3	TPIN4	I	
95	TPOP1	O	**Twisted Pair Data Outputs, Positive & Negative (ports 1–4).** These pins are the positive (TPOP) and negative (TPON), twisted-pair data output pins for ports 1 - 4, respectively. The outputs are pre-equalized; no external filters are required.
96	TPON1	O	
93	TPOP2	O	
92	TPON2	O	
89	TPOP3	O	
90	TPON3	O	
87	TPOP4	O	
86	TPON4	O	

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Table 2: MAC Interface Signal Descriptions

Pin	Symbol	I/O	Description
27 35 43 51	TXEN1 TXEN2 TXEN3 TXEN4	I I I I	**Transmit Enable (ports 1–4).** These pins enable data transmission from the respective controller and start the watch dog timers. The signals are synchronous to TCLK. Pulled Low internally.
26 34 42 50	TXD1 TXD2 TXD3 TXD4	I I I I	**Transmit Data (ports 1–4).** These pins are input signals containing NRZ data to be transmitted on the network. The TXD pins should be tied directly to the data output of the respective controller. Pulled Low internally.
25	TCLK *(global)*	O	**Transmit Clock.** 10 MHz clock output. This clock signal should be directly connected to the transmit clock input of each controller.
29 37 45 53	RXD1 RXD2 RXD3 RXD4	O O O O	**Receive Data (ports 1–4).** These are the output signals and should be connected directly to the data input of the respective controller.
30 38 46 54	RCLK1 RCLK2 RCLK3 RCLK4	O O O O	**Receive Clock (ports 1–4).** These pins provide recovered 10MHz clocks which are synchronous to the receive data from the respective port. These pins should be connected to the receive clock input of the respective controller.
31 39 47 55	CD1 CD2 CD3 CD4	O O O O	**Carrier Detect (ports 1–4).** Outputs for notifying the controller that activity exists on the respective network.
32 40 48 56	COL1 COL2 COL3 COL4	O O O O	**Collision Detect (ports 1–4).** Outputs for driving the respective collision detect inputs of the controller. COL1 - COL4 also carry signal quality error (SQE) signals.

Table 3: Control Signal Descriptions

Pin	Symbol	I/O	Description
73 72	MD0 MD1 *(global)*	I	**Mode Select 0 (MD0), Mode Select 1 (MD1).** These pins determine the controller compatibility mode as specified in Table 7. Default is mode 3.
74	LOOPBK *(global)*	I	**Global Loopback.** When Low, all ports are forced to internal loopback, disabling collision and the transmission of both data and link pulses. When High, the loopback function is controlled on a per port basis using LEDT1 - 4/LBK1 - 4.
76	DSQE *(global)*	I	**SQE Disable.** When this pin is pulled High, the SQE function is disabled. When this pin is driven Low or floated, the SQE function is enabled. This pin controls the SQE function for all four TP ports.
77	PWDN *(global)*	I	**Power Down.** When driven High the LXT944 enters power down state with all outputs tri–stated. When Low the LXT944 is in operational mode.

Table 4: Status Indication Signal Descriptions

Pin	Symbol	I/O	Description
28 36 44 52	LINK1 LINK2 LINK3 LINK4	O O O O	**Link Status (ports 1–4).** These four signals indicate link status for each port: Low = link test pass. High = link test fail. The link status is valid for both half and full duplex modes.
75	LEDCFN *(global)*	I	**LEDC Function Select.** When driven Low or floated, the LEDC1–4/FDE1–4 pins are bidirectional. When driven High the LEDC1–4/FDE1–4 pins are TTL inputs only.
17 22 59 64	LEDC1/FDE1 LEDC2/FDE2 LEDC3/FDE3 LEDC4/FDE4	I/O I/O I/O I/O	**Collision LED drivers (ports 1–4).** Open drain drivers for the collision indicators. The output is pulled Low and the pulse is extended for 100ms to indicate collision. **Full Duplex Enable (ports 1–4).** If Externally tied Low, the respective port is forced into Full Duplex Mode. These pins are internally pulled up.
15 20 57 62	LEDT1/LBK1 LEDT2/LBK2 LEDT3/LBK3 LEDT4/LBK4	I/O I/O I/O I/O	**Transmit LED drivers (ports 1–4).** Open drain drivers for the transmit indicators. The output is pulled Low and the pulse is extended for 100 ms to indicate transmit activity. **Loopback (ports 1–4).** If Externally tied Low, the respective port is forced to Internal Loopback, disabling collision detection and the transmission of both data and link pulses. See LOOPBK pin 74. These pins are internally pulled up.
16 21 58 63	LEDR1 LEDR2 LEDR3 LEDR4	O O O O	**Receive LED drivers (ports 1–4).** Open drain drivers for the receive indicators. The output is pulled Low and the pulse is extended for 100 ms to indicate receive activity.
18 23 60 65	LEDL1 LEDL2 LEDL3 LEDL4	O O O O	**Link LED drivers (ports 1–4).** These tri–level LED drivers indicate Link status for each port. The outputs are pulled Low to indicate half duplex link pass state. The outputs are driven High to indicate full duplex link pass state. When in link fail state the driver is tri–stated.

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Table 5: Miscellaneous Signal Descriptions

78	TEST	I	**Test.** Factory use only. This pin must be tied to **ground**.
24	SYSCLK	I	**System Clock.** A 20 MHz clock input is required at this pin.
1 2 79 80 81 82 83 84 98 99 100	NC1 NC2 NC3 NC4 NC5 NC6 NC7 NC8 NC9 NC10 NC11	– – – – – – – – – – –	**No Connects.** These pins must be left unconnected.

Table 6: Power and Ground Signal Descriptions

Pin	Symbol	I/O	Description
11 12 33 49 70 71 88 94	VCC	–	**Power Input.** These pins are to be connected to the power supply (**+5 volts**)
13 14 19 41 61 66 67 69 85 91 97	GND	–	**Ground.** These pins are to be connected to the **ground** plane.
68	RBIAS	I	**Bias.** Bias current for internal circuitry. This pin should be connected to ground through an external **7.5 kΩ 1%** resistor.

FUNCTIONAL DESCRIPTION

Introduction

The LXT944 Quad Ethernet Transceiver performs the physical layer signaling (PLS) and Media Attachment Unit (MAU) functions as defined by the IEEE 802.3 specification. It functions as an integrated PLS/MAU for use with four 10BASE-T twisted-pair networks.

The LXT944 interfaces between the Media Access Controller (four singles or one Quad MAC) and four twisted-pair (TP) cables. The MAC interface includes transmit and receive clock and NRZ data channels, as well as mode control logic and signaling. The twisted-pair interfaces include Twisted-Pair Input (TPI±) and Twisted-Pair Output (TPO±) pairs. In addition to the two basic interfaces, the LXT944 has a 20 MHz system clock input; a single 10 MHz TCLK output to all four controllers; LED drivers for Collision, Receive, Transmit, and Link Status of each port; independent or global internal loopback; full duplex operation on a per port basis; and four TTL link status outputs.

LXT944 functions are defined from the back end controller side of the interface. The LXT944 Transmit function refers to data transmitted by the back end controllers to the twisted-pair network. The LXT944 receive function refers to the data received by the back end controllers from the twisted-pair networks. The LXT944 performs all required MAU functions defined by the IEEE 802.3 10BASE-T specification such as collision detection, link integrity testing, signal quality error messaging, jabber control and loopback.

Controller Compatibility Modes

The LXT944 is compatible with most industry standard controllers including devices produced by Advanced Micro Devices (AMD), Fujitsu, Intel, Motorola, National Semiconductor, Seeq and Texas Instruments.

NOTE

Refer to Level One Application Note 51 when designing with Intel controllers. Note that Seeq controllers require inverters on the following signals: SYSCLK, LBK1-4, RCLK1-4 and COL1-4.

Four different control signal timing and polarity schemes (modes 1 through 4) are required to achieve this compatibility. The Mode select pins (MD1 & MD0) determine the controller compatibility mode as listed in Table 7. Controller compatibility mode is selected globally. Each of the four independent controller inputs (one per port) is configured to operate in the same mode. The user must select a single controller operating mode for all four ports. Refer to the Test Specification section for the timing parameters.

Transmit Function

The LXT944 receives NRZ data from the controller at the TXD input (as shown in the block diagram on the first page of the data sheet) and passes it through a Manchester encoder. The encoder data is then transferred to the twisted-pair network (the four TPO circuits). The advanced integrated pulse shaping and filtering network produces the output signal on TPON*x* and TPOP*x*, shown in Figure 2. The TPO output is pre-distorted and pre-filtered to meet the 10BASE-T jitter template. An internal, continuous, resistor-capacitor filter removes high frequency clocking noise from the pulse shaping circuitry. Integrated filters simplify the design work required for FCC compliant EMI performance. During idle periods the LXT944 transmits link integrity test pulses on the TPO*x* circuits (if the Loopback function is disabled).

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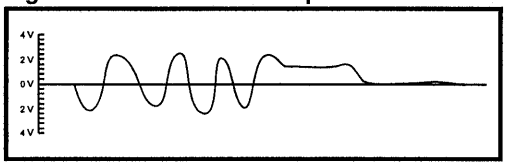
Table 7: Controller Compatibility Modes

Ethernet Controllers Supported	Mode	MD1	MD0
Advanced Micro Devices AM7990, Motorola 68EN360, MPC860 and compatible controllers	Mode 1	Low	Low
Intel 82596 and compatible controllers[1]	Mode 2	Low	High
Fujitsu MB86950, MB86960, Seeq 8005, and compatible controllers[2]	Mode 3	High	Low
National Semiconductor 8390, Texas Instruments TMS380C26, and compatible controllers	Mode 4	High	High

1. Refer to Level One Application Note 51 when designing with Intel controllers.
2. Seeq controllers require inverters on CLKI, LBK, RCLK and COL.

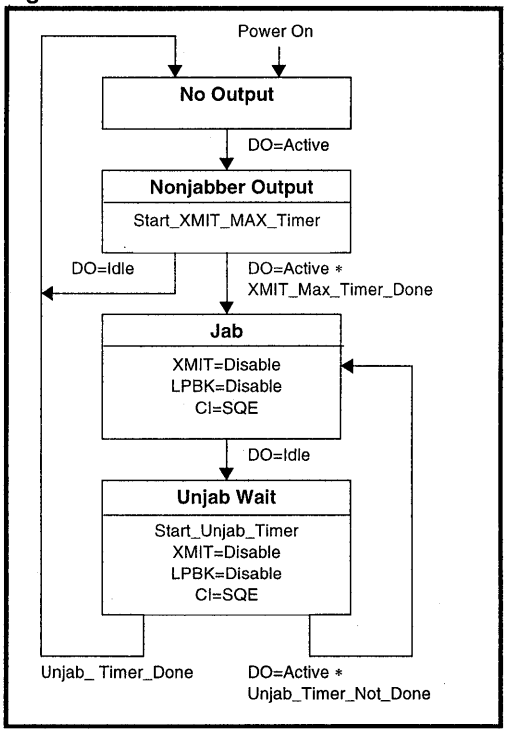
Figure 2: LXT944 TPO Output Waveform



Jabber Control Function

Figure 3 is a state diagram of the LXT944 jabber control function per port. The LXT944 on-chip watchdog timer prevents the DTE from locking into a continuous transmit mode. When a transmission exceeds the time limit, the watchdog timer disables the transmit and loopback functions and activates the COL*x* pins. Once the LXT944 is in jabber state, the TXD circuit must remain idle for a period of 0.25 to 0.75 seconds before it will exit the jabber state.

Figure 3: LXT944 Jabber Control Function

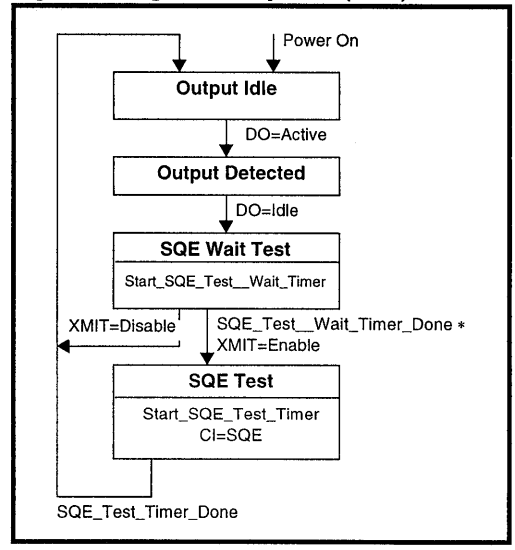


SQE Function

The LXT944 supports the Signal Quality Error (SQE) function as shown in Figure 4. After every successful transmission on the 10BASE-T network, the LXT944 transmits the SQE signal for 10 bit times (BT) ±5 BT on the COL*x* pins of the device.

The SQE function can be disabled for repeater or switch applications. When the DSQE pin = High, the SQE function is disabled. When DSQE = Low, the SQE function is enabled. The pin has an internal pull down enabling the SQE function when unconnected.

Figure 4: Signal Quality Error (SQE) Function



Receive Function

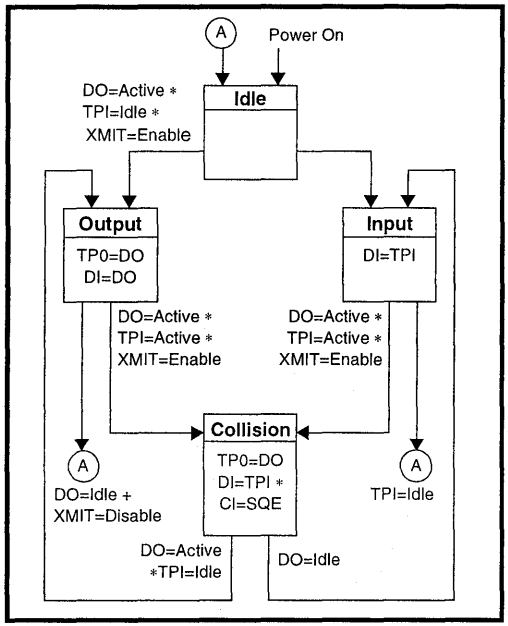
The LXT944 receive function acquires timing and data from the twisted-pair network (the TPI*x* circuits). Valid receive signals are passed through the on-chip filters and Manchester decoder then output as decoded NRZ data receive timing on the RXD RCLK pins, respectively.

An internal RC filter and an intelligent squelch function discriminates noise from link test pulses and valid data streams. The receive function is activated only by valid data streams above the squelch level and with proper timing. If the differential signals at the TPI*x* circuit inputs fall below 85% of the threshold level (unsquelched) for 8 bit times (typical), the LXT944 receive function enters the idle state. The LXT944 automatically corrects reversed polarity on the TPI*x* circuits.

Collision Detection Function

A collision is defined as the simultaneous presence of valid signals on both the TPI*x* circuits and the TPO*ix* circuits. The LXT944 reports collisions to the back-end via the COL*x* pins. If the TPI*x* circuits become active while there is activity on the TPO*x* circuits, the TPI*x* data is passed to the back-end over the RXD circuit, disabling normal loopback. Figure 5 is a state diagram of the LXT944 collision detection function per port.

Figure 5: LXT944 Collision Detection State Machine



Polarity Reverse Function

The LXT944 supports auto polarity detection and correction. The polarity reverse function uses both the link pulses and the end-of-frame data to determine polarity of the received signal. A reversed polarity condition is detected when eight consecutive opposite receive link pulses are detected without receipt of a link pulse of the expected polarity. Reversed polarity is also detected if four consecutive frames are received with a reversed start-of-idle. Whenever a corrected polarity frame is received, these two counters are reset to zero. If the LXT944 enters the link fail state and no valid data or link pulses are received within 96 to 128 ms, the polarity is reset to the default non-flipped condition. (If Link Integrity testing is disabled, polarity detection is based only on receive data.) Polarity correction is always enabled.

Loopback Function

The LXT944 provides the normal loopback function specified by the 10BASE-T standard for the twisted-pair port, as well as a forced loopback function. The loopback function operates in conjunction with the transmit function. Data transmitted by the back-end is internally looped back within the LXT944 from the TXD*x* pins through the Manchester encoder/decoder to the RXD1-4 pins and returned to the back-end. This "normal" loopback function is disabled when a data collision occurs, clearing the RXD*x* circuits for the TPI*x* data. Normal loopback is also disabled during link fail, jabber, and full duplex states. Loopback is always enabled during the forced loopback state.

The LXT944 provides an additional loopback function. **External loopback mode**, useful for system-level testing, is controlled by the LEDC*x*/FDE*x* pins. With both LEDC*x*/FDE*x*, and LEDT*x*/LBK*x*, or the global Loopback pins Low, the LXT944 device:

- disables internal loopback circuits
- disables SQE
- disables the collision detection circuitry
- enables full duplex mode

This allows for external loopback testing. This can be controlled on a per port basis using the individual port controls or globally by using the "Loopback" pin.

Full Duplex Operation

Full duplex operation is enabled by driving the LEDC*x*/FDE*x* pins with an open collector driver. The LEDCFN pin when enabled will disable the collision LED driver and allow the LEDC*x*/FDE*x* pin to be driven by a TTL driver to enable or disable the full duplex operation of the TP ports.

LED Driver Functions

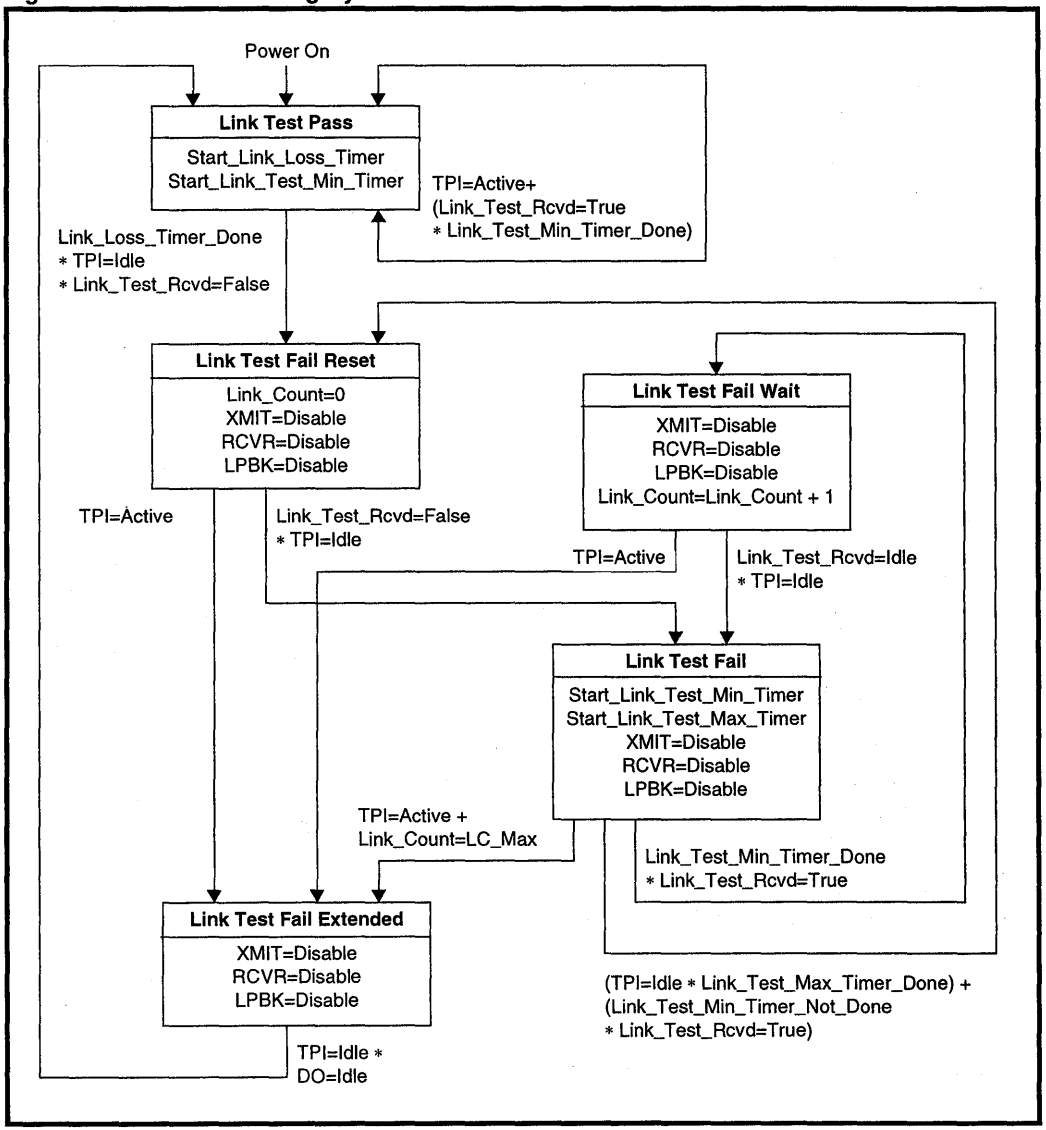
The LXT944 supports individual LED drivers for each port. Per-port LED drivers include link (both half & full duplex), receive, transmit, and collision. The signal pulse widths on all activity outputs (receive, transmit, and collision) are a minimum of a 100 ms to increase visual recognition of the LED status.

The LINK*x* signals are TTL level outputs indicating link pass state for both half and full duplex operation. The signal is active Low and can be read as a status bit or be used to activate port link LEDs.

Link Integrity Test Function

Figure 6 is a state diagram of the LXT944 Link Integrity Test function. The link integrity test is used to determine the status of the receive side twisted-pair cable. Link integrity testing is always enabled unless the loopback function is enabled (LBK or Loopback = High). When enabled, the receiver recognizes link integrity pulses which are transmitted in the absence of receive traffic. If no serial data stream or link integrity pulses are detected within 50-150 ms, the device enters a link fail state and disables the transmit and normal loopback functions. The LXT944 ignores any link integrity pulse with an interval less than 2-7 ms. The LXT944 will remain in the Link Fail state until it detects either a serial data packet or two or more link integrity pulses.

Figure 6: LXT944 Link Integrity Test Function State Machine



APPLICATION INFORMATION

The following diagrams group similar pins; they do not portray the actual chip pinout. The controller interface pins (transmit, data, clock, and enable; receive data and clock; and the collision detect and carrier detect pins) are at the upper left.

The VCC and GND pins are at the bottom of each diagram. All VCC pins use a single power supply with decoupling capacitors installed between the VCC and GND pins and their respective planes.

Magnetics Information

The LXT944 requires a 1:1 ratio for the receive transformers and a 1:$\sqrt{2}$ ratio for the transmit transformers. The LXT944 uses the same magnetics which are currently used on the LXT914 Quad Repeater. Various front end design options are available: a simple per port Rx/Tx pair configuration (see Figure 7), the receive quad and the transmit quad (see Figure 8), and the new single 40 pin octal transformer configuration (see Figure 9).

Transformers for these designs are available from various manufacturers (see Table 8) is a list of available Quad and Single port transformers with manufacturers and their part numbers. Before committing to a specific component, designers should test and validate all specifications of the magnetics used in all applications.

Table 8: Magnetics Manufacturers

Mfgr.	Quad Tx	Quad Rx	Tx/Rx Pairs
Bell Fuse	S553-5999-02	S553-5999-03	
Fil-Mag	23Z339	23Z338	
HALO	TD54-1006L1 TG54-1006N2	TD01-1006L1 TG01-1006N2	TD42-2006Q TD43-2006K TG42-1406N1 TG43-1406N
(Octal)			TG44-S010NX
Kappa	TP4003P	TP497P101	
Nan-opulse	5976	5977	
PCA	EPE6009	EPE6010	
VALOR	PT4116	PT4117	PT4069N1 PT4068N1 ST7011S2 ST7010S2

Layout Requirements

The Twisted-Pair Interface

The four, twisted-pair output circuits are identical. Each TPDOP/TDPON signal has a 24.9 Ω, 1%, series resistor and a 120 pF capacitor differentially across the positive and negative outputs. These signals go directly to a 1:$\sqrt{2}$ transformer creating the necessary 100 Ω termination for the cable. The TPDIP/TPDIN signals have a 100 Ω resistor across the positive and negative input signals to terminate the 100 Ω signal received from the line. To calculate the impedance on the output line interface, use:

$$(24.9\ \Omega + 24.9\ \Omega) * \sqrt{2}^2 \approx 100\ \Omega.$$

The layout of the twisted-pair ports is critical in complex designs. Run the signals directly from the device to the discrete termination components (located close to the transformers).

The transformer isolation voltage should be rated at 2 kV to protect the circuitry from static voltages across the connectors and cables. The signals running from the transformers to the connector should run in close pairs directly to the connector. Be careful not to cross the transmit and receive pairs. One way to avoid a problem is to run the receive pairs on the component side and the transmit pairs on the solder side. Careful planning during the schematic and layout stages can avoid these problems.

The PCB layout should have no ground or power planes between the transformers and the connectors. The data signals should be the only traces in this area. Place the chassis ground for the connectors near the edge of the PCB, away from the signals, connecting the connector shield with the chassis.

The RBIAS Pin

The RBIAS signal sets the levels for the output drivers of the LXT944. Any emissions or common mode noise entering the device here could be measured on the twisted-pair output signals.

The LXT944 requires a 7.5 kΩ, 1% resistor directly connected between pin 68 and ground. These traces should be as short as possible. The ground signals from pins 67 & 69 should come directly off of the device to enclose the resistor and pin forming a shielded area between the RBIAS connection and the switching signals on the PCB.

Figure 7: Simple Receive/Transmit on Each Port Application

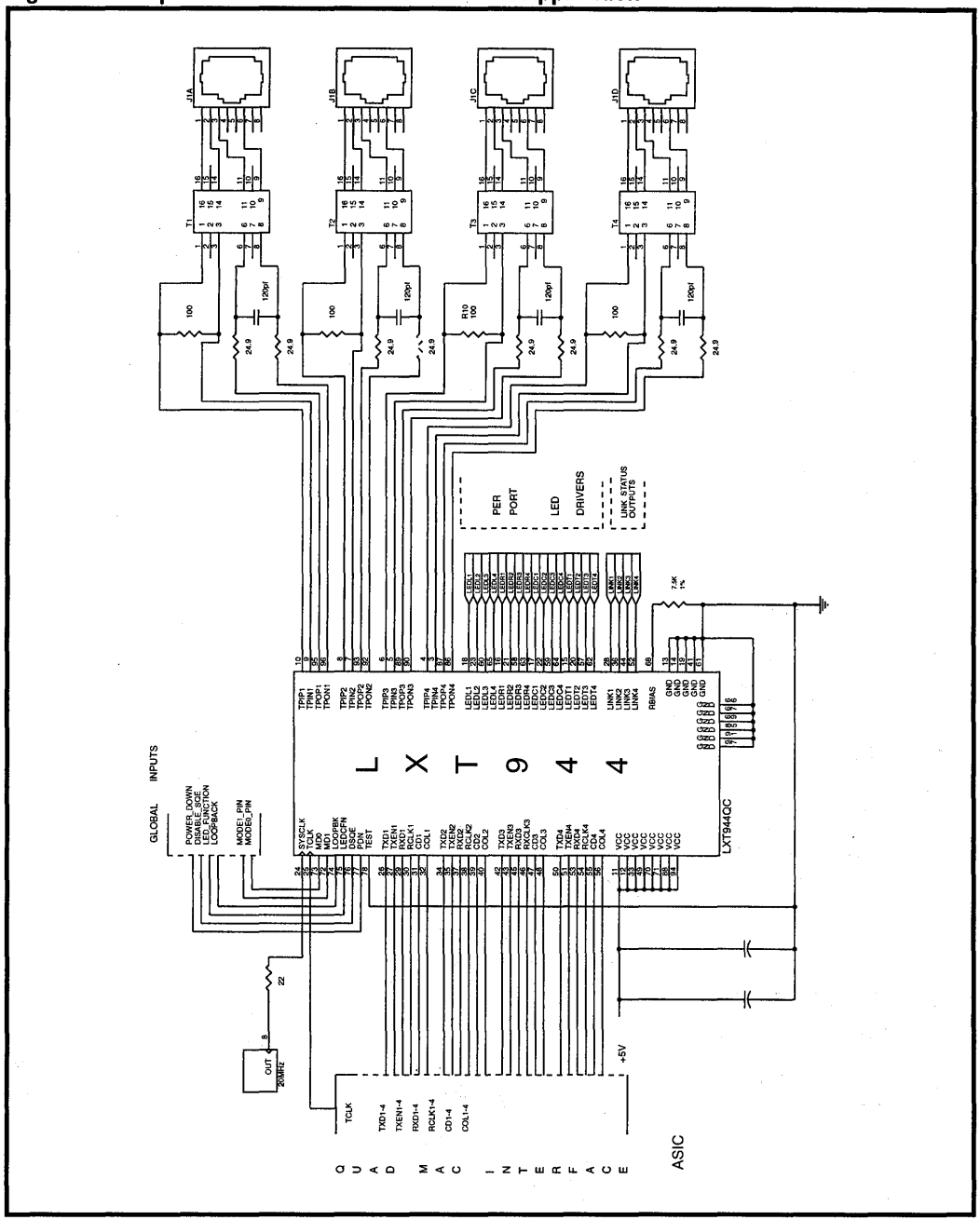


Figure 8: Receive Quad and Transmit Quad Application

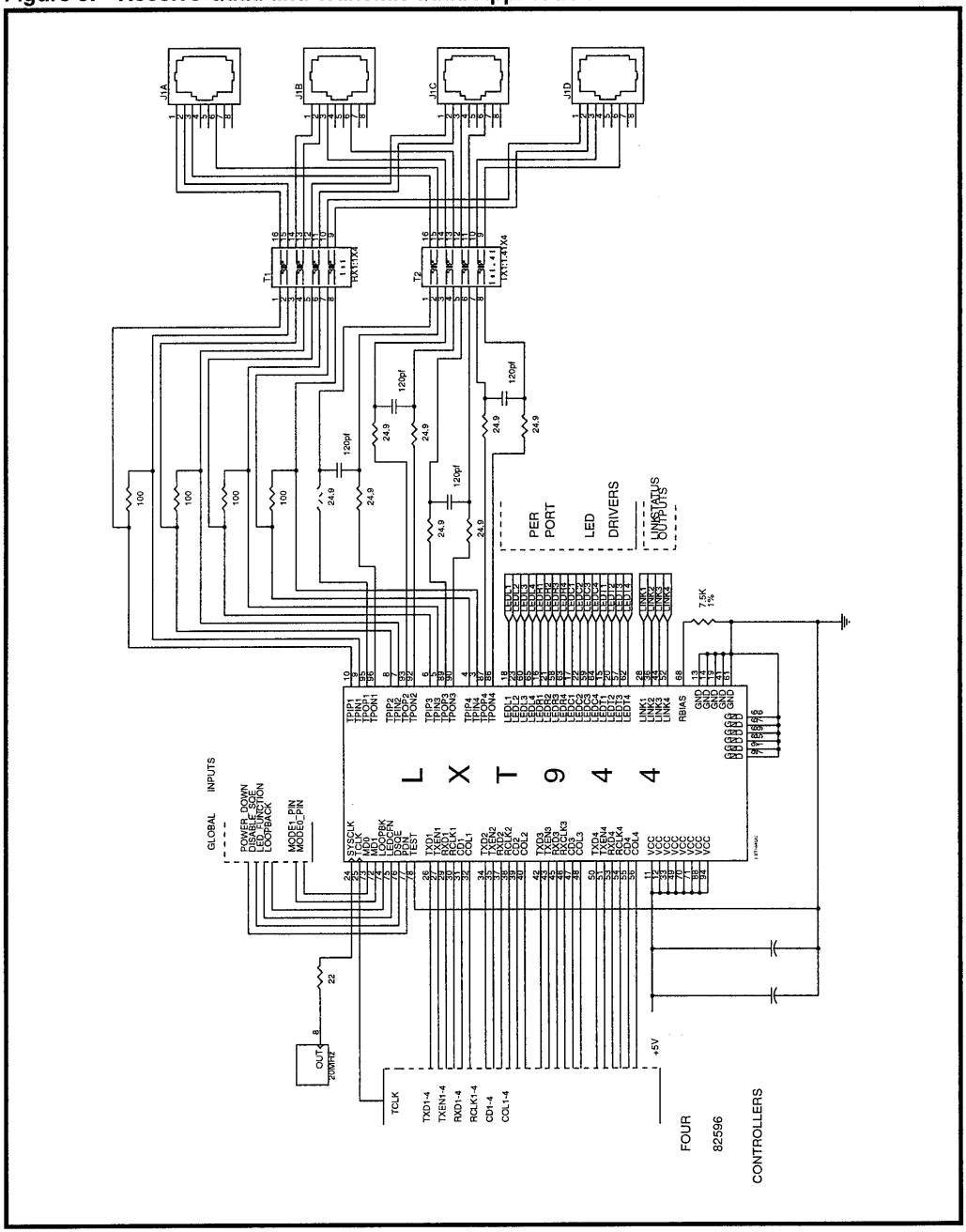
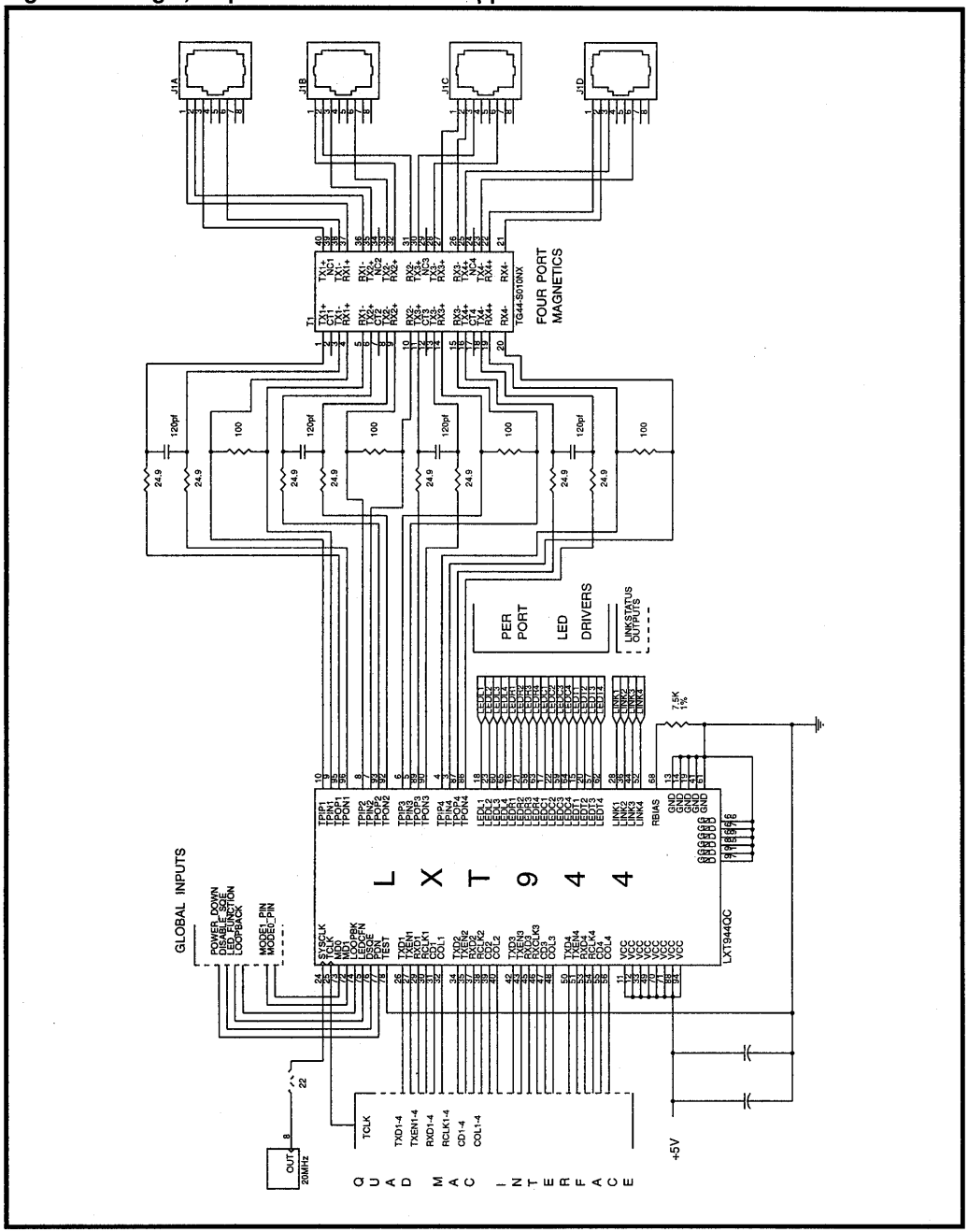


Figure 9: Single, 40-pin Octal Transformer Application



TEST SPECIFICATIONS

NOTE

The minimum and maximum values in Tables 9 through 17 and Figures 10 through 25 represent the performance specifications of the LXT944 and are guaranteed by test, except where noted by design

Table 9: Absolute Maximum Values

Parameter	Symbol	Min	Max	Units
Supply Voltage	VCC	-0.3	6	V
Operating Temperature	TOP	0	70	°C
Storage Temperature	TST	-65	+150	°C

CAUTION

Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 10: Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Recommended Supply Voltage[1]	VCC	4.75	5.0	5.25	V	
Recommended Operating Temperature	TOP	0	-	70	°C	

1. Voltages with respect to ground unless otherwise specified.

Table 11: I/O Electrical Characteristics (Over Recommended Range)

Parameter		Sym	Min	Typ[1]	Max	Units	Test Conditions
Input Low voltage		VIL	–	–	0.8	V	
Input High voltage		VIH	2.0	–	–	V	
Output Low voltage		VOL	–	–	0.4	V	IOL = 1.6 mA
		VOL	–	–	10	%VCC	IOL < 10 µA
Output Low voltage - LEDs		VOLL	–	–	1.0	%VCC	IOLL = 5 mA
Output High voltage		VOH	2.4	–	–	V	IOH = 40 µA
		VOH	90	–	–	%VCC	IOH < 10 µA
Output High voltage - LEDs		VOHL	2.4	–	–	V	IOHL = -5 mA
Input Low current		IIL	–	–	2	mA	VOL = .4 V
Output Rise Time	CMOS	-	-	3	15	ns	CLOAD = 20 pF
TCLK & RCLK	TTL	-	-	2	15	ns	
Output Fall Time	CMOS	-	-	3	15	ns	CLOAD= 20 pF
TCLK & RCLK	TTL	-	-	2	15	ns	

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 11: I/O Electrical Characteristics (Over Recommended Range) – continued

Parameter		Sym	Min	Typ[1]	Max	Units	Test Conditions
CLKI rise time (externally driven)		-	-	-	10	ns	
CLKI duty cycle (externally driven)		-	-	50/50	40/60	%	
Supply Current	Normal Mode	ICC	0	140	200	mA	Idle
	Normal Mode	ICC	0	180	220	mA	Transmitting on TP
	Power Down Mode	ICC	-	0.1	100	µA	

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 12: Twisted-Pair Electrical Characteristics (Over Recommended Range)

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Transmit output impedance	ZOUT	–	2	–	Ω	
Transmit timing jitter addition[2]	–	–	±6.4	±10	ns	0 line length for internal MAU
Transmit timing jitter added by the MAU and PLS sections[2, 3]	–	–	±3.5	±5.5	ns	After line model specified by IEEE 802.3 for 10BASE-T internal MAU
Receive input impedance	ZIN	–	24	–	kΩ	Between TPIP/TPIN
Differential Squelch Threshold	VDS	300	420	585	mV	5 MHz square wave input

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Guaranteed by design; not subject to production testing.
3. IEEE 802.3 specifies maximum jitter additions at 0.5 ns from the encoder and 3.5 ns from the MAU.

Table 13: Switching Characteristics (Over Recommended Range)

Parameter		Sym	Min	Typ[1]	Max	Units
Jabber Timing	Maximum Transmit Timing	-	20	-	150	ms
	Unjab Timing	-	250	-	750	ms
Link Integrity Timing	Time Link Loss Receive	-	50	-	150	ms
	Link Min Receive	-	2	-	7	ms
	Link Max Receive	-	50	-	150	ms
	Link Transmit Period	-	8	10	24	ms

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 14: RCLK/Start-of-Frame Timing (Over Recommended Range)

Parameter	Sym.	Min	Typ[1]	Max	Units
Decoder acquisition time	tDATA	-	900	1100	ns
CD turn-on delay	tCD	-	50	200	ns

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 14: RCLK/Start-of-Frame Timing (Over Recommended Range) – continued

Parameter		Sym.	Min	Typ[1]	Max	Units
Receive data setup from RCLK	Mode 1	tRDS	60	70	-	ns
	Modes 2, 3 and 4	tRDS	30	45	-	ns
Receive data hold from RCLK	Mode 1	tRDH	10	20	-	ns
	Modes 2, 3 and 4	tRDH	30	45	-	ns
RCLK shut off delay from CD assert (Mode 3)		tSWS	-	±100	-	ns

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 15: RCLK/End-of-Frame Timing (Over Recommended Range)

Parameter	Type	Sym	Mode 1	Mode 2	Mode 3	Mode 4	Units
RCLK after CD off	Minimum	tRC	5	1	27	5	bit times
Rx data throughput delay	Maximum	tRD	400	375	375	375	ns
CD turn off delay [1]	Maximum	tCDOFF	500	475	475	475	ns
Receive block out after TEN off [2]	Typical[3]	tIFG	5	50	-	-	bit times
RCLK switching delay after CD off	Typical[3]	tSWE	-	-	120 (±80)	-	bit times

1. CD Turnoff delay measured from middle of last bit; timing specification is unaffected by the value of the last bit.
2. Blocking of Carrier Detect is disabled during full duplex operation.
3. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.

Table 16: Transmit Timing (Over Recommended Range)

Parameter	Symbol	Minimum	Typical [1]	Maximum	Units
TEN Setup from TCLK	tEHCH	22	-	-	ns
TXD Setup from TCLK	tDSCH	22	-	-	ns
TEN Hold after TCLK	tCHEL	5	-	-	ns
TXD Hold after TCLK	tCHDU	5	-	-	ns
Transmit Start-up Delay	tSTUD	-	350	450	ns
Transmit Through-put Delay	tTPD	-	338	350	ns

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.

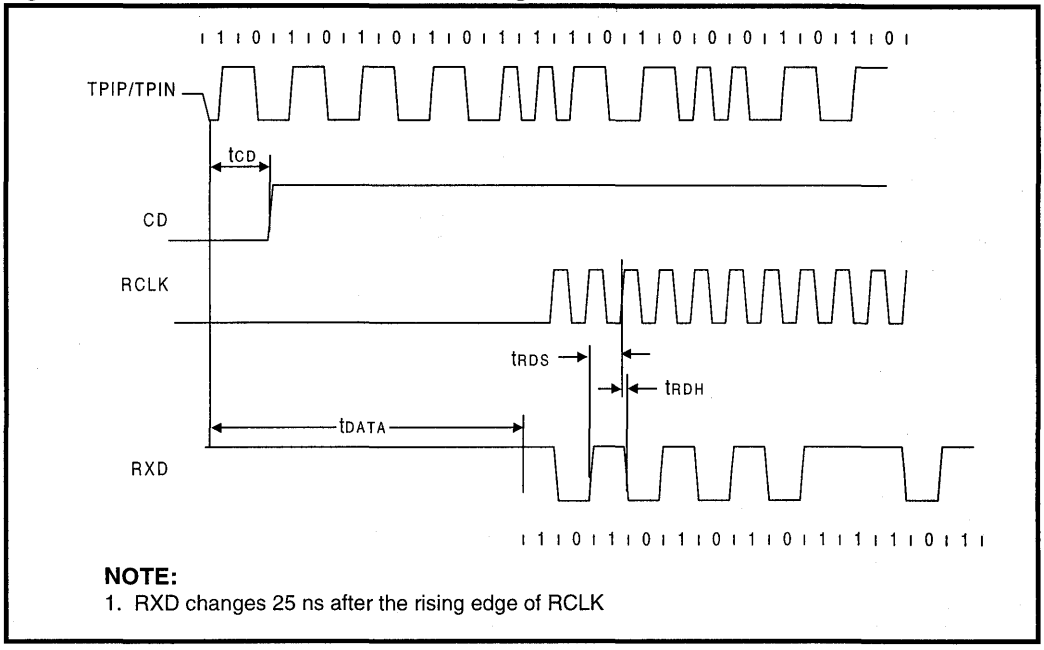
Table 17: Miscellaneous Timing (Over Recommended Range)

Parameter	Symbol	Minimum	Typical [1]	Maximum	Units
COL (SQE) Delay after TEN off	tSQED	0.65	-	1.6	µs
COL (SQE) Pulse Duration	tSQEP	500	-	1500	ns
Power Down recovery time	tPDR	-	TBD	-	ms

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.

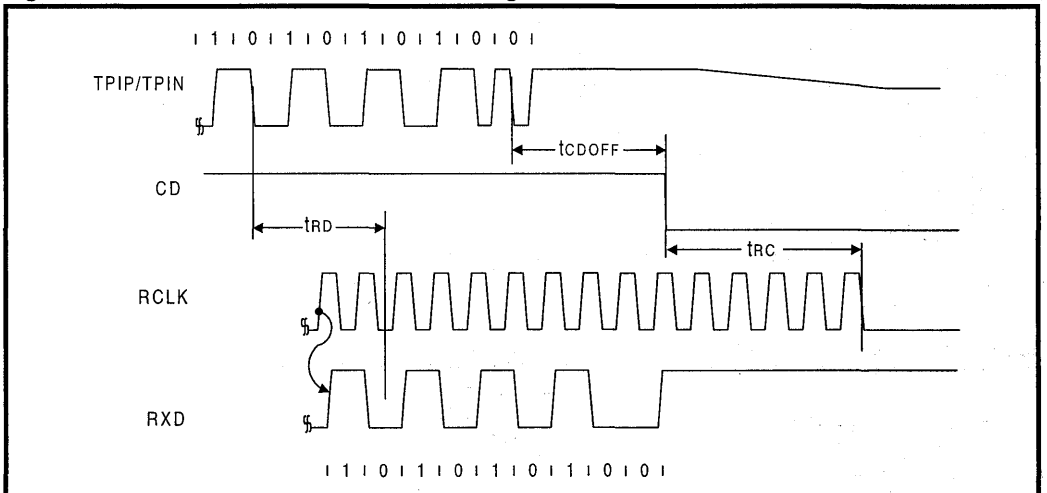
Timing Diagrams for Mode 1 *(MD1=Low, MD0=Low) Figures 10 through 13*

Figure 10: Mode 1 RCLK/Start-of-Frame Timing



NOTE:
1. RXD changes 25 ns after the rising edge of RCLK

Figure 11: Mode 1 RCLK/End-of-Frame Timing



NOTE:
1. RXD changes 25 ns after the rising edge of RCLK

Figure 12: Mode 1 Transmit Timing

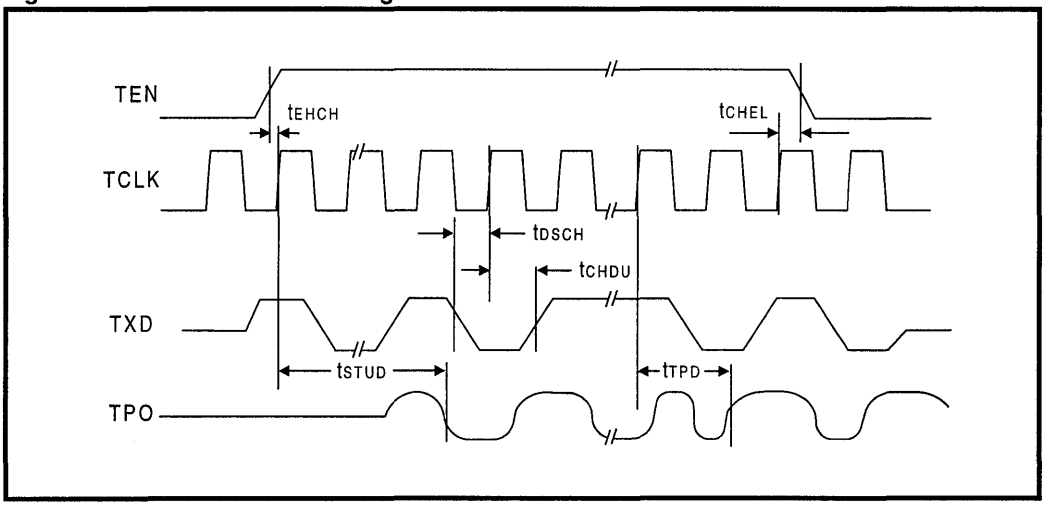
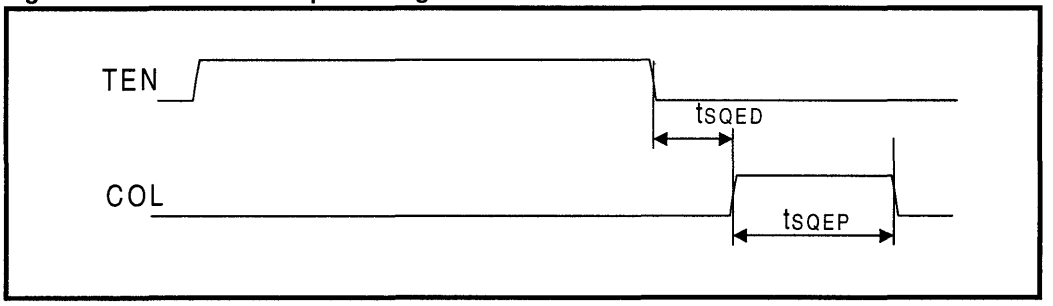
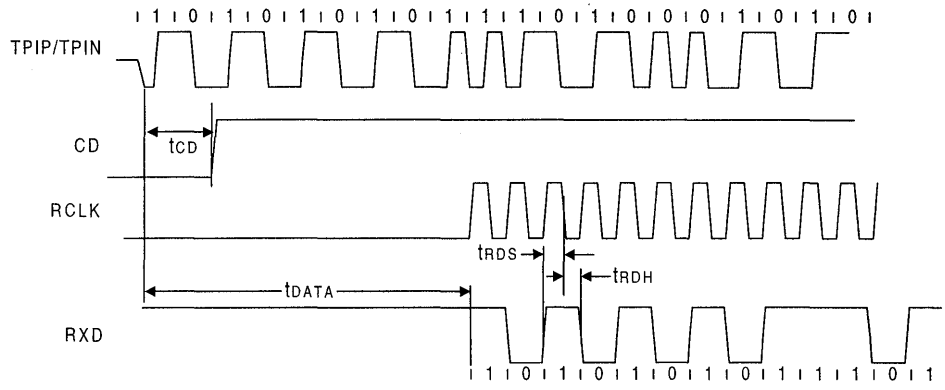


Figure 13: Mode 1 COL Output Timing



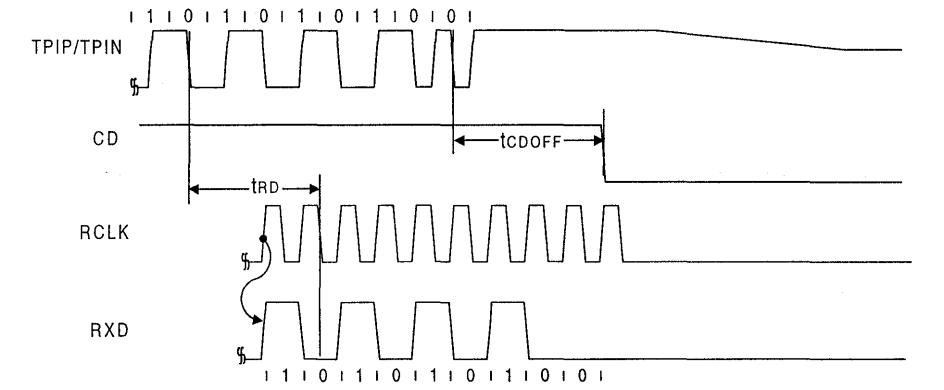
Timing Diagrams for Mode 2 *(MD1=Low, MD0=High) Figures 14 through 17*

Figure 14: Mode 2 RCLK/Start-of-Frame Timing



NOTE:
1. RXD changes at the rising edge of RCLK; the controller is sampled at the falling edge.

Figure 15: Mode 2 RCLK/End-of-Frame Timing



NOTE:
1. RXD changes at the rising edge of RCLK; the controller is sampled at the falling edge.

Figure 16: Mode 2 Transmit Timing

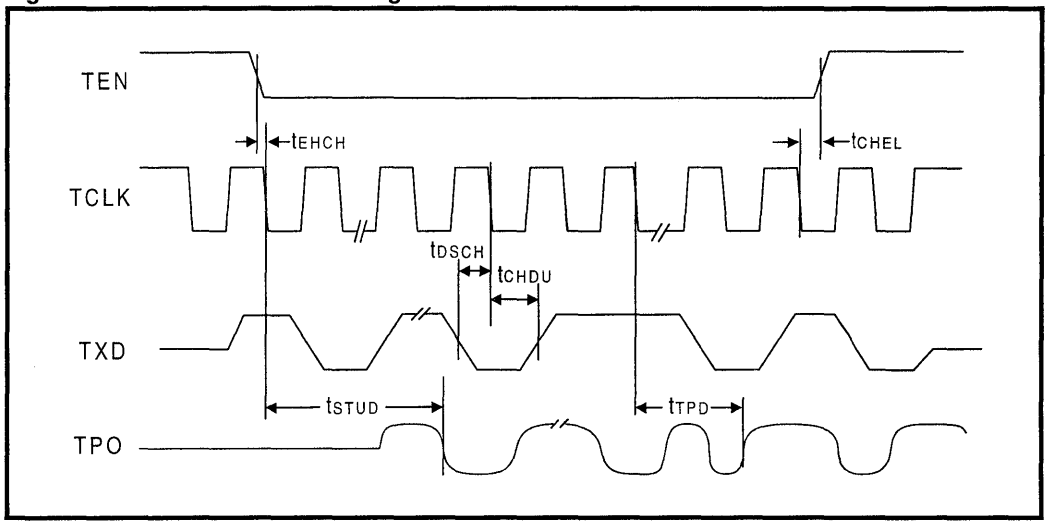
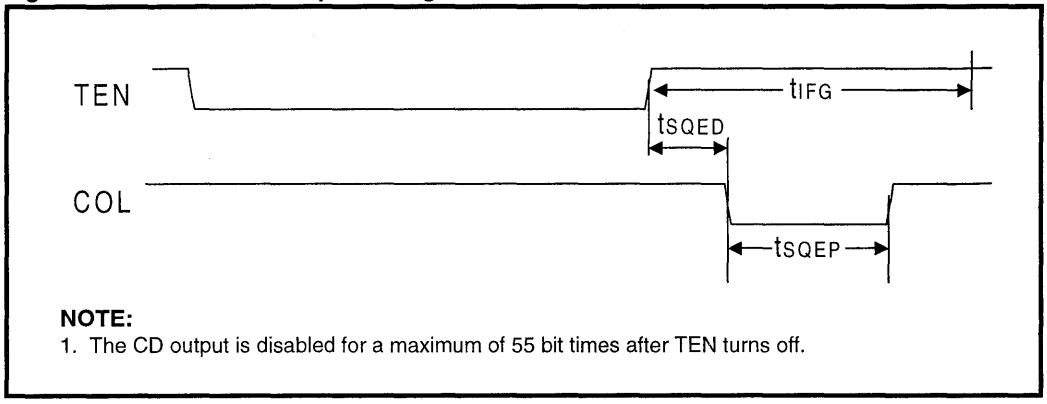


Figure 17: Mode 2 COL Output Timing



NOTE:
1. The CD output is disabled for a maximum of 55 bit times after TEN turns off.

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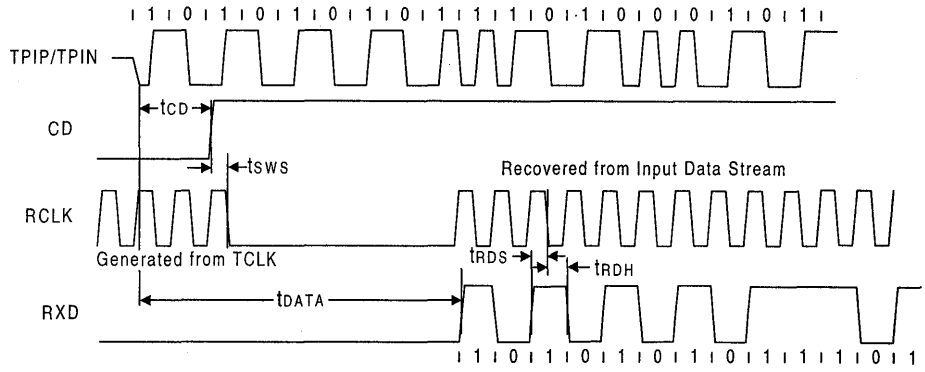
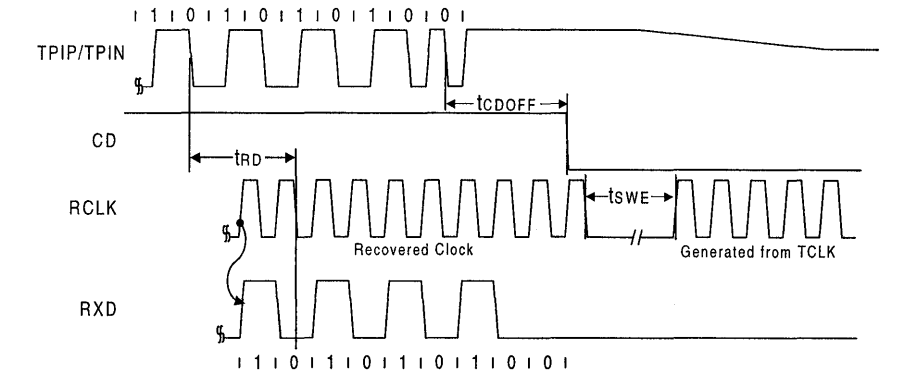
Timing Diagrams for Mode 3 *(MD1=High, MD0=Low) Figures 18 through 21*

Figure 18: Mode 3 RCLK/Start-of-Frame Timing



NOTE:
1. RXD changes at the rising edge of RCLK; the controller is sampled at the falling edge.

Figure 19: Mode 3 RCLK/End-of-Frame Timing



NOTE:
1. RXD changes at the rising edge of RCLK; the controller is sampled at the falling edge.

Figure 20: Mode 3 Transmit Timing

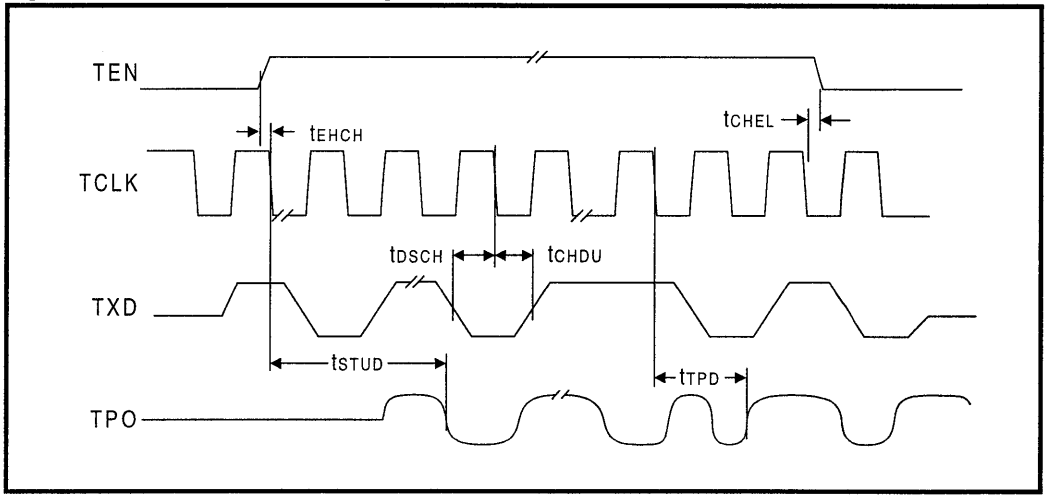
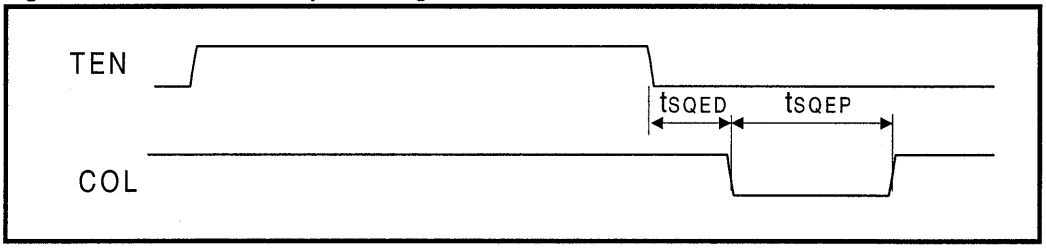


Figure 21: Mode 3 COL Output Timing



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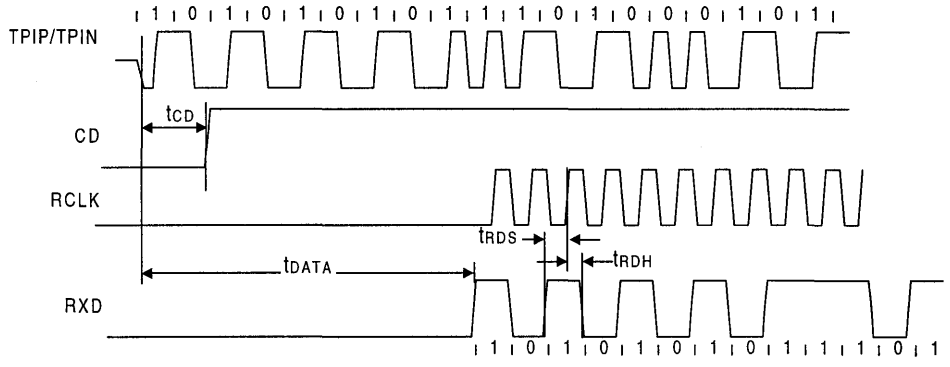
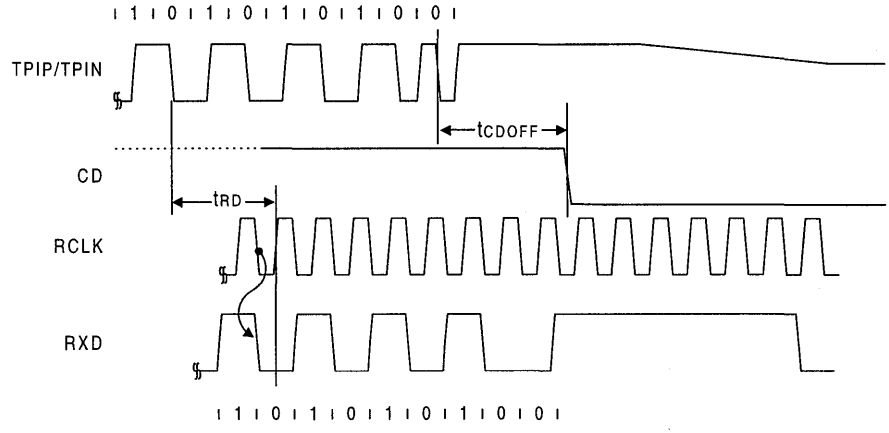
Timing Diagrams for Mode 4 *(MD1=High, MD0=High) Figures 22 through 25*

Figure 22: Mode 4 RCLK/Start-of-Frame Timing



NOTE:
1. RXD changes at the falling edge of RCLK; the controller is sampled at the rising edge.

Figure 23: Mode 4 RCLK/End-of-Frame Timing



NOTE:
1. RXD changes at the falling edge of RCLK; the controller is sampled at the rising edge.

Figure 24: Mode 4 Transmit Timing

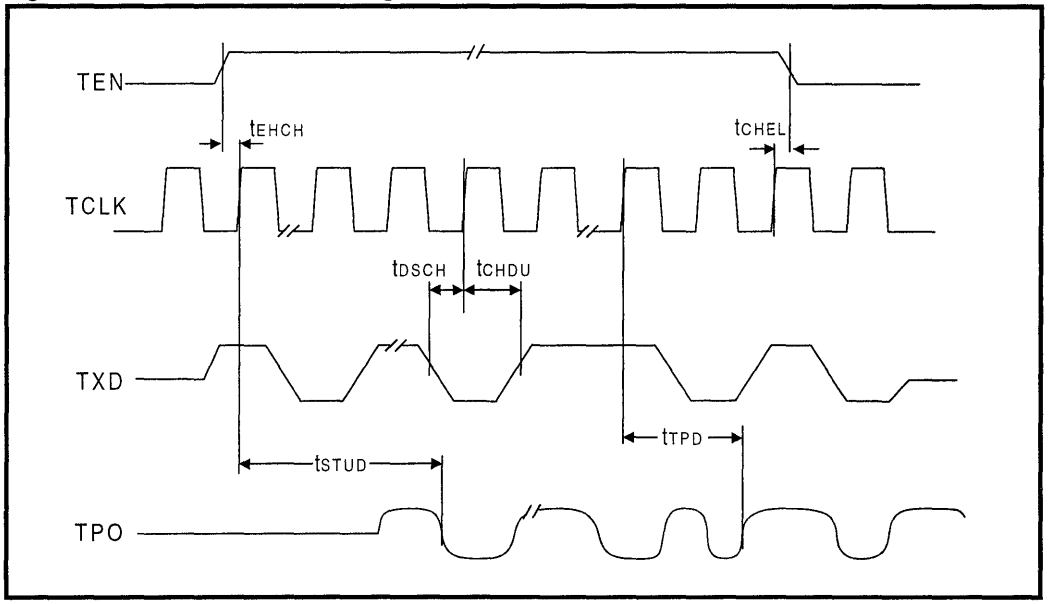
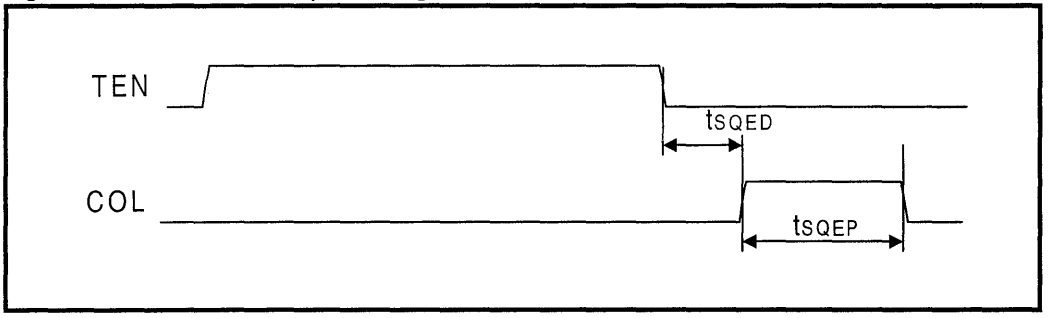


Figure 25: Mode 4 COL Output Timing



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NOTES

LXT970

Fast Ethernet Transceiver

General Description

The LXT970 Fast Ethernet Transceiver supports IEEE 802.3 compliant Ethernet applications at both 10 and 100Mbps operation. It provides the active circuitry to interface 802.3 media independent interface (MII) compliant controllers to 10BASE-T and/or 100BASE-TX media. The LXT970 also provides an ECL-type interface for use with 100BASE-FX fiber networks.

The LXT970 supports full duplex operation at 10 and 100 Mbps. Its operating condition can be set using auto-negotiation, parallel detection or manual control. The encoder can be bypassed for symbol mode applications.

The LXT970 is fabricated with an advanced CMOS process and requires only a single 5 volt power supply. The MII may be operated independently with either a 5 volt supply or a 3.3 volt supply.

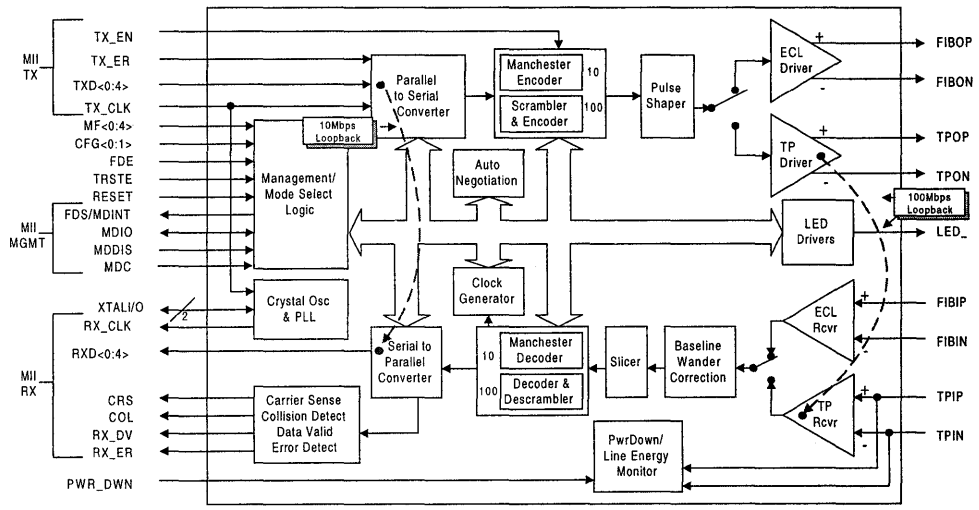
Applications

- Combination 10BASE-T/100BASE-TX Network Interface Cards (NICs)
- 10/100 Switches, 10/100 Repeaters
- 100BASE-FX Network Interface Cards (NICs)

Features

- IEEE 802.3 Compliant:
  - 10BASE-T and 100BASE-TX using a single RJ45 connection
  - Supports both auto-negotiation via Fast Link Pulse (FLP) exchange and parallel detection for legacy 10BASE-T and 100BASE-TX systems
  - MII interface with extended register capability
- Baseline wander correction
- 100BASE-FX fiber optic capable
- Standard CSMA/CD or full duplex operation at 10 or 100 Mbps
- Configurable through MII serial port or via external control pins
- Configurable for DTE, repeater or switch applications
- CMOS process with single 5 volt supply operation with provision for interface to 3.3 V MII bus
- Integrated transmit and receive filtering for 10BASE-T and 100BASE-TX
- Integrated LED drivers
- Integrated supply monitor and line disconnect during low supply fault

LXT970 Block Diagram



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PIN ASSIGNMENTS AND SIGNAL DESCRIPTIONS

Figure 1: LXT970 Pin Assignments and Signal Descriptions

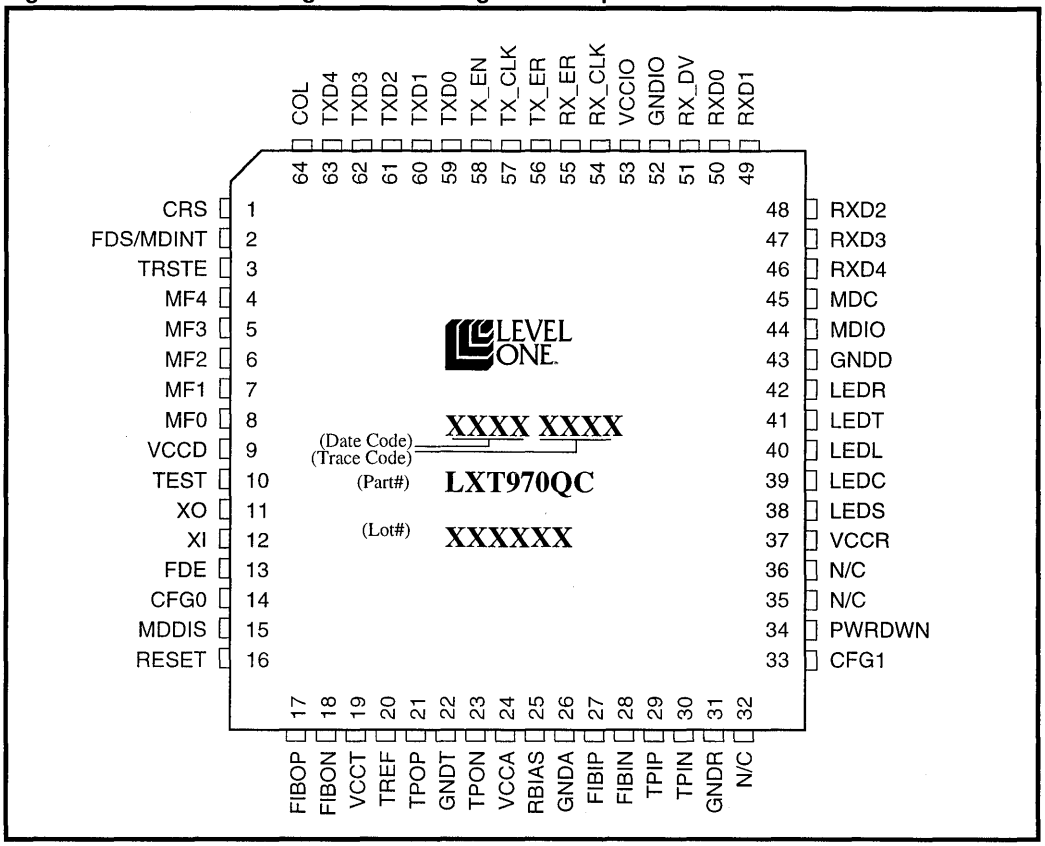

Table 1: LXT970 Power Supply Signal Descriptions

Pin#	Pin Name	I/O	Pin Description
19 22	VCCT GNDT	-	**Transmitter Supply** (+5V) and **Ground**.
37 31	VCCR GNDR	-	**Receiver Supply** (+5V) and **Ground**.
24 26	VCCA GNDA	-	**Analog Supply** (+5V) and **Ground**.
9 43	VCCD GNDD	-	**Digital Supply** (+5V) and **Ground**.
53 52	VCCIO GNDIO	-	**MII Supply** (+3.3V or +5V) and **Ground**.

Table 2: LXT970 MII Signal Descriptions

Pin#	Pin Name	I/O[1]	Pin Description
			MII Data Interface Pins
63 62 61 60 59	TXD4 TXD3 TXD2 TXD1 TXD0	I	**Transmit Data**. The MAC drives data to the LXT970 using these inputs. TXD4 is monitored only in Symbol (5B) Mode. These signals must be synchronized to the TX_CLK.
58	TX_EN	I	**Transmit Enable**. The MAC asserts this signal when it drives valid data on the TXD inputs. This signal must be synchronized to the TX_CLK.
57	TX_CLK	I/O	**Transmit Clock**. 25 MHz for 100 Mbps operation, 2.5 MHz for 10 Mbps operation. Refer to the Clock Requirements discussion in the Functional Description section.
56	TX_ER	I	**Transmit Coding Error**. The Media Access Controller (MAC) asserts this input when an error has occurred in the transmit data stream. When the LXT970 is operating at 100Mbps, the LXT970 responds by sending "Invalid Code Symbols" on the line.
46 47 48 49 50	RXD4 RXD3 RXD2 RXD1 RXD0	O	**Receive Data**. The LXT970 drives received data on these outputs, synchronous to RX_CLK. RXD4 is driven only in Symbol (5B) Mode.
51	RX_DV	O	**Receive Data Valid**. The LXT970 asserts this signal when it drives valid data on RXD. This output is synchronous to RX_CLK.
55	RX_ER	O	**Receive Error**. The LXT970 asserts this output when it receives invalid symbols from the network. This signal is synchronous to RX_CLK.
54	RX_CLK	O	**Receive Clock**. 25 MHz for 100 Mbps operation, 2.5 MHz for 10 Mbps operation. Refer to the Clock Requirements discussion in the Functional Description section.
64	COL	O	**Collision Detected**. The LXT970 asserts this output when a collision is detected. This output remains High for the duration of the collision. This signal is asynchronous and is inactive during full duplex operation.
1	CRS	O	**Carrier Sense**. During half-duplex operation (bit 0.8 = 0)[2], the LXT970 asserts this output when either transmit or receive medium is non-idle. During full-duplex operation (bit 0.8 = 1) or repeater operation (bit 19.13 = 1), CRS is asserted only when the receive medium is non-idle.
3	TRSTE	I	**Tristate**. In DTE Mode (19.13 = 0), when TRSTE input is High, the LXT970 isolates itself from the MII Data Interface, and controls the MDIO register bit 0.10 (Isolate bit). When MDDIS is High, TRSTE provides continuous control over bit 0.10. When MDDIS is Low, TRSTE sets initial (default) values only and reverts control back to the MDIO interface. In Repeater Mode (19.13 = 1), when TRSTE input is High, the LXT970 tri-states the receive outputs of the MII (RXD<4:0>, RX_DV, RX_ER, RX_CLK).

1. I/O Column Coding: I = Input, O = Output, OD = Open Drain
2. The LXT970 supports the 802.3 MDIO register set. Specific bits in the registers are referenced using an "X.Y" notation, where X is the register number (0-31) and Y is the bit number (0-15).

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Table 2: LXT970 MII Signal Descriptions – continued

Pin#	Pin Name	I/O[1]	Pin Description
			MII Control Interface Pins
15	MDDIS	I	**Management Disable**. When MDDIS is High, the MDIO is restricted to Read Only and the MF<4:0>, CFG<1:0> and FDE pins provide continual control of their respective bits. When MDDIS is Low at power up or Reset, the MF<4:0>, CFG<1:0> and FDE pins control only the initial or "default" values of their respective register bits. After the power-up/reset cycle is complete, bit control reverts to the MDIO serial channel.
45	MDC	I	**Management Data Clock**. Clock for the MDIO serial data channel. Maximum frequency is 2.5 MHz.
44	MDIO	I/O	**Management Data Input/Output**. Bidirectional serial data channel for PHY/STA communication.
2	FDS/MDINT	OD	**Full Duplex Status**. When bit 17.1 = 0 (default), this pin indicates full duplex status. (High = Full Duplex, Low = Half Duplex) This pin can drive a high efficiency LED. (See Table 22 for detail specifications). **Management Data Interrupt**. When bit 17.1 = 1, an active Low output on this pin indicates status change. Interrupt is cleared by sequentially reading Register 1, then Register 18.

1. I/O Column Coding: I = Input, O = Output, OD = Open Drain
2. The LXT970 supports the 802.3 MDIO register set. Specific bits in the registers are referenced using an "X.Y" notation, where X is the register number (0-31) and Y is the bit number (0-15).

Table 3: LXT970 Fiber Interface Signal Descriptions

Pin#	Pin Name	I/O	Pin Description
17 18	FIBOP FIBON	O	**Fiber Output, Positive and Negative**. Differential pseudo-ECL driver pair compatible with standard fiber transceiver for 100BASE-FX.
27 28	FIBIP FIBIN	I	**Fiber Input, Positive and Negative**. Differential pseudo-ECL receive pair compatible with standard fiber transceiver for 100BASE-FX.

1. I/O Column Coding: I = Input, O = Output

Table 4: LXT970 Twisted Pair Interface Signal Descriptions

Pin#	Pin Name	I/O	Pin Description
21 23	TPOP TPON	AO	**Twisted Pair Output, Positive and Negative**. Differential driver pair produces 802.3-compliant pulses for either 100BASE-TX or 10BASE-T transmission.
20	TREF	AO	**Transmit Reference**. Tie to center tap of output transformer.
29 30	TPIP TPIN	AI	**Twisted Pair Input, Positive and Negative**. Differential input pair for either 100BASE-TX or 10BASE-T reception.

1. I/O Column Coding: I = Input, O = Output, A = Analog

Table 5: LXT970 LED Indicator Signal Descriptions

Pin#	Pin Name	I/O	Pin Description
38	LEDS	O	**Speed LED**. Active Low output indicates 100 Mbps operation is selected.
42	LEDR	O	**Receive LED**. Active Low output indicates that receiver is active.
41	LEDT	O	**Transmit LED**. Active Low output indicates transmitter is active.
40	LEDL	O	**Link LED**. Active Low output; During 100 Mbps operation, indicates scrambler lock and receipt of valid Idle codes. During 10 Mbps operation, indicates Link Valid status.
39	LEDC	O	**Collision LED**. In default mode, active Low output indicates collision. However, LEDC is programmable and may be set for other indications. For programming options, see Configuration Register 19 in Table 53.

1. I/O Column Coding: O = Output

Table 6: LXT970 Miscellaneous Signal Descriptions

Pin#	Pin Name	I/O	Pin Description
10	TEST	I	**Test**. Must be tied Low.
12 11	XI XO	I O	**Crystal Input and Output**. A 25 MHz crystal oscillator circuit can be connected across XI and XO. A clock can also be used at XI. Refer to Functional Description for detailed clock requirements.
25	RBIAS	AI	**Bias Control**. Controls operating circuit bias via an external 22 kΩ, 1% resistor to ground.
16	RESET	I	**Reset**. This active Low input is OR'ed with the control register Reset bit (0.15). The LXT970 reset cycle is extended 205ns (nominal) after Reset is de-asserted.
34	PWRDWN	I	**Power Down**. When High, forces LXT970 into power down mode. This pin is OR'ed with the Power Down bit (0.11). Refer to Table 43 for more information.
32, 35, 36	N/C	-	**No Connection**. Leave open.

1. I/O Column Coding: I = Input, O = Output, A = Analog

Table 7: LXT970 Hardware Control Interface Signal Descriptions

Pin#	Pin Name	I/O	Pin Description
	MF0 - MF4	I	**Multi-Function (MF).** Each pin has two independent settings that are established by 4-level supply voltages. The first setting (ADD), determines the PHY address on the MDIO bus and the second setting (FUNC), determines configuration of the LXT970. The MF inputs directly affect particular bits in the MDIO register set. The effect is mediated by the MDDIS pin. When MDDIS is High, these inputs continually affect the MDIO registers. When MDDIS is Low, they determine initial (default) values only. Table 21 shows the 4-level supply voltages (voltage levels referred to as VMF1, VMF2, VMF3 and VMF4) that establish the settings per pin. An external voltage divider, as shown in the Layout Requirement section, is required to establish mid-level (VMF2 and VMF3) settings. VMF1 and VMF4 (default) settings, can be established with the LXT970 standard power supply and do not require a voltage divider. Tables 8 and 9 show the selected MF pin function and address with respect to the applied input voltage level. The descriptions below detail the configuration of each of these pins.
8	MF0	I	Enables Auto-Negotiation (A/N) and directly affects MDIO register bit 0.12. When input value = VMF1 or VMF4, A/N is disabled and 0.12 = 0. When input value = VMF2 or VMF3, A/N is enabled and 0.12 = 1.
7	MF1	I	Selects Repeater Mode and directly affects MDIO register bit 19.13. When input value = VMF1 or VMF4, DTE Mode is enabled and 19.13 = 0. When input value = VMF2 or VMF3, Repeater Mode is enabled and 19.13 = 1.
6	MF2	I	In TX mode, selects 4B Nibble (normal) or 5B Symbol Mode and directly affects MDIO register bit 19.4. When input value = VMF1 or VMF4, 4B Nibble Mode is selected and 19.4 = 0. When input value = VMF2 or VMF3, 5B Symbol Mode is selected and 19.4 = 1.
5	MF3	I	In TX mode, enables or bypasses Scrambler operation and directly affects MDIO register bit 19.3. When input value = VMF1 or VMF4, Scrambler is enabled and 19.3 = 0. When input value = VMF2 or VMF3, Scrambler is bypassed and 19.3 = 1. In FX mode, the LXT970 *automatically* bypasses the Scrambler. *Selecting* Scrambler bypass in FX mode will cause the LXT970 to also bypass the 4B/5B encoder and enable Symbol mode MII operation.
4	MF4	I	**When A/N is enabled**, MF4 determines operating speed advertisement capabilities in combination with CFG1. See Table 9 for details. **When A/N is disabled**, this input selects either TX or FX interface. When FX interface is selected, the LXT970 will automatically disable the scrambler. For correct FX operation, 100Mbps operation must also be selected. When input value = VMF1 or VMF4, TX is enabled and 19.2 = 0. When input value = VMF2 or VMF3, FX is enabled and 19.2 = 1.

1. I/O Column Coding: I = Input

Table 7: LXT970 Hardware Control Interface Signal Descriptions – continued

Pin#	Pin Name	I/O	Pin Description
13	FDE	I	**Full Duplex Enable.** **When A/N is enabled**, FDE determines full duplex advertisement capability in combination with MF4 and CFG1. See Table 9 for details. **When A/N is disabled**, FDE directly affects full duplex operation and determines the value of bit 0.8 (Duplex Mode). When FDE is High, F/D is enabled and 0.8 = 1. When FDE is Low, F/D is disabled and 0.8 = 0.
14	CFG0	I	**Configuration Control 0.** **When A/N is enabled,** Low to High transition on CFG0 causes auto-negotiate to re-start and 0.9 = 1. **When A/N is disabled**, this input selects operating speed and directly affects bit 0.13. When CFG0 is High, 100Mbps is selected and 0.13 = 1. When CFG0 is Low, 10Mbps is selected and 0.13 = 0.
33	CFG1	I	**Configuration Control 1.** **When A/N is enabled**, CFG1 determines operating speed advertisement capabilities in combination with MF4. See Table 9 for details. **When A/N is disabled**,CFG1 enables 10Mbps link test function and directly affects bit 19.8. When CFG1 is High, 10Mbps link test is disabled and 19.8 = 1. When CFG1 is Low, 10Mbps link test is enabled and 19.8 = 0.

1. I/O Column Coding: I = Input

Table 8: MF Pin Function Descriptions[1, 3]

Pin	Address / Function	Input Voltage Levels[2] VMF1	VMF2	VMF3	VMF4
MF0	**Address Bit 0**	1	1	0	0
	Auto-Negotiation **Sets the initial value of bit 0.12**	Disabled (0.12 = 0)	Enabled (0.12 = 1)	Enabled (0.12 = 1)	Disabled (0.12 = 0)
MF1	**Address Bit 1**	1	1	0	0
	Repeater / DTE Mode **Sets the initial value of bit 19.13**	DTE (19.13 = 0)	Repeater (19.13 = 1)	Repeater (19.13 = 1)	DTE (19.13 = 0)
MF2	**Address Bit 2**	1	1	0	0
	Nibble (4B) / Symbol (5B) Mode **Sets the initial value of bit 19.4**	Nibble (4B) (19.4 = 0)	Symbol (5B) (19.4 = 1)	Symbol (5B) (19.4 = 1)	Nibble (4B) (19.4 = 0)
MF3	**Address Bit 3**	1	1	0	0
	Scrambler Operation **Sets the initial value of bit 19.3**	Enabled (19.3 = 0)	Bypassed (19.3 = 1)	Bypassed (19.3 = 1)	Enabled (19.3 = 0)
MF4	**Address Bit 4**	1	1	0	0
	If Auto-Negotiate Enabled via MF0, MF4 works in combination with CFG1 to control operating speed and duplex advertisement capabilities via bits 4.5 through 4.8. See Table 9 for details.				
	If Auto-Negotiate Disabled via MF0 Then TX/FX Mode Sets the initial value of bit 19.2	100TX (19.2 = 0)	100FX (19.2 = 1)	100FX (19.2 = 1)	100TX (19.2 = 0)

1. In MDIO Control Mode, the MF pins control only the initial or default value for the respective register bits. In Manual Control mode, the MF pins provide continuous control of the respective register bits.
2. Input Voltage Levels (VMF1, VMF2, VMF3, VMF4) for MF pins.
3. See Tables 10 and 11 for operating configuration set-up.

Table 9: LXT970 Operating Speed/Full Duplex Advertisement Settings

MF4 Input Voltage Levels[2]	CFG1	FDE	MDIO Registers[1]	Function
If Auto-Negotiate Enabled via MF0				
VMF1, VMF4	Low	–	Sets 4.5, 4.6, 4.7 and 4.8 = 1	Advertise all capabilities Ignore FDE
VMF1, VMF4	High	High	Sets 4.5 = 1 Sets 4.7 and 4.8 = 0 Sets 4.6 = 1	Advertise 10 Mbps only FD Advertised
		Low	Sets 4.5 = 1 Sets 4.7 and 4.8 = 0 Sets 4.6 = 0	Advertise 10 Mbps only FD Not Advertised
VMF2, VMF3	Low	High	Sets 4.7 = 1 Sets 4.5 and 4.6 = 0 Sets 4.8 = 1	Advertise 100 Mbps only FD Advertised
		Low	Sets 4.7 = 1 Sets 4.5 and 4.6 = 0 Sets 4.8 = 0	Advertise 100 Mbps only FD Not Advertised
VMF2, VMF3	High	High	Sets 4.5 and 4.7 = 1 Sets 4.6 and 4.8 = 1	Advertise 10/100 Mbps FD Advertised
		Low	Sets 4.5 and 4.7 = 1 Sets 4.6 and 4.8 = 0	Advertise 10/100 Mbps FD Not Advertised

FUNCTIONAL DESCRIPTION

Introduction

The LXT970 Fast Ethernet Transceiver is a physical layer (PHY) device that supports 10 Mbps and 100 Mbps Ethernet networks. It provides all the functions necessary to build an IEEE 802.3 compliant solution. The LXT970 can directly drive a twisted-pair cable for up to 100 meters. The LXT970 also provides a pseudo-ECL interface for driving a 100BASE-FX fiber connection.

On power-up, the LXT970 can use auto-negotiation with parallel detection to automatically determine line operating conditions. If the PHY device on the other side of the link supports auto-negotiation, the LXT970 will auto-negotiate with it using Fast Link Pulse (FLP) Bursts. If the PHY partner does not support auto-negotiation, the LXT970 will automatically detect the presence of either link pulses (10 Mbps PHY) or Idle symbols (100 Mbps PHY) and set its operating speed accordingly. When the line speed selection is made via the parallel detection method, the duplex mode will be set to half. The user may later select full duplex operation by subsequent writes to the appropriate MDIO register. Line operation can also be set using the Hardware Control Interface.

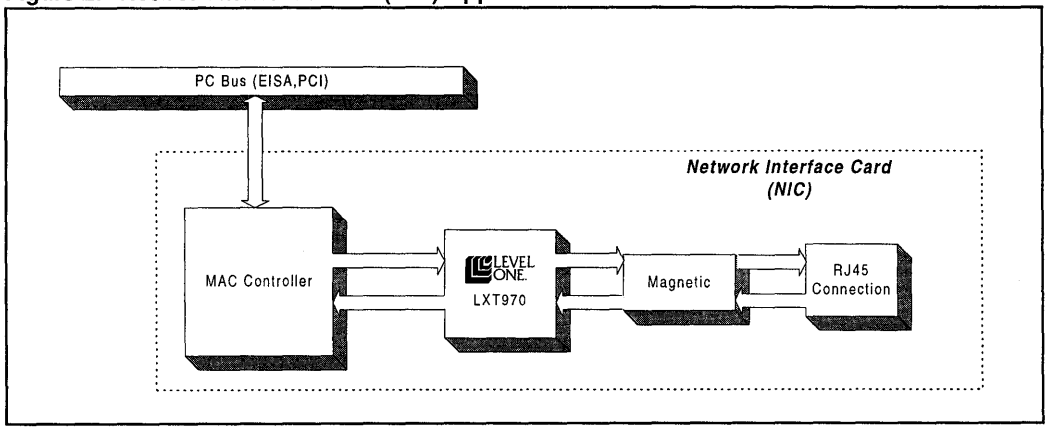
The LXT970 interfaces to a 10/100 MAC through the MII interface. The LXT970 performs all functions of the Physical Coding Sublayer (PCS) and Physical Media Attachment (PMA) sublayer as defined in the IEEE 802.3 100BASE-X specification. It also performs all functions of the Physical Media Dependent (PMD) sublayer for 100BASE-TX connections. The MII speed is automatically set once line operating conditions have been determined.

The LXT970 supports NIC, repeater and switch applications. It provides half- and full-duplex operation at 100Mbps and 10Mbps. See Figure 2 for a typical Network Interface Card (NIC).

NOTE

The LXT970 supports the 802.3 MDIO register set. Specific bits in the registers are referenced using an "X.Y" notation, where X is the register address (0-31) and Y is the bit number (0:15).

Figure 2: Network Interface Card (NIC) Application



Network Media / Protocol Support

The LXT970 supports both 10BASE-T and 100BASE-TX Ethernet over twisted-pair, or 100 Mbps Ethernet over fiber media (100BASE-FX). A standard Media Independent Interface (MII) is used for communication with the Media Access Controller (MAC).

10/100 Mbps Twisted Pair Interface

The twisted-pair interface consists of two differential pairs: the Twisted-Pair Input (TPIP/N) for receiving data, and the Twisted-Pair Output (TPOP/N) for transmitting data. This interface is used for both 10Mbps and 100Mbps operation. Auto-negotiation/parallel detection or manual control can be used to determine operation of the twisted-pair interface.

When operating at 100Mbps, MLT3 symbols are continuously transmitted and received. When not transmitting data, the LXT970 generates "IDLE" symbols.

During 10Mbps operation, Manchester encoded data is exchanged. During idle periods, the line is left in an idle voltage state.

In 100Mbps mode, the LXT970 is capable of driving a 100BASE-TX connection over 100Ω, Category 5, Unshielded Twisted Pair (UTP). A 10BASE-T connection can be supported using 100Ω, Category 3 or Category 5, UTP.

A transformer with 1:1 windings for transmit and receive, load resistors and bypass capacitors are all that is needed to complete this interface. The Transmit Reference (TREF) pin is used to supply +5V to the output transformer center tap. Using Level One's patented waveshaping technology, the transmitter pre-distorts the outgoing signal to reduce the need for external filters for EMI compliance.

When the twisted-pair interface is selected the FIBOP/N drivers are disabled. All data presented on the FIBIP/N input pins is ignored. In applications where the fiber interface is not used, the fiber I/O pins (FIBIP/N and FIBOP/N) may be left unconnected.

100 Mbps Fiber Interface

The LXT970 provides a pseudo-ECL interface that complies with the ANSI X3.166 specification. This interface is suitable for driving a fiber-optic coupler. This interface consists of four signals: FIBIP/N are the input pair and FIBOP/N are the output pair. The Fiber Port cannot be enabled via auto-negotiation, it must be enabled via the Hardware Control Interface or MDIO registers. When the fiber interface is selected, the TPOP/N drivers are disabled and the TREF pin is tri-stated. All data presented on the TPIP/N input pins is ignored. In applications where the twisted pair interface is not used, the twisted pair I/O pins (TPIP/N, TPOP/N and TREF) may be left unconnected.

MII Interface

The MII Interface is specified in IEEE 802.3. For this discussion, the MII is divided into two blocks; the MII Data Interface and the MII Management Interface.

MII Data Interface

This interface is used to pass data between the LXT970 and a Media Access Controller (MAC). The MII operates at either 2.5 MHz or 25 MHz, depending on the network link speed.

Ten signals are used to pass received data to the MAC: RXD<4:0>, RX_CLK, RX_DV, RX_ER, COL and CRS. Eight signals are used to transmit data from the MAC: TXD<4:0>, TX_CLK, TX_EN, and TX_ER.

Nibble (4B) vs. Symbol (5B) Mode

In nibble mode (19.4 = 0), 4-bit nibbles are passed across the MII data interface. RXD4 is set Low and TXD4 is ignored.

In symbol mode (19.4 = 1), 5-bit symbols are passed across the MII data interface. RXD4 and TXD4 are active.

DTE vs. Repeater Mode

In DTE mode (19.13 = 0), the LXT970 asserts RX_DV, RXD, RX_CLK and RX_ER as soon as it receives a packet from the network. In repeater mode (19.13 = 1), when TRSTE input is High, these output signals are tri-stated. This allows multiple LXT970's to share a single MII Interface and an external arbiter to determine which LXT970 should drive the MII Data Interface.

Loopback Operation

Loopback is determined by the operational state of the device and by bits 0.14 and 19.11. Bit 0.14 controls MII loopback test at both 10 and 100Mbps. Bit 19.11 controls normal twisted-pair loopback during 10Mbps, half-duplex operation. CRS is generated when the LXT970 is receiving data during all modes of operation.

- Full Duplex - During full duplex mode loopback and collision detection are always disabled. CRS is not generated on transmission.

- Repeater Mode - (bit 19.13 = 1) During repeater mode, loopback is disabled. CRS is not generated on transmit and collision detection is enabled.
- Half-Duplex/DTE Mode (10Mbps) - If 19.11 = 0 (default), data is looped back. If 19.11 = 1, data is not looped back. In both cases CRS is generated on transmit and collision detection is enabled.
- Half-Duplex/DTE Mode (100Mbps) - Data is not looped back. CRS is generated on transmit and collision detection is enabled.
- Loopback Test - Register bit 0.14 controls the MII loopback function. This capability is provided for diagnostics. Setting bit 0.14 = 1, causes the LXT970 to disconnect from the media interface and any data transmitted will be looped back to the receiver. No data will be sent or received from the media when this mode is enabled. When this diagnostic loopback is enabled, bit 0.7 can be used to test the operation of the COL pin.

MII Management Interface

The LXT970 supports the IEEE 802.3 MII Management Interface also known as the Management Data Input/Output (MDIO) Interface. This interface allows upper-layer devices to monitor and control the state of the LXT970. MDIO interface consists of a physical connection, a specific protocol which runs across the connection, and an internal set of addressable registers. The physical interface consists of a data line (MDIO) and clock line (MDC), a control line (MDDIS) and an optional interrupt line (MDINT). The LXT970 can signal an interrupt using the MDIO signal as shown in Figure 3. The user can also assign a separate pin for this function. If Bit 17.1 = 1, pin 2 (FDS/MDINT) will be used as an MDINT pin.

Operation of this interface is controlled by the MDDIS input pin. When MDDIS is High, the MDIO operates as a read-only interface. When MDDIS is Low, read and write are enabled. The timing for the MDIO Interface is shown in Table 40. Read and write operations are shown in Figures 4 and 5. The protocol allows one controller to communicate with multiple LXT970 devices; each LXT970 is assigned an address between 0 and 31.

The LXT970 supports twelve 16-bit MDIO registers. Registers 0-7 are required and their functions are specified by the IEEE 802.3 specification. Additional registers are included for expanded functionality. The MDIO Register set for the LXT970 is described in Tables 43 through 54. Specific bits in the registers are referenced using an "X.Y" notation, where X is the register number (0-31) and Y is the bit number (0-15).

Figure 3: MDIO Interrupt Signaling

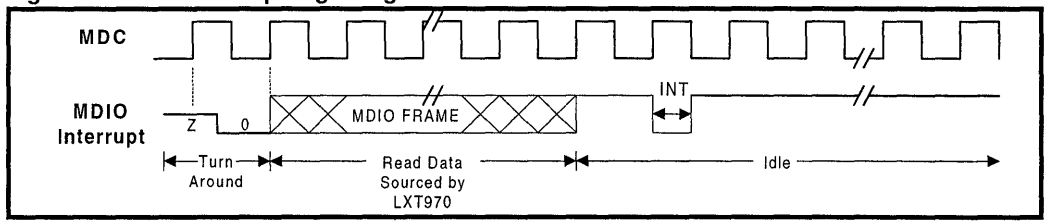


Figure 4: Management Interface - Read Frame Structure

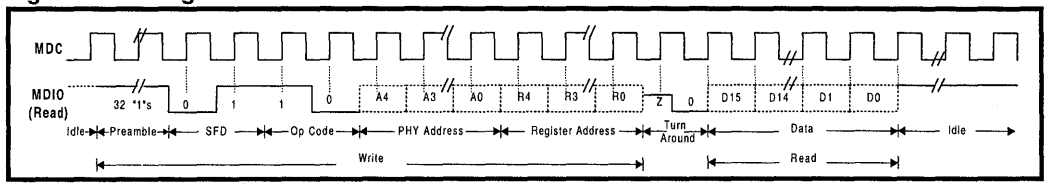
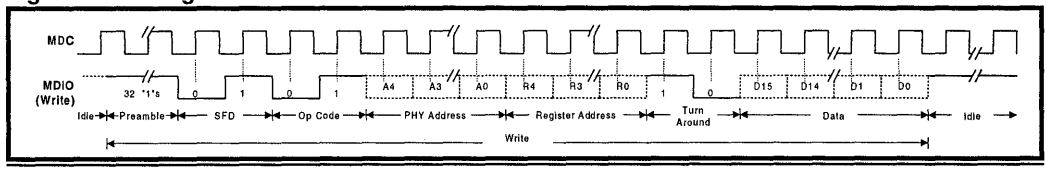


Figure 5: Management Interface - Write Frame Structure



Hardware Control Interface

The Hardware Control Interface consists of MF<4:0>, CFG <1:0> and FDE input pins. This interface is used to configure operating characteristics of the LXT970 and to determine the MDIO Address. When MDDIS is Low, the Hardware Control Interface provides initial values for the MDIO registers, and then passes control to the MDIO Interface.

When MDDIS is High, the Hardware Control Interface provides continuous control over the LXT970. Individual chip addressing allows multiple LXT970 devices to share the MII in either mode. Tables 10, 11 and 12 show how to set-up the desired operating configurations using the Hardware Control Interface.

Table 10: Configuring the LXT970 via Hardware Control

Desired Configuration	Pin Name	Input Value	MDIO Registers
Auto-Negotiation Enabled[1]	MF0	VMF2, VMF3	0.12 = 1
Auto-Negotiation Disabled[2]	MF0	VMF1, VMF4	0.12 = 0
Normal Operation (PHY Mode, Nibble Mode, Scrambler Enabled)	MF1 MF2 MF3	VMF1, VMF4	19.13 = 0 19.4 = 0 19.3 = 0
Repeater Mode	MF1	VMF2, VMF3	19.13 = 1
Symbol Mode	MF2	VMF2, VMF3	19.4 = 1
Scrambler Bypass Mode	MF3	VMF2, VMF3	19.3 = 1

1. Refer to Table 11 for Hardware Control Interface functions available when auto-negotiation is enabled.
2. Refer to Table 12 for Hardware Control Interface functions available when auto-negotiation is disabled.

Table 11: LXT970 Operating Configurations / Auto-Negotiation Enabled

Desired Configuration[1,2]	Pin Settings			MDIO Registers			
	MF4	CFG1	FDE	4.5	4.6	4.7	4.8
Advertise All	VMF1, VMF4	Low	Ignore	1	1	1	1
Advertise 100 HD	VMF2, VMF3	Low	Low	0	0	1	0
Advertise 100 HD/FD	VMF2, VMF3	Low	High	0	0	1	1
Advertise 10 HD	VMF1, VMF4	High	Low	1	0	0	0
Advertise 10 HD/FD	VMF1, VMF4	High	High	1	1	0	0
Advertise 10/100 HD	VMF2, VMF3	High	Low	1	0	1	0

1. Refer to Table 10 for basic configurations.
2. Refer to Table 12 for Hardware Control Interface functions available when auto-negotiation is disabled.

Table 12: LXT970 Operating Configurations / Auto-Negotiation Disabled

Desired Configuration[1,2]	Pin Name	Input Value	MDIO Registers
Force 100FX Operation	MF4	VMF2, VMF3	19.2 = 1
Force 100TX Operation	MF4	VMF1, VMF4	19.2 = 0
	CFG0	High	0.13 = 1
Force 10T Operation	MF4	VMF1, VMF4	19.2 = 0
	CFG0	Low	0.13 = 0
Force Full Duplex Operation	FDE	High	0.8 = 1
Disable 10T Link Test	CFG1	High	19.8 = 1
Enable 10T Link Test	CFG1	Low	19.8 = 0

1. Refer to Table 10 for basic configurations.
2. Refer to Table 11 for Hardware Control Interface functions available when auto-negotiation is enabled.

Initialization

At power-up or reset, the LXT970 performs the initialization as shown in Figure 6. When pin 15 (MDDIS) is High, the LXT970 enters Manual Control Mode. When MDDIS is Low, MDIO Control Mode is enabled. Mode control selection is provided via the MDDIS pin as shown in Table 13.

MDIO Control Mode

In the MDIO Control mode, the LXT970 uses the Hardware Control Interface to set up initial (default) values of the MDIO registers. Once initial values are set, bit control reverts to the MDIO interface.

Manual Control Mode

In the Manual Control Mode, LXT970 disables direct write operations to the MDIO registers on the MDIO interface. The Hardware Control Interface is continuously monitored and the MDIO registers are updated accordingly.

Table 13: Mode Control Settings

MDDIS Pin 15	RESET Pin 16	PWRDWN Pin 34	Mode
Low	High	Low	MDIO Control
High	High	Low	Manual Control
-	Low	Low	Reset
-	-	High	Power Down

Link Configuration

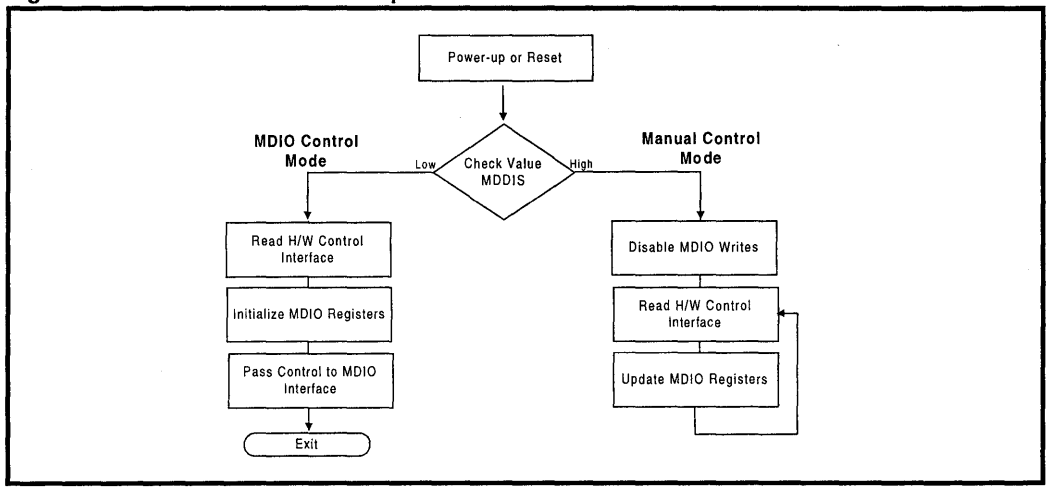
When the LXT970 is first powered on, reset, or encounters a link failure state, it must determine the line speed and operating conditions to use for the network link.

The LXT970 first checks the MDIO registers (initialized via the Hardware Control Interface or software) for operating instructions. Using these mechanisms, the user can command the LXT970 to do one of the following:

- Force 100FX (Fiber)
- Force twisted-pair link operation to:
  - 100TX, Full Duplex
  - 100TX, Half Duplex
  - 10BASE-T, Full Duplex
  - 10BASE-T, Half Duplex
- Allow auto-negotiation/parallel-detection.

In the first two cases, the LXT970 immediately begins operating the network interface as commanded. In the third case, the LXT970 begins the auto-negotiation/parallel-detection operation.

Figure 6: LXT970 Initialization Sequence



Auto-Negotiation

At power-up or reset, with auto-negotiation enabled, the LXT970 attempts to establish link operating conditions with its partner by sending FLP (Fast Link Pulse) bursts. By exchanging FLP bursts, the LXT970 and its link partner communicate their capabilities to each other. Each side finds the highest common capabilities that both sides can support and then begins operating in that mode.

Parallel Detection

In parallel with auto-negotiation, the LXT970 also checks for 10 Mbps Normal Link Pulses (NLP) or 100 Mbps Idle symbols. If either is detected, the device automatically configures to match the detected operating speed in half duplex mode. This ability allows the LXT970 to communicate with devices that do not support auto-negotiation.

Controlling Auto-Negotiation

When auto-negotiation is controlled by software, the following steps are recommended:

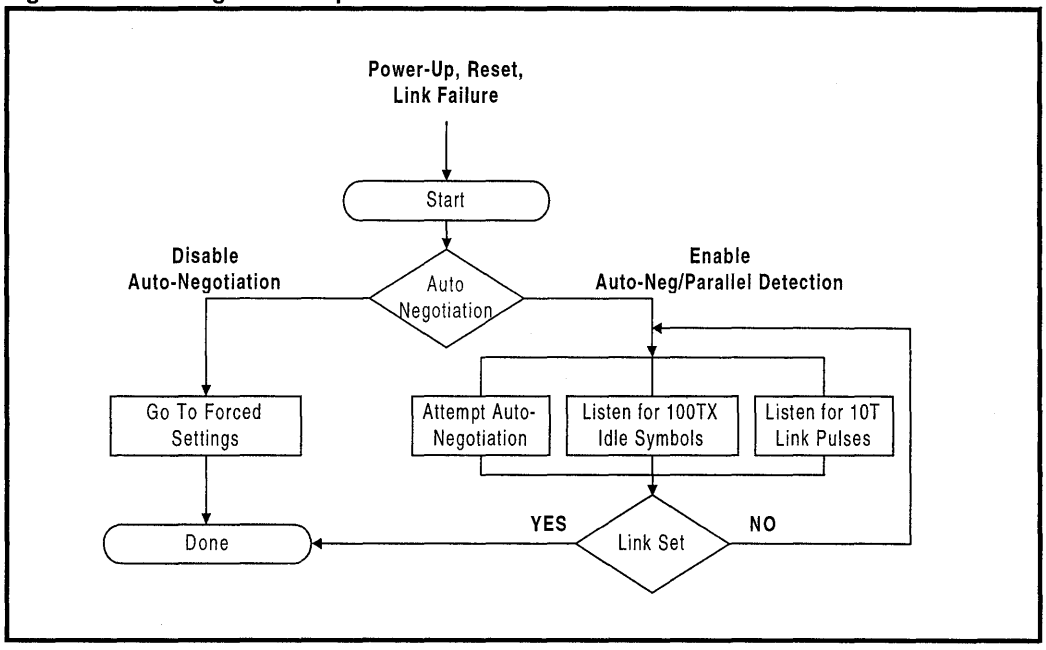
- After power-up, power down, or reset, the power down recovery time, as specified in Table 41, must be exhausted before proceeding.
- Set MDIO Register 4 advertisement capabilities before enabling auto-negotiation by setting MDIO bit 0.12 = 1

Monitoring Auto-Negotiation

When auto-negotiation is being monitored, the following apply:

- Bit 20.13 is set to 1 once the link is established
- Bits 20.12 and 20.11 can be used to determine the link operating conditions (speed and duplex)
- Operation can be forced by disabling auto-negotiation (bit 0.12 = 0) and setting bits 0.13, 0.8 and 19.2

Figure 7: Auto-Negotiation Operation



100 Mbps Operation

The MAC transmits data to the LXT970 over the MII. In 100BASE-TX mode, the LXT970 encodes and scrambles the data, then transmits it using MLT-3 signalling. The LXT970 descrambles and decodes MLT-3 data received from the network. In 100BASE-FX mode, the LXT970 transmits and receives data as NRZI signals.

When the MAC is not actively transmitting data, the LXT970 sends out Idle symbols on the line.

As shown in Figure 8, the MAC starts each transmission with a preamble pattern. When TX_EN is asserted, the LXT970 transmits a J/K symbol to the network (Start of Stream Delimiter or SSD). It then encodes and transmits the rest of the packet, including the balance of the preamble, the SFD (Start of Frame Delimiter), packet data, and CRC. Once the packet ends, the LXT970 transmits the T/R symbol (End of Stream Delimiter or ESD) and then returns to transmitting Idle symbols.

Normally, 4-bit wide nibble data is transmitted across the MII interface and RXD4/TXD4 are ignored. The encoder translates the 4-bit nibbles into 5-bit symbols which are sent over the 100BASE-X connection. In Symbol Mode, a fifth bit is provided (RXD4/TXD4) to allow a 5-bit symbol to be sent across the MII interface.

Figure 9 shows the data conversion flow from nibbles to symbols. Table 14 shows 4B/5B symbol coding. Note that some symbols are invalid.

Figure 8: 100BASE-TX Frame Structure

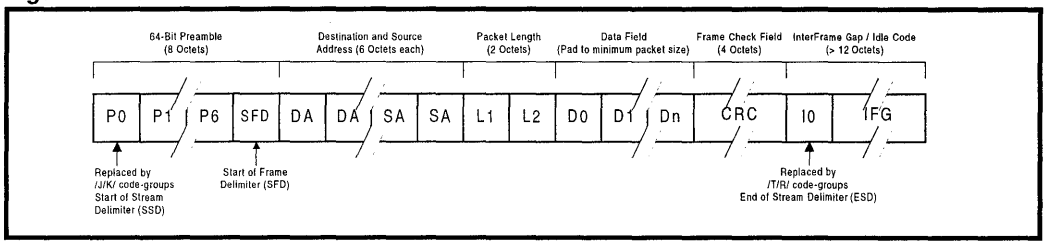


Figure 9: 100BASE-TX Data Flow

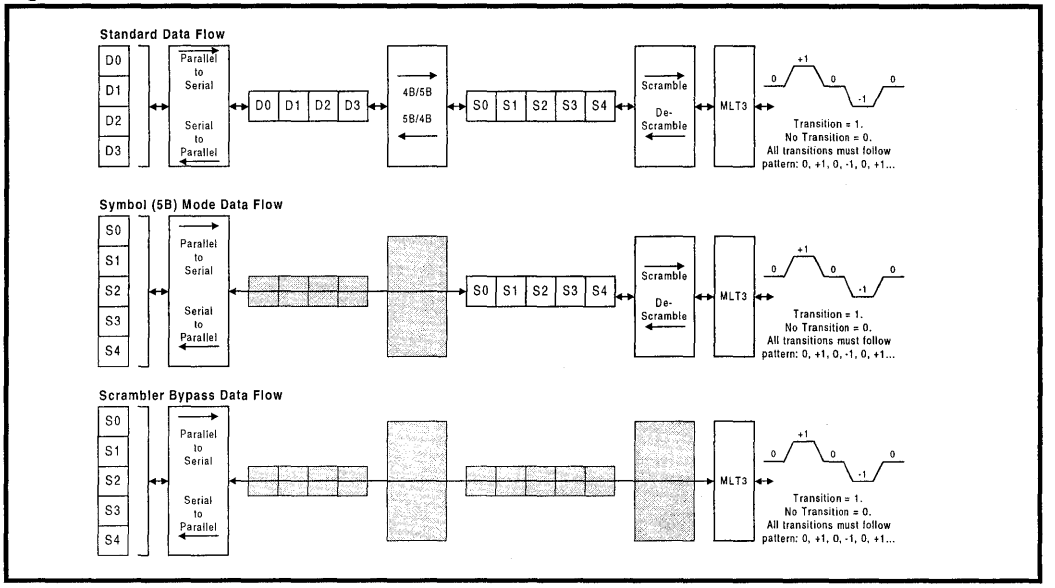


Table 14: 4B/5B Coding

Code Type	4B Code 3 2 1 0	Name	5B Symbol 4 3 2 1 0	Interpretation
DATA	0 0 0 0	0	1 1 1 1 0	Data 0
	0 0 0 1	1	0 1 0 0 1	Data 1
	0 0 1 0	2	1 0 1 0 0	Data 2
	0 0 1 1	3	1 0 1 0 1	Data 3
	0 1 0 0	4	0 1 0 1 0	Data 4
	0 1 0 1	5	0 1 0 1 1	Data 5
	0 1 1 0	6	0 1 1 1 0	Data 6
	0 1 1 1	7	0 1 1 1 1	Data 7
	1 0 0 0	8	1 0 0 1 0	Data 8
	1 0 0 1	9	1 0 0 1 1	Data 9
	1 0 1 0	A	1 0 1 1 0	Data A
	1 0 1 1	B	1 0 1 1 1	Data B
	1 1 0 0	C	1 1 0 1 0	Data C
	1 1 0 1	D	1 1 0 1 1	Data D
	1 1 1 0	E	1 1 1 0 0	Data E
	1 1 1 1	F	1 1 1 0 1	Data F
IDLE	undefined	I [1]	1 1 1 1 1	Idle. Used as inter-stream fill code
CONTROL	0 1 0 1	J [2]	1 1 0 0 0	Start-of-Stream Delimiter (SSD), part 1 of 2
	0 1 0 1	K [2]	1 0 0 0 1	Start-of-Stream Delimiter (SSD), part 2 of 2
	undefined	T [3]	0 1 1 0 1	End-of-Stream Delimiter (SSD), part 1 of 2
	undefined	R [3]	0 0 1 1 1	End-of-Stream Delimiter (SSD), part 2 of 2
INVALID	undefined	H [4]	0 0 1 0 0	Transmit Error. Used to force signaling errors
	undefined	Invalid	0 0 0 0 0	Invalid
	undefined	Invalid	0 0 0 0 1	Invalid
	undefined	Invalid	0 0 0 1 0	Invalid
	undefined	Invalid	0 0 0 1 1	Invalid
	undefined	Invalid	0 0 1 0 1	Invalid
	undefined	Invalid	0 0 1 1 0	Invalid
	undefined	Invalid	0 1 0 0 0	Invalid
	undefined	Invalid	0 1 1 0 0	Invalid
	undefined	Invalid	1 0 0 0 0	Invalid
	undefined	Invalid	1 1 0 0 1	Invalid

1. The /I/ (Idle) code-group is sent continuously between frames.
2. The /J/ and /K/ (SSD) code-groups are always sent in pairs; /K/ follows /J/.
3. The /T/ and /R/ (ESD) code-groups are always sent in pairs; /R/ follows /T/.
4. An /H/ (Error) code-group is used to signal an error condition.

5B Symbol Mode

In Symbol Mode, raw 5-bit symbol data is passed directly across the MII interface and the encoder is bypassed. Symbol Mode is selected by setting bit 19.4 = 1 or by setting input pin MF2 = VMF2 or VMF3.

This mode reduces device latency for use in repeater applications. See Table 31 and 32 for timing parameters.

Scrambler Seeding

Once the transmit data (or Idle symbols) are properly encoded, they are scrambled to further reduce EMI and to spread the power spectrum using an 11-bit scrambler seed. Ten seed bits are determined by MF<4:0> inputs and LED outputs, and one bit is randomly determined.

Scrambler Bypass

The scrambler/descrambler can be bypassed by either setting bit 19.3 = 1 or setting input pin MF3 to VMF2/VMF3. The scrambler is automatically bypassed when the fiber port is enabled. Symbol Mode (5B) must also be enabled for the LXT970 to work properly while in Scrambler Bypass Mode. Scrambler Bypass is provided for diagnostic and test support.

Link Failure

Link failure is declared when an excessive number (250 out of 1000) of invalid symbols are received. The LXT970 reports link failure via the MII status bits (1.2, 18.15 and 20.13) and interrupt functions. If auto-negotiation is enabled, link failure causes the LXT970 to re-negotiate.

Link Failure Override

The LXT970 will normally transmit 100Mbps data packets only if it detects the link is up, and transmits only Idle symbols or FLP bursts if the link is not up. Setting bit 19.14 = 1 overrides this function, allowing the LXT970 to transmit data packets even when the link is down. This feature is provided as a diagnostic tool. Note that auto-negotiation must be disabled to transmit data packets in the absence of link. If auto-negotiation is enabled, the LXT970 will automatically begin transmitting FLP bursts if the link goes down.

Baseline Wander Correction

The LXT970 provides a baseline wander correction function which makes the device robust under all network operating conditions. The MLT3 coding scheme used in 100BASE-TX is by definition "unbalanced". This means that the DC average value of the signal voltage can "wander" significantly over short time intervals (tenths of seconds). This wander can cause receiver errors, particularly at long line lengths (100 meters). The exact characteristics of the wander are completely data dependent. "Killer Packets" have been created that exhibit worst case baseline wander characteristics. The LXT970 baseline wander correction characteristics allow the LXT970 to recover error-free data, even at long line lengths.

FX Operation

To enable 100BASE-FX operation, auto-negotiation must be disabled and FX selected.

- To disable auto-negotiation, set 0.12 = 0, or set MF0 = VMF1 or VMF4.
- To select FX, set 19.2 = 1, or set MF4 = VMF2 or VMF3.

In FX mode, the following conditions apply:

- CFG0 / 0.13 still controls speed and must be set to 1 for 100 Mbps operation.
- Scrambler is automatically disabled.
- 5-bit symbol mode may be selected by setting 19.4 = 1, or setting MF2 = VMF2 or VMF3.
- Duplex operation is controlled by pin FDE or by bit 0.8.

Data Errors

Figure 10 shows normal reception. When the LXT970 receives invalid symbols from the line, it asserts RX_ER, as shown in Figure 11.

Collision Indication

Figure 12 shows normal transmission. The LXT970 detects a collision if transmit and receive are active at the same time. As shown in Figure 13, upon detection of a collision, the COL output is asserted and remains asserted for the duration of the collision.

Figure 10: 100BASE-TX Reception with No Errors

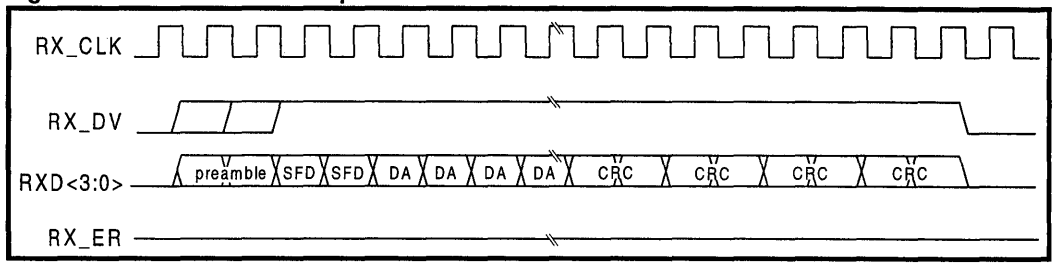


Figure 11: 100BASE-TX Reception with Invalid Symbol

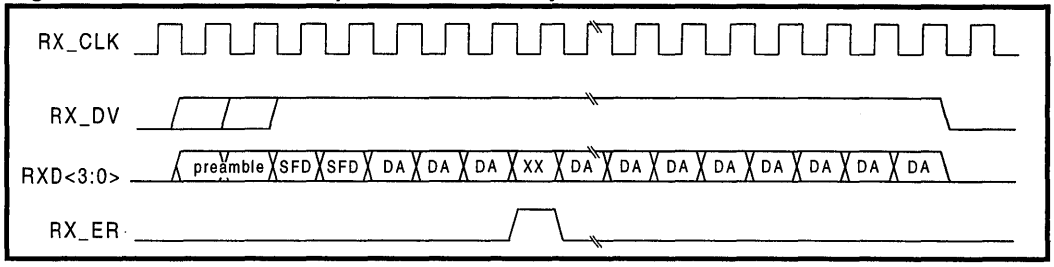


Figure 12: 100BASE-TX Transmission with No Errors

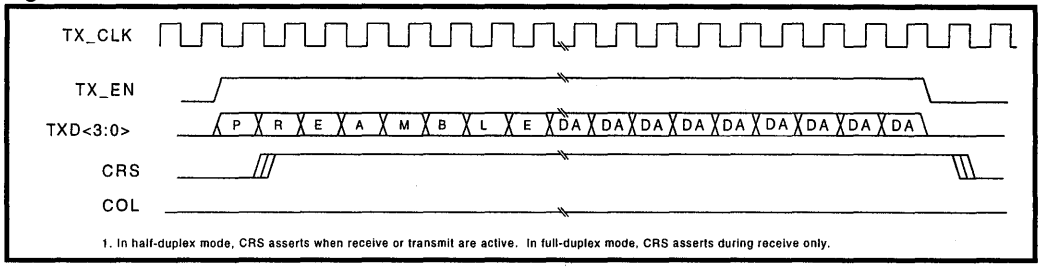
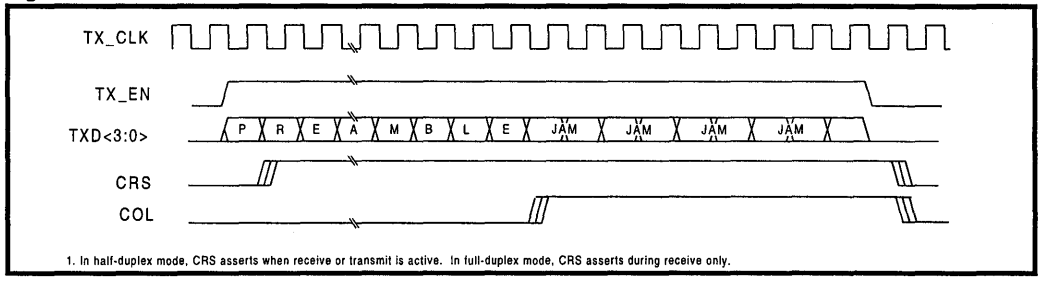


Figure 13: 100BASE-TX Transmission with Collision



10 Mbps Operation

The LXT970 will operate as a standard 10 Mbps transceiver. Data transmitted by the MAC as 4-bit nibbles is serialized, Manchester-encoded, and transmitted on the TPOP/N outputs. Received data is decoded, de-serialized into 4-bit nibbles and passed to the MAC across the MII. The LXT970 supports all the standard 10Mbps functions.

Link Test

In 10 Mbps mode, the LXT970 always transmits link pulses. If the Link Test Function is enabled, it monitors the connection for link pulses. Once it detects 2 to 7 link pulses, data transmission will be enabled and will remain enabled as long as the link pulses or data transmission continues. If the link pulses stop, the data transmission will be disabled.

If the Link Test function is disabled, the LXT970 will transmit to the connection regardless of detected link pulses. The Link Test function can be disabled by setting Bit 19.8 = 1 or by setting MF0 to disable auto-negotiation and setting CFG1 input High.

SQE (Heartbeat)

By default, the SQE (heartbeat) function is disabled on the LXT970. To enable this function, set bit 19.10 = 1. When this function is enabled, the LXT970 will assert its COL output for 5-15 BT after each packet. See Figure 24 for SQE timing parameters.

Jabber

If the MAC begins a transmission that exceeds the jabber timer, the LXT970 disables the transmit and loopback functions and enables the COL pin. The LXT970 automatically exits jabber mode after 250-750ms. This function can be disabled by setting Bit 19.9 = 1. See Figure 25 for Jabber timing parameters.

Polarity Correction

The LXT970 automatically detects and corrects for the condition where the receive signal (TPIP/N) is inverted. Reversed polarity is detected if 8 inverted link pulses, or 4 inverted end-of-frame markers, are received consecutively. If link pulses or data are not received for 96-128 ms, the polarity state is reset to a non-inverted state.

Link Failure

Link failure occurs if Link Test is enabled and link pulses stop being received. If this condition occurs, the LXT970 returns to the auto-negotiation phase if auto-negotiation is enabled.

Operating Requirements

Power Requirements

The LXT970 requires four +5V supply inputs (VCCA, VCCD, VCCR and VCCT). These inputs may be supplied from a single source although decoupling is required to each respective ground. As a matter of good practice, these supplies should be as clean as possible. Typical filtering and decoupling are shown in the Application Information section, Figure 15. An additional supply is required for the MII (VCCIO). The MII supply may be either +5V or +3.3V. Power for the MII should be supplied from the same power source used for the controller on the other side of the MII interface.

Low Voltage Fault Detect

The LXT970 has a low voltage fault detection function that prevents transmission of invalid symbols when VCC goes below normal operating levels. This function disables the transmit outputs when a low voltage fault on Vcc occurs. If this condition happens, the LXT970 sets 20.2 = 1. Operation is automatically restored when Vcc returns to normal. Table 24 indicates voltage levels used to detect and clear the low voltage fault condition.

Power Down Mode

The LXT970 goes into Power Down Mode when PWRDWN is asserted. In this mode, all functions are disabled except the MDIO. The power supply current is significantly reduced. Refer to Table 19 for power down specifications. This mode can be used for energy-efficient applications or for redundant applications where there are two devices and one is left as a stand-by. When the LXT970 is returned to normal operation, configuration settings of the MDIO registers are maintained.

Clock Requirements

The LXT970 requires a constant clock that must be enabled at all times. Depending on the mode of operation, the clock may be supplied at the crystal oscillator pins (XI, XO), or at the Transmit Clock pin (TX_CLK). There are two clock modes, master clock mode and slave clock mode. See Table 23 for input clock requirements.

Master Clock Mode

The Master Clock mode is recommended in most Network Interface Cards (NICs) and switch applications. In the Master Clock mode the LXT970 is the master clock source for data transmission, and requires a 25 MHz reference signal at XI.

In master clock mode, TX_CLK is an output and the LXT970 automatically sets the speed of TX_CLK to match line conditions. If the line is operating at 100Mbps, TX_CLK will be set to 25MHz. If the line is operating at 10Mpbs, TX_CLK will be set to 2.5MHz.

External Crystal

An external 25 MHz crystal connected across XI and XO is recommended to supply the LXT970 internal clock reference. A crystal is typically used in NIC applications.

External Clock

An external 25 MHz clock source, rather than a crystal, is frequently used in switch applications. When a clock is supplied to XI, XO is left open.

TX Clock Advance Mode

When operating in Master Clock mode under MDIO Control, the user can advance the transmit clock relative to TXD<4:0> and TX_ER. This option can be used to compensate for propagation delays in applications with long MII cables. When TX_CLK Advance is selected, the LXT970 clocks TXD data in on the falling edge of TX_CLK, instead of the rising edge. This mode provides an increase in timing margins of TXD, relative to TX_CLK. TX_CLK Advance is enabled when bit 19.5 = 1.

Slave Clock Mode

The Slave Clock mode is typically used for repeater applications, where the LXT970 is not the master clock source for data transmissions.

In slave clock mode, the application circuit must drive TX_CLK in accordance with the line conditions. A frequency of 25MHz will support a line rate of 100Mbps only. A clock frequency of 2.5MHz will only support a line rate of 10Mbps. Either speed can be used during auto-negotiation. In Slave Clock mode XI is connected to ground and XO is left open.

APPLICATION INFORMATION

Magnetics Information

The LXT970 requires a 1:1 ratio for both the receive and the transmit transformers. Refer to Table 16 for transformer requirements. Transformers meeting these requirements are available from various manufacturers. Designers should test and validate all magnetics before using them in production.

Crystal Information

Refer to Table 17 for crystal requirements. Crystals are available from various manufacturers. Designers should test and validate all crystals before committing to a specific component.

Component Manufacturers.

Based on limited evaluations, Table 15 provides a list of suitable components and manufacturers.

Table 15: Component Manufacturers

Component	Manufacturer	Part Number
Magnetics	Halo	TG22-3506ND
		TD22-3506G1
		TG22-S010ND
		TG22-S012ND
	Nanopulse	NPI 6120-30
		NPI 6120-37
		NPI 6170-30
		NPI 6181-37
	Pulse	PE-68517
		PE-68515
	Valor	ST6114
		ST6118
Crystals	CTS	CTX093
	Epson America	SE2539CT

Table 16: Magnetics Requirements

Parameter	Min	Nom	Max	Units	Test Condition
Turns Ratio	–	1:1	–	–	
Insertion Loss	0.0	–	0.6	dB	
Primary Inductance	350	–	–	µH	
Transformer Isolation	–	2	–	kV	
Differential to common mode rejection	40	–	–	dB	.1 to 60 MHz
	35	–	–	dB	60 to 100 MHz
Return Loss	17	–	–	dB	.1 to 60 MHz
	15	–	–	dB	60 to 100 MHz
Rise Time	2.0	–	3.5	ns	10% to 90%

Table 17: Crystal Requirements

Parameter	Min	Nom	Max	Units	Test Condition
Frequency	–	25.0	–	MHz	
Frequency Stability	–	–	±100	ppm	-40 - 85°C

1. See Table 23 (Clock Characteristics) for additional device specifications.

Layout Requirements

The Twisted Pair Interface

The layout of the twisted-pair ports is critical in complex high-speed designs. Careful planning during the schematic and layout stages of the design will minimize these problems.

General Twisted-Pair Interface Layout Considerations

- The transformer isolation voltage should be rated at 2kV to protect the circuitry from static voltages across the connectors and cables.
- Place the transformer as close as possible to the connector.
- The traces running from the transformer to the connector should run in close pairs directly to the connector.
- Be careful not to cross the transmit and receive pairs.
- Vias should be avoided as much as possible.

Ground Plane Layout Considerations

Ground plane layout depends on the availability and quality of chassis ground. If a solid chassis ground is not available, there should be no power or ground planes in the area between the LXT970, the transformers and the connectors. High frequency noise on these planes causes interference on the data signals and induces EMI emissions. The data signals should be the only traces in this area, except for the termination of unused pairs or LEDs.

If a solid and quiet chassis ground is available that is well-decoupled from the active power and ground planes, it can be routed under the twisted pair signal traces to reduce EMI emissions. Position chassis ground at the edge of the board, encircling the PCB. Separate chassis ground from the digital and analog ground planes with an isolating moat and connect them through inductors. Keep chassis ground away from all active signals. If required, the RJ45 connector and any unused pins can be tied to chassis ground through a resistor divider network and a 2kV bypass capacitor.

The RBIAS Pin

The RBIAS pin sets the levels for the LXT970 output drivers. Any emissions or common mode noise entering the device here could be measured on the twisted pair output signals.

The LXT970 requires a 22kΩ, 1% resistor directly connected between the RBIAS pin and ground. This resistor should be as close to the device as possible and the traces should be as short as possible. Keep all high speed signals away from the RBIAS pin. The ground traces from adjacent pin GNDA should come directly off of the device to enclose the resistor and pin forming a shielded area between the RBIAS connection and the switching signals on the PCB.

Power Supply Decoupling

Ferrite Beads

Ferrite beads are recommended for decoupling the analog and digital supplies. The ferrite bead used should have an impedance of at least 100Ω at 100MHz. A suitable bead is the Panasonic surface mount bead, part number EXCCL4532U, or equivalent. For all applications,

- GNDT should be connected directly to GNDA.
- VCCT and VCCA should be connected and isolated from VCCD by a ferrite bead.
- For long line length performance (>120 meters), beads may be installed between VCCT and VCCR and between GNDT and GNDR. These beads are not required for applications <120 meters.
- Depending on the application, a ferrite bead may be required between GNDT/GNDA and GNDD. See explanation below.

For applications where the digital ground plane is noisy, a ferrite bead between GNDT/GNDA and GNDD may be required to prevent noise interference. If the digital ground plane is quiet, this ground bead may not be required.

Bypass Caps

Bypass caps are required between each supply and its associated ground return (VCCA/GNDA, VCCR/GNDR, VCCT/GNDT, VCCD/GNDD and VCCIO/GNDIO). The recommended cap is 0.1µF or .01µF, as required by the design layout.

10µF tantalum caps are recommended between VCCA and GNDA and between VCCD and GNDD on both sides of the ferrite beads.

For long line applications, when ferrite beads are used between the transmit and receive supplies and grounds, a tantalum cap is required on the device side of the ferrite bead between GNDR and VCCR.

If a crystal is used, it should be bypassed to GNDD.

The Fiber Interface

In fiber-only applications, reference the fiber ports to the analog power and ground planes (VCCA, GNDA, VCCT, GNDT, VCCR, GNDR). In a combination fiber and twisted-pair application, reference the fiber ports to the digital power and ground planes (VCCD, GNDD). In applications where the fiber interface is not used, the fiber I/O pins (FIBIP/N and FIBOP/N) may be left unconnected

Typical Application

Figure 15 is a typical application of the LXT970. The diagram groups similar pins; it does not portray the actual chip pinout. The Media Independent Interface pins are at the upper left. Hardware Control Interface pins are center left. The line interface pins for twisted-pair and fiber are shown on the top and bottom right respectively.

The VCCD and VCCIO pins are at the bottom of the diagram. VCCT, VCCR and VCCA are at the center right. All VCC pins (except VCCIO) use a single power supply. VCCIO may be powered by a 3.3V supply, and may be separately connected.

Voltage Divider For MF Inputs

The LXT970 requires an external voltage divider to provide optional (V_{MF2} and V_{MF3}) multi-level inputs to the Multi-Function (MF) pins. These voltage levels are designated as V_{MF1} - V_{MF4}. Figure 14 shows a voltage divider with three 1kΩ resistors configured in series between VCC and Ground.

Figure 14: Voltage Divider

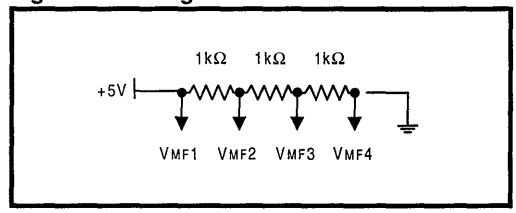


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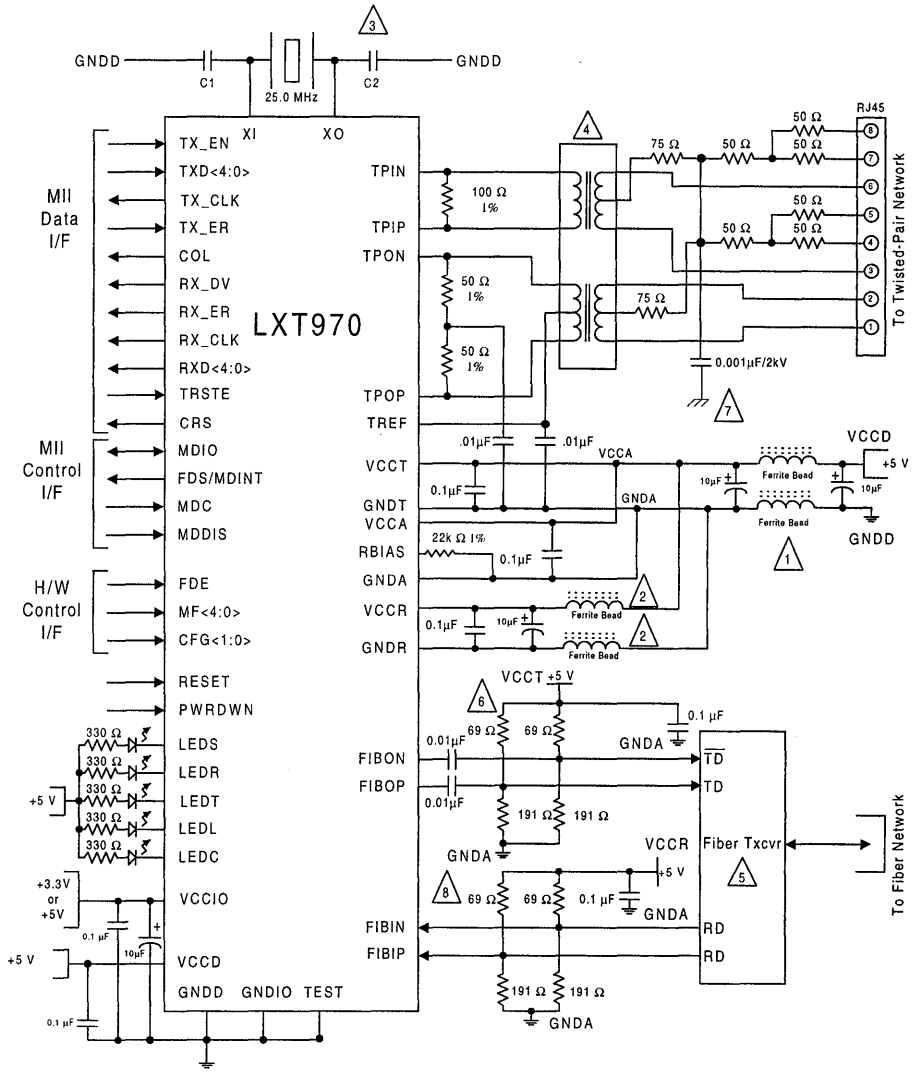
Figure 15: Typical Network Interface Card (NIC) Application



1. This ferrite bead is suggested for applications with noisy ground planes.
2. These beads may improve long line length performance (>120 meters), but not required for applications <120 meters.
3. Refer to Tables 15 and 17 for crystals.
4. Refer to Tables 15 and 16 for magnetics.
5. Refer to fiber transceiver manufacturers recommendations for termination circuitry. Suitable fiber transceivers include the HFBR-5103 and HFBR-5105.
6. Suggested supply layout for fiber-only applications. In combination twisted-pair and fiber applications, use VCCD/GNDD.
7. Bypassing to chassis ground (if available) provides additional EMI shielding.
8. If the Fiber Interface is not used, FIBIN, FIBIP, FIBON and FIBOP may be left unconnected.

TEST SPECIFICATIONS

Note

Minimum and maximum values in Tables 18 through 41 and Figures 16 through 30 represent the performance specifications of the LXT970 and are guaranteed by test except, where noted, by design.

Table 18: Absolute Maximum Ratings

Parameter	Sym	Min	Max	Units
Supply Voltage	VCC	-0.3	6	V
Operating Temperature	TOP	-15	+85	°C
Storage Temperature	TST	-65	+150	°C

CAUTION

Exceeding these values may cause permanent damage.
Functional operation under these conditions is not implied.
Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 19: Operating Conditions

Parameter		Sym	Min	Typ[1]	Max	Units	Test Conditions
Recommended Supply Voltage[2]	Except MII Supply	VCC	4.75	5.0	5.25	V	
	MII Supply	VCCIO	3.125	–	5.25	V	
Recommended Operating Temperature		TOP	0	–	70	°C	
VCC Current (+5V Only)	100BASE-TX	ICC	–	170	–	mA	
	100BASE-FX	ICC	–	80	–	mA	
	10BASE-T	ICC	–	185	–	mA	
	Power Down Mode	ICC	–	9	–	mA	
	Auto-Negotiation	ICC	–	240	270	mA	

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Voltages with respect to ground unless otherwise specified.

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Table 20: Digital I/O Characteristics[1] - (Over Recommended Range)

Parameter	Symbol	Min	Typ[2]	Max	Units	Test Conditions
Input Low voltage[3]	V_{IL}	–	–	0.8	V	
Input High voltage[3]	V_{IH}	2.0	–	–	V	
Input Current	I_I	-10	–	10	µA	$0.0 < V_I < V_{CC}$
Output Low voltage	V_{OL}	–	–	0.4	V	I_{OL} = 4 mA
Output High voltage	V_{OH}	2.4	–	–	V	I_{OH} = -4 mA

1. Applies to all pins except MII and MF<4:0> pins. Refer to Table 21 for MF pin I/O Characteristics and Table 22 for MII I/O Characteristics.
2. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
3. Does not apply to XI or TX_CLK pins. Refer to Table 23 for clock input levels.

Table 21: Digital I/O Characteristics - MultiFunction Pins MF<4:0> (Over Recommended Range)

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Input Voltage Level 1	V_{MF1}	V_{CC} - 0.5	–	–	V	
Input Voltage Level 2	V_{MF2}	(V_{CC}/2) + 0.5	–	V_{CC} - 1.2	V	
Input Voltage Level 3	V_{MF3}	1.2	–	V_{CC}/2 - 0.5	V	
Input Voltage Level 4	V_{MF4}	–	–	0.5	V	

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 22: Digital I/O Characteristics - MII Pins (Over Recommended Range)

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Input Low voltage	V_{IL}	–	–	.8	V	
Input High voltage	V_{IH}	2.0	–	–	V	
Input Current	I_I	-10	–	10	µA	$0.0 < V_I < V_{CC}$
Output Low voltage	V_{OL}	–	–	0.4	V	I_{OL} = 4 mA
Output High voltage	V_{OH}	2.2	–	–	V	I_{OH} = -4 mA, V_{CCIO} = 3.3V
	V_{OH}	2.4	–	–	V	I_{OH} = -4 mA, V_{CCIO} = 5.0V
Driver Output Resistance (Line driver output enabled)	R_O[1]	6.0	–	25.0	Ω	V_{CCIO} = 3.3V
	R_O[1]	6.0	–	25.0	Ω	V_{CCIO} = 5.0V

1. Parameter is guaranteed by design; not subject to production testing.

Table 23: Required Clock Characteristics

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Master Clock Mode - External XI Clock Input						
Input Low Voltage[2]	VIL	–	–	1.0	V	
Input High Voltage[2]	VIH	3.2	–	–	V	
Input Clock Frequency Tolerance[2]	Δf	–	–	± 100	ppm	Clock frequency is 25 MHz or 2.5 MHz
Input Clock Duty Cycle[2]	TDC	40	–	60	%	
Input Capacitance (XI and XO)	CIN	–	3.0	–	pF	
Slave Clock Mode - External TX_CLK Input						
Input Low Voltage	VIL	–	–	.8	V	
Input High Voltage	VIH	2.0	–	–	V	
Input Clock Frequency Tolerance[2]	Δf	–	–	± 100	ppm	Clock frequency is 25 MHz or 2.5 MHz
Input Clock Duty Cycle[2]	TDC	35	–	65	%	

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Parameter is guaranteed by design; not subject to production testing.

Table 24: Low Voltage Fault Detect Characteristics

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Detect Fault Threshold	VLT	3.4	–	4.0	V	–
Clear Fault Threshold	VLH	4.1	–	4.7	V	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 25: 10BASE-T Link Integrity Timing Characteristics (Over Recommended Range)

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Time Link Loss Receive	TLL	50	64	150	ms	–
Link Pulse	TLP	2	4	7	Link Pulses	–
Link Min Receive Timer	TLR MIN	2	4	7	ms	–
Link Max Receive Timer	TLR MAX	50	64	150	ms	–
Link Transmit Period	TLT	8	10	24	ms	–
Link Pulse Width	TLPW	–	100	–	ns	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 26: 100BASE-TX Transceiver Characteristics (Over Recommended Range)

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Peak differential output voltage	VOP	0.95	–	1.05	V	Note 2
Signal amplitude symmetry	Vss	98	–	102	%	Note 2
Signal rise/fall time	TRF	3.0	–	5.0	ns	Note 2
Rise/fall time symmetry	TRFS	–	–	0.5	ns	Note 2
Duty cycle distortion	DCD	–	–	± 0.5	ns	Offset from 16ns pulse width at 50% of pulse peak
Overshoot/Undershoot	VOS	–	–	5	%	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Measured at the line side of the specified transformer, line replaced by 100Ω (±1%) resistor.

Table 27: 100BASE-FX Transceiver Characteristics (Over Recommended Range)

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Transmitter						
Peak Differential Output Voltage (single ended)	VOP	0.6	–	1.0	V	–
Signal rise/fall time	TRF	–	–	1.6	ns	10 <–> 90% 2.0 pF load
Jitter (measured differentially)	–	–	–	1.3	ns	–
Receiver						
Peak Differential Input Voltage	VIP	0.55	–	1.5	V	–
Common Mode Input Range	VCMIR	2.25	–	VCC - 0.5	V	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 28: 10BASE-T Transceiver Characteristics (Over Recommended Range)

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Transmitter						
Peak Differential Output Voltage	VOP	2.2	2.5	2.8	V	With specified transformer, line replaced by 100Ω (±1%) resistor
Transmit timing jitter added by the MAU and PLS sections[2,3]	–	0	2	11	ns	After line model specified by IEEE 802.3 for 10BASE-T MAU
Receiver						
Receive Input Impedance[2]	ZIN	–	3.6	–	kΩ	Between TPIP/TPIN
Differential Squelch Threshold	VDS	300	420	585	mV	5 MHz square wave input

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Parameter is guaranteed by design; not subject to production testing.
3. IEEE 802.3 specifies maximum jitter additions at 1.5ns for the AUI cable, 0.5ns from the encoder, and 3.5ns from the MAU.

Figure 16: MII - 100BASE-TX Receive Timing / 4B Mode

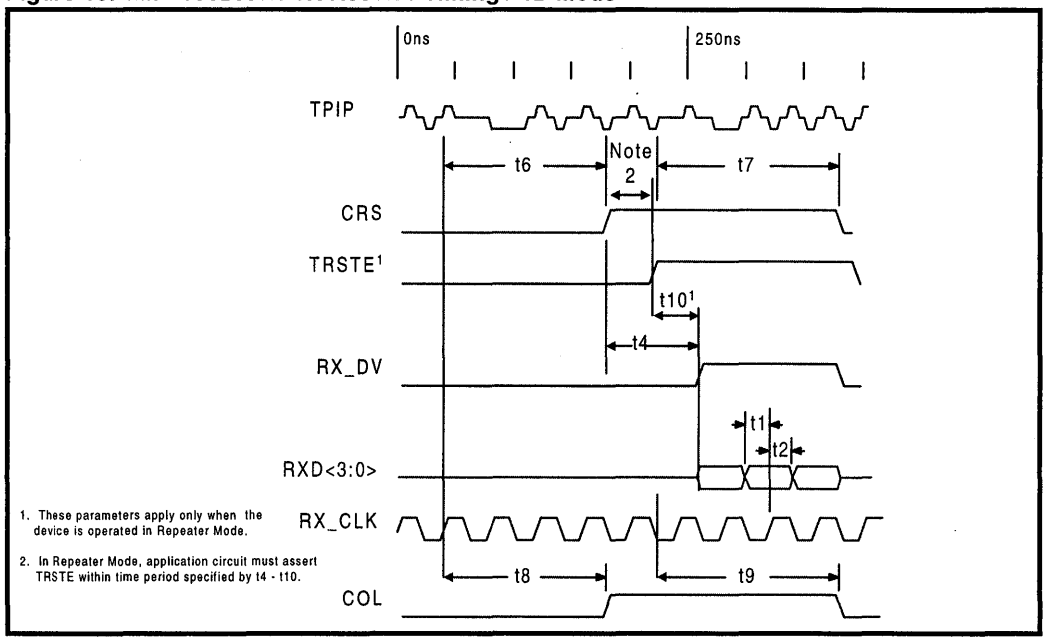

Table 29: MII - 100BASE-TX Receive Timing Parameters / 4B Mode (Over Recommended Range)

Parameter	Sym	Min	Typ[1]	Max	Units
RXD, RX_DV, RX_ER Setup to RX_CLK High	t1	10	–	–	ns
RXD, RX_DV, RX_ER Hold from RX_CLK High	t2	5	–	–	ns
CRS asserted to RXD<3:0>, RX_DV asserted	t4	–	8	–	BT
Receive start of "J" to CRS asserted	t6	0	15 - 19	20	BT
Receive start of "T" to CRS de-asserted	t7	13	23 - 27	28	BT
Receive start of "J" to COL asserted	t8	0	15 - 19	20	BT
Receive start of "T" to COL de-asserted	t9	13	23 - 27	28	BT
TRSTE asserted to RX_DV, RXD<3:0> driven[2]	t10	–	20	–	ns

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. These parameters apply only when the device is operated in Repeater Mode.

Figure 17: MII - 100BASE-TX Transmit Timing / 4B Mode

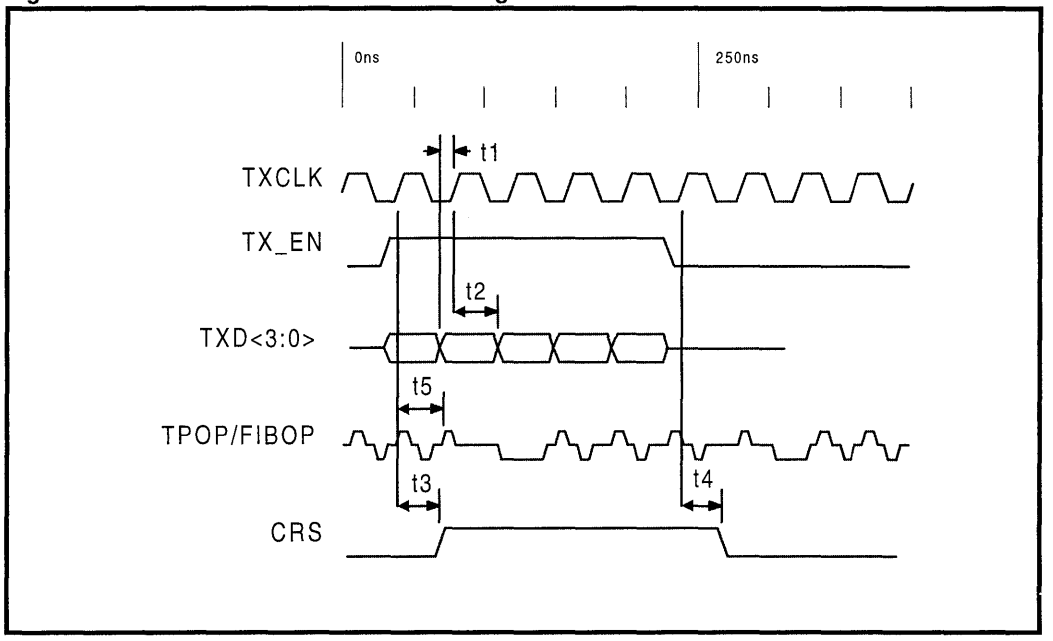

Table 30: MII - 100BASE-TX Transmit Timing Parameters / 4B Mode (Over Recommended Range)

Parameter	Sym	Min	Typ[1]	Max	Units
TXD<3:0>, TX_EN, TX_ER Setup to TX_CLK High	t1	10	–	–	ns
TXD<3:0>, TX_EN, TX_ER Hold from TX_CLK High	t2	5	–	–	ns
TX_EN sampled to CRS asserted	t3	–	3	4	BT
TX_EN sampled to CRS de-asserted	t4	–	4	16	BT
TX_EN sampled to TPO out (Tx latency)	t5	6	10	14	BT

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

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Figure 18: MII - 100BASE-TX Receive Timing / 5B Mode

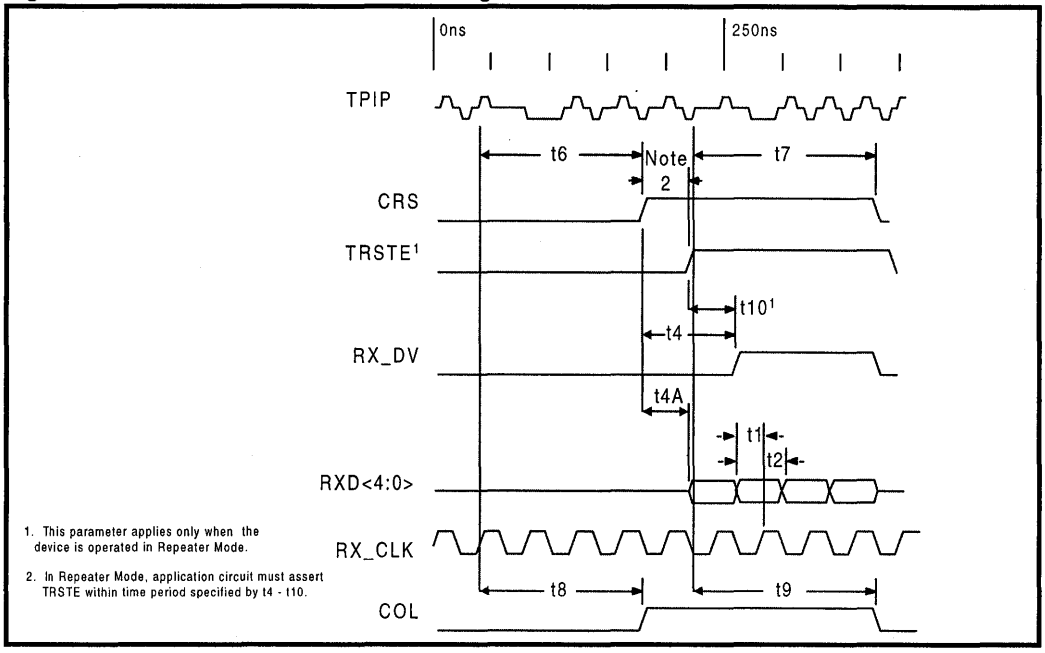

Table 31: MII - 100BASE-TX Receive Timing Parameters / 5B Mode (Over Recommended Range)

Parameter	Sym	Min	Typ[1]	Max	Units
RXD, RX_DV, RX_ER Setup to RX_CLK High	t1	10	–	–	ns
RXD, RX_DV, RX_ER Hold from RX_CLK High	t2	5	–	–	ns
CRS asserted to RX_DV asserted	t4	–	8	–	BT
CRS asserted to RXD<4:0> asserted	t4A	–	4	–	BT
Receive start of "J" to CRS asserted	t6	0	15 - 19	20	BT
Receive start of "T" to CRS de-asserted	t7	13	23 - 27	28	BT
Receive start of "J" to COL asserted	t8	0	15 - 19	20	BT
Receive start of "T" to COL de-asserted	t9	13	23 - 27	28	BT
TRSTE asserted to RX_DV, RXD<4:0> driven[2]	t10	–	20	–	ns

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. These parameters apply only when the device is operated in Repeater Mode

Figure 19: MII - 100BASE-TX Transmit Timing / 5B Mode

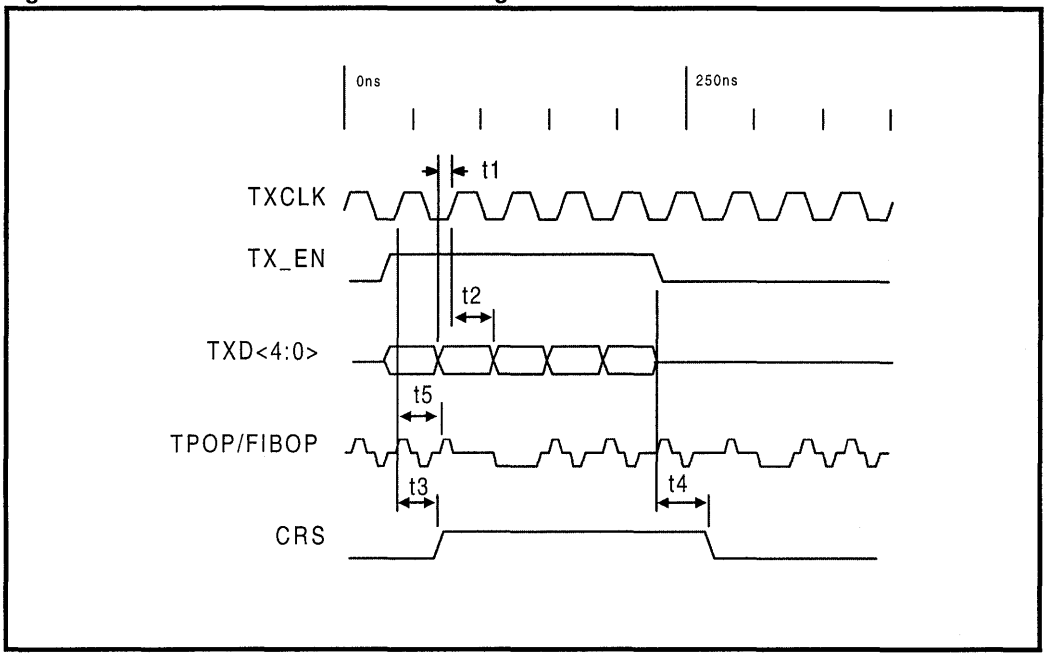

Table 32: MII - 100BASE-TX Transmit Timing Parameters / 5B Mode (Over Recommended Range)

Parameter	Sym	Min	Typ[1]	Max	Units
TXD, TX_EN, TX_ER Setup to TX_CLK High	t1	10	–	–	ns
TXD, TX_EN, TX_ER Hold from TX_CLK High	t2	5	–	–	ns
TX_EN sampled to CRS asserted	t3	–	3	4	BT
TX_EN sampled to CRS de-asserted	t4	–	4	16	BT
TX_EN sampled to TPO out (Tx latency)	t5	4	6	9	BT

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 20: MII - 100BASE-FX Receive Timing / 4B Mode

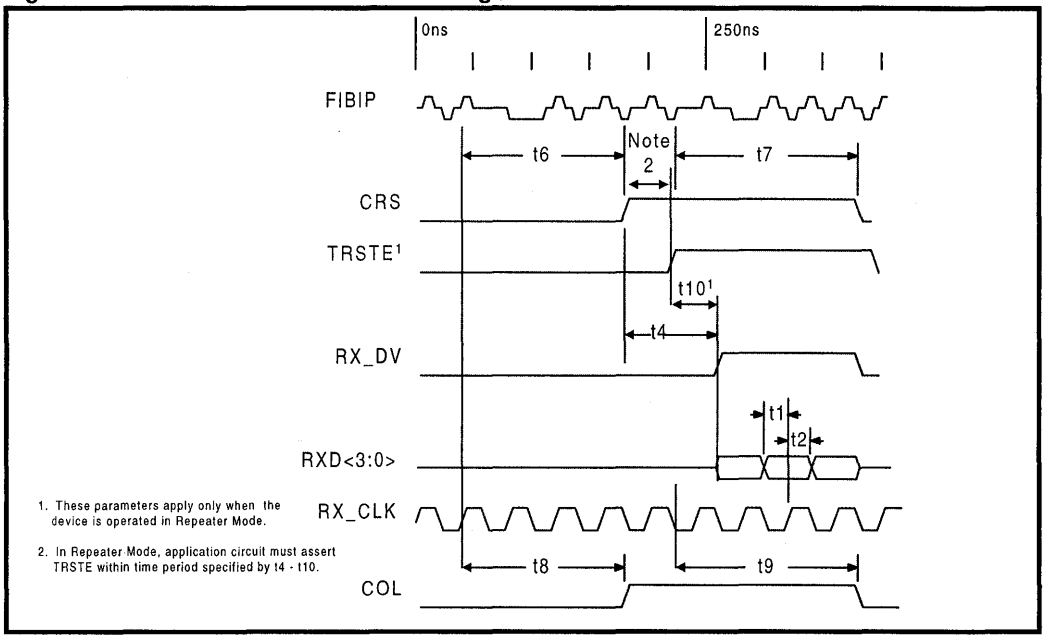

Table 33: MII - 100BASE-FX Receive Timing Parameters / 4B Mode (Over Recommended Range)

Parameter	Sym	Min	Typ[1]	Max	Units
RXD, RX_DV, RX_ER Setup to RX_CLK High	t1	10	–	–	ns
RXD, RX_DV, RX_ER Hold from RX_CLK High	t2	5	–	–	ns
CRS asserted to RXD<3:0>, RX_DV asserted	t4	–	8	–	BT
Receive start of "J" to CRS asserted	t6	0	13 - 17	20	BT
Receive start of "T" to CRS de-asserted	t7	13	21 - 25	26	BT
Receive start of "J" to COL asserted	t8	0	13 - 17	20	BT
Receive start of "T" to COL de-asserted	t9	13	21 - 25	26	BT
TRSTE asserted to RX_DV, RXD<3:0> driven[2]	t10	–	20	–	ns

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. These parameters apply only when the device is operated in Repeater Mode.

Figure 21: MII - 100BASE-FX Transmit Timing / 4B Mode

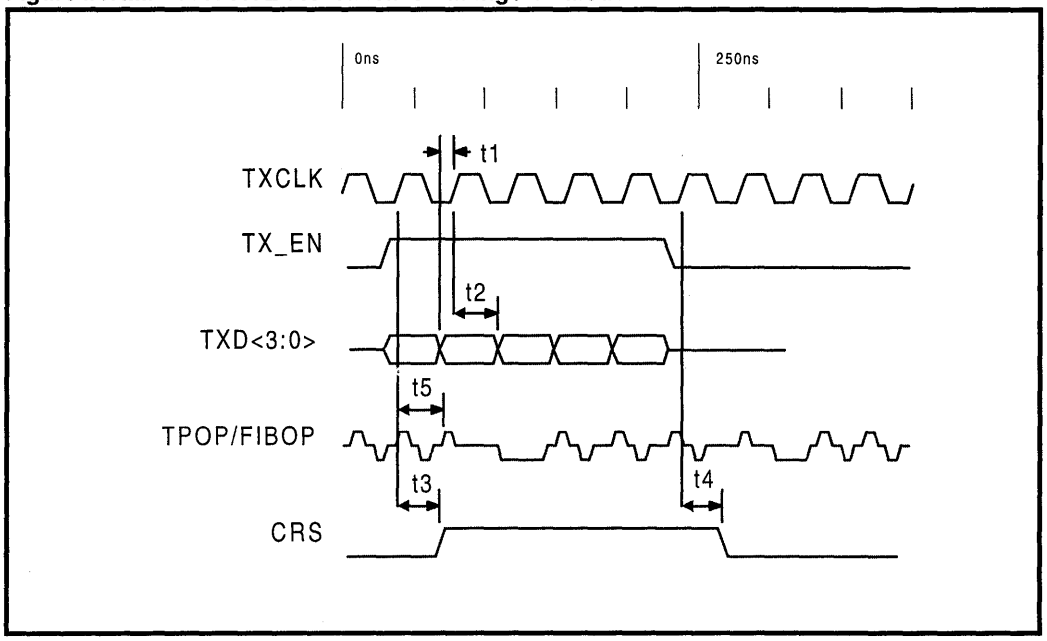

Table 34: MII - 100BASE-FX Transmit Timing Parameters / 4B Mode (Over Recommended Range)

Parameter	Sym	Min	Typ[1]	Max	Units
TXD<3:0>, TX_EN, TX_ER Setup to TX_CLK High	t1	10	–	–	ns
TXD<3:0>, TX_EN, TX_ER Hold from TX_CLK High	t2	5	–	–	ns
TX_EN sampled to CRS asserted	t3	–	3	4	BT
TX_EN sampled to CRS de-asserted	t4	–	4	16	BT
TX_EN sampled to TPO out (Tx latency)	t5	6	11	14	BT

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

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Figure 22: MII - 10BASE-T Receive Timing

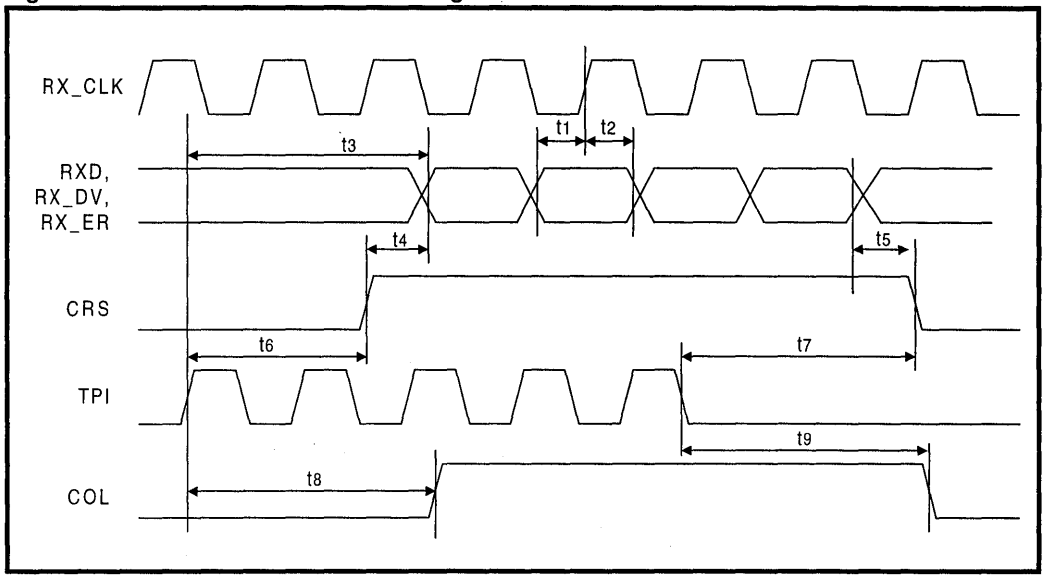

Table 35: MII - 10BASE-T Receive Timing Parameters (Over Recommended Range)

Parameter	Sym	Min	Typ[1]	Max	Units
RXD, RX_DV, RX_ER Setup to RX_CLK High	tI	10	–	–	ns
RXD, RX_DV, RX_ER Hold from RX_CLK High	t2	10	–	–	ns
TPI in to RXD out (Rx latency)	t3	–	–	73[3]	BT[2]
CRS asserted to RXD, RX_DV, RX_ER asserted	t4	0	–	69[3]	BT
RXD, RX_DV, RX_ER de-asserted to CRS de-asserted	t5	0	2.5 - 5.5	6	BT
TPI in to CRS asserted	t6	0	4	5	BT
TPI quiet to CRS de-asserted	t7	0	18	19	BT
TPI in to COL asserted	t8	0	4	5	BT
TPI quiet to COL de-asserted	t9	0	18	19	BT

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. IEEE 802.3 defines BT as "the duration of one bit as transferred to and from the MAC. The bit time is the reciprocal of the bit rate. For example, for 10BASE-T the bit time is 10^{-7} or 100 ns."
3. CRS is asserted. RXD/RX_DV are not driven during preamble and SFD (64 BT).

Figure 23: MII - 10BASE-T Transmit Timing

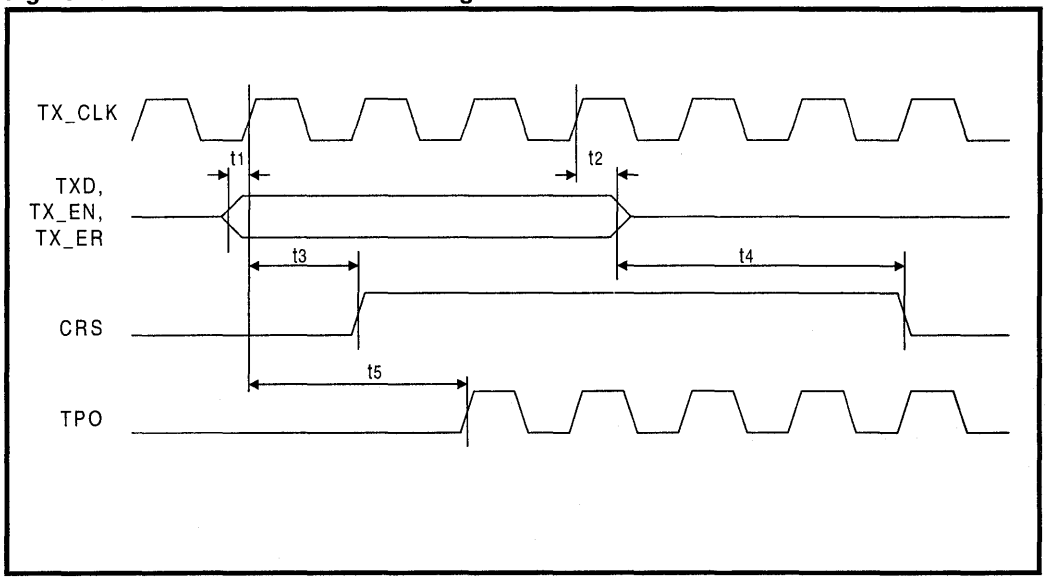

Table 36: MII - 10BASE-T Transmit Timing Parameters (Over Recommended Range)

Parameter	Sym	Min	Typ[1]	Max	Units
TXD, TX_EN, TX_ER Setup to TX_CLK High	t1	10	–	–	ns
TXD, TX_EN, TX_ER Hold from TX_CLK High	t2	5	–	–	ns
TX_EN sampled to CRS asserted	t3	–	0	4	BT
TX_EN sampled to CRS de-asserted	t4	–	8	–	BT
TX_EN sampled to TPO out (Tx latency)	t5	–	3 - 5	–	BT

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

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Figure 24: 10BASE-T SQE (Heartbeat) Timing

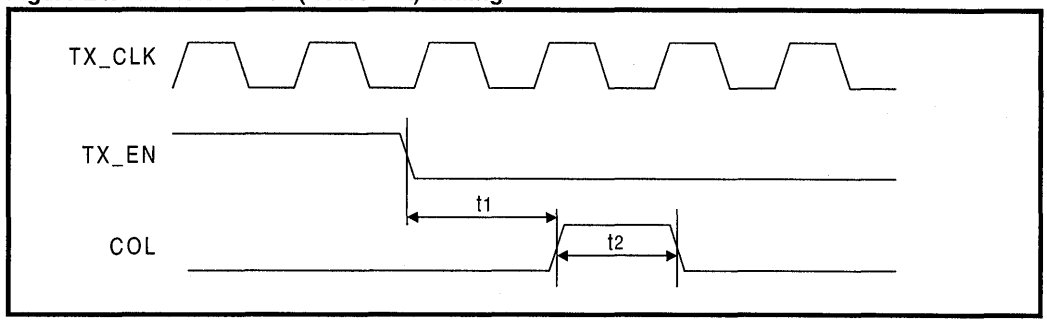

Table 37: 10BASE-T SQE (Heartbeat) Timing Parameters (Over Recommended Range)

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
COL (SQE) Delay after TX_EN off	t1	0.65	1.0	1.6	µs	
COL (SQE) Pulse duration	t2	.5	1.0	1.5	µs	

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 25: 10BASE-T Jab and Unjab Timing

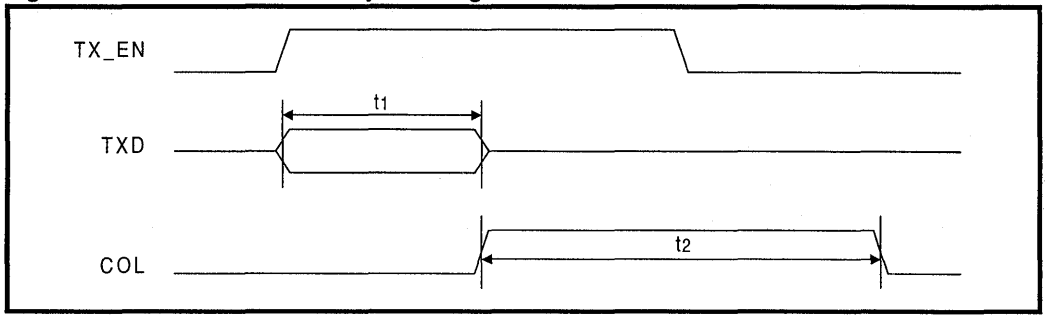

Table 38: 10BASE-T Jab and Unjab Timing Parameters (Over Recommended Range)

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Maximum Transmit time	t1	20	96 - 128	150	ms	
Unjab time	t2	250	525	750	ms	

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing. Typical transmit and unjab times may be either of these values depending on internal 32 ms clock synchronization.

Figure 26: Auto Negotiation and Fast Link Pulse Timing

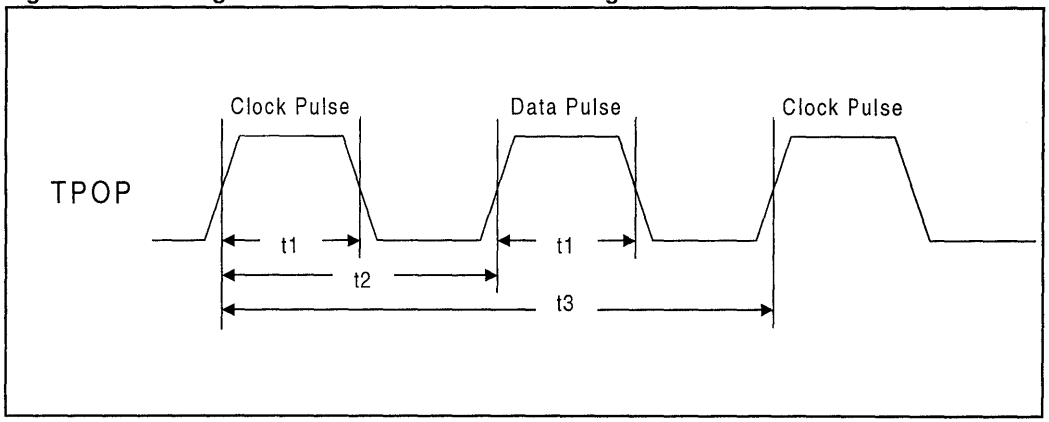

Figure 27: Fast Link Pulse Timing

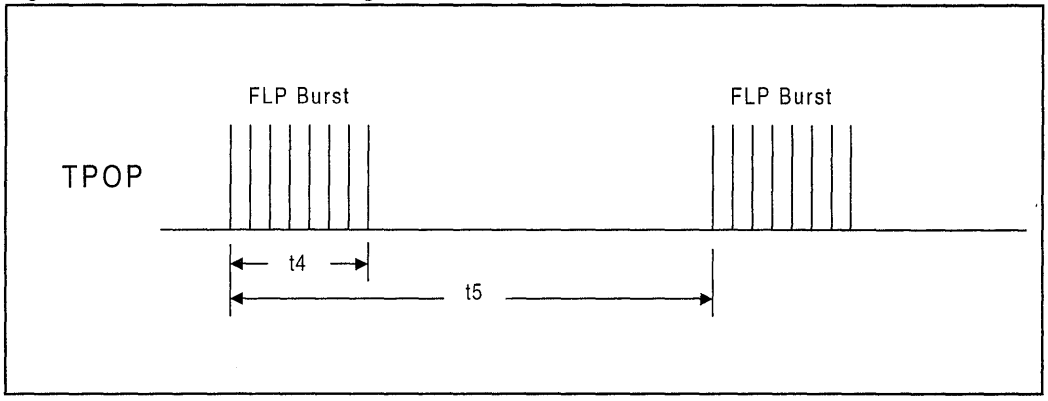

Table 39: Auto Negotiation and Fast Link Pulse Timing Parameters (Over Recommended Range)

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Clock/Data pulse width	t1	–	100	–	ns	
Clock pulse to Data pulse	t2	55.5	62.5	69.5	µs	
Clock pulse to Clock pulse	t3	111	125	139	µs	
FLP burst width	t4	–	2	–	ms	
FLP burst to FLP burst	t5	8	12	24	ms	
Clock/Data pulses per burst	–	17	–	33	ea	

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

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Figure 28: MDIO Timing when Sourced by STA

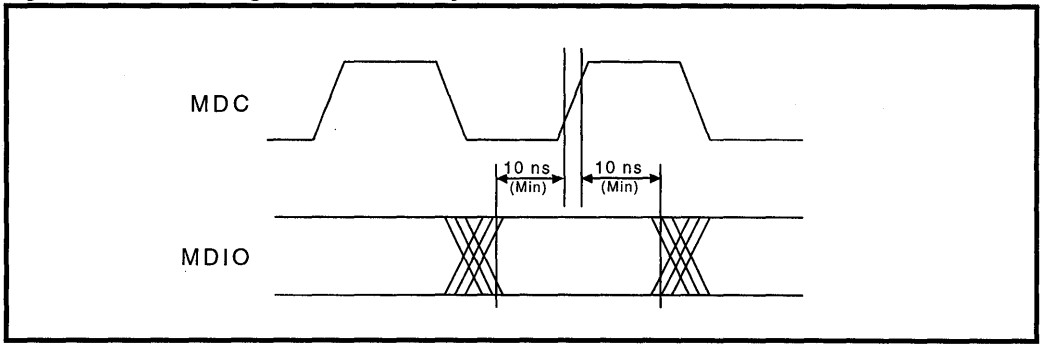


Figure 29: MDIO Timing when Sourced by PHY

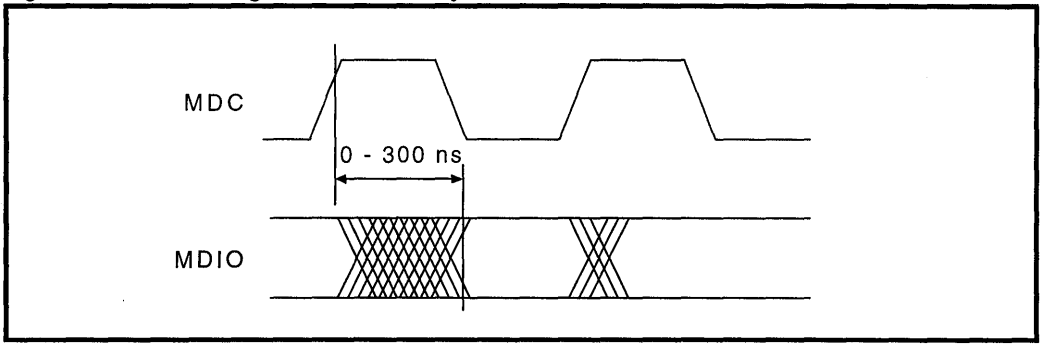


Table 40: MDIO Timing Parameters (Over Recommended Range)

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
MDIO Setup before MDC	–	10	–	–	ns	When sourced by STA
MDIO Hold after MDC	–	10	–	–	ns	When sourced by STA
MDC to MDIO Output delay	–	0	10	300	ns	When sourced by PHY

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.

Figure 30: Miscellaneous Timing Parameters (Over Recommended Range)

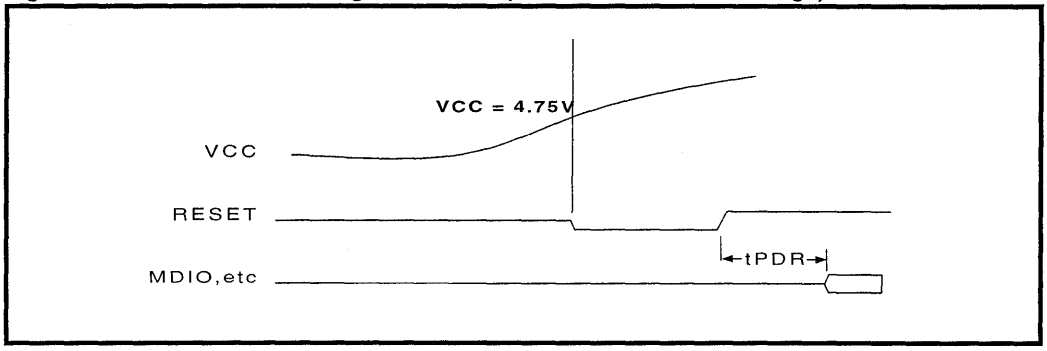


Table 41: Miscellaneous Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Power Down recovery time	tPDR	–	50	–	ms	

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.

REGISTER DEFINITIONS

The LXT970 register set includes a total of 12 16-bit registers. Refer to Table 42 for a complete register listing.

- Seven base registers (0 through 6) are defined in accordance with the "Reconciliation Sublayer and Media Independent Interface" and "Physical Layer Link Signalling for 10/100 Mbps Auto-Negotiation" sections of the IEEE 802.3 specification (Register 7, Next Page, is not supported).
- Five additional registers (16 through 20) are defined in accordance with the IEEE 802.3 specification for adding unique chip functions.

Table 42: Register Set

Address	Register Name	Bit Assignments
0	Control Register	Refer to Table 43
1	Status Register	Refer to Table 44
2	PHY Identification Register 1	Refer to Table 45
3	PHY Identification Register 2	Refer to Table 46
4	Auto-Negotiation Advertisement Register	Refer to Table 47
5	Auto-Negotiation Link Partner Ability Register	Refer to Table 48
6	Auto-Negotiation Expansion Register	Refer to Table 49
16	Mirror Register	Refer to Table 50
17	Interrupt Enable Register	Refer to Table 51
18	Interrupt Status Register	Refer to Table 52
19	Configuration Register	Refer to Table 53
20	Chip Status Register	Refer to Table 54

Table 43: Control Register (Address 0)

Bit	Name	Description	Type [1]	Default
0.15	Reset	1 = Reset chip. 0 = Enable normal operation.	R/W SC	0
0.14	Loopback	1 = Enable loopback mode. When Loopback is enabled, during 100Mbps operation, the LXT970 disconnects its transmitter and receiver from the network. Data sent by the controller passes through the chip and then gets looped back to the MII. During 10Mbps operation, data is looped directly back to the MII. 0 = Disable loopback mode.	R/W	0
0.13	Speed Selection	1 = 100 Mbps 0 = 10 Mbps	R/W	Note 2
0.12	Auto-Negotiation Enable	1 = Enable auto-negotiate process (overrides speed select and duplex mode bits). 0 = Disable auto-negotiate process.	R/W	Note 3
0.11	Power Down	1 = Enable power down. 0 = Enable normal operation.	R/W	Note 4
0.10	Isolate	1 = Electrically isolate LXT970 from MII. 0 = Normal operation.	R/W	Note 5
0.9	Restart Auto-Negotiation	1 = Restart auto-negotiation process. 0 = Normal operation.	R/W SC	Note 6
0.8	Duplex Mode	1 = Enable full duplex. 0 = Enable half duplex.	R/W	Note 7
0.7	Collision Test	1 = Enable COL signal test. Bit 0.14 must be enabled to use this bit. This bit is used in conjunction with bit 0.14 to test the COL output. 0 = Disable COL signal test.	R/W	0 Note 8
0.6:4	Transceiver Test Mode	Not Supported	RO	0
0.3	Master-Slave Enable	Not Supported	RO	0
0.2	Master-Slave Value	Not Supported	RO	0
0.1:0	Reserved		R/W	0

1. R/W = Read/Write
   SC = Self Clearing
2. If auto-negotiation is enabled, this bit is ignored. If auto-negotiation is disabled, the default value of bit 0.13 is determined by pin CFG0.
3. The default value of bit 0.12 is determined by pin MF0/AUTO-NEG.
4. The LXT970 will internally reset all registers to their default values upon exiting power down mode. A delay of 500 ns minimum is required from the time power down is cleared until any register can be written.
5. The default value of bit 0.10 is determined by pin TRSTE.
6. If auto-negotiation is enabled, the default value of bit 0.9 is determined by pin CFG0. If auto-negotiation is disabled, the default value of bit 0.9 = 0.
7. If auto-negotiation is enabled, this bit is ignored. If auto-negotiation is disabled, the default value of bit 0.8 is determined by pin FDE.
8. This bit is ignored unless loopback is enabled (0.14 = 1).

Table 44: Status Register (Address 1)

Bit	Name	Description	Type [1]	Default
1.15	100BASE-T4	Not Supported	RO	0
1.14	100BASE-X Full Duplex	1 = LXT970 able to perform full duplex 100BASE-X.	RO	1
1.13	100BASE-X Half Duplex	1 = LXT970 able to perform half duplex 100BASE-X	RO	1
1.12	10 Mb/s Full Duplex	1 = LXT970 able to operate at 10 Mb/s in full duplex mode	RO	1
1.11	10 Mb/s Half Duplex	1 = LXT970 able to operate at 10 Mb/s in half duplex mode	RO	1
1.10	100BASE-T2 Full Duplex	Not Supported	RO	0
1.9	100BASE-T2 Half Duplex	Not Supported	RO	0
1.8	Reserved	Ignore on read	RO	0
1.7	Master-Slave Configuration Fault	Not Supported	RO	0
1.6	MF Preamble Suppression	0 = LXT970 will not accept management frames with preamble suppressed.	RO	0
1.5	Auto-Negotiation Complete	1 = Auto-negotiation process complete. 0 = Auto-negotiation process not complete.	RO	0
1.4	Remote Fault	1 = Remote fault condition detected. 0 = No remote fault condition detected.	RO/LH	0
1.3	Auto-Negotiation Ability	1 = LXT970 is able to perform auto-negotiation.	RO	1
1.2	Link Status	1 = Link is up. 0 = Link is down.	RO/LL	0
1.1	Jabber Detect (10BASE-T Only)	1 = Jabber condition detected. 0 = No jabber condition detected.	RO/LH	0
1.0	Extended Capability	1 = Extended register capabilities.	RO	1

1. RO = Read Only
LL = Latching Low (This bit remains Low until read, and then returns High).
LH = Latching High (This bit remains High until read, and then returns Low).

Table 45: PHY Identification Register 1 (Address 2)

Bit	Name	Description	Type [1]	Default
2.15:0	PHY ID Number	The PHY identifier composed of bits 3 through 18 of the OUI.	RO	7810 hex

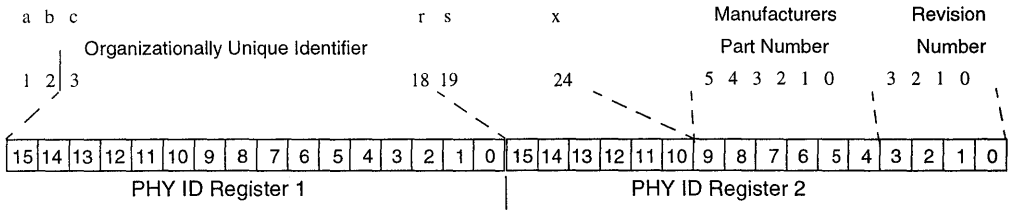
1. RO = Read Only

Table 46: PHY Identification Register 2 (Address 3)

Bit	Name	Description	Type [1]	Default
3.15:10	PHY ID number	The PHY identifier composed of bits 19 through 24 of the OUI.	RO	000000 bin
3.9:4	Manufacturer's model number	6 bits containing manufacturer's part number.	RO	000000 bin
3.3:0	Manufacturer's revision number	4 bits containing manufacturer's revision number.	RO	0000 bin

1. RO = Read Only

Figure 31: PHY Identifier Bit Mapping



The Level One OUI is 00207B hex.

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Table 47: Auto Negotiation Advertisement Register (Address 4)

Bit	Name	Description	Type [1]	Default
4.15	Next Page	Not Supported	RO	0
4.14	Reserved		RO	0
4.13	Remote Fault	1 = Remote fault. 0 = No remote fault.	R/W	0
4.12:10	Reserved		R/W	0
4.9	100BASE-T4	1 = 100BASE-T4 capability is available. 0 = 100BASE-T4 capability is not available. (The LXT970 does not support 100BASE-T4 but allows this bit to be set to advertise in the Auto-Negotiation sequence for 100BASE-T4 operation. An external 100BASE-T4 transceiver could be switched in if this capability is desired.)	R/W	0
4.8	100BASE-TX Full Duplex	1 = DTE is 100BASE-TX full duplex capable. 0 = DTE is not 100BASE-TX full duplex capable.	R/W	Note 2
4.7	100BASE-TX	1 = DTE is 100BASE-TX capable. 0 = DTE is not 100BASE-TX capable.	R/W	Note 3
4.6	10BASE-T full duplex	1 = DTE is 10BASE-T full duplex capable. 0 = DTE is not 10BASE-T full duplex capable.	R/W	Note 4
4.5	10BASE-T	1 = DTE is 10BASE-T capable. 0 = DTE is not 10BASE-T capable.	R/W	Note 5
4.4:0	Selector Field, S<4:0>	<00001> = IEEE 802.3 <00010> = IEEE 802.9 ISLAN-16T <00000> = Reserved for future Auto-Negotiation development <11111> = Reserved for future Auto-Negotiation development Unspecified or reserved combinations should not be transmitted.	R/W	00001

1. R/W = Read/Write
   RO = Read Only
2. The default value of bit 4.8 is determined by pin FDE ANDed with pin MF4/100BASE-TX/FX.
3. The default value of bit 4.7 is determined by pin MF4/100BASE-TX/FX.
4. The default value of bit 4.6 is determined by pin FDE AND'ed with pin CFG1.
5. The default value of bit 4.5 is determined by pin CFG1.

Table 48: Auto Negotiation Link Partner Ability Register (Address 5)

Bit	Name	Description	Type [1]	Default
5.15	Next Page	1 = Link Partner has ability to send multiple pages. 0 = Link Partner has no ability to send multiple pages.	RO	N/A
5.14	Acknowledge	1 = Link Partner has received Link Code Word from LXT970. 0 = Link Partner has not received Link Code Word from LXT970.	RO	N/A
5.13	Remote Fault	1 = Remote fault. 0 = No remote fault.	RO	N/A
5.12:10	Reserved		RO	N/A
5.9	100BASE-T4	1 = Link Partner is 100BASE-T4 capable. 0 = Link Partner is not 100BASE-T4 capable.	RO	N/A
5.8	100BASE-TX full duplex	1 = Link Partner is 100BASE-TX full duplex capable. 0 = Link Partner is not 100BASE-TX full duplex capable.	RO	N/A
5.7	100BASE-TX	1 = Link Partner is 100BASE-TX capable. 0 = Link Partner is not 100BASE-TX capable.	RO	N/A
5.6	10BASE-T full duplex	1 = Link Partner is 10BASE-T full duplex capable. 0 = Link Partner is not 10BASE-T full duplex capable.	RO	N/A
5.5	10BASE-T	1 = Link Partner is 10BASE-T capable. 0 = Link Partner is not 10BASE-T capable.	RO	N/A
5.4:0	Selector Field S[4:0]	<00001> = IEEE 802.3 <00010> = IEEE 802.9 ISLAN-16T <00000> = Reserved for future Auto-Negotiation development <11111> = Reserved for future Auto-Negotiation development Unspecified or reserved combinations shall not be transmitted.	RO	N/A

1. RO = Read Only

Table 49: Auto Negotiation Expansion (Address 6)

Bit	Name	Description	Type [1]	Default
6.15:5	Reserved	Ignore.	RO	0
6.4	Parallel Detection Fault	1 = Parallel detection fault has occurred. 0 = Parallel detection fault has not occurred.	RO/ LH	0
6.3	Link Partner Next Page Able	1 = Link partner is next page able. 0 = Link partner is not next page able.	RO	0

1. RO = Read Only
LH = Latching High (This bit remains High until read, and then returns Low).

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Table 49: Auto Negotiation Expansion (Address 6) – continued

Bit	Name	Description	Type [1]	Default
6.2	Next Page Able	Not Supported	RO	0
6.1	Page Received	1 = 3 identical and consecutive link code words have been received from link partner. 0 = 3 identical and consecutive link code words have not been received from link partner.	RO/ LH	0
6.0	Link Partner Auto Neg Able	1 = Link partner is auto-negotiation able. 0 = Link partner is not auto-negotiation able.	RO	0

1. RO = Read Only
LH = Latching High (This bit remains High until read, and then returns Low).

Table 50: Mirror Register (Address 16, Hex 10)

Bit	Name	Description	Type [1]	Default
16.15:0	User Defined	This register is intended for use in checking the MII serial port and has no effect on chip operation.	R/W	0

1. R/W = Read /Write

Table 51: Interrupt Enable Register (Address 17, Hex 11)

Bit	Name	Description	Type [1]	Default
17.15:2	Reserved	Write as 0; ignore on read.	R/W	N/A
17.1	INTEN	1 = Enable interrupts on pin 2. Must be enabled for bit 17.0 or 19.12 to be effective. 0 = Enable Half/Full duplex indications on pin 2.	R/W	0
17.0	TINT	1 = Forces MDINT Low and sets bit 18.15 = 1. Also forces interrupt pulse on MDIO when bit 19.12 = 1. 0 = Normal operation. This bit is ignored unless the interrupt function is enabled (17.1 = 1).	R/W	0

1. R/W = Read /Write

Table 52: Interrupt Status Register (Address 18, Hex 12)

Bit	Name	Description	Type [1]	Default
18.15	MINT	1 = Indicates MII interrupt pending. 0 = Indicates no MII interrupt pending. This bit is cleared by reading Register 1 followed by reading Register 18.	RO	N/A
18.14	XTALOK	1 = Indicates that the LXT970 is fully powered up and the on-chip clocks are stable. 0 = Indicates that XTAL circuit is not stable.	RO	0
18.13:0	Reserved	Ignore	RO	0

1. RO = Read Only

Table 53: Configuration Register (Address 19, Hex 13)

Bit	Name	Description	Type [1]	Default
19.15	Reserved	Write as 0; ignore on read.	R/W	N/A
19.14	Txmit Test (100BASE-TX)	1 = 100BASE-T transmit test enabled, LXT970 will transmit data regardless of link status. This function is the analog of the link test function (19.8) for 100BASE-TX. 0 = Normal operation.	R/W	0
19.13	Repeater Mode	1 = Enable Repeater Mode. 0 = Enable DTE Mode.	R/W	Note 2
19.12	MDIO_INT	1 = Enable interrupt signaling on MDIO (if 17.1 = 1). 0 = Normal operation (MDIO Interrupt disabled). Bit is ignored unless the interrupt function is enabled (17.1 = 1).	R/W	0
19.11	TP Loopback (10BASE-T)	1 = Disable 10BT TP Loopback. Data transmitted by the MAC will not loopback to the RXD and RX_DV pins. CRS is asserted during a transmission only in DTE mode and half-duplex operation. 0 = Enable 10BT TP Loopback	R/W	0
19.10	SQE (10BASE-T)	1 = Enable SQE. 0 = Disable SQE (Default).	R/W	0
19.9	Jabber (10BASE-T)	1 = Disable jabber. 0 = Normal operation (jabber enabled).	R/W	0
19.8	Link Test (10BASE-T)	1 = Disable 10BASE-T link integrity test. 0 = Normal operation (10BASE-T link integrity test enabled).	R/W	Note 3

1. R/W = Read/Write
2. The default value of bit 19.13 is determined by pin MF1/AUTO-NEG.
3. If auto-negotiation is disabled, the default value of bit 19.8 is determined by pin CFG1. If auto-neg is enabled, the default value of bit 19.8 = 0.
4. The default value of bit 19.4 is determined by pin MF2/ENCODER Operation.
5. The default value of bit 19.3 is determined by pin MF3/SCRAMBLER Operation.
6. If auto-negotiation is disabled, default value of bit 19.2 is determined by pin MF4/100BASE-TX/FX. If auto-negotiation is enabled, default value of bit 19.2 = 0.

Table 53: Configuration Register (Address 19, Hex 13) – continued

Bit	Name	Description	Type [1]	Default
19.7:6	LEDC Programming bits	Determine condition indicated by LEDC. bit 7 bit 6 Description 0 0 LEDC indicates collision 0 1 LEDC is off 1 0 LEDC indicates activity. 1 1 LEDC is continuously on (for diagnostic use).	R/W	0,0
19.5	Advance TX Clock	1 = TX clock is advanced relative to TXD<4:0> and TX_ER by 1/2 TX_CLK cycle. 0 = Normal operation.	R/W	0
19.4	4B Nibble/ 5BSymbol (100BASE-X only)	1 = 5-bit Symbol Mode (Bypass encoder/decoder); RXD<4:0> symbol data is not aligned. 0 = 4-bit Nibble Mode (Normal operation).	R/W	Note 4
19.3	Scrambler (100BASE-X only)	1 = Bypass transmit scrambler and receive descrambler. 0 = Normal operation (scrambler and descrambler enabled). In FX mode, the LXT970 *automatically* bypasses the Scrambler. *Selecting* Scrambler bypass in FX mode will cause the LXT970 to also bypass the 4B/5B encoder and enable Symbol mode MII operation.	R/W	Note 5
19.2	100BASE-FX	1 = Enable 100BASE fiber interface. 0 = Enable 100BASE twisted pair interface.	R/W	Note 6
19.1	Reserved	Write as 0; Ignore on read.	R/W	0
19.0	Transmit Disconnect	1 = Disconnect TP transmitter from line. 0 = Normal operation.	R/W	0

1. R/W = Read/Write
2. The default value of bit 19.13 is determined by pin MF1/AUTO-NEG.
3. If auto-negotiation is disabled, the default value of bit 19.8 is determined by pin CFG1. If auto-neg is enabled, the default value of bit 19.8 = 0.
4. The default value of bit 19.4 is determined by pin MF2/ENCODER Operation.
5. The default value of bit 19.3 is determined by pin MF3/SCRAMBLER Operation.
6. If auto-negotiation is disabled, default value of bit 19.2 is determined by pin MF4/100BASE-TX/FX. If auto-negotiation is enabled, default value of bit 19.2 = 0.

Table 54: Chip Status Register (Address 20, Hex 14)

Bit	Name	Description	Type [1]	Default
20.15:14	Reserved	Ignore.	RO	N/A
20.13	Link	1 = Link is up. 0 = Link is down. Link bit 20.13 is a duplicate of bit 1.2, except that it is a dynamic indication, whereas bit 1.2 latches Low.	RO	0
20.12	Duplex Mode	1 = Full Duplex. 0 = Half Duplex.	RO	Note 2
20.11	Speed	1 = 100 Mbps operation. 0 = 10 Mbps operation.	RO	Note 2
20.10	Reserved	Ignore.	RO	N/A
20.9	Auto-Negotiation Complete	1 = Auto-negotiation process complete. 0 = Auto-negotiation process not complete. Auto-Negotiation Complete bit 20.9 is a duplicate of bit 1.5.	RO/LH	0
20.8	Page Received	1 = Three identical and consecutive link code words have been received. 0 = Three identical and consecutive link code words have not been received. Page Received bit 20.8 is a duplicate of bit 6.1	RO/LH	0
20:7	Reserved	Write as 0; Ignore on read.	RO/LH	0
20.6	Stream scrambler/ decoder lock (100BASE-TX only)	1 = Stream scrambler/decoder locked. 0 = Stream scrambler/decoder not locked.	RO	0
20.5	Symbol Error	1 = Symbol error detected. 0 = No symbol error detected.	RO/LH	N/A
20.4	MLT3 Encoding Error	1 = MLT3 encoding error detected. 0 = No MLT3 encoding error detected.	RO/LH	N/A
20.3	Reserved	Ignore.	RO	N/A
20.2	Low Voltage	1 = Low voltage fault on VCC has occurred. 0 = No fault.	RO/LH	N/A
20.1	Reserved	Ignore.	RO	N/A
20.0	PLL Lock (100BASE-TX)	1 = 100BASE-TX/FX Receiver PLL is not locked. 0 = PLL is locked.	RO/LH	N/A

1. RO = Read Only
   LH = Latching High (This bit remains High until read, and then returns Low).
2. Bits 20.12 and 20.11 reflect the current operating mode of the LXT970.

NOTES

LXT974

Fast Ethernet 10/100 Quad Transceiver

General Description

The LXT974 is a 4-port Fast Ethernet Transceiver which supports IEEE 802.3 physical layer applications at both 10 Mbps and 100 Mbps. It provides all the active circuitry to interface four 802.3 media independent interface (MII) compliant controllers to 10BASE-T and/or 100BASE-TX media. Each LXT974 PHY port also provides a PECL-type interface for 100BASE-FX fiber networks.

The LXT974 provides a complete multi-mode MII. In addition to the standard MII mode, LXT974 offers a Super MII mode which multiplexes a single MII to all 4 ports for switch applications, and a Shared MII for repeater applications. The LXT974 provides three separate LED drivers for each of the four PHY ports and a serial LED interface.

In addition to standard CSMA/CD Ethernet, the chip supports full duplex operation at 10 Mbps and 100 Mbps.

The LXT974 is fabricated with an advanced CMOS process and requires only a single 5 volt power supply.

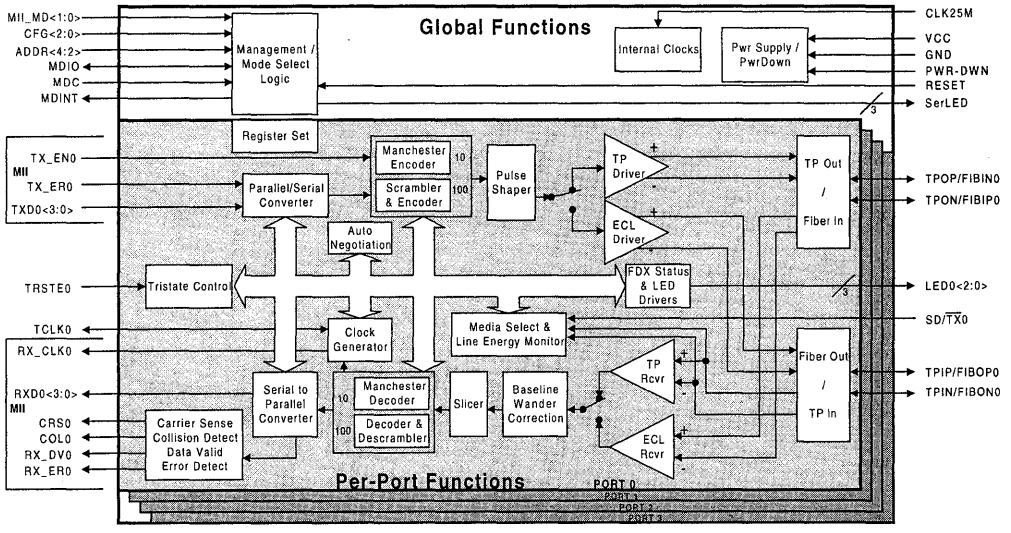
Applications

- 10BASE-T, 10/100-TX, or 100BASE-FX Switches
- 10BASE-T, 10/100-TX, or 100BASE-FX Repeaters

Features

- Four independent IEEE 802.3-compliant 10BASE-T or 100BASE-TX ports in a single chip
- 100BASE-FX fiber optic capable
- Standard CSMA/CD or full duplex operation at 10 or 100 Mbps
- Compliant with IEEE 802.3u auto-negotiation protocol and with legacy 10BASE-T and 100BASE-T systems without auto-negotiation capability
- On-chip transmit and receive filtering for 10BASE-T and 100BASE-TX
- Baseline wander correction
- Configurable on-chip LED drivers as well as serial LED output
- Super MII Interface Mode for reducing customer ASIC pin requirements.
- Configurable through MII serial port or via external control pins
- CMOS process with single 5 volt supply operation
- Available in 160-pin MQUAD

LXT974 Block Diagram



NOTES

Ethernet Hub and Repeater Products

DATA SHEET

LXT914

Flexible Quad Ethernet Repeater

JUNE 1997
Revision 2.2

General Description

The LXT914 is an integrated multi-port repeater designed for mixed-media networks. It provides all the active circuitry required for the repeater function in a single CMOS device. It includes one Attachment Unit Interface (AUI) port and four 10BASE-T transceivers. The AUI port is mode selectable: DTE mode allows connection of an external transceiver (10BASE2, 10BASE5, 10BASE-T or FOIRL) or a drop cable. MAU mode creates a MAU output allowing direct connection to another DTE interface. The 10BASE-T transceivers are entirely self-contained with internal filters which simplify the design work required for FCC-compliant EMI performance.

An inter-repeater backplane interface allows 128 or more 10BASE-T ports to be cascaded together. In addition, a serial port provides information for network management.

The LXT914 requires only a single 5-volt power supply due to an advanced CMOS fabrication process.

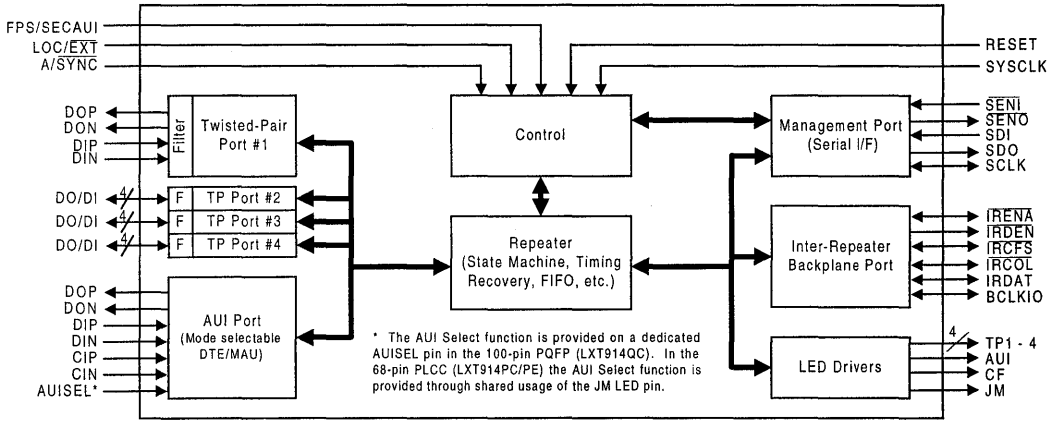
Applications

- LAN Repeaters
- Integrated Repeaters
- Switched Repeater Clusters

Features

- Four integrated 10BASE-T transceivers and one AUI transceiver on a single chip
- Programmable DTE/MAU interface on AUI port
- Seven integrated LED drivers with four unique operational modes
- On-chip transmit and receive filtering
- Automatic partitioning of faulty ports, enabled on an individual port basis
- Automatic polarity detection and correction
- Programmable squelch level allows extended range in low-noise environments
- Synchronous or asynchronous inter-repeater backplane supports "hot swapping"
- Inter-repeater backplane allows cascaded repeaters, linking 128 or more 10BASE-T ports
- Serial port for selecting programmable options
- 68-pin PLCC (Commercial or Extended temp range)
- 100-pin PQFP (Commercial temp range)

LXT914 Block Diagram



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LXT914 PIN ASSIGNMENTS AND SIGNAL DESCRIPTIONS

Figure 1: LXT914 Pin Assignments

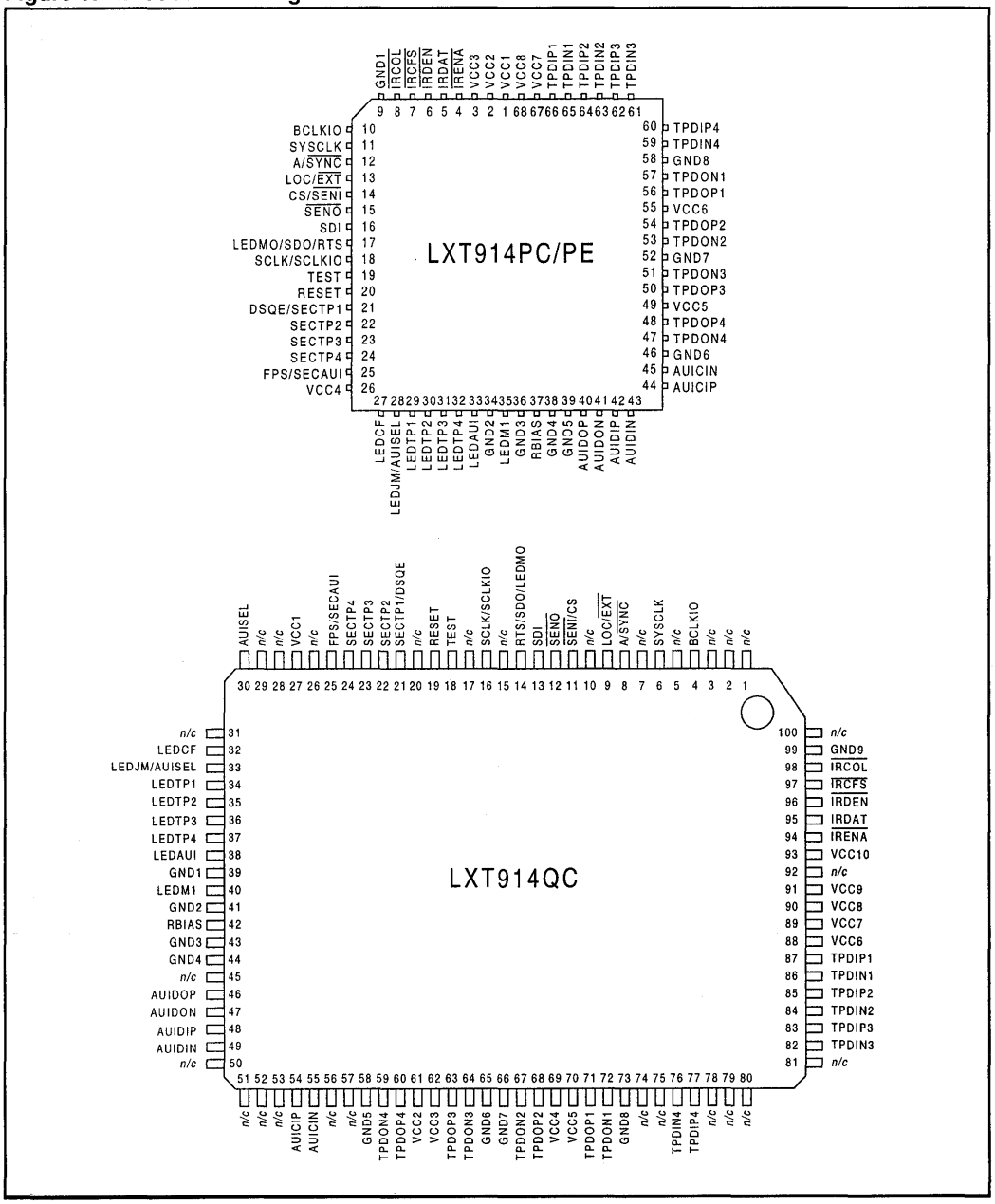

Table 1: LXT914 Power, Ground and Clock Signal Descriptions

Pin #		Symbol	I/O	Description
PLCC	PQFP			
1	27	VCC1	—	**Power Supply Inputs.** These pins each require a +5 VDC power supply. The various pins may be supplied from a single power source, but special de-coupling requirements may apply. Each VCC input must be within ±0.3 V of every other VCC input.
2	61	VCC2	—	
3	62	VCC3	—	
26	69	VCC4	—	
49	70	VCC5	—	
55	88	VCC6	—	
67	89	VCC7	—	
68	90	VCC8	—	
—	91	VCC9	—	
—	93	VCC10	—	
9	39	GND1	—	**Ground.** These pins provide ground return paths for the various power supply pins.
34	41	GND2	—	
36	43	GND3	—	
38	44	GND4	—	
39	58	GND5	—	
46	65	GND6	—	
52	66	GND7	—	
58	73	GND8	—	
—	99	GND9	—	
37	42	RBIAS	—	**Bias.** This pin provides bias current for the internal circuitry. The 100 µA bias current is provided through an external 12.4 kΩ resistor to ground.
10	4	BCLKIO	I/O	**Backplane Clock.** This 10 MHz clock synchronizes multiple repeaters on a common backplane. In the synchronous mode, BCLKIO must be supplied to all repeaters from a common external source. In the asynchronous mode, BCLKIO is supplied only when a repeater is outputting data to the bus. Each repeater outputs its internally recovered clock when it takes control of the bus. Other repeaters on the backplane then sync to BCLKIO for the duration of the transmission.
11	6	SYSCLK	I	**System Clock.** The required 20 MHz system clock is input at this pin. Clock must have a 40-60 duty cycle with < 10 ns rise time.

Table 2: LXT914 Inter-Repeater Backplane Signal Descriptions

PLCC	PQFP	Symbol	I/O	Description
4	94	$\overline{\text{IRENA}}$	I/O	**Inter-Repeater Backplane Enable.** This pin allows individual LXT914 repeaters to take control of the Inter-Repeater Backplane (IRB) data bus (IRDAT). The $\overline{\text{IRENA}}$ bus must be pulled up locally by a 330 Ω resistor.[1]
5	95	IRDAT	I/O	**IRB Data.** This pin is used to pass data between multiple repeaters on the IRB. The IRDAT bus must be pulled up locally by a 330 Ω resistor.[1]
6	96	$\overline{\text{IRDEN}}$	O	**IRB Driver Enable.** The $\overline{\text{IRDEN}}$ pin is used to enable external bus drivers which may be required in synchronous systems with large backplanes. This is an active Low signal, maintained for the duration of the data transmission. $\overline{\text{IRDEN}}$ must be pulled up locally by a 330 Ω resistor.
7 8	97 98	$\overline{\text{IRCFS}}$ $\overline{\text{IRCOL}}$	I/O I/O	**IRB Collision Flag Sense** ($\overline{\text{IRCFS}}$) and **IRB Collision** ($\overline{\text{IRCOL}}$). These two pins are used for collision signalling between multiple LXT914 devices on the Inter-Repeater Backplane (IRB). Both the $\overline{\text{IRCFS}}$ bus and the $\overline{\text{IRCOL}}$ bus must be pulled up globally with 330 Ω resistors. ($\overline{\text{IRCFS}}$ requires a precision resistor [±1%].)[2]

1. $\overline{\text{IRENA}}$ and IRDAT can be buffered between boards in multi-board configurations. Where buffering is used, a 330 Ω pull-up resistor can be used on each signal, on each board. Where no buffering is used, the total impedance should be no less than 330 Ω.
2. $\overline{\text{IRCFS}}$ and $\overline{\text{IRCOL}}$ cannot be buffered. In multi-board configurations, the total impedance on $\overline{\text{IRCOL}}$ should be no smaller than 330 Ω. $\overline{\text{IRCFS}}$ should be pulled up only once, by a single 330 Ω, 1% resistor.

Table 3: LXT914 Mode Select and Control Signal Descriptions

PLCC	PQFP	Symbol	I/O	Description
12	8	A/$\overline{\text{SYNC}}$	I	**Backplane Sync Mode Select.** This pin selects the backplane sync mode. When this pin is left floating an internal pull-up defaults to the Asynchronous mode (A/$\overline{\text{SYNC}}$ High). In the asynchronous mode 12 or more LXT914s can be connected on the backplane, and an external 10 MHz backplane clock source is not required. When the synchronous mode is selected (A/$\overline{\text{SYNC}}$ tied Low), 32 or more LXT914s can be connected to the backplane and an external 10 MHz backplane clock source is required.
13	9	LOC/$\overline{\text{EXT}}$	I	**Management Mode Select.** This pin selects the management mode. When this pin is left floating, an internal pull-up defaults to the Local management mode (LOC/$\overline{\text{EXT}}$ High). In the Local mode, setup parameters are downloaded from an EEPROM during initialization. Once initialized with the setup parameters, the repeater functions independently.
28	33	LEDJM/ AUISEL	I/O	**LED Driver or DTE/MAU Select.** At reset, this pin selects the mode of the AUI port. If left floating, an internal pull-down device forces the AUI port to DTE mode. If pulled High with an external resistor, the port changes to a MAU, in which case the functions of the LEDJM pin are disabled and the default LED mode (Refer to Table 7) is not available.
—	30	AUISEL	I	**DTE/MAU Select.** This pin changes the mode of the AUI port independent of the condition at reset. This function is available only in the 100-pin PQFP package.
17 35	14 40	LEDM0 LEDM1	I/O I/O	**LED Mode 0 & 1 Select.** These two pins select one of four possible LED modes of operation. The Functional Description section describes the four modes.

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Table 4: LXT914 Serial Port Signal Descriptions (External Management Mode)

PLCC	PQFP	Symbol	I/O	Description
14	11	$\overline{\text{SENI}}$	I	**Serial Enable Input.** This active Low input is used to access the LXT914 serial interface. To write to the serial input (SDI), an External Management Device (EMD) must drive this pin from High to Low. The input must be asserted Low concurrent with the appearance of data on SDI and remain Low for the duration of the serial input transaction.
15	12	$\overline{\text{SENO}}$	O	**Serial Enable Output.** This active Low output is used to access the serial interface of an EMD. When the LXT914 sends a data stream to the EMD through the serial port (SDO), this output transitions from High to Low and remains Low for the duration of the serial transmission.
16	13	SDI	I	**Serial Data Input.** This pin is the input for the EMD serial interface. Setup and operating parameters are supplied to the LXT914 in a serial data stream through this port when operating in the External Management Mode.
17	14	SDO	I/O	**Serial Data Output.** After each packet transmission or interrupt event, the LXT914 reports status information to the EMD in a serial data stream through this port.
18	16	SCLK	I	**Serial Clock.** This 10 MHz clock synchronizes the serial interface between the LXT914 and the EMD. Both devices must be supplied from the same clock source. In synchronous mode, SCLK and BCLK may be tied together.

Table 5: LXT914 Serial Port Signal Descriptions (Local Management Mode)

PLCC	PQFP	Symbol	I/O	Description
14	11	CS	O	**Chip Select.** The LXT914 is designed for use with an EEPROM or similar device which may be used to store setup parameters and serially download them to the LXT914 during initialization. In a single-device application or in the first device of a daisy chain application, this pin is an active High Chip Select output used to enable the EEPROM.
		$\overline{\text{SENI}}$	I	**Serial Enable Input.** In subsequent devices of a daisy-chain configuration, a High-to-Low transition on this pin enables the serial input port (SDI). The input must be asserted concurrent with the appearance of data on SDI and remain Low for the duration of the serial input transaction.
15	12	$\overline{\text{SENO}}$	O	**Serial Enable Output.** During initialization, the LXT914 accepts 48 bits of setup data through the SDI port. After the 48th bit, the LXT914 asserts this pin Low. When multiple LXT914 devices are connected in a daisy-chain, this output is tied to the $\overline{\text{SENI}}$ input of the next device in the chain. Thus each device in the chain is serially enabled by the previous device until all the devices have read in their 48 bits of setup data.
16	13	SDI	I	**Setup Data Input.** This pin is the serial input port for the setup parameters (48 bits).This pin should be tied Low if no EEPROM is present.
17	14	RTS	I/O	**Request To Send.** In a single-device application or in the first device of a daisy chain application, this pin outputs a 9-bit, active High sequence. This pin must be tied to the EEPROM DI input to trigger the EEPROM to download its stored data. In subsequent devices this pin is not used.
18	16	SCLKIO	I/O	**Serial Clock.** A 1 MHz clock provided by the first LXT914 in the chain to all subsequent repeaters and the EEPROM. In the Local mode all repeaters have their SCLKIO pins tied together.

Table 6: LXT914 Miscellaneous Control Signal Descriptions

PLCC	PQFP	Symbol	I/O	Description
19	18	TEST	I	**Test Mode Select.** This pin must be tied Low for normal operation.
20	19	RESET	I	**RESET.** This pin resets the LXT914 circuitry when pulled High for ≥ 1 ms.
21	21	DSQE (Local)	I	**DSQE.** In Local Mode, this pin controls the SQE function. When High, the SQE function of the AUI port is disabled. When Low, SQE is enabled.
		SECTP1 (External)	I	**Security Mode Select (TP Port 1).** In External Mode, this pin enables the security mode for twisted-pair port 1. When pulled High, the LXT914 Jams the port. This pin must be tied Low if external security control is not required.
22 23 24	22 23 24	SECTP2 SECTP3 SECTP4 (External)	I I I	**Security Mode Select (TP Ports 2-4).** In External Mode, these pins enable the security mode for the respective twisted-pair ports (TP1 through TP4). When pulled High, the LXT914 jams the affected port. The SEC pins must be tied Low if external security control is not required.
25	25	FPS (Local)	I	**First Position Select.** In the Local mode this pin identifies the first device in a daisy chain configuration. When tied High (First position), the LXT914 controls the local EEPROM by providing clock and handshaking. When tied Low (Not First), the LXT914 will accept CLK and data in its turn from previous LXT914s in the data chain.
		SECAUI (External)	I	**Security Mode Select (AUI Port).** In the External mode this pin enables the security mode for the AUI port. When pulled High, the LXT914 jams the AUI port. The security feature is available only in External management mode.

Table 7: LXT914 LED Driver Signal Descriptions

PLCC	PQFP	Symbol	I/O	Description
27	32	LEDCF	O	**Collision & FIFO Error LED Driver.** This tri-state LED driver pin reports collisions and FIFO errors. It pulses Low to report collisions, and pulses High to report FIFO errors. When this pin is connected to the anode of one LED and to the cathode of a second LED, the LXT914 will simultaneously monitor and report both conditions independently.
28	33	LEDJM	O	**Jabber/MJLP & Manchester Code Violation LED Driver.** This tri-state LED driver pin reports jabber and code violations. It pulses Low to report MAU Jabber Lockup Protection (MJLP), and pulses High to report Manchester code violations. When this pin is connected to the anode of one LED and to the cathode of a second LED, the LXT914 will simultaneously monitor and report both conditions independently.
29 30 31 32	34 35 36 37	LEDTP1 LEDTP2 LEDTP3 LEDTP4	O O O O	**Twisted-Pair Port LED Drivers.** These tri-state LED drivers use an alternating pulsed output to report TP port status. Each pin should be tied to a pair of LEDs (to the anode of one LED and the cathode of a second LED). When connected this way, each pin reports five separate conditions (receive, transmit, link integrity, reverse polarity and auto partition).
33	38	LEDAUI	O	**AUI Port LED Driver.** This tri-state LED driver uses an alternating pulsed output to report AUI port status. This pin should be tied to a pair of LEDs (to the anode of one LED and the cathode of a second LED). When connected this way, this pin reports five separate conditions (receive, transmit, receive jabber, receive collision and auto partition.

Table 8: LXT914 Repeater Port Signal Descriptions

PLCC	PQFP	Symbol	I/O	Description
40	46	AUIDOP	O	**AUI Data Outputs (Positive and Negative).** These pins are the positive and negative data outputs for the AUI Port. In MAU Mode these pins are connected to the DI pins of the DTE.
41	47	AUIDON	O	
42	48	AUIDIP	I	**AUI Data Input (Positive and Negative).** These pins are the positive and negative data inputs for the AUI Port. In MAU Mode, these pins are connected to the DO pins of the DTE.
43	49	AUIDIN	I	
44	54	AUICIP	I/O	**AUI Collision (Positive and Negative).** These pins are the positive and negative Collision inputs for the AUI Port in DTE Mode. In MAU Mode, these pins output a collision indication to the DTE.
45	55	AUICIN	I/O	
56	71	TPDOP1	O	**Twisted-Pair Data Outputs (Positive and Negative).** These pins are the positive (TPDOP1-4) and negative (TPDON1-4) outputs to the network from the respective twisted-pair ports.
57	72	TPDON1	O	
54	68	TPDOP2	O	
53	67	TPDON2	O	
50	63	TPDOP3	O	
51	64	TPDON3	O	
48	60	TPDOP4	O	
47	59	TPDON4	O	
66	87	TPDIP1	I	**Twisted-Pair Data Inputs (Positive and Negative).** These pins are the positive (TPDIP1-4) and negative (TPDIN1-4) inputs from the network to the respective twisted-pair ports.
65	86	TPDIN1	I	
64	85	TPDIP2	I	
63	84	TPDIN2	I	
62	83	TPDIP3	I	
61	82	TPDIN3	I	
60	77	TPDIP4	I	
59	76	TPDIN4	I	

FUNCTIONAL DESCRIPTION

Introduction

The LXT914 is an integrated hub repeater for 10BASE-T networks. The hub repeater is the central point for information transfer across the network. The LXT914 offers multiple operating modes to suit a broad range of applications ranging from simple 4-port stand-alone hubs or attachments for print and file servers, up to intelligent 128-port enterprise systems with microprocessor/gate array management.

The main functions of the LXT914 hub repeater are data recovery and re-transmission and collision propagation. Data packets received at the AUI or 10BASE-T ports are detected and recovered by the port receivers before being passed to the repeater core circuitry for re-timing and re-transmission. Data packets received through the IRB port are essentially passed directly to the core for retransmission. After recovery of a valid data packet, the repeater broadcasts it to all enabled stations, except the originator station.

External Interfaces

The LXT914 includes four 10BASE-T ports with internal filters. The LXT914 also includes an Attachment Unit Interface (AUI) port, a serial port and an Inter-Repeater Backplane (IRB) port. The serial port allows an external device such as an EEPROM to download setup parameters to the repeater. In more complex designs the serial port can also be used to monitor repeater status. The IRB port enables multiple LXT914 devices to be cascaded, creating a large, multi-port repeater.

10BASE-T Ports

The four 10BASE-T transceiver ports are completely self-contained. Since the transmitters and receivers include the required filtering, only simple, inexpensive transformers are required to complete the 10BASE-T interface. Each individual Twisted-Pair (TP) port is implemented in accordance with the IEEE 802.3 10BASE-T standard.

AUI Port

The AUI port mode is selectable (DTE mode or MAU mode). With DTE mode selected, the AUI port allows connection of an external transceiver (10BASE2, 10BASE5, 10BASE-T or FOIRL) or a drop cable. With MAU mode selected, the AUI port establishes a MAU output allowing direct connection to another DTE interface.

Serial Port

The serial port provides the management interface to the LXT914. Refer to Test Specifications for serial port timing. The serial port can be either unidirectional or bidirectional, depending on the management mode selected. In the Local management mode the serial port is unidirectional (input only), and is used only to download setup parameters during initialization. The Local mode is intended for use with a simple EEPROM, but the serial port may be tied Low if an EEPROM is not required.

In the External management mode, the serial port is bi-directional (input for setup parameters, output for status reports). The External mode is intended for use with an External Management Device (EMD) and a Media Access Controller (MAC). The EMD (typically a gate array) communicates with a microprocessor (e.g., Intel 8051) and can control up to three LXT914 repeaters. This simplifies design of a relatively standard 12-port repeater on a single printed circuit board.

Inter-Repeater Backplane

The Inter-Repeater Backplane (IRB) allows several LXT914s to function as a single repeater. Refer to Test Specifications for IRB timing. The IRB also allows several multi-repeater boards to be integrated in a standard rack and to function as a single unit. The IRB supports "hot swapping" for easy maintenance and troubleshooting. Each individual repeater distributes recovered and re-timed data to other repeaters on the IRB for broadcast on all ports simultaneously. This simultaneous rebroadcast allows the multi-repeater system to act as a single large repeater unit. The maximum number of repeaters on the IRB is limited by bus loading factors such as parasitic capacitance. The IRB can be operated synchronously or asynchronously.

Synchronous IRB Operation

In the synchronous mode, a common external source provides the 10 MHz backplane clock (BCLKIO) and the 20 MHz system clock (SYSCLK) to all repeaters. BCLKIO must be synchronous to SYSCLK and may be derived from SYSCLK using a divide-by-two circuit. In the synchronous mode 32 or more LXT914 repeaters may be connected on the IRB, providing 128 10BASE-T ports and 32 AUI ports.

Asynchronous IRB Operation

In the asynchronous mode an external BCLKIO source is not required. The repeaters run independently until one takes control of the IRB. The transmitting repeater then outputs its own 10 MHz clock onto the BCLKIO line. All other repeaters sync to that clock for the duration of the transmission. In the asynchronous mode 12 or more LXT914 devices may be connected to the IRB, providing 48 10BASE-T ports and 12 AUI ports.

NOTE

The maximum number of repeaters which may be linked on the backplane is limited by board design factors. The numbers listed above are engineering estimates only. Stronger drivers and reduced capacitive loading in PCB layout may allow an increased device count.

Internal Repeater Circuitry

The basic repeater circuitry is shared among all the ports within the LXT914. It consists of a global repeater state machine, several timers and counters and the timing recovery circuit. The timing recovery circuit includes a FIFO for re-timing and recovery of the clock which is used to clock the receive data out onto the IRB.

The shared functional blocks of the LXT914 are controlled by the global state machine (Figure 2). This diagram and all associated notations used are in strict accordance with section 9.6 of the IEEE 802.3 standard.

The LXT914 also implements the Partition State Diagram as defined by the IEEE 802.3 standard and shown in Figure 3. The value of CCLimit as implemented in the LXT914 is 64.

The CCLimit value sets the number of consecutive collisions that must occur before the port is subjected to automatic partitioning. Auto-partition/re-connection is also supported by the LXT914 with Tw5 conforming to the standard requirement of 450 to 560 bit times.

Initialization

The following description applies to the initial power-on reset and to any subsequent hardware reset. When a reset occurs (RESET pin pulled High for > 1 ms), the device senses the levels at the various control pins (see Table 3) to determine the correct operating modes for Management, LEDs, and the AUI port functions.

Local Management Mode Initialization

An internal pull-up causes the LXT914 to default to the Local management mode unless the LOC/$\overline{\text{EXT}}$ pin is tied Low. In the Local mode the serial port is a unidirectional interface used only to download setup parameters from an external device.

In a Locally managed multiple-repeater (daisy chain) configuration, the first repeater in the chain performs special functions. The First Position Select (FPS) pin is used to establish position (FPS High = First, FPS Low = Not First). After establishing the Hardware mode, each LXT914 monitors the FPS pin to determine its position.

If FPS is High (First Position), the repeater performs the following functions:

1. Outputs a 1 MHz Serial Clock (SCLK). SCLK is derived from the 20 MHz SYSCLK input in ASYNC mode and from BCLKIO in SYNC mode; it is supplied to the SCLK inputs of all other repeaters on the bus and to the EEPROM.
2. Asserts Chip Select (CS) High to enable the EEPROM.
3. Outputs a serial 9-bit request-to-send (RTS) strobe. The programmable device responds to the RTS strobe with a serial data stream containing the setup parameters for all repeaters in the chain.
4. Clocks the first 48 serial data input (SDI) bits from the EEPROM into its setup register. Refer to Table 9 and Table 10 for Setup Register bit assignments.
5. Asserts Serial Enable Output ($\overline{\text{SENO}}$) Low to enable the next repeater in line.

The second repeater has FPS tied Low and Serial Enable Input ($\overline{\text{SENI}}$) connected to the Serial Enable Output ($\overline{\text{SENO}}$) of the first repeater. When enabled by a Low on $\overline{\text{SENI}}$, each repeater downloads its portion of the stream, then stops accepting data and asserts $\overline{\text{SENO}}$ Low. The $\overline{\text{SENO}}$ pin is linked to the $\overline{\text{SENI}}$ input of the next repeater. This enables the next repeater to clock in its 48-bit word and so on.

If FPS is Low (Not First Position), the repeater performs the following functions:

1. Syncs to the 1 MHz Serial Clock (SCLK) input. SCLK is supplied by the First Position repeater.
2. Responds to $\overline{\text{SENI}}$ Low by enabling the SDI port.
3. Clocks 48 bits from the EEPROM into its setup register through the SDI port.
4. Asserts $\overline{\text{SENO}}$ Low to enable the next repeater in line.

Figure 2: Global State Machine

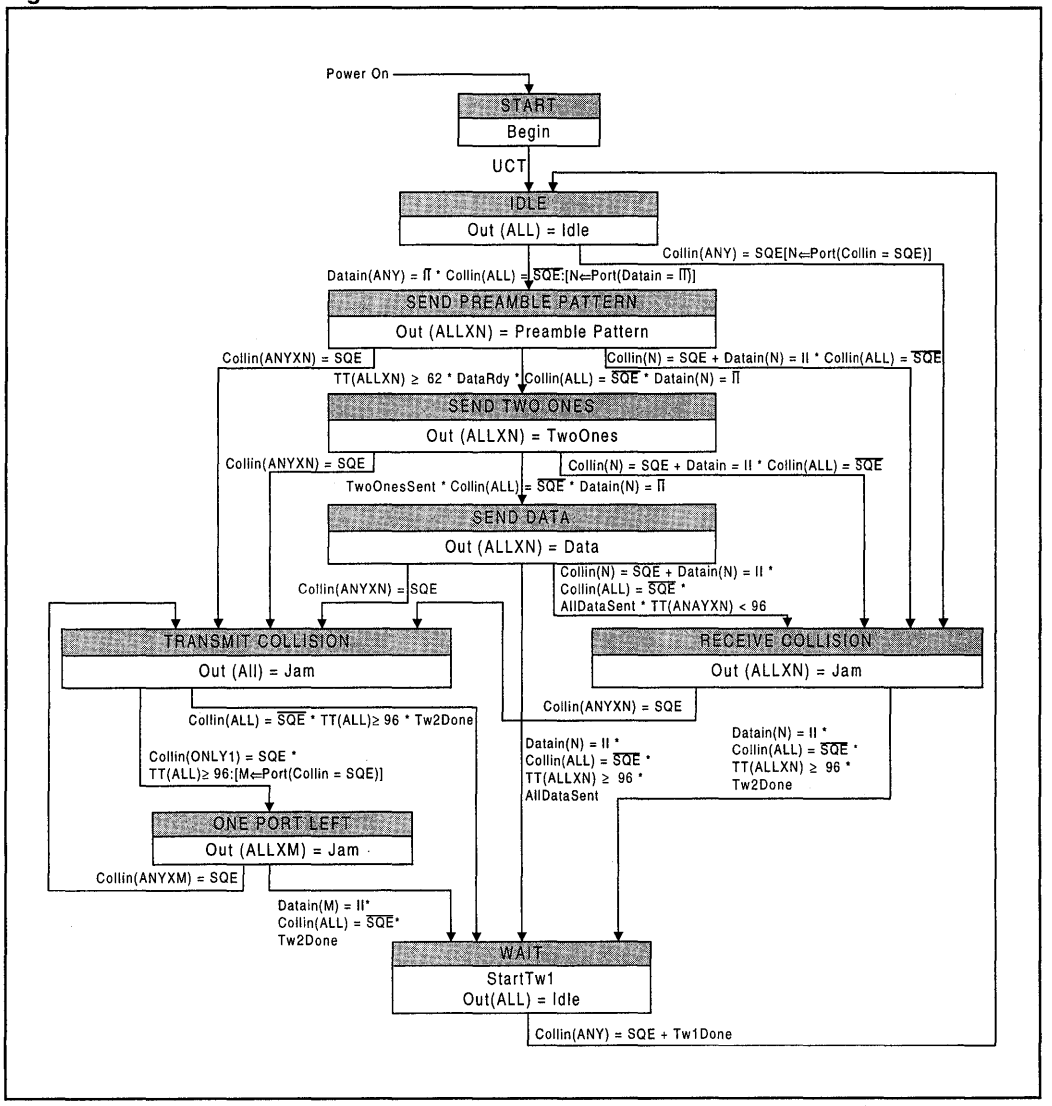

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Figure 3: Partitioning State Machine

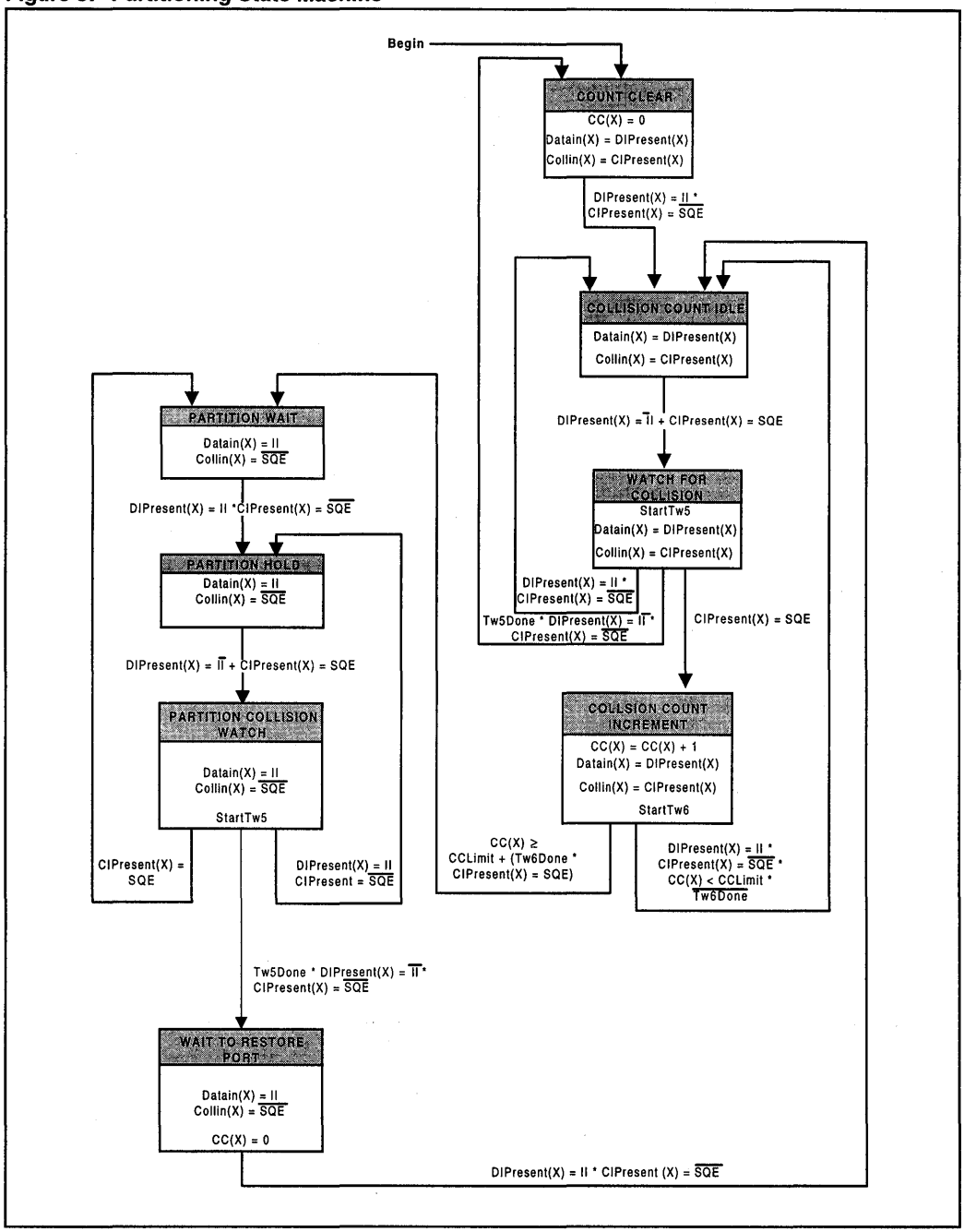


Table 9: Setup Register Bit Assignments

Register	D7	D6	D5	D4	D3	D2	D1	D0
SR(0)	DISLI3	DISLI2	DISLI1	DISAP4	DISAP3	DISAP2	DISAP1	DISAPA
SR(1)	DISTX2	DISTX1	DISTXA	DPRC4	DPRC3	DPRC2	DPRC1	DISLI4
SR(2)	ERSQ1	DISRX4	DISRX3	DISRX2	DISRX1	DISRXA	DISTX4	DISTX3
SR(3)	DFIFOE	DPFRM	DSQE	DMCV	ERXJAB	ERSQ4	ERSQ3	ERSQ2
SR(4)	RES	RES	RES	RES	RES	RES	RES	RES
SR(5)	RES	RES	RES	RES	RES	RES	RES	RES

Table 10: Setup Register Bit Definitions

Bit	Definition
DISAP*x*	1 = Disable Auto-Partitioning on Port *x*
DISLI*x*	1 = Disable Link Integrity on Port *x* (Twisted-pair ports only)
DPRC*x*	1 = Disable Polarity Reverse detection and Correction on Port *x* (Twisted-pair ports only)
DISTX*x*	1 = Disable Transmit on Port *x*
DISRX*x*	1 = Disable Receive on Port *x*
ERSQ*x*	1 = Enable Reduced Squelch on Port *x* (Twisted-pair ports only)
ERXJAB	1 = Enable Receive JAB (Long Packet) (Global)
DMCV	1 = Disable entering Tx Collision state on reception of Manchester Code Violation
DSQE	1 = Disable Signal Quality Error to provide heartbeat (AUI port only)
DPFRM	1 = Disable End-of-Frame checking for polarity correction (Global)
DFIFOE	1 = Disable entering Tx Collision state on FIFO over/underflow condition (Global)
DMJLP	1 = Disable MJLP counter (Global)
RES	*Reserved. Must be set to 0.*

External Management Mode Initialization

The LXT914 operates in the External management mode when the LOC/$\overline{EXT}$ pin is tied Low. In the External mode, the serial port is a bidirectional interface between the LXT914 and an external management device (EMD). The serial port is used to download initial setup parameters to the repeater and to monitor status reports from the repeater. The LXT914 setup parameters can be changed at any time by the EMD. The initialization process for each repeater in a managed mode configuration is the same, regardless of its position; each repeater is connected directly to the EMD. Each LXT914 initializes as follows:

1. Syncs to the 10 MHz Serial Clock (SCLK) input. SCLK must be supplied from an external source.
2. Responds to $\overline{SENI}$ Low by enabling the SDI port.
3. Clocks 48 bits from the EMD into its setup register through the SDI port.
4. Once initialized, the LXT914 reports its status in a 48-bit serial stream after every packet transmission or interrupt event. Refer to Table 11 and Table 12 for packet status register bit assignments and definitions.

Table 11: Packet Status Register Bit Definitions

Register	D7	D6	D5	D4	D3	D2	D1	D0
PSR(0)	COL2	COL1	COLA	RX4	RX3	RX2	RX1	RXA
PSR(1)	PR2	PR1	LLS4	LLS3	LLS2	LLS1	COL4	COL3
PSR(2)	SPA	AP4	AP3	AP2	AP1	APA	PR4	PR3
PSR(3)	LP3	LP2	LP1	LPA	SP4	SP3	SP2	SP1
PSR(4)	RXJABA	MJLP	LCOL4	LCOL3	LCOL2	LCOL1	LCOLA	LP4
PSR(5)	RES	RXCOL	MANCV	FIFOER	RXJAB4	RXJAB3	RXJAB2	RXJAB1

Table 12: Packet Status Register Bit Definitions

Bit[1]	Definition
RX*x*	Received Packet on Twisted-Pair Port 1-4 or on AUI Port
COL*x*	Transmit Collision of Twisted -Pair Port 1-4 or on AUI Port
LLSC*x*	Link Loss State on Twisted-Pair Port 1-4 or on AUI Port
PR*x*	Polarity reversed on Twisted-Pair Port 1-4 or on AUI Port
AP*x*	Auto-Partition circuit isolated Twisted-Pair Port 1-4 or the AUI Port
SP*x*	Short Packet (less than 74 bits) on Twisted-Pair Port 1-4 or on AUI Port
LP*x*	Long Packet (more than 1.3 ms) on Twisted-Pair Port 1-4 or on AUI Port
LCOL*x*	Late Collision on Twisted-Pair Port 1-4 or on AUI Port
MJLP	MAU Jabber Lockup Protection
RXJAB*x*	Receive Jabber Lockup Protection
FIFOER	FIFO overflow/underflow
MANCV	Manchester Code Violation
RXCOL	Receive Collision on the AUI Port
RES	*Reserved. Not used*

1. The notation ABCD*x* means bit ABCD associated with port *x*, which can be any of the four Twisted-Pair Ports or the AUI Port.

10BASE-T Port Operation

10BASE-T Reception

Each LXT914 10BASE-T port receiver acquires data packets from its twisted-pair input (TPDIP/TPDIN). An internal RC filter and an intelligent squelch function discriminate noise from link test pulses and valid data streams. The receive function is activated only by valid data streams (above the squelch level and with proper timing). If the differential signal at the DI circuit inputs falls below 75% of the threshold level (unsquelched) for eight bit times (typical), the port receiver enters the idle state.

Programmable Internal Squelch Level

The 10BASE-T port receivers have two squelch levels: a normal level or default setting and a reduced level squelch (-4.5 dB) selected when the ERSQx is set in the Setup register. When used with Low noise media such as shielded twisted-pair cabling, the reduced squelch level allows longer loop lengths in the network.

Polarity Detection and Correction

The LXT914 10BASE-T ports detect and correct for reversed polarity by monitoring link pulses and end-of-frame sequences. A reversed polarity condition is declared when the port receives sixteen or more incorrect link pulses consecutively, or four frames with reversed start-of-idle sequence. In these cases the receiver reverses the polarity of the signal and thereby corrects for this failure condition. If the port enters the link fail state and no valid data or link pulses are received within 96 to 128 ms, the polarity is reset to the default non-flipped condition. (If Link Integrity Testing is disabled, polarity detection is based only on received data.)

10BASE-T Transmission

Each LXT914 10BASE-T port receives NRZ data from the repeater core and passes it through a Manchester encoder. The encoded data is then transmitted to the twisted-pair network (the DO circuit). The advanced integrated pulse shaping and filtering network produces the pre-distorted and pre-filtered output signal to meet the 10BASE-T jitter template. An internal continuous resistor-capacitor filter is used to remove any high-frequency clocking noise from the pulse shaping circuitry. Integrated filters simplify the design work required for FCC compliant EMI performance. During idle periods, the LXT914 10BASE-T ports transmit link integrity test pulses in accordance with the 802.3 10BASE-T standard.

Data packets transmitted by the LXT914 contain a minimum of 56 preamble bits before the start of frame delimiter (SFD). In the Asynchronous mode, preamble regeneration takes place on the transmit side. In the Synchronous mode, the preamble is regenerated on the receive side and distributed via the IRB. If the total packet is less than 96 bits including the preamble, the LXT914 extends the packet length to 96 bits by appending a Jam signal (1010...) at the end.

10BASE-T Link Integrity Testing

The LXT914 fully supports the 10BASE-T Link Integrity test function. The link integrity test determines the status of the receive side twisted-pair cable. Link integrity testing is enabled unless disabled via the DISLIx bit in the Setup register. When enabled, the receiver recognizes link integrity pulses transmitted in the absence of data traffic. With no data packets or link integrity pulses within 100 (±50) ms, the port enters a link fail state and disables its transmitter. The port remains in the link fail state until it detects three or more data packets or link integrity pulses.

AUI Port Operation

AUI Reception

The LXT914 AUI port receiver acquires data packets from the network (AUIDIP/AUIDIN). Only valid data streams above the squelch level activate the receive function. If the differential signal at the DI circuit inputs falls below 75% of the threshold level (unsquelched) for 8 bit times (typical), the AUI receiver enters the idle state.

AUI Transmission

The LXT914 AUI port receives NRZ data from the repeater core, and passes it through a Manchester encoder. The encoded data then goes out on the network (AUIDOP/AUIDON).

AUI Mode Selection (DTE/MAU)

The LXT914 allows the user to change the mode of the AUI from a DTE to a MAU interface. This option is available on both 68- and 100-pin versions except as follows:

- When using the LEDJM/AUISEL pin to select the AUI interface mode the following is true: After reset the state of the LEDJM/AUISEL pin is sensed for the correct mode. The LEDJM/AUISEL pin when floated or pulled Low will select the DTE interface and the LEDJM/AUISEL output is still available. When the LEDJM/AUISEL pin is pulled High the MAU interface is selected and the LEDJM/AUISEL function is unavailable.
- The 100-pin PQFP has an additional pin, AUISEL (pin 30). When using this pin to select the AUI interface mode the LEDJM/AUISEL pin is still a functional LED driver. The AUISEL pin is not latched after reset and is actively polled to determine which AUI interface mode is to be used. Refer to Table 13.

Table 13: AUI Mode Selection (DTE/MAU)

App #	AUISEL (PQFP only)	LEDJM/ AUISEL (both pkgs)	AUI Mode	Available LED Modes
1	Low	Low	DTE	default, 0-3
2	Low	High	MAU	1-3
3[1]	High	Low	MAU	default, 0-3
4	High	High	MAU	1-3

1. Application 3 is valid only when using the 100-pin PQFP.

Collision Handling

A collision occurs when two or more repeater ports receive simultaneously, or when the AUI CIP/CIN signal is active. The LXT914 fully complies with the IEEE 802.3 collision specifications, both in individual and multi-repeater applications. In multiple-repeater configurations, collision signaling on the IRB allows all repeaters to share collision parameters, acting as a single large repeater.

$\overline{\text{IRCOL}}$ is a digital open-drain pin. $\overline{\text{IRCFS}}$ is an analog/digital port. The $\overline{\text{IRCOL}}$ and $\overline{\text{IRCFS}}$ lines are pulled up globally (*i.e.*, each signal requires one pull-up resistor for all boards). If there are eight 3-repeater boards in the system, all eight boards share a single pull-up resistor for $\overline{\text{IRCOL}}$ and a single pull-up resistor for $\overline{\text{IRCFS}}$. The global pull-up may be located on one of the boards, or on the backplane. The $\overline{\text{IRCFS}}$ line requires a precision (± 1%) resistor.

The $\overline{\text{IRENA}}$, IRDAT and $\overline{\text{IRDEN}}$ lines are each pulled up locally (one pull-up resistor per board) if external bus drivers are used. If no bus drivers are used then only one global pull-up per signal is used.

Security Mode

The LXT914 security mode is fully transparent to the user. In the External management mode, the security feature is available for all four TP ports and the AUI port. In the Local mode, security is available for the TP ports only (the SECAUI input is reassigned as FPS). The security inputs are normally held Low to disable the security feature. Any input can independently be pulled High to scramble the respective port for any given length of time. For applications which do not require security control, the SEC pins must be tied Low.

The security mode pins are real time response inputs. This allows the board designer to screen the destination address with an application specific device and (on match of the destination address) to assert the security input to jam the respective port for the given frame. This real time detection and jam assertion method provides the flexibility to implement customer specific solutions. The destination address decoding and security signal assertion functions can be integrated into the external management device.

LED Display

The LED display interface consists of seven integrated LED drivers, one for each of the five network ports and two for common functions. Each pin provides a three-state pulsed output (+5 V, high Z, and 0 V) which allows multiple conditions to be monitored and reported independently. Table 14 shows the LED Mode selected with each LEDM1 and LEDM0 combination. Figure 4 shows the LED Driver output conditions, and Tables 15 through 18 list the repeater states associated with each of the five conditions.

NOTE

If LED mode 0 is selected and the LEDJM/ AUISEL pin is High (which selects MAU Mode), the device defaults to LED Mode 1. LED Mode 0 is not available when LEDJM/AUISEL is pulled High.

Table 14: LED Mode Selection

	LEDM1	LEDM0	LED Mode Selected
PLCC pin	35	17	
PQFP pin	40	14	
	Low	Low	0 (default)[1]
	Low	High	1
	High	Low	2
	High	High	3

1. This mode is not available when using the LEDJM/AUISEL pin to select a MAU interface in the AUI port. In this case, the LED Mode defaults to LED Mode 1.

LED Mode 0 (Default). This mode is selected when LEDM1 and LEDM0 are floating or pulled Low. Refer to Table 15. This mode is not available when using the LEDJM/AUISEL pin to select a MAU interface in the AUI port. In this case, the LED Mode defaults to Mode 1.

LED Mode 1. This mode is selected when LEDM1 is floating or pulled Low and LEDM0 is pulled High by a pull-up resistor. Refer to Table 16.

LED Mode 2. This mode is selected when LEDM1 is pulled High by a pull-up resistor and LEDM0 is floating or pulled Low. Refer to Table 17.

LED Mode 3. This mode is selected when LEDM1 is pulled High by a pull-up resistor and LEDM0 is also pulled High by a pull-up resistor. Refer to Table 18.

Table 15: Mode 0 (Default) LED Truth Table

Condition	LEDTP 1-4	LEDAUI	LEDCF	LEDJM
1	Rx Link Pulse	N/A	FIFO Error	Manchester Code Violation
2	Tx Packet	Tx Packet	N/A	N/A
3	Reversed Polarity	N/A	Collision	MAU Jabber Lockup Protection (MJLP)
4	Rx Packet	Rx Packet	N/A	N/A
5	Partitioned Out	Partitioned Out	N/A	N/A

Table 16: Mode 1 LED Truth Table

Condition	LEDTP 1-4	LEDAUI	LEDCF	LEDJM
1	Rx Link Pulse	N/A	MAU Jabber Lockup Protection (MJLP)	N/A
2	N/A	N/A	N/A	N/A
3	N/A	N/A	Collision	N/A
4	Rx Packet	Rx Packet	N/A	N/A
5	N/A	N/A	N/A	N/A

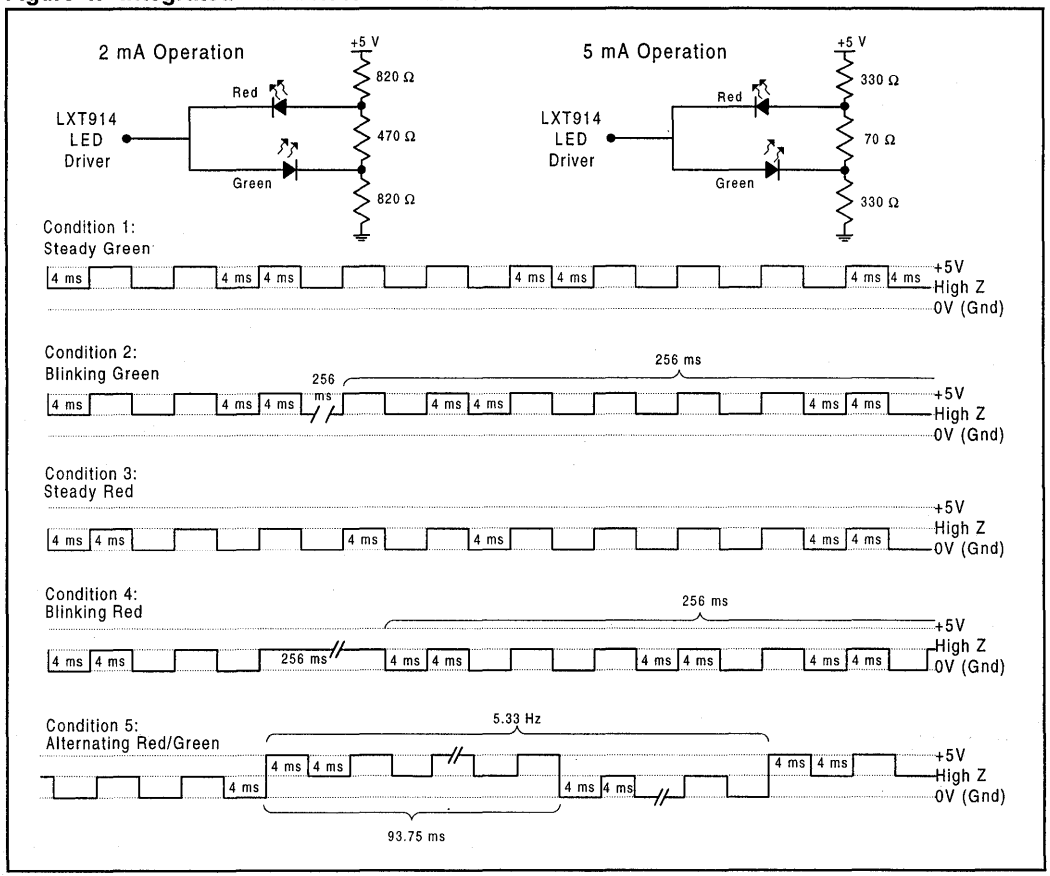
Table 17: Mode 2 LED Truth Table

Condition	LEDTP 1-4	LEDAUI	LEDCF	LEDJM
1	Rx Link Pulse	N/A	MAU Jabber Lockup Protection (MJLP)	N/A
2	Partitioned Out	Partitioned Out	N/A	N/A
3	N/A	N/A	Collision	N/A
4	Rx Packet	Rx Packet	N/A	N/A
5	N/A	N/A	N/A	N/A

Table 18: Mode 3 LED Truth Table

Condition	LEDTP 1-4	LEDAUI	LEDCF	LEDJM
1	Rx Link Pulse	N/A	MAU Jabber Lockup Protection (MJLP)	N/A
2	Rx Packet	Rx Packet	N/A	N/A
3	Partitioned Out	Partitioned Out	Collision	N/A
4	N/A	N/A	N/A	N/A
5	N/A	N/A	N/A	N/A

Figure 4: Integrated LED Driver Indications



APPLICATION INFORMATION

12-Port Hub Repeater

Figure 5 (Sheets 1 through 4) shows a simple 12-port hub repeater application with 3 LXT914s. This application also provides two additional AUI ports—one DB-15 connector and one coaxial port. The application shown uses the asynchronous backplane mode so no external backplane clock source is required.

Figure 5 (Sheet 1) shows the XL93C46 EEPROM which downloads the setup parameters for all the LXT914 devices at initialization. (This EEPROM could be replaced with a simple pull down resistor on the SDI pin. This will select the default conditions of the set up register.) A single 20 MHz crystal provides the SYSCLK for all three LXT914 chips. The LXT914 hub repeater on Sheet 1 provides the AUI DB-15 connector as well as four twisted-pair ports. Table 19 lists transformers suggested for use with the LXT914.

Figure 5 (Sheet 2) shows a second LXT914 hub repeater with four TP ports and a coaxial port. The MD-001 coax transceiver is used to implement the port. Sheet 3 shows the third LXT914 device with its four TP ports and indicator LEDs. The AUI port of the third LXT914 hub repeater is not used. Sheet 4 of the schematic shows the LEDs for the remaining LXT914 devices, along with the LED operation table.

8-Port Print or File Server

Figure 6 (Sheets 1 and 2) shows an eight-port repeater attachment for an existing single port AUI or 10BASE5 interface. This application can be added to a current design with an existing AUI or 10BASE5 interface. This circuit allows increased connectivity without the need for another external remote hub. The application shown is a 68-pin PLCC, an asynchronous backplane with both LXT914s in the first position.

In Figure 6 (Sheet 1) the LXT914 is set up with the LEDs in Mode 1 with one LED per port and a single collision LED. The twisted pair port LEDs display link integrity only. (Refer to Table 16.) LED Mode 1 is selected by pulling LEDM0 High with a 1 kΩ resistor on pin 17 and pulling LEDM1 Low with pin 35 attached to ground.

Figure 6 (Sheet 2) has the same configuration, mode of operation and LED Mode as used in Sheet 1. However, the AUI port has been configured as a MAU interface. This is selected when LEDJM/AUISEL on pin 28 is pulled up through a 1 kΩ resistor. This mode disables the LEDJM pin as an LED driver. (See Table 13.) The MAU interface now configured on the LXT914 allows the AUI port to attach to a DTE interface. This application increases connectivity to any existing single-port Ethernet design. This unique application allows the designer to integrate an external hub, eliminating the need for additional external equipment.

Table 19: Manufacturers Magnetics List

Manufacturer	Quad Transmit	Quad Receive	Tx/Rx Pairs
Bell Fuse	S553-5999-02	S553-5999-03	
Fil-Mag	23Z339	23Z338	
HALO	TD54-1006L1 TG54-1006N2	TD01-1006L1 TG01-1006N2	TD42-2006Q; TD43-2006K; TG42-1406N1 TG43-1406N
(Octal)			TG44-S010NX
Kappa	TP4003P	TP497P101	
Nanopulse	5976	5977	
PCA	EPE6009	EPE6010	
Pulse Eng.	PE68810	PE68820	PE65745; PE65994; PE65746; PE65998
VALOR	PT4116	PT4117	PT4069N1; PT4068N1; ST7011S2; ST7010S2

Figure 5: 12-Port Application Schematic, 68-Pin PLCC Package (Sheet 1 of 4)

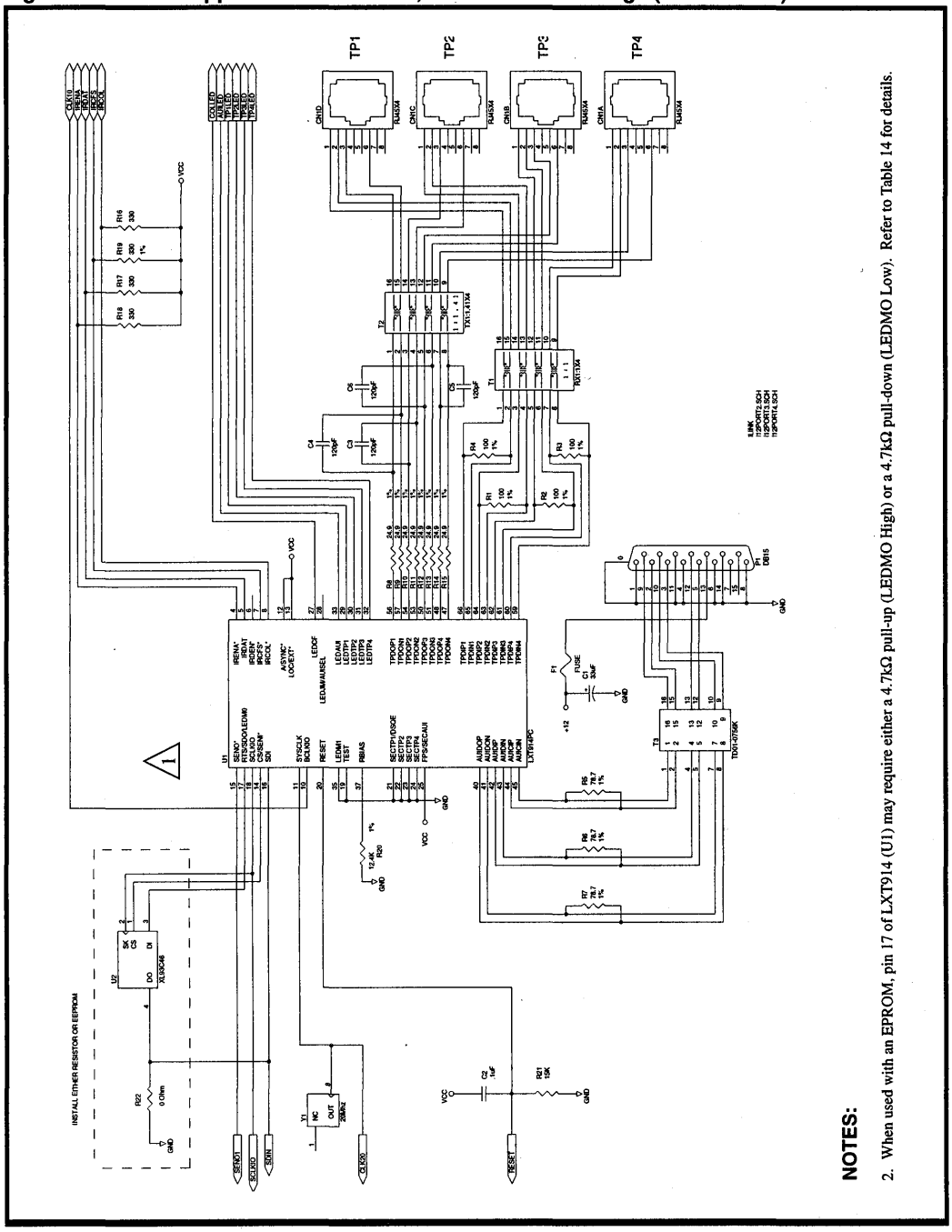


Figure 5: 12-Port Application Schematic, 68-Pin PLCC Package (Sheet 2 of 4)

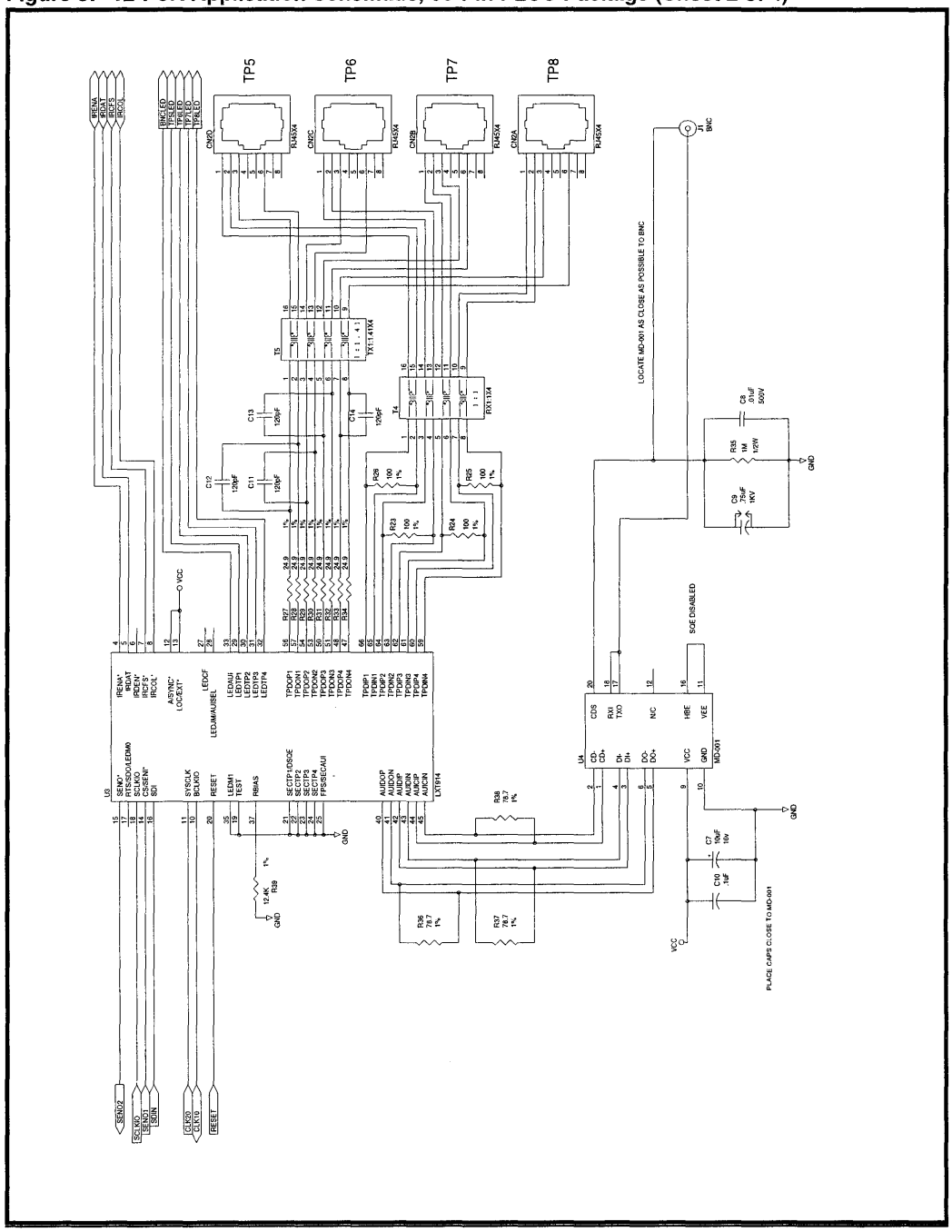


Figure 5: 12-Port Application Schematic, 68-Pin PLCC Package (Sheet 3 of 4)

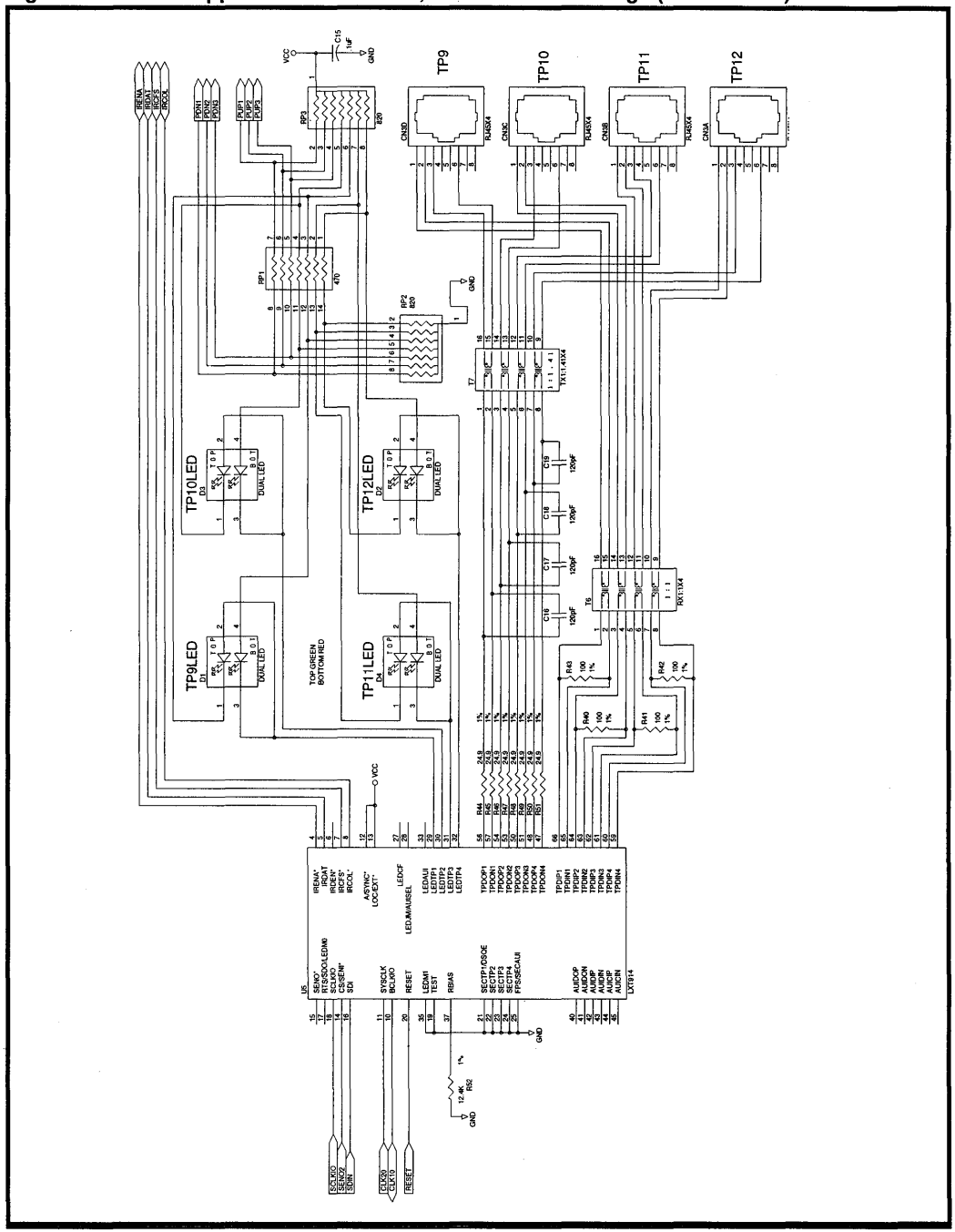


Figure 5: 12-Port Application Schematic, 68-Pin PLCC Package (Sheet 4 of 4)

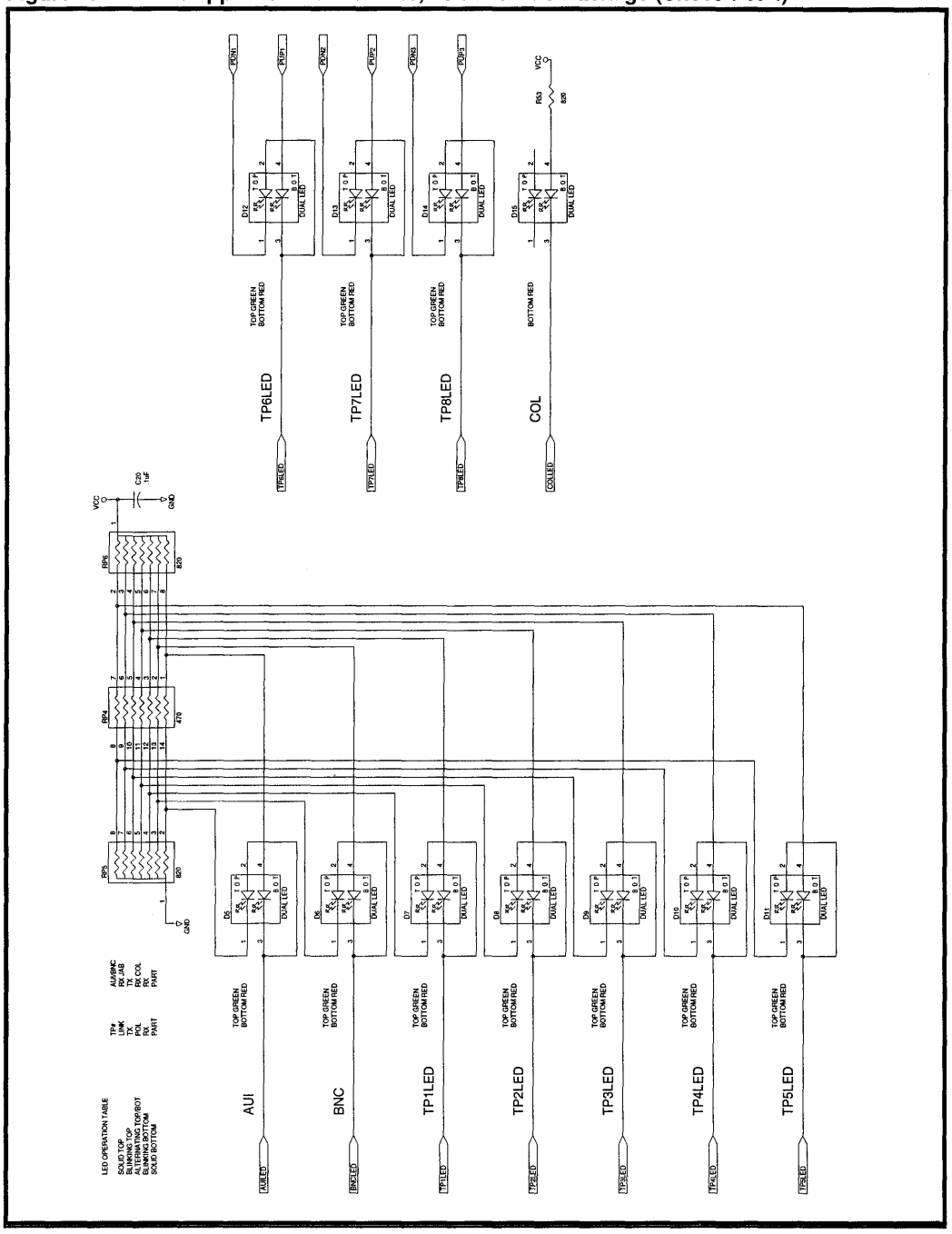


Figure 6: 8-Port Application Schematic, LED Mode 1 with AUISEL = MAU (Sheet 1 of 2)

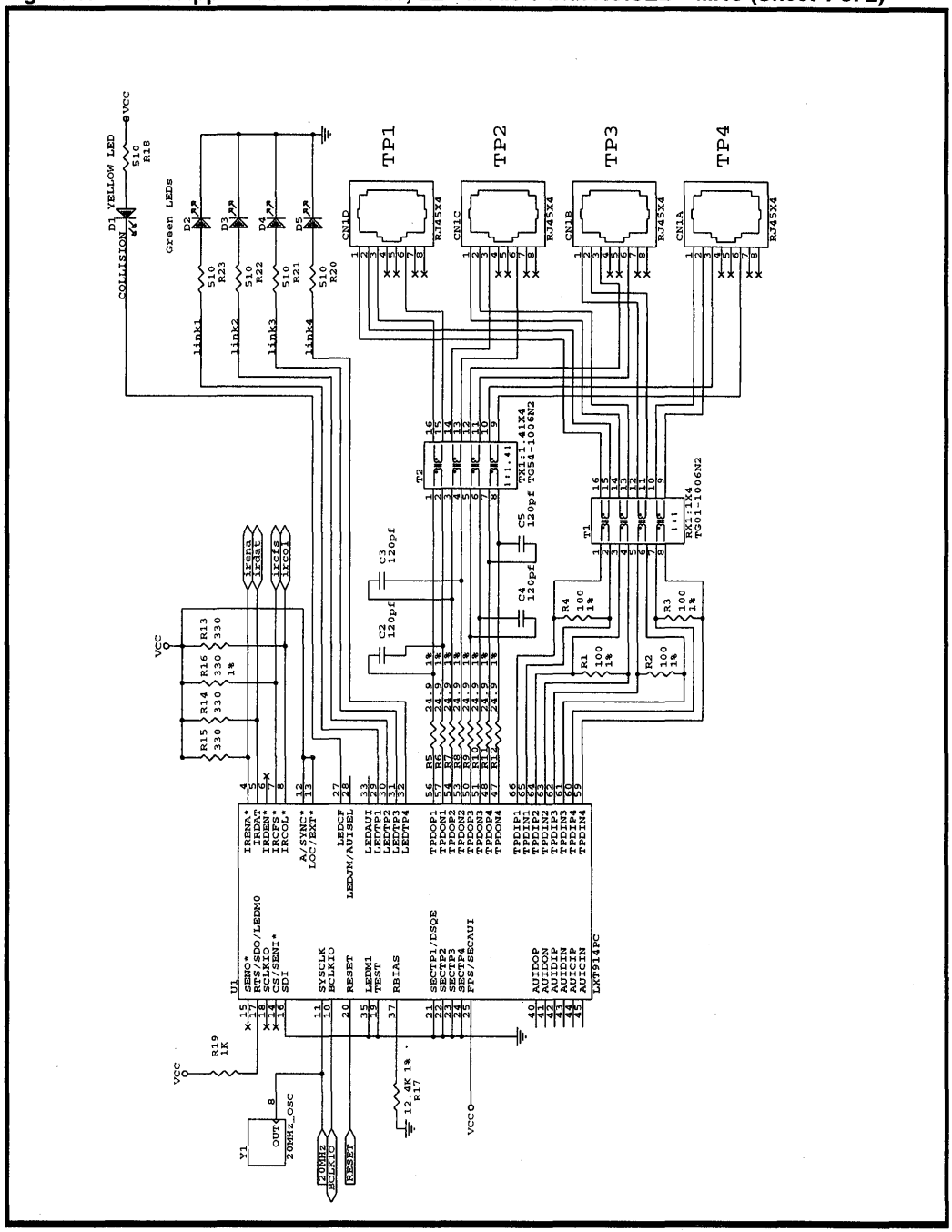
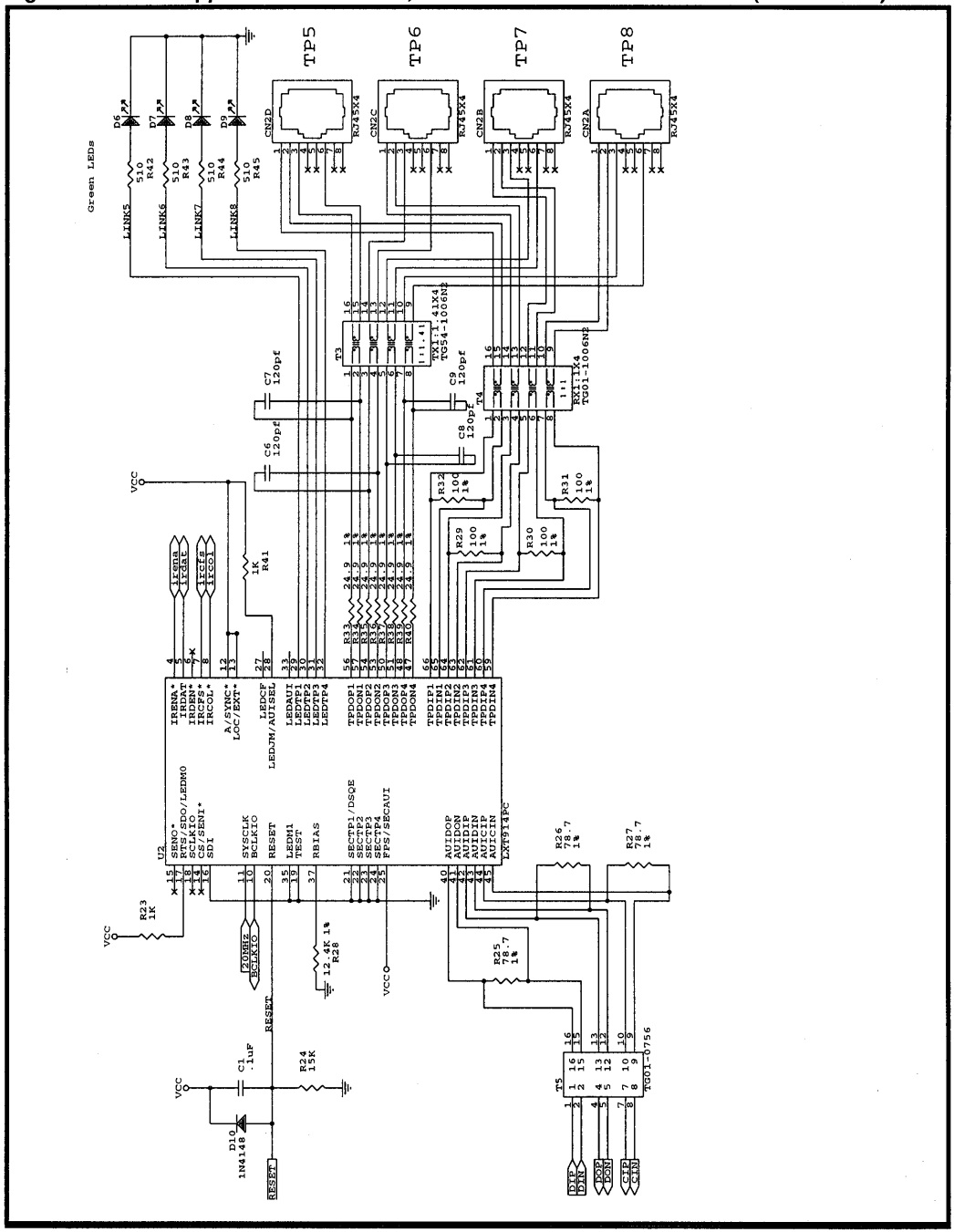


Figure 6: 8-Port Application Schematic, LED Mode 1 with AUISEL = MAU (Sheet 2 of 2)



TEST SPECIFICATIONS

NOTE

Minimum and maximum values in Tables 20 through 28, and Figures 7 and 8 represent the performance specifications of the LXT914 and are guaranteed by test except, where noted, by design.

Table 20: Absolute Maximum Ratings

Parameter		Symbol	Min	Typ	Max	Units
Supply voltage		VCC	-0.3	–	6	V
Operating temperature	LXT914PC/QC	TOP	0	–	+70	° C
	LXT914PE	TOP	-40	–	+85	° C
Storage temperature		TST	-65	–	+150	° C

CAUTION

Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 21: Recommended Operating Conditions

Parameter		Symbol	Min	Typ	Max	Units
Recommended supply voltage		VCC	4.75	5.0	5.25	V
Recommended operating temperature	LXT914PC/QC	TOP	0	–	+70	° C
	LXT914PE	TOP	-40	–	+85	° C

Table 22: I/O Electrical Characteristics[1] (over recommended range)

Parameter	Symbol	Min	Typ[2]	Max	Units	Test Conditions
Supply current	ICC	–	–	180	mA	
Input Low voltage	VIL	–	–	0.8	V	
Input Low voltage (RESET)	VILRESET	–	–	0.8	V	VCC = 5.25 V
Input High voltage	VIH	2.0	–	–	V	
Input High voltage (RESET)	VIHRESET	4.0	–	–	V	VCC = 4.75 V
Output Low voltage	VOL	–	–	0.4	V	IOL = 1.6 mA
Output Low voltage	VOL	–	–	10	% V_{CC}	IOL < 10 µA
Output Low voltage (LED)	VOLL	–	–	1.0	V	IOLL = 5 mA
Output High voltage	VOH	2.4	–	–	V	IOH = 40 µA
Output High voltage	VOH	90	–	–	% V_{CC}	IOH < 10 µA
Output High voltage (LED)	VOHL	4	–	–	V	IOHL = -5 mA
Input Low current	IIL	–	–	2	mA	VOL = .4 V
Output rise / fall time	–	–	3	8	ns	CLOAD = 20 pF
RESET pulse width	PWRESET	1.0	–	–	ms	VCC = 4.75 V
RESET fall time	TFRESET	–	–	20.0	µs	VIHRESET to VILRESET

1. Not applicable to IRB signals. IRB electrical characteristics are specified in Table 25.
2. Typical values are at 25° C and are for design aid only; they are not guaranteed and not subject to production testing.

Table 23: AUI Electrical Characteristics (over recommended range)

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Input Low current	IIL	–	–	-700	µA	
Input High current	IIH	–	–	500	µA	
Differential output voltage	VOD	±550	–	±1200	mV	
Receive input impedance	ZIN	–	20	–	kΩ	Between CIP/CIN & DIP/DIN
Differential squelch threshold	VDS	–	220	–	mV	

1. Typical values are at 25° C and are for design aid only; they are not guaranteed and not subject to production testing.

Table 24: Twisted-Pair Electrical Characteristics (over recommended range)

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Transmit output impedance	ZOUT	–	5	–	Ω	
Peak differential output voltage	VOD	3.3	3.5	3.7	V	Load = 100 Ω at TPOP and TPON
Transmit timing jitter addition	–	–	± 6.4	± 10	ns	0 line length
Transmit timing jitter added by the MAU and PLS sections[2]	–	–	± 3.5	± 5.5	ns	After line model specified by IEEE 802.3 for 10BASE-T
Receive input impedance	ZIN	–	20	–	kΩ	Between TPIP/TPIN
Differential squelch threshold (Normal threshold: ERSQ*x* = 0)	VDS	300	420	565	mV	5 MHz square wave input
Differential squelch threshold (Reduced threshold: ERSQ*x* = 1)	VDSL	180	250	345	mV	5 MHz square wave input

1. Typical values are at 25° C and are for design aid only; they are not guaranteed and not subject to production testing.
2. IEEE 802.3 specifies maximum jitter additions at 1.5 ns for the AUI cable, 0.5 ns from the encoder, and 3.5 ns from the MAU.

Table 25: IRB Electrical Characteristics (over recommended range)

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Output Low voltage	VOL	–	.3	.6	V	
Output rise or fall time	TF	–	4	12	ns	
Input Low voltage: $\overline{\text{IRENA}}$, $\overline{\text{IRCOL}}$ & IRDAT	VILIRB	–	–	0.8	V	RL = 330 Ω
Input High voltage: $\overline{\text{IRENA}}$, $\overline{\text{IRCOL}}$ & IRDAT	VIHIRB	3.0	–	–	V	RL = 330 Ω
Input Low voltage: BCLKIO	VILBCLK	–	–	0.4	V	RL = 330 Ω
Input High voltage: BCLKIO	VIHBCLK	4.0	–	–	V	RL = 330 Ω

1. Typical values are at 25° C and are for design aid only; they are not guaranteed and not subject to production testing.

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Table 26: Switching Characteristics (over recommended range)

Parameter		Min	Typ[1]	Max	Units
Jabber Timing	Maximum transmit time	5.0	–	5.5	ms
	Unjab time	–	9.6	–	µs
Link Integrity Timing	Time link loss	–	60	–	ms
	Time between Link Integrity Pulses	10	–	20	ms
	Interval for valid receive Link Integrity Pulses	4.1	–	30	ms

1. Typical values are at 25° C and are for design aid only; they are not guaranteed and not subject to production testing.

Table 27: Serial Port Timing - External Mode (over recommended range)

Parameter	Symbol	Minimum	Typical[1]	Maximum	Units
SCLKIO High to $\overline{\text{SENI}}$ Low (active)	tS1	0	–	50	ns
SCLKIO High to SDIN data valid	tS2	0	–	50	ns
SCLKIO High to $\overline{\text{SENO}}$ Low (active)	tS3	5	–	15	ns
SCLKIO Low to SDOUT data valid	tS4	5	–	15	ns

1. Typical values are at 25° C and are for design aid only; they are not guaranteed and not subject to production testing.

Figure 7: Serial Port Timing

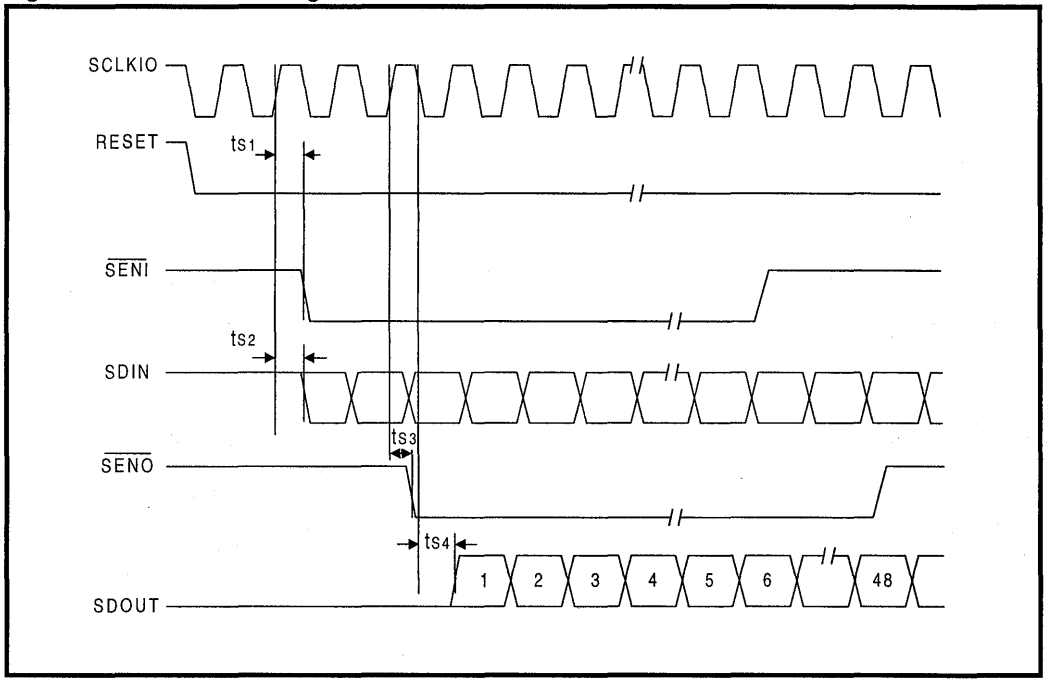
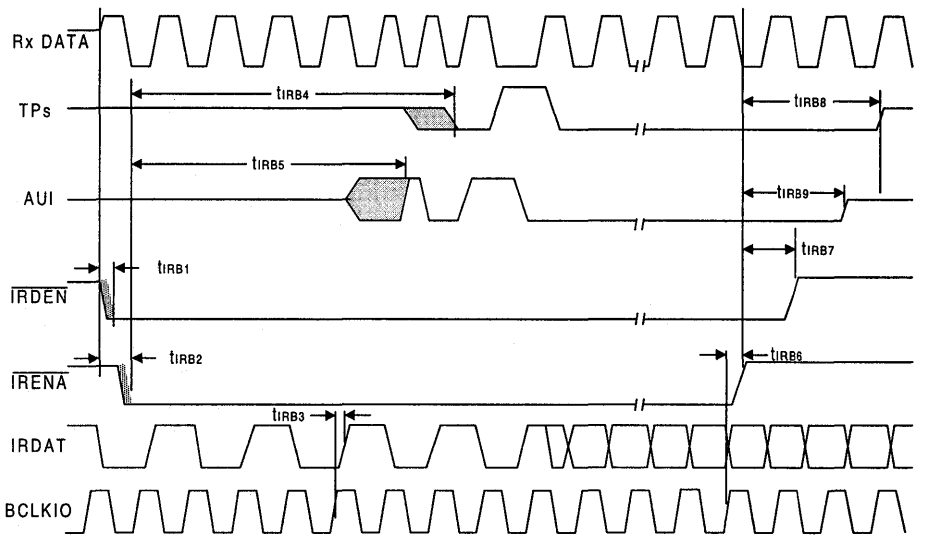


Table 28: Inter-Repeater Bus Timing (over recommended range)

Parameter	Symbol	Minimum	Typical[1]	Maximum	Units
Start of Frame to $\overline{\text{IRDEN}}$ Low (active)	tIRB1	10	–	150	ns
Start of Frame to $\overline{\text{IRENA}}$ Low (active)	tIRB2	125	–	225	ns
BCLKIO to IRDAT valid (Synchronous mode)	tIRB3	5	–	30	ns
BCLKIO to IRDAT valid (Asynchronous mode)	tIRB3	–	50	–	ns
$\overline{\text{IRENA}}$ Low (active) to TP outputs active	tIRB4	525	–	600	ns
$\overline{\text{IRENA}}$ Low (active) to AUI output active	tIRB5	475	–	525	ns
End of Frame clock to $\overline{\text{IRENA}}$ High (inactive)	tIRB6	5	–	30	ns
$\overline{\text{IRENA}}$ High (inactive) to $\overline{\text{IRDEN}}$ High (inactive)	tIRB7	95	–	105	ns
$\overline{\text{IRENA}}$ High (inactive) to TP outputs inactive	tIRB8	575	–	600	ns
$\overline{\text{IRENA}}$ High (inactive) to AUI output inactive	tIRB9	425	–	450	ns

1. Typical values are at 25° C and are for design aid only; they are not guaranteed and not subject to production testing.

Figure 8: Inter-Repeater Bus Timing



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NOTES

APRIL 1997
Revision 2.0

LXT915

Simple Quad Ethernet Repeater

General Description

The LXT915 is an integrated multi-port repeater designed for mixed-media networks. It provides all the active circuitry required for the repeater function in a single CMOS device. It includes one Attachment Unit Interface (AUI) port and four 10BASE-T transceivers. The AUI port allows connection of an external transceiver (10BASE-2, 10BASE-5, 10BASE-T or FOIRL) or a drop cable. The 10BASE-T transceivers are entirely self-contained with internal filters which simplify the design work required for FCC-compliant EMI performance.

An Inter-Repeater Backplane (IRB) interface allows 128 or more 10BASE-T ports to be cascaded, creating a large single-segment multi-port repeater.

The LXT915 requires only a single 5-volt power supply due to its advanced CMOS fabrication process.

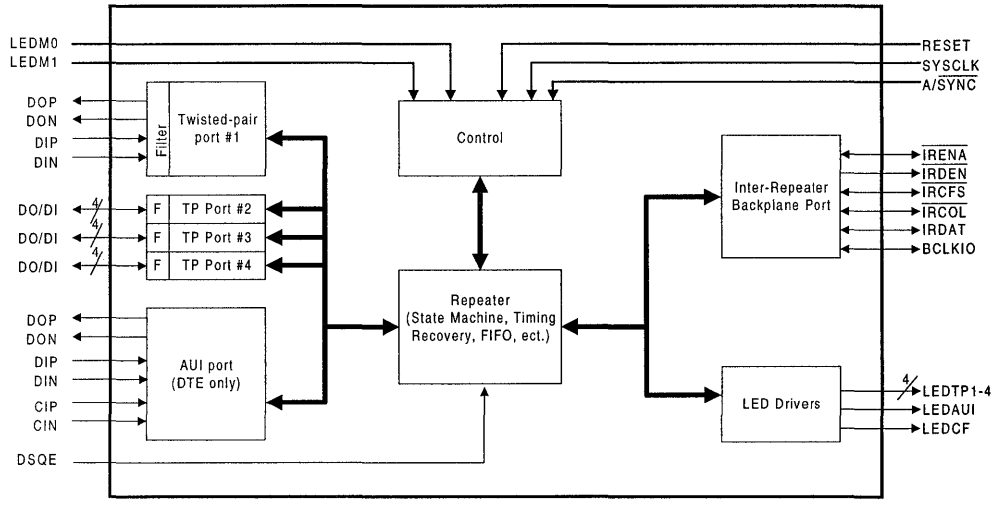
Features

- Four integrated 10BASE-T transceivers and one AUI transceiver on a single chip
- Six integrated LED drivers with four unique operational modes
- On-chip transmit and receive filtering
- Automatic polarity detection and correction
- Synchronous or asynchronous Inter-Repeater Backplane supports "hot swapping"
- Inter-repeater backplane allows cascaded repeaters, linking 128 or more 10BASE-T ports
- Packaged in 64-pin PQFP

Applications

- Remote or Stand-alone Unmanaged Hubs
- Stackable Unmanaged Hubs

LXT915 Block Diagram



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LXT915 PIN ASSIGNMENTS AND SIGNAL DESCRIPTIONS

Figure 1: LXT915 Pin Assignments

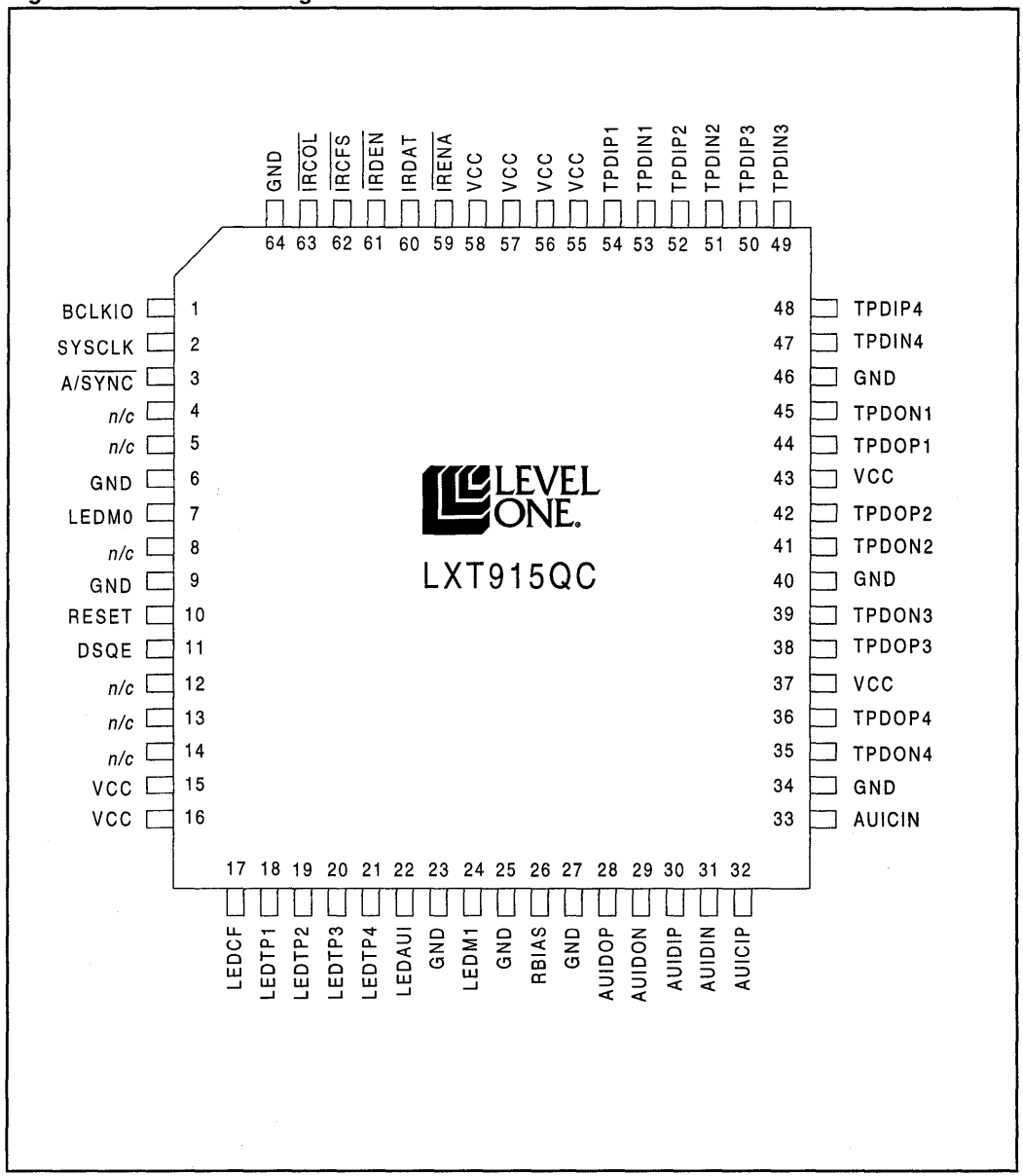

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Table 1: Twisted-Pair Port Signal Descriptions

Pin	Symbol	I/O	Description
44	TPDOP1	O	**Twisted-Pair Data Outputs (Positive and Negative).** These pins are the positive (TPDOP1-4) and negative (TPDON1-4) outputs to the network from the respective twisted-pair ports.
45	TPDON1	O	
42	TPDOP2	O	
41	TPDON2	O	
38	TPDOP3	O	
39	TPDON3	O	
36	TPDOP4	O	
35	TPDON4	O	
54	TPDIP1	I	**Twisted-Pair Data Inputs (Positive and Negative).** These pins are the positive (TPDIP1-4) and negative (TPDIN1-4) inputs from the network to the respective twisted-pair ports.
53	TPDIN1	I	
52	TPDIP2	I	
51	TPDIN2	I	
50	TPDIP3	I	
49	TPDIN3	I	
48	TPDIP4	I	
47	TPDIN4	I	

Table 2: AUI Port Signal Descriptions

Pin	Symbol	I/O	Description
28	AUIDOP	O	**AUI Data Outputs (Positive and Negative)**. These pins are the positive and negative data outputs from the AUI port.
29	AUIDON	O	
30	AUIDIP	I	**AUI Data Inputs (Positive and Negative).** These pins are the positive and negative data inputs to the AUI port.
31	AUIDIN	I	
32	AUICIP	I	**AUI Collision Inputs (Positive and Negative).** These pins are the positive and negative collision inputs to the AUI port.
33	AUICIN	I	

Table 3: Control, Status and Miscellaneous Signal Descriptions

Pin	Symbol	I/O	Description
2	SYSCLK	I	**System Clock**. The required 20 MHz system clock is input at this pin. Clock must have a 40-60 duty cycle with <10 ns rise time.
10	RESET	I	**Reset**. This pin resets the LXT915 internal circuitry when pulled or driven High for ≥ 1 ms.
11	DSQE	I	**Disable SQE.** When High the SQE function is disabled.
7	LEDM0	I	**LED Mode Select 0 & 1.** These two pins select one of four possible modes of LED operation. The Functional Description section describes the four modes and Table 6 lists the four settings.
24	LEDM1	I	

Table 3: Control, Status and Miscellaneous Signal Descriptions – continued

Pin	Symbol	I/O	Description
17	LEDCF	O	**Collision & FIFO Error LED Driver.** This tri-state LED driver pin reports collisions and FIFO errors. It pulses Low to report collisions, and pulses High to report FIFO errors. When this pin is connected to the anode of one LED and to the cathode of a second LED, the LXT915 will simultaneously monitor and report both conditions independently.
18 19 20 21	LEDTP1 LEDTP2 LEDTP3 LEDTP4	O O O O	**TP Port LED Drivers.** These tri-state LED drivers use an alternating pulsed output to report TP port status. Each pin should be tied to a pair of LEDs (to the anode of one LED and the cathode of a second LED). When connected this way, each pin reports five separate conditions (receive, transmit, link integrity, reverse polarity and auto partition).
22	LEDAUI	O	**AUI Port LED Driver.** This tri-state LED driver uses an alternating pulsed output to report AUI port status. This pin should be tied to a pair of LEDs (to the anode of one LED and the cathode of a second LED). When connected this way, this pin reports five separate conditions (receive, transmit, receive jabber, receive collision and auto partition).
4 5 8 12 13 14	NC	_	**No Connects**. *Leave these pins unconnected (mandatory).*

Table 4: Inter-Repeater Backplane Signal Descriptions

Pin	Symbol	I/O	Description
1	BCLKIO	I/O	**Backplane Clock.** This 10 MHz clock synchronizes multiple repeaters on a common backplane. In the synchronous mode, BCLKIO must be supplied to all repeaters from a common external source. In the asynchronous mode, BCLKIO is supplied only when a repeater is outputting data to the bus. Each repeater outputs its internally recovered clock when it takes control of the bus. Other repeaters on the backplane then sync to BCLKIO for the duration of the transmission.
3	A/$\overline{\text{SYNC}}$	I	**Backplane Synch Mode Select.** This pin selects the backplane synch mode. When this pin is left floating an internal pull-up defaults to the Asynchronous mode (A/$\overline{\text{SYNC}}$ High). In the asynchronous mode 12 or more LXT915s can be connected on the backplane, and an external 10 MHz backplane clock source is not required. When the synchronous mode is selected (A/$\overline{\text{SYNC}}$ tied Low), 32 or more LXT915s can be connected to the backplane and an external 10 MHz backplane clock source is required.
59	$\overline{\text{IRENA}}$	I/O	**Inter-Repeater Backplane Enable.** This pin allows individual LXT915 repeaters to take control of the Inter-Repeater Backplane (IRB) data bus (IRDAT). The $\overline{\text{IRENA}}$ bus must be pulled up locally by a 330 Ω resistor.[1]

1. $\overline{\text{IRENA}}$ and IRDAT can be buffered between boards in multi-board configurations. Where buffering is used, a 330 Ω pull-up resistor can be used on each signal, on each board. Where no buffering is used, the total impedance should be no less than 330 Ω.
2. $\overline{\text{IRCFS}}$ and $\overline{\text{IRCOL}}$ cannot be buffered. In multi-board configurations, the total impedance on $\overline{\text{IRCOL}}$ should be no smaller than 330 W. $\overline{\text{IRCFS}}$ should be pulled up only once, by a single 330 Ω, 1% resistor.

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Table 4: Inter-Repeater Backplane Signal Descriptions – continued

Pin	Symbol	I/O	Description
60	IRDAT	I/O	**IRB Data.** This pin is used to pass data between multiple repeaters on the IRB. The IRDAT bus must be pulled up locally by a 330 Ω resistor.[1]
61	$\overline{\text{IRDEN}}$	O	**IRB Driver Enable.** The $\overline{\text{IRDEN}}$ pin is used to enable external bus drivers which may be required in synchronous systems with large backplanes. This is an active low signal, maintained for the duration of the data transmission. $\overline{\text{IRDEN}}$ must be pulled up locally by a 330 Ω resistor.
62 63	$\overline{\text{IRCFS}}$ $\overline{\text{IRCOL}}$	I/O I/O	**IRB Collision Flag Sense ($\overline{\text{IRCFS}}$) and IRB Collision ($\overline{\text{IRCOL}}$).** These two pins are used for collision signalling between multiple LXT915 devices on the IRB. Both the $\overline{\text{IRCFS}}$ bus and the $\overline{\text{IRCOL}}$ bus must be pulled up globally with 330 Ω resistors.[1] ($\overline{\text{IRCFS}}$ requires a precision resistor [±1%].)[2]

1. $\overline{\text{IRENA}}$ and IRDAT can be buffered between boards in multi-board configurations. Where buffering is used, a 330 Ω pull-up resistor can be used on each signal, on each board. Where no buffering is used, the total impedance should be no less than 330 Ω.
2. $\overline{\text{IRCFS}}$ and $\overline{\text{IRCOL}}$ cannot be buffered. In multi-board configurations, the total impedance on $\overline{\text{IRCOL}}$ should be no smaller than 330 W. $\overline{\text{IRCFS}}$ should be pulled up only once, by a single 330 Ω, 1% resistor.

Table 5: LXT915 Power Supply Signal Descriptions

Pin	Symbol	I/O	Description
15 16 37 43 55 56 57 58	VCC	_	**Power Supply.** These pins each require a +5 VDC power supply. These various pins may be supplied from a single power source, but special de-coupling requirements may apply. Each VCC pin must be within ±0.3 V of every other VCC pin.
6 9 23 25 27 34 40 46 64	GND	_	**Ground.** These pins provide ground return paths for the various VCC power supply pins. *Connect these pins to external ground (mandatory).*
26	RBIAS	I	**Bias.** This pin provides bias current for internal circuitry. Connect this pin to ground through an external 12.4k 1% resistor.

FUNCTIONAL DESCRIPTION

Introduction

The LXT915 is an integrated hub repeater for 10BASE-T networks. The hub repeater is the central point for information transfer across the network. The LXT915 offers multiple operating modes to suit a broad range of applications from simple 4-, 8- or 16-port stand-alone models up to 128-port stackable hubs.

The main functions of the LXT915 hub repeater are data recovery and retransmission and collision propagation. Data packets received at the AUI or 10BASE-T ports are detected and recovered by the port receivers before being passed to the repeater core circuitry for retiming and retransmission. Data packets received through the IRB port are essentially passed directly to the core for retransmission. After recovery of a valid data packet, the repeater broadcasts it to all enabled stations, except the originator station.

External Interfaces

The LXT915 includes four 10BASE-T ports with internal filters. The LXT915 also includes an Attachment Unit Interface (AUI) port and an Inter-Repeater Backplane (IRB) port. The IRB port enables multiple LXT915 devices to be interconnected, creating a large, single-segment, multi-port repeater.

10BASE-T Ports

The four 10BASE-T transceiver ports are completely self-contained. Since the transmitters and receivers include the required filtering, only simple, inexpensive transformers are required to complete the 10BASE-T interface. Each individual Twisted-Pair (TP) port is implemented in accordance with the IEEE 802.3 10BASE-T standard. Refer to Table 1 for TP Port signal descriptions.

AUI Port

The AUI port operates in standard DTE mode and allows connection of an external transceiver (10BASE-2, 10BASE-5, 10BASE-T or FOIRL) or a drop cable. Refer to Table 2 for AUI Port signal descriptions.

Inter-Repeater Backplane

The Inter-Repeater Backplane (IRB) allows several LXT915s to function as a single repeater. The IRB also allows several multi-repeater boards to be integrated in a standard rack and to function as a single unit. The IRB supports "hot swapping" for easy maintenance and trouble-shooting. Each individual repeater distributes recovered and retimed data to other repeaters on the IRB for broadcast on all ports simultaneously. This simultaneous rebroadcast allows the multi-repeater system to act as a single large repeater unit. The maximum number of repeaters on the IRB is limited by bus loading factors such as parasitic capacitance. The IRB can be operated synchronously or asynchronously. Refer to Table 3 for control signals and to Table 4 for IRB signal descriptions.

Synchronous IRB Operation

In the synchronous mode, a common external source provides the 10 MHz backplane clock (BCLKIO) and the 20 MHz system clock (SYSCLK) to all repeaters. (BCLKIO must be synchronous to SYSCLK and may be derived from SYSCLK using a divide-by-two circuit.) In the synchronous mode 32 or more LXT915 repeaters may be connected on the IRB, providing 128 10BASE-T ports and 32 AUI ports.

Asynchronous IRB Operation

In the asynchronous mode an external BCLKIO source is not required. The repeaters run independently until one takes control of the IRB. The transmitting repeater then outputs its own 10 MHz clock onto the BCLKIO line. All other repeaters sync to that clock for the duration of the transmission. In the asynchronous mode 12 or more LXT915 devices may be connected to the IRB, providing 48 10BASE-T ports and 12 AUI ports.

NOTE

The maximum number of repeaters which may be linked on the backplane is limited by board design factors. The numbers listed above are engineering estimates only. Stronger drivers and reduced capacitive loading in PCB layout may allow an increased device count.

Internal Repeater Circuitry

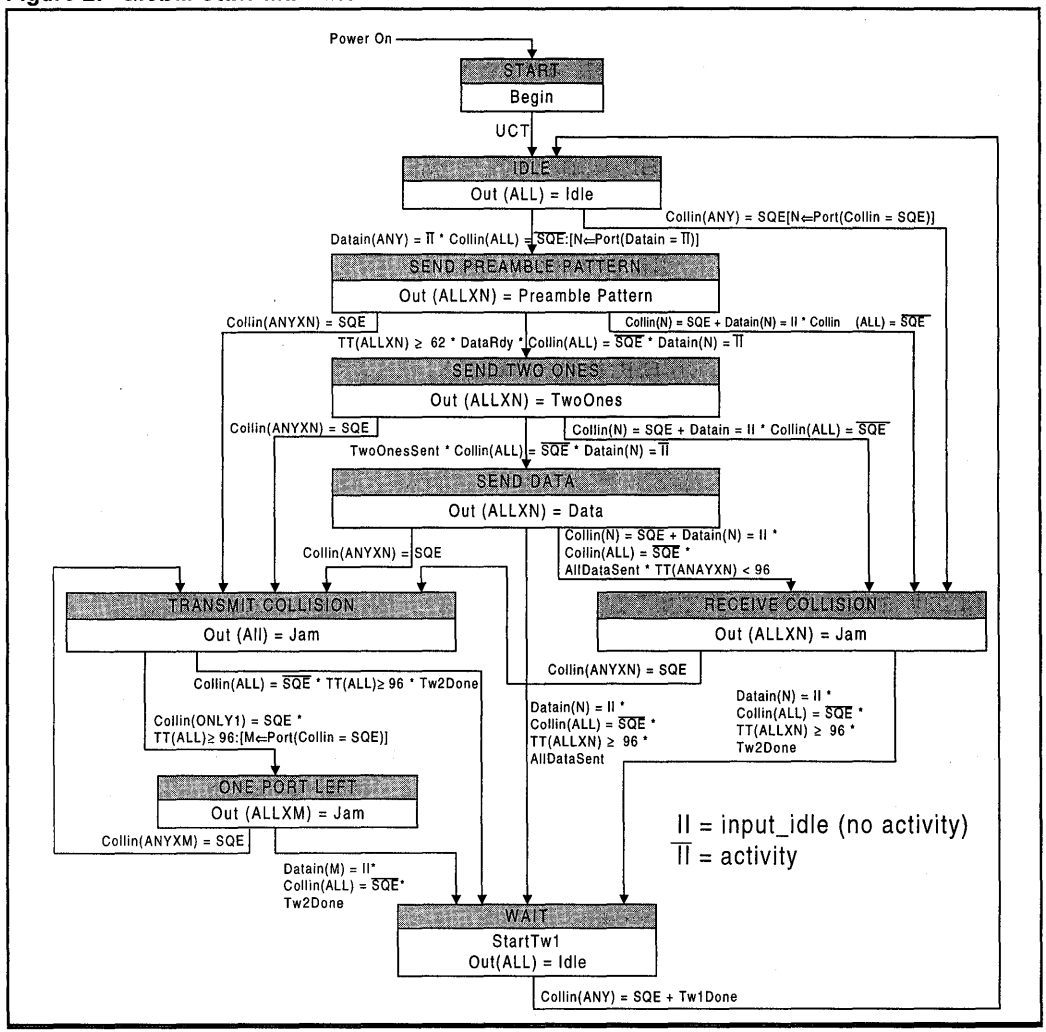
The basic repeater circuitry is shared among all the ports within the LXT915. It consists of a global repeater state machine, several timers and counters and the timing recovery circuit. The timing recovery circuit includes a FIFO for retiming and recovery of the clock which is used to clock the receive data out onto the IRB.

The shared functional blocks of the LXT915 are controlled by the global state machine shown in Figure 2. This diagram and all associated notations used are in strict accordance with section 9.6 of the IEEE 802.3 standard.

The LXT915 also implements the Partition State Diagram as defined by the IEEE 802.3 standard and shown in Figure 3. The value of CCLIMIT as implemented in the LXT915 is 64.

The CCLIMIT value sets the number of consecutive collisions that must occur before the port is subjected to automatic partitioning. Auto-partition/reconnection is also supported by the LXT915 with Tw5 conforming to the standard requirement of 450 to 560 bit times.

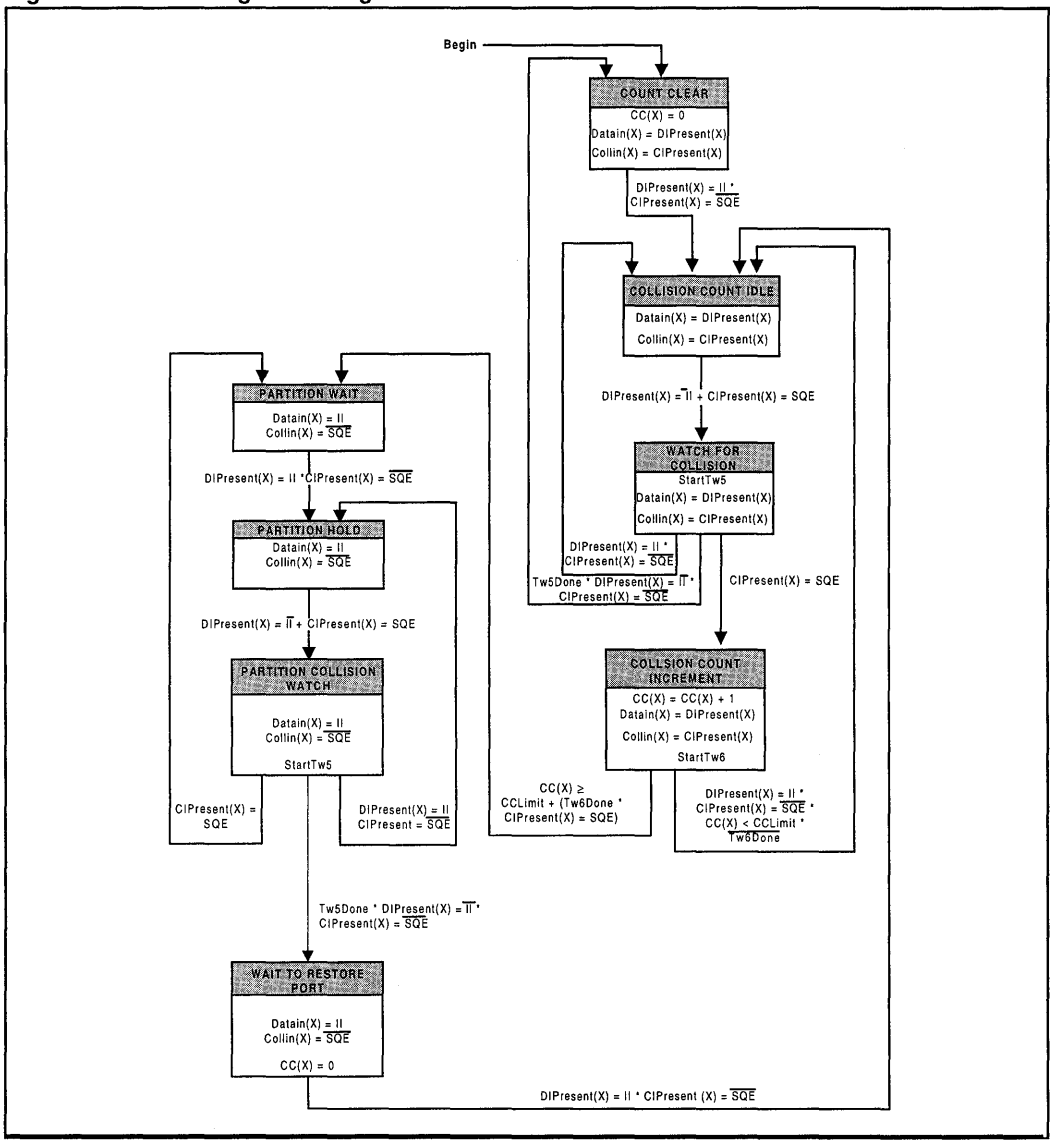
Figure 2: Global State Machine



Initialization

The following description applies to the initial power-on reset and to any subsequent hardware reset. When a reset occurs (RESET pin pulled high for > 1 ms), the device senses the levels at the various control pins (see Tables 3 and 4) to determine the correct operating modes for the LEDs and the IRB.

Figure 3: Partitioning State Diagram



10BASE-T Port Operation

10BASE-T Reception

Each LXT915 10BASE-T port receiver acquires data packets from its twisted-pair input (DIP/DIN). An internal RC filter and an intelligent squelch function discriminate noise from link test pulses and valid data streams. No external filters are required. The receive function is activated only by valid data streams (above the squelch level and with proper timing). If the differential signal at the DI circuit inputs falls below 75% of the threshold level (unsquelched) for eight bit times (typical), the port receiver enters the idle state.

Polarity Detection and Correction

The LXT915 10BASE-T ports detect and correct for reversed polarity by monitoring link pulses and end-of-frame sequences. A reversed polarity condition is declared when the port receives sixteen or more incorrect link pulses consecutively, or four frames with reversed start-of-idle sequence. In these cases the receiver reverses the polarity of the signal and thereby corrects for this failure condition. If the port enters the link fail state and no valid data or link pulses are received within 96 to 128 ms, the polarity is reset to the default non-flipped condition. (If Link Integrity Testing is disabled, polarity detection is based only on received data.)

10BASE-T Link Integrity Testing

The LXT915 fully supports the 10BASE-T Link Integrity test function. The link integrity test determines the status of the receive side twisted-pair cable. The receiver recognizes link integrity pulses transmitted in the absence of data traffic. With no data packets or link integrity pulses within 100 (±50) ms, the port enters a link fail state and disables its transmitter. The port remains in the link fail state until it detects three or more data packets or link integrity pulses.

10BASE-T Transmission

Each LXT915 10BASE-T port receives NRZ data from the repeater core and passes it through a Manchester encoder. The encoded data is then transmitted to the twisted-pair network (the DO circuit). The advanced integrated pulse shaping and filtering network produces the pre-distorted and pre-filtered output signal to meet the 10 Base-T jitter template. An internal continuous resistor-capacitor filter is used to remove any high-frequency clocking noise from the pulse shaping circuitry. Integrated filters simplify the design work required for FCC compliant EMI performance.

During idle periods, the LXT915 10BASE-T ports transmit link integrity test pulses in accordance with the 802.3 10BASE-T standard.

Data packets transmitted by the LXT915 contain a minimum of 56 preamble bits before the start of frame delimiter (SFD). In the Asynchronous mode, preamble regeneration takes place on the transmit side. In the Synchronous mode, the preamble is regenerated on the receive side and distributed via the IRB. If the total packet is less than 96 bits including the preamble, the LXT915 extends the packet length to 96 bits by appending a Jam signal (1010...) at the end.

AUI Port Operation

AUI Reception

The LXT915 AUI port receiver acquires data packets from the network (DIP/DIN). Only valid data streams above the squelch level activate the receive function. If the differential signal at the DI circuit inputs falls below 75% of the threshold level (unsquelched) for 8 bit times (typical), the AUI receiver enters the idle state.

AUI Transmission

The LXT915 AUI port receives NRZ data from the repeater core, and passes it through a Manchester encoder. The encoded data then goes out on the network (DOP/DON).

Collision Handling

A collision occurs when two or more repeater ports receive simultaneously, or when the AUI CIP/CIN signal is active. The LXT915 fully complies with the IEEE 802.3 collision specifications, both in individual and multi-repeater applications. In multiple-repeater configurations, collision signaling on the IRB allows all repeaters to share collision parameters, acting as a single large repeater.

$\overline{\text{IRCOL}}$ is a digital open-drain pin. $\overline{\text{IRCFS}}$ is an analog/digital port. The $\overline{\text{IRCOL}}$ and $\overline{\text{IRCFS}}$ lines are pulled up globally (i.e., each signal requires one pull-up resistor for all boards). If there are eight 3-repeater boards in the system, all eight boards share a single pull-up resistor for $\overline{\text{IRCOL}}$ and a single pull-up resistor for $\overline{\text{IRCFS}}$. The global pull-up may be located on one of the boards, or on the backplane. The $\overline{\text{IRCFS}}$ line requires a precision (± 1%) resistor.

The $\overline{\text{IRENA}}$, IRDAT and $\overline{\text{IRDEN}}$ lines are each pulled up locally (one pull-up resistor per board) if external bus drivers are used. If no bus drivers are used then only one global pull-up per signal is used.

LED Display

The LED display interface consists of seven integrated LED drivers, one for each of the five network ports and two for common functions. Each pin provides a three-state pulsed output (+5 V, high Z, and 0 V) which allows multiple conditions to be monitored and reported independently. Table 6 shows the LED Mode selected with each LEDM1 and LEDM0 combination. Figure 4 shows the LED Driver output conditions and Tables 7 through 10 list the repeater states associated with each of the five conditions.

LED Mode 0 (Default)

This mode is selected when LEDM1 and LEDM0 are floated or pulled low. Refer to Table 7.

LED Mode 1

This mode is selected when LEDM1 is tied, floated or pulled low and LEDM0 is pulled high by a pull-up resistor. Refer to Table 8.

LED Mode 2

This mode is selected when LEDM1 is pulled high by a pull-up resistor and LEDM0 is floated or pulled low. Refer to Table 9.

LED Mode 3

This mode is selected when LEDM1 is pulled high by a pull-up resistor and LEDM0 is also pulled high by a pull-up resistor. Refer to Table 10.

Table 6: LED Mode Selection

LEDM1 Pin 24	LEDM0 Pin 7	LED Mode Selected
0	0	0 (default)
0	1	1
1	0	2
1	1	3

Table 7: Mode 0 LED Truth Table (Default)

Condition	LEDTP 1-4	LEDAUI	LEDCF
1	Rx Link Pulse	N/A	FIFO Error
2	Tx Packet	Tx Packet	N/A
3	Reversed Polarity	N/A	Collision
4	Rx Packet	Rx Packet	N/A
5	Partitioned Out	Partitioned Out	N/A

Table 8: Mode 1 LED Truth Table

Condition	LEDTP 1-4	LEDAUI	LEDCF
1	Rx Link Pulse	N/A	MAU Jabber Lockup Protection (MJLP)
2	N/A	N/A	N/A
3	N/A	N/A	Collision
4	Rx Packet	Rx Packet	N/A
5	N/A	N/A	N/A

Table 9: Mode 2 LED Truth Table

Condition	LEDTP 1-4	LEDAUI	LEDCF
1	Rx Link Pulse	N/A	MAU Jabber Lockup Protection (MJLP)
2	Partitioned Out	Partitioned Out	N/A
3	N/A	N/A	Collision
4	Rx Packet	Rx Packet	N/A
5	N/A	N/A	N/A

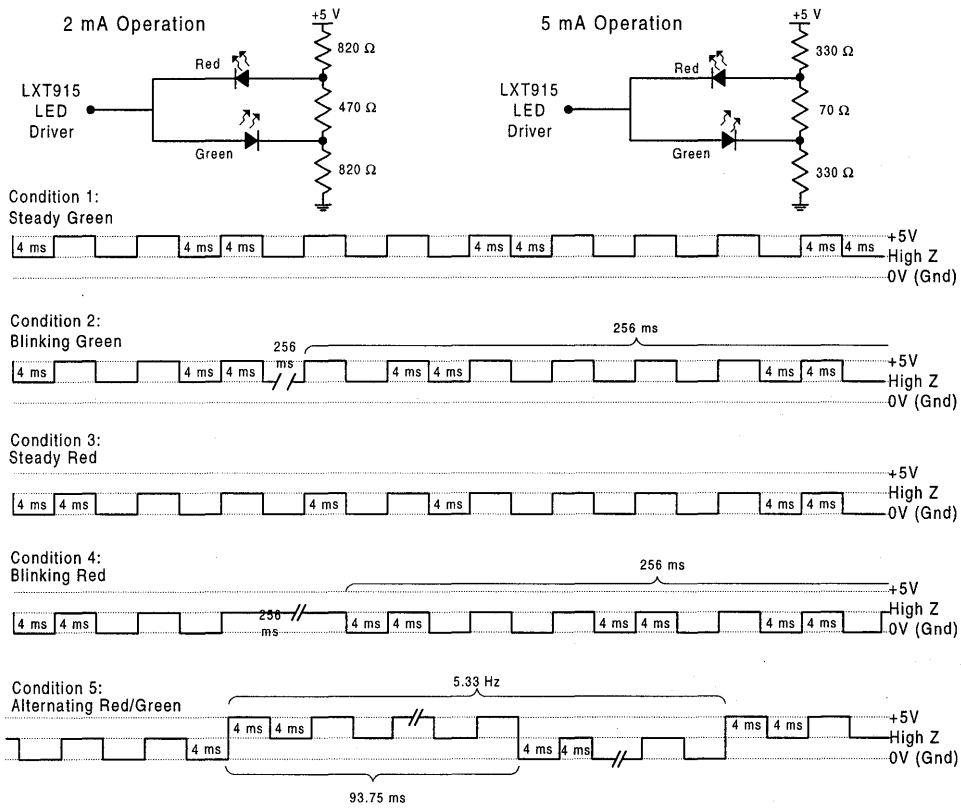
Table 10: Mode 3 LED Truth Table

Condition	LEDTP 1-4	LEDAUI	LEDCF
1	Rx Link Pulse	N/A	MAU Jabber Lockup Protection (MJLP)
2	Rx Packet	Rx Packet	N/A
3	Partitioned Out	Partitioned Out	Collision
4	N/A	N/A	N/A
5	N/A	N/A	N/A

Figure 4: Integrated LED Driver Indications

NOTE

The drivers are capable of driving a 10 mA load. The signal is pulsed every 4 ms, making the average current approximately 5 mA.



APPLICATION INFORMATION

Layout Requirements

The Twisted Pair Interface

The four, twisted-pair output circuits are identical. Each TPDOP/TDPON signal has a 24.9 Ω, 1%, series resistor and a 120 pF capacitor differentially across the positive and negative outputs. These signals go directly to a 1:$\sqrt{2}$ transformer creating the necessary 100 Ω termination for the cable. The TPDIP/TDPIN signals have a 100 Ω resistor across the positive and negative input signals to terminate the 100 Ω signal received from the line. To calculate the impedance on the output line interface, use:

$$(24.9\ \Omega + 24.9\ \Omega) * \sqrt{2}^2 \approx 100\ \Omega.$$

The layout of the twisted-pair ports is critical in complex designs. Run the signals directly from the device to the discrete termination components (located close to the transformers).

The signals running from the transformers to the connector should run in close pairs directly to the connector. Be careful not to cross the transmit and receive pairs. One way to avoid a problem is to run the receive pairs on the component side and the transmit pairs on the solder side. Careful planning during the schematic and layout stages can avoid these problems.

The PCB layout should have no ground or power planes from the transformers to the connectors. The data signals should be the only traces in this area. Place the chassis ground for the connectors near the edge of the PCB, away from the signals, connecting the connector shield with the chassis.

The RBIAS Pin

The RBIAS signal sets the levels for the output drivers of the LXT915. Any emissions or common mode noise entering the device here could be measured on the twisted pair output signals. The LXT915 requires a 12.4 kΩ, 1% resistor directly connected to RBIAS at pin 26. This connection should be as short as possible. The ground rails from pins 25 & 27 should come directly off of the device to enclose the resistor and pin forming a shielded area between the RBIAS connection and the switching signals on the PCB.

Unmanaged Hub Application

Figure 5 shows an eight-port unmanaged hub application. The application shows a pair of LXT915s connected using the Asynchronous IRB mode.

Figure 5 (Sheet 1) has the LXT915 set up with the LEDs in Mode 1 with one link LED per port and a single collision LED. In LED Mode 1, the twisted pair port LEDs display link integrity only (refer to Table 8). LED Mode 1 is selected by pulling LEDM0 High with a 1 kΩ resistor on pin 7 and pulling LEDM1 Low with pin 24 attached to ground.

Figure 5 (Sheet 2) shows the second LXT915 set up in the same LED Mode (Mode 1). The AC/DC plug and regulator circuits are commonly used in remote hub applications.

The VCC and GND pins are at the bottom of each diagram. All VCC pins use a single power supply with decoupling capacitors installed between the VCC and GND pins and their respective planes.

Figure 5: LXT915 8-Port Unmanaged Hub Application, LED Mode 1 Selected (sheet 1 of 2)

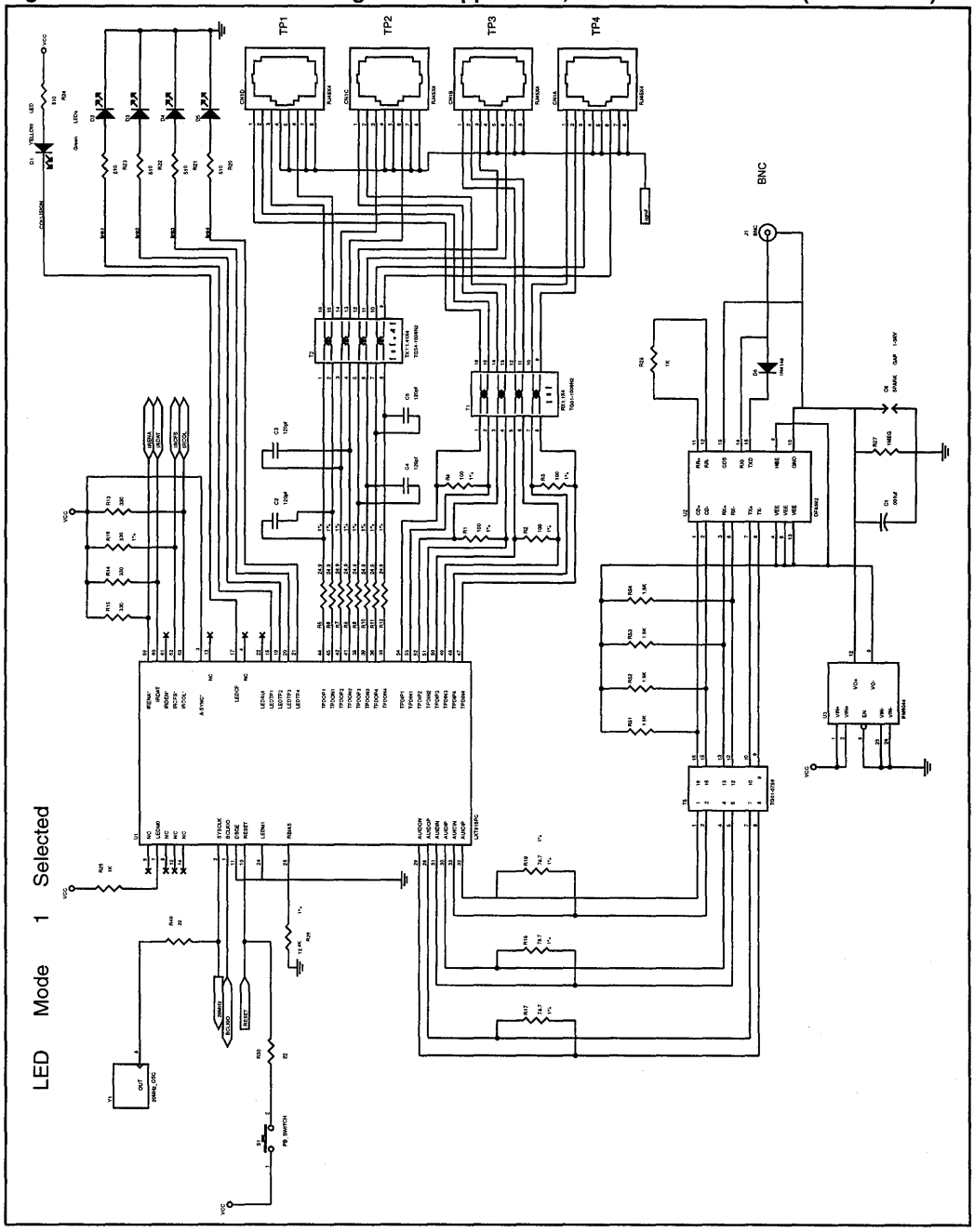
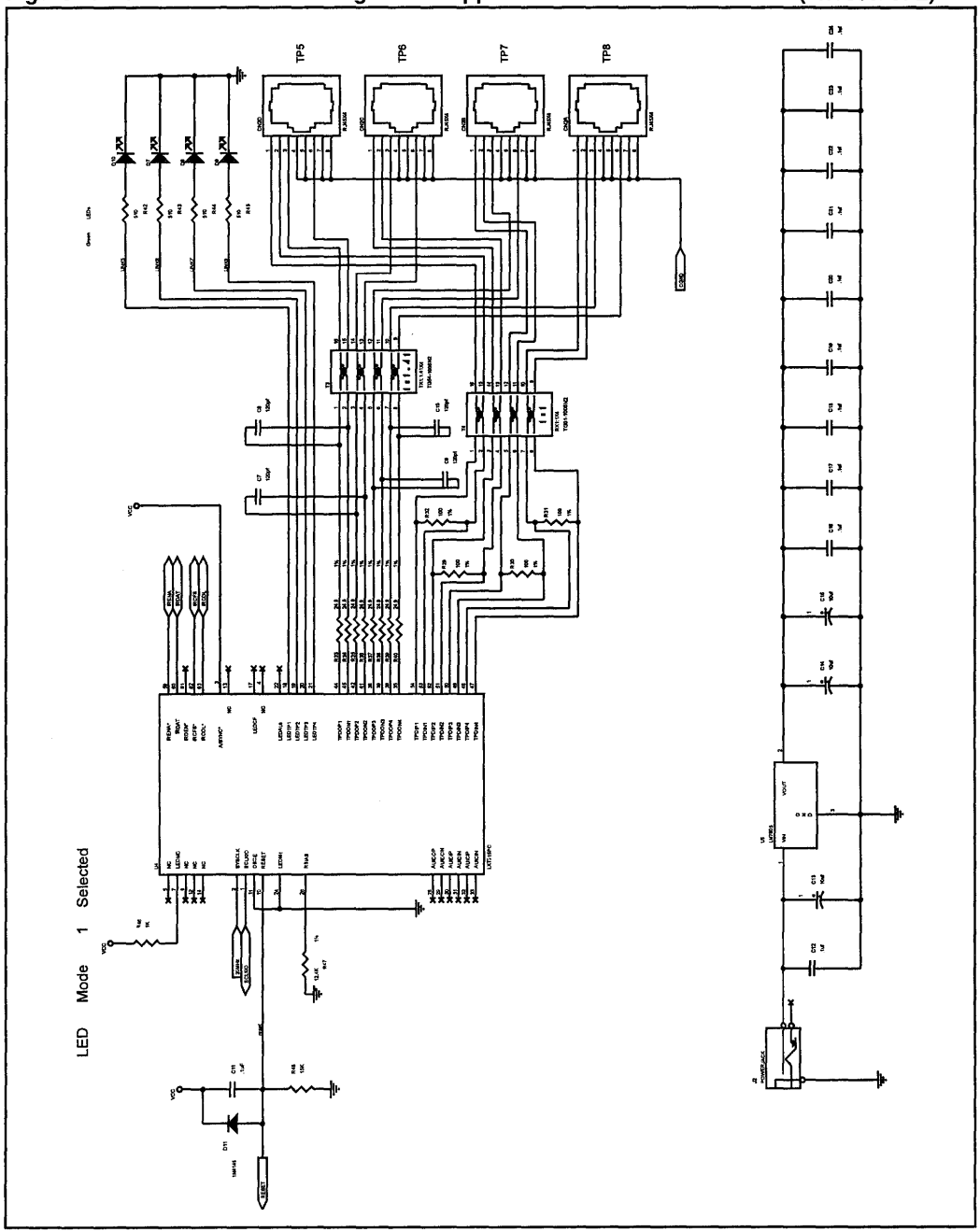


Figure 5: LXT915 8-Port Unmanaged Hub Application LED Mode 1 Selected (sheet 2 of 2)



Magnetics Requirements

The Twisted Pair Interface

The LXT915 requires transformers with a 1:1 ratio for the receive pairs and 1:$\sqrt{2}$ on the transmit pairs. The transformer isolation voltage should be rated at 2 KV to protect the circuitry from static voltages across the connectors and cables. Magnetics suitable for the LXT915 are currently available, and are used on the LXT914 Quad Repeater. Available magnetics include the following options:

- simple per-port Rx/Tx pair transformers
- receive quad transformers and transmit quad transformers
- single 40 pin octal transformers

Component Selection

Table 11 is a list of available Quad and Single port transformers with manufacturers and part numbers. This information was valid as of the printing date of this document. Before committing to a specific component, designers should contact the manufacturer for current product specifications, and should test and validate the magnetics for the specific application.

Table 11: Manufacturers Magnetics List

Manufacturer	Quad Transmit	Quad Receive	Quad Port Tx/Rx
BEL	S553-5999-02	S553-5999-03	
HALO	TD54-1006L1 TG54-1006N2	TD01-1006L1 TG01-1006N2	TG44-S010NX TG45-S010NX TG46-S010NX
Nanopulse	5976	5977	
Kappa	TP4003P	TP497P101	
PCA	EPE6009	EPE6010	
TDK	TLA-3T107	TLA-3T106	
VALOR	PT4116	PT4117	

LXT915 TEST SPECIFICATIONS

NOTE

Minimum and maximum values in Tables 12 through 19 and Figure 6 represents the performance specifications of the LXT915 and are guaranteed by test except, where noted, by design

Table 12: Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
Supply voltage	VCC	-0.3	–	6	V
Operating temperature	TOP	0	–	+70	° C
Storage temperature	TST	-65	–	+150	° C

NOTE

Exceeding these values may cause permanent damage.
Functional operation under these conditions is not implied.
Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 13: Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Recommended supply voltage	VCC	4.75	5.0	5.25	V
Recommended operating temperature	TOP	0	–	70	° C

Table 14: I/O Electrical Characteristics[1] (over recommended range)

Parameter	Symbol	Min	Typ[2]	Max	Units	Test Conditions
Supply current	ICC	–	–	180	mA	
Input Low voltage	VIL	–	–	0.8	V	
Input Low voltage (RESET)	$V_{ILRESET}$	–	–	0.8	V	V_{CC} = 5.25 V
Input High voltage	$V_{IHRESET}$	4.0	–	–	V	V_{CC} = 4.75 V
Input High voltage (RESET)	VIH	2.0	–	–	V	
Output Low voltage	VOL	–	–	0.4	V	IOL = 1.6 mA
Output Low voltage	VOL	–	–	10	% V_{CC}	IOL < 10 µA
Output Low voltage (LED)	VOLL	–	–	1.0	V	IOLL = 5 mA
Output High voltage	VOH	2.4	–	–	V	IOH = 40 µA

1. Not applicable to IRB signals; IRB electrical characteristics are specified in Table 17.
2. Typical values are at 25° C and are for design aid only; they are not guaranteed and not subject to production testing.

Table 14: I/O Electrical Characteristics[1] (over recommended range) – continued

Parameter	Symbol	Min	Typ[2]	Max	Units	Test Conditions
Output High voltage	VOH	90	–	–	% V_{CC}	IOH < 10 µA
Output High voltage (LED)	VOHL	4	–	–	V	IOHL = -5 mA
Input Low current	IIL	–	–	2	mA	VOL = .4 V
Output rise / fall time	–	–	3	8	ns	CLOAD = 20 pF
RESET pulse width	PWRESET	1.0	–	–	ms	V_{CC} = 4.75 V
RESET fall time	TFRESET	–	–	20.0	µs	VIHRESET to VILRESET

1. Not applicable to IRB signals; IRB electrical characteristics are specified in Table 17.
2. Typical values are at 25° C and are for design aid only; they are not guaranteed and not subject to production testing.

Table 15: AUI Electrical Characteristics (over recommended range)

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Input Low current	IIL	–	–	-700	µA	
Input High current	IIH	–	–	500	µA	
Differential output voltage	VOD	±550	–	±1200	mV	
Receive input impedance	ZIN	–	20	–	kΩ	Between CIP/CIN & DIP/DIN
Differential squelch threshold	VDS	–	220	–	mV	

1. Typical values are at 25 °C and are for design aid only; they are not guaranteed and no subject to production testing.

Table 16: TP Electrical Characteristics (over recommended range)

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Transmit output impedance	ZOUT	–	5	–	Ω	
Peak differential output voltage	VOD	3.3	3.5	3.7	V	Load = 100 Ω at TPOP and TPON
Transmit timing jitter addition	–	–	± 6.4	± 10	ns	0 line length
Transmit timing jitter added by the MAU and PLS sections[2]	–	–	± 3.5	± 5.5	ns	After line model specified by IEEE 802.3 for 10BASE-T
Receive input impedance	ZIN	–	20	–	kΩ	Between TPIP/TPIN
Differential squelch threshold	VDS	300	420	565	mV	5 MHz square wave input

1. Typical values are at 25 °C and are for design aid only; they are not guaranteed and not subject to production testing.
2. IEEE 802.3 specifies maximum jitter additions at 1.5 ns for the AUI cable, 0.5 ns from the encoder, and 3.5 ns from the MAU.

Table 17: IRB Electrical Characteristics (over recommended range)

Parameter	Sym	Min.	Typ[1]	Max	Units	Test Conditions
Output Low voltage	VOL	–	0.3	0.6	V	
Output rise or fall time	TRF	–	4	12	ns	
Input Low voltage: $\overline{\text{IRENA}}$, $\overline{\text{IRCOL}}$ & IRDAT	VILIRB	–	–	0.8	V	RL = 330Ω
Input High voltage: $\overline{\text{IRENA}}$, $\overline{\text{IRCOL}}$ & IRDAT	VIHIRB	3.0	–	–	V	RL = 330Ω
Input Low voltage: BCLKIO	VILBCLK	–	–	0.4	V	RL = 330Ω
Input High voltage: BCLKIO	VIHBCLK	4.0	–	–	V	RL = 330Ω

1. Typical values are at 25 °C and are for design aid only; they are not guaranteed and not subject to production testing.

Table 18: Switching Characteristics (over recommended range)

Parameter		Min	Typ[1]	Max	Units
Jabber Timing	Maximum transmit time	5.0	–	5.5	ms
	Unjab time	–	9.6	–	µs
Link Integrity Timing	Time link loss	–	60	–	ms
	Time between Link Integrity Pulses	10	–	20	ms
	Interval for valid receive Link Integrity Pulses	4.1	–	30	ms

1. Typical values are at 25 °C and are for design aid only; they are not guaranteed and not subject to production testing.

Figure 6: Inter-Repeater Bus Timing

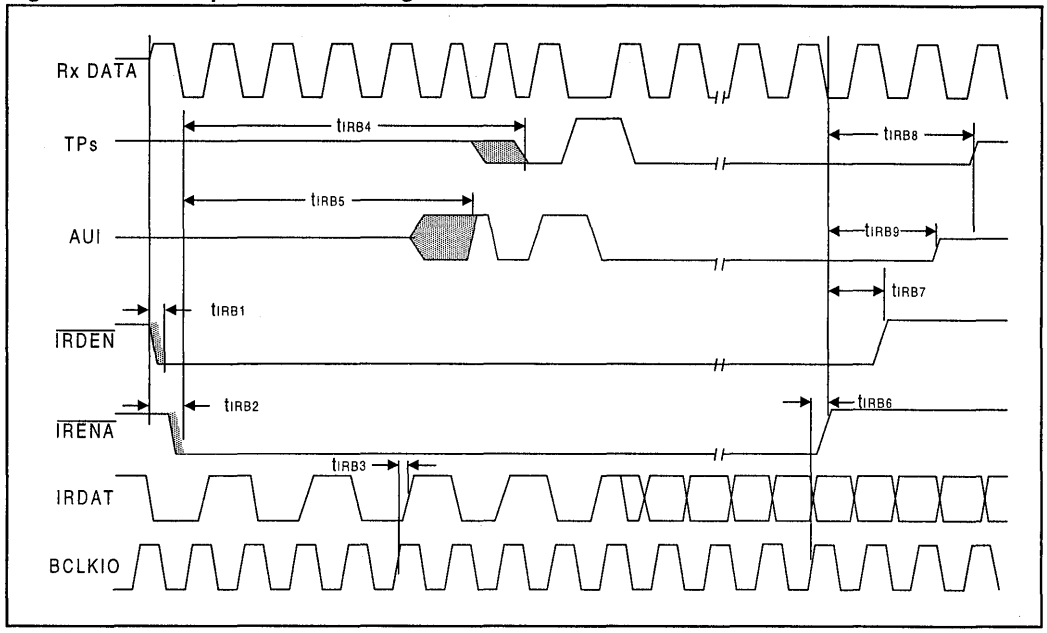


Table 19: Inter-Repeater Bus Timing (over recommended range)

Parameter	Symbol	Min	Typical[1]	Max.	Units
Start of Frame to $\overline{\text{IRDEN}}$ Low (active)	tIRB1	10	–	150	ns
Start of Frame to $\overline{\text{IRENA}}$ Low (active)	tIRB2	125	–	225	ns
BCLKIO to IRDAT valid (Synchronous mode)	tIRB3	5	–	30	ns
BCLKIO to IRDAT valid (Asynchronous mode)	tIRB3	–	50	–	ns
$\overline{\text{IRENA}}$ Low (active) to TP outputs active	tIRB4	525	–	600	ns
$\overline{\text{IRENA}}$ Low (active) to AUI output active	tIRB5	475	–	525	ns
End of Frame clock to $\overline{\text{IRENA}}$ High (inactive)	tIRB6	5	–	30	ns
$\overline{\text{IRENA}}$ High (inactive) to $\overline{\text{IRDEN}}$ High (inactive)	tIRB7	95	–	105	ns
$\overline{\text{IRENA}}$ High (inactive) to TP outputs inactive	tIRB8	575	–	600	ns
$\overline{\text{IRENA}}$ High (inactive) to AUI output inactive	tIRB9	425	–	450	ns

1. Typical values are at 25 °C and are for design aid only; they are not guaranteed and not subject to production testing.

Preliminary Information
December, 1996
Revision 1.0

LXT917/916 Multi-Port Hub Repeaters for Managed 10BASE-T Applications

General Description

The LXT917 is a fully manageable, 12-port Ethernet repeater. Using mixed-signal technology, this single IC provides direct support for RMON and for the Repeater MIB using on-chip 32-bit counters. A high-speed serial management interface provides complete control over all device operations as well as access to the counters. An inter-repeater backplane allows multiple devices to be cascaded into a single logical repeater. This backplane has been specifically designed to aid in the development of systems with multiple modules, for stackable- and modular-hub applications.

The LXT917 provides twelve 10BASE-T ports, a reversible 10BASE-5 port (AUI), and a 7-pin MAC Interface. All 10BASE-T ports are outfitted with integrated filters. The reversible AUI port can function either as a DTE or as a MAU.

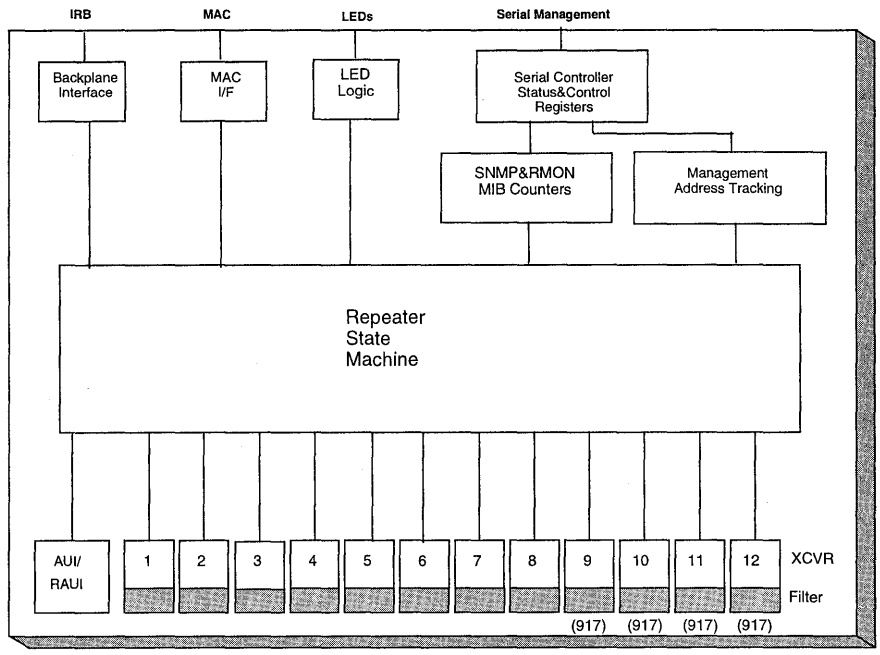
The LXT916 is an eight-port version of the LXT917 with all the same functionality.

Features

Targeted for manageable 10 Mbit repeater and router/hub applications, and remote access systems

- Eight or twelve 10BASE-T ports with Integrated Filters
- Hardware assist for RMON and the Repeater MIB
- Reversible AUI port
- Cascadable digital backplane
- 7-pin MAC interface supports bridging and advanced management applications
- High-speed serial management interface
- Two address-tracking registers per port
- Source Address matching function
- 208-pin PQFP
- 0-70°C Temperature Range

LXT917 Block Diagram



12

PIN ASSIGNMENTS AND SIGNAL DESCRIPTIONS

Figure 1: LXT917QC and LXT916QC Pin Assignments

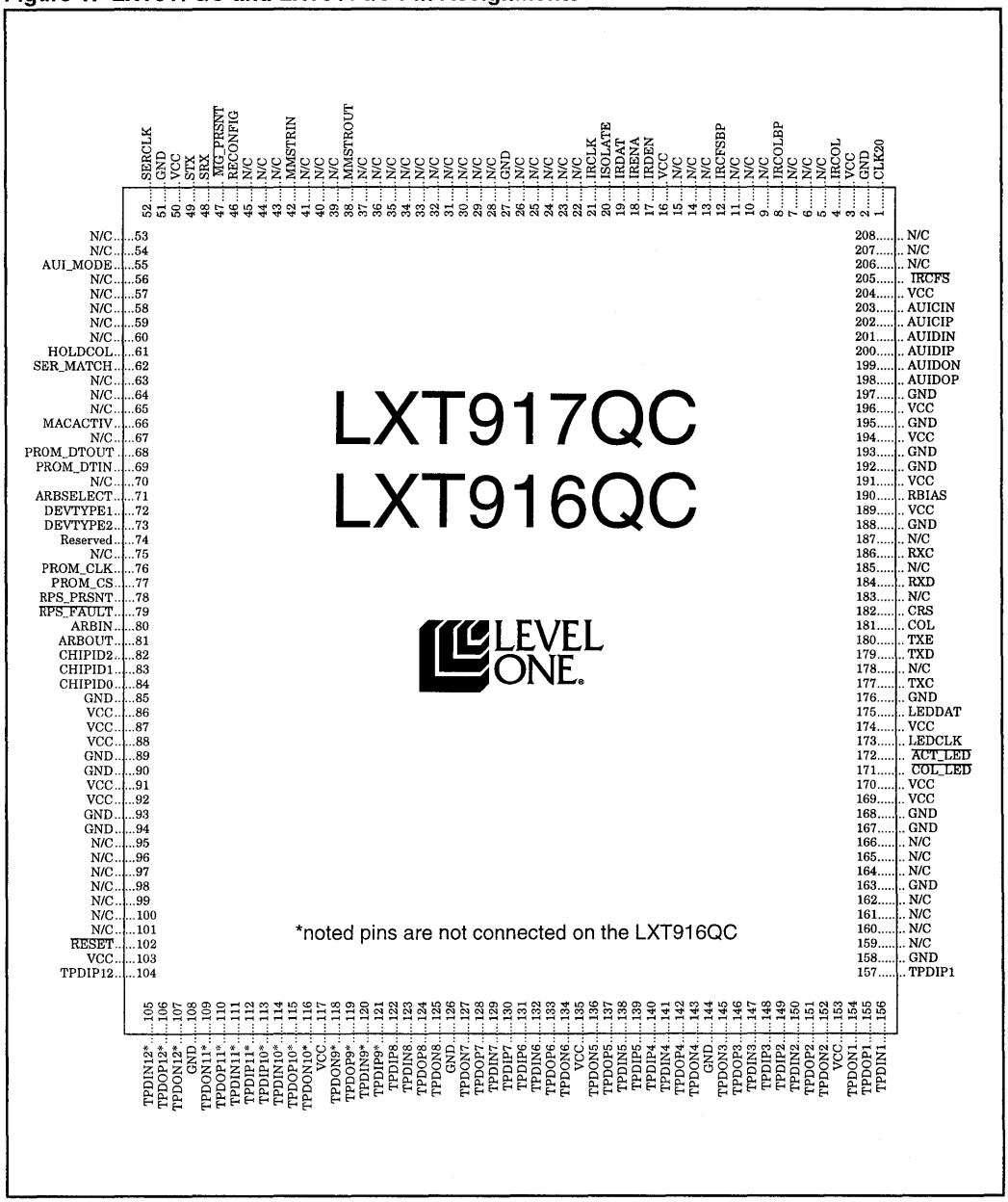


Table 1: Twisted-Pair Port Signal Descriptions

Pin	Symbol	Type	Description
155, 154 151, 152 146, 145 142, 143 137, 136 133, 134 128, 127 124, 125	TPDOP1, TPDON1 TPDOP2, TPDON2 TPDOP3, TPDON3 TPDOP4, TPDON4 TPDOP5, TPDON5 TPDOP6, TPDON6 TPDOP7, TPDON7 TPDOP8, TPDON8	Analog Output	**Twisted-Pair Data Outputs - Ports 1 through 8.** These pins are the positive and negative outputs from the respective twisted-pair port line drivers.
157, 156 149, 150 148, 147 140, 141 139, 138 131, 132 130, 129 122, 123	TPDIP1, TPDIN1 TPDIP2, TPDIN2 TPDIP3, TPDIN3 TPDIP4, TPDIN4 TPDIP5, TPDIN5 TPDIP6, TPDIN6 TPDIP7, TPDIN7 TPDIP8, TPDIN8	Analog Input	**Twisted-Pair Data Inputs - Ports 1 through 8.** These pins are the positive and negative inputs to the respective twisted-pair ports.
119, 118 115, 116 110, 109 106, 107	TPDOP9, TPDON9 TPDOP1, TPDON10 TPDOP11, TPDON11 TPDOP12, TPDON12	Analog Output	**Twisted-Pair Data Outputs - Ports 9 through 12.** These pins are the positive and negative outputs from the respective twisted-pair port line drivers. On the 916, ports 9 through 12 should be left unconnected.
121, 120 113, 114 112, 111 104, 105	TPDIP9, TPDIN9 TPDIP10, TPDIN10 TPDIP11, TPDIN11 TPDIP12, TPDIN12	Analog Input	**Twisted-Pair Data Inputs - Ports 9 through 12.** These pins are the positive and negative inputs to the respective twisted-pair ports. On the LXT916, ports 9 through 12 should be left unconnected.

Table 2: AUI Port Signal Descriptions

Pin	Symbol	Type	Description
55	AUI_MODE	TTL Input PD	**AUI Mode Select.** Low = Normal Mode (DTE). High = Reverse Mode (MAU)
198 199	AUIDOP AUIDON	Analog Output	**AUI Data Outputs.** Positive and negative data outputs for the AUI port. In normal (DTE) mode, connect to pins 3 and 10 of the AUI D-connector. In reverse (MAU) mode, connect to pins 5 and 12 of the AUI D-connector.
200 201	AUIDIP AUIDIN	Analog Input	**AUI Data Inputs.** Positive and negative data inputs for the AUI port. In normal (DTE) mode, connect to pins 5 and 12 of the AUI D-connector. In reverse (MAU) mode, connect to pins 3 and 10 of the AUI D-connector.
202 203	AUICIP AUICIN	Tri-State, Analog, I/O	**AUI Collision Inputs.** In normal (DTE) mode these pins are the positive and negative collision inputs for the AUI port. In reverse (MAU) mode these pins are outputs.

1. PD = Input contains pull-down.

Table 3: Inter-Repeater Backplane Signal Descriptions

Pin	Symbol	Type	Description
17	$\overline{\text{IRDEN}}$	Open-Drain Output	**IRB Driver Enable.** This output provides directional control for an external bi-directional transceiver ('245) used to buffer the IRBs in multi-module applications. It must be pulled up by 330 Ω resistors. When there are multiple devices on one module, tie all $\overline{\text{IRDEN}}$ outputs together. If $\overline{\text{IRDEN}}$ is tied directly to the DIR pin on a '245, attach the on-board IRDAT, IRCLK and $\overline{\text{IRENA}}$ signals to the "B" side of the '245, and connect the off-board signals to the "A" side of the '245.
18	$\overline{\text{IRENA}}$	CMOS I/O Open Drain	**Inter-Repeater Backplane Enable.** This active low output indicates carrier presence on the IRB. When the IRB is idle, a 330 Ω pull-up resistor pulls the $\overline{\text{IRENA}}$ output High. When there are multiple devices, tie all $\overline{\text{IRENA}}$ outputs together. This signal may be buffered between modules.
19	IRDAT	CMOS I/O Open Drain	**IRB Data.** This bidirectional signal carries data on the IRB. Data is driven and sampled on the rising edge of IRCLK. This signal must be pulled up by a 330 Ω resistor. Between modules, this signal can be buffered.
20	ISOLATE	Output	**Isolate Enable.** This output allows one LXT917/916 per module the ability to enable or disable an external bidirectional transceiver ('245). Attach the output to the Enable input of the '245. The output is driven High (disable) to isolate the IRB.
21	IRCLK	CMOS I/O TriState Schmitt Trigger #2	**IRB Clock.** This bi-directional, non-continuous, 10 MHz clock is recovered from received network traffic. During idle periods, this output is high-impedanced. Schmitt triggering is used to increase noise immunity, therefore full rail-to-rail signals are required. Between modules, buffering may be used on this signal.
4	$\overline{\text{IRCOL}}$	CMOS I/O Open Drain	**IRB Collision.** This output is driven low to indicate that a collision has occurred. When there is no collision, a 330 Ω pull-up resistor (required) on the output pulls it High. This signal is intended only to be used between devices on the same module; it may not be buffered.
8	$\overline{\text{IRCOLBP}}$	CMOS I/O Open Drain NC	**IRB Collision-BackPlane.** This active Low output has the same function as $\overline{\text{IRCOL}}$, but is used between modules. Attach this signal only from the device with ChipID = 0 to the backplane or connector, **without buffering**. The output must be pulled up by one 330Ω resistor per system.
205	$\overline{\text{IRCFS}}$	Analog, I/O	**IRB Collision Force Sense.** This three-state analog output indicates that a transmit collision has occurred when it is driven Low. It must be pulled up with a 680 Ω, 1% resistor. This signal is intended only to be used between devices on the same module; it may not be buffered.
12	$\overline{\text{IRCFSBP}}$	Analog I/O, N/C	**IRB Collision Force Sense-BackPlane.** This output has exactly the same function as $\overline{\text{IRCFS}}$, but is used between modules. Attach this signal only from the device with ChipID = 0 to the backplane or connector, **without buffering**. This output must be pulled up by one 330 Ω, 1% resistor per system.

1. PU = Input contains pull-up.
2. PD = Input contains pull-down.
3. NC = No Clamp. Pad will not clamp input in the absence of power.
4. Even if the IRB is not used, required pull-up resistors must be installed as listed above.

Table 3: Inter-Repeater Backplane Signal Descriptions– *continued*

Pin	Symbol	Type	Description
61	HOLDCOL	TTL Tri-state I/O, PD	**Hold Collision.** This active High signal is driven by the device with ChipID = 0 to extend a non-local transmit collision to other devices on the same module. The HOLDCOL signals from different modules should NOT be attached together.
42	MMSTRIN	TTL Input, NC	**Management Master In.** The MMSTR daisy chain ensures that collisions will be counted correctly in multi-module applications. Attach the MMSTRIN input of each device to the MMSTROUT output of the previous device. Ground MMSTRIN of the first or only device.
38	MMSTROUT	Output, NC	**Management Master Out.** MMSTR daisy chain output. In hot-swap applications, a 1 kΩ - 3 kΩ resistor can be used as a by-pass between MMSTRIN and MMSTROUT.
66	MACACTIV	TTL Input, PD	**MAC Active.** This active High input allows external Ethernet controllers to directly drive the Inter Repeater Backplane. When the controller asserts MACACTIV, the LXT917 drives the $\overline{\text{IRCOL}}$, $\overline{\text{IRCOLBP}}$, $\overline{\text{IRCFS}}$ and $\overline{\text{IRCFSBP}}$ signals on behalf of the controller. If any of these inputs are unused, tie them to ground.

1. PU = Input contains pull-up.
2. PD = Input contains pull-down.
3. NC = No Clamp. Pad will not clamp input in the absence of power.
4. Even if the IRB is not used, required pull-up resistors must be installed as listed above.

Table 4: MAC Interface Signal Descriptions

Pin	Symbol	Type	Description
177	TXC	Output	**Transmit Clock.** This 10 MHz continuous output is derived from the 20 MHz input clock.
179	TXD	TTL Input, PD	**Transmit Data.** External controllers use this input to transmit data to the LXT917. The device samples TXD on the rising edge of TXC, when TXE is High.
180	TXE	TTL Input, PD	**Transmit Enable** External controllers drive this input High to indicate that data is being transmitted on the TXD pin. Tie this input Low if it is unused.
181	COL	Output	**Collision.** The LXT917 drives this signal High to indicate that a collision has occurred.
182	CRS	Output	**Carrier Sense.** The LXT917 drives this signal High to indicate that valid data is present on RXD.
184	RXD	Output	**Receive Data.** The LXT917 transmits received data to the controller on this output. Data is driven on the falling edge of RXC.
186	RXC	Output	**Receive Clock.** This is a non-continuous 10 MHz clock that the LXT917 recovers from the network when traffic is actively being received.

1. PD = Input contains pull-down.

Table 5: Serial Management Interface Signal Descriptions

Pin	Symbol	Type	Description
46	RECONFIG	TTL Input, NC	**Reconfigure.** This input controls the driving of the clock signal on the high-speed serial management interface (SERCLK). When this input is High, the LXT917 drives SERCLK with a 625 kHz output. When this input is Low, SERCLK is an input to the LXT917. In addition, a Low-to-High transition on RECONFIG causes the LXT917 to drive 13 continuous 0's on the serial management bus, causing a re-arbitration to occur.
47	$\overline{\text{MG\_PRSNT}}$	TTL Input NC	**Manager Present.** This signal is sensed at power up. If it is High, it indicates that no local manager is present, and the 917 enables all ports and sets all LEDs to operate in "hardware mode". If it is Low, indicating that a manager is present, the 917 disables all ports, pending control of network manager.
48	SRX	TTL Input	**Serial Receive.** Receive data input for high-speed serial management interface. Must be tied to STX externally. SRX is sampled on the rising edge of SERCLK.
49	STX	Open Drain Output	**Serial Transmit.** Transmit data output for high-speed serial management interface. Must be tied to SRX externally. Data transmitted on STX is compared with data received on SRX. In the event of a mismatch, STX is put in the high impedance state. STX is driven on the falling edge of SERCLK.
52	SERCLK	Tri-State TTL Output	**Serial Clock.** Clock for serial management interface. Depending on RECONFIG, this pin is either a 625 kHz output or a 0 to 1 MHz input.

1. NC = No Clamp. Pad will not clamp input in the absence of power.

Table 6: LED Signal Descriptions

Pin	Symbol	Type	Description
171	COL_LED	Open-Drain Output, PU	**Collision LED Driver.** This output provides up to 10 mA of sink current.
172	ACT_LED	Open-Drain Output, PU	**Activity LED Driver.** This output provides up to 10 mA of sink current.
173	LED_CLK	Output	**LED Clock.** Clock for LED serial data output.
175	LED_DAT	Output	**LED Data.** Serial data output for LED data.

1. PU = Pad contains pull-up.

Table 7: PROM Interface Signal Descriptions

Pin	Symbol	Type	Description
76	PROM_CLK	TTL Input, Tri-State Output	**PROM Clock.** 1 MHz clock for reading PROM data.
77	PROM_CS	Tri-State Output, PD	**PROM Chip Select.**
68	PROM_OUT	Tri-State Output, PD	**PROM Data Output.**
69	PROM_IN	TTL Input	**PROM Data Input.** If a PROM is not used, this input can be tied Low or High.

1. PD = Input contains pull-down.

Table 8: Power Supply and Indication Signal Descriptions

Pin	Symbol	Type	Description
3, 16, 50, 86-88, 91-92, 103, 117, 135, 153, 169-170, 174, 189, 191, 194, 196, 204	VCC	Power	**Power Supply Inputs.** Each of these pins must be connected to a common +5 VDC power supply. A de-coupling capacitor to digital ground should be supplied for every one of these pins.
2, 27 51, 85 89-90 93-94 108 126, 144 158, 163 167-168, 176, 188 192-193 195, 197	GND	Power	**Ground.** Connect each of these pins to digital ground. Note: the LXT917 does NOT require separate digital and analog grounds.
190	RBIAS	Analog	**RBias.** Connect this pin to ground through a 22 kΩ, 1% resistor. Note: Do NOT route any other signals near or around this resistor.
78	RPS_PRSNT	TTL Input	**Redundant Power Supply.** Active High input indicates presence of redundant power supply. The state of this input and the RPS_FAULT input is reflected in the RPS LED bit in the serial LED output (refer to Tables 10 and 11). Tie Low if not used.
79	$\overline{\text{RPS\_FAULT}}$	TTL Input	**Redundant Power Supply Fault.** Active Low input indicates redundant power supply fault. Tie High if not used.

Table 9: Miscellaneous Signal Descriptions

Pin	Symbol	Type	Description
1	CLK20	CMOS Input, Schmitt Trigger #1	**20 MHz System Clock.** Drive with CMOS levels.
62	SER_MATCH	Output	**Hub ID Match.** Active High. The device with ChipID = 0 asserts this signal whenever it detects a message on the serial bus which matches the local Hub ID.
71	ARBSELECT	TTL Input, PU	**Arbitration Select.** If this pin is pulled Low, Arbitration Mechanism #1 is disabled, only Arbitration Mechanism #2 will be available. If this pin is pulled High, both mechanisms will be enabled. If Arbitration Mechanism #1 is enabled, the device with ChipID = 0 will transmit an "Arbitration Request" message every 2-3 ms on the serial management interface until a Hub ID is assigned.

2. PU = Input contains pull-up.
3. PD = Input contains pull-down.
4. NC = No Clamp. Pad will not clamp input in the absence of power.

Table 9: Miscellaneous Signal Descriptions– *continued*

Pin	Symbol	Type	Description
72 73	DEVTYPE1 DEVTYPE2	TTL Input, PD TTL Input, PU	**Device Type 1 and 2.** Used to identify product type. Set DEVTYPE(2:1) = 00 for the LXT916. Set DEVTYPE(2:1) = 01 for the LXT917.
80	ARBIN	Tri-State Input, PD, NC	**Arbitration In/Out.** Daisy chain hub ID arbitration mechanism #2. If used, tie ARBIN to ARBOUT of the previous device, and to ground of the first/only device. If unused, tie ARBIN High.
81	ARBOUT	Output, NC	
82 83 84	CHIPID2 CHIPID1 CHIPID0	TTL Input	**Chip ID.** These pins assign unique ChipIDs to as many as eight devices on a single module. One device on each module must be assigned ChipID=0.
102	$\overline{\text{RESET}}$	CMOS Input, Schmitt Trigger #1, PU, NC	**Reset**. This active Low input causes internal circuits and state machines to reset, but does not affect counters or address tracking registers. On power-up, devices should not be brought out of reset until the power supply has stabilized and reached 4.5 volts. When there are multiple devices, it is recommended that all be supplied by a common reset that is driven by an 'LS14 or similar device.
74	RESERVED	-	**Reserved**. Reserved for future application development. *Leave this pin unconnected.*
5-7 9-11 13-15 22-26 28-37 39-41 43-45 53-54 56-60 63-65 67 70 75 95-101 159-162 164-166 178 183 185 187 206-208	No Connect	-	**No Connects**. *Leave these pins unconnected.*

2. PU = Input contains pull-up.
3. PD = Input contains pull-down.
4. NC = No Clamp. Pad will not clamp input in the absence of power.

FUNCTIONAL DESCRIPTION

INTRODUCTION

The LXT917 is ideally suited for managed 10 Megabit Ethernet repeater solutions. This device furnishes a complete 12-port repeater with built-in support for RMON and the Repeater MIB. The LXT917 supplies 10BASE-T Ethernet ports with integrated filters, a reversible AUI port, and a 7-pin MAC Interface. In addition, the device furnishes an Inter Repeater Backplane (IRB) and a serial management interface, both of which support multiple devices for cascaded repeater applications. The LXT916 is identical to the LXT917 except that it provides 8 10BASE-T ports, not 12. Unless specifically noted, all references to the LXT917 also apply to the LXT916.

10BASE-T Ports

The LXT917 provides 10BASE-T ports with integrated filters. Level One's patented filter technology helps facilitate low-cost systems which meet EMI requirements. Refer to Table 1 for 10BASE-T port pin assignments and signal descriptions.

AUI Port

The LXT917 provides a reversible AUI interface that can function either as a DTE or as a MAU. When this interface functions as a MAU, it supports remote-office and embedded-hub applications (such as file servers) by allowing integration of the LXT917 to existing PHY interfaces. The mode of operation is selected externally through the AUI_MODE pin. Refer to Table 2 for AUI port pin assignments and signal descriptions.

Inter-Repeater Backplane

The LXT917 easily accommodates stackable and modular hub architectures through the Inter-Repeater Backplane, which allows multiple devices to function as one logical repeater. For example, typical LXT917 stack designs accomodate as many as 192 10BASE-T ports. Refer to Table 3 for IRB pin assignments and signal descriptions.

7-pin MAC Interface

The LXT917 provides a 7-pin MAC Interface, which can be interfaced to an Ethernet controller. Refer to Table 4 for MAC I/F pin assignments and signal descriptions.

Serial Management Interface

Multiple devices can easily be managed through the high-speed serial management interface. This synchronous interface operates at rates up to 1 Mbps, and uses an HDLC-like zero-bit insertion protocol. This interface provides access to the RMON and Repeater MIB variables as well as complete control over all device functions and visibility of all status registers. Refer to Table 5 for serial management bus pin assignments and signal descriptions.

Management Support

The LXT917 supports RMON and the Repeater MIB using on-chip 32-bit counters. Counters are provided for each port, including the MAC port, and for the interface as a whole. Interface counters include all of the RMON Statistics group and Repeater MIB Total Octets and Transmit Collisions. Per-port counters include:

Readable Frames	Readable Octets	FCS Errors
Alignment Errors	FramesTooLong	ShortEvents
Runts	Collisions	LateEvents
VeryLongEvents	DataRateMismatch	AutoPartitions
Broadcast	Multicast	SA Changes

Source Address Management Functions

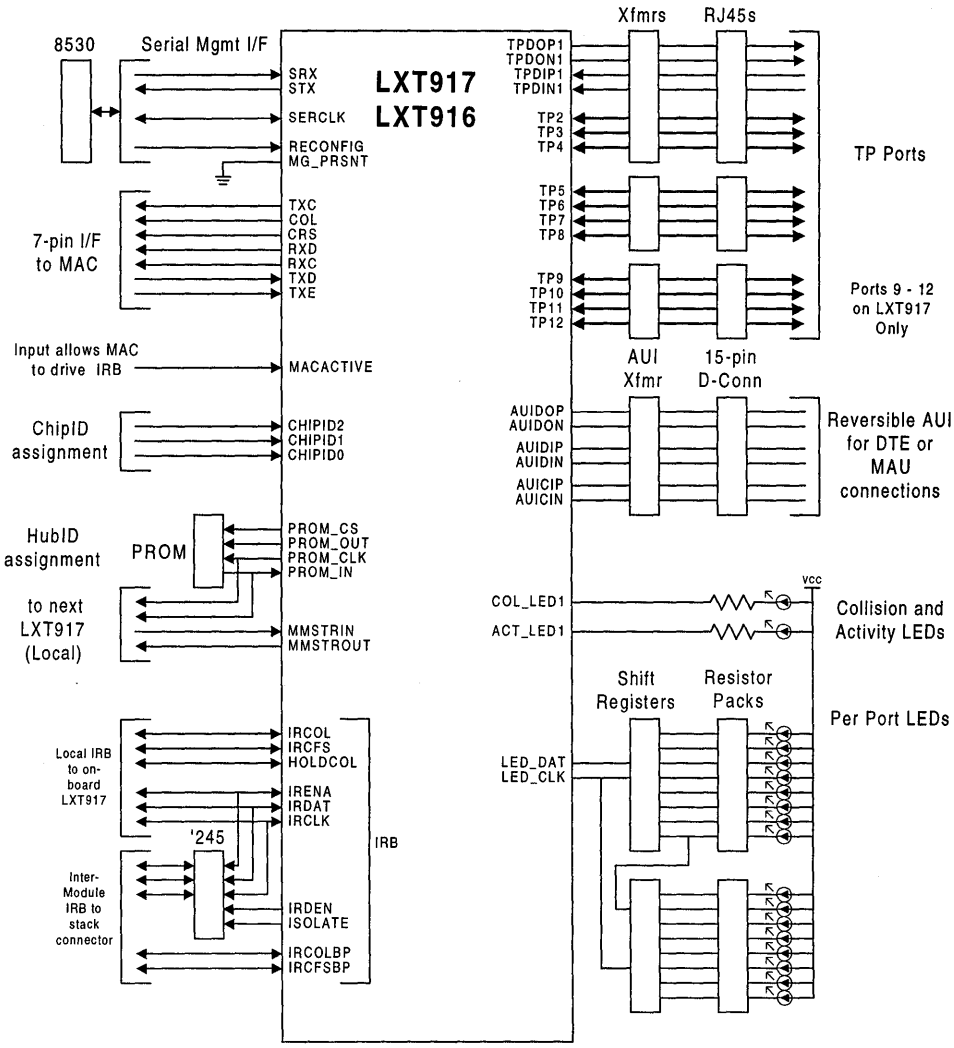
The LXT917 provides Source Address Management functions for all ports. Each port has two source-address tracking registers. The rptrAddrTrackNewLastSrcAddress register is always free-running and contains the source address of the last valid packet received from the port. The Authorized Address Register operates in three states: free-run, lock-on-next or lock. This register can track source addresses or lock on an address that has been assigned by the network manager or that it has previously tracked. Once this register is locked, subsequent Source Address changes on a port cause the device to set the corresponding bits in the SA Change Detection Register and the Interrupt Status Register.

The LXT917 also provides a Source Address Tracking Function. Supplied with a 48-bit Ethernet Source Address, this function identifies all ports that sourced that Source Address.

LED Interface

The serial LED interface (data and clock) supplies link and partition status for each of the TP ports, status for the AUI port, and miscellaneous functions. The device directly provides activity and collision LEDs. Refer to Table 6 for LED Interface pin assignments and signal descriptions.

Figure 2: Typical Application Block Diagram



Notes:

1. Refer to Figure 10 for typical TP port interface circuitry.
2. Refer to Figures 11 and 12 for typical AUI port interface circuitry.
3. Refer to Figure 13 for typical IRB circuitry.
4. Refer to Figure 14 for typical Serial Management Interface circuitry.
5. Refer to Figure 16 for typical PROM circuitry.
6. Refer to Figure 17 for typical LED circuitry.

REQUIREMENTS

Power

The LXT917 requires a single +5V power supply, and a single ground reference. Separate analog and digital grounds are NOT required. Refer to Table 8 for power and ground pin assignments.

Clock

The LXT917 requires a continuous 20 MHz clock input, driven with CMOS levels.

RBIAS

The LXT917 requires a 1% 22 kΩ resistor connecting its RBIAS input to ground.

Reset

At power up, the reset input must be held low until VCC reaches at least 4.5V. An 'LS14 or equivalent should be used to drive reset if there are multiple 917 devices.

PROM

The LXT917 requires an external, auto-incrementing PROM, which is used to supply a 48-bit ID at power-up. If the PROM is not available, the PROM data input signal must be tied either high or low. Multiple devices on the same module can share a single common PROM. Refer to Table 7 for PROM interface pin assignments and signal descriptions.

Chip ID

Each LXT917 on a module requires a unique 3-bit Chip ID value asserted on these pins in order for the serial management bus to function correctly. Exactly one and only one LXT917 on each module must be assigned ChipID = 0.

MMSTRIN/MMSTROUT

In multiple device applications, the Management Master daisy chain (MMSTRIN/MMSTROUT) ensures that collisions are correctly counted . Connect the MMSTRIN input to the MMSTROUT output of the previous device, even across module boundaries. Ground the MMSTRIN input of the first/only device in the system. In hot-swap applications, resistive bypassing can be used, with a value between 1 and 3 kΩ.

REPEATER OPERATION

LXT917 repeater operation is controlled by the state machine shown in Figure 3. When the LXT917 detects activity at any input, it begins generating preamble to all other outputs. Once 62 bits of preamble have been transmitted, and a start-of-frame delimiter (SFD) has been received, the device begins repeating the received packet to all outputs. An internal fifo provides buffering. Operation continues until the receiver goes idle, or until the jabber timer is exceeded.

If activity is detected simultaneously at two or more inputs, the LXT917 enters the transmit collision state. The device sends a jam signal to all ports on the repeater for 96 bit times. A jam signal continues to be sent to all ports as long as two or more inputs are active. If activity simultaneously ceases at all inputs, the device returns to the idle state. If activity continues at only one input, the device enters the one-port-left state. In that state, the LXT917 continues to transmit a jam signal to all ports *except* to the one that has the active input. Once this activity ceases, the repeater returns to the idle state.

If the AUI port is functioning as the DTE, and an external MAU activates the CI inputs while the port is active, the device enters the receive collision state. The LXT917 sends a jam signal to all ports (except the AUI port) for at least 96 bit times and until all activity ceases.

In multiple-device configurations, all devices participate in data exchange and the various collision states via the Inter Repeater Backplane.

Exception Conditions

Fragment Extension

Any received activity shorter than 96 bits (also known as a fragment) will be extended so that it is at least 96 bits long. On the Inter Repeater Backplane, a fragment extension will look like a receive collision, however it will not be counted as a collision.

Packets with no SFD

Packets with no start-of-frame delimiter will be repeated to all ports as a long preamble pattern with no SFD. These packets will be counted as "fragments" by the management counters, no matter how long they are.

Packets with too early SFD

Any packet with less than 40 bits of preamble will cause the internal fifo to overflow, causing invalid packets to be transmitted to all ports. If the EFIFOERR bit in the Master Configuration register is set when this occurs, a transmit collision will be generated.

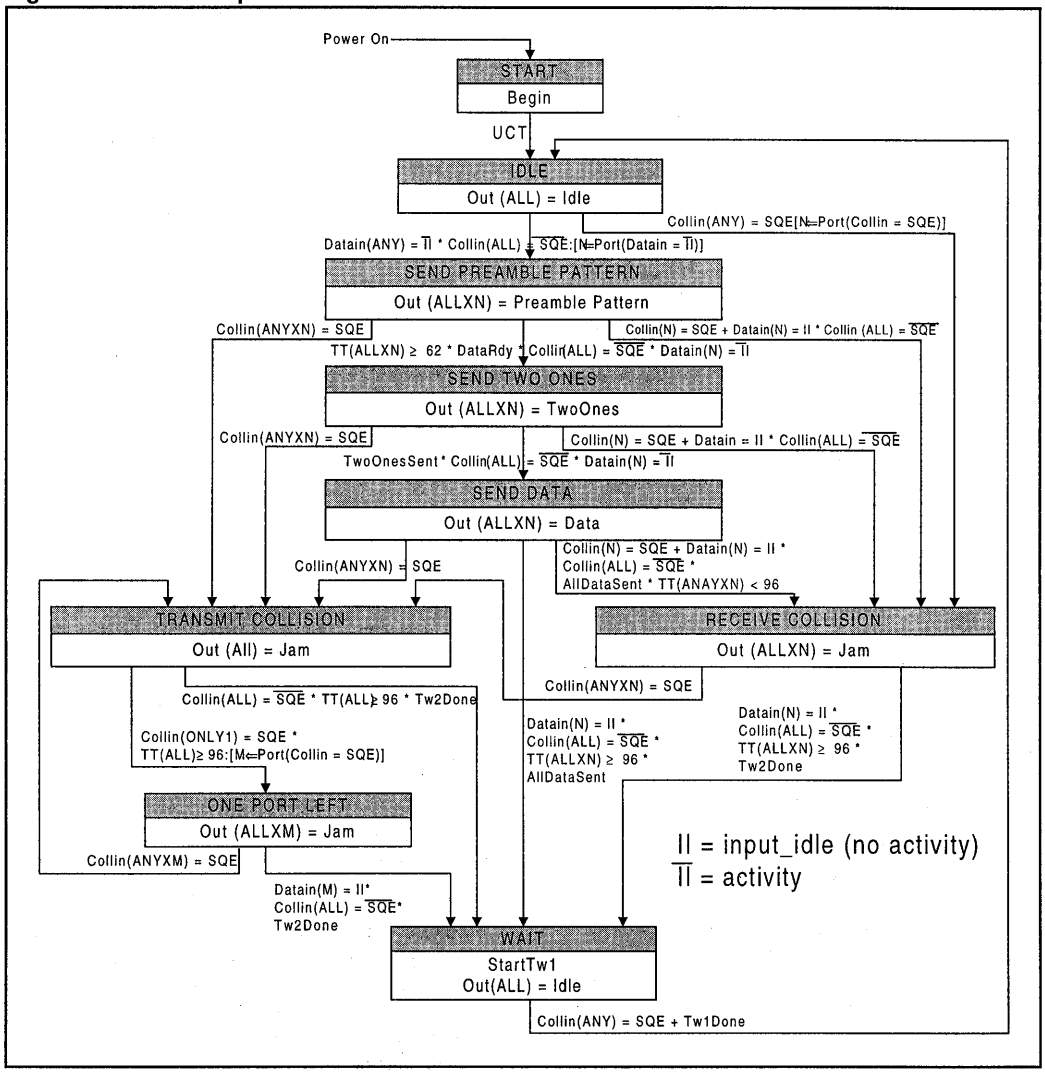
Manchester Code Violations

If the EMCV bit in the Master Configuration register is set, an input packet with Manchester Code Violations will be treated as a transmit collision. If this bit is clear (default), incoming packets with this type of error will simply be repeated to all ports. **Note that a packet that does not have a proper end-of-frame marker (2 bit times high with no transitions) will also be flagged as having a Manchester Code Violation.**

Data Rate Mismatches

Severe data rate mismatches will cause the internal fifo to underflow or overflow. Depending on the state of the EFIFOERR bit, these conditions can be treated either as transmit collision, or simply passed along as bad data.

Figure 3: LXT917 Repeater State Machine



Port Functions

Jabber (all ports)

If any input port is active for more than 5 ms, the device will automatically terminate all transmit activity for at least 96 bit times. This will give waiting ports an opportunity to access the network. A port that is continuously babbling will constantly collide with other ports, and will eventually be isolated by the auto-partitioning function.

Auto-partitioning (all ports)

Any port that causes 32 consecutive collisions will be *partitioned* as shown in Figure 4. A port will also be partitioned if it continues to be active for more than 100 us after a collision has occurred. Once a port is partitioned, data received from that port is not repeated, until the port is *re-connected.* There are two re-connection algorithms. The normal algorithm allows a port to be reconnected if a packet can be successfully transmitted or received from the port. The alternative algorithm allows re-connection only if a packet can be successfully transmitted to the port. For re-connection to occur, at least 512 bit times of non-idle, non-collision activity must occur. Once this happens, the port is re-connected after the activity stops. The activity that causes the re-connection is *not* repeated.

Link Integrity Function (10BASE-T ports only)

The device supports the Link Integrity function, which is used to determine if a 10BASE-T connection is working. The function can be enabled on a port-by-port basis. When enabled, the device looks for Link Integrity Pulses from each of the 10BASE-T ports. When these pulses are received from a port, it is put into the "Link Up" state, enabling transmissions to the port, and vice versa. If the Link Integrity function is disabled, the port is forced into the Link Up state. The device generates Link Pulses to all ports, regardless of the Link State of any port or whether the Link Function is enabled or disabled.

Polarity Detection and Correction (10BASE-T ports only)

The device can detect reversed polarity on any 10BASE-T port and internally correct for it. This function can also be disabled on a port-by-port basis.

SQE Mask (AUI Port only)

Ethernet MAU devices (also known as transceivers) typically generate an SQE signal (also called heartbeat) on the CI inputs after each data transmission to the MAU. This function is normally supposed to be disabled when a MAU is attached to a repeater, but often times this is overlooked. The result can be a collision at the end of each packet transmitted. An SQE Mask function is provided to overcome this problem. When the Mask is set, SQE heartbeat signals from external MAU's will not be passed on as collisions.

Reverse AUI Mode

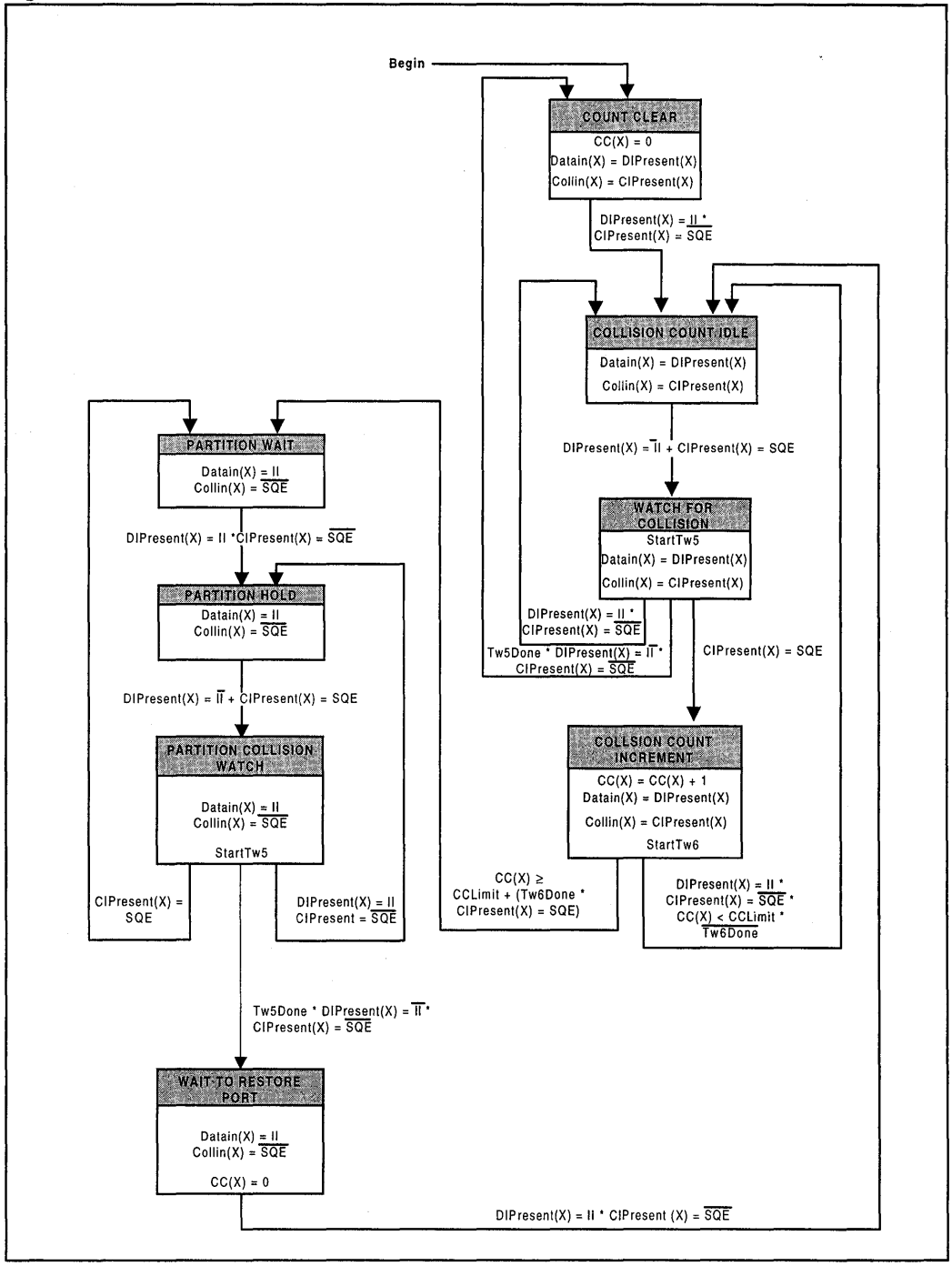
In the reverse mode, the AUI interface operates as a MAU rather than as a DTE. This allows it to directly interface to an LXT901/904/907. In this mode, the following apply:

- The CI pins function as outputs.
- The MaskSQE function determines whether or not the device generates SQE/heartbeat after each successful transmission to the device.
- The AUIDI pins continue to function as inputs, and the AUIDO pins continue to function as outputs. If these signals are being brought out to an external connector, they must be physically swapped from their normal positions (Refer to Figures 11 and 12.)
- The device will loopback data presented at the AUIDI inputs to the AUIDO outputs.

Reduced Squelch (10BASE-T ports only)

The squelch threshold on the 10BASE-T receivers can be lowered. This allows the device to detect weaker than normal signals, and can be used to support cables longer than 100m. It also makes the device more sensitive to cross-talk and other noise, and must be used with great care.

Figure 4: LXT917 Partition State Machine



LED FUNCTIONS

The LXT917 provides a serial LED output and two global LEDs. Two programmable blink rates are provided. Refer to Table 49 for details.

Serial LEDs

The LXT917 provides a serial LED interface which should be attached to an external shift register. This interface provides status LEDs for the 10BASE-T and AUI ports. It also provides a global fault LED, a redundant power supply (RPS) LED and a user definable LED. Refer to Figure 17 in the Application section, and to Tables 10 and 11 below for details on the serial LED interface.

Activity and Collision LEDs (global)

These outputs can directly drive LEDs to indicate activity and collision status.

Table 10: LED-DAT Serial Port Bit Assignments

15[1]	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RPS	GF	UD	AUI	TP12	TP11	TP10	TP9	TP8	TP7	TP6	TP5	TP4	TP3	TP2	TP1

1. Bit 15 is shifted out first.

Table 11: Serial LED Operational Modes

Bit	Name	SW Control	H/W Control		
			On	Slow	Off
15	RPS	N/A	Present, No Fault	Present & Fault	Any other state
14	Global Fault	On, Off or Slow Blink via Global LED Control Register, Address 181	N/A	Any Port Partitioned or RPS Fault	Any other state
13	User Definable		N/A		
12	AUI Port LEDs	On, Off or Fast Blink, via LED Control Register, Address 176	Enabled, Link Up, Not Partitioned	Partitioned	Any other state
11:0	TP Port LEDs				

IRB OPERATION

The Inter Repeater Backplane (IRB) allows multiple devices to operate as a single logical repeater, exchanging data collision status information. The IRB uses a combination of digital and analog signals as shown in Figure 5.

Data Handling

Three signals - $\overline{\text{IRENA}}$, IRDAT and IRCLK - are used to transmit data. All of them can be buffered between modules. A fourth signal - IRDEN - provides directional control of this buffer. IRDAT, $\overline{\text{IRENA}}$ and IRDEN need to be pulled high by 330 Ω resistors. During a collision, the LXT917 releases all four signals to prevent bus contention.

Collision Handling

Four signals - $\overline{\text{IRCOL}}$, $\overline{\text{IRCOLBP}}$, $\overline{\text{IRCFS}}$ and $\overline{\text{IRCFSBP}}$ - handle collisions. $\overline{\text{IRCFS}}$ and $\overline{\text{IRCOL}}$ should be connected between all the devices on any module. $\overline{\text{IRCFSBP}}$ and $\overline{\text{IRCOLBP}}$ should be connected between modules, to the devices that have ChipID = 0.

Collision States

There are three repeater collision states:

- Receive Collision - This occurs when an external transceiver detects a collision. On the LXT917, this can only happen on the AUI port.
- Transmit Collision - This occurs when two or more inputs become active at the same time.
- One Port Left - This is a special state that can occur after a Transmit Collision, when only one port remains active. This state prevents dead-locks in multiple-repeater configurations.

Collision Indications

$\overline{\text{IRCOL}}$ and $\overline{\text{IRCOLBP}}$ go low to indicate any collision (receive, transmit or one-port-left). $\overline{\text{IRCFS}}$ and $\overline{\text{IRCFSBP}}$ are three-state signals which are used to detect when a transmit collision occurs. The three states are:

- Idle (+5V). Indicates that no ports are active.
- Single drive (+2.8 volts). Indicates that exactly one port is active (normal data transmission, receive collision, or one-port-left).
- Multiple-drive (0 volts). Indicates that two or more ports are active (transmit collision).

$\overline{\text{IRCFSBP}}$ indicates the number of active drivers across all the ports in a repeater stack. $\overline{\text{IRCFS}}$ indicates the number of active drivers on the local board, and the first 96-bits of a non-local transmit collision (defined as a collision between a local port and a non-local port, or between two non-local ports). The state of $\overline{\text{IRCFS}}$ is fed forward to $\overline{\text{IRCFSBP}}$ by the device with ChipID = 0. To prevent dead-locks, $\overline{\text{IRCFSBP}}$ is NOT fed back to $\overline{\text{IRCFS}}$. During non-local transmit collisions, the signal HOLDCOL is used to hold the local devices in the transmit collision state. Table 12 summarizes the use of these signals.

Collision Hold (HOLDCOL)

The LXT917 can produce a HOLDCOL signal to prevent dead-locks between $\overline{\text{IRCFS}}$ and $\overline{\text{IRCFSBP}}$. The device with ChipID = 0 drives HOLDCOL high to indicate that a transmit collision is in progress, and that local devices should remain in the transmit collision state.

MAC IRB Access

The MACACTIV pin allows an external MAC or other digital ASIC to interface directly to the LXT917 IRB. When the MACACTIV pin is asserted, the LXT917 will drive the $\overline{\text{IRCFS}}$ and $\overline{\text{IRCFSBP}}$ signals on behalf of the external device, allowing it to participate in the transmit collision detection function of $\overline{\text{IRCFS}}$ and $\overline{\text{IRCFSBP}}$.

IRB Isolation

The ISOLATE output is provided to control the enable pins of external bidirectional transceivers. In multi-module applications, it can be used to isolate one module from the rest of the system. Only one device can control this signal. The output state of this pin is controlled by the Isolate bit in the Master Configuration Register.

MMSTRIN / MMSTROUT

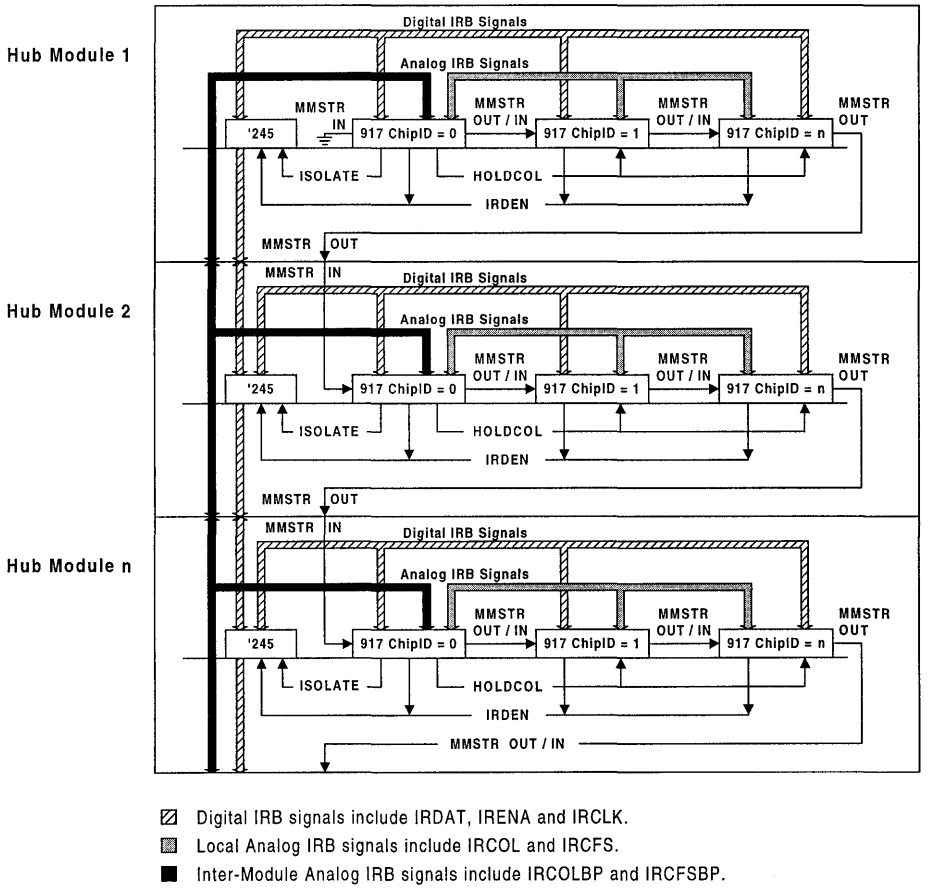
This daisy chain is provided for correct gathering of statistics in multiple-device configurations. In multiple-module applications, this daisy chain must be maintained across modules. In stand-alone applications, or for the first device in a chain, the MMSTRIN input must be pulled Low in order for the management counters to work correctly.

Table 12: $\overline{\text{IRCOL}}$ and $\overline{\text{IRCFS}}$ Condition Indications

Condition	$\overline{\text{IRCOLBP}}$	$\overline{\text{IRCOL}}$	$\overline{\text{IRCFSBP}}$	$\overline{\text{IRCFS}}$
Idle	High	High	High	High
Local Data	High	High	Mid	Mid
Non-Local Data	High	High	Mid	High
Local RxCol or OPL [1]	Low	Low	Mid	Mid
Non-local RxCol/OPL [1]	Low	Low	Mid	High
Local TxCol or first 96 bits of non-local TxCol [2]	Low	Low	Low	Low
Non-local TxCol after 96 bits [2]	Low	Low	Low	Mid or High

1. Receive Collision (RxCol) and One Port Left (OPL) conditions have identical bus characteristics and can be differentiated only by timing. Fragment extensions are generally treated as receive collisions.
2. Manchester code violations and fifo overruns are generally treated as transmit collisions.

Figure 5: IRB Block Diagram

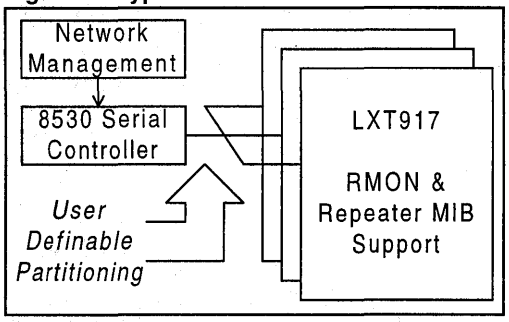


SERIAL MANAGEMENT I/F

The serial management interface provides access to Repeater MIB variables, RMON Statistics attributes and status and control information. A network manager can access the interface through a simple serial communications controller. The interface is designed to be used in a multi-drop configuration, allowing multiple LXT917 devices to be managed from one common line.

The interface consists of a data input line (SRX), data output line (STX) and a clock (SERCLK), and can operate up to 1 Mbps. The interface operates on a simple command response model, with the network manager as the master and the LXT917 devices as slaves. Figure 6 is a simplified view of typical serial management interface architecture.

Figure 6: Typical Serial I/F Architecture



Serial Clock

SERCLK is a bidirectional pin; direction control is provided by the RECONFIG input. If RECONFIG is High, the LXT917 will drive SERCLK at 625 kHz. If RECONFIG is Low, SERCLK is an input, between 0 and 1 MHz. There is no lower bound to how slow the interface can operate. The clock can be stopped after each operation, as long as an idle (ten 1's in a row) is transmitted first.

Serial Data I/O

The serial data pins, SRX and STX, should be tied together. The SRX input is compared with the STX output. If a mismatch occurs, STX goes to a high impedance. STX is driven on the falling edge of SERCLK. SRX is sampled on the rising edge.

Management Format

Normally the network manager directs read and write operations to a specific LXT917 device using a two-part address consisting of HubID and ChipID. The interface allows up to 127 32-bit registers to be read at one time. Up to two registers can be written at a time.

The interface uses a simple frame format, which is shown in Figure 7. All frames begin and end with a flag of consisting of "01111110". All fields are transmitted LSB first. Zero-bit stuffing is required if more than five 1's in a row appear in the header, data or CRC fields. In addition, all operations directed to the device must be followed by an idle (ten 1's in a row), and the first operation must be preceded with an idle.

Figure 7: Serial Management Frame Format

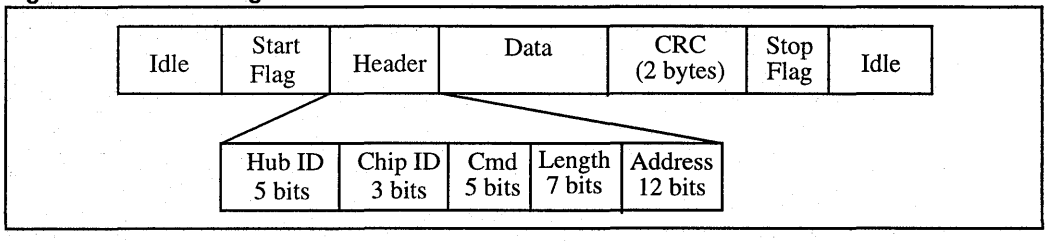


Table 13: Serial Management Frame Message Fields

Message	Description
Start or Stop Flag	"01111110". Protocol requires zero insertion after any five consecutive "1's" in the data stream.
Hub ID	Identifies module or sub-system. Assigned by one of two arbitration mechanisms at power-up.
Chip ID	Identifies one of eight modules on a system. Assigned by 3 external pins on each device.
Command	Identifies the particular operation being performed (see Table 14)
Length	Specifies number of registers to be transferred (1 to 127). Maximum is 2 per write, 127 per read.
Address	Specifies address of register or register block to be transferred.

1. All fields are transmitted LSB first.

Table 14: Serial Management Instruction Set

Command Value	Name	Usage	Normally Sent By	Description
18 (Hex)	Write	Normal Ops	Network Mgr	Used to write up to 2 registers (8 bytes) at a time.
04 (Hex)	Read	Normal Ops	Network Mgr	Used to read up to 127 registers at a time.
08 (Hex)	RequestID	Arbitration	LXT917	Requests Hub ID. Repeated periodically.
00 (Hex)	ConfigChg	Arbitration	LXT917	Notifies system of configuration change (hot swap). Requests new arbitration phase.
10 (Hex)	Re-arbitrate	Arbitration	Network Mgr	Re-starts arbitration
14 (Hex)	Assign HubID	Arbitration Mech. 2	Network Mgr	Assigns Hub ID to device with ARBIN=0 and ARBOUT = 1 (top of chain)
0C (Hex)	Set Arbout to 1	Arbitration Mech. 2	Network Mgr	Commands specific device to set ARBOUT to 1.
1C (Hex)	Set Arbout to 0	Arbitration Mech. 2	Network Mgr	Commands specific device to set ARBOUT to 0
02 (Hex)	DevID	Config	Network Mgr	Generic command for reading device type (no register address needed).

Table 15: Typical Serial Management Packets

Message	Contents of Fields in Serial Management Packet					
	Hub ID	Chip ID	Command	Length	Address	Data
Write	User Defined	User Defined	18 (Hex)	01 or 02	User Defined	User Defined
Read Request	User Defined	User Defined	04 (Hex)	01 to 7F Hex	User Defined	Null
Read Response	00000	000	04 (Hex)	Echo	Echo	Data Values
Assign Hub ID (Arb Method 1)	11111	111	18 (Hex)	02	188 Hex	Formatted per Table 51
Assign Hub ID (Arb Method 2)	11111	111	14 (Hex)	01	0	Hub ID (LSB) and 27 0's
Set Arbout to 1	User Defined	User Defined	0C (Hex)	00	0	Null
Set Arbout to 0	User Defined	User Defined	1C (Hex)	00	0	Null
Arb Request	00000	000	08 (Hex)	02	190	PROM ID
Re-Arbitrate	11111	111	10 (Hex)	00	0	Null
Request Device ID	User Defined	User Defined	02 (Hex)	01	0	Null
Device ID Response	00000	000	02 (Hex)	01	185	Formatted per Table 50
Config Change	13 0's					

Address Arbitration

Each device has a two part address, consisting of a HubID and a ChipID. The ChipID is assigned the input pins CHIPID<2:0>. The HubID is assigned through one of two arbitration mechanisms.

Arbitration Mechanism #1 - EPROM method

This method requires that a PROM be located on each module, and that the ARBSELECT pin (71) not be pulled Low. At power-up, the device with ChipID = 0 reads a 48-bit ID from the PROM. All other devices on the module listen in and also record this ID. The device with ChipID = 0 then transmits "Arbitration Request Messages" on the Serial Management Interface every 2-3 milliseconds. The request messages from two modules may collide; if this happens a resolution scheme ensures that only one message will win (see Figure 8). The network manager responds to each request with a message that includes the 48-bit ID and the HubID. All devices hear this message, but only those that match the 48-bit ID receive the HubID as their own. Once the HubID is assigned, the device with ChipID=0 stops sending request messages. It is possible for response messages to be lost due to collisions with request messages.

Arbitration Mechanism #2 - Chain method

In this method, all of the devices are daisy-chained using the ARBIN and ARBOUT pins. This scenario is shown in Figure 9. The ARBIN input of the first device is directly connected to an output of the network manager. At power-up all the devices drive their ARBOUT outputs High while the network manager drives the ARBIN input to the first device Low. The manager transmits a special "Assign Hub ID" message which is recognized only by the device with ARBIN = Low and ARBOUT = High. The network manager then sends a command addressed to this device which commands it to set its ARBOUT pin Low. This cycle repeats until all devices have been assigned a HubID.

Address Re-arbitration

There are two mechanisms for address re-arbitration following a configuration change, such as a hot-swap of a module:

- Device power up - At power-up, the LXT917 normally sends out a "Configuration Change" message (all 0's) on the bus, which causes re-arbitration.
- The network manager can direct or re-start arbitration at any time by sending the "Re-arbitrate" command.

SOURCE ADDRESS UTILITY FUNCTIONS

Source Address Tracking Function

Each port has two source address tracking registers. The rptrAddrTrackNewLastSrcAddress register for each port continuously tracks the source addresses of packets emanating from that port. The Authorized Address Register operates in three modes: it can free run, lock, or lock on the next packet. In any mode, it can always be updated by network management.

Source Address Matching Function

The LXT917 has a Source Address Matching Function to discover which port or ports sourced packets with a particular Source Address. The input to the function is an Ethernet Address; the output is a register which identifies any ports that sourced packets with that Source Address.

Figure 8: Arbitration Mechanism #1 - Collision Resolution

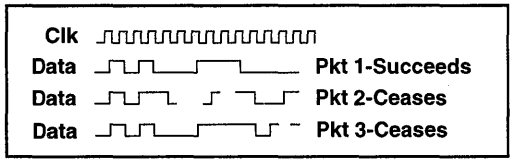
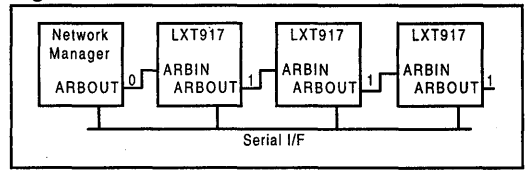


Figure 9: Arbitration Mechanism #2



APPLICATION INFORMATION

MAGNETICS INFORMATION

The LXT917 requires a 1:1 ratio for the TP receive transformers and a 1:1.41 ratio for the TP transmit transformers. Table 16 lists suitable transformers by manufacturer and part number. This information was valid as of the printing date of this document. Before committing to a specific component, designers should contact the manufacturer for current product specifications, and should test and validate the magnetics for the specific application to verify that system requirements are met.

LAYOUT REQUIREMENTS

The Twisted Pair Interface

The layout of the twisted-pair port is critical in complex designs. Run the traces directly from the LXT917 to the discrete termination components (located close to the transformers).

The transformer isolation voltage should be rated at 2 kV to protect the circuitry from static voltages across the connectors and cables. The traces running from the transformers to the connector should run in close pairs directly to the connector. Be careful not to cross the transmit and receive pairs. One way to avoid this problem is to run the receive pairs on the component side and the transmit pairs on the solder side. Careful planning during the schematic and layout stages can avoid these problems.

The PCB layout should have no ground or power planes between the transformers and the connectors. The data signals should be the only traces in this area. Place the chassis ground for the connectors near the edge of the PCB, away from the signals, connecting the connector shield with the chassis.

The RBIAS Pin

The RBIAS signal sets the levels for the output drivers. Any emissions or common mode noise entering the device here could be measured on the twisted pair output signals.

The LXT917 requires a 22 kΩ, 1% resistor directly connected between the RBIAS pin and ground. These traces should be as short as possible. The ground traces from adjacent GND pins should come directly off of the device to enclose the resistor and pin forming a shielded area between the RBIAS connection and other signals on the PCB.

TYPICAL APPLICATION CIRCUITRY

Figures 10 through 17 show typical LXT917 application circuitry. Table 17 summarizes signal operation of the three AUI signal pairs in the two modes (normal and reversed).

Table 16: Suggested Magnetics List[1]

Manufacturer	Quad Transmit	Quad Receive	Quad Tx/Rx (Octal)
BEL	S553-5999-02	S553-5999-03	
HALO	TD54-1006L1 TG54-1006N2	TD01-1006L1 TG01-1006N2	TG44-S010NX TG45-S010NX TG46-S010NX
Nanopulse	5976	5977	
Kappa	TP4003P	TP497P101	
PCA	EPE6009	EPE6010	
TDK	TLA-3T107	TLA-3T106	
VALOR	PT4116	PT4117	

1. Before committing to a specific component, designers should contact the manufacturer for current product specifications, and should test and validate the magnetics for the specific application to verify that system requirements are met.

Figure 10: Typical 10BASE-T Port Interface

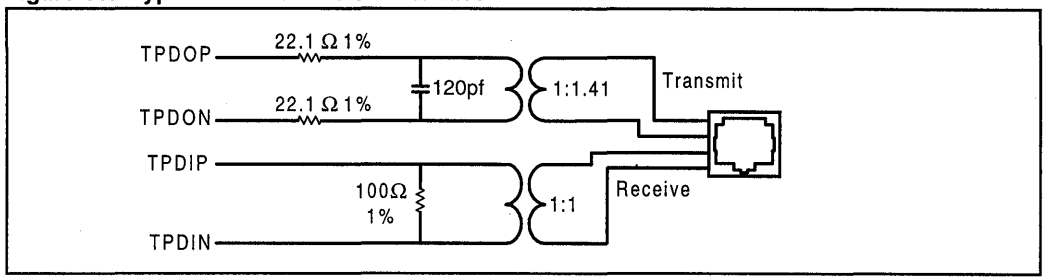


Figure 11: Normal AUI Circuit

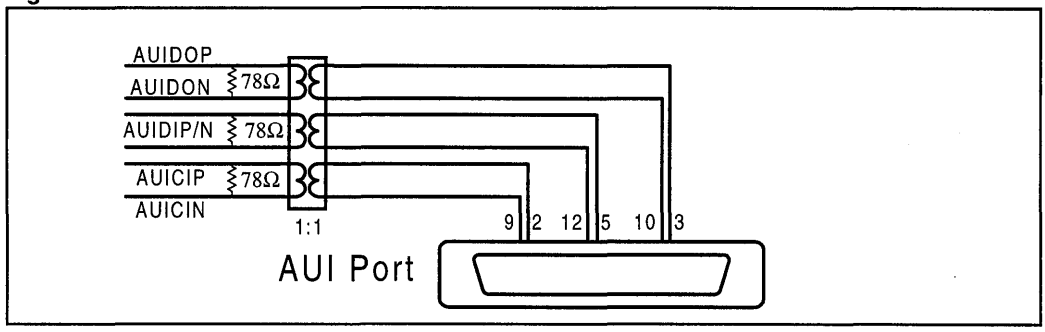


Figure 12: Reversed AUI Circuit

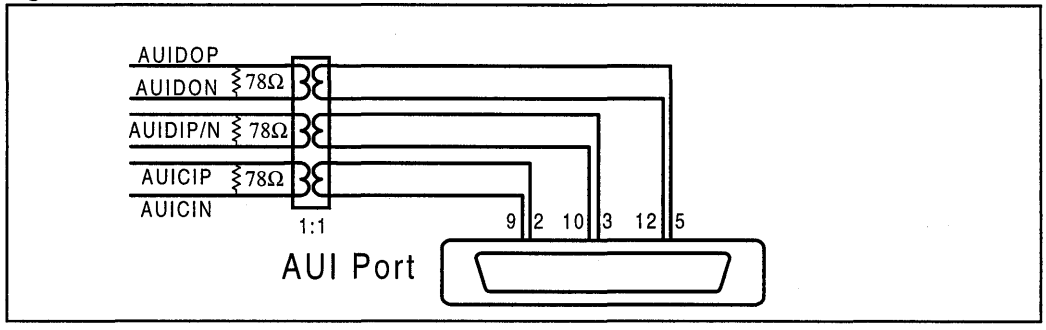


Table 17: AUI Signals - Direction and Pin-Out

LXT917		AUI Connector Pin #	
Signal	**Pin #**	**Normal**	**Reversed**
DOP DON	198 199	3 10	5 12
DIP DIN	200 201	5 12	3 10
CIP CIN	202 203	2 9	2 9

Figure 13: Typical IRB Implementation

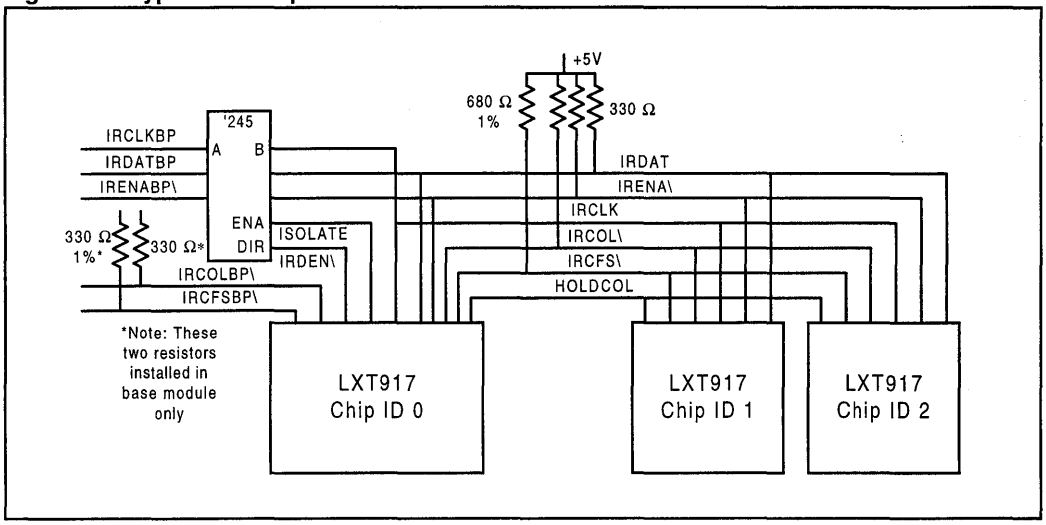


Figure 14: Typical Serial Management Interface Connections

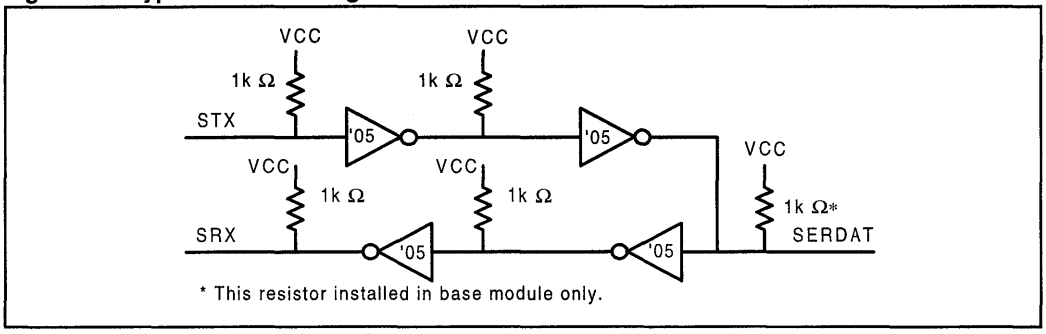
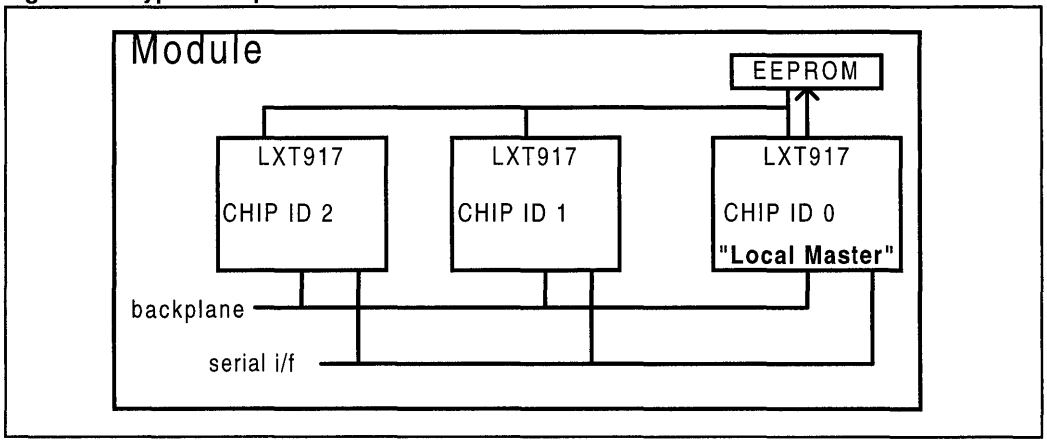


Figure 15: Typical Chip ID Architecture



12

Figure 16: Typical EPROM Circuit

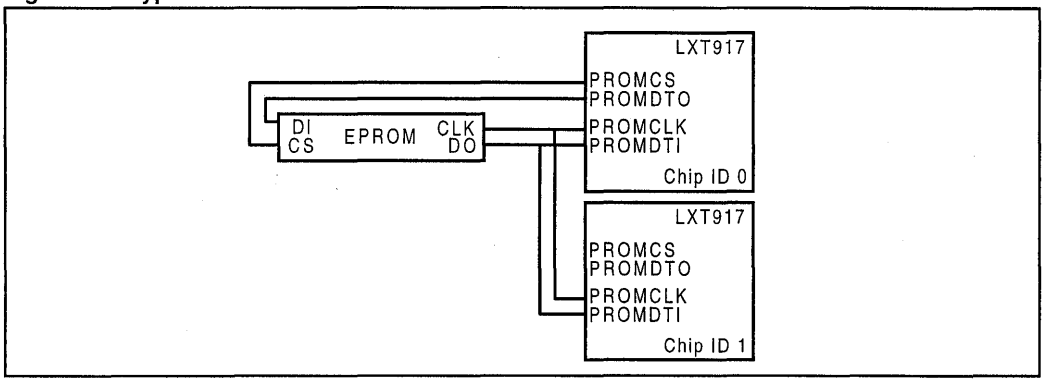


Figure 17: Typical Serial LED Interface Circuit

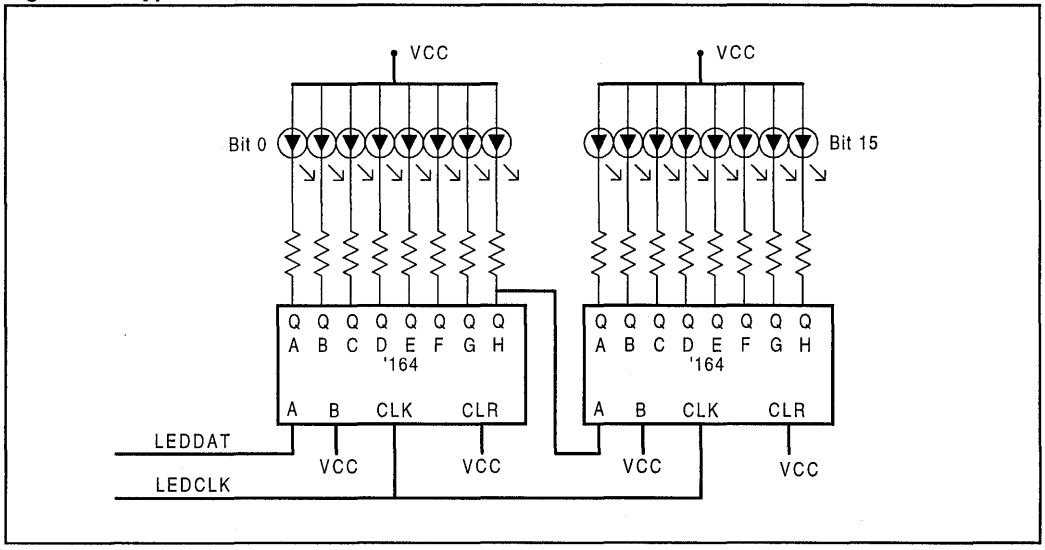
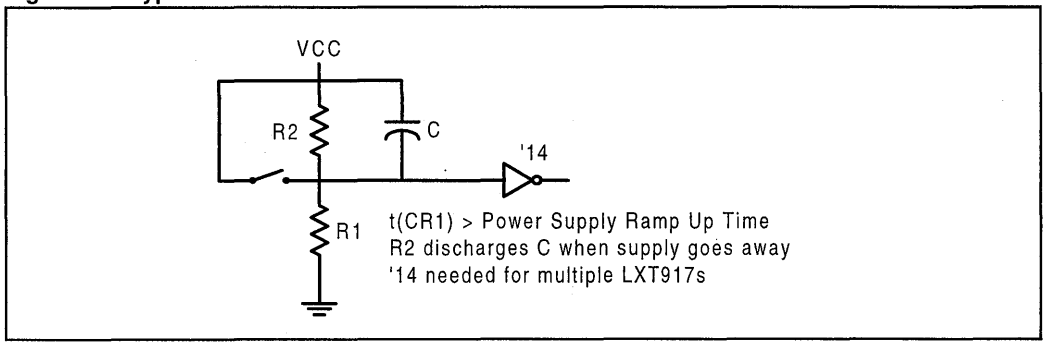


Figure 18: Typical Reset Circuit



TEST SPECIFICATIONS

Note

Minimum and maximum values in Tables 18 through 28 and Figures 19 through 23 represent the performance specifications of the LXT917/916 and are guaranteed by test except, where noted, by design.

Table 18: Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Supply voltage	VCC	-0.3	6	V
Operating temperature	TOP	0	70	°C
Storage temperature	TST	-65	+150	°C
CAUTION Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.				

Table 19: Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Recommended supply voltage[1]	VCC	4.75	5.0	5.25	V	
Recommended operating temperature	TOP	0	–	70	°C	
VCC current	ICC	–	400	–	mA	

1. Voltages with respect to ground unless otherwise specified.

Table 20: I/O Electrical Characteristics *(Over Recommended Range)*

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Input Low voltage	VIL	–	–	0.8	V	TTL inputs
		–	–	2.0	V	CMOS inputs [2]
		–	–	1.0	V	Schmitt Trigger #1
		–	–	1.0	V	Schmitt Trigger #2
Input High voltage	VIH	2.0	–	–	V	TTL inputs
		VCC-2.0	–	–	V	CMOS inputs [2]
		VCC-1.0	–	–	V	Schmitt Trigger #1
		VCC-2.0	–	–	V	Schmitt Trigger #2
Hysteresis voltage	–	1.0	–	–	V	Schmitt Trigger #1
		0.5	–	–	V	Schmitt Trigger #2

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Does not apply to IRB pins. Refer to Table 23 for IRB I/O characteristics.

Table 20: I/O Electrical Characteristics *(Over Recommended Range)– continued*

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Output Low voltage	V_{OL}	–	–	0.4	V	I_{OL} = 1.6 mA
Output Low voltage (LED)	V_{OLL}	–	–	1.0	V	I_{OLL} = 10 mA
Output High voltage	V_{OH}	2.4	–	–	V	I_{OH} = 40 µA
Input Low current	I_{IL}	-100	–	–	µA	
Input High current	I_{IH}	–	–	100	µA	
Output rise / fall time	–	–	3	10	ns	C_{LOAD} = 15 pF

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Does not apply to IRB pins. Refer to Table 23 for IRB I/O characteristics.

Table 21: 10BASE-T Electrical Characteristics *(Over Recommended Range)*

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Transmitter						
Transmit output impedance	Z_{OUT}	–	2	–	Ω	
Peak differential output voltage	V_{OD}	2.2	2.5	2.8	V	Load = 100Ω at TPOP/TPON
Transmit timing jitter addition	–	–	±2	±10	ns	0 line length for internal MAU
Transmit timing jitter added by the MAU and PLS sections	–	–	±1	±5.5	ns	After line model specified by IEEE 802.3 for 10BASE-T internal MAU
Receiver						
Receive input impedance	Z_{IN}	20	36	–	kΩ	Between TPIP/TPIN
Differential squelch threshold - Normal	V_{DSN}	300	420	585	mV	5 MHz square wave input
Differential squelch threshold - Reduced	V_{DSR}	150	250	350	mV	5 MHz square wave input

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 22: AUI Electrical Characteristics *(Over Recommended Range)*

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Differential output voltage	V_{OD}	±550	–	±1200	mV	
Receive input impedance	Z_{IN}	20	36	–	kΩ	Between CIP/CIN & DIP/DIN
Differential squelch threshold	V_{DS}	150	250	350	mV	

1. Typical values are at 25° C and are for design aid only; they are not guaranteed and not subject to production testing.

Table 23: IRB Electrical Characteristics *(Over Recommended Range)*

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Output Low voltage	VOL	–	.3	.7	V	RL = 330 Ω
Output rise or fall time	TF	–	4	10	ns	CL = 15 pF
Input High voltage	VIH	VCC - 2.0	–	–	V	CMOS inputs
Input Low voltage	VIL	–	–	2.0	V	CMOS inputs
$\overline{\text{IRCFS}}$ current		2.6	3.3	4.0	mA	RL = 680 Ω
$\overline{\text{IRCFSBP}}$ current		5.4	6.7	8.3	mA	RL = 330 Ω

1. Typical values are at 25° C and are for design aid only; they are not guaranteed and not subject to production testing.

Table 24: Repeater Timing Characteristics[1] *(Over Recommended Range)*

Parameter	Symbol	Min	Typ[2]	Max	Units	Test Conditions
AUI DIN active to $\overline{\text{IRENA}}$ Low	trep1	–	2	3	BT[4]	
TP DIN to $\overline{\text{IRENA}}$ Low	trep2	–	5	7	BT	
$\overline{\text{IRENA}}$ Low to AUI DOP active	trep3	–	3	4	BT	
$\overline{\text{IRENA}}$ Low to TP DOP active	trep4	–	4	5	BT	
IRCLK rising edge to IRDAT rising edge.	trep5	25	–	55	ns	330 Ω pullup, 150 pF load on IRDAT. 1k Ω pullup, 150 pF load on IRCLK. All measurements at 2.5V.
IRCLK rising edge to IRDAT falling edge.	trep6	5	–	25	ns	
AUI DIN idle to $\overline{\text{IRENA}}$ High	trep7	–	–	8	BT	
TP DIN idle to $\overline{\text{IRENA}}$ High	trep8	–	–	11	BT	
$\overline{\text{IRENA}}$ High to AUI DOP idle	trep9	–	–	5	BT	
$\overline{\text{IRENA}}$ High to TP DOP idle	trep10	–	–	5	BT	

1. This table contains propagation delays from the TP and AUI ports to the IRB, and from the IRB to the AUI and TP ports, for normal repeater operation (start of packet, end of packet). All values in this table are output timings.
2. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
3. There is a delay of approximately 13 to 16 bit times between the assertion of $\overline{\text{IRENA}}$ and the assertion of IRCLK and IRDAT. This delay does not affect repeater operation because downstream devices begin generating preamble as soon as $\overline{\text{IRENA}}$ is asserted.
4. BT = Bit Times (100 ns).

Figure 19: Repeater Timing

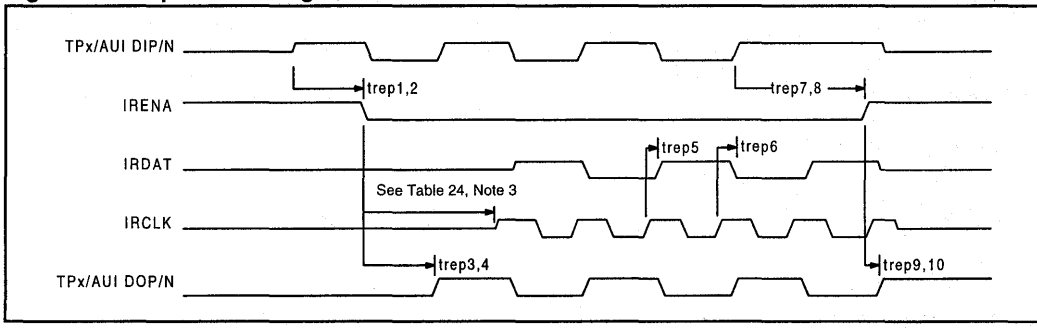


Table 25: MAC I/F Transmit Timing Characteristics [1] *(Over Recommended Range)*

Parameter	Symbol	Min	Typ[2]	Max	Units	Test Conditions
TXD to TXC setup time	tmactx1	20	–	–	ns	TXD valid to TXC rising edge [3]
TXC to TXD hold time	tmactx2	5	–	–	ns	TXC rising edge to TXD change [3]
TXE to TP DOP prop delay	tmactx3	–	6	7	BT	TXE High to TPDOP active [4]

1. This table contains propagation delay times for the 7-pin MAC interface.
2. Typical values are at 25° C and are for design aid only; they are not guaranteed and not subject to production testing.
3. Input.
4. Output.

Figure 20: MAC I/F Transmit Timing

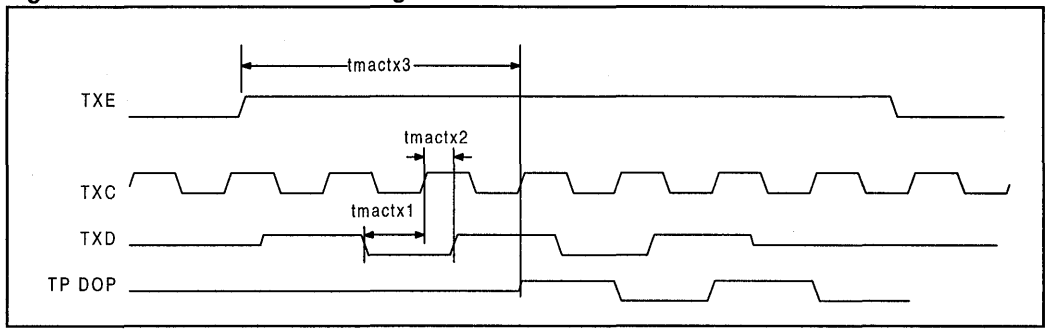


Table 26: MAC I/F Receive Timing Characteristics [1] *(Over Recommended Range)*

Parameter	Symbol	Min	Typ[2]	Max	Units	Test Conditions
RXC to RXD prop delay	tmacrx1	–	–	10	ns	Falling edge of RXC to RXD valid
TP/AUI to CRS delay	tmacrx2	–	9	10	BT	TP/AUI DIP active to CRS High
Number of extra receive clocks	tmacrx3	–	5	–	ea	RXC rising edges after CRS Low

1. This table contains propagation delay times for the 7-pin MAC interface outputs.
2. Typical values are at 25° C and are for design aid only; they are not guaranteed and not subject to production testing.

Figure 21: MAC I/F Receive Timing

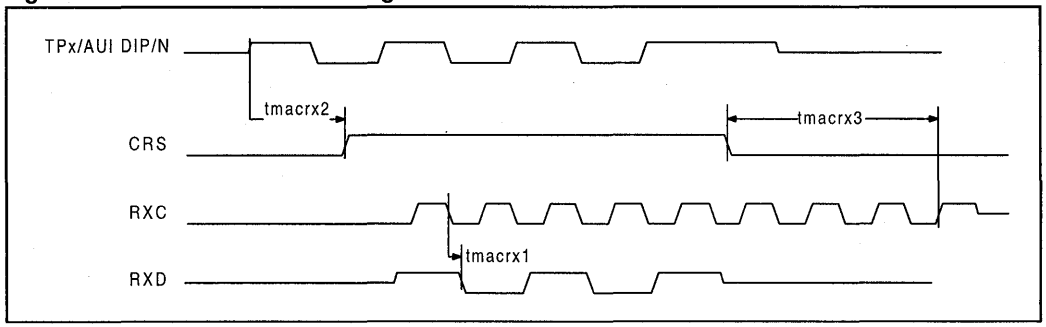


Table 27: MACACTIVE Delays - MAC/IRB Interface Characteristics *(Over Recommended Range)*

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
MACACTIV to $\overline{\text{IRENA}}$ assertion delay [3]	tmacbp1	–	100	–	ns	MACACTIV High to $\overline{\text{IRENA}}$ Low [2]
IRDAT to IRCLK setup time	tmacbp2	21	–	–	ns	IRDAT valid to IRCLK rising edge [2]
IRDAT to IRCLK hold time	tmacbp3	0	–	–	ns	IRCLK rising edge to IRDAT change [2]

1. Typical values are at 25° C and are for design aid only; they are not guaranteed and not subject to production testing.
2. Input.
3. External devices should allow at least one 10 MHz clock cycle (10 ns) between assertion of MACACTIV and $\overline{\text{IRENA}}$.

Figure 22: MACACTIVE Timing (MAC to IRB Interface)

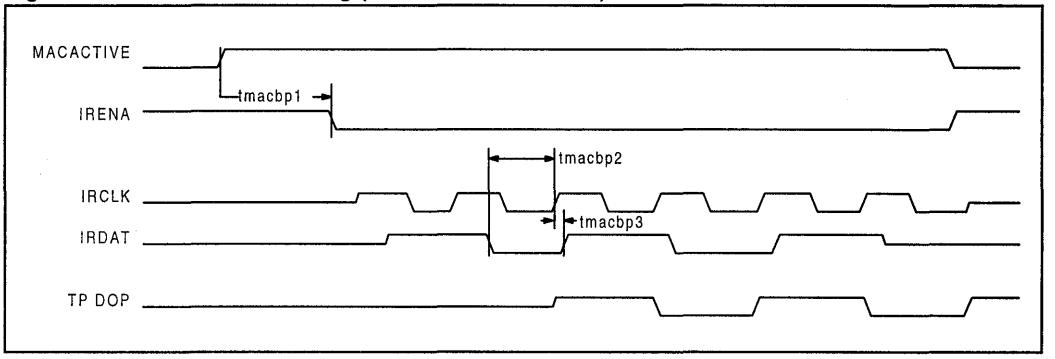
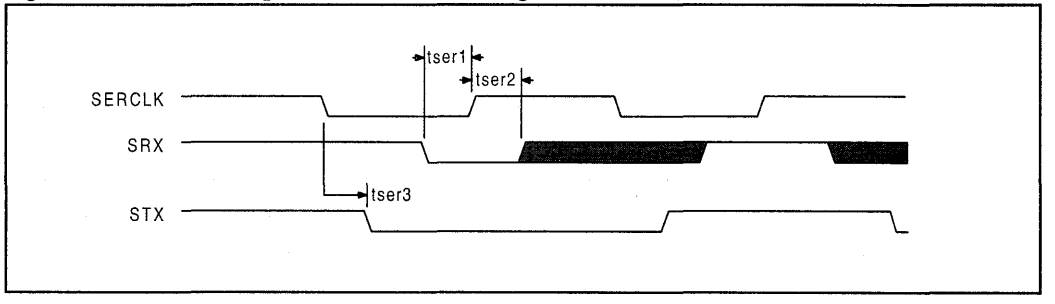


Table 28: Serial Management Interface Timing Characteristics *(Over Recommended Range)*

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Data to Clock setup	tser1	100	–	–	ns	SRX valid to SERCLK rising edge [2]
Clock to Data Hold Time	tser2	100	–	–	ns	SERCLK rising edge to SRX change [2]
Data Propagation Delay	tser3	–	–	100	ns	SERCLK falling edge to STX valid [3]

1. Typical values are at 25° C and are for design aid only; they are not guaranteed and not subject to production testing.
2. Input.
3. Output.

Figure 23: Serial Management Interface Timing



REGISTER DEFINITIONS

The LXT917 register set is composed of multiple 32-bit registers of the following types:

- Configuration Registers
- Control and Status Registers
- Ethernet Address Registers
- Counters

Table 29 lists the register base memory locations. Refer to Tables 30 through 54 for specific addresses and bit assignments.

Table 29: Memory Map

Base Address	Register Type	Notes
181	Configuration	11 Registers
170	Control and Status	9 Control Registers, 7 Status Registers
156	Ethernet Address	3 Search Registers
13C		Authorized Port Address, 2 per port (TP and AUI)
120		Port Address Tracking, 2 per port (TP, AUI and MAC)
118	Counters	MAC I/F Counters, 8 Registers
100		Reserved
0F0		Reserved
0E0		Reserved
0D0		Interface Counters, 18 Registers
0C0		AUI Port Counters, 15 Registers
0B0		TP Port 12 Counters, LXT917 Only, 15 Registers.
0A0		TP Port 11 Counters, LXT917 Only, 15 Registers.
090		TP Port 10 Counters, LXT917 Only, 15 Registers.
080		TP Port 9 Counters, LXT917 Only, 15 Registers.
070		TP Port 8 Counters, 15 Registers.
060		TP Port 7 Counters, 15 Registers.
050		TP Port 6 Counters, 15 Registers.
040		TP Port 5 Counters, 15 Registers.
030		TP Port 4 Counters, 15 Registers.
020		TP Port 3 Counters, 15 Registers.
010		TP Port 2 Counters, 15 Registers.
000		TP Port 1 Counters, 15 Registers.

COUNTER REGISTERS

As shown in Table 30, all counters are 32-bit, read-only, "little-Endian" registers, with undetermined values at power-up. The "Zero Counters" bit in the Master Configuration Register allows all counters to be "zeroed".

Table 30: Counter Registers Bit Assignments

31	30	29	28	27	26	25 : 7	6	5	4	3	2	1	0
D31	D30	D29	D28	D27	D26	D25:D7	D6	D5	D4	D3	D2	D1	D0

Port Counter Registers

Table 31 contains descriptions of the per-port counters for the TP ports and the AUI port. These descriptions are intended to be illustrative. For the exact definitions of these counters, refer to the Repeater MIB, RFC 1516. All counters count packets, octets or events that were received at each port. In the descriptions, the length of a packet never includes preamble or framing bits (start-of-frame, end-of-frame, dribble bits, etc.), but an "event" does include these items..

Table 31: Port Counter Registers

Name	Address	Description[1]
rptrMonitorPortReadableFrames	000	Counts valid-length (64 to 1518 bytes), valid-CRC, collision-free packets. Depending on the state of the CountMode bit in the Master Configuration Register, this counter will count either all packets (CountMode=0) or only Unicast Packets (CountMode=1) Minimum roll-over time = 80 hours
rptrMonitorPortReadableOctets	001	Counts the number of octets in the packets counted by the rptr-MonitorPortReadableFrames counter, not including preamble and framing bits. Minimum roll-over time = 58 minutes.
rptrMonitorPortFrameCheckSequence	002	Counts valid length, collision-free packets that had FCS errors, but were correctly framed (had an integral number of octets). Minimum roll-over time = 80 hours.
rptrMonitorPortAlignmentErrors	003	Counts valid length, collision-free packets that had FCS errors and were incorrectly framed (had a non-integral number of octets) . Minimum roll-over time = 80 hours.
rptrMonitorPortFramesTooLong	004	Counts packets that had a length greater than 1518 octets. Minimum roll-over time = 61 days.
rptrMonitorPortShortEvents	005	Counts events that lasted for 82 bit times or less. Minimum roll-over time = 16 hours.
rptrMonitorPortRunts	006	Counts events longer than 82 bit times, but shorter than 512 bit times. Minimum roll-over time = 16 hours.
rptrMonitorPortCollisions	007	Counts the number of collisions that occurred, not including late collisions. Minimum roll-over time = 16 hours.
rptrMonitorPortLateEvents	008	Counts the number of times collision was detected more than 512 bit times after the start of carrier. Minimum roll-over time = 81 hours.

1. All Port Counters are Read Only.

Table 31: Port Counter Registers– *continued*

Name	Address	Description[1]
rptrMonitorPortVeryLongEvents	009	Counts the number of times any activity continued for more than 4 to 7.5 ms. Minimum roll-over time = 198 days.
rptrMonitorPortDataRateMismatches	00A	Counts the number of times the incoming data rate mismatched the local clock source enough to cause a fifo underflow or overflow.
rptrMonitorPortAutoPartitions	00B	Counts the number of times this port has been partitioned by the Auto-partition algorithm.
rptrTrackSourceAddrChanges	00C	Counts the number of times the source address has changed. Minimum roll-over time of 81 hours.
rptrMonitorPortBroadcastPkts	00D	Counts the number of good broadcast packets received by this port.
rptrMonitorPortMulticastPkts	00E	Counts the number of good multicast packets received by this port.

1. All Port Counters are Read Only.

Interface Counter Registers

Table 32 contains descriptions of the interface counters, which are intended to be illustrative. For the exact definition of these counters, refer to the RMON MIB, RFC 1757. All counters count events, octets or packets that were received from the interface. Packet length never includes preamble or framing bits (start-of-frame, end-of-frame, dribble bits, etc.).

Table 32: Interface Counter Registers

Name	Address	Description[2]
etherStatsOctets	0D0	The number of data octets including those in bad packets and octets in FCS fields, but does not include preamble or other framing bits.
etherStatsPkts	0D1	The number of packets received from the network, including errored packets.
etherStatsBroadcastPkts	0D2	The number of good broadcast packets received.
etherStatsMulticastPkts	0D3	The number of good multicast packets received.
etherStatsCRCAlignErrors	0D4	The number of valid-length packets (64 to 1518 bytes inclusive) that had a bad Frame Check Sequence (FCS).
etherStatsUndersizePkts	0D5	The number of well-formed packets that were smaller than 64 octets.
etherStatsOversizePkts	0D6	The number of well-formed packets that were longer than 1518 octets.
etherStatsFragments	0D7	The number of ill-formed packets less than 64 octets. Note: Any event without a start-of-frame delimiter (0-octet packet) will be counted as a fragment, no matter how long it is.
etherStatsJabbers	0D8	The number of ill-formed packets longer than 1518 octets. An ill-formed packet is one with an FCS error.
etherStatsCollisions	0D9	The best estimate of the total number of collisions on this interface.
etherStatsPkts64Octets	0DA	The number of packets (good and bad) that were 64 octets long.

1. All Interface Counters are Read Only

Table 32: Interface Counter Registers– *continued*

Name	Address	Description[2]
etherStatsPkts65to127Octets	0DB	The number of packets (good and bad) between 65 and 127 octets long.
etherStatsPkts128to255Octets	0DC	The number of packets (good and bad) between 128 and 255 octets long.
etherStatsPkts256to511Octets	0DD	The number of packets (good and bad) between 256 and 511 octets long.
etherStatsPkts512to1023Octets	0DE	The number of packets (good and bad) between 512 and 1023 octets long.
etherStatsPkts1024to1518Octets	0DF	The number of packets (good and bad) between 1024 and 1518 octets long.
rptrMonitorTotalOctets	110	The total number of octets received.
rptrMonitorTransmitCollisions	114	The total number of transmit collisions that occurred.

1. All Interface Counters are Read Only

Port Counters for the 7-pin MAC Interface

Port Counters for the 7-pin MAC Interface are described in Table 33. These counters are a subset of the port counters for the other ports. Refer to Table 30 for bit assignments.

Table 33: MAC Interface Registers

Name	Type[1]	Addr	Description
MAC I/F-ReadableFrames	R	118	Valid-length (64 to 1518 bytes), valid-CRC, non-collision frames. Depending on the state of the CountMode bit in the Master Configuration Register, this counter counts either all valid packets (CountMode=0) or Unicast packets only (CountMode=1). Minimum roll-over time = 80 hours.
MAC I/F-ReadableOctets	R	119	Octets contained in MAC I/F-ReadableFrames. Minimum roll-over time = 58 minutes.
MAC I/F-Runts	R	11A	Number of packets and events shorter than 512 bit times. Minimum roll-over time = 16 hours.
MAC I/F-Collisions	R	11B	Number of collisions that were detected on this interface. Minimum roll-over time = 16 hours.
MAC I/F-FCS/FAE	R	11C	Valid length (64-1518 bytes), non-collision packets with FCS errors. Minimum roll-over time = 80 hours.
MAC I/F-Broadcast	R	11D	Number of good broadcast packets received from this port.
MAC I/F-Multicast	R	11E	Number of good multicast packets received from this port.
MAC I/F-SAchanges	R	11F	Number of times the source address has changed. Minimum roll-over time = 81 hours.

1. R = Read Only.

ETHERNET ADDRESS REGISTERS

All Ethernet Address Registers consist of two 32-bit registers that together contain a 48-bit Ethernet address. Refer to Table 34 for register bit assignments.

Table 34: Ethernet Address Register Bit Assignments

Upper Address	Bits 15:0 contain bits 47:32 of the Ethernet Address.
Lower Address	Bits 31:0 contain bits 31:0 of the Ethernet Address.

Port Address Tracking Registers

The Port Address Tracking Register set is described in Table 35. These registers continuously monitor the Source Addresses of packets emanating from the corresponding ports. Refer to Table 34 for bit assignments.

Table 35: Port Address Tracking Registers

Name	Type[1]	Addr	Description
rptrAddrTrackNewLastSrcAddress-Tp Port 1	R/W	120, 121	
rptrAddrTrackNewLastSrcAddress-TP Port 2	R/W	122, 123	
rptrAddrTrackNewLastSrcAddress-TP Port 3	R/W	124, 125	
rptrAddrTrackNewLastSrcAddress-TP Port 4	R/W	126, 127	
rptrAddrTrackNewLastSrcAddress-TP Port 5	R/W	128, 129	
rptrAddrTrackNewLastSrcAddress-TP Port 6	R/W	12A, 12B	
rptrAddrTrackNewLastSrcAddress-TP Port 7	R/W	12C, 12D	
rptrAddrTrackNewLastSrcAddress-TP Port 8	R/W	12E, 12F	
rptrAddrTrackNewLastSrcAddress-TP Port 9	R/W	130, 131	LXT917 Only
rptrAddrTrackNewLastSrcAddress-TP Port 10	R/W	132, 133	LXT917 Only
rptrAddrTrackNewLastSrcAddress-TP Port 11	R/W	134, 135	LXT917 Only
rptrAddrTrackNewLastSrcAddress-TP Port 12	R/W	136, 137	LXT917 Only
rptrAddrTrackNewLastSrcAddress-AUI Port	R/W	138, 139	
rptrAddrTrackNewLastSrcAddress-MAC Port	R/W	13A, 13B	

1. R/W = Read / Write

Authorized Port Address Registers

The Authorized Port Address Register set is described in Table 36. The operation of these registers is determined by the Authorization Control Register. Refer to Table 34 for bit assignments.

Table 36: Authorized Port Address Registers

Name	Type[1]	Addr	Description
Authorized Address Register - TP Port 1	R/W	13C, 13D	
Authorized Address Register - TP Port 2	R/W	13E, 13F	
Authorized Address Register - TP Port 3	R/W	140, 141	
Authorized Address Register - TP Port 4	R/W	142, 143	
Authorized Address Register - TP Port 5	R/W	144, 145	
Authorized Address Register - TP Port 6	R/W	146, 147	
Authorized Address Register - TP Port 7	R/W	148, 149	
Authorized Address Register - TP Port 8	R/W	14A, 14B	
Authorized Address Register - TP Port 9	R/W	14C, 14D	LXT917 Only
Authorized Address Register - TP Port 10	R/W	14E, 14F	LXT917 Only
Authorized Address Register - TP Port 11	R/W	150, 151	LXT917 Only
Authorized Address Register - TP Port 12	R/W	152, 153	LXT917 Only
Authorized Address Register - AUI Port	R/W	154, 155	

1. R/W = Read / Write

Search Registers

The Search Register set is described in Table 37.

Table 37: Search Registers

Name	Type[1]	Addr	Description
Search Address Register	R/W	156,157	This register-pair specifies an Ethernet Source Address to match. Refer to Table 34 for bit assignments
Search Result Register	R	160	This register indicates which ports sent packets with source addresses that matched the register pair described in the row above. Refer to Table 38 for bit assignments (Bit 13 not used). This register clears when read.

1. R/W = Read / Write.
R = Read Only.

CONTROL AND STATUS REGISTERS

The Control and Status Register set includes general port control and status registers which conform to the bit assignments shown in Table 38, and additional control and status registers with alternate bit assignments shown in Tables 40 through 45.

Table 38: Port Control and Status Register Bit Assignments

31:14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Rsvd	MAC	AUI	TP12	TP11	TP10	TP9	TP8	TP7	TP6	TP5	TP4	TP3	TP2	TP1

1. Bits 13:12 not used in all registers. Refer to individual register descriptions.
2. Bits 11:8 not used in the LXT916.

General Port Control Registers

The General Port Control Register set is described in Table 39. Refer to Table 38 for Port Control Register bit assignments. Bits 12 and 13 are not used in all cases (refer to specific register descriptions).

Table 39: Port Control Registers

Name	Type[1]	Addr	Description
Enable Register	R/W	171	Writing a 1 to any bit enables the transmitter and receiver on the corresponding port, writing a 0 disables them. Changing a port's status while the network is active may cause packet fragments to be generated. If the $\overline{\text{MG\_PRSNT}}$ pin is Low, this register will initialize to all 0's (all ports disabled). If the $\overline{\text{MG\_PRSNT}}$ pin is High, this register will initialize to all 1's (all ports enabled).
Reserved	-	172	
Reserved	-	173	
Alternate Partition Register	R/W	174	Writing a 1 to any bit enables the alternate partition algorithm (re-connect on transmit only) for the corresponding port, a 0 the normal algorithm (re-connect on transmit or receive). (Bits 31:13 not used)
Link Control Register	R/W	178	Writing a 1 to any bit enables the Link Partition Algorithm for the corresponding Twisted Pair port, writing a 0 disables it. When this function is disabled, the port automatically goes to Link Pass state and continues to transmit link pulses. (Bits 31:12 not used; Power-up state is all 1's)
Polarity Control Register	R/W	179	Writing a 1 to any bit disables polarity correction for the corresponding Twisted Pair port. (Bits 31:12 not used)
Squelch Control Register	R/W	17A	Writing a 1 to any bit enables the receiver for the corresponding port to use reduced squelch levels for longer-distance cables; writing a 0 enables normal squelch levels to be used. (Bits 31:12 not used)

1. R/W = Read/Write.

Interrupt Status Register

The Interrupt Status Register is described in Table 41. Refer to Table 40 for bit assignments.

Table 40: Interrupt Status Register Bit Assignments

Bits 31:3	Bit 2	Bit 1	Bit 0
Reserved	Jabber	Source Address Change - TP Port	Source Address Change - AUI Port

Table 41: Interrupt Status Register

Name	Type[1]	Addr	Notes
Interrupt Status Register	R	17B	Indicates one of three interrupt conditions. Clears when read. Power-up state is all 0s.

1. R = Read Only

Port Status Registers

The Port Status Register set is described in Table 42. Refer to Table 38 for bit assignments.

Table 42: Port Status Registers

Name	Type[1]	Addr	Notes
AUI Status Register	R	17C	Reports SQE (heartbeat) and Loopback status of AUI port. Refer to Table 44 for details.
Link Status Register	R	17D	A "1" in any bit position indicates the corresponding port is in the "Link Up" state. (Bits 31:12 not used)
Partition Status Register	R	17E	A "1" in any bit position indicates the corresponding port has been partitioned. (Bits 31:13 not used.)
Polarity Status Register	R	17F	A "1" in any bit position indicates that the polarity for the corresponding port has been reversed (Bits 31:12 not used.)
SA Change Detection Register	R	180	A "1" in any bit position indicates that the Source Address has changed on the corresponding port. (Bits 31:13 not used.)

1. R = Read Only.

AUI Control and Status Registers

The AUI Control and Status Register set is described in Table 44. Refer to Table 43 for bit assignments.

Table 43: AUI Control and Status Register Bit Assignments

Register	Bits 31:2	Bit 1	Bit 0
AUI Control	Reserved	Reserved	SQE Mask
AUI Status	Reserved	Loopback	SQE (Heartbeat) Status

Table 44: AUI Control and Status Registers

Name	Type[1]	Addr	Description
AUI Control Register	R/W	177	This bit controls masking or generation of the AUI "heartbeat", defined as brief activity on the AUI CI pair generated by the MAU shortly after successful completion of a transmission. The power-up state of this register is "0". **When the AUI is functioning as a DTE** - If this bit is 1 the device will not react to heartbeat, other than to update the AUI status register. If this bit is 0, the device will react to heartbeat by going into a full receive collision. **When the AUI is functioning as a MAU** - If this bit is 1, the device will not generate heartbeat; if it is 0, the device will generate heartbeat.
AUI Status Register	R	17C	This register reports SQE and Loopback status of AUI port when the LXT917 is operating as the DTE, and has no function when the operating as the MAU). **SQE Heartbeat Status** - This bit indicates the presence or absence of a heartbeat signal from an external MAU (1 = present, 0 = absent). This function operates regardless of the state of the SQE Mask bit in the AUI Control Register. **Loopback** - This bit indicates whether or not data loopback was detected from an external MAU (1 = present, 0 = absent.)

1. R/W = Read/Write.
   R = Read Only.

Authorization and LED Control Registers

The Authorization and LED Control Registers are described in Table 46. Refer to Table 45 for bit assignments.

Table 45: Authorization and LED Control Register Bit Assignments[1]

31:26	25:24	23:22	21:20	19:18	17:16	15:14	13:12	11:10	9:8	7:6	5:4	3:2	1:0
Reserved	AUI	TP12	TP11	TP10	TP9	TP8	TP7	TP6	TP5	TP4	TP3	TP2	TP1

1. Bits 23:16 not used by the LXT916.

Table 46: Authorization and LED Control Registers

Name	Addr	Description[1]
Authorization Control Register	175	Determines the operational mode of the Authorized Address Register for each port. 00 = Free-Run. The Authorized Address Register continuously re-learns its contents from the source addresses of incoming packets (Power-up default). 01 = Next Lock. The Authorized Address Register learns the source address of the next valid packet and locks. Once it locks, the corresponding bits in this register automatically change to '10'. 10 = Lock. The Authorized Address Register does not change with traffic flow. In this mode, it can only be updated under network management control. 11 = Reserved.
LED Control Register	176	Controls operation of the serial LED bits associated with each port. The power-up state of this register is all 1's if an external manager is detected, and defaults to "hardware control" otherwise. 00 = LED off 01 = LED fast blink 10 = hardware control 11 = LED on

1. The Authorization Control Register and the LED Control Register are both Read/Write.

CONFIGURATION REGISTERS

Configuration Registers are listed in Table 47. Bit assignments for the Configuration Registers are shown in Table 48 through 53. The Master Configuration Register is defined in Table 54.

Table 47: Configuration Registers

Name	Type[1]	Addr	Notes
Global LED Control Register	R/W	181	Refer to Table 48 for bit assignments. This register controls the operating modes of the Global Fault LED and User Defined LED as follows: **Global Fault LED**, Bit Encoding: 00 Off 01 Hardware Control 10 Slow Blink 11 On Steady **User Defined LED**, Bit Encoding: 00 Off 01 Fast Blink 10 Reserved 11 On Steady
LED Timer Register	R/W	182	Refer to Table 49 for bit assignments. Bits 8-15 of this register set the fast blink frequency of the LEDs. Bits 0-7 set the slow blink frequency. The same formula is used in each case, with a maximum of 128 Hz and a minimum of 0.5 Hz (for example, fast blink = 32 (0.4 s); slow blink = CC (1.6 s)).
Master Configuration Register	R/W	183	Refer to Table 53 for bit assignments. At power-up, all bits in this register default to 0.
Reserved	R	184	
Device ID Register	R	185	This register follows the IEEE 1149.1 specification; refer to Table 50 for bit assignments. The upper 4 bits identify the device revision level. The next 16 bits store the Part ID Number in hexadecimal, which is '0396'. The lower 12 bits contain a JEDEC Manufacturer ID, which for Level One is hexadecimal 'FE'.
Repeater Reset Register	W	186	Writing any data value to this register causes all functional logic to reset, but does not affect the state of counters, configuration registers or status registers.
Software Reset Register	W	187	Writing any data value to this register is identical to a hardware reset. Everything is reset except counters and addresses.
HUB ID Register (1 and 2)	W	188, 189	Refer to Table 51 for bit assignments. Writing a valid 48-bit ID (one that matches the EPROM ID) to this register causes the device to change its Hub ID to the contents of the EPROM ID register listed below. This register cannot be read.
EPROM ID Register (1 and 2)	R	190, 191	These two registers contain the 48-bit ID read in from EPROM at power-up. Refer to Table 52 for bit assignments.

1. R = Read Only.
   W = Write Only.
   R/W = Read/Write.

Table 48: Global LED Control Register Bit Assignments

31:4	3	2	1	0
Reserved	Global Fault LED		User Defined LED	

Table 49: LED Timing Control Register Bit Assignments

31:16	15:8	7:0
Reserved	Fast Blink Frequency	Slow Blink Frequency

1. Period = 7.8125 ms x (Register Value + 1)

2. Frequency = $\frac{1}{7.8125 \text{ ms} \times (\text{Register Value} + 1)}$

Table 50: Device ID Register Bit Assignments

31:28	27:12	11:8	7:1	0
Version	Part ID	Jedec Continuation Characters	JEDEC ID	Chip ID
XXXX	0000 0011 1001 0101 (LXT917) 0000 0011 1001 0100 (LXT916)	0000	111 1110	0

Table 51: Hub ID Register Bit Assignments

Upper Address	31:21 - All 0s	20:16 - Hub ID	15:0 - Must match bits 15:0 of upper EPROM ID Register
Lower Address	31:0 - Must match bits 31:0 of lower EPROM ID Register		

Table 52: EPROM ID Register Bit Assignments

Upper Address	31:16 - All 0s	15:0 - Bits 15:0 of Address read from EPROM
Lower Address	31:0 - Bits 47:16 of Address read from EPROM	

Table 53: Master Configuration Register Bit Assignments

31:11	10	9	8:6	5	4	3	2	1	0
Reserved	Arbin	Zero Counters	Reserved	Isolate	CountMode	Reserved	EFIFOERR	EMCV	Reserved

Table 54: Master Configuration Register Bit Definitions

Bit	Name	Type[1]	Description	Default
31:11	Reserved	-	Write as 0, ignore on read.	N/A
10	Arbin	R	This bit shows the value present at the ARBIN input pin.	0
9	Zero Counters	R/W	Setting this bit to "1" will cause all counters to be zeroed. Upon completion of this operation, the device will reset this bit to "0".	0
8:6	Reserved	-	Write as 0, ignore on read.	N/A
	Isolate	R/W	This bit controls the Isolate output. Setting the bit to "1" causes the Isolate output pin to be asserted High.	0
4	CountMode	R/W	This bit affects the operation of the portReadableFrames and MACReadableFrames counters. Setting this bit to 0 will cause these counters to count all readable frames; setting this bit to 1 will cause these counters to count only readable unicast frames.	0
3	Reserved	-	Write as 0, ignore on read.	N/A
2	EFIFOERR	R/W	This bit determines whether the device will enter the Transmit Collision State if its internal fifo overflows or underflows (data-rate mismatch). 0 = no, 1 = yes.	0
1	EMCV	R/W	This bit determines whether the device will enter the Transmit Collision State upon reception of a Manchester Code Violation; 0 = no, 1 = yes.	0
0	Reserved	-	Write as 0, ignore on read.	N/A

1. R/W = Read/Write.
   R = Read Only.

DATA SHEET

LXT918

Multi-Segment Hub Repeater

MAY 1997
Revision 1.1

General Description

The LXT918 provides four complete 10 Megabit Ethernet repeaters in one mixed-signal IC. An internal switch matrix allows any of the external ports - including a 7-pin MAC interface - to be switched to any repeater segment at will. Each segment has its own independent Inter-Repeater Backplane which allows multiple segments to be cascaded in stackable and modular hub applications.

The LXT918 provides per-segment and per-port support for the Repeater MIB and for RMON. All variables are implemented as 32-bit counters for maximum roll-over time. A high-speed serial management interface provides software access to the internal switch, RMON and Repeater MIB counters, and to port status and control features.

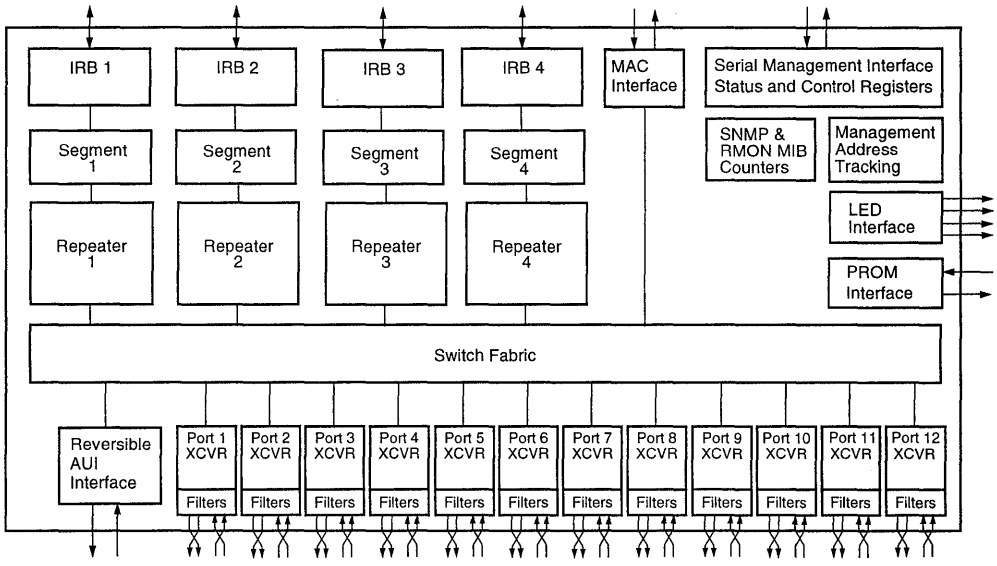
A unique feature of the LXT918 architecture is that when a port is switched to a new segment, its counters follow it. In addition the LXT918 has a SoftReconnect feature, which switches ports without corrupting network traffic.

Features

Advanced features enable new dimensions in Next Generation Repeater applications:

- Four independent 10 Mbit Ethernet Repeaters
- Twelve 10BASE-T ports with Integrated Filters
- Hardware assist for RMON and the Repeater MIB
- Reversible AUI port
- Four mixed-signal backplanes for cascading
- 7-pin "roaming" MAC interface for probe access
- High-speed serial management interface
- Two address-tracking registers per port
- Source Address matching function
- 0-70°C Temperature Range
- 208-pin PQFP

LXT918 Block Diagram



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PIN ASSIGNMENTS AND SIGNAL DESCRIPTIONS

Figure 1: LXT918QC Pin Assignments

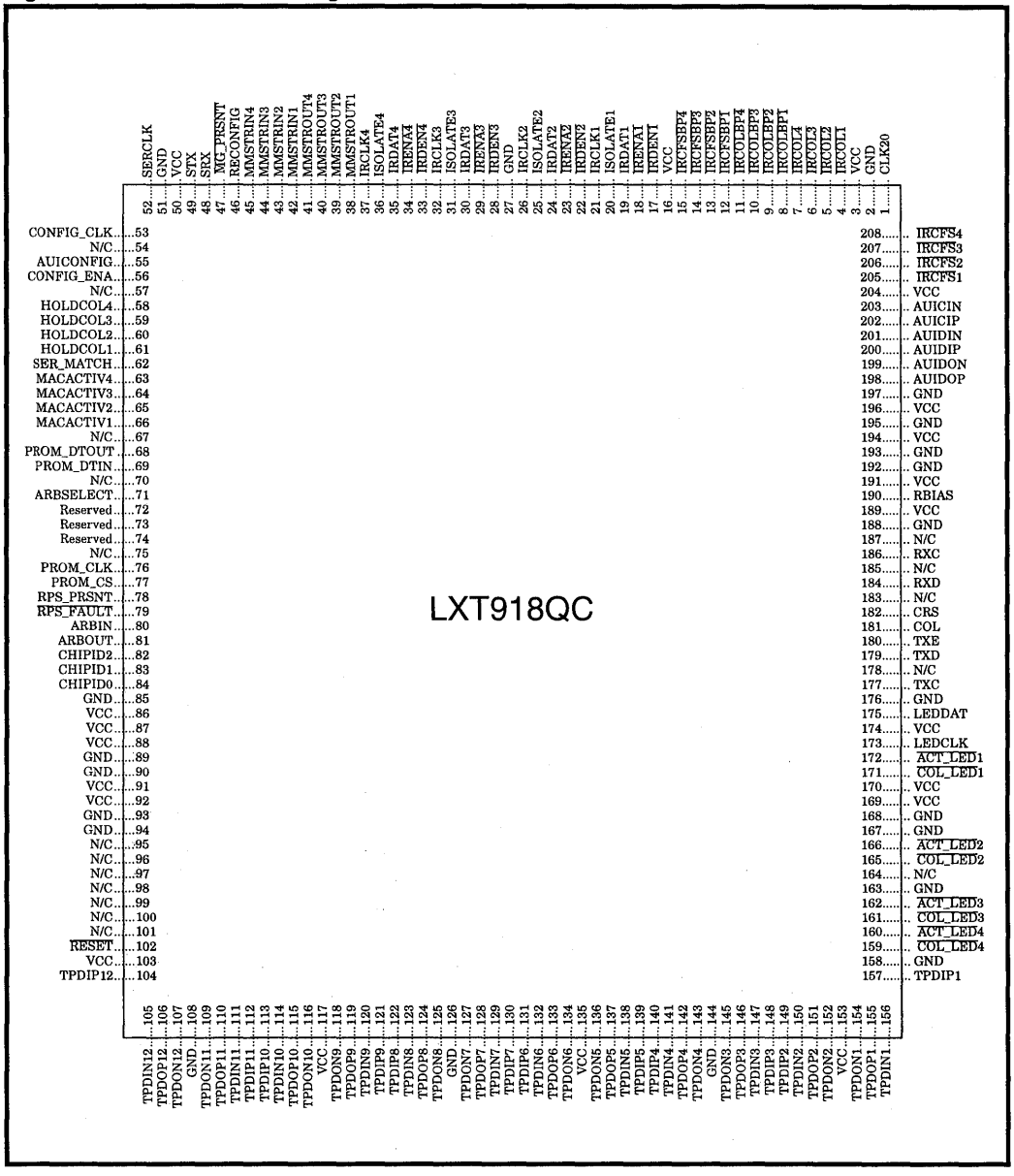


Table 1: Twisted-Pair Port Signal Descriptions

Pin	Symbol	Type	Description
155 154	TPDOP1 TPDON1	Analog Output Port 1	**Twisted-Pair Data Outputs - Ports 1 through 12.** These pins are the positive (TPDOP*x*) and negative (TPDON*x*) differential output pairs from the respective LXT918 twisted-pair port line drivers.
151 152	TPDOP2 TPDON2	Analog Output Port 2	
146 145	TPDOP3 TPDON3	Analog Output Port 3	
142 143	TPDOP4 TPDON4	Analog Output Port 4	
137 136	TPDOP5 TPDON5	Analog Output Port 5	
133 134	TPDOP6 TPDON6	Analog Output Port 6	
128 127	TPDOP7 TPDON7	Analog Output Port 7	
124 125	TPDOP8 TPDON8	Analog Output Port 8	
119 118	TPDOP9 TPDON9	Analog Output Port 9	
115 116	TPDOP10 TPDON10	Analog Output Port 10	
110 109	TPDOP11 TPDON11	Analog Output Port 11	
106 107	TPDOP12 TPDON12	Analog Output Port 12	
157 156	TPDIP1 TPDIN1	Analog Input Port 1	**Twisted-Pair Data Inputs - Ports 1 through 12.** These pins are the positive (TPDIP*x*) and negative (TPDIN*x*) differential input pairs to the respective LXT918 twisted-pair ports.
149 150	TPDIP2 TPDIN2	Analog Input Port 2	
148 147	TPDIP3 TPDIN3	Analog Input Port 3	
140 141	TPDIP4 TPDIN4	Analog Input Port 4	
139 138	TPDIP5 TPDIN5	Analog Input Port 5	
131 132	TPDIP6 TPDIN6	Analog Input Port 6	
130 129	TPDIP7 TPDIN7	Analog Input Port 7	
122 123	TPDIP8 TPDIN8	Analog Input Port 8	
121 120	TPDIP9 TPDIN9	Analog Input Port 9	
113 114	TPDIP10 TPDIN10	Analog Input Port 10	
112 111	TPDIP11 TPDIN11	Analog Input Port 11	
104 105	TPDIP12 TPDIN12	Analog Input Port 12	

Table 2: AUI Port Signal Descriptions

Pin	Symbol	Type	Description
55	AUICONFIG	TTL Input PD	**AUI Configuration Data In.** Up to 16 bits of AUI Configuration Register data is shifted in via this pin (LSB to MSB). Bits 15:1 are user defined. Bit 0 sets the AUI port operating mode as follows: 0 = Normal (DTE) mode; 1 = Reversed (MAU) mode.
56	CONFIG_ENA	TTL Output	**AUI Configuration Register Read Enable.** An active Low pulse is output on this pin at the beginning of each AUI Configuration Register read cycle. This signal is provided to control an external shift register.
53	CONFIG_CLK	TTL Output	**AUI Configuration Register Clock.** The LXT918 drives sixteen 100ns clock pulses on this pin each time the AUI Configuration Register is read. This signal is used to clock in configuration data (up to 16 bits) from an external shift register.
198 199	AUIDOP AUIDON	Analog Output	**AUI Data Outputs**. Positive and negative data outputs from the AUI port. In normal (DTE) mode, connect to pins 3 and 10 of the AUI D-connector. In reverse (MAU) mode, connect to pins 5 and 12 of the AUI D-connector.
200 201	AUIDIP AUIDIN	Analog Input	**AUI Data Inputs.** Positive and negative data inputs to the AUI port. In normal (DTE) mode, connect to pins 5 and 12 of the AUI D-connector. In reverse (MAU) mode, connect to pins 3 and 10 of the AUI D-connector.
202 203	AUICIP AUICIN	Tri-State, Analog, I/O	**AUI Collision Inputs.** In normal (DTE) mode these pins are the positive and negative collision inputs for the AUI port. In reverse (MAU) mode these pins are outputs.

1. PD = Input contains pull-down.

Table 3: Inter-Repeater Backplane Signal Descriptions

Pin	Symbol	Type	Description
17 22 28 33	$\overline{\text{IRDEN1}}$ $\overline{\text{IRDEN2}}$ $\overline{\text{IRDEN3}}$ $\overline{\text{IRDEN4}}$	Open-Drain Output	**IRB Driver Enables - Segments 1 through 4.** These outputs allow multiple devices to share a common set of external bi-directional transceivers ('245s) for driving the IRB's off-board. Each IRB must have its own transceiver. When a device assumes control of an IRB, it drives the corresponding $\overline{\text{IRDENx}}$ output Low. When an IRB is idle, a 330 Ω pull-up resistor (required) pulls the corresponding $\overline{\text{IRDEN}x}$ output High. Attach each output to the direction control of the corresponding transceiver.
18 23 29 34	$\overline{\text{IRENA1}}$ $\overline{\text{IRENA2}}$ $\overline{\text{IRENA3}}$ $\overline{\text{IRENA4}}$	CMOS I/O Open Drain	**Inter-Repeater Backplane Enables - Segments 1 through 4.** These active Low outputs indicate carrier presence on the corresponding IRB's. When an IRB is idle, a 330 Ω pull-up resistor pulls the corresponding $\overline{\text{IRENA}x}$ output High. These signals may be buffered between modules.
19 24 30 35	IRDAT1 IRDAT2 IRDAT3 IRDAT4	CMOS I/O Open Drain	**IRB Data - Segments 1 through 4.** These bidirectional signals carry data on the corresponding IRB's. Data is driven and sampled on the rising edge of the corresponding IRCLK. Each of these signals must be pulled up by a 330 Ω resistor. Between modules, these signals can be buffered.

1. PU = Input contains pull-up.
2. PD = Input contains pull-down.
3. NC = No Clamp. Pad will not clamp input in the absence of power.
4. Even if the IRB is not used, required pull-up resistors must be installed as listed above.

Table 3: Inter-Repeater Backplane Signal Descriptions – continued

Pin	Symbol	Type	Description
20 25 31 36	ISOLATE1 ISOLATE2 ISOLATE3 ISOLATE4	Output	**Isolate Enables - Segments 1 through 4.** These outputs allow one device per module the ability to isolate the IRB's from the outside world. Attach each output to the Enable input of the corresponding transceiver. The output is driven High (disable) when the corresponding IRB should be isolated, and Low (enable), when it should not be isolated.
21 26 32 37	IRCLK1 IRCLK2 IRCLK3 IRCLK4	CMOS I/O TriState, PU Schmitt Trigger #2	**IRB Clocks - Segments 1 through 4.** These bi-directional, non-continuous, 10 MHz clocks are recovered from received network traffic. During idle periods, these outputs are high-impedanced. Schmitt triggering is used to increase noise immunity, therefore full rail-to-rail signals are required. Between modules, buffering may be used on these signals.
4 5 6 7	$\overline{\text{IRCOL1}}$ $\overline{\text{IRCOL2}}$ $\overline{\text{IRCOL3}}$ $\overline{\text{IRCOL4}}$	CMOS I/O Open Drain	**IRB Collision - Segments 1 through 4.** Each of these outputs is driven Low to indicate that a collision has occurred on the corresponding segment. When there is no collision, a 330 Ω pull-up resistor (required) on each output pulls it High. These signals are intended only to be used between devices on the same module; they may not be buffered.
8 9 10 11	$\overline{\text{IRCOLBP1}}$ $\overline{\text{IRCOLBP2}}$ $\overline{\text{IRCOLBP3}}$ $\overline{\text{IRCOLBP4}}$	CMOS I/O Open Drain NC	**IRB Collision-BackPlane - Segments 1 through 4.** These active Low outputs have the same function as $\overline{\text{IRCOL}}$, but are used between modules. Attach these signals only from the device with ChipID = 0 to the backplane or connector, **without buffering**. Each output must be pulled up by one 330Ω resistor per system.
205 206 207 208	$\overline{\text{IRCFS1}}$ $\overline{\text{IRCFS2}}$ $\overline{\text{IRCFS3}}$ $\overline{\text{IRCFS4}}$	Analog, I/O	**IRB Collision Force Sense - Segments 1 through 4.** Each of these three-state analog outputs indicates that a transmit collision has occurred on its corresponding segment when it is driven Low. Each must be pulled up with a 680 Ω 1% resistor. These signals are intended only to be used between devices on the same module; they may not be buffered.
12 13 14 15	$\overline{\text{IRCFSBP1}}$ $\overline{\text{IRCFSBP2}}$ $\overline{\text{IRCFSBP3}}$ $\overline{\text{IRCFSBP4}}$	Analog I/O, N/C	**IRB Collision Force Sense-BackPlane - Segments 1 through 4.** These outputs have exactly the same function as $\overline{\text{IRCFS}}$, but are used between modules. Attach these signals only from the device with ChipID = 0 to the backplane or connector, **without buffering**. Each output must be pulled up by one 330 Ω, 1% resistor per system.
61 60 59 58	HOLDCOL1 HOLDCOL2 HOLDCOL3 HOLDCOL4	TTL Tri-state I/O, PD	**Hold Collision - Segments 1 through 4.** Each of these active High signals is driven by the device with ChipID = 0 to extend a non-local transmit collision to other devices on the same module. The HOLDCOLx signals from different modules should NOT be attached together.

1. PU = Input contains pull-up.
2. PD = Input contains pull-down.
3. NC = No Clamp. Pad will not clamp input in the absence of power.
4. Even if the IRB is not used, required pull-up resistors must be installed as listed above.

Table 3: Inter-Repeater Backplane Signal Descriptions – continued

Pin	Symbol	Type	Description
42 43 44 45	MMSTRIN1 MMSTRIN2 MMSTRIN3 MMSTRIN4	TTL Input, NC	**Management Master In - Segments 1 through 4.** The MMSTR daisy chain ensures that collisions will be counted correctly in multi-module applications. Attach the MMSTRIN input of each device to the MMSTROUT output of the previous device. Ground MMSTRIN of the first or only device.
38 39 40 41	MMSTROUT1 MMSTROUT2 MMSTROUT3 MMSTROUT4	Output, NC	**Management Master Out - Segments 1 through 4.** MMSTR daisy chain output. In hot-swap applications, a 1 kΩ - 3 kΩ resistor can be used as a bypass between MMSTRIN and MMSTROUT.
66 65 64 63	MACACTIV1 MACACTIV2 MACACTIV3 MACACTIV4	TTL Input, PD	**MAC Active - Segments 1 through 4.** These active High inputs allow external Ethernet controllers to directly drive the Inter Repeater Backplanes. When the controller asserts MACACTIV*x*, the LXT918 drives the $\overline{\text{IRCOL}x}$, $\overline{\text{IRCOLBP}x}$, $\overline{\text{IRCFS}x}$ and $\overline{\text{IRCFSBP}x}$ signals on behalf of the controller. If any of these inputs are unused, tie them to ground.

1. PU = Input contains pull-up.
2. PD = Input contains pull-down.
3. NC = No Clamp. Pad will not clamp input in the absence of power.
4. Even if the IRB is not used, required pull-up resistors must be installed as listed above.

Table 4: MAC Interface Signal Descriptions

Pin	Symbol	Type	Description
177	TXC	Output	**Transmit Clock.** This 10 MHz continuous output is derived from the 20 MHz input clock.
179	TXD	TTL Input, PD	**Transmit Data.** External controllers use this input to transmit data to the LXT918. The device samples TXD on the rising edge of TXC, when TXE is High.
180	TXE	TTL Input, PD	**Transmit Enable** External controllers drive this input High to indicate that data is being transmitted on the TXD pin. Tie this input Low if it is unused.
181	COL	Output	**Collision.** The LXT918 drives this signal High to indicate that a collision has occurred.
182	CRS	Output	**Carrier Sense.** The LXT918 drives this signal High to indicate that valid data is present on RXD.
184	RXD	Output	**Receive Data.** The LXT918 transmits received data to the controller on this output. Data is driven on the falling edge of RXC.
186	RXC	Output	**Receive Clock.** This is a non-continuous 10 MHz clock that the LXT918 recovers from the network when traffic is actively being received.

1. PD = Input contains pull-down.

Table 5: Serial Management Interface Signal Descriptions

Pin	Symbol	Type	Description
46	RECONFIG	TTL Input, NC	**Reconfigure**. This input controls the driving of the clock signal on the high-speed serial management interface (SERCLK). When this input is High, the LXT918 drives SERCLK with a 625 kHz output. When this input is Low, SERCLK is an input to the LXT918. In addition, a Low-to-High transition on RECONFIG causes the LXT918 to drive 13 continuous 0's on the serial management bus, causing a re-arbitration to occur.
47	$\overline{\text{MG\_PRSNT}}$	TTL Input, NC	**Manager Present**. This signal is sensed at power up. If it is High, it indicates that no local manager is present, and the 918 enables all ports and sets all LEDs to operate in "hardware mode". If it is Low, indicating that a manager is present, the 918 disables all ports, pending control of network manager.
48	SRX	TTL Input	**Serial Receive.** Receive data input for high-speed serial management interface. Must be tied to STX externally. SRX is sampled on the rising edge of SERCLK.
49	STX	Open Drain Output	**Serial Transmit.** Transmit data output for high-speed serial management interface. Must be tied to SRX externally. Data transmitted on STX is compared with data received on SRX. In the event of a mismatch, STX is put in the high impedance state. STX is driven on the falling edge of SERCLK.
52	SERCLK	Tri-State TTL Output	**Serial Clock.** Clock for serial management interface. Depending on RECONFIG, this pin is either a 625 kHz output or a 0 to 1 MHz input.

1. NC = No Clamp. Pad will not clamp input in the absence of power.

Table 6: LED Signal Descriptions

Pin	Symbol	Type	Description
171 165 161 159	$\overline{\text{COL\_LED1}}$ $\overline{\text{COL\_LED2}}$ $\overline{\text{COL\_LED3}}$ $\overline{\text{COL\_LED4}}$	Open-Drain Output, PU	**Collision LED Driver - Segments 1 through 4.** These outputs provide up to 10 mA of sink current.
172 166 162 160	$\overline{\text{ACT\_LED1}}$ $\overline{\text{ACT\_LED2}}$ $\overline{\text{ACT\_LED3}}$ $\overline{\text{ACT\_LED4}}$	Open-Drain Output, PU	**Activity LED Driver - Segments 1 through 4.** These outputs provide up to 5 mA of sink current.
173	LED_CLK	Output	**LED Clock.** Clock for LED serial data output.
175	LED_DAT	Output	**LED Data.** Serial data output for LED data.

1. PU = Pad contains pull-up.

Table 7: PROM Interface Signal Descriptions

Pin	Symbol	Type	Description
76	PROM_CLK	TTL Input, Tri-State Output	**PROM Clock.** 1 MHz clock for reading PROM data.
77	PROM_CS	Tri-State Output, PD	**PROM Chip Select.**
68	PROM_OUT	Tri-State Output, PD	**PROM Data Output.**
69	PROM_IN	TTL Input	**PROM Data Input.** If a PROM is not used, this input can be tied Low or High.

1. PD = Input contains pull-down.

Table 8: Power Supply and Indication Signal Descriptions

Pin	Symbol	Type	Description
3, 16, 50, 86, 87, 88, 91, 92, 103, 117, 135, 153, 169, 170, 174, 189, 191, 194, 196, 204	VCC	Power	**Power Supply Inputs.** Each of these pins must be connected to a common +5 VDC power supply. A de-coupling capacitor to digital ground should be supplied for every one of these pins.
2, 27, 51, 85, 89, 90 93, 94, 108 126, 144, 158, 163, 167, 168, 176, 188, 192, 193, 195, 197	GND	Power	**Ground.** Connect each of these pins to digital ground. Note: the LXT918 does NOT require separate digital and analog grounds.
190	RBIAS	Analog	**RBias**. Connect this pin to ground through a 22 kΩ, 1% resistor. Note: Do NOT route any other signals near or around this resistor.
78	RPS_PRSNT	TTL Input	**Redundant Power Supply**. Active High input indicates presence of redundant power supply. The state of this input and the $\overline{\text{RPS\_FAULT}}$ input is reflected in the RPS LED bit in the serial LED output (refer to Tables 10 and 11). Tie Low if not used.
79	$\overline{\text{RPS\_FAULT}}$	TTL Input	**Redundant Power Supply Fault**. Active Low input indicates redundant power supply fault. Tie High if not used.

Table 9: Miscellaneous Signal Descriptions

Pin	Symbol	Type	Description
1	CLK20	CMOS Input, Schmitt Trigger #1	**20 MHz System Clock.** Drive with CMOS levels.
62	SER_MATCH	Output	**Hub ID Match.** Active High. The device with ChipID = 0 asserts this signal whenever it detects a message on the serial bus which matches the local Hub ID.
71	ARBSELECT	TTL Input, PU	**Arbitration Select.** If this pin is pulled Low, Arbitration Mechanism #1 is disabled, only Arbitration Mechanism #2 will be available. If this pin is pulled High, both mechanisms will be enabled. If Arbitration Mechanism #1 is enabled, the device with ChipID = 0 will transmit an "Arbitration Request" message every 2-3 ms on the serial management interface until a Hub ID is assigned.
80	ARBIN	Tri-State Input, PD, NC	**Arbitration In/Out.** Daisy chain hub ID arbitration mechanism #2. If used, tie ARBIN to ARBOUT of the previous device, and to ground of the first/only device. If unused, tie ARBIN High.
81	ARBOUT	Output, NC	
82 83 84	CHIPID2 CHIPID1 CHIPID0	TTL Input	**Chip ID.** These pins assign unique ChipIDs to as many as eight devices on a single module. One device on each module must be assigned ChipID=0.
102	$\overline{\text{RESET}}$	CMOS Input, Schmitt Trigger #1, PU, NC	**Reset.** This active Low input causes internal circuits and state machines to reset, but does not affect counters or address tracking registers. On power-up, devices should not be brought out of reset until the power supply has stabilized and reached 4.5 volts. When there are multiple devices, it is recommended that all be supplied by a common reset that is driven by an 'LS14 or similar device.
72, 73, 74	RESERVED	-	**Reserved.** Reserved for future application development. *Leave these pins unconnected.*
53, 54, 56, 57, 67, 70, 75, 95, 96, 97, 98, 99, 100, 101, 164, 178, 183, 185, 187	NO CONNECT	-	***No Connects.*** *Leave these pins unconnected.*

1. PU = Input contains pull-up.
2. PD = Input contains pull-down.
3. NC = No Clamp. Pad will not clamp input in the absence of power

FUNCTIONAL DESCRIPTION

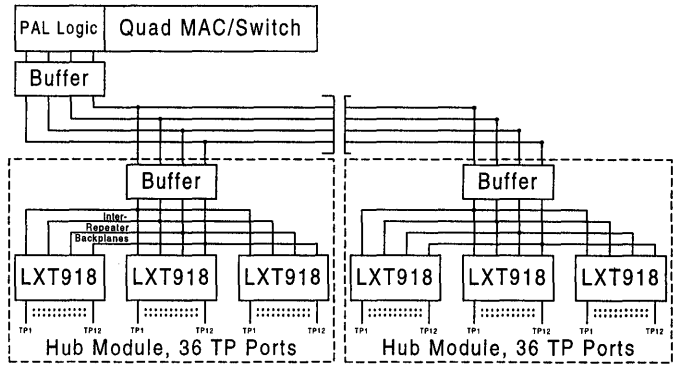
Introduction

With its unique port-switching architecture, the LXT918 revolutionizes the design of networking products by facilitating hybrid repeater/switch architectures. A mixture of the traditional repeater and the state-of-the-art switch, the hybrid repeater/switch architecture provides a cost optimized solution that allows network bandwidth to be allocated as needed under the control of the end-user. The key to this approach is to tie switched 10 Megabit outputs to the 14 LXT918 ports (12 TP + AUI + 7-Pin MAC Interface). This can be done in several different architectures depending on application needs as shown in Figure 2.

Figure 2: LXT918 Hybrid Architecture

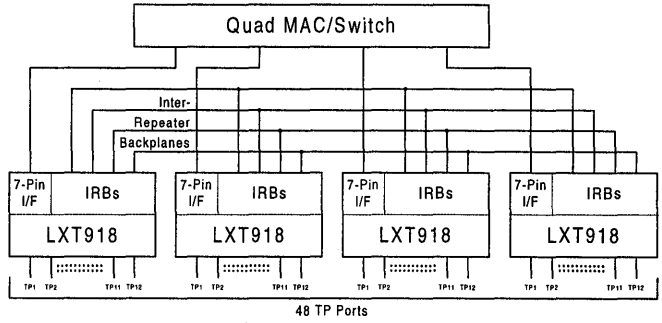
Architecture Type 1:

IRB Connected Switch



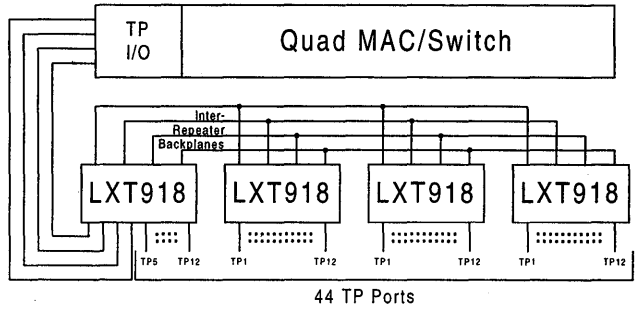
Architecture Type 2:

Direct MAC Connected Switch



Architecture Type 3:

Twisted Pair Connected Switch



The switching matrix of the LXT918 allows the dedicated bandwidth of the switch outputs to be shared among a set of users, which can be changed at will. The additional cascading capability provided by the Inter Repeater Backplanes allows the set of users sharing the bandwidth to grow arbitrarily larger. A more detailed LXT918 application block diagram is shown in Figure 3.

The switching capabilities of the LXT918 also create support for static VLANs (Virtual LANs), where users can easily be re-configured to support moves, adds and changes to the network topology. The switchable MAC interface provides the opportunity for a built-in "roaming" network monitoring or bridging function.

10BASE-T Ports

The LXT918 provides 10BASE-T ports with integrated filters. Level One's patented filter technology helps facilitate low-cost systems which meet EMI requirements. Refer to Table 1 for 10BASE-T port pin assignments and signal descriptions.

AUI Port

The LXT918 provides a reversible AUI interface that can function either as a DTE or as a MAU. When this interface functions as a MAU, it supports remote-office and embedded-hub applications (such as file servers) by allowing integration of the LXT918 to existing PHY interfaces. The mode of operation is determined by bit 0 of the AUI Configuration Register. Refer to Table 2 for AUI port pin assignments and signal descriptions.

Inter-Repeater Backplane

The LXT918 easily accommodates stackable and modular hub architectures through the Inter-Repeater Backplane, which allows multiple devices to function as one logical repeater. For example, typical LXT918 stack designs accommodate as many as 192 10BASE-T ports. Refer to Table 3 for IRB pin assignments and signal descriptions.

7-pin MAC Interface

The LXT918 provides a 7-pin MAC Interface, which can be interfaced to an Ethernet controller or a switch ASIC. Refer to Table 4 for MAC Interface pin assignments and signal descriptions.

Serial Management Interface

Multiple devices can easily be managed through the high-speed serial management interface. This synchronous interface operates at rates up to 1 Mbps, and uses an HDLC-like zero-bit insertion protocol. This interface provides access to the Port Switching functions, RMON and Repeater MIB variables as well as complete control over all device functions and visibility of all status registers. Refer to Table 5 for Serial Management Interface pin assignments and signal descriptions.

Management Support

The LXT918 supports RMON and the Repeater MIB using on-chip 32-bit counters. Counters are provided for each port, including the MAC Interface port, and for each segment. Interface counters include all of the RMON Statistics group and Repeater MIB Total Octets and Transmit Collisions. Per-port counters include:

Readable Frames	Readable Octets	FCS Errors
Alignment Errors	FramesTooLong	ShortEvents
Runts	Collisions	LateEvents
VeryLongEvents	DataRateMismatch	AutoPartitions
Broadcast	Multicast	SA Changes

Source Address Management Functions

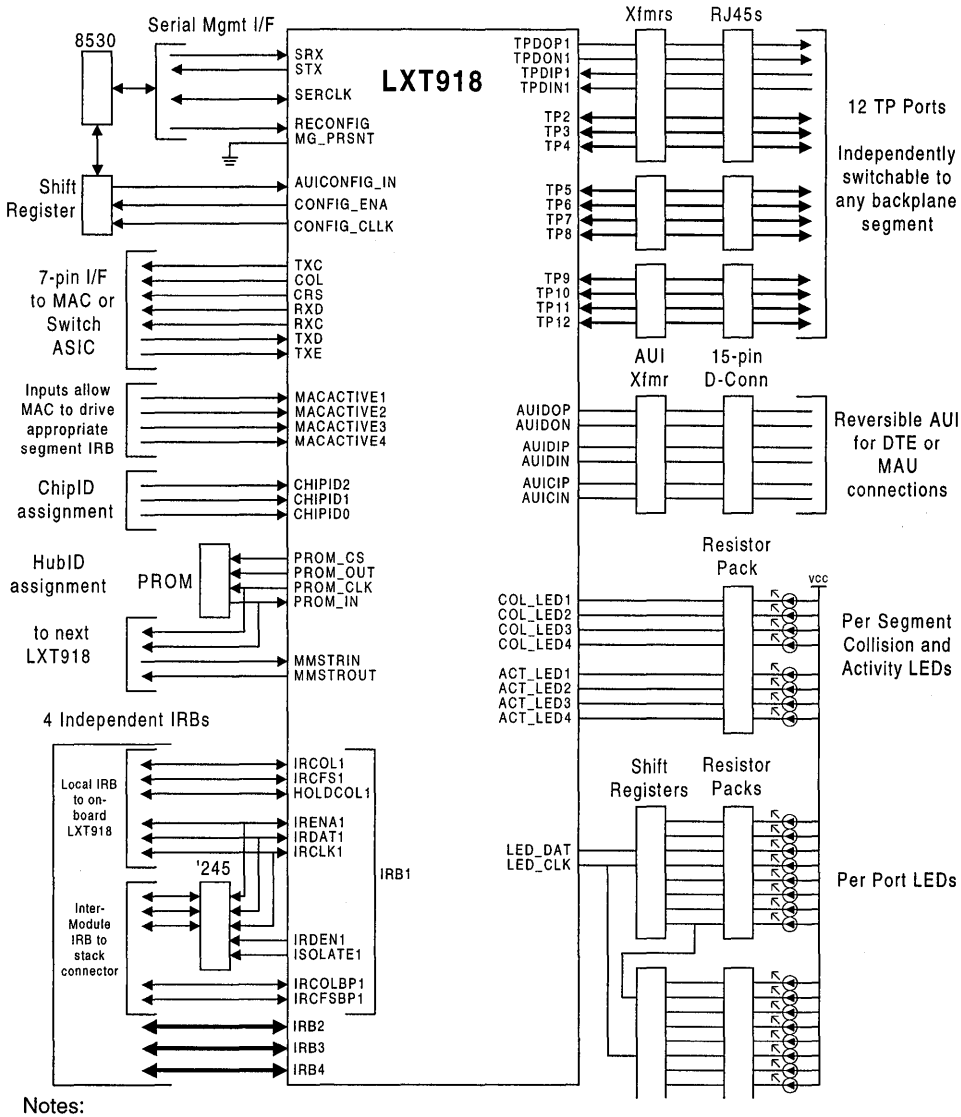
The LXT918 provides Source Address Management functions for all ports. Each port has two source address tracking registers. The rptrAddrTrackNewLastSrcAddress register is always free-running and contains the source address of the last valid packet received from the port. The Authorized Address Register operates in three states: free-run, lock-on-next or lock. This register can track source addresses or lock on an address that has been assigned by the network manager or that it has previously tracked. Once this register is locked, subsequent Source Address changes on a port cause the device to set the corresponding bits in the SA Change Detection Register and the Interrupt Status Register.

The LXT918 also provides a Source Address Tracking Function for each segment. Supplied with a 48-bit Ethernet Source Address, this function identifies all ports on a particular segment that sourced that Source Address.

LED Interface

The serial LED interface (data and clock) supplies link and partition status for each of the TP ports, status for the AUI port, and miscellaneous functions. The device directly provides activity and collision LEDs for each segment. Refer to Table 6 for LED Interface pin assignments and signal descriptions.

Figure 3: Typical Application Block Diagram



Notes:

1. Refer to Figure 11 for typical TP port interface circuitry.
2. Refer to Figures 12 and 13 for typical AUI port interface circuitry.
3. Refer to Figure 14 for typical IRB circuitry.
4. Refer to Figure 15 for typical Serial Management Interface circuitry.
5. Refer to Figure 17 for typical PROM circuitry.

Requirements

Power

The LXT918 requires a single +5V power supply, and a single ground reference. Separate analog and digital grounds are NOT required. Refer to Table 8 for power and ground pin assignments.

Clock

The LXT918 requires a continuous 20 MHz clock input, driven with CMOS levels.

RBIAS Input

The LXT918 requires a 1%, 22 kΩ resistor connecting its RBIAS input to ground.

Reset Signal

At power up, the $\overline{\text{RESET}}$ input must be held Low until VCC reaches at least 4.5V. An 'LS14 or equivalent should be used to drive $\overline{\text{RESET}}$ if there are multiple 918 devices.

External PROM

The LXT918 requires an external, auto-incrementing PROM, which is used to supply a 48-bit ID at power-up. If the PROM is not available, the PROM data input signal must be tied either High or Low. Multiple devices on the same module can share a single common PROM. Refer to Table 7 for PROM interface pin assignments and signal descriptions.

Chip Identification

Each LXT918 on a module requires a unique 3-bit Chip ID value asserted on these pins in order for the serial management bus to function correctly. One LXT918 on each module must be assigned ChipID = 0.

Management Master I/O Link

In multiple device applications, the Management Master daisy chain (MMSTRIN/MMSTROUT) ensures that collisions are counted correctly. Connect the MMSTRIN input to the MMSTROUT output of the previous device, even across module boundaries. Ground the MMSTRIN input of the first or only device in the system. In hot-swap applications, resistive bypassing can be used, with a value between 1k and 3 kΩ.

Repeater Operation

LXT918 repeater operation is controlled by the state machine shown in Figure 4. When the LXT918 detects activity at any input, it begins generating preamble to all other outputs on the same segment. Once 62 bits of preamble have been transmitted, and a start-of-frame delimiter (SFD) has been received, the device begins repeating the received packet to all outputs on that segment. An internal FIFO provides buffering. Operation continues until the receiver goes idle, or until the jabber timer is exceeded.

If activity is detected simultaneously at two or more inputs on the same segment, that segment enters the transmit collision state. The device sends a jam signal to all ports on that segment for 96 bit times. A jam signal continues to be sent to all ports as long as two or more inputs on that segment are active. If activity simultaneously ceases at all inputs, the segment returns to the idle state. If activity continues at only one input, the segment enters the one-port-left state. In that state, the device continues to transmit a jam signal to all ports on that segment *except* to the one that has the active input. Once this activity ceases, the segment returns to the idle state.

If the AUI port is functioning as the DTE, and an external MAU activates the CI inputs while the port is active, the segment to which the AUI port is attached enters the receive collision state. The device sends a jam signal to all ports on the segment except for the AUI port for at least 96 bit times and until all activity ceases.

In multiple-device configurations, all devices participate in data exchange and the various collision states via the Inter Repeater Backplane.

Exception Conditions

Fragment Extension

Any received activity shorter than 96 bits (also known as a fragment) will be extended so that it is at least 96 bits long. On the Inter Repeater Backplane, a fragment extension will look like a receive collision, however it will not be counted as a collision.

Packets with No SFD

Packets with no start-of-frame delimiter will be repeated to all ports as long preamble patterns with no SFD. These packets will be counted as "fragments" by the management counters, no matter how long they are.

Packets with Too Early SFD

Any packet with less than 40 bits of preamble will cause the internal FIFO to overflow, causing invalid packets to be transmitted to all ports.

If the EFIFOERR bit in the Master Configuration register is set when this occurs, a transmit collision will be generated.

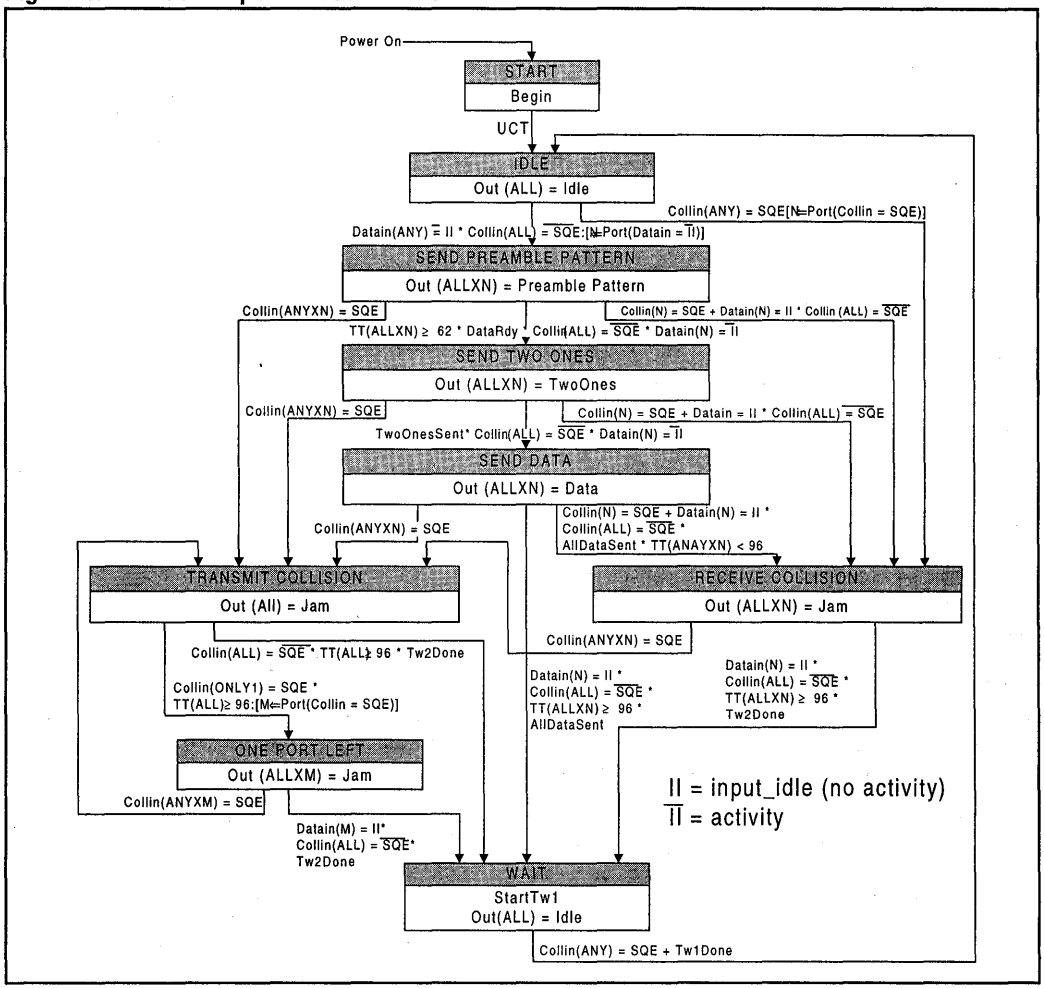
Manchester Code Violations

If the EMCV bit in the Master Configuration register is set, an input packet with Manchester Code Violations will be treated as a transmit collision. If this bit is clear (default), incoming packets with this type of error will simply be repeated to all ports. **Note that a packet that does not have a proper end-of-frame marker (2 bit times High with no transitions) will also be flagged as having a Manchester Code Violation.**

Data Rate Mismatches

Severe data rate mismatches will cause the internal FIFO to underflow or overflow. Depending on the state of the EFIFOERR bit, these conditions can be treated either as transmit collisions, or simply passed along as bad data.

Figure 4: LXT918 Repeater State Machine



Port Functions

Jabber (all ports)

If any input port is active for more than 5 ms, the device will automatically terminate all transmit activity for at least 96 bit times. This will give waiting ports an opportunity to access the network. A port that is continuously babbling will constantly collide with other ports, and will eventually be isolated by the auto-partitioning function.

Auto-partitioning (all ports)

Any port that causes 32 consecutive collisions will be *partitioned* as shown in Figure 5. A port will also be partitioned if it continues to be active for more than 100 µs after a collision has occurred. Once a port is partitioned, data received from that port is not repeated, until the port is *re-connected.* There are two re-connection algorithms. The normal algorithm allows a port to be reconnected if a packet can be successfully transmitted or received from the port. The alternative algorithm allows re-connection only if a packet can be successfully transmitted to the port. For re-connection to occur, at least 512 bit times of non-idle, non-collision activity must occur. Once this happens, the port is re-connected after the activity stops. The activity that causes the re-connection is *not* repeated.

Link Integrity Function (10BASE-T ports only)

The device supports the Link Integrity function, which is used to determine if a 10BASE-T connection is working. The function can be enabled on a port-by-port basis. When enabled, the device looks for Link Integrity Pulses from each of the 10BASE-T ports. When these pulses are received from a port, it is put into the "Link Up" state, enabling transmissions to the port, and vice versa. If the Link Integrity function is disabled, the port is forced into the Link Up state. The device generates Link Pulses to all ports, regardless of the Link State of any port or whether the Link Function is enabled or disabled.

Polarity Detection and Correction (10BASE-T ports only)

The device can detect reversed polarity on any 10BASE-T port and internally correct for it. This function can also be disabled on a port-by-port basis.

SQE Mask (AUI Port only)

Ethernet MAU devices (also known as transceivers) typically generate an SQE signal (also called heartbeat) on the CI inputs after each data transmission to the MAU. This function is normally supposed to be disabled when a MAU is attached to a repeater, but often times this is overlooked. The result can be a collision at the end of each packet transmitted. An SQE Mask function is provided to overcome this problem. When the Mask is set, SQE heartbeat signals from external MAU's will not be passed on as collisions.

Reverse AUI Mode

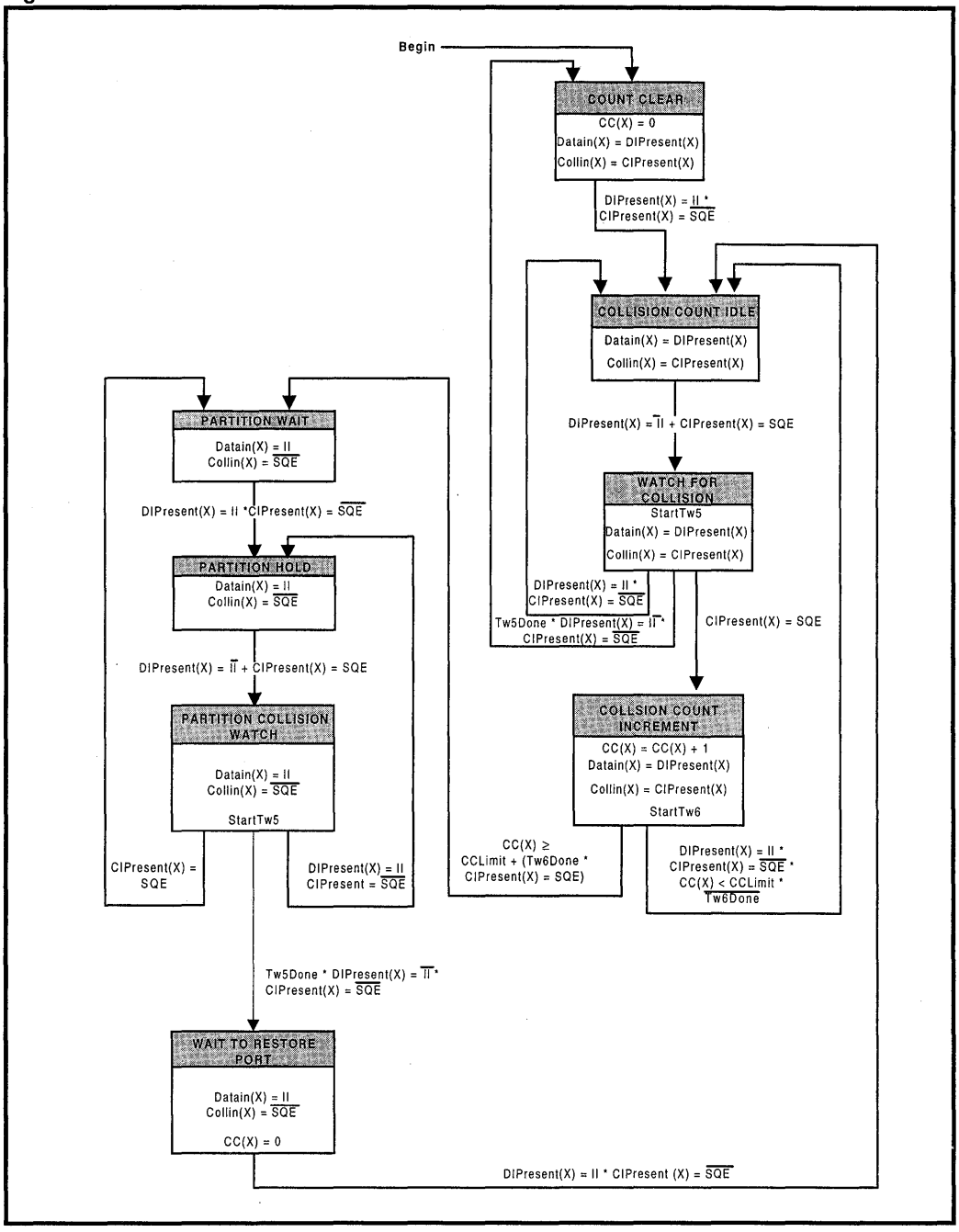
In the reverse mode, the AUI interface operates as a MAU rather than as a DTE. This allows it to directly interface to an LXT901/904/907. In this mode, the following apply:

- The CI pins function as outputs.
- The MaskSQE function determines whether or not the device generates SQE/heartbeat after each successful transmission to the device.
- The AUIDI pins continue to function as inputs, and the AUIDO pins continue to function as outputs. If these signals are being brought out to an external connector, they must be physically swapped from their normal positions (Refer to Figures 12 and 13.)
- The device will loopback data presented at the AUIDI inputs to the AUIDO outputs.

Reduced Squelch (10BASE-T ports only)

The squelch threshold on the 10BASE-T receivers can be lowered. This allows the device to detect weaker than normal signals, and can be used to support cables longer than 100m. It also makes the device more sensitive to cross-talk and other noise, and must be used with great care.

Figure 5: LXT918 Partition State Machine



LED Functions

The LXT918 provides a serial LED output and two global LEDs. Two programmable blink rates are provided. Refer to Table 49 for details.

Serial LEDs

The LXT918 provides a serial LED interface which should be attached to an external shift register. This interface provides status LEDs for the 10BASE-T and AUI ports. It also provides a global fault LED, a redundant power supply (RPS) LED and a user definable LED. Refer to Figure 18 in the Application section, and to Tables 10 and 11 below for details on the serial LED interface.

Activity and Collision LEDs (global)

These outputs can directly drive LEDs to indicate activity and collision status.

Table 10: LED-DAT Serial Port Bit Assignments

15[1]	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RPS	GF	UD	AUI	TP12	TP11	TP10	TP9	TP8	TP7	TP6	TP5	TP4	TP3	TP2	TP1

1. Bit 15 is shifted out first.

Table 11: Serial LED Operational Modes

Bit	Name	Software Control	Hardware Control		
			On	Slow	Off
15	RPS	N/A	Present, No Fault	Present & Fault	Any other state
14	Global Fault	On, Off or Slow Blink via Global LED Control Register, Address 181	N/A	Any Port Partitioned or RPS Fault	Any other state
13	User Definable		N/A		
12	AUI Port LEDs	On, Off or Fast Blink, via LED Control Register, Address 176	Enabled, Link Up, Not Partitioned	Partitioned	Any other state
11:0	TP Port LEDs				

IRB Operation

The Inter Repeater Backplane (IRB) allows multiple devices to operate as a single logical repeater, exchanging data collision status information. Each segment on the LXT918 has its own complete, independent IRB. Each backplane uses a combination of digital and analog signals as shown in Figure 6. In the following discussion '*x*' is used to indicate the segment number

Data Handling

Three signals - $\overline{\text{IRENA}x}$, IRDAT*x* and IRCLK*x* - are used to transmit data. All of them can be buffered between modules. A fourth signal - $\overline{\text{IRDEN}x}$ - provides directional control of this buffer. IRDAT*x*, $\overline{\text{IRENA}x}$ and $\overline{\text{IRDEN}x}$ need to be pulled High by 330 Ω resistors. During a collision, the LXT918 releases all four signals to prevent bus contention.

Collision Handling

Four signals - $\overline{\text{IRCOL}x}$, $\overline{\text{IRCOLBP}x}$, $\overline{\text{IRCFS}x}$ and $\overline{\text{IRCFSBP}x}$ - handle collisions. $\overline{\text{IRCFS}x}$ and $\overline{\text{IRCOL}x}$ should be connected between all the devices on any module. $\overline{\text{IRCFSBP}x}$ and $\overline{\text{IRCOLBP}x}$ should be connected between modules, to the devices that have ChipID = 0.

Collision States

There are three repeater collision states:

- Receive Collision - This occurs when an external transceiver detects a collision. On the LXT918, this can only happen on the AUI port.
- Transmit Collision - This occurs when two or more inputs become active at the same time.
- One Port Left - This is a special state that can occur after a Transmit Collision, when only one port remains active. This state prevents deadlocks in multiple-repeater configurations.

Collision Indications

$\overline{\text{IRCOL}x}$ and $\overline{\text{IRCOLBP}x}$ go Low to indicate any collision (receive, transmit or one-port-left). $\overline{\text{IRCFS}x}$ and $\overline{\text{IRCFSBP}x}$ are three-state signals which are used to detect when a transmit collision occurs. The three states are:

- Idle: High (+5V) Indicates that no ports are active.
- Single drive: Mid (+2.8V) Indicates that exactly one port is active (normal data transmission, receive collision, or one-port-left).
- Multiple-drive: Low (0V). Indicates that two or more ports are active (transmit collision).

$\overline{\text{IRCFSBP}x}$ indicates the number of active drivers across all the ports in a repeater stack. $\overline{\text{IRCFS}x}$ indicates the number of active drivers on the local board, and the first 96-bits of a non-local transmit collision (defined as a collision between a local port and a non-local port, or between two non-local ports). The state of $\overline{\text{IRCFS}x}$ is fed forward to $\overline{\text{IRCFSBP}x}$ by the device with ChipID = 0. To prevent dead-locks, $\overline{\text{IRCFSBP}x}$ is NOT fed back to $\overline{\text{IRCFS}x}$. During non-local transmit collisions, the signal HOLDCOL*x* is used to hold the local devices in the transmit collision state. Table 12 summarizes the use of these signals.

Collision Hold (HOLDCOL)

Each segment can produce a HOLDCOL signal to prevent dead-locks between $\overline{\text{IRCFS}}$ and $\overline{\text{IRCFSBP}}$. The device with ChipID = 0 drives HOLDCOL High to indicate that a transmit collision is in progress, and that local devices should remain in the transmit collision state.

MAC IRB Access

The MACACTIV1:4 pins allow external MACs or other digital ASICs to interface directly to the IRB via any of the LXT918 segments. When a segment's MACACTIV pin is asserted, the LXT918 will drive the associated $\overline{\text{IRCFS}}$ and $\overline{\text{IRCFSBP}}$ signals on behalf of the external device, allowing it to participate in the transmit collision detection function of $\overline{\text{IRCFS}}$ and $\overline{\text{IRCFSBP}}$.

IRB Isolation

The ISOLATE1:4 outputs are provided to control the enable pins of external bidirectional transceivers. In multi-module applications, they can be used to isolate one module from the rest of the system. Only one device can control these signals. The output states of these pins are controlled by the Isolate bits in the Master Configuration Register.

MMSTRIN / MMSTROUT

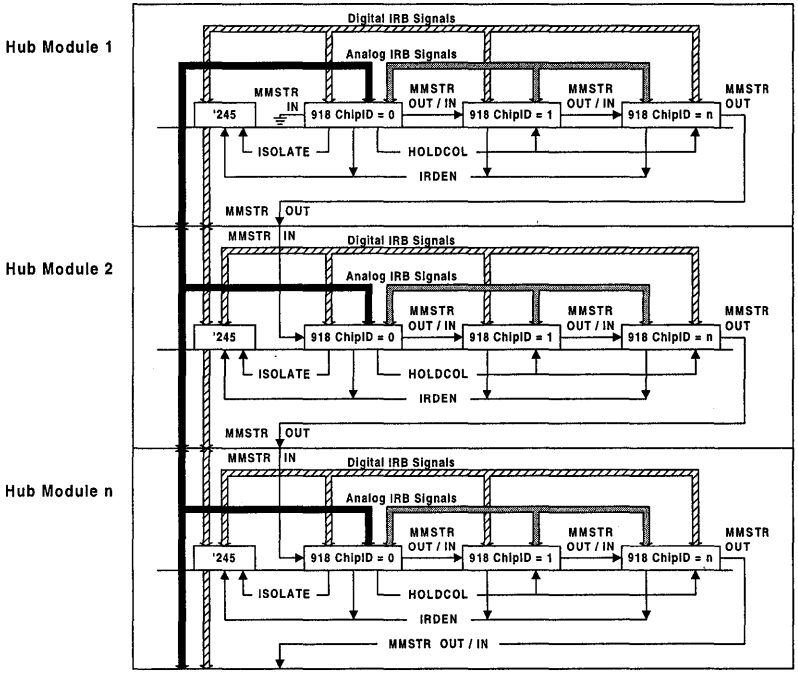
This daisy chain is provided for correct gathering of statistics in multiple-device configurations. In multiple-module applications, this daisy chain must be maintained across modules. In stand-alone applications, or for the first device in a chain, the MMSTRIN input must be pulled Low in order for the management counters to work correctly.

Table 12: $\overline{\text{IRCOL}}$ and $\overline{\text{IRCFS}}$ Condition Indications

Condition	$\overline{\text{IRCOLBP}}$	$\overline{\text{IRCOL}}$	$\overline{\text{IRCFSBP}}$[3]	$\overline{\text{IRCFS}}$[3]
Idle	High	High	High	High
Local Data	High	High	Mid	Mid
Non-Local Data	High	High	Mid	High
Local RxCol or OPL [1]	Low	Low	Mid	Mid
Non-local RxCol/OPL [1]	Low	Low	Mid	High
Local TxCol or first 96 bits of non-local TxCol [2]	Low	Low	Low	Low
Non-local TxCol after 96 bits [2]	Low	Low	Low	Mid or High

1. Receive Collision (RxCol) and One Port Left (OPL) conditions have identical bus characteristics and can be differentiated only by timing. Fragment extensions are generally treated as receive collisions.
2. Manchester code violations and FIFO overruns are generally treated as transmit collisions.
3. Signal employs 3-state logic: High = 5V; Mid = 2.8V; Low = 0V.

Figure 6: IRB Block Diagram



This diagram shows a single IRB. The LXT918 actually has four independent IRBs, one per segment.

- Digital IRB signals include IRDAT, IRENA and IRCLK.
- Local Analog IRB signals include IRCOL and IRCFS.
- Inter-Module Analog IRB signals include IRCOLBP and IRCFSBP.

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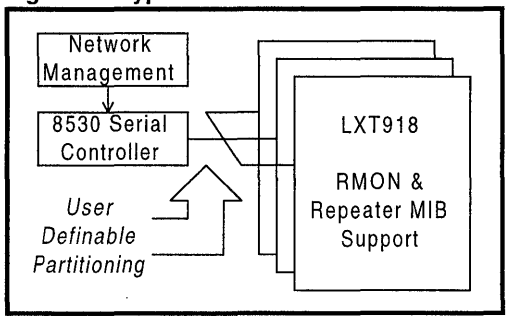
Serial Management Interface

The serial management interface provides access to Repeater MIB variables, RMON Statistics attributes and status and control information. A network manager can access the interface through a simple serial communications controller. The interface is designed to be used in a multi-drop configuration, allowing multiple LXT918 devices to be managed from one common line.

The interface consists of a data input line (SRX), data output line (STX) and a clock (SERCLK), and can operate up to 1 Mbps. The interface operates on a simple command response model, with the network manager as the master and the LXT918 devices as slaves. Figure 7 is a simplified view of typical serial management interface architecture.

Figure 7: Typical Serial I/F Architecture



Serial Clock

SERCLK is a bidirectional pin; direction control is provided by the RECONFIG input. If RECONFIG is High, the LXT918 will drive SERCLK at 625 kHz. If RECONFIG is Low, SERCLK is an input, between 0 and 1 MHz. There is no lower bound to how slow the interface can operate. The clock can be stopped after each operation, as long as an idle (ten 1's in a row) is transmitted first.

Serial Data I/O

The serial data pins, SRX and STX, should be tied together. The SRX input is compared with the STX output. If a mismatch occurs, STX goes to a high impedance. STX is driven on the falling edge of SERCLK; SRX is sampled on the rising edge.

Management Format

Normally the network manager directs read and write operations to a specific LXT918 device using a two-part address consisting of HubID and ChipID. The interface allows up to 127 32-bit registers to be read at one time. Up to two registers can be written at a time.

The interface uses a simple frame format, which is shown in Figure 8. All frames begin and end with a flag of consisting of "01111110". All fields are transmitted LSB first. Zero-bit stuffing is required if more than five 1's in a row appear in the header, data or CRC fields. In addition, all operations directed to the device must be followed by an idle (ten 1's in a row), and the first operation must be preceded with an idle.

Figure 8: Serial Management Frame Format

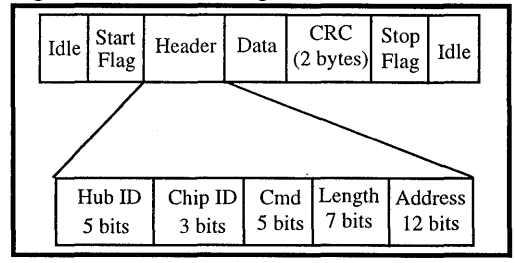


Table 13: Serial Management Frame Message Fields

Message	Description
Start or Stop Flag	"01111110". Protocol requires zero insertion after any five consecutive "1's" in the data stream.
Hub ID	Identifies module or sub-system. Assigned by one of two arbitration mechanisms at power-up.
Chip ID	Identifies one of eight modules on a system. Assigned by 3 external pins on each device.
Command	Identifies the particular operation being performed (see Table 14)
Length	Specifies number of registers to be transferred (1 to 127). Maximum is 2 per write, 127 per read.
Address	Specifies address of register or register block to be transferred.

1. All fields are transmitted LSB first.

Table 14: Serial Management Instruction Set

Command Value	Name	Usage	Normally Sent By	Description
18 (Hex)	Write	Normal Ops	Network Mgr	Used to write up to 2 registers (8 bytes) at a time.
04 (Hex)	Read	Normal Ops	Network Mgr	Used to read up to 127 registers at a time.
08 (Hex)	RequestID	Arbitration	LXT918	Requests Hub ID. Repeated periodically.
00 (Hex)	ConfigChg	Arbitration	LXT918	Notifies system of configuration change (hot swap). Requests new arbitration phase.
10 (Hex)	Re-arbitrate	Arbitration	Network Mgr	Re-starts arbitration
14 (Hex)	Assign HubID	Arbitration Mech. 2	Network Mgr	Assigns Hub ID to device with ARBIN=0 and ARBOUT = 1 (top of chain)
0C (Hex)	Set ARBOUT to 1	Arbitration Mech. 2	Network Mgr	Commands specific device to set ARBOUT to 1.
1C (Hex)	Set ARBOUT to 0	Arbitration Mech. 2	Network Mgr	Commands specific device to set ARBOUT to 0
02 (Hex)	DevID	Config	Network Mgr	Generic command for reading device type (no register address needed).

Table 15: Typical Serial Management Packets

Message	Contents of Fields in Serial Management Packet					
	Hub ID	Chip ID	Command	Length	Address	Data
Write	User Defined	User Defined	18 (Hex)	01 or 02	User Defined	User Defined
Read Request	User Defined	User Defined	04 (Hex)	01 to 7F Hex	User Defined	Null
Read Response	00000	000	04 (Hex)	Echo	Echo	Data Values
Assign Hub ID (Arb Method 1)	11111	111	18 (Hex)	02	188 Hex	Formatted per Table 51
Assign Hub ID (Arb Method 2)	11111	111	14 (Hex)	01	0	Hub ID (LSB) and 27 0's
Set ARBOUT To 1	User Defined	User Defined	0C (Hex)	00	0	Null
Arb Request	00000	000	08 (Hex)	02	190	PROM ID
Re-Arbitrate	11111	111	10 (Hex)	00	0	Null
Request Device ID	User Defined	User Defined	02 (Hex)	01	0	Null
Device ID Response	00000	000	02 (Hex)	01	185	Formatted per Table 50
Config Change	thirteen 0's					

AUI Configuration Register

The AUI Configuration Register (Address 184) operates differently from the rest of the Serial Management Interface. This 16-bit register is loaded from an external shift register which can be implemented using a pair of LS'165 devices. Three dedicated pins: AUICONFIG_IN, CONFIG_CLK and CONFIG_ENA are used to load the register (refer to Table 2 for pin

assignments and signal descriptions). Bits 15:1 may be used to hold up to 15 bits of user-defined board or system configuration data.

Bit 0 (LSB) sets the AUI port operating mode as follows:

- 0 = Normal (DTE) mode
- 1 = Reversed (MAU) mode

Two events cause shift register data to be loaded into the AUI Configuration Register: reset/power-up and a management read of Register 184. To load new data into the register, two reads are required. The first read reflects the initial content and causes the register to shift in data from AUICONFIG_IN. The new data will be reflected in the second read.

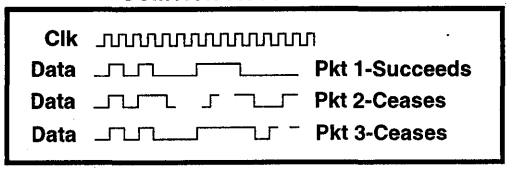
Address Arbitration

Each device has a two part address, consisting of a HubID and a ChipID. The ChipID is assigned the input pins CHIPID<2:0>. The HubID is assigned through one of two arbitration mechanisms.

Arbitration Mechanism #1: EPROM Method

This method requires that a PROM be located on each module, and that the ARBSELECT pin (71) not be pulled Low. At power-up, the device with ChipID = 0 reads a 48-bit ID from the PROM. All other devices on the module listen in and also record this ID. The device with ChipID = 0 then transmits "Arbitration Request Messages" on the Serial Management Interface every 2-3 milliseconds. The request messages from two modules may collide; if this happens a resolution scheme ensures that only one message will win (see Figure 9). The network manager responds to each request with a message that includes the 48-bit ID and the HubID. All devices hear this message, but only those that match the 48-bit ID receive the HubID as their own. Once the HubID is assigned, the device with ChipID=0 stops sending request messages. It is possible for response messages to be lost due to collisions with request messages.

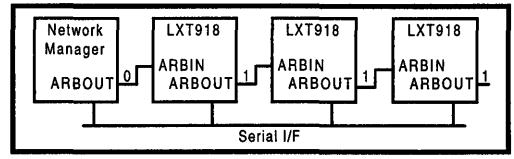
Figure 9: Arbitration Mechanism #1 : Collision Resolution



Arbitration Mechanism #2: Chain Method

In this method, all of the devices are daisy-chained using the ARBIN and ARBOUT pins as shown in Figure 10. The ARBIN input of the first device is directly connected to an output of the network manager. At power-up all the devices drive their ARBOUT outputs High while the network manager drives the ARBIN input to the first device Low. The manager transmits a special "Assign Hub ID" message which is recognized only by the device with ARBIN = Low and ARBOUT = High. The network manager then sends a command addressed to this device which commands it to set its ARBOUT pin Low. This cycle repeats until all devices have been assigned a HubID.

Figure 10: Arbitration Mechanism #2: ARBIN/OUT Chain Links



Address Re-arbitration

There are two mechanisms for address re-arbitration following a configuration change, such as a module hot-swap:

- Device power up - At power-up, the LXT918 normally sends out a "Configuration Change" message (all 0's) on the bus, which causes re-arbitration.
- The network manager can direct or re-start arbitration at any time by sending the "Re-arbitrate" command.

Source Address Utilities

Source Address Tracking Function

Each port has two source address tracking registers. The rptrAddrTrackNewLastSrcAddress register for each port continuously tracks the source addresses of packets emanating from that port. The Authorized Address Register operates in three modes: it can free run, lock, or lock on the next packet. In any mode, it can always be updated by network management.

Source Address Matching Function

Each segment has a Source Address Matching Function to discover which port or ports sourced packets with a particular Source Address. The input to the function is an Ethernet Address; the output is a register which identifies any ports that sourced packets with that Source Address.

APPLICATION INFORMATION

Magnetics Information

The LXT918 requires a 1:1 ratio for the TP receive transformers and a 1:1.41 ratio for the TP transmit transformers. Table 16 lists suitable transformers by manufacturer and part number. This information was valid as of the printing date of this document. Before committing to a specific component, designers should contact the manufacturer for current product specifications, and should test and validate the magnetics for the specific application to verify that system requirements are met.

Layout Requirements

The Twisted Pair Interface

The layout of the twisted-pair port is critical in complex designs. Run the traces directly from the LXT918 to the discrete termination components (located close to the transformers).

The transformer isolation voltage should be rated at 2 kV to protect the circuitry from static voltages across the connectors and cables. The traces running from the transformers to the connector should run in close pairs directly to the connector. Be careful not to cross the transmit and receive pairs. One way to avoid this problem is to run the receive pairs on the component side and the transmit pairs on the solder side. Careful planning during the schematic and layout stages can avoid these problems.

The PCB layout should have no ground or power planes between the transformers and the connectors. The data signals should be the only traces in this area. Place the chassis ground for the connectors near the edge of the PCB, away from the signals, connecting the connector shield with the chassis.

The RBIAS Pin

The RBIAS signal sets the levels for the output drivers. Any emissions or common mode noise entering the device here could be measured on the twisted pair output signals.

The LXT918 requires a 22 kΩ, 1% resistor directly connected between the RBIAS pin and ground. These traces should be as short as possible. The ground traces from adjacent GND pins should come directly off of the device to enclose the resistor and pin forming a shielded area between the RBIAS connection and other signals on the PCB.

Typical Application Circuitry

Figures 11 through 19 show typical LXT918 application circuitry. Table 17 summarizes signal operation of the three AUI signal pairs in the two modes (normal and reversed).

Table 16: Suggested Magnetics List[1]

Manufacturer	Quad Transmit	Quad Receive	Quad Tx/Rx (Octal)
BEL	S553-5999-02	S553-5999-03	
HALO	TD54-1006L1 TG54-1006N2	TD01-1006L1 TG01-1006N2	TG44-S010NX TG45-S010NX TG46-S010NX
Nanopulse	5976	5977	
Kappa	TP4003P	TP497P101	
PCA	EPE6009	EPE6010	
TDK	TLA-3T107	TLA-3T106	
VALOR	PT4116	PT4117	

1. Before committing to a specific component, designers should contact the manufacturer for current product specifications, and should test and validate the magnetics for the specific application to verify that system requirements are met.

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Figure 11: Typical 10BASE-T Port Interface

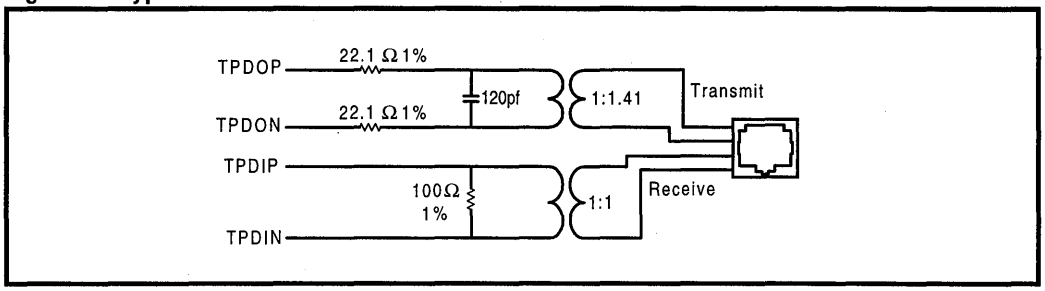

Figure 12: Normal AUI Circuit

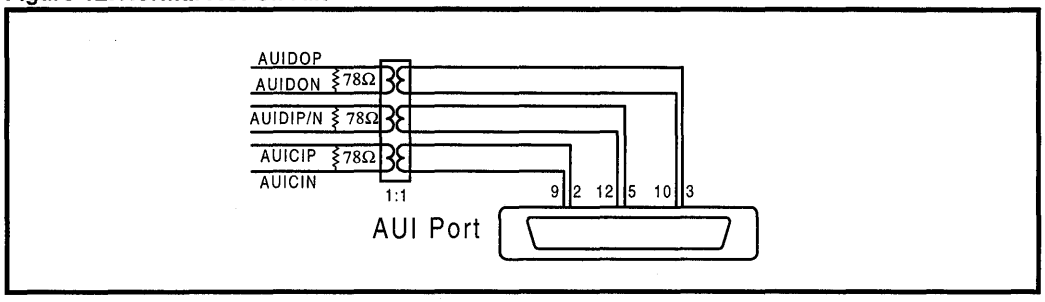

Figure 13: Reversed AUI Circuit

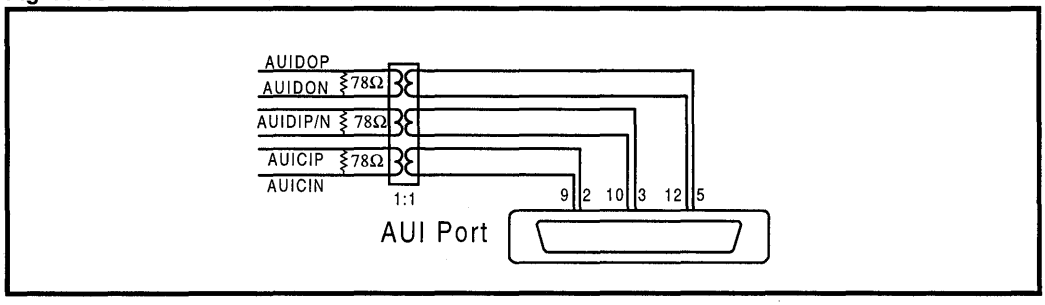

Table 17: AUI Signals - Direction and Pin-Out

LXT918		AUI Connector Pin #	
Signal	Pin #	Normal	Reversed
DOP	198	3	5
DON	199	10	12
DIP	200	5	3
DIN	201	12	10
CIP	202	2	2
CIN	203	9	9

Figure 14: Typical IRB Implementation

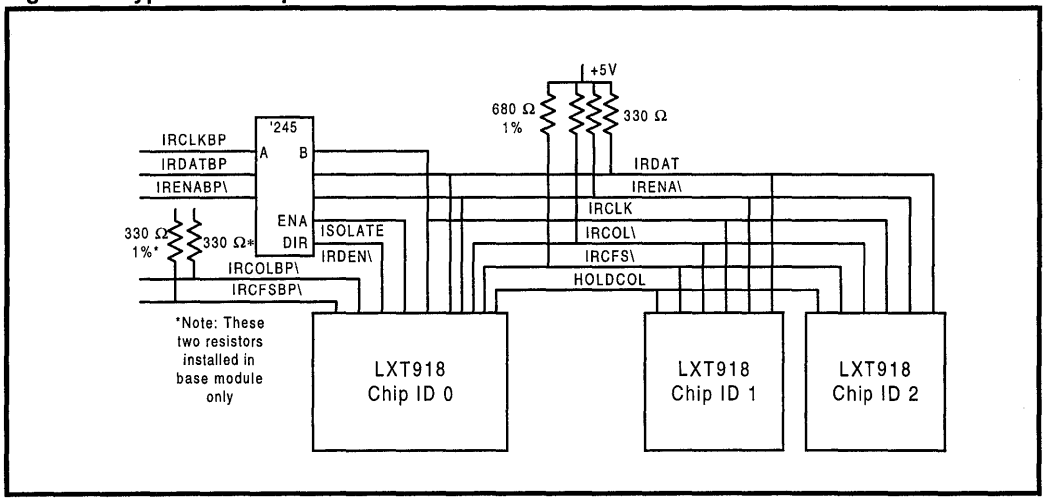

Figure 15: Typical Serial Management Interface Connections

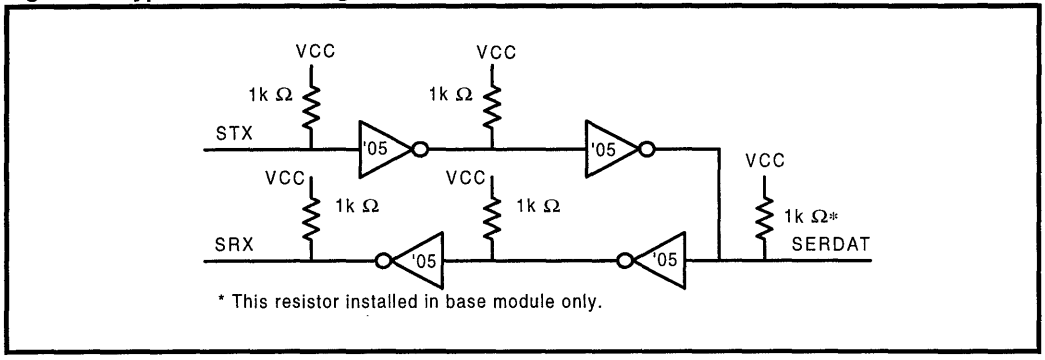

Figure 16: Typical Chip ID Architecture

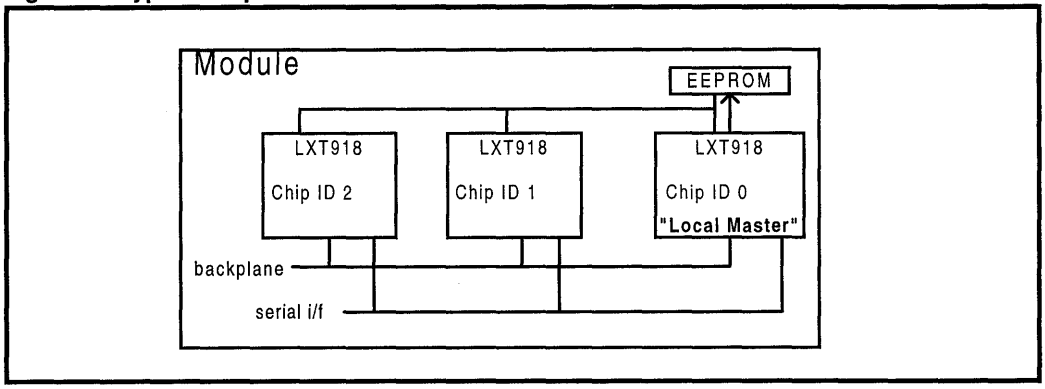

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Figure 17: Typical EPROM Circuit

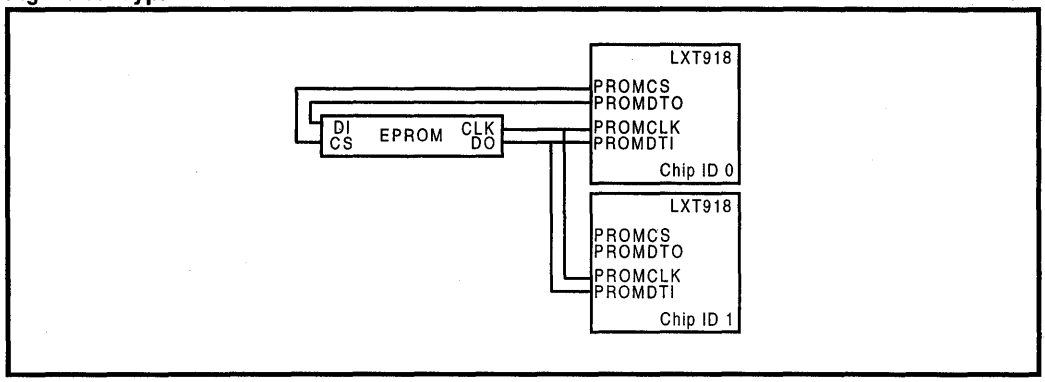


Figure 18: Typical Serial LED Interface Circuit

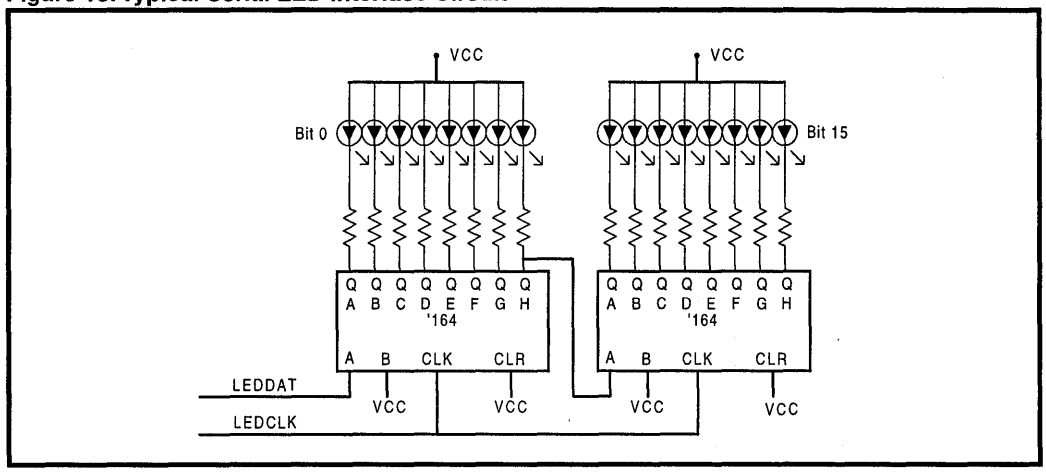
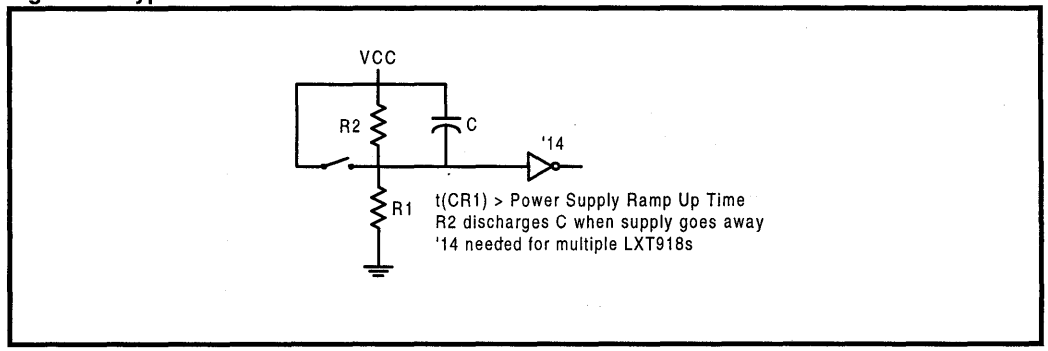


Figure 19: Typical $\overline{\text{RESET}}$ Circuit



TEST SPECIFICATIONS

NOTE

The minimum and maximum values in Tables 18 through 28 and Figures 20 through 24 represent the performance specifications of the LXT918 and are guaranteed by test, except where noted by design

Table 18: Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Supply voltage	VCC	-0.3	6	V
Operating temperature	TOP	0	70	°C
Storage temperature	TST	-65	+150	°C

CAUTION

Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 19: Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Recommended supply voltage[1]	VCC	4.75	5.0	5.25	V	
Recommended operating temperature	TOP	0	–	70	°C	
VCC current	ICC	–	400	–	mA	

1. Voltages with respect to ground unless otherwise specified.

Table 20: I/O Electrical Characteristics (Over Recommended Range)

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Input Low voltage	VIL	–	–	0.8	V	TTL inputs
		–	–	2.0	V	CMOS inputs [2]
		–	–	1.0	V	Schmitt Trigger #1
		–	–	1.0	V	Schmitt Trigger #2
Input High voltage	VIH	2.0	–	–	V	TTL inputs
		VCC-2.0	–	–	V	CMOS inputs [2]
		VCC-1.0	–	–	V	Schmitt Trigger #1
		VCC-2.0	–	–	V	Schmitt Trigger #2
Hysteresis voltage	–	1.0	–	–	V	Schmitt Trigger #1
		0.5	–	–	V	Schmitt Trigger #2

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Does not apply to IRB pins. Refer to Table 23 for IRB I/O characteristics.

Table 20: I/O Electrical Characteristics (Over Recommended Range) – continued

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Output Low voltage	VOL	–	–	0.4	V	IOL = 1.6 mA
Output Low voltage (LED)	VOLL	–	–	1.0	V	IOLL = 10 mA
Output High voltage	VOH	2.4	–	–	V	IOH = 40 µA
Input Low current	IIL	-100	–	–	µA	
Input High current	IIH	–	–	100	µA	
Output rise / fall time	–	–	3	10	ns	CLOAD = 15 pF

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Does not apply to IRB pins. Refer to Table 23 for IRB I/O characteristics.

Table 21: 10BASE-T Electrical Characteristics (Over Recommended Range)

Parameter		Symbol	Min	Typ[1]	Max	Units	Test Conditions
Transmitter	Transmit output impedance	ZOUT	–	2	–	Ω	
	Peak differential output voltage	VOD	2.2	2.5	2.8	V	Load = 100Ω at TPOP/ TPON
	Transmit timing jitter addition	–	–	±2	±10	ns	0 line length for internal MAU
	Transmit timing jitter added by the MAU and PLS sections	–	–	±1	±5.5	ns	After line model specified by IEEE 802.3 for 10BASE-T internal MAU
Receiver	Receive input impedance	ZIN	20	36	–	kΩ	Between TPIP/TPIN
	Differential squelch threshold - Normal	VDSN	300	420	585	mV	5 MHz square wave input
	Differential squelch threshold - Reduced	VDSR	150	250	350	mV	5 MHz square wave input

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 22: AUI Electrical Characteristics (Over Recommended Range)

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Differential output voltage	VOD	±550	–	±1200	mV	
Receive input impedance	ZIN	20	36	–	kΩ	Between CIP/CIN & DIP/DIN
Differential squelch threshold	VDS	150	250	350	mV	

1. Typical values are at 25° C and are for design aid only; they are not guaranteed and not subject to production testing.

Table 23: IRB Electrical Characteristics (Over Recommended Range)

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Output Low voltage	VOL	–	.3	.7	V	RL = 330 Ω
Output rise or fall time	TF	–	4	10	ns	CL = 15 pF
Input High voltage	VIH	VCC - 2.0	–	–	V	CMOS inputs
Input Low voltage	VIL	–	–	2.0	V	CMOS inputs
$\overline{\text{IRCFS}}$ current	–	2.6	3.3	4.0	mA	RL = 680 Ω
$\overline{\text{IRCFSBP}}$ current	–	5.4	6.7	8.3	mA	RL = 330 Ω

1. Typical values are at 25° C and are for design aid only; they are not guaranteed and not subject to production testing.

Table 24: Repeater Timing Characteristics[1] (Over Recommended Range)

Parameter	Symbol	Min	Typ[2]	Max	Units	Test Conditions
AUI DIN active to $\overline{\text{IRENA}}$ Low	trep1	–	2	3	BT[4]	
TP DIN to $\overline{\text{IRENA}}$ Low	trep2	–	5	7	BT	
$\overline{\text{IRENA}}$ Low to AUI DOP active	trep3	–	3	4	BT	
$\overline{\text{IRENA}}$ Low to TP DOP active	trep4	–	4	5	BT	
IRCLK rising edge to IRDAT rising edge.	trep5	25	–	55	ns	330 Ω pullup, 150 pF load on IRDAT. 1k Ω pullup, 150 pF load on IRCLK. All measurements at 2.5V.
IRCLK rising edge to IRDAT falling edge.	trep6	5	–	25	ns	
AUI DIN idle to $\overline{\text{IRENA}}$ High	trep7	–	–	8	BT	
TP DIN idle to $\overline{\text{IRENA}}$ High	trep8	–	–	11	BT	
$\overline{\text{IRENA}}$ High to AUI DOP idle	trep9	–	–	5	BT	
$\overline{\text{IRENA}}$ High to TP DOP idle	trep10	–	–	5	BT	

1. This table contains propagation delays from the TP and AUI ports to the IRB, and from the IRB to the AUI and TP ports, for normal repeater operation (start of packet, end of packet). All values in this table are output timings.
2. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
3. There is a delay of approximately 13 to 16 bit times between the assertion of $\overline{\text{IRENA}}$ and the assertion of IRCLK and IRDAT. This delay does not affect repeater operation because downstream devices begin generating preamble as soon as $\overline{\text{IRENA}}$ is asserted.
4. BT = Bit Times (100 ns).

Figure 20: Repeater Timing

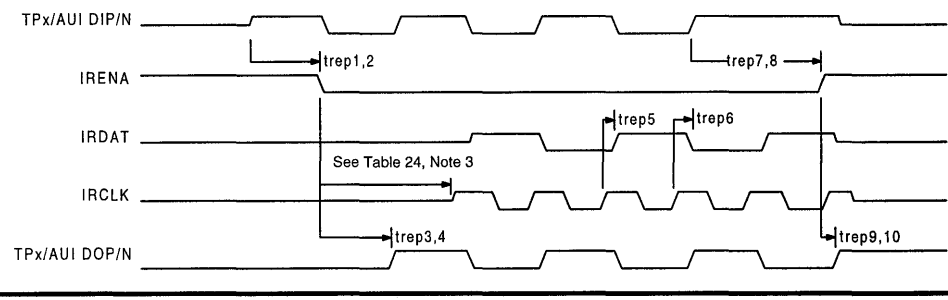


Table 25: MAC Interface Transmit Timing Characteristics [1] (Over Recommended Range)

Parameter	Symbol	Min	Typ[2]	Max	Units	Test Conditions
TXD to TXC setup time	tmactx1	20	–	–	ns	TXD valid to TXC rising edge [3]
TXC to TXD hold time	tmactx2	5	–	–	ns	TXC rising edge to TXD change [3]
TXE to TP DOP prop delay	tmactx3	–	6	7	BT	TXE High to TPDOP active [4]

1. This table contains propagation delay times for the 7-pin MAC interface.
2. Typical values are at 25° C and are for design aid only; they are not guaranteed and not subject to production testing.
3. Input.
4. Output.

Figure 21: MAC Interface Transmit Timing

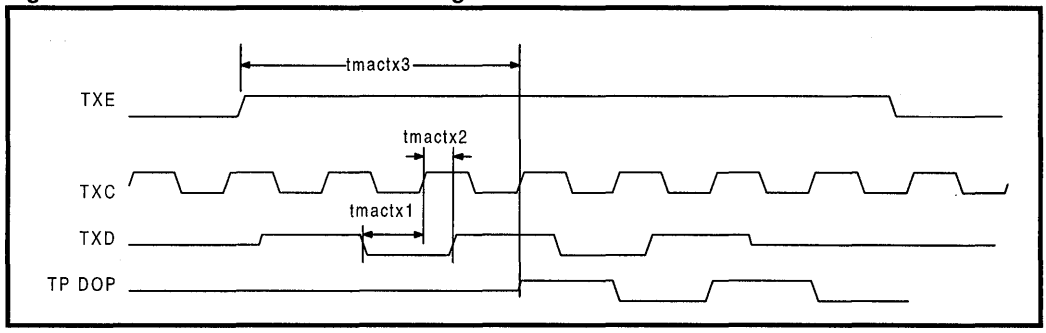


Table 26: MAC Interface Receive Timing Characteristics [1] (Over Recommended Range)

Parameter	Symbol	Min	Typ[2]	Max	Units	Test Conditions
RXC to RXD prop delay	tmacrx1	–	–	10	ns	Falling edge of RXC to RXD valid
TP/AUI to CRS delay	tmacrx2	–	9	10	BT	TP/AUI DIP active to CRS High
Number of extra receive clocks	tmacrx3	–	5	–	ea	RXC rising edges after CRS Low

1. This table contains propagation delay times for the 7-pin MAC interface outputs.
2. Typical values are at 25° C and are for design aid only; they are not guaranteed and not subject to production testing.

Figure 22: MAC Interface Receive Timing

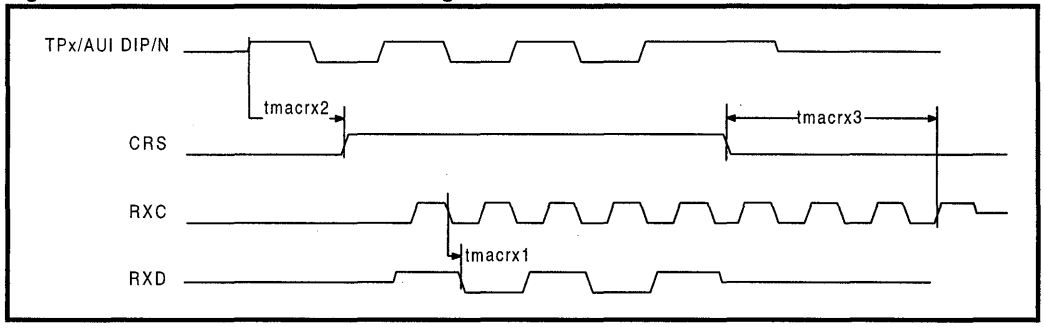


Table 27: MACACTIVE Delays - MAC/IRB Interface Characteristics (Over Recommended Range)

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
MACACTIV to $\overline{\text{IRENA}}$ assertion delay [3]	tmacbp1	–	100	–	ns	MACACTIV High to $\overline{\text{IRENA}}$ Low [2]
IRDAT to IRCLK setup time	tmacbp2	21	–	–	ns	IRDAT valid to IRCLK rising edge [2]
IRDAT to IRCLK hold time	tmacbp3	0	–	–	ns	IRCLK rising edge to IRDAT change [2]

1. Typical values are at 25° C and are for design aid only; they are not guaranteed and not subject to production testing.
2. Input.
3. External devices should allow at least one 10 MHz clock cycle (10 ns) between assertion of MACACTIV and $\overline{\text{IRENA}}$.

Figure 23: MACACTIVE Timing (MAC to IRB Interface)

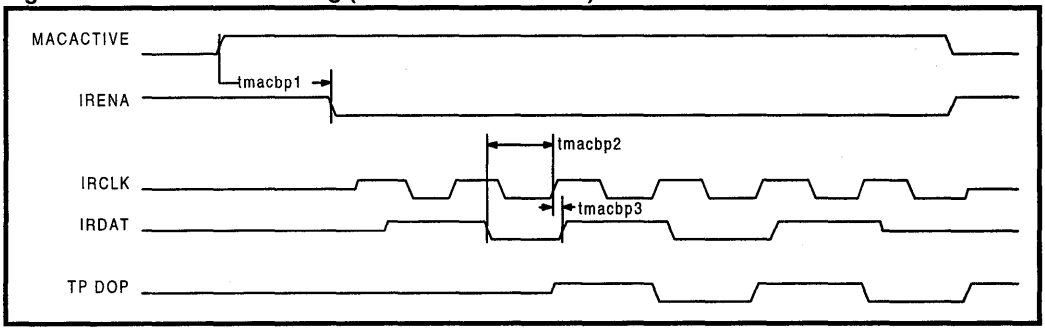
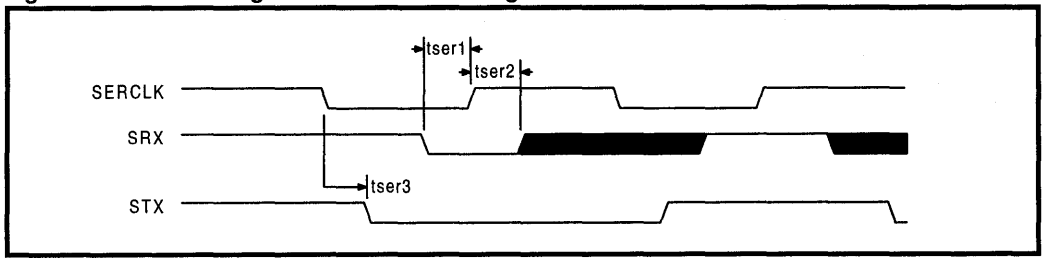


Table 28: Serial Management Interface Timing Characteristics (Over Recommended Range)

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Data to Clock setup	tser1	100	–	–	ns	SRX valid to SERCLK rising edge [2]
Clock to Data Hold Time	tser2	100	–	–	ns	SERCLK rising edge to SRX change [2]
Data Propagation Delay	tser3	–	–	100	ns	SERCLK falling edge to STX valid [3]

1. Typical values are at 25° C and are for design aid only; they are not guaranteed and not subject to production testing.
2. Input.
3. Output.

Figure 24: Serial Management Interface Timing



REGISTER DEFINITIONS

Introduction

The LXT918 register set is composed of multiple 32-bit registers (and a single 16-bit register) of the following types:

- Configuration Registers
- Control and Status Registers
- Ethernet Address Registers
- Counters

Table 29 lists the register base memory locations. Refer to Tables 30 through 54 for specific addresses and bit assignments. *Note that all register addresses are specified in hexadecimal*

Table 29: Memory Map

Base Address	Register Type	Notes
184	AUI Configuration	1 Register. This is the only 16-bit register in the LXT918. The AUI Configuration Register is loaded from an external shift register and may be read via the Serial Management Port.
181	Configuration	11 Registers
170	Control and Status	9 Control Registers, 7 Status Registers
156	Ethernet Address	12 Search Registers
13C		Authorized Port Address, 2 per port (TP and AUI)
120		Port Address Tracking, 2 per port (TP, AUI and MAC)
118	Counters	MAC Interface Counters, 8 Registers
100		Segment 4 Interface Counters, 18 Registers
0F0		Segment 3 Interface Counters, 18 Registers
0E0		Segment 2 Interface Counters, 18 Registers
0D0		Segment 1 Interface Counters, 18 Registers
0C0		AUI Port Counters, 15 Registers
0B0		TP Port 12 Counters, 15 Registers.
0A0		TP Port 11 Counters, 15 Registers.
090		TP Port 10 Counters, 15 Registers.
080		TP Port 9 Counters, 15 Registers.
070		TP Port 8 Counters, 15 Registers.
060		TP Port 7 Counters, 15 Registers.
050		TP Port 6 Counters, 15 Registers.
040		TP Port 5 Counters, 15 Registers.
030		TP Port 4 Counters, 15 Registers.
020		TP Port 3 Counters, 15 Registers.
010		TP Port 2 Counters, 15 Registers.
000		TP Port 1 Counters, 15 Registers.

Counter Registers

As shown in Table 30, all counters are 32-bit, read-only, "little-Endian" registers, with undetermined values at power-up. The "Zero Counters" bit in the Master Configuration Register allows all counters to be "zeroed".

Table 30: Counter Registers Bit Assignments

31	30	29	28	27	26	25 : 7	6	5	4	3	2	1	0
D31	D30	D29	D28	D27	D26	D25:D7	D6	D5	D4	D3	D2	D1	D0

Port Counter Registers

Table 31 contains descriptions of the per-port counters for the TP ports and the AUI port. These descriptions are intended to be illustrative. For the exact definitions of these counters, refer to the Repeater MIB, RFC 1516. To obtain the address of a particular register for a particular port, add the offset value for the register (from Table 31) to the base address for that port (from Table 29).

Table 31: Port Counter Registers

Name	Offset	Description[1]
rptrMonitorPortReadableFrames	0	Counts valid-length (64 to 1518 bytes), valid-CRC, collision-free packets. Depending on the state of the CountMode bit in the Master Configuration Register, this counter will count either all packets (CountMode=0) or only Unicast Packets (CountMode=1) Minimum roll-over time = 80 hours
rptrMonitorPortReadableOctets	1	Counts the number of octets in the packets counted by the rptrMonitor-PortReadableFrames counter, not including preamble and framing bits. Minimum roll-over time = 58 minutes.
rptrMonitorPortFrameCheckSe-quence	2	Counts valid length, collision-free packets that had FCS errors, but were correctly framed (had an integral number of octets). Minimum roll-over time = 80 hours.
rptrMonitorPortAlignmentErrors	3	Counts valid length, collision-free packets that had FCS errors and were incorrectly framed (had a non-integral number of octets) . Minimum roll-over time = 80 hours.
rptrMonitorPortFramesTooLong	4	Counts packets that had a length greater than 1518 octets. Minimum roll-over time = 61 days.
rptrMonitorPortShortEvents	5	Counts events that lasted for 82 bit times or less. Minimum roll-over time = 16 hours.
rptrMonitorPortRunts	6	Counts events longer than 82 bit times, but shorter than 512 bit times. Minimum roll-over time = 16 hours.
rptrMonitorPortCollisions	7	Counts the number of collisions that occurred, not including late collisions. Minimum roll-over time = 16 hours.
rptrMonitorPortLateEvents	8	Counts the number of times collision was detected more than 512 bit times after the start of carrier. Minimum roll-over time = 81 hours.

1. All Port Counters are Read Only.

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Table 31: Port Counter Registers – continued

Name	Offset	Description[1]
rptrMonitorPortVeryLongEvents	9	Counts the number of times any activity continued for more than 4 to 7.5 ms. Minimum roll-over time = 198 days.
rptrMonitorPortDataRateMismatches	A	Counts the number of times the incoming data rate mismatched the local clock source enough to cause a FIFO underflow or overflow.
rptrMonitorPortAutoPartitions	B	Counts the number of times this port has been partitioned by the Auto-partition algorithm.
rptrTrackSourceAddrChanges	C	Counts the number of times the source address has changed. Minimum roll-over time of 81 hours.
rptrMonitorPortBroadcastPkts	D	Counts the number of good broadcast packets received by this port.
rptrMonitorPortMulticastPkts	E	Counts the number of good multicast packets received by this port.

1. All Port Counters are Read Only.

Interface Counter Registers

Table 32 contains descriptions of the segment counters, which are intended to be illustrative. For the exact definition of these counters, refer to the RMON MIB, RFC 1757. To arrive at the address of a particular register for a particular segment, add the offset for that register (shown below) to the base address for the segment (refer to Table 29), except for repeaterMonitorTotalOctets and repeaterMonitorTotalCollisions.

Table 32: Interface Counter Registers

Name	Offset[1]	Description[2]
etherStatsOctets	0	The number of data octets including those in bad packets and octets in FCS fields, but does not include preamble or other framing bits.
etherStatsPkts	1	The number of packets received from the network, including errored packets.
etherStatsBroadcastPkts	2	The number of good broadcast packets received.
etherStatsMulticastPkts	3	The number of good multicast packets received.
etherStatsCRCAlignErrors	4	The number of valid-length packets (64 to 1518 bytes inclusive) that had a bad Frame Check Sequence (FCS).
etherStatsUndersizePkts	5	The number of well-formed packets that were smaller than 64 octets.
etherStatsOversizePkts	6	The number of well-formed packets that were longer than 1518 octets.
etherStatsFragments	7	The number of ill-formed packets less than 64 octets. Note: Any event without a start-of-frame delimiter (0-octet packet) will be counted as a fragment, no matter how long it is.
etherStatsJabbers	8	The number of ill-formed packets longer than 1518 octets. An ill-formed packet is one with an FCS error.
etherStatsCollisions	9	The best estimate of the total number of collisions on this interface.
etherStatsPkts64Octets	A	The number of packets (good and bad) that were 64 octets long.
etherStatsPkts65to127Octets	B	The number of packets (good and bad) between 65 and 127 octets long.

1. Absolute addresses are given for repeaterMonitorTotalOctets and repeaterMonitorTotalCollisions
2. All Interface Counters are Read Only

Table 32: Interface Counter Registers – continued

Name	Offset[1]	Description[2]
etherStatsPkts128to255Octets	C	The number of packets (good and bad) between 128 and 255 octets long.
etherStatsPkts256to511Octets	D	The number of packets (good and bad) between 256 and 511 octets long.
etherStatsPkts512to1023Octets	E	The number of packets (good and bad) between 512 and 1023 octets long.
etherStatsPkts1024to1518Octets	F	The number of packets (good and bad) between 1024 and 1518 octets long.
rptrMonitorTotalOctets	110 (Seg 1) 111 (Seg 2) 112 (Seg 3) 113 (Seg 4)	These per-segment counters record the total number of octets received on each interface.
rptrMonitorTransmitCollisions	114 (Seg 1) 115 (Seg 2) 116 (Seg 3) 117 (Seg 4)	These per-segment counters record the total number of transmit collisions that occurred each interface.

1. Absolute addresses are given for repeaterMonitorTotalOctets and repeaterMonitorTotalCollisions
2. All Interface Counters are Read Only

Port Counters for the 7-pin MAC Interface

Port Counters for the 7-pin MAC Interface are described in Table 33. These counters are a subset of the port counters for the other ports. Refer to Table 30 for bit assignments.

Table 33: MAC Interface Registers

Name	Type[1]	Addr	Description
MAC Interface-Readable-Frames	R	118	Valid-length (64 to 1518 bytes), valid-CRC, non-collision frames. Depending on the state of the CountMode bit in the Master Configuration Register, this counter counts either all valid packets (CountMode=0) or Unicast packets only (CountMode=1). Minimum roll-over time = 80 hours.
MAC Interface-Readable-Octets	R	119	Octets contained in MAC Interface-ReadableFrames. Minimum roll-over time = 58 minutes.
MAC Interface-Runts	R	11A	Number of packets and events shorter than 512 bit times. Minimum roll-over time = 16 hours.
MAC Interface-Collisions	R	11B	Number of collisions that were detected on this interface. Minimum roll-over time = 16 hours.
MAC Interface-FCS/FAE	R	11C	Valid length (64-1518 bytes), non-collision packets with FCS errors. Minimum roll-over time = 80 hours.
MAC Interface-Broadcast	R	11D	Number of good broadcast packets received from this port.
MAC Interface-Multicast	R	11E	Number of good multicast packets received from this port.
MAC Interface-SAchanges	R	11F	Number of times the source address has changed. Minimum roll-over time = 81 hours.

1. R = Read Only.

Ethernet Address Registers

All Ethernet Address Registers consist of two 32-bit registers that together contain a 48-bit Ethernet address. Refer to Table 34 for register bit assignments.

Table 34: Ethernet Address Register Bit Assignments

Upper Address	Bits 15:0 contain bits 47:32 of the Ethernet Address.
Lower Address	Bits 31:0 contain bits 31:0 of the Ethernet Address.

Port Address Tracking Registers

The Port Address Tracking Register set is described in Table 35. These registers continuously monitor the Source Addresses of packets emanating from the corresponding ports. Refer to Table 34 for bit assignments.

Table 35: Port Address Tracking Registers

Name	Type[1]	Addr	Description
rptrAddrTrackNewLastSrcAddress-TP Port 1	R/W	120, 121	
rptrAddrTrackNewLastSrcAddress-TP Port 2	R/W	122, 123	
rptrAddrTrackNewLastSrcAddress-TP Port 3	R/W	124, 125	
rptrAddrTrackNewLastSrcAddress-TP Port 4	R/W	126, 127	
rptrAddrTrackNewLastSrcAddress-TP Port 5	R/W	128, 129	
rptrAddrTrackNewLastSrcAddress-TP Port 6	R/W	12A, 12B	
rptrAddrTrackNewLastSrcAddress-TP Port 7	R/W	12C, 12D	
rptrAddrTrackNewLastSrcAddress-TP Port 8	R/W	12E, 12F	
rptrAddrTrackNewLastSrcAddress-TP Port 9	R/W	130, 131	
rptrAddrTrackNewLastSrcAddress-TP Port 10	R/W	132, 133	
rptrAddrTrackNewLastSrcAddress-TP Port 11	R/W	134, 135	
rptrAddrTrackNewLastSrcAddress-TP Port 12	R/W	136, 137	
rptrAddrTrackNewLastSrcAddress-AUI Port	R/W	138, 139	
rptrAddrTrackNewLastSrcAddress-MAC Port	R/W	13A, 13B	

1. R/W = Read / Write

Authorized Port Address Registers

The Authorized Port Address Register set is described in Table 36. The operation of these registers is determined by the Authorization Control Register. Refer to Table 34 for bit assignments.

Table 36: Authorized Port Address Registers

Name	Type[1]	Addr	Description
Authorized Address Register - TP Port 1	R/W	13C, 13D	
Authorized Address Register - TP Port 2	R/W	13E, 13F	
Authorized Address Register - TP Port 3	R/W	140, 141	
Authorized Address Register - TP Port 4	R/W	142, 143	
Authorized Address Register - TP Port 5	R/W	144, 145	
Authorized Address Register - TP Port 6	R/W	146, 147	
Authorized Address Register - TP Port 7	R/W	148, 149	
Authorized Address Register - TP Port 8	R/W	14A, 14B	
Authorized Address Register - TP Port 9	R/W	14C, 14D	
Authorized Address Register - TP Port 10	R/W	14E, 14F	
Authorized Address Register - TP Port 11	R/W	150, 151	
Authorized Address Register - TP Port 12	R/W	152, 153	
Authorized Address Register - AUI Port	R/W	154, 155	

1. R/W = Read / Write

Search Registers

The Search Register set is described in Table 37.

Table 37: Search Registers

Name	Type[1]	Addr	Description
Search Address Register - Segment 1	R/W	156,157	Each register-pair specifies an Ethernet Source Address to match on the corresponding segment. Refer to Table 34 for bit assignments
Search Address Register - Segment 2	R/W	158,159	
Search Address Register - Segment 3	R/W	15A,15B	
Search Address Register - Segment 4	R/W	15C,15D	
Search Result Register - Segment 1	R	160	Each register indicates which ports on a particular segment sent packets with source addresses that matched the register pair described in the row above. Refer to Table 38 for bit assignments (bit 13 not used). These registers clear when read.
Search Result Register - Segment 2	R	161	
Search Result Register - Segment 3	R	162	
Search Result Register - Segment 4	R	163	

1. R/W = Read / Write.
R = Read Only.

Control and Status Registers

The Control and Status Register set includes general port control and status registers which conform to the bit assignments shown in Table 38, and additional control and status registers with alternate bit assignments shown in Tables 40 through 45.

Table 38: Port Control and Status Register Bit Assignments

31:14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Rsvd	MAC	AUI	TP12	TP11	TP10	TP9	TP8	TP7	TP6	TP5	TP4	TP3	TP2	TP1

1. Bits 13:12 not used in all registers. Refer to individual register descriptions.

General Port Control Registers

The General Port Control Register set is described in Table 39. Refer to Table 38 for Port Control Register bit assignments. Bits 12 and 13 are not used in all cases (refer to specific register descriptions).

Table 39: Port Control Registers

Name	Type[1]	Addr	Description
Enable Register	R/W	171	Writing a 1 to any bit enables the transmitter and receiver on the corresponding port, writing a 0 disables them. Changing a port's status while the network is active may cause packet fragments to be generated. If the $\overline{\text{MG\_PRSNT}}$ pin is Low, this register will initialize to all 0's (all ports disabled). If the $\overline{\text{MG\_PRSNT}}$ pin is High, this register will initialize to all 1's (all ports enabled).
Reserved	-	172	
Reserved	-	173	
Alternate Partition Register	R/W	174	Writing a 1 to any bit enables the alternate partition algorithm (re-connect on transmit only) for the corresponding port, a 0 the normal algorithm (re-connect on transmit or receive). (Bits 31:13 not used)
Link Control Register	R/W	178	Writing a 1 to any bit enables the Link Partition Algorithm for the corresponding Twisted Pair port, writing a 0 disables it. When this function is disabled, the port automatically goes to Link Pass state and continues to transmit link pulses. (Bits 31:12 not used; Power-up state is all 1's)
Polarity Control Register	R/W	179	Writing a 1 to any bit disables polarity correction for the corresponding Twisted Pair port. (Bits 31:12 not used)
Squelch Control Register	R/W	17A	Writing a 1 to any bit enables the receiver for the corresponding port to use reduced squelch levels for longer-distance cables; writing a 0 enables normal squelch levels to be used. (Bits 31:12 not used)

1. R/W = Read/Write.

Interrupt Status Register

The Interrupt Status Register is described in Table 41. Refer to Table 40 for bit assignments.

Table 40: Interrupt Status Register Bit Assignments

Bits 31:3	Bit 2	Bit 1	Bit 0
Reserved	Jabber	Source Address Change - TP Port	Source Address Change - AUI Port

Table 41: Interrupt Status Register

Name	Type[1]	Addr	Notes
Interrupt Status Register	R	17B	Indicates one of three interrupt conditions. Clears when read. Power-up state is all 0s.

1. R = Read Only

Port Status Registers

The Port Status Register set is described in Table 42. Refer to Table 38 for bit assignments.

Table 42: Port Status Registers

Name	Type[1]	Addr	Notes
AUI Status Register	R	17C	Reports SQE (heartbeat) and Loopback status of AUI port. Refer to Table 44 for details.
Link Status Register	R	17D	A "1" in any bit position indicates the corresponding port is in the "Link Up" state. (Bits 31:12 not used)
Partition Status Register	R	17E	A "1" in any bit position indicates the corresponding port has been partitioned. (Bits 31:13 not used.)
Polarity Status Register	R	17F	A "1" in any bit position indicates that the polarity for the corresponding port has been reversed (Bits 31:12 not used.)
SA Change Detection Register	R	180	A "1" in any bit position indicates that the Source Address has changed on the corresponding port. (Bits 31:13 not used.)

1. R = Read Only.

AUI Control and Status Registers

The AUI Control and Status Register set is described in Table 44. Refer to Table 43 for bit assignments.

Table 43: AUI Control and Status Register Bit Assignments

Register	Bits 31:2	Bit 1	Bit 0
AUI Control	Reserved	Reserved	SQE Mask
AUI Status	Reserved	Loopback	SQE (Heartbeat) Status

Table 44: AUI Control and Status Registers

Name	Type[1]	Addr	Description
AUI Control Register	R/W	177	This bit controls masking or generation of the AUI "heartbeat", defined as brief activity on the AUI CI pair generated by the MAU shortly after successful completion of a transmission. The power-up state of this register is "0". **When the AUI is functioning as a DTE** - If this bit is 1 the device will not react to heartbeat, other than to update the AUI status register. If this bit is 0, the device will react to heartbeat by going into a full receive collision. **When the AUI is functioning as a MAU** - If this bit is 1, the device will not generate heartbeat; if it is 0, the device will generate heartbeat.
AUI Status Register	R	17C	This register reports SQE and Loopback status of AUI port when the LXT918 is operating as the DTE, and has no function when the operating as the MAU). **SQE Heartbeat Status** - This bit indicates the presence or absence of a heartbeat signal from an external MAU (1 = present, 0 = absent). This function operates regardless of the state of the SQE Mask bit in the AUI Control Register. **Loopback** - This bit indicates whether or not data loopback was detected from an external MAU (1 = present, 0 = absent.)

1. R/W = Read/Write.
R = Read Only.

Port Switch, Authorization and LED Control Registers

The Port Switch, Authorization and LED Control Registers are described in Table 46. Refer to Table 45 for bit assignments.

Table 45: Port Switch, Authorization and LED Control Register Bit Assignments[1]

31:28	27:26	25:24	23:22	21:20	19:18	17:16	15:14	13:12	11:10	9:8	7:6	5:4	3:2	1:0
Rs'vd	MAC	AUI	TP12	TP11	TP10	TP9	TP8	TP7	TP6	TP5	TP4	TP3	TP2	TP1

1. Bits 27:26 used by Port Switch Control Register only.

Table 46: Port Switch, Authorization and LED Control Registers

Name	Addr	Description[1]
Port Switch Control Register	170	This register controls the mapping of ports to segments. Each port is assigned two bits in this register, as shown in Table 45. For each set of bits, the mapping is as follows: 00 = Segment 1 01 = Segment 2 10 = Segment 3 11 = Segment 4
Authorization Control Register	175	Determines the operational mode of the Authorized Address Register for each port. 00 = Free-Run. The Authorized Address Register continuously re-learns its contents from the source addresses of incoming packets (Power-up default). 01 = Next Lock. The Authorized Address Register learns the source address of the next valid packet and locks. Once it locks, the corresponding bits in this register automatically change to '10'. 10 = Lock. The Authorized Address Register does not change with traffic flow. In this mode, it can only be updated under network management control. 11 = Reserved.
LED Control Register	176	Controls operation of the serial LED bits associated with each port. The power-up state of this register is all 1's if an external manager is detected, and defaults to "hardware control" otherwise. 00 = LED off 01 = LED fast blink 10 = hardware control 11 = LED on

1. The Port Switch Control Register, Authorization Control Register and the LED Control Register are all Read/Write.

Configuration Registers

Configuration Registers are listed in Table 47. Bit assignments for the Configuration Registers are shown in Table 48 through 53. The Master Configuration Register is defined in Table 54.

Table 47: Configuration Registers

Name	Type[1]	Addr	Notes
Global LED Control Register	R/W	181	Refer to Table 48 for bit assignments. This register controls the operating modes of the Global Fault LED and User Defined LED. Bit Encodingas follows: **Global Fault LED** 00 = Off 01 = Hardware Control 10 = Slow Blink 11 = On Steady **User Defined LED** 00 = Off 01 = Fast Blink 10 = Reserved 11 = On Steady
LED Timer Register	R/W	182	Refer to Table 49 for bit assignments. Bits 8-15 of this register set the fast blink frequency of the LEDs. Bits 0-7 set the slow blink frequency. The same formula is used in each case, with a maximum of 128 Hz and a minimum of 0.5 Hz (for example, fast blink = 32 (0.4 s); slow blink = CC (1.6 s)).
Master Configuration Register	R/W	183	Refer to Tables 53 and 54 for bit assignments and definitions. At power-up, all bits in this register default to 0.
AUI Configuration Register	R/W [2]	184	Bit 0 sets the AUI port mode (0 = Normal, 1 = Reversed). Bits 15:1 may contain user-defined configuration data.
Device ID Register	R	185	This register follows the IEEE 1149.1 specification; refer to Table 50 for bit assignments. The upper 4 bits identify the device revision level. The next 16 bits store the Part ID Number in hexadecimal, which is '0396'. The lower 12 bits contain a JEDEC Manufacturer ID, which for Level One is hexadecimal 'FE'.
Repeater Reset Register	W	186	Writing any data value to this register causes all functional logic to reset, but does not affect the state of counters, configuration registers or status registers.
Software Reset Register	W	187	Writing any data value to this register is identical to a hardware reset. Everything is reset except counters and addresses.
HUB ID Register (1 and 2)	W	188, 189	Refer to Table 51 for bit assignments. Writing a valid 48-bit ID (one that matches the EPROM ID) to this register causes the device to change its Hub ID to the contents of the EPROM ID register listed below. This register cannot be read.
EPROM ID Register (1 and 2)	R	190, 191	These two registers contain the 48-bit ID read in from EPROM at power-up. Refer to Table 52 for bit assignments.

1. R = Read Only.
   W = Write Only.
   R/W = Read/Write.
2. Writes to Register 184 are accomplished via the AUICONFIG_IN pin, not via the STX pin. Reads to Register 184 are standard, except that 2 reads are required to ensure new data is shifted into the register after a change.

Table 48: Global LED Control Register Bit Assignments

31:4	3	2	1	0
Reserved	Global Fault LED		User Defined LED	

Table 49: LED Timing Control Register Bit Assignments

31:16	15:8	7:0
Reserved	Fast Blink Frequency	Slow Blink Frequency

1. Period = 7.8125 ms x (Register Value + 1)

2. Frequency = $\frac{1}{7.8125 \text{ ms} \times (\text{Register Value} + 1)}$

Table 50: Device ID Register Bit Assignments

31:28	27:12	11:8	7:1	0
Version	Part ID	Jedec Continuation Characters	JEDEC ID	Chip ID
XXXX	0000 0011 1001 0110	0000	111 1110	0

Table 51: Hub ID Register Bit Assignments

Upper Address	31:21 - All 0s	20:16 - Hub ID	15:0 - Must match bits 15:0 of upper EPROM ID Register
Lower Address	31:0 - Must match bits 31:0 of lower EPROM ID Register		

Table 52: EPROM ID Register Bit Assignments

Upper Address	31:16 - All 0s	15:0 - Bits 15:0 of Address read from EPROM
Lower Address	31:0 - Bits 47:16 of Address read from EPROM	

Table 53: Master Configuration Register Bit Assignments

31:11	10	9	8:5	4	3	2	1	0
Reserved	Arbin	Zero Counters	Isolate 4:1	CountMode	Soft Reconnect	EFIFOERR	EMCV	Reserved

Table 54: Master Configuration Register Bit Definitions

Bit	Name	Type[1]	Description	Default
31:11	Reserved	-	Write as 0, ignore on read.	N/A
10	Arbin	R	This bit shows the value present at the ARBIN input pin.	0
9	Zero Counters	R/W	Setting this bit to "1" will cause all counters to be zeroed. Upon completion of this operation, the device will reset this bit to "0".	0
8:5	Isolate4:1	R/W	Each of these bits controls the corresponding Isolate output. Setting any bit to "1" causes the corresponding Isolate output pin to be asserted High.	0
4	CountMode	R/W	This bit affects the operation of the portReadableFrames and MACReadableFrames counters. Setting this bit to 0 will cause these counters to count all readable frames; setting this bit to 1 will cause these counters to count only readable unicast frames.	0
3	Soft Reconnect	R/W	Setting this bit to 1 enables the Soft Reconnect feature of the device. When this feature is enabled, when a port switch is initiated (by writing to the Port Switch Register), the device waits until traffic is idle before removing the port from the old segment, or adding it to the new segment.	0
2	EFIFOERR	R/W	This bit determines whether the device will enter the Transmit Collision State if its internal FIFO overflows or underflows (data-rate mismatch). 0 = no, 1 = yes.	0
1	EMCV	R/W	This bit determines whether the device will enter the Transmit Collision State upon reception of a Manchester Code Violation; 0 = no, 1 = yes.	0
0	Reserved	-	Write as 0, ignore on read.	N/A

1. R/W = Read/Write.
   R = Read Only.

LAN Application Notes

LXT902 and 906

Impedance Matching for Shielded and Unshielded Twisted-Pair Lines

General Description

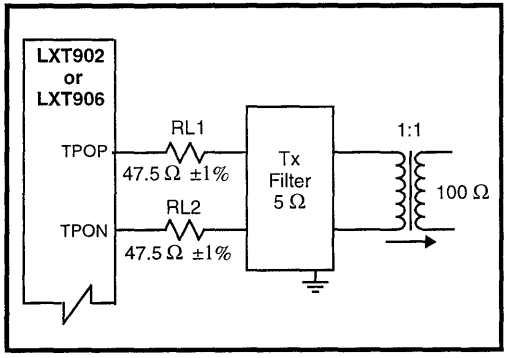
The LXT902 Media Attachment Unit (MAU) and LXT906 Twisted-Pair/Coax (TP-CX) Adapter both require impedance matching with the network media. This application note provides a short explanation of the impedance matching networks required for shielded and unshielded twisted-pair lines. This information applies to both the LXT902 and the LXT906

Transmit Line Matching

On the transmit side, the LXT902 and LXT906 use resistors in line with the output as shown in the figure below. To provide an optimum match, the total impedance of the resistors and the filter should equal the line impedance:

RL1 + RL2 + ZF = ZL.

Transmit Line Interface



Receive Line Matching

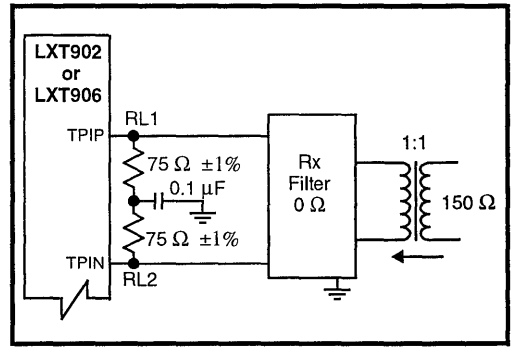
On the receive side the LXT902 and LXT906 use a pair of resistors across the input with the center node tied to ground through a capacitor as shown in the figure below. To provide an optimum impedance match, use the same formula as used for the transmit side:

RL1 + RL2 + ZF = ZL.

Typical Examples

For example, when the network media is 100 Ω UTP and the filter impedance is 5 Ω, each resistor value should be 47.5 Ω. When the network media is 150 Ω STP and the filter impedance is 0 Ω, each resistor value should be 75 Ω. This simple formula provides optimum impedance matching for both the transmit and receive line interfaces.

Receive Line Interface



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NOTES

Design Guide for LXT901/907 Ethernet Interface

Connection to Motorola MC68EN360 Controller

General Description

This application note describes a method for connecting the LXT901 or LXT907 Ethernet Interface Adapter to the Motorola MC68EN360 Quad Integrated Communications Controller (QUICC) with Ethernet capability. The QUICC/LXT901 combination makes designing routers, bridges, print servers and other, similar products simple and fast.

The LXT901 and LXT907 devices have advanced features that make design and fabrication faster and cheaper than typical competitors' products. These two devices meet all of the Motorola QUICC design requirements with minimal external circuitry needed to use the MC68EN360 features. Either of these devices gives the lowest cost, highest performance possible with the Motorola QUICC.

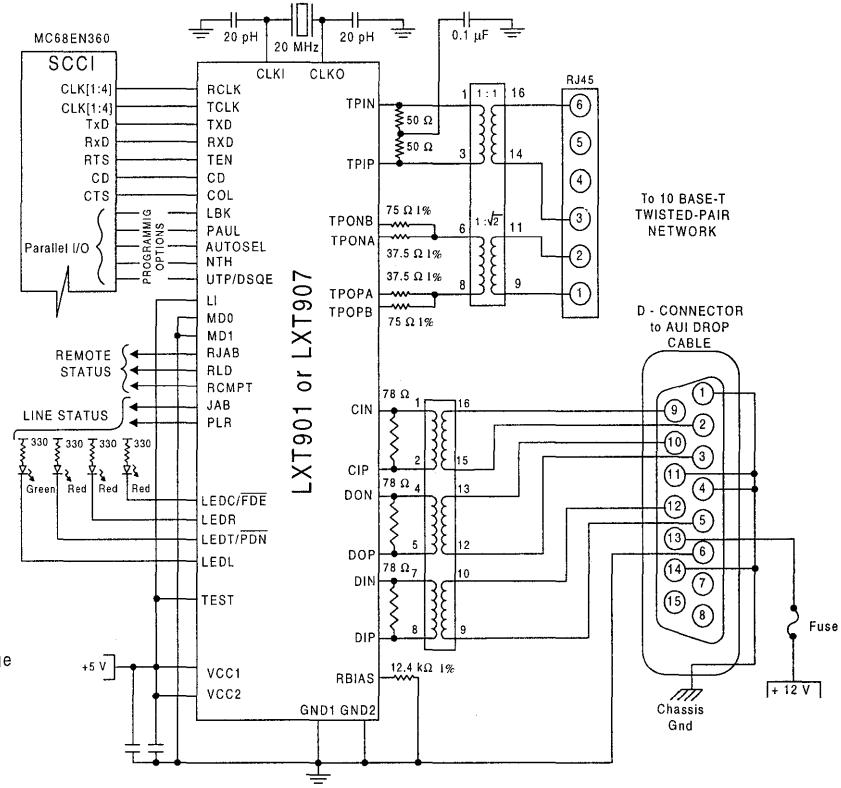
LXT901/LXT907 Device Features

- Glueless interface to the MC68EN360 QUICC controller in 10 Mbps Ethernet/IEEE 802.3 LAN with either twisted- pair connection or AUI transceiver
- Integrated filters make design faster, fabrication cheaper
- Integrated LED drivers for operation monitoring
- Supports full duplex operation
- Automatic port selection makes choosing between the twisted-pair and AUI options seamless

Applications

This application note addresses the Ethernet LAN side of the circuit only. To connect to a T1 or E1 network, use a Level One LXT301/305 family or an LXT310 or LXT318 transceiver.

Typical LXT901/LXT907 Device and MC68EN360 QUICC Connection



NOTE:
LXT 901/907 pin-out varies with IC package design. See Table 1.

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LXT90x / QUICC Interface

The LXT901 device is available in either a 44-pin PLCC format or a 64-pin TQFP package. The LXT907 device is available in the 44-pin PLCC form. The two PLCC packages are pin compatible except for pin 37. This pin is UTP (unshielded/shielded twisted-pair select) on the LXT901 and DSQE (Disable SQE) on the LXT907 device.

The following pins on the LXT901 or LXT907 device connect to the MC68EN360 SCC1 signals as shown.

Table 1: Pin Connections

LXT901/LXT907 Device			Motorola QUICC MC68EN360 SCC1 Signal
PLCC Pin	TQFP Pin	Signal	
28	47	RCLK	CLK1-4[1]
11	23	TCLK	CLK1-4[1]
12	24	TXD	TXD
26	45	RXD	RXD
13	25	TEN	RTS[2]
27	46	CD	CD[2]
16	28	COL	CTS[2]
22	38	LBK	Connect these bits to the Parallel I/O bus on the QUICC[3] and program as needed.
40	3	PAUI	
17	29	AUTOSEL	
4	13	NTH	
37 (901)	59	UTP	
37 (907)	n/a	DSQE	

1. The design must provide separate clocks for TCLK and RCLK. Any of the clocks on the QUICC will do.
2. These signals are active high in this application.
3. Please check the Motorola specification for the connections needed for the desired result.

Setting QUICC Parameters

Refer to the Motorola MC68360 Quad Integrated Communications Controller User's Manual for settings required to make the QUICC function. Be aware of the following:

Only SCC1 has Ethernet communications capability. Use SCC1 for the LAN connection, and use another SCC (or a parallel) port for the other side of the connection.

Bypass both the Digital Phase-Locked Loop (DPLL) and Manchester Encoding/Decoding function for Ethernet operation.

The TCI (Time Clock Invert) bit must be High to allow the QUICC to clock the data out to the LXT901 or LXT907 device on the rising edge of the clock pulse. This improves data setup time at the 10 Mbps speed used by Ethernet. TCI is bit 28 of the General SCC Mode Register (GSMR).

The MODE bits (0~3) must be set to 1, 1, 0, 0 respectively. The Transparent Receiver (TRX) and Transparent Transmitter bits (TTX), bits 43 and 44, must both be 0 (normal operation) or 1 (transparent operation). Do not mix TRX and TTX values. The 0 setting is recommended; in transparent mode, the QUICC does not manipulate protocols in the data stream.

The Transmit FIFO Length (TFL) bit should be 0. TFL is bit 38 in the GSMR. The Receive FIFO Width (RFW) bit, bit 37, should also be 0.

GSMR bits 19 and 20 are the Transmit Preamble Pattern (TPP) bits. For Ethernet operation, set them to 0, 1 to transmit a repeating 10 pattern as a preamble.

Figure 1 shows a typical set up for a full duplex 10BASE-T LAN connection, using the LXT907 device. This application requires only the TP transformer, two 18 pF capacitors, two 330 Ω resistors, two 24.9 Ω 1% resistors, one 12.4 kΩ 1% resistor, and a green LED. The 20 MHz clock signal is common in all 10BASE-T applications, so no crystal is required. All QUICC parameters remain the same.

This completes the Ethernet/IEEE 802.3 LAN side of the circuit setup. There are other steps in designing a working circuit that go beyond the scope of this application note.

Layout Guidelines

Fabricate the circuit as shown in the diagram on page 1. Take care to isolate the bias circuit at RBIAS and locate the resistor close to the pin. If this resistor is not positioned properly it may act as an antenna and cause erratic performance. Keep it away from other components or signal traces, and do not run any signals under the resistor. Be sure to use a bypass capacitor at each Vcc pin.

External Components

The application on page 1 requires two DIP transformer packages for isolation and impedance matching on the AUI or twisted-pair transmit and receive lines. Recommended transformers are listed in Table 2.

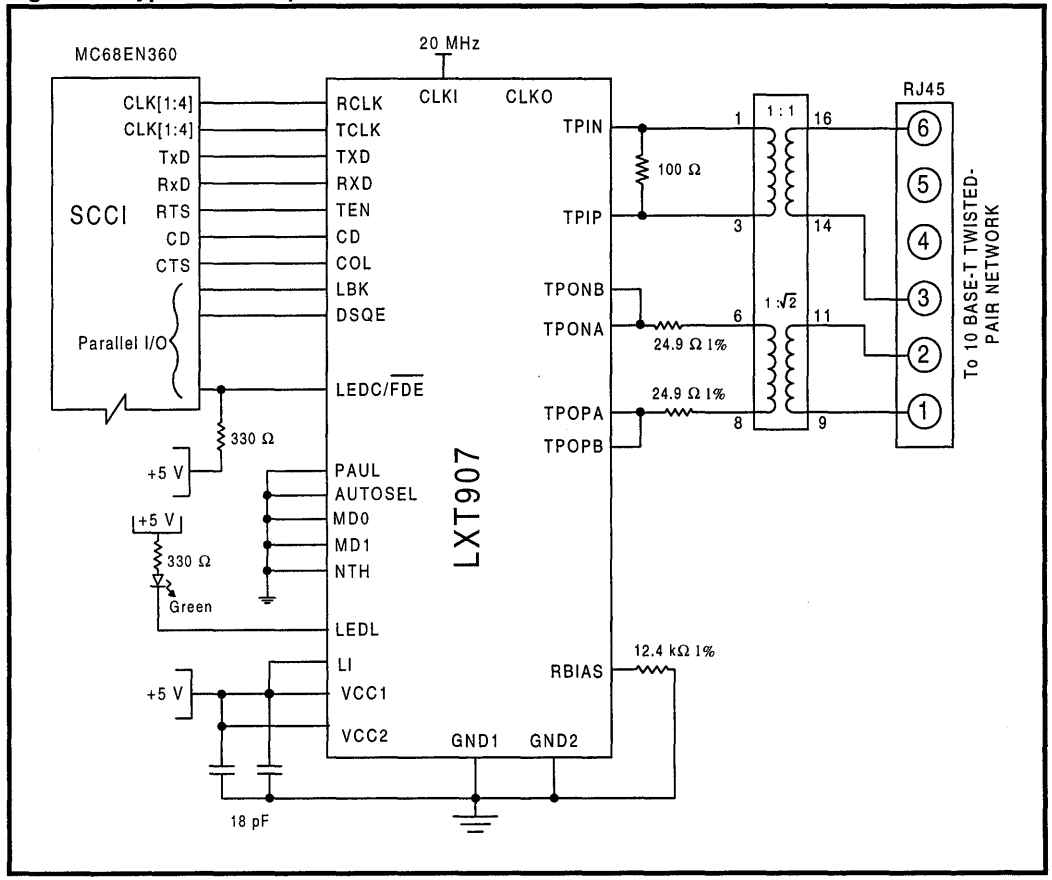
The application on page 1 also requires a 20 MHz clock and several resistors, diodes and capacitors. That example uses the following parts:

- 20 MHz crystal (one each, or external 20 MHz clock)
- 300 Ω, 1% resistor (four each)
- 50 Ω, 1% resistor (two each)
- 75 Ω, 1% resistor (two each)
- 78 Ω, 1% resistor (three each)
- 37.5 Ω, 1% resistor (two each)
- 12.4 kΩ, 1% resistor (one each)
- 0.1 µF capacitor (three each)
- 20 pF capacitor (two each, required with Xtal only)
- 18 pF capacitor (one each)
- Red LED (three each, optional)
- Green LED (one each, optional)

Table 2: Transformer Manufacturers

Mfgr	Part Number	TP/AUI
Bel Fuse	S553-0716/A553-0716	TP
	A553-0756/S553-0756	AUI
Fil-Mag	23Z128/23Z128	TP
	23Z90/23Z90SM	AUI
HALO Electronics	TD42-2006Q	TP
	TG42-2006WH1	
	TD01-0756K	AUI
	TG01-0756W	
Valor	PT4069/SM4069	TP
	LT6030/SM6030	AUI

Figure 1: Typical Full Duplex 10BASE-T Connection



JULY, 1997
Revision 1.1

Design Guide for LXT914 Quad Ethernet Repeater with the LXT901/904/907 and Motorola MC68EN360

General Description

This application note describes a method for integrating the LXT914 Quad Ethernet Repeater into existing and new architectures using the MC68EN360 (QUICC) device. It also includes the design notes for the MC68EN360 and the LXT901/7 found in Application Note 35 for new users of Level One devices who also use the QUICC interface. The LXT914 has a new advanced feature set which allows integration of the repeater function with existing QUICC/LXT901/7 designs.

The QUICC/LXT90X/LXT914 device combination demonstrates Level One's commitment to supplying highly integrated solutions to meet our customers' ever increasing requirements for advanced new products.

LXT914 Advanced Feature Set

- Three new LED operating modes
- Selectable AUI interface (DTE/MAU)
- Four integrated 10BASE-T transceivers
- Integrated transmit and receive filters
- Seven integrated LED drivers
- Synchronous or Asynchronous inter-repeater backplane operation
- Inter-repeater backplane supports glueless cascading of repeater devices for maximum port count
- Serial port interface for initial port configuration
- Packaged in both 68-pin PLCC and 100-pin PQFP

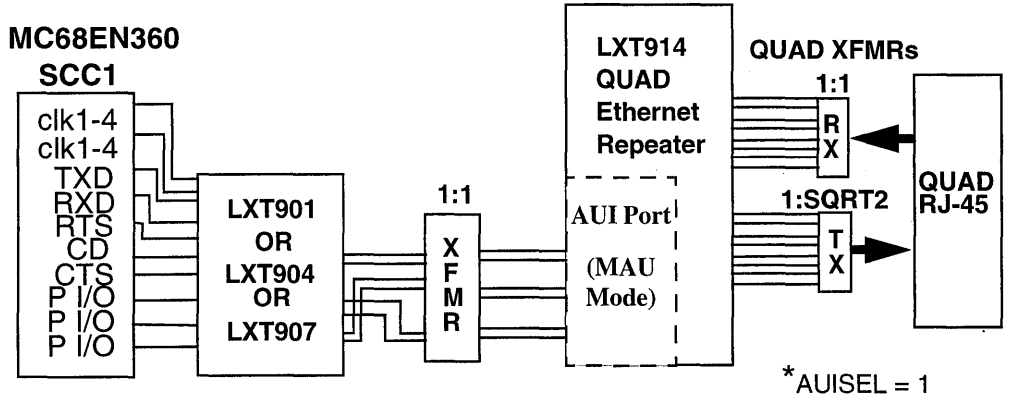
Application Overview

The LXT914 Flexible Quad Ethernet Repeater can be used to increase the connectivity of your current and future designs, including Routers, Bridges, Print Servers, etc. Any single port Ethernet design can be upgraded to a multi-port repeated network simply and easily using the LXT914 device with the new advanced feature set.

The LXT914's advanced feature set includes three new LED modes and the selectable AUI interface (DTE/MAU).

The LXT914 AUISEL pin allows the designer to select the MAU interface mode of operation. The MAU mode allows for the connection of the DTE interface of the LXT901/4/7 with the MAU interface of the LXT914. This application will increase the connectivity of the product from one port to 4, 8, or 12 TP ports. The LXT914 advanced feature set also allows for growth from LED managed to a fully managed solution.

LXT914 Integrated Ethernet Repeater Block Diagram



DESIGN REQUIREMENTS

LXT90X - QUICC Compatibility

The LXT901, LXT904 and LXT907 devices are each available in a 44-pin PLCC package. There are functional differences between the three devices, but each product has all of the features required for compatibility with the QUICC in this application. The LXT907, for example, uses pin 37 for the DSQE function, allowing the designer to make SQE a programmable option in the design. The LXT901 uses pin 37 for UTP/STP media selection. These device-specific options apply to the use of the TP port which is unused in this application. The LXT904 device has only the single AUI port—the only port required for this application. Refer to the Level One data sheet for the specific device to fit your individual requirements.

LXT90X - LXT914 Connections

The LXT901/4/7 device should be set up in a fixed mode of operation. This fixed mode of operation reduces the number of required programmable pins. The mode selected for operation with the LXT914 is: Autoselect disabled, LI disabled, and PAUI set (for AUI only operation).

The actual connection between the LXT901/4/7 and the LXT914 is shown in Figures 1 and 2, which detail the two interface options: capacitive coupling and isolation transformers, respectively. Capacitive coupling is used for like-biased devices. Some devices will require transformers. The AUI circuitry has voltage biasing on all lines and requires isolation when transmitting between devices. Either option also requires the 78.7 Ω termination resistors on both sides of the transformer or the capacitive coupling as shown in Figures 1 and 2.

NOTE

Some existing designs may require reprogramming.
The programmable pins should be set as follows:
AUTOSEL = Low: Auto Port Select disabled
LI = Low: Link Integrity Test disabled
PAUI = High: AUI Port selected
MD0 = Low: Controller Mode 1 selected
MD1 = Low: Controller Mode 1 selected

The following pins on the LXT901/4/7 connect to MC68EN360 SCC1 signals.

Table 1: Connections to QUICC SCC1

LXT90X Pin #	LXT90X Signal Name	Motorola QUICC MC68EN360 SCC1 Signal
28	RCLK	CLK1-4[1]
11	TCLK	CLK1-4[1]
12	TXD	TXD
26	RXD	RXD
13	TEN	RTS
27	CD	CD
16	COL	CTS
22	LBK	PI/O1[2]
4	NTH	PI/O2[2]
37	UTP(901)	PI/O3[2]
37	DSQE(907)	PI/O3[2]

1. The design must provide separate clocks for TCLK & RCLK. Any of the clocks on the QUICC will do.
2. Please refer to the Motorola specification for the correct connections and desired results. These pins should be programmable output pins for use with TTL inputs. Check the pin's state at reset and power up for compatibility with Level One devices.

Setting QUICC Parameters

Refer to the Motorola MC68EN360 Quad Integrated Communications Controller User's Manual for settings required to operate the QUICC properly. Here are some points to be aware of when setting up the QUICC's internal registers:

- Use SCC1 for the LAN connection, and use another SCC or a parallel port for another remote connection. (Only the SCC1 has Ethernet communications capability.)
- Bypass both the Digital Phase -Locked Loop (DPLL) and Manchester Encoding/Decoding functions for Ethernet operations (This is integrated into the LXT901/4/7).
- Set the TCI (Time Clock Invert) bit high to allow the QUICC to clock the data out to the LXT901 or LXT907 device on the rising edge of the clock pulse. This improves data setup time at the 10 Mbps speed used by Ethernet. TCI is bit 28 of the General SCC Mode Register (GSMR).
- Set the MODE bits (0-3) must to 1, 1, 0, 0. Set both the Transparent Receiver (TRX) and Transparent Transmitter (TTX), bits 43 & 44, to 0 for Normal Operation, or a 1 for Transparent Operation. Do not mix the two signals, set them for the same mode. We recommend the 0 setting: In this mode the QUICC does not manipulate the protocols in the data stream.
- Set the Transmit FIFO Length (TFL) bit & the Receive FIFO Width (RFW) bits to 0.
- Set the bits to 0, 1 (Ethernet operation) for a repeating (1,0,1,0,...) pattern as a preamble. GSMR bits 19-20 are Transmit Preamble Pattern (TPP) bits.

LXT914 Configuration

The following is a complete list of the settings as shown in Figure 3. Some of these settings are optional. Select the settings which will be best for your product.

- LOC/$\overline{\text{EXT}}$: Set this bit High (1) for Local Management. (Use External Management to meet the requirement for managed TP port statistics, SNMP protocol or RMON operation with a EMD device.)
- A/$\overline{\text{SYNC}}$: Select Asynchronous mode High (1) to eliminate the need for an external clock source. The Asynchronous and Synchronous modes of operation determine the relationship between the System Clock and the IRB Clock. The IRB clock is internally generated in Asynchronous mode only.
- AUISEL/LEDJM: Pull this pin High (1) for this application. (This pin can be an external LED driver or used as an input to select MAU mode for the AUI port.)
- LEDM1/0: Set these pins for one of four possible LED modes. The available modes are shown in Table 2. In the MAU configuration, Mode 0 and the LEDJM driver are not available with the PLCC package.
- DSQE: Set the disable SQE pin High (1) to disable the SQE function or Low (0) to enable the SQE function.
- FPS: Set the first position pin High (1).
- SDI: Tie this pin Low for the default settings of the internal setup register used here. (Use an external EEPROM to customize the port settings. Refer to the LXT914 data sheet for further information.)
- SCLKIO, $\overline{\text{SENO}}$, $\overline{\text{SENI}}$: Leave the remaining serial management pins floating.
- TEST: Tie this pin Low (0).

Figure 1: AUI Capacitive Coupling Interface

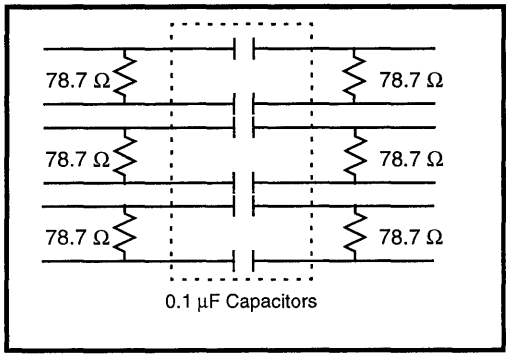


Figure 2: Isolation Transformer Interface

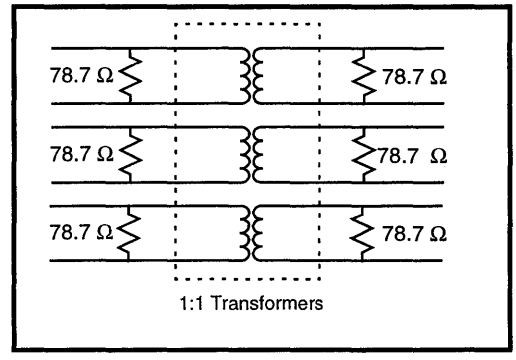


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Table 2: LED Modes Available in the LXT914

Condition (LEDM0, 1)	LEDTP 1-4	LEDAUI	LEDCF
MODE 1 (0, 1)			
1 Steady High	Rx Link Pulse	*n/a*	MJLP
2 Blink High	*n/a*	*n/a*	*n/a*
3 Steady Low	*n/a*	*n/a*	Collision
4 Blink Low	Rx Packet	Rx Packet	*n/a*
MODE 2 (1, 0)			
1 Steady High	Rx Link Pulse	*n/a*	MJLP
2 Blink High	Partition Out	Partition Out	*n/a*
3 Steady Low	*n/a*	*n/a*	Collision
4 Blink Low	Rx Packet	Rx Packet	*n/a*
MODE 3 (1, 1)			
1 Steady High	Rx Link Pulse	*n/a*	MJLP
2 Blink High	Rx Packet	Rx Packet	*n/a*
3 Steady Low	Partition Out	Partition Out	Collision
4 Blink Low	*n/a*	*n/a*	*n/a*

Inter-Repeater Bus (IRB)

The IRB connects multiple LXT914 devices on a single repeated segment. Each repeater device distributes recovered and retimed data to other repeaters on the IRB simultaneously. This simultaneous rebroadcast allows the multiple devices to act as a single large repeated segment.

- $\overline{\text{IRENA}}$, IRDAT, $\overline{\text{IRCOL}}$, $\overline{\text{IRCFS}}$: These four signals must each be pulled up through a single 330 Ω 1% resistor.
- $\overline{\text{IRDEN}}$: This signal controls the transceivers for synchronous mode of operation. The synchronous mode is required for a fully managed solution.

Table 3: Four TP Port BOM (*see Figure 3*)

#	Qty	Description
1	6	.1 µF caps *AC Coupling only*
2	4	120 pF capacitors
3	8	24.9 Ω 1% resistor
4	4	100 Ω resistors
5	4	330 Ω resistors
6	2	12.4 kΩ resistors
7	4	1 kΩ resistors
8	1	1:1 XFMR, *No AC coupling*
9	1	1:1 Rx XFMR (quad)
10	1	1:1.41 Tx XFMR (quad)
11	1	20 MHz Oscillator (or 20 MHz system clock)
12	-	LEDs, user defined

LAYOUT REQUIREMENTS

The Twisted-Pair Interface

The four twisted-pair output circuits are identical. Each TPDOP/TPDON output pair has a 24.9 Ω, 1% resistor in series at each output pin and a 120 pF capacitor across the output lines. These signals go directly to a 1:$\sqrt{2}$ transformer creating the necessary 100 Ω termination for the cable. The TPDIP/TPDIN signals have a 100 Ω resistor across the differential pairs to terminate the 100 Ω signal from the line. To calculate the impedance on the output line interface, use the formula:

$$(24.9\ \Omega + 24.9\ \Omega) * \sqrt{2}^2 \approx 100\ \Omega.$$

Table 4 lists available quad and single port transformers with manufacturers and their part numbers. This information was valid as of the printing date of this document. Before committing to a specific component, designers should review the specifications for any device to be used in the design.

The layout of the twisted-pair ports is critical in complex designs. Run the differential pairs directly from the device to the discrete termination components (located close to the transformers).

The transformer isolation voltage rating should be 2 kV to protect the circuitry from static voltages across the connectors and cables. The signals running from the transformers to the connector should run in close pairs directly to the connector. Be careful not to cross the transmit and receive pairs. One way to avoid a problem is to run the receive pairs on the component side and the transmit pairs on the solder side.

The PCB layout should have no ground or power planes from the transformers to the connectors. The receive and transmit signals should be the only traces in this area. Place the chassis ground for the connectors near the edge of the PCB, away from the signals, connecting the connector shield within the wide etch of the chassis ground.

RBIAS Pins

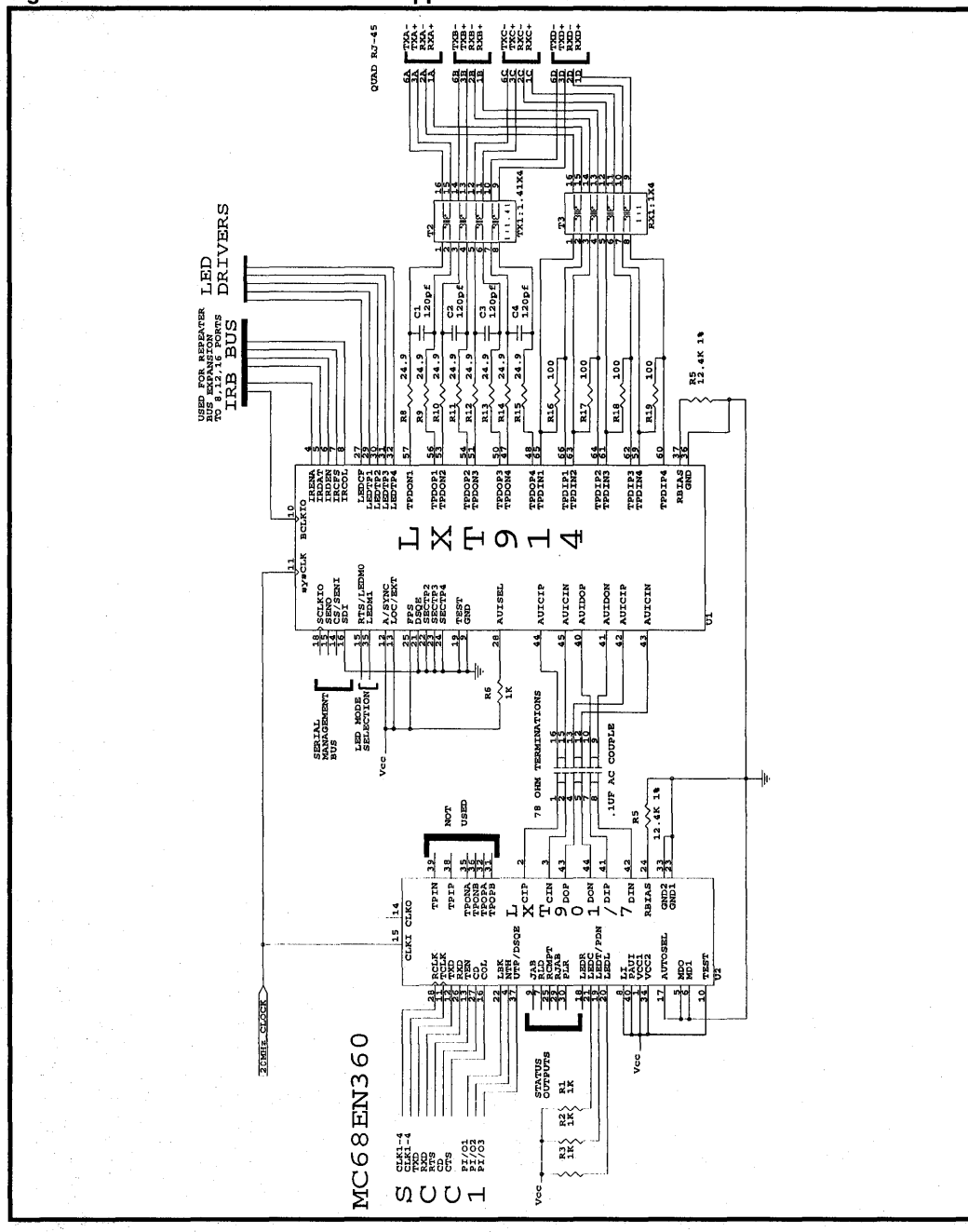
The RBIAS resistor for the LXT901/4/7 devices should be placed as close to the pin as possible with no vias between the device and the resistor (SMT). The other side should share the via with GND1 (pin 23). There should be no other signals running through or under this area. The RBIAS signal sets the levels for the output drivers of the device. Emissions or common mode noise entering the device here will be seen on the output signals.

Lay out the LXT914 device with a 12.4 kΩ, 1% resistor directly connected to pin 37. The ground signals from pins 36 & 38 should come directly off of the device to surround the resistor and pin forming a partition between the RBIAS resistor and the other signals on the PCB.

Table 4: Manufacturers Magnetics List

Manufacturer	Quad Transmit	Quad Receive	Tx/Rx Pairs
Bell Fuse	S553-5999-02	S553-5999-03	
Fil-Mag	23Z338	23Z339	
HALO (Octal)	TD54-1006L1 TG54-1006N2	TD01-1006L1 TG01-1006N2	TD42-2006Q TD43-2006K TG42-1406N1 TG43-1406N TG44-S010NX
Kappa	TP4003P	TP497P101	
Nanopulse	5976	5977	
PCA	EPE6009	EPE6010	
VALOR	PT4116	PT4117	PT4069N1 PT4068N1 ST7011S2 ST7010S2

Figure 3: QUICC-LXT901/4/7-LXT914 Application Schematic



APRIL, 1996
Revision 1.0

MAC Interface Design Guide

Interfacing Level One Ethernet Transceivers to Intel Controllers

General Description

This application note describes operation of the Intel 82596 LAN coprocessor with Level One Ethernet transceivers for IEEE 802.3 10BASE-T and AUI connections. The 82596 can be used with a variety of Level One devices including the LXT901, LXT904, LXT905, LXT907 and LXT944. The 82596 performs the Medium Access Control (MAC) functions, while the Level One transceivers perform the Physical (PHY) layer functions of Manchester encoding/ decoding, receiver squelch and transmit pulse shaping, jabber, link integrity testing, reversed polarity detection and correction, and AUI driving and receiving. This note details the transceiver-to-controller interface. It also describes the Carrier Sense mode settings required for compatibility between Level One LXT905 and LXT944 transceivers and the Intel 82596 LAN controller.

Features

- Integrated filters - No external filters required
- Integrated Manchester encoders/decoders
- 10BASE-T compliant transceivers
- AUI transceivers
- Automatic /Manual AUI/RJ45 Selection
- Automatic polarity correction
- SQE enable/disable
- Integrated LED drivers
- Full duplex capability

Consult individual product data sheets for specific product feature sets.

Application Overview

CSMA/CD or Full-Duplex Ethernet

The above listed Level One transceivers are capable of full duplex operation. This makes them an excellent choice for use with the Intel 82596. The 82596 has two link management algorithms. One of these is Carrier Sense Multiple Access with Collision Detection (CSMA/CD) for compliance with the IEEE 802.3 standard. In CSMA/CD operation, the presence of activity on the serial link delays any data transmission until the link is clear. Collisions can be detected internally or externally to the 82596. With external collision detection, the 82596 is notified of collisions by the COL output of the Level One transceiver.

In addition to CSMA/CD, the 82596 is capable of full-duplex communication. In full-duplex operation, the 82596 uses the $\overline{\text{RTS}}$ output to enable data transmission through the TEN input of a Level One transceiver. In order for Level One transceivers to operate in full duplex mode, the transceiver collision detect circuits must be disabled. Collision detection disable is performed through the LEDC pin on the transceiver. In half-duplex operation (for CSMA/CD), the LEDC pin is an output for driving a collision indicator LED. Externally tying the LEDC pin low disables internal twisted-pair loopback and collision detect, enabling full-duplex communication.

Full-duplex operation effectively doubles the bandwidth of an Ethernet connection, without any change in the physical media.

TRANSCEIVER TO CONTROLLER INTERFACE

Level One transceivers use an 8-pin interface to connect with LAN controllers. Table 1 describes the connections between Level One transceivers and the 82596. Note that the CD output from the transceiver is not used with the 82596 controller.

Table 1: Transceiver Pin Description and 82596 Connections

Transceiver Pin Name	I/O	Signal Name	Signal Description	82596 Pin Name
TXD	I	Transmit Data	Input signal containing NRZ data to be transmitted on the network. TXD is connected directly to the transmit data output of the controller.	TXD
TEN	I	Transmit Enable	Enables data transmission and starts the watchdog timer. Synchronous to TCLK.	$\overline{RTS}$
TCLK	O	Transmit Clock	10 MHz clock output. This clock signal should be directly connected to the transmit clock input of the controller.	$\overline{TXC}$
RCLK	O	Receive Clock	Recovered 10 MHz clock which is synchronous to the received data and connected directly to the receive clock input of the controller.	$\overline{RXC}$
RXD	O	Receive Data	Output signal connected directly to the receive data input of the controller.	RXD
CD	O	Carrier Detect	Output to notify the controller of activity on the network. **Do not connect** when using an Intel 82596 with either an LXT905 or LXT944.	$\overline{CRS}$
COL	O	Collision Detect	Output which drives the collision detect input of the controller.	$\overline{CDT}$
LBK	I	Loopback	Enables internal loopback mode.[1]	$\overline{LPBK}$

1. Loopback is an optional connection. Both devices recognize Loopback, but it is not necessary for normal operation.

Carrier Sense Mode Settings

The Intel 82596 LAN controller offers two modes for the carrier sense function: Internal and External. Mode compatibility is listed in Table 2. The LXT901, LXT904 and LXT907 can be used with either mode. The LXT905 and LXT944 can be used with the Internal Mode only.

In the Internal Carrier Sense mode the external carrier sense on the 82596 $\overline{CRS}$ pin is ignored. Instead, the presence of the receive clock is interpreted as Carrier Sense active. Therefore, the Carrier Detect output from the transceiver is not required and should not be connected to the controller. To set the 82596 controller to the Internal Carrier Sense mode, use the configure command to set the 82596 configuration parameter CARRIER SENSE SOURCE (Byte 9, Bit 3) to 1.

In the External Carrier Sense mode the controller looks at the Carrier Detect signal from the transceiver. In the LXT905 and LXT944, the delay between the end of frame and the de-assertion of Carrier Detect can cause the 82596 to mis-read several bits. Selecting the Internal Carrier Sense mode eliminates this condition.

Table 2: Carrier Sense Mode Compatibility

Transceiver	Internal	External
LXT901	Yes	Yes
LXT904	Yes	Yes
LXT905	Yes	No
LXT907	Yes	Yes
LXT944	Yes	No

APRIL 1997
Revision 1.0

LXT905 MAC Interface Update

End-of-Frame Timing Issues

Introduction

Level One has determined that LXT905 Revision C1 compatibility with certain Medium Access Controller (MAC) chips is affected by End-of-Frame timing variations. This compatibility issue can result in excessive CRC errors at End-of-Frame. This Application Update provides solutions to the End-of-Frame compatibility issue.

Background

One of the events associated with receipt of an End-of-Frame is CD (Carrier Detect) de-assertion. The timing of this event (CD de-assertion) varies, relative to RCLK.

Some MAC devices check CD at the end of every byte (every 8 bits). In this case, variation of the CD de-assertion timing does not impact MAC operation. However, other MAC devices check CD at every bit. In this case, variation of the CD de-assertion timing can cause the MAC to miss the last bit of the CRC, resulting in a CRC error.

If you have been using the LXT905 without problems, it is likely that your MAC is not sensitive to this issue. At present, only controllers from Motorola and Intel are known to be susceptible to the CD de-assertion timing variation.

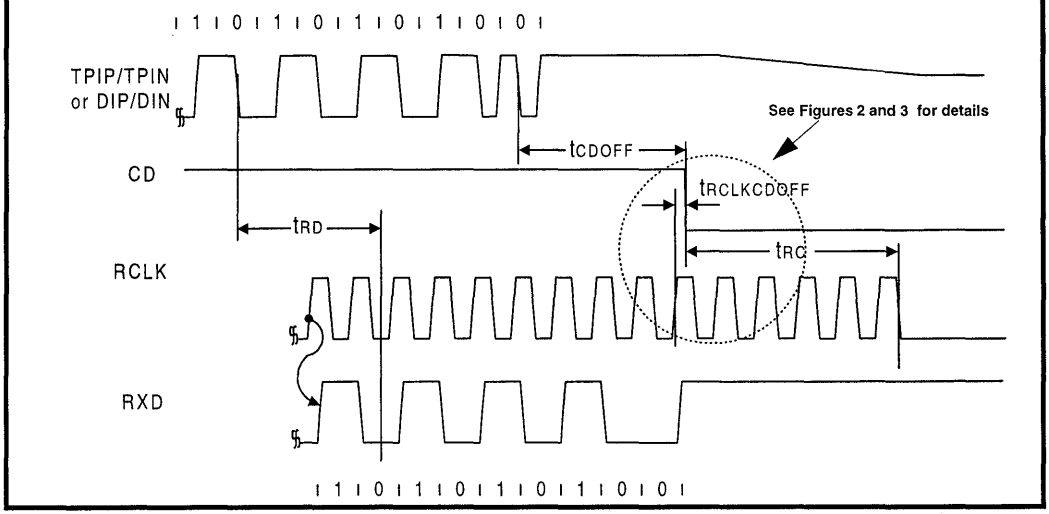
End-of-Frame Timing

CD turn-off delay (t_{CDOFF}) is a timing parameter associated with receipt of an End-of-Frame. As shown in Figure 1 below, CD turn-off delay is the time between the falling edge in the middle of the last Manchester encoded signal (always a zero) and the transition edge of the CD line. (The CD transition may be falling or rising, depending on the controller mode.)

The "C1" revision of the LXT905 (in production since January, 1996) has significant variation in the length of t_{CDOFF}. The delay time is consistently below the specified maximum, but the position of the CD transition varies widely, and is dependent on the incoming data stream pattern that precedes the end of frame.

Data Sheet Reference Note:
The LXT905 data sheet shows t_{CDOFF} timing for each controller mode in Figures 11, 15, 19, and 23. Table 9 of the data sheet gives maximum values of t_{CDOFF} for each of the 4 operating modes. Note that there is a maximum value specified for this parameter, but no minimum.

Figure 1 LXT905 End-of-Frame Timing



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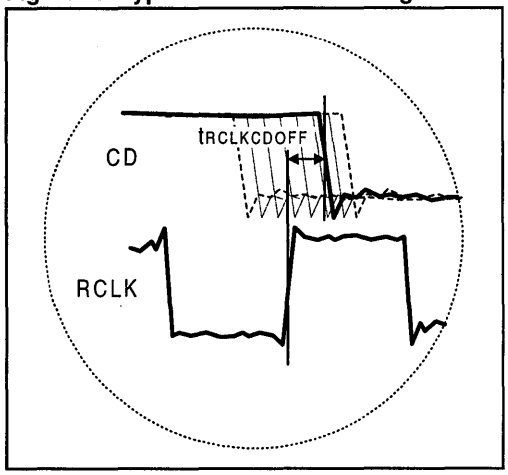
The Critical Relationship

A related parameter, not specified in the data sheet, is the time between the rising edge of the RCLK pulse associated with the last bit (zero) of the End-of-Frame sequence and the transition edge of CD as it is de-asserted. Figure 1 shows the End-of-Frame timing relationships and identifies this parameter as tRCLKCDOFF. This hold time between RLCK and CD off, tRCLKCDOFF, has a typical value of 27 ns.

Figure 2 shows a close-up detail of this parameter. Variation in CD de-assertion is indicated by the dashed lines on the falling edge. As CD de-assertion is shifted left, tRCLKCDOFF is correspondingly reduced and may become negative.

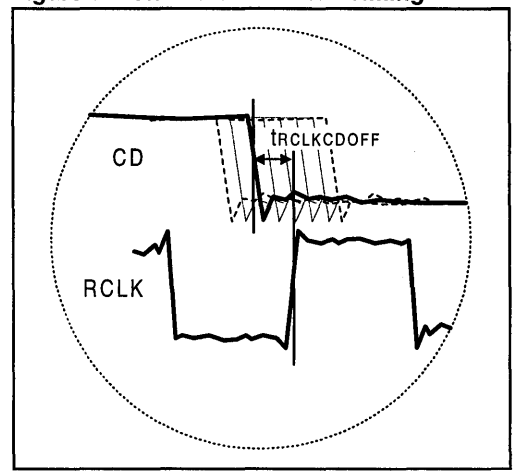
Figure 2: Typical tRCLKCDOFF Timing



When tRCLKCDOFF goes negative, the RLCK edge which normally precedes CD de-assertion now comes after CD de-assertion. This condition (Figure 3) presents compatibility problems with certain MAC chips from Intel and Motorola.

Note that the variation in the timing of CD depends primarily on the data preceding the end-of-frame sequence, but is consistent across devices. If you have been using the LXT905 without problems, it is likely that your MAC is not sensitive to this issue. At present, only controllers from Motorola and Intel are known to be susceptible to the CD de-assertion timing variation.

Figure 3: Shifted tRCLKCDOFF Timing



The Solution for Intel MACs

Use the MAC's Internal Carrier Sense mode.

The Intel 82596 LAN controller offers two modes for the carrier sense function: Internal and External. Selecting the Internal Carrier Sense mode eliminates the incompatibility. To set the MAC to Internal Carrier Sense mode, set Carrier Sense Source (Byte 9, bit 3) = 1.

In this mode the external carrier sense on the 82596 "$\overline{\text{CRS}}$" pin is ignored. Instead, the presence of the receive clock is interpreted as Carrier Sense active. Therefore, the output from the LXT905 Carrier Detect pin is not required and should not be connected to the controller. Refer to Level One Application Note AN51 for details.

The Solution for Motorola MACs

Use the LXT905's Controller Compatibility Mode 4.

To provide compatibility with the Motorola MAC, the $t_{RCLKCDOFF}$ characteristic has been changed on a new "C2" revision of the LXT905. Table 1 summarizes the differences between the C1 and C2 revisions with respect to this issue.

Data Sheet Reference Note:
The Motorola MC68EN360 controller requires a minimum of 10 ns for $t_{RCLKCDOFF}$. This is specified in Table 10.26 on page 10-77 of the MC68360 User's Manual, MC68360UM/AD Rev. 1, parameter number 125, "RENA Active Delay (from RCLK1 rising edge of the last data bit)". Note that CD on the LXT905 data sheet corresponds to RENA on the Motorola data sheet (also referred to as "NOT CD1" in some Motorola documentation).

Table 1: $t_{RCLKCDOFF}$ Timing in LXT905 for Mode 1 and Mode 4

Mode	$t_{RLCKCDOFF}$			
	Minimum	Typical	Maximum	Units
1	-10	27	30	ns
4	40	77	80	ns

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NOTES

Transformer Manufacturers

for Level One Networking Product Applications

Transformer Manufacturers

Table 1: Twisted-Pair Transformer Manufacturers

Product	Port & Ratio	Manufacturer	Transformer Part Numbers
LXT901/901A	Rx = 1:1	Bell Fuse	S553-0716, A553-0716
LXT907/907A	Tx = 1:√2	Fil-Mag	23Z128, 23Z128SM
		HALO	TD42-2006Q, TG42-1406N1
		Valor	PT4069, ST7011
LXT902	Rx = 1:1	Fil-Mag	78Z1122B-01, 78Z1122D-01
LXT906	Tx = 1:1	Valor	PT3877
		HALO	FD02-101G, FD12-101G, FD22-101G
LXT905	Rx = 1:1	Fil-Mag	23Z441, 23Z441SM, 23Z118, 23Z118SM
LXT908	Tx = 1:2	HALO	TD75-1406N, TG74-1406N1
		Valor	ST4160, ST4202, ST4167, ST4152, PT4152
LXT970	Rx = 1:1	HALO	TG22-3506ND, TD22-3506G1, TG22-S010ND, TG22-S012ND
	Tx = 1:1	Nanopulse	NPI 6120-30, NPI 6120-37, NPI 6170-30, NPI 6181-37
		Pulse	PE-68517, PE-68515
		Valor	ST6114, ST6118
LXT914	Quad Txfmr	Bel Fuse	A553-5999-01, S553-5999-02
LXT915	Tx = 1:√2	Fil-Mag	23Z339, 23Z339SM
LXT916		HALO	TD54-1006L1, TG54-1006N2
LXT917		Kappa	TP4003P
LXT918		Nanopulse	5976
LXT944		PCA	6038, EPE6009
		Valor	PT4116
	Quad Txfmr	Bel Fuse	A553-5999-00, S553-5999-03
	Rx = 1:1	Fil-Mag	23Z338, 23Z338SM
		HALO	TD01-1006L1, TG01-1006N2
		Nanopulse	5977
		PCA	6037, EPE6010
		TDK	TLA-3T106
		Valor	PT4117

Table 2: AUI Transformer Manufacturers

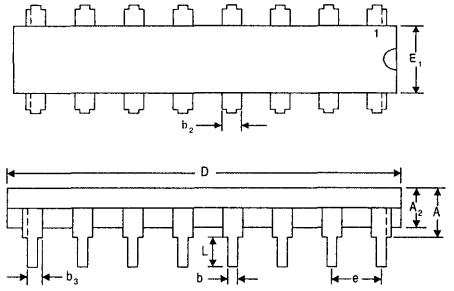
Product	Ratio	Manufacturer	Transformer Part Numbers
LXT901/901A	AUI	Bel Fuse	S553-1006-AE
LXT902	Rx = 1:1	Fil-Mag	23Z90, 23Z90SM
LXT904	Tx = 1:1	HALO Electronics	TD01-0756K, TG01-0756N
LXT906		Valor	LT6032, ST7032
LXT907/907A			
LXT908			
LXT914			
LXT915			
LXT916			
LXT917			
LXT918			

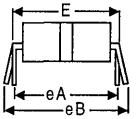
Package Information and Order Information

This section contains a summary of the Package Specifications for Level One Products.

In case of a conflict, the latest issue of the JEDEC publication #95 shall take precedence over these drawings.

Plastic Dual In-Line Package (8-pin, 14-pin, 16-pin, 24-pin, 28-pin, 40-pin DIP)





Dual In-Line Packages (dimension D in lower tables)

Dim	300 mil DIP				600 mil DIP			
	Inches		Millimeters		Inches		Millimeters	
	Min	Max	Min	Max	Min	Max	Min	Max
A	–	0.210	–	5.334	–	0.250	–	6.350
A2	0.115	0.195	2.921	4.953	0.125	0.195	3.175	4.953
b	0.014	0.022	0.356	0.559	0.014	0.022	0.356	0.559
b2	0.045	0.070	1.143	1.778	0.030	0.070	0.762	1.778
b3[1]	0.030	0.045	0.762	1.143	–	–	–	–
E	0.300	0.325	7.620	8.255	0.600	0.625	15.240	15.875
E1	0.240	0.280	6.096	7.112	0.485	0.580	12.319	14.732
e	0.100 BSC[2] (Nominal)		2.540 BSC[2] (Nominal)		0.100 BSC[2] (Nominal)		2.540 BSC[2] (Nominal)	
eA	0.300 BSC[2] (Nominal)		7.620 BSC[2] (Nominal)		0.600 BSC[2] (Nominal)		15.240 BSC[2] (Nominal)	
eB	–	0.430	–	10.922	–	0.700	–	17.780
L	0.115	0.150	2.921	3.810	0.115	0.200	2.921	5.080

Length of 300 mil Packages

Package Type	Dim D	8-pin DIP		14-pin DIP		16-pin DIP		24-pin DIP	
		Min	Max	Min	Max	Min	Max	Min	Max
Full Lead	Inch	–	–	0.735	0.775	0.780	0.800	1.230	1.280
	mm	–	–	18.669	19.685	19.812	20.320	31.242	32.512
1/2 Lead	Inch	0.355	0.400	–	–	0.735	0.775	1.160	1.195
	mm	9.017	10.160	–	–	18.669	19.685	29.464	30.353

Length of 600 mil Packages

Dim D	28-pin DIP		40-pin DIP	
	Min	Max	Min	Max
Inch	1.380	1.565	1.980	2.095
mm	35.052	39.751	50.292	53.213

NOTES:

1. b3 is for 1/2 lead only
2. BSC — Basic Spacing between Centers

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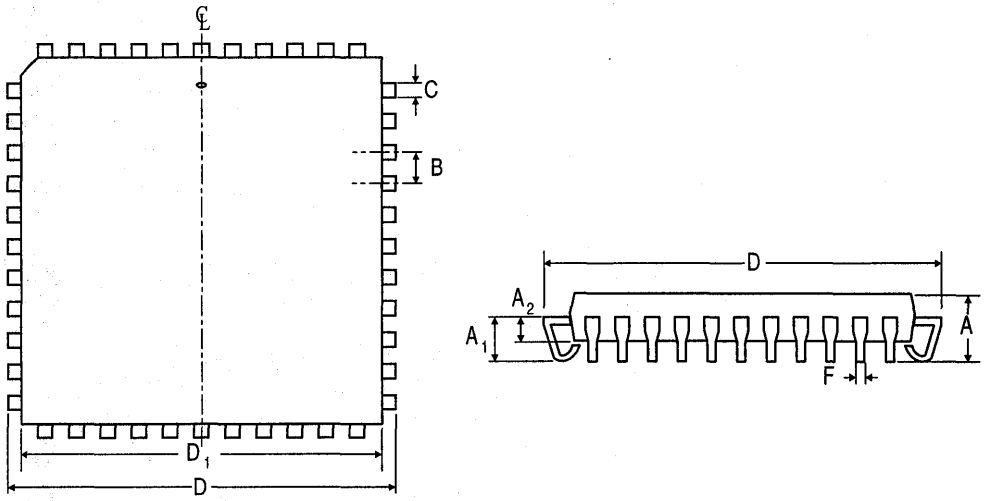
Plastic Leaded Chip Carrier (28-pin PLCC; 44-pin PLCC; 68-pin PLCC)



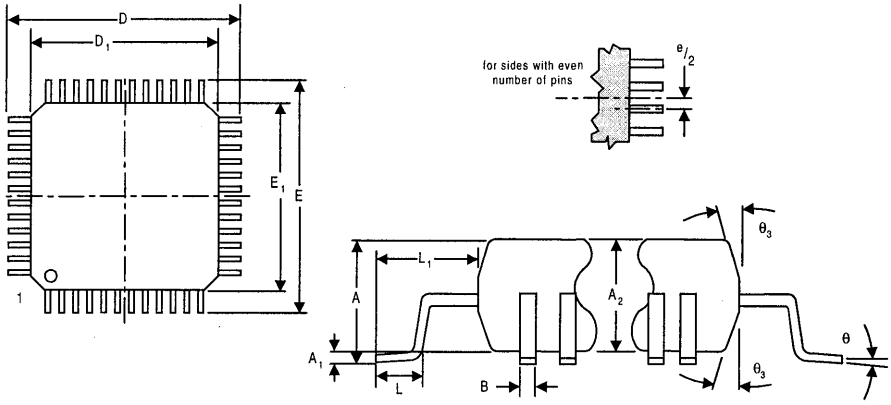
Plastic Leaded Chip Carriers

Dim	Inches		Millimeters	
	Min	Max	Min	Max
A	0.165	0.180	4.191	4.572
A1	0.090	0.120	2.286	3.048
A2	0.062	0.083	1.575	2.108
B	0.050	–	1.270	–
C	0.026	0.032	0.660	0.813
D	See table below		See table below	
D1	See table below		See table below	
F	0.013	0.021	0.330	0.533

Outside Package Size (Dimensions D and D_1)

Dim	28-pin PLCC				44-pin PLCC				68-pin PLCC			
	Inch		Millimeter		Inch		Millimeter		Inch		Millimeter	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
D	0.485	0.495	12.319	12.573	0.685	0.695	17.399	17.653	0.985	0.995	25.019	25.273
D_1	0.450	0.456	11.430	11.582	0.650	0.656	16.510	16.662	0.950	0.958	24.130	24.333

Quad Flat Pack (32-pin LQFP)



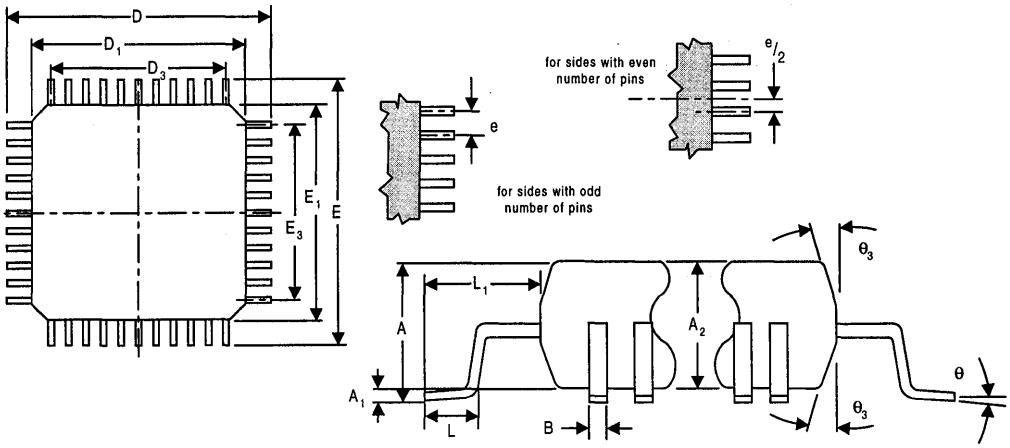
32-Pin Quad Flat Pack (LQFP)

Dim	Millimeters		
	Min	Typ.	Max
A	–	–	1.60
A_1	0.05	0.10	0.15
A_2	1.35	1.40	1.45
B	0.30	0.37	0.45
D		9.00 BSC	
D_1		7.00 BSC	
E		9.00 BSC	
E_1		7.00 BSC	
e		0.80 BSC	
L	0.45	0.60	0.75
L_1		1.00 REF	
θ_3	11 °	–	13 °
θ	0 °	–	7 °

NOTE:

1. BSC — Basic Spacing between Centers

Plastic Quad Flat Pack (44-pin QFP)



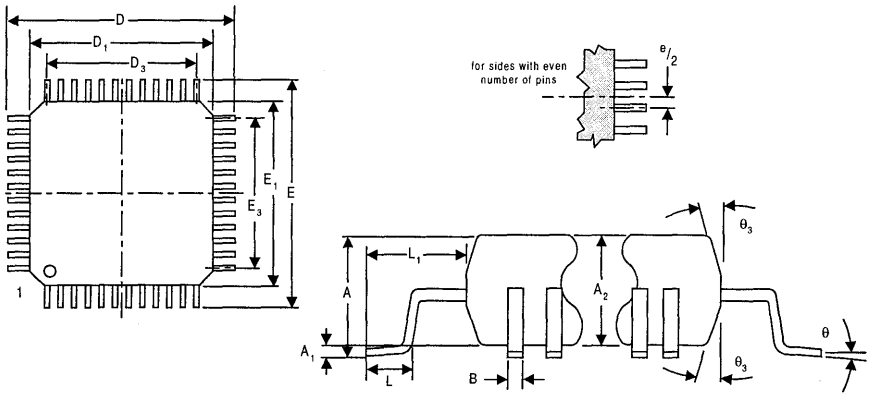
44-Pin Plastic Quad Flat Packs

Dim	Inches		Millimeters	
	Min	Max	Min	Max
A	–	0.096	–	2.45
A_1	0.010	–	0.25	–
A_2	0.077	0.083	1.95	2.10
B	0.012	0.018	0.30	0.45
D	0.510	0.530	12.95	13.45
D_1	0.390	0.398	9.90	10.10
D_3	0.315 BSC[1] (Nominal)		8.00 BSC[1] (Nominal)	
E	0.510	0.530	12.95	13.45
E_1	0.390	0.398	9.90	10.10
E_3	0.315 BSC[1] (Nominal)		8.00 BSC[1] (Nominal)	
e	0.031 BSC[1] (Nominal)		0.80 BSC[1] (Nominal)	
L	0.029	0.041	0.73	1.03
L_1	0.063 REF (Nominal)		1.60 REF (Nominal)	
θ_3	5°	16°	5°	16°
θ	0°	7°	0°	7°

NOTE:

1. BSC — Basic Spacing between Centers

Quad Flat Pack (64-pin QFP)



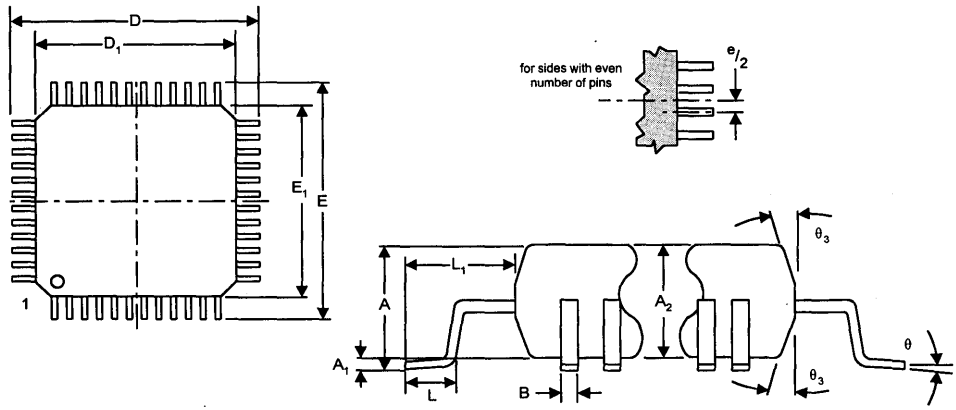
64-Pin Quad Flat Pack (QFP)

Dim	Inches		Millimeters	
	Min	Max	Min	Max
A	–	0.130	–	3.30
A_1	0.000	0.010	0.00	0.25
A_2	0.100	0.120	2.55	3.05
b	0.012	0.018	0.30	0.45
D	0.695	0.715	17.65	18.15
D_1	0.549	0.553	13.95	14.05
D_3	0.472 REF		12.00 REF	
E	0.695	0.715	17.65	18.15
E_1	0.549	0.553	13.95	14.05
E_3	0.472 REF		12.00 REF	
e	0.031 BSC		0.80 BSC	
L	0.029	0.041	0.73	1.03
L_1	0.077 REF		1.95 REF	
θ_3	5 °	16 °	5 °	16 °
θ	0 °	7 °	0 °	7 °

NOTE:

1. BSC — Basic Spacing between Centers

Thin Quad Flat Pack (64-pin LQFP)



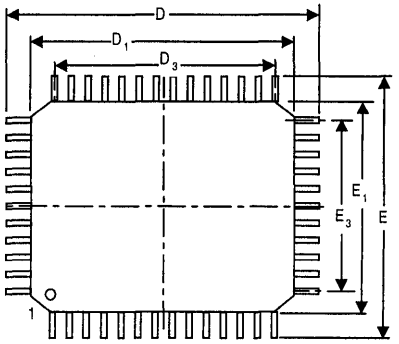
64-pin Thin Quad Flat Pack (LQFP)

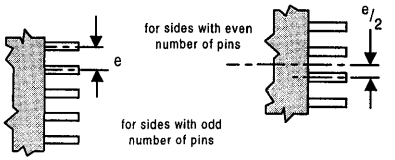
Dim	Inches		Millimeters	
	Min	Max	Min	Max
A		.063	–	1.60
A_1	.002	.006	0.05	0.15
A_2	.053	.057	1.35	1.45
b	.007	.011	0.17	0.27
D	0.472 BSC[1]		12.00 BSC[1]	
D_1	0.394 BSC[1]		10.00 BSC[1]	
E	0.472 BSC[1]		12.00 BSC[1]	
E_1	0.394 BSC[1]		10.00 BSC[1]	
e	0.020 BSC[1]		0.50 BSC[1]	
L	0.018	0.030	0.45	0.75
L_1	0.039 REF		1.00 REF	
θ_3	11°	13°	11°	13°
θ	0°	7°	0°	7°

NOTE:

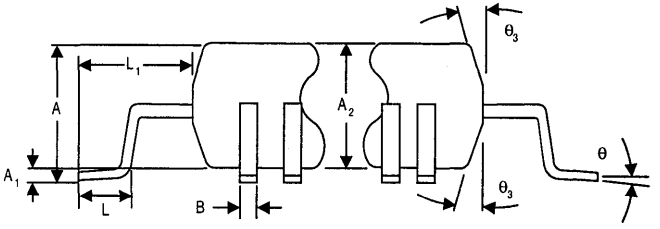
1. BSC — Basic Spacing between Centers

Plastic Quad Flat Pack (100-pin PQFP)





D Side pin count = 30 pins
E Side pin count = 20 pins



100-Pin Plastic Quad Flat Packs (PQFP)

	Inches		Millimeters	
Dim	Min	Max	Min	Max
A	–	0.134	–	3.40
A_1	0.010	–	0.25	–
A_2	0.100	0.120	2.55	3.05
B	0.009	0.015	0.22	0.38
D	0.931	0.951	23.65	24.15
D_1	0.783	0.791	19.90	20.10
D_3	0.742 REF		18.85 REF	
E	0.695	0.715	17.65	18.15
E_1	0.547	0.555	13.90	14.10
E_3	0.486 REF		12.35 REF	
e	0.026 BSC		0.65 BSC	
L	0.026	0.037	0.65	0.95
L_1	0.077 REF		1.95 REF	
θ_3	5°	16°	5°	16°
θ	0°	7°	0°	7°

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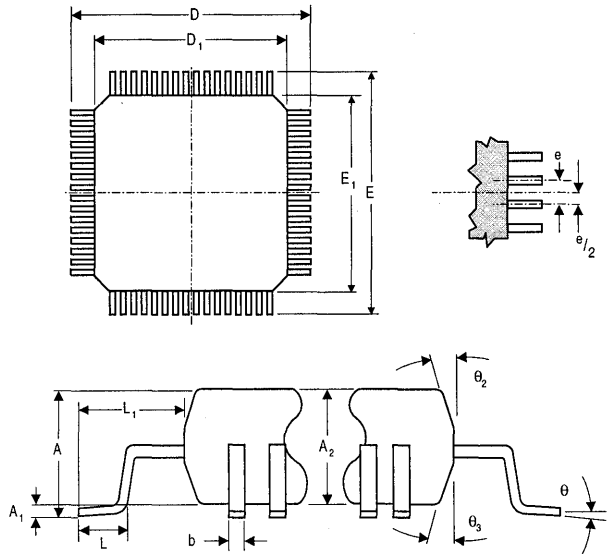
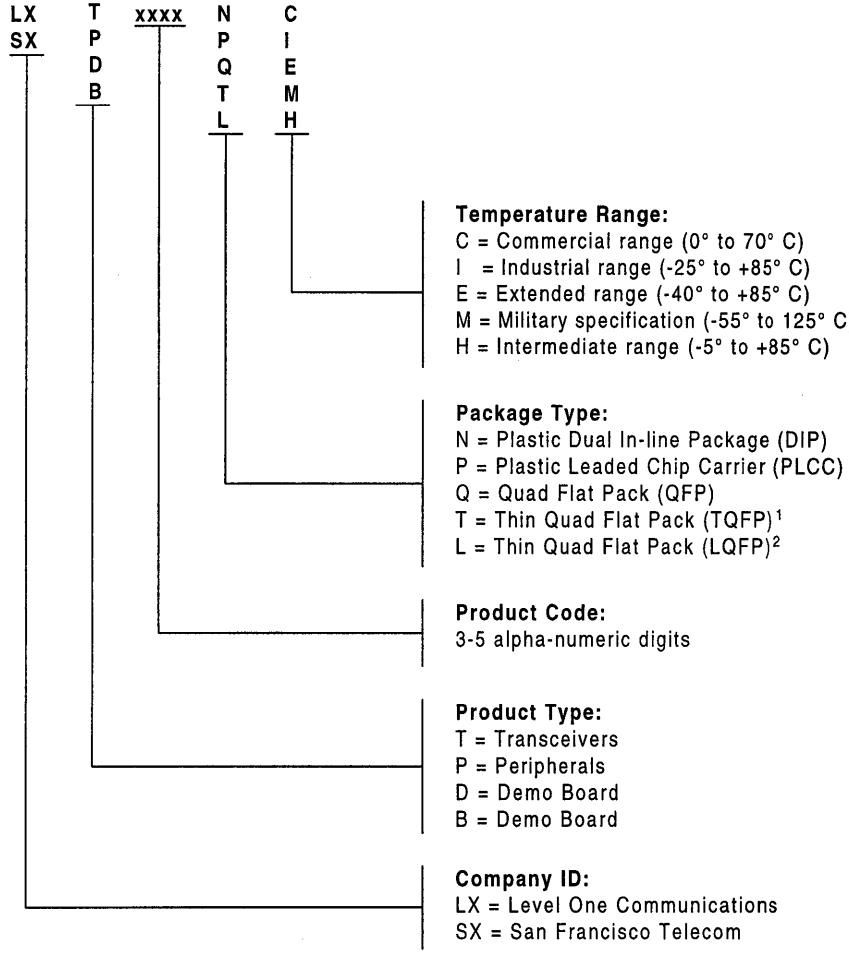
Plastic Quad Flat Pack (208-pin PQFP)



208-Pin Plastic Quad Flat Packs (PQFP)

Dim	Millimeters	
	Min	Max
A	-	4.10
A1	0.25	-
A2	3.20	3.60
b	0.17	0.27
D	30.60 BASIC	
D_1	28.00 BASIC	
E	30.60 BASIC	
E_1	28.00 BASIC	
e	.50 BASIC	
L	0.50	0.75
L_1	1.30 REF	
θ	0°	7°
θ_2	5°	16°
θ_3	5°	16°

ORDERING INFORMATION



Notes:
1. TQFP has a 1 mm body thickness.
2. LQFP has a 1.4 mm body thickness.

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NOTES

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Number/Title	Product / Description	Pages	Pub. Date	Quantity
Data Sheets — Short Haul T1/E1 Transceivers				
LXT300Z/301Z	Advanced Single Transceiver with Receive JA	24	4/96	
LXT304A	Low Power Single Transceiver with Receive JA	20	4/96	
LXT305A	Low Power Single Transceiver with Transmit JA	20	4/96	
LXT307	Low Power E1 Integrated Short Haul Transceiver	24	4/96	
LXT325	Quad Receiver with LOS Output	12	4/96	
LXT332	Dual Transceiver with Crystal-less JA	36	4/97	
LXT331	Dual T1/E1 Line Interface Unit	20	7/97	
LXT334	Quad Short Haul Transceiver w/Clock Recovery	28	5/97	
LXT335	Quad Short Haul PCM Analog Interface	20	6/97	
LXT350/351	Integrated T1/E1 Transceiver with Crystal-less JA	48	7/96	
LXT360/361	Integrated T1/E1 Long Haul/Short Haul Xcvr	52	8/96	
Data Sheets — T1/E1 Long Haul Transceivers				
LXT310	Single T1 Transceiver with Selectable JA	20	4/96	
LXT317	DECT Twisted Pair LIU Transceiver	20	4/96	
LXT318	Single E1 Transceiver with Selectable JA	24	4/96	
LXT360/361	Integrated T1/E1 Long Haul/Short Haul Xcvr	52	8/96	
Data Sheets – Digital Subscriber Line (DSL) Products				
SK70704/70706	784 kbps HDSL Data Pump Chip Set	40	9/96	
SK70704/70707	1168 kbps HDSL Data Pump Chip Set	40	9/96	
SK70720/70721	Multi-Rate DSL Data Pump Chip Set	44	1/97	
Data Sheets — T1/E1 Long Haul/Short Haul Transceivers				
LXT360/361	Integrated T1/E1 Long Haul/Short Haul Xcvr	52	8/96	
Data Sheets — T1/E1 Repeaters				
LXT312/315	Low Power T1 PCM Repeaters	12	4/96	
LXT313/316	Low Power E1 PCM Repeaters	12	4/96	
Data Sheets — T1/E1 Clock Adapters				
LXP600A/2/4	1.544 - 2.048 - 4.096 MHz Adapter	12	4/96	
LXP610	Multi-Rate Selectable Adapter	16	4/96	

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Data Sheets — Wide Area Network Products				
LXT400	Switched 56 / DDS 4-Wire Transceiver	20	4/96	
LXT441	Switched 56 / DDS Integrated DSU / CSU	36	1/97	
Data Sheets —Ethernet PHY Products				
LXT901A/907A	Universal 10BASE-T Ethernet Interface	32	4/96	
LXT902	10BASE-T Ethernet Media Attachment Unit	16	4/96	
LXT904	10BASE-T Ethernet Media Attachment Unit	20	4/96	
LXT905	10BASE-T Transceiver	28	4/97	
	Application Update - MAC Interface	4	4/97	
LXT906	Ethernet Twisted-pair to Coax Adapter	12	4/96	
LXT908	3.3v Universal 10-BASE-T Ethernet Adapter	36	5/97	
LXT944	Quad 10BASE-T Transceiver	28	4/97	
LXT970	Fast Ethernet Transceiver	60	5/97	
Data Sheeets - Ehternet Repeaters				
LXT914	Flexible Quad Hub Repeater	32	4/96	
LXT915	Simple Quad Hub Repeater	24	4/97	
LXT916/917	10BASE-T Repeaters for advanced management	44	12/96	
LXT918	Multi-Segment Hub Repeater	48	5/97	
Data Sheeets — San Francisco Telecom Products				
SXT6234	E-Rate Multiplexer	20	4/96	
Application Notes				
AN21	LXT304A - D4 Channel Bank Applications	4	4/96	
AN23	LXT902/906 - Line Impedance Matching	2	5/96	
AN25	LXT30x/310 - Long-Haul/Short-Haul Commonality	4	4/96	
AN26a	LXT310 - Circuit Protection	4	4/96	
AN29	LXT3xx - Mitel Framer Interface Applications	4	4/96	
AN31a	LXT318 - Migration to Single-chip Long Haul E1 Aps	4	4/96	
AN32	LXT3xx - T1 Jitter Measurement	8	4/96	
AN34	LXT30x/318 - Migration from Short to Long-Haul E1	4	4/96	

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.pplication Notes (continued)				
.N35	LXT901/907 - 68EN360 Controller Applications	4	4/96	
.N36	LXT318 - Long-Haul E1 Line Interface Design	2	4/96	
.N38	LXT332 - Migration from Siemens PEB2236	8	4/96	
.N39	LXT332 - Migration from AT&T 7290	8	4/96	
.N41	Short-Haul Devices - Compliance w/ITU G.775 LOS	4	4/96	
.N42	LXT360/310 - Crystal-less T1 Long haul Solutions	8	4/96	
.N44	E1 Devices - Compliance w/ETSI TBR-12/13	4	4/96	
.N45	LXT914 - 68EN360 Controller Applications	8	4/96	
.N46	LXT300/300Z/304A/305A - Crystal Layout Guide	2	4/96	
.N47	LXT360/361 - Line Protection Circuitry Guide	4	4/96	
.N48	SCR Latch-up - Prevent Latch-up in Transceivers	4	4/96	
.N50	LXT318/360- Crystal-less T1 Long haul Solutions	8	4/96	
.N51	LXT901/904/905/907/944 - MAC Interface Design Guide for Ethernet Transceivers to Intel Controllers	4	4/96	
.N52	Migration from CS61574A/CS61575 to LXT350 Guide	8	8/96	
.N54	Migration from LXT324 to LXT325 Design Guide	2	8/96	
.N55	Universal 120/100/75 Ohm Transceiver Termination for the LXT35x/36x	4	8/96	
.N56	LXT332 - Designing an ITU G.742 Compliant PDH Multiplexer	7	4/97	
.N57	LXT360 - TBR12/13 Compliant Design Solutions	7	4/97	
.N9501	SXT6234 -16 E1/E3 Mux/Demux Applications	12	4/96	
.N9601	SXT6234 -4 data channels E-Rate Multiplexer	4	12/96	
.N60	LXT905 Application Update	4	4/97	

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Number/Title	Product / Description	Pages	Pub. Date	Quantity
Design Notes				
DN3	LXT332 Reference Guide	7	4/97	
T1/E1 Demo Board / Evaluation Kit User Guides				
LDB300	For all single channel LXT3xx family transceivers	12	5/96	
LDB332	For LXT332 Dual Line Interface	12	5/96	
LDB350/360	For LXT350/360 - Demonstration/Evaluation Kit	24	9/96	
LDB70206	HDSL Evaluation Kit for 784 kbps Applications	13	4/96	
LDB70207	HDSL Evaluation Kit for 1168 kbps Applications	13	4/96	
LXDMDSL	MDSL Evaluation Kit for Multi-Rate Applications	20	5/97	
LXD334	Evaluation Board for Quad E1 Applications	20	6/97	
SDB6234	For SXT6234 E-Rate Multiplexer	16	5/96	
Quality and Reliability				
Reliability	Periodic report covers all Level One products	64	4/97	
Qualification	Individual reports - Order by product/package type	various	various	
General Information				
Fact Sheet	Corporate Backgrounder	4	4/96	
Sales Locations	Level One Sales, Distributor and Corporate offices	4	4/96	
Product Reference	Short Form Catalogue of Level One Products	52	4/97	
1996 Data Book	Complete Product Listing	800	7/96	
1996 Data Book CD-ROM	Complete Product Listing on CD for Windows 3.1/95, Macintosh, Sun, HP, Silicon Graphics	—	9/96	

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Wyle Electronics
451 East 124th Street
Thorton, CO 80241
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Wyle Electronics
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St. Petersburg, FL 33716
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Marshall Industries
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Austin, Texas 78759
Telephone: (512) 346-6331
Fax: (512) 346-1975

Texas
Oasis Sales, Inc.
Telephone: (602) 277-2714
Fax: (602) 263-9352
(El Paso)

Utah
Thorson Rocky Mountain, Inc.
5505 So. 900 E., Suite 140
Salt Lake City, Utah 84117
Telephone: (801) 264-9665
Fax: (801) 264-9881

Vermont
New Tech Solutions, Inc.
Telephone: (617) 229-8888
Fax: (617) 229-1614

Virginia
Third Wave Solutions, Inc.
Telephone: (410) 290-5990
Fax: (410) 381-5846

West Virginia
Great Lakes Group
Telephone: (614) 885-6700
Fax: (614) 885-6701
(Western West Virginia)

West Virginia
Third Wave Solutions, Inc.
Telephone: (410) 290-5990
Fax: (410) 381-5846
(Eastern West Virginia)

Washington
Trinity Technologies, Inc.
Telephone: (206) 440-3059
Fax: (206) 364-6739

Wisconsin
Beta Technology Sales, Inc.
150 N. Sunnyslope Road, Suite 365
Brookfield, Wisconsin 53005
Telephone: (414) 797-7977
Fax: (414) 797-8051
(Eastern Wisconsin)

Wisconsin
Russell and Associates
8030 Cedar Ave. South, Suite 114
Minneapolis, Minnesota 55425
Telephone: (612) 854-1166
Fax: (612) 854-6799
(Western Wisconsin)

Wyoming
Thorson Rocky Mountain, Inc.
Telephone: (303) 773-6300
Fax: (303) 773-6302

Sales Representatives (Canada)

Alberta
Electro Source Inc.
2635 37th Avenue NE, Suite 245
Calgary, Alberta T1Y 5Z6
Telephone: (403) 735-6230
Fax: (403) 735-0599

British Columbia
Electro Source Inc.
6875 Royal Oak Avenue
Burnaby, British Columbia V5J 4J3
Telephone: (604) 435-2533
Fax: (604) 435-2538

Ontario
Electro Source Inc.
230 Galaxy Boulevard
Rexdale, Ontario M9W 5R8
Telephone: (416) 675-4490
Fax: (416) 675-6871

Ontario
Electro Source Inc.
300 March Road, Suite 203
Kanata, Ontario K2K 2E2
Telephone: (613) 592-3214
Fax: (613) 592-4256

Quebec
Electro Source Inc.
6600 Trans-Canada Hwy, #420
Pointe Claire, Quebec H9R 4S2
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Fax: (514) 630-7421

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Europe

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A-1239 Vienna
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Intl. Telephone: +43 1 61066 0
Fax: 01 61066 10
Intl. Fax: +43 1 6106610
Email: 100532.716@compuserve.com
also: Czech, Hungary, Slovinia, Slovakia, Croatia

Benelux
- Stocking Representative
D & D Electronics
VIIe Olympiadelaan 93
2020 Antwerpen
Telephone: +32 3 827 79 34
Fax: +32 3 828 72 54
Email: dad@glo.be

Denmark
- Stocking Representative
C-88 AS
Kokkedal Industripark 101
Kokkedal, DK-2980
Telephone: +45 70 10 48 88
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Email: c88@c88.dk
Internet-Homepage: www.c88.dk

Finland / Baltics
- Stocking Representative
Bexab Finland OY
Asemakuja 2 A
Fin-02770, Espoo
Telephone: +358 9 752 76630
Fax: +358 9 752 76655
Email: acte@acte.fi

France
- Stocking Representative
MISIL Technologies
2, Rue de la Couture, Silic 301
Rungis Cedex, 94588
Telephone: +33 1 - 45 60 0021
Fax: +33 1 - 45 60 0186
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Germany
- Stocking Representative
Scantec GmbH
Behringstrasse 10
D-82152 Planegg/Munchen
Telephone: +49 89-89 91 43-0
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Internet-Homepage: www.scantec.de
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- Sales Representative
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73230 Kirchheim/Teck
Telephone: +49 7021-97 93 21
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Germany
- Sales Representative
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Telephone: +49 911-9578037
Fax: +49 911-9578039
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Germany
- Sales Representative
Scantec GmbH
D-71394 Kernen / Stuttgart
Rommelesweg 28
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- Sales Representative
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- Sales Representative
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D-25456 Quickborn/Hamburg
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Greece
- Sales Representative
ATEX Electronics S.A.
Elia Eliou 31
Athens 117 43
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Fax: +30 1 9017024
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Israel
- Stocking Representative
Seg Tec
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Italy
- Stocking Representative
ESCO ITALIANA S.p.A.
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Norway
Northern Europe Regional Office
Torshamnsgatan 35
164 40 Kista/Stockholm, Sweden
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Poland
- Sales Representative
Amber Group, Inc.
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Telephone: +48 22 619-8900
Fax: +48 22 189 546
Email: AmberGrp@aol.com

- Distributor
Amber Group, Inc.
70 Birmingham Parkway
Boston, Massachusetts 02135
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Europe cont.

Russia / Belarus / Ukraine
- Sales Representative
BelElectronComplect Co., Ltd.
27, Bagriany Sidestreet
220137 Minsk, Belarus
Telephone: (+375) 17 2436971
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Email: admin@bec.minsk.by

Spain
- Stocking Representative
AQL electronica, s.a.
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Telephone: +34 1 467 75 12
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- Stocking Representative
EGEVO Elektronik AB
Box 8100
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Switzerland
- Stocking Representative
Eurodis Electronic AG
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- Distributor
Manhattan Skyline Ltd.
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ACD
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Fax: +91 40-815321

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- Representative & Distributor
Macnica
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4-2-10 Odori, Utsunomiya City, 320
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Fax: +81 286-27-5274

Japan
- Representative & Distributor
Macnica
Shin-Osaka Kimura Daiichi Bldg.
5-11-8 Nishi-Nakashima,
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- Representative & Distributor
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Nagoya City, 461
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Fax: +81 52-933-4542

Japan
- Representative & Distributor
Macnica
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1-22-2 Hakusan, Midori-Ku
Yokohama City, 226
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Korea
- Representative
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- Sales Representative
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Fax: +64 4 564 4998

New Zealand
- Sales Representative
ACD
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Penrose, Auckland
Telephone: +64 9 636 5984
Fax: +64 9 636 5985

New Zealand
- Sales Representative
ACD
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Christchurch
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Fax: +64 3 379 3072

Peoples Republic of China
- Distributor
Sunny Comm, Inc.
395 West El Camino Real - 2nd Floor
Sunnyvale, CA 94087
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Fax: (408) 739-7782

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- Sales Representative
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- Representative & Distributor
Achieva Components Pte. Ltd.
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- Representative
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Level One Communications, Inc.

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